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IEEE Standard for Ethernet

IEEE Computer Society

Developed by the
LAN/MAN Standards Committee

IEEE Std 802.3™-2022
(Revision of IEEE Std 802.3-2018)

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IEEE Standard for Ethernet

LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 13 May 2022

IEEE SA Standards Board

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Abstract: Ethernet local area network operation is specified for selected speeds of operation from 1 Mb/s to 400 Gb/s using a common media access control (MAC) specification and management information base (MIB). The Carrier Sense Multiple Access with Collision Detection (CSMA/CD) MAC protocol specifies shared medium (half duplex) operation, as well as full duplex operation. Speed specific Media Independent Interfaces (MIIs) allow use of selected Physical Layer devices (PHYs) for operation over coaxial, twisted pair or fiber optic cables, or electrical backplanes. System considerations for multisegment shared access networks describe the use of Repeaters that are defined for operational speeds up to 1000 Mb/s. Local Area Network (LAN) operation is supported at all speeds. Other specified capabilities include: various PHY types for access networks, PHYs suitable for metropolitan area network applications, and the provision of power over selected twisted pair PHY types.

Keywords: 2.5 Gigabit Ethernet, 5 Gigabit Ethernet, 10 Gigabit Ethernet, 25 Gigabit Ethernet, 40 Gigabit Ethernet, 50 Gigabit Ethernet, 100 Gigabit Ethernet, 200 Gigabit Ethernet, 400 Gigabit Ethernet, AN, attachment unit interface, AUI, Auto-Negotiation, Backplane Ethernet, balanced cable, data processing, DTE Power via the MDI, EEE, Energy-Efficient Ethernet, EPoC, EPON, EPON protocol over coax, Ethernet, Ethernet in the first mile, Ethernet Passive Optical Network, express traffic, Fast Ethernet, FEC, forward error correction, Gigabit Ethernet, IEEE 802.3™, information exchange, isolation, LAN, local area network, management, MCRS, MDI, media independent interface, medium dependent interface, MIB, MII, MMF, MPCP, Multi-Channel Reconciliation Sublayer, multimode fiber, multipoint control protocol, P2MP, PCS, PD, PHY, physical coding sublayer, Physical Layer, Physical Layer Collision Avoidance, Physical Layer device, physical medium attachment, physical medium dependent, PLCA, PMA, PMD, PoDL, PoE, point to multipoint, Power over Data Lines, Power over Ethernet, Power Sourcing Equipment, Powered Device, PSE, reconciliation sublayer, repeater, RS, single-mode fiber, SMF, type field

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Participants

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Adam Healey, *IEEE 802.3 Working Group Vice-Chair*
Jon Lewis, *IEEE 802.3 Working Group Secretary*
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Adam Healey, *IEEE P802.3 (IEEE 802.3dc) Task Force Chair and Editor-in-Chief*
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Jon Lewis, *IEEE P802.3 (IEEE 802.3dc) Task Force Section Editor*
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Historical participants

The following individuals participated in the IEEE 802.3 working group during various stages of the standard's development. Since the initial publication, many IEEE standards have added functionality or provided updates to material included in this standard. Included is a historical list of participants who have dedicated their valuable time, energy, and knowledge to the creation of this material:

IEEE Std 802.3 document	Date approved by IEEE and ANSI	Officers at the time of working group ballot
IEEE Std 802.3-1985, Original 10 Mb/s standard, MAC, PLS, AUI, 10BASE5	23 June 1983 (IEEE) 31 December 1984 (ANSI)	**Donald C. Loughry,** *Working Group Chair*
IEEE Std 802.3a-1988 (Clause 10), 10 Mb/s MAU 10BASE2	15 November 1985 (IEEE) 28 December 1987 (ANSI)	**Donald C. Loughry,** *Working Group Chair* **Alan Flatman,** *Task Force Chair*
IEEE Std 802.3b-1985 (Clause 11), 10 Mb/s Broadband MAU, 10BROAD36	19 September 1985 (IEEE) 28 February 1986 (ANSI)	**Donald C. Loughry,** *Working Group Chair* **Menachem Abraham,** *Task Force Chair*
IEEE Std 802.3c-1985 (9.1–9.8), 10 Mb/s Baseband Repeater	12 December 1985 (IEEE) 4 June 1986 (ANSI)	**Donald C. Loughry,** *Working Group Chair* **Geoffrey O. Thompson,** *Task Force Chair*
IEEE Std 802.3d-1987 (9.9), 10 Mb/s Fiber MAU, FOIRL	10 December 1987 (IEEE) 9 February 1989 (ANSI)	**Donald C. Loughry,** *Working Group Chair* **Steven Moustakas,** *Task Force Chair*
IEEE Std 802.3e-1987 (Clause 12), 1 Mb/s MAU and Hub 1BASE5	11 June 1987 (IEEE) 15 December 1987 (ANSI)	**Donald C. Loughry,** *Working Group Chair* **Robert Galin,** *Task Force Chair*
IEEE Std 802.3h-1990 (Clause 5), 10 Mb/s Layer Management, DTEs	28 September 1990 (IEEE) 11 March 1991 (ANSI)	**Donald C. Loughry,** *Working Group Chair* **Andy J. Luque,** *Task Force Chair*
IEEE Std 802.3i-1990 (Clauses 13 and 14), 10 Mb/s UTP MAU, 10 BASE-T	28 September 1990 (IEEE) 11 March 1991 (ANSI)	**Donald C. Loughry**, *Working Group Chair* **Patricia Thaler,** *Task Force Chair (initial)* **Richard Anderson,** *Task Force Chair (final)*

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IEEE Std 802.3j-1993 (Clauses 15–18), 10 Mb/s Fiber MAUs 10BASE-FP, 10BASE-FB, and 10BASE-FL	15 September 1993 (IEEE) 15 March 1994 (ANSI)	**Patricia Thaler,** *Working Group Chair* **Keith Amundsen,** *Task Force Chair (initial)* **Frederick Scholl,** *Task Force Chair (final)* **Michael E. Lee,** *Technical Editor*
IEEE Std 802.3k-1993 (Clause 19), 10 Mb/s Layer Management, Repeaters	17 September 1992 (IEEE) 8 March 1993 (ANSI)	**Patricia Thaler,** *Working Group Chair* **Joseph S. Skorupa,** *Task Force Chair* **Geoffrey O. Thompson,** *Vice Chair and Editor*
IEEE Std 802.3*l*-1992 (14.10), 10 Mb/s PICS Proforma 10BASE-T MAU	17 September 1992 (IEEE) 23 February 1993 (ANSI)	**Patricia Thaler,** *Working Group Chair* **Mike Armstrong,** *Task Force Chair and Editor* **Paul Nikolich,** *Vice Chair* **William Randle,** *Editorial Coordinator*
IEEE Std 802.3m-1995, Maintenance 2	21 September 1995 (IEEE) 16 July 1996 (ANSI)	**Patricia Thaler,** *Working Group Chair* **Gary Robinson,** *Maintenance Chair*
IEEE Std 802.3n-1995, Maintenance 3	21 September 1995 (IEEE) 4 April 1996 (ANSI)	**Patricia Thaler,** *Working Group Chair* **Gary Robinson,** *Maintenance Chair*
IEEE Std 802.3p-1993 (Clause 20), Management, 10 Mb/s Integrated MAUs	17 June 1993 (IEEE) 4 January 1994 (ANSI)	**Patricia Thaler,** *Working Group Chair* **Joseph S. Skorupa,** *Task Force Chair* **Geoffrey O. Thompson,** *Vice Chair and Editor*
IEEE Std 802.3q-1993 (Clause 5), 10 Mb/s Layer Management, GDMO Format	17 June 1993 (IEEE) 4 January 1994 (ANSI)	**Patricia Thaler,** *Working Group Chair* **Joseph S. Skorupa,** *Task Force Chair* **Geoffrey O. Thompson,** *Vice Chair and Editor*
IEEE Std 802.3r-1996 (8.8), Type 10BASE5 Medium Attachment Unit PICS proforma	29 July 1996 (IEEE) 6 January 1997 (ANSI)	**Patricia Thaler,** *Working Group Chair* **Imre Juhász**, *Task Force Chair* **William Randle,** *Task Force Editor*
IEEE Std 802.3s-1995, Maintenance 4	21 September 1995 (IEEE) 8 April 1996 (ANSI)	**Geoffrey O. Thompson,** *Working Group Chair* **Gary Robinson,** *Maintenance Chair*
IEEE Std 802.3t-1995, 120 Ω informative annex to 10BASE-T	14 June 1995 (IEEE) 12 January 1996 (ANSI)	**Geoffrey O. Thompson,** *Working Group Chair* **Jacques Christ,** *Task Force Chair*
IEEE Std 802.3u-1995 (Clauses 21–30), Type 100BASE-T MAC parameters, Physical Layer, MAUs, and Repeater for 100 Mb/s Operation	14 June 1995 (IEEE) 4 April 1996 (ANSI)	**Geoffrey O. Thompson,** *Working Group Chair* **Peter Tarrant,** *Task Force Chair (Phase 1)* **Howard Frazier,** *Task Force Chair (Phase 2)* **Paul Sherer,** *Task Force Editor-in-Chief (Phase 1)* **Howard Johnson,** *Task Force Editor-in-Chief (Phase 2)* **Colin Mick,** *Task Force Comment Editor*
IEEE Std 802.3v-1995, 150 Ω informative annex to 10BASE-T	12 December 1995 (IEEE) 16 July 1996 (ANSI)	**Geoffrey O. Thompson,** *Working Group Chair* **Larry Nicholson,** *Task Force Chair*
IEEE Std 802.3x-1997 and IEEE Std 802.3y-1997 (Revisions to IEEE Std 802.3, Clauses 31 and 32), Full-Duplex Operation and Type 100BASE-T2	20 March 1997 (IEEE) 5 September 1997 (ANSI)	**Geoffrey O. Thompson,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Rich Seifert,** *Task Force Chair and Editor (802.3x)* **J. Scott Carter,** *Task Force Chair (802.3y)* **Colin Mick**, *Task Force Editor (802.3y)*
IEEE Std 802.3z-1998 (Clauses 34–39, 41–42), Type 1000BASE-X MAC Parameters, Physical Layer, Repeater, and Management Parameters for 1000 Mb/s Operation	25 June 1998 (IEEE)	**Geoffrey O. Thompson,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Howard M. Frazier, Jr.,** *Task Force Chair* **Howard W. Johnson,** *Task Force Editor*
IEEE Std 802.3aa-1998, Maintenance 5	25 June 1998 (IEEE)	**Geoffrey O. Thompson,** *Working Group Chair* **Colin Mick**, *Task Force Editor*

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IEEE Std 802.3ab-1999 (Clause 40), Physical Layer Parameters and Specifications for 1000 Mb/s Operation Over 4 Pair of Category 5 Balanced Copper Cabling, Type 1000BASE-T	26 June 1999 (IEEE)	**Geoffrey O. Thompson,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Robert M. Grow,** *Working Group Secretary* **George Eisler**, *Task Force Chair* **Colin Mick**, *Task Force Editor*
IEEE Std 802.3ac-1998, Frame Extensions for Virtual Bridged Local Area Network (VLAN) Tagging on IEEE 802.3 Networks	16 September 1998 (IEEE)	**Geoffrey O. Thompson,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Andy J. Luque,** *Working Group Secretary* **Ian Crayford,** *Task Force Chair* **Rich Seifert,** *Task Force Editor*
IEEE Std 802.3ad-2000 (Clause 43), Aggregation of Multiple Link Segments	30 March 2000 (IEEE)	**Geoffrey O. Thompson,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Robert M. Grow,** *Working Group Secretary* **Steven Haddock,** *Task Force Chair* **Tony Jeffree,** *Task Force Co-Editor* **Rich Seifert,** *Task Force CoEditor*
IEEE Std 802.3-2002 (IEEE 802.3ag, Maintenance 6, Revision of the base), Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access method and Physical Layer specifications	14 January 2002 (IEEE)	**Geoffrey O. Thompson,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Robert M. Grow,** *Working Group Secretary*
IEEE Std 802.3ae-2002, (Clauses 44–53) Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 Gb/s Operation	13 June 2002 (IEEE)	**Geoffrey O. Thompson,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Robert M. Grow,** *Working Group Secretary* **R. Jonathan Thatcher,** *Task Force Chair* **Stephen Haddock,** *Task Force Vice Chair* **Bradley J. Booth,** *Task Force Editor* **Lacreshia Laningham,** *Task Force Assistant Editor* **Benjamin Brown,** *Logic Track Chair* **Walter Thirion,** *Optical Track Chair*
IEEE Std 802.3af-2003, (Clause 33) Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI)	12 June 2003 (IEEE)	**Geoffrey O. Thompson,** *Working Group Chair (Phase 1)* **Robert M. Grow,** *Working Group Chair (Phase 2)* **David J. Law,** *Working Group Vice Chair* **Robert M. Grow,** *Working Group Secretary (Phase 1)* **Steven B. Carlson,** *Working Group Secretary (Phase 2)* **Steven B. Carlson,** *Task Force Chair* **Michael S. McCormack,** *Task Force Editor (Phase 1)* **John J. Jetzt,** *Task Force Editor (Phase 2)* **Chad M. Jones,** *Task Force Comment Editor*
IEEE Std 802.3ah-2004, Media Access Control Parameters, Physical Layers, and Management Parameters for Subscriber Access Networks	6 April 2005 (IEEE)	**Robert M. Grow,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Steven B. Carlson,** *Working Group Secretary* **Howard Frazier,** *Task Force Chair* **Wael W. Diab,** *Task Force Editor-in-Chief* **Hugh Barrass,** *Task Force Vice-Chair* **Scott Simon,** *Task Force Recording Secretary* **Behrooz Rezvani,** *Task Force Executive Secretary*
IEEE Std 802.3aj-2003, Maintenance 7	11 September 2003 (IEEE)	**Robert M. Grow,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair, Task Force Chair* **Steven B. Carlson,** *Working Group Secretary* **Catherine K. N. Berger,** *Task Force Editor*
IEEE Std 802.3ak-2004, Physical Layer and Management Parameters for 10Gb/s Operation, Type 10GBASE-CX4	9 February 2004 (IEEE)	**Robert M. Grow,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Steven B. Carlson,** *Working Group Secretary* **Daniel J. Dove,** *Task Force Chair* **Howard A. Baumer,** *Task Force Editor*

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IEEE Std 802.3-2005 (IEEE 802.3REVam, Revision of the base), Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access method and Physical Layer specifications	9 June 2005 (IEEE)	**Robert M. Grow,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Wael W. Diab,** *Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Piers Dawe,** *Review Editor*
IEEE Std 802.3an-2006, Physical Layer and Management Parameter for 10 Gb/s Operation, Type 10GBASE-T	8 June 2006 (IEEE)	**Robert M. Grow,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Wael William Diab,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Bradley Booth,** *Task Force Chair* **Sanjay Kasturia,** *Task Force Editor-in Chief* **George Eisler,** *Task Force Recording Secretary*
IEEE Std 802.3ap-2007, Ethernet Operation over Electrical Backplanes	22 March 2007 (IEEE)	**Robert M. Grow,** *Working Group Chair* **David J. Law,** *Working Group Vice-Chair* **Wael W. Diab**, *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Bradley Booth,** *Working Group Treasurer* **Adam Healey,** *Task Force Chair* **John D'Ambrosia,** *Task Force Secretary* **Schelto vanDoorn,** *Task Force Editor-in-Chief (Phase 1)* **Ilango S. Ganga,** *Task Force Editor-in-Chief (Phase 2)*
IEEE Std 802.3aq-2006, Physical Layer and Management Parameters for 10 Gb/s Operation, Type 10GBASE-LRM	15 September 2006 (IEEE)	**Robert M. Grow,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Wael William Diab,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **David G. Cunningham,** *Task Force Chair* **Nick Weiner,** *Task Force Editor* **Piers Dawe,** *Task Force Contributing Editor*
IEEE Std 802.3as-2006, Frame format extensions	15 September 2006 (IEEE)	**Robert M. Grow,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair* **Wael William Diab,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Kevin Q. Daines,** *Task Force Chair* **Glenn W. Parsons,** *Task Force Editor*
IEEE Std 802.3-2005/Cor 1-2006 (IEEE 802.3au), DTE Power via MDI Isolation corrigendum	8 June 2006 (IEEE)	**Robert M. Grow,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair, Task Force Editor* **Wael W. Diab**, *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary*
IEEE Std 802.3-2005/Cor 2-2007 (IEEE 802.3aw), 10GBASE-T corrigendum	7 June 2007 (IEEE)	**Robert M. Grow,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair, Task Force Editor* **Wael W. Diab**, *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Bradley Booth,** *Working Group Treasurer*
IEEE Std 802.3-2008 (IEEE 802.3ay), Maintenance #9 (Revision of the base), Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access method and Physical Layer specifications	26 September 2008 (IEEE)	**Robert M. Grow,** *Working Group Chair* **David J. Law,** *Working Group Vice Chair, Task Force Editor* **Wael William Diab,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Bradley Booth,** *Working Group Treasurer*
IEEE Std 802.3at-2009 Data Terminal Equipment (DTE) Power via the Media Dependent Interface (MDI) Enhancements	11 September 2009 (IEEE)	**David J. Law,** *Working Group Chair* **Wael William Diab,** *Working Group Vice Chair* **Adam Healey,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Bradley Booth,** *Working Group Treasurer* **Mike McCormack,** *Task Force Chair* **D. Matthew Landry,** *Task Force Chief Editor* **Chad Jones,** *Task Force Comment Editor*

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IEEE Std 802.3av-2009 Physical Layer Specifications and Management Parameters for 10 Gb/s Passive Optical Networks	11 September 2009 (IEEE)	**David J. Law,** *Working Group Chair* **Wael William Diab,** *Working Group Vice Chair* **Adam Healey,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Bradley Booth,** *Working Group Treasurer* **Glen Kramer,** *Task Force Chair* **Duane Remein,** *Task Force Chief Editor* **Marek Hajduczenia,** *Task Force Assistant Editor*
IEEE Std 802.3az-2010 Media Access Control Parameters, Physical Layers, and Management Parameters for Energy-Efficient Ethernet	30 September 2010 (IEEE)	**David J. Law,** *Working Group Chair* **Wael William Diab,** *Working Group Vice Chair* **Steven B. Carlson,** *Working Group Executive Secretary* **Adam Healey,** *Working Group Secretary* **Bradley Booth,** *Working Group Treasurer* **Michael Bennett,** *Task Force Chair* **Sanjay Kasturia,** *Task Force Editor-in-Chief*
IEEE Std 802.3ba Media Access Control Parameters, Physical Layers, and Management Parameters for 40 Gb/s and 100 Gb/s Operation	17 June 2010 (IEEE)	**David J. Law,** *Working Group Chair* **Wael William Diab,** *Working Group Vice-Chair* **Steven B. Carlson,** *Working Group Executive Secretary* **Adam Healey,** *Working Group Secretary* **Bradley Booth,** *Working Group Treasurer* **John D'Ambrosia,** *Task Force Chair* **Ilango S. Ganga,** *Task Force Editor-in-Chief*
IEEE Std 802.3-2008/Cor 1-2009 (IEEE 802.3bb) Pause Reaction Delay Corrigendum.	9 December 2009 (IEEE)	**David J. Law,** *Working Group Chair* **Wael William Diab,** *Working Group Vice-Chair* **Steven B. Carlson,** *Working Group Executive Secretary* **Adam Healey,** *Working Group Secretary* **Bradley Booth,** *Working Group Treasurer*
IEEE Std 802.3bc-2009 Ethernet Organizationally Specific Type, Length, Value (TLVs)	11 September 2009 (IEEE)	**David J. Law,** *Working Group Chair and Task Force Editor* **Wael W. Diab,** *Working Group Vice Chair, Task Force Chair* **Steven B. Carlson,** *Working Group Executive Secretary* **Adam Healey,** *Working Group Secretary* **Bradley Booth,** *Working Group Treasurer*
IEEE Std 802.3bd-2011 MAC Control Frame for Priority-based Flow Control	16 June 2011 (IEEE)	**Tony Jeffree,** *IEEE 802.1 Working Group Chair* **Paul Congdon,** *IEEE 802.1 Working Group Vice Chair* **David J. Law,** *IEEE 802.3 Working Group Chair* **Wael W. Diab,** *IEEE 802.3 Working Group Vice Chair* **Pat Thaler,** *Data Center Bridging Task Group Chair*
IEEE Std 802.3bf-2011 Media Access Control (MAC) Service Interface and Management Parameters to Support Time Synchronization Protocols	16 May 2011 (IEEE)	**David J. Law,** *Working Group Chair* **Wael William Diab,** *Working Group Vice-Chair* **Adam Healey,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Steven B. Carlson,** *Task Force Chair* **Marek Hajduczenia,** *Task Force Editor-in-Chief*
IEEE Std 802.3bg-2011 Physical Layer and Management Parameters for Serial 40 Gb/s Ethernet Operation Over Single-Mode Fiber	31 March 2011 (IEEE)	**David J. Law,** *Working Group Chair* **Wael William Diab,** *Working Group Vice-Chair* **Adam Healey,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Mark Nowell,** *Task Force Chair* **Pete Anslow,** *Task Force Editor-in-Chief*
IEEE Std 802.3-2012 (IEEE 802.3ah), Maintenance #10 (Revision of the base), Standard for Ethernet	28 December 2012 (IEEE)	**David J. Law,** *Working Group Chair* **Wael William Diab,** *Working Group Vice-Chair, Task Force Chair and Editor-in-Chief* **Adam Healey,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasure*
IEEE Std 802.3bk-2013 Physical Layer Specifications and Management Parameters for Extended Ethernet Passive Optical Networks	23 August 2013 (IEEE)	**David J. Law,** *Working Group Chair* **Wael William Diab,** *Working Group Vice-Chair* **Adam Healey,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Marek Hajduczenia,** *Task Force Chair* **Susumu Nishihara,** *Task Force Editor-in-Chief*

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IEEE Std 802.3bj-2014 Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables	12 June 2014 (IEEE)	**David J. Law,** *Working Group Chair* **Wael William Diab,** *Working Group Vice-Chair (initial)* **Adam Healey,** *Working Group Secretary, (initial), Task Force Editor-in-Chief (initial), Working Group Vice-Chair (final), Task Force Chair (final)* **Pete Anslow,** *Working Group Secretary (final)* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **John D'Ambrosia,** *Task Force Chair (initial)* **Matthew Brown,** *Task Force Editor-in-Chief (final)*
IEEE Std 802.3bm-2015 Physical Layer Specifications and Management Parameters for 40 Gb/s and 100 Gb/s Operation Over Fiber Optic Cables	16 February 2015 (IEEE)	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary and Task Force Editor-in-Chief* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Dan Dove,** *Task Force Chair* **Kapil Shrikhande,** *Task Force Vice-Chair*
IEEE Std 802.3-2015 (IEEE 802.3bx), Maintenance #11 (Revision of the base), Standard for Ethernet	3 September 2015	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair, Task Force Chair, and Task Force Editor-in-Chief* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer*
IEEE Std 802.3bw-2015 Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable (100BASE-T1)	26 October 2015	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary and Task Force Chair, Phase 2* **Valerie Maguire,** *Working Group Treasurer* **Thomas Hogenmüller**, *Task Force Chair, Phase 1* **Mehmet Tazebay**, *Task Force Vice-Chair* **Curtis Donahue**, *Task Force Editor-in-Chief*
IEEE Std 802.3by-2016 Media Access Control Parameters, Physical Layers, and Management Parameters for 25 Gb/s Operation	30 June 2016	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Mark Nowell**, *Task Force Chair* **Matthew Brown***, Task Force Editor-in-Chief*
IEEE Std 802.3bq-2016 Physical Layers and Management Parameters for 25 Gb/s and 40 Gb/s Operation, Types 25GBASE-T and 40GBASE-T	30 June 2016	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **David Chalupsky**, *Task Force Chair* **George Zimmerman***, Task Force Editor-in-Chief*
IEEE Std 802.3bp-2016 Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted-Pair Copper Cable	30 June 2016	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary and Task Force Chair* **Valerie Maguire,** *Working Group Treasurer* **Marek Hajduczenia***, Task Force Editor-in-Chief*
IEEE Std 802.3br-2016 Specification and Management Parameters for Interspersing Express Traffic	30 June 2016	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Ludwig Winkel**, *Task Force Chair* **Patricia Thaler***, Task Force Editor-in-Chief*

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IEEE Std 802.3bn-2016 Physical Layer Specifications and Management Parameters for Ethernet Passive Optical Networks Protocol over Coax	22 September 2016	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Mark Laubach**, *Task Force Chair* **Duane Remein**, *Task Force Editor-in-Chief*
IEEE Std 802.3bz-2016 Media Access Control Parameters, Physical Layers, and Management Parameters for 2.5 Gb/s and 5 Gb/s Operation, Types 2.5GBASE-T and 5GBASE-T	22 September 2016	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **David Chalupsky**, *Task Force Chair* **George Zimmerman**, *Task Force Editor-in-Chief*
IEEE Std 802.3bu-2016 Physical Layer and Management Parameters for Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet	7 December 2016	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Dave Dwelley,** *Task Force Chair, Phase 1* **Dan Dove,** *Task Force Chair, Phase 2* **Andy Gardner**, *Task Force Editor-in-Chief*
IEEE Std 802.3bv-2017 Physical Layer Specifications and Management Parameters for 1000 Mb/s Operation Over Plastic Optical Fiber	14 February 2017	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Robert M. Grow,** *Task Force Chair* **Rubén Pérez-Aranda**, *Task Force Editor-in-Chief*
IEEE Std 802.3-2015/Cor 1-2017 (IEEE Std 802.3ce) Multilane Timestamping	23 March 2017	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair, Task Force Chair, and Task Force Editor-in-Chief* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer*
IEEE Std 802.3bs-2017 Media Access Control Parameters, Physical Layers, and Management Parameters for 200 Gb/s and 400 Gb/s Operation	6 December 2017	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary and Task Force Editor-in-Chief* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **John D'Ambrosia,** *Task Force Chair*
IEEE Std 802.3cc-2017 Physical Layer and Management Parameters for Serial 25 Gb/s Ethernet Operation Over Single-Mode Fiber	6 December 2017	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **David Lewis,** *Task Force Chair* **Kohichi R. Tamura,** *Task Force Editor-in-Chief*
IEEE Std 802.3cb-2018 Physical Layer Specifications and Management Parameters for 2.5 Gb/s and 5 Gb/s Operation over Backplane	27 September 2018	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Yong Kim,** *Task Force Chair, Phase 1* **Daniel F. Smith,** *Task Force Chair, Phase 2* **William Lo,** *Task Force Editor-in-Chief, Phase 1* **Daniel F. Smith,** *Task Force Editor-in-Chief, Phase 2*

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IEEE Std 802.3bt-2018 Physical Layer and Management Parameters for Power over Ethernet over 4 pairs	27 September 2018	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Chad Jones,** *Task Force Chair* **Koussalya Balasubramanian,** *Task Force Editor-in-Chief, Phase 1* **Lennart Yseboodt,** *Task Force Editor-in-Chief, Phase 2*
IEEE Std 802.3cd-2018 Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation	5 December 2018	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Mark Nowell,** *Task Force Chair* **Matt Brown,** *Task Force Editor-in-Chief*
IEEE Std 802.3cn-2019 Physical Layers and Management Parameters for 50 Gb/s, 200 Gb/s, and 400 Gb/s Operation over Single-Mode Fiber	7 November 2019	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary and Task Force Editor-in-Chief* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **John D'Ambrosia,** *Task Force Chair*
IEEE Std 802.3cg-2019 Physical Layers Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors	7 November 2019	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **George Zimmerman,** *Task Force Chair* **Valerie Maguire,** *Task Force Editor-in-Chief*
IEEE Std 802.3cq-2020 Maintenance #13: Power over Ethernet over 2 pairs	30 January 2020	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Chad Jones,** *Task Force Chair* **Lennart Yseboodt,** *Task Force Editor-in-Chief*
IEEE Std 802.3cm-2020 Physical Layer and Management Parameters for 400 Gb/s over Multimode Fiber	30 January 2020	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Robert Lingle, Jr.,** *Task Force Chair* **Jonathan P. King,** *Task Force Editor-in-Chief, Phase 1* **Jonathan D. Ingham,** *Task Force Editor-in-Chief, Phase 2*
IEEE Std 802.3ch-2020 Physical Layer Specifications and Management Parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s Automotive Electrical Ethernet	4 June 2020	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary, Phase 1* **Jon Lewis,** *Working Group Secretary, Phase 2* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Steven B. Carlson,** *Task Force Chair* **Natalie Wienckowski,** *Task Force Editor-in-Chief*
IEEE Std 802.3ca-2020 Physical Layer Specifications and Management Parameters for 25 Gb/s and 50 Gb/s Passive Optical Networks	4 June 2020	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Pete Anslow,** *Working Group Secretary, Phase 1* **Jon Lewis,** *Working Group Secretary, Phase 2* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Curtis Knittle,** *Task Force Chair* **Glen Kramer,** *Task Force Vice-Chair* **Marek Hajduczenia,** *Task Force Editor-in-Chief*

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IEEE Std 802.3cr-2021 Maintenance #14: Isolation	9 February 2021	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Jon Lewis,** *Working Group Secretary, Task Force Chair, and Task Force Editor* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer*
IEEE Std 802.3cu-2021 Physical Layers and Management Parameters for 100 Gb/s and 400 Gb/s Operation over Single-Mode Fiber at 100 Gb/s per Wavelength	9 February 2021	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Jon Lewis,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Mark Nowell,** *Task Force Chair* **Gary Nicholl,** *Editor-in-Chief*
IEEE Std 802.3cv-2021 Maintenance #15: Power over Ethernet	9 May 2021	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Jon Lewis,** *Working Group Secretary and Task Force Editor-in-Chief* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Chad Jones,** *Task Force Chair*
IEEE Std 802.3ct-2021 Physical Layers and Management Parameters for 100 Gb/s Operation over DWDM Systems	16 June 2021	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Jon Lewis,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **John D'Ambrosia,** *Task Force Chair* **Tom Issenhuth,** *Task Force Editor-in-Chief*
IEEE Std 802.3cp-2021 Bidirectional 10 Gb/s, 25 Gb/s, and 50 Gb/s Optical Access PHYs	16 June 2021	**David J. Law,** *Working Group Chair* **Adam Healey,** *Working Group Vice-Chair* **Jon Lewis,** *Working Group Secretary* **Steven B. Carlson,** *Working Group Executive Secretary* **Valerie Maguire,** *Working Group Treasurer* **Frank Effenberger,** *Task Force Chair* **Duane Remein,** *Task Force Editor-in-Chief, Phase 1* **Yuanqiu Luo,** *Task Force Editor-in-Chief, Phase 2*

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Chow, Jacky
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Crepin, J. Francois
Cronin, Bill
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Cross, Richard
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Cui, Kai
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Cullin, Chris
Cunningham, David G.
Curcio, Joe
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Dahmouh, Saleem
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Dai, Shaoan
Daido, Fumio
Daines, Bernard
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D'Ambrosia, John
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Introduction

This introduction is not part of IEEE Std 802.3-2022, IEEE Standard for Ethernet.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. “Local Area Networks: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications” was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol and the ability to use an EtherType to specify the MAC client protocol were added in 1997. The title was changed to Standard for Ethernet with the 2012 Revision.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2022 and are not maintained as separate documents.

At the date of IEEE Std 802.3-2022 publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2022

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex K and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33A. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

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Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 140 and Annex 119A through Annex 136D. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well as 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 includes general information on 2.5 Gb/s and 5 Gb/s operation. Clause 126 through Clause 130 and associated annexes include 2.5 Gb/s and 5 Gb/s Physical Layer specifications. Clause 131 provides general information on 50 Gb/s operation. Clause 132 through Clause 140 and associated annexes include 50 Gb/s Physical Layer specifications and additional 100 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications.

Section Nine—Includes Clause 141 through Clause 160 and Annex 142A through Annex 154A. Clause 141 through Clause 144 and associated annexes specify symmetric and asymmetric operation of Ethernet passive optical networks over multiple 25 Gb/s channels. Clause 145 and associated annexes specify increased power delivery using all four pairs in the structured wiring plant. Clause 146 through Clause 149 and associated annexes specify Physical Layers for 10 Mb/s, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation over a single balanced pair of conductors. Clause 150 and Clause 151 include additional 400 Gb/s Physical Layer specifications. Clause 153 and Clause 154 specify 100 Gb/s operation over DWDM channels. Clause 157 through Clause 160 include 10 Gb/s, 25 Gb/s, and 50 Gb/s bidirectional Physical Layer specifications.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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141. Physical Medium Dependent (PMD) sublayer and medium for Nx25G-EPON passive optical networks 5449

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IEEE Standard for Ethernet

1. Introduction

1.1 Overview

This is an international standard for Local and Metropolitan Area Networks (LANs and MANs), employing CSMA/CD as the shared media access method and the IEEE 802.3 (Ethernet) protocol and frame format for data communication. This international standard is intended to encompass several media types and techniques for a variety of MAC data rates as shown in Figure 1–1 and in 4.4.2.

1.1.1 Scope

This standard defines Ethernet local area, access and metropolitan area networks. Ethernet is specified at selected speeds of operation; and uses a common media access control (MAC) specification and management information base (MIB). The Carrier Sense Multiple Access with Collision Detection (CSMA/CD) MAC protocol specifies shared medium (half duplex) operation, as well as full duplex operation. Speed specific Media Independent Interfaces (MIIs) provide an architectural and optional implementation interface to selected Physical Layer devices (PHYs). The Physical Layer encodes frames for transmission and decodes received frames with the modulation specified for the speed of operation, transmission medium and supported link length. Other specified capabilities include: control and management protocols, and the provision of power over selected twisted pair PHY types.

1.1.2 Basic concepts

This standard provides for two distinct modes of operation: half duplex and full duplex. A given IEEE 802.3 instantiation operates in either half or full duplex mode at any one time. The term “CSMA/CD MAC” is used throughout this standard synonymously with “802.3 MAC,” and may represent an instance of either a half duplex or full duplex mode data terminal equipment (DTE), even though full duplex mode DTEs do not implement the CSMA/CD algorithms traditionally used to arbitrate access to shared-media LANs.

1.1.2.1 Half duplex operation

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If, after initiating a transmission, the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again. Each aspect of this access method process is specified in detail in subsequent clauses of this standard.

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Half duplex operation can be used with certain media types and configurations as defined by this standard. For allowable configurations, see 4.4.2.

1.1.2.2 Full duplex operation

Full duplex operation allows simultaneous communication between a pair of stations using point-to-point media (dedicated channel). Full duplex operation does not require that transmitters defer, nor do they monitor or react to receive activity, as there is no contention for a shared medium in this mode. Full duplex mode can only be used when all of the following are true:

a) The physical medium is capable of supporting simultaneous transmission and reception without interference.
b) There are exactly two stations connected with a full duplex point-to-point link. Since there is no contention for use of a shared medium, the multiple access (i.e., CSMA/CD) algorithms are unnecessary.
c) Both stations on the LAN are capable of, and have been configured to use, full duplex operation.

The most common configuration envisioned for full duplex operation consists of a central bridge (also known as a switch) with a dedicated LAN connecting each bridge port to a single device. Repeaters as defined in this standard are outside the scope of full duplex operation.

Full duplex operation constitutes a proper subset of the MAC functionality required for half duplex operation.

1.1.3 Architectural perspectives

There are two important ways to view network design corresponding to the following:

a) *Architecture.* Emphasizing the logical divisions of the system and how they fit together.
b) *Implementation.* Emphasizing actual components, their packaging, and interconnection.

This standard is organized along architectural lines, emphasizing the large-scale separation of the system into two parts: the Media Access Control (MAC) sublayer of the Data Link Layer and the Physical Layer. These layers are intended to correspond closely to the lowest layers of the ISO/IEC Model for Open Systems Interconnection (see Figure 1–1). (See ISO/IEC 7498-1:1994.[6]) The Logical Link Control (LLC) sublayer, or other MAC client, and MAC sublayer together encompass the functions intended for the Data Link Layer as defined in the OSI model.

1.1.3.1 Architectural rationale

An architectural organization of the standard has two main advantages:

a) *Clarity.* A clean overall division of the design along architectural lines makes the standard clearer.
b) *Flexibility.* Segregation of medium-dependent aspects in the Physical Layer allows the LLC and MAC or equivalent sublayers to apply to a family of transmission media.

Partitioning the Data Link Layer allows various media access methods within the family of LAN standards.

The architectural model is based on a set of interfaces that may be different from those emphasized in implementations. One critical aspect of the design, however, shall be addressed largely in terms of the implementation interfaces: compatibility.

[6]For information about references, see 1.3.

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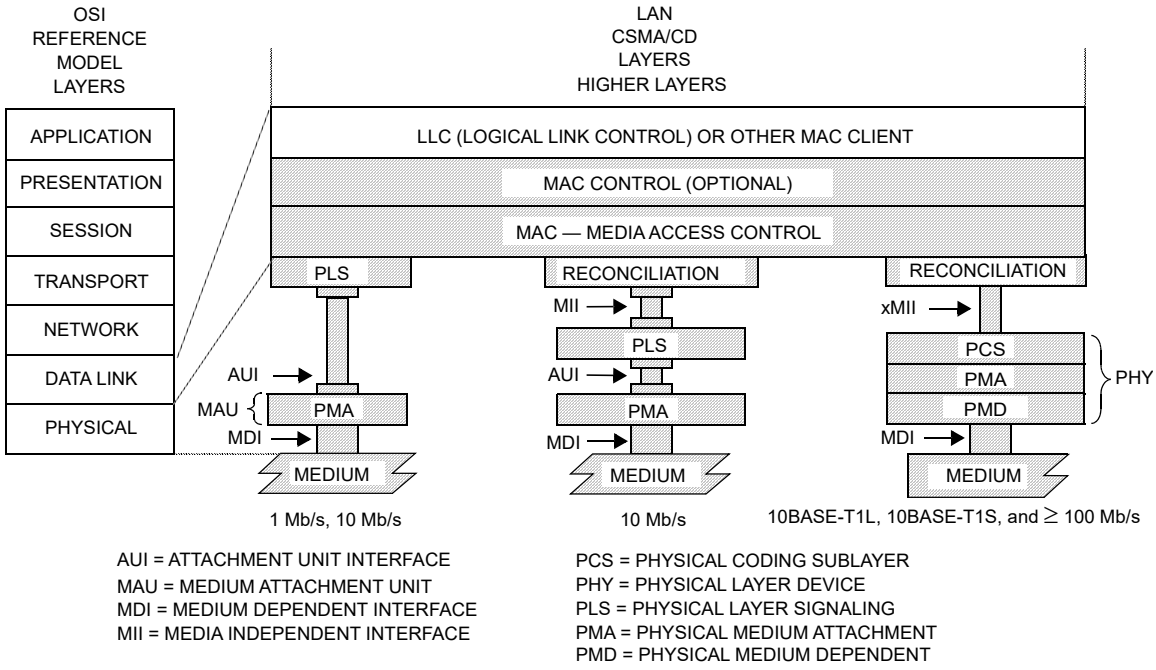

NOTE—In this figure, the xMII is used as a generic term for the Media Independent Interfaces for implementations of 10BASE-T1L, 10BASE-T1S, and 100 Mb/s and above. For example: for 100 Mb/s implementations this interface is called MII; for 1 Gb/s implementations it is called GMII; for 10 Gb/s implementations it is called XGMII; etc.

Figure 1–1—IEEE 802.3 standard relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

1.1.3.2 Compatibility interfaces

The following important compatibility interfaces are defined within what is architecturally the Physical Layer.

a) *Medium Dependent Interfaces (MDI).* To communicate in a compatible manner, all stations shall adhere rigidly to the exact specification of physical media signals defined in the appropriate clauses in this standard, and to the procedures that define correct behavior of a station. The medium-independent aspects of the LLC sublayer and the MAC sublayer or equivalent should not be taken as detracting from this point; communication in an Ethernet Local Area Network requires complete compatibility at the Physical Medium interface (that is, the physical cable interface).

b) *Attachment Unit Interface (AUI).* Some DTEs are located some distance from their connection to the physical cable. A small amount of circuitry will exist in the Medium Attachment Unit (MAU) directly adjacent to the physical cable, while the majority of the hardware and all of the software will be placed within the DTE. The AUI is defined as a second compatibility interface. While conformance with this interface is not strictly necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing MAUs and DTEs. The AUI may be optional or not specified for some implementations of this standard that are expected to be connected directly to the medium and so do not use a separate MAU or its interconnecting AUI cable. The PLS and PMA are then part of a single unit, and no explicit AUI implementation is required.

c) *Media Independent Interface (MII).* It is anticipated that some DTEs will be connected to a remote PHY, and/or to different medium dependent PHYs. The MII is defined as a third compatibility interface. While conformance with implementation of this interface is not strictly necessary to ensure

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communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs. The MII is optional.

d) *Gigabit Media Independent Interface (GMII).* The GMII is designed to connect a 1 Gb/s capable MAC or repeater unit to a 1 Gb/s PHY. While conformance with implementation of this interface is not strictly necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 1 Gb/s speeds. The GMII is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the GMII. The GMII is optional.

e) *Ten-bit Interface (TBI).* The TBI is provided by the 1000BASE-X PMA sublayer as a physical instantiation of the PMA service interface. The TBI is recommended for 1000BASE-X systems, since it provides a convenient partition between the high-frequency circuitry associated with the PMA sublayer and the logic functions associated with the PCS and MAC sublayers. The TBI is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the TBI. The TBI is optional.

f) *10 Gigabit Media Independent Interface (XGMII).* The XGMII is designed to connect a 2.5 Gb/s, 5 Gb/s, or 10 Gb/s capable MAC to a PHY of the same rate. While conformance with implementation of this interface is not necessary to ensure communication, it allows maximum flexibility in intermixing PHYs and DTEs at 2.5 Gb/s, 5 Gb/s, and 10 Gb/s speeds. The XGMII is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the XGMII. The XGMII is optional.

g) *10 Gigabit Attachment Unit Interface (XAUI).* The XAUI is designed to extend the connection between a 10 Gb/s capable MAC and a 10 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 10 Gb/s speeds. The XAUI is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the XAUI. The XAUI is optional.

h) *10 Gigabit Sixteen-Bit Interface (XSBI).* The XSBI is provided as a physical instantiation of the PMA service interface for 10GBASE-R and 10GBASE-W PHYs. While conformance with implementation of this interface is not necessary to ensure communication, it provides a convenient partition between the high-frequency circuitry associated with the PMA sublayer and the logic functions associated with the PCS and MAC sublayers. No mechanical connector is specified for use with the XSBI. The XSBI is optional.

i) *25 Gigabit Media Independent Interface (25GMII).* The 25GMII is designed to connect a 25 Gb/s capable MAC to a 25 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 25 Gb/s speeds. The 25GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 25GMII. The 25GMII is optional.

j) *25 Gigabit Attachment Unit Interface (25GAUI).* The 25GAUI is a physical instantiation of the PMA service interface to extend the connection between 25 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 25 Gb/s speeds. The 25GAUI is intended for use as a chip-to-chip or a chip-to-module interface. No mechanical connector is specified for use with the 25GAUI. The 25GAUI is optional.

k) *40 Gb/s Media Independent Interface (XLGMII).* The XLGMII is designed to connect a 40 Gb/s capable MAC to a 40 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 40 Gb/s speeds. The XLGMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the XLGMII. The XLGMII is optional.

l) *40 Gb/s Attachment Unit Interface (XLAUI).* The XLAUI is a physical instantiation of the PMA service interface to extend the connection between 40 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 40 Gb/s speeds. The XLAUI is

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intended for use as a chip-to-chip or a chip-to-module interface. No mechanical connector is specified for use with the XLAUI. The XLAUI is optional.

m) *40 Gb/s Parallel Physical Interface (XLPPI)*. The XLPPI is provided as a physical instantiation of the PMD service interface for 40GBASE-SR4 and 40GBASE-LR4 PMDs. The XLPPI has four lanes. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in connecting the 40GBASE-SR4 or 40GBASE-LR4 PMDs. The XLPPI is intended for use as a chip-to-module interface. No mechanical connector is specified for use with the XLPPI. The XLPPI is optional.

n) *50 Gb/s Media Independent Interface (50GMII).* The 50GMII is designed to connect a 50 Gb/s capable MAC to a 50 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 50 Gb/s speeds. The 50GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 50GMII. The 50GMII is optional.

o) *50 Gb/s Attachment Unit Interface (LAUI-2/50GAUI-n).* The LAUI-2/50GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 50 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 50 Gb/s speeds. The LAUI-2/50GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Two widths of 50GAUI-n are defined: a two-lane version (50GAUI-2) in Annex 135D and Annex 135E, and a one-lane version (50GAUI-1) in Annex 135F and Annex 135G. No mechanical connector is specified for use with the LAUI-2/50GAUI-n. The LAUI-2/50GAUI-n is optional.

p) *100 Gb/s Media Independent Interface (CGMII).* The CGMII is designed to connect a 100 Gb/s capable MAC to a 100 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 100 Gb/s speeds. The CGMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the CGMII. The CGMII is optional.

q) *100 Gb/s Attachment Unit Interface (CAUI-n/100GAUI-n).* The CAUI-n/100GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 100 Gb/s speeds. The CAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Three widths of CAUI-n are defined: a ten-lane version (CAUI-10) in Annex 83A and Annex 83B, a four-lane version (CAUI-4/100GAUI-4) in Annex 83D, Annex 83E, Annex 135D, and Annex 135E, and a two-lane version (100GAUI-2) in Annex 135F and Annex 135G. No mechanical connector is specified for use with the CAUI-n/100GAUI-n. The CAUI-n/100GAUI-n is optional.

r) *100 Gb/s Parallel Physical Interface (CPPI)*. The CPPI is provided as a physical instantiation of the PMD service interface for 100GBASE-SR10 PMDs. The CPPI has ten lanes. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in connecting the 100GBASE-SR10 PMDs. The CPPI is intended for use as a chip-to-module interface. No mechanical connector is specified for use with the CPPI. The CPPI is optional.

s) *200 Gb/s Media Independent Interface (200GMII).* The 200GMII is designed to connect a 200 Gb/s capable MAC to a 200 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 200 Gb/s speeds. The 200GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 200GMII. The 200GMII is optional.

t) *200 Gb/s Attachment Unit Interface (200GAUI-n).* The 200GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 200 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 200 Gb/s speeds. The 200GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Two widths of 200GAUI-n are defined: an eight-lane version (200GAUI-8) in Annex 120B and

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Annex 120C, and a four-lane version (200GAUI-4) in Annex 120D and Annex 120E. No mechanical connector is specified for use with the 200GAUI-n. The 200GAUI-n is optional.

u) *400 Gb/s Media Independent Interface (400GMII).* The 400GMII is designed to connect a 400 Gb/s capable MAC to a 400 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 400 Gb/s speeds. The 400GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 400GMII. The 400GMII is optional.

v) *400 Gb/s Attachment Unit Interface (400GAUI-n).* The 400GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 400 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 400 Gb/s speeds. The 400GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Two widths of 400GAUI-n are defined: a sixteen-lane version (400GAUI-16) in Annex 120B and Annex 120C, and an eight-lane version (400GAUI-8) in Annex 120D and Annex 120E. No mechanical connector is specified for use with the 400GAUI-n. The 400GAUI-n is optional.

1.1.4 Layer interfaces

In the architectural model used here, the layers interact by way of well-defined interfaces, providing services as specified in Clause 2 and Clause 6. In general, the interface requirements are as follows:

a) The interface between the MAC sublayer and its client includes facilities for transmitting and receiving frames, and provides per-operation status information for use by higher-layer error recovery procedures.
b) The interface between the MAC sublayer and the Physical Layer includes signals for framing (carrier sense, receive data valid, transmit initiation) and contention resolution (collision detect), facilities for passing a pair of serial bit streams (transmit, receive) between the two layers, and a wait function for timing.

These interfaces are described more precisely in 4.3. Additional interfaces are necessary to provide for MAC Control services, and to allow higher level network management facilities to interact with these layers to perform operation, maintenance, and planning functions. Network management functions are described in Clause 30.

1.1.5 Application areas

Use of this standard is not restricted to any specific environments or applications.

In the context of this standard, the term “LAN” is used to indicate all networks that utilize the IEEE 802.3 (Ethernet) protocol for communication. These may include (but are not limited to) LANs and MANs.

1.1.6 Word usage

The word *shall* indicates mandatory requirements strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*).[7] [8]

The word *should* indicates that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required (*should* equals *is recommended that*).

[7]The use of the word *must* is deprecated and cannot be used when stating mandatory requirements, *must* is used only to describe unavoidable situations.

[8]The use of *will* is deprecated and cannot be used when stating mandatory requirements, *will* is only used in statements of fact.

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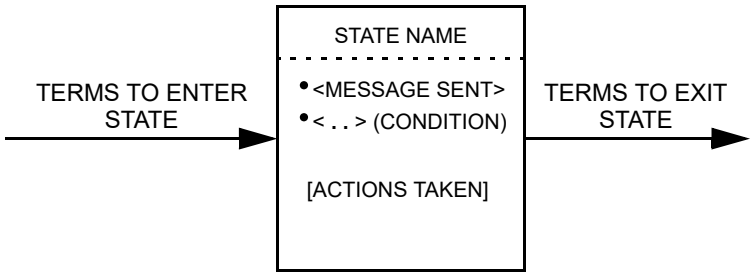
The word *may* is used to indicate a course of action permissible within the limits of the standard (*may* equals *is permitted to*).

The word *can* is used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

1.2 Notation

1.2.1 State diagram conventions

The operation of a protocol can be described by subdividing the protocol into a number of interrelated functions. The operation of the functions can be described by state diagrams. Each diagram represents the domain of a function and consists of a group of connected, mutually exclusive states. Only one state of a function is active at any given time (see Figure 1–1).



Key: ( ) = condition, for example, (if no_collision)
[ ] = action, for example, [reset PLS functions]
* = logical AND
+ = logical OR, arithmetic addition
Tw = Wait Time, implementation dependent
Td = Delay Timeout
Tb = Backoff Timeout
UCT = unconditional transition

Figure 1–1—State diagram notation example

Each state that the function can assume is represented by a rectangle. These are divided into two parts by a horizontal line. In the upper part the state is identified by a name in capital letters. The lower part contains the name of any ON signal that is generated by the function. Actions are described by short phrases and enclosed in brackets.

All permissible transitions between the states of a function are represented graphically by arrows between them. A transition that is global in nature (for example, an exit condition from all states to the IDLE or RESET state) is indicated by an open arrow. Labels on transitions are qualifiers that have to be fulfilled before the transition will be taken. The label UCT designates an unconditional transition. Qualifiers described by short phrases are enclosed in parentheses.

State transitions and sending and receiving of messages occur instantaneously. When a state is entered and the condition to leave that state is not immediately fulfilled, the state executes continuously, sending the messages and executing the actions contained in the state in a continuous manner.

Some devices described in this standard (e.g., repeaters) are allowed to have two or more ports. State diagrams that are capable of describing the operation of devices with an unspecified number of ports require a qualifier notation that allows testing for conditions at multiple ports. The notation used is a term that

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includes a description in parentheses of which ports have to meet the term for the qualifier to be satisfied (e.g., ANY and ALL). It is also necessary to provide for term-assignment statements that assign a name to a port that satisfies a qualifier. The following conventions are used to describe a term-assignment statement that is associated with a transition:

a) The character ":" (colon) is a delimiter used to denote that a term assignment statement follows.
b) The character "⇐" (left arrow) denotes assignment of the value following the arrow to the term preceding the arrow.

The state diagrams contain the authoritative statement of the functions they depict; when apparent conflicts between descriptive text and state diagrams arise, the state diagrams are to take precedence. This does not override, however, any explicit description in the text that has no parallel in the state diagrams.

The models presented by state diagrams are intended as the primary specifications of the functions to be provided. It is important to distinguish, however, between a model and a real implementation. The models are optimized for simplicity and clarity of presentation, while any realistic implementation may place heavier emphasis on efficiency and suitability to a particular implementation technology. It is the functional behavior of any unit that has to match the standard, not its internal structure. The internal details of the model are useful only to the extent that they specify the external behavior clearly and precisely.

1.2.2 Service specification method and notation

The service of a layer or sublayer is the set of capabilities that it offers to a user in the next higher (sub)layer. Abstract services are specified here by describing the service primitives and parameters that characterize each service. This definition of service is independent of any particular implementation (see Figure 1–2).

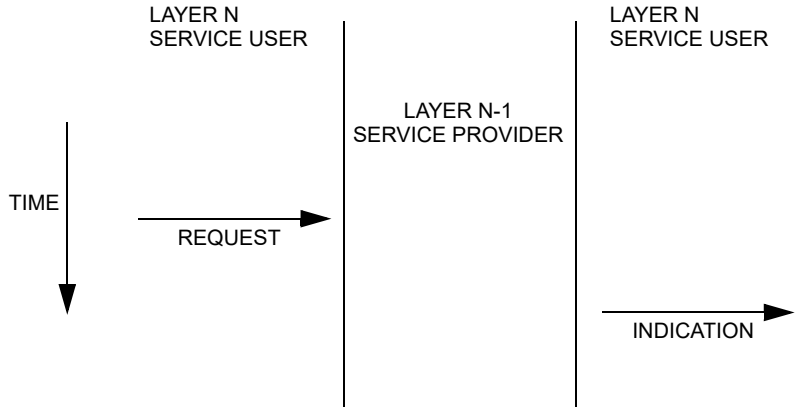

Figure 1–2—Service primitive notation

Specific implementations may also include provisions for interface interactions that have no direct end-to-end effects. Examples of such local interactions include interface flow control, status requests and indications, error notifications, and layer management. Specific implementation details are omitted from this service specification both because they will differ from implementation to implementation and because they do not impact the peer-to-peer protocols.

1.2.2.1 Classification of service primitives

Primitives are of two generic types:

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a) REQUEST. The request primitive is passed from layer N to layer N-1 to request that a service be initiated.
b) INDICATION. The indication primitive is passed from layer N-1 to layer N to indicate an internal layer N-1 event that is significant to layer N. This event may be logically related to a remote service request, or may be caused by an event internal to layer N-1.

The service primitives are an abstraction of the functional specification and the user-layer interaction. The abstract definition does not contain local detail of the user/provider interaction. For instance, it does not indicate the local mechanism that allows a user to indicate that it is awaiting an incoming call. Each primitive has a set of zero or more parameters, representing data elements that shall be passed to qualify the functions invoked by the primitive. Parameters indicate information available in a user/provider interaction; in any particular interface, some parameters may be explicitly stated (even though not explicitly defined in the primitive) or implicitly associated with the service access point. Similarly, in any particular protocol specification, functions corresponding to a service primitive may be explicitly defined or implicitly available.

1.2.3 Physical Layer and media notation

Users of this standard need to reference which particular implementation is being used or identified. Therefore, a means of identifying each implementation is given by a simple, three-field, type notation that is explicitly stated at the beginning of each relevant clause. In general, the Physical Layer type is specified by these fields:

<data rate> <modulation type> <additional distinction>

The data rate, if only a number, is in Mb/s, and if suffixed by a “G”, is in Gb/s. The modulation type (e.g., BASE) indicates how encoded data is transmitted on the medium. The additional distinction may identify characteristics of transmission or medium and, in some cases, the type of PCS encoding used (examples of additional distinctions are “T” for twisted pair, “B” for bidirectional optics, and “X” for a block PCS coding used for that speed of operation). Expansions for defined Physical Layer types are included in 1.4.

1.2.4 Physical Layer message notation

Messages generated within the Physical Layer, either within or between PLS and the MAU (that is, PMA circuitry), are designated by an italic type to designate either form of physical or logical message used to execute the Physical Layer signaling process (for example, *input_idle* or *mau_available*).

1.2.5 Hexadecimal notation

Numerical values designated by the 0x prefix indicate a hexadecimal interpretation of the corresponding number. For example: 0x0F represents an 8-bit hexadecimal value of the decimal number 15 and 0x00000000 represents a 32-bit hexadecimal value of the decimal number 0.

Numerical values designated with a 16 subscript indicate a hexadecimal interpretation of the corresponding number. For example: $0F_{16}$ represents an 8-bit hexadecimal value of the decimal number 15.

Hexadecimal values may also be indicated in text as hexadecimal or hex.

Hexadecimal numbers and values use upper case for hexadecimal digits A through F.

Separators may be used to improve readability of numbers—typically after every two or four hex digits counting from right to left. When hexadecimal is used for a fixed length value, protocol field, etc., where the value is not a multiple of 4 bits, the leftmost hexadecimal digit is truncated to fit the value's length (e.g., an 11 bit value of 0x25F is 010 0101 1111 in binary).

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1.2.6 Accuracy and resolution of numerical quantities

Unless otherwise stated, numerical limits in this standard are to be taken as exact, with the number of significant digits and trailing zeros having no significance.

1.2.7 Qm.n number format

The Qm.n number format is a fixed-point number format where the number of fractional bits is specified by n and optionally the number of integer bits is specified by m. For example, a Q14 number has 14 fractional bits; a Q2.14 number has 2 integer bits and 14 fractional bits. Preceding the "Q" with a "U" indicates an unsigned number.

1.2.8 Em dash (—) in a table cell

A table cell containing an em-dash (—) indicates a lack of data for that cell, or:

— For a units cell, that there is no unit for that parameter
— For a maximum cell, that there is no requirement on the maximum value of that parameter
— For a minimum cell, that there is no requirement on the minimum value of that parameter

1.3 Normative references

The following standards contain provisions that, through reference in this text, constitute provisions of this standard. Standards may be subject to revision, and parties subject to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below. Members of IEC and ISO maintain registers of currently valid international standards. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

ANSI INCITS 230-1994 (R1999), Information Technology—Fibre Channel—Physical and Signaling Interface (FC-PH) [formerly ANSI X3.230-1994 (R1999)].[9]

ANSI INCITS 263-1995 (S2010), Fibre Distributed Data Interface (FDDI)—Token Ring Twisted Pair Physical Layer Medium Dependent (TP-PMD) [formerly INCITS 263-1995 (R2005)].

ANSI/TIA-568-C.0 (February 2009), Generic Telecommunications Cabling for Customer Premises.[10]

ANSI/TIA-568-C.2-1 (July 2016), Balanced Twisted-Pair Telecommunications Cabling and Components Standard, Addendum 1: Specifications for 100 Ω Next Generation Cabling.

ANSI/TIA-568-C.2 (August 2009), Commercial Building Telecommunications Cabling Standard Part 2: Balanced Twisted-Pair Cabling Components.

ANSI/TIA-568-C.3 (June 2008), Optical Fiber Cabling Components Standard.

ANSI/TIA-568.0-D, Generic Telecommunications Cabling for Customer Premises.

ANSI/TIA-604-18:2015, FOCIS 18—Fiber Optic Connector Intermateability Standard—Type MPO-16.

ANSI/TIA-604-18-A:2018, FOCIS 18—Fiber Optic Connector Intermateability Standard—Type MPO-16.

[9]ANSI publications are available from the American National Standards Institute (https://www.ansi.org/).
[10]ANSI/TIA publications are available from the IHS Standards Store (https://global.ihs.com/) or from the Telecommunications Industry Association (https://www.tiaonline.org/).

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ANSI/TIA/EIA-455-95-2019, Absolute Optical Power Test for Optical Fibers and Cables.

ANSI/TIA/EIA-455-204-2013, Measurement of Bandwidth on Multimode Fiber..

ANSI/TIA/EIA-568-A-1995, Commercial Building Telecommunications Cabling Standard.

ASTM D4728, Standard Test Method for Random Vibration Testing of Shipping Containers.[11]

ATIS-0300269.2006(S2016), Structure and Representation of Trace Message Formats for Information Exchange.[12]

ATIS-0600416.1999(R2010), Network to Customer Installation Interfaces—Synchronous Optical NETwork (SONET)—Physical Layer Specification: Common Criteria.

ATIS-0600417.2003(S2015), Spectrum Management for Loop Transmission Systems.

ATIS-0600424.2004(S2015), Interface Between Networks and Customer Installation Very-high-bit-rate Digital Subscriber Lines (VDSL) Metallic Interface (DMT based).

ATIS-0600601.1999(S2015), Integrated Services Digital Network (ISDN)—Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification).

ATIS-0600605.1991(S2015), Integrated Services Digital Network (ISDN)—Basic Access Interface for S and T Reference Points (Layer 1 Specification).

ATIS-0900105.2008, Synchronous Optical Network (SONET)—Basic Description including Multiplex Structure, Rates, and Formats.

CFR 76, Code of Federal Regulations, Title 47, Part 76, October 2005.

CISPR 22: 1993, Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment.[13]

CISPR 25: Vehicles, boats and internal combustion engines—Radio disturbance characteristics—Limits and methods of measurement for the protection of on-board receivers.

EIA/JEDEC Standard EIA/JESD8-6, High Speed Transceiver Logic (HSTL), August 1995.[14]

ETSI TS 101 270-1 (1999), Transmission and Multiplexing (TM); Access transmission systems on metallic access cables; Very high speed Digital Subscriber Line (VDSL); Part 1: Functional requirements.[15]

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[11]ASTM publications are available from the American Society for Testing and Materials (https://www.astm.org/).
[12]ATIS publications are available from the Alliance for Telecommunications Industry Solutions (https://atis.org/).
[13]CISPR documents are available from the International Electrotechnical Commission (https://www.iec.ch/). CISPR documents are also available in the United States from the American National Standards Institute (https://www.ansi.org/).
[14]EIA publications are available from the IHS Standards Store (https://global.ihs.com/). JEDEC publications are available from the JEDEC Solid State Technology Association (https://www.jedec.org/).
[15]ETSI publications are available the European Telecommunications Standards Institute (https://www.etsi.org/).
[16]IEC publications are available from the International Electrotechnical Commission (https://www.iec.ch/). IEC publications are also available in the United States from the American National Standards Institute (https://www.ansi.org/).

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[17]IEEE publications are available from The Institute of Electrical and Electronics Engineers (https://standards.ieee.org/).

[18]The IEEE standards or products referred to in this clause are trademarks of The Institute of Electrical and Electronics Engineers, Inc.

[19]IEEE Std 802.1F-1993 has been withdrawn; however, copies can be obtained from The Institute of Electrical and Electronics Engineers (https://standards.ieee.org/).

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[22]IETF RFCs are available from the Internet Engineering Task Force (https://www.ietf.org/rfc.html).

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[23]ISO/IEC publications are available from the International Organization for Standardization (https://www.iso.org/) and the International Electrotechnical Commission (https://www.iec.ch/). ISO/IEC publications are also available in the United States from the American National Standards Institute (https://www.ansi.org/).

[24]Previous editions of ISO/IEC standards are available from Deutsches Institut für Normung (https://www.din.de/).

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[25]ITU-T publications are available from the International Telecommunications Union (https://www.itu.int/).

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NOTE—Local and national standards such as those supported by ANSI, EIA, MIL, NFPA, and UL are not a formal part of this standard except where no international standard equivalent exists. A number of local and national standards are

[26]For information on MATLAB, contact The MathWorks (https://www.mathworks.com/).

[27]NAMUR publications are available from the User Association of Automation Technology in Process Industries (https://www.namur.net/).

[28]SFF specifications are available from the Storage Networking Industry Association (https://www.snia.org/sff/specifications/).

[29]TIA publications are available from the IHS Standards Store (https://global.ihs.com/) or from the Telecommunications Industry Association (https://www.tiaonline.org/).

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referenced as resource material; these bibliographical references are located in the bibliography in Annex A.[30]

1.4 Definitions

For the purposes of this document, the following terms and definitions apply. The *IEEE Standards Dictionary Online* should be referenced for terms not defined in this clause.[31]

1.4.1 1000BASE-BX10: IEEE 802.3 Physical Layer specification for a 1000 Mb/s point-to-point link over one single-mode optical fiber. (See IEEE Std 802.3, Clause 59 and Clause 66.)

1.4.2 1000BASE-CX: 1000BASE-X over specialty shielded balanced copper jumper cable assemblies. (See IEEE Std 802.3, Clause 39.)

1.4.3 1000BASE-H: IEEE 802.3 PCS and PMA sublayers for 1000 Mb/s Ethernet that support PMDs using duplex plastic optical fiber. (See IEEE Std 802.3, Clause 115.)

1.4.4 1000BASE-KX: IEEE 802.3 Physical Layer specification for 1 Gb/s using 1000BASE-X encoding over an electrical backplane. (See IEEE Std 802.3 Clause 70.)

1.4.5 1000BASE-LX: 1000BASE-X using long wavelength laser devices over multimode and single-mode fiber. (See IEEE Std 802.3, Clause 38.)

1.4.6 1000BASE-LX10: IEEE 802.3 Physical Layer specification for a 1000 Mb/s point-to-point link over two single-mode or multimode optical fibers. (See IEEE Std 802.3, Clause 59 and Clause 66.)

1.4.7 1000BASE-PX: A collection of IEEE 802.3 Physical Layer specifications for a 1000 Mb/s point-to-multipoint link over one single-mode optical fiber. (See IEEE Std 802.3, Table 56–1, Clause 60, Clause 65, and Clause 64.)

1.4.8 1000BASE-RHA: IEEE 802.3 Physical Layer specification for 1000 Mb/s Ethernet using 1000BASE-H encoding and red light (approximately 650 nm) PMD tailored for home-network and other consumer application requirements. (See IEEE Std 802.3, Clause 115.)

1.4.9 1000BASE-RHB: IEEE 802.3 Physical Layer specification for 1000 Mb/s Ethernet using 1000BASE-H encoding and red light (approximately 650 nm) PMD tailored for industrial application requirements. (See IEEE Std 802.3, Clause 115.)

1.4.10 1000BASE-RHC: IEEE 802.3 Physical Layer specification for 1000 Mb/s Ethernet using 1000BASE-H encoding and red light (approximately 650 nm) PMD tailored for automotive application requirements. (See IEEE Std 802.3, Clause 115.)

1.4.11 1000BASE-RHx: IEEE 802.3 specification for 1000 Mb/s Ethernet using duplex plastic optical fiber and red light (approximately 650 nm) with unspecified optical power budget (optical power budget is defined by the specific PMD type). (See IEEE Std 802.3, Clause 115.)

1.4.12 1000BASE-SX: 1000BASE-X using short wavelength laser devices over multimode fiber. (See IEEE Std 802.3, Clause 38.)

1.4.13 1000BASE-T: IEEE 802.3 Physical Layer specification for a 1000 Mb/s CSMA/CD LAN using four pairs of Category 5 balanced copper cabling. (See IEEE Std 802.3, Clause 40.)

[30]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement this standard.
[31]The *IEEE Standards Dictionary Online* is available at https://dictionary.ieee.org/.

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1.4.14 1000BASE-T1: IEEE 802.3 Physical Layer specification for 1000 Mb/s Ethernet using a single twisted-pair copper cable. (See IEEE Std 802.3, Clause 97.)

1.4.15 1000BASE-X: IEEE 802.3 Physical Layer specification for a 1000 Mb/s CSMA/CD LAN that uses a Physical Layer derived from ANSI INCITS 230-1994 (FC-PH). (See IEEE Std 802.3, Clause 36.)

1.4.16 100BASE-BX10: IEEE 802.3 Physical Layer specification for a 100 Mb/s point-to-point link over one single-mode fiber. The link includes two different specifications for 100BASE-BX10-D and 100BASE-BX10-U. (See IEEE Std 802.3, Clause 58 and Clause 66.)

1.4.17 100BASE-FX: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD local area network over two multimode optical fibers. (See IEEE Std 802.3, Clause 24 and Clause 26.)

1.4.18 100BASE-LX10: IEEE 802.3 Physical Layer specification for a 100 Mb/s point-to-point link over two single-mode optical fibers. (See IEEE Std 802.3, Clause 58 and Clause 66.)

1.4.19 100BASE-T: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD local area network. (See IEEE Std 802.3, Clause 22 and Clause 28.)

1.4.20 100BASE-T1: IEEE 802.3 Physical Layer specification for a 100 Mb/s Ethernet full duplex local area network over a single balanced twisted-pair. (See IEEE Std 802.3, Clause 96.)

1.4.21 100BASE-T2: IEEE 802.3 specification for a 100 Mb/s CSMA/CD local area network over two pairs of Category 3 or better balanced cabling. (See IEEE Std 802.3, Clause 32.)

1.4.22 100BASE-T4: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD local area network over four pairs of Category 3, 4, and 5 twisted-pair cabling. (See IEEE Std 802.3 Clause 23.)

1.4.23 100BASE-TX: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD local area network over two pairs of Category 5 twisted-pair cabling. (See IEEE Std 802.3, Clause 24 and Clause 25.)

1.4.24 100BASE-X: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD local area network that uses the Physical Medium Dependent (PMD) sublayer and Medium Dependent Interface (MDI) of the ISO/IEC 9314 group of standards developed by ASC X3T12 (FDDI). (See IEEE Std 802.3, Clause 24.)

1.4.25 100GBASE-CR10: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over ten lanes of shielded balanced copper cabling, with reach up to at least 7 m. (See IEEE Std 802.3, Clause 85.)

1.4.26 100GBASE-CR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136.)

1.4.27 100GBASE-CR4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding and Clause 91 RS-FEC over four lanes of shielded balanced copper cabling, with reach up to at least 5 m. (See IEEE Std 802.3, Clause 92.)

1.4.28 100GBASE-DR: IEEE 802.3 Physical Layer specification for 100 Gb/s serial transmission using 100GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 140.)

1.4.29 100GBASE-ER4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 40 km. (See IEEE Std 802.3, Clause 88.)

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1.4.30 100GBASE-FR1: IEEE 802.3 Physical Layer specification for 100 Gb/s serial transmission using 100GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 140.)

1.4.31 100GBASE-KP4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding, Clause 91 RS-FEC, and 4-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 33 dB at 7 GHz. (See IEEE Std 802.3, Clause 94.)

1.4.32 100GBASE-KR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

1.4.33 100GBASE-KR4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding, Clause 91 RS-FEC, and 2-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 35 dB at 12.9 GHz. (See IEEE Std 802.3, Clause 93.)

1.4.34 100GBASE-LR1: IEEE 802.3 Physical Layer specification for 100 Gb/s serial transmission using 100GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 140.)

1.4.35 100GBASE-LR4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 88.)

1.4.36 100GBASE-P: An IEEE 802.3 family of Physical Layer devices using 100GBASE-R encoding and a PMD that employs pulse amplitude modulation with more than 2 levels. (See IEEE Std 802.3, Clause 80.)

1.4.37 100GBASE-R: An IEEE 802.3 family of Physical Layer devices using 100GBASE-R encoding and a PMD that employs 2-level pulse amplitude modulation. (See IEEE Std 802.3, Clause 80.)

1.4.38 100GBASE-R encoding: The physical coding sublayer encoding defined in Clause 82 for 100 Gb/s operation. (See IEEE Std 802.3, Clause 82.)

1.4.39 100GBASE-SR10: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over ten lanes of multimode fiber, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 86.)

1.4.40 100GBASE-SR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of multimode fiber with reach up to at least 100 m. (See IEEE Std 802.3, Clause 138.)

1.4.41 100GBASE-SR4: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over four lanes of multimode fiber, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 95.)

1.4.42 100GBASE-Z: An IEEE 802.3 family of Physical Layer devices using 100GBASE-R encoding, a combination of phase and amplitude modulation, and coherent detection. (See IEEE Std 802.3, Clause 154.)

1.4.43 100GBASE-ZR: IEEE 802.3 Physical Layer specification for a 100 Gb/s dense wavelength division multiplexing (DWDM) PHY using 100GBASE-R encoding, dual polarization differential quadrature phase shift keying (DP-DQPSK) modulation, and coherent detection with reach up to at least 80 km. (See IEEE Std 802.3, Clause 154.)

1.4.44 100 Gb/s Attachment Unit Interface (CAUI-n, 100GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. Three widths are defined: a ten-lane version (CAUI-10), two

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four-lane versions (CAUI-4, 100GAUI-4), and a two-lane version (100GAUI-2). (See IEEE Std 802.3, Annex 83A and Annex 83B for CAUI-10, Annex 83D and Annex 83E for CAUI-4, Clause 135, Annex 135D, and Annex 135E for 100GAUI-4, or Clause 135, Annex 135F, and Annex 135G for 100GAUI-2.)

1.4.45 100 Gb/s Media Independent Interface (CGMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 100 Gb/s operation. (See IEEE Std 802.3, Clause 81.)

1.4.46 100 Gb/s Parallel Physical Interface (CPPI): The interface between the Physical Medium Attachment (PMA) sublayer and the Physical Medium Dependent (PMD) sublayer for 100GBASE-SR10 PHYs. (See IEEE Std 802.3, Annex 86A.)

1.4.47 10/10G-EPON: An EPON architecture operating at 10 Gb/s in both downstream and upstream directions (symmetric rate). (See IEEE Std 802.3, Clause 56.)

1.4.48 10/1GBASE-PRX: A collection of IEEE 802.3 Physical Layer specifications for a 10 Gb/s downstream, 1 Gb/s upstream (10/1G-EPON) point-to-multipoint link over one single-mode optical fiber. (See IEEE Std 802.3, Table 56–1, Clause 75, Clause 76, and Clause 77.)

1.4.49 10/1G-EPON: An EPON architecture operating at 10 Gb/s in downstream direction and at 1 Gb/s data rate in upstream direction (asymmetric rate). (See IEEE Std 802.3, Clause 56.)

1.4.50 10BASE2: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD local area network over RG 58 coaxial cable. (See IEEE Std 802.3, Clause 10.)

1.4.51 10BASE5: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD local area network over coaxial cable (i.e., thicknet). (See IEEE Std 802.3, Clause 8.)

1.4.52 10BASE-F: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD local area network over multimode fiber optic cable. (See IEEE Std 802.3, Clause 15.)

1.4.53 10BASE-FB port: A port on a repeater that contains an internal 10BASE-FB Medium Attachment Unit (MAU) that can connect to a similar port on another repeater. (See IEEE Std 802.3, Clause 9, Figure 15–1b, and Clause 17.)

1.4.54 10BASE-FB segment: A fiber optic link segment providing a point-to-point connection between two 10BASE-FB ports on repeaters. (See link segment IEEE Std 802.3, Figure 15–1b and Figure 15–2.)

1.4.55 10BASE-FL segment: A fiber optic link segment providing point-to-point connection between two 10BASE-FL Medium Attachment Units (MAUs). (See link segment IEEE Std 802.3, Figure 15–1c and Figure 15–2.)

1.4.56 10BASE-FP segment: A fiber optic mixing segment, including one 10BASE-FP Star and all of the attached fiber pairs. (See IEEE Std 802.3, Figure 15–1a, Figure 1–2, and mixing segment.)

1.4.57 10BASE-FP Star: A passive device that is used to couple fiber pairs together to form a 10BASE-FP segment. Optical signals received at any input port of the 10BASE-FP Star are distributed to all of its output ports (including the output port of the optical interface from which it was received). A 10BASE-FP Star is typically composed of a passive-star coupler, fiber optic connectors, and a suitable mechanical housing. (See IEEE Std 802.3, 16.5.)

1.4.58 10BASE-T: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD local area network over two pairs of twisted-pair telephone wire. (See IEEE Std 802.3, Clause 14.)

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1.4.59 10BASE-T1L: IEEE 802.3 Physical Layer specification for a 10 Mb/s Ethernet local area network over a single balanced pair of conductors up to at least 1000 m reach. (See IEEE Std 802.3, Clause 146.)

1.4.60 10BASE-T1S: IEEE 802.3 Physical Layer specification for a 10 Mb/s Ethernet local area network over a single balanced pair of conductors up to at least 15 m reach. (See IEEE Std 802.3, Clause 147.)

1.4.61 10BASE-Te: IEEE 802.3 Physical Layer specification for an energy-efficient version of 10BASE-T for a 10 Mb/s CSMA/CD local area network over two pairs of Category 5 or better-balanced cabling. (See IEEE Std 802.3, Clause 14.)

1.4.62 10BROAD36: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD local area network over single broadband cable. (See IEEE Std 802.3, Clause 11.)

1.4.63 10GBASE-BR10: IEEE 802.3 Physical Layer specification for a 10 Gb/s bidirectional link over one single-mode fiber with reach up to at least 10 km. There are different specifications for 10GBASE-BR10-D and 10GBASE-BR10-U; a transmission path connects one to the other. (See IEEE Std 802.3, Clause 158.)

1.4.64 10GBASE-BR20: IEEE 802.3 Physical Layer specification for a 10 Gb/s bidirectional link over one single-mode fiber with reach up to at least 20 km. There are different specifications for 10GBASE-BR20-D and 10GBASE-BR20-U; a transmission path connects one to the other. (See IEEE Std 802.3, Clause 158.)

1.4.65 10GBASE-BR40: IEEE 802.3 Physical Layer specification for a 10 Gb/s bidirectional link over one single-mode fiber with reach up to at least 40 km. There are different specifications for 10GBASE-BR40-D and 10GBASE-BR40-U; a transmission path connects one to the other. (See IEEE Std 802.3, Clause 158.)

1.4.66 10GBASE-CX4: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-X encoding over four lanes over shielded balanced copper cabling. (See IEEE Std 802.3, Clause 54.)

1.4.67 10GBASE-E: IEEE 802.3 PMD specifications for 10 Gb/s serial transmission using extra long wavelength. (See IEEE Std 802.3, Clause 52.)

1.4.68 10GBASE-ER: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-R encoding and 10GBASE-E optics. (See IEEE Std 802.3, Clause 49 and Clause 52.)

1.4.69 10GBASE-EW: IEEE 802.3 Physical Layer specification for 10Gb/s using 10GBASE-W encoding and 10GBASE-E optics. (See IEEE Std 802.3, Clause 50 and Clause 52.)

1.4.70 10GBASE-KR: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-R encoding over an electrical backplane. (See IEEE Std 802.3 Clause 72.)

1.4.71 10GBASE-KX4: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-X encoding over an electrical backplane. (See IEEE Std 802.3 Clause 71.)

1.4.72 10GBASE-L: IEEE 802.3 PMD specifications for 10 Gb/s serial transmission using long wavelength. (See IEEE Std 802.3, Clause 52)

1.4.73 10GBASE-LR: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-R encoding and 10GBASE-L optics. (See IEEE Std 802.3, Clause 49 and Clause 52.)

1.4.74 10GBASE-LRM: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-R encoding and long wavelength optics for multimode fiber (See IEEE Std 802.3 Clause 68).

1.4.75 10GBASE-LW: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-W encoding and 10GBASE-L optics. (See IEEE Std 802.3, Clause 50 and Clause 52.)

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1.4.76 10GBASE-LX4: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-X encoding over four WWDM lanes over multimode fiber. (See IEEE Std 802.3, Clause 54.)

1.4.77 10GBASE-PR: A collection of IEEE 802.3 Physical Layer specifications for a 10 Gb/s (10/10G-EPON) point-to-multipoint link over one single-mode optical fiber. (See IEEE Std 802.3, Table 56–1, Clause 75, Clause 76, and Clause 77.)

1.4.78 10GBASE-R: An IEEE 802.3 physical coding sublayer for serial 10 Gb/s operation. (See IEEE Std 802.3, Clause 49.)

1.4.79 10GBASE-S: IEEE 802.3 PMD specifications for 10 Gb/s serial transmission using short wavelength. (See IEEE Std 802.3, Clause 52.)

1.4.80 10GBASE-SR: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-R encoding and 10GBASE-S optics. (See IEEE Std 802.3, Clause 49 and Clause 52.)

1.4.81 10GBASE-SW: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-W encoding and 10GBASE-S optics. (See IEEE Std 802.3, Clause 50 and Clause 52.)

1.4.82 10GBASE-T: IEEE 802.3 Physical Layer specification for a 10 Gb/s LAN using four pairs of Class E or Class F balanced copper cabling. (See IEEE Std 802.3, Clause 55.)

1.4.83 10GBASE-T1: IEEE 802.3 Physical Layer specification for a 10 Gb/s Ethernet full duplex local area network over a single balanced pair of conductors. (See IEEE Std 802.3, Clause 149.)

1.4.84 10GBASE-W: An IEEE 802.3 physical coding sublayer for serial 10 Gb/s operation that is data-rate and format compatible with SONET STS-192c. (See IEEE Std 802.3, Clause 49.)

1.4.85 10GBASE-X: An IEEE 802.3 physical coding sublayer for 10 Gb/s operation over XAUI and four lane PMDs. (See IEEE Std 802.3, Clause 48.)

1.4.86 10G-EPON: An EPON architecture operating at 10 Gb/s in either downstream or both downstream and upstream directions. This term collectively refers to 10/10G-EPON and 10/1G-EPON architectures. (See IEEE Std 802.3, Clause 56.)

1.4.87 10 Gigabit Attachment Unit Interface (XAUI): The interface between two 10 Gigabit Extender Sublayers (XGXS) to extend the reach of the XGMII for 10 Gb/s operation. (See IEEE Std 802.3, Clause 47.)

1.4.88 10 Gigabit Media Independent Interface (XGMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation. (See IEEE Std 802.3, Clause 46.)

1.4.89 10 Gigabit Sixteen-Bit Interface (XSBI): The interface between the Physical Coding Sublayer (PCS) in 10GBASE-R or the WAN Interface Sublayer (WIS) in 10GBASE-W and the Physical Medium Attachment (PMA) sublayer for 10 Gb/s operation. (See IEEE Std 802.3, Clause 51.)

1.4.90 10GPASS-XR: A collection of IEEE 802.3 EPON Protocol over Coax (EPoC) Physical Layer specifications for up to 10 Gb/s downstream and up to 1.6 Gb/s upstream point-to-multipoint link over a coax cable distribution network. (See IEEE Std 802.3, Table 56–1, Clause 100, Clause 101, Clause 102, and Clause 103.)

1.4.91 10PASS-TS: IEEE 802.3 Physical Layer specification up to 100 Mb/s point-to-point link over single copper wire pair. (See IEEE Std 802.3, Clause 61 and Clause 62.)

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1.4.92 1BASE5: IEEE 802.3 Physical Layer specification for a 1 Mb/s CSMA/CD local area network over two pairs of twisted-pair telephone wire. (See IEEE Std 802.3, Clause 12.)

1.4.93 1-Event classification: The application of a single class event during PI probing (see IEEE Std 802.3, Clause 33, 33.2.6).

1.4.94 1-Event class signature: The response of the PD to 1-Event classification (see IEEE Std 802.3, Clause 33).

1.4.95 1G-EPON: An EPON architecture operating at 1 Gb/s in both downstream and upstream directions.

1.4.96 2.5GBASE-KX: IEEE 802.3 Physical Layer specification for 2.5 Gb/s using 2.5GBASE-X encoding over an electrical backplane. (See IEEE Std 802.3, Clause 128.)

1.4.97 2.5GBASE-T: IEEE 802.3 Physical Layer specification for a 2.5 Gb/s LAN using four pairs of Category 5e/Class D balanced copper cabling. (See IEEE Std 802.3, Clause 126.)

1.4.98 2.5GBASE-T1: IEEE 802.3 Physical Layer specification for a 2.5 Gb/s Ethernet full duplex local area network over a single balanced pair of conductors. (See IEEE Std 802.3, Clause 149.)

1.4.99 2.5GBASE-X: IEEE 802.3 physical coding and physical medium attachment for serial 2.5 Gb/s operation. (See IEEE Std 802.3, Clause 127.)

1.4.100 2.5GPII: The 2.5 Gb/s PCS Internal Interface is a logical interface that is internal to the 2.5GBASE-X PCS and exists solely for the purposes of defining the 2.5GBASE-X PCS functionality. (See IEEE Std 802.3, 127.2.5.1.)

1.4.101 2.5GSEI: The 2.5 Gb/s Interface from storage sub-system or bridge subsystem onto backplane (See IEEE Std 802.3, Annex 128A.)

1.4.102 200GBASE-CR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136)

1.4.103 200GBASE-DR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over four lanes of single-mode fiber, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 121.)

1.4.104 200GBASE-ER4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over four WDM lanes on single-mode fiber, with reach up to at least 40 km. (See IEEE Std 802.3, Clause 122.)

1.4.105 200GBASE-FR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over four WDM lanes on single-mode fiber, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 122.)

1.4.106 200GBASE-KR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

1.4.107 200GBASE-LR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over four WDM lanes on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 122.)

1.4.108 200GBASE-R: An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 119 for 200 Gb/s operation. (See IEEE Std 802.3, Clause 119.)

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1.4.109 200GBASE-SR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of multimode fiber with reach up to at least 100 m. (See IEEE Std 802.3, Clause 138.)

1.4.110 200 Gb/s Attachment Unit Interface (200GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 200 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. Two widths of 200GAUI-n are defined: an eight-lane version (200GAUI-8), and a four-lane version (200GAUI-4). (See IEEE Std 802.3, Annex 120B and Annex 120C for 200GAUI-8, or Annex 120D and Annex 120E for 200GAUI-4.)

1.4.111 200 Gb/s Media Independent Interface (200GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 200 Gb/s operation. (See IEEE Std 802.3, Clause 117.)

1.4.112 200GMII Extender: The 200 Gb/s Media Independent Interface Extender extends the reach of the 200GMII and consists of two 200GXS sublayers with a 200GAUI-n between them. (See IEEE Std 802.3, Clause 118.)

1.4.113 200GXS: The 200 Gb/s Extender Sublayer (200GXS) is part of the 200GMII Extender. In functionality, it is almost identical to the 200GBASE-R PCS Sublayer defined in Clause 119. Two types of 200GXS are defined: the DTE 200GXS adjacent to the RS sublayer and the PHY 200GXS adjacent to the PHY. (See IEEE Std 802.3, Clause 118.)

1.4.114 25/10G-EPON: An EPON architecture supporting a maximum sustained throughput of 25 Gb/s in the downstream direction and 10 Gb/s in the upstream direction (asymmetric rate).

1.4.115 25/25G-EPON: An EPON architecture supporting a maximum sustained throughput of 25 Gb/s in both downstream and upstream directions (symmetric rate).

1.4.116 25GBASE: A family of Physical Layer devices (PHYs) for 25 Gb/s operation. (See IEEE Std 802.3, Clause 105.)

1.4.117 25GBASE-BR10: IEEE 802.3 Physical Layer specification for a 25 Gb/s bidirectional link over one single-mode fiber with reach up to at least 10 km. There are different specifications for 25GBASE-BR10-D and 25GBASE-BR10-U; a transmission path connects one to the other. (See IEEE Std 802.3, Clause 159.)

1.4.118 25GBASE-BR20: IEEE 802.3 Physical Layer specification for a 25 Gb/s bidirectional link over one single-mode fiber with reach up to at least 20 km. There are different specifications for 25GBASE-BR20-D and 25GBASE-BR20-U; a transmission path connects one to the other. (See IEEE Std 802.3, Clause 159.)

1.4.119 25GBASE-BR40: IEEE 802.3 Physical Layer specification for a 25 Gb/s bidirectional link over one single-mode fiber with reach up to at least 40 km. There are different specifications for 25GBASE-BR40-D and 25GBASE-BR40-U; a transmission path connects one to the other. (See IEEE Std 802.3, Clause 159.)

1.4.120 25GBASE-CR: IEEE 802.3 Physical Layer specification for 25 Gb/s using 25GBASE-R encoding over one lane of twinaxial copper cable. (See IEEE Std 802.3, Clause 110.)

1.4.121 25GBASE-CR-S: IEEE 802.3 Physical Layer specification equivalent to 25GBASE-CR without support for the RS-FEC sublayer specified in Clause 108. (See IEEE Std 802.3, Clause 110.)

1.4.122 25GBASE-ER: IEEE 802.3 Physical Layer specification for 25 Gb/s using 25GBASE-R encoding over single-mode fiber, with reach up to at least 40 km. (See IEEE Std 802.3, Clause 114.)

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1.4.123 25GBASE-KR: IEEE 802.3 Physical Layer specification for 25 Gb/s using 25GBASE-R encoding over one lane of an electrical backplane. (See IEEE Std 802.3, Clause 111.)

1.4.124 25GBASE-KR-S: IEEE 802.3 Physical Layer specification equivalent to 25GBASE-KR without support for the RS-FEC sublayer specified in Clause 108. (See IEEE Std 802.3, Clause 111.)

1.4.125 25GBASE-LR: IEEE 802.3 Physical Layer specification for 25 Gb/s using 25GBASE-R encoding over single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 114.)

1.4.126 25GBASE-R: An IEEE 802.3 physical coding sublayer for one-lane 25 Gb/s operation. (See IEEE Std 802.3, Clause 107.)

1.4.127 25GBASE-SR: IEEE 802.3 Physical Layer specification for 25 Gb/s using 25GBASE-R encoding over multimode fiber. (See IEEE Std 802.3, Clause 112.)

1.4.128 25GBASE-T: IEEE 802.3 Physical Layer specification for a 25 Gb/s LAN using four pairs of ANSI/TIA Category 8, ISO/IEC Class I, or ISO/IEC Class II balanced copper cabling. (See IEEE Std 802.3, Clause 113.)

1.4.129 25G-EPON: An EPON architecture supporting a maximum sustained throughput of 25 Gb/s in either downstream or both downstream and upstream directions. This term collectively refers to 25/10G-EPON and 25/25G-EPON architectures. (See IEEE Std 802.3, Clause 56.)

1.4.130 25 Gigabit Attachment Unit Interface (25GAUI): A physical instantiation of the Physical Medium Attachment (PMA) service interface to extend the connection between 25 Gb/s capable PMAs over one lane, used for chip-to-chip or chip-to-module interconnections. (See IEEE Std 802.3, Annex 109A and Annex 109B.)

1.4.131 25 Gigabit Media Independent Interface (25GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 25 Gb/s operation. (See IEEE Std 802.3, Clause 106.)

1.4.132 2BASE-TL: IEEE 802.3 Physical Layer specification up to 5.696 Mb/s point-to-point link over single copper wire pair. (See IEEE Std 802.3, Clause 61 and Clause 63.)

1.4.133 2-Event classification: The application of two class events during PI probing (see IEEE Std 802.3, Clause 33, 33.2.6).

1.4.134 2-Event class signature: The response of the PD to 2-Event classification (see IEEE Std 802.3, Clause 33).

1.4.135 400GBASE-DR4: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over four lanes of single-mode fiber, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 124.)

1.4.136 400GBASE-ER8: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over eight WDM lanes on single-mode fiber, with reach up to at least 40 km. (See IEEE Std 802.3, Clause 122.)

1.4.137 400GBASE-FR4: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over four WDM lanes on single-mode fiber, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 151.)

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1.4.138 400GBASE-FR8: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over eight WDM lanes on single-mode fiber, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 122.)

1.4.139 400GBASE-LR4-6: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over four WDM lanes on single-mode fiber, with reach up to at least 6 km. (See IEEE Std 802.3, Clause 151.)

1.4.140 400GBASE-LR8: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over eight WDM lanes on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 122.)

1.4.141 400GBASE-R: An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 119 for 400 Gb/s operation. (See IEEE Std 802.3, Clause 119.)

1.4.142 400GBASE-SR16: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding over sixteen lanes of multimode fiber, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 123.)

1.4.143 400GBASE-SR4.2: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding over eight lanes on multimode fiber in a bidirectional WDM format, with reach up to at least 150 m. (See IEEE Std 802.3, Clause 150.)

1.4.144 400GBASE-SR8: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding over eight lanes of multimode fiber, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 138.)

1.4.145 400 Gb/s Attachment Unit Interface (400GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 400 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. Two widths of 400GAUI-n are defined: a sixteen-lane version (400GAUI-16), and an eight-lane version (400GAUI-8). (See IEEE Std 802.3, Annex 120B and Annex 120C for 400GAUI-16, or Annex 120D and Annex 120E for 400GAUI-8.)

1.4.146 400 Gb/s Media Independent Interface (400GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 400 Gb/s operation. (See IEEE Std 802.3, Clause 117.)

1.4.147 400GMII Extender: The 400 Gb/s Media Independent Interface Extender extends the reach of the 400GMII and consists of two 400GXS sublayers with a 400GAUI-n between them. (See IEEE Std 802.3, Clause 118.)

1.4.148 400GXS: The 400 Gb/s Extender Sublayer (400GXS) is part of the 400GMII Extender. In functionality, it is almost identical to the 400GBASE-R PCS Sublayer defined in Clause 119. Two types of 400GXS are defined: the DTE 400GXS adjacent to the RS sublayer and the PHY 400GXS adjacent to the PHY. (See IEEE Std 802.3, Clause 118.)

1.4.149 40GBASE-CR4: IEEE 802.3 Physical Layer specification for 40 Gb/s using 40GBASE-R encoding over four lanes of shielded balanced copper cabling, with reach up to at least 7 m. (See IEEE Std 802.3, Clause 85.)

1.4.150 40GBASE-ER4: IEEE 802.3 Physical Layer specification for 40 Gb/s using 40GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 40 km. (See IEEE Std 802.3, Clause 87.)

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1.4.151 40GBASE-FR: IEEE 802.3 Physical Layer specification for 40 Gb/s serial transmission using 40GBASE-R encoding over one wavelength on single-mode fiber, with reach up to at least 2 km (See IEEE Std 802.3, Clause 89.)

1.4.152 40GBASE-KR4: IEEE 802.3 Physical Layer specification for 40 Gb/s using 40GBASE-R encoding over four lanes of an electrical backplane, with reach up to at least 1 m. (See IEEE Std 802.3, Clause 84.)

1.4.153 40GBASE-LR4: IEEE 802.3 Physical Layer specification for 40 Gb/s using 40GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 87.)

1.4.154 40GBASE-R: An IEEE 802.3 family of Physical Layer devices using 40GBASE-R encoding. (See IEEE Std 802.3, Clause 80.)

1.4.155 40GBASE-R encoding: The physical coding sublayer encoding defined in Clause 82 for 40 Gb/s operation. (See IEEE Std 802.3, Clause 82.)

1.4.156 40GBASE-SR4: IEEE 802.3 Physical Layer specification for 40 Gb/s using 40GBASE-R encoding over four lanes of multimode fiber, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 86.)

1.4.157 40GBASE-T: IEEE 802.3 Physical Layer specification for a 40 Gb/s LAN using four pairs of ANSI/TIA Category 8, ISO/IEC Class I, or ISO/IEC Class II balanced copper cabling. (See IEEE Std 802.3, Clause 113.)

1.4.158 40 Gb/s Attachment Unit Interface (XLAUI): A physical instantiation of the PMA service interface to extend the connection between 40 Gb/s capable PMAs, used for chip-to-chip or chip-to-module interconnections. (See IEEE Std 802.3, Annex 83A and Annex 83B.)

1.4.159 40 Gb/s Media Independent Interface (XLGMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 40 Gb/s operation. (See IEEE Std 802.3, Clause 81.)

1.4.160 40 Gb/s Parallel Physical Interface (XLPPI): The interface between the Physical Medium Attachment (PMA) sublayer and the Physical Medium Dependent (PMD) sublayer for 40GBASE-SR4 and 40GBASE-LR4 PHYs. (See IEEE Std 802.3, Annex 86A.)

1.4.161 4B/3B: For IEEE 802.3, the data encoding technique used by 100BASE-T1 when converting 4-bit (4B) MII data with 25 MHz clock to 3-bit (3B) data with $33.33\overline{3}$ MHz clock. (See IEEE Std 802.3, 96.3.3.1.2.)

1.4.162 4D-PAM5: The symbol encoding method used in 1000BASE-T. The four-dimensional quinary symbols (4D) received from the 8B1Q4 data encoding are transmitted using five voltage levels (PAM5). Four symbols are transmitted in parallel each symbol period. (See IEEE Std 802.3, Clause 40.)

1.4.163 50/10G-EPON: An EPON architecture supporting a maximum sustained throughput of 50 Gb/s in the downstream direction and 10 Gb/s in the upstream direction (asymmetric rate). (See IEEE Std 802.3, Clause 56.)

1.4.164 50/25G-EPON: An EPON architecture supporting a maximum sustained throughput of 50 Gb/s in the downstream direction and 25 Gb/s in the upstream direction (asymmetric rate). (See IEEE Std 802.3, Clause 56.)

1.4.165 50/50G-EPON: An EPON architecture supporting a maximum sustained throughput of 50 Gb/s in both downstream and upstream directions (symmetric rate). (See IEEE Std 802.3, Clause 56.)

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1.4.166 50GBASE-BR10: IEEE 802.3 Physical Layer specification for a 50 Gb/s bidirectional link over one single-mode fiber with reach up to at least 10 km. There are different specifications for 50GBASE-BR10-D and 50GBASE-BR10-U; a transmission path connects one to the other. (See IEEE Std 802.3 Clause 160.)

1.4.167 50GBASE-BR20: IEEE 802.3 Physical Layer specification for a 50 Gb/s bidirectional link over one single-mode fiber with reach up to at least 20 km. There are different specifications for 50GBASE-BR20-D and 50GBASE-BR20-U; a transmission path connects one to the other. (See IEEE Std 802.3, Clause 160.)

1.4.168 50GBASE-BR40: IEEE 802.3 Physical Layer specification for a 50 Gb/s bidirectional link over one single-mode fiber with reach up to at least 40 km. There are different specifications for 50GBASE-BR40-D and 50GBASE-BR40-U; a transmission path connects one to the other. (See IEEE Std 802.3, Clause 160.)

1.4.169 50GBASE-CR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over one lane of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136.)

1.4.170 50GBASE-ER: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 40 km. (See IEEE Std 802.3, Clause 139.)

1.4.171 50GBASE-FR: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 139.)

1.4.172 50GBASE-KR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over one lane of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

1.4.173 50GBASE-LR: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 139.)

1.4.174 50GBASE-R: An IEEE 802.3 physical coding sublayer for one-lane 50 Gb/s operation. (See IEEE Std 802.3, Clause 131.)

1.4.175 50GBASE-SR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over multimode fiber with reach up to at least 100 m. (See IEEE Std 802.3, Clause 138.)

1.4.176 50 Gb/s Attachment Unit Interface (50GAUI-n, LAUI-2): A physical instantiation of the PMA service interface to extend the connection between 50 Gb/s capable PMAs over one lane (50GAUI-1) or two lanes (50GAUI-2, LAUI-2), used for chip-to-chip or chip-to-module interconnections. (See IEEE Std 802.3, Clause 135 and Annex 135B through Annex 135G.)

1.4.177 50 Gb/s Media Independent Interface (50GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 50 Gb/s operation. (See IEEE Std 802.3, Clause 132.)

1.4.178 50G-EPON: An EPON architecture supporting a maximum sustained throughput of 50 Gb/s in either downstream or both downstream and upstream directions. This term collectively refers to 50/10G-EPON, 50/25G-EPON, and 50/50G-EPON architectures. (See IEEE Std 802.3, Clause 56.)

1.4.179 5GBASE-KR: IEEE 802.3 Physical Layer specification for 5 Gb/s using 5GBASE-R encoding over an electrical backplane. (See IEEE Std 802.3, Clause 130.)

1.4.180 5GBASE-R: An IEEE 802.3 physical coding sublayer and physical medium attachment sublayer for serial 5 Gb/s operation. (See IEEE Std 802.3, Clause 129.)

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1.4.181 5GBASE-T: IEEE 802.3 Physical Layer specification for a 5 Gb/s LAN using four pairs of Category 5e/Class D balanced copper cabling. (See IEEE Std 802.3, Clause 126.)

1.4.182 5GBASE-T1: IEEE 802.3 Physical Layer specification for a 5 Gb/s Ethernet full duplex local area network over a single balanced pair of conductors. (See IEEE Std 802.3, Clause 149.)

1.4.183 5GSEI: The 5 Gb/s Interface from storage sub-system or bridge subsystem onto backplane (See IEEE Std 802.3, Annex 130A.)

1.4.184 64B/65B transmission code: A block oriented encoding where 64-bit blocks are prepended with a single bit to indicate whether the block contains only data or a mix of data and control information. The details of each 64B/65B encoding are specific to the PCS. (See IEEE Std 802.3, Clause 55, and Clause 115.)

1.4.185 8B/10B transmission code: A DC-balanced octet-oriented data encoding specified in IEEE Std 802.3, Table 36–1a–e and Table 36–2.

1.4.186 8B1Q4: For IEEE 802.3, the data encoding technique used by 1000BASE-T when converting GMII data (8B-8 bits) to four quinary symbols (Q4) that are transmitted during one clock (1Q4). (See IEEE Std 802.3, Clause 40.)

1.4.187 ability: A mode that a device can advertise using Auto-Negotiation. For modes that represent a type of data service, a device shall be able to operate that data service before it may advertise this ability. A device may support multiple abilities. (See IEEE Std 802.3, 28.2.1.2.2.)

1.4.188 Acknowledge Bit: A bit used by IEEE 802.3 Auto-Negotiation to indicate that a station has successfully received multiple identical copies of the link codeword. This bit is only set after an identical link codeword has been received three times in succession. (See IEEE Std 802.3, 28.2.1.2.5.)

1.4.189 advertised ability: An operational mode that is advertised using Auto-Negotiation. (See IEEE Std 802.3, 28.2.1.2.2.)

1.4.190 agent: A term used to refer to the managed nodes in a network. Managed nodes are those nodes that contain a network management entity (NME), which can be used to configure the node and/or collect data describing operation of that node. The agent is controlled by a network control host or manager that contains both an NME and network management application (NMA) software to control the operations of agents. Agents include systems that support user applications as well as nodes that provide communications services such as front-end processors, bridges, and routers. (See IEEE Std 802.3, Clause 30.)

1.4.191 agent code: A term used to refer to network management entity software residing in a node that can be used to remotely configure the host system based on commands received from the network control host, collect information documenting the operation of the host, and communicate with the network control host. (See IEEE Std 802.3, Clause 30.)

1.4.192 Aggregation group: A collection of PMEs that may be aggregated according to a particular implementation of the PME aggregation function. (See IEEE Std 802.3, 61.2.2.)

1.4.193 agile device: A device that supports automatic switching between multiple Physical Layer technologies. (See IEEE Std 802.3, Clause 28.)

1.4.194 ampacity: The maximum current, in ampere, that a conductor can carry continuously under the conditions of use without exceeding its temperature rating.

1.4.195 AN half-duplex function: The ability to exchange Auto-Negotiation DME pages over a single differential-pair medium. (See IEEE Std 802.3, Clause 98.)

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1.4.196 anomaly: A discrepancy between the actual and desired characteristics of an item. This definition is derived from ATIS-0600416.1999(R2010) and ATIS-0900105.2008, which take precedence.

1.4.197 arbitration: In 1000BASE-X, Auto-Negotiation process that ensures proper sequencing of configuration information between link partners using the Physical Coding Sublayer (PCS) Transmit and Receive functions. (See IEEE Std 802.3, Clause 36 and Clause 37.)

1.4.198 Attachment Unit Interface (AUI): In 10 Mb/s CSMA/CD, the interface between the Medium Attachment Unit (MAU) and the data terminal equipment (DTE) within a data station. Note that the AUI carries encoded signals and provides for duplex data transmission. (See IEEE Std 802.3, Clause 7 and Clause 8.)

1.4.199 Auto-Negotiation: The algorithm that allows two devices at either end of a link segment to negotiate common data service functions. (See IEEE Std 802.3, Clause 28, Clause 37, Clause 73, and Clause 98.)

1.4.200 balanced cable: A cable consisting of one or more metallic symmetrical cable elements (twisted pairs or quads). (From ISO/IEC 11801.)

1.4.201 Bandplan: The set of parameters that control the lowest and highest frequencies and power at which 10PASS-TS and 2BASE-TL may operate.

1.4.202 baseband coaxial system: A system whereby information is directly encoded and impressed upon the transmission medium. At any point on the medium only one information signal at a time can be present without disruption.

1.4.203 Base link codeword: The first 16-bit message exchanged during IEEE 802.3 Auto-Negotiation. (See IEEE Std 802.3, 28.2.1.2.)

1.4.204 Base Page: *See:* **Base link codeword**.

1.4.205 BASE-R: An IEEE 802.3 family of Physical Layer devices using the 64B/66B encoding defined in Clause 49, Clause 82, Clause 107, Clause 119, or Clause 129 of IEEE Std 802.3.

1.4.206 BASE-T1: PHYs that belong to the set of specific Ethernet PCS/PMA/PMDs that operate on a single twisted-pair copper cable, including 10BASE-T1L, 10BASE-T1S, 100BASE-T1, and 1000BASE-T1. (See IEEE Std 802.3, Clause 96, Clause 97, Clause 146, and Clause 147.)

1.4.207 basic frame: A MAC frame that carries a Length/Type field with the Length or Type interpretation and has a maximum length of 1518 octets. The basic frame is not intended to allow inclusion of additional tags (i.e., untagged) or encapsulations required by higher layer protocols. (See IEEE Std 802.3, 3.2.7.)

1.4.208 baud (Bd): A unit of signaling speed, expressed as the number of times per second the signal can change the electrical state of the transmission line or other medium.

NOTE—Depending on the encoding strategies, a signal event may represent a single bit, more, or less than one bit. *Contrast with:* **bit rate**; **bits per second**. (From IEEE Std 610.7-1995 [B38].)

1.4.209 Binary Phase Shift Keying (Binary PSK or BPSK): A form of modulation in which binary data are transmitted by changing the carrier phase by 180 degrees. (See IEEE Std 802.3, Clause 11.)

1.4.210 bit cell: The time interval used for the transmission of a single data (CD0 or CD1) or control (CVH or CVL) symbol.

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1.4.211 bit error ratio (BER): The ratio of the number of bits received in error to the total number of bits received.

1.4.212 bit interleaved parity N (BIP-N): A method of error monitoring using even (or odd) parity, such that an N-bit codeword is generated over a specified portion of an input data stream in such a manner that the i-th bit of the codeword provides even (or odd) parity over the i-th bit of all N-bit sequences in the covered portion of the data stream. This definition is derived from ATIS-0600416.1999(R2010) and ATIS-0900105.2008, which take precedence.

1.4.213 bit rate (BR): The total number of bits per second transferred to or from the Media Access Control (MAC). For example, 100BASE-T has a bit rate of one hundred million bits per second (10^8 b/s).

1.4.214 bit rate (BR)/2: One-half of the BR in hertz.

1.4.215 bit time (BT): The duration of one bit as transferred to and from the Media Access Control (MAC). The bit time is the reciprocal of the bit rate. For example, for 100BASE-T the bit time is 10^{-8} s or 10 ns.

1.4.216 black link approach: The specification of the input, output, and transfer characteristics of the unidirectional transmission path from TP2 to TP3 for a given dense wavelength division multiplexing (DWDM) channel within a DWDM black link, without specifying how the transmission path is implemented. (See, for example, IEEE Std 802.3, Clause 154, Figure 154–3.)

1.4.217 BR/2: *See:* **bit rate (BR)/2.**

1.4.218 branch cable: In 10BROAD36, the Attachment Unit Interface (AUI) cable interconnecting the data terminal equipment and Medium Attachment Unit (MAU) system components.

1.4.219 bridge: A layer 2 interconnection device that does not form part of a CSMA/CD collision domain but conforms to IEEE Std 802.1Q. A bridge does not form part of a CSMA/CD collision domain but, rather appears as a Media Access Control (MAC) to the collision domain. (See also IEEE 100.)

1.4.220 broadband local area network (LAN): A local area network in which information is transmitted on modulated carriers, allowing coexistence of multiple simultaneous services on a single physical medium by frequency division multiplexing. (See IEEE Std 802.3, Clause 11.)

1.4.221 bundle: A group of signals that have a common set of characteristics and differ only in their information content.

1.4.222 carrier extension: The addition of non-data symbols to the end of frames that are less than slotTime bits in length so that the resulting transmission is at least one slotTime in duration.

1.4.223 carrier sense: In a local area network, an ongoing activity of a data station to detect whether another station is transmitting.

NOTE—The carrier sense signal indicates that one or more DTEs are currently transmitting.

1.4.224 Category 3 balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 16 MHz (i.e., performance meets the requirements of a Class C link as per ISO/IEC 11801:1995). Commonly used by IEEE 802.3 10BASE-T installations. In addition to the requirements outlined in ISO/IEC 11801:1995, IEEE Std 802.3 Clause 14, Clause 23, and Clause 32 specify additional requirements for cabling when used with 10BASE-T, 100BASE-T4, and 100BASE-T2.

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1.4.225 Category 4 balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 20 MHz as per ISO/IEC 11801:1995. In addition to the requirements outlined in ISO/IEC 11801:1995, IEEE Std 802.3 Clause 14, Clause 23, and Clause 32 specify additional requirements for this cabling when used with 10BASE-T, 100BASE-T4, and 100BASE-T2.

1.4.226 Category 5 balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 100 MHz (i.e., cabling components meet the performance specified in ISO/IEC 11801:1995 and ANSI/EIA/TIA-568-A-1995). In addition to the requirements outlined in ISO/IEC 11801:1995 and ANSI/EIA/TIA-568-A-1995, IEEE Std 802.3 Clause 14, Clause 23, Clause 25, and Clause 40 specify additional requirements for this cabling when used with 10BASE-T, 100BASE-T4, 100BASE-TX, and 1000BASE-T.

1.4.227 Category 5e balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 100 MHz per ISO/IEC 11801:2002 and ANSI/TIA-568-B.2-2001. (See IEEE Std 802.3, Clause 14, Clause 25, Clause 40, Clause 33, and Clause 126.)

1.4.228 Category 6A balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 500 MHz (i.e., cabling components meet the performance specified in ISO/IEC 11801:2002 Amendment 2 and ANSI/TIA-568-C.2). In addition to the requirements outlined in ISO/IEC 11801:2002 Amendment 2 and ANSI/TIA-568-C.2, IEEE Std 802.3 Clause 14, Clause 23, Clause 25, Clause 40, Clause 55, and Clause 126 specify additional requirements for this cabling when used with 10BASE-T, 100BASE-T4, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T.

1.4.229 Category 6 balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 250 MHz per ISO/IEC 11801:2002 and ANSI/TIA-568-C.2-2009. (See IEEE Std 802.3, Clause 14, Clause 25, Clause 40, Clause 55, Clause 33, and Clause 126.)

1.4.230 Category 7A balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 1000 MHz (i.e., cabling components meet the performance specified in ISO/IEC 11801:2002 Amendment 2). In addition to the requirements outlined in ISO/IEC 11801:2002 Amendment 2, IEEE Std 802.3 Clause 14, Clause 23, Clause 25, Clause 40, Clause 55, and Clause 126 specify additional requirements for this cabling when used with 10BASE-T, 100BASE-T4, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T.

1.4.231 Category 7 balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 600 MHz (i.e., cabling components meet the performance specified in ISO/IEC 11801:2002). In addition to the requirements outlined in ISO/IEC 11801:2002, IEEE Std 802.3 Clause 14, Clause 23, Clause 25, Clause 40, Clause 55, and Clause 126 specify additional requirements for this cabling when used with 10BASE-T, 100BASE-T4, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T.

1.4.232 Category 8 balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 2000 MHz (i.e., cabling components that meet the Category 8.1 or Category 8.2 requirements specified in ISO/IEC DIS 11801-1:2016 or Category 8 specified in ANSI/TIA-568-C.2-1-2016). In addition to the requirements outlined in ISO/IEC DIS 11801-1 and ANSI/TIA-568-C.2-1, IEEE Std 802.3 Clause 14, Clause 23, Clause 25, Clause 40, Clause 55, Clause 113, and Clause 126 specify additional requirements for this cabling when used with 10BASE-T, 100BASE-T4, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, 10GBASE-T, 25GBASE-T, and 40GBASE-T.

1.4.233 CATV-type broadband medium: *See:* **Community Antenna Television (CATV)-type broadband medium.**

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1.4.234 center wavelength: The average of two optical wavelengths at which the spectral radiant intensity is 50% of the maximum value. (See IEEE Std 802.3, Clause 11.)

1.4.235 channel: In 10BROAD36 and 10GPASS-XR, a band of frequencies dedicated to a certain service transmitted on the broadband medium. Otherwise, a defined path along which data in the form of an electrical or optical signal passes. (For 10BROAD36, see IEEE Std 802.3, Clause 11, for 10GPASS-XR see Clause 100, Clause 101, and Clause 102.)

1.4.236 channel insertion loss: As used in IEEE 802.3 for fiber optic links, the static loss of light through a link between a transmitter and receiver. It includes the loss of the fiber, connectors, and splices and, for EPON links, optional power splitter/combiner.

1.4.237 Channel Operating Margin (COM): A figure of merit for a channel derived from a measurement of its scattering parameters. (See IEEE Std 802.3, Clause 93A.1.)

1.4.238 channel spacing: The center-to-center difference in frequency or wavelength between adjacent channels in a WDM application. Dense wavelength division multiplexing (DWDM) channel spacings are based on the grid found in ITU-T G.694.1.

1.4.239 chassis ground: The electrical node that contains the chassis (see IEEE 100).

1.4.240 circuit: The physical medium on which signals are carried across the Attachment Unit Interface (AUI) for 10BASE-T or Media Independent Interface (MII) for 100BASE-T. For 10BASE-T, the data and control circuits consist of an A circuit and a B circuit forming a balanced transmission system so that the signal carrier on the B circuit is the inverse of the signal carried on the A circuit.

1.4.241 Class II repeater: A type of IEEE 802.3 100BASE-T repeater set with internal delay such that only two or fewer such repeater sets may exist between any two DTEs within a single collision domain when two maximum length copper cable segments are used. (See IEEE Std 802.3, Clause 27.)

1.4.242 Class I repeater: A type of 100BASE-T repeater set with internal delay such that only one repeater set may exist between any two DTEs within a single collision domain when two maximum length copper cable segments are used. (See IEEE Std 802.3, Clause 27.)

1.4.243 Clocked Data One (CD1): A Manchester-encoded data 1. A CD1 is encoded as a LO for the first half of the bit-cell and a HI for the second half of the bit-cell. (See IEEE Std 802.3, Clause 12.)

1.4.244 Clocked Data Zero (CD0): A Manchester-encoded data 0. A CD0 is encoded as a HI for the first half of the bit-cell and a LO for the second half of the bit-cell. (See IEEE Std 802.3, Clause 12.)

1.4.245 Clocked Violation HI (CVH): A symbol that deliberately violates Manchester-encoding rules, used as a part of the Collision Presence signal. A CVH is encoded as a transition from LO to HI at the beginning of the bit cell, HI for the entire bit cell, and a transition from HI to LO at the end of the bit cell. (See IEEE Std 802.3, Clause 12.)

1.4.246 Clocked Violation LO (CVL): A symbol that deliberately violates Manchester-encoding rules, used as a part of the Collision Presence signal. A CVL is encoded as a transition from HI to LO at the beginning of the bit cell, LO for the entire bit cell, and a transition from LO to HI at the end of the bit cell. (See IEEE Std 802.3, Clause 12.)

1.4.247 coax cable distribution network (CCDN): A radio frequency (RF) distribution plant composed of either amplified or passive coaxial media.

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1.4.248 coaxial cable: A two-conductor (center conductor, shield system), concentric, constant impedance transmission line used as the trunk medium in the baseband system.

1.4.249 coaxial cable interface: The electrical and mechanical interface to the shared coaxial cable medium either contained within or connected to the Medium Attachment Unit (MAU). Also known as the Medium Dependent Interface (MDI).

1.4.250 coaxial cable section: A single length of coaxial cable, terminated at each end with a male BNC connector. Cable sections are joined to other cable sections via BNC plug/receptacle barrel or Type T adapters.

1.4.251 coaxial cable segment: A length of coaxial cable made up from one or more coaxial cable sections and coaxial connectors, and terminated at each end in its characteristic impedance.

1.4.252 coax line terminal (CLT): The network-end DTE for a coaxial access network. The CLT is the master entity in a P2MP EPoC network with regard to the MPCP protocol.

1.4.253 coax network unit (CNU): The subscriber-end DTE to a coaxial access network. A CNU is a slave entity in a P2MP EPoC network with regard to the MPCP protocol.

1.4.254 code-bit: Within IEEE 802.3, in 100BASE-T, the unit of data passed across the Physical Medium Attachment (PMA) service interface, and the smallest signaling element used for transmission on the medium. A group of five code-bits constitutes a code-group in the 100BASE-X Physical Coding Sublayer (PCS). (See IEEE Std 802.3, Clause 24.)

1.4.255 code-group: For IEEE 802.3, a set of encoded symbols representing encoded data or control information. For 100BASE-T4, a set of six ternary symbols that, when representing data, conveys an octet. For 100BASE-TX and 100BASE-FX, a set of five code-bits that, when representing data, conveys a nibble. For 100BASE-T2, a pair of PAM5×5 symbols that, when representing data, conveys a nibble. For 1000BASE-X, a set of ten bits that, when representing data, conveys an octet. For 1000BASE-T, a vector of four 8B1Q4 coded quinary symbols that, when representing data, conveys an octet. For 100BASE-T1, a set of ternary symbols that, when representing data, conveys three bits, as defined in 96.3. For 10BASE-T1L, a set of three ternary symbols that, when representing data, conveys a nibble, as defined in 146.3. (See IEEE Std 802.3, Clause 23, Clause 24, Clause 32, Clause 36, Clause 40, Clause 96, and Clause 146.)

1.4.256 code-group alignment: In 1000BASE-X, the receiver action that resets the existing code-group boundary to that of the comma or K28.5 character currently being received. (See IEEE Std 802.3, Clause 36.)

1.4.257 code-group slipping: In 1000BASE-X, the receiver action to align the correct receive clock and code-group containing a comma. (See IEEE Std 802.3, Clause 36.)

1.4.258 Code Rule Violation (CRV): An analog waveform that is not the result of the valid Manchester-encoded output of a single optical transmitter. The collision of two or more 10BASE-FB optical transmissions will cause multiple CRVs. The preamble encoding of a single 10BASE-FP optical transmission contains a single CRV. (See IEEE Std 802.3, 16.3.1.1.)

1.4.259 collision: A condition that results from concurrent transmissions from multiple data terminal equipment (DTE) sources within a single collision domain.

1.4.260 collision domain: A single, half duplex mode CSMA/CD network. If two or more Media Access Control (MAC) sublayers are within the same collision domain and both transmit at the same time, a collision will occur. MAC sublayers separated by a repeater are in the same collision domain. MAC sublayers separated by a bridge are within different collision domains. (See IEEE Std 802.3.)

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1.4.261 collision presence: A signal generated within the Physical Layer by an end station or hub to indicate that multiple stations are contending for access to the transmission medium. (See IEEE Std 802.3, Clause 8 and Clause 12.)

1.4.262 comma: In 1000BASE-X, the seven-bit sequence that is part of an 8B/10B code-group that is used for the purpose of code-group alignment. (See IEEE Std 802.3, Clause 36.)

1.4.263 comma-: In 1000BASE-X, the seven-bit sequence (1100000) of an encoded data stream. (See IEEE Std 802.3, Clause 36.)

1.4.264 comma+: In 1000BASE-X, the seven-bit sequence (0011111) of an encoded data stream. (See IEEE Std 802.3, Clause 36.)

1.4.265 common-mode voltage: The instantaneous algebraic average of two signals applied to a balanced circuit, with both signals referenced to a common reference. Also called *longitudinal voltage* in the telephone industry.

1.4.266 Community Antenna Television (CATV)-type broadband medium: A broadband system comprising coaxial cables, taps, splitters, amplifiers, and connectors the same as those used in CATV or cable television installations. (See IEEE Std 802.3, Clause 11.)

1.4.267 Company ID (CID): A 24-bit unique number that identifies a manufacturer or other organization. A CID is used as a globally unique identifier on its own, and may be included as part of a context dependent identifier, as part of a protocol identifier, in other management data, etc. Any MAC addresses created from a CID are by definition, locally administered and not guaranteed to be unique in any MAC address context. OUI (see 1.4.440) and CID are non-overlapping and therefore mutually unique.

NOTE—See https://standards.ieee.org/develop/regauth/

1.4.268 compatibility interfaces: Several hardware points of attachment have been defined by this standard to allow connection of independently designed and manufactured components to the transmission medium. (See IEEE Std 802.3, 1.1.3.2.)

1.4.269 container: An SDH term that is equivalent to the payload capacity of a synchronous payload envelope. This definition is derived from ATIS-0900105.2008 and ATIS-0600416.1999(R2010), which take precedence.

1.4.270 continuous wave (CW): A carrier that is not modulated or switched.

1.4.271 Control mode: In 1000BASE-T, the period of operation in which the PHY is transmitting code-groups that represent control information. The end of a frame is accompanied by a transition to the Control mode, which immediately follows the Data mode and precedes the Idle mode. This occurs when the GMII signal TX_EN is set FALSE. During this time, several control fields are transmitted as code-groups to complete a stream. These include two convolutional encoder reset code-groups, two End-of-Stream delimiter (ESD) code-groups and, possibly, carrier extend code-groups. In 100BASE-T1, the period of operation in which the PHY is transmitting code-groups that represent control information. The end of a frame is accompanied by a transition to the Control mode, which immediately follows the Data mode and precedes the Idle mode. This occurs when the MII signal TX_EN is set FALSE. During this time, several control fields are transmitted as code-groups to complete a stream. (See IEEE Std 802.3, Clause 40 and Clause 96.)

1.4.272 Control Signal One (CS1): An encoded control signal used on the Control In and Control Out circuits. A CS1 is encoded as a signal at half the bit rate (BR)/2). (See IEEE Std 802.3, Clause 7.)

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1.4.273 Control Signal Zero (CS0): An encoded control signal used on the Control In and Control Out circuits. A CS0 is encoded as a signal at the bit rate (BR). (See IEEE Std 802.3, Clause 7.)

1.4.274 Coupled Power Ratio (CPR): The ratio (in dB) of the total power coupled into a multimode fiber to the optical power that can be coupled into a single-mode fiber.

1.4.275 cross connect: A group of connection points, often wall- or rack-mounted in a wiring closet, used to mechanically terminate and interconnect twisted-pair building wiring.

1.4.276 cyclic prefix (CP): A redundant set of samples prepended to an OFDM symbol.

1.4.277 data frame: Use of this term is restricted to Clause 9, 27 and 41 (*See:* **MAC Frame**).

1.4.278 Data mode: In 1000BASE-T, the period of operation in which the PHY is transmitting code-groups that represent data. This mode is preceded by a start of a frame during which the GMII signal TX_EN is set TRUE for data transmission. This mode begins with transmission of two Start-of-Stream delimiter code-groups followed by code-groups encoded from the data octets arriving on TXD<7:0> via the GMII. In 100BASE-T1, the period of operation in which the PHY is transmitting code-groups that represent data. This mode is preceded by a start of a frame during which the MII signal TX_EN is set TRUE for data transmission. This mode begins with transmission of three Start-of-Stream delimiter code-groups followed by code-groups encoded from the data nibbles arriving on TXD<3:0> via the MII. (See IEEE Std 802.3 Clause 40 and Clause 96.)

1.4.279 data terminal equipment (DTE): Any source or destination of data connected to the local area network.

1.4.280 dBm: Decibels referenced to 1.0 mW.

1.4.281 dBmV: Decibels referenced to 1.0 mV measured at the same impedance. Used to define signal levels in Community Antenna Television (CATV)-type broadband systems. (See IEEE Std 802.3 Clause 11.)

1.4.282 dedicated service: A CSMA/CD network in which the collision domain consists of two and only two DTEs so that the total network bandwidth is dedicated to supporting the flow of information between them.

1.4.283 deep sleep: One of the two modes of operation for Energy-Efficient Ethernet. Deep sleep refers to the mode for which the transmitter ceases transmission during Low Power Idle to maximize the energy saving potential. (See IEEE Std 802.3, Figure 78–3).

1.4.284 defect: A limited interruption in the ability of an item to perform a required function. This definition is derived from ATIS-0600416.1999(R2010) and ATIS-0900105.2008, which take precedence.

1.4.285 dense wavelength division multiplexing: An optical WDM technology where the frequency spacing is less than or equal to 1000 GHz.

1.4.286 differential group delay (DGD): The time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal.

1.4.287 differential Manchester encoding: Data encoding system used in Backplane Ethernet for Auto-Negotiation signaling and 10GBASE-KR training frame control channel encoding. (See IEEE Std 802.3 72.6.10.2.2 and 73.5.)

1.4.288 differential-mode voltage: The instantaneous algebraic difference between the potential of two signals applied to the two sides of a balanced circuit. Also called *metallic voltage* in the telephone industry.

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1.4.289 differential skew: The difference in time between the midpoint voltage crossings of the true and complement components of a differential signal.

1.4.290 dispersion slope: The rate of change of the chromatic dispersion of a fiber with wavelength.

1.4.291 Downstream: In an access network, where there is a clear indication in each deployment as to which end of a link is closer to a subscriber, transmission toward the subscriber end of the link.

1.4.292 drop cable: In 10BROAD36, the small diameter flexible coaxial cable of the broadband medium that connects to a Medium Attachment Unit (MAU). (*See:* **trunk cable**.)

1.4.293 DSQ128: The 128 point double square (DSQ) constellation mapping used in 10GBASE-T. This constellation is obtained by taking a 2D constellation with 16-level pulse amplitude modulation (PAM16) on each dimension and eliminating half the points to create a checkerboard pattern. This constellation is based on a lattice called RZ^2 in the literature. (See IEEE Std 802.3, Clause 55.)

NOTE—See also Forney [B28A][32]

1.4.294 dual duplex: Within IEEE 802.3, a signaling system that supports simultaneous duplex communication over two cabling pairs.

1.4.295 dual-signature PD: A PD that has independent detection signatures, class signatures, and maintain power signatures on each pairset. (See IEEE Std 802.3, Clause 145.)

1.4.296 duplex channel: Within IEEE 802.3, a communications channel capable of simultaneous duplex communication.

1.4.297 DWDM black link: An aggregate of pairs of dense wavelength division multiplexing (DWDM) channels, with each pair supporting one full duplex connection where the implementation of the transmission paths is not specified.

1.4.298 DWDM channel: The transmission path from TP2 associated with a transmitting DWDM PHY, to TP3 at a receiving DWDM PHY.

1.4.299 DWDM PHY: An Ethernet PHY that transmits and receives on selected dense wavelength division multiplexing (DWDM) center frequencies for transmission over one selected DWDM channel in each direction.

1.4.300 eight-pin modular: An eight-wire connector. (From IEC 60603-7.)

1.4.301 encapsulation: In 1000BASE-X, the process by which a MAC packet is enclosed within a PCS code-group stream. (See IEEE Std 802.3, Clause 36.)

1.4.302 encircled flux: The optical power within a specified radius of a fiber center, as a percentage of that within 36 μm (for 62.5 μm fiber) or 29 μm (for 50 μm fiber).

1.4.303 End_of_Packet Delimiter (EPD): In 1000BASE-X, a defined sequence of three single code-group 8B/10B ordered sets used to delineate the ending boundary of a data transmission sequence for a single packet. (See IEEE Std 802.3, Clause 36.)

1.4.304 End-of-Stream Delimiter (ESD): Within IEEE 802.3, a code-group pattern used to terminate a normal data transmission. For 100BASE-T4, the ESD is indicated by the transmission of five predefined ternary

[32]The numbers in brackets preceded by the letter B correspond to those of the bibliography in Annex A.

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code-groups named eop1-5. For 100BASE-X, the ESD is indicated by the transmission of the code-group/T/R. For 100BASE-T2, the ESD is indicated by two consecutive pairs of predefined PAM5×5 symbols (see Table 32–15), which are generated using unique Start-of-Stream Delimiter (SSD)/ESD coding rules. For 1000BASE-T, the ESD is indicated by two consecutive vectors of four quinary symbols as specified in Table 40–1. For 100BASE-T1, the ESD consists of three code-groups as defined in 96.3.3.3.5. (See IEEE Std 802.3, Clause 22, Clause 23, Clause 32, Clause 40, and Clause 96.)

1.4.305 Endpoint PSE: Power Sourcing Equipment (PSE) that is located at an endpoint.

1.4.306 Energy-Efficient Ethernet (EEE): Provides a protocol for PHYs to coordinate transitions to or from a lower level of power consumption, without changing the link status and without dropping or corrupting frames. (See IEEE Std 802.3, Clause 78).

1.4.307 envelope: In the Multi-Channel Reconciliation Sublayer (MCRS, see IEEE Std 802.3, Clause 143), an envelope encapsulates data belonging to a specific LLID being transmitted on a specific MCRS channel, i.e., the data or idles sourced from a specific MAC instance and sent over a specific MCRS channel.

1.4.308 envelope allocation: In Nx25G-EPON, an envelope allocation represents a transmission window allocated to a single LLID (including GLID). A single GATE MPCPDU can carry up to seven envelope allocations.

1.4.309 envelope descriptor: A set of parameters consisting of LLID, StartTime, and EnvLength. An envelope descriptor defines a specific envelope pending transmission. Envelope descriptors are generated by the local MPCP sublayer and are passed to MCRS at the appropriate time to start the envelope transmission.

1.4.310 envelope frame: A MAC frame that carries a Length/Type field with the Type interpretation that may indicate additional encapsulation information within the MAC client data and has a maximum length of 2000 octets. The envelope frame is intended to allow inclusion of additional prefixes and suffixes required by higher layer encapsulation protocols. The encapsulation protocols may use up to 482 octets. (See IEEE 802.3, 3.2.7.)

1.4.311 envelope header: An MCRS-specific marker that is inserted at the beginning of every envelope (envelope start header) and in place of every frame preamble (envelope continuation header). The envelope header includes fields that identify the LLID that sourced the encapsulated data and the length of the data (in units of EQ). Envelope headers also include a CRC8 field used to detect bit errors.

1.4.312 envelope quantum: A unit of information volume. Each envelope quantum represents 64 bits of data plus the layer-specific encoding. Thus, at the MAC Control sublayer and above, an envelope quantum is equal to 64 bits. Within the MCRS, an envelope quantum contains 72 bits (i.e., 64 bits of data and 8 bits of control). Within the PCS, after the 64B/66B encoding, an envelope quantum contains 66 bits, and after 256B/257B encoding, four envelope quanta are packed into a single 257-bit block.

1.4.313 EQT: The unit of measurement of time for time-related parameters specified in IEEE Std 802.3, Clause 144 Multipoint MAC Control for Nx25G-EPON. Each EQT is equal to the time required to transmit one EQ between the MCRS and the PCS across 25GMII, and equal to 2.56 ns.

1.4.314 EtherType: A 2 octet value that indicates the nature of the MAC client protocol. Type values are assigned by the IEEE Registration Authority. (See: IEEE Std 802.3, 3.2.6.)

1.4.315 Exception Window: A time interval during which the impedance of a mated connector and associated transmission line is allowed to exceed the impedance tolerance specification for signals passed through that connector.

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1.4.316 express Media Access Control (eMAC): The instance of a Media Access Control sublayer (IEEE Std 802.3, Annex 4A) that is the client of a MAC Merge sublayer service interface that handles express traffic. (See IEEE Std 802.3, Clause 99.)

1.4.317 express traffic: Frames transmitted through an express Media Access Control (eMAC) sublayer. (See IEEE Std 802.3, Clause 99.)

1.4.318 extension bit: A bit decoded from the received carrier stream that does not map into the data space but nonetheless denotes the presence of carrier for the purposes of CSMA/CD.

1.4.319 extinction ratio: The ratio of the low optical power level to the high optical power level on an optical segment. (See IEEE Std 802.3, Clause 15.)

1.4.320 eye-opening penalty: The difference, in dB, between (a) the optical power measured at the center of the data eye, and (b) the optical power measured at a point defined by the total worst-case peak-to-peak jitter at the receiver.

1.4.321 Fast Link Pulse (FLP) Burst: A group of no more than 33 and not less than 17 10BASE-T compatible link integrity test pulses. Each FLP Burst encodes 16 bits of data using an alternating clock and data pulse sequence. (See Figure 14–15, IEEE Std 802.3, Clause 14 and Figure 28–4, IEEE Std 802.3, Clause 28.)

1.4.322 Fast Link Pulse (FLP) Burst Sequence: The sequence of FLP Bursts transmitted by the local station. This term is intended to differentiate the spacing between FLP Bursts from the individual pulse spacings within an FLP Burst. (See IEEE Std 802.3, Clause 28.)

1.4.323 fast wake: One of the two modes of operation for Energy-Efficient Ethernet (EEE). Fast wake refers to the mode for which the transmitter continues to transmit signals during Low Power Idle so that the receiver can resume operation with a shorter wake time. (See IEEE Std 802.3, Figure 78–4.)

1.4.324 FEC lane (FECL): In 50GBASE-R and 100GBASE-R, the FEC distributes encoded data to multiple logical lanes; these logical lanes are called FEC lanes. One or more FEC lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 135.)

1.4.325 fiber optic cable: A cable containing one or more optical fibers as specified in IEEE Std 802.3, 15.3.1.

1.4.326 Fiber Optic Inter-Repeater Link (FOIRL): A Fiber Optic Inter-Repeater Link segment and its two attached Medium Attachment Units (MAUs). (See IEEE Std 802.3, Clause 15.)

1.4.327 Fiber Optic Inter-Repeater Link (FOIRL) bit error ratio (BER): For 10BASE-F, the mean bit error ratio of the FOIRL. (See IEEE Std 802.3, Clause 9.)

1.4.328 Fiber Optic Inter-Repeater Link (FOIRL) collision: For 10BASE-F, the simultaneous transmission and reception of data in a Fiber Optic Medium Attachment Unit (FOMAU). (See IEEE Std 802.3, Clause 9.)

1.4.329 Fiber Optic Inter-Repeater Link (FOIRL) Compatibility Interface: For 10BASE-F, the FOMDI and Attachment Unit Interface (AUI) (optional); the two points at which hardware compatibility is defined to allow connection of independently designed and manufactured components to the baseband optical fiber cable link segment. (See IEEE Std 802.3, Clause 9.)

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1.4.330 Fiber Optic Inter-Repeater Link (FOIRL) Segment: A fiber optic link segment providing a point-to-point connection between two FOIRL Medium Attachment Units (MAUs) or between one FOIRL MAU and one 10BASE-FL MAU. *See:* **link segment**.

1.4.331 Fiber Optic Medium Attachment Unit (FOMAU): A MAU for fiber applications. (See IEEE Std 802.3, Clause 9.)

1.4.332 Fiber Optic Medium Attachment Unit's (FOMAU's) Receive Optical Fiber: For 10BASE-F, the optical fiber from which the local FOMAU receives signals. (See IEEE Std 802.3, Clause 9.)

1.4.333 Fiber Optic Medium Attachment Unit's (FOMAU's) Transmit Optical Fiber: For 10BASE-F, the optical fiber into which the local FOMAU transmits signals. (See IEEE Std 802.3, Clause 9.)

1.4.334 Fiber Optic Medium Dependent Interface (FOMDI): For 10BASE-F, the mechanical and optical interface between the optical fiber cable link segment and the Fiber Optic Medium Attachment Unit (FOMAU). (See IEEE Std 802.3, Clause 9.)

1.4.335 Fiber Optic Physical Medium Attachment (FOPMA): For 10BASE-F, the portion of the Fiber Optic Medium Attachment Unit (FOMAU) that contains the functional circuitry. (See IEEE Std 802.3 Clause 9.)

1.4.336 fiber pair: Optical fibers interconnected to provide two continuous light paths terminated at each end in an optical connector. Any intermediate optical connections have to have insertion and return loss characteristics that meet or exceed IEEE Std 802.3, 15.3.2.1 and 15.3.2.2, respectively. (See IEEE Std 802.3, 15.3.1.)

1.4.337 Fibre Channel (FC-PH): Name used to refer to ANSI INCITS 230-1994. (See IEEE Std 802.3, Clause 36.)

1.4.338 Fibre Distributed Data Interface (FDDI): A 100 Mb/s, fiber optic-based, token-ring local area network standard (ISO/IEC 9314 series of standards).

1.4.339 fixed stuff: Null or padding octets inserted to compensate for the bandwidth differences between the byte interleaving and the concatenation rules of SONET/SDH. This definition is derived from ATIS-0600416.1999(R2010) and ATIS-0900105.2008, which take precedence.

1.4.340 FLP Burst: *See:* **Fast Link Pulse (FLP) Burst.**

1.4.341 FOIRL: *See:* **Fiber Optic Inter-Repeater Link (FOIRL).**

1.4.342 FOMAU: *See:* **Fiber Optic Medium Attachment Unit (FOMAU).**

1.4.343 frame ground: *See:* **chassis ground**.

1.4.344 frame loss ratio: The number of transmitted frames not received as valid by the MAC divided by the total number of transmitted frames.

1.4.345 full duplex: A mode of operation of a network, DTE, or Medium Attachment Unit (MAU) that supports duplex transmission as defined in IEEE 100. Within the scope of this standard, this mode of operation allows for simultaneous communication between a pair of stations, provided that the Physical Layer is capable of supporting simultaneous transmission and reception without interference. (See IEEE Std 802.3.)

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1.4.346 Gigabit Media Independent Interface (GMII): The interface between the Reconciliation sublayer and the physical coding sublayer (PCS) for 1000 Mb/s operation. (See IEEE Std 802.3, Clause 35.)

1.4.347 GPON: A Gigabit-capable Passive Optical Network, as specified in ITU-T G.984.2.

NOTE—ITU-T G.984.2 [B48].

1.4.348 grant: Within P2MP protocols, a permission to transmit at a specific time, for a specific duration. Grants are issued by the OLT (master) to ONUs (slaves) by means of GATE messages. In IEEE Std 802.3, Clause 64 and Clause 77, a GATE MPCPDU contains one or multiple grants issued to a single LLID, with each grant resulting in one or multiple upstream bursts transmitted by the ONU. In Clause 144, a grant includes envelope allocations for multiple LLIDs and there is a one-to-one correspondence between the grants issued to an ONU and upstream bursts transmitted by that ONU.

1.4.349 group: A repeater port or a collection of repeater ports that can be related to the logical arrangement of ports within a repeater.

1.4.350 group delay: In 10BROAD36, the rate of change of total phase shift, with respect to frequency, through a component or system. Group delay variation is the maximum difference in delay as a function of frequency over a band of frequencies. (See IEEE Std 802.3, Clause 11.)

1.4.351 half duplex: A mode of operation of a CSMA/CD local area network (LAN) in which DTEs contend for access to a shared medium. Multiple, simultaneous transmissions in a half duplex mode CSMA/CD LAN result in interference, requiring resolution by the CSMA/CD access control protocol. (See IEEE Std 802.3.)

1.4.352 headend: In 10BROAD36, the location in a broadband system that serves as the root for the branching tree comprising the physical medium; the point to which all inbound signals converge and the point from which all outbound signals emanate. (See IEEE Std 802.3, Clause 11.)

1.4.353 header hub (HH): The highest-level hub in a hierarchy of hubs. The HH broadcasts signals transmitted to it by lower-level hubs or DTEs such that they can be received by all DTEs that may be connected to it either directly or through intermediate hubs. (See IEEE Std 802.3, 12.2.1.)

1.4.354 hub: A device used to provide connectivity between DTEs. Hubs perform the basic functions of restoring signal amplitude and timing, collision detection, and notification and signal broadcast to lower-level hubs and DTEs. (See IEEE Std 802.3, Clause 12.)

1.4.355 hybrid: A circuit (implementable with active or passive components) that enables full duplex transmission by allowing symbols to be transmitted and received on the same wire pair at the same time. It is often used together with an echo canceller to get adequate separation of transmit and receive signals.

1.4.356 idle (IDL): A signal condition where no transition occurs on the transmission line, that is used to define the end of a frame and ceases to exist after the next LO or HI transition on the Attachment Unit Interface (AUI) or Media Independent Interface (MII) circuits. An IDL always begins with a HI signal level. A driver is required to send the IDL signal for at least 2 bit times and a receiver is required to detect IDL within 1.6 bit times. (See IEEE Std 802.3, 7.3 and 12.3.2.4.4 for additional details.)

1.4.357 Idle mode: In 1000BASE-T, the period of operation in which the PHY is transmitting special code-groups that use only the values {2, 0, –2}. Idle mode occurs during startup when the PHYs at each end of a link are attempting to establish adaptive filter parameters and then synchronize both phase and timing so that normal operation can begin. Idle mode also occurs during normal operation between frames. Idle mode occurs after a control mode ends and before another Data mode begins. The Idle mode is not used between frames in a packet burst. (See IEEE Std 802.3, Clause 40.)

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1.4.358 IEEE 802.3 Power over Ethernet (IEEE 802.3 PoE): A system consisting of one PSE and one PD that provides power across balanced twisted-pair cabling. (See IEEE Std 802.3, Clause 33 and Clause 145.)

1.4.359 in-band signaling: The transmission of a signal using a frequency that is within the bandwidth of the information channel. *Contrast with:* **out-of-band signaling**. *Syn:* **in-channel signaling**. (From IEEE Std 610.7-1995 [B38].)

1.4.360 Infofield: A 16-octet frame transmitted at regular intervals containing messages for startup operation by certain PHYs. (See IEEE Std 802.3, Clause 55, Clause 113, and Clause 126.) Also a 12-octet frame transmitted at regular intervals containing messages for startup operation by certain PHYs. (See IEEE Std 802.3, Clause 97 and Clause 149.)

1.4.361 intermediate hub (IH): A hub that occupies any level below the header hub in a hierarchy of hubs. (See IEEE Std 802.3, 12.2.1 for details.)

1.4.362 interpacket gap (IPG): A delay or time gap between Ethernet packets intended to provide inter-frame recovery time for other Ethernet sublayers and for the Physical Medium. (See IEEE Std 802.3, 4.2.3.2.1 and 4.2.3.2.2.) The minimum length of IPG at the transmitting MAC is enforced by the MAC parameter interPacketGap; the actual interpacket gap may change between the transmitting MAC and receiving MAC.

1.4.363 Inter-Repeater Link (IRL): A mechanism for connecting two and only two repeater sets.

1.4.364 intersymbol interference penalty: The power penalty due to the finite bandwidth of the link. (See IEEE Std 802.3, Clause 38.)

1.4.365 jabber: A condition wherein a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition.

1.4.366 Jabber function: A mechanism for controlling abnormally long transmissions (i.e., jabber).

1.4.367 jitter: The variations of signal transitions from their ideal positions in time. Jitter may be characterized by its spectral properties and its distribution in time.

1.4.368 jumper cable assembly: An electrical or optical assembly, used for the bidirectional transmission and reception of information, consisting of a pair of transmission lines terminated at their ends with plug connectors. This assembly may or may not contain additional components, located between the plug connectors, to perform equalization. (See IEEE Std 802.3, Clause 39.)

1.4.369 Kojiri-safe: A property of the mechanical design for receptacles and mated plugs to protect sensitive functional elements, especially fiber optic ferrules and receptacles. Also called scoop-proof.

1.4.370 lane: A logical subset of the data and control information transmitted from one sublayer (e.g., PCS, PMA) to an adjacent sublayer across the inter-sublayer interface or from one PHY to another across the transmission medium (e.g. optical fiber, optical wavelength, wire pair). Lanes are transmitted in parallel and combine to deliver the full set of data and control information across the interface.

1.4.371 LDPC(1723,2048) frame: 64B/65B transmission code blocks mapped into a low density parity check (LDPC) frame with 1723 coded bits, 325 check bits and 1536 uncoded bits. (See IEEE Std 802.3, Clause 55.)

1.4.372 link: The transmission path between any two interfaces of generic cabling. (From ISO/IEC 11801.)

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1.4.373 Link codeword: The 16 bits of data encoded into a Fast Link Pulse (FLP) Burst. (See IEEE Std 802.3, Clause 28.)

1.4.374 Link Layer Discovery Protocol (LLDP): A media-independent protocol intended to run on any IEEE 802® LAN station and to allow an LLDP agent to learn the connectivity and management information from adjacent stations (see IEEE Std 802.1AB-2009).

1.4.375 link partner: The device at the opposite end of a link segment from the local station. The link partner device may be either a DTE or a repeater. (See IEEE Std 802.3, Clause 28.)

1.4.376 link penalties: For fiber optic links, the power penalties of a link not attributed to link attenuation. These power penalties include modal noise, relative intensity noise (RIN), intersymbol interference (ISI), mode partition noise, extinction ratio, and eye-opening penalties.

1.4.377 link pulse: Communication mechanism used in 10BASE-T and 100BASE-T networks to indicate link status and (in Auto-Negotiation-equipped devices) to communicate information about abilities and negotiate communication methods. 10BASE-T uses Normal Link Pulses (NLPs), which indicate link status only. 10BASE-T and 100BASE-T nodes equipped with Auto-Negotiation exchange information using a Fast Link Pulse (FLP) mechanism that is compatible with NLP. (See IEEE Std 802.3, Clause 14 and Clause 28.)

1.4.378 link section: The portion of the link between the PSE Power Interface (PI) and the PD PI.

1.4.379 link segment: The point-to-point full-duplex medium connection between two and only two Medium Dependent Interfaces (MDIs).

1.4.380 Link Segment Delay Value (LSDV): A number associated with a given segment that represents the delay on that segment used to assess path delays for 100 Mb/s CSMA/CD networks. LSDV is similar to SDV; however, LSDV values do not include the delays associated with attached end stations and/or repeaters. (See IEEE Std 802.3, 29.3.)

1.4.381 local ability: *See:* **ability**.

1.4.382 local device: The local device that may attempt to perform Auto-Negotiation with a link partner. The local device may be either a DTE or repeater. (See IEEE Std 802.3, Clause 28.)

1.4.383 Logical Link Identifier (LLID): A numeric identifier assigned to a P2MP association between an OLT and ONU established through the Point-to-Point Emulation sublayer. Each P2MP association is assigned a unique LLID. The P2MP association is bound to an ONU DTE, where the ONU MAC is to observe a private association. In Nx25G-EPON, an LLID is also a collective term that refers to a Physical Layer ID (PLID), management link ID (MLID), user link ID (ULID), and a group link ID (GLID).

1.4.384 Low Power Idle (LPI) mode: An optional mode intended to save power that may be enabled during periods of low link utilization in which either side of a link may disable portions of device or system functionality.

1.4.385 MAC frame: Consists of the Destination Address, Source Address, Length/Type field, MAC Client Data, Pad (if required), and Frame Check Sequence.

1.4.386 MAC Merge sublayer: An optional sublayer that supports interspersing express traffic with preemptable traffic by attaching an express Media Access Control (eMAC) and a preemptable Media Access Control (pMAC) to a single Physical Signaling Sublayer (PLS) service. (See IEEE Std 802.3, Clause 99.)

1.4.387 Management Information Base (MIB): A repository of information to describe the operation of a specific network device.

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1.4.388 management interface: An interface provided by both the Media Independent Interface (MII) or Gigabit Media Independent Interface (GMII) that provides access to management parameters and services.

1.4.389 master Physical Layer device (PHY): Within IEEE 802.3, in a 100BASE-T2, 1000BASE-T, 10BASE-T1L, 100BASE-T1, 1000BASE-T1, or any MultiGBASE-T link containing a pair of PHYs, the PHY that uses an external clock for generating its clock signals to determine the timing of transmitter and receiver operations. It also uses the master transmit scrambler generator polynomial for side-stream scrambling. Master and slave PHY status is determined during the Auto-Negotiation process that takes place prior to establishing the transmission link, or in the case of a PHY where Auto-Negotiation is optional and not used, master and slave PHY status is determined by management or hardware configuration. *See also:* **slave Physical Layer device (PHY).**

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

1.4.390 maximum differential input: The largest value of peak-to-peak differential (ppd) amplitude at which a receiver is expected to operate, under worst-case conditions, without exceeding the objective bit error ratio.

1.4.391 MCRS channel: In IEEE Std 802.3, Clause 143, an MCRS channel represents one of a number of defined paths along which data passes in an MCRS.

1.4.392 Media Access Control (MAC): The data link sublayer that is responsible for transferring data to and from the Physical Layer.

1.4.393 Media Independent Interface (MII): A transparent signal interface at the bottom of the Reconciliation sublayer. (See IEEE Std 802.3, Clause 22.)

1.4.394 Medium Attachment Unit (MAU): A device containing an Attachment Unit Interface (AUI), Physical Medium Attachment (PMA), and Medium Dependent Interface (MDI) that is used to connect a repeater or data terminal equipment (DTE) to a transmission medium.

1.4.395 Medium Dependent Interface (MDI): The mechanical and electrical or optical interface between the transmission medium and the MAU (e.g., 10BASE-T) or the PHY (e.g., 1000BASE-T) and also between the transmission medium and any associated (optional per IEEE Std 802.3, Clause 33, Clause 104, and Clause 145) Powered Device (PD) or Endpoint Power Sourcing Equipment (PSE).

1.4.396 Message Code (MC): The predefined 12-bit code contained in an Auto-Negotiation Message Page. (See IEEE Std 802.3, Clause 28.)

1.4.397 Message Page (MP): An Auto-Negotiation Next Page encoding that contains a predefined 12-bit Message Code. (See IEEE Std 802.3, Clause 28.)

1.4.398 midspan: An entity located within a link segment that is distinctly separate from and between the Medium Dependent Interfaces (MDIs).

1.4.399 Midspan PSE: Power Sourcing Equipment (PSE) that is located in the midspan.

1.4.400 Midspan PSE, 1000BASE-T: A Midspan PSE that results in a link that can support 10BASE-T, 100BASE-TX, and 1000BASE-T operation (see IEEE 802.3, Clause 33).

1.4.401 Midspan PSE, 10BASE-T/100BASE-TX: A Midspan PSE that results in a link that can only support 10BASE-T and 100BASE-TX operation (see IEEE 802.3, Clause 33).

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1.4.402 minimum differential sensitivity: The smallest value of peak-to-peak differential (ppd) amplitude at which a receiver is expected to operate, under worst-case conditions, without exceeding the objective bit error ratio.

1.4.403 mixing segment: A medium that may be connected to more than two Medium Dependent Interfaces (MDIs).

1.4.404 modulation error ratio (MER): The ratio of average signal constellation power to average constellation error power—that is, digital complex baseband signal-to-noise ratio—expressed in decibels.

1.4.405 Multi-Channel Reconciliation Sublayer (MCRS): The MCRS provides a mapping function that reconciles the signals at a specific Media Independent Interface (xMII) to a specific Media Access Control (MAC) Physical Signaling Sublayer (PLS) service definitions.

1.4.406 MultiGBASE-T: PHYs that belong to the set of specific BASE-T PHYs at speeds in excess of 1000 Mb/s, including 2.5GBASE-T, 5GBASE-T, 10GBASE-T, 25GBASE-T, and 40GBASE-T. [See IEEE Std 802.3, Clause 126 (for both 2.5GBASE-T and 5GBASE-T), Clause 55 (10GBASE-T) and Clause 113 (for both 25GBASE-T and 40GBASE-T).]

1.4.407 MultiGBASE-T1: PHYs that belong to the set of specific BASE-T1 PHYs at speeds in excess of 1000 Mb/s, including 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1. (See IEEE Std 802.3, Clause 149.)

1.4.408 multi-level coset code (MLCC): A forward error correcting technique consisting of splitting the information bit stream among several levels, for each one a binary component code (possibly none) is employed with an error correction capability according to the reliability of each level in data transmission over noisy channels. (See IEEE Std 802.3, Clause 115.)

1.4.409 multiport device: A device with multiple instances of MDI. (See IEEE Std 802.3, Clause 40 and Clause 42.)

1.4.410 network control host: A network management central control center that is used to configure agents, communicate with agents, and display information collected from agents.

1.4.411 network interface device (NID): A device that contains a MDI or a PI.

1.4.412 Next Page: General class of pages optionally transmitted by Auto-Negotiation able devices following the base link codeword negotiation. (See IEEE Std 802.3, Clause 28.)

1.4.413 Next Page algorithm (NPA): The algorithm that governs Next Page communication. (See IEEE Std 802.3, Clause 28.)

1.4.414 Next Page bit: A bit in the Auto-Negotiation base link codeword or Next Page encoding(s) that indicates that further link codeword transfer is required. (See IEEE Std 802.3, Clause 28.)

1.4.415 nibble: A group of four data bits. The unit of data exchange on the Media Independent Interface (MII). (See IEEE Std 802.3, Clause 22.)

1.4.416 NLP: *See:* **Normal Link Pulse (NLP).**

1.4.417 Non-Return-to-Zero, Invert on Ones (NRZI): An encoding technique used in FDDI (ISO/IEC 9314-1:1989, ISO/IEC 9314-2:1989, ISO/IEC 9314-3:1989) where a polarity transition represents a logical ONE. The absence of a polarity transition denotes a logical ZERO.

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1.4.418 Non-Return-to-Zero, Invert on Ones (NRZI)-bit: A code-bit transferred in NRZI format. The unit of data passed across the Physical Medium Dependent (PMD) service interface in 100BASE-X.

1.4.419 normalized amplitude: The amplitude of a signal when driving its steady-state value; i.e., not under the influence of ringing or other dynamic influences.

1.4.420 Normal Link Pulse (NLP): An out-of-band communications mechanism used in 10BASE-T to indicate link status. (See IEEE Std 802.3, Figure 14–13.)

1.4.421 Normal Link Pulse (NLP) Receive Link Integrity Test function: A test function associated with Auto-Negotiation that allows backward compatibility with the 10BASE-T Link Integrity Test function of IEEE Std 802.3 Figure 14–6. (See IEEE Std 802.3, Clause 28.)

1.4.422 Normal Link Pulse (NLP) sequence: A Normal Link Pulse sequence, defined in IEEE Std 802.3, 14.2.1.1 as TP_IDL.

1.4.423 nPPI: The term "nPPI" denotes either XLPPI or CPPI or both. (See IEEE Std 802.3, Annex 86A.)

1.4.424 NRZI: *See:* **Non-Return-to-Zero, Invert on Ones**.

1.4.425 Nx25G-EPON: An EPON architecture operating at a number of different downstream and upstream speeds. This term collectively refers to 25/10G-EPON, 25/25G-EPON, 50/10G-EPON, 50/25G-EPON, and 50/50G-EPON architectures. (See IEEE Std 802.3, Clause 56.)

1.4.426 OAM Discovery: Process that detects the presence and configuration of the OAM sublayer in the remote DTE.

1.4.427 OFDM channel: See orthogonal frequency division multiplexing (OFDM) channel.

1.4.428 offline: In 1000BASE-X, a DTE in its nonfunctional state. (See IEEE Std 802.3, Clause 37.)

1.4.429 Operations, Administration, and Maintenance (OAM): A group of network support functions that monitor and sustain segment operation, activities that are concerned with, but not limited to, failure detection, notification, location, and repairs that are intended to eliminate faults and keep a segment in an operational state and support activities required to provide the services of a subscriber access network to users/subscribers.

1.4.430 optical distribution network (ODN): An optical distribution plant composed of fiber optic cabling and a passive optical splitter or cascade of splitters.

1.4.431 optical fiber: A filament-shaped optical waveguide made of dielectric materials.

1.4.432 Optical Fiber Cable Interface: *See:* **Fiber Optic Medium Dependent Interface (FOMDI)**.

1.4.433 optical fiber cable link segment: A length of optical fiber cable that contains two optical fibers and is composed of one or more optical fiber cable sections and their means of interconnection, with each optical fiber terminated at each end in the optical connector plug. (See IEEE Std 802.3, 9.9.5.1 and 9.9.5.1.)

1.4.434 Optical Idle Signal: The signal transmitted by the Fiber Optic Medium Attachment Unit (FOMAU) into its transmit optical fiber during the idle state of the DO circuit. (See IEEE Std 802.3, Clause 9.)

1.4.435 optical interface: The optical input and output connection interface to a 10BASE-FP Star. (See IEEE Std 802.3, Clause 15.)

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1.4.436 Optical Line Terminal (OLT): The network-end DTE for an optical access network. The OLT is the master entity in a P2MP network with regard to the MPCP protocol.

1.4.437 Optical Modulation Amplitude (OMA): The absolute difference between the optical power of a logic one level and the optical power of a logic zero level.

1.4.438 Optical Network Unit (ONU): The subscriber-end DTE to an optical access network. An ONU is a slave entity in a P2MP network with regard to the MPCP protocol.

1.4.439 ordered set: A single special code-group, a combination of special and data code-groups, or a combination of a control character and data characters that are used to send control and status information such as remote fault and local fault status over the link. Also used by the 1000BASE-X and 10GBASE-X PCS for delineation of a packet and synchronization between the transmitter and receiver circuits at opposite ends of a link. (See IEEE Std 802.3, Clause 36, Clause 48, Clause 49, Clause 55, and Clause 82.)

1.4.440 Organizationally Unique Identifier (OUI): A 24-bit unique number that identifies a manufacturer or other organization. While an OUI may be used as a globally unique identifier on its own, its primary purpose is to be extended to form universally administered, globally unique MAC addresses or other extended globally-unique identifiers. It may also be used as part of a context dependent identifier, as part of a protocol identifier, in other management data, etc. OUI and CID (see 1.4.267) are non-overlapping and therefore mutually unique.

NOTE—See https://standards.ieee.org/develop/regauth/

1.4.441 orthogonal frequency division multiplexing (OFDM) channel: A data transmission channel in which the transmitted data is carried over a number of orthogonal subcarriers.

1.4.442 out-of-band signaling: The transmission of a signal using a frequency that is within the pass band of the transmission facility but outside a frequency range normally used for data transmission. *Contrast with:* **in-band signaling**. (From IEEE Std 610.7-1995 [B38].)

1.4.443 overfilled launch: The overfilled launch condition that excites both radial and azimuthal modes defined in Annex D of ANSI/EIA/TIA-455-204-2013.

1.4.444 P2MP Discovery: Process by which the OLT finds a newly attached and active ONU in the P2MP network, and by which the OLT and ONU exchange registration information. The OLT sends a GATE flagged for discovery.

1.4.445 P2MP Discovery window: A time period in a given wavelength band used by the OLT exclusively for the discovery process.

1.4.446 P2MP Timestamp: The timestamp used to synchronize slaves (e.g., ONUs) with the master (OLT) and for the ranging process.

1.4.447 packet: Consists of a MAC frame as defined previously, preceded by the Preamble and the Start Frame Delimiter, encoded, as appropriate, for the Physical Layer type.

1.4.448 page: In Auto-Negotiation, the encoding for a link codeword. Auto-Negotiation can support an arbitrary number of link codeword encodings. The Base Page has a constant encoding as defined in 28.2.1.2. Additional pages may have a predefined encoding *(see:* **Message Page**) or may be custom encoded *(see:* **Unformatted Page**).

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1.4.449 pairset: Either of the two valid 4-conductor connections, Alternative A or Alternative B, as listed in IEEE Std 802.3, 145.2.4. The PSE Alternative A and Alternative B connections are referred to as Mode A and Mode B, respectively, at the PD.

1.4.450 PAM5×5: Within IEEE 802.3, a block coding technique utilizing a 5×5 matrix (representing two 5-level signals) to generate pairs of quinary codes representing data nibbles and control characters. In 100BASE-T2, PAM5×5 code pairs are sent in parallel across two wire pairs. (See IEEE Std 802.3, Clause 32.)

1.4.451 parallel detection: In Auto-Negotiation, the ability to detect 100BASE-TX and 100BASE-T4 technology specific link signaling while also detecting the Normal Link Pulse (NLP) sequence or Fast Link Pulse (FLP) Burst sequence. (See IEEE Std 802.3, Clause 28.)

1.4.452 Passive-Star Coupler: A component of a 10BASE-FP fiber optic mixing segment that divides optical power received at any of N input ports among all N output ports. The division of optical power is approximately uniform. (See IEEE Std 802.3, Clause 15.)

1.4.453 patch cord: Flexible cable unit or element with connector(s) used to establish connections on a patch panel. (From ISO/IEC 11801:1995.)

1.4.454 patch panel: A cross-connect designed to accommodate the use of patch cords. It facilitates administration for moves and changes. (From ISO/IEC 11801:1995.)

1.4.455 path: The sequence of segments and repeaters providing the connectivity between two DTEs in a single collision domain. In CSMA/CD networks there is one and only one path between any two DTEs.

1.4.456 Path Delay Value (PDV): The sum of all Segment Delay Values for all segments along a given path. (See IEEE Std 802.3, Clause 13 and Clause 29.)

1.4.457 Path Variability Value (PVV): The sum of all Segment Variability Values for all the segments along a given path. (See IEEE Std 802.3, Clause 13.)

1.4.458 pause: A mechanism for full duplex flow control. (See IEEE Std 802.3, Annex 31B.)

1.4.459 pause_quantum: The unit of measurement for pause time specified; 512 MAC bit times.

NOTE—See IEEE Std 802.3, Annex 31B.

1.4.460 payload pointer: An indicator of the location of the beginning of the synchronous payload envelope. This definition is derived from ATIS-0600416.1999(R2010) and ATIS-0900105.2008, which take precedence.

1.4.461 PCS lane (PCSL): In 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R, the PCS distributes encoded data to multiple logical lanes, these logical lanes are called PCS lanes. One or more PCS lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 83, Clause 120, and Clause 135.)

1.4.462 Physical Coding Sublayer (PCS): Within IEEE 802.3, a sublayer used in certain port types to couple the Media Independent Interface (MII), Gigabit Media Independent Interface (GMII) or 10 Gigabit Media Independent Interface (XGMII) and the Physical Medium Attachment (PMA). The PCS contains the functions to encode data bits for transmission via the PMA and to decode the received conditioned signal from the PMA. There are several PCS structures. (For example, See IEEE Std 802.3, Clause 23, Clause 24, Clause 32, Clause 36, Clause 40, Clause 48, Clause 49, Clause 82, and Clause 96.)

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1.4.463 physical data block (PDB): The minimum data unit of 65 bits used to encode the GMII data stream. (See IEEE Std 802.3, Clause 115.)

1.4.464 physical header data (PHD): Side information block embedded inside a Transmit Block that is used to exchange control and for negotiation of PCS and PMA parameters between two link partners. (See IEEE Std 802.3, Clause 115.)

1.4.465 physical header subframe (PHS): Block of symbols that are the result of adding error detection and error correction parities plus modulation to PHD. (See IEEE Std 802.3, Clause 115.)

1.4.466 Physical Layer Collision Avoidance (PLCA): A method for generating transmit opportunities for 10BASE-T1S operating on mixing segments. (See IEEE Std 802.3, Clause 148.)

1.4.467 Physical Layer device (PHY): Within IEEE 802.3, the portion of the Physical Layer between the Medium Dependent Interface (MDI) and the media independent interface specific to the data rate (e.g., MII, GMII, XGMII). The PHY contains the functions that transmit, receive, and manage the encoded signals that are impressed on and recovered from the physical medium.

1.4.468 Physical Layer entity: *Syn:* **Physical Layer device.**

1.4.469 Physical Medium Attachment (PMA) sublayer: Within 802.3, that portion of the Physical Layer that contains the functions for transmission, reception, and (depending on the PHY) collision detection, clock recovery and skew alignment. (For example, See IEEE Std 802.3, Clauses 7, 12, 14, 16, 17, 18, 23, 24, 32, 36, 40, 51, 62, 63, 66, 83, and Clause 96.)

1.4.470 Physical Medium Dependent (PMD) sublayer: Within 802.3, that portion of the Physical Layer responsible for interfacing to the transmission medium. The PMD is located just above the Medium Dependent Interface (MDI). (For example, See IEEE Std 802.3, Clause 25, Clause 26, Clause 38, Clause 39, Clause 54, Clauses 58 to 60, Clause 62, Clause 63, and Clauses 84 to 89.)

1.4.471 Physical Signaling Sublayer (PLS): In 10BASE-T, that portion of the Physical Layer contained within the data terminal equipment (DTE) that provides the logical and functional coupling between the Medium Attachment Unit (MAU) and the Data Link Layer.

1.4.472 PoDL PD: A Powered Device that is intended to receive power from a link section consisting of a single twisted pair. (See IEEE Std 802.3, Clause 104.)

1.4.473 PoDL PSE: A device that provides power to a PoDL PD, connected via a link section consisting of a single twisted pair. DTE powering is intended to provide a single 100BASE-T1 or 1000BASE-T1 device with a unified interface for both the reception and transmission of data as well as the power to operate. (See IEEE Std 802.3, Clause 104.)

1.4.474 PoDL Regulated PSE: A PoDL PSE that is required to regulate the dc voltage at the PSE MDI/PI over the required range of PD load current.

1.4.475 PoDL Unregulated PSE: A PoDL PSE that is not required to regulate the voltage at the PSE MDI/PI over the required range of PD load current.

1.4.476 pointer: *See:* **payload pointer.**

1.4.477 Point-to-Multipoint network (P2MP): A network topology based on a centralized station connected to a number of end stations. Frames transit the network between the central station and the end stations and do not transit directly from end station to end station. (See IEEE Std 802.3, Clause 64, Clause 65, Clause 76, Clause 77, Clause 101, and Clause 103).

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1.4.478 Point-to-point emulation (P2PE): Emulation of private communication between two end-stations (e.g., ONU) in a P2MP. Emulation creates the equivalent of a star topology with the OLT in the nexus, and is required for compliance with IEEE 802.1Q bridging.

1.4.479 polarization dependent loss: The variation of insertion loss due to a variation of the state of polarization of an optical signal over all states of polarization within the channel frequency or wavelength range.

1.4.480 port: A segment or Inter-Repeater Link (IRL) interface of a repeater unit.

1.4.481 postamble: In 10BROAD36, the bit pattern appended after the last bit of the Frame Check Sequence by the Medium Attachment Unit (MAU). The Broadband End-of-Frame Delimiter (BEOFD). (See IEEE Std 802.3, Clause 11.)

1.4.482 power budget: The minimum optical power available to overcome the sum of attenuation plus power penalties of the optical path between the transmitter and receiver calculated as the difference between the transmitter launch power (min) and the receive power (min).

1.4.483 Powered Device (PD): A device that is either drawing power or requesting power from a PSE.

1.4.484 Power Interface (PI): The mechanical and electrical interface between the Power Sourcing Equipment (PSE) or Powered Device (PD) and the transmission medium. In an Endpoint PSE and in a PD the Power Interface is the MDI.

1.4.485 Power Sourcing Equipment (PSE): A DTE or midspan device that provides power to a single link section, which may also carry data (for 2 or 4 pair systems, see IEEE Std 802.3, Clause 33 and Clause 145; for single pair systems, see IEEE Std 802.3, Clause 104).

1.4.486 preemptable Media Access Control (pMAC): The instance of a Media Access Control sublayer (IEEE Std 802.3, Annex 4A) that is the client of a MAC Merge sublayer service interface that handles preemptable traffic. (See IEEE Std 802.3, Clause 99.)

1.4.487 preemptable traffic: Frames transmitted through a preemptable Media Access Control (pMAC) sublayer (See IEEE Std 802.3, Clause 99.)

1.4.488 prepend: To append to the beginning. For example, a Media Access Control (MAC) frame is prepended with a preamble, and appended with a frame check sequence (FCS).

1.4.489 Priority-based Flow Control (PFC): A mechanism for applying flow control to frames with a given priority on a full duplex link. (See IEEE Std 802.1Q.)

1.4.490 priority resolution: A mechanism that allows a local device and its link partner to resolve to a single mode of operation given a set of prioritized rules governing resolution. (See IEEE Std 802.3, Clause 28 and Clause 37.)

1.4.491 Priority Resolution Table: The look-up table used by Auto-Negotiation to select the network connection type where more than one common network ability exists (100BASE-TX, 100BASE-T4, 10BASE-T, etc.) The priority resolution table defines the relative hierarchy of connection types from the highest common denominator to the lowest common denominator. (See IEEE Std 802.3, Clause 28.)

1.4.492 PSE Group: A PSE or a collection of PSEs that can be related to the logical arrangement for management within an encompassing system.

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1.4.493 Q: In the context of a fiber optic communication system, one-half of the ratio of peak-to-peak signal to rms noise.

1.4.494 Q-tagged frame: A MAC frame with a specific EtherType value, and that has a maximum length of 1522 octets. (See IEEE Std 802.3, 3.2.7 and IEEE Std 802.1Q, Annex G.)

1.4.495 QTag Prefix: The first four octets of an Ethernet-encoded Tag Header. The Ethernet-encoded Tag Header is defined in IEEE Std 802.1Q.

1.4.496 quad: *See:* **star quad**.

1.4.497 quadrature amplitude modulation (QAM) symbol: The amplitude-phase representation of the bits of data that modulate a carrier signal or that modulate each of the subcarriers in OFDM.

1.4.498 quinary: Five-level.

1.4.499 quinary symbol: In 1000BASE-T, one of five numeric values corresponding to five voltage levels on a single balanced twisted pair. The values come from the set {2, 1, 0, –1, –2}. Table 40–1 lists groups of four quinary symbols. Idle is a special case where numeric values are limited to the set {2, 0, and –2}. (See IEEE Std 802.3, Clause 40.)

1.4.500 radial overfilled launch: A launch condition created when a multimode optical fiber is illuminated by the coherent optical output of a source operating in its lowest-order transverse mode in a manner that excites predominantly the radial modes of the multimode fiber.

1.4.501 ranging: A procedure by which the propagation delay between a master (e.g., OLT) and slave (e.g., ONU) is measured. The round trip delay computation is performed by the OLT, using the timestamp in MPCP messages from the ONU.

1.4.502 receiver training: Within IEEE 802.3, a startup routine in 100BASE-T2, 1000BASE-T, and 100BASE-T1 used to acquire receiver parameters and synchronize the scramblers of two connected Physical Layers (PHYs).

1.4.503 Reconciliation Sublayer (RS): A mapping function that reconciles the signals at the Media Independent Interface (MII) to the Media Access Control (MAC)-Physical Signaling Sublayer (PLS) service definitions. (See IEEE Std 802.3, Clause 22.)

1.4.504 reflectance: Ratio of reflected to incident power. This is the inverse of return loss.

1.4.505 relative intensity noise: The ratio of the variance in the optical power to the average optical power.

1.4.506 remote fault: The generic ability of a link partner to signal its status even in the event that it may not have an operational receive link. (See IEEE Std 802.3, Clause 28 and Clause 37.)

1.4.507 renegotiation: Restart of the Auto-Negotiation algorithm caused by management or user interaction. (See IEEE Std 802.3, Clause 28.)

1.4.508 repeater: Within IEEE 802.3, a device as specified in Clause 9 and Clause 27 that is used to extend the length, topology, or interconnectivity of the physical medium beyond that imposed by a single segment, up to the maximum allowable end-to-end transmission line length. Repeaters perform the basic actions of restoring signal amplitude, waveform, and timing applied to the normal data and collision signals. For wired star topologies, repeaters provide a data distribution function. In 100BASE-T, a device that allows the interconnection of 100BASE-T Physical Layer network segments using similar or dissimilar PHY

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implementations (e.g., 100BASE-X to 100BASE-X, 100BASE-X to 100BASE-T4). Repeaters are only for use in half duplex mode networks. (See IEEE Std 802.3, Clause 9 and Clause 27.)

1.4.509 repeater port: *See:* **port**.

1.4.510 repeater set: A repeater unit plus its associated Physical Layer interfaces [Medium Attachment Units (MAUs) or PHYs] and, if present, Attachment Unit (AU) or Media Independent (MI) interfaces (i.e., AUIs, MIIs).

1.4.511 repeater unit: The portion of a repeater that is inboard of its Physical Medium Attachment (PMA)/Physical Signaling Sublayer (PLS), or PMA/Physical Coding Sublayer (PCS) interfaces.

1.4.512 reserved: A key word indicating an object (bit, register, connector pin, encoding, interface signal, enumeration, etc.) to be defined only by this standard. A reserved object shall not be used for any user-defined purpose such as a user- or device-specific function; and such use of a reserved object shall render the implementation noncompliant with this standard.

1.4.513 retraining: Within IEEE 802.3, the process of re-acquiring receiver parameters and synchronizing the scramblers of two connected 100BASE-T2, 1000BASE-T, or 100BASE-T1 PHYs. *See:* **receiver training, blind mode.**

1.4.514 return loss: In 10BROAD36, the ratio in decibels of the power reflected from a port to the power incident to the port. An indicator of impedance matching in a broadband system. (See IEEE Std 802.3, Clause 11.)

1.4.515 RIN_xOMA: Relative intensity noise. Laser noise in dB/Hz with x dB optical return loss, with respect to the optical modulation amplitude.

1.4.516 rising edge: A rising edge for a differential signal pair, e.g., signal(P,N) is when, signal(P) transitions from logic low to high and signal(N) transitions from logic high to low.

1.4.517 RMS spectral width: A measure of the optical wavelength range as defined by IEC 61280-1-3.

1.4.518 router: A layer 3 interconnection device that appears as a Media Access Control (MAC) to a CSMA/CD collision domain. (See IEEE Std 610.7-1995 [B38].)

1.4.519 run length: The number of consecutive identical bits in a code-group. For example, the pattern 0011111010 has a run length of five. (See IEEE Std 802.3 Clause 36.)

1.4.520 run-length-limited code: Any transmission code that has limited run-length for its transmission. (See IEEE Std 802.3 Clause 36.)

1.4.521 running disparity: A binary parameter having a value of + or –, representing the imbalance between the number of ones and zeros in a sequence of 8B/10B code-groups. (See IEEE Std 802.3, 36.2.4.3.)

1.4.522 scrambler: A randomizing mechanism that is used to eliminate long strings of consecutive identical transmitted symbols and avoid the presence of spectral lines in the signal spectrum without changing the signaling rate. A self-synchronous scrambler is one in which the current state of the scrambler is the prior n bits of the scrambled output. Therefore, the descrambler can acquire the correct state directly from the received stream. A side-stream scrambler is one in which the current state of the scrambler is dependent only on the prior state of the scrambler and not on the transmitted data. Therefore, the descrambler has to acquire state either by searching for a state that decodes a known pattern or by agreement to start at a known state in synchronization with the scrambler. A frame-synchronous scrambler is a side-stream scrambler that begins each

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frame in a known state. This definition is derived from ATIS-0600416.1999(R2010) and ATIS-0900105.2008, which take precedence.

1.4.523 Seed: In 10BROAD36, the 23 bits residing in the scrambler shift register prior to the transmission of a packet. (See IEEE Std 802.3, Clause 11.)

1.4.524 segment: The medium connection, including connectors, between Medium Dependent Interfaces (MDIs) in a CSMA/CD local area network.

1.4.525 Segment Delay Value (SDV): A number associated with a given segment that represents the delay on that segment including repeaters and end stations, if present, used to assess path delays for 10 Mb/s CSMA/CD networks. (See IEEE Std 802.3, 13.4.)

1.4.526 Segment Variability Value (SVV): A number associated with a given segment that represents the delay variability on that segment (including a repeater) for 10 Mb/s CSMA/CD networks. The SVVs for different segment types are specified in IEEE Std 802.3, Table 13–3. (See IEEE Std 802.3, 13.4.)

1.4.527 shared service: A CSMA/CD network in which the collision domain consists of more than two DTEs so that the total network bandwidth is shared among them.

1.4.528 shielded twisted-pair (STP) cable: An electrically conducting cable, comprising one or more elements, each of which is individually shielded. There may be an overall shield, in which case the cable is referred to as shielded twisted-pair cable with an overall shield (from ISO/IEC 11801:1995). Specifically for IEEE 802.3 100BASE-TX, 150 Ω balanced inside cable with performance characteristics specified to 100 MHz (i.e., performance to Class D link standards as per ISO/IEC 11801:1995). In addition to the requirements specified in ISO/IEC 11801:1995, IEEE Std 802.3, Clause 23 and Clause 25, provide additional performance requirements for 100BASE-T operation over STP.

1.4.529 simplex fiber optic link segment: A single fiber path between two Medium Attachment Units (MAUs) or PHYs, including the terminating connectors, consisting of one or more fibers joined serially with appropriate connection devices, for example, patch cables and wall plates. (See IEEE Std 802.3, Clause 15.)

1.4.530 simplex link segment: A path between two Medium Dependent Interfaces (MDIs), including the terminating connectors, consisting of one or more segments of twisted pair cable joined serially with appropriate connection devices, for example, patch cords and wall plates. (See IEEE Std 802.3, Figure 14–2.)

1.4.531 single-port device: A device with a single instance of MDI. (See IEEE Std 802.3, Clause 40.)

1.4.532 single-signature PD: A PD that simultaneously shares the same detection signature, class signature, and maintain power signature between both pairsets. (See IEEE Std 802.3, Clause 145.)

1.4.533 single twisted-pair copper cable: Two insulated conductors twisted together in a regular fashion to form a balanced transmission line.

1.4.534 skew between pairs: The difference in arrival times of two initially coincident signals propagated over two different pairs, as measured at the receiving end of the cable. Total skew includes contributions from transmitter circuits as well as the cable.

1.4.535 slave Physical Layer device (PHY): Within IEEE 802.3, in a 100BASE-T2, 1000BASE-T, 10BASE-T1L, 100BASE-T1, 1000BASE-T1, or any MultiGBASE-T link containing a pair of PHYs, the PHY that recovers its clock from the received signal and uses it to determine the timing of transmitter operations. It also uses the slave transmit scrambler generator polynomial for side-stream scrambling. Master and slave PHY status is determined during the Auto-Negotiation process that takes place prior to establishing the transmission link, or in the case of a PHY where Auto-Negotiation is optional and not used,

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master and slave PHY status is determined by management or hardware configuration. *See also:* **master Physical Layer device (PHY).**

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

1.4.536 sliver: A pulse with a duration less than that specified for that signal (e.g., truncated clock signal).

1.4.537 special link (SL): A transmission system that replaces the normal medium. (See IEEE Std 802.3, 12.8.)

1.4.538 spectral width, full-width half maximum (FWHM): The absolute difference between the wavelengths at which the spectral radiant intensity is 50% of the maximum. (See IEEE Std 802.3, Clause 15.)

1.4.539 spectrum mask: A graphic representation of the required power distribution as a function of frequency for a modulated transmission.

1.4.540 star quad: A cable element that comprises four insulated connectors twisted together. Two diametrically facing conductors form a transmission pair.

NOTE—Cables containing star quads can be used interchangeably with cables consisting of pairs, provided the electrical characteristics meet the same specifications. (From ISO/IEC 11801.)

1.4.541 Start_of_Packet Delimiter (SPD): In 1000BASE-X, a single code-group 8B/10B ordered set used to delineate the starting boundary of a data transmission sequence for a single packet. (See IEEE Std 802.3, Clause 36.)

1.4.542 Start-of-Stream Delimiter (SSD): Within IEEE 802.3, a pattern of defined codewords used to delineate the boundary of a data transmission sequence on the Physical Layer stream. The SSD is unique in that it may be recognized independent of previously defined code-group boundaries and it defines subsequent code-group boundaries for the stream it delimits. For 100BASE-T4, SSD is a pattern of three predefined sosb code-groups (one per wire pair) indicating the positions of the first data code-group on each wire pair. For 100BASE-X, SSD consists of the code-group sequence /J/K/. For 100BASE-T2, the SSD is indicated by two consecutive pairs of predefined PAM5×5 symbols (±2, ±2) (±2, 0) which are generated using unique SSD/ESD coding rules. For 1000BASE-T, the SSD is indicated by two consecutive vectors of four quinary symbols as specified in Table 40–1. For 100BASE-T1, the SSD consists of three code-groups, as defined in 96.3.3.3.5.

1.4.543 stream: The Physical Layer encapsulation of a Media Access Control (MAC) frame. Depending on the particular PHY, the MAC frame may be modified or have information appended or prepended to it to facilitate transfer through the Physical Medium Attachment (PMA). Any conversion from a MAC frame to a PHY stream and back to a MAC frame is transparent to the MAC. (See IEEE Std 802.3, Clause 23 and Clause 24.)

1.4.544 switch: *Syn:* **bridge.**

1.4.545 symbol: Within IEEE 802.3, the smallest unit of data transmission on the medium. Symbols are unique to the coding system employed. For example, 100BASE-T4 and 100BASE-T1 use ternary symbols; 10BASE-T uses Manchester symbols; 100BASE-X uses binary symbols or code-bits; 100BASE-T2 and 1000BASE-T uses quinary symbols. For 1000BASE-X PMDs operating at 1.25 GBd, a symbol corresponds to a code-bit after the 8B/10B encoding operation i.e., has the duration of 0.8 ns. For 10GBASE-R PMDs operating at 10.3125 GBd, a symbol corresponds to a code-bit after the 64B/66B encoding operation i.e., has the duration of approximately 0.097 ns.

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1.4.546 symbol period: In 1000BASE-T, the time interval for transmission of one code-group. This is equivalent to 8 ns. In 100BASE-T1, this is equivalent to 15 ns with a code-group of 30 ns. (See IEEE Std 802.3, Clause 40 and Clause 96.)

1.4.547 symbol rate (SR): Within IEEE 802.3, the total number of symbols per second transferred to or from the Medium Dependent Interface (MDI) on a single wire pair. For 100BASE-T4, the symbol rate is 25 MBd; for 100BASE-X, the symbol rate is 125 MBd; for 100BASE-T2, the symbol rate is 25 MBd; for 1000BASE-T, the symbol rate is 125 MBd; for 100BASE-T1, the symbol rate is $66.66\overline{6}$ MBd.

1.4.548 symbol time (ST): The duration of one symbol as transferred to and from the Medium Dependent Interface (MDI) via a single wire pair. The symbol time is the reciprocal of the symbol rate.

1.4.549 Synchronous Payload Envelope (SPE): A 125 μs frame structure composed of STS Path Overhead and bandwidth for payload (payload capacity). The equivalent SDH term is Virtual Container (VC). This definition is derived from ATIS-0600416.1999(R2010) and ATIS-0900105.2008, which take precedence.

1.4.550 ternary symbol: In 10BASE-T1L, 100BASE-T4, and 100BASE-T1, a ternary data element. A ternary symbol can have one of three values: –1, 0, or +1. (See IEEE Std 802.3, Clause 23, Clause 96, and Clause 146.)

1.4.551 time_quantum: The unit of measurement for time related parameters specified in Multipoint MAC Control.

NOTE—See Clause 64, Clause 77, and Clause 103. The value of time_quantum is defined in 64.2.2.1.

1.4.552 Time Synchronization Service Interface (TSSI): Time Synchronization Service Interface (TSSI) between the generic Reconciliation Sublayer and a TimeSync client. (See IEEE Std 802.3, Clause 90.)

1.4.553 Tomlinson-Harashima precoder (THP): A precoding technique for intersymbol interference mitigation. (See IEEE Std 802.3, Clause 55 and Clause 115.)

1.4.554 transition density: The number of times the stream of bits within an 8B/10B code-group changes its value. (See IEEE Std 802.3, Clause 36.)

1.4.555 translation: In a single-cable 10BROAD36 system, the process by which incoming transmissions at one frequency are converted into another frequency for outgoing transmission. The translation takes place at the headend. (See IEEE Std 802.3, Clause 11.)

1.4.556 transmitter and dispersion penalty: A measure of the performance of a transmitter relative to an ideal transmitter. (See IEEE Std 802.3, 52.9.10 and 58.7.9.)

1.4.557 truncation loss: In a modulated data waveform, the power difference before and after implementation filtering necessary to constrain its spectrum to a specified frequency band.

1.4.558 trunk cable: The main (often large diameter) cable of a coaxial cable system. *See also:* **drop cable**.

1.4.559 twinaxial cable: A cable similar to coaxial cable in construction but containing two insulated inner conductors rather than one.

1.4.560 twinaxial cable assembly: An assembly containing multiple twinaxial cables, terminated in a connector at each end, for use as a link segment between MDIs, such as that used in 10GBASE-CX4.

1.4.561 twisted pair: A cable element that consists of two insulated conductors twisted together in a regular fashion to form a balanced transmission line. (From ISO/IEC 11801:1995.)

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1.4.562 twisted-pair cable: A bundle of multiple twisted pairs within a single protective sheath. The bundle may be unshielded or enclosed by an overall shield.

1.4.563 twisted-pair cable binder group: A group of twisted pairs within a cable that are bound together. Large telephone cables have multiple binder groups with high interbinder group near-end crosstalk loss.

1.4.564 twisted-pair link: A twisted-pair cable plus connecting hardware. (From ISO/IEC 11801:1995.) (See also IEEE Std 802.3, 14.1.2.)

1.4.565 twisted-pair link segment: In 100BASE-T, a twisted-pair link for connecting two Physical Layer devices (PHYs). (See also IEEE Std 802.3, 14.1.2.)

1.4.566 Twisted Pair Medium Dependent Interface (TP MDI): The mechanical and electrical interface between the transmission medium and the Medium Attachment Unit (MAU) or PHY, e.g., 10BASE-T, 100BASE-TX, or 1000BASE-T.

1.4.567 Type 1 PD: A PD that requests Class 0 to Class 3 during Physical Layer classification, and that is not a PoDL PD. (See IEEE Std 802.3, Clause 33.)

1.4.568 Type 1 PSE: A PSE that supports Class 0 to Class 3 power levels and provides power over 2 pairs. (See IEEE Std 802.3, Clause 33.)

1.4.569 Type 2 PD: A PD that requests Class 4 during Physical Layer classification, supports 2-Event Classification, and supports Data Link Layer classification. (See IEEE Std 802.3, Clause 33.)

1.4.570 Type 2 PSE: A PSE that supports Class 0 to Class 4 power levels and provides power over 2 pairs. (See IEEE Std 802.3, Clause 33.)

1.4.571 Type 3 PD: A single-signature PD that requests Class 1 to Class 6, or a dual-signature PD that requests Class 1 to Class 4 on both Modes, during Physical Layer classification. Additionally, the PD implements Multiple-Event classification and accepts power on both Modes simultaneously. (See IEEE Std 802.3, Clause 145.)

1.4.572 Type 3 PSE: A PSE that supports up to Class 6 power levels, supports short MPS, and may support 4-pair power. (See IEEE Std 802.3, Clause 145.)

1.4.573 Type 4 PD: A single-signature PD that requests Class 7 or Class 8, or a dual-signature PD that request Class 5 on at least one Mode, during Physical Layer classification. Additionally, the PD implements Multiple-Event classification, is capable of Data Link Layer classification, and accepts power on both Modes simultaneously. (See IEEE Std 802.3, Clause 145.)

1.4.574 Type 4 PSE: A PSE that supports at least Class 7 power levels, in addition to lower PD Classes, short MPS, and 4-pair power. (See IEEE Std 802.3, Clause 145.)

1.4.575 Type A PoDL System: A system comprising a PoDL PSE, link section, and PD that are compatible with 100BASE-T1 PHYs.

1.4.576 Type B PoDL System: A system comprising a PoDL PSE, link section, and PD that are compatible with 1000BASE-T1 PHYs.

1.4.577 Type C PoDL System: A PoDL PSE, link section, and PD that are compatible with both 100BASE-T1 and 1000BASE-T1 PHYs.

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1.4.578 Type D PoDL System: A PoDL PSE, link section, and PD that lack a data entity or are incompatible with IEEE 802.3 PHYs.

1.4.579 Type E PoDL System: A system comprising a PoDL PSE, link section, and PD that are compatible with 10BASE-T1L PHYs.

1.4.580 Type F PoDL System: A system comprising a PoDL PSE, link section, and PD that are compatible with 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1.

1.4.581 type, length, value (TLV): A short, variable length encoding of an information element consisting of sequential type, length, and value fields where the type field identifies the type of information, the length field indicates the length of the information field in octets, and the value field contains the information, itself. (See IEEE Std 802.3, 57.5.2 and 57.5.3.)

1.4.582 uncorrelated jitter: Jitter that is not associated with the sequence being transmitted. (See IEEE Std 802.3, 68.6.8.)

1.4.583 Unformatted Page (UP): A Next Page encoding that contains an unformatted 12-bit message field. Use of this field is defined through message codes and information contained in the UP. (See IEEE Std 802.3, 28.2.1.2.)

1.4.584 unit interval (UI): A period of time, usually allocated for the transmission of one symbol on one channel; the inverse of the modulation rate. Generally not the same as bit time (BT).

1.4.585 unshielded twisted-pair cable (UTP): An electrically conducting cable, comprising one or more pairs, none of which are shielded.

1.4.586 upstream: In an access network, transmission away from the subscriber end of the link. Applicable to networks where there is a clear indication in each deployment as to which end of a link is closer to a subscriber.

1.4.587 WAN Interface Sublayer (WIS): Within 10GBASE-W, a sublayer used to couple the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer. The WIS contains functions to perform SONET STS-192c/SDH VC-4-64c framing and scrambling. (See IEEE Std 802.3, Clause 50.)

1.4.588 weight of 6T code group: The algebraic sum of the logical ternary symbol values listed in the 100BASE-T4 8B6T code table. (See IEEE Std 802.3, Clause 23.)

1.4.589 worst-case modal bandwidth (WCMB): The lowest value of the modal bandwidth found when measured using either an overfilled launch (OFL) or a radial overfilled launch (ROFL).

1.4.590 zero dispersion wavelength: That wavelength where the chromatic dispersion of a fiber is zero.

1.5 Abbreviations

This standard contains the following abbreviations:

100GAUI	100 Gb/s Attachment Unit Interface
10P	label to indicate “pertains to 10PASS-TS port-type”
10P/2B	label to indicate “pertains to 10PASS-TS and 2BASE-TL port-types”
2.5GPII	2.5 Gb/s PCS Internal Interface
2.5GSEI	2.5 Gb/s Storage Enclosure Interface
200GAUI-n	200 Gb/s Attachment Unit Interface over n lanes

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200GMII	200 Gb/s Media Independent Interface
200GXS	200GMII Extender Sublayer
25GAUI	25 Gigabit Attachment Unit Interface
25GMII	25 Gigabit Media Independent Interface
2B	label to indicate “pertains to 2BASE-TL port-type”
2-PAM	two level pulse amplitude modulation
400GAUI-n	400 Gb/s Attachment Unit Interface over n lanes
400GMII	400 Gb/s Media Independent Interface
400GXS	400GMII Extender Sublayer
50GAUI	50 Gb/s Attachment Unit Interface
50GMII	50 Gb/s Media Independent Interface
5GSEI	5 Gb/s Storage Enclosure Interface
8802-3	ISO/IEC 8802-3 (IEEE Std 802.3)
8802-5	ISO/IEC 8802-5 (IEEE Std 802.5)
ACRF	attenuation to crosstalk ratio, far-end
AFEXT	alien FEXT
AIS	Alarm Indication Signal
ALSNR	alien limited signal-to-noise ratio
AN	Auto-Negotiation
ANEXT	alien NEXT
ANSI	American National Standards Institute
ASIC	application-specific integrated circuit
ASN.1	Abstract Syntax Notation One as defined in ISO/IEC 8824:1990
AUI	attachment unit interface
BCH	Bose, Ray-Chaudhuri, Hocquenghem
BER	bit error ratio
BERT	bit error ratio tester
BiDi	bidirectional
BIP	Bit Interleaved Parity
BP	backplane
BPSK	binary phase shift keying
BR	bit rate
BT	bit time
C2C	chip-to-chip
C2M	chip-to-module
CAT3	Category 3 balanced cable
CAT4	Category 4 balanced cable
CAT5	Category 5 balanced cable
CAT6	Category 6 balanced cabling
CAUI-n	100 Gb/s Attachment Unit Interface over n lanes
CCDN	coax cable distribution network
CD0	clocked data zero
CD1	clocked data one
CDR	clock and data recovery
CGMII	100 Gb/s Media Independent Interface
CID	Company ID (in Clause 50, Consecutive Identical Digit)
CJPAT	continuous jitter test pattern
CLT	coax line terminal
CMIP	common management information protocol as defined in ISO/IEC 9596-1:1991
CMIS	common management information service as defined in ISO/IEC 9595:1991
CMOS	complementary metal oxide semiconductor
CNU	coax network unit
CO	central office
COM	Channel Operating Margin

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CP	cyclic prefix
CPE	customer premises equipment
CPPI	100 Gb/s Parallel Physical Interface
CPR	coupled power ratio
CRC	cyclic redundancy check
CRPAT	continuous random test pattern
CRU	clock recovery unit
CRV	code rule violation
CS0	control signal zero
CS1	control signal one
CVH	clocked violation high
CVL	clocked violation low
CW	continuous wave
DA	destination address
DCD	duty cycle distortion
DCR	direct current resistance
DDJ	data dependent jitter
DFB	distributed feedback
DFE	decision feedback equalizer
DGD	differential group delay
DIC	deficit idle count
DJ	deterministic jitter
DLL	Data Link Layer
DME	Differential Manchester encoding
DMT	discrete multi-tone
DP-DQPSK	dual polarization differential quadrature phase shift keying
DPI	direct power injection
DQPSK	differential quadrature phase shift keying
DSL	digital subscriber line
DSQ	double square
DTE	data terminal equipment
DUT	device under test
DWDM	dense wavelength division multiplexing
ECH	envelope continuation header
EEE	Energy-Efficient Ethernet
EFM	Ethernet in the first mile
EIA	Electronic Industries Association
ELFEXT	equal-level far-end crosstalk
eMAC	express Media Access Control
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EOB	end of burst delimiter
EPD	End_of_Packet delimiter
EPoC	EPON protocol over coax
EPON	Ethernet Passive Optical Network
EQ	envelope quantum
EQT	envelope quantum time
ERDI	Enhanced Remote Defect Indication
ERL	effective return loss
ESD	end of stream delimiter
ESH	envelope start header
FAS	frame alignment signal
FC-PH	Fibre Channel—Physical and Signaling Interface
FCS	frame check sequence

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FDDI	fibre distributed data interface
FEC	forward error correction
FECL	FEC Lane
FEXT	far-end crosstalk
FIFO	first in, first out
FIR	finite impulse response
FLP	fast link pulse
FOIRL	fiber optic inter-repeater link
FOMAU	fiber optic medium attachment unit
FOMDI	fiber optic medium dependent interface
FOPMA	fiber optic physical medium attachment
FOTP	fiber optic test procedure
FSM	Finite State Machine
FSW	frame synchronization word
GLID	group link ID
GMII	Gigabit Media Independent Interface
GMP	generic mapping procedure (see ITU-T G.709)
GPON	Gigabit-capable Passive Optical Network (see ITU-T G.984.2 [B48])
gRS	generic Reconciliation Sublayer
HCB	Host Compliance Board
HFC	hybrid fiber coax
HH	header hub
IB	indicator bits
IEC	International Electrotechnical Commission
IFEC	inverse RS-FEC
IH	intermediate hub
IPG	interpacket gap
IRL	inter-repeater link
ISI penalty	intersymbol interference penalty
ISO	International Organization for Standardization
LACP	Link Aggregation Control Protocol
LACPDU	Link Aggregation Control Protocol Data Unit
LAG ID	Link Aggregation Group Identifier
LAN	local area network
LAUI	50 Gb/s Attachment Unit Interface
LCD	Loss Of Code-Group Delineation
LCL	longitudinal conversion loss Sdc11/Sdc22
LCTL	longitudinal conversion transmission loss Sdc12/Sdc21
LD	local device
LDPC	low density parity check
LED	light emitting diode
LLC	logical link control
LLDP	Link Layer Discovery Protocol (see IEEE Std 802.1AB-2009)
LLDPDU	LLDP data unit (see IEEE Std 802.1AB-2009)
LLID	logical link identifier
LOF	Loss Of Framing
LOP	Loss Of Pointer
LOS	Loss Of Signal
LP	link partner
LPI	Low Power Idle
LSB	least significant bit
LSDV	link segment delay value
LT	line termination
LVDS	Low-Voltage Differential Signals

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MAC	media access control
MACI	MA_CONTROL.indication
MACR	MA_CONTROL.request
MADI	MA_DATA.indication
MADR	MA_DATA.request
MAN	Metropolitan Area Network
MAU	medium attachment unit
MC	message code
MCB	Module Compliance Board
MCRS	Multi-Channel Reconciliation Sublayer
MDAFEXT	multiple disturber alien far-end crosstalk
MDANEXT	multiple disturber alien near-end crosstalk
MDELFEXT	multiple-disturber equal-level far-end crosstalk
MDFEXT	multiple-disturber far-end crosstalk
MDI	medium dependent interface
MDIO	management data input/output
MDNEXT	multiple-disturber near-end crosstalk
MER	modulation error ratio
MFAS	multi-frame alignment signal
MFVS	Maintain Full Voltage Signature
MIB	management information base
MII	media independent interface
MLCC	multi-level coset code
MLID	management link ID
MMD	MDIO Manageable Device
MMF	multimode fiber
MMSI	MAC Merge service interface
MP	message page
MPCP	multipoint control protocol
MPS	Maintain Power Signature
MSB	most significant bit
Mux	multiplexer
NEXT	Near-end Crosstalk
NID	network interface device
NLP	normal link pulse
NP	Next Page
NPA	Next Page algorithm
NRZI	non return to zero and invert on ones
NT	network termination
NTT	Need To Transmit
OAM	operations, administration, and maintenance
OAMPDU	operations, administration, and maintenance protocol data unit
ODN	optical distribution network
OFDM	orthogonal frequency division multiplexing
OFDMA	orthogonal frequency division multiple access
OFL	overfilled launch
OFSTP	optical fiber system test procedure
OH	overhead
OIF	Optical Internetworking Forum
OLT	optical line terminal
OMA	Optical Modulation Amplitude
ONU	optical network unit
OPU3	Optical channel Payload Unit 3
ORLT	optical return loss tolerance

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OSNR	optical signal-to-noise ratio
OTN	Optical Transport Network
OUI	Organizationally Unique Identifier
P2MP	point to multipoint
P2P	point to point
P2PE	point-to-point emulation
PAF	PME aggregation function
PAM	pulse amplitude modulation
PCB	printed circuit board
PCS	physical coding sublayer
PCSL	PCS lane
PD	Powered Device
PDB	physical data block
PDU	Protocol Data Unit
PDV	path delay value
PFC	Priority-based Flow Control
PHD	physical header data
PHS	physical header subframe
PHY	Physical Layer device
PI	Power Interface
PICS	protocol implementation conformance statement
PIPO	parallel in parallel out
PISO	parallel in serial out
pk-pk	peak-to-peak
PLCA	Physical Layer Collision Avoidance
PLID	Physical Layer ID
PLL	phase locked loop
PLM	Path Label Mismatch
PLS	physical signaling sublayer
PMA	physical medium attachment
pMAC	preemptable Media Access Control
PMD	physical medium dependent
PME	physical medium entity
PMI	physical medium independent
PMS-TC	physical media specific - transmission convergence
PoDL	Power over Data Lines
PoE	Power over Ethernet
POF	plastic optical fiber
ppd	peak-to-peak differential
PRBS	pseudo random bit sequence
PSAACRF	power sum alien attenuation to crosstalk ratio far-end
PSANEXT	power sum alien near-end crosstalk
PSD	power spectral density
PSE	Power Sourcing Equipment
PVV	path variability value
QAM	quadrature amplitude modulation
QC-LDPC	quasi-cyclic low-density parity check
RD	running disparity
REI	Remote Error Indication
RF	radio frequency
RFER	RS-FEC frame error ratio
RFI	radio frequency interference
RIN	relative intensity noise
RJ	random jitter

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RMS	root mean square
ROFL	radial overfilled launch
RS	reconciliation sublayer
RS-FEC	Reed-Solomon forward error correction
RTT	round trip time
SA	source address
SCB	single copy broadcast
SCCP	Serial Communication Classification Protocol
SC-FEC	staircase FEC
SDH	Synchronous Digital Hierarchy
SDV	segment delay value
SEF	Severely Errored Frame
SELV	Safety Extra Low Voltage
SER	symbol error ratio
SERDES	serializer and deserializer circuit
SES	Severely Errored Second
SFD	start-of-frame delimiter
SFDR	spurious free dynamic range
SHDSL	single-pair high-speed digital subscriber line
SIPO	serial in parallel out
SI-POF	step index plastic optical fiber
SLD	Start of LLID Delimiter
SMF	single-mode fiber
SMSR	side mode suppression ratio
SNR	signal-to-noise ratio
SONET	Synchronous Optical Network
SPD	Start_of_Packet delimiter
SPE	Synchronous Payload Envelope
SR	symbol rate
SSD	start-of-stream delimiter
ST	symbol time
STA	station management entity
STP	shielded twisted pair (copper)
STS	Synchronous Transport Signal
SVV	segment variability value
TBI	Ten-Bit Interface
TC	transmission convergence
TCL	transverse conversion loss Scd11/Scd22
TCM	trellis coded modulation
TCTL	transverse conversion transmission loss Scd12/Scd21
TDMA	time division multiple access
TDP	transmitter and dispersion penalty
TDR	time domain reflectometer
THP	Tomlinson-Harashima precoder
TIA	Telecommunications Industry Association
TLV	Type/Length/Value
TP-PMD	Twisted Pair, Physical Medium Dependent (ANSI INCITS 263)
TPS-TC	transport protocol specific transmission convergence sublayer
TQ	time_quantum
TSS	Test Signal Structure
TSSI	Time Synchronization Service Interface
TWDP	transmitter waveform and dispersion penalty
UCT	unconditional transition
UI	unit interval

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UJ	uncorrelated jitter
ULID	user link ID
UP	unformatted page
UPBO	upstream power backoff
UTP	unshielded twisted pair
VC	Virtual Container
VDSL	very high speed digital subscriber line
VECP	vertical eye closure penalty
VLAN	Virtual Bridged Local Area Network (see IEEE Std 802.1Q)
VTU	VDSL transceiver unit
VTU-O	VTU at the central office end
VTU-R	VTU at the remote end
WAN	Wide Area Network
WCMB	worst-case modal bandwidth
WDM	wavelength division multiplexing
WIS	WAN Interface Sublayer
WWDM	wide wavelength division multiplexing
XAUI	10 Gigabit Attachment Unit Interface
xDSL	generic term covering the family of all DSL technologies
XGMII	10 Gigabit Media Independent Interface
XGXS	XGMII Extender Sublayer
XLAUI	40 Gb/s Attachment Unit Interface
XLGMII	40 Gb/s Media Independent Interface
XLPPI	40 Gb/s Parallel Physical Interface
xMII	generic Media Independent Interface
XNP	Extended Next Page
XS	Extender Sublayer
XSBI	10 Gigabit Sixteen-Bit Interface
XTALK	crosstalk

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2. Media Access Control (MAC) service specification

2.1 Scope and field of application

This clause specifies the services provided by the Media Access Control (MAC) sublayer to the client of the MAC (see Figure 1–1). MAC clients may include the Logical Link Control (LLC) sublayer, Bridge Relay Entity, or other users of ISO/IEC LAN International Standard MAC services (see Figure 2–1). The services are described in an abstract way and do not imply any particular implementation or any exposed interface. Other clauses in this standard may add optional protocol sublayers directly above the MAC that preserve the service interface to the MAC client. Any augmentations to the MAC client interface are specified in the relevant sublayer clause (e.g., Clause 31).

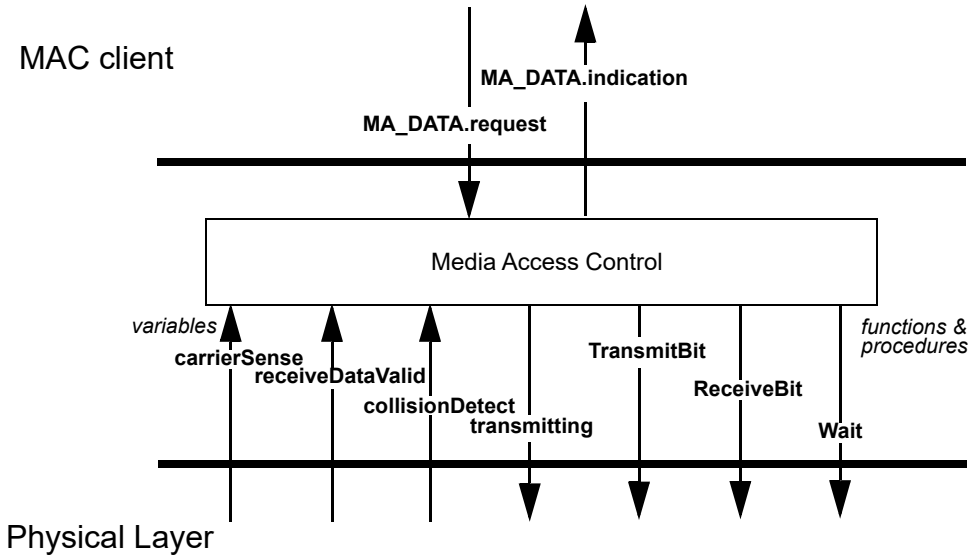

Figure 2–1—Service specification primitive relationships

2.2 Overview of the service

2.2.1 General description of services provided by the layer

The services provided by the MAC sublayer allow the local MAC client entity to exchange upper layer client data units with peer sublayer entities. Optional support may be provided for resetting the MAC sublayer entity to a known state.

2.2.2 Model used for the service specification

The model used in this service specification is identical to that used in 1.2.2.

2.2.3 Overview of interactions

MA_DATA.request
MA_DATA.indication

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2.2.4 Basic services

The MA_DATA.request and MA_DATA.indication service primitives described in this subclause are mandatory.

2.3 Detailed service specification

2.3.1 MA_DATA.request

2.3.1.1 Function

This primitive defines the transfer of data from a MAC client entity to a single peer entity or multiple peer entities in the case of group addresses.

2.3.1.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
MA_DATA.request     (
                    destination_address,
                    source_address,
                    mac_service_data_unit,
                    frame_check_sequence
                    )
```

The destination_address parameter may specify either an individual or a group MAC entity address. It has to contain sufficient information to create the DA field that is prepended to the frame by the local MAC sublayer entity and any physical information. The source_address parameter, if present, has to specify an individual MAC address. If the source_address parameter is omitted, the local MAC sublayer entity will insert a value associated with that entity. The mac_service_data_unit parameter specifies the MAC service data unit to be transmitted by the MAC sublayer entity. There is sufficient information associated with the mac_service_data_unit for the MAC sublayer entity to determine the length of the data unit. The frame_check_sequence parameter, if present, has to specify the frame check sequence field for the frame (see 3.2.9). If the frame_check_sequence parameter is omitted, the local MAC sublayer entity will compute this field and append it to the end of the frame.

2.3.1.3 When generated

This primitive is generated by the MAC client entity whenever data shall be transferred to a peer entity or entities. This can be in response to a request from higher protocol layers or from data generated internally to the MAC client, such as required by Type 2 LLC service.

2.3.1.4 Effect of receipt

The receipt of this primitive will cause the MAC entity to insert all MAC specific fields, including DA, SA, and any fields that are unique to the particular media access method, and pass the properly formed frame to the lower protocol layers for transfer to the peer MAC sublayer entity or entities.

2.3.1.5 Additional comments

If this primitive contains the frame_check_sequence parameter, the MAC client entity has to take into account this parameter's special bit-transmission order requirements, as specified in 3.3.

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The mapping between the MA_UNITDATA.request primitive specified in IEEE Std 802.1AC (for end stations) and the MA_DATA.request primitive specified here is as follows:

a) The user_priority parameter specified for MA_UNITDATA.request is not relevant for IEEE 802.3 operation and is ignored by MA_DATA.request.
b) The access_priority parameter specified for MA_UNITDATA.request is not relevant for IEEE 802.3 operation and is ignored by MA_DATA.request.
c) The frame_check_sequence parameter is not present for MA_UNITDATA.request.

The mapping between the M_UNITDATA.request primitive specified in IEEE Std 802.1AC (for MAC Bridges) and the MA_DATA.request primitive specified here is as follows:

d) The frame_type parameter specified for M_UNITDATA.request is not relevant for IEEE 802.3 operation and is ignored by MA_DATA.request.
e) The mac_action parameter specified for M_UNITDATA.request is not relevant for IEEE 802.3 operation and is ignored by MA_DATA.request.
f) The user_priority parameter specified for M_UNITDATA.request is not relevant for IEEE 802.3 operation and is ignored by MA_DATA.request.
g) The access_priority parameter specified for M_UNITDATA.request is not relevant for IEEE 802.3 operation and is ignored by MA_DATA.request.

2.3.2 MA_DATA.indication

2.3.2.1 Function

This primitive defines the transfer of data from the MAC sublayer entity (through the optional MAC Control sublayer, if implemented) to the MAC client entity or entities in the case of group addresses.

2.3.2.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
MA_DATA.indication      (
                        destination_address,
                        source_address,
                        mac_service_data_unit,
                        frame_check_sequence,
                        reception_status
                        )
```

The destination_address parameter may be either an individual or a group address as specified by the DA field of the incoming frame. The source_address parameter is an individual address as specified by the SA field of the incoming frame. The mac_service_data_unit parameter specifies the MAC service data unit as received by the local MAC entity. The frame_check_sequence parameter is the cyclic redundancy check value (see 3.2.9) as specified by the FCS field of the incoming frame. This parameter may be either omitted or (optionally) passed by the MAC sublayer entity to the MAC client. The reception_status parameter is used to pass status information to the MAC client entity.

2.3.2.3 When generated

The MA_DATA.indication is passed from the MAC sublayer entity (through the optional MAC Control sublayer, if implemented) to the MAC client entity or entities to indicate the arrival of a frame to the local MAC sublayer entity that is destined for the MAC client. Such frames are reported only if they are validly formed, received without error, and their destination address designates the local MAC entity. Frames destined

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for the optional MAC Control sublayer are not passed to the MAC client if the MAC Control sublayer is implemented.

2.3.2.4 Effect of receipt

The effect of receipt of this primitive by the MAC client is unspecified.

2.3.2.5 Additional comments

If the local MAC sublayer entity is designated by the destination_address parameter of an MA_DATA.request, the indication primitive will also be invoked by the MAC entity to the MAC client entity. This characteristic of the MAC sublayer may be due to unique functionality within the MAC sublayer or characteristics of the lower layers (for example, all frames transmitted to the broadcast address will invoke MA_DATA.indication at all stations in the network including the station that generated the request).

If this primitive contains the frame_check_sequence parameter, the MAC client entity has to take into account this parameter's special bit-transmission order requirements, as specified in 3.3.

The mapping between the MA_DATA.indication primitive specified here and the MA_UNITDATA.indication primitive specified in IEEE Std 802.1AC (for end stations) is as follows:

a) The user_priority parameter specified for MA_UNITDATA.indication is not relevant for IEEE 802.3 operation.
b) The frame_check_sequence parameter is not present for MA_UNITDATA.indication.
c) The reception_status parameter is not mapped to any parameter and is ignored by MA_UNITDATA.indication.

The mapping between the MA_DATA.indication primitive and the M_UNITDATA.indication primitive specified in IEEE Std 802.1AC (for MAC Bridges) is as follows:

a) The frame_type parameter specified for M_UNITDATA.indication is not relevant for IEEE 802.3 operation and is always assigned the value of user_data_frame.
b) The mac_action parameter specified for M_UNITDATA.indication is not relevant for IEEE 802.3 operation and is always assigned the value of request_with_no_response.
c) The user_priority parameter specified for M_UNITDATA.indication is not relevant for IEEE 802.3 operation.
d) The reception_status parameter is not mapped to any parameter and is ignored by M_UNITDATA.indication.

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3. Media Access Control (MAC) frame and packet specifications

3.1 Overview

This clause defines the mapping between MAC service interface primitives and Ethernet packets, including the syntax and semantics of the various fields of MAC frames and the fields used to form those MAC frames into packets.

During Ethernet's history, capabilities have been added to allow data link layer (layer 2) protocol encapsulations within the MAC Client Data field. As a result, there are now more than one type of MAC frame.

The frame format specified in this clause includes the following three types of MAC frames:

a) A basic frame
b) A Q-tagged frame
c) An envelope frame

All three frame types use the same Ethernet frame format.

3.1.1 Packet format

Figure 3–1 shows the fields of a packet: the Preamble, Start Frame Delimiter (SFD), the addresses of the MAC frame's destination and source, a length or type field to indicate the length or protocol type of the following field that contains the MAC client data, a field that contains padding if required, and the Frame Check Sequence (FCS) field containing a cyclic redundancy check value to detect errors in a received MAC frame. An Extension field is added, if required (for 1000 Mb/s half duplex operation only). Of these fields, all are of fixed size except for the MAC Client Data, Pad and Extension fields, which may contain an integer number of octets between the minimum and maximum values that are determined by the specific implementation of the MAC. See 4.4 for particular MAC parameters.

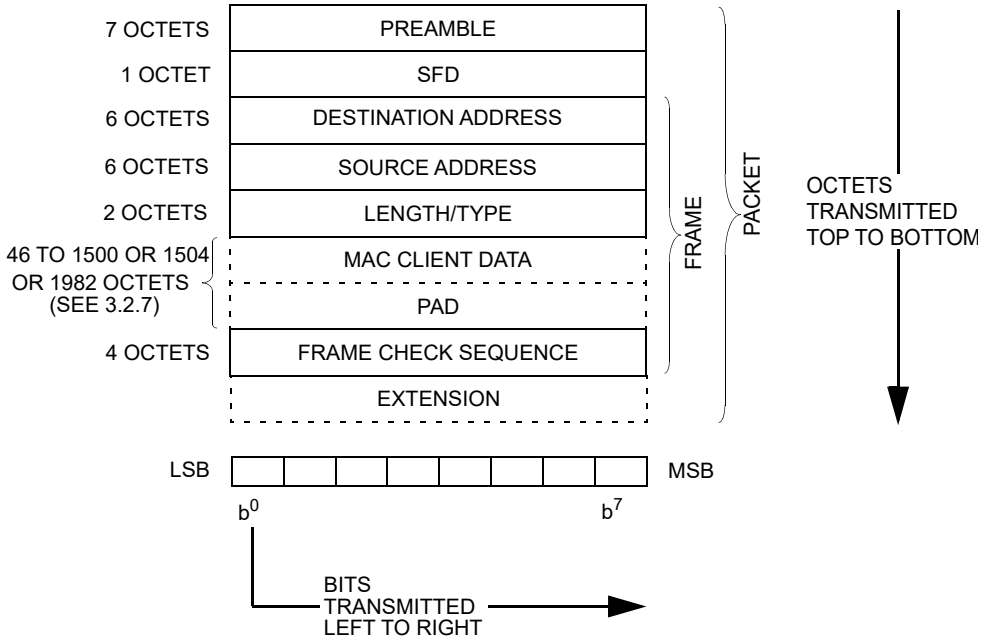

Figure 3–1—Packet format

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The minimum and maximum MAC frame size limits in 4.4 refer to that portion of the packet from the Destination Address field through the Frame Check Sequence field, inclusive (i.e., the MAC frame).

Relative to Figure 3–1, the octets of a packet are transmitted from top to bottom, and the bits of each octet are transmitted from left to right.

3.1.2 Service interface mappings

Figure 3–2 shows the mapping of service interface parameters to the fields of a MAC frame within a packet. The MAC client may or may not supply Pad and FCS. For this reason the mappings for Pad and FCS are shown with dashed lines.

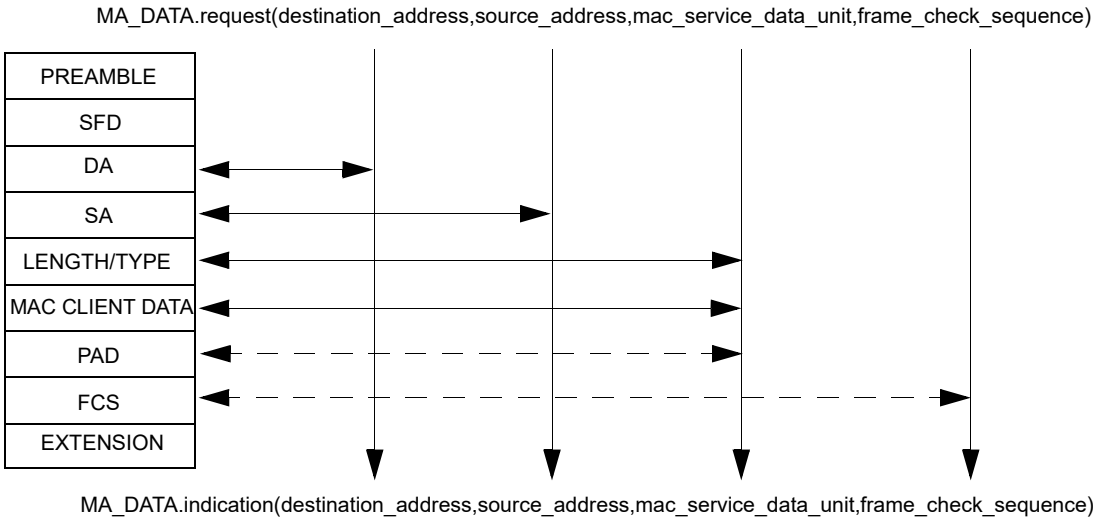

Figure 3–2—Service primitive mappings

3.2 Elements of the MAC frame and packet

A MAC frame is encapsulated in a packet by the MAC. This subclause describes in detail the fields of the MAC frame and the additional fields that the MAC creates to encapsulate the MAC frame. These fields are described in order of transmission.

3.2.1 Preamble field

The Preamble field is a 7-octet field that is used to allow the PLS circuitry to reach its steady-state synchronization with the received packet's timing (see 4.2.5).

3.2.2 Start Frame Delimiter (SFD) field

The SFD field is the sequence 10101011. It immediately follows the preamble pattern. A MAC frame starts immediately after the SFD.

3.2.3 Address fields

Each MAC frame shall contain two address fields: the Destination Address field and the Source Address field, in that order. The Destination Address field shall specify the destination addressee(s) for which the MAC frame is intended. The Source Address field shall identify the station from which the MAC frame was initiated. The representation of each address field shall be as follows (see Figure 3–3):

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a) Each address field shall be 48 bits in length.
b) The first bit (LSB) shall be used in the Destination Address field as an address type designation bit to identify the Destination Address either as an individual or as a group address. If this bit is 0, it shall indicate that the address field contains an individual address. If this bit is 1, it shall indicate that the address field contains a group address that identifies none, one or more, or all of the stations connected to the LAN. In the Source Address field, the first bit is reserved and set to 0.
c) The second bit shall be used to distinguish between locally or globally administered addresses. For globally administered (or U, universal) addresses, the bit is set to 0. If an address is to be assigned locally, this bit shall be set to 1. Note that for the broadcast address, this bit is also a 1.
d) Each octet of each address field shall be transmitted least significant bit first.



I/G = 0 INDIVIDUAL ADDRESS
I/G = 1 GROUP ADDRESS
U/L = 0 GLOBALLY ADMINISTERED ADDRESS
U/L = 1 LOCALLY ADMINISTERED ADDRESS

Figure 3–3—Address field format

3.2.3.1 Address designation

A MAC sublayer address is one of two types:

a) *Individual Address*. The address associated with a particular station on the network.
b) *Group Address*. A multidestination address, associated with one or more stations on a given network. There are two kinds of multicast addresses:
   1) *Multicast-Group Address*. An address associated by higher-level convention with a group of logically related stations.
   2) *Broadcast Address*. A distinguished, predefined multicast address that always denotes the set of all stations on a given LAN.

All 1's in the Destination Address field shall be predefined to be the Broadcast Address. This group shall be predefined for each communication medium to consist of all stations actively connected to that medium; it shall be used to broadcast to all the active stations on that medium. All stations shall be able to recognize the Broadcast Address. It is not necessary that a station be capable of generating the Broadcast Address.

The address space shall also be partitioned into locally administered and globally administered addresses. The nature of a body and the procedures by which it administers these global (U) addresses is beyond the scope of this standard.[33]

3.2.4 Destination Address field

The Destination Address field specifies the station(s) for which the MAC frame is intended. It may be an individual or multicast (including broadcast) address.

[33]For information on how to use MAC addresses, see IEEE Std 802, Overview and Architecture. To apply for an Organizationally Unique Identifier for building a MAC address, contact the Registration Authority, IEEE Standards Department, 445 Hoes Lane, Piscataway, NJ 08854, USA; +1 732 562 3813; fax +1 732 562 1571. URL: https://standards.ieee.org/develop/regauth/.

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3.2.5 Source Address field

The Source Address field specifies the station sending the MAC frame. The Source Address field is not interpreted by the MAC sublayer.

3.2.6 Length/Type field

This two-octet field takes one of two meanings, depending on its numeric value. For numerical evaluation, the first octet is the most significant octet of this field.

a) If the value of this field is less than or equal to 1500 decimal (05DC hexadecimal), then the Length/Type field indicates the number of MAC client data octets contained in the subsequent MAC Client Data field of the basic frame (Length interpretation).
b) If the value of this field is greater than or equal to 1536 decimal (0600 hexadecimal), then the Length/Type field indicates the EtherType of the MAC client protocol (Type interpretation).[34]
The Length and Type interpretations of this field are mutually exclusive.

When used as a Type field, it is the responsibility of the MAC client to ensure that the MAC client operates properly when the MAC sublayer pads the supplied MAC Client data, as discussed in 3.2.7.

Regardless of the interpretation of the Length/Type field, if the length of the MAC Client Data field is less than the minimum required for proper operation of the protocol, a Pad field (a sequence of octets) will be added after the MAC Client Data field but prior to the FCS field, specified below. The procedure that determines the size of the Pad field is specified in 4.2.8. The Length/Type field is transmitted and received with the high order octet first.

NOTE—Clause 2 of IEEE Std 802 defines a set of EtherType values and associated mechanisms for use in prototype and vendor-specific protocol development.

3.2.7 MAC Client Data field

The MAC Client Data field contains a sequence of octets. Full data transparency is provided in the sense that any arbitrary sequence of octet values may appear in the MAC Client Data field up to a maximum field length determined by the particular implementation.

Ethernet implementations shall support at least one of three maximum MAC Client Data field sizes defined as follows:

a) 1500 decimal—basic frames (see 1.4.207)
b) 1504 decimal—Q-tagged frames (see 1.4.494)
c) 1982 decimal—envelope frames (see 1.4.310)

If layer management is implemented, frames with a MAC Client Data field larger than the supported maximum MAC Client Data field size are counted. It is recommended that new implementations support the transmission and reception of envelope frames, item c) above.

NOTE 1—The envelope frame is intended to allow inclusion of additional prefixes and suffixes required by higher layer encapsulation protocols (see 1.4.302) such as those defined by the IEEE 802.1 working group (such as Provider Bridges and MAC Security), ITU-T or IETF (such as MPLS). The original MAC Client Data field maximum remains 1500 octets while the encapsulation protocols may add up to an additional 482 octets. Use of these extra octets for other purposes is not recommended, and may result in MAC frames being dropped or corrupted as they may violate maximum MAC frame size restrictions if encapsulation protocols are required to operate on them.

[34]EtherType assignments are administered by the Registration Authority, IEEE Standards Department, 445 Hoes Lane, Piscataway, NJ 08554, USA; +1 732 562 3813; fax +1 732 562 1571. URL: https://standards.ieee.org/develop/regauth/.

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NOTE 2—All IEEE 802.3 MAC frames share a common format. The processing of the three types of MAC frames is not differentiated within the IEEE 802.3 MAC, except for management. However, they may be distinguished within the MAC client.

NOTE 3—All Q-tagged frames are envelope frames, but not all envelope frames are Q-tagged frames.

See 4.4 for a discussion of MAC parameters; see 4.2.3.3 for a discussion of the minimum frame size and minFrameSize.

3.2.8 Pad field

A minimum MAC frame size is required for correct CSMA/CD protocol operation (see 4.2.3.3 and 4.4). If necessary, a Pad field (in units of octets) is appended after the MAC Client Data field prior to calculating and appending the FCS field. The size of the Pad, if any, is determined by the size of the MAC Client Data field supplied by the MAC client and the minimum MAC frame size and address size MAC parameters (see 4.4).

The length of the Pad field required for MAC Client Data that is clientDatasize/8 octets long is max [0, minFrameSize – (clientDatasize + 2 × addressSize + 48)] bits.

3.2.9 Frame Check Sequence (FCS) field

A cyclic redundancy check (CRC) is used by the transmit and receive algorithms to generate a CRC value for the FCS field. The FCS field contains a 4-octet (32-bit) CRC value. This value is computed as a function of the contents of the protected fields of the MAC frame: the Destination Address, Source Address, Length/Type field, MAC Client Data, and Pad (that is, all fields except FCS). The encoding is defined by the following generating polynomial.

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

Mathematically, the CRC value corresponding to a given MAC frame is defined by the following procedure:

a) The first 32 bits of the frame are complemented.
b) The n bits of the protected fields are then considered to be the coefficients of a polynomial $M(x)$ of degree $n – 1$. (The first bit of the Destination Address field corresponds to the $x^{(n-1)}$ term and the last bit of the MAC Client Data field (or Pad field if present) corresponds to the x^0 term.)
c) $M(x)$ is multiplied by x^{32} and divided by $G(x)$, producing a remainder $R(x)$ of degree ≤ 31.
d) The coefficients of $R(x)$ are considered to be a 32-bit sequence.
e) The bit sequence is complemented and the result is the CRC.

The 32 bits of the CRC value are placed in the FCS field so that the x^{31} term is the left-most bit of the first octet, and the x^0 term is the right most bit of the last octet. (The bits of the CRC are thus transmitted in the order $x^{31}, x^{30},\ldots, x^1, x^0$.) See Hammond, et al. [B30].

3.2.10 Extension field

The Extension field follows the FCS field, and is made up of a sequence of extension bits, which are readily distinguished from data bits. The length of the field is in the range of zero to (slotTime–minFrameSize) bits, inclusive. The contents of the Extension field are not included in the FCS computation.

The Extension field may have a length of greater than zero under the conditions that are described in 4.2.3.4. The length of the Extension field will be zero under all other conditions. Implementations defined in 4.4.2 may ignore this field altogether if the number of bit times in the slotTime parameter is equal to the number of bits in the minFrameSize parameter.

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3.3 Order of bit transmission

Each octet of the MAC frame, with the exception of the FCS, is transmitted least significant bit first.

3.4 Invalid MAC frame

An invalid MAC frame shall be defined as one that meets at least one of the following conditions:

a) The frame length is inconsistent with a length value specified in the length/type field. If the length/type field contains a type value as defined by 3.2.6, then the frame length is assumed to be consistent with this field and should not be considered an invalid frame on this basis.
b) It is not an integral number of octets in length.
c) The bits of the incoming frame (exclusive of the FCS field itself) do not generate a CRC value identical to the one received.

The contents of invalid MAC frames shall not be passed to the LLC or MAC Control sublayers. Invalid MAC frames may be ignored, discarded, or used in a private manner. The use of such frames by clients other than LLC or MAC control is beyond the scope of this standard. The occurrence of invalid MAC frames may be communicated to network management.

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4. Media Access Control

4.1 Functional model of the MAC method

4.1.1 Overview

The architectural model described in Clause 1 is used in this clause to provide a functional description of the LAN CSMA/CD MAC sublayer.

The MAC sublayer defines a medium-independent facility, built on the medium-dependent physical facility provided by the Physical Layer, and under the access-layer-independent LAN LLC sublayer (or other MAC client). It is applicable to a general class of local area broadcast media suitable for use with the media access discipline known as Carrier Sense Multiple Access with Collision Detection (CSMA/CD).

The LLC sublayer and the MAC sublayer together are intended to have the same function as that described in the OSI model for the Data Link Layer alone. In a broadcast network, the notion of a data link between two network entities does not correspond directly to a distinct physical connection. Nevertheless, the partitioning of functions presented in this standard requires two main functions generally associated with a data link control procedure to be performed in the MAC sublayer. They are as follows:

a) Data encapsulation (transmit and receive)
    1) Framing (frame boundary delimitation, frame synchronization)
    2) Addressing (handling of source and destination addresses)
    3) Error detection (detection of physical medium transmission errors)
b) Media Access Management
    1) Medium allocation (collision avoidance)
    2) Contention resolution (collision handling)

An optional MAC control sublayer, architecturally positioned between LLC (or other MAC client) and the MAC, is specified in Clause 31. This MAC Control sublayer is transparent to both the underlying MAC and its client (typically LLC). The MAC sublayer operates independently of its client; i.e., it is unaware whether the client is LLC or the MAC Control sublayer. This allows the MAC to be specified and implemented in one manner, whether or not the MAC Control sublayer is implemented. References to LLC as the MAC client in text and figures apply equally to the MAC Control sublayer, if implemented.

This standard provides for two modes of operation of the MAC sublayer:

a) In *half duplex* mode, stations contend for the use of the physical medium, using the CSMA/CD algorithms specified. Bidirectional communication is accomplished by rapid exchange of frames, rather than full duplex operation. Half duplex operation is possible on all supported media; it is required on those media that are incapable of supporting simultaneous transmission and reception without interference, for example, 10BASE2 and 100BASE-T4.
b) The *full duplex* mode of operation can be used when all of the following are true:
    1) The physical medium is capable of supporting simultaneous transmission and reception without interference (e.g., 10BASE-T, 10BASE-FL, and 100BASE-TX/FX).
    2) There are exactly two stations on the LAN. This allows the physical medium to be treated as a full duplex point-to-point link between the stations. Since there is no contention for use of a shared medium, the multiple access (i.e., CSMA/CD) algorithms are unnecessary.
    3) Both stations on the LAN are capable of and have been configured to use full duplex operation.

The most common configuration envisioned for full duplex operation consists of a central bridge (also known as a switch) with a dedicated LAN connecting each bridge port to a single device.

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The formal specification of the MAC in 4.2 comprises both the half duplex and full duplex modes of operation. The remainder of this clause provides a functional model of the CSMA/CD MAC method.

4.1.2 CSMA/CD operation

This subclause provides an overview of frame transmission and reception in terms of the functional model of the architecture. This overview is descriptive, rather than definitional; the formal specifications of the operations described here are given in 4.2 and 4.3. Specific implementations for CSMA/CD mechanisms that meet this standard are given in 4.4. Figure 1–1 provides the architectural model described functionally in the subclauses that follow.

The Physical Layer Signaling (PLS) component of the Physical Layer provides an interface to the MAC sublayer for the serial transmission of bits onto the physical media. For completeness, in the operational description that follows some of these functions are included as descriptive material. The concise specification of these functions is given in 4.2 for the MAC functions and in Clause 7 for PLS.

Transmit frame operations are independent from the receive frame operations. A transmitted frame addressed to the originating station will be received and passed to the MAC client at that station. This characteristic of the MAC sublayer may be implemented by functionality within the MAC sublayer or full duplex characteristics of portions of the lower layers.

4.1.2.1 Normal operation

4.1.2.1.1 Transmission without contention

When a MAC client requests the transmission of a frame, the Transmit Data Encapsulation component of the CSMA/CD MAC sublayer constructs the frame from the client-supplied data. It prepends a preamble and a Start Frame Delimiter to the beginning of the frame. Using information provided by the client, the CSMA/CD MAC sublayer also appends a Pad at the end of the MAC information field of sufficient length to ensure that the transmitted frame length satisfies a minimum frame-size requirement (see 4.2.3.3). It also prepends destination and source addresses, the length/type field, and appends a frame check sequence to provide for error detection. If the MAC supports the use of client-supplied frame check sequence values, then it shall use the client-supplied value, when present. If the use of client-supplied frame check sequence values is not supported, or if the client-supplied frame check sequence value is not present, then the MAC shall compute this value. The frame is then handed to the Transmit Media Access Management component in the MAC sublayer for transmission.

In half duplex mode, Transmit Media Access Management attempts to avoid contention with other traffic on the medium by monitoring the carrier sense signal provided by the Physical Layer Signaling (PLS) component and deferring to passing traffic. When the medium is clear, frame transmission is initiated (after a brief interframe delay to provide recovery time for other CSMA/CD MAC sublayers and for the physical medium). The MAC sublayer then provides a serial stream of bits to the Physical Layer for transmission.

In half duplex mode, at an operating speed of 1000 Mb/s, the minimum frame size is insufficient to ensure the proper operation of the CSMA/CD protocol for the desired network topologies. To circumvent this problem, the MAC sublayer will append a sequence of extension bits to frames which are less than slotTime bits in length so that the duration of the resulting transmission is sufficient to ensure proper operation of the CSMA/CD protocol.

In half duplex mode, at an operating speed of 1000 Mb/s, the CSMA/CD MAC may optionally transmit additional frames without relinquishing control of the transmission medium, up to a specified limit.

In full duplex mode, there is no need for Transmit Media Access Management to avoid contention with other traffic on the medium. Frame transmission may be initiated after the interframe delay, regardless of the

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presence of receive activity. In full duplex mode, the MAC sublayer does not perform either carrier extension or frame bursting.

The Physical Layer performs the task of generating the signals on the medium that represent the bits of the frame. Simultaneously, it monitors the medium and generates the collision detect signal, which in the contention-free case under discussion, remains off for the duration of the frame. A functional description of the Physical Layer is given in Clause 7 and beyond.

When transmission has completed without contention, the CSMA/CD MAC sublayer so informs the MAC client and awaits the next request for frame transmission.

4.1.2.1.2 Reception without contention

At each receiving station, the arrival of a frame is first detected by the Physical Layer, which responds by synchronizing with the incoming preamble, and by turning on the receiveDataValid signal. As the encoded bits arrive from the medium, they are decoded and translated back into binary data. The Physical Layer passes subsequent bits up to the MAC sublayer, where the leading bits are discarded, up to and including the end of the preamble and Start Frame Delimiter.

Meanwhile, the Receive Media Access Management component of the MAC sublayer, having observed receiveDataValid, has been waiting for the incoming bits to be delivered. Receive Media Access Management collects bits from the Physical Layer entity as long as the receiveDataValid signal remains on. When the receiveDataValid signal is removed, the frame is truncated to an octet boundary, if necessary, and passed to Receive Data Decapsulation for processing.

Receive Data Decapsulation checks the frame's Destination Address field to decide whether the frame should be received by this station. If so, it passes the Destination Address (DA), the Source Address (SA), the Length/Type, the Data and (optionally) the Frame Check Sequence (FCS) fields to the MAC client, along with an appropriate status code, as defined in 4.3.2. It also checks for invalid MAC frames by inspecting the frame check sequence to detect any damage to the frame enroute, and by checking for proper octet-boundary alignment of the end of the frame. Frames with a valid FCS may also be checked for proper octet-boundary alignment.

In half duplex mode, at an operating speed of 1000 Mb/s, frames may be extended by the transmitting station under the conditions described in 4.2.3.4. The extension is discarded by the MAC sublayer of the receiving station, as defined in the procedural model in 4.2.9.

4.1.2.2 Access interference and recovery

In half duplex mode, if multiple stations attempt to transmit at the same time, it is possible for them to interfere with each other's transmissions, in spite of their attempts to avoid this by deferring. When transmissions from two stations overlap, the resulting contention is called a collision. Collisions occur only in half duplex mode, where a collision indicates that there is more than one station attempting to use the shared physical medium. In full duplex mode, two stations may transmit to each other simultaneously without causing interference. The Physical Layer may generate a collision indication, but this is ignored by the full duplex MAC.

A given station can experience a collision during the initial part of its transmission (the collision window) before its transmitted signal has had time to propagate to all stations on the CSMA/CD medium. Once the collision window has passed, a transmitting station is said to have acquired the medium; subsequent collisions are avoided since all other (properly functioning) stations can be assumed to have noticed the signal and to be deferring to it. The time to acquire the medium is thus based on the round-trip propagation time of the Physical Layer whose elements include the PLS, PMA, and physical medium.

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In the event of a collision, the transmitting station's Physical Layer initially notices the interference on the medium and then turns on the collision detect signal. In half duplex mode, this is noticed in turn by the Transmit Media Access Management component of the MAC sublayer, and collision handling begins. First, Transmit Media Access Management enforces the collision by transmitting a bit sequence called jam. In 4.4, implementations that use this enforcement procedure are provided. This ensures that the duration of the collision is sufficient to be noticed by the other transmitting station(s) involved in the collision. After the jam is sent, Transmit Media Access Management terminates the transmission and schedules another transmission attempt after a randomly selected time interval. Retransmission is attempted again in the face of repeated collisions. Since repeated collisions indicate a busy medium, however, Transmit Media Access Management attempts to adjust to the medium load by backing off (voluntarily delaying its own retransmissions to reduce its load on the medium). This is accomplished by expanding the interval from which the random retransmission time is selected on each successive transmit attempt. Eventually, either the transmission succeeds, or the attempt is abandoned on the assumption that the medium has failed or has become overloaded.

In full duplex mode, a station ignores any collision detect signal generated by the Physical Layer. Transmit Media Access Management in a full duplex station will always be able to transmit its frames without contention, so there is never any need to jam or reschedule transmissions.

At the receiving end, the bits resulting from a collision are received and decoded by the PLS just as are the bits of a valid frame. Fragmentary frames received during collisions are distinguished from valid transmissions by the MAC sublayer's Receive Media Access Management component.

4.1.3 Relationships to the MAC client and Physical Layers

The CSMA/CD MAC sublayer provides services to the MAC client required for the transmission and reception of frames. Access to these services is specified in 4.3. The CSMA/CD MAC sublayer makes a best effort to acquire the medium and transfer a serial stream of bits to the Physical Layer. Although certain errors are reported to the client, error recovery is not provided by MAC. Error recovery may be provided by the MAC client or higher (sub)layers.

4.2 CSMA/CD Media Access Control (MAC) method: Precise specification

4.2.1 Introduction

A precise algorithmic definition is given in this subclause, providing procedural model for the CSMA/CD MAC process with a program in the computer language Pascal. See references [B9] and [B17] for resource material. Note whenever there is any apparent ambiguity concerning the definition of some aspect of the CSMA/CD MAC method, it is the Pascal procedural specification in 4.2.7 through 4.2.10 that should be consulted for the definitive statement. Subclauses 4.2.2 through 4.2.6 provide, in prose, a description of the access mechanism with the formal terminology to be used in the remaining subclauses.

4.2.2 Overview of the procedural model

The functions of the CSMA/CD MAC method are presented below, modeled as a program written in the computer language Pascal. This procedural model is intended as the primary specification of the functions to be provided in any CSMA/CD MAC sublayer implementation. It is important to distinguish, however, between the model and a real implementation. The model is optimized for simplicity and clarity of presentation, while any realistic implementation shall place heavier emphasis on such constraints as efficiency and suitability to a particular implementation technology or computer architecture. In this context, several important properties of the procedural model shall be considered.

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4.2.2.1 Ground rules for the procedural model

The ground rules for the procedural model are as follows:

a) First, it shall be emphasized that *the description of the MAC sublayer in a computer language is in no way intended to imply that procedures shall be implemented as a program executed by a computer.* The implementation may consist of any appropriate technology including hardware, firmware, software, or any combination.
b) Similarly, it shall be emphasized that it is the behavior of any MAC sublayer implementations that shall match the standard, not their internal structure. The internal details of the procedural model are useful only to the extent that they help specify that behavior clearly and precisely.
c) The handling of incoming and outgoing frames is rather stylized in the procedural model, in the sense that frames are handled as single entities by most of the MAC sublayer and are only serialized for presentation to the Physical Layer. In reality, many implementations will instead handle frames serially on a bit, octet or word basis. This approach has not been reflected in the procedural model, since this only complicates the description of the functions without changing them in any way.
d) The model consists of algorithms designed to be executed by a number of concurrent processes; these algorithms collectively implement the CSMA/CD procedure. The timing dependencies introduced by the need for concurrent activity are resolved in two ways:
    1) *Processes Versus External Events.* It is assumed that the algorithms are executed "very fast" relative to external events, in the sense that a process never falls behind in its work and fails to respond to an external event in a timely manner. For example, when a frame is to be received, it is assumed that the Media Access procedure ReceiveFrame is always called well before the frame in question has started to arrive.
    2) *Processes Versus Processes.* Among processes, no assumptions are made about relative speeds of execution. This means that each interaction between two processes shall be structured to work correctly independent of their respective speeds. Note, however, that the timing of interactions among processes is often, in part, an indirect reflection of the timing of external events, in which case appropriate timing assumptions may still be made.

It is intended that the concurrency in the model reflect the parallelism intrinsic to the task of implementing the MAC client and MAC procedures, although the actual parallel structure of the implementations is likely to vary.

4.2.2.2 Use of Pascal in the procedural model

Several observations need to be made regarding the method with which Pascal is used for the model. Some of these observations are as follows:

a) The following limitations of the language have been circumvented to simplify the specification:
    1) The elements of the program (variables and procedures, for example) are presented in logical groupings, in top-down order. Certain Pascal ordering restrictions have thus been circumvented to improve readability.
    2) The *process* and *cycle* constructs of Concurrent Pascal, a Pascal derivative, have been introduced to indicate the sites of autonomous concurrent activity. As used here, a process is simply a parameterless procedure that begins execution at "the beginning of time" rather than being invoked by a procedure call. A cycle statement represents the main body of a process and is executed repeatedly forever.
    3) The lack of variable array bounds in the language has been circumvented by treating frames as if they are always of a single fixed size (which is never actually specified). The size of a frame depends on the size of its data field, hence the value of the "pseudo-constant" frameSize should be thought of as varying in the long term, even though it is fixed for any given frame.
    4) The use of a variant record to represent a frame (as fields and as bits) follows the spirit but not the letter of the Pascal Report, since it allows the underlying representation to be viewed as two different data types.

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b) The model makes no use of any explicit interprocess synchronization primitives. Instead, all interprocess interaction is done by way of carefully stylized manipulation of shared variables. For example, some variables are set by only one process and inspected by another process in such a manner that the net result is independent of their execution speeds. While such techniques are not generally suitable for the construction of large concurrent programs, they simplify the model and more nearly resemble the methods appropriate to the most likely implementation technologies (microcode, hardware state machines, etc.)

4.2.2.3 Organization of the procedural model

The procedural model used here is based on seven cooperating concurrent processes. The Frame Transmitter process and the Frame Receiver process are provided by the clients of the MAC sublayer (which may include the LLC sublayer) and make use of the interface operations provided by the MAC sublayer. The other five processes are defined to reside in the MAC sublayer. The seven processes are as follows:

a) Frame Transmitter process
b) Frame Receiver process
c) Bit Transmitter process
d) Bit Receiver process
e) Deference process
f) BurstTimer process
g) SetExtending process

This organization of the model is illustrated in Figure 4–1 and reflects the fact that the communication of entire frames is initiated by the client of the MAC sublayer, while the timing of collision backoff and of individual bit transfers is based on interactions between the MAC sublayer and the Physical-Layer-dependent bit time.

Figure 4–1 depicts the static structure of the procedural model, showing how the various processes and procedures interact by invoking each other. Figure 4–2a, 4–2b, 4–3a, and 4–3b summarize the dynamic behavior of the model during transmission and reception, focusing on the steps that shall be performed, rather than the procedural structure that performs them. The usage of the shared state variables is not depicted in the figures, but is described in the comments and prose in the following subclauses.

4.2.2.4 Layer management extensions to procedural model

In order to incorporate network management functions, this Procedural Model has been expanded. Network management functions have been incorporated in two ways. First, 4.2.7–4.2.10, 4.3.2, Figure 4–2a, and Figure 4–2b have been modified and expanded to provide management services. Second, Layer Management procedures have been added as 5.2.4. Note that Pascal variables are shared between Clause 4 and Clause 5. Within the Pascal descriptions provided in Clause 4, a "‡" in the left margin indicates a line that has been added to support management services. These lines are only required if Layer Management is being implemented. These changes do not affect any aspect of the MAC behavior as observed at the LLC-MAC and MAC-PLS interfaces.

The Pascal procedural specification shall be consulted for the definitive statement when there is any apparent ambiguity concerning the definition of some aspect of the CSMA/CD MAC access method.

The Layer Management facilities provided by the CSMA/CD MAC and Physical Layer management definitions provide the ability to manipulate management counters and initiate actions within the layers. The managed objects within this standard are defined as sets of attributes, actions, notifications, and behaviors in accordance with IEEE Std 802.1F-1993, and ISO/IEC International Standards for network management.

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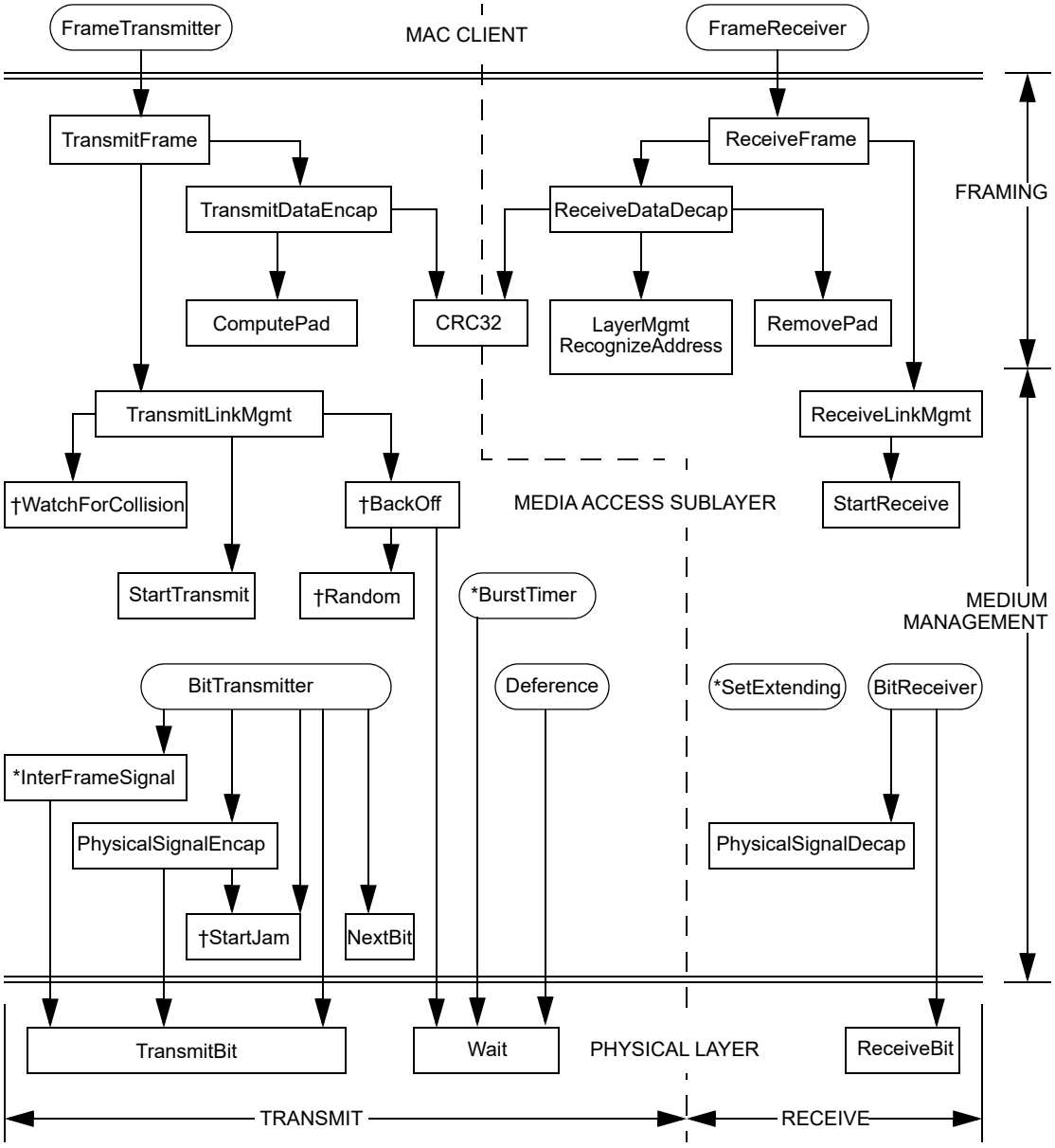

† Not applicable to full duplex operation.
* Applicable only to half duplex operation at 1000 Mb/s.

Figure 4–1—Relationship among CSMA/CD procedures

4.2.3 Packet transmission model

Packet transmission includes the following data encapsulation and Media Access management aspects:

a) Transmit Data Encapsulation includes the assembly of the outgoing packet (from the values provided by the MAC client) and frame check sequence generation (if not provided by the MAC client).
b) Transmit Media Access Management includes carrier deference, interpacket gap, collision detection and enforcement, collision backoff and retransmission, carrier extension and packet bursting.

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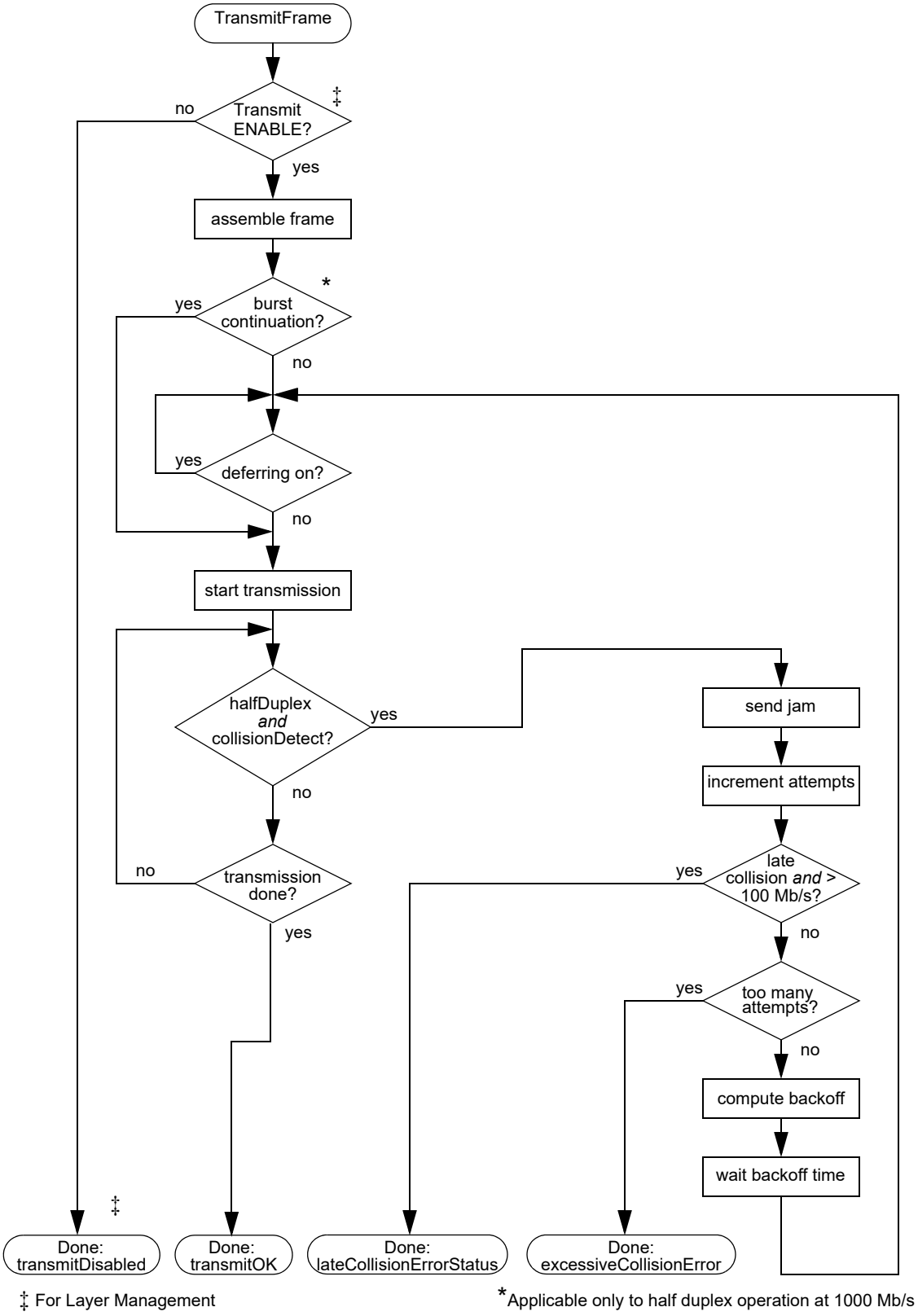

a) TransmitFrame

Figure 4–2a—Control flow summary

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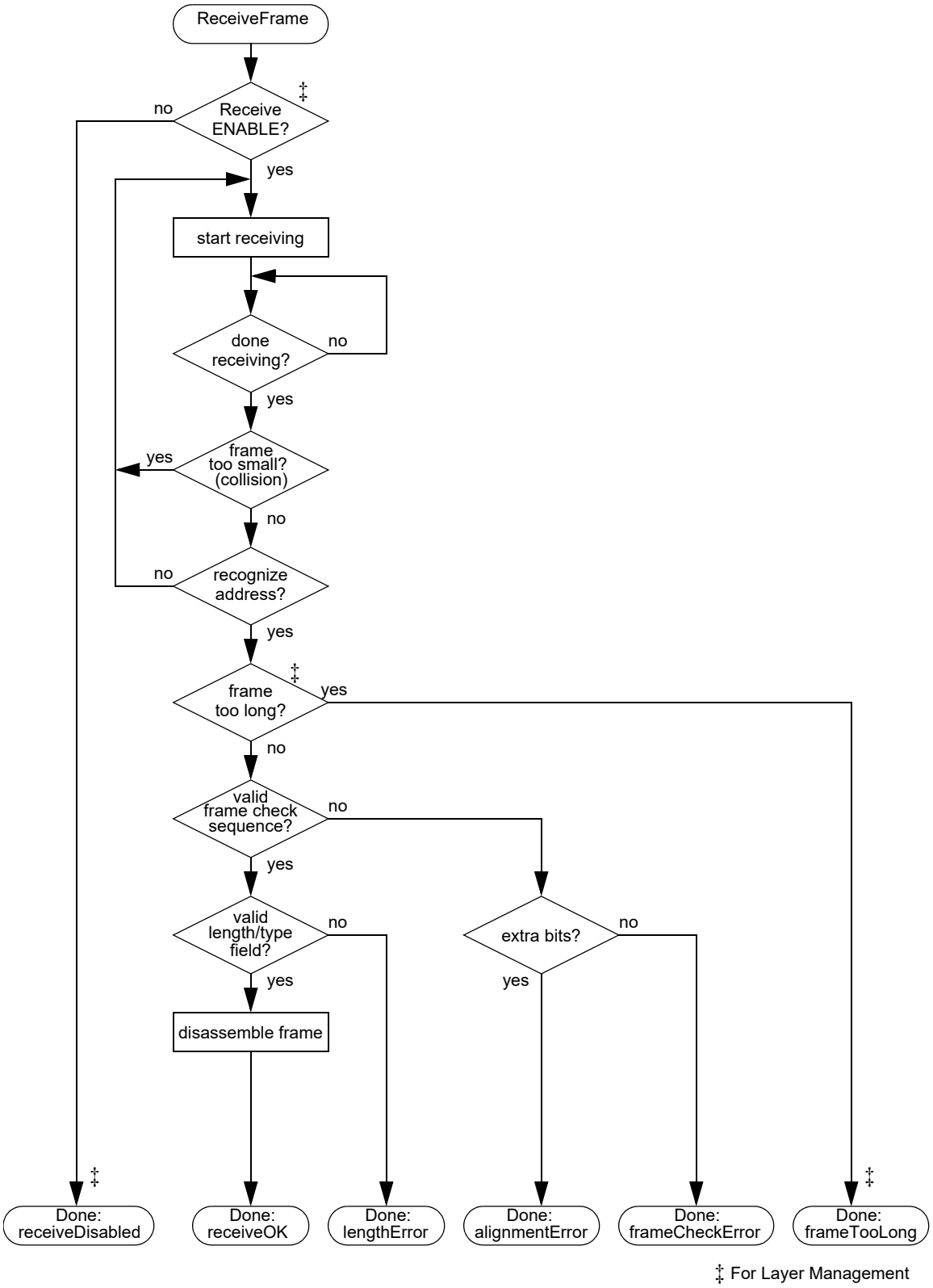

b) ReceiveFrame

Figure 4–2b—Control flow summary

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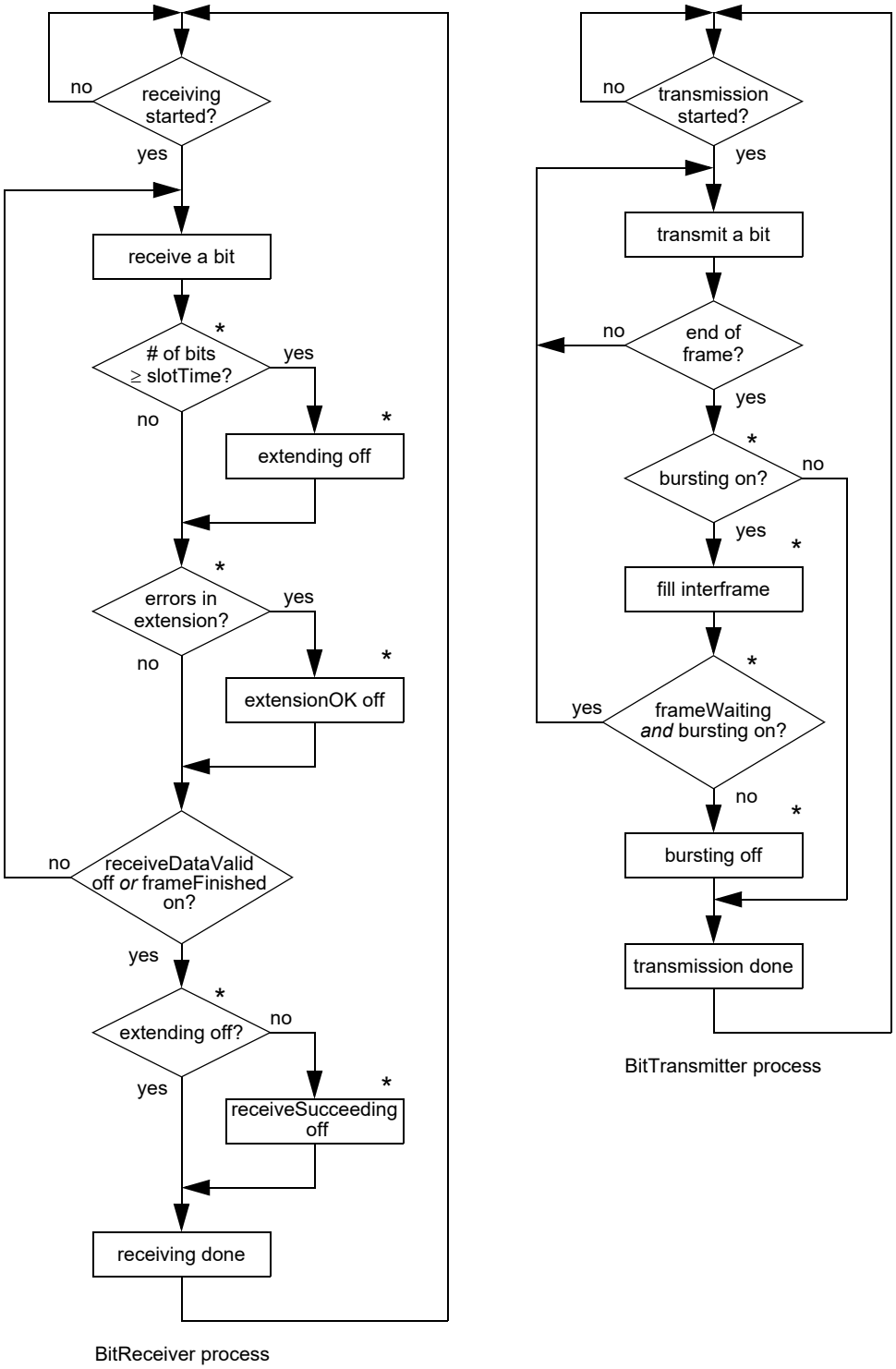

*Applicable only to half duplex operation at 1000 Mb/s

a) MAC sublayer

Figure 4–3a—Control flow

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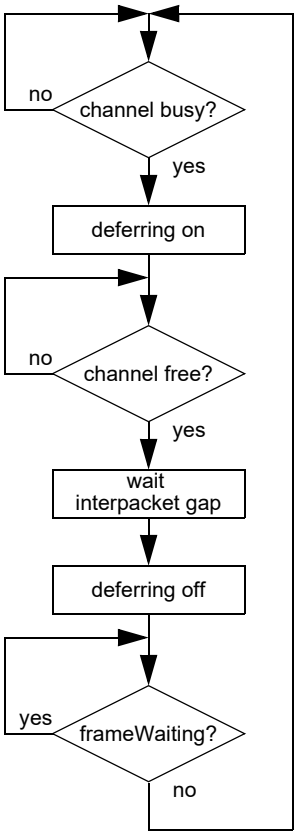
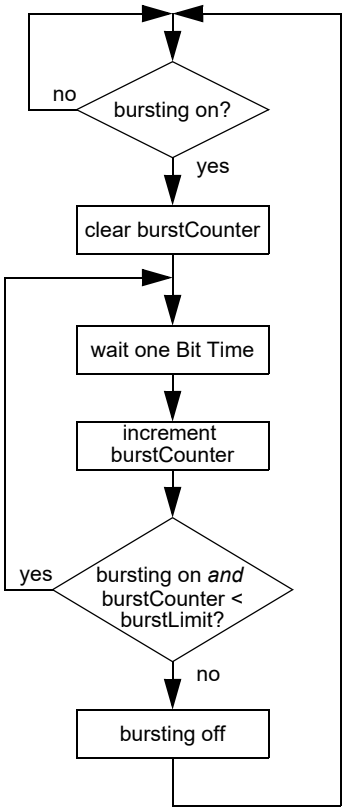
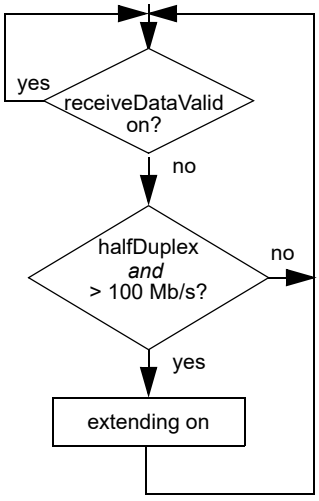


Deference process



*BurstTimer process



*SetExtending process

*Applicable only to half duplex operation at 1000 Mb/s

b) MAC sublayer

Figure 4–3b—Control flow

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4.2.3.1 Transmit data encapsulation

The fields of the CSMA/CD MAC frame are set to the values provided by the MAC client as arguments to the TransmitFrame operation (see 4.3) with the following possible exceptions: the padding field, the extension field, and the frame check sequence. The padding field is necessary to enforce the minimum frame size. The extension field is necessary to enforce the minimum carrier event duration on the medium in half duplex mode at an operating speed of 1000 Mb/s. The frame check sequence field may be (optionally) provided as an argument to the MAC sublayer. It is optional for a MAC to support the provision of the frame check sequence in such an argument. If this field is provided by the MAC client, the padding field shall also be provided by the MAC client, if necessary. If this field is not provided by the MAC client, or if the MAC does not support the provision of the frame check sequence as an external argument, it is set to the CRC value generated by the MAC sublayer, after appending the padding field, if necessary.

4.2.3.2 Transmit media access management

4.2.3.2.1 Deference

When a packet is submitted by the MAC client for transmission, the transmission is initiated as soon as possible, but in conformance with the rules of deference stated below. The rules of deference differ between half duplex and full duplex modes.

a) *Half duplex mode*

Even when it has nothing to transmit, the CSMA/CD MAC sublayer monitors the physical medium for traffic by watching the carrierSense signal provided by the PLS. Whenever the medium is busy, the CSMA/CD MAC defers to the passing packet by delaying any pending transmission of its own. After the last bit of the passing packet (that is, when *carrierSense* changes from true to false), the CSMA/CD MAC continues to defer for a proper interPacketGap (see 4.2.3.2.2).

If, at the end of the interPacketGap, a packet is waiting to be transmitted, transmission is initiated independent of the value of carrierSense. When transmission has completed (or immediately, if there was nothing to transmit) the CSMA/CD MAC sublayer resumes its original monitoring of carrierSense.

NOTE—It is possible for the PLS carrier sense indication to fail to be asserted briefly during a collision on the media. If the Deference process simply times the interpacket gap based on this indication it is possible for a short interpacket gap to be generated, leading to a potential reception failure of a subsequent frame. To enhance system robustness the following optional measures, as specified in 4.2.8, are recommended when interPacketGapPart1 is other than zero:

Start the timing of the interPacketGap as soon as transmitting and carrierSense are both false. Reset the interPacketGap timer if carrierSense becomes true during the first 2/3 of the interPacketGap timing interval. During the final 1/3 of the interval, the timer shall not be reset to ensure fair access to the medium. An initial period shorter than 2/3 of the interval is permissible including zero.

b) *Full duplex mode*

In full duplex mode, the CSMA/CD MAC does not defer pending transmissions based on the carrierSense signal from the PLS. Instead, it uses the internal variable *transmitting* to maintain proper MAC state while the transmission is in progress. After the last bit of a transmitted frame, (that is, when *transmitting* changes from true to false), the MAC continues to defer for a proper interPacketGap (see 4.2.3.2.2).

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4.2.3.2.2 Interpacket gap

As defined in 4.2.3.2.1, the rules for deferring to passing packets ensure a minimum interpacket spacing of interPacketGap bit times. This is intended to provide interpacket recovery time for other CSMA/CD sublayers and for the physical medium.

Note that interPacketGap is the minimum value of the interpacket gap. If necessary for implementation reasons, a transmitting sublayer may use a larger value with a resulting decrease in its throughput. The larger value is determined by the parameters of the implementation, see 4.4.

A larger value for interpacket gap is used for dynamically adapting the nominal data rate of the MAC sublayer to SONET/SDH data rates (with packet granularity) for WAN-compatible applications of this standard. While in this optional mode of operation, the MAC sublayer counts the number of bits sent during a frame's transmission. After the packet's transmission has been completed, the MAC sublayer extends the minimum interpacket gap by a number of bits that is proportional to the length of the previously transmitted packet. For more details, see 4.2.7 and 4.2.8.

4.2.3.2.3 Collision handling (half duplex mode only)

Once a CSMA/CD sublayer has finished deferring and has started transmission, it is still possible for it to experience contention for the medium. Collisions can occur until acquisition of the network has been accomplished through the deference of all other stations' CSMA/CD sublayers.

The dynamics of collision handling are largely determined by a single parameter called the slot time. This single parameter describes three important aspects of collision handling:

a) It is an upper bound on the acquisition time of the medium.
b) It is an upper bound on the length of a packet fragment generated by a collision.
c) It is the scheduling quantum for retransmission.

To fulfill all three functions, the slot time shall be larger than the sum of the Physical Layer round-trip propagation time and the Media Access Layer maximum jam time. The slot time is determined by the parameters of the implementation, see 4.4.

4.2.3.2.4 Collision detection and enforcement (half duplex mode only)

Collisions are detected by monitoring the collisionDetect signal provided by the Physical Layer. When a collision is detected during a packet transmission, the transmission is not terminated immediately. Instead, the transmission continues until additional bits specified by jamSize have been transmitted (counting from the time collisionDetect went on). This collision enforcement or jam guarantees that the duration of the collision is sufficient to ensure its detection by all transmitting stations on the network. The content of the jam is unspecified; it may be any fixed or variable pattern convenient to the Media Access implementation; however, the implementation shall not be intentionally designed to be the 32-bit CRC value corresponding to the (partial) packet transmitted prior to the jam.

4.2.3.2.5 Collision backoff and retransmission (half duplex mode only)

When a transmission attempt has terminated due to a collision, it is retried by the transmitting CSMA/CD sublayer until either it is successful or a maximum number of attempts (attemptLimit) have been made and all have terminated due to collisions. Note that all attempts to transmit a given packet are completed before any subsequent outgoing packets are transmitted. The scheduling of the retransmissions is determined by a controlled randomization process called "truncated binary exponential backoff." At the end of enforcing a collision (jamming), the CSMA/CD sublayer delays before attempting to retransmit the packet. The delay is

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an integer multiple of slotTime. The number of slot times to delay before the *n*th retransmission attempt is chosen as a uniformly distributed random integer *r* in the range:

$$0 \le r < 2^k$$

where

$$k = \min(n, 10)$$

If all attemptLimit attempts fail, this event is reported as an error. Algorithms used to generate the integer *r* should be designed to minimize the correlation between the numbers generated by any two stations at any given time.

Note that the values given above define the most aggressive behavior that a station may exhibit in attempting to retransmit after a collision. In the course of implementing the retransmission scheduling procedure, a station may introduce extra delays that will degrade its own throughput, but in no case may a station's retransmission scheduling result in a lower average delay between retransmission attempts than the procedure defined above.

4.2.3.2.6 Full duplex transmission

In full duplex mode, there is never contention for a shared physical medium. The Physical Layer may indicate to the MAC that there are simultaneous transmissions by both stations, but since these transmissions do not interfere with each other, a MAC operating in full duplex mode does not react to such Physical Layer indications. Full duplex stations do not defer to received traffic, nor abort transmission, jam, backoff, and reschedule transmissions as part of Transmit Media Access Management. Transmissions may be initiated whenever the station has a packet queued, subject only to the interpacket gap required to allow recovery for other sublayers and for the physical medium.

4.2.3.2.7 Packet bursting (half duplex mode only)

At an operating speed of 1000 Mb/s, an implementation may optionally transmit a series of packets without relinquishing control of the transmission medium. This mode of operation is referred to as *burst mode*. Once a packet has been successfully transmitted, the transmitting station can begin transmission of another packet without contending for the medium because all of the other stations on the network will continue to defer to its transmission, provided that it does not allow the medium to assume an idle condition between packets. The transmitting station fills the interpacket gap interval with extension bits, which are readily distinguished from data bits at the receiving stations, and which maintain the detection of carrier in the receiving stations. The transmitting station is allowed to initiate packet transmission until a specified limit, referred to as burstLimit, is reached. The value of burstLimit is specified in 4.4.2. Figure 4–4 shows an example of transmission with packet bursting.

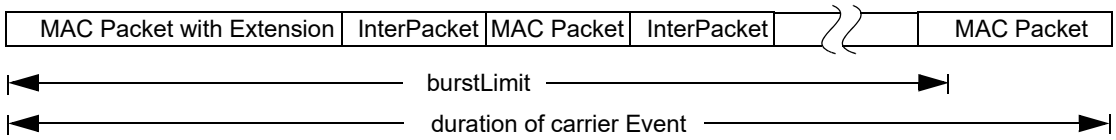

Figure 4–4—Packet bursting

The first packet of a burst will be extended, if necessary, as described in 4.2.3.4. Subsequent packets within a burst do not require extension. In a properly configured network, and in the absence of errors, collisions cannot occur during a burst at any time after the first packet of a burst (including any extension) has been

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transmitted. Therefore, the MAC will treat any collision that occurs after the first packet of a burst, or that occurs after the slotTime has been reached in the first packet of a burst, as a late collision.

4.2.3.3 Minimum frame size

The CSMA/CD Media Access mechanism requires that a minimum frame length of minFrameSize bits be transmitted. If frameSize is less than minFrameSize, then the CSMA/CD MAC sublayer shall append extra bits in units of octets (Pad), after the end of the MAC Client Data field but prior to calculating and appending the FCS (if not provided by the MAC client). The number of extra bits shall be sufficient to ensure that the frame, from the DA field through the FCS field inclusive, is at least minFrameSize bits. If the FCS is (optionally) provided by the MAC client, the Pad shall also be provided by the MAC client. The content of the Pad is unspecified.

4.2.3.4 Carrier extension (half duplex mode only)

At an operating speed of 1000 Mb/s, the slotTime employed at slower speeds is inadequate to accommodate network topologies of the desired physical extent. Carrier Extension provides a means by which the slotTime can be increased to a sufficient value for the desired topologies, without increasing the minFrameSize parameter, as this would have deleterious effects. Non-data bits, referred to as extension bits, are appended to frames that are less than slotTime bits in length so that the resulting transmission is at least one slotTime in duration. Carrier Extension can be performed only if the underlying Physical Layer is capable of sending and receiving symbols that are readily distinguished from data symbols, as is the case in most Physical Layers that use a block encoding/decoding scheme. The maximum length of the extension is equal to the quantity (slotTime − minFrameSize). Figure 4–5 depicts a frame with carrier extension.

The MAC continues to monitor the medium for collisions while it is transmitting extension bits, and it will treat any collision that occurs after the threshold (slotTime) as a late collision.

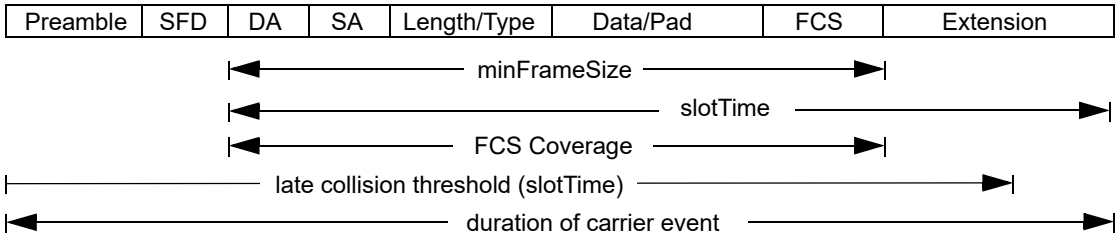

Figure 4–5—Frame with carrier extension

4.2.4 Frame reception model

CSMA/CD MAC sublayer frame reception includes both data decapsulation and Media Access management aspects:

a) Receive Data Decapsulation comprises address recognition, frame check sequence validation, and frame disassembly to pass the fields of the received frame to the MAC client.

b) Receive Media Access Management comprises recognition of collision fragments from incoming frames and truncation of frames to octet boundaries.

4.2.4.1 Receive data decapsulation

4.2.4.1.1 Address recognition

The CSMA/CD MAC sublayer is capable of recognizing individual and group addresses.

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a) *Individual Addresses.* The CSMA/CD MAC sublayer recognizes and accepts any frame whose DA field contains the individual address of the station.

b) *Group Addresses.* The CSMA/CD MAC sublayer recognizes and accepts any frame whose DA field contains the Broadcast address.

The CSMA/CD MAC sublayer is capable of activating some number of group addresses as specified by higher layers. The CSMA/CD MAC sublayer recognizes and accepts any frame whose Destination Address field contains an active group address. An active group address may be deactivated.

The MAC sublayer may also provide the capability of operating in the promiscuous receive mode. In this mode of operation, the MAC sublayer recognizes and accepts all valid frames, regardless of their Destination Address field values.

4.2.4.1.2 Frame check sequence validation

FCS validation is essentially identical to FCS generation. If the bits of the incoming frame (exclusive of the FCS field itself) do not generate a CRC value identical to the one received, an error has occurred and the frame is identified as invalid.

4.2.4.1.3 Frame disassembly

Upon recognition of the Start Frame Delimiter at the end of the preamble sequence, the CSMA/CD MAC sublayer accepts the frame. If there are no errors, the frame is disassembled and the fields are passed to the MAC client by way of the output parameters of the ReceiveFrame operation.

4.2.4.2 Receive media access management

4.2.4.2.1 Framing

The CSMA/CD sublayer recognizes the boundaries of an incoming MAC frame by monitoring the receiveDataValid signal provided by the Physical Layer. Two possible length errors can occur that indicate ill-framed data: the MAC frame may be too long, or its length may not be an integer number of octets.

a) *Maximum Frame Size.* The receiving CSMA/CD sublayer is not required to enforce the MAC frame size limit, but it is allowed to truncate MAC frames longer than maxFrameSizeLimit octets (see 4.2.7.1). If optional layer management is implemented, such frames may be counted whether or not they are truncated. They may also be reported as an implementation-dependent error.

CAUTION
It is recommended that any implementation that truncates MAC frames should invalidate those frames as they may have severely weakened error protection and may cause serious problems if forwarded to the MAC client.

b) *Integer Number of Octets in Frame.* Since the format of a valid MAC frame specifies an integer number of octets, only a collision or an error can produce a MAC frame with a length that is not an integer multiple of 8 bits. Complete MAC frames (that is, not rejected as collision fragments; see 4.2.4.2.2) that do not contain an integer number of octets are truncated to the nearest octet boundary. If frame check sequence validation detects an error in such a MAC frame, the status code alignmentError is reported.

When a burst of MAC frames is received while operating in half duplex mode at an operating speed of 1000 Mb/s, the individual MAC frames within the burst are delimited by sequences of interpacket fill symbols, which are conveyed to the receiving MAC sublayer as extension bits. Once the collision filtering requirements for a given MAC frame, as described in 4.2.4.2.2, have been satisfied, the receipt of an extension bit can be used as an indication that all of the data bits of the MAC frame have been received.

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4.2.4.2.2 Collision filtering

In the absence of a collision, the shortest valid transmission in half duplex mode has to be at least one slotTime in length. Within a burst of frames, the first frame of a burst has to be at least slotTime bits in length in order to be accepted by the receiver, while subsequent frames within a burst have to be at least minFrameSize in length. Anything less is presumed to be a fragment resulting from a collision, and is discarded by the receiver. In half duplex mode, occasional collisions are a normal part of the Media Access management procedure. The discarding of such a fragment by a MAC is not reported as an error.

The shortest valid transmission in full duplex mode has to be at least minFrameSize in length. While collisions do not occur in full duplex mode MACs, a full duplex MAC nevertheless discards received frames containing less than minFrameSize bits. The discarding of such a frame by a MAC is not reported as an error.

4.2.5 Preamble generation

In a LAN implementation, most of the Physical Layer components are allowed to provide valid output some number of bit times after being presented valid input signals. Thus it is necessary for a preamble to be sent before the start of data, to allow the PLS circuitry to reach its steady state. Upon request by TransmitLinkMgmt to transmit the first bit of a new frame, PhysicalSignalEncap shall first transmit the preamble, a bit sequence used for physical medium stabilization and synchronization, followed by the Start Frame Delimiter. If, while transmitting the preamble or Start Frame Delimiter, the collision detect variable becomes true, any remaining preamble and Start Frame Delimiter bits shall be sent. The preamble pattern is:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

The bits are transmitted in order, from left to right. The nature of the pattern is such that, for Manchester encoding, it appears as a periodic waveform on the medium that enables bit synchronization. It should be noted that the preamble ends with a “0.”

4.2.6 Start frame sequence

The receiveDataValid signal is the indication to the MAC that the frame reception process should begin. Upon reception of the sequence 10101011 following the assertion of receiveDataValid, PhysicalSignalDecap shall begin passing successive bits to ReceiveLinkMgmt for passing to the MAC client.

4.2.7 Global declarations

This subclause provides detailed formal specifications for the CSMA/CD MAC sublayer. It is a specification of generic features and parameters to be used in systems implementing this media access method. Subclause 4.4 provides values for these sets of parameters for recommended implementations of this media access mechanism.

4.2.7.1 Common constants, types, and variables

The following declarations of constants, types and variables are used by the MAC frame transmission and reception sections of each CSMA/CD sublayer:

```
const
    addressSize = 48; {In bits, in compliance with 3.2.3}
    lengthOrTypeSize = 16; {In bits}
    clientDataSize = ...; {In bits, size of MAC Client Data; see 4.2.2.2, a) 3)}
    padSize = ...; {In bits, = max (0, minFrameSize ─ (2 x addressSize + lengthOrTypeSize +
```


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```
                                                clientDataSize + crcSize))}
    dataSize = ...; {In bits, = clientDataSize + padSize}
    crcSize = 32; {In bits, 32-bit CRC}
    frameSize = ...; {In bits, = 2 x addressSize + lengthOrTypeSize + dataSize + crcSize; see 4.2.2.2, a)}
    minFrameSize = ..; {In bits, see 4.4}
    maxBasicFrameSize = 1518; {In octets, see 3.2.7, 4.4}
    maxEnvelopeFrameSize = 2000; {In octets, see 3.2.7, 4.4}
    qTagPrefixSize = 4; {In octets, length of Q-tag prefix, see 3.2.7, 4.4}
    maxFrameSizeLimit = maxBasicFrameSize or (maxBasicFrameSize + qTagPrefixSize) or
                        maxEnvelopeFrameSize ; {in octets}
    extend = ...; {Boolean, true if (slotTime ─ minFrameSize) > 0, false otherwise}
    extensionBit = ...; {A non-data value which is used for carrier extension and interpacket
                        during bursts}
    extensionErrorBit = ...; {A non-data value which is used to jam during carrier extension}
    minTypeValue = 1536; {Minimum value of the Length/Type field for Type interpretation}
    maxBasicDataSize = 1500;
                        {In octets, the maximum length of the MAC Client Data field of the basic frame.}
    slotTime = ...; {In bit times, unit of time for collision handling, implementation-dependent, see 4.4}
    preambleSize = 56; {In bits, see 4.2.5}
    sfdSize = 8; {In bits, Start Frame Delimiter}
    headerSize = 64; {In bits, sum of preambleSize and sfdSize}
type
    Bit = (0, 1);
    PhysicalBit = (0, 1, extensionBit, extensionErrorBit);
                                {Bits transmitted to the Physical Layer can be either 0, 1, extensionBit or
                                extensionErrorBit. Bits received from the Physical Layer can be either 0, 1
                                or extensionBit}
    AddressValue = array [1..addressSize] of Bit;
    LengthOrTypeValue = array [1..lengthOrTypeSize] of Bit;
    DataValue = array [1..dataSize] of Bit; {Contains the portion of the MAC frame that starts with the first
                                            bit following the Length/Type field and ends with the last bit
                                            prior to the FCS field.
    CRCValue = array [1..crcSize] of Bit;
    PreambleValue = array [1..preambleSize] of Bit;
    SfdValue = array [1..sfdSize] of Bit;
    ViewPoint = (fields, bits); {Two ways to view the contents of a frame}
    HeaderViewPoint = (headerFields, headerBits);
    Frame = record {Format of MAC frame}
        case view: ViewPoint of
            fields: (
                destinationField: AddressValue;
                sourceField: AddressValue;
                lengthOrTypeField: LengthOrTypeValue;
                dataField: DataValue;
                fcsField: CRCValue);
            bits: (contents: array [1..frameSize] of Bit)
        end; {MAC frame}
    Header = record {Format of Preamble and Start Frame Delimiter}
        case headerView: HeaderViewPoint of
            headerFields: (
                preamble: PreambleValue;
                sfd: SfdValue);
            headerBits: (headerContents: array [1..headerSize] of Bit)
```


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```
    end; {Defines header for MAC frame}
  TransmitStatus = (transmitOK, excessiveCollisionError, lateCollisionErrorStatus);
‡ TransmitStatus = (transmitDisabled, transmitOK, excessiveCollisionError,
                    lateCollisionErrorStatus);
  ReceiveStatus = (receiveOK, lengthError, frameCheckError, alignmentError);
‡ ReceiveStatus = (receiveDisabled, receiveOK, frameTooLong, frameCheckError,
                    lengthError, alignmentError);
var
  halfDuplex: Boolean; {Indicates the desired mode of operation. halfDuplex is a static variable; its value
                        shall only be changed by the invocation of the Initialize procedure}
```

4.2.7.2 Transmit state variables

The following items are specific to packet transmission. (See also 4.4.)

```
const
  interPacketGap = ...; {In bit times, minimum gap between packets, see 4.4}
  interPacketGapPart1 = ...; {In bit times, duration of the first portion of
                              interPacketGap. In the
                              range of 0 to 2/3 of interPacketGap}
  interPacketGapPart2 = ...; {In bit times, duration of the remainder of
                              interPacketGap. Equal to
                              interPacketGap –
                              interPacketGapPart1}
  ipgStretchRatio = ...; {In bits, determines the number of bits in a packet that
                          require one octet of interPacketGap extension,
                          when ipgStretchMode is enabled;
                          see 4.4 and 4.2.8}
  attemptLimit = ...; {Max number of times to attempt transmission}
  backOffLimit = ...; {Limit on number of times to back off}
  burstLimit= ...; {In bits, limit for initiation of packet transmission in Burst Mode,
                    see 4.4 and 4.2.8}
  jamSize = ...; {In bits, the value depends upon port type and duplex/half-duplex mode.
                  See 4.1.2.2 and 4.4.}
var
  outgoingFrame: Frame; {The frame to be transmitted}
  outgoingHeader: Header;
  currentTransmitBit, lastTransmitBit: 1..frameSize; {Positions of current and last outgoing bits in
                                                      outgoingFrame}
  lastHeaderBit: 1..headerSize;
  deferring: Boolean; {Implies any pending transmission has to wait for the medium to clear}
  frameWaiting: Boolean; {Indicates that outgoingFrame is deferring}
  attempts: 0..attemptLimit; {Number of transmission attempts on outgoingFrame}
  newCollision: Boolean; {Indicates that a collision has occurred but has not yet been jammed}
  transmitSucceeding: Boolean; {Running indicator of whether transmission is succeeding}
  burstMode: Boolean; {Indicates the desired mode of operation, and enables the transmission of
                       multiple frames in a single carrier event. burstMode is a static variable; its
                       value shall only be changed by the invocation of the Initialize procedure}
  bursting: Boolean; {In burstMode, the given station has acquired the medium and the burst timer has
                      not yet expired}
  burstStart: Boolean; {In burstMode, indicates that the first frame transmission is in progress}
  extendError: Boolean; {Indicates a collision occurred while sending extension bits}
  ipgStretchMode: Boolean; {Indicates the desired mode of operation, and enables
```


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```
                    the lowering of the average data rate
                    of the MAC sublayer (with packet granularity), using
                    extension of the minimum interPacketGap.
                    ipgStretchMode is a static
                    variable; its value shall only be changed by the invocation of the Initialize
                    procedure}
  ipgStretchCount: 0..ipgStretchRatio; {In bits, a running
                                        counter that counts the number of bits during a
                                        packet's transmission that are to be considered for the
                                        minimum interPacketGap extension,
                                        while operating in ipgStretchMode}
  ipgStretchSize: 0..(((maxFrameSizeLimit) x 8 + headerSize + interPacketGap
                  + ipgStretchRatio – 1) div ipgStretchRatio);
                  {In octets, a running counter that counts the integer number of octets that are to be
                  added to the minimum interPacketGap, while operating in
                  ipgStretchMode}
```

4.2.7.3 Receive state variables

The following items are specific to frame reception. (See also 4.4.)

```
var
  incomingFrame: Frame; {The frame being received}
  receiving: Boolean; {Indicates that a frame reception is in progress}
  excessBits: 0..7; {Count of excess trailing bits beyond octet boundary}
  receiveSucceeding: Boolean; {Running indicator of whether reception is succeeding}
  validLength: Boolean; {Indicator of whether received frame has a length error}
  exceedsMaxLength: Boolean; {Indicator of whether received frame has a length longer than the
                              maximum permitted length}
  extending: Boolean; {Indicates whether the current frame is subject to carrier extension}
  extensionOK: Boolean; {Indicates whether any bit errors were found in the extension part of a packet,
                         which is not checked by the CRC}
  passReceiveFCSMode: Boolean; {Indicates the desired mode of operation, and enables passing of
                                the frame check sequence field of all received frames from the
                                MAC sublayer to the MAC client. passReceiveFCSMode is a
                                static variable}
```

4.2.7.4 State variable initialization

The procedure Initialize has to be run when the MAC sublayer begins operation, before any of the processes begin execution. Initialize sets certain crucial shared state variables to their initial values. (All other global variables are appropriately reinitialized before each use.) Initialize then waits for the medium to be idle, and starts operation of the various processes.

NOTE—Care should be taken to ensure that the time from the completion of the Initialize process to when the first packet transmission begins is at least an interPacketGap.

If Layer Management is implemented, the Initialize procedure shall only be called as the result of the initializeMAC action (30.3.1.2.1).

```
procedure Initialize;
begin
  frameWaiting := false;
  deferring := false;
```


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```
    newCollision := false;
    transmitting := false; {An interface to Physical Layer; see below}
    receiving := false;
    halfDuplex := ...; {True for half duplex operation, false for full duplex operation. For operation at
                        speeds above 1000 Mb/s, halfDuplex shall always be false}
    bursting := false;
    burstMode := ...; { True for half duplex operation at an operating speed of 1000
                        Mb/s, when multiple frames' transmission in a single carrier event is desired and
                        supported, false otherwise}
    extending := extend and halfDuplex;
    ipgStretchMode := ...; {True for operating speeds above 1000 Mb/s when lowering the average data rate
                            of the MAC sublayer (with frame granularity) is desired and supported, false
                            otherwise}
    ipgStretchCount := 0;
    ipgStretchSize := 0;
    passReceiveFCSMode := ...; {True when enabling the passing of the frame check sequence of all
                                received frames from the MAC sublayer to the MAC client is desired and
                                supported, false otherwise}
    if halfDuplex then while carrierSense or receiveDataValid do nothing
    else while receiveDataValid do nothing
    {Start execution of all processes}
end; {Initialize}
```

4.2.8 Frame transmission

The algorithms in this subclause define MAC sublayer frame transmission. The function TransmitFrame implements the frame transmission operation provided to the MAC client.

The TransmitFrame operation is synchronous. Its duration is the entire attempt to transmit the frame; when the operation completes, transmission has either succeeded or failed, as indicated by the TransmitStatus status code.

The transmitDisabled status code (if layer management is implemented) indicates that the transmitter is not enabled. Successful transmission is indicated by the status code transmitOK. The code excessiveCollisionError indicates that the transmission attempt was aborted due to excessive collisions, because of heavy traffic or a network failure. MACs operating in the half duplex mode at the speed of 1000 Mb/s are required to report lateCollisionErrorStatus in response to a late collision; MACs operating in the half duplex mode at speeds of 100 Mb/s and below are not required to do so. TransmitStatus is not used by the service interface defined in 2.3.1. TransmitStatus may be used in an implementation dependent manner.

```
function TransmitFrame (
    destinationParam: AddressValue;
    sourceParam: AddressValue;
    lengthOrTypeParam: LengthOrTypeValue;
    dataParam: DataValue;
    fcsParamValue: CRCValue;
    fcsParamPresent: Bit): TransmitStatus;
procedure TransmitDataEncap; {Nested procedure; see body below}
begin
    if transmitEnabled then
        begin
            TransmitDataEncap;
```


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```
            TransmitFrame := TransmitLinkMgmt
        end
    else TransmitFrame := transmitDisabled
end; {TransmitFrame}
```

If transmission is enabled, TransmitFrame calls the internal procedure TransmitDataEncap to construct the frame. Next, TransmitLinkMgmt is called to perform the actual transmission. The TransmitStatus returned indicates the success or failure of the transmission attempt.

TransmitDataEncap builds the frame and places the 32-bit CRC in the frame check sequence field:

```
procedure TransmitDataEncap;
begin
    with outgoingFrame do
        begin {Assemble frame}
            view := fields;
            destinationField := destinationParam;
            sourceField := sourceParam;
            lengthOrTypeField := lengthOrTypeParam;
            if fcsParamPresent then
                begin
                    dataField := dataParam; {No need to generate pad if the FCS is passed from MAC client}
                    fcsField := fcsParamValue {Use the FCS passed from MAC client}
                end
            else
                begin
                    dataField := ComputePad(dataParam);
                    fcsField := CRC32(outgoingFrame)
                end;
            view := bits
        end {Assemble frame}
    with outgoingHeader do
        begin
            headerView := headerFields;
            preamble := ...; {* '1010...10,' LSB to MSB*}
            sfd := ...; {* '10101011,' LSB to MSB*}
            headerView := headerBits
        end
end; {TransmitDataEncap}
```

If the MAC client chooses to generate the frame check sequence field for the frame, it passes this field to the MAC sublayer via the fcsParamValue parameter. If the fcsParamPresent parameter is true, TransmitDataEncap uses the fcsParamValue parameter as the frame check sequence field for the frame. Such a frame shall not require any padding, since it is the responsibility of the MAC client to ensure that the frame meets the minFrameSize constraint. If the fcsParamPresent parameter is false, the fcsParamValue parameter is unspecified.TransmitDataEncap first calls the ComputePad function, followed by a call to the CRC32 function to generate the padding (if necessary) and the frame check sequence field for the frame internally to the MAC sublayer.

ComputePad appends an array of arbitrary bits to the MAC client data to pad the frame to the minimum frame size:

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```
function ComputePad(var dataParam: DataValue): DataValue;
begin
   ComputePad := {Append an array of size padSize of arbitrary bits to the MAC client dataField}
end; {ComputePad}
```

TransmitLinkMgmt attempts to transmit the frame. In half duplex mode, it first defers to any passing traffic. In half duplex mode, if a collision occurs, transmission is terminated properly and retransmission is scheduled following a suitable backoff interval:

```
function TransmitLinkMgmt: TransmitStatus;
begin
   attempts := 0;
   transmitSucceeding := false;
   lateCollisionCount := 0;
   deferred := false; {Initialize}
   excessDefer := false;
   while  (attempts < attemptLimit) and (not transmitSucceeding)
                                          and (not extend or lateCollisionCount = 0) do
                                  {No retransmission after late collision if operating at 1000 Mb/s}
      begin {Loop}
         if bursting then {This is a burst continuation}
            frameWaiting := true {Start transmission without checking deference}
         else {Non bursting case, or first frame of a burst}
            begin
               if attempts>0 then BackOff;
               frameWaiting := true;
               while deferring do {Defer to passing frame, if any[35]}
                  if halfDuplex then deferred := true;
               burstStart := true;
               if burstMode then bursting := true
            end;
         lateCollisionError := false;
         StartTransmit;
         frameWaiting := false;
         if halfDuplex then
         begin
            while transmitting do WatchForCollision;
            if lateCollisionError then lateCollisionCount := lateCollisionCount + 1;
            attempts := attempts + 1
         end {Half duplex mode}
         else while transmitting do nothing {Full duplex mode}
      end; {Loop}
   LayerMgmtTransmitCounters; {Update transmit and transmit error counters in 5.2.4.2}
   if transmitSucceeding then
      begin
         if burstMode then burstStart := false; {Can't be the first frame anymore}
         TransmitLinkMgmt := transmitOK
      end
   else if (extend and lateCollisionCount > 0) then TransmitLinkMgmt := lateCollisionErrorStatus;
   else  TransmitLinkMgmt := excessiveCollisionError
end;{TransmitLinkMgmt}
```

[35] The Deference process ensures that the reception of traffic does not cause deferring to be true when in full duplex mode. Deferring is used in full duplex mode to enforce the minimum interpacket gap spacing.

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Each time a frame transmission attempt is initiated, StartTransmit is called to alert the BitTransmitter process that bit transmission should begin:

```
procedure StartTransmit;
begin
    currentTransmitBit := 1;
    lastTransmitBit := frameSize;
    lastHeaderBit := headerSize;
    transmitSucceeding := true;
    transmitting := true
end; {StartTransmit}
```

In half duplex mode, TransmitLinkMgmt monitors the medium for contention by repeatedly calling WatchForCollision, once frame transmission has been initiated:

```
procedure WatchForCollision;
begin
    if transmitSucceeding and collisionDetect then
        begin
            if currentTransmitBit > (slotTime – headerSize) then lateCollisionError := true;
            newCollision := true;
            transmitSucceeding := false;
            if burstMode then
            begin
                bursting := false;
                if not burstStart then
                    lateCollisionError := true {Every collision is late, unless it hits the first frame in a burst}
            end
        end
end; {WatchForCollision}
```

WatchForCollision, upon detecting a collision, updates newCollision to ensure proper jamming by the BitTransmitter process. The current transmit bit number is checked to see if this is a late collision. If the collision occurs later than a collision window of slotTime bits into the packet, it is considered as evidence of a late collision. The point at which the collision is received is determined by the network media propagation time and the delay time through a station and, as such, is implementation-dependent (see 4.1.2.2). While operating at speeds of 100 Mb/s or lower, an implementation may optionally elect to end retransmission attempts after a late collision is detected. While operating at the speed of 1000 Mb/s, an implementation shall end retransmission attempts after a late collision is detected.

After transmission of the jam has been completed, if TransmitLinkMgmt determines that another attempt should be made, BackOff is called to schedule the next attempt to retransmit the frame.

```
function Random (low, high: integer): integer;
begin
    Random := ...{Uniformly distributed random integer r, such that low ≤ r < high}
end; {Random}
```

BackOff performs the truncated binary exponential backoff computation and then waits for the selected multiple of the slot time:

```
var maxBackOff: 2..1024; {Working variable of BackOff}
procedure BackOff;
```


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```
begin
    if attempts = 1 then maxBackOff := 2
    else if attempts ≤ backOffLimit then maxBackOff := maxBackOff x 2;
    Wait(slotTime x Random(0, maxBackOff))
end; {BackOff}
```

BurstTimer is a process that does nothing unless the bursting variable is true. When bursting is true, BurstTimer increments burstCounter until the burstLimit limit is reached, whereupon BurstTimer assigns the value false to bursting:

```
process BurstTimer;
begin
    cycle
        while not bursting do nothing; {Wait for a burst}
        Wait(burstLimit);
        bursting := false
    end {burstMode cycle}
end; {BurstTimer}
```

The Deference process runs asynchronously to continuously compute the proper value for the variable deferring. In the case of half duplex burst mode, deferring remains true throughout the entire burst. Interpacket gap spacing may be used to lower the average data rate of a MAC at operating speeds above 1000 Mb/s in the full duplex mode, when it is necessary to adapt it to the data rate of a WAN-based Physical Layer. When interpacket stretching is enabled, deferring remains true throughout the entire extended interpacket gap, which includes the sum of interPacketGap and the interpacket extension as determined by the BitTransmitter:

```
process Deference;
    var realTimeCounter: integer; wasTransmitting: Boolean;
begin
    if halfDuplex then cycle{Half duplex loop}
        while not carrierSense do nothing; {Watch for carrier to appear}
        deferring := true;  {Delay start of new transmissions}
        wasTransmitting := transmitting;
        while carrierSense or transmitting do wasTransmitting := wasTransmitting or transmitting;
        if wasTransmitting then Wait(interPacketGapPart1) {Time out first part of
            interpacket gap}
        else
            begin
                realTimeCounter := interPacketGapPart1;
                repeat
                    while carrierSense do realTimeCounter := interPacketGapPart1;
                    Wait(1);
                    realTimeCounter := realTimeCounter – 1
                until (realTimeCounter = 0)
            end;
        Wait(interPacketGapPart2); {Time out second part of
            interpacket gap}
        deferring := false; {Allow new transmissions to proceed}
        while frameWaiting do nothing {Allow waiting transmission, if any}
    end {Half duplex loop}
    else cycle {Full duplex loop}
        while not transmitting do nothing; {Wait for the start of a transmission}
        deferring := true; {Inhibit future transmissions}
```


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```
        while transmitting do nothing; {Wait for the end of the current transmission}
        Wait(interPacketGap + ipgStretchSize × 8); {Time out entire interpacket
            gap and IPG extension}
        if not frameWaiting then {Don't roll over the remainder into the next frame}
            begin
                Wait(8);
                ipgStretchCount := 0
            end
        deferring := false {Don't inhibit transmission}
    end {Full duplex loop}
end; {Deference}
```

If the ipgStretchMode is enabled, the Deference process continues to enforce interpacket gap for an additional number of bit times, after the completion of timing the interPacketGap. The additional number of bit times is reflected by the variable ipgStretchSize. If the variable ipgStretchCount is less than ipgStretchRatio and the next frame is ready for transmission (variable frameWaiting is true), the Deference process enforces interpacket gap only for the integer number of octets, as indicated by ipgStretchSize, and saves ipgStretchCount for the next frame's transmission. If the next frame is not ready for transmission (variable frameWaiting is false), then the Deference process initializes the ipgStretchCount variable to zero.

The BitTransmitter process runs asynchronously, transmitting bits at a rate determined by the Physical Layer's TransmitBit operation:

```
process BitTransmitter;
begin
    cycle {Outer loop}
        if transmitting then
            begin {Inner loop}
                extendError := false;
                if ipgStretchMode then {Calculate the counter values}
                    begin
                        ipgStretchSize := (ipgStretchCount + headerSize +
                            frameSize + interPacketGap) div
                                                ipgStretchRatio; {Extension of the
                                                interpacket gap}
                        ipgStretchCount := (ipgStretchCount + headerSize +
                            frameSize + interPacketGap)
                                mod ipgStretchRatio {Remainder to carry over into
                                    the next frame's transmission}
                    end;
                PhysicalSignalEncap;  {Send preamble and start of frame delimiter}
                while transmitting do
                    begin
                        if (currentTransmitBit > lastTransmitBit) then TransmitBit(extensionBit)
                        else if extendError then TransmitBit(extensionErrorBit) {Jam in extension}
                        else TransmitBit(outgoingFrame[currentTransmitBit]);
                        if newCollision then StartJam else NextBit
                    end;
                if bursting then
                    begin
                        interPacketSignal;
                        if extendError then
                            if transmitting then transmitting := false
                                        {TransmitFrame may have been called during
```


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```
                                        interPacketSignal}
                    else IncLargeCounter(lateCollision);
                                        {Count late collisions which were missed by TransmitLinkMgmt}
                bursting := bursting and (frameWaiting or transmitting)
            end
        end {Inner loop}
    end {Outer loop}
end; {BitTransmitter}
```

The bits transmitted to the Physical Layer can take one of four values: data zero (0), data one (1), extensionBit (EXTEND), or extensionErrorBit (EXTEND_ERROR). The values extensionBit and extensionErrorBit are not transmitted between the first preamble bit of a frame and the last data bit of a frame under any circumstances. The BitTransmitter calls the procedure TransmitBit with bitParam = extensionBit only when it is necessary to perform carrier extension on a frame after all of the data bits of a frame have been transmitted. The BitTransmitter calls the procedure TransmitBit with bitParam = extensionErrorBit only when it is necessary to jam during carrier extension.

```
procedure PhysicalSignalEncap;
begin
    while currentTransmitBit ≤ lastHeaderBit do
        begin
            TransmitBit(outgoingHeader[currentTransmitBit]); {Transmit header one bit at a time}
            currentTransmitBit := currentTransmitBit + 1
        end;
    if newCollision then StartJam else currentTransmitBit := 1
end; {PhysicalSignalEncap}
```

The procedure interPacketSignal fills the interpacket interval between the frames of a burst with extensionBits. InterPacketSignal also monitors the variable collisionDetect during the interpacket interval between the frames of a burst, and will end a burst if a collision occurs during the interpacket interval. The procedural model is defined such that a MAC operating in the burstMode will emit an extraneous sequence of interPacketSize extensionBits in the event that there are no additional frames ready for transmission after interPacketSignal returns. Implementations may be able to avoid sending this extraneous sequence of extensionBits if they have access to information (such as the occupancy of a transmit queue) that is not assumed to be available to the procedural model.

```
procedure interPacketSignal;
    var interPacketCount, interPacketTotal: integer;
begin
    interPacketCount := 0;
    interPacketTotal := interPacketGap;
    while interPacketCount < interPacketTotal do
        begin
            if not extendError then TransmitBit(extensionBit)
            else TransmitBit(extensionErrorBit);
            interPacketCount := interPacketCount + 1;
            if collisionDetect and not extendError then
            begin
                bursting := false;
                extendError := true;
                interPacketCount := 0;
                interPacketTotal := jamSize
            end
        end
```


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```
end; {interPacketSignal}

procedure NextBit;
begin
    currentTransmitBit := currentTransmitBit + 1;
    if halfDuplex and burstStart and transmitSucceeding then {Carrier extension may be required}
        transmitting := (currentTransmitBit ≤ max(lastTransmitBit, slotTime))
    else transmitting := (currentTransmitBit ≤ lastTransmitBit)
end; {NextBit}

procedure StartJam;
begin
    extendError := currentTransmitBit > lastTransmitBit;
    currentTransmitBit := 1;
    lastTransmitBit := jamSize;
    newCollision := false
end; {StartJam}
```

BitTransmitter, upon detecting a new collision, immediately enforces it by calling StartJam to initiate the transmission of the jam. The jam should contain a sufficient number of bits of arbitrary data so that it is assured that both communicating stations detect the collision. (StartJam uses the first set of bits of the frame up to jamSize, merely to simplify this program.)

4.2.9 Frame reception

The algorithms in this subclause define CSMA/CD Media Access sublayer frame reception.

The function ReceiveFrame implements the frame reception operation provided to the MAC client.

The ReceiveFrame operation is synchronous. The operation does not complete until a frame has been received. The fields of the frame are delivered via the output parameters with a status code.

The receiveDisabled status code (if layer management is implemented) indicates that the receiver is not enabled. Successful reception is indicated by the status code receiveOK. The frameTooLong error code (if layer management is implemented) indicates that the last frame received had a frameSize beyond the maximum allowable frame size. The code frameCheckError indicates that the frame received was damaged by a transmission error. The lengthError indicates that the lengthOrTypeParam value was both consistent with a length interpretation of this field (i.e., its value was less than or equal to maxValidFrame), and inconsistent with the frameSize of the received frame. The code alignmentError indicates that the frame received was damaged, and that in addition, its length was not an integer number of octets. ReceiveStatus is not mapped to any MAC client parameter by the service interface defined in 2.3.2. ReceiveStatus may be used in an implementation dependent manner.

```
function ReceiveFrame (
    var destinationParam: AddressValue;
    var sourceParam: AddressValue;
    var lengthOrTypeParam: LengthOrTypeValue;
    var dataParam: DataValue;
    var fcsParamValue: CRCValue;
    var fcsParamPresent: Bit): ReceiveStatus;
function ReceiveDataDecap: ReceiveStatus; {Nested function; see body below}
begin
    if receiveEnabled then
        repeat
```


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```
            ReceiveLinkMgmt;
            ReceiveFrame := ReceiveDataDecap;
          until receiveSucceeding
        else ReceiveFrame := receiveDisabled
    end; {ReceiveFrame}
```

If enabled, ReceiveFrame calls ReceiveLinkMgmt to receive the next valid frame, and then calls the internal function ReceiveDataDecap to return the frame's fields to the MAC client if the frame's address indicates that it should do so. The returned ReceiveStatus indicates the presence or absence of detected transmission errors in the frame.

```
    function ReceiveDataDecap: ReceiveStatus;
‡       var status: ReceiveStatus; {Holds receive status information}
    begin
‡       with incomingFrame do
‡           begin
‡               view := fields;
‡               receiveSucceeding := LayerMgmtRecognizeAddress(destinationField);
                if receiveSucceeding then
                    begin {Disassemble MAC frame}
                        destinationParam := destinationField;
                        sourceParam := sourceField;
                        lengthOrTypeParam := lengthOrTypeField;
                        dataParam := RemovePad(lengthOrTypeField, dataField);
                        fcsParamValue := fcsField;
                        fcsParamPresent := passReceiveFCSMode;
                        exceedsMaxLength := ...; {Check to determine if received MAC frame size exceeds
                                                  maxFrameSizeLimit.
                                                  MAC implementations use maxFrameSizeLimit to
                                                  determine if management counts the frame as too long.
                                                  It is recommended that new implementations support
                                                  maxFrameSizeLimit = maxEnvelopeFrameSize )
                        if exceedsMaxLength then status := frameTooLong
                        else if fcsField = CRC32(incomingFrame) and extensionOK then
‡                               if validLength then status := receiveOK else status := lengthError
‡                       else if excessBits = 0 or not extensionOK then status := frameCheckError
‡                       else status := alignmentError;
‡                       LayerMgmtReceiveCounters(status); {Update receive counters in 5.2.4.3}
                        view := bits
                    end {Disassemble MAC frame}
‡           end; {With incomingFrame}
‡       ReceiveDataDecap := status
    end; {ReceiveDataDecap}

    function LayerMgmtRecognizeAddress(address: AddressValue): Boolean;
    begin
        if {promiscuous receive enabled} then LayerMgmtRecognizeAddress := true;
        if address = ... {MAC station address} then LayerMgmtRecognizeAddress := true;
        if address = ... {Broadcast address} then LayerMgmtRecognizeAddress := true;
        if address = ... {One of the addresses on the multicast list and multicast reception is enabled} then
                                                LayerMgmtRecognizeAddress := true;
        LayerMgmtRecognizeAddress := false
    end; {LayerMgmtRecognizeAddress}
```


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The function RemovePad strips any padding that was generated to meet the minFrameSize constraint, if possible. When the MAC sublayer operates in the mode that enables passing of the frame check sequence field of all received MAC frames to the MAC client (passReceiveFCSMode variable is true), it shall not strip the padding and it shall leave the data field of the MAC frame intact. Length checking is provided for Length interpretations of the Length/Type field. For Length/Type field values in the range between maxBasicDataSize and minTypeValue, the behavior of the RemovePad function is unspecified:

```
function RemovePad(var lengthOrTypeParam: LengthOrTypeValue; dataParam: DataValue): DataValue;
begin
   if lengthOrTypeParam ≥ minTypeValue then
      begin
         validLength := true; {Don't perform length checking for Type interpretation}
         RemovePad := dataParam
      end
   else if lengthOrTypeParam ≤ maxBasicDataSize then
      begin
         validLength := {For length interpretations of the Length/Type field, check to determine if value
                         represented by Length/Type field matches the received clientDataSize};
         if validLength and not passReceiveFCSMode then
            RemovePad := {Truncate the dataParam (when present) to the value represented by the
                          lengthOrTypeParam (in octets) and return the result}
         else RemovePad := dataParam
      end
end; {RemovePad}
```

ReceiveLinkMgmt attempts repeatedly to receive the bits of a frame, discarding any fragments from collisions by comparing them to the minimum valid frame size:

```
procedure ReceiveLinkMgmt;
begin
   repeat
      StartReceive;
      while receiving do nothing; {Wait for frame to finish arriving}
      excessBits := frameSize mod 8;
      frameSize := frameSize – excessBits; {Truncate to octet boundary}
      receiveSucceeding := receiveSucceeding and (frameSize ≥ minFrameSize)
                                                 {Reject collision fragments}
   until receiveSucceeding
end; {ReceiveLinkMgmt}

procedure StartReceive;
begin
   receiveSucceeding := true;
   receiving := true
end; {StartReceive}
```

The BitReceiver process runs asynchronously, receiving bits from the medium at the rate determined by the Physical Layer's ReceiveBit operation, partitioning them into frames, and optionally receiving them:

```
process BitReceiver;
   var   b: PhysicalBit;
         incomingFrameSize: integer; {Count of all bits received in frame including extension}
         frameFinished: Boolean;
         enableBitReceiver: Boolean;
```


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```
        currentReceiveBit: 1..frameSize; {Position of current bit in incomingFrame}
begin
  cycle {Outer loop}
    if receiveEnabled then
      begin {Receive next frame from Physical Layer}
        currentReceiveBit := 1;
        incomingFrameSize := 0;
        frameFinished := false;
        enableBitReceiver := receiving;
        PhysicalSignalDecap; {Skip idle and extension, strip off preamble and sfd}
        if enableBitReceiver then extensionOK := true;
        while receiveDataValid and not frameFinished do
          begin {Inner loop to receive the rest of an incoming frame}
            b := ReceiveBit; {Next bit from physical medium}
            incomingFrameSize := incomingFrameSize + 1;
            if b = 0 or b = 1 then {Normal case}
              if enableBitReceiver then {Append to frame}
              begin
                if incomingFrameSize > currentReceiveBit then extensionOK := false;
                                    {Errors in the extension get mapped to data bits on input}
                incomingFrame[currentReceiveBit] := b;
                currentReceiveBit := currentReceiveBit + 1
              end
            else if not extending then frameFinished := true; {b has to be an extensionBit}
            if incomingFrameSize ≥ slotTime then extending := false
          end; {Inner loop}
        if enableBitReceiver then
          begin
            frameSize := currentReceiveBit – 1;
            receiveSucceeding := not extending;
            receiving := false
          end
      end {Enabled}
  end {Outer loop}
end; {BitReceiver}
```

The bits received from the Physical Layer can take one of three values: data zero (0), data one (1), or extensionBit (EXTEND). The value extensionBit will not occur between the first preamble bit of a frame and the last data bit of a frame in normal circumstances. Extension bits are counted by the BitReceiver but are not appended to the incoming frame. The BitReceiver checks whether the bit received from the Physical Layer is a data bit or an extensionBit before appending it to the incoming frame. Thus, the array of bits in incomingFrame will only contain data bits. The underlying Reconciliation Sublayer (RS) maps incoming EXTEND_ERROR bits to normal data bits. Thus, the reception of additional data bits after the frame extension has started is an indication that the frame should be discarded.

```
procedure PhysicalSignalDecap;
begin
  {Receive one bit at a time from physical medium until a valid sfd is detected, discard bits and return}
end; {PhysicalSignalDecap}
```

The process SetExtending controls the extending variable, which determines whether a received frame has to be at least slotTime bits in length or merely minFrameSize bits in length to be considered valid by the BitReceiver. SetExtending sets the extending variable to true whenever receiveDataValid is de-asserted, while in half duplex mode at an operating speed of 1000 Mb/s:

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```
process SetExtending;
begin
    cycle {Loop forever}
        while receiveDataValid do nothing;
        extending := extend and halfDuplex
    end {Loop}
end; {SetExtending}
```

4.2.10 Common procedures

The function CRC32 is used by both the transmit and receive algorithms to generate a 32-bit CRC value:

```
function CRC32(f: Frame): CRCValue;
begin
    CRC32 := {The 32-bit CRC for the entire frame as defined in 3.2.9, excluding the FCS field (if pres-
             ent)}
end; {CRC32}
```

Purely to enhance readability, the following procedure is also defined:

```
procedure nothing; begin end;
```

The idle state of a process (that is, while waiting for some event) is cast as repeated calls on this procedure.

4.3 Interfaces to/from adjacent layers

4.3.1 Overview

The purpose of this clause is to provide precise definitions of the interfaces between the architectural layers defined in Clause 1 in compliance with the Media Access Service Specification given in Clause 2. In addition, the services required from the physical medium are defined.

The notation used here is the Pascal language, in keeping with the procedural nature of the precise MAC sublayer specification (see 4.2). Each interface is described as a set of procedures or shared variables, or both, that collectively provide the only valid interactions between layers. The accompanying text describes the meaning of each procedure or variable and points out any implicit interactions among them.

Note that the description of the interfaces in Pascal is a notational technique, and in no way implies that they can or should be implemented in software. This point is discussed more fully in 4.2, that provides complete Pascal declarations for the data types used in the remainder of this clause. Note also that the synchronous (one frame at a time) nature of the frame transmission and reception operations is a property of the architectural interface between the MAC client and MAC sublayers, and need not be reflected in the implementation interface between a station and its sublayer.

4.3.2 MAC service

The services provided to the MAC client by the MAC sublayer are transmission and reception of MAC frames using service primitives MA_DATA.request and MA_DATA.indication, as defined in Clause 2. For historical reasons the MAC sublayer definitions use two functions, TransmitFrame and ReceiveFrame, defined in 4.2.8 and 4.2.9. The relationship between these two functions and the service primitives is defined by the MAC client state diagrams in 4.3.2.1 and 4.3.2.2.

The state machines in 4.3.2 follow the conventions in 21.5.

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4.3.2.1 MAC client transmit interface state diagram

4.3.2.1.1 Variables

data
: The value of mac_service_data_unit excluding the first two octets (Length/Type field).

destination_address
: The Destination Address field parsed from the client request.

fcsPresent
: Indicates whether the MA_DATA.request service primitive contained the frame_check_sequence field.

frame_check_sequence
: The fcs field parsed from the client request.

lengthOrType
: The value of the first two octets at the start of the mac_service_data_unit.

mac_service_data_unit
: The concatenation of the lengthOrType field and the data field parsed from the client request.

source_address
: The Source Address field parsed from the client request.

TransmitStatus
: Indicates the status of the transmitted MAC frame. See 4.2.8.

4.3.2.1.2 Functions

TransmitFrame
: The MAC sublayer function invoked to transmit a MAC frame with the specified parameters. See 4.2.8.

4.3.2.1.3 Messages

MA_DATA.request
: The service primitive used to convey a MAC frame to be transmitted from the MAC client. See 2.3.1. The action invoked is not considered to end until the transmission of the frame by the MAC has concluded.

4.3.2.1.4 MAC client transmit interface state diagram

Figure 4–6 specifies the behavior of the transmit interface from the MAC client.

4.3.2.2 MAC client receive interface state diagram

4.3.2.2.1 Variables

destination_address
: The Destination Address field parsed from the received MAC frame.

source_address
: The Source Address field parsed from the received MAC frame.

lengthOrType
: The lengthOrType field parsed from the received MAC frame.

data
: The data payload field parsed from the received MAC frame.

fcsPresent
: A Boolean set by the MAC sublayer.

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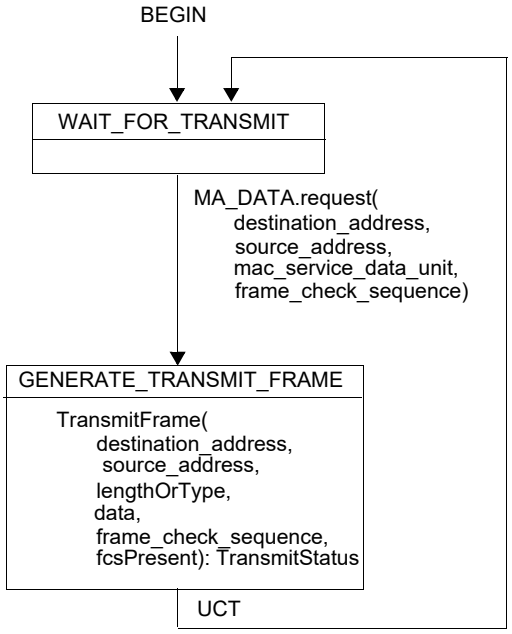

Figure 4–6—MAC client transmit interface state diagram

ReceiveStatus
: Indicates the status of the received MAC frame.

mac_service_data_unit
: The concatenation of the lengthOrType field and the data field parsed from the received MAC frame.

frame_check_sequence
: The fcs field parsed from the received MAC frame.

4.3.2.2.2 Functions

ReceiveFrame
: The MAC sublayer function invoked to accept an incoming MAC frame with the specified parameters. See 4.2.9.

4.3.2.2.3 Messages

MA_DATA.indication
: The service primitive used to transfer an incoming MAC frame to the MAC client with the specified parameters. See 2.3.2.

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4.3.2.2.4 MAC client receive interface state diagram

Figure 4–7 specifies the behavior of the receive interface to the MAC client.

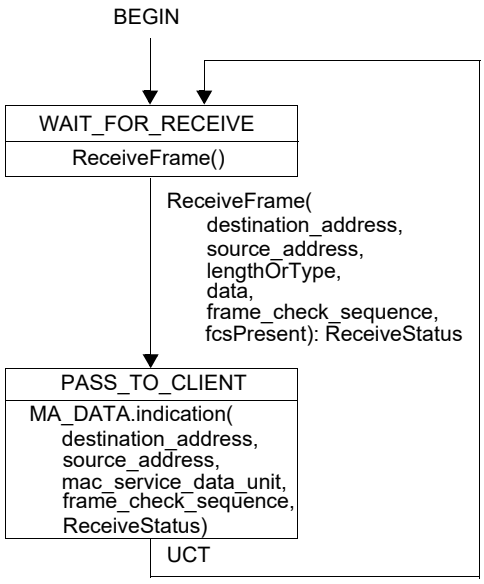

Figure 4–7—MAC client receive interface state diagram

4.3.3 Services required from the Physical Layer

The interface through which the CSMA/CD MAC sublayer uses the facilities of the Physical Layer consists of a function, a pair of procedures and four Boolean variables:

Table 4–1—Physical Layer interface

Function	Procedures	Variables
ReceiveBit	TransmitBit Wait	collisionDetect carrierSense receiveDataValid transmitting

During transmission, the contents of an outgoing frame are passed from the MAC sublayer to the Physical Layer by way of repeated use of the TransmitBit operation:

procedure TransmitBit (bitParam: PhysicalBit);

Each invocation of TransmitBit passes one new bit of the outgoing frame to the Physical Layer. The TransmitBit operation is synchronous. The duration of the operation is the entire transmission of the bit. The operation completes, when the Physical Layer is ready to accept the next bit and it transfers control to the MAC sublayer.

The overall event of data being transmitted is signaled to the Physical Layer by way of the variable transmitting:

var transmitting: Boolean*;*

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Before sending the first bit of a frame, the MAC sublayer sets transmitting to true, to inform the Physical Media Access that a stream of bits will be presented via the TransmitBit operation. After the last bit of the frame has been presented, the MAC sublayer sets transmitting to false to indicate the end of the frame.

The presence of a collision in the physical medium is signaled to the MAC sublayer by the variable collisionDetect:

var collisionDetect: Boolean*;*

The collisionDetect signal remains true during the duration of the collision.

NOTE—In full duplex mode, collision indications may still be generated by the Physical Layer; however, they are ignored by the full duplex MAC.

The collisionDetect signal is generated only during transmission and is never true at any other time; in particular, it cannot be used during frame reception to detect collisions between overlapping transmissions from two or more other stations.

During reception, the contents of an incoming frame are retrieved from the Physical Layer by the MAC sublayer via repeated use of the ReceiveBit operation:

function ReceiveBit: PhysicalBit;

Each invocation of ReceiveBit retrieves one new bit of the incoming frame from the Physical Layer. The ReceiveBit operation is synchronous. Its duration is the entire reception of a single bit. Upon receiving a bit, the MAC sublayer shall immediately request the next bit until all bits of the frame have been received. (See 4.2 for details.)

The overall event of data being received is signaled to the MAC sublayer by the variable receiveDataValid:

var receiveDataValid: Boolean*;*

When the Physical Layer sets receiveDataValid to true, the MAC sublayer shall immediately begin retrieving the incoming bits by the ReceiveBit operation. When receiveDataValid subsequently becomes false, the MAC sublayer can begin processing the received bits as a completed frame. If an invocation of ReceiveBit is pending when receiveDataValid becomes false, ReceiveBit returns an undefined value, which should be discarded by the MAC sublayer. (See 4.2 for details.)

NOTE—When a burst of frames is received in half duplex mode at an operating speed of 1000 Mb/s, the variable receiveDataValid will remain true throughout the burst. Furthermore, the variable receiveDataValid remains true throughout the extension field. In these respects, the behavior of the variable receiveDataValid is different from the underlying GMII signal RX_DV, from which it may be derived. See 35.2.1.7.

The overall event of activity on the physical medium is signaled to the MAC sublayer by the variable carrierSense:

var carrierSense: Boolean*;*

In half duplex mode, the MAC sublayer shall monitor the value of carrierSense to defer its own transmissions when the medium is busy. The Physical Layer sets carrierSense to true immediately upon detection of activity on the physical medium. After the activity on the physical medium ceases, carrierSense is set to false. Note that the true/false transitions of carrierSense are not defined to be precisely synchronized with the beginning and the end of the frame, but may precede the beginning and lag the end, respectively. (See 4.2 for details.) In full duplex mode, carrierSense is undefined.

The Physical Layer also provides the procedure Wait:

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procedure Wait (bitTimes: integer)*;*

This procedure waits for the specified number of bit times. This allows the MAC sublayer to measure time intervals in units of the (physical-medium-dependent) bit time.

Another important property of the Physical Layer, which is an implicit part of the interface presented to the MAC sublayer, is the round-trip propagation time of the physical medium. Its value represents the maximum time required for a signal to propagate from one end of the network to the other, and for a collision to propagate back. The round-trip propagation time is primarily (but not entirely) a function of the physical size of the network. The round-trip propagation time of the Physical Layer is defined in 4.4 for a selection of physical media.

4.4 Specific implementations

4.4.1 Compatibility overview

To provide total compatibility at all levels of the standard, it is required that each network component implementing the CSMA/CD MAC sublayer procedure adheres rigidly to these specifications. The information provided in 4.4.2 provides design parameters for specific implementations of this access method. Variations from these values result in a system implementation that violates the standard.

A DTE shall be capable of operating in half duplex mode, full duplex mode, or both. In any given instantiation of a network conforming to this standard, all stations shall be configured to use the same mode of operation, either half duplex or full duplex.

All DTEs connected to a repeater or a mixing segment shall be configured to use the half duplex mode of operation. When a pair of DTEs are connected to each other with a link segment, both devices shall be configured to use the same mode of operation, either half duplex or full duplex.

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4.4.2 MAC parameters

The parameter values shown in Table 4–2 shall be used for their corresponding MAC data rate.

Table 4–2—MAC parameters

Parameters	MAC data rate			
	Up to and including 100 Mb/s	**1 Gb/s**	**2.5 Gb/s, 5 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s**	**10 Gb/s**
slotTime	512 bit times	4096 bit times	not applicable	not applicable
interPacketGap[a]	96 bits	96 bits	96 bits	96 bits
attemptLimit	16	16	not applicable	not applicable
backoffLimit	10	10	not applicable	not applicable
jamSize	32 bits	32 bits	not applicable	not applicable
maxBasicFrameSize	1518 octets	1518 octets	1518 octets	1518 octets
maxEnvelopeFrameSize	2000 octets	2000 octets	2000 octets	2000 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	not applicable	not applicable
ipgStretchRatio	not applicable	not applicable	not applicable	104 bits

[a]References to interFrameGap or interFrameSpacing in other clauses (e.g., Clause 13, Clause 35, and Clause 42) shall be interpreted as interPacketGap.

NOTE 1—For 10 Mb/s operation, the spacing between two successive non-colliding packets, from start of idle at the end of the first packet to start of Preamble of the subsequent packet, can have a minimum value of 47 BT (bit times), at the AUI receive line of the DTE. This interpacket gap shrinkage is caused by variable network delays, added preamble bits, and clock skew.

NOTE 2—For 1BASE-5operation, see also DTE Deference Delay in 12.9.2.

NOTE 3—For 1 Gb/s operation, the spacing between two non-colliding packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet, can have a minimum value of 64 BT (bit times), as measured at the GMII receive signals at the DTE. This interpacket gap shrinkage may be caused by variable network delays, added preamble bits, and clock tolerances.

NOTE 4—For 2.5 Gb/s, 5 Gb/s, 10 Gb/s, and 25 Gb/s operation, the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet, can have a minimum value of 40 BT (bit times), as measured at the XGMII or 25GMII receive signals at the DTE. This interpacket gap shrinkage may be caused by variable network delays and clock tolerances.

NOTE 5—For 10 Gb/s operation, the value of ipgStretchRatio of 104 bits adapts the average data rate of the MAC sublayer to SONET/SDH STS-192 data rate (with frame granularity), for WAN-compatible applications of this standard.

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NOTE 6—For 10 Mb/s half-duplex operation, the use of envelope frames is not recommended for use with repeaters, as described in Clause 9, as a result of possible frame corruption due to clock skew.

NOTE 7—For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s operation, the received interpacket gap (the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet) can have a minimum value of 8 BT (bit times), as measured at the XLGMII, 50GMII, CGMII, 200GMII, or 400GMII receive signals at the DTE due to clock tolerance and lane alignment requirements.

WARNING

Any deviation from the above specified values may affect proper operation of the network.

4.4.3 Configuration guidelines

The operational mode of the MAC may be determined either by the Auto-Negotiation functions specified in Clause 28 and Clause 37, or through manual configuration. When manual configuration is used, the devices on both ends of a link segment have to be configured to matching modes to ensure proper operation. When Auto-Negotiation is used, the MAC has to be configured to the mode determined by Auto-Negotiation before assuming normal operation.

NOTE—Improper configuration of duplex modes may result in improper network behavior.

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5. Layer Management

All parts of Clause 5, except for 5.2.4 and its subclauses, are deprecated by Clause 30.

5.1 Introduction

This clause provides the Layer Management specification for DTEs based on the CSMA/CD access method. It defines facilities composed of a set of statistics and actions needed to provide Layer Management services. The information in this clause should be used in conjunction with the Procedural Model defined in 4.2.7 to 4.2.10. The Procedural Model provides a formal description of the relationship between the CSMA/CD Layer Entities and the Layer Management facilities.

This Layer Management specification has been developed in accordance with the OSI management architecture as specified in the ISO Management Framework document, ISO/IEC 7498-4:1989. It is independent of any particular management application or management protocol.

The management facilities defined in this standard may be accessed both locally and remotely. Thus, the Layer Management specification provides facilities that can be accessed from within a station or can be accessed remotely by means of a peer management protocol operating between application entities.

In CSMA/CD no peer management facilities are necessary for initiating or terminating normal protocol operations or for handling abnormal protocol conditions. The monitoring of these activities is done by the carrier sense and collision detection mechanisms. Since these activities are necessary for normal operation of the protocol, they are not considered to be a function of Layer Management and are therefore not discussed in this clause.

Implementation of DTE Management is not a requirement for conformance to Clause 4 and Clause 7.

5.1.1 Systems Management overview

Within the ISO/IEC Open Systems Interconnection (OSI) architecture, the need to handle the special problems of initializing, terminating, and monitoring ongoing activities and assisting in their harmonious operations, as well as handling abnormal conditions, is recognized. These needs are collectively addressed by the systems management component of the OSI architecture.

A Management Protocol is required for the exchange of information between systems on a network. This Layer Management clause is independent of any particular Management Protocol.

This Layer Management clause, in conjunction with the Layer Management standards of other layers, provides the means to perform various management functions. Layer Management collects information needed from the MAC and Physical Layers. It also provides a means to exercise control over those layers.

The relationship between the various management entities and the layer entities according to the ISO model is shown in Figure 19–1.

5.1.2 Layer Management model

The Layer Management facilities provided by the CSMA/CD MAC and Physical Layer management definitions provide the ability to manipulate management counters and initiate actions within the layers.

The managed objects within this standard are defined as sets of attributes, actions, notifications, and behaviors in accordance with IEEE Std 802-2001 and ISO/IEC International Standards for network management.

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The precise semantics of the relationship between the CSMA/CD Layer Entities and the Layer Management facilities are defined in 4.2.7 to 4.2.10 and in 5.2.4.

5.1.3 Packages

This standard and ISO/IEC guidelines make provision for grouping attributes, operations and notifications in implementation groups or "packages" within each managed object class. DTE Management has two packages that are required for management at the minimum conformance configuration. The basic package is also useful for system configurations that wish to implement MAU Management without DTE Management. The packages for DTE Management are specified in Table 1.

5.1.4 Conformance requirements

Implementation of both the basic and the mandatory package of the MAC entity are the minimum requirements for claiming conformance to DTE Management.

5.2 Management facilities

5.2.1 Introduction

This subclause of the standard defines the Layer Management facilities for the Ethernet MAC and Physical Layers. The intent of this subclause is to furnish a management specification that can be used by the wide variety of different DTE devices that may be attached to a network specified by this standard. Thus, a comprehensive list of management facilities is provided.

The improper use of some of the facilities described in this subclause may cause serious disruption of the network. In accordance with ISO management architecture, any necessary security provisions should be provided by the Agent in the Local System Environment. This can be in the form of specific security features or in the form of security features provided by the peer communication facilities.

All counters defined in this specification are assumed to be wraparound counters. Wraparound counters are those that automatically go from their maximum value (or final value) to zero and continue to operate. These unsigned counters do not provide for any explicit means to return them to their minimum (zero), i.e., reset. Because of their nature, wraparound counters should be read frequently enough to avoid loss of information.

5.2.2 DTE MAC Sublayer Management facilities

This subclause defines the Layer Management facilities specific to the MAC sublayer Managed Object Class. Note that with regard to reception-related error statistics, a hierarchical order has been established such that when multiple error statuses can be associated with one frame, only one status is returned to the MAC client. This hierarchy in descending order is as follows:

frameTooLong

alignmentError

frameCheckError

lengthError

The counters are primarily incremented based on the status returned to the MAC client, and therefore the hierarchical order of the counters is determined by the order of the status. Frame fragments are not included

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in any of the statistics unless otherwise stated. In implementing any of the specified actions, receptions and transmissions that are in progress are completed before the action takes effect.

Table 5-1—Packages

			Basic Package (Mandatory)	Mandatory Package (Mandatory)	Recommended Package (Optional)	Optional Package (Optional)	Array Package (Optional)	Excessive Deferral Package (Optional)
oMAC-entity managed object class								
aMACID	ATTRIBUTE	GET	X					
aFramesTransmittedOK	ATTRIBUTE	GET			X			
aSingleCollisionFrames	ATTRIBUTE	GET			X			
aMultipleCollisionFrames	ATTRIBUTE	GET			X			
aFramesReceivedOK	ATTRIBUTE	GET			X			
aFrameCheckSequenceErrors	ATTRIBUTE	GET			X			
aAlignmentErrors	ATTRIBUTE	GET			X			
acInitializeMAC	ACTION		X					
aOctetsTransmittedOK	ATTRIBUTE	GET				X		
aFramesWithDeferredXmissions	ATTRIBUTE	GET				X		
aLateCollisions	ATTRIBUTE	GET				X		
aFramesAbortedDueToXSColls	ATTRIBUTE	GET				X		
aFramesLostDueToIntMACXmitError	ATTRIBUTE	GET				X		
aCarrierSenseErrors	ATTRIBUTE	GET				X		
aOctetsReceivedOK	ATTRIBUTE	GET				X		
aFramesLostDueToIntMACRcvError	ATTRIBUTE	GET				X		
aPromiscuousStatus	ATTRIBUTE	GET-SET				X		
aReadMulticastAddressList	ATTRIBUTE	GET				X		
acAddGroupAddress	ACTION					X		
acDeleteGroupAddress	ACTION					X		
aMulticastFramesXmittedOK	ATTRIBUTE	GET					X	
aBroadcastFramesXmittedOK	ATTRIBUTE	GET					X	
aFramesWithExcessiveDeferral	ATTRIBUTE	GET						X
aMulticastFramesReceivedOK	ATTRIBUTE	GET					X	
aBroadcastFramesReceivedOK	ATTRIBUTE	GET					X	
aInRangeLengthErrors	ATTRIBUTE	GET					X	
aOutOfRangeLengthField	ATTRIBUTE	GET					X	
aFrameTooLongErrors	ATTRIBUTE	GET					X	
aMACEnableStatus	ATTRIBUTE	GET-SET					X	
aTransmitEnableStatus	ATTRIBUTE	GET-SET					X	
aMulticastReceiveStatus	ATTRIBUTE	GET-SET					X	
aReadWriteMACAddress	ATTRIBUTE	GET-SET					X	
acExecuteSelfTest	ACTION						X	
aCollisionFrames	ATTRIBUTE	GET						X
oResourceTypeID managed object class								
aResourceTypeIDName	ATTRIBUTE	GET	X					
aResourceInfo	ATTRIBUTE	GET	X					
oPHY-entity managed object class								
aPHYID	ATTRIBUTE	GET				X		
aSQETestErrors	ATTRIBUTE	GET				X		

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5.2.2.1 DTE MAC sublayer attributes

5.2.2.1.1 aMACID

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The value of aMACID is assigned so as to uniquely identify a MAC among the subordinate managed objects of the containing object.

5.2.2.1.2 aFramesTransmittedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are successfully transmitted. This counter is incremented when the TransmitStatus is reported as transmitOK. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.3 aSingleCollisionFrames

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 13 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are involved in a single collision and are subsequently transmitted successfully. This counter is incremented when the result of a transmission is reported as transmitOK and the attempt value is 2. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.4 aMultipleCollisionFrames

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 11 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are involved in more than one collision and are subsequently transmitted successfully. This counter is incremented when the TransmitStatus is reported as transmitOK and the value of the attempts variable is greater than 2 and less or equal to attemptLimit. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

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5.2.2.1.5 aFramesReceivedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are successfully received (receiveOK). This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented when the ReceiveStatus is reported as receiveOK. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.6 aFrameCheckSequenceErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are an integral number of octets in length and do not pass the FCS check. This counter is incremented when the ReceiveStatus is reported as frameCheckError. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.7 aAlignmentErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are not an integral number of octets in length and do not pass the FCS check. This counter is incremented when the ReceiveStatus is reported as alignmentError. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.8 aOctetsTransmittedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 1 230 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of data and padding octets of frames that are successfully transmitted. This counter is incremented when the TransmitStatus is reported as transmitOK. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

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5.2.2.1.9 aFramesWithDeferredXmissions

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 13 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames whose transmission was delayed on its first attempt because the medium was busy. This counter is incremented when the boolean variable deferred has been asserted by the TransmitLinkMgmt function (4.2.8). Frames involved in any collisions are not counted. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.10 aLateCollisions

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of the times that a collision has been detected later than 512 bit times into the transmitted packet. A late collision is counted twice, i.e., both as a collision and as a lateCollision. This counter is incremented when the lateCollisionCount variable is nonzero. The actual update is incremented in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.11 aFramesAbortedDueToXSColls

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 3255 counts per second.
BEHAVIOUR DEFINED AS:
A count of the frames that due to excessive collisions are not transmitted successfully. This counter is incremented when the value of the attempts variable equals attemptLimit during a transmission. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.12 aFramesLostDueToIntMACXmitError

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 75 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that would otherwise be transmitted by the station, but could not be sent due to an internal MAC sublayer transmit error. If this counter is incremented, then none of the other counters in this subclause are incremented. The exact meaning and mechanism for incrementing this counter is implementation dependent.

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5.2.2.1.13 aCarrierSenseErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of times that the carrierSense variable was not asserted or was deasserted during the transmission of a frame without collision (see 7.2.4.6). This counter is incremented when the carrierSenseFailure flag is true at the end of transmission. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.14 aOctetsReceivedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 1 230 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of data and padding octets in frames that are successfully received. This does not include octets in frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented when the result of a reception is reported as a receiveOK status. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.15 aFramesLostDueToIntMACRcvError

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that would otherwise be received by the station, but could not be accepted due to an internal MAC sublayer receive error. If this counter is incremented, then none of the other counters in this subclause are incremented. The exact meaning and mechanism for incrementing this counter is implementation dependent.

5.2.2.1.16 aPromiscuousStatus

ATTRIBUTE
APPROPRIATE SYNTAX:
BOOLEAN
BEHAVIOUR DEFINED AS:
A GET operation returns the value true for promiscuous mode enabled, and false otherwise.
Frames without errors received solely because this attribute has the value true are counted as frames received correctly; frames received in this mode that do contain errors update the appropriate error counters.
A SET operation to the value true provides a means to cause the LayerMgmtRecognizeAddress function to accept frames regardless of their destination address.

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A SET operation to the value false causes the MAC sublayer to return to the normal operation of carrying out address recognition procedures for station, broadcast, and multicast group addresses (LayerMgmtRecognizeAddress function).;

5.2.2.1.17 aReadMulticastAddressList

ATTRIBUTE
APPROPRIATE SYNTAX:
Sequence of MAC addresses.
BEHAVIOUR DEFINED AS:
Return the current multicast address list.;

5.2.2.1.18 aMulticastFramesXmittedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are successfully transmitted, as indicated by the status value transmitOK, to a group destination address other than broadcast. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.19 aBroadcastFramesXmittedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of the frames that were successfully transmitted, as indicated by the TransmitStatus transmitOK, to the broadcast address. Frames transmitted to multicast addresses are not broadcast frames and are excluded. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.20 aFramesWithExcessiveDeferral

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 412 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that deferred for an excessive period of time. This counter may only be incremented once per MAC client sublayer transmission. This counter is incremented when the excessDefer flag is set. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

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5.2.2.1.21 aMulticastFramesReceivedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are successfully received and are directed to an active nonbroadcast group address. This does not include frames received with frame-too-long, FCS, length, or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.22 aBroadcastFramesReceivedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are successfully received and are directed to the broadcast group address. This does not include frames received with frame-too-long, FCS, length, or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.23 aInRangeLengthErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames with a length field value between the minimum unpadded LLC data size and the maximum allowed LLC data size, inclusive, that does not match the number of LLC data octets received. The counter also contains frames with a length field value less than the minimum unpadded LLC data size. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.24 aOutOfRangeLengthField

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames with a length field value greater than the maximum allowed LLC data size. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

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5.2.2.1.25 aFrameTooLongErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 815 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are received and exceed the maximum permitted frame size. This counter is incremented when the status of a frame reception is frameTooLong. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.26 aMACEnableStatus

ATTRIBUTE
APPROPRIATE SYNTAX:
BOOLEAN
BEHAVIOUR DEFINED AS:
True if MAC sublayer is enabled, and false if disabled. This is accomplished by setting or checking the values of the receiveEnabled and transmitEnabled variables.;
Setting to true provides a means to cause the MAC sublayer to enter the normal operational state at idle. The PLS is reset by this operation (see 7.2.2.2.1). This is accomplished by setting receiveEnabled and transmitEnabled to true.
Setting to false causes the MAC sublayer to end all transmit and receive operations, leaving it in a disabled state. This is accomplished by setting receiveEnabled and transmitEnabled to false.

5.2.2.1.27 aTransmitEnableStatus

ATTRIBUTE
APPROPRIATE SYNTAX:
BOOLEAN
BEHAVIOUR DEFINED AS:
True if transmission is enabled, and false otherwise. This is accomplished by setting or checking the value of the transmitEnabled variable.
Setting this to true provides a means to enable MAC sublayer frame transmission (TransmitFrame function). This is accomplished by setting transmitEnabled to true.
Setting this to false will inhibit the transmission of further frames by the MAC sublayer (TransmitFrame function). This is accomplished by setting transmitEnabled to false.

5.2.2.1.28 aMulticastReceiveStatus

ATTRIBUTE
APPROPRIATE SYNTAX:
BOOLEAN
BEHAVIOUR DEFINED AS:
True if multicast receive is enabled, and false otherwise.;
Setting this to true provides a means to cause the MAC sublayer to return to the normal operation of multicast frame reception.

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Setting this to false will inhibit the reception of further multicast frames by the MAC sublayer.

5.2.2.1.29 aReadWriteMACAddress

ATTRIBUTE
APPROPRIATE SYNTAX:
MACAddress
BEHAVIOUR DEFINED AS:
Read the MAC station address or change the MAC station address to the one supplied (RecognizeAddress function). Note that the supplied station address shall not have the group bit set and shall not be the null address.

5.2.2.1.30 aCollisionFrames

ATTRIBUTE
APPROPRIATE SYNTAX:
A SEQUENCE of 32 generalized nonresetable counters. Each counter has a maximum increment rate of 13 000 counts per second.
BEHAVIOUR DEFINED AS:
A histogram of collision activity. The indices of this array (1 to attemptLimit–1) denote the number of collisions experienced in transmitting a frame. Each element of this array contains a counter that denotes the number of frames that have experienced a specific number of collisions. When the TransmitStatus is reported as transmitOK and the value of the attempts variable equals n, then collisionFrames[n–1] counter is incremented. The elements of this array are incremented in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.2 DTE MAC Sublayer actions

5.2.2.2.1 acInitializeMAC

ACTION
APPROPRIATE SYNTAX:
None required
BEHAVIOUR DEFINED AS:
This action provides a means to call the Initialize procedure (4.2.7.4). This action also results in the initialization of the PLS.

5.2.2.2.2 acAddGroupAddress

ACTION
APPROPRIATE SYNTAX:
MACAddress
BEHAVIOUR DEFINED AS:
Add the supplied multicast group address to the address recognition filter (RecognizeAddress function).

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5.2.2.2.3 acDeleteGroupAddress

ACTION
APPROPRIATE SYNTAX:
MACAddress
BEHAVIOUR DEFINED AS:
Delete the supplied multicast group address from the address recognition filter (RecognizeAddress function).

5.2.2.2.4 acExecuteSelfTest

ACTION
APPROPRIATE SYNTAX:
None required
BEHAVIOUR DEFINED AS:
Execute a self-test and report the results (success or failure). The actual mechanism employed to carry out the self-test is not defined in this standard.

5.2.2.3 ResourceTypeID Managed Object Class

5.2.2.3.1 ResourceTypeID

Implementation of this managed object in accordance with the definition contained in IEEE Std 802.1F-1993 is a conformance requirement of this standard. A single instance of the Resource Type ID managed object exists within the DTE–MAC managed object class. The managed object itself is contained in IEEE Std 802.1F-1993; therefore, only the name binding appears in this standard.

5.2.3 DTE Physical Sublayer Management facilities

This subclause defines the Layer Management facilities specific to the Physical Layer Signaling (PLS) sublayer Managed Object Class. The PLS is required to be within a managed CSMA/CD port of a DTE. Management of that portion of the physical sublayer whose physical containment within the DTE is optional is outside the scope of this subclause.

5.2.3.1 DTE Physical Sublayer attributes

5.2.3.1.1 aPHYID

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The value of aPHYID is assigned so as to uniquely identify a PHY, i.e., Physical Layer among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2:1992).;

5.2.3.1.2 aSQETestErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 16 000 counts per second.

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BEHAVIOUR DEFINED AS:

A count of times that the SQE_TEST_ERROR was received. The SQE_TEST_ERROR is set in accordance with the rules for verification of the SQE detection mechanism in the PLS Carrier Sense Function (see 7.2.4.6).

5.2.4 DTE Management procedural model

The following model provides the descriptions for Layer Management facilities.

5.2.4.1 Common constants and types

The following are the common constants and types required for the Layer Management procedures:

const

maxDeferTime = …; {2 × (maxBasicFrameSize × 8), for operating speeds of 100 Mb/s and below, and 2 × (burstLimit + maxBasicFrameSize × 8 + headerSize) for operating speeds greater than 100 Mb/s, in bits, error timer limit for maxDeferTime}

type

CounterLarge = 0..maxLarge; {see footnote[36]}.

5.2.4.2 Transmit variables and procedures

The following items are specific to frame transmission:

var

excessDefer: Boolean; {set in process DeferTest}
carrierSenseFailure: Boolean; {set in process CarrierSenseTest}
transmitEnabled: Boolean; {set by MAC action}
lateCollisionError: Boolean; {set in Section 4 procedure WatchForCollision}
deferred: Boolean; {set in Section 4 function TransmitLinkMgmt}
carrierSenseTestDone: Boolean; {set in process CarrierSenseTest}
lateCollisionCount: 0..attemptLimit – 1; {count of late collision that is used in Clause 4 TransmitLinkMgmt and BitTransmitter}
{MAC transmit counters}
framesTransmittedOK: CounterLarge; {mandatory}
singleCollisionFrames: CounterLarge; {mandatory}
multipleCollisionFrames: CounterLarge; {mandatory}
collisionFrames: array [1..attemptLimit – 1] of CounterLarge; {recommended}
octetsTransmittedOK: CounterLarge; {recommended}
deferredTransmissions: CounterLarge; {recommended}
multicastFramesTransmittedOK: CounterLarge; {optional}
broadcastFramesTransmittedOK: CounterLarge; {optional}
{MAC transmit error counters}
lateCollision: CounterLarge; {recommended}
excessiveCollision: CounterLarge; {recommended}
carrierSenseErrors: CounterLarge; {optional}
excessiveDeferral: CounterLarge; {optional}
halfDuplex: Boolean; {Indicates the desired mode. halfDuplex is a static variable; its value does not change between invocations of the Initialize procedure}

[36]The CounterLarge declaration is an example of how to declare a counter. This particular example produces a 32 bit counter.

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Procedure LayerMgmtTransmitCounters is invoked from the TransmitLinkMgmt function and from the BitTransmitter process in 4.2.8 to update the transmit and transmit error counters.

```
procedure LayerMgmtTransmitCounters;
begin
   if halfDuplex then
      while not carrierSenseTestDone do nothing;
   if transmitSucceeding then
   begin
      IncLargeCounter(framesTransmittedOK);
      SumLarge(octetsTransmittedOK, dataSize/8); {dataSize (in bits) is defined in 4.2.7.1}
      if destinationField = … {check to see if to a multicast destination}
         then IncLargeCounter(multicastFramesTransmittedOK);
      if destinationField = … {check to see if to a broadcast destination}
         then IncLargeCounter(broadcastFramesTransmittedOK);

      if attempts > 1 then
      begin {transmission delayed by collision}
         if attempts = 2 then
            IncLargeCounter(singleCollisionFrames) {delay by 1 collision}
         else {attempts > 2, delayed by multiple collisions}
            IncLargeCounter(multipleCollisionFrames)
         IncLargeCounter(collisionFrames[attempts – 1])
      end {delay by collision}
   end; {transmitSucceeding}

   if deferred and (attempts = 1) then
      IncLargeCounter(deferredTransmissions);
   if lateCollisionCount > 0 then {test if late collision detected}
      SumLarge(lateCollision, lateCollisionCount);
   if attempts = attemptLimit and not transmitSucceeding then
      IncLargeCounter(excessiveCollision);
   if carrierSenseFailure then
      IncLargeCounter(carrierSenseErrors);
   if excessDefer then
      IncLargeCounter(excessiveDeferral)
end; {LayerMgmtTransmitCounters}
```

The DeferTest process sets the excessDefer flag if a transmission attempt has been deferred for a period of time longer than maxDeferTime.

```
process DeferTest;
   var deferBitTimer: 0..maxDeferTime;
begin
   cycle
   begin
      deferBitTimer := 0;
      while frameWaiting and not excessDefer do
      begin
         Wait(oneBitTime); {see 4.3.3}
         if deferBitTimer = maxDeferTime then
            excessDefer := true
         else
            deferBitTimer := deferBitTimer + 1
```


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```
        end; {while}
        while transmitting do nothing
    end {cycle}
end; {DeferTest}
```

The CarrierSenseTest process sets the carrierSenseFailure flag if carrier sense disappears while transmitting or if it never appears during an entire transmission.

```
process CarrierSenseTest;
    var
        carrierSeen: Boolean; {Running indicator of whether or not carrierSense has been true at any
                                time during the current transmission}
        collisionSeen: Boolean; {Running indicator of whether or not the collisionDetect asserted any
                                time during the entire transmission}
begin
    cycle {main loop}
        while not transmitting do nothing; {wait for start of transmission}
        carrierSenseFailure := false;
        carrierSeen := false;
        collisionSeen := false;
        carrierSenseTestDone := false;
        while transmitting do
        begin {inner loop}
            if carrierSense then
                carrierSeen := true;
            else
                if carrierSeen then {carrierSense disappeared before end of transmission}
                    carrierSenseFailure := true;
            if collisionDetect then
                collisionSeen := true
        end; {inner loop}
        if not carrierSeen then
            carrierSenseFailure := true {carrier sense never appeared}
        else
            if collisionSeen then
                carrierSenseFailure := false;
        carrierSenseTestDone := true
    end {main loop}
end; {CarrierSenseTest}
```

5.2.4.3 Receive variables and procedures

The following items are specific to frame reception:

```
var
    receiveEnabled: Boolean; {set by MAC action}
    {MAC receive counters}
    framesReceivedOK: CounterLarge; {mandatory}
    octetsReceivedOK: CounterLarge; {recommended}

    {MAC receive error counters}
    frameCheckSequenceErrors: CounterLarge; {mandatory}
    alignmentErrors: CounterLarge; {mandatory}
    inRangeLengthErrors: CounterLarge; {optional}
```


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```
    outOfRangeLengthField: CounterLarge; {optional}
    frameTooLongErrors: CounterLarge; {optional}

    {MAC receive address counters}
    multicastFramesReceivedOK: CounterLarge; {optional}
    broadcastFramesReceivedOK: CounterLarge; {optional}
```

Procedure LayerMgmtReceiveCounters is called by the ReceiveDataDecap function in 4.2.9 and increments the appropriate receive counters.

```
procedure LayerMgmtReceiveCounters (status: ReceiveStatus);
begin
  case status of
    receiveDisabled:
    begin
      nothing
    end; {receiveDisabled}
    receiveOK:
    begin
      IncLargeCounter(framesReceivedOK);
      SumLarge(octetsReceivedOK, dataSize/8); {dataSize (in bits) is defined in 4.2.7.1}
      if destinationField = … {check to see if to a multicast destination}
        then IncLargeCounter(multicastFramesReceivedOK);
      if destinationField = … {check to see if to a broadcast destination}
        then IncLargeCounter(broadcastFramesReceivedOK)
    end; {receiveOK}
    frameTooLong:
    begin
      IncLargeCounter(frameTooLongErrors)
    end; {frameTooLong}
    frameCheckError:
    begin
      IncLargeCounter(frameCheckSequenceErrors)
    end; {frameCheckError}
    alignmentError:
    begin
      IncLargeCounter(alignmentErrors)
    end; {alignmentError}
    lengthError: {Note that ReceiveStatus is never lengthError for a type interpretation of the
                  Length/Type field. See 4.2.9}
    begin
      if {Length/Type field value is between the minimum MAC client data size that does not
        require padding and maxBasicDataSize inclusive, and does not match the number of data
        octets received} or {Length/Type field value is less than the minimum allowed MAC
        client data size that does not require padding and the number of MAC client data octets
        received is greater than the minimum MAC client data size that does not
        require padding}
        then
        IncLargeCounter(inRangeLengthErrors);
      if {Length/Type field value is greater than maxBasicDataSize} then
        IncLargeCounter(outOfRangeLengthField)
    end {lengthError}
  end {case status}
end; {LayerMgmtReceiveCounters}
```


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Function LayerMgmtRecognizeAddress checks if reception of certain addressing types has been enabled. Note that in Pascal, assignment to a function causes the function to return immediately.

```
function LayerMgmtRecognizeAddress(address: AddressValue): Boolean;
begin
   if {promiscuous receive enabled} then
      LayerMgmtRecognizeAddress := true;
   if address = … {MAC station address} then
      LayerMgmtRecognizeAddress := true;
   if address = … {broadcast address} then
      LayerMgmtRecognizeAddress := true;
   if address = … {one of the addresses on the multicast list and multicast reception is enabled} then
      LayerMgmtRecognizeAddress := true;
   LayerMgmtRecognizeAddress := false
end; {LayerMgmtRecognizeAddress}
```

5.2.4.4 Common procedures

Procedure LayerMgmtInitialize initializes all the variables and constants required to implement Layer Management.

```
procedure LayerMgmtInitialize;
begin
   {initialize flags for enabling/disabling transmission and reception}
   receiveEnabled := true;
   transmitEnabled := true;
   {initialize transmit flags for DeferTest and CarrierSenseTest}
   deferred := false;
   lateCollisionError := false;
   excessDefer := false;
   carrierSenseFailure := false;
   carrierSenseTestDone := false

   {Initialize all MAC sublayer management counters to zero}

end; {LayerMgmtInitialize}
```

Procedure IncLargeCounter increments a 32-bit wraparound counter.

```
procedure IncLargeCounter (var counter: CounterLarge);
begin
   {increment the 32-bit counter}
end; {IncLargeCounter}
```

Procedure SumLarge adds a value to a 32-bit wraparound counter.

```
procedure SumLarge (
   var counter: CounterLarge;
   var offset: Integer);
begin
   {add offset to the 32-bit counter}
end; {SumLarge}
```


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6. Physical Signaling (PLS) service specifications

6.1 Scope and field of application

This clause specifies the services provided by the PLS sublayer to the MAC sublayer for 1 Mb/s and 10 Mb/s implementations of this standard (see Figure 6–1). The services are described in an abstract way and do not imply any particular implementation.

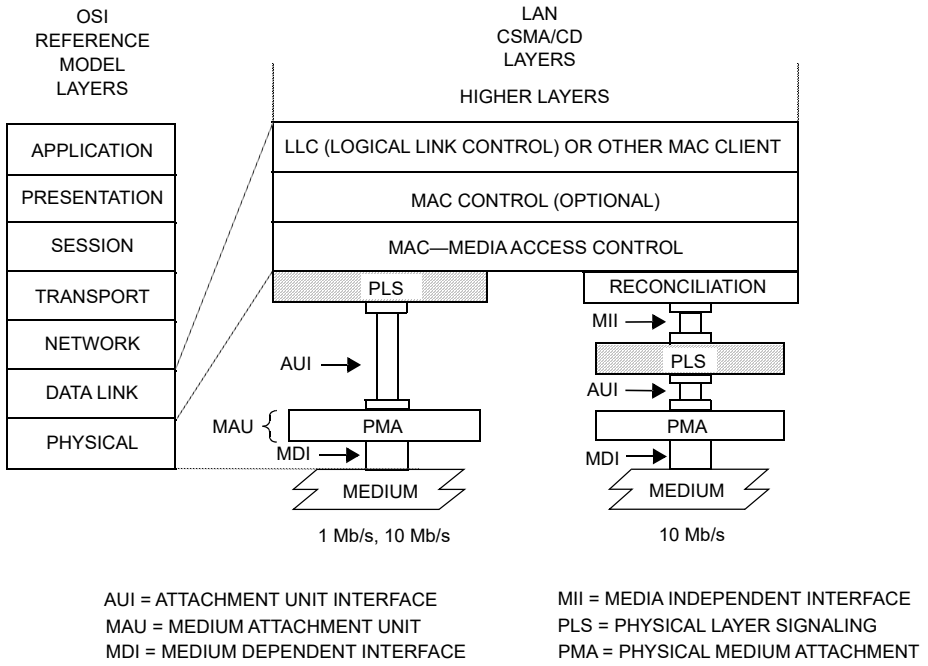

Figure 6–1—PLS service specification relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

6.2 Overview of the service

6.2.1 General description of services provided by the layer

The services provided by the PLS sublayer allow the local MAC sublayer entity to exchange data bits (PLS data_units) with peer MAC sublayer entities.

6.2.2 Model used for the service specification

The model used in this service specification is identical to that used in 1.2.2.1.

6.2.3 Overview of interactions

The primitives associated with the MAC sublayer to PLS sublayer interface fall into two basic categories:

a) Service primitives that support MAC peer-to-peer interactions.
b) Service primitives that have local significance and support sublayer-to-sublayer interactions.

The following primitives are grouped into these two categories:

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a) Peer-to-Peer
   PLS_DATA.request
   PLS_DATA.indication
b) Sublayer-to-Sublayer
   PLS_CARRIER.indication
   PLS_SIGNAL.indication
   PLS_DATA_VALID.indication

The PLS_DATA primitives support the transfer of data from a single MAC sublayer entity to all other peer MAC sublayer entities contained within the same LAN defined by the broadcast medium.

NOTE—In half duplex mode, all bits transferred from a MAC sublayer entity will in turn be received by the entity itself.

The PLS_CARRIER, PLS_DATA_VALID, and the PLS_SIGNAL primitives provide information needed by the local MAC sublayer entity to perform the media access functions.

6.2.4 Basic services and options

All of the service primitives described in this subclause are considered mandatory.

6.3 Detailed service specification

6.3.1 Peer-to-peer service primitives

6.3.1.1 PLS_DATA.request

6.3.1.1.1 Function

This primitive defines the transfer of data from the MAC sublayer to the local PLS entity.

6.3.1.1.2 Semantics of the service primitive

The primitive shall provide the following parameters:

PLS_DATA.request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take on one of three values: ONE, ZERO, or DATA_COMPLETE and represent a single data bit. The DATA_COMPLETE value signifies that the Media Access Control sublayer has no more data to output.

6.3.1.1.3 When generated

This primitive is generated by the MAC sublayer to request the transmission of a single data bit on the physical medium or to stop transmission.

6.3.1.1.4 Effect of receipt

The receipt of this primitive will cause the PLS entity to encode and transmit either a single data bit or to cease transmission.

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6.3.1.2 PLS_DATA.indication

6.3.1.2.1 Function

This primitive defines the transfer of data from the PLS sublayer to the MAC sublayer.

6.3.1.2.2 Semantics of the service primitive

The semantics of the service primitive are as follows:

PLS_DATA. indicate (INPUT_UNIT)

The INPUT_UNIT parameter can take one of two values each representing a single bit: ONE or ZERO.

6.3.1.2.3 When generated

The PLS_DATA.indication is generated to all MAC sublayer entities in the network after a PLS_DATA.request is issued.

NOTE—In half duplex mode, an indication is also presented to the MAC entity that issued the request.

6.3.1.2.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is not specified in this clause.

6.3.2 Sublayer-to-sublayer service primitives

6.3.2.1 PLS_CARRIER.indication

6.3.2.1.1 Function

This primitive transfers the status of the activity on the physical medium from the PLS sublayer to the MAC sublayer.

6.3.2.1.2 Semantics of the service primitive

The semantics of the primitive are as follows:

PLS_CARRIER.indication (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. The CARRIER_ON value indicates that the DTE Physical Layer had received an *input* message or a *signal_quality_error* message from the MAU. The CARRIER_OFF value indicates that the DTE Physical Layer had received an *input_idle* message and is not receiving an SQE *signal_quality_error* message from the MAU.

6.3.2.1.3 When generated

The PLS_CARRIER.indication service primitive is generated whenever CARRIER_STATUS makes a transition from CARRIER_ON to CARRIER_OFF or vice versa.

6.3.2.1.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is not specified in this clause.

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6.3.2.2 PLS_SIGNAL.indication

6.3.2.2.1 Function

This primitive transfers the status of the Physical Layer signal quality from the PLS sublayer to the MAC sublayer.

6.3.2.2.2 Semantics of the service primitive

The semantics of the service primitive are as follows:

PLS_SIGNAL.indication (SIGNAL_STATUS)

The SIGNAL_STATUS parameter can take one of two values: SIGNAL_ERROR or NO_SIGNAL_ERROR. The SIGNAL_ERROR value indicates to the MAC sublayer that the PLS has received a *signal_quality_error* message from the MAU. The NO_SIGNAL_ERROR value indicates that the PLS has ceased to receive *signal_quality_error* messages from the MAU.

6.3.2.2.3 When generated

The PLS_SIGNAL.indication service primitive is generated whenever SIGNAL_ STATUS makes a transition from SIGNAL_ERROR to NO_SIGNAL_ERROR or vice versa.

6.3.2.2.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is not specified in this clause.

6.3.2.3 PLS_DATA_VALID.indication

6.3.2.3.1 Function

This primitive provides a facility for transferring framing information to the MAC sublayer.

6.3.2.3.2 Semantics of the service primitive

The semantics of the service primitive are as follows:

PLS_DATA_VALID.indication (DATA_VALID_STATUS)

The DATA_VALID_STATUS parameter can take one of two values: DATA_VALID or DATA_NOT_VALID. The DATA_VALID value indicates that the INPUT_UNIT parameter of the PLS_DATA.indication primitive contains valid data of an incoming frame. The DATA_NOT_VALID value indicates that the INPUT_UNIT parameter of the PLS_DATA.indication primitive does not contain valid data of an incoming frame.

6.3.2.3.3 When generated

The PLS_DATA_VALID.indication service primitive is generated whenever the DATA_VALID_STATUS parameter makes a transition from DATA_VALID to DATA_NOT_VALID or vice versa.

6.3.2.3.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is not specified in this clause.

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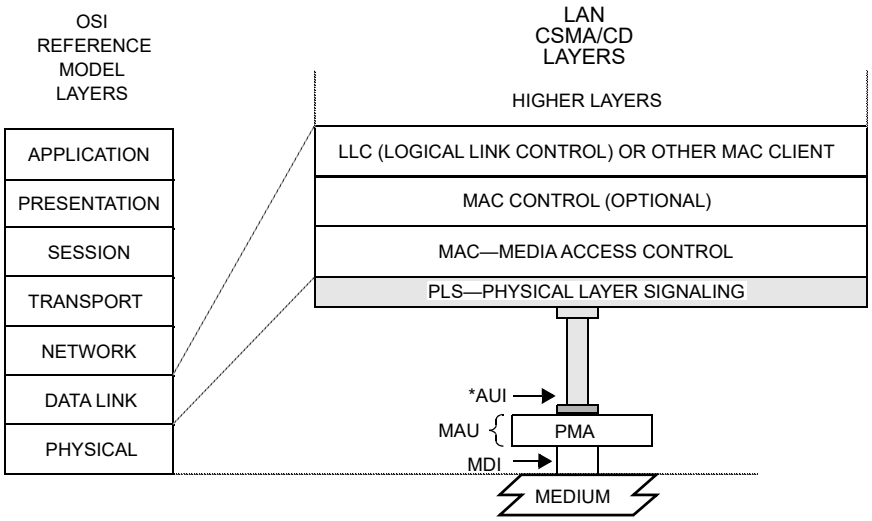
7. Physical Signaling (PLS) and Attachment Unit Interface (AUI) specifications

7.1 Scope

This clause defines the logical, electrical, and mechanical characteristics for the PLS and AUI between Data Terminal Equipment and Medium Attachment Units used in CSMA/CD local area networks. The relationship of this specification to the entire IEEE LAN standard is shown in Figure 7–1. The purpose of this interface is to provide an interconnection that is simple and inexpensive and that permits the development of simple and inexpensive MAUs.



AUI = ATTACHMENT UNIT INTERFACE
MAU = MEDIUM ATTACHMENT UNIT
MDI = MEDIUM DEPENDENT INTERFACE
PMA = PHYSICAL MEDIUM ATTACHMENT

NOTE—For an exposed AUI residing below an MII, see 22.5.

Figure 7–1—Physical Layer partitioning, relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

This interface has the following characteristics:

a) Capable of supporting one or more of the specified data rates.
b) Capable of driving up to 50 m of cable.
c) Permits the DTE to test the AUI, AUI cable, MAU, and the medium itself.
d) Supports MAUs for baseband coax, baseband twisted-pair, broadband coax, and baseband fiber.

7.1.1 Definitions

See 1.4.

7.1.2 Summary of major concepts

a) Each direction of data transfer is serviced with two (making a total of four) balanced circuits: “Data” and “Control.”

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b) The Data and Control circuits are independently self-clocked, thereby, eliminating the need for separate timing circuits. This is accomplished with encoding of all signals. The Control circuit signaling rate is nominally (but not of necessity exactly) equal to the Data circuit signaling rate.
c) The Data circuits are used only for data transfer. No control signals associated with the interface are passed on these circuits. Likewise, the Control circuits are used only for control message transfer. No data signals associated with the interface are passed on these circuits.

7.1.3 Application

This standard applies to the interface used to interconnect Data Terminal Equipment (DTE) to a MAU that is not integrated as a physical part of the DTE. This interface is used to

a) Provide the DTE with media independence for baseband coax, baseband twisted pair, broadband coax, and baseband fiber media so that identical PLS, MAC, and MAC clients may be used with any of these media.
b) Provide for the separation, by cable of up to 50 m, of the DTE and the MAU.

7.1.4 Modes of operation

The AUI can operate in two different modes. All interfaces shall support the normal mode. The monitor mode is optional.

When the interface is being operated in the *normal* mode, the AUI is logically connected to the MDI. The DTE is required to follow the media access algorithms, which provide a single access procedure compatible with all LAN media, to send data over the AUI. The MAU always sends back to the DTE whatever data the MAU receives on the MDI.

When the interface is in the optional *monitor* mode, the MAUs transmitter is logically isolated from the medium. The MAU, in this mode, functions as an observer on the medium. Both the input function and the signal quality error function are operational (see the MAU state diagrams for specific details).

The PLS and AUI as specified here are able to support DTEs and MAUs operating in either half duplex or full duplex modes without change to the PLS or AUI. Full duplex MAUs do not support the monitor mode.

7.1.5 Allocation of function

The allocation of functions in the AUI is such that the majority of the functionality required by the interface can be provided by the DTE, leaving the MAU as simple as possible. This division of functions is based upon the recognition of the fact that since, in many cases, the MAU may be located in an inaccessible location adjacent to the physical medium, service of the MAU may often be difficult and expensive.

7.2 Functional specification

The AUI is designed to make the differences among the various media as transparent as possible to the DTE. The selection of logical control signals and the functional procedures are all designed to this end. Figure 7–2 is a reference model, a generalized MAU as seen by the DTE through the AUI.

Many of the terms used in this subclause are specific to the interface between this sublayer and the MAC sublayer. These terms are defined in the Service Specification for the PLS sublayer.

7.2.1 PLS–PMA (DTE–MAU) Interface protocol

The DTE and MAU communicate by means of a simple protocol across the AUI.

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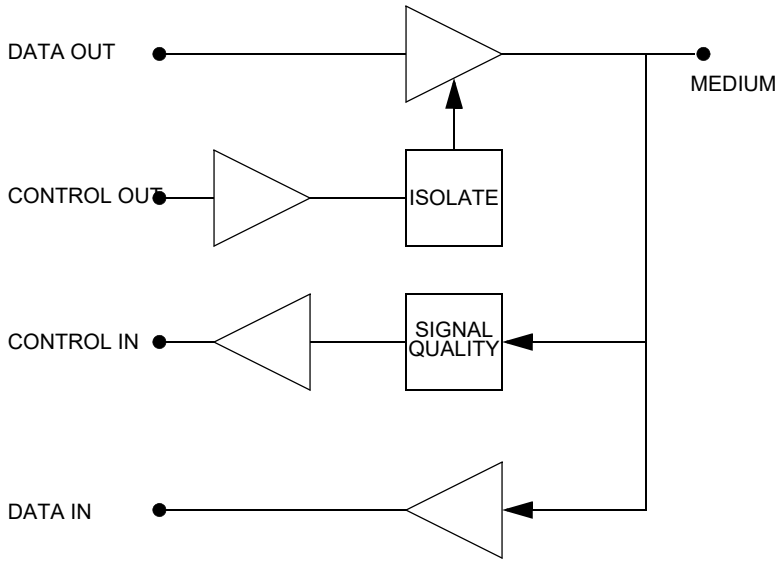

Figure 7–2—Generalized MAU model

7.2.1.1 PLS to PMA messages

The following messages can be sent by PLS sublayer entities in the DTE to PMA sublayer entities in the MAU:

Message	Meaning
output	Output information
output_idle	No data to be output
normal	Cease to isolate the MAU
(Optional)	
isolate	Isolate MAU
mau_request	Request that the MAU be made available

7.2.1.1.1 *output* message

The PLS sublayer sends an *output* message to the PMA sublayer when the PLS sublayer receives an OUTPUT_UNIT from the MAC sublayer.

The physical realization of the *output* message is a CD0 or a CD1 sent by the DTE to the MAU on the Data Out circuit. The DTE sends a CD0 if the OUTPUT_UNIT is a ZERO or a CD1 if the OUTPUT_UNIT is a ONE. This message is time coded—that is, once this message has been sent, the function is not completed over the AUI until one bit time later. The *output* message cannot be sent again until the bit cell being sent as a result of sending the previous *output* message is complete.

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7.2.1.1.2 *output_idle* message

The PLS sublayer sends an *output_idle* message to the PMA sublayer at all times when the MAC sublayer is not in the process of transferring output data across the MAC to PLS interface. The *output_idle* message is no longer sent (and the first OUTPUT_UNIT is sent using the *output* message) as soon after the arrival of the first OUTPUT_UNIT as the MAU can be made available for data output. The *output_idle* message is again sent to the MAU when the DATA_COMPLETE is received from the MAC sublayer. The detailed usage of the *output_idle* message is shown in Figure 7–5.

The physical realization of the *output_idle* message is IDL sent by the DTE to the MAU on the Data Out circuit.

7.2.1.1.3 *normal* message

The PLS sublayer sends a *normal* message to the PMA sublayer after it receives the PLS *start* message from the PLS Reset and Identify function. The *normal* message is also sent after receipt of RESET_MONITOR_MODE from the management entity. The *normal* message is sent continuously by the PLS sublayer to the MAU, unless the PLS Output function requires that the *mau_request* message be sent to permit data output. If *mau_request* is sent during data output, the sending of *normal* will be resumed when the PLS Output function returns to the IDLE state. The *normal* signal is reset by the SET_MONITOR_MODE (this reset function is described more fully by Figure 7–4).

7.2.1.1.4 *isolate* message (optional)

The PLS sublayer sends an *isolate* message to the PMA (in the MAU) whenever the PLS sublayer receives SET_MONITOR_MODE from the management entity. In response to the *isolate* message, the MAU causes the means employed to impress data on the physical medium to be positively prevented from affecting the medium. Since signaling and isolation techniques differ from medium to medium, the manner in which this positive isolation of the transmitting means is accomplished is specified in the appropriate MAU subclause. However, the intent of this positive isolation of the transmitter is to ensure that the MAU will not interfere with the physical medium in such a way as to affect transmissions of other stations even in the event that the means normally employed to prevent the transmitter from affecting the medium have failed to do so. The specification of positive isolation is not to be construed to preclude use of either active or passive devices to accomplish this function.

The physical realization of the *isolate* message is a CS0 signal sent by the DTE to the MAU over the Control Out circuit.

7.2.1.1.5 *mau_request* message (optional)

The PLS sublayer sends the *mau_request* message to the PMA sublayer if the PMA sublayer is sending the *mau_not_available* message and the MAC sublayer has sent the first OUTPUT_UNIT of a new transmission. The PLS sublayer continues to send the *mau_request* message to the MAU until the MAC sublayer sends the DATA_COMPLETE request to the PLS sublayer across the MAC to PLS interface. See Figure 7–3, Figure 7–5, and Figure 7–9 for details.

In addition, the *mau_request* message is used by the Reset and Identify function in the IDENTIFY 3 state to determine whether the MAU has the Isolate function.

The physical realization of *mau_request* is a CS1 sent by the DTE to the MAU on the Control Out circuit.

The physical realization of the *normal* message is the IDL signal sent by the DTE to the MAU on the Control Out circuit. In the absence of the CO circuit, MAUs implementing the Isolate function shall act as if the *normal* message is present. The CO circuit components may be absent from the DTE, AUI, or MAU.

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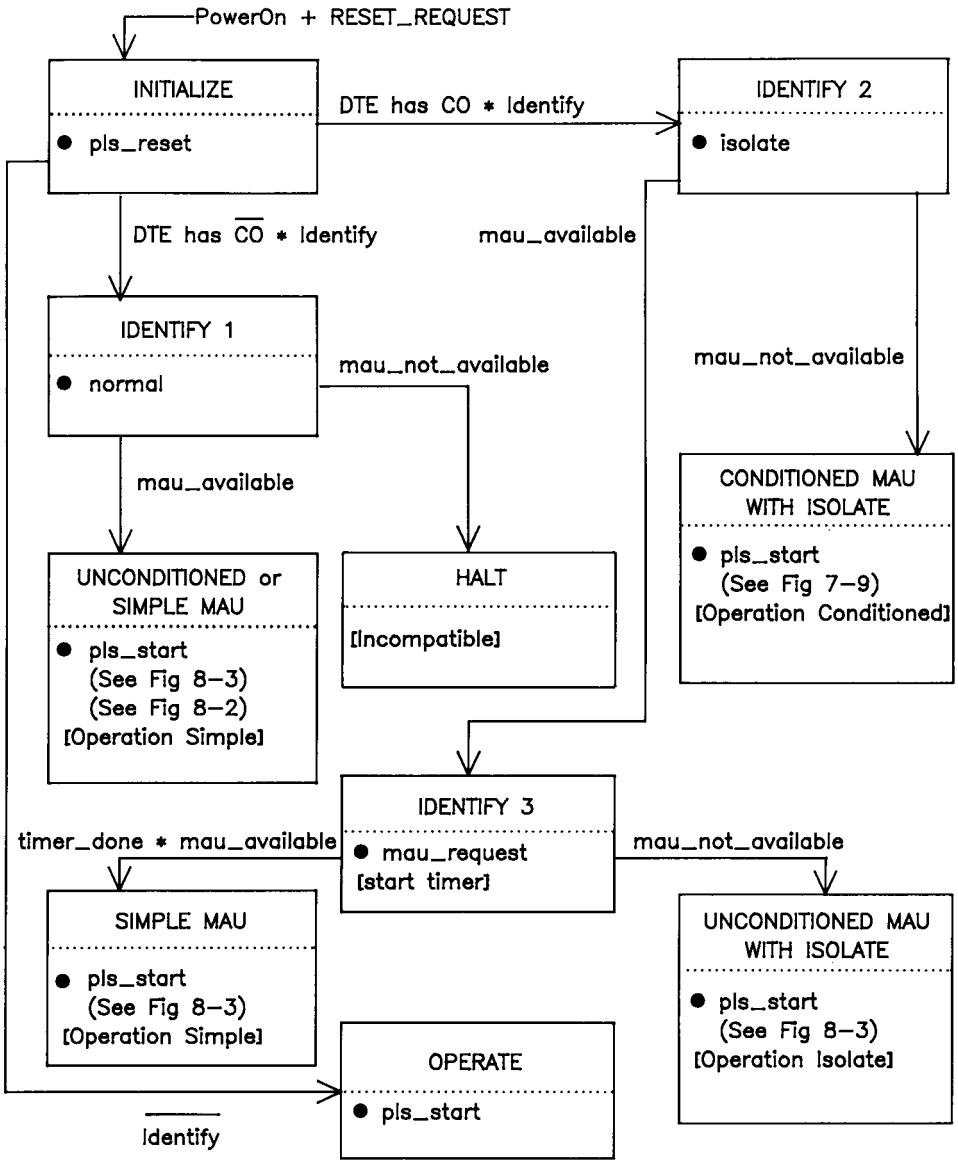

NOTES: (1) All states may be omitted except INITIALIZE and OPERATE
(2) "Identify" means DTE can recognize uniquely all CI messages and the entire function has been implemented
(3) "Identify" with bar means DTE fails to recognize *mau_not_available* or has a partial implementation of the function

Figure 7–3—PLS Reset and Identify function

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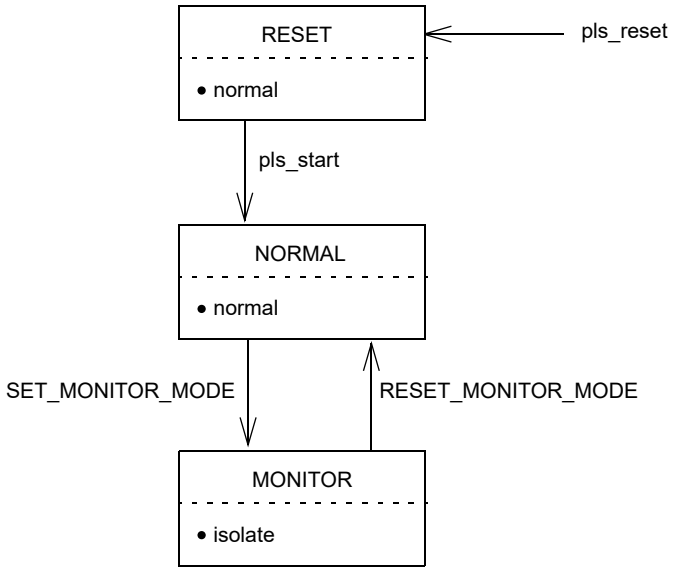

Figure 7–4—PLS Mode function

7.2.1.2 PMA to PLS interface

The following messages can be sent by the Physical Medium Attachment sublayer entities in the MAU to the PLS sublayer entities in the DTE:

Message	Meaning
input	Input information
input_idle	No input information
signal_quality_error	Error detected by MAU
mau_available	MAU is available for output
(Optional)	
mau_not_available	MAU is not available for output

In systems operating in full duplex mode, it is permitted, but not required, to implement the *signal_quality_error* message.

7.2.1.2.1 *input* message

The PMA sublayer sends an *input* message to the PLS sublayer when the MAU has received a bit from the medium and is prepared to transfer this bit to the DTE. The actual mapping of the signals on the medium to the type of *input* message to be sent to the DTE is contained in the specifications for each specific MAU type. In general, when the *signal_quality_error* message is being sent by the MAU, the symmetry specifications for circuit DI are not guaranteed to be met.

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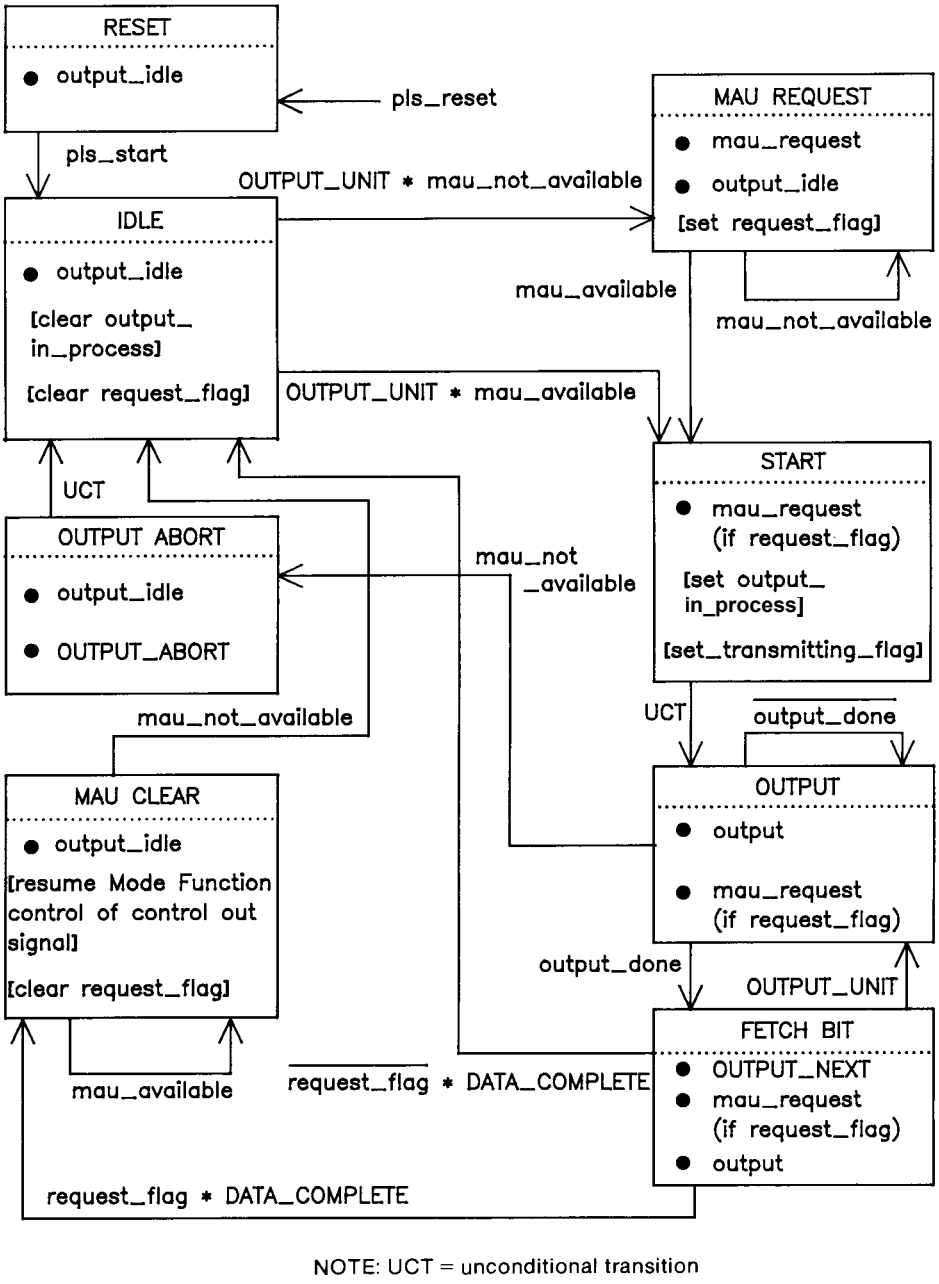

Figure 7–5—PLS Output function

The physical realization of the *input* message consists of CD0 or CD1 waveforms. If the *signal_quality_error* message is being sent from the MAU, the input waveform is unpredictable.

NOTE—This signal is not necessarily retimed by the MAU. Consult the appropriate MAU specification for timing and jitter.

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7.2.1.2.2 *input_idle* message

The PMA sublayer sends an *input_idle* message to the PLS sublayer when the MAU does not have data to send to the DTE.

The physical realization of the *input_idle* message is an IDL sent by the MAU to the DTE on the Data In circuit.

7.2.1.2.3 *signal_quality_error* message

The PMA sublayer sends a *signal_quality_error* message to the PLS sublayer in response to any of three possible conditions. These conditions are improper signals on the medium, collision on the medium, and reception of the *output_idle* message. They are described in the lettered paragraphs that follow. The physical realization of the *signal_quality_error* message is a CS0 sent by the MAU to the DTE on the Control In circuit.

In systems operating in half duplex mode, the MAU is required to assert the *signal_quality_error* message at the appropriate times whenever the MAU is powered, and not just when the DTE is requesting data output. In systems operating in full duplex mode, it is permitted, but not required, to implement the *signal_quality_error* message. See Figure 7–9, Figure 8–2, and Figure 8–3 for details.

a) Improper Signals on the Medium. The MAU may send the *signal_quality_error* message at any time due to improper signals on the medium. The exact nature of these improper signals are medium-dependent. Typically, this condition might be caused by a malfunctioning MAU (for example, repeater or head-end) connected to the medium or by a break or short in the medium. See the appropriate MAU specification for specific conditions that may cause improper signals on a given medium.
b) Collision. Collision occurs when more than one MAU is transmitting on the medium. The local MAU shall send the *signal_quality_error* message in every instance when it is possible for it to ascertain that more than one MAU is transmitting on the medium. The MAU shall make the best determination possible. The MAU shall not send the *signal_quality_error* message when it is unable to determine conclusively that more than one MAU is transmitting.
c) *signal_quality_error* Message Test. The MAU sends the *signal_quality_error* message at the completion of the Output function. See Figure 7–9 and Clause 8 for a more complete description of this test.

7.2.1.2.4 *mau_available* message

The PMA sublayer sends the *mau_available* message to the PLS sublayer when the MAU is available for output. The *mau_available* message is always sent by a MAU that is always prepared to output data except when it is required to signal the *signal_quality_error* message. Such a MAU does not require *mau_request* to prepare itself for data output. See Figure 7–3, Figure 7–5, and Figure 7–9 for details.

The physical realization of the *mau_available* message is an IDL sent by the MAU to the DTE on the Control In circuit.

7.2.1.2.5 *mau_not_available* message (optional)

The PMA sublayer sends a *mau_not_available* message to the PLS sublayer when the MAU is not available for output. Figure 7–5 shows the relationship of *mau_not_available* to the Output function.

The *mau_not_available* message is also used by a MAU that contains the Isolate function and does not need to be conditioned for output to signal the presence of the Isolate function during the PLS Reset function (see Figure 7–3 and Figure 8–3).

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The physical realization of the *mau_not_available* message is a CS1 sent by the MAU to the DTE on the Control In circuit.

7.2.2 PLS interface to MAC and management entities

The PLS sublayer interfaces described here are for reference only. This clause specifies the services sent between the MAC sublayer and the PLS sublayer.

7.2.2.1 PLS–MAC interface

The following messages can be sent between PLS sublayer entities and MAC sublayer entities:

Message	Meaning
OUTPUT_UNIT	Data sent to the MAU
OUTPUT_STATUS	Response to OUTPUT_UNIT
INPUT_UNIT	Data received from the MAU
CARRIER_STATUS	Indication of channel activity
SIGNAL_STATUS	Indication of error/no error condition
DATA_VALID_STATUS	Indication of input activity

7.2.2.1.1 OUTPUT_UNIT

The MAC sublayer sends the PLS sublayer an OUTPUT_UNIT every time the MAC sublayer has a bit to send. Once the MAC sublayer has sent an OUTPUT_UNIT to the PLS sublayer, it may not send another OUTPUT_UNIT until it has received an OUTPUT_STATUS message from the PLS sublayer. The OUTPUT_UNIT is a ONE if the MAC sublayer wants the PLS sublayer to send a CD1 to the PMA sublayer, a ZERO if a CD0 is desired, or a DATA_COMPLETE if an IDL is desired.

7.2.2.1.2 OUTPUT_STATUS

The PLS sublayer sends the MAC sublayer OUTPUT_STATUS in response to every OUTPUT_UNIT received by the PLS sublayer. OUTPUT_STATUS sent is an OUTPUT_NEXT if the PLS sublayer is ready to accept the next OUTPUT_UNIT from the MAC sublayer, or an OUTPUT_ABORT if the PLS sublayer was not able to process the previous OUTPUT_UNIT. (The purpose of OUTPUT_STATUS is to synchronize the MAC sublayer data output with the data rate of the physical medium.)

7.2.2.1.3 INPUT_UNIT

The PLS sublayer sends the MAC sublayer an INPUT_UNIT every time the PLS receives an *input* message from the PMA sublayer. The INPUT_UNIT is a ONE if the PLS sublayer receives a CD1 from the PMA sublayer, a ZERO if the PLS sublayer receives a CD0 from the PMA sublayer.

7.2.2.1.4 CARRIER_STATUS

The PLS sublayer sends the MAC sublayer CARRIER_STATUS whenever the PLS sublayer detects a change in carrier status. The PLS sublayer sends CARRIER_ON when it receives an *input* or *signal_quality_error* message from the PMA and the previous CARRIER_STATUS that the PLS sublayer sent to the MAC sublayer was CARRIER_OFF. The PLS sublayer sends CARRIER_OFF when it receives an *input_idle* from the PMA sublayer, no *signal_quality_error* (either *mau_available* or *mau_not_available*)

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message and the previous CARRIER_STATUS that the PLS sublayer sent to the MAC sublayer was CARRIER_ON.[37]

7.2.2.1.5 SIGNAL_STATUS

The PLS sublayer sends the MAC sublayer SIGNAL_STATUS whenever the PLS sublayer detects a change in the signal quality (as reported by the PMA). The PLS sublayer sends SIGNAL_ERROR when it receives a *signal_quality_error* message from the PMA sublayer and the previous SIGNAL_STATUS the PLS sublayer sent was NO_SIGNAL_ERROR. The PLS sublayer sends NO_SIGNAL_ERROR when it receives no *signal_quality_error* (either *mau_available* or *mau_not_available)* message from the PMA sublayer and the previous CARRIER_STATUS that the PLS sent to the MAC sublayer was SIGNAL_ERROR.[38]

7.2.2.1.6 DATA_VALID_STATUS

The PLS sublayer sends the MAC sublayer DATA_VALID_STATUS whenever the PLS sublayer detects a change in receive data status. The PLS sublayer sends DATA_VALID when it receives an *input* message from the PMA and the previous DATA_VALID_STATUS that the PLS sublayer sent to the MAC sublayer was DATA_NOT_VALID. The PLS sublayer sends DATA_NOT_VALID when it is not receiving an input message from the PMA and the previous DATA_VALID_STATUS that the PLS sublayer sent to the MAC sublayer was DATA_VALID.

7.2.2.2 PLS–management entity interface

The following messages may be sent between the PLS sublayer entities and intralayer or higher layer management entities:

Message	Meaning
RESET_REQUEST	Reset PLS to initial “Power On” state
RESET_RESPONSE	Provides operational information
MODE_CONTROL	Control operation
SQE_TEST	Signal Quality Error test results

7.2.2.2.1 RESET_REQUEST

The management entity sends the PLS sublayer RESET_REQUEST when the PLS sublayer needs to be reset to a known state. Upon receipt of RESET_REQUEST, the PLS sublayer resets all internal logic and restarts all functions. See Figure 7–3 for details.

---

[37] Formerly, the Carrier Sense function described in Figure 7–8 generated the CARRIER_STATUS message described above. For the sake of consistency with common implementation practice, the variable carrierSense (see 4.3.3) is generated directly by the Carrier Sense function in recent editions of the standard.

The mapping between the CARRIER_STATUS message and the carrierSense variable is as follows. When the carrierSense variable changes from False to True, the CARRIER_STATUS message is sent with the parameter CARRIER_ON. When the value of the carrierSense variable changes from True to False, the CARRIER_STATUS message is sent with the parameter CARRIER_OFF.

[38] Formerly, the PLS Error Sense function described in Figure 7–7 generated the SIGNAL_STATUS message described above. For the sake of consistency with common implementation practice, the variable collisionDetect (see 4.3.3) is generated directly by the PLS Error Sense function in recent editions of the standard.

The mapping between the SIGNAL_STATUS message and the collisionDetect variable is as follows. When the collisionDetect variable changes from False to True, the SIGNAL_STATUS message is sent with the parameter SIGNAL_ERROR. When the value of the collisionDetect variable changes from True to False, the SIGNAL_STATUS message is sent with the parameter NO_SIGNAL_ERROR.

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7.2.2.2.2 RESET_RESPONSE

The PLS sublayer sends the management entity RESET_RESPONSE upon completion of the Reset and Identify function (see Figure 7–3 and 7.2.4.1) whether invoked due to power on or due to a RESET_REQUEST. Which RESET_RESPONSE was sent is determined by the Reset and Identify function. A RESET_RESPONSE of OPERATION SIMPLE, OPERATION ISOLATE, or OPERATION CONDITIONED is sent if the MAU is compatible with the DTE and the MAU is simple (no isolate) or if the DTE does not support Isolate even if Isolate is supported by the MAU, supports Isolate but does not require conditioning, or supports Isolate and does require conditioning to output. A RESET_RESPONSE of INCOMPATIBLE is sent if the MAU is not compatible with the DTE (that is, the MAU requires conditioning but the DTE does not support conditioning).

7.2.2.2.3 MODE_CONTROL

The management entity sends MODE_CONTROL to the PLS sublayer to control PLS functions. MODE_CONTROL capabilities are as follows:

Message	Meaning
ACTIVATE PHYSICAL	Supply power on circuit VP
DEACTIVATE PHYSICAL	Remove power from circuit VP
SET_MONITOR_MODE	Send Isolate to MAU
RESET_MONITOR_MODE	Send Normal to MAU

7.2.2.2.4 SQE_TEST

The PLS sublayer sends SQE_TEST to the management entity at the conclusion of each *signal_quality_error* test (see Output Function, 7.2.4.3). The PLS sublayer sends SQE_TEST_ERROR if the *signal_quality_error* test fails or SQE_TEST_OK if the *signal_quality_error* test passes.

In systems operating in full duplex mode, it is permitted, but not required, to implement the SQE_TEST message.[39]

7.2.3 Frame structure

Frames transmitted on the AUI shall have the following structure:

<silence><preamble><sfd><data><etd><silence>

[39]Formerly, the PLS Carrier Sense function described in Figure 7–8 generated the SQE_TEST message described above. For the sake of consistency with common implementation practice, the variable SQETestError is generated directly by the PLS Carrier Sense function in recent editions of the standard.

The mapping between the SQE_TEST message and the PLS Carrier Sense function described in Figure 7–8 is as follows. When the transition from the state WAIT 1 to the state FAILURE occurs, the SQE_TEST message is sent with the parameter SQE_TEST_ERROR. When the transition from either the state WAIT 1 or the state ABORT_TEST to the state WAIT 2 occurs, the SIGNAL_STATUS message is sent with the parameter NO_SIGNAL_ERROR.

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The frame elements shall have the following characteristics:

Element	Characteristics
<silence>	= no transitions
<preamble>	= alternating (CD1) and (CD0) | 56 bit times (ending in CD0)
<sfd>	= (CD1)(CD0)(CD1)(CD0)(CD1)(CD0)(CD1)(CD1)
<data>	= 8 × N instances of CD0 or CD1
<etd>	= IDL

7.2.3.1 Silence

The <silence> delimiter provides an observation window for an unspecified period of time during which no transitions occur on the AUI. The minimum length of this period is specified by the access procedure.

7.2.3.2 Preamble

The <preamble> delimiter begins a frame transmission and provides a signal for receiver synchronization. The signal shall be an alternating pattern of (CD1) and (CD0). This pattern shall be transmitted on the Data Out circuit by the DTE to the MAU for a minimum of 56 bit times at the beginning of each frame. The last bit of the preamble (that is, the final bit of preamble before the start of frame delimiter) shall be a CD0.

The DTE is required to supply at least 56 bits of preamble in order to satisfy system requirements. System components consume preamble bits in order to perform their functions. The number of preamble bits sourced ensures an adequate number of bits are provided to each system component to correctly implement its function.

7.2.3.3 Start of Frame Delimiter (SFD)

The <sfd> indicates the start of a frame, and follows the preamble. The <sfd> element of a frame shall be

(CD1)(CD0)(CD1)(CD0)(CD1)(CD0)(CD1)(CD1)

7.2.3.4 Data

The <data> in a transmission shall be in multiples of eight (8) encoded data bits (CD0s and CD1s).

7.2.3.5 End of transmission delimiter

The <etd> delimiter indicates the end of a transmission and serves to turn off the transmitter. The signal shall be start of IDL.

7.2.4 PLS functions

The PLS sublayer functions consist of a Reset and Identify function and five simultaneous and asynchronous functions. These functions are Output, Input, Mode, Error Sense, and Carrier Sense. All of the five functions are started immediately following the completion of the Reset and Identify function. These functions are depicted in the state diagrams shown in Figure 7–3 through Figure 7–8, using notation described in 1.2.1.

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7.2.4.1 Reset and Identify function

The Reset and Identify function is executed any time either of two conditions occur. These two conditions are “power on” and the receipt of RESET_REQUEST from the management entity. The Reset and Identify function initializes all PLS functions, and (optionally) determines the capability of the MAU attached to the AUI. Figure 7–3 is the state diagram of the Reset and Identify function. The Identify portion of the function is optional.

7.2.4.2 Mode function

The MAU functions in two modes: normal and monitor. The monitor mode is optional. The state diagram of Figure 7–4 depicts the operation of the Mode function. When the MAU is operating in the normal mode, it functions as a direct connection between the DTE and the medium. Data sent from the DTE are impressed onto the medium by the MAU and all data appearing on the medium are sent to the DTE by the MAU. When the MAU is operating in the monitor mode, data appearing on the medium is sent to the DTE by the MAU as during the normal mode. *signal_quality_error* is also asserted on the AUI as during operation in the normal mode. However, in the monitor mode, the means employed to impress data on the physical medium is positively prevented from affecting the medium. Since signaling and isolation techniques differ from medium to medium, the manner in which this positive isolation of the transmitting means is accomplished is specified in the appropriate MAU document. However, the intent of this positive isolation of the transmitter is to ensure that the MAU will not interfere with the physical medium in such a way as to affect transmission of other stations even in the event of failure of the normal transmitter disabling control paths within the transmitting mechanism of the MAU.

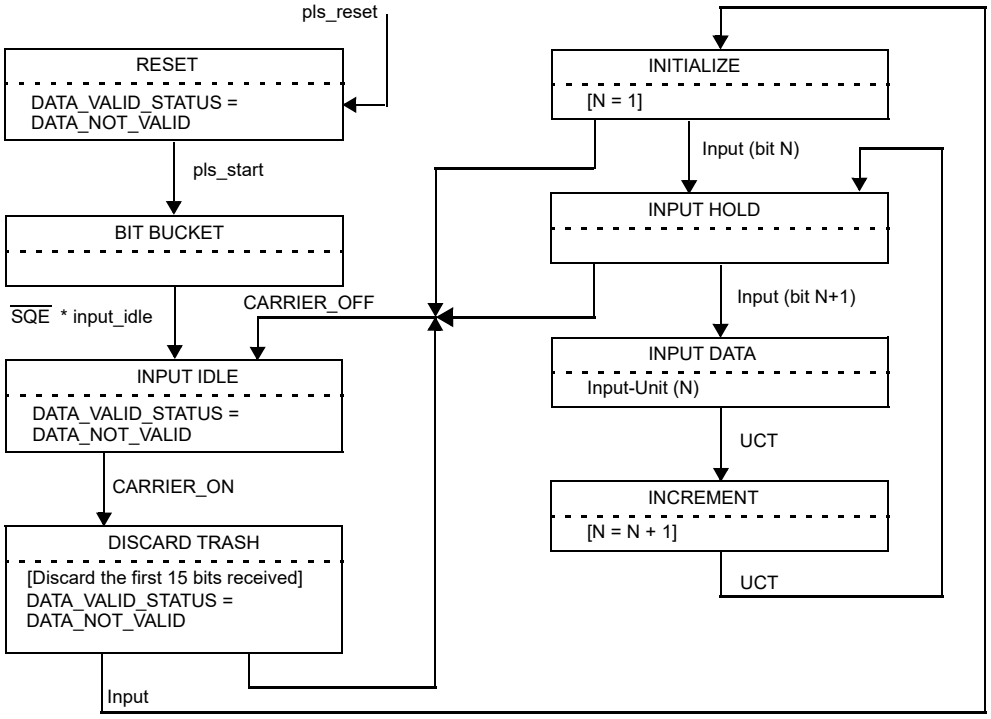

Figure 7–6—PLS Input and Data_Valid function

The monitor mode is intended to permit a network station to determine if it is the source of interference observed on the medium.

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NOTE—The monitor mode is intended to be used only by Network Management for fault isolation and network operation verification. It is intended that the *isolate* message provide direct control over the mode function so that these tasks can be performed. IMPROPER USE OF THE ISOLATE FUNCTION CAN CAUSE ERRONEOUS FRAMES. Clause 5, Layer Management, provides details on the proper use of this function.

7.2.4.3 Output function

The PLS sublayer Output function transparently performs the tasks of conditioning the MAU for output and data transfer from the MAC sublayer to the MAU. The state diagram of Figure 7–5 depicts the Output function operation.

At the conclusion of the Output function, if a collision has not occurred, a test is performed to verify operation of the signal quality detection mechanism in the MAU and to verify the ability of the AUI to pass the *signal_quality_error* message to the PLS sublayer. The operation of this test in the DTE is shown in Figure 7–8.

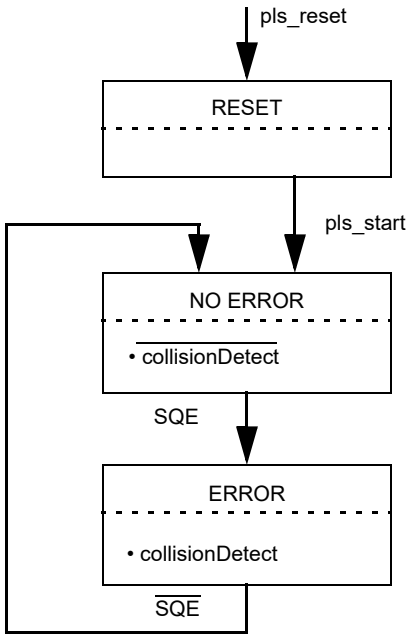
NOTE—In systems operating in full duplex mode, it is permitted, but not required, to implement the *signal_quality_error* message test.

7.2.4.4 Input function

The PLS sublayer Input function transparently performs the task of data transfer from the MAU to the MAC sublayer. Additionally, the Input function sends DATA_VALID_STATUS to the MAC sublayer, as appropriate. The state diagram of Figure 7–6 depicts the Input function operation.

7.2.4.5 Error Sense function

The PLS sublayer Error Sense function performs the task of sending collisionDetect to the MAC sublayer whenever the PLS receives the *signal_quality_error* message from the PMA sublayer. The state diagram of Figure 7–7 depicts the Error Sense function operation.



NOTE—SQE = *signal_quality_error*

Figure 7–7—PLS Error Sense function

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7.2.4.6 Carrier Sense function

The PLS sublayer Carrier Sense function performs the task of sending carrierSense and sqeTestError to the MAC sublayer. The state diagram of Figure 7–8 depicts the Carrier Sense function operation.[40]

Verification of the *signal_quality_error* detection mechanism occurs in the following manner (in the absence of a fault on the medium):

a) At the conclusion of the Output function, the DTE opens a time window during which it expects to see the *signal_quality_error* message asserted on the Control In circuit. The time window begins when carrierSense de-asserts and the variable transmitting is false. The duration of the window shall be at least 4.0 μs but no more than 8.0 μs. During the time window (depicted as carrier_inhibit_timer, Figure 7–8) the carrierSense function is inhibited.
b) The MAU, upon waiting Tw after the conclusion of output, activates as much of the *signal_quality_error* detecting mechanism as is possible without placing signals on the medium, thus sending the *signal_quality_error* message across the AUI for 10 bit times ± 5 bit times (10/BR seconds ± 5/BR seconds).
c) The DTE interprets the reception of the *signal_quality_error* message from the MAU as indication that the *signal_quality_error* detecting mechanism is operational and the *signal_quality_error* message may be both sent by the MAU and received by the DTE.

NOTE 1—The occurrence of multiple (overlapping) transmitters on the medium during the time that the test window is open, as specified above, will satisfy the test and will verify proper operation of the signal quality error detecting mechanism and sending and receiving of the appropriate physical error message.

NOTE 2—If *signal_quality_error* exists at the DTE before CARRIER_OFF occurs, then the Collision Presence test sequence within the PLS as described in 7.2.4.3 above is aborted as shown in Figure 7–8.

NOTE 3—In systems operating in full duplex mode, it is permitted, but not required, to implement the *signal_quality_error* message test.

7.3 Signal characteristics

7.3.1 Signal encoding

Two different signal encoding mechanisms may be used by the AUI. One of the mechanisms is used to encode data, the other to encode control.

7.3.1.1 Data encoding

Manchester encoding is used for the transmission of data across the AUI. Manchester encoding is a binary signaling mechanism that combines data and clock into “bit-symbols.” Each bit-symbol is split into two halves with the second half containing the binary inverse of the first half; a transition always occurs in the middle of each bit-symbol. During the first half of the bit-symbol, the encoded signal is the logical complement of the bit value being encoded. During the second half of the bit-symbol, the encoded signal is the uncomplemented value of the bit being encoded. Thus, a CD0 is encoded as a bit-symbol in which the first half is HI and the second half is LO. A CD1 is encoded as a bit-symbol in which the first half is LO and the second half is HI. Examples of Manchester waveforms are shown in Figure 7–10.

[40]Formerly, this function utilized the variable output_in_process generated by the PLS output function described in Figure 7–5. For the sake of consistency with common implementation practice, the variable transmitting (see 4.3.3) is utilized directly by the PLS Carrier Sense function in recent editions of the standard.

The mapping between variable output_in_process and the variable transmitting is as follows. When output_in_process is true, transmitting is true; when output_in_process is false, transmitting is false.

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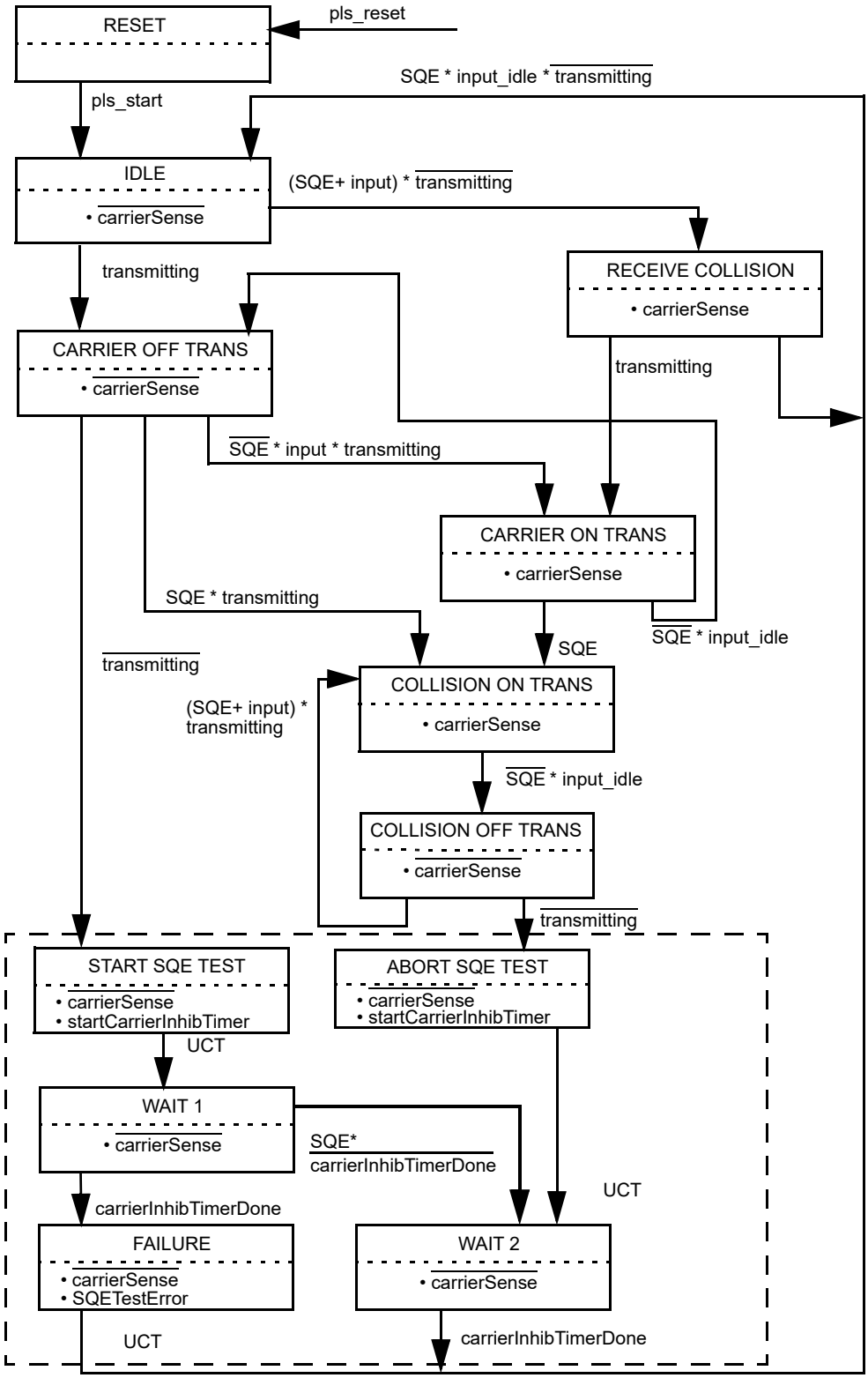

NOTE 1—UCT is unconditional transition; SQE is *signal_quality_error*.
NOTE 2—States within the dotted box are not implemented for the PLS sublayer within a repeater port.

Figure 7–8—PLS Carrier Sense function

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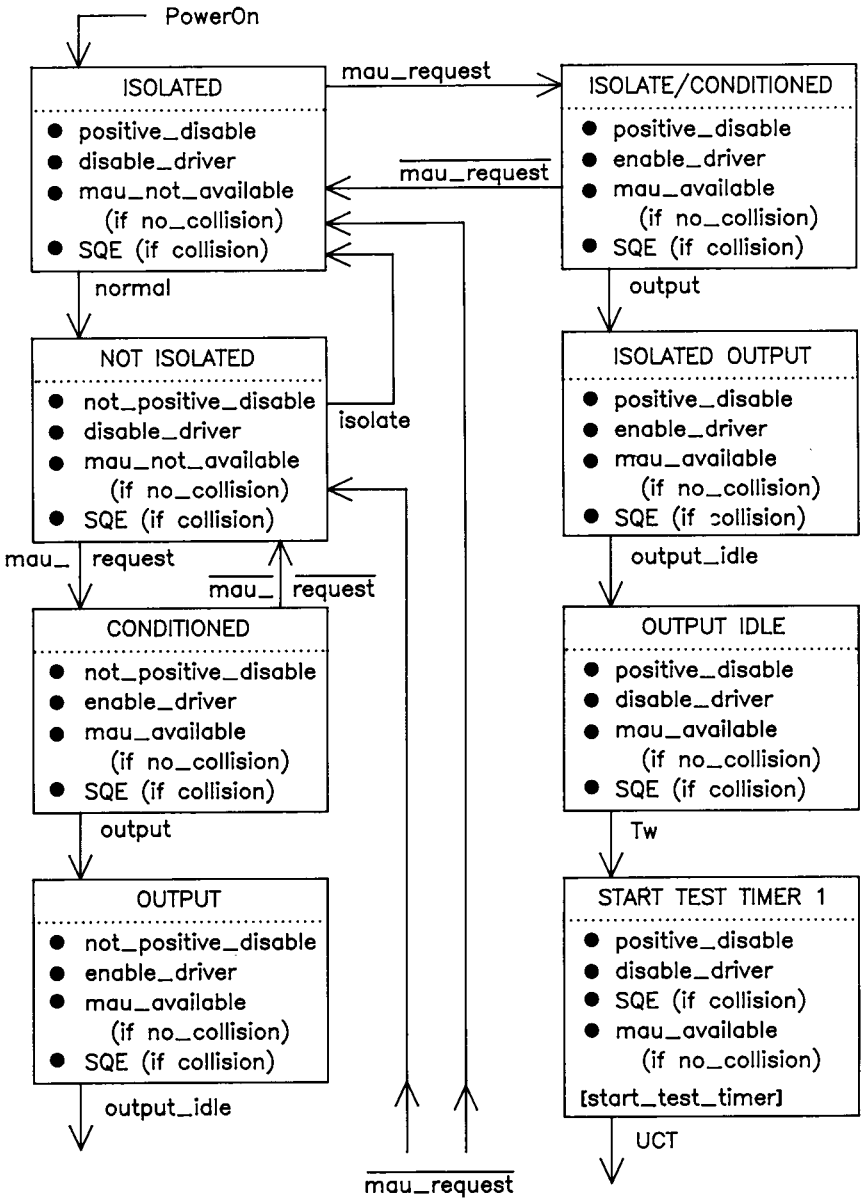

NOTE—See Figure 8–2 and Figure 8–3 for simple and isolate type MAUs.

a)

Figure 7–9—Interface function for MAU with conditioning

The line condition IDL is also used as an encoded signal. An IDL always starts with a HI signal level. Since IDL always starts with a HI signal, an additional transition will be added to the data stream if the last bit sent was a zero. This transition cannot be confused with clocked data (CD0 or CD1) since the transition will occur at the start of a bit cell. There will be no transition in the middle of the bit cell. The IDL condition, as sent by a driver, shall be maintained for a minimum of 2 bit times. The IDL condition shall be detected within l.6 bit times at the receiving device.

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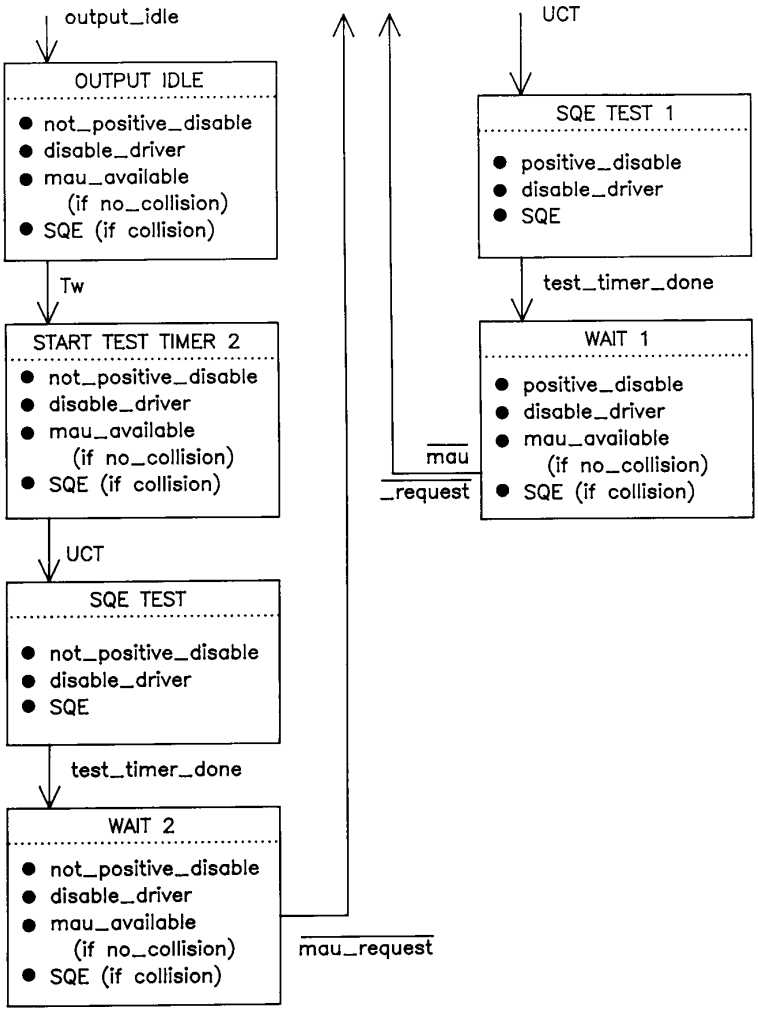

NOTE—See Figure 8–2 and Figure 8–3 for simple and isolate type MAUs.

b)

Figure 7–9—*(Continued)* Interface function for MAU with conditioning

a) System jitter considerations make detection of IDL (etd, end transmission delimiter) earlier than 1.3 bit times impractical. The specific implementation of the phase-locked loop or equivalent clock recovery mechanism determines the lower bound on the actual IDL detection time. Adequate margin between lower bound and 1.6 bit times should be considered.

b) Recovery of timing implicit in the data is easily accomplished at the receiving side of the interface because of the wealth of binary transitions guaranteed to be in the encoded waveform, independent of the data sequence. A phase-locked loop or equivalent mechanism maintains continuous tracking of the phase of the information on the Data circuit.

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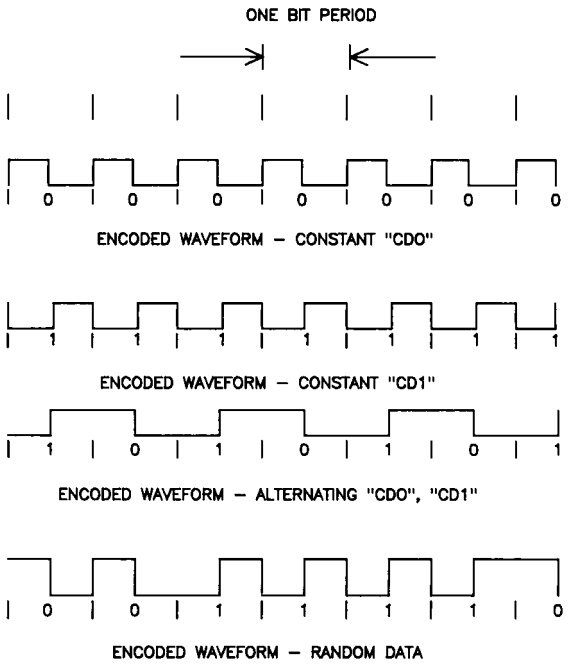

Figure 7–10—Examples of Manchester waveforms

7.3.1.2 Control encoding

A simpler encoding mechanism is used for control signaling than for data signaling. The encoded symbols used in this signaling mechanism are CS0, CS1, and IDL. The CS0 signal is a signal stream of frequency equal to the bit rate (BR). The CS1 signal is a signal stream of frequency equal to half of the bit rate (BR/2). If the interface supports more then one bit rate (see 4.2), the bit rate in use on the data circuits is the one to which the control signals are referenced. The IDL signal used on the control circuits is the same as the IDL signal defined for the data circuits (see 7.3.1.1). The Control Out circuit is optional (O) as is one message on Control In.

The frequency tolerance of the CS1 and CS0 signals on the CO circuit shall be ±5% and that of the CS1 signal on the CI circuit shall be ±15%. The duty cycle of the above signals is nominally 50%/50% and shall be no worse than 60%/40%. The CS0 signal on the CI circuit shall have a frequency tolerance of BR +25%, –15% with the pulse widths no less than 35 ns and no greater than 70 ns at the zero crossing points.

The meaning of the signals on the Control Out circuit (DTE to MAU) are as follows:

Signal	Message	Description
IDL	normal	Instructs the MAU to enter (remain in) normal mode
CS1	*mau_request* (O)	Requests that the MAU should be made available
CS0	*isolate* (O)	Instructs the MAU to enter (remain in) monitor mode

The meaning of the signals on the Control In circuit (MAU to DTE) are as follows:

Signal	Message	Description
IDL	mau_available	Indicates that the MAUs ready to output data
CS1	mau_not_available	Indicates that the MAU is not ready to output data
CS0	s*ignal_quality_error*	Indicates that the MAU has detected an error output data

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7.3.2 Signaling rate

Multiple signaling rates are encompassed by this standard. The signaling rate specified here is 10 million bits per second ±0.01%.

It is intended that a given MDI operate at a single data rate. It is not precluded that specific DTE and MAU designs be manually switched or set to alternate rates. A given local network shall operate at a single signaling rate. To facilitate the configuration of operational systems, DTE and MAU devices shall be labeled with the actual signaling rate used with that device.

7.3.3 Signaling levels

Exact voltage and current specifications are listed in 7.4.

7.4 Electrical characteristics

Terms BR and BR/2 have very specific meaning as used in this subclause. The term BR is used to mean the bit rate of the highest signaling rate supported by any one implementation of this interface, BR/2 is used to mean half the bit rate of the lowest signaling rate supported by any one implementation of this interface (see 7.3.2). An interface may support one or more signaling rates.

NOTE—The characteristics of the driver and receiver can be achieved with standard ECL logic with the addition of an appropriate coupling network; however, this implementation is not mandatory.

7.4.1 Driver characteristics

The driver is a differential driver capable of driving the specified 78 Ω interface cable. Only the parameters necessary to ensure compatibility with the specified receiver and to assure personnel safety at the interface connector are specified in the following subclauses.

7.4.1.1 Differential output voltage, loaded

Drivers shall meet all requirements of this subclause under *two* basic sets of test conditions (that is, each of two resistive values). For drivers located within a DTE, a combined inductive load of 27 μH ± 1% and either a 73 Ω or 83 Ω ± 1% resistive load shall be used. For a driver located within a MAU, a combined inductive load of 50 μH ± 1% and either 73 Ω or 83 Ω ± 1% resistive load shall be used.

The differential output voltage, V_{dm}, is alternately positive and negative in magnitude with respect to zero voltage. The value of V_{dm} into either of the two test loads identified above (R = 73 Ω or 83 Ω ± 1%) at the interface connector of the driving unit shall satisfy conditions defined by values V_{min} and V_{max} shown in Figure 7–11 for signals in between BR and BR/2 meeting the frequency and duty cycle tolerances specified for the signal being driven. The procedure for measuring and applying the test condition is as follows:

a) Construct a template representing the shaded area of Figure 7–11. Once constructed, the template may be shifted along the time axis in order to accommodate differences in the 10% to 50% and 50% to 90% transition times of the driver waveform.
b) Find the peak value of V_{dm}. This is V_{max}.
c) Find the minimum value of V_{dm} during the period between the shaded regions for the waveform's rising and falling transitions (time T1 in Figure 7–11). This minimum value is V_{min}.
d) V_{max} shall be < 1315 mV, V_{min} shall be > 450 mV, and V_{max}/V_{min} shall be < 1.37.
e) V_{dm} shall remain < 1170 mV 24 ns after a zero crossing.
f) The waveform shall remain within the shaded area limits.

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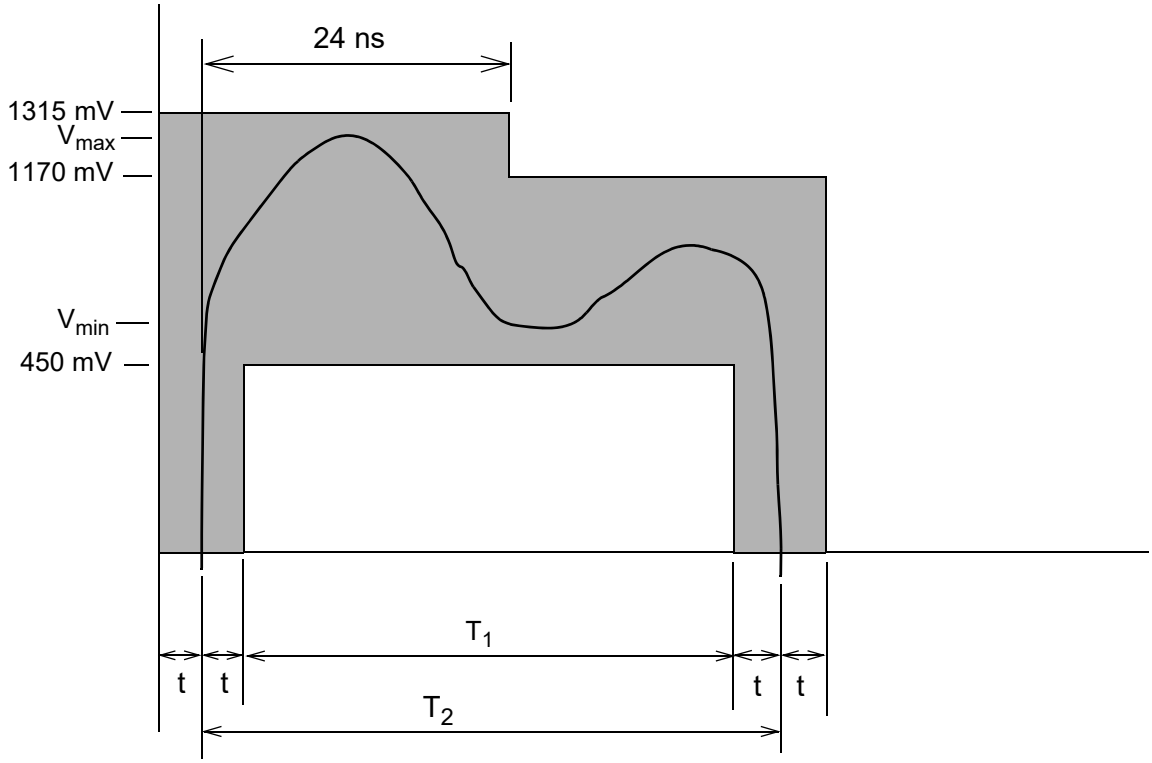
The differential output voltage magnitude, V_{dm}, into either of the two test loads identified above, at the interface connector of the driving unit during the idle state shall be within 40 mV of 0 V. The current into either of the two test loads shall be limited to 4 mA.

When a driver, connected to the appropriate two test loads identified above, enters the idle state, it shall maintain a minimum differential output voltage of at least 380 mV for at least 2 bit times after the last low to high transition.



t = 3.5 ns at 1–10 MHz data rates
T_2 = (BT or BT/2) ± 2 × T_j, where T_j is the amount of MAU–DTE permissible edge jitter
T_1 = T_2 – 7.0 ns

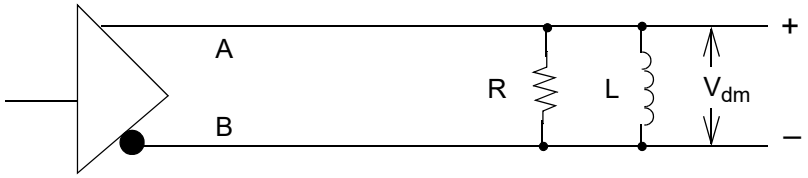


Figure 7–11—Differential output voltage, loaded

For drivers on either the CO or CI circuits, the first transition or the last positive going transition may occur asynchronously with respect to the timing of the following transitions or the preceding transition(s), respectively.

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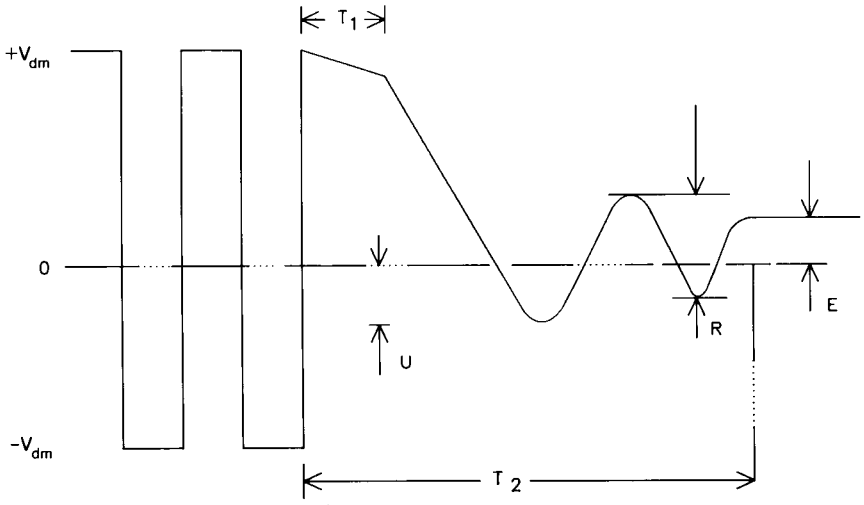

T1 = 200 ns MINIMUM
T2 = 80 BIT TIMES MAXIMUM
U = −100 mV MAXIMUM UNDERSHOOT
E = STEADY STATE OFFSET INTO SPECIFIED TEST LOAD
+/− 40 mV MAX
+/− 4 mA MAX
R = RINGING SHALL BE <200 mV PK−PK
AFTER T1 AND BEFORE T2

Figure 7–12—Generalized driver waveform

7.4.1.2 Requirements after idle

When the driver becomes nonidle after a period of idle on the interface circuit, the differential output voltage at the interface connector shall meet the requirements of 7.4.1.1 beginning with the second bit transmitted.The first bit sent over the driver circuit may contain phase violations or invalid data.

7.4.1.3 AC common-mode output voltage

The magnitude of the ac component of the common-mode output voltage of the driver, measured between the midpoint of a test load consisting of a pair of matched 39 Ω ± 1% resistors and circuit VC, as shown in Figure 7–13, shall not exceed 2.5 V peak from 30 Hz to 40 kHz and 160 mV peak from 40 kHz to BR.

7.4.1.4 Differential output voltage, open circuit

The differential output voltage into an open circuit, measured at the interface connector of the driving unit, shall not exceed 13 V peak.

7.4.1.5 DC common-mode output voltage

The magnitude of the dc component of the common-mode output voltage of the driver, measured between the midpoint of a test load consisting of a pair of matched 39 Ω ± 1% resistors and circuit VC, as shown in Figure 7–13, shall not exceed 5.5 V.

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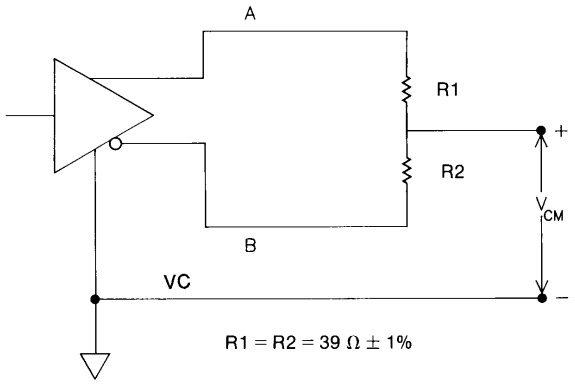
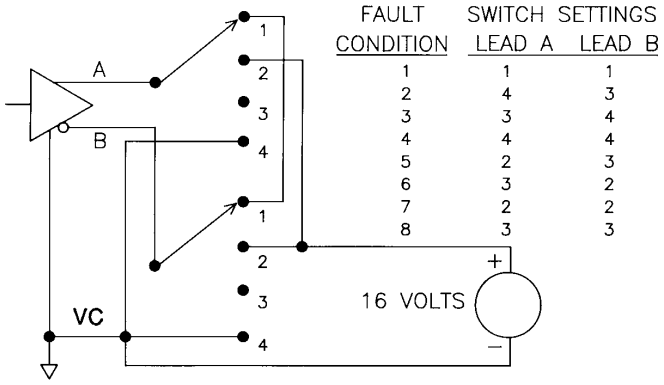


Figure 7–13—Common-mode output voltage

7.4.1.6 Fault tolerance

Any single driver in the interface, when idle or driving any permissible signal, shall tolerate the application of each of the faults specified by the switch settings in Figure 7–14 indefinitely; and after the fault condition is removed, the operation of the driver, according to the specifications of 7.4.1.1 through 7.4.1.5, shall not be impaired.

In addition, the magnitude of the output current from either output of the driver under any of the fault conditions specified shall not exceed 150 mA.



FAULT CONDITION	SWITCH SETTINGS LEAD A	LEAD B
1	1	1
2	4	3
3	3	4
4	4	4
5	2	3
6	3	2
7	2	2
8	3	3

Figure 7–14—Driver fault conditions

7.4.2 Receiver characteristics

The receiver specified terminates the interface cable in its characteristic impedance. The receiver shall function normally over the specified dc and ac common-mode ranges.

7.4.2.1 Receiver threshold levels

When the receiving interface circuit at the interface connector of the receiving equipment is driven by a differential input signal at either BR or BR/2 meeting the frequency and duty cycle tolerances specified for the receiving circuit, when the A lead is 160 mV positive with respect to the B lead, the interface circuit is in the HI state, and when the A lead is 160 mV negative with respect to the B lead, the interface circuit is in the

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LO state. The receiver output shall assume the intended HI and LO states for the corresponding input conditions.

If the receiver has a squelch feature, the specified receive threshold levels apply only when the squelch is allowing the signal to pass through the receiver.

NOTE—The specified threshold levels do not take precedence over the duty cycle and jitter tolerance specified elsewhere. Both sets of specifications have to be met.

7.4.2.2 AC differential input impedance

The ac differential input impedance for AUI receivers located in MAUs shall have a real part of 77.83 Ω ± 6%, with the sign of the imaginary part positive, and the phase angle of the impedance in degrees less than or equal to 0.0338 times the real part of the impedance, when measured with a 10 MHz sine wave.

The ac differential input impedance for AUI receivers located in the DTE shall have a real part of 77.95 Ω ± 6%, with the sign of the imaginary part positive, and the phase angle of the impedance in degrees less than or equal to 0.0183 times the real part of the impedance, when measured with a 10 MHz sine wave.

A 78 Ω ± 6% resistor in parallel with an inductance of greater than 27 μH or 50 μH for receivers in the MAU and DTE respectively, satisfies this requirement.

7.4.2.3 AC common-mode range

When the receiving interface circuit at the receiving equipment is driven by a differential input signal at either BR or BR/2 meeting the frequency and duty cycle tolerances specified for the circuit being driven, the receiver output shall assume the proper output state as specified in 7.4.2.1, in the presence of a peak common-mode ac sine wave voltage either of from 30 Hz to 40 kHz referenced to circuit VC in magnitude from 0 V to 3 V, or in magnitude 0 V to 200 mV for ac voltages of from 40 kHz to BR as shown in Figure 7–15.

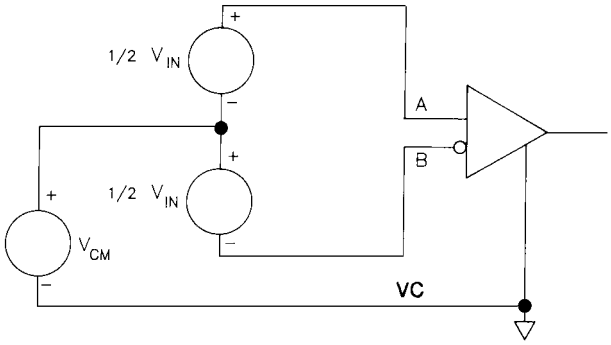

Figure 7–15—Common-mode input test

7.4.2.4 Total common-mode range

When the receiving interface circuit at the receiving equipment is driven by a differential input signal at either BR or BR/2 meeting the frequency and duty cycle tolerances specified for the circuit being driven, the receiver output shall assume the intended output state as specified in 7.4.2.1 in the presence of a total common-mode voltage, dc plus ac, referenced to circuit VC in magnitude from 0 V to 5.5 V, as shown in the test setup of Figure 7–15. The ac component shall not exceed the requirements of 7.4.2.3.

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The receiver shall be so designed that the magnitude of the current from the common-mode voltage source used in the test shall not exceed 1 mA.

7.4.2.5 Idle input behavior

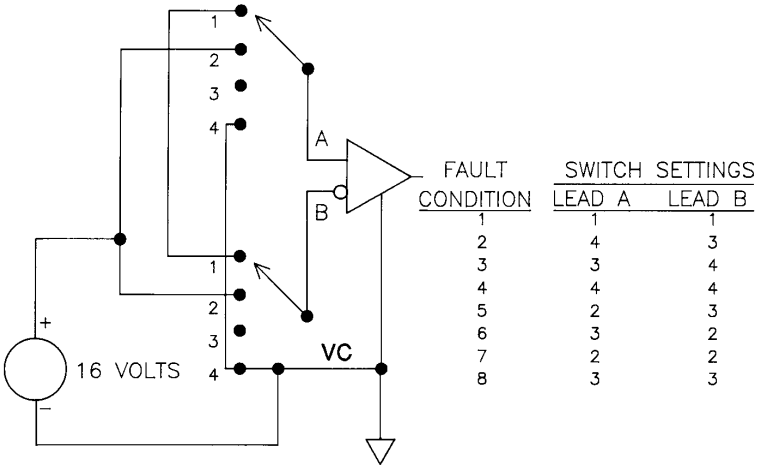
When the receiver becomes nonidle after a period of idle on the interface circuit, the characteristics of the signal at the output of the receiver shall stabilize within the startup delay allowed for the device incorporating the receiver so that it is not prevented from meeting the jitter specifications established for that device.

The receiving unit shall take precautions to ensure that a HI to idle transition is not falsely interpreted as an idle to nonidle transition, even in the presence of signal droop due to AC-coupling in the interface driver or receiver circuits.

7.4.2.6 Fault tolerance

Any single receiver in the interface shall tolerate the application of each of the faults specified by the switch settings in Figure 7–16 indefinitely, and after the fault condition is removed, the operation of the receiver according to the specifications of 7.4.2.1 through 7.4.2.6 shall not be impaired.

In addition, the magnitude of the current into either input of the receiver under any of the fault conditions specified shall not exceed 3 mA.



FAULT CONDITION	SWITCH SETTINGS LEAD A	LEAD B
1	1	1
2	4	3
3	3	4
4	4	4
5	2	3
6	3	2
7	2	2
8	3	3

Figure 7–16—Receiver fault conditions

7.4.3 AUI cable characteristics

The interface cable consists of individually shielded twisted pairs of wires with an overall shield covering these individual shielded wire pairs. These shields have to provide sufficient shielding to meet the requirements of protection against rf interference and the following cable parameters. Individual shields for each signal pair are electrically isolated from the outer shield but not necessarily from each other.

The overall shield shall be returned to the MAU and DTE Units via the AUI connector shell as defined in 7.6.2 and 7.6.3. If a common drain wire is used for all the signal pair shields, then it shall be connected to pin 4 and pin 1. Individual drain wire returns for each signal pair may be used (see 7.6.3). It is recommended that individual drain wires be used on all control and data circuit shields to meet satisfactory crosstalk levels.

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If individual drain wires are used, they shall be interconnected within the AUI cable at each end and shall be connected at least to pin 4 and pin 1 at each end of the cable.

The presence of the Control Out signal pair is optional. If driver or receiver circuit components for CO are not provided, consideration should be given to properly terminating the CO signal pair within the DTE and MAU to preclude erroneous operation.

7.4.3.1 Conductor size

The dc power pair in the interconnecting cable, voltage common and voltage minus, shall be composed of a twisted pair of sufficient gauge stranded wires to result in a nominal dc resistance not to exceed 1.75 Ω per conductor.

Conductor size for the signal pairs shall be determined according to the ac related parameters in 7.4.3.2 through 7.4.3.6.

7.4.3.2 Pair-to-pair balanced crosstalk

The balanced crosstalk from one pair of wires to any other pair in the same cable sheath (when each pair is driven per 7.4.1.1 through 7.4.1.5) shall have a minimum value of 40 dB of attenuation measured over the range of BR/2 to BR.

7.4.3.3 Differential characteristic impedance

The differential characteristic impedance for all signal pairs shall be equal within 3 Ω and shall be 78 Ω ± 5 Ω measured at a frequency of BR.

7.4.3.4 Transfer impedance

a) The common-mode transfer impedance shall not exceed the values shown in Figure 7–17 over the indicated frequency range.
b) The differential mode transfer impedance for all pairs shall be at least 20 dB below the common-mode transfer impedance.

7.4.3.5 Attenuation

Total cable attenuation levels between driver and receiver (at separate stations) for each signal pair shall not exceed 3 dB over the frequency range of BR/2 to BR (Hz) for sinewave measurements.

7.4.3.6 Timing jitter

Cable meeting this specification shall exhibit edge jitter of no more than 1.5 ns at the receiving end when the longest legal length of the cable as specified in 7.4.3.1 through 7.4.3.7 is terminated in a 78 Ω ± 1% resistor at the receiving end and is driven with pseudorandom Manchester encoded binary data from a data generator which exhibits no more than 0.5 ns of edge jitter on half bit cells of exactly 1/2 BT and whose output meets the specifications of 7.4.1.1 through 7.4.1.5. This test shall be conducted in a noise-free environment. The above specified component is not to introduce more than 1 ns of edge jitter into the system.

7.4.3.7 Delay

Total signal delay between driver and receiver (at separate stations) for each signal pair shall not exceed 257 ns.

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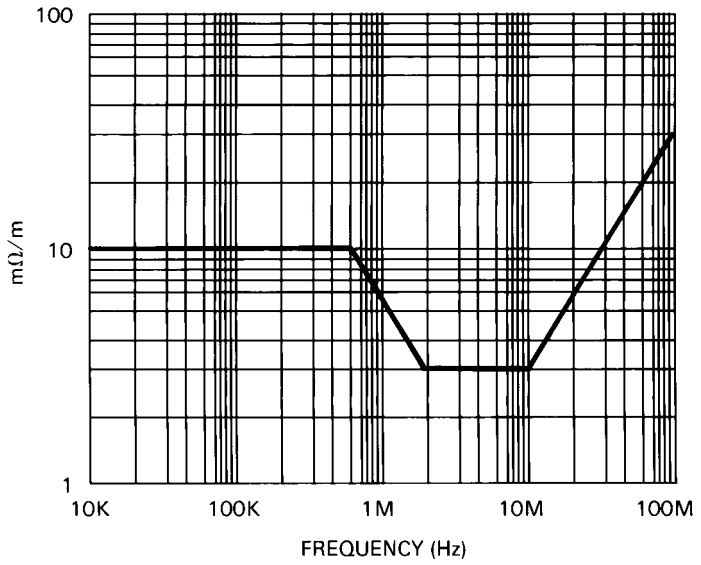

Figure 7–17—Common-mode transfer impedance

7.5 Functional description of interchange circuits

7.5.1 General

The AUI consists of either three or four differential signal circuits, power, and ground. Two of the circuits carry encoded data and two carry encoded control information. Circuits DO (Data Out) and CO (Control Out) are sourced by the DTE, and circuits DI (Data In) and CI (Control In) are sourced by the MAU. The interface also provides for power transfer from the DTE to the MAU. The CO circuit is optional.

7.5.2 Definition of interchange circuits

The following circuits are defined by this specification:

Circuit	Name	Signal direction		Remarks
		to MAU	from MAU	
DO	Data Out	X		Encoded Data
DI	Data In		X	Encoded Data
CO	Control Out	X		Encoded Control
CI	Control In		X	Encoded Control
VP	Voltage Plus	X		12 V
VC	Voltage Common	X		Return for VP
PG	Protective Ground	X		Shield

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7.5.2.1 Circuit DO–Data Out

The Data Out (DO) circuit is sourced by the DTE. It is a differential pair consisting of DO-A (Data Out circuit A) and DO-B (Data Out circuit B).

The signal transferred over this circuit is Manchester encoded. An *output* message containing a one bit is encoded as CD1. An *output_idle* message is encoded as an IDL.

The following symmetry requirements shall be met when the DTE transfers pseudorandom Manchester encoded binary data over a DO circuit loaded by the test load specified in 7.4.1.1.

Bit cells generated internal to the DTE are required to be 1 BT within the permitted tolerance on data rate specified in 7.3.2. Half bit cells in each data bit are the be exactly 1/2 BT (that is, the reference point for edge jitter measurements) within the permitted tolerance on the data rate specified in 7.3.2. Each transition on the DO circuit is permitted to exhibit edge jitter not to exceed 0.5 ns in each direction. This means that any transition may occur up to 0.5 ns earlier or later than this transition would have occurred had no edge jitter occurred on this signal.

7.5.2.2 Circuit DI–Data In

The Data In (DI) circuit is sourced by the MAU. It is a differential pair consisting of DI-A (Data In circuit A) and DI-B (Data In circuit B).

The signal transferred over this circuit is Manchester encoded. An *input* message containing a zero bit is encoded as CD0. An *input* message containing a one bit is encoded as CD1. An *input_idle* message is encoded as an IDL.

A DTE meeting this specification shall be able to receive, on the DI circuit without a detectable FCS error, normal preamble data arranged in legal length packets as sent by another station to the DTE. The test generator for the data on the DI circuit shall meet the requirements for drivers in MAUs specified in 7.4.1.1 through 7.4.1.5 and shall drive the DI circuit through a zero length AUI cable. Random amounts of edge jitter from 0 ns to 12 ns on either side of each transition shall be added by the test generator to transitions in bits in the preamble, and random amounts of edge jitter of from 0 ns to 18 ns on either side of each transition shall be added to the transitions in all bits in the frame. Preamble length from the test generator shall be 47 bits of preamble, followed by the 8 bit SFD.

NOTE—A significant portion of the system jitter may be nonrandom in nature and consists of a steady-state shift of the midbit transitions in either direction from their nominal placement. A 16.5 ns edge jitter is expected on the transmitted signal at the receiving DTE, worst case. The difference between 16.5 ns and 18 ns jitter represents receiver design margin.

7.5.2.3 Circuit CO–Control Out (optional)

The Control Out (CO) circuit is sourced by the DTE. It is a differential pair consisting of CO-A (Control Out circuit A) and CO-B (Control Out circuit B).

The signal transferred over this circuit is encoded as described in 7.3.1.2. A *mau_request* message is encoded as CS1. A *normal* message is encoded as IDL. An *isolate* message is encoded as CS0.

7.5.2.4 Circuit CI–Control In

The Control In (CI) circuit is sourced by the MAU. It is a differential pair consisting of CI-A (Control In circuit A) and CI-B (Control In circuit B).

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The signal transferred over this circuit is encoded as described in 7.3.1.2. A *mau_available* message is encoded as IDL. A *mau_not_available* message is encoded as CS1. A *signal_quality_error* message is encoded as a CS0.

7.5.2.5 Circuit VP–Voltage Plus

The Voltage Plus (VP) circuit is sourced from the DTE. It shall be capable of operating at one fixed level between + 12 V dc – 6% and + 15 V dc + 5% with respect to circuit VC at the DTE AUI for all currents from 0 to 500 mA. The source shall provide protection for this circuit against an overload condition. The method of overload protection is not specified; however, under no conditions of operation, either normal or overload, shall the source apply a voltage to circuit VP of less than 0 or greater than + 15.75 V dc as specified above. MAU designers are cautioned that protection means employed by power sources may cause the voltage at signal VP to drop below the minimum operational voltage specified without going completely to zero volts when loads drawing in excess of the current supplied are applied between VP and VC. Adequate provisions shall be made to ensure that such a condition does not cause the MAU to disrupt the medium.

7.5.2.6 Circuit VC–Voltage Common

Circuit VC is the ground return to the power source for circuit VP, capable of sinking 2.0 A. Also, all common-mode terminators for AUI circuits shall be made to circuit VC.

7.5.2.7 Circuit PG–Protective Ground

Circuit PG shall be connected to chassis ground through a maximum dc resistance of 20 mΩ at the DTE end.

7.5.2.8 Circuit shield terminations

Individual pin terminations shall meet the following requirements:

a) Pins 1, 4, 8, 11, 14 connected to logic ground in the DTE
b) Pins 1, 4, 8, 11, 14 capacitively coupled to VC in MAU
c) Impedance to ground < 5 Ω at the lowest operational BR/2 in the MAU and at the highest BR in the DTE

7.6 Mechanical characteristics

7.6.1 Definition of mechanical interface

All connectors used shall be as specified in 7.6.2. The DTE shall have a female connector and the MAU shall have a male connector. The MAU may be plugged directly into the DTE or may be connected by one or more cable segments whose total length is less than or equal to 50 m. All cable segments shall have a male connector on one end and a female connector on the other end. All female connectors shall have the slide latch, and all male connectors shall have the locking posts (as defined in Figure 7–18, Figure 7–19, and Figure 7–20) as the retention system.

7.6.2 Line interface connector

A 15-pole connector having the mechanical mateability dimensions as specified in IEC 60807-2 with gold-plated contacts shall be used for the line interface connector. The shells of these connectors shall be tin plated to ensure the integrity of the cable shield to chassis current path. The resistance of the cable shield to equipment chassis shall not exceed 5 mΩ, after a minimum of 500 cycles of mating and unmaking.

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In order to ensure intermateability of connectors obtained from different manufacturers, the connector with female contacts shall conform to IEC 60807-2 and have gold-plated contacts and tin-plated shells. All additions to provide for female shell to male shell conductivity shall be on the shell of the connector with male contacts. There should be multiple contact points around the sides of this shell to provide for shield continuity.

NOTE—Use of similar metallic surfaces on connector conductors and similar metallic surfaces on the connector shells minimizes galvanic action and reduced performance.

The connector is not specified to prevent operator contact with the shield, and precautions shall be taken at installation time to ensure that the installer is warned that the shield is not to be brought into contact with any hazardous voltage while being handled by operating personnel. See reference [B54].

7.6.3 Contact assignments

The following table shows the assignment of circuits to connector contacts.

Contact	Circuit	Use
3	DO-A	Data Out circuit A
10	DO-B	Data Out circuit B
11	DO-S	Data Out circuit shield
5	DI-A	Data In circuit A
12	DI-B	Data In circuit B
4	DI-S	Data In circuit shield
7	CO-A	Control Out circuit A
15	CO-B	Control Out circuit B
8	CO-S	Control Out circuit shield
2	CI-A	Control in circuit A
9	CI-B	Control In circuit B
1	CI-S	Control In circuit shield
6	VC	Voltage Common
13	VP	Voltage Plus
14	VS	Voltage Shield
Shell	PG	Protective Ground (Conductive Shell)

NOTE—Voltage Plus and Voltage Common use a single twisted pair in the AUI cable.

As indicated in 7.4.2.1, the A lead of a circuit is positive relative to the B lead for a HI signal and negative for a LO signal.

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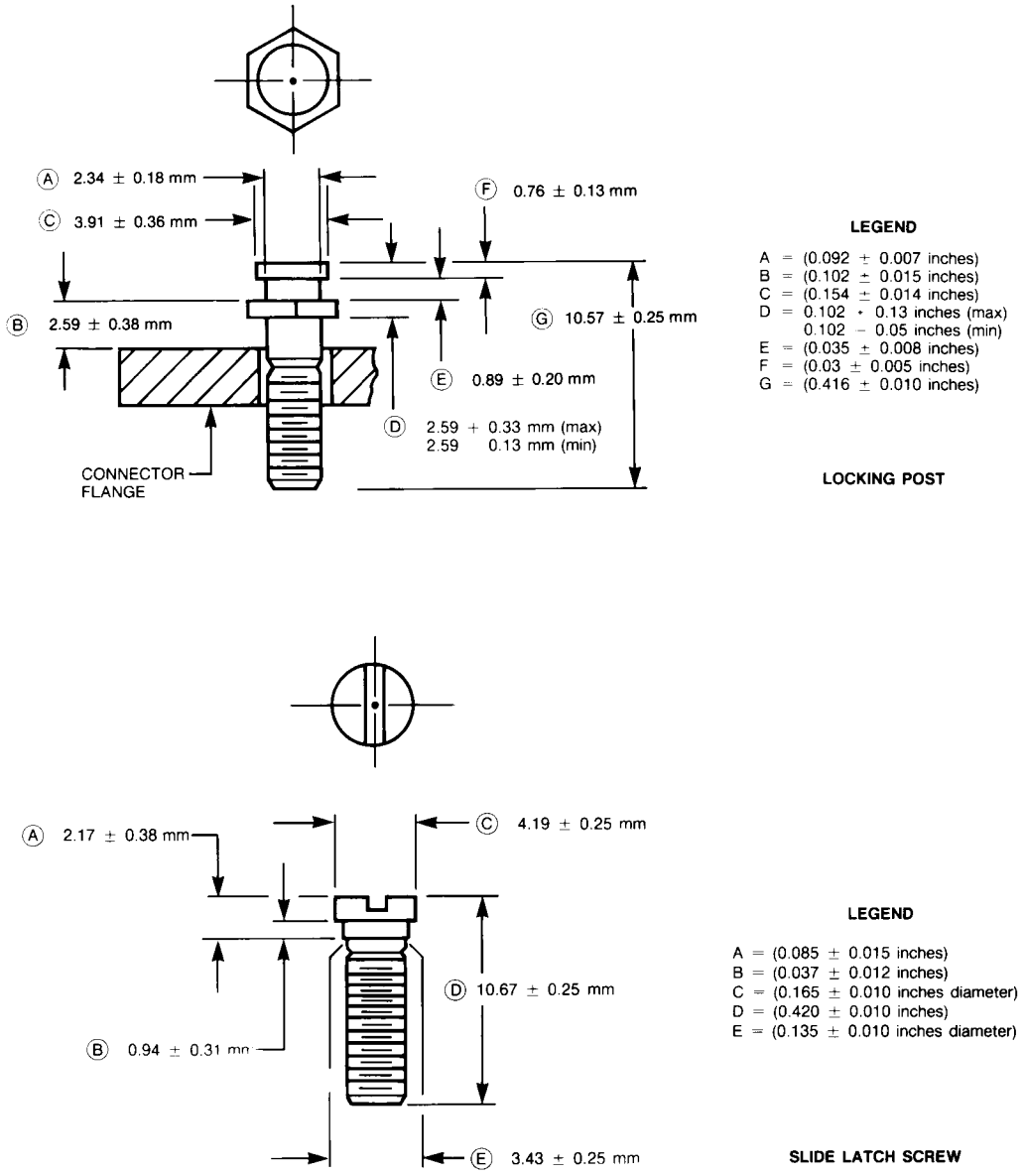

Figure 7–18—Connector locking posts

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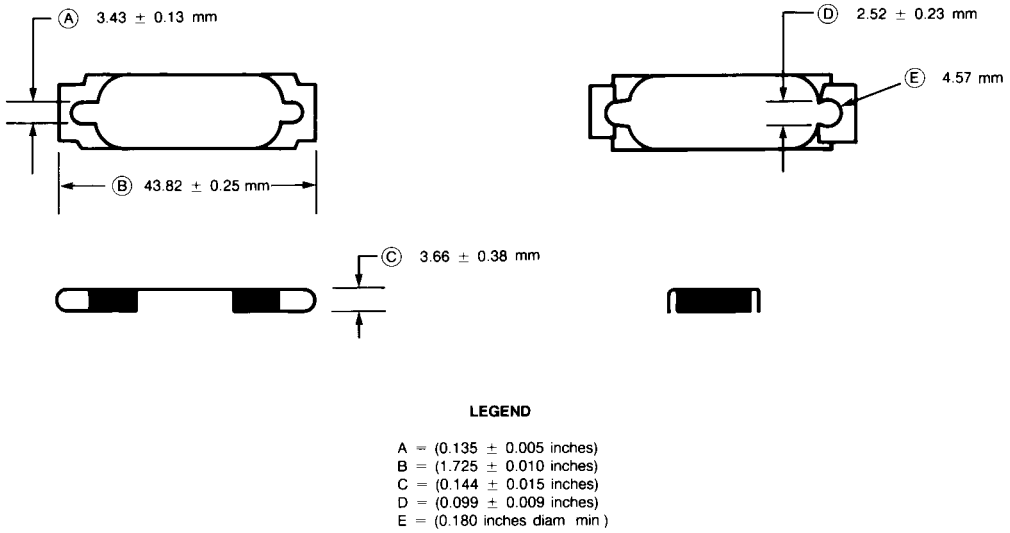

Figure 7–19—Connector slide latch

(material 24 gauge maximum)

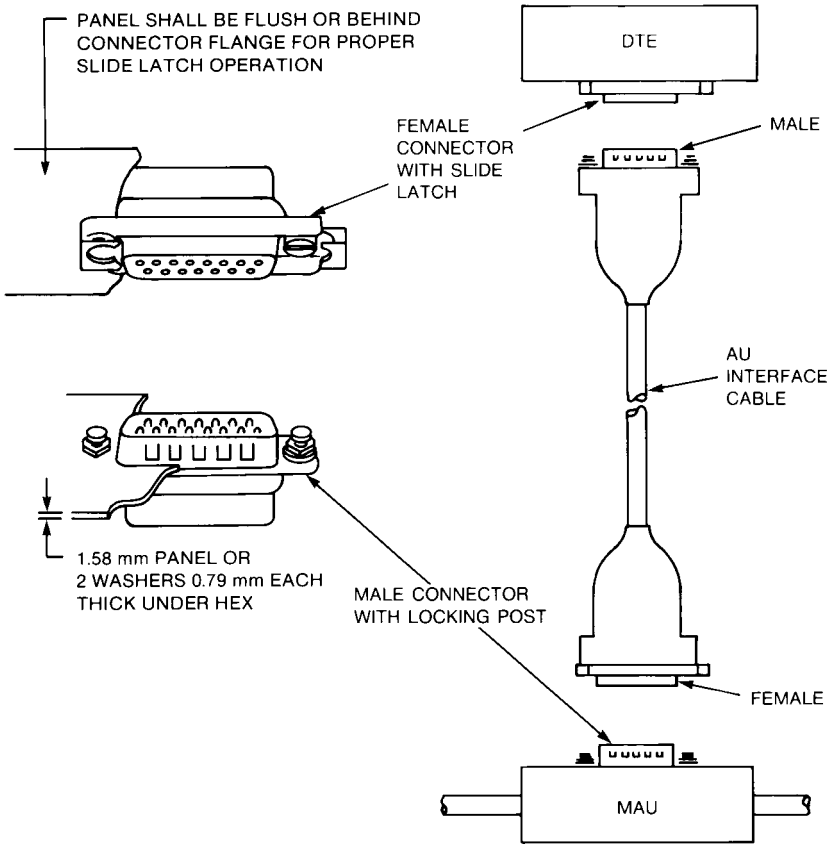

Figure 7–20—Connector hardware and AUI cable configuration

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8. Medium Attachment Unit and baseband medium specifications, type 10BASE5

NOTE—This MAU is not recommended for new installations. Since September 2003, maintenance changes are no longer being considered for this clause.

8.1 Scope

8.1.1 Overview

This standard defines the functional, electrical, and mechanical characteristics of the MAU and one specific medium for use with local networks. The relationship of this specification to the entire ISO/IEC Local Network International Standard is shown in Figure 8–1. The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the local network medium.

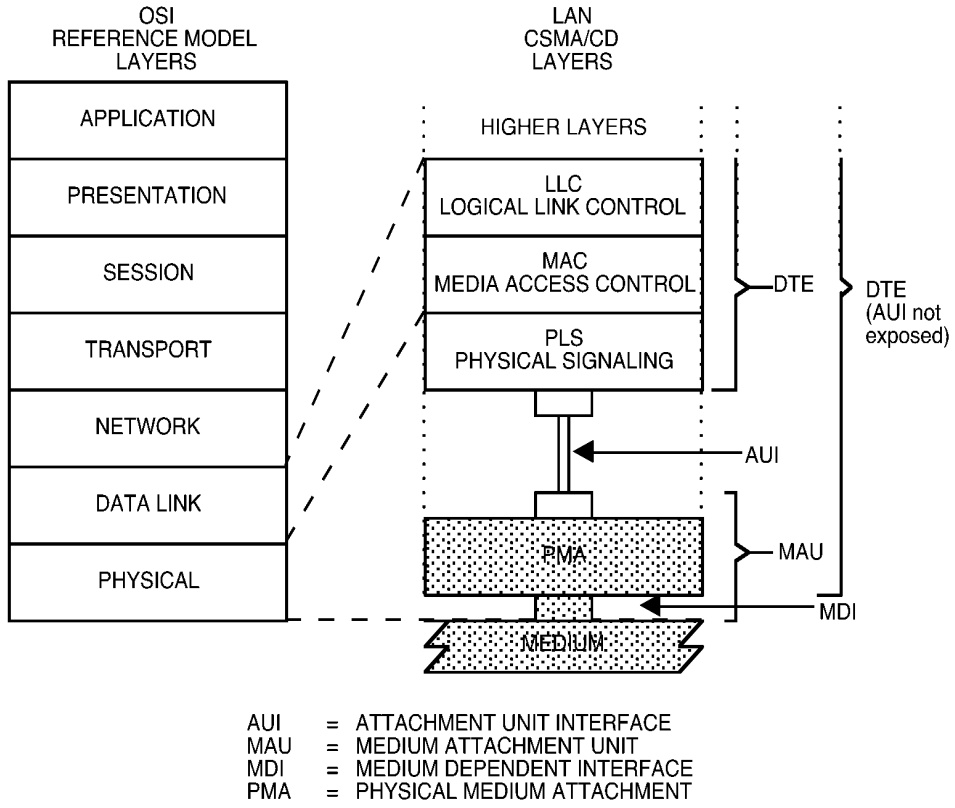

Figure 8–1—Physical Layer partitioning, relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

8.1.1.1 Medium Attachment Unit

The MAU has the following general characteristics:

a) Enables coupling the PLS by way of the AUI to the explicit baseband coaxial transmission system defined in this clause of the standard.
b) Supports message traffic at a data rate of 10 Mb/s (alternative data rates may be considered in future additions to the standard).
c) Provides for driving up to 500 m of coaxial trunk cable without the use of a repeater.
d) Permits the DTE to test the MAU and the medium itself.

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e) Supports system configurations using the CSMA/CD access mechanism defined with baseband signaling.
f) Supports a bus topology interconnection means.

8.1.1.2 Repeater unit

The repeater unit is used to extend the physical system topology, has the same general characteristics as defined in 8.1.1.1, and provides for coupling together two or more 500 m coaxial trunk cable segments. Multiple repeater units are permitted within a single system to provide a maximum trunk cable connection path of 2.5 km between any two MAUs.

8.1.2 Definitions

See 1.4.

8.1.3 Application perspective: MAU and MEDIUM objectives

This subclause states the broad objectives and assumptions underlying the specifications defined throughout this subclause of the standard.

8.1.3.1 Object

a) Provide the physical means for communication between local network data link entities.

NOTE—This standard covers a portion of the Physical Layer as defined in the OSI Reference Model and, in addition, the physical medium itself, which is beyond the scope of the OSI Reference Model.

b) Define a physical interface that can be implemented independently among different manufacturers of hardware and achieve the intended level of compatibility when interconnected in a common local network.
c) Provide a communication channel capable of high bandwidth and low bit error ratio performance. The resultant mean bit error ratio, at the Physical Layer service interface should be less than one part in 10^8 (on the order of one part in 10^9 at the link level).
d) Provide for ease of installation and service.
e) Provide for high network availability (ability of a station to gain access to the medium and enable the data link connection in a timely fashion).
f) Enable relatively low-cost implementations.

8.1.3.2 Compatibility considerations

All implementations of this baseband coaxial system shall be compatible at the MDI.

This standard provides one explicit trunk cable medium specification for the interconnection of all MAU devices. The medium itself, the functional capability of the MAU, and the AUI are defined to provide the highest possible level of compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the MAU in an application-dependent manner provided the MD Interface and AUI specifications are satisfied.

Subsystems based on this specification may be implemented in several different ways provided compatibility at the medium is maintained. It is possible, for example, to design an integrated station where the MAU is contained within a physical DTE system component, thereby eliminating the AUI cable. The device designer (and system user) shall then consider such factors as topological flexibility, system availability, and configurability.

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8.1.3.3 Relationship to PLS and AU interface

This subclause defines the primary Physical Layer for the LAN, a layer composed of both the physical medium and the rudimentary circuitry necessary to couple a station's message path directly to/from the medium. The complete logical Physical Layer of the LAN may reside physically in two distinct locations, the MAU and the DTE. Therefore, a close relationship exists between this subclause and Clause 7. This subclause specifies all of the physical medium parameters, all of the PMA logical functions residing in the physical MAU, and references the AUI associated with and defined throughout Clause 7.

NOTE—The design of a physical MAU component requires the use of both this subclause and Clause 7 for the PLS and AUI specifications.

8.1.3.4 Modes of operation

The MAU is capable of operating in either a "Normal" mode or an optional "Monitor" mode.

a) *Normal mode.* The MAU functions as a direct connection between the baseband medium and the DTE. Data output from the DTE is output to the coaxial trunk medium and all data on the coaxial trunk medium is input to the DTE. This mode is the "normal" mode of operation for the intended message traffic between stations.
b) *Monitor mode.* The MAU Transmit function is disabled to prevent data from being output on the trunk coaxial medium while the receive function and collision presence function remain active for purposes of monitoring medium message traffic. This mode also serves as a limited test mode at the same time it isolates the MAU transmitter from the medium. Under most local (that is, intrastation) fault conditions the monitor mode enables continued use of the network while the local station is being serviced.

8.2 MAU functional specifications

The MAU component provides the means by which signals on the four physically separate AUI signal circuits to/from the DTE and their associated interlayer messages are coupled to the single coaxial cable baseband signal line. To achieve this basic objective, the MAU component contains the following functional capabilities to handle message flow between the DTE and the baseband medium:

a) *Transmit function.* The ability to transmit serial data bit streams on the baseband medium from the local DTE entity and to one or more remote DTE entities on the same network.
b) *Receive function.* The ability to receive serial data bit streams over the baseband medium.
c) *Collision Presence function*. The ability to detect the presence of two or more stations' concurrent transmissions.
d) *Monitor function* (Optional). The ability to inhibit the normal transmit data stream to the medium at the same time the normal receive function and collision presence function remain operational.
e) *Jabber function.* The ability to automatically interrupt the transmit function and inhibit an abnormally long output data stream.

8.2.1 MAU Physical Layer functions

8.2.1.1 Transmit function requirements

At the start of a frame transmission on the coaxial cable, no more than 2 bits (2 full bit cells) of information may be received from the DO circuit and not transmitted onto the coaxial medium. In addition, it is permissible for the first bit sent to contain encoded phase violations or invalid data; however, all successive bits of the frame shall be reproduced with no more than the specified amount of jitter. The second bit cell transmitted onto the coaxial cable shall be carried from the DO signal line and transmitted onto the coaxial trunk

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cable medium with the correct timing and signal levels. The steady-state propagation delay between the DO circuit receiver input and the coaxial cable output shall not exceed one-half bit cell. At the start of transmission, the MAU bit loss plus steady-state propagation delay between the DO and the coaxial cable shall vary by less than 2 bits between successive packets separated by 96 bit times or less. There shall be no logical signal inversions between the branch cable DO circuit and the coaxial trunk cable (for example, a “high” logic level input to the MAU shall result in the less negative current flow value on the trunk coaxial medium). A positive signal on the A signal lead of the DO circuit shall result in a more positive voltage level on the trunk coaxial medium. It is assumed that the AUI shall provide adequate protection against noise. It is recommended that the designer provide an implementation in which a minimum threshold signal is required to establish a transmit bit stream.

The Transmit function shall output a signal on the trunk coaxial medium whose levels and waveform comply with 8.3.1.3.

In addition, when the DO circuit has gone idle after a frame is output, the MAU shall then activate the collision presence function as close to the trunk coaxial cable as possible without introducing an extraneous signal on the trunk coaxial medium. The MAU shall initiate the collision presence state within 0.6 μs to 1.6 μs after the start of the output idle signal and shall maintain an active collision presence state for a time equivalent to 10 bit cells ± 5 bit cells.

8.2.1.2 Receive function requirements

The signal from the coaxial trunk cable shall be directly coupled to the receiver and subsequently AC-coupled before reaching the receive circuit connected to the DTE. The receive function shall output a signal onto the DI circuit of the AUI cable that complies with the AUI specification for drivers in MAUs.

At the start of a frame reception from the coaxial cable, no more than 5 bits (five full bit cells) of information may be received from the coaxial cable and not transmitted onto the receive (DI) circuit. In addition, it is permissible for the first bit sent over the receive circuit to contain encoded phase violations or invalid data; however, all successive bits of the frame shall reproduce the incoming signal with no more than the above specified amount of jitter. This implies that the second bit cell sent onto the DI circuit presents valid data to the branch cable. The steady-state propagation delay between the coaxial cable and the receive (DI) circuit output shall not exceed one-half bit cell. At the start of reception, the MAU bit loss plus steady-state propagation delay between the coaxial cable and the DI circuit shall vary by less than 5 bits between successive packets separated by 96 bit times or less when the signal level on the coaxial cable is constant (that is, when both packets are transmitted by the same MAU). There are no logical signal inversions between the coaxial (trunk) cable and the MAU (branch) cable receive circuit.

A MAU meeting this specification shall exhibit edge jitter into the DI pair when terminated in the appropriate test load specified in 7.4.3.6, of no more than 8.0 ns in either direction when it is installed on the distant end of all lengths between 2.5 m and 500 m of the cable specified in 8.4.1.1 through 8.4.2.1.5 terminated at both ends with terminators meeting the impedance requirements of 8.5.2.1 and driven at one end with pseudorandom Manchester encoded binary data from a data generator that exhibits no more than 1.0 ns of edge jitter in either direction on half-bit cells of exactly 1/2 BT and whose output meets the specifications of 8.3.1.3 except that the risetime of the signal has to be 30 ns + 0, – 2 ns. This test shall be conducted in a noise-free environment. The combination of coaxial cable and MAU receiver introduce no more than 6 ns of edge jitter into the system.

The local transmit and receive functions shall operate simultaneously while connected to the medium operating in the half duplex operating mode.

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8.2.1.3 Collision Presence function requirements

The signal presented to the CI circuit in the absence of a collision shall be the IDL signal except when the MAU is required to signal the CS1 signal.

The signal presented to the CI circuit during the presence of a collision shall be the CS0 signal encoded as specified in 7.3.1.2. Under no conditions shall the collision presence function generate an output when only one MAU is transmitting. Table 8–1 summarizes the allowable conditions under which collisions shall be detected.

a) Collision Assertion
   1) In the case where the MAU has been transmitting for at least 20 bit times before the arrival at the MAU on the coaxial cable of a transmission from another MAU, the CS0 signal shall be presented to the CI circuit no more than 17 bit times after the arrival at the MAU on the MDI of a transmission from another MAU. Arrival at the MAU shall be considered to be the time when the transmission of the other MAU causes the dc level on the MDI to become more negative.
   2) In all other cases where the MAU is transmitting, the CS0 signal shall be presented to the CI circuit no more than 29 bit times after the later of start of transmission by the MAU and the arrival of a transmission from another MAU.

b) Collision De-assertion
   1) In the case where a collision has occurred between the MAU and one other MAU, the IDL signal shall be presented to the CI circuit no more than 17 bit times after either the end of transmission by the MAU or the arrival of the end of transmission from the other MAU, whichever occurs earlier. The arrival of the end of transmission from the other MAU shall be the time when the cessation of transmission causes the dc level on the MDI to become less negative.
   2) In the case where a collision has occurred between more than two MAUs, the IDL signal shall be presented to the CI circuit no more than 29 bit times after the arrival of the end of transmission from all but one MAU.

These timing conditions shall be met for all data bit patterns and combinations of MDI, MAU transmit levels, and MAU locations on the segment.

The collision presence function may, in some implementations, be able to sense an abnormal (for example, open) medium.

Table 8–1—Generation of collision presence signal

MAU	Numbers of transmitters		
	<2	=2	>2
Transmitting	N	Y	Y
Not transmitting	N	Y	Y
Y= shall generate SQE message N= shall not generate SQE message			

8.2.1.4 Monitor function requirements (optional)

Upon receipt of the *isolate* message the MAU shall, within 20 ms (implementations: solid-state preferred, relay switched permitted), disable the transmit function in such a way as to prevent both the transmission of signals on the trunk coaxial medium and any abnormal loading by the disabled transmitter on the trunk coaxial medium itself. The monitor function is intended to prevent a malfunctioning active component (for example, transmit driver) from bringing down the network. The *isolate* message shall not interact with the

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receive or collision presence functions, thus permitting the normal operational mode wherein all data appearing on the trunk coaxial medium are carried to the DTE on the DI signal circuit.

NOTE—Verification for successful execution of the *isolate* message requires use of the trunk coaxial medium itself. This level of guaranteed performance requires use of system layers above the Physical Layer and implies some interruption of normal trunk coaxial medium message traffic.

8.2.1.5 Jabber function requirements

The MAU shall contain a self-interrupt capability to inhibit transmit data from reaching the medium. Hardware within the MAU (with no external message other than the detection of output data, bits, or leakage, by way of the transmit function) shall provide a nominal window of at least 20 ms to at most 150 ms during which time a normal data link frame may be transmitted. If the frame length exceeds this duration, the jabber function shall inhibit further output data from reaching the medium.

When the transmit function has been positively disabled, the MAU shall then activate the collision presence function as close to the trunk coaxial medium as possible without introducing an extraneous signal on the trunk coaxial medium. A MAU without the monitor function may reset the jabber and collision presence functions on power reset. Alternatively, a MAU without the monitor function may reset these functions after a period of 0.5 s ± 50% if the monitor function has not been implemented. If the monitor function has been implemented then it shall be used to reset the collision presence and jabber functions.

8.2.2 MAU interface messages

8.2.2.1 DTE Physical Layer to MAU Physical Layer messages

The following messages can be sent by the DTE Physical Layer entities to the MAU Physical Layer entities:

Message	Circuit	Signal	Meaning
output	DO	CD1, CD0	Output information
output_idle	DO	IDL	No data to be output
normal	CO	IDL	Assume the nonintrusive state on the trunk coaxial medium
(Optional circuit)			
isolate	CO	CS0(BR)	Positively disable the trunk coaxial medium transmitter

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8.2.2.2 MAU Physical Layer to DTE Physical Layer

The following messages can be sent by the MAU Physical Layer entities to the DTE Physical Layer entities:

Message	Circuit	Signal	Meaning
input	DI	CD1, CD0	Input information
input_idle	DI	IDL	No information to be input
mau_available	CI	IDL	MAU is available for output
signal_quality_error	CI	CS0	Error detected by MAU

8.2.2.2.1 *input* message

The MAU Physical Layer sends an *input* message to the DTE Physical Layer when the MAU has a bit of data to send to the DTE. The physical realization of the input message is a CD0 or CD1 sent by the MAU to the DTE on the data in circuit. The MAU sends CD0 if the *input* bit is a zero or CD1 if the *input* bit is a one. No retiming of the CD1 or CD0 signals takes place within the MAU.

8.2.2.2.2 *input_idle* message

The MAU Physical Layer sends an *input_idle* message to the DTE Physical Layer when the MAU does not have data to send to the DTE. The physical realization of the *input_idle* message is the IDL signal sent by the MAU to the DTE on the data in circuit.

8.2.2.2.3 *mau_available* message

The MAU Physical Layer sends the *mau_available* message to the DTE Physical Layer when the MAU is available for output. The *mau_available* message is always sent by a MAU that is always prepared to output data unless the *signal_quality_error* message shall be sent instead. Such a MAU does not require *mau_request* to prepare itself for data output. The physical realization of the *mau_available* message is an IDL signal sent by the MAU to the DTE on the control in circuit.

8.2.2.2.4 *signal_quality_error* message

The *signal_quality_error* message shall be implemented in the following fashion:

a) The *signal_quality_error* message shall not be sent by the MAU if no MAU or only one MAU is transmitting on the trunk coaxial medium in the normal mode.
b) If two or more remote MAUs are transmitting on the trunk coaxial medium, but the MAU connected to the local node is not transmitting, then the local MAU shall send the *signal_quality_error* message.
c) When the local MAU is transmitting on the trunk coaxial medium, all occurrences of one or more additional MAUs transmitting shall cause the *signal_quality_error* message to be sent by the local MAU to its DTE.
d) When the MAU has completed each output frame it shall perform an SQE test sequence, as defined in Figure 8–2 and Figure 8–3.
e) When the MAU has inhibited the transmit function it shall send the *signal_quality_error* message in accordance with the jabber function requirements of 8.2.1.5.

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The physical realization of the *signal_quality_error* message is the CS0 signal sent by the MAU to the DTE on the control in circuit. See 8.2.1.3 for timing requirements on the assertion and de-assertion of the CS0 signal in a collision.

Note that the MAU is required to assert the *signal_quality_error* message at the appropriate times whenever the MAU is powered and not just when the DTE is providing output data.

8.2.3 MAU state diagrams

The state diagrams, Figure 8–2 (a–d), Figure 8–3, and Figure 8–4, depict the full set of allowed MAU state functions relative to the control circuits of the DTE-MAU interface for MAUs without conditioning requirements. Messages used in these state diagrams are explained below:

a) *positive_disable.* Activates the positive means provided in the MAU transmitter to prevent interference with the trunk coaxial medium.
b) *enable_driver.* Activates the path employed during normal operation to cause the MAU transmitter to impress data onto the trunk coaxial medium.
c) *disable_driver.* Deactivates the path employed during normal operation to cause the MAU transmitter to impress data onto the trunk coaxial medium.
d) *no_collision.* Signifies that the condition of multiple transmitters simultaneously active on the trunk coaxial medium does not exist.
e) *collision.* Signifies that the condition of multiple transmitters simultaneously active on the trunk coaxial medium does exist.
f) *not_positive_disable.* Deactivates the positive means provided in the MAU transmitter to prevent interference with the trunk coaxial medium.

When no state is asserting the message *signal_quality_error*, the message *MAU_input_idle* is sent.

8.3 MAU–medium electrical characteristics

8.3.1 MAU-to-coaxial cable interface

The following subclauses describe the interface between the MAU and the coaxial cable. Negative current is defined as current into the MAU (out of the center conductor of the cable).

8.3.1.1 Input impedance

The shunt capacitance presented to the coaxial cable by the MAU circuitry (not including the means of attachment to the coaxial cable) is recommended to be no greater than 2 pF. The resistance to the coaxial cable shall be greater than 100 kΩ.

The total capacitive load due to MAU circuitry and the mechanical connector as specified in 8.5.3.2 shall be no greater than 4 pF.

These conditions shall be met in the power-off and power-on, not transmitting states (over the frequencies BR/2 to BR).

The magnitude of the reflection from a MAU shall not be more than that produced by a 4 pF capacitance when measured by both a 25 ns rise time and 25 ns fall time waveform. This shall be met in both the power on and power off, not transmitting states.

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8.3.1.2 Bias current

The MAU shall draw (from the cable) between +2 μA and –25 μA in the power-off and the power-on, not transmitting states.

8.3.1.3 Coaxial cable signaling levels

The signal on the coaxial cable due to a single MAU as measured at the MAU transmitter output is composed of an ac component and an offset component. Expressed in terms of current immediately adjacent to the MAU connection (just prior to splitting the current flow in each direction) the signal has an offset component (direct current including the effects of timing distortion) of from –37 mA minimum to –45 mA maximum and an ac component from +28 mA up to the offset value.

The current drive limit shall be met even in the presence of one other MAU transmitter. A MAU shall be capable of maintaining at least 2.2 V of average dc level on the coaxial cable in the presence of two or more other MAUs transmitting concurrently. The MAU shall, in addition, sink no more than ±250 μA when the voltage on the center conductor of the cable drops to –10 V when the MAU is transmitting.

The MAU shall sink no more than –25 μA when the voltage on the center conductor of the cable drops to –7 V when the MAU is transmitting.

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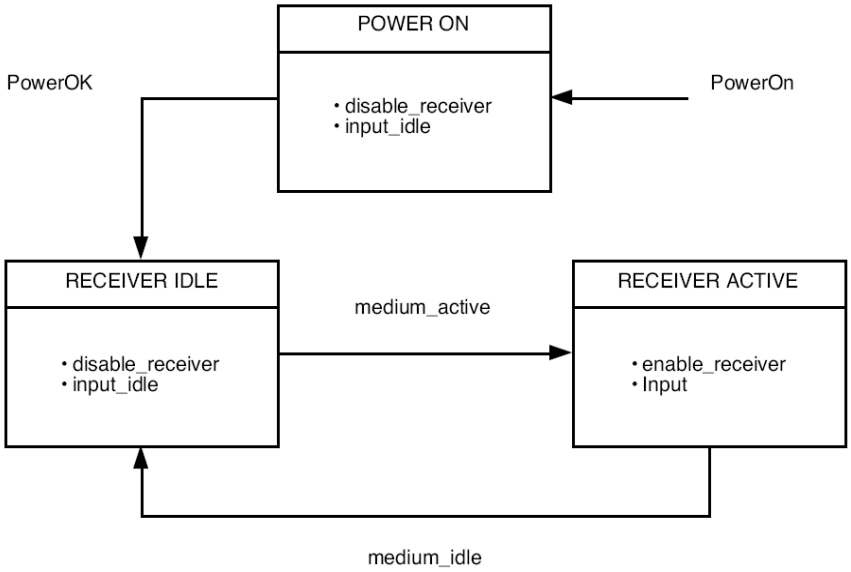
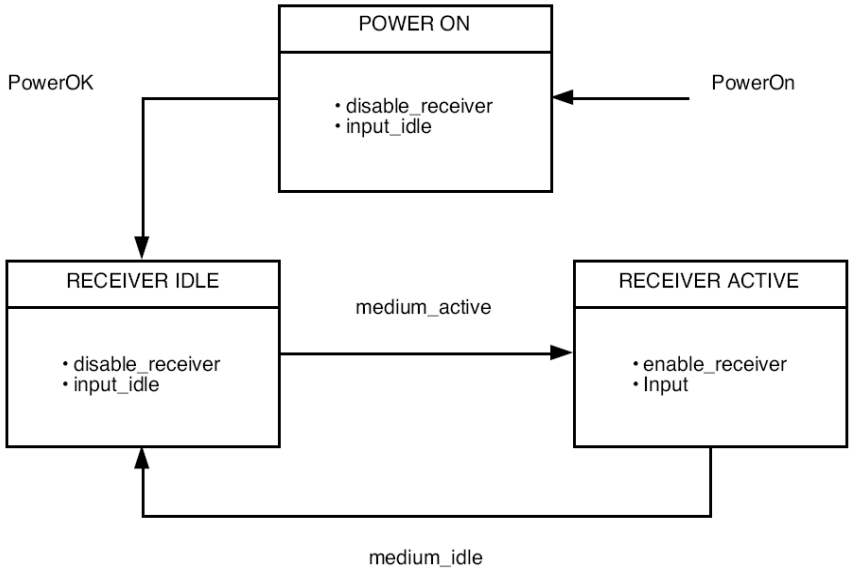


a) Receive function state diagram



b) Collision Presence function state diagram

Figure 8–2—Interface function: Simple MAU without isolate capability

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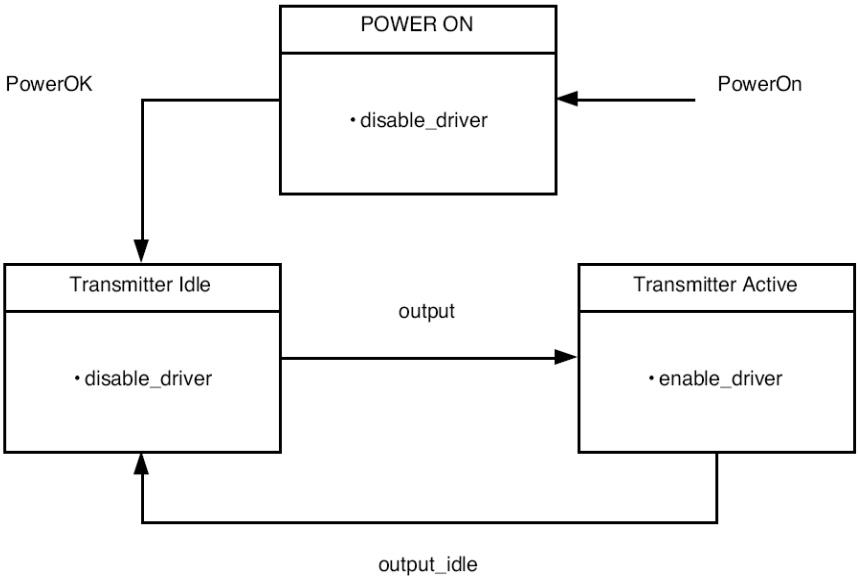
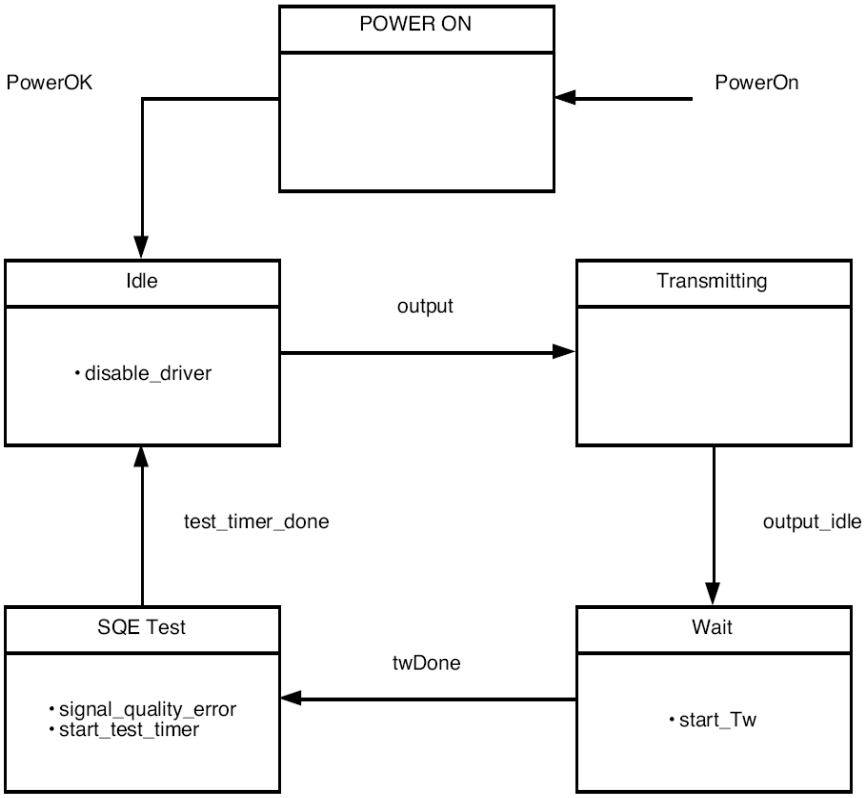


c) Transmit function state diagram



d) SQE test state diagram

Figure 8–2—*(Continued)*
Interface function: Simple MAU without isolate capability

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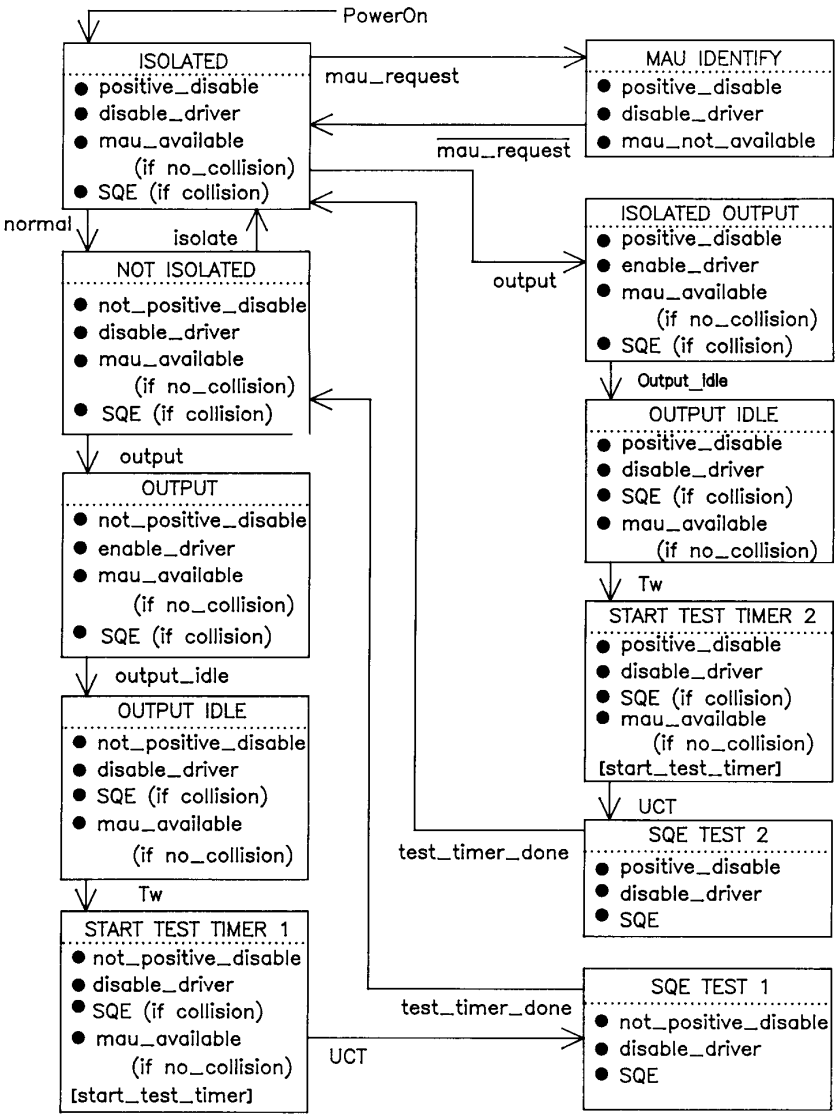

NOTE: UCT = unconditional transition
Tw = wait time, see 8.2.1.1

Figure 8–3—Interface function: Simple MAU with isolate capability

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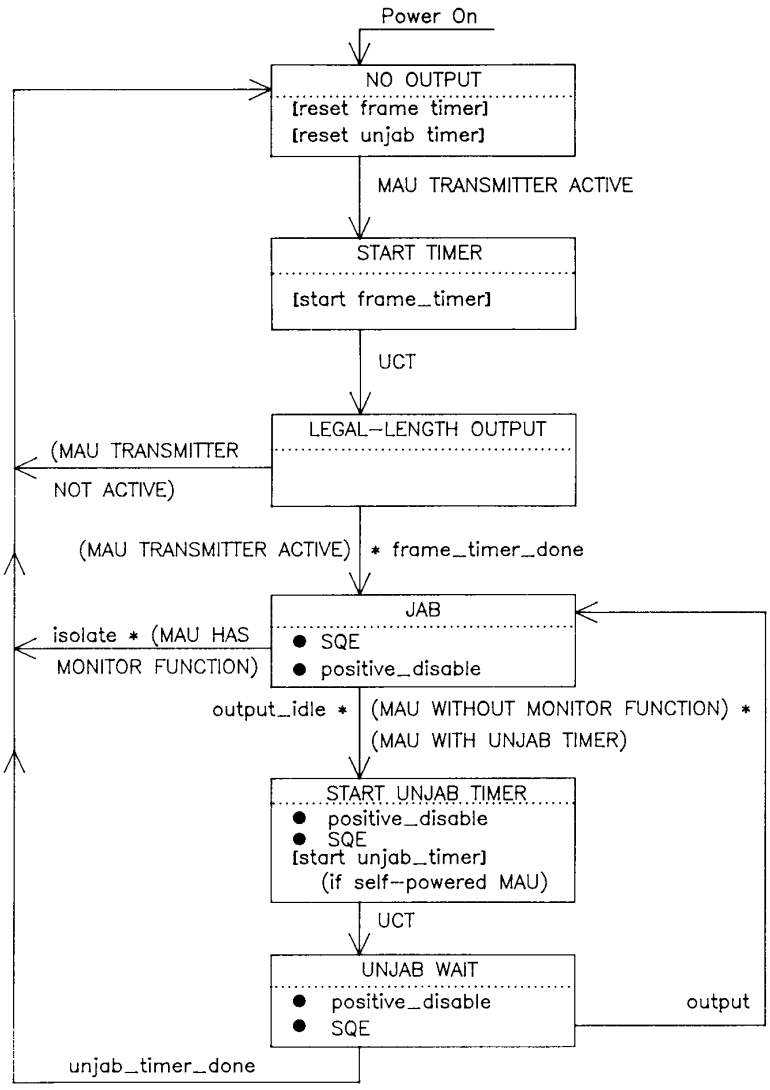

Figure 8–4—Jabber function

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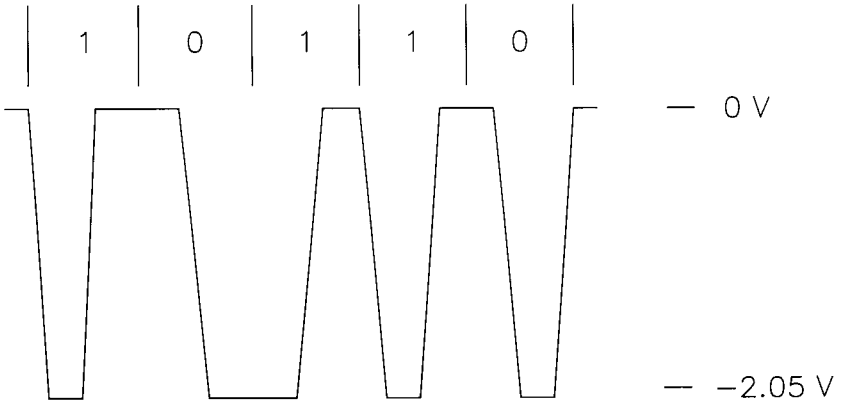
The actual current measured at a given point on the cable is a function of the transmitted current and the cable loss to the point of measurement. Negative current is defined as current out of the center conductor of the cable (into the MAU). The 10–90% rise/fall times shall be 25 ns ± 5 ns at 10 Mb/s. The rise and fall times shall match within 2 ns. Figure 8–5 and Figure 8–6 shows typical waveforms present on the cable. Harmonic content generated from the BR fundamental periodic input shall meet the following requirements:

2nd and 3rd Harmonics:at least 20 dB below fundamental
4th and 5th Harmonics:at least 30 dB below fundamental
6th and 7th Harmonics:at least 40 dB below fundamental
All higher Harmonics:at least 50 dB below fundamental

NOTE—Even harmonics are typically much lower.

The above specifications concerning harmonics cannot be satisfied by a square-wave with a single-pole filter, nor can they be satisfied by an output waveform generator employing linear ramps without additional waveshaping. The signals as generated from the encoder within PLS shall appear on the coaxial cable without any inversions (see Figure 8–6).



NOTES: (1) Voltages given are nominal, for a single transmitter
(2) Rise and fall time is 25 ns nominal at 10 Mb/s rate
(3) Voltages are measured on terminated coaxial cable adjacent to transmitting MAU
(4) Manchester coding

Figure 8–5—Typical coaxial trunk cable signal waveform

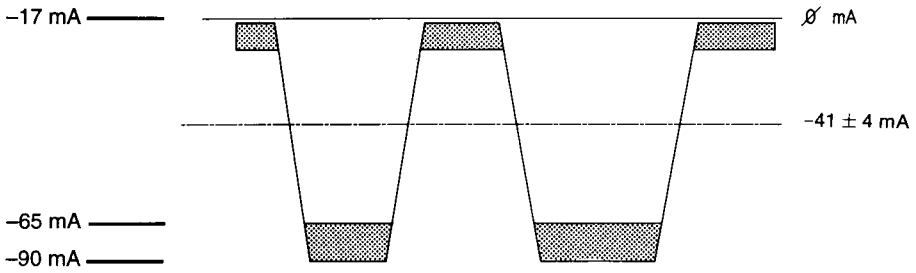


Figure 8–6—Recommended driver current signal levels

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8.3.1.4 Transmit output levels symmetry

Signals received from the AUI DO circuit shall be transmitted onto the coaxial cable with the characteristics specified in 8.3.1.3. Since the coaxial cable proceeds in two directions from the MAU, the current into the MAU is nominally twice the current measured on the coaxial cable.

The output signal of a MAU meeting this specification shall exhibit edge jitter of no more than 2.5 ns into a 25 Ω ± 1% resistor substituted for the connection to the coaxial cable when the DO circuit into the MAU is driven through a zero length AUI cable with pseudorandom Manchester encoded binary data from a data generator that exhibits no more than 0.5 ns of edge jitter on half bit cells of exactly 1/2 BT whose output meets the specifications of 7.4.1.1 through 7.4.1.5. The above specified component is not to introduce more than 2 ns of edge jitter into the system.

The MAU shall not transmit a negative going edge after cessation of the CD output data stream on DO or before the first edge of the next frame on the DO circuit.

8.3.1.5 Collision detect thresholds

Receive mode collision detection indicates that a nontransmitting MAU has the capability to detect collisions when two or more MAUs are transmitting simultaneously. For receive mode collision detection, the MAU's collision detection threshold shall be within the range –1448 mV to –1590 mV. The actual dc voltage on the cable during a noncollision transmission has a maximum value of –1293 mV. The lower threshold limit of –1448 mV allows 55 mV for sending end overshoot during preamble and filter impulse response during the remainder of the packet. These limits take account of up to 12% collision detect filter impulse response. If a specific filter implementation has a higher value of impulse response, the lower threshold limit of 1448 mV shall be replaced by 1293 mV × [1 + impulse response].

All MAUs are required to implement receive mode collision detection.

NOTE—The above threshold limits are measured at the coaxial cable center conductor with respect to the shield at the MAU connector. The MAU designer has to take into account circuit offsets, low-frequency noise (for example, 50 Hz, 60 Hz), and 5 MHz ripple at the filter output in determining the actual internal threshold value and its tolerance.

8.3.2 MAU electrical characteristics

8.3.2.1 Electrical isolation

The MAU provides isolation between the AUI cable and the coaxial trunk cable. This isolation shall meet the isolation requirements as specified in J.1.

CAUTION

The current electrical isolation requirement is a change that was incorporated into IEEE Std 802.3-1996. Older editions of IEEE Std 802.3 had a significantly lower isolation requirement.

8.3.2.2 Power consumption

The current drawn by the MAU shall not exceed 0.5 A as powered by the AUI source. The MAU shall be capable of operating from all possible voltage sources as supplied by the DTE through the resistance of all permissible AUI cables. The MAU shall not disrupt the trunk coaxial medium should the DTE power source fall below the minimum operational level under abnormal MAU load conditions.

The MAU shall be labeled externally to identify the maximum value of current required by the device at any specified input voltage.

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8.3.2.3 Reliability

The MAU shall be designed to provide an MTBF of at least 1 million hours of continuous operation without causing communication failure among other stations attached to the local network medium. Component failures within the MAU electronics should not prevent communication among other MAUs on the coaxial cable. Connectors and other passive components comprising the means of connecting the MAU to the coaxial cable shall be designed to minimize the probability of total network failure.

It should be noted that a fault condition that causes a MAU to draw in excess of 2 mA may cause communication failure among other stations.

8.3.3 MAU–DTE electrical characteristics

The electrical characteristics for the driver and receiver components connected to the branch cable within the MAU shall be identical to those as specified in Clause 7 of this standard.

8.3.4 MAU–DTE mechanical connection

The MAU shall be provided with a 15-pin male connector as specified in detail in the AUI specification, Clause 7.

8.4 Characteristics of the coaxial cable

The trunk cable is of constant impedance, coaxial construction. It is terminated at each end by a terminator (see 8.5.2), and provides the transmission path for MAU device connection. Coaxial cable connectors are used to make the connection from the cable to the terminators, and between cable sections (if needed). The cable has various electrical and mechanical requirements that shall be met to ensure proper operation.

8.4.1 Coaxial cable electrical parameters

8.4.1.1 Characteristic impedance

The average characteristic cable impedance shall be 50 ± 2 Ω, measured at 10 MHz according to IEC 60096-1: 1986 and Amd. 2: 1993. Periodic variations in impedance along a single piece of cable may be up to ±3 Ω sinusoidal centered around the average value, with a period of less than 2 m.

NOTE—If the requirements of 8.4.2.1.1 item b), 8.4.2.1.2, 8.4.2.1.3, and 8.4.2.1.4 item b) are met, then it is expected that the characteristic impedance periodicity requirement is met.

8.4.1.2 Attenuation

The attenuation of a 500 m cable segment shall not exceed 8.5 dB (17 dB/km) measured with a 10 MHz sine wave, nor 6.0 dB (12 dB/km) measured with a 5 MHz sine wave.

8.4.1.3 Velocity of propagation

The minimum required velocity of propagation is 0.77 c.

8.4.1.4 Edge jitter, untapped cable

Untapped coaxial cable meeting this specification shall exhibit edge jitter of no more the 8.0 ns in either direction at the receiving end when 500 m of the cable is terminated at both ends with terminators meeting the impedance requirements of 8.5.2.1 and is driven at one end with pseudorandom Manchester-encoded

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binary data from a data generator that exhibits no more than 1.0 ns of edge jitter in either direction on half bit cells of exactly 1/2 BT and whose output meets the specifications of 8.3.1.3 except that the rise time of the signal has to be 30 ns + 0, – 2 ns, and no offset component in the output current is required. This test shall be conducted in a noise-free environment. The above specified component is not to introduce more than 7 ns of edge jitter into the system.

8.4.1.5 Transfer impedance

The coaxial cable medium shall provide sufficient shielding capability to minimize its susceptibility to external noise and also to minimize the generation of interference by the medium and related signals. While the cable construction is not mandated, it is necessary to indicate a measure of performance expected from the cable component. A cable's EMC performance is determined, to a large extent, by the transfer impedance value of the cable. See reference [B53].

The transfer impedance of the cable shall not exceed the values shown in Figure 8–7 as a function of frequency.

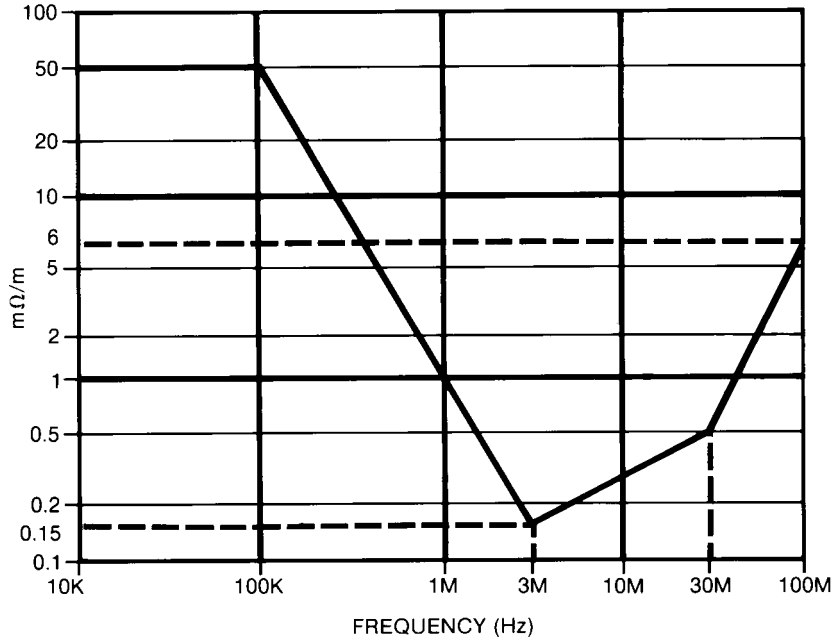

Figure 8–7—Maximum coaxial cable transfer impedance

8.4.1.6 Cable dc loop resistance

The sum of the center conductor resistance plus the shield resistance, measured at 20 °C, shall not exceed 10 mΩ/m.

8.4.2 Coaxial cable properties

8.4.2.1 Mechanical requirements

The cable used should be suitable for routing in various environments, including but not limited to, dropped ceilings, raised floors, cable troughs, and throughout open floor space. The jacket shall provide insulation between the cable sheath and any building structural metal. Also, the cable shall be capable of accepting coaxial cable connectors, described in 8.5. The cable shall conform to the following requirements.

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8.4.2.1.1 General construction

a) The coaxial cable shall consist of a center conductor, dielectric, shield system, and overall insulating jacket.
b) The concentricity (for example, positional relationship between center conductor to shield system and outer jacket) of the coaxial cable elements shall be greater than 92% as measured in accordance with the following general configuration:

$$\frac{(\text{jacket radius}) - (\text{center offset})}{\text{jacket radius}} \times 100 \geq 92\%$$

It is assumed that the offset and radius values are worst case at any point within the measured system.
c) The coaxial cable jacket, shield system, and dielectric material shall be pierceable either by means of the connector type specified in 8.5.3.2 or by an external core tool. Overall cable system pierceability (the ability of a tap probe to pierce the jacket, shields, and dielectric cable system without substantial dielectric deformation and without causing a short circuit between center conductor and shield system) is a vital parameter affecting tap connection reliability.

Pierceability of the cable system can be measured in terms of the probe's load versus displacement signature. A pierceable cable exists where the displacement is ≥ 1.52 mm (0.06 in) between rupture (piercing) of the shield system and contact with the center conductor.
d) The coaxial cable shall be sufficiently flexible to support a bend radius of 254 mm (10 in).

8.4.2.1.2 Center conductor

The center conductor shall be 2.17 mm ± 0.013 mm (0.0855 in ± 0.0005 in) diameter tinned or plain solid copper.

8.4.2.1.3 Dielectric material

The dielectric may be of any type provided the conditions of 8.4.1.2, 8.4.1.3, and 8.4.2.1.1item d) are met.

8.4.2.1.4 Shielding system

a) The shielding system may contain both braid and foil elements sufficient to meet the transfer impedance of 8.4.1.5 and the EMC specifications of 8.7.2.
b) The inside diameter of the innermost shield shall be 6.00 mm (0.236 in) minimum.
c) The outside diameter of the outermost shield shall be 8.00 mm ± 0.40 mm (0.315 in ± 0.016 in).
d) The outermost shield shall be a tinned copper braid. The percent coverage shall be sufficient to meet 8.4.1.5, 8.4.1.6, 8.5.3.2.3, and 8.7.2.

8.4.2.1.5 Overall jacket

a) Any one of several jacket materials shall be used provided the specifications of 8.4.1 and 8.4.2 are met.
b) Either of two jacket dimensions may be used for the two broad classes of materials, provided the specification of 8.4.2.1.1 are met:
    1) Polyvinyl Chloride (for example, PVC) or equivalent having an OD of 10.3 mm ± 0.25 mm (0.406 nominal ± 0.010 in).
    2) Fluoropolymer (for example, FEP, E-CTFE) or equivalent having an OD of 9.525 mm ± 0.254 mm (0.375 nominal ± 0.010 in).

The cable shall meet applicable flammability and smoke criteria and local and national codes for the installed environment. See 8.7.4. Different types of cable sections (for example, polyvinyl chloride and

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fluoropolymer dielectric) may be interconnected, while meeting the sectioning requirements of 8.6. See references [B14] and [B67].

8.4.2.2 Jacket marking

The cable jacket shall be marked in a color contrasting with the background color of the jacket. The markings shall be spaced at 2.5 m ± 5 cm regularly along the entire length of the cable. It is permissible for the 2.5 m spacing to be interrupted at discontinuities between cable sections joined by connectors. (See 8.6.2.2 for MAU placement rules that mandate cable markings.) It is recommended that the base color of the jacket itself be a bright color (for example, yellow) other than that normally used for power mains.

8.4.3 Total segment dc loop resistance

The sum of the center conductor, connectors, and shield resistance shall not exceed 5 Ω total per segment.

Each in-line connector pair or MAU shall be no more than 10 mΩ. Use of these components reduces the overall allowable segment length accordingly. Values given above are at 20 °C. For temperature variations, cable length shall be adjusted accordingly such that the 5 Ω total is not exceeded.

If a trunk coaxial cable segment consists of several cable sections, then all connectors and internal resistance of the shield and center conductor shall be included in the loop resistance measurement.

8.5 Coaxial trunk cable connectors

The trunk coaxial medium requires termination and may be extended or partitioned into sections. Devices to be attached to the medium as MAUs require a means of connection to the medium. Two basic connector types provide the necessary connection means:

a) Standard Type N connectors (IEC 60169-16)
b) A coaxial “tap” connector

All Type N connectors shall be of the 50 Ω constant impedance type. Since the frequencies present in the transmitted data are well below UHF range (being band-limited to approximately 20 MHz), high-quality versions of the connectors are not required (but are recommended).

All of the coaxial tap connectors shall follow the requirements as defined in 8.5.3.

8.5.1 Inline coaxial extension connector

All coaxial cables shall be terminated with the Type N plug connectors. A means shall be provided to ensure that the connector shell (which connects to the cable sheath) does not make contact with any building metal or other unintended conductor. An insulating sleeve or boot slipped over the connector at installation time is suitable.

Inline coaxial extensions between two sections of coaxial cable shall be made with a pair of Type N receptacle connectors joined together to form one “barrel.” An insulating sleeve or boot shall also be provided with each barrel assembly.

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8.5.2 Coaxial cable terminator

8.5.2.1 Termination

Coaxial cable terminators are used to provide a termination impedance for the cable equal in value to its characteristic impedance, thereby minimizing reflection from the ends of the cables. Terminators shall be packaged within an inline female receptacle connector. The termination impedance shall be 50 Ω ± 1% measured from 0 MHz to 20 MHz, with the magnitude of the phase angle of the impedance not to exceed 5°. The terminator power rating shall be 1 W or greater.

8.5.2.2 Earthing

Either the coaxial cable terminator or inline extension connector provides a convenient location for meeting the earth grounding requirement of 8.6.2.3. It is recommended that a ground lug with current rating of at least 1500 ampacity be provided on one of the two terminators or on one extension connector used within a cable segment.

NOTE 1—A single ground return lug on an inline connector located in the center of the cable transmission system may be used to satisfy this requirement.

NOTE 2—Alternatively, terminators might be supplied in pairs, one with and one without the ground lug connection point.

8.5.3 MAU-to-coaxial cable connection

A means shall be provided to allow for attaching a MAU to the coaxial cable. The connection shall not disturb the transmission line characteristics of the cable significantly; it shall present a predictably low shunt capacitance, and therefore a negligibly short stub length. This is facilitated by the MAU being located as close to its cable connection as possible; the MAU and connector are normally considered to be one assembly. Long (greater than 30 mm) connections between the coaxial cable and the input of the MAU jeopardize this objective.

Overall system performance is dependent largely on the MAU-to-coaxial cable connection being of low shunt capacitance.

If the design of the connection is such that the coaxial cable is to be severed to install the MAU, the coaxial cable segment shall still meet the sectioning requirements of 8.6.2.1. Coaxial connectors used on a severed cable shall be Type N, as specified in 8.5.1.

The Type N connectors selected should be of high quality (that is, low contact resistance) to minimize the impact on system performance.

If the design of the connection is such that the piercing tap connector is to be used without severing the cable, then the tap connector and cable assembly shall conform to the mechanical and electrical requirements as defined throughout 8.5.3.1 and 8.5.3.2.

8.5.3.1 Electrical requirements

Requirements for the coaxial tap connector are as follows:

a) *Capacitance:* 2 pF nominal connector loading measured at 10 MHz.

NOTE—**Total** capacitance of tap and active circuitry connected directly is required to be no greater than 4 pF. Specific implementations may allocate capacitance between tap and circuitry as deemed appropriate.

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b) *Contact resistance (*applies to center conductor and shield contacts): 50 mΩ maximum for both shield and center conductor over useful connector lifetime.
c) *Contact material:* surface material on signal probe or shield sufficient to meet contact resistance requirements in environment and over time.
d) *Voltage rating:* 600 V dc or ac rms maximum.
e) *Insulation:* dc leakage resistance of tap housing shall be higher than 1 GΩ between braid and external conductors in the normal operating environment.
f) *Probe current rating:* 0.1 A per contact (probe and shield).
g) *Shield current rating:* 1 A surge for 1 s.

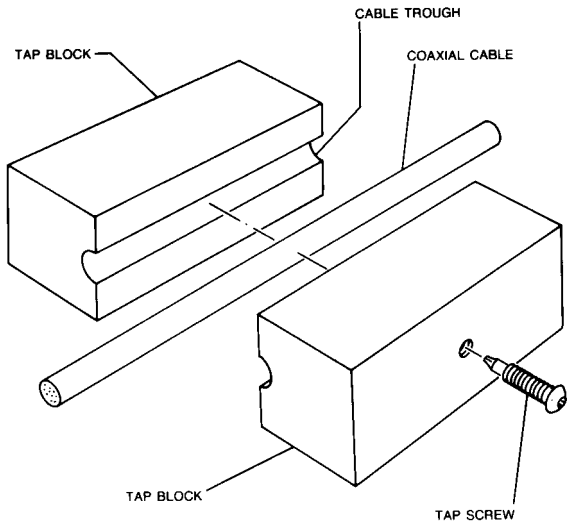
8.5.3.2 Mechanical requirements

8.5.3.2.1 Connector housing

Shielding characteristics: > 40 dB at 50 MHz.

8.5.3.2.2 Contact reliability

Overall performance of the LAN system depends to a large extent on the reliability of the coaxial cable medium and the connection to that medium. Tap connection systems should consider the relevant electrical and mechanical parameters at the point of electrical connection between tap probe and cable center conductor to ensure that a reliable electrical contact is made and retained throughout the useful life of these components. It is recommended that some means be provided to ensure relatively constant contact loading over time, with creep, in temperature, and typical environment. Typical coaxial tap connector configurations are shown in Figure 8–8 and Figure 8–9. See references [B3], [B1], and [B2].



NOTE: **Tutorial only** and **not** part of specification

Figure 8–8—Coaxial tap connector configuration concepts

8.5.3.2.3 Shield probe characteristics

The shield probe shall penetrate the cable jacket and outer layer(s) of the shield system to make effective capture of the outer braid (pick 2 or more typical strands).

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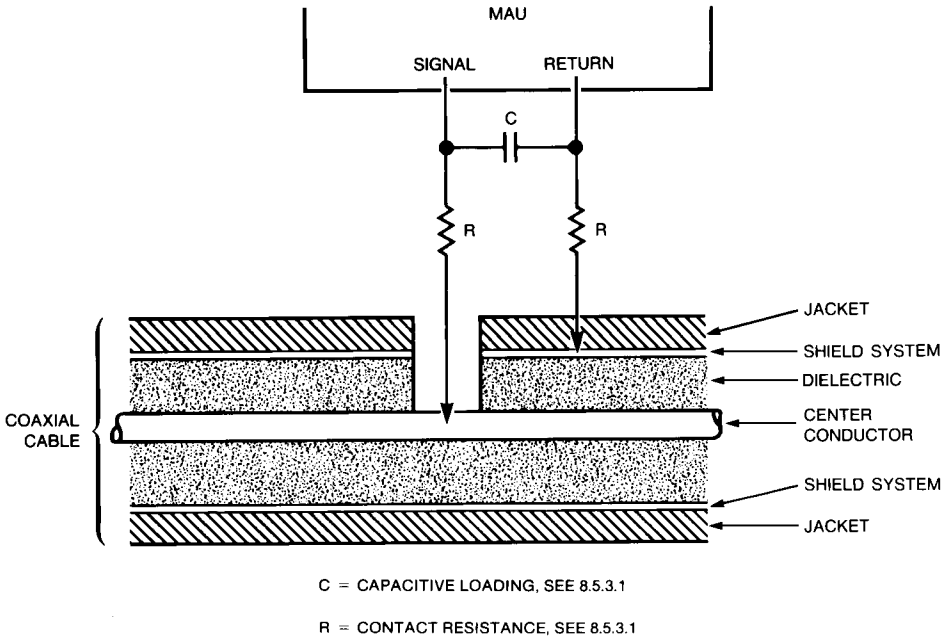

Figure 8–9—Typical coaxial tap connection circuit

8.6 System considerations

8.6.1 Transmission system model

The maximum configuration for the physical transmission system is as follows:

a) A trunk coaxial cable, terminated in its characteristic impedance at each end, constitutes a coaxial cable segment. A coaxial cable segment may contain a maximum of 500 m of coaxial cable and a maximum of 100 MAUs. The propagation velocity of the coaxial cable is assumed to be 0.77 c minimum (c = 300 000 km/s). The maximum end-to-end propagation delay for a coaxial cable segment is 2165 ns.

b) Repeater sets are required for segment interconnection. Repeater sets occupy MAU positions on coaxial cable segments and count toward the maximum number of MAUs on a coaxial cable segment. Repeater sets may be located in any MAU position on a coaxial cable segment.

c) The repeater unit specified in Clause 9 provides the means for connecting 10 Mb/s baseband segments into a CSMA/CD network. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of interpacket gap as it travels through the network. Configuration rules, which ensure that these limits are not exceeded, are given in Clause 13.

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8.6.2 Transmission system requirements

8.6.2.1 Cable sectioning

The 500 m maximum length coaxial cable segment need not be made from a single, homogeneous length of cable. The boundary between two cable sections (joined by coaxial connectors: two male plugs and a barrel) represents a signal reflection point due to the impedance discontinuity caused by the batch-to-batch impedance tolerance of the cable. Since the worst-case variation from 50 Ω is 2 Ω, a possible worst-case reflection of 4% may result from the joining of two cable sections. The configuration of long cable segments (up to 500 m) from smaller sections has to be made with care. The following *recommendations* apply, and are *given in order of preference*:

a) If possible, the total segment should be made from one homogeneous (no breaks) cable. This is feasible for short segments, and results in minimal reflections from cable impedance discontinuities.
b) If cable segments are built up from smaller sections, it is recommended that all sections come from the same manufacturer and lot. This is equivalent to using a single cable, since the cable discontinuities are due to extruder limitations, and not extruder-to-extruder tolerances. There are no restrictions in cable sectioning if this method is used. However, if a cable section in such a system is later replaced, it shall be replaced either with another cable from the same manufacturer and lot, or with one of the standard lengths described below.
c) If uncontrolled cable sections have to be used in building up a longer segment, the lengths should be chosen so that reflections, when they occur, do not have a high probability of adding in phase. This can be accomplished by using lengths that are odd integral multiples of a half wavelength in the cable at 5 MHz; this corresponds to using lengths of 23.4 m, 70.2 m, and 117 m (± 0.5 m) for all sections. These are considered to be the standard lengths for all cable sections. Using these lengths exclusively, any mix or match of cable sections may be used to build up a 500 m segment without incurring excessive reflections.

NOTE—If cable segments are to be added to existing installations, then care should be taken (explicit physical or TDR measurements) to ensure that no more than a 500 m cable segment results.

d) As a last resort, an arbitrary configuration of cable sections may be employed, if it has been confirmed by analysis or measurement that the worst-case signal reflection due to the impedance discontinuities at any point on the cable does not exceed 7% of the incident wave when driven by a MAU meeting these specifications.

8.6.2.2 MAU placement

MAU components and their associated connections to the cable cause signal reflections due to their noninfinite bridging impedance. While this impedance shall be implemented as specified in Clause 7, placement of MAUs along the coaxial cable also has to be controlled to ensure that reflections from the MAU do not add in phase to a significant degree.

Coaxial cables marked as specified in 8.4.2.2 have marks at regular 2.5 m spacing; a MAU shall only be placed at a mark on the cable. This guarantees both a minimum spacing between MAUs of 2.5 m, and controlling the relative spacing of MAUs to ensure nonalignment on fractional wavelength boundaries.

The total number of MAUs on a cable segment shall not exceed 100.

8.6.2.3 Trunk cable system grounding

The *shield conductor* of each coaxial cable segment *shall make electrical contact with an effective earth reference* (see [B10], Articles 250 and 800) *at one point and shall not make electrical contact with earth elsewhere* on such objects as building structural metal, ducting, plumbing fixture, or other unintended

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conductor. Insulators may be used to cover any coaxial connectors used to join cable sections and terminators, to ensure that this requirement is met. A sleeve or boot attached at installation time is acceptable.

This specification is intended for use within (intraplant) buildings. Applications requiring interplant connections by way of external (outdoors) means may require special consideration beyond the scope of the standard.

The sheath conductor of the AUI cable shall be connected to the earth reference or chassis of the DTE.

8.6.3 Labeling

It is recommended that each MAU (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in megabits per second
b) Power level in terms of maximum current drain
c) Safety warning (for example, shock hazard)

8.7 Environmental specifications

8.7.1 General safety requirements

All Physical Layer MDIs meeting this standard shall conform to the general safety requirements in J.2.

8.7.2 Network safety requirements

This subclause sets forth a number of recommendations and guidelines related to safety concerns, the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate standards. References [B10] and [B19] provide additional guidance.

LAN trunk cable systems as described in this standard are subject to at least four direct electrical safety hazards during their use. These hazards are

a) Direct contact between local network components and power or lighting circuits.
b) Static charge buildup on local network cables and components.
c) High-energy transients coupled onto the local network cabling system.
d) Potential differences between safety grounds to which various network components are connected.

These electrical safety hazards, to which all similar cabling systems are subject, should be alleviated properly for a local network to perform properly. In addition to provisions for properly handling these faults in an operational system, special measures have to be taken to ensure that the intended safety features are not negated during installation of a new network or during modification of an existing network.

Proper implementation of the following provisions will greatly decrease the likelihood of shock hazards to persons installing and operating the LAN.

8.7.2.1 Installations

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

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8.7.2.2 Grounding

The shield of the trunk coaxial cable shall be effectively grounded at only one point along the length of the cable. Effectively grounded means permanently connected to earth through a ground connection of sufficiently low impedance and having sufficient ampacity to prevent the building up of voltages that may result in undue hazard to connected equipment or to persons.

8.7.2.3 Safety

All portions of the trunk cabling system that are at the same potential as the trunk cable shall be insulated by adequate means to prevent their contact by either persons or by unintended conductors or grounds. The insulation employed shall provide the same or greater dielectric resistance to current flow as the insulation required between the outermost shield of the trunk cable and the above-mentioned unintended conductors. The use of insulating boots is permitted, provided that such boots (or sleeves) are mechanically and electrically equivalent to the trunk cable outer insulation characteristics and are not removed easily (that is, they shall prevent inadvertent removal by a system operator).

The MAU shall be so designed that the provisions of 8.7.2.3 and 8.7.2.4 are not defeated if the connector affixing the AUI cable to the MAU is removed.

Portions of the trunk cabling system that may become live during the dissipation of a high-energy transient by the cabling system shall also be insulated as described in 8.7.2.3.

8.7.2.4 Breakdown path

MAUs meeting this standard should provide a controlled breakdown path that will shunt high-energy transients to an effective ground either through a separate safety ground connection or through the overall shield of the branch cable. The breakdown voltage of this controlled breakdown path has to meet the isolation requirements for the MAU specified in 8.3.2.1.

8.7.2.5 Isolation boundary

The isolation boundary between the branch cable and trunk cable specified in 8.3.2.1 shall be maintained to properly meet the safety requirements of this standard.

WARNING

It is assumed that the DTE equipment is properly earthed and not left floating or serviced by “doubly insulated ac power distribution system.” The use of floating or insulated DTEs is beyond the scope of this standard.

8.7.2.6 Installation and maintenance guidelines

a) When exposing the shield of the trunk coaxial cable for any reason, care shall be exercised to ensure that the shield does not make electrical contact with any unintended conductors or grounds. Personnel performing the operation should not do so if dissipation of a high energy transient by the cabling system is likely during the time the shield is to be exposed. Personnel should not contact both the shield and any grounded conductor at any time.
b) Before breaking the trunk coaxial cable for any reason, a strap with ampacity equal to that of the shield of the coaxial cable shall be affixed to the cable shield in such a manner as to join the two pieces and to maintain continuity when the shield of the trunk cable is severed. This strap shall not be removed until after normal shield continuity has been restored.
c) At no time should the shield of any portion of the coaxial trunk cable to which an MAU or MAUs are attached be permitted to float without an effective ground connection. If a section of floating

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cable is to be added to an existing cable system, the installer shall take care not to complete the circuit between the shield of the floating cable section and the grounded cable section through body contact.

d) The installation instructions for network components shall contain language which familiarizes the installer with the cautions mentioned in the above paragraphs.
e) Network components shall contain prominent warning labels that refer installers and service personnel to the safety notes in the installation instructions.

8.7.3 Electromagnetic environment

8.7.3.1 Susceptibility levels

Sources of interference from the environment include electromagnetic fields, electrostatic discharge, transient voltages between earth connections, and similar interference. Multiple sources of interference may contribute to voltage buildup between the coaxial cable and the earth connection of a DTE.

The physical channel hardware shall meet its specifications when operating in either of the following conditions:

a) Ambient plane wave field of 2 V/m from 10 kHz through 30 MHz, 5 V/m from 30 MHz through 1 GHz.

NOTE—Levels typically l km from broadcast stations.

b) Interference voltage of 1 V/ns peak slope, between coaxial cable shield and DTE earth connection; for example, 15.8 V peak for a 10 MHz sine wave with a 50 Ω source resistance.

MAUs meeting this standard should provide adequate rf ground return to satisfy the referenced EMC specifications.

8.7.3.2 Emission levels

The physical MAU and trunk cable system shall comply with applicable local and national codes such as FCC Docket 20780-1980 [B23] in the USA. Equipment shall comply with local and national requirements for limitation of electromagnetic interference. Where no local or national requirements exist, equipment shall comply with CISPR 22: 1993.

8.7.4 Temperature and humidity

The MAU and associated connector/cable systems are expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling such as shock and vibration. Specific requirements and values for these parameters are considered to be beyond the scope of this standard. Manufacturers are requested to indicate in the literature associated with the MAU (and on the MAU if possible) the operating environment specifications to facilitate selection, installation, and maintenance of these components. See reference [B20] for specification terminology.

8.7.5 Regulatory requirements

The design of MAU and medium components should take into consideration applicable local or national requirements. See references [B10], [B14], [B15], [B19], [B23], and Annex B for helpful resource material.

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8.8 Protocol implementation conformance statement (PICS) proforma for Clause 8, Medium Attachment Unit and baseband medium specifications, type 10BASE5[41]

8.8.1 Overview

The supplier of a protocol implementation that is claimed to conform to Clause 8, Medium Attachment Unit and baseband medium specifications, type 10BASE5, shall complete the following PICS proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. The PICS can be used for a variety of purposes by various parties, including the following:

— As a checklist by the protocol implementer, to reduce the risk of failure to conform to the standard through oversight;
— As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
— As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICs);
— As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

8.8.2 Abbreviations and special symbols

8.8.2.1 Status symbols

The following abbreviations are used in the PICS proforma tables:

M mandatory

O optional

O. <n> optional, but support of at least one of the group of options labeled by the same numeral <n> is required

X prohibited

<item>: conditional-item symbol, dependent upon the support for <item>

! logical negation, applied to a conditional item symbol

8.8.2.2 Abbreviations

Ref reference section

8.8.3 Instructions for completing the PICS proforma

8.8.3.1 General structure of the PICS proforma

The structure of this PICS proforma is based on the guidelines given in ISO/IEC 9646-1: 1994 and ISO/IEC 9646-2: 1994. The first part of the PICS proforma, Implementation Identification and Protocol Summary, is

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to be completed as indicated with the information necessary to identify fully both the supplier and the particular MAU.

The main part of the PICS proforma is a fixed-format questionnaire. Each item is identified by an item reference in the first column; the second column contains the question to be asked or the parameter to be measured; the third column contains the reference(s) to the material that specifies the item in the main body of this standard; the fourth column records the status of the item—whether support is mandatory, optional, prohibited, or conditional—and provides space for the answers; the fifth column provides additional comments and/or value(s) for measurable parameters. The tables below group related items into separate subclauses. This satisfies the requirement of ISO/IEC 9646-2 that all PICS proforma clauses be individually identified.

A supplier wishing to submit a 10BASE5 MAU for conformance testing against this standard has to fill in the column headed Support in the PICS proforma tables and submit the resulting PICS with the equipment for test. One of the boxes in this column has to be checked, with Yes indicating that the implementation is intended to meet the particular mandatory or optional requirement, No indicating that the option has not been implemented (or enabled where switchable) or that the requirement is not met, or N/A indicating the item is not applicable (for example, an item that is conditional). It should be noted that any instances of No checked against a mandatory requirement will result in the implementation failing the static conformance test.

8.8.3.2 Additional information

Any additional information that is needed to ensure that the MAU or the coaxial cable submitted for test is configured as a 10BASE5 MAU or coaxial cable should be entered into the PIXIT (Protocol Implementation eXtra Information for Testing) document supplied by the conformance testing organization. Relevant information on 10BASE5 MAUs includes the following:

a) Enable/disable mechanisms for SQE Test
b) Enable/disable mechanisms for features that allow compatibility with nonstandard implementations
c) Operational instructions for DTEs or repeaters in cases where the MAU is embedded
d) Environmental conditions
e) Power supply voltage range

The above list is illustrative and is neither mandatory nor exhaustive.

8.8.3.3 Exception information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this. Instead, the supplier shall write the missing answer into the Support column, together with an X<i> reference to an item of Exception Information, and shall provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this standard.

8.8.3.4 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it applies—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form “<item>:<s>” in the Status column, where “<item>” is the section number and item reference that appears in the first column of the

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table for some other item, and "<s>" is a status symbol, M, O, O.<n>, or X. The "!" symbol, prefixed to an item reference, means logical negation.

If the item referred to by the conditional symbol is marked as supported, the conditional item is applicable, and its status is given by "<s>"; the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

8.8.4 Identification

8.8.4.1 Implementation identification

The MAU supplier shall complete the relevant fields in this section to identify the supplier and the particular MAU.

Supplier	
Contact point for inquiries about the PICS	
Implementation name(s) and version(s)	

8.8.4.2 Protocol summary

The supplier will complete this section to identify the precise protocol implemented.

Identification of protocol standard	IEEE Std 802.3-2018, Clause 8, Medium Attachment Unit and baseband medium specifications, type 10BASE5
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exception items been required? (The answer Yes means that the implementation does not conform to this standard.)	Yes [ ] No [ ]

Date of Statement	

8.8.5 Global statement of conformance

The supplier should indicate below whether or not the implementation implements all the mandatory requirements. Answering No to this question indicates nonconformance to the protocol specification. Nonsupported mandatory capabilities are to be identified in the PICS, with an explanation of why the implementation is non-conforming.

This implementation meets all mandatory requirements	Yes [ ] No [ ]

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8.8.6 PICS proforma tables for MAU

8.8.6.1 MAU compatibility

Item	Parameter	Reference	Status	Support	Value/Comment
*1	MAU intended for attachment to repeater		O	Yes [ ]No [ ]	
*2	Monitor Function supported		O	Yes [ ]No [ ]	
*3	AUI Circuit CO supported		8.8.6.1/2 :M !8.8.6.1/2 :O	N/A [ ] Yes [ ]No [ ] N/A [ ] Yes [ ]No [ ]	Required for Monitor function
4	SQE Test supported	9.4.1	8.8.6.1/1 :X !8.8.6.1/1 :M	N/A [ ] Yes [ ]No [ ] N/A [ ] Yes [ ]No [ ]	Function not performed for MAUs attached to repeaters

8.8.6.2 Transmit function

Item	Parameter	Reference	Status	Support	Value/Comment
1	Transmit path	8.2.1.1	M	Yes [ ]No [ ]	DO circuit to coaxial cable
2	Transmit signal polarity	8.2.1.1	M	Yes [ ] No [ ]	DO A positive relative to DO B causes more positive voltage on the coaxial medium
3	Start-up bit loss (DO to coaxial cable)	8.2.1.1	M	Yes [ ]No [ ]	2 bits max
4	Transmit settling time	8.2.1.1	M	Yes [ ]No [ ]	Second and following bits meet amplitude and jitter specifications
5	Transmit steady-state delay	8.2.1.1	M	Yes [ ]No [ ]	1/2 bit times max
6	Start-up bit loss (DO to coaxial cable) variability	8.2.1.1	M	Yes [ ]No [ ]	2 bits max between packets separated by ≤ 96 BT
7	No extraneous signal on the coaxial media after DO idle	8.2.1.1	M	Yes [ ]No [ ]	
8	Start collision presence state	8.2.1.1	M	Yes [ ]No [ ]	Within 0.6 µs to 1.6 µs after idle
9	Collision presence state duration	8.2.1.1	M	Yes [ ]No [ ]	5–15 bit times

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8.8.6.3 Receive function

Item	Parameter	Reference	Status	Support	Value/Comment
1	Direct coupling of signal from medium to the receiver	8.2.1.2	M	Yes [ ] No [ ]	
2	AC-coupling from the receiver to AUI interface	8.2.1.2	M	Yes [ ] No [ ]	
3	Start-up bit loss (coaxial cable to DI)	8.2.1.2	M	Yes [ ] No [ ]	5 bits max
4	Receive settling time	8.2.1.2	M	Yes [ ] No [ ]	Second and following bits meet jitter specifications
5	Receive steady-state delay	8.2.1.2	M	Yes [ ] No [ ]	1/2 bit times max
6	Start-up bit loss (coaxial cable to DI) variability	8.2.1.2	M	Yes [ ] No [ ]	5 bits max between packets separated by ≤ 96 BT
7	Receive signal polarity	8.2.1.2	M	Yes [ ] No [ ]	More positive voltage on the coaxial cable will convert as DI A positive relative to DI B on the DI circuits
8	Edge jitter	8.2.1.2	M	Yes [ ] No [ ]	MAU receiver + cable introduce ≤ 6 ns
9	Receive function while transmitting	8.2.1.2	M	Yes [ ] No [ ]	

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8.8.6.4 Collision function

Item	Parameter	Reference	Status	Support	Value/Comment
1	Collision absence	8.2.1.3	M	Yes [ ] No [ ]	IDL signal on the CI circuit, unless sending *mau_not_available*
2	Collision Presence function require-ments	8.2.1.3	8.8.6.1/1 :X !8.8.6.1/1 :M	N/A [ ] Yes [ ] No [ ] N/A [ ] Yes [ ] No [ ]	CS0 on CI circuit at BR +25%, –15% with a duty cycle not worse than 40/60 ratio with ≥ 2 MAUs transmitting
3	No collision detection with single transmitter	8.2.1.3 8.2.2.2.4	M	Yes [ ] No [ ]	No CS0 on CI
4	Collision assertion after transmission of ≥ 20 bit times	8.2.1.3 8.2.2.2.4	8.8.6.1/1 :X !8.8.6.1/1 :M	N/A [ ] Yes [ ] No [ ] N/A [ ] Yes [ ] No [ ]	CS0 on CI ≤ 17 BT after collision
5	Collision assertion by transmission < 20 bit times	8.2.1.3 8.2.2.2.4	8.8.6.1/1 :X !8.8.6.1/1 :M	N/A [ ] Yes [ ] No [ ] N/A [ ] Yes [ ] No [ ]	CS0 on CI ≤ 29 BT after collision
6	Collision deassertion after end of collision between second MAU	8.2.1.3	M	Yes [ ] No [ ]	IDL on CI ≤ 17 BT after arrival of end of transmission
7	Collision deassertion after end of collision between more than two MAUs	8.2.1.3	M	Yes [ ] No [ ]	IDL on CI ≤ 29 BT after arrival of end of transmission from all but one MAU

8.8.6.5 Monitor function

Item	Parameter	Reference	Status	Support	Value/Comment
1	Signal path	8.2.1.4	8.8.6.1/2 :M	N/A [ ] Yes [ ] No [ ]	From DTE to MAU through CO circuit
2	Transmit disable delay	8.2.1.4	8.8.6.1/2 :M	N/A [ ] Yes [ ] No [ ]	≤ 20 ms
3	MAU function in isolated state	8.2.1.4	8.8.6.1/2 :M	N/A [ ] Yes [ ] No [ ]	Receive and collision functions are normal, XMIT disabled

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8.8.6.6 Jabber function

Item	Parameter	Reference	Status	Support	Value/Comment
1	Jabber function implementation	8.2.1.5	M	Yes [ ] No [ ]	Self-interruption of the transmitter
2	Frame timer range	8.2.1.5	M	Yes [ ] No [ ]	20 ms min, 150 ms max
3	CI circuit during jabber	8.2.1.5 8.2.2.2.4	8.8.6.1/1 :X !8.8.6.1/1 :M	N/A [ ] Yes [ ] No [ ] N/A [ ] Yes [ ] No [ ]	CS0 signal
4	Collision presence function activated after transmit disable	8.2.1.5	M	Yes [ ] No [ ]	No extraneous signal on the coaxial media
5	Unjab timer range	8.2.1.5	O	Yes [ ] No [ ]	0.5 s ± 50%
6	MAU unjab (reset) with monitor function	8.2.1.5	8.8.6.1/2 :M	N/A [ ] Yes [ ] No [ ]	Isolate message
7	MAU jabber lockup protection	9.4.1	8.8.6.1/1 :M !8.8.6.1/1 :O	N/A [ ] Yes [ ] No [ ] N/A [ ] Yes [ ] No [ ]	Jabber function not activated under worst case conditions in 9.6.5

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8.8.6.7 MAU to coaxial cable interface

Item	Parameter	Reference	Status	Support	Value/Comment
1	Input impedance	8.3.1.1	M	Yes [ ] No [ ]	R ≥ 100 kΩ
2	Total capacitive load	8.3.1.1	M	Yes [ ] No [ ]	C ≤ 4 pF
3	Bias current	8.3.1.2	M	Yes [ ] No [ ]	Max +2 μA Min –25 μA
4	Transmit offset current	8.3.1.3	M	Yes [ ] No [ ]	–37 mA to – 45 mA
5	Transmit ac component	8.3.1.3	M	Yes [ ] No [ ]	+28 mA to offset value
6	Transmitter sink current during collision	8.3.1.3	M	Yes [ ] No [ ]	No more than –25 μA at –7 V; no more than ±250 μA at –10 V
7	Rise and fall time at 10 Mb/s	8.3.1.3	M	Yes [ ] No [ ]	25 ns ± 5 ns (10–90%)
8	Rise and fall time match	8.3.1.3	M	Yes [ ] No [ ]	Within 2 ns at 10 Mb/s
9	Harmonic content at BR	8.3.1.3	M	Yes [ ] No [ ]	2nd and 3rd harmonics ≥ 20 dB below fundamental, 4th and 5th harmonics ≥ 30 dB below fundamental, 6th and 7th harmonics ≥ 40 dB below fundamental, all higher harmonics ≥ 50 dB below fundamental
10	Transmit signal polarity	8.3.1.4	M	Yes [ ] No [ ]	No inversion of signal from PLS to coaxial cable
11	Transmit signal edge jitter	8.3.1.4	M	Yes [ ] No [ ]	MAU introduce no more than 2 ns of edge jitter
12	Receive collision detection threshold	8.3.1.5	M	Yes [ ] No [ ]	–1.448 V to –1.59 V
13	Receive collision detection threshold, large impulse response	8.3.1.5	M	Yes [ ] No [ ]	–1293 mV * [1+ impulse response] if filter impulse response is larger than nominal
14	No negative edge transmission	8.3.1.4	M	Yes [ ] No [ ]	After cessation of CD output stream on DO or before first edge of next frame on DO

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8.8.6.8 MAU electrical characteristics

Item	Parameter	Reference	Status	Support	Value/Comment
1	Isolation between MDI and AUI cable (each conductor, including shields)	8.3.2.1	M	Yes [ ] No [ ]	Conforms to J.1
2	Current drawn from AUI sources	8.3.2.2	M	Yes [ ] No [ ]	≤ 0.5 A
3	Operation over VP voltage range	8.3.2.2	M	Yes [ ] No [ ]	11.28–15.75 V, any permissible AUI cable
4	Low VP circuit behavior	8.3.2.2	M	Yes [ ] No [ ]	No disruption of media
5	MAU current labeling	8.3.2.2	M	Yes [ ] No [ ]	Current consumption shall be labeled externally
6	Reliability	8.3.2.3	M	Yes [ ] No [ ]	MTBF ≥ 1 million hours of continuous operation

8.8.6.9 MAU-DTE requirements

Item	Parameter	Reference	Status	Support	Value/Comment
1	AUI electrical characteristics	8.3.3	M	Yes [ ] No [ ]	As specified in Clause 7; refer to 8.8.7.1–5
2	AUI mechanical connection	8.3.4	M	Yes [ ] No [ ]	As specified in Clause 7; refer to 8.8.7.6

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8.8.6.10 MAU to coaxial cable connection

Item	Parameter	Reference	Status	Support	Value/Comment
1	Standard N-type connector	8.5	O.1	Yes[ ] No [ ]	50 Ω, according to IEC 60169-16: 1982 and Amd. 1: 1996
*2	Coaxial tap connector	8.5.3	O.1	Yes[ ] No [ ]	
3	Capacitance	8.5.3.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	2 pF nominal at 10 MHz
4	Contact resistance	8.5.3.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	≤ 50 mΩ for shield and center conductor
5	Voltage rating	8.5.3.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	600 V dc or ac rms max
6	Dc leakage resistance between braid and external conductors	8.5.3.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	> 1 GΩ
7	Probe current rating	8.5.3.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	0.1 A per contact (probe and shield)
8	Shield current rating	8.5.3.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	1 A surge for 1 s
9	Connector housing	8.5.3.2.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	Shielding > 40 dB at 50 MHz
10	Shield probe characteristics	8.5.3.2.3	8.8.6.10/2 :M	N/A[ ] Yes [ ] No [ ]	Effective capture of outer braid

8.8.6.11 Safety requirements

Item	Parameter	Reference	Status	Support	Value/Comment
1	MAU labeling	8.6.3	O	Yes [ ] No [ ]	Data rate, current, any applicable safety warnings (recommended)
2	General safety	8.7.1	M	Yes [ ] No [ ]	Conforms to J.2
3	Susceptibility levels	8.7.3.1	M	Yes [ ] No [ ]	Either ambient plane wave field of 2 V/m from 10 kHz through 30 MHz, 5 V/m from 30 MHz through 1 GHz, or interference voltage of 1 V/ns peak slope, between coaxial cable shield and DTE earth connection
4	Emission levels	8.7.3.2	M	Yes [ ] No [ ]	Comply with applicable local and national standards

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8.8.7 PICS proforma tables for MAU AUI characteristics

8.8.7.1 Signal characteristics

Item	Parameter	Reference	Status	Support	Value/Comment
1	Signaling rate (stated on label)	7.3.2	M	Yes [ ] No [ ]	10 Mb/s
2	CS0 signal frequency (on CI)	7.3.1.2	M	Yes [ ] No [ ]	10 MHz +25%, –15%
3	CS0 signal duty cycle	7.3.1.2	M	Yes [ ] No [ ]	60:40 worst case

8.8.7.2 DI and CI driver characteristics

Item	Parameter	Reference	Status	Support	Value/Comment
1	Differential output voltage, loaded	7.4.1.1	M	Yes [ ] No [ ]	Figure 7–11
2	Differential output voltage, idle state	7.4.1.1	M	Yes [ ] No [ ]	≤ 40 mV into test load
3	Differential output voltage, start of idle	7.4.1.1	M	Yes [ ] No [ ]	Figure 7–12
4	Current into test load while idle	7.4.1.1	M	Yes [ ] No [ ]	4 mA max after 80 BT
5	Requirements after idle	7.4.1.2	M	Yes [ ] No [ ]	Second bit to Figure 7–11
6	Common-mode output voltage, ac	7.4.1.3	M	Yes [ ] No [ ]	≤ 40 mV peak, Figure 7–13
7	Differential output voltage, open circuit	7.4.1.4	M	Yes [ ] No [ ]	13 V peak max
8	Common-mode output voltage, dc	7.4.1.5	M	Yes [ ] No [ ]	≤ 5.5 V, Figure 7–13
9	Fault tolerance	7.4.1.6	M	Yes [ ] No [ ]	Figure 7–14
10	Fault current	7.4.1.6	M	Yes [ ] No [ ]	≤ 150 mA, any Figure 7–14 state

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8.8.7.3 DO receiver characteristics

Item	Parameter	Reference	Status	Support	Value/Comment
1	Unsquelched threshold	7.4.2.1	M	Yes [ ] No [ ]	160 mV max differential
2	High-to-idle transition on DO circuit	7.4.1.1	M	Yes [ ] No [ ]	Does not cause output
3	Differential input impedance at 10 MHz	7.4.2.2	M	Yes [ ] No [ ]	Real part: 77.83 Ω ± 6%; 0 ≤ phase angle (deg) ≤ real part × 0.0338
4	Common-mode range, ac	7.4.2.3	M	Yes [ ] No [ ]	3 V min 30 Hz to 40 kHz, 100 mV min 40 kHz to 10 MHz
5	Total common-mode range	7.4.2.4	M	Yes [ ] No [ ]	Magnitude of 0 to 5.5 V ac + dc
6	Common-mode current limit	7.4.2.4	M	Yes [ ] No [ ]	≤ 1 mA
7	IDL detection	7.3.1.1	M	Yes [ ] No [ ]	≤ 1.6 bit times
8	Requirements after idle	7.4.2.5	M	Yes [ ] No [ ]	Receiver in spec after start-up delay
9	Receiver fault tolerance	7.4.2.6	M	Yes [ ] No [ ]	Figure 7–16
10	Input fault current	7.4.2.6	M	Yes [ ] No [ ]	3 mA max

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8.8.7.4 CO receiver characteristics

Item	Parameter	Reference	Status	Support	Value/Comment
1	Unsquelched threshold	7.4.2.1	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	160 mV max differential
2	High-to-idle transition on DO circuit	7.4.1.1	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	Does not cause output
3	Differential input impedance at 10 MHz	7.4.2.2	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	Real part: 77.83 Ω ± 6%; 0 ≤ phase angle (deg) ≤ real part × 0.0338
4	Common-mode range, ac	7.4.2.3	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	3 V min 30 Hz to 40 kHz, 100 mV min 40 kHz to 10 MHz
5	Total common-mode range	7.4.2.4	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	Magnitude of 0 to 5.5 V ac + dc
6	Common-mode current limit	7.4.2.4	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	≤ 1 mA
7	IDL detection	7.3.1.1	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	≤ 1.6 bit times
8	Requirements after idle	7.2.4.5	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	Receiver in spec after start-up delay
9	Receiver fault tolerance	7.4.2.6	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	Figure 7–16
10	Input fault current	7.4.2.6	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	3 mA max

8.8.7.5 Circuit termination

Item	Parameter	Reference	Status	Support	Value/Comment
1	Common-mode termination	7.4.2.6	M	Yes [ ] No [ ]	If used, is to VC
2	Pins 1, 4, 8, 11, 14 impedance to VC circuit	7.5.2.8	M	Yes [ ] No [ ]	≤ 5 Ω at 5 MHz
3	Pins 1, 4, 8, 11, 14 coupling to VC circuit	7.5.2.8	M	Yes [ ] No [ ]	Capacitive

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8.8.7.6 Mechanical characteristics

Item	Parameter	Reference	Status	Support	Value/Comment
1	D-type connector dimensions	7.6.2	M	Yes [ ] No [ ]	IEC 60807-2: 1992 15-pole male
2	Shell plating material	7.6.2	M	Yes [ ] No [ ]	Conductive
3	Shell multiple contact points	7.6.2	O	Yes [ ] No [ ]	Number not defined (recommended)
4	Shell life expectancy	7.6.2	M	Yes [ ] No [ ]	≤ 5 mΩ/500 matings
5	Locking posts and mounting	7.6.1	M	Yes [ ] No [ ]	Figures 7–18, 7–20
	Pin connections:				Circuit
6	3	7.6.3	M	Yes [ ] No [ ]	Data out A
7	10	7.6.3	M	Yes [ ] No [ ]	Data out B
8	11	7.6.3	M	Yes [ ] No [ ]	Capacitor to VC
9	5	7.6.3	M	Yes [ ] No [ ]	Data in A
10	12	7.6.3	M	Yes [ ] No [ ]	Data in B
11	4	7.6.3	M	Yes [ ] No [ ]	Capacitor to VC
12	7	7.6.3	M	Yes [ ] No [ ]	Control out A
13	15	7.6.3	M	Yes [ ] No [ ]	Control out B
14	8	7.6.3	M	Yes [ ] No [ ]	Capacitor to VC
15	2	7.6.3	M	Yes [ ] No [ ]	Control in A
16	9	7.6.3	M	Yes [ ] No [ ]	Control in B
17	1	7.6.3	M	Yes [ ] No [ ]	Capacitor to VC
18	6	7.6.3	M	Yes [ ] No [ ]	Voltage common
19	13	7.6.3	M	Yes [ ] No [ ]	Voltage plus
20	14	7.6.3	M	Yes [ ] No [ ]	Capacitor to VC
21	Shell	7.6.3	M	Yes [ ] No [ ]	Protective ground (conductive shell)

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8.8.8 PICS proforma tables for 10BASE5 coaxial cable

8.8.8.1 10BASE5 coaxial cable characteristics

Item	Parameter	Reference	Status	Support	Value/Comment
1	Characteristic impedance	8.4.1.1	M	Yes [ ] No [ ]	50 Ω ± 2 Ω, measured according to IEC 60096-1: 1986 and Amd. 2: 1993
2	Impedance variation per 2 m segment	8.4.1.1	O	Yes [ ] No [ ]	±3 Ω
3	Attenuation of 500 m segment	8.4.1.2	M	Yes [ ] No [ ]	≤8.5 dB with 10 MHz sine wave, ≤6.0 dB with 5 MHz sine wave
4	Velocity of propagation	8.4.1.3	M	Yes [ ] No [ ]	Min 0.77 c
5	Edge jitter of 500 m cable	8.4.1.4	M	Yes [ ] No [ ]	≤7 ns
6	Transfer impedance	8.4.1.5	M	Yes [ ] No [ ]	According to Figure 8–7
7	Cable DC loop resistance (center conductor plus shield)	8.4.1.6	M	Yes [ ] No [ ]	≤10 mΩ/m at 20 °C
Coaxial cable properties:					
8	a) Center conductor, dielectric, shield system, insulating jacket	8.4.2.1.1	M	Yes [ ] No [ ]	
9	b) Concentricity	8.4.2.1.1	M	Yes [ ] No [ ]	≥ 92%
10	c) Jacket, shield, dielectric	8.4.2.1.1	M	Yes [ ] No [ ]	pierceable
11	d) Cable flexibility	8.4.2.1.1	M	Yes [ ] No [ ]	support bend radius of 254 mm
12	Center conductor	8.4.2.1.2	M	Yes [ ] No [ ]	2.17 mm ± 0.013 mm
13	Dielectric material	8.4.2.1.3	M	Yes [ ] No [ ]	meets 8.4.1.2, 8.4.1.3 and 8.4.2.1.1 c)
Shielding system:					
14	a) Inside diameter	8.4.2.1.4	M	Yes [ ] No [ ]	≥ 6.15 mm
15	b) Outside diameter	8.4.2.1.4	M	Yes [ ] No [ ]	8.28 mm ± 0.178 mm
16	c) Outermost shield	8.4.2.1.4	M	Yes [ ] No [ ]	> 90% coverage
17	Jacket material	8.4.2.1.5	M	Yes [ ] No [ ]	meets 8.4.1 and 8.4.2 specs
18	Jacket dimensions, Polyvinyl Chloride	8.4.2.1.5	O.2	Yes [ ] No [ ]	OD of 10.287 mm ± 0.178 mm
19	Jacket dimensions, Fluoropolymer	8.4.2.1.5	O.2	Yes [ ] No [ ]	OD of 9.525 mm ± 0.254 mm
20	Flammability and smoke criteria	8.4.2.1.5	M	Yes [ ] No [ ]	Meet applicable local and national codes
21	Jacket marking	8.4.2.2	M	Yes [ ] No [ ]	Annular rings spaced 2.5 m ± 5 cm

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Item	Parameter	Reference	Status	Support	Value/Comment
22	Color of jacket	8.4.2.2	O	Yes [ ] No [ ]	Bright (example: yellow)
Total segment dc loop resistance:					
23	a) Sum of center conductor, connector and shield	8.4.3	M	Yes [ ] No [ ]	≤5 Ω at 20° C
24	b) Inline connector pair or MAU	8.4.3	M	Yes [ ] No [ ]	≤10 mΩ at 20° C
25	Inline coaxial extension connector	8.5.1	M	Yes [ ] No [ ]	Type N plug connector
26	Coaxial cable termination	8.5.2.1	M	Yes [ ] No [ ]	50 Ω ± 1% at 0–20 MHz, phase angle ≤ 5°, power rating ≥1 Ω

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9. Repeater unit for 10 Mb/s baseband networks

NOTE—This repeater is not recommended for new installations. Since September 2011, maintenance changes are no longer being considered for this clause.

9.1 Overview

This clause specifies a repeater for use with IEEE 802.3 10 Mb/s baseband networks, with the exceptions of 10BASE-T1L (Clause 146) and 10BASE-T1S (Clause 147). A repeater for any other IEEE 802.3 network type is beyond the scope of this clause.

A repeater set connects segments of network medium together, thus allowing larger topologies and a larger MAU base than are allowed by rules governing individual segments.

Repeater sets are used to extend the network length and topology beyond what could be achieved by a single mixing segment. Mixing segments may be connected directly by a repeater set (Figure 9–1) or by several repeater units that are, in turn, connected by link segments. Repeater sets are also used as the hub in a star topology network in which DTEs attach directly to link segments (e.g., 10BASE-T, Clause 14). Allowable topologies shall contain only one operative signal path between any two points on the network. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of interpacket gap as it travels through the network. The method for validating networks with respect to these requirements is specified in Clause 13.

If the repeater set uses MAUs connected via AUIs to a repeater unit, these MAUs shall not perform the *signal_quality_error* Test function. A manufacturer may, optionally, integrate one or all MAUs into a single package with the repeater unit (internal MAUs). In all cases, the MAU portion of the repeater set has to be counted toward the maximum number of MAUs on each segment. A repeater set is not a station and does not count toward the overall limit of 1024 stations on a network.

A repeater set can receive and decode data from any segment under worst-case noise, timing, and signal amplitude conditions. It retransmits the data to all other segments attached to it with timing and amplitude restored. The retransmission of data occurs simultaneously with reception. If a collision occurs, the repeater set propagates the collision event throughout the network by transmitting a Jam signal.

9.2 References

See 1.3.

9.3 Definitions

See 1.4.

9.4 Compatibility interface

The repeater shall attach to its network segments by any of the means specified below.

9.4.1 AUI compatibility

The repeater unit shall be compatible at its AUI connector (if so equipped) as specified in Clause 7 with the exception of the *signal_quality_error* message Test, 7.2.1.2.3, which shall not be implemented.

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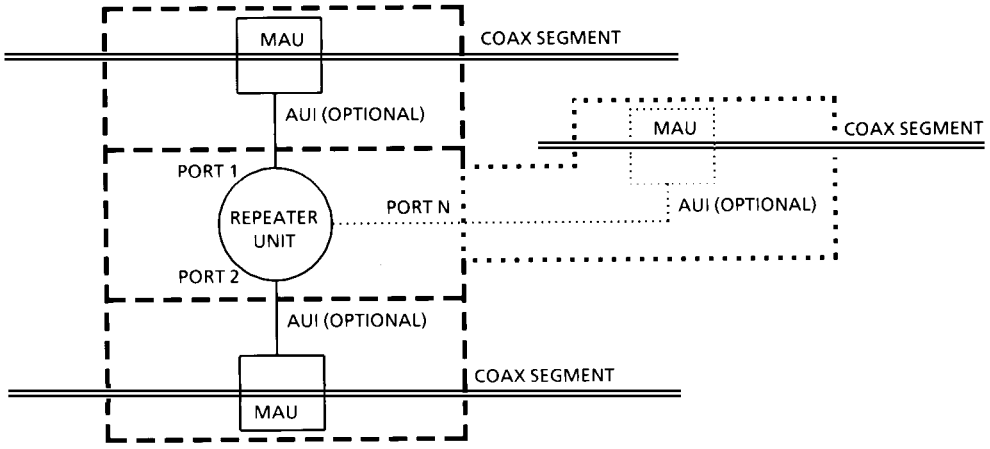

NOTE: The AUI is not necessarily exposed when the MAU is, optionally, part of the physical repeater.

Figure 9–1—Repeater set, coax-to-coax configuration

10BASE5 and 10BASE2 MAUs associated with the repeater unit shall be as specified in Clause 8 for type 10BASE5 and Clause 10 for type 10BASE2 with the following restrictions:

a) The MAU shall implement receive mode collision detect as defined in 8.3.1.5 or 10.4.1.5.
b) The MAU shall not implement the *signal_quality_error* Message Test function as defined in 8.2.1.1 and 10.3.1.1. The MAU shall not activate its Jabber function when operated under the worst-case Jabber Lockup Protection condition as specified in 9.6.5.
c) The MAU shall operate only in the normal mode as defined in 8.1.3.4, not in the monitor mode.

All other MAUs associated with the repeater unit shall be as specified in their respective clauses and shall not perform the *signal_quality_error* Message Test function.

9.4.2 Mixing segment compatibility

The repeater set, which includes MAUs integrated with the repeater package (internal MAUs), may have any of the interfaces specified in the following subclauses. The MAUs associated with the repeater that are connected in this manner shall be subject to the restrictions of MAUs as specified in 9.4.1.

9.4.2.1 Direct coaxial cable attachment compatibility

The repeater shall be compatible at its coaxial tap connector (if so equipped) as specified in 8.5.3 of the 10BASE5 standard.

9.4.2.2 “N” connector compatibility

The repeater shall be compatible at its Type N connector (if so equipped) as specified in 8.5.

9.4.2.3 BNC compatibility

The repeater shall be compatible at its BNC connector (if so equipped) as specified in 10.6.

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9.4.2.4 BFOC/2.5 (10BASE-FP) compatibility

The repeater shall be compatible at its BFOC/2.5 10BASE-FP connector (if so equipped) as specified in 15.3.2 (also see 15.1).

9.4.3 Link segment compatibility

The compatibility interfaces for link segments including IRL segments are either vendor-dependent, as specified in 9.4.3.1, or are vendor-independent MDI, as defined in the remainder of this clause. The MAUs associated with the repeater that are connected in this manner shall be subject to the restrictions of MAUs as specified in 9.4.1.

9.4.3.1 Vendor-dependent IRL

The budget allowances for the topology supported by the IRL shall ensure that the total network round-trip delay requirement is met and the maximum collision frame size of 511 bits is not exceeded. (See 13.4.1.)

9.4.3.2 Fiber optic FOIRL compatibility

The repeater shall be compatible at its FSMA connector (if so equipped) as specified in 9.9.

9.4.3.3 Twisted-pair jack compatibility

The repeater set shall be compatible at its 8-pin modular jack (if so equipped), as specified in 14.5.

9.4.3.4 Fiber optic 10BASE-FB and 10BASE-FL compatibility

The repeater shall be compatible at its BFOC/2.5 (10BASE-FB and/or 10BASE-FL) connector (if so equipped) as specified in 15.3.2 (also see 15.1).

9.5 Basic functions

9.5.1 Repeater set network properties

The repeater set shall be transparent to all network acquisition activity and to all DTEs. The repeater set shall not alter the basic fairness criterion for all DTEs to access the network or weigh it toward any DTE or group of DTEs regardless of network location. A repeater set shall not attempt to be a packet store and forward device.

Repeaters are not addressable. An addressable station on the network that controls a repeater is outside the scope of this standard.

9.5.2 Signal amplification

The repeater set (including its associated or integral MAUs) shall ensure that the amplitude characteristics of the signals at the MDI outputs of the repeater set are within the tolerance of the specification for the appropriate MAU type. Therefore, any loss of signal-to-noise ratio due to cable loss and noise pickup is regained at the output of the repeater set as long as the incoming data is within the system specification.

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9.5.3 Signal symmetry

The repeater set shall ensure that the symmetry characteristics of the signals at the MDI outputs of a repeater set are within the tolerance of the specification for the appropriate MAU type. Therefore, any loss of symmetry due to MAUs and media distortion is regained at the output of the repeater set.

9.5.4 Signal retiming

The repeater unit shall ensure that the encoded data output from the repeater unit is within the jitter tolerance of a transmitting DTE as specified in 7.3. Therefore jitter cannot accumulate over multiple segments.

9.5.5 Data handling

The repeater unit, when presented a packet at any of its ports, shall pass the data frame of said packet intact and without modification, subtraction, or addition to all other ports connected with the repeater unit. The only exceptions to this rule are when contention exists among any of the ports or when the receive port is partitioned as defined in 9.6.6. Between unpartitioned ports, the rules for collision handling (9.5.6) take precedence.

9.5.5.1 Start-of-packet propagation delays

The start-of-packet propagation delay for a repeater set is the time delay between the first edge transition of the packet on its repeated from (input) port to the first edge transition of the packet on its repeated to (output) port (or ports).

For a repeater unit with AUI connectors at input and output ports, this time shall be less than or equal to 8 bit times.

For a repeater set with internal MAUs on input and output ports, additional delays shall be allowed as enumerated in Table 9–1.

Table 9–1—Start-of-packet propagation delays (Repeater unit delay of 8 BT plus)

MAU type	Input (BT)	Output (BT)
10BASE5	6.5	3.5
10BASE2	6.5	3.5
FOIRL	3.5	3.5
10BASE-T	8	5
10BASE-FP	3	4
10BASE-FB	2	2
10BASE-FL	5	5

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9.5.5.2 Start-of-packet variability

The start-of-packet variability, defined as the total worst-case difference between start-of-packet propagation delays for successive packets separated by 96 bit times or less, shall be less than 4 bit times for a repeater unit. For a 10BASE-FB repeater set the total worst-case difference between start-of-packet propagation delays for successive packets separated by 96 bit times or less, shall be less than 2 bit times for a repeater set, all of which is allocated to the repeater unit.

9.5.6 Collision handling

9.5.6.1 Collision presence

All MAUs connected to the repeater unit shall provide uninterrupted Carrier Sense. Uninterrupted Carrier Sense means that the input messages remain valid during activity on the medium even in the presence of a collision. 10BASE5 and 10BASE2 MAUs shall provide this capability by implementing Receive Mode Collision Detection.

9.5.6.2 Jam generation

If a collision is detected on any of the ports to which the repeater set is transmitting, the repeater set shall transmit a Jam to all of the ports to which it is connected. The Jam shall be transmitted in accordance with the Repeater Unit State Diagram in Figure 9–2 and shall be as specified in 4.2.3.2.4 with the further constraint that the first 62 bits transmitted to any port shall be a pattern of alternate 1's and 0's starting with the first bit transmitted as a 1.

9.5.6.3 Collision-jam propagation delays

The start-of-collision propagation delay for a repeater set is the time delay between the first edge transition of the *signal_quality_error* signal on any of its ports to the first edge transition of the Jam on its (output) port (or ports).

For a repeater unit with AUI connectors at input and output ports, this time shall be less than or equal to 6.5 bit times.

For a repeater set with internal MAUs on input and output ports, additional delays shall be allowed as enumerated in Table 9–2.

The cessation-of-jam propagation delay for a repeater unit is the time delay between the input signals at its ports reaching a state such that Jam should end at a port and the last transition of Jam at that port. The states of the input signals that should cause Jam to end are covered in detail in the repeater state diagrams.

For a repeater unit with AUI connectors at input and output ports, this time shall be less than or equal to 5 bit times when not extending fragments. When extending fragments, this delay may be longer as required by the fragment extension algorithm. See 9.6.4.

For a repeater set with internal MAUs on input and output ports, an additional allowance for cessation-of-Jam propagation shall be allowed as specified in Table 9–3.

For a repeater set with internal MAUs on its input ports, an additional delay allowance for DI and for *signal_quality_error* de-assertion shall be made as specified in Table 9–3.

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Table 9–2—Start-of-collision jam delays (repeater unit delay of 6.5 BT plus)

MAU type	Input (BT)	Output (BT)
10BASE5	9[a]	3.5
10BASE2	9[a]	3.5
FOIRL	3.5	3.5
10BASE-T	9	5
10BASE-FP	11.5	1
10BASE-FB	3.5	2
10BASE-FL	3.5	5

[a] This does not include collision rise time on the coaxial media. For the worst-case round-trip delay calculation, collision rise time plus MAU propagation delay = 17 bit times.

Table 9–3—Cessation-of-jam delays (repeater unit delay of 5 BT plus)

MAU type	Cessation-of-Collision jam from DI (BT)		Cessation-of-Collision jam from SQE (BT)	
	Input	Output	Input	Output
10BASE5	0.5	0.5	20	0.5
10BASE2	0.5	0.5	20	0.5
FOIRL	0.5	0.5	7	0.5
10BASE-T	2	2	9	2
10BASE-FP	3	3	36	3
10BASE-FB	5	2	5	2
10BASE-FL	2	2	7	2

9.5.6.4 Transmit recovery time

It is essential that the repeater unit not monitor a port for input for a short time after the repeater stops transmitting to that port. This recovery time prevents the repeater from receiving its own transmission as a new receive activity. The minimum recovery time allowable for a repeater is implementation-dependent, but has to be greater than the sum of the delays in the transmit and receive paths for the port. In all cases the recovery time has to be less than 10 bit times from the last transition on the transmitting AU interface.

9.5.6.5 Carrier recovery time

During a collision, the *input_idle* signal is unreliable for short periods of time (bits) because of the possibility of signal cancellation on the collision segment. In order to prevent premature detection of the true end of the collision, the repeater unit has to wait for data to become sensed from a port for a short time after *signal_quality_error* has gone inactive from that port. This recovery time prevents the repeater from

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prematurely ending a Jam on an active network. The minimum carrier recovery time allowable for a repeater is implementation-dependent, but shall be greater than the CARRIER ON time after *signal_quality_error* is de-asserted. In all cases, the carrier recovery time shall be less than 4 bit times from the last transition on the AU Interface.

9.5.7 Electrical isolation

Network segments that have different isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of the repeater set.

9.6 Detailed repeater functions and state diagrams

A precise algorithmic definition is given in this subclause, providing a complete procedural model for the operation of a repeater, in the form of state diagrams. Note that whenever there is any apparent ambiguity concerning the definition of repeater operation, the state diagrams should be consulted for the definitive statement.

The model presented in this subclause is intended as a primary specification of the functions to be provided by any repeater unit. It is important to distinguish, however, between the model and a real implementation. The model is optimized for simplicity and clarity of presentation, while any realistic implementation should place heavier emphasis on such constraints as efficiency and suitability to a particular implementation technology.

It is the functional behavior of any repeater unit implementation that shall match the standard, not the internal structure. The internal details of the procedural model are useful only to the extent that they help specify the external behavior clearly and precisely. For example, the model uses a separate Transmit Timer state diagram for each port. However, in an actual implementation, the hardware may be shared.

9.6.1 State diagram notation

The notation used in the state diagrams (Figure 9–2 through Figure 9–5) follows the conventions in 1.2.1.

Description of state diagram variables

Input/Output variables

DataIn (X)

Status of DataIn input at port X.
Values: **II** ; *input_idle*; i.e., indicates no activity
–II ; indicates activity
Note that DataIn (X) may be undefined during collision but that it is a don't care in all instances when this is true.

CollIn (X)

Status of ControlIn input at port X.
Values: **SQE** ; *signal_quality_error*; i.e., indicates collision
–SQE ; indicates no collision

Out (X)

Type of output repeater is sourcing at port X.
Values: **Idle** ; Repeater is not transmitting
–Idle ; Repeater is transmitting Preamble Pattern or Data or Jam or TwoOnes.
Preamble Pattern ; Repeater is sourcing alternating 1's and 0's on port X.

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Data ; Repeater is repeating data frame on port X.
Jam ; Repeater is sourcing Jam on port X.
TwoOnes ; Repeater is sourcing two consecutive Manchester-encoded ones on port X.

DisableOut (X)
Override of Out (X)
Values: **ON** ; Disable repeater transmission regardless of value of Out (X).
–ON ; Repeater transmission depends on the value of Out (X).

Port variables

TT (X)
Transmit Timer indicates number of bits transmitted on port X.
Values: Positive integers

Inter-Process flags

AllDataSent

All received data frame bits have been sent.

Bit Transmitted

Indicates a bit has been transmitted by the repeater unit.

DataRdy

Indicates the repeater has detected the SFD and is ready to send the received data. The search for SFD shall not begin before 15 bits have been received. Note, transmit and receive clock differences shall also be accommodated.

Tw1
Wait Timer for the end of transmit recovery time (see 9.5.6.4). It is started by StartTw1. Tw1Done is satisfied when the end of transmit recovery time is completed.

Tw2
Wait Timer for the end of carrier recovery time (see 9.5.6.5). It is started by StartTw2. Tw2Done is satisfied when the timer has expired.

Tw3
Wait Timer for length of continuous output (see 9.6.5). It is started by StartTw3. Tw3Done is satisfied when the timer has expired.

Tw4
Wait Timer for time to disable output for Jabber Lockup Protection (see 9.6.5). It is started by StartTw4. Tw4Done is satisfied when the timer has expired.

Port functions

Port (*Test*)
A function that returns the designation of a port passing the test condition. For example, Port (CollIn=SQE) returns the designation: X for a port that has SQE true. If multiple ports meet the test condition, the Port function will be assigned one and only one of the acceptable values.

Port designation

Ports are referred to by number. Port information is obtained by replacing the X in the desired function with the number of the port of interest. Ports are referred to in general as follows:

ALL Indicates all repeater ports are to be considered. All ports shall meet test conditions in order for the test to pass.

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ANY Indicates all ports are to be considered. One or more ports shall meet the test conditions in order for the test to pass.

ONLY1 Indicates all ports are to be considered. One, but not more than one, port shall meet the test condition in order for the test to pass.

X Generic port designator. When X is used in a state diagram, its value is local to that diagram and not global to the set of state diagrams.

N Is defined by the Port function on exiting the IDLE state of Figure 9–2. It indicates a port that caused the exit from the IDLE state.

M Is defined by the Port function on exiting the TRANSMIT COLLISION state of Figure 9–2. It indicates the only port where CollIn=SQE.

ALLXN Indicates all ports except N should be considered. All ports considered shall meet the test conditions in order for the test to pass.

ALLXM Indicates all ports except M should be considered. All ports considered shall meet the test conditions in order for the test to pass.

ANYXN Indicates any port other than N meeting the test conditions shall cause the test to pass.

ANYXM Indicates any port other than M meeting the test conditions shall cause the test to pass.

9.6.2 Data and collision handling

The repeater unit shall implement the CARRIER_ON function for all its ports. Upon detection of carrier from one port, the repeater unit shall repeat all received signals in the Data Frame from that port to the other port (or ports).

The repeater unit data and collision-handling algorithm shall be as defined in Figure 9–2.

9.6.3 Preamble regeneration

The repeater unit shall output at least 56 bits of preamble followed by the SFD. When the repeater unit has to send more than 56 bits, the maximum length preamble pattern it shall send is the number received plus 6. If the receive port is type 10BASE-FB, then the maximum length preamble pattern it shall send is the number received plus 2.

NOTE—Type 10BASE-FB ports always receive at least 56 bits of preamble due to the constraints on the transmitter and link.

9.6.4 Fragment extension

If the received bit sequence from CARRIER_ON to CARRIER_OFF is fewer than 96 bits in length, including preamble, the repeater unit shall extend the output bit sequence with Jam such that the total number of bits output from the repeater unit shall equal 96.

9.6.5 MAU Jabber Lockup Protection

MAU Jabber Lockup Protection operates as shown in the MAU Jabber Lockup Protection state diagram. The repeater unit shall interrupt its output if it has transmitted continuously for longer than 5 ms or 50 000 bit times – 20% + 50%. The repeater unit shall then, after 96 to 116 bit times (9.6 to 11.6 μs), re-enable transmissions.

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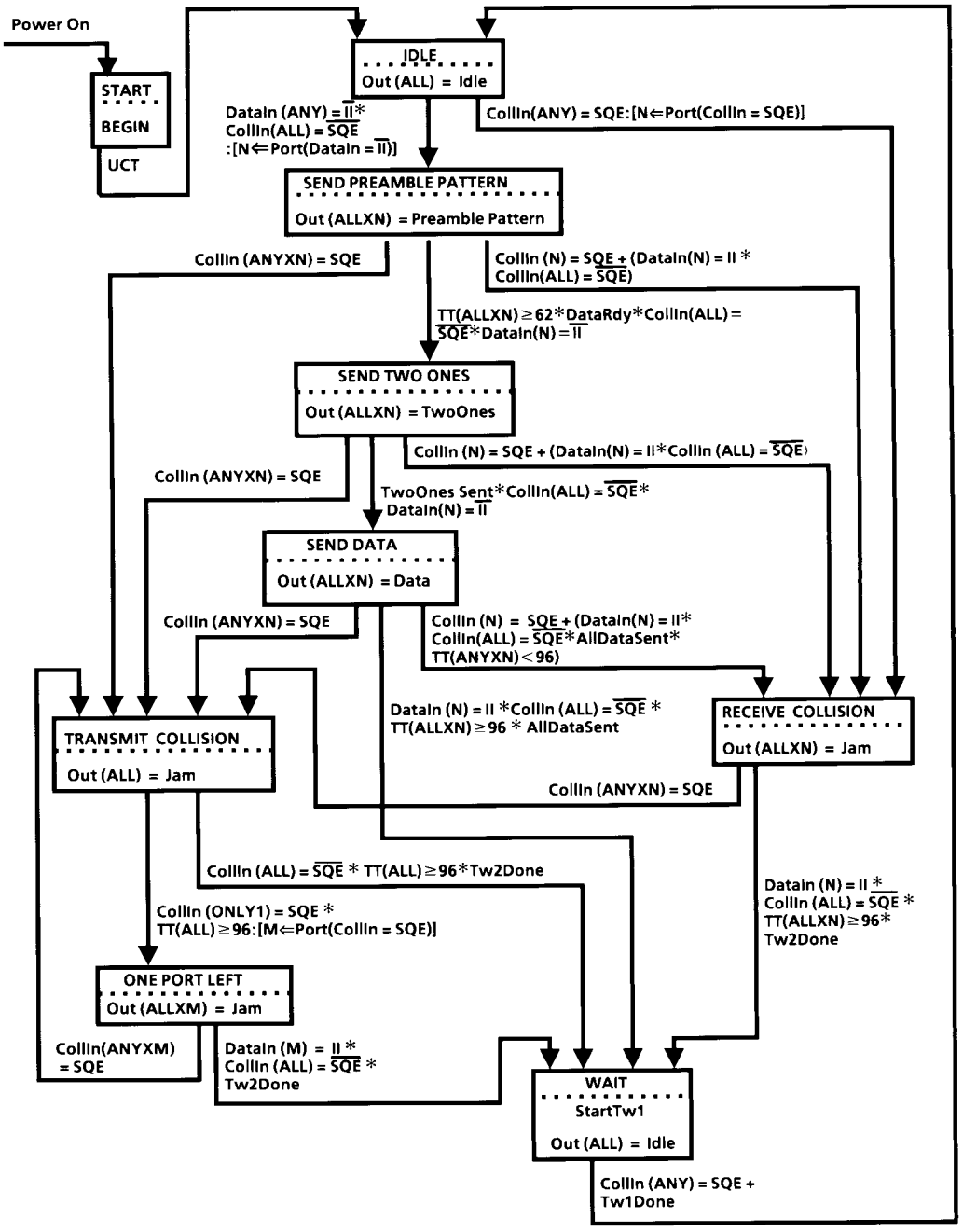

NOTE: Out (X) = Idle in all instances unless specified otherwise.

Figure 9–2—Repeater unit state diagram

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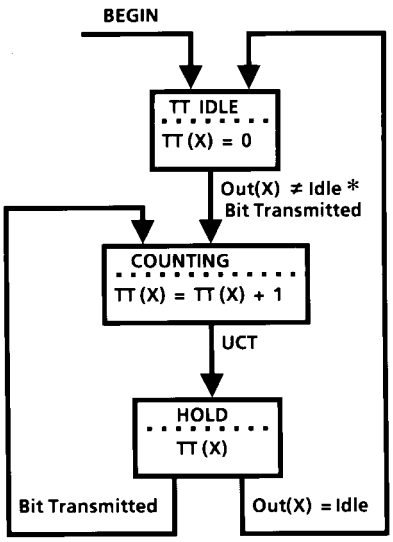

Figure 9–3—Transmit timer state diagram for Port X

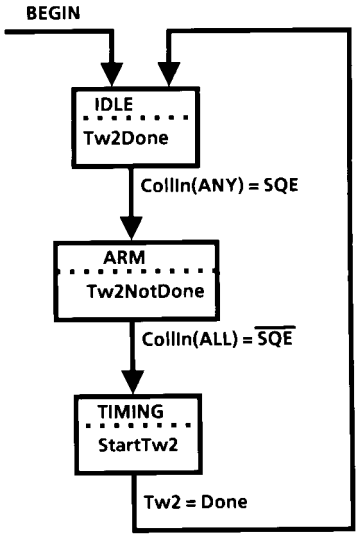

Figure 9–4—Tw2 state diagram

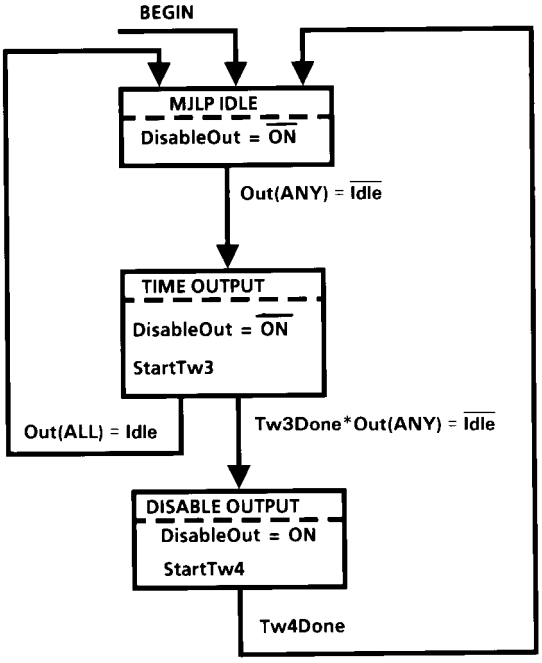

Figure 9–5—MAU jabber lockup protection state diagram

9.6.6 Auto-Partitioning/Reconnection (optional)

9.6.6.1 Overview

In large multisegment networks it may be desirable that the repeater unit protect the network from some fault conditions that would halt all network communication. A potentially likely cause of this condition could be due to a cable break, a faulty connector, or a faulty or missing termination.

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In order to isolate a faulty segment's collision activity from propagating through the network, the repeater unit may optionally implement an auto-partition algorithm and, on detection of the malfunction being cleared, an auto-reconnection algorithm.

9.6.6.2 Detailed auto-partition/reconnection algorithm state diagram

Repeater sets with 10BASE-T MAUs shall implement an auto-partition/reconnection algorithm on those parts. The repeater unit may optionally implement an auto-partition/reconnection algorithm that protects the rest of the network from an open-circuited segment. If the repeater unit provides this function, it shall conform to the state diagram of Figure 9–6.

The algorithm defined in Figure 9–6 shall isolate a segment from the network when one of the following two conditions has occurred on the segment:

a) When a consecutive collision count has been reached; or
b) When a single collision duration has exceeded a specific amount of time.

When a segment is partitioned, DataIn (X) and CollIn (X) from that segment are forced to II (input idle) and –SQE (no collision), respectively, so that activity on the port will not affect the repeater unit. Output from the repeater to the segment is not blocked.

The segment will be reinstated when the repeater has detected activity on the segment for more than the number of bits specified for Tw5 without incurring a collision.

Description of state diagram variables and constants

Port constants

CCLimit
: The number of consecutive collisions that have to occur before a segment is partitioned. The value shall be greater than 30.

Input/Output variables

DIPresent(X)
: Data in from the MAU on port X. (This input is gated by the partition state diagram to produce Dataln (X) to the main state diagram.)
Values: II = *input_idle* ; no activity
–II = Input not idle ; activity

CIPresent(X)
: Control input from the MAU on port X. (This input is gated by the partition state diagram to produce CollIn (X) to the main state diagram.)
Values: SQE = *signal_quality_error* ; indicates collision
–SQE ; indicates no collision

Port variables

CC(X)
: Consecutive port collision count on a particular port X. Partitioning occurs on a terminal count of CCLimit being reached.
Values: Positive integers up to a terminal count of CCLimit.

Inter-Process Flags

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Tw5

Wait Timer for length of packet without collision. Its value shall be between 450 and 560 bit times. It is started by StartTw5. Tw5Done is satisfied when the timer has expired.

Tw6

Wait Timer for excessive length of collision. Its value shall be between 1000 and 30 000 bit times. It is started by StartTw6. Tw6Done is satisfied when the timer has expired.

9.7 Electrical isolation

There are two electrical power distribution environments to be considered that require different electrical isolation properties.

Environment A—When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.

Environment B—When a LAN crosses the boundary between separate power distribution systems or the boundaries of a single building.

The repeater unit shall comply with applicable local and national codes related to safety. See [B19].

9.7.1 Environment A requirements

Attachment of network segments via repeaters (sets) possessing internal MAUs requires electrical isolation of 500 V rms, 1 min withstand, between the segment and the protective ground of the repeater unit.

For repeater ports that connect to external MAUs via an AU Interface, the requirement for isolation is encompassed within the isolation requirements of the basic MAU/medium standard. (See 8.3.2.1, 9.9.3.1, 10.4.2.1, 14.3.1.1, and 15.3.4.) The repeater unit shall not require any electrical isolation between exposed AU Interfaces or between exposed AU Interfaces and chassis ground of the repeater unit. No isolation boundary need therefore exist at any AUI compatible interface (that is, “D” connector) provided by a repeater unit.

9.7.2 Environment B requirements

The attachment of network segments, which cross environment A boundaries, requires electrical isolation of 1500 V rms, 1 min withstand, between each segment and all other attached segments and also the protective ground of the repeater unit.

If segments are of an electrically conductive medium, it is recommended that this isolation be provided by the use of external MAUs connected by AU Interfaces. If internal MAUs are used for attachment to conductive media segments, then the segments shall be installed such that it is not possible for an equipment user to touch the trunk cable screen or signal conductor. A repeater of this variety requires professional installation.

The requirements for interconnected electrically conducting LAN segments that are partially or fully external to a single building environment may require additional protection against lightning strike hazards. Such requirements are beyond the scope of this standard.

It is recommended that the above situation be handled by the use of a nonelectrically conducting LAN segment (see 9.9 or Clause 15).

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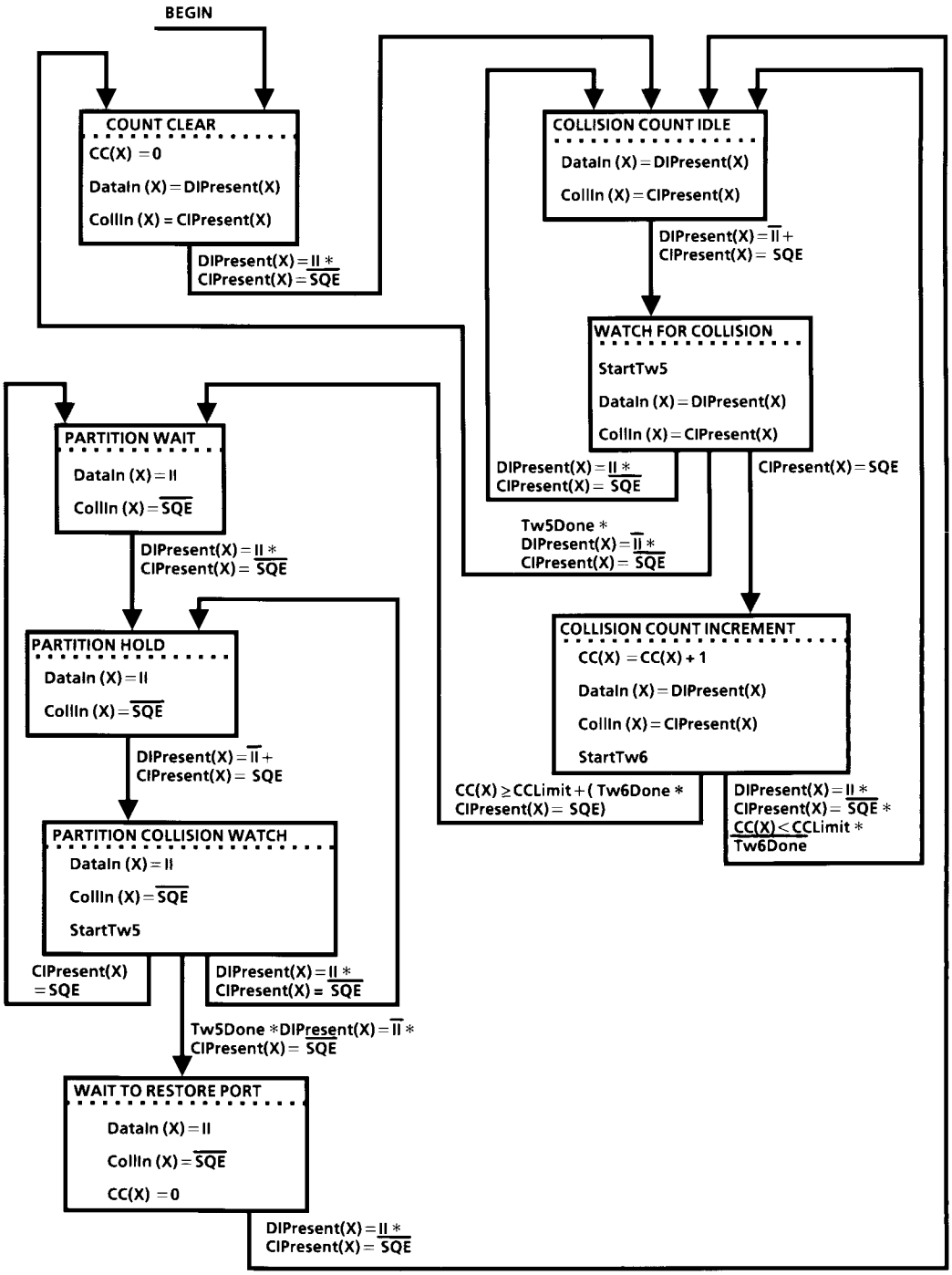

Figure 9–6—Partitioning state diagram for Port X

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9.8 Reliability

A 2-port repeater set shall be designed to provide a mean time between failure (MTBF) of at least 50 000 hours of continuous operation without causing a communication failure among stations attached to the network medium. Repeater sets with more than two ports shall add no more than 3.46×10^{-6} failures per hour for each additional port.

The repeater set electronics shall be designed to minimize the probability of component failures within the repeater electronics that prevent communication among the other MAUs on the individual coaxial cable segments. Connectors and other passive components comprising the means of connecting the repeater to the coaxial cable shall be designed to minimize the probability of total network failure.

9.9 Medium attachment unit and baseband medium specification for a vendor-indepedent FOIRL

9.9.1 Scope

9.9.1.1 Overview

A vendor-independent FOIRL provides a standard means for connecting a repeater via optical fiber to another repeater or to a DTE. It thus extends the network length and topology beyond that which could be achieved by interconnecting coaxial cable segments via repeater sets only, as defined in 8.6 or 10.7. A vendor-independent FOIRL is suited for interconnecting repeaters and their respective segments located in different buildings. FOMAUs that are used for the DTE end of the link segment are beyond the scope of this clause. See Clause 18.

NOTE—The FOMAU specified in 9.9 has been superseded by the specification to be found in Clause 18. The new specification is fully compatible (except for media connector) with the specifications of 9.9 at the MDI. The new specification calls out more recent practice in connectors and state machines. It also provides improved performance for long link segments and reflects more recent industry input on flux parameters.

In particular, this clause defines the following:

a) The functional, optical, electrical, and mechanical characteristics of a fiber optic MAU (FOMAU) suitable for interfacing to a repeater unit, either directly (FOMAU and repeater unit integrated into a single package) or via an AUI mechanical connection.
b) Various optical fiber sizes suitable for connecting only two FOMAUs.

A schematic of the vendor-independent FOIRL and its relationship to the repeater unit is shown in Figure 9–7. The vendor-independent FOIRL comprises an optical fiber cable link segment, a vendor-independent FOMAU at each end of the link segment and, if present, AUI cables.

The purpose of this specification is to enable interoperability of FOMAUs that originate from different manufacturers, thereby facilitating the development of simple and inexpensive inter-repeater links (IRLs). To satisfy this objective, the FOMAU has the following general characteristics:

— Enables coupling the repeater unit PLS directly, or by way of the AUI mechanical connection, to the explicit baseband optical fiber cable link segment defined in this clause of the standard.
— Supports signaling at a data rate of 10 Mb/s.
— Provides for driving up to 1000 m of an optical fiber cable link segment.
— Operates indistinguishably from other types of repeater set MAUs, as defined in their respective 10 Mb/s baseband MAU sections when viewed from the AU Interface.

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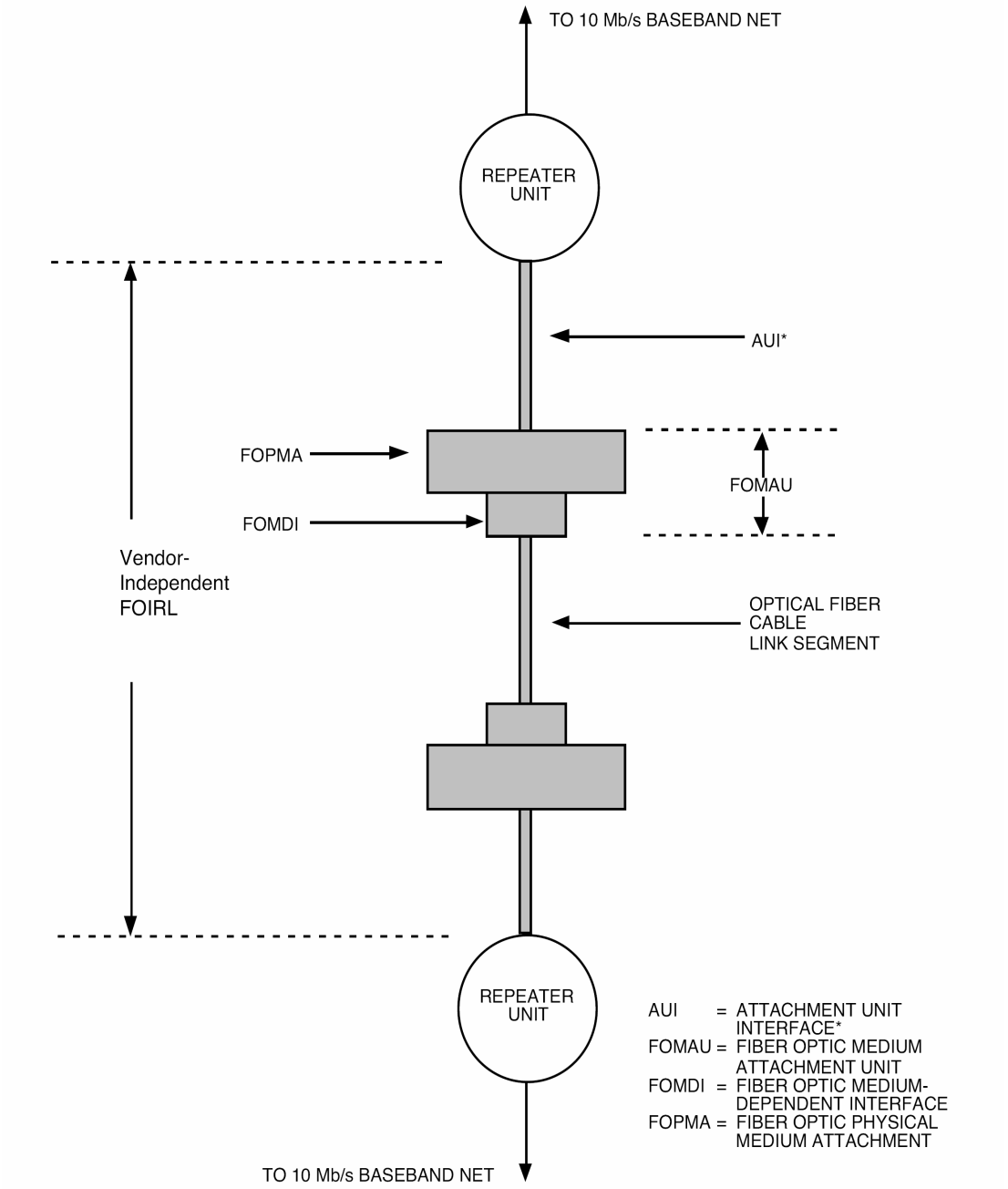

See 9.9.1.3 for implementation requirements

Figure 9–7—Schematic of the vendor-independent FOIRL and its relationship to the repeater unit

— Supports 10 Mb/s baseband system configurations as defined in Clause 13 of this standard.

— Allows integration of the FOMAU into a single package with the repeater unit, thereby eliminating the need for an AUI mechanical connection.

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9.9.1.2 Application perspective: FOMAU and medium objectives

This clause states the broad objectives underlying the vendor-independent FOIRL specification defined throughout this clause of the standard. These are as follows:

a) Provide the physical means for connecting a repeater via fiber to another repeater or to a DTE.
b) Define a physical interface for the vendor-independent FOMAU component of the vendor-independent FOIRL that can be implemented independently among different manufacturers of hardware and achieve the intended level of compatibility when interconnected in a common IRL.
c) Provide a communication channel capable of high bandwidth and low bit error ratio performance. The resultant BER of the FOIRL should be less than one part in 10^{10}.
d) Provide a means to prevent packet transmission through an FOIRL when transmission capability in one or both directions is disrupted.

9.9.1.3 Compatibility considerations

All implementations of the vendor-independent FOMAU shall be compatible at the FOMDI and at the AUI (when physically and mechanically implemented).

This standard provides an optical fiber cable link segment specification for the interconnection of only two FOMAU devices. The medium itself, the functional capability of the FOMAU, and the AUI are defined to provide the highest possible level of compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the FOMAU in an application-dependent manner provided the FOMDI and AUI are satisfied. (The provision of the physical and mechanical implementation of the AUI is optional.)

9.9.1.4 Relationship to AUI

A close relationship exists between this subclause and Clause 7. This subclause specifies all of the physical medium parameters, all of the FOPMA logical functions residing in the FOMAU, and references the AUI defined in Clause 7 with the exception of the *signal_quality_error* message Test of 7.2.1.2.3(3), which shall not be implemented, that is, shall not be enabled when connected to a repeater unit.

NOTE—The specification of a FOMAU component requires the use of both this subclause and Clause 7 for the AUI specifications.

9.9.1.5 Mode of operation

The FOMAU functions as a direct connection between the optical fiber cable link segment and the repeater unit. During collision-free operation, data from the repeater unit is transmitted into the FOMAU's transmit optical fiber, and all data in the FOMAU's receive optical fiber is transmitted to the repeater unit.

9.9.2 FOMAU functional specifications

The FOMAU component provides the means by which signals on the three AUI signal circuits are coupled:

a) From the repeater unit into the FOMAU's transmit optical fiber, and
b) From the FOMAU's receive optical fiber to the repeater unit.

To achieve this basic objective, the FOMAU component contains the following functional capabilities to handle message flow between the repeater unit and the optical fiber cable link segment:

a) *Transmit function*: The ability to receive serial bit streams from the attached repeater unit and transmit them into the FOMAU's optical fiber.

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b) *Receive function*: The ability to receive serial data bit streams from the FOMAU's receive optical fiber and transmit them to the attached repeater unit.
c) *Collision Presence function*: The ability to detect, and report to the attached repeater unit, an FOIRL collision.
d) *Jabber function*: The ability to automatically interrupt the Transmit function and inhibit an abnormally long output data stream.
e) *Low Light Level Detection function*: The ability to automatically interrupt the Receive function and inhibit the reception of signals from the FOMAU's receive optical fiber, which could result in abnormally high BERs.

9.9.2.1 Transmit function requirements

At the start of a packet transmission into the FOMAU's transmit optical fiber, no more than two bits (two full bit cells) of information may be received from the DO circuit and not transmitted into the FOMAU's transmit optical fiber. In addition, it is permissible for the first bit sent to contain encoded phase violations or invalid data. All successive bits of the packet shall be transmitted into the FOMAU's transmit optical fiber and shall exhibit the following:

a) No more edge jitter than that given by the sum of the worst-case edge jitter components specified in 7.4.3.6, 7.5.2.1, and 9.9.4.1.7, and
b) The levels and waveforms specified in 9.9.4.1.

The FOMAU DO circuit shall comply with the AUI specification for receivers given in 7.4.2. The FOMAU's DI circuit driver shall comply with the AUI specification for drivers given in 7.4.1.

The steady-state propagation delay between the DO circuit receiver input and the FOMAU's transmit optical fiber input shall not exceed one-half a bit cell. It is recommended that the designer provide an implementation in which a minimum threshold level is required on the DO circuit to establish a transmit bit stream.

The higher optical power level transmitted into the FOMAU's transmit optical fiber shall be defined as the low (LO) logic state on the optical fiber link segment. There shall be no logical signal inversions between the DO circuit and the FOMAU's transmit optical fiber, as specified in 9.9.4.1.5.

The difference in the start-up delay (bit loss plus invalid bits plus steady-state propagation delay), as distinct from the absolute start-up delays, between any two packets that are separated by 9.6 μs or less shall not exceed 2 bit cells.

The FOMAU shall loop back a packet received from the DO circuit into the DI circuit. At the start of a packet transmission, no more than five bits of information may be received from the DO circuit and not transmitted into the DI circuit. It is permissible for the first bit sent to contain encoded phase violations or invalid data. All successive bits of the packet shall be transmitted into the DI circuit and shall exhibit no more edge jitter than that specified for signals transmitted into the DI circuit by the Receive function, as specified in 9.9.2.2. The steady-state propagation delay between the DO circuit receiver input and the DI circuit driver output for such signals shall not exceed one bit cell. There shall be no logical signal inversions between the DO circuit and the DI circuit during collision-free transmission.

When the DO circuit has gone idle after a packet has been transmitted into the FOMAU's transmit optical fiber, the FOMAU shall not activate the Collision Presence function so as not to send the *signal_quality_error* message Test of 7.2.1.2.3(3) to the repeater unit.

During the idle state of the DO circuit, the Transmit function shall output into the transmit optical fiber an optical idle signal as specified in 9.9.4.1.4. The transmitted optical signals shall exhibit the optical power levels specified in 9.9.4.1.8. At the end of a packet transmission, the first optical idle signal pulse transition

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to the higher optical power level has to occur no sooner than 400 ns and no later than 2100 ns after the packet's last transition to the lower optical power level. This first optical pulse has to meet the timing requirements of 9.9.4.1.4.

The FOMAU shall not introduce extraneous optical signals into the transmit optical fiber under normal operating conditions, including powering-up or powering-down of the FOMAU.

9.9.2.2 Receive function requirements

At the start of a packet reception from the FOMAU's receive optical fiber, no more than two bits (two full bit cells) of information may be received from the FOMAU's receive optical fiber and not transmitted into the DI circuit. It is permissible for the first bit transmitted into the DI circuit to contain encoded phase violations or invalid data. All successive bits of the packet shall be transmitted into the DI circuit and shall exhibit the following:

a) The levels and waveforms specified in 7.4.1, and
b) No more edge jitter than that given by the sum of the worst-case edge jitter components specified in 7.4.3.6, 7.5.2.1, 9.9.4.1.7, 9.9.4.2.2, and 9.9.5.1.

The steady-state propagation delay between the output of the FOMAU's receive optical fiber and the output of the DI circuit driver shall not exceed one-half a bit cell. There shall be no logical signal inversions between the FOMAU's receive optical fiber and the DI circuit during collision-free operation, as specified in 9.9.4.2.3.

The difference in the start-up delay (bit loss plus invalid bits plus steady-state propagation delay), as distinct from the absolute start-up delays, between any two packets that are separated by 9.6 μs or less shall not exceed 2 bit cells.

The FOMAU shall not introduce extraneous signals into the DI circuit under normal operating conditions, including powering-up or powering-down of the FOMAU.

9.9.2.3 Collision Presence function requirements

The signal presented to the CI circuit in the absence of an SQE signal shall be the IDL signal.

The signal presented to the CI circuit during the presence of a collision shall be the CS0 signal, a periodic pulse waveform of frequency 10 MHz +25% –15% with pulse transitions that are no less than 35 ns and no greater than 70 ns apart at the zero crossing points. This signal shall be presented to the CI circuit no more than 3.5 bit times after the simultaneous appearance of signals at both the input of the FOMAU's transmit optical fiber and the output of the FOMAU's receive optical fiber. This signal shall be de-asserted no earlier than 4.5 bit times and no later than 7 bit times after the above defined collision condition ceases to exist.

During a collision, if a packet is received at the DO circuit before a packet is received at the FOMAU's receive optical fiber, then only the packet received at the DO circuit shall be transmitted into the DI circuit, as specified in 9.9.2.1. Conversely, if during a collision a packet is received at the FOMAU's receive optical fiber before a packet is received at the DO circuit, then only the packet received at the FOMAU's receive optical fiber shall be transmitted into the DI circuit, as specified in 9.9.2.2. In the event of both packets being received at their respective ports within 3.5 bit times of each other, then either one, but only one, of the packets shall be selected to be transmitted into the DI circuit.

The Collision function shall not introduce extraneous signals into the CI circuit under normal operating conditions, including powering-up or powering-down of the FOMAU.

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9.9.2.4 Jabber function requirements

The FOMAU shall have the capability, as defined in Figure 9–9, to interrupt a transmission from the repeater unit that exceeds a time duration determined by the FOMAU. This time duration shall not be less than 20 ms nor more than 150 ms. If the packet being transmitted is still being transmitted after the specified time duration, the FOMAU shall activate the Jabber function by the following:

a) First inhibiting the transmission of bits from its DO circuit into its transmit optical fiber,
b) Then transmitting into its transmit optical fiber the optical idle signal specified in 9.9.4.1.4, and
c) Presenting the CS0 signal to the CI circuit.

Once the error condition has been cleared, the FOMAU shall reset the Jabber function and present the IDL signal to the CI circuit:

a) On power reset, and
b) Optionally, automatically after a continuous period of 0.5 s ± 50% of inactivity on the DO circuit.

The FOMAU shall not activate its Jabber function when operated under the worst-case Jabber Lockup Protection condition specified in 9.6.5.

When both the Jabber function and the Low Light Level Detection function (see 9.9.2.5) have been activated, the Jabber function shall override the Low Light Level Detection function.

9.9.2.5 Low Light Level Detection function requirements

The FOMAU shall have a low light level detection capability, as defined in Figure 9–10, whereby it shall interrupt the reception of both the optical idle signal and packets from the FOMAU's receive optical fiber when reliable reception can no longer be assured. This error condition shall not be activated if the peak optical power level at the output of the FOMAU's receive optical fiber exceeds –27 dBm. It shall be activated before the peak optical power level at the output of the FOMAU's receive optical fiber has fallen to a level that is lower than the peak optical power level that corresponds to a BER = 10^{-10} for the FOMAU under consideration. Once this error condition has been activated, the FOMAU shall, no earlier than 30 bit times and no later than 200 bit times

a) Disable its Receive function so that the transmission of bits from its receive optical fiber to the DI circuit is inhibited.
b) Assure that only the optical idle signal is transmitted into its transmit optical fiber, irrespective of the state of the DO circuit.
c) Disable its Transmit function during the period of time that the FOMAU recognizes the presence of a packet on the DO circuit such that the transmission of the packet from the DO circuit into the DI circuit is inhibited.

Once this error condition has been cleared, the FOMAU shall return automatically to its normal mode of operation within 40 bit times once the DO circuit is in the idle state.

When both the Jabber function (see 9.9.2.4) and the Low Light Level Detection function have been activated, the Jabber function shall override the Low Light Level Detection function.

NOTE—It is recommended that, for diagnostic purposes, the status of the Low Light Level Detection function be indicated on the exterior of the FOMAU package.

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9.9.2.6 Repeater Unit to FOMAU Physical Layer messages

The following messages can be received by the FOMAU Physical Layer entities from the repeater unit:

Message	Circuit	Signal	Meaning
output	DO	CD1, CD0	Output information
output_idle	DO	IDL	No data to be output

9.9.2.7 FOMAU Physical Layer to repeater unit messages

The following messages can be sent by the FOMAU Physical Layer entities to the repeater unit:

Message	Circuit	Signal	Meaning
input	**DI**	**CD1, CD0**	**Input information**
input_idle	DI	IDL	No information to be input
fomau_available	CI	IDL	FOMAU is available for output
signal_quality_error	CI	CS0	Collision or error detected by FOMAU

9.9.2.7.1 *input* message

The FOMAU Physical Layer sends an *input* message to the repeater unit when the FOMAU has a bit of data to send to the repeater unit. The physical realization of the *input* message is a CD0 or CD1 sent by the FOMAU to the repeater unit on the DI circuit. The FOMAU sends CD0 if the input bit is a zero, or CD1 if the input bit is a one. No retiming of the CD1 or CD0 signals takes place within the FOMAU.

9.9.2.7.2 *input_idle* message

The FOMAU Physical Layer sends an *input_idle* message to the repeater unit when the FOMAU does not have data to send to the repeater unit. The physical realization of the *input_idle* message is the IDL signal sent by the FOMAU to the repeater unit on the DI circuit.

9.9.2.7.3 *fomau_available* message

The FOMAU Physical Layer sends the *fomau_available* message to the repeater unit when the FOMAU is available for output, and when the FOMAU has activated the Low Light Level Detection function in accordance with the Low Light Level Detection function requirements of 9.9.2.5 and Figure 9–10. The *fomau_available* message shall be sent by a FOMAU that is prepared to output data. The physical realization of the *fomau_available* message is an IDL signal sent by the FOMAU to the repeater unit on the CI circuit.

9.9.2.7.4 *signal_quality_error* message

The *signal_quality_error* message shall be implemented in the following fashion:

a) When the FOMAU has completed the transmission of a packet into its transmit optical fiber, it shall not send any *signal_quality_error* message Test sequence.

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b) The simultaneous appearance of packets at both the input of a FOMAU's transmit optical fiber and the output of its receive optical fiber shall cause the *signal_quality_error* message to be sent by the FOMAU to the repeater unit.
c) When the FOMAU has activated the Jabber function, it shall send the *signal_quality_error* message in accordance with the Jabber function requirements of 9.9.2.4 and Figure 9–9.

The physical realization of the *signal_quality_error* message is the CS0 signal sent by the FOMAU to the repeater unit on the CI circuit.

The FOMAU is required to assert the *signal_quality_error* message at the appropriate times whenever the FOMAU is powered and not just when the repeater unit is providing output data.

9.9.2.8 FOMAU state diagrams

The state diagrams, Figure 9–8, Figure 9–9, and Figure 9–10, depict the full set of allowed FOMAU state functions relative to the control circuits of the repeater unit/FOMAU interface for FOMAUs. Messages used in these state diagrams are explained as follows:

NOTE—Figure 9–8, Figure 9–9, and Figure 9–10 should all be considered together.

a) *enable_opt_driver* : Activates the path employed during normal operation to cause the FOMAU transmitter to impress the packet data received from the DO circuit into the FOMAU's transmit optical fiber.
b) *disable_opt_driver* : Deactivates the path employed during normal operation to cause the FOMAU transmitter to impress the packet data received from the DO circuit into the FOMAU's transmit optical fiber.
c) *enable_opt_idle_driver* : Causes the FOMAU transmitter to impress the optical idle signal into the FOMAU's transmit optical fiber.
d) *disable_opt_idle_driver* : Causes the FOMAU to stop transmitting the optical idle signal into the FOMAU's transmit optical fiber.
e) *enable_loop_back* : Activates the path employed during normal operation to cause the FOMAU Transmit function to impress the packet data received from the DO circuit into the DI circuit.
f) *disable_loop_back* : Deactivates the path employed during normal operation to cause the FOMAU Transmit function to impress the packet data received from the DO circuit into the DI circuit.
g) *enable_opt_receiver* : Activates the path employed during normal operation to cause the FOMAU to impress the packet data received from the FOMAU's receive optical fiber into the DI circuit.
h) *disable_opt_receiver* : Deactivates the path employed during normal operation to cause the FOMAU to impress the packet data received from the FOMAU's receive optical fiber into the DI circuit.
i) [*start_packet_timer*] : Starts a timing function which is used to monitor the amount of time the FOMAU is transmitting a packet into the transmit optical fiber. The timing function is maintained as long as *output* is true and is stopped on the transition to *output_idle true.* The term *packet_timer_done* is satisfied when the timing function has run to expiration (see 9.9.2.4).
j) [*start_unjab_timer*] : Starts a timing function that is used to monitor the amount of time that the Jabber error condition has been clear. The timing function is maintained as long as *output_idle* is true and is stopped on the transition to *output true*. The term *unjab_timer_done* is satisfied when the timing function has run to expiration (see 9.9.2.4).

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k) *opt_input* : Signifies that a packet is present at the FOMAU's receive optical fiber.
l) *opt_input_idle* : Signifies that a packet is no longer present at the FOMAU's receive optical fiber.
m) *opt_input_coll_select* : Signifies that, during a collision, a packet has been received at the DO circuit within 3.5 bit times of a packet being received at the FOMAU's receive optical fiber, and that only the packet received at the FOMAU's receive optical fiber is to be transmitted into the DI circuit.
n) *output_coll_select* : Signifies that, during a collision, a packet has been received at the DO circuit within 3.5 bit times of the packet being received at the FOMAU's receive optical fiber, and that only the packet received at the DO circuit is to be transmitted into the DI circuit.

The following abbreviations have been used in Figure 9–8, Figure 9–9, and Figure 9–10:

— LLP = Low Light Level Condition Present
— LLNP = Low Light Level Condition Not Present
— p_t_d = *packet_timer_done*
— p_t_n_d = *packet_timer_not_done*
— * = logical AND operator

9.9.3 FOMAU electrical characteristics

9.9.3.1 Electrical isolation

NOTE—Since February 2021, electrical isolation requirements are in J.1.

Electrical isolation shall be provided between FOMAUs attached to the FOIRL by the optical fiber cable link segment. There shall be no conducting path between the optical medium connector plug and any conducting element within the optical fiber cable link segment. This isolation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50–60 Hz for 60 s, applied as specified in 5.3.2 of IEC 60950: 1991.
b) 2250 V dc for 60 s, applied as specified in 5.3.2 of IEC 60950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time of half value), as defined IEC 60060.

There shall be no isolation breakdown, as defined in 5.3.2 of IEC 60950: 1991, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 V dc.

NOTE—Although isolation is provided by the optical fiber cable link segment, it is recommended that the normal noise immunity provided by common-mode isolation on the AUI be retained.

9.9.3.2 Power consumption

The current drawn by the FOMAU shall not exceed 0.5 A when powered by the AUI source. The FOMAU shall be capable of operating from all possible voltage sources as supplied by the repeater unit (7.5.2.5 and 7.5.2.6) through the resistance of all permissible AUI cables. The surge current drawn by the FOMAU on power-up shall not exceed 5 A peak for a period of 10 ms. In addition, the FOMAU shall be capable of powering-up from 0.5 A current limited sources.

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It is permissible as an option to provide a separate power source for the FOMAU. If a separate power source is implemented, provision will be made to assure that power shall under no circumstances be sourced on pin 13 (Circuit VP) of the AUI.

The FOMAU shall be labeled externally to identify the maximum value of power supply current required by the device when the AUI mechanical connection is implemented.

The FOMAU shall not introduce into the FOMAU's transmit optical fiber or onto the DI or CI circuits of the AUI any extraneous signal on routine power-up or power-down under normal operating conditions.

The FOMAU shall be fully functional no later than 0.5 s after power is applied to it.

9.9.3.3 Reliability

The FOMAU shall be designed to provide a MTBF of at least 200 000 hours of operation without causing a communication failure amongst DTEs attached to the network. The FOMAU electronics shall be designed to minimize the probability of component failures within the FOMAU that prevent communication amongst other MAUs on the 10BASE5 and 10BASE2 segments. Connectors and other passive means of connection shall be designed to minimize the probability of total network failure.

9.9.3.4 FOMAU/Repeater unit electrical characteristics

The electrical characteristics of the driver and receiver components connected to the AUI cable shall be identical to those specified in Clause 7.

9.9.3.5 FOMAU/Repeater unit mechanical connection

The FOMAU, if it implements the AUI mechanical connection, shall be provided with a 15-pin male connector, as specified in the AUI specification of Clause 7.

9.9.4 FOMAU/Optical medium interface

9.9.4.1 Transmit optical parameters

9.9.4.1.1 Wavelength

The center wavelength of the optical source emission shall be between 790 nm and 860 nm. See 15.2.1.1.

9.9.4.1.2 Spectral width

The spectral width of the optical source shall be less than 75 nm full width half maximum (FWHM).

9.9.4.1.3 Optical modulation

The optical modulation during packet transmission shall be on-off keying of the optical source power. The minimum extinction ratio shall be 13 dB.

9.9.4.1.4 Optical idle signal

During the idle state of the DO circuit, the Transmit function shall input into the FOMAU's transmit optical fiber an optical idle signal. This signal shall consist of a periodic pulse waveform of frequency 1 MHz +25% –15% with a duty cycle ratio between 45/55 and 55/45.

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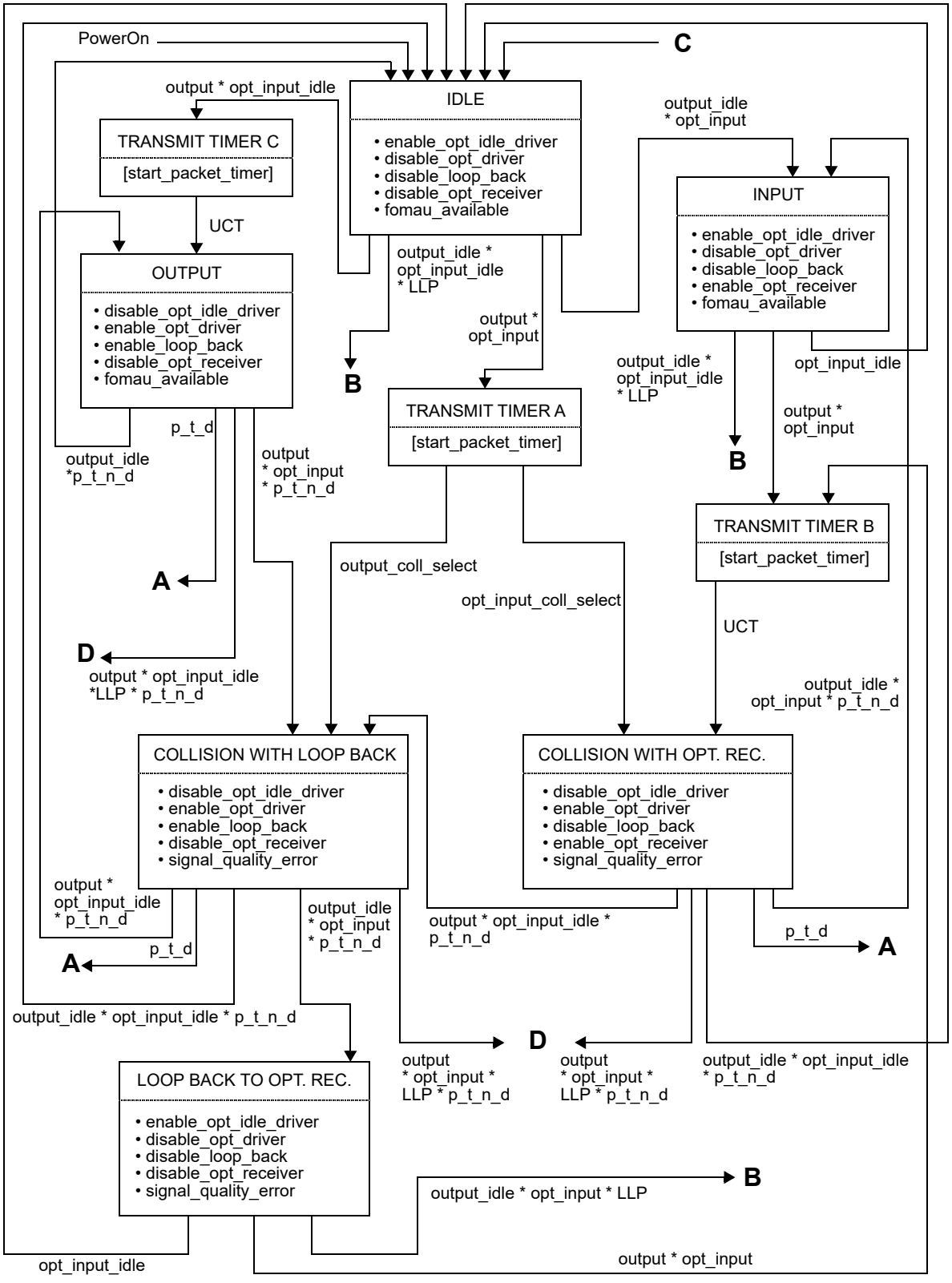

Figure 9–8—FOMAU Transmit, Receive, and Collision functions state diagram

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9.9.4.1.5 Transmit optical logic polarity

The higher optical power level transmitted into the FOMAU's transmit optical fiber shall correspond to the low (LO) logic state (see 7.4.2.1) of the AUI DO circuit.

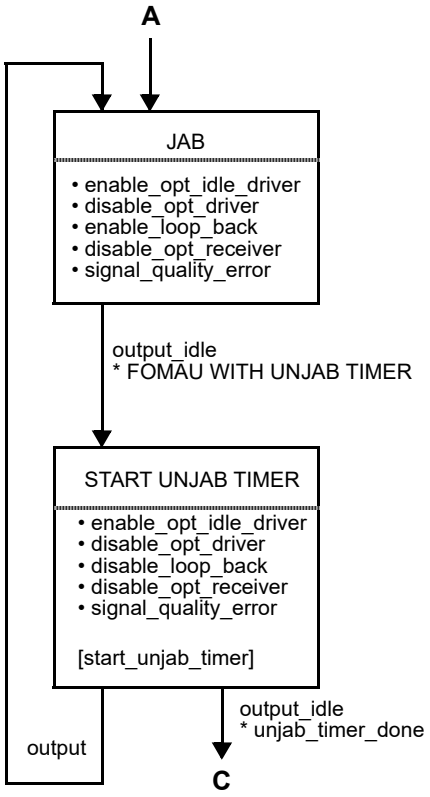

**Figure 9–9—
FOMAU Jabber function
state diagram**

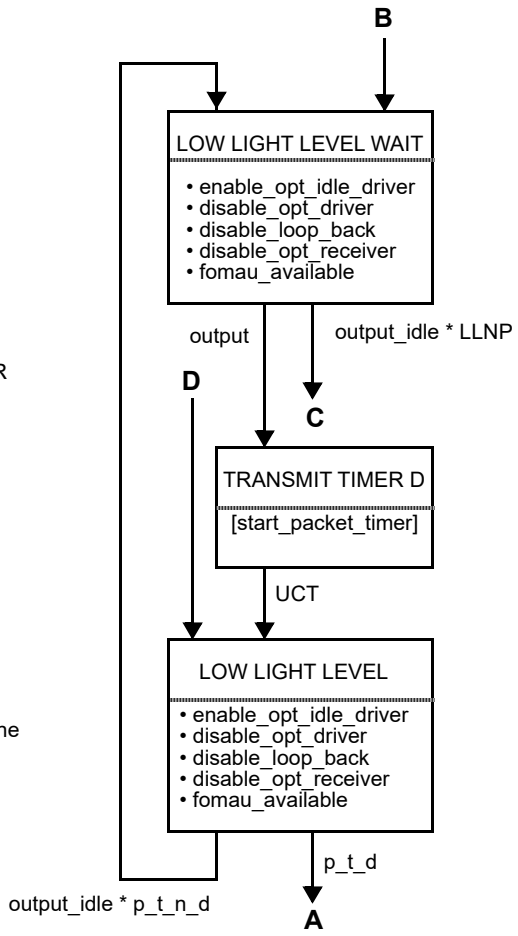

**Figure 9–10—
Low Light Level Detection
function state diagram**

9.9.4.1.6 Optical rise and fall times

The optical rise and fall times of the FOMAU shall be no more than 10 ns from the 10% to the 90% levels. There shall be no more than 3 ns difference between the rise and fall times.

9.9.4.1.7 Transmit optical pulse edge jitter

The additional edge jitter introduced by the FOMAU from the input of the DO circuit receiver to the output of the electro-optic source shall be no more than 2 ns. The jitter measured at the input of the DO circuit receiver shall be measured at the zero crossing points, as determined from the previous 16 or more transitions in any valid bit stream. The jitter measured at the output of the electro-optic source shall be measured at the power level median of the optical waveform's upper and lower power levels, as determined from the previous 16 or more transitions in any valid optical bit stream.

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9.9.4.1.8 Peak coupled optical power

At the beginning of the FOMAU's lifetime, the peak optical power coupled into the FOMAU's transmit optical fiber, when terminated with an optical connector as specified in 9.9.5.2, shall be –12 dBm ± 2 dB, when measured with a graded index optical fiber of nominal dimension of 62.5 μm core diameter and 0.275 nominal numerical aperture. The actual optical power, which will be coupled into other fiber sizes listed in 9.9.5.1, may differ from the above value. The peak optical power shall be measured in the steady state, and the measurement shall be independent of optical pulse ringing effects. Peak optical overshoot shall not exceed 10%.

NOTE 1—The source is allocated an aging margin of 3 dB over its operating lifetime. Thus, with respect to an optical fiber of nominal dimension of 62.5 μm core diameter and 0.275 nominal numerical aperture, the minimum launch peak power at the end of life is –17 dBm and the maximum initial launch peak power is –10 dBm. The variation in the peak coupled optical power into any of the optical fibers specified in 9.9.5.1 is ±1 dB with respect to the above-mentioned nominal optical fiber. Hence, with respect to any of the optical fibers specified in 9.9.5.1, the minimum possible launch peak power at the end of life is –18 dBm and the maximum possible initial launch peak power is –9 dBm. The start of life minimum possible launch peak power is then –15 dBm.

NOTE 2—The transmit optical power range specified above is the power coupled into the core of the optical fiber. Typical current fibers require 1 m to 5 m to remove optical power from the cladding. For links under 5 m in length, it may be necessary to use techniques such as attenuators or mode-stripping filters to attenuate optical power coupled into the cladding in order to meet the requirements of 9.9.4.2.1.

9.9.4.2 Receive optical parameters

9.9.4.2.1 Receive peak optical power range

The BER shall be $< 10^{-10}$ for peak optical powers at the output of the FOMAU's receive optical fiber between –27 dBm and –9 dBm.

9.9.4.2.2 Receive optical pulse edge jitter

The additional edge jitter introduced by the FOMAU from the input of the opto-electric detector to the output of the DI circuit driver shall be no more than 4 ns. The jitter measured at the input of the opto-electric receiver shall be measured at the power level median of the optical waveform's upper and lower power levels as determined from the previous 16 or more transitions in any valid optical bit stream. The jitter measured at the output of the DI circuit driver shall be measured at the zero crossing points as determined from the previous 16 or more transitions in any valid bit stream. This requirement shall apply when the optical receive peak power level is in the range –27 to –9 dBm.

9.9.4.2.3 Receive optical logic polarity

The low (LO) logic state (see 7.4.2.1) on the DI circuit shall correspond to the presence of the higher optical power level at the output of the FOMAU's receive optical fiber.

9.9.5 Characteristics of the optical fiber cable link segment

The optical fiber cable link segment is a length of optical fiber cable (IEC 60794-1: 1993 and IEC 60794-2: 1989) containing two optical fibers, as specified in 9.9.5.1, and comprising one or more optical fiber cable sections and their means of interconnection. Each optical fiber is terminated at each end in the optical connector plug specified in 9.9.5.2. The two optical fibers correspond to the FOMAU's transmit and receive optical fibers.

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9.9.5.1 Optical fiber medium

The FOMAU can operate with a variety of optical fiber sizes, e.g., 50/125 μm, 62.5/125 μm, 85/125 μm, 100/140 μm.

Interoperability of FOMAUs that originate from different manufacturers, using any of these fiber sizes, is assured provided that the received peak optical power is between –27 dBm and –9 dBm and the optical fiber cable link segment bandwidth is greater than or equal to 150 MHz.

In order to satisfy the above attenuation and bandwidth criteria for all allowable FOIRL lengths, and assuming up to 4 dB of connection losses within the optical fiber cable link segment, it is recommended that the cabled optical fiber have an attenuation ≤ 4 dB/km and a bandwidth of ≥ 150 MHz referred to 1 km at a wavelength of 850 nm.

The total incremental optical pulse edge jitter introduced by the optical fiber cable link segment shall be less than 1 ns when driven by an optical transmitter as specified in 9.9.4.1. The pulse delay introduced by the optical fiber cable shall not exceed 50 bit times for a 1 km length.

In the specific case of 62.5/125 μm fiber, to ensure interoperability of FOMAUs that originate from different manufacturers:

a) The two cabled optical fibers contained in the optical fiber cable link segment shall satisfy the optical fiber parameters specified in IEC 60793-2: 1992 type A1b (62.5/125 μm), and
b) The optical fiber cable link segment shall have an attenuation less than or equal to 8 dB and a bandwidth greater than or equal to 150 MHz.

NOTE—For newer fiber installations, it is recommended that the requirements of 15.3 be used.

9.9.5.2 Optical medium connector plug and socket

The two optical fibers contained in the optical fiber cable link segment shall be terminated at each end in an optical connector plug as specified in IEC 60874-1: 1993 and 60874-2: 1993.

The corresponding mating connector socket shall conform with the specifications given in IEC 60874-1: 1993 and 60874-2: 1993. This document specifies the mechanical mating face dimensions to ensure mechanical intermateability without physical damage, of all F-SMA connectors covered by the document. In addition, the optical insertion loss when interconnecting two optical connector plugs shall not exceed 2.5 dB (measured using a socket adaptor conforming to the mechanical specifications given in IEC 60874-1: 1993 and 60874-2: 1993 and also using two identical fibers, as specified in 9.9.5.1, assuming uniform mode distribution launch conditions).

9.9.6 System requirements

9.9.6.1 Optical transmission system considerations

Subclause 9.9.4.2.1 specifies that the BER shall be $<10^{-10}$ for peak optical powers at the output of the FOMAU's receive optical fiber between –27 dBm and –9 dBm. The value of –9 dBm corresponds to the maximum allowable peak optical power that can be coupled into the worst-case optical fiber specified in 9.9.5.1 at the beginning of the FOMAU's lifetime (see 9.9.4.1.8), and assumes zero optical loss between the optical source output and the optical detector input.

The value of –27 dBm is calculated by subtracting the FOIRL flux budget from the minimum allowable peak optical power that can be coupled into the FOMAU's transmit optical fiber at the beginning of the FOMAU's lifetime (see 9.9.4.1.8). The flux budget is the maximum loss allowed within the FOIRL to guar-

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antee a BER < 10^{-10} assuming worst-case link components. A portion of the flux budget has been allocated as a design margin to allow for degradation and tolerance effects in the optical source. This is noted in the table below as the optical source lifetime degradation. The remaining flux budget of 9 dB assumes a system margin allowance for the optical fiber cable link segment over its lifetime, and may be allocated to the optical fiber cable link segment loss at the discretion of the network planner/installer. The following summarizes the allocated optical flux budgets for the example graded index optical fiber of worst-case dimensions 62.5 μm – 3 μm (i.e., 59.5 μm) core diameter and 0.275 – 0.015 (i.e., 0.260) numerical aperture:

Start of life minimum peak coupled optical power (9.9.4.1.8) : –15 dBm

Optical source lifetime degradation : 3 dB

Maximum optical fiber cable link segment loss including system margin allowance : 9 dB

Resultant required receive peak optical power : –27 dBm

9.9.6.2 Timing considerations

Table 9–4 summarizes the maximum allowable timing budget contributions to the system timing budget for the FOIRL. The last bit in to last bit out delay shall equal the Steady-State Propagation Delay.

Table 9–4—Maximum allowable timing budget contributions to the FOIRL system timing budget

Symbol	Function	Bit loss (bit times)	Invalid bits (bit times)	Steady-state propagation delay (bit times)	Start-up delay (bit times)
I1	OPTICAL DATA IN ASSERT→INPUT	2.0	1.0	0.5	3.5
I2	OUTPUT→OPTICAL DATA OUT ASSERT	2.0	1.0	0.5	3.5
LOOP BACK	DO CIRCUIT ASSERT →DI CIRCUIT ASSERT	5.0	1.0	1.0	7.0
I3	OPTICAL COLLISION →SQE ASSERT	—	—	—	3.5
I4	COLLISION DE-ASSERT →SQE DE-ASSERT	—	—	—	7.0[a]
A1	AUI propagation	—	—	2.57	2.57
F1	Optical fiber propagation per kilometer	—	—	50	50

[a]Minimum start-up delay for I4 is 4.5 bit times.

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9.9.7 Environmental specifications

9.9.7.1 Safety requirements

9.9.7.1.1 Electrical safety

A major application for the vendor-independent FOIRL is interconnecting electrically conductive cable segments located within different buildings. The level of isolation provided by the optical fiber cable link segment shall be consistent with this application and provide adequate personnel and equipment safety from earth faults and lightning strike hazards.

9.9.7.1.2 Optical source safety

The recommendations of IEC 60825: 1993, if applicable, shall be adhered to in determining the optical source safety and user warning requirements.

9.9.7.2 Electromagnetic environment

9.9.7.2.1 Susceptibility levels

Sources of interference from the environment include electromagnetic fields, electrostatic discharge, and transient voltages between earth connections. Several sources of interference contribute to voltage between the optical fiber cable link segment (either a metallic strength member in the cable, a metallic optical connector plug, or the outermost conducting element of the FOMAU for the case of no metallic strength member) and the earth connection of a DTE.

For information on limits and methods of measurements of radio interference characteristics of information technology equipment, see 1.3 in CISPR 22: 1993.

The physical channel hardware shall meet its specifications when operating in both of the following conditions:

a) Ambient plane wave field of 2 V/m from 10 kHz through 30 MHz and 5 V/m from 30 MHz through 1 GHz.

NOTE—These are the levels typically found 1 km from radio broadcast stations.

b) Interference source voltage of 15.8 V peak sine wave of frequency 10 MHz in series with a 50 Ω source resistance applied between the optical fiber cable link segment (either a metallic strength member in the cable, a metallic optical connector plug, or the outermost conducting element of the FOMAU for the case of no metallic strength member) and the earth connection of a DTE.

NOTE—The optical fiber link segment is capable of withstanding higher levels of electromagnetic interference. The above specifications are the minimum requirements for the environment in which the FOMAU is required to operate.

9.9.7.2.2 Emission levels

The FOMAU and optical fiber cable link segment shall comply with CISPR 22: 1993.

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9.9.7.3 Temperature and humidity

The FOMAU and associated connector/cable systems are expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling such as shock and vibration. Specific requirements and values for these parameters are beyond the scope of this standard. Manufacturers should indicate in the literature associated with the FOMAU (and on the FOMAU if possible) the operating environment specifications to facilitate selection, installation, and maintenance of these components. It is further recommended that such specifications be stated in standard terms, as specified in IEC 60068, IEC 60793-1: 1992, IEC 60794-1: 1993, and IEC 60874-1: 1993.

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10. Medium attachment unit and baseband medium specifications, type 10BASE2

NOTE—This MAU is not recommended for new installations. Since September 2011, maintenance changes are no longer being considered for this clause.

10.1 Scope

10.1.1 Overview

This standard defines the functional, electrical, and mechanical characteristics of the Medium Attachment Unit (MAU) and one specific medium for use with LANs. The relationship of this specification to the OSI Reference Model is shown in Figure 10–1.

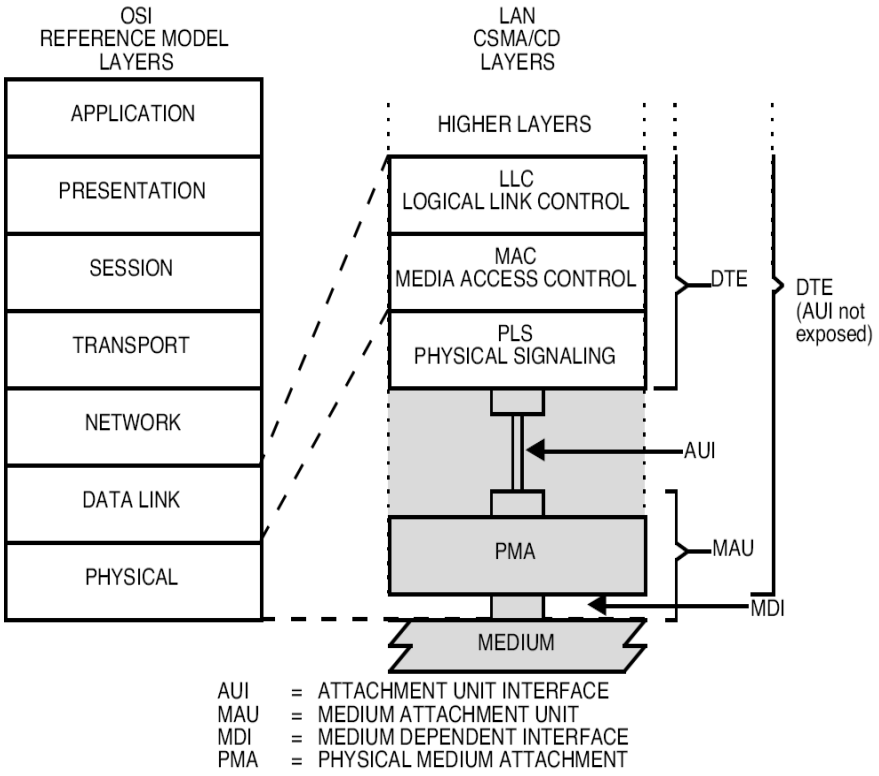

Figure 10–1—Physical Layer partitioning, relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the LAN medium. This standard defines a means of incorporating the MAU function within the DTE and bringing the trunk coaxial cable directly to the DTE. Interconnection of DTE units is easily achieved by the use of industry standard coaxial cables and BNC connectors.

This MAU and medium specification is aimed primarily at applications where there are a relatively small number of devices located in a work area. Installation and reconfiguration simplicity is achieved by the type of cable and connectors used. An inexpensive implementation is achieved by eliminating the MAU and Attachment Unit Interface (AUI) as separate components and using widely available interconnection components.

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10.1.1.1 Medium attachment unit (normally contained within the data terminal equipment [DTE])

The MAU has the following general characteristics:

a) Enables coupling the PLS to the explicit baseband coaxial transmission system defined in this clause of the standard.
b) Supports message traffic at a data rate of 10 megabits per second (Mb/s).
c) Provides for driving up to 185 m coaxial trunk cable segment without a repeater.
d) Permits the DTE to test the MAU and the medium itself.
e) Supports system configurations using the CSMA/CD access mechanism defined in IEEE 802.3.
f) Supports a bus topology interconnection means.
g) Supports low-cost capability by incorporating the MAU function within the physical bounds of the DTE, thereby eliminating the need for a separate AU connector and cable but containing the remaining AU interface functionality.

10.1.1.2 Repeater unit

The Repeater Unit is used to extend the physical system topology and provides for coupling two or more coaxial trunk cable segments. Multiple Repeater Units are permitted within a single system to provide the maximum trunk cable connection path specified in 10.7. The repeater is not a DTE and therefore has slightly different attachment requirements.

10.1.2 Definitions

See 1.4.

10.1.3 Application perspective: MAU and medium objectives

This subclause states the broad objectives and assumptions underlying the specifications defined throughout Clause 10 of the standard.

10.1.3.1 Object

a) Provide the physical means for communication between local network Data Link entities.

   NOTE—This specification covers a portion of the Physical Layer as defined in the OSI Reference Model and, in addition, the physical medium itself, which is beyond the scope of the OSI Reference Model.

b) Define a physical interface that can be implemented independently among different manufacturers of hardware and achieves the intended level of compatibility when interconnected in a common local network.
c) Provide a communication channel capable of high bandwidth and low bit error ratio performance. The resultant mean bit error ratio, at the Physical Layer service interface, should be less than one part in 10^7 (on the order of one part in 10^8 at the link level).
d) Provide for ease of installation and service.
e) Provide for high network availability (ability of a station to gain access to the medium and enable the Data Link connection in a timely fashion).
f) Enable low-cost implementations.

NOTE—The figures and numerous textual references throughout this clause refer to terminology associated with the AUI (that is, DO, DI, CI). Since the normal embodiment of the type 10BASE2 configuration does not require an AUI, actual existence of the DO, DI, CI circuit may not be required. Use of this terminology, however, is retained throughout Clause 10 for purposes of clarity and consistency.

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10.1.3.2 Compatibility considerations

All implementations of this baseband coaxial system shall be compatible at the Medium Dependent Interface (MDI).

This standard provides one explicit trunk cable medium specification for the interconnection of all MAU devices. The medium itself, and the functional capability of the MAU, are defined to provide the highest possible level of compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the MAU in an application-dependent manner provided the MDI specifications are satisfied.

10.1.3.3 Relationship to PLS and AUI

This clause defines the Primary Physical Layer for the LAN, a layer composed of both the physical medium and the rudimentary circuitry necessary to couple a station's message path directly to/from the medium. The complete Logical Physical Layer of the LAN resides within the DTE. Therefore, a close relationship exists between this subclause and Clause 7. This subclause specifies the physical medium parameters, the PMA logical functions residing in the MAU, and references the signal circuits associated with the AUI as defined in Clause 7.

The design of a MAU component requires the use of both this clause and parts of the PLS and AUI specifications contained in Clause 7.

10.1.3.4 Mode of operation

The MAU functions as a direct connection between the baseband medium and the DTE. Data from the DTE is output to the coaxial trunk medium and all data on the coaxial trunk medium is input to the DTE.

10.2 References

References to such local or national standards that may be useful resource material for the reader are identified and located in Annex A.

10.3 MAU functional specifications

The MAU component provides the means by which signals on the three AUI signal circuits to/from the DTE and their associated interlayer messages are coupled to the single coaxial cable baseband signal line. To achieve this basic objective, the MAU component contains the following functional capabilities to handle message flow between the DTE and the baseband medium:

a) *Transmit function.* The ability to transmit serial data bit streams on the baseband medium from the local DTE entity to one or more remote DTE entities on the same network.
b) *Receive function.* The ability to receive serial data bit streams over the baseband medium.
c) *Collision Presence function.* The ability to detect the presence of two or more stations' concurrent transmissions.
d) *Jabber function.* The ability to automatically interrupt the Transmit function and inhibit an abnormally long output data stream.

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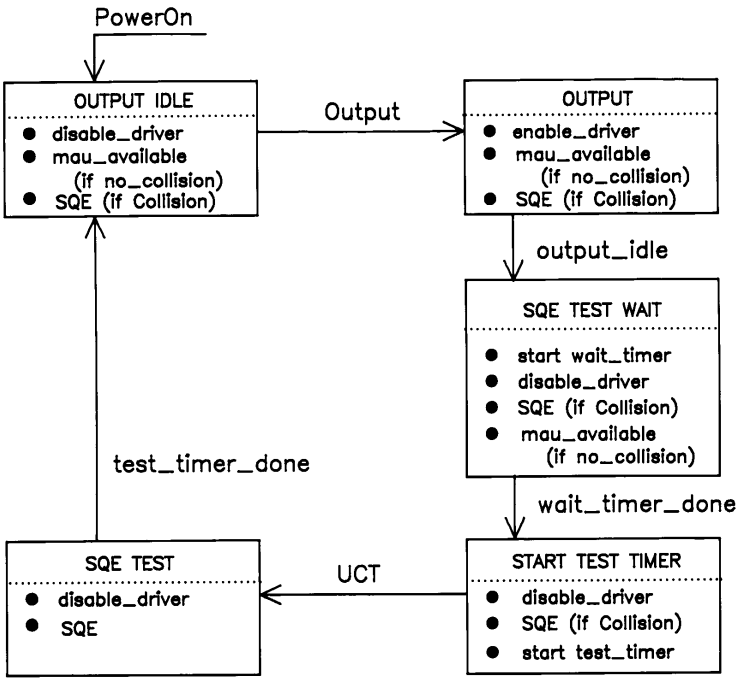
10.3.1 MAU Physical Layer functional requirements

10.3.1.1 Transmit function requirements

At the start of a frame transmission on the coaxial cable, no more than 2 bits (2 full bit cells) of information may be received from the DO circuit and not transmitted onto the coaxial medium. In addition, it is permissible for the first bit sent to contain invalid data or timing; however, all successive bits of the frame shall be reproduced with no more than the specified amount of jitter. The 4th bit cell shall be carried from the DO signal line and transmitted onto the coaxial trunk cable medium with the correct timing and signal levels. The steady-state propagation delay between the DO circuit receiver input and the coaxial cable output shall not exceed 1/2 bit cell. There shall be no logical signal inversions between the branch cable DO circuit and the coaxial trunk cable (for example, a "high" logic level input to the MAU shall result in the less negative current flow value on the trunk coaxial medium). A positive signal on the A signal lead of the DO circuit shall result in a more positive voltage level on the trunk coaxial medium. It is assumed that the AUI shall provide adequate protection against noise. It is recommended that the designer provide an implementation in which a minimum threshold signal is required to establish a transmit bit stream.

The Transmit function shall output a signal on the trunk coaxial medium whose levels and waveform comply with 10.4.1.3.

In addition, when the DO circuit has gone idle after a frame is output, the MAU shall then activate the Collision Presence Function as close to the trunk coaxial cable as possible without introducing an extraneous signal on the trunk coaxial medium. The MAU shall initiate the Collision Presence state within 0.6 μs to 1.6 μs after the Output Idle signal (Wait_Timer_Done in Figure 10–2) and shall maintain an active Collision Presence state for a time equivalent to 10 bit cells ± 5 bit cells.



(UCT = unconditional transition)
(Wait_Timer_Done is specified in 10.3.1.1)

Figure 10–2—MAU Interface function

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10.3.1.2 Receive function requirements

The signal from the coaxial trunk cable shall be AC-coupled before reaching the receive DI circuit. The Receive Function shall output a signal onto the DI circuit that complies with the specification for drivers in MAUs (7.5).

At the start of a frame reception from the coaxial cable, no more than 5 bits (5 full bit cells) of information may be received from the coaxial cable and not transmitted onto the receive DI circuit. In addition, it is permissible for the first bit sent over the receive circuit to contain invalid data or timing; however, all successive bits of the frame shall reproduce the incoming signal with no more than the amount of jitter specified below. This implies that the 7th bit cell presents valid data to the PLS. The steady-state propagation delay between the coaxial cable and the receive DI circuit output shall not exceed 1/2 bit cell. There are no logical signal inversions between the coaxial (trunk) cable and the MAU receive circuit.

A MAU meeting this specification shall exhibit edge jitter into the DI pair when terminated in the appropriate test load specified in 7.4.1.1, of no more than 7.0 ns in either direction when it is installed on the distant end of all lengths up to 185 m of the cable specified in 10.5.1.1 through 10.5.2.1.5 terminated at both ends with terminators meeting the impedance requirements of 10.6.2 and driven at one end with pseudorandom Manchester encoded binary data from a data generator that exhibits no more than 1.0 ns of edge jitter in either direction on half bit cells of exactly 1/2 BT and whose output meets the specifications of 10.4.1.3 except that the rise time of the signal shall be 30 ns + 0, – 2 ns. The combination of coaxial cable and MAU receiver introduce no more than 6 ns of edge jitter into the system.

The local Transmit and Receive functions shall operate simultaneously while connected to the medium.

10.3.1.3 Collision Presence function requirements

The signal presented to the CI circuit in the absence of a collision shall be the IDL signal.

The signal presented to the CI circuit during the presence of a collision shall be the CS0 signal encoded as specified in 7.3.1.2. Under no conditions shall the Collision Presence function generate an output when only one MAU is transmitting. Table 10–1 summarizes the allowable conditions under which collisions shall be detected.

a) Collision Assertion
    1) In the case where the MAU has been transmitting for at least 20 bit times, the CS0 signal shall be presented to the CI circuit no more than 17 bit times after the arrival at the MAU on the coaxial cable of a transmission from another MAU. Arrival at the MAU shall be considered to be the time when the transmission of the other MAU causes the dc level on the coaxial cable to become more negative.
    2) In all other cases where the MAU is transmitting, the CS0 signal shall be presented to the CI circuit no more than 29 bit times after the later of start of transmission by the MAU and the arrival of a transmission from another MAU.
b) Collision De-assertion
    1) In the case where a collision has occurred between the MAU and one other MAU, the IDL signal shall be presented to the CI circuit no more than 17 bit times after either the end of transmission by the MAU or the arrival of the end of transmission from the other MAU, whichever occurs earlier. The arrival of the end of transmission from the other MAU shall be the time when the cessation of transmission causes the dc level on the coaxial cable to become less negative.
    2) In the case where a collision has occurred between more than two MAUs, the IDL signal shall be presented to the CI circuit no more than 29 bit times after the arrival of the end of transmission from all but one MAU.

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These timing conditions shall be met for all data bit patterns and combinations of MDI, MAU transmit levels, and MAU locations on the segment.

The Collision Presence function may, in some implementations, be able to sense an abnormal (for example, open) medium.

Table 10–1—Generation of collision presence signal

MAU	Numbers of transmitters		
	<2	=2	>2
Transmitting	N	Y	Y
Not transmitting	N	Y	Y
Y = shall generate SQE message N = shall not generate SQE message			

10.3.1.4 Jabber functional requirements

The MAU shall contain the capability as defined in Figure 10–3 to interrupt a transmission from a DO circuit that exceeds a time duration determined by the MAU. This time duration shall not be less than 20 ms nor more than 150 ms. If the frame being transmitted continues longer than the specified time duration, the MAU shall inhibit transmission and assume its not-transmitting state on the coaxial cable.

When the Transmit function has been positively disabled, the MAU shall then activate the Collision Presence function without introducing an extraneous signal on the trunk coaxial medium. A MAU may reset the Jabber and Collision Presence functions on power reset once the error condition has been cleared. Alternately, a MAU may reset these functions automatically after a period of 0.5 s ± 50%.

10.3.2 MAU interface messages

10.3.2.1 DTE to MAU messages

The following messages can be sent by the DTE Physical Layer (PLS Sublayer) Entities to the MAU Entities:

Message	Circuit	Signal	Meaning
output	DO	CD1, CD0	Output information
output_IDL	DO	IDL	No data to be output

10.3.2.2 MAU to DTE messages

The following messages can be sent by the MAU Physical Layer entities to the DTE Physical Layer entities:

Message	Circuit	Signal	Meaning
input	DI	CD1, CD0[a]	Input information
input_idle	DI	IDL	No information to be input
mau_available	CI	IDL	MAU is available for output
SQE	CI	CS0	Error detected by MAU

[a]It is assumed that no retiming of these clocked data signals takes place within the MAU.

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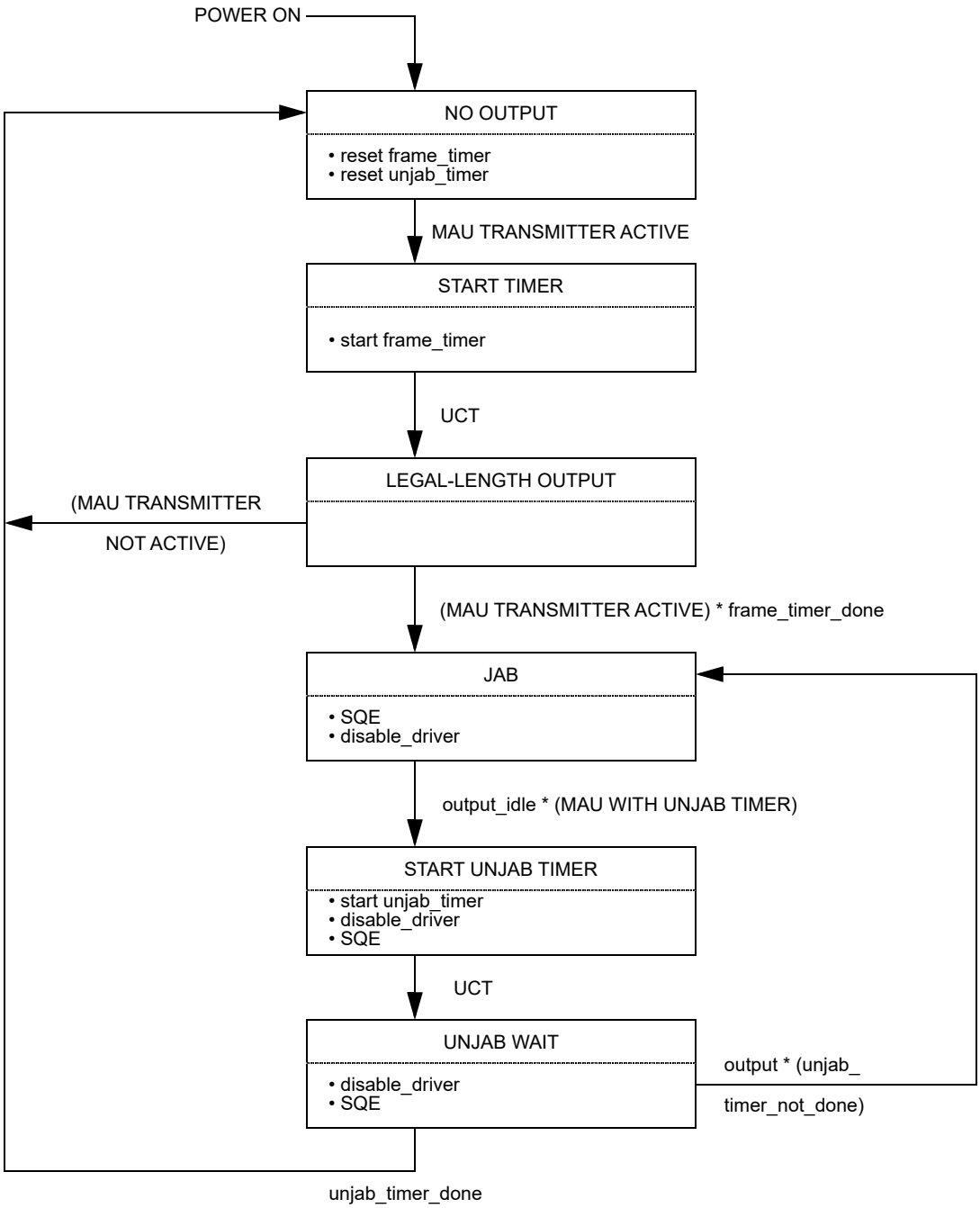

(Figure 10–3 outputs override those in Figure 10–2.
Optional states: START UNJAB TIMER, UNJAB WAIT.)

Figure 10–3—Jabber function state diagram

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10.3.2.2.1 *input* message

The MAU sends an input message to the DTE Physical Layer when the MAU has a bit of data to send to the DTE. The physical realization of the input message is a CD0 or CD1 sent by the MAU to the DTE on the Data In circuit. The MAU sends CD0 if the input bit is a zero or CD1 if the input bit is a one. No retiming of the CD1 or CD0 signals takes place within the MAU.

10.3.2.2.2 *input_idle* message

The MAU sends an *input_idle* message to the DTE Physical Layer when the MAU does not have data to send to the DTE. The physical realization of the *input_idle* message is the IDL signal sent by the MAU to the DTE on the Data In circuit.

10.3.2.2.3 *mau_available* message

The MAU sends the *mau_available* message to the DTE Physical Layer when the MAU is available for output. The *mau_available* message is always sent by a MAU that is always prepared to output data unless the SQE message should be sent instead. Such a MAU does not require *mau_request* to prepare itself for data output. The physical realization of the *mau_available* message is an IDL signal sent by the MAU to the DTE on the Control In circuit.

10.3.2.2.4 *signal_quality_error* (SQE) message

The SQE message shall be implemented in the following fashion:

a) The SQE message shall not be sent by the MAU if no or only one MAU is transmitting on the trunk coaxial medium.
b) If two or more remote MAUs are transmitting on the trunk coaxial medium, but the MAU connected to the local DTE is not transmitting, then the local MAU shall send the SQE message.
c) When the local MAU is transmitting on the trunk coaxial medium, all occurrences of one or more additional MAUs transmitting shall cause the SQE to be sent by the local MAU to its DTE.
d) When the MAU has completed each output frame it shall perform an SQE test sequence. Note that MAUs associated with repeaters shall not generate the SQE test sequence.
e) When the MAU has inhibited the Transmit function, it shall send the SQE message in accordance with the Jabber function requirements of 10.3.1.4 and Figure 10–3.

The physical realization of the SQE message is the CS0 signal sent by the MAU to the DTE Physical Layers on the Control In circuit.

NOTE—The MAU is required to assert the SQE at the appropriate times whenever the MAU is powered and not just when the DTE Physical Layer is providing data output.

10.3.3 MAU state diagrams

The state diagrams, Figure 10–2 and Figure 10–3, depict the full set of allowed MAU state functions relative to the control circuits of the DTE-MAU interface for MAUs without conditioning requirements. Messages used in these state diagrams are explained as follows:

enable_driver. Activates the path employed during normal operation to cause the MAU transmitter to impress data onto the trunk coaxial medium.

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disable_driver. Deactivates the path employed during normal operation to cause the MAU transmitter to impress data onto the trunk coaxial medium.

no_collision. Signifies that the condition of multiple transmitters simultaneously active on the trunk coaxial medium does not exist.

collision. Signifies that the condition of multiple transmitters simultaneously active on the trunk coaxial medium does exist.

frame_timer. Measures the time the MAU transmits on the trunk coaxial cable.

test_timer. Measures the length of the SQE Test.

unjab_timer. Measures the amount of time the MAU has been in Jab mode.

wait_timer. Measures the time between output idle and the start of the SQE Test.

10.4 MAU–medium electrical characteristics

10.4.1 MAU-to-coaxial cable interface

The following subclauses describe the interface between the MAU and the coaxial cable. Negative current is defined as current into the MAU (out of the center conductor of the cable).

10.4.1.1 Input impedance

The shunt capacitance presented to the coaxial cable by the MAU circuitry (not including the means of attachment to the coaxial cable) is recommended to be not greater than 6 pF. The magnitude of the reflection from a MAU plus the cable connection specified in 10.6.3 shall not be more than that produced by an 8 pF capacitance when measured by both a 25 ns rise time and 25 ns fall time waveform. The resistance presented to the coaxial cable shall be greater than 100 kΩ.

These conditions shall be met in both the power-off and power-on, not-transmitting states.

10.4.1.2 Bias current

The MAU has to draw (from the cable) between +2 μA and –25 μA in the power-off and the power-on, not-transmitting states.

10.4.1.3 Coaxial cable signaling levels

The signal on the coaxial cable due to a single MAU as measured at the MAU's transmitter output is composed of an ac component and an offset component. Expressed in terms of current immediately adjacent to the MAU connection (just prior to splitting the current flow in each direction), the signal has an offset component (average dc current including the effects of timing distortion) of from –37 mA min to –45 mA max and an ac component from ± 28 mA up to the offset value.

The current drive limit shall be met even in the presence of one other MAU transmitter. The MAU shall be capable of generating at least 2.2 V of average dc level on the coaxial cable in the presence of two or more other MAUs transmitting concurrently. The MAU shall, in addition, sink no more than ± 250 μA when the voltage on the center conductor of the cable drops to –10 V when the MAU is transmitting.

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The actual current measured at a given point on the cable is a function of the transmitted current and the cable loss to the point of measurement. Negative current is defined as current out of the center conductor of the cable (into the MAU). The 10 – 90% rise/fall times shall be 25 ns ± 5 ns at 10 Mb/s. The rise and fall times have to match within 2 ns. Figure 10–4 shows typical waveforms present on the cable. Harmonic content generated from the 10 MHz fundamental periodic input shall meet the following requirements:

Second and Third Harmonics: At least 20 dB below fundamental
Fourth and Fifth Harmonics: At least 30 dB below fundamental
Sixth and Seventh Harmonics: At least 40 dB below fundamental
All Higher Harmonics: At least 50 dB below fundamental

NOTE—Even harmonics are typically much lower.

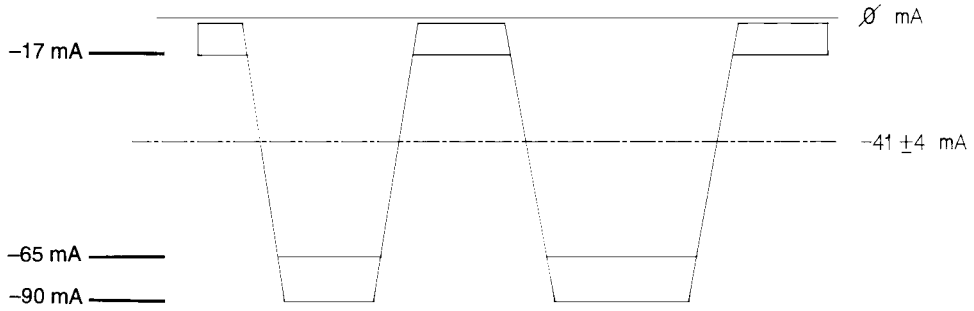
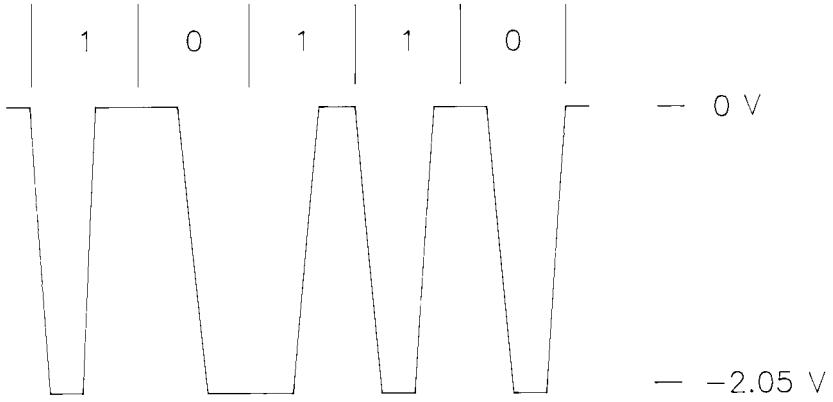


Figure 10–4—Driver current signal levels

The above specifications concerning harmonics cannot be satisfied by a square wave with a single-pole filter, nor can they be satisfied by an output waveform generator employing linear ramps without additional waveshaping. The signals, as generated from the encoder within PLS, shall appear on the coaxial cable without any inversions (see Figure 10–5).



NOTE: (1) Voltages given are nominal, for a single transmitter.
(2) Rise time is 25 ns nominal at 10 Mb/s rate.
(3) Voltages are measured on terminated coaxial cable adjacent to transmitting MAU.
(4) Manchester coding.

Figure 10–5—Coaxial trunk cable signal waveform

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10.4.1.4 Transmit output levels symmetry

Signals received from the DO circuit have to be transmitted onto the coaxial cable with the characteristics specified in 10.4.1.3. Since the coaxial cable proceeds in two directions from the MAU, the current into the MAU is nominally twice the current measured on the coaxial cable.

The output signal of a MAU meeting this specification shall exhibit edge jitter of no more than 2.5 ns into a 25 Ω ± 1% resistor substituted for the connection to the coaxial cable when the DO circuit into the MAU is driven with pseudo-random Manchester encoded binary data from a data generator that exhibits no more than 0.5 ns of edge jitter on half bit cells of exactly 1/2 BT, whose output meets the specifications of 7.4.1.1 through 7.4.1.5. The above specified component shall not introduce more than 2 ns of edge jitter into the system.

The MAU shall not transmit a negative going edge after cessation of the CD output data stream or before the first valid edge of the next frame.

10.4.1.5 Collision detect thresholds

For receive mode collision detection the MAU shall have its collision detection threshold set in the range –1404 mV and –1581 mV. These limits take account of up to 8% collision detect filter impulse response. If a specific filter implementation has a higher value of impulse response, the lower threshold limit of –1404 mV is required to be replaced by –1300 mV × [1 + impulse response].

Receive mode collision detection indicates that a nontransmitting MAU has the capability to detect collisions when two or more MAUs are transmitting simultaneously.

All MAUs are required to implement receive mode collision detection.

NOTE—The above threshold limits are measured at the coaxial cable center conductor with respect to the shield at the MAU connector. The MAU designer has to take into account circuit offsets, low-frequency noise (for example, 50 Hz, 60 Hz), and 5 MHz ripple at the filter output in determining the actual internal threshold value and its tolerance.

10.4.2 MAU electrical characteristics

10.4.2.1 Electrical isolation

The MAU has to provide isolation between the DTE Physical Layer circuits and the coaxial trunk cable. The isolation impedance measured between any conductor in the DTE Physical Layer circuitry and either the center conductor or shield of the coaxial cable shall be greater than 250 kΩ at 50 Hz, 60 Hz. In addition, the isolation impedance between the DTE ground and the coaxial cable shield shall be less than 15 Ω between 3 MHz and 30 MHz. The isolation means provided shall withstand 500 V ac, rms for one minute.

10.4.2.2 Power consumption

The current drawn by the MAU shall not exceed 0.5 A if powered by the AUI source. The MAU shall be capable of operating from all permissible voltage sources as supplied by the DTE through the resistance of all permissible AUI cables. The MAU shall not disrupt the trunk coaxial medium should the DTE power source fall below the minimum operational level under abnormal MAU load conditions.

The MAU shall be labeled externally to identify the maximum value of current required by the device. This requirement only applies to MAUs that are external to DTEs.

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10.4.2.3 Reliability

The MAU shall be designed to provide an MTBF of at least 100 000 hours of continuous operation without causing communication failure among other stations attached to the local network medium. Component failures within the MAU electronics should not impede the communication among other MAUs on the coaxial cable. Connectors and other passive components comprising the means of connecting the MAU to the coaxial cable shall be designed to minimize the probability of total network failure.

It should be noted that a fault condition that causes a MAU to draw in excess of 2 mA from the coaxial cable may cause communication failure among other stations.

10.4.3 MAU–DTE electrical characteristics

If the AUI is exposed, the electrical characteristics for the driver and receiver components connected between the DTE Physical Layer circuitry and the MAU shall be identical with those as specified in Clause 7 of this standard.

10.5 Characteristics of coaxial cable system

The trunk cable is of constant impedance, coaxial construction. It is terminated at each of the two ends by a terminator (see 10.6.2), and provides the transmission path for connection of MAU devices. Coaxial cable connectors are used to make the connection from the cable to the terminators and between cable sections. The cable has various electrical and mechanical requirements that shall be met to ensure proper operation.

10.5.1 Coaxial cable electrical parameters

The parameters specified in 10.5.1 are met by cable types RG 58 A/U or RG 58 C/U.

10.5.1.1 Characteristic impedance

The average characteristic cable impedance shall be 50 ± 2 Ω. Periodic variations in impedance along a single piece of cable may be up to ±3 Ω sinusoidal, centered around the average value, with a period of less than 2 m.

10.5.1.2 Attenuation

The attenuation of a 185 m cable segment shall not exceed 8.5 dB measured at 10 MHz, or 6.0 dB measured at 5 MHz.

10.5.1.3 Velocity of propagation

The minimum required velocity of propagation is 0.65 c.

10.5.1.4 Edge jitter; entire segment without DTEs attached

A coaxial cable segment meeting this specification shall exhibit edge jitter of no more than 8.0 ns in either direction at the receiving end when 185 m of the cable is terminated at both ends with terminators meeting the impedance requirements of 10.6.2 and is driven at one end with pseudorandom Manchester encoded binary data from a data generator that exhibits no more than 1.0 ns of edge jitter in either direction on half bit cells of exactly $^1/_2$ BT and whose output meets the specifications of 10.4.1.3, except that the rise time of the signal has to be 30 ns + 0, – 2 ns, and no offset component in the output current is required. This test shall be conducted in a noise-free environment. The above specified component is not to introduce more than 7 ns of edge jitter into the system.

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10.5.1.5 Transfer impedance

The coaxial cable medium shall provide sufficient shielding capability to minimize its susceptibility to external noise and also to minimize the generation of interference by the medium and related signals. While the cable construction is not mandated, it is necessary to indicate a measure of performance expected from the cable component. A cable's EMC performance is determined, to a large extent, by the transfer impedance value of the cable.

The transfer impedance of the cable shall not exceed the values shown in Figure 10–6 as a function of frequency.

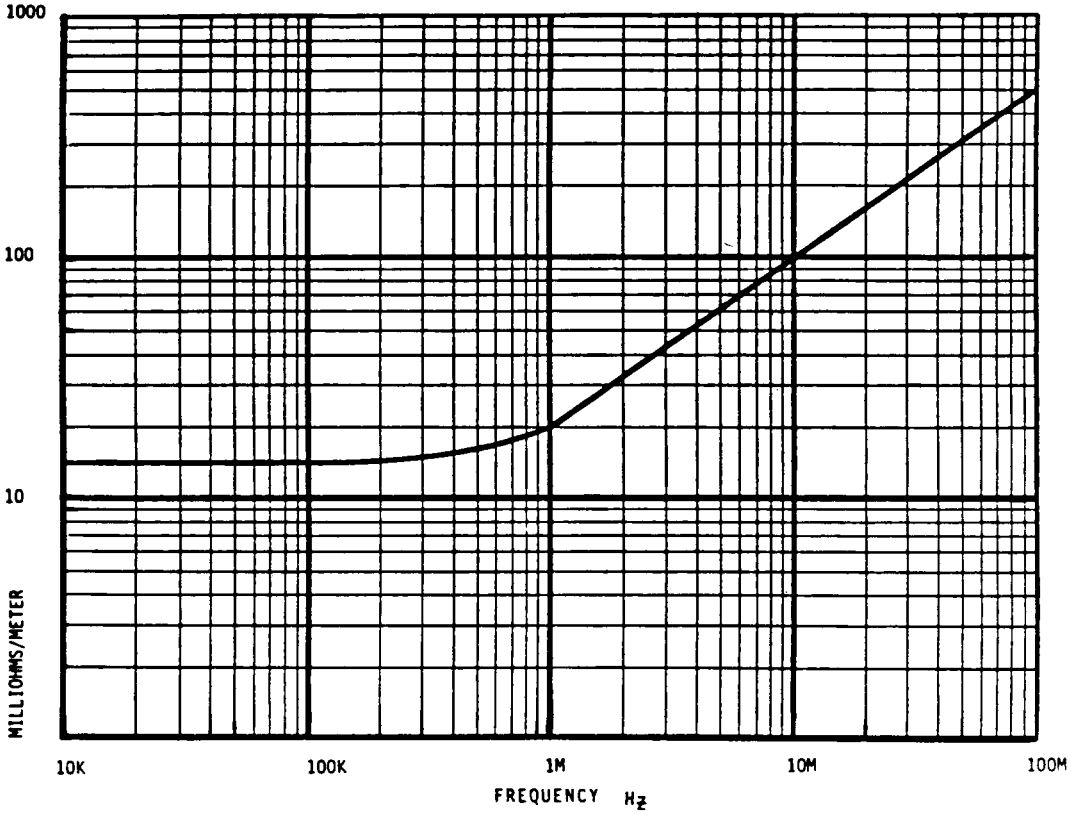

Figure 10–6—Maximum coaxial cable transfer impedance

10.5.1.6 Cable dc loop resistance

The sum of the center conductor resistance plus the shield resistance measured at 20 °C shall not exceed 50 mΩ/m.

10.5.2 Coaxial cable physical parameters

10.5.2.1 Mechanical requirements

The cable used should be suitable for routing in various environments, including but not limited to, dropped ceilings, raised floors, and cable troughs as well as throughout open floor space. The jacket shall provide insulation between the cable sheath and any building structural metal. Also, the cable shall be capable of accepting coaxial cable connectors, described in 10.6. The cable shall conform to the following requirements.

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10.5.2.1.1 General construction

a) The coaxial cable shall consist of a center conductor, dielectric, shield system, and overall insulating jacket.
b) The coaxial cable shall be sufficiently flexible to support a bend radius of 5 cm.

10.5.2.1.2 Center conductor

The center conductor shall be stranded, tinned copper with an overall diameter of 0.89 mm ± 0.05 mm.

10.5.2.1.3 Dielectric material

The dielectric may be of any type, provided that the conditions of 10.5.1.2 and 10.5.1.3 are met; however, a solid dielectric is preferred.

10.5.2.1.4 Shielding system

The shielding system may contain both braid and foil elements sufficient to meet the transfer impedance of 10.5.1.5 and the EMC specifications of 10.8.2.

The inside diameter of the shielding system shall be 2.95 mm ± 0.15 mm.

The shielding system shall be greater than 95% coverage. The use of tinned copper braid is recommended to meet the contact resistance and shielding requirements.

10.5.2.1.5 Overall jacket

a) Any one of several jacket materials shall be used provided the specifications of 10.5.1 and 10.5.2 are met.
b) Either of two jacket dimensions may be used for the two broad classes of materials provided the specification of 10.5.2.1.1 are met:
    1) Polyvinyl chloride (for example, PVC) or equivalent having an OD of 4.9 mm ± 0.3 mm.
    2) Fluoropolymer (for example, FEP, ECTFE) or equivalent having an OD of 4.8 mm ± 0.3 mm.

The cable shall meet applicable flammability and smoke criteria to meet the local and national codes for the installed environment (see 10.8.3).

Different types of cable sections (for example, polyvinyl chloride and fluoropolymer dielectric) may be interconnected, while meeting the sectioning requirements of 10.7.2.1.

10.5.2.2 Jacket marking

It is recommended that the cable jacket be marked with manufacturer and type at a nominal frequency of at least once per meter along the cable.

10.5.3 Total segment dc loop resistance

The sum of the center conductor, connectors, and shield resistance shall not exceed 10 Ω total per segment. Each in-line connector pair or MAU shall contribute no more than 10 mΩ.

As a trunk coaxial cable segment consists of several cable sections, all connectors and internal resistance of the shield and center conductor shall be included in the loop resistance measurement.

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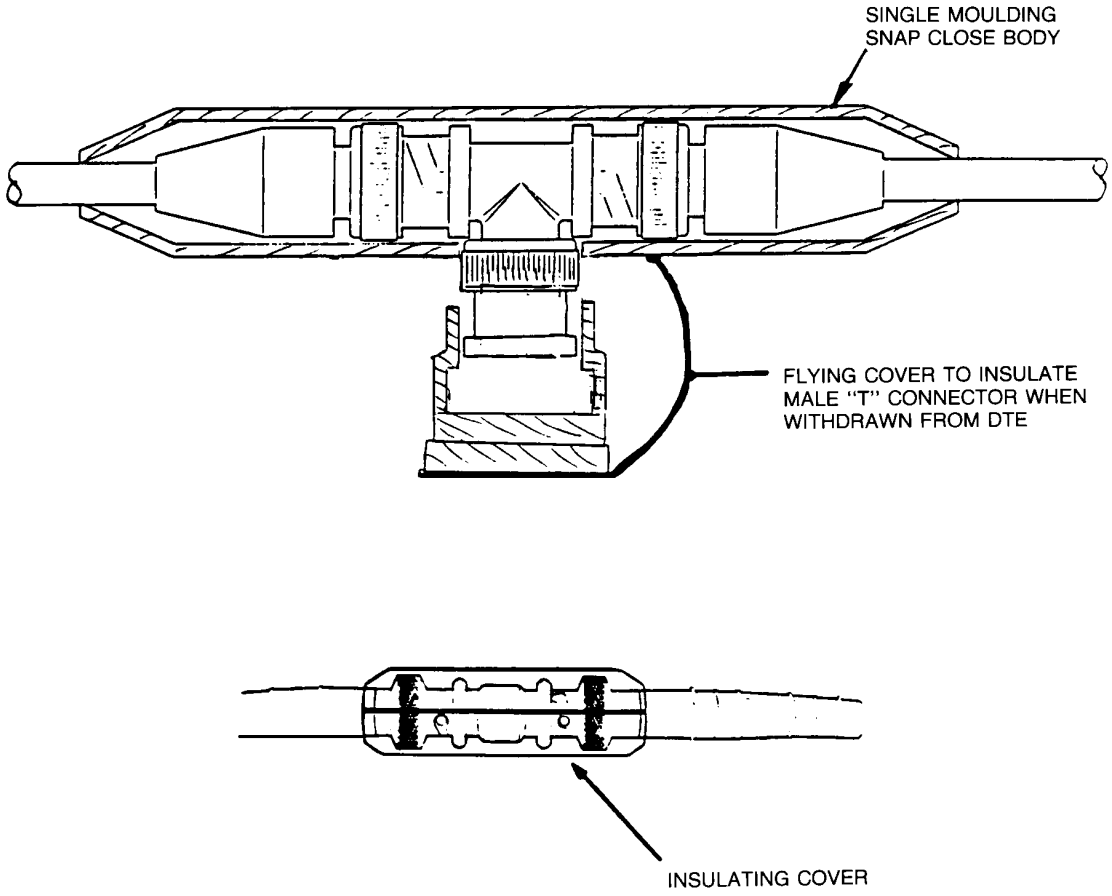
10.6 Coaxial trunk cable connectors

The trunk coaxial medium requires termination and is partitioned into sections. Devices to be attached to the medium require a means of connection to the medium. This means is provided by a BNC "T" adapter, as shown in Figure 10–7.



(Tutorial only and not part of the standard.)

Figure 10–7—Examples of insulated connector cover

The BNC connectors shall be of the 50 Ω constant impedance type. High-quality versions of these connectors (per IEC 169-8) are recommended in order to meet dc loop resistance and reliability considerations. All of the coaxial connectors shall follow the requirements as defined in 10.6.3.

10.6.1 In-line coaxial extension connector

All coaxial cables shall be terminated with BNC plug connectors. A means shall be provided to ensure that the connector shell (which connects to the cable sheath) does not make contact with any building metal (at ground potential) or other unintended conductor.

An insulating sleeve or boot slipped over the connector at installation time is suitable.

In-line coaxial extensions shall be made with BNC receptacle-to-receptacle connectors joined together to form one "barrel." An insulating sleeve or boot shall also be provided with each barrel assembly.

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10.6.2 Coaxial cable terminator

Coaxial cable terminators are used to provide a termination impedance for the cable equal in value to its characteristic impedance, thereby minimizing reflection from the ends of the cables. Terminators shall be packaged within a male or female connector. The termination impedance shall be 50 Ω ± 1% measured from 0 MHz to 20 MHz, with the magnitude of the phase angle of the impedance not to exceed 5°. The terminator power rating shall be 0.5 W or greater. A means of insulation shall be provided with each terminator.

10.6.3 MAU-to-coaxial cable connection

A BNC "T" (plug, receptacle, plug) adaptor provides a means of attaching a MAU to the coaxial cable. The connection shall not disturb the transmission line characteristics of the cable significantly; it shall present a low shunt capacitance, and therefore a negligibly short stub length. This is facilitated by the MAU being located as close to its cable connection as possible; the MAU and connector are normally considered to be one assembly. Long (greater than 4 cm) connections between the coaxial cable and the input of the MAU jeopardize this objective.

Overall system performance is dependent largely on the MAU-to-coaxial cable connection being of low shunt capacitance.

The design of the connection shall meet the electrical requirements contained in 10.4.1.1 and the reliability specified in 10.4.2.3. The use of BNC "T" adaptors and connectors satisfies these requirements. Figure 10–7 shows a MAU-to-coaxial cable attachment.

A means shall be provided to ensure that the connector assembly (that is, BNC "T" plus male connectors) does not make contact with any building metalwork (at ground potential) or any other unintended conductors. An insulating cover should therefore be applied after connection. A possible design is depicted in Figure 10–7. The insulating cover should have these characteristics:

a) It should guard against accidental grounding of the connector assembly.
b) It should allow ease of attachment and detachment of an assembled "T" connector to the MAU without necessitating the removal of section cable connectors (that is, segment integrity is maintained).
c) It should be a simple moulding that attaches firmly to a connector assembly.

10.7 System considerations

10.7.1 Transmission system model

The maximum configuration for the physical transmission system is as follows:

a) A trunk coaxial cable, terminated in its characteristic impedance at each end, constitutes a coaxial cable segment. A coaxial cable segment may contain a maximum of 185 m of coaxial cable and a maximum of 30 MAUs. The propagation velocity of the coaxial cable is assumed to be 0.65 c minimum ($c = 3 \times 10^8$ m/s). The maximum end-to-end propagation delay for a coaxial cable segment is 950 ns.
b) The maximum transmission path permitted between any two MAUs is limited by the number of repeater sets that can be connected in series.

   NOTE—Care should be taken to ensure that the safety requirements are met when extending the trunk cable by the use of repeaters (see 10.7.2.4.1).

c) The repeater unit specified in Clause 9 provides the means for connecting 10 Mb/s baseband segments into a CSMA/CD network. The proper operation of a CSMA/CD network requires network

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size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of the interpacket gap as it travels through the network. Configuration rules, which ensure that these limits are not exceeded, are given in Clause 13.

NOTE—Care should be taken to ensure that the safety requirements are met when extending the trunk cable by the use of repeaters (see 10.7.2.4.1)

Figure 10–8 and Figure 10–9 show minimal single segment and repeatered transmission systems. For specifications on the boundary conditions on topologies, see Clause 13.

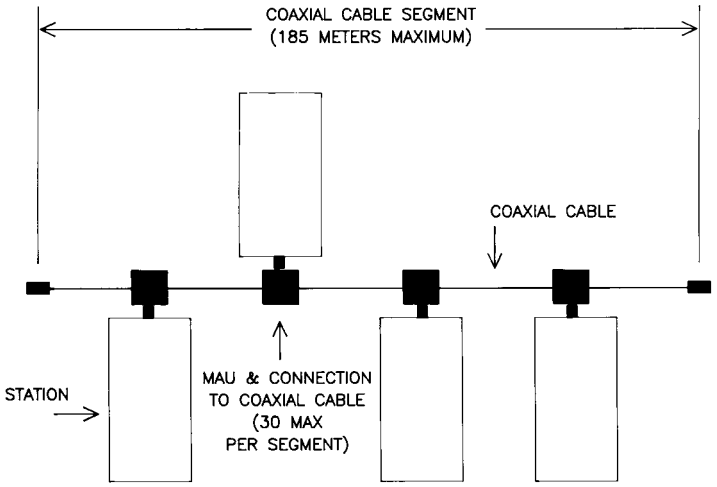

Figure 10–8—The minimum system configuration

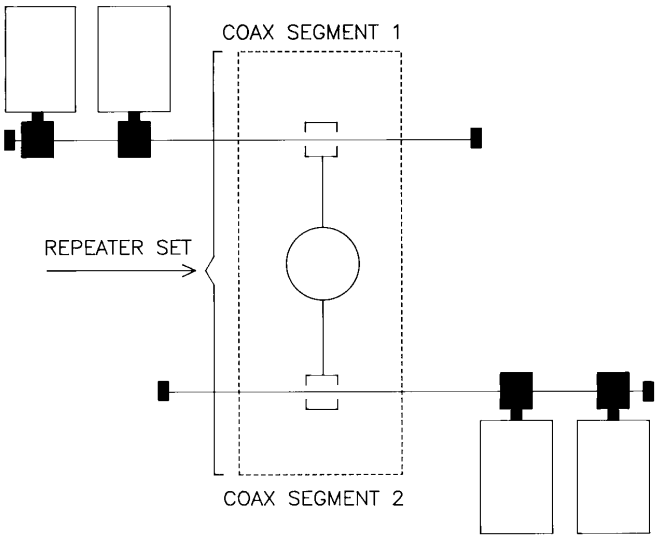

Figure 10–9—The minimum system configuration requiring a repeater set

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10.7.2 Transmission system requirements

10.7.2.1 Cable sectioning

The 185 m maximum length coaxial cable segment will be made from a number of cable sections. As the variation on cable characteristic impedance is ±2 Ω on 50 Ω, a possible worst-case reflection of 4% may result from the mismatch between two adjacent cable sections. The MAU will add to this reflection by the introduction of its noninfinite bridging impedance.

The accumulation of this reflection can be minimized by observing a minimum distance between MAUs (and between cable sections). In order to maintain reflections at an acceptable level, the minimum length cable section shall be 0.5 m.

10.7.2.2 MAU placement

MAU components and their associated connections to the cable cause signal reflections due to their noninfinite bridging impedance. While this impedance has to be implemented as specified in 10.6, the placement of MAUs along the coaxial cable also has to be controlled to ensure that reflections from the MAU do not accumulate to a significant degree.

Coaxial cable sections as specified in 10.7.2.1 shall be used to connect MAUs. This guarantees a minimum spacing between MAUs of 0.5 m.

The total number of MAUs on a cable segment shall not exceed 30.

10.7.2.3 Trunk cable system earthing

The shield conductor of each coaxial cable segment may make electrical contact with an effective earth reference[42] at one point and shall not make electrical contact with earth elsewhere on such objects as building structural metal, ducting, plumbing fixture, or other unintended conductor. Insulators should be used to cover any coaxial connectors used to join cable sections and terminators, to ensure that this requirement is met. A sleeve or boot attached at installation time is acceptable. (See 10.6.3.)

10.7.2.4 Static discharge path

A static discharge path shall be provided. The shield of the trunk coaxial cable is required to be connected to each DTE earth (within the DTE) via a 1 MΩ, 0.25 W resistor that has a voltage rating of at least 750 V dc.

10.7.2.4.1 Installation environment

This specification is intended for networks in use within a single building and within an area served by a single low-voltage power distribution system. Applications requiring interplant connections via external (outdoors) means may require special considerations. Repeaters and nonconducting IRL components may provide the means to satisfy these isolation requirements.

NOTE—The reader is advised that devices should not be operated at significantly different frame potentials. The 10BASE2 connection system may not be capable of handling excessive earth currents.

[42]See local or national regulations for guidance on these matters and reference [B53].

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10.8 Environmental specifications

10.8.1 Safety requirements

The designer should consult relevant local and national safety regulations to assure compliance with the appropriate standards (for example, see Annex A for reference material).

10.8.1.1 Installations

If the trunk coaxial cable is to be installed in close proximity to electrical power cables, then installation practice according to local and national code shall be followed (see Annex A for resource material).

10.8.1.2 Earthing

Where earthing is mandated by locally or nationally prescribed codes of practice, the shield of the trunk coaxial cable shall be effectively earthed at only one point along the length of the cable. Effectively earthed means permanently connected to earth through an earth connection of sufficiently low impedance and having sufficient ampacity to prevent the building up of voltages that may result in undue hazard to connected equipment or to persons.

10.8.2 Electromagnetic environment

10.8.2.1 Susceptibility levels

Sources of interference from the environment include electromagnetic fields, electrostatic discharge, transient voltages between earth connections, etc.

Several sources of interference will contribute to voltage buildup between the coaxial cable and the earth connection of a DTE.

The physical channel hardware shall meet its specifications when operating in either of the following conditions:

a) Ambient plane wave field of 1 V/m from 10 kHz through 1 GHz.

   NOTE—Levels typically >1 km from broadcast stations.

b) Interference source voltage of 15.10 V peak 10 MHz sine wave with a 50 Ω source resistance applied between the coaxial cable shield and the DTE ground connection.

MAUs meeting this standard should provide adequate RF ground return (coaxial cable shield to DTE ground) to satisfy the referenced EMC specifications.

10.8.2.2 Emission levels

The physical MAU and trunk cable system shall comply with local and national regulations (see Annex A for resource material).

10.8.3 Regulatory requirements

NOTE—Since September 2011, maintenance changes are no longer being considered for this clause. Since February 2021, electrical isolation requirements are in J.1.

The MAU and medium should consider IEC 60950 in addition to local and national regulations. See IEC 60950 and MIL-C-17F-1983 [B53].

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11. Broadband medium attachment unit and broadband medium specifications, type 10BROAD36

NOTE—This MAU is not recommended for new installations. Since September 2003, maintenance changes are no longer being considered for this clause.

11.1 Scope

11.1.1 Overview

This clause defines the functional, electrical, and mechanical characteristics of the Broadband Medium Attachment Unit (MAU) and the specific single- and dual-cable broadband media for use with LANs. The headend frequency translator for single-cable broadband systems is also defined. The relationship of this clause to all of the ISO/IEC LAN International Standards is shown in Figure 11–1. Repeaters as defined in Clause 9 are not relevant for 10BROAD36.

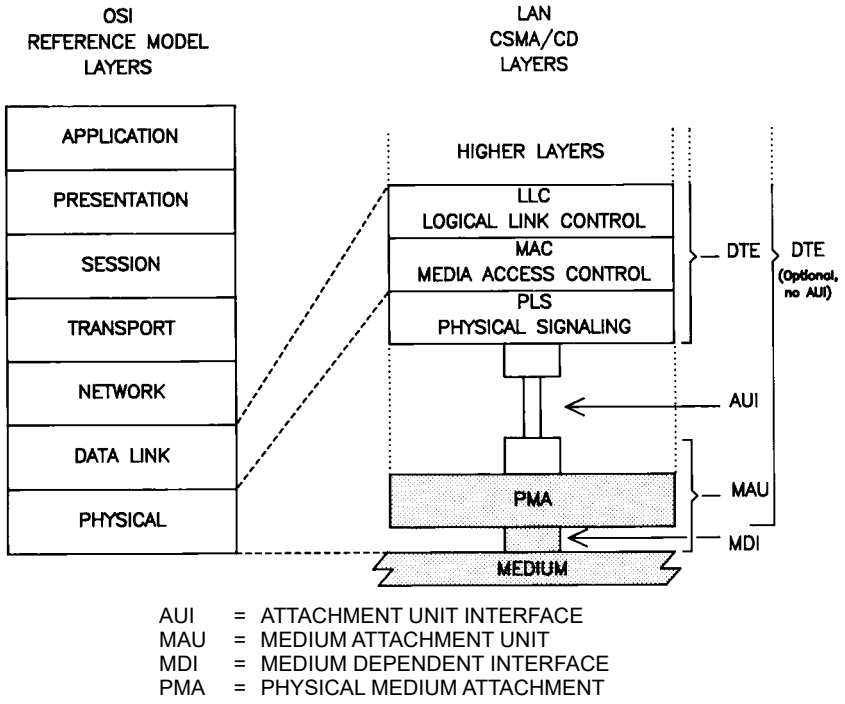

Figure 11–1—Physical Layer partitioning, relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

The purpose of the MAU is to provide a means of attaching devices to a broadband local network medium. The medium comprises CATV-type cable, taps, connectors, and amplifiers. A coaxial broadband system permits the assignment of different frequency bands to multiple applications. For example, a band in the spectrum can be utilized by LANs while other bands are used by point-to-point or multidrop links, television, or audio signals.

The physical tap is a passive directional device such that the MAU transmission is directed toward the headend location (reverse direction). On a single-cable system the transmission from the MAU is at a carrier fre-

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quency f1. A frequency translator (or remodulator) located at the headend up-converts to a carrier frequency f2, which is sent in the forward direction to the taps (receiver inputs). On a dual-cable system the transmit and receive carrier frequencies are identical (both f1) and the MAU connects to the medium via two taps, one on the receive cable and the other on the transmit cable. The transmit and receive cables are connected to each other at the headend location. Figure 11–2 shows broadband single- and dual-cable systems.

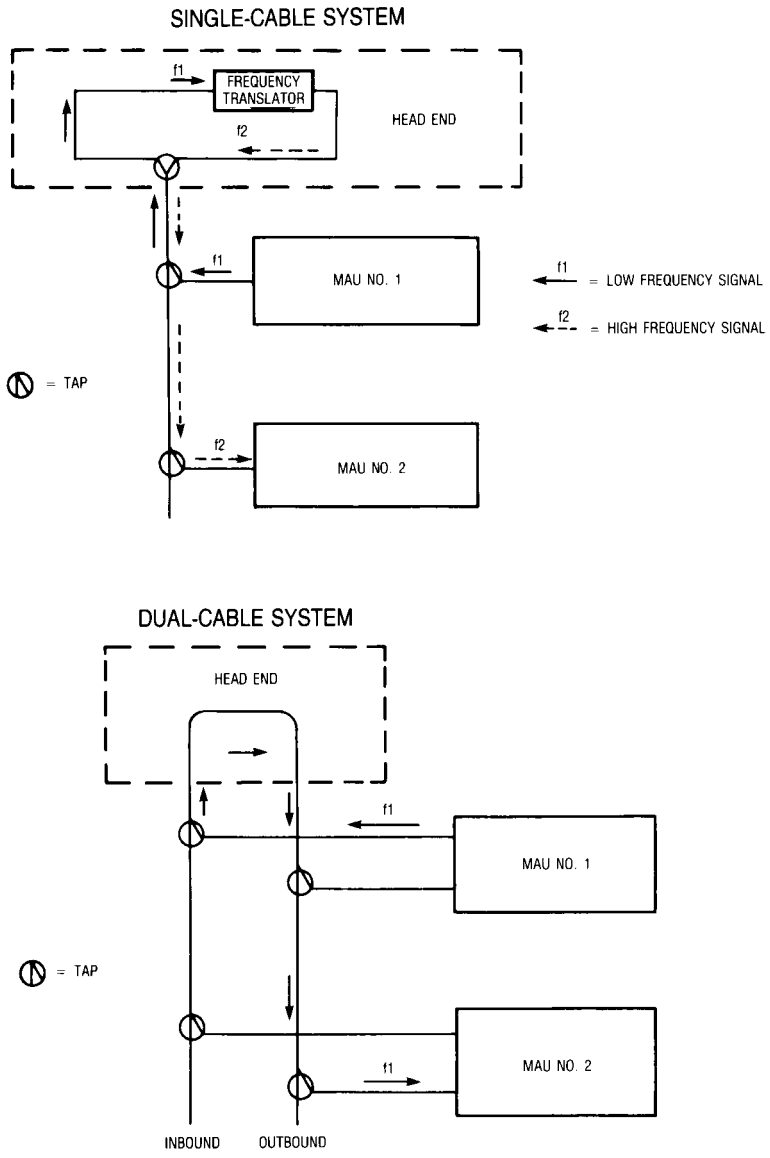

Figure 11–2—Broadband cable systems

The broadband MAU operates by accepting data from the attached Data Termination Equipment (DTE) and transmitting a modulated radio frequency (RF) data signal in a data band on the broadband coaxial cable system. All MAUs attached to the cable system receive and demodulate this RF signal and recover the DTE data. The broadband MAU emulates a baseband MAU except for delay between transmission and reception, which is inherent in the broadband cable system.

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A transmitting MAU logically compares the beginning of the received data with the data transmitted. Any difference between them, which may be due to errors caused by colliding transmissions, or reception of an earlier transmission from another MAU, or a bit error on the channel, is interpreted as a collision.

When a collision is recognized, the MAU stops transmission in the data band and begins transmission of an RF collision enforcement (CE) signal in a separate CE band adjacent to the data band. The CE signal is detected by all MAUs and informs them that a collision has occurred. All MAUs signal to their attached Medium Access Controllers (MACs) the presence of the collision. The transmitting MACs then begin the collision handling process.

Collision enforcement is necessary because RF data signals from different MAUs on the broadband cable system may be received at different power levels. During a collision between RF data signals at different levels, the MAU with the higher received power level may see no errors in the detected data stream. However, the MAU with the lower RF signal will see a difference between transmitted and received data; this MAU transmits the CE signal to force recognition of the collision by all transmitting MAUs.

11.1.2 Definitions

See 1.4.

11.1.3 MAU and medium objectives

This subclause states the broad objectives and assumptions underlying the specifications defined throughout this clause of the standard.

a) Provide the physical means for communication among local network Data Link Entities using a broadband coaxial medium.
b) Provide a broadband Medium Attachment Unit (MAU) that is compatible at the Attachment Unit Interface (AUI) with DTEs used on a baseband medium.
c) Provide a broadband MAU that emulates the baseband MAU except for the signal delay from Circuit DO to Circuit DI.
d) Provide a broadband MAU that detects collisions within the timing constraints specified in the baseband case.
e) Provide a broadband network diameter no less than 2800 m.
f) Provide a broadband Physical Layer that ensures that no MAU is allowed to capture the medium during a collision due to signal level advantage (that is, ensures fairness of the Physical Layer).
g) Provide a broadband MAU that detects collisions in both receive and transmit modes.
h) Provide a broadband MAU that requires a transmission bandwidth no wider than 18 MHz.
i) Define a physical interface that can be implemented independently among different manufacturers of hardware and achieve the intended level of compatibility when interconnected in a common broadband LAN.
j) Provide a communication channel capable of high bandwidth and low bit error ratio performance. The resultant mean bit error ratio at the Physical Layer service interface should be less than one part in 10^8 (on the order of one part in 10^9 at the link level) in a worst-case signal-to-noise ratio of 26 dB.
k) Provide a broadband medium Physical Layer that allows for implementation in both dual- and single-cable systems.
l) Provide for ease of installation and service.
m) Provide a communication channel that coexists with other channels on the same physical medium.

It is not an objective of this broadband MAU to allow its use with the baseband repeater defined in Clause 9 of this standard.

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11.1.4 Compatibility considerations

All implementations of the broadband coaxial system shall be compatible at the Medium Dependent Interface (MDI). This standard provides medium specifications for the interconnection of all MAU devices. The medium itself, the functional capability of the MAU and the AU Interface are defined to provide the highest possible level of compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the MAU in an application-dependent manner provided the MDI and AUI specifications are satisfied. Subsystems based on this specification may be implemented in several different ways provided compatibility at the medium is maintained. It is possible, for example, to design an integrated station where the MAU is contained within a physical DTE system component, thereby eliminating the AUI cable.

11.1.5 Relationship to PLS and AUI

The broadband MAU and cable system specifications are closely related to Clause 7 (Physical Signaling and Attachment Unit Interface Specifications). The design of a physical MAU component requires the use of both this clause and the PLS and AUI specifications in Clause 7.

11.1.6 Mode of operation

In its normal mode of operation, the MAU functions as a direct connection between the DTE and the broadband medium. Data from the DTE are transmitted onto the broadband coaxial system and all inband data on the coaxial cable system is received by the DTE. This mode is the mode of operation for the intended message traffic between stations. Other operating modes, such as a loopback mode or a monitor mode, may be provided but are not defined by this standard.

11.2 MAU functional specifications

11.2.1 MAU functional requirements

The MAU component provides the means by which signals on the physically separate AUI signal circuits to and from the DTE and their associated interlayer messages are coupled to the broadband coaxial medium. To achieve this basic objective, the MAU component contains the following capabilities to handle message flow between the DTE and the broadband medium:

a) *Transmit function.* The ability to transmit serial data bit streams originating at the local DTE in a band-limited modulated RF carrier form, to one or more remote DTEs on the same network.
b) *Receive function.* The ability to receive a modulated RF data signal in the band of interest from the broadband coaxial medium and demodulate it into a serial bit stream.
c) *Collision Presence function.* The ability to detect the presence of two or more stations' concurrent transmissions.
d) *Jabber function.* The ability of the MAU itself to interrupt the Transmit function and inhibit an abnormally long output data stream.

11.2.1.1 Transmit function requirements

The Transmit function shall include the following capabilities:

a) Receive Manchester encoded data sent by the local DTE to the attached MAU on Circuit DO (transmit data pair).
b) Decode the Manchester encoded data received on Circuit DO to produce NRZ (Non-Return to Zero) data and a recovered clock signal.

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c) Scramble the NRZ data using a CCITT V.29-type scrambler with seed changed on each transmitted packet.
d) Transform the incoming bits (prior to modulation) to provide an unscrambled alternating zero-one pattern terminated by an Unscrambled Mode Delimiter (UMD); scramble the remainder of the incoming preamble, Start Frame Delimiter (SFD), and data frame; and append an unscrambled postamble (Broadband End of Frame Delimiter [BEOFD]).
e) Differentially encode the packet generated above.
f) Produce a bandlimited, double sideband suppressed carrier, binary PSK modulated RF signal representing the above generated differentially encoded packet.
g) Drive the coaxial cable with the modulated RF signal.

Figure 11–3 functionally represents these capabilities. The order of the functional blocks may be altered provided that the result is the same.

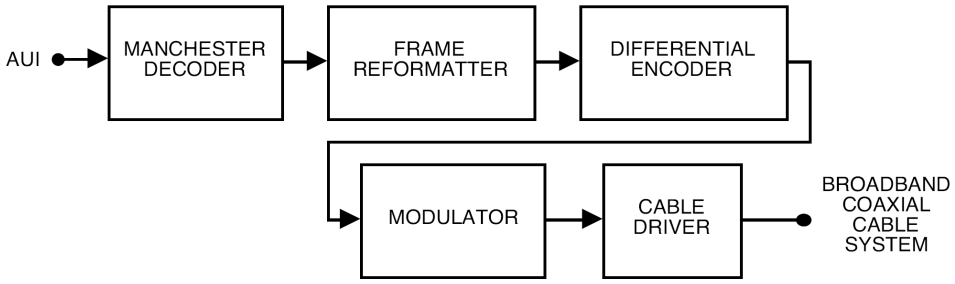

Figure 11–3—Transmit function requirements

11.2.1.2 Receive function requirements

The receive function shall include the following:

a) Receive the differentially encoded binary PSK modulated RF signal from the broadband coaxial medium.
b) Receive the data band RF signals and reject signals in bands other than the data band (rejection of signals in the adjacent collision enforcement band is optional).
c) Demodulate and differentially decode the incoming RF data signal from the coaxial medium to provide a receive bit stream that represents the scrambled bit stream at the transmitter.
d) Descramble the receive bit stream using a self-synchronizing descrambler.
e) Manchester encode the descrambled bit stream.
f) Send to the DTE, using Circuit DI (receive data pair), an additional, locally-generated, Manchester encoded preamble equal to the number of preamble bits lost in the receive data path (plus or minus one bit), followed by the Manchester encoded bit stream. No more than 6 preamble bits may be lost from the preamble presented to Circuit DO at the transmitting MAU.
g) Detect end of frame, using the postamble (BEOFD), and ensure that no extraneous bits are sent to the DTE on Circuit DI.
h) Receive signals in the collision enforcement band and reject signals in the data band and all other bands on the broadband medium.

11.2.1.3 Collision Detection function requirements

The MAU shall perform the following functions to meet the collision detection requirements:

a) Store the scrambled bits (not differentially encoded) in the transmit section through to the last bit in the source address.

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b) Detect the UMD in the transmit and receive paths.
c) Compare received scrambled bits after the received UMD with transmitted scrambled bits after the transmit UMD through to the last bit in the source address.
d) A Receive UMD Timer function shall be performed by the MAU. The timer shall be as long as the time required from initial detection of RF data signal presence to detection of a UMD in a normally received (no collision) packet.
e) Enter a LOCAL COLLISION DETection state if one of the following occurs:
    1) A bit error is found in the bit compare process through the last bit in the source address.
    2) The Receive UMD Timer expires before a UMD is detected in the received bit stream.
    3) The MAU receives the *output* (that is, transmit) signal from the AUI AFTER having received an RF signal from the coaxial cable.
f) Upon entering the LOCAL COLLISION DET state, cease transmission in the data band and commence transmission in the collision enforcement band for as long as the DTE continues to send data to the MAU.
g) Upon entering the LOCAL COLLISION DET state send the *signal_quality_error* (SQE) message on Circuit CI (collision presence pair) using the CS0 signal for as long as RF signals are detected on the broadband coaxial medium in either the data or collision enforcement bands.
h) Detect power in the collision enforcement band and send the SQE message on Circuit CI using the CS0 signal. Send the SQE message for as long as energy is detected in the collision enforcement band.
i) Ensure that during collisions, due to phase cancellations of the colliding carriers, Circuit DI does not become inactive before Circuit CI becomes active.
j) Test the collision detection circuitry following every transmission that does not encounter a collision. This test consists of transmitting a burst of collision enforcement RF signal after the end of the postamble transmission and detecting this burst on the receive side. If the burst is detected, the CS0 (BR) signal is sent on Circuit CI of the transmitting MAU.

11.2.1.3.1 Collision enforcement transmitter requirements

The MAU shall provide a collision enforcement (CE) transmitter that generates a constant amplitude RF signal in the CE band at the same power level as the data signal postamble.

11.2.1.3.2 Collision enforcement detection requirements

The MAU shall detect energy in the CE band that is within the specified range of receive levels, irrespective of the signal power level in the data band.

11.2.1.4 Jabber function requirements

The MAU shall have a Jabber function that inhibits transmission onto the coaxial cable interface if the MAU attempts to transmit an RF signal longer than 150 ms. The MAU shall provide an MTBF of at least 1 million hours of continuous operation without rendering the transmission medium unusable by other transceivers. Transmissions of less then 20 ms shall not be affected. When the jabber circuit is activated, *signal_quality_error* shall be sent on Circuit CI.

Circuit DO shall also be monitored for transmissions in excess of the maximum packet length. If the packet is longer than 20 ms, an attempt shall be made to deactivate the transmitter before the jabber circuit is activated, to avoid locking up the unit due to a non-MAU failure.

State diagrams defining the Jabber function may be found in 11.2.3.

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11.2.2 DTE PLS to MAU and MAU to DTE PLS messages

11.2.2.1 DTE Physical Layer to MAU Physical Layer messages

The following messages can be sent by the DTE Physical Layer entities to the MAU Physical Layer entities (refer to 7.3 of this standard for the definitions of the signals):

Message	Circuit	Signal	Meaning
output	DO	CD1, CD0	Output information
output_idle	DO	IDL	No data to be output

11.2.2.2 MAU Physical Layer to DTE Physical Layer messages

The following messages can be sent by the MAU Physical Layer entities to the DTE Physical Layer entities:

Message	Circuit	Signal	Meaning
input	DI	CD1, CD0	Input information
input_idle	DI	IDL	No input information
mau_available	CI	IDL	MAU is available for output
signal_quality_error	CI	CS0 (BR)	Error detected by MAU

11.2.2.2.1 *input* message

The MAU Physical Layer sends an *input* message to the DTE Physical Layer when the MAU has a bit of data to send to the DTE. The physical realization of the *input* message is a CD0 or CD1 sent by the MAU to the DTE on Circuit DI. The MAU sends CD0 if the input bit is a zero or CD1 if the input bit is a one. The jitter and asymmetry on CD0 and CD1 shall be no more than that specified in 7.5.2.1.

11.2.2.2.2 *input_idle* message

The MAU Physical Layer sends an *input_idle* message to the DTE Physical Layer when the MAU does not have data to send to the DTE. The physical realization of the *input_idle* message is the IDL signal sent by the MAU to the DTE on Circuit DI.

11.2.2.2.3 *mau_available* message

The MAU Physical Layer sends a *mau_available* message to the DTE Physical Layer when the MAU is available for output. The *mau_available* message is always sent by an MAU that is prepared to output data. The physical realization of the *mau_available* message is an IDL signal sent by the MAU to the DTE on Circuit CI.

11.2.2.3 *signal_quality_error* message

The *signal_quality_error* message shall be implemented in the following fashion:

a) The *signal_quality_error* (SQE) message shall not be sent by the MAU if no or only one MAU is transmitting a legal length packet (as specified in this standard) on the coaxial medium, except as a part of the SQE self test.

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b) If the MAU connected to the local node is not transmitting, then the local MAU shall send the *signal_quality_error* message in every instance when it detects power in the collision enforcement band earlier than the time equivalent for reception of a 512 bit data frame plus preamble and SFD.
c) When the local MAU is transmitting on the coaxial medium, all occurrences of one or more additional MAUs transmitting shall cause the *signal_quality_error* message to be sent by the local MAU to the attached DTE.
d) When the MAU has completed a successful transmission of a packet it shall perform an SQE Test sequence. In this instance, the collision enforcement RF signal is interpreted as an SQE Test signal.

11.2.3 MAU state diagrams

The operation of the MAU during normal transmission and reception can be described by a state diagram that relates the functions of transmission, reception, collision detection, and collision detection testing. Figure 11–4, at the end of this subclause, shows the state transitions for normal operation. Abnormal conditions are implementation-specific.

The state diagram in Figure 11–4 does not describe the operation of the MAU in detail. This is found in 11.2 and 11.3.

The operation of the Jabber function is described by the state diagram of Figure 11–5. When the MAU Jabber state machine is in the INTERRUPT or JAB state, outputs of the MAU Jabber state machine shall override those of the MAU state machine.

11.2.3.1 MAU state diagram messages

The following messages are used in the state diagram:

a) disable_data_driver. Deactivates the mechanism by which the RF data signal is impressed onto the coaxial cable.
b) enable_data_driver. Activates the mechanism by which the RF data signal is impressed onto the coaxial cable.
c) disable_CE_driver. Deactivates the mechanism by which collision enforcement RF signals are impressed onto the coaxial cable.
d) enable_CE_driver. Activates the mechanism by which collision enforcement RF signals are impressed onto the coaxial cable.
e) *mau_available.* Signifies that the MAU is available for transmission (that is, there is no SQE active).
f) *signal_quality_error* (SQE). Signifies that the MAU has detected a collision, it has successfully completed the SQE Test sequence, or the jabber circuit is active.
g) start_SQE_test_timer. Causes a timer to begin counting so that the SQE Test signal may be sent to the coaxial cable interface.
h) positive_disable. Prevents any RF signal from being sent onto the coaxial cable.

11.2.3.2 MAU state diagram signal names

The signal names used in the state diagram are as follows:

a) PowerOn. This signal signifies that power has been applied to the unit.
b) rx_energy. When this signal is active, an RF signal on the coaxial cable has been detected either in the data band or in the collision enforcement band or in both. The delay in asserting or de-asserting this signal is sufficiently short that the delays specified in 11.3.4.5 are met.
c) output. Signifies that data from the DTE is being presented for transmission at the AUI.
d) tx_umd (Transmit Unscrambled Mode Delimiter). When the Unscrambled Mode Delimiter has been detected in the transmit data sequence, this signal is asserted.

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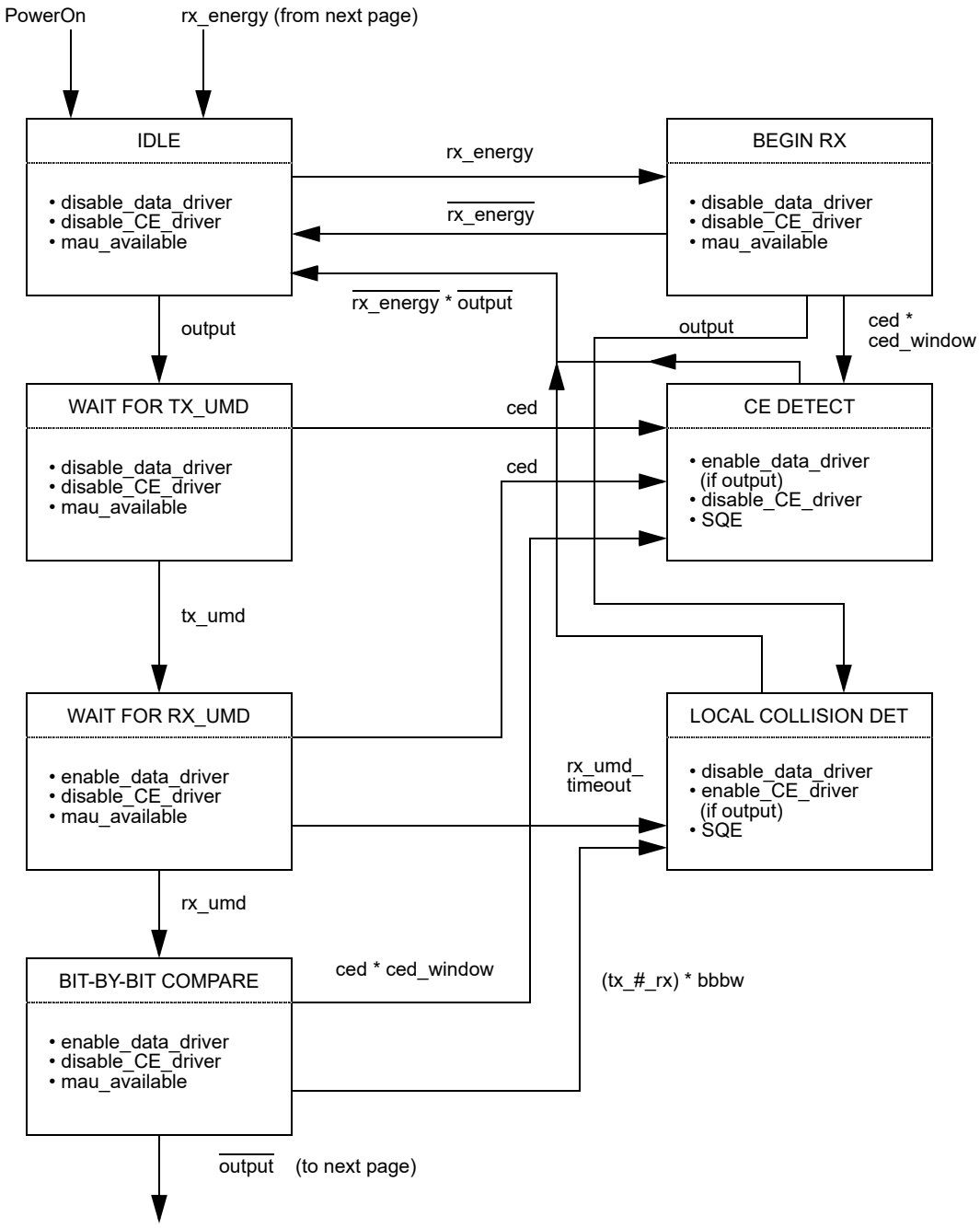

Figure 11–4—MAU state diagram

e) rx_umd (Receive Unscrambled Mode Delimiter). When the Unscrambled Mode Delimiter has been detected in the receive data sequence as it is conveyed from the coaxial cable interface, this signal is asserted.

f) SQE_test_timer. This signal is on during the time that the SQE Test Timer is engaged. At the end of the time, this signal is de-asserted.

g) rx (Receive). As long as data is being presented by the MAU to Circuit DI of the AUI, this signal is active. When the last bit of the receive data has been presented to the AUI, this signal is de-asserted.

h) ced (Collision Enforcement Detection). RF signal power in the collision enforcement band causes this signal to be asserted.

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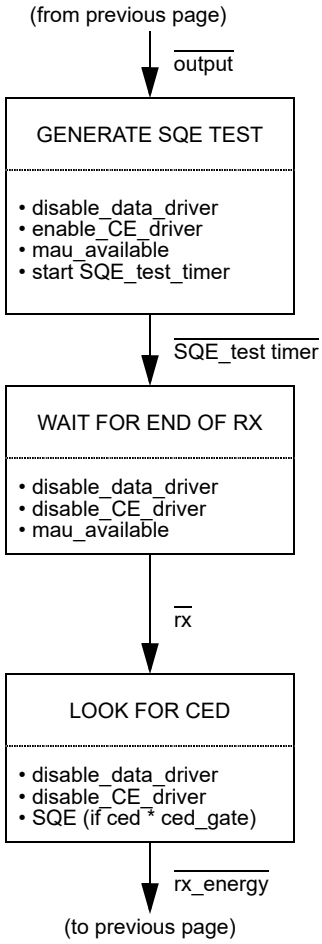

Figure 11-4—MAU state diagram *(continued)*

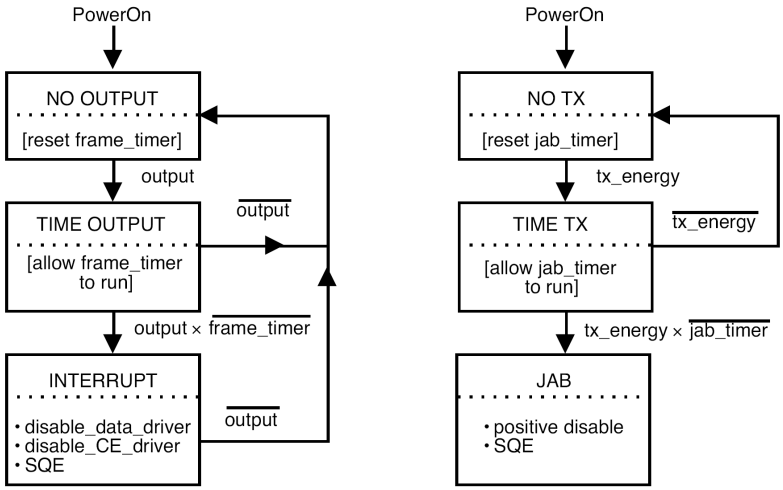

Figure 11–5—MAU jabber state diagram

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i) ced_window (Collision Enforcement Detection Window). This signal defines a period of time (a "window") during which collisions may occur. Its purpose is to distinguish collision enforcements from SQE Test sequences on the coaxial cable. The window opens when rx_energy goes active and closes a minimum of 365 bit times later. The maximum time the window may be open is the minimum frame length, plus preamble and SFD: 576 bits.
j) rx_umd_timeout (Receive Unscrambled Mode Delimiter Timeout). It is possible that the Receive Unscrambled Mode Delimiter may be corrupted by a collision such that the bit-by-bit comparison may not begin. This signal forces detection of a collision due to failure to detect the rx_umd within a maximum time. The timeout begins upon receipt of RF signal in the data band and expires 32 bit times later.
k) tx_#_rx (Transmit Not Equal to Receive). Assertion of this signal occurs when a difference is detected between the received data stream and the transmitted data stream.
l) bbbw (Bit-by-Bit Window). Bit-by-bit comparison shall be performed only for a time long enough to guarantee that the last bit of the source address has been examined. This signal is asserted after the UMD is received and throughout the bit-by-bit comparison process. To place a bound on the location of the source address relative to the UMD, the maximum preamble length permitted for operation with the broadband MAU is 62 bits. This places the last bit of the source address no later than 143 bits after the UMD.
m) ced_gate. This signal is a gating function that serves to shape the timing of ced during an SQE Test. It becomes true a minimum of 6 and a maximum of 16 bit times after the last bit has been presented to Circuit DI and stays active 10 bit times ± 5 bit times.
n) tx_energy. This signal signifies that the MAU is attempting to transmit an RF signal onto the coaxial cable.
o) frame_timer. This signal is on from the beginning of output until it is reset or until it has been on continuously for timeout1 s. The value of timeout1 shall be greater than 20 ms and less than timeout2.
p) jab_timer. This signal turns on when tx energy turns on and lasts until it is reset or until it has been on continuously for timeout2 s. The value of timeout2 shall be greater than timeout1 and less than 150 ms.

11.3 MAU characteristics

11.3.1 MAU-to-coaxial cable interface

The following subclauses describe the interface between the MAU and the broadband coaxial medium. The medium is a 75 Ω CATV-type broadband cable installation employing a single bidirectional cable with band-split amplifiers and filters, or dual unidirectional cables with line amplifiers.

11.3.1.1 Receive interface

11.3.1.1.1 Receive input impedance

The nominal input impedance at the receive port shall be 75 Ω. The return loss within the data and collision enforcement frequency bands shall be at least 14 dB with power applied to the MAU.

11.3.1.1.2 Receiver squelch requirements

There shall be a receiver squelch that inhibits reception of RF signals that are too low in level. This squelch shall permit reception of RF data or collision enforcement signals that are greater than or equal to –7 dBmV rms as measured by the method of 11.3.1.2.5. RF signals (data, collision enforcement, noise, or other signals) of levels lower than –15 dBmV rms shall be ignored.

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The receive squelch for CE signals shall be derived from a power detector with noise bandwidth greater than or equal to 1.5 MHz centered at the CE center frequency.

11.3.1.1.3 Receive level requirements

The receiver shall operate with RF data and CE signals having levels from –4 dBmV to +16 dBmV rms. The nominal receive level shall be +6 dBmV rms.

11.3.1.1.4 Receiver selectivity and linearity requirements

The MAU shall operate in the presence of single frequency (CW) signals adjacent to the receive band of the MAU and offset from the band edges, received at the following levels:

a) 0 dBmV rms at 0.25 MHz below and above the band
b) 10 dBmV rms at 1.25 MHz below and above the band

The receiver shall be capable of operating in a cable environment loaded with TV signals (for example, every 6 MHz in the USA). The TV signals shall be no higher than +10 dBmV peak video at the receiver coaxial cable interface.

11.3.1.1.5 Receive input mechanical requirements

The receiver mechanical interface shall be a 75 Ω female F-series coaxial connector. The connection to the broadband medium shall be through a coaxial drop cable with a mating male F-series connector. For single-cable configurations, the same connector may be used for receive and transmit.

11.3.1.2 Transmit interface

11.3.1.2.1 Transmit output impedance

The nominal output impedance at the transmit port shall be 75 Ω. The return loss within the data and collision enforcement frequency bands shall be at least 14 dB with power applied.

11.3.1.2.2 Transmitted RF packet format

Figure 11–6 shows the transmitted RF packet format.

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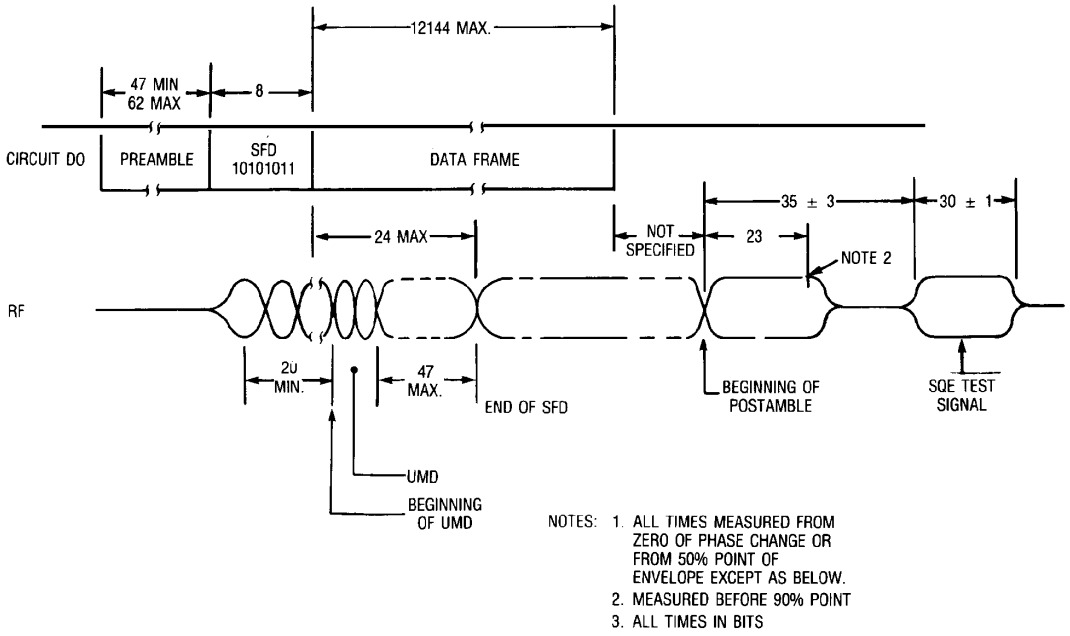

Figure 11–6—Packet format and timing diagram (AUI to coaxial cable interface)

11.3.1.2.3 Transmit spectrum and group delay characteristics

The transmit RF data signal shall be binary phase-shift-keyed (PSK) modulated and shall have a frequency spectrum equivalent to baseband raised-cosine Nyquist filtering with a rolloff factor (a) of 0.4, and within the limits of Figure 11–7. For rectangular pulses, the filter characteristic is

$$H(jw) \begin{cases} \dfrac{w(T/2)}{\sin\left(w\dfrac{T}{2}\right)}; & \left[0 <= w < \dfrac{\pi}{T}(1-a)\right] \\ \dfrac{w(T/2)}{\sin(wT/2)} \quad ;\cos^2\left(\dfrac{T}{4a}\left[w - \dfrac{\pi(1-a)}{T}\right]\right); & \left[\dfrac{\pi}{t}(1-a) <= w < \dfrac{\pi}{T}(1+a)\right] \\ 0; & \left[w >= \dfrac{\pi}{T}(1+a)\right] \end{cases}$$

where T = one symbol time (100 ns for 10 Mb/s) and a = 0.4, and the first term accounts for the sin x/x spectrum of NRZ random data.

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The total variation in group delay from Circuit DO to the RF coaxial medium interface shall not exceed 20 ns in the frequency band from the carrier frequency to ± 5 MHz, and 32 ns to ± 5.5 MHz.

The collision enforcement (CE) signal shall be a constant amplitude pulse with controlled turn-on and turn-off times. Random modulation may be added to reduce the probability of cancellation when more than one CE signal is received simultaneously. The modulated signal shall have an instantaneous frequency within 0.75 MHz of the CE band center frequency and shall conform to the spectrum mask specified in 11.3.1.2.4. The random modulation may be derived from the transmit NRZ data stream.
The CE signal rise and fall times shall approximate a Gaussian shape of the form

$$f(t) = \exp\left(-\frac{1}{2}\left[\frac{t}{T}\right]^2\right)$$

where T = one symbol time and $t < 0$ for the rise time and $t > 0$ for the fall time.

The CE and data RF signals shall not be transmitted simultaneously.

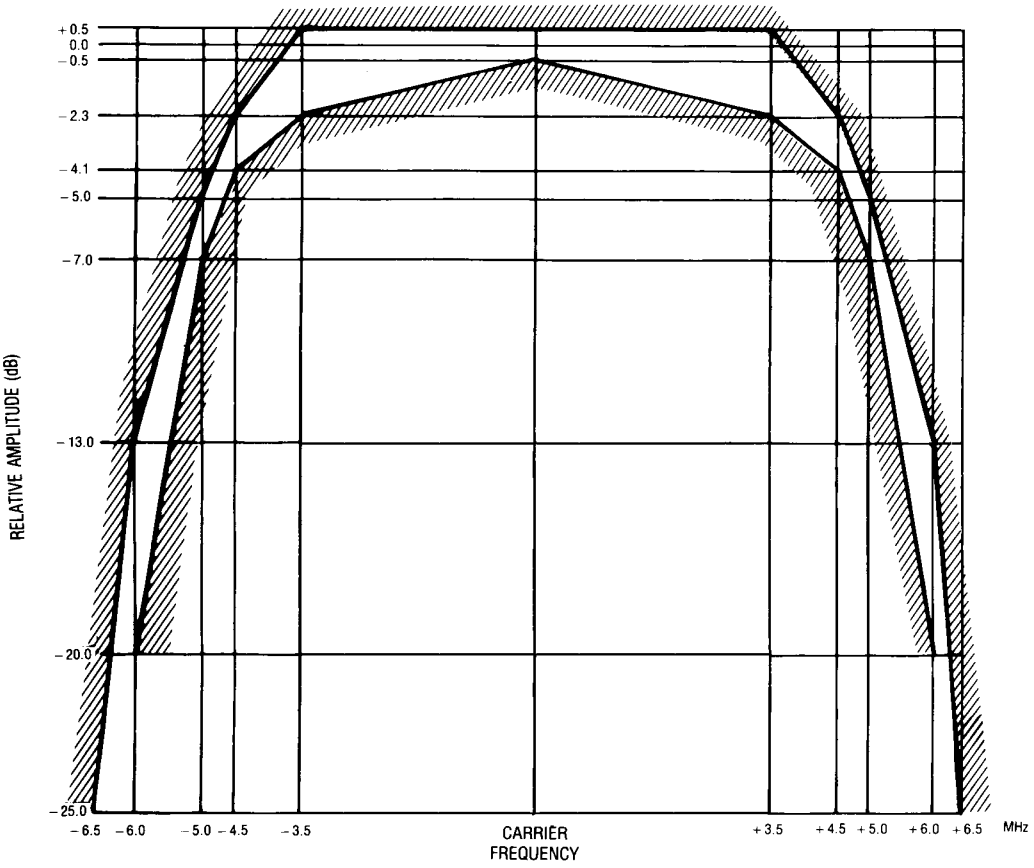

Figure 11–7—Spectrum mask for RF data signal

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11.3.1.2.4 Transmit out-of-band spectrum

The transmitted power outside the specified band shall meet or exceed the relative attenuation (RA) specified below, under the following conditions:

a) Transmitted packet length is 256 bits with a 25.6 μs interval between packets, for 50% duty cycle on the cable.
b) Reference level is an unmodulated carrier, equivalent to the postamble transmitted level.
c) *RA* is the attenuation in decibels relative to the reference level outside the specified band, measured in a 30 kHz noise bandwidth with a video filter of 300 Hz bandwidth or less.
d) *B* is 18 MHz, the width of data plus collision enforcement bands.
e) *MF* is the measurement frequency in MHz.
f) *NCEF* is the frequency of the nearest edge of the band, in MHz.

$$RA = \min (63, 55 + 30 \times | (MF - NCEF) / B|)$$

Figure 11–8 graphically shows the attenuation requirement for out-of-band power.

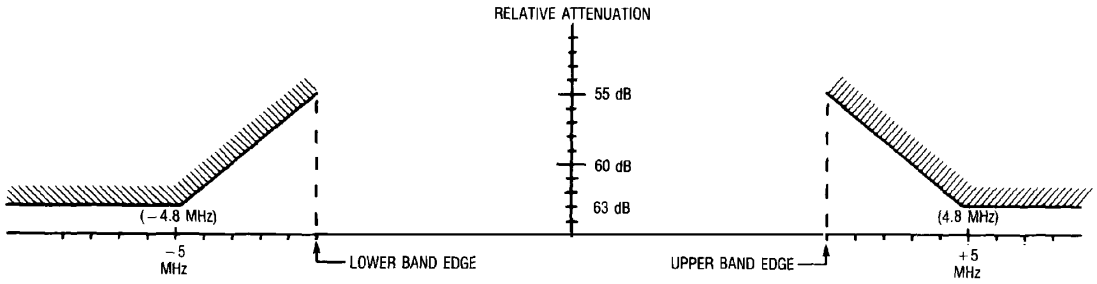

Figure 11–8—Transmit out-of-band power attenuation

11.3.1.2.5 Transmit level requirements

The transmitter output power during the postamble and during the SQE Test of the collision enforcement signal shall be 1000 mV peak-to-peak into a 75 Ω load (51 dBmV rms). Truncation loss due to the specified data filtering is 1 dB; transmitted RF data signal power is 50 dBmV rms. Transmit output power variations shall not exceed ± 2 dB.

11.3.1.2.6 Nontransmitting signal leakage requirement

The RF data signal and collision enforcement signal leakage to the coaxial cable interface while the MAU is not in its transmission mode shall be less than –20 dBmV rms.

11.3.1.2.7 Transmit spurious output requirement

All spurious signals from the transmitter (inband and out-of-band) while not transmitting shall be less than –20 dBmV rms. All spurious signals from the transmitter while transmitting data or collision enforcement shall be below the spectrum mask specified in 11.3.1.2.4.

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11.3.1.2.8 Collision enforcement signal leakage requirement

The collision enforcement RF signal leakage to the coaxial cable during data transmission and while the MAU is not enforcing collisions shall be less than 5 dBmV rms. Leakage shall be less than –20 dBmV rms when the MAU is not in the transmission mode.

11.3.1.2.9 Transmit output mechanical requirements

The transmit mechanical interface shall be a 75 Ω female F-series coaxial connector. The connection to the broadband medium shall be through a coaxial drop cable with a mating male F-series connector. For single cable installations, the same connector may be used for transmit and receive.

11.3.2 MAU frequency allocations

The broadband MAU uses a data band 14 MHz wide and an adjacent collision enforcement band 4 MHz wide. A single cable midsplit configuration with a frequency offset of 156.25 MHz or 192.25 MHz between forward and reverse channels is recommended. Other configurations, including dual-cable, where forward and reverse channels are on separate unidirectional cables, also are permitted.[43] The preferred pairing for the usual North American 6 MHz channels is specified in Table 11–1 and Table 11–2. The tables also specify the data carrier or collision enforcement center frequency for each band, and for single-cable systems, the frequency translation and the headend local oscillator frequency.

11.3.2.1 Single-cable systems frequency allocations

Table 11–1 lists the permissible frequency band allocations for single-cable systems. The 192.25 MHz translation is recommended for all new designs. The 156.25 MHz translation is allowed for compatibility with some existing systems. The 156.25 MHz translation results in a reversal of the data and collision enforcement bands, as the lower sideband is used.

Table 11–1—Single-cable frequency allocations (frequencies in MHz)

TRANSMITTER				RECEIVER		
Data carrier	Coll enf center freq	Transmit band	Translation 156.25 MHz		Translation 192.25 MHz	
			Headend local osc	Receive band	Headend local osc	Receive band
43	52	35.75–53.75	245.75	192-210	192.25	228-246
49	58	41.75–59.75	257.75	198-216	192.25	234-252
55	64	47.75–65.75	269.75	204-222	192.25	240-258
+61	70	53.75–71.75	281.75	210-228	192.25	246-264
67	76	59.75–77.75	293.75	216-234	192.25	252-270
73	82	65.75-83.75	305.75	222-240	192.25	258-276

NOTE 1—Some of these optional bands are overlapping.
NOTE 2—Frequency tolerance of the data carrier and headend local oscillator are ± 25 kHz each.
NOTE 3—+ denotes the preferred frequency allocation.

[43] The remainder of 11.3.2 and all of 11.3.2.1 and 11.3.2.2 are not part of the ISO/IEC International Standard. Frequency allocations are a subject for national standardization.

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11.3.2.2 Dual-cable systems frequency allocations[44]

In nontranslated dual-cable systems transmit and receive frequencies are identical. Table 11–2 lists the permissible frequency band allocations. In some instances translated dual-cable systems are installed. In such cases the single-cable frequency allocations may be used.

Table 11–2—Dual-cable frequency allocations (frequencies in MHz)

Data carrier	Coll enf center freq	Data band	Coll enf band
43	52	36–50	50–54
49	58	42–56	56–60
55	64	48–62	62–66
+61	70	54–68	68–72
67	76	60–74	74–78
73	82	66–80	80–84
235.25	244.25	228–242	242–246
241.25	250.25	234–248	248–252
247.25	256.25	240–254	254–258
253.25	262.25	246–260	260–264
259.25	268.25	252–266	266–270
265.25	274.25	258–272	272–276

NOTE 1— Some of these optional bands are overlapping.
NOTE 2—Frequency tolerance of the data carrier is ± 25 kHz.
NOTE 3— + denotes the preferred frequency allocations.

11.3.3 AUI electrical characteristics

11.3.3.1 Electrical isolation requirements

The MAU has to provide isolation between the AUI cable and the broadband coaxial medium. The isolation impedance shall be greater than 250 kΩ at 60 Hz, measured between any conductor (including shield) of the AU Interface cable and either the center conductor or shield of the coaxial cable. The isolation means provided shall be able to withstand 500 Vac rms for one minute.

The MAU power supply, if provided, shall meet the appropriate national requirements. See IEC 950: 1991 for guidance.

11.3.3.2 Current consumption

The MAU may have its own power supply but is also allowed to use the power supplied by the DTE through the AUI cable. When drawing current from the AUI, the current shall not exceed 0.5 A as provided by the AUI source. The MAU shall be capable of operating from all possible voltage sources as supplied by the DTE through the resistance of all permissible AUI cables. The MAU shall not disrupt the broadband coaxial medium should the DTE power source fall below the minimum operational level under abnormal MAU load conditions. The MAU shall be labeled externally to identify the nominal value of current required by the device at the AUI.

[44] See Footnote 43.

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11.3.3.3 Driver and receiver requirements

The requirements for AUI cable driver and receiver components within the MAU are identical with those specified in Clause 7 of this standard. The drivers shall provide signals that meet the symmetry and jitter requirements of Circuit DI defined in Clause 7 and the receivers shall accept signals that have traversed the worst-case lengths of AUI cable.

11.3.3.4 AUI mechanical connection

The MAU shall be provided with a 15-pin male connector as specified in detail in the PLS/AUI specifications, in 7.6 of this standard.

11.3.4 MAU transfer characteristics

Signals presented on Circuit DO are transformed into signals at the coaxial cable interface by delaying them and by reformatting them. Signals at the coaxial cable interface are transformed into signals on Circuit DI and Circuit CI by a different framing change and by additional delay.

11.3.4.1 AUI to coaxial cable framing characteristics.

Data presented on Circuit DO shall first be received differentially, then Manchester decoded into an NRZ data stream. The framing of the data shall then be transformed into a new packet for presentation to the RF modulator in the following way (see Figure 11–6 and Figure 11–9):

a) Up to 5 bits of the incoming data stream may be dropped for detection and Manchester decoding purposes.
b) Beginning with the first zero, 20 bits of zero-one pattern shall be sent for receiver synchronization and clock recovery.

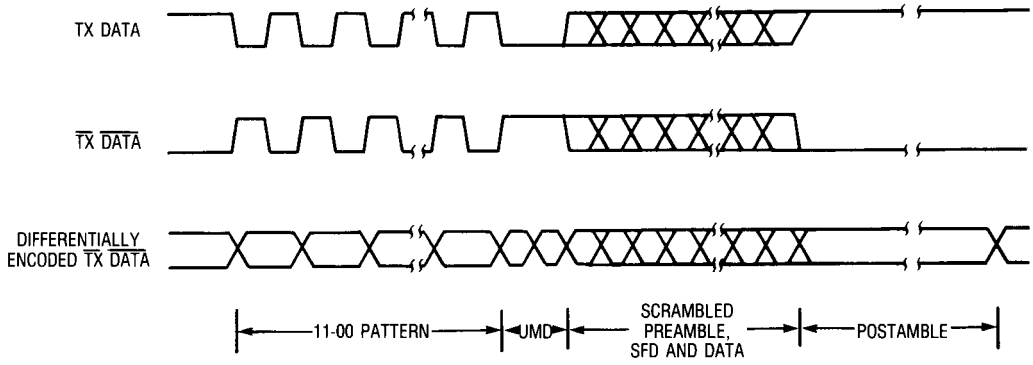

Figure 11–9—Packet format at modulator input

c) The next two bits (zero-one in the incoming pattern) shall both be set to zero and form the Unscrambled Mode Delimiter (UMD). The UMD shall take the place of the zero-one in the incoming pattern; it shall not be inserted into the data stream.
d) All remaining bits in the preamble, SFD, and data fields shall be scrambled (using a CCITT V.29 scrambler plus a differential encoder per 11.3.4.1).
e) A postamble (BEOFD) consisting of a zero followed by 22 ones shall be added immediately after the last scrambled data bit (the postamble is not scrambled). The postamble may be extended to allow controlled turnoff of the transmitted signal, as shown in Figure 11–6.

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f) All bits (unmodified preamble; UMD; scrambled preamble, SFD, and data; and postamble) are inverted.
g) All bits sent to the RF modulator are differentially encoded. Figure 11–9 shows the appearance of the data before and after the differential encoder.
h) The SQE Test sequence shall be generated after a successful data transmission by transmitting a collision enforcement RF signal with the timing shown in Figure 11–6.

Because the preamble of the incoming data on Circuit DO is modified, it is assumed that DTEs generate a minimum length preamble of 47 bits. The maximum preamble length is allowed to be 62 bits, as shown in Figure 11–6.

11.3.4.1.1 Scrambler and differential encoding requirements

The NRZ data shall be scrambled (using a CCITT V.29-type scrambler). A new seed shall be used by the scrambler for every new packet presented by the DTE to the MAU. Figure 11–10 is a diagram of a typical scrambler implementation.

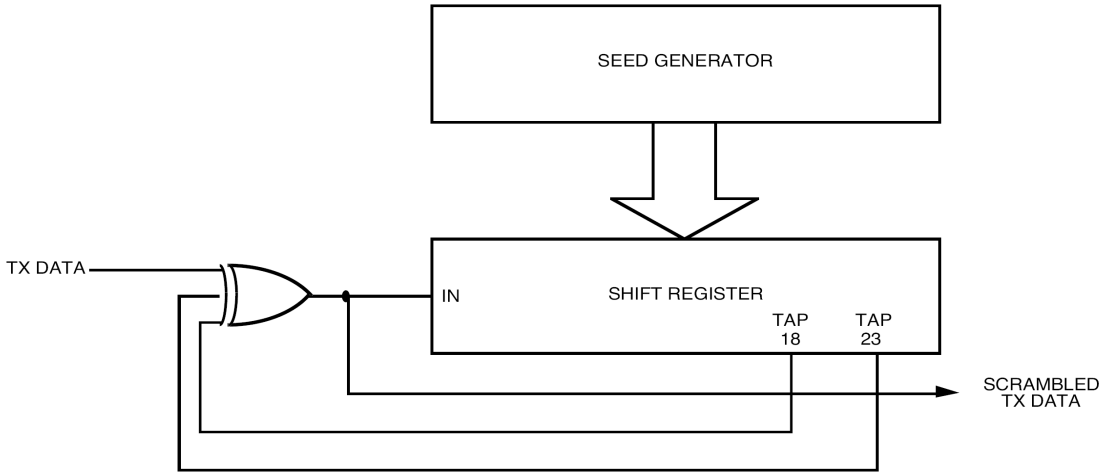

Figure 11–10—Scrambler

The scrambled NRZ data shall be differentially encoded (see Figure 11–11 for a typical implementation).

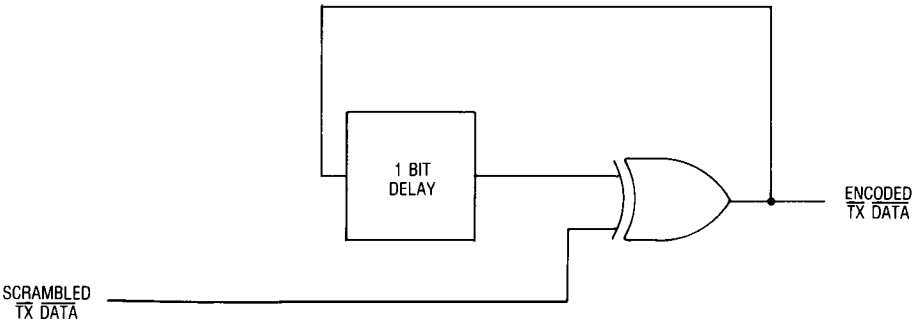

Figure 11–11—Differential encoder

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The entire encoding process comprising the scrambling and differential encoding is essentially equivalent to a division of the polynomial representing the data to be transmitted by the following polynomial:

$$G(x) = 1 + x^{-1} + x^{-18} + x^{-19} + x^{-23} + x^{-24}$$

11.3.4.2 Coaxial cable to AUI framing characteristics

The MAU shall demodulate, differentially decode, and invert the received RF data signal to recover the scrambled and inverted data stream. Clock shall be recovered and a replica of the unfiltered and noninverted transmitted data stream shall be created. The restored data shall be forced to a logic "one" state whenever no RF data signal is detected. This prevents false UMD detection and forces postamble detection when no carrier is present.

The framing information contained in the RF data stream shall be used to reconstruct the received data so that no more than 6 bits are lost and no more than one bit added to the preamble field, and no bits are added to or lost from the end of the transmit data. Detection of the UMD in the receive data shall initiate, after a fixed delay, a locally generated preamble sequence of zero-one pattern. This pattern "fills in" the preamble bits altered due to the framing information at the beginning of the packet: the zero-one synchronization and clock recovery sequence, the UMD, and the descrambler synchronization sequence.

The MAU shall descramble the received data using a self-synchronizing (CCITT V.29-type) descrambler. No prior knowledge of the seed used by the scrambler shall be assumed by the descrambler circuit. The descrambler shall have valid output no later than 23 bit intervals after the UMD is detected by the receiver. An example of a descrambler is shown in Figure 11–12. The differential decoding performed by the demodulator and the descrambling function are essentially equivalent to multiplying the received polynomial by G(x) as defined in the scrambling and differential encoding requirements subclause above.

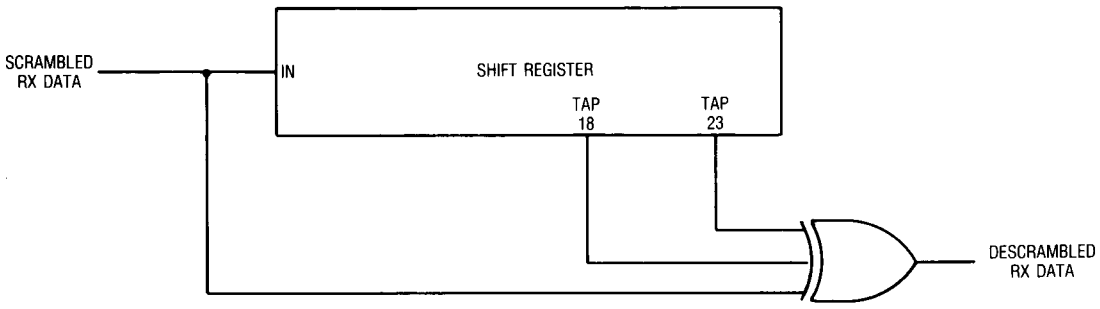

Figure 11–12—Descrambler

After the descrambler is synchronized, 23 bits after the UMD, the correctly descrambled receive data, starting with the 24th bit after the UMD, shall be transferred to the Manchester encoder and therefrom to the AUI. The delay from the detection of the UMD to the beginning of the locally generated zero-one pattern shall be chosen so that no more than 6 bits of preamble are lost, and no more than one bit added, in transmission from Circuit DO to Circuit DI.

The MAU shall detect the "zero" followed by 22 "ones" (the postamble pattern) and, in conjunction with the loss of carrier detection in the data band or the presence of a collision enforcement detection signal, shall ensure that the packet presented to the local DTE has no extraneous bits added by the MAU to the end of the packet.

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The SQE Test signal shall be detected on the RF interface and the SQE signal shall be presented to Circuit CI of the transmitting MAU, subject to the timing restrictions of 11.3.4.5.4. If the signal is not observed at the RF interface due to failure of any element in the transmitter or receiver, no SQE signal may be presented to the AUI. In the event of a collision enforcement, energy will appear in the collision enforcement band within the ced_window time after energy first appears in the data band. Circuit CI shall be asserted when collision enforcement is first detected and shall continue to be active until after the RF signal on the RF port has subsided. Note that an SQE Test signal appended to a packet whose length is less than the ced_window time (less than the minimum allowed packet length) will be indistinguishable from a collision enforcement, except by the MAU transmitting. The transmitting MAU shall take this into account and shall not interpret energy in the collision enforcement band to be a collision when the length of the transmitted packet is less than the ced_window time and the SQE Test sequence has been transmitted. See the discussion in 11.4.2 for more information on ced_window.

11.3.4.3 Circuit DO to circuit DI framing characteristics

In the absence of a collision, the packet format of the receive data at the AUI is identical to that of the transmit data, except that there may be one more preamble bit than was sent at the transmit port and up to 6 bits of the preamble lost. In the presence of a collision, the receive data is undefined, but shall still be properly Manchester encoded.

11.3.4.4 AUI to coaxial cable delay characteristics

The timing and delays associated with the transmitter of the MAU are identified below. To ensure compatibility with all MAUs the delays identified below cannot be exceeded nor traded off with other delays in the system.

11.3.4.4.1 Circuit DO to RF data signal delay

The delay from a transition on Circuit DO at the end of a bit to the corresponding phase change of the RF data signal (such bit chosen so that an RF burst phase change does exist) shall be no more than 24 bit times. The delay from the first transition on Circuit DO to the first appearance of RF energy, however, is not specified except as it is determined by other timing constraints.

11.3.4.4.2 Circuit DO to CE RF output delay

In the event that the MAU begins receiving energy on the coaxial medium just before the DTE presents data to the AUI, a collision shall be detected locally, as described in Figure 11–4. The delay from the first bit at Circuit DO of the AUI to the presentation of collision enforcement at the coaxial cable interface in this circumstance shall be 32 bit times maximum.

11.3.4.4.3 Transmit postamble to SQE test signal delay

The delay from the initial transition of the first bit of the postamble (Broadband End of Frame Delimiter) measured at the RF port to the 50% point of the rising edge of the SQE Test signal shall be 35 bit times ± 3 bit times.

11.3.4.4.4 SQE test signal length

The SQE Test signal length shall be 30 bit times ± 1 bit time as measured at the 50% points of the RF signal.

11.3.4.5 Coaxial cable to AUI delay characteristics

The MAU receiver timing and delays described below shall not be exceeded or traded off against any other delays in the system.

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11.3.4.5.1 Received RF to circuit DI delay

When there is no collision in progress, the delay from the end of the SFD in the received RF data signal at the coaxial cable interface to the end of the SFD on Circuit DI, shall be a maximum of 75 bit times (see Figure 11–13). The minimum is not specified, nor is the delay specified at other locations in the packet. The end of the SFD in the received RF data signal (at the coaxial cable interface) is defined as the time at which the envelope of the carrier would pass through the midpoint if the first bit following the SFD was a zero and the scrambler disabled.

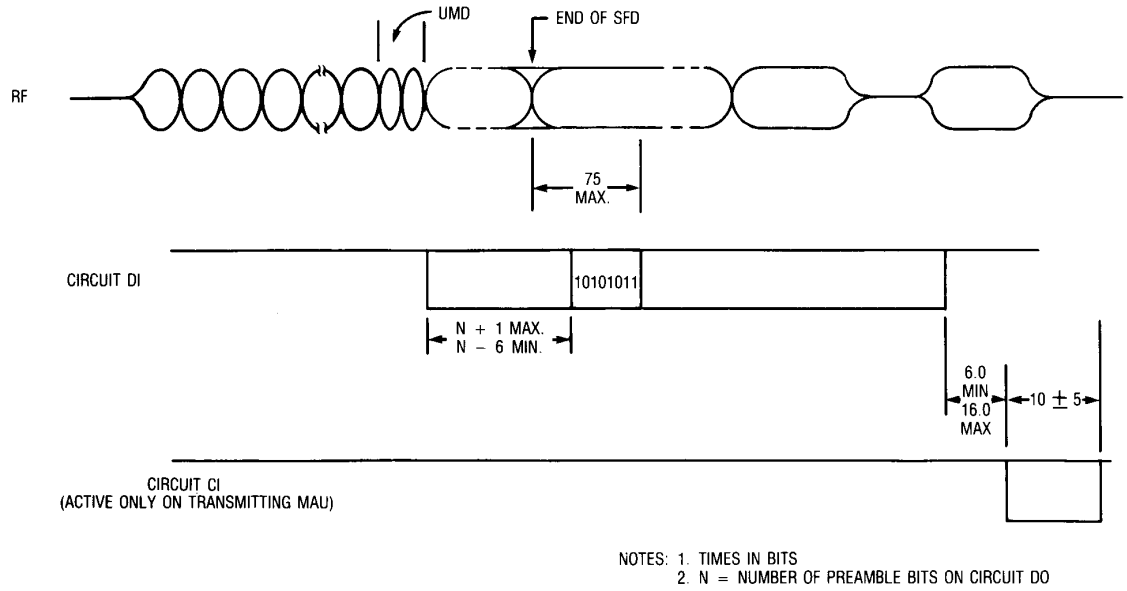

Figure 11–13—No collision timing diagram (coax to AUI)

11.3.4.5.2 Received RF to CE RF output and circuit CI delay

In the event that a collision is detected via the bit-by-bit comparison, the delay from the end of the bit in which the collision was detected, as represented by the RF signal, to the 50% point on the rising edge of the collision enforcement signal shall not exceed 34 bit times. The delay from the same point to the first transition of Circuit CI shall not exceed 27 bit times. Circuit CI shall cease activity no more than 31 bit times after activity on the RF interface (in both data channel and collision enforcement channel) ceases. See Figure 11–14 and Figure 11–15.

11.3.4.5.3 Collision enforcement to circuit CI delay

In the event of a collision enforcement by another MAU, the delay from the 50% point on the rising edge of the RF collision enforcement signal to the first transition of Circuit CI shall be no more than 31 bit times. Circuit CI shall be active for a minimum of 5 bit times and shall become inactive within 31 bit times of the cessation of activity on the RF coaxial cable interface, as shown in Figure 11–15.

11.3.4.5.4 Receive data to SQE test delay

If a collision enforcement signal is received after the ced_window signal becomes inactive [see item i) in 11.2.3.2], or if the MAU has transmitted an SQE Test sequence, the MAU is to interpret the collision enforcement signal as an SQE Test signal. If the SQE Test sequence is correctly detected (that is, the test passes), then the delay from the last transition of Circuit DI to the first transition of Circuit CI shall be at

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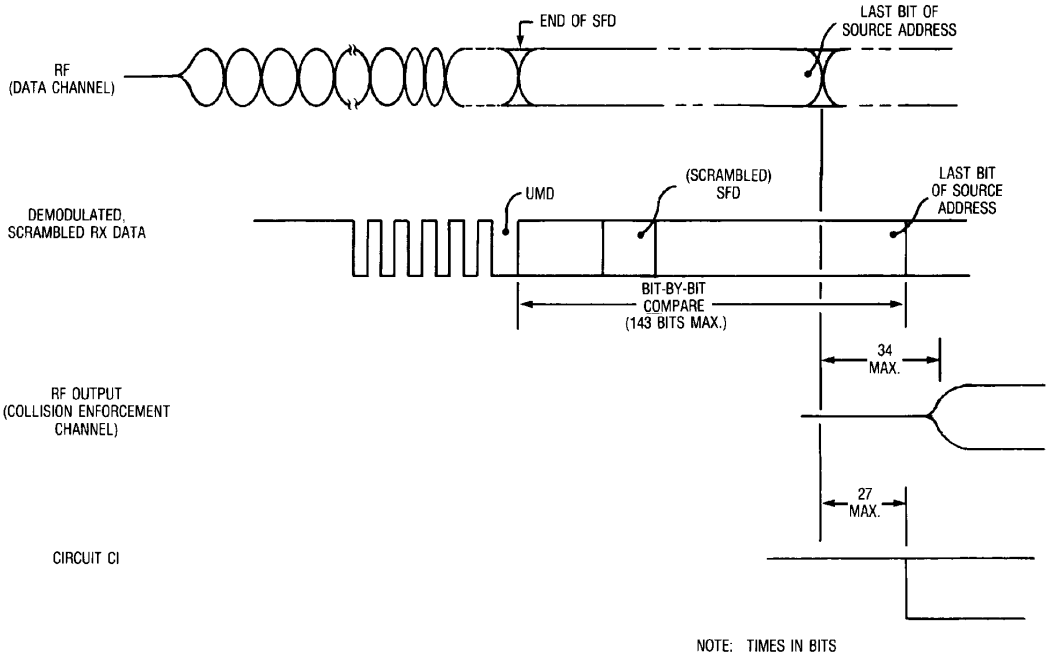

Figure 11–14—Collision timing diagram (RF data to RF collision enforcement)

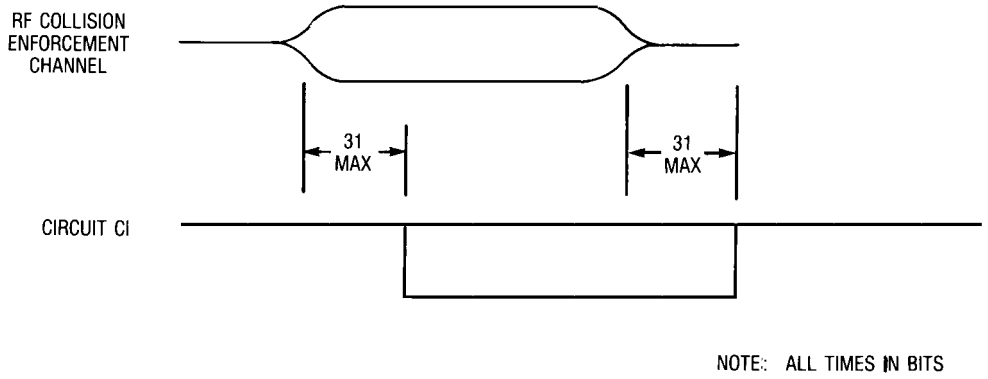

Figure 11–15—Collision timing diagram (coaxial cable interface to AUI circuit)

least 6 but not more than 16 bit times. Circuit CI shall remain active for 10 bit times ± 5 bit times. Only the transmitting MAU shall assert its Circuit CI as a result of successful completion of the SQE Test sequence.

If a collision enforcement signal is received before the ced_window signal becomes inactive, the MAU shall interpret it as a collision enforcement and the timing of 11.3.4.5.3 shall apply.

11.3.4.6 Delay from circuit DO to circuit DI

The time delay from a bit on Circuit DO at the AU Interface to the corresponding bit on Circuit DI at the AU Interface is equal to the round trip delay of the MAU connected back-to-back with itself (that is, in RF loop-back) plus the round trip delay through the cable system at the location of the MAU. Therefore, the delay is a function of the location of the MAU on the cable system. It is never less than the transmitter delay plus the postamble length plus the time to detect loss of carrier or presence of the SQE Test signal. See Figure 11–16 for the timing relationship when the cable has zero length.

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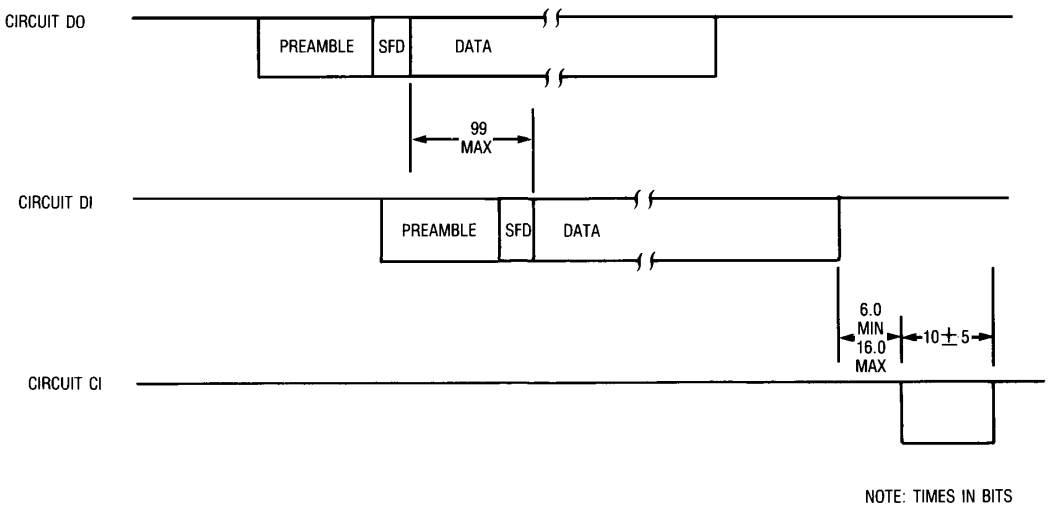

Figure 11–16—Timing at AUI for zero-length coax

When the MAU is transmitting a short packet (less than 576 bits), the timing for Circuit CI during the SQE Test sequence shall be the same as it is for normal length packets. If the MAU transmits a short packet (less than 576 bits) that encounters a collision and if the SQE Test sequence has not been transmitted when the collision is detected by the MAU, then the timing for Circuit CI shall be the same as it is for any normal collision.

11.3.4.7 Interpacket gap requirement

The MAU shall be able and ready to transmit data presented to it by the DTE no later than 90 bit times after the last bit of a received packet was presented by the MAU at its AUI.

11.3.4.8 Bit error ratio

The MAU shall have a Bit Error Ratio (BER) as measured at the AUI lower than one error in 10^8 in a "zero-length coax" test environment (that is, a coaxial cable connection sufficiently short to have negligible delay and transmission impairments). It shall have this BER for receive signal levels in the range specified in 11.3.1.1.3 and in the presence of –28.3 dBmV rms/14 MHz white Gaussian noise. This represents a 24.3 dB signal-to-noise ratio for the specified minimum signal level, –4 dBmV rms. For the same BER in a "system" environment (as opposed to zero-length coax), a 26 dB signal-to-noise ratio is required.

The MAU shall meet the BER requirements specified above when receiving strings of up to 33 consecutive identical bits.

11.3.5 Reliability

Component failures within the MAU electronics should not impede communication among other MAUs on the broadband coaxial cable. Connectors and other passive components comprising the means of connecting the MAU to the coaxial cable shall be designed to minimize the probability of total network failure. The MAU shall be designed to provide an MTBF of at least 1 000 000 hours without causing communication failure among other stations attached to the broadband local network medium.

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11.4 System considerations

11.4.1 Delay budget and network diameter

The delay budget for the broadband MAU and rest of the Physical Layer is tabulated in Table 11–3. This table includes allocations for trunk cables (the backbone cables in the system), drop cables (a length of 25 m is assumed), etc. The velocities of propagation assumed are included in the table; use of other types of cables will alter the system diameter accordingly. The types of cables, including the mix of drop and trunk cable lengths, can be altered as long as the total propagation delay from the most distant MAU to the headend does not exceed 70 bit times. The total delay budget of 576 bit times includes allowance for the preamble and SFD (64 bits).

Table 11–3 tabulates delay allocations for a dual-cable system with no headend delay. In translated single-cable systems, the headend translator delay reduces the maximum trunk cable distance by $[D/(2 \times CV)]$, where D is the delay in nanoseconds, and CV is the cable velocity in nanoseconds per meter. For 3.83 ns/m velocity trunk cable, this reduction is [Delay (ns) / 7.66] m.

Table 11–3—Broadband dual-cable systems—Physical Layer delay budget

Delay element	Maximum allowed value (bits)
DTE1 starts to put out first bit	0.00
First bit from DTE1 at AUI	3.00
AUI cable (50 m at 5.13 ns/m)	2.57
Circuit DO to Tx RF out	24.00
Tx drop cable (25 m at 4.27 ns/m)	1.05
Tx trunk cable (1800 m at 3.83 ns/m)	68.95
Rx trunk cable (25 m at 4.27 ns/m)	68.95
Rx drop cable (25 m at 4.27 ns/m)	1.05
End of bit comparison (last bit of source address)	160.00
Rx RF to collision enforcement RF out (from RX bit that is found to be in error to collision enforcement out)	34.00
Tx drop cable (25 m at 4.27 ns/m)	1.05
Tx trunk cable (1800 m at 3.83 ns/m)	68.95
Rx trunk cable (1800 m at 3.83 ns/m)	68.95
Rx drop cable (25 m at 4.27 ns/m)	1.05
Rx collision enforcement to circuit Ci	31.00
AUI cable (50 m at 5.13 ns/m)	2.57
DTE1 detects collision presence	3.00
DTE1 jams channel	32.00
Allowance for traps, splitters, amplifiers, and margin	3.86
Total	576.00

11.4.2 MAU operation with packets shorter than 512 bits

The MAU transmits an SQE Test sequence onto the RF medium after every transmitted packet. If the frame plus preamble and SFD is less than the ced_window in length, a receiving MAU cannot distinguish the SQE

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Test signal from a collision enforcement signal due to a collision. Therefore, operation of the MAU with data frames shorter than 512 bits may cause all other receiving MAUs to see a collision. The transmitting MAU, however, recognizes the SQE Test because that MAU was the one that transmitted the test. An MAU transmitting a short packet that encounters a collision can distinguish the resulting collision enforcement from an SQE Test signal by the fact that the transmitting MAU will not have transmitted the SQE Test sequence unless the packet is shorter than the round trip delay on the cable plant. In the latter instance, the transmitting MAU may not detect a collision enforcement.

11.5 Characteristics of the coaxial cable system

The cable system upon which the broadband MAU operates shall meet the following electrical and mechanical requirements.

11.5.1 Electrical requirements

The electrical requirements of the cable system are listed in Table 11–4. Each parameter is applicable over the frequency range to be used by the broadband MAU.

Table 11–4—Cable system electrical requirements

Impedance	75 Ω
Return loss	14 dB min
Transmit level	+50 dBmV ±2 dB
Receive level	+6 dBmV ±10 dB
Maximum receive noise level	–30 dBmV/14 MHz
Loss variation[a] (per 18 MHz band)	2 dB min, 52 dB max
Path loss (between any transmit port and receive port, including loss variation)	36 dB min, 52 dB max
Group delay variation —around data carrier —over 18 MHz band	 20 ns/10 MHz max 34 ns max

[a]Not including headend.

Adjacent channel signal levels shall be consistent with the requirements of 11.3.1.1.4.

11.5.2 Mechanical requirements

The connection of the cable system to the broadband MAU is via a standard F-series screw-on male connector. For the dual-cable case, two such connectors are required: one for transmit and the other for receive.

11.5.3 Delay requirements

The maximum length of the cable system is constrained by the allowable round trip delay from the farthest transmitting MAU to the farthest receiving MAU. Table 11–3 allows 140 bit times round trip delay in the cable system. For trunk cable propagation velocity of 3.83 ns/m, this allows 3600 m of trunk cable (round trip; 1800 m from the farthest point to the headend), and 25 m of 4.27 ns/m velocity drop cable at each MAU. In addition, 50 m of AUI cable is allowed on each MAU, therefore allowing, in this case, a maximum

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of 3750 m DTE to DTE separation. These lengths will be different if cables of different propagation velocity are used. This is acceptable so long as the maximum delay is not exceeded.

For single-cable systems, the maximum delay of 140 bit times includes the delay through the headend. The maximum cable system length has to be reduced appropriately, as described in 11.4.1.

11.6 Frequency translator requirements for the single-cable version

11.6.1 Electrical requirements

The headend frequency translator performance is included in the cable system characteristics specified in 11.5, except as defined in Table 11–5.

Table 11–5—Frequency translator requirements

Group delay variation —around data carrier frequency —between data carrier and CE center frequency	 20 ns/10 MHz max 50 ns max
Amplitude variation (from 6 MHz below the input data carrier frequency to 1 MHz above the CE center frequency)	2 dB max
Translation frequency	per Table 11–1

The frequency translator contributes to total cable system delay and shall be labeled by the vendor with the input-to-output delay in the band of operation. The effect on network length can then be computed per 11.4.1.

11.6.2 Mechanical requirements

The input and output mechanical interface shall be 75 Ω female F-series coaxial connectors. The connection to the broadband medium shall be through a coaxial cable with a mating male F-series connector.

11.7 Environmental specifications

11.7.1 Safety requirements

This subclause sets forth a number of recommendations and guidelines related to safety concerns. This list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to assure compliance with the appropriate standards.

LAN cable systems, as described in this clause, are subject to at least four direct electrical safety hazards during their use, and designers of connecting equipment should be aware of these hazards. The hazards are as follows:

a) Direct contact between local network components and power or lighting circuits
b) Static charge buildup on local network cables and components
c) High-energy transients coupled onto the local network cabling system
d) Potential differences between safety grounds to which various network components are connected

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These electrical safety hazards, to which all similar cabling systems are subject, should be alleviated for a local network to perform properly. In addition to provisions for properly handling these faults in an operational system, special measures shall be taken to ensure that the intended safety features are not negated when attaching or detaching equipment from the LAN medium of an existing network.

Sound installation practice, as defined in applicable national and local codes and regulations, shall be followed in every instance in which such practice is applicable.

11.7.2 Electromagnetic environment

11.7.2.1 Susceptibility levels

Sources of interference from the environment include electromagnetic fields, electrostatic discharge, transient voltages between earth connections, etc.

The physical MAU hardware shall meet its specifications when operating in an ambient plane wave field of:

a) 2 V/m from 10 kHz through 30 MHz
b) 5 V/m from 30 MHz through 1 GHz

MAUs meeting this clause should provide adequate RF ground return to satisfy the EMC specification.

11.7.2.2 Emission levels

The physical MAU hardware shall comply with the applicable national and local regulations for emission levels.

11.7.3 Temperature and humidity

The MAU and associated cable system are expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling such as shock and vibration. Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

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12. Physical signaling, medium attachment, and baseband medium specifications, type 1BASE5

NOTE—This MAU is not recommended for new installations. Since September 2003, maintenance changes are no longer being considered for this clause.

12.1 Introduction

12.1.1 Overview

1BASE5 is a 1 Mb/s CSMA/CD network based on twisted-pair wiring. Each DTE (Data Terminal Equipment) is star-connected to a shared hub through two pairs that function as transmit and receive channels. Hubs can be cascaded, and DTEs can be connected to any hub. Packets transmitted by a DTE are propagated by the hub to a higher-level hub if one exists; otherwise the hub broadcasts the packet back down to all DTEs and lower-level hubs. Packets received by a hub from a higher-level hub are retransmitted to all attached DTEs and lower-level hubs. If two or more DTEs or lower-level hubs transmit concurrently, the hub generates a collision-presence signal that the DTEs detect as a collision. Hubs between a transmitting DTE and the header (highest level) hub propagate data or the collision-presence signal to the header hub; this hub in turn broadcasts the packet or collision signal to all DTEs and lower-level hubs.

12.1.2 Scope

The 1BASE5 specification builds upon the first six major clauses of this standard; the remaining major clauses (other than this one, of course) do not apply to 1BASE5. That is, the Media Access Control (MAC) and Physical Signaling (PLS) Service Specifications are used in common with the other implementations of this standard, but the Physical Medium Attachment (PMA) sublayer, transmission medium, and hub functions for type 1BASE5 are specified in this clause. The relationship of the 1BASE5 specification to the OSI reference model and the IEEE 802.3 CSMA/CD LAN model is shown in Figure 12–1.

12.1.3 Definitions

See 1.4.

12.1.4 General characteristics

Type 1BASE5 has the following general characteristics:

a) 1 Mb/s signaling rate, Manchester encoded
b) Twisted-pair wiring
c) Point-to-point interconnection of DTEs to hubs, with one twisted-pair serving as the upward link, the other as the downward link
d) Data pairs can coexist in the same telephone cable bundles as voice pairs
e) When a hub receives signals from a DTE or lower-level hub, it propagates them to a higher-level hub if one exists; otherwise, the hub broadcasts the signals back down to the DTEs and lower-level hubs
f) When a hub receives signals concurrently from two or more DTEs or lower-level hubs, it generates a unique collision presence signal, and distributes it as in item e) above
g) DTE-to-hub and hub-to-hub interfaces are electrically isolated at both ends
h) Up to five hub levels are allowed
i) Hubs serve as repeaters
j) Maximum DTE-to-hub and hub-to-hub distance is approximately 250 m for telephone wiring (cable-type dependent; see 12.7)

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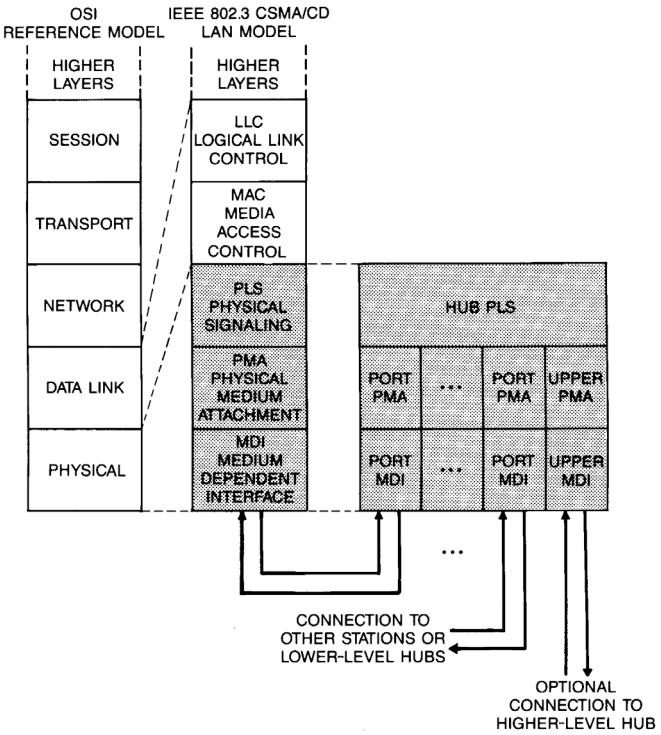

Figure 12–1—1BASE5 relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

k) Special links may be used to extend some DTE-to-hub or hub-to-hub distances to 4 km

12.1.5 Compatibility

This specification calls out one principal compatibility interface, namely PMA-to-Medium. It is intended that different implementations of DTEs and hubs be able to interoperate in 1BASE5 networks.

12.1.6 Objectives of type 1BASE5 specification

a) Provide for low-cost networks, as related to both equipment and cabling
b) Make it possible to use telephone-type building wiring, and in particular spare wiring when available
c) Provide for easy installability, reconfigurability, and service
d) Ensure interconnectability of independently developed DTEs and hubs
e) Ensure fairness of DTE access
f) Provide a communication channel with a resultant mean bit error ratio, at the Physical Layer service interface, of less than one part in 10^8 (on the order of one part in 10^9 at the link level)

12.2 Architecture

12.2.1 Major concepts

Type 1BASE5 is a 1 Mb/s CSMA/CD network. DTEs are connected to hubs (and hubs to other hubs) by point-to-point wiring, resulting in a star topology network. Data transmissions are Manchester encoded.

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An elementary configuration is illustrated in Figure 12–2. In this instance, each DTE is connected to the hub via separate transmit and receive channels (normally two twisted pairs). The hub serves as the point of concentration and performs two major functions: signal regeneration/retiming (repeating) and collision detection. When only one DTE transmits, the hub repeats the signals, compensating for amplitude and phase distortion, and broadcasts to all DTEs. When a hub detects two or more DTEs transmitting concurrently, the hub generates a unique Collision Presence (CP) signal, which it broadcasts instead of the originally transmitted signals. The hub continues to send CP until it receives IDL from all lower-level DTEs. CP has the property that it can be detected by DTEs as a Manchester code violation.

The interconnection architecture does not imply any minimum, typical, or maximum number of DTEs to be connected to a given hub; this is an implementation or installation detail.

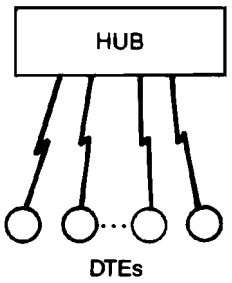

Figure 12–2—Single hub network

Up to five levels of hubs may be cascaded. A two-level configuration is illustrated in Figure 12–3, with a header hub (HH) and intermediate hubs (IH). There can be a number of IHs; there has to be one and only one HH. Each DTE or IH is connected to a hub via separate transmit and receive channels (normally two twisted pairs). An IH propagates signals from its DTEs toward the HH; it sends CP toward the HH in the event of a collision. The HH repeats the signals it receives from DTEs or IHs back down to all DTEs and IHs. The HH generates CP if more than one of its inputs becomes active. The IHs repeat the signals received from the HH, and broadcast to all the connected DTEs' receivers. Hubs do not distinguish whether input signals along the upward path emanate from DTEs or lower-level IHs. If a single input is active, the hub repeats the signal regardless of its source; if more than one is active, it generates CP.

A configuration involving four hub levels and a special link is illustrated in Figure 12–4. In this example, one IH is used for simple repeating (one connection upward and one connection downward). Other than having one link in and one link out, repeaters are identical to other hubs. Special links are connections, possibly containing active devices, that are used for situations requiring extra propagation delay or special transmission media.

12.2.2 Application perspective

The primary application area for type 1BASE5 is expected to be in office environments for networking DTEs such as personal computers or other workstations. In many cases, spare wiring contained in existing telephone wire bundles will be used.

12.2.3 Packet structure

Packets are transmitted from the PLS to the PMA as follows:

<silence> <preamble> <sfd> <data> <etd> <silence>

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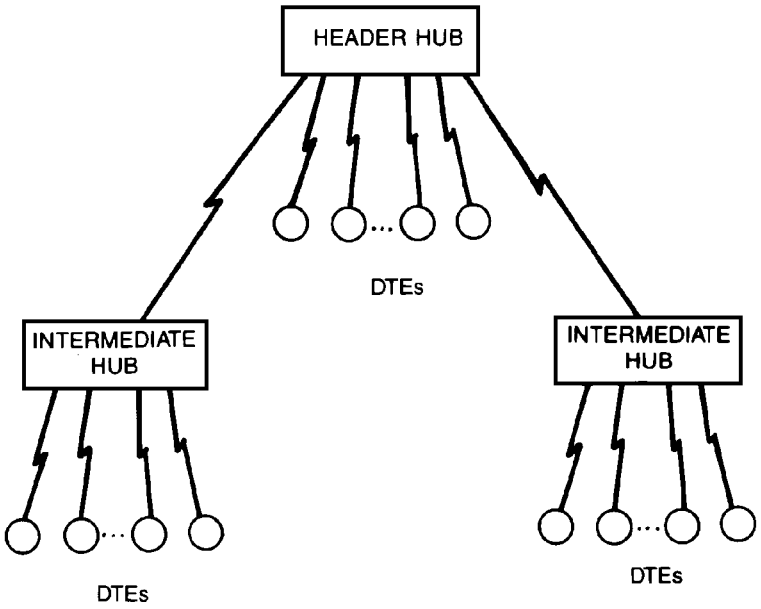

Figure 12–3—Network with two levels of hubs

The packet elements shall have the following characteristics:

Element	Characteristics
<silence>	No transitions
<preamble>	Alternating CD1 and CD0 for ≥56 bit times (ending in CD0)
<sfd>	CD1 CD0 CD1 CD0 CD1 CD0 CD1 CD1
<data>	8 × N instances of CD0 or CD1
<etd>	First part of IDL

12.2.3.1 Silence

The <silence> delimiter provides an observation window for an unspecified period of time during which no transitions occur. The minimum duration of <etd> followed by <silence> is the interFrameGap defined in 4.4.2.

12.2.3.2 Preamble

The <preamble> delimiter begins a packet transmission and provides a signal for receiver synchronization. The signal shall be an alternating pattern of CD1 and CD0. This pattern shall be transmitted by the DTE for a minimum of 56 bit times at the beginning of each packet. The last bit of the preamble (that is, the final bit of preamble before the start-of-frame delimiter) shall be a CD0.

The DTE is required to supply at least 56 bits of preamble in order to satisfy system requirements. System components consume preamble bits in order to perform their functions. The number of preamble bits sourced ensures an adequate number of bits are provided to each system component to correctly implement its function.

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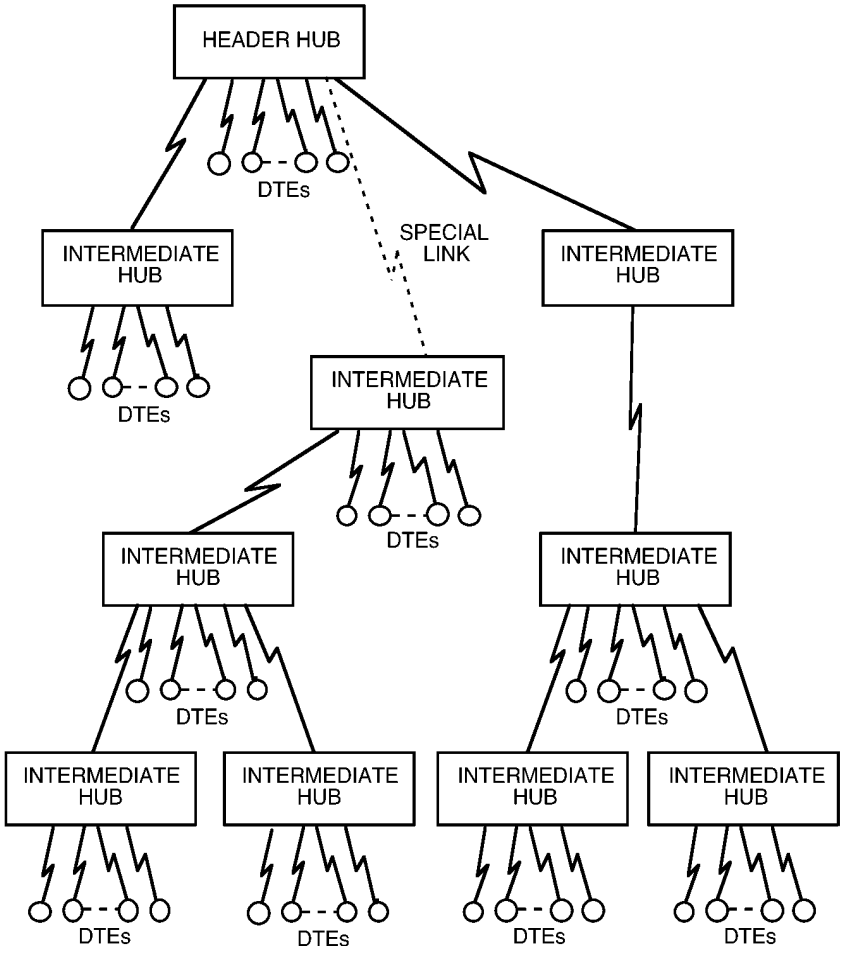

Figure 12–4—Network with four levels of hubs

12.2.3.3 Start-of-frame delimiter

The <sfd> indicates the start of a frame, and follows the preamble.

12.2.3.4 Data

The <data> in a transmission shall be in multiples of eight (8) encoded data bits (CD0s and CD1s).

12.2.3.5 End-of-transmission delimiter

The <etd> indicates the end of a transmission and serves to turn off the transmitter. The signal shall be the first part of an IDL.

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12.3 DTE physical signaling (PLS) specification

12.3.1 Overview

This subclause defines logical characteristics of the DTE PLS sublayer for IBASE5. The relationship of this specification to the entire standard is shown in Figure 12–5. The sublayer and its relationship to the MAC and PMA sublayers are described in an abstract way and do not imply any particular implementation.

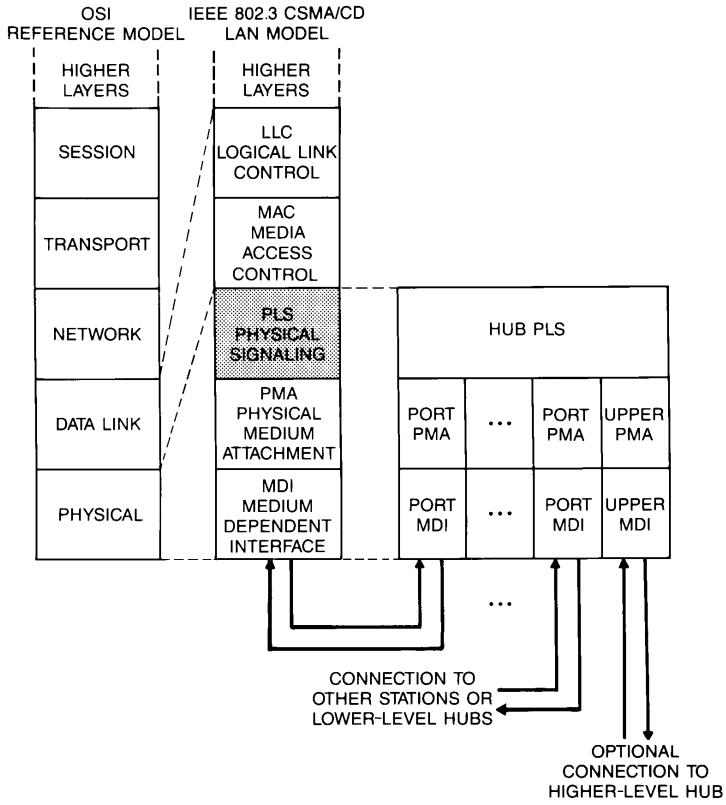

Figure 12–5—Station physical signaling, relationship to the ISO OSI reference model and the IEEE 802.3 CSMA/CD LAN model

12.3.1.1 Summary of major concepts

a) There are two channels between the PLS and PMA sublayers. Output data are passed through the output channel and input data and control (CP) are passed through the input channel.
b) Each direction of data transfer through the PLS operates independently and simultaneously (that is, the PLS is full duplex).

12.3.1.2 Application perspective

The DTE PLS sublayer performs the following functions:

a) Encodes OUTPUT_UNITs from the MAC sublayer into a Manchester encoded waveform that it sends to the PMA sublayer output circuit
b) Decodes a Manchester encoded waveform from the PMA sublayer input circuit into INPUT_ UNITS, CARRIER_STATUS, and SIGNAL_STATUS

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12.3.2 Functional specification

This subclause provides a detailed model for the DTE PLS sublayer.

Many of the terms used in this subclause are specific to the interface between this sublayer and the MAC sublayer. These terms are defined in the service specification for the PLS sublayer (see 6.3).

12.3.2.1 PLS-PMA interface

The PLS and PMA communicate by means of the following messages:

Message	Meaning	Source
output	Output information	PLS
output_idle	No data to be output	PLS
input	Input information	PMA
input_idle	No input information	PMA

12.3.2.1.1 *output* message

The PLS sublayer sends an *output* message to the PMA sublayer when the PLS sublayer receives an OUTPUT_UNIT from the MAC sublayer.

The physical realization of the *output* message is a CD0 or a CD1 sent by the PLS to the PMA. The PLS sends a CD0 if the OUTPUT_UNIT is a ZERO or a CD1 if the OUTPUT_UNIT is a ONE. This message is time-coded. That is, once this message has been sent, the function is not completed until one bit time later. The *output* message cannot be sent again until the bit cell being sent as a result of sending the previous *output* message is complete.

12.3.2.1.2 *output_idle* message

The PLS sublayer sends an *output_idle* message to the PMA sublayer at all times when the MAC sublayer is not in the process of transferring output data across the MAC to PLS interface. The *output_idle* message is no longer sent (and the first OUTPUT_UNIT is sent using the *output* message) when the first OUTPUT_UNIT of a packet is received from the MAC sublayer. The *output_idle* message is again sent to the PMA when DATA_COMPLETE is received from the MAC sublayer.

The physical realization of the *output_idle* message is IDL sent by the PLS to the PMA.

12.3.2.1.3 *input* message

The PMA sublayer sends an *input* message to the PLS sublayer when the PMA has received a bit from the medium and is prepared to transfer this bit to the PLS.

The physical realization of the *input* message consists of data units, CD0, CD1, CVL, or CVH, derived from the incoming data stream. If ambiguity exists due to excessive noise or jitter, the PMA may send an arbitrary combination of these.

12.3.2.1.4 *input_idle* message

The PMA sublayer sends an *input_idle* message to the PLS sublayer when the PMA sublayer does not have data to send to the PLS sublayer. This condition exists when carrier is lost or IDL is received.

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12.3.2.2 PLS-MAC interface

The PLS and MAC communicate by means of the following messages:

Message	Meaning	Source
OUTPUT_UNIT	Data sent to the PMA	MAC
OUTPUT_STATUS	Response to OUTPUT_UNIT	PLS
INPUT_UNIT	Data received from the PMA	PLS
CARRIER_STATUS	Indication of input activity	PLS
SIGNAL_STATUS	Indication of error/no error condition	PLS

12.3.2.2.1 OUTPUT_UNIT

The MAC sublayer sends the PLS sublayer an OUTPUT_UNIT every time the MAC sublayer has a bit to send. Once the MAC sublayer has sent an OUTPUT_UNIT to the PLS sublayer, it may not send another OUTPUT_UNIT until it has received an OUTPUT_STATUS message from the PLS sublayer. The OUTPUT_ UNIT is a ONE if the MAC sublayer wants the PLS sublayer to send a CD1 to the PMA sublayer, a ZERO if a CD0 is desired, or a DATA_COMPLETE if an IDL is desired.

12.3.2.2.2 OUTPUT_STATUS

The PLS sublayer sends the MAC sublayer an OUTPUT_STATUS in response to every OUTPUT_UNIT received by the PLS sublayer. OUTPUT_STATUS sent is an OUTPUT_NEXT when the PLS sublayer is ready to accept the next OUTPUT_UNIT from the MAC sublayer. (The purpose of OUTPUT_STATUS is to synchronize the MAC sublayer data output with the data rate of the physical medium.)

12.3.2.2.3 INPUT_UNIT

The PLS sublayer sends the MAC sublayer an INPUT_UNIT every time the PLS receives an *input* message from the PMA sublayer. The INPUT_UNIT is a ONE if the PLS sublayer receives a CD1 from the PMA sublayer or a ZERO if the PLS sublayer receives a CD0 from the PMA sublayer. The INPUT_UNIT may be either ZERO or ONE if the PLS sublayer receives a CVL or CVH from the PMA sublayer.

12.3.2.2.4 CARRIER_STATUS

The PLS sublayer sends the MAC sublayer_CARRIER_STATUS whenever there is a change in carrier status, as detected by the PMA. The PLS sublayer sends CARRIER_ON when it receives an *input* message from the PMA and the previous CARRIER_STATUS that the PLS sublayer sent to the MAC sublayer was CARRIER_OFF. The PLS sublayer sends CARRIER_OFF when it receives an *input_idle* message from the PMA sublayer, and the previous CARRIER_STATUS that the PLS sublayer sent to the MAC sublayer was CARRIER_ON.

12.3.2.2.5 SIGNAL_STATUS

The PLS sublayer sends the MAC sublayer SIGNAL_STATUS whenever it detects the beginning or end of Collision Presence. The PLS sublayer sends SIGNAL_ERROR when it receives *input* message CVL or CVH from the PMA sublayer and the previous SIGNAL_STATUS the PLS sublayer sent was NO_SIGNAL_ERROR. The PLS sublayer sends NO_SIGNAL_ERROR when it receives an *input_idle* message from the PMA sublayer and the previous SIGNAL_STATUS that the PLS sent to the MAC sublayer was SIGNAL_ERROR. The PLS shall send SIGNAL_ERROR to the MAC sublayer when the

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Collision Presence pattern is detected; it may send SIGNAL_ERROR any time it receives an *input* message that is neither CD0 nor CD1.

12.3.2.3 PLS functions

The PLS sublayer functions consist of four simultaneous and asynchronous functions. These functions are Output, Input, Error Sense, and Carrier Sense. All of the four functions are started immediately following PowerOn. These functions are depicted in the state diagrams shown in Figure 12–6 through Figure 12–9, using the notation described in 1.2.1.

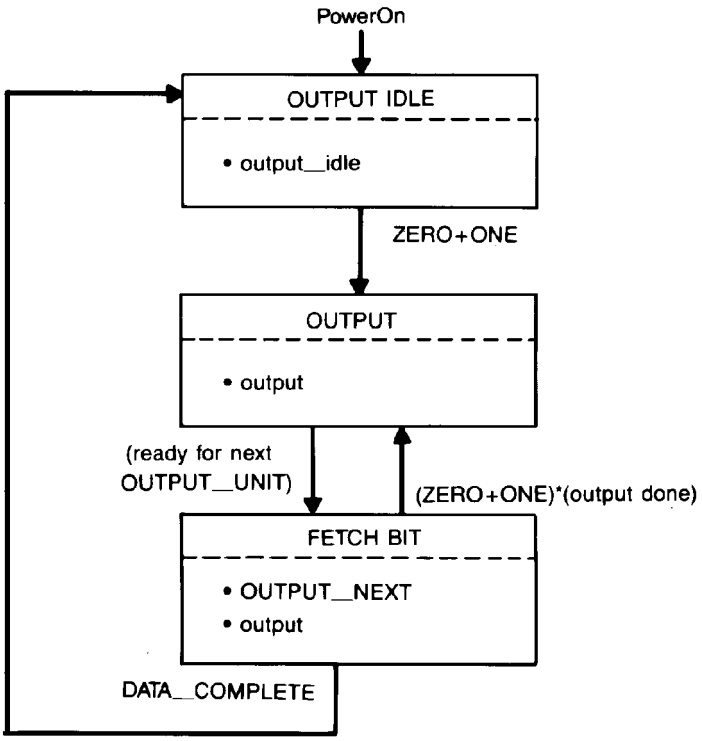

Figure 12–6—DTE PLS Output function

12.3.2.3.1 State diagram variables

The variables used in the state diagrams and the corresponding descriptions are the following:

a) Inter Process Flags

disable_SIGNAL_ERRORUsed in the state diagrams and functions. It is used by the Input function to prevent false collision detection by the Error Sense function during preamble startup.

protectTimer Used by the Carrier Sense function to implement the protection period described in 12.5.3.2.3. It is started by "start-protectTimer." "protectTimer_done" is satisfied when the timer has expired.

12.3.2.3.2 Output function

The Output function transparently performs the task of data transfer from the MAC sublayer to the PMA sublayer. The state diagram of Figure 12–6 depicts the Output function operation.

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12.3.2.3.3 Input function

The Input function transparently performs the task of data transfer from the PMA sublayer to the MAC sublayer. The state diagram of Figure 12–7 depicts the Input function operation.

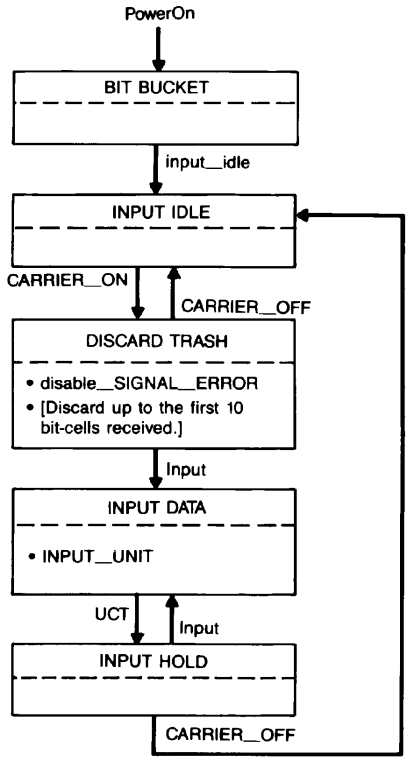

Figure 12–7—DTE PLS Input function

12.3.2.3.4 Error Sense function

The Error Sense function performs the task of sending SIGNAL_STATUS to the MAC sublayer at the beginning and end of the Collision Presence pattern. The state diagram of Figure 12–8 depicts the Error Sense function operation.

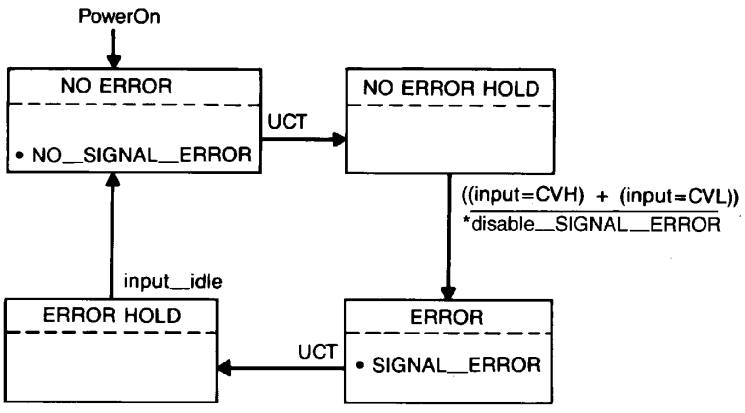

Figure 12–8—DTE PLS Error Sense function

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12.3.2.3.5 Carrier Sense function

The Carrier Sense function performs the task of sending CARRIER_STATUS to the MAC sublayer whenever the input becomes active or idle, as detected by the PMA sublayer. The state diagram of Figure 12–9 depicts the Carrier Sense function operation.

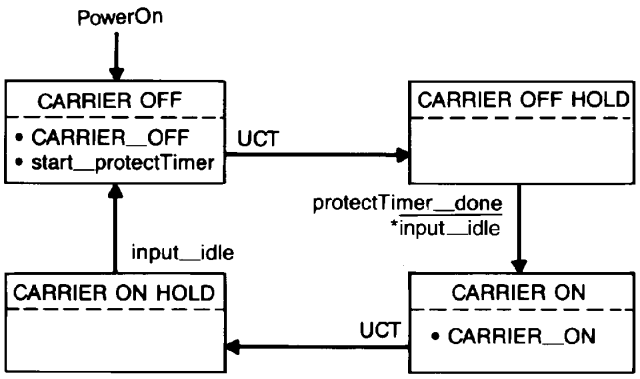

Figure 12–9—DTE PLS Carrier Sense function

A timer may be used by the Carrier Sense function to implement the protection period described in 12.5.3.2.3. It is started by "start-protectTimer" and asserts "protectTimer_done" after 0 to 30 μs since starting.

12.3.2.4 Signal encoding

Five distinct symbols can be transmitted on the line: CD0, CD1, CVL, CVH, and IDL. Of these, CVL and CVH are transmitted only as part of the collision presence reporting pattern CP.

12.3.2.4.1 Data transmission rate

The data transmission rate (BR) is 1 Mb/s ± 0.01%. A bit time (BT) is therefore nominally 1 μs.

12.3.2.4.2 Data symbol encoding

Manchester encoding is used for the transmission of packets. Manchester encoding is a binary signaling mechanism that combines data and clock into bit cells. Each bit cell is split into two halves with the second half containing the binary inverse of the first half; a transition always occurs in the middle of each bit cell. During the first half of the bit cell, the encoded signal is the logical complement of the bit value being encoded. During the second half of the bit cell, the encoded signal is the uncomplemented value of the bit being encoded. Thus, a CD0 is encoded as a bit cell in which the first half is HI and the second half is LO. A CD1 is encoded as a bit cell in which the first half is LO and the second half is HI. Examples of Manchester waveforms are shown in Figure 12–10. The zero crossings of an ideal Manchester waveform occur on precise half-bit-cell boundaries. The zero crossings of real waveforms may include timing jitter that causes deviation from these "idealized zero crossings."

12.3.2.4.3 Collision presence encoding

Two signals, CVL and CVH, that are transmitted only as part of the collision presence reporting pattern, CP, violate the normal Manchester encoding rule requiring a transition in the middle of each symbol. A CVH is encoded as a transition from LO to HI at the beginning of the bit cell, HI for the entire bit cell, and transition

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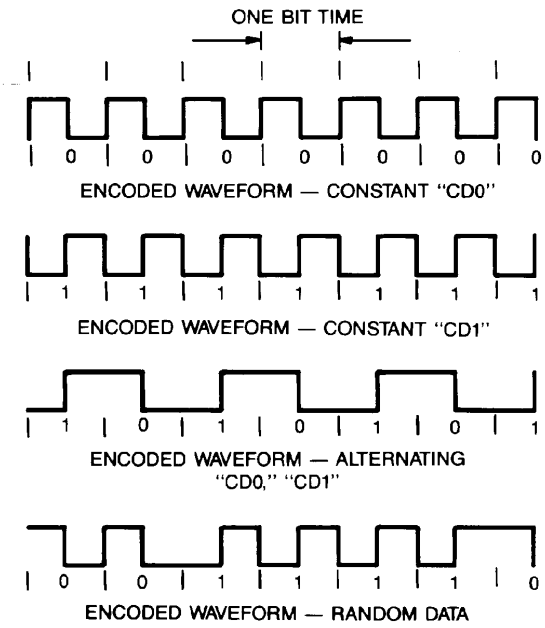

Figure 12–10—Examples of Manchester waveforms

from HI to LO at the end of the bit cell. A CVL is encoded as a transition from HI to LO at the beginning of the bit cell, LO for the entire bit cell, and transition from LO to HI at the end of the bit cell.

The Collision Presence reporting signal, CP, is a special sequence that differs from any legitimate Manchester-encoded signal. CP is encoded as a repeating sequence of 1 bit time LO, 1/2 bit time HI, 1 bit time LO, 1 bit time HI, 1/2 bit time LO, and 1 bit time HI. This may also be interpreted as repetitions of the five-symbol sequence CVL, CD0, CD1, CD0, CVH. Should a transmitter's or receiver's timing be shifted by 1/2 bit time, then the same sequence will be interpretable as repetitions of CD1, CVL, CVH, CD1, CD0. In either case, the presence of non-Manchester symbols distinguishes the sequence from data. Examples of Collision Presence waveforms are shown in Figure 12–11. See 12.3.2.2.5 and 12.4.3.2 for further details on the detection and generation of CP.

NOTE—CP is the minimal length sequence that meets the following design criteria:

a) The sequence should not look like legitimate Manchester-encoded data even if the receiver does not lock onto the correct bit-cell boundaries.
b) The sequence should maintain overall dc balance. That is, it should be HI 50% of the time and LO the other 50%.
c) The signal should occupy the same part of the frequency spectrum as normal data. That is, transitions should occur every half or whole bit time so that the fundamental signaling frequencies of BR/2 and BR are maintained. Furthermore, allowing more than one bit time to pass without a transition would introduce ambiguity with the idle line condition (IDL).

12.3.2.4.4 Idle line encoding

The line condition IDL is also used as an encoded signal. An IDL always starts with a HI signal level. Since IDL always starts with a HI signal, an additional transition will be added to the data stream if the last bit sent was a zero. This transition cannot be confused with clocked data (CD0 or CD1) since the transition will occur at the start of a bit cell. There will be no transition in the middle of the bit cell. The HI signal level, as sent by a transmitter, shall be maintained for a minimum of 2 bit times.

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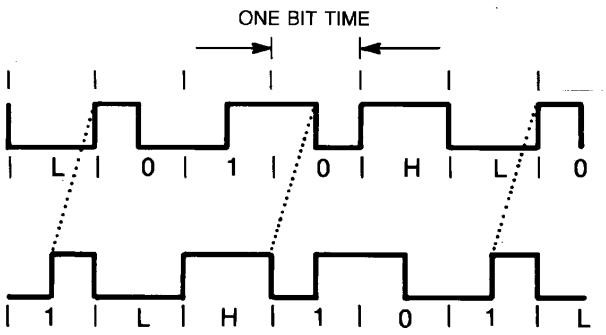

Figure 12–11—Examples of collision presence waveforms

12.4 Hub specification

12.4.1 Overview

This subclause defines the logical characteristics of the hub used in 1BASE5. The relationship of this specification to the entire standard is shown in Figure 12–12.

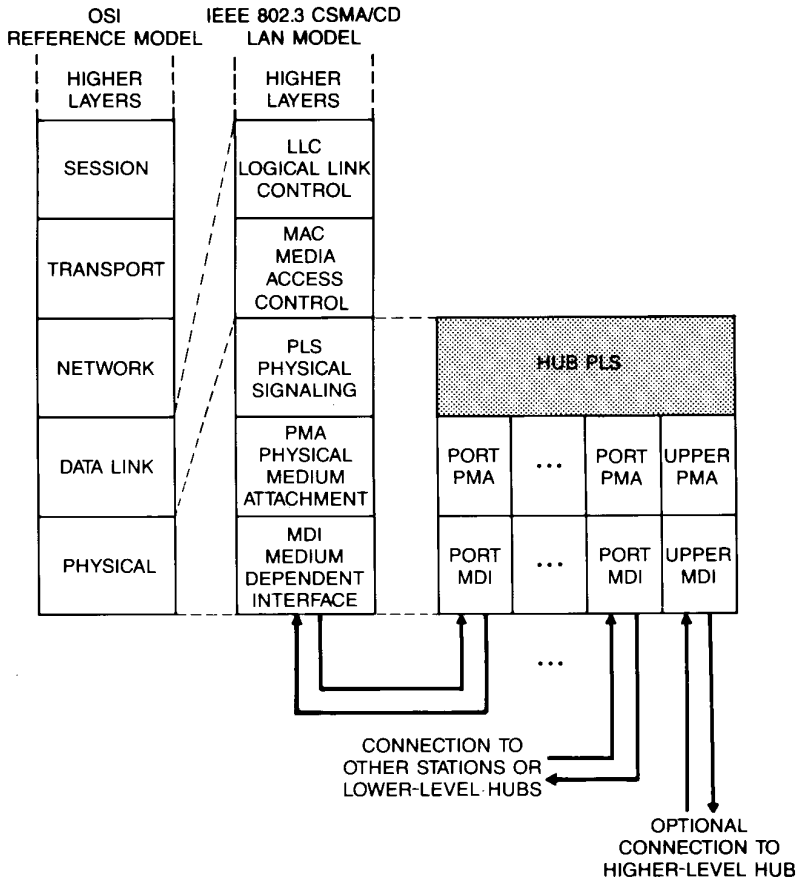

Figure 12–12—Hub relationship to the OSI reference model and the IEEE 802.3 CSMA/CD LAN model

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12.4.1.1 Summary of major concepts

a) A hub consists of a Hub PLS sublayer and a number of instances of the PMA sublayer.
b) One instance of the PMA sublayer, the "upper PMA," provides a connection to a higher-level hub. This PMA is not required for the header hub.
c) Each of the remaining instances of the PMA sublayer, called "port PMAs," provides a connection to a DTE or a lower-level hub.
d) The Hub PLS transfers data in two directions: upward from the port PMAs, to the upper PMA and downward from the upper PMA to the port PMAs.
e) The upward and downward "sides" of the hub operate independently and simultaneously.

12.4.1.2 Application perspective

The hub is a Physical Layer entity that performs two functions:

a) It retransmits incoming signals with amplitude and timing restored.
b) It detects collisions between any two or more ports and reports knowledge of the collision by transmitting a special collision presence reporting pattern.

12.4.2 Hub structure

Each hub is functionally divided into two parts: the upward side and the downward side. The upward side is responsible for combining the transmissions from DTEs and hubs lower in the network into a single transmission to the next level up. The downward side is responsible for distributing the combined signal (which is wrapped around from the upward side of the header hub) to each of the DTEs and hubs below. Except as specified in 12.4.3.2.3 and 12.4.3.2.6, the two sides function independently.

There is an upward input channel and a corresponding downward output channel for each DTE or hub immediately below the hub. Although there is no electrical connection between the two lines, they do share a connector and cable (see 12.6 and 12.7) and are collectively known as a hub port. Each port is accessed through an instance of the PMA sublayer referred to as a "port PMA."

The one output channel from the upward side and the one input channel to the downward side of a hub are similarly paired and, for all but the header hub, are connected to a port of the next-higher-level hub, They are accessed through an instance of the PMA sublayer referred to as the "upper PMA."

NOTE—A hub that includes n hub ports should be called an n-port hub, even though it may have an extra jack for the upper PMA. The latter connection should never be counted as a port, despite common engineering usage, because it does not meet the specific definition of a 1BASE5 hub port given above.

12.4.2.1 Upward side

The primary function of the upward side of a hub is to propagate signals from each of its inputs to its single output. If more than one input is active, then the Collision Presence signal CP is transmitted instead. In addition, the signals are retimed to restore the transitions to half-bit-time boundaries; see 12.4.3.2.5 for the details of retiming.

12.4.2.2 Downward side

The primary function of the downward side of a hub is to repeat signals from its one input to each of its outputs. In addition, the signals are retimed to restore the transitions to half-bit-time boundaries; see 12.4.3.2.5 for the details of retiming.

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12.4.3 Hub PLS functional specification

This subclause provides a detailed model for the Hub PLS sublayer.

12.4.3.1 Hub PLS to PMA interface

The interface between the Hub PLS and the PMA is the same as that specified in 12.3.2.1 for use between the DTE PLS and the PMA except that the *output* message from the Hub PLS to the PMA is used to transmit CVL and CVH in addition to CD0 and CD1.

12.4.3.2 Hub PLS functions

The Hub PLS sublayer functions consist of three asynchronous functions. These functions are Upward Transfer, Jabber, and Downward Transfer. All three functions are started immediately following PowerOn; an independent copy of the Jabber function is started for each port PMA. These functions are depicted in the state diagrams shown in Figure 12–13 through Figure 12–15, using the notation described in 1.2.1.

12.4.3.2.1 State diagram variables

The variables used in the state diagrams and the corresponding descriptions are the following:

a) *Port designators:* Instances of the PMA sublayer are referred to by index. PMA information is obtained by replacing the X in the desired function with the index of the PMA of interest. Furthermore, PMAs may be referenced by several special designators used as indices:

X Generic port PMA designator. When X is used in a state diagram its value indicates the particular instance of a generic function.

UPPERIndicates the upper PMA.

ALLPORTSIndicates that all port PMAs are to be considered. All port PMAs have to meet a test condition in order for that test to pass.

ALLENABLEDPORTSIndicates that all port PMAs that are not disabled by the Jabber function are to be considered. All such port PMAs have to meet a test condition in order for that test to pass.

ONEPORTIndicates that all port PMAs that are not disabled by the Jabber function are to be considered. One, but not more than one, such port PMA has to meet a test condition in order for that test to pass.

>ONEPORTIndicates that all port PMAs that are not disabled by the Jabber function are to be considered. Two or more such port PMAs have to meet a test condition in order for that test to pass.

N Defined by the PORT function on exiting from the UPWARD IDLE state of Figure 12–13. It indicates which port PMA caused the exit from the UPWARD IDLE state.

b) *Port functions*:

PORT(TestCondition)Returns the index of a port PMA passing the indicated test condition. If multiple port PMAs meet the test condition, the PORT function will return one and only one of the acceptable values.

c) *Input variables:*

INPUT(X) Indicates the state of activity on the designated PMA input channel. It may be either “idle” or “active.” The former indicates that *input_idle* is asserted; the latter indicates that it is not asserted.

input(X) Used to receive an *input* message (see 12.3.2.1) from the designated PMA input channel.

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probation_alternative Used to distinguish between the two allowed alternatives for exiting the JABBER JAM state of Figure 12–14 when an active port becomes idle. The implementer of a hub may treat the variable as either true or false.

d) *Output variables:*

output(X)Used to send an *output* message (see 12.3.2.1 and 12.4.3.1) to the designated PMA output channel.

output_idle(X)Used to send an *output_idle* message (see 12.3.2.1) on the designated PMA output channel.

e) *Inter process flags:*

send_collisionUsed by the Upward Signal Transfer function to indicate a series of *output* messages to the upper PMA sublayer, the effect of which is to transmit the CP signal, as described in 12.3.2.4.2, 12.3.2.4.3, and 12.4.3.2.7.

jabber_collisionUsed by the various instances of the Jabber function to signal the Upward Signal Transfer function that CP should be generated.

disable_input(X)Used to disable the designated PMA input channel. The input is re-enabled when disable-input(X) is no longer asserted. Only the Upward Signal Transfer function is affected by the disabling of a port (via the ALLENABLEDPORTS, ONEPORT, and >ONEPORT designators).

jabberTime1Used by the Jabber function (see 12.4.3.2.3) to detect excessively long transmissions. It is started by "start_jabberTime1." "jabberTime1_done" is satisfied when the timer has expired.

jabberTime2Used by the Jabber function (see 12.4.3.2.3) to determine when to disable ports due to excessively long transmissions. It is started by "start_jabberTime2." "jabberTime2_done" is satisfied when the timer has expired.

12.4.3.2.2 Upward Signal Transfer function

The Upward Signal Transfer function combines signals from the various port inputs and passes them on to the upper output. It also detects and reports collisions as appropriate. The state diagram of Figure 12–13 depicts its operation.

Signals are propagated upward according to the following rules, except as controlled by the Jabber function (see 12.4.3.2.3):

a) If IDL is present on all port inputs, then transmit IDL.
b) If IDL is present on all but one of the port inputs, then repeat the signal received from that one line. If that one signal is CP, then a hub may generate its own CP signal instead of repeating the received CP signal.
c) If two or more inputs are active (non-IDL) at the same time, then transmit CP and continue transmitting CP until all inputs indicate IDL again.

Whenever the hub finishes transmitting CP, it shall then transmit IDL, including the extended HI period.

12.4.3.2.3 Jabber function

The Jabber function detects abnormally long transmissions and takes appropriate action to abort them. The state diagram of Figure 12–14 depicts its operation.

Two timers are used by the Jabber function. They may be implemented either as local timers for each instance of the Jabber function or as global timers shared by all instances. Furthermore, because the two timers are always started concurrently, an implementation may share circuitry between the two.

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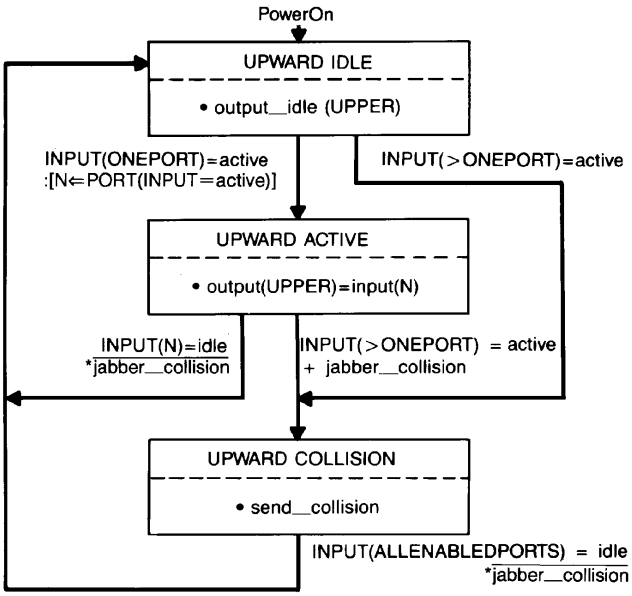

Figure 12–13—Hub PLS Upward Transfer function

The first timer is started by "start_jabberTime1" and asserts "jabberTime1_done" after 25 to 50 ms since starting. If implemented as a single global timer, assertion of start_jabberTime1 by any instance of the Jabber function with any other instance(s) still waiting for that timer shall not restart the timer, thereby shortening the waiting period for the latest instance.

Similarly, the second timer is started by "start_jabberTime2" and asserts "jabberTime2_done" after 51 to 100 ms since starting. If implemented as a single global timer, assertion of start_jabberTime2 by any instance of the Jabber function with any other instance(s) still waiting for that timer shall not restart the timer, thereby shortening the waiting period for the latest instance. Furthermore, if this second timer is implemented as a single global timer, then assertion of start_jabberTime1 by any instance of the Jabber function with any other instance(s) still waiting for just the second timer (in the JABBER JAM state) shall be treated as if the first timer expires immediately (asserting jabberTime1_done) for the latest instance, thereby causing that instance to join the other instance(s) waiting for the second timer.

Hardware within the upward side of a hub shall provide a window of 25 to 50 ms, during which time a normal packet or CP sequence may be propagated upward. If any port input (or, as an alternative implementation, the hub's combined upward signal) exceeds this duration without becoming idle, then the hub shall switch to transmitting CP until 51 to 100 ms after the beginning of the window and then, if that input is still active, disable that input (or all nonidle inputs) until it once again becomes active while the downward side is idle.

The "probation_alternative" input variable is used to distinguish between the two allowed alternatives for exiting the JABBER JAM state of Figure 12–14 when an active port becomes idle. The implementer of a hub may treat the variable as either true or false. If true, the port will enter the JABBER PROBATION state (via the JABBER SHUTOFF state); if false, the port will instead return to the JABBER IDLE state.

12.4.3.2.4 Downward Signal Transfer function

The Downward Signal Transfer function repeats signals from the upper input to the various port outputs. The state diagram of Figure 12–15 depicts its operation.

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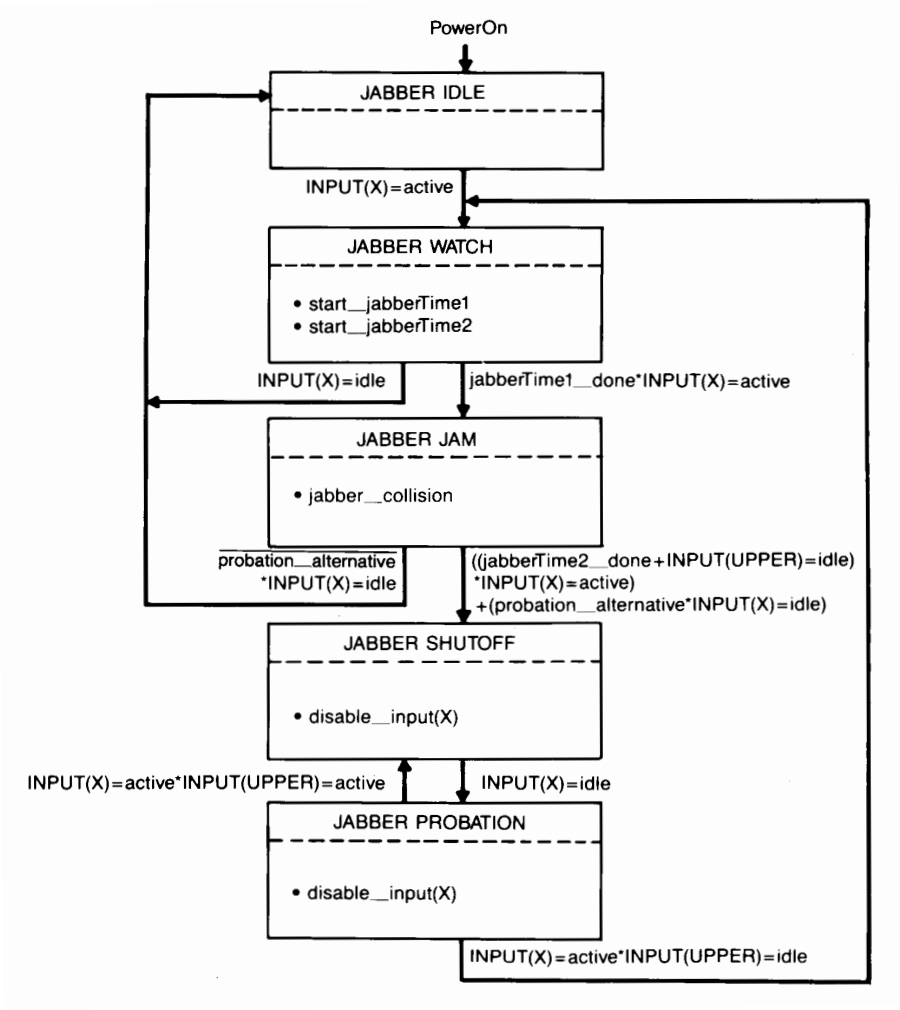

Figure 12–14—Hub PLS Jabber function for port X

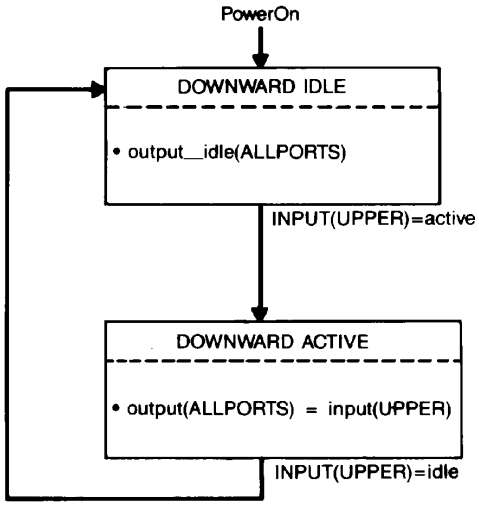

Figure 12–15—Hub PLS Downward Transfer function

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The downward side of a hub may detect the Collision Presence signal at the upper input and generate its own CP signal to be transmitted at the port outputs (in place of repeating the received CP signal).

Whenever the hub finishes transmitting CP, it shall then transmit IDL, including the extended HI period.

12.4.3.2.5 Retiming (jitter removal)

Each side of each hub shall retime any clocked signals that it propagates so that the transitions occur on half-bit-time boundaries, thereby avoiding accumulation of excessive jitter. Such retiming shall preserve the sequence of CD0, CD1, CVL, and CVH symbols being propagated.

If an ambiguity exists in the incoming bit cells due to excessive noise or jitter, than the appropriate side of the hub may either switch to generating CP or replace the erroneous bit cell with an arbitrary combination of half or whole bit cells.

Retiming also accounts for differences (if any) in clock rates between that used to send bit cells to the hub and that used to send them out from the hub. Excessive differences in clock rates (caused by clocks not meeting 12.3.2.4.1) and excessively long packets (caused by exceeding maxFrameSize) may each cause the capacity of the retiming function to be exceeded. In such circumstances, the appropriate side of the hub may either switch to transmitting CP or add or delete half or whole bit cells as needed.

Whenever bit cells are added, deleted, or replaced, the hub shall maintain synchronization of the outgoing bit cells to a half or whole bit cell boundary. Furthermore, it shall not generate periods of more than one bit time without a transition.

12.4.3.2.6 Header hub wrap-around

For each particular network configuration, one hub operates as the header hub and all others as intermediate hubs. It is suggested, but not required, that hub implementations be capable of being used for either purpose. Methods for switching between these two modes are beyond the scope of this standard.

For an intermediate hub, the upper output shall be connected to a port input of the next higher-level hub and the upper input shall be connected to a port output of a higher-level hub.

For the header hub, the upper output shall be connected to the upper input. This wraparound may appropriately bypass parts of the PMA specification so long as the resulting implementation is functionally equivalent to one with a wired connection. For example, signals internal to the hub need not be translated to the corresponding external levels and then translated back to internal levels. Similarly, it shall not be necessary to retime the wrapped signal twice, once in the upward side and then again in the downward side of the same header hub; a single retiming is permissible.

12.4.3.2.7 Collision presence startup

When a hub starts generating CP (as specified in 12.4.3.2.2 through 12.4.3.2.5) it shall synchronize the startup to a half or whole bit-cell boundary of any immediately preceding signal. If it was sending IDL immediately before the CP, no synchronization or preamble is required.

A hub may start transmission of CP at any point in the sequence that does not result in periods of more than one bit time without a transition during the switch from passing on data to sending CP. Depending on the preceding signal, it may start with L010H, 010HL, 10HL0, 0HL01, or HL010. Because startup may be synchronized to any half-bit-cell boundary, a hub may also transmit the shifted version of CP starting with 1LH10, LH101, H101L, 101LH, or 01LH1.

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12.4.3.3 Reliability

Hubs shall be designed to provide a mean time between failure (MTBF) of at least 45 000 hours of operation. Hubs, including the associated connectors and other passive components, should be designed to minimize the probability that, a particular failure results in total network failure. Furthermore, the port electronics of each hub should be designed so as to minimize the probability that the failure of one port prevents communication by equipment attached to the other ports.

12.5 Physical medium attachment (PMA) specification

12.5.1 Overview

This subclause defines the Physical Medium Attachment (PMA) sublayer for 1BASE5. The relationship of this specification to the entire International Standard is shown in Figure 12–16. The PMA sublayer connects the PLS sublayer to the Medium Dependent Interface (MDI).

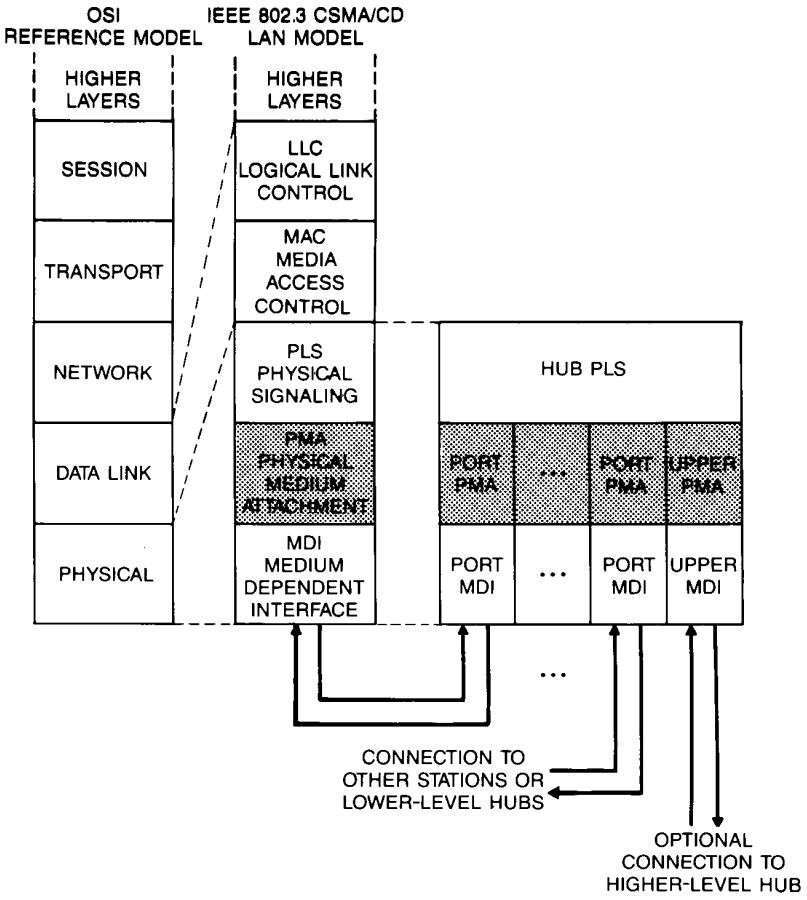

Figure 12–16—Physical medium attachment, relationship to the OSI reference model and the IEEE 802.3 CSMA/CD LAN model

12.5.2 PLS–PMA interface

The interface between the PLS and the PMA sublayers is specified in 12.3.2.1 for DTEs and in 12.4.3.1 for hubs.

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12.5.3 Signal characteristics

12.5.3.1 Transmitter characteristics

Transmitters should operate properly when loaded with any cable meeting the requirements of 12.7. To approximate the boundary conditions of such loading, two specific test loads are specified. Transmitters shall meet all requirements of this subclause when connected to both the "light" (115 Ω) load shown in Figure 12–17 and the "heavy" (approximately 80 Ω) load shown in Figure 12–18. It is expected that transmitters that perform correctly with these two loads will also perform acceptably under intermediate loading conditions.

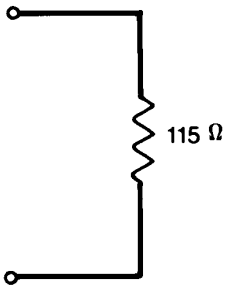

Figure 12–17—Simulated light load

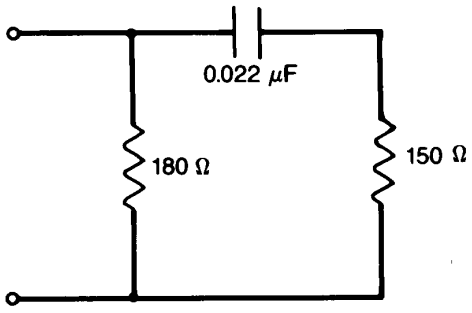

Figure 12–18—Simulated heavy load

12.5.3.1.1 Differential output voltage

For simplicity of explanation, the text and figures of this subclause describe the differential output voltage in terms of voltage magnitudes. The requirements of this subclause apply to the negative pulses as well as the positive ones.

Beginning with the second bit of the preamble (or CP, if no preamble is present), pulses of duration BT/2 shall meet the conditions of Figure 12–19. Pulses of duration BT shall meet the conditions of Figure 12–20. After the zero-crossing, the output shall exceed the voltage of a signal rising from the zero-crossing to 2.0 V with a slope of magnitude 20 mV/ns. The output shall remain above 2.0 V until 100 ns before the next, zero-crossing. The peak output voltage shall not exceed 3.65 V. While falling from 2.0 V to the zero-crossing, the signal shall exceed the voltage of a signal falling from 2.0 V to the zero-crossing with a slope of magnitude 20 mV/ns.

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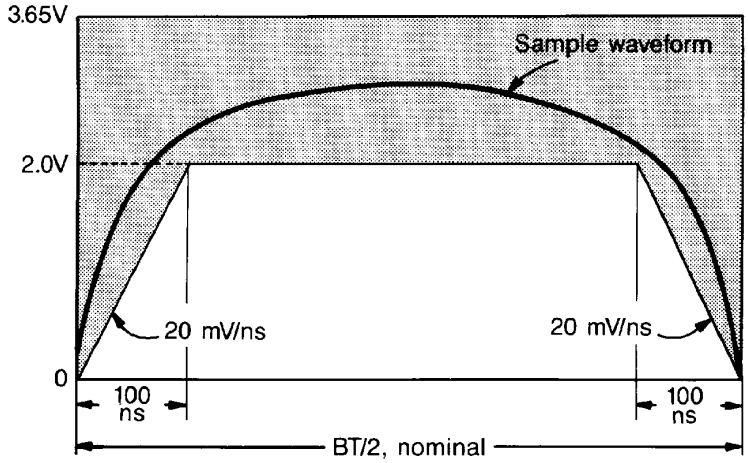

Figure 12–19—Differential output voltage, nominal duration BT/2

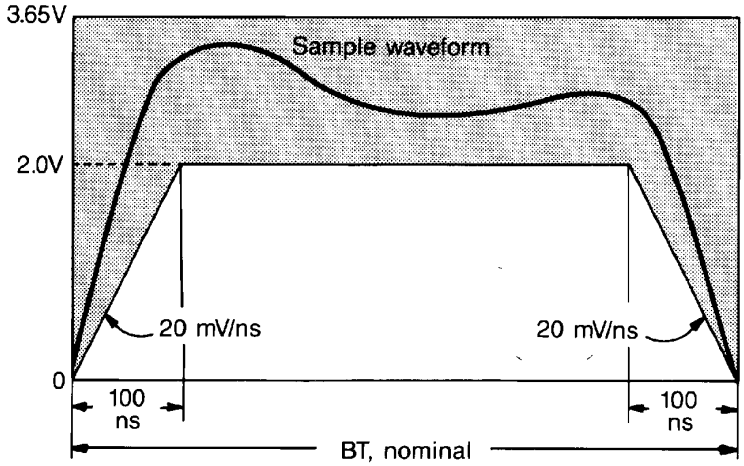

Figure 12–20—Differential output voltage, duration BT

For pulses of duration BT, the average voltage that appears from 100 ns after the zero-crossing through BT/2 shall be between 0.95 and 1.8 times the average voltage that appears from time BT/2 through 100 ns before the following zero-crossing. Similarly, for pulses of duration BT, the peak voltage that appears from 100 ns after the zero-crossing through BT/2 shall be between 0.95 and 1.8 times the peak voltage that appears from time BT/2 through 100 ns before the following zero-crossing.

NOTE—The purpose of the above restrictions on average and peak voltages is to avoid transmitter waveforms that peak excessively during the second half of signals of duration BT, resulting in excessive jitter at the receiver. Some equalization to produce slight droop in the second half of signals of duration BT, on the other hand, may help decrease jitter at the far end of long cables.

The amplitude of the power spectrum at the output of the transmitter for all possible sequences of signals shall not exceed that produced by an idealized transmitter sending corresponding rectangular waveforms with magnitude 3.65 V at any frequency.

When a transmitter enters the idle state, it shall maintain a minimum differential output, voltage of 2.0 V from 100 ns through 2 BT after the last low-to high transition, as illustrated in Figure 12–21. The differential

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output voltage shall then fall to 1.1 V within 3 BT after that same low-to-high transition. Starting when the differential output voltage first reaches 1.1 V, the magnitude of the output voltage driven into the test loads indicated in Figure 12–22 and Figure 12–23 shall then remain within the limits indicated in Figure 12–21 until the transmitter leaves the idle state.

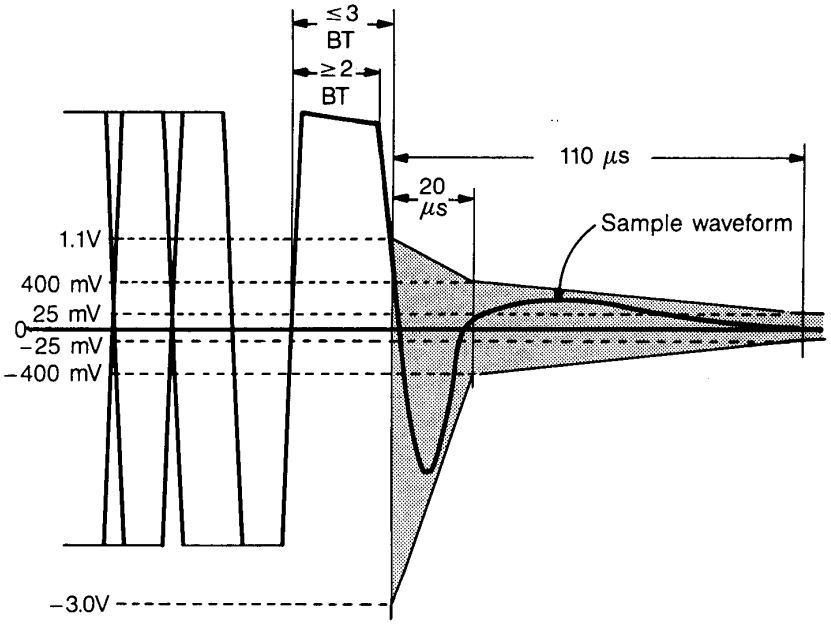

Figure 12–21—Transmitter waveform for idle

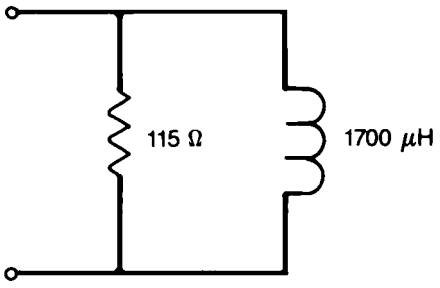

Figure 12–22—Start-of-idle test load #1

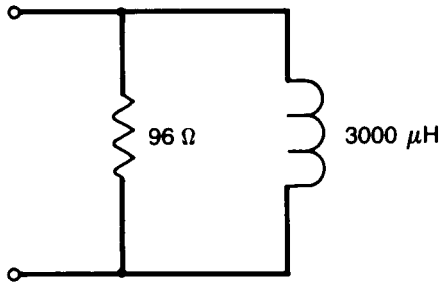

Figure 12–23—Start-of-idle test load #2

The transmitter output at the start of idle may exhibit overshoot, ringing, slow voltage decay, or a combination thereof due to the following factors:

a) Change in transmitter source impedance between the active and idle states
b) Difference in the magnitudes of the differential output voltage between the high and low output states (ΔV_{OD})
c) Waveform asymmetry at the transmitter (ΔT)
d) Transmitter and receiver (transformer) inductance (L)

NOTE 1—The contribution to the undershoot from each of these can be computed with the following equations:

$$V_{\Delta V_{OD}} = \pm V_{OD} \times (R_{OFF}/2R_N)$$

$$V_{\Delta T} = (\pm \Delta T/1000\ \text{ns}) \times V_P(R_{OFF}/R_{ON})$$

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$$V_L = V_P \times (1 - e^{-2.75\ \mu s/(L_P/R_{ON})}) \times (R_{OFF}/R_{ON})$$

where

$R_{OFF} = (R_{SRC\text{-}OFF} \parallel R_L)$

$R_{ON} = (R_{SRC\text{-}ON} \parallel R_L)$

$R_{SRC\text{-}OFF}$ = source impedance (Ω) when the driver is off

$R_{SRC\text{-}ON}$ = source impedance (Ω) when the driver is on

R_L = load impedance (Ω)

L_P = combined inductance (μH) of the transmitter and receiver transformers

ΔV_{OD} = the difference (V) in magnitude of the HI and LO output voltages

ΔT = asymmetry of the waveform equals the difference between the average HI and average LO pulse widths (ns) at the transmitter

VP = the maximum output voltage (V) during the start of IDL

NOTE 2—The waveform shown in Figure 12–21 and the equations in the preceding note apply to a transmitter connected to the test loads of Figure 12–22 and Figure 12–23. An actual receiver may present a more complex termination impedance and so the undershoot or overshoot may exceed that encountered with the test loads.

12.5.3.1.2 Output timing jitter

The transmitted signal zero-crossings shall deviate from the idealized zero-crossings by no more than ± 10 ns.

12.5.3.1.3 Transmitter impedance balance

The longitudinal to metallic impedance balance of the transmitter, defined as 20 $\log_{10}(E_{test}/E_{dif})$, where E_{test} is an externally applied ac voltage, as shown in Figure 12–24, shall exceed 44 dB at all frequencies up to and including 4BR in the idle and nonidle states.

NOTE—It may be difficult to measure the transmitter impedance balance in the nonidle state. A frequency-selective wavemeter or other measurement technique may be required. Furthermore, the balance of the test equipment (such as the matching of the 400 Ω resistors) has to exceed that required of the transmitter.

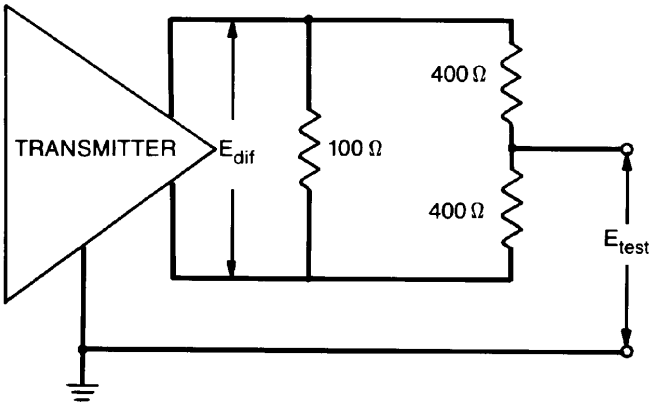

Figure 12–24—Transmitter impedance balance

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12.5.3.1.4 Common-mode output voltage

The magnitude of the total common-mode output voltage of the transmitter, E_{cm}, measured as shown in Figure 12–25, shall not exceed 300 mV.

NOTE—The implementer should consider any applicable local, national, or international regulations and standards concerning RF emission. Driving unshielded twisted pairs with high-frequency common-mode voltages may result in interference to other equipment.

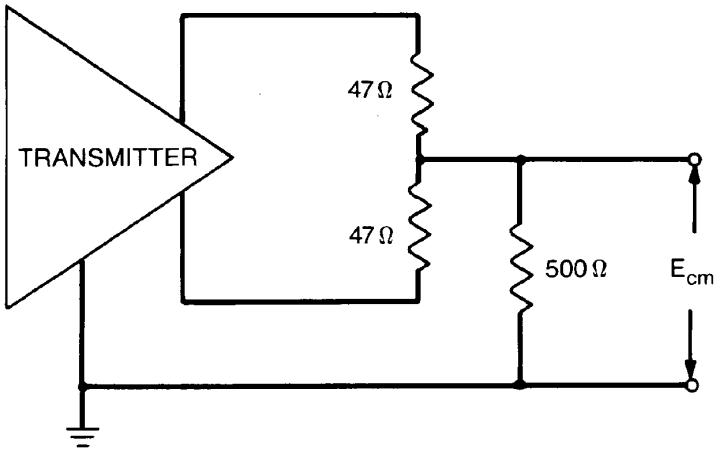

Figure 12–25—Common-mode output voltage

12.5.3.1.5 Common-mode tolerance

Transmitters shall meet the requirements of 12.5.3.1.1 and 12.5.3.1.2 even in the presence of common-mode sinusoidal voltage, E_{cm} (as shown in Figure 12–26), of ± 20 V peak at frequencies from 40 kHz through 6BR.

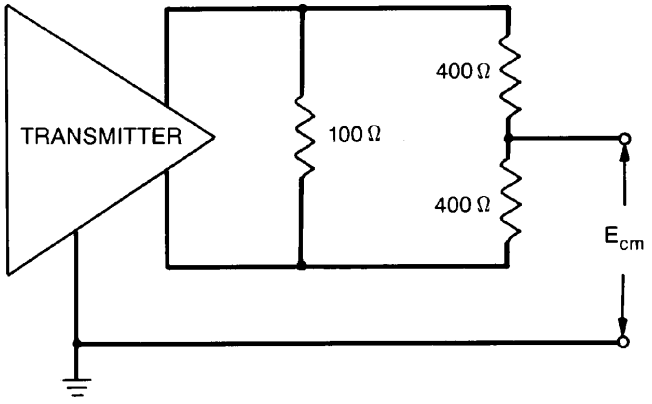

Figure 12–26—Transmitter common-mode tolerance

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12.5.3.1.6 Transmitter fault tolerance

Transmitters, both when idle and when nonidle, shall tolerate the application of short circuits across their outputs for an indefinite period of time without damage and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Transmitters, both when idle and when nonidle, shall withstand, without damage, a 1000 V common-mode impulse of either polarity, applied as indicated in Figure 12–27. The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

NOTE—Tolerance of, and recovery from, the application of the telephony voltages described in 12.10.2 is optional, but the safety requirements of that subclause are mandatory.

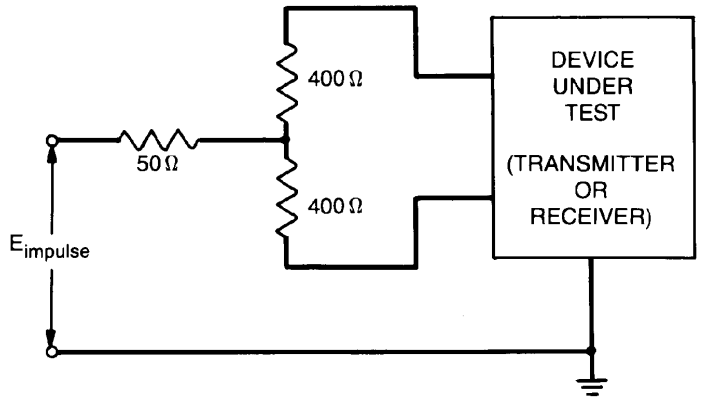

Figure 12–27—Common-mode impulse test

12.5.3.2 Receiver characteristics

12.5.3.2.1 Differential input voltage

The receiver shall operate properly when a signal meeting the minimum magnitude requirements of Figure 12–28 is received. When less than 300 mV, the magnitude of the voltage will exceed that of a straight line through the nearest zero-crossing with slope of magnitude 9 mV/ns. That is, the average slew rate near each zero-crossing will exceed 9 mV/ns. The magnitude of the voltage will also remain at or above 1.0 V for some period lasting at least 150 ns (650 ns for pulses of duration BT) that starts within 250 ns of the preceding zero-crossing and its peak will be at least 1.1 V.

12.5.3.2.2 Input timing jitter

Receivers shall operate properly with zero-crossing jitter of up to ± 32 ns from the ideal.

12.5.3.2.3 Idle input behavior

The IDL condition shall be detected within 1.8 bit times of the last low-to-high transition at the receiver.

NOTE 1—It is necessary to distinguish CVH from IDL.
NOTE 2—System jitter considerations make it impractical to detect IDL (<etd>, end-of-transmission delimiter) any sooner than 1.3 bit times. The specific implementation of the clock recovery mechanism, or equivalent, determines the lower bound on the actual IDL detection time. Adequate margin should be provided between the lower bound and 1.8 bit times.

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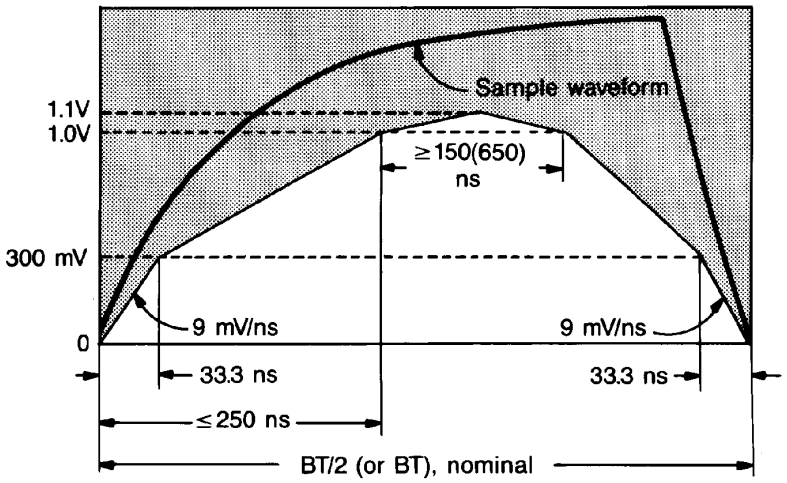

Figure 12–28—Receiver signal envelope

The receiver shall take precautions to ensure that the HI-to-silence transition of the start of IDL is not falsely interpreted as a silence-to-nonidle transition, even in the presence of signal droop, overshoot, ringing, slow voltage decay, or a combination thereof due to capacitive and inductive effects in the transmitter, cable, and receiver, including those discussed in 12.5.3.1.1.

To this end, a receiver in a hub shall treat its input as if it were idle for between 20 and 30 μs after detecting IDL. The timing of this "protection" period for the port PMAs may use a single timer that is started when all ports have become idle or disabled by the Jabber function. Receivers in DTEs may include a similar protection period of up to 30 μs.

NOTE—The protection period is required in hubs because erroneously interpreting the start-of-idle as a new transmission will result in propagation of the error to DTEs, despite any precautions taken in those DTEs. The protection period is optional in DTEs because any implementation error in a DTE will affect only that particular DTE.

12.5.3.2.4 Differential input impedance

The (complex) differential input impedance of the receiver, $Z_{receiver}$, shall be such that the reflection attenuation, defined as 20 $\log_{10}$ ($|Z_{receiver} + Z_{cable}|/|Z_{receiver} - Z_{cable}|$), where Z_{cable} is the differential characteristic impedance of the attached cable, exceeds 16 dB over the range BR/2 through 2BR for all cables meeting the requirements of 12.7.2.

12.5.3.2.5 Common-mode rejection

Receivers shall assume the proper output state for any differential input signal, E_s, that results in a signal, E_{dif}, that meets 12.5.3.2.1 and 12.5.3.2.2, even in the presence of common-mode sinusoidal, voltages, E_{cm} (as shown in Figure 12–29), of ±20 V peak at frequencies from 40 kHz through 6BR.

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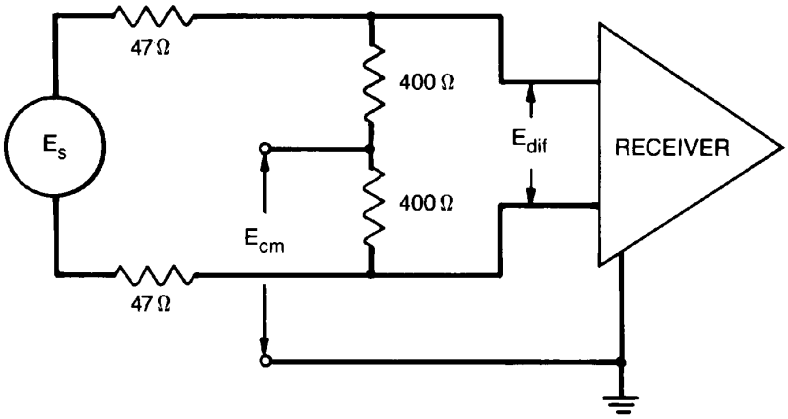

Figure 12–29—Receiver common-mode rejection

12.5.3.2.6 Noise immunity

Receivers shall meet the following limits on average error ratios when the noise described in 12.7.4 is added to the signals described in 12.5.3.2.1 and 12.5.3.2.2:

a) When nonidle, the receiver error ratio shall not exceed one error in 10^8 bits.
b) When idle, a receiver used in a DTE shall not falsely detect carrier more than one in 100 s.
c) When idle, a receiver used in a hub shall not falsely detect carrier more than once in 1500 s.

NOTE—Receivers whose inputs include a 2–4 MHz, 2-pole, low-pass, Butterworth filter and a 560 mV squelch level will meet this last requirement for idle-mode noise immunity yet still perform properly with the weakest signal allowed by 12.5.3.2.1.

12.5.3.2.7 Receiver fault tolerance

Receivers shall tolerate the application of short circuits across their inputs for an indefinite period of time without damage and shall resume normal operation after such faults are removed.

Receivers shall withstand, without damage, a 1000 V common-mode impulse of either polarity, applied as indicated in Figure 12–27. The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

NOTE—Tolerance of, and recovery from, the application of the telephony voltages described in 12.10.2 is optional, but the safety requirements of that subclause are mandatory.

12.6 Medium Dependent Interface (MDI) specification

12.6.1 Line interface connector

8-pin connectors meeting the requirements of Clause 3 and Figure 1 through Figure 5 of IEC 60603-7 shall be used as the compatibility interface between the PMA and the medium. The use of other types of connectors, if any, within a PMA or within the medium, although not explicitly prohibited, is outside the scope of this standard.

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12.6.2 Connector contact assignments

The contacts of the connectors, as depicted in Figure 12–32 and Figure 12–31, shall correspond to signaling circuits as indicated below:

Contact	Signal
1	Upward Data+ (positive for HI signal)
2	Upward Data– (negative for HI signal)
3	Downward Data+ (positive for HI signal)
4	not used by 1BASE5
5	not used by 1BASE5
6	Downward Data– (negative for HI signal)
7	reserved
8	reserved

For DTEs and the upper MDI of hubs, contacts 1 and 2 are used for transmitting and contacts 3 and 6 are used for receiving. For the port MDIs of hubs, however, contacts 1 and 2 are used for receiving and contacts 3 and 6 are used for transmitting.

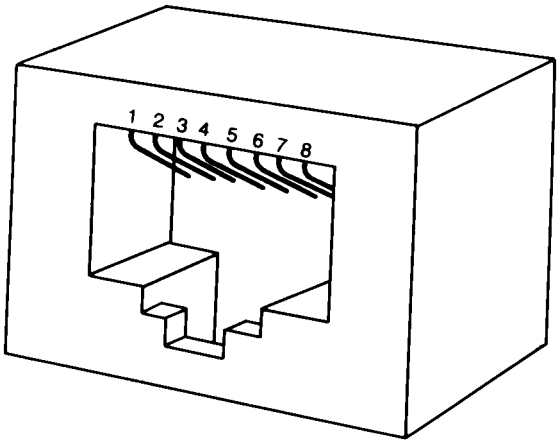

Figure 12–30—DTE and hub connector

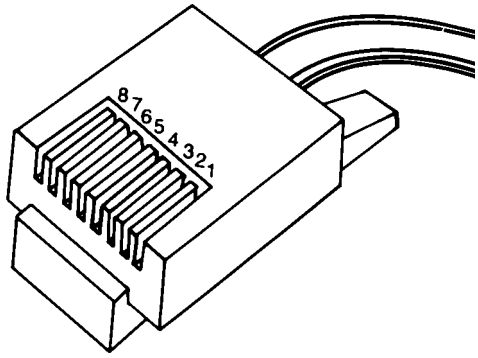

Figure 12–31—Cable connector

12.6.3 Labeling

To distinguish 1BASE5 connectors from those used for other purposes, it is recommended that appropriate labels be affixed to wall outlets and other connectors. This is particularly important in environments in which the specified 8-contact connectors are used for more than one purpose.

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12.7 Cable medium characteristics

12.7.1 Overview

A significant number of IBASE5 networks are expected to utilize in-place building wiring. In this environment, DTEs connect to wall outlets using twisted-pair telephone cord. The wall outlets, in turn, connect to wiring closets, where hubs could be located, using standard telephone wiring. This wiring typically consists of 0.4–0.6 mm diameter (26–22 gauge) unshielded twisted pairs.

12.7.2 Transmission parameters

Each wire pair used to interconnect DTEs and hubs shall meet the requirements of 12.9.3 and also have the following characteristics.

12.7.2.1 Attenuation

Total cable attenuation between a transmitter and the corresponding receiver shall be no more than 6.5 dB at all frequencies between BR/2 and BR, 9.2 dB at frequencies between BR and 2BR, and 13.8 dB at frequencies between 2BR and 4BR.

12.7.2.2 Differential characteristic impedance

The magnitude of the differential characteristic impedance at frequency BR, Z_{BR}, of each wire pair used shall be between 80 Ω and 115 Ω. In addition, the magnitude and phase angle of the characteristic impedance at each of the following frequencies shall be within the corresponding ranges indicated:

Magnitude			Phase angle	
Frequency	**Minimum**	**Maximum**	**Minimum**	**Maximum**
BR/4	Z_{BR}	Z_{BR} + 7 Ω	–10°	0°
BR/2	Z_{BR}	Z_{BR} + 5 Ω	–8°	0°
BR	Z_{BR}	Z_{BR}	–6°	0°
2BR	Z_{BR} – 4 Ω	Z_{BR}	–4°	0°
4BR	Z_{BR} – 5 Ω	Z_{BR}	–3°	0°

12.7.2.3 Medium timing jitter

Intersymbol interference and reflections due to impedance mismatches between the sections of a cable segment can introduce jitter in the timing of the zero-crossings. A cable segment terminated in 96 Ω shall add no more than ± 17 ns, referenced to the transmit clock, of edge jitter when driven with a rectangular signal of magnitude 2.5 V through a source impedance 22 Ω. The driving signal shall be a Manchester-encoded pseudo-random sequence of data with a repetition period of at least 511 bits.

NOTE 1—The reflections caused by splicing two cable sections that have different characteristic impedances (but that each meet the requirements of 12.7.2.2) will not contribute significantly to timing jitter if the splice is within 10 m of either end of the segment.
NOTE 2—Branches off a wire pair (often referred to as “bridged taps” or “stubs”) will generally cause excessive jitter and so should be avoided.
NOTE 3—Jitter can be measured at the receiving end of a segment using an oscilloscope. The oscilloscope is triggered

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on zero-crossings; the deviation of subsequent zero-crossings from multiples of BT/2 is then observed. The deviation of each zero-crossing should not exceed ±34 ns.

12.7.2.4 Dispersion

Each wire pair shall produce an output signal that meets the zero-crossing edge rate described in 12.5.3.2.1 when driven with a 1 MHz trapezoidal signal of magnitude 2.0 V (that is, 4.0 V peak-to-peak) with edge rate 20 mV/ns.

12.7.3 Coupling parameters

To avoid excessive coupling of signals between pairs of a cable, the crosstalk and imbalance have to be limited.

Crosstalk attenuation is specified with the far end of both the disturbed and the disturbing pairs and the near end of the disturbed pair terminated in 96 Ω.

12.7.3.1 Pair-to-pair crosstalk

The near-end, differential, crosstalk attenuation between each wire pair and each other pair in the same cable shall be at least 45 dB frequencies up to BR and at least $45 - 15 \log_{10}(f/\mathrm{BR})$ dB for each frequency f between BR and 4BR.

12.7.3.2 Multiple-disturber crosstalk

The near-end, differential, crosstalk attenuation between multiple disturbing wire pairs and a disturbed pair in the same cable shall be at least 38.5 dB at frequency BR and at least $38.5 - 15 \log_{10}(f/\mathrm{BR})$ dB for each frequency f between BR and 4BR.

When two or more disturbers are present in a common cable sheath, the multiple-disturber, near-end, crosstalk attenuation (MDNEXT) into each pair, measured in dB, may be determined using the following equations:

$$H_j = \sum_{i \neq j} 10^{(-X_{ij}/20)} \cos\theta_{ij}$$

$$V_j = \sum_{i \neq j} 10^{(-X_{ij}/20)} \sin\theta_{ij}$$

$$MDNEXT_j = 10\log_{10}(H_j^2 + V_j^2)$$

where

i iterates over each disturbing pair
j is the disturbed pair
X_{ij} is the magnitude of the near-end, differential, crosstalk attenuation from pair i to pair j
θ_{ij} is the phase angle of the near-end, differential, crosstalk attenuation from pair i to pair j

If only the probability distribution of X_{ij} is known, then the distribution of MDNEXT can be determined using Monte Carlo methods with that X_{ij} distribution and a phase angle uniformly distributed between 0 and 2π rad.

NOTE—See B.3 for example computations of MDNEXT distributions.

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12.7.3.3 Balance

The longitudinal to metallic balance of the cable, defined as 20 $\log_{10}$ (E_{test}/ $2E_x$), where E_{test} is an externally applied voltage, as shown in Figure 12–32, shall exceed 44 dB at all frequencies up to 4BR.

NOTE—The balance of the test equipment (such as the balance of the transformer and the matching of the 300 Ω resistors) has to exceed that required of the cable.

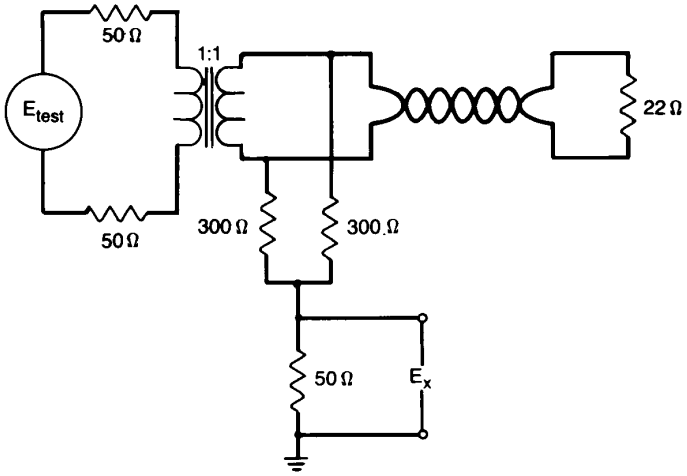

Figure 12–32—Cable balance test

12.7.4 Noise environment

Links used with 1BASE5 shall provide a noise environment no worse than that described below. The total noise environment generally results from two primary contributions: self-crosstalk from other 1BASE5 wire pairs and externally induced impulse noise, typically from telephone ringing and dialing signals, and office machinery. For the purposes of this standard, it can be assumed that the two components contribute independently and so the total error ratio can be appropriately split between the two.

12.7.4.1 Impulse noise

The noise voltage on wire pairs terminated at both ends in 96 Ω, as measured through the following specified filters, shall not exceed the corresponding threshold voltages more than 9 times per 1800 s interval. Following the start of any particular impulse that is counted, any additional impulses shall be ignored (that is, not counted) for a period of 100 μs. Each filter is a 2-pole Butterworth low-pass filter with the indicated cut-off (3 dB point) frequency.

Cut-off frequency	Threshold
2 MHz	170 mV
4 MHz	275 mV
10 MHz	560 mV

The impulse noise occurrence rate changes inversely by one decade for each 7 dB change in the threshold voltage. That is, if the noise occurrence rate is 9 counts per 1800 s at a particular threshold voltage, then a rate of 9 counts per 18 000 s will occur at a threshold 7 dB above that voltage. If a count rate of *N* counts per

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1800 s is measured on a specific cable and filter at the specified voltage threshold, the media noise margin is $7 \log_{10}(9/N)$ dB.

12.7.4.2 Crosstalk

The level of crosstalk noise on a pair depends on the level of the disturbing signal(s) and the crosstalk attenuation from the pair(s) carrying the signal(s). With the maximum transmit level specified in 12.5.3.1, the sinusoidal crosstalk attenuations specified in 12.7.3.1 and 12.7.3.2, and multiple, synchronized, random Manchester disturbers, the peak self-crosstalk (that is, crosstalk from other 1BASE5 signals) noise levels, as measured through the following specified filters, shall be less than or equal to the levels indicated below. Each filter is a 2-pole Butterworth low-pass filter with the indicated cut-off (3 dB point) frequency.

Cut-off frequency	Level
2 MHz	105 mV
4 MHz	160 mV

12.8 Special link specification

12.8.1 Overview

Some 1BASE5 networks may require extension beyond the limits imposed by 12.7 or, due to the installation environment, may require special media such as optical fiber, high-grade cable, or even free-space transmission. The detailed design of special links that replace standard links for use in such circumstances is beyond the scope of this standard, but the end-to-end characteristics are specified. It shall be the responsibility of the supplier to ensure the proper operation of special links with other 1BASE5 equipment.

12.8.2 Transmission characteristics

Special links shall meet the overall attenuation, jitter, and dispersion specifications of 12.7.2.1, 12.7.2.3, and 12.7.2.4, respectively. Total noise introduced due to crosstalk or other sources shall not exceed that allowed for standard media, as specified in 12.7.4. To the extent that it affects operability with 1BASE5 transmitters and receivers, special links shall also meet the impedance and balance requirements of 12.7.2.2 and 12.7.3. The delay and preamble loss allowed for special links is specified in 12.9.4.

12.8.3 Permitted configurations

No more than one special link is permitted in the path between any DTE and the header hub. That is, special links may be installed in parallel but not in series.

NOTE—Special links may be combined with other 1BASE5 components, such as hubs. Such combinations are subject to the performance specifications of this standard only as visible at their external interfaces. For example, explicit MDIs are not required internal to such combinations.

12.9 Timing

12.9.1 Overview

The successful interconnection of multivendor system components mandates that delay and bit loss be allocated fairly and realistically among the various system elements. The balance of this subclause defines the upper limits of delay and bit loss allocated to each component. These values allow proper operation with the

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worst-case system configuration of five levels of hubs, special links, maximum-length cable segments throughout the network, and colliding DTEs at extremes of the network.

12.9.2 DTE timing

DTE Initial Transmit Delay is the time from the first full transition (due to the first OUTPUT_UNIT of preamble) from the MAC to the first full transition (after startup bit loss, if any) at the MDI. This delay shall not exceed 3 BT. The start bit loss shall not exceed 1 bit.

DTEs shall correctly receive frames that are preceded by 13 or more bits of preamble plus 8 bits of <sfd>.

There is a delay between the reception of signal at the PMA input of a DTE and operation of the deferral process in the MAC. Therefore, there is a window in which a DTE may fail to defer to a transmission even after it has arrived at the input. The DTE Deference Delay is the time from the receipt of the first transition of the preamble at the MDI until the last moment that the DTE might start transmitting at the MDI. This delay includes the following components:

a) The delay from the first input transition at the MDI to CARRIER_ON at the PLS-MAC interface
b) The delay through the MAC processes from CARRIER_ON to the last moment that a new transmission would miss being deferred
c) The delay from the first OUTPUT_UNIT at the MAC-PLS interface to the first output transition at the MDI

The DTE Deference Delay shall be no more than 21 BT.

The DTE Collision Shutdown Delay is the time from the first CVL or CVH arriving at the MDI of a transmitting DTE until that DTE transmits IDL at that interface. This time shall be no more than 26 BT + jamSize=58 BT. This limit shall not start until after the <sfd> has been transmitted.

12.9.3 Medium timing

The Medium Transit Delay is the time from when a signal enters the medium until that signal leaves the medium. This delay shall not exceed 4 BT.

12.9.4 Special link timing

The Special Link Transit Delay is the time from when a signal enters a special link until that signal leaves the special link. This delay shall not, exceed 15 BT. The preamble leaving a special link shall be no more than 2 bit cells longer than the preamble sent to that special link and no more than 1 bit cell shorter than the preamble sent to that special link. For the purposes of these limits only, the first bit transmitted shall be considered part of the silence of the preceding IDL unless it meets the requirements for the succeeding bits specified in 12.5.3.1.1 and 12.5.3.1.2.

12.9.5 Hub timing

Hub Startup Delay is the time from when the first bit cell of the preamble arrives at a hub until the first bit cell (also preamble) leaves that hub. This time shall be no greater than 12 BT. The preamble sent by a hub shall be no more than 1 bit cell longer than the preamble sent to that hub or more than 4 bit cells shorter than the preamble sent to that hub. For the purposes of these limits only, the first bit transmitted shall be considered part of the silence of the preceding IDL unless it meets the requirements for the succeeding bits specified in 12.5.3.1.1 and 12.5.3.1.2.

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Hub Idle Collision Startup Delay applies to any case in which CP arrives preceded by fewer (or no) bit times of preamble than the Hub Startup Delay. The time from arrival of the first bit cell (either preamble or CP) until the first bit cell leaves the hub shall be no greater than 12 BT.

Hub Transit Delay is the time from the arrival of any bit cell at a hub to the transmission of the corresponding bit cell from the hub. This delay shall not exceed 9 BT, excluding the cumulative effects of clock tolerance.

The transit (propagation) delay between the upward and downward sides of the Header Hub shall be negligible.

Hub Delay Stretch/Shrink is the increase or decrease in a hub's transit delay due to the effects of differing clock rates. The clock rate tolerance of 0.01% specified in 12.3.2.4.1 and the maximum frame size of 1518 octets specified in 4.4.2 yield a maximum stretch or shrink of $(56 + 8 + 1518 \cdot 8) \cdot 0.01\% \cdot 2 < 3$ BT, both at any given hub and through an entire network.

Hub Collision Detect Delay is the time required for a hub to detect multiple incoming signals and initiate transmission of CP. The time until transmission of the first CVH or CVL shall be no greater than 21 BT.

Hub Active Collision Startup Delay is the time from the arrival of the first CVH or CVL of a CP pattern at a hub that is repeating bit cells until transmission of the first CVH or CVL from the hub. This delay shall be no greater than 12 BT in either the upward or downward direction.

Hub Collision Shutdown Delay is the time from IDL arriving at a hub that is passing on or generating CP until that hub starts transmitting IDL. This delay shall be limited to 9 BT. The limit is relaxed to 25 BT, however, for the upward side of a hub that is generating CP. This extra allowance is made to avoid requiring implementation of a separate <etd> detection mechanism in each port of the hub.

12.10 Safety

Implementers are urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate standards. EIA CB8-1981 [B20] provides additional guidance concerning many relevant regulatory requirements.

Sound installation practice, as defined by applicable codes and regulations, shall be followed. ECMA-97 [B19] describes safety requirements for local area networks.

12.10.1 Isolation

NOTE—Since September 2003, maintenance changes are no longer being considered for this clause. Since February 2021, electrical isolation requirements are in J.1.

Each PMA/MDI interface lead shall be isolated from frame ground. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 V (rms) at 50 Hz to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC 60950: 1991.
b) 2250 V (dc) for 60 s, applied as specified in Section 5.3.2 of IEC 60950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC 60950: 1991, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

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12.10.2 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 1BASE5 equipment. Other than voice signals (which are very low voltage), the primary voltages that may be encountered are the “battery” and ringing voltages. Although there is no universal standard that constrains them, the following maximums generally apply:

a) Battery voltage to an on-hook telephone line is about –56 Vdc applied to the line through a balanced 400 Ω source impedance. This voltage is used to power the telephone instrument and detect the off-hook condition. Source inductance can cause large spikes on disconnect.
b) Battery voltage to an off-hook telephone line is also about –56 Vdc applied to the line through a balanced 400 Ω source impedance, but most of the voltage appears across the source impedance because the telephone instrument’s impedance is relatively much lower.
c) Ringing voltage is a composite signal. The first portion can be up to 175 V peak at 20 to 66 Hz, limited by a 100 Ω source resistance or a 400 to 600 Ω source inductive impedance. The second portion is –56 Vdc limited by a 300 to 600 Ω source impedance. Large spikes can occur at the start and end of each ring.

Although 1BASE5 equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across the 1BASE5 transmitters or receivers. Because the termination resistance likely to be present across a receiver’s input is of substantially lower impedance than an off-hook telephone instrument, however, receivers will generally appear to the telephone system as off-hook telephones. Full ring voltages, therefore, will be applied for only short periods of time. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to low resistance of the transformer coil.

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13. System considerations for multisegment 10 Mb/s baseband networks

NOTE—This clause relates to clauses that are not recommended for new installations. This clause is not recommended for new installations. Since March 2012, maintenance changes are no longer being considered for this clause.

13.1 Overview

This clause provides information on building 10 Mb/s multisegment baseband networks within a single collision domain. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of the interpacket gap as it travels through the network.

This clause provides two network models. Transmission System Model 1 is a set of configurations that have been validated under conservative rules and have been qualified as meeting the two requirements set forth above. Transmission System Model 2 is a set of calculation aids that allow a configuration to be qualified against the two requirements. This set of calculation aids allows those configuring a network to test a proposed configuration against a simple set of criteria that allows it to be qualified. The Model 2 Transmission System Model validates an additional broad set of topologies that are fully functional and do not fit within the simpler but more restrictive rules of Model 1. Figure 13–1 illustrates an example of such a topology. The five repeaters are beyond the scope of the Model 1 rules yet this topology is fully functional within the limits of round-trip delay and can be validated as such by Model 2.

The physical size of a CSMA/CD network is limited by the characteristics of individual network components. These characteristics include the following:

a) Media lengths and their associated propagation time delay
b) Delay of repeater units (start-up and steady-state)
c) Delay of MAUs (start-up and steady-state)
d) Interpacket gap shrinkage due to repeater units
e) Delays within the DTE associated with the CSMA/CD access method
f) Collision detect and deassertion times associated with MAUs

Table 13–1 summarizes the delays for the various network media segments. In addition, Clause 14 summarizes the delays for the 10BASE-T MAU (Table 14–2); Clause 8, the delays for the 10BASE5 MAU; Clause 10, the delays for the 10BASE2 MAU; Clause 9, the delays of the Fiber Optic Inter Repeater Link (FOIRL) and the repeater (Tables 9–1, 9–2, and 9–3); Clause 16, the delays for the 10BASE-FP MAU (Table 16–1, also see

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15.1); Clause 17, the delays for the 10BASE-FB MAU (Table 17–1, also see 15.1), and Clause 18, the delays for the 10BASE-FL MAU (Table 18–1, also see 15.1).

Table 13–1—Delays for network media segments

Media type	Maximum number of MAUs per segment	Maximum segment length (m)	Maximum medium delay per segment (ns)
Mixing segment			
10BASE5	100	500	2165
10BASE2	30	185	950
10BASE-FP	33[a]	1000[b]	5000
Link segment			
FOIRL	2	1000	5000
10BASE-T	2	100[c]	1000
10BASE-FB	2	2000	10 000
10BASE-FL	2	2000	10 000
AUI[d] 1 DTE/1 MAU		50	257

[a]Actual number depends on the passive-star characteristics; see 16.5.2.1.
[b]In addition, a MAU to passive-star link will not exceed 500 m.
[c]Actual maximum segment length depends on cable characteristics; see 14.1.1.3.
[d]AUI is not a segment.

For a more detailed description of the calculation methods used to arrive at Transmission System Model 2, see B.1.5.

13.1.1 Repeater usage

Repeaters are the means used to connect segments of network medium together, thus allowing larger topologies and a larger MAU base than are allowed by the rules governing individual segments. Different media/segment types can only be connected to each other using repeaters.

13.2 Definitions

See 1.4.

13.3 Transmission System Model 1

The following network topology constraints apply to networks using Transmission System Model 1. If no segment length constraints are given for a segment type, the maximum segment length, as defined in the relevant MAU clause, applies.

a) Repeater sets are required for all segment interconnection.
b) MAUs that are part of repeater sets count toward the maximum number of MAUs on a segment.
c) The transmission path permitted between any two DTEs may consist of up to five segments, four repeater sets (including optional AUIs), two MAUs, and two AUIs.
d) AUI cables for 10BASE-FP and 10BASE-FL shall not exceed 25 m. (Since two MAUs per segment are required, 25 m per MAU results in a total AUI cable length of 50 m per segment.)
e) When a transmission path consists of four repeater sets and five segments, up to three of the segments may be mixing and the remainder have to be link segments (Figure 13–2, Figure 13–3, and

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Figure 13–6). When five segments are present, each fiber optic link segment (FOIRL, 10BASE-FB, or 10BASE-FL) shall not exceed 500 m, and each 10BASE-FP segment shall not exceed 300 m.

f) When a transmission path consists of three repeater sets and four segments (Figure 13–4 and Figure 13–5), the following restrictions apply:
   1) The maximum allowable length of any inter-repeater fiber segment shall not exceed 1000 m for FOIRL, 10BASE-FB, and 10BASE-FL segments and shall not exceed 700 m for 10BASE-FP segments.
   2) The maximum allowable length of any repeater to DTE fiber segment shall not exceed 400 m for 10BASE-FL segments and shall not exceed 300 m for 10BASE-FP segments and 400 m for segments terminated in a 10BASE-FL MAU.
   3) There is no restriction on the number of mixing segments in this case.

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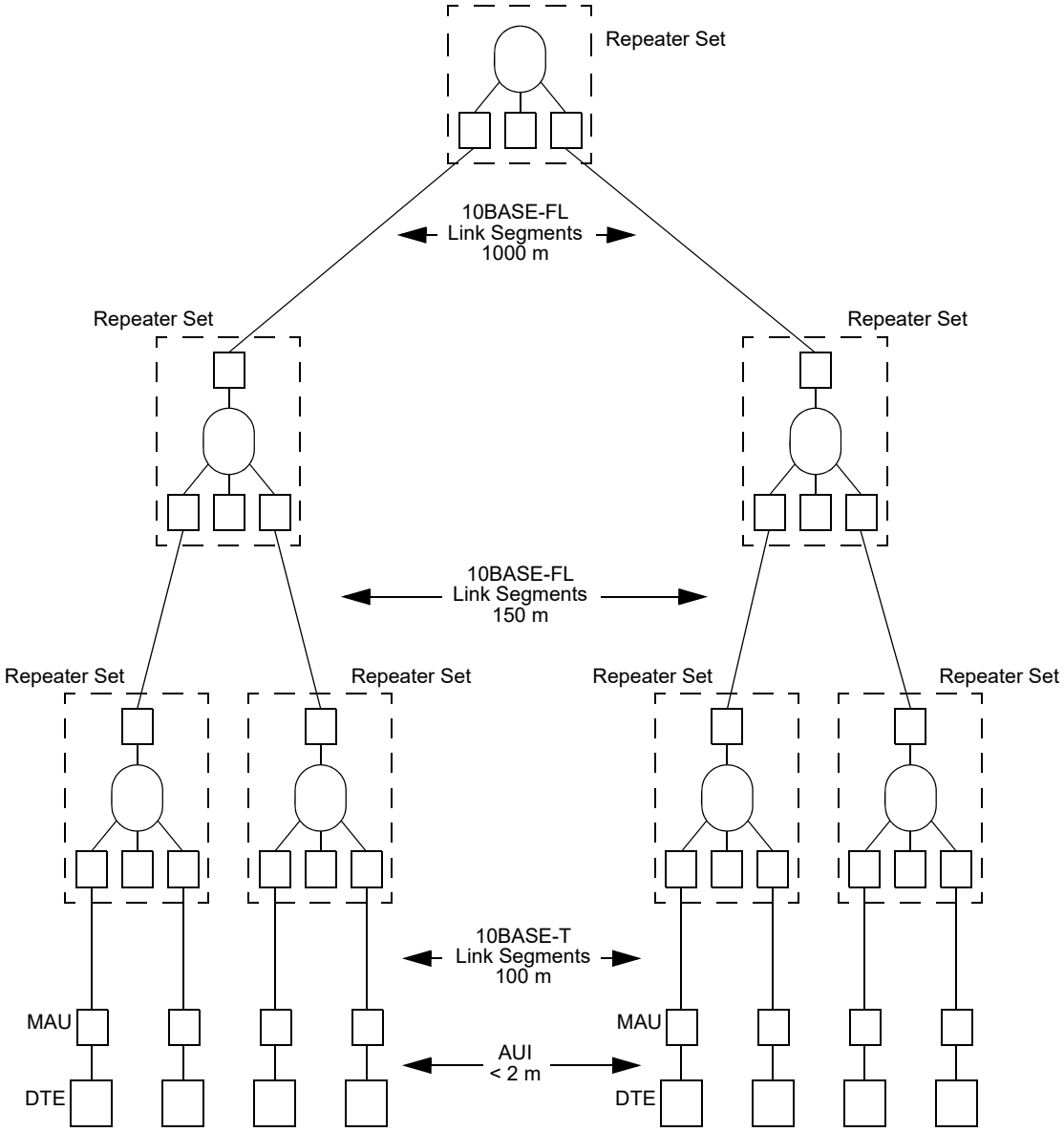

Figure 13–1—Example of maximum transmission path with five repeater sets enabled by Model 2 Transmission System validation

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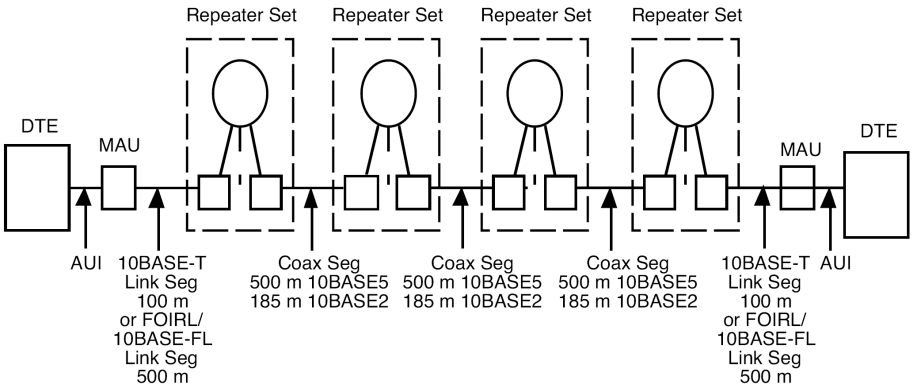

Figure 13–2—Maximum transmission path with three coaxial cable segments and two link segments

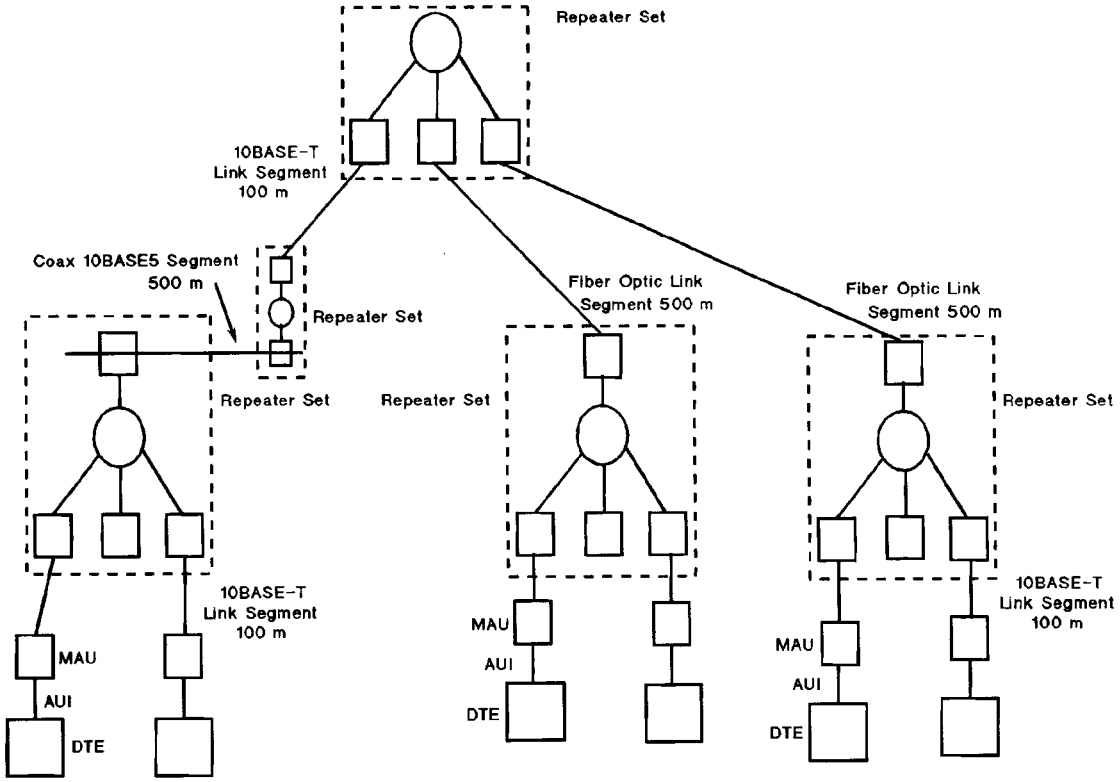

Figure 13–3—Example of maximum transmission path using coaxial cable segments, 10BASE-T link segments, and fiber optic link segments

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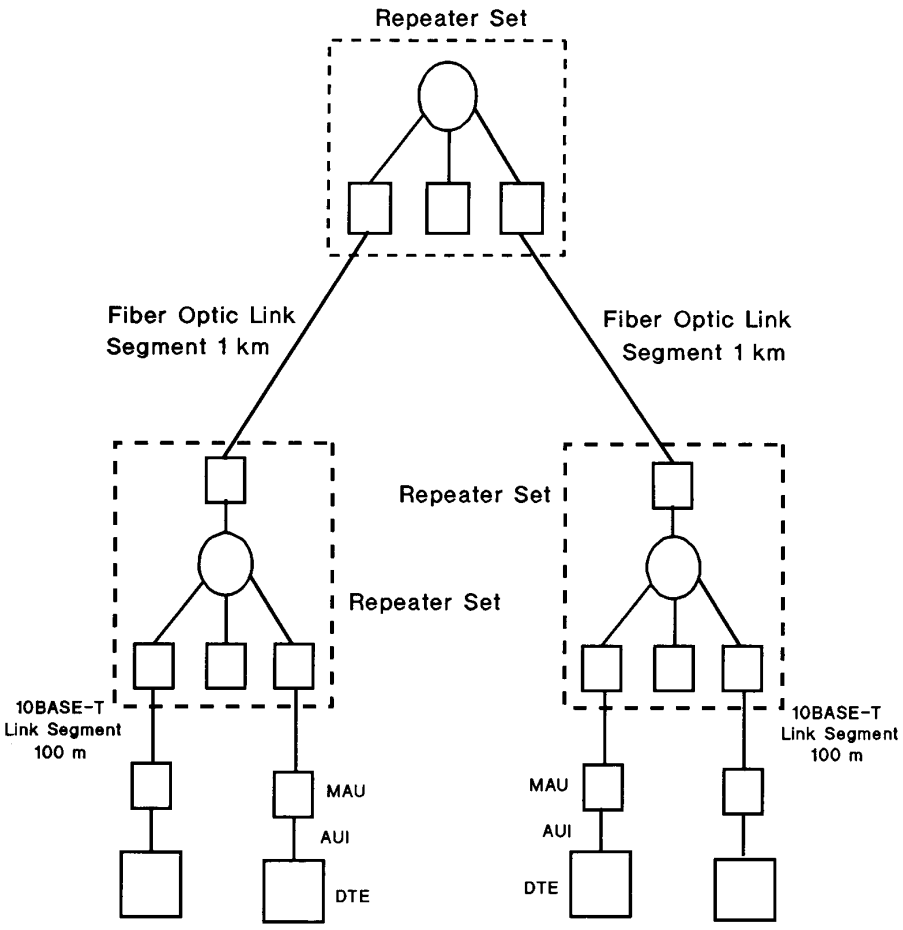

Figure 13–4—Example of maximum transmission path with three repeater sets, four link segments (two are 100 m 10BASE-T and two are 1 km fiber)

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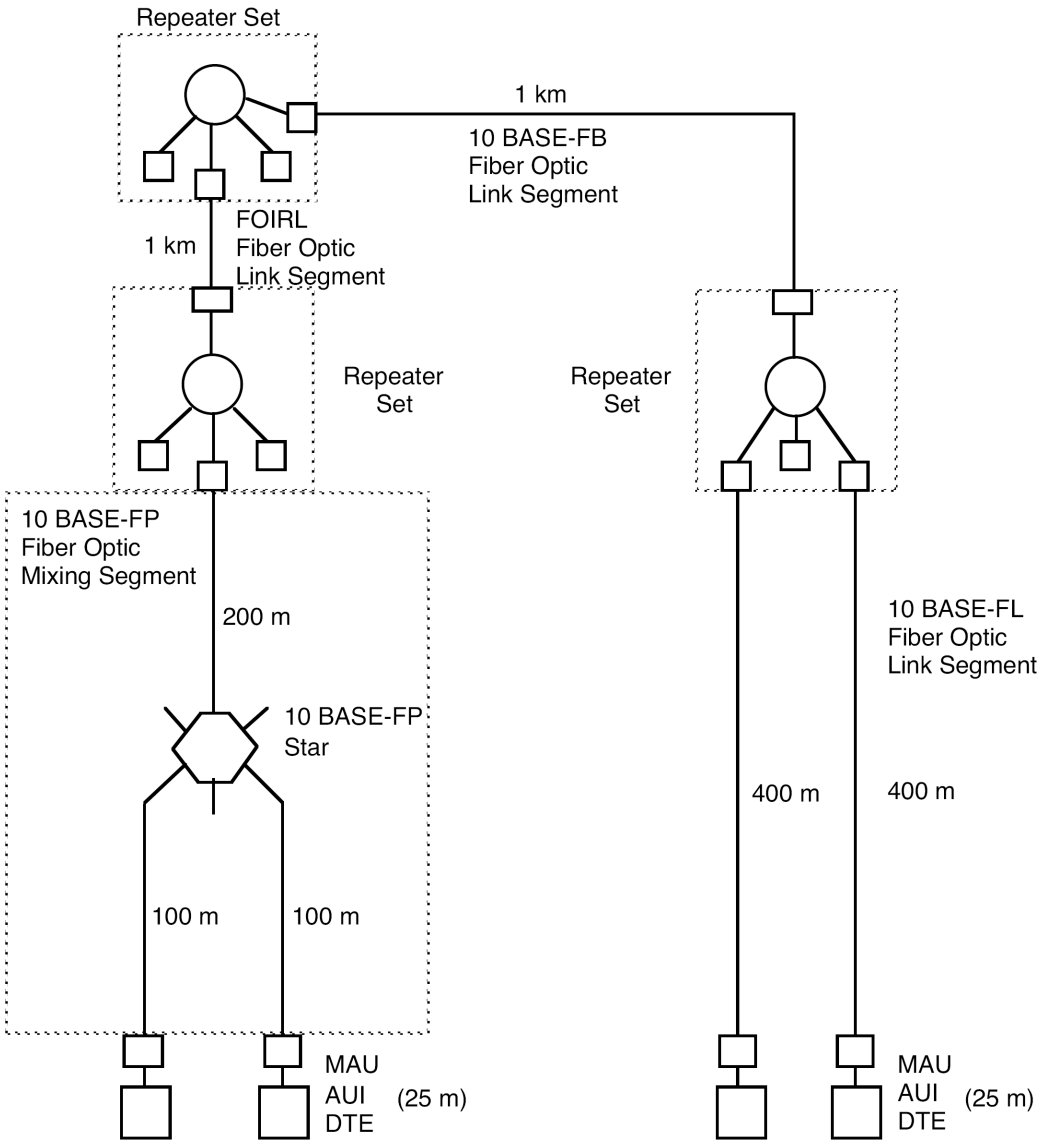

Figure 13–5—Example of maximum transmission path with three repeater sets, four segments (one 1 km 10BASE-FB, one 1 km FOIRL, one 400 m 10BASE-FL, and one 300 m 10BASE-FP)

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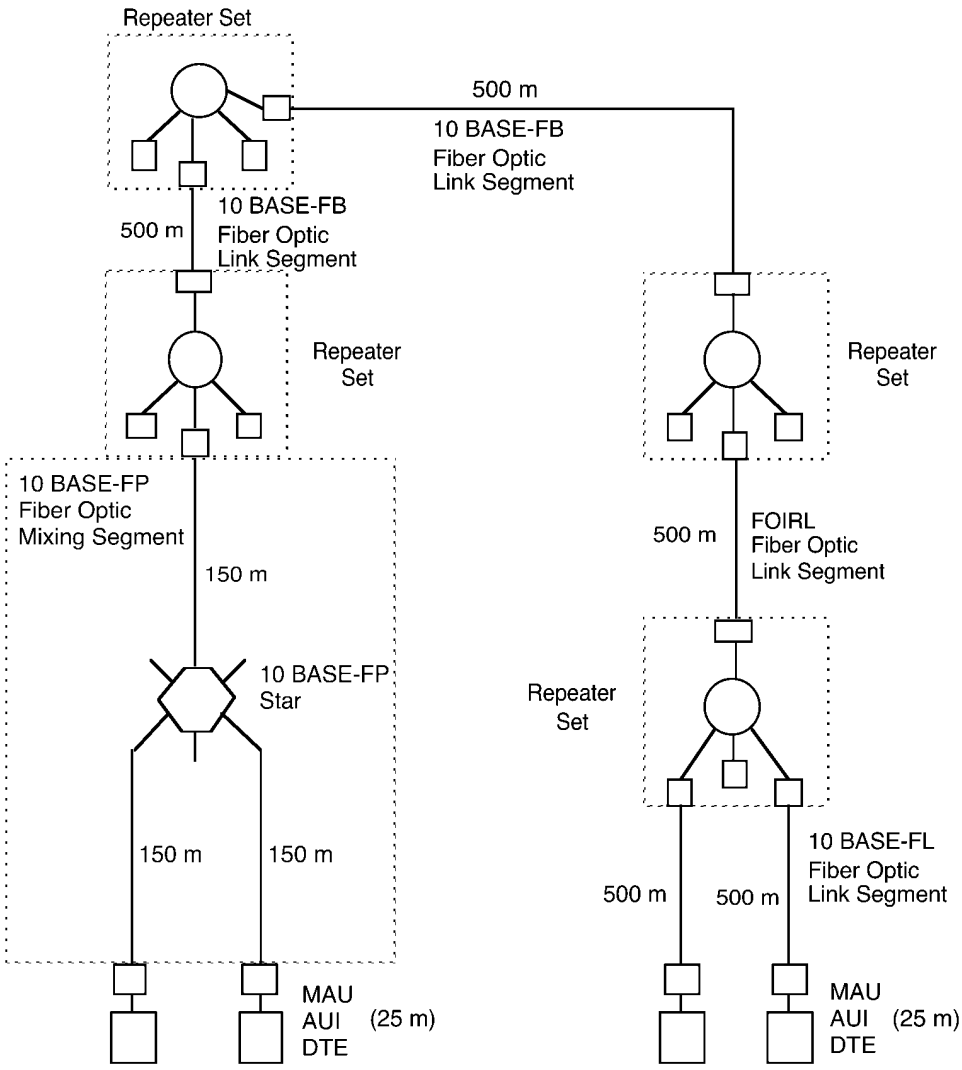

Figure 13–6—Example of maximum transmission path with four repeater sets, five segments (two 500 m 10BASE-FB, one 500 m FOIRL, one 500 m 10BASE-FL, and one 300 m 10BASE-FP)

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13.4 Transmission System Model 2

The physical size and number of topological elements in a 10 Mb/s baseband network is limited by two factors, round-trip collision delay and interpacket gap shrinkage. A network configuration has to be validated against each of these separately. A model of the network is required for each of the calculations. The model consists of a series of segments consisting of a left-end segment, mid-segments, and a right-end segment. The model of the network used in the calculations consists of the worst-case path through the network for that particular calculation. The calculations are sufficiently straightforward that they can be done manually. They are also easy to implement in a spreadsheet. In general, the worst-case path for the two calculations is not the same for any single network. The requirements for each calculation and its respective model are detailed in the following subclauses and in Figure 13–7.

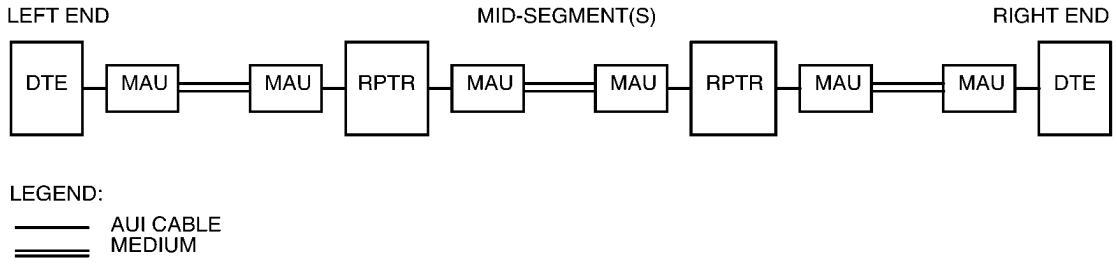

Figure 13–7—Generalized transmission path model

13.4.1 Round-trip collision delay

For a network to be valid, it has to be possible for any two DTEs on that network to contend for the network at the same time. Each station attempting to transmit has to be notified of the contention by the returned "collision" signal within the "collision window" (see 4.1.2.2 and 5.2.2.1.10). Additionally, the maximum length fragment created has to contain less than 511 bits after the Start Frame Delimiter (SFD). This requirement limits the physical diameter (maximum distance between DTEs) of a network. The maximum round-trip delay has to be qualified between all pairs of DTEs in the network. In practice this means that the qualification needs to be done between those that, by inspection of the topology, are candidates for the longest delay.

The following network modeling methodology is provided to assist that calculation.

13.4.1.1 Worst-case path delay value (PDV) selection

The worst-case path through a network to be validated shall be identified. The worst case consists of the path between the two DTEs at opposite ends of the network that have the longest round-trip time (see Figure 13–7).

13.4.1.2 Worst-case PDV calculation

Once a set of paths is chosen for calculation, each shall be checked for validity against the following formulas. (If a candidate for worst-case path has end segments of different types, calculations for the path have to be performed twice, considering first one end segment as the left end, and then the other, and the maximum value obtained used as the PDV.)

a) Determine the Segment Delay Value (SDV) from Table 13–2 for each of the segments in the path.

$$SDV = \text{Base} + [\text{Length} \times (\text{Round-Trip Delay/meter})]$$

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(For mixing segments, length is the length between the repeater and the farthest end of the segment for end segments, or the length between two repeaters for mid-segments.)

or

SDV = Max

(Max is equal to the value above for the maximum media segment length. It is provided for ease of calculation with segments that are at their maximum length or as a default value when the length is not known).

NOTE—The SDV figure in the table includes allowance for an AUI at each end of the segment (except for 10BASE-FB) and up to 2 m of AUI cable. In 10BASE5 segments, AUI cables are normally longer than 2 m. Care should be exercised to assure that provision is made for the delay associated with their actual length.

b) From Table 13–2, determine the SDV for the sum of all AUI cables in excess of 2 m (except the AUI associated with the left end DTE, which does not contribute to the PDV).

c) Sum all SDVs from item a) and item b) plus a margin of up to 5 bits to form the PDV. The margin may be from 0 to 5 bits; 5 bits is recommended. If the PDV is less than or equal to 575, the path is qualified in terms of worst-case delay.

Table 13–2—Segment round-trip delay values in bit times (PDV not to exceed 572)

Segment type	Max length	Left end		Mid-segment		Right end		RT delay/ meter
		Base	Max	Base	Max	Base	Max	
10BASE5 Coax	500	11.75	55.05	46.5	89.8	169.5	212.8	0.0866
10BASE2 Coax	185	11.75	30.731	46.5	65.48	169.5	188.48	0.1026
FOIRL	1000	7.75	107.75	29	129	152	252	0.1
10BASE-T	100[a]	15.25	26.55	42	53.3	165	176.3	0.113
10BASE-FP	1000	11.25	111.25	61	161	183.5	284	0.1
10BASE-FB	2000	N/A[b]	N/A[b]	24	224	N/A[b]	N/A[b]	0.1
10BASE-FL	2000	12.25	212.25	33.5	233.5	156.5	356.5	0.1
Excess length AUI	48	0	4.88	0	4.88	0	4.88	0.1026

[a]Actual maximum segment length depends on cable characteristics; see 14.1.1.3.
[b]Not Applicable, 10BASE-FB does not support end connections.

13.4.2 Interpacket gap (IPG) shrinkage

The worst-case variabilities of transmission elements in the network plus some of the signal reconstruction facilities required in the 10 Mb/s baseband repeater specification combine in such a way that the gap between two packets travelling across the network may be reduced below the interFrameGap specified in 4.4.2. This parameter limits the equipment (i.e., number of repeaters) between any two DTEs. Again this limit applies to all combinations of DTEs on any network but the worst case is apparent from an inspection of a map or schematic representation of the topology in question.

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13.4.2.1 Worst-case path variability value (PVV) selection

A worst-case path through a network to be validated shall be identified.

It should be noted that the receive end segment is not counted in this scenario. This means that in an asymmetrical network where the end segments are of different types, the end segment with the worst variability shall be designated as the “Transmitting End” for this evaluation.

13.4.2.2 Worst-case path variability value (PVV) calculation

Once a set of paths is chosen for calculation each shall be checked for qualification by the following method:

a) Determine the Segment Variability Value (SVV) from Table 13–3 for each of the segments in the Path, excluding the end segment with the lower SVV.
b) Sum all of the SVVs from item 1 to form the PVV. If the PVV is less than or equal to 49, the path is qualified in terms of worst-case variability.

Table 13–3—Segment variability values in bit times (PVV not to exceed 49)

Segment type	Transmitting end	Mid-segment
Coax	16	11
Link except 10BASE-FB	10.5	8
10BASE-FB	N/A[a]	2
10BASE-FP	11	8

[a]Not Applicable, 10BASE-FB does not support end connections.

13.5 Full duplex topology limitations

Unlike half duplex CSMA/CD networks, the physical size of full duplex 10 Mb/s networks is not limited by the round-trip collision propagation delay. Instead, the maximum link length between DTEs is limited only by the signal transmission characteristics of the specific cable.

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14. Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T including type 10BASE-Te

14.1 Scope

14.1.1 Overview

Clause 14 defines the functional, electrical, and mechanical characteristics of the type 10BASE-T MAU and one specific medium for use with that MAU. This clause also specifies the functional, electrical, and mechanical characteristics of the energy-efficient version of 10BASE-T, the type 10BASE-Te MAU, and one specific medium for use with that MAU. The relationship of this clause to the entire IEEE 802-3 LAN International Standard is shown in Figure 14–1. The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the medium.

NOTE—Support for both 10BASE-T and 10BASE-Te signal levels in a single device is not required.

This MAU and medium specification is aimed primarily at office applications where twisted-pair cable is often installed. Installation and reconfiguration simplicity is allowed by the type of cable and connectors used.

The 10BASE-T specification builds upon Clause 1 through Clause 7 and Clause 9 of this standard.

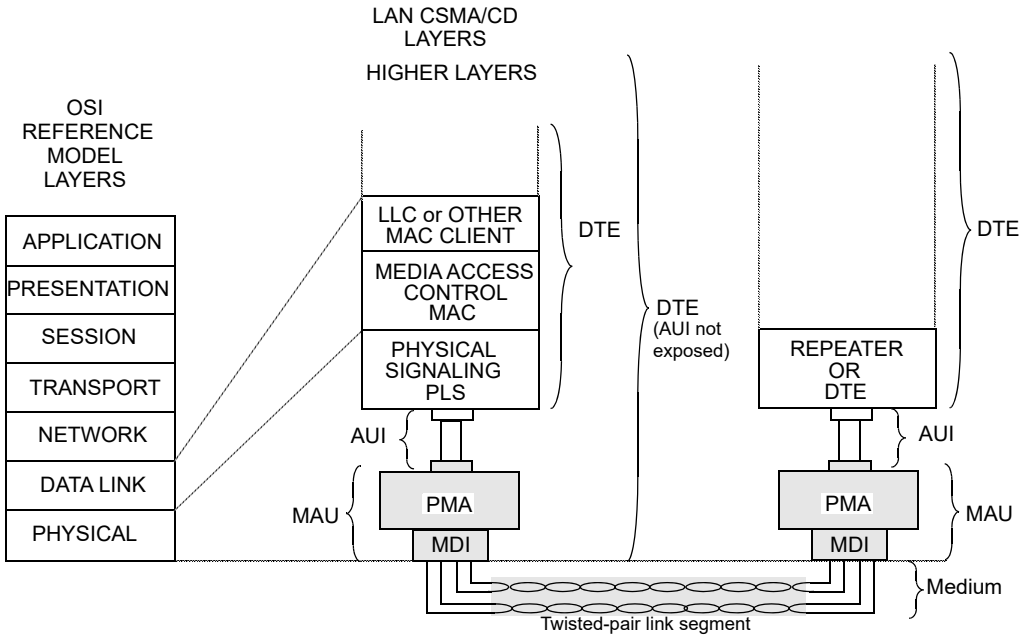

Figure 14–1—10BASE-T relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

14.1.1.1 Medium Attachment Unit (MAU)

The MAU has the following general characteristics:

a) Enables coupling the Physical Signaling (PLS) sublayer by way of the Attachment Unit Interface (AUI) to the baseband twisted-pair link defined in Clause 14.

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b) Supports message traffic at a data rate of 10 Mb/s.
c) Provides for operating over 0 m to at least 100 m of twisted pair without the use of a repeater.
d) Permits the Data Terminal Equipment (DTE) or repeater to confirm operation of the MAU and availability of the medium.
e) Supports network configurations using the CSMA/CD access method defined in this standard with baseband signaling.
f) Supports a point-to-point interconnection between MAUs and, when used with repeaters having multiple ports, supports a star wiring topology.
g) Allows incorporation of the MAU within the physical bounds of a DTE or repeater.
h) Allows for either half duplex operation, full duplex operation, or both.
i) Provides for operation with reduced peak differential voltage on the TD circuit for type 10BASE-Te. A 10BASE-Te MAU interoperates with a 10BASE-T MAU if the minimum cabling requirements of a 10BASE-Te MAU are met.
j) All references to 10BASE-T include 10BASE-Te unless otherwise stated.

14.1.1.2 Repeater unit

The repeater unit is used to extend the physical system topology and provides for coupling two or more segments. Repeaters are an integral part of all 10BASE-T networks with more than two DTEs (see Figure 13–1 and Figure 13–2). The repeater unit is defined in Clause 9. Multiple repeater units are permitted within a single collision domain to provide the maximum connection path length specified in Clause 13. The repeater unit is not a DTE and therefore has slightly different requirements for its attached MAUs, as defined in 9.4.1. Repeater sets with 10BASE-T MAUs are required to provide the auto-partition/reconnection algorithm on those ports, as specified in 9.6.6.2.

14.1.1.3 Twisted-pair media

The medium for 10BASE-T is twisted-pair wire. The performance specifications of the 10BASE-T except 10BASE-Te simplex link segment are contained in 14.4. This wiring normally consists of 0.4 mm to 0.6 mm diameter (26 AWG to 22 AWG) unshielded wire in a multipair cable. The performance specifications are generally met by 100 m of 0.5 mm telephone twisted pair. Longer lengths are permitted providing the simplex link segment meets the requirements of 14.4. A length of 100 m, the design objective, will be used when referring to the length of a twisted-pair link segment.

The medium for 10BASE-Te is twisted-pair wire. The performance specifications of the 10BASE-Te simplex link segment (either pure 10BASE-Te or mixed 10BASE-T, 10BASE-Te) is a channel meeting or exceeding the requirements of the Class D channel specified by ISO/IEC 11801:1995. These channel requirements can also be met by the Category 5 channel specified by ANSI/TIA/EIA-568-A.

NOTE—ISO/IEC 11801:2002 provides a specification for media that exceeds the minimum requirements of this standard.

14.1.2 Definitions

See 1.4 for additional definitions.

14.1.2.1 twisted-pair link: A twisted-pair link segment and its two attached MAUs (see Figure 14–1).

14.1.2.2 twisted-pair link segment (duplex link segment): Two simplex link segments for connecting two MAUs (see Figure 14–2).

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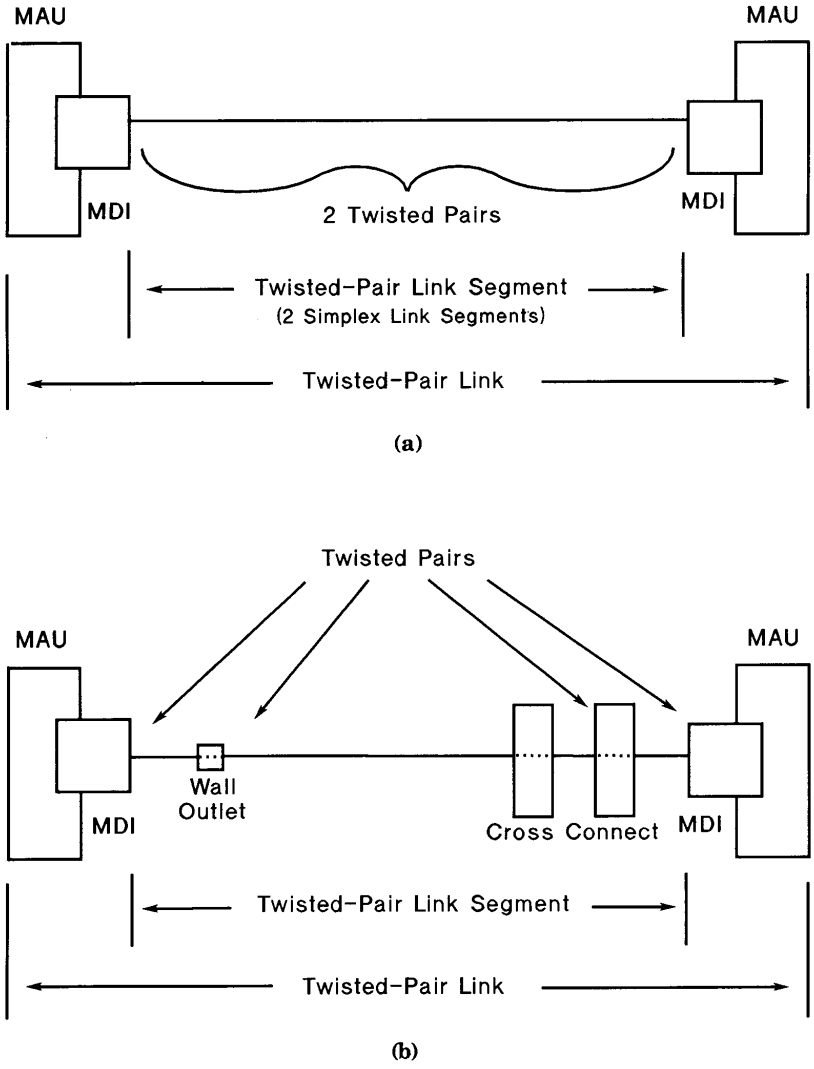

Figure 14–2—Twisted-pair link

14.1.3 Application perspective

This clause states the broad objectives and assumptions underlying the specifications defined throughout Clause 14.

14.1.3.1 Objectives

a) Provide the physical means for communication between LAN Data Link Layer entities.
b) Ensure compatibility of independently developed physical and electrical interfaces.
c) Provide a communication channel with a mean bit error ratio, at the Physical Layer service interface of less than one part in 10^8.
d) Provide for ease of installation and service.
e) Ensure that fairness of DTE access is not compromised.
f) Provide for low-cost networks, as related to both equipment and cabling.
g) Make use of telephone twisted-pair building wiring and telephony wiring practices.

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14.1.3.2 Compatibility considerations

All implementations of the twisted-pair link shall be compatible at the MDI. The MAU and the medium are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the MAU in an application-dependent manner provided the MDI and AUI (when implemented) specifications are met.

14.1.3.3 Modes of operation

The 10BASE-T MAU is capable of operating in *normal* mode only (see 7.1.4). The MAU shall not operate in *monitor* mode.

When normal mode is in operation, the MAU functions as a direct connection between the medium and the DTE or repeater. Data from the DTE or repeater is output to one of the simplex link segments of the link segment, and data received on the other simplex link segment is input to the DTE or repeater.

The operation of a 10BASE-T MAU differs depending on whether the attached DTE is operating in the half duplex or full duplex mode (see 1.1.2). In the full duplex mode, functions relating to the loopback of transmitted data (DO) onto the receive path (DI) are disabled (see 14.2.1.3 and 14.2.1.6). The requirements specified in subclauses of this standard labeled “half duplex mode only” do not apply to a MAU used with a DTE configured for full duplex operation.

14.1.4 Relationship to PLS and AUI

A close relationship exists between Clause 14 and Clause 7. Clause 14 specifies the physical medium parameters and the PMA logical functions residing in the physical MAU. The MAU provides services to the PLS defined in Clause 7 by means of the AUI. 10BASE-T MAUs support a subset of the AUI services specified in Clause 7. 10BASE-T MAUs do not support the optional isolate function, the optional CO circuit, or the optional CS1 signal on the CI circuit.

The design of an external MAU component requires the use of both Clause 14 and Clause 7 for the PLS and AUI specifications.

The figures and numerous textual references throughout Clause 14 refer to terminology associated with the AUI (that is, DO, DI, and CI). Since an embodiment of the 10BASE-T MAU does not require the implementation of an AUI, the DO, DI, and CI circuits may not physically exist. However, they are logically present and MAU operation is defined in terms of them.

14.2 MAU functional specifications

The MAU provides the means by which signals on the three AUI signal circuits to and from the DTE or repeater and their associated interlayer messages are coupled to the twisted-pair link segment. The MAU provides the following functional capabilities to handle message flow between the DTE or repeater and the twisted-pair link segment:

a) Transmit function. Provides the ability to transfer Manchester-encoded data from the DO circuit to the TD circuit. While not sending Manchester-encoded data on the TD circuit, the MAU sends an idle signal, TP_IDL, on the TD circuit.
b) Receive function. Provides the ability to transfer Manchester-encoded data from the RD circuit to the DI circuit. While not sending Manchester-encoded data on the DI circuit, the MAU sends an idle signal, IDL, on the DI circuit.

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c) Loopback function (half duplex mode only). Provides the ability to transfer Manchester-encoded data from the DO to the DI circuit when the MAU is sending Manchester-encoded data to the TD circuit.
d) Collision Presence function. Provides the ability to detect simultaneous occurrence of Manchester-encoded data on the RD and DO circuits and to report such an occurrence as a collision. MAUs connected to full duplex mode DTEs are permitted, but not required, to implement the Collision Presence function.
e) *signal_quality_error* Message (SQE) Test function. Provides the ability to indicate to the DTE that the Collision Presence function is operational and that the *signal_quality_error* message can be sent by the MAU.
f) Jabber function. Provides the ability to prevent abnormally long reception of Manchester-encoded data on the DO circuit from indefinitely disrupting transmission on the network. While such a condition is present, transfer of Manchester-encoded data by the Transmit and Loopback functions is disabled.
g) Link Integrity Test function. Provides the ability to protect the network from the consequences of failure of the simplex link attached to the RD circuit. While such a failure is present, transfer of Manchester-encoded data by the Transmit, Receive, and Loopback functions is disabled.
h) Auto-Negotiation. Optionally provides the capability for a device at one end of a link segment to advertise its abilities to the device at the other end (its link partner), to detect information defining the abilities of the link partner, and to determine if the two devices are compatible.

14.2.1 MAU functions

The MAU shall provide the Transmit, Receive, Loopback, Collision Presence, Jabber, and Link Integrity Test functions for half duplex mode DTEs and repeater units. The MAU shall provide the Transmit, Receive, Jabber, and Link Integrity Test functions, and shall not provide the Loopback function for full duplex mode DTEs. The SQE Test function shall be performed by MAUs that are connected to half duplex DTEs and shall not be performed by MAUs that are connected to repeaters.

MAUs connected to full duplex mode DTEs are permitted, but not required, to implement the Collision Presence function, the SQE Test function, and the generation of the CS0 signal on the CI circuit by the Jabber function. If these optional capabilities are implemented in a MAU connected to a full duplex mode DTE, either all of the optional functions shall be implemented, or none of them shall be.

The MAU function requirements are summarized in the table below:

	MAU connected to:		
Functions	**Repeater**	**Half duplex DTE**	**Full duplex DTE**
Transmit	Required	Required	Required
Receive	Required	Required	Required
Loopback	Required	Required	Required
Jabber	Required	Required	Required
Link Integrity Test	Required	Required	Required
Collision Presence	Required	Required	Optional (Note 2)
SQE Test	Required	Required	Optional (Note 2)
Generation of CS0 signal on the CI circuit by jabber	Required	Required	Optional (Note 2)

NOTE 1—The functional requirements of a MAU connected to a full duplex DTE are a proper subset of the requirements for half duplex operation.

NOTE 2—Optional capabilities, if implemented, have to be implemented as a group (i.e., all or none).

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A capability may be provided in the MAU to activate or inhibit the SQE Test function, or to configure the MAU for full or half duplex operation. It is not required that a MAU determine that it is connected to either a DTE or a repeater and automatically activate or inhibit the SQE Test function. It is also not required that a MAU determine that it is connected to either a half duplex or full duplex DTE and automatically activate or inhibit the appropriate functions for those modes. The use of the Auto-Negotiation algorithm of Clause 28 in 10BASE-T MAUs is discussed in 14.2.1.8. The MAU may optionally provide the Auto-Negotiation algorithm. When provided, the Auto-Negotiation algorithm shall be implemented in accordance with Clause 28.

14.2.1.1 Transmit function requirements

The MAU shall receive the signals on the DO circuit and send them to the TD circuit of the MDI. A positive signal on the A lead relative to the B lead of the DO circuit shall result in a positive signal on the TD+ (Transmit Data +) lead of the MDI with respect to the TD– lead.

At the start of a packet transmission, no more than 2 bits may be received from the DO circuit and not transmitted on the TD circuit. In addition, it is permissible for the first bit sent to contain phase violations or invalid amplitude. All subsequent bits of the packet shall be reproduced with the differential voltage specified in 14.3.1.2.1 and with no more jitter than is specified in 14.3.1.2.3. The second bit transmitted on the TD circuit shall be transmitted with the correct timing and signal levels. The steady-state propagation delay between the DO circuit input and the TD circuit shall not exceed 2 BT.

For any two packets that are separated by 9.6 μs or less, the startup delay (bit loss plus steady-state propagation delay) of the first packet shall not exceed that of the second packet by more than 2 BT.

Whenever data is not being transmitted on the TD circuit, an idle signal, TP_IDL, shall be transmitted on the TD circuit. TP_IDL is a start of idle, as defined in 14.3.1.2.1, followed by a repeating sequence of a 16 ms ± 8 ms period of silence (the time where the differential voltage remains at 0 mV ± 50 mV) and a link test pulse (see 14.3.1.2.1). Following a packet and start of idle, the repeating sequence shall start with a period of silence.

Transmission of TP_IDL may be terminated at any time with respect to the link test pulse. It shall be terminated such that no more than the first transmitted bit of a packet is corrupted, and with no more delay than is specified for bit loss and steady-state propagation.

For a MAU that implements the Auto-Negotiation algorithm defined in Clause 28, Clause 28 shall define the allowable transmitted link pulse sequence.

14.2.1.2 Receive function requirements

The MAU shall receive the signals on the RD circuit of the MDI and send them to the DI circuit. A positive signal on the RD+ (Receive Data +) lead relative to the RD– lead of the MDI shall result in a positive signal on the A lead with respect to the B lead of the DI circuit.

At the start of a packet reception from the RD circuit, no more than 5 bits may be received on the RD circuit and not transmitted onto the DI circuit. In addition, it is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall be sent with no more than the amount of jitter specified in 14.3.1.3.1. The steady-state propagation delay between the RD circuit and the DI circuit shall not exceed 2 BT.

For any two packets that are separated by 9.6 μs or less, the startup delay of the first packet shall not exceed that of the second packet by more than 2 BT.

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14.2.1.3 Loopback function requirements (half duplex mode only)

When the MAU is transmitting on the TD circuit and is not receiving *RD_input* messages (14.2.2.4) on the RD circuit, the MAU shall transmit on the DI circuit the signals received on the DO circuit in order to provide loopback of the transmitted signal. At the start of packet transmission on the TD circuit, no more than 5 bits of information may be received from the DO circuit and not transmitted to the DI circuit. In addition, it is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall meet the jitter specified in 14.3.1.3.1 (that is, 13.5 ns plus 1.5 ns). The steady-state propagation delay between the DO circuit and the DI circuit shall not exceed 1 BT.

14.2.1.4 Collision Presence function requirements (half duplex mode only)

The MAU shall detect as a collision the simultaneous occurrence of activity on the DO circuit and the RD circuit while in the Link Test Pass state. While a collision is detected, a CS0 signal (see 7.3.1.2) shall be sent on the CI circuit. The signal shall be presented to the CI circuit no more than 9 BT after the occurrence of a collision. The signal shall be deasserted within 9 BT after the DO circuit or the RD circuit changes from active to idle.

When CS0 is asserted on the CI circuit due to a collision, the data on the RD circuit shall be sent to the DI circuit within 9 BT.

When the RD circuit changes from active to idle and data is present on the DO circuit, the data on the DO circuit shall be sent to the DI circuit within 9 BT.

The signal presented on the CI circuit in the absence of collision, SQE test, or Jabber shall be the IDL signal.

MAUs connected to full duplex mode DTEs are permitted, but not required, to implement the Collision Presence function (see 14.2.1).

14.2.1.5 *signal_quality_error* Message (SQE) Test function requirements

The SQE Test function shall be performed by MAUs that are connected to DTEs in half duplex mode, and shall not be performed by MAUs that are connected to repeaters. When the SQE test is performed, the MAU shall send CS0 on the CI circuit for a time “SQE_test” beginning a time “SQE_test_wait” after the last positive transition of a packet on the DO circuit. The value of “SQE_test” shall be 10 BT ± 5 BT and the value of “SQE_test_wait” shall be between 0.6 μs and 1.6 μs. This function should use as much of the normal collision detection and signaling circuitry as possible without introducing extraneous signals on the TD circuit or the DI circuit.

The CS0 signal shall not be sent by the SQE Test function while in any of the Link Test Fail states.

MAUs connected to full duplex mode DTEs are permitted, but not required, to implement the SQE Test function (see 14.2.1).

14.2.1.6 Jabber function requirements

The MAU shall contain a self-interrupt capability to prevent an illegally long transmission by a DTE from permanently disrupting transmission on the network and to disable loopback to the DI circuit (Figure 14–5). The MAU shall provide a window “xmit_max” during which time the Transmit function may continuously transmit *TD_output* messages to the TD circuit. The value of “xmit_max” shall be between 20 and 150 ms. If a transmission exceeds this duration, the Jabber function shall

a) Inhibit the Loopback function and the transmission of *TD_output* messages by the Transmit function, and shall

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b) Send the CS0 signal on the CI circuit, when the MAU is connected to a DTE operating in half duplex mode. MAUs connected to DTEs operating in full duplex mode are permitted, but not required, to send the CS0 signal on the CI circuit in this manner (see 14.2.1).

These actions shall continue until *output_idle* has been continuously present on the DO circuit for a time "unjab." The value of "unjab" shall be 0.5 s ± 0.25 s.

It is permissible to activate the Jabber function when the TD circuit transmitter is sending *TD_output* messages for longer than "xmit_max."

The MAU shall not activate its Jabber function when the repeater's MAU Jabber Lockup Protection function operates at its longest permitted time as specified in 9.6.5.

14.2.1.7 Link Integrity Test function requirements

In order to protect the network from the consequences of a simplex link segment failure, the MAU shall monitor the RD circuit for *RD_input* and link test pulse activity. If neither *RD_input* nor a link test pulse is received for a time "link_loss," the MAU shall enter the Link Test Fail state and cause the *input_idle* message to be sent on the DI circuit and the *TD_idle* message to be sent on the TD circuit (Figure 14–6). The value of "link_loss" shall be between 50 ms and 150 ms. When RD_input or a number "lc_max" of consecutive link test pulses is received on the RD circuit, the MAU shall exit the Link Test Fail state. The value of "lc_max" shall be between 2 and 10 inclusive.

Only link test pulses that occur within time "link_test_max" of each other shall be considered consecutive. The value of "link_test_max" shall be between 25 ms and 150 ms. In addition, detected pulses that occur within a time "link_test_min" of a previous pulse or packet shall be ignored while in the Link Test Pass state. In the Link Test Fail state, such pulses shall reset the counted number of consecutive link test pulses to zero. The value of "link_test_min" shall be between 2 ms and 7 ms. Re-enabling shall be deferred until the signals on the RD and DO circuits become idle. The MAU shall not detect a link test pulse as *RD_input*. Additionally, a MAU may exit the Link Test Fail Extend state and enter the Link Test Pass state when the RD circuit becomes idle and the Jabber function has disabled transmission on the TD circuit.

While the MAU is not in the Link Test Pass state, the Link Integrity Test function shall disable the bit transfer of the Transmit, Receive, and Loopback functions, and the Collision Presence and SQE Test functions.

At PowerOn, in place of entering the Link Test Pass state as shown in Figure 14–6, a MAU may optionally enter the Link Test Fail Reset state.

For a MAU that implements the Auto-Negotiation algorithm defined in Clause 28, the MAU shall enter the LINK TEST FAIL RESET state at power-on as specified in Clause 28. For a MAU that does not implement the Auto-Negotiation algorithm defined in Clause 28, it is highly recommended that it also power-on in the LINK TEST FAIL RESET state, although implementations may power-on in the LINK TEST PASS state. For a MAU that implements the Auto-Negotiation function defined in Clause 28, the Auto-Negotiation Technology Dependent Interface shall be supported. Supporting the Technology Dependent Interface requires that in the Link Integrity Test function state diagram "link_status=OK" is added to the LINK TEST PASS state and "link_status=FAIL" is added to the LINK TEST FAIL RESET state. Note these ISO message variables follow the conventions of Clause 21.

If a visible indicator is provided on the MAU to indicate the link status, it is recommended that the color be green and that the indicator be labeled appropriately. It is further recommended that the indicator be on when the MAU is in the Link Test Pass state and off otherwise.

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14.2.1.8 Auto-Negotiation

It is strongly recommended that Auto-Negotiation be used for the determination of half or full duplex operation. When Auto-Negotiation is used in an exposed AUI-based MAU implementation, the MAU has to be capable of operating in the half duplex mode, and shall not advertise the ability to operate in full duplex mode.

10BASE-T MAUs used in an embedded system (i.e., where the MAU is incorporated within the physical bounds of the DTE), or incorporating a physical implementation of the MII interface of Clause 22 with a DTE operating in full duplex mode, may indicate the capability to operate in full duplex mode using the Auto-Negotiation algorithm in accordance with Clause 28.

NOTE—Since there is no way to communicate the half or full duplex abilities between a DTE or repeater and a MAU separated by an AUI, caution should be used when connecting full duplex capable DTEs or MAUs that are manually configured.

Manual configuration is not recommended. Connecting incompatible DTE/MAU combinations such as a full duplex mode DTE to a half duplex mode MAU, or a full-duplex mode station (DTE and MAU) to a repeater or other half duplex network, can lead to severe network performance degradation, increased collisions, late collisions, CRC errors, and undetected data corruption.

14.2.2 PMA interface messages

The messages between the PLS in the DTE and the PMA in the MAU shall comply with the PMA interface messages described in 7.2.1. These messages also are used in repeater unit to PMA communication. These and the messages between the PMAs over the MDI are summarized below.

14.2.2.1 PLS to PMA messages

The following messages are sent by the PLS in the DTE or repeater to the PMA in the MAU:

Message	Circuit	Signal	Meaning
output	DO	CD1,CD0	Output information
output_idle	DO	IDL	No data to be output

14.2.2.1.1 PMA to PLS messages

The following messages are sent by the MAU to the PLS in the DTE or repeater:

Message	Circuit	Signal	Meaning
input	DI	CD1,CD0	Input information
input_idle	DI	IDL	No information to input
mau_available	CI	IDL	MAU is available for output
signal_quality_error	CI	CS0	Error detected by MAU

Retiming of CD1 and CD0 signals within the MAU is neither prohibited nor required. Considerable jitter may be present (see 14.3.1.3.1).

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14.2.2.2 PMA to twisted-pair link segment messages

Message	Circuit	Signal	Meaning
TD_output	TD	CD1,CD0	Output information
TD_idle	TD	TP_IDL	No information to output

The encoding for TP_IDL is defined in 14.2.1.1. The encoding for CD1 and CD0 is the same as that used on the AUI. Retiming of CD1 and CD0 signals within the MAU is neither prohibited nor required.

14.2.2.3 Twisted-pair link segment to PMA messages

Message	Circuit	Signal	Meaning
RD_input	RD	CD1,CD0	Input information
RD_idle	RD	TP_IDL	No information to input

The encoding for TP_IDL is defined in 14.2.1.1. The encoding for CD1 and CD0 is the same as that used on the AUI.

14.2.2.4 Interface message time references

Delay and bit loss specifications are measured from the occurrence of messages at the MDI and MAU AUI. The following describes the point where each message starts:

Message	Reference
output	leading bit cell boundary (BCB) of first valid CD1 or CD0
output_idle	last positive-going transition prior to start of IDL
input	leading BCB of first valid CD1 or CD0
input_idle	last positive-going transition prior to start of IDL
signal_quality_error	first transition of valid amplitude
mau_available	last positive-going transition prior to start of IDL
TD_output	leading BCB of first valid CD1 or CD0
TD_idle	last positive-going transition prior to start of TP_IDL
RD_output	leading BCB of first valid CD1 or CD0
RD_idle	last positive-going transition prior to start of TP_IDL

14.2.3 MAU state diagrams

The state diagrams of Figure 14–3a), Figure 14–3b), Figure 14–4, Figure 14–5, and Figure 14–6 depict the full set of allowed MAU state functions relative to the circuits of the AUI and MDI.

The notation used in the state diagrams follows the conventions in 1.2.1. The variables and timers used in the state diagrams are defined in the following subclauses.

14.2.3.1 State diagram variables

Variables are used in the state diagrams to indicate the status of MAU inputs and outputs, to control MAU operation, and to pass state information between functions.

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In the variable definitions, the name of the variable is followed by a brief description of the variable and a list of values the variable may take. For those variables that are state diagram outputs, one value will be identified as the default. The variable has the default value when no active state contains a term assigning a different value.

For example, the variable “xmit” has the value “disable” whenever the Jabber function or the Link Integrity Test function is in a state that asserts “xmit=disable.” The variable has the default value “enable” all other times.

The variables used in the state diagrams are defined as follows:

DI. Controls the signal sent by the MAU on the DI circuit.
Values:idle; MAU is sending *input_idle*, IDL (default).
DO; MAU sends the signal received on the DO circuit.
lpbk = disable overrides this and causes *input_idle* to be sent.
RD; MAU sends the signal received on the RD circuit.
rcv = disable overrides this and causes *input_idle* to be sent.

CI. Controls the signal sent by the MAU on the CI circuit.
Values:idle; MAU sends *mau_available*, IDL (default).
SQE; MAU sends *signal_quality_error*, CS0.

DO. Status of the signal received by the MAU on the DO circuit.
Values:idle; MAU is receiving *output_idle*, IDL.
active; MAU is receiving *output*, CD0 or CD1.

TD. Controls the signal sent by the MAU on the TD circuit.
Values:idle; MAU sends *TD_idle*, TP_IDL (default).
DO; MAU sends the signal received on the DO circuit.
xmit = disable overrides this and causes *TD_idle* to be sent.

RD. Status of the signal received by the MAU on the RD circuit.
Values:idle; MAU is receiving silence or a link test pulse.
active; MAU is detecting signals which meet the requirements of 14.3.1.3.2.

link_test_rcv. Status of the link test signal received by the MAU on the RD circuit.
Values:false; MAU is not detecting a link test pulse.
true; MAU is detecting a link test pulse.

link_count. Count of the number of consecutive link test pulses received while in the Link Fail state.
Values:non-negative integers.

lc_max. The number of consecutive link test pulses required before exit from the Link Fail state.
Values:positive integer between 2 and 10 inclusive.

rcv. Controls the path from the RD circuit to the DI circuit.
Values:enable; receive is enabled (default).
disable; the output to the DI circuit is *input_idle* when DI=RD.

lpbk. Controls the path from the DO circuit to the DI circuit.
Values:enable; loopback is enabled (default).
disable; the output to the DI circuit is *input_idle* when DI=DO.

xmit. Controls the path from the DO circuit to the TD circuit.
Values:enable; transmit is enabled (default).
disable; transmit is disabled and the signal sent on the TD circuit is TP_IDL.

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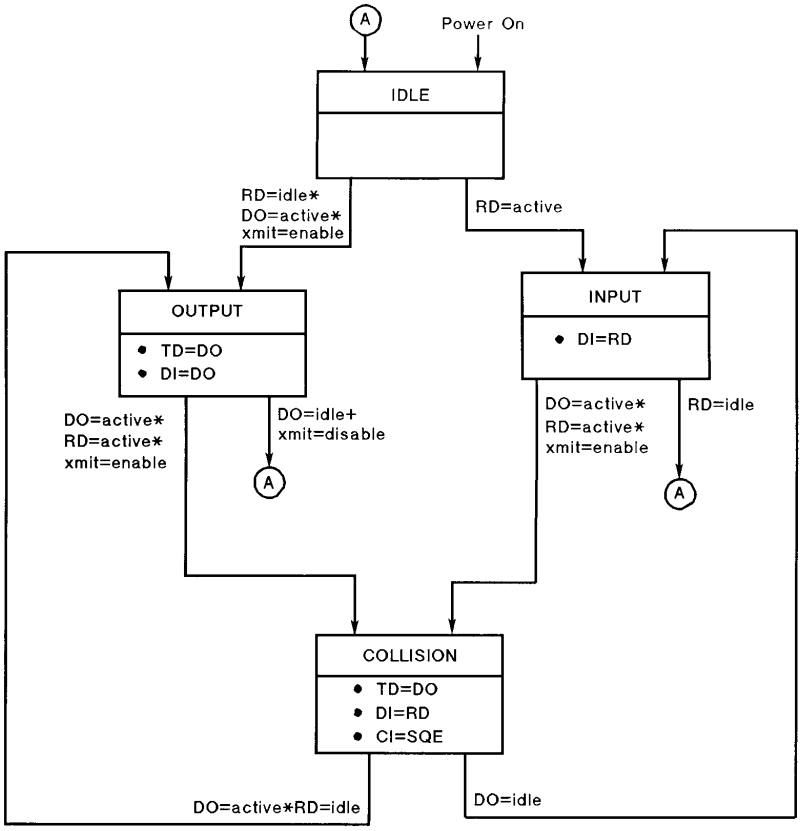
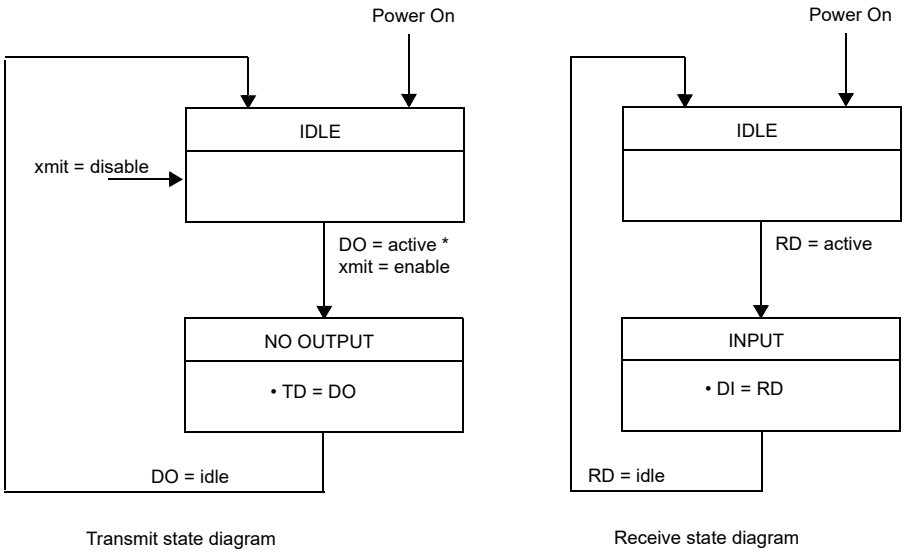


a) MAU Transmit, Receive, Loopback, and Collision Presence functions (half duplex mode)



b) MAU Transmit and Receive functions (full duplex mode)

Figure 14–3—MAU state diagrams

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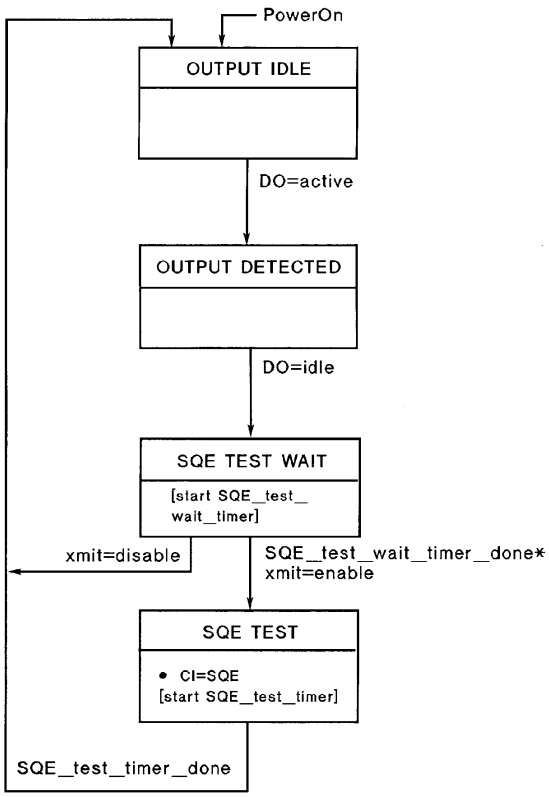

Figure 14–4—*signal_quality_error* Message Test function state diagram

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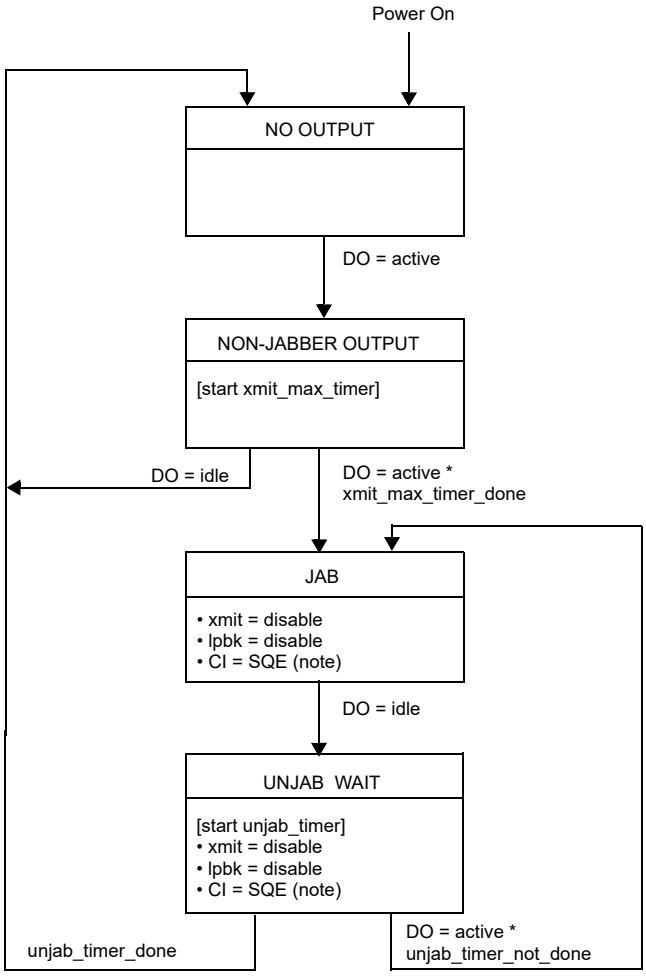

NOTE 1— Sending SQE on CI is optional for MAUs connected to DTEs operating in full duplex mode.

NOTE 2—The implementation of the Collision Presence function is not required in a MAU connected to a full duplex mode DTE, and is not shown in Figure 14–3b).

NOTE 3—The implementation of the SQE Test function shown in Figure 14–4 is not required in a MAU connected to a full duplex mode DTE.

NOTE 4—The enabling of the variable *lpbk* in Figure 14–6 is applicable only in half duplex mode.

Figure 14–5—Jabber function state diagram

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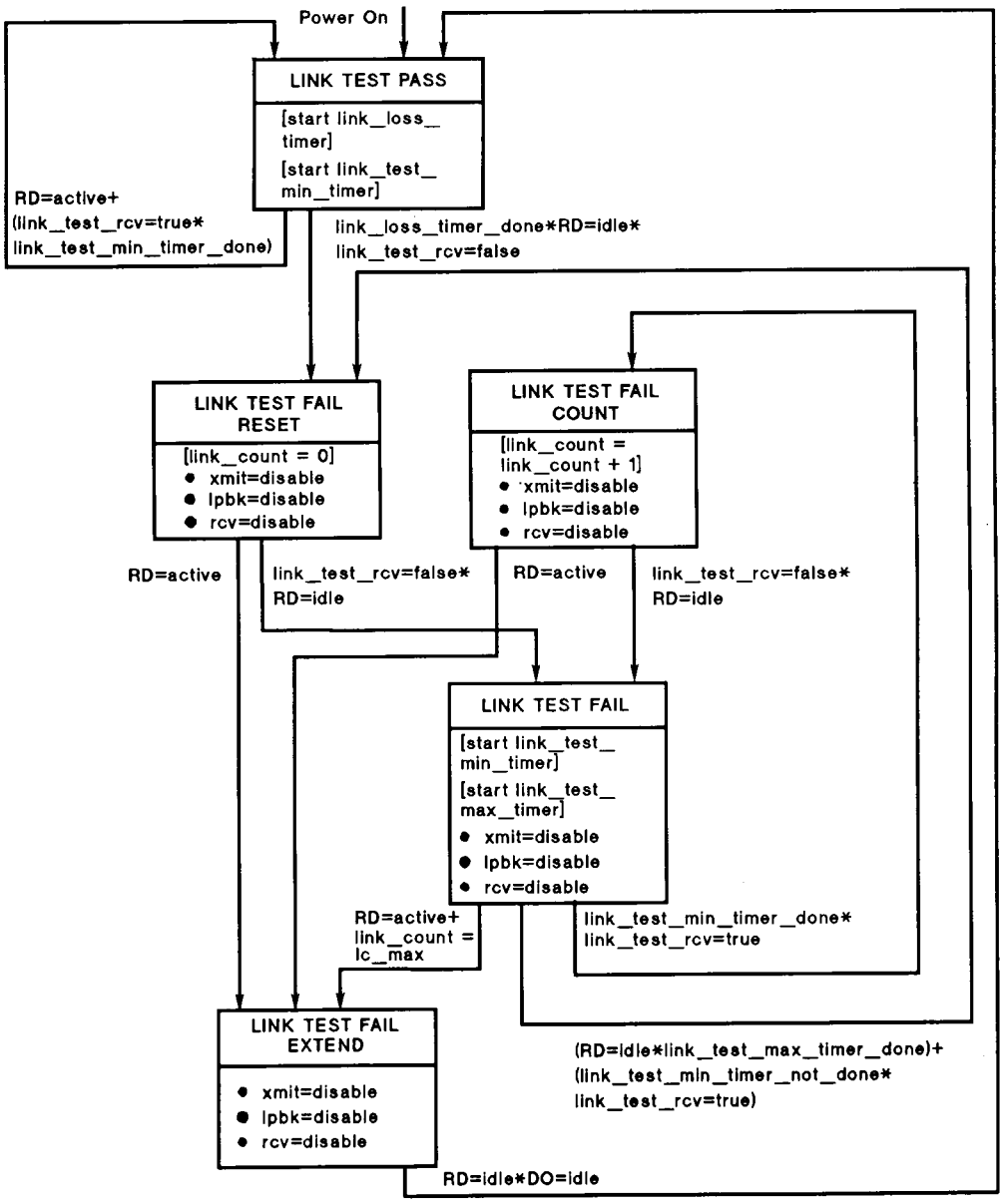

Figure 14–6—Link Integrity Test function state diagram

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14.2.3.2 State diagram timers

All timers operate in the same fashion. A timer is reset and starts counting upon entering a state where "start x_timer" is asserted. Time "x" after the timer has been started, "x_timer_done" is asserted and remains asserted until the timer is reset. At all other times, "x_timer_not_done" is asserted.

When entering a state where "start x_timer" is asserted, the timer is reset and restarted even if the entered state is the same as the exited state; for example, when in the Link Test Pass state of the Link Integrity Test function state diagram, the "link_loss_timer" and the "link_test_min_timer" are reset each time the term "RD = active + (link_test_rcv=true * link_test_min_timer_done)" is satisfied.

link_loss_timer. Timer for longest time input activity can be missing before the MAU determines that a link fail condition exists (14.2.1.7).

link_test_min_timer. Timer for the minimum time between valid link test pulses (14.2.1.7).

link_test_max_timer. Timer for maximum time input activity can be missing before Link Test Fail state is exited (14.2.1.7).

SQE_test_timer. Timer for the duration of the CS0 signal used for the SQE Test function (14.2.1.5).

SQE_test_wait_timer. Timer for the delay from end of packet to the start of the CS0 signal used for the SQE Test function (14.2.1.5).

unjab_timer. Timer for the length of time the DO circuit has to be continuously idle to allow transmission to be re-enabled (14.2.1.6).

xmit_max_timer. Timer for excessively long transmit time (14.2.1.6).

14.3 MAU electrical specifications

This subclause defines the electrical characteristics of the MAU at the MDI and the AUI. The MAU shall also meet the AUI requirements specified in Clause 7 when the AUI is implemented.

Additional information relative to conformance testing is given in B.4.3.

The ground for all common-mode tests is circuit PG, Protective Ground of the AUI. In implementations without an AUI, chassis ground is used as circuit PG. All components in test circuits shall be ±1% unless otherwise stated.

14.3.1 MAU-to-MDI interface characteristics

14.3.1.1 Electrical isolation

A MAU with a MDI that is a PI (see 33.1.3) shall meet the isolation requirements defined in 33.4.1 or 145.4.1.

A MAU with a MDI that is not a PI shall provide isolation between the DTE Physical Layer circuits including frame ground and all MDI leads including those not used by 10BASE-T.

This electrical isolation shall meet the isolation requirements as specified in J.1.

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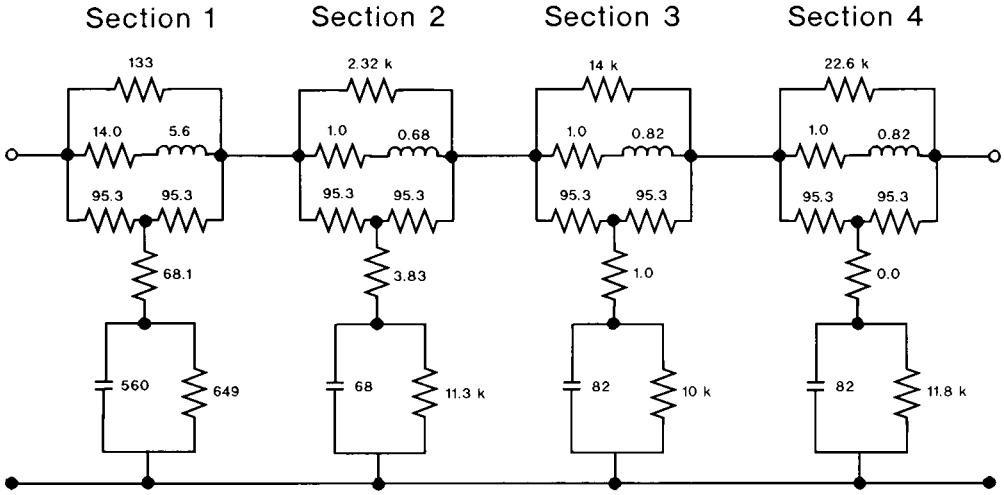
14.3.1.2 Transmitter specifications

The MAU shall provide the Transmit function specified in 14.2.1.1 in accordance with the electrical specifications of this subclause.

Where a load is not specified, the transmitter shall meet requirements of this subclause when connected to a 100 Ω resistive load. The use of 100 Ω terminations simplifies the measurement process when using 50 Ω measurement equipment as 50 Ω to 100 Ω impedance matching transformers are readily available.

Some tests in this subclause require the use of an equivalent circuit that models the distortion introduced by a simplex link segment. This twisted-pair model shall be constructed according to Figure 14–7 or a type 10BASE-T MAU that is not a type 10BASE-Te MAU and according to Figure 14–8 for a type 10BASE-Te MAU with component tolerances as follows: Resistors, ±1%; capacitors, ±5%; inductors, ±10%. Component tolerance specifications shall be met from 5.0 MHz to 15 MHz. For all measurements, the TD circuit shall be connected through a balun to section 1 and the signal measured across a load connected to section 4 of the model. The balun shall not affect the peak differential output voltage specified in 14.3.1.2.1 by more than 1% when inserted between the 100 Ω resistive load and the TD circuit. Also, the value of the resistor that is in series with the inductors includes the series resistance of the inductor itself. The actual value of the resistor that is used is computed by subtracting the series resistance of the inductor from the resistor value shown in the figure.

For a type 10BASE-T MAU that is not a type 10BASE-Te MAU, the insertion loss of the twisted-pair model when measured with a 100 Ω source and 100 Ω load shall be between 9.70 dB and 10.45 dB at 10 MHz, and between 6.50 dB and 7.05 dB at 5 MHz.



NOTE—Care should be taken that layout and parasitics do not exceed R, C, and L tolerance values.

Resistances are in Ω
Capacitances are in pF
Inductances are in μH

Figure 14–7—Twisted-pair model for 10BASE-T

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For a type 10BASE-Te MAU, the insertion loss of the twisted-pair model when measured with a 100 Ω source and 100 Ω load shall be between 6.8 dB and 7.4 dB at 10 MHz, and between 4.75 dB and 5.25 dB at 5 MHz.

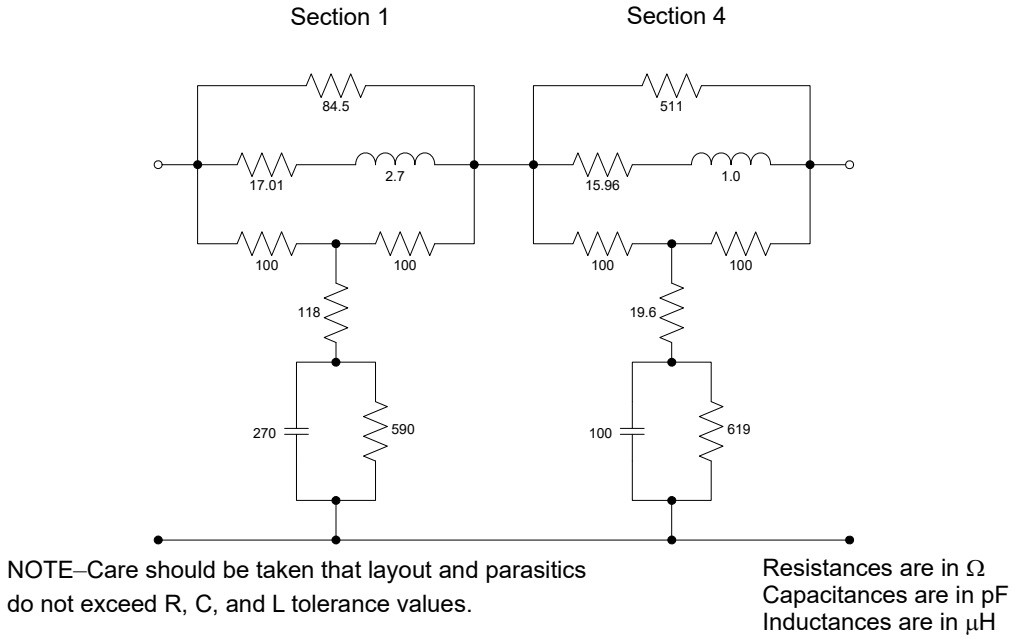

Figure 14–8—Twisted-pair model for 10BASE-Te

14.3.1.2.1 Differential output voltage

Some of the text and figures of this subclause describe the differential voltage in terms of magnitudes. These requirements apply to negative as well as positive pulses.

The peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 2.2 V and 2.8 V for all data sequences for a type 10BASE-T MAU that is not a type 10BASE-Te MAU. For a type 10BASE-Te MAU, the peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 1.54 V and 1.96 V for all data sequences. When the DO circuit is driven by an all-ones Manchester-encoded signal, any harmonic measured on the TD circuit shall be at least 27 dB below the fundamental.

NOTE—The specification on maximum spectral components is not intended to ensure compliance with regulations concerning RF emissions. The implementer should consider any applicable local, national, or international regulations. Additional filtering of spectral components may therefore be necessary.

The output signal V_o is defined at the output of the twisted-pair model as shown in Figure 14–9. The specific twisted-pair model used in Figure 14–9 shall be the equivalent circuit shown in Figure 14–7 for 10BASE-T except 10BASE-Te and shall be the equivalent circuit shown in Figure 14–8 for 10BASE-Te. The TD transmitter shall provide equalization such that the output waveform shall fall within the template shown in Figure 14–10 for all data sequences. Voltage and time coordinates for inflection points on Figure 14–10 are given in Table 14–1. (Zero crossing points are different for external and internal MAUs. The zero crossings depicted in Figure 14–10 apply to an external MAU.) The template voltage may be scaled by a factor of 0.9 to 1.1 but any scaling below 0.9 or above 1.1 shall not be allowed. The recommended measurement procedure is described in B.4.3.1. Time t = 0 on the template represents a zero crossing, with positive slope, of the output waveform. During this test the twisted-pair model shall be terminated in 100 Ω and driven by a

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transmitter with a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511

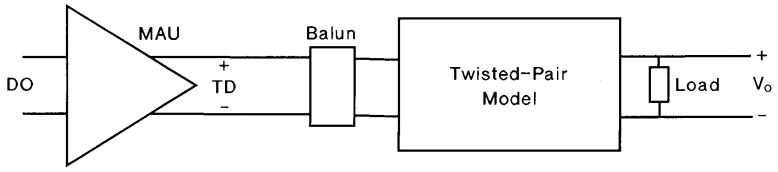

Figure 14–9—Differential output voltage test

bits.

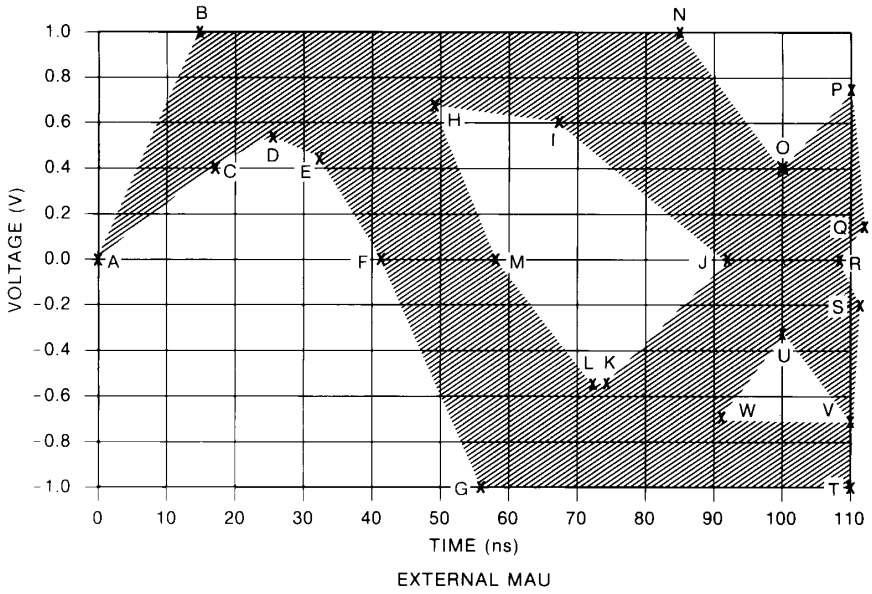

Figure 14–10—Voltage template

Table 14–1—Voltage template values for Figure 14–10

Reference	Time (ns)		Voltage (V)
	External MAU	Internal MAU	
A	0	0	0
B	15	15	1.0
C	15	15	0.4
D	25	25	0.55
E	32	32	0.45
F	42	39	0
G	57	57	–1.0
H	48	48	0.7
I	67	67	0.6
J	92	89	0
K	74	74	–0.55
L	73	73	–0.55
M	58	61	0
N	85	85	1.0
O	100	100	0.4
P	110	110	0.75
Q	111	111	0.15
R	108	111	0
S	111	111	–0.15
T	110	110	–1.0
U	100	100	–0.3

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Table 14–1—Voltage template values for Figure 14–10 *(continued)*

Reference	Time (ns)		Voltage (V)
	External MAU	Internal MAU	
V	110	110	–0.7
W	90	90	–0.7

This test shall be repeated with the template inverted about the time axis. In that case, t = 0 on the template represents a zero crossing, with negative slope, of the output waveform. When testing an external MAU the input waveform to the DO circuit of the MAU shall contribute no more than 0.5 ns of jitter. Adherence to this template does not verify that the requirements of 14.3.1.2.3 are met. (See B.4.3.3 for modification of the template to test jitter.)

The TP_IDL shall always start with a positive waveform when a waveform conforming to Figure 7–12 is applied to the DO circuit. If the last bit transmitted was a CD1, the last transition will be at the bit cell center of the CD1. If the last bit transmitted was a CD0, the PLS will generate an additional transition at the bit cell boundary following the CD0. After the zero crossing of the last transition, the differential voltage shall remain within the shaded area of Figure 14–11. Once the differential voltage has gone more negative than –50 mV, it shall not exceed +50 mV. The template requirements of Figure 14–11 shall be met when measured across each of the test loads defined in Figure 14–12, both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–9 for 10BASE-T except 10BASE-Te, and Figure 14–8 and Figure 14–9 for 10BASE-Te.

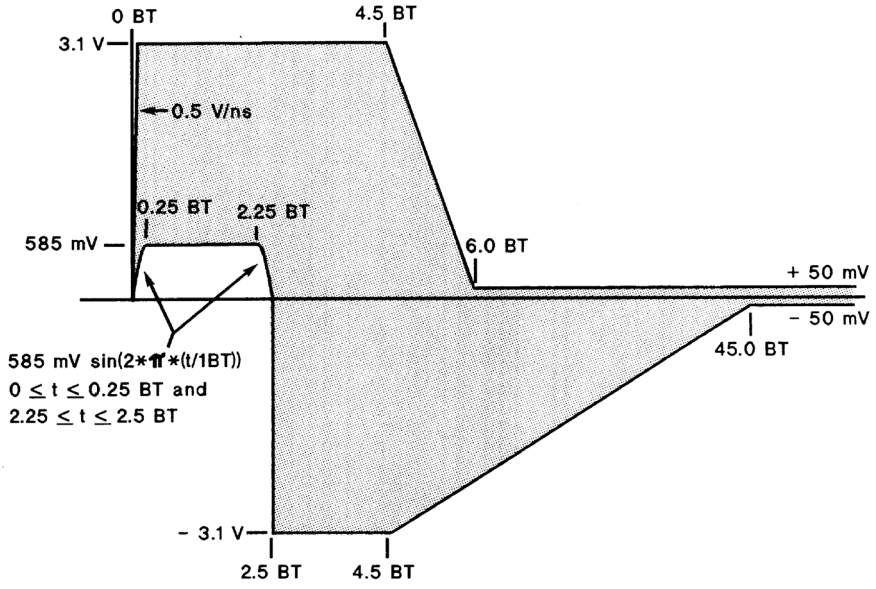

Figure 14–11—Transmitter waveform for start of TP_IDL

The link test pulse shall be a single positive (TD+ lead positive with respect to TD– lead) pulse, which falls within the shaded area of Figure 14–13. Once the differential output voltage has become more negative than –50 mV, it shall remain less than +50 mV. The template requirements of Figure 14–13 shall be met when measured across each of the test loads defined in Figure 14–12; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–9 for 10BASE-T except 10BASE-Te, and Figure 14–8 and Figure 14–9 for 10BASE-Te.

For a MAU that implements the Auto-Negotiation algorithm defined in Clause 28, the FLP Burst Sequence will consist of multiple link test pulses. All link test pulses in the FLP Burst sequence shall meet the

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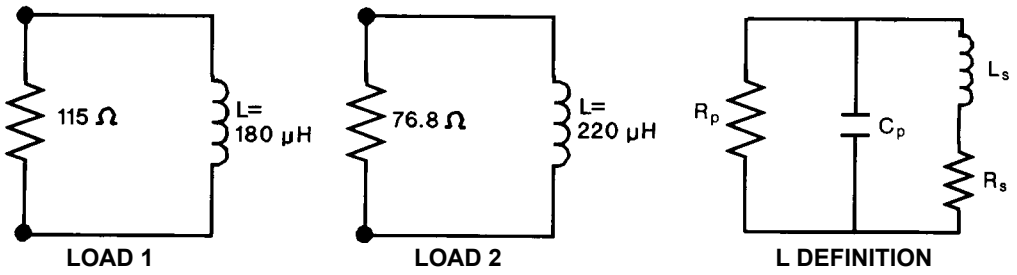

All parameters are defined over the frequency range of 250 kHz to 6 MHz.

$L_s = L \pm 1\%$ $R_p \geq 2\ k\Omega$
$C_p = 12\ pF \pm 20\%$ $R_s \leq 0.5\ \Omega$

Figure 14–12—Start-of-TP_IDL test load

template requirements of Figure 14–13 when measured across each of the test loads defined in Figure 14–12; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–9 for 10BASE-T except 10BASE-Te, and Figure 14–8 and Figure 14–9 for 10BASE-Te.

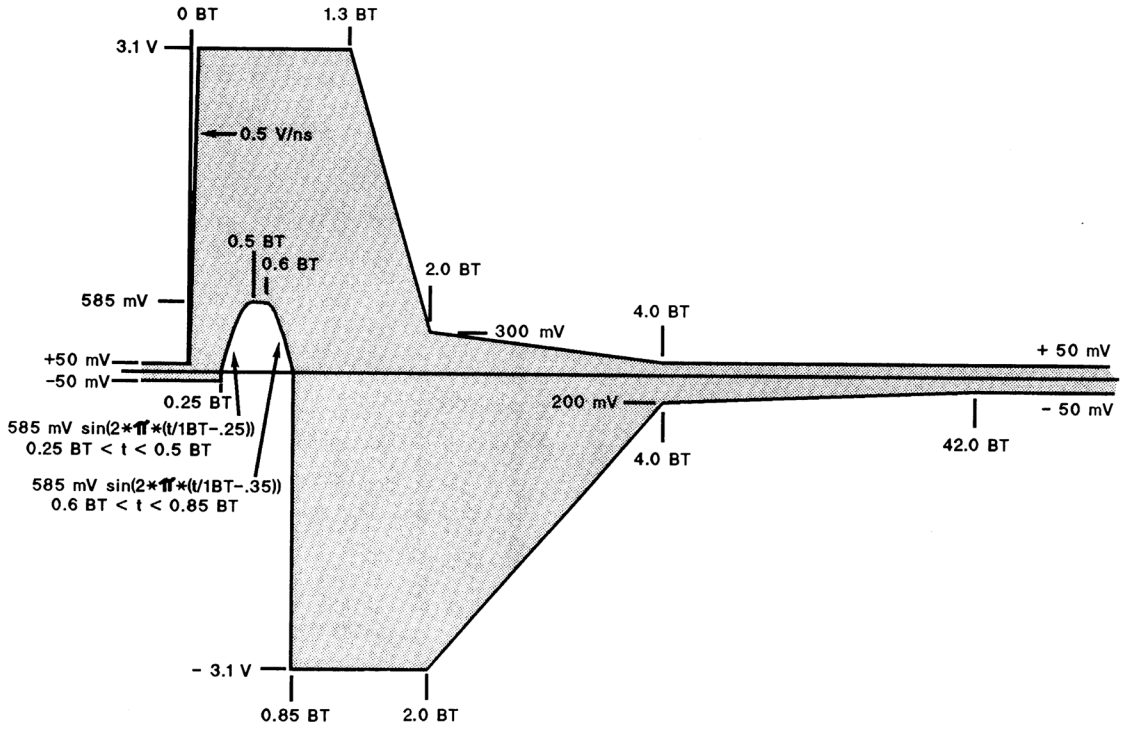

Figure 14–13—Transmitter waveform for link test pulse

14.3.1.2.2 Transmitter differential output impedance

The differential output impedance as measured on the TD circuit shall be such that any reflection, due to differential signals incident upon the TD circuit from a simplex link segment having any impedance within the range specified in 14.4.2.2, shall be at least 15 dB below the incident, over the frequency range of

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5.0 MHz to 10 MHz. This return loss shall be maintained at all times when the MAU is powered, including when the TD circuit is sending TP_IDL.

14.3.1.2.3 Output timing jitter

The transmitter output jitter is measured at the output of the twisted-pair model terminated in a 100 Ω load, as shown in Figure 14–9. The jitter added to the signal on the DO circuit as it propagates through the MAU and the twisted-pair model shall be no more than ±3.5 ns. Additionally, the MAU shall add no more than ±8 ns of jitter to the signal received on the DO circuit when the TD circuit is directly driving a 100 Ω resistive load.

14.3.1.2.4 Transmitter impedance balance

The common-mode to differential-mode impedance balance of the TD circuit shall exceed $29 - 17 \log_{10}(f/10)$ dB (where f is the frequency in MHz) over the frequency range 1.0 MHz to 20 MHz. This balance is defined as $20 \log_{10}(E_{cm}/E_{dif})$, where E_{cm} is an externally applied sine wave voltage as shown in Figure 14–14.

NOTE—The balance of the test equipment (such as the matching of the 147 Ω resistors) should exceed that required of the transmitter.

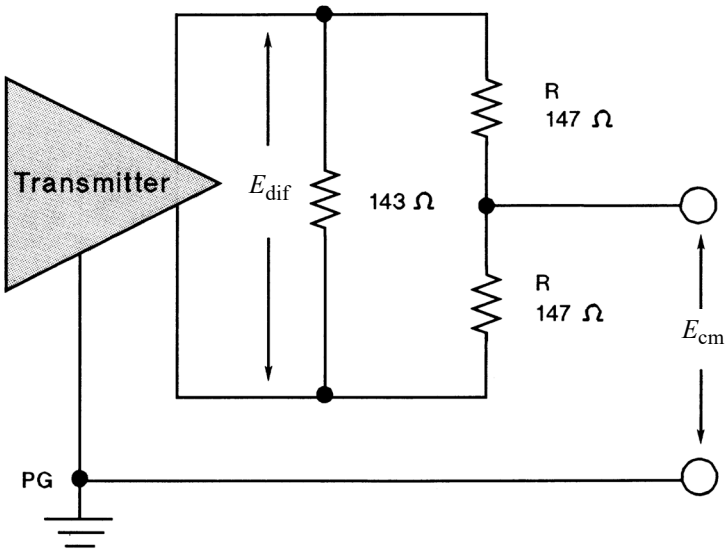

Figure 14–14—Transmitter impedance balance and common-mode rejection test circuit

14.3.1.2.5 Common-mode output voltage

The magnitude of the total common-mode output voltage of the transmitter, E_{cm}, measured as shown in Figure 14–15, shall be less than 50 mV peak at frequencies above 1 MHz.

NOTE—This specification is not intended to ensure compliance with regulations concerning RF emissions. The implementer should consider any applicable local, national, or international regulations. Driving unshielded twisted pairs with high-frequency, common-mode voltages may result in interference to other equipment.

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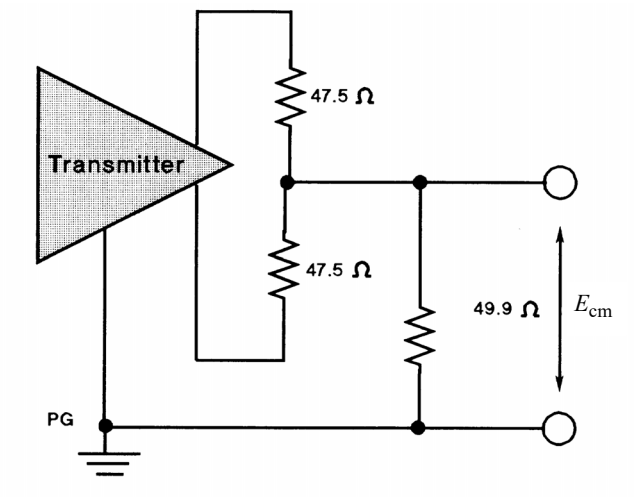

Figure 14–15—Common-mode output voltage test circuit

14.3.1.2.6 Transmitter common-mode rejection

The application of E_{cm}, as shown in Figure 14–14, shall not change the differential voltage at the TD circuit, E_{dif}, by more than 100 mV for all data sequences. Additionally, the edge jitter added by the application of E_{cm} shall be no more than 1.0 ns. E_{cm} shall be a 15 V peak 10.1 MHz sine wave.

14.3.1.2.7 Transmitter fault tolerance

Transmitters, when either idle or non-idle, shall withstand without damage the application of short circuits across the TD circuit for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

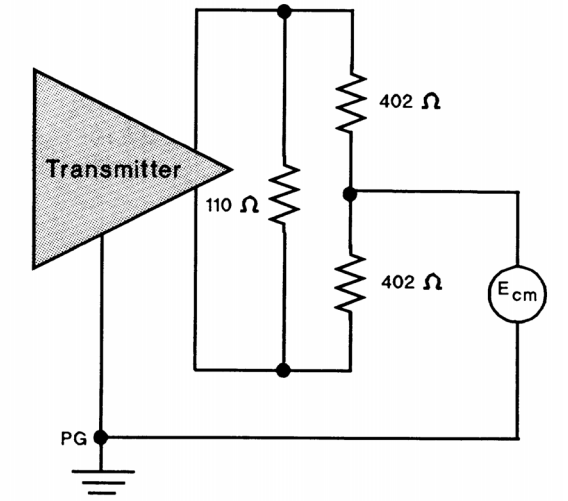

Figure 14–16—Transmitter fault tolerance test circuit

Transmitters, when either idle or non-idle, shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 14–16). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

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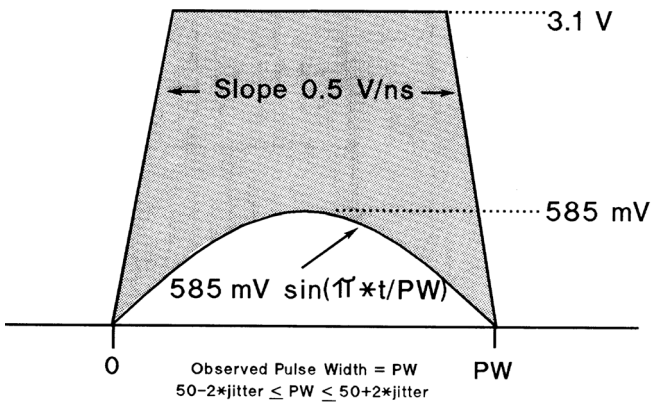

Figure 14–17—Receive differential input voltage—narrow pulse

14.3.1.3 Receiver specifications

The MAU shall provide the Receive function specified in 14.2.1.2 in accordance with the electrical specifications of this clause.

14.3.1.3.1 Receiver differential input signals

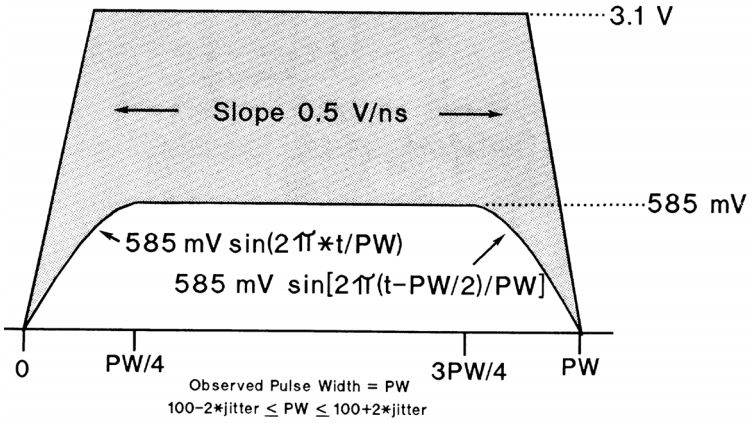

Figure 14–18—Receiver differential input voltage—wide pulse

Differential signals received on the RD circuit that are within the envelope of Figure 14–17 and Figure 14–18, and have a maximum zero crossing jitter up to ±13.5 ns from the ideal shall be sent to the DI circuit. The 13.5 ns includes jitter caused by an encoder, AUI cable and transmitting MAU, the twisted pair, and noise. Additionally, the MAU receiver shall add no more than ±1.5 ns jitter to the receive signal before sending the signal to the DI circuit.

14.3.1.3.2 Receiver differential noise immunity

The receiver, when presented with Manchester-encoded data meeting the requirements of 14.3.1.3.1, shall send this data to the DI circuit with a bit loss of no more than that specified in 14.2.1.2. In addition, the receiver, when presented with a signal meeting the requirements of 14.2.1.1 and within the envelope of Figure 14–13, shall accept it as a link test pulse.

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The receiver, while in the Idle state, shall reject as *RD_input* the following signals:

a) All signals that when measured at the output of the following filter would produce a peak magnitude less than 300 mV. The filter is a 3-pole low-pass Butterworth with a 3 dB cutoff at 15 MHz (refer to B.4.2).
b) All continuous sinusoidal signals of amplitude less than 6.2 V peak-to-peak and frequency less than 2 MHz.
c) All sine waves of single cycle duration, starting with phase 0 or 180 degrees, and of amplitude less than 6.2 V peak-to-peak where the frequency is between 2 MHz and 15 MHz. For a period of 4 BT before and after this single cycle, the signal shall be less than 300 mV when measured through the filter specified in a) above.

14.3.1.3.3 Idle input behavior

The idle condition shall be detected within 2.3 BT of the last low-to-high transition at the receiver. The receiver shall take precautions to ensure that the high-to-silence transition of the start of idle is not falsely interpreted as a silence-to-non-idle-transition, even in the presence of signal droop, overshoot, ringing, slow voltage decay, or a combination thereof due to capacitive and inductive effects in the transmitter, link segment, and receiver.

14.3.1.3.4 Receiver differential input impedance

The differential input impedance shall be such that any reflection, due to differential signals incident upon the RD circuit from a twisted pair having any impedance within the range specified in 14.4.2.2 shall be at least 15 dB below the incident over the frequency range of 5.0 MHz to 10 MHz. The return loss shall be maintained when the MAU is powered.

14.3.1.3.5 Common-mode rejection

Receivers shall assume the proper state on DI for any differential input signal E_s that results in a signal E_{dif} that meets 14.3.1.3.1 even in the presence of common-mode voltages E_{cm} (applied as shown in Figure 14–19). E_{cm} shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%–80%). Additionally, E_{cm} shall contribute no more than 2.5 ns of edge jitter to the signal transmitted on the DI circuit. The combination of the receiver timing jitter of 14.3.1.3.1 and the common-mode induced jitter are such that the MAU shall add no more than 4.0 ns of edge jitter to E_s before sending the signal on the DI circuit.

14.3.1.3.6 Receiver fault tolerance

The receiver shall tolerate the application of short circuits between the leads of the RD circuit for an indefinite period of time without damage and shall resume normal operation after such faults are removed. Receivers shall withstand without damage a 1000 V common-mode impulse of either polarity ($E_{impulse}$ as indicated in Figure 14–20). The shape of the impulse shall be 0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value), as defined in IEC 60060.

14.3.2 MAU-to-AUI specification

When a MAU contains a physical AUI connector, the following specifications shall be met.

14.3.2.1 MAU-AUI electrical characteristics

The electrical characteristics for the driver and receiver components within the MAU that are connected to the AUI shall be identical to those specified in 7.4 and 7.5. Additionally, the AUI DO receiver, while in the Idle state, shall reject an input waveform of less than ±160 mV differential.

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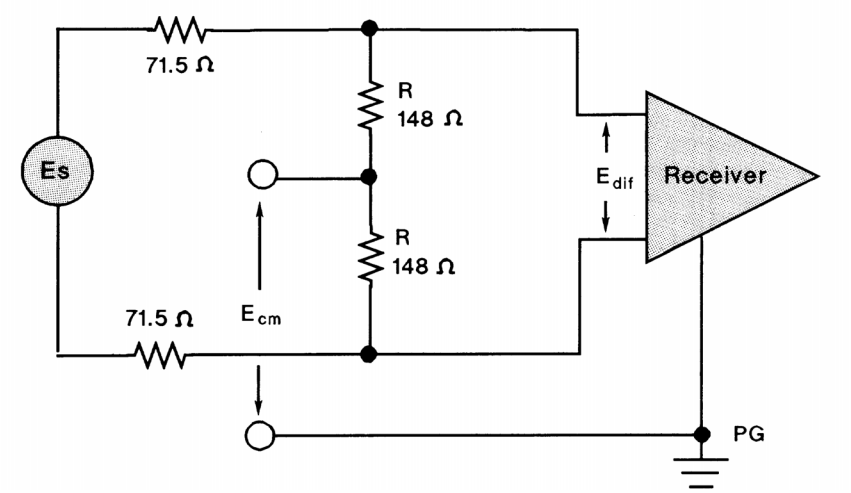

Figure 14–19—Receiver common-mode rejection test circuit

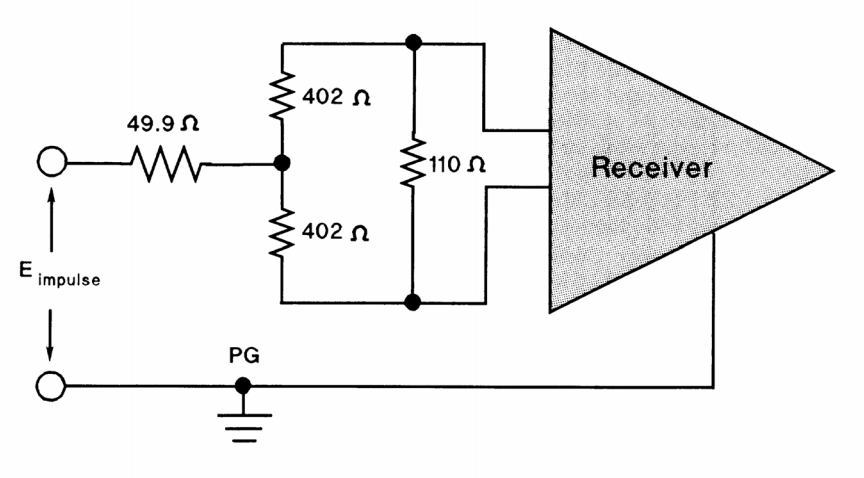

Figure 14–20—Common-mode impulse test circuit

14.3.2.2 MAU–AUI mechanical connection

The MAU shall be provided with a 15-pin male connector as specified in 7.6.

14.3.2.3 Power consumption

Following PowerOn, the surge current drawn by the MAU shall be such that $I_p \times T_w$ is less than or equal to 2×10^{-3} ampere-seconds, where I_p is the peak surge current and T_w is the time during which the current exceeds the larger of 0.5 A or $0.5 \times I_p$. After the 100 ms following PowerOn, the current drawn by the MAU shall not exceed 0.5 A when powered by the AUI.

The MAU shall be capable of operating from all possible voltage sources, including those current limited to 0.5 A, as supplied by the DTE or repeater through the resistance of all permissible AUI cables.

The MAU shall not introduce extraneous signals on the TD, CI, or DI circuits during normal power-up and power-down.

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14.4 Characteristics of the simplex link segment

Except where otherwise stated, the simplex link segment shall be tested with source and load impedances of 100 Ω.

14.4.1 Overview

The medium for 10BASE-T is twisted-pair wiring. A significant number of 10BASE-T networks are installed utilizing in-place unshielded telephone wiring and typical telephony installation practices, the end-to-end path including different types of wiring, cable connectors, and cross connects have to be considered. Typically, a DTE connects to a wall outlet using a twisted-pair patch cord. Wall outlets connect through building wiring and a cross connect to the repeater MAU in a wiring closet.

The medium for 10BASE-Te is twisted-pair wire. The requirements of the 10BASE-Te simplex link segment (either pure 10BASE-Te or mixed 10BASE-T, 10BASE-Te) are equivalent to the requirements of the Class D channel specified by ISO/IEC 11801:1995. This requirement can also be met by Category 5 cable and components as specified in ANSI/TIA/EIA-568-A.

NOTE—ISO/IEC 11801:2002 provides a specification for media that exceeds the minimum requirements of this standard.

14.4.2 Transmission parameters

Each simplex link segment shall have the following characteristics. All characteristics specified apply to the total simplex link segment unless otherwise noted. These characteristics are generally met by 100 m of twisted-pair cable composed of 0.5 mm [24 AWG] twisted pairs.

14.4.2.1 Insertion loss

The insertion loss of a simplex link segment shall be no more than 11.5 dB at all frequencies between 5.0 MHz and 10 MHz for a 10BASE-T MAU that is not a 10BASE-Te MAU. For a 10BASE-Te MAU, the insertion loss of a simplex link segment shall be no more than 8.5 dB at all frequencies between 5.0 MHz and 10 MHz. This consists of the attenuation of the twisted pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the simplex link segment. The insertion loss specification shall be met when the simplex link segment is terminated in source and load impedances that satisfy 14.3.1.2.2 and 14.3.1.3.4.

NOTE—Multipair PVC-insulated 0.5 mm [24 AWG] cable typically exhibits an attenuation of 8 dB to 10 dB/100 m at 20 °C. The loss of PVC-insulated cable exhibits significant temperature dependence. At temperatures greater than 40 °C, it may be necessary to use a less temperature-dependent cable, such as most plenum-rated cables.

14.4.2.2 Differential characteristic impedance

The magnitude of the differential characteristic impedance of a 3 m length of twisted pair used in a simplex link segment shall be between 85 Ω and 111 Ω for all frequencies between 5.0 MHz and 10 MHz. Since characteristic impedance tends to decrease with increasing frequency, the above requirement is generally implied by the condition that the magnitude of the characteristic impedance over the frequency band 1 MHz to 16 MHz is 100 Ω ± 15 Ω. Also, the magnitude of the input impedance averaged over the 5.0 MHz to 10 MHz frequency band of a simplex link segment terminated in 100 Ω shall be between 85 Ω and 111 Ω.

14.4.2.3 Medium timing jitter

Intersymbol interference and reflections due to impedance mismatches between tandem twisted pairs of a twisted-pair link segment and effects of connection devices can introduce jitter to the CD1 and CD0 signals

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received on the RD circuit. No more than ±5.0 ns of jitter shall be introduced to a test signal by a simplex link segment. The test signal shall have a peak amplitude of 3.0 V and 10% to 90% rise and fall times of 12 ns. The content of the test signal shall be a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

NOTE—Branches off a twisted pair (often referred to as "bridged taps" or "stubs") will generally cause excessive jitter and so should be avoided.

14.4.2.4 Delay

The maximum propagation delay of twisted pair shall be 5.7 ns/m (minimum velocity of $0.585 \times c$). The maximum propagation delay of a link segment shall not exceed 1000 ns.

14.4.3 Coupling parameters

To avoid excessive coupling of signals between twisted pairs of a twisted-pair cable, the crosstalk has to be limited. Crosstalk loss is specified for the twisted pairs in a twisted-pair cable or twisted-pair cable binder group that are used as 10BASE-T twisted-pair links. Crosstalk loss is specified with the far ends of both the disturbed and the disturbing pairs and the near end of the disturbed pair terminated in 100 Ω. Drivers of disturbing pairs shall have a source impedance of 100 Ω.

14.4.3.1 Differential near-end crosstalk (NEXT) loss

The NEXT loss between any two twisted pairs of a twisted-pair cable is dependent upon the geometry of the twisted-pair cable. Since the proximity of any two twisted pairs is influenced by the size of the twisted-pair cable, the NEXT loss is affected by twisted-pair cable size.

14.4.3.1.1 Twenty-five-pair cable and twenty-five-pair binder groups

The NEXT loss between any two twisted pairs in a twenty-five-pair twisted-pair cable or binder group used for 10BASE-T applications shall be at least $30 - 15 \log_{10}(f/10)$ dB (where f is the frequency in MHz) over the frequency range 5.0 MHz and 10 MHz.

14.4.3.1.2 Four-pair cable

The NEXT loss between any two twisted pairs in a four-pair twisted-pair cable used for 10BASE-T applications shall be at least $26 - 15 \log_{10}(f/10)$ dB (where f is the frequency in MHz) over the frequency range 5.0 MHz and 10 MHz.

14.4.3.1.3 Other cables

The NEXT loss requirement for all other twisted-pair cables shall be the multiple-disturber NEXT loss of 14.4.3.2.

14.4.3.2 Multiple-disturber NEXT (MDNEXT) loss

When a twisted-pair cable or twisted-pair cable binder group contains twisted pairs from multiple 10BASE-T twisted-pair link segments, the multiple-disturber crosstalk loss is dependent upon the specific selection of disturbing and disturbed pairs. For each 10BASE-T receive pair, MDNEXT is measured by having the remaining near-end transmit pairs (excluding the transmit pair associated with the receive pair under test) driven with identical and synchronized sine wave signals. MDNEXT may then be determined from the signal level observed on the receive pair under test. By examining all pair combinations with a fixed number of disturbers, a cumulative distribution of MDNEXT is obtained at each frequency of interest. The one percentile of this cumulative distribution shall be at least $23 - 15 \log_{10}(f/10)$ (where f is the frequency in

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MHz) at 5.0 MHz, 7.5 MHz, and 10 MHz. When the number of possible combinations allowed by a cable is fewer than 100, the MDNEXT loss for all combinations shall be at least $23 - 15 \log_{10}(f/10)$ (where f is the frequency in MHz) at 5.0 MHz, 7.5 MHz, and 10 MHz. Refer to 12.7.3.2 and B.3 for a tutorial and method for estimating the MDNEXT loss for a complete n-pair cable.

14.4.4 Noise environment

The noise level on the link segments shall be such that the objective error ratio is met. The noise environment consists generally of two primary contributors: crosstalk from other 10BASE-T circuits; and externally induced impulse noise, typically from telephone ringing and dialing signals, and other office and building equipment.

14.4.4.1 Impulse noise

The average rate of occurrence of impulses greater than 264 mV shall be less than or equal to 0.2/s as measured at the output of the following specified filter. Following the start of any particular impulse that is counted, any additional impulse shall be ignored for a period of 1 μs. The simplex link segment shall be terminated at the far end in 100 Ω. The filter is a 3-pole Butterworth low-pass with a 3 dB cutoff at 15 MHz (refer to B.4.2).

NOTE—Typically, the impulse noise occurrence rate changes inversely by one decade for each 5 dB to 9 dB change in the threshold voltage. If a count rate of N counts/s is measured on a specific twisted pair and filter at the specified voltage threshold, the media noise margin is approximately $7 \log_{10}(0.2/N)$ dB. Impulse noise may be a burst phenomenon and should be measured over an extended period of time.

14.4.4.2 Crosstalk noise

The level of crosstalk noise on a simplex link segment depends on the level of the disturbing signal(s) and the crosstalk loss between the pair(s) carrying the signal(s) and the disturbed pair. With the maximum transmit level (14.3.1.2), the sinusoidal crosstalk loss (14.4.3.2), and multiple, random Manchester-encoded disturbers, the peak self-crosstalk noise levels as measured at the output of the following specified filter shall be less than or equal to 264 mV. The filter is a 3-pole Butterworth low-pass with a 3 dB cutoff at 15 MHz (refer to B.4.2).

14.5 MDI specification

This subclause defines the MDI for the twisted-pair link segment. The link topology requires a crossover function between PMAs. Implementation and location of this crossover is also defined in this clause.

14.5.1 MDI connectors

Eight-pin connectors meeting the requirements of Clause 3 and Figures 1 through 5 of IEC 60603-7:1990 shall be used as the mechanical interface to the twisted-pair link segment. The plug connector shall be used on the

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twisted-pair link segment and the jack on the MAU. These connectors are depicted (for informational use only) in Figure 14–21 and Figure 14–22. The following table shows the assignment of signals to connector contacts.

Contact	MDI signal
1	TD+
2	TD–
3	RD+
4	Not used by 10BASE-T
5	Not used by 10BASE-T
6	RD–
7	Not used by 10BASE-T
8	Not used by 10BASE-T

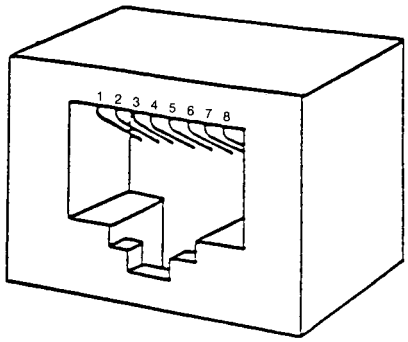

Figure 14–21—MAU MDI connect

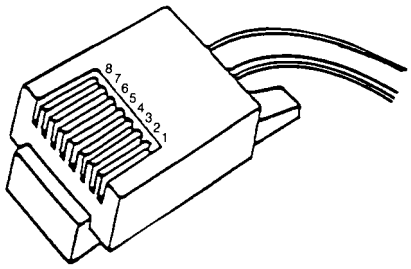

Figure 14–22—Twisted-pair link segment connector

14.5.2 Crossover function

A crossover function shall be implemented in every twisted-pair link. The crossover function connects the transmitter of one MAU to the receiver of the MAU at the other end of the twisted-pair link. Crossover functions may be implemented internally to a MAU or elsewhere in the twisted-pair link. For MAUs that do not implement the crossover function, the signal names of 14.5.1 refer to their own internal circuits. For MAUs that do implement the crossover function, the signal names refer to the remote MAU of the twisted-pair link. Additionally, the MDI connector for a MAU that implements a fixed crossover function shall be marked with the graphical symbol “X”. Internal and external crossover functions are shown in Figure 14–23.

When a twisted-pair link connects a DTE to a repeater, it is recommended that the crossover be implemented in the MAU local to the repeater. If both MAUs of a twisted-pair link contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the MAUs. When both MAUs contain internal crossovers, it is further recommended in networks in which the topology identifies either a central backbone segment or a central hub that the MAU furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable, or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

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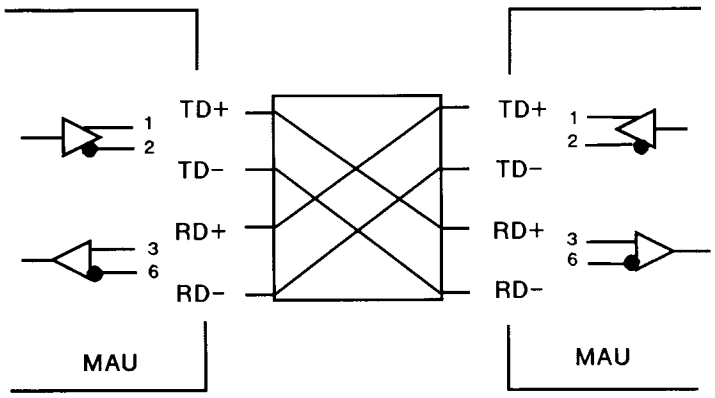
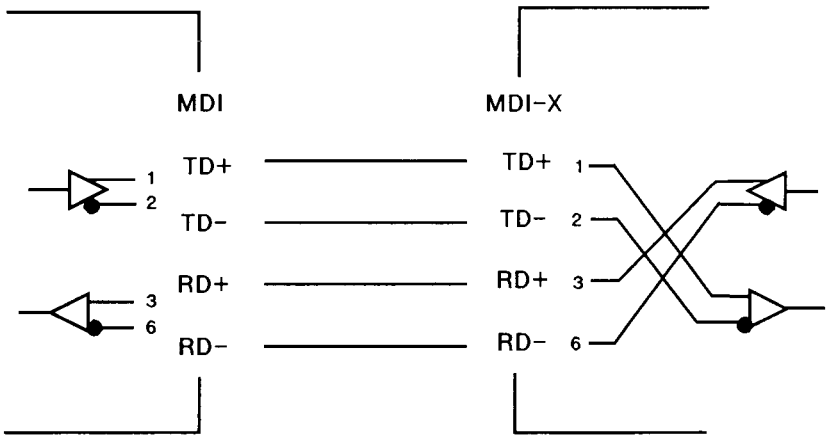


a) External Crossover function



b) MAU-Embedded Crossover function

Figure 14–23—Crossover function

14.6 System considerations

The repeater unit specified in Clause 9 forms the central unit for interconnecting 10BASE-T twisted-pair links in networks of more than two nodes. It also provides the means for connecting 10BASE-T twisted-pair links to other 10 Mb/s baseband segments. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of the interpacket gap as it travels through the network. Configuration rules, which ensure that these limits are not exceeded, are given in Clause 13.

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14.7 Environmental specifications

14.7.1 General safety

An MAU meeting this standard shall conform to the general safety requirements in J.2.

14.7.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cables and components.
c) High-energy transients coupled onto the LAN cable system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards have to be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures have to be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network. Isolation requirements are defined in 14.3.1.1.

14.7.2.1 Installation

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

14.7.2.2 Grounding

Any safety grounding path for the MAU shall be provided through the circuit PG of the AUI connection.

WARNING

It is assumed that the equipment to which the MAU is attached is properly earthed, and not left floating nor serviced by a “doubly insulated ac power distribution system.” The use of floating or insulated equipment, and the consequent implications for safety are beyond the scope of this standard.

14.7.2.3 Installation and maintenance guidelines

During installation and maintenance of the cable plant, care shall be taken to ensure that uninsulated network cable conductors do not make electrical contact with unintended conductors or ground.

14.7.2.4 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 10BASE-T equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the “battery” and ringing voltages. Although there is no universal standard, the following maximums generally apply.

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Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.

Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 Vdc with a 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 10BASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 10BASE-T transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

14.7.3 Environment

14.7.3.1 Electromagnetic emission

The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

14.7.3.2 Temperature and humidity

The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the MAU the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the twisted-pair link segment, the distance and operating environmental conditions over which the specifications of 14.4 will be met.

14.8 MAU labeling

It is recommended that each MAU (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in Mb/s,
b) Power level in terms of maximum current drain (for external MAUs),
c) Any applicable safety warnings,
d) Duplex capabilities, and
e) Which of the two specifications is implemented, i.e., 10BASE-T or 10BASE-Te (not both).

See also 14.5.2.

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14.9 Timing summary

Table 14–2 summarizes the timing requirements for the 10BASE-T twisted-pair link. This table is a summary; for complete descriptions of the timing requirements, refer to the referenced subclauses.

Table 14–2—Maximum timing parameters

Symbol	Function	Bit loss[a]	Invalid bits[b]	Steady-state propagation delay[b]	Startup delay[b]		Specified in
					Maximum	Variability	
M1	*RD_input* to *input* on DI	5.0	1.0	2.0	8.0	2.0	14.2.1.2
M2	*output* on DO to *TD_output*	2.0	1.0	2.0	5.0	2.0	14.2.1.1
M3	*RD_input* * *output* to *signal_quality_error*	—	—	—	9.0	—	14.2.1.4
M4	*RD_idle* + *output_idle* (end of collision) to *mau_available*	—	—	—	9.0	—	14.2.1.4
M5	*RD_input* * *output* to *input* on DI from circuit RD	—	—	—	9.0	—	14.2.1.4
M6	*RD_idle* * *output* to *input* on DI from circuit DO	—	—	—	9.0	—	14.2.1.4
M7	*output_idle* on DO to *signal_quality_error*	—	—	—	6 < x < 16	—	14.2.1.5
M8	*signal_quality_error* duration for SQE test	—	—	—	5 < x < 15	—	14.2.1.5
M9	*output* on DO to *input* on DI	5.0	1.0	1.0	7.0	—	14.2.1.3
T1	twisted-pair propagation	0	0	10.00	10.00	—	14.4.2.4
A1	AUI cable propagation (50 m)	0	0	2.57	2.57	—	7.4.3.7

[a]All time in BT.
[b]For an explanation of the meaning of variability, see 14.2.1.1 and 14.2.1.2.

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14.10 Protocol implementation conformance statement (PICS) proforma for Clause 14, Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T and type 10BASE-Te[45]

14.10.1 Introduction

To evaluate conformance of a particular implementation, it is necessary to state which capabilities and options have been implemented for a given OSI protocol. Such a statement is called a protocol implementation conformance statement (PICS).

This PICS proforma defines conformance requirements for type 10BASE-T MAU implementations. When the supplier completes this proforma, this document becomes the PICS for the specified implementation. The PICS is then used to perform a static conformance review of the implementation to determine that all mandatory features are implemented and that all conditional features are correctly supported dependent on the options claimed to be implemented. The PICS is used also as an aid in test-case selection and result analysis during the dynamic conformance testing.

Separate MAU and link segment implementations are expected; submissions of either for testing do not require submission of the other. Furthermore, there is no current intention to produce an Abstract Test Suite from the subclause of the PICS proforma that discusses the link segment.

14.10.1.1 Scope

This subclause provides the PICS proforma for type 10BASE-T MAU specifications in accordance with the relevant guidance given in ISO/IEC 9646-2.

14.10.1.2 Reference

Type 10BASE-T MAU requirements referenced in this PICS proforma are found in 14.2 through 14.8 and in 7.3 through 7.6 of this standard. Subclauses 7.3 through 7.6 and 14.2 through 14.8 take precedence over 14.10 in case of any conflict.

The use and the requirements for PICS proforma are defined in ISO/IEC 9646-1 and ISO/IEC 9646-2.

14.10.1.3 Definitions

This document uses the following terms defined in ISO/IEC 9646-1:

PICS proforma
protocol implementation conformance statement (PICS)
static conformance review
dynamic conformance testing

14.10.1.4 Conformance

The supplier of a MAU that is claimed to conform to type 10BASE-T MAU specifications shall complete a copy of the PICS proforma provided in this document and shall provide the information necessary to identify both the supplier and the implementation.

[45] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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14.10.2 Identification of implementation

The MAU supplier shall complete the relevant fields in this subclause to identify the supplier and the particular MAU.

14.10.2.1 Supplier information

The MAU supplier shall complete the relevant fields in this subclause to identify the supplier and the particular MAU.

Company name:	
Representative name:	
Address:	
Phone:	
Fax:	
E-mail:	

14.10.2.2 Implementation information

Implementation name:	
Implementation identifier (including version/release):	

14.10.3 Identification of the protocol

The supplier will complete this subclause to identify the precise protocol implemented.

Check Y [ ] if the MAU identified in the previous subclause implements the following protocol standard; check N [ ] if otherwise and attach an explanation.

IEEE Std 802.3-2018,Clause 14, Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T except type 10BASE-Te	Y [ ]	N [ ]
IEEE Std 802.3-2018, Clause 14, Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-Te	Y [ ]	N [ ]

List any other addenda or amendment documents implemented.

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14.10.4 PICS proforma for 10BASE-T

14.10.4.1 Abbreviations

The following abbreviations are used in the PICS proforma tables:

Req=Requirement. This column indicates whether the conformance requirement of a particular clause in the standard is mandatory, optional, or conditional.
Imp=Implementation. This column is filled in for a particular implementation with a "Y" or an "N" to indicate claimed conformance.
M=Mandatory. Conformance cannot be met unless the parameter is implemented as specified.
O=Optional. The parameter may be implemented or not but, if implemented, it has to be as stated in the standard.
C=Conditional. If an associated major option is implemented, this parameter has to be implemented.

NOTE—Recommendations in the standard become "Optional" parameters in the context of a PICS proforma.

14.10.4.2 PICS Completion instructions and implementation statement

A supplier wishing to submit a 10BASE-T MAU for conformance testing against this standard has to fill in the column headed "Imp" in the PICS proforma tables and submit the resulting PICS with the equipment for test. This column has to be filled in either with a "Y" for yes, indicating that the implementation is intended to meet the particular mandatory or optional requirement, or "N" for no, indicating that the option has not been implemented (or enabled where switchable) or that the requirement is not met. It should be noted that any instances of "N" entered against a mandatory requirement will result in the implementation failing the static conformance test. In addition, the supplier should indicate below whether or not the implementation implements all the mandatory requirements.

This implementation implements all mandatory requirements	Y [ ]	N [ ]

14.10.4.3 Additional information

Any additional information that is needed to ensure that the MAU or link segment submitted for test is configured as a 10BASE-T MAU or link segment should be entered into the PIXIT (Protocol Implementation eXtra Information for Testing) document supplied by the conformance testing organization. Relevant information on 10BASE-T MAUs or link segments includes the following:

a) Enable/disable mechanisms for SQE Test
b) Enable/disable mechanisms for features that allow compatibility with nonstandard implementations
c) Operational instructions for DTEs or repeaters in cases where the MAU is embedded
d) Environmental conditions
e) Input voltage range for implementations with embedded MAUs

The above list is illustrative and is not intended to be either mandatory or exhaustive.

14.10.4.4 References

ISO/IEC 9646-2 requires that all PICS proforma clauses be individually identified. Tables have subclause headings and numbered clauses in order to meet this requirement.

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14.10.4.5 PICS proforma tables for MAU

14.10.4.5.1 MAU functions

	Parameter	Subclause	Req	Imp	Value/Comment
	MAU functions:	14.2.1			
MF1	Transmit		M		
MF2	Receive		M		
MF3	Loopback		C		Function performed by MAUs attached to half duplex mode DTEs and repeaters, not performed by MAUs attached to full duplex mode DTEs.
MF4	Collision Presence		C		Function performed by MAUs attached to half duplex mode DTEs and repeaters, optionally performed by MAUs attached to full duplex mode DTEs that fully support this option as described in 14.2.1.
MF5	Jabber		M		
MF6	Link Integrity Test		M		
MF7	SQE Test		C		Function performed by MAUs attached to half duplex DTEs, optionally performed by MAUs attached to full duplex DTEs that fully support this option as described in 14.2.1, not performed by MAUs attached to repeaters.
MF8	Auto-Negotiation		C		Function provided by MAUs implementing the Auto-Negotiation algorithm, as defined in Clause 28.

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14.10.4.5.2 Transmit function

	Parameter	Subclause	Req	Imp	Value/Comment
TF1	Transmit path	14.2.1.1	M		DO circuit to TD circuit
TF2	Transmit signal polarity	14.2.1.1	M		DO A positive relative to DO B causes TD+ positive relative to TD–
TF3	Startup bit loss (DO to TD circuits)	14.2.1.1	M		2 bits max
TF4	Transmit settling time	14.2.1.1	M		Second and following bits meet amplitude and jitter specifications
TF5	Transmit steady-state delay	14.2.1.1	M		2 bit times max
TF6	Transmit delay variability	14.2.1.1	M		2 bit times max
TF7	TP_IDL	14.2.1.1	M		Start of idle followed by a repeating sequence of silence and link test pulse
TF8	Silence duration	14.2.1.1	M		16 ms ± 8 ms, ≤ ±50 mV
TF9	TP_IDL termination with respect to start of packet	14.2.1.1	M		Normal start of packet requirements apply

14.10.4.5.3 Receive function

	Parameter	Subclause	Req	Imp	Value/Comment
RF1	Receive path	14.2.1.2	M		RD circuit to DI circuit
RF2	Receive signal polarity	14.2.1.2	M		RD+ positive relative to RD– causes DI A positive relative to DI B
RF3	Startup bit loss (RD to DI circuits)	14.2.1.2	M		5 bits max
RF4	Receive settling time	14.2.1.2	M		Second and following bits meet jitter specifications
RF5	Receive steady-state delay	14.2.1.2	M		2 bit times max
RF6	Receive delay variability	14.2.1.2	M		2 bit times max

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14.10.4.5.4 Loopback function

The following are conditional based on whether the Loopback function is to be performed (14.10.4.5.1, item MF3).

	Parameter	Subclause	Req	Imp	Value/Comment
BF1	Loopback function requirements when RD = idle and DO = active	14.2.1.3	C		DO signals to DI circuit
BF2	Loopback bit loss (DO to DI circuits)	14.2.1.3	C		5 bits max
BF3	Loopback settling time	14.2.1.3	C		Second and following bits meet jitter specifications
BF4	Loopback steady-state delay	14.2.1.3	C		1 bit time max

14.10.4.5.5 Collision Detect function

The following are conditional based on whether the Collision Presence function is to be performed (14.10.4.5.1, item MF4).

	Parameter	Subclause	Req	Imp	Value/Comment
CF1	Collision Presence function requirements	14.2.1.4	C		CS0 on CI circuit if DO=active, RD=active and in Link Test Pass state
CF2	Collision indication delay	14.2.1.4	C		9 bit times max
CF3	Collision indicate de-assert delay	14.2.1.4	C		9 bit times max
CF4	CI circuit with no collision, SQE Test, or jabber	14.2.1.4	C		IDL signal
CF5	DI circuit source switch delay from CS0 assert	14.2.1.4	C		9 bit times max
CF6	DI circuit source switch delay from CS0 de-assert	14.2.1.4	C		9 bit times max

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14.10.4.5.6 *signal_quality_error* Message Test function

The following are conditional based on whether the *signal_quality_error* Message Test is to be performed (14.10.4.5.1, item MF7).

	Parameter	Subclause	Req	Imp	Value/Comment
SF1	SQE Test induced TD or DI circuit signals	14.2.1.5	C		No extraneous signals permitted
SF2	SQE_test _wait timer range	14.2.1.5	C		0.6 μs to 1.6 μs
SF3	SQE_test timer range	14.2.1.5	C		5 to 15 bit times
SF4	CI circuit during SQE Test	14.2.1.5	C		CS0 signal
SF5	SQE Test in Link Fail state	14.2.1.5	C		CS0 is not sent

14.10.4.5.7 Jabber function

	Parameter	Subclause	Req	Imp	Value/Comment
JF1	Jabber Function implementation	14.2.1.6	M		Self-interrupt of transmit and loopback
JF2	Xmit_max timer range	14.2.1.6	M		20 ms min, 150 ms max
JF3	CI circuit during jabber	14.2.1.6	M		CS0 signal
JF4	Unjab timer range	14.2.1.6	M		0.5 s ± 0.25 s
JF5	MAU Jabber Lockup Protection	14.2.1.6	M		Jabber not activated by the longest permitted output specified in 9.6.5

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14.10.4.5.8 Link Integrity Test function

	Parameter	Subclause	Req	Imp	Value/Comment
LF1	Link_loss timer	14.2.1.7	M		50 ms min, 150 ms max
	Signals during detected failure:	14.2.1.7			
LF2	TD circuit		M		TP_IDL
LF3	DI circuit		M		IDL
LF4	CI circuit		M		IDL (except when jabber condition is also present)
LF5	Link Test Fail state exit conditions	14.2.1.7	M		RD = active or consecutive link test pulses = 2 min, 10 max
LF6	Link_test_min timer range	14.2.1.7	M		2 ms to 7 ms
LF7	Link_test_max timer range	14.2.1.7	M		25 ms to 150 ms
	Pulses outside acceptance window:	14.2.1.7			
LF8	Early while in Link Test Pass state		M		Ignore
LF9	Early or late while not in Link Test Pass state		M		Reset link test pulse counter
	Link fail effect on MAU functions:	14.2.1.7			
LF10	Transmit		M		Disable
LF11	Receive		M		Disable
LF12	Loopback		M		Disable
LF13	Collision Presence		M		Disable
LF14	SQE Test		M		Disable
LF15	Link Test Fail Extend state exit condition	14.2.1.7	M		Deferred until RD = idle and DO = idle
LF16	Power-on state	14.2.1.7	O		Link Test Fail Reset
LF17	Pulse/data discrimination	14.2.1.7	M		Link test pulse not detected as data

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14.10.4.5.9 MAU state diagram requirements

	Parameter	Subclause	Req	Imp	Value/Comment
SD1	Transmit, Receive, Loopback, and Collision Presence Functions state diagram	14.2.3	C		Meets requirements of Figure 14–3. Conditional on whether or not the function is to be performed (14.10.4.5.1/MF3 and 14.10.4.5.1/MF4)
SD2	MAU Transmit and Receive Functions state diagram (full duplex mode)	14.2.3	C		Conditional on whether or not the function is to be performed (14.10.4.5.1/MF3 and 14.10.4.5.1/MF4)
SD3	*signal_quality_error* Message Test Function state diagram	14.2.3	C		Meets requirements of Figure 14–4. Conditional on whether or not the function is to be performed (14.10.4.5.1/MF7)
SD4	Jabber Function state diagram	14.2.3	M		Meets requirements of Figure 14–5
SD5	Link Integrity Test Function state diagram	14.2.3	M		Meets requirements of Figure 14–6

14.10.4.5.10 AUI requirements

	Parameter	Subclause	Req	Imp	Value/Comment
AR1	AUI implementation	14.3	O		If implemented, refer to 14.10.4.6
AR2	AUI messages	14.2.2	M		Comply to 7.2.1

14.10.4.5.11 Electrical isolation

	Parameter	Subclause	Req	Imp	Value/Comment
IR1	Electrical isolation	14.3.1.1	C		Conforms to J.1

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14.10.4.5.12 Transmitter specification

	Parameter	Subclause	Req	Imp	Value/Comment
TS1	Peak differential output voltage on TD circuit for a type 10BASE-T MAU that is not a type 10BASE-Te MAU	14.3.1.2.1	C		Conditional on whether it is a type 10BASE-T MAU that is not a type 10BASE-Te MAU, 2.2 to 2.8 V
TS2	Peak differential output voltage on TD circuit for a type 10BASE-Te MAU	14.3.1.2.1	C		Conditional on whether it is a type 10BASE-Te MAU, 1.54 to 1.96 V
TS3	Harmonic content, all-ones signal	14.3.1.2.1	M		All harmonics ≥ 27 dB below fundamental
TS4	Output waveform, with scaling of voltage template	14.3.1.2.1	M		Within Figure 14–10 template
TS5	Start of TP_IDL waveform, with each specified load, with and without twisted-pair model	14.3.1.2.1	M		Within Figure 14–11 template, overshoot ≤ +50 mV after excursion below –50 mV
TS6	Link test pulse waveform, with each specified load, with and without twisted-pair model	14.3.1.2.1	M		Within Figure 14–11 template, overshoot ≤ +50 mV after excursion below –50 mV
TS7	TD circuit differential output impedance	14.3.1.2.2	M		Reflection ≥ 15 dB below incident, any simplex link segment
	Transmitter added timing jitter:	14.3.1.2.3			
TS8	Into 100 Ω through twisted-pair model		M		±3.5 ns max
TS9	Into 100 Ω		M		±8 ns max
TS10	Common-mode to differential-mode conversion	14.3.1.2.4	M		≥ 29 – 17 $\log_{10}(f/10)$ dB, f=1–20 MHz, f in MHz
TS11	TD circuit common-mode output voltage	14.3.1.2.5	M		< 50 mV peak
TS12	TD circuit common-mode rejection, 15 V peak 10.1 MHz sinusoid	14.3.1.2.6	M		≤ 100 mV differential and ≤ 1 ns jitter
TS13	TD circuit fault tolerance	14.3.1.2.7	M		No damage from a short circuit
TS14	TD circuit short-circuit current	14.3.1.2.7	M		300 mA max
TS15	TD circuit common-mode voltage withstand	14.3.1.2.7	M		1000 V min, applied per Figure 14–16
TS16	Power cycle behavior	14.3.2.3	M		No extraneous signals on the TD circuit

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14.10.4.5.13 Receiver specification

	Parameter	Subclause	Req	Imp	Value/Comment
RS1	RD circuit signal acceptance	14.3.1.3.1	M		Figure 14–17, Figure 14–18, template
RS2	Received signal jitter accept	14.3.1.3.1	M		At least ±13.5 ns
RS3	Receiver added jitter	14.3.1.3.1	M		≤ ±1.5 ns, RD to DI circuits
RS4	RD circuit link test pulse acceptance	14.3.1.3.2	M		Figure 14–13 template
 RS5 RS6 RS7	RD circuit differential noise rejection: Signal (1) Signal (2) Signal (3)	14.3.1.3.2	 M M M		 ≤ 300 mV peak ≤ 6.2 V peak-to-peak, ≤ 2 MHz Single cycle ≤ 6.2 V, either phase, 2–15 MHz
RS8	Idle detection, RD circuit	14.3.1.3.3	M		Within 2.3 bit times
RS9	RD circuit differential input impedance	14.3.1.3.4	M		Reflected signal ≥ 15 dB below incident, any simplex link segment
RS10	RD circuit common-mode rejection	14.3.1.3.5	M		25 V peak-to-peak square wave to add ≤ 2.5 ns jitter
 RS11 RS12	RD circuit fault tolerance: Short circuit Common-mode voltage	14.3.1.3.6	 M M		 Indefinite short circuit 1000 V impulse, applied per Figure 14–20

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14.10.4.5.14 MDI requirements

	Parameter	Subclause	Req	Imp	Value/Comment
MR1	MDI connector	14.5.1	M		IEC 60603-7:1990 jack
 MR2 MR3 MR4 MR5	MDI connector contact assignment: 1 2 3 6	14.5.1	 M M M M		 TD+ TD– RD+ RD–
MR6	Crossover function implemented	14.5.2	O		Remote MAU from DTE (recommended)
MR7	Crossover function indication	14.5.2	C		X symbol on MDI connector. Conditional on crossover function implementation. Refer to response to 14.10.4.5.14/MR6
 MR8 MR9 MR10 MR11	MDI-X connector contact assignment: 1 2 3 6	14.5.2	 C C C C		 RD+ RD– TD+ TD– Conditional on crossover function implementation. Refer to response to 14.10.4.5.14/MR6

14.10.4.5.15 Safety requirements

	Parameter	Subclause	Req	Imp	Value/Comment
SR1	Safety grounding path	14.7.2.2	C		Has to be via PG circuit. Conditional on AUI implementation. Refer to response for 14.10.4.5.10/AR1 or PIXIT
SR2	MAU labeling	14.8	O		Data rate, current, any applicable safety warnings (recommended)
SR3	General safety	14.7.1	M		Conforms to J.2
SR4	Application of telephony voltages	14.7.2.4	M		Creates no safety hazard

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14.10.4.6 PICS proforma tables for MAU AUI characteristics

The whole of 14.10.4.6 is conditional on the AUI being implemented and accessible for testing. Refer to response for 14.10.4.5.10/AR1 or PIXIT.

14.10.4.6.1 Signal characteristics

	Parameter	Subclause	Req	Imp	Value/Comment
SC1	Signaling rate (stated on label)	7.3.2	C		10 Mb/s
SC2	CS0 signal frequency (on CI)	7.3.1.2	C		10 MHz ± 15%
SC3	CS0 signal duty cycle	7.3.1.2	C		60:40 worst case

14.10.4.6.2 DI and CI driver characteristics

	Parameter	Subclause	Req	Imp	Value/Comment
	Differential output voltage:	7.4.1.1			
DC1	Loaded		C		Figure 7–11
DC2	Idle state		C		≤ 40 mV into test load
DC3	Start of idle		C		Figure 7–12
DC4	Current into test load while idle	7.4.1.1	C		4 mA max after 80 BT
DC5	Requirements after idle	7.4.1.2	C		First bit to Figure 7–11
DC6	Common-mode output voltage, ac	7.4.1.3	C		≤ 40 mV peak. Figure 7–13
DC7	Differential output voltage, open circuit	7.4.1.4	C		13 V peak max
DC8	Common-mode output voltage, dc	7.4.1.5	C		≤ 5.5 V. Figure 7–13
DC9	Fault tolerance	7.4.1.6	C		Figure 7–14
DC10	Fault current	7.4.1.6	C		≤ 150 mA, any Figure 7–14 state

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14.10.4.6.3 DO receiver characteristics

	Parameter	Subclause	Req	Imp	Value/Comment
DO1	Unsquelched threshold	7.4.2.1	C		160 mV max differential
DO2	Squelch	14.3.2.1	C		Reject signals ≤ 160 mV magnitude
DO3	High-to-idle transition on DO circuit	7.4.1.1	C		Does not cause output
DO4	Differential input impedance at 10 MHz	7.4.2.2	C		Real part: 77.83 Ω ± 6%, 0 ≤ phase angle in degrees ≤ real part × 0.0338
DO5	Common-mode range, ac	7.4.2.3	C		3 V min 30 Hz to 40 kHz, 100 mV min 40 kHz to 10 MHz
DO6	Total common-mode range	7.4.2.4	C		Magnitude of 0 to 5.5 V ac + dc
DO7	Common-mode current limit	7.4.2.4	C		≤ 1 mA
DO8	IDL detection	7.3.1.1	C		≤ 1.6 bit times
DO9	Requirements after idle	7.4.2.5	C		Receiver in specification after startup delay
DO10	Receiver fault tolerance	7.4.2.6	C		Figure 7–15
DO11	Input fault current	7.4.2.6	C		3 mA max for Figure 7–15

14.10.4.6.4 Power consumption

	Parameter	Subclause	Req	Imp	Value/Comment
PC1	Power surge limitation	14.3.2.3	C		$\leq 2 \times 10^{-3}$ A·s
PC2	Power surge duration	14.3.2.3	C		100 ms max
PC3	Steady-state current drawn	14.3.2.3	C		≤ 500 mA
PC4 PC5	Power-up capability: Current limited sources Voltage sources	 14.3.2.3 7.5.2.5	 C C		 500 mA limited 11.28 to 15.75 V, any permissible AUI cable
PC6	Power cycle behavior	14.3.2.3	C		No extraneous signals on CI nor DI circuits
PC7	Low VP circuit behavior	7.5.2.5	C		No disruption of media

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14.10.4.6.5 Circuit termination

	Parameter	Subclause	Req	Imp	Value/Comment
CT1	Common-mode termination	7.5.2.6	C		If used, is to VC
CT2	Pins 1,4,11,14 impedance to VC circuit	7.5.2.8	C		≤ 5 Ω at 5 MHz
CT3	Pins 1,4,11,14 coupling to VC circuit	7.5.2.8	C		Capacitive

14.10.4.6.6 Mechanical characteristics

	Parameter	Subclause	Req	Imp	Value/Comment
MC1	D-type connector dimensions	7.6.2	C		IEC 60807-2:1992 15-pole male
MC2	Shell plating material	7.6.2	C		Conductive
MC3	Shell multiple contact points	7.6.2	O		Number not defined (recommended)
MC4	Shell life expectancy	7.6.2	C		≤5 mΩ / 500 matings
MC5	Locking posts and mounting	7.6.1	C		Figure 7–17, Figure 7–19
	Pin connections:	7.6.3			Circuit
MC6	3		C		Data out A
MC7	10		C		Data out B
MC8	11		C		Capacitor to VC
MC9	5		C		Data in A
MC10	12		C		Data in B
MC11	4		C		Capacitor to VC
MC12	7		C		No connection
MC13	15		C		No connection
MC14	8		C		Capacitor to VC
MC15	2		C		Control in A
MC16	9		C		Control in B
MC17	1		C		Capacitor to VC
MC18	6		C		Voltage common
MC19	13		O		Voltage plus
MC20	14		C		Capacitor to VC
MC21	Shell		C		Protective Ground (Conductive Shell)

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14.10.4.7 PICS proforma tables for 10BASE-T link segment

14.10.4.7.1 10BASE-T link segment characteristics

	Parameter	Subclause	Req	Imp	Value/Comment
	Cable size:				Cable size affects NEXT limits
LS1	25-pair cable or binder groups	14.4.3.1.1	O		
LS2	4-pair cable	14.4.3.1.2	O		
LS3	Other	14.4.3.1.3	O		
LS4	Insertion loss, 5.0 MHz to 10 MHz for a type 10BASE-T MAU that is not a type 10BASE-Te MAU	14.4.2.1	C		Conditional on whether it is a type 10BASE-T MAU that is not a type 10BASE-Te MAU, ≤ 11.5 dB
LS5	Insertion loss, 5.0 MHz to 10 MHz for a type 10BASE-Te MAU	14.4.2.1	C		Conditional on whether it is a type 10BASE-Te MAU, ≤ 8.5 dB
LS6	Differential characteristic impedance of a 3 m cable section, 5.0 MHz to 10 MHz	14.4.2.2	M		85 Ω to 111 Ω
LS7	Input impedance averaged, 5.0 MHz to 10 MHz	14.4.2.2	M		85 Ω to 111 Ω
LS8	Medium timing jitter (for defined test signal)	14.4.2.4	M		±5.0 ns max
	Delay:				
LS9	Per meter		M		≤ 5.7 ns/m
LS10	Link segment		M		≤ 1000 ns
	NEXT loss, pair-to-pair, 5.0 MHz to 10 MHz:				
LS11	25-pair cable and binder groups	14.4.3.1.1	C		≥ 30 – 15 $\log_{10}(f/10)$ dB
LS12	4-pair cable	14.4.3.1.2	C		≥ 26 – 15 $\log_{10}(f/10)$ dB These requirements are conditional on the responses in clauses 14.10.4.7.1/LS1 and 14.10.4.7.1/LS2, f in MHz
LS13	MDNEXT at 5.0 MHz, 7.5 MHz, and 10 MHz	14.4.3.2	M		≥ 23 – 15 $\log_{10}(f/10)$ dB, f in MHz
	Noise environment:				
LS14	Impulse noise (into defined circuit)	14.4.4.1	M		Fewer than 0.2 impulses/s of ≥ 264 mV
LS15	Crosstalk noise	14.4.4.2	M		≤ 264 mV
LS16	Connectors	14.5.1	M		IEC 60603-7:1990 plug
LS17	Literature indicates the distance and environmental conditions over which 14.4 specifications are met	14.7.3.2	O		

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14.10.4.8 PICS proforma tables for Auto-Negotiation able MAUs

The following are conditional on whether the Auto-Negotiation algorithm is provided (Clause 28).

	Parameter	Subclause	Req	Imp	Value/Comment
AN1	TP_IDL	14.2.1.1	C		Defined in 28.2.1
AN2	Link Integrity Test Function State Diagram power-on default	14.2.1.7	C		Power-on in Link Test Fail Reset state
AN3	Link Test Fail state exit conditions	14.2.1.7	C		autoneg_wait_timer expired and either RD = active or consecutive link test pulses = 3 min, 10 max
AN4	Technology Dependent Interface support	14.2.1.7	C		In the Link Integrity Test state diagram function “link_status=OK” is added to the LINK TEST PASS state and “link_status=FAIL” is added to the LINK TEST FAIL RESET state
AN5	Link test pulse waveform for FLP Burst with and without twisted-pair model	14.3.1.2.1	C		Within Figure 14–11 template for, all pulses in FLP Burst, overshoot ≤ +50 mV after excursion below –50 mV
AN6	MAU indicates full duplex mode capability during Auto-Negotiation	14.2.1.8	C		Function optionally performed by embedded MAUs, not performed by MAUs that implement an AUI connector

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15. Fiber optic medium and common elements of medium attachment units and star, type 10BASE-F

15.1 Scope

15.1.1 Overview

Clause 15, Clause 16, Clause 17, and Clause 18 define the functional, electrical, optical, and mechanical characteristics of the type 10BASE-FP (Passive) MAU, the type 10BASE-FB Backbone (Synchronous Active) MAU, the type 10BASE-FL Link (Asynchronous Active) MAU, the type 10BASE-FP (Passive) Star, and one common medium for use with those MAUs and the star. The purpose of the MAUs is to provide a means of attaching full duplex DTEs (10BASE-FL only), half duplex DTEs (10BASE-FP and 10BASE-FL only), or repeaters to the local network medium. The purpose of the 10BASE-FP Star is to provide the means of interconnecting 10BASE-FP MAUs into a star topology segment. The IEEE 802.3 repeaters are used to interconnect the star segment to other 10 Mb/s baseband segments. Information on selecting segment types for various applications is provided in 15.1.3.4.

The 10BASE-F specification builds upon Clause 1 through Clause 7 and Clause 9 of this standard. The relationship of this clause to the OSI Reference Model is shown in Figure 15–1a), Figure 15-1b), and Figure 15-1c) for 10BASE-FP, 10BASE-FB, and 10BASE-FL, respectively.

10BASE-F is specifically intended to be interoperable and compliant with the requirements for attachment to DTEs and repeaters via the 10 Mb/s Attachment Unit Interface (AUI). The use of 10BASE-F in networks with other IEEE 802.3, 10 Mb/s baseband segments is governed by the system considerations detailed in Clause 13.

15.1.1.1 Fiber optic medium attachment units (MAUs)

The MAUs specified in this clause, Clause 16 (10BASE-FP), Clause 17 (10BASE-FB), and Clause 18 10BASE-FL) have the following general characteristics:

a) They provide a means of coupling the PLS through the AUI to the fiber optic segment by way of the MDI.
b) They support message traffic at a data rate of 10 Mb/s.
c) They provide for driving up to 1 km of fiber optic cable with a 10BASE-FP Star connected in the middle between two 10BASE-FP MAUs. Provide for driving up to 2 km of fiber optic cable between two repeaters that have embedded 10BASE-FB MAUs. Provide for driving up to 2 km of fiber optic cable between two 10BASE-FL MAUs. Provide backward compatibility for communicating between FOIRL MAUs and 10BASE-FL MAUs over up to 1 km of fiber optic cable.
d) They permit the DTE to test the MAU and the availability of the medium.
e) They support system configurations using the CSMA/CD access mechanism defined in this standard.
f) They provide uninterrupted carrier sense during collisions.
g) They support a star cabling topology.
h) They allow incorporation of the MAU within the physical bounds of a DTE or repeater. (See Clause 17 for 10BASE-FB restrictions.)

15.1.1.2 Fiber optic passive star

The 10BASE-FP Star is a passive optical device that receives optical signals from, and distributes them to, connected devices (see Figure 15–2b). The 10BASE-FP Star is not a repeater.

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15.1.1.3 Repeater unit

The repeater unit has the characteristics defined in Clause 9. Repeater units are used as a hub in a star topology network in which DTEs attach directly to link segments. Repeater units are also used to extend the physical system topology of mixing segments by connecting 10BASE-FP or coaxial cable segments to other segments. Repeater units are used to connect 10BASE-F segments of any type to other 10BASE-F segments, and to any other 10 Mb/s baseband media types. 10BASE-FB segments connect only 10BASE-FB ports on repeaters.

NOTE—While 9.6.6 autopartitioning is not required as a mandatory feature on 10BASE-FB ports, it should be recognized that it could be of benefit where there is a high probability of misconnections of incompatible ports, e.g., patch panels shared between 10BASE-FB and other fiber optic communication technologies.

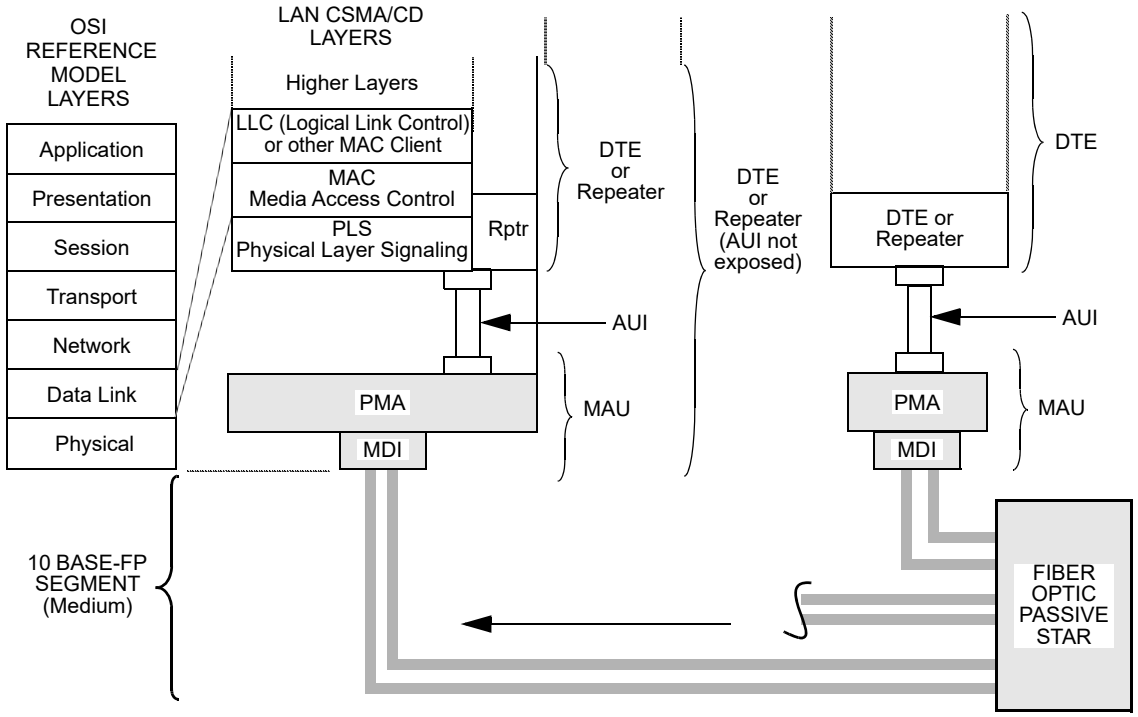
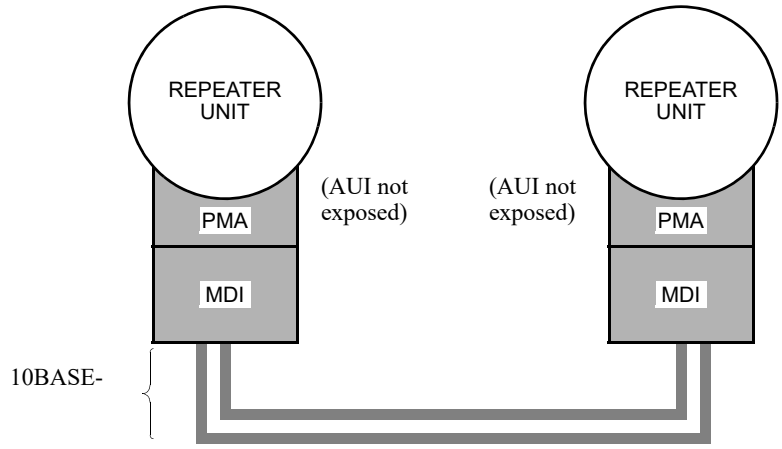


Figure 15–1—10BASE-F relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model



b) 10BASE-FB relationship to CSMA/CD LAN

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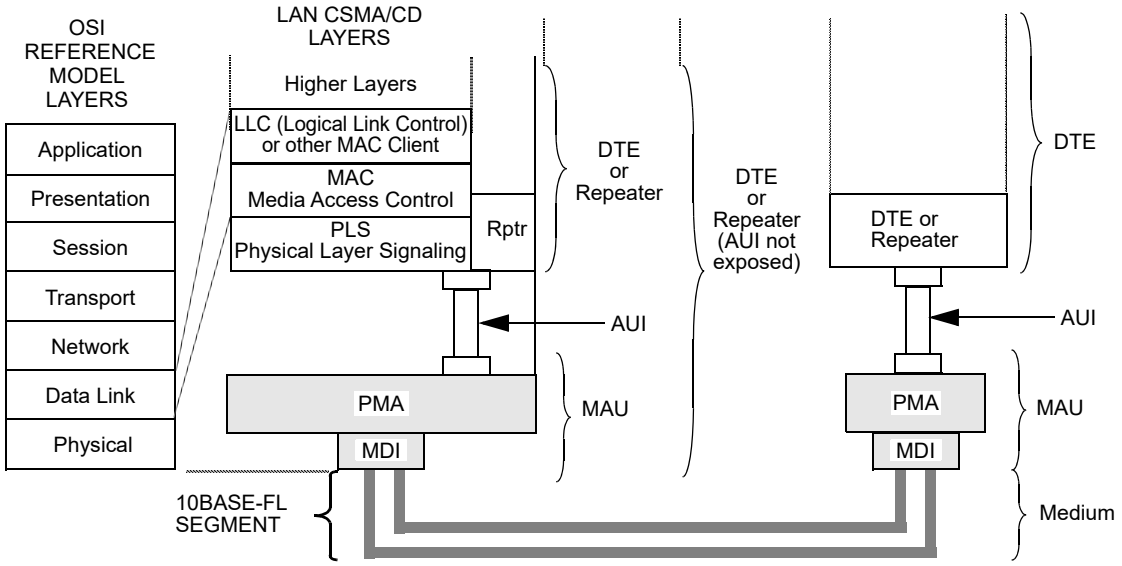

c) 10BASE-FL relationship to OSI and CSMA/CD LAN

Figure 15-1—(*Continued*)
10BASE-FL relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the ISO/IEC CSMA/CD LAN model

15.1.2 Definitions

See 1.4.

15.1.3 Applications perspective: MAUs, stars, and fiber optic medium

This clause states the broad objectives and assumptions underlying the specifications defined in Clause 15, Clause 16, Clause 17, and Clause 18.

15.1.3.1 Objectives

a) To provide a physical means for communication between LAN data link entities using fiber optic media connected in a star topology.
b) To ensure compatibility of independently developed physical, electrical, and optical interfaces.
c) To provide a communication channel capable of high bandwidth and low bit-error ratio performance. The resultant mean bit-error ratio, between AUIs over a fiber segment, should be less than one part in 10^9.
d) To provide for ease of installation and service.
e) To ensure that fairness of DTE access is not compromised.

15.1.3.2 Compatibility considerations

All implementations of 10BASE-FP, 10BASE-FB, and 10BASE-FL fiber optic systems shall be compatible at their respective MDIs when used in accordance with the restrictions of Clause 9 and 16.5 where appropriate. When FOIRL segments are used, all 10BASE-FL MAUs shall be compatible with the FOIRL MDI specified in 9.9 except for the media connector, which shall be as specified in 15.3.2.

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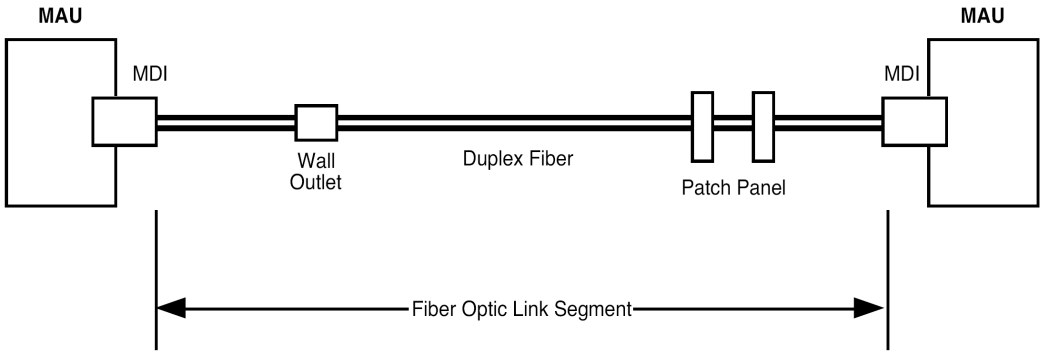
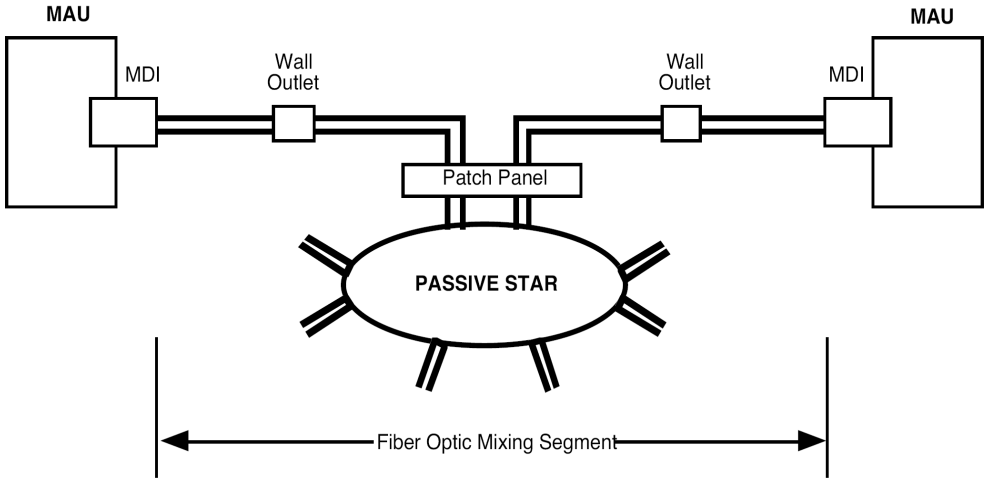


a) Example fiber optic link segment, 10BASE-FB and 10BASE-FL



b) Example fiber optic mixing segment, 10BASE-FP

Figure 15–2—Fiber optic link and mixing segments

Implementations of 10BASE-F of any one type are not compatible with 10BASE-F of any other type at the MDI.

Clause 15 provides medium specifications for interconnection of the fiber optic MAUs and star defined in Clause 16, Clause 17, and Clause 18. The star specified in 16.5 completes the specification of the media for a 10BASE-FP segment. The medium itself, the functional capability of the 10BASE-FP, 10BASE-FB, and 10BASE-FL MAUs, and the AUI are defined to provide the highest possible level of compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the MAU in an application-dependent manner provided that the MDI and AUI specifications are satisfied. The provision of the physical and mechanical implementation of the AUI is optional for Clause 16 and Clause 18 MAUs, and is not applicable for Clause 17 MAUs.

15.1.3.3 Relationship to PLS and AUI

Clause 15, together with Clause 16, Clause 17, or Clause 18, defines the portion of the Physical Layer and medium for the LAN necessary to couple a DTE or repeater message path to and from the medium.

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A close relationship exists between Clause 7 and the 10BASE-FP, 10BASE-FB, and 10BASE-FL MAUs defined in Clause 16, Clause 17, and Clause 18, respectively. Clause 15 specifies the physical medium parameters, and Clause 16, Clause 17, and Clause 18 the PMA logical functions residing in the physical MAU. The MAU provides services to the PLS defined in Clause 7 by means of the AUI. 10BASE-F MAUs support a subset of the AUI services specified in Clause 7. 10BASE-F MAUs do not support the optional *isolate* function, the optional CO circuit, or the optional CS1 signal on the CI circuit.

The design of an external MAU component requires the use of Clause 15, Clause 16 or Clause 18, and Clause 7 for the PLS and AUI specifications.

The figures and numerous textual references throughout Clause 15, Clause 16, Clause 17, and Clause 18 refer to terminology associated with the AUI (that is, DO, DI, and CI). Since an embodiment of the 10BASE-FP, 10BASE-FB, or 10BASE-FL MAU does not require implementation of an AUI, the DO, DI, and CI circuits may not physically exist. However, they are logically present, and MAU operation is defined in terms of their messages.

15.1.3.4 Guidelines for implementation of systems

The fiber optic systems defined herein cover a wide range of LAN applications in which the advantages of fiber optics are paramount. These advantages include noise immunity, low attenuation, bandwidth upgradeability, data security, and use in environments where the use of electric circuits would be hazardous. These systems allow construction of complex networks according to the system topology rules in Clause 13. Choice of system approach may be aided by the following guidelines:

— 10BASE-FP, Clause 16: A passive-star system for interconnecting repeaters or DTEs with up to 1 km per segment, useful where central power is unavailable or not sufficiently reliable for the intended application.
— 10BASE-FB, Clause 17: A system for interconnecting repeaters with up to 2 km per segment and for backbone applications where a large number of repeaters have to be cascaded.
— 10BASE-FL, Clause 18: A system for interconnecting repeaters or DTEs with up to 2 km per segment and where backward compatibility with 9.9 (FOIRL) (up to 1 km per segment) is desirable. This system also supports full duplex operation (see 1.1.2).

Repeaters (Clause 9) have to be used to connect other media to the above fiber optic segments. Repeaters also have to be used to interconnect FOIRL, 10BASE-FB, 10BASE-FP, and 10BASE-FL segments. 10BASE-FB segments can be used only between 10BASE-FB ports on repeaters.

15.1.3.5 Modes of operation

10BASE-F MAUs are capable of operating in normal mode only (see 7.1.4). They shall not operate in monitor mode. A MAU attached to a repeater shall not be in full duplex mode.

The operation of a 10BASE-FL MAU differs depending on whether the attached DTE is operating in the half duplex or full duplex mode (see 1.1.2). In the full duplex mode, functions relating to the loopback of transmitted data (DO) onto the receive path (DI) are disabled (see 18.3.1.3, 18.3.1.6).

The requirements specified in clauses of this standard labeled “half duplex mode only” do not apply to a MAU used with a DTE configured for full duplex operation. It is the responsibility of the designer and/or user of equipment operating in full duplex mode to ensure that the 10BASE-FL MAU used or incorporated is properly configured for full duplex operation.

10BASE-FP and 10BASE-FB MAUs are capable of operating in half duplex mode only.

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15.2 MDI optical characteristics

The transmit and receive optical parameters for the 10BASE-FP, 10BASE-FB, and 10BASE-FL fiber optic systems are summarized in Table 15–1. Optical measurements shall be made with the MDI terminated with the optical connector specified in 15.3.2 and the optical fiber specified in 15.3.1. Fiber length shall be sufficient to attenuate cladding mode distribution.

NOTE—Transmit and receive optical parameters refer to optical power in the core of the respective fiber (15.3.1). Fibers currently available typically require 1 m to 5 m to remove optical power from the cladding.

15.2.1 Transmit optical parameters

15.2.1.1 Center wavelength

The center wavelength of the optical source emission shall be as specified in Table 15–1.

15.2.1.2 Spectral width

The full width half maximum (FWHM) spectral width of the optical source shall be as specified in Table 15–1.

15.2.1.3 Optical modulation extinction ratio

The optical modulation method is on-off keying of the optical power source. The minimum extinction ratio shall be as specified in Table 15–1, measured at the normalization points (15.2.1.11).

15.2.1.4 Optical Idle Signal amplitude

The optical Idle Signal shall be as specified in Table 15–1.

15.2.1.5 Optical transmit pulse logic polarity

LO on the AUI DO circuit shall be represented at the MDI as LO and as the higher optical power level transmitted at the MDI. HI on the AUI DO circuit shall be represented at the MDI as HI and as the lower optical power level transmitted at the MDI (see 7.4.2.1). A 10BASE-FP Star by its nature is noninverting from any input to any output.

15.2.1.6 Optical transmit pulse rise and fall times

The optical rise and fall times at the MDI transmitter shall be measured from the 10% to 90% levels. The rise and fall times and their difference shall be as specified in Table 15–1.

15.2.1.7 Optical transmit pulse overshoot and undershoot

The maximum optical overshoot and undershoot shall be as specified in Table 15–1.

15.2.1.8 Optical transmit pulse edge jitter

The total transmitted edge jitter measured at the MDI shall be as specified in Table 15–1 for a transmitted waveform consisting of a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits. The jitter at the MDI shall be measured at the power level median of the optical waveform's upper and lower power levels (as determined from the previous 16 or more transitions in any valid optical bit stream). This does not include any effects from variations of Optical Transmit Pulse Duty Cycle (15.2.1.9).

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Table 15–1—MDI parameters

Subclause	Parameter	Units	10BASE-FP	10BASE-FB	10BASE-FL
15.2.1	TRANSMIT OPTICAL PARAMETERS				
15.2.1.1	Center wavelength —min. —max.	 nm nm	 800 910	 800 910	 800 910
15.2.1.2	Spectral width (FWHM)	nm	<75	<75	<75
15.2.1.3	Optical modulation extinction ratio	dB	≤13	≤13	≤13
15.2.1.4	Optical idle signal amplitude	dBm	≤57	see 15.2.1.10	see 15.2.1.10
15.2.1.6	Optical transmit pulse rise and fall times —max. (data) —min. (data) —max. difference (data) —max. (idle) —min. (idle) —max. difference (idle)	 ns ns ns ns ns ns	 10 2 3 N/A N/A N/A	 10 0 3 10 0 3	 10 0 3 25 0 25
15.2.1.7	Optical transmit pulse —overshoot —undershoot	 % %	 5 5	 25 10	 25 10
15.2.1.8	Optical transmit pulse edge jitter —added, DO circuit to MDI —total at MDI (data) —total at MDI (idle)	 ns ns ns	 N/A ±1 N/A	 N/A ±2 ±2	 ±2 ±4 N/A
15.2.1.9	Optical transmit pulse Duty cycle distortion —data —idle	 ns ns	 ±1 N/A	 ±2.5 ±2.5	 ±2.5 ±50.0
15.2.1.10	Optical transmit average power range —min. —max.	 dBm dBm	 –15 –11	 –20 –12	 –20 –12
15.2.2	RECEIVE OPTICAL PARAMETERS				
15.2.2.1	Optical receive average power range —min. —max.	 dBm dBm	 –41 –27	 –32.5 –12.0	 –32.5 –12.0
15.2.2.2	MAU optical receive edge jitter (data) —received at MDI —added, MDI to DI circuit —total at DI circuit (MAU end of AUI)	 ns ns ns	 ±4.5 N/A N/A	 ±2.0 N/A ±6.5	 ±6.5 ±8.5 ±15.0
15.2.2.4	Optical receive pulse rise and fall times —max. (data) —min. (data) —max. difference (data) —max. (idle) —min. (idle) —max. difference (idle)	 ns ns ns ns ns ns	 18.5 2.0 3.0 N/A N/A N/A	 31.5 0.0 3.0 31.5 0.0 3.0	 31.5 0.0 3.0 41.0 0.0 25.0

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15.2.1.9 Optical transmit pulse duty cycle distortion

The optical pulse duty cycle shall be as specified in Table 15–1. The duty cycle distortion measured at the output of the electro-optic source shall be measured at the power level median of the optical waveform's upper and lower power levels (as determined in 15.2.1.10).

15.2.1.10 Optical transmit average power range

The optical transmit average power coupled into the core of the fiber shall be in the range specified in Table 15–1 at the MDI.

To meet the 10BASE-FP power range, the use of one or more techniques such as emitters with a focused radiation pattern, optical power setting, or temperature compensation may be necessary.

NOTE—The optical power ranges shown in Table 15–1 can be met by the following:

10BASE-FB and 10BASE-FL MDI

Nominal average power, beginning of life–15 dBm
Transmit power tolerance*±3 dB
Transmit power degradation, end of life–2 dB

10BASE-FP MDI

Nominal average power, beginning of life–12.5 dBm
Transmit power tolerance*±1.5 dB
Transmit power degradation, end of life–1 dB

* Transmit power tolerance includes emitter, optical connector, and optical fiber tolerances.

15.2.1.11 Optical transmit signal templates

The transmitted optical waveforms for the 10BASE-FP MAU, 10BASE-FB MAU, and 10BASE-FL MAU shall fall within the templates shown in Figure 15–3, Figure 15–4, and Figure 15–5, respectively, when normalized. Normalization is achieved by linearly scaling and shifting the waveform amplitude and shifting the waveform timebase so that it intersects the two normalization points indicated by the black dots on the templates. These templates show a graphical representation of the transmit parameters described in 15.2.1.3, 15.2.1.6, 15.2.1.8, and 15.2.1.9. Table 15–1 lists the appropriate numerical values for these parameters. If any conflict exists between the templates and Table 15–1, the table shall take precedence.

The definition of "normalized optical power" is indicated on Figure 15–3, Figure 15–4, and Figure 15–5. The measured optical power is scaled and shifted so that the definition of "0" optical power and "1" optical power is determined by the average signal value at the points indicated by the black dots on the figures.

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15.2.1.11.1 10BASE-FP optical transmit signal template

The points of inflection for the template of Figure 15–3 are defined by the coordinate pairs contained in Table 15–2.

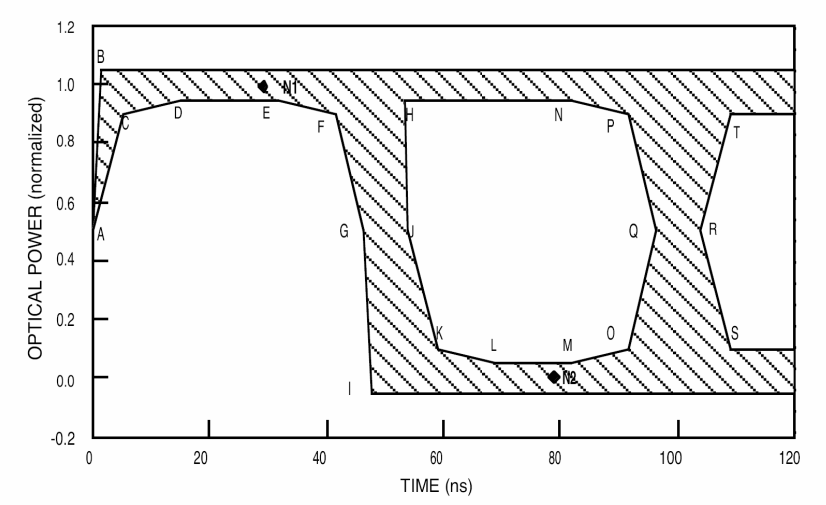

Figure 15–3—10BASE-FP MAU transmit waveform template

Table 15–2—Transmitted optical waveform values for Figure 15–3

Reference	Time (ns)	Optical power (normalized)
A	0.0	0.5
B	1.375	1.05
C	5.0	0.9
D	15.0	0.95
E	31.0	0.95
F	41.0	0.9
G	46.0	0.5
H	52.875	0.95
I	47.375	–0.05
J	54.0	0.50
K	59.0	0.10
L	69.0	0.05

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Table 15–2—Transmitted optical waveform values for Figure 15–3 *(continued)*

Reference	Time (ns)	Optical power (normalized)
M	81.0	0.05
N	81.0	0.95
O	91.0	0.10
P	91.0	0.90
Q	96.0	0.50
R	104.0	0.50
S	109.0	0.10
T	109.0	0.90
N1	29.0	1.00
N2	79.0	0.00

15.2.1.11.2 10BASE-FB optical transmit signal template

The points of inflection for the template of Figure 15–4 are defined by the coordinate pairs contained in Table 15–3.

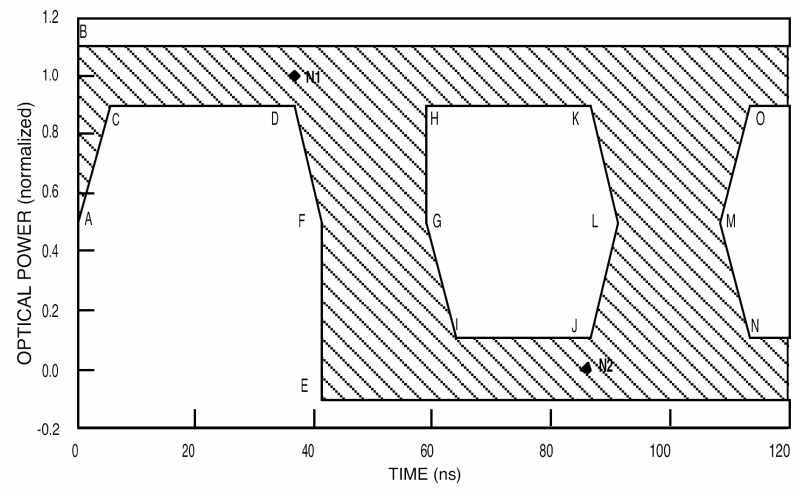

Figure 15–4—10BASE-FB MAU transmit waveform template

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Table 15–3—Transmitted optical waveform for Figure 15–4

Reference	Time (ns)	Optical power (normalized)
A	0.0	0.5
B	0.0	1.1
C	5.0	0.9
D	36.0	0.9
E	41.0	–0.1
F	41.0	0.5
G	59.0	0.5
H	59.0	0.9
I	64.0	0.1
J	86.0	0.1
K	86.0	0.9
L	91.0	0.5
M	109.0	0.5
N	114.0	0.1
O	114.0	0.9
N1	36.0	1.00
N2	86.0	0.00

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15.2.1.11.3 10BASE-FL Optical transmit signal template

The points of inflection for the template of Figure 15–5 are defined by the coordinate pairs contained in Table 15–4. This template is for data only.

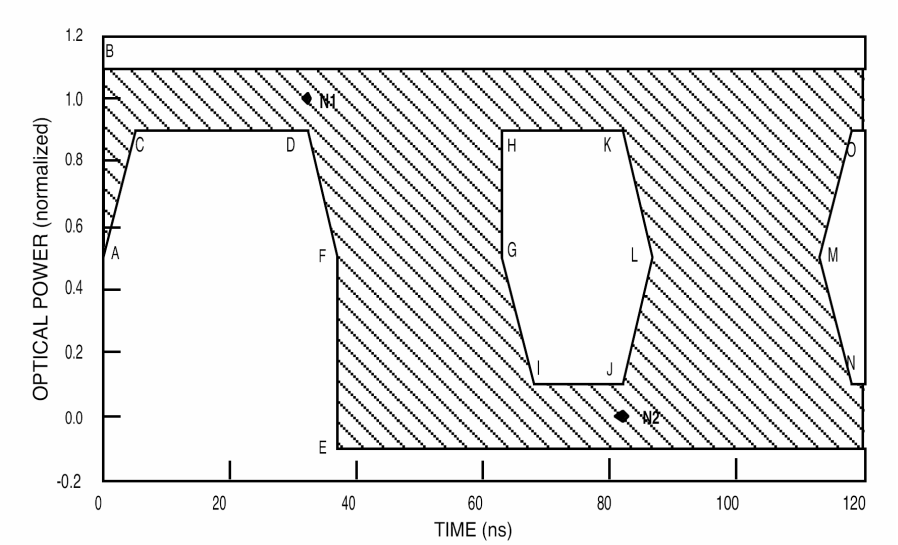

Figure 15–5—10BASE-FL MAU transmit waveform template (data only)

Table 15–4—Transmitted optical waveform values for Figure 15–5

Reference	Time (ns)	Optical power (normalized)
A	0.0	0.5
B	0.0	1.1
C	5.0	0.9
D	32.0	0.9
E	37.0	–0.1
F	37.0	0.5
G	63.0	0.5
H	63.0	0.9
I	68.0	0.1
J	82.0	0.1
K	82.0	0.9
L	87.0	0.5
M	113.0	0.5

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Table 15–4—Transmitted optical waveform values for Figure 15–5 *(continued)*

Reference	Time (ns)	Optical power (normalized)
N	118.0	0.1
O	118.0	0.9
N1	32.0	1.00
N2	82.0	0.00

15.2.2 Receive optical parameters

The bit-error ratio (BER) shall be less than one part in 10^9, when measured between two AUIs attached to a single 10BASE-FP, 10BASE-FB, or 10BASE-FL segment for all combinations of valid optical receive parameters specified in the following subclauses and valid optical transmit pulse duty cycle distortion (15.2.1.9). For the case of integrated MAUs this measurement has to be made by inference.

15.2.2.1 Optical receive average power range

The optical receive average power shall be in the range specified in Table 15–1 at the MDI when a single transmitter is transmitting on the medium.

15.2.2.2 Optical receive pulse edge jitter

The received edge jitter shall be as specified for a received waveform consisting of a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits. The jitter at the input MDI shall be measured at the power level median of the optical waveform's upper and lower power levels (as determined from the previous 16 or more transitions in any valid bit stream). The jitter measured at the output of the DI circuit driver shall be measured at the zero crossing points (as determined from the previous 16 or more transitions in any valid bit stream).

NOTE—For the transmit optical parameters of Table 15–1 and the fiber parameters of 15.3.1, the contribution to jitter for a 2 km long fiber is less than 10 ps (.01 ns). For purposes of calculation and specifications, no jitter contribution is allocated to the fiber optic segment (including any 10BASE-FP Star).

Optical signals at the input of the MDI receiver shall be received and sent to the DI circuit if they have total received jitter of no more than that specified in Table 15–1.

The maximum additional edge jitter introduced at a MAU from the input of the MDI receiver to the output of the DI circuit driver shall be as specified in Table 15–1.

The total edge jitter at the output of the DI circuit driver shall be no more than that given by the sum of the worst-case edge jitter components specified in Table 15–1.

15.2.2.3 Optical receive pulse logic polarity

The higher optical power level received at the MDI shall be represented by LO at both the MDI and the AUI DI circuit. The lower optical power level received at the MDI shall be represented by HI at both the MDI and the AUI DI circuit (see 7.4.2.1).

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15.2.2.4 Optical receive pulse rise and fall times

The optical rise and fall times at the MDI receiver shall be measured from the 10% to 90% levels. The rise and fall times and their maximum difference shall be as specified in Table 15–1 at the MDI.

15.3 Characteristics of the fiber optic medium

The fiber optic transmission medium consists of one or more sections of fiber optic cables with any intermediate connectors required to connect sections together and terminated at each end in the optical connector plug as specified in 15.3.2. The fiber optic medium spans from one MDI to another MDI.

15.3.1 Optical fiber and cable

The optical medium requirements are satisfied by the 62.5/125 μm nominal diameter fiber specified in IEC 60793-2:1992, type A1b with the exceptions noted in 15.3.1.1 to 15.3.1.3. For links under 5 m in length it may be necessary to use techniques such as attenuators or mode-stripping filters to attenuate optical power coupled into the cladding in order to meet the requirements of 15.2.2.1. The system can operate, subject to certain restrictions, with a variety of optical fibers. Information on other fiber sizes is contained in D.4. However, conformance to this standard and interoperability between different vendors' equipment is assured only through the use of the optical fiber specified in this subclause.

15.3.1.1 Attenuation

This standard was developed on the basis of cabled optical fiber with an attenuation value of less than or equal to 3.75 dB/km, when measured at a wavelength of 850 nm. Higher loss fiber may be used for shorter fiber pair lengths as long as the requirements in 15.3.3 are met.

NOTE—This value of attenuation is a relaxation of the standard IEC 60793-2:1992, type A1b, category ≤3.5 dB/km and ISO/IEC 11801:2002.

15.3.1.2 Modal bandwidth

Each optical fiber shall have a modal bandwidth-length product of not less than 160 MHz·km at a wavelength of 850 nm.

NOTE—This value of modal bandwidth is a relaxation of the standard IEC 60793-2:1992, type A1b, category >200 MHz·km and ISO/IEC 11801:2002.

15.3.1.3 Propagation delay

The propagation delay shall be ≤5 μs/km. (This is equivalent to a velocity of propagation of 0.67c.)

15.3.2 Optical medium connector plug and socket

Each end of the fiber optic cable that is to be connected to a 10BASE-FP, 10BASE-FB, or 10BASE-FL MAU or a 10BASE-FP Star shall be terminated in the BFOC/2.5 connector plug shown in Figure 15–6 (for informational use only) (one per fiber), as specified in IEC 60874-10:1992. The corresponding mating connector sockets shown in Figure 15–7 (for informational use only) shall be used on all network elements covered by this specification (10BASE-FP MAU, 10BASE-FB MAU, 10BASE-FL MAU, and 10BASE-FP Star) to which the fiber optic cable attaches. In-line or patch panel connectors may be of other types, but have to meet the requirements of 15.3.2.1 and 15.3.2.2.

NOTE—It is good practice to cap unused connectors to protect the system from ambient light and the connector interface from contamination.

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15.3.2.1 Optical connector insertion loss

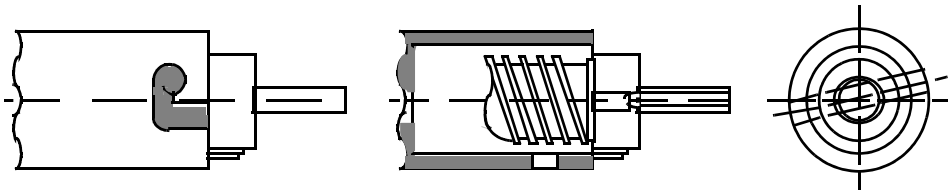
This standard was developed on the basis of a maximum insertion loss of 1.0 dB (see note below). Connectors with different loss characteristics may be used as long as the requirements in 15.3.2.2 and either 15.3.3.1 or 15.3.3.2 are met. Use of connectors with greater than 1.0 dB insertion loss is likely to reduce achievable transmission distances below those mentioned in 15.1.3.4.

NOTE—Per test method ANSI/EIA/TIA 455-34-1985 [B4], Method A, or ANSI/EIA/TIA 455-59-1989 [B6]. (No ISO/IEC test method was available at the time this standard was developed.)

15.3.2.2 Optical connector return loss

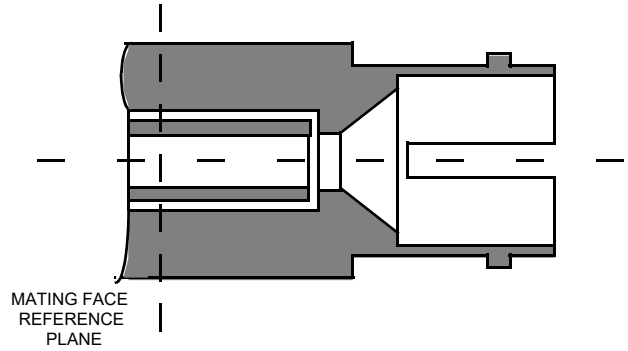
The return loss of optical connectors for 10BASE-FP segments shall be greater than 25 dB.

NOTE—The number of intermediate connectors in a fiber pair may have system implications because of return loss considerations (see B.5.2).



(for illustration only)

Figure 15–6—BFOC/2.5 connector plug



(for illustration only)

Figure 15–7—BFOC/2.5 connector socket

15.3.3 Fiber optic medium insertion loss

The optical insertion loss may be allocated between the elements of the fiber optic cable plant in any manner as long as the requirements of 15.3.3.1 and 15.3.3.2 are met. The optical insertion loss shall be measured in accordance with ANSI/EIA/TIA 526-14-1990 [B8], Method A, Two Reference Jumpers.

NOTE—No ISO/IEC test method was available at the time this standard was developed.

15.3.3.1 10BASE-FP segment insertion loss

The optical insertion loss of the 10BASE-FP segment including 10BASE-FP Star shall be between 16 dB and 26 B, measured using an optical signal source with a center wavelength of 850 nm and spectral width of

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75 nm. The range of measured insertion losses across the 10BASE-FP segment shall be less than 6 dB for any given star output port with respect to all input ports (see note in 16.5.2.2). See B.5.2 for examples of system implementation.

15.3.3.2 10BASE-FB and 10BASE-FL segment insertion loss

The optical insertion loss of the 10BASE-FB and 10BASE-FL segment shall be less than 12.5 dB, measured using an optical signal source with a center wavelength of 850 nm and spectral width of 75 nm.

15.3.4 Electrical isolation

Electrical isolation shall be provided between MDIs attached to the fiber optic cable. There shall be no conducting path between the optical medium connector plug and any conducting element within the fiber optic cable. This isolation shall meet the isolation requirements as specified in J.1.

15.4 MAU reliability

The MAU shall be designed to have a Mean Time Before Failure (MTBF) of at least 10 million hours of continuous operation without causing communication failure among other stations attached to the network. Component failures within the MAU electronics should not prevent communication among other MAUs on the network.

15.5 MAU–AUI specification

When a MAU contains a physical AUI connector, the following specifications shall be met.

15.5.1 MAU–AUI electrical characteristics

The electrical characteristics for the driver and receiver components within the MAU that are connected to the AUI shall be identical to those specified in 7.4 and 7.5. Additionally, the AUI DO receiver shall reject an input waveform of less than ± 160 mV differential.

15.5.2 MAU–AUI mechanical connections

The MAU shall be provided with a 15-pin male connector as specified in 7.6.

15.5.3 Power consumption

Following power on, the surge current drawn by the MAU through the AUI shall be such that $I_p \times T_w$ is less than or equal to 2×10^{-3} Ampere-seconds, where I_p is the peak surge current and T_w is the time during which the current exceeds the larger of 0.5 A or $0.5 \times I_p$. After 100 ms following power on, the current drawn by the MAU shall not exceed 0.5 A when powered by the AUI.

The MAU shall be capable of operating from all possible AUI voltage sources, including those current-limited to 0.5 A, as supplied by the DTE or repeater through the resistance of all permissible AUI cables.

It is permissible, as an option, to provide a separate power source for the MAU. If a separate power source is implemented, provision shall be made to assure that under no circumstances power can be sourced on pin 13 (Circuit VP) of the AUI. The separate power source if implemented shall withstand at least one of the tests of 15.3.4.

The MAU shall be labeled externally to identify the maximum value of power supply current required by the device when the AUI is implemented.

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The MAU shall not introduce at the MDI or onto the DI or CI circuits of the AUI any extraneous signals on power-up or power-down.

15.5.4 MAU–AUI messages

The messages between the PLS in the DTE and the PMA in the MAU shall comply with 7.2.1. These messages also are used in repeater unit to PMA communications.

15.5.4.1 PLS to PMA messages

The following messages are sent by the PLS in the DTE or repeater to the PMA in the MAU (see 7.2.1.1):

Message	Circuit*	Signal	Meaning
output	DO	CD1, CD0	Output information
output_idle	DO	IDL	No data to be output
* Or virtual equivalent for an embedded MAU.			

15.5.4.2 PMA to PLS messages

The following messages are sent by the PMA in the MAU to the PLS in the DTE or repeater (see 7.2.1.2):

Message	Circuit*	Signal	Meaning
input	DI	CD1, CD0	Input information
input_idle	DI	IDL	No input information
signal_quality_error	CI	CS0	Collision or error detected by MAU
mau_available	CI	IDL	MAU is available for output
* Or virtual equivalent for an embedded MAU.			

15.5.4.2.1 *signal_quality_error* message

The *signal_quality_error* (SQE) message shall operate in the following fashion:

a) The SQE message shall be sent whenever a collision exists, as described in 16.3.4, 17.3.3 or 18.3.1.4.
b) The SQE message shall be sent whenever a jabber condition exists, as described in 16.3.6 or 18.3.1.6.
c) The SQE message shall be sent as a result of SQE Test, as described in 16.3.5 or 18.3.1.5. SQE Test shall not be performed by MAUs connected to repeaters.
d) Under all other conditions, the MAU shall send the *mau_available* message.

The MAU is required to assert the SQE message at the appropriate times, as described in a) through c) above, whenever the MAU is powered.

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15.6 Environmental specifications

15.6.1 Safety requirements

An application of the equipment specified herein is for interconnecting equipment in different buildings. This may present hazards beyond the range of protection assured by 15.3.4. Installation practice shall be consistent with this application and provide adequate personnel and equipment safety from earth faults and lightning strike hazards.

Installation practice shall be in accordance with local and national regulations.

NOTE—While optical fibers are nonconducting, some fiber optic cables do contain metallic strength members or sheathing that should be considered during installation. However, since grounding of these metallic members does not involve the signal path, it is beyond the scope of this standard.

15.6.2 Electromagnetic environment

Sources of interference from the environment include electromagnetic fields, electrostatic discharge, and transient voltages between earth connections. The MAUs shall meet their specifications when operating in an ambient plane wave field of 2 V/m from 10 kHz through 30 MHz, and 5 V/m from 30 MHz through 1 GHz.

NOTE—These are levels typically found 1 km from radio broadcast stations.

The MAUs, stars, and associated connector/cable systems shall comply with applicable local and national codes, such as FCC Docket 20780-1980 [B23] in the USA. Equipment shall comply with local and national requirements for limitation of electromagnetic interference and susceptibility. Where no local or national requirements exist, equipment shall comply with CISPR 22: 1993.

15.6.3 Other environmental requirements

The MAUs, stars, and associated connector/cable systems are expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling such as shock and vibration. Specific requirements and values for these parameters are considered to be beyond the scope of this standard. Manufacturers should indicate in the literature associated with a unit (and on the unit if possible) the operating environment specifications to facilitate selection, installation, and maintenance of these components. It is further recommended that such specifications be stated in standard terms, as specified in IEC 60068, IEC 60874-10:1992, IEC 60793-1:1992, and IEC 60794-1:1993.

15.7 MAU labeling

It is recommended that each MAU (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Whether 10BASE-FP MAU, 10BASE-FB MAU, or 10BASE-FL MAU
b) Data rate capability in Mb/s
c) Power level in terms of maximum current drain (for external MAUs as required by 15.5.3)
d) Any applicable safety warnings
e) Which connector is input and which is output
f) For 10BASE-FP MAUs, the Manufacturer ID and the MAU ID in two separate fields (see 16.3.1.1.3)
g) For 10BASE-FL MAUs, if capable of full duplex operation

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15.7.1 10BASE-FP star labeling

It is recommended that each 10BASE-FP Star (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Label as 10BASE-FP Star
b) Label input/output connectors

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15.8 Protocol implementation conformance statement (PICS) proforma for Clause 15, Fiber optic medium and common elements of medium attachment units and star, type 10BASE-F[46]

15.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 15, Fiber optic medium and common elements of medium attachment units and star, type 10BASE-F, shall complete the following PICS proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. The PICS can be used for a variety of purposes by various parties, including the following:

— As a checklist by the protocol implementer, to reduce the risk of failure to conform to the standard through oversight;
— As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
— As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICs);
— As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

15.8.2 Abbreviations and special symbols

15.8.2.1 Status symbols

The following symbols are used in the PICS proforma:

M is mandatory field/function
O is optional field/function
O.<n> is optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n> is optional field/function, but one and only one of the group of options labeled by the same numeral <n> is required
X is prohibited field/function
<item> is simple-predicate condition, dependent on the support marked for <item>

15.8.2.2 Abbreviations

N/A Not applicable

15.8.3 Instructions for completing the PICS proforma

15.8.3.1 General structure of the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

[46] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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The main part of the PICS proforma is a fixed-format questionnaire divided into subclauses, each containing a group of items. Answers to the questionnaire items are to be provided in the right-most column, either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable), or by entering a value or a set or range of values. (Note that there are some items where two or more choices from a set of possible answers can apply; all relevant choices are to be marked.)

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to the material that specifies the item in the main body of the standard; the fourth column contains values and/or comments pertaining to the question to be answered. The remaining columns record the status of the item—whether the support is mandatory, optional, or conditional—and provide the space for the answers; see also 15.8.3.4.

The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the protocol implementation conformance statement for the implementation in question.

Note that where an implementation is capable of being configured in more than one way, according to the items listed under 15.8.5, Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation's configuration capabilities, if that would make presentation of the information easier and clearer.

15.8.3.2 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features which, although optional, are nonetheless commonly present in implementations of the 10BASE-F protocol.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

15.8.3.3 Exception information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this standard.

Note that a possible reason for the situation described above is that a defect in the standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

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15.8.3.4 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M, O, or X.

If the item referred to by the conditional symbol is marked as supported, the conditional item is applicable, and its status is given by "<s>"; the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

15.8.4 Identification

15.8.4.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation name(s) and version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

15.8.4.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2018, Clause 15, 10 Mb/s Fiber Optic Medium Attachment Unit (MAU) and Medium Specification, type 10BASE-F
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exception items been required?No [ ]Yes [ ] (See 15.8.3.3; The answer Yes means that the implementation does not conform to IEEE 802.3-2018.)	

Date of statement	

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15.8.5 Major capabilities/options

Item	Feature	Reference	Value/Comment	Status	Support
*FP	10BASE-FP Implementation	15.1.1	N/A	0.1	Yes[ ] No [ ]
*FB	10BASE-FB Implementation	15.1.1	N/A	0.1	Yes[ ] No [ ]
*FL	10BASE-FL Implementation	15.1.1	N/A	0.1	Yes[ ] No [ ]

In addition, the following predicate name is defined for use when different implementations from the set above have common parameters:

*FA: FB or FL

15.8.6 PICS Proforma for the fiber optic medium

15.8.6.1 Characteristics of the fiber optic medium

Item	Feature	Reference	Value/Comment	Status	Support
*M1	Fiber size	15.3.1	62.5/125 μm	O	Yes [ ] No [ ]
M2	Attenuation of cabled optical fiber	15.3.1.1	≤ 3.75 dB/km at 850 nm when 62.5/125 μm fiber is used	M1: M	N/A [ ] M: Yes [ ]
M3	Fiber modal bandwidth	15.3.1.2	≥160 MHz·km at 850 nm	M	Yes [ ]
M4	Velocity of propagation	15.3.1.3	≤ 5 μs/km	M	Yes [ ]

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15.8.6.2 Optical medium connector plug and socket

Item	Feature	Subclause	Value/Comment	Status	Support
MC1	Connector plug for termination of fiber	15.3.2	BFOC/2.5—see IEC 60874-10:1992	M	Yes [ ]
MC2	Optical connector loss	15.3.2.1	< 1.0 dB	O	Yes [ ] No [ ]
MC3	Optical connector return loss (10BASE-FP only)	15.3.2.2	> 25 dB	FP: M	N/A [ ]M: Yes [ ]

15.8.6.3 Fiber optic medium insertion loss

Item	Feature	Subclause	Value/Comment	Status	Support
	Fiber optic medium insertion loss		Measured as per ANSI/ EIA/TIA 526-14-1990 [B8], Method A, using optical signal with center wavelength of 850 nm and spectral width of 75 nm		
IL1	10BASE-FP segment insertion loss (including 10BASE-FP Star)	15.3.3.1	Between 16 dB and 26 dB	FP: M	N/A [ ] M: Yes [ ]
IL2	10BASE-FB and 10BASE-FL segment insertion loss	15.3.3.2	< 12.5 dB	FA: M	N/A [ ] M: Yes [ ]
IL3	Range of insertion losses measured across one 10BASE-FP segment or one star output port	15.3.3.1	< 6 dB	FP: M	N/A [ ] M: Yes [ ]

15.8.6.4 Electrical isolation requirements

Item	Feature	Subclause	Value/Comment	Status	Support
IR1	Electrical isolation, optical connector plug to any electrically conducting element in cable	15.3.4	Conforms to J.1	M	Yes [ ]

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16. Fiber optic passive star and medium attachment unit, type 10BASE-FP

NOTE—This MAU is not recommended for new installations. Since September 2003, maintenance changes are no longer being considered for this clause.

16.1 Scope

16.1.1 Overview

This clause, along with Clause 15, defines the functional, electrical, optical, and mechanical characteristics of a fiber optic passive-star system for interconnecting DTEs and repeaters. The relationship of this clause to the OSI Reference Model is shown in Figure 15–1a). This system, which may be interconnected to other 10 Mb/s baseband segments using repeaters, consists of the 10BASE-FP MAU (including a fiber optic MDI specified in 15.2), a 10BASE-FP fiber optic Star, and the fiber optic medium specified in 15.3. The 10BASE-FP MAU provides the means for attaching DTEs and repeaters to a 10BASE-FP Star LAN, and a 10BASE-FP Star provides the only means to interconnect 10BASE-FP MAUs via their MDIs.

16.1.1.1 10BASE-FP medium attachment unit

The 10BASE-FP MAU has the following general characteristics:

a) It supports a totally passive-star topology interconnection means.
b) It connects a DTE or repeater to a 10BASE-FP fiber optic segment.
c) It supports message traffic at a data rate of 10 Mb/s.
d) It permits up to 500 m of fiber optic cable, as specified in 15.3, between 10BASE-FP MAUs and a 10BASE-FP Star. (See B.5.2.)
e) It permits the DTE or repeater to confirm operation of the MAU and availability of the medium.
f) It permits the DTE to test the collision detection circuitry of the MAU.
g) It recodes the preamble prior to transmission at the MDI to allow passive-system collision detection and restores normal preamble to packets received at the MDI.
h) It transmits coded jam during collision for deterministic detection of end of collision.
i) It supports network configurations using the CSMA/CD access mechanism defined in this standard.

16.1.1.2 10BASE-FP Star

The star has the following general characteristics:

a) It supports a totally passive-star topology interconnection means.
b) It receives an optical signal from any 10BASE-FP MAU connected to the passive fiber optic segment and distributes the signal uniformly to all 10BASE-FP MAUs connected to the passive fiber optic segment, including the one from which the transmission originated.
c) It supports message traffic at a data rate of 10 Mb/s.
d) It permits segments of up to 500 m radius of fiber optic cable, as specified in 15.3, among MAUs and the star. (See B.5.2.)
e) It supports system configurations using the CSMA/CD access mechanism defined in this standard.

16.1.1.3 Repeater unit

The repeater unit (Clause 9), along with 10BASE-FP MAUs (making a repeater set), is used to interconnect 10BASE-FP segments to achieve the maximum 10BASE-FP connection path. The repeater is also used to extend the physical system topology by connecting 10BASE-FP segments to 10BASE-FB and 10BASE-FL segments as well as all other 10 Mb/s baseband media types.

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Multiple repeater units are permitted within a single collision domain to provide the maximum connection path length specified in Clause 13. The repeater is not a DTE and therefore has slightly different requirements for its attached MAUs as defined in 9.4.1. It is recommended that repeater sets with 10BASE-FP MAUs provide the auto partition/reconnection algorithm on those ports as specified in 9.6.6.2.

16.2 PMA interface messages

The messages between PLS in the DTE or the repeater and the PMA in the MAU shall comply with the PMA interface messages in 7.2.1 and 15.5.4. The messages between the PMAs over the MDI are summarized below.

16.2.1 PMA-to-MDI interface signal encodings

The following signals are used by the interface messages between the PMA and the MDI.

Code Rule Violation, CRV. See 15.1.2.

Manchester-Coded Data One, CD1. A clocked bit symbol in which the first half is LO and the second half is HI.

Manchester-Coded Data Zero, CD0. A clocked bit symbol in which the first half is HI and the second half is LO.

Manchester Code Violation Zero, MV0. A clocked bit symbol in which the symbol is LO for the bit duration.

Received Idle, RDARK. See 15.2.1.4 and 16.2.3.2.

Transmitted Idle, TDARK. See 15.2.1.4 and 16.2.2.2.

16.2.2 PMA-to-MDI OTD messages

The following messages can be sent by the MAU PMA to the MDI OTD (Optical Transmit Data) circuit:

Message	Circuit	Signal	Meaning
OTD_output	OTD	CD1, CD0	Output information
OTD_idle	OTD	TDARK	No data to be output
OTD_manch_violation	OTD	MV0	Manchester violation to be output

16.2.2.1 *OTD_output*

The PMA sublayer shall send the *OTD_output* message to the OTD circuit when the DTE or repeater outputs a bit of data, as modified by the Preamble Encoding function (see 16.3.1.1 and Figure 16–1), and neither link fault nor jabber has been detected. The physical realization of the *OTD_output* message shall be a CD0 or CD1 signal sent by the PMA.

16.2.2.2 *OTD_idle*

The PMA sublayer shall send the *OTD_idle* message to the OTD circuit when the DTE or repeater sends idle or if either link fault or jabber has been detected. The physical realization of the *OTD_idle* message shall be a TDARK signal sent by the PMA. TDARK shall be a signal with an optical level as specified in 15.2.1.4, Optical Idle Signal Amplitude, and shall have a duration of 1.5 bit times (BT) or greater.

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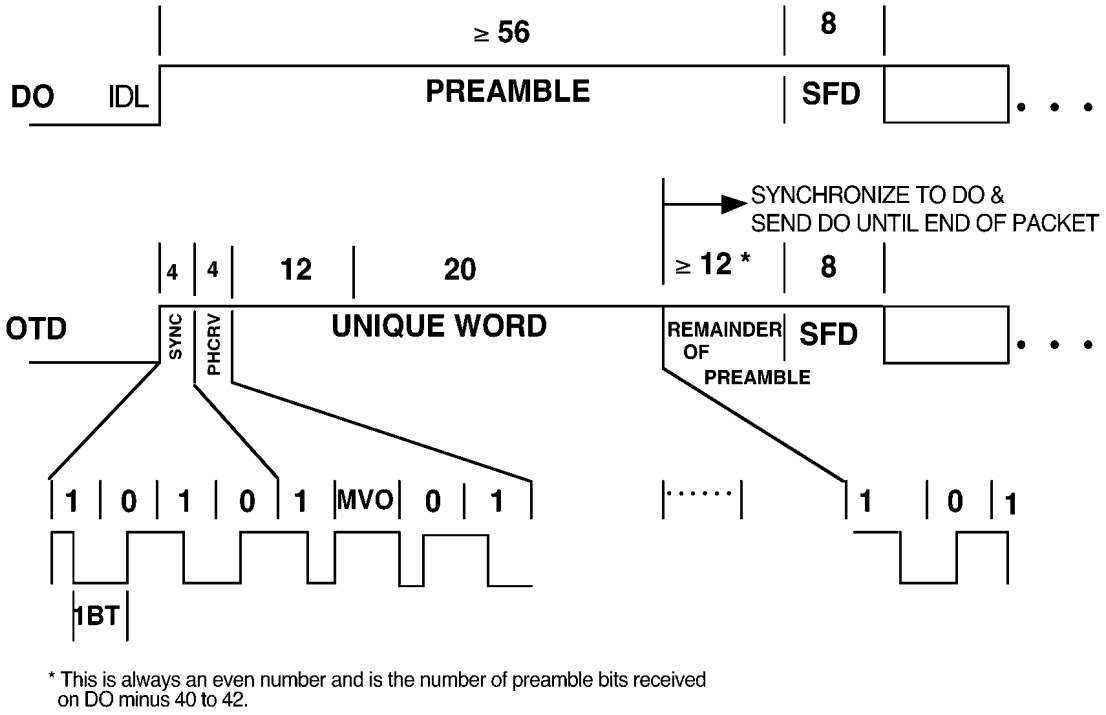

Figure 16–1—10BASE-FP MAU preamble encoding

16.2.2.3 *OTD_manch_violation*

The PMA shall send the *OTD_manch_violation* message whenever the Preamble Encoding function (16.3.1.1) or the Collision Encoding function (16.3.1.3) requires it to do so. The physical realization of the *OTD_manch_violation* message shall be an MV0 signal sent by the PMA.

16.2.3 MDI ORD-to-PMA messages

The following messages can be received by the MAU PMA from the MDI ORD (Optical Receive Data) circuit:

Message	Circuit	Signal	Meaning
ORD_input	ORD	CD1, CD0	Input information
ORD_idle	ORD	RDARK	No information to input
ORD_crv	ORD	CRV	Detected Manchester violation

16.2.3.1 *ORD_input*

When the PMA sublayer receives the *ORD_input* message on its ORD circuit, it detects a bit of data. The physical realization of the *ORD_input* message shall be a CD0 or CD1 signal.

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16.2.3.2 *ORD_idle*

When the PMA sublayer receives the *ORD_idle* message on its ORD circuit, it detects idle. The physical realization of the *ORD_idle* message shall be an RDARK signal. RDARK shall be a signal with an optical level as specified in 15.2.1.4, Idle Signal Amplitude, and shall have a duration of 1.25 BT or greater.

16.2.3.3 *ORD_crv*

When the PMA sublayer receives the *ORD_crv* message on its ORD circuit, it detects a code rule violation. The physical realization of the *ORD_crv* message shall be a CRV signal. CRV is defined in 15.1.2.

16.3 10BASE-FP MAU functional specifications

The MAU component provides the means by which signals on the DO and DI circuits are coupled:

a) From the DTE or repeater to the MAU's transmit MDI, and
b) From the MAU's receive MDI to the DTE or repeater.

Further, simultaneous transmissions from two or more MAUs are reported as a collision on the CI circuit.

To achieve this basic objective, the MAU component shall contain the following functional capabilities to handle message flow between the DTE or repeater and the MDI:

— Transmit function: Provides the ability to transmit serial data bit streams from the attached device into the MAU's transmit MDI.
— Receive function: Provides the ability to receive serial data bit streams from the MAU's receive MDI and transmit them to the attached device.
— Loopback function: Provides the ability to transfer serial data bit streams from the DO to the DI circuit when the MAU is sending data to the OTD circuit.
— Collision Presence function: Provides the ability to detect, and report to the attached device, a collision.
— *signal_quality_error* Message (SQE) Test function: Provides the ability to indicate to the DTE that the Collision Presence function is operational and that the *signal_quality_error* message can be sent by the MAU.
— Jabber function: Provides the ability to detect abnormally long data streams on the DO circuit and inhibit Data Transmit and Receive, SQE Test, Data Loopback, and the Collision Presence function.
— Link Fault Detection and Low Light function: Provides the ability to detect faults in the 10BASE-FP fiber optic segment and inhibit Data Transmit and Receive, SQE Test, Data Loopback, and the Collision Presence function.

16.3.1 Transmit function requirements

The function of the MAU transmitter shall be to transmit the data received at the DO circuit of the AUI onto the MDI. The Transmit function has four purposes:

a) To convert the electrical signals to optical signals.
b) To recode the preamble to guarantee collision detection.
c) To generate a unique jam signal to facilitate deterministic end of collision detection.
d) To retime signals received on the DO circuit.

The levels and timing of the optical signal shall be as specified in 15.2.1. When a packet is received at the DO interface, transmission of encoded preamble at the MDI shall begin within 5.5 BT. The first bit transmit-

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ted onto the fiber from the MDI shall be a CD1 (see 16.3.1.1.1). The signaling rate at the MDI shall be 10 Mb/s ± 0.005%.

NOTE—The tolerance of ±0.005% simplifies the detection of data and collision in the MAU receiver. It may not be necessary to retime signals in an embedded MAU.

16.3.1.1 Preamble encoding

The Transmit function shall replace the first 40 bits of preamble with a pattern consisting of a 4-bit synchronization pattern, a 4-bit packet header Manchester-coding violation pattern (see 16.3.1.1.2), and a 32-bit unique word (see 16.3.1.1.3) as shown in Figure 16–1. Following the unique word, the remainder of the preamble received on the DO shall be transmitted as received subject to the following rules:

a) The encoded preamble shall be aligned with the preamble received from the DO circuit in such a way that the first bit of the remainder is a Manchester-encoded 1; i.e., the remainder of the preamble is CD1, CD0, CD1, CD0,….
b) The number of bits of preamble received from the DO circuit and sent to the MDI prior to the transmission of SFD shall be no less than the total number received from the DO circuit minus 42 bits and no greater than the total number received from the DO circuit minus 40 bits. The above ensures that the preamble transmitted on the OTD circuit is no more than 2 bits shorter than the preamble received from the DO circuit.

The purpose of preamble encoding is to provide synchronization and collision detection information to the Receive function. This unique encoding exists only on the medium and is removed by the receiving MAU.

16.3.1.1.1 Synchronization pattern

The synchronization pattern shall be a Manchester-encoded 1010 (SYNC=CD1 CD0 CD1 CD0). No other pattern, including 0101, is allowed.

16.3.1.1.2 Packet header code rule violation

The packet header code rule violation pattern shall be a fixed, 4-bit pattern that contains a single violation of the Manchester coding rules. The pattern consists of a CD1, MV0, CD0, CD1. The single Manchester violation in the pattern is the only violation allowed in a properly transmitted packet.

16.3.1.1.3 Unique word

The unique word shall be a 32-bit long Manchester-encoded data pattern that is used to guarantee that the preambles sent by any two 10BASE-FP MAUs are different. The word consists of a 12-bit Manufacturer ID assigned by the IEEE Registration Authority and a 20-bit 10BASE-FP MAU ID assigned by the manufacturer to ensure that the 32-bit word is unique. The nature of the Registration Authority and the procedure by which it administers these 12-bit manufacturer identifiers is beyond the scope of this standard. Each of the elements of the unique word shall be transmitted least significant bit first, starting with the Manufacturer ID followed by the MAU ID.

16.3.1.2 Data transmit

The Data Transmit function shall receive the data signals on the DO circuit and send them on the MDI following the encoded preamble.

The steady-state delay between the DO circuit and transmission on the MDI at the time of the start bit in the SFD, shall be no more than 3.5 BT. The difference between start-of-packet propagation delay for any two packets that are separated by 9.6 μs or less shall not exceed 3 BT.

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16.3.1.3 Collision encoding (unique word jam)

After the start of collision (see 16.3.4.2), the Transmit function shall, within 3.5 BT, cease to send the encoded preamble or data from the DO circuit and shall send a repeating, unique, 33-bit pattern. This pattern shall consist of MV0 followed by the 32-bit unique word. In the presence of a collision, a MAU will detect at least two *ORD_crv* within 33 BT and can thereby guarantee accurate detection of end of collision. This pattern shall be repeatedly transmitted at the MDI OTD until the MAU ceases to receive data on the DO circuit. When this occurs, the MAU shall begin sending *OTD_idle* at the MDI within 3.5 BT of the last bit on the DO circuit.

16.3.2 Receive function requirements

The function of the MAU Receive function is to transmit the data received on the MDI ORD circuit into the DI circuit. The Receive function has the following three purposes:

a) To convert optical signals to electrical signals.
b) To replace the coded preamble with normal preamble as specified in 4.2.5.
c) To provide uninterrupted carrier sense during collision presence.

The optical-to-electrical conversion shall be as specified in 15.2.2.3.

16.3.2.1 Preamble reconstruction and alignment

When a packet is received on the MDI ORD circuit, transmission of the reconstructed preamble to the DI circuit shall begin within 2.5 BT. The difference between start-of-packet propagation delay for any two packets that are separated by 9.6 μs or less shall not exceed 1 BT.

The reconstructed preamble shall consist of exactly 40 bits of standard preamble (CD1, CD0, CD1,…CD0) followed by the preamble remainder received on the ORD circuit. The Receive function shall align the preamble remainder such that the 41st bit transmitted on the DI circuit is a Manchester-encoded 1 (CD1).

16.3.2.2 Data receive

The Data Receive function shall receive data signals on the MDI ORD circuit and send them into the DI circuit following the reconstructed preamble.

At the start of SFD reception at the MDI ORD circuit, the steady-state delay between the MDI ORD circuit and the DI circuit shall not exceed 2.5 BT.

16.3.2.3 Signal presence during collision

When a collision is detected (see 16.3.4.2), the Receive function shall transmit Manchester Fill, a sequence of Manchester-encoded alternating CD1s and CD0s on the DI circuit. This Manchester sequence shall be sent on the DI circuit for the duration of activity on the MDI ORD circuit and shall be deasserted within 3 BT from the start of RDARK on the MDI ORD circuit. In addition, the data being sent to the DI circuit shall be monitored and altered to be a valid Manchester sequence if any sequence besides a valid Manchester sequence or RDARK is seen, in the absence of collision yet being signaled.

16.3.3 Loopback function requirements

The MAU shall transmit the bit stream received from the DO circuit into the DI circuit. At the start-of-packet transmission, no more than 2 bits of information shall be received from the DO circuit and not transmitted into the DI circuit. It is permissible for the first bit sent to contain encoded phase violations or invalid data. All successive bits shall be transmitted into the DI circuit and shall exhibit no more edge jitter than that

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specified for signals transmitted into the DI circuit by the Receive function, as specified in 15.2.2.2. The steady-state propagation delay between the DO circuit receiver input and the DI circuit driver output for such signals shall not exceed 1 BT. The MAU's DI circuit driver shall comply with the specification for AUI drivers in 7.4.1. There shall be no logical signal inversions between the DO circuit and the DI circuit during collision-free transmission.

16.3.4 Collision presence function requirements

16.3.4.1 CI Circuit signaling

CI circuit signaling and timing shall meet the requirements of 7.3.1.2, as modified by 15.1.3.3, and 15.5.4.1.

16.3.4.2 Collision detection

The MAU shall detect as a collision the following two cases (see Figure 16–6):

a) DO becoming active while ORD is active, except for the instance where ORD is still active from a previous transmission's loopback from the star.
b) The detection of a second *ORD_crv* without an intervening *ORD_idle*.

The start of collision is measured from the time DO becomes active in case a) above and from the occurrence of the second *ORD_crv* for case b) above.

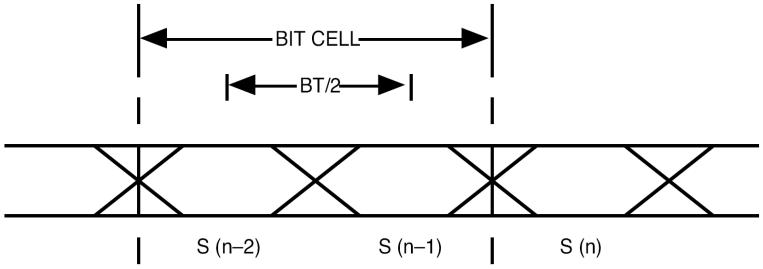
The MAU shall detect *ORD_crv*'s over the received optical power ranges specified in 15.2.2.1. In addition, *ORD_crv* detection shall occur over a differential power range of 8.0 dB.

While a collision is occurring, a CS0 (7.3.1.2) signal shall be sent on the CI circuit. The signal shall be presented to the CI circuit no more than 3.5 BT after start of collision.

If two or more packets arrive simultaneously at the MDI, then the MAU will receive the packet header *ORD_crv* and at least one additional *ORD_crv* during reception of the overlapping unique word patterns. Otherwise the MAU will receive the multiple packet header *ORD_crv*'s from the interfering packet(s).

In order to meet the performance requirements, *ORD_crv* detection needs to be performed in the analog portion of the receiver, as the amplitude information that is essential for *ORD_crv* detection is lost after converting the analog signal into a digital (binary) waveform.

One possible way to detect *ORD_crv* is to compare the amplitudes of three consecutive samples separated by one half BT. The samples are obtained by using a recovered 20 MHz receive clock as shown below.



The differences d1 = | S(n) – S(n-1) | and d2 = | S(n) – S(n-2) | are produced. The computation has to be done once per bit cell, with S(n) being the sample from the first half of the bit cell. In a valid Manchester-encoded sequence, one of these differences has to be zero. Thus, if both differences are above a certain threshold, a Manchester code rule violation (*ORD_crv* message) is detected. The actual value of the threshold is imple-

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mentation dependent but needs to be such that the probability of obtaining an *ORD_crv* when two or more MAUs are sending simultaneously is 100% (also see 15.2.2). Also, at least one of S(n), S(n–1), or S(n–2) has to be HI.

The approach described above may not be the only approach that may meet the requirements for reliable collision detection through *ORD_crv.* The implementer may choose any approach that satisfies the requirements.

NOTE—Implementers are cautioned that optical waveforms received during collisions are the superpositions of multiple transmitted waveforms and that any receive clock synchronization may then be undefined. Under these conditions, collisions will continue to be detected and indicated correctly.

16.3.4.3 End of collision

After detection of a collision (16.3.4.2), CI shall send CS0 until (see Figure 16–2 and Figure 16–6[47])

a) Either DO becomes inactive,
b) ORD becomes idle, or,
c) After waiting for a delay of 54 BT for the unique word jam to loop back from the star, 33 BT have passed with no more than one *ORD_crv.*

The CS0 signal shall be deasserted within 3 BT after any of the above conditions has occurred (see Figure 16–6).

The signal presented on the CI circuit in the absence of collision, SQE Test, or Jabber shall be the IDL signal.

NOTE—The Transmit function (16.3.1) encodes the signal transmitted to guarantee that
a)All transmissions received without collision contain one and only one *ORD_crv*.
b)All transmissions received with collision contain more than one *ORD_crv*.
c)During a collision, spacing between *ORD_crv* events is no more than 32 BT (UWJ has an MV0 every 33 BT).

If a collision is in progress, either the MV0s are in alignment and at least one additional *ORD_crv* will occur during (and because of) the superposition of the unique words, or the MV0s are not in alignment and will be detected in each of the UWJs as *ORD_crv*.

16.3.5 *signal_quality_error* Message (SQE) Test function requirements

The SQE Test function shall be performed by MAUs connected to DTEs and shall not be performed by MAUs connected to repeaters. A capability may be provided in the MAU to activate or inhibit the SQE Test function. It is not required that a MAU determine that it is connected to either a DTE or a repeater and automatically activate or inhibit the SQE Test function. When the SQE test is performed, the MAU shall send CS0 on the CI circuit for a time “SQE_test” beginning a time “SQE_test_wait” after the last positive transition of a packet on the DO circuit. The value of “SQE_test” shall be 10 BT + 5 BT and the value of SQE_test_wait shall be between 0.6 μs and 1.6 μs. This function should use as much of the normal collision detection and signaling circuitry as possible without introducing extraneous signals on the OTD circuit or DI circuit.

16.3.6 Jabber function requirements

The MAU shall contain a self-interrupting capability to prevent an illegally long transmission by the DTE from permanently disrupting transmission on the network (see Figure 16–5). If the transmission exceeds time “xmit_max”, then Jabber shall be detected. The value of “xmit_max” shall be in the range of 20 ms to 150 ms.

Upon detection of the Jabber condition, the MAU shall perform the following:

a) Disable Data Transmit,

[47]The MAU state diagrams, Figures 16–2 through 16–6, follow 16.3.4.3.

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b) Send the CS0 signal on the CI circuit, and
c) Disable the Loopback function (16.3.1.3) from the DO circuit to the DI circuit.

The MAU shall reset the Jabber function after a continuous period of IDL on the DO circuit of time "unjab". The value of "unjab" shall be 0.5 s ± 0.25 s.

The MAU shall not activate its Jabber function when the repeater's MAU Jabber Lockup Protection function operates at its longest permitted time as specified in 9.6.5.

NOTE—It is recommended that the Jabber function be activated when the OTD circuit transmitter is sending *OTD_output* messages for longer than the value of "xmit_max_timer".

16.3.7 Link fault detection and low light function requirements

The MAU shall have the capability, as defined in Figure 16–4, to detect faults in the passive fiber optic segment that may affect the reliable carrier sense required by the CSMA/CD access method. The Link Fault Detection and Low Light function ascertains the integrity of the link, during packet transmission, by detecting the presence, at the MDI ORD circuit, of an optical signal that meets the requirements of 15.2.2.1 returned from the star. The MAU shall detect a Link Fault if, after the start of a packet onto the OTD circuit, time "link_test" elapses with no optical signal having been received on the ORD circuit. The value of "link_test" shall be 10 μs ± 2.5 μs. A Link Fault shall also be detected if the optical power of a received optical signal is not sufficient to maintain a BER of one part in 10^7.

On detection of the Link Fault condition, the MAU shall perform the following:

a) Disable its Data Transmit,
b) Disable its Data Receive, and
c) Disable the Loopback (16.3.1.3) from the DO circuit to the DI circuit.

The MAU shall reset the Link Fault function after time "link_heal", followed by the presence of an optical signal on the ORD circuit having sufficient optical power to maintain a BER of one part in 10^7, and then followed by DO circuit and ORD circuit becoming idle. The value of "link_heal" shall be 0.5 s ± 0.25 s.

The Link Fault state diagram (Figure 16–4) controls the measurement of optical loopback time. The value for link_test has been chosen to ensure that a correctly operating 10BASE-FP MAU attached to a 10BASE-FP Star via an unbroken fiber pair 500 m long will always exit the START LINK TEST state before link_test_ timer_done is asserted.

When not transmitting, and not receiving idle, if the optical power of the received optical signal is not sufficient to maintain a BER of one part in 10^7, the MAU shall set CRV to *true* and send the *ORD_crv* message.

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16.3.8 Interface message time references

Delay and bit loss specifications are measured from the occurrence of messages at the MDI and MAU AUI. A “positive-going” transition is from LO to HI. The following describes the point where each message starts:

Message	Reference
output	leading bit cell boundary (BCB) of first valid CD1 or CD0
output_idle	last positive-going transition prior to start of IDL
input	leading BCB of first valid CD1 or CD0
input_idle	last positive-going transition prior to start of IDL.
signal_quality_error	first transition of valid amplitude
mau_available	last positive-going transition prior to start of IDl
OTD_output	leading BCB of first (valid) CD1 or CD0
OTD_idle	last positive-going transition prior to start of TDARK
OTD_manch_violation	leading BCB of valid MV0
ORD_input	leading BCB of first (valid) CD1 or CD0
ORD_idle	last positive-going transition prior to start of RDARK
ORD_crv	leading BCB of a Manchester code rule violated bit

16.3.9 MAU state diagram

The state diagrams, Figure 16–2 through Figure 16–6, depict the full set of allowed MAU state functions relative to the circuits of the AUI and MDI.

The notation used in the state diagrams follows the conventions in 1.2.1. The variables, timers, and counters used in the state diagrams are defined in the following subclauses.

16.3.9.1 MAU state diagram variables

Variables are used in the state diagrams to indicate the status of MAU inputs and outputs, to control MAU operation, and to pass state information between functions.

In the variable definitions, the name of the variable is followed by a brief description of the variable and a list of values the variable may take. For those variables that are state diagram outputs, one value will be identified as the default. The variable has the default value when no active state contains a term assigning a different value.

The variables used in the state diagrams are as follows:

begin

The interprocess flag controlling state diagram initialization values.
Values: false (default).
true.

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DI

Controls the signal sent by the MAU on the DI circuit.
Values: idle; MAU sends *input_idle*, IDL (default)
DO; MAU sends the signal received on the DO circuit.
Manchester fill; (16.3.2.3).
ORD; MAU sends the Manchester-encoded data received on the ORD circuit.
STANDARD PREAMBLE; MAU sends CD1 CD0 CD1 CD0 etc., preamble as defined in 4.2.5 and described in 16.3.2.1.

CI

Controls the signal sent by the MAU on the CI circuit.
Values: idle; MAU sends *mau_available*, IDL (default).
SQE; MAU sends *signal_quality_error*, CS0.

DO

Status of the signal received by the MAU on the DO circuit.
Values: idle; MAU receives *output_idle*, IDL.
active; MAU receives output, CD0 or CD1.

OTD

Controls the signal sent by the MAU on the OTD circuit.
Values: idle; MAU sends TDARK (default).
MP; MAU sends MODIFIED PREAMBLE (16.3.1.1).
DO; MAU sends the Manchester-encoded data received on the DO circuit.
UWJ; MAU sends UNIQUE WORD JAM (16.3.1.3).

ORD

Status of the signal received by the MAU on the ORD circuit.
Values: idle; MAU receives RDARK.
active; MAU receives CD0, CD1 or CRV.

jab

Interprocess variable that indicates whether a jabber has been detected.
Values: not_detect; jabber not detected (default).
detect; jabber detected.

link_status

Interprocess variable that indicates whether a link fault has been detected.
Values: good; no link fault detected (default).
bad; link fault detected.

col_status

Interprocess variable that indicates whether a CRV *(ORD_crv)* was received near the beginning of a received packet.
Values: good; no CRV fault detected (default).
fault; CRV fault detected.

status

Interprocess variable that indicates if a CRV fault, link fault or a jabber is detected.
Values: ok; link_status=good ∗ jab=not_detect ∗ col_status=good.
fault; link_status=bad + jab=detect + col_status=fault.

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collision

Status of the Collision Detect function.
Values: false; no collision detected (default).
true; collision detected (16.3.4.2).

E_col

Status indicating that a collision was detected in the electrical domain.
Values: false; no electrical collision detected (default).
true; electrical collision detected.

CRV

Status of the code rule violation detector.
Values: false; no code rule violation.
true; a code rule violation has occurred.

SQE_test

A capability may be provided in the MAU to activate or inhibit the SQE Test function. It is not required that a MAU determine that it is connected to either a DTE or a repeater and automatically activate or inhibit the SQE Test function.
Values: false; MAU is connected to a repeater.
true; MAU is connected to a DTE.

MPT

Status indicator for transmission of Modified Preamble.
Values: not done; Modified Preamble being transmitted.
done; transmission of Modified Preamble complete.

MPR

Status indicator for reception of Modified Preamble.
Values: not done; Modified Preamble being received.
done; reception of Modified Preamble complete.

low_light

Status indicator for low light detection.
Values: false; low_light not detected (16.3.7).
true; low_light detected (16.3.7).

16.3.9.2 MAU state diagram timers

All timers operate in the same fashion. A timer is reset and starts counting upon entering a state where “start x_timer” is asserted. At time “x” after the timer has been started, “x_timer_done” is asserted and remains asserted until the timer is reset. At all other times “x_timer_not_done” is asserted.

When entering a state where “start x_timer” is asserted, the timer is reset and restarted even if the entered state is the same as the exited state.

The timers used in the MAU state diagrams are defined as follows:

link_test_timer. The timer for longest time between start of DO and start of ORD before Link Fault state is entered (16.3.7).

link_heal_timer. The timer that defines the time delay from Link Fault detection to start of qualification procedure that resets link_fault (16.3.7 and Figure 16–4).

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SQE_test_timer. The timer for the duration of the Signal Quality Error test signal (16.3.5).

SQE_test_wait_timer. The timer for the delay from end of packet to the start of the SQE test signal (16.3.5).

xmit_max_timer. The timer for excessively long transmit time (16.3.6).

unjab_timer. The timer for the length of time the DO circuit has to be continuously idle to allow transmission to be re-enabled (16.3.6).

16.3.9.3 MAU state diagram counters

All counters operate in the same fashion. A counter is reset (set to zero) upon entering a state where "start_x_cntr" is asserted. The counter then increments each time the associated event occurs until the counter reaches its maximum value.

The counters used in the MAU state diagrams are defined as follows:

CRV_cntr. Counts the number of CRVs. Used to differentiate between collision and UWJ. *Values:* Integers between and including 0 and 2.

EOC_cntr. Counts the number of BTs since last CRV. Used to identify end of collision (when EOC_cntr = 33). *Values:* Integers between and including 0 and 33.

DELAY_cntr. Counts BTs. Used to control the state transition after receiving MV0 in the preamble as a CRV. *Values:* Integers between and including 0 and 108.

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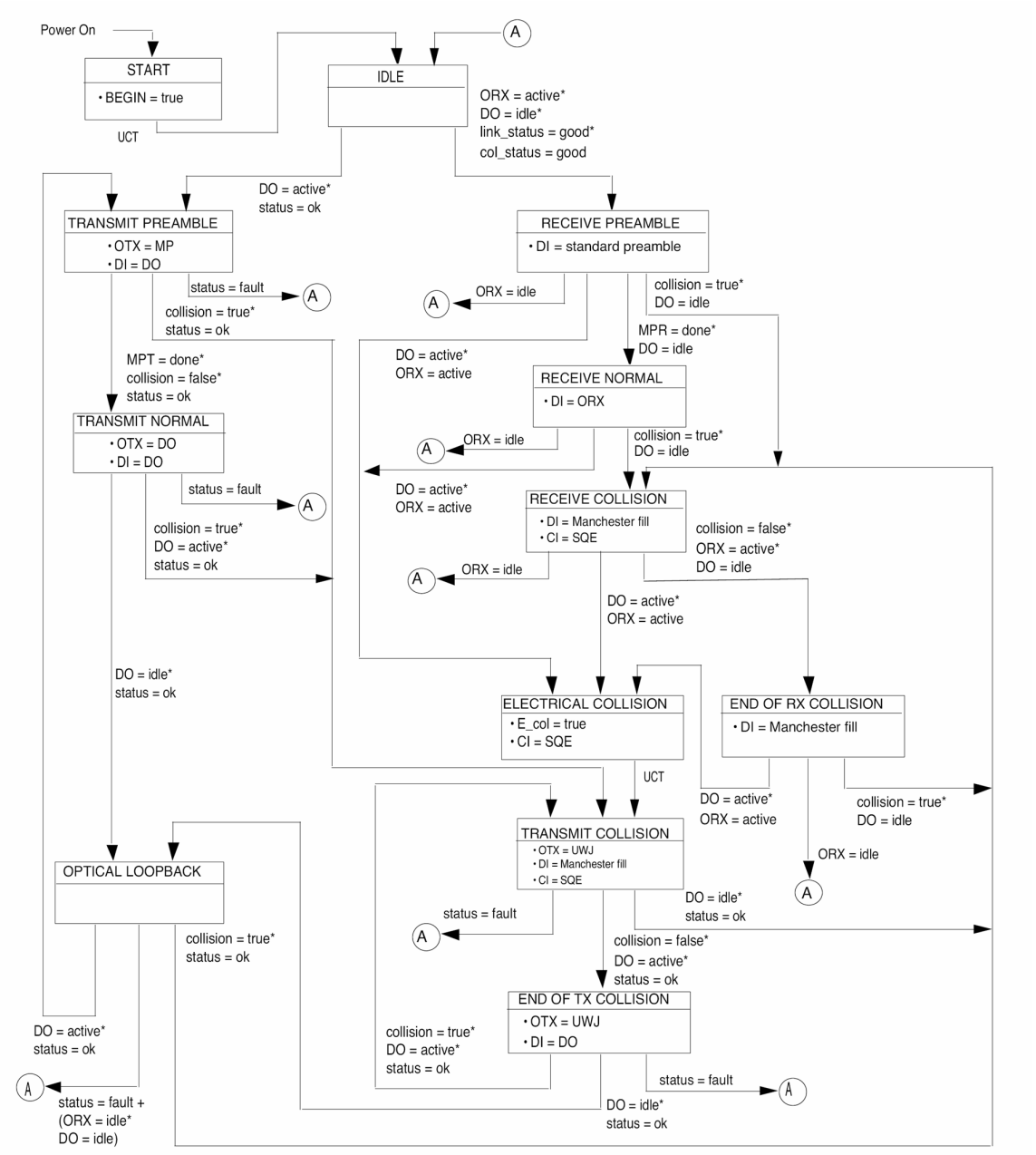

Figure 16–2—Transmit and Receive function state diagram

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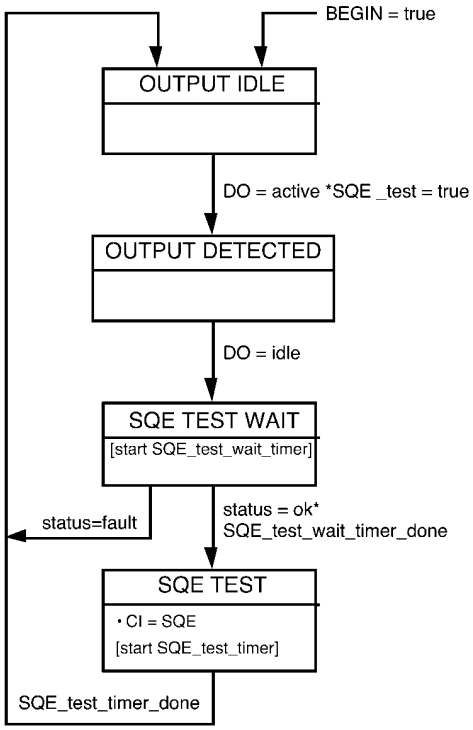

Figure 16–3—*signal_quality_error* Message Test function state diagram

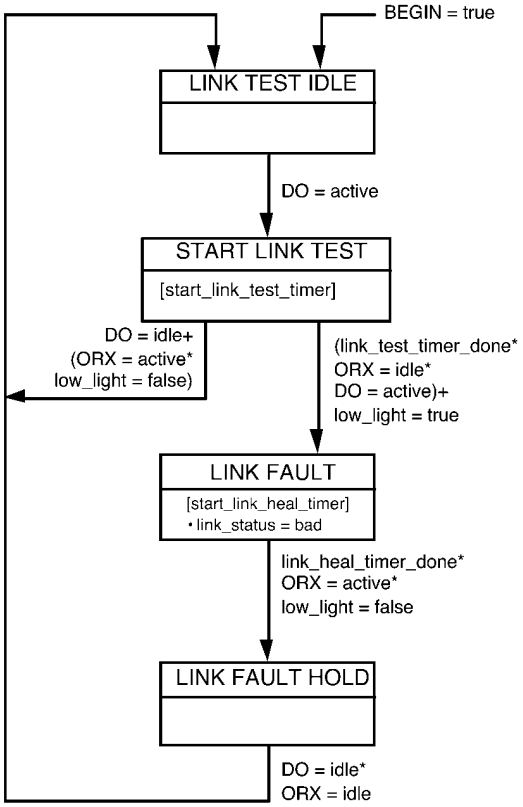

Figure 16–4—Link fault state diagram

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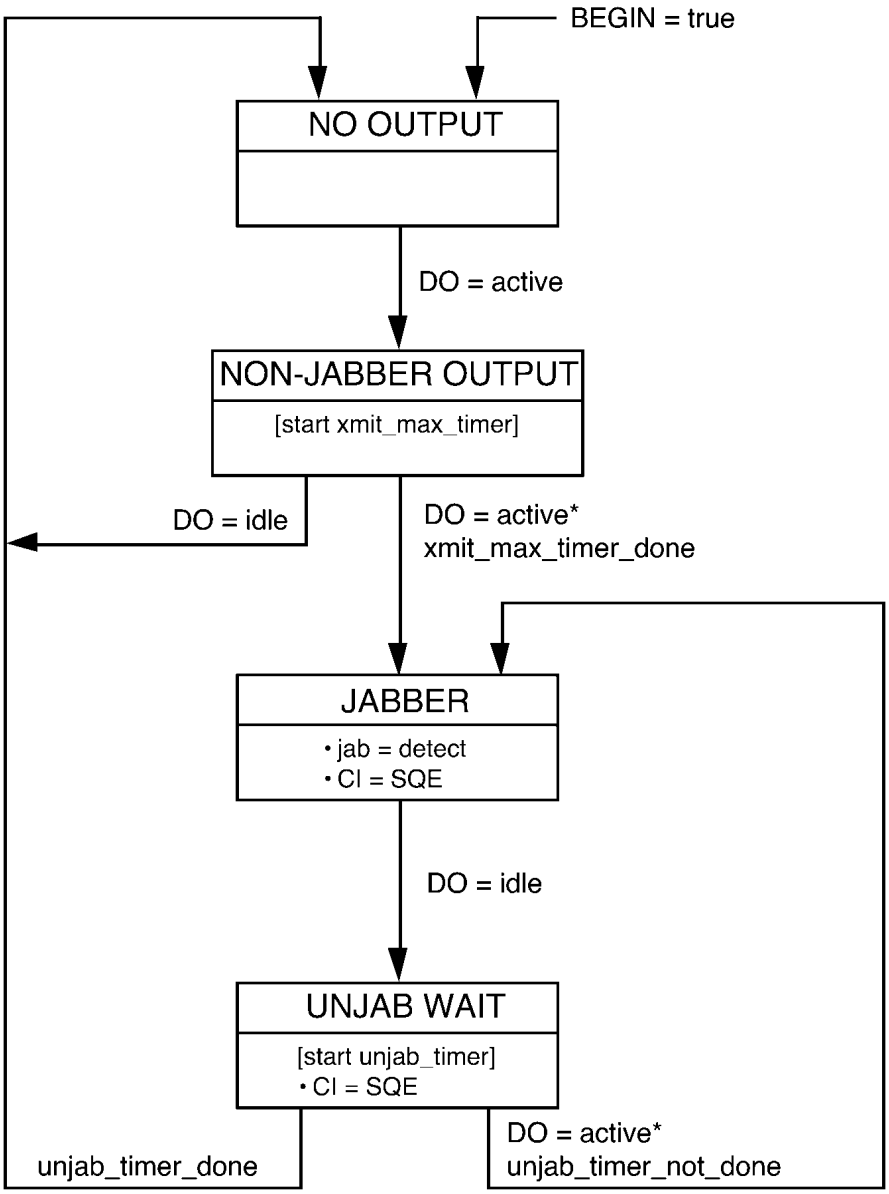

Figure 16–5—Jabber function state diagram

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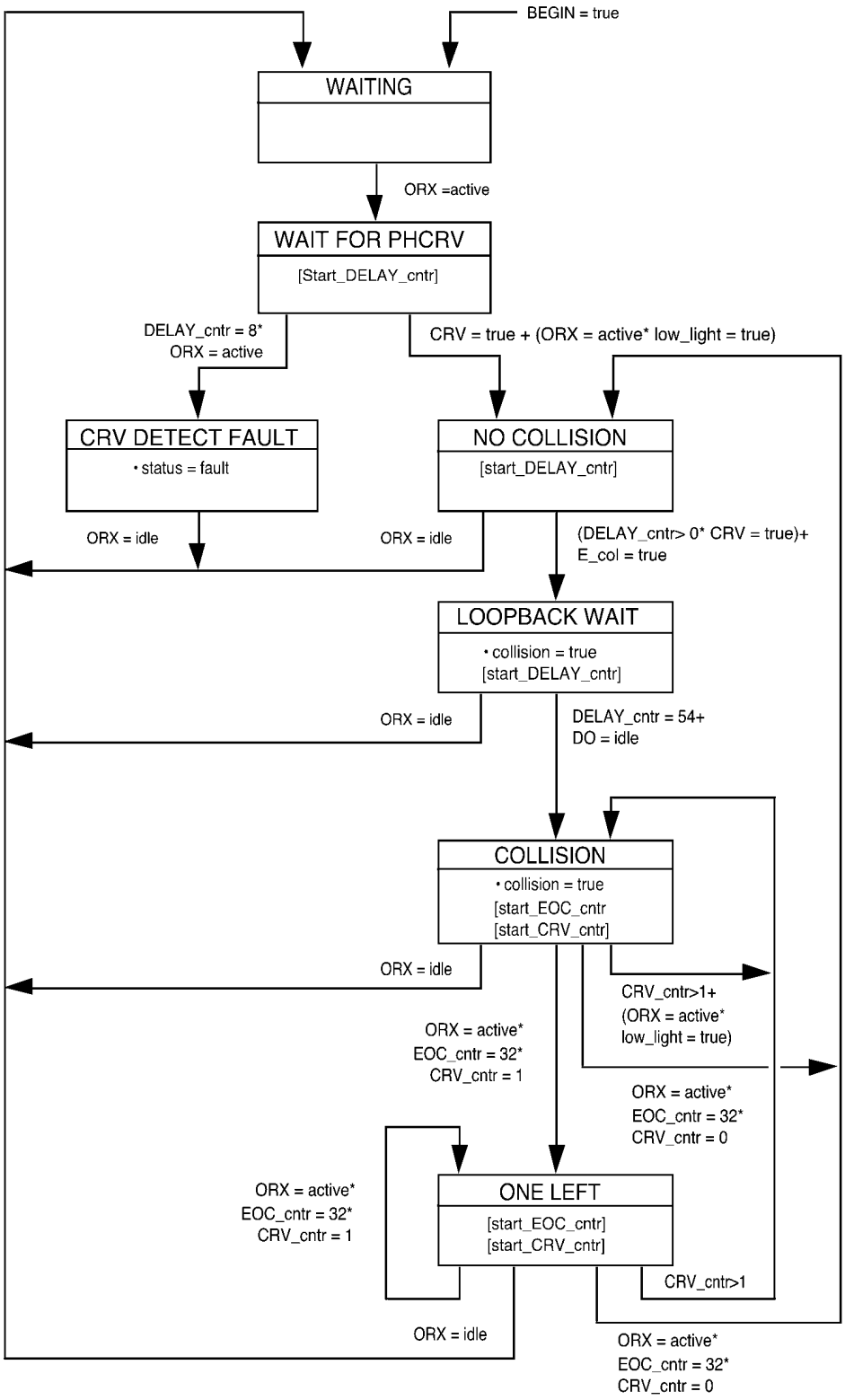

Figure 16–6—Collision detect state diagram

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16.4 Timing summary

Table 16–1 summarizes the timing requirements for 10BASE-FP. This table is a summary; for complete descriptions of the timing to the referenced subclauses. All times are in bit times (BT).

Table 16–1—Maximum timing parameters

Symbol	Function	Bit loss	Invalid bits	Steady-state prop. delay	Start-up delay		
					Max.	Var.	Specified in
M1	*ORD_input* to *input* on DI	0.0	0.0	2.5	2.5	1.0	16.3.2
M2	*output* on DO to *OTD_output*	2.0	0.0	3.5	5.5	3.0	16.3.1
M3	non-looped-back *ORD_input*, and then *output* on DO, to *signal_quality_error* or two *ORD_ crv*, without intervening *ORD_idle*, to *signal_quality_error*				3.5		16.3.4.2
M4a	33 BT with only one *ORD_crv* to *mau_available*			3.0			16.3.4.3
M4b	non-looped-back *ORD_input*, and then *output* on DO, to UWJ as *OTD_output*				3.5		16.3.1.3
M5	while transmitting: two *ORD_crv*, without intervening *ORD_idle*, to UWJ as *OTD_output*			3.5			16.3.1.3
M6	while UWJ as *OTD_output*: *output_idle* to *OTD_idle*			3.5			16.3.1.3
M7	*output_idle* on DO to *signal_quality_error*			6 to 16			16.3.5
M8	*signal_quality_error* duration for SQE test			5 to 15			16.3.5
M9	*output* on DO to *input* on DI	2.0	1.0	1.0	4.0		16.3.3
F1	Fiber Optic Cable Propagation (1000 m)	0	0	50	50		15.3.1.3
A1	AUI Cable Propagation (50 m)	0	0	2.57	2.57		7.4.3.7

16.5 10BASE-FP Star functional specifications

The 10BASE-FP Star provides a means by which the optical signal output from any 10BASE-FP MAU is coupled to the inputs of all 10BASE-FP MAUs attached to the same 10BASE-FP fiber optic segment.

16.5.1 Star functions

16.5.1.1 Number of ports

A star may contain any number of input/output optical interfaces as long as the requirements of 16.5.2 are met.

16.5.1.2 Optical power division

A star shall divide optical power incident on an input port uniformly (within the limits defined in 16.5.2.2) among all output ports without any amplification of the input optical signal.

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16.5.1.3 Configuration

A 10BASE-FP fiber optic segment is configured by attaching a fiber pair between each MAU MDI and a star optical interface. Each MAU OTD circuit shall be connected to an input port of the star, and each MAU ORD circuit shall be connected to an output port. It is recommended for media management purposes to use each output port of the star with its corresponding input port.

16.5.1.4 Reliability

The star shall be designed to provide an MTBF of at least 10 million hours of continuous operation without causing a communication failure among stations attached to the network medium.

16.5.2 Star optical characteristics

16.5.2.1 Star insertion loss

The insertion loss between each input/output optical interface (including the loss of one connector pair) shall be in the range 16 dB to 20 dB, when measured in accordance with ANSI/EIA/TIA 455-180-1990 [B7] using the optical fiber, wavelength, and connector specifications of 15.2.1.1, 15.2.1.2, 15.3.1, and 15.3.2. This insertion loss can generally be met by a star with 33 or fewer input/output optical interfaces. Small-port-count stars may need attenuation in addition to that of the star coupler in order to meet this requirement. A star with more than 33 input/output optical interfaces is not precluded as long as the insertion loss, uniformity, and directivity requirements of this subclause, 16.5.2.2, and 16.5.2.3 are met.

NOTE—The mixing segment insertion loss specified in 15.3.3.1 is generally met by a 33-port star coupler constructed from optical fiber (15.3.1) with connectors (15.3.2) and up to 500 m of optical fiber (15.3.1) on each port. Different sizes and grades of fiber and star coupler may also meet this insertion loss and, while not prohibited, are beyond the scope of this standard.

16.5.2.2 Star single output port uniformity

Single output port uniformity is defined to be the difference between the maximum and minimum insertion loss values (measured according to 16.5.2.1) of any given output port and all input ports. Star single output port uniformity for each output port shall be less than 2.5 dB.

NOTE—Optical uniformity of a star refers to the variation in insertion loss of all input/output port combinations. In the 10BASE-FP system, the uniformity requirement is determined by the receiver. The variation between any given output port and all the input ports needs to be specified. Therefore, it is recommended that each output port connection remain constant during the insertion loss measurements involving that output port. This single output port uniformity is typically better than the overall uniformity of the star.

16.5.2.3 Star directivity

Directivity is the portion of light which is incident on an input port that appears as light emitted from another input port. For the star, directivity for all input optical interface combinations shall be greater than 35 dB. Directivity is measured in accordance with ANSI/EIA/TIA 455-180-1990 [B7] using the optical fiber and wavelength specifications of 15.2.1.1, 15.2.1.2, and 15.3.1.

NOTE—Although passive-star couplers are bidirectional (i.e., light can be transmitted in both directions on one fiber simultaneously), a 10BASE-FP Star cannot use this attribute to support two LANs simultaneously.

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16.6 Protocol implementation conformance statement (PICS) proforma for Clause 16, Fiber optic passive star and medium attachment unit, type 10BASE-FP[48]

16.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 16, Fiber optic passive star and medium attachment unit, type 10BASE-FP, shall complete the following protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. The PICS can be used for a variety of purposes by various parties, including the following:

— As a checklist by the protocol implementer, to reduce the risk of failure to conform to the standard through oversight;
— As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
— As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICs);
— As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

16.6.2 Abbreviations and special symbols

16.6.2.1 Status symbols

The following symbols are used in the PICS proforma:

M	mandatory field/function
O	optional field/function
O.<n>	is optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n>	is optional field/function, but one and only one of the group of options labeled by the same numeral <n> is required
X	is prohibited field/function
<item>:	is simple-predicate condition, dependent on the support marked for <item>

16.6.2.2 Abbreviations

N/A	not applicable

16.6.3 Instructions for completing the PICS proforma

16.6.3.1 General structure of the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

[48] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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The main part of the PICS proforma is a fixed-format questionnaire divided into subclauses, each containing a group of items. Answers to the questionnaire items are to be provided in the right-most column, either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable), or by entering a value or a set or range of values. (Note that there are some items where two or more choices from a set of possible answers can apply; all relevant choices are to be marked.)

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to the material that specifies the item in the main body of the standard; the fourth column contains values and/or comments pertaining to the question to be answered. The remaining columns record the status of the item—whether the support is mandatory, optional, or conditional—and provide the space for the answers; see also 16.6.3.4 below.

The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the protocol implementation conformance statement for the implementation in question.

Note that where an implementation is capable of being configured in more than one way, according to the items listed under 16.6.5, Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation's configuration capabilities, if that would make presentation of the information easier and clearer.

16.6.3.2 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features which, although optional, are nonetheless commonly present in implementations of the 10BASE-FP protocol.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

16.6.3.3 Exception information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this standard.

Note that a possible reason for the situation described above is that a defect in the standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

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16.6.3.4 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M, O, or X.

If the item referred to by the conditional symbol is marked as supported, the conditional item is applicable, and its status is given by "<s>"; the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

16.6.4 Identification

16.6.4.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

16.6.4.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2018, Clause 16, Fiber optic passive star and medium attachment unit, type 10BASE-FP
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See 17.5.3.3; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2018.)	

Date of statement	

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16.6.5 Major capabilities/options

Item	Feature	Reference	Value/Comment	Status	Support
*DTE	MAU supports DTE connections	15.1.1	N/A	O.1	Yes [ ] No [ ]
*RPT	MAU supports repeater connections	15.1.1	N/A	O.1	Yes [ ] No [ ]
*AUI	AUI connection physically exists and is accessible for test	15.1.3.2	N/A	O	Yes [ ] No [ ]

16.6.6 PICS proforma for the type 10BASE-FP MAU

16.6.6.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Compatibility Considerations: 10BASE-FP Systems compatible at 10BASE-FP MDI	15.1.3.2		M	Yes [ ]
CC2	Mode of operation	15.1.3.5	normal mode only	M	Yes [ ]

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16.6.6.2 Optical transmit parameters

Item	Feature	Subclause	Value/Comment	Status	Support
OT1	Center Wavelength	15.2.1.1	min 800 nm max 910 nm	M	Yes [ ]
OT2	Spectral Width (FWHM)	15.2.1.2	< 75 nm	M	Yes [ ]
OT3	Optical Modulation Extinction Ratio	15.2.1.3	< –13 dB	M	Yes [ ]
OT4	Optical Idle Signal Amplitude	15.2.1.4	< 57 dBm	M	Yes [ ]
OT5	Optical Transmit Pulse Logic Polarity	15.2.1.5	High Optical Power = LO on AUI DO and MDI. Low Optical Power = HI on AUI DO and MDI.	M	Yes [ ]
	Optical Transmit Pulse Rise and Fall times	15.2.1.6	Measured from 10% to 90% level		
OT6	Max. (Data)		10.0 ns	M	Yes [ ]
OT7	Min. (Data)		2.0 ns	M	Yes [ ]
OT8	Max. Difference (Data)		3.0 ns	M	Yes [ ]
OT9	Optical Transmit Pulse Over-shoot	15.2.1.7	< 5%	M	Yes [ ]
OT10	Optical Transmit Pulse Under-shoot	15.2.1.7	< 5%	M	Yes [ ]
OT11	Optical Transmit Pulse Edge Jitter, Total at MDI (Data)	15.2.1.8	± 1.0 ns Measured as in 15.2.1.8	M	Yes [ ]
OT12	Optical Transmit Pulse Duty Cycle Distortion (Data)	15.2.1.9	± 1.0 ns max Measured at median power level	M	Yes [ ]
	Optical Transmit Average Power	15.2.1.10			
OT13	Min.		–15 dBm	M	Yes [ ]
OT14	Max.		–11 dBm	M	Yes [ ]
OT15	Transmit signal template	Figure 15–3	Optical signal within template	M	Yes [ ]

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16.6.6.3 Optical receive parameters

Item	Feature	Subclause	Value/Comment	Status	Support
OR1	BER between two AUIs attached to a single segment	15.2.2	< one part in 10^9	M	Yes [ ]
 OR2 OR3	Optical Receive Average Power Min. Max.	15.2.2.1	When a single transmitter transmits on the medium –41.0 dBm –27.0 dBm	 M M	 Yes [ ] Yes [ ]
OR4	MAU optical receive Edge Jitter (Data) Received at MDI	15.2.2.2	± 4.5 ns at median power. Measured as in 15.2.2.2.	M	Yes [ ]
OR5	Optical Receive Pulse Logic Polarity	15.2.2.3	High Optical Power = LO on AUI DI and MDI. Low Optical Power = HI on AUI DI and MDI.	M	Yes [ ]
 OR6 OR7	Optical Receive Pulse Rise and Fall Times: Max. (Data) Min. (Data)	15.2.2.4	Measured from 10% to 90% level 18.5 ns 2.0 ns	 M M	 Yes [ ] Yes [ ]

16.6.6.4 Optical medium connector plug and socket

Item	Feature	Subclause	Value/Comment	Status	Support
CS1	Connector Socket	15.3.2	BFOC/2.5—see IEC 60874-10:1992	M	Yes [ ]

16.6.6.5 MAU functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Transmit	16.3.1		M	Yes [ ]
MF2	Data Loopback	16.3.3		M	Yes [ ]
MF3	Receive	16.3.2		M	Yes [ ]
MF4	Collision Presence	16.3.4		M	Yes [ ]
MF5	Jabber	16.3.6		M	Yes [ ]
MF6	Link Fault Detection	16.3.7		M	Yes [ ]
MF7	Low Light Detection	16.3.7		M	Yes [ ]
MF8	SQE Test	16.3.5		DTE: M	N/A [ ] M: Yes [ ]
				RPT: X	N/A [ ] X: Yes [ ]

16.6.6.6 PMA interface messages

Item	Feature	Subclause	Value/Comment	Status	Support
PIM1	Messages between DTE or repeater PLS and MAU PMA	16.2	As in 7.2.1 and 15.5.4	M	Yes [ ]

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16.6.6.7 PMA to MDI OTD messages

Item	Feature	Subclause	Value/ Comment	Status	Support
OTD1	Signal sent on OTD corresponding to *OTD_output* message	16.2.2.1	CD1,CD0	M	Yes [ ]
OTD2	Signal sent on OTD corresponding to *OTD_idle* message	16.2.2.2	TDARK	M	Yes [ ]
OTD3	TDARK optical level	16.2.2.2	As in 15.2.1.4	M	Yes [ ]
OTD4	TDARK duration	16.2.2.2	≥ 1.5 BT	M	Yes [ ]
OTD5	Signal sent on OTD to ensure detection of collisions: *OTD_manch_violation* message	16.2.2.3	MV0	M	Yes [ ]

16.6.6.8 MDI ORD to PMA messages

Item	Feature	Subclause	Value/ Comment	Status	Support
OTD1	Signal received on ORD corresponding to *ORD_input* message	16.2.3.1	CD1,CD0	M	Yes [ ]
OTD2	Signal received on ORD corresponding to *ORD_idle* message	16.2.3.2	RDARK	M	Yes [ ]
OTD3	RDARK Optical Level	16.2.3.2	As in 15.2.1.4	M	Yes [ ]
OTD4	RDARK Duration	16.2.3.2	≥ 1.25 BT	M	Yes [ ]
OTD5	Signal received on ORD corresponding to *ORD_crv* message	16.2.3.3	CRV	M	Yes [ ]

16.6.6.9 Transmit functions

Item	Feature	Subclause	Value/Comment	Status	Support
XT1	Signaling rate	16.3.1	10 Mb/s ± 0.005%	M	Yes [ ]
XT2	Optical transmit levels and timing	16.3.1	As in 15.2.1	M	Yes [ ]
XT3	Transmit start-up delay	16.3.1	≤ 5.5 BT	M	Yes [ ]
XT4	First bit transmitted	16.3.1	CD1	M	Yes [ ]
XT5	Transmit path	16.3.1	DO circuit to transmit MDI	M	Yes [ ]
XT6	Preamble encoding	16.3.1.1	Replace first 40 bits of preamble with pattern as described	M	Yes [ ]
XT7	Remainder of preamble	16.3.1.1	Transmitted as received	M	Yes [ ]
XT8	Alignment of remainder of preamble	16.3.1.1	CD1,CD0,…	M	Yes [ ]

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16.6.6.9 Transmit functions *(continued)*

XT9	Number of preamble bits received from DO and sent to the transmit MDI prior to transmission of SFD	16.3.1.1	≥ total number received from DO minus 42 bits and ≤ total number received from DO minus 40 bits	M	Yes [ ]
XT10	Synchronization pattern	16.3.1.1.1	CD1,CD0,CD1,CD0	M	Yes [ ]
XT11	Packet header code rule violation	16.3.1.1.2	CD1,MV0,CD0,CD1	M	Yes [ ]
XT12	Unique Word	16.3.1.1.3	32 bit word as described	M	Yes [ ]
XT13	Unique Word order of transmission	16.3.1.1.3	Least significant bit first	M	Yes [ ]
XT14	Data transmit	16.3.1.2	Following preamble, all data received from DO is sent to transmit MDI	M	Yes [ ]
XT15	Transmit steady-state delay	16.3.1.2	3.5 BT max	M	Yes [ ]
XT16	Transmit delay variability	16.3.1.2	3 BT max for packets ≤ 9.6 μs apart	M	Yes [ ]

16.6.6.10 Collision Encoding (Unique Word Jam) function

Item	Feature	Subclause	Value/Comment	Status	Support
CE1	Collision detection to Unique Word Jam transmission delay	16.3.1.3	3.5 BT max	M	Yes [ ]
CE2	Unique Word Jam composition	16.3.1.3	MV0,Unique Word, MV0,Unique Word, MV0,Unique Word, etc.…	M	Yes [ ]
CE3	End of data on DO to end of Unique Word Jam transmission delay	16.3.1.3	3.5 BT max	M	Yes [ ]

16.6.6.11 Receive functions

Item	Feature	Subclause	Value/Comment	Status	Support
RCV1	Optical to Electrical conversion	16.3.2	As specified in 15.2.2.3	M	Yes [ ]

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16.6.6.12 Preamble reconstruction and alignment function

Item	Feature	Subclause	Value/Comment	Status	Support
PRA1	Start-up delay (receive MDI to DI)	16.3.2.1	2.5 BT max	M	Yes [ ]
PRA2	Receive delay variability	16.3.2.1	1 BT max for any two packets ≤ 9.6 μs apart	M	Yes [ ]
PRA3	Reconstructed preamble composition	16.3.2.1	40 bits of CD1,CD0,CD1,…,CD0 followed by remainder of preamble received on receive MDI	M	Yes [ ]
PRA4	Reconstructed preamble alignment	16.3.2.1	41st bit is CD1	M	Yes [ ]

16.6.6.13 Data receive function

Item	Feature	Subclause	Value/Comment	Status	Support
DR1	Receive path (following reconstructed preamble)	16.3.2.2	Receive MDI to DI circuit	M	Yes [ ]
DR2	Steady-state delay (receive MDI to DI)	16.3.2.2	2.5 BT max	M	Yes [ ]

16.6.6.14 Signal presence during collision

Item	Feature	Subclause	Value/Comment	Status	Support
SPC1	Signal transmitted on DI during Collision	16.3.2.3	Manchester Fill (CD1,CD0,CD1, etc.)	M	Yes [ ]
SPC2	Transmit valid Manchester during collision	16.3.2.3	For duration of activity on receive MDI	M	Yes [ ]
SPC3	RDARK to end of valid Manchester delay on DI	16.3.2.3	3 BT max	M	Yes [ ]
SPC4	Signal transmitted on DI during invalid data on receive MDI	16.3.2.3	Valid Manchester sequence	M	Yes [ ]

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16.6.6.15 Loopback function

Item	Feature	Subclause	Value/Comment	Status	Support
LP1	Data Loopback function	16.3.3	DO signals to DI circuit	M	Yes [ ]
LP2	Loopback bit loss (DO to DI)	16.3.3	2 bits max at start of packet	M	Yes [ ]
LP3	Loopback settling time	16.3.3	2nd and following bits shall meet jitter specifications in 15.2.2.2.1	M	Yes [ ]
LP4	Loopback steady-state delay	16.3.3	1 BT max	M	Yes [ ]
LP5	DI circuit driver	16.3.3	See 7.4.1	M	Yes [ ]
LP6	Loopback polarity	16.3.3	No signal inversion from DO to DI	M	Yes [ ]

16.6.6.16 Collision presence function

Item	Feature	Subclause	Value/Comment	Status	Support
CP1	CI signaling and timing	16.3.4.1	As specified in 7.3.1.2, and modified by 15.1.3.3 and 15.5.4.1	M	Yes [ ]
CP2	Collision Detection	16.3.4.2	CS0 on CI if DO = active and ORD = active (if IPG ≥ OTD to ORD loopback time) or two CRVs detected with no intervening *ORD_idle*	M	Yes [ ]
CP3	Collision indication delay	16.3.4.2	3.5 BT max after second CRV or 3.5 BT max after presence of DO = active and ORD = active	M	Yes [ ]
CP4	Received Power range for detection of CRV	16.3.4.2	As specified in 15.2.2.1	M	Yes [ ]
CP5	Received Differential Power Range for detection of CRV	16.3.4.2	8.0 dB	M	Yes [ ]
CP6	End of Collision determination	16.3.4.3	CS0 on CI until DO = inactive or ORD = idle; or after waiting 54 BT, 33 BT with no more than one CRV detected	M	Yes [ ]
CP7	End of Collision deassertion delay	16.3.4.3	3 BT max	M	Yes [ ]
CP8	CI circuit with no collision, SQE Test or jabber	16.3.4.3	IDL	M	Yes [ ]

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16.6.6.17 *signal_quality_error* Message (SQE) test function

Item	Feature	Subclause	Value/Comment	Status	Support
STF1	SQE Test induced OTD or DI signal	16.3.5	No extraneous signals permitted	DTE: M	N/A [ ] M: Yes [ ]
STF2	SQE Test timing (after last positive edge on DO) of CS0 on CI	16.3.5	Start 0.6 µs to 1.6 µs. Duration 5 bits to 15 bits	DTE: M	N/A [ ] M: Yes [ ]

16.6.6.18 Jabber function

Item	Feature	Subclause	Value/Comment	Status	Support
JAB1	Jabber function implementation	16.3.6	Self-interrupt of transmit and loopback	M	Yes [ ]
JAB2	Excessive frame timer for jabber detection	16.3.6	20 ms min., 150 ms max.	M	Yes [ ]
JAB3	CI circuit during jabber	16.3.6	CS0 signal	M	Yes [ ]
JAB4	MAU jabber reset delay	16.3.6	0.5 s ± 0.25 s	M	Yes [ ]
JAB5	State of Loopback function during jabber	16.3.6	Disabled	M	Yes [ ]
JAB6	State of Transmit function during jabber	16.3.6	Disabled	M	Yes [ ]
JAB7	Jabber inhibit	16.3.6	Jabber not activated by the longest permitted output specified in 9.6.5	M	Yes [ ]

16.6.6.19 Link Fault Detect function

Item	Feature	Subclause	Value/Comment	Status	Support
LF1	Link Test Timer	16.3.7	10 µs ± 2.5 µs	M	Yes [ ]
LF2 LF3 LF4	Actions during detected failure: Data Transmit function Data Receive function Loopback function	16.3.7	 Disabled Disabled Disabled	 M M M	 Yes [ ] Yes [ ] Yes [ ]
LF5	Link heal timer	16.3.7	0.5 s ± 0.25 s	M	Yes [ ]
LF6	Receive power level for link fault detect	16.3.7	Not sufficient to maintain BER $< 10^{-7}$	M	Yes [ ]
LF7	Action if receive power level not sufficient to maintain BER $< 10^{-7}$	16.3.7	CRV = true	M	Yes [ ]
LF8	Link fault reset	16.3.7	Expiration of link_heal_timer followed by optical signal of sufficient power to maintain BER $\leq 10^{-7}$	M	Yes [ ]

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16.6.6.20 MAU state diagram requirements

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Transmit and Receive function state diagram	16.3.9	Meets requirements of Figure 16–2	M	Yes [ ]
SD2	SQE Message Test function state diagram	16.3.9	Meets requirements of Figure 16–3	DTE: M	N/A [ ] M: Yes [ ]
SD3	Link Fault state diagram	16.3.9	Meets requirements of Figure 16–4	M	Yes [ ]
SD4	Jabber function state diagram	16.3.9	Meets requirements of Figure 16–5	M	Yes [ ]
SD5	Collision Detect state diagram	16.3.9	Meets requirements of Figure 16–6	M	Yes [ ]

16.6.6.21 MAU-to-AUI signal characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
ASC1	Signaling rate (stated on label)	7.3.2	10 Mb/s	AUI: M	N/A [ ] M: Yes [ ]
ASC2	CS0 signal frequency (on CI)	7.3.1.2	10 MHz ± 15%	AUI: M	N/A [ ] M: Yes [ ]
ASC3	CS0 signal duty cycle	7.3.1.2	60:40 worst case	AUI: M	N/A [ ] M: Yes [ ]

16.6.6.22 MAU-to-AUI DI and CI driver characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
ADC1 ADC2	Differential output voltage: Idle state Start of idle	7.4.1.1	 ≤ 40 mV after 80 BT. Figure 7–12	 AUI: M AUI: M	 N/A [ ] M: Yes [ ] N/A [ ] M: Yes [ ]
ADC3	Current into test load while idle	7.4.1.1	4 mA max after 80 BT	AUI: M	N/A [ ] M: Yes [ ]
ADC4	Requirements after idle	7.4.1.2	1st bit to Figure 7–11	AUI: M	N/A [ ] M: Yes [ ]
ADC5	Common-mode output voltage, ac	7.4.1.3	≤ 2.5 V peak for 30 Hz to 40 kHz, ≤ 160 mV peak for 40 kHz to 10 MHz, Figure 7–13	AUI: M	N/A [ ] M: Yes [ ]
ADC6	Differential output voltage, open circuit	7.4.1.4	13 V peak max	AUI: M	N/A [ ] M: Yes [ ]
ADC7	Common-mode output voltage, dc	7.4.1.5	≤ 5.5 V, Figure 7–1	AUI: M	N/A [ ] M: Yes [ ]
ADC8	Fault tolerance	7.4.1.6	Figure 7–14	AUI: M	N/A [ ] M: Yes [ ]
ADC9	Fault current	7.4.1.6	≤ 150 mA, any state, Figure 7–14	AUI: M	N/A [ ] M: Yes [ ]

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16.6.6.23 AUI-to-MAU DO receiver characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
DO1	Unsquelched threshold	7.4.2.1	160 mV max diff	AUI: M	N/A [ ] M: Yes [ ]
DO2	Squelch	15.5.1	Reject signals < ±160 mV differential	AUI: M	N/A [ ] M: Yes [ ]
DO3	High to idle transition	7.4.1.1	Does not cause output	AUI: M	N/A [ ] M: Yes [ ]
DO4	Differential input impedance	7.4.2.2	Real part: 77.83 Ω ± 6%, 0 ≤ phase angle ≤ real part ∗ 0.0338	AUI: M	N/A [ ] M: Yes [ ]
DO5	Common-mode range, ac	7.4.2.3	3 V min for 30 Hz to 40 kHz, 200 mV min for 40 kHz to 10 MHz	AUI: M	N/A [ ] M: Yes [ ]
DO6	Total common-mode range	7.4.2.4	Magnitude of 0 to 5.5 Vac+dc	AUI: M	N/A [ ] M: Yes [ ]
DO7	Common-mode current limit	7.4.2.4	≤ 1 mA	AUI: M	N/A [ ] M: Yes [ ]
DO8	IDL detection	7.3.1.1	≤ 1.6 BT	AUI: M	N/A [ ] M: Yes [ ]
DO9	Requirements after idle	7.4.2.5	Receiver in specification after start-up delay	AUI: M	N/A [ ] M: Yes [ ]
DO10	Receiver fault tolerance	7.4.2.6	Figure 7–16	AUI: M	N/A [ ] M: Yes [ ]
DO11	Input fault current	7.4.2.6	3 mA max for Figure 7–16	AUI: M	N/A [ ] M: Yes [ ]

16.6.6.24 MAU-to-AUI circuit termination

Item	Feature	Subclause	Value/Comment	Status	Support
ACT1	Common-mode termination	7.5.2.6	If used, is to VC	AUI: M	N/A [ ] M: Yes [ ]
ACT2	Pins 1, 4, 8, 11, 14 impedance to VC circuit	7.5.2.8	≤ 5 Ω at 5 MHz	AUI: M	N/A [ ] M: Yes [ ]
ACT3	Pins 1, 4, 8, 11, 14 coupling to VC circuit	7.5.2.8	Capacitive	AUI: M	N/A [ ] M: Yes [ ]

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16.6.6.25 MAU-to-AUI mechanical connections

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	D-type connector dimensions	7.6.2	IEC 60807-2:1992 15-pole male	AUI: M	N/A [ ] M: Yes [ ]
AM2	Shell plating material	7.6.2	Conductive	AUI: M	N/A [ ] M: Yes [ ]
AM3	Shell multiple contact points	7.6.2	Number not defined (recommended)	AUI: O	N/A [ ] O: Yes [ ] O: No [ ]
AM4	Shell life expectancy	7.6.2	≤ 5 mΩ after 500 matings	AUI: M	N/A [ ] M: Yes [ ]
AM5	Locking posts and mounting	7.6.1	Figures 7–18 and 7–20	AUI: M	N/A [ ] M: Yes [ ]
	Pin connections	7.6.3	Circuit		
AM6	3		Data Out A	AUI: M	N/A [ ] M: Yes [ ]
AM7	10		Data Out B	AUI: M	N/A [ ] M: Yes [ ]
AM8	11		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM9	5		Data In A	AUI: M	N/A [ ] M: Yes [ ]
AM10	12		Data In B	AUI: M	N/A [ ] M: Yes [ ]
AM11	4		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM12	7		No connection	AUI: M	N/A [ ] M: Yes [ ]
AM13	15		No connection	AUI: M	N/A [ ] M: Yes [ ]
AM14	8		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM15	2		Control In A	AUI: M	N/A [ ] M: Yes [ ]
AM16	9		Control In B	AUI: M	N/A [ ] M: Yes [ ]
AM17	1		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM18	6		Voltage common	AUI: M	N/A [ ] M: Yes [ ]
AM19	13		Voltage plus	AUI: M	N/A [ ] M: Yes [ ]
AM20	1		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM21	Shell		Isolated from all pins	AUI: M	N/A [ ] M: Yes [ ]

16.6.6.26 MAU reliability

Item	Feature	Subclause	Value/Comment	Status	Support
MR1	Mean Time Before Failure	15.4	$> 10^7$ hours without causing communications failure among other stations	M	Yes [ ]

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16.6.6.27 Power consumption

Item	Feature	Subclause	Value/Comment	Status	Support
PC1	Power surge limitation	15.5.3	$< 2 \times 10^{-3}$ A–s	APW: M	N/A [ ] M: Yes [ ]
PC2	Power surge duration	15.5.3	100 ms max	APW: M	N/A [ ] M: Yes [ ]
PC3	Steady-state current drawn	15.5.3	≤ 0.5 A	APW: M	N/A [ ] M: Yes [ ]
PC4 PC5	Power-up capability: Current-limited sources Voltage-limited sources	15.5.3 7.5.2.5	0.5 A limited. 11.28 to 15.75 V via any AUI cable	APW: M APW: M	N/A [ ] M: Yes [ ] N/A [ ] M: Yes [ ]
PC6	Labeling	15.5.3	As in 15.5.315.5.3	APW: M	N/A [ ] M: Yes [ ]
PC7	Power cycle behavior	15.5.3	No extraneous signals on MDI, DI, or CI	AUI: M	
PC8	Low VP behavior	7.5.2.5	No disruption of media	APW: M	N/A [ ] M: Yes [ ]
PC9	Power sourced on pin 13 of AUI	15.5.3	None if separate power source is implemented	SPW: X	N/A [ ] X: Yes [ ]
PC10	Optional power source isolation	15.5.3	If implemented, shall withstand one of 15.3.4 tests	SPW: M	N/A [ ] M: Yes [ ]

16.6.6.28 PLS–PMA requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	Messages between PLS in DTE or Repeater and PMA	15.5.4	As in 7.2.1	M	Yes [ ]

16.6.6.29 *signal_quality_error* message (SQE)

Item	Feature	Subclause	Value/Comment	Status	Support
SQE1	Local MAU Transmitting and no Collision or Fault Detected	15.5.4.2.1	*MAU_available* sent on CI	M	Yes [ ]
SQE2	Whenever a Collision exists as described in 16.3.4	15.5.4.2.1	SQE sent	M	Yes [ ]
SQE3	SQE Test as described in 16.3.5	15.5.4.2.1	SQE sent	DTE: M RPT: X	N/A [ ] M: Yes [ ] N/A [ ] X: Yes [ ]
SQE4	Jabber Condition exists as described in 16.3.6	15.5.4.2.1	SQE sent	M	Yes [ ]
SQE5	Message sent in the absence of SQE	15.5.4.2.1	*MAU_available* message	M	Yes [ ]

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16.6.6.30 Environmental requirements

Item	Feature	Subclause	Value/Comment	Status	Support
E1	Ambient plane wave field in which MAU meets specification	15.6.2	2 V/m from 10 kHz to 30 MHz. 5 V/m from 30 MHz to 1 GHz	M	Yes [ ]
E2	Electromagnetic emissions and susceptibility	15.6.2	Comply with local and/or national requirements. If none exist, comply with CISPR 22: 1993.	M	Yes [ ]

16.6.6.31 MAU labeling

Item	Feature	Subclause	Value/Comment	Status	Support
LBL1	MAU Type	15.7	10BASE-FP	O	Yes [ ] No [ ]
LBL2	Data Rate	15.7	10 Mb/s	O	Yes [ ] No [ ]
LBL3	Power Level	15.7	Maximum current drain	O	Yes [ ] No [ ]
LBL4	Safety Warnings	15.7	Any applicable	O	Yes [ ] No [ ]
LBL5	Port Labeling	15.7	Input and output	O	Yes [ ] No [ ]
LBL6	Manufacturer ID and MAU ID	15.7	12-bit Manufacturer ID and 20-bit MAU ID in separate fields	O	Yes [ ] No [ ]

16.6.7 PICS proforma tables for 10BASE-FP stars

16.6.7.1 Star basic functions

Item	Feature	Subclause	Value/Comment	Status	Support
SB1	Optical power division	16.5.1.2	Divide optical power from an input among all outputs (as described in 16.5.2.2)	M	Yes [ ]
SB2	Configuration of 10BASE-FP Stars and MAUs	16.5.1.3	MAU OTD to star input port. MAU ORD to star output port.	M	Yes [ ]
SB3	MTBF without causing communications failure among attached stations	16.5.1.4	10^7 hours	M	Yes [ ]

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16.6.7.2 Star optical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
SO1	Insertion loss	16.5.2.1	16 dB min 20 dB max	M	Yes [ ]
SO2	Single output port uniformity	16.5.2.2	2.5 dB max	M	Yes [ ]
SO3	Directivity	16.5.2.3	35 dB min	M	Yes [ ]
SO4	Connector socket	15.3.2	BFOC/2.5—see IEC 60874-10:1992	M	Yes [ ]
SO5	Optical connector loss	15.3.2.1	< 1.0 dB	O	Yes [ ] No [ ]
SO6	Optical connector return loss	15.3.2.2	> 25 dB	M	Yes [ ]

16.6.7.3 Star environmental requirements

Item	Feature	Subclause	Value/Comment	Status	Support
SE1	Ambient plane wave field in which star meets specification	15.6.2	2 V/m from 10 kHz to 30 MHz. 5 V/m from 30 MHz to 1 GHz	M	Yes [ ]
SE2	Electromagnetic emissions and susceptibility	15.6.2	Comply with local and/or national requirements. If none exist, comply with CISPR 22: 1993.	M	Yes [ ]

16.6.7.4 10BASE-FP star labeling

Item	Feature	Subclause	Value/Comment	Status	Support
SL1	Device type	15.7.1	10BASE-FP Star	O	Yes [ ] No [ ]
SL2	Port labeling	15.7.1	Input and output	O	Yes [ ] No [ ]

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17. Fiber optic medium attachment unit, type 10BASE-FB

NOTE—This MAU is not recommended for new installations. Since September 2011, maintenance changes are no longer being considered for this clause.

17.1 Scope

17.1.1 Overview

This clause, along with Clause 15, defines the functional, electrical, optical, and mechanical characteristics of an optimized fiber optic link for interconnecting repeaters. The relationship of this specification to the sublayers used within this standard is shown in Figure 15-1b). This fiber optic link may be used to interconnect repeaters in star topologies and consists of a new PMA specific to the repeater (including a fiber optic MDI specified in 15.2), and the fiber optic medium specified in 15.3. This clause defines a MAU that extends the link distances beyond MAUs specified in 9.9 and significantly increases the number of allowable repeaters in series. While this clause defines a MAU, the AUI shall exist only as a logical service interface.

17.1.1.1 Medium attachment unit

The 10BASE-FB MAU has the following general characteristics:

a) It enables coupling of the Physical Layer Signaling (PLS) messages to the baseband fiber optic link defined in Clause 15.
b) It supports message traffic at a data rate of 10 Mb/s.
c) It provides for operating over 0 to at least 2000 m of fiber optic cable specified in 15.3.
d) It transmits both data and idle signals synchronously with the bit clock and receives data without resynchronizing on each packet.
e) It connects a repeater to a fiber optic backbone link segment.
f) It provides point-to-point signaling of status via synchronous signaling as defined in 17.2.1.
g) It transmits synchronous signals as defined in 17.2.1.
h) It supports network configurations using the CSMA/CD access method defined in IEEE 802.3 with baseband signaling.
i) It supports a point-to-point interconnection between repeaters, and when used with repeaters having multiple ports, supports a star wiring topology.

17.1.1.2 Relationship to repeater

A close relationship exists between Clause 17 and Clause 9. Clause 17 specifies the PMA logical functions residing in the MAU that exist as an integrated MAU in the repeater. A logical interface using messages associated with the AUI is provided as the interface with the repeater. In addition, the Data Loopback function is provided to ensure proper operation of the Partition function defined in 9.6.6.

17.1.1.3 Remote diagnostic messages

The MAU implements remote status signaling during fault conditions. The MAU transmits status messages defined in 17.2.2 and detects the messages described in 17.2.3.

17.1.2 Relationship to AUI

There is no physical implementation of AUI associated with the MAU. Implementation of an AUI, while possible, is beyond the scope of the International Standard. Messages associated with the AUI, however, are used throughout this document as a means to interface with the repeater. Thus, the sole purpose of the use of

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the messages associated with the AUI is as a service interface. The PMA uses the variables In, Out, and Col and their associated messages to communicate with a port in the repeater.

17.2 PMA interface messages

The messages between a port in the repeater and the PMA in the MAU shall comply with the PMA interface messages in 17.2.1 and 15.5.4. The messages between the PMAs over the MDI are summarized below.

17.2.1 PMA-to-MDI interface signal encodings

The following signals are used by the interface messages between the PMA and the MDI:

Manchester-Encoded Data One, CD. A clocked bit symbol in which the first half is LO and the second half is HI.

Manchester-Encoded Data Zero, CD0. A clocked bit symbol in which the first half is HI and the second half is LO.

Manchester Code Violation One, MV1. A clocked bit symbol in which the symbol is HI for the bit duration.

Manchester Code Violation Zero, MV0. A clocked bit symbol in which the symbol is LO for the bit duration.

Synchronous Idle, SIDL. Control symbol series coded as the repeating sequence of MV1, MV1, MV0, MV0, starting with the first MV1, resulting in 2.5 MHz signal.

Remote Fault, RF. Control symbol series coded as the repeating sequence of MV1, MV1, MV1, MV0, MV0, MV0, starting with the first MV1, resulting in 1.667 MHz signal.

17.2.2 PMA-to-MDI OTD messages

The signals SIDL and RF shall be made up of sequences of the symbols MV1 and MV0 listed in the table and illustrated in Figure 17–1. All signals shall be transmitted synchronized to the local bit clock. SIDL and RF appear only between PMAs. The following messages can be sent by the MAU PMA to the MDI OTD (Optical Transmit Data) circuit:

Message	Circuit	Signal	Meaning
OTD_output	OTD	CD1, CD0	Output information
OTD_sync_idle	OTD	SIDL (MV1, MV1, MV0, MV0)	Synchronous idle
OTD_remote_fault	OTD	RF (MV1, MV1, MV1, MV0, MV0,MV0)	Jabber, Low Light, Invalid Data, or Lock Lost detected

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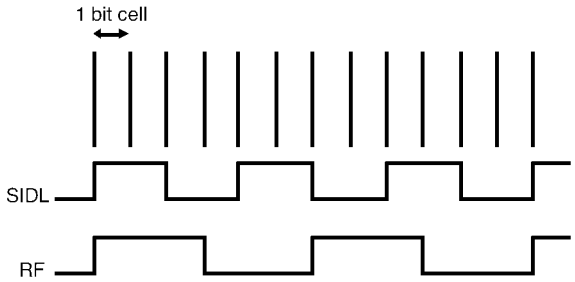

Figure 17–1—MDI status signaling messages

17.2.2.1 OTD_output

The PMA sublayer sends the *OTD_output* message to the OTD circuit when the repeater outputs a bit of data to the MDI's OTD circuit and the MDI's OTD circuit and the PMA is not sending the *OTD_remote_fault* message. The physical realization of the *OTD_output* message is a CD0 or CD1 signal sent by the PMA.

17.2.2.2 OTD_sync_idle

The PMA sublayer sends the *OTD_sync_idle* message to the OTD circuit when the repeater sends idle and the PMA is not sending *OTD_remote_fault* message. The physical realization of the *OTD_sync_idle* message is a repeating sequence of the SIDL signal sent by the PMA.

17.2.2.3 OTD_remote_fault

The PMA sublayer sends *OTD_remote_fault* message to the OTD circuit when receive jabber is detected, low light has been detected, invalid data has been detected, or continuous clock recovery condition per 17.3.8 is not met ("lock_lost" = true). The physical realization of the *OTD_remote_fault* message is a repeating sequence of the RF signal sent by the PMA. The *OTD_remote_fault* message may be sent when local faults other than the receive jabber, low light or invalid data are present on the ORD circuit. However, the partition condition of the repeater port shall not cause *OTD_remote_fault* to be sent.

17.2.3 MDI ORD-to-PMA messages

17.2.3.1 Status decoding

The following messages shall be received by the MAU PMA from the MDI ORD (Optical Receive Data) circuit.

17.2.3.2 ORD_input

When the PMA sublayer receives the *ORD_input* message on its ORD circuit, it detects a bit of data. The physical realization of the *ORD_input* message is the CD0 or CD1 signal.

17.2.3.3 ORD_sync_idle

When the PMA sublayer receives the *ORD_sync_idle* message on its ORD circuit, it detects idle. The physical realization of the *ORD_sync_idle* message is the SIDL signal.

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17.2.3.4 ORD_remote_fault

When the PMA sublayer receives the *ORD_remote_fault* message on its ORD circuit, it detects remote fault. The physical realization of the *ORD_remote_fault* message is the RF signal.

17.2.3.5 ORD_invalid_data

When the PMA sublayer receives signals other than CD0, CD1, SIDL, or RF while low light is not detected, or input signals that do not meet the requirements in 17.2.4 and 17.3.8, it detects invalid data. The physical realization of the *ORD_invalid_data* message is a signal not meeting the above allowed set.

Message	Circuit	Signal	Meaning
ORD_input	ORD	CD1, CD0	Input Information
ORD_sync_idle	ORD	SIDL (MV1, MV1, MV0, MV0)	Synchronous Idle
ORD_remote_fault	ORD	RF (MV1, MV1, MV1, MV0, MV0, MV0)	Jabber, Low Light, Invalid Data, or LockLost=true detected by the far-end MAU
ORD_invalid_data	ORD	Any signal other than CD0, CD1, SIDL or RF	Undefined or asynchronous signal

17.2.4 Transitions between signals

The SIDL to data (CD0 or CD1) transition shall occur at any bit cell boundary. SIDL shall begin with its first MV1 immediately following the last bit cell of a packet. When a fault is detected during data transmission, the RF signal shall be transmitted immediately following the next bit cell boundary, starting with the first MV1. When a signal that contains alternating MV0 and MV1, starting with a MV0, is detected during a data reception, it shall be interpreted as alternating CD0 and CD1 as long as the sequence persists. When a fault is detected during idle, the SIDL sequence shall be completed before sending RF. Other than defined above, any transition from one status signal to another status signal shall begin only after the previous signal has been sent in its entirety.

17.2.5 Signaling rate

The signaling rate shall conform to 7.3.2.

17.3 MAU functional specifications

The MAU provides the means by which repeaters can be connected for backbone applications by the use of synchronous signaling. In addition, the MAU provides the means by which status on one end of the link may be signaled to the other end to provide media diagnostics.

17.3.1 Transmit function requirements

The Transmit function shall transmit the output message received from the repeater unit onto the MDI. The Transmit function has three purposes:

a) To convert the electrical signals to optical signals.
b) To generate the SIDL signal when receiving the *output_idle* message from the repeater.
c) To generate the RF signal.

The levels and timing of the optical signal shall be as specified in 15.2.1, and any transition from one signal to another shall meet the requirements in 17.2.4.

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17.3.1.1 Data transmit

The Transmit function shall receive the output messages from the repeater unit and send them onto the MDI OTD circuit. When a packet is received at this interface, no bit of information shall be received from the repeater and not transmitted to the MDI. In addition, only the bits of information received from the repeater shall be transmitted to the MDI. The start-up and steady-state delay between output message and transmission on the MDI shall each be no more than 2 BT. If a fault is detected during data transmission, data transmission shall cease and the RF signal shall be transmitted as specified in 17.2.4 and 17.3.1.3.

17.3.1.2 Synchronous idle

Whenever the repeater unit sends the *idle* message, SIDL signal shall be sent on the OTD circuit of the MDI, when the PMA is not sending the *OTD_remote_fault* message.

17.3.1.3 Fault signaling

Upon detecting receive jabber as specified in 17.3.6, or low light as specified in 17.3.7, or unqualified input signal as specified in 17.3.8, the Transmit function shall output RF signal on the OTD circuit of the MDI.

17.3.2 Receive function requirements

The Receive function shall receive optical signals from the ORD circuit of the MDI and send *input* or *idle* messages to the repeater unit. The Receive function has two purposes:

a) To convert optical signals to electrical signals.
b) To detect and interpret CD0, CD1, SIDL, and RF.

The optical to electrical conversion shall be as specified in 15.2.2.3.

17.3.2.1 Data receive

The Receive function shall receive the CD0 or CD1 signals from the ORD circuit of the MDI and send *input* messages to the repeater unit. When a packet is received, all bits of information shall be received from the ORD circuit and sent to the repeater unit. In addition, only the bits of information received from the ORD circuit shall be sent to the repeater unit. Any transition of one signal to another not meeting the requirements in 17.2.4 shall be detected as *ORD_invalid_data* message. When *ORD_invalid _data* message is received, data transmission shall be prevented. The start-up and steady-state delay between reception on MDI to *input* message shall be no more than 2 BT.

17.3.2.2 Remote status message handling

The Receive function shall recognize the signals SIDL or RF at the MDI and send the *input_idle* message to the repeater unit. The reception of the RF signal at the MDI shall prevent data transmissions.

17.3.3 Collision function requirements

17.3.3.1 Collision detection

The MAU shall detect as a collision the simultaneous occurrence of *ORD_input* message on the ORD circuit and the *output* message from the repeater. When a collision has occurred, the *signal_quality_error* message shall be sent to the repeater within 3.5 BT.

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17.3.3.2 End of collision

The MAU shall detect as the end of collision either the *output_idle* message or messages other than *ORD_input* received from the ORD circuit. When the end of a collision occurs, the *mau_available* message shall be sent to the repeater within 5 BT and the *input_idle* message shall be sent to the repeater within 5 BT.

17.3.4 Loopback function requirements

The Loopback function is defined to provide the same service interface as other MAUs between the PMD and the repeater. Since this MAU does not have a physical AUI, this function is logically present but not necessarily physically implemented.

When the MAU is transmitting on the OTD circuit and is not receiving *ORD_input* messages on the ORD circuit, the MAU shall transmit either *output* messages as *input* messages or *output_idle* messages as *input_idle* messages. The steady-state propagation delay of this message transfer shall not exceed 2 BT.

17.3.5 Fault-handling function requirements

There are two types of faults that shall be detected: local and remote. The local faults are detection of low light, receive jabber, and invalid data conditions. The remote status signals consist of receptions of normal idle (indicated by the signal SIDL), and remote faults (indicated by the signal RF). Table 17–1 defines the signals that shall be sent onto the media at the port's MDI during fault conditions.

Table 17–1—MDI fault conditions and their states

Fault types	Signal at OTD MDI
Low Light detected	RF
Receive Jabber detected	RF
Invalid Data detected	RF
Receive RF	SIDL

During reception of RF, SIDL shall be transmitted at the MDI, unless there is a local fault.

17.3.6 Jabber function requirements

A MAU shall contain a self-interrupt capability, as described in Figure 17–3, to prevent an illegally long reception of data from reaching the Data-Handling function of the repeater. The MAU shall provide a window "rcv_max" during which the *input* messages may be sent to the repeater unit. The value of "rcv_max" shall be between 8 ms and 12 ms. If a reception exceeds this duration, the jabber condition shall be detected.

Upon detection of the jabber condition, the MAU shall perform the following:

a) Inhibit sending further *input* messages to the repeater unit,
b) Disable the *OTD_sync_idle* message (17.2.2.2) to the MDI, and
c) Send the *OTD_remote_fault* message (17.2.2.3) to the MDI.

The MAU shall reset the Jabber function and reassert *OTD_sync_idle* message when one of the following conditions is met:

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— On power-up reset, or
— After a continuous time “rcv_unjab” of not detecting jabber on the ORD circuit of the MAU (see Figure 17–3).

The value of “rcv_unjab” shall be 0.5 s ± 0.25 s.

17.3.7 Low light level detection function requirements

The MAU shall have the capability to interrupt a port’s reception at the MDI ORD circuit when reliable reception can no longer be assured at that port based on the incoming optical power level.

The MAU shall have a low light level detection capability as defined in Figure 17–2. It shall interrupt reception of any signals from the ORD circuit of the MDI when reliable detection can no longer be assured. This error condition shall not be detected if the average receive optical power level at the MDI exceeds –32.5 dBm in the frequency band between 0.5 MHz to 25 MHz. It shall also not be detected if the low light condition remains for less than 30 BT. It shall be detected before the average receive optical power level at the MDI has fallen to a level that is lower than the average receive optical power level that corresponds to a BER of one part in 10^{10} for the MAU for a duration of 2000 BT. The low light level detected condition shall cease to exist when the received optical power level exceeds the power level required to maintain a BER of one part in 10^{10} and the requirements in 17.3.8 are met.

On detection of the low light level detection condition at its MDI, the MAU shall perform the following:

a) Inhibit sending further input messages to the repeater unit,
b) Inhibit the Data Transmit function,
c) Disable the *OTD_sync_idle* message (17.2.2.2) to the MDI, and
d) Send the *OTD_remote_fault* message (17.2.2.3) to the MDI.

Once the low light condition continuously ceases to exist at the port for a time “low_light_heal” of 0.5 s ± 0.25 s, the MAU shall reset the Low Light function.

17.3.8 Synchronous qualification function requirements

The MAU shall have the capability in Figure 17–2 to interrupt reception at the MDI when reliable reception can no longer be assured based on the loss of clock recovery. The synchronous signaling condition shall be detected at a port if SIDL or RF is detected for the entire duration of the time “validation” of successful and continuous clock recovery. The value of time “validation” shall be between 64 BT and 128 BT. The clock recovery shall tolerate the jitter specified in 15.2.2.2 at the MDI and recover clocks with proper frequency and tolerances. The variable “lock_lost” shall not take the value “true” when the input meets the requirements of 15.2.2. The variable “lock_lost” shall take the value true within 20 μs after the input frequency on the ORD circuit is less than or equal to 1.55 MHz or greater than or equal to 15.5 MHz.

On qualifying the synchronous signaling condition for signals received on the ORD circuit of the MAU, Data Transmit and Data Receive for that port shall be enabled. On loss of synchronous signaling qualification for the MAU, Data Transmit and Data Receive for that port shall be disabled, and the PMA sublayer shall send *OTD_remote_fault* on the MDI.

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17.3.9 Interface message time references

Delay and bit loss specification are measured from the occurrence of messages at the MDIs. The following describes the point where each message starts:

Message	Reference
OTD_output	leading bit cell boundary of first CD1 or CD0
OTD_sync_idle	last positive-going transition prior to start of SIDL
OTD_remote_fault	last positive-going transition prior to start of RF
ORD_input	leading bit cell boundary of first CD1 or CD0
ORD_sync_idle	last positive-going transition prior to start of SIDL
ORD_remote_fault	last positive-going transition prior to start of RF

17.3.10 MAU state diagrams

The state diagrams of Figure 17–2, Figure 17–3, and Figure 17–4[49] depict the full set of allowed MAU state functions relative to the circuits of the MDI and AUI Service Interface. The notation used in the state diagrams follows the conventions in 1.2.1. The variables, counters, and timers used in the state diagrams are defined in the following subclauses.

17.3.10.1 MAU state diagram variables

Variables are used in the state diagrams to indicate the status of the MAU's inputs and outputs, to control its operation, and to pass state information between functions.

In the variable definitions, the name of the variables is followed by a brief description of the variable and a list of values the variable may take. For those variables that are state diagram outputs, one value will be identified as the default. The variable has the default value when no active state contains a term assigning a different value.

The variables used in the state diagrams are as follows:

begin

The interprocess flag controlling state diagram initialization values.
Values: false (default).
true.

OTD

Controls the signal sent by the MAU's PMA to the OTD circuit.
Values: idle; the MAU sends *OTD_sync_idle*, SIDL (default).
output; the MAU sends *OTD_output*; CD0 or CD1, based on the *output* message from the repeater unit.
remote_fault; the MAU sends *OTD_remote_fault*, RF.

ORD

Status of the signal sent by the MAU's ORD circuit to the PMA.
Values: idle; the MAU receives *ORD_sync_idle*, SIDL.
input; the MAU receives *ORD_input*; CD0, CD1, or MV0,MV1 signal sequence meeting 17.2.4.
remote_fault; the MAU receives *ORD_remote_fault*, RF.

[49]The MAU state diagrams, Figure 17–2 through Figure 17–4, follow 17.3.10.2.

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invalid_data; the MAU receives *ORD_invalid_data*, all signals not meeting 17.2.4. and 17.3.8.

OUT

Status of the messages sent by the repeater to the PMA.
Values: idle; receives *output_idle* message from the repeater unit.
output; receives *output* message from the repeater unit.

IN

Controls the signal sent by the MAUs PMA to the repeater.
Values: idle; the MAU sends the *input_idle* message to the repeater (default).
input; the MAU sends the *input* message to the repeater.
OUT; the MAU sends messages from the repeater back to the repeater.

COL

Controls the signal sent by the MAUs PMA to the repeater.
Values: mau_available; the MAU sends the *mau_available* message to the repeater (default).
signal_quality_error; The MAU sends the *signal_quality_error* message to the repeater.

low_light_detected

Controls the paths of the signals received from the ORD circuit.
Values: true; low light condition is being detected.
false; low light condition is not being detected (default).

rcv_jab_detected

Also controls the path of the signals received from the ORD circuit.
Values: false; receive jabber condition is not being detected (default).
true; receive jabber condition is being detected.

low_light_level

Status of the optical signal level received on the ORD circuit.
Values: true; insufficient light is being received for reliable reception (see 17.3.7).
false; sufficient light is being received for reliable reception.

lock_lost

Status of the Synchronous Qualification function of the ORD circuit.
Values: true; clock has not been recovered.
false; clock has been recovered.

link_valid

Interprocess flag indicating that the link is valid.
Values: false; link is determined to be invalid (default).
true; link is determined to be valid.

17.3.10.2 MAU state diagram timers

All timers operate in the same fashion. A timer is reset and starts counting upon entering a state where “start x_timer” is asserted. When the timer has expired, x_timer_done is asserted and remains asserted until the timer is reset. At all other times, x_timer_not_done is asserted. The timer is reset and restarted even if the entered state is the same as the exited state.

The timers used in the MAU state diagrams are defined as follows:

validation_timer. Timer for synchronous link detection (17.3.8).

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rcv_max_timer. Timer for excessively long reception (17.3.6).

rcv_unjab_timer. Timer for the length of time the ORD circuit has to have no excessively long activity to exit the jabber state (17.3.6).

low_light_heal_timer. Timer for low light condition cessation (17.3.7).

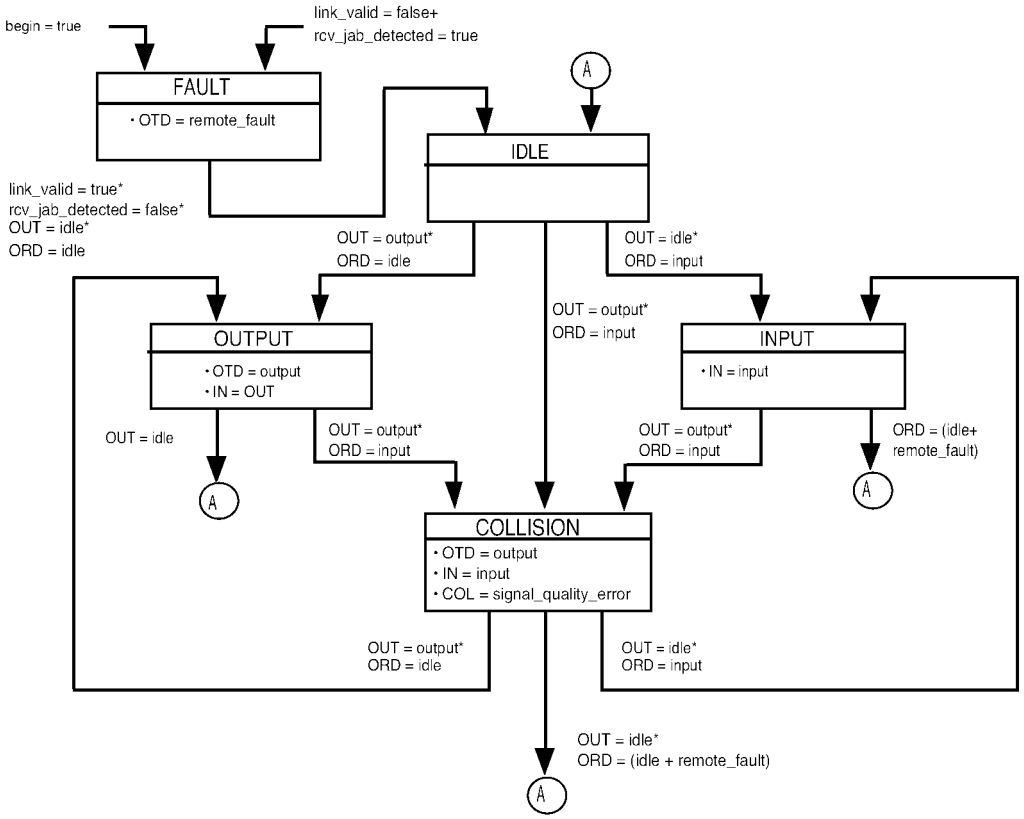

Figure 17–4—MAU transmit, receive, loopback, and collision presence functions state diagram

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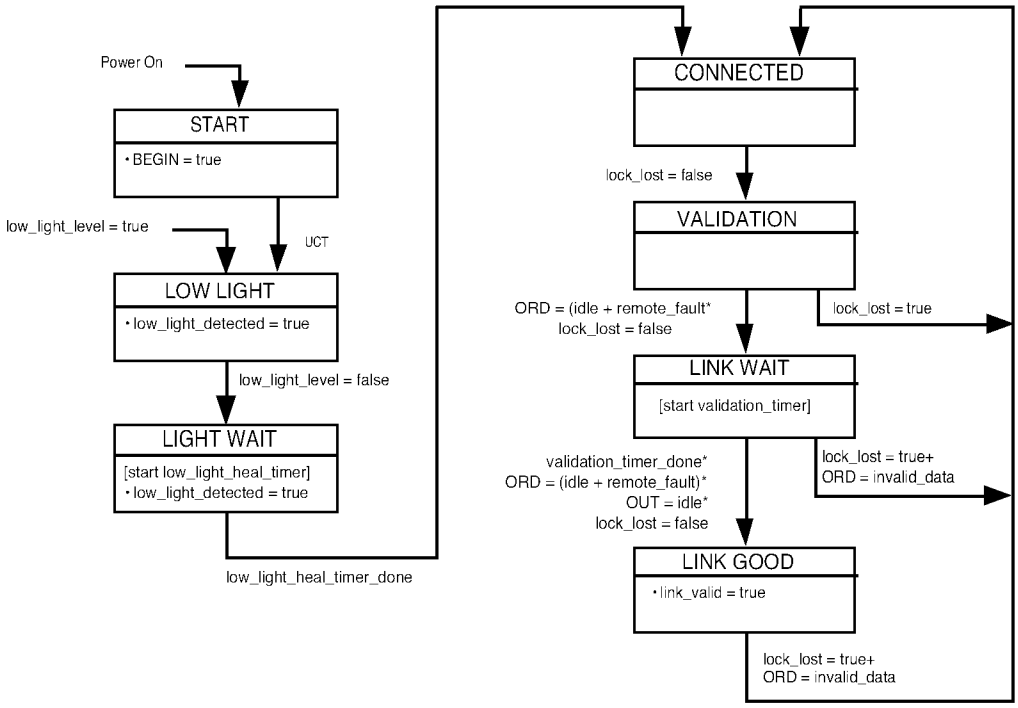

Figure 17–2—Synchronous qualification state diagram

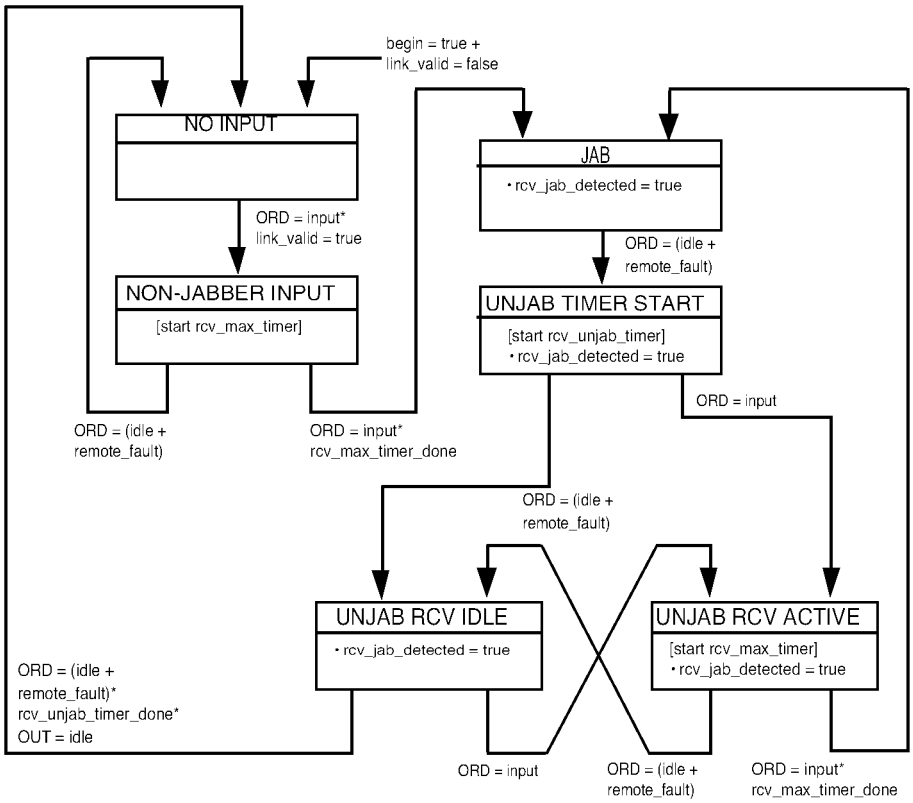

Figure 17–3—Receive jabber state diagram

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17.4 Timing summary

Table 17–2 summarizes the timing requirements for the 10BASE-FB fiber link. This table is a summary; for complete descriptions of the timing requirements, refer to the referenced subclauses. All times are in bit times.

Table 17–2—Maximum timing parameters

Symbol	Function	Bit loss	Invalid bits	Steady-state prop. delay	Start-up delay		Specified in
					Max	Var.	
M1	*ORD_input* to *input* to PMA	0.0	0.0	2.0	2.0	2.0	17.3.2.1
M2	*output* on PMA to *OTD_output*	0.0	0.0	2.0	2.0	2.0	17.3.1.1
M3	ORD_*input* * *output* to *signal_quality_error*				3.5		17.3.3.1
M4	*ORD_sync_idle* + *output_idle* (end of collision) to *mau_available*				5.0		17.3.3.2
M5	*ORD_input* * *output* to *input* to PMA from circuit ORD				5.0		17.3.3.2
M6	*ORD_sync_idle* **output* to *input* to PMA from PMA output circuit				5.0		17.3.3.2
M9	*output* on PMA to *input* to PMA	0.0	0.0	2.0			17.3.4
F1	Fiber Optic Cable Propagation (2000 m)	0	0	100	100		15.3.1.3

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17.5 Protocol implementation conformance statement (PICS) proforma for Clause 17, Fiber optic medium attachment unit, type 10BASE-FB[50]

17.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 17, Fiber optic medium attachment unit, type 10BASE-FB, shall complete the following protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. The PICS can be used for a variety of purposes by various parties, including the following:

— As a checklist by the protocol implementer, to reduce the risk of failure to conform to the International Standard through oversight;
— As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
— As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICs);
— As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

17.5.2 Abbreviations and special symbols

17.5.2.1 Status symbols

The following symbols are used in the PICS proforma:

M mandatory field/function
O optional field/function
O.<n> optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n> optional field/function, but one and only one of the group of options labeled by the same numeral <n> is required
X prohibited field/function
<item>:simple-predicate condition, dependent on the support marked for <item>

17.5.2.1.1 Abbreviations

N/A not applicable

17.5.3 Instructions for completing the PICS proforma

17.5.3.1 General structure of the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

[50] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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The main part of the PICS proforma is a fixed-format questionnaire divided into subclauses, each containing a group of items. Answers to the questionnaire items are to be provided in the right-most column, either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable), or by entering a value or a set or range of values. (Note that there are some items where two or more choices from a set of possible answers can apply; all relevant choices are to be marked.)

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to the material that specifies the item in the main body of the International Standard; the fourth column contains values and/or comments pertaining to the question to be answered. The remaining columns record the status of the item—whether the support is mandatory, optional, or conditional—and provide the space for the answers; see also 17.5.3.4 below.

The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the protocol implementation conformance statement for the implementation in question.

Note that where an implementation is capable of being configured in more than one way, according to the items listed under 17.5.5, Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation's configuration capabilities, if that would make presentation of the information easier and clearer.

17.5.3.2 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features which, although optional, are nonetheless commonly present in implementations of the 10BASE-FB protocol.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

17.5.3.3 Exception information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this International Standard.

Note that a possible reason for the situation described above is that a defect in the International Standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

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17.5.3.4 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M, O, or X.

If the item referred to by the conditional symbol is marked as supported, the conditional item is applicable, and its status is given by "<s>"; the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

17.5.4 Identification

17.5.4.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

17.5.4.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2018, Clause 17, Fiber optic medium attachment unit, type 10BASE-FB
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exception items been required? No [ ]Yes [ ] (See 17.5.3.3; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2018.)	

Date of Statement	

17.5.5 PICS proforma for the type 10BASE-FB MAU

None.

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17.5.6 PICS proforma for the type 10BASE-FB MAU

17.5.6.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Compatibility Considerations: 10BASE-FB Systems compatible at 10BASE-FB MDI	15.1.3.2		M	Yes [ ]
CC2	Mode of operation	15.1.3.5	normal mode only	M	Yes [ ]

17.5.6.2 Optical transmit parameters

Item	Feature	Subclause	Value/Comment	Status	Support
OT1	Center wavelength	15.2.1.1	min. 800 nm max. 910 nm	M	Yes [ ]
OT2	Spectral width (FWHM)	15.2.1.2	< 75 nm	M	Yes [ ]
OT3	Optical modulation extinction ratio	15.2.1.3	< –13 dB	M	Yes [ ]
OT4	Optical idle signal amplitude	15.2.1.4	See 15.2.1.10	M	Yes [ ]
OT5	Optical transmit pulse logic polarity	15.2.1.5	High Optical Power=LO on AUI DO and MDI. Low Optical Power =HI on AUI DO and MDI	M	Yes [ ]
	Optical transmit pulse rise and fall times	15.2.1.6	Measured from 10% to 90% level		
OT6	Max. (Data)		10.0 ns	M	Yes [ ]
OT7	Min. (Data)		0.0 ns	M	Yes [ ]
OT8	Max. difference (Data)		3.0 ns	M	Yes [ ]
OT9	Max. (Idle)		10.0 ns	M	Yes [ ]
OT10	Min. (Idle)		0.0 ns	M	Yes [ ]
OT11	Max. difference (Idle)		3.0 ns	M	Yes [ ]
OT12	Optical Transmit Pulse Overshoot	15.2.1.7	< 25%	M	Yes [ ]
OT13	Optical Transmit Pulse Undershoot	15.2.1.7	< 10%	M	Yes [ ]
	Optical Transmit Pulse Edge Jitter	15.2.1.8	Measured as in 15.2.1.8		
OT14	Added		± 2.0 ns	M	Yes [ ]
OT15	Total at MDI (Data) Total at MDI (Idle)		± 4.0 ns	M	Yes [ ]
	Optical Transmit Pulse Duty Cycle Distortion	15.2.1.9	Measured at median power level		
OT16	Max. (Data)		± 2.5 ns	M	Yes [ ]
OT17	Max. (Idle)		± 2.5 ns	M	Yes [ ]
	Optical Transmit Average Power Range	15.2.1.10			
OT18	Min.		–20 dBm	M	Yes [ ]
OT19	Max.		–12 dBm	M	Yes [ ]
OT20	Transmit Signal Templates	Figure 15–4	Optical signals within template	M	Yes [ ]

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17.5.6.3 Optical receive parameters

Item	Feature	Subclause	Value/Comment	Status	Support
OR1	BER between two AUIs attached to a single segment	15.2.2	< one part in 10^9 (measurement made by inference)	M	Yes [ ]
	Optical Receive Average Power	15.2.2.1	When a single transmitter transmits on the medium		
OR2	Min.		–32.5 dBm	M	Yes [ ]
OR3	Max.		–12.0 dBm	M	Yes [ ]
	MAU optical receive Edge Jitter (Data)	15.2.2.2	Measured as in 15.2.2.2		
OR4	Received at MDI		± 2.0 ns at median	M	Yes [ ]
OR5	Total at DI circuit (MAU end of AUI)		± 6.5 ns at zero crossing points	M	Yes [ ]
OR6	Optical Receive Pulse Logic Polarity	15.2.2.3	High Optical Power = LO on AUI DI and MDI. Low Optical Power = HI on AUI DI and MDI.	M	Yes [ ]
	Optical Receive Pulse Rise and Fall Times	15.2.2.4	Measured from 10% to 90% level		
OR7	Max. (Data)		31.5 ns	M	Yes [ ]
OR8	Min. (Data)		0.0 ns	M	Yes [ ]
OR9	Max. difference (Data)		3.0 ns	M	Yes [ ]
OR10	Max. (Idle)		31.5 ns	M	Yes [ ]
OR11	Min. (Idle)		2.0 ns	M	Yes [ ]
OR12	Max. difference (Idle)		3.0 ns	M	Yes [ ]

17.5.6.4 Optical medium connector plug and socket

Item	Feature	Subclause	Value/Comment	Status	Support
CS1	Connector socket	15.3.2	BFOC/2.5—see IEC 60874-10:1992	M	Yes [ ]

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17.5.6.5 MAU functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Transmit data	17.3.1.1		M	Yes [ ]
MF2	Transmit SIDL	17.3.1.2		M	Yes [ ]
MF3	Transmit RF	17.3.1.3		M	Yes [ ]
MF4	Data Loopback	17.3.4		M	Yes [ ]
MF5	Receive data	17.3.2.1		M	Yes [ ]
MF6	Receive SIDL	17.3.2.2		M	Yes [ ]
MF7	Receive RF	17.3.2.2		M	Yes [ ]
MF8	Collision Presence	17.3.3		M	Yes [ ]
MF9	Fault Handling	17.3.5		M	Yes [ ]
MF10	Jabber	17.3.6		M	Yes [ ]
MF11	Low light level detect	17.3.7		M	Yes [ ]

17.5.6.6 PMA-to-MDI OTD messages and signaling

Item	Feature	Subclause	Value/Comment	Status	Support
OTD1	Repeater port to MAU PMA messages	17.2	As in 7.2.1 and 15.5.4	M	Yes [ ]
OTD2	Signal sent on OTD corresponding to *OTD_output* message	17.2.2	CD1,CD0	M	Yes [ ]
OTD3	Signal sent on OTD corresponding to *OTD_sync_idle* message	17.2.2	SIDL (i.e., MV1, MV1,MV0,MV0)	M	Yes [ ]
OTD4	Signal sent on OTD corresponding to *OTD_remote_fault* message	17.2.2	RF (i.e., MV1,MV1, MV1,MV0,MV0,MV0)	M	Yes [ ]
OTD5	Signal sent on OTD when repeater port is partitioned	17.2.2.3	SIDL (i.e., MV1 MV1,MV0,MV0)	M	Yes [ ]
OTD6	Synchronization of transmitted signals	17.2.2	To local bit clock	M	Yes [ ]
OTD7	AUI	17.1.1	Logical service interface only	M	Yes [ ]

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17.5.6.7 MDI ORD-to-PMA messages and signaling

Item	Feature	Subclause	Value/Comment	Status	Support
ORD1	Signal received on ORD corresponding to *ORD_input* message	17.2.3.2	CD1, CD0	M	Yes [ ]
ORD2	Signal received on ORD corresponding to *ORD_sync_idle* message	17.2.3.3	SIDL (i.e., MV1,MV1, MV0,MV0)	M	Yes [ ]
ORD3	Signal received on ORD corresponding to *ORD_remote_fault* message	17.2.3.4	RF (i.e., MV1,MV1, MV1, MV0,MV0,MV0)	M	Yes [ ]
ORD4	Signal received on ORD corresponding to *ORD_invalid_data* message	17.2.3.5	Not CD0, CD1, SIDL, or RF	M	Yes [ ]

17.5.6.8 Transitions between signals

Item	Feature	Subclause	Value/Comment	Status	Support
TBS1	SIDL to data transition	17.2.4	Only at any bit cell boundary	M	Yes [ ]
TBS2	Start of SIDL	17.2.4	End of last bit cell of packet. Start with first MV1 of signal.	M	Yes [ ]
TBS3	Start of RF	17.2.4	Next bit cell boundary following fault detection. Start with first MV1 of signal.	M	Yes [ ]
TBS4	Transition between status signals	17.2.4	Only after signal sequence has been completed	M	Yes [ ]
TBS5	Interpretation of signal containing alternating MV0 and MV1, starting with MV0	17.2.4	CD0, CD1	M	Yes [ ]

17.5.6.9 Signaling rate

Item	Feature	Subclause	Value/Comment	Status	Support
SR1	Signaling rate	17.2.5	As in 7.3.2	M	Yes [ ]

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17.5.6.10 Transmit functions

Item	Feature	Subclause	Value/Comment	Status	Support
XT1	Data Transmit Path for *output* message	17.3.1	Repeater unit to MDI OTD circuit	M	Yes [ ]
XT2	Levels and timing of optical signal	17.3.1	15.2.1	M	Yes [ ]
XT3	Transition from one signal to another	17.3.1	17.2.4	M	Yes [ ]
XT4	Data Transmit	17.3.1.1	Receives *output* message and sends it on the MDI OTD circuit	M	Yes [ ]
XT5	Information received from repeater and passed to MDI OTD	17.3.1.1	All	M	Yes [ ]
XT6	Information passed to MDI OTD that was not received from repeater	17.3.1.1	None	M	Yes [ ]
XT7	Conditions for SIDL transmission on OTD circuit of the MDI	17.3.1.2	Whenever repeater sends *idle* message and the PMA is not sending the *OTD_remote_fault* message	M	Yes [ ]
XT8	Conditions for RF transmission on OTD circuit of the MDI	17.3.1.3	Whenever *receive_jabber*, *low_light*, or unqualified input signal is detected at port's receive MDI	M	Yes [ ]
XT9	Maximum start-up and steady-state delay circuit of the MDI	17.3.1.1	2 BT between *output* message and transmission on MDI	M	Yes [ ]

17.5.6.11 Receive functions

Item	Feature	Subclause	Value/Comment	Status	Support
RCV1	Data Receive Path for *input* or *idle* message	17.3.2	MDI ORD circuit to repeater unit	M	Yes [ ]
RCV2	Optical to Electrical conversion	17.3.2	15.2.2.3	M	Yes [ ]

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17.5.6.12 Data receive function

Item	Feature	Subclause	Value/Comment	Status	Support
DR1	Bits of information received from ORD MDI and not passed to repeater	17.3.2.1	None	M	Yes [ ]
DR2	Bits of information passed to repeater other than those received from ORD MDI	17.3.2.1	None	M	Yes [ ]
DR3	Signals detected as *ORD_invalid_data*	17.3.2.1	Signals with transitions not meeting 17.2.4 requirements	M	Yes [ ]
DR4	Action when CD0 or CD1 is received on ORD MDI	17.3.2.1	Send *input* message to repeater	M	Yes [ ]
DR5	Maximum start-up and steady-state delay	17.3.2.1	2 BT from reception on MDI to *input* message	M	Yes [ ]
DR6	Action when *ORD_invalid_data* message is received	17.3.2.1	Prevent data transmission	M	Yes [ ]

17.5.6.13 Remote status message handling

Item	Feature	Subclause	Value/Comment	Status	Support
RSM1	Action when SIDL or RF is received on ORD MDI	17.3.2.2	Send *input_idle* message to repeater	M	Yes [ ]
RSM2	Action when RF is received on ORD MDI	17.3.2.2	Prevent data transmission	M	Yes [ ]
RSM3	Action when *ORD_remote_fault* or *ORD_invalid_data* is received	17.3.2.2	Prevent *output* message from the repeater	M	Yes [ ]

17.5.6.14 Collision function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
CF1	Collision Detected	17.3.3.1	Simultaneous occurrence of *output* and *ORD_input*.	M	Yes [ ]
CF2	Action when collision detected	17.3.3.1	Send *signal_quality_error* to repeater within 3.5 BT	M	Yes [ ]

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17.5.6.15 End of collision

Item	Feature	Subclause	Value/Comment	Status	Support
EOC1	End of collision determination	17.3.3.2	*OTD_sync_idle* or messages other than *ORD_input* received from ORD circuit	M	Yes [ ]
EOC2	Action when end of collision is detected	17.3.3.2	Send *mau_available* message and idle message to repeater within 5 BT	M	Yes [ ]

17.5.6.16 Loopback function

Item	Feature	Subclause	Value/Comment	Status	Support
LP1	MAU transmitting on OTD and not receiving *ORD_input* message on the ORD circuit	17.3.4	Transmit *output* messages as *input* messages or transmit *output_idle* messages as *input_idle* messages	M	Yes [ ]
LP2	Steady-state propagation delay	17.3.4	≤ 2 BT	M	Yes [ ]

17.5.6.17 Fault-handling function

Item	Feature	Subclause	Value/Comment	Status	Support
FH1	Types of faults detected	17.3.5	Local and remote	M	Yes [ ]
FH2	Signal at OTD MDI for different fault conditions	17.3.5	See 17.3.5	M	Yes [ ]
FH3	Action during reception of remote fault signals	17.3.5	Transmit SIDL unless local fault detected	M	Yes [ ]

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17.5.6.18 Jabber-handling function

Item	Feature	Subclause	Value/Comment	Status	Support
JAB1	Sending of *input* message to repeater during jabber	17.3.6	Inhibit	M	Yes [ ]
JAB2	Transmission of *OTD_sync_idle* during jabber	17.3.6	Disabled	M	Yes [ ]
JAB3	rcv_max_timer	17.3.6	8 ms min., 12 ms max.	M	Yes [ ]
JAB4	Message sent to repeater during jabber	17.3.6	signal_quality error	M	Yes [ ]
JAB5	Receive unjabber timer duration	17.3.6	0.5 s ± 0.25 s	M	Yes [ ]
JAB6	Detection of jabber	17.3.6	Reception ≥ rcv_max_timer	M	Yes [ ]
JAB7	MAU self-interrupt	17.3.6	As in Figure 17–3	M	Yes [ ]
JAB8	Message sent to OTD MDI during jabber	17.3.6	OTD_remote_fault	M	Yes [ ]
JAB9	Message sent to OTD MDI on power reset or after rcv_unjab_timer	17.3.6	OTD_sync_idle	M	Yes [ ]

17.5.6.19 Low light detection

Item	Feature	Subclause	Value/Comment	Status	Support
LLD1	Low light detection	17.3.7	Interrupt reception of signals from ORD MDI when receive optical power does not support BER of 1 part in 10^{10} for between 30 BT and 2000 BT	M	Yes [ ]
LLD2	Low light not detected	17.3.7	Average receive optical power > –32.5 dBm for 0.5 MHz to 25 MHz frequency band	M	Yes [ ]
LLD3	End of low light	17.3.7	Resume reception of signals from ORD MDI when receive optical power is more than needed to support BER of 1 part in 10^{10}	M	Yes [ ]
LLD4	State of Data Receive	17.3.7	Disabled	M	Yes [ ]
LLD5	State of Data Transmit	17.3.7	Disabled	M	Yes [ ]
LLD6	Signal sent on OTD MDI during low light	17.3.7	RF	M	Yes [ ]
LLD7	Low light state exit timer	17.3.7	0.5 s ± 0.25 s	M	Yes [ ]

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17.5.6.20 Synchronous qualification

Item	Feature	Subclause	Value/Comment	Status	Support
SQ1	Condition for interrupt of reception at MDI	17.3.8	When reliable reception cannot be assured	M	Yes [ ]
SQ2	Synchronous signaling qualification	17.3.8	SIDL or RF detected for the duration of a period between 64 BT and 128 BT of clock recovery valid	M	Yes [ ]
SQ3	Action on successful synchronous signaling qualification	17.3.8	Data Transmit = enabled Data Receive = enabled	M	Yes [ ]
SQ4	Action on loss of synchronous signaling qualification	17.3.8	Data Transmit = disabled Data Receive = disabled *OTD_remote_fault* sent on MDI	M	Yes [ ]
SQ5	Clock recovery jitter tolerance	17.3.8	As in 15.2.2.1	M	Yes [ ]
SQ6	*lock_lost* not true	17.3.8	As in 15.2.2	M	Yes [ ]
SQ7	*lock_lost* true	17.3.8	Within 20 μs when input frequency on ORD ≥ 15.5 MHz or ≤ 1.55 MHz	M	Yes [ ]

17.5.6.21 MAU state diagram requirements

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Synchronous Qualification function state diagram	17.3.10	Meets requirements of Figure 17–2	M	Yes [ ]
SD2	Receive Jabber function state diagram	17.3.10	Meets requirements of Figure 17–3	M	Yes [ ]
SD3	MAU Transmit, Receive, Loopback and Collision Presence Functions state diagram	17.3.10	Meets requirements of Figure 17–4	M	Yes [ ]

17.5.6.22 MAU reliability

Item	Feature	Subclause	Value/Comment	Status	Support
MR1	Mean Time Before Failure	15.4	$> 10^7$ hours without causing communications failure among other stations	M	Yes [ ]

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17.5.6.23 PLS–PMA requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	Messages between PLS in Repeater and PMA	15.5.4	As in 7.2.1	M	Yes [ ]

17.5.6.24 *signal_quality_error* message (SQE)

Item	Feature	Subclause	Value/Comment	Status	Support
SQE1	Local MAU transmitting and no collision or fault detected	15.5.4.2.1	*MAU_available* message sent to repeater	M	Yes [ ]
SQE2	Whenever a collision exists as described in 17.3.3	15.5.4.2.1	*signal_quality_error* message sent to repeater	M	Yes [ ]
SQE3	Message sent in the absence of SQE	15.5.4.2.1	*MAU_available* message	M	Yes [ ]

17.5.6.25 Environmental requirements

Item	Feature	Subclause	Value/Comment	Status	Support
E1	Ambient plane wave field in which MAU meets specification	15.6.2	2 V/m from 10 kHz to 30 MHz. 5 V/m from 30 MHz to 1 GHz.	M	Yes [ ]
E2	Electromagnetic emissions and susceptibility	15.6.2	Comply with local and/or national requirements. If none exist, comply with CISPR 22: 1993.	M	Yes [ ]

17.5.6.26 MAU labeling

Item	Feature	Subclause	Value/Comment	Status	Support
LBL1	MAU Type	15.7	10BASE-FB	O	Yes [ ] No [ ]
LBL2	Data Rate	15.7	10 Mb/s	O	Yes [ ] No [ ]
LBL3	Safety Warnings	15.7	Any applicable	O	Yes [ ] No [ ]
LBL4	Port Labeling	15.7	Input and output	O	Yes [ ] No [ ]

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18. Fiber optic medium attachment unit, type 10BASE-FL

18.1 Scope

18.1.1 Overview

This clause, along with Clause 15, defines the functional, electrical, optical, and mechanical characteristics of a fiber optic link for interconnecting DTEs and repeaters. The relationship of this specification to the OSI Reference Model is shown in Figure 15-1c). This link, which may be interconnected to other 10 Mb/s baseband segments using repeaters, consists of a 10BASE-FL MAU (including a fiber optic MDI specified in 15.2), and the fiber optic medium specified in 15.3. The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the LAN medium.

18.1.1.1 10BASE-FL medium attachment unit (MAU)

The 10BASE-FL MAU has the following general characteristics:

a) It enables coupling the PLS by way of the AUI to the baseband fiber link defined in Clause 15.
b) It supports message traffic at a data rate of 10 Mb/s.
c) It provides for operating over 0 to at least 2000 m of the fiber optic cable specified in 15.3 without the use of a repeater.
d) It permits the DTE or repeater to confirm operation of the MAU and availability of the medium.
e) It supports network configurations using the CSMA/CD access method with baseband signaling.
f) It supports a point-to-point interconnection between MAUs and, when used with repeaters having multiple ports, supports a star wiring topology.
g) It allows incorporation of the MAU within the physical bounds of a DTE or repeater.

18.1.1.2 Repeater unit

The repeater unit is used to extend the physical system topology and provides for coupling two or more segments. Repeaters are an integral part of all 10BASE-FL networks with more than two DTEs (see Figure 13–1 and Figure 13–2). The repeater unit is defined in Clause 9. Multiple repeater units are permitted within a single collision domain to provide the maximum connection path length specified in Clause 13. The repeater unit is not a DTE and therefore has slightly different requirements for its attached MAUs as defined in 9.4.1. It is recommended that repeater sets with 10BASE-FL MAUs provide the Auto Partition/ Reconnection algorithm on those ports as specified in 9.6.6.2.

18.2 PMA interface messages

The messages between the PLS in the DTE and the PMA in the MAU shall comply with the PMA interface messages described in 7.2.1. These messages also are used in repeater unit to PMA communication. The messages between the PMA and the PLS in the DTE are specified in 15.5.4.1 and 15.5.4.2. These messages are also used in repeater unit to PMA communications. The messages between the PMAs and the fiber optic link segment are summarized in the following subclauses.

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18.2.1 PMA to fiber optic link segment messages

The following messages can be sent by the MAU PMA to the Fiber Optic Link Segment:

Message	Circuit	Signal	Meaning
OTD_output	OTD	CD1, CD0	Output information
OTD_idle	OTD	OPT_IDL	No information to output

18.2.1.1 *OTD_output*.

The PMA sublayer sends the *OTD_output* message to the OTD (Optical Transmit Data) circuit when the DTE or repeater outputs a bit of data, the MAU is available and is in the link test pass state. The physical realization of the *OTD_output* message shall be a CD0 or CD1 signal sent by the PMA. The encoding for CD1 and CD0 is the same as used on the AUI. Retiming of the CD1 and CD0 signals within the MAU is neither prohibited nor required.

18.2.1.2 OTD_idle

The PMA sublayer sends the *OTD_idle* message to the OTD circuit when the DTE or repeater sends idle; or upon detection of jabber or link integrity test failure. The physical realization of the *OTD_idle* message shall be the OPT_IDL defined in 18.3.1.1.

18.2.2 Fiber optic link segment to PMA messages

The following messages can be received by the MAU PMA from the Fiber Optic Link Segment:

Message	Circuit	Signal	Meaning
ORD_input	ORD	CD1, CD0	Input information
ORD_idle	ORD	OPT_ILD	No information to input

18.2.2.1 ORD_input

When the PMA sublayer receives the *ORD_input* message on its ORD (Optical Receive Data) circuit, it detects a bit of data. The physical realization of the *ORD_input* message shall be a CD0 or CD1 signal.

18.2.2.2 ORD_idle

When the PMA sublayer receives the *ORD_idle* message on its ORD circuit, it detects idle. The physical realization of the *ORD_idle* message shall be the OPT_IDL signal defined in 18.3.1.1.

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18.2.3 Interface message time references

Delay and bit loss specifications are measured from the occurrence of messages at the MDI and MAU AUI. A "positive-going" transition is from LO to HI. The following describes the point where each message starts:

Message	Reference
output	leading bit cell boundary (BCB) of first valid CD1 or CD0
output_idle	last positive-going transition prior to start of IDL
input	leading BCB of first valid CD1 or CD0
input_idle	last positive-going transition prior to start of IDL
signal_quality_error	first transition of valid amplitude
mau_available	last positive-going transition prior to start of IDL
OTD_output	leading BCB of first valid CD1 or CD0
OTD_idle	last positive going_transition prior to start of OPT_IDL
ORD_output	leading BCB of first valid CD1 or CD0
ORD_idle	last positive-going transition prior to start of OPT_IDL

18.3 MAU functional specifications

The MAU provides the means by which signals on the three AUI signal circuits to and from the DTE or repeater and their associated interlayer messages are coupled to the fiber optic link segment. The MAU provides the following functional capabilities to handle message flow between the DTE or repeater and the fiber optic link segment:

a) Transmit function. Provides the ability to transfer Manchester-encoded data from the DO circuit to the OTD circuit. While not sending Manchester-encoded data on the OTD circuit, an idle signal, OPT_IDL, is sent on the OTD circuit.
b) Receive function. Provides the ability to transfer Manchester-encoded data from the ORD circuit to the DI circuit. While not sending Manchester-encoded data on the DI circuit, an idle signal, IDL, is sent on the DI circuit.
c) Loopback function (half duplex mode only). Provides the ability to transfer Manchester-encoded data from the DO to the DI circuit when the MAU is sending Manchester-encoded data to the OTD circuit.
d) Collision Presence function. Provides the ability to detect simultaneous occurrence of Manchester-encoded data on the ORD and DO circuits and to report such an occurrence as a collision.
e) *signal_quality_error* Message (SQE) Test function. Provides the ability to indicate to the DTE that the Collision Presence function is operational and that the *signal_quality_error* message can be sent by the MAU.
f) Jabber function. Provides the ability to prevent abnormally long reception of Manchester-encoded data on the DO circuit from indefinitely disrupting transmission on the network. While such a condition is present, transfer of Manchester-encoded data by the Transmit and Loopback functions is disabled.
g) Link Integrity Test function. Provides the ability to protect the network from the consequences of failure of the simplex link attached to the ORD circuit. While such a failure is present, transfer of Manchester-encoded data by the Transmit, Receive, and Loopback functions is disabled.

18.3.1 MAU functions

The MAU shall provide the Transmit, Receive, Loopback, Collision Presence, Jabber, and Link Integrity Test functions for half duplex mode DTEs and repeater units. The MAU shall provide the Transmit, Receive, Jabber, and Link Integrity Test functions, and shall not provide the Loopback function, for full duplex mode

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DTEs. The SQE Test function shall be performed by MAUs that are connected to half duplex DTEs and shall not be performed by MAUs that are connected to repeaters.

MAUs connected to full duplex mode DTEs are permitted, but not required, to implement the Collision Presence function, the SQE Test function, and the generation of the CS0 signal on the CI circuit by the Jabber function. If these optional capabilities are implemented in a MAU connected to a full duplex mode DTE, either all of the optional functions shall be implemented, or none of them shall be.

The MAU function requirements are summarized in the table below:

MAU connected to:			
Function	**Repeater**	**Half duplex DTE**	**Full duplex DTE**
Transmit	Required	Required	Required
Receive	Required	Required	Required
Loopback	Required	Required	Prohibited
Jabber	Required	Required	Required
Link Integrity Test	Required	Required	Required
Collision Presence	Required	Required	Optional (note 2)
SQE Test	Prohibited	Required	Optional (note 2)
Generation of CS0 signal on the CI circuit by Jabber	Required	Required	Optional (note 2)

NOTE 1—The functional requirements of a MAU connected to a full duplex DTE are a proper subset of the requirements for half duplex operation.
NOTE 2—Optional capabilities, if implemented, have to be implemented as a group (i.e., all or none).

A capability may be provided in the MAU to activate or inhibit the SQE Test function or to configure the MAU for full or half duplex operation. It is not required that a MAU determine that it is connected to either a DTE or a repeater and automatically activate or inhibit the SQE Test function. It is also not required that a MAU determine that it is connected to either a half duplex or full duplex DTE and automatically activate or inhibit the appropriate functions for those modes.

18.3.1.1 Transmit function requirements

The MAU shall receive messages on the DO circuit and send the appropriate signals to the OTD circuit of the MDI.

At the start of a packet transmission, no more than 2 bits shall be received from the DO circuit and not transmitted on the OTD circuit. In addition, it is permissible for the first bit sent to contain phase violations or invalid amplitude. All subsequent bits of the packet shall be reproduced with levels and timing meeting the specifications of 15.2.1. The second bit transmitted on the OTD circuit shall be transmitted with the correct timing and signal levels. The steady-state propagation delay between the DO circuit input and the OTD circuit shall not exceed 2.0 BT.

For any two packets that are separated by 9.6 ms or less, the startup delay (bit loss plus steady-state propagation delay) of the first packet shall not exceed that of the second packet by more than 2.0 BT.

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Whenever data is not being transmitted on the OTD circuit, an idle signal, OPT_IDL, shall be transmitted on the OTD circuit. OPT_IDL consists of a start of idle (4 BT to 21 BT of the lower light level) followed by a periodic pulse waveform of frequency 1 MHz +25%, –15%. Following a packet and the start of idle, the periodic pulse wave form shall start with a transition to the higher optical light level.

Transmission of OPT_IDL may be terminated at any time with respect to the periodic pulse waveform. It shall be terminated such that no more than the first transmitted bit of a packet is corrupted, and with no more delay than is specified for bit loss and steady-state propagation.

18.3.1.2 Receive function requirements

The MAU shall receive the signals on the ORD circuit of the MDI and send the appropriate message to the DI circuit. The optical-to-electrical conversion shall be as specified in 15.2.2.3.

At the start of a packet reception from the ORD circuit, no more than 2 bits shall be received on the ORD circuit and not transmitted onto the DI circuit. In addition, it is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall be sent with no more than the amount of jitter specified in 15.2. The steady-state propagation delay between the ORD circuit and the DI circuit shall not exceed 2.0 BT.

For any two packets that are separated by 9.6 μs or less, the startup delay of the first packet shall not exceed that of the second packet by more than 2.0 BT.

18.3.1.3 Loopback function requirements (half duplex mode only)

When the MAU is transmitting on the OTD circuit and is not receiving *ORD_input* messages (18.2.2.1) on the ORD circuit, the MAU shall transmit on the DI circuit the signals received on the DO circuit in order to provide loopback of the transmitted signal. At the start-of-packet transmission on the OTD circuit, no more than 5 bits of information shall be received from the DO circuit and not transmitted to the DI circuit. In addition, it is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall meet the jitter specified in 15.2. The steady-state propagation delay between the DO circuit and the DI circuit shall not exceed 1.0 BT.

18.3.1.4 Collision Presence function requirements (half duplex mode only)

The MAU shall detect as a collision the simultaneous occurrence of activity on the DO circuit and the ORD circuit while in the Link Test Pass state. While a collision is detected, a CS0 signal (see 7.3.1.2) shall be sent on the CI circuit. The signal shall be presented to the CI circuit no more than 3.5 BT after the occurrence of a collision. The signal shall be de-asserted within 7.0 BT after the DO circuit or the ORD circuit changes from active to idle.

When CS0 is asserted on the CI circuit due to a collision, the data on the ORD circuit shall be sent to the DI circuit within 9.0 BT.

When the ORD circuit changes from active to idle and data is present on the DO circuit, the data on the DO circuit shall be sent to the DI circuit within 7.0 BT.

The signal presented on the CI circuit in the absence of collision, SQE test, or Jabber shall be the IDL signal.

MAUs connected to full duplex mode DTEs are permitted, but not required, to implement the Collision Presence function (see 18.3.1).

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18.3.1.5 *signal_quality_error* Message (SQE) Test function requirements

The SQE Test function shall be performed by MAUs that are connected to DTEs and shall not be performed by MAUs that are connected to repeaters. When the SQE test is performed, the MAU shall send CS0 on the CI circuit for a time "SQE_test" beginning a time "SQE_test_wait" after the last positive transition of a packet on the DO circuit. The value of "SQE_test" shall be 10 BT ±5 BT and the value of "SQE_test_wait" shall be between 0.6 and 1.6 μs. This function should use as much of the normal collision detection and signaling circuitry as possible without introducing extraneous signals on the OTD circuit or the DI circuit.

The CS0 signal shall not be sent by the SQE Test function while in any of the Link Test Fail states.

MAUs connected to full duplex mode DTEs are permitted, but not required to implement the SQE Test function (see 18.3.1).

18.3.1.6 Jabber function requirements

The MAU shall contain a self-interrupt capability to prevent an illegally long transmission by a DTE from permanently disrupting transmission on the network and to disable loopback to the DI circuit (Figure 18–3). The MAU shall provide a window "xmit_max" during which time the Transmit function may continuously transmit *OTD_output* messages to the OTD circuit. The value of "xmit_max" shall be between 20 and 150 ms. If a transmission exceeds this duration, the Jabber function shall

a) Inhibit the Loopback function and the transmission of *OTD_output* messages by the Transmit function, and shall
b) Send the CS0 signal on the CI circuit, when the MAU is connected to a DTE operating in half duplex mode. MAUs connected to DTEs operating in full duplex mode are permitted, but not required, to send the CS0 signal on the CI circuit in this manner (see 18.3.1).

These actions shall continue until *output_idle* has been continuously present on the DO circuit for a time "unjab." The value of "unjab" shall be 0.5 s ± 0.25 s.

It is permissible to activate the Jabber function when the OTD circuit transmitter is sending *OTD_output* messages for longer than "xmit_max."

The MAU shall not activate its Jabber function when the repeater's MAU Jabber Lockup Protection function operates at its longest permitted time as specified in 9.6.5.

18.3.1.7 Link Integrity Test function requirements

In order to protect the network from the consequences of a simplex fiber optic link segment failure, the MAU shall monitor the light level on the ORD circuit. When a light level below that required for reliable reception (low light) is detected, the MAU shall enter the Link Test Fail Low Light state and cause the *input_idle* message to be sent on the DI circuit and the *OTD_idle* message to be sent on the OTD circuit (Figure 18–4).

Low light shall not be detected if the optical power level at the ORD circuit exceeds –32.5 dBm. Low light shall also not be detected if the low light condition remains for less than 30 BT. It shall be detected and the Link Test Fail Low Light state entered if the optical power level at ORD circuit has fallen to a level lower than the optical power level that corresponds to a BER = 10^{-10} for the MAU for a duration of 2000 BT. Additionally, when the optical receive average power has maintained a value less than –30 dBm for 2000 BT and then falls lower than the level that corresponds to a BER = 10^{-10} for the MAU for a duration of 500 BT, low light shall be detected and the Link Test Fail Low Light state entered.

The MAU shall exit the Link Test Fail Low Light state once the optical power level on the ORD circuit exceeds –32.5 dBm for 0.5 s ±0.25 s. Exiting the Link Test Fail Extend state and entering the Link Test Pass state (thus,

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re-enabling the OTD and DI circuits) shall be deferred until the signals on the ORD and DO circuits become idle. Optionally, a MAU may exit the Link Test Fail Extend state and enter the Link Test Pass state when the ORD circuit becomes idle and the Jabber function has disabled transmission on the OTD circuit.

While the MAU is not in the Link Test Pass state, the Link Integrity Test function shall disable the bit transfer of the Transmit, Receive, and Loopback functions, and the Collision Presence and SQE Test functions.

At power-on, in place of entering the Link Test Pass state as shown in Figure 18–4,[51] a MAU may optionally enter the Link Test Fail Low Light state.

If a visible indicator is provided on the MAU to indicate the link status, it is recommended that the color be green and that the indicator be labeled appropriately. It is further recommended that the indicator be on when the MAU is in the Link Test Pass state and off otherwise.

18.3.1.8 Auto-Negotiation

The Auto-Negotiation algorithm of Clause 28, while the preferred method for the determination of half or full duplex operation, is not currently defined for fiber MAUs.

Manual configuration, while not recommended for copper-based MAUs, is the only practical choice for fiber implementations. Connecting incompatible DTE/MAU combinations such as a full duplex mode DTE to a half duplex mode MAU, or a full duplex mode station (DTE and MAU) to a half duplex network, can lead to severe network performance degradation, increased collisions, late collisions, CRC errors, and undetected data corruption.

18.3.2 MAU state diagrams

The state diagrams of Figure 18–1a), Figure 18–1b), Figure 18–2, Figure 18–3, and Figure 18–4 depict the full set of allowed MAU state functions relative to the circuits of the AUI and MDI.

The notation used in the state diagrams follows the conventions in 1.2.1. The variables and timers used in the state diagrams are defined in the following subclauses.

18.3.2.1 MAU state diagram variables

Variables are used in the state diagrams to indicate the status of MAU inputs and outputs, to control MAU operation, and to pass state information between functions.

In the variable definitions, the name of the variable is followed by a brief description of the variable and a list of values the variable may take. For those variables which are state diagram outputs, one value will be identified as the default. The variable has the default value when no active state contains a term assigning a different value.

For example, the variable “xmit” has the value “disable” whenever the Jabber function or the Link Integrity Test function is in a state that asserts “xmit=disable”. The variable has the default value “enable” all other times.

[51]The MAU state diagrams, Figures 18–1 through 18–4, follow 18.3.2.2.

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The variables used in the state diagrams are defined as follows:

DI

Controls the signal sent by the MAU on the DI circuit.
Values: idle; MAU is sending *input_idle*, IDL (default).
DO; MAU sends the signal received on the DO circuit.
lpbk = disable overrides this and causes *input_idle* to be sent.
ORD; MAU sends the signal received on the ORD circuit.
rcv = disable overrides this and causes *input_idle* to be sent.

CI

Controls the signal sent by the MAU on the CI circuit.
Values: idle; MAU sends *mau_available*, IDL (default).
SQE; MAU sends *signal_quality_error*, CS0.

DO

Status of the signal received by the MAU on the DO circuit.
Values: idle; MAU is receiving *output_idle*, IDL.
active; MAU is receiving *output*, CD0 or CD1.

OTD

Controls the signal sent by the MAU on the OTD circuit.
Values: idle; MAU sends *OTD_idle*, OPT_IDL (default).
DO; MAU sends the signal received on the DO circuit.
xmit = disable overrides this and causes *OTD_idle* to be sent.

ORD

Status of the signal received by the MAU on the ORD circuit.
Values: idle; MAU is receiving *ORD_idle*; OPT_idle.
active; MAU is receiving *ORD_input*; CD0 or CD1.

low_light_level

Status of the light level received by the MAU on the ORD circuit.
Values: false; MAU is receiving sufficient light level for reliable reception.
true; MAU is not receiving sufficient light level for reliable reception (see 18.3.1.7).

rcv

Controls the path from the ORD circuit to the DI circuit.
Values: enable; receive is enabled (default).
disable; the output to the DI circuit will be input_idle when DI=ORD.

lpbk

Controls the path from the DO circuit to the DI circuit.
Values: enable; loopback is enabled (default).
disable; the output to the DI circuit will be input_idle when DI=DO.

xmit

Controls the path from the DO circuit to the OTD circuit.
Values: enable; transmit is enabled (default).
disable; transmit is disabled and the signal sent on the OTD circuit will be OPT_IDL.

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18.3.2.2 MAU state diagram timers

All timers operate in the same fashion. A timer is reset and starts counting upon entering a state where start x_timer is asserted. Time x after the timer has been started, x_timer_done is asserted and remains asserted until the timer is reset. At all other times, x_timer_not_done is asserted.

When entering a state where start x_timer is asserted, the timer is reset and restarted even if the entered state is the same as the exited state.

low_light_heal_timer. Timer for low light condition cessation.

SQE_test_timer. Timer for the duration of the CS0 signal used for the SQE Test function (18.3.1.5).

SQE_test_wait_timer. Timer for the delay from end of packet to the start of the CS0 signal used for the SQE Test function (18.3.1.5).

unjab_timer. Timer for the length of time the DO circuit has to be continuously idle to allow transmission to be re-enabled (18.3.1.6).

xmit_max_timer. Timer for excessively long transmit time (18.3.1.6).

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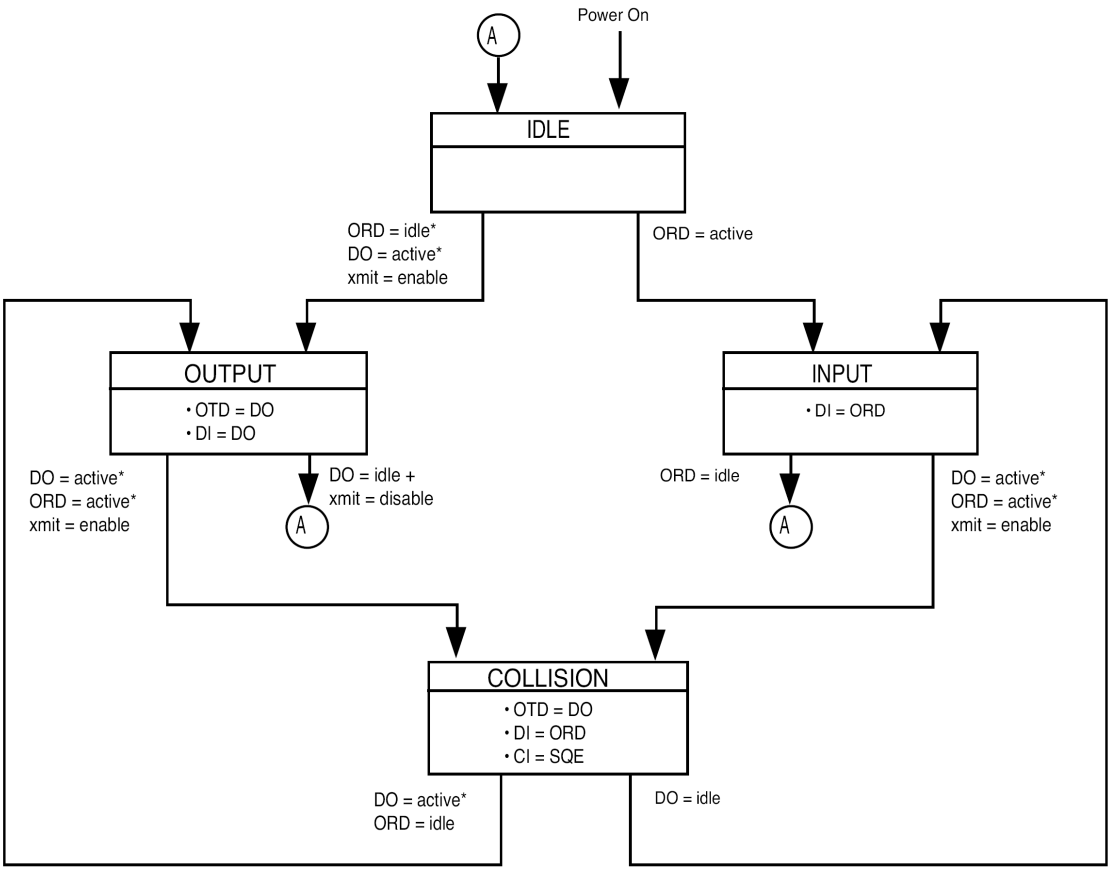
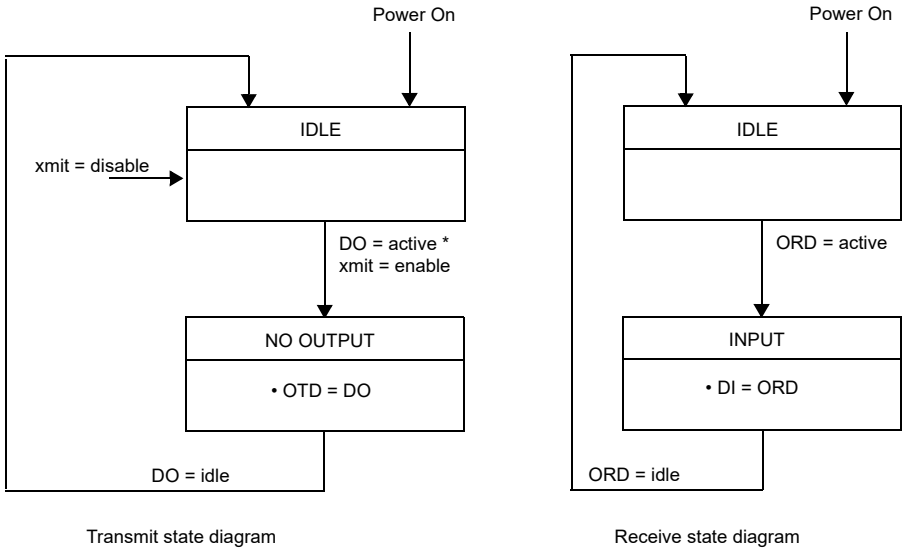


a) MAU Transmit, Receive, Loopback, and Collision Presence functions (half duplex mode)



Transmit state diagram

Receive state diagram

b) MAU Transmit and Receive functions (full duplex mode)

Figure 18–1—MAU state diagrams

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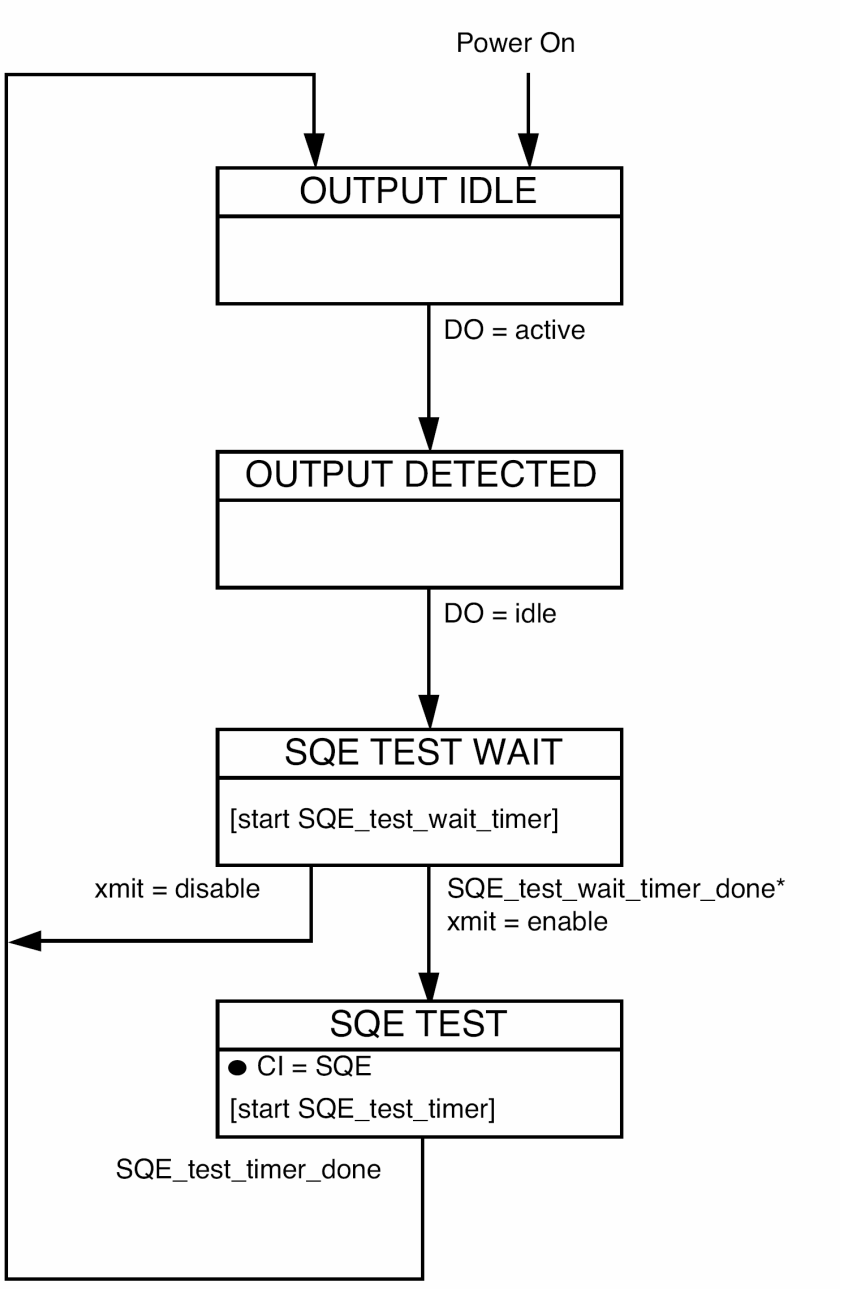

Figure 18–2—*signal_quality_error* Message Test function state diagram

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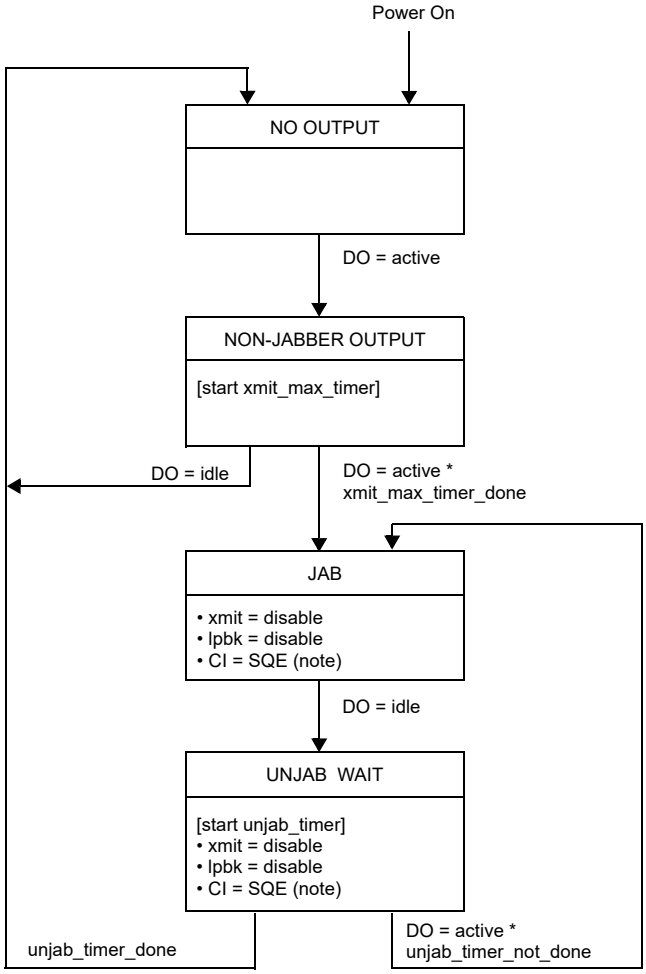

NOTE 1—Optional for MAUs connected to DTEs operating in full duplex mode.

NOTE 2—The implementation of the Collision Presence function is not required in a MAU connected to a full duplex mode DTE, and is not shown in Figure 18–1b).

NOTE 3—The implementation of the SQE Test function shown in Figure 18–2 is not required in a MAU connected to a full duplex mode DTE.

NOTE 4—The enabling of the variable *lpbk* in Figure 18–4 is applicable in half duplex mode only.

Figure 18–3—Jabber function state diagram

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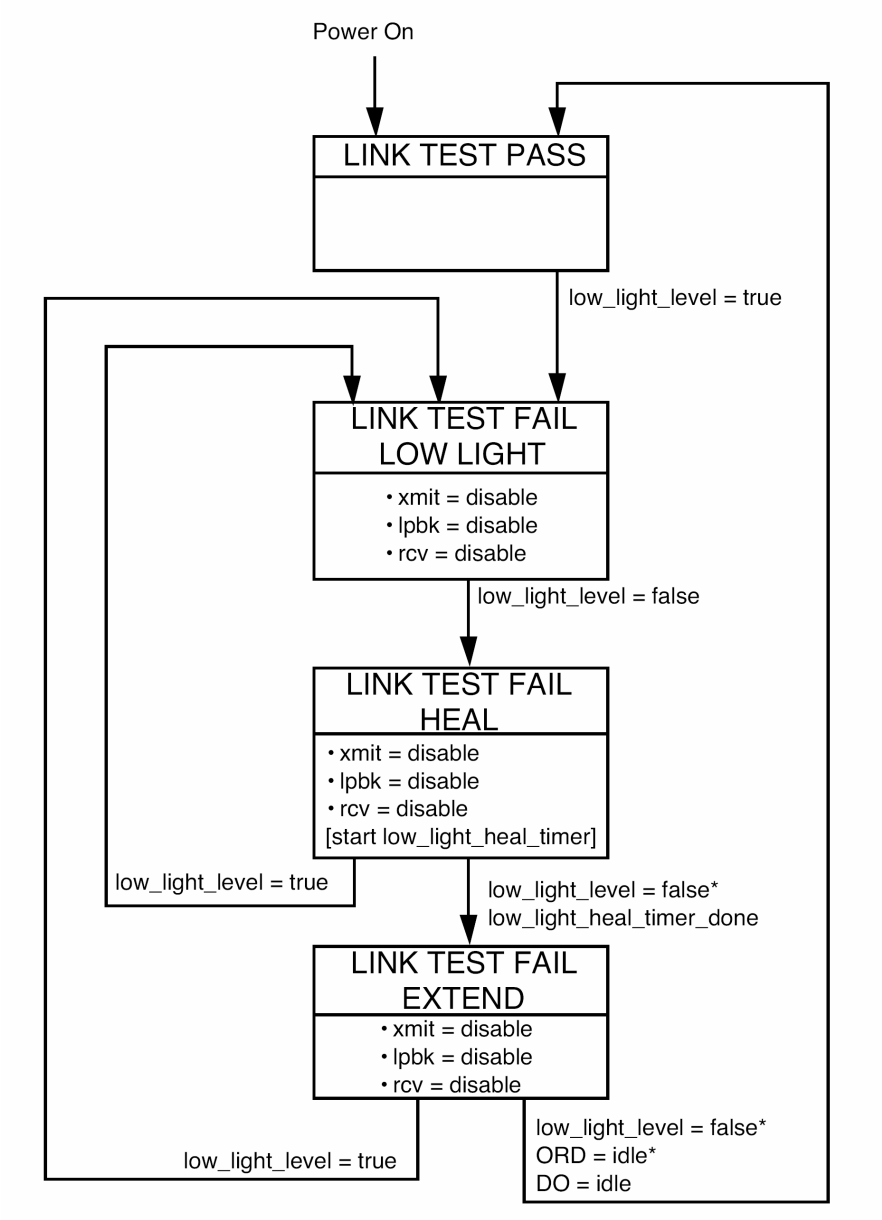

Figure 18–4—Link Integrity Test function state diagram

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18.4 Timing summary

Table 18–1 summarizes the timing requirements for the 10BASE-FL fiber link. This table is a summary; for complete descriptions of the timing requirements, refer to the referenced clauses. All times are in bit times.

Table 18–1—Maximum timing parameters

Symbol	Function	Bit loss	Invalid bits	Steady-state prop. delay	Startup delay		
					Max.	Var	Specified in
M1	*ORD_input* to *input* on DI	2.0	1.0	2.0	5.0	2.0	18.3.1.2
M2	*output* on DO to *OTD_output*	2.0	1.0	2.0	5.0	2.0	18.3.1.1
M3	*ORD_input* **output* to *signal_quality_error*				3.5		18.3.1.4
M4	*ORD_idle* + *output_idle* (end of collision) to *mau_available*				7.0		18.3.1.4
M5	*ORD_input* **output* to *input* on DI from circuit ORD				9.0		18.3.1.4
M6	*ORD_idle* **output* to *input* on DI from circuit DO				7.0		18.3.1.4
M7	*output_idle* on DO to *signal_quality_error*				$6 < x < 16$		18.3.1.5
M8	*signal_quality_error* duration for SQE test				$5 \leq x \geq 15$		18.3.1.5
M9	*output* on DO to *input* on DI	5.0	1.0	1.0	7.0		18.3.1.3
F1	Fiber Optic Cable Propagation (2000 m)	0	0	100	100		15.3.1.3
A1	AUI Cable Propagation (50 m)	0	0	2.57	2.57		7.4.3.7

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18.5 Protocol implementation conformance statement (PICS) proforma for Clause 18, Fiber optic medium attachment unit, type 10BASE-FL[52]

18.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 18, Fiber optic medium attachment unit, type 10BASE-FL, shall complete the following protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. The PICS can be used for a variety of purposes by various parties, including the following:

— As a checklist by the protocol implementer, to reduce the risk of failure to conform to the standard through oversight;
— As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
— As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICs);
— As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

18.5.2 Abbreviations and special symbols

18.5.2.1 Status symbols

The following symbols are used in the PICS proforma:

M	mandatory field/function
O	optional field/function
O.<n>	optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n>	optional field/function, but one and only one of the group of options labeled by the numeral <n> is required
X	prohibited field/function
<item>:	simple-predicate condition, dependent on the support marked for <item>

18.5.2.2 Abbreviations

N/A	Not applicable

In addition, the following predicate names are defined for use when different implementations from the set above have common parameters:

*HRP : HDX or RPT
*HDS : HDX or FDS
*HFC : HDX or FDS or RPT

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18.5.3 Instructions for completing the PICS proforma

18.5.3.1 General structure of the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

The main part of the PICS proforma is a fixed-format questionnaire divided into subclauses, each containing a group of items. Answers to the questionnaire items are to be provided in the right-most column, either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable), or by entering a value or a set or range of values. (Note that there are some items where two or more choices from a set of possible answers can apply; all relevant choices are to be marked.)

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to the material that specifies the item in the main body of the standard; the fourth column contains values and/or comments pertaining to the question to be answered. The remaining columns record the status of the item—whether the support is mandatory, optional, or conditional—and provide the space for the answers; see also 18.5.3.4.

The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the protocol implementation conformance statement for the implementation in question.

Note that where an implementation is capable of being configured in more than one way, according to the items listed under 18.5.5, Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation’s configuration capabilities, if that would make presentation of the information easier and clearer.

18.5.3.2 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features which, although optional, are nonetheless commonly present in implementations of the 10BASE-FL protocol.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

18.5.3.3 Exception information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

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An implementation for which an Exception item is required in this way does not conform to this standard.

Note that a possible reason for the situation described above is that a defect in the standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

18.5.3.4 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M, O, or X.

If the item referred to by the conditional symbol is marked as supported, the conditional item is applicable, and its status is given by "<s>"; the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

18.5.4 Identification

18.5.4.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

18.5.4.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2018, Clause 18, Fiber optic medium attachment unit, Type 10BASE-FL
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See 17.5.3.3; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2018.)	

Date of Statement	

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18.5.5 Major capabilities/options

Item	Feature	Subclause	Value/ Comment	Status	Support
*DTE	MAU supports DTE connections	15.1.1	N/A	O.1	Yes [ ] No [ ]
*RPT	MAU supports repeater connections	15.1.1	N/A	O.1	Yes [ ] No [ ]
*AUI	AUI connection physically exists and is accessible for test.	15.1.3.2	N/A	O	Yes [ ] No [ ]
*APW	AUI powers MAU	15.5.3	N/A	AUI: O.2	N/A [ ] Yes [ ] No [ ]
*SPW	AUI implemented but MAU powered separately	15.5.3	N/A	AUI: O.2	N/A [ ] Yes [ ] No [ ]
*FDX	MAU supports full duplex mode DTE connections	15.1.3.5	N/A	DTE: O.3	N/A [ ] Yes [ ] No [ ]
*HDX	MAU supports half duplex mode DTE connections	15.1.3.5	N/A	DTE: O.3	N/A [ ] Yes [ ] No [ ]
*FDS	MAU supports optional set of SQE related function for full duplex mode DTE connections	18.3.1	N/A	FDX: O	N/A [ ] Yes [ ] No [ ]

18.5.6 PICS proforma tables for the type 10BASE-FL MAU

18.5.6.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Compatibility considerations: 10BASE-FL systems compatible at 10BASE-FL MDI	15.1.3.2		M	Yes [ ]
CC2	10BASE-FL MAUs interoperable with FOIRL MAUs except for media connector	15.1.3.2		M	Yes [ ]
CC3	Mode of operation	15.1.3.5	normal mode only	M	Yes [ ]

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18.5.6.2 Optical transmit parameter

Item	Feature	Subclause	Value/Comment	Status	Support
OT1	Center wavelength	15.2.1.1	min. 800 nm; max. 910 nm	M	Yes [ ]
OT2	Spectral width (FWHM)	15.2.1.2	< 75 nm	M	Yes [ ]
OT3	Optical modulation extinction ratio	15.2.1.3	< –13 dB	M	Yes [ ]
OT4	Optical Idle signal amplitude	15.2.1.4	See 15.2.1.10	M	Yes [ ]
OT5	Optical transmit pulse logic polarity	15.2.1.5	High Optical Power = LO on AUI DO and MDI. Low Optical Power = HI on AUI DO and MDI.	M	Yes [ ]
	Optical transmit pulse rise and fall times	15.2.1.6	Measured from 10% to 90% level		
OT6	Max. (Data)		10.0 ns	M	Yes [ ]
OT7	Min. (Data)		0.0 ns	M	Yes [ ]
OT8	Max. Difference (Data)		3.0 ns	M	Yes [ ]
OT9	Max. (Idle)		25.0 ns	M	Yes [ ]
OT10	Min. (Idle)		0.0 ns	M	Yes [ ]
OT11	Max. Difference (Idle)		25.0 ns	M	Yes [ ]
OT12	Optical transmit pulse overshoot	15.2.1.7	< 25%	M	Yes [ ]
OT13	Optical transmit pulse undershoot	15.2.1.7	< 10%	M	Yes [ ]
	Optical transmit pulse edge jitter added	15.2.1.8	Measured as in 15.2.1.8		
OT14	DO circuit to MDI		± 2.0 ns	M	Yes [ ]
OT15	Total at MDI		±4.0 ns	M	Yes [ ]
	Optical transmit pulse duty cycle distortion	15.2.1.9	Measured at median power level		
OT16	Max. (Data)		± 2.5 ns	M	Yes [ ]
OT17	Max. (Idle)		± 50.0 ns	M	Yes [ ]
	Optical transmit average power range Min.	15.2.1.10			
OT18	Max.		–20 dBm	M	Yes [ ]
OT19			–12 dBm	M	Yes [ ]
OT20	Transmit signal templates	Figure 15–5	Optical signals within template	M	Yes [ ]

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18.5.6.3 Optical receive parameters

Item	Feature	Subclause	Value/Comment	Status	Support
OR1	BER between two AUIs attached to a single segment	15.2.2	< one part in 10^9	M	Yes [ ]
	Optical receive average power	15.2.2.1	When a single transmitter transmits on the medium		
OR2	Min.		–32.5 dBm	M	Yes [ ]
OR3	Max.		–12.0 dBm	M	Yes [ ]
	MAU optical receive Edge jitter (Data)	15.2.2.2	Measured as in 15.2.2.2		
OR4	Received at MDI		± 6.5 ns at median power	M	Yes [ ]
OR5	Added MDI to DI circuit		± 8.5 ns	M	Yes [ ]
OR6	Total at DI circuit (MAU end of AUI)		± 15.0 ns at zero crossing points	M	Yes [ ]
OR7	Optical receive pulse logic polarity	15.2.2.3	High Optical Power = LO on AUI DI and MDI. Low Optical Power = HI on AUI DI and MDI	M	Yes [ ]
	Optical receive pulse rise and fall times:	15.2.2.4	Measured from 10% to 90% level		
OR8	Max. (Data)		31.5 ns	M	Yes [ ]
OR9	Min. (Data)		0.0 ns	M	Yes [ ]
OR10	Max. Difference (Data)		3.0 ns	M	Yes [ ]
OR11	Max. (Idle)		41.0 ns	M	Yes [ ]
OR12	Min. (Idle)		0.0 ns	M	Yes [ ]
OR13	Max. Difference (Idle):		25.0 ns	M	Yes [ ]

18.5.6.4 Optical medium connector plug and socket

Item	Feature	Subclause	Value/Comment	Status	Support
CS1	Connector socket for MAU	15.3.2	BFOC/2.5—see IEC 60874-10:1992	M	Yes [ ]

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18.5.6.5 MAU functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Transmit	18.3.1.1		M	Yes [ ]
MF2	Receive	18.3.1.2		M	Yes [ ]
MF3	Loopback	18.3.1.3		HRP: M FDX: X	N/A [ ] M: Yes [ ] N/A [ ] X: Yes [ ]
MF4	Collision Presence	18.3.1.4		HFC: M	N/A [ ] M: Yes [ ]
MF5	Jabber	18.3.1.6		M	Yes [ ]
MF6	Link Integrity Test	18.3.1.7		M	Yes [ ]
MF7	SQE Test	18.3.1.5		HDS: M RPT: X	N/A [ ] M: Yes [ ] N/A [ ] X: Yes [ ]

18.5.6.6 PMA interface messages

Item	Feature	Subclause	Value/Comment	Status	Support
PIM1	Messages between the PLS in the DTE and the PMA in the MAU	18.2	As described in 7.2.1	M	Yes [ ]

18.5.6.7 PMA-to-MDI OTD messages

Item	Feature	Subclause	Value/Comment	Status	Support
OTD1	Signal sent on OTD corresponding to *OTD_output* message	18.2.1.1	CD1,CD0	M	Yes [ ]
OTD2	Signal sent on OTD corresponding to *OTD_idle* message	18.2.1.2	OPT_IDL	M	Yes [ ]

18.5.6.8 MDI ORD-to-PMA messages

Item	Feature	Subclause	Value/Comment	Status	Support
ORD1	Signal received on ORD corresponding to *ORD_input* message	18.2.2.1	CD1,CD0	M	Yes [ ]
ORD2	Signal received on ORD corresponding to *ORD_idle* message	18.2.2.2	OPT_IDL or signal other than valid Manchester Data	M	Yes [ ]

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18.5.6.9 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
XT1	Data Transmit path for *output* message	18.3.1.1	DO circuit to OTD circuit	M	Yes [ ]
XT2	Levels and timing of optical signal	18.3.1.1	As in 15.2.1	M	Yes [ ]
XT3	Startup bit loss (DO to OTD circuits)	18.3.1.1	2 bits max.	M	Yes [ ]
XT4	Transmit settling time	18.3.1.1	Second and following bits meet jitter, level, and waveform specifications of 15.2.1	M	Yes [ ]
XT5	Transmit steady-state delay	18.3.1.1	2 BT max.	M	Yes [ ]
XT6	Transmit delay variability	18.3.1.1	2 BT max.	M	Yes [ ]
XT7	Signal sent on OTD corresponding to OPT_IDL message	18.3.1.1	Start of idle followed by a periodic pulse waveform	M	Yes [ ]
XT8	Periodic pulse waveform	18.3.1.1	1 MHz +25%, –15%	M	Yes [ ]
XT9	OPT_IDL termination with respect to start of packet	18.3.1.1	Normal start-of-packet requirement apply	M	Yes [ ]

18.5.6.10 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RCV1	Optical to electrical	18.3.1.2	As specified in 15.2.2.3	M	Yes [ ]
RCV2	Receive path	18.3.1.2	ORD circuit to DI circuit	M	Yes [ ]
RCV3	Startup bit loss (ORD to DI circuits)	18.3.1.2	2 bits max.	M	Yes [ ]
RCV4	Receive settling time	18.3.1.2	Second and following bits meet jitter specifications of 15.2	M	Yes [ ]
RCV5	Receive steady-state delay	18.3.1.2	2 BT max.	M	Yes [ ]
RCV6	Receive delay variability	18.3.1.2	2 BT max.	M	Yes [ ]

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18.5.6.11 Loopback function

Item	Feature	Subclause	Value/Comment	Status	Support
LP1	Loopback function requirements when ORD = idle and DO = active	18.3.1.3	DO signals to DI circuit.	HRP: M	N/A [ ] M: Yes [ ]
LP2	Loopback bit loss (DO to DI circuits)	18.3.1.3	5 bits max	HRP: M	N/A [ ] M: Yes [ ]
LP3	Loopback settling time	18.3.1.3	Second and following bits meet jitter specifications.	HRP: M	N/A [ ] M: Yes [ ]
LP4	Loopback steady-state delay	18.3.1.3	1 BT max	HRP: M	N/A [ ] M: Yes [ ]

18.5.6.12 Collision Presence function

Item	Feature	Subclause	Value/Comment	Status	Support
CP1	Collision Presence function requirements	18.3.1.4	CS0 on CI circuit if DO=active, ORD=active and in Link Test Pass state.	HFC: M	N/A [ ] M: Yes [ ]
CP2	Collision indication delay	18.3.1.4	3.5 BT max.	HFC: M	N/A [ ] M: Yes [ ]
CP3	Collision indicate deassert delay	18.3.1.4	7 BT max.	HFC: M	N/A [ ] M: Yes [ ]
CP4	CI circuit with no collision, SQE Test, or jabber	18.3.1.4	IDL signal	HFC: M	N/A [ ] M: Yes [ ]
CP5	DI circuit source switch delay from CS0 assert	18.3.1.4	9 BT max.	HFC: M	N/A [ ] M: Yes [ ]
CP6	DI circuit source switch delay from CS0 deassert	18.3.1.4	7 BT max.	HFC: M	N/A [ ] M: Yes [ ]

18.5.6.13 *signal_quality_error* Message (SQE) Test function

Item	Feature	Subclause	Value/Comment	Status	Support
STF1	SQE Test induced OTD or DI circuit signals	18.3.1.5	No extraneous signals permitted	HDS: M	N/A [ ] M: Yes [ ]
STF2	SQE_test_wait timer range	18.3.1.5	0.6 to 1.6 µs	HDS: M	N/A [ ] M: Yes [ ]
STF3	SQE_test timer range	18.3.1.5	5 to 15 BT	HDS: M	N/A [ ] M: Yes [ ]
STF4	CI circuit during SQE Test	18.3.1.5	CS0 signal	HDS: M	N/A [ ] M: Yes [ ]
STF5	SQE Test in Link Fail states	18.3.1.5	CS0 is not sent	HDS: M	N/A [ ] M: Yes [ ]

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18.5.6.14 Jabber function

Item	Feature	Subclause	Value/Comment	Status	Support
JAB1	Jabber function implementation	18.3.1.6	Self-interrupt of transmit and loopback.	M	Yes [ ]
JAB2	Xmit_max. timer range	18.3.1.6	20 ms min., 150 ms max.	M	Yes [ ]
JAB3	CI circuit during jabber	18.3.1.6	CS0 signal	HFC: M	N/A [ ] M: Yes [ ]
JAB4	Unjab timer range	18.3.1.6	0.5 s ± 0.25 s	M	Yes [ ]
JAB5	MAU Jabber Lockup Protection	18.3.1.6	Jabber not activated by the longest permitted output specified in 9.6.5	M	Yes [ ]

18.5.6.15 Link Integrity Test function

Item	Feature	Subclause	Value/Comment	Status	Support
LI1	Low light detected	18.3.1.7	ORD optical power does not support a BER of 10^{-10} for a duration of 2000 BT, or ORD optical power is < –30 dBm for 2000 BT and does not support a BER of 10^{-10} for a duration of 500 BT	M	Yes [ ]
LI2	Low light not detected	18.3.1.7	ORD optical power exceeds –32.5 dBm or low light condition remains < 30 BT	M	Yes [ ]
	Signals during detected failure	18.3.1.7			
LI3	OTD circuit		OPT_IDL	M	Yes [ ]
LI4	DI circuit		IDL	M	Yes [ ]
LI5	CI circuit		IDL (except when jabber condition is also present)	M	Yes [ ]

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LI6	Link Test Fail state exit conditions	18.3.1.7	ORD optical power exceeds –32.5 dBm for 0.5 s ± 0.25 s	M	Yes [ ]
	Link fail effect on MAU functions	18.3.1.7			
LI7	Transmit		Disable	M	Yes [ ]
LI8	Receive		Disable	M	Yes [ ]
LI9	Loopback		Disable	M	Yes [ ]
LI10	Collision Presence		Disable	M	Yes [ ]
LI11	SQE Test		Disable	M	Yes [ ]
LI12	Link Test Fail Extend state exit condition	18.3.1.7	Deferred until ORD = idle and DO = idle	M	Yes [ ]
LI13	Power-on state	18.3.1.7	Link Test Fail Low Light	O	Yes [ ] No [ ]
LI14	Link status indicator	18.3.1.7	Color=green on=Link Test Pass	O	Yes [ ] No [ ]

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18.5.6.16 MAU state diagram requirements

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Full duplex mode MAU Transmit and Receive functions state diagram	18.3.2	Meets requirements of Figure 18–1b)	FDX: M	N/A [ ] M: Yes [ ]
SD2	Half duplex Transmit, Receive, Loopback, and Collision Presence functions state diagrams	18.3.2	Meets requirements of Figure 18–1a)	HFC:M	N/A [ ] M: Yes [ ]
SD3	*signal_quality_error* Message Test function state diagram	18.3.2	Meets requirements of Figure 18–2	HDS: M	N/A [ ] M: Yes [ ]
SD4	Jabber function state diagram	18.3.2	Meets requirements of Figure 18–3	M	Yes [ ]
SD5	Link Integrity Test function state diagram	18.3.2	Meets requirements of Figure 18–4	M	Yes [ ]

18.5.6.17 MAU-to-AUI signal characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
ASC1	Signaling rate (stated on label)	7.3.2	10 Mb/s	AUI: M	N/A [ ] M: Yes [ ]
ASC2	CS0 signal frequency (on CI)	7.3.1.2	10 MHz ± 15%	AUI: M	N/A [ ] M: Yes [ ]
ASC3	CS0 signal duty cycle	7.3.1.2	60:40 worst case	AUI: M	N/A [ ] M: Yes [ ]

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18.5.6.18 MAU-to-AUI DI and CI driver characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
ADC1 ADC2	Differential output voltage Idle state Start of idle	7.4.1.1	 ≤ 40 mV after 80 BT Figure 7–12	AUI: M	N/A [ ] M: Yes [ ]
ADC3	Current into test load while idle	7.4.1.1	4 mA max. after 80 BT	AUI: M	N/A [ ] M: Yes [ ]
ADC4	Requirements after idle	7.4.1.2	1st bit to Figure 7–11	AUI: M	N/A [ ] M: Yes [ ]
ADC5	Common-mode output voltage, ac	7.4.1.3	≤ 2.5 V peak for 30 Hz to 40 kHz, ≤ 160 mV peak for 40 kHz to 10 MHz, Figure 7–13	AUI: M	N/A [ ] M: Yes [ ]
ADC6	Differential output voltage, open circuit	7.4.1.4	13 V peak max.	AUI: M	N/A [ ] M: Yes [ ]
ADC7	Common-mode output voltage, dc	7.4.1.5	≤ 5.5 V, Figure 7–13	AUI: M	N/A [ ] M: Yes [ ]
ADC8	Fault tolerance	7.4.1.6	Figure 7–14	AUI: M	N/A [ ] M: Yes [ ]
ADC9	Fault current	7.4.1.6	≤ 150 mA, any state, Figure 7–14	AUI: M	N/A [ ] M: Yes [ ]

18.5.6.19 AUI-to-MAU DO receiver characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
DO1	Unsquelched threshold	7.4.2.1	160 mV max. differential	AUI: M	N/A [ ] M: Yes [ ]
DO2	Squelch	15.5.1	Reject signals < ±160 mV differential	AUI: M	N/A [ ] M: Yes [ ]
DO3	High to idle transition	7.4.1.1	Does not cause output	AUI: M	N/A [ ] M: Yes [ ]
DO4	Differential input impedance	7.4.2.2	Real part: 77.83 Ω ± 6%, 0 ≤ phase angle ≤ real part ∗ 0.0338	AUI: M	N/A [ ] M: Yes [ ]
DO5	Common-mode range, ac	7.4.2.3	3 V min. for 30 Hz to 40 kHz, 200 mV min. for 40 kHz to 10 MHz	AUI: M	N/A [ ] M: Yes [ ]
DO6	Total common-mode range	7.4.2.4	Magnitude of 0 to 5.5 V ac+dc	AUI: M	N/A [ ] M: Yes [ ]
DO7	Common-mode current limit	7.4.2.4	≤ 1 mA	AUI: M	N/A [ ] M: Yes [ ]
DO8	IDL detection	7.3.1.1	≤ 1.6 BT	AUI: M	N/A [ ] M: Yes [ ]
DO9	Requirements after idle	7.4.2.5	Receiver in specification after startup delay	AUI: M	N/A [ ] M: Yes [ ]
DO10	Receiver fault tolerance	7.4.2.6	Figure 7–16	AUI: M	N/A [ ] M: Yes [ ]
DO11	Input fault current	7.4.2.6	3 mA max. for Figure 7–16	AUI: M	N/A [ ] M: Yes [ ]

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18.5.6.20 AUI circuit termination

Item	Feature	Subclause	Value/Comment	Status	Support
ACT1	Common-mode termination	7.5.2.6	If used, is to VC	AUI: M	N/A [ ] M: Yes [ ]
ACT2	Pins 1, 4, 8, 11, 14 impedance to VC circuit	7.5.2.8	≤ 5 Ω at 5 MHz	AUI: M	N/A [ ] M: Yes [ ]
ACT3	Pins 1, 4, 8, 11, 14 coupling to VC circuit	7.5.2.8	Capacitive	AUI: M	N/A [ ] M: Yes [ ]

18.5.6.21 MAU-to-AUI mechanical connections

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	D-type connector dimensions	7.6.2	IEC 60807-2:1992 15-pole male	AUI: M	N/A [ ] M: Yes [ ]
AM2	Shell plating material	7.6.2	Conductive	AUI: M	N/A [ ] M: Yes [ ]
AM3	Shell multiple contact points	7.6.2	Number not defined (recommended)	AUI: M	N/A [ ] M: Yes [ ]
AM4	Shell life expectancy	7.6.2	≤ 5 mΩ after 500 matings	AUI: M	N/A [ ] M: Yes [ ]
AM5	Locking posts and mounting	7.6.1	Figures 7–18 and 7–20	AUI: M	N/A [ ] M: Yes [ ]
	Pin connections	7.6.3	Circuit		
AM6	3		Data Out A	AUI: M	N/A [ ] M: Yes [ ]
AM7	10		Data Out B	AUI: M	N/A [ ] M: Yes [ ]
AM8	11		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM9	5		Data In A	AUI: M	N/A [ ] M: Yes [ ]
AM10	12		Data In B	AUI: M	N/A [ ] M: Yes [ ]
AM11	4		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM12	7		No connection	AUI: M	N/A [ ] M: Yes [ ]
AM13	15		No connection	AUI: M	N/A [ ] M: Yes [ ]
AM14	8		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM15	2		Control In A	AUI: M	N/A [ ] M: Yes [ ]
AM16	9		Control In B	AUI: M	N/A [ ] M: Yes [ ]
AM17	1		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM18	6		Voltage common	AUI: M	N/A [ ] M: Yes [ ]
AM19	13		Voltage plus	AUI: M	N/A [ ] M: Yes [ ]
AM20	1		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM21	Shell		Isolated from all pins	AUI: M	N/A [ ] M: Yes [ ]

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18.5.6.22 MAU reliability

Item	Feature	Subclause	Value/Comment	Status	Support
MR1	Mean Time Before Failure	15.4	$> 10^7$ hours without causing communications failure among other stations	M	Yes [ ]

18.5.6.23 Power consumption

Item	Feature	Subclause	Value/Comment	Status	Support
PC1	Power surge limitation	15.5.3	$< 2 \times 10^{-3}$ A–s	APW: M	N/A [ ] M: Yes [ ]
PC2	Power surge duration	15.5.3	100 ms max.	APW: M	N/A [ ] M: Yes [ ]
PC3	Steady-state current drawn power-up capability:	15.5.3	≤ 0.5 A	APW: M	N/A [ ] M: Yes [ ]
PC4	Current-limited sources	15.5.3	0.5 A limited	APW: M	N/A [ ] M: Yes [ ]
PC5	Voltage-limited sources	7.5.2.5	11.28 to 15.75 V via any AUI cable	APW: M	N/A [ ] M: Yes [ ]
PC6	Labeling	15.5.3	As in 15.5.3	APW: M	N/A [ ] M: Yes [ ]
PC7	Power cycle behavior	15.5.3	No extraneous signals on MDI, DI, or CI	AUI: M	N/A [ ] M: Yes [ ]
PC8	Low VP behavior	7.5.2.5	No disruption of media	APW: M	N/A [ ] M: Yes [ ]
PC9	Power sourced on pin 13 of AUI	15.5.3	None if separate power source is implemented	SPW: X	N/A [ ] X: Yes [ ]
PC10	Optional power source isolation	15.5.3	If implemented, shall withstand one of 15.3.4 tests	SPW: M	N/A [ ] M: Yes [ ]

18.5.6.24 PLS–PMA requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	Messages between PLS in DTE or Repeater and PMA	15.5.4	As in 7.2.1	M	Yes [ ]

18.5.6.25 *signal_quality_error* message (SQE)

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Item	Feature	Subclause	Value/Comment	Status	Support
SQE1	Local MAU transmitting and no collision or fault detected	15.5.4.2.1	*MAU_available* sent on CI	M	Yes [ ]
SQE2	Whenever a collision exists as described in 18.3.1.4	15.5.4.2.1	SQE sent	HFC: M	N/A [ ] M: Yes [ ]
SQE3	SQE Test as described in 18.3.1.5	15.5.4.2.1	SQE sent	HDS:M RPT: X	N/A [ ] M: Yes [ ] N/A [ ] X: Yes [ ]
SQE4	Jabber Condition exists as described in 18.3.1.6	15.5.4.2.1	SQE sent	HFC:M	N/A [ ] M: Yes [ ]
SQE5	Message sent in the absence of SQE	15.5.4.2.1	*MAU_available* message	M	Yes [ ]

18.5.6.26 Environmental requirements

Item	Feature	Subclause	Value/Comment	Status	Support
E1	Ambient Plane Wave field in which MAU meets specification	15.6.2	2 V/m from 10 kHz to 30 MHz. 5 V/m from 30 MHz to 1 GHz.	M	Yes [ ]
E2	Electromagnetic Emissions and Susceptibility	15.6.2	Comply with local and/or national requirements. If none exist, comply with CISPR 22: 1993.	M	Yes [ ]

18.5.6.27 MAU labeling

Item	Feature	Subclause	Value/Comment	Status	Support
LBL1	MAU type	15.7	10BASE-FL	O	Yes [ ] No [ ]
LBL2	Data rate	15.7	10 Mb/s	O	Yes [ ] No [ ]
LBL3	Power level	15.7	Maximum current drain	O	Yes [ ] No [ ]
LBL4	Safety warnings	15.7	Any applicable	O	Yes [ ] No [ ]
LBL5	Port labeling	15.7	Input and output	O	Yes [ ] No [ ]
LBL6	Full duplex mode	15.7	Full duplex capable	FDX: O	N/A [ ] Yes [ ] No [ ]

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19. Layer Management for 10 Mb/s baseband repeaters

Clause 19 is deprecated by Clause 30.

19.1 Introduction

The Repeater Management specification has been developed in accordance with the OSI management architecture as specified in ISO/IEC 7498-4: 1989 and the specific requirements of IEEE Std 802.1F-1993. Implementation of this clause is not a requirement for conformance to Clause 9.

19.1.1 Scope

This clause defines a set of mechanisms that enable management of Ethernet 10 Mb/s baseband repeater units. The managed objects within this International Standard are defined in terms of their behaviour, attributes, actions, notifications, and packages in accordance with IEEE 802.1 and ISO/IEC International Standards for network management. Managed objects are grouped into mandatory and optional packages.

This International Standard is defined to be independent of any particular management application or management protocol. The means by which the managed objects defined in this International Standard are accessed is beyond the scope of this International Standard.

19.1.2 Relationship to objects in IEEE Std 802.1F-1993

The following managed object classes, if supported by an implementation, shall be as specified in IEEE Std 802.1F-1993: oResourceTypeID, oEWMAMetricMonitor:

a) **oResourceTypeID.** This object class is mandatory and shall be implemented as defined in IEEE Std 802.1F-1993. This object is bound to repeater as defined by the NAMEBINDING in 19.2.4 and H.2.2.1.
b) **oEWMAMetricMonitor.** This object class is optional. When implemented, it shall be implemented as defined in IEEE Std 802.1F-1993, subject to the specific requirements described below. This object is bound to system as defined by the NAMEBINDING in H.2.2.1.

Implementations of Repeater Management that support the oEWMAMetricMonitor managed object class are required to support values of aGranularityPeriod as small as one second. Implementations are required to support at least one sequence of low and high thresholds. The granularity period may be set to equal to the moving time period as a minimal conformant implementation.

19.1.3 Definitions

See 1.4.

19.1.4 Symbols and abbreviations

See 1.5.

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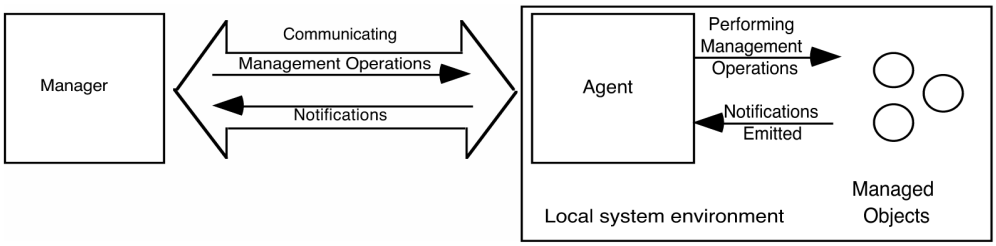
19.1.5 Management model

This International Standard describes management of repeaters in terms of a general model of management of resources within the open systems environment. The model is described in ISO/IEC 10040: 1992, a brief summary of the model is included here.

Management is viewed as a distributed application modeled as a set of interacting management processes. These processes are executed by systems within the open environment. A managing system executes a managing process that invokes management operations. A managed system executes a process that is receptive to these management operations and provides an interface to the resources to be managed. A managed object is the abstraction of a resource that represents its properties as seen by (and for the purpose of) management. Managed objects respond to a defined set of management operations. Managed objects are also capable of emitting a defined set of notifications. This interaction of processes is shown in Figure 19–1.



NOTE—Figure 1 of ISO/IEC 10040 has been reproduced with the permission of ISO. Copies of the complete standard may be obtained from the International Organization for Standardization, Case Postale 56, 1 rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse.

Figure 19–1—Interaction between manager, agent, and objects

A managed object is a management view of a resource. The resource may be a logical construct, function, physical device, or anything subject to management. Managed objects are defined in terms of four types of elements:

a) *Attributes.* Data-like properties (as seen by management) of a managed object.
b) *Actions.* Operations that a managing process may perform on an object or its attributes.
c) *Notifications.* Unsolicited reports of events that may be generated by an object.
d) *Behaviour.* The way in which managed objects, attributes, and actions interact with the actual resources they model and with each other.

The above items are defined in 19.2.3 through 19.2.6 of this International Standard in terms of the template requirements of ISO/IEC 10165-4: 1992.

Some of the functions and resources within a repeater are appropriate targets for management. They have been identified by specifying managed objects that provide a management view of the functions or resources. Within this general model, a repeater is viewed as a managed device. It performs functions as defined by the applicable standard for such a device. Managed objects providing a view of those functions and resources appropriate to the management of a repeater are specified. The purpose of this International Standard is to define the object classes associated with repeaters in terms of their attributes, operations, notifications, and behaviour.

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19.2 Managed objects

19.2.1 Introduction

This document defines the management of IEEE 802.3 repeaters by defining associated managed objects. This management encompasses two distinct aspects of repeater management.

The first aspect provides the means to monitor and control the functions of a repeater. These functions include, but are not limited to, identifying a repeater, testing and initializing a repeater, and enabling/disabling a port.

The second aspect provides the means to monitor traffic from attached segments, and to measure traffic sourced by DTEs connected to these segments. This is done by gathering statistics on packets that enter a repeater and maintaining those statistics on a per-port basis.

19.2.2 Overview of managed objects

Managed objects provide a means to

a) Identify a resource
b) Control a resource
c) Monitor a resource

19.2.2.1 Text description of managed objects

In case of conflict, the formal behaviour definitions in 19.2.3 through 19.2.6 take precedence over the text descriptions in this subclause.

a) **repeater.** The topmost managed object class of that portion of the containment tree shown in Figure 19–3. All other managed objects and their attributes defined in this clause are contained within the repeater managed object.
b) **repeaterMonitor.** A managed object class called out by IEEE Std 802.1F-1993.
c) **resourceTypeID.** A managed object class called out by IEEE Std 802.1F-1993.
d) **group.** The group managed object class is a view of a collection of ports.
e) **port.** The port managed object class provides a view of the functional link between the data transfer service and a single PMA. The attributes associated with port deal with the monitoring of traffic being handled by the repeater from the port and control of the operation of the port. The port enable/disable function as reported by portAdminState is preserved across events involving loss of power.

   NOTE—Attachment to nonstandard PMAs is outside the scope of this International Standard.

19.2.2.2 Port functions to support management

The port object class contains seven functions that are used to collect statistics on the activity received by the port. The relationship of the functions to the port and to the port attributes is shown in Figure 19–2.

a) **Activity Timing function.** Measures the duration of the assertion of the CarrierEvent signal. This duration value has to be adjusted by removing the value of Carrier Recovery Time (see 9.5.6.5) to obtain the true duration of activity on the network. The output of the Activity Timing function is the ActivityDuration value, which represents the duration of the CarrierEvent signal as expressed in units of bit times.
b) **Carrier Event function.** Asserts the CarrierEvent signal when the repeater exits the IDLE state (see Figure 9–2) and the port has been determined to be port N. It de-asserts the CarrierEvent signal when, for a duration of at least Carrier Recovery Time (see 9.5.6.5), both the DataIn(N) variable has

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the value II and the CollIn(N) variable has the value -SQE. The value N is the port assigned at the time of transition from the IDLE state.

c) **Collision Event function.** Asserts the CollisionEvent signal when the CollIn(X) variable has the value SQE. The CollisionEvent signal remains asserted until the assertion of any CarrierEvent signal due to the reception of the following event.

d) **Cyclic Redundancy Check function.** Verifies that the sequence of octets output by the framing function contains a valid frame check sequence field. The frame check sequence field is the last four octets received from the output of the framing function. The algorithm for generating an FCS from the octet stream is specified in 3.2.9. If the FCS generated according to this algorithm is not the same as the last four octets received from the framing function, then the FCSError signal is asserted. The FCSError signal is cleared upon the assertion of the CarrierEvent signal due to the reception of the following event.

e) **Framing function.** Recognizes the boundaries of an incoming frame by monitoring the CarrierEvent signal and the decoded data stream. Data bits are accepted while the CarrierEvent signal is asserted. The framing function strips preamble and start of frame delimiter from the received data stream. The remaining bits are aligned along octet boundaries. If there is not an integral number of octets, then FramingError shall be asserted. The FramingError signal is cleared upon the assertion of the CarrierEvent signal due to the reception of the following event.

f) **Octet Counting function.** Counts the number of complete octets received from the output of the framing function. The output of the octet counting function is the OctetCount value. The OctetCount value is reset to zero upon the assertion of the CarrierEvent signal due to the reception of the following event.

g) **Source Address function.** Extracts octets from the stream output by the framing function. The seventh through twelfth octets shall be extracted from the octet stream and output as the SourceAddress variable. The SourceAddress variable is set to an invalid state upon the assertion of the CarrierEvent signal due to the reception of the following event.

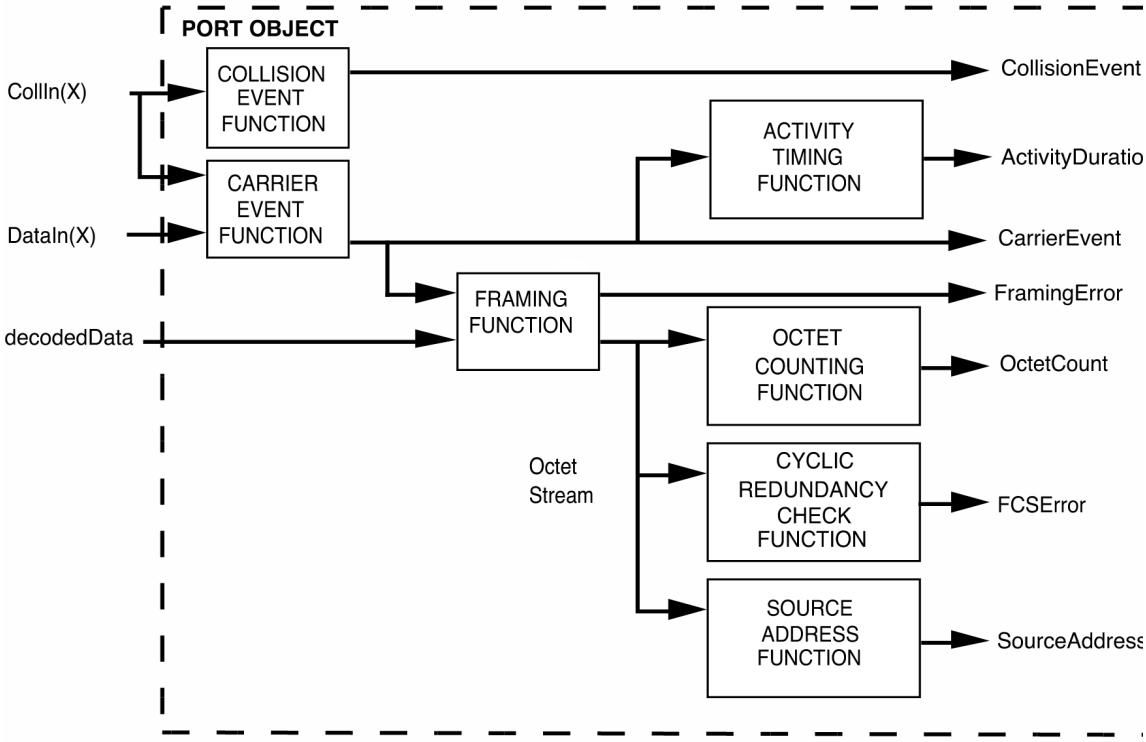

Figure 19–2—Functions relationship

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19.2.2.3 Containment

A containment relationship is a structuring relationship for managed objects in which the existence of a managed object is dependent on the existence of a containing managed object. The contained managed object is said to be the subordinate managed object and the containing managed object the superior managed object. The containment relationship is used for naming managed objects. The local containment relationships among object classes are depicted in Figure 19–3. This figure also shows the names, naming attributes, and data attributes of the object classes as well as whether a particular containment relationship is one-to-one or one-to-many. For further requirements on this topic, see IEEE Std 802.1F-1993.

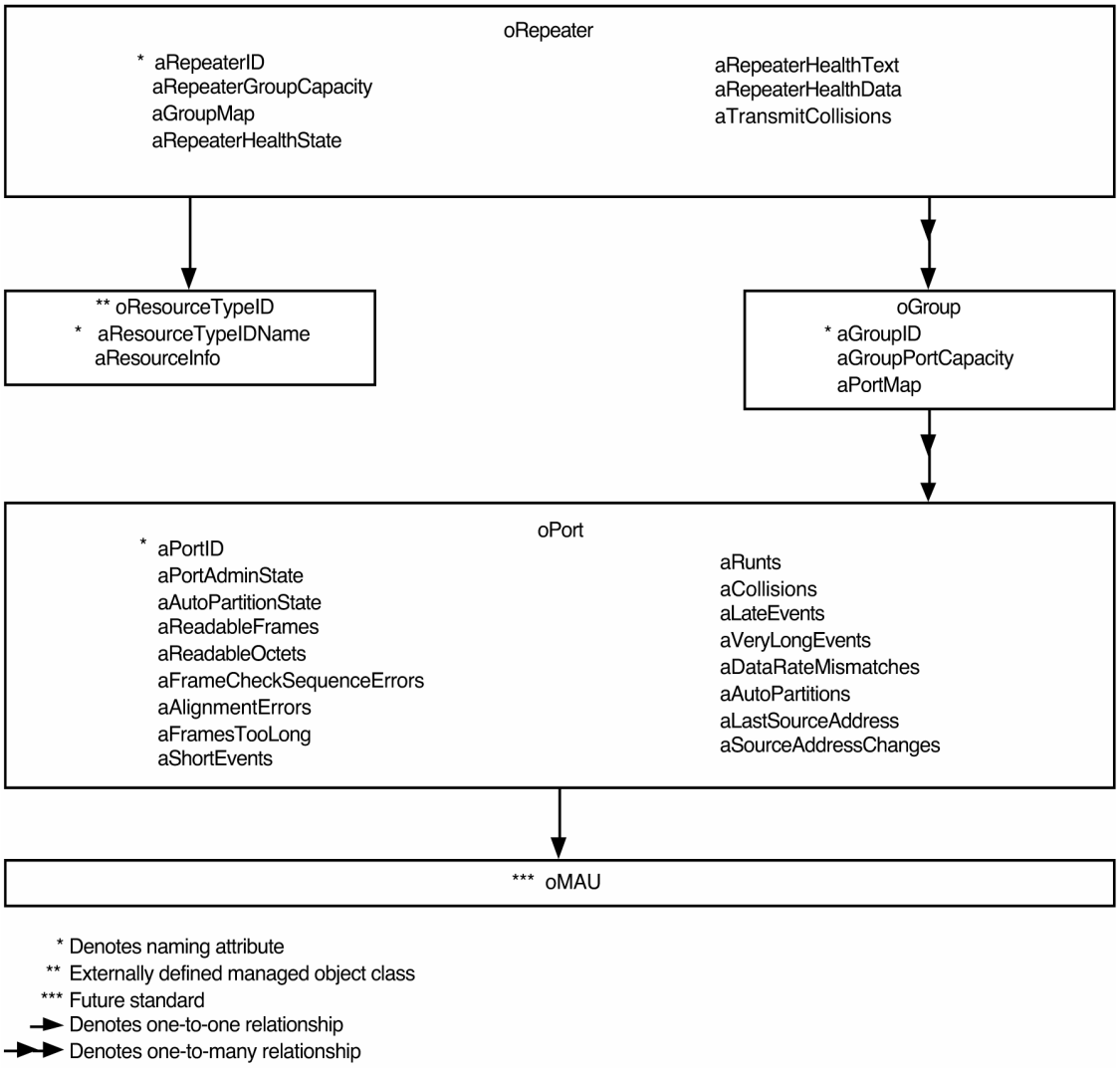

Figure 19–3—Entity relationship diagram

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19.2.2.4 Naming

The name of an individual managed object is hierarchically defined within a managed system. For example, a port might be identified as “repeater 3, group 01, port 13,” that is, port 13 of group 01 of a repeater with repeaterID 3 within the managed system. This is represented in the relationship of the naming attributes in Figure 19–3.

19.2.2.5 Packages and capabilities

This International Standard makes use of the concept of “packages” as defined in ISO/IEC 10165-4:1992 as a means of grouping behaviour, attributes, actions, and notifications within a managed object class definition. Packages may either be mandatory or conditional, that is to say, present if a given condition is true. Within this International Standard, “capabilities” are defined, each of which corresponds to a set of packages, which are components of a number of managed object class definitions and which share the same condition for presence. The “Basic Control Capability” consists of the set of mandatory packages. All other capabilities are optional and comprise sets of conditional packages. For a managed repeater to be conformant to this International Standard, it shall fully implement the Basic Control Capability. For the repeater to be conformant to an optional capability, it shall implement that entire capability. The capabilities and their associated packages are summarized in Table 19–1 (see facing page).

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Table 19–1—Packages and capabilities

		Basic Control Capability (Mandatory)	Performance Monitor Capability (Optional)	Address Tracking Capability (Optional)
oRepeater managed object class				
aRepeaterID	ATTRIBUTE GET	X		
aRepeaterGroupCapacity	ATTRIBUTE GET	X		
aGroupMap	ATTRIBUTE GET	X		
aRepeaterHealthState	ATTRIBUTE GET	X		
aRepeaterHealthText	ATTRIBUTE GET	X		
aRepeaterHealthData	ATTRIBUTE GET	X		
aTransmitCollisions	ATTRIBUTE GET		X	
acResetRepeater	ACTION	X		
acExecuteNonDisruptiveSelfTest	ACTION	X		
nRepeaterHealth	NOTIFICATION	X		
nRepeaterReset	NOTIFICATION	X		
nGroupMapChange	NOTIFICATION	X		
oResourceTypeID managed object class				
aResourceTypeIDName	ATTRIBUTE GET	X		
aResourceInfo	ATTRIBUTE GET	X		
oGroup managed object class				
aGroupID	ATTRIBUTE GET	X		
aGroupPortCapacity	ATTRIBUTE GET	X		
aPortMap	ATTRIBUTE GET	X		
nPortMapChange	NOTIFICATION	X		
oPort managed object class				
aPortID	ATTRIBUTE GET	X		
aPortAdminState	ATTRIBUTE GET	X		
aAutoPartitionState	ATTRIBUTE GET	X		
aReadableFrames	ATTRIBUTE GET		X	
aReadableOctets	ATTRIBUTE GET		X	
aFrameCheckSequenceErrors	ATTRIBUTE GET		X	
aAlignmentErrors	ATTRIBUTE GET		X	
aFramesTooLong	ATTRIBUTE GET		X	
aShortEvents	ATTRIBUTE GET		X	
aRunts	ATTRIBUTE GET		X	
aCollisions	ATTRIBUTE GET		X	
aLateEvents	ATTRIBUTE GET		X	
aVeryLongEvents	ATTRIBUTE GET		X	
aDataRateMismatches	ATTRIBUTE GET		X	
aAutoPartitions	ATTRIBUTE GET		X	
aLastSourceAddress	ATTRIBUTE GET			X
aSourceAddressChanges	ATTRIBUTE GET			X
acPortAdminControl	ACTION	X		
Common Attributes Template				
aRMCounter	ATTRIBUTE GET		X	X

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19.2.3 Repeater managed object class

This subclause formally defines the behaviours for Repeater managed object classes, attributes, actions, and notifications.

19.2.3.1 Repeater attributes

19.2.3.1.1 aRepeaterID

ATTRIBUTE
APPROPRIATE SYNTAX
INTEGER
BEHAVIOUR DEFINED AS:
The value of aRepeaterID is assigned so as to uniquely identify a repeater among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2: 1992).

19.2.3.1.2 aRepeaterGroupCapacity

ATTRIBUTE
APPROPRIATE SYNTAX
INTEGER
BEHAVIOUR DEFINED AS:
The aRepeaterGroupCapacity is the number of groups that can be contained within the repeater. Within each managed repeater, the groups are uniquely numbered in the range from 1 to aRepeaterGroupCapacity. Some groups may not be present in a given repeater instance, in which case the actual number of groups present is less than aRepeaterGroupCapacity. The number of groups present is never greater than aRepeaterGroupCapacity.

19.2.3.1.3 aGroupMap

ATTRIBUTE
APPROPRIATE SYNTAX
BITSTRING
BEHAVIOUR DEFINED AS:
A string of bits which reflects the current configuration of units which are viewed by group managed objects. The length of the bitstring is "aRepeaterGroupCapacity" bits. The first bit relates to group 1. A "1" in the bitstring indicates presence of the group, "0" represents absence of the group.

19.2.3.1.4 aRepeaterHealthState

ATTRIBUTE
APPROPRIATE SYNTAX:
An ENUMERATED VALUE LIST that has the following entries:

other	--undefined or unknown
ok	--no known failures
repeaterFailure	--known to have a repeater related failure
groupFailure	--known to have a group related failure
portFailure	--known to have a port related failure
generalFailure	--has a failure condition, unspecified type

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BEHAVIOUR DEFINED AS:

The aRepeaterHealthState attribute indicates the operational state of the repeater. The aRepeaterHealthData and aRepeaterHealthText attributes may be consulted for more specific information about the state of the Repeater's health. In case of multiple kinds of failures (e.g., repeater failure and port failure), the value of this attribute shall reflect the highest priority in the following order:

repeater failure
group failure
port failure
general failure.

19.2.3.1.5 aRepeaterHealthText

ATTRIBUTE
APPROPRIATE SYNTAX:

A PrintableString, 255 characters max.

BEHAVIOUR DEFINED AS:

The aRepeaterHealthText attribute is a text string that provides information relevant to the operational state of the repeater. Repeater vendors may use this mechanism to provide detailed failure information or instructions for problem resolution.
The contents are vendor specific.

19.2.3.1.6 aRepeaterHealthData

ATTRIBUTE
APPROPRIATE SYNTAX:

OCTET STRING, 0–255.

BEHAVIOUR DEFINED AS:

The aRepeaterHealthData attribute is a block of data octets that provides information relevant to the operational state of the repeater. The encoding of this data block is vendor dependent. Repeater vendors may use this mechanism to provide detailed failure information or instructions for problem resolution.

19.2.3.1.7 aTransmitCollisions

ATTRIBUTE
APPROPRIATE SYNTAX:

Generalized non-resettable counter. This counter has a maximum increment rate of 75 000 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented every time the repeater state machine enters the TRANSMIT COLLISION state from any state other than ONE PORT LEFT (see Figure 9–2).

19.2.3.2 Repeater actions

19.2.3.2.1 acResetRepeater

ACTION
APPROPRIATE SYNTAX

None required

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BEHAVIOUR DEFINED AS:

This is the transition to the START state of Figure 9–2 in Clause 9. The repeater performs a disruptive self-test that has the following characteristics:

a) The components are not specified.
b) The test resets the repeater but without affecting management information about the repeater.
c) The test does not inject packets onto any segment.
d) Packets received during the test may or may not be transferred.
e) The test does not interfere with management functions.

This causes an nRepeaterReset notification to be sent.

19.2.3.2.2 acExecuteNonDisruptiveSelfTest

ACTION

APPROPRIATE SYNTAX

None required

BEHAVIOUR DEFINED AS:

The repeater performs a vendor-specific, non-disruptive self-test that has the following characteristics:

a) The components are not specified.
b) The test does not change the state of the repeater or management information about the repeater.
c) The test does not inject packets onto any segment.
d) The test does not prevent the transfer of any packets.
e) Completion of the test causes an nRepeaterHealth to be sent.

19.2.3.3 Repeater notifications

19.2.3.3.1 nRepeaterHealth

NOTIFICATION

APPROPRIATE SYNTAX

A SEQUENCE of 3 data types. The first is mandatory, the following two are optional. The first is value of the attribute aRepeaterHealthState. The second is the value of the attribute aRepeaterHealthText. The third is the value of the attribute aRepeaterHealthData.

BEHAVIOUR DEFINED AS:

This notification conveys information related to the operational state of the repeater. See the aRepeaterHealthState, aRepeaterHealthText, and aRepeaterHealthData attributes for descriptions of the information that is sent. The nRepeaterHealth notification is sent only when the health state of the repeater changes. The nRepeaterHealth notification shall contain repeaterHealthState. repeaterHealthData and repeaterHealthText may or may not be included. The nRepeaterHealth notification is not sent as a result of powering up a repeater.

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19.2.3.3.2 nRepeaterReset

NOTIFICATION
APPROPRIATE SYNTAX
A SEQUENCE of 3 data types. The first is mandatory, the following two are optional. The first is value of the attribute aRepeaterHealthState. The second is the value of the attribute aRepeaterHealthText. The third is the value of the attribute aRepeaterHealthData.
BEHAVIOUR DEFINED AS:
This notification conveys information related to the operational state of the repeater. The nRepeaterReset notification is sent when the repeater is reset as the result of a power-on condition or upon completion of the acResetRepeater action. The nRepeaterReset notification shall contain repeaterHealthState. repeaterHealthData and RepeaterHealthText may, or may not be included.

19.2.3.3.3 nGroupMapChange

NOTIFICATION
APPROPRIATE SYNTAX
BITSTRING
BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the group structure of a repeater. This occurs only when a group is logically removed from or added to a repeater. The nGroupMapChange notification is not sent when powering up a repeater. The value of the notification is the updated value of the aGroupMap attribute.

19.2.4 ResourceTypeID Managed Object Class

Implementation of this managed object in accordance with the definition contained in IEEE Std 802.1F-1993 is a conformance requirement of this International Standard. A single instance of the Resource Type ID managed object exists within the Repeater managed object class. The managed object itself is contained in IEEE Std 802.1F-1993; therefore, only the name binding appears in this International Standard.

19.2.5 Group managed object class

This subclause formally defines the behaviours for Group managed object classes attributes and notification.

19.2.5.1 Group attributes

19.2.5.1.1 aGroupID

ATTRIBUTE
APPROPRIATE SYNTAX
INTEGER
BEHAVIOUR DEFINED AS:
A value unique within the repeater. This value is never greater than aRepeaterGroupCapacity.

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19.2.5.1.2 aGroupPortCapacity

ATTRIBUTE
APPROPRIATE SYNTAX
INTEGER
BEHAVIOUR DEFINED AS:
The aGroupPortCapacity is the number of ports contained within the group. Valid range is 1–1024. Within each group, the ports are uniquely numbered in the range from 1 to aGroupPortCapacity. Some ports may not be present in a given group instance, in which case the actual number of ports present is less than aGroupPortCapacity. The number of ports present is never greater than aGroupPortCapacity.

19.2.5.1.3 aPortMap

ATTRIBUTE
APPROPRIATE SYNTAX
BitString
BEHAVIOUR DEFINED AS:
A string of bits which reflects the current configuration of port managed objects within this group. The length of the bitstring is "aGroupPortCapacity" bits. The first bit relates to group 1. A "1" in the bitstring indicates presence of the port, "0" represents absence of the port.

19.2.5.2 Group Notifications

19.2.5.2.1 nPortMapChange

NOTIFICATION
APPROPRIATE SYNTAX
BitString
BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the port structure of a group. This occurs only when a port is logically removed from or added to a group. The nPortMapChange notification is not sent when powering up a repeater. The value of the notification is the updated value of the aPortMap attribute.

19.2.6 Port managed object class

This subclause formally defines the behaviours for Port managed object classes attributes and action.

19.2.6.1 Port Attributes

19.2.6.1.1 aPortID

ATTRIBUTE
APPROPRIATE SYNTAX
INTEGER
BEHAVIOUR DEFINED AS:
A value unique in the group. It is assumed that ports are partitioned into groups that also have IDs. This value can never be greater than aGroupPortCapacity.

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19.2.6.1.2 aPortAdminState

ATTRIBUTE
APPROPRIATE SYNTAX:
An ENUMERATED VALUE LIST that has the following entries.
disabled
enabled
BEHAVIOUR DEFINED AS:
A disabled port neither transmits nor receives. The port shall be explicitly enabled to restore operation. The acPortAdminControl action provides this ability. The port enable/disable function as reported by this attribute is preserved across repeater reset including loss of power. aPortAdminState takes precedence over auto-partition and functionally operates between the auto-partition mechanism and the AUI/PMA. Auto-partition is reinitialized whenever acPortAdminControl is enabled.

19.2.6.1.3 aAutoPartitionState

ATTRIBUTE
APPROPRIATE SYNTAX:
An ENUMERATED VALUE LIST that has the following entries.
autoPartitioned
notAutoPartitioned
BEHAVIOUR DEFINED AS:
The aAutoPartitionState flag indicates whether the port is currently partitioned by the repeater's auto-partition protection. The conditions that cause port partitioning are specified in partition state machine in Clause 9. They are not differentiated here.

19.2.6.1.4 aReadableFrames

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 15 000 counts per second.
BEHAVIOUR DEFINED AS:
A representation of the total frames of valid frame length. Increment counter by one for each frame whose OctetCount is greater than or equal to minFrameSize and less than or equal to maxFrameSize (see 4.4.2) and for which the FCSError and CollisionEvent signals are not asserted.

NOTE—This statistic provides one of the parameters necessary for obtaining the packet error ratio.

19.2.6.1.5 aReadableOctets

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 1 240 000 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by OctetCount for each frame which has been determined to be a readable frame.

NOTE—This statistic provides an indicator of the total data transferred.

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19.2.6.1.6 aFrameCheckSequenceErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 15 000 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each frame with the FCSError signal asserted and the FramingError and CollisionEvent signals deasserted and whose OctetCount is greater than or equal to minFrameSize and less than or equal to maxFrameSize (see 4.4.2).

19.2.6.1.7 aAlignmentErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 15 000 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each frame with the FCSError and FramingError signals asserted and CollisionEvent signal deasserted and whose OctetCount is greater than or equal to minFrameSize and less than or equal to maxFrameSize (see 4.4.2). If aAlignmentErrors is incremented then the aFrameCheckSequenceErrors attribute shall not be incremented for the same frame.

19.2.6.1.8 aFramesTooLong

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 815 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each frame whose OctetCount is greater than maxFrameSize (see 4.4.2). If aFrameTooLong is counted then neither the aAlignmentErrors nor the aFrameCheckSequenceErrors attribute shall be incremented for the frame.

19.2.6.1.9 aShortEvents

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 75 000 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each CarrierEvent with ActivityDuration less than ShortEventMaxTime. ShortEventMaxTime is greater than 74 bit times and less than 82 bit times. ShortEventMaxTime has tolerances included to provide for circuit losses between a conformance test point at the AUI and the measurement point within the state machine.

NOTE—shortEvents may indicate externally generated noise hits which will cause the repeater to transmit Runts to its other ports, or propagate a collision (which may be late) back to the transmitting DTE and damaged frames to the rest of the network.

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Implementers may wish to consider selecting the ShortEventMaxTime towards the lower end of the allowed tolerance range to accommodate bit losses suffered through physical channel devices not budgeted for within this International Standard.

19.2.6.1.10 aRunts

ATTRIBUTE
APPROPRIATE SYNTAX:

Generalized non-resettable counter. This counter has a maximum increment rate of 75 000 counts per second.

BEHAVIOUR DEFINED AS:

Increment counter by one for each CarrierEvent that meets one of the following two conditions. Only one test need be made. (1) The ActivityDuration is greater than ShortEventMaxTime and less than ValidPacketMinTime and the CollisionEvent signal is deasserted. (2) The OctetCount is less than 64, the ActivityDuration is greater than ShortEventMaxTime and the CollisionEvent signal is deasserted. ValidPacketMinTime is greater than or equal to 552 bit times and less than 565 bit times. An event whose length is greater than 74 bit times but less than 82 bit times shall increment either the aShortEvents attribute or the aRunts attribute but not both. A CarrierEvent greater than or equal to 552 bit times but less than 565 bit times may or may not be counted as a runt. ValidPacketMinTime has tolerances included to provide for circuit losses between a conformance test point at the AUI and the measurement point within the state machine.

NOTE—Runts usually indicate collision fragments, a normal network event. In certain situations associated with large diameter networks a percentage of runts may exceed ValidPacketMinTime.

19.2.6.1.11 aCollisions

ATTRIBUTE
APPROPRIATE SYNTAX:

Generalized non-resettable counter. This counter has a maximum increment rate of 75 000 counts per second.

BEHAVIOUR DEFINED AS:

Increment counter by one for each CarrierEvent in which the CollisionEvent signal is asserted.
Increment counter by one for any CarrierEvent signal on any port in which the CollisionEvent signal on this port is asserted.

19.2.6.1.12 aLateEvents

ATTRIBUTE
APPROPRIATE SYNTAX:

Generalized non-resettable counter. This counter has a maximum increment rate of 75 000 counts per second.

BEHAVIOUR DEFINED AS:

Increment counter by one for each CarrierEvent in which the CollIn(X) variable transitions to the value SQE (see 9.9.6.2) while the ActivityDuration is greater than the LateEventThreshold. Such a CarrierEvent is counted twice, as both a aCollision and as a aLateEvent. The LateEventThreshold is greater than 480 bit times and less than 565 bit times. LateEventThreshold has tolerances included to permit an

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implementation to build a single threshold to serve as both the LateEventThreshold and ValidPacketMinTime threshold.

19.2.6.1.13 aVeryLongEvents

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 250 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each CarrierEvent whose ActivityDuration is greater than the MAU Jabber Lockup Protection timer TW3 (see 9.6.1, 9.6.5). Other counters may be incremented as appropriate.

19.2.6.1.14 aDataRateMismatches

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter.
BEHAVIOUR DEFINED AS:
Increment counter by one for each frame received by this port that meets all of the conditions required by only one of the following two measurement methods: Measurement method A: 1) The CollisionEvent signal is not asserted. 2) The ActivityDuration is greater than ValidPacketMinTime. 3) The frequency (data rate) is detectably mismatched from the local transmit frequency. Measurement method B: 1) The CollisionEvent signal is not asserted. 2) The OctetCount is greater than 63. 3) The frequency (data rate) is detectably mismatched from the local transmit frequency. The exact degree of mismatch is vendor specific and is to be defined by the vendor for conformance testing.
When this event occurs, other counters whose increment conditions were satisfied may or may not also be incremented, at the implementer's discretion.

NOTE—Whether or not the repeater was able to maintain data integrity is beyond the scope of this International Standard.

19.2.6.1.15 aAutoPartitions

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter.
BEHAVIOUR DEFINED AS:
Increment counter by one for each time that the repeater has automatically partitioned this port. The conditions that cause port partitioning are specified in the partition state machine in Clause 9. They are not differentiated here.

19.2.6.1.16 aLastSourceAddress

ATTRIBUTE
APPROPRIATE SYNTAX:
MACAddress
BEHAVIOUR DEFINED AS:

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The aLastSourceAddress attribute is the Source Address of the last readableFrame received by this port.

19.2.6.1.17 aSourceAddressChanges

ATTRIBUTE
APPROPRIATE SYNTAX:

Generalized non-resettable counter. This counter has a maximum increment rate of 15 000 counts per second.

BEHAVIOUR DEFINED AS:

Increment counter by one each time that the aLastSourceAddress attribute has changed.

NOTE—This may indicate whether a link is connected to a single DTE or another multiuser segment.

19.2.6.2 Port Actions

19.2.6.2.1 acPortAdminControl

ACTION
APPROPRIATE SYNTAX:

Same as aPortAdminState.

BEHAVIOUR DEFINED AS:

This action provides a means to alter aPortAdminState and exert a BEGIN on the Auto-Partition state machine (Figure 9–6) upon taking the value “enabled”.

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20. Layer Management for 10 Mb/s baseband medium attachment units

Clause 20 is deprecated by Clause 30.

20.1 Introduction

The MAU Management specification has been developed in accordance with the Open Systems Interconnection (OSI) management architecture as specified in ISO/IEC 7498-4: 1989.

20.1.1 Scope

This clause defines a set of mechanisms that enable management of IEEE 802.3 10 Mb/s integrated Medium Attachment Units (MAUs). In addition, for ports without integral MAUs, attributes are provided for characteristics observable from the AUI of the connected DTE or repeater. Direct management of MAUs that are external to their respective DTEs or repeaters is beyond the scope of this standard. The managed objects within this standard are defined as sets of attributes, actions, notifications, and behaviours in accordance with IEEE Std 802.1-1990 and ISO/IEC International Standards for network management. This clause builds upon the concepts and terminology that are defined more fully in Clause 19.

This standard is defined to be independent of any particular management application or management protocol. The means by which the managed objects defined in this standard are accessed is beyond the scope of this standard.

20.1.2 Management model

See 19.1.5.

20.2 Managed objects

20.2.1 Text description of managed objects

In case of conflict, the formal behaviour definitions in Annex H.3 take precedence over the text descriptions in this clause.

a) **oRepeaterPort.** The managed object that contains the MAU managed object in a repeater set.
b) **oDTEPort.** The managed object that contains the MAU managed object in a DTE.
c) **oMAU.** The managed object of that portion of the containment tree shown in Figure 20–1. The attributes, notifications and actions defined in this clause are contained within the MAU managed object.

Neither counter values nor the value of aMAUadminState is required to be preserved across events involving the loss of power.

20.2.1.1 Naming

The name of an individual managed object is hierarchically defined within a managed system. In the case of MAU management, this will present itself in one of the two forms that are appropriate for a MAU's use, that is, as associated with a CSMA/CD interface of a DTE or with a particular port of a managed repeater. For example, a MAU could be identified as "repeater 3, group 01, port 13, mau 1," that is, the MAU associated with port 13 of group 01 of a repeater with repeaterID 3 within the managed system. An example of this is represented in the relationship of the naming attributes in the Entity Relationship Diagram, Figure 19–3.

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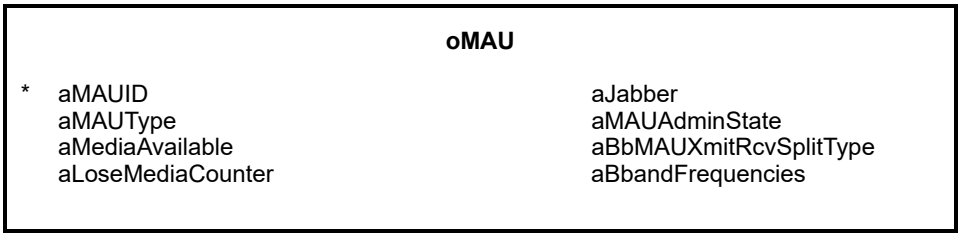

NOTE—The * denotes naming attribute.

Figure 20–1—Entity relationship diagram

20.2.1.2 Containment

A containment relationship is a structuring relationship for managed objects in which the existence of a managed object is dependent on the existence of a containing managed object. The contained managed object is said to be the subordinate managed object, and the containing managed object the superior managed object. MAU management is only valid in a system that provides management at the next higher containment level, that is, either a DTE or Repeater with Layer Management. The containment relationships among object classes are depicted in the Entity Relationship Diagram, Figure 20–1, and specified in the name bindings in Annex H, H.3.1.

20.2.1.3 Packages

This standard and ISO/IEC guidelines make provision for grouping attributes, actions, and notifications in implementation groups, or "packages," within each managed object class. The "Basic Control Package" is mandatory; all other packages are optional. For a managed MAU to be conformant to this standard, it shall fully implement the Basic Control Package. For a MAU to be conformant to an optional package, it shall implement that entire package. While nonconformant (reference aMAUType = "other") MAUs may utilize some or all of this clause to specify their management, conformance to this clause requires both a conformant MAU and conformant management. MAU Management is optional with respect to all other CSMA/CD Management. The packages are summarized in Table 20–1.

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Table 20–1—Packages

			Basic Package (Mandatory)	MAU Control Package (Optional)	Media Loss Tracking Package (Conditional)	Broadband DTE MAU Package (Conditional
MAU managed object class						
aMAUID	ATTRIBUTE	GET	X			
aMAUType	ATTRIBUTE	GET	X			
aMediaAvailable	ATTRIBUTE	GET	X			
aLoseMediaCounter	ATTRIBUTE	GET			X	
aJabber	ATTRIBUTE	GET	X			
aMAUAdminState	ATTRIBUTE	GET	X			
aBbMAUXmitRcvSplitType	ATTRIBUTE	GET				X
aBroadbandFrequencies	ATTRIBUTE	GET				X
acResetMAUAction	ACTION			X		
acMAUAdminControl	ACTION			X		
nJabber	NOTIFICATION		X			

20.2.2 MAU Managed object class

This subclause formally defines the behaviours for MAU Management objects, attributes, actions, and notifications.

20.2.2.1 MAU attributes

20.2.2.1.1 aMAUID

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The value of aMAUID is assigned so as to uniquely identify a MAU among the subordinate managed objects of the containing object.

20.2.2.1.2 aMAUType

ATTRIBUTE
APPROPRIATE SYNTAX:
An INTEGER that meets the requirements of the description below. Additional values are needed for following types:

global	--reserved for future use
other	--see 20.2.1.3
unknown	--initializing, true state or type not yet known

BEHAVIOUR DEFINED AS:
Returns a value that identifies the 10 Mb/s internal MAU type. The enumeration of the type is such that the value matches the clause number of the standard that specifies the particular MAU. If an AUI is to be identified to access an external MAU, then type “AUI” is returned.

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20.2.2.1.3 aMediaAvailable

ATTRIBUTE
APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	--undefined
unknown	--initializing, true state not yet known
available	--link or light normal, loopback normal
not available	--link loss or low light, no loop back
remote fault	--remote fault, applies only to 10BASE-FB
invalid signal	--invalid signal, applies only to 10BASE-FB

BEHAVIOUR DEFINED AS:

If the MAU is a link or fiber type (FOIRL, 10BASE-T, 10BASE-F), then this is equivalent to the link test fail state/low light function. For an AUI or a coaxial cable (including broadband) MAU, this indicates whether or not loopback is detected on the DI circuit. The value of this attribute persists between packets for MAU types AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP.

At power-up or following a reset, the value of this attribute will be "unknown" for AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP MAUs. For these MAUs, loopback will be tested on each transmission during which no collision is detected. If DI is receiving *input* when DO returns to IDL after a transmission and there has been no collision during the transmission, then loopback will be detected. The value of this attribute will only change during noncollided transmissions for AUI, coaxial cable, and 10BASE-FP MAUs.

20.2.2.1.4 aLoseMediaCounter

ATTRIBUTE
APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 10 counts per second.

BEHAVIOUR DEFINED AS:

Counts the number of times that the MAU leaves MediaAvailState "available." Mandatory for MAU type "AUI," optional for all others.

20.2.2.1.5 aJabber

ATTRIBUTE
APPROPRIATE SYNTAX:

A SEQUENCE of two indications.

The first, JabberFlag, consists of an ENUMERATED value list that has the following entries:

other	--undefined
unknown	--initializing, true state not yet known
normal	--state is true or normal
fault	--state is false, fault, or abnormal

The second, jabberCounter, is a generalized nonresetable counter. This counter has a maximum increment rate of 40 counts per second.

BEHAVIOUR DEFINED AS:

If the MAU is in the jabber state, the jabberFlag portion of the attribute is set to the "fault" value. The jabberCounter portion of the attribute is incremented each time the flag is set to the "fault" value. This attribute returns the value "other" for type AUI.

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20.2.2.1.6 aMAUAdminState

ATTRIBUTE
APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	--undefined
unknown	--initializing, true state not yet known
operational	--powered and connected
standby	--inactive but on
shutdown	--similar to power down

BEHAVIOUR DEFINED AS:

A MAU in management state “standby” forces DI and CI to idle and the media transmitter to idle or fault, if supported. The management state “standby” only applies to link type MAUs. The state of MediaAvailable is unaffected. A MAU or AUI in the management state “shutdown” assumes the same condition on DI, CI, and the media transmitter as if it were powered down or not connected. For an AUI, this management state will remove power from the AUI. The MAU may return the value “undefined” for Jabber and MediaAvailable attributes when it is in this management state. A MAU in the management state “operational” is fully functional, and operates and passes signals to its attached DTE or repeater port in accordance to its specification.

20.2.2.1.7 aBbMAUXmitRcvSplitType

ATTRIBUTE
APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	--undefined
single	--single-cable system
dual	--dual-cable system, offset normally zero

BEHAVIOUR DEFINED AS:

Returns a value that indicates the type of frequency multiplexing/cabling system used to separate the transmit and receive paths for the 10BROAD36 MAU. All other types return “undefined.”

20.2.2.1.8 aBroadbandFrequencies

ATTRIBUTE
APPROPRIATE SYNTAX:

A SEQUENCE of two instances of the type INTEGER.
The first INTEGER represents the Transmitter Carrier Frequency. The value of its integer represents the frequency of the carrier divided by 250 kHz.
The second INTEGER represents the Translation Offset Frequency. The value of its integer represents the frequency of the offset divided by 250 kHz.

BEHAVIOUR DEFINED AS:

Returns a value that indicates the transmit carrier frequency and translation offset frequency in MHz/4 for the 10BROAD36 MAU. This allows the frequencies to be defined to a resolution of 250 kHz.

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20.2.2.2 MAU actions

20.2.2.2.1 acResetMAU

ACTION
APPROPRIATE SYNTAX:
None required.
BEHAVIOUR DEFINED AS:
Resets the MAU in the same manner as would a power-off, power-on cycle of at least 0.5 s duration. During the 0.5 s DO, DI, and CI should be idle.

20.2.2.2.2 acMAUAdminControl

ACTION
APPROPRIATE SYNTAX:
The same as used for **aMAUAdminState**
BEHAVIOUR DEFINED AS:
Executing an acMAUAdminControl action causes the MAU to assume the aMAUAdminState attribute value of one of the defined valid management states for control input. The valid inputs are “standby,” “operational,” and “shutdown” state (see the behaviour definition bMAUAdminState for the description of each of these states) except that a “standby” action to a mixing type MAU or an AUI will cause the MAU to enter the “shutdown” management state.

20.2.2.3 MAU notifications

20.2.2.3.1 nJabber

NOTIFICATION
APPROPRIATE SYNTAX:
The same as used for **aJabber**
BEHAVIOUR DEFINED AS:
The notification is sent whenever a managed MAU enters the jabber state.

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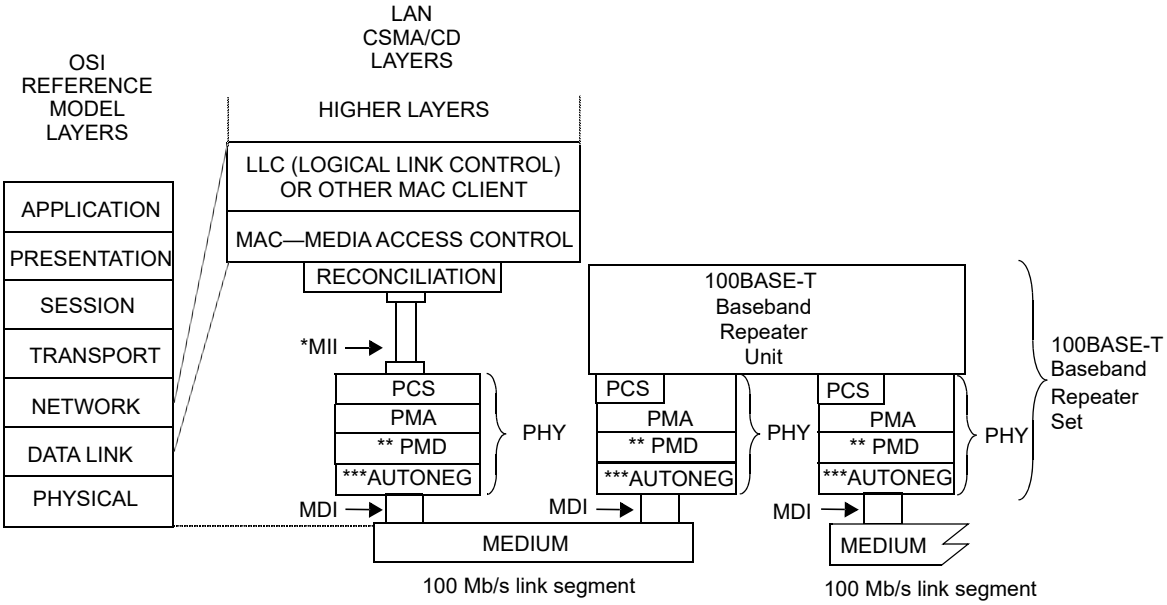
21. Introduction to 100 Mb/s baseband networks, type 100BASE-T

21.1 Overview

100BASE-T couples the IEEE 802.3 CSMA/CD MAC with a family of 100 Mb/s Physical Layers. While the MAC can be readily scaled to higher performance levels, new Physical Layer standards are required for 100 Mb/s operation.

The relationships between 100BASE-T, the existing IEEE 802.3 (CSMA/CD MAC), and the ISO/IEC Open System Interconnection (OSI) reference model is shown in Figure 21–1.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
** PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.
Use of MII between PCS and Baseband Repeater Unit is optional.
*** AUTONEG is optional.

Figure 21–1—Architectural positioning of 100BASE-T

100BASE-T uses the existing IEEE 802.3 MAC layer interface, connected through a Media-Independent Interface layer to a Physical Layer device (PHY) such as 100BASE-T4, 100BASE-TX, or 100BASE-FX.

100BASE-T extends the IEEE 802.3 MAC to 100 Mb/s. The bit rate is faster, bit times are shorter, packet transmission times are reduced, and cable delay budgets are smaller—all in proportion to the change in bandwidth. This means that the ratio of packet duration to network propagation delay for 100BASE-T is the same as for 10BASE-T.

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21.1.1 Reconciliation Sublayer (RS) and Media Independent Interface (MII)

The Media Independent Interface (Clause 22) provides an interconnection between the Media Access Control (MAC) sublayer and Physical Layer devices (PHYs) and between PHY Layer and Station Management (STA) entities. This MII is capable of supporting both 10 Mb/s and 100 Mb/s data rates through four bit wide (nibble wide) transmit and receive paths. The Reconciliation sublayer provides a mapping between the signals provided at the MII and the MAC/PLS service definition.

21.1.2 Physical Layer signaling systems

The following portion of this standard specifies a family of Physical Layer implementations. Typically 100BASE-TX (Clause 24 and Clause 25) uses two pairs of Category 5 balanced cabling as defined by ISO/IEC 11801, 100BASE-FX (Clause 24 and Clause 26) uses two multimode fibers. There are a number of other PHY types and their associated media.

21.1.3 Repeater

Repeater sets (Clause 27) are an integral part of any 100BASE-T network with more than two DTEs in a collision domain. They extend the physical system topology by coupling two or more segments. Multiple repeaters are permitted within a single collision domain to provide the maximum path length.

21.1.4 Auto-Negotiation

Auto-Negotiation (Clause 28) provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation. Auto-Negotiation is performed out-of-band using a pulse code sequence that is compatible with the 10BASE-T link integrity test sequence.

21.1.5 Management

Managed objects, attributes, and actions are defined for all 100BASE-T components (Clause 30).

21.2 References

See 1.3.

21.3 Definitions

See 1.4.

21.4 Abbreviations

See 1.5.

21.5 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, with the following extensions.

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21.5.1 Actions inside state blocks

The actions inside a state block execute instantaneously. Actions inside state blocks are atomic (i.e., uninterruptible).

After performing all the actions listed in a state block one time, the state block then continuously evaluates its exit conditions until one is satisfied, at which point control passes through a transition arrow to the next block. While the state awaits fulfillment of one of its exit conditions, the actions inside do not implicitly repeat.

The characters • and [bracket] are *not* used to denote any special meaning.

Valid state actions may include .indication and .request messages.

No actions are taken outside of any state block.

21.5.2 State diagram variables

Once set, variables retain their values as long as succeeding blocks contain no references to them.

Setting the parameter of a formal interface message assures that, on the next transmission of that message, the last parameter value set will be transmitted.

Testing the parameter of a formal interface messages tests the value of that message parameter that was received on the last transmission of said message. Message parameters may be assigned default values that persist until the first reception of the relevant message.

21.5.3 State transitions

The following terms are valid transition qualifiers:

a) Boolean expressions
b) An event such as the expiration of a timer: timer_done
c) An event such as the reception of a message: PMA_UNITDATA.indication
d) An unconditional transition: UCT
e) A branch taken when other exit conditions are not satisfied: ELSE

Any open arrow (an arrow with no source block) represents a global transition. Global transitions are evaluated continuously whenever any state is evaluating its exit conditions. When a global transition becomes true, it supersedes all other transitions, including UCT, returning control to the block pointed to by the open arrow.

21.5.4 Operators

The state diagram operators are shown in Table 21–1.

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Table 21–1—State diagram operators

Character	Meaning
*	Boolean AND
+	Boolean OR
∧	Boolean XOR
!	Boolean NOT
<	Less than
≤	Less than or equal to
=	Equals (a test of equality)
≠	Not equals
≥	Greater than or equal to
>	Greater than
( )	Indicates precedence
⇐	Assignment operator
∈	Indicates membership
∉	Indicates nonmembership
|	Catenate
ELSE	No other state condition is satisfied

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21.6 Protocol implementation conformance statement (PICS) proforma

21.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to any 100 Mb/s portion of this standard shall complete a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. The PICS can be used for a variety of purposes by various parties, including the following:

a) As a checklist by the protocol implementer, to reduce the risk of failure to conform to the standard through oversight;
b) As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
c) As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICS);
d) As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

21.6.2 Abbreviations and special symbols

The following symbols are used in the PICS proforma:

M	mandatory field/function
!	negation
O	optional field/function
O.<n>	optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n>	optional field/function, but one and only one of the group of options labeled by the same numeral <n> is required
X	prohibited field/function
<item>:	simple-predicate condition, dependent on the support marked for <item>
<item1>*<item2>:	AND-predicate condition, the requirement has to be met if both optional items are implemented

21.6.3 Instructions for completing the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

The main part of the PICS proforma is a fixed-format questionnaire divided into subclauses, each containing a group of items. Each item is identified by an item reference in the first column. Additional columns contain the question to be answered, the reference or references to the material that specifies the item in the main body of the standard, values and/or comments pertaining to the question to be answered, and the status of the item (whether support is mandatory, optional, or conditional). Answers to the questionnaire items are to be provided in a column labeled “Support”. This is done either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable) or by entering a value or a set or a range of values. There are some items where two or more choices from a set of possible answers can apply and all relevant choices are to be marked.

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The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the protocol implementation conformance statement for the implementation in question.

Note that where an implementation is capable of being configured in more than one way, according to the items listed under Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation's configuration capabilities, if that would make presentation of the information easier and clearer.

21.6.4 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features that, although optional, are nonetheless commonly present in implementations.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

21.6.5 Exceptional information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this standard.

Note that a possible reason for the situation described above is that a defect in the standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

21.6.6 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M (Mandatory), O (Optional), or X (Not Applicable).

If the item referred to by the conditional symbol is marked as supported, then 1) the conditional item is applicable, 2) its status is given by "<s>", and 3) the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

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Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

21.7 MAC delay constraints (exposed MII)

100BASE-T makes the following assumptions about MAC performance. These assumptions apply to any MAC operating in half duplex mode with an exposed MII.

Table 21–2—MAC delay assumptions (exposed MII)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MAC ⇔ MII	MAC transmit start to TX_EN sampled		4		TX_CLK rising
	CRS assert to MAC detect	0	8		
	CRS deassert to MAC detect	0	8		
	CRS assert to TX_EN sampled (worst case nondeferred transmit)		16		TX_CLK rising
	COL assert to MAC detect	0	8		
	COL deassert to MAC detect	0	8		
	COL assert to TXD = Jam sampled (worst-case collision response)		16		TX_CLK rising; first nibble of jam

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22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

22.1 Overview

This clause defines the logical, electrical, and mechanical characteristics for the Reconciliation Sublayer (RS) and Media Independent Interface (MII) between CSMA/CD media access controllers and various PHYs. Figure 22–1 shows the relationship of the Reconciliation sublayer and MII to the ISO/IEC OSI reference model.

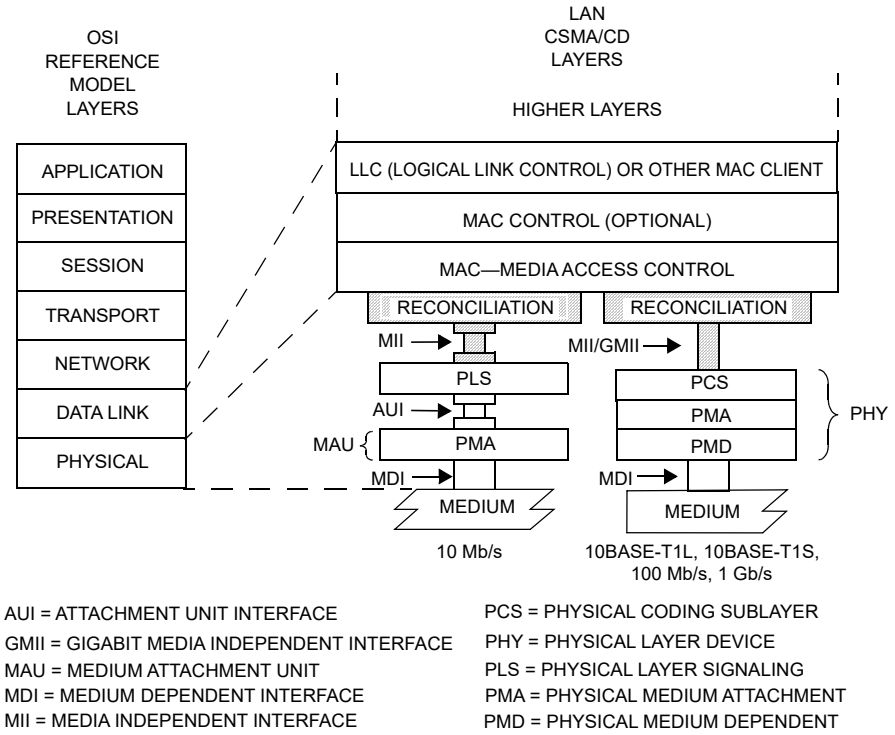

Figure 22–1—MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

The purpose of this interface is to provide a simple, inexpensive, and easy-to-implement interconnection between Media Access Control (MAC) sublayers and PHYs for data transfer at 10 Mb/s and 100 Mb/s, and between Station Management (STA) and PHYs.

This interface has the following characteristics:

a) It is capable of supporting 10 Mb/s and 100 Mb/s rates for data transfer, and management functions.
b) Data and delimiters are synchronous to clock references.
c) It provides independent four bit wide transmit and receive data paths.
d) It uses TTL signal levels, compatible with common digital CMOS ASIC processes.
e) It provides a simple management interface.
f) It is capable of driving a limited length of shielded cable.
g) It provides full duplex operation.

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22.1.1 Summary of major concepts

a) Each direction of data transfer is serviced with seven (making a total of 14) signals: Data (a four-bit bundle), Delimiter, Error, and Clock.
b) Two media status signals are provided. One indicates the presence of carrier, and the other indicates the occurrence of a collision.
c) A management interface composed of two signals provides access to management parameters and services.
d) The Reconciliation sublayer maps the signal set provided at the MII to the PLS service definition specified in Clause 6.

22.1.2 Application

This clause applies to the interface between MAC sublayer and PHYs, and between PHYs and Station Management entities. The implementation of the interface may assume any of the following three forms:

a) A chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board.
b) A motherboard to daughterboard interface between two or more printed circuit boards.
c) An interface between two printed circuit assemblies that are attached with a length of cable and an appropriate connector.

Figure 22–2 provides an example of the third application environment listed above. All MII conformance tests are performed at the mating surfaces of the MII connector, identified by the line A-A.

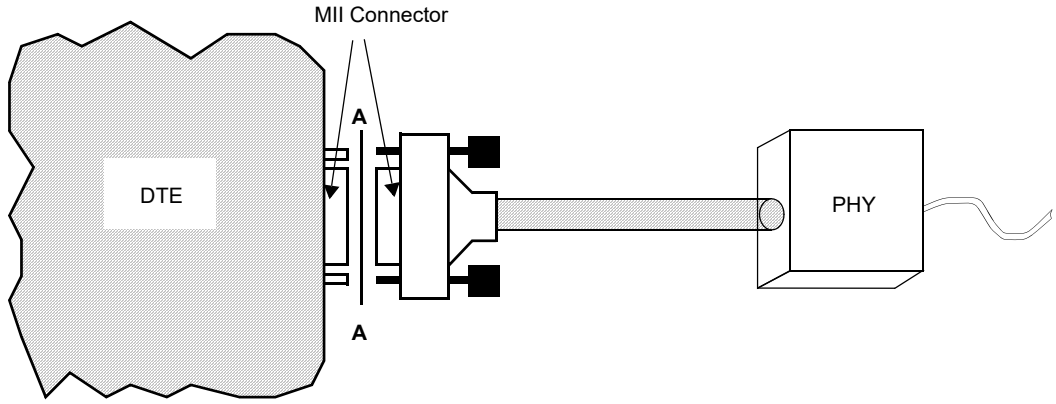

Figure 22–2—Example application showing location of conformance test

This interface is used to provide media independence for various forms of unshielded twisted-pair wiring, shielded twisted-pair wiring, fiber optic cabling, and potentially other media, so that identical media access controllers may be used with any of these media.

To allow for the possibility that multiple PHYs may be controlled by a single station management entity, the MII management interface has provisions to accommodate up to 32 PHYs, with the restriction that a maximum of one PHY may be attached to a management interface via the mechanical interface defined in 22.6.

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22.1.3 Rates of operation

The MII can support two specific data rates, 10 Mb/s and 100 Mb/s. The functionality is identical at both data rates, as are the signal timing relationships. The only difference between 10 Mb/s and 100 Mb/s operation is the nominal clock frequency.

PHYs that provide an MII are not required to support both data rates, and may support either one or both. PHYs have to report the rates they are capable of operating at via the management interface, as described in 22.2.4.

22.1.4 Allocation of functions

The allocation of functions at the MII is such that it readily lends itself to implementation in both PHYs and MAC sublayer entities. The division of functions balances the need for media independence with the need for a simple and cost-effective interface.

While the Attachment Unit Interface (AUI) was defined to exist between the Physical Signaling (PLS) and Physical Media Attachment (PMA) sublayers for 10 Mb/s DTEs, the MII maximizes media independence by cleanly separating the Data Link and Physical Layers of the ISO (IEEE) seven-layer reference model. This allocation also recognizes that implementations can benefit from a close coupling of the PLS or PCS sublayer and the PMA sublayer.

22.1.5 Relationship of MII and GMII

The Gigabit Media Independent Interface (GMII) is similar to the MII. The GMII uses the MII Management Interface and register set specified in 22.2.4. These common elements of operation allow Station Management to determine PHY capabilities and configure the station based on those capabilities. In a station supporting both MII and GMII operation, configuration of the station would include enabling either the MII or GMII operation as appropriate for the data rate of the selected PHY.

Most of the MII and GMII signals use the same names, but the width of the RXD and TXD data bundles and the semantics of the associated control signals differ between MII and GMII operation. The GMII transmit path clocking also differs significantly from MII clocking. MII operation of these signals and clocks is specified within Clause 22 and GMII operation is specified within Clause 35.

22.2 Functional specifications

The MII is designed to make the differences among the various media absolutely transparent to the MAC sublayer. The selection of logical control signals and the functional procedures are all designed to this end. Additionally, the MII is designed to be easily implemented at minimal cost using conventional design techniques and manufacturing processes.

22.2.1 Mapping of MII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the MII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the Reconciliation sublayer behave in exactly the same manner as defined in Clause 6. The MII signals are defined in detail in 22.2.2.The mapping is changed if EEE capability is supported (see 78.3), as described in 22.7. EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

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Figure 22–3 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the MII management interface is controlled by the station management entity (STA).

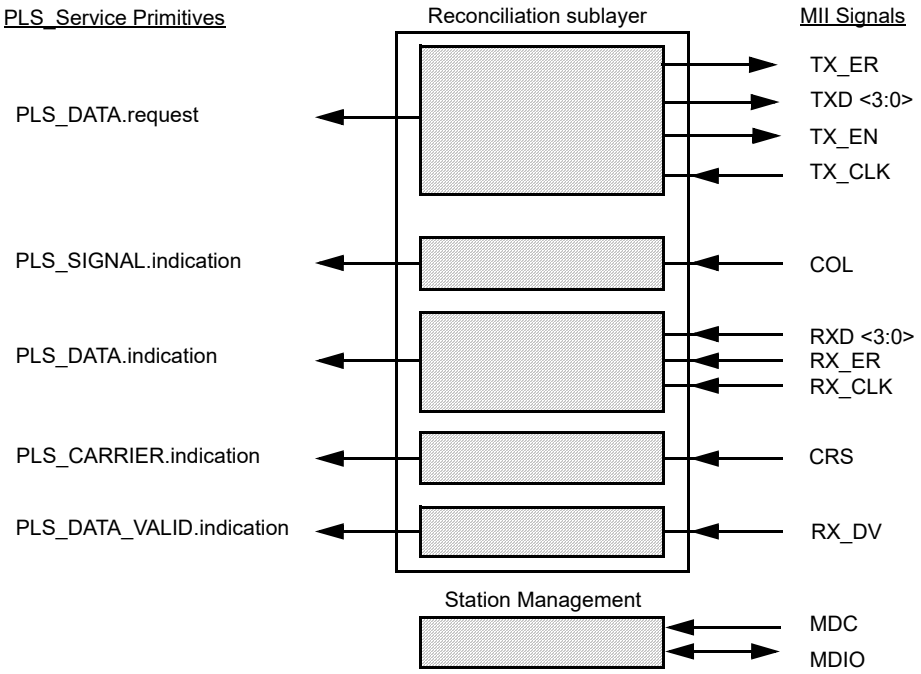

Figure 22–3—Reconciliation Sublayer (RS) inputs and outputs, and STA connections to MII

22.2.1.1 Mapping of PLS_DATA.request

22.2.1.1.1 Function

Map the primitive PLS_DATA.request to the MII signals TXD<3:0>, TX_EN, and TX_CLK.

22.2.1.1.2 Semantics of the service primitive

PLS_DATA.request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take one of three values: ONE, ZERO, or DATA_COMPLETE. It represents a single data bit. The values ONE and ZERO are conveyed by the signals TXD<3>, TXD<2>, TXD<1> and TXD<0>, each of which conveys one bit of data while TX_EN is asserted. The value DATA_COMPLETE is conveyed by the deassertion of TX_EN. Synchronization between the Reconciliation sublayer and the PHY is achieved by way of the TX_CLK signal.

22.2.1.1.3 When generated

The TX_CLK signal is generated by the PHY. The TXD<3:0> and TX_EN signals are generated by the Reconciliation sublayer after every group of four PLS_DATA.request transactions from the MAC sublayer to request the transmission of four data bits on the physical medium or to stop transmission.

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22.2.1.2 Mapping of PLS_DATA.indication

22.2.1.2.1 Function

Map the primitive PLS_DATA.indication to the MII signals RXD<3:0>, RX_DV, RX_ER, and RX_CLK.

22.2.1.2.2 Semantics of the service primitive

PLS_DATA.indication (INPUT_UNIT)

The INPUT_UNIT parameter can take one of two values: ONE or ZERO. It represents a single data bit. The values ONE and ZERO are derived from the signals RXD<3>, RXD<2>, RXD<1>, and RXD<0>, each of which represents one bit of data while RX_DV is asserted.

The value of the data transferred to the MAC is controlled by the RX_ER signal, see 22.2.1.5, Response to RX_ER indication from MII.

Synchronization between the PHY and the Reconciliation sublayer is achieved by way of the RX_CLK signal.

22.2.1.2.3 When generated

This primitive is generated to all MAC sublayer entities in the network after a PLS_DATA.request is issued. Each nibble of data transferred on RXD<3:0> will result in the generation of four PLS_DATA.indication transactions.

22.2.1.3 Mapping of PLS_CARRIER.indication

22.2.1.3.1 Function

Map the primitive PLS_CARRIER.indication to the MII signal CRS, and the LPI assert function if the EEE capability supported (see 22.7.2).

22.2.1.3.2 Semantics of the service primitive

PLS_CARRIER.indication (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. The values CARRIER_ON and CARRIER_OFF are derived from the MII signal CRS.

22.2.1.3.3 When generated

The PLS_CARRIER.indication service primitive is generated by the Reconciliation sublayer whenever the CARRIER_STATUS parameter changes from CARRIER_ON to CARRIER_OFF or vice versa.

Any transition of the CRS signal from deasserted to asserted causes a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and any transition of the CRS signal from asserted to deasserted causes a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value.

NOTE—The behavior of the CRS signal is specified within this clause so that it can be mapped directly (with the appropriate implementation-specific synchronization) to the carrierSense variable in the MAC process Deference, which is described in 4.2.8. The behavior of the RX_DV signal is specified within this clause so that it can be mapped directly to

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the receiveDataValid variable in the MAC process BitReceiver, which is described in 4.2.9, provided that the MAC processBitReceiver is implemented to receive a nibble of data on each cycle through the inner loop.

For EEE capability, CARRIER_STATUS is overridden according to the behavior of the LPI transmit state diagram (see Figure 22–23). The signal CRS has no effect on CARRIER_STATUS while in states LPI_ASSERTED and LPI_WAIT. A transition to the LPI_ASSERTED state in the transmit LPI state diagram shall cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and a transition to the LPI_DEASSERTED state in the transmit LPI state diagram shall cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value.

22.2.1.4 Mapping of PLS_SIGNAL.indication

22.2.1.4.1 Function

Map the primitive PLS_SIGNAL.indication to the MII signal COL.

22.2.1.4.2 Semantics of the service primitive

PLS_SIGNAL.indication (SIGNAL_STATUS)

The SIGNAL_STATUS parameter can take one of two values: SIGNAL_ERROR or NO_SIGNAL_ERROR. SIGNAL_STATUS assumes the value SIGNAL_ERROR when the MII signal COL is asserted, and assumes the value NO_SIGNAL_ERROR when COL is deasserted.

22.2.1.4.3 When generated

The PLS_SIGNAL.indication service primitive is generated whenever SIGNAL_STATUS makes a transition from SIGNAL_ERROR to NO_SIGNAL_ERROR or vice versa.

22.2.1.5 Response to RX_ER indication from MII

If, during frame reception, both RX_DV and RX_ER are asserted, the Reconciliation sublayer shall ensure that the MAC will detect a FrameCheckError in that frame.

This requirement may be met by incorporating a function in the Reconciliation sublayer that produces a result that is guaranteed to be not equal to the CRC result, as specified by the algorithm in 3.2.9, of the sequence of nibbles comprising the received frame as delivered to the MAC sublayer. The Reconciliation sublayer has to then ensure that the result of this function is delivered to the MAC sublayer at the end of the received frame in place of the last nibble(s) received from the MII.

Other techniques may be employed to respond to RX_ER, provided that the result is that the MAC sublayer behaves as though a FrameCheckError occurred in the received frame.

22.2.1.6 Conditions for generation of TX_ER

If, during the process of transmitting a frame, it is necessary to request that the PHY deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability, then the signal TX_ER may be generated.

For example, a repeater that detects an RX_ER during frame reception on an input port may propagate that error indication to its output ports by asserting TX_ER during the process of transmitting that frame.

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Since there is no mechanism in the definition of the MAC sublayer by which the transmit data stream can be deliberately corrupted, the Reconciliation sublayer is not required to generate TX_ER.

22.2.1.7 Mapping of PLS_DATA_VALID.indication

22.2.1.7.1 Function

Map the primitive PLS_DATA_VALID.indication to the MII signal RX_DV.

22.2.1.7.2 Semantics of the service primitive

PLS_DATA_VALID.indication (DATA_VALID_STATUS)

The DATA_VALID_STATUS parameter can take one of two values: DATA_VALID or DATA_NOT_VALID. DATA_VALID_STATUS assumes the value DATA_VALID when the MII signal RX_DV is asserted, and assumes the value DATA_NOT_VALID when RX_DV is deasserted.

22.2.1.7.3 When generated

The PLS_DATA_VALID.indication service primitive is generated by the Reconciliation sublayer whenever the DATA_VALID_STATUS parameter changes from DATA_VALID to DATA_NOT_VALID or vice versa.

22.2.2 MII signal functional specifications

22.2.2.1 TX_CLK (transmit clock)

TX_CLK (Transmit Clock) is a continuous clock that provides the timing reference for the transfer of the TX_EN, TXD, and TX_ER signals from the Reconciliation sublayer to the PHY. TX_CLK is sourced by the PHY.

The TX_CLK frequency shall be 25% of the nominal transmit data rate ± 100 ppm. For example, a PHY operating at 100 Mb/s has to provide a TX_CLK frequency of 25 MHz, and a PHY operating at 10 Mb/s has to provide a TX_CLK frequency of 2.5 MHz. The duty cycle of the TX_CLK signal shall be between 35% and 65% inclusive.

NOTE—See additional information in 22.2.4.1.5.

22.2.2.2 RX_CLK (receive clock)

RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV, RXD, and RX_ER signals from the PHY to the Reconciliation sublayer. RX_CLK is sourced by the PHY. The PHY may recover the RX_CLK reference from the received data or it may derive the RX_CLK reference from a nominal clock (e.g., the TX_CLK reference).

The minimum high and low times of RX_CLK shall be 35% of the nominal period under all conditions.

While RX_DV is asserted, RX_CLK shall be synchronous with recovered data, shall have a frequency equal to 25% of the data rate of the received signal, and shall have a duty cycle of between 35% and 65% inclusive.

When the signal received from the medium is continuous and the PHY can recover the RX_CLK reference and supply the RX_CLK on a continuous basis, there is no need to transition between the recovered clock reference and a nominal clock reference on a frame-by-frame basis. If loss of received signal from the

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medium causes a PHY to lose the recovered RX_CLK reference, the PHY shall source the RX_CLK from a nominal clock reference.

Transitions from nominal clock to recovered clock or from recovered clock to nominal clock shall be made only while RX_DV is deasserted. During the interval between the assertion of CRS and the assertion of RX_DV at the beginning of a frame or while the PHY is asserting LPI, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition until the PHY has successfully locked onto the recovered clock. Following the deassertion of RX_DV at the end of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition for an interval that shall not exceed twice the nominal clock period. For EEE capability, RX_CLK may be stopped by the PHY during LPI when the Clock stop enable bit is asserted (see 22.2.2.9 and 45.2.3.1.4).

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. See additional information in 22.2.4.1.5 and 22.2.2.9.

22.2.2.3 TX_EN (transmit enable)

TX_EN indicates that the Reconciliation sublayer is presenting nibbles on the MII for transmission. It shall be asserted by the Reconciliation sublayer synchronously with the first nibble of the preamble and shall remain asserted while all nibbles to be transmitted are presented to the MII. TX_EN shall be negated prior to the first TX_CLK following the final nibble of a frame. TX_EN is driven by the Reconciliation sublayer and shall transition synchronously with respect to the TX_CLK.

Figure 22–4 depicts TX_EN behavior during a frame transmission with no collisions.

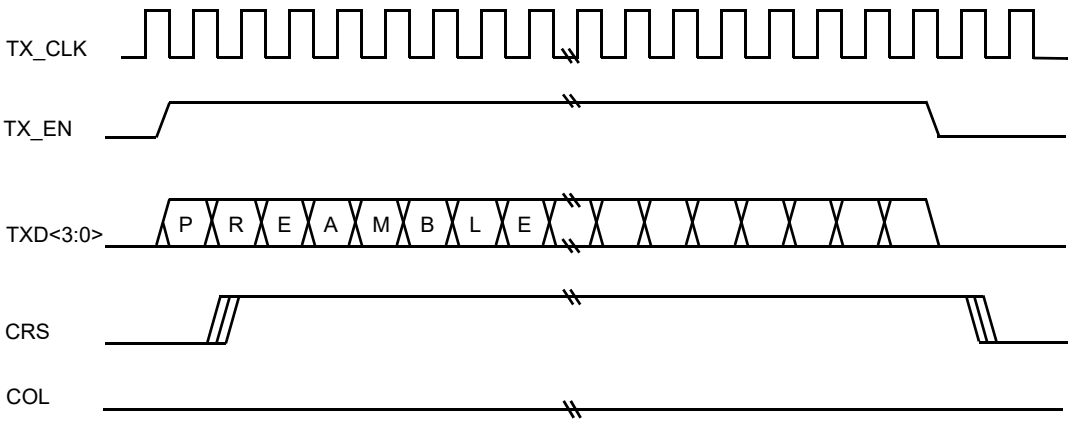

Figure 22–4—Transmission with no collision

22.2.2.4 TXD (transmit data)

TXD is a bundle of 4 data signals (TXD<3:0>) that are driven by the Reconciliation sublayer. TXD<3:0> shall transition synchronously with respect to the TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD<3:0> are accepted for transmission by the PHY. TXD<0 >is the least significant bit. While TX_EN and TX_ER are both deasserted, TXD<3:0> shall have no effect upon the PHY.

For EEE capability, the RS shall use the combination of TX_EN deasserted, TX_ER asserted, and TXD<3:0> equal to 0001 as shown in Table 22–1 as a request to enter, or remain in a low power state.

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When PLCA capability is supported and enabled (see 30.16.1.1.1), the RS shall use the combination of TX_EN deasserted, TX_ER asserted, and TXD<3:0> equal to 0010 or 0011 as shown in Table 22–1 to send respectively a BEACON request or a COMMIT request as defined in 148.4.4.1.

When TX_EN is deasserted and TX_ER is asserted, values of TXD<3:0> other than 0001, 0010, and 0011 shall have no effect upon the PHY.

Figure 22–4 depicts TXD<3:0> behavior during the transmission of a frame.

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

Table 22–1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Reserved
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON request
0	1	0011	PLCA COMMIT request
0	1	0100 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

22.2.2.5 TX_ER (transmit coding error)

TX_ER shall transition synchronously with respect to the TX_CLK. When TX_ER is asserted for one or more TX_CLK periods while TX_EN is also asserted, the PHY shall emit one or more symbols that are not part of the valid data or delimiter set somewhere in the frame being transmitted. The relative position of the error within the frame need not be preserved.

Assertion of the TX_ER signal shall not affect the transmission of data when TX_EN is deasserted. Additionally, the assertion of the TX_ER signal shall not affect the transmission of data when a PHY is operating at 10 Mb/s, with the exception of 10BASE-T1L (see 146.3.3.1) and 10BASE-T1S (see 147.3.2.1, Figure 147–4).

Figure 22–5 shows the behavior of TX_ER during the transmission of a frame propagating an error.

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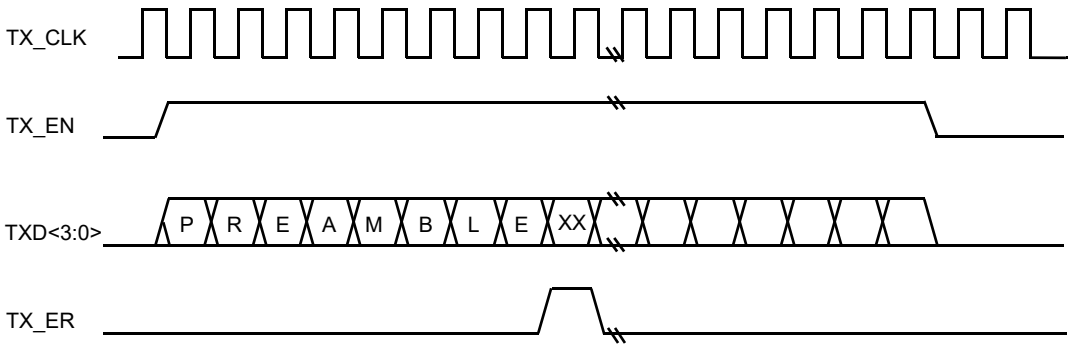

Figure 22–5—Propagating an error

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

The TX_ER signal shall be implemented at the MII of a PHY, may be implemented at the MII of a repeater that provides an MII port, and may be implemented in MAC sublayer devices. If a Reconciliation sublayer or a repeater with an MII port does not actively drive the TX_ER signal, it shall ensure that the TX_ER signal is pulled down to an inactive state at all times.

22.2.2.6 Transmit direction LPI transition

When the transmit LPI state diagram is in state LPI_ASSERTED, the LPI client requests the PHY to transition to the LPI state by deasserting TX_EN, asserting TX_ER, and setting TXD<3:0> to 0001. The LPI client maintains the same state for these signals for the entire time that the PHY is to remain in the LPI state.

The LPI client requests the PHY to transition out of the LPI state by deasserting TX_ER and TXD. The LPI client should not assert TX_EN for valid transmit data until after the resolved wake up time specified for the PHY.

Figure 22–6 shows the behavior of TX_EN, TX_ER, and TXD<3:0> during the transition into and out of the LPI state.

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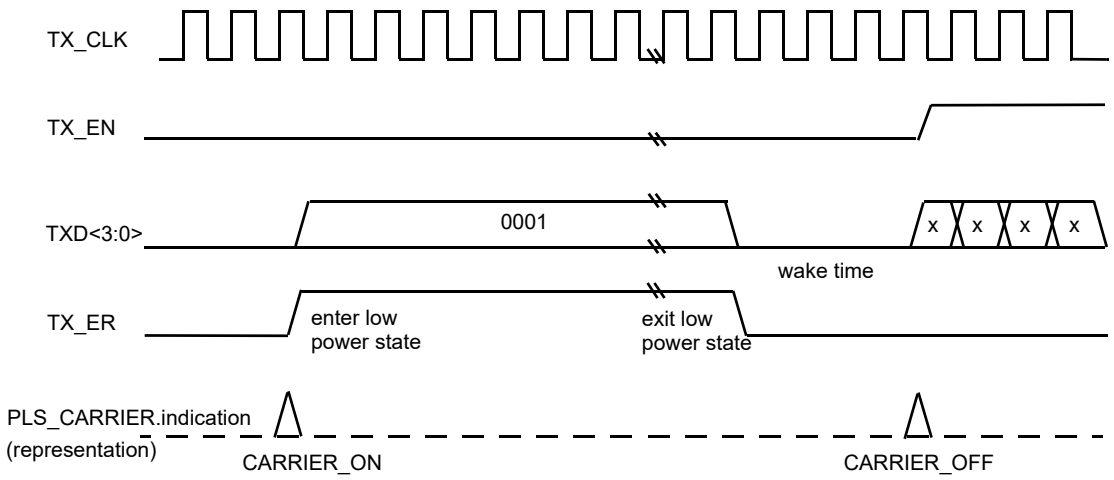

Figure 22–6—LPI transition

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

22.2.2.7 RX_DV (Receive Data Valid)

RX_DV (Receive Data Valid) is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on the RXD<3:0> bundle and that the data on RXD<3:0> is synchronous to RX_CLK. RX_DV shall transition synchronously with respect to the RX_CLK. RX_DV shall remain asserted continuously from the first recovered nibble of the frame through the final recovered nibble and shall be negated prior to the first RX_CLK that follows the final nibble. In order for a received frame to be correctly interpreted by the Reconciliation sublayer and the MAC sublayer, RX_DV has to encompass the frame, starting no later than the Start Frame Delimiter (SFD) and excluding any End-of-Frame delimiter.

Figure 22–7 shows the behavior of RX_DV during frame reception.

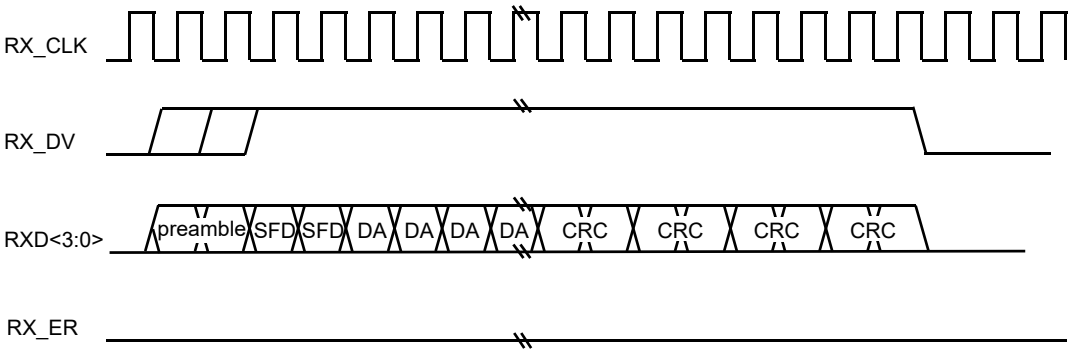

Figure 22–7—Reception with no errors

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22.2.2.8 RXD (receive data)

RXD is a bundle of four data signals (RXD<3:0>) that transition synchronously with respect to the RX_CLK. RXD<3:0> are driven by the PHY. For each RX_CLK period in which RX_DV is asserted, RXD<3:0> transfer four bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the least significant bit. While RX_DV is deasserted, RXD<3:0> shall have no effect on the Reconciliation sublayer.

While RX_DV is deasserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal while driving the value <1110> onto RXD<3:0>. See 24.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

For EEE capability, the PHY indicates that it is receiving LPI by asserting the RX_ER signal and driving the value 0001 onto RXD<3:0> while RX_DV is deasserted.

When PLCA capability is supported and enabled, the PHY indicates that it is receiving a BEACON or COMMIT by asserting the RX_ER signal and driving respectively the values 0010 or 0011 onto RXD<3:0> while RX_DV is deasserted. See 148.4.4.1 for the definition and usage of PLCA BEACON and COMMIT.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD has to be passed across the MII. In a DTE operating in half duplex mode, a PHY is not required to loop data transmitted on TXD<3:0> back to RXD<3:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2. In a DTE operating in full duplex mode, data transmitted on TXD <3:0> has to not be looped back to RXD <3:0> unless the loopback mode of operation is selected.

Figure 22–7 shows the behavior of RXD<3:0> during frame reception.

Table 22–2 summarizes the permissible encoding of RXD<3:0>, RX_ER, and RX_DV, along with the specific indication provided by each code.

Table 22–2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON indication
0	1	0011	PLCA COMMIT indication
0	1	0100 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

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22.2.2.9 Receive direction LPI transition

When the PHY receives signals from the link partner to indicate transition into the low power state, it indicates this to the LPI client by asserting RX_ER and setting RXD<3:0> to 0001 while keeping RX_DV deasserted. The PHY maintains these signals in this state while it remains in the low power state. When the PHY receives signals from the link partner to indicate transition out of the low power state, it indicates this to the LPI client by deasserting RX_ER and returning to a normal interframe state.

While the PHY device is indicating LPI, it may halt the RX_CLK at any time more than 9 clock cycles after the start of the low power state as shown in (Figure 22–8) if and only if the Clock stop enable bit is asserted (see 45.2.3.1.4). The PHY may restart RX_CLK at any time while it is asserting LPI, but shall restart RX_CLK so that at least one positive transition occurs before it deasserts LPI.

Figure 22–8 shows the behavior of RX_ER, RX_DV and RXD<3:0> during LPI transitions.

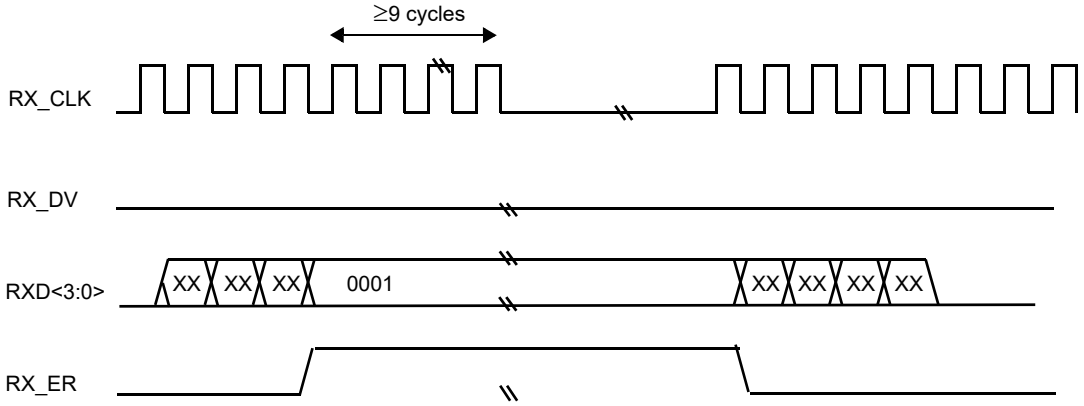

Figure 22–8—LPI transitions (receiver)

22.2.2.10 RX_ER (receive error)

RX_ER (Receive Error) is driven by the PHY. RX_ER shall be asserted for one or more RX_CLK periods to indicate to the Reconciliation sublayer that an error (e.g., a coding error, or any error that the PHY is capable of detecting, and that may otherwise be undetectable at the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY to the Reconciliation sublayer. RX_ER shall transition synchronously with respect to RX_CLK. While RX_DV is deasserted, RX_ER shall have no effect on the Reconciliation sublayer.

While RX_DV is deasserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal for at least one cycle of the RX_CLK while driving the appropriate value onto RXD<3:0>, as defined in 22.2.2.8. See 24.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

The effect of RX_ER on the Reconciliation sublayer is defined in 22.2.1.5, Response to RX_ER indication from MII.

Figure 22–9 shows the behavior of RX_ER during the reception of a frame with errors.

Figure 22–10 shows the behavior of RX_ER, RX_DV and RXD<3:0> during a False Carrier indication.

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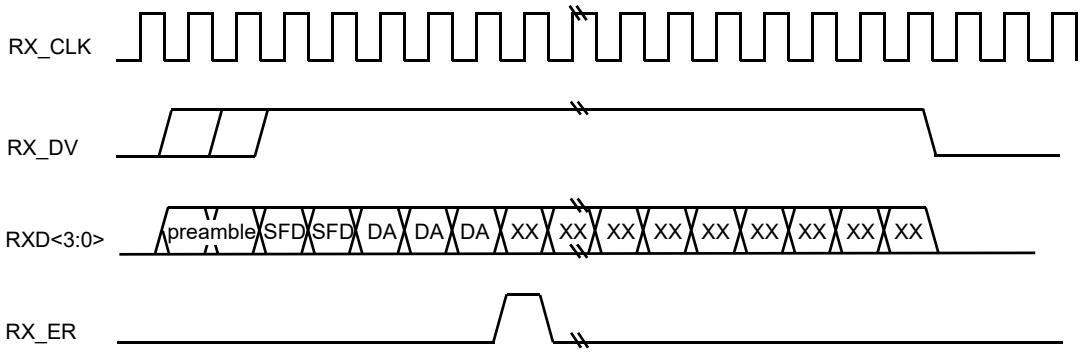

Figure 22–9—Reception with errors

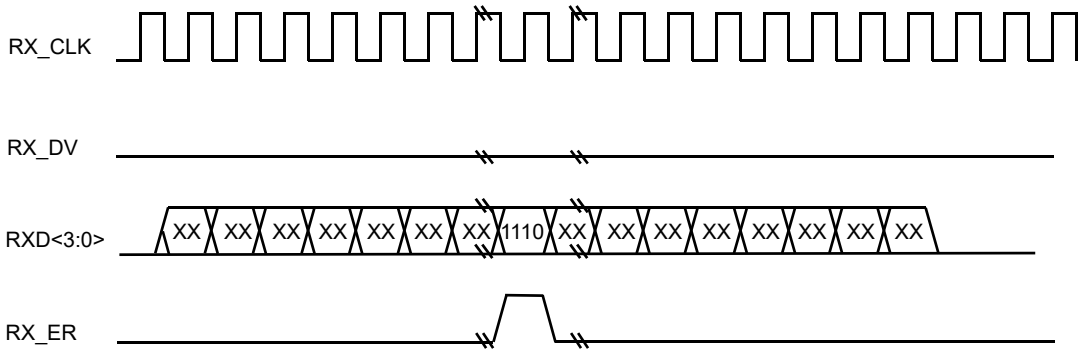

Figure 22–10—False Carrier indication

22.2.2.11 CRS (carrier sense)

CRS shall be asserted by the PHY when either the transmit or receive medium is nonidle. CRS shall be deasserted by the PHY when both the transmit and receive media are idle. The PHY shall ensure that CRS remains asserted throughout the duration of a collision condition.

CRS is not required to transition synchronously with respect to either the TX_CLK or the RX_CLK.

The behavior of the CRS signal is unspecified when the duplex mode bit 0.8 in the control register is set to a logic one, as described in 22.2.4.1.8, or when the Auto-Negotiation process selects a full duplex mode of operation.

Figure 22–4 shows the behavior of CRS during a frame transmission without a collision, while Figure 22–11 shows the behavior of CRS during a frame transmission with a collision.

22.2.2.12 COL (collision detected)

COL shall be asserted by the PHY upon detection of a collision on the medium, and shall remain asserted while the collision condition persists.

COL shall be asserted by a PHY that is operating at 10 Mb/s in response to a *signal_quality_error* message from the PMA.

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COL is not required to transition synchronously with respect to either the TX_CLK or the RX_CLK.

The behavior of the COL signal is unspecified when the duplex mode bit 0.8 in the control register is set to a logic one, as described in 22.2.4.1.8, or when the Auto-Negotiation process selects a full duplex mode of operation.

Figure 22–11 shows the behavior of COL during a frame transmission with a collision.

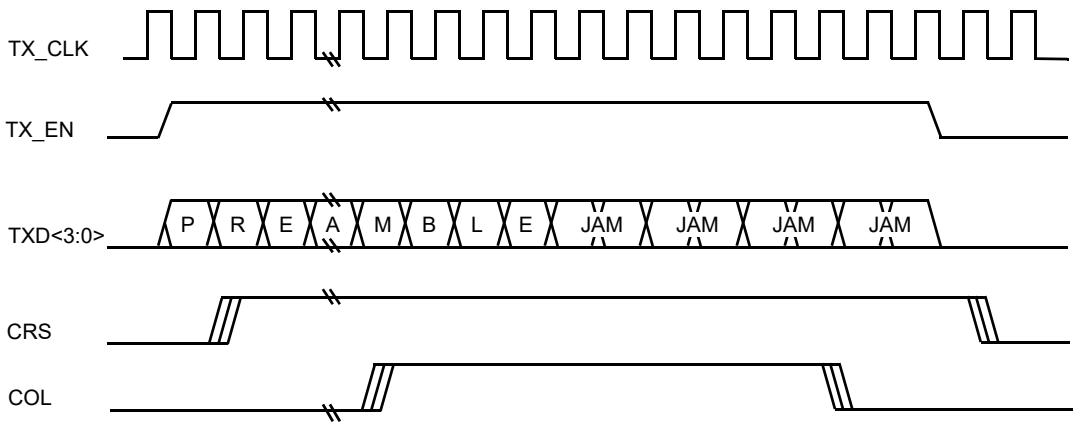

Figure 22–11—Transmission with collision

NOTE—The circuit assembly that contains the Reconciliation sublayer may incorporate a weak pull-up on the COL signal as a means of detecting an open circuit condition on the COL signal at the MII. The limit on the value of this pull-up is defined in 22.4.4.2.

22.2.2.13 MDC (management data clock)

MDC is sourced by the station management entity to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal that has no maximum high or low times. The minimum high and low times for MDC shall be 160 ns each, and the minimum period for MDC shall be 400 ns, regardless of the nominal period of TX_CLK and RX_CLK.

22.2.2.14 MDIO (management data input/output)

MDIO is a bidirectional signal between the PHY and the STA. It is used to transfer control information and status between the PHY and the STA. Control information is driven by the STA synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the STA.

MDIO shall be driven through three-state circuits that enable either the STA or the PHY to drive the signal. A PHY that is attached to the MII via the mechanical interface specified in 22.6 shall provide a resistive pull-up to maintain the signal in a high state. The STA shall incorporate a resistive pull-down on the MDIO signal and thus may use the quiescent state of MDIO to determine if a PHY is connected to the MII via the mechanical interface defined in 22.6. The limits on the values of these pull-ups and pull-downs are defined in 22.4.4.2.

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22.2.3 MII data stream

Packets transmitted through the MII shall have the format shown in Figure 22–12.

<inter-frame><preamble><sfd><data><efd>

Figure 22–12—MII data stream

For the MII, transmission and reception of each octet of data shall be done a nibble at a time with the order of nibble transmission and reception as shown in Figure 22–13.

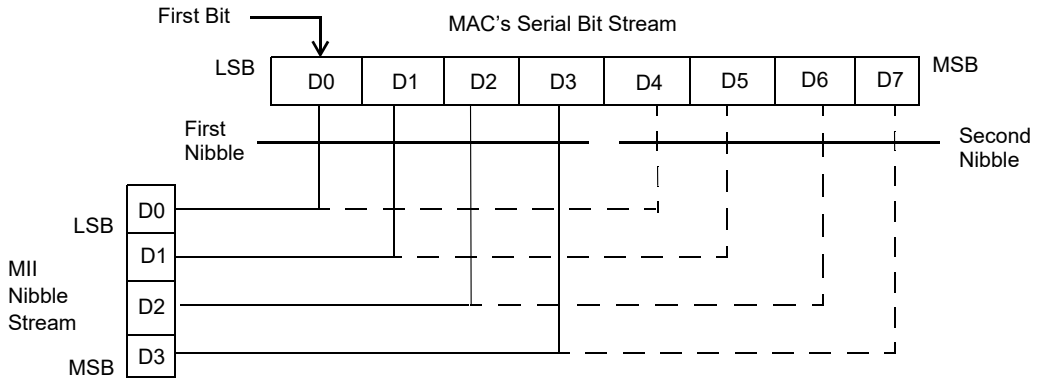

Figure 22–13—Octet/nibble transmit and receive order

The bits of each octet are transmitted and received as two nibbles, bits 0 through 3 of the octet corresponding to bits 0 through 3 of the first nibble transmitted or received, and bits 4 through 7 of the octet corresponding to bits 0 through 3 of the second nibble transmitted or received.

22.2.3.1 Inter-frame

The inter-frame period provides an observation window for an unspecified amount of time during which no data activity occurs on the MII. The absence of data activity is indicated by the deassertion of the RX_DV signal on the receive path, and the deassertion of the TX_EN signal on the transmit path. The MAC interFrameSpacing parameter defined in Clause 4 is measured from the deassertion of the CRS signal to the assertion of the CRS signal.

22.2.3.2 Preamble and start of frame delimiter

22.2.3.2.1 Transmit case

The preamble <preamble> begins a frame transmission. The bit value of the preamble field at the MII is unchanged from that specified in 7.2.3.2 and shall consist of 7 octets with the following bit values:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

In the preceding example, the preamble is displayed using the bit order it would have if transmitted serially. This means that for each octet the leftmost l value represents the LSB of the octet, and the rightmost 0 value the octet MSB.

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The SFD (Start Frame Delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value of the SFD at the MII is unchanged from that specified in 7.2.3.3 and is the bit sequence:

10101011

The preamble and SFD shall be transmitted through the MII as nibbles starting from the assertion of TX_EN as shown in Table 22–3.

Table 22–3—Transmitted preamble and SFD

Signal	Bit values of nibbles transmitted through MII																		
TXD0	X	1[a]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[b]	1	D0[c]	D4[d]
TXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[a]1st preamble nibble transmitted.
[b]1st SFD nibble transmitted.
[c]1st data nibble transmitted.
[d]D0 through D7 are the first eight bits of the data field from the Protocol Data Unit (PDU).

22.2.3.2.2 Receive case

The conditions for assertion of RX_DV are defined in 22.2.2.7.

The alignment of the received SFD and data at the MII shall be as shown in Table 22–4 and Table 22–5. Table 22–4 depicts the case where no preamble nibbles are conveyed across the MII, and Table 22–5 depicts the case where the entire preamble is conveyed across the MII.

Table 22–4—Start of receive with no preamble preceding SFD

Signal	Bit values of nibbles received through MII										
RXD0	X	X	X	X	X	X	X	1[a]	1	D0[b]	D4[c]
RXD1	X	X	X	X	X	X	X	0	0	D1	D5
RXD2	X	X	X	X	X	X	X	1	1	D2	D6
RXD3	X	X	X	X	X	X	X	0	1	D3	D7
RX_DV	0	0	0	0	0	0	0	1	1	1	1

[a]1st SFD nibble received.
[b]1st data nibble received.
[c]D0 through D7 are the first eight bits of the data field from the PDU.

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Table 22–5—Start of receive with entire preamble preceding SFD

Signal	Bit values of nibbles received through MII																		
RXD0	X	1[a]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[b]	1	D0[c]	D4[d]
RXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
RXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
RXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
RX_DV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[a]1st preamble nibble received.
[b]1st SFD nibble received.
[c]1st data nibble received.
[d]D0 through D7 are the first eight bits of the data field from the PDU.

22.2.3.3 Data

The data in a well formed frame shall consist of N octets of data transmitted as 2N nibbles. For each octet of data the transmit order of each nibble is as specified in Figure 22–13. Data in a collision fragment may consist of an odd number of nibbles.

22.2.3.4 End-of-Frame delimiter (EFD)

Deassertion of the TX_EN signal constitutes an End-of-Frame delimiter for data conveyed on TXD<3:0>, and deassertion of RX_DV constitutes an End-of-Frame delimiter for data conveyed on RXD<3:0>.

22.2.3.5 Handling of excess nibbles

An excess nibble condition occurs when an odd number of nibbles is conveyed across the MII beginning with the SFD and including all nibbles conveyed until the End-of-Frame delimiter. Reception of a frame containing a non-integer number of octets shall be indicated by the PHY as an excess nibble condition.

Transmission of an excess nibble may be handled by the PHY in an implementation-specific manner. No assumption should be made with regard to truncation, octet padding, or exact nibble transmission by the PHY.

22.2.4 Management functions

The management interface specified here provides a simple, two-wire, serial interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY. This interface is referred to as the MII Management Interface.

The MII Management Interface consists of a pair of signals that physically transport the management information across the MII or GMII, a frame format and a protocol specification for exchanging management frames, and a register set that can be read and written using these frames. The register definition specifies a basic register set with an extension mechanism. The MII uses two basic registers. The GMII also uses the same two basic registers and adds a third basic register.

The MII basic register set consists of two registers referred to as the Control register (register 0) and the Status register (register 1). All PHYs that provide an MII Management Interface shall incorporate the basic register set. All PHYs that provide a GMII shall incorporate an extended basic register set consisting of the Control register (register 0), Status register (register 1), and Extended Status register (register 15). The status

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and control functions defined here are considered basic and fundamental to 100 Mb/s and 1000 Mb/s PHYs. Registers 2 through 14 are part of the extended register set. The format of registers 4 through 10 are defined for the specific Auto-Negotiation protocol used (Clause 28 or Clause 37). The format of these registers is selected by the bit settings of registers 1 and 15.

The full set of management registers is listed in Table 22–6.

Table 22–6—MII management register set

Register address	Register name	Basic/Extended	
		MII	GMII
0	Control	B	B
1	Status	B	B
2,3	PHY Identifier	E	E
4	Auto-Negotiation Advertisement	E	E
5	Auto-Negotiation Link Partner Base Page Ability	E	E
6	Auto-Negotiation Expansion	E	E
7	Auto-Negotiation Next Page Transmit	E	E
8	Auto-Negotiation Link Partner Received Next Page	E	E
9	MASTER-SLAVE Control Register	E	E
10	MASTER-SLAVE Status Register	E	E
11	PSE Control register	E	E
12	PSE Status register	E	E
13	MMD Access Control Register	E	E
14	MMD Access Address Data Register	E	E
15	Extended Status	Reserved	B
16 through 31	Vendor Specific	E	E

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

22.2.4.1 Control register (Register 0)

The assignment of bits in the Control Register is shown in Table 22–7. The default value for each bit of the Control Register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

22.2.4.1.1 Reset

Resetting a PHY is accomplished by setting bit 0.15 to a logic one. This action shall set the status and control registers to their default states. As a consequence this action may change the internal state of the PHY and the state of the physical link associated with the PHY. This bit is self-clearing, and a PHY shall return a value of one in bit 0.15 until the reset process is completed. A PHY is not required to accept a write transaction to the control register until the reset process is completed, and writes to bits of the control register other than 0.15 may have no effect until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 0.15.

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Table 22–7—Control register bit definitions

Bit(s)	Name	Description	R/W[a]
0.15	Reset	1 = PHY reset 0 = normal operation	R/W SC
0.14	Loopback	1 = enable loopback mode 0 = disable loopback mode	R/W
0.13	Speed Selection (LSB)	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
0.12	Auto-Negotiation Enable	1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	R/W
0.11	Power Down	1 = power down 0 = normal operation[b]	R/W
0.10	Isolate	1 = electrically Isolate PHY from MII or GMII 0 = normal operation[b]	R/W
0.9	Restart Auto-Negotiation	1 = restart Auto-Negotiation process 0 = normal operation	R/W SC
0.8	Duplex Mode	1 = full duplex 0 = half duplex	R/W
0.7	Collision Test	1 = enable COL signal test 0 = disable COL signal test	R/W
0.6	Speed Selection (MSB)	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
0.5	Unidirectional enable	When bit 0.12 is one or bit 0.8 is zero, this bit is ignored. When bit 0.12 is zero and bit 0.8 is one: 1 = Enable transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established 0 = Enable transmit from media independent interface only when the PHY has determined that a valid link has been established	R/W
0.4:0	Reserved	Write as 0, ignore on read	R/W

[a]R/W = Read/Write, SC = Self-clearing.
[b]For normal operation, both 0.10 and 0.11 have to be cleared to zero; see 22.2.4.1.5.

The default value of bit 0.15 is zero.

NOTE—This operation may interrupt data communication.

22.2.4.1.2 Loopback

The PHY shall be placed in a loopback mode of operation when bit 0.14 is set to a logic one. When bit 0.14 is set, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII or GMII shall not result in the transmission of data on the network medium. When bit 0.14 is set, the

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PHY shall accept data from the MII or GMII transmit data path and return it to the MII or GMII receive data path in response to the assertion of TX_EN. When bit 0.14 is set, the delay from the assertion of TX_EN to the assertion of RX_DV shall be less than 512 BT. When bit 0.14 is set, the COL signal shall remain deasserted at all times, unless bit 0.7 is set, in which case the COL signal shall behave as described in 22.2.4.1.9. Clearing bit 0.14 to zero allows normal operation.

The default value of bit 0.14 is zero.

NOTE—The signal path through the PHY that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PHY circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths through a PHY may be enabled via the extended register set, in an implementation-specific fashion.

22.2.4.1.3 Speed selection

Link speed can be selected via either the Auto-Negotiation process, or manual speed selection. Manual speed selection is allowed when Auto-Negotiation is disabled by clearing bit 0.12 to zero. When Auto-Negotiation is disabled and bit 0.6 is cleared to a logic zero, setting bit 0.13 to a logic one configures the PHY for 100 Mb/s operation, and clearing bit 0.13 to a logic zero configures the PHY for 10 Mb/s operation. When Auto-Negotiation is disabled and bit 0.6 is set to a logic one, clearing bit 0.13 to a logic zero selects 1000 Mb/s operation. The combination of both bits 0.6 and 0.13 set to a logic one is reserved for future standardization. When Auto-Negotiation is enabled, bits 0.6 and 0.13 can be read or written, but the state of bits 0.6 and 0.13 have no effect on the link configuration, and it is not necessary for bits 0.6 and 0.13 to reflect the operating speed of the link when it is read. If a PHY reports via bits 1.15:9 and bits 15.15:12 that it is not able to operate at all speeds, the value of bits 0.6 and 0.13 shall correspond to a speed at which the PHY can operate, and any attempt to change the bits to an invalid setting shall be ignored.

The default value of bits 0.6 and 0.13 are the encoding of the highest data rate at which the PHY can operate as indicated by bits 1.15:9 and 15.15:12.

22.2.4.1.4 Auto-Negotiation enable

The Auto-Negotiation process shall be enabled by setting bit 0.12 to a logic one. If bit 0.12 is set to a logic one, then bits 0.13, 0.8, and 0.6 shall have no effect on the link configuration, and station operation other than that specified by the Auto-Negotiation protocol. If bit 0.12 is cleared to a logic zero, then bits 0.13, 0.8, and 0.6 will determine the link configuration, regardless of the prior state of the link configuration and the Auto-Negotiation process.

If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, the PHY shall return a value of zero in bit 0.12. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, bit 0.12 should always be written as zero, and any attempt to write a one to bit 0.12 shall be ignored.

The default value of bit 0.12 is one, unless the PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, in which case the default value of bit 0.12 is zero.

22.2.4.1.5 Power down

The PHY may be placed in a low-power consumption state by setting bit 0.11 to a logic one. Clearing bit 0.11 to zero allows normal operation. The specific behavior of a PHY in the power-down state is implementation specific. While in the power-down state, the PHY shall respond to management transactions. During the transition to the power-down state and while in the power-down state, the PHY shall not generate spurious signals on the MII or GMII.

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A PHY is not required to meet the RX_CLK and TX_CLK signal functional requirements when either bit 0.11 or bit 0.10 is set to a logic one. A PHY shall meet the RX_CLK and TX_CLK signal functional requirements defined in 22.2.2 within 0.5 s after both bit 0.11 and 0.10 are cleared to zero.

The default value of bit 0.11 is zero.

22.2.4.1.6 Isolate

The PHY may be forced to electrically isolate its data paths from the MII or GMII by setting bit 0.10 to a logic one. Clearing bit 0.10 allows normal operation. When the PHY is isolated from the MII or GMII it shall not respond to the TXD data bundle, TX_EN, TX_ER and GTX_CLK inputs, and it shall present a high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RXD data bundle, COL, and CRS outputs. When the PHY is isolated from the MII or GMII it shall respond to management transactions.

A PHY that is connected to the MII via the mechanical interface defined in 22.6 shall have a default value of one for bit 0.10 so as to avoid the possibility of having multiple MII output drivers actively driving the same signal path simultaneously.

NOTE—This clause neither requires nor assumes any specific behavior at the MDI resulting from setting bit 0.10 to a logic one.

22.2.4.1.7 Restart Auto-Negotiation

If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the PHY shall return a value of zero in bit 0.9. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, bit 0.9 should always be written as zero, and any attempt to write a one to bit 0.9 shall be ignored.

Otherwise, the Auto-Negotiation process shall be restarted by setting bit 0.9 to a logic one. This bit is self-clearing, and a PHY shall return a value of one in bit 0.9 until the Auto-Negotiation process has been initiated. The Auto-Negotiation process shall not be affected by writing a zero to bit 0.9.

The default value of bit 0.9 is zero.

22.2.4.1.8 Duplex mode

The duplex mode can be selected via either the Auto-Negotiation process, or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by clearing bit 0.12 to zero. When Auto-Negotiation is disabled, setting bit 0.8 to a logic one configures the PHY for full duplex operation, and clearing bit 0.8 to a logic zero configures the PHY for half duplex operation. When Auto-Negotiation is enabled, bit 0.8 can be read or written, but the state of bit 0.8 has no effect on the link configuration. If a PHY reports via bits 1.15:9 and 15.15:12 that it is able to operate in only one duplex mode, the value of bit 0.8 shall correspond to the mode in which the PHY can operate, and any attempt to change the setting of bit 0.8 shall be ignored.

When a PHY is placed in the loopback mode of operation via bit 0.14, the behavior of the PHY shall not be affected by the state of bit 0.8.

The default value of bit 0.8 is zero, unless a PHY reports via bits 1.15:9 and 15.15:12 that it is able to operate only in full duplex mode, in which case the default value of bit 0.8 is one.

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22.2.4.1.9 Collision test

The COL signal at the MII or GMII may be tested by setting bit 0.7 to a logic one. When bit 0.7 is set to one, the PHY shall assert the COL signal within 512 BT in response to the assertion of TX_EN. While bit 0.7 is set to one, the PHY shall deassert the COL signal within 4 BT when connected to an MII, or 16 BT when connected to a GMII, in response to the deassertion of TX_EN. Clearing bit 0.7 to zero allows normal operation.

The default value of bit 0.7 is zero.

NOTE—It is recommended that the Collision Test function be used only in conjunction with the loopback mode of operation defined in 22.2.4.1.2.

22.2.4.1.10 Speed selection

Bit 0.6 is used in conjunction with bits 0.13 and 0.12 to select the speed of operation as described in 22.2.4.1.3.

22.2.4.1.11 Reserved bits

Bits 0.4:0 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

22.2.4.1.12 Unidirectional enable

If a PHY reports via bit 1.7 that it lacks the ability to encode and transmit data from the media independent interface regardless of whether the PHY has determined that a valid link has been established, the PHY shall return a value of zero in bit 0.5, and any attempt to write a one to bit 0.5 shall be ignored.

The ability to encode and transmit data from the media independent interface regardless of whether the PHY has determined that a valid link has been established is controlled by bit 0.5 as well as the status of Auto-Negotiation Enable bit 0.12 and the Duplex Mode bit 0.8 as this ability can only be supported if Auto-Negotiation is disabled and the PHY is operating in full-duplex mode. If bit 0.5 is set to a logic one, bit 0.12 to logic zero and bit 0.8 to logic one, encoding and transmitting data from the media independent interface shall be enabled regardless of whether the PHY has determined that a valid link has been established. If bit 0.5 is set to a logic zero, bit 0.12 to logic one or bit 0.8 to logic zero, encoding and transmitting data from the media independent interface shall be dependent on whether the PHY has determined that a valid link has been established. When bit 0.12 is one or bit 0.8 is zero, bit 0.5 shall be ignored.

A management entity shall set bit 0.5 to a logic one only after it has enabled an associated OAM sublayer (see Clause 57) or if this device is a 1000BASE-PX-D PHY. A management entity shall clear bit 0.5 to a logic zero prior to it disabling an associated OAM sublayer when this device is not a 1000BASE-PX-D PHY. To avoid collisions, a management entity should not set bit 0.5 of a 1000BASE-PX-U PHY to a logic one.

The default value of bit 0.5 is zero, except for 1000BASE-PX-D, where it is one.

22.2.4.2 Status register (Register 1)

The assignment of bits in the Status register is shown in Table 22–8. All of the bits in the Status register are read only, a write to the Status register shall have no effect.

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Table 22–8—Status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO
1.14	100BASE-X Full Duplex	1 = PHY able to perform full duplex 100BASE-X 0 = PHY not able to perform full duplex 100BASE-X	RO
1.13	100BASE-X Half Duplex	1 = PHY able to perform half duplex 100BASE-X 0 = PHY not able to perform half duplex 100BASE-X	RO
1.12	10 Mb/s Full Duplex	1 = PHY able to operate at 10 Mb/s in full duplex mode 0 = PHY not able to operate at 10 Mb/s in full duplex mode	RO
1.11	10 Mb/s Half Duplex	1 = PHY able to operate at 10 Mb/s in half duplex mode 0 = PHY not able to operate at 10 Mb/s in half duplex mode	RO
1.10	100BASE-T2 Full Duplex	1 = PHY able to perform full duplex 100BASE-T2 0 = PHY not able to perform full duplex 100BASE-T2	RO
1.9	100BASE-T2 Half Duplex	1 = PHY able to perform half duplex 100BASE-T2 0 = PHY not able to perform half duplex 100BASE-T2	RO
1.8	Extended Status	1 = Extended status information in register 15 0 = No extended status information in register 15	RO
1.7	Unidirectional ability	1 = PHY able to transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established 0 = PHY able to transmit from media independent interface only when the PHY has determined that a valid link has been established	RO
1.6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed	RO
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
1.4	Remote Fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO/ LH
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
1.2	Link Status	1 = link is up 0 = link is down	RO/ LL
1.1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	RO/ LH
1.0	Extended Capability	1 = extended register capabilities 0 = basic register set capabilities only	RO

[a]RO = Read only, LL = Latching low, LH = Latching high

22.2.4.2.1 100BASE-T4 ability

When read as a logic one, bit 1.15 indicates that the PHY has the ability to perform link transmission and reception using the 100BASE-T4 signaling specification. When read as a logic zero, bit 1.15 indicates that the PHY lacks the ability to perform link transmission and reception using the 100BASE-T4 signaling specification.

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22.2.4.2.2 100BASE-X full duplex ability

When read as a logic one, bit 1.14 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 100BASE-X signaling specification. When read as a logic zero, bit 1.14 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 100BASE-X signaling specification.

22.2.4.2.3 100BASE-X half duplex ability

When read as a logic one, bit 1.13 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 100BASE-X signaling specification. When read as a logic zero, bit 1.13 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 100BASE-X signaling specification.

22.2.4.2.4 10 Mb/s full duplex ability

When read as a logic one, bit 1.12 indicates that the PHY has the ability to perform full duplex link transmission and reception while operating at 10 Mb/s. When read as a logic zero, bit 1.12 indicates that the PHY lacks the ability to perform full duplex link transmission and reception while operating at 10 Mb/s.

22.2.4.2.5 10 Mb/s half duplex ability

When read as a logic one, bit 1.11 indicates that the PHY has the ability to perform half duplex link transmission and reception while operating at 10 Mb/s. When read as a logic zero, bit 1.11 indicates that the PHY lacks the ability to perform half duplex link transmission and reception while operating at 10 Mb/s.

22.2.4.2.6 100BASE-T2 full duplex ability

When read as a logic one, bit 1.10 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 100BASE-T2 signaling specification. When read as a logic zero, bit 1.10 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 100BASE-T2 signaling specification.

22.2.4.2.7 100BASE-T2 half duplex ability

When read as a logic one, bit 1.9 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 100BASE-T2 signaling specification. When read as a logic zero, bit 1.9 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 100BASE-T2 signaling specification.

22.2.4.2.8 Unidirectional ability

When read as a logic one, bit 1.7 indicates that the PHY has the ability to encode and transmit data from the media independent interface regardless of whether the PHY has determined that a valid link has been established. When read as a logic zero, bit 1.7 indicates the PHY is able to transmit data from the media independent interface only when the PHY has determined that a valid link has been established.

A PHY shall return a value of zero in bit 1.7 if it is not a 100BASE-X PHY using the PCS and PMA specified in 66.1 or a 1000BASE-X PHY using the PCS and PMA specified in 66.2.

22.2.4.2.9 MF preamble suppression ability

When read as a logic one, bit 1.6 indicates that the PHY is able to accept management frames regardless of whether they are or are not preceded by the preamble pattern described in 22.2.4.5.2. When read as a logic

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zero, bit 1.6 indicates that the PHY is not able to accept management frames unless they are preceded by the preamble pattern described in 22.2.4.5.2.

22.2.4.2.10 Auto-Negotiation complete

When read as a logic one, bit 1.5 indicates that the Auto-Negotiation process has been completed, and that the contents of the extended registers implemented by the Auto-Negotiation protocol (either Clause 28 or Clause 37) are valid. When read as a logic zero, bit 1.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of the extended registers are as defined by the current state of the Auto-Negotiation protocol, or as written for manual configuration. A PHY shall return a value of zero in bit 1.5 if Auto-Negotiation is disabled by clearing bit 0.12. A PHY shall also return a value of zero in bit 1.5 if it lacks the ability to perform Auto-Negotiation.

22.2.4.2.11 Remote fault

When read as a logic one, bit 1.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The Remote Fault bit shall be implemented with a latching function, such that the occurrence of a remote fault will cause the Remote Fault bit to become set and remain set until it is cleared. The Remote Fault bit shall be cleared each time register 1 is read via the management interface, and shall also be cleared by a PHY reset.

If a PHY has no provision for remote fault detection, it shall maintain bit 1.4 in a cleared state. Further information regarding the remote fault indication can be found in 37.2.1.5, 22.2.1.2, and 24.3.2.1.

22.2.4.2.12 Auto-Negotiation ability

When read as a logic one, bit 1.3 indicates that the PHY has the ability to perform Auto-Negotiation. When read as a logic zero, bit 1.3 indicates that the PHY lacks the ability to perform Auto-Negotiation.

22.2.4.2.13 Link Status

When read as a logic one, bit 1.2 indicates that the PHY has determined that a valid link has been established. When read as a logic zero, bit 1.2 indicates that the link is not valid. The criteria for determining link validity is PHY specific. The Link Status bit shall be implemented with a latching function, such that the occurrence of a link failure condition will cause the Link Status bit to become cleared and remain cleared until it is read via the management interface. This status indication is intended to support the management attribute defined in 30.5.1.1.4, aMediaAvailable.

22.2.4.2.14 Jabber detect

When read as a logic one, bit 1.1 indicates that a jabber condition has been detected. This status indication is intended to support the management attribute defined in 30.5.1.1.6, aJabber, and the MAU notification defined in 30.5.1.3.1, nJabber. The criteria for the detection of a jabber condition is PHY specific. The Jabber Detect bit shall be implemented with a latching function, such that the occurrence of a jabber condition will cause the Jabber Detect bit to become set and remain set until it is cleared. The Jabber Detect bit shall be cleared each time register 1 is read via the management interface, and shall also be cleared by a PHY reset.

PHYs specified for 100 Mb/s operation or above do not incorporate a Jabber Detect function, as this function is defined to be performed in the repeater unit at these speeds. Therefore, PHYs specified for 100 Mb/s operation and above shall always return a value of zero in bit 1.1.

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22.2.4.2.15 Extended capability

When read as a logic one, bit 1.0 indicates that the PHY provides an extended set of capabilities which may be accessed through the extended register set. When read as a logic zero, bit 1.0 indicates that the PHY provides only the basic register set.

22.2.4.2.16 Extended status

When read as a logic one, bit 1.8 indicates that the base register status information is extended into register 15. All PHYs supporting 1000 Mb/s operation shall have this bit set to a logic one. When read as a logic zero, bit 1.8 indicates that the extended status is not implemented.

22.2.4.3 Extended capability registers

In addition to the basic register set defined in 22.2.4.1 and 22.2.4.2, PHYs may provide an extended set of capabilities that may be accessed and controlled via the MII management interface. Thirteen registers have been defined within the extended address space for the purpose of providing a PHY-specific identifier to layer management, to provide control and monitoring for the Auto-Negotiation process, and to provide control and monitoring of power sourcing equipment, and to provide MDIO Manageable Device (MMD) register access.

If an attempt is made to perform a read transaction to a register in the extended register set, and the PHY being read does not implement the addressed register, the PHY shall not drive the MDIO line in response to the read transaction. If an attempt is made to perform a write transaction to a register in the extended register set, and the PHY being written does not implement the addressed register, the write transaction shall be ignored by the PHY.

22.2.4.3.1 PHY Identifier (Registers 2 and 3)

Registers 2 and 3 provide a 32-bit value, which shall constitute a unique identifier for a particular type of PHY. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier.

Bit 2.15 shall be the MSB of the PHY Identifier, and bit 3.0 shall be the LSB of the PHY Identifier.

The PHY Identifier shall be composed of the third through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the PHY manufacturer by the IEEE,[53] plus a six-bit manufacturer's model number, plus a four-bit manufacturer's revision number. The PHY Identifier is intended to provide sufficient information to support the oResourceTypeID object as required in 30.1.2.

The third bit of the OUI is assigned to bit 2.15, the fourth bit of the OUI is assigned to bit 2.14, and so on. Bit 2.0 contains the eighteenth bit of the OUI. Bit 3.15 contains the nineteenth bit of the OUI, and bit 3.10 contains the twenty-fourth bit of the OUI. Bit 3.9 contains the MSB of the manufacturer's model number. Bit 3.4 contains the LSB of the manufacturer's model number. Bit 3.3 contains the MSB of the manufacturer's revision number, and bit 3.0 contains the LSB of the manufacturer's revision number.

NOTE—The use of only 22 bits of the OUI as described here has been deprecated by the IEEE Registration Authority. In this case, Company ID (CID) is not an acceptable alternative to OUI due to the possibility that a CID and OUI could be identical in the 22-bit subset. The definition of vendor-specific device identifiers for other applications is expected to use the full 24 bits to accommodate the use of either an OUI or CID.

[53]Interested applicants should contact the IEEE Standards Department, Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854, USA.

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Figure 22–14 depicts the mapping of this information to the bits of registers 2 and 3. Additional detail describing the format of OUIs can be found in IEEE Std 802.

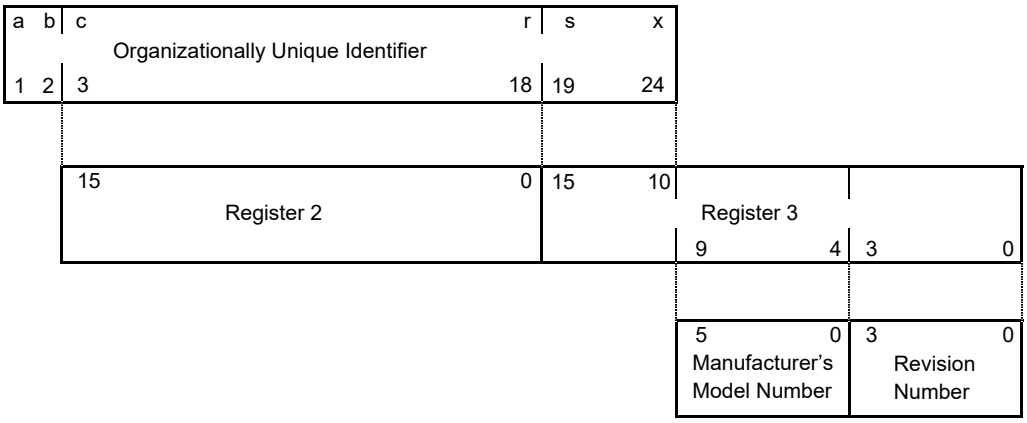

Figure 22–14—Format of PHY Identifier

22.2.4.3.2 Auto-Negotiation advertisement (Register 4)

Register 4 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.3 Auto-Negotiation link partner ability (Register 5)

Register 5 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.4 Auto-Negotiation expansion (Register 6)

Register 6 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.5 Auto-Negotiation Next Page (Register 7)

Register 7 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.6 Auto-Negotiation link partner Received Next Page (Register 8)

Register 8 provides 16 bits that are used by the Auto-Negotiation process. See 32.5.1 and 37.2.5.1.

22.2.4.3.7 MASTER-SLAVE control register (Register 9)

Register 9 provides bit values by 100BASE-T2 (as specified in 32.5) and 1000BASE-T (as specified in 40.5).

22.2.4.3.8 MASTER-SLAVE status register (Register 10)

Register 10 provides bit values by 100BASE-T2 (as specified in 32.5) and 1000BASE-T (as specified in 40.5).

22.2.4.3.9 PSE Control register (Register 11)

Register 11 provides control bits that are used by a PSE. See 33.5.1.1.

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22.2.4.3.10 PSE Status register (Register 12)

Register 12 provides status bits that are supplied by a PSE. See 33.5.1.2.

22.2.4.3.11 MMD access control register (Register 13)

The assignment of bits in the MMD access control register is shown in Table 22–9. The MMD access control register is used in conjunction with the MMD access address data register (register 14) to provide access to the MMD address space using the interface and mechanisms defined in 22.2.4.

Table 22–9—MMD access control register bit definitions

Bit(s)	Name	Description	R/W[a]
13.15:14	Function	13.1513.14 00= address 01= data, no post increment 10= data, post increment on reads and writes 11= data, post increment on writes only	R/W
13.13:5	Reserved	Write as 0, ignore on read	R/W
13.4:0	DEVAD	Device address	R/W

[a]R/W = Read/Write

Each MMD maintains its own individual address register as described in 45.2.10. The DEVAD field directs any accesses of register 14 to the appropriate MMD as described in 45.2. If the access of register 14 is an address access (bits 13.15:14 = 00) then it is directed to the address register within the MMD associated with the value in the DEVAD field (bits 13.4:0). Otherwise, both the DEVAD field and that MMD's address register direct the register 14 data accesses to the appropriate registers within that MMD.

The Function field can be set to any of four values:

a) When set to 00, accesses to register 14 access the MMD's individual address register. This address register should always be initialized before attempting any accesses to other MMD registers.
b) When set to 01, accesses to register 14 access the register within the MMD selected by the value in the MMD's address register.
c) When set to 10, accesses to register 14 access the register within the MMD selected by the value in the MMD's address register. After that access is complete, for both read and write accesses, the value in the MMD's address field is incremented.
d) When set to 11, accesses to register 14 access the register within the MMD selected by the value in the MMD's address register. After that access is complete, for write accesses only, the value in the MMD's address field is incremented. For read accesses, the value in the MMD's address field is not modified.

For additional insight into the operation and usage of this register, see Annex 22D.

22.2.4.3.12 MMD access address data register (Register 14)

The assignment of bits in the MMD access address data register is shown in Table 22–10. The MMD access address data register is used in conjunction with the MMD access control register (register 13) to provide access to the MMD address space using the interface and mechanisms defined in 22.2.4. Accesses to this

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register are controlled by the value of the fields in register 13 and the contents of the MMD's individual address field as described in 22.2.4.3.11.

Table 22–10—MMD access address data register bit definitions

Bit(s)	Name	Description	R/W[a]
14.15:0	Address Data	If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register	R/W

[a]R/W = Read/Write

For additional insight into the operation and usage of this register, see Annex 22D.

22.2.4.3.13 PHY specific registers

A particular PHY may provide additional registers beyond those defined above. Register addresses 16 through 31 (decimal) may be used to provide vendor-specific functions or abilities. The definition of registers 4 through 14 are dependent on the version (Clause 28 or Clause 37) of Auto-Negotiation protocol used by the PHY.

22.2.4.4 Extended Status register (Register 15)

The Extended Status register is implemented for 1000BASE-T PHYs and all PHYs using the 1000BASE-X signaling specifications. The assignment of bits in the Extended Status register is shown in Table 22–11. All of the bits in the Extended Status register are read only; a write to the Extended Status register shall have no effect.

Table 22–11—Extended Status register bit definitions

Bit(s)	Name	Description	R/W[a]
15.15	1000BASE-X Full Duplex	1 = PHY able to perform full duplex 1000BASE-X 0 = PHY not able to perform full duplex 1000BASE-X	RO
15.14	1000BASE-X Half Duplex	1 = PHY able to perform half duplex 1000BASE-X 0 = PHY not able to perform half duplex 1000BASE-X	RO
15.13	1000BASE-T Full Duplex	1 = PHY able to perform full duplex 1000BASE-T 0 = PHY not able to perform full duplex 1000BASE-T	RO
15.12	1000BASE-T Half Duplex	1 = PHY able to perform half duplex 1000BASE-T 0 = PHY not able to perform half duplex 1000BASE-T	RO
15.11:0	Reserved	Ignore when read	RO

[a]RO = Read only

22.2.4.4.1 1000BASE-X full duplex ability

When read as a logic one, bit 15.15 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 1000BASE-X signaling specification. When read as a logic zero, the

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bit 15.15 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 1000BASE-X signaling specification.

22.2.4.4.2 1000BASE-X half duplex ability

When read as a logic one, bit 15.14 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 1000BASE-X signaling specification. When read as a logic zero, the bit 15.14 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 1000BASE-X signaling specification.

22.2.4.4.3 1000BASE-T full duplex ability

When read as a logic one, bit 15.13 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 1000BASE-T signaling specification. When read as a logic zero, the bit 15.13 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 1000BASE-T signaling specification.

22.2.4.4.4 1000BASE-T half duplex ability

When read as a logic one, bit 15.12 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 1000BASE-T signaling specification. When read as a logic zero, the bit 15.12 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 1000BASE-T signaling specification.

22.2.4.4.5 Reserved bits

Bits 15:11:0 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

22.2.4.5 Management frame structure

Frames transmitted on the MII Management Interface shall have the frame structure shown in Table 22–12. The order of bit transmission shall be from left to right.

Table 22–12—Management frame format

	Management frame fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

22.2.4.5.1 IDLE (IDLE condition)

The IDLE condition on MDIO is a high-impedance state. All three state drivers shall be disabled and the PHY's pull-up resistor will pull the MDIO line to a logic one.

22.2.4.5.2 PRE (preamble)

At the beginning of each transaction, the station management entity shall send a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can

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use to establish synchronization. A PHY shall observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

If the STA determines that every PHY that is connected to the MDIO signal is able to accept management frames that are not preceded by the preamble pattern, then the STA may suppress the generation of the preamble pattern, and may initiate management frames with the ST (Start of Frame) pattern.

22.2.4.5.3 ST (start of frame)

The start of frame is indicated by a <01> pattern. This pattern assures transitions from the default logic one line state to zero and back to one.

22.2.4.5.4 OP (operation code)

The operation code for a read transaction is <10>, while the operation code for a write transaction is <01>.

22.2.4.5.5 PHYAD (PHY Address)

The PHY Address is five bits, allowing 32 unique PHY addresses. The first PHY address bit transmitted and received is the MSB of the address. A PHY that is connected to the station management entity via the mechanical interface defined in 22.6 shall always respond to transactions addressed to PHY Address zero <00000>. A station management entity that is attached to multiple PHYs has to have prior knowledge of the appropriate PHY Address for each PHY.

22.2.4.5.6 REGAD (Register Address)

The Register Address is five bits, allowing 32 individual registers to be addressed within each PHY. The first Register Address bit transmitted and received is the MSB of the address. The register accessed at Register Address zero <00000> shall be the control register defined in 22.2.4.1, and the register accessed at Register Address one <00001> shall be the status register defined in 22.2.4.2.

22.2.4.5.7 TA (turnaround)

The turnaround time is a 2 bit time spacing between the Register Address field and the Data field of a management frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY shall remain in a high-impedance state for the first bit time of the turnaround. The PHY shall drive a zero bit during the second bit time of the turnaround of a read transaction. During a write transaction, the STA shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround. Figure 22–15 shows the behavior of the MDIO signal during the turnaround field of a read transaction.

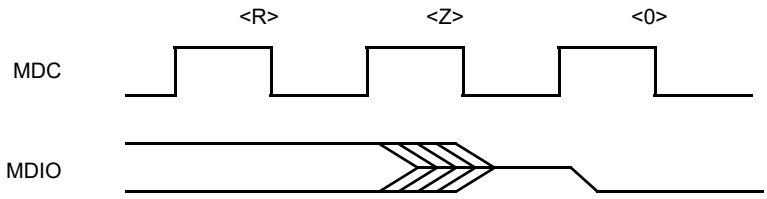

Figure 22–15—Behavior of MDIO during TA field of a read transaction

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22.2.4.5.8 DATA (data)

The data field is 16 bits. The first data bit transmitted and received shall be bit 15 of the register being addressed.

22.3 Signal timing characteristics

All signal timing characteristics shall be measured using the techniques specified in Annex 22C. The signal threshold potentials $V_{ih(min)}$ and $V_{il(max)}$ are defined in 22.4.4.1.

The HIGH time of an MII signal is defined as the length of time that the potential of the signal is greater than or equal to $V_{ih(min)}$. The LOW time of an MII signal is defined as the length of time that the potential of the signal is less than or equal to $V_{il(max)}$.

The setup time of an MII signal relative to an MII clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region. The hold time of an MII signal relative to an MII clock edge is defined as the length of time between when the clock exits the switching region and when the signal enters the switching region.

The propagation delay from an MII clock edge to a valid MII signal is defined as the length of time between when the clock exits the switching region and when the signal exits and remains out of the switching region.

22.3.1 Signals that are synchronous to TX_CLK

Figure 22–16 shows the timing relationship for the signals associated with the transmit data path at the MII connector. The clock to output delay shall be a minimum of 0 ns and a maximum of 25 ns.

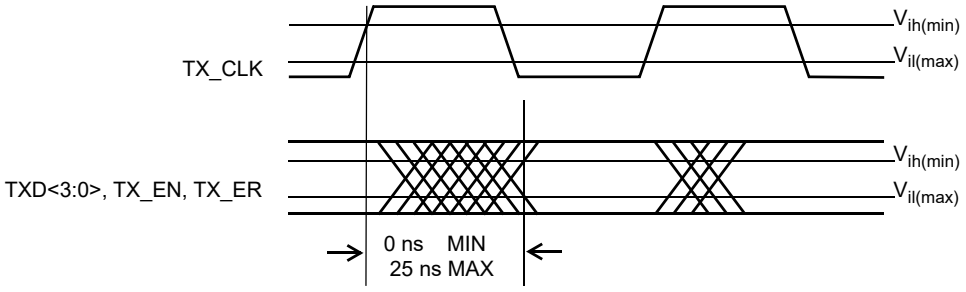

Figure 22–16—Transmit signal timing relationships at the MII

22.3.1.1 TX_EN

TX_EN is transitioned by the Reconciliation sublayer synchronously with respect to the TX_CLK rising edge with the timing as shown in Figure 22–16.

22.3.1.2 TXD<3:0>

TXD<3:0> is transitioned by the Reconciliation sublayer synchronously with respect to the TX_CLK rising edge with the timing as depicted in Figure 22–16.

22.3.1.3 TX_ER

TX_ER is transitioned synchronously with respect to the rising edge of TX_CLK as shown in Figure 22–16.

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22.3.2 Signals that are synchronous to RX_CLK

Figure 22–17 shows the timing relationship for the signals associated with the receive data path at the MII connector. The timing is referenced to the rising edge of the RX_CLK. The input setup time shall be a minimum of 10 ns and the input hold time shall be a minimum of 10 ns.

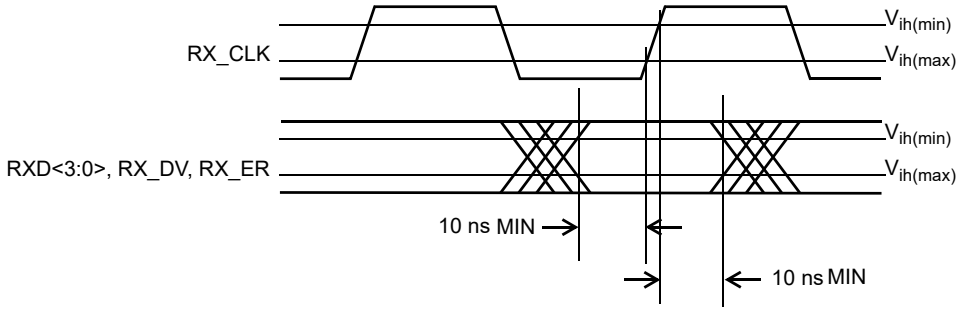

Figure 22–17—Receive signal timing relationships at the MII

22.3.2.1 RX_DV

RX_DV is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK with the timing shown in Figure 22–17.

22.3.2.2 RXD<3:0>

RXD<3:0> is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK as shown in Figure 22–17. The RXD<3:0> timing requirements have to be met at all rising edges of RX_CLK.

22.3.2.3 RX_ER

RX_ER is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK as shown in Figure 22–17. The RX_ER timing requirements have to be met at all rising edges of RX_CLK.

22.3.3 Signals that have no required clock relationship

22.3.3.1 CRS

CRS is driven by the PHY. Transitions on CRS have no required relationship to either of the clock signals provided at the MII.

22.3.3.2 COL

COL is driven by the PHY. Transitions on COL have no required relationship to either of the clock signals provided at the MII.

22.3.4 MDIO timing relationship to MDC

MDIO (Management Data Input/Output) is a bidirectional signal that can be sourced by the Station Management Entity (STA) or the PHY. When the STA sources the MDIO signal, the STA shall provide a

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minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC, as shown in Figure 22–18, measured at the MII connector.

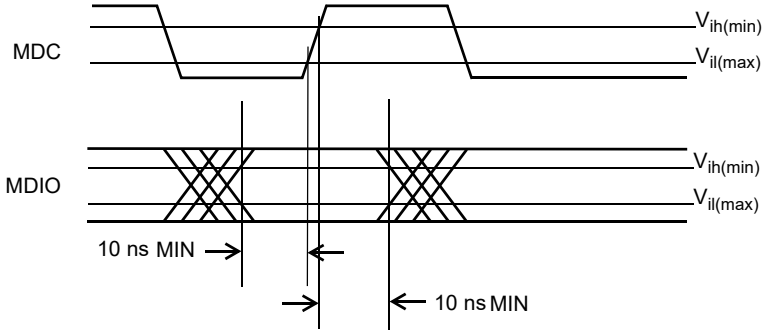

Figure 22–18—MDIO sourced by STA

When the MDIO signal is sourced by the PHY, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock to output delay from the PHY, as measured at the MII connector, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in Figure 22–19.

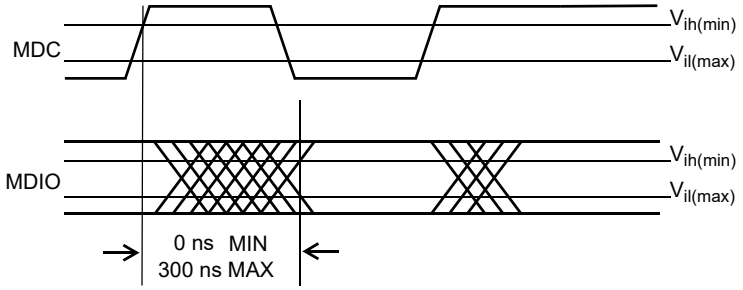

Figure 22–19—MDIO sourced by PHY

22.4 Electrical characteristics

The electrical characteristics of the MII are specified such that the three application environments described in 22.1 are accommodated. The electrical specifications are optimized for the integrated circuit to integrated circuit application environment, but integrated circuit drivers and receivers that are implemented in compliance with the specification will also support the mother board to daughter board and short cable application environments, provided those environments are constrained to the limits specified in this clause.

NOTE—The specifications for the driver and receiver characteristics can be met with TTL compatible input and output buffers implemented in a digital CMOS ASIC process.

22.4.1 Signal levels

The MII uses TTL signal levels, which are compatible with devices operating at a nominal supply voltage of either 5.0 V or 3.3 V.

NOTE—Care should be taken to ensure that all MII receivers can tolerate dc input potentials from 0.00 V to 5.50 V, referenced to the COMMON signal, and transient input potentials as high as 7.3 V, or as low as –1.8 V, referenced to the COMMON signal, which can occur when MII signals change state. The transient duration will not exceed 15 ns. The dc

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source impedance will be no less than $R_{oh(min)}$. The transient source impedance will be no less than ($68 \times 0.85 = 57.8\ \Omega$).

22.4.2 Signal paths

MII signals can be divided into two groups: signals that go between the STA and the PHY, and signals that go between the Reconciliation sublayer and the PHY.

Signals between the STA and the PHY may connect to one or more PHYs. When a signal goes between the STA and a single PHY, the signal's path is a point-to-point transmission path. When a signal goes between the STA and multiple PHYs, the signal's transmission path has drivers and receivers attached in any order along the length of the path and is not considered a point-to-point transmission path.

Signals between the Reconciliation sublayer and the PHY may also connect to one or more PHYs. However, the transmission path of each of these signals shall be either a point-to-point transmission path or a sequence of point-to-point transmission paths connected in series.

All connections to a point-to-point transmission path are at the path ends. The simplest point-to-point transmission path has a driver at one end and a receiver at the other. Point-to-point transmission paths can also have more than one driver and more than one receiver if the drivers and receivers are lumped at the ends of the path, and if the maximum propagation delay between the drivers and receivers at a given end of the path is a very small fraction of the 10%–90% rise/fall time for signals driven onto the path.

The MII shall use unbalanced signal transmission paths. The characteristic impedance Z_o of transmission paths is not specified for electrically short paths where transmission line reflections can be safely ignored.

The characteristic impedance Z_o of electrically long transmission paths or path segments shall be $68\ \Omega \pm 15\%$.

The output impedance of the driver shall be used to control transmission line reflections on all electrically long point-to-point signal paths.

NOTE—In the context of this clause, a transmission path whose round-trip propagation delay is less than half of the 10%–90% rise/fall time of signals driven onto the path is considered an electrically short transmission path.

22.4.3 Driver characteristics

The driver characteristics defined in this clause apply to all MII signal drivers. The driver characteristics are specified in terms of both their ac and dc characteristics.

NOTE—Rail-to-rail drivers that comply with the driver output V-I diagrams in Annex 22B will meet the following ac and dc characteristics.

22.4.3.1 DC characteristics

The high (one) logic level output potential V_{oh} shall be no less than 2.40 V at an output current I_{oh} of –4.0 mA. The low (zero) logic level output potential V_{ol} shall not be greater than 0.40 V at an output current I_{ol} of 4.0 mA.

22.4.3.2 AC characteristics

Drivers have to also meet certain ac specifications in order to ensure adequate signal quality for electrically long point-to-point transmission paths. The ac specifications shall guarantee the following performance requirements.

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The initial incident potential change arriving at the receiving end of a point-to-point MII signal path plus its reflection from the receiving end of the path has to switch the receiver input potential monotonically from a valid high (one) level to $V_{il} \leq V_{il(max)} - 200$ mV, or from a valid low (zero) level to $V_{ih} \geq V_{ih(min)} + 200$ mV.

Subsequent incident potential changes arriving at the receiving end of a point-to-point MII signal path plus their reflections from the receiving end of the path has to not cause the receiver input potential to reenter the range $V_{il(max)} - 200\ mV < V_i < V_{ih(min)} + 200$ mV except when switching from one valid logic level to the other. Such subsequent incident potential changes result from a mismatch between the characteristic impedance of the signal path and the driver output impedance.

22.4.4 Receiver characteristics

The receiver characteristics are specified in terms of the threshold levels for the logical high (one) and logical low (zero) states. In addition, receivers have to meet the input current and capacitance limits.

22.4.4.1 Voltage thresholds

An input potential V_i of 2.00 V or greater shall be interpreted by the receiver as a logical high (one). Thus, $V_{ih(min)} = 2.00$ V. An input potential V_i of 0.80 V or less shall be interpreted by the receiver as a logical low (zero). Thus, $V_{il(max)} = 0.80$ V. The switching region is defined as signal potentials greater than $V_{il(max)}$ and less than $V_{ih(min)}$. When the input signal potential is in the switching region, the receiver output is undefined.

22.4.4.2 Input current

The input current requirements shall be measured at the MII connector and shall be referenced to the +5 V supply and COMMON pins of the connector. The input current requirements shall be met across the full range of supply voltage specified in 22.5.1.

The bidirectional signal MDIO has two sets of input current requirements. The MDIO drivers have to be disabled when the input current measurement is made.

The input current characteristics for all MII signals shall fall within the limits specified in Table 22–13.

NOTE—These limits for dc input current allow the use of weak resistive pull-ups or pull-downs on the input of each MII signal. They allow the use of weak resistive pull-downs on the signals other than COL, MDC, and MDIO. They allow the use of a weak resistive pull-up on the signal COL. They allow the use of a resistive pull-down of 2 kΩ ± 5% on the MDIO signal in the STA. They require a resistive pull-up of 1.5 kΩ ± 5% on the MDIO signal in a PHY that is attached to the MII via the mechanical interface specified in 22.6. The limits on MDC and MDIO allow the signals to be “bused” to several PHYs that are contained on the same printed circuit assembly, with a single PHY attached via the MII connector.

22.4.4.3 Input capacitance

For all signals other than MDIO, the receiver input capacitance C_i shall not exceed 8 pF.

For the MDIO signal, the transceiver input capacitance shall not exceed 10 pF.

22.4.5 Cable characteristics

The MII cable consists of a bundle of individual twisted pairs of conductors with an overall shield covering this bundle. Each twisted pair shall be composed of a conductor for an individual signal and a return path dedicated to that signal.

NOTE—It is recommended that the signals RX_CLK and TX_CLK be connected to pairs that are located in the center of the cable bundle.

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Table 22–13—Input current limits

Symbol	Parameter	Condition	Signal(s)	Min (µA)	Max (µA)
I_{ih}	Input high current	V_i=5.25 V	All except COL, MDC, MDIO[a]	—	200
			COL[b]	—	20
			MDC[c]	—	20
			MDIO[d]	—	3000
			MDIO[e]	—	20
I_{il}	Input low current	V_i=0.00 V	All except COL, MDC, MDIO[a]	–20	—
			COL[b]	–200	—
			MDC[c]	–20	—
			MDIO[d]	–180	—
			MDIO[e]	–3800	—
I_{iq}	Input quiescent current	V_i=2.4 V	MDIO[d]	—	1450
			MDIO[e]	–1450	—

[a]Measured at input of Reconciliation sublayer for CRS, RXD<3:0>, RX_CLK, RX_DV, RX_ER, and TX_CLK. Measured at inputs of PHY for TXD<3:0>, TX_EN, and TX_ER.
[b]Measured at input of Reconciliation sublayer.
[c]Measured at input of PHY.
[d]Measured at input of STA.
[e]Measured at input of PHY, which can be attached via the mechanical interface specified in 22.6.

22.4.5.1 Conductor size

The specifications for dc resistance in 22.4.5.6 and characteristic impedance in 22.4.5.2 assume a conductor size of 0.32 mm (28 AWG).

22.4.5.2 Characteristic impedance

The single-ended characteristic impedance of each twisted pair shall be 68 Ω ± 10%. The characteristic impedance measurement shall be performed with the return conductor connected to the cable's overall shield at both ends of the cable.

22.4.5.3 Delay

The propagation delay for each twisted pair, measured from the MII connector to the PHY, shall not exceed 2.5 ns. The measurement shall be made with the return conductor of the pair connected to the cable's overall shield at both ends of the cable. The propagation delay shall be measured at a frequency of 25 MHz.

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22.4.5.4 Delay variation

The variation in the propagation delay of the twisted pairs in a given cable bundle, measured from the MII connector to the PHY, shall not exceed 0.1 ns. The measurement shall be made with the return conductor of the pair connected to the cable's overall shield at both ends of the cable.

22.4.5.5 Shielding

The overall shield has to provide sufficient shielding to meet the requirements of protection against electromagnetic interference.

The overall shield shall be terminated to the connector shell as defined in 22.6.2. A double shield, consisting of both braid and foil shielding, is strongly recommended.

22.4.5.6 DC resistance

The dc resistance of each conductor in the cable, including the contact resistance of the connector, shall not exceed 150 mΩ measured from the MII connector to the remote PHY.

22.4.6 Hot insertion and removal

The insertion or removal of a PHY from the MII with power applied (hot insertion or removal) shall not damage the devices on either side of the MII. In order to prevent contention between multiple output buffers driving the PHY output signals, a PHY that is attached to the MII via the mechanical interface defined in 22.6 shall ensure that its output buffers present a high impedance to the MII during the insertion process, and shall ensure that this condition persists until the output buffers are enabled via the Isolate control bit in the management interface basic register.

NOTE—The act of inserting or removing a PHY from an operational system may cause the loss of one or more packets or management frames that may be in transit across the MII or MDI.

22.5 Power supply

When the mechanical interface defined in 22.6 is used to interconnect printed circuit subassemblies, the Reconciliation sublayer shall provide a regulated power supply for use by the PHY.

The power supply shall use the following MII lines:

+5 V: The plus voltage output to the PHY.
COMMON: The return to the power supply.

22.5.1 Supply voltage

The regulated supply voltage to the PHY shall be 5 Vdc ± 5% at the MII connector with respect to the COMMON circuit at the MII over the range of load current from 0 mA to 750 mA. The method of over/under voltage protection is not specified; however, under no conditions of operation shall the source apply a voltage to the +5 V circuit of less than 0 V or greater than +5.25 Vdc.

Implementations that provide a conversion from the MII to the Attachment Unit Interface (AUI) to support connection to 10 Mb/s Medium Attachment Units (MAUs) will require a supplemental power source in order to meet the AUI power supply requirements specified in 7.5.2.5.

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22.5.2 Load current

The sum of the currents carried on the +5 V lines shall not exceed 750 mA, measured at the MII connector. The surge current drawn by the PHY shall not exceed 5 A peak for a period of 10 ms. The PHY shall be capable of powering up from 750 mA current limited sources.

22.5.3 Short-circuit protection

Adequate provisions shall be made to ensure protection of the power supply from overload conditions, including a short circuit between the +5 V lines and the COMMON lines.

22.6 Mechanical characteristics

When the MII is used to interconnect two printed circuit assemblies via a short length of cable, the cable shall be connected to the circuit assembly that implements the Reconciliation sublayer by means of the mechanical interface defined in this clause.

22.6.1 Definition of mechanical interface

A 40-pole connector having the mechanical mateability dimensions as specified in IEC 61076-3-101:1997 shall be used for the MII connector. The circuit assembly that contains the MAC sublayer and Reconciliation sublayer shall have a female connector with screw locks, and the mating cable shall have a male connector with jack screws.

No requirements are imposed on the mechanical interface used to connect the MII cable to the PHY circuit assembly when the MII cable is permanently attached to the PHY circuit assembly, as shown in Figure 22–2. If the cable is not permanently attached to the PHY circuit assembly, then a male connector with jack screws shall be used for the MII connector at the PHY circuit assembly.

NOTE—All MII conformance tests are performed at the mating surfaces of the MII connector at the Reconciliation sublayer end of the cable. If a PHY circuit assembly does not have a permanently attached cable, the requirements of this clause also have to be met when a cable that meets the requirements of 22.4.5 is used to attach the PHY circuit assembly to the circuit assembly that contains the Reconciliation sublayer.

22.6.2 Shielding effectiveness and transfer impedance

The shells of these connectors shall be plated with conductive material to ensure the integrity of the current path from the cable shield to the chassis. The transfer impedance of this path shall not exceed the values listed in Table 22–14, after a minimum of 500 cycles of mating and unmating. The shield transfer impedance values listed in the table are measured in accordance with the procedure defined in Annex L of IEEE Std 1394.

Table 22–14—Transfer impedance performance requirements

Frequency	Value
30 MHz	–26 dBΩ
159 MHz	–13 dBΩ
500 MHz	–5 dBΩ

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All additions to provide for female shell to male shell conductivity shall be on the shell of the connector with male contacts. There should be multiple contact points around the sides of this shell to provide for shield continuity.

22.6.3 Connector pin numbering

Figure 22–20 depicts the MII connector pin numbering, as seen looking into the contacts of a female connector from the mating side.

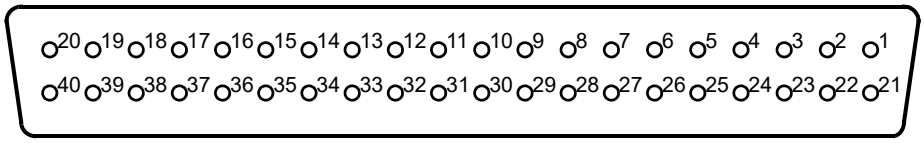

Figure 22–20—MII connector pin numbering

22.6.4 Clearance dimensions

The circuit assembly that contains the MAC sublayer and Reconciliation sublayer shall provide sufficient clearance around the MII connector to allow the attachment of cables that use die cast metal backshells and overmold assemblies. This requirement may be met by providing the clearance dimensions shown in Figure 22–21.

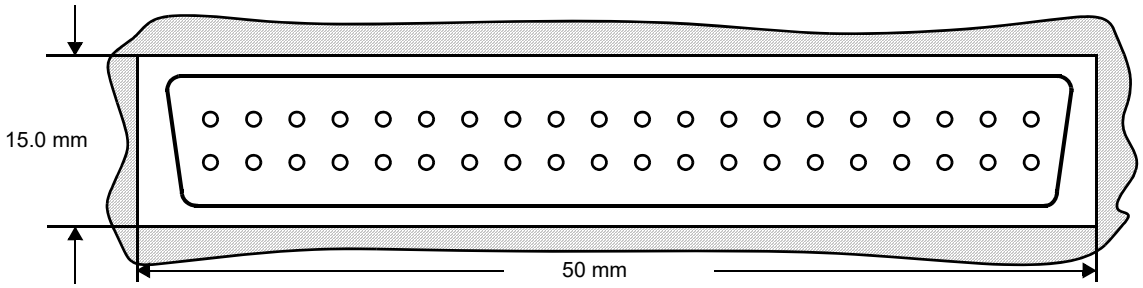

Figure 22–21—MII connector clearance dimensions

22.6.5 Contact assignments

Table 22–15 shows the assignment of circuits to connector contacts.

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Table 22–15—MII connector contact assignments

Contact	Signal name	Contact	Signal name
1	+5 V	21	+5 V
2	MDIO	22	COMMON
3	MDC	23	COMMON
4	RXD<3>	24	COMMON
5	RXD<2>	25	COMMON
6	RXD<1>	26	COMMON
7	RXD<0>	27	COMMON
8	RX_DV	28	COMMON
9	RX_CLK	29	COMMON
10	RX_ER	30	COMMON
11	TX_ER	31	COMMON
12	TX_CLK	32	COMMON
13	TX_EN	33	COMMON
14	TXD<0>	34	COMMON
15	TXD<1>	35	COMMON
16	TXD<2>	36	COMMON
17	TXD<3>	37	COMMON
18	COL	38	COMMON
19	CRS	39	COMMON
20	+5 V	40	+5 V

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22.7 LPI assertion and detection

Certain PHYs support Energy-Efficient Ethernet (EEF) (see Clause 78). PHYs with EEE capability support LPI assertion and detection. LPI operation and the LPI client are described in 78.1. LPI signaling allows the LPI client to signal to the PHY and to the link partner that an interruption in the data stream is expected and components may use this information to enter power-saving modes that require additional time to resume normal operation. Similarly, it allows the LPI client to understand that the link partner has sent such an indication. LPI signaling on the MII is specified only for 100 Mb/s operation.

The LPI assertion and detection mechanism fits conceptually between the PLS Service Primitives and the MII signals as shown in Figure 22–22.

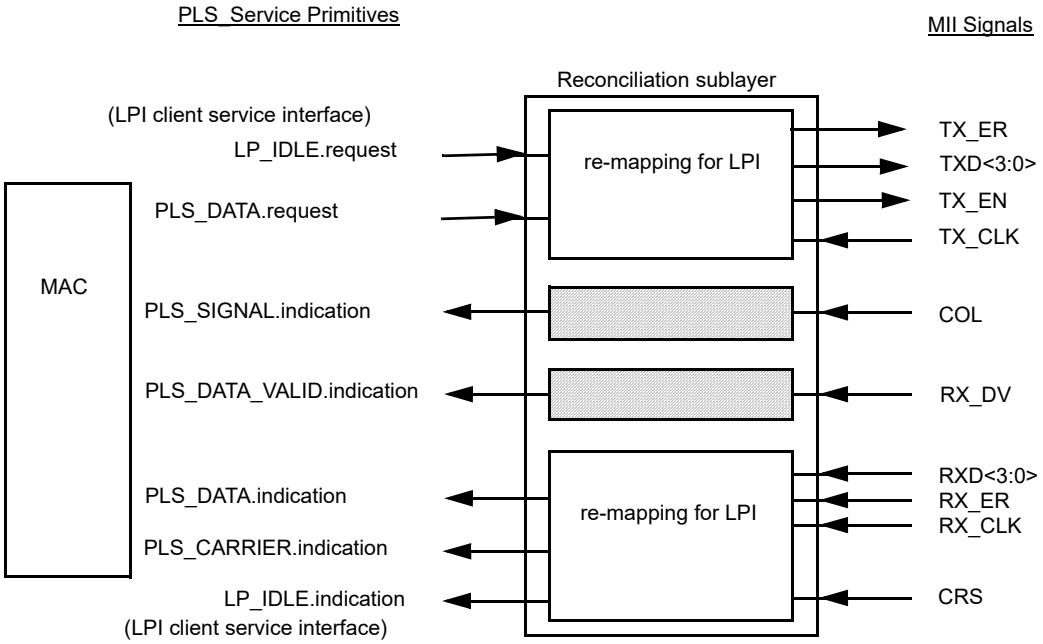

Figure 22–22—LPI assertion and detection mechanism

The definition of TX_EN, TX_ER and TXD<3:0> is derived from the state of PLS_DATA.request (22.2.1.1), except when it is overridden by an assertion of LP_IDLE.request. Similarly, RX_ER and RXD<3:0> are mapped to PLS_DATA.indication except when LP_IDLE is detected. CRS is mapped to PLS_CARRIER.indication except when LP_IDLE.request is asserted or the wake timer has yet to expire. The timing of PLS_CARRIER.indication when used for the LPI function is controlled by the LPI transmit state diagram.

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22.7.1 LPI messages

LP_IDLE.indication(LPI_INDICATION)

A primitive that indicates to the LPI client that the PHY has detected the assertion or deassertion of LPI from the link partner.

Values:DEASSERT: The link partner is operating with normal interframe behavior (default).

ASSERT: The link partner has asserted LPI.

LP_IDLE.request(LPI_REQUEST)

The LPI_REQUEST parameter can take one of two values: ASSERT or DEASSERT. ASSERT initiates the signaling of LPI to the link partner. DEASSERT stops the signaling of LPI to the link partner. The effect of receipt of this primitive is undefined if link_status is not OK (see 28.2.6.1.1) or if LPI_REQUEST=ASSERT within 1 second of the change of link_status to OK.

22.7.2 Transmit LPI state diagram

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been deasserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake up time is enforced by the transmit LPI state diagram and the rules mapping CARRIER_SENSE.indication defined in 22.2.1.3. The implementation shall conform to the behavior described by the transmit LPI state diagram shown in Figure 22–23.

22.7.2.1 Conventions

The notation used in the state diagram follows the conventions of 21.5.

22.7.2.2 Variables and counters

The transmit LPI state diagram uses the following variables and counters:

power_on

Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.

Values:FALSE: The device is completely powered (default).

TRUE: The device has not been completely powered.

rs_reset

Used by management to control the resetting of the RS.

Values:FALSE: Do not reset the RS (default).

TRUE: Reset the RS.

tw_timer

A timer that counts the time since the deassertion of LPI. The terminal count of the timer shall be the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2 and 78.4. The minimum value of $T_{w\_sys\_tx}$ shall be 30 μs for 100BASE-TX. Signal tw_timer_done is asserted on reaching its terminal count.

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22.7.2.3 State diagram

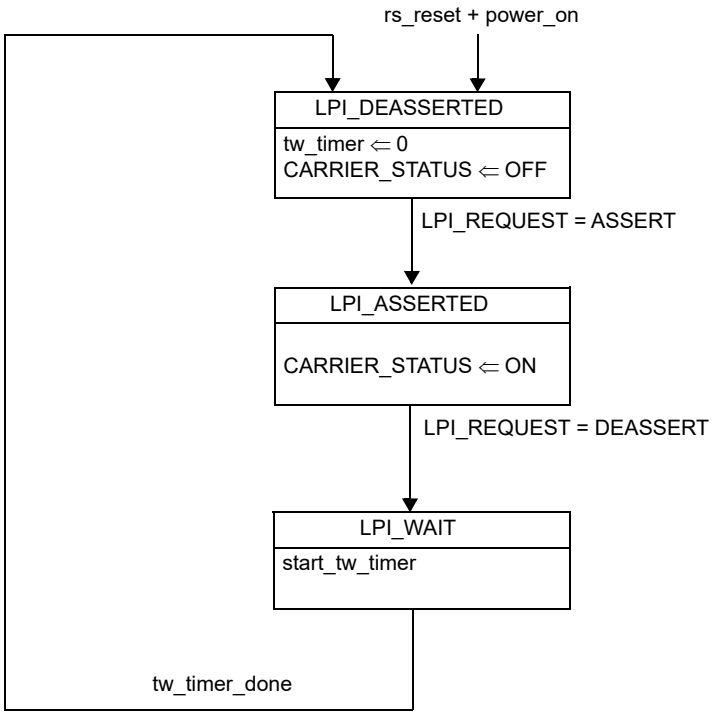

Figure 22–23—Transmit LPI state diagram

22.7.3 Considerations for transmit system behavior

The transmit system should expect that egress data flow will be halted for at least resolved $T_{w\_sys\_tx}$ (see 78.2) time, in microseconds, after it requests the deassertion of LPI. Buffering and queue management should be designed to accommodate this.

22.7.3.1 Considerations for receive system behavior

The mapping function of the Reconciliation Sublayer shall continue to signal IDLE on PLS_DATA.indicate while it is detecting LP_IDLE on the MII. The receive system should be aware that data frames may arrive at the MII following the deassertion of LPI_INDICATION with a delay corresponding to the link partner's resolved $T_{w\_sys\_rx}$ (as specified in 78.5) time, in microseconds.

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22.8 Protocol implementation conformance statement (PICS) proforma for Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)[54]

22.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

22.8.2 Identification

22.8.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

22.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	No [ ] Yes [ ]

Date of Statement	

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22.8.2.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*GM	Implementation of GMII	22.2.4	O		
*MUNI	Implementation of unidirectional PCS	22.2.4	O		
*LPI	Implementation of LPI	22.7	O		
*PLCA	Implementation of PLCA	22.2.2.4	O		

22.8.3 PICS proforma tables for reconciliation sublayer and media independent interface

22.8.3.1 Mapping of PLS service primitives

Item	Feature	Subclause	Status	Support	Value/Comment
PL1	Response to RX_ER	22.2.1.5	M		Produce FrameCheckError at MAC

22.8.3.2 MII signal functional specifications

Item	Feature	Subclause	Status	Support	Value/Comment
SF1	TX_CLK frequency	22.2.2.1	M		25% of transmitted data rate (25 MHz or 2.5 MHz)
SF2	TX_CLK duty cycle	22.2.2.1	M		35% to 65%
SF3	RX_CLK min high/low time	22.2.2.2	M		35% of nominal period
SF4	RX_CLK synchronous to recovered data	22.2.2.2	M		
SF5	RX_CLK frequency	22.2.2.2	M		25% of received data rate (25 MHz or 2.5 MHz)
SF6	RX_CLK duty cycle	22.2.2.2	M		35% to 65%
SF7	RX_CLK source due to loss of signal	22.2.2.2	M		Nominal clock reference (e.g., TX_CLK reference)
SF8	RX_CLK transitions only while RX_DV deasserted	22.2.2.2	M		
SF9	RX_CLK max high/low time following deassertion of RX_DV	22.2.2.2	M		Max 2 times the nominal period
SF10	TX_EN assertion	22.2.2.3	M		On first nibble of preamble
SF11	TX_EN remains asserted	22.2.2.3	M		Stay asserted while all nibbles are transmitted over MII
SF12	TX_EN transitions	22.2.2.3	M		Synchronous with TX_CLK

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22.8.3.2 MII signal functional specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
SF13	TX_EN negation	22.2.2.3	M		Before first TX_CLK after final nibble of frame
SF14	TXD<3:0> transitions	22.2.2.4	M		Synchronous with TX_CLK
SF15	TX_ER transitions	22.2.2.5	M		Synchronous with TX_CLK
SF16	TX_ER effect on PHY while TX_EN is asserted	22.2.2.5	M		Cause PHY to emit invalid symbol
SF17	TX_ER effect on PHY while operating at 10 Mb/s (with the exception of 10BASE-T1S and 10BASE-T1L), or when TX_EN is deasserted	22.2.2.5	M		No effect on PHY
SF18	TX_ER implementation	22.2.2.5	!LPI:M		At MII of a PHY
SF19	Effect on PHY while TXD<3:0> is any value other than 0001, and TX_EN is deasserted and TX_ER is asserted	22.2.2.4	LPI:M		No effect
SF20	TX_ER pulled down if not actively driven	22.2.2.5	M		At MII of a repeater or MAC/ RS only
SF21	RX_DV transitions	22.2.2.7	M		Synchronous with RX_CLK
SF22	RX_DV assertion	22.2.2.7	M		From first recovered nibble to final nibble of a frame per Figure 22–7
SF23	RX_DV negation	22.2.2.7	M		Before the first RX_CLK follows the final nibble per Figure 22–7
SF24	RXD<3:0> effect on Reconciliation sublayer while RX_DV is deasserted	22.2.2.8	M		No effect
SF25	RX_ER assertion	22.2.2.10	M		By PHY to indicate error
SF26	RX_ER transitions	22.2.2.10	M		Synchronous with RX_CLK
SF27	RX_ER effect on Reconciliation sublayer while RX_DV is deasserted	22.2.2.10	M		No effect
SF28	CRS assertion	22.2.2.11	M		By PHY when either transmit or receive is NON-IDLE
SF29	CRS deassertion	22.2.2.11	M		By PHY when both transmit and receive are IDLE
SF30	CRS assertion during collision	22.2.2.11	M		Remain asserted throughout
SF31	COL assertion	22.2.2.12	M		By PHY upon detection of collision on medium
SF32	COL remains asserted while collision persists	22.2.2.12	M		

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22.8.3.2 MII signal functional specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
SF33	COL response to SQE	22.2.2.12	M		Assertion by PHY
SF34	MDC min high/low time	22.2.2.13	M		160 ns
SF35	MDC min period	22.2.2.13	M		400 ns
SF36	MDIO uses three-state drivers	22.2.2.14	M		
SF37	PHY pull-up on MDIO	22.2.2.14	M		1.5 kΩ ± 5% (to +5 V)
SF38	STA pull-down on MDIO	22.2.2.14	M		2 kΩ ± 5% (to 0 V)
SF39	Effect on PHY while TXD<3:0> is 0010, and TX_EN is deasserted, and TX_ER is asserted	22.2.2.4	PLCA: M		RS sends BEACON request
SF40	Effect on PHY while TXD<3:0> is 0011, and TX_EN is deasserted, and TX_ER is asserted	22.2.2.4	PLCA: M		RS sends COMMIT request
SF41	Effect on PHY while TXD<3:0> is any value other than 0010 or 0011, and TX_EN is deasserted, and TX_ER is asserted	22.2.2.4	PLCA: M		No effect

22.8.3.3 LPI functions

Item	Feature	Subclause	Status	Support	Value/Comment
L1	Transitions to LPI_ASSERTED and LPI_DEASSERTED reflected in CARRIER_STATUS	22.2.1.3.3	LPI:M		
L2	RX_CLK max high/low time while the PHY is asserting LPI	22.2.2.2	LPI:M		Max 2 times the nominal period
L3	Assertion of LPI as defined in Table 22–1	22.2.2.4	LPI:M		
L4	RX_CLK stoppable during LPI	22.2.2.9	LPI:O		At least 9 cycles after LPI assertion
L5	RX_CLK restart before LPI deasserted	22.2.2.9	LPI:O		At least 1 positive edge before LPI deassertion
L6	Behavior matches the transmit LPI state diagram	22.7.2	LPI:M		
L7	Terminal count for tw_timer	22.7.2.2	LPI:M		Based on resolved $T_{w\_sys\_tx}$
L8	RS continues to indicate IDLE on PLS_DATA.indicate	22.7.3.1	LPI:M		

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22.8.3.4 Frame structure

Item	Feature	Subclause	Status	Support	Value/Comment
FS1	Format of transmitted frames	22.2.3	M		Per Figure 22–12
FS2	Nibble transmission order	22.2.3	M		Per Figure 22–13
FS3	Preamble 7 octets long	22.2.3.2.1	M		10101010 10101010 10101010 10101010 10101010 10101010 10101010
FS4	Preamble and SFD transmission	22.2.3.2.1	M		Per Table 22–3
FS5	Preamble and SFD reception	22.2.3.2.2	M		Per Table 22–4, Table 22–5
FS6	N octets transmitted as 2N nibbles	22.2.3.3	M		Per Figure 22–13
FS7	Indication of excess nibbles	22.2.3.5	M		Frame contains non-integer number of octets is received

22.8.3.5 Management functions

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	Incorporate of basic register set	22.2.4	M		Two 16-bit registers as Control register (register 0) and Status register (register 1)
MF2	Action on reset	22.2.4.1.1	M		Reset the entire PHY including Control and Status to default value and set bit 0.15 = 1
MF3	Return 1 until reset completed	22.2.4.1.1	M		Yes (when reset is done, 0.15 is self-clearing)
MF4	Reset completes within 0.5 s	22.2.4.1.1	M		
MF5	Loopback mode	22.2.4.1.2	M		Whenever 0.14 is 1
MF6	Receive circuitry isolated from network in loopback mode	22.2.4.1.2	M		
MF7	Effect of assertion of TX_EN in loopback mode	22.2.4.1.2	M		No transmission
MF8	Propagation of data in loopback mode	22.2.4.1.2	M		PHY accepts transmit data and return it as receive data
MF9	Delay from TX_EN to RX_DV in loopback mode	22.2.4.1.2	M		Less than 512 BT
MF10	Behavior of COL in loopback mode	22.2.4.1.2	M		Deasserted (for 0.7 = 0)
MF11	Behavior of COL in loopback mode	22.2.4.1.2	M		If 0.7 = 1, see MF33 and MF34
MF12	Value of speed selection bits	22.2.4.1.3	M		Set to match a valid PHY speed

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22.8.3.5 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF13	Ignore writes to speed selection bits for unsupported speed	22.2.4.1.3	M		
MF14	Auto-Negotiation enable	22.2.4.1.4	M		By setting 0.12 = 1
MF15	Duplex mode, speed selection have no effect when Auto-Negotiation is enabled	22.2.4.1.4	M		If 0.12=1, bits 0.13, 0.8 and 0.6 have no effect on link configuration
MF16	PHY without Auto-Negotiation returns value of zero	22.2.4.1.4	M		Yes (if 1.3=0, then 0.12=0)
MF17	PHY without Auto-Negotiation ignores writes to enable bit	22.2.4.1.4	M		Yes (if 1.3=0, 0.12 always = 0 and cannot be changed)
MF18	Response to management transactions in power down	22.2.4.1.5	M		Remains active
MF19	Spurious signals in power down	22.2.4.1.5	M		None (not allowed)
MF20	TX_CLK and RX_CLK stabilize within 0.5 s	22.2.4.1.5	M		Yes (after both bits 0.11 and 0.10 are cleared to zero)
MF21	PHY Response to input signals while isolated	22.2.4.1.6	M		NONE
MF22	High impedance on PHY output signals while isolated	22.2.4.1.6	M		Yes (TX_CLK, RX_CLK, RX_DV, RX_ER, RXD bundle, COL, and CRS)
MF23	Response to management transactions while isolated	22.2.4.1.6	M		Remains active
MF24	Default value of isolate	22.2.4.1.6	M		0.10 =1
MF25	PHY without Auto-Negotiation returns value of zero	22.2.4.1.7	M		0.9 = 0 if 1.3 = 0 or 0.12 = 0
MF26	PHY without Auto-Negotiation ignores writes to restart bit	22.2.4.1.7	M		0.9 = 0, cannot be changed if 1.3 = 0 or 0.12 = 0
MF27	Restart Auto-Negotiation	22.2.4.1.7	M		When 0.9 = 1 if 0.12 = 1 and 1.3 = 1
MF28	Return 1 until Auto-Negotiation initiated	22.2.4.1.7	M		0.9 is self-clearing to 0
MF29	Auto-Negotiation not affected by clearing bit	22.2.4.1.7	M		
MF30	Value of duplex mode bit for PHYs with one duplex mode	22.2.4.1.8	M		Set 0.8 to match the correct PHY duplex mode
MF31	PHY with one duplex mode ignores writes to duplex bit	22.2.4.1.8	M		Yes (0.8 remains unchanged)

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22.8.3.5 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF32	Loopback not affected by duplex mode	22.2.4.1.8	M		Yes (0.8 has no effect on PHY when 0.14 = 1)
MF33	Assertion of COL in collision test mode	22.2.4.1.9	M		Within 512 BT after TX_EN is asserted
MF34	deassertion of COL in collision test mode	22.2.4.1.9	M		After TX_EN is deasserted within: MII = 4 BT, GMII = 16 BT
MF35	Reserved bits written as zero	22.2.4.1.11	M		
MF36	Reserved bits ignored when read	22.2.4.1.11	M		
MF37	PHY returns 0 in reserved bits	22.2.4.1.11	M		
MF38	PHY without unidirectional ability	22.2.4.1.12	M		PHY returns a value of 0 in 0.5 if 1.7=0
MF39	PHY without unidirectional ability	22.2.4.1.12	M		PHY always maintains a value of 0 in 0.5 if 1.7=0
MF40	Unidirectional enable	22.2.4.1.12	MUNI:M		By setting 0.12 = 0, 0.8 = 1 and 0.5 = 1
MF41	Unidirectional disable	22.2.4.1.12	MUNI:M		By setting 0.12 = 1, 0.8 = 0 or 0.5 = 0
MF42	Ignore bit 0.5	22.2.4.1.12	MUNI:M		Ignore 0.5 when 0.12 = 1 or 0.8 = 0
MF43	Enable unidirectional mode	22.2.4.1.12	MUNI:M		Enable only when OAM sublayer is enabled or when part of 1000BASE-PX-D PHY
MF44	Disable unidirectional mode	22.2.4.1.12	MUNI:M		Unidirectional mode is disabled before disabling OAM sublayer when not part of 1000BASE-PX-D PHY
MF45	Unidirectional ability	22.2.4.2.8	M		Bit 1.7 = 0 for all PHYs except those using 66.1 and 66.2
MF46	Effect of write on status register	22.2.4.2	M		No effect
MF47	Reserved bits ignored when read	22.2.4.2.8	M		
MF48	PHY returns 0 in reserved bits	22.2.4.2.8	M		
MF49	PHY returns 0 if Auto-Negotiation disabled	22.2.4.2.10	M		Yes (1.5 = 0 when 0.12 = 0)
MF50	PHY returns 0 if it lacks ability to perform Auto-Negotiation	22.2.4.2.10	M		Yes (1.5 = 0 when 1.3 = 0)
MF51	Remote fault has latching function	22.2.4.2.11	M		Yes (once set will remain set until cleared)
MF52	Remote fault cleared on read	22.2.4.2.11	M		Yes

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22.8.3.5 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF53	Remote fault cleared on reset	22.2.4.2.11	M		Yes (when 0.15 = 1)
MF54	PHY without remote fault returns value of zero	22.2.4.2.11	M		Yes (1.4 always 0)
MF55	Link status has latching function	22.2.4.2.13	M		Yes (once cleared by link failure will remain cleared until read by MII)
MF56	Jabber detect has latching function	22.2.4.2.14	M		Yes (once set will remain set until cleared)
MF57	Jabber detect cleared on read	22.2.4.2.14	M		
MF58	Jabber detect cleared on reset	22.2.4.2.14	M		
MF59	All PHYs operating at rates of 100 Mb/s or above return 0 for jabber detect	22.2.4.2.14	M		Yes (1.1 always = 0 for all PHYs operating at rates of 100 Mb/s or above)
MF60	MDIO not driven if register read is unimplemented	22.2.4.3	M		Yes (MDIO remain high impedance)
MF61	Write has no effect if register written is unimplemented	22.2.4.3	M		
MF62	Registers 2 and 3 constitute unique identifier for PHY type	22.2.4.3.1	M		
MF63	MSB of PHY identifier is 2.15	22.2.4.3.1	M		
MF64	LSB of PHY identifier is 3.0	22.2.4.3.1	M		
MF65	Composition of PHY identifier	22.2.4.3.1	O		22-bit OUI, 6-bit model, 4-bit version per Figure 22–14
MF66	Format of management frames	22.2.4.5	M		Per Table 22–11
MF67	Idle condition on MDIO	22.2.4.5.1	M		High impedance state
MF68	MDIO preamble sent by STA	22.2.4.5.2	M		32 contiguous logic one bits
MF69	MDIO preamble observed by PHY	22.2.4.5.2	M		32 contiguous logic one bits
MF70	Assignment of PHYAD 0	22.2.4.5.5	M		Address of PHY attached via Mechanical Interface
MF71	Assignment of REGAD 0	22.2.4.5.6	M		MII control register address
MF72	Assignment of REGAD 1	22.2.4.5.6	M		MII status register address
MF73	High impedance during first bit time of turnaround in read transaction	22.2.4.5.7	M		
MF74	PHY drives zero during second bit time of turnaround in read transaction	22.2.4.5.7	M		
MF75	STA drives MDIO during turnaround in write transaction	22.2.4.5.7	M		

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22.8.3.5 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF76	First data bit transmitted	22.2.4.5.8	M		Bit 15 of the register being addressed
MF77	Incorporate Extended Status register	22.2.4	GM:M		16-bit register Extended Status register (register 15)
MF78	Reserved bits written as zero	22.2.4.2.8	GM:M		
MF79	Extended Status	22.2.4.2.16	GM:M		Yes (1.8 always = 1 for 1000 Mb/s operation)
MF80	Write to Extended Status register	22.2.4.4	GM:M		No effect
MF81	Reserved bits written as zero	22.2.4.4.5	GM:M		
MF82	Reserved bits ignored when read	22.2.4.4.5	GM:M		
MF83	PHY returns 0 in reserved bits	22.2.4.4.5	GM:M		

22.8.3.6 Signal timing characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
ST1	Timing characteristics measured in accordance with Annex 22C	22.3	M		
ST2	Transmit signal clock to output delay	22.3.1	M		Min = 0 ns; Max = 25 ns per Figure 22–16
ST3	Receive signal setup time	22.3.2	M		Min = 10 ns per Figure 22–17
ST4	Receive signal hold time	22.3.2	M		Min = 10 ns per Figure 22–17
ST5	MDIO setup and hold time	22.3.4	M		Setup min = 10 ns; Hold min = 10 ns per Figure 22–18
ST6	MDIO clock to output delay	22.3.4	M		Min = 0 ns; Max = 300 ns per Figure 22–19

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22.8.3.7 Electrical characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
EC1	Signal paths are either point to point, or a sequence of point-to-point transmission paths	22.4.2	M		
EC2	MII uses unbalanced signal transmission paths	22.4.2	M		
EC3	Characteristic impedance of electrically long paths	22.4.2	M		68 Ω ± 15%
EC4	Output impedance of driver used to control reflections	22.4.2	M		On all electrically long point to point signal paths
EC5	V_{oh}	22.4.3.1	M		≥ 2.4 V (I_{oh} = –4 mA)
EC6	V_{ol}	22.4.3.1	M		≤ 0.4 V (I_{ol} = 4 mA)
EC7	Performance requirements to be guaranteed by ac specifications	22.4.3.2	M		Min switching potential change (including its reflection) ≥ 1.8 V
EC8	$V_{ih(min)}$	22.4.4.1	M		2 V
EC9	$V_{il(max)}$	22.4.4.1	M		0.8 V
EC10	Input current measurement point	22.4.4.2	M		At MII connector
EC11	Input current reference potentials	22.4.4.2	M		Reference to MII connector +5 V and COMMON pins
EC12	Input current reference potential range	22.4.4.2	M		0 V to 5.25 V
EC13	Input current limits	22.4.4.2	M		Per Table 22–12
EC14	Input capacitance for signals other than MDIO	22.4.4.3	M		≤ 8 pF
EC15	Input capacitance for MDIO	22.4.4.3	M		≤ 10 pF
EC16	Twisted-pair composition	22.4.5	M		Conductor for each signal with dedicated return path
EC17	Single-ended characteristic impedance	22.4.5.2	M		68 Ω ± 10%
EC18	Characteristic impedance measurement method	22.4.5.2	M		With return conductor connected to cable shield
EC19	Twisted-pair propagation delay	22.4.5.3	M		≤ 2.5 ns
EC20	Twisted-pair propagation delay measurement method	22.4.5.3	M		With return conductor connected to cable shield
EC21	Twisted-pair propagation delay measurement frequency	22.4.5.3	M		25 MHz
EC22	Twisted-pair propagation delay variation	22.4.5.4	M		≤ 0.1 ns

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22.8.3.7 Electrical characteristics *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
EC23	Twisted-pair propagation delay variation measurement method	22.4.5.4	M		With return conductor connected to cable shield
EC24	Cable shield termination	22.4.5.5	M		To the connector shell
EC25	Cable conductor DC resistance	22.4.5.6	M		≤ 150 mΩ
EC26	Effect of hot insertion/removal	22.4.6	M		Causes no damage
EC27	State of PHY output buffers during hot insertion	22.4.6	M		High impedance
EC28	State of PHY output buffers after hot insertion	22.4.6	M		High impedance until enabled via Isolate bit

22.8.3.8 Power supply

Item	Feature	Subclause	Status	Support	Value/Comment
PS1	Regulated power supply provided	22.5	M		To PHY by Reconciliation sublayer
PS2	Power supply lines	22.5	M		+5 V and COMMON (return of +5 V)
PS3	Regulated supply voltage limits	22.5.1	M		5 Vdc ± 5%
PS4	Over/under voltage limits	22.5.1	M		Over limit = 5.25 Vdc Under limit = 0 V
PS5	Load current limit	22.5.2	M		750 mA
PS6	Surge current limit	22.5.2	M		≤ 5 A peak for 10 ms
PS7	PHY can power up from current limited source	22.5.2	M		From 750 mA current limited source
PS8	Short-circuit protection	22.5.2	M		When +5 V and COMMON are shorted

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22.8.3.9 Mechanical characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
*MC1	Use of Mechanical Interface	22.6	O		Optional
MC2	Connector reference standard	22.6.1	MC1:M		IEC 61076-3-101:1997
MC3	Use of female connector	22.6.1	MC1:M		At MAC/RS side
MC4	Use of male connector	22.6.1	MC1:M		At PHY mating cable side
MC5	Connector shell plating	22.6.2	MC1:M		Use conductive material
MC6	Shield transfer impedance	22.6.2	MC1:M		After 500 cycles of mating/ unmating, per Table 22–13
MC7	Additions to provide for female shell to male shell conductivity	22.6.2	MC1:M		On shell of conductor with male contacts
MC8	Clearance dimensions	22.6.4	MC1:M		15 mm × 50 mm, per Figure 22–21

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23. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T4

NOTE—This PHY is not recommended for new installations. Since September 2003, maintenance changes are no longer being considered for this clause.

23.1 Overview

The 100BASE-T4 PCS, PMA, and baseband medium specifications are aimed at users who want 100 Mb/s performance, but would like to retain the benefits of using voice-grade twisted-pair cable. 100BASE-T4 signaling requires four pairs of Category 3 or better cable, installed according to ISO/IEC 11801: 1995, as specified in 23.6. This type of cable, and the connectors used with it, are simple to install and reconfigure. 100BASE-T4 does not transmit a continuous signal between packets, which makes it useful in battery powered applications. The 100BASE-T4 PHY is one of the 100BASE-T family of high-speed CSMA/CD network specifications.

23.1.1 Scope

This clause defines the type 100BASE-T4 Physical Coding Sublayer (PCS), type 100BASE-T4 Physical Medium Attachment (PMA) sublayer, and type 100BASE-T4 Medium Dependent Interface (MDI). Together, the PCS and PMA layers comprise a 100BASE-T4 Physical Layer device (PHY). Provided in this document are full functional, electrical, and mechanical specifications for the type 100BASE-T4 PCS, PMA, and MDI. This clause also specifies the baseband medium used with 100BASE-T4.

23.1.2 Objectives

The following are the objectives of 100BASE-T4:

a) To support the CSMA/CD MAC in the half duplex mode of operation.
b) To support the 100BASE-T MII, Repeater, and optional Auto-Negotiation.
c) To provide 100 Mb/s data rate at the MII.
d) To provide for operating over twisted pairs of Category 3, 4, or 5 cable, installed as horizontal runs in accordance with ISO/IEC 11801: 1995, as specified in 23.6, at distances up to 100 m (328 ft).
e) To allow for a nominal network extent of 200 m, including:
    1) Unshielded twisted-pair links of 100 m.
    2) Two-repeater networks of approximately a 200 m span.
f) To provide a communication channel with a mean ternary symbol error ratio, at the PMA service interface, of less than one part in 10^8.

23.1.3 Relation of 100BASE-T4 to other standards

Relations between the 100BASE-T4 PHY and the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model are shown in Figure 23–1. The PHY Layers shown in Figure 23–1 connect one Clause 4 Media Access Control (MAC) layer to a Clause 27 repeater. This clause also discusses other variations of the basic configuration shown in Figure 23–1. This whole clause builds on Clause 1 through Clause 4 of this standard.

23.1.4 Summary

The following paragraphs summarize the PCS and PMA clauses of this standard.

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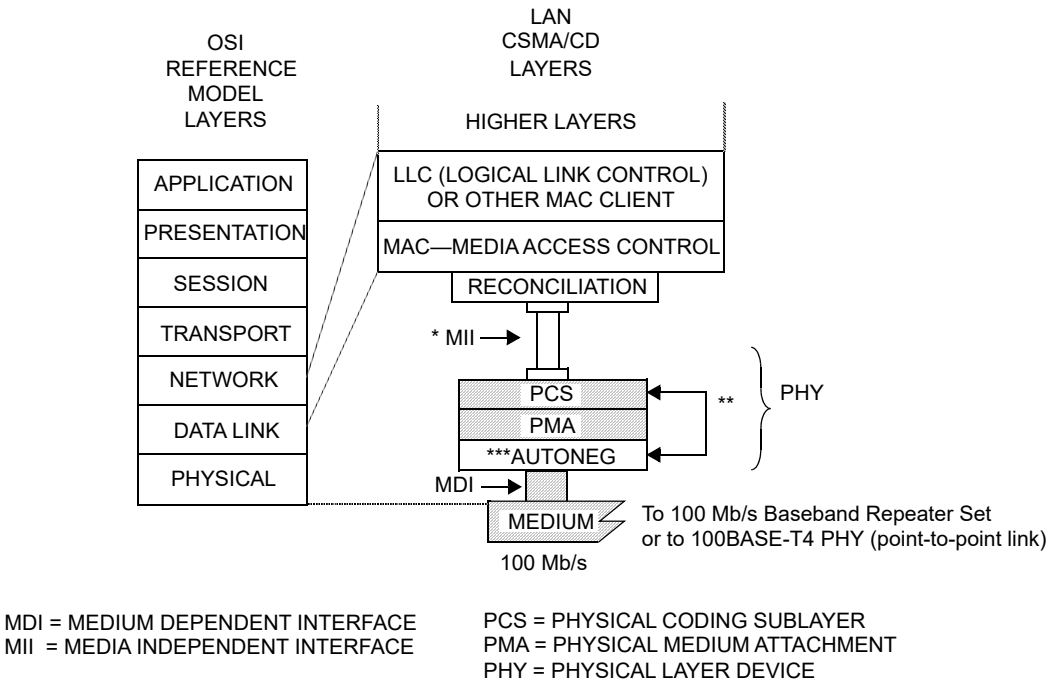

Figure 23–1—Type 100BASE-T4 PHY relationship to the ISO Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

23.1.4.1 Summary of Physical Coding Sublayer (PCS) specification

The 100BASE-T4 PCS couples a Media Independent Interface (MII), as described in Clause 22, to a Physical Medium Attachment sublayer (PMA).

The PCS Transmit function accepts data nibbles from the MII. The PCS Transmit function encodes these nibbles using an 8B6T coding scheme (to be described) and passes the resulting ternary symbols to the PMA. In the reverse direction, the PMA conveys received ternary symbols to the PCS Receive function. The PCS Receive function decodes them into octets, and then passes the octets one nibble at a time up to the MII. The PCS also contains a PCS Carrier Sense function, a PCS Error Sense function, a PCS Collision Presence function, and a management interface.

Figure 23–2 shows the division of responsibilities between the PCS, PMA, and MDI layers.

Physical level communication between PHY entities takes place over four twisted pairs. This specification permits the use of Category 3, 4, or 5 twisted pairs, installed according to ISO/IEC 11801: 1995, as specified in 23.6. Figure 23–3 shows how the PHY manages the four twisted pairs at its disposal.

The 100BASE-T4 transmission algorithm always leaves one pair open for detecting carrier from the far end (see Figure 23–3). Leaving one pair open for carrier detection in each direction greatly simplifies media access control. All collision detection functions are accomplished using only the unidirectional pairs TX_D1 and RX_D2, in a manner similar to 10BASE-T. This collision detection strategy leaves three pairs in each direction free for data transmission, which uses an 8B6T block code, schematically represented in Figure 23–4.

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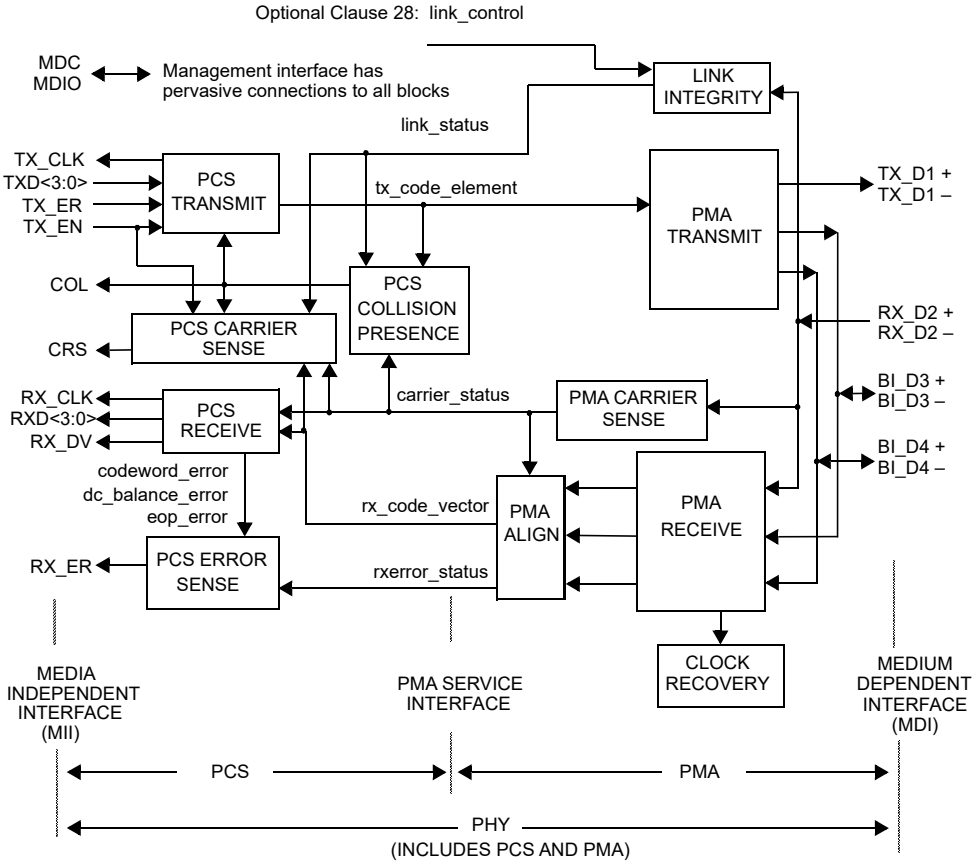

Figure 23–2—Division of responsibilities between 100BASE-T4 PCS and PMA

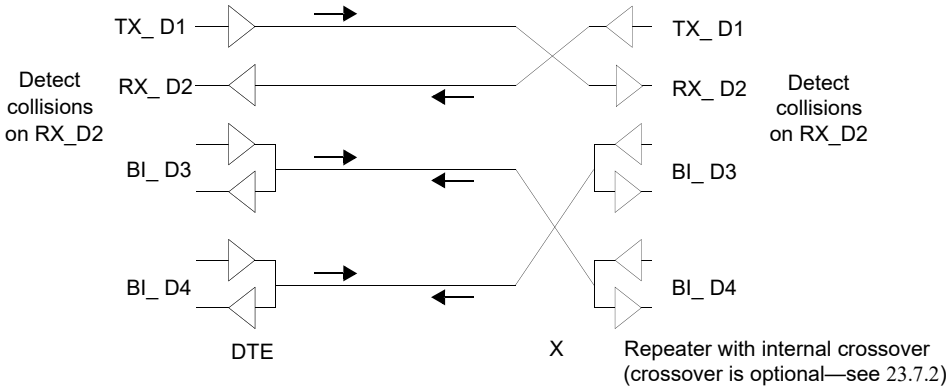

Figure 23–3—Use of wire pairs

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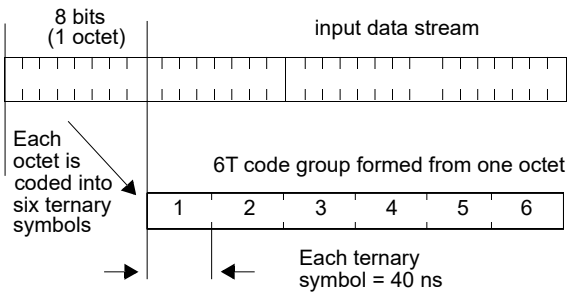

Figure 23–4—8B6T coding

8B6T coding, as used with 100BASE-T4 signaling, maps data octets into ternary symbols. Each octet is mapped to a pattern of 6 ternary symbols, called a 6T code group. The 6T code groups are fanned out to three independent serial channels. The effective data rate carried on each pair is one third of 100 Mb/s, which is 33.333... Mb/s. The ternary symbol transmission rate on each pair is 6/8 times 33.33 Mb/s, or precisely 25.000 MHz.

Refer to Annex 23A for a complete listing of 8B6T codewords.

The PCS functions and state diagrams are specified in 23.2. The PCS electrical interface to the MII conforms to the interface requirements of Clause 21. The PCS interface to the PMA is an abstract message-passing interface specified in 23.3.

23.1.4.2 Summary of physical medium attachment (PMA) specification

The PMA couples messages from the PMA service interface onto the twisted-pair physical medium. The PMA provides communications, at 100 Mb/s, over four pairs of twisted-pair wiring up to 100 m in length.

The PMA Transmit function, shown in Figure 23–2, comprises three independent ternary data transmitters. Upon receipt of a PMA_UNITDATA.request message, the PMA synthesizes one ternary symbol on each of the three output channels (TX_D1, BI_D3, and BI_D4). Each output driver has a *ternary* output, meaning that the output waveform can assume any of three values, corresponding to the transmission of ternary symbols CS0, CS1, or CS-1 (see 23.4.3.1) on each of the twisted pairs.

The PMA Receive function comprises three independent ternary data receivers. The receivers are responsible for acquiring clock, decoding the Start of Stream Delimiter (SSD) on each channel, and providing data to the PCS in the synchronous fashion defined by the PMA_UNITDATA.indication message. The PMA also contains functions for PMA Carrier Sense and Link Integrity.

PMA functions and state diagrams appear in 23.4. PMA electrical specifications appear in 23.5.

23.1.5 Application of 100BASE-T4

23.1.5.1 Compatibility considerations

All implementations of the twisted-pair link shall be compatible at the MDI. The PCS, PMA, and the medium are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the PCS and PMA (in an application-dependent manner) provided the MDI (and MII, when implemented) specifications are met.

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23.1.5.2 Incorporating the 100BASE-T4 PHY into a DTE

The PCS is required when used with a DTE. The PCS provides functions necessary to the overall system operation (such as 8B6T coding) and cannot be omitted. Refer to Figure 23–1.

When the PHY is incorporated within the physical bounds of a DTE, conformance to the MII interface is optional, provided that the observable behavior of the resulting system is identical to a system with a full MII implementation. For example, an integrated PHY may incorporate an interface between PCS and MAC that is logically equivalent to the MII, but does not have the full output current drive capability called for in the MII specification.

23.1.5.3 Use of 100BASE-T4 PHY for point-to-point communication

The 100BASE-T4 PHY, in conjunction with the MAC specified in Clause 1 through Clause 4 (including parameterized values in 4.2.2 to support 100 Mb/s operation), may be used at both ends of a link for point-to-point applications between two DTEs. Such a configuration does not require a repeater. In this case each PHY may connect through an MII to its respective DTE. Optionally, either PHY (or both PHYs) may be incorporated into the DTEs without an exposed MII.

23.1.5.4 Support for Auto-Negotiation

The PMA service interface contains primitives used by the Auto-Negotiation algorithm (Clause 28) to automatically select operating modes when connected to a like device.

23.2 PCS functional specifications

The 100BASE-T4 PCS couples a Media Independent Interface (MII), as described in Clause 22, to a 100BASE-T4 Physical Medium Attachment sublayer (PMA).

At its interface with the MII, the PCS communicates via the electrical signals defined in Clause 22.

The interface between PCS and the next lower level (PMA) is an abstract message-passing interface described in 23.3. The physical realization of this interface is left to the implementer, provided the requirements of this standard, where applicable, are met.

23.2.1 PCS functions

The PCS comprises one PCS Reset function and five simultaneous and asynchronous operating functions. The PCS operating functions are PCS Transmit, PCS Receive, PCS Error Sense, PCS Carrier Sense, and PCS Collision Presence. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 23–5, shows how the five operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive, and are not shown in Figure 23–5. The management functions are specified in Clause 30. See also Figure 23–6, which defines the structure of frames passed from PCS to PMA. See also Figure 23–7, which presents a reference model helpful for understanding the definitions of PCS Transmit function state variables ohr1-4 and tsr.

23.2.1.1 PCS Reset function

The PCS Reset function shall be executed any time either of two conditions occur. These two conditions are “power on” and the receipt of a reset request from the management entity. The PCS Reset function initializes

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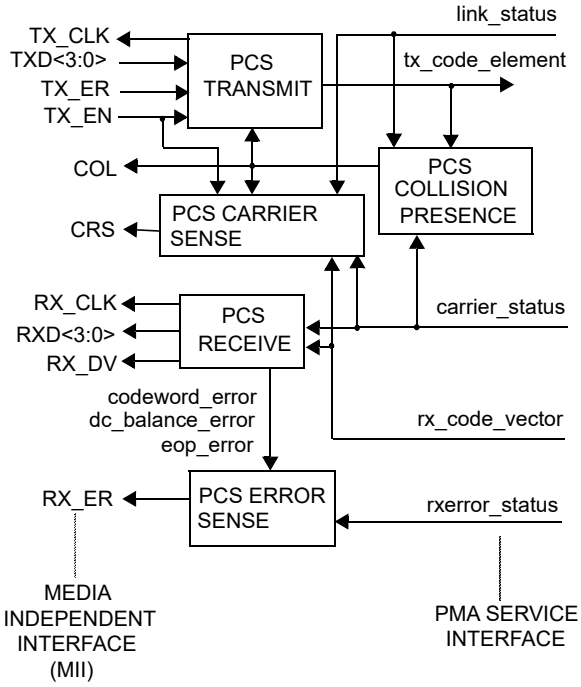

Figure 23–5—PCS reference diagram

all PCS functions. The PCS Reset function sets pcs_reset=ON for the duration of its reset function. All state diagrams take the open-ended pcs_reset branch upon execution of the PCS Reset function. The reference diagrams do not explicitly show the PCS Reset function.

23.2.1.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 23–8.

The PCS Transmit function receives nibbles from the TXD signals of the MII, assembles pairs of nibbles to form octets, converts the octets into 6T code groups according to the 8B6T code table, and passes the resulting ternary data to the PMA using the PMA_UNITDATA.request message. The state diagram of Figure 23–8 depicts the PCS Transmit function operation. Definitions of state variables tsr, ohr, sosa, sosb, eop1-5, and tx_extend used in that diagram, as well as in the following text, appear in 23.2.4.1. The physical structure represented in Figure 23–7 is not required; it merely serves to explain the meaning of the state diagram variables ohr and tsr in Figure 23–8. Implementers are free to construct any logical devices having functionality identical to that described by this functional description and the PCS Transmit state diagram, Figure 23–8.

PCS Transmit makes use of the tsr and ohr shift registers to manage nibble assembly and ternary symbol transmission. Nibbles from the MII go into tsr, which PCS Transmit reads as octets. PCS Transmit then encodes those octets and writes 6T code groups to the ohr registers. The PMA_UNITDATA.request message passes ternary symbols from the ohr registers to the PMA. In each state diagram block, the ohr loading operations are conducted first, then tx_code_vector is loaded and the state diagram waits 40 ns.

The first 5 octets assembled by the PCS Transmit function are encoded into the sosa codeword and the next 3 octets assembled are encoded into the sosb codeword. This guarantees that every packet begins with a valid preamble pattern. This is accomplished by the definition of tsr. In addition, the PCS Transmit state

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diagram also specifies that at the start of a packet all three output holding registers ohr1, ohr3 and ohr4 will be loaded with the same value (sosa). This produces the ternary symbols labeled P3 and P4 in Figure 23–6.

At the conclusion of the MAC frame, the PCS Transmit function appends eop1-5. This is accomplished by defining a variable tx_extend to stretch the TX_EN signal, and defining tsr during this time to be a sequence of constants that decodes to the proper eop code groups.

The encoding operation shall use the 8B6T code table listed in Annex 23A, and the dc balance encoding rules listed below. Encoding is performed separately for each transmit pair.

23.2.1.2.1 DC balance encoding rules

The encoding operation maintains dc balance on each transmit pair by keeping track of the cumulative weight of all 6T code groups (see *weight of 6T code group*, Annex 23A) transmitted on that pair. For each pair, it initiates the cumulative weight to 0 when the PCS Transmit function is in the AWAITING DATA TO TRANSMIT state. All 6T code groups in the code table have weight 0 or 1. The dc balance algorithm conditionally negates transmitted 6T code groups, so that the code weights transmitted on the line include 0, +1, and –1. This dc balance algorithm ensures that the cumulative weight on each pair at the conclusion of each 6T code group is always either 0 or 1, so only one bit per pair is needed to store the cumulative weight. As used below, the phrase “invert the cumulative weight bit” means “if the cumulative weight bit is zero then set it to one, otherwise set it to zero.”

After encoding any octet, except the constants sosa, sosb, eop1-5 or bad_code, update the cumulative weight bit for the affected pair according to rules a) through c):

a) If the 6T code group weight is 0, do not change the cumulative weight.
b) If the 6T code group weight is 1, and the cumulative weight bit is 0, set the cumulative weight bit to 1.
c) If the 6T code group weight is 1, and the cumulative weight bit is also 1, set the cumulative weight bit to 0, and then algebraically negate all the ternary symbol values in the 6T code group.

After encoding any of the constants sosa, sosb, or bad_code, update the cumulative weight bit for the affected pair according to rule d):

d) Do not change the cumulative weight. Never negate sosa, sosb or bad_code.

After encoding any of the constants eop1-5, update the cumulative weight bit for the affected pair according to rules e) and f):

e) If the cumulative weight is 0, do not change the cumulative weight; algebraically negate all the ternary symbol values in eop1-5.
f) If the cumulative weight is 1, do not change the cumulative weight.

NOTE—The inversion rules for eop1-5 are opposite rule b). That makes eop1-5 look very unlike normal data, increasing the number of errors required to synthesize a false end-of-packet marker.

23.2.1.3 PCS Receive function

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 23–9.

The PCS Receive function accepts ternary symbols from the PMA, communicated via the PMA_UNITDATA.indication message, converts them using 8B6T coding into a nibble-wide format and passes them up to the MII. This function also generates RX_DV. The state diagram of Figure 23–9 depicts the PCS Receive function. Definitions of state variables ih2, ih3, and ih4 used in that diagram, as well as in the following text, appear in 23.2.4.1.

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The last 6 values of the rx_code_vector are available to the decoder. PCS Receive makes use of these stored rx_code_vector values as well as the ih2-4 registers to manage the assembly of ternary symbols into 6T code groups, and the conversion of decoded data octets into nibbles. The last 6 ternary symbols for pair BI_D3 (as extracted from the last 6 values of rx_code_vector) are referred to in the state diagram as BI_D3[0:5]. Other pairs are referenced accordingly.

The PCS Receive state diagram starts the first time the PCS receives a PMA_UNITDATA.indication message with rx_code_vector=DATA (as opposed to IDLE or PREAMBLE). The contents of this first PMA_UNITDATA.indication (DATA) message are specified in 23.4.1.6.

After the sixth PMA_UNITDATA.indication (DATA) message (state DECODE CHANNEL 3), there is enough information to decode the first data octet. The decoded data is transmitted across the MII in two parts, a least significant nibble followed by a most significant nibble (see Clause 22).

During state COLLECT 4TH TERNARY SYMBOL the PCS Receive function raises RX_DV and begins shifting out the nibbles of the 802.3 MAC SFD, least significant nibble first (SFD:LO). The most significant nibble of the 802.3 MAC SFD, called SFD:HI, is sent across the MII during the next state, COLLECT 5TH TERNARY SYMBOL.

Once eop is signaled by the decode operation, the state diagram deasserts RX_DV, preventing the end-of-packet bits from reaching the MII. At any time that RX_DV is deasserted, RXD<3:0> shall be all zeros.

The decode operation shall use the 8B6T code table listed in Annex 23A, and the error-detecting rules listed in 23.2.1.3.1. Decoding and maintenance of the cumulative weight bit is performed separately for each receive pair.

23.2.1.3.1 Error-detecting rules

The decoding operation checks the dc balance on each receive pair by keeping track of the cumulative weight of all 6T code group received on that pair. For each pair, initialize the cumulative weight to 0 when the PCS Receive function is in the AWAITING INPUT state. As in the encoding operation, only one bit per pair is needed to store the cumulative weight.

Before decoding each octet, check the weight of the incoming code group and then apply rules a) through h) in sequence:

a) If the received code group is eop1 (or its negation), set eop=ON. Then check the other pairs for conformance to the end-of-packet rules as follows: Check the last four ternary symbols of the next pair, and the last two ternary symbols from the third pair for exact conformance with the end-of-packet pattern specified by PCS Transmit, including the cumulative weight negation rules. If the received data does not conform, set the internal variable eop_error=ON. Skip the other rules.
b) If the received code group weight is greater than 1 or less than –1, set the internal variable dc_balance_error=ON. Decode to all zeros. Do not change the cumulative weight.
c) If the received code group weight is zero, use the code table to decode. Do not change the cumulative weight.
d) If the received code group weight is +1, and the cumulative weight bit is 0, use the code table to decode. Invert the cumulative weight bit.
e) If the received code group weight is –1, and the cumulative weight bit is 1, algebraically negate each ternary symbol in the code group and then use the code table to decode. Invert the cumulative weight bit.
f) If the received code group weight is +1 and the cumulative weight bit is 1, set the internal variable dc_balance_error=ON. Decode to all zeros. Do not change the cumulative weight.
g) If the received code group weight is –1 and the cumulative weight bit is 0, set the internal variable dc_balance_error=ON. Decode to all zeros. Do not change the cumulative weight.

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h) If the (possibly negated) code group is not found in the code table, set codeword_error =ON. Decode to all zeros. Do not change the cumulative weight.

The variables dc_balance_error, eop_error and codeword_error shall remain OFF at all times other than those specified in the above error-detecting rules.

The codeword_error=ON indication for a (possibly negated) code group not found in the code table shall set RX_ER during the transfer of both affected data nibbles across the MII.

The dc_balance_error=ON indication for a code group shall set RX_ER during the transfer of both affected data nibbles across the MII.

The eop_error=ON indication shall set RX_ER during the transfer of the last decoded data nibble of the previous octet across the MII. That is at least one RX_CLK period earlier than the requirement for codeword_error and dc_balance_error.

These timing requirements imply consideration of implementation delays not specified in the PCS Receive state diagram.

RX_DV is asserted coincident with the transmission across the MII of valid packet data, including the Clause 4 MAC SFD, but not including the 100BASE-T4 end-of-packet delimiters eop1-5. When a packet is truncated due to early deassertion of carrier_status, an RX_ER indication shall be generated and RX_DV shall be deasserted, halting receive processing. The PCS Receive Function may use any of the existing signals codeword_error, dc_balance_error, or eop_error to accomplish this function.

23.2.1.4 PCS Error Sense function

The PCS Error Sense function performs the task of sending RX_ER to the MII whenever rxerror_status=ERROR is received from the PMA sublayer or when any of the PCS decoding error conditions occur. The PCS Error Sense function shall conform to the PCS Error Sense state diagram in Figure 23–10.

Upon detection of any error, the error sense process shall report RX_ER to the MII before the last nibble of the Clause 4 MAC frame has been passed across the MII. Errors attributable to a particular octet are reported to the MII coincident with the octet in which they occurred.

The timing of rxerror_status shall cause RX_ER to appear on the MII no later than the last nibble of the first data octet in the frame.

23.2.1.5 PCS Carrier Sense function

The PCS Carrier Sense function shall perform the function of controlling the MII signal CRS according to the rules presented in this clause.

While link_status = OK, CRS is asserted whenever rx_crs=ON or TX_EN=1, with timing as specified in 23.11.2, and Table 23-6.

23.2.1.6 PCS Collision Presence function

A PCS collision is defined as the simultaneous occurrence of tx_code_vector≠IDLE and the assertion of carrier_status=ON while link_status=OK. While a PCS collision is detected, the MII signal COL shall be asserted, with timing as specified in 23.11.2 and Table 23–7.

At other times COL shall remain deasserted.

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23.2.2 PCS interfaces

23.2.2.1 PCS–MII interface signals

The following signals are formally defined in 22.2.2. Jabber detection as specified in 22.2.4.2.14 is not required by this standard.

Table 23–1—MII interface signals

Signal name	Meaning
TX_CLK	Transmit Clock
TXD<3:0>	Transmit Data
TX_ER	Forces transmission of illegal code
TX_EN	Frames Transmit Data
COL	Collision Indication
CRS	Non-Idle Medium Indication
RX_CLK	Receive Clock
RXD<3:0>	Receive Data
RX_DV	Frames Receive SFD and DATA
RX_ER	Receive Error Indication
MDC	Management Data Clock
MDIO	Management Data

23.2.2.2 PCS–Management entity signals

The management interface has pervasive connections to all functions. Operation of the management control lines MDC and MDIO, and requirements for managed objects inside the PCS and PMA, are specified in Clause 22 and Clause 30, respectively.

The loopback mode of operation shall be implemented in accordance with 22.2.4.1.2. The loopback mode of operation loops back transmit data to receive data, thus providing a way to check for the presence of a PHY.

No spurious signals shall be emitted onto the MDI when the PHY is held in power-down mode as defined in 22.2.4.1.5 (even if TX_EN is ON) or when released from power-down mode, or when external power is first applied to the PHY.

23.2.3 Frame structure

Frames passed from the PCS sublayer to the PMA sublayer shall have the structure shown in Figure 23–6. This figure shows how ternary symbols on the various pairs are synchronized as they are passed by the PMA_UNITDATA.indication and PMA_UNITDATA.request messages. Time proceeds from left to right in the figure.

In the frame structure example, the last 6T code group, DATA N, happens to appear on transmit pair BI_D3. It could have appeared on any of the three transmit pairs, with the five words eop1 through eop5 appended afterward as the next five octets in sequence. The end of packet as recognized by the PCS is defined as the end of the last ternary symbol of eop1. At this point a receiver has gathered enough information to locate the last word in the packet and check the dc balance on each pair.

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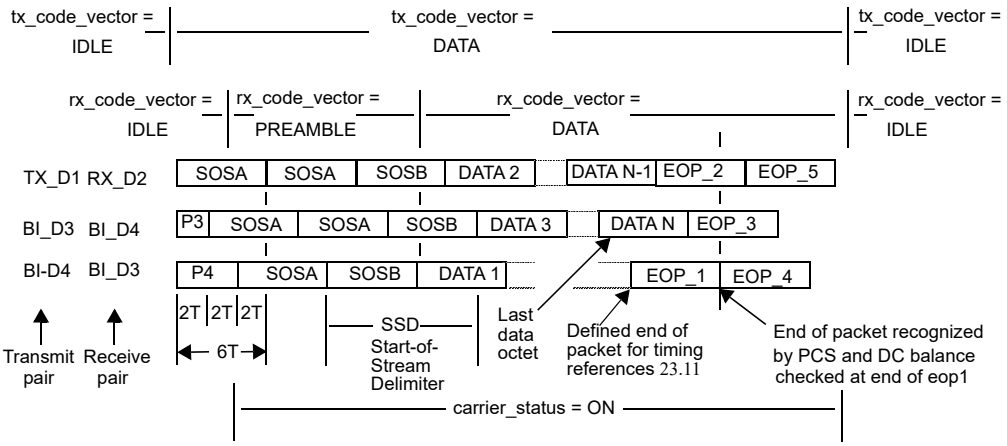

Figure 23–6—PCS sublayer to PMA sublayer frame structure

If the PMA service interface is exposed, data carried between PCS and PMA by the PMA_UNITDATA.indication and PMA_UNITDATA.request messages shall have a clock in each direction. Details of the clock implementation are left to the implementer. The choice of binary encoding for each ternary symbol is left to the implementer.

The following frame elements appear in Figure 23–6 (ternary symbols are transmitted leftmost first):

SOSA	The succession of six ternary symbols: `[ 1 -1 1 -1 1 -1]`, which is the result of encoding the constant sosa.
SOSB	The succession of six ternary symbols: `[ 1 -1 1 -1 -1 1]`, which is the result of encoding the constant sosb.
P3	The succession of two ternary symbols: `[ 1 -1]`.
P4	The succession of four ternary symbols: `[ 1 -1 1 -1]`.
DATA	A 6T code group that is the result of encoding a data octet in a packet that is not part of the Clause 4 MAC preamble or SFD.
EOP1-5	A 6T code group that is the result of encoding one of the end-of-packet patterns eop1-5.

23.2.4 PCS state diagrams

The notation used in the state diagrams follows the conventions of 21.5. Transitions shown without source states are evaluated continuously and take immediate precedence over all other conditions.

23.2.4.1 PCS state diagram constants

Register tsr may take on any of the nine constant values listed below (sosa through eop5, bad_code, and zero_code). These values are used to describe the functional operation of the coding process.

NOTE—Implementers are under no obligation to implement these constants in any particular way. For example, some implementers may choose to implement these codes as special flag bits attached to MII TXD nibble registers. Other implementers may choose to implement insertion of these codes on the downstream side of the coder function, using precoded 6T sequences.

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All 6T codewords are sent leftmost ternary symbol first.

sosa	A constant that encodes to:	[1 -1 1 -1 1 -1].
sosb	A constant that encodes to:	[1 -1 1 -1 -1 1].
eop1	A constant that encodes to:	[1 1 1 1 1 1].
eop2	A constant that encodes to:	[1 1 1 1 -1 -1].
eop3	A constant that encodes to:	[1 1 -1 -1 0 0].
eop4	A constant that encodes to:	[-1 -1 -1 -1 -1 -1].
eop5	A constant that encodes to:	[-1 -1 0 0 0 0].
bad_code	A constant that encodes to:	[-1 -1 -1 1 1 1].
zero_code	A constant that encodes to:	[0 0 0 0 0 0].

23.2.4.2 PCS state diagram variables

codeword_error

Indicates reception of invalid 6T code group.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

dc_balance_error

Indicates reception of dc coding violation.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

eop

Indicates reception of eop1.

A state variable set by the decoding operation. Reset to OFF when in PCS Receive state AWAITING INPUT. When the decoder detects eop1 on any pair, it sets this flag ON. The timing of eop shall be adjusted such that the last nibble of the last decoded data octet in a packet is the last nibble sent across the MII by the PMA Receive state diagram with RX_DV set ON.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

eop_error

Indicates reception of data with improper end-of-packet coding.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

ih2, ih4, and ih3 (input holding registers)

A set of holding registers used for the purpose of holding decoded data octets in preparation for sending across the MII one nibble at a time. One register is provided for each of the three receive pairs RX_D2, BI_D4, and BI_D3, respectively.

Value: octet

Set by: PCS Receive

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Each time the PCS Receive function decodes a 6T code group, it loads the result (an octet) into one of the ih2-4 registers. These three registers are loaded in round-robin fashion, one register being loaded every two ternary symbol times.

The PCS Receive state diagram reads nibbles as needed from the ih2-4 registers and stuffs them into RXD.

ohr1, ohr3, and ohr4 (output holding registers)

(See Figure 23–7.) A set of shift registers used for the purpose of transferring coded 6T ternary symbol groups one ternary symbol at a time into the PMA. One register is provided for each of the three transmit pairs TX_D1, BI_D3, and BI_D4, respectively.

Value: 6T code group. Each of the six cells holds one ternary symbol (i.e., –1, 0, or 1).

Set by: PCS Transmit

Each time the PCS Transmit function encodes a data octet, it loads the result (a 6T code group) into one of the ohr registers. Three registers are loaded in round-robin fashion, one register being loaded every two ternary symbol times. The PCS shall transmit octets on the three transmit pairs in round-robin fashion, in the order TX_D1, BI_D3, and BI_D4, starting with TX_D1.

The PMA_UNITDATA.request (DATA) message picks the least significant (rightmost) ternary symbol from each ohr register and sends it to the PMA, as shown below. (Note that 6T codewords in Annex 23A are listed with lsb on the left, not the right.)

tx_code_vector[TX_D1] = the LSB of ohr1, also called ohr1[0]

tx_code_vector[BI_D3] = the LSB of ohr3, also called ohr3[0]

tx_code_vector[BI_D4] = the LSB of ohr4, also called ohr4[0]

After each PMA_UNITDATA.request message, all three ohr registers shift right by one ternary symbol, shifting in zero from the left. The PCS Transmit function loads a new 6T code group into each ohr immediately after the last ternary symbol of the previous group is shifted out.

At the beginning of a preamble, the PCS Transmit function loads the same value (sosa) into all three output holding registers, which causes alternating transitions to immediately appear on all three output pairs. The result on pairs BI_D3 and BI_D4 is depicted by codewords P3 and P4 in Figure 23–6.

pcs_reset

Causes reset of all PCS functions when ON.

Values: ON and OFF

Set by: PCS Reset

rx_crs

A latched asynchronous variable. Timing for the MII signal CRS is derived from rx_crs.

Values: ON and OFF

Set ON when: carrier_status changes to ON

Set OFF when either of two events occurs:

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carrier_status changes to OFF, or
detection of eop1, properly framed, on any of the lines RX_D2, BI_D4, or BI_D3

Additionally, if, 20 ternary symbol times after rx_crs falls, carrier_status remains set to ON then set rx_crs=ON.

NOTE—A special circuit for the detection of eop1 and subsequent deassertion of rx_crs, faster than the full 8B6T decoding circuits, is generally required to meet the timing requirements for CRS listed in 23.11.

tsr (transmit shift register)

(See Figure 23–7.) A shift register defined for the purpose of assembling nibbles from the MII TXD into octets.

Values: The variable tsr always contains both the current nibble of TXD and the previous nibble of TXD. Valid values for tsr therefore include all octets. Register tsr may also take on any of the nine constant values listed in 23.2.4.1.

Nibble order: When encoding the tsr octet, the previous TXD nibble is considered the least significant nibble.

Set by: PCS Transmit

During the first 16 TX_CLK cycles after TX_EN is asserted, tsr shall assume the following values in sequence regardless of TXD: sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosb, sosb, sosb, sosb, sosb, sosb. This action substitutes the 100BASE-T4 preamble for the Clause 4 MAC preamble. The PCS Transmit state diagram samples the tsr only every other clock, which reduces the number of sosa and sosb constants actually coded to 5 and 3, respectively.

During the first 10 TX_CLK cycles after TX_EN is deasserted, tsr shall assume the following values in sequence, regardless of TXD: eop1, eop1, eop2, eop2, eop3, eop3, eop4, eop4, eop5, eop5. This action appends the 100BASE-T4 end-of-packet delimiter to each pair. The PCS Transmit state diagram samples the tsr only every other clock, which reduces the number of eop1-5 constants actually coded to 1 each.

Except for the first 16 TX_CLK cycles after TX_EN is asserted, any time TX_ER and TX_EN are asserted, tsr shall assume the value bad_code with such timing as to cause both nibbles of the affected octet to be encoded as bad_code. If TX_ER is asserted at any time during the first 16 TX_CLK cycles after TX_EN is asserted, tsr shall during the 17th and 18th clock cycles assume the value bad_code.

If TX_EN is deasserted on an odd nibble boundary, the PCS shall extend TX_EN by one TX_CLK cycle, and behave as if TX_ER were asserted during that additional cycle.

Except for the first 10 TX_CLK cycles after TX_EN is deasserted, any time TX_EN is not asserted, tsr shall assume the value zero_code.

tx_extend

A latched, asynchronous state variable used to extend the TX_EN signal long enough to ensure complete transmission of all nonzero ternary symbols in eop1-5.

Values: ON and OFF

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Set ON upon: rising edge of TX_EN

Set OFF upon: either of two conditions:
a) In the event of a collision (COL is asserted at any time during transmission) set tx_extend=OFF when TX_EN deasserts.
b) In the event of no collision (COL remains deasserted throughout transmission) set tx_extend=OFF upon completion of transmission of last ternary symbol in eop4.

NOTE 1—The 6T code group eop5 has four zeros at the end. The 6T code group eop4 contains the last non-zero ternary symbol to be transmitted.

NOTE 2—The effect of a collision, if present, is to truncate the frame at the original boundary determined by TX_EN. Noncolliding frames are extended, while colliding frames are not.

23.2.4.3 PCS state diagram timer

tw1_timer

A continuous free-running timer.

Values: The condition tw1_timer_done goes true when the timer expires.

Restart when: Immediately after expiration (restarting the timer resets condition tw1_timer_done).

Duration: 40 ns nominal.

TX_CLK shall be generated synchronous to tw1_timer (see tolerance required for TX_CLK in 23.5.1.2.10).

On every occurrence of tw1_timer_done, the state diagram advances by one block. The message PMA_UNITDATA.request is issued concurrent with tw1_timer_done.

23.2.4.4 PCS state diagram functions

encode()

The encode operation of 23.2.1.2.

Argument: octet

Returns: 6T code group

decode()

The decode operation of 23.2.1.3.

Argument: 6T code group

Returns: octet

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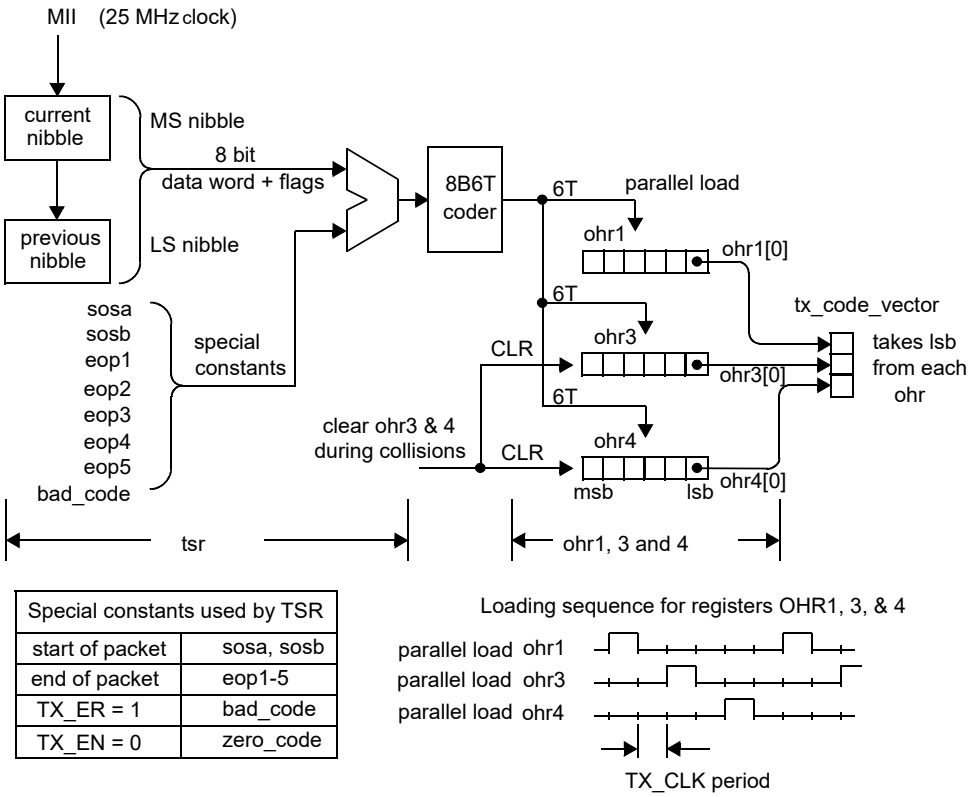

Special constants used by TSR	
start of packet	sosa, sosb
end of packet	eop1-5
TX_ER = 1	bad_code
TX_EN = 0	zero_code

Figure 23–7—PCS Transmit reference diagram

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23.2.4.5 PCS state diagrams

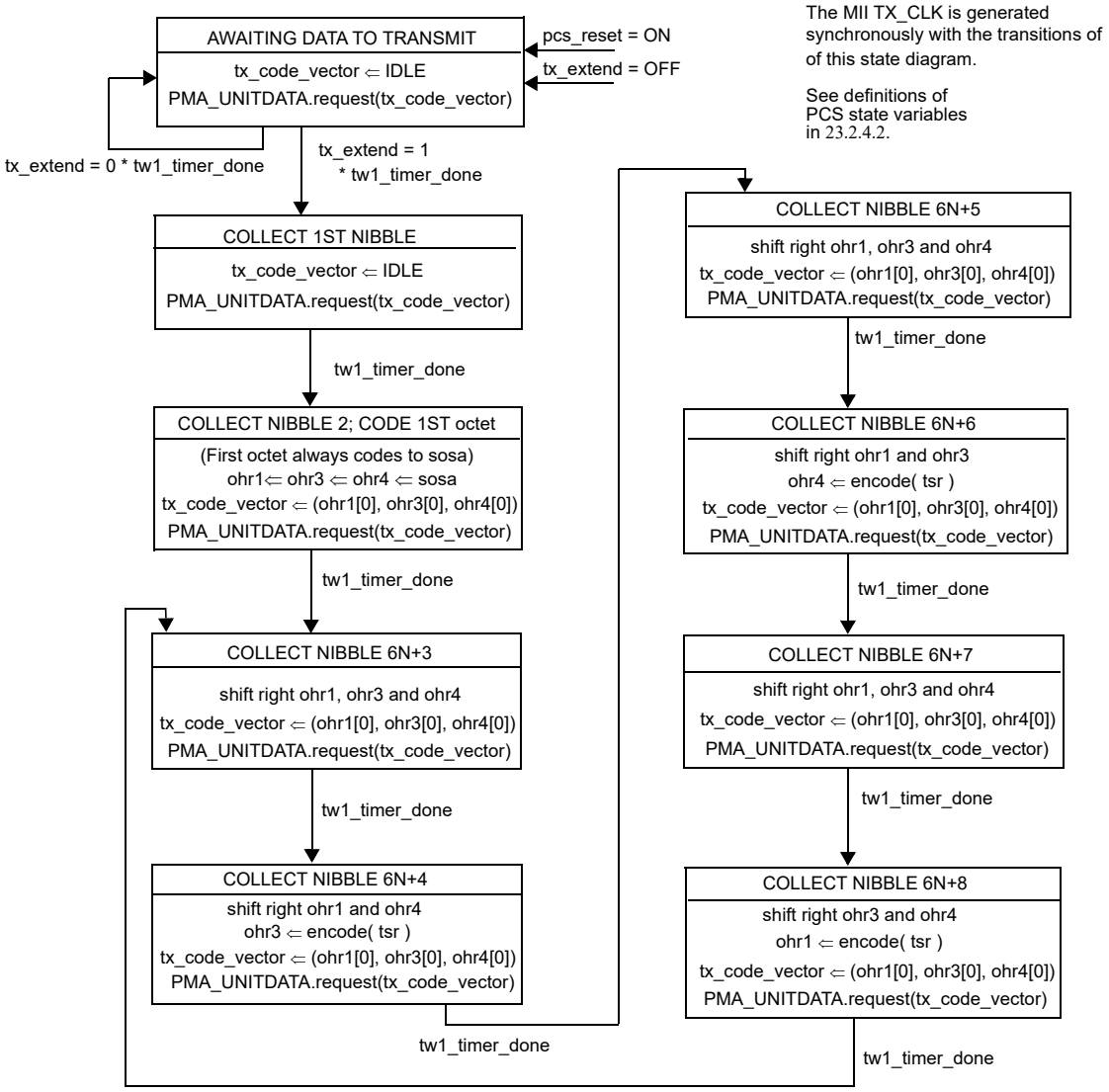

Figure 23–8—PCS Transmit state diagram

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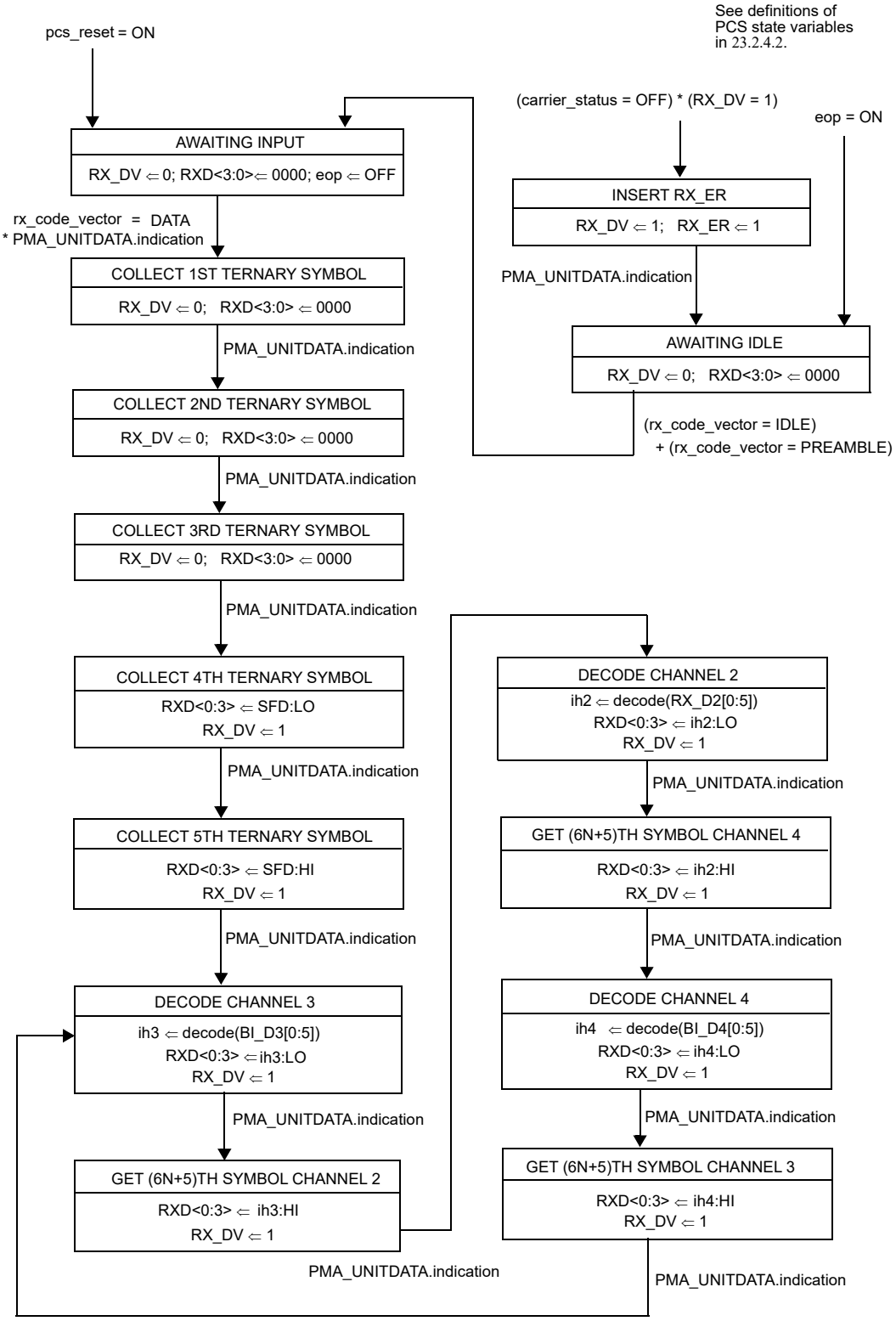

Figure 23–9—PCS Receive state diagram

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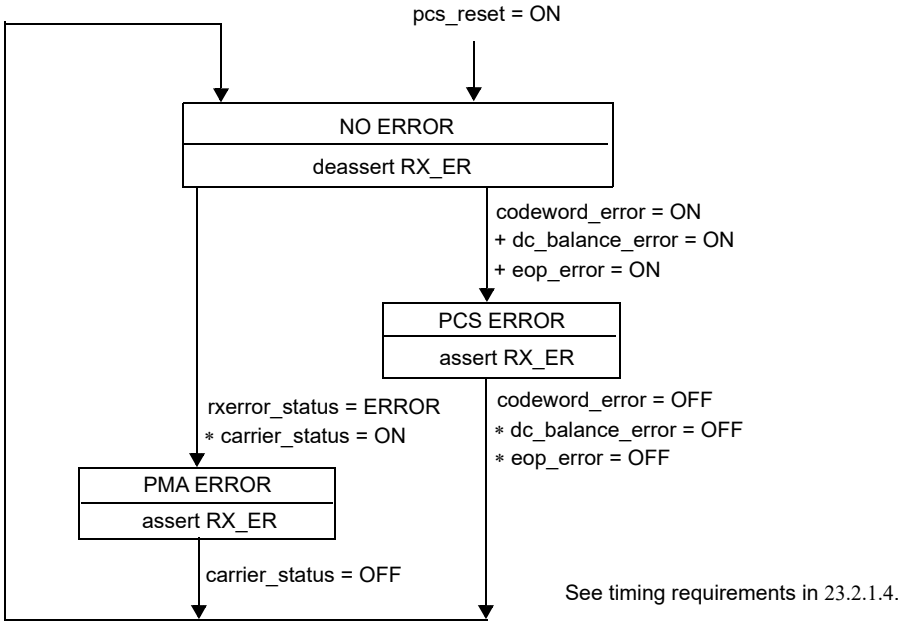

Figure 23–10—PCS Error Sense state diagram

23.2.5 PCS electrical specifications

The interface between PCS and PMA is an abstract message-passing interface, having no specified electrical properties.

Electrical characteristics of the signals passing between the PCS and MII may be found in Clause 22.

23.3 PMA service interface

This clause specifies the services provided by the PMA to either the PCS or a Repeater client. These services are described in an abstract manner and do not imply any particular implementation.

The PMA Service Interface supports the exchange of code vectors between the PMA and its client (either the PCS or a Repeater). The PMA also generates status indications for use by the client.

The following primitives are defined:

PMA_TYPE.indication

PMA_UNITDATA.request

PMA_UNITDATA.indication

PMA_CARRIER.indication

PMA_LINK.indication

PMA_LINK.request

PMA_RXERROR.indication

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23.3.1 PMA_TYPE.indication

This primitive is generated by the PMA to indicate the nature of the PMA instantiation. The purpose of this primitive is to allow clients to support connections to the various types of 100BASE-T PMA entities in a generalized manner.

23.3.1.1 Semantics of the service primitive

PMA_TYPE.indication (pma_type)

The pma_type parameter for use with the 100BASE-T4 PMA is T4.

23.3.1.2 When generated

The PMA shall continuously generate this primitive to indicate the value of pma_type.

23.3.1.3 Effect of receipt

The client uses the value of pma_type to define the semantics of the PMA_UNITDATA.request and PMA_UNITDATA.indication primitives.

23.3.2 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of tx_code_vector parameters) from the PCS or repeater to the PMA.

23.3.2.1 Semantics of the service primitive

PMA_UNITDATA.request (tx_code_vector)

When transmitting data using 100BASE-T4 signaling, the PMA_UNITDATA.request conveys to the PMA simultaneously the logical output value for each of the three transmit pairs TX_D1, BI_D3, and BI_D4. The value of tx_code_vector during data transmission is therefore a three-element vector, with one element corresponding to each output pair. Each of the three elements of the tx_code_vector may take on one of three logical values: 1, 0, or –1, corresponding to the three ternary possibilities +, 0, and - listed for each ternary symbol in the 8B6T code table (see Annex 23A).

Between packets, the 100BASE-T4 PMA layer sends the 100BASE-T4 idle signal, TP_IDL_100. The PCS informs the PMA layer that it is between packets, thus enabling the PMA idle signal, by setting the tx_code_vector parameter to IDLE.

For pma_type 100BASE-T4, the tx_code_vector parameter can take on either of two forms:

IDLE	A single value indicating to the PMA that there is no data to convey. The PMA generates link integrity pulses during the time that tx_code_vector = IDLE.
DATA	A vector of three ternary symbols, one for each of the three transmit pairs TX_D1, BI_D3, and BI_D4. The ternary symbol for each pair may take on one of three values, 1, 0, or –1.

The ternary symbols comprising tx_code_vector, when they are conveyed using the DATA format, are called, according to the pair on which each will be transmitted, tx_code_vector[BI_D4], tx_code_vector[TX_D1], and tx_code_vector[BI_D3].

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23.3.2.2 When generated

The PCS or Repeater client generates PMA_UNITDATA.request synchronous with every MII TX_CLK.

For the purposes of state diagram descriptions, it may be assumed that at the time PMA_UNITDATA.request is generated, the MII signals TX_EN, and TX_ER, and TXD instantly become valid and that they retain their values until the next PMA_UNITDATA.request.

In the state diagrams, PMA_UNITDATA.request is assumed to occur at the conclusion of each tw1 wait function.

23.3.2.3 Effect of receipt

Upon receipt of this primitive, the PMA transmits the indicated ternary symbols on the MDI.

23.3.3 PMA_UNITDATA.indication

This primitive defines the transfer of data (in the form of rx_code_vector parameters) from the PMA to the PCS or repeater during the time that link_status=OK.

23.3.3.1 Semantics of the service primitive

PMA_UNITDATA.indication (rx_code_vector)

When receiving data using 100BASE-T4 signaling, the PMA_UNITDATA.indication conveys to the PCS simultaneously the logical input value for each of the three receive pairs RX_D2, BI_D4, and BI_D3. The value of rx_code_vector during data reception is therefore a three-element vector, with one element corresponding to each input pair. Each of the three elements of the rx_code_vector may take on one of three logical values: 1, 0, or –1, corresponding to the three ternary possibilities +, 0, and – listed for each ternary symbol in the 8B6T code table (see Annex 23A).

Between packets, the rx_code_vector is set by the PMA to the value IDLE.

From the time the PMA asserts carrier_status=ON until the PMA recognizes the SSD pattern (not all of the pattern need be received in order for the PMA to recognize the pattern), the PMA sets rx_code_vector to the value PREAMBLE.

For pma_type 100BASE-T4, the rx_code_vector parameter can take on any of three forms:

IDLE	A single value indicating that the PMA has no data to convey.
PREAMBLE	A single value indicating that the PMA has detected carrier, but has not received a valid SSD.
DATA	A vector of three ternary symbols, one for each of the three receive pairs RX_D2, BI_D3, and BI_D4. The ternary symbol for each pair may take on one of three values, 1, 0, or –1.

The ternary symbols comprising rx_code_vector, when they are conveyed using the DATA format, are called, according to the pair upon which each symbol was received, rx_code_vector[BI_D3], rx_code_vector[RX_D2], and rx_code_vector[BI_D4].

23.3.3.2 When generated

The PMA shall generate PMA_UNITDATA.indication (DATA) messages synchronous with data received at the MDI.

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23.3.3.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.3.4 PMA_CARRIER.indication

This primitive is generated by the PMA to indicate the status of the signal being received from the MDI. The purpose of this primitive is to give the PCS or repeater client the earliest reliable indication of activity on the underlying medium.

23.3.4.1 Semantics of the service primitive

PMA_CARRIER.indication (carrier_status)

The carrier_status parameter can take on one of two values: OFF or ON, indicating whether the incoming signal should be interpreted as being between packets (OFF) or as a packet in progress (ON).

23.3.4.2 When generated

The PMA shall generate this primitive to indicate the value of carrier_status.

23.3.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.3.5 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium. The purpose of this primitive is to give the PCS or repeater client or Auto-Negotiation algorithm a means of determining the validity of received code elements.

23.3.5.1 Semantics of the service primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK:

FAIL	The link integrity function does not detect a valid 100BASE-T4 link.
READY	The link integrity function detects a valid 100BASE-T4 link, but has not been enabled by Auto-Negotiation.
OK	The 100BASE-T4 link integrity function detects a valid 100BASE-T4 link, and has been enabled by Auto-Negotiation.

23.3.5.2 When generated

The PMA shall generate this primitive to indicate the value of link_status.

23.3.5.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

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23.3.6 PMA_LINK.request

This primitive is generated by the Auto-Negotiation algorithm. The purpose of this primitive is to allow the Auto-Negotiation algorithm to enable and disable operation of the PHY.

23.3.6.1 Semantics of the service primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PHY reports link_status=READY if it recognizes 100BASE-T4 carrier from the far end, but no other actions are enabled.
DISABLE	Used by the Auto-Negotiation algorithm to disable PHY processing in the event fast link pulses are detected. This gives the Auto-Negotiation algorithm a chance to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions. This is the default mode if Auto-Negotiation is not present.

23.3.6.2 Default value of parameter link_control

Upon power-on, reset, or release from power-down, the link_control parameter shall revert to ENABLE. If the optional Auto-Negotiation algorithm is not implemented, no PMA_LINK.request message will arrive and the PHY will operate indefinitely with link_control=ENABLE.

23.3.6.3 When generated

The Auto-Negotiation algorithm generates this primitive to indicate to the PHY how to behave.

Upon power-on, reset, or release from power down, the Auto-Negotiation algorithm, if present, issues the message PMA_LINK.request (SCAN_FOR_CARRIER).

23.3.6.4 Effect of receipt

Whenever link_control=SCAN_FOR_CARRIER, the PHY shall enable the Link Integrity state diagram, but block passage into the state LINK_PASS, while holding rcv=DISABLE, and xmit=DISABLE. While link_control=SCAN_FOR_CARRIER, the PHY shall report link_status=READY if it recognizes 100BASE-T4 link integrity pulses coming from the far end, otherwise it reports link_status=FAIL.

Whenever link_control=DISABLE, the PHY shall report link_status=FAIL and hold the Link Integrity state diagram in the RESET state, while holding rcv=disable and xmit=DISABLE.

While link_control=ENABLE, the PHY shall allow the Link Integrity function to determine if the link is available and, if so, set rcv=ENABLE and xmit=ENABLE.

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23.3.7 PMA_RXERROR.indication

The primitive is generated in the PMA by the PMA Align function to indicate the status of the signal being received from the MDI. The purpose of this primitive is to give the PCS or repeater client an indication of a PMA detectable receive error.

23.3.7.1 Semantics of the service primitive

PMA_RXERROR.indication (rxerror_status)

The rxerror_status parameter can take on one of two values: ERROR or NO_ERROR, indicating whether the incoming signal contains a detectable error (ERROR) or not (NO_ERROR).

23.3.7.2 When generated

The PMA shall generate this primitive to indicate whether or not each incoming packet contains a PMA detectable error (23.2.1.4).

23.3.7.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.4 PMA functional specifications

The PMA couples messages from a PMA service interface (23.3) to the 100BASE-T4 baseband medium (23.6).

The interface between PCS and the baseband medium is the Medium Dependent Interface (MDI), specified in 23.7.

23.4.1 PMA functions

The PMA sublayer comprises one PMA Reset function and six simultaneous and asynchronous operating functions. The PMA operating functions are PMA Transmit, PMA Receive, PMA Carrier Sense, Link Integrity, PMA Align, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function. When the PMA is used in conjunction with a PCS, the RESET function may be shared between layers.

The PMA reference diagram, Figure 23–11, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive, and are not shown in Figure 23–11. The Management Interface and its functions are specified in Clause 22.

23.4.1.1 PMA Reset function

The PMA Reset function shall be executed any time either of two conditions occur. These two conditions are power-on and the receipt of a reset request from the management entity. The PMA Reset function initializes all PMA functions. The PMA Reset function sets pma_reset=ON for the duration of its reset function. All state diagrams take the open-ended pma_reset branch upon execution of the PMA Reset function. The reference diagrams do not explicitly show the PMA Reset function.

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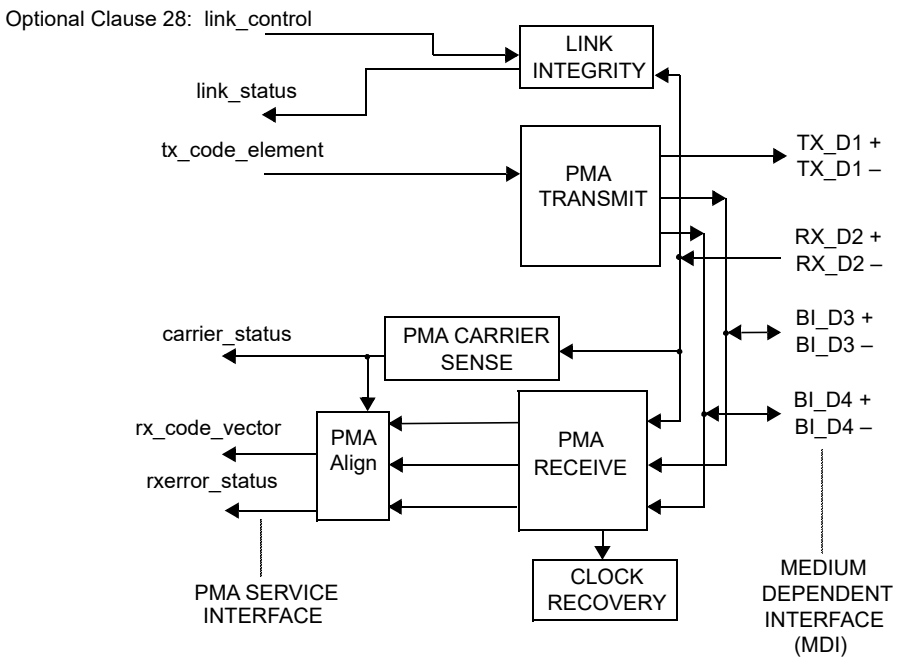

Figure 23–11—PMA reference diagram

23.4.1.2 PMA Transmit function

Except as provided for in the next paragraph, whenever (tx_code_vector=DATA)×(pma_carrier=OFF), the PMA shall transmit onto the MDI ternary symbols on pairs TX_D1, BI_D3, and BI_D4 equal to tx_code_vector[TX_D1], tx_code_vector[BI_D3], and tx_code_vector[BI_D4], respectively.

Whenever (tx_code_vector=DATA)×(pma_carrier=ON), the PMA shall transmit onto the MDI ternary symbols on pairs TX_D1, BI_D3, and BI_D4 equal to tx_code_vector[TX_D1], CS0, and CS0, respectively, and continue doing so until tx_code_vector=IDLE.

NOTE—This shuts off the transmitters on channels BI_D3 and BI_D4, and keeps them off, in the event of a collision. Shutting off the transmitters prevents overload and saturation of the transmitters, and also reduces the amount of near-end crosstalk present while monitoring for the end of carrier.

Whenever tx_code_vector=IDLE, an idle signal shall be transmitted on pair TX_D1 and silence on pairs BI_D3 and BI_D4. The idle signal consists of periods of silence (times where the differential output voltage remains at 0 mV ± 50 mV) broken by the transmission of link integrity test pulses.

The 100BASE-T4 idle signal is similar to the 10BASE-T idle signal, but with 100BASE-T4 ternary signal levels and a faster repetition rate. The 100BASE-T4 idle signal is called TP_IDL_100. The TP_IDL_100 signal shall be a repeating sequence formed from one 1.2 ms ± 0.6 ms period of silence (the time where the differential voltage remains at 0 mV ± 50 mV) and one link test pulse. Each link test pulse shall be a succession of two ternary symbols having logical values of –1 and 1 transmitted on pair TX_D1 using CS-1 and CS1 as defined in 23.4.3.1. Following a packet, the TP_IDL_100 shall start with a period of silence.

Transmission of TP_IDL_100 may be terminated at any time with respect to the link test pulse. It shall be terminated such that ternary symbols of the subsequent packet are not corrupted, and are not delayed any more than is specified in 23.11.

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For any link test pulse occurring within 20 ternary symbol times of the beginning of a preamble, the zero crossing jitter (as defined in 23.5.1.2.5) of the link test pulse when measured along with the zero crossings of the preamble shall be less than 4 ns p-p.

NOTE—The above condition allows clock recovery implementations that optionally begin fast-lock sequences on part of a link integrity pulse to properly acquire lock on a subsequent preamble sequence.

Regardless of other considerations, when the transmitter is disabled (xmit=DISABLE), the PMA Transmit function shall transmit the TP_IDL_100 signal.

23.4.1.3 PMA Receive function

PMA Receive contains the circuits necessary to convert physically encoded ternary symbols from the physical MDI receive pairs (RX_D2, BI_D3 and BI_D4) into a logical format suitable for the PMA Align function. Each receive pair has its own dedicated PMA Receive circuitry.

The PHY shall receive the signals on the receive pairs (RX_D2, BI_D3, and BI_D4) and translate them into one of the PMA_UNITDATA.indication parameters IDLE, PREAMBLE, or DATA with a ternary symbol error ratio of less than one part in 10^8.

If both pma_carrier=ON and tx_code_vector=DATA, the value of rx_code_vector is unspecified until pma_carrier=OFF.

23.4.1.4 PMA Carrier Sense function

The PMA Carrier Sense function shall set pma_carrier=ON upon reception of the following pattern on pair RX_D2 at the receiving MDI, as measured using a 100BASE-T4 transmit test filter (23.5.1.2.3):

> Any signal greater than 467 mV, followed by any signal less than –225 mV, followed by any signal greater than 467 mV, all three events occurring within 2 ternary symbol times.

The operation of carrier sense is undefined for signal amplitudes greater than 4.5 V.

See 23.5.1.3.2 for a list of signals defined *not* to set pma_carrier=ON.

After asserting pma_carrier=ON, PMA Carrier Sense shall set pma_carrier=OFF upon receiving either of these conditions:

a) Seven consecutive ternary symbols of value CS0 on pair RX_D2.
b) (tx_code_vector=DATA) has not been true at any time since pma_carrier was asserted, *and* the 6T code group eop1 has been received, properly framed, on any of the lines RX_D2, BI_D4, or BI_D3, *and* enough time has passed to assure passage of all ternary symbols of eop4 across the PMA service interface.

NOTE—Designers may wish to take advantage of the fact that the minimum received packet fragment will include at least 24 ternary symbols of data on pair RX_D2. Therefore, once carrier is activated, it is not necessary to begin searching for seven consecutive zeros until after the 24th ternary symbol has been received. During the time that the first 24 ternary symbols are being received, the near-end crosstalk from pairs BI_D3 and BI_D4, which are switched off during collisions, decays substantially.

While rcv=ENABLE, the PMA CARRIER function shall set carrier_status = pma_carrier.

While rcv≠ENABLE, the PMA CARRIER function shall set carrier_status = OFF.

This function operates independently of the Link Integrity function.

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23.4.1.5 Link Integrity function

Link Integrity provides the ability to protect the network from the consequences of failure of the simplex link attached to RX_D2. While such a failure is present, transfer of data by the Transmit and Receive functions is disabled.

Link Integrity observes the incoming wire pair, RX_D2, to determine whether the device connected to the far end is of type 100BASE-T4. Based on its observations, Link Integrity sets two important internal variables:

a) pma_type variable is set to 100BASE-T4.
b) link_status variable is a parameter sent across the PMA Service interface.

The Link Integrity function shall comply with the state diagram of Figure 23–12.

Four conditions gate the progression of states toward LINK_PASS: (1) reception of at least 31 link integrity test pulses; (2) reception of at least 96 more link integrity test pulses, or reception of carrier; (3) cessation of carrier, if it was present; (4) detection of equals link_control ENABLE.

While the PMA is not in the LINK_PASS state, the Link Integrity function sets rcv=DISABLE and xmit=DISABLE, thus disabling the bit transfer of the Transmit and Receive functions.

If a visible indicator is provided on the PHY to indicate the link status, it is recommended that the color be green and that the indicator be labeled appropriately. It is further recommended that the indicator be on when the PHY is in the LINK_PASS state and off otherwise.

23.4.1.6 PMA Align function

The PMA Align function accepts received ternary symbols from the PMA Receive function, along with pma_carrier. PMA Align is responsible for realigning the received ternary symbols to eliminate the effects of unequal pair propagation time, commonly called pair skew. PMA Align also looks for the SSD pattern to determine the proper alignment of 6T code groups, and then forwards PMA_UNITDATA.indication (DATA) messages to the PCS. The SSD pattern includes referencing patterns on each of the three receive lines that may be used to establish the proper relationship of received ternary symbols (see Figure 23–6).

NOTE—The skew between lines is not expected to change measurably from packet to packet.

At the beginning of each received frame, the PMA Carrier Sense function asserts pma_carrier=ON. During the preamble, the Clock Recovery function begins synchronizing its receive clock. Until clock is synchronized, data coming from the low-level PMA Receive function is meaningless. The PMA Align function is responsible for waiting for the receiver clock to stabilize and then properly recognizing the 100BASE-T4 coded SSD pattern. The PMA Align function shall send PMA_UNITDATA.indication (PREAMBLE) messages to the PCS from the time pma_carrier=ON is asserted until the PMA is ready to transfer the first PMA_UNITDATA.indication (DATA) message. Once the PMA Align function locates a SSD pattern, it begins forwarding PMA_UNITDATA.indication (DATA) messages to the PCS, starting with the first ternary symbol of the first data word on pair BI_D3, as defined in Figure 23–6. This first PMA_UNITDATA.indication (DATA) message shall transfer the following ternary symbols, as specified in the frame structure diagram, Figure 23–6:

rx_code_vector[BI_D3]first ternary symbol of first data code group

rx_code_vector[RX_D2]second ternary symbol prior to start of second data code group

rx_code_vector[BI_D4]fourth ternary symbol prior to start of third data code group

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PMA Align shall continue sending PMA_UNITDATA.indication (DATA) messages until pma_carrier=OFF. While pma_carrier=OFF, PMA Align shall emit PMA_UNITDATA.indication (IDLE) messages.

If no valid SSD pattern is recognized within 22 ternary symbol times of the assertion of pma_carrier=ON, the PMA Align function shall set rxerror_status=ERROR. The PMA Align function is permitted to begin sending PMA_UNITDATA.indication (DATA) messages upon receipt of a partially recognized SSD pattern, but it is required to set rxerror_status=ERROR if the complete SSD does not match perfectly the expected ternary symbol sequence. Rxerror_status shall be reset to NO_ERROR when pma_carrier=OFF.

The PMA Align function is permitted to use the first received packet of at least minimum size after RESET or the transition to LINK_PASS to learn the nominal skew between pairs, adjust its equalizer, or perform any other initiation functions. During this first packet, the PMA Align function shall emit PMA_UNITDATA.indication (PREAMBLE) messages, but may optionally choose to never begin sending PMA_UNITDATA.indication (DATA) messages.

The PMA Align function shall tolerate a maximum skew between any two pairs of 60 ns in either direction without error.

To protect the network against the consequences of mistaken packet framing, the PMA Align function shall detect the following error and report it by setting rxerror_status=ERROR (optionally, those error patterns already detected by codeword_error, dc_balance_error, or eop_error do not also have to be detected by rxerror_status): *In a series of good packets, any one packet that has been corrupted with three or fewer ternary symbols in error causing its sosb 6T code groups on one or more pairs to appear in the wrong location.*

Several approaches are available for meeting this requirement, including, but not limited to, a) comparing the relative positions of sosb 6T code groups on successive packets; b) measuring the time between the first preamble pulse and reception of sosb on each pair; c) counting the number of zero crossings from the beginning of the preamble until sosb; and d) monitoring for exception strings like “11” and “–1–1–1” in conjunction with one or more of the above techniques.

Regardless of other considerations, when the receive function is disabled (rcv=DISABLE), the PMA Align function shall emit PMA_UNITDATA.indication (IDLE) messages and no others.

23.4.1.7 Clock Recovery function

The Clock Recovery function couples to all three receive pairs. It provides a synchronous clock for sampling each pair. While it may not drive the MII directly, the Clock Recovery function is the underlying root source of RX_CLK.

The Clock Recovery function shall provide a clock suitable for synchronously decoding ternary symbols on each line within the bit error tolerance provided in 23.4.1.3. During each preamble, in order to properly recognize the frame delimiting pattern formed by codeword sosb on each pair, the received clock signal has to be stable and ready for use in time to decode the following ternary symbols: the 16th ternary symbol of pair RX_D2, the 18th ternary symbol of pair BI_D4, and the 14th ternary symbol of pair BI_D3.

23.4.2 PMA interface messages

The messages between the PMA and PCS are defined above in 23.3, PMA Service Interface. Communication between a repeater unit and PMA also uses the PMA Service Interface. Communication through the MDI is summarized in Tables 23–2 and 23–3.

TP_IDL_100 is defined in 23.4.1.2. The waveforms used to convey CS1, CS0, and CS-1 are defined in 23.5.1.2.

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Table 23–2—MDI signals transmitted by the PHY

Signal	Allowed pair	Meaning
CS1	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol 1. Nominal voltage level +3.5 V.
CS0	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol 0. Nominal voltage level 0 V.
CS-1	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol –1. Nominal voltage level –3.5 V.
TP_IDL_100	TX_D1	Idle signal. Indicates transmitter is currently operating at 100 Mb/s.

Table 23–3—Signals received at the MDI

Signal	Allowed pair	Meaning
CS1	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol 1. Nominal transmitted voltage level +3.5 V.
CS0	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol 0. Nominal transmitted voltage level 0 V.
CS-1	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol –1. Nominal transmitted voltage level –3.5 V.
TP_IDL_100	RX_D2	Idle signal. Indicates transmitter is currently operating at 100 Mb/s.

TP_IDL_100 is defined in 23.4.1.2. The encodings for CS1, CS0, and CS-1 are defined in 23.5.1.2.

Re-timing of CS1, CS0, and CS-1 signals within the PMA is required.

23.4.3 PMA state diagrams

The notation used in the state diagrams follows the conventions of 21.5. Transitions shown without source states are evaluated continuously and take immediate precedence over all other conditions.

23.4.3.1 PMA constants

CS0

A waveform that conveys the ternary symbol 0.

Value: CS0 has a nominal voltage of 0 V. See 23.5.1.2.

CS1

A waveform that conveys the ternary symbol 1.

Value: CS1 has a nominal peak voltage of +3.5 V. See 23.5.1.2.

CS-1

A waveform that conveys the ternary symbol –1.

Value: CS-1 has a nominal peak voltage of –3.5 V. See 23.5.1.2.

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link_100_max

A constant.

Value: Greater than 5.0 ms and less than 7.0 ms.

Used by link_max_timer to detect the absence of 100BASE-T4 link test pulses on pair RX_D2.

link_100_min

A constant.

Value: Greater than 0.15 ms and less than 0.45 ms.

Used by cnt_link to detect link test pulses on pair RX_D2 that are too close together to be valid 100BASE-T4 link test pulses.

23.4.3.2 State diagram variables

pma_reset

Causes reset of all PCS functions.

Values: ON and OFF

Set by: PMA Reset

pma_carrier

A version of carrier_status used internally by the PMA sublayer. The variable pma_carrier always functions regardless of the link status. The value of pma_carrier is passed on through the PMA service interface as carrier_status when rcv=ENABLE. At other times, the passage of pma_carrier information to the PMA service interface is blocked.

Values: ON, OFF

Set by: PMA CARRIER

rcv

Controls the flow of data from the PMA to PCS through the PMA_UNITDATA.indication message.

Values: ENABLE (receive is enabled)
DISABLE (the PMA always sends PMA_UNITDATA.indication (IDLE), and carrier_status is set to OFF)

xmit

Controls the flow of data from PCS to PMA through the PMA_UNITDATA.request message.

Values: ENABLE (transmit is enabled)
DISABLE (the PMA interprets all PMA_UNITDATA.request messages as PMA_UNITDATA.request (IDLE). The PMA transmits no data, but continues sending TP_IDL_100).

23.4.3.3 State diagram timers

link_max_timer

A re-triggerable timer.

Values: The condition link_max_timer_done goes true when the timer expires.

Restart when: Timer is restarted for its full duration by every occurrence of either a link test pulse on pair RX_D2 or the assertion of pma_carrier=ON (restarting the timer

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resets the condition link_max_timer_done).

Duration: link_100_max

Used by Link Integrity to detect the absence of 100BASE-T4 link test pulses on pair RX_D2.

23.4.3.4 State diagram counters

cnt_link

Counts number of 100BASE-T4 link test pulses (see 23.5.1.3.1) received on pair RX_D2.

Values: nonnegative integers

Reset to zero: On either of two conditions:

a) While in any state other than LINK_PASS, reset counter to zero if successive link test pulses are received within link_100_min.
b) While in any state, reset to zero if link_max_timer expires.

While in the LINK_PASS state, ignore pulses received within link_100_min (i.e., do not count them).

23.4.3.5 Link Integrity state diagram

The Link Integrity state diagram is shown in Figure 23–12.

23.5 PMA electrical specifications

This clause defines the electrical characteristics of the PHY at the MDI.

The ground reference point for all common-mode tests is the MII ground circuit. Implementations without an MII use the chassis ground. The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

23.5.1 PMA-to-MDI interface characteristics

23.5.1.1 Isolation requirement

NOTE—Since September 2003, maintenance changes are no longer being considered for this clause. Since February 2021, electrical isolation requirements are in J.1.

The PHY shall provide electrical isolation between the DTE, or repeater circuits including frame ground, and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in subclause 5.3.2 of IEC 60950: 1991.
b) 2250 Vdc for 60 s, applied as specified in subclause 5.3.2 of IEC 60950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in subclause 5.3.2 of IEC 60950: 1991, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

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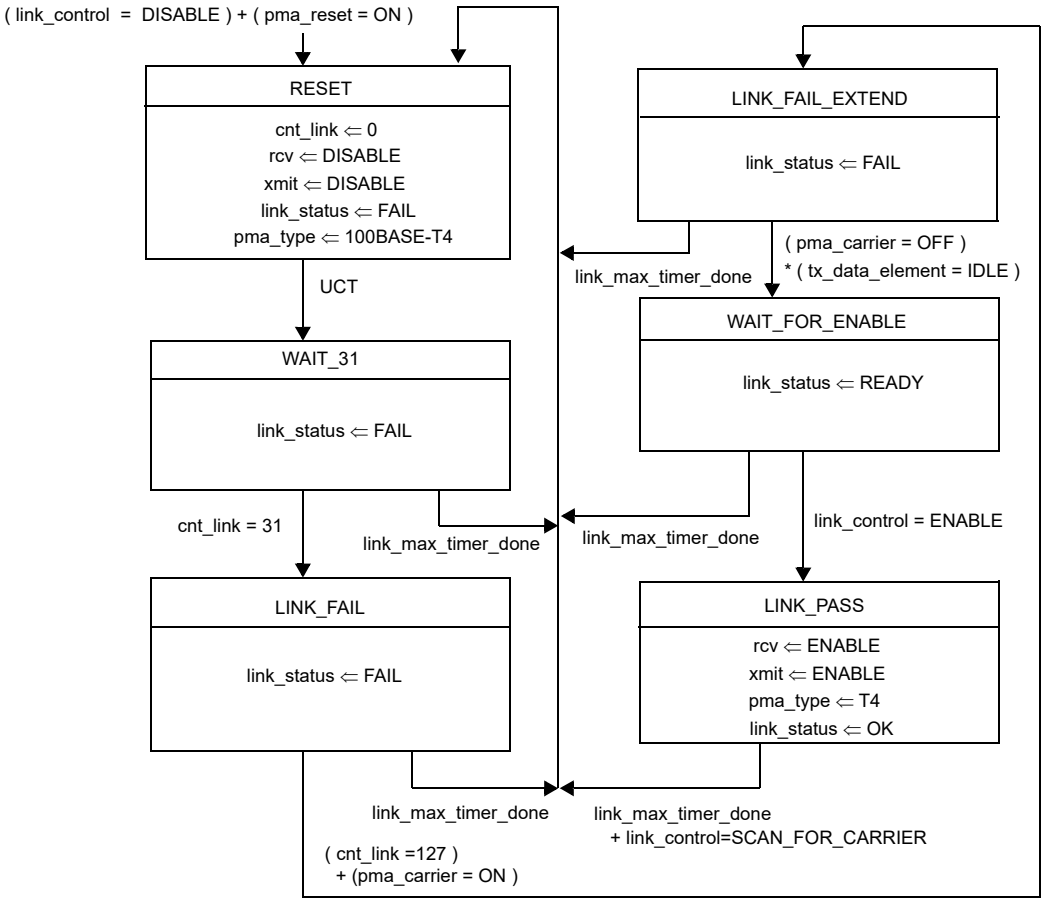

NOTE—The variables link_control and link_status are designated as link_control_[T4] and link_status_[T4], respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

Figure 23–12—Link Integrity state diagram

23.5.1.2 Transmitter specifications

The PMA shall provide the Transmit function specified in 23.4.1.2 in accordance with the electrical specifications of this clause.

Where a load is not specified, the transmitter shall meet requirements of this clause when each transmit output is connected to a differentially connected 100 Ω resistive load.

23.5.1.2.1 Peak differential output voltage

While repetitively transmitting the ternary sequence [0 0 1 0 0 0 0 0 −1 0 0 0] (leftmost ternary symbol first), and while observing the differential transmitted output at the MDI, for any pair, with no intervening cable, the absolute value of both positive and negative peaks shall fall within the range of 3.15 V to 3.85 V (3.5 V ± 10%).

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23.5.1.2.2 Differential output templates

While repetitively transmitting the ternary sequence [0 0 1 0 0 0 0 0 −1 0 0 0], and while observing the transmitted output at the MDI, the observed waveform shall fall within the normalized transmit template listed in Table 23–4. Portions of this table are represented graphically in Figure 23–13. The entire normalized transmit template shall be scaled by a single factor between 3.15 and 3.85. It is a functional requirement that linear interpolation be used between points. The template time axis may be shifted horizontally to attain the most favorable match. In addition to this simple test pattern, all other pulses, including link integrity pulses and also including the first pulse of each packet preamble, should meet this same normalized transmit template, with appropriate shifting and linear superposition of the CS1 and CS-1 template limits. Transmitters are allowed to insert additional delay in the transmit path in order to meet the first pulse requirement, subject to the overall timing limitations listed in 23.11, Timing summary.

While transmitting the TP_IDL_100 signal, and while observing the transmitted output at the MDI, the observed waveform shall fall within the normalized link pulse template listed in Table 23–4. Portions of this table are represented graphically in Figure 23–14. The entire template shall be scaled by the same factor used for the normalized transmit template test. It is a functional requirement that linear interpolation be used between template points. The template time axis may be shifted horizontally to attain the most favorable match.

After transmitting seven or more consecutive CS0 waveforms during the TP_IDL_100 signal, each pair, as observed using the 100BASE-T4 Transmit Test Filter (23.5.1.2.3) connected to the MDI, shall attain a state within 50 mV of zero.

When the TX_D1, BI_D3, or BI_D4 pair is driven with a repeating pattern (1 −1 1 −1 ...) any harmonic measured at the MDI output shall be at least 27 dB below the fundamental at 12.5 MHz.

NOTE 1—The specification on maximum spectral components is not intended to ensure compliance with regulations concerning RF emissions. The implementer should consider any applicable local, national, or international regulations. Additional filtering of spectral components may therefore be necessary.

NOTE 2—The repetitive pattern [0 0 1 0 0 0 0 0 −1 0 0 0] (leftmost ternary symbol first) may be synthesized using the 8B6T coding rules from a string of repeating data octets with value 73 hex. The repetitive pattern [1 −1 1 −1 1 −1] (leftmost ternary symbol first) may be synthesized using the 8B6T coding rules from a string of repeating data octets with value 92 hex.

The ideal template values may be automatically generated from the following equations:

Laplace transform of
Ideal transmit response $$IdealResponse(s) = \frac{Ideal(s)}{LPF(s)}$$

Where $Ideal(s)$ is a 100% raised cosine system response

Where $LPF(s)$ is a 3-pole Butterworth low pass filter response with –3 dB point at 25 MHz

Convert *IdealResponse(s)* from frequency domain to time domain

Use at least 8 samples per ternary symbol for the conversion

Superimpose alternating positive and negative copies of the ideal time response, separated by 6 ternary symbol times, to form the ideal transmit voltage waveform.

The template limits are formed by offsetting the ideal transmit voltage waveform by plus and minus 6% of its peak.

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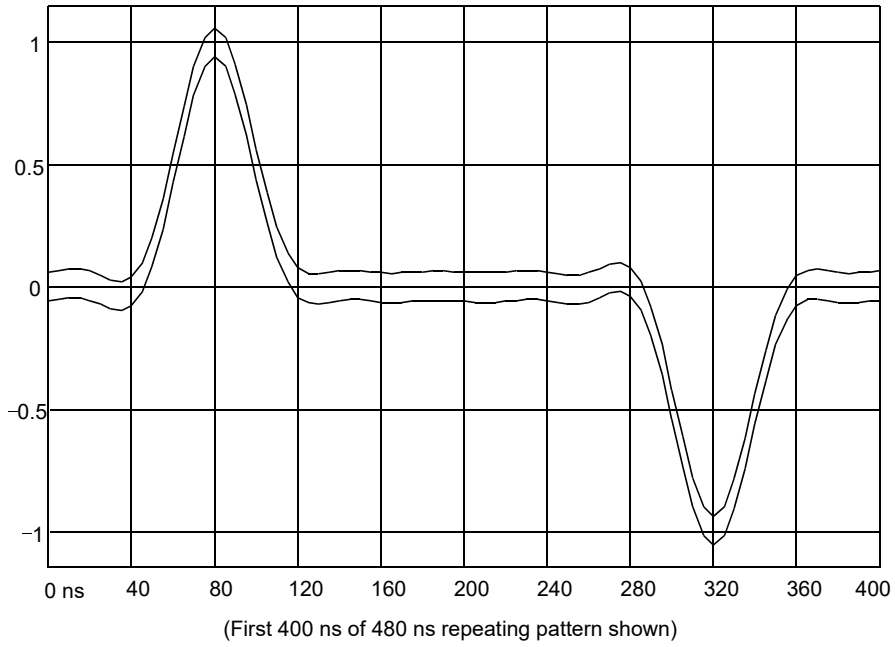

Figure 23–13—Normalized transmit template as measured at MD

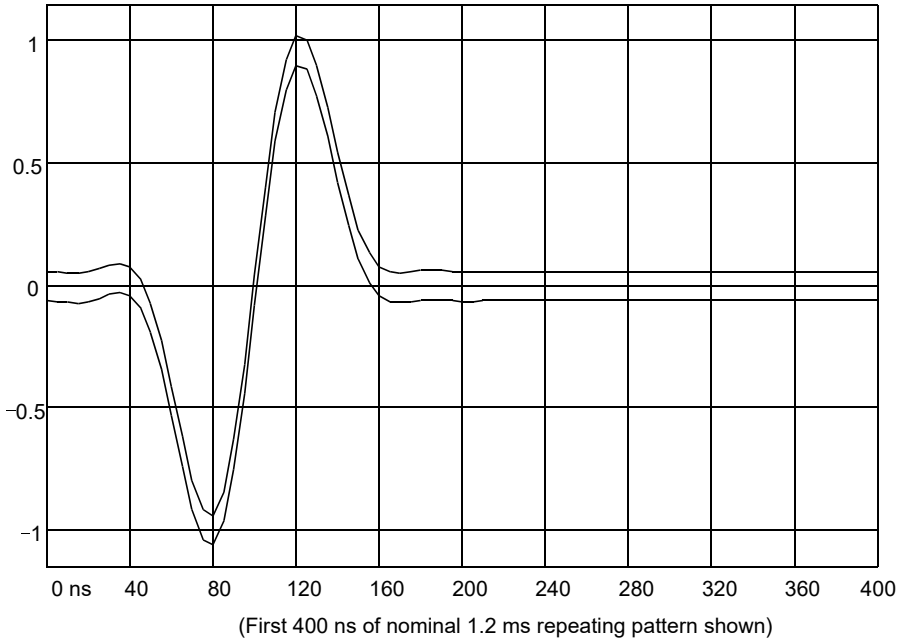

Figure 23–14—Normalized link pulse template as measured at MDI

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Table 23–4—Normalized voltage templates as measured at the MDI

Time, ns	Normalized transmit template, pos. limit	Normalized transmit template, neg. limit	Normalized link template, pos. limit	Normalized link template, neg. limit
0	0.060	–0.061	0.061	–0.060
5	0.067	–0.054	0.056	–0.065
10	0.072	–0.049	0.052	–0.069
15	0.072	–0.049	0.052	–0.069
20	0.063	–0.058	0.058	–0.063
25	0.047	–0.074	0.071	–0.050
30	0.030	–0.091	0.086	–0.035
35	0.023	–0.098	0.094	–0.027
40	0.041	–0.080	0.080	–0.041
45	0.099	–0.022	0.027	–0.094
50	0.206	0.085	–0.076	–0.197
55	0.358	0.237	–0.231	–0.352
60	0.544	0.423	–0.428	–0.549
65	0.736	0.615	–0.640	–0.761
70	0.905	0.784	–0.829	–0.950
75	1.020	0.899	–0.954	–1.075
80	1.060	0.940	–0.977	–1.098
85	1.020	0.899	–0.876	–0.997
90	0.907	0.786	–0.653	–0.774
95	0.744	0.623	–0.332	–0.453
100	0.560	0.439	0.044	–0.077
105	0.384	0.263	0.419	0.298
110	0.239	0.118	0.738	0.617
115	0.137	0.016	0.959	0.838
120	0.077	–0.044	1.060	0.940
125	0.053	–0.068	1.044	0.923
130	0.050	–0.071	0.932	0.811
135	0.057	–0.064	0.759	0.638
140	0.064	–0.057	0.565	0.444
145	0.067	–0.054	0.383	0.262
150	0.065	–0.056	0.238	0.117
155	0.061	–0.060	0.138	0.017
160	0.057	–0.064	0.081	–0.040
165	0.055	–0.066	0.057	–0.064

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Table 23–4—Normalized voltage templates as measured at the MDI *(continued)*

Time, ns	Normalized transmit template, pos. limit	Normalized transmit template, neg. limit	Normalized link template, pos. limit	Normalized link template, neg. limit
170	0.056	–0.065	0.054	–0.067
175	0.059	–0.062	0.058	–0.063
180	0.062	–0.059	0.063	–0.058
185	0.064	–0.057	0.064	–0.057
190	0.064	–0.057	0.063	–0.058
195	0.062	–0.059	0.060	–0.061
200	0.060	–0.061	0.058	–0.063
205	0.057	–0.064	0.058	–0.063
210	0.056	–0.065	0.059	–0.062
215	0.058	–0.063	0.060	–0.061
220	0.061	–0.060	0.062	–0.059
225	0.064	–0.057	0.062	–0.059
230	0.066	–0.055	0.062	–0.059
235	0.065	–0.056	0.061	–0.060
240	0.061	–0.060	0.060	–0.061
245	0.054	–0.067	0.060	–0.061
250	0.049	–0.072	0.060	–0.061
255	0.049	–0.072	0.060	–0.061
260	0.058	–0.063	0.061	–0.060
265	0.074	–0.047	0.061	–0.060
270	0.091	–0.030	0.061	–0.060
275	0.099	–0.022	0.061	–0.060
280	0.080	–0.041	0.060	–0.061
285	0.022	–0.099	0.060	–0.061
290	–0.085	–0.206	0.060	–0.061
295	–0.238	–0.359	0.060	–0.061
300	–0.423	–0.544	0.061	–0.060
305	–0.615	–0.736	0.061	–0.060
310	–0.783	–0.904	0.061	–0.060
315	–0.899	-1.020	0.061	–0.060
320	–0.940	-1.061	0.060	–0.061
325	–0.899	-1.020	0.060	–0.061
330	–0.786	–0.907	0.060	–0.061
335	–0.623	–0.744	0.060	–0.061

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Table 23–4—Normalized voltage templates as measured at the MDI *(continued)*

Time, ns	Normalized transmit template, pos. limit	Normalized transmit template, neg. limit	Normalized link template, pos. limit	Normalized link template, neg. limit
340	–0.439	–0.560	0.061	–0.060
345	–0.263	–0.384	0.061	–0.060
350	–0.118	–0.239	0.061	–0.060
355	–0.016	–0.137	0.061	–0.060
360	0.044	–0.077	0.060	–0.061
365	0.068	–0.053	0.060	–0.061
370	0.070	–0.051	0.060	–0.061
375	0.064	–0.057	0.060	–0.061
380	0.057	–0.064	0.061	–0.060
385	0.054	–0.067	0.061	–0.060
390	0.056	–0.065	0.061	–0.060
395	0.060	–0.061	0.061	–0.060
400	0.064	–0.057	0.060	–0.061
405	0.065	–0.056	0.060	–0.061
410	0.064	–0.057	0.060	–0.061
415	0.061	–0.060	0.060	–0.061
420	0.059	–0.062	0.061	–0.060
425	0.058	–0.063	0.061	–0.060
430	0.059	–0.062	0.061	–0.060
435	0.060	–0.061	0.061	–0.060
440	0.061	–0.060	0.060	–0.061
445	0.062	–0.059	0.060	–0.061
450	0.062	–0.059	0.060	–0.061
455	0.061	–0.060	0.060	–0.061
460	0.060	–0.061	0.061	–0.060
465	0.059	–0.062	0.061	–0.060
470	0.060	–0.061	0.061	–0.060
475	0.060	–0.061	0.061	–0.060
480	0.061	–0.060	0.060	–0.061

23.5.1.2.3 Differential output ISI (intersymbol interference)

While observing a pseudo-random 8B6T coded data sequence (with every 6T code group represented at least once) preceded by at least 128 octets and followed by at least 128 octets of data, and while observing the transmitted output through a 100BASE-T4 Transmit Test Filter (one implementation of which is

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depicted in Figure 23–16), the ISI shall be less than 9%. The ISI for this test is defined by first finding the largest of the three peak-to-peak ISI error voltages marked in Figure 23–15 as TOP ISI, MIDDLE ISI, and BOTTOM ISI.

The largest of these peak-to-peak ISI error voltages is then divided by the overall peak-to-peak signal voltage. (The technique of limiting the ratio of worst ISI to overall peak-to-peak voltage at 9% accomplishes the same end as limiting the ratio of worst ISI to nominal peak-to-peak at 10%.)

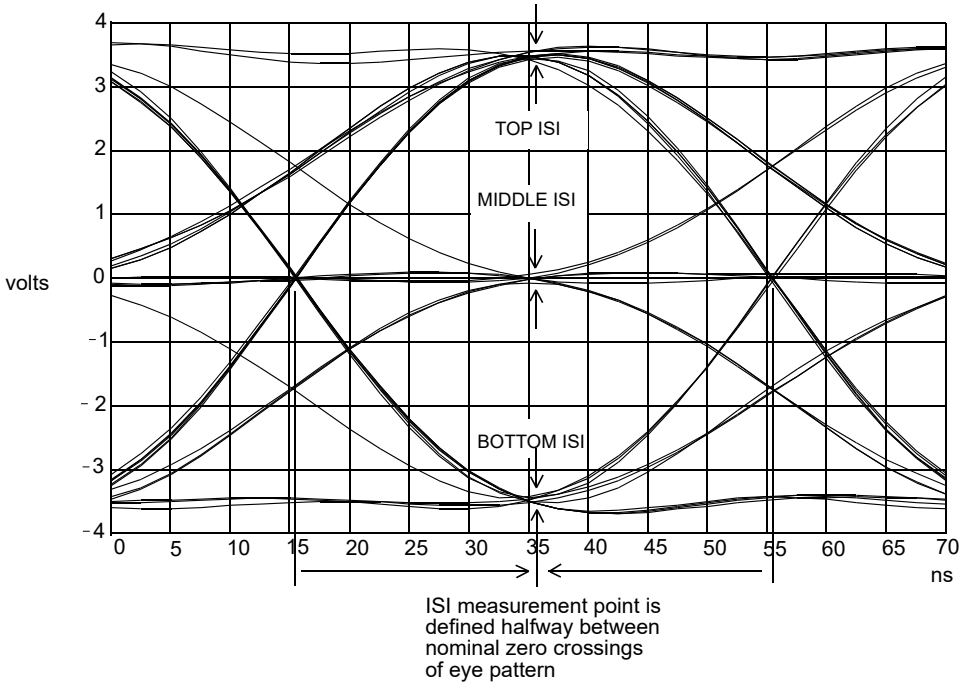

Figure 23–15—Definition of sampling points for ISI measurement

It is a mandatory requirement that the peak-to-peak ISI, and the overall peak-to-peak signal voltage, be measured at a point in time halfway between the nominal zero crossings of the observed eye pattern.

It is a mandatory requirement that the 100BASE-T4 Transmit Test Filter perform the function of a third-order Butterworth filter with its –3 dB point at 25.0 MHz.

One acceptable implementation of a 100BASE-T4 Transmit Test Filter appears in Figure 23–16. That implementation uses the 100BASE-T4 Transmit Test Filter as a line termination. The output of the filter is terminated in 100 Ω. It is a mandatory requirement that such implementations of the 100BASE-T4 Transmit Test Filter be designed such that the reflection loss of the filter, when driven by a 100 Ω source, exceeds 17 dB across the frequency range 2 to 12.5 MHz.

Equivalent circuits that implement the same overall transfer function are also acceptable. For example, the 100BASE-T4 Transmit Test Filter may be tapped onto a line in parallel with an existing termination. It is a mandatory requirement that such implementations of the 100BASE-T4 Transmit Test Filter be designed with an input impedance sufficiently high that the reflection loss of the parallel combination of filter and 100 Ω termination, when driven by 100 Ω, exceeds 17 dB across the frequency range 2 to 12.5 MHz.

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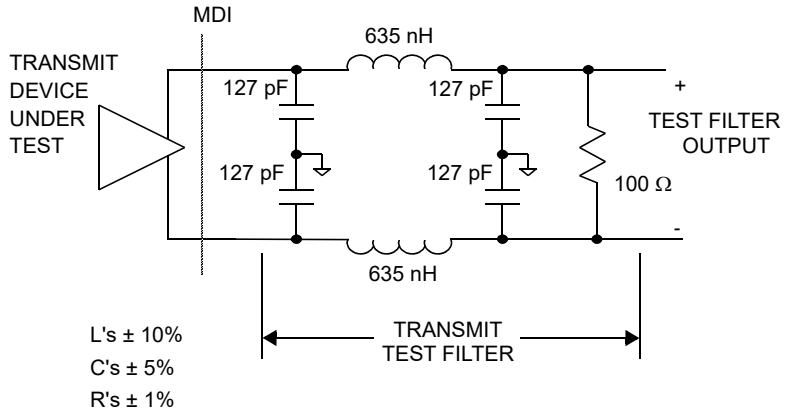

Figure 23–16—Acceptable implementation of transmit test filter

23.5.1.2.4 Transmitter differential output impedance

The differential output impedance as measured at the MDI for each transmit pair shall be such that any reflection due to differential signals incident upon the MDI from a balanced cable having an impedance of 100 Ω is at least 17 dB below the incident signal, over the frequency range of 2.0 MHz to 12.5 MHz. This return loss shall be maintained at all times when the PHY is fully powered.

With every transmitter connected as in Figure 23–17, and while transmitting a repeating sequence of packets as specified in Table 23–5, the amount of droop on any transmit pair as defined in Figure 23–18 during the transmission of eop1 and eop4 shall not exceed 6.0%.

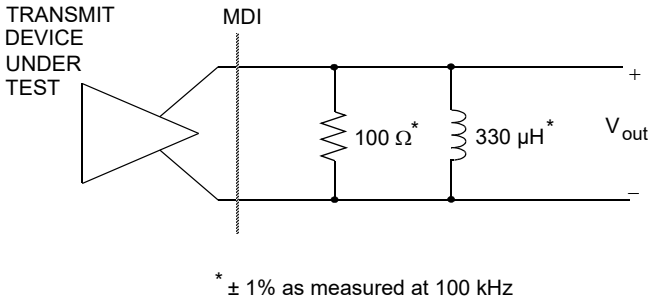

Figure 23–17—Output impedance test setup

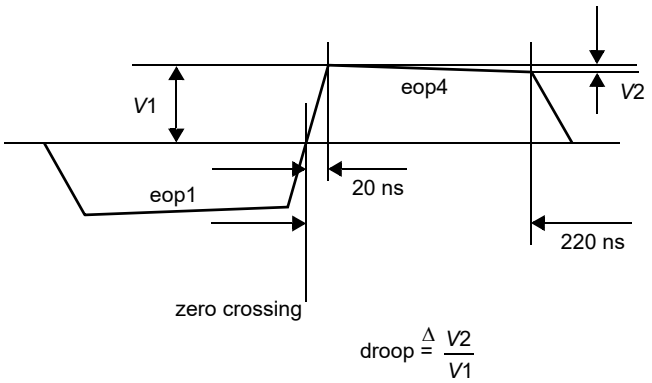

Figure 23–18—Measurement of output droop

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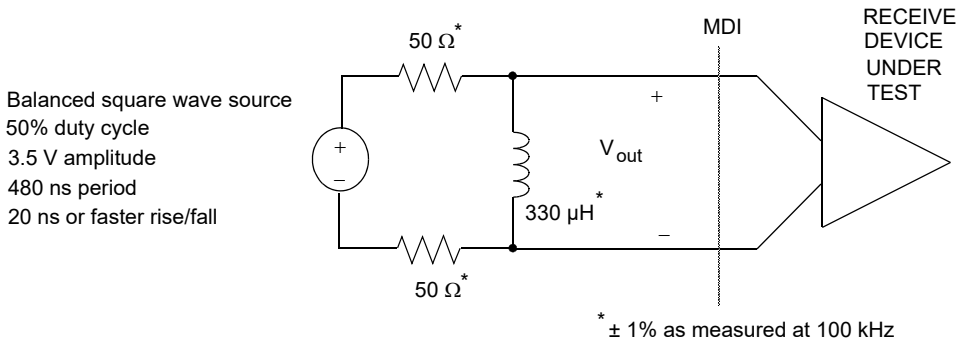

Figure 23–19—Input impedance test setup

Table 23–5—Sequence of packets for droop test

Packet sequence (Transmit this sequence of packets in a repetitive loop)	**Packet length** (Number of data octets)	**Data, hex** (All octets in each packet are the same)
First packet	64	AA
Second packet	65	AA
Third packet	66	AA

23.5.1.2.5 Output timing jitter

While repetitively transmitting a random sequence of valid 8B6T codewords, and while observing the output of a 100BASE-T4 Transmit Test Filter connected at the MDI to any of the transmit pairs as specified in 23.5.1.2.3, the measured jitter shall be no more than 4 ns p-p. For the duration of the test, each of the other transmit pairs shall be connected to either a 100BASE-T4 Transmit Test Filter or a 100 Ω resistive load.

NOTE 1—Jitter is the difference between the actual zero crossing point in time and the ideal time. For various ternary transitions, the zero crossing time is defined differently. For transitions between +1 and –1 or vice versa, the zero crossing point is defined as that point in time when the voltage waveform crosses zero. For transitions between zero and the other values, or from some other value to zero, the zero crossing time is defined as that point in time when the voltage waveform crosses the boundary between logical voltage levels, halfway between zero volts and the logical +1 or logical –1 ideal level.

NOTE 2—The ideal zero crossing times are contained in a set of points $\{t_n\}$ where $t_n = t_0 + n/f$, where n is an integer, and f is in the range 25.000 MHz ± 0.01%. A collection of zero crossing times satisfies the jitter requirement if there exists a pair (t_0, f) such that each zero crossing time is separated from some member of $\{t_n\}$ by no more than 4 ns.

23.5.1.2.6 Transmitter impedance balance

The common-mode to differential-mode impedance balance of each transmit output shall exceed

$$29 - 17\log\left(\frac{f}{10}\right)\text{dB}$$

where f is the frequency (in MHz) over the frequency range 2.0 MHz to 12.5 MHz. The balance is defined as

$$20\log\left(\frac{E_{\text{cm}}}{E_{\text{dif}}}\right)$$

where E_{cm} is an externally applied sine-wave voltage as shown in Figure 23–20.

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NOTE—The balance of the test equipment (such as the matching of the test resistors) has to be insignificant relative to the balance requirements.

23.5.1.2.7 Common-mode output voltage

The implementer should consider any applicable local, national, or international regulations. Driving unshielded twisted pairs with high-frequency, common-mode voltages may result in interference to other equipment. FCC conducted and radiated emissions tests may require that, while transmitting data, the magnitude of the total common-mode output voltage, $E_{cm(out)}$, on any transmit circuit, be less than a few millivolts when measured as shown in Figure 23–21.

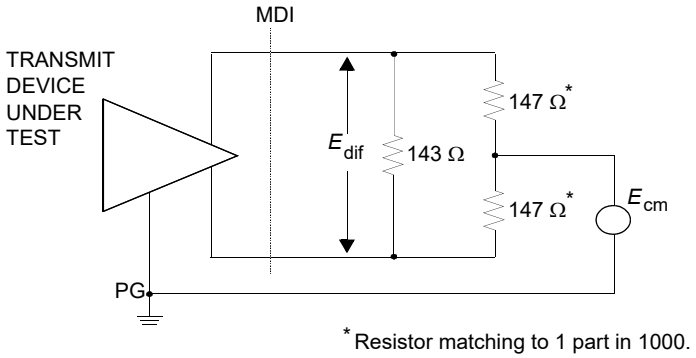

Figure 23–20—Transmitter impedance balance and common-mode rejection test circuit

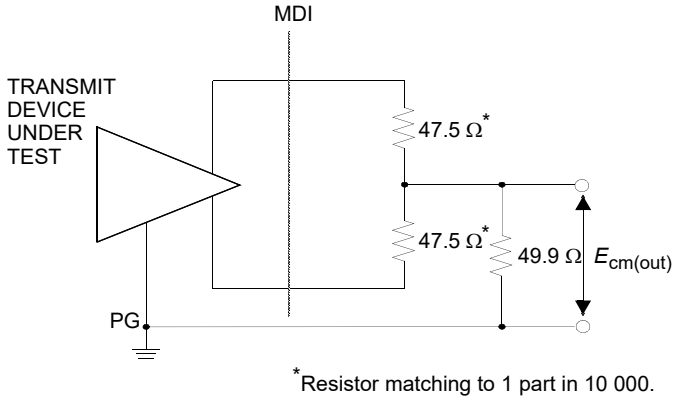

Figure 23–21—Common-mode output voltage test circuit

23.5.1.2.8 Transmitter common-mode rejection

The application of E_{cm} as shown in Figure 23–20 shall not change the differential voltage at any transmit output, E_{dif}, by more than 100 mV for all data sequences while the transmitter is sending data. Additionally, the edge jitter added by the application of E_{cm} shall be no more than 1.0 ns. E_{cm} shall be a 15 V peak 10.1 MHz sine wave.

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23.5.1.2.9 Transmitter fault tolerance

Transmitters, when either idle or nonidle, shall withstand without damage the application of short circuits across any transmit output for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 420 mA.

Transmitters, when either idle or nonidle, shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 23–22). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

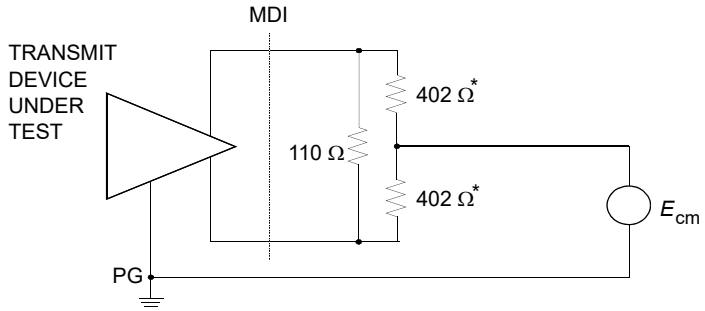

Figure 23–22—Transmitter fault tolerance test circuit

23.5.1.2.10 Transmit clock frequency

The ternary symbol transmission rate on each pair shall be 25.000 MHz ± 0.01%.

23.5.1.3 Receiver specifications

The PMA shall provide the Receive function specified in 23.4.1.3 in accordance with the electrical specifications of this clause. The patch cables and interconnecting hardware used in test configurations shall meet Category 5 specifications as in ISO/IEC 11801: 1995.

The term *worst-case UTP model*, as used in this clause, refers to lumped-element cable model shown in Figure 23–23 that has been developed to simulate the attenuation and group delay characteristics of 100 m of worst-case Category 3 PVC UTP cable.

This constant resistance filter structure has been optimized to best match the following amplitude and group delay characteristics, where the argument f is in hertz, and the argument x is the cable length in meters. For the worst-case UTP model, argument x was set to 100 m, and the component values determined for a best least mean squared fit of both real and imaginary parts of $H(f, x)$ over the frequency range 2 to 15 MHz.

NOTE—This group delay model is relative and does not includes the fixed delay associated with 100 m of Category 3 cable. An additional 570 ns of fixed delay should be added in order to obtain the absolute group delay.

$$PropagationImag(f, x) = j(-10)\sqrt{\frac{f}{10^7}}\left(\frac{x}{100}\right)$$

$$PropagationReal(f, x) = -\left(7.1\sqrt{\frac{f}{10^6}} + 0.70\frac{f}{10^6}\right)\left(\frac{x}{305}\right)$$

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$$H(f,x) = 10^{\frac{PropagationImag(f,x) + PropagationReal(f,x)}{20}}$$

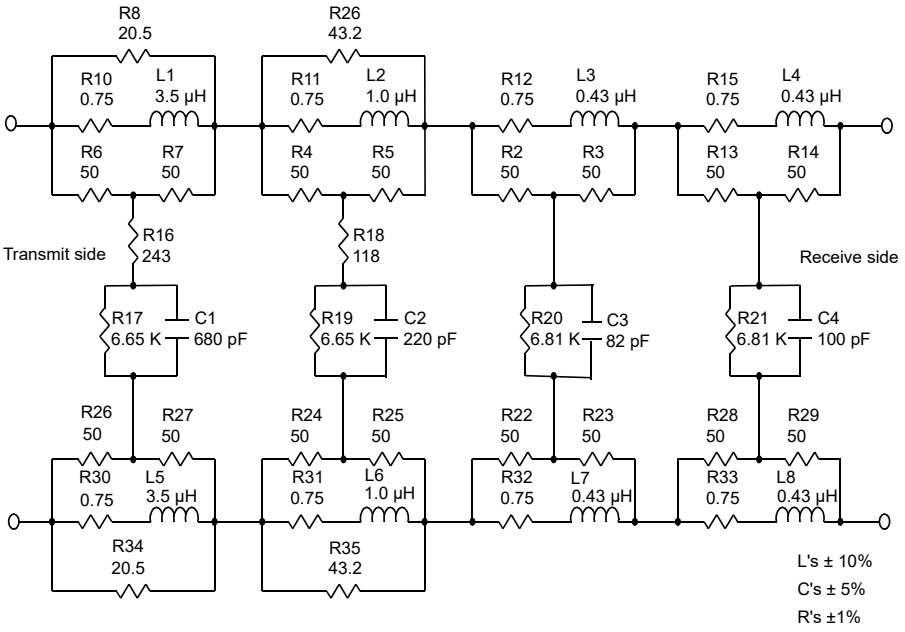

Figure 23–23—Worst-case UTP model

23.5.1.3.1 Receiver differential input signals

Differential signals received on the receive inputs that were transmitted within the constraints of 23.5.1.2, and have then passed through a worst-case UTP model, shall be correctly translated into one of the PMA_UNITDATA.indication messages and sent to the PCS. In addition, the receiver, when presented with a link test pulse generated according to the requirements of 23.4.1.2 and followed by at least 3T of silence on pair RX_D2, shall accept it as a link test pulse.

Both data and link test pulse receive features shall be tested in at least two configurations: using the worst-case UTP model, and with a connection less than one meter in length between transmitter and receiver.

A receiver is allowed to discard the first received packet after the transition into state LINK_PASS, using that packet for the purpose of fine-tuning its receiver equalization and clock recovery circuits.

NOTE—Implementers may find it practically impossible to meet the requirements of this subclause without using some form of adaptive equalization.

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23.5.1.3.2 Receiver differential noise immunity

The PMA, when presented with 8B6T encoded data meeting the requirements of 23.5.1.3.1, shall translate this data into PMA_UNITDATA.indication (DATA) messages with a bit loss of no more than that specified in 23.4.1.3.

The PMA Carrier Sense function shall *not* set pma_carrier=ON upon receiving any of the following signals on pair RX_D2 at the receiving MDI, as measured using a 100BASE-T4 transmit test filter (23.5.1.2.3):

a) All signals having a peak magnitude less than 325 mV.
b) All continuous sinusoidal signals of amplitude less than 8.7 V peak-to-peak and frequency less than 1.7 MHz.
c) All sine waves of single cycle or less duration, starting with phase 0° or 180°, and of amplitude less than 8.7 V peak-to-peak, where the frequency is between 1.7 MHz and 15 MHz. For a period of 7 BT before and after this single cycle, the signal shall be less than 325 mV.
d) Fast link pulse burst (FLP burst), as defined in Clause 28.
e) The link integrity test pulse signal TP_IDL_100.

23.5.1.3.3 Receiver differential input impedance

The differential input impedance as measured at the MDI for each receive input shall be such that any reflection due to differential signals incident upon each receive input from a balanced cable having an impedance of 100 Ω is at least 17 dB below the incident signal, over the frequency range of 2.0 MHz to 12.5 MHz. This return loss shall be maintained at all times when the PHY is fully powered.

With each receiver connected as in Figure 23–19, and with the source adjusted to simulate eop1 and eop4 (50% duty cycle square wave with 3.5 V amplitude, period of 480 ns, and risetime of 20 ns or faster), the amount of droop on each receive pair as defined in Figure 23–18 shall not exceed 6.0%.

23.5.1.3.4 Common-mode rejection

While receiving packets from a compliant 100BASE-T4 transmitter connected to all MDI pins, a receiver shall send the proper PMA_UNITDATA.indication messages to the PCS for any differential input signal E_s that results in a signal E_{dif} that meets 23.5.1.3.1 even in the presence of common-mode voltages E_{cm} (applied as shown in Figure 23–24). E_{cm} shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%–80%), connected to each of the receive pairs RX_D2, BI_D3, and BI_D4.

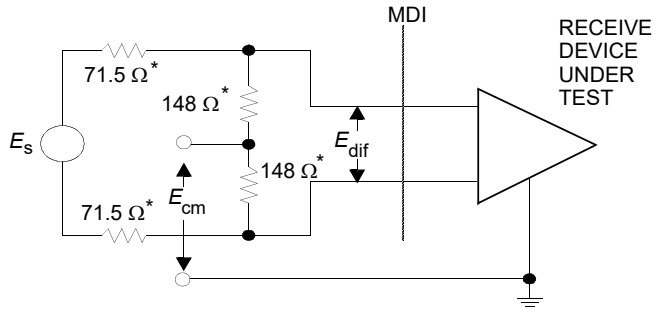

Figure 23–24—Receiver common-mode rejection test circuit

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23.5.1.3.5 Receiver fault tolerance

The receiver shall tolerate the application of short circuits between the leads of any receive input for an indefinite period of time without damage and shall resume normal operation after such faults are removed. Receivers shall withstand without damage a 1000 V common-mode impulse of either polarity (E_{cm} as indicated in Figure 23–25). The shape of the impulse shall be 0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value), as defined in IEC 60060.

23.5.1.3.6 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a ternary symbol rate within the range 25.000 MHz ± 0.01%.

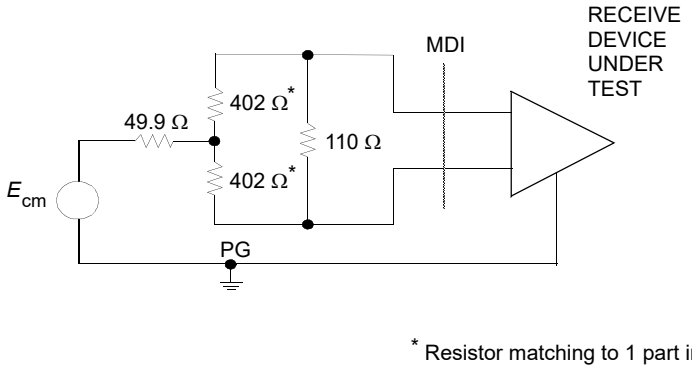

Figure 23–25—Common-mode impulse test circuit

23.5.2 Power consumption

After 100 ms following PowerOn, the current drawn by the PHY shall not exceed 0.75 A when powered through the MII.

The PHY shall be capable of operating from all voltage sources allowed by Clause 22, including those current limited to 0.75 A, as supplied by the DTE or repeater through the resistance of all permissible MII cables.

The PHY shall not introduce extraneous signals on the MII control circuits during normal power-up and power-down.

While in power-down mode the PHY is not required to meet any of the 100BASE-T4 performance requirements.

23.6 Link segment characteristics

23.6.1 Cabling

Cabling and installation practices generally suitable for use with this standard appear in ISO/IEC 11801: 1995. Exceptions, notes, and additional requirements are as follows:

a) 100BASE-T4 uses a star topology. Horizontal cabling is used to connect PHY entities.

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b) 100BASE-T4 is an ISO/IEC 11801: 1995 class C application, with additional installation requirements and transmission parameters specified in 23.6.2 through 23.6.4. The highest fundamental frequency transmitted by 8B6T coding is 12.5 MHz. The aggregate data rate for three pairs using 8B6T coding is 100 Mb/s.
c) 100BASE-T4 shall use four pairs of balanced cabling, Category 3 or better, with a nominal characteristic impedance of 100 Ω.
d) When using Category 3 cable for the link segment, Clause 23 recommends, but does not require, the use of Category 4 or better connecting hardware, patch cords and jumpers. The use of Category 4 or better connecting hardware increases the link segment composite NEXT loss, composite ELFEXT loss and reduces the link segment insertion loss. This lowers the link segment crosstalk noise, which in turn decreases the probability of errors.
e) The use of shielded cable is outside the scope of this standard.

23.6.2 Link transmission parameters

Unless otherwise specified, link segment testing shall be conducted using source and load impedances of 100 Ω.

23.6.2.1 Insertion loss

The insertion loss of a simplex link segment shall be no more than 12 dB at all frequencies between 2 MHz and 12.5 MHz. This consists of the attenuation of the twisted pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the simplex link segment. The insertion loss specification shall be met when the simplex link segment is terminated in source and load impedances that satisfy 23.5.1.2.4 and 23.5.1.3.3.

NOTE—The loss of PVC-insulated cable exhibits significant temperature dependence. At temperatures greater than 40 °C, it may be necessary to use a less temperature-dependent cable, such as many Fluorinated Ethylene Propylene (FEP), Polytetrafluoroethylene (PTFE), or Perfluoroalkoxy (PFA) plenum-rated cables.

23.6.2.2 Differential characteristic impedance

The magnitude of the differential characteristic impedance of a 3 m length of twisted pair used in a simplex link shall be between 85 Ω and 115 Ω for all frequencies between 2 MHz and 12.5 MHz.

23.6.2.3 Coupling parameters

In order to limit the noise coupled into a simplex link segment from adjacent simplex link segments, Near-End Crosstalk (NEXT) loss and Equal Level Far-End Crosstalk (ELFEXT) loss are specified for each simplex link segment. In addition, since three simplex links (TX_D1, Bl_D3, and Bl_D4) are used to send data between PHYs and one simplex link (RX_D2) is used to carry collision information as specified in 23.1.4, Multiple-Disturber NEXT loss and Multiple-Disturber ELFEXT loss are also specified.

23.6.2.3.1 Differential Near-End Crosstalk (NEXT) loss

The differential Near-End Crosstalk (NEXT) loss between two simplex link segments is specified in order to ensure that collision information can be reliably received by the PHY receiver. The NEXT loss between each of the three data carrying simplex link segments and the collision sensing simplex link segment shall be at least $24.5 - 15 \times \log_{10}(f/12.5)$ (where f is the frequency in MHz) over the frequency range 2.0 MHz to 12.5 MHz.

23.6.2.3.2 Multiple-disturber NEXT (MDNEXT) loss

Since three simplex links are used to send data between PHYs and one simplex link is used to carry collision information, the NEXT noise that is coupled into the collision, sensing simplex link segment is from multiple (three) signal sources, or disturbers. The MDNEXT loss between the three data carrying simplex link

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segments and the collision sensing simplex link segment shall be at least $21.4 - 15\times\log_{10}(f/12.5)$ dB (where f is the frequency in MHz) over the frequency range 2.0 to 12.5 MHz. Refer to 12.7.3.2 and Annex B.3 Example Crosstalk Computation for Multiple Disturbers, for a tutorial and method for estimating the MDNEXT loss for an n-pair cable.

23.6.2.3.3 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk noise at the far end of a simplex link segment to meet the BER objective specified in 23.1.2 and the noise specifications of 23.6.3. Far-End Crosstalk (FEXT) noise is the crosstalk noise that appears at the far end of a simplex link segment which is coupled from an adjacent simplex link segment with the noise source (transmitters) at the near end. ELFEXT loss is the ratio of the data signal to FEXT noise at the output of a simplex link segment (receiver input). To limit the FEXT noise from adjacent simplex link segments, the ELFEXT loss between two data carrying simplex link segments shall be greater than $23.1 - 20\times\log_{10}(f/12.5)$ dB (where f is the frequency in MHz) over the frequency range 2.0 MHz to 12.5 MHz. ELFEXT loss at frequency f and distance l is defined as

$$\text{ELFEXT\_Loss}\ (f,l) = 20 \times \log_{10}\left(\frac{V_{\text{pds}}}{V_{\text{pcn}}}\right) - \text{SLS\_Loss}\ (\text{dB})$$

where

V_{pds} is the peak voltage of disturbing signal (near-end transmitter)
V_{pcn} is the peak crosstalk noise at the far end of disturbed simplex link segment
SLS_Loss is the insertion loss of the disturbing simplex link segment

23.6.2.3.4 Multiple-disturber ELFEXT (MDELFEXT) loss

Since three simplex links are used to transfer data between PHYs, the FEXT noise that is coupled into an data carrying simplex link segment is from multiple (two) signal sources, or disturbers. The MDELFEXT loss between a data carrying simplex link segment and the other two data carrying simplex link segments shall be greater than $20.9 - 20\times\log_{10}(f/12.5)$ (where f is the frequency in MHz) over the frequency range 2.0 MHz to 12.5 MHz. Refer to 12.7.3.2 and Annex B.3, Example Crosstalk Computation for Multiple Disturbers, for a tutorial and method for estimating the MDELFEXT loss for an n-pair cable.

23.6.2.4 Delay

Since T4 sends information over three simplex link segments in parallel, the absolute delay of each and the differential delay are specified to comply with network round-trip delay limits and ensure the proper decoding by receivers, respectively.

23.6.2.4.1 Maximum link delay

The propagation delay of a simplex link segment shall not exceed 570 ns at all frequencies between 2.0 MHz and 12.5 MHz.

23.6.2.4.2 Maximum link delay per meter

The propagation delay per meter of a simplex link segment shall not exceed 5.7 ns/m at all frequencies between 2.0 MHz and 12.5 MHz.

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23.6.2.4.3 Difference in link delays

The difference in propagation delay, or skew, under all conditions, between the fastest and the slowest simplex link segment in a link segment shall not exceed 50 ns at all frequencies between 2.0 MHz and 12.5 MHz. It is a further functional requirement that, once installed, the skew between all pair combinations due to environmental conditions shall not vary more than ± 10 ns, within the above requirement.

23.6.3 Noise

The noise level on the link segments shall be such that the objective error ratio is met. The noise environment consists generally of two primary contributors: self-induced near-end crosstalk, which affects the ability to detect collisions, and far-end crosstalk, which affects the signal-to-noise ratio during packet reception.

23.6.3.1 Near-End Crosstalk

The MDNEXT (Multiple-Disturber Near-End Crosstalk) noise on a link segment depends on the level of the disturbing signals on pairs TX_D1, BI_D3, and BI_D4, and the crosstalk loss between those pairs and the disturbed pair, RX_D2.

The MDNEXT noise on a link segment shall not exceed 325 mVp.

This standard is compatible with the following assumptions:

a) Three disturbing pairs with 99th percentile pair-to-pair NEXT loss greater than 24.5 dB at 12.5 MHz (i.e., Category 3 cable).
b) Six additional disturbers (2 per simplex link) representing connectors at the near end of the link segment with 99th percentile NEXT loss greater than 40 dB at 12.5 MHz (i.e., Category 3 connectors installed in accordance with 23.6.4.1).
c) All disturbers combined according to the MDNEXT Monte Carlo procedure outlined in Appendix A3, Example Crosstalk Computation for Multiple Disturbers.

The MDNEXT noise is defined using three maximum level 100BASE-T4 transmitters sending uncorrelated continuous data sequences while attached to the simplex link segments TX_D1, BI_D3, and BI_D4 (disturbing links), and the noise measured at the output of a filter connected to the simplex link segment RX_D2. (disturbed link). Each continuous data sequence is a pseudo-random bit pattern having a length of at least 2047 bits that has been coded according to the 8B6T coding rules in 23.2.1.2. The filter is the 100BASE-T4 Transmit Test Filter specified in 23.5.1.2.3.

23.6.3.2 Far-End Crosstalk

The MDFEXT (Multiple-Disturber Far-End Crosstalk) noise on a link segment depends on the level of the disturbing signals on pairs TX_D1, BI_D3, and BI_D4, and the various crosstalk losses between those pairs.

The MDFEXT noise on a link segment shall not exceed 87 mVp.

This standard is compatible with the following assumptions:

a) Two disturbing pairs with 99th percentile ELFEXT (Equal Level Far-End Crosstalk) loss greater than 23 dB at 12.5 MHz.
b) Nine additional disturbers (three per simplex link) representing connectors in the link segment with 99th percentile NEXT loss greater than 40 dB at 12.5 MHz.
c) All disturbers combined according to the MDNEXT Monte Carlo procedure outlined in Appendix A3, Example Crosstalk Computation for Multiple Disturbers.

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The MDFEXT noise is defined using two maximum level 100BASE-T4 transmitters sending uncorrelated continuous data sequences while attached to two simplex link segments (disturbing links) and the noise measured at the output of a filter connected to the far end of a third simplex link segment (disturbed link). Each continuous data sequence is a pseudo-random bit pattern having a length of at least 2047 bits that has been coded according to the 8B6T coding rules in 23.2.1.2. The filter is the 100BASE-T4 Transmit Test Filter specified in 23.5.1.2.3.

23.6.4 Installation practice

23.6.4.1 Connector installation practices

The amount of untwisting in a pair as a result of termination to connecting hardware should be no greater than 25 mm (1.0 in) for Category 3 cables. This is the same value recommended in ISO/IEC 11801: 1995 for Category 4 connectors.

23.6.4.2 Disallow use of Category 3 cable with more than four pairs

Jumper cables, or horizontal runs, made from more than four pairs of Category 3 cable are not allowed.

23.6.4.3 Allow use of Category 5 jumpers with up to 25 pairs

Jumper cables made from up to 25 pairs of Category 5 cable, for the purpose of mass-terminating port connections at a hub, are allowed. Such jumper cables, if used, shall be limited in length to no more than 10 m total.

23.7 MDI specification

This clause defines the MDI. The link topology requires a crossover function between PMAs. Implementation and location of this crossover are also defined in this clause.

23.7.1 MDI connectors

Eight-pin connectors meeting the requirements of section 3 and figures 1 through 5 of IEC 60603-7: 1990 shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figure 23–26 and Figure 23–27. Table 23-6 shows the assignment of PMA signals to connector contacts for PHYs with and without an internal crossover.

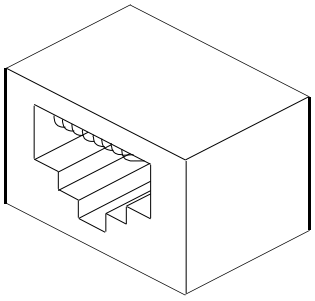

Figure 23–26—MDI connector

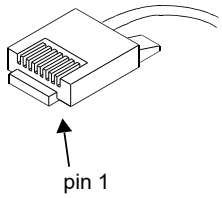

Figure 23–27—Balanced cabling connector

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Table 23-6—MDI connection and labeling requirements

Contact	PHY without internal crossover (recommended for DTE) internal PMA signals	PHY with internal crossover (recommended for repeater) internal PMA signals	MDI labeling requirement
1	TX_D1+	RX_D2+	TX_D1+
2	TX_D1–	RX_D2–	TX_D1–
3	RX_D2+	TX_D1+	RX_D2+
4	BI_D3+	BI_D4+	BI_D3+
5	BI_D3–	BI_D4–	BI_D3–
6	RX_D2–	TX_D1–	RX_D2–
7	BI_D4+	BI_D3+	BI_D4+
8	BI_D4–	BI_D3–	BI_D4–

23.7.2 Crossover function

It is a functional requirement that a crossover function be implemented in every link segment. The crossover function connects the transmitters of one PHY to the receivers of the PHY at the other end of the link segment. Crossover functions may be implemented internally to a PHY or elsewhere in the link segment. For a PHY that does not implement the crossover function, the MDI labels in the last column of Table 23–4 refer to its own internal circuits (second column). For PHYs that do implement the internal crossover, the MDI labels in the last column of Table 23–4 refer to the internal circuits of the remote PHY of the link segment. Additionally, the MDI connector for a PHY that implements the crossover function shall be marked with the graphical symbol “X”. Internal and external crossover functions are shown in Figure 23–28. The crossover function specified here for pairs TX_D1 and RX_D2 is compatible with the crossover function specified in 14.5.2 for pairs TD and RD.

When a link segment connects a DTE to a repeater, it is recommended the crossover be implemented in the PHY local to the repeater. If both PHYs of a link segment contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the PHYs. When both PHYs contain internal crossovers, it is further recommended in networks in which the topology identifies either a central backbone segment or a central repeater that the PHY furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable, or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

23.8 System considerations

The repeater unit specified in Clause 27 forms the central unit for interconnecting 100BASE-T4 twisted-pair links in networks of more than two nodes. It also provides the means for connecting 100BASE-T4 twisted-pair links to other 100 Mb/s baseband segments. The proper operation of a CSMA/CD network requires that network size be limited to control round-trip propagation delay as specified in Clause 29.

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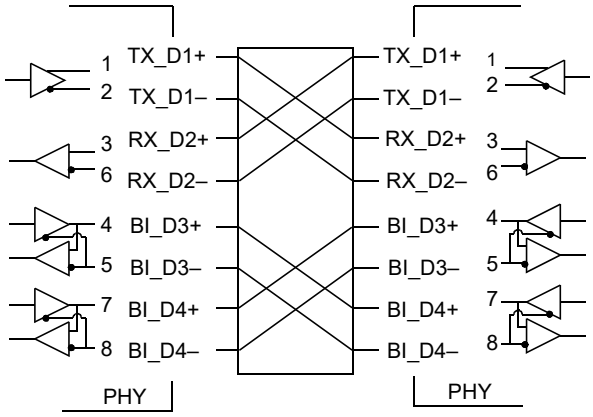
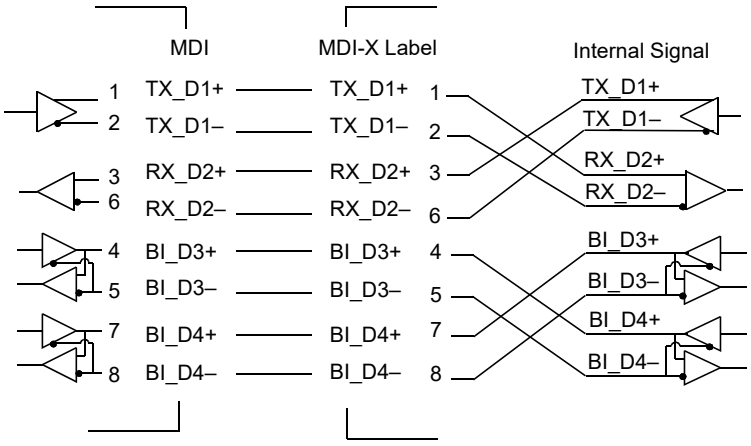


a) Two PHYs with external crossover function



b) PHY with internal crossover function

Figure 23–28—Crossover function

23.9 Environmental specifications

23.9.1 General safety

NOTE—Since September 2003, maintenance changes are no longer being considered for this clause. Since February 2021, safety information is in J.2.

All equipment meeting this standard shall conform to IEC 60950: 1991.

23.9.2 Network safety

This clause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

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a) Direct contact between LAN components and power, lighting, or communications circuits
b) Static charge buildup on LAN cables and components
c) High-energy transients coupled onto the LAN cable system
d) Voltage potential differences between safety grounds to which various LAN components are connected

Such electrical safety hazards have to be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures have to be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

23.9.2.1 Installation

It is a mandatory functional requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

23.9.2.2 Grounding

Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection.

WARNING

It is assumed that the equipment to which the PHY is attached is properly grounded, and not left floating nor serviced by a "doubly insulated, ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety, are beyond the scope of this standard.

23.9.2.3 Installation and maintenance guidelines

It is a mandatory functional requirement that, during installation and maintenance of the cable plant, care be taken to ensure that noninsulated network cable conductors do not make electrical contact with unintended conductors or ground.

23.9.2.4 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 100BASE-T4 equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply.

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.

Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 Vdc with a 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 100BASE-T4 equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 100BASE-T4 transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore,

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full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

23.9.3 Environment

23.9.3.1 Electromagnetic emission

The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

23.9.3.2 Temperature and humidity

The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

23.10 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in Mb/s
b) Power level in terms of maximum current drain (for external PHYs)
c) Any applicable safety warnings

See also 23.7.2.

23.11 Timing summary

23.11.1 Timing references

All MII signals are defined (or corrected to) the DTE end of a zero length MII cable.

NOTE—With a finite length MII cable, TX_CLK appears in the PHY one cable propagation delay *earlier* than at the MII. This advances the transmit timing. Receive timing is retarded by the same amount.

The phrase *adjusted for pair skew*, when applied to a timing reference on a particular pair, means that the designated timing reference has been adjusted by adding to it the difference between the time of arrival of preamble on the latest of the three receive pairs and the time of arrival of preamble on that particular pair.

PMA_UNITDATA.request

Figures 23–29, 23–30, 23–31, and 23–32. The implementation of this abstract message is not specified. Conceptually, this is the time at which the PMA has been given full knowledge and use of the ternary symbols to be transmitted.

PMA_UNITDATA.indication

Figure 23–33. The implementation of this abstract message is not specified. Conceptually, this is the time at which the PCS has been given full knowledge and use of the ternary symbols received.

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WAVEFORM

Figure 23–29. Point in time at which output waveform has moved 1/2 way from previous nominal output level to present nominal output level.

TX_EN

Figure 23–30. First rising edge of TX_CLK following the rising edge of TX_EN.

NOT_TX_EN

Figure 23–31 and Figure 23–32. First rising edge of TX_CLK following the falling edge of TX_EN.

CRS

Figure 23–33. Rising edge of CRS.

CARRIER_STATUS

Figure 23–33. Rising edge of carrier_status.

NOT_CARRIER_STATUS

Figure 23–34. Falling edge of carrier_status.

RX_DV

No figure. First rising edge of RX_CLK following rising edge of RX_DV.

COL

No figure. Rising edge of COL signal at MII.

NOT_COL

No figure. Falling edge of COL signal at MII.

PMA_ERROR

No figure. Time at which rxerror_status changes to ERROR.

23.11.2 Definitions of controlled parameters

PMA_OUT

Figure 23–29. Time between PMA_UNITDATA.request (tx_code_vector) and the WAVEFORM timing reference for each of the three transmit channels TX_D1, BI_D3, or BI_D4.

TEN_PMA

Figure 23–30, Figure 23–31, and Figure 23–32. Time between TX_EN timing reference and MA_UNITDATA.request (tx_code_vector).

TEN_CRS

Figure 23–30. Time between TX_EN timing reference and the loopback of TX_EN to CRS as measured at the CRS timing reference point.

NOT_TEN_CRS

Figure 23–31 and Figure 23–32. Time between NOT_TX_EN timing reference and the loopback of TX_EN to CRS as measured at the NOT_CRS timing reference point. In the event of a collision (COL is raised at any point during a packet) the minimum time for NOT_TEN_CRS may optionally be as short as 0.

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RX_PMA_CARRIER

Figure 23–33. Time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the CARRIER_STATUS timing reference.

RX_CRS

Figure 23–33. Time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the CRS timing reference.

NOTE—The input waveform used for this test is an ordinary T4 preamble, generated by a compliant T4 transmitter. As such, the delay between the first and third pulses of the preamble (which are used by the carrier sense logic) is very nearly 80 ns.

RX_NOT_CRS

For a data packet, the time between the WAVEFORM timing reference, adjusted for pair skew, of the first pulse of eop1, and the deassertion of CRS. For a collision fragment, the time between the WAVEFORM timing reference, adjusted for pair skew, of the ternary symbol on pair TX_D2, which follows the last ternary data symbol received on pair RX_D2, and the deassertion of CRS.

Both are limited to the same value. For a data packet, detection of the six ternary symbols of eopo1 is accomplished in the PCS layer. For a collision fragment, detection of the concluding seven ternary zeros is accomplished in the PMA layer, and passed to the PCS in the form of the carrier_status indication.

FAIRNESS

The difference between RX_NOT_CRS at the conclusion of one packet and RX_CRS on a subsequent packet. The packets used in this test may arrive with an IPG anywhere in the range of 80 to 160.

RX_PMA_DATA

Figure 23–33. Time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the particular PMA_UNITDATA.indication that transfers to the PCS the first ternary symbol of the first 6T code group from receive pair BI_D3.

EOP_CARRIER_STATUS

Figure 23–34. For a data packet, the time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of eop1 and the NOT_CARRIER_STATUS timing reference.

EOC_CARRIER_STATUS

Figure 23–35. In the case of a colliding packet, the time between the WAVEFORM timing reference, adjusted for pair skew, of the ternary symbol on pair RX_D2, which follows the last ternary data symbol received on pair RX_D2 and the NOT_CARRIER_STATUS timing reference.

RX_RXDV

No figure. Time between WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the RX_DV timing reference.

RX_PMA_ERROR

No figure. In the event of a preamble in error, the time between the WAVEFORM timing reference adjusted for pair skew, of first pulse of that preamble (or first pulse of the preamble preceded by a link test pulse or a partial link test pulse), and the PMA_ERROR timing reference.

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RX_COL

No figure. In the event of a collision, the time between the WAVEFORM timing reference adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse), and the COL timing reference.

RX_NOT_COL

No figure. In the event of a collision in which the receive signal stops before the locally transmitted signal, the time between the WAVEFORM timing reference adjusted for pair skew, of the ternary symbol on pair RX_D2, which follows the last ternary data symbol received on pair RX_D2 and the NOT_COL timing reference point.

TX_NOT_COL

No figure. In the event of a collision in which the locally transmitted signal stops before the received signal, the time between the NOT_TX_EN timing reference and the loopback of TX_EN to COL as measured at the NOT_COL timing reference point.

TX_SKEW

Greatest absolute difference between a) the waveform timing reference of the first pulse of a preamble as measured on output pair TX_D1; b) the waveform timing reference of the first pulse of a preamble as measured on output pair BI_D3; and c) the waveform timing reference of the first pulse of a preamble as measured on output pair BI_D4. Link test pulses, if present during the measurement, have to be separated from the preamble by at least 100 ternary symbols.

CRS_PMA_DATA

Time between the timing reference for CARRIER STATUS and the transfer, via PMA_UNITDATA.indication, of the first ternary symbol of the 6T code group marked DATA1 in Figure 23–6.

COL_to_BI_D3/D4_OFF

No figure. In the case of a colliding packet, the time between the WAVE FORM timing reference, adjusted for pair skew, of the first pulse of preamble (or the first pulse of the preamble preceded by a link test pulse or a partial link test pulse) on RX_D2, and the first ternary zero transmitted on BI_D3 and on BI_D4.

NOTE—Subclause 23.4.1.2 mandates that transmission on pairs BI_D3 and BI_D4 be halted in the event of a collision.

23.11.3 Table of required timing values

While in the LINK_PASS state, each PHY timing parameter shall fall within the Low and High limits listed in Table 23–7. All units are in bit times. A bit time equals 10 ns.

Table 23–7—Required timing values

Controlled parameter	Low limit (bits)	High limit (bits)	Comment
PMA_OUT	1	9.5	
TEN_PMA + PMA_OUT	7	17.5	
TEN_CRS	0	+4	
NOT_TEN_CRS	0	36	
RX_PMA_CARRIER	0	15.5	

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Table 23–7—Required timing values *(continued)*

Controlled parameter	Low limit (bits)	High limit (bits)	Comment
RX_CRS	0	27.5	
RX_NOT_CRS	0	51.5	
FAIRNESS	0	28	
RX_PMA_DATA	67	90.5	
EOP_CARRIER_STATUS	51	74.5	
EOC_CARRIER_STATUS	3	50.5	
RX_RXDV	81	114.5	
RX_PMA_ERROR	RX_PMA_DATA	RX_PMA_DATA + 20	Allowed limits equal the actual RX_PMA_DATA time for the device under test plus from 0 to 20 BT
RX_COL	0	27.5	SAME AS RX_CRS
RX_NOT_COL	0	51.5	SAME AS RX_NOT_CRS
TX_NOT_COL	0	36	
TX_SKEW	0	0.5	
CRS_PMA_DATA	0	78.5	
COL_to_BI_D3/D4_OFF	0	40	

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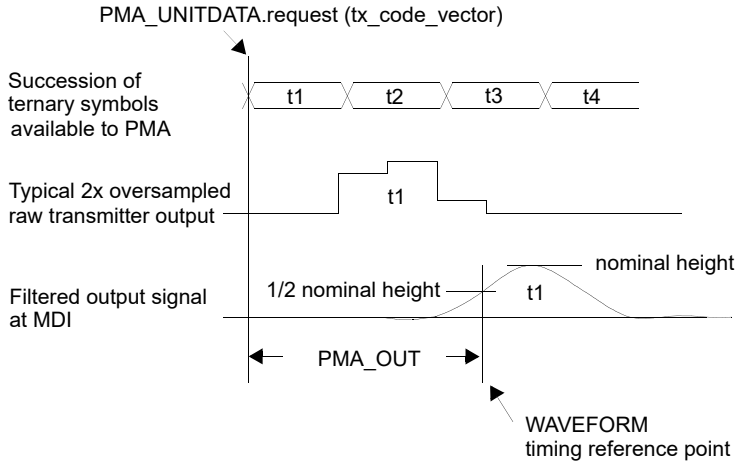

Figure 23–29—PMA TRANSMIT timing while tx_code_vector = DATA

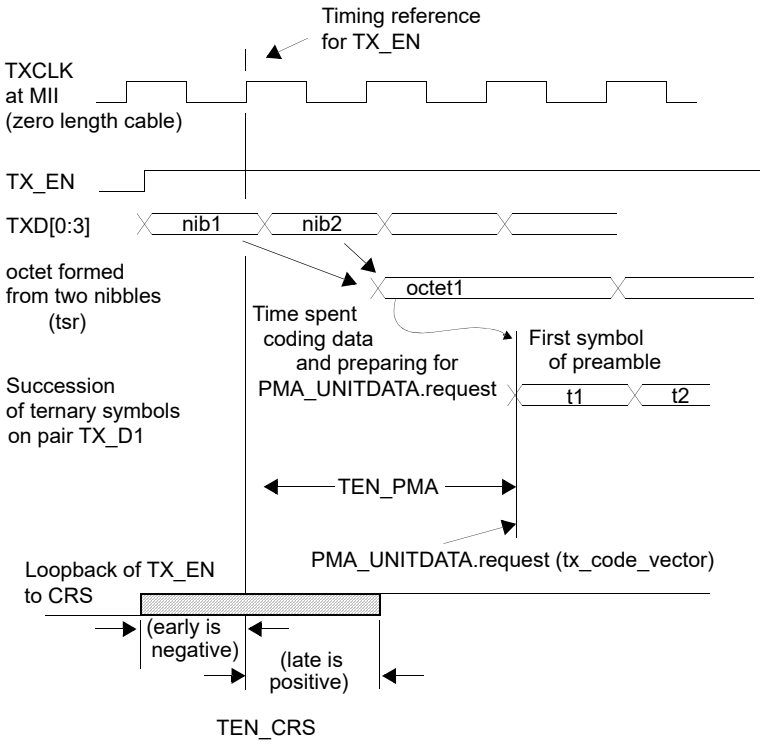

Figure 23–30—PCS TRANSMIT timing at start of packet

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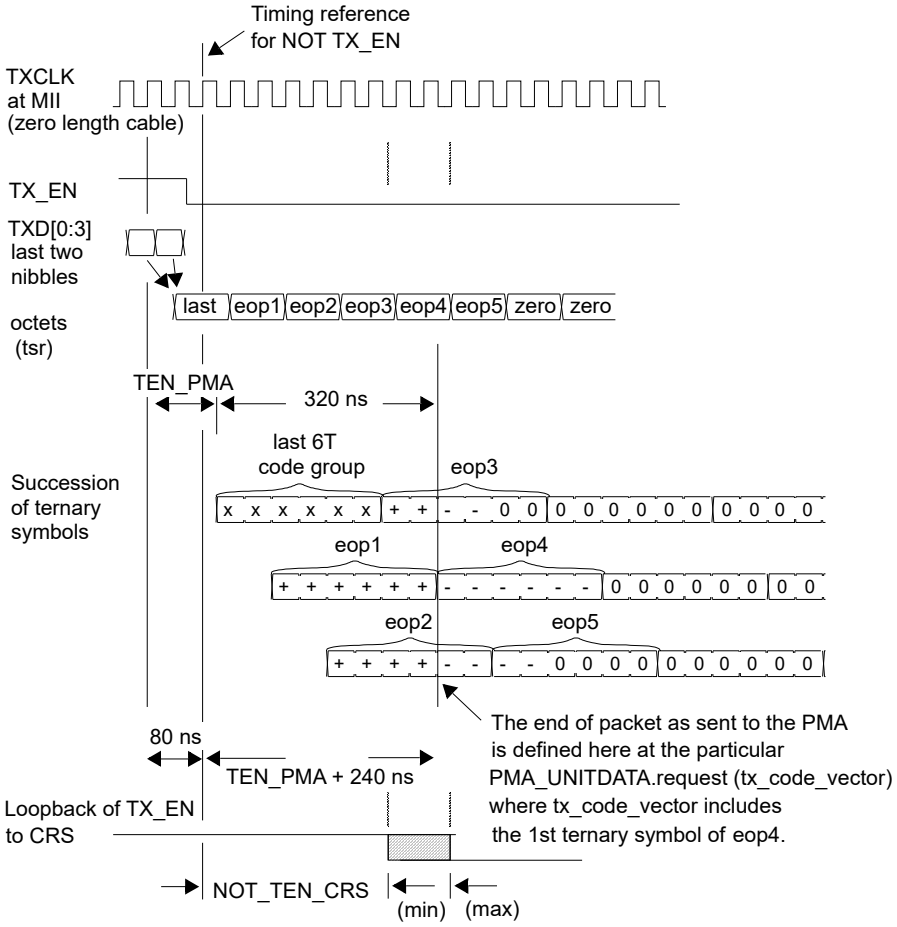

Figure 23–31—PCS TRANSMIT timing end of normal packet

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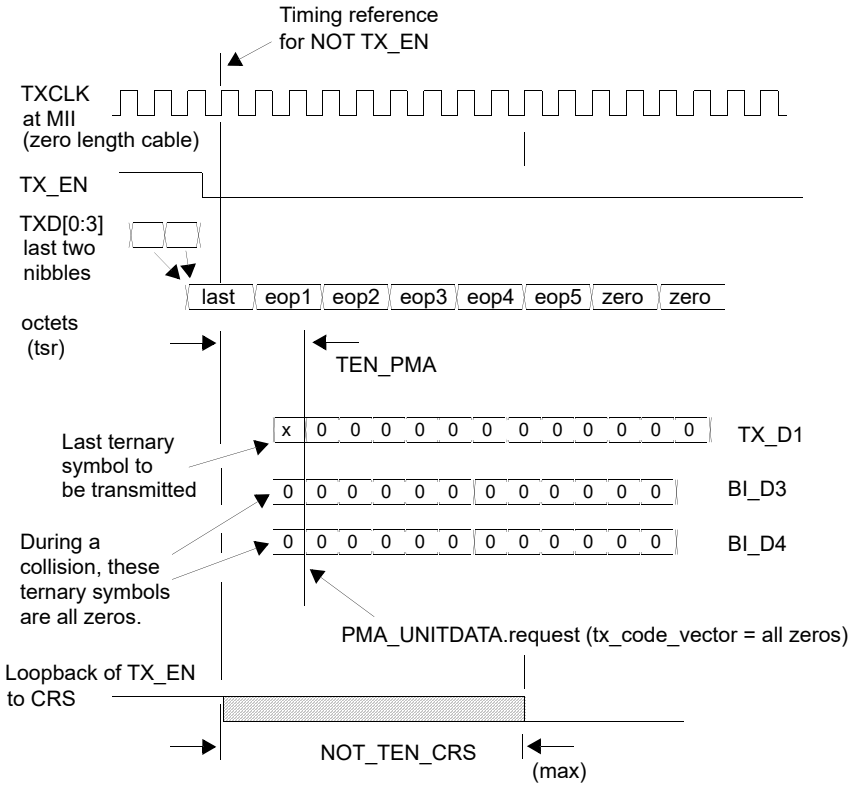

Figure 23–32—PCS TRANSMIT timing end of colliding packet

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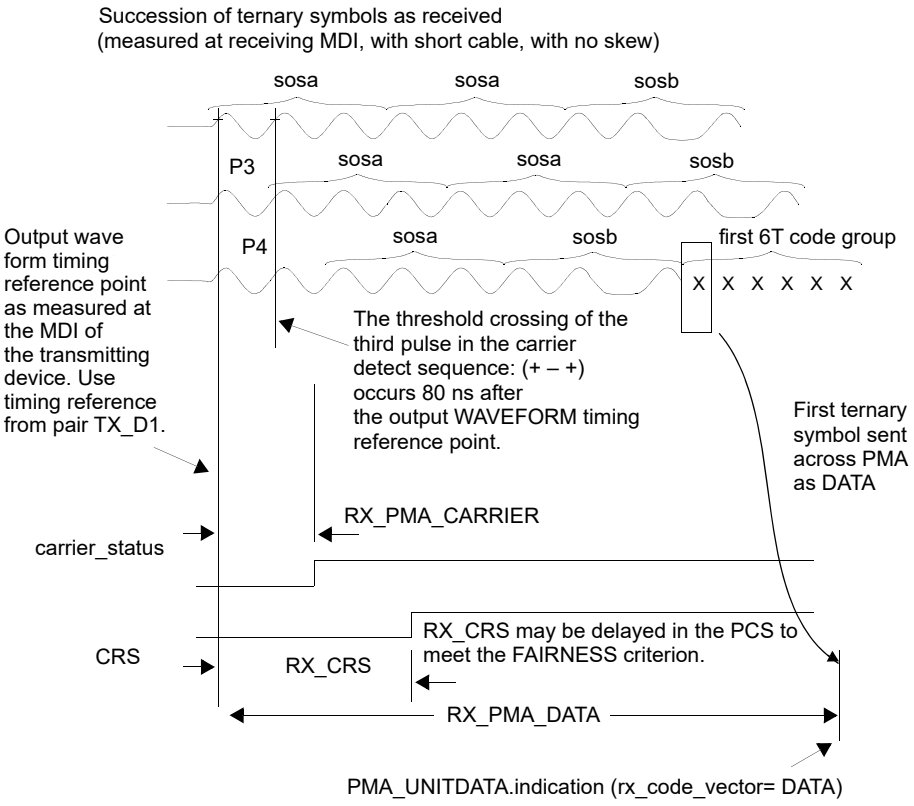

Figure 23–33—PMA RECEIVE timing start of packet

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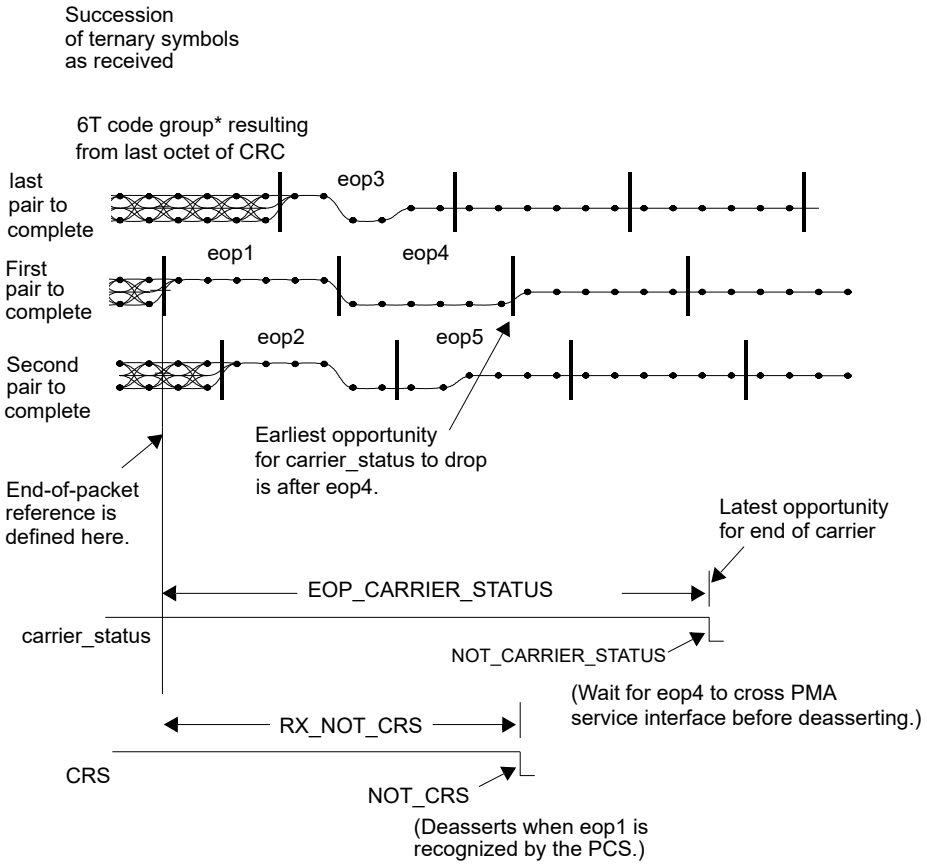

*RX_DV deasserts after sending the last nibble of this decoded octet across the MII.
CRS may deassert prior to that time.

Figure 23–34—PMA RECEIVE timing end of normal packet

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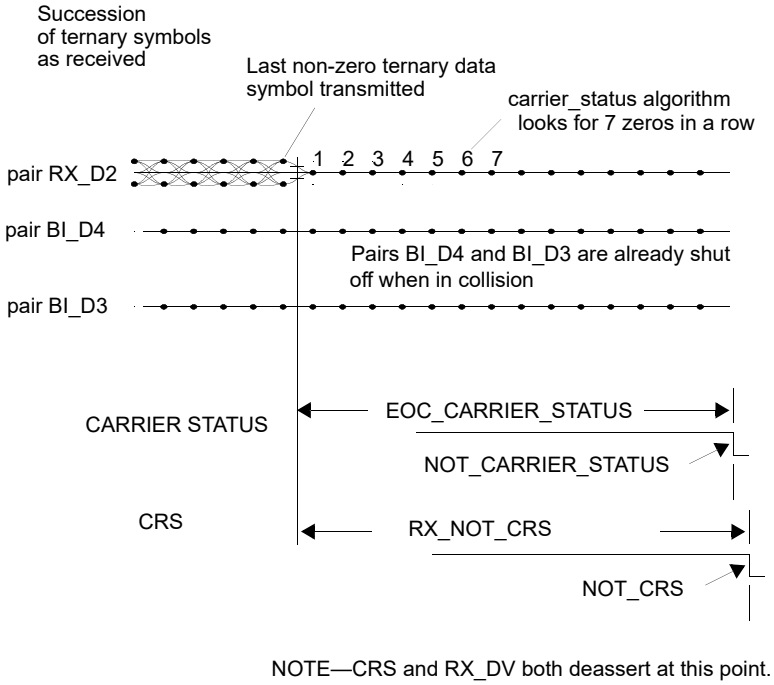

Figure 23–35—PMA RECEIVE timing end of colliding packet

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23.12 Protocol implementation conformance statement (PICS) proforma for Clause 23, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100BASE-T4[55]

23.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 23, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100BASE-T4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

23.12.2 Identification

23.12.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

23.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2018, Clause 23, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100BASE-T4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2018.)	

Date of Statement	

[55] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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23.12.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*MII	Exposed MII interface	23.1.5.3	O		Devices supporting this option also have to support the PCS option
*PCS	PCS functions	23.1.5.2	O		Required for integration with DTE or MII
*PMA	Exposed PMA service interface	23.1.5.2	O		Required for integration into symbol level repeater core
*XVR	Internal wiring crossover	23.7.2	O		Usually implemented in repeater, usually not in DTE
*NWY	Support for optional Auto-Negotiation (Clause 28)	23.1.5.4	O		Required if Auto-Negotiation is implemented
*INS	Installation / cable		O		Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer

23.12.4 PICS proforma tables for the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T4

23.12.4.1 Compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
CCO-1	Compatibility at the MDI	23.1.5.1	M		

23.12.4.2 PCS Transmit functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCT-1	PCS Transmit function	23.2.1.2	PCS:M		Complies with state diagram Figure 23–8
PCT-2	Data encoding	23.2.1.2	PCS:M		8B6T with DC balance encoding rules
PCT-3	Order of ternary symbol transmission	Annex 23A	PCS:M		Leftmost symbol of each 6T code group first

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23.12.4.3 PCS Receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR1	PCS Receive function	23.2.1.3	PCS:M		Complies with state diagram Figure 23–9
PCR2	Value of RXD<3:0> while RXDV is deasserted	23.2.1.3	PCS:M		All zeros
PCR3	Data decoding	23.2.1.3	PCS:M		8B6T with error detecting rules
PCR4	Value of dc_balance_error, eop_error and codeword_error at times other than those specified in the error detecting rules.	23.2.1.3	PCS:M		OFF
PCR5	Codeword_error indication sets RX_ER when	23.2.1.3	PCS:M		During transfer of both affected data nibbles across the MII
PCR6	Dc_balance_error sets RX_ER when	23.2.1.3	PCS:M		During transfer of both affected nibbles across the MII
PCR7	Eop_error sets RX_ER when	23.2.1.3	PCS:M		During transfer of last decoded data nibble across the MII
PCR8	Action taken if carrier_status is truncated due to early deassertion of carrier_status	23.2.1.3	PCS:M		Assert RX_ER, and then deassert RX_DV

23.12.4.4 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	PCS Reset function executed when	23.2.1.1	PCS:M		Power-on, or the receipt of a reset request from the management entity
PCO2	PCS Error Sense function	23.2.1.4	PCS:M		Complies with state diagram Figure 23–10
PCO3	Signaling of RX_ER to MII	23.2.1.4	PCS:M		Before last nibble of Clause 4 MAC frame has passed across MII
PCO4	Timing of rxerror_status	23.2.1.4	PCS:M		Causes RX_ER to appear on the MII no later than last nibble of first data octet
PCO5	PCS Carrier Sense function	23.2.1.5	PCS:M		Controls MII signal CRS according to rules in 23.2.1.5
PCO6	MII signal COL is asserted when	23.2.1.6	PCS:M		Upon detection of a PCS collision
PCO7	At other times COL remains	23.2.1.6	PCS:M		Deasserted
PCO8	Loopback implemented in accordance with 22.2.4.1.2	23.2.2.2	PCS:M		Redundantly specified in 22.2.4.1.2

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23.12.4.4 Other PCS functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PCO9	No spurious signals emitted on the MDI during or after power down	23.2.2.2	M		
PCO10	PMA frame structure	23.2.3	M		Conformance to Figure 23–6
PCO11	PMA_UNITDATA messages	23.2.3	PMA:M		Have a clock for both directions

23.12.4.5 PCS state diagram variables

Item	Feature	Subclause	Status	Support	Value/Comment
PCS1	Timing of eop adjusted such that the last nibble sent across the MII with RX_DV asserted is	23.2.4.2	PCS:M		Last nibble of last decoded data octet in a packet
PCS2	Transmission of octets on the three transmit pairs	23.2.4.2	PCS:M		Transmission order is: TX_D1, then BI_D3, and then BI_D4
PCS3	Value of tsr during first 16 TX_CLK cycles after TX_EN is asserted	23.2.4.2	PCS:M		sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosb, sosb, sosb, sosb, sosb, sosb
PCS4	Value of tsr during first 10 TX_CLK cycles after TX_EN is deasserted	23.2.4.2	PCS:M		eop1, eop1, eop2, eop2, eop3, eop3, eop4, eop4, eop5, eop5
PCS5	TX_ER causes transmission of	23.2.4.2	PCS:M		bad_code
PCS6	TX_ER received during the first 16 TX_CLK cycles causes	23.2.4.2	PCS:M		Transmission of **bad_code** during 17th and 18th clock cycles
PCS7	Action taken in event TX_EN falls on an odd nibble boundary	23.2.4.2	PCS:M		Extension of TX_EN by one TX_CLK cycle, and transmission of bad_code
PCS8	Transmission when TX_EN is not asserted	23.2.4.2	PCS:M		zero_code
PCS9	TX_CLK generated synchronous to	23.2.4.2	PCS:M		tw1_timer

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23.12.4.6 PMA service interface

Item	Feature	Subclause	Status	Support	Value/Comment
PMS1	Continuous generation of PMA_TYPE	23.3.1.2	M		
PMS2	Generation of PMA_UNIT-DATA.indication (DATA) messages	23.3.3.2	M		synchronous with data received at the MDI
PMS3	Generation of PMA_CARRIER.indication message	23.3.4.2	M		ON/OFF
PMS4	Generation of PMA_LINK.indication message	23.3.5.2	M		FAIL/READY/OK
PMS5	Link_control defaults on power-on or reset to	23.3.6.2	M		ENABLE
PMS6	Action taken in SCAN_FOR_CARRIER mode	23.3.6.4	NWY:M		Enables link integrity state diagram, but blocks passage into LINK_PASS
PMS7	Reporting of link_status while in SCAN_FOR_CARRRIER mode	23.3.6.4	NWY:M		FAIL / READY
PMS8	Reporting of link_status while in DISABLE mode	23.3.6.4	NWY:M		FAIL
PMS9	Action taken in ENABLE mode	23.3.6.4	NWY:M		enables data processing functions
PMS10	Generation of PMA_RXERROR	23.3.7.2	M		ERROR / NO_ERROR

23.12.4.7 PMA Transmit functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMT1	Transmission while (tx_code_vector=DATA) * (pma_carrier=OFF)	23.4.1.2	M		tx_code_vector[TX_D1] tx_code_vector[BI_D3] tx_code_vector[BI_D4]
PMT2	Transmission from time (tx_code_vector=DATA) * (pma_carrier=ON), until (tx_code_vector=IDLE	23.4.1.2	M		tx_code_vector[TX_D1] CS0 CS0
PMT3	Transmission while tx_code_vector=IDLE	23.4.1.2	M		Idle signal TP_DIL_100
PMT4	Duration of silence between link test pulses	23.4.1.2	M		1.2 ms ± 0.6 ms
PMT5	Link test pulse composed of	23.4.1.2	M		CS-1, CS1 transmitted on TX_D1

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23.12.4.7 PMA Transmit functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PMT6	Following a packet, TP_IDL_100 signal starts with	23.4.1.2	M		Period of silence
PMT7	Effect of termination of TP_IDL_100	23.4.1.2	M		No delay or corruption of subsequent packet
PMT8	Zero crossing jitter of link test pulse	23.4.1.2	M		Less than 4 ns p-p
PMT9	Action taken when xmit=disable	23.4.1.2	M		Transmitter behaves as if tx_code_vector=IDLE

23.12.4.8 PMA Receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMR1	Reception and translation of data with ternary symbol error ratio less than	23.4.1.3	M		One part in 10^8
PMR2	Assertion of pma_carrier=ON upon reception of test signal	23.4.1.4	M		Test signal is a succession of three data values, produced synchronously with a 25 MHz clock, both preceded and followed by 100 symbols of silence. The three values are: 467 mV, –225 mV, and then 467 mV again
PMR3	condition required to turn off pma_carrier	23.4.1.4	M		Either of a) Seven consecutive zeros b) Reception of eop1 per 23.4.1.4
PMR4	Value of carrier_status while rcv=ENABLE	23.4.1.4	M		pma_carrier
PMR5	Value of carrier_status while rcv=DISABLE	23.4.1.4	M		OFF

23.12.4.9 Link Integrity functions

Item	Feature	Subclause	Status	Support	Value/Comment
LIF1	Link Integrity function complies with	23.4.1.5	M		State diagram Figure 23–12

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23.12.4.10 PMA Align functions

Item	Feature	Subclause	Status	Support	Value/Comment
ALN1	Generation of PMA_UNITDATA.indication (PREAMBLE) messages	23.4.1.6	M		
ALN2	Ternary symbols transferred by first PMA_UNITADATA.indication (DATA) message	23.4.1.6	M		rx_code_vector[BI_D3]: first ternary symbol of first data code group rx_code_vector[BI_D2]: two ternary symbols prior to start of second data code group rx_code_vector[BI_D4]: four ternary symbols prior to start of third data code group
ALN3	PMA_UNITDATA.indication (DATA) messages continue until carrier_status=OFF	23.4.1.6	M		
ALN4	While carrier_status=OFF, PMA emits message	23.4.1.6	M		PMA_UNITDATA.indication (IDLE)
ALN5	Failure to recognize SSD generates rxerror_status=ERROR	23.4.1.6	M		
ALN6	Action taken when carrier_status=OFF	23.4.1.6	M		Clear rxerror_status
ALN7	Action taken if first packet is used for alignment	23.4.1.6	M		PMA emits PMA_UNITDATA..indication (PREAMBLE)
ALN8	Tolerance of line skew	23.4.1.6	M		60 ns
ALN9	Detection of misplaced **sosb** 6T code group caused by 3 or fewer ternary symbols in error	23.4.1.6	M		
ALN10	Action taken if **rcv**=disable	23.4.1.6	M		PMA emits PMA_UNITDATA..indication (IDLE)

23.12.4.11 Other PMA functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMO1	PMA Reset function	23.4.1.1	M		
PMO2	Suitable clock recovery	23.4.1.7	M		

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23.12.4.12 Isolation requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ISO1	Values of all components used in test circuits	23.5	M		Accurate to within ±1% unless required otherwise
ISO2	Electrical isolation meets	23.5.1.1	M		1500 V at 50–60 Hz for 60 s per IEC 60950: 1991 *or* 2250 Vdc for 60 s per IEC 60950: 1991 *or* Ten 2400 V pulses per IEC 60060
ISO3	Insulation breakdown during isolation test	23.5.1.1	M		None per IEC 60950: 1991
ISO4	Resistance after isolation test	23.5.1.1	M		At least 2 M Ω

23.12.4.13 PMA electrical requirements

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	Conformance to all transmitter specifications in 23.5.1.2	23.5.1.2	M		
PME2	Transmitter load unless otherwise specified	23.5.1.2	M		100 Ω
PME3	Peak differential output voltage	23.5.1.2.1	M		3.15–3.85 V
PME4	Differential transmit template at MDI	23.5.1.2.2	M		Table 23–2
PME5	Differential MDI output template voltage scaling	23.5.1.2.2	M		3.15– 3.85 V
PME6	Interpolation between points on transmit template	23.5.1.2.2	M		Linear
PME7	Differential link pulse template at MDI	23.5.1.2.2	M		Table 23–2
PME8	Differential link pulse template scaling	23.5.1.2.2	M		Same value as used for differential transmit template scaling
PME9	Interpolation between point on link pulse template	23.5.1.2.2	M		Linear
PME10	State when transmitting seven or more consecutive CS0 during TP_IDL-100 signal	23.5.1.2.2	M		–50 mV to 50 mV
PME11	Limit on magnitude of harmonics measured at MDI	23.5.1.2.2	M		27 dB below fundamental
PME12	Differential output ISI	23.5.1.2.3	M		Less than 9%

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23.12.4.13 PMA electrical requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME13	Measurement of ISI and peak-to-peak signal voltage	23.5.1.2.3	M		Halfway between nominal zero crossing of the observed eye pattern
PME14	Transfer function of 100BASE-T4 transmit test filter	23.5.1.2.3	M		Third-order Butterworth filter with –3 dB point at 25.0 MHz
PME15	Reflection loss of 100BASE-T4 transmit test filter and 100 W load across the frequency range 2–12.5 MHz	23.5.1.2.3	M		Exceeds 17 dB
PME16	Differential output impedance	23.5.1.2.4	M		Provide return loss into 100 Ω of 17 dB from 2.0 to 12.5 MHz
PME17	Maintenance of return loss	23.5.1.2.4	M		At all times PHY is fully powered
PME18	Droop as defined in Figure 23–18 during transmission of eop1 and eop4	23.5.1.2.4	M		Less than 6%
PME19	Output timing jitter	23.5.1.2.5	M		No more than 4 ns peak-to-peak
PME20	Measurement of output timing jitter	23.5.1.2.5	M		Other transmit outputs connected to 100BASE-T4 ISI test filter or 100 Ω load
PME21	Minimum transmitter impedance balance	23.5.1.2.6	M		$29 - 17\log\left(\frac{f}{10}\right)$ dB
PME22	Transmitter common-mode rejection; effect of E_{cm} as shown in Figure 23–20 upon E_{dif}	23.5.1.2.8	M		Less than 100 mV
PME23	Transmitter common-mode rejection; effect of E_{cm} as shown in Figure 23–20 upon edge jitter	23.5.1.2.8	M		Less than 1.0 ns
PME24	E_{cm} used for common-mode rejection tests	23.5.1.2.8	M		15 V peak, 10.1 MHz sine wave
PME25	Transmitter faults; response to indefinite application of short circuits	23.5.1.2.9	M		Withstand without damage and resume operation after fault is removed
PME26	Transmitter faults; response to 1000 V common-mode impulse per IEC 60060	23.5.1.2.9	M		Withstand without damage
PME27	Shape of impulse used for common-mode impulse test	23.5.1.2.9	M		0.3/50 μs as defined in IEC 60060
PME28	Ternary symbol transmission rate	23.5.1.2.10	M		25.000 MHz ± 0.01%

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23.12.4.13 PMA electrical requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME29	Conformance to all receiver specifications in 23.5.1.3	23.5.1.3	M		
PME30	Action taken upon receipt of differential signals that were transmitted within the constraints of 23.5.1.2 and have passed through worst-case UTP model	23.5.1.3.1	M		Correctly translated into PMA_UNITDATA messages
PME31	Action taken upon receipt of link test pulse	23.5.1.3.1	M		Accept as a link test pulse
PME32	Test configuration for data reception and link test pulse tests	23.5.1.3.1	M		Using worst-case UTP model, and with a connection less than one meter in length
PME33	Bit loss	23.5.1.3.2	M		No more than that specified in 23.5.1.3.1
PME34	Reaction of pma_carrier to signal less than 325 mV peak	23.5.1.3.2	M		Does not set pma_carrier=ON
PME35	Reaction of pma_carrier to continuous sinusoid less than 1.7 MHz	23.5.1.3.2	M		Does not set pma_carrier=ON
PME36	Reaction of pma_carrier to single cycle or less	23.5.1.3.2	M		Does not set pma_carrier=ON
PME37	Reaction of pma_carrier to fast link pulse as defined in Clause 28	23.5.1.3.2	M		Does not set pma_carrier=ON
PME38	Reaction of pma_carrier to link integrity test pulse signal TP_IDL_100	23.5.1.3.2	M		Does not set pma_carrier=ON
PME39	Differential input impedance	23.5.1.3.3	M		Provide return loss into 100 Ω of 17 dB from 2.0 to 12.5 MHz
PME40	Maintenance of return loss	23.5.1.3.3	M		At all times PHY is fully powered
PME41	Droop as defined in Figure 23–18 during reception of test signal defined in Figure 23–19	23.5.1.3.3	M		Less than 6%
PME42	Receiver common-mode rejection; effect of E_{cm} as shown in Figure 23–24	23.5.1.3.4	M		Receiver meets 23.5.1.3.1
PME43	E_{cm} used for common-mode rejection tests	23.5.1.3.4	M		25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns
PME44	Receiver faults; response to indefinite application of short circuits	23.5.1.3.5	M		Withstand without damage and resume operation after fault is removed

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23.12.4.13 PMA electrical requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME45	Receiver faults; response to 1000 V common-mode impulse per IEC 60060	23.5.1.3.5	M		Withstand without damage
PME46	Shape of impulse used for common-mode impulse test	23.5.1.3.5	M		0.3/50 μs as defined in IEC 60060
PME47	Receiver properly receives data have a worst-case ternary symbol range	23.5.1.3.6	M		25.00 MHz ± 0.01%
PME48	Steady-state current consumption	23.5.2	MII:M		0.75 A maximum
PME49	PHY operating voltage range	23.5.2	MII:M		Includes worst voltage available from MII
PME50	Extraneous signals induced on the MII control circuits during normal power-up and power-down	23.5.2	M		None

23.12.4.14 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LNK1	Cable used	23.6.1	INS:M		Four pairs of balanced cabling, Category 3 or better, with a nominal characteristic impedance of 100 Ω
LNK2	Source and load impedance used for cable testing (unless otherwise specified)	23.6.2	INS:M		100 Ω
LNK3	Insertion loss of simplex link segment	23.6.2.1	INS:M		Less than 12 dB
LNK4	Source and load impedances used to measure cable insertion loss	23.6.2.1	INS:M		Meet 23.5.1.2.4 and 23.5.1.3.3
LNK5	Characteristic impedance over the range 2–12.5 MHz	23.6.2.2	INS:M		85–115 Ω
LNK6	NEXT loss between 2 and 12.5 MHz	23.6.2.3.1	INS:M		Greater than $24.5 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK7	MDNEXT loss between 2 and 12.5 MHz	23.6.2.3.2	INS:M		Greater than $21.4 - 15\log\left(\frac{f}{12.5}\right)$ dB

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23.12.4.14 Characteristics of the link segment *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
LNK8	ELFEXT loss between 2 and 12.5 MHz	23.6.2.3.3	INS:M		Greater than $23.1 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK9	MDELFEXT loss between 2 and 12.5 MHz	23.6.2.3.4	INS:M		Greater than $20.9 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK10	Propagation delay	23.6.2.4.1	INS:M		Less than 570 ns
LNK11	Propagation delay per meter	23.6.2.4.2	INS:M		Less than 5.7 ns/m
LNK12	Skew	23.6.2.4.3	INS:M		Less than 50 ns
LNK13	Variation in skew once installed	23.6.2.4.3	INS:M		Less than ± 10 ns, within constraint of LNK8
LNK14	Noise level	23.6.3	INS:M		Such that objective error ratio is met
LNK15	MDNEXT noise	23.6.3.1	INS:M		Less than 325 mVp
LNK16	MDFEXT noise	23.6.3.2	INS:M		Less than 87 mVp
LNK17	Maximum length of Category 5, 25-pair jumper cables	23.6.3.2	INS:M		10 m

23.12.4.15 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	23.7.1	M		IEC 60603-7: 1990
MDI2	Connector used on PHY	23.7.1	M		Jack (as opposed to plug)
MDI3	Crossover in every twisted-pair link	23.7.2	INS:M		
MDI4	MDI connector that implements the crossover function	23.7.2	XVR:M		Marked with “X”

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23.12.4.16 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
SAF1	Conformance to safety specifications	23.9.1	M		IEC 60950: 1991
SAF2	Installation practice	23.9.2.1	INS:M		Sound practice, as defined by applicable local codes
SAF3	Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection	23.9.2.2	M		
SAF4	Care taken during installation to ensure that noninsulated network cable conductors do not make electrical contact with unintended conductors or ground	23.9.2.3	INS:M		
SAF5	Application of voltages specified in 23.9.2.4 does not result in any safety hazard	23.9.2.4	M		
SAF6	Conformance with local and national codes for the limitation of electromagnetic interference	23.9.3.1	INS:M		

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23.12.4.17 Timing requirements

Item	Feature	Subclause	Status	Support	Value/Comment
TIM1	PMA_OUT	23.11.3	PMA:M		1 to 9.5 BT
TIM2	TEN_PMA + PMA_OUT	23.11.3	PCS:M		7 to 17.5 BT
TIM3	TEN_CRS	23.11.3	PCS:M		0 to +4 BT
TIM4	NOT_TEN_CRS	23.11.3	PCS:M		28 to 36 BT
TIM5	RX_PMA_CARRIER	23.11.3	PMA:M		Less than 15.5 BT
TIM6	RX_CRS	23.11.3	PCS:M		Less than 27.5 BT
TIM7	RX_NOT_CRS	23.11.3	PCS:M		0 to 51.5 BT
TIM8	FAIRNESS	23.11.3	PCS:M		0 to 28 BT
TIM9	RX_PMA_DATA	23.11.3	PMA:M		67 to 90.5 BT
TIM10	EOP_CARRIER_STATUS	23.11.3	M		51 to 74.5 BT
TIM11	EOC_CARRIER_STATUS	23.11.3	M		3 to 50.5 BT
TIM12	RX_RXDV	23.11.3	PCS:M		81 to 114.5 BT
TIM13	RX_PMA_ERROR	23.11.3	M		Allowed limits equal the actual RX_PMA_DATA time for the device under test plus from 0 to 20 BT
TIM14	RX_COL	23.11.3	PCS:M		Less than 27.5 BT
TIM15	RX_NOT_COL	23.11.3	PCS:M		Less than 51.5 BT
TIM16	TX_NOT_COL	23.11.3	PCS:M		Less than 36 BT
TIM17	TX_SKEW	23.11.3	M		Less than 0.5 BT
TIM18	CRS_PMA_DATA	23.11.3	PMA:M		Less than 78.5 BT
TIM19	COL_to_BI_D3/4_OFF	23.11.3	PMA:M		Less than 40 BT

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24. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

24.1 Overview

24.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer that are common to a family of 100 Mb/s Physical Layer implementations, collectively known as 100BASE-X. There are currently two embodiments within this family: 100BASE-TX and 100BASE-FX. 100BASE-TX specifies operation over two pairs of twisted-pair Category 5 cabling. 100BASE-FX specifies operation over two optical fibers. The term 100BASE-X is used when referring to issues common to both 100BASE-TX and 100BASE-FX.

The 100BASE-X may support the capability of Energy-Efficient Ethernet (EEE) as described in Clause 78. When a transmitting station of a link with this capability detects low link utilization, it can request the local PHY transmitter to enter the Low Power Idle (LPI) mode and send appropriate symbols over the link. Upon receiving and decoding those symbols, the link partner's receiver can enter the LPI mode. The transmit and receive paths can enter and exit low power states independently. Energy is conserved by deactivating the corresponding functional blocks of individual path. Only 100BASE-TX supports this optional capability.

100BASE-X leverages the Physical Layer standards of ISO/IEC 9314 and ANSI X3T12 (FDDI) through the use of their Physical Medium Dependent (PMD) sublayers, including their Medium Dependent Interfaces (MDI). For example, ANSI INCITS 263-1995 (TP-PMD) defines a 125 Mb/s, full duplex signaling system for twisted-pair wiring that forms the basis for 100BASE-TX as defined in Clause 25. Similarly, ISO/IEC 9314-3:1990 defines a system for transmission on optical fiber that forms the basis for 100BASE-FX as defined in Clause 26.

100BASE-X maps the interface characteristics of the FDDI PMD sublayer (including MDI) to the services expected by the CSMA/CD MAC. 100BASE-X can be extended to support any other full duplex medium requiring only that the medium be PMD compliant.

24.1.2 Objectives

The following are the objectives of 100BASE-X:

a) Support the CSMA/CD MAC in the half duplex and the full duplex modes of operation.
b) Support the 100BASE-T MII, repeater, and optional Auto-Negotiation.
c) Provide 100 Mb/s data rate at the MII.
d) Support cable plants using Category 5 twisted-pair, 150 Ω STP or cabled optical fiber, compliant with ISO/IEC 11801.
e) Allow for a nominal network extent of 200–400 m, including
    1) Unshielded twisted-pair links of 100 m
    2) Two repeater networks of approximately 200 m span
    3) One repeater network of approximately 300 m span (using fiber)
    4) DTE/DTE links of approximately 400 m (half duplex mode using fiber) and 2 km (full duplex mode using multimode fiber.
f) Preserve full duplex behavior of underlying PMD channels.
g) Optionally support EEE through the function of LPI (see Clause 78), available only for 100BASE-TX.

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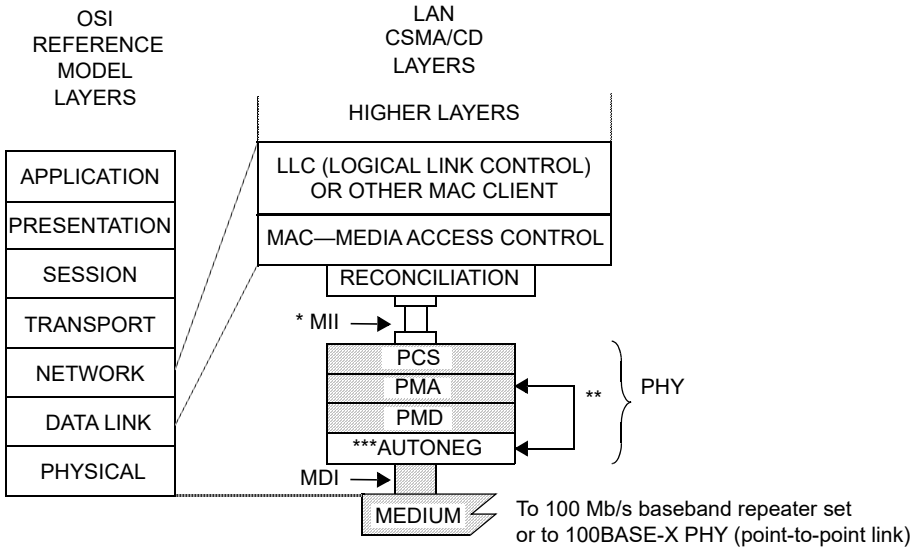
24.1.3 Relationship of 100BASE-X to other standards

Figure 24–1 depicts the relationships among the 100BASE-X sublayers (shown shaded), other 100BASE-T sublayers, the CSMA/CD MAC, and the IEEE 802.2 LLC.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional.
** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indicate.
*** AUTONEG is mandatory for EEE capability and optional otherwise.

Figure 24–1—Type 100BASE-X PHY relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

24.1.4 Summary of 100BASE-X sublayers

The following provides an overview of the 100BASE-X sublayers that are embodied in the 100BASE-X Physical Layer device (PHY).[56]

24.1.4.1 Physical Coding Sublayer (PCS)

The PCS interface is the Media Independent Interface (MII) that provides a uniform interface to the Reconciliation sublayer for all 100BASE-T PHY implementations (e.g., 100BASE-X and 100BASE-T4). 100BASE-X, as other 100BASE-T PHYs, is modeled as providing services to the MII. This is similar to the use of an AUI interface.

The 100BASE-X PCS realizes all services required by the MII, including the following:

a) Encoding (decoding) of MII data nibbles to (from) five-bit code-groups (4B/5B).
b) Generating Carrier Sense and Collision Detect indications.

[56] The 100BASE-X PHY should not be confused with the FDDI PHY, which is a sublayer functionally aligned to the 100BASE-T PCS.

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c) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMA.
d) Mapping of Transmit, Receive, Carrier Sense and Collision Detection between the MII and the underlying PMA.
e) Optionally, interpreting and generating MII data signals to enable or disable the LPI mode.

24.1.4.2 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS and other bit-oriented clients (e.g., repeaters) to support the use of a range of physical media. The 100BASE-X PMA performs the following functions:

a) Mapping of transmit and receive code-bits between the PMA's client and the underlying PMD.
b) Generating a control signal indicating the availability of the PMD to a PCS or other client, also synchronizing with Auto-Negotiation when implemented.
c) Optionally, generating indications of activity (carrier) and carrier errors from the underlying PMD.
d) Optionally, sensing receive channel failures and transmitting the Far-End Fault Indication; and detecting the Far-End Fault Indication.
e) Optionally, receiving and processing LPI control signals from the PCS.
f) Recovery of clock from the NRZI data supplied by the PMD.

24.1.4.3 Physical Medium Dependent (PMD) sublayer

100BASE-X uses the FDDI signaling standards ISO/IEC 9314-3:1990 and ANSI INCITS 263-1995 (TP-PMD). These signaling standards, called PMD sublayers, define 125 Mb/s, full duplex signaling systems that accommodate multimode optical fiber and twisted-pair cabling. 100BASE-X uses the PMDs specified in these standards with the PMD Service Interface specified in 24.4.1.

The MDI, logically subsumed within the PMD, provides the actual medium attachment, including connectors, for the various supported media.

100BASE-X does not specify the PMD and MDI other than including the appropriate standard by reference along with the minor adaptations necessary for 100BASE-X. Figure 24–2 depicts the relationship between 100BASE-X and the PMDs of ISO/IEC 9314-3:1990 (for 100BASE-FX) and ANSI INCITS 263-1995 (for 100BASE-TX). The PMDs (and MDIs) for 100BASE-TX and 100BASE-FX are specified in subsequent clauses of this standard.

24.1.4.4 Auto-Negotiation

Auto-Negotiation shall be implemented for EEE capability. See Clause 28.

24.1.5 Inter-sublayer interfaces

There are a number of interfaces employed by 100BASE-X. Some (such as the PMA and PMD interfaces) use an abstract service model to define the operation of the interface. The PCS Interface is defined as a set of physical signals, in a medium-independent manner (MII). Figure 24–3 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 100BASE-X.

It is important to note that, while this specification defines interfaces in terms of bits, nibbles, and code-groups, implementations may choose other data path widths for implementation convenience. The only exceptions are: a) the MII, which, when implemented, uses a nibble-wide data path as specified in Clause 22, and b) the MDI, which uses a serial, physical interface.

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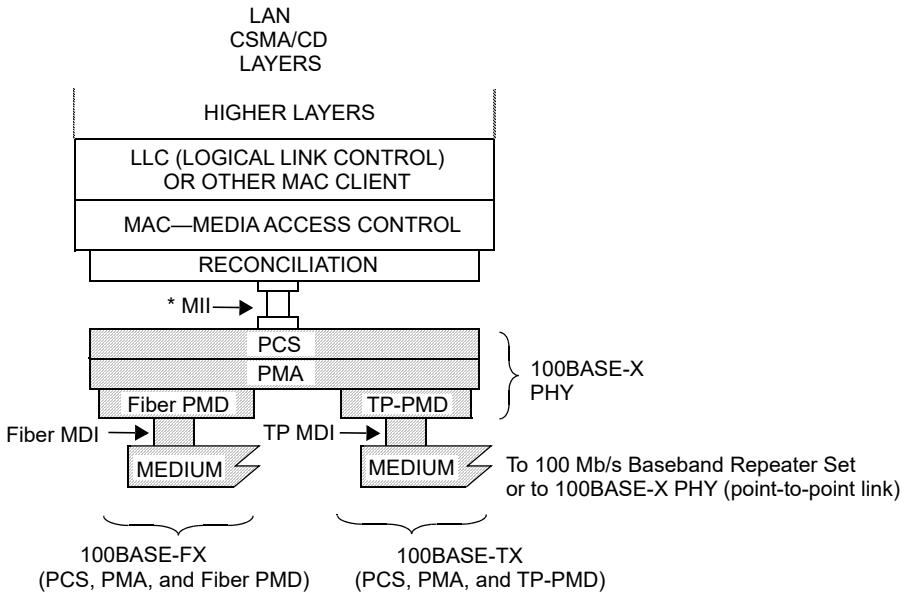

MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
Fiber PMD = PHYSICAL MEDIUM DEPENDENT SUBLAYER FOR FIBER
TP-PMD = PHYSICAL MEDIUM DEPENDENT SUBLAYER FOR TWISTED PAIRS

NOTE—The PMD sublayers are mutually independent.
* MII is optional.

Figure 24–2—Relationship of 100BASE-X and the PMDs

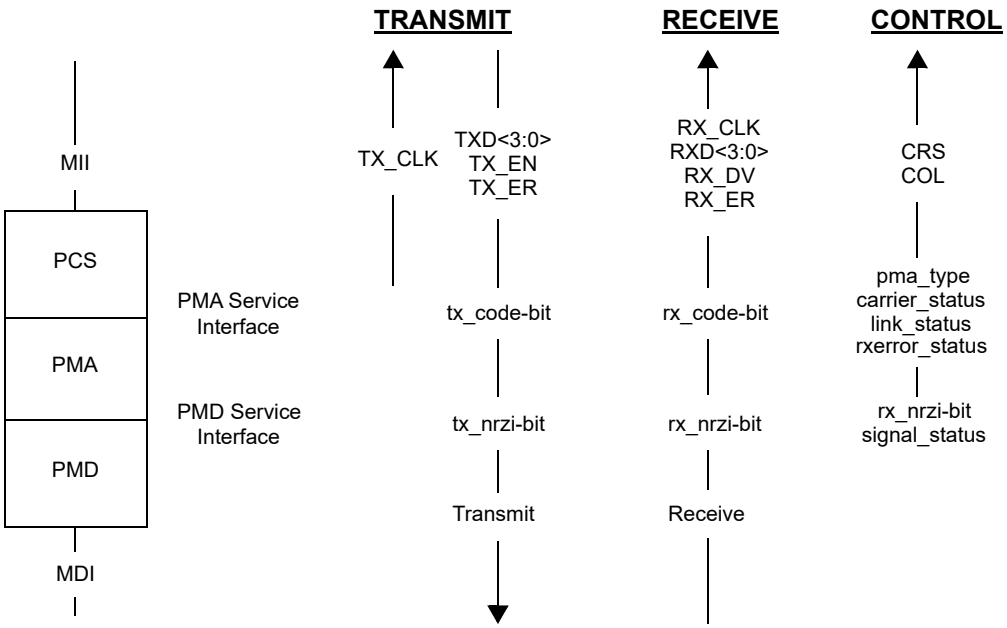

Figure 24–3—Interface mapping

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24.1.6 Functional block diagram

Figure 24–4 provides a functional block diagram of the 100BASE-X PHY. Signals or functions shown with dashed lines are optional.

24.1.7 State diagram conventions

The body of this standard is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5; state diagram timers follow the conventions of 14.2.3.2.

24.2 Physical Coding Sublayer (PCS)

24.2.1 Service Interface (MII)

The PCS Service Interface allows the 100BASE-X PCS to transfer information to and from the MAC (via the Reconciliation sublayer) or other PCS client, such as a repeater. The PCS Service Interface is precisely defined as the Media Independent Interface (MII) in Clause 22.

In this clause, the setting of MII variables to TRUE or FALSE is equivalent, respectively, to “asserting” or “deasserting” them as specified in Clause 22.

24.2.2 Functional requirements

The PCS comprises the Transmit, Receive, and Carrier Sense functions for 100BASE-T. In addition, the collisionDetect signal required by the MAC (COL on the MII) is derived from the PMA code-bit stream. The PCS shields the Reconciliation sublayer (and MAC) from the specific nature of the underlying channel. Specifically for receiving, the 100BASE-X PCS passes to the MII a sequence of data nibbles derived from incoming code-groups, each composed of five code-bits, received from the medium. Code-group alignment and MAC packet delimiting is performed by embedding special non-data code-groups. The MII uses a nibble-wide, synchronous data path, with packet delimiting being provided by separate TX_EN and RX_DV signals. The PCS provides the functions necessary to map these two views of the exchanged data. The process is reversed for transmit.

The following provides a detailed specification of the functions performed by the PCS, which comprise five parallel processes (Transmit, Transmit Bits, Receive, Receive Bits, and Carrier Sense). Figure 24–4 includes a functional block diagram of the PCS.

The Receive Bits process accepts continuous code-bits via the PMA_UNITDATA.indicate primitive. Receive monitors these bits and generates RXD<3:0>, RX_DV, and RX_ER on the MII, and the internal flag, receiving, used by the Carrier Sense and Transmit processes.

Upon receiving proper code-groups via rx_code_bits from the link partner as described in 24.2.2.1.6, the Receive process may support the LPI function by deactivating all or part of receive functional blocks of the PCS, PMA, and PMD to conserve energy during the low link utilization period, and generate commands through the MII as described in 22.2.2.8. By interacting with the Link Monitor of the PMA, a link failure detection mechanism is included to differentiate two conditions of link failure due to signal off: the loss of channel signal during the normal operation and the loss of refresh signal in the LPI mode.

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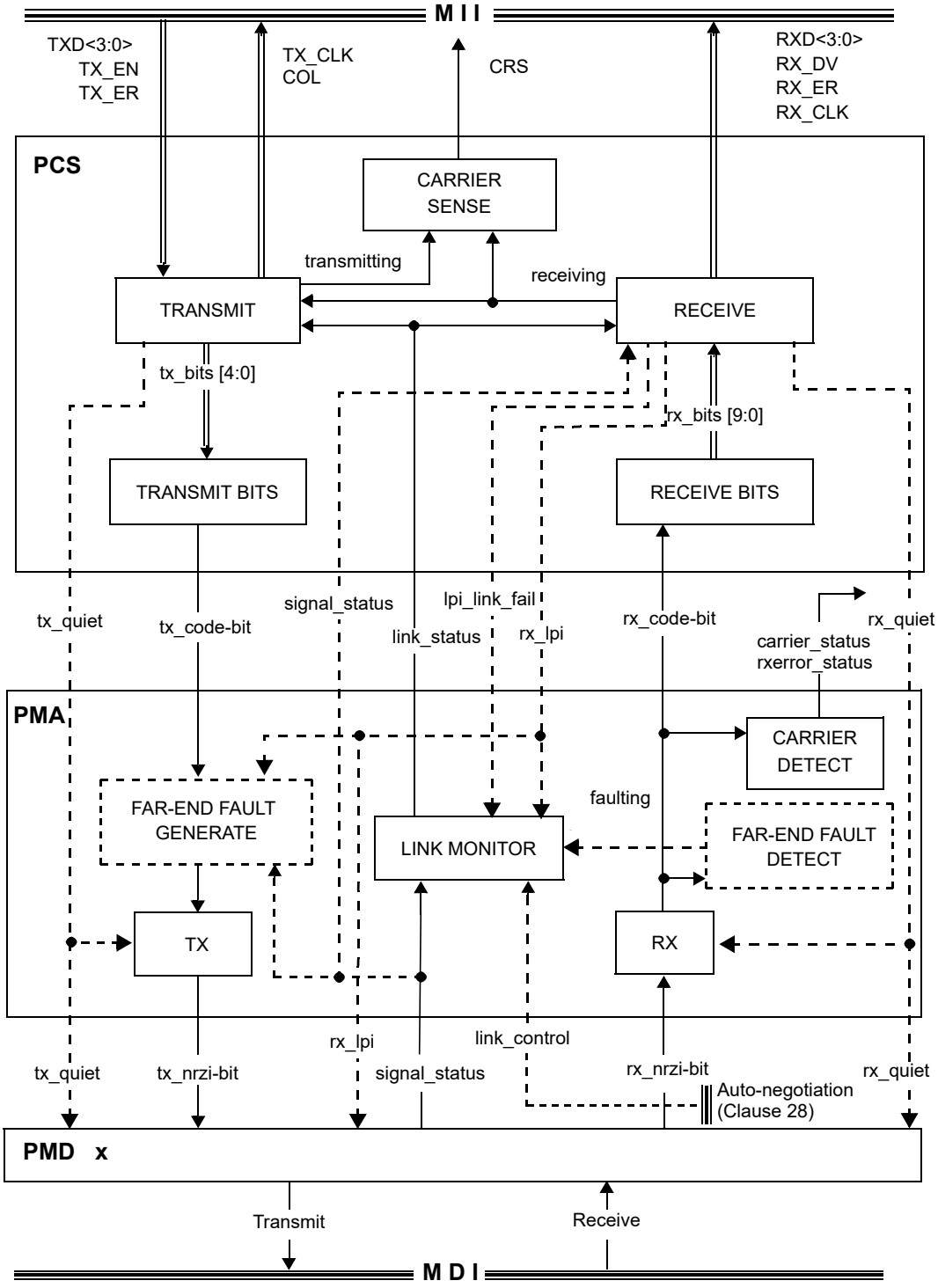

Figure 24–4—Functional block diagram

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The Transmit process generates continuous code-groups based upon the TXD<3:0>, TX_EN, and TX_ER signals on the MII. These code-groups are transmitted by Transmit Bits via the PMA_UNITDATA.request primitive. The Transmit process generates the MII signal COL based on whether a reception is occurring simultaneously with transmission. Additionally, it generates the internal flag, transmitting, for use by the Carrier Sense process.

The Transmit process may support the LPI function by deactivating all or part of the transmit functional blocks of the PCS, PMA, and PMD to conserve energy during the low link utilization period upon receiving the proper command from MII as described in 22.2.2.4. In this mode, the Transmit process is periodically activated to transmit refresh signal through tx_code_bits in order to allow the remote receiver to keep track of the long-term variation of channel characteristics and the clock drift between link partners.

The Carrier Sense process asserts the MII signal CRS when either transmitting or receiving is TRUE. Both the Transmit and Receive processes monitor link_status via the PMA_LINK.indicate primitive, to account for potential link failure conditions.

24.2.2.1 Code-groups

The PCS maps four-bit nibbles from the MII into five-bit code-groups, and vice versa, using a 4B/5B block coding scheme. A code-group is a consecutive sequence of five code-bits interpreted and mapped by the PCS. Implicit in the definition of a code-group is an establishment of code-group boundaries by an alignment function within the PCS Receive process. It is important to note that, with the sole exception of the SSD, which is used to achieve alignment, code-groups are undetectable and have no meaning outside the 100BASE-X physical protocol data unit, called a “stream.”

The coding method used, derived from ISO/IEC 9314-1, provides

a) Adequate codes (32) to provide for all Data code-groups (16) plus necessary control code-groups.
b) Appropriate coding efficiency (4 data bits per 5 code-bits; 80%) to effect a 100 Mb/s Physical Layer interface on a 125 Mb/s physical channel as provided by FDDI PMDs.
c) Sufficient transition density to facilitate clock recovery (when not scrambled).

Table 24–1 specifies the interpretation assigned to each five bit code-group, including the mapping to the nibble-wide (TXD or RXD) Data signals on the MII. The 32 code-groups are divided into four categories, as shown.

For clarity in the remainder of this clause, code-group names are shown between /slashes/. Code-group sequences are shown in succession, e.g., /1/2/....

The indicated code-group mapping is identical to ISO/IEC 9314-1:1989, with the following five exceptions:

a) The FDDI term *symbol* is avoided in order to prevent confusion with other 100BASE-T terminology. In general, the term *code-group* is used in its place.
b) The /S/ and /Q/ code-groups are not used by 100BASE-X and are interpreted as INVALID.
c) The /R/ code-group is used in 100BASE-X as the second code-group of the End-of-Stream delimiter rather than to indicate a Reset condition.
d) The /H/ code-group is used to propagate receive errors rather than to indicate the Halt Line State.
e) The /P/ code-group is used to indicate LPI.

24.2.2.1.1 Data code-groups

A Data code-group conveys one nibble of arbitrary data between the MII and the PCS. The sequence of Data code-groups is arbitrary, where any Data code-group can be followed by any other Data code-group. Data code-groups are coded and decoded but not interpreted by the PCS. Successful decoding of Data code-groups depends on proper receipt of the Start-of-Stream delimiter sequence, as defined in Table 24–1.

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Table 24–1—4B/5B code-groups

	PCS code-group [4:0] 4 3 2 1 0	Name	MII (TXD/RXD) <3:0> 3 2 1 0	Interpretation
DATA	1 1 1 1 0	0	0 0 0 0	Data 0
	0 1 0 0 1	1	0 0 0 1	Data 1
	1 0 1 0 0	2	0 0 1 0	Data 2
	1 0 1 0 1	3	0 0 1 1	Data 3
	0 1 0 1 0	4	0 1 0 0	Data 4
	0 1 0 1 1	5	0 1 0 1	Data 5
	0 1 1 1 0	6	0 1 1 0	Data 6
	0 1 1 1 1	7	0 1 1 1	Data 7
	1 0 0 1 0	8	1 0 0 0	Data 8
	1 0 0 1 1	9	1 0 0 1	Data 9
	1 0 1 1 0	A	1 0 1 0	Data A
	1 0 1 1 1	B	1 0 1 1	Data B
	1 1 0 1 0	C	1 1 0 0	Data C
	1 1 0 1 1	D	1 1 0 1	Data D
	1 1 1 0 0	E	1 1 1 0	Data E
	1 1 1 0 1	F	1 1 1 1	Data F
	1 1 1 1 1	I	undefined	IDLE; used as inter-stream fill code
	0 0 0 0 0	P	0 0 0 1	SLEEP; LPI code only for the EEE capability. Otherwise, Invalid code; refer to Table 22–1 and Table 22–2
CONTROL	1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
	1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
	0 1 1 0 1	T	undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
	0 0 1 1 1	R	undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
INVALID	0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
	0 0 0 0 0	V	Undefined	Invalid code
	0 0 0 0 1	V	Undefined	Invalid code
	0 0 0 1 0	V	Undefined	Invalid code
	0 0 0 1 1	V	Undefined	Invalid code
	0 0 1 0 1	V	Undefined	Invalid code
	0 0 1 1 0	V	Undefined	Invalid code
	0 1 0 0 0	V	Undefined	Invalid code
	0 1 1 0 0	V	Undefined	Invalid code
	1 0 0 0 0	V	Undefined	Invalid code
	1 1 0 0 1	V	Undefined	Invalid code

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24.2.2.1.2 Idle code-groups

The Idle code-group (/I/) is transferred between streams. It provides a continuous fill pattern to establish and maintain clock synchronization. Idle code-groups are emitted from, and interpreted by, the PCS.

24.2.2.1.3 Control code-groups

The Control code-groups are used in pairs (/J/K/, /T/R/) to delimit MAC packets. Control code-groups are emitted from, and interpreted by, the PCS.

24.2.2.1.4 Start-of-Stream delimiter (/J/K/)

A Start-of-Stream delimiter (SSD) is used to delineate the boundary of a data transmission sequence and to authenticate carrier events. The SSD is unique in that it may be recognized independently of previously established code-group boundaries. The Receive function within the PCS uses the SSD to establish code-group boundaries. A SSD consists of the sequence /J/K/.

On transmission, the first 8 bits of the MAC preamble are replaced by the SSD, a replacement that is reversed on reception.

24.2.2.1.5 End-of-Stream delimiter (/T/R/)

An End-of-Stream delimiter (ESD) terminates all normal data transmissions. Unlike the SSD, an ESD cannot be recognized independent of previously established code-group boundaries. An ESD consists of the sequence /T/R/.

24.2.2.1.6 SLEEP code-groups (/P/)

The SLEEP code-group (/P/) is used to delineate the boundary of an LPI sequence and to deliver a refresh signal to maintain clock synchronization and verify the link status. The SLEEP code-groups are emitted from, and interpreted by, the PCS.

24.2.2.1.7 Invalid code-groups

The /H/ code-group indicates that the PCS's client wishes to indicate a Transmit Error to its peer entity. The normal use of this indicator is for repeaters to propagate received errors. Transmit Error code-groups are emitted from the PCS, at the request of the PCS's client through the use of the TX_ER signal, as described in 24.2.4.2.

The presence of any invalid code-group on the medium, including /H/, denotes a collision artifact or an error condition. Invalid code-groups are not intentionally transmitted onto the medium by DTE's. The PCS indicates the reception of an Invalid code-group on the MII through the use of the RX_ER signal, as described in 24.2.4.4.

24.2.2.2 Encapsulation

The 100BASE-X PCS accepts frames from the MAC through the Reconciliation sublayer and MII. Due to the continuously signaled nature of the underlying PMA, and the encoding performed by the PCS, the 100BASE-X PCS encapsulates the MAC frame (100BASE-X Service Data Unit, SDU) into a Physical Layer stream (100BASE-X Protocol Data Unit, PDU).

Except for the two code-group SSD, data nibbles within the SDU (including the non-SSD portions of the MAC preamble and SFD) are not interpreted by the 100BASE-X PHY. The conversion from a MAC frame to a Physical Layer stream and back to a MAC frame is transparent to the MAC.

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Figure 24–5 depicts the mapping between MAC frames and Physical Layer streams.

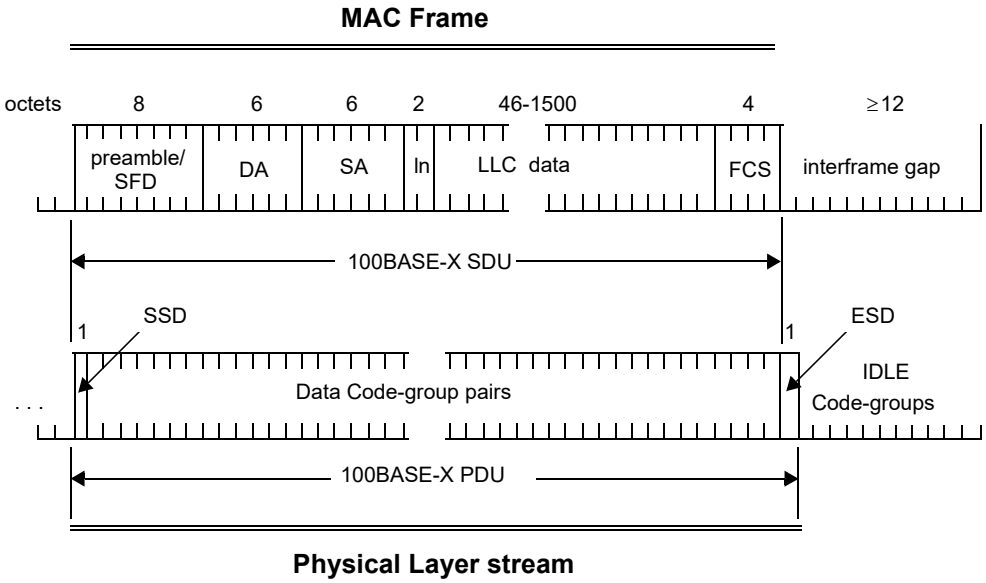

Figure 24–5—PCS encapsulation

A properly formed stream can be viewed as comprising the following three elements:

a) *Start-of-Stream Delimiter.* The start of a Physical Layer stream is indicated by a SSD, as defined in 24.2.2.1. The SSD replaces the first octet of the preamble from the MAC frame and vice versa.
b) *Data Code-groups.* Between delimiters (SSD and ESD), the PCS conveys Data code-groups corresponding to the data nibbles of the MII. These Data code-groups comprise the 100BASE-X Service Data Unit (SDU). Data nibbles within the SDU (including those corresponding to the MAC preamble and SFD) are not interpreted by the 100BASE-X PCS.
c) *End-of-Stream Delimiter.* The end of a properly formed stream is indicated by an ESD, as defined in 24.2.2.1. The ESD is transmitted by the PCS following the deassertion of TX_EN on the MII, which corresponds to the last data nibble composing the FCS from the MAC. It is transmitted during the period considered by the MAC to be the interframe gap (IFG). On reception, ESD is interpreted by the PCS as terminating the SDU.

Between streams, IDLE code-groups are conveyed between the PCS and PMA.

24.2.2.3 Data delay

The PCS maps a non-aligned code-bit data path from the PMA to an aligned, nibble-wide data path on the MII, both for Transmit and Receive. Logically, received bits have to be buffered to facilitate SSD detection and alignment, coding translation, and ESD detection. These functions necessitate an internal PCS delay of at least two code-groups. In practice, alignment may necessitate even longer delays of the incoming code-bit stream.

When the MII is present as an exposed interface, the MII signals TX_CLK and RX_CLK, not depicted in the following state diagrams, shall be generated by the PCS in accordance with Clause 22.

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24.2.2.4 Mapping between MII and PMA

Figure 24–6 depicts the mapping of the nibble-wide data path of the MII to the five-bit-wide code-groups (internal to the PCS) and the code-bit path of the PMA interface.

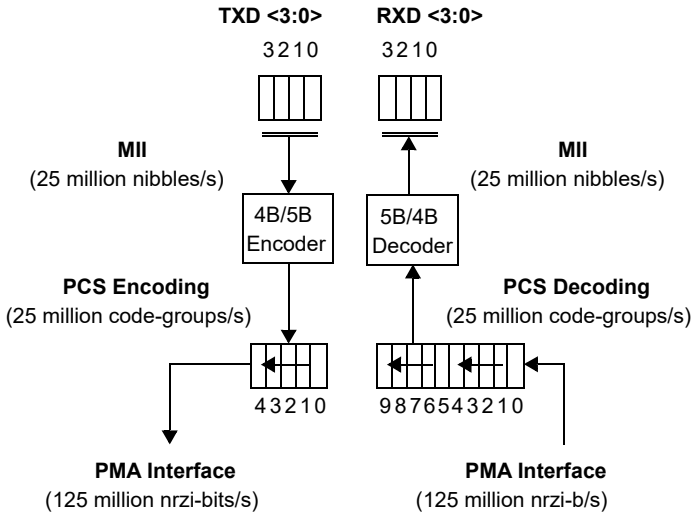

Figure 24–6—PCS reference diagram

Upon receipt of a nibble from the MII, the PCS encodes it into a five-bit code-group, according to 24.2.2.1. Code-groups are serialized into code-bits and passed to the PMA for transmission on the underlying medium, according to Figure 24–6. The first transmitted code-bit of a code-group is bit 4, and the last code-bit transmitted is bit 0. There is no numerical significance ascribed to the bits within a code-group; that is, the code-group is simply a five-bit pattern that has some predefined interpretation.

Similarly, the PCS deserializes code-bits received from the PMA, according to Figure 24–6. After alignment is achieved, based on SSD detection, the PCS converts code-groups into MII data nibbles, according to 24.2.2.1.

24.2.3 State variables

24.2.3.1 Constants

DATA

The set of 16 code-groups corresponding to valid DATA, as specified in 24.2.2.1. (In the Receive state diagram, the set operators $\in$ and $\notin$ are used to represent set membership and non-membership, respectively.)

ESD

The code-group pair corresponding to the End-of-Stream delimiter, as specified in 24.2.2.1.

ESD1

The code-group pair corresponding to the End-of-Stream delimiter, Part 1 (/T/), as specified in 24.2.2.1.

ESD2

The code-group pair corresponding to the End-of-Stream delimiter, Part 2 (/R/), as specified in

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24.2.2.1.

HALT
: The Transmit Error code-group (/H/), as specified in 24.2.2.1.

IDLE
: The IDLE code-group, as specified in 24.2.2.1.

IDLES
: A code-group pair composed of /I/I/; /I/ as specified in 24.2.2.1.

SSD
: The code-group pair corresponding to the Start-of-Stream delimiter, as specified in 24.2.2.1.

SSD1
: The code-group corresponding to the Start-of-Stream delimiter, Part 1 (/J/), as specified in 24.2.2.1.

SSD2
: The code-group corresponding to the Start-of-Stream delimiter, Part 2 (/K/), as specified in 24.2.2.1.

The following constants are required only for the optional EEE capability:

SLEEP
: The SLEEP code-group (/P/) used by the LPI state delineator, as specified in 24.2.2.1.

TX_LP_IDLE
: A binary value 0001 of transmit nibble-wide Data signals (TXD), together with the deassertion of TX_EN and the assertion of TX_ER on the MII, used to indicate “Assert LPI”, as specified in 22.2.2.

RX_LP_IDLE
: A binary value 0001 of receive nibble-wide Data signals (RXD), together with the deassertion of RX_DV and the assertion of RX_ER on the MII, used to indicate “Assert LPI”, as specified in 22.2.2.

24.2.3.2 Variables

In the following, values for the MII parameters are definitively specified in Clause 22.

COL
: The COL signal of the MII as specified in Clause 22.

CRS
: The CRS signal of the MII as specified in Clause 22.

link_status
: The link_status parameter as communicated by the PMA_LINK.indicate primitive.

  Values: FAIL; the receive channel is not intact
  READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
  OK; the receive channel is intact and enabled for reception

receiving
: A Boolean set by the Receive process to indicate non-IDLE activity (after squelch). Used by the Carrier Sense process, and also interpreted by the Transmit process for indicating a collision.

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Values: TRUE; unsquelched carrier being received
FALSE; carrier not being received

rx_bits [9:0]

A vector of the 10 most recently received code-bits from the PMA as assembled by Receive Bits and processed by Receive. rx_bits [0] is the most recently received (newest) code-bit; rx_bits [9] is the least recently received code-bit (oldest). When alignment has been achieved, it contains the last two code-groups.

rx_code-bit

The rx_code-bit parameter as communicated by the most recent PMA_UNITDATA.indicate primitive (that is, the value of the most recently received code-bit from the PMA).

RX_DV

The RX_DV signal of the MII as specified in Clause 22. Set by the Receive process, RX_DV is also interpreted by the Receive Bits process as an indication that rx_bits is code-group aligned.

RX_ER

The RX_ER signal of the MII as specified in Clause 22.

RXD <3:0>

The RXD <3:0> signal of the MII as specified in Clause 22.

transmitting

A Boolean set by the Transmit Process to indicate a transmission in progress. Used by the Carrier Sense process.

Values: TRUE; the PCS's client is transmitting
FALSE; the PCS's client is not transmitting

tx_bits [4:0]

A vector of code-bits representing a code-group prepared for transmission by the Transmit Process and transmitted to the PMA by the Transmit Bits process.

TX_EN

The TX_EN signal of the MII as specified in Clause 22.

TX_ER

The TX_ER signal of the MII as specified in Clause 22.

TXD <3:0>

The TXD <3:0> signal of the MII as specified in Clause 22.

The following variables are required only for the optional EEE capability:

lpi_link_fail

A Boolean set by the Receive process to control the transition to a Link Down state when in the LPI mode. Used by the Link Monitor process of the PMA as communicated through the PMA_LPILINKFAIL.request primitive.

Values: TRUE; local receiver has detected a link failure status when in the LPI mode
FALSE; local receiver is functioning normally when in the LPI mode

rx_lpi

A Boolean set by the Receive process to indicate the LPI mode. Used by the Link Monitor process of the PMA as communicated through the PMA_RXLPI.request primitive. This parameter is used to alter the signal detection time as shown in Table 25–3. It can also be used to halt the clock RXC of MII as described in Clause 22.

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Values: TRUE; local receiver is in the LPI mode
FALSE; local receiver is in the normal mode

rx_quiet

A Boolean set by the Receive process to indicate a Quiet state of the receiver in the LPI mode as communicated through the PMD_RXQUIET.request primitive. Also may be used to control the power-saving function of various receive blocks (PCS, PMA, and PMD).

Values: TRUE; the local receiver is in the Quiet state
FALSE; the local receiver is not in the Quiet state

tx_quiet

A Boolean set by the Transmit process to indicate a Quiet state of the transmitter in the LPI mode as communicated through the PMD_TXQUIET.request primitive. Also may be used to control the power-saving function of various transmit blocks (PCS, PMA, and PMD).

Values: TRUE; the local transmitter is in the Quiet state
FALSE; the local transmitter is not in the Quiet state

signal_status

The signal_status parameter as communicated by the PMD_SIGNAL.indicate primitive.

Values: ON; the quality and level of the received signal is satisfactory
OFF; the quality and level of the received signal is not satisfactory

24.2.3.3 Functions

nibble DECODE (code-group)

In Receive, this function takes as its argument a five-bit code-group and returns the corresponding MII RXD <3:0> nibble, per Table 24–1.

code-group ENCODE (nibble)

In the Transmit process, this function takes as its argument an MII TXD <3:0> nibble, and returns the corresponding five-bit code-group per Table 24–1.

SHIFTLEFT (rx_bits)

In Receive Bits, this function shifts rx_bits left one bit placing rx_bits [8] in rx_bits [9], rx_bits [7] in rx_bits [8] and so on until rx_bits [1] gets rx_bits [0].

24.2.3.4 Timers

code-bit_timer

In the Transmit Bits process, the timer governing the output of code-bits from the PCS to the PMA and thereby to the medium with a nominal 8 ns period. This timer shall be derived from a fixed frequency oscillator with a base frequency of 125 MHz ± 0.005% and phase jitter above 20 kHz less than ± 8°.

The following timers are required only for the optional EEE capability:

lpi_link_fail_timer

In the LPI mode, the receiver in Wake state is checking if valid symbols are properly received. This timer defines the maximum time allowed for the PHY between entry into the Wake state and subsequent entry into the Quiet, Sleep, or Idle states before assuming a link failure. The timer shall have a period between 90 μs and 110 μs.

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lpi_rx_ti_timer

In the LPI mode, the receiver can move to the Idle state when it receives consecutive IDLE symbols. In order to distinguish the intended IDLE symbols sent by the link partner from ones falsely decoded during the transition from the Sleep state to the Quiet state before the signal status is deasserted, this receiver timer counts the minimum duration of received IDLE symbols. During this period of time, the receiver stays in an intermediate state. The timer shall have a period between 0.8 μs and 0.9 μs.

lpi_rx_tq_timer

In the LPI mode, this receiver timer counts the maximum duration the PHY stays in the Quiet state before it expects a Refresh signal. If the PHY fails to receive a valid Refresh signal or Wake signal before this timer expires, the receiver shall assume a link failure. The timer shall have a period between 24 ms and 26 ms.

lpi_rx_ts_timer

In the LPI mode, this receiver timer counts the maximum duration the PHY is allowed to stay in the Sleep state before assuming a link failure. The timer shall have a period between 240 μs and 260 μs.

lpi_rx_tw_timer

In the LPI mode, the receiver in the Quiet state is woken up by the receiving signal. This receiver timer counts the expected duration for the PHY to identify if valid SLEEP symbols for the Refresh state or valid IDLES for the Wake state have been properly received. If none of the SLEEP or IDLE symbols are received when the timer expires, the wake error counter as defined in MDIO manageable device (MMD) register 3.22 (see 45.2.3.12) shall be incremented. The timer shall have a period that does not exceed 20.5 μs.

lpi_tx_tq_timer

In the LPI mode, this transmitter timer counts the duration the PHY remains in the Quiet state before it has to wake to send a refresh signal. The timer shall have a period between 20 ms and 22 ms.

lpi_tx_ts_timer

In the LPI mode, this transmitter timer counts the duration the PHY is sending continuous SLEEP symbols in the Sleep state before going into the Quiet state. The timer shall have a period between 200 μs and 220 μs.

24.2.3.5 Messages

gotCodeGroup.indicate

A signal sent to the Receive process by the Receive Bits process after alignment has been achieved signifying completion of reception of the next code-group in rx_bits(4:0), with the preceding code-group moved to rx_bits [9:5]. rx_bits [9:5] may be considered as the “current” code-group.

PMA_UNITDATA.indicate (rx_code-bit)

A signal sent by the PMA signifying that the next code-bit from the medium is available in rx_code-bit.

sentCodeGroup.indicate

A signal sent to the Transmit process from the Transmit Bits process signifying the completion of transmission of the code-group in tx_bits [4:0].

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24.2.4 State diagrams

24.2.4.1 Transmit Bits

Transmit Bits is responsible for taking code-groups prepared by the Transmit process and transmitting them to the PMA using PMA_UNITDATA.request, the frequency of which determines the transmit clock. Transmit deposits these code-groups in tx_bits with Transmit Bits signaling completion of a code-group transmission with sentCodeGroup.indicate.

The PCS shall implement the Transmit Bits process as depicted in Figure 24–7 including compliance with the associated state variables as specified in 24.2.3.

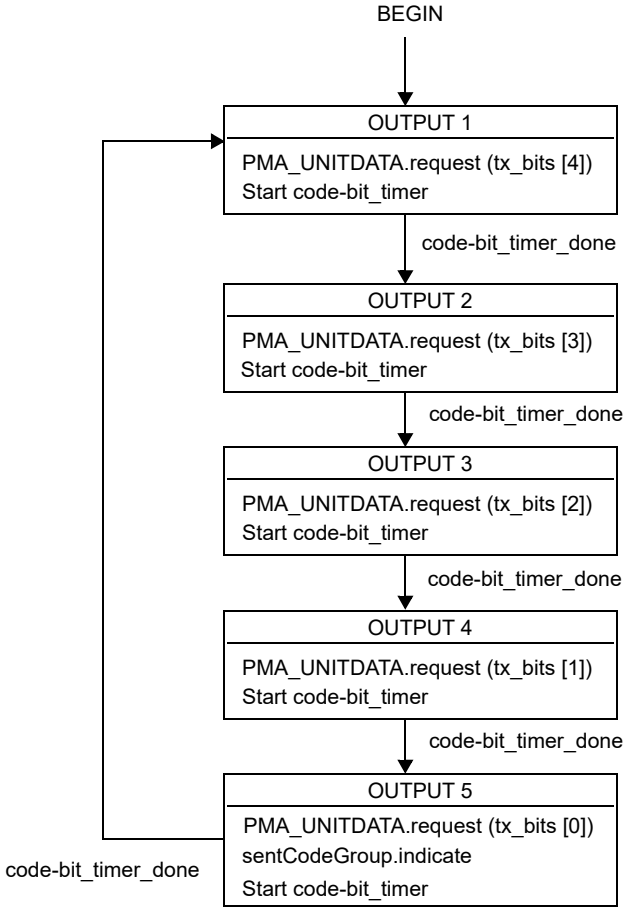

Figure 24–7—Transmit Bits state diagram

24.2.4.2 Transmit

The Transmit process sends code-groups to the PMA via tx_bits and the Transmit Bits process. When initially invoked, and between streams (delimited by TX_EN on the MII), except in the LPI mode for the optional EEE capability, the Transmit process sources continuous Idle code-groups (/I/) to the PMA. Upon the assertion of TX_EN by the MII, the Transmit process passes an SSD (/J/K/) to the PMA, ignoring the TXD<3:0> nibbles during these two code-group times. Following the SSD, each TXD<3:0> nibble is encoded into a five-bit code-group until TX_EN is deasserted. If, while TX_EN is asserted, the TX_ER signal is asserted, the Transmit process passes Transmit Error code-groups (/H/) to the PMA. Following the deassertion of TX_EN, an ESD (/T/R/) is generated, after which the transmission of Idle code-groups is resumed by the IDLE state.

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If EEE Capability is supported, upon the assertion of LPI on the MII (a binary value 0001 of TXD, together with the deassertion of TX_EN and the assertion of TX_ER, see 22.2.2), the Transmit process enters the LPI mode and starts to source SLEEP (/P/) code-groups to the PMA. In the LPI mode, the Transmit process is controlled by timers to switch between the TX_SLEEP and TX_QUIET states. The Transmit process returns to the IDLE state whenever the MII deasserts LPI.

Collision detection is implemented by noting the occurrence of carrier receptions during transmissions, following the model of 10BASE-T.

The indication of link_status ≠ OK by the PMA at any time causes an immediate transition to the IDLE state and supersedes any other Transmit process operations.

The PCS shall implement the Transmit process as depicted in Figure 24–8 including compliance with the associated state variables as specified in 24.2.3.

24.2.4.3 Receive Bits

The Receive Bits process collects code-bits from the PMA interface passing them to the Receive process via rx_bits. rx_bits [9:0] represents a sliding, 10-bit window on the PMA code-bits, with newly received code-bits from the PMA (rx_code-bit) being shifted into rx_bits [0]. This is depicted in Figure 24–9. Bits are collected serially until Receive indicates alignment by asserting RX_DV, after which Receive Bits signals Receive for every five code-bits accumulated. Serial processing resumes with the deassertion of RX_DV.

The PCS shall implement the Receive Bits process as depicted in Figure 24–10 including compliance with the associated state variables as specified in 24.2.3.

24.2.4.4 Receive

The Receive process state diagram can be viewed as comprising two sections: prealigned and aligned. In the prealigned states, IDLE, CARRIER DETECT, and IDENTIFY JK, except for the detection of SLEEP code-groups when supporting the optional EEE capability, the Receive process is waiting for an indication of channel activity followed by an SSD. After successful alignment, the incoming code-groups are decoded while waiting for stream termination.

If EEE Capability is supported, when the Receive process successfully aligns and decodes two consecutive SLEEP (/P/) code-groups, it enters the LPI mode and stays in LPI states until either the IDLE code-groups are received, where it leads the Receive process to the IDLE state, or a link failure condition in the LPI mode occurs, where it causes the Receive process to enter the RX_LPI_LINK_FAIL state and eventually move to the IDLE state.

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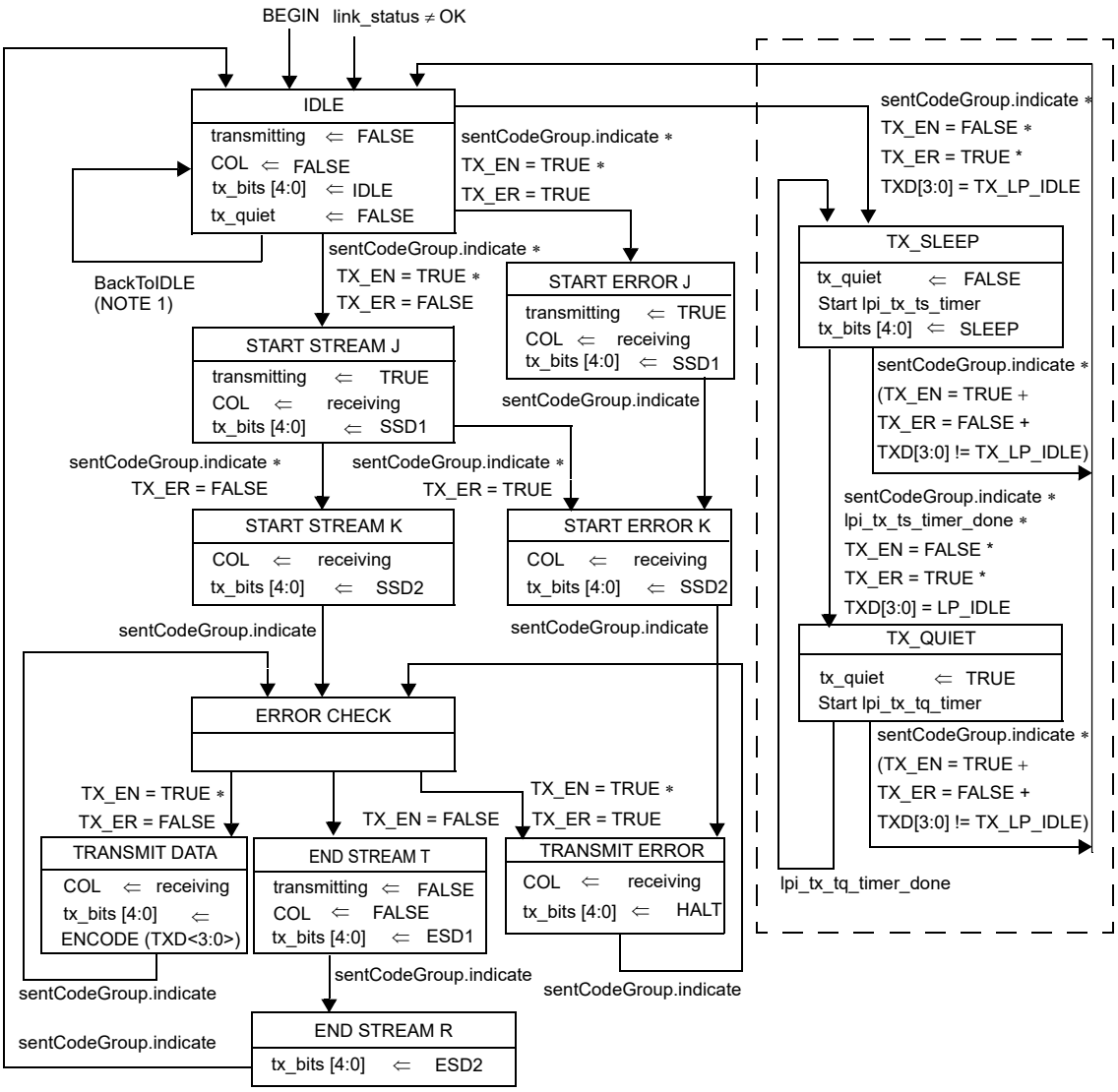

NOTE 1—BackToIDLE represents the following branch condition:

If the EEE capability is supported,
sentCodeGroup.indicate * TX_EN = FALSE * (TX_E R= FALSE + (TX_ER = TRUE * TXD[3:0] ≠ TX_LP_IDLE))
Otherwise,
sentCodeGroup.indicate * TX_EN = FALSE

NOTE 2—States and state transitions shown within the dashed box are only required for the EEE capability

Figure 24–8—Transmit state diagram

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24.2.4.4.1 Detecting channel activity

In a DTE operating in half duplex mode, the detection of activity on the underlying channel is used both by the MAC (via the MII CRS signal and the Reconciliation sublayer) for deferral purposes, and by the Transmit process for collision detection. Activity, signaled by the assertion of receiving, is indicated by the receipt of two non-contiguous ZEROS within any 10 code-bits of the incoming code-bit stream.

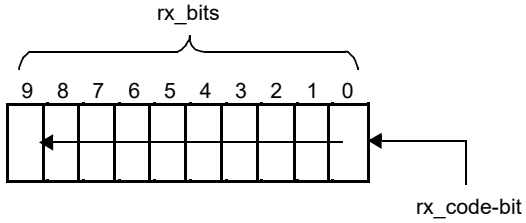

Figure 24–9—Receive Bits reference diagram

24.2.4.4.2 Code-group alignment

After channel activity is detected, the Receive process first aligns the incoming code-bits on code-group boundaries for subsequent data decoding. This is achieved by scanning the rx_bits vector for a SSD (/J/K/). The MII RX_DV signal remains deasserted during this time, which ensures that the Reconciliation sublayer will ignore any signals on RXD <3:0>. Detection of the SSD causes the Receive process to enter the START OF STREAM J state.

Well-formed streams contain SSD (/J/K/) in place of the first eight preamble bits. In the event that something else is sensed immediately following detection of carrier, a False Carrier Indication is signaled to the MII by asserting RX_ER and setting RXD to 1110 while RX_DV remains deasserted. The associated carrier event, as terminated by 10 ONEs, is otherwise ignored.

24.2.4.4.3 Stream decoding

The Receive process substitutes a sequence of alternating ONE and ZERO data-bits for the SSD, which is consistent with the preamble pattern expected by the MAC.

The Receive process then performs the DECODE function on the incoming code-groups, passing decoded data to the MII, including those corresponding to the remainder of the MAC preamble and SFD. The MII signal RX_ER is asserted upon decoding any code-group following the SSD that is neither a valid Data code-group nor a valid stream termination sequence.

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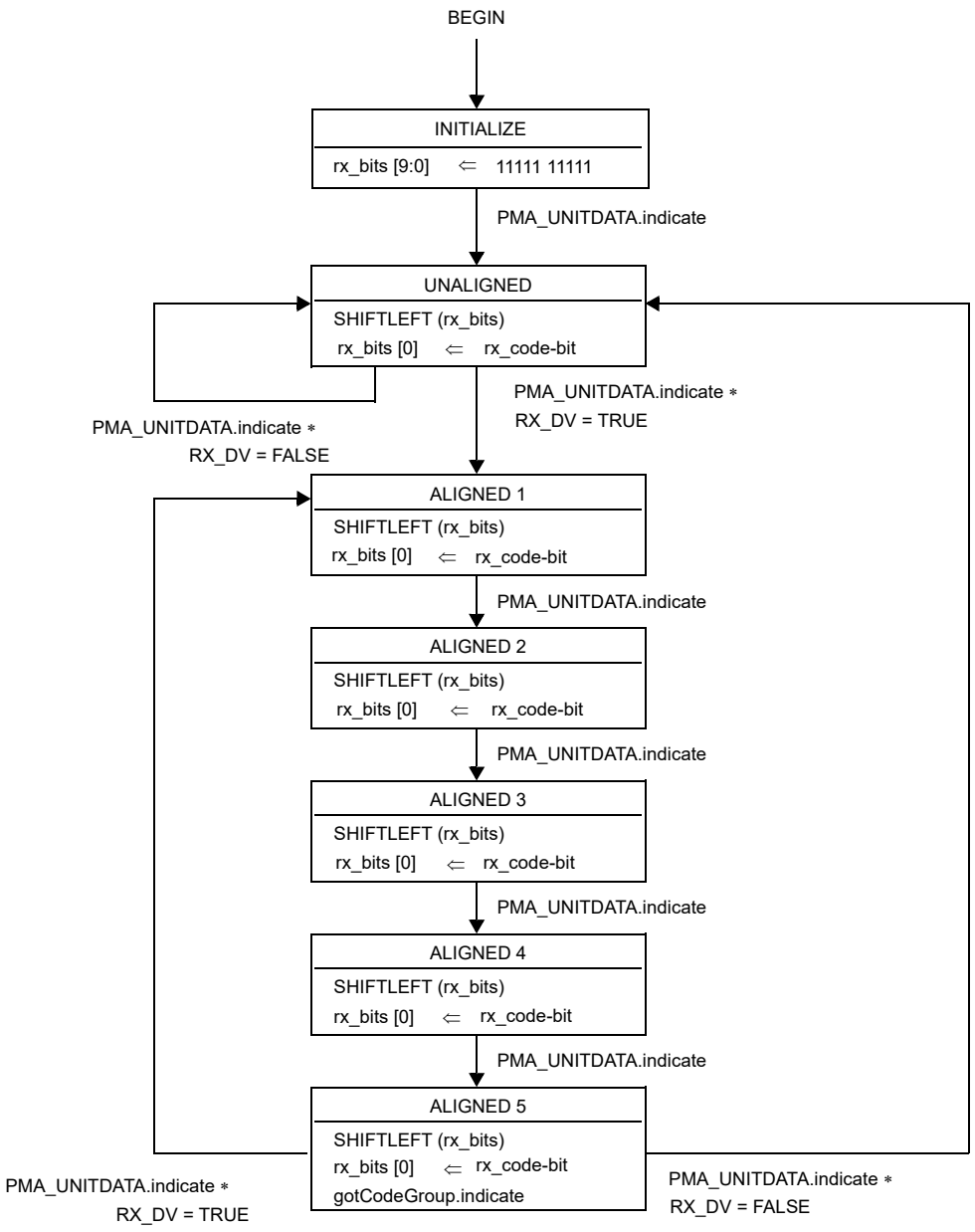

Figure 24–10—Receive Bits state diagram

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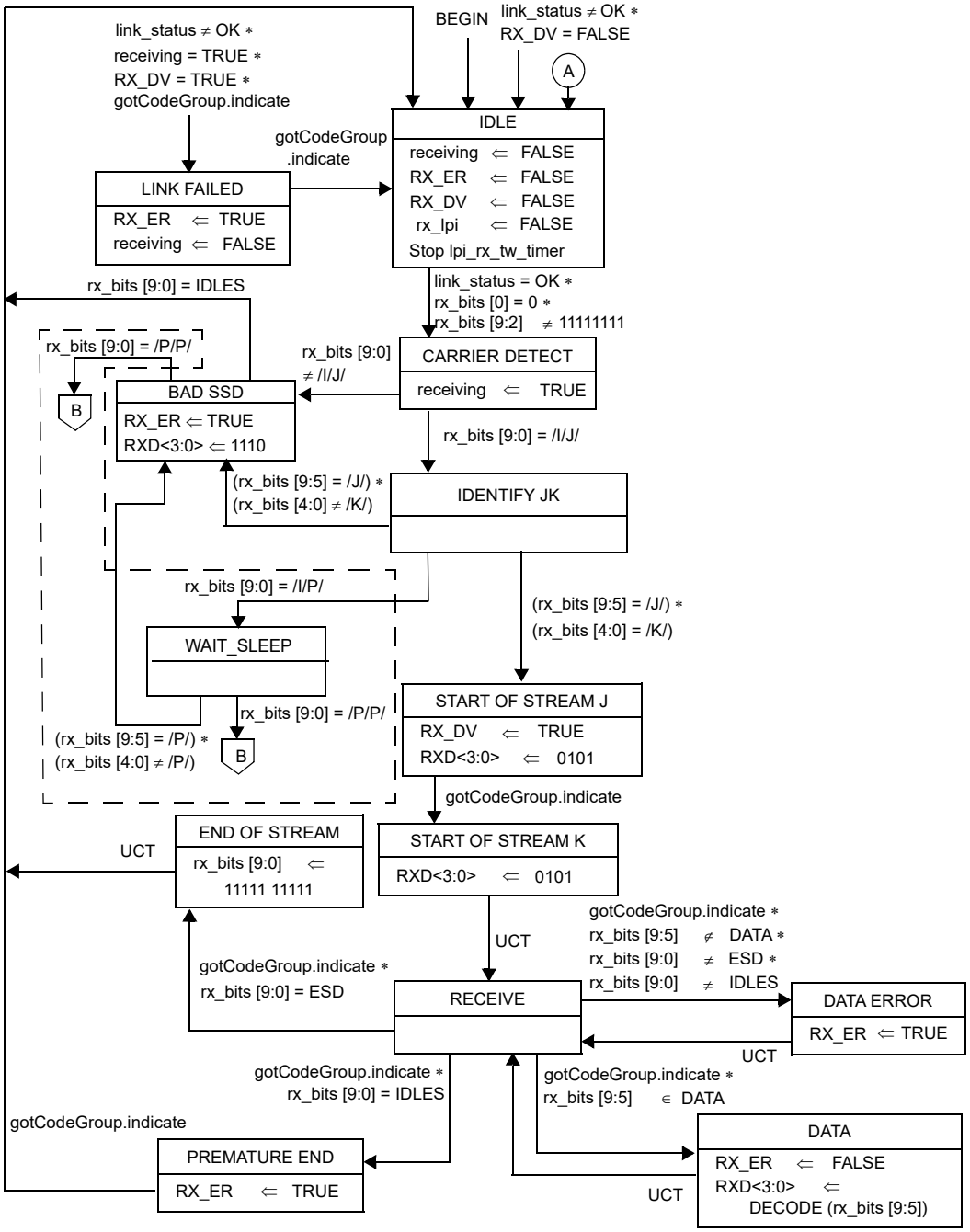
24.2.4.4.4 Stream termination

There are two means of effecting stream termination in the Receive process (Figure 24–11 and Figure 24–12) .



NOTE—States and state transitions shown within the dashed box are only required for the EEE capability

Figure 24–11—Receive state diagram, part a

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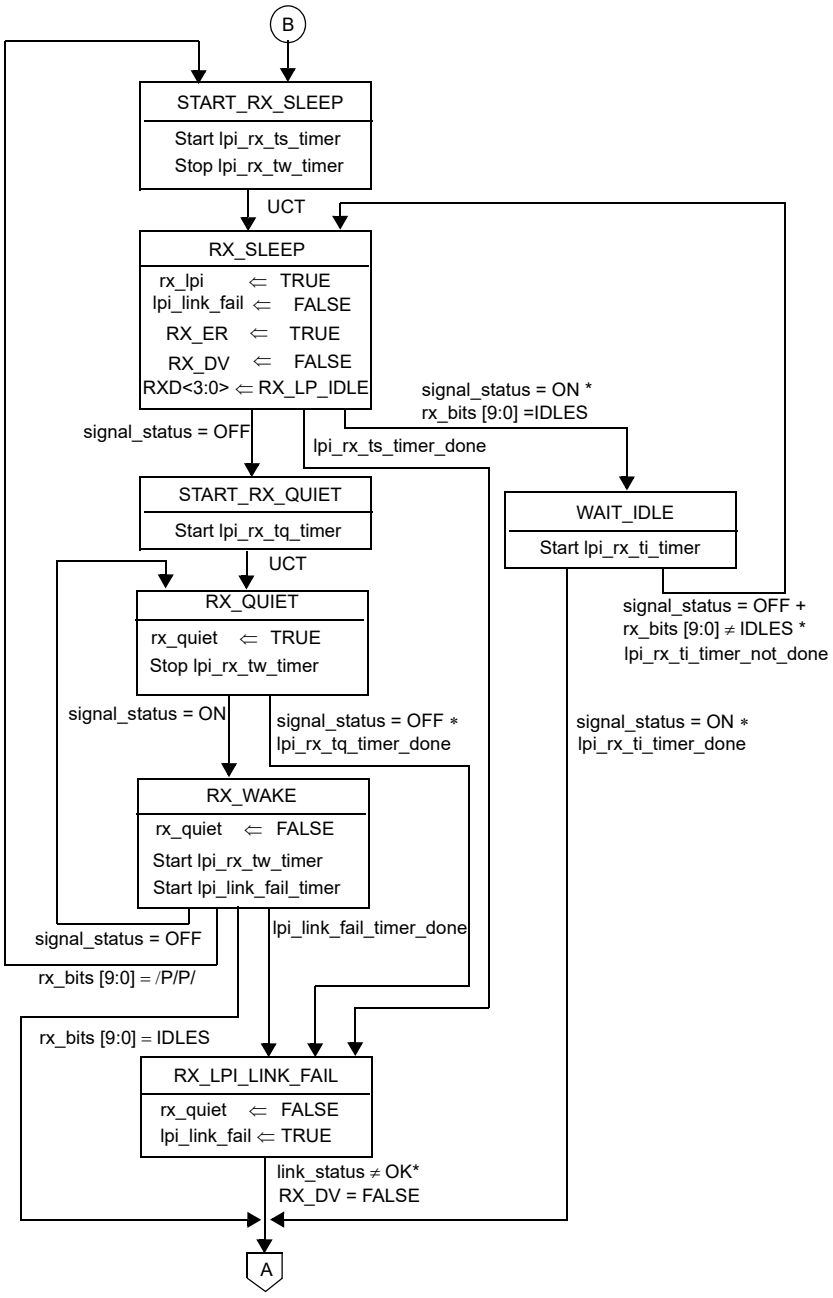

Figure 24–12—Receive state diagram, part b (only required for the EEE capability)

A normal stream termination is caused by detection of an ESD (/T/R/) in the rx_bits vector. In order to preserve the ability of the MAC to properly delimit the FCS at the end of the frame (that is, to avoid incorrect AlignmentErrors in the MAC) the internal signal receiving (and through it, the MII CRS signal, per Clause 22) is deasserted immediately following the last code-bit in the stream that maps to the FCS. Note that the condition link_status ≠ OK during stream reception (that is, when receiving = TRUE) causes an immediate transition to the LINK FAILED state and supersedes any other Receive process operations.

A premature stream termination is caused by the detection of two Idle code-groups (/I/I) in the rx_bits vector prior to an ESD. Note that RX_DV remains asserted during the nibble corresponding to the first five

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contiguous ONEs while RX_ER is signaled on the MII. RX_ER is also asserted in the LINK FAILED state, which ensures that RX_ER remains asserted for sufficient time to be detected.

Stream termination causes a transition to the IDLE state.

The PCS shall implement the Receive process as depicted in Figure 24–11 and Figure 24–12 including compliance with the associated state variables as specified in 24.2.3.

24.2.4.5 Carrier Sense

The Carrier Sense process generates the signal CRS on the MII, which (via the Reconciliation sublayer) a MAC operating in half duplex mode uses for deferral. The process operates by performing a logical OR operation on the internal messages receiving and transmitting, generated by the Receive and Transmit processes, respectively.

The PCS shall implement the Carrier Sense process as depicted in Figure 24–13 including compliance with the associated state variables as specified in 24.2.3.

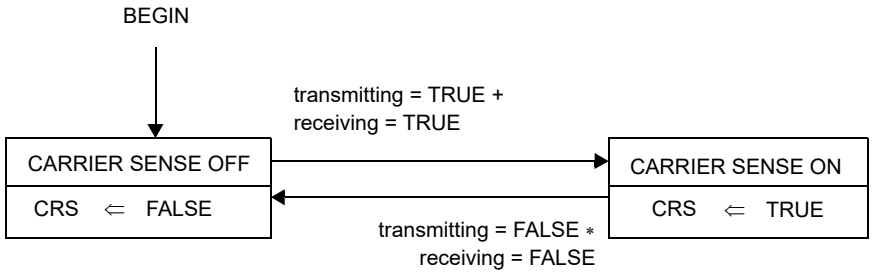

Figure 24–13—Carrier Sense state diagram

24.3 Physical Medium Attachment (PMA) sublayer

24.3.1 Service interface

The following specifies the service interface provided by the PMA to the PCS or another client, such as a repeater. These services are described in an abstract manner and do not imply any particular implementation.

The PMA Service Interface supports the exchange of code-bits between the PCS and/or Repeater entities. The PMA converts code-bits into NRZI format and passes these to the PMD, and vice versa. It also generates additional status indications for use by its client.

The following primitives are defined:

PMA_TYPE.indicate

PMA_UNITDATA.request

PMA_UNITDATA.indicate

PMA_CARRIER.indicate

PMA_LINK.indicate

PMA_LINK.request

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PMA_RXERROR.indicate

PMA_LPILINKFAIL.request

PMA_RXLPI.request

24.3.1.1 PMA_TYPE.indicate

This primitive is generated by the PMA to indicate the nature of the PMA instantiation. The purpose of this primitive is to allow clients to support connections to the various types of 100BASE-T PMA entities in a generalized manner.

24.3.1.1.1 Semantics of the service primitive

PMA_TYPE.indicate (pma_type)

The pma_type parameter for use with a 100BASE-X PMA is “X”.

24.3.1.1.2 When generated

The PMA continuously generates this primitive to indicate the value of pma_type.

24.3.1.1.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.2 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of code-bits) from the PMA’s client to the PMA.

24.3.1.2.1 Semantics of the service primitive

PMA_UNITDATA.request (tx_code-bit)

This primitive defines the transfer of data (in the form of code-bits) from the PCS or other client to the PMA. The tx_code-bit parameter can take one of two values: ONE or ZERO.

24.3.1.2.2 When generated

The PCS or other client continuously sends, at a nominal 125 Mb/s rate, the appropriate code-bit for transmission on the medium.

24.3.1.2.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a PMD_UNITDATA.request primitive, requesting transmission of the indicated code-bit, in NRZI format (tx_nrzi-bit), on the MDI.

24.3.1.3 PMA_UNITDATA.indicate

This primitive defines the transfer of data (in the form of code-bits) from the PMA to the PCS or other client.

24.3.1.3.1 Semantics of the service primitive

PMA_UNITDATA.indicate (rx_code-bit)

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The data conveyed by PMA_UNITDATA.indicate is a continuous code-bit sequence at a nominal 125 Mb/s rate. The rx_code-bit parameter can take one of two values: ONE or ZERO.

24.3.1.3.2 When generated

The PMA continuously sends code-bits to the PCS or other client corresponding to the PMD_UNITDATA.indicate primitives received from the PMD.

24.3.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.4 PMA_CARRIER.indicate

This primitive is generated by the PMA to indicate that a non-squelched, non-IDLE code-bit sequence is being received from the PMD. The purpose of this primitive is to give clients the earliest reliable indication of activity on the underlying continuous-signaling channel.

24.3.1.4.1 Semantics of the service primitive

PMA_CARRIER.indicate (carrier_status)

The carrier_status parameter can take on one of two values, ON or OFF, indicating whether a non-squelched, non-IDLE code-bit sequence (that is, carrier) is being received (ON) or not (OFF).

24.3.1.4.2 When generated

The PMA generates this primitive to indicate a change in the value of carrier_status.

24.3.1.4.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.5 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying PMD receive link.

24.3.1.5.1 Semantics of the service primitive

PMA_LINK.indicate (link_status)

The link_status parameter can take on one of three values: READY, OK, or FAIL, indicating whether the underlying receive channel is intact and ready to be enabled by Auto-Negotiation (READY), intact and enabled (OK), or not intact (FAIL). Link_status is set to FAIL when the PMD sets signal_status to OFF; when Auto-Negotiation (optional) sets link_control to DISABLE; or when Far-End Fault Detect (optional) sets faulting to TRUE. When link_status ≠ OK, then rx_code-bit and carrier_status are undefined.

24.3.1.5.2 When generated

The PMA generates this primitive to indicate a change in the value of link_status.

24.3.1.5.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

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24.3.1.6 PMA_LINK.request

This primitive is generated by the Auto-Negotiation algorithm, when implemented, to allow it to enable and disable operation of the PMA. See Clause 28. When Auto-Negotiation is not implemented, the primitive is never invoked and the PMA behaves as if link_control = ENABLE.

24.3.1.6.1 Semantics of the service primitive

PMA_LINK.request (link_control)

The link_control parameter takes on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE. Auto-Negotiation sets link_control to SCAN_FOR_CARRIER prior to receiving any fast link pulses, permitting the PMA to sense a 100BASE-X signal. Auto-Negotiation sets link_control to DISABLE when it senses an Auto-Negotiation partner (fast link pulses) and has to temporarily disable the 100BASE-X PHY while negotiation ensues. Auto-Negotiation sets link_control to ENABLE when full control is passed to the 100BASE-X PHY.

24.3.1.6.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in Clause 28.

24.3.1.6.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in 24.3.4.4.

24.3.1.7 PMA_RXERROR.indicate

This primitive is generated by the PMA to indicate that an error has been detected during a carrier event.

24.3.1.7.1 Semantics of the service primitive

PMA_RXERROR.indicate (rxerror_status)

The rxerror_status parameter can take on one of two values: ERROR or NO_ERROR, indicating whether the received carrier event contains a detectable error (ERROR) or not (NO_ERROR). A carrier event is considered to be in error when it is not started by a Start-of-Stream Delimiter.

24.3.1.7.2 When generated

The PMA generates this primitive whenever a new, non-squelched carrier event is not started by a Start-of-Stream Delimiter.

24.3.1.7.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.8 PMA_LPILINKFAIL.request

This primitive is generated by the Receive Process of the PCS only if EEE is supported to control one of the link failure conditions of the Link Monitor in the PMA (see 24.2.4.3 and Figure 24–12).

24.3.1.8.1 Semantics of the service primitive

PMA_LPILINKFAIL.request (lpi_link_fail)

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The lpi_link_fail parameter takes on one of two values, TRUE or FALSE, indicating whether a link failure condition has been set (TRUE) or not (FALSE). The value of TRUE, when in the LPI mode, sets the link_status of the Link Monitor to FAIL (see 24.3.4.4 and Figure 24–15).

24.3.1.8.2 When generated

The PCS generates this primitive to indicate a link failure condition caused by the loss of Refresh signal when in the LPI mode.

24.3.1.8.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in 24.3.4.4.

24.3.1.9 PMA_RXLPI.request

This primitive is generated by the Receive Process of the PCS only if EEE is supported to indicate that the receiver is in the LPI mode (see 24.2.4.3 and Figure 24–12).

24.3.1.9.1 Semantics of the service primitive

PMA_RXLPI.request (rx_lpi)

The rx_lpi parameter takes on one of two values, TRUE or FALSE, indicating whether the receiver is in the LPI mode (TRUE) or not (FALSE).

24.3.1.9.2 When generated

The PCS generates this primitive to indicate the LPI mode.

24.3.1.9.3 Effect of receipt

This primitive affects the operation of the PMA Link Monitor function as described in 24.3.4.4. Other use of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.2 Functional requirements

The 100BASE-X PMA comprises the following functions:

a) Mapping of transmit and receive code-bits between the PMA Service Interface and the PMD Service Interface.
b) Link Monitor, which maps the PMD_SIGNAL.indicate primitive to the PMA_LINK.indicate primitive, indicating the availability of the underlying PMD.
c) Carrier Detection, which generates the PMA_CARRIER.indicate and PMA_RXERROR.indicate primitives from inspection of received PMD signals.
d) Far-End Fault (optional), composed of the Far-End Fault Generate and Far-End Fault Detect processes, which sense receive channel failures and send the Far-End Fault Indication, and sense the Far-End Fault Indication.
e) EEE capability, which disables the Far-End Fault function and modifies the link down condition with the PMA_RXLPI.request primitive.

Figure 24–4 includes a functional block diagram of the PMA.

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24.3.2.1 Far-End fault

Auto-Negotiation provides a Remote Fault capability useful for detection of asymmetric link failures; i.e., channel error conditions detected by the far-end station but not the near-end station. Since Auto-Negotiation is specified only for media supporting eight-pin modular connectors, such as used by 100BASE-TX over twisted pair, Auto-Negotiation's Remote Fault capability is unavailable to other media for which it may be functionally beneficial, such as 100BASE-TX over shielded twisted pair or 100BASE-FX. A remote fault capability for 100BASE-FX is particularly useful due to this medium's applicability over longer distances (making end-station checking inconvenient) and for backbones (in which detection of link failures can trigger redundant systems).

For these reasons, 100BASE-X provides an optional Far-End Fault facility when Auto-Negotiation cannot be used. Far-End Fault shall not be implemented for media capable of supporting Auto-Negotiation.

When no signal is being received, as indicated by the PMD's signal detect function, the Far-End Fault feature permits the station to transmit a special Far-End Fault Indication to its far-end peer. The Far-End Fault Indication is sent only when a physical error condition is sensed on the receive channel. In all other situations, including reception of the Far-End Fault Indication itself, the PMA passes through tx_code-bit. (Note that the Far-End Fault architecture is such that IDLEs are automatically transmitted when the Far-End Fault Indication is detected. This is necessary to re-establish communication when the link is repaired.)

The Far-End Fault Indication is composed of three or more repeating cycles, each of 84 ONEs followed by a single ZERO. This signal is sent in-band and is readily detectable but is constructed so as to not satisfy the 100BASE-X carrier sense criterion. It is therefore transparent to the PMA's client and to stations not implementing Far-End Fault.

As shown in Figure 24–4, Far-End Fault is implemented through the Far-End Fault Generate, Far-End Fault Detect, and the Link Monitor processes.

The Far-End Fault Generate process, which is interposed between the incoming tx_code-bit stream and the TX process, is responsible for sensing a receive channel failure (signal_status=OFF during the normal operation) and transmitting the Far-End Fault Indication in response. The transmission of the Far-End Fault Indication may start or stop at any time depending only on signal_status. The Far-End Fault shall not be generated when in the LPI mode.

The Far-End Fault Detect process continuously monitors rx_code-bits from the RX process for the Far-End Fault Indication. Detection of the Far-End Fault Indication disables the station by causing the Link Monitor process to deassert link_status, which in turn causes the station to source IDLEs. Far-End Fault detection can also be used by management functions not specified in this clause.

24.3.2.2 Comparison to previous IEEE 802.3 PMAs

Previous IEEE 802.3 PMAs perform the additional functions of SQE Test and Jabber. Neither of these functions is implemented in the 100BASE-X PMA.

SQE Test is provided in other Physical Layers to check the integrity of the Collision Detection mechanism independently of the Transmit and Receive capabilities of the Physical Layer. Since 100BASE-X effects collision detection by sensing receptions that occur during transmissions, collision detection is dependent on the health of the receive channel. By checking the ability to properly receive signals from the PMD, the Link Monitor function therefore functionally subsumes the functions previously implemented by SQE Test.

The Jabber function prevents a DTE from causing total network failure under certain classes of faults. When using mixing media (e.g., coaxial cables or passive optical star couplers), this function naturally has to be implemented in the DTE. 100BASE-X requires the use of an active repeater, with one DTE or repeater

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attached to each port. As an implementation optimization, the Jabber function has therefore been moved to the repeater in 100BASE-X.

24.3.2.3 EEE capability

EEE capability, when communicated by the PMA_RXLPI.request primitive, affects the PMA in two ways. It disables the operation of the Far-End Fault processes to ignore the frequent on and off activity of signal_status. It receives link failure detection as communicated by the PMA_LPILINKFAIL.request primitive and changes the Link Monitor process to allow an exit from the LPI mode to a link down state. The EEE capability of the PMA is required only if the PCS supports EEE. If LPI is implemented, the operation of the PMA shall comply with the requirements in this subclause.

24.3.3 State variables

24.3.3.1 Constants

FEF_CYCLES

The number of consecutive cycles (of FEF_ONES ONEs and a single ZERO) necessary to indicate the Far-End Fault Indication. This value is 3.

FEF_ONES

The number of consecutive ONEs to be transmitted for each cycle of the Far-End Fault Indication. This value is 84.

24.3.3.2 Variables

carrier_status

The carrier_status parameter to be communicated by the Carrier Detect process through the PMA_CARRIER.indicate primitive. Carrier is defined as receipt of two noncontiguous ZEROs in 10 code-bits.

Values: ON; carrier is being received
OFF; carrier is not being received

faulting

The faulting variable set by the Far-End Fault Detect process, when implemented, indicating whether or not a Far-End Fault Indication is being sensed. This variable is used by the Link Monitor process to force link_status to FAIL.When Far-End Fault is not implemented, this variable is always FALSE.

Values: TRUE; Far-End Fault Indication is being sensed
FALSE; Far-End Fault Indication is not being sensed

link_control

The link_control parameter as communicated by the PMA_LINK.request primitive. When Auto-Negotiation is not implemented, the value of link_control is always ENABLE. See Clause 28 for a complete definition.

link_status

The link_status parameter as communicated by the Link Monitor process through the PMA_LINK.indicate primitive.

Values: FAIL; the receive channel is not intact

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READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
OK; the receive channel is intact and enabled for reception

r_bits [9:0]

In Carrier Detect, a vector of the 10 most recently received code-bits from the PMD RX process. r_bits [0] is the most recently received (newest) code-bit; r_bits [9] is the least recently received code-bit (oldest). r_bits is an internal variable used exclusively by the Carrier Detect process.

rx_code-bit

The rx_code-bit parameter as delivered by the RX process, which operates in synchronism with the PMD_UNITDATA.indicate primitive. rx_code-bit is the most recently received code-bit from the PMD after conversion from NRZI.

rxerror_status

The rxerror_status parameter to be communicated by the Carrier Detect process through the PMA_RXERROR.indicate primitive.

Values: NO_ERROR; no error detected in the carrier event being received
ERROR; the carrier event being received is in error

signal_status

The signal_status parameter as communicated by the PMD_SIGNAL.indicate primitive.

Values: ON; the quality and level of the received signal is satisfactory
OFF; the quality and level of the received signal is not satisfactory

tx_code-bit_in

In Link Fault Generate, the tx_code-bit parameter as conveyed to the PMA from the PMA client by the PMA_UNITDATA.request.

tx_code-bit_out

In Link Fault Generate, the tx_code-bit parameter to be passed to the TX process. Note that this is called tx_code-bit by the TX process.

The following variables are required only for the optional EEE capability:

lpi_link_fail

The lpi_link_fail parameter is communicated by the PMA_LPILINKFAIL.request primitive. In the LPI mode, this variable is generated by the Receive process of the PCS to control the transition to a Link Down state. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.

Values: TRUE; local receiver has detected a link failure status when in an LPI state
FALSE; local receiver is functioning normally when in an LPI state

rx_lpi

The rx_lpi parameter is communicated by the PMA_RXLPI.request primitive. This variable is generated by the Receive process of the PCS to indicate the LPI mode. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.

Values: TRUE; local receiver is in the LPI mode
FALSE; local receiver is in the normal operation mode

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24.3.3.3 Functions

SHIFTLEFT (rx_bits)

In Carrier Detect, this function shifts rx_bits left one bit placing rx_bits [8] in rx_bits [9], rx_bits [7] in rx_bits [8] and so on until rx_bits [1] gets rx_bits [0].

24.3.3.4 Timers

stabilize_timer

An implementation-dependent delay timer between 330 µs and 1000 µs, inclusive, to ensure that the link is stable.

24.3.3.5 Counters

num_cycles

In Link Fault Detect, a counter containing the number of consecutive Far-End Fault cycles currently sensed. This counter gets reset on initialization or when the bit stream fails to qualify as a potential Far-End Fault Indication. It never exceeds FEF_CYCLES.

num_ones

This represents two separate and independent counters: In Link Fault Generate, a counter containing the number of consecutive ONEs already sent during this cycle of the Far-End Fault Indication. In Link Fault Detect, a counter containing the number of consecutive ONEs currently sensed; it gets reset whenever a ZERO is detected or when the bit stream fails to qualify as a potential Far-End Fault Indication. These counters never exceed FEF_ONES.

24.3.3.6 Messages

PMD_UNITDATA.indicate (rx_nrzi-bit)

A signal sent by the PMD signifying that the next nrzi-bit is available from the medium. nrzi-bit is converted (instantaneously) to code-bit by the RX process and used by the Carrier Detect process.

5xPMD_UNITDATA.indicates

In Carrier Detect, this shorthand notation represents repetition of the preceding state five times synchronized with five successive PMD_UNITDATA.indicates.

PMA_UNITDATA.request (tx_code-bit)

A signal sent by the PMA's client signifying that the next nrzi-bit is available for transmission. For this process, the tx_code-bit parameter is interpreted as tx_code-bit_in.

24.3.4 Process specifications and state diagrams

24.3.4.1 TX

The TX process passes data from the PMA's client directly to the PMD. The PMA shall implement the TX process as follows: Upon receipt of a PMA_UNITDATA.request (tx_code-bit), the PMA performs a conversion to NRZI format and generates a PMD_UNITDATA.request (tx_nrzi-bit) primitive with the same logical value for the tx_nrzi-bit parameter. Note that tx_code-bit is equivalent to tx_code-bit_out of the Link Fault Generate process when implemented.

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24.3.4.2 RX

The RX process passes data from the PMD directly to the PMA's client and to the Carrier Detect process. The PMA shall implement the RX process as follows: Upon receipt of a PMD_UNITDATA.indicate (rx_nrzi-bit), the PMA performs a conversion from NRZI format and generates a PMA_UNITDATA.indicate (rx_code-bit) primitive with the same logical value for the rx_code-bit parameter.

24.3.4.3 Carrier detect

The PMA Carrier Detect process provides repeater clients an indication that a carrier event has been sensed and an indication if it is deemed in error. A carrier event is defined as receipt of two non-contiguous ZEROS within any 10 rx_code-bits. A carrier event is in error if it does not start with an SSD. The Carrier Detect process performs this function by continuously monitoring the code-bits being delivered by the RX process, and checks for specific patterns that indicate non-IDLE activity and SSD bit patterns.

The Carrier Detect process collects code-bits from the PMD RX process. r_bits [9:0] represents a sliding, 10-bit window on the code-bit sequence, with newly received code-bits from the RX process being shifted into r_bits [0]. The process shifts the r_bits vector to the left, inserts the newly received code-bit into position 0, and waits for the next PMD.UNITDATA.indicate before repeating the operation. This is depicted in Figure 24–13. The Carrier Detect process monitors the r_bits vector until it detects two noncontiguous ZEROS in the incoming code-bit sequence. This signals a transition of carrier_status from OFF to ON. Each new carrier is further examined for a leading SSD (1100010001) with rxerror_status set to ERROR if it is not confirmed. A pattern of 10 contiguous ONEs in the stream indicates a return to carrier_status = OFF. Code-bit patterns of contiguous ONEs correspond to IDLE code-groups in the PCS, per the encoding specified in 24.2.2.1.

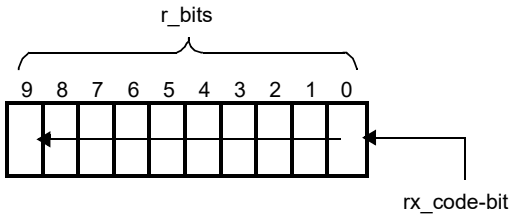

Figure 24–13—Carrier Detect reference diagram

The PMA shall, if it is supporting a repeater, implement the Carrier Detect process as depicted in Figure 24–14 including compliance with the associated state variables as specified in 24.3.3.

24.3.4.4 Link Monitor

The Link Monitor process is responsible for determining whether the underlying receive channel is providing reliable data. Failure of the underlying channel typically causes the PMA's client to suspend normal actions. The Link Monitor process takes advantage of the PMD sublayer's continuously signaled transmission scheme, which provides the PMA with a continuous indication of signal detection on the channel through signal_status as communicated by the PMD_SIGNAL.indicate primitive. It responds to control by Auto-Negotiation, when implemented, which is effected through the link_control parameter of PMA_SIGNAL.request.

The Link Monitor process monitors signal_status, setting link_status to FAIL whenever signal_status is OFF during the normal operation or when Auto-Negotiation sets link_control to DISABLE. If the EEE capability is supported, when the receiver is in the LPI mode, the assertion of lpi_link_fail shall set the link_status to FAIL and eventually brings the receiver out of the LPI mode. The link is deemed to be reliably operating

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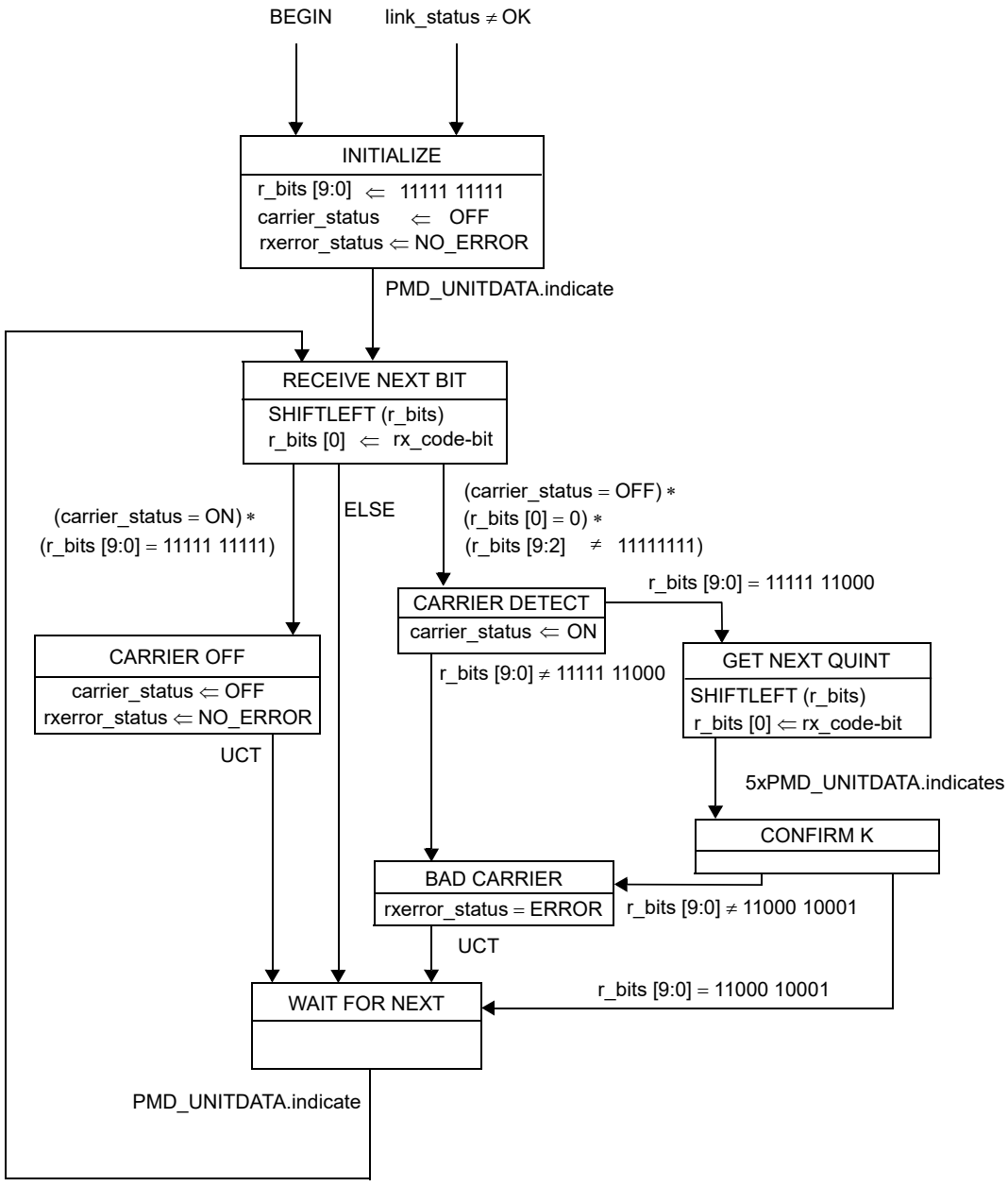

Figure 24–14—Carrier Detect state diagram

when signal_status has been continuously ON for a period of time. This period is implementation dependent but not less than 330 µs or greater than 1000 µs. If so qualified, Link Monitor sets link_status to READY in order to synchronize with Auto-Negotiation, when implemented. Auto-Negotiation permits full operation by setting link_control to ENABLE. When Auto-Negotiation is not implemented, Link Monitor operates with link_control always set to ENABLE.

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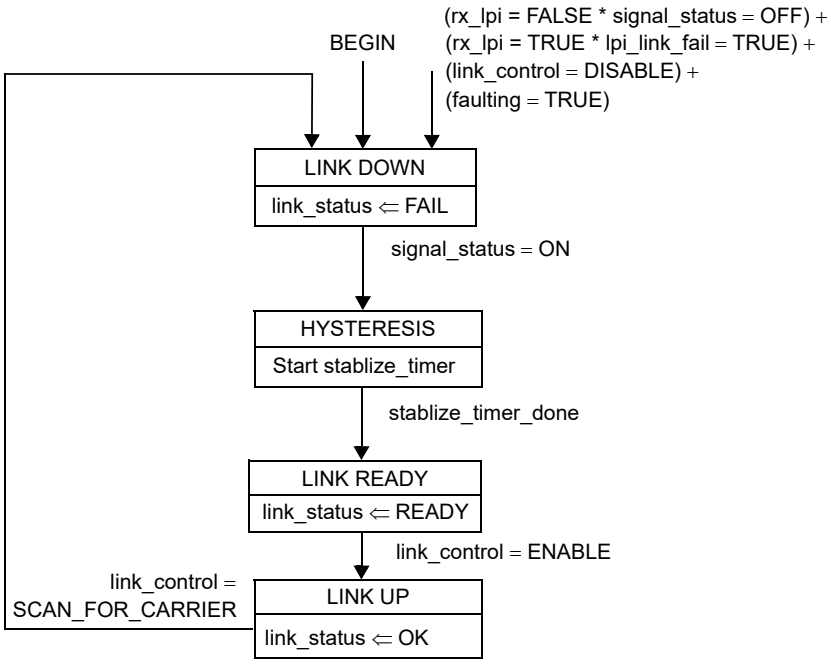
The PMA shall implement the Link Monitor process as depicted in Figure 24–15 including compliance with the associated state variables as specified in 24.3.3.



NOTE 1—The variables link_control and link_status are designated as link_control_[TX] and link_status_[TX], respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

NOTE 2—The variables rx_lpi and lpi_link_fail are only required for the EEE capability and should be treated as if the value of these two variables is FALSE otherwise.

Figure 24–15—Link Monitor state diagram

24.3.4.5 Far-End Fault Generate

Far-End Fault Generate simply passes tx_code-bits to the TX process when signal_status=ON. When signal_status=OFF and not in the LPI mode, it repetitively generates each cycle of the Far-End Fault Indication until signal_status is reasserted.

If Far-End Fault is implemented, the PMA shall implement the Far-End Fault Generate process as depicted in Figure 24–16 including compliance with the associated state variables as specified in 24.3.3.

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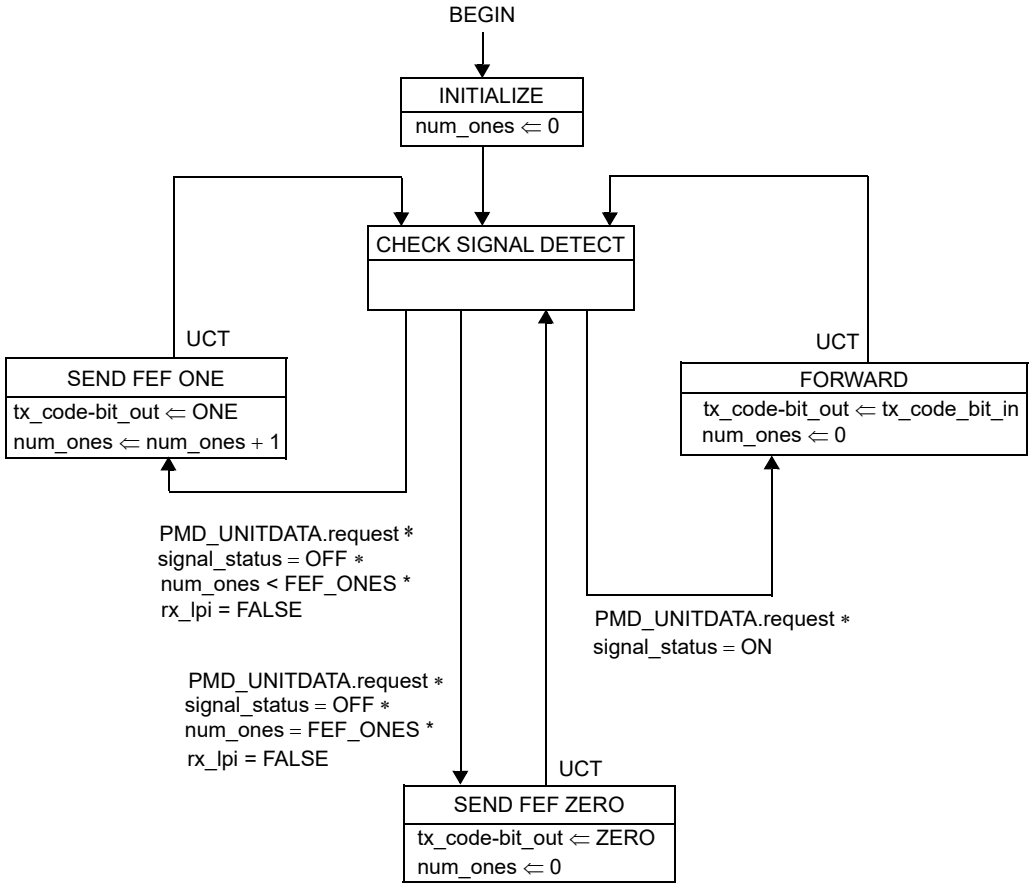

NOTE—The variable rx_lpi is only required for the EEE capability and should be treated as if the value of this variable is FALSE otherwise.

Figure 24–16—Far-End Fault Generation state diagram

24.3.4.6 Far-End Fault Detect

Far-End Fault Detect passively monitors the rx_code-bit stream from the RX process for the Far-End Fault Indication. It does so by maintaining counters for the number of consecutive ONEs seen since the last ZERO (num_ones) and the number of cycles of 84 ONEs and a single ZERO (num_cycles). The Far-End Fault Indication is denoted by three or more cycles, each of 84 ONEs and a single ZERO. Note that the number of consecutive ONEs may exceed 84 on the first cycle.

If Far-End Fault is implemented, the PMA shall implement the Far-End Fault Detect process as depicted in Figure 24–17 including compliance with the associated state variables as specified in 24.3.3.

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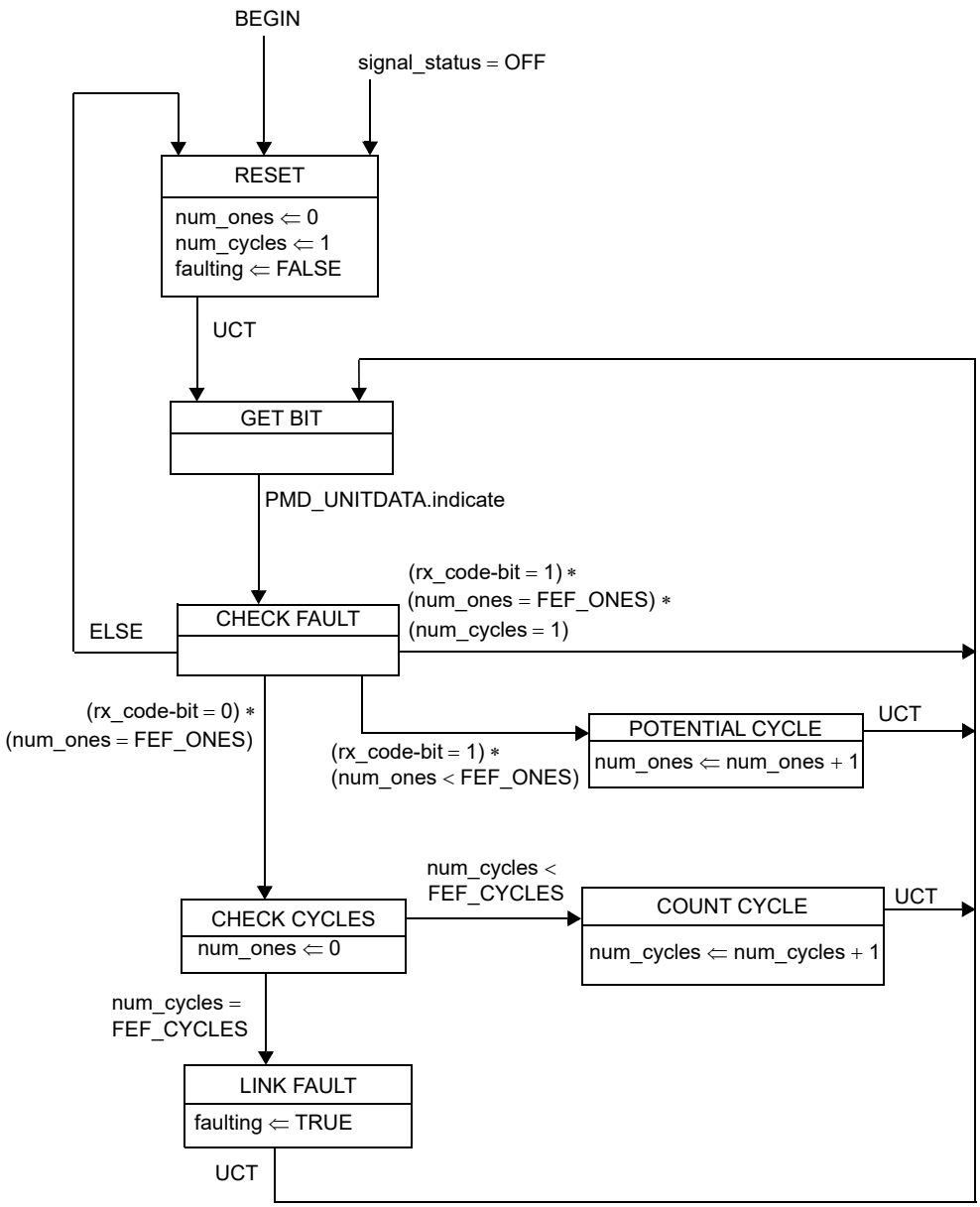

Figure 24–17—Far-End Fault Detect state diagram

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24.4 Physical Medium Dependent (PMD) sublayer service interface

24.4.1 PMD service interface

The following specifies the services provided by the PMD. The PMD is a sublayer within 100BASE-X and may not be present in other 100BASE-T PHY specifications. PMD services are described in an abstract manner and do not imply any particular implementation. It should be noted that these services are functionally identical to those defined in the FDDI standards, such as ISO/IEC 9314-3:1990 and ANSI INCITS 263-1995, with the following three exceptions:

a) 100BASE-X does not include a Station Management (SMT) function; therefore the PMD-to-SMT interface defined in ISO/IEC 9314-3:1990 and ANSI INCITS 263-1995.
b) 100BASE-X does not support multiple instances of a PMD in service to a single PMA; therefore, no qualifiers are needed to identify the unique PMD being referenced.
c) 100BASE-X may support LPI for the EEE capability.

There are also *editorial* differences between the interfaces specified here and in the referenced standards, as required by the context of 100BASE-X.

The PMD Service Interface supports the exchange of nrzi-bits between PMA entities. The PMD translates the nrzi-bits to and from signals suitable for the specified medium.

The following primitives are defined:

PMD_UNITDATA.request
PMD_UNITDATA.indicate
PMD_SIGNAL.indicate
PMD_RXQUIET.request
PMD_TXQUIET.request

24.4.1.1 PMD_UNITDATA.request

This primitive defines the transfer of data (in the form of nrzi-bits) from the PMA to the PMD.

24.4.1.1.1 Semantics of the service primitive

PMD_UNITDATA.request (tx_nrzi-bit)

The data conveyed by PMD_UNITDATA.request is a continuous sequence of nrzi-bits. The tx_nrzi-bit parameter can take one of two values: ONE or ZERO.

24.4.1.1.2 When generated

The PMA continuously sends, at a nominal 125 Mb/s rate, the PMD the appropriate nrzi-bits for transmission on the medium.

24.4.1.1.3 Effect of receipt

Upon receipt of this primitive, the PMD converts the specified nrzi-bit into the appropriate signals on the MDI.

24.4.1.2 PMD_UNITDATA.indicate

This primitive defines the transfer of data (in the form of nrzi-bits) from the PMD to the PMA.

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24.4.1.2.1 Semantics of the service primitive

PMD_UNITDATA.indicate (rx_nrzi-bit)

The data conveyed by PMD_UNITDATA.indicate is a continuous nrzi-bit sequence. The rx_nrzi-bit parameter can take one of two values: ONE or ZERO.

24.4.1.2.2 When generated

The PMD continuously sends nrzi-bits to the PMA corresponding to the signals received from the MDI.

24.4.1.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.4.1.3 PMD_SIGNAL.indicate

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

24.4.1.3.1 Semantics of the service primitive

PMD_SIGNAL.indicate (signal_status)

The signal_status parameter can take on one of two values: ON or OFF, indicating whether the quality and level of the received signal is satisfactory (ON) or unsatisfactory (OFF). When signal_status = OFF, then rx_nrzi-bit is undefined, but consequent actions based on PMD_SIGNAL.indicate, where necessary, interpret rx_nrzi-bit as logic ZERO.

24.4.1.3.2 When generated

The PMD generates this primitive to indicate a change in the value of signal_status.

24.4.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.4.1.4 PMD_RXQUIET.request

This primitive is generated by the Receive Process of the PCS only if EEE is supported to indicate that the receiver is in the LPI mode and the line is in the Quiet state (see 24.2.4.3 and Figure 24–12).

24.4.1.4.1 Semantics of the service primitive

PMD_RXQUIET.request(rx_quiet)

The rx_quiet parameter takes on one of two values, TRUE or FALSE, indicating whether the receiver is in the Quiet state (TRUE) or not (FALSE).

24.4.1.4.2 When generated

The PCS generates this primitive to indicate a Quiet state of the transmitter in the LPI mode.

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24.4.1.4.3 Effect of receipt

This primitive affects operation of the PMD function of type 100BASE-TX as described in 25.5.2. Other use of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.4.1.5 PMD_TXQUIET.request

This primitive is generated by the Transmit Process of the PCS only if EEE is supported to indicate that the transmitter is in the LPI mode and the line is in the Quiet state (see 24.2.4.2 and Figure 24–8).

24.4.1.5.1 Semantics of the service primitive

PMD_TXQUIETrequest(tx_quiet)

The tx_quiet parameter takes on one of two values, TRUE or FALSE, indicating whether the transmitter is in the Quiet state (TRUE) or not (FALSE).

24.4.1.5.2 When generated

The PCS generates this primitive to indicate a Quiet state of the transmitter in the LPI mode.

24.4.1.5.3 Effect of receipt

This primitive affects operation of the PMD function of type 100BASE-TX as described in 25.5.1. Other use of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.4.2 Medium Dependent Interface (MDI)

The MDI, a physical interface associated with a PMD, is composed of an electrical or optical medium connector. The 100BASE-X MDIs, defined in subsequent clauses, are specified by reference to the appropriate FDDI PMD, such as in ISO/IEC 9314-3:1990 and ANSI INCITS 263-1995, together with minor modifications (such as connectors and pin-outs) necessary for 100BASE-X.

24.5 Compatibility considerations

There is no requirement for a compliant device to implement or expose any of the interfaces specified for the PCS, PMA, or PMD. However, if an exposed interface is provided to the PCS, it shall comply with the requirements for the MII, as specified in Clause 22.

24.6 Delay constraints

In half duplex mode, proper operation of a CSMA/CD LAN demands that there be an upper bound on the propagation delays through the network. This implies that MAC, PHY, and repeater implementations conform to certain delay minima and maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

In full duplex mode, predictable operation of the (optional) MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

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MAC constraints are contained in Clause 21. Topological constraints are contained in Clause 29. MAC Control sublayer constraints are contained in Clause 31.

The reference point for all MDI measurements is the 50% point of the mid-cell transition corresponding to the reference code-bit, as measured at the MDI. Although 100BASE-TX output is scrambled, it is assumed that these measurements are made via apparatuses that appropriately account for this.

24.6.1 PHY delay constraints (exposed MII)

Every 100BASE-X PHY with an exposed MII shall comply with the bit delay constraints specified in Table 24–2 and Table 24–3. These figures apply for all 100BASE-X PMDs.

Table 24–2—Bit delay constraints

a) MDI to MII delay constraints (exposed MII, half duplex mode)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MII ⇔ MDI	TX_EN sampled to MDI output	6	14	TX_CLK rising	1st bit of /J/
	MDI input to CRS assert		20	1st bit of /J/	
	MDI input to CRS deassert (aligned)	13	24	1st bit of /T/	
	MDI input to CRS deassert (unaligned)	13	24	1st ONE	
	MDI input to COL assert		20	1st bit of /J/	
	MDI input to COL deassert (aligned)	13	24	1st bit of /T/	
	MDI input to COL deassert (unaligned)	13	24	1st ONE	
	TX_EN sampled to CRS assert	0	4	TX_CLK rising	
	TX_EN sampled to CRS deassert	0	16	TX_CLK rising	

Table 24–3—Bit delay constraints *(continued)*

b) PHY delay constraints (exposed MII, full duplex mode)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MII ⇔ MDI	TX_EN sampled to MDI output		14	TX_CLK rising	1st bit of /J/
	MDI Input to RX_DV deassert		32	first bit of /T/	RX_CLK rising

24.6.2 DTE delay constraints (unexposed MII)

Every 100BASE-X DTE with no exposed MII shall comply with the bit delay constraints specified in Table 24–4. These figures apply for all 100BASE-X PMDs.

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Table 24–4—DTE delay constraints (unexposed MII, half duplex mode)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MAC ⇔ MDI	MAC transmit start to MDI output		18		1st bit of /J/
	MDI input to MDI output (worst-case nondeferred transmit)		54	1st bit of /J/	1st bit of /J/
	MDI input to collision detect		28	1st bit of /J/	
	MDI input to MDI output = Jam (worst case collision response)		54	1st bit of /J/	1st bit of jam

24.6.3 Carrier deassertion/assertion constraint (half duplex mode only)

To ensure fair access to the network, each DTE shall, additionally, satisfy the following:

(MAX MDI to MAC Carrier Deassert Detect) – (MIN MDI to MAC Carrier Assert Detect) < 13

24.7 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801.

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24.8 Protocol implementation conformance statement (PICS) proforma for Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X[57]

24.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

24.8.2 Identification

24.8.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

24.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[57] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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24.8.2.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*DTE	Supports DTE without MII	24.4	O/1		
*REP	Supports Repeater without MII	24.4	O/1		
*MII	Supports exposed MII interface	24.4	O/1		
*PCS	Implements PCS functions	24.2	REP: O DTE: M MII: M		
PMA	Implements PMA RX, TX and Link Monitor functions	24.3	M		
*LPC	PCS implementation of LPI	24.2	PCS:O		
*LPM	PMA implementation of LPI	24.3	LPC:M		
*NWC	Medium capable of supporting Auto-Negotiation		O		See Clause 28
*FEF	Implements Far-End Fault	24.3.2.1	NWC: X LPM:X		
NWY	Supports Auto-Negotiation (Clause 28)	24.1.4.4	NWC: O LPC:M		See Clause 28

24.8.3 PICS proforma tables for the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

24.8.3.1 General compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
GN1	Compliance with MII requirements	24.4	MII:M		See Clause 22
GN2	Environmental specifications	24.7	M		

24.8.3.2 PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PS1	Transmit Bits process	24.2.4.1	PCS:M		
PS2	Transmit process	24.2.4.2	PCS:M		
PS3	Receive Bits process	24.2.4.3	PCS:M		
PS4	Receive process	24.2.4.4	PCS:M		
PS5	Carrier Sense process	24.2.4.5	PCS:M		

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24.8.3.3 PMA functions

Item	Feature	Subclause	Status	Support	Value/Comment
PA1	TX process	24.3.4.1	M		
PA2	RX process	24.3.4.2	M		
PA3	Carrier Detect process	24.3.2.1	REP: M		
PA4	Link Monitor process	24.3.4.4	M		
PA5	Far-End Fault Generate process	24.3.4.5	FEF: M		
PA6	Far-End Fault Detect process	24.3.4.6	FEF: M		

24.8.3.4 Timing

Item	Feature	Subclause	Status	Support	Value/Comment
TM1	Support for MII signals TX_CLK and RX_CLK	24.2.2.3	MII:M		See Clause 22
TM2	Accuracy of code-bit_timer	24.2.3	M		
TM3	Compliance with PHY bit delay constraints	24.6.1	MII:M REP: O		
TM4	Compliance with DTE bit delay constraints	24.6.2	DTE:M		
TM5	Compliance with Carrier Deassert/Assert Constraint	24.6.3	DTE:M		

24.8.3.5 LPI functions

Item	Feature	Subclause	Status	Support	Value/Comment
LF1	lpi_rx_ti_timer	24.2.3.4	LPC:M		The timer has a period between 0.8–0.9 μs.
LF2	lpi_rx_tq_timer	24.2.3.4	LPC:M		The timer has a period between 24–26 ms.
LF3	lpi_rx_ts_timer	24.2.3.4	LPC:M		The timer has a period between 240–260 μs.
LF4	lpi_rx_tw_timer	24.2.3.4	LPC:M		The timer has a period that does not exceed 20.5 μs.
LF5	LPI wake error counter	24.2.3.4	LPC:M		Increment the wake error counter for each transition of lpi_rx_tw_timer_done from false to true.

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Item	Feature	Subclause	Status	Support	Value/Comment
LF6	lpi_tx_tq_timer	24.2.3.4	LPC:M		The timer has a period between 20–22 ms.
LF7	link failure caused by lpi_rx-_tq_timer	24.2.3.4	LPC:M		The receiver assumes a link failure if the PHY fails to receive a valid Refresh or Wake signal before the lpi_rx_tq_timer expires.
LF8	lpi_tx_ts_timer	24.2.3.4	LPC:M		The timer has a period between 200–220 μs.
LF9	lpi_link_fail_timer	24.2.3.4	LPC:M		The timer has a period between 90–110 μs.
LF11	lpi_link_fail	24.3.3.2	LPM:M		The PHY operates as if the value of this variable is FALSE in the absence of the optional EEE capability.
LF12	rx_lpi	24.3.3.2	LPM:M		The PHY operates as if the value of this variable is FALSE in the absence of the optional EEE capability.
LF13	link_status affected by lpi_link_fail	24.3.4.4	LPM:M		The assertion of lpi_link_fail sets the link_status to FAIL if the EEE is supported and the receiver is in the LPI mode.

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25. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

25.1 Overview

This clause specifies the 100BASE-X PMD (including MDI) and baseband medium for twisted-pair wiring, 100BASE-TX. In order to form a complete 100BASE-TX Physical Layer, the 100BASE-X PMD (including MDI) shall be integrated with the 100BASE-X PCS and PMA of Clause 24, which are assumed incorporated by reference. As such, the 100BASE-TX PMD shall comply with the PMD service interface specified in 24.4.1.

25.1.1 State diagram conventions

The body of this standard is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams follows the conventions of 21.5; state diagram timers follow the conventions of 14.2.3.2.

25.2 Functional specifications

The 100BASE-TX PMD (and MDI) is specified by incorporating the FDDI TP-PMD standard, ANSI INCITS 263-1995 (TP-PMD), by reference, with the modifications noted below. This standard provides support for Category 5 twisted pair cabling. For improved legibility in this clause, ANSI INCITS 263-1995 (TP-PMD), will henceforth be referred to as TP-PMD.

25.3 General exceptions

The 100BASE-TX PMD is precisely the PMD specified as TP-PMD, with the following general modifications:

a) The Scope and General description discussed in TP-PMD 1 and 5 relate to the use of those standards with an FDDI PHY, ISO/IEC 9314-1:1989, and MAC, ISO/IEC 9314-2:1989. These sections are not relevant to the use of the PMD with 100BASE-X.
b) The Normative references, Definitions and Conventions of TP-PMD 2, 3, and 4 are used only as necessary to interpret the applicable sections of TP-PMD referenced in this clause.
c) The PMD Service Specifications of TP-PMD 6 are replaced by those specified in 24.4.1. The 100BASE-TX PMD Service specification is a proper subset of the PMD Service Specification in TP-PMD.
d) The twisted-pair cabling specifications of TP-PMD 11.1 are replaced by those specified in 25.4.9.
e) 100BASE-TX optionally supports Energy-Efficient Ethernet (EEE), as described in Clause 78, with its Low Power Idle (LPI). Two new service primitives PMD_RXQUIET.request(rx_quiet) (see 24.4.1.4) and PMD_TXQUIET.request(tx_quiet) (see 24.4.1.5) are generated by the PCS to pass the energy saving requests.
f) There are minor terminology differences between this standard and TP-PMD that do not cause ambiguity. The terminology used in 100BASE-X was chosen to be consistent with other IEEE 802 standards, rather than with FDDI. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 25–1.

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Table 25–1—Interpretation of general FDDI terms and concepts

FDDI term or concept	Interpretation for 100BASE-TX
bypass	<unused>
Connection Management (CMT)	<no comparable entity>
frame	stream
Halt Line State (HLS)	<unused>
hybrid mode	<no comparable entity>
MAC (or MAC-2)	MAC
Master Line State (MLS)	<unused>
maximum frame size = 9000 symbols	maximum stream size = 4018 code-groups
PHY (or PHY-2)	PMA; i.e., PMD client
PHY Service Data Unit (SDU)	stream
PM_SIGNAL.indication (Signal_Detect)	PMD_SIGNAL.indication (signal_status)
PM_UNITDATA.indication (PM_Indication)	PMD_UNITDATA.indication (nrzi-bit)
PM_UNITDATA.request (PM_Request)	PMD_UNITDATA.request (nrzi-bit)
preamble	inter-packet IDLEs
Quiet Line State (QLS)	<unused>
SM_PM_BYPASS.request (Control_Action)	Assume: SM_PM_BYPASS.request(Control_Action = Insert)
SM_PM_CONTROL.request (Control_Action)	Assume: SM_PM_CONTROL.request (Control_Action = Transmit_Enable)
SM_PM_SIGNAL.indication (Signal_Detect)	<unused>
Station Management (SMT)	<no comparable entity>
symbol	code-group

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25.4 Specific requirements and exceptions

The 100BASE-TX PMD (including MDI) shall comply to the requirements of TP-PMD, 7, 8, 9, 10, and 11, and normative Annex A with the exceptions listed below. In TP-PMD, informative annexes B, C, E, G, I, and J, with exceptions listed below, provide additional information useful to PMD sublayer implementers. Where there is conflict between specifications in TP-PMD and those in this standard, those of this standard shall prevail.

25.4.1 Change to 7.2.3.1.1, “Line state patterns”

Descrambler synchronization on the Quiet Line State (QLS), Halt Line State (HLS), and Master Line State (MLS) Line State Patterns cited in TP-PMD 7.2.3.1.1 is optional.

25.4.2 Change to 7.2.3.3, “Loss of synchronization”

The synchronization error triggered by PH_Invalid as defined in TP-PMD 7.2.3.3a is not applicable.

25.4.3 Change to Table 8-1, “Contact assignments for twisted pair”

100BASE-TX for twisted pair adopts the contact assignments of 10BASE-T. Therefore, the contact assignments shown in TP-PMD Table 8-1 shall instead be as depicted in Table 25–2.

Table 25–2—Twisted-pair MDI contact assignments

Contact	PHY without internal crossover MDI SIGNAL	PHY with internal crossover MDI SIGNAL
1	Transmit +	Receive +
2	Transmit –	Receive –
3	Receive +	Transmit +
4		
5		
6	Receive –	Transmit –
7		
8		

25.4.4 Deletion of 8.3, “Station labelling”

Clause 8.3 of TP-PMD shall not be applied to 100BASE-TX.

25.4.5 Change to 9.1.7, “Worst case droop of transformer”

A 100BASE-TX receiver in a Type 2, Type 3, or Type 4 Endpoint PSE or Type 2, Type 3, or Type 4 PD (see Clause 33 and Clause 145) shall meet the requirements of 25.4.7. A 100BASE-TX transmitter in a Type 2 Endpoint PSE or Type 2 PD delivering or accepting more than 13.0 W average power shall meet either the Open Circuit Inductance (OCL) requirement in 9.1.7 of TP-PMD or meet the requirements of

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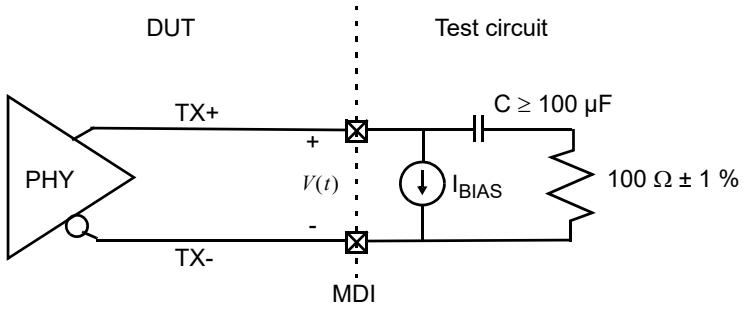
25.4.5.1. A 100BASE-TX transmitter in a Type 3 or Type 4 Endpoint PSE or Type 3 or Type 4 PD shall meet either the Open Circuit Inductance (OCL) requirement in 9.1.7 of TP-PMD, or meet the requirements of 25.4.5.1.

25.4.5.1 Equivalent system time constant

While transmitting the Data Dependent Jitter (DDJ) packet of TP-PMD A.2, using the test circuit shown in Figure 25–1, the equivalent system time constant, τ, shall be greater than 2.4 µs when calculated using measurement points A and C as shown in Figure 25–2.



DUT = Device under test

NOTE— I_{BIAS} is the current I_{unb} / 2 defined in Clause 33.

Figure 25–1—Type 2 System time constant test circuit

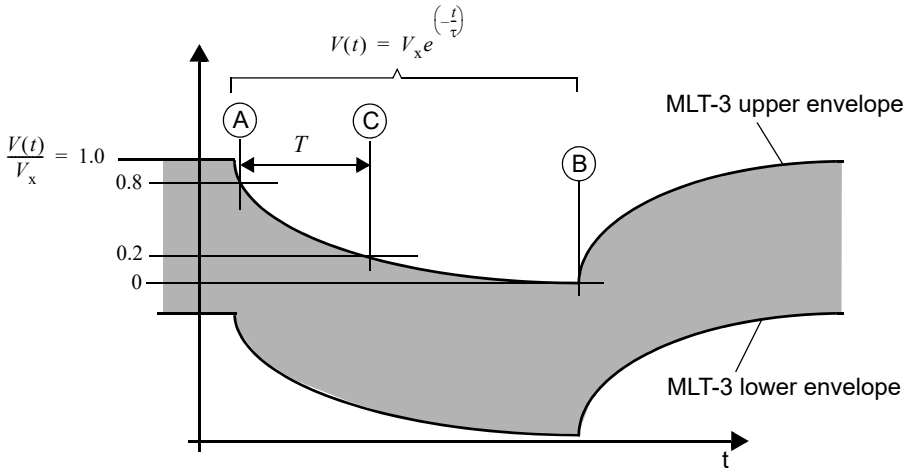


Figure 25–2—Type 2 System time constant measurement

Point B is the point of maximum baseline wander droop, and is the zero point for the vertical axis. Point A, with MDI voltage V_A, is earlier in time from B, with a magnitude that is 80 % of the MLT-3 upper envelope value. Point C, with MDI voltage V_C, is between A and B, with a magnitude that is 20 % of the MLT-3 upper envelope value. The time between A and C is *T*.

These measurements are to be made for the transmitter pair, observing the differential signal output at the MDI with intervening cable, meeting or exceeding the requirements of 25.4.7, less than 1 m long.

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The time constant of the transmitter MDI connected to the test circuit of Figure 25–1 is given by Equation (25–1).

$$\left\{ \tau = \frac{T}{\ln\left(\frac{V_A}{V_C}\right)} = \frac{2L}{R} \right\}_s \tag{25–1}$$

where

τ	is the effective time constant of the transmitter
T	is the time in seconds from point A to point C as shown in Figure 25–2
V_A	is the MDI voltage at point A
V_C	is the MDI voltage at point C
L	is the open-circuit inductance of the Ethernet isolation transformer for all operating conditions
R	is the 100 Ω termination impedance

25.4.6 Replacement of 8.4.1, “UTP isolation requirements”

A PMD with a MDI that is a PI (see 33.1.3 and 145.1.3) shall meet the isolation requirements defined in 33.4.1 and 145.4.1.

A PMD with a MDI that is not a PI shall provide isolation between frame ground and all MDI leads including those not used by the 100BASE-TX PMD.

This electrical isolation shall meet the isolation requirements as specified in J.1.

NOTE—In the case of a PMD with a MDI that is not a PI, these requirements are equivalent to those found in TP-PMD.

25.4.7 Addition to 10.1, “Receiver”

Differential voltage signals generated by a remote transmitter that meets the specifications of Clause 25; passed through a link specified in 25.4.9; and received at the MDI of a 100BASE-TX PMD in a Type 2, Type 3, or Type 4 Endpoint PSE or a Type 2, Type 3, or Type 4 PD shall be translated into one of the PMD_UNITDATA.indicate messages with a bit error ratio less than 10^{-9} after link reset completion.

25.4.8 Change to 9.1.9, “Jitter”

The jitter measurement specified in 9.1.9 of TP-PMD may be performed using scrambled IDLEs.

In the LPI mode, jitter shall be measured using scrambled SLEEP code-groups transmitted during the TX_SLEEP state (see Figure 24–8). Total transmit jitter with respect to a continuous unjittered reference shall not exceed 1.4 ns peak-to-peak with the exception that the jitter contributions from the clock transitions occurring during the TX_QUIET state and the first 5 µs of the TX_SLEEP state or the first 5 µs of the IDLE state following a TX_QUIET state are ignored. The jitter measurement time period shall be not less than 100 ms and not greater than 1 s.

25.4.9 Cable plant

The twisted-pair cabling specification of TP-PMD 11.1 is replaced by that specified in this subclause. The term “link segment” used in this subclause refers to a duplex channel of two pairs. Specifications for a link

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segment apply equally to each of the two pairs of a duplex channel. All implementations of the balanced cabling link shall be compatible at the MDI.

25.4.9.1 Cabling system characteristics

The cabling system used to support a 100BASE-TX duplex channel requires two pairs of Category 5 balanced cabling with a nominal impedance of 100 Ω. The cabling system components (cables, cords, and connectors) used to provide the link segment shall consist of Category 5 components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995 (Class D).

NOTE—ISO/IEC 11801:2002 provides a specification (Class D) for media that exceeds the minimum requirements of this standard.

25.4.9.2 Link transmission parameters

The transmission parameters contained in this subclause are specified to ensure that a Category 5 link segment of up to 100 m, will provide a reliable medium. The transmission parameters of the link segment include insertion loss, characteristics impedance, return loss, NEXT loss, and external coupled noise.

25.4.9.2.1 Insertion loss

The insertion loss of the link segment shall be less than,

$$\text{Insertion\_Loss}(f) < 2.1f^{0.529} + 0.4/f \qquad \text{(dB)}$$

at all frequencies from 1 MHz to 100 MHz. This includes the attenuation of the balanced cabling pairs, including work area and equipment cables plus connector losses within the link segment.

The insertion loss specification shall be met when the link segment is terminated in 100 Ω.

NOTE—The above equation approximates the insertion loss specification at 20°C for discrete frequencies of Category 5 100-meter links specified in ANSI/TIA/EIA-568-A Annex E and in TIA/EIA TSB-67.

25.4.9.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each link segment, which includes cable cords and connecting hardware, is 100 Ω for all frequencies between 1 MHz and 100 MHz.

25.4.9.2.3 Return loss

Each link segment shall meet or exceed the return loss specified in the following equation at all frequencies from 1 MHz to 100 MHz.

$$\text{Return\_Loss}(f) \begin{cases} 15 & (1 - 20\ \text{MHz}) \\ 15 - 10\log_{10}(f/20) & (20 - 100\ \text{MHz}) \end{cases} \text{(dB)}$$

where f is the frequency in MHz. The reference impedance shall be 100 Ω.

25.4.9.2.4 Differential near-end crosstalk (NEXT)

In order to limit the crosstalk at the near end of a duplex channel, the differential pair-to-pair near-end crosstalk (NEXT) loss between the two pairs of a duplex channel shall be at least,

$$27.1 - 16.8\log_{10}(f/100) \text{ (dB)}$$

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where *f* is the frequency over the range of 1 MHz to 100 MHz.

NOTE—The above equation approximates the NEXT loss specification at discrete frequencies for Category 5 100-meter links specified in ANSI/TIA/EIA-568-A Annex E and in TIA/EIA TSB-67.

25.4.9.3 Noise environment

The 100BASE-TX noise environment consists of noise from external sources and could impact the objective BER. This noise may consist of sources outside the cabling that couple into the link segment via electric and magnetic fields. In addition noise from adjacent cables, referred to as alien crosstalk, may couple into the link segment. This alien crosstalk is generally present when cables are bound tightly together. To ensure robust operation a 100BASE-TX PHY should operate in the presence of an external noise as specified in 25.4.9.3.1.

25.4.9.3.1 External coupled noise

The differential noise coupled from external sources that is measured at the output of a filter connected to the output of the near end of a disturbed link segment should not exceed 40 mV peak-to-peak. The filter for this measurement is a fifth order Butterworth filter with a 3 dB cutoff at 100 MHz.

25.4.10 Replacement of 11.2, “Crossover function”

Subclause 11.2 of TP-PMD is replaced with the following:

A crossover function compliant with 14.5.2 shall be implemented except that a) the signal names are those used in TP-PMD, and b) the contact assignments for 150 Ω Type 1 STP are those shown in Table 8-2 of TP-PMD. Note that compliance with 14.5.2 implies a recommendation that crossover (for both balanced twisted-pair and 150 Ω Type 1 STP) be performed within repeater PHYs.

25.4.11 Change to A.2, “DDJ test pattern for baseline wander measurements”

The length of the test pattern specified in TP-PMD A.2 may be shortened to accommodate feasible 100BASE-X measurements, but shall not be shorter than 3000 code-groups.

NOTE—This pattern is to be applied to the MII. (When applied to the MAC, the nibbles within each byte are to be swapped, e.g., as delivered to the MAC, the test pattern would start, “60 C9 16 ...”.)

25.4.12 Change to Annex G, “Stream cipher scrambling function”

An example of a stream cipher scrambling implementation is shown in TP-PMD Annex G. This may be modified to allow synchronization solely on the IDLE sequences between packets.

25.4.13 Change to Annex I, “Common mode cable termination”

The contact assignments shown in TP-PMD Figures I-1 and I-2 shall instead comply with those specified in Table 25–2.

25.5 EEE capability

TP-PMD does not have an option to support EEE. In order to add this capability to existing TP-PMD specification, the TP-PMD 7.1.2, 7.2.2, 10.1.2, 10.1.3, and Table 4 are modified to incorporate the LPI function. This subclause only applies to the optional EEE capability. If LPI is implemented, the operation of the PMD shall comply with the requirements in this subclause.

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25.5.1 Change to TP-PMD 7.1.2 “Encoder”

The Encoder receives the scrambled NRZ data stream from the scrambler (see TP-PMD 7.1.1) and encodes the stream into MLT3 code for presentation to the driver (see TP-PMD 7.1.3). MLT3 coding is similar to NRZI coding, but three instead of two levels are transmitted. The Encoder can be deactivated when in the LPI mode. The PMD Encoder function of the 100BASE-TX with EEE capability is identical to that of the TP-PMD except that the output of the Encoder is set to a value ZERO_VOLTAGE when the transmitter is in the Quiet state of the LPI mode (TX_QUIET, see Figure 24–8).

The PMD in the LPI mode shall implement the Encoder state diagram as depicted in Figure 25–3.

25.5.1.1 State variables

25.5.1.1.1 Variables

encoder_input
: Indicates the value of each scrambled NRZ bit to be encoded.

  Values: ZERO; the NRZ bit from the scrambler has a logical value 0
  ONE; the NRZ bit from the scrambler has a logical value 1

encoder_output
: Indicates the value from the encoder for each MLT-3 encoded bit.

  Values: POSITIVE_VOLTAGE; the output indicates a positive value of voltage to TP-PMD driver
  ZERO_VOLTAGE; the output indicates a zero value of voltage to TP-PMD driver
  NEGATIVE_VOLTAGE; the output indicates a negative value of voltage to TP-PMD driver

tx_quiet
: The tx_quiet parameter as communicated by the PMD_TXQUIET.request (tx_quiet) primitive. This variable is generated by the Transmit process of the PCS to control the power-saving function of the local transmitter. It sets the Encoder state diagram to an initial state of ZERO_V.

  Values: TRUE; the local transmitter is in the Quiet state
  FALSE; the local transmitter is not in the Quiet state

le_flag
: A Boolean set by the Encoder process to indicate whether the last non-zero value of encoder_output was POSITIVE_VOLTAGE. The flag le_flag is set upon entry to the PLUS_V state and is cleared upon entry to the MINUS_V state.

  Values: ONE; the encoder is in the PLUS_V state
  ZERO; the encoder is in the MINUS_V state

25.5.1.1.2 Messages

gotNRZbit.indicate
: A signal sent to the Encoder process by the scrambler after a scrambled NRZ text bit has been generated using recursive linear function by the scrambler from plaintext bit stream and is ready to transmit.

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25.5.1.2 State diagram

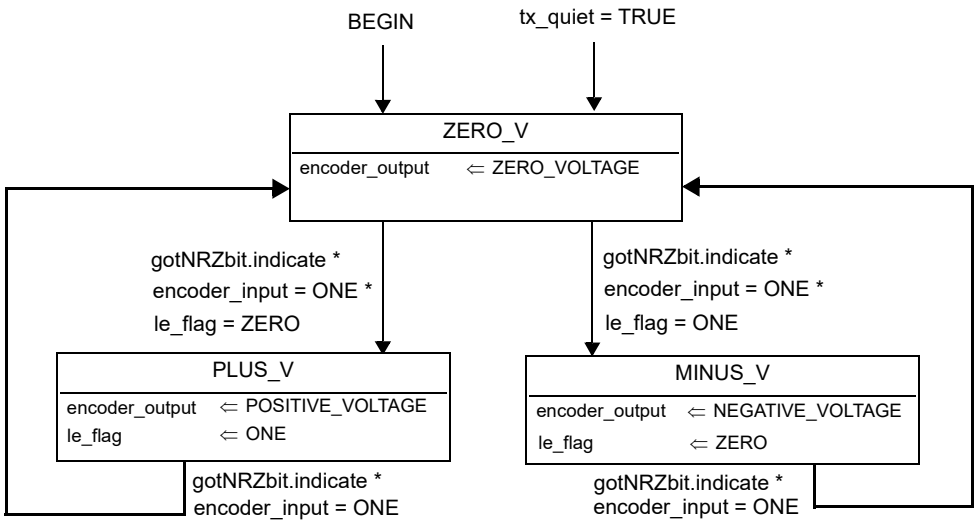

Figure 25–3—Encoder state diagram

25.5.2 Change to TP-PMD 7.2.2 “Decoder”

The Decoder receives the MLT3 encoded bit stream from the receiver (see TP-PMD 7.2.1), and decodes it into a NRZ encoded bit stream for presentation to the descrambler (see TP-PMD 7.2.3). The Decoder can be deactivated when in the LPI mode. The PMD Decoder function of the 100BASE-TX with EEE capability is identical to that of the TP-PMD except that the output of the Decoder is set to a value ZERO when the receiver is in the Quiet state of the LPI mode (RX_QUIET, Figure 24–12).

The PMD in the LPI mode shall implement the Decoder state diagram as depicted in Figure 25–4.

25.5.2.1 State variables

25.5.2.1.1 Variables

decoder_input
: Indicates the value of the MLT-3 encoded bit from the receiver.

  Values: ZERO; the MLT3 bit from the receiver has a logical value 0
  NONZERO; the MLT3 bit from the receiver has a non-zero logical value

decoder_output
: Indicates the value of the NRZ encoded bit.

  Values: ZERO; the output indicates a logical value of 0 to the descrambler
  ONE; the output indicates a logical value of 1 to the descrambler

rx_quiet
: The rx_quiet parameter as communicated by the PMD_RXQUIET.request (rx_quiet) primitive. This variable is generated by the Receive process of the PCS to control the power-saving function of local receiver. It sets the Decoder state diagram to an initial state of ZERO_VALUE.

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Values: TRUE; the local receiver is in the Quiet state
FALSE; the local receiver is not in the Quiet state

prev_data

Indicates whether the last value of decoder_input was ZERO or NONZERO.

Values: ZERO; the last value of MLT3 bit of decoder_input has a logical value 0
NONZERO; the last value of MLT3 bit of decoder_input has a non-zero logical value

25.5.2.1.2 Messages

sentNRZbit.indicate

A signal sent to the Decoder process by the descrambler after an NRZ bit from ciphertext bit stream has been processed using recursive linear function and is ready to process the next bit from Decoder.

25.5.2.2 State diagram

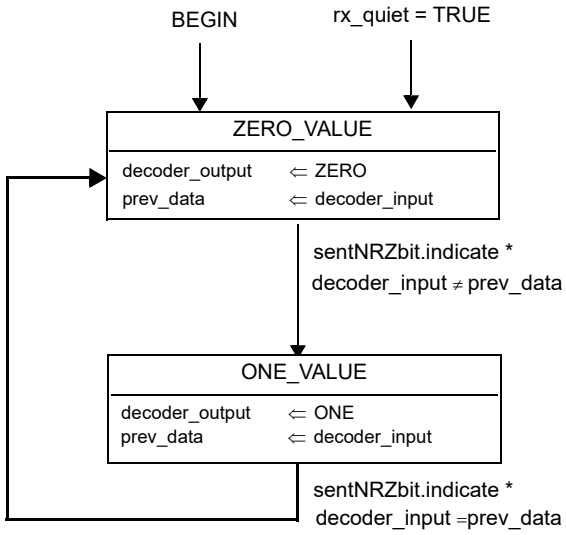

Figure 25–4—Decoder state diagram

25.5.3 Changes to 10.1.1.1 “Signal_Detect assertion threshold”

The TP-PMD 10.1.1.1 is applicable to the normal operation. In the LPI mode, when rx_lpi as communicated by the PMA_RXLPI.request primitive is asserted, Signal_Detect shall be asserted per 25.5.5 for any valid peak-to-peak signal, VSDA, of greater than 400 mV.

25.5.4 Changes to 10.1.1.2 “Signal_Detect deassertion threshold”

The TP-PMD 10.1.1.2 is applicable to the normal operation. In the LPI mode, when rx_lpi is deasserted, Signal_Detect shall be deasserted per 25.5.6 for any valid peak-to-peak signal, VSDD, of smaller than 200 mV.

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25.5.5 Change to 10.1.2 “Signal_Detect timing requirements on assertion”

The TP-PMD 10.1.2 is applicable to the normal operation. In the LPI mode, when rx_lpi is asserted, Signal_Detect output shall be asserted within 5 µs under the same quality requirement of the received signal as in normal operation. The new definition of conditional parameter AS_Max is inserted in TP-PMD Table 4 as depicted in Table 25–3.

25.5.6 Change to 10.1.3 “Signal_Detect timing requirements on deassertion”

The TP-PMD 10.1.3 is applicable to the normal operation. In the LPI mode, when rx_lpi is asserted, Signal_Detect output shall be deasserted within 5 µs under the same quality requirement of the received signal as in normal operation. The new definition of conditional parameter ANS_Max is inserted in TP-PMD Table 4 as depicted in Table 25–3.

25.5.7 Changes to TP-PMD 10.2 “Transmitter”

For the optional EEE capability, when tx_quiet (as communicated by the PMD_TXQUIET.request primitive) is set to FALSE, the transmitter output shall deliver a signal that exceeds Signal_Detect assertion threshold within 2 µs. The scrambler shall continue to operate for the first 5 µs following tx_quiet = TRUE. Transmit functions may be deactivated after this period. The transmitter shall deliver a fully compliant signal when tx_quiet is set to FALSE less than 5 µs after being set to TRUE. If tx_quiet is set to FALSE more than 5 µs after being set to TRUE, then the transmitter shall deliver a fully compliant signal within 5 µs (see 25.4.8).

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25.5.8 Replace TP-PMD Table 4 “Signal_Detect summary” with Table 25–3

The requirement of signal detection time and threshold are different between the normal operation mode and the LPI mode. In order to share one Signal_Detect, the timing and threshold characteristics may be qualified by LPI signal rx_lpi as communicated by the PMA_RXLPI.request primitive.

Table 25–3—Signal_Detect summary

Characteristic	Minimum	Maximum	Units
Assert time Normal operation mode		1000	µs
Deassert time Normal operation mode		350	µs
Assert time LPI mode		5	µs
Deassert time LPI mode		5	µs
Assert threshold VSDA 100 Ω balanced cable Normal operation mode		1000	mV peak to peak
Deassert threshold VSDD 100 Ω balanced cable Normal operation mode	200		mV peak to peak
Assert threshold VSDA 150 Ω balanced shielded cable Normal operation mode		1225	mV peak to peak
Deassert threshold VSDD 150 Ω balanced shielded cable Normal operation mode	245		mV peak to peak
Assert threshold VSDA LPI mode		400	mV peak to peak
Deassert threshold VSDD LPI mode	200		mV peak to peak

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25.6 Protocol implementation conformance statement (PICS) proforma for Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX[58]

25.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

25.6.2 Identification

25.6.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

25.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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25.6.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*TXU	Supports unshielded twisted pair	25.2	O/1		
TXS	Supports shielded twisted pair	25.2	O/1		
*LPI	Implementation of LPI	25.5	O		

25.6.3.1 Power over Ethernet major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*PSET2	Type 2 PSE implementation	33.1.4	O	Yes [ ] No [ ]	Optional
*PDT2	Type 2 PD implementation	33.3.2	O	Yes [ ] No [ ]	Optional

25.6.4 PICS proforma tables for the Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

25.6.4.1 General compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
GN1	Integrates 100BASE-X PMA and PCS	25.1	M		See Clause 24

25.6.4.2 PMD compliance

Item	Feature	Subclause	Status	Support	Value/Comment
PD1	Compliance with 100BASE-X PMD Service Interface	25.1	M		See 24.2.3
PD2	Compliance with ANSI INCITS 263-1995, 7, 8 (excluding 8.3), 9, 10, 11 and normative annex A, with listed exceptions	25.4 25.4.8	M		
PD3	Precedence over ANSI INCITS 263-1995	25.4	M		
PD4	MDI contact assignments for twisted pair	25.4.4 25.4.3	TXU: M		

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Item	Feature	Subclause	Status	Support	Value/Comment
PD5	Compliance with crossover function of 14.5.2 with listed adaptations	25.4.11	M		
PD6	Minimum jitter test pattern length	25.4.12	M		3000 code-groups
PD7	Isolation requirements	25.4.6	M		Conforms to J.1

25.6.4.3 Characteristics of link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	Implementations of balanced cabling link	25.4.9	M		Compatible at the MDI.
LKS2	100BASE-T links	25.4.9.1	M		Category 5 components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995 (Class D).
LKS3	Insertion loss	25.4.9.2.1	M		As specified in 25.4.9.2.1 at all frequencies from 1 MHz to 100 MHz when link segment is terminated in 100 Ω.
LKS4	Return loss	25.4.9.2.3	M		As specified in 25.4.9.2.3 at all frequencies from 1 MHz to 100 MHz when link segment is terminated in 100 Ω.
LKS5	Differential Near-End Crosstalk (NEXT)	25.4.9.2.4	M		As specified in 25.4.9.2.4 at all frequencies from 1 MHz to 100 MHz.

25.6.4.4 Power over Ethernet compliance

Item	Feature	Subclause	Status	Support	Value/Comment
DTEP1	Type 2 PD receiver worst-case droop transformer	25.4.5	PDT2:M	Yes [ ] No [ ]	Meet requirements of 25.4.7: differential voltage signals translated into one of the PMD_UNITDATA.indicate messages with a bit error ratio less than 10^{-9} after link reset completion
DTEP2	Type 2 Endpoint PSE receiver worst-case droop transformer	25.4.5	PSET2:M	Yes [ ] No [ ]	Meet requirements of 25.4.7: differential voltage signals translated into one of the PMD_UNITDATA.indicate messages with a bit error ratio less than 10^{-9} after link reset completion

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Item	Feature	Subclause	Status	Support	Value/Comment
DTEP3	Type 2 PD transmitter worst-case droop transformer while accepting more than 13 W average power	25.4.5	PDT2:M	Yes [ ] No [ ]	Meet OCL requirements of 9.1.7 or requirements in 25.4.5.1
DTEP4	Type 2 Endpoint PSE transmitter worst-case droop transformer while delivering more than 13 W average power	25.4.5	PSET2:M	Yes [ ] No [ ]	Meet OCL requirements in 9.1.7 or requirements in 25.4.5.1
DTEP5	Equivalent system time constant	25.4.5.1	M	Yes [ ] N/A [ ]	Greater than 2.4 µs when calculated using measurement points A and C in Figure 25–2

25.6.4.5 LPI functions

Item	Feature	Subclause	Status	Support	Value/Comment
LP1	Jitter measurement in the LPI mode	25.4.8	LPI:M	Yes [ ]	1.4 ns peak to peak
LP2	Code-groups used to measure jitter in the LPI mode	25.4.8	LPI:M	Yes [ ]	Scrambled SLEEP code-groups
LP3	Jitter measurement time interval in the LPI mode	25.4.8	LPI:M	Yes [ ]	No less than 100 ms and no greater than 1 s.
LP4	Encoder function in the LPI mode	25.5.1	LPI:M	Yes [ ]	Comply with the state diagram shown in Figure 25–3.
LP5	Decoder function in the LPI mode	25.5.2	LPI:M	Yes [ ]	Comply with the state diagram shown in Figure 25–4.
LP6	Signal_Detect assertion threshold in the LPI mode	25.5.3	LPI:M	Yes [ ]	Minimum 400 mV peak to peak
LP7	Signal_Detect deassertion threshold in the LPI mode	25.5.4	LPI:M	Yes [ ]	Maximum 200 mV peak to peak
LP8	Signal_Detect assertion time in the LPI mode	25.5.5	LPI:M	Yes [ ]	Maximum 5 µs
LP9	Signal_Detect deassertion time in the LPI mode	25.5.6	LPI:M	Yes [ ]	Maximum 5 µs
LP10	Scrambler and transmit functions deactivation time	25.5.7	LPI:M	Yes [ ]	The scrambler and transmit functions continue to operate for the first 5 µs following tx_quiet = TRUE.
LP11	Transmitter output amplitude initial ramp up time	25.5.7	LPI:M	Yes [ ]	The transmitter output delivers a signal that exceeds Signal_Detect assertion threshold within 2 µs when tx_quiet is set to TRUE.

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Item	Feature	Subclause	Status	Support	Value/Comment
LP12	Transmitter output recovery time after a short Quiet state	25.5.7	LPI:M	Yes [ ]	The transmitter delivers a fully compliant signal promptly if tx_quiet is set to FALSE less than 5 μs after being set to TRUE.
LP13	Transmitter output recovery time after a long Quiet state	25.5.7	LPI:M	Yes [ ]	The transmitter delivers a fully compliant signal within 5 μs if tx_quiet is set to FALSE more than 5 μs after being set to TRUE.

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26. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX

26.1 Overview

This clause specifies the 100BASE-X PMD (including MDI) and fiber optic medium for multimode fiber, 100BASE-FX. In order to form a complete 100BASE-FX Physical Layer it shall be integrated with the 100BASE-X PCS and PMA of Clause 24, which are assumed incorporated by reference. As such, the 100BASE-FX PMD shall comply with the PMD service interface specified in 24.4.1.

26.2 Functional specifications

The 100BASE-FX PMD (and MDI) is specified by incorporating the FDDI PMD standard, ISO/IEC 9314-3:1990, by reference, with the modifications noted below. This standard provides support for two optical fibers. For improved legibility in this clause, ISO/IEC 9314-3:1990 will henceforth be referred to as fiber-PMD.

26.3 General exceptions

The 100BASE-FX PMD is precisely the PMD specified as fiber-PMD, with the following general modifications:

a) The scope and general description discussed in fiber-PMD 1 and 5 relate to the use of those standards with an FDDI PHY, ISO/IEC 9314-1:1989, and MAC, ISO/IEC 9314-2:1989. These clauses are not relevant to the use of the PMD with 100BASE-X.
b) The normative references, definitions, and conventions of fiber-PMD 2, 3, and 4 are used only as necessary to interpret the applicable sections of fiber-PMD referenced in this clause.
c) The PMD Service Specifications of fiber-PMD 6 are replaced by those specified in 24.4.1. The 100BASE-FX PMD Service specification is a proper subset of the PMD service specification in fiber-PMD.
d) There are minor terminology differences between this standard and fiber-PMD that do not cause ambiguity. The terminology used in 100BASE-X was chosen to be consistent with other IEEE 802 standards, rather than with FDDI. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 26–1.

Table 26–1—Interpretation of general FDDI terms and concepts

FDDI term or concept	Interpretation for 100BASE-X
bypass	<unused>
Connection Management (CMT)	<no comparable entity>
frame	stream
Halt Line State (HLS)	<unused>
hybrid mode	<no comparable entity>
MAC (or MAC-2)	MAC
Master Line State (MLS)	<unused>
maximum frame size = 9000 symbols	maximum stream size = 4018 code-groups

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Table 26–1—Interpretation of general FDDI terms and concepts *(continued)*

FDDI term or concept	Interpretation for 100BASE-X
PHY (or PHY-2)	PMA; i.e., PMD client
PHY Service Data Unit (SDU)	stream
PM_SIGNAL.indication (Signal_Detect)	PMD_SIGNAL.indication (signal_status)
PM_UNITDATA.indication (PM_Indication)	PMD_UNITDATA.indication (nrzi-bit)
PM_UNITDATA.request (PM_Request)	PMD_UNITDATA.request (nrzi-bit)
preamble	inter-packet IDLEs
Quiet Line State (QLS)	<unused>
SM_PM_BYPASS.request (Control_Action)	Assume: SM_PM_BYPASS.request (Control_Action = Insert)
SM_PM_CONTROL.request (Control_Action)	Assume: SM_PM_CONTROL.request (Control_Action = Transmit_Enable)
SM_PM_SIGNAL.indication (Signal_Detect)	<unused>
Station Management (SMT)	<no comparable entity>
symbol	code-group

26.4 Specific requirements and exceptions

The 100BASE-FX PMD (including MDI) and baseband medium shall conform to the requirements of fiber-PMD Clauses 8, 9, and 10. In the referenced standard, fiber-PMD, informative Annex A through Annex G provide additional information useful to PMD sublayer implementers. Where there is conflict between specifications in fiber-PMD and those in this standard, those of this standard shall prevail.

26.4.1 Medium Dependent Interface (MDI)

The 100BASE-FX medium dependent interface (MDI) shall conform to one of the following connectors. The recommended alternative is the duplex SC connector.

a) The duplex SC connector as specified in IEC 61754-4 [B25][59] and IEC 61754-4, Interface 4-2. (See 38.11.3).
b) Media Interface Connector (MIC) as specified in fiber-PMD 7 and Annex F. When the MIC is used, the receptacle shall be keyed as “M”.
c) Optical Medium Connector Plug and Socket (commonly called ST[60] connector) as specified in 15.3.2.

26.4.2 Crossover function

A crossover function shall be implemented in every cable-pair link. The crossover function connects the transmitter of one PHY to the receiver of the PHY at the other end of the cable-pair link. For 100BASE-FX, the crossover function is realized in the cable plant.

[59]The numbers in brackets correspond to those of the bibliography in Annex A in Section One of this standard.
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26.5 Protocol implementation conformance statement (PICS) proforma for Clause 26, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX[61]

26.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 26, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

26.5.2 Identification

26.5.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

26.5.3 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 26, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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26.5.4 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
FSC	Supports duplex SC connector	26.4.1	O/1		Recommended. See IEC 61754-4 [B25] and IEC 61754-4, Interface 4-2. (See 38.11.3).
*FMC	Supports Media Interface Connector (MIC)	26.4.1	O/1		See ISO/IEC 9314-3:1990, 7 and Annex F
FST	Supports Optical Medium Connector Plug and Socket (ST)	26.4.1	O/1		See 15.3.2

26.5.5 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX

26.5.5.1 General compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
GN1	Integrates 100BASE-X PMA and PCS	26.1	M		See Clause 24

26.5.5.2 PMD compliance

Item	Feature	Subclause	Status	Support	Value/Comment
PD1	Compliance with 100BASE-X PMD Service Interface	26.1	M		See 24.4.1
PD2	Compliance with ISO/IEC 9314-3:1990 8, 9, and 10	26.4	M		
PD3	Precedence over ISO/IEC 9314-3:1990	26.4	M		
PD4	MIC receptacle keying	26.4.1	FMC: M		“M”
PD5	Crossover function in cable	26.4.2	M		

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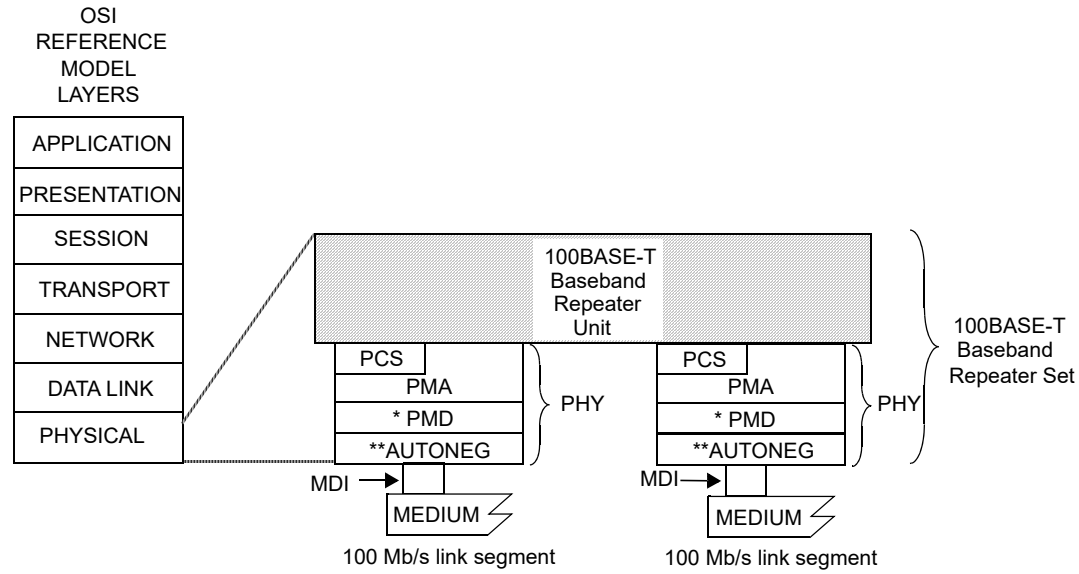
27. Repeater for 100 Mb/s baseband networks

NOTE—This repeater is not recommended for new installations. Since September 2011, maintenance changes are no longer being considered for this clause.

27.1 Overview

27.1.1 Scope

Clause 27 defines the functional and electrical characteristics of a repeater for use with 100BASE-T 100 Mb/s baseband networks. A repeater for any other IEEE 802.3 network type is beyond the scope of this clause. The relationship of this standard to the OSI Reference Model is shown in Figure 27–1. The purpose of the repeater is to provide a simple, inexpensive, and flexible means of coupling two or more segments.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* PMD is specified for 100BASE-TX and -FX only; 100BASE-T4 does not use this layer.
Use of MII between PCS and baseband repeater unit is optional.
** AUTONEG is optional.

Figure 27–1—100BASE-T repeater set relationship to the ISO/IEC OSI reference model

27.1.1.1 Repeater set

Repeater sets are an integral part of all 100 Mb/s baseband networks with more than two DTEs and are used to extend the physical system topology by providing a means of coupling two or more segments. Multiple repeater sets are permitted within a single collision domain to provide the maximum connection path length. Segments may be connected directly by a repeater or a pair of repeaters that are, in turn, connected by a inter-repeater link (IRL). Allowable topologies shall contain only one operative signal path between any two

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points on the network. A repeater set is not a station and does not count toward the overall limit of 1024 stations on a network.

A repeater set can receive, and if necessary decode, data from any segment under worst-case noise, timing, and signal amplitude conditions. It retransmits the data to all other segments attached to it with timing, amplitude, and, if necessary, coding restored. The retransmission of data occurs simultaneously with reception. If a collision occurs, the repeater set propagates the collision event throughout the network by transmitting a Jam signal. A repeater set also provides a degree of protection to a network by isolating a faulty segment's carrier activity from propagating through the network.

27.1.1.2 Repeater unit

A repeater unit is a subset of a repeater set containing all the repeater-specific components and functions, exclusive of PHY components and functions. A repeater unit connects to the PMA and, if necessary, the PCS sublayers of its PHYs.

27.1.1.3 Repeater classes

Two classes of repeater sets are defined—Class I and Class II.

Class I:

A type of repeater set specified such that in a maximum length segment topology, only one such repeater set may exist between any two DTEs within a single collision domain.

Class II:

A type of repeater set specified such that in a maximum length segment topology, only two such repeater sets may exist between any two DTEs within a single collision domain.

More complex topologies are possible in systems that do not use worst-case cable. See Clause 29 for requirements.

27.1.2 Application perspective

This subclause states the broad objectives and assumptions underlying the specification defined through Clause 27.

27.1.2.1 Objectives

a) Provide physical means for coupling two or more LAN segments at the Physical Layer.
b) Support interoperability of independently developed physical, electrical, and optical interfaces.
c) Provide a communication channel with a mean bit error ratio, at the physical service interface equivalent to that for the attached PHY.
d) Provide for ease of installation and service.
e) Ensure that fairness of DTE access is not compromised.
f) Provide for low-cost networks, as related to both equipment and cabling.
g) Make use of building wiring appropriate for the supported PHYs and telephony wiring practices.

27.1.2.2 Compatibility considerations

All implementations of the repeater set shall be compatible at the MDI. The repeater set is defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the repeater set in an application-dependent manner provided the appropriate PHY specifications are met.

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27.1.2.2.1 Internal segment compatibility

Implementations of the repeater set that contain a MAC layer for network management or other purposes, irrespective of whether they are connected through an exposed repeater port or are internally ported, shall conform to the requirements of Clause 30 on that port if repeater management is implemented.

27.1.3 Relationship to PHY

A close relationship exists between Clause 27 and the PHY clauses, Clause 23 for the 100BASE-T4 PHY and Clause 24 to Clause 26 for the 100BASE-X PHYs, and Clause 32 for the 100BASE-T2 PHY. The PHY's PMA, PCS, and MDI specifications provide the actual medium attachment, including drivers, receivers, and Medium Interface Connectors for the various supported media. The repeater clause does not define a new PHY; it utilizes the existing PHYs complete and without modification.

27.2 PMA interface messages

The messages between the repeater unit and the PMA in the PHY utilizes the PMA service interface defined in 23.3, 24.3, and 32.4.2. The PMA service interface primitives are summarized below:

PMA_TYPE.indication
PMA_UNITDATA.request
PMA_UNITDATA.indication
PMA_CARRIER.indication
PMA_LINK.indication
PMA_RXERROR.indication

27.3 Repeater functional specifications

A repeater set provides the means whereby data from any segment can be received under worst case noise, timing, and amplitude conditions and then retransmitted with timing and amplitude restored to all other attached segments. Retransmission of data occurs simultaneously with reception. If a collision occurs, the repeater set propagates the collision event throughout the network by transmitting a Jam signal. If an error is received by the repeater set, no attempt is made to correct it and it is propagated throughout the network by transmitting an invalid signal.

The repeater set provides the following functional capability to handle data flow between ports:

a) *Signal restoration.* Provides the ability to restore the timing and amplitude of the received signal prior to retransmission.
b) *Transmit function.* Provides the ability to output signals on the appropriate port and encoded appropriately for that port. Details of signal processing are described in the specifications for the PHYs.
c) *Receive function.* Provides the ability to receive input signals presented to the ports. Details of signal processing are described in the specifications for the PHYs.
d) *Data Handling function.* Provides the ability to transfer code-elements between ports in the absence of a collision.
e) *Received Event Handling requirement.* Provides the ability to derive a carrier signal from the input signals presented to the ports.
f) *Collision Handling function.* Provides the ability to detect the simultaneous reception of frames at two or more ports and then to propagate a Jam message to all connected ports.
g) *Error Handling function.* Provides the ability to prevent substandard links from generating streams of false carrier and interfering with other links.
h) *Partition function.* Provides the ability to prevent a malfunctioning port from generating an excessive number of consecutive collisions and indefinitely disrupting data transmission on the network.

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i) *Receive Jabber function.* Provides the ability to interrupt the reception of abnormally long streams of input data.

27.3.1 Repeater functions

The repeater set shall provide the Signal Restoration, Transmit, Receive, Data Handling, Received Event Handling, Collision Handling, Error Handling, Partition, and Receive Jabber functions. The repeater is transparent to all network acquisition activity and to all DTEs. The repeater will not alter the basic fairness criterion for all DTEs to access the network or weigh it toward any DTE or group of DTEs regardless of network location.

The Transmit and Receive functional requirements are specified by the PHY clauses, Clause 23 for 100BASE-T4, Clause 24 to Clause 26 for 100BASE-X, and Clause 32 for 100BASE-T2.

27.3.1.1 Signal restoration functional requirements

27.3.1.1.1 Signal amplification

The repeater set (including its integral PHYs) shall ensure that the amplitude characteristics of the signals at the MDI outputs of the repeater set are within the tolerances of the specification for the appropriate PHY type. Therefore, any loss of signal-to-noise ratio due to cable loss and noise pickup is regained at the output of the repeater set as long as the incoming data is within system specification.

27.3.1.1.2 Signal wave-shape restoration

The repeater set (including its integral PHYs) shall ensure that the wave-shape characteristics of the signals at the MDI outputs of a repeater set are within the specified tolerance for the appropriate PHY type. Therefore, any loss of wave-shape due to PHYs and media distortion is restored at the output of the repeater set.

27.3.1.1.3 Signal retiming

The repeater set (including its integral PHYs) shall ensure that the timing of the encoded data output at the MDI outputs of a repeater set are within the specified tolerance for the appropriate PHY type. Therefore, any receive jitter from the media is removed at the output of the repeater set.

27.3.1.2 Data handling functional requirements

27.3.1.2.1 Data frame forwarding

The repeater set shall ensure that the data frame received on a single input port is distributed to all other output ports in a manner appropriate for the PHY type of that port. The data frame is that portion of the packet after the SFD and before the end-of-frame delimiter. The only exceptions to this rule are when contention exists among any of the ports, when the receive port is partitioned as defined in 27.3.1.6, when the receive port is in the Jabber state as defined in 27.3.1.7, or when the receive port is in the Link Unstable state as defined in 27.3.1.5.1. Between unpartitioned ports, the rules for collision handling (see 27.3.1.4) take precedence.

27.3.1.2.2 Received code violations

The repeater set shall ensure that any code violations received while forwarding a packet are propagated to all outgoing segments. These code violations shall be forwarded as received or replaced by bad_code (see 23.2.1.2), /H/ (see 24.2.2.1), or (ESC/0, 0/ESC) (see Figure 32–9) code-groups, as appropriate for the outgoing PHY type. Once a received code violation has been replaced by the bad_code, /H/, or (ESC/0, 0/ESC) code-groups, this substitution shall continue for the remainder of the packet regardless of its content. The only exception to this rule is when contention exists among any of the ports, where the rules for collision handling (see 27.3.1.4) then take precedence.

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27.3.1.3 Received event handling functional requirements

27.3.1.3.1 Received event handling

For all its ports, the repeater set shall implement a function (scarrier_present) that represents a received event. Received events include both the Data Frame and any encapsulation of the Data Frame such as Preamble, SFD, and the code-groups /H/, /J/, /K/, bad_code, eop, /T/, /R/, SSD, ESD, etc. A received event is exclusive of the IDLE pattern. Upon detection of scarrier_present from one port, the repeater set repeats all received signals in the Data Frame from that port to the other port (or ports) as described in Figure 27–2.

27.3.1.3.2 Preamble regeneration

The repeater set shall output preamble as appropriate for the outgoing PHY type followed by the SFD.

27.3.1.3.3 Start-of-packet propagation delay

The start-of-packet propagation delay for a repeater set is the time delay between the start of the packet (see 24.6, 23.11.3, and 32.12.1) on its repeated-from (input) port to the start of the packet on its repeated-to (output) port (or ports). This parameter is referred to as the SOP delay. The maximum value of this delay is constrained by Table 27–2.

27.3.1.3.4 Start-of-packet variability

The start-of-packet variability for a repeater set is defined as the total worst-case difference between start-of-packet propagation delays for successive packets separated by 104 bit times (BT) or less at the same input port. The variability shall be less than or equal to those specified in Table 27–1.

Table 27–1—Start-of-packet variability

Input port type	Variability (BT)
100BASE-FX	7.0
100BASE-TX	7.0
100BASE-T4	8.0
100BASE-T2	8.0

27.3.1.4 Collision handling functional requirements

27.3.1.4.1 Collision detection

The repeater performs collision detection by monitoring all its enabled input ports for received events. When the repeater detects received events on more than one input port, it shall enter a collision state and transmit the Jam message to all of its output ports.

27.3.1.4.2 Jam generation

While a collision is occurring between any of its ports, the repeater unit shall transmit the Jam message to all of the PMAs to which it is connected. The Jam message shall be transmitted in accordance with the repeater state diagram in Figure 27–4 and Figure 27–5.

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27.3.1.4.3 Collision-jam propagation delay

The start-of-collision Jam propagation delay for a repeater set is the time delay between the start of the second packet input signals to arrive at its port and the start of Jam (see 24.6, 23.11, and 32.12.1) out on all ports. This parameter is referred to as the SOJ delay. The delay shall be constrained by Table 27–2. Note that a device defined by two columns in Table 27–2 has to meet the performance requirements specified in both columns.

Table 27–2—Start-of-packet propagation and start-of-collision jam propagation delays

Class I repeater	Class II repeater with all ports TX/FX	Class II repeater with any port T4	Class II repeater with any port T2
SOP + SOJ ≤ 140 BT	SOP ≤ 46 BT, SOJ ≤ 46 BT	SOP+SOJ ≤ 67 BT	SOP+SOJ ≤ 90 BT

27.3.1.4.4 Cessation-of-collision Jam propagation delay

The cessation-of-collision Jam propagation delay for a repeater set is the time delay between the end of the packet (see 24.6 and 23.11.3) that creates a state such that Jam should end at a port and the end of Jam (see 24.6 and 23.11.3) at that port. The states of the input signals that should cause Jam to end are covered in detail in the repeater state diagrams. This parameter is referred to as the EOJ delay. The delay shall be constrained by Table 27–3.

Table 27–3—Cessation-of-collision Jam propagation delay

Class I repeater	Class II repeater
EOJ ≤ SOP	EOJ ≤ SOP

27.3.1.5 Error handling functional requirements

27.3.1.5.1 100BASE-X and 100BASE-T2 carrier integrity functional requirements

In 100BASE-TX, 100BASE-FX, and 100BASE-T2 systems, it is desirable that the repeater set protect the network from some transient fault conditions that would disrupt network communications. Potential likely causes of such conditions are DTE and repeater power-up and power-down transients, cabling disconnects, and faulty wiring.

Each 100BASE-TX, 100BASE-FX, and 100BASE-T2 repeater PMA interface shall contain a self-interrupt capability, as described in Figure 27–9, to prevent a segment's spurious carrier activity from reaching the repeater unit and hence propagating through the network.

The repeater PMA interface shall count consecutive false carrier events. A false carrier event is defined as a carrier event that does not begin with a valid start of stream delimiter (see 24.2.2.1.4 and 32.3.1.2.3). The count shall be incremented on each false carrier event and shall be reset on reception of a valid carrier event. In addition, each PMA interface shall contain a false carrier timer, which is enabled at the beginning of a false carrier event and reset at the conclusion of such an event. A repeater unit shall transmit the JAM message to all of the PMAs to which it is connected for the duration of the false carrier event or until the duration of the event exceeds the time specified by the false_carrier_timer (see 27.3.2.1.4), whichever is shorter. The JAM message shall be transmitted in accordance with the Repeater state diagram in Figure 27–4 and Figure 27–5. The LINK UNSTABLE condition shall be detected when the False Carrier Count exceeds

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the value FCCLimit (see 27.3.2.1.1) or the duration of a false carrier event exceeds the time specified by the false_carrier_timer. In addition, the LINK UNSTABLE condition shall be detected upon power-up reset.

Upon detection of LINK UNSTABLE, the port shall perform the following:

a) Inhibit sending further messages to the repeater unit.
b) Inhibit sending further output messages from the repeater unit.
c) Continue to monitor activity on that PMA interface.

The repeater shall exit the LINK UNSTABLE condition when one of the following is met:

a1) The repeater has detected no activity (Idle) for more than the time specified by ipg_timer plus idle_timer (see 27.3.2.1.4) on Port X.
b1) A valid carrier event with a duration greater than the time specified by valid_carrier_timer (see 27.3.2.1.4) has been received, preceded by no activity (Idle) for more than the time specified by ipg_timer (see 27.3.2.1.4) on Port X.

27.3.1.5.2 Speed handling

If the PHY has the capability of detecting speeds other than 100 Mb/s, then the repeater set shall have the capability of blocking the flow of non-100 Mb/s signals. The incorporation of 100 Mb/s and 10 Mb/s repeater functionality within a single repeater set is beyond the scope of this standard.

27.3.1.6 Partition functional requirements

In large multisegment networks it may be desirable that the repeater set protect the network from some fault conditions that would disrupt network communications. A potentially likely cause of this condition could be due to a cable fault.

Each repeater PMA interface shall contain a self-interrupt capability, as described in Figure 27–8, to prevent a faulty segment's carrier activity from reaching the repeater unit and hence propagating through the network. The repeater PMA interface shall count collisions. The count shall be incremented on each transmission that suffers a collision. The count shall be reset on a carrier event of duration in excess of no_collision_timer (see 27.3.2.1.4) without incurring a collision. If this count reaches the value CCLimit (see 27.3.2.1.1), the Partition condition shall be detected.

Upon detection of Partition, the port shall perform the following:

a) Inhibit sending further input messages to the repeater unit.
b) Continue to output messages from the repeater unit.
c) Continue to monitor activity on that PMA interface.

The repeater shall reset the Partition function when one of the following conditions is met:

a1) On power-up reset.
b1) The repeater has transmitted on the port for a duration in excess of no_collision_timer (see 27.3.2.1.4) without incurring a collision.

NOTE—It is possible that under some network conditions the partition state diagram will partition a port due to normal network collisions rather than a fault condition. It is also possible that some double fault conditions will remain undetected. To reduce the likelihood of these events occurring, the following optional measures, as described in Figure 27–8, are recommended:

a2) The collision count is additionally reset when the repeater has transmitted on the port for a duration in excess of no_collision_timer without detecting a collision.

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b2) The Partition function is additionally reset when the repeater has received activity on the port for a duration in excess of no_collision_timer without detecting a collision.
c2) The Partition condition is additionally detected due to a carrier event of duration in excess of jabber_timer (see 27.3.1.7) in which a collision has occurred.

27.3.1.7 Receive jabber functional requirements

Each repeater PMA interface shall contain a self-interrupt capability, as described in Figure 27–7, to prevent an illegally long reception of data from reaching the repeater unit. The repeater PMA interface shall provide a window of duration jabber_timer bit times (see 27.3.2.1.4) during which the input messages may be passed on to other repeater unit functions. If a reception exceeds this duration, the jabber condition shall be detected.

Upon detection of jabber, the port shall perform the following:

a) Inhibit sending further input messages to the repeater unit.
b) Inhibit sending further output messages from the repeater unit.

The repeater PMA interface shall reset the Jabber function and re-enable data transmission and reception when either one of the following conditions is met:

a1) On power-up reset.
b1) When carrier is no longer detected.

27.3.2 Detailed repeater functions and state diagrams

A precise algorithmic definition is given in this subclause, providing a complete procedural model for the operation of a repeater, in the form of state diagrams. Note that whenever there is any apparent ambiguity concerning the definition of repeater operation, the state diagrams should be consulted for the definitive statement.

The model presented in this subclause is intended as a primary specification of the functions to be provided by any repeater unit. It is important to distinguish, however, between the model and a real implementation. The model is optimized for simplicity and clarity of presentation, while any realistic implementation should place heavier emphasis on such constraints as efficiency and suitability to a particular implementation technology.

It is the functional behavior of any repeater unit implementation that shall match the standard, not the internal structure. The internal details of the procedural model are useful only to the extent that they help specify the external behavior clearly and precisely. For example, the model uses a separate Receive Port Jabber state diagram for each port. However, in actual implementation, the hardware may be shared.

The notation used in the state diagram follows the conventions of 1.2.1. Note that transitions shown without source states are evaluated at the completion of every state and take precedence over other transition conditions.

27.3.2.1 State diagram variables

27.3.2.1.1 Constants

CCLimit

The number of consecutive collisions that have to occur before a segment is partitioned.

Values: Positive integer greater than 60.

FCCLimit

The number of consecutive False Carrier events that have to occur before a segment is isolated.

Value: 2.

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27.3.2.1.2 Variables

activity(Port designation)

Indicates port activity status. The repeater core effects a summation of this variable received from all its attached ports and responds accordingly.

Values: 0; no frame or packet activity at any port.
1; exactly 1 port of the repeater set has frame or packet activity input.
>1; more than 1 port of the repeater set has frame or packet activity input. Alternately, one or more ports has detected a carrier that is not valid.

all_data_sent

Indicates if all received data frame bits or code-groups from the current frame have been sent. During or after collision the all_data_sent variable follows the inverse of the carrier of port N.

Values: true; all received data frame bits or code-groups have been sent.
false; all received data frame bits or code-groups have not been sent.

begin

The Interprocess flag controlling state diagram initialization values.

Values: true
false

carrier_status(X)

Signal received from PMA; indicates the status of sourced Carrier input at Port X.

Values: ON; the carrier_status parameter of the PMA_CARRIER.indication primitive for Port X is ON.
OFF; the carrier_status parameter of the PMA_CARRIER.indication primitive for Port X is OFF.

data_ready

Indicates if the repeater has detected and/or decoded the MAC SFD and is ready to send the received data.

Values: true; the MAC SFD has been detected and/or decoded.
false; the MAC SFD has not been detected nor decoded.

force_jam(X)

Flag from Carrier Integrity state diagram for Port X, which determines whether all ports should transmit Jam.

Values: true; the Carrier Integrity Monitor has determined that it requires all ports be forced to transmit Jam.
false; the Carrier Integrity Monitor has determined that it does not require all ports be forced to transmit Jam.

Default: for T4 ports: false

isolate(X)

Flag from Carrier Integrity state diagram for Port X, which determines whether a port should be enabled or disabled.

Values: true; the Carrier Integrity Monitor has determined the port should be disabled.
false; the Carrier Integrity Monitor has determined the port should be enabled.

jabber(X)

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Flag from Receive Timer state diagram for Port X, which indicates that the port has received excessive length activity.

Values: true; port has exceeded the continuous activity limit.
false; port has not exceeded the continuous activity limit.

link_status(X)

Signal received from PMA; indicates link status for Port X (see 23.3.5, 24.3.1.5, and 32.4.1.3.1).

Values: OK; the link_status parameter of the PMA_LINK.indication primitive for Port X is OK.
READY; the link_status parameter of the PMA_LINK.indication primitive for Port X is READY (for 100BASE-TX and 100BASE-T4).
FAIL; the link_status parameter of the PMA_LINK.indication primitive for Port X is FAIL.

opt(X)

Implementation option. Either value may be chosen for repeater implementation.

Values: true; port will emit the JamT4 pattern in response to collision conditions.
false; port will append Jam pattern after preamble and SFD in response to collision conditions.

OUT(X)

Type of output repeater is sourcing at Port X.

Values: Idle; repeater is transmitting an IDLE pattern as described by 23.4.1.2, 24.2.2.1.2, or 32.3.1.2.3.
In(N); repeater is transmitting rx_code_bit(s) as received from Port (N) except /J/K/ (see 24.3.4.2), or recoded rx_symbol_vector as received from Port (N) except SSD (see 32.3.5.2).
Pream; repeater is sourcing preamble pattern as defined by the PMA or PCS of the port type (see 23.2.1.2, 24.2.2.2, 32.3.1.2, Figure 23–6 and Figure 24–9.)
Data; repeater is transmitting data frame on Port X. This data represents the original MAC source data field, properly encoded for the PHY type (see 23.2.1.2, 24.2.2.2, and 32.3.1.2.3).
Jam; repeater is sourcing well formed arbitrary data encodings, excluding SFD, to the port PMA.
JamX; repeater is sourcing a pattern representing 010101... repetitively on Port X.
JamT4; repeater is sourcing the pattern +-+-... repetitively on Port X.

JamT2; repeater is sending a pattern representing 010101... repetitively on Port X.
SFD; repeater is sourcing the Start Frame Delimiter on Port X encoded as defined by the appropriate PHY (see 23.2.3, Figure 24–9, and 32.3.1.2).
/J/K/; repeater is sourcing the code-groups /J/K/ as defined by the PMA on Port X (see 24.2.2.1.4).
/T/R/; repeater is sourcing the code-groups /T/R/ as defined by the PMA on Port X (see 24.2.2.1.5).

SSD; repeater is sourcing the code-groups SSD as defined by the PMA on Port X (see 32.4.2.5).

ESD; repeater is sourcing the code-groups ESD as defined by the PMA on Port X (see 32.3.1.2.3).
DF; repeater is sourcing the Data Frame of the packet on Port X. These are code elements originating on Port N exclusive of EOP1-5, SOSA and SOSB (see 23.2.3 and 23.2.4).
EOP; repeater is sourcing end of packet delimiter (EOP1-5) as defined by the appropriate PMA on Port X (see 23.2.1.2 and 23.2.4.1).

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bad_code; repeater is sourcing bad_code as defined by the PMA of the transmit port (see 23.2.4.1).
tx_err; repeater is sourcing a transmit error code element, either bad_code (see 23.2.4.1) or the code-group /H/ (see 24.2.2.1), or (ESC/0, 0/ESC) (see Figure 32–12) as appropriate to the outgoing PHY type.

partition(X)

Flag from Partition state diagram for Port X, which determines whether a port receive path should be enabled or disabled.

Values: true; port has exceeded the consecutive collision limit.
false; port has not exceeded the consecutive collision limit.

part_opt(X)

Implementation option. Either value may be chosen for repeater implementation (see 27.3.1.6).

Values: true; port supports the recommended optional measures in the partition state diagram.
false; port does not support the recommended optional measures in the partition state diagram.

rxerror_status(X)

Signal received from PMA; indicates if Port X has detected an error condition from the PMA (see 23.3.7.1, Figure 24–14, and Figure 32–14).The repeater need not propagate this error condition during collision events.

Values: ERROR; the rxerror_status parameter of the PMA_RXERROR.indication primitive for Port X is ERROR.
NO_ERROR; the rxerror_status parameter of the PMA_RXERROR.indication primitive for Port X is NO_ERROR.

RX_ER(X)

Signal received from PCS; indicates if Port X has detected an error condition from the PCS (see 23.2.1.4, 24.2.3.2, 32.3.4.1, Figure 23–10, Figure 24–15, and Figure 32–13). The repeater need not propagate this error condition during collision events.

Values: true; the PCS RX_ER signal for Port X is asserted.
false; the PCS RX_ER signal for Port X is negated.

scarrier_present(X)

Signal received from PMA; indicates the status of sourced Carrier input at Port X.

Values: true; the carrier_status parameter of the PMA_CARRIER.indication primitive for Port X is ON.
false; the carrier_status parameter of the PMA_CARRIER.indication primitive for Port X is OFF.

source_type(X)

Signal received from PMA; indicates PMA type for Port X. The first port to assert activity maintains the source type status for all transmitting port(s) until activity is deasserted. Repeaters may optionally force nonequality on comparisons using this variable. It has to then follow the behavior of the state diagrams accordingly and meet all the delay parameters as applicable for the real implemented port type(s).

Values: FXTX; the pma_type parameter of the PMA_TYPE.indication primitive for Port X is X.
T4; the pma_type parameter of the PMA_TYPE.indication primitive for Port X is T4.
T2; the pma_type parameter of the PMA_TYPE.indication primitive for Port X is T2.

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27.3.2.1.3 Functions

command(X)

A function that passes an inter-process flag to all ports specified by X.

Values: copy; indicates that the repeater core has summed the activity levels of its active ports and is in the ACTIVE state.
collision; indicates that the repeater core has summed the activity levels of its active ports and is in the JAM state.
quiet; indicates that the repeater core has summed the activity levels of its active ports and is in the IDLE state.

port(Test)

A function that returns the designation of a port passing the test condition. For example, port(activity = scarrier_present) returns the designation: X for a port for which scarrier_present = true. If multiple ports meet the test condition, the Port function will be assigned one and only one of the acceptable values.

27.3.2.1.4 Timers

All timers operate in the same fashion. A timer is reset and starts timing upon entering a state where "start x_timer" is asserted. At time "x" after the timer has been started, "x_timer_done" is asserted and remains asserted until the timer is reset. At all other times, "x_timer_not_done" is asserted.

When entering a state where "start x_timer" is asserted, the timer is reset and restarted even if the entered state is the same as the exited state.

The timers used in the repeater state diagrams are defined as follows:

false_carrier_timer

Timer for length of false carrier (27.3.1.5.1) that has to be present before the ISOLATION state is entered. The timer is done when it reaches 450 – 500 BT.

idle_timer

Timer for length of time without carrier activity that has to be present before the ISOLATION state is exited (27.3.1.5.1). The timer is done when it reaches 33 000 BT ± 25% BT.

ipg_timer

Timer for length of time without carrier activity that has to be present before carrier integrity tests (27.3.1.5.1) are re-enabled. The timer is done when it reaches 64 – 86 BT.

jabber_timer

Timer for length of carrier that has to be present before the Jabber state (27.3.1.7), and optionally during a collision the Partition state (27.3.1.6), is entered. The timer is done when it reaches 40 000 – 75 000 BT.

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no_collision_timer

Timer for length of packet without collision before the Partition state is exited (27.3.1.6). The timer is done when it reaches 450 – 560 BT.

valid_carrier_timer

Timer for length of valid carrier that has to be present before the Isolation state is exited (27.3.1.5.1). The timer is done when it reaches 450 – 500 BT.

27.3.2.1.5 Counters

CC(X)

Consecutive port collision count for Port X. Partitioning occurs on a terminal count of CCLimit being reached.

Values: Non-negative integers up to a terminal count of CCLimit.

FCC(X)

False Carrier Counter for Port X. Isolation occurs on a terminal count of FCCLimit being reached.

Values: Non-negative integers up to a terminal count of FCCLimit.

27.3.2.1.6 Port designation

Ports are referred to by number. Port information is obtained by replacing the X in the desired function with the number of the port of interest. Ports are referred to in general as follows:

X

Generic port designator. When X is used in a state diagram, its value is local to that diagram and not global to the set of state diagrams.

N

Is defined by the Port function on exiting the IDLE or JAM states of Figure 27–2. It indicates a port that caused the exit from these states.

ALL

Indicates all repeater ports are to be considered. All ports shall meet test conditions in order for the test to pass.

ALLXN

Indicates all ports except N should be considered. All ports considered shall meet the test conditions in order for the test to pass.

ANY

Indicates all ports are to be considered. One or more ports shall meet the test conditions in order for the test to pass.

ANYXN

Indicates any port other than N meeting the test conditions shall cause the test to pass.

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27.3.2.2 State diagrams

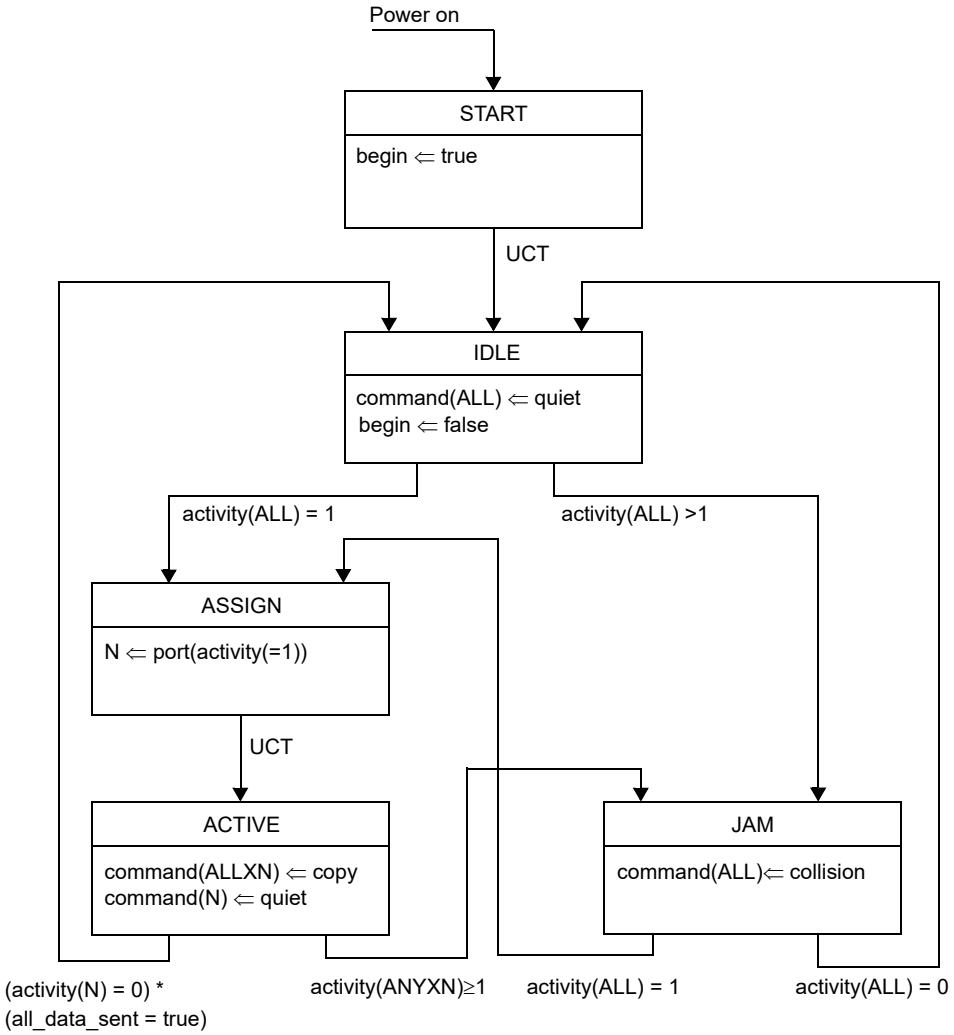

Figure 27–2—Repeater Core state diagram

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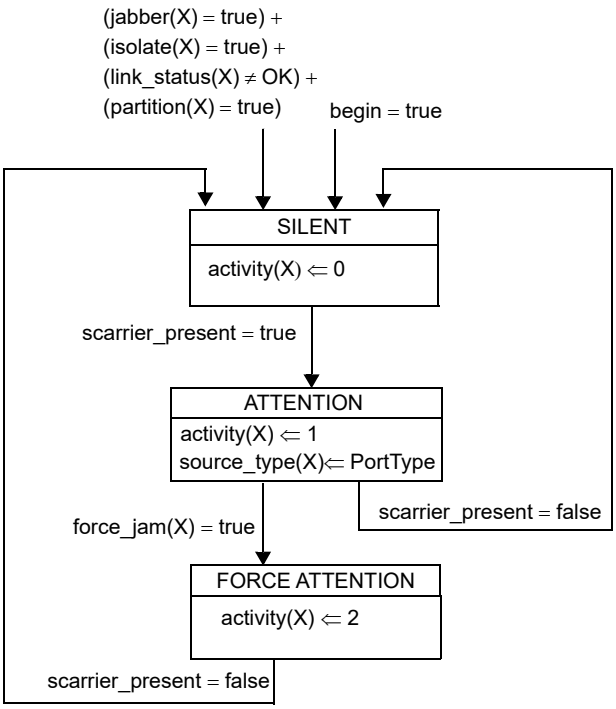

Figure 27–3—Receive state diagram for Port X

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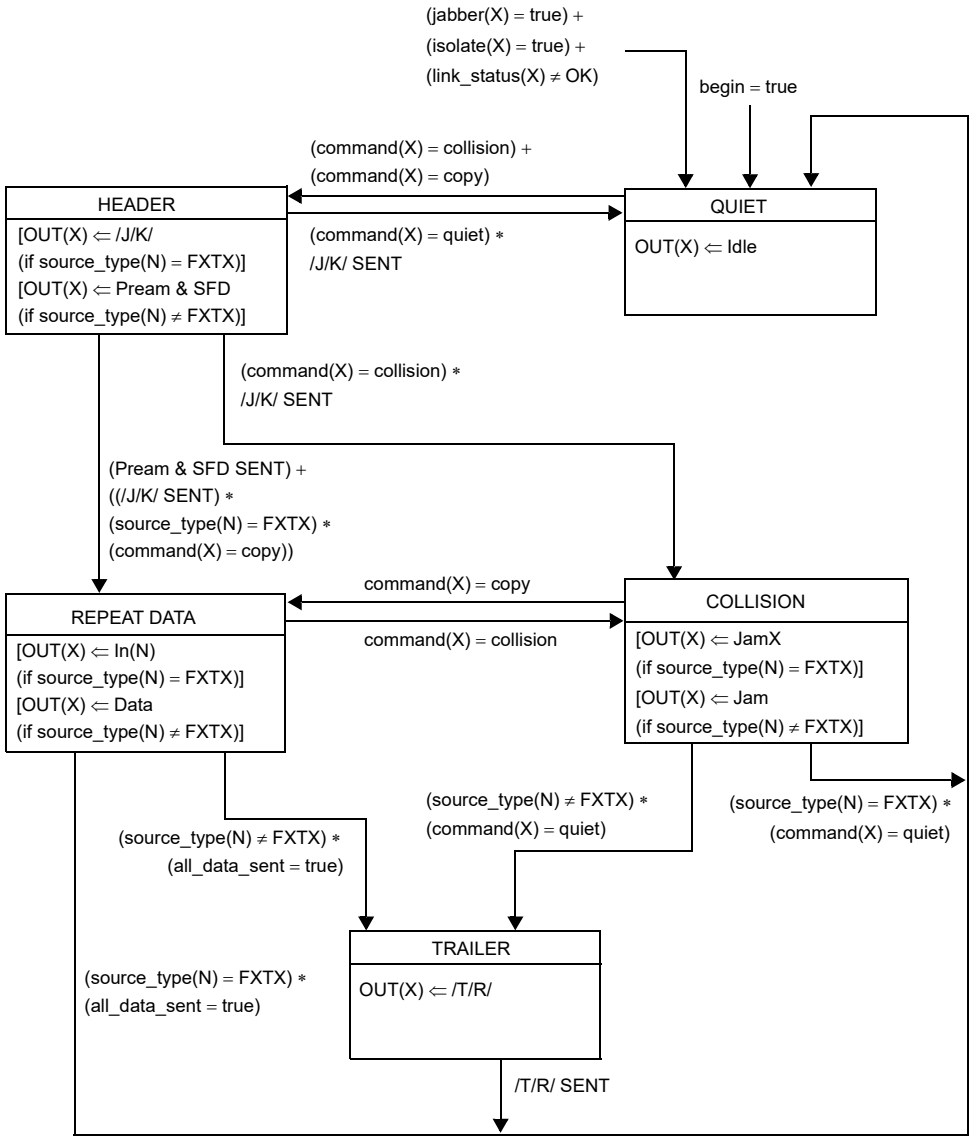

Figure 27–4—100BASE-TX and 100BASE-FX Transmit state diagram for Port X

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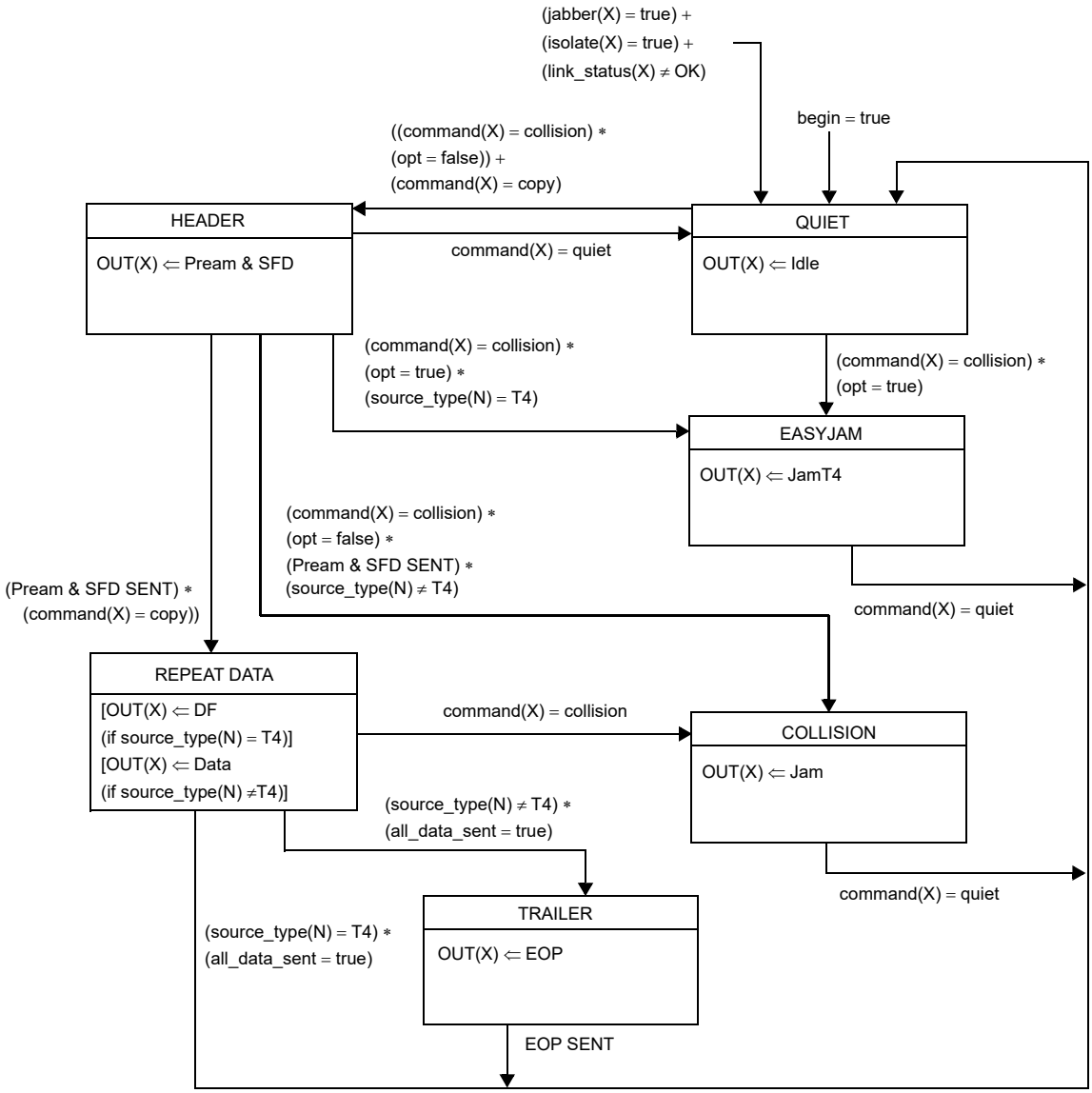

Figure 27–5—100BASE-T4 Transmit state diagram for Port X

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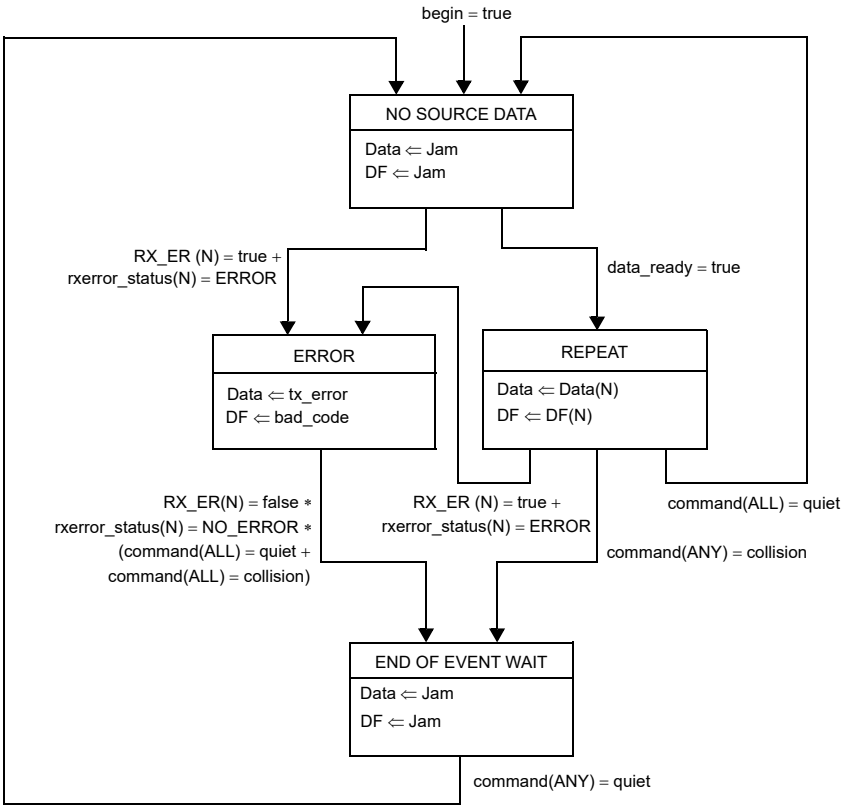

Figure 27–6—Repeater Data Handler state diagram

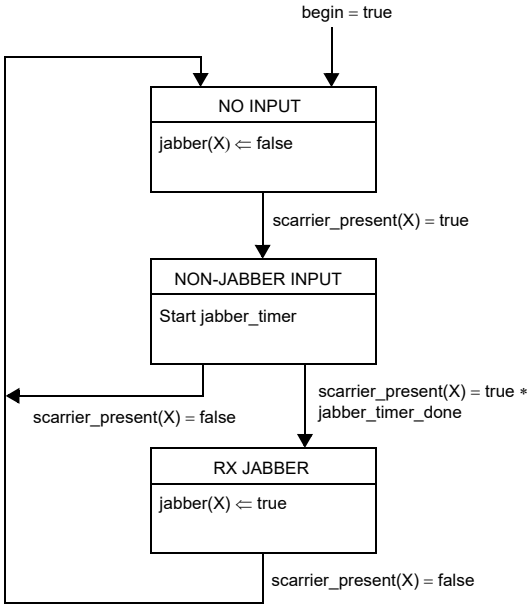

Figure 27–7—Receive Timer state diagram for Port X

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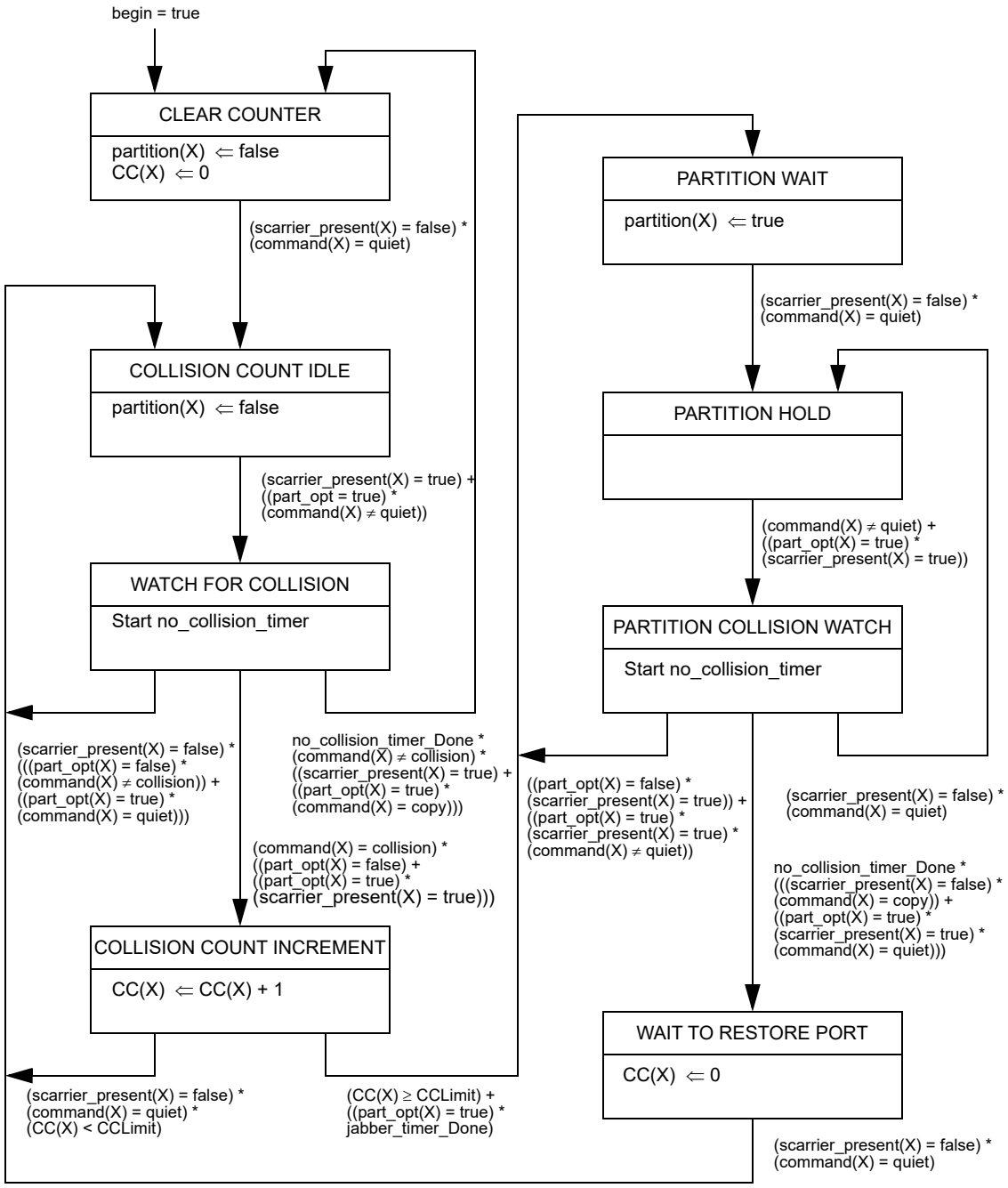

Figure 27–8—Partition state diagram for Port X

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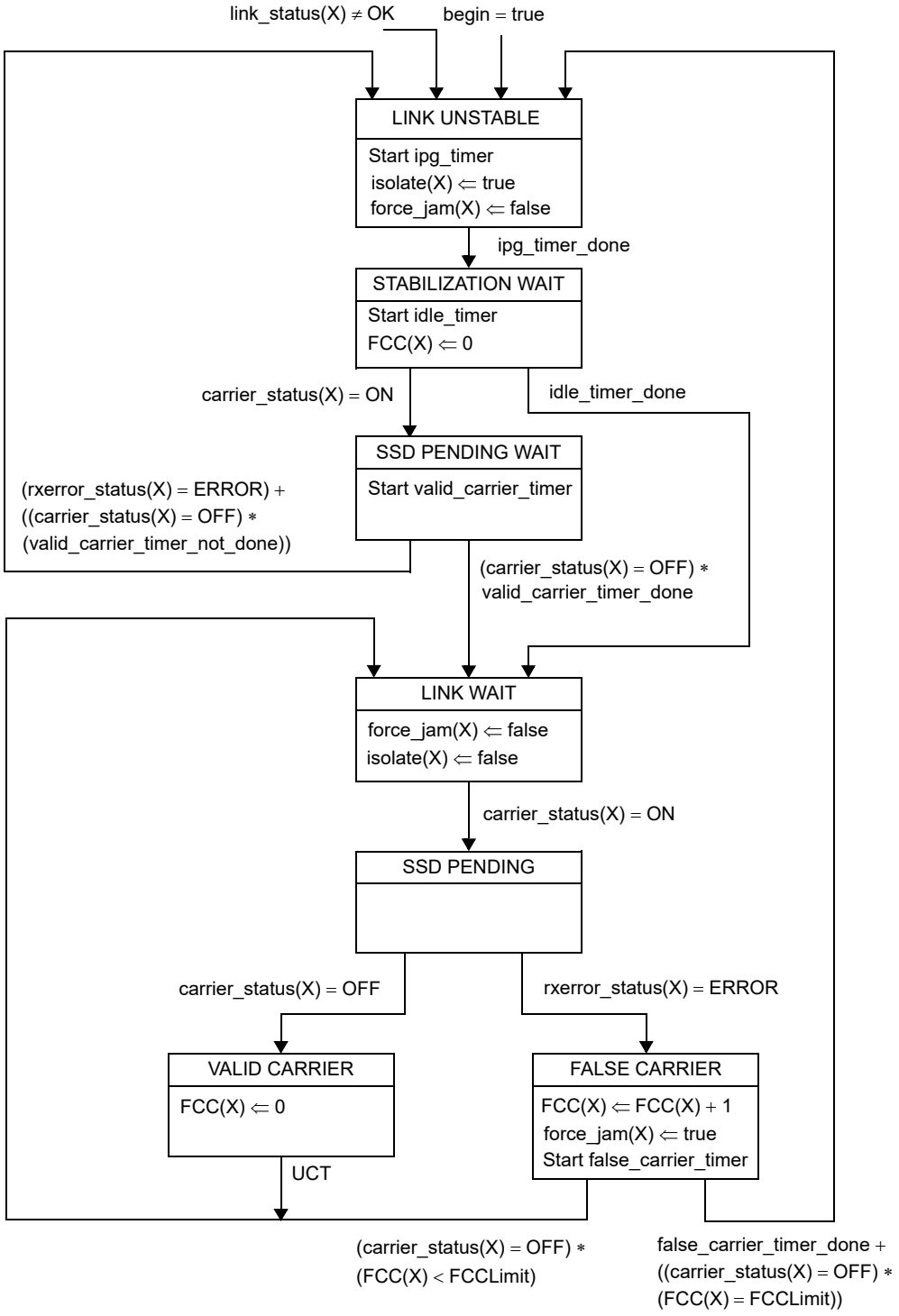

Figure 27–9—100BASE-X/T2 Carrier Integrity Monitor state diagram for Port X

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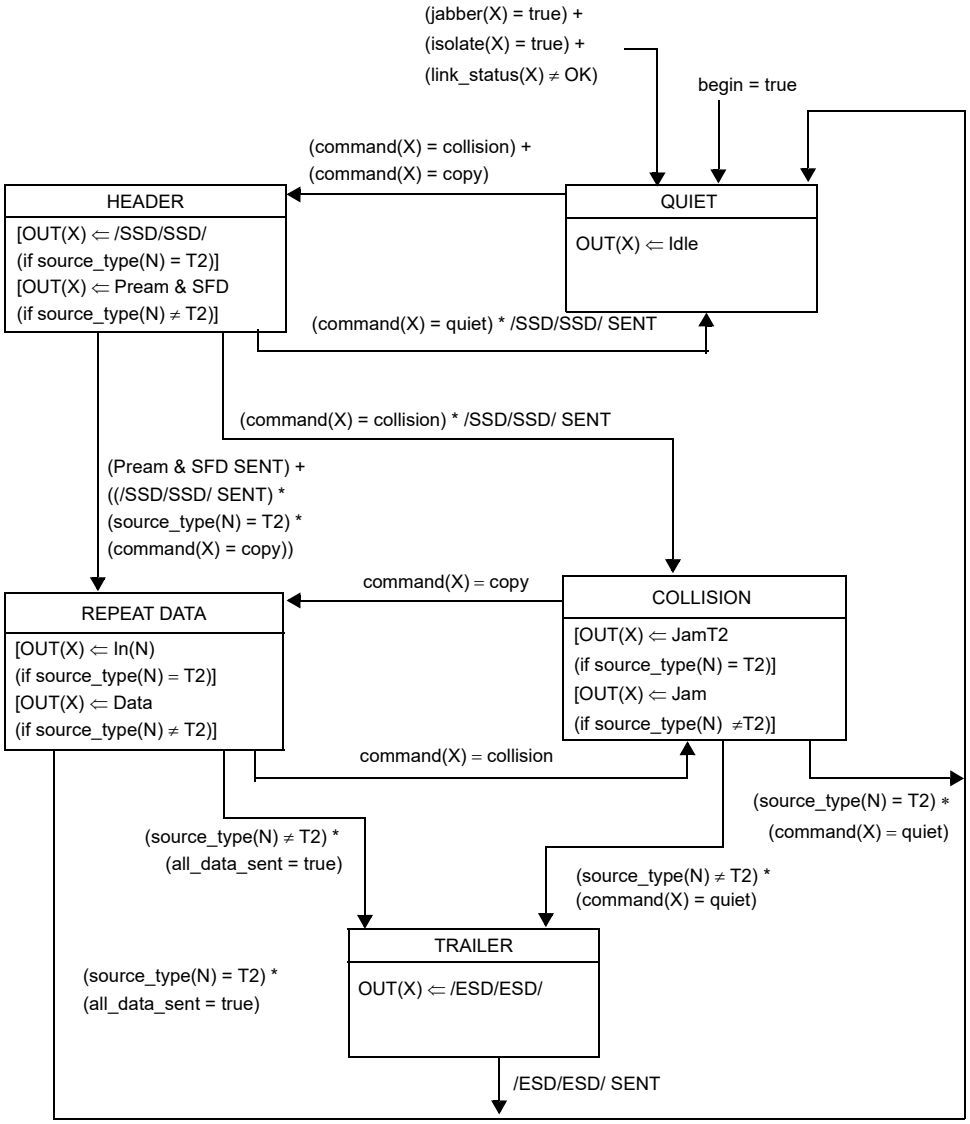

Figure 27–10—100BASE-T2 Transmit state diagram for Port X

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27.4 Repeater electrical specifications

27.4.1 Electrical isolation

Network segments that have different isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of the repeater set.

27.5 Environmental specifications

27.5.1 General safety

NOTE—Since September 2011, maintenance changes are no longer being considered for this clause. Since February 2021, safety information is in J.2.

All equipment meeting this standard shall conform to IEC 60950-1.

27.5.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cables and components.
c) High-energy transients coupled onto the LAN cable system.
d) Voltage potential differences between safety grounds to which the various LAN components are connected.

Such electrical safety hazards have to be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures have to be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network. Isolation requirements are defined in 27.5.3.

27.5.2.1 Installation

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

27.5.2.2 Grounding

The safety ground, or chassis ground for the repeater set, shall be provided through the main ac power cord via the third wire ground as defined by applicable local codes and regulations. It is recommended that an external PHY to the repeater should also be mechanically grounded to the repeater unit through the power and ground signals in the MII connection and via the metal shell and shield of the MII connector if available.

If the MDI connector should provide a shield connection, the shield may be connected to the repeater safety ground. A network segment connected to the repeater set through the MDI may use a shield. If both ends of the network segment have a shielded MDI connector available, then the shield may be grounded at both ends according to local regulations and ISO/IEC 11801:1995, and as long as the ground potential difference

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between both ends of the network segment is less than 1 V rms. The same rules apply towards an inter-repeater link between two repeaters. Multiple repeaters should reside on the same power main; if not, then it is highly recommended that the repeaters be connected via fiber.

WARNING

It is assumed that the equipment to which the repeater is attached is properly grounded and not left floating nor serviced by a "doubly insulated ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety, are beyond the scope of this standard.

27.5.2.3 Installation and maintenance guidelines

During installation and maintenance of the cable plant, care should be taken to ensure that uninsulated network cable connectors do not make electrical contact with unintended conductors or ground.

27.5.3 Electrical isolation

There are two electrical power distribution environments to be considered that require different electrical isolation properties:

a) *Environment A.* When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.
b) *Environment B.* When a LAN crosses the boundary between separate power distribution systems or the boundary of a single building.

27.5.3.1 Environment A requirements

Attachment of network segments via repeater sets requires electrical isolation of 500 V rms, one-minute withstand, between the segment and the protective ground of the repeater unit.

27.5.3.2 Environment B requirements

The attachment of network segments that cross Environment B boundaries requires electrical isolation of 1500 V rms, one-minute withstand, between each segment and all other attached segments and also the protective ground of the repeater unit.

The requirements for interconnected electrically conducting LAN segments that are partially or fully external to a single building environment may require additional protection against lightning strike hazards. Such requirements are beyond the scope of this standard. It is recommended that the above situation be handled by the use of nonelectrically conducting segments (e.g., fiber optic).

It is assumed that any nonelectrically conducting segments will provide sufficient isolation within that media to satisfy the isolation requirements of Environment B.

27.5.4 Reliability

A two-port repeater set shall be designed to provide a mean time between failure (MTBF) of at least 50 000 hours of continuous operation without causing a communications failure among stations attached to the network medium. Repeater sets with more than two ports shall add no more than 3.46×10^{-6} failures per hour for each additional port.

The repeater set electronics should be designed to minimize the probability of component failures within the repeater electronics that prevent communications among other PHYs on the individual segments. Connec-

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tors and other passive components comprising the means of connecting the repeater to the cable should be designed to minimize the probability of total network failure.

27.5.5 Environment

27.5.5.1 Electromagnetic emission

The repeater shall comply with applicable local and national codes for the limitation of electromagnetic interference.

27.5.5.2 Temperature and humidity

The repeater is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the repeater the operating environmental conditions to facilitate selection, installation, and maintenance.

27.6 Repeater labeling

It is required that each repeater (and supporting documentation) shall be labeled in a manner visible to the user with these parameters:

a) Crossover ports appropriate to the respective PHY should be marked with an X.
b) The repeater set class type should be labeled in the following manner:
    1) Class I: a Roman numeral “I” centered within a circle.
    2) Class II: a Roman numeral “II” centered within a circle.

Additionally, it is recommended that each repeater (and supporting documentation) also be labeled in a manner visible to the user with at least these parameters:

c) Data rate capability in Mb/s
d) Any applicable safety warnings
e) Port type, i.e., 100BASE-TX, 100BASE-T4, or 100BASE-T2
f) Worst-case bit time delays between any two ports appropriate for
    1) Start-of-packet propagation delay
    2) Start-of-collision Jam propagation delay
    3) Cessation-of-collision Jam propagation delay

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27.7 Protocol implementation conformance statement (PICS) proforma for Clause 27, Repeater for 100 Mb/s baseband networks[62]

27.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 27, Repeater for 100 Mb/s baseband networks, shall complete the following protocol implementation conformance statement (PICS) proforma.

27.7.2 Identification

27.7.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

27.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2018, Clause 27, Repeater for 100 Mb/s baseband networks
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2018.)	

Date of Statement	

[62] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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27.7.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*FXP	Repeater supports 100BASE-FX connections	27.1.2.2	O		
*TXP	Repeater supports 100BASE-TX connections	27.1.2.2	O		
*T4P	Repeater supports 100BASE-T4 connections	27.1.2.2	O		
*T2P	Repeater supports 100BASE-T2 connections	27.1.2.2	O		
*CLI	Repeater meets Class I delays	27.1.1.3	O		
*CLII	Repeater meets Class II delays	27.1.1.3	O		
*PHYS	PHYs capable of detecting non 100BASE-T signals	27.3.1.5.2	O		
*OPF	Partition function supports the recommended optional measures as described	27.3.1.6	O		

In addition, the following predicate name is defined for use when different implementations from the set above have common parameters:

*XP:FXP or TXP

27.7.4 PICS proforma tables for the repeater for 100 Mb/s baseband networks

27.7.4.1 Compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
CC1	100BASE-FX port compatible at the MDI	27.1.2.2	FXP:M		
CC2	100BASE-TX port compatible at the MDI	27.1.2.2	TXP:M		
CC3	100BASE-T4 port compatible at the MDI	27.1.2.2	T4P:M		
CC4	Internal segment compatibility	27.1.2.2.1	M		Internal port meets Clause 30 when repeater management implemented
CC5	100BASE-T2 port compatible at the MDI	27.1.2.2	T2P:M		

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27.7.4.2 Repeater functions

Item	Feature	Subclause	Status	Support	Value/Comment
RF1	Signal Restoration	27.3.1	M		
RF2	Data Handling	27.3.1	M		
RF3	Received Event Handling	27.3.1	M		
RF4	Collision Handling	27.3.1	M		
RF5	Error Handling	27.3.1	M		
RF6	Partition	27.3.1	M		
RF7	Received Jabber	27.3.1	M		

27.7.4.3 Signal Restoration function

Item	Feature	Subclause	Status	Support	Value/Comment
SR1	Output amplitude as required by 100BASE-FX	27.3.1.1.1	FXP:M		
SR2	Output amplitude as required by 100BASE-TX	27.3.1.1.1	TXP:M		
SR3	Output amplitude as required by 100BASE-T4	27.3.1.1.1	T4P:M		
SR4	Output signal wave-shape as required by 100BASE-FX	27.3.1.1.2	FXP:M		
SR5	Output signal wave-shape as required by 100BASE-TX	27.3.1.1.2	TXP:M		
SR6	Output signal wave-shape as required by 100BASE-T4	27.3.1.1.2	T4P:M		
SR7	Output data timing as required by 100BASE-FX	27.3.1.1.3	FXP:M		
SR8	Output data timing as required by 100BASE-TX	27.3.1.1.3	TXP:M		
SR9	Output data timing as required by 100BASE-T4	27.3.1.1.3	T4P:M		
SR10	Output amplitude as required by 100BASE-T2	27.3.1.1.1	T2P:M		
SR11	Output signal wave-shape as required by 100BASE-T2	27.3.1.1.2	T2P:M		
SR12	Output data timing as required by 100BASE-T2	27.3.1.1.3	T2P:M		

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27.7.4.4 Data Handling function

Item	Feature	Subclause	Status	Support	Value/Comment
DH1	Data frames forwarded to all ports except receiving port	27.3.1.2.1	M		
DH2	Data frames transmitted as appropriate for 100BASE-FX	27.3.1.2.1	FXP:M		
DH3	Data frames transmitted as appropriate for 100BASE-TX	27.3.1.2.1	TXP:M		
DH4	Data frames transmitted as appropriate for 100BASE-T4	27.3.1.2.1	T4P:M		
DH5	Code Violations forwarded to all transmitting ports	27.3.1.2.2	M		
DH6	Code Violations forwarded as received	27.3.1.2.2	O.1		
DH7	Received Code Violation forwarded as /H/ or as received	27.3.1.2.2	XP:O.1		
DH8	Received Code Violation forwarded as bad_code or as received	27.3.1.2.2	T4P:O.1		
DH9	Code element substitution for remainder of packet after received Code Violation	27.3.1.2.2	M		
DH10	Data frames transmitted as appropriate for 100BASE-T2	27.3.1.2.1	T2P:M		

27.7.4.5 Receive Event Handling function

Item	Feature	Subclause	Status	Support	Value/Comment
RE1	scarrier_present detect implemented	27.3.1.3.1	M		
RE2	Repeat all received signals	27.3.1.3.1	M		
RE3	Preamble encoded as required by 100BASE-FX	27.3.1.3.2	FXP:M		
RE4	Preamble encoded as required by 100BASE-TX	27.3.1.3.2	TXP:M		
RE5	Preamble encoded as required by 100BASE-T4	27.3.1.3.2	T4P:M		
RE6	Start-of-packet propagation delay, Class I repeater	27.3.1.3.3	CLI:M		
RE7	Start-of-packet propagation delay, Class II repeater	27.3.1.3.3	CLII:M		
RE8	Start-of-packet variability for 100BASE-FX input port	27.3.1.3.4	FXP:M		7.0 BT

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27.7.4.5 Receive Event Handling function *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
RE8	Start-of-packet variability for 100BASE-TX input port	27.3.1.3.4	TXP:M		7.0 BT
RE9	Start-of-packet variability for 100BASE-T4 input port	27.3.1.3.4	T4P:M		8.0 BT
RE10	Preamble encoded as required by 100BASE-T2	27.3.1.3.2	T2P:M		
RE11	Start of packet variability for 100BASE-T2 input port	27.3.1.3.4	T2P:M		8.0 BT

27.7.4.6 Collision Handling function

Item	Feature	Subclause	Status	Support	Value/Comment
CO1	Collision detection	27.3.1.4.1	M		Receive event on more than one port
CO2	Jam generation	27.3.1.4.2	M		Transmit Jam message while collision is detected
CO3	Collision-jam propagation delay, Class I repeater	27.3.1.4.3	CLI:M		SOP + SOJ ≤ 140 BT
CO4	Collision-jam propagation delay, Class II repeater with any port T4	27.3.1.4.3	CLII:M		SOP + SOJ ≤ 67 BT
CO5	Collision-jam propagation delay, Class II repeater, all TX/FX ports	27.3.1.4.3	CLII:M		SOP ≤ 46, SOJ ≤ 46 BT
CO6	Cessation of collision propagation delay, Class I repeater	27.3.1.4.4	CLI:M		EOJ ≤ SOP
CO7	Cessation of collision propagation delay, Class II repeater	27.3.1.4.4	CLII:M		EOJ ≤ SOP
CO8	Collision-jam propagation delay, Class II repeater with any port T2	27.3.1.4.3	CLII * T2P:M		SOP + SOJ ≤ 90 BT

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27.7.4.7 Error Handling function

Item	Feature	Subclause	Status	Support	Value/Comment
EH1	Carrier Integrity function implementation	27.3.1.5.1	XP:M		Self-interrupt of data reception
EH2	False carrier count for Link Unstable detection	27.3.1.5.1	XP:M		False carrier count in excess of FCCLimit
EH3	False carrier count reset	27.3.1.5.1	XP:M		Count reset on valid carrier
EH4	False carrier timer for Link Unstable detection	27.3.1.5.1	XP:M		False carrier of length in excess of false_carrier_timer
EH5	Jam message duration	27.3.1.5.1	XP:M		Equals duration of false carrier event, but not greater than duration of false_carrier_timer
EH6	Link Unstable detection	27.3.1.5.1	XP:M		False Carrier count exceed FCCLimit or False carrier exceeds the false_carrier_timer or power-up reset
EH7	Messages sent to repeater unit in Link Unstable state	27.3.1.5.1	XP:M		Inhibited sending messages to repeater unit
EH8	Messages sent from repeater unit in Link Unstable state	27.3.1.5.1	XP:M		Inhibited sending output messages
EH9	Monitoring activity on PMA interface in Link Unstable state	27.3.1.5.1	XP:M		Continue monitoring activity at PMA interface
EH10	Reset of Link Unstable state	27.3.1.5.1	XP:M		No activity for more than ipg_timer plus idle_timer or Valid carrier event of duration greater than valid_carrier_timer preceded by Idle of duration greater than ipg_timer
EH11	Block flow of non-100 Mb/s signals	27.3.1.5.2	PHYS:M		

27.7.4.8 Partition functions

Item	Feature	Subclause	Status	Support	Value/Comment
PA1	Partition function implementation	27.3.1.6	M		Self-interrupt of data reception
PA2	Collision count for entry into partition state	27.3.1.6	M		Collision count greater than or equal to CCLimit
PA3	Collision counter incrementing	27.3.1.6	M		Count incremented on a collision
PA4	*Collision counter reset*	*27.3.1.6*	*M*		*Count reset on receive activity in excess of no_collision_timer without collision*

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27.7.4.8 Partition functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PA5			OPF:M		Count reset on transmission in excess of no_collision_timer without collision
PA6	Messages sent to repeater unit in Partition state	27.3.1.6	M		Inhibited sending messages to repeater unit
PA7	Messages sent from repeater unit in Partition state	27.3.1.6	M		Continue sending output messages
PA8	Monitoring activity on PMA interface in Partition state	27.3.1.6	M		Continue monitoring activity at PMA interface
PA9	Reset of Partition state	27.3.1.6	M		Power-up reset or transmission in excess of no_collision_timer without collision
PA10			OPF:M		Receive activity in excess of no_collision_timer without collision
PA11	Excessive carrier entry into Partition state	27.3.1.6	OPF:M		Carrier duration in excess of jabber_timer in which a collision occurs

27.7.4.9 Receive Jabber function

Item	Feature	Subclause	Status	Support	Value/Comment
RJ1	Receive Jabber function implementation	27.3.1.7	M		Self-interrupt of data reception
RJ2	Excessive receive duration timer for Receive Jabber detection	27.3.1.7	M		Reception duration in excess of jabber_timer
RJ3	Messages sent to repeater unit in Receive Jabber state	27.3.1.7	M		Inhibit sending input messages to repeater unit
RJ4	Messages sent from repeater unit in Receive Jabber state	27.3.1.7	M		Inhibit sending output messages
RJ5	Reset of Receive Jabber state	27.3.1.7	M		Power-up reset or Carrier no longer detected

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27.7.4.10 Repeater state diagrams

Item	Feature	Subclause	Status	Support	Value/Comment
SD1	Repeater Core state diagram	27.3.2.2	M		Meets the requirements of Figure 27–2
SD2	Receive state diagram for Port X	27.3.2.2	M		Meets the requirements of Figure 27–3
SD3	100BASE-TX and 100BASE-FX Transmit state diagram for Port X	27.3.2.2	XP:M		Meets the requirements of Figure 27–4
SD4	100BASE-T4 Transmit state diagram for Port X	27.3.2.2	T4P:M		Meets the requirements of Figure 27–5
SD5	Repeater Data Handler state diagram	27.3.2.2	M		Meets the requirements of Figure 27–6
SD6	Receive Timer for Port X state diagram	27.3.2.2	M		Meets the requirements of Figure 27–7
SD7	Repeater Partition state diagram for Port X	27.3.2.2	M		Meets the requirements of Figure 27–8
SD8	Carrier Integrity Monitor for Port X state diagram	27.3.2.2	M		Meets the requirements of Figure 27–9
SD9	100BASE-T2 Transmit state diagram for Port X	27.3.2.2	T2P:M		Meets the requirements of Figure 27–10

27.7.4.11 Repeater electrical

Item	Feature	Subclause	Status	Support	Value/Comment
EL1	Port-to-port isolation	27.4.1	M		Satisfies isolation and grounding requirements for attached network segments
EL2	Safety	27.5.1	M		IEC 60950:1991
EL3	Installation practices	27.5.2.1	M		Sound, as defined by local code and regulations
EL4	Grounding	27.5.2.2	M		Chassis ground provided through ac mains cord
EL5	2-port repeater set MTBF	27.5.4	M		At least 50 000 hours
EL6	Additional port effect on MTBF	27.5.4	M		No more than 3.46×10^{-6} increase in failures per hour
EL7	Electromagnetic interference	27.5.5.1	M		Comply with local or national codes

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27.7.4.12 Repeater labeling

Item	Feature	Subclause	Status	Support	Value/Comment
LB1	Crossover ports	27.6	M		Marked with an X
LB2	Class I repeater	27.6	CLI:M		Marked with a Roman numeral I centered within a circle
LB3	Class II repeater	27.6	CLII:M		Marked with Roman numerals II centered within a circle
LB4	Data rate	27.6	O		100 Mb/s
LB5	Safety warnings	27.6	O		Any applicable
LB6	Port types	27.6	O		100BASE-FX or 100BASE-TX or 100BASE-T4 or 100BASE-T2
LB7	Worst-case start-of-packet propagation delay	27.6	O		Value in bit times
LB8	Worst-case start-of-collision-Jam propagation delay	27.6	O		Value in bit times
LB9	Worst-case cessation-of-collision Jam propagation delay	27.6	O		Value in bit times

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28. Physical Layer link signaling for Auto-Negotiation on twisted pair

28.1 Overview

28.1.1 Scope

Clause 28 describes the Auto-Negotiation function that allows a device to advertise enhanced modes of operation it possesses to a device at the remote end of a link segment and to detect corresponding enhanced operational modes that the other device may be advertising. The normative definitions for all extensions to Auto-Negotiation and all related register assignments for this standard are documented in Annex 28D.

The objective of the Auto-Negotiation function is to provide the means to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. Auto-Negotiation is performed using a modified 10BASE-T link integrity test pulse sequence, such that no packet or upper layer protocol overhead is added to the network devices (see Figure 28–1). Auto-Negotiation does not test the link segment characteristics (see 28.1.4).

The function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and understanding of the common mode(s) of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The Auto-Negotiation function allows the devices to switch between the various operational modes in an ordered fashion, permits management to disable or enable the Auto-Negotiation function, and allows management to select a specific operational mode. The Auto-Negotiation function also provides a Parallel Detection function to allow 10BASE-T, 100BASE-TX, and 100BASE-T4 compatible devices to be recognized, even though they may not provide Auto-Negotiation.

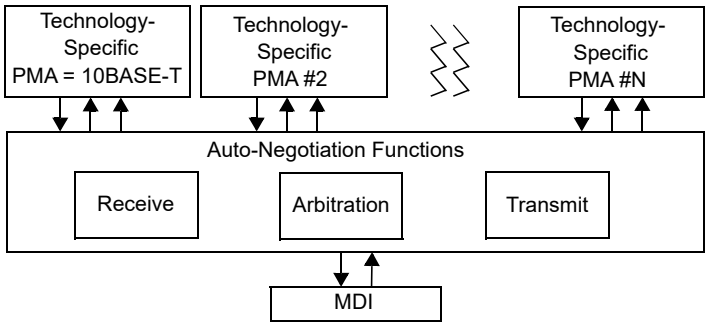

Figure 28–1—High-level model

The basic mechanism to achieve Auto-Negotiation is to pass information encapsulated within a burst of closely spaced link integrity test pulses that individually meet the 10BASE-T Transmitter Waveform for Link Test Pulse (Figure 14–13). This burst of pulses is referred to as a Fast Link Pulse (FLP) Burst. Each device capable of Auto-Negotiation issues FLP Bursts at power up, on command from management, or due to user interaction. The FLP Burst consists of a series of link integrity test pulses that form an alternating clock/data sequence. Extraction of the data bits from the FLP Burst yields a link codeword that identifies the operational modes supported by the remote device, as well as some information used for the Auto-Negotiation function's handshake mechanism.

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To maintain interoperability with existing 10BASE-T devices, the function also supports the reception of 10BASE-T compliant link integrity test pulses. 10BASE-T link pulse activity is referred to as the Normal Link Pulse (NLP) sequence and is defined in 14.2.1.1. A device that fails to respond to the FLP Burst sequence by returning only the NLP sequence is treated as a 10BASE-T compatible device.

28.1.2 Application perspective/objectives

The Auto-Negotiation function is designed to be expandable and allow IEEE 802.3 compatible devices using an eight-pin modular connector to self-configure a jointly compatible operating mode. Implementation of the Auto-Negotiation function is optional. However, it is highly recommended that this method alone be utilized to perform the negotiation of the link operation.

The following are the objectives of Auto-Negotiation:

a) Interoperate with the IEEE 802.3 10BASE-T installed base.
b) Allow automatic upgrade from the 10BASE-T mode to the desired “High-Performance Mode.”
c) Requires that the 10BASE-T data service is the Lowest Common Denominator (LCD) that can be resolved. A 10BASE-T PMA is not required to be implemented, however. Only the NLP Receive Link Integrity Test function is required.
d) Reasonable and cost-effective to implement.
e) Provide a sufficiently extensible code space to
    1) Meet existing and future requirements.
    2) Allow simple extension without impacting the installed base.
    3) Accommodate remote fault signals.
    4) Accommodate Link Partner ability detection.
f) Allow manual or Network Management configuration to override the Auto-Negotiation.
g) Capable of operation in the absence of Network Management.
h) Does not preclude the ability to negotiate “back” to the 10BASE-T operational mode.
i) Operates when
    1) The link is initially electrically connected.
    2) A device at either end of the link is powered up, reset, or a renegotiation request is made.
j) The Auto-Negotiation function may be enabled by automatic, manual, or Network Management intervention.
k) Completes the Base Page Auto-Negotiation function in a bounded time period.
l) Will provide the basis for the link establishment process in future CSMA/CD compatible LAN standards that use an eight-pin modular connector.
m) Does not cause corruption of IEEE 802.3 Layer Management statistics.
n) Operates using a peer-to-peer exchange of information with no requirement for a master device (not master-slave).
o) To be robust in the UTP cable noise environment.
p) To not significantly impact EMI/RFI emissions.

28.1.3 Relationship to architectural layering

The Auto-Negotiation function is provided at the Physical Layer of the OSI reference model as shown in Figure 28–2. Devices that support multiple modes of operation may advertise this fact using this function. The actual transfer of information of ability is observable only at the MDI or on the medium. Auto-Negotiation signaling does not occur across either the AUI or MII. Control of the Auto-Negotiation function may be supported through the Management Interface of the MII or equivalent. If an explicit embodiment of the MII is supported, the control and status registers to support the Auto-Negotiation function shall be implemented in accordance with the definitions in Clause 22 and 28.2.4. If a physical embodiment of the MII management is not present, then it is strongly recommended that the implementation provide control and status mechanisms equivalent to those described in Clause 22 and 28.2.4 for manual and/or management interaction.

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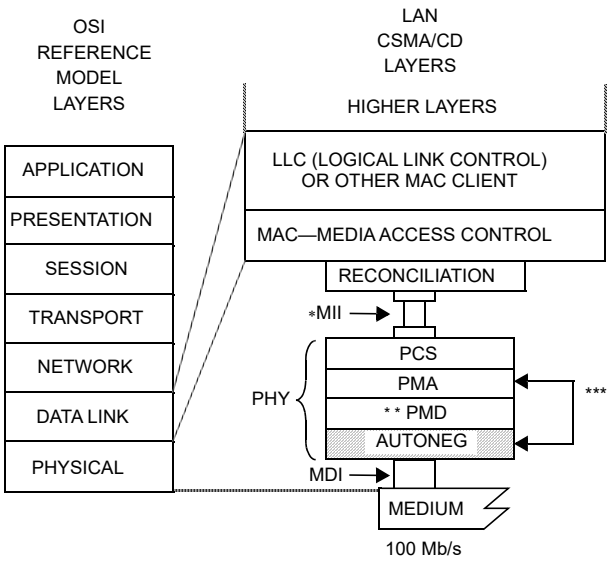

MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
AUTONEG = AUTO-NEGOTIATION
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
** PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.
*** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indication.

Figure 28–2—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

28.1.4 Compatibility considerations

The Auto-Negotiation function is designed to be completely backwards compatible and interoperable with 10BASE-T compliant devices. In order to achieve this, a device supporting the Auto-Negotiation function has to provide the NLP Receive Link Integrity Test function as defined in Figure 28–19. The Auto-Negotiation function also supports connection to 100BASE-TX and 100BASE-T4 devices without Auto-Negotiation through the Parallel Detection function. Connection to technologies other than 10BASE-T, 100BASE-TX, or 100BASE-T4 that do not incorporate Auto-Negotiation is not supported.

Implementation of the Auto-Negotiation function is optional. For CSMA/CD compatible devices that use the eight-pin modular connector of IEC 60603-7 and that also encompass multiple operational modes, if a signaling method is used to automatically configure the preferred mode of operation, then the Auto-Negotiation function shall be used in compliance with Clause 28. If the device uses 10BASE-T compatible link signaling to advertise non-CSMA/CD abilities, the device shall implement the Auto-Negotiation function as administered by this specification. All future CSMA/CD implementations that use an eight-pin modular connector shall be interoperable with devices supporting Clause 28. If the implementer of a non-CSMA/CD eight-pin modular device wishes to assure that its operation does not conflict with CSMA/CD devices, then adherence to Clause 28 is recommended.

While this Auto-Negotiation function has to be implemented in CSMA/CD compatible devices that utilize the eight-pin modular connector, encompass multiple operational modes, and offer an Auto-Negotiation mechanism, the use of this function does not mandate that the 10BASE-T packet data communication service has to exist. A device that employs this function has to support the 10BASE-T Link Integrity Test

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function through the NLP Receive Link Integrity Test state diagram. The device may also need to support other technology-dependent link test functions depending on the modes supported. Auto-Negotiation does not perform cable tests, such as detect number of conductor pairs (if more than two pairs are required) or cable performance measurements. Some PHYs that explicitly require use of high-performance cables, may require knowledge of the cable type, or additional robustness tests (such as monitoring CRC or framing errors) to determine if the link segment is adequate.

28.1.4.1 Interoperability with existing 10BASE-T devices

During Auto-Negotiation, FLP Bursts separated by 16 ms ± 8 ms are transmitted. The FLP Burst itself is a series of pulses separated by 62.5 μs ± 7 μs. The timing of FLP Bursts will cause a 10BASE-T device that is in the LINK TEST PASS state to remain in the LINK TEST PASS state while receiving FLP Bursts. An Auto-Negotiation able device has to recognize the NLP sequence from a 10BASE-T Link Partner, cease transmission of FLP Bursts, and enable the 10BASE-T PMA, if present. If the NLP sequence is detected and if the Auto-Negotiation able device does not have a 10BASE-T PMA, it will cease transmission of FLP Bursts, forcing the 10BASE-T Link Partner into the LINK TEST FAIL state(s) as indicated in Figure 14–6.

NOTE—Auto-Negotiation does not support the transmission of the NLP sequence. The 10BASE-T PMA provides this function if it is connected to the MDI. In the case where an Auto-Negotiation able device without a 10BASE-T PMA is connected to a 10BASE-T device without Auto-Negotiation, the NLP sequence is not transmitted because the Auto-Negotiation function has no 10BASE-T PMA to enable that can transmit the NLP sequence.

28.1.4.2 Interoperability with Auto-Negotiation compatible devices

An Auto-Negotiation compatible device decodes the base link codeword from the FLP Burst, and examines the contents for the highest common ability that both devices share. Both devices acknowledge correct receipt of each other's base link codewords by responding with FLP Bursts containing the Acknowledge Bit set. After both devices complete acknowledgment, and optionally, Next Page exchange, both devices enable the highest common mode negotiated. The highest common mode is resolved using the priority resolution hierarchy specified in Annex 28B. It may subsequently be the responsibility of a technology-dependent link integrity test function to verify operation of the link prior to enabling the data service.

28.1.4.3 Cabling compatibility with Auto-Negotiation

Provision has been made within Auto-Negotiation to limit the resulting link configuration in situations where the cabling may not support the highest common capability of the two end points. The system administrator/installer has to take the cabling capability into consideration when configuring a repeater port's advertised capability. That is, the advertised capability of a hub port should not result in an operational mode that is not compatible with the cabling.

28.2 Functional specifications

The Auto-Negotiation function provides a mechanism to control connection of a single MDI to a single PMA type, where more than one PMA type may exist. Management may provide additional control of Auto-Negotiation through the Management function, but the presence of a management agent is not required.

The Auto-Negotiation function shall provide the Auto-Negotiation Transmit, Receive, and Arbitration functions and comply with the state diagrams of Figure 28–16 to Figure 28–19. The Auto-Negotiation function shall provide the NLP Receive Link Integrity Test function and comply with the state diagram of Figure 28–19 if the PHY supports 10BASE-T operation.The Auto-Negotiation functions shall interact with the technology-dependent PMAs through the Technology-Dependent Interface. Technology-dependent PMAs include, but are not limited to, 100BASE-TX and 100BASE-T4. Technology-dependent link integrity test functions shall be implemented and interfaced to only if the device supports the given technology. For example, a 10BASE-T and 100BASE-TX Auto-Negotiation able device has to implement and interface to

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the 100BASE-TX PMA/link integrity test function, but does not need to include the 100BASE-T4 PMA/ Link Integrity Test function. The Auto-Negotiation function may include a management function that provides a control and status mechanism.

28.2.1 Transmit function requirements

The Transmit function provides the ability to transmit FLP Bursts. The first FLP Bursts exchanged by the local device and its Link Partner after Power-On, link restart, or renegotiation contain the base link codeword defined in 28.2.1.2. The local device may modify the link codeword to disable an ability it possesses, but will not transmit an ability it does not possess. This makes possible the distinction between local abilities and advertised abilities so that multimode devices may Auto-Negotiate to a mode lower in priority than the highest common local ability.

28.2.1.1 Link pulse transmission

Auto-Negotiation's method of communication builds upon the link pulse mechanism employed by 10BASE-T MAUs to detect the status of the link. Compliant 10BASE-T MAUs transmit link integrity test pulses as a mechanism to determine if the link segment is operational in the absence of packet data. The 10BASE-T NLP sequence is a pulse (Figure 14–13) transmitted every 16 ms ± 8 ms while the data transmitter is idle.

Auto-Negotiation substitutes the FLP Burst in place of the single 10BASE-T link integrity test pulse within the NLP sequence (Figure 28–3). The FLP Burst encodes the data that is used to control the Auto-Negotiation function. FLP Bursts shall not be transmitted when Auto-Negotiation is complete and the highest common denominator PMA has been enabled.

FLP Bursts were designed to allow use beyond initial link Auto-Negotiation, such as for a link monitor type function. However, use of FLP Bursts beyond the current definition for link startup shall be prohibited. Definition of the use of FLP Bursts while in the FLP LINK GOOD state is reserved.

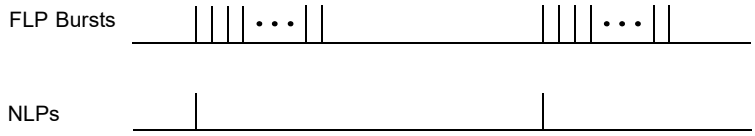

Figure 28–3—FLP Burst sequence to NLP sequence mapping

28.2.1.1.1 FLP burst encoding

All link test pulses in the FLP Burst sequence shall meet the template requirements of Figure 14–13 when measured across each of the test loads defined in Figure 14–12; both with the load connected directly to the TD circuit and with the load connected through all of the cable types and distances supported by the advertised capabilities. A Fast Link Pulse Burst consists of 33 pulse positions. The 17 odd-numbered pulse positions shall contain a link pulse and represent clock information. The 16 even-numbered pulse positions shall represent data information as follows: a link pulse present in an even-numbered pulse position represents a logic one, and a link pulse absent from an even-numbered pulse position represents a logic zero. Clock pulses are differentiated from data pulses by the spacing between pulses as shown in Figure 28–5 and

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enumerated in Table 28–1. An extended FLP Burst contains 97 similarly defined pulse positions with 49 odd-numbered clock pulses and 48 even-numbered data pulses.

Table 28–1—FLP Burst timing summary

	Parameter	Min.	Typ.	Max.	Units
T1	Clock/Data Pulse Width (Figure 14–13)		100		ns
T2	Clock Pulse to Clock Pulse	111	125	139	μs
T3	Clock Pulse to Data Pulse (Data = 1)	55.5	62.5	69.5	μs
T4	Pulses in a Burst	17 for 16-bit 49 for 48-bit		33 for 16-bit 97 for 48-bit	—
T5	Burst Width		2 for 16-bit 6 for 48-bit		ms
T6	FLP Burst to FLP Burst	8	16	24	ms
T7	Optimized FLP Burst to FLP Burst	8		8.5	ms

The encoding of data using pulses in an FLP Burst is illustrated in Figure 28–4.

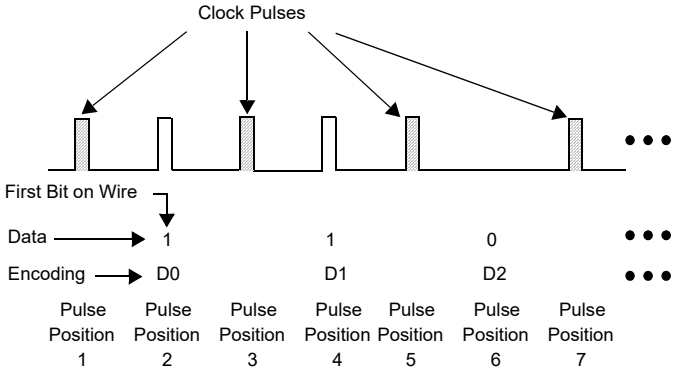

Figure 28–4—Data bit encoding within FLP Bursts

28.2.1.1.2 Transmit timing

The first pulse in an FLP Burst shall be defined as a clock pulse. Clock pulses within an FLP Burst shall be spaced at 125 μs ± 14 μs. If the data bit representation of logic one is to be transmitted, a pulse shall occur 62.5 μs ± 7 μs after the preceding clock pulse. If a data bit representing logic zero is to be transmitted, there shall be no link integrity test pulses within 111 μs of the preceding clock pulse.

The first link pulse in consecutive FLP Bursts shall occur at a 16 ms ± 8 ms interval when using non-optimized FLP Burst to FLP Burst timing, see parameter T6 (Figure 28–6). Devices supporting Extended Next Pages shall use optimized FLP Burst to FLP Burst timing. The first link pulse in consecutive FLP Bursts shall occur at a 8.25 ms ± 0.25 ms interval when using optimized FLP Burst to FLP Burst timing, see parameter T7 (Figure 28–6). Optimized FLP Burst to FLP Burst limits are intended to reduce negotiation time.

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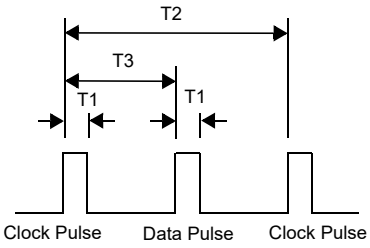

Figure 28–5—FLP Burst pulse-to-pulse timing

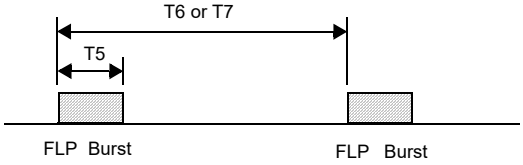

Figure 28–6—FLP Burst to FLP Burst timing

28.2.1.2 Link codeword encoding

The base link codeword (Base Page) transmitted within an FLP Burst shall convey the encoding shown in Figure 28–7. The Auto-Negotiation function may support additional pages using the Next Page function. Encodings for the link codeword(s) used in Next Page exchange are defined in 28.2.3.4. In an FLP Burst, D0 shall be the first bit transmitted.

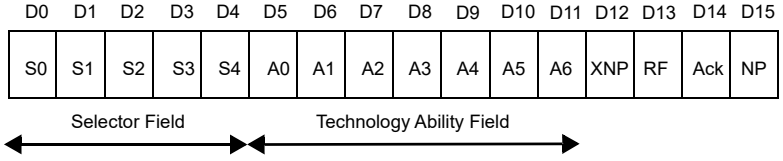

Figure 28–7—Base Page encoding

28.2.1.2.1 Selector Field

Selector Field (S[4:0]) is a five bit wide field, encoding 32 possible messages. Selector Field encoding definitions are shown in Annex 28A. Combinations not specified are reserved for future use. Reserved combinations of the Selector Field shall not be transmitted.

28.2.1.2.2 Technology Ability Field

Technology Ability Field (A[6:0]) is a seven-bit wide field containing information indicating supported technologies specific to the selector field value. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. The Technology Ability Field encoding for the IEEE 802.3 selector is described in Annex 28B.2 and in Annex 28D. Multiple technologies may be advertised in the link codeword. A device shall support the data service ability for a technology it advertises.

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It is the responsibility of the Arbitration function to determine the common mode of operation shared by a Link Partner and to resolve multiple common modes.

NOTE—While devices using a Selector Field value other than the IEEE 802.3 Selector Field value are free to define the Technology Ability Field bits, it is recommended that the 10BASE-T bit be encoded in the same bit position as in the IEEE 802.3 selector. A common bit position can be important if the technology using the other selector will ever coexist on a device that also offers a 10BASE-T mode.

28.2.1.2.3 Extended Next Page

Extended Next Page (XNP) is encoded in bit D12 of the base link codeword. The Extended Next Page bit indicates that the local device supports transmission of Extended Next Pages when set to a logic one, and indicates that the local device does not support Extended Next Pages when set to a logic zero. The use of Extended Next Page is orthogonal to the negotiated data rate, medium, or link technology. The Extended Next Page bit is used in accordance with the Extended Next Page function specifications in 28.2.3.4.

When the selector field value is the IEEE Std 802.5v-2001 (withdrawn) value or the IEEE Std 802.9a-1995 (withdrawn) value the Extended Next Page function is not supported and bit D12 is defined as being an additional Technology Ability Field bit A7, extending the Technology Ability Field to be an eight bit wide field (A[7:0]).

28.2.1.2.4 Remote Fault

Remote Fault (RF) is encoded in bit D13 of the base link codeword. The default value is logic zero. The Remote Fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the Auto-Negotiation advertisement register (register 4) is set to logic one, the RF bit in the transmitted base link codeword is set to logic one. When the RF bit in the received base link codeword is set to logic one, the Remote Fault bit in the MII status register (register 1) will be set to logic one, if the MII management function is present.

The Remote Fault bit shall be used in accordance with the Remote Fault function specifications (28.2.3.5).

28.2.1.2.5 Acknowledge

Acknowledge (Ack) is used by the Auto-Negotiation function to indicate that a device has successfully received its Link Partner’s link codeword. The Acknowledge Bit is encoded in bit D14 regardless of the value of the Selector Field or link codeword encoding. If no Next Page information is to be sent, this bit shall be set to logic one in the link codeword after the reception of at least three consecutive and consistent FLP Bursts (ignoring the Acknowledge bit value). If Next Page information is to be sent, this bit shall be set to logic one after the device has successfully received at least three consecutive and matching FLP Bursts (ignoring the Acknowledge bit value), and will remain set until the Next Page information has been loaded into the Auto-Negotiation Next Page transmit register (register 7). In order to save the current received link codeword, it has to be read from the Auto-Negotiation Link Partner ability register (register 6) before the Next Page of transmit information is loaded into the Auto-Negotiation Next Page transmit register. After the COMPLETE ACKNOWLEDGE state has been entered, the link codeword shall be transmitted six to eight (inclusive) times.

28.2.1.2.6 Next Page

Next Page (NP) is encoded in bit D15 regardless of the Selector Field value or link codeword encoding. Support for transmission and reception of additional link codeword encodings is optional. If Next Page ability is not supported, the NP bit shall always be set to logic zero. If a device implements Next Page ability and wishes to engage in Next Page exchange, it shall set the NP bit to logic one. A device may implement Next Page ability and choose not to engage in Next Page exchange by setting the NP bit to a logic zero. The Next Page function is defined in 28.2.3.4.

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28.2.1.3 Transmit Switch function

The Transmit Switch function shall enable the transmit path from a single technology-dependent PMA to the MDI once a highest common denominator choice has been made and Auto-Negotiation has completed.

During Auto-Negotiation, the Transmit Switch function shall connect only the FLP Burst generator controlled by the Transmit State Diagram, Figure 28–16, to the MDI.

When a PMA is connected to the MDI through the Transmit Switch function, the signals at the MDI shall conform to all of the PHY's specifications.

28.2.2 Receive function requirements

The Receive function detects the NLP sequence using the NLP Receive Link Integrity Test function of Figure 28–19. The NLP Receive Link Integrity Test function will not detect link pass based on carrier sense.

The Receive function detects the FLP Burst sequence, decodes the information contained within, and stores the data in rx_link_code_word[16:1]. The Receive function incorporates a receive switch to control connection to the 100BASE-TX or 100BASE-T4 PMAs in addition to the NLP Receive Link Integrity Test function, excluding the 10BASE-T Link Integrity Test function present in a 10BASE-T PMA. If Auto-Negotiation detects link_status=READY from any of the technology-dependent PMAs prior to FLP Burst detection, the autoneg_wait_timer (28.3.2) is started. If any other technology-dependent PMA indicates link_status=READY when the autoneg_wait_timer expires, Auto-Negotiation will not allow any data service to be enabled and may signal this as a remote fault to the Link Partner using the Base Page and will flag this in the Local Device by setting the Parallel Detection Fault bit (6.4) in the Auto-Negotiation expansion register. If a 10BASE-T PMA exists above the Auto-Negotiation function, it is not permitted to receive MDI activity in parallel with the NLP Receive Link Integrity Test function or any other technology-dependent function.

28.2.2.1 FLP Burst ability detection and decoding

In Figure 28–8 to Figure 28–10, the symbol "t_0=0" indicates the event that caused the timers described to start, and all subsequent times given are referenced from that point. All timers referenced shall expire within the range specified in Table 28–9 in 28.3.2.

The Receive function shall identify the Link Partner as Auto-Negotiation able if it receives 6 to 17 (inclusive) consecutive link pulses that are separated by at least flp_test_min_timer time (5 µs to 25 µs) but less than flp_test_max_timer time (165 µs to 185 µs) as shown in Figure 28–8. The information contained in the FLP Burst that identifies the Link Partner as Auto-Negotiation able shall not be passed to the Arbitration function if the FLP Burst is not complete. The Receive function may use the FLP Burst that identifies the Link Partner as Auto-Negotiation able for ability matching if the FLP Burst is complete. However, it is not required to use this FLP Burst for any purpose other than identification of the Link Partner as Auto-Negotiation able. Implementations may ignore multiple FLP Bursts before identifying the Link Partner as Auto-Negotiation able to allow for potential receive equalization time.

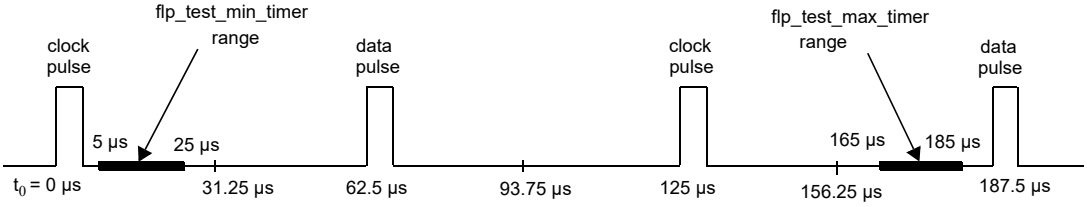

Figure 28–8—FLP detect timers (flp_test_min/max_timers)

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The Receive function captures and decodes link pulses received in FLP Bursts. The first link pulse in an FLP Burst shall be interpreted as a clock link pulse. Detection of a clock link pulse shall restart the data_detect_min_timer and data_detect_max timer. The data_detect_min/max_timers enable the receiver to distinguish data pulses from clock pulses and logic one data from logic zero data, as follows:

a) If, during an FLP Burst, a link pulse is received when the data_detect_min_timer has expired while the data_detect_max_timer has not expired, the data bit shall be interpreted as a logic one (Figure 28–9).
b) If, during an FLP Burst, a link pulse is received after the data_detect_max_timer has expired, the data bit shall be interpreted as a logic zero (Figure 28–9) and that link pulse shall be interpreted as a clock link pulse.

As each data bit is identified it is stored in the appropriate rx_link_code_word[16:1] element.

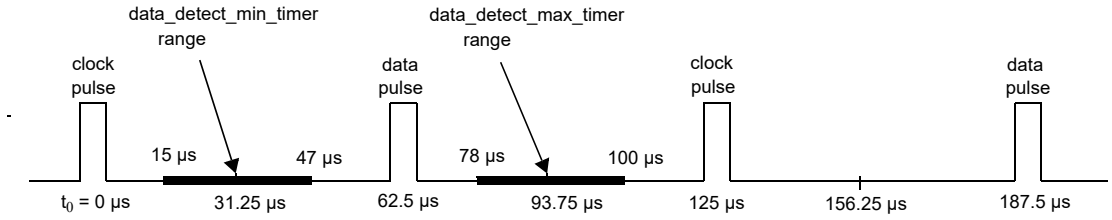
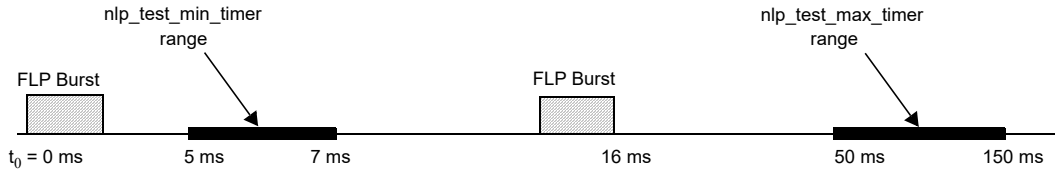


Figure 28–9—FLP data detect timers (data_detect_min/max_timers)

FLP Bursts conforming to the nlp_test_min_timer and nlp_test_max_timer timing as shown in Figure 28–10 shall be considered to have valid separation. The nlp_test_min_timer range for devices that do not support Extended Next Pages is shown in Figure 28–10. The range of nlp_test_min_timer for devices that support Extended Next Pages is specified in 28.3.2.



NOTE—The reference for the starting of the nlp_test_min_timer is from the beginning of the FLP Burst, as shown by t_0, while the reference for the starting of the nlp_test_max_timer is from the expiration of the nlp_test_min_timer.

Figure 28–10—FLP Burst timer (nlp_test_min/max_timers)

28.2.2.2 NLP detection

NLP detection is accomplished via the NLP Receive Link Integrity Test function in Figure 28–19. The NLP Receive Link Integrity Test function is a modification of the original 10BASE-T Link Integrity Test function (Figure 14–6), where the detection of receive activity will not cause a transition to the LINK TEST PASS state during Auto-Negotiation. The NLP Receive Link Integrity Test function also incorporates the Technology-Dependent Interface requirements.

28.2.2.3 Receive Switch function

The Receive Switch function shall enable the receive path from the MDI to a single technology-dependent PMA once a highest common denominator choice has been made and Auto-Negotiation has completed.

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During Auto-Negotiation, the Receive Switch function shall connect both the FLP Burst receiver controlled by the Receive state diagram, Figure 28–17, and the NLP Receive Link Integrity Test state diagram, Figure 28–19, to the MDI. During Auto-Negotiation, the Receive Switch function shall also connect the 100BASE-TX and 100BASE-T4 PMA receivers to the MDI if the 100BASE-TX and/or 100BASE-T4 PMAs are present.

When a PMA is connected to the MDI through the Receive Switch function, the signals at the PMA shall conform to all of the PHY's specifications.

28.2.2.4 Link codeword matching

The Receive function shall generate ability_match, acknowledge_match, and consistency_match variables as defined in 28.3.1.

28.2.3 Arbitration function requirements

The Arbitration function ensures proper sequencing of the Auto-Negotiation function using the Transmit function and Receive function. The Arbitration function enables the Transmit function to advertise and acknowledge abilities. Upon indication of acknowledgment, the Arbitration function determines the highest common denominator using the priority resolution function and enables the appropriate technology-dependent PMA via the Technology-Dependent Interface (28.2.6).

28.2.3.1 Parallel detection function

The Local Device detects a Link Partner that supports Auto-Negotiation by FLP Burst detection. The Parallel Detection function allows detection of Link Partners that support 100BASE-TX, 100BASE-T4, and/or 10BASE-T, but do not support Auto-Negotiation. Prior to detection of FLP Bursts, the Receive Switch shall direct MDI receive activity to the NLP Receive Link Integrity Test state diagram, 100BASE-TX and 100BASE-T4 PMAs, if present, but shall not direct MDI receive activity to the 10BASE-T or any other PMA. If at least one of the 100BASE-TX, 100BASE-T4, or NLP Receive Link Integrity Test functions establishes link_status=READY, the LINK STATUS CHECK state is entered and the autoneg_wait_timer is started. If exactly one link_status=READY indication is present when the autoneg_wait_timer expires, then Auto-Negotiation shall set link_control=ENABLE for the PMA indicating link_status=READY. If a PMA is enabled, the Arbitration function shall set link_control=DISABLE to all other PMAs and indicate that Auto-Negotiation has completed. On transition to the FLP LINK GOOD CHECK state from the LINK STATUS CHECK state the Parallel Detection function shall set the bit in the Link Partner ability register (register 5) corresponding to the technology detected by the Parallel Detection function.

NOTE 1—Native 10BASE-T devices will be detected by the NLP Receive Link Integrity Test function, an integrated part of the Auto-Negotiation function. Hence, Parallel Detection for the 10BASE-T PMA is not required or allowed.

NOTE 2—When selecting the highest common denominator through the Parallel Detection function, only the half-duplex mode corresponding to the selected PMA may automatically be detected.

28.2.3.2 Renegotiation function

A renegotiation request from any entity, such as a management agent, shall cause the Arbitration function to disable all technology-dependent PMAs and halt any transmit data and link pulse activity until the break_link_timer expires (28.3.2). Consequently, the Link Partner will go into link fail and normal Auto-Negotiation resumes. The Local Device shall resume Auto-Negotiation after the break_link_timer has expired by issuing FLP Bursts with the Base Page valid in tx_link_code_word[16:1].

Once Auto-Negotiation has completed, renegotiation will take place if the Highest Common Denominator technology that receives link_control=ENABLE returns link_status=FAIL. To allow the PMA an

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opportunity to determine link integrity using its own link integrity test function, the link_fail_inhibit_timer qualifies the link_status=FAIL indication such that renegotiation takes place if the link_fail_inhibit_timer has expired and the PMA still indicates link_status=FAIL or link_status=READY.

28.2.3.3 Priority Resolution function

Since a Local Device and a Link Partner may have multiple common abilities, a mechanism to resolve which mode to configure is required. The mechanism used by Auto-Negotiation is a Priority Resolution function that predefines the hierarchy of supported technologies. The single PMA enabled to connect to the MDI by Auto-Negotiation shall be the technology corresponding to the bit in the Technology Ability Field common to the Local Device and Link Partner that has the highest priority as defined in Annex 28B. This technology is referred to as the Highest Common Denominator, or HCD, technology. If the Local Device receives a Technology Ability Field with a bit set that is reserved, the Local Device shall ignore that bit for priority resolution. Determination of the HCD technology occurs on entrance to the FLP LINK GOOD CHECK state. In the event that a technology is chosen through the Parallel Detection function, that technology shall be considered the highest common denominator (HCD) technology. In the event that there is no common technology, HCD shall have a value of "NULL," indicating that no PMA receives link_control=ENABLE, and link_status_[HCD]=FAIL.

28.2.3.4 Next Page function

The Next Page function uses the standard Auto-Negotiation arbitration mechanisms to allow exchange of arbitrary pieces of data. Data is carried by optional Next Pages of information, which follow the transmission and acknowledgment procedures used for the base link codeword. Four types of Next Page encodings are defined: Message Pages, Unformatted Pages, extended Message Pages, and extended Unformatted Pages.

A dual acknowledgment system is used. Acknowledge (Ack) is used to acknowledge receipt of the information; Acknowledge 2 (Ack2) is used to indicate that the receiver is able to act on the information (or perform the task) defined in the message.

Next Page operation is controlled by the same three mandatory control bits, Next Page, Extended Next Page, and Acknowledge, used in the base link codeword. Setting the NP bit in the base link codeword to logic one indicates that the device is Next Page able. Setting the Extended Next Page bit in the Base Page link codeword to logic one indicates that the device is Extended Next Page able. If both a device and its Link Partner are Next Page able, then Next Page exchange may occur. If both a device and its Link Partner are Extended Next Page able, then any Next Page exchange that occurs shall use the Extended Next Page encoding. If one or both devices are not Next Page able, then Next Page exchange will not occur and, after the base link codewords have been exchanged, the FLP LINK GOOD CHECK state will be entered. The Toggle bit is used to ensure proper synchronization between the Local Device and the Link Partner.

Next Page exchange occurs after the base link codewords have been exchanged. Next Page exchange consists of using the normal Auto-Negotiation arbitration process to send Next Page messages. Four message encodings are defined: Message Pages, Unformatted Pages, extended Message Pages, and extended Unformatted Pages. Unformatted Pages can be combined to send extended messages. If the Selector Field values do not match, then each series of Unformatted Pages shall be preceded by a Message Page containing a message code that defines how the following Unformatted Pages will be interpreted. If the Selector Field values match, then the convention governing the use of Message Pages shall be as defined by the Selector Field value definition. Any number of Next Pages may be sent in any order; however, it is recommended that the total number of Next Pages sent be kept small to minimize the link startup time.

Next Page transmission ends when both ends of a link segment set their Next Page bits to logic zero, indicating that neither has anything additional to transmit. It is possible for one device to have more pages to transmit than the other device. Once a device has completed transmission of its Next Page information, it

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shall transmit Message Pages, or extended Message Pages, with Null message codes and the NP bit set to logic zero while its Link Partner continues to transmit valid Next Pages. An Auto-Negotiation able device shall recognize reception of Message Pages, or extended Message Pages, with Null message codes as the end of its Link Partner's Next Page information.

28.2.3.4.1 Next Page encodings

The Next Page shall use the encoding shown in Figure 28–11 and Figure 28–12 for the NP, Ack, MP, Ack2, and T bits. The 11-bit field D10–D0 shall be encoded as a Message Code Field if the MP bit is logic one and an Unformatted Code Field if MP is set to logic zero.

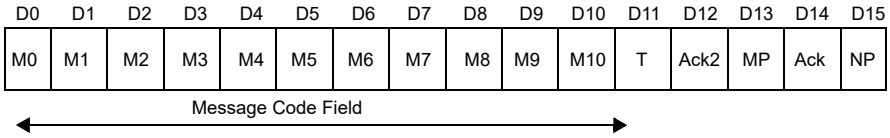

Figure 28–11—Message Page encoding

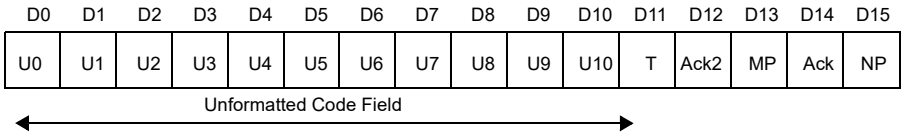

Figure 28–12—Unformatted Page encoding

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28.2.3.4.2 Extended Next Page encodings

Extended Next Pages shall use the encoding shown in Figure 28–13 and Figure 28–14 for the NP, Ack, MP, Ack2, and T bits. The 11-bit field D10:D0 shall be encoded as a Message Code Field if the MP is a logic one and an Unformatted Code Field if the MP bit is set to logic zero.

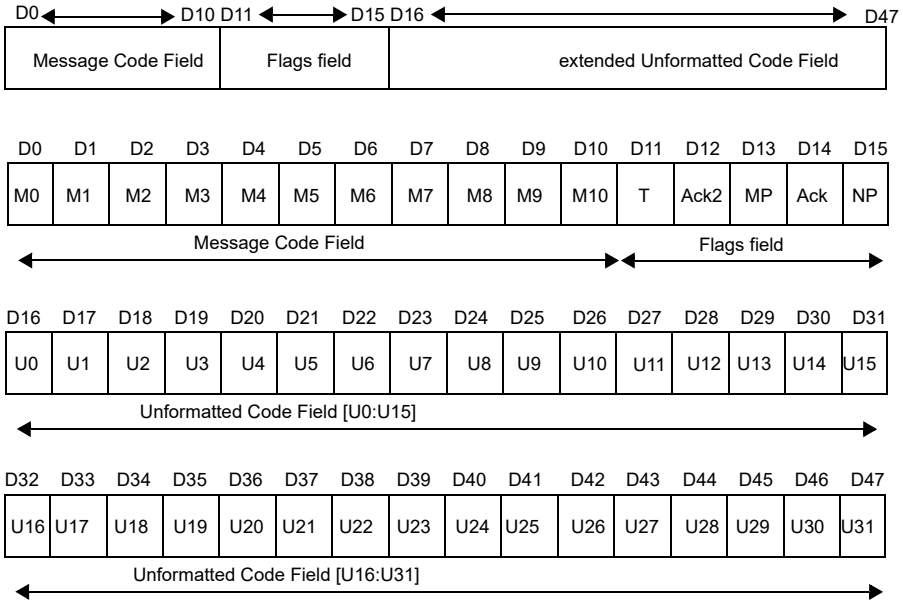

Figure 28–13—Extended Message Page encoding

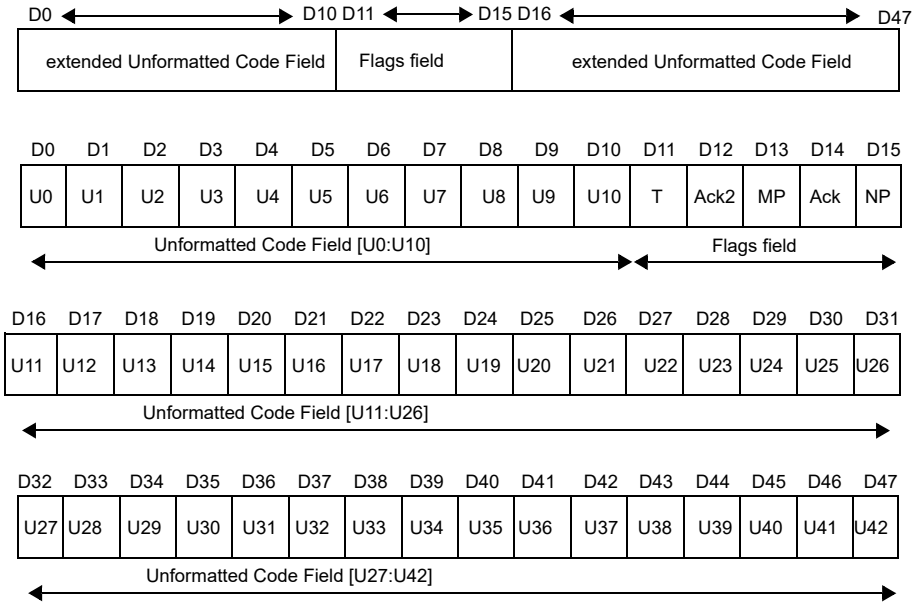

Figure 28–14—Extended Unformatted Page encoding

28.2.3.4.3 Next Page

Next Page (NP) is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. NP shall be set as follows:

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logic zero = last page.
logic one = additional Next Page(s) will follow.

28.2.3.4.4 Acknowledge

As defined in 28.2.1.2.5.

28.2.3.4.5 Message Page

Message Page (MP) is used by the Next Page function to differentiate a Message Page from an Unformatted Page. MP shall be set as follows:

logic zero = Unformatted Page.
logic one = Message Page.

28.2.3.4.6 Acknowledge 2

Acknowledge 2 (Ack2) is used by the Next Page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows:

logic zero = cannot comply with message.
logic one = will comply with message.

28.2.3.4.7 Toggle

Toggle (T) is used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged link codeword. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit D11 in the base link codeword and, therefore, may assume a value of logic one or zero. The Toggle bit shall be set as follows:

logic zero = previous value of the transmitted link codeword equaled logic one.
logic one = previous value of the transmitted link codeword equaled logic zero.

28.2.3.4.8 Message Page encoding

Message Pages are formatted pages that carry a single predefined message code, which is enumerated in Annex 28C. Two-thousand and forty-eight message codes are available. The allocation of these codes will be controlled by the contents of Annex 28C. If the Message Page bit is set to logic one, then the bit encoding of the link codeword shall be interpreted as a Message Page.

28.2.3.4.9 Message Code Field

Message Code Field (M[10:0]) is an eleven bit wide field, encoding 2048 possible messages. Message Code Field definitions are shown in Annex 28C. Combinations not specified are reserved for future use. Reserved combinations of the Message Code Field shall not be transmitted.

28.2.3.4.10 Unformatted Page encoding

Unformatted Pages carry the messages indicated by Message Pages. Five control bits are predefined, the remaining 11 bits may take on an arbitrary value. If the Message Page bit is set to logic zero, then the bit encoding of the link codeword shall be interpreted as an Unformatted Page.

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28.2.3.4.11 Unformatted Code Field

Unformatted Code Field (U[10:0]) is an eleven bit wide field, which may contain an arbitrary value.

28.2.3.4.12 Extended Unformatted Code Field

The extended Unformatted Code Field is a 32-bit or 43-bit wide field, which may contain an arbitrary value. The field is 32 bits wide in an extended Message Page and 43 bits wide in an extended Unformatted Page.

28.2.3.4.13 Use of Next Pages

a) Both devices have to indicate Next Page ability for either to commence exchange of Next Pages.
b) Both devices have to indicate Extended Next Page ability for either to commence exchange of Extended Next Pages.
c) If both devices are Next Page able, then both devices shall send at least one Next Page.
d) If both devices are Extended Next Page able, then both devices only transmit Extended Next Pages.
e) Next Page exchange shall continue until neither device on a link has more pages to transmit as indicated by the NP bit. A Message Page with a Null Message Code Field value shall be sent if the device has no other information to transmit.
f) A message code can carry either a specific message or information that defines how following Unformatted Page(s) should be interpreted.
g) If a message code references Unformatted Pages, the Unformatted Pages shall immediately follow the referencing message code in the order specified by the message code.
h) Unformatted Page users are responsible for controlling the format and sequencing for their Unformatted Pages.
i) An Extended Next Page provides a message code and extended Unformatted Code Field. The Message Code Field can carry either a specific message or information that defines how the following extended Unformatted Code Field should be interpreted.

28.2.3.4.14 MII register requirements

The Next Page Transmit register defined in 28.2.4.1.6 shall hold the Next Page to be sent by Auto-Negotiation. Received Next Pages may be stored in the Auto-Negotiation Link Partner ability register.

28.2.3.5 Remote fault sensing function

The Remote Fault function may indicate to the Link Partner that a fault condition has occurred using the Remote Fault bit and, optionally, the Next Page function.

Sensing of faults in a device as well as subsequent association of faults with the Remote Fault bit shall be optional. If the Local Device has no mechanism to detect a fault or associate a fault condition with the received Remote Fault bit indication, then it shall transmit the Remote Fault bit with the value contained in the Auto-Negotiation advertisement register bit (4.13).

A Local Device may indicate it has sensed a fault to its Link Partner by setting the Remote Fault bit in the Auto-Negotiation advertisement register and renegotiating.

If the Local Device sets the Remote Fault bit to logic one, it may also use the Next Page function to specify information about the fault that has occurred. Remote Fault Message Page Codes have been specified for this purpose.

The Remote Fault bit shall remain set until after successful negotiation with the base link codeword, at which time the Remote Fault bit shall be reset to a logic zero. On receipt of a base link codeword with the

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Remote Fault bit set to logic one, the device shall set the Remote Fault bit in the MII status register (1.4) to logic one if the MII management function is present.

28.2.4 Management function requirements

The management interface is used to communicate Auto-Negotiation information to the management entity. If an MII is physically implemented, then management access is via the MII Management interface. Where no physical embodiment of the MII exists, an equivalent to MII registers 0, 1, 4, 5, 6, and 7 (Clause 22) are recommended to be provided.

28.2.4.1 Media Independent Interface

The Auto-Negotiation function shall have five dedicated registers:

a) MII control register (register 0).
b) MII status register (register 1).
c) Auto-Negotiation advertisement register (register 4).
d) Auto-Negotiation Link Partner ability register (register 5).
e) Auto-Negotiation expansion register (register 6).

If the Next Page function is implemented, the Auto-Negotiation Next Page transmit register (register 7) shall be implemented.

28.2.4.1.1 MII control register

MII control register (register 0) provides the mechanism to disable/enable and/or restart Auto-Negotiation. The definition for this register is provided in 22.2.4.1.

The Auto-Negotiation function shall be enabled by setting bit 0.12 to a logic one. If bit 0.12 is set to a logic one, then bits 0.13 and 0.8 shall have no effect on the link configuration, and the Auto-Negotiation process will determine the link configuration. If bit 0.12 is cleared to logic zero, then bits 0.13 and 0.8 will determine the link configuration regardless of the prior state of the link configuration and the Auto-Negotiation process.

A PHY shall return a value of one in bit 0.9 until the Auto-Negotiation process has been initiated. The Auto-Negotiation process shall be initiated by setting bit 0.9 to a logic one. If Auto-Negotiation was completed prior to this bit being set, the process shall be reinitiated. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, then this bit will have no meaning, and should be written as zero. This bit is self-clearing. The Auto-Negotiation process shall not be affected by clearing this bit to logic zero.

28.2.4.1.2 MII status register

The MII status register (register 1) includes information about all modes of operations supported by the Local Device's PHY, the status of Auto-Negotiation, and whether the Auto-Negotiation function is supported by the PHY or not. The definition for this register is provided in 22.2.4.2.

When read as a logic one, bit 1.5 indicates that the Auto-Negotiation process has been completed, and that the contents of registers 4, 5, and 6 are valid. When read as a logic zero, bit 1.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of registers 4, 5, and 6 are meaningless. A PHY shall return a value of zero in bit 1.5 if Auto-Negotiation is disabled by clearing bit 0.12. A PHY shall also return a value of zero in bit 1.5 if it lacks the ability to perform Auto-Negotiation.

When read as logic one, bit 1.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The Remote Fault bit shall be

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implemented with a latching function, such that the occurrence of a remote fault will cause the Remote Fault bit to become set and remain set until it is cleared. The Remote Fault bit shall be cleared each time register 1 is read via the management interface, and shall also be cleared by a PHY reset.

When read as a one, bit 1.3 indicates that the PHY has the ability to perform Auto-Negotiation. When read as a logic zero, bit 1.3 indicates that the PHY lacks the ability to perform Auto-Negotiation.

28.2.4.1.3 Auto-Negotiation advertisement register (Register 4) (R/W)

This register contains the Advertised Ability of the PHY. (See Table 28–2). The bit definition for the Base Page is defined in 28.2.1.2. On power-up, before Auto-Negotiation starts, this register shall have the following configuration: The Selector Field (4.4:0) is set to an appropriate code as specified in Annex 28A. The Acknowledge bit (4.14) is set to logic zero. The Technology Ability Field (4.11:5) is set based on the values set in the MII status register (register 1) (1.15:11) or equivalent. See also 28.2.1.2.3 and Annex 28D.

Table 28–2—Advertisement register bit definitions

Bit(s)	Name	Description	R/W[a]
4.15	Next Page	See 28.2.1.2	R/W
4.14	Reserved	Write as zero, ignore on read	RO
4.13	Remote Fault	See 28.2.1.2	R/W
4.12	Extended Next Page	See 28.2.1.2	R/W
4.11:5	Technology Ability Field	See 28.2.1.2	R/W
4.4:0	Selector Field	See 28.2.1.2	R/W

[a]RO = Read only, R/W = Read/Write.

Only the bits in the Technology Ability Field that represent the technologies supported by the Local Device may be set. Any of the Technology Ability Field bits that may be set can also be cleared by management before a renegotiation. This can be used to enable management to Auto-Negotiate to an alternate common mode.

The management entity may initiate renegotiation with the Link Partner using alternate abilities by setting the Selector Field (4.4:0) and Technology Ability Field (4.11:5) to indicate the preferred mode of operation and setting the Restart Auto-Negotiation bit (0.9) in the control register (register 0) to logic one.

Any writes to this register prior to completion of Auto-Negotiation as indicated by bit 1.5 should be followed by a renegotiation for the new values to be properly used for Auto-Negotiation. Once Auto-Negotiation has completed, this register value may be examined by software to determine the highest common denominator technology.

28.2.4.1.4 Auto-Negotiation Link Partner ability register (Register 5) (RO)

All of the bits in the Auto-Negotiation Link Partner ability register are read only. A write to the Auto-Negotiation Link Partner ability register shall have no effect.

This register contains the Advertised Ability of the Link Partner's PHY. (See Tables 28–3 and 28–4.) The bit definitions shall be a direct representation of the received link codeword (Figure 28–7). Upon successful completion of Auto-Negotiation, status register (register 1) Auto-Negotiation Complete bit (1.5) shall be set

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to logic one. If the Next Page function is supported and bit (6.6) in the Auto-Negotiation expansion register (register 6) is set to logic zero, then the Auto-Negotiation Link Partner ability register may be used to store Link Partner Next Pages. If bit (6.6) in the Auto-Negotiation expansion register (register 6) is set to logic one, then bit (6.5) determines where the Link Partner Next Pages are stored.

Table 28–3—Link partner ability register bit definitions (Base Page)

Bit(s)	Name	Description	R/W[a]
5.15	Next Page	See 28.2.1.2	RO
5.14	Acknowledge	See 28.2.1.2	RO
5.13	Remote Fault	See 28.2.1.2	RO
5.12	Extended Next Page	See 28.2.1.2	RO
5.11:5	Technology Ability Field	See 28.2.1.2	RO
5.4:0	Selector Field	See 28.2.1.2	RO

[a]RO = Read only.

Table 28–4—Link partner ability register bit definitions (Next Page)

Bit(s)	Name	Description	R/W[a]
5.15	Next Page	See 28.2.3.4	RO
5.14	Acknowledge	See 28.2.3.4	RO
5.13	Message Page	See 28.2.3.4	RO
5.12	Acknowledge 2	See 28.2.3.4	RO
5.11	Toggle	See 28.2.3.4	RO
5.10:0	Message/Unformatted Code Field	See 28.2.3.4	RO

[a]RO = Read only.

The values contained in this register are only guaranteed to be valid once Auto-Negotiation has successfully completed, as indicated by bit 1.5 or, if used with Next Page exchange, after the Page Received bit (6.1) has been set to logic one.

NOTE—If this register is used to store Link Partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent Link Partner Next Pages.

28.2.4.1.5 Auto-Negotiation expansion register (Register 6) (RO)

All of the bits in the Auto-Negotiation expansion register are read only; a write to the Auto-Negotiation expansion register shall have no effect. (See Table 28–5.)

Bits 6.15:7 are reserved for future Auto-Negotiation expansion.

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Table 28–5—Expansion register bit definitions

Bit(s)	Name	Description	R/W[a]	Default
6.15:7	Reserved	Write as zero, ignore on read	RO	0
6.6	Receive Next Page Location Able	1 = Received Next Page storage location is specified by bit (6.5) 0 = Received Next Page storage location is not specified by bit (6.5)	RO	—
6.5	Received Next Page Storage Location	1 = Link Partner Next Pages are stored in register 8 0 = Link Partner Next Pages are stored in register 5	RO	—
6.4	Parallel Detection Fault	1 = A fault has been detected via the Parallel Detection function. 0 = A fault has not been detected via the Parallel Detection function.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able	RO	0
6.2	Next Page Able	1 = Local Device is Next Page able 0 = Local Device is not Next Page able	RO	0
6.1	Page Received	1 = A New Page has been received 0 = A New Page has not been received	RO/ LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able	RO	0

[a]RO = Read only, LH = Latching high.

The Receive Next Page Location Able bit (6.6) shall be set to logic one to indicate that the Link Partner Next Page Storage Location bit (6.5) is supported.

The Receive Next Page Storage Location bit (6.5) shall be set to logic one to indicate that the Link Partner's Next Pages are stored in the Auto-Negotiation Link Partner Received Next Page register (register 8). This bit shall be set to logic zero to indicate that the Link Partner’s Next Pages are stored in the Auto-Negotiation Link Partner ability register (register 5). It is recommended that all new implementations store the Link Partner’s Next Pages in the Auto-Negotiation Link Partner Received Next Page ability register (register 8).

NOTE— It is highly recommended that the Link Partner Next Page Storage Location bit (6.5) is supported. If this bit is not supported there is no indication if the Link Partners Next Page is stored in register 5 or register 8.

The Parallel Detection Fault bit (6.4) shall be set to logic one to indicate that zero or more than one of the NLP Receive Link Integrity Test function, 100BASE-TX, or 100BASE-T4 PMAs have indicated link_status=READY when the autoneg_wait_timer expires. The Parallel Detection Fault bit shall be reset to logic zero on a read of the Auto-Negotiation expansion register (register 6).

The Link Partner Next Page Able bit (6.3) shall be set to logic one to indicate that the Link Partner supports the Next Page function. This bit shall be reset to logic zero to indicate that the Link Partner does not support the Next Page function.

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The Next Page Able bit (6.2) shall be set to logic one to indicate that the Local Device supports the Next Page function. The Next Page Able bit (6.2) shall be set to logic zero if the Next Page function is not supported.

The Page Received bit (6.1) shall be set to logic one to indicate that a new link codeword has been received and stored in the Auto-Negotiation Link Partner ability register. The Page Received bit shall be reset to logic zero on a read of the Auto-Negotiation expansion register (register 6).

The Link Partner Auto-Negotiation Able bit (6.0) shall be set to logic one to indicate that the Link Partner is able to participate in the Auto-Negotiation function. This bit shall be reset to logic zero if the Link Partner is not Auto-Negotiation able.

28.2.4.1.6 Auto-Negotiation Next Page transmit register (Register 7) (R/W)

The Auto-Negotiation Next Page Transmit register contains the Next Page link codeword to be transmitted when Next Page ability is supported. (See Table 28–6.) The contents are defined in 28.2.3.4. On power-up, this register shall contain the default value of 2001H, which represents a Message Page with the message code set to Null Message. This value may be replaced by any valid Next Page message code that the device wishes to transmit. Writing to this register shall set mr_next_page_loaded to true.

Table 28–6—Next Page transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
7.15	Next Page	See 28.2.3.4	R/W
7.14	Reserved	Write as 0, ignore on read	RO
7.13	Message Page	See 28.2.3.4	R/W
7.12	Acknowledge 2	See 28.2.3.4	R/W
7.11	Toggle	See 28.2.3.4	RO
7.10:0	Message/Unformatted Code field	See 28.2.3.4	R/W

[a]RO = Read only, R/W = Read/Write.

28.2.4.1.7 Auto-Negotiation Link Partner Received Next Page register (Register 8) (RO)

Support for 100BASE-T2 and 1000BASE-T requires support for Next Page and the provision of an Auto-Negotiation Link Partner Received Next Page register (register 8) to store Link Partner Next Pages as shown in Table 28–7. All of the bits in the Auto-Negotiation Link Partner Received Next Page register are read only. A write to the Auto-Negotiation Link Partner Received Next Page register shall have no effect.

The values contained in this register are only guaranteed to be valid after the Page Received bit (6.1) has been set to logical one or once Auto-Negotiation has successfully completed, as indicated by bit 1.5.

NOTE—If this register is used to store multiple Link Partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent Link Partner Next Pages.

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Table 28–7—Link Partner Received Next Page register bit definitions

Bit(s)	Name	Description	R/W[a]
8.15	Next Page	see 28.2.3.4	RO
8.14	Acknowledge	see 28.2.3.4	RO
8.13	Message Page	see 28.2.3.4	RO
8.12	Acknowledge 2	see 28.2.3.4	RO
8.11	Toggle	see 28.2.3.4	RO
8.10:0	Message/Unformatted Code Field	see 28.2.3.4	RO

[a]RO = Read only.

28.2.4.1.8 State diagram variable to MII register mapping

The state diagrams of Figure 28–16 to Figure 28–19 generate and accept variables of the form "mr_x," where x is an individual signal name. These variables comprise a management interface that may be connected to the MII management function or other equivalent function. Table 28–8 describes how the MII registers map to the management function interface signals.

Table 28–8—State diagram variable to MII register mapping

State diagram variable	MII register	MDIO register
mr_adv_ability[16:1]	4.15:0 Auto-Negotiation advertisement register	7.16.15:0 AN advertisement register
mr_autoneg_complete	1.5 Auto-Negotiation Complete	7.1.5 Auto-Negotiation Complete
mr_autoneg_enable	0.12 Auto-Negotiation Enable	7.0.12 Auto-Negotiation Enable
mr_lp_adv_ability[16:1]	For Base Page: 5.15:0 Auto-Negotiation link partner ability register For Next Page(s): If 6.6=1 and 6.5=1 then 8.15:0 is Auto-Negotiation link partner Received Next Page register If 6.6=1 and 6.5= 0 then 5.15:0 is Auto-Negotiation link partner ability register If 6.6=0 then 8.15:0 or 5.15:0 is Auto-Negotiation link partner Next Page ability register	7.19.15:0 AN LP Base Page ability register
mr_lp_autoneg_able	6.0 Link Partner Auto-Negotiation able	
mr_lp_np_able	6.3 Link Partner Next Page able	
mr_main_reset	0.15 Reset	7.0.15 Reset
mr_next_page_loaded	Set on write to Auto-Negotiation Next Page Transmit register; cleared by Arbitration state diagram	
mr_np_able	6.2 Next Page able	

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Table 28–8—State diagram variable to MII register mapping *(continued)*

State diagram variable	MII register	MDIO register
mr_np_tx[16:1]	7.15:0 Auto-Negotiation Next Page Transmit Register	7.22.15:0 AN XNP transmit register
mr_np_tx[32:17]	Extended Next Pages not supported by MII register interface	7.23.15:0 Unformatted Code Field 1
mr_np_tx[48:33]	Extended Next Pages not supported by MII register interface	7.24.15:0 Unformatted Code Field 2
mr_page_rx	6.1 Page Received	7.1.6 Page Received
mr_parallel_detection_fault	6.4 Parallel Detection Fault	
mr_restart_negotiation	0.9 Auto-Negotiation Restart	7.0.9 Auto-Negotiation Restart
set if Auto-Negotiation is available	1.3 Auto-Negotiation Ability	7.1.3 Auto-Negotiation Ability

28.2.4.2 Auto-Negotiation managed object class

The Auto-Negotiation Managed Object Class is defined in Clause 30.

28.2.5 Absence of management function

In the absence of any management function, the advertised abilities shall be provided through a logical equivalent of mr_adv_ability[16:1]. A device shall comply with all Next Page function requirements, including the provision of the mr_np_able, mr_lp_np_able, and mr_next_page_loaded variables (or their logical equivalents), in order to permit the NP bit to be set to logic one in the transmitted link codeword.

NOTE—Storage of a valid base link codeword is required to prevent a deadlock situation where negotiation has to start again while Next Pages are being transmitted. If a shared transmit register were used, then renegotiation could not occur when Next Pages were being transmitted because the base link codeword would not be available. This requirement can be met using a number of different implementations, including use of temporary registers or register stacks.

28.2.6 Technology-Dependent Interface

The Technology-Dependent Interface is the communication mechanism between each technology's PMA and the Auto-Negotiation function. Auto-Negotiation can support multiple technologies, all of which need not be implemented in a given device. Each of these technologies may utilize its own technology-dependent link integrity test function.

28.2.6.1 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium. The purpose of this primitive is to give the PCS, repeater client, or Auto-Negotiation function a means of determining the validity of received code elements.

28.2.6.1.1 Semantics of the service primitive

PMA_LINK.indication(link_status)

The link_status parameter shall assume one of three values: READY, OK, or FAIL, indicating whether the underlying receive channel is intact and ready to be enabled (READY), intact and enabled (OK), or not

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intact (FAIL). When link_status=FAIL or link_status=READY, the PMA_CARRIER.indication and PMA_UNITDATA.indication primitives are undefined.

28.2.6.1.2 When generated

A technology-dependent PMA and the NLP Receive Link Integrity Test state diagram (Figure 28–19) shall generate this primitive to indicate the value of link_status.

28.2.6.1.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the state diagrams of Figure 28–18.

28.2.6.2 PMA_LINK.request

This primitive is generated by Auto-Negotiation to allow it to enable and disable operation of the PMA.

28.2.6.2.1 Semantics of the service primitive

PMA_LINK.request(link_control)

The link_control parameter shall assume one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

The link_control=SCAN_FOR_CARRIER mode is used by the Auto-Negotiation function prior to receiving any FLP Bursts or link_status=READY indications. During this mode, the PMA shall search for carrier and report link_status=READY when carrier is received, but no other actions shall be enabled.

The link_control=DISABLE mode shall be used by the Auto-Negotiation function to disable PMA processing.

The link_control=ENABLE mode shall be used by Auto-Negotiation to turn control over to a single PMA for all normal processing functions.

28.2.6.2.2 When generated

The Auto-Negotiation function shall generate this primitive to indicate to the PHY how to respond, in accordance with the state diagrams of Figure 28–17 and Figure 28–18.

Upon power-on or reset, if the Auto-Negotiation function is enabled (mr_autoneg_enable=true) the PMA_LINK.request(DISABLE) message shall be issued to all technology-dependent PMAs. If Auto-Negotiation is disabled at any time including at power-on or reset, the state of PMA_LINK.request(link_control) is implementation dependent.

28.2.6.2.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the NLP Receive Link Integrity Test state diagram (Figure 28–19) and the receiving technology-dependent link integrity test function, based on the intent specified in the primitive semantics.

28.2.6.3 PMA_LINKPULSE.request

This primitive is generated by Auto-Negotiation to indicate that a valid Link Pulse, as transmitted in compliance with Figure 14–13, has been received.

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28.2.6.3.1 Semantics of the service primitive

PMA_LINKPULSE.request (linkpulse)

The linkpulse parameter shall assume one of two values: TRUE or FALSE.

The linkpulse=FALSE mode shall be used by the Auto-Negotiation function to indicate that the Receive state diagram has performed a state transition.

The linkpulse=TRUE mode shall be used by the Auto-Negotiation function to indicate that a valid Link Pulse has been received.

28.2.6.3.2 When generated

The Auto-Negotiation function shall generate this primitive to indicate to the PHY how to respond, in accordance with the state diagram of Figure 28–17.

Upon power-on or reset, if the Auto-Negotiation function is enabled (mr_autoneg_enable=true) the PMA_LINKPULSE.request (FALSE) message shall be issued to all technology-dependent PMAs. If Auto-Negotiation is disabled at any time including at power-on or reset, the state of PMA_LINKPULSE.request (linkpulse) is implementation dependent.

28.2.6.3.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the receiving technology-dependent PMA function, based on the intent specified in the primitive semantics.

28.3 State diagrams and variable definitions

The notation used in the state diagrams (Figure 28–16 to Figure 28–19) follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set. Variables using the “mr_x” notation do not have state diagram defaults; however, their appropriate initialization conditions when mapped to the MII interface are covered in 28.2.4 and 22.2.4, and Clause 45 MDIO management interface. The variables, timers, and counters used in the state diagrams are defined in 28.3, 14.2.3, and 28.2.6.

Auto-Negotiation shall implement the Transmit state diagram, Receive state diagram, Arbitration state diagram, and NLP Receive Link Integrity Test state diagram as depicted in 28.3. Additional requirements to these state diagrams are made in the respective functional requirements sections. Options to these state diagrams clearly stated as such in the functional requirements sections or state diagrams shall be allowed. In the case of any ambiguity between stated requirements and the state diagrams, the state diagrams shall take precedence.

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The functional reference diagram (Figure 28–15) provides a generic example, illustrated with initial PMA implementations and showing the mechanism for expansion. New PMAs are documented in Annex 28D.

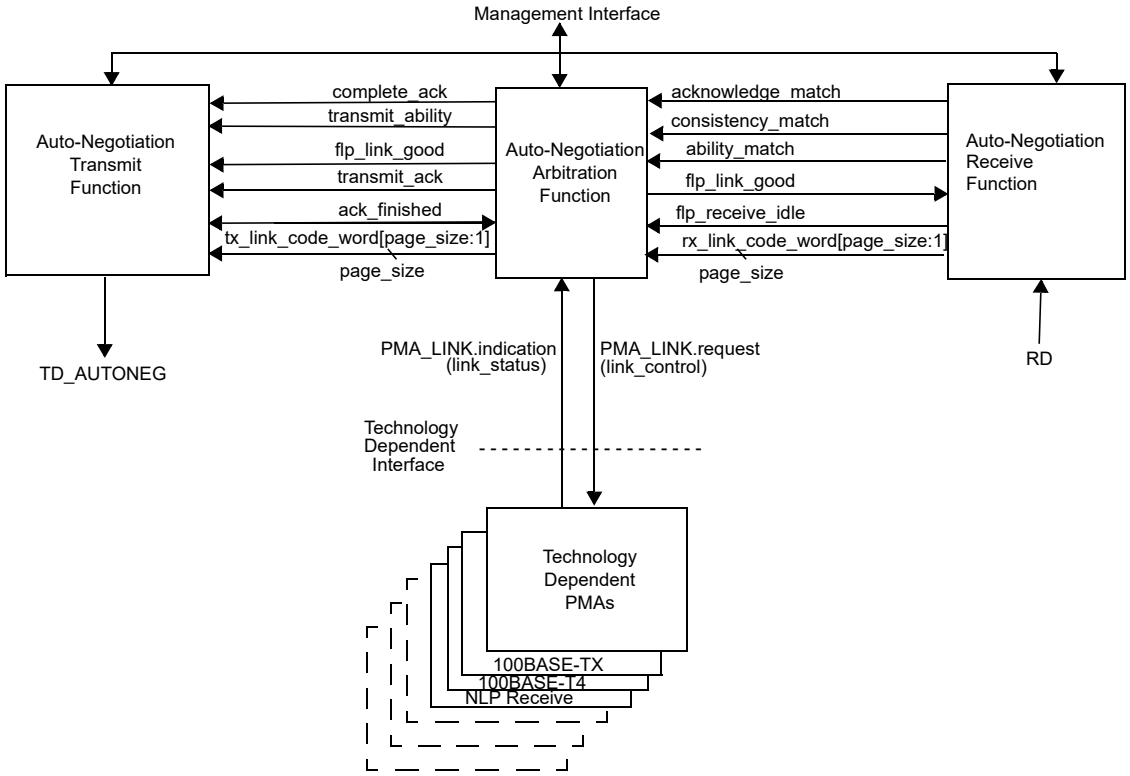

Figure 28–15—Functional reference diagram

28.3.1 State diagram variables

A variable with "_[x]" appended to the end of the variable name indicates a variable or set of variables as defined by "x". "x" may be as follows:

all;	represents all specific technology-dependent PMAs supported in the Local Device and the NLP Receive Link Integrity Test state diagram.
1GigT;	represents that the 1000BASE-T PMA is the signal source.
2p5GigT;	represents that the 2.5GBASE-T PMA is the signal source.
5GigT;	represents that the 5GBASE-T PMA is the signal source.
10GigT;	represents that the 10GBASE-T PMA is the signal source.
25GigT;	represents that the 25GBASE-T PMA is the signal source.
40GigT;	represents that the 40GBASE-T PMA is the signal source.
HCD;	represents the single technology-dependent PMA chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or Parallel Detection function. To select 10BASE-T, LIT is used instead of NLP to enable the full 10BASE-T Link Integrity Test function state diagram.
notHCD;	represents all technology-dependent PMAs not chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or Parallel Detection function.
TX;	represents that the 100BASE-TX PMA is the signal source.
T4;	represents that the 100BASE-T4 PMA is the signal source.

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NLP; represents that the NLP Receive Link Integrity Test function is the signal source.

PD; represents all of the following that are present: 100BASE-TX PMA, 100BASE-T4 PMA, and the NLP Receive Link Integrity Test state diagram.

LIT; represents the 10BASE-T Link Integrity Test function state diagram is the signal source or destination.

Variables with [16:1] appended to the end of the variable name indicate arrays that can be directly mapped to 16-bit registers. For these variables, "[x]" indexes an element or set of elements in the array, where "[x]" may be as follows:

— Any integer.
— Any variable that takes on integer values.
— NP; represents the index of the Next Page bit.
— ACK; represents the index of the Acknowledge bit.
— RF; represents the index of the Remote Fault bit.

Variables of the form "mr_x", where x is a label, comprise a management interface that is intended to be connected to the MII Management function. However, an implementation-specific management interface may provide the control and status function of these bits.

ability_match

Indicates that three consecutive link codewords match, ignoring the Acknowledge bit. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word-match comparison or not.

Values: false; three matching consecutive link codewords have not been received, ignoring the Acknowledge bit (default).
true; three matching consecutive link codewords have been received, ignoring the Acknowledge bit.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

ability_match_word [16:1]

A 16-bit array that contains the last link codeword that caused ability_match = true. For each element in the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

ack_finished

Status indicating that the final remaining_ack_cnt link codewords with the Ack bit set have been transmitted.

Values: false; more link codewords with the Ack bit set to logic one have to be transmitted.
true; all remaining link codewords with the Ack bit set to logic one have been transmitted.

acknowledge_match

Indicates that three consecutive link codewords match and have the Acknowledge bit set. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word match comparison or not.

Values: false; three matching and consecutive link codewords have not been received with the Acknowledge bit set (default).
true; three matching and consecutive link codewords have been received with the

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Acknowledge bit set.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

base_page

Status indicating that the page currently being transmitted by Auto-Negotiation is the initial link codeword encoding used to communicate the device's abilities.

Values: false; a page other than base link codeword is being transmitted.
true; the base link codeword is being transmitted.

complete_ack

Controls the counting of transmitted link codewords that have their Acknowledge bit set.

Values: false; transmitted link codewords with the Acknowledge bit set are not counted (default).
true; transmitted link codewords with the Acknowledge bit set are counted.

consistency_match

Indicates that the link codeword that caused ability_match to be set is the same as the link codeword that caused acknowledge_match to be set.

Values: false; the link codeword that caused ability_match to be set is not the same as the link codeword that caused acknowledge_match to be set, ignoring the Acknowledge bit value.
true; the link codeword that caused ability_match to be set is the same as the link codeword that caused acknowledge_match to be set, independent of the Acknowledge bit value.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

desire_np

Status indicating that the Local Device desires to engage in Next Page exchange. This information comes from the setting of the NP bit in the base link codeword stored in the Auto-Negotiation advertisement register (register 4).

Values: false; Next page exchange is not desired.
true; Next page exchange is desired.

flp_link_good

Indicates that Auto-Negotiation has completed.

Values: false; negotiation is in progress (default).
true; negotiation is complete, forcing the Transmit and Receive functions to IDLE.

flp_receive_idle

Indicates that the Receive state diagram is in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state.

Values: false; the Receive state diagram is not in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state (default).
true; the Receive state diagram is in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state.

incompatible_link

Parameter used following Priority Resolution to indicate the resolved link is incompatible with the Local Device settings. A device's ability to set this variable to true is optional.

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Values: false; A compatible link exists between the Local Device and Link Partner (default).
true; Optional indication that Priority Resolution has determined no highest common denominator exists following the most recent negotiation.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

link_control

This variable is defined in 28.2.6.2.1.

link_status

This variable is defined in 28.2.6.1.1.

linkpulse

This variable is defined in 28.2.6.3.1.

Values: false; linkpulse is set to false after any Receive State Diagram state transition (default).
true; linkpulse is set to true when a valid Link Pulse is received.

mr_autoneg_complete

Status indicating whether Auto-Negotiation has completed or not.

Values: false; Auto-Negotiation has not completed.
true; Auto-Negotiation has completed.

mr_autoneg_enable

Controls the enabling and disabling of the Auto-Negotiation function.

Values: false; Auto-Negotiation is disabled.
true; Auto-Negotiation is enabled.

mr_adv_ability[16:1]

A 16-bit array that contains the Advertised Abilities link codeword.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_adv_ability[16:1]

A 16-bit array that contains the Link Partner’s Advertised Abilities link codeword.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_np_able

Status indicating whether the Link Partner supports Next Page exchange.

Values: false; the Link Partner does not support Next Page exchange.
true; the Link Partner supports Next Page exchange.

mr_np_able

Status indicating whether the Local Device supports Next Page exchange.

Values: false; the Local Device does not support Next Page exchange.
true; the Local Device supports Next Page exchange.

mr_lp_autoneg_able

Status indicating whether the Link Partner supports Auto-Negotiation.

Values: false; the Link Partner does not support Auto-Negotiation.

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true; the Link Partner supports Auto-Negotiation.

mr_main_reset

Controls the resetting of the Auto-Negotiation state diagrams.

Values: false; do not reset the Auto-Negotiation state diagrams.
true; reset the Auto-Negotiation state diagrams.

mr_next_page_loaded

Status indicating whether a new page has been loaded into the Auto-Negotiation Next Page Transmit register (register 7).

Values: false; a New Page has not been loaded.
true; a New Page has been loaded.

mr_np_tx[page_size:1]

A 16-bit or 48-bit array that contains the new Next Page to transmit.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_page_rx

Status indicating whether a New Page has been received. A New Page has been successfully received when acknowledge_match=true and consistency_match=true and the link codeword has been written to mr_lp_adv_ability[16:1].

Values: false; a New Page has not been received.
true; a New Page has been received.

mr_parallel_detection_fault

Error condition indicating that while performing Parallel Detection, either flp_receive_idle = false, or zero or more than one of the following indications were present when the autoneg_wait_timer expired. This signal is cleared on read of the Auto-Negotiation expansion register.

1) link_status_ [NLP] = READY
2) link_status_[TX] = READY
3) link_status_[T4] = READY

Values: false; exactly one of the above three indications was true when the autoneg_wait_timer expired, and flp_receive_idle = true.
true; either zero or more than one of the above three indications was true when the autoneg_wait_timer expired, or flp_receive_idle = false.

mr_restart_negotiation

Controls the entrance to the TRANSMIT DISABLE state to break the link before Auto-Negotiation is allowed to renegotiate via management control.

Values: false; renegotiation is not taking place.
true; renegotiation is started.

np_rx

Flag to hold the value of rx_link_code_word[NP] upon entry to the COMPLETE ACKNOWLEDGE state. This value is associated with the value of rx_link_code_word[NP] when acknowledge_match was last set.

Values zero; local device np_rx bit equals a logical zero.
one; local device np_rx bit equals a logical one.

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page_size

Status indicating the size of Next Page that the device is prepared to transmit and receive.

Values: 16; the device does not support Extended Next Pages or Extended Next Page ability has not been enabled.
48; Extended Next Page ability is supported and has been enabled.

NOTE— This variable is set by this variable definition; it is not set explicitly in the state diagrams. The variable takes on the value of 16 upon entry into the TRANSMIT DISABLE state and is updated upon entry into the NEXT PAGE WAIT state.

power_on

Condition that is true until such time as the power supply for the device that contains the Auto-Negotiation state diagrams has reached the operating region or the device has low power mode set via MII control register bit 0.11.

Values: false; the device is completely powered (default).
true; the device has not been completely powered.

rx_link_code_word[page_size:1]

A 16-bit or 48-bit array that contains the data bits to be received from an FLP Burst.
For each element within the array:

Values: zero; data bit is a logical zero.
one; data bit is a logical one.

single_link_ready

Status indicating that flp_receive_idle = true and only one the of the following indications is being received:

1) link_status_[NLP] = READY
2) link_status_[TX] = READY
3) link_status_[T4] = READY

Values: false; either zero or more than one of the above three indications are true or flp_receive_idle = false.
true; Exactly one of the above three indications is true and flp_receive_idle = true.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

TD_AUTONEG

Controls the signal sent by Auto-Negotiation on the TD_AUTONEG circuit.

Values: idle; Auto-Negotiation prevents transmission of all link pulses on the MDI.
link_test_pulse; Auto-Negotiation causes a single link pulse as defined by Figure 14–13 to be transmitted on the MDI.

toggle_rx

Flag to keep track of the state of the Link Partner’s Toggle bit.

Values: 0; Link Partner’s Toggle bit equals logic zero.
1; Link Partner’s Toggle bit equals logic one.

toggle_tx

Flag to keep track of the state of the Local Device’s Toggle bit.

Values: 0; Local Device’s Toggle bit equals logic zero.
1; Local Device’s Toggle bit equals logic one.

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transmit_ability
: Controls the transmission of the link codeword containing tx_link_code_word[page_size:1].

  Values: false; any transmission of tx_link_code_word[page_size:1] is halted (default).
  true; the transmit state diagram begins sending tx_link_code_word[page_size:1].

transmit_ack
: Controls the setting of the Acknowledge bit in the tx_link_code_word[page_size:1] to be transmitted.

  Values: false; sets the Acknowledge bit in the transmitted tx_link_code_word[page_size:1] to a logic zero (default).
  true; sets the Acknowledge bit in the transmitted tx_link_code_word[page_size:1] to a logic one.

transmit_disable
: Controls the transmission of tx_link_code_word[page_size:1].

  Values: false; tx_link_code_word[page_size:1] transmission is allowed (default).
  true; tx_link_code_word[page_size:1] transmission is halted.

tx_link_code_word[page_size:1]
: A 16-bit or 48-bit array that contains the data bits to be transmitted in an FLP Burst. This array may be loaded from mr_adv_ability or mr_np_tx.
  For each element within the array:

  Values: Zero; data bit is logical zero.
  One; data bit is logical one.

28.3.2 State diagram timers

All timers operate in the manner described in 14.2.3.2.

autoneg_wait_timer
: Timer for the amount of time to wait before evaluating the number of link integrity test functions with link_status=READY asserted. The autoneg_wait_timer shall expire 500 ms to 1000 ms from the assertion of link_status=READY from the 100BASE-TX PMA, 100BASE-T4 PMA, or the NLP Receive State diagram.

break_link_timer
: Timer for the amount of time to wait in order to assure that the Link Partner enters a Link Fail state. The timer shall expire 1200 ms to1500 ms after being started.

data_detect_max_timer
: Timer for the maximum time between a clock pulse and the next link pulse. This timer is used in conjunction with the data_detect_min_timer to detect whether the data bit between two clock pulses is a logic zero or a logic one. The data_detect_max_timer shall expire 78 µs to 100 µs from the last clock pulse.

data_detect_min_timer
: Timer for the minimum time between a clock pulse and the next link pulse. This timer is used in conjunction with the data_detect_max_timer to detect whether the data bit between two clock pulses is a logic zero or a logic one. The data_detect_min_timer shall expire 15 µs to 47 µs from the last clock pulse.

flp_test_max_timer
: Timer for the maximum time between two link pulses within an FLP Burst. This timer is used in conjunction with the flp_test_min_timer to detect whether the Link Partner is transmitting FLP

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Bursts. The flp_test_max_timer shall expire 165 µs to 185 µs from the last link pulse.

flp_test_min_timer
: Timer for the minimum time between two link pulses within an FLP Burst. This timer is used in conjunction with the flp_test_max_timer to detect whether the Link Partner is transmitting FLP Bursts. The flp_test_min_timer shall expire 5 µs to 25 µs from the last link pulse.

interval_timer
: Timer for the separation of a transmitted clock pulse from a data bit. The interval_timer shall expire 55.5 µs to 69.5 µs from each clock pulse and data bit.

link_fail_inhibit_timer
: Timer for qualifying a link_status=FAIL indication or a link_status=READY indication when a specific technology link is first being established. A link will only be considered "failed" if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The link_fail_inhibit_timer shall expire 750 ms to 1000 ms after entering the FLP LINK GOOD CHECK state for devices operating at 10/100/1000 Mb/s. The link_fail_inhibit_timer shall expire 2000 ms to 2250 ms after entering the FLP LINK GOOD CHECK state for devices in the MultiGBASE-T PHY set.

  NOTE—The link_fail_inhibit_timer expiration value has to be greater than the time required for the Link Partner to complete Auto-Negotiation after the Local Device has completed Auto-Negotiation plus the time required for the specific technology to enter the link_status=OK state. The maximum time difference between a Local Device and its Link Partner completing Auto-Negotiation is

  (Maximum FLP Burst to FLP Burst separation) × (Maximum number of FLP Bursts needed to complete acknowledgment) = (24 ms) × (8 bursts) = 192 ms.

  For example, 100BASE-T4 requires approximately 460 ms to enter link_status=OK for a total minimum link_fail_inhibit_timer time of 652 ms. The lower bound for the link_fail_inhibit_timer was chosen to provide adequate margin for the current technologies and any future PMAs.

nlp_test_max_timer
: Timer for the maximum time that no FLP Burst may be seen before forcing the receive state diagram to the IDLE state. The nlp_test_max_timer shall expire 50 ms to 150 ms after being started or restarted.

nlp_test_min_timer
: Timer for the minimum time between two consecutive FLP Bursts. The nlp_test_min_timer shall expire 5 ms to 7 ms after being started or restarted for devices that do not support Extended Next Pages, and shall expire 6.75 ms to 7.25 ms after being started or restarted for devices that do support Extended Next Pages.

transmit_link_burst_timer
: Timer for the separation of a transmitted FLP Burst from the next FLP Burst. The transmit_link_burst_timer shall expire 5.7 ms to 22.3 ms after the last transmitted link pulse in an FLP Burst when Extended Next Pages are not supported. When Extended Next Pages are supported, the timer shall expire 5.7 ms to 6.8 ms after the last transmitted link pulse when transmitting 16-bit pages, and shall expire 1.3 ms to 3.1 ms after the last transmitted pulse when transmitting 48-bit pages.

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Table 28–9—Timer min./max. value summary

Parameter	Min.	Typ.	Max.	Units
autoneg_wait_timer	500		1000	ms
break_link_timer	1200		1500	ms
data_detect_min_timer	15		47	µs
data_detect_max_timer	78		100	µs
flp_test_min_timer	5		25	µs
flp_test_max_timer	165		185	µs
interval_timer	55.5	62.5	69.5	µs
link_fail_inhibit_timer (10/100/1000 Mb/s devices)	750		1000	ms
link_fail_inhibit_timer (devices in the MultiGBASE-T set)	2000		2250	ms
nlp_test_max_timer	50		150	ms
nlp_test_min_timer (no support of Extended Next Pages)	5		7	ms
nlp_test_min_timer (support of Extended Next Pages)	6.75		7.25	ms
transmit_link_burst_timer (no support of Extended Next Pages)	5.7	14	22.3	ms
transmit_link_burst_timer (support of Extended Next Pages when page_size is 16)	5.7	6.25	6.8	ms
transmit_link_burst_timer (support of Extended Next Pages when page_size is 48)	1.3	2.25	3.2	ms

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28.3.3 State diagram counters

flp_cnt

A counter that may take on integer values from 0 to 17. This counter is used to keep a count of the number of FLPs detected to enable the determination of whether the Link Partner supports Auto-Negotiation.

Values: not_done; 0 to 5 inclusive.
done; 6 to 17 inclusive.
init; counter is reset to zero.

remaining_ack_cnt

A counter that may take on integer values from 0 to 8. The number of additional link codewords with the Acknowledge Bit set to logic one to be sent to ensure that the Link Partner receives the acknowledgment.

Values: not_done; positive integers between 0 and 5 inclusive.
done; positive integers 6 to 8 inclusive (default).
init; counter is reset to zero.

rx_bit_cnt

A counter that may take on integer values from 0 to (page_size+1). This counter is used to keep a count of data bits received from an FLP Burst and to ensure that when erroneous extra pulses are received, the first page_size bits are kept while the rest are ignored. When this variable reaches page_size or (page_size+1), enough data bits have been received. This counter does not increment beyond (page_size+1) and does not return to 0 until it is reinitialized.

Values: not_done; 1 to (page_size–1) inclusive.
done; page_size or (page_size+1)
init; counter is reset to zero.
rx_bit_cnt_check; 10 to 17 inclusive.

tx_bit_cnt

A counter that may take on integer values from 1 to (page_size+1). This counter is used to keep a count of data bits sent within an FLP Burst. When this variable reaches (page_size+1), all data bits have been sent.

Values: not_done; 1 to page_size inclusive.
done; (page_size+1).
init; counter is initialized to 1.

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28.3.4 State diagrams

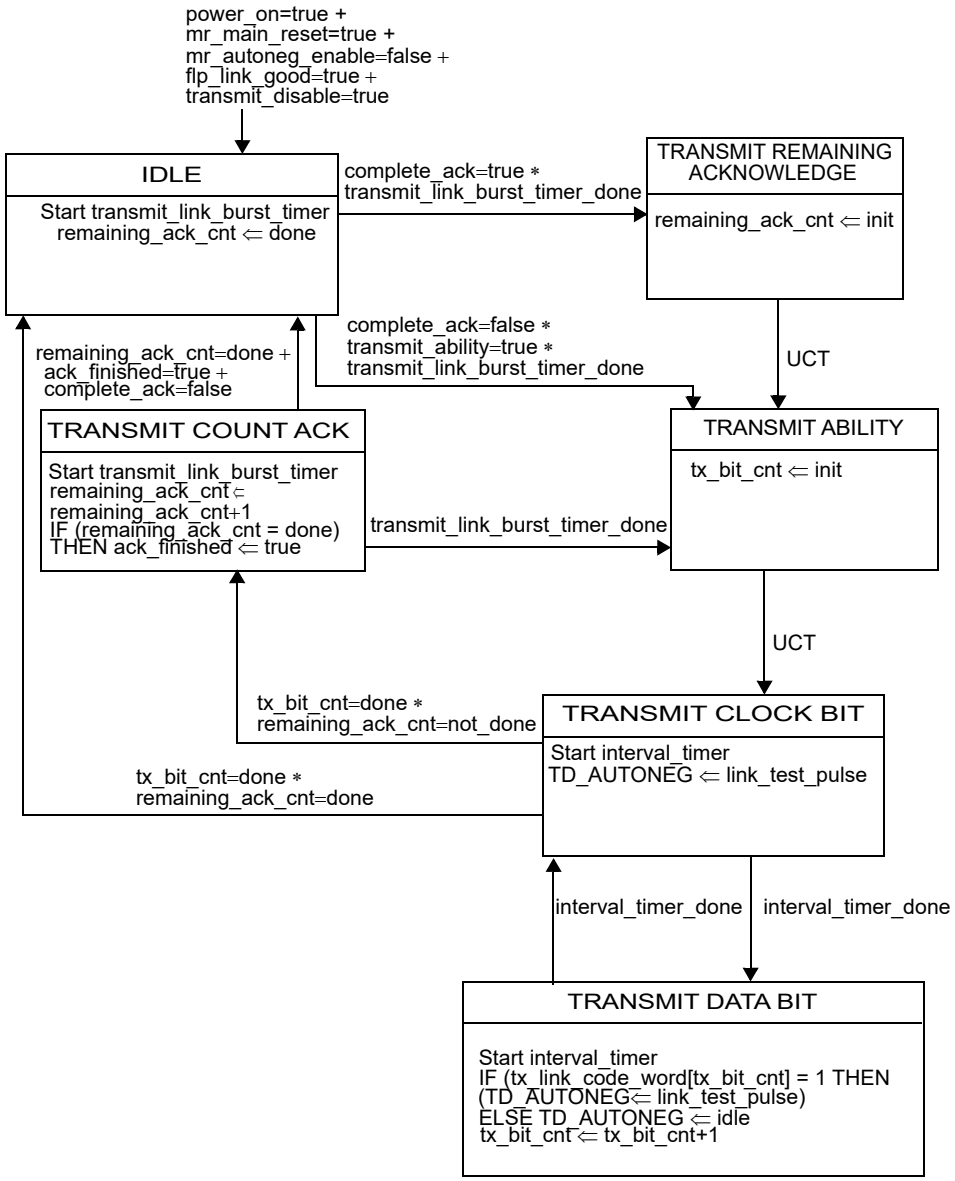

Figure 28–16—Transmit state diagram

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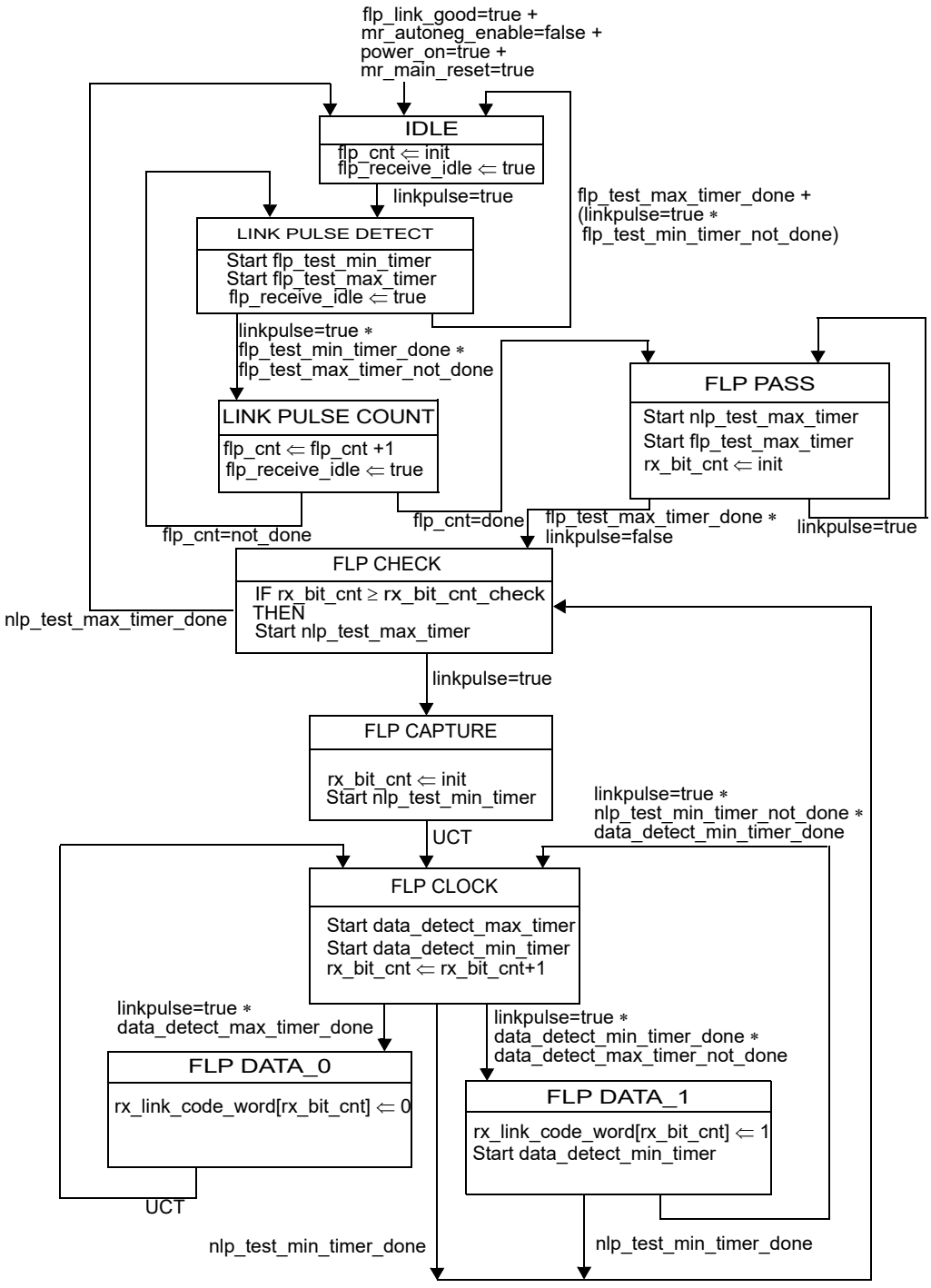

Figure 28–17—Receive state diagram

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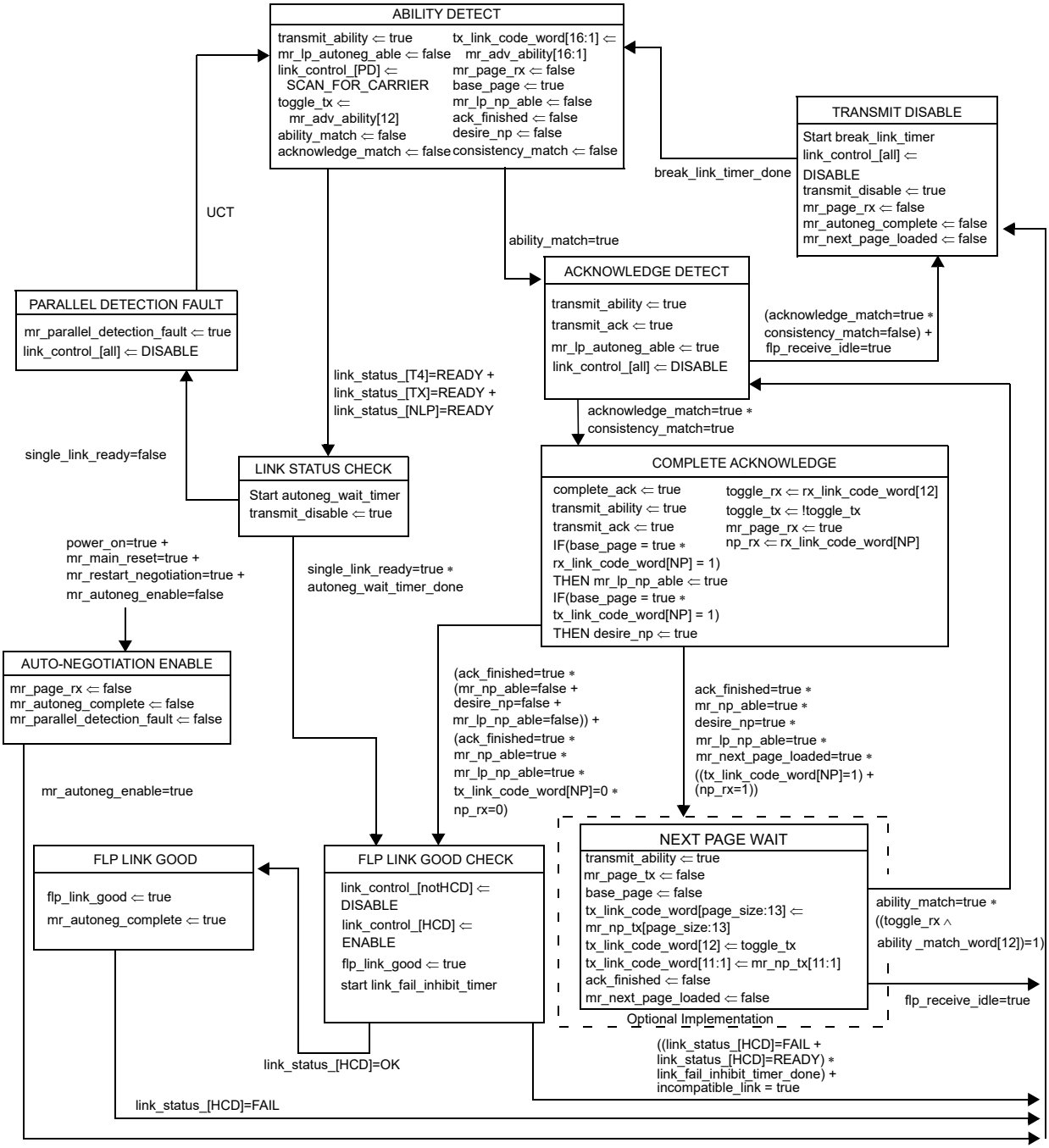

NOTE—The transition from COMPLETE ACKNOWLEDGE to FLP LINK GOOD CHECK can be simplified to "ack_finished=true" if the optional Next Page function is not supported.

NOTE—ability_match, acknowledge_match, single_link_ready, consistency_match, incompatible_link, and page_size are set according to the variable definitions and are not set explicitlly in the state diagrams.

Figure 28–18—Arbitration state diagram

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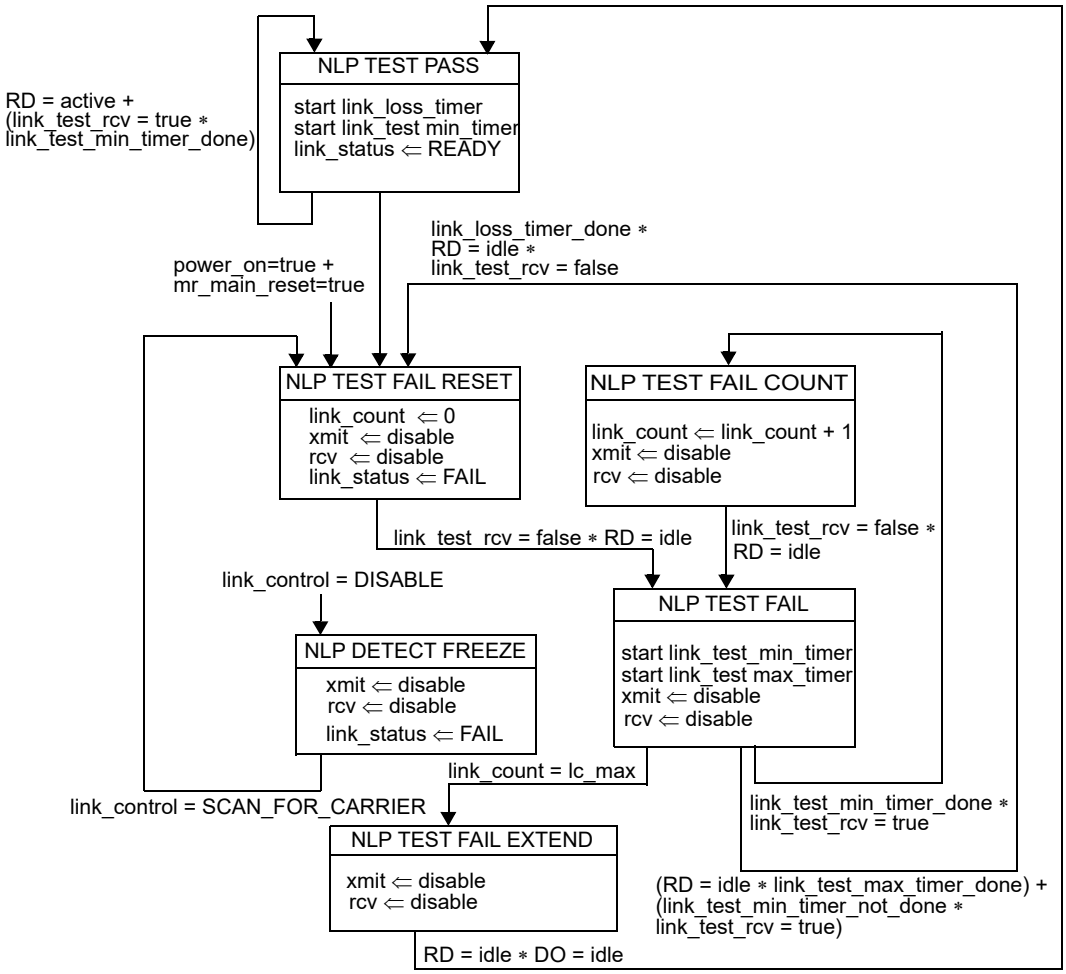

NOTE—The variables link_control and link_status are viewed as dedicated signals by the NLP Receive Link integrity Test state diagram, but are viewed as link_control_[NLP] and link_status_[NLP] by the Auto-Negotiation Arbitration state diagram, Figure 28–18.

Figure 28–19—NLP Receive Link Integrity Test state diagram

28.4 Electrical specifications

The electrical characteristics of pulses within FLP Bursts shall be identical to the characteristics of NLPs and shall meet the requirements of Figure 14–13.

It is the responsibility of the technology-specific Transmit and Receive functions to interface to the MDI correctly.

NOTE—The requirements relative to the interface to the MDI are specified via the Transmit Switch and Receive Switch functions.

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28.5 Protocol implementation conformance statement (PICS) proforma for Clause 28, Physical Layer link signaling for Auto-Negotiation on twisted pair[63]

28.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 28, Physical Layer link signaling for Auto-Negotiation on twisted pair, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

28.5.2 Identification

28.5.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

28.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[63] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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28.5.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
10BT	Implementation supports a 10BASE-T data service	28.1.2	O		N/A
*NP	Implementation supports Next Page function	28.1.2	O		N/A
*MII	Implementation supports the MII Management Interface	28.1.2	O/1		N/A
MGMT	Implementation supports a non-MII Management Interface	28.1.2	O/1		N/A
*NOM	Implementation does not support management	28.1.2	O/1		N/A
*RF	Implementation supports Remote Fault Sensing	28.2.3.5	O		N/A
*NPSL	Link Partner Next Page Storage Location bit	28.2.4.1.5	O		N/A
*ENP	Implementation supports Extended Next Pages	28.2.3.4.2	O		N/A
*OPT	Implementation supports optimized FLP burst to FLP burst timing	28.2.1.1.2	ENP:M !ENP:O		N/A
*MG	Implementation supports a member of the MultiGBASE-T PHY set (see 1.4.406)	55, 113, and 126	O		N/A

28.5.4 PICS proforma tables for Physical Layer link signaling for Auto-Negotiation on twisted pair

28.5.4.1 Scope

Item	Feature	Subclause	Status	Support	Value/Comment
SC1	MII Management Interface control and status registers	28.1.3	MII:M		Implemented in accordance with the definitions in Clause 22 and 28.2.4
SC2	CSMA/CD compatible devices using an eight-pin modular connector and using a signaling method to automatically configure the preferred mode of operation	28.1.4	M		Auto-Negotiation function implemented in compliance with Clause 28
SC3	Device uses 10BASE-T compatible link signaling to advertise non-CSMA/CD abilities	28.1.4	M		Auto-Negotiation function implemented in compliance with Clause 28
SC4	Future CSMA/CD implementations that use an eight-pin modular connector	28.1.4	M		Interoperable with devices compliant with Clause 28

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28.5.4.2 Auto-Negotiation functions

Item	Feature	Subclause	Status	Support	Value/Comment
AN1	Transmit	28.2	M		Complies with Figure 28–16
AN2	Receive	28.2	M		Complies with Figure 28–17
AN3	Arbitration	28.2	M		Complies with Figure 28–18
AN4	NLP Receive Link Integrity Test	28.2	10BT:M		Complies with Figure 28–19
AN5	Technology-Dependent Interface	28.2	M		Complies with 28.2.6
AN6	Technology-dependent link integrity test	28.2	M		Implemented and interfaced to for those technologies supported by device
AN7	Management function	28.2	O		

28.5.4.3 Transmit function requirements

Item	Feature	Subclause	Status	Support	Value/Comment
TF1	FLP Burst transmission	28.2.1.1	M		Not transmitted once Auto-Negotiation is complete and highest common denominator PMA has been enabled. Prohibited other than for link startup
TF2	FLP Burst composition	28.2.1.1.1	M		Pulses in FLP Bursts meet the requirements of Figure 14–13
TF3	FLP Burst pulse definition	28.2.1.1.1	M		Odd-numbered pulse positions represent clock information; even-numbered pulse positions represent data information
TF4	The first pulse in an FLP Burst	28.2.1.1.2	M		Defined as a clock pulse for timing purposes
TF5	FLP Burst clock pulse spacing	28.2.1.1.2	M		Within an FLP Burst, spacing is 125 μs ± 14 μs
TF6	Logic one data bit representation	28.2.1.1.2	M		Pulse transmitted 62.5 μs ± 7 μs after the preceding clock pulse
TF7	Logic zero data bit representation	28.2.1.1.2	M		No link integrity test pulses within 111 μs of the preceding clock pulse
TF8	Consecutive FLP Bursts	28.2.1.1.2	M		The first link pulse in each FLP Burst is separated by 16 ms ± 8 ms
TF9	Consecutive FLP Bursts	28.2.1.1.2	OPT:M		The first link pulse in each FLP Burst is separated by 8.25 ms ± 0.25 ms
TF10	FLP Burst Base Page	28.2.1.2	M		Conforms to Figure 28–7

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28.5.4.3 Transmit function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
TF11	FLP Burst bit transmission order	28.2.1.2	M		Transmission is D0 first to D15 last
TF12	Selector Field values	28.2.1.2.1	M		Only defined values transmitted
TF13	Technology Ability Field values	28.2.1.2.2	M		Implementation supports a data service for each ability set in the Technology Ability Field
TF14	Remote Fault bit	28.2.1.2.4	M		Used in accordance with the Remote Fault function specifications
TF15	Acknowledge bit set, no Next Page to be sent	28.2.1.2.5	M		Set to logic one in the link codeword after the reception of at least three consecutive and consistent FLP Bursts
TF16	Acknowledge bit set, Next Page to be sent	28.2.1.2.5	NP:M		Set to logic one in the transmitted link codeword after the reception of at least three consecutive and consistent FLP Bursts and the current receive link codeword is saved
TF17	Number of link codewords sent with Acknowledge bit set	28.2.1.2.5	M		6 to 8 inclusive after COMPLETE ACKNOWLEDGE state entered
TF18	Device does not implement optional Next Page ability	28.2.1.2.6	M		NP=0 in base link codeword
TF19	Device implements optional Next Page ability and wishes to engage in Next Page exchange	28.2.1.2.6	NP:M		NP=1 in base link codeword
TF20	Transmit Switch function on completion of Auto-Negotiation	28.2.1.3	M		Enables the transmit path from a single technology-dependent PMA to the MDI once the highest common denominator has been selected
TF21	Transmit Switch function during Auto-Negotiation	28.2.1.3	M		Connects FLP Burst generator governed by Figure 28–16 to the MDI
TF22	Signals presented at MDI after connection through Transmit Switch from PMA	28.2.1.3	M		Conform to appropriate PHY specifications

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28.5.4.4 Receive function requirements

Item	Feature	Subclause	Status	Support	Value/Comment
RF1	Timer expiration	28.2.2.1	M		Timer definition in 28.3.2, values shown in Table 28–9
RF2	Identification of Link Partner as Auto-Negotiation able	28.2.2.1	M		Reception of 6 to 17 (inclusive) consecutive link pulses separated by at least flp_test_min_timer time but less than flp_test_max_timer time
RF3	First FLP Burst identifying Link Partner as Auto-Negotiation able	28.2.2.1	M		Data recovered is discarded if FLP Burst is incomplete
RF4	First link pulse in an FLP Burst	28.2.2.1	M		Interpreted as a clock link pulse
RF5	Restart of the data_detect_min_timer and data_detect_max_timer	28.2.2.1	M		Detection of a clock link pulse (Figure 28–9)
RF6	Reception of logic one	28.2.2.1	M		Link pulse received between greater than data_detect_min_timer time and less than data_detect_max_timer time after a clock pulse (Figure 28–9)
RF7	Reception of logic zero	28.2.2.1	M		Link pulse received after greater than data_detect_max_timer time after clock pulse, is treated as clock pulse (Figure 28–9)
RF8	FLP Bursts separation	28.2.2.1	M		Conforms to the nlp_test_min_timer and nlp_test_max_timer timing (Figure 28–10)
RF9	Receive Switch function on completion of Auto-Negotiation	28.2.2.3	M		Enables the receive path from the MDI to a single technology-dependent PMA once the highest common denominator has been selected
RF10	Receive Switch function during Auto-Negotiation	28.2.2.3	M		Connects the MDI to the FLP and NLP receivers governed by Figure 28–17 and Figure 28–19, and to the 100BASE-TX and 100BASE-T4 receivers if present
RF11	Signals presented to PMA after connection through Receive Switch from MDI	28.2.2.3	M		Conform to appropriate PHY specifications
RF12	Generation of ability_match, acknowledge_match, and consistency_match	28.2.2.4	M		Responsibility of Receive function in accordance with 28.3.1

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28.5.4.5 Arbitration functions

Item	Feature	Subclause	Status	Support	Value/Comment
AF1	MDI receive connection during Auto-Negotiation, prior to FLP detection	28.2.3.1	M		Connected to the NLP Receive Link Integrity Test state diagram, and the link integrity test functions of 100BASE-TX and/or 100BASE-T4. Not connected to the 10BASE-T or any other PMA
AF2	Parallel detection operational mode selection	28.2.3.1	M		Set link_control=ENABLE for the single PMA indicating link_status=READY when the autoneg_wait_timer expires
AF3	Parallel detection PMA control	28.2.3.1	M		Set link_control=DISABLE to all PMAs except the selected operational PMA and indicate Auto-Negotiation has completed
AF4	Parallel detection setting of Link Partner ability register	28.2.3.1	M		On transition to the FLP LINK GOOD CHECK state from the LINK STATUS CHECK state the Parallel Detection function shall set the bit in the Link Partner ability register (register 5) corresponding to the technology detected by the Parallel Detection function
AF5	Response to renegotiation request	28.2.3.2	M		Disable all technology-dependent link integrity test functions and halt transmit activity until break_link_timer expires
AF6	Auto-Negotiation resumption	28.2.3.2	M		Issue FLP Bursts with Base Page valid in tx_link_code_word[16:1] after break_link_timer expires
AF7	Priority resolution	28.2.3.3	M		Single PMA connected to MDI is enabled corresponding to Technology Ability Field bit common to both Local/Link Partner Device and that has highest priority as defined by Annex 28B
AF8	Effect of receipt of reserved Technology Ability Field bit on priority resolution	28.2.3.3	M		Local Device ignores during priority resolution
AF9	Effect of parallel detection on priority resolution	28.2.3.3	M		Local Device considers technology identified by parallel detection as HCD
AF10	Values for HCD and link_status_[HCD] in the event there is no common technology	28.2.3.3	M		HCD=NULL link_status_[HCD]=FAIL

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28.5.4.5 Arbitration functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
AF11	Message Page to Unformatted Page relationship for non-matching Selector Fields	28.2.3.4	NP:M		Each series of Unformatted Pages is preceded by an Message Page containing a message code that defines how the following Unformatted Page(s) will be interpreted
AF12	Message Page to Unformatted Page relationship for matching Selector Fields	28.2.3.4	NP:M		Use of Message Pages is specified by the Selector Field value
AF13	Transmission of Null message codes	28.2.3.4	NP:M		Sent with NP=0 on completion of all Next Pages while Link Partner continues to transmit valid Next Page information
AF14	Reception of Null message codes	28.2.3.4	NP:M		Recognized as indicating end of Link Partner's Next Page information
AF15	Next Page encoding	28.2.3.4.1	NP:M		Comply with Figure 28–11 and Figure 28–12 for the NP, Ack, MP, Ack2, and T bits
AF16	Message/Unformatted Code Field	28.2.3.4.1	NP:M		D10-D0 encoded as Message Code Field if MP=1 or Unformatted Code Field if MP=0
AF17	NP bit encoding	28.2.3.4.3	NP:M		Logic 0=last page, logic 1=additional Next Page(s) follow
AF18	Message Page bit encoding	28.2.3.4.5	NP:M		Logic 0=Unformatted Page, logic 1=Message Page
AF19	Ack2 bit encoding	28.2.3.4.6	NP:M		Logic 0=cannot comply with message; logic 1= will comply with message
AF20	Toggle	28.2.3.4.7	NP:M		Takes the opposite value of the Toggle bit in the previously exchanged link codeword
AF21	Toggle encoding	28.2.3.4.7	NP:M		Logic zero = previous value of the transmitted link codeword equaled logic one Logic one = previous value of the transmitted link codeword equaled logic zero
AF22	Message Page encoding	28.2.3.4.8	NP:M		If MP=1, link codeword interpreted as Message Page
AF23	Message Code Field	28.2.3.4.9	NP:M		Combinations not shown in Annex 28C are reserved and may not be transmitted
AF24	Unformatted Page encoding	28.2.3.4.10	NP:M		If MP=0, link codeword interpreted as Unformatted Page

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28.5.4.5 Arbitration functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
AF25	Minimum Next Page exchange	28.2.3.4.13	NP:M		If both devices indicate Next Page able, both send a minimum of one Next Page
AF26	Multiple Next Page exchange	28.2.3.4.13	NP:M		If both devices indicate Next Page able, exchange continues until neither Local/Remote Device has additional information; device sends Next Page with Null message code if it has no information to transmit
AF27	Unformatted Page ordering	28.2.3.4.13	NP:M		Unformatted Pages immediately follow the referencing message code in the order specified by the message code
AF28	Next Page Transmit register	28.2.3.4.14	NP:M		Defined in 28.2.4.1.6
AF29	Next Page receive data	28.2.3.4.14	NP:O		May be stored in Auto-Negotiation Link Partner ability register
AF30	Remote Fault sensing	28.2.3.5	RF:M		Optional
AF31	Transmission of RF bit by Local Device	28.2.3.5	M		If Local Device has no method to set RF bit, it transmits RF bit with value of RF bit in Auto-Negotiation advertisement register (4.13)
AF32	RF bit reset	28.2.3.5	M		Once set, the RF bit remains set until successful renegotiation with the base link codeword
AF33	Receipt of Remote Fault indication in base link codeword	28.2.3.5	MII:M		Device sets the Remote Fault bit in the MII status register (1.4) to logic one if MII is present
AF34	Extended Next Page exchange	28.2.3.4	ENP:M		If both device and link partner are ENP able, any NP exchange uses Extended Next Pages

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28.5.4.6 Management function requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	Mandatory MII registers for Auto-Negotiation	28.2.4.1	MII:M		Registers 0, 1, 4, 5, 6
MF2	Optional MII register for Auto-Negotiation	28.2.4.1	MII* NP:M		Register 7
MF3	Auto-Negotiation enable	28.2.4.1.1	MII:M		Set control register Auto-Negotiation Enable bit (0.12)
MF4	Manual Speed/Duplex settings	28.2.4.1.1	MII:M		When bit 0.12 set, control register Speed Detection (0.13) and Duplex Mode (0.8) are ignored, and the Auto-Negotiation function determines link configuration
MF5	Control register (register 0) Restart Auto-Negotiation (0.9) default	28.2.4.1.1	MII:M		PHY returns value of one in 0.9 until Auto-Negotiation has been initiated
MF6	Control register (register 0) Restart Auto-Negotiation (0.9) set	28.2.4.1.1	MII:M		When 0.9 set, Auto-Negotiation will (re)initiate. On completion, 0.9 will be reset by the PHY device. Writing a zero to 0.9 at any time has no effect
MF7	Control register (register 0) Restart Auto-Negotiation (0.9) reset	28.2.4.1.1	MII:M		0.9 is self-clearing; writing a zero to 0.9 at any time has no effect
MF8	Status register (register 1) Auto-Negotiation Complete (1.5) reset	28.2.4.1.2	MII:M		If bit 0.12 reset, or a PHY lacks the ability to perform Auto-Negotiation, (1.5) is reset
MF9	Status register (register 1) Remote Fault (1.4)	28.2.4.1.2	MII:M		Set by the PHY and remains set until either the status register is read or the PHY is reset
MF10	Advertisement register power on default	28.2.4.1.3	MII:M		Selector field as defined in Annex 28A; Ack=0; Technology Ability Field based on MII status register (1.15:11) or logical equivalent
MF11	Link partner ability register read/write	28.2.4.1.4	MII:M		Read only; write has no effect
MF12	Link partner ability register bit definitions	28.2.4.1.4	MII:M		Direct representation of the received link codeword (Figure 28–7)
MF13	Status register (register 1) Auto-Negotiation Complete (1.5) set	28.2.4.1.4	MII:M		Set to logic one upon successful completion of Auto-Negotiation
MF14	Auto-Negotiation expansion register (register 6)	28.2.4.1.5	MII:M		Read only; write has no effect

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28.5.4.6 Management function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF15	Link Partner Auto-Negotiation Able bit (6.0)	28.2.4.1.5	MII:M		Set to indicate that the Link Partner is able to participate in the Auto-Negotiation function
MF16	Page Received bit (6.1) set	28.2.4.1.5	MII:M		Set to indicate that a new link codeword has been received and stored in the Auto-Negotiation Link Partner ability register
MF17	Page Received bit (6.1) reset	28.2.4.1.5	MII:M		Reset on a read of the Auto-Negotiation expansion register (register 6)
MF18	The Next Page Able bit (6.2) set	28.2.4.1.5	NP* MII:M		Set to indicate that the Local Device supports the Next Page function
MF19	The Link Partner Next Page Able bit (6.3) set	28.2.4.1.5	MII:M		Set to indicate that the Link Partner supports the Next Page function
MF20	Parallel Detection Fault bit (6.4) set	28.2.4.1.5	MII:M		Set to indicate that zero or more than one of the NLP Receive Link Integrity Test function, 100BASE-TX, or 100BASE-T4 PMAs have indicated link_status=READY when the autoneg_wait_timer expires
MF21	Parallel Detection Fault bit (6.4) reset	28.2.4.1.5	MII:M		Reset on a read of the Auto-Negotiation expansion register (register 6)
MF22	Link Partner Next Page Storage Location bit	28.2.4.1.5	NPSL * MII:M		Indicates location of Link Partner Next Page
MF23	Receive Next Page Location Able bit	28.2.4.1.5	MII:M		Indicates if Link Partner Next Page Storage Location bit is supported.
MF24	Next Page Transmit register default	28.2.4.1.6	NP* MII:M		On power-up, contains value of 2001 H
MF25	Write to Next Page Transmit register	28.2.4.1.6	NP* MII:M		mr_next_page_loaded set to true
MF26	Absence of management function	28.2.5	NOM:M		Advertised abilities provided through a logical equivalent of mr_adv_ability[16:1]
MF27	Next Page support in absence of MII management	28.2.5	NOM:M		Device provides logical equivalent of mr_np_able, mr_lp_np_able, or mr_next_page_loaded variables in order to set NP bit in transmitted link codeword

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28.5.4.7 Technology-dependent interface

Item	Feature	Subclause	Status	Support	Value/Comment
TD1	PMA_LINK.indication (link_status) values	28.2.6.1.1	M		link_status set to READY, OK or FAIL
TD2	PMA_LINK.indication (link_status) generation	28.2.6.1.2	M		Technology-dependent PMA and NLP Receive Link Integrity Test state diagram (Figure 28–19) responsibility
TD3	PMA_LINK.indication (link_status), effect of receipt	28.2.6.1.3	M		Governed by the state diagram of Figure 28–18
TD4	PMA_LINK.request (link_control) values	28.2.6.1.3	M		link_control set to SCAN_FOR_CARRIER, DISABLE, or ENABLE
TD5	Effect of link_control=SCAN_FOR_CARRIER	28.2.6.2.1	M		PMA to search for carrier and report link_status=READY when carrier is received, but no other actions are enabled
TD6	Effect of link_control=DISABLE	28.2.6.2.1	M		Disables PMA processing
TD7	Effect of link_control=ENABLE	28.2.6.2.1	M		Control passed to a single PMA for normal processing functions
TD8	PMA_LINK.request(link_control) generation	28.2.6.2.2	M		Auto-Negotiation function responsibility in accordance with Figure 28–17 and Figure 28–18
TD9	PMA_LINK.request(link_control) default upon power-on, reset, or release from power-down	28.2.6.2.2	M		link_control = DISABLE state to all technology-dependent PMAs
TD10	PMA_LINK.request(link_control) effect of receipt	28.2.6.2.3	M		Governed by Figure 28–19 and the receiving technology-dependent link integrity test function
TD11	The linkpulse parameter shall	28.2.6.3.1	M		TRUE or FALSE.
TD12	The linkpulse=FALSE shall be used	28.2.6.3.1	M		By the Auto-Negotiation function to indicate that the Receive State Diagram has performed a state transition
TD13	The linkpulse=TRUE shall be used	28.2.6.3.1	M		By the Auto-Negotiation function to indicate that a valid Link Pulse has been received

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28.5.4.7 Technology-dependent interface *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
TD14	The Auto-Negotiation function shall generate linkpulse	28.2.6.3.2	M		To indicate to the PHY how to respond, in accordance with the state diagram of Figure 28–17
TD15	Upon power-on or reset, if Auto-Negotiation is enabled (mr_autoneg_enable=true) the PMA_LINKPULSE.request(FALSE) message shall be	28.2.6.3.2	M		Issued to all technology-dependent PMAs
TD16	The effect of the receipt of linkpulse shall be governed	28.2.6.3.3	M		By the receiving technology-dependent PMA function, based on the intent specified in the primitive semantics

28.5.4.8 State diagrams

Item	Feature	Subclause	Status	Support	Value/Comment
SD1	Adherence to state diagrams	28.3	M		Implement all features of Figure 28–16 to Figure 28–19. Identified options to Figure 28–16 to Figure 28–19 are permitted
SD2	Ambiguous requirements	28.3	M		State diagrams take precedence in defining functional operation
SD3	autoneg_wait_timer	28.3.2	M		Expires 500 ms to 1000 ms after being started
SD4	break_link_timer	28.3.2	M		Expires 1200 ms to 1500 ms after being started
SD5	data_detect_min_timer	28.3.2	M		Expires 15 μs to 47 μs from the last clock pulse
SD6	data_detect_max_timer	28.3.2	M		Expire 78 μs to 100 μs from the last clock pulse
SD7	flp_test_max_timer	28.3.2	M		Expires 165 μs to 185 μs from the last link pulse
SD8	flp_test_min_timer	28.3.2	M		Expires 5 μs to 25 μs from the last link pulse
SD9	interval_timer	28.3.2	M		Expires 55.5 μs to 69.5 μs from each clock pulse and data bit
SD10	link_fail_inhibit_timer (10/100/1000 Mb/s)	28.3.2	!MG:M		Expires 750 ms to 1000 ms after entering the FLP LINK GOOD CHECK state

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28.5.4.8 State diagrams *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
SD11	link_fail_inhibit_timer (MultiGBASE-T devices)	28.3.2	MG:M		Expires 2000 ms to 2250 ms after entering the FLP LINK GOOD CHECK state upon successful master/slave resolution
SD12	nlp_test_max_timer	28.3.2	M		Expires 50 ms to 150 ms after being started if not restarted
SD13	nlp_test_min_timer	28.3.2	!ENP:M		Expires 5 ms to 7 ms after being started if not restarted
SD14	nlp_test_min_timer (with Extended Next Page)	28.3.2	ENP:M		Expires 6.75 ms to 7.25 ms after being started if not restarted
SD15	transmit_link_burst_timer (with no optimized timing)	28.3.1	!OPT:M		Expires 5.7 ms to 22.3 ms after the last transmitted link pulse in an FLP Burst
SD16	transmit_link_burst_timer (with optimized timing and 16-bit pages)	28.3.1	OPT:M		Expires 5.7 ms to 6.8 ms after the last transmitted link pulse in an FLP Burst
SD17	transmit_link_burst_timer (with optimized timing and 48-bit pages)	28.3.1	OPT:M		Expires 1.3 ms to 3.2 ms after the last transmitted link pulse in an FLP Burst containing Extended Next Pages

28.5.4.9 Electrical characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
EC1	Pulses within FLP Bursts	28.4	M		Identical to the characteristics of NLPs and meet the requirements of Figure 14–13

28.5.4.10 Auto-Negotiation annexes

Item	Feature	Annex	Status	Support	Value/Comment
AA1	Selector field, S[4:0] values in the link codeword	Annex 28A	M		Identifies base message type as defined by Table 28A–1
AA2	Selector field reserved combinations	Annex 28A	M		Transmission not permitted
AA3	Relative priorities of the technologies supported by the IEEE 802.3 Selector Field value	28B.3	M		Defined in Annex 28B.3
AA4	Relative order of the technologies supported by IEEE 802.3 Selector Field	28B.3	M		Remain unchanged

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28.5.4.10 Auto-Negotiation annexes *(continued)*

Item	Feature	Annex	Status	Support	Value/Comment
AA5	Addition of new technology	28B.3	M		Inserted into its appropriate place in the priority resolution hierarchy, shifting technologies of lesser priority lower in priority
AA6	Addition of vendor-specific technology	28B.3	M		Priority of IEEE 802.3 standard topologies maintained, vendor-specific technologies to be inserted into an appropriate location
AA7	Message Code Field	Annex 28C	NP:M		Defines how following Unformatted Pages (if applicable) are interpreted
AA8	Order of Unformatted Code Fields within extended Pages	Annex 28C	NP:M		Pages to be in order specified by message code
AA9	Message Code Field reserved combinations	Annex 28C	NP:M		Transmission not permitted
AA10	Auto-Negotiation reserved code 1	28C.1	NP:M		Transmission of M10 to M0 equals 0, not permitted
AA11	Null message code	28C.2	NP:M		Transmitted during Next Page exchange when the Local Device has no information to transmit and Link Partner has additional pages to transmit
AA12	Remote Fault Identifier message code	28C.5	NP:M		Followed by single Unformatted Page to identify fault type with types defined in 28C.5
AA13	Organizationally Unique Identifier message code	28C.6	NP:M		Followed by 4 Unformatted Pages. First Unformatted Page contains most significant 11 bits of OUI or CID (bits 23:13) with MSB in U10; Second Unformatted Page contains next most significant 11 bits of OUI or CID (bits 12:2), with MSB in U10; Third Unformatted Page contains the least significant 2 bits of OUI or CID (bits 1:0) with MSB in U10, bits U8:0 contains user-defined code specific to OUI or CID; Fourth Unformatted Page contains user-defined code specific to OUI or CID

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28.5.4.10 Auto-Negotiation annexes *(continued)*

Item	Feature	Annex	Status	Support	Value/Comment
AA14	PHY Identifier message code	28C.7	NP:M		Followed by 4 Unformatted Pages. First Unformatted Page contains most significant 11 bits of PHY ID (2.15:5) with MSB in U10; Second Unformatted Page contains PHY ID bits 2.4:0 to 3.15:10, with MSB in U10; Third Unformatted Page contains PHY ID bits 3.9:0, with MSB in U10, and U0 contains user-defined code specific to PHY ID; Fourth Unformatted Page contains user-defined code specific to PHY ID
AA15	Auto-Negotiation reserved code 2	28C.8	NP:M		Transmission of M10 to M0 equals 1, not permitted

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28.6 Auto-Negotiation expansion

Auto-Negotiation is designed in a way that allows it to be easily expanded as new technologies are developed. When a new technology is developed, the following things have to be done to allow Auto-Negotiation to support it:

a) The appropriate Selector Field value to contain the new technology has to be selected and allocated.
b) A Technology bit has to be allocated for the new technology within the chosen Selector Field value.
c) The new technology's relative priority within the technologies supported within a Selector Field value has to be established.

Code space allocations are enumerated in Annex 28A, Annex 28B, and Annex 28C. Additions and insertions to the annexes are allowed. No changes to existing bits already defined are allowed.

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29. System considerations for multisegment 100BASE-T networks

NOTE—This clause relates to clauses that are not recommended for new installations. This clause is not recommended for new installations. Since March 2012, maintenance changes are no longer being considered for this clause.

29.1 Overview

This clause provides information on building 100BASE-T networks. The 100BASE-T technology is designed to be deployed in both homogenous 100 Mb/s networks and heterogeneous 10/100 Mb/s mixed CSMA/CD networks. Network topologies can be developed within a single 100BASE-T collision domain, but maximum flexibility is achieved by designing multiple collision domain networks that are joined by bridges and/or routers configured to provide a range of service levels to DTEs. For example, a combined 100BASE-T/10BASE-T system built with repeaters and bridges can deliver dedicated 100 Mb/s, shared 100 Mb/s, dedicated 10 Mb/s, and shared 10 Mb/s service to DTEs. The effective bandwidth of shared services is controlled by the number of DTEs that share the service.

Linking multiple 100BASE-T collision domains with bridges maximizes flexibility. Bridged topology designs can provide single bandwidth (Figure 29–1) or multiple bandwidth (Figure 29–2) services.

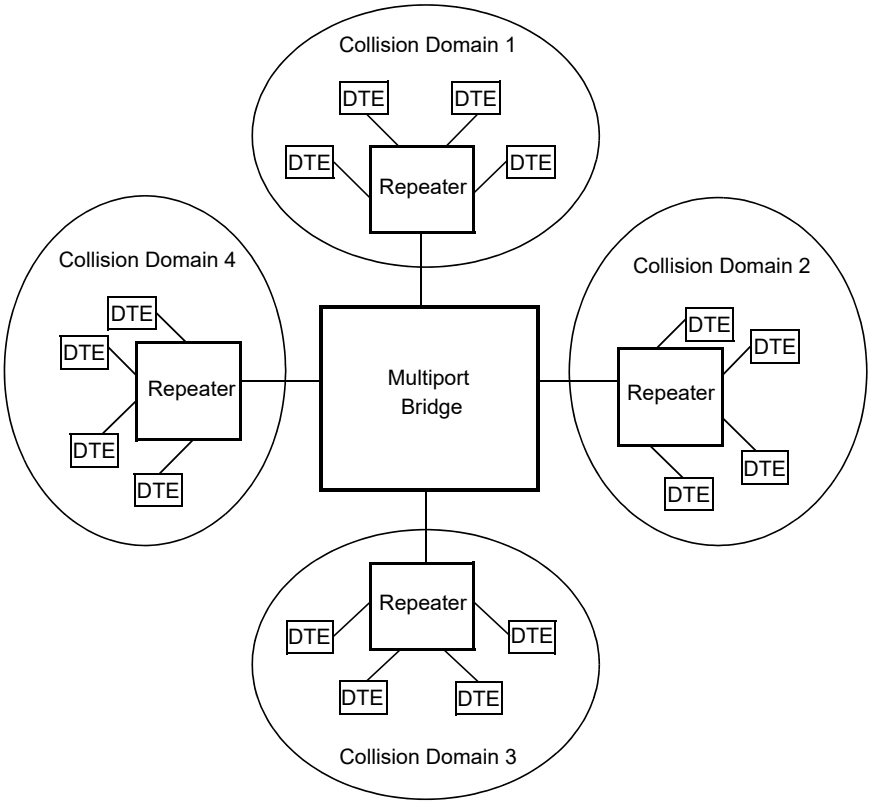

Figure 29–1—100 Mb/s multiple collision domain topology using multiport bridge

Individual collision domains can be linked by single devices (as shown in Figure 29–1 and Figure 29–2) or by multiple devices from any of several transmission systems. The design of multiple-collision-domain networks is governed by the rules defining each of the transmission systems incorporated into the design.

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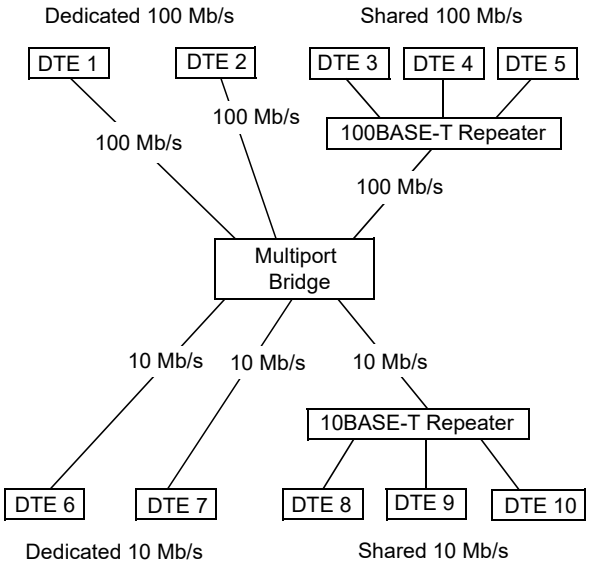

Figure 29–2—Multiple bandwidth, multiple collision domain topology using multiport bridge

The design of shared bandwidth 10 Mb/s collision domains is defined in 13.1 through 13.4; the design of shared bandwidth 100 Mb/s CSMA/CD collision domains is defined in 29.1.1 through 29.3.1.2. The design of 10BASE full duplex LANs is defined in 13.5; the design of full duplex 100BASE-X LANs is defined in 29.4.

29.1.1 Single collision domain multisegment networks

This clause provides information on building 100 Mb/s CSMA/CD multisegment networks within a single collision domain. The proper operation of a CSMA/CD network requires the physical size and number of repeaters to be limited in order to meet the round-trip propagation delay requirements of 4.2.3.2.3 and 4.4.2 and IPG requirements specified in 4.4.2.

This clause provides two network models. Transmission System Model 1 is a set of configurations that have been validated under conservative rules and have been qualified as meeting the requirements set forth above. Transmission System Model 2 is a set of calculation aids that allow those configuring a network to test a proposed configuration against a simple set of criteria that allows it to be qualified. Transmission System Model 2 validates an additional broad set of topologies that are fully functional and do not fit within the simpler, but more restrictive rules of Model 1.

The physical size of a CSMA/CD network is limited by the characteristics of individual network components. These characteristics include the following:

a) Media lengths and their associated propagation time delay
b) Delay of repeater units (startup, steady-state, and end of event)
c) Delay of MAUs and PHYs (startup, steady-state, and end of event)
d) Interpacket gap shrinkage due to repeater units
e) Delays within the DTE associated with the CSMA/CD access method
f) Collision detect and deassertion times associated with the MAUs and PHYs

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Table 29–1 summarizes the delays for 100BASE-T media segments. For more detailed information on the delays associated with individual 100BASE-T components, see

MII: Annex 22A
100BASE-T2:32.12
100BASE-T4:23.11
100BASE-TX:24.6
100BASE-FX: ISO/IEC 9314-3:1990
Repeater:27.3

Table 29–1—Delays for network media segments Model 1

Media type	Maximum number of PHYs per segment	Maximum segment length (m)	Maximum medium round-trip delay per segment (BT)
Balanced cable link segment 100BASE-T	2	100	114
Fiber link segment	2	412	412

29.1.2 Repeater usage

Repeaters are the means used to connect segments of a network medium together into a single collision domain. Different signaling systems (i.e., 100BASE-T2, 100BASE-T4, 100BASE-TX, 100BASE-FX) can be joined into a common collision domain using repeaters. Bridges can also be used to connect different signaling systems; however, if a bridge is so used, each system connected to the bridge will be a separate collision domain.

Two types of repeaters are defined for 100BASE-T (see Clause 27). Class I repeaters are principally used to connect unlike physical signaling systems and have internal delays such that only one Class I repeater can reside within a single collision domain when maximum cable lengths are used (see Figure 29–4). Class II repeaters typically provide ports for only one physical signaling system type (e.g., 100BASE-TX but not 100BASE-T4) and have smaller internal delays so that two such repeaters may reside within a given collision domain when maximum cable lengths are used (see Figure 29–6). Cable length can be sacrificed to add additional repeaters in a collision domain (see 29.3).

29.2 Transmission System Model 1

The following network topology constraints apply to networks using Transmission System Model 1.

a) All balanced cable (copper) segments less than or equal to 100 m each.
b) Fiber segments less than or equal to 412 m each.
c) MII cables for 100BASE-T shall not exceed 0.5 m each. When evaluating system topology, MII cable delays need not be accounted for separately. Delays attributable to the MII are incorporated into DTE and repeater component delays.

29.3 Transmission System Model 2

The physical size and number of topological elements in a 100BASE-T network is limited primarily by round-trip collision delay. A network configuration has to be validated against collision delay using a net-

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work model. Since there are a limited number of topology models for any 100BASE-T collision domain, the modeling process is quite straightforward and can easily be done either manually or with a spreadsheet.

The model proposed here is derived from the one presented in 13.4. Modifications have been made to accommodate adjustments for DTE, repeater, and cable speeds.

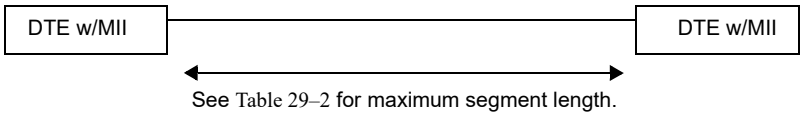

Figure 29–3—Model 1: Two DTEs, no repeater

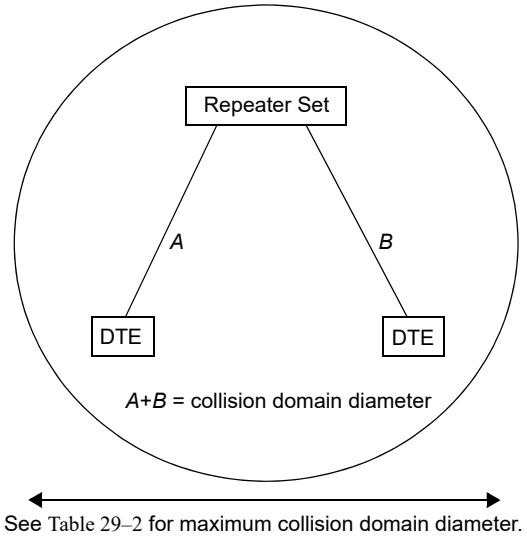

Figure 29–4—Model 1: Single repeater

Table 29–2—Maximum Model 1 collision domain diameter[a]

Model	Balanced cabling (copper)	Fiber	Balanced cabling & fiber (T2 or T4 and FX)	Balanced cabling & fiber (TX and FX)
DTE-DTE (see Figure 29–3)	100	412	NA	NA
One Class I repeater (see Figure 29–4)	200	272	231[a]	260.8[a]
One Class II repeater (see Figure 29–4)	200	320	304[b]	308.8[b]
Two Class II repeaters (see Figure 29–5)	205	228	236.3[c]	216.2[c]

[a]Assumes 100 m of balanced cabling and one fiber link.
[b]This entry included for completeness. It may be impractical to construct a T4 to FX class II repeater.
[c] Assumes 105 m of balanced cabling and one fiber link.

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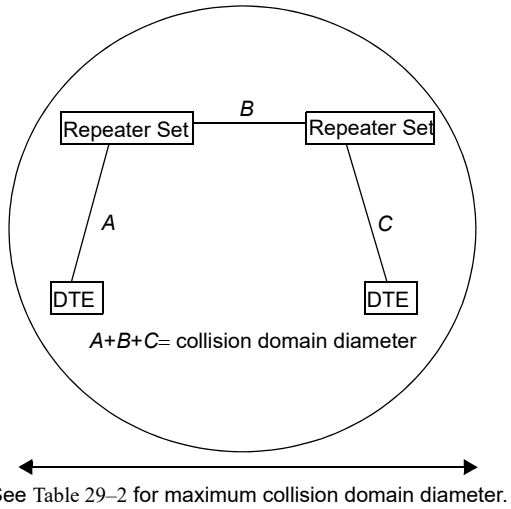

Figure 29–5—System Model 1: Two Class II repeaters

29.3.1 Round-trip collision delay

For a network to be valid, it has to be possible for any two DTEs on the network to contend for the network at the same time. Each station attempting to transmit has to be notified of the contention by the returned "collision" signal within the "collision window" (see 4.1.2.2 and 5.2.2.1.2). Additionally, the maximum length fragment created has to contain less than 512 bits after the start-of-frame delimiter (SFD). These requirements limit the physical diameter (maximum distance between DTEs) of a network. The maximum round-trip delay has to be qualified between all pairs of DTEs in the network. In practice this means that the qualification needs to be done between those that, by inspection of the topology, are candidates for the longest delay. The following network modeling methodology is provided to assist that calculation.

29.3.1.1 Worst-case path delay value (PDV) selection

The worst-case path through a network to be validated shall be identified by examination of aggregate DTE delays, cable delays, and repeater delays. The worst case consists of the path between the two DTEs at opposite ends of the network that have the longest round-trip time. Figure 29–6 and Figure 29–7 show schematic representations of one-repeater and two-repeater paths.

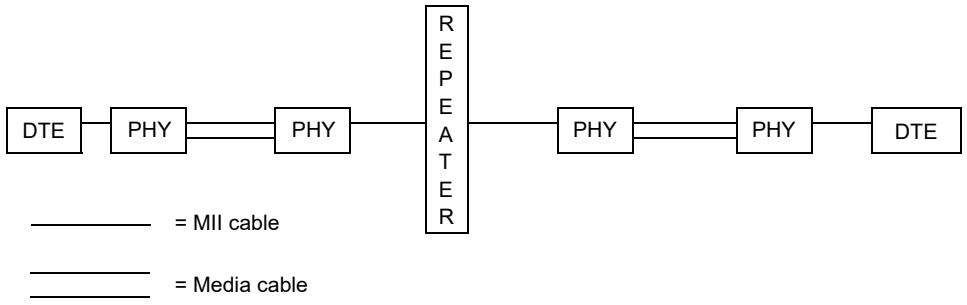

Figure 29–6—System Model 2: Single repeater

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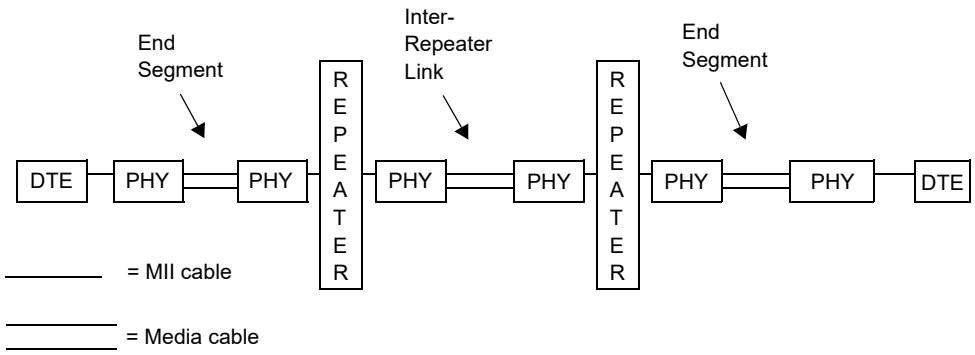

Figure 29–7—System Model 2-2: Two repeaters

29.3.1.2 Worst-case PDV calculation

Once a set of paths is chosen for calculation, each shall be checked for validity against the following formula:

$$PDV = \sum\text{link delays (LSDV)} + \sum\text{repeater delays} + \text{DTE delays} + \text{safety margin}$$

Values for the formula variables are determined by the following method:

a) Determine the delay for each link segment (Link Segment Delay Value, or LSDV), including inter-repeater links, using the formula

$$LSDV = 2 \text{ (for round-trip delay)} \times \text{segment length} \times \text{cable delay for this segment}$$

NOTE 1—Length is the sum of the cable lengths between the PHY interfaces at the repeater and the farthest DTE for End Segments plus the sum of the cable lengths between the repeater PHY interfaces for Inter-Repeater Links. All measurements are in meters.

NOTE 2—Cable delay is the delay specified by the manufacturer or the maximum value for the type of cable used as shown in Table 29–3. For this calculation, cable delay needs to be specified in bit times per meter (BT/m). Table 29–4 can be used to convert values specified relative to the speed of light (%c) or nanoseconds per meter (ns/m).

NOTE 3—When actual cable lengths or propagation delays are not known, use the Max delay in bit times as specified in Table 29–3 for copper cables. Delays for fiber should be calculated, as the value found in Table 29–3 will be too large for most applications.

b) Sum together the LSDVs for all segments in the path.

c) Determine the delay for each repeater in the path. If model-specific data are not available from the manufacturer, determine the class of each repeater (I or II) and enter the appropriate default value from Table 29–3.

d) MII cables for 100BASE-T shall not exceed 0.5 m each. When evaluating system topology, MII cable delays need not be accounted for separately. Delays attributable to the MII are incorporated into DTE and repeater component delays.

e) Use the DTE delay value shown in Table 29–3 unless your equipment manufacturer defines a different value.

f) Decide on appropriate safety margin—0 to 5 bit times—for the PDV calculation. Safety margin is used to provide additional margin to accommodate unanticipated delay elements, such as extra-long connecting cable runs between wall jacks and DTEs. (A safety margin of 4 BT is recommended.)

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g) Insert the values obtained through the calculations above into the following formula to calculate the PDV. (Some configurations may not use all the elements of the formula.)

PDV = ∑link delays (LSDV) + ∑repeater delays + DTE delay + safety margin

h) If the PDV is less than 512, the path is qualified in terms of worst-case delay.

i) Late collisions and/or CRC errors are indicators that path delays exceed 512 BT.

Table 29–3—Network component delays, Transmission System Model 2

Component	Round trip delay in bit times per meter	Maximum round trip delay in bit times
Two TX/FX DTEs		100
Two T4 DTEs		138
Two T2 DTEs		96
One T2 or T4 and one TX/FX DTE[a]		127
Cat 3 cabling segment	1.14	114 (100 m)
Cat 4 cabling segment	1.14	114 (100 m)
Cat 5 cabling segment	1.112	111.2 (100 m)
STP cabling segment	1.112	111.2 (100 m)
Fiber optic cabling segment	1.0	412 (412 m)
Class I repeater		140
Class II repeater with all ports TX/FX		92
Class II repeater with any port T4		67
Class II repeater with any port T2		90

[a] Worst-case values are used (TX/FX values for MAC transmit start and MDI input to collision detect; T4 value for MDI input to MDI output).

29.4 Full duplex 100 Mb/s topology limitations

Unlike half duplex CSMA/CD networks, the physical size of full duplex 100 Mb/s CSMA/CD networks is not limited by the round-trip collision propagation delay. Instead, the maximum link length between DTEs is limited only by the signal transmission characteristics of the specific cable, as specified in Table 29–5.

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Table 29–4—Conversion table for cable delays

Speed relative to *c*	ns/m	BT/m
0.4	8.34	0.834
0.5	6.67	0.667
0.51	6.54	0.654
0.52	6.41	0.641
0.53	6.29	0.629
0.54	6.18	0.618
0.55	6.06	0.606
0.56	5.96	0.596
0.57	5.85	0.585
0.58	5.75	0.575
0.5852	5.70	0.570
0.59	5.65	0.565
0.6	5.56	0.556
0.61	5.47	0.547
0.62	5.38	0.538
0.63	5.29	0.529
0.64	5.21	0.521
0.65	5.13	0.513
0.654	5.10	0.510
0.66	5.05	0.505
0.666	5.01	0.501
0.67	4.98	0.498
0.68	4.91	0.491
0.69	4.83	0.483
0.7	4.77	0.477
0.8	4.17	0.417
0.9	3.71	0.371

Table 29–5—Link segment length limits; 100 Mb/s full duplex segments

Cable type	Maximum link segment length
100BASE-TX (UTP, STP per Clause 25)	100 m
100BASE-FX (multimode fiber per Clause 26)	2000 m
100BASE-T2 (UTP per Clause 32)	100 m

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30. Management

30.1 Overview

This clause provides the Layer Management specification for DTEs, repeaters, MAUs, and Midspans based on the CSMA/CD access method. The clause is produced from the ISO framework additions to Clause 5, Layer Management; Clause 19, Repeater Management; and Clause 20, MAU Management. It incorporates additions to the objects, attributes, and behaviours to support 100 Mb/s, 1000 Mb/s and 10 Gb/s, full duplex operation, MAC Control, Link Aggregation, DTE Power via MDI, Power over Data Lines, subscriber access networks, and the Link Layer Discovery Protocol (LLDP) IEEE 802.3 Organizationally Specific TLVs. The objects, attributes, and behaviours to support Link Aggregation are deprecated by IEEE Std 802.1AX-2008.

The layout of this clause takes the same form as 5.1, 5.2, and Clause 19, and Clause 20, although with equivalent subclauses grouped together. It identifies a common management model and framework applicable to IEEE 802.3 managed elements, identifies those elements and defines their managed objects, attributes, and behaviours in a protocol-independent language.

This clause provides the Layer Management specification for DTEs, repeaters, and MAUs based on the CSMA/CD access method. It defines facilities composed of a set of statistics and actions needed to provide IEEE 802.3 Management services. The information in this clause should be used in conjunction with the Procedural Model defined in 4.2.7 through 4.2.10. The Procedural Model provides a formal description of the relationship between the CSMA/CD Layer Entities and the Layer Management facilities.

This management specification has been developed in accordance with the OSI management architecture as specified in the ISO Management Framework document, ISO/IEC 7498-4:1989. It is independent of any particular management application or management protocol.

The management facilities defined in this standard may be accessed both locally and remotely. Thus, the Layer Management specification provides facilities that can be accessed from within a station or can be accessed remotely by means of a peer-management protocol operating between application entities.

In CSMA/CD no peer management facilities are necessary for initiating or terminating normal protocol operations or for handling abnormal protocol conditions. Since these activities are subsumed by the normal operation of the protocol, they are not considered to be a function of Layer Management and are, therefore, not discussed in this clause.

Implementation of part or all of Layer Management is not a requirement for conformance to any other clause of this standard.

The intent of this standard is to furnish a management specification that can be used by the wide variety of different devices that may be attached to an Ethernet network. Thus, a comprehensive list of management facilities is provided.

The improper use of some of the facilities described in this clause may cause serious disruption of the network. In accordance with ISO management architecture, any necessary security provisions should be provided by the Agent in the Local System Environment. This can be in the form of specific security features or in the form of security features provided by the peer communication facilities.

The device that connects directly to the media is called MAU for 10 Mb/s operation and its equivalent is the combined PMA and PMD sublayers at higher operating speeds. Because this clause defines management for use at many speeds, it needs to be able to refer to MAUs and the PMA and PMD sublayer combination as a group. Therefore, in this clause, the term MAU will include PMA and PMD sublayers as well as MAUs, except in those instances where it is explicitly restricted to 10 Mb/s.

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30.1.1 Scope

This clause includes selections from Clause 5, Clause 19, and Clause 20. It is intended to be an entirely equivalent specification for the management of 10 Mb/s DTEs, 10 Mb/s baseband repeater units, and 10 Mb/s integrated MAUs. It incorporates additions to the objects, attributes, and behaviours to support subsequent additions to this standard. Implementations of management for DTEs, repeater units, and embedded MAUs should follow the requirements of this clause (e.g., a 10 Mb/s implementation should incorporate the attributes to indicate that it is not capable of 100 Mb/s or 1000 Mb/s operation; half duplex DTE should incorporate the attributes to indicate that it is not capable of full duplex operation, etc.).

For 10 Mb/s ports without integral MAUs, attributes are provided for characteristics observable from the AUI of the connected DTE or repeater. Direct management of AUI MAUs that are external to their respective DTEs or repeaters is beyond the scope of this standard.

The managed objects within this standard are defined in terms of their behaviour, attributes, actions, notifications, and packages in accordance with IEEE 802.1 and ISO standards for network management. Managed objects are grouped into mandatory and optional packages.

This specification is defined to be independent of any particular management application or management protocol. The means by which the managed objects defined in this standard are accessed is beyond the scope of this standard.

30.1.2 Relationship to objects in IEEE 802.1F

The following managed object classes, if supported by an implementation, shall be as specified in IEEE Std 802.1F-1993 (withdrawn): ResourceTypeID, EWMAMetricMonitor.

oResourceTypeID

This object class is mandatory and shall be implemented as defined in IEEE 802.1F. This object is bound to oMAC-Entity, oRepeater, oMidSpan, and oMAU as defined by the NAMEBINDINGs. Note that the binding to oMAU is mandatory only when MII is present. The Entity Relationship Diagrams, Figure 30–3, Figure 30–4, and Figure 30–5 show these bindings pictorially.

oEWMAMetricMonitor

This object class is optional. When implemented, it shall be implemented as defined in IEEE 802.1F, subject to the specific requirements described below. This object is bound to system as defined by the NAMEBINDINGs.

Implementations of IEEE 802.3 Management that support the oEWMAMetricMonitor managed object class are required to support values of granularity period as small as one second. Implementations are required to support at least one sequence of low and high thresholds. The granularity period may be set to equal to the moving time period as a minimal conformant implementation.

30.1.3 Systems management overview

Within the ISO Open Systems Interconnection (OSI) architecture, the need to handle the special problems of initializing, terminating, and monitoring ongoing activities and assisting in their operations, as well as handling abnormal conditions, is recognized. These needs are collectively addressed by the systems management component of the OSI architecture.

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A management protocol is required for the exchange of information between systems on a network. This management standard is independent of any particular management protocol.

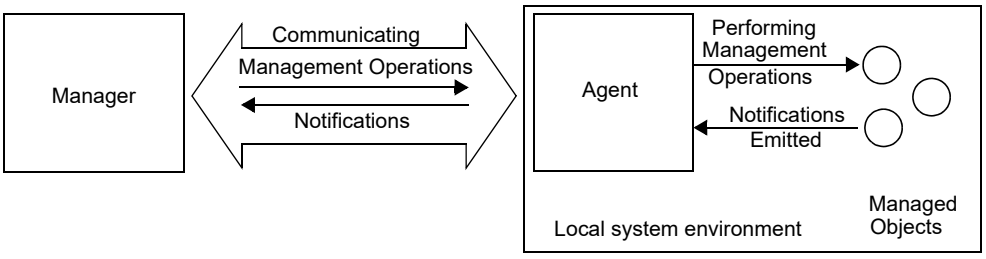
This management standard, in conjunction with the management standards of other layers, provides the means to perform various management functions. IEEE 802.3 Management collects information needed from the MAC and Physical Layers and the devices defined in IEEE 802.3. It also provides a means to exercise control over those elements.

The relationship between the various management entities and the layer entities according to the ISO model is shown in Figure 30–1.

30.1.4 Management model

This standard describes management of DTEs, repeaters, and integrated MAUs in terms of a general model of management of resources within the open systems environment. The model, which is described in ISO/IEC 10040:1992, is briefly summarized here.

Management is viewed as a distributed application modeled as a set of interacting management processes. These processes are executed by systems within the open environment. A managing system executes a managing process that invokes management operations. A managed system executes a process that is receptive to these management operations and provides an interface to the resources to be managed. A managed object is the abstraction of a resource that represents its properties as seen by (and for the purpose of) management. Managed objects respond to a defined set of management operations. Managed objects are also capable of emitting a defined set of notifications. This interaction of processes is shown in Figure 30–1.



NOTE—This figure is drawn from Figure 1 of ISO/IEC 10040:1992, Information technology—Open Systems Interconnection—Systems management overview. In the event of any conflict, the depiction in ISO/IEC 10040:1992 takes precedence.

Figure 30–1—Interaction between manager, agent, and objects

A managed object is a management view of a resource. The resource may be a logical construct, function, physical device, or anything subject to management. Managed objects are defined in terms of four types of elements:

a) *Attributes.* Data-like properties (as seen by management) of a managed object.
b) *Actions.* Operations that a managing process may perform on an object or its attributes.
c) *Notifications.* Unsolicited reports of events that may be generated by an object.
d) *Behaviour.* The way in which managed objects, attributes, and actions interact with the actual resources they model and with each other.

The above items are defined in 30.3 through 30.16.1 of this clause in terms of the template requirements of ISO/IEC 10165-4:1991.

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Some of the functions and resources within IEEE 802.3 devices are appropriate targets for management. They have been identified by specifying managed objects that provide a management view of the functions or resources. Within this general model, the IEEE 802.3 device is viewed as a managed device. It performs functions as defined by the applicable standard for such a device. Managed objects providing a view of those functions and resources appropriate to the management of the device are specified. The purpose of this standard is to define the object classes associated with the devices in terms of their attributes, operations, notifications, and behaviour.

30.2 Managed objects

30.2.1 Introduction

This clause identifies the Managed Object classes for IEEE 802.3 components within a managed system. It also identifies which managed objects and packages are applicable to which components.

All counters defined in this specification are assumed to be wrap-around counters. Wrap-around counters are those that automatically go from their maximum value (or final value) to zero and continue to operate. These unsigned counters do not provide for any explicit means to return them to their minimum (zero), i.e., reset. Because of their nature, wrap-around counters should be read frequently enough to avoid loss of information. When a counter has a maximum increment rate specified at one speed of operation, and that counter is appropriate to a higher speed of operation, then the maximum increment rate at that higher speed of operation is

$$\text{maximum increment rate specified} \times \left(\frac{\text{higher speed of operation in Mb/s}}{\text{specified speed of operation in Mb/s}} \right) \tag{30–1}$$

unless otherwise indicated.

30.2.2 Overview of managed objects

Managed objects provide a means to

— Identify a resource
— Control a resource
— Monitor a resource

30.2.2.1 Text description of managed objects

In case of conflict, the formal behaviour definitions in 30.3, 30.4, 30.5, 30.6, and 30.7 take precedence over the text descriptions in this subclause.

oAggPortDebugInformation

If oAggregator is implemented, a single instance of oAggPortDebugInformation may be contained within oAggregationPort. This managed object class provides optional additional information that can assist with debugging and fault finding in Systems that support Link Aggregation.

NOTE—This object is deprecated by IEEE Std 802.1AX-2008.

oAggPortStats

If oAggregator is implemented, a single instance of oAggPortStats may be contained within oAggregationPort. This managed object class

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provides optional additional statistics related to LACP and Marker protocol activity on an instance of an Aggregation Port that is involved in Link Aggregation.

NOTE—This object is deprecated by IEEE Std 802.1AX-2008.

oAggregationPort If oAggregator is implemented, oAggregationPort is contained within oAggregator. An instance of this managed object class is present for each Aggregation Port that is part of the aggregation represented by the oAggregator instance. This managed object class provides the basic management controls necessary to allow an instance of an Aggregation Port to be managed, for the purposes of Link Aggregation.

NOTE—This object is deprecated by IEEE Std 802.1AX-2008.

oAggregator If implemented, oAggregator is the top-most managed object class of the DTE containment tree shown in Figure 30–4. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this International Standard. The oAggregator managed object class provides the management controls necessary to allow an instance of an Aggregator to be managed.

NOTE—This object is deprecated by IEEE Std 802.1AX-2008.

oAutoNegotiation The managed object of that portion of the containment trees shown in Figure 30–4 and Figure 30–5. The attributes, notifications, and actions defined in 30.6 are contained within the MAU managed object.

oGroup The group managed object class is a view of a collection of repeater ports.

oEXTENSION If implemented, oEXTENSION is contained within oMACControlEntity. The oEXTENSION managed object class provides the management controls necessary to allow an instance of the MAC Control EXTENSION function to be managed.

oLldpXdot3Config The top-most managed object class of the Link Layer Discovery Protocol (LLDP) containment tree shown in Figure 30–6. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this standard.

oLldpXdot3LocSystemsGroup
If oLldpXdot3Config is implemented, a single instance of oLldpXdot3LocSystemsGroup may be contained within oLldpXdot3Config. This managed object class provides the LLDP local system information.

oLldpXdot3RemSystemsGroup
If oLldpXdot3Config is implemented, a single instance of oLldpXdot3RemSystemsGroup may be contained within oLldpXdot3Config. This managed object class provides the LLDP remote system information.

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oMACControlEntity If implemented, and if oOAM is implemented, a single instance of oMACControlEntity is contained within oOAM. Otherwise, if implemented, and if oAggregator is implemented, oMACControlEntity is contained within oAggregator. Otherwise, if implemented, oMACControlEntity becomes the top-most managed object class of the DTE containment tree shown in Figure 30–4. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this International Standard.

oMACControlFunctionEntity
If implemented, oMACControlFunctionEntity is contained within oMACControlEntity. The oMACControlFunctionEntity managed object class provides the management controls necessary to allow an instance of the MAC Control PAUSE function to be managed.

oMACEntity If oMACControlEntity is implemented, oMACEntity is contained within oMACControlEntity. Otherwise, if oOAM is implemented, oMACEntity is contained within oOAM. Otherwise, if oAggregator is implemented, oMACEntity is contained within oAggregator. Otherwise, oMACEntity becomes the top-most managed object class of the DTE containment tree shown in Figure 30–3. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this International Standard. If oMACMergeEntity is implemented, the oMACEntity for the express MAC (eMAC) and the oMACEntity for the preemptable MAC (pMAC) are connected to an instance of oMACMergeEntity.

oMACMergeEntity If implemented, a single instance of oMACMergeEntity is contained within oMACEntity for an express MAC (eMAC) and oMACEntity for a preemptable MAC (pMAC) (see Clause 99). oMACMergeEntity managed object class provides the management controls necessary for the MAC Merge sublayer.

oMAU The managed object of that portion of the containment trees shown in Figure 30–3 and Figure 30–4. The attributes, notifications, and actions defined in 30.5 are contained within the MAU managed object. Neither counter values nor the value of MAUAdminState is required to be preserved across events involving the loss of power.

oMidSpan The top-most managed object class of the Midspan containment tree shown in Figure 30–5. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this standard.

oMPCP If implemented, oMPCP is contained within oMACControlEntity. The oMPCP managed object class provides the management controls necessary to allow an instance of the Multipoint MAC Control function to be managed.

oOAM If implemented, and if oAggregator is implemented, oOAM is contained within oAggregator. An instance of this managed object class is present for each Aggregation Port that is part of the aggregation represented by the oAggregator instance. Otherwise, if implemented, oOAM becomes the top-most managed object class of the DTE containment tree shown in Figure 30–3. Note that this managed object class may be contained

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within another superior managed object class. Such containment is expected, but is outside the scope of this International Standard.

oOMPEmulation If implemented, oOMPEmulation is contained within oMACEntity. The oOMPEmulation managed object class provides the management controls necessary to allow an instance of an OMPEmulation sublayer to be managed.

oPHYEntity If oOMPEmulation is implemented, oPHYEntity is contained within oOMPEmulation. If oMACMergeEntity is implemented, oPHYEntity is contained within oMACMergeEntity. Otherwise oPHYEntity is contained within oMACEntity. Many instances of oPHYEntity may coexist within one instance of oMACEntity or oMACMergeEntity; however, only one PHY may be active for data transfer to and from the MAC at any one time. oPHYEntity is the managed object that contains the MAU, PAF, PLCA, PSE, and PoDLPSE managed objects in a DTE.

oPAF The oPAF managed object class provides the management controls necessary to allow an instance of a PME aggregation function (PAF) to be managed. The PAF managed object class also provides a view of a collection of PMEs.

oPLCA If implemented, oPLCA is contained within oPHYEntity. The oPLCA managed object class provides the management controls necessary to allow an instance of a PLCA RS to be managed.

oPME The oPME managed object class provides the management controls necessary to allow an instance of a PME to be managed. The oPAF managed object contains the PME managed object in a DTE.

oPoDLPSE The managed object of that portion of the containment trees shown in Figure 30–3. The attributes, notifications, and actions defined in 30.15 are contained within the PoDLPSE managed object.

oPSE The managed object of that portion of the containment trees shown in Figure 30–3, Figure 30–4, and Figure 30–5. This managed object class provides the attributes, actions, and notifications required for management of a PD system.

oPSEGroup The PSE Group managed object class is a view of a collection of PSEs.

oRepeater The top-most managed object class of the repeater containment tree shown in Figure 30–4. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this standard.

oRepeaterMonitor A managed object class called out by IEEE Std 802.1F-1993. See 30.1.2, oEWMAMetricMonitor.

oRepeaterPort The repeater port managed object class provides a view of the functional link between the data transfer service and a single PMA. The attributes associated with repeater port deal with the monitoring of traffic being handled by the repeater from the port and control of the operation of the port. The Port Enable/Disable function as reported by portAdminState is preserved across events involving loss of power. The oRepeaterPort managed object contains the MAU managed object in a repeater set.

NOTE—Attachment to nonstandard PMAs is outside the scope of this standard.

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oResourceTypeID	A managed object class called out by IEEE Std 802.1F-1993. It is used within this clause to identify manufacturer, product, and revision of managed components that implement functions and interfaces defined within IEEE 802.3. The Clause 22 MII or Clause 35 GMII specifies two registers to carry PHY Identifier (22.2.4.3.1), which provides succinct information sufficient to support oResourceTypeID.
oTimeSync	If implemented, oTimeSync is contained within oPHYEntity. The oTimeSync managed object class provides the controls neccessary to manage the instance of the TimeSync function.
oWIS	The managed object of that portion of the containment tree shown in Figure 30–3. The attributes defined in 30.8 are contained within the oMAU managed object.

30.2.2.2 Functions to support management

Functions are defined in other clauses that facilitate managed operation. The functions in other clauses that facilitate managed operation are referenced from the text of this management clause.

30.2.2.2.1 DTE MAC sublayer functions

A hierarchical order has been established for DTE MAC reception-related error statistics such that, when multiple error statuses can be associated with one frame, only one status is returned to the upper client sublayer. This hierarchy in descending order is as follows:

— frameTooLong
— alignmentError
— frameCheckError
— lengthError

The counters are primarily incremented based on the status returned to the MAC client; therefore, the hierarchical order of the counters is determined by the order of the status. Frame fragments are not included in any of the statistics unless otherwise stated. In implementing any of the specified actions, receptions and transmissions that are in progress are completed before the action takes effect.

30.2.2.2.2 Repeater functions

The Repeater Port Object class contains seven functions which are defined in this clause and are used to collect statistics on the activity received by the port. The relationship of the functions to the repeater port and to the port attributes is shown in Figure 30–2.

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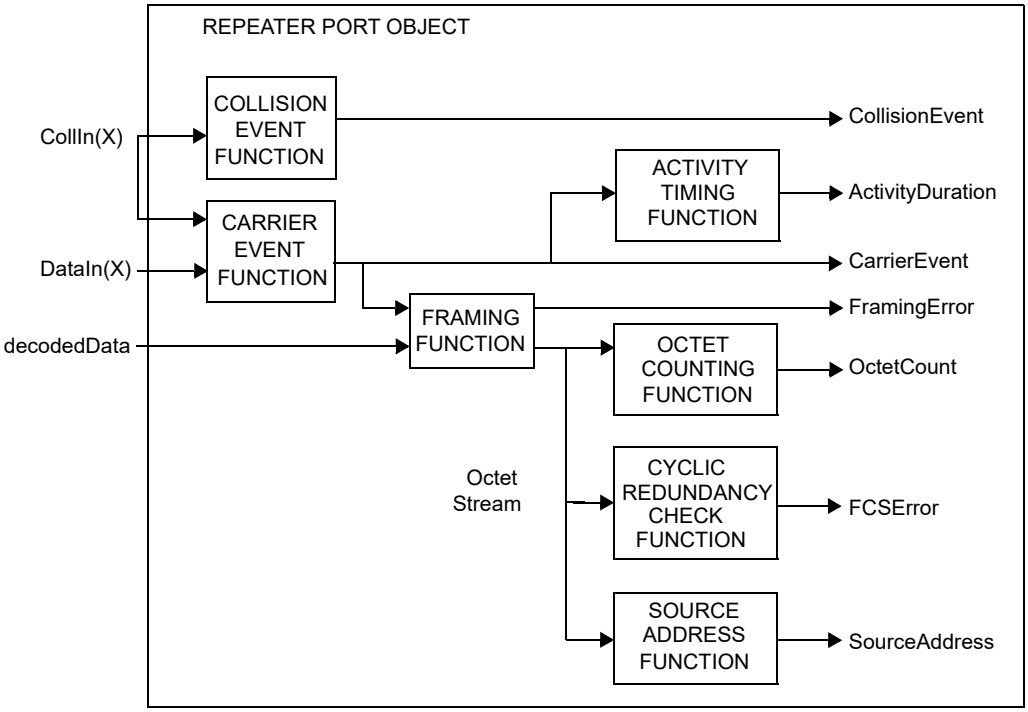

Figure 30–2—Functions relationship

Activity Timing function

The Activity Timing function measures the duration of the assertion of the CarrierEvent signal. For 10 Mb/s repeaters, this duration value has to be adjusted by removing the value of Carrier Recovery Time (see 9.5.6.5) to obtain the true duration of activity on the network. The output of the Activity Timing function is the ActivityDuration value, which represents the duration of the CarrierEvent signal as expressed in units of bit times.

Carrier Event function

For 10 Mb/s repeaters the Carrier Event function for port N asserts the CarrierEvent signal when the repeater exits the IDLE state (see Figure 9–2) and the port has been determined to be port N. It deasserts the CarrierEvent signal when, for a duration of at least Carrier Recovery Time (see 9.5.6.5), both the DataIn(N) variable has the value II and the CollIn(N) variable has the value –SQE. The value N is the port assigned at the time of transition from the IDLE state. For 100 and 1000 Mb/s repeaters the Carrier Event function for port N asserts the CarrierEvent signal when the repeater exits the IDLE state of the repeater state diagram (Figure 27–2 and Figure 41–2) and the port has been determined to be port N. The Carrier Event function for Port N deasserts the CarrierEvent signal when the repeater enters the IDLE state of the repeater state diagram (Figure 27–2 and Figure 41–2).

Collision Event function

The Collision Event function asserts the CollisionEvent signal when a

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collision is detected at a repeater port. For a 10 Mb/s repeater port this is indicated by the CollIn(X) variable having the value SQE. For a 100 and 1000 Mb/s repeater port this is indicated by entering the COLLISION COUNT INCREMENT state of the partition state diagram (Figure 27–8 and Figure 41–4). The CollisionEvent signal remains asserted until the assertion of any CarrierEvent signal due to the reception of the following event.

Cyclic Redundancy Check function

The Cyclic Redundancy Check function verifies that the sequence of octets output by the Framing function contains a valid Frame Check Sequence Field. The Frame Check Sequence Field is the last four octets received from the output of the Framing function. The algorithm for generating an FCS from the octet stream is specified in 3.2.9. If the FCS generated according to this algorithm is not the same as the last four octets received from the Framing function, then the FCSError signal is asserted. The FCSError signal is cleared and the Cyclic Redundancy Check function is reinitialized upon the assertion of the CarrierEvent signal due to the reception of the following event and, additionally in the case of a frame burst on a 1000 Mb/s network, upon the recognition of a valid Start of Packet delimiter (see 35.2.3.6), once the duration of the CarrierEvent is greater than or equal to slotTime.

Framing function

The Framing function recognizes the boundaries of an incoming frame by monitoring the CarrierEvent signal and the decoded data stream. Data bits are accepted while the CarrierEvent signal is asserted. The framing function delineates frames by stripping the Start of Packet delimiter (see 35.2.3.6), preamble, Start of frame delimiter, End of Packet delimiter (see 35.2.3.6), and any Carrier Extend from the received data stream. The remaining bits of each frame are aligned along octet boundaries. If there is not an integral number of octets, then FramingError shall be asserted. The FramingError signal is cleared upon the assertion of the CarrierEvent signal due to the reception of the following event. For 1000 Mb/s repeaters, the data stream shall continue until the end of the CarrierEvent signal or upon the recognition of a valid Start of Packet delimiter once the duration of the CarrierEvent is greater than or equal to slotTime. Such a Start of Packet delimiter will begin a new data stream.

Octet Counting function

The Octet Counting function counts the number of complete octets received from the output of the framing function. The output of the octet counting function is the OctetCount value. The OctetCount value is reset to zero upon the assertion of the CarrierEvent signal due to the reception of the following event and, additionally in the case of a frame burst on a 1000 Mb/s network, upon the recognition of a valid Start of Packet delimiter (see 35.2.3.6), once the duration of the CarrierEvent is greater than or equal to slotTime.

Source Address function

The Source Address function extracts octets from the stream output by the framing function. The seventh through twelfth octets shall be extracted from the octet stream and output as the SourceAddress variable. The SourceAddress variable is set to an invalid state upon the

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assertion of the CarrierEvent signal due to the reception of the following event and, additionally in the case of a frame burst on a 1000 Mb/s network, upon the recognition of a valid Start of Packet delimiter (see 35.2.3.6), once the duration of the CarrierEvent is greater than or equal to slotTime.

30.2.3 Containment

A containment relationship is a structuring relationship for managed objects in which the existence of a managed object is dependent on the existence of a containing managed object. The contained managed object is said to be the subordinate managed object, and the containing managed object the superior managed object. The containment relationship is used for naming managed objects. The local containment relationships among object classes are depicted in the entity relationship diagrams, Figure 30–3 through Figure 30–6. These figures show the names of the object classes and whether a particular containment relationship is one-to-one, one-to-many or many-to-one. For further requirements on this topic, see IEEE Std 802.1F-1993. PSE and PoDL PSE management are only valid in a system that provides management at the next higher containment level, that is, either a DTE, or in the case of PSE management only, a repeater or Midspan with management.

MAU management is only valid in a system that provides management at the next higher containment level, that is, either a DTE or repeater with management.

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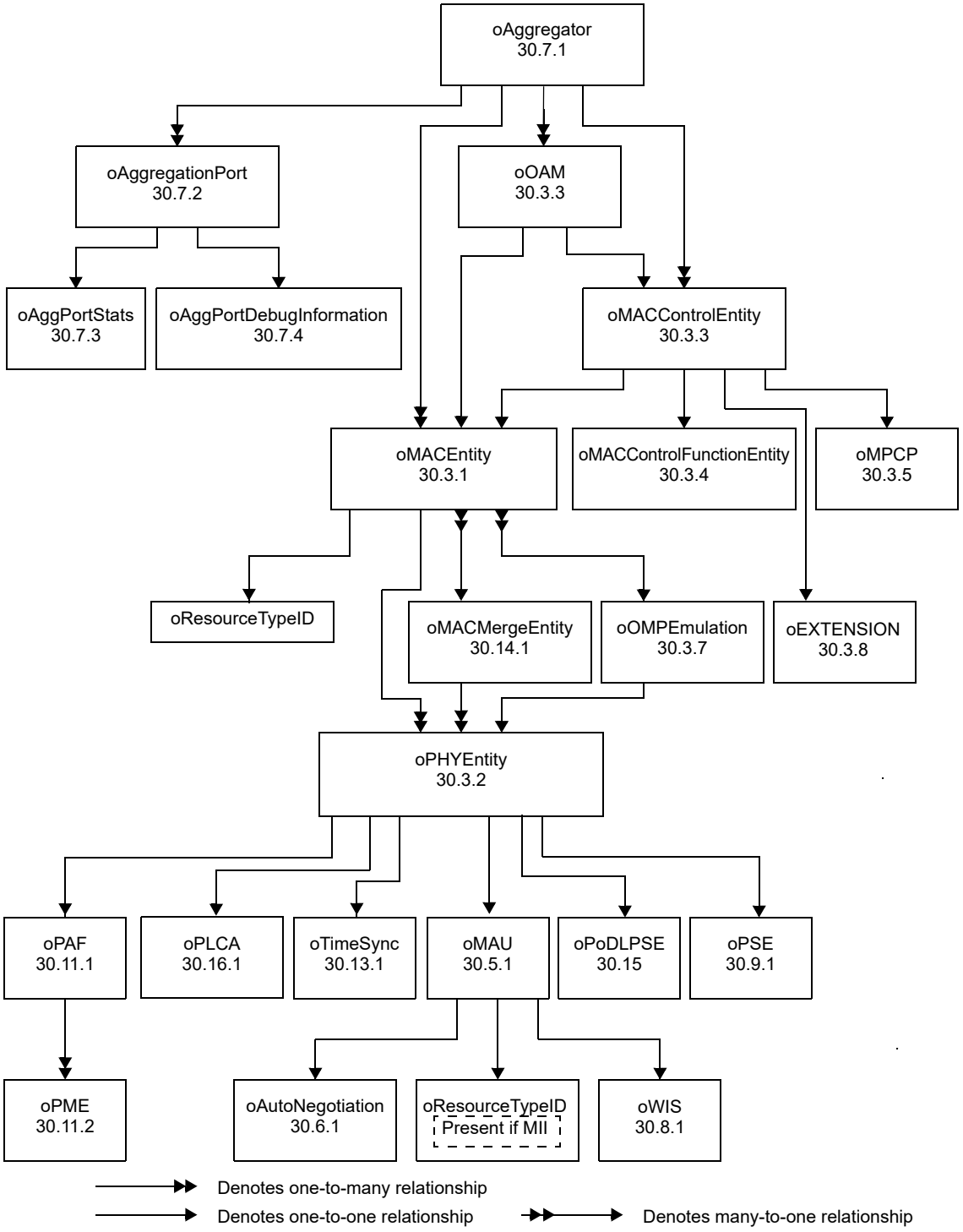

NOTE—The objects oAggregator, oAggregationPort, oAggPortStats, and oAggPortDebugInformation are deprecated by IEEE Std 802.1AX™-2008.

Figure 30–3—DTE System entity relationship diagram

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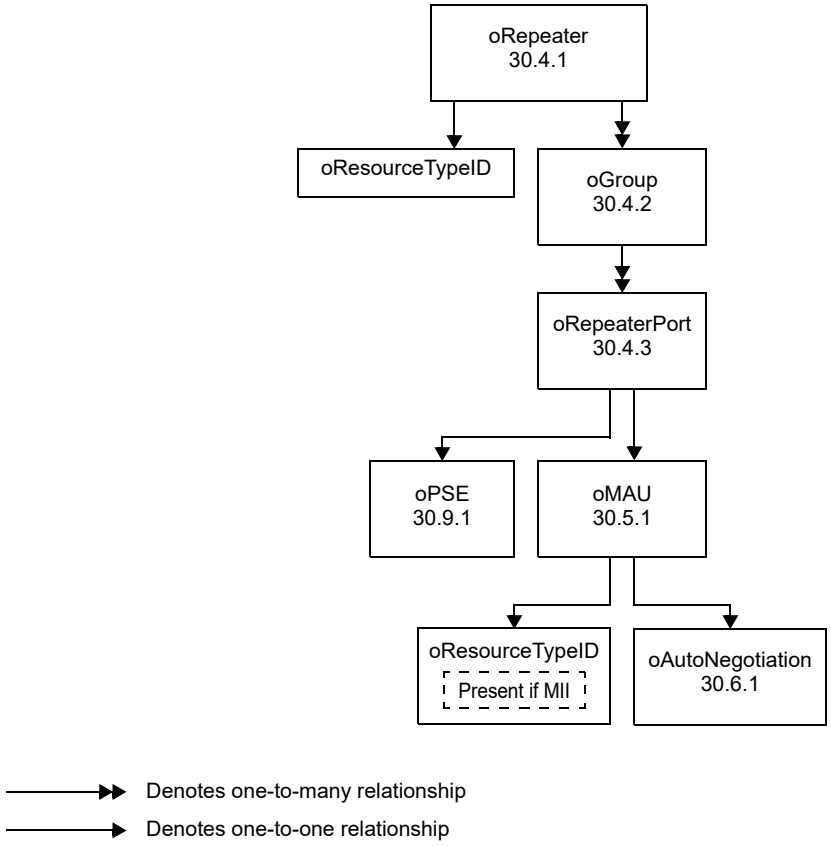

Figure 30–4—Repeater entity relationship diagram

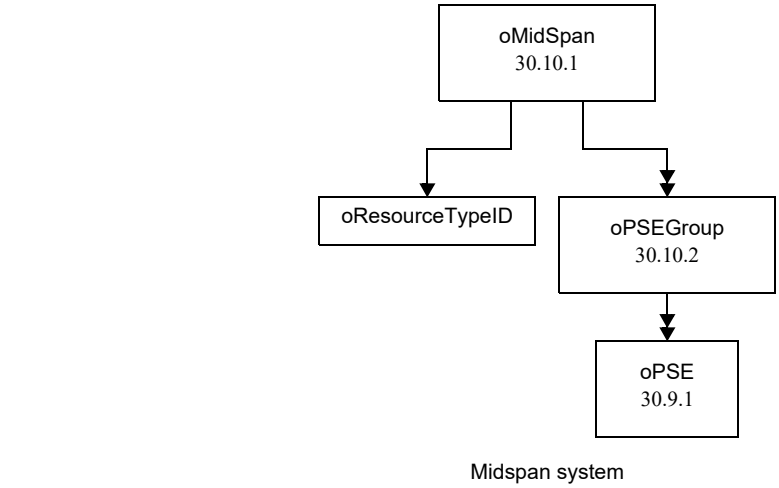

Figure 30–5—Midspan entity relationship diagram

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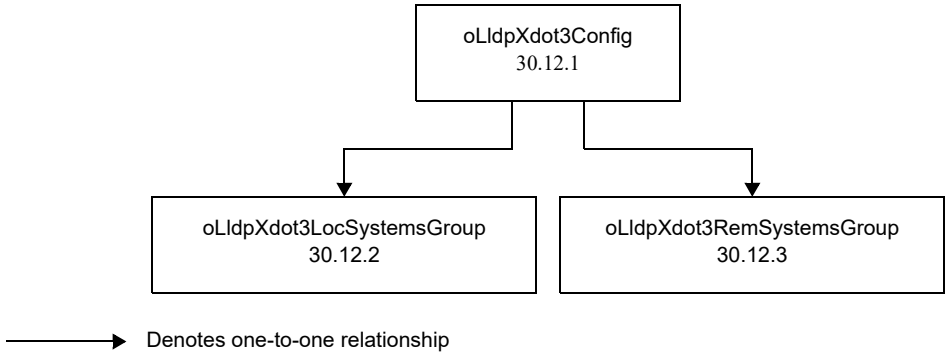

Figure 30–6—Link Layer Discovery Protocol entity relationship diagram

30.2.4 Naming

The name of an individual managed object is hierarchically defined within a managed system. For example, in the context of repeater management, a repeater port might be identified as "repeater 3, group 01, port 13," that is, port 13 of group 01 of a repeater with repeaterID 3 within the managed system.

In the case of MAU management, this will present itself in one of the two forms that are appropriate for a MAU's use, that is, as associated with a CSMA/CD interface of a DTE or with a particular port of a managed repeater. For example, a MAU could be identified as "repeater 3, group 01, port 13, MAU 1" or, that is, the MAU associated with port 13 of group 01 of a repeater with repeaterID 3 within the managed system. Examples of this are represented in the relationship of the naming attributes in the entity relationship diagram, Figure 30–3.

30.2.5 Capabilities

This standard makes use of the concept of *packages* as defined in ISO/IEC 10165-4:1992 as a means of grouping behaviour, attributes, actions, and notifications within a managed object class definition. Packages may either be mandatory, or be conditional, that is to say, present if a given condition is true. Within this standard *capabilities* are defined, each of which corresponds to a set of packages, which are components of a number of managed object class definitions and which share the same condition for presence. Implementation of the appropriate Basic and Mandatory packages is the minimum requirement for claiming conformance to IEEE 802.3 Management. Implementation of an entire optional capability is required in order to claim conformance to that capability. The capabilities and packages for IEEE 802.3 Management are specified in Table 30–1a through Table 30–11.

DTE Management has two packages that are required for management at the minimum conformance configuration—the Basic Package and the Mandatory Package. Systems that implement the optional MAC Control sublayer shall also implement the Basic and Mandatory Packages for the MAC Control Entity managed object class to claim DTE minimum conformance. For systems that include multiple PHY entities per MAC entity and implement the Multiple PHY Package to manage the selection of the active PHY, the optional Recommended Package shall be implemented. Systems that implement the optional Link Aggregation sublayer shall also implement the Basic and Mandatory Packages for the Aggregator and Aggregation Port managed object class to claim minimum DTE conformance.

For managed MAUs, the Basic Package is mandatory; all other packages are optional. For a managed MAU to be conformant to this standard, it shall fully implement the Basic Package. For a MAU to be conformant to an optional package it shall implement that entire package. While nonconformant (reference aMAUType

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= “other”) MAUs may utilize some or all of this clause to specify their management, conformance to this clause requires both a conformant MAU and conformant management. MAU Management is optional with respect to all other CSMA/CD Management. If an MII is present then the conditional MII Capability has to be implemented. This provides the means to identify the vendor and type of the externally connected device.

There are two distinct aspects of Repeater Management.

The first aspect provides the means to monitor and control the functions of a repeater. These functions include, but are not limited to: identifying a repeater, testing and initializing a repeater, and enabling/disabling a port. This is encompassed by the mandatory Basic Control Capability.

The second aspect provides the means to monitor traffic from attached segments, and to measure traffic sourced by DTEs connected to these segments. This is done by gathering statistics on packets that enter a repeater and maintaining those statistics on a per port basis. This is encompassed by the optional Performance Monitor Capability. The optional Address Tracking Capability provides the means to identify existence and movement of attached DTEs by their MAC addresses. While nonconformant (reference aRepeaterType = “other”) repeaters may utilize some or all of this clause to specify their management, conformance to this clause requires both a conformant repeater and conformant management.

If link Auto-Negotiation is present and managed, the Auto-Negotiation managed object class shall be implemented in its entirety. All attributes and actions are mandatory.

The 1000 Mb/s Burst Monitor Capability provides additional attributes that relate only to 1000 Mb/s operation, while the 100 Mb/s Monitor Capability has attributes that apply to a mixed 100 and 1000 Mb/s operation. These attributes are provided to complement the counter attributes of the optional packages and capabilities that apply to 10 Mb/s and mixed 10, 100, and 1000 Mb/s implementations. It is recommended that when the 100/1000 Mb/s Monitor Capability or 1000 Mb/s Burst Monitor Capability is implemented, the appropriate complementary counter packages and capabilities are also implemented.

For managed PSEs, the PSE Basic Package is mandatory and the PSE Recommended Package is optional. For managed PoDL PSEs, the PoDLPSE Basic Package is mandatory and the PoDLPSE Recommended Package is optional. For managed PDs, the PD Basic Package is mandatory. For a managed PSE to be conformant to this standard, it shall fully implement the PSE Basic Package. For a managed PoDL PSE to be conformant to this standard, it shall fully implement the PoDLPSE Basic Package. For a managed PD to be conformant to this standard, it shall fully implement the PD Basic Package. For a managed PSE to be conformant to the optional Recommended Package it shall implement that entire package. For a managed PoDL PSE to be conformant to the optional PoDL PSE Recommended Package it shall implement that entire package. PSE, PD, PoDL PSE, and PoDL PD management is optional with respect to all other CSMA/CD management.

For managed Midspans, the Midspan managed object class shall be implemented in its entirety. All attributes and notifications are mandatory. Midspan management is optional with respect to all other CSMA/CD management.

For LLDP management, the LLDP Basic Package is mandatory. All other LLDP packages are conditional on the IEEE 802.3 Organizationally Specific TLVs supported and the LLDP operating mode (see IEEE Std 802.1AB, Clause 10).

LLDP MAC/PHY Configuration/Status Local Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “MAC/PHY Configuration/Status” and are either in LLDP transmit only mode or in LLDP transmit and receive mode. LLDP MAC/PHY Config/Status Remote Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “MAC/PHY Configuration/Status” and are either in LLDP receive only mode or in LLDP transmit and receive mode.

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LLDP Power via MDI Local Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “Power via MDI” and are either in LLDP transmit only mode or in LLDP transmit and receive mode. LLDP Power via MDI Remote Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “Power via MDI” and are either in LLDP receive only mode or in LLDP transmit and receive mode.

LLDP Link Aggregation Local Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “Link Aggregation” and are either in LLDP transmit only mode or in LLDP transmit and receive mode. LLDP Link Aggregation Remote Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “Link Aggregation” and are either in LLDP receive only mode or in LLDP transmit and receive mode.

LLDP Max Frame Size Local Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “Max Frame Size” and are either in LLDP transmit only mode or in LLDP transmit and receive mode. LLDP Max Frame Size Remote Package is mandatory for managed entities that IEEE 802.3 Organizationally Specific TLV named “Max Frame Size” and are either in LLDP receive only mode or in LLDP transmit and receive mode. (See Table 30–7.)

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Table 30–1a—Capabilities

				DTE								Repeater					MAU						
				Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	Auto-Negotiation Package (mandatory)
oResourceTypeID managed object																							
	aResourceTypeIDName	ATTRIBUTE	GET	X								X									X		
	aResourceInfo	ATTRIBUTE	GET	X								X									X		
oMACEntity managed object class (30.3.1)																							
	aMACID	ATTRIBUTE	GET	X																			
	aFramesTransmittedOK	ATTRIBUTE	GET		X																		
	aSingleCollisionFrames	ATTRIBUTE	GET		X																		
	aMultipleCollisionFrames	ATTRIBUTE	GET		X																		
	aFramesReceivedOK	ATTRIBUTE	GET		X																		
	aFrameCheckSequenceErrors	ATTRIBUTE	GET		X																		
	aAlignmentErrors	ATTRIBUTE	GET		X																		
	aOctetsTransmittedOK	ATTRIBUTE	GET			X																	
	aFramesWithDeferredXmissions	ATTRIBUTE	GET			X																	
	aLateCollisions	ATTRIBUTE	GET			X																	
	aFramesAbortedDueToXSColls	ATTRIBUTE	GET			X																	
	aFramesLostDueToIntMACXmitError	ATTRIBUTE	GET			X																	
	aCarrierSenseErrors	ATTRIBUTE	GET			X																	
	aOctetsReceivedOK	ATTRIBUTE	GET			X																	
	aFramesLostDueToIntMACRcvError	ATTRIBUTE	GET			X																	
	aPromiscuousStatus	ATTRIBUTE	GET-SET			X																	
	aReadMulticastAddressList	ATTRIBUTE	GET			X																	
	aMaxFrameLength	ATTRIBUTE	GET				X																
	aSlowProtocolFrameLimit	ATTRIBUTE	GET				X																
	aMulticastFramesXmittedOK	ATTRIBUTE	GET				X																
	aBroadcastFramesXmittedOK	ATTRIBUTE	GET				X																
	aFramesWithExcessiveDeferral	ATTRIBUTE	GET						X														
	aMulticastFramesReceivedOK	ATTRIBUTE	GET				X																
	aBroadcastFramesReceivedOK	ATTRIBUTE	GET				X																
	aInRangeLengthErrors	ATTRIBUTE	GET				X																
	aOutOfRangeLengthField	ATTRIBUTE	GET				X																
	aFrameTooLongErrors	ATTRIBUTE	GET				X																
	aMACEnableStatus	ATTRIBUTE	GET-SET				X																

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Table 30–1b—Capabilities

				DTE										Repeater					MAU					
				Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Energy-Efficient Ethernet (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	Auto-Negotiation Package (mandatory)
oMACEntity managed object class (con'd.)																								
	aTransmitEnableStatus	ATTRIBUTE	GET-SET				X																	
	aMulticastReceiveStatus	ATTRIBUTE	GET-SET				X																	
	aReadWriteMACAddress	ATTRIBUTE	GET-SET				X																	
	aCollisionFrames	ATTRIBUTE	GET					X																
	aMACCapabilities	ATTRIBUTE	GET		X[1]	X																		
	aDuplexStatus	ATTRIBUTE	GET-SET		X[1]	X																		
	aRateControlAbility	ATTRIBUTE	GET		X																			
	aRateControlStatus	ATTRIBUTE	GET-SET		X																			
	aDeferControlAbility	ATTRIBUTE	GET		X																			
	aDeferControlStatus	ATTRIBUTE	GET-SET		X																			
	acInitializeMAC	ACTION		X																				
	acAddGroupAddress	ACTION				X																		
	acDeleteGroupAddress	ACTION				X																		
	acExecuteSelfTest	ACTION					X																	
oPHYEntity managed object class (30.3.2)																								
	aPHYID	ATTRIBUTE	GET	X																				
	aPHYType	ATTRIBUTE	GET	X																				
	aPHYTypeList	ATTRIBUTE	GET	X																				
	aSQETestErrors	ATTRIBUTE	GET			X																		
	aSymbolErrorDuringCarrier	ATTRIBUTE	GET								X													
	aMIIDetect	ATTRIBUTE	GET	X																				
	aPHYAdminState	ATTRIBUTE	GET	X																				
	acPHYAdminControl	ACTION								X														
	aTransmitLPIMicroseconds	ATTRIBUTE	GET									X												
	aReceiveLPIMicroseconds	ATTRIBUTE	GET									X												
	aTransmitLPITransitions	ATTRIBUTE	GET									X												
	aReceiveLPITransitions	ATTRIBUTE	GET									X												

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Table 30–1b—Capabilities *(continued)*

				DTE										Repeater				MAU					
				Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Energy-Efficient Ethernet (optional)		Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	Auto-Negotiation Package (mandatory)
oMACControlEntity managed object class (30.3.3)																							
	aMACControlID	ATTRIBUTE	GET		X																		
	aMACControlFunctionsSupported	ATTRIBUTE	GET-SET		X																		
	aMACControlFramesTransmitted	ATTRIBUTE	GET			X																	
	aMACControlFramesReceived	ATTRIBUTE	GET			X																	
	aUnsupportedOpcodesReceived	ATTRIBUTE	GET			X																	
	aPFCEnableStatus	ATTRIBUTE	GET		X[2]																		

NOTE 1: The aMACCapabilities and aDuplexStatus attributes are mandatory in systems that can operate in full duplex mode. They are recommended in systems that can operate only in half duplex mode.

NOTE 2: The aPFCenableStatus attribute is mandatory in systems that support the PFC MAC Control Function. It is optional in systems that do not support the PFC MAC Control Function.

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Table 30–1c—Capabilities

			DTE								Repeater					MAU					
			Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	Auto-Negotiation Package (mandatory)
oMACControlFunctionEntity managed object class (30.3.4)																					
aPAUSELinkDelayAllowance	ATTRIBUTE	GET-SET		X																	
aPAUSEMACCtrlFramesTransmitted	ATTRIBUTE	GET			X																
aPAUSEMACCtrlFramesReceived	ATTRIBUTE	GET			X																
oEXTENSION managed object class (30.3.8)																					
aEXTENSIONMACCtrlFramesTrans-	ATTRIBUTE	GET			X																
aEXTENSIONMACCtrlFramesRe-	ATTRIBUTE	GET			X																
oRepeater managed object class (30.4.1)																					
aRepeaterID	ATTRIBUTE	GET									X										
aRepeaterType	ATTRIBUTE	GET									X										
aRepeaterGroupCapacity	ATTRIBUTE	GET									X										
aGroupMap	ATTRIBUTE	GET									X										
aRepeaterHealthState	ATTRIBUTE	GET									X										
aRepeaterHealthText	ATTRIBUTE	GET									X										
aRepeaterHealthData	ATTRIBUTE	GET									X										
aTransmitCollisions	ATTRIBUTE	GET										X									
acResetRepeater	ACTION										X										
acExecuteNonDisruptiveSelfTest	ACTION										X										
nRepeaterHealth	NOTIFICATION										X										
nRepeaterReset	NOTIFICATION										X										
nGroupMapChange	NOTIFICATION										X										
oGroup managed object class (30.4.2)																					
aGroupID	ATTRIBUTE	GET									X										
aGroupPortCapacity	ATTRIBUTE	GET									X										
aPortMap	ATTRIBUTE	GET									X										
nPortMapChange	NOTIFICATION										X										

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Table 30–1d—Capabilities

				DTE							Repeater					MAU						
				Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	Auto-Negotiation Package (mandatory)
oRepeaterPort managed object class (30.4.3)																							
	aPortID	ATTRIBUTE	GET									X											
	aPortAdminState	ATTRIBUTE	GET									X											
	aAutoPartitionState	ATTRIBUTE	GET									X											
	aReadableFrames	ATTRIBUTE	GET										X										
	aReadableOctets	ATTRIBUTE	GET										X										
	aFrameCheckSequenceErrors	ATTRIBUTE	GET										X										
	aAlignmentErrors	ATTRIBUTE	GET										X										
	aFramesTooLong	ATTRIBUTE	GET										X										
	aShortEvents	ATTRIBUTE	GET										X										
	aRunts	ATTRIBUTE	GET										X										
	aCollisions	ATTRIBUTE	GET										X										
	aLateEvents	ATTRIBUTE	GET										X										
	aVeryLongEvents	ATTRIBUTE	GET										X										
	aDataRateMismatches	ATTRIBUTE	GET										X										
	aAutoPartitions	ATTRIBUTE	GET										X										
	aIsolates	ATTRIBUTE	GET												X								
	aSymbolErrorDuringPacket	ATTRIBUTE	GET												X								
	aLastSourceAddress	ATTRIBUTE	GET											X									
	aSourceAddressChanges	ATTRIBUTE	GET											X									
	aBursts	ATTRIBUTE	GET													X							
	acPortAdminControl	ACTION										X											

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Table 30–1e—Capabilities

			DTE									Repeater					MAU										
			Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	MultiGBASE-T Operating Margin package (conditional)	Forward Error Correction Package (conditional)	Energy-Efficient Ethernet (optional)	Auto-Negotiation Package (mandatory)		
oMAU managed object class (30.5.1)																											
	aMAUID	ATTRIBUTE	GET													X											
	aMAUType	ATTRIBUTE	GET-SET													X											
	aMAUTypeList	ATTRIBUTE	GET													X											
	aMediaAvailable	ATTRIBUTE	GET													X											
	aLoseMediaCounter	ATTRIBUTE	GET															X									
	aJabber	ATTRIBUTE	GET													X											
	aMAUAdminState	ATTRIBUTE	GET													X											
	aBbMAUXmitRcvSplitType	ATTRIBUTE	GET																X								
	aBroadbandFrequencies	ATTRIBUTE	GET																X								
	aFalseCarriers	ATTRIBUTE	GET																		X						
	aBIPErrorCount	ATTRIBUTE	GET																		X						
	aLaneMapping	ATTRIBUTE	GET																		X						
	aRSFECBIPErrorCount	ATTRIBUTE	GET																		X						
	aRSFECLaneMapping	ATTRIBUTE	GET																		X						
	aSCFECLaneMapping	ATTRIBUTE	GET																		X						
	aIdleErrorCount	ATTRIBUTE	GET																		X						
	aFECAbility	ATTRIBUTE	GET																				X				
	aFECmode	ATTRIBUTE	GET-SET																				X				
	aFECCorrectedBlocks	ATTRIBUTE	GET																				X				
	aFECUncorrectableBlocks	ATTRIBUTE	GET																				X				
	aRSFECBypassAbility	ATTRIBUTE	GET																				X				
	aRSFECBypassIndicationAbility	ATTRIBUTE	GET																				X				
	aRSFECBypassEnable	ATTRIBUTE	GET-SET																				X				
	aRSFECBypassIndicationEnable	ATTRIBUTE	GET-SET																				X				
	aPCSFECBypassIndicationAbility	ATTRIBUTE	GET																				X				
	aPCSFECBypassIndicationEnable	ATTRIBUTE	GET-SET																				X				
	aSNROpMarginChnlA	ATTRIBUTE	GET																			X					
	aSNROpMarginChnlB	ATTRIBUTE	GET																			X					
	aSNROpMarginChnlC	ATTRIBUTE	GET																			X					
	aSNROpMarginChnlD	ATTRIBUTE	GET																			X					
	acResetMAU	ACTION															X										
	acMAUAdminControl	ACTION															X										

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Table 30–1e—Capabilities *(continued)*

			DTE								Repeater					MAU										
			Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	MultiGBASE-T Operating Margin package (conditional)	Forward Error Correction Package (conditional)	Energy-Efficient Ethernet (optional)	Auto-Negotiation Package (mandatory)
	nJabber	NOTIFICATION														X									
	aLDFastRetrainCount	ATTRIBUTE	GET																					X	
	aLPFastRetrainCount	ATTRIBUTE	GET																					X	
oAuto-Negotiation managed object class (30.6.1)																									
	aAutoNegID	ATTRIBUTE	GET																						X
	aAutoNegAdminState	ATTRIBUTE	GET																						X
	aAutoNegRemoteSignaling	ATTRIBUTE	GET																						X
	aAutoNegAutoConfig	ATTRIBUTE	GET-SET																						X
	aAutoNegLocalTechnologyAbility	ATTRIBUTE	GET																						X
	aAutoNegAdvertisedTechnologyAbil-	ATTRIBUTE	GET-SET																						X
	aAutoNegReceivedTechnologyAbility	ATTRIBUTE	GET																						X
	aAutoNegLocalSelectorAbility	ATTRIBUTE	GET																						X
	aAutoNegAdvertisedSelectorAbility	ATTRIBUTE	GET-SET																						X
	aAutoNegReceivedSelectorAbility	ATTRIBUTE	GET																						X
	acAutoNegRestartAutoConfig	ACTION																							X
	acAutoNegAdminControl	ACTION																							X
Common Attributes Template																									
	aCMCounter	ATTRIBUTE	GET		X	X	X		X		X		X	X	X			X	X			X				

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Table 30–2—Link Aggregation capabilities

				DTE					
	Object name	Object type	Operations supported	Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Aggregation Port Statistics (optional)	Aggregation Port Debug Information (optional)
oAggregator (30.7.1) NOTE—This object is deprecated by IEEE Std 802.1AX-2008									
	aAggID	ATTRIBUTE	GET	X					
	aAggDescription	ATTRIBUTE	GET		X				
	aAggName	ATTRIBUTE	GET-SET		X				
	aAggActorSystemID	ATTRIBUTE	GET-SET		X				
	aAggActorSystemPriority	ATTRIBUTE	GET-SET		X				
	aAggAggregateOrIndividual	ATTRIBUTE	GET		X				
	aAggActorAdminKey	ATTRIBUTE	GET-SET		X				
	aAggActorOperKey	ATTRIBUTE	GET		X				
	aAggMACAddress	ATTRIBUTE	GET		X				
	aAggPartnerSystemID	ATTRIBUTE	GET		X				
	aAggPartnerSystemPriority	ATTRIBUTE	GET		X				
	aAggPartnerOperKey	ATTRIBUTE	GET		X				
	aAggAdminState	ATTRIBUTE	GET-SET		X				
	aAggOperState	ATTRIBUTE	GET		X				
	aAggTimeOfLastOperChange	ATTRIBUTE	GET		X				
	aAggDataRate	ATTRIBUTE	GET		X				
	aAggOctetsTxOK	ATTRIBUTE	GET			X			
	aAggOctetsRxOK	ATTRIBUTE	GET			X			
	aAggFramesTxOK	ATTRIBUTE	GET		X				
	aAggFramesRxOK	ATTRIBUTE	GET		X				
	aAggMulticastFramesTxOK	ATTRIBUTE	GET				X		
	aAggMulticastFramesRxOK	ATTRIBUTE	GET				X		
	aAggBroadcastFramesTxOK	ATTRIBUTE	GET				X		
	aAggBroadcastFramesRxOK	ATTRIBUTE	GET				X		
	aAggFramesDiscardedOnTx	ATTRIBUTE	GET			X			
	aAggFramesDiscardedOnRx	ATTRIBUTE	GET			X			
	aAggFramesWithTxErrors	ATTRIBUTE	GET			X			

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Table 30–2—Link Aggregation capabilities *(continued)*

				DTE					
	Object name	Object type	Operations supported	Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Aggregation Port Statistics (optional)	Aggregation Port Debug Information (optional)
	aAggFramesWithRxErrors	ATTRIBUTE	GET			X			
	aAggUnknownProtocolFrames	ATTRIBUTE	GET			X			
	aAggLinkUpDownNotificationEnable	ATTRIBUTE	GET-SET		X				
	nAggLinkUpNotification	NOTIFICATION			X				
	nAggLinkDownNotification	NOTIFICATION			X				
	aAggPortList	ATTRIBUTE	GET			X			
	aAggCollectorMaxDelay	ATTRIBUTE	GET-SET		X				
oAggregationPort (30.7.2) NOTE—This object is deprecated by IEEE Std 802.1AX-2008									
	aAggPortID	ATTRIBUTE	GET	X					
	aAggPortActorSystemPriority	ATTRIBUTE	GET-SET		X				
	aAggPortActorSystemID	ATTRIBUTE	GET		X				
	aAggPortActorAdminKey	ATTRIBUTE	GET-SET		X				
	aAggPortActorOperKey	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminSystemPriority	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperSystemPriority	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminSystemID	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperSystemID	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminKey	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperKey	ATTRIBUTE	GET		X				
	aAggPortSelectedAggID	ATTRIBUTE	GET		X				
	aAggPortAttachedAggID	ATTRIBUTE	GET		X				
	aAggPortActorPort	ATTRIBUTE	GET		X				
	aAggPortActorPortPriority	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerAdminPort	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperPort	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminPortPriority	ATTRIBUTE	GET-SET		X				

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Table 30–2—Link Aggregation capabilities *(continued)*

				DTE					
	Object name	Object type	Operations supported	Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Aggregation Port Statistics (optional)	Aggregation Port Debug Information (optional)
	aAggPortPartnerOperPortPriority	ATTRIBUTE	GET		X				
	aAggPortActorAdminState	ATTRIBUTE	GET-SET		X				
	aAggPortActorOperState	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminState	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperState	ATTRIBUTE	GET		X				
	aAggPortAggregateOrIndividual	ATTRIBUTE	GET		X				
oAggPortStats (30.7.3) Note—This object is deprecated by IEEE Std 802.1AX-2008									
	aAggPortStatsID	ATTRIBUTE	GET					X	
	aAggPortStatsLACPDUsRx	ATTRIBUTE	GET					X	
	aAggPortStatsMarkerPDUsRx	ATTRIBUTE	GET					X	
	aAggPortStatsMarkerResponsePDUsRx	ATTRIBUTE	GET					X	
	aAggPortStatsUnknownRx	ATTRIBUTE	GET					X	
	aAggPortStatsIllegalRx	ATTRIBUTE	GET					X	
	aAggPortStatsLACPDUsTx	ATTRIBUTE	GET					X	
	aAggPortStatsMarkerPDUsTx	ATTRIBUTE	GET					X	
	aAggPortStatsMarkerResponsePDUsTx	ATTRIBUTE	GET					X	
oAggPortDebugInformation (30.7.4) Note—This object is deprecated by IEEE Std 802.1AX-2008									
	aAggPortDebugInformationID	ATTRIBUTE	GET						X
	aAggPortDebugRxState	ATTRIBUTE	GET						X
	aAggPortDebugLastRxTime	ATTRIBUTE	GET						X
	aAggPortDebugMuxState	ATTRIBUTE	GET						X
	aAggPortDebugMuxReason	ATTRIBUTE	GET						X
	aAggPortDebugActorChurnState	ATTRIBUTE	GET						X
	aAggPortDebugPartnerChurnState	ATTRIBUTE	GET						X
	aAggPortDebugActorChurnCount	ATTRIBUTE	GET						X
	aAggPortDebugPartnerChurnCount	ATTRIBUTE	GET						X

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Table 30–2—Link Aggregation capabilities *(continued)*

				DTE					
	Object name	Object type	Operations supported	Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Aggregation Port Statistics (optional)	Aggregation Port Debug Information (optional)
	aAggPortDebugActorSyncTransitionCount	ATTRIBUTE	GET						X
	aAggPortDebugPartnerSyncTransitionCount	ATTRIBUTE	GET						X
	aAggPortDebugActorChangeCount	ATTRIBUTE	GET						X
	aAggPortDebugPartnerChangeCount	ATTRIBUTE	GET						X
Common Attributes Template									
	aCMCounter	ATTRIBUTE	GET		X	X	X	X	X

Table 30–3—WIS capabilities

				WIS Basic Package (mandatory)	WIS Recommended Package (optional)
oWIS managed object class (30.8.1)					
	aWISID	ATTRIBUTE	GET	**X**	
	aSectionStatus	ATTRIBUTE	GET	**X**	
	aSectionSESThreshold	ATTRIBUTE	GET-SET		**X**
	aSectionSESs	ATTRIBUTE	GET		**X**
	aSectionESs	ATTRIBUTE	GET		**X**
	aSectionSEFSs	ATTRIBUTE	GET		**X**
	aSectionCVs	ATTRIBUTE	GET		**X**
	aJ0ValueTX	ATTRIBUTE	GET-SET		**X**
	aJ0ValueRX	ATTRIBUTE	GET		**X**
	aLineStatus	ATTRIBUTE	GET	**X**	

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Table 30–3—WIS capabilities *(continued)*

				WIS Basic Package (mandatory)	WIS Recommended Package (optional)
	aLineSESThreshold	ATTRIBUTE	GET-SET		X
	aLineSESs	ATTRIBUTE	GET		X
	aLineESs	ATTRIBUTE	GET		X
	aLineCVs	ATTRIBUTE	GET		X
	aFarEndLineSESs	ATTRIBUTE	GET		X
	aFarEndLineESs	ATTRIBUTE	GET		X
	aFarEndLineCVs	ATTRIBUTE	GET		X
	aPathStatus	ATTRIBUTE	GET	X	
	aPathSESThreshold	ATTRIBUTE	GET-SET		X
	aPathSESs	ATTRIBUTE	GET		X
	aPathESs	ATTRIBUTE	GET		X
	aPathCVs	ATTRIBUTE	GET		X
	aJ1ValueTX	ATTRIBUTE	GET-SET		X
	aJ1ValueRX	ATTRIBUTE	GET		X
	aFarEndPathStatus	ATTRIBUTE	GET	X	
	aFarEndPathSESs	ATTRIBUTE	GET		X
	aFarEndPathESs	ATTRIBUTE	GET		X
	aFarEndPathCVs	ATTRIBUTE	GET		X
Common Attributes Template					
	aCMCounter	ATTRIBUTE	GET		X

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Table 30–4—DTE Power via MDI capabilities

				PSE Basic Package (mandatory)	PSE Recommended Package (optional)	Midspan Basic Capability (mandatory)
oResourceTypeID managed object						
	aResourceTypeIDName	ATTRIBUTE	GET			X
	aResourceInfo	ATTRIBUTE	GET			X
oMidSpan managed object class (30.10.1)						
	aMidSpanID	ATTRIBUTE	GET			X
	aMidSpanPSEGroupCapacity	ATTRIBUTE	GET			X
	aMidSpanPSEGroupMap	ATTRIBUTE	GET			X
	nMidSpanPSEGroupMapChange	NOTIFICATION				X
oPSEGroup managed object class (30.10.2)						
	aPSEGroupID	ATTRIBUTE	GET			X
	aPSECapacity	ATTRIBUTE	GET			X
	aPSEMap	ATTRIBUTE	GET			X
	nPSEMapChange	NOTIFICATION				X
oPSE managed object class (30.9.1)						
	aPSEID	ATTRIBUTE	GET	X		
	aPSEAdminState	ATTRIBUTE	GET	X		
	aPSEPowerPairsControlAbility	ATTRIBUTE	GET	X		
	aPSEPowerPairs	ATTRIBUTE	GET-SET	X		
	aPSEPowerDetectionStatus	ATTRIBUTE	GET	X		
	aPSEPowerDetectionStatusA	ATTRIBUTE	GET	X		
	aPSEPowerDetectionStatusB	ATTRIBUTE	GET	X		
	aPSEPowerClassification	ATTRIBUTE	GET		X	
	aPSEPowerClassificationA	ATTRIBUTE	GET		X	
	aPSEPowerClassificationB	ATTRIBUTE	GET		X	
	aPSEInvalidSignatureCounter	ATTRIBUTE	GET		X	
	aPSEInvalidSignatureCounterA	ATTRIBUTE	GET		X	
	aPSEInvalidSignatureCounterB	ATTRIBUTE	GET		X	
	aPSEPowerDeniedCounter	ATTRIBUTE	GET		X	
	aPSEPowerDeniedCounterA	ATTRIBUTE	GET		X	
	aPSEPowerDeniedCounterB	ATTRIBUTE	GET		X	
	aPSEOverLoadCounter	ATTRIBUTE	GET		X	
	aPSEOverLoadCounterA	ATTRIBUTE	GET		X	
	aPSEOverLoadCounterB	ATTRIBUTE	GET		X	
	aPSEMPSAbsentCounter	ATTRIBUTE	GET		X	

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Table 30–4—DTE Power via MDI capabilities *(continued)*

				PSE Basic Package (mandatory)	PSE Recommended Package (optional)	Midspan Basic Capability (mandatory)
	aPSEMPSAbsentCounterA	ATTRIBUTE	GET		X	
	aPSEMPSAbsentCounterB	ATTRIBUTE	GET		X	
	acPSEAdminControl	ACTION		X		
	aPSEActualPower	ATTRIBUTE	GET		X	
	aPSEPowerAccuracy	ATTRIBUTE	GET		X	
	aPSECumulativeEnergy	ATTRIBUTE	GET		X	
Common Attributes Template						
	aCMCounter	ATTRIBUTE	GET		X	

Table 30–5—EFM capabilities

				DTE				MAU		PME		
				Multipoint Control Protocol Package (conditional)	Operation Administration Maintenance Package (conditional)	Optical Multipoint Emulation Package (conditional)	Optical Multipoint Emulation Monitor Package (optional)	PCS Code Error Monitor Package (optional)	Forward Error Correction Package (conditional)	Basic Package (mandatory)	PME Aggregation Package (optional)	10P/2B Package (mandatory)
oMPCP managed object class (30.3.5)												
	aMPCPID	ATTRIBUTE	GET	X								

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Table 30–5—EFM capabilities *(continued)*

			DTE				MAU		PME		
			Multipoint Control Protocol Package (conditional)	Operation Administration Maintenance Package (conditional)	Optical Multipoint Emulation Package (conditional)	Optical Multipoint Emulation Monitor Package (optional)	PCS Code Error Monitor Package (optional)	Forward Error Correction Package (conditional)	Basic Package (mandatory)	PME Aggregation Package (optional)	10P/2B Package (mandatory)
aMPCPAdminState	ATTRIBUTE	GET	X								
aMPCPMode	ATTRIBUTE	GET	X								
aMPCPLinkID	ATTRIBUTE	GET	X								
aMPCPRemoteMACAddress	ATTRIBUTE	GET	X								
aMPCPRegistrationState	ATTRIBUTE	GET	X								
aMPCPMACCtrlFramesTransmitted	ATTRIBUTE	GET	X								
aMPCPMACCtrlFramesReceived	ATTRIBUTE	GET	X								
aMPCPTxGate	ATTRIBUTE	GET	X								
aMPCPTxRegAck	ATTRIBUTE	GET	X								
aMPCPTxRegister	ATTRIBUTE	GET	X								
aMPCPTxRegRequest	ATTRIBUTE	GET	X								
aMPCPTxReport	ATTRIBUTE	GET	X								
aMPCPRxGate	ATTRIBUTE	GET	X								
aMPCPRxRegAck	ATTRIBUTE	GET	X								
aMPCPRxRegister	ATTRIBUTE	GET	X								
aMPCPRxRegRequest	ATTRIBUTE	GET	X								
aMPCPRxReport	ATTRIBUTE	GET	X								
aMPCPTransmitElapsed	ATTRIBUTE	GET	X								
aMPCPReceiveElapsed	ATTRIBUTE	GET	X								
aMPCPRoundTripTime	ATTRIBUTE	GET	X								
aMPCPDiscoveryWindowsSent	ATTRIBUTE	GET	X								
aMPCPDiscoveryTimeout	ATTRIBUTE	GET	X								
aMPCPMaximumPendingGrants	ATTRIBUTE	GET	X								
aMPCPRecognizedMulticastIDs	ATTRIBUTE	GET	X								
acMPCPAdminControl	ACTION		X								
oOAM managed object class (30.3.6)											
aMACControlID	ATTRIBUTE	GET		X							
aOAMAdminState	ATTRIBUTE	GET		X							
aOAMDiscoveryState	ATTRIBUTE	GET		X							
aOAMRemoteMACAddress	ATTRIBUTE	GET		X							
aOAMLocalConfiguration	ATTRIBUTE	GET		X							
aOAMRemoteConfiguration	ATTRIBUTE	GET		X							

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Table 30–5—EFM capabilities *(continued)*

				DTE				MAU		PME		
				Multipoint Control Protocol Package (conditional)	Operation Administration Maintenance Package (conditional)	Optical Multipoint Emulation Package (conditional)	Optical Multipoint Emulation Monitor Package (optional)	PCS Code Error Monitor Package (optional)	Forward Error Correction Package (conditional)	Basic Package (mandatory)	PME Aggregation Package (optional)	10P/2B Package (mandatory)
	aOAMLocalPDUConfiguration	ATTRIBUTE	GET		X							
	aOAMRemotePDUConfiguration	ATTRIBUTE	GET		X							
	aOAMLocalFlagsField	ATTRIBUTE	GET		X							
	aOAMRemoteFlagsField	ATTRIBUTE	GET		X							
	aOAMLocalRevision	ATTRIBUTE	GET		X							
	aOAMRemoteRevision	ATTRIBUTE	GET		X							
	aOAMLocalState	ATTRIBUTE	GET		X							
	aOAMRemoteState	ATTRIBUTE	GET		X							
	aOAMRemoteVendorOUI	ATTRIBUTE	GET		X							
	aOAMRemoteVendorSpecificInfo	ATTRIBUTE	GET		X							
	aOAMUnsupportedCodesTx	ATTRIBUTE	GET		X							
	aUnsupportedOpcodesReceived	ATTRIBUTE	GET		X							
	aOAMInformationTx	ATTRIBUTE	GET		X							
	aOAMInformationRx	ATTRIBUTE	GET		X							
	aOAMUniqueEventNotificationTx	ATTRIBUTE	GET		X							
	aOAMDuplicateEventNotificationTx	ATTRIBUTE	GET		X							
	aOAMUniqueEventNotificationRx	ATTRIBUTE	GET		X							
	aOAMDuplicateEventNotificationRx	ATTRIBUTE	GET		X							
	aOAMLoopbackControlTx	ATTRIBUTE	GET		X							
	aOAMLoopbackControlRx	ATTRIBUTE	GET		X							
	aOAMVariableRequestTx	ATTRIBUTE	GET		X							
	aOAMVariableRequestRx	ATTRIBUTE	GET		X							
	aOAMVariableResponseTx	ATTRIBUTE	GET		X							
	aOAMVariableResponseRx	ATTRIBUTE	GET		X							
	aOAMOrganizationSpecificTx	ATTRIBUTE	GET		X							
	aOAMOrganizationSpecificRx	ATTRIBUTE	GET		X							
	aOAMLocalErrSymPeriodConfig	ATTRIBUTE	GET		X							
	aOAMLocalErrSymPeriodEvent	ATTRIBUTE	GET		X							
	aOAMLocalErrFrameConfig	ATTRIBUTE	GET		X							
	aOAMLocalErrFrameEvent	ATTRIBUTE	GET		X							
	aOAMLocalErrFramePeriodConfig	ATTRIBUTE	GET		X							
	aOAMLocalErrFramePeriodEvent	ATTRIBUTE	GET		X							

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Table 30–5—EFM capabilities *(continued)*

			DTE				MAU		PME		
			Multipoint Control Protocol Package (conditional)	Operation Administration Maintenance Package (conditional)	Optical Multipoint Emulation Package (conditional)	Optical Multipoint Emulation Monitor Package (optional)	PCS Code Error Monitor Package (optional)	Forward Error Correction Package (conditional)	Basic Package (mandatory)	PME Aggregation Package (optional)	10P/2B Package (mandatory)
aOAMLocalErrFrameSecsSummaryConfig	ATTRIBUTE	GET		X							
aOAMLocalErrFrameSecsSummaryEvent	ATTRIBUTE	GET		X							
aOAMRemoteErrSymPeriodEvent	ATTRIBUTE	GET		X							
aOAMRemoteErrFrameEvent	ATTRIBUTE	GET		X							
aOAMRemoteErrFramePeriodEvent	ATTRIBUTE	GET		X							
aOAMRemoteErrFrameSecsSummaryEvent	ATTRIBUTE	GET		X							
aFramesLostDueToOAMError	ATTRIBUTE	GET		X							
acOAMAdminControl	ACTION			X							
oOMPEmulation managed object class (30.3.7)											
aOMPEmulationID	ATTRIBUTE	GET			X						
aOMPEmulationType	ATTRIBUTE	GET			X						
aSLDErrors	ATTRIBUTE	GET			X						
aCRC8Errors	ATTRIBUTE	GET			X						
aGoodLLID	ATTRIBUTE	GET				X					
aONUPONcastLLID	ATTRIBUTE	GET				X					
aOLTPONcastLLID	ATTRIBUTE	GET				X					
aBadLLID	ATTRIBUTE	GET				X					
oMAU managed object class (30.5.1)											
aPCSCodingViolation	ATTRIBUTE	GET					X				
aFECAbility	ATTRIBUTE	GET						X			
aFECmode	ATTRIBUTE	GET-SET						X			
aFECCorrectedBlocks	ATTRIBUTE	GET						X			
aFECUncorrectableBlocks	ATTRIBUTE	GET						X			
oPAF managed object class (30.11.1)											
aPAFID	ATTRIBUTE	GET							X		
aPhyEnd	ATTRIBUTE	GET							X		
aPHYCurrentStatus	ATTRIBUTE	GET							X		
aPAFSupported	ATTRIBUTE	GET							X		
aPAFAdminState	ATTRIBUTE	GET-SET								X	
aLocalPAFCapacity	ATTRIBUTE	GET								X	
aLocalPMEAvailable	ATTRIBUTE	GET								X	

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Table 30–5—EFM capabilities *(continued)*

			DTE				MAU		PME		
			Multipoint Control Protocol Package (conditional)	Operation Administration Maintenance Package (conditional)	Optical Multipoint Emulation Package (conditional)	Optical Multipoint Emulation Monitor Package (optional)	PCS Code Error Monitor Package (optional)	Forward Error Correction Package (conditional)	Basic Package (mandatory)	PME Aggregation Package (optional)	10P/2B Package (mandatory)
aLocalPMEAggregate	ATTRIBUTE	GET								X	
aRemotePAFSupported	ATTRIBUTE	GET								X	
aRemotePAFCapacity	ATTRIBUTE	GET								X	
aRemotePMEAggregate	ATTRIBUTE	GET								X	
oPME managed object class (30.11.2)											
aPMEID	ATTRIBUTE	GET									X
aPMEAdminState	ATTRIBUTE	GET-SET									X
aPMEStatus	ATTRIBUTE	GET									X
aPMESNRMgn	ATTRIBUTE	GET									X
aTCCodingViolations	ATTRIBUTE	GET									X
aProfileSelect	ATTRIBUTE	GET-SET									X
aOperatingProfile	ATTRIBUTE	GET									X
aPMEFECCorrectedBlocks	ATTRIBUTE	GET									X
aPMEFECUncorrectableBlocks	ATTRIBUTE	GET									X
aTCCRCErrors	ATTRIBUTE	GET									X
Common Attributes Template											
aCMCounter	ATTRIBUTE	GET	X	X	X	X	X	X		X	X

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Table 30–6—TimeSync Capabilities

				Support for Time Sync(mandatory)
oTimeSync managed object				
	aTimeSyncCapabilityTX	ATTRIBUTE	GET	X
	aTimeSyncCapabilityRX	ATTRIBUTE	GET	X
	aTimeSyncDelayTXmax	ATTRIBUTE	GET	X
	aTimeSyncDelayTXmin	ATTRIBUTE	GET	X
	aTimeSyncDelayRXmax	ATTRIBUTE	GET	X
	aTimeSyncDelayRXmin	ATTRIBUTE	GET	X

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Table 30–7—LLDP capabilities

			LLDP Basic Package (mandatory)	LLDP MAC/PHY Configuration/Status Local Package (conditional)	LLDP MAC/PHY Configuration/Status Remote Package (conditional)	LLDP Power via MDI Local Package (conditional)	LLDP Power via MDI Remote Package (conditional)	LLDP Power via MDI Measurements Local Package (conditional)	LLDP Power via MDI Measurements Remote Package (conditional)	LLDP Link Aggregation Local Package (conditional)	LLDP Link Aggregation Remote Package (conditional)	LLDP Maximum Frame Size Local Package (conditional)	LLDP Maximum Frame Size Remote Package (conditional)	LLDP EEE Local Package (optional)	LLDP EEE Remote Package (optional)
oLldpXdot3Config managed object class (30.12.1)															
aLldpXdot3PortConfigTLVsTxEnable	ATTRIBUTE	GET-SET	X												
oLldpXdot3LocSystemsGroup managed object class (30.12.2)															
aLldpXdot3LocPortAutoNegSupported	ATTRIBUTE	GET		X											
aLldpXdot3LocPortAutoNegEnabled	ATTRIBUTE	GET		X											
aLldpXdot3LocPortAutoNegAdvertisedCap	ATTRIBUTE	GET		X											
aLldpXdot3LocPortOperMauType	ATTRIBUTE	GET		X											
aLldpXdot3LocPowerPortClass	ATTRIBUTE	GET				X									
aLldpXdot3LocPowerMDISupported	ATTRIBUTE	GET				X									
aLldpXdot3LocPowerMDIEnabled	ATTRIBUTE	GET				X									
aLldpXdot3LocPowerPairControllable	ATTRIBUTE	GET				X									
aLldpXdot3LocPowerPairs	ATTRIBUTE	GET				X									
aLldpXdot3LocPowerClass	ATTRIBUTE	GET				X									
aLldpXdot3LocLinkAggStatus	ATTRIBUTE	GET								X					
aLldpXdot3LocLinkAggPortId	ATTRIBUTE	GET								X					
aLldpXdot3LocMaxFrameSize	ATTRIBUTE	GET										X			
aLldpXdot3LocPowerType	ATTRIBUTE	GET				X									
aLldpXdot3LocPowerSource	ATTRIBUTE	GET				X									
aLldpXdot3LocPowerPriority	ATTRIBUTE	GET-SET				X									
aLldpXdot3LocPDRequestedPowerValue	ATTRIBUTE	GET				X									
aLldpXdot3LocPSEAllocatedPowerValue	ATTRIBUTE	GET				X									
aLldpXdot3LocPDRequestedPowerValueA	ATTRIBUTE	GET				X									
aLldpXdot3LocPDRequestedPowerValueB	ATTRIBUTE	GET				X									
aLldpXdot3LocPSEAllocatedPowerValueA	ATTRIBUTE	GET				X									
aLldpXdot3LocPSEAllocatedPowerValueB	ATTRIBUTE	GET				X									
aLldpXdot3LocPSEPoweringStatus	ATTRIBUTE	GET				X									
aLldpXdot3LocPDPoweredStatus	ATTRIBUTE	GET				X									
aLldpXdot3LocPowerpairsExt	ATTRIBUTE	GET				X									

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Table 30–7—LLDP capabilities *(continued)*

				LLDP Basic Package (mandatory)	LLDP MAC/PHY Configuration/Status Local Package (conditional)	LLDP MAC/PHY Configuration/Status Remote Package (conditional)	LLDP Power via MDI Local Package (conditional)	LLDP Power via MDI Remote Package (conditional)	LLDP Power via MDI Measurements Local Package (conditional)	LLDP Power via MDI Measurements Remote Package (conditional)	LLDP Link Aggregation Local Package (conditional)	LLDP Link Aggregation Remote Package (conditional)	LLDP Maximum Frame Size Local Package (conditional)	LLDP Maximum Frame Size Remote Package (conditional)	LLDP EEE Local Package (optional)	LLDP EEE Remote Package (optional)
	aLldpXdot3LocPDLoad	ATTRIBUTE	GET				X									
	aLldpXdot3LocPowerClassExtA	ATTRIBUTE	GET				X									
	aLldpXdot3LocPowerClassExtB	ATTRIBUTE	GET				X									
	aLldpXdot3LocPowerClassExt	ATTRIBUTE	GET				X									
	aLldpXdot3LocPowerTypeExt	ATTRIBUTE	GET				X									
	aLldpXdot3LocPD4PID	ATTRIBUTE	GET				X									
	aLldpXdot3LocPSEMaxAvailPower	ATTRIBUTE	GET				X									
	aLldpXdot3LocPSEAutoclassSupport	ATTRIBUTE	GET				X									
	aLldpXdot3LocAutoclassCompleted	ATTRIBUTE	GET				X									
	aLldpXdot3LocAutoclassRequest	ATTRIBUTE	SET				X									
	aLldpXdot3LocPowerDownRequest	ATTRIBUTE	SET				X									
	aLldpXdot3LocPowerDownTime	ATTRIBUTE	SET				X									
	aLldpXdot3LocMeasVoltageSupport	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasCurrentSupport	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasPowerSupport	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasEnergySupport	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasurementSource	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasVoltageRequest	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasCurrentRequest	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasPowerRequest	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasEnergyRequest	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasVoltageValid	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasCurrentValid	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasPowerValid	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasEnergyValid	ATTRIBUTE	GET						X							

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Table 30–7—LLDP capabilities *(continued)*

				LLDP Basic Package (mandatory)	LLDP MAC/PHY Configuration/Status Local Package (conditional)	LLDP MAC/PHY Configuration/Status Remote Package (conditional)	LLDP Power via MDI Local Package (conditional)	LLDP Power via MDI Remote Package (conditional)	LLDP Power via MDI Measurements Local Package (conditional)	LLDP Power via MDI Measurements Remote Package (conditional)	LLDP Link Aggregation Local Package (conditional)	LLDP Link Aggregation Remote Package (conditional)	LLDP Maximum Frame Size Local Package (conditional)	LLDP Maximum Frame Size Remote Package (conditional)	LLDP EEE Local Package (optional)	LLDP EEE Remote Package (optional)
	aLldpXdot3LocMeasVoltageUncertainty	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasCurrentUncertainty	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasPowerUncertainty	ATTRIBUTE	GET						X							
	aLldpXdot3LocMeasEnergyUncertainty	ATTRIBUTE	GET						X							
	aLldpXdot3LocVoltageMeasurement	ATTRIBUTE	GET						X							
	aLldpXdot3LocCurrentMeasurement	ATTRIBUTE	GET						X							
	aLldpXdot3LocPowerMeasurement	ATTRIBUTE	GET						X							
	aLldpXdot3LocEnergyMeasurement	ATTRIBUTE	GET						X							
	aLldpXdot3LocPSEPowerPriceIndex	ATTRIBUTE	GET						X							
	aLldpXdot3LocResponseTime	ATTRIBUTE	GET				X									
	aLldpXdot3LocReady	ATTRIBUTE	GET				X									
	aLldpXdot3LocTxTwSys	ATTRIBUTE	GET												X	
	aLldpXdot3LocTxTwSysEcho	ATTRIBUTE	GET												X	
	aLldpXdot3LocRxTwSys	ATTRIBUTE	GET												X	
	aLldpXdot3LocRxTwSysEcho	ATTRIBUTE	GET												X	
	aLldpXdot3LocFbTwSys	ATTRIBUTE	GET												X	
	aLldpXdot3TxDllReady	ATTRIBUTE	GET												X	
	aLldpXdot3RxDllReady	ATTRIBUTE	GET												X	
	aLldpXdot3LocDllEnabled	ATTRIBUTE	GET												X	
	aLldpXdot3LocTxFw	ATTRIBUTE	GET												X	
	aLldpXdot3LocTxFwEcho	ATTRIBUTE	GET												X	
	aLldpXdot3LocRxFw	ATTRIBUTE	GET												X	
	aLldpXdot3LocRxFwEcho	ATTRIBUTE	GET												X	

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Table 30–7—LLDP capabilities *(continued)*

			LLDP Basic Package (mandatory)	LLDP MAC/PHY Configuration/Status Local Package (conditional)	LLDP MAC/PHY Configuration/Status Remote Package (conditional)	LLDP Power via MDI Local Package (conditional)	LLDP Power via MDI Remote Package (conditional)	LLDP Power via MDI Measurements Local Package (conditional)	LLDP Power via MDI Measurements Remote Package (conditional)	LLDP Link Aggregation Local Package (conditional)	LLDP Link Aggregation Remote Package (conditional)	LLDP Maximum Frame Size Local Package (conditional)	LLDP Maximum Frame Size Remote Package (conditional)	LLDP EEE Local Package (optional)	LLDP EEE Remote Package (optional)
oLldpXdot3RemSystemsGroup managed object class (30.12.3)																
aLldpXdot3RemPortAutoNegSupported	ATTRIBUTE	GET			X											
aLldpXdot3RemPortAutoNegEnabled	ATTRIBUTE	GET			X											
aLldpXdot3RemPortAutoNegAdvertisedCap	ATTRIBUTE	GET			X											
aLldpXdot3RemPortOperMauType	ATTRIBUTE	GET			X											
aLldpXdot3RemPowerPortClass	ATTRIBUTE	GET					X									
aLldpXdot3RemPowerMDISupported	ATTRIBUTE	GET					X									
aLldpXdot3RemPowerMDIEnabled	ATTRIBUTE	GET					X									
aLldpXdot3RemPowerPairControllable	ATTRIBUTE	GET					X									
aLldpXdot3RemPowerPairs	ATTRIBUTE	GET					X									
aLldpXdot3RemPowerClass	ATTRIBUTE	GET					X									
aLldpXdot3RemLinkAggStatus	ATTRIBUTE	GET									X					
aLldpXdot3RemLinkAggPortId	ATTRIBUTE	GET									X					
aLldpXdot3RemMaxFrameSize	ATTRIBUTE	GET											X			
aLldpXdot3RemPowerType	ATTRIBUTE	GET					X									
aLldpXdot3RemPowerSource	ATTRIBUTE	GET					X									
aLldpXdot3RemPowerPriority	ATTRIBUTE	GET					X									
aLldpXdot3RemPDRequestedPowerValue	ATTRIBUTE	GET					X									
aLldpXdot3RemPSEAllocatedPowerValue	ATTRIBUTE	GET					X									
aLldpXdot3RemPDRequestedPowerValueA	ATTRIBUTE	GET					X									
aLldpXdot3RemPDRequestedPowerValueB	ATTRIBUTE	GET					X									
aLldpXdot3RemPSEAllocatedPowerValueA	ATTRIBUTE	GET					X									
aLldpXdot3RemPSEAllocatedPowerValueB	ATTRIBUTE	GET					X									
aLldpXdot3RemPSEPoweringStatus	ATTRIBUTE	GET					X									
aLldpXdot3RemPDPoweredStatus	ATTRIBUTE	GET					X									
aLldpXdot3RemPowerPairsExt	ATTRIBUTE	GET					X									
aLldpXdot3RemPDLoad	ATTRIBUTE	GET					X									
aLldpXdot3RemPowerClassExtA	ATTRIBUTE	GET					X									

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Table 30–7—LLDP capabilities *(continued)*

				LLDP Basic Package (mandatory)	LLDP MAC/PHY Configuration/Status Local Package (conditional)	LLDP MAC/PHY Configuration/Status Remote Package (conditional)	LLDP Power via MDI Local Package (conditional)	LLDP Power via MDI Remote Package (conditional)	LLDP Power via MDI Measurements Local Package (conditional)	LLDP Power via MDI Measurements Remote Package (conditional)	LLDP Link Aggregation Local Package (conditional)	LLDP Link Aggregation Remote Package (conditional)	LLDP Maximum Frame Size Local Package (conditional)	LLDP Maximum Frame Size Remote Package (conditional)	LLDP EEE Local Package (optional)	LLDP EEE Remote Package (optional)
	aLldpXdot3RemPowerClassExtB	ATTRIBUTE	GET					X								
	aLldpXdot3RemPowerClassExt	ATTRIBUTE	GET					X								
	aLldpXdot3RemPowerTypeExt	ATTRIBUTE	GET					X								
	aLldpXdot3RemPD4PID	ATTRIBUTE	GET					X								
	aLldpXdot3RemPSEMaxAvailPower	ATTRIBUTE	GET					X								
	aLldpXdot3RemPSEAutoclassSupport	ATTRIBUTE	GET					X								
	aLldpXdot3RemAutoclassCompleted	ATTRIBUTE	GET					X								
	aLldpXdot3RemAutoclassRequest	ATTRIBUTE	GET					X								
	aLldpXdot3RemPowerDownRequest	ATTRIBUTE	GET					X								
	aLldpXdot3RemPowerDownTime	ATTRIBUTE	GET					X								
	aLldpXdot3RemMeasVoltageSupport	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasCurrentSupport	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasPowerSupport	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasEnergySupport	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasurementSource	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasVoltageRequest	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasCurrentRequest	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasPowerRequest	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasEnergyRequest	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasVoltageValid	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasCurrentValid	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasPowerValid	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasEnergyValid	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasVoltageUncertainty	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasCurrentUncertainty	ATTRIBUTE	GET							X						

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Table 30–7—LLDP capabilities *(continued)*

				LLDP Basic Package (mandatory)	LLDP MAC/PHY Configuration/Status Local Package (conditional)	LLDP MAC/PHY Configuration/Status Remote Package (conditional)	LLDP Power via MDI Local Package (conditional)	LLDP Power via MDI Remote Package (conditional)	LLDP Power via MDI Measurements Local Package (conditional)	LLDP Power via MDI Measurements Remote Package (conditional)	LLDP Link Aggregation Local Package (conditional)	LLDP Link Aggregation Remote Package (conditional)	LLDP Maximum Frame Size Local Package (conditional)	LLDP Maximum Frame Size Remote Package (conditional)	LLDP EEE Local Package (optional)	LLDP EEE Remote Package (optional)
	aLldpXdot3RemMeasPowerUncertainty	ATTRIBUTE	GET							X						
	aLldpXdot3RemMeasEnergyUncertainty	ATTRIBUTE	GET							X						
	aLldpXdot3RemVoltageMeasurement	ATTRIBUTE	GET							X						
	aLldpXdot3RemCurrentMeasurement	ATTRIBUTE	GET							X						
	aLldpXdot3RemPowerMeasurement	ATTRIBUTE	GET							X						
	aLldpXdot3RemEnergyMeasurement	ATTRIBUTE	GET							X						
	aLldpXdot3RemPSEPowerPriceIndex	ATTRIBUTE	GET							X						
	aLldpXdot3RemTxTwSys	ATTRIBUTE	GET													X
	aLldpXdot3RemTxTwSysEcho	ATTRIBUTE	GET													X
	aLldpXdot3RemRxTwSys	ATTRIBUTE	GET													X
	aLldpXdot3RemRxTwSysEcho	ATTRIBUTE	GET													X
	aLldpXdot3RemFbTwSys	ATTRIBUTE	GET													X
	aLldpXdot3RemTxFw	ATTRIBUTE	GET													X
	aLldpXdot3RemTxFwEcho	ATTRIBUTE	GET													X
	aLldpXdot3RemRxFw	ATTRIBUTE	GET													X
	aLldpXdot3RemRxFwEcho	ATTRIBUTE	GET													X

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Table 30–8—LLDP capabilities (additional packages)

				LLDP MAC Merge Package (optional)
oLldpXdot3LocSystemsGroup managed object class (30.14)				
	aLldpXdot3LocPreemptSupported	ATTRIBUTE	GET	X
	aLldpXdot3LocPreemptEnabled	ATTRIBUTE	GET	X
	aLldpXdot3LocPreemptActive	ATTRIBUTE	GET	X
	aLldpXdot3LocAddFragSize	ATTRIBUTE	GET-SET	X
	aLldpXdot3RemPreemptSupported	ATTRIBUTE	GET	X
	aLldpXdot3RemPreemptEnabled	ATTRIBUTE	GET	X
	aLldpXdot3RemPreemptActive	ATTRIBUTE	GET	X
	aLldpXdot3RemAddFragSize	ATTRIBUTE	GET	X

Table 30–9—MAC Merge sublayer capabilities

				MAC Merge Basic Package (mandatory)
oMACMergeEntity managed object class (30.14)				
	aMACMergeSupport	ATTRIBUTE	GET	X
	aMACMergeStatusVerify	ATTRIBUTE	GET	X
	aMACMergeEnableTx	ATTRIBUTE	GET-SET	X

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Table 30–9—MAC Merge sublayer capabilities *(continued)*

				MAC Merge Basic Package (mandatory)
	aMACMergeVerifyDisableTx	ATTRIBUTE	GET-SET	X
	aMACMergeStatusTx	ATTRIBUTE	GET	X
	aMACMergeVerifyTime	ATTRIBUTE	GET-SET	X
	aMACMergeAddFragSize	ATTRIBUTE	GET	X
	aMACMergeFrameAssErrorCount	ATTRIBUTE	GET	X
	aMACMergeFrameSmdErrorCount	ATTRIBUTE	GET	X
	aMACMergeFrameAssOkCount	ATTRIBUTE	GET	X
	aMACMergeFragCountRx	ATTRIBUTE	GET	X
	aMACMergeFragCountTx	ATTRIBUTE	GET	X
	aMACMergeHoldCount	ATTRIBUTE	GET	X

Table 30–10—PoDL PSE capabilities

				PoDLPSE Basic Package (mandatory)	PoDLPSE Recommended Package (optional)
oResourceTypeID managed object					
	aResourceTypeIDName	ATTRIBUTE	GET	X	
	aResourceInfo	ATTRIBUTE	GET	X	
oPoDLPSE managed object class (30.15)					
	aPoDLPSEID	ATTRIBUTE	GET	X	
	aPoDLPSEAdminState	ATTRIBUTE	GET	X	
	aPoDLPSEPowerDetectionStatus	ATTRIBUTE	GET	X	
	aPoDLPSEType	ATTRIBUTE	GET	X	
	aPoDLPSEDetectedPDType	ATTRIBUTE	GET	X	

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Table 30–10—PoDL PSE capabilities *(continued)*

				PoDLPSE Basic Package (mandatory)	PoDLPSE Recommended Package (optional)
	aPoDLPSEDetectedPDPowerClass	ATTRIBUTE	GET	X	
	aPoDLPSEInvalidSignatureCounter	ATTRIBUTE	GET		X
	aPoDLPSEInvalidClassCounter	ATTRIBUTE	GET		X
	aPoDLPSEPowerDeniedCounter	ATTRIBUTE	GET		X
	aPoDLPSEOverLoadCounter	ATTRIBUTE	GET		X
	aPoDLPSEMaintainFullVoltageSignatureAbsentCounter	ATTRIBUTE	GET		X
	aPoDLPSEActualPower	ATTRIBUTE	GET		X
	aPoDLPSEPowerAccuracy	ATTRIBUTE	GET		X
	aPoDLPSECumulativeEnergy	ATTRIBUTE	GET		X
	acPoDLPSEAdminControl	ACTION		X	
Common Attributes Template					
	aCMCounter	ATTRIBUTE	GET		X

Table 30–11—PLCA capabilities

				PLCA capability (optional)
oPLCA managed object class (30.16.1)				
	aPLCAAdminState	ATTRIBUTE	GET	X
	aPLCAStatus	ATTRIBUTE	GET	X
	aPLCABurstTimer	ATTRIBUTE	GET-SET	X
	aPLCALocalNodeID	ATTRIBUTE	GET-SET	X
	aPLCAMaxBurstCount	ATTRIBUTE	GET-SET	X
	aPLCANodeCount	ATTRIBUTE	GET-SET	X
	aPLCATransmitOpportunityTimer	ATTRIBUTE	GET-SET	X
	acPLCAAdminControl	ACTION		X
	acPLCAReset	ACTION		X

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30.3 Layer management for DTEs

30.3.1 MAC entity managed object class

This subclause formally defines the behaviours for the oMACEntity managed object class attributes, actions, and notifications.

30.3.1.1 MAC entity attributes

30.3.1.1.1 aMACID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aMACID is assigned so as to uniquely identify a MAC among the subordinate managed objects of the containing object.;

30.3.1.1.2 aFramesTransmittedOK

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of frames that are successfully transmitted. This counter is incremented when the TransmitStatus is reported as transmitOK. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).;

30.3.1.1.3 aSingleCollisionFrames

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 13 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of frames that are involved in a single collision, and are subsequently transmitted successfully. This counter is incremented when the result of a transmission is reported as transmitOK and the attempt value is 2. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.4 aMultipleCollisionFrames

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 11 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of frames that are involved in more than one collision and are subsequently transmitted

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successfully. This counter is incremented when the TransmitStatus is reported as transmitOK and the value of the attempts variable is greater than 2 and less or equal to attemptLimit. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.5 aFramesReceivedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are successfully received (receiveOK). This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented when the ReceiveStatus is reported as receiveOK. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.6 aFrameCheckSequenceErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of receive frames that are an integral number of octets in length and do not pass the FCS check. This does not include frames received with frame-too-long, or frame-too-short (frame fragment) error. This counter is incremented when the ReceiveStatus is reported as frameCheckError. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

NOTE—Coding errors detected by the Physical Layer for speeds above 10 Mb/s will cause the frame to fail the FCS check.;

30.3.1.1.7 aAlignmentErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are not an integral number of octets in length and do not pass the FCS check. This counter is incremented when the ReceiveStatus is reported as alignmentError. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3). This counter will not increment for group encoding schemes encoding greater than 4 bits per group.;

30.3.1.1.8 aOctetsTransmittedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second at 10 Mb/s

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BEHAVIOUR DEFINED AS:

A count of data and padding octets of frames that are successfully transmitted. This counter is incremented when the TransmitStatus is reported as transmitOK. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).;

30.3.1.1.9 aFramesWithDeferredXmissions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 13 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames whose transmission was delayed on its first attempt because the medium was busy. This counter is incremented when the Boolean variable deferred has been asserted by the TransmitLinkMgmt function (4.2.8). Frames involved in any collisions are not counted. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.10 aLateCollisions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of the times that a collision has been detected later than one slotTime from the start of the packet transmission. A late collision is counted twice, i.e., both as a collision and as a lateCollision. This counter is incremented when the lateCollisionCount variable is nonzero. The actual update is incremented in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.11 aFramesAbortedDueToXSColls

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 3255 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of the frames that, due to excessive collisions, are not transmitted successfully. This counter is incremented when the value of the attempts variable equals attemptLimit during a transmission. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.12 aFramesLostDueToIntMACXmitError

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

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A count of frames that would otherwise be transmitted by the station, but could not be sent due to an internal MAC sublayer transmit error. If this counter is incremented, then none of the other counters in this section are incremented. The exact meaning and mechanism for incrementing this counter is implementation dependent.;

30.3.1.1.13 aCarrierSenseErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of times that the carrierSense variable was not asserted or was deasserted during the transmission of a frame without collision. This counter is incremented when the carrierSenseFailure flag is true at the end of transmission. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.14 aOctetsReceivedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of data and padding octets in frames that are successfully received. This does not include octets in frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented when the result of a reception is reported as a receiveOK status. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.15 aFramesLostDueToIntMACRcvError

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that would otherwise be received by the station, but could not be accepted due to an internal MAC sublayer receive error. If this counter is incremented, then none of the other counters in this section are incremented. The exact meaning and mechanism for incrementing this counter is implementation dependent.;

30.3.1.1.16 aPromiscuousStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET operation returns the value “true” for promiscuous mode enabled, and “false” otherwise.

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Frames without errors received solely because this attribute has the value “true” are counted as frames received correctly; frames received in this mode that do contain errors update the appropriate error counters.

A SET operation to the value “true” provides a means to cause the LayerMgmtRecognizeAddress function to accept frames regardless of their destination address.

A SET operation to the value “false” causes the MAC sublayer to return to the normal operation of carrying out address recognition procedures for station, broadcast, and multicast group addresses (LayerMgmtRecognizeAddress function).;

30.3.1.1.17 aReadMulticastAddressList

ATTRIBUTE

APPROPRIATE SYNTAX:
SEQUENCE OF MAC addresses

BEHAVIOUR DEFINED AS:
The current multicast address list.;

30.3.1.1.18 aMulticastFramesXmittedOK

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of frames that are successfully transmitted, as indicated by the status value transmitOK, to a group destination address other than broadcast. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).;

30.3.1.1.19 aBroadcastFramesXmittedOK

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of the frames that were successfully transmitted as indicated by the TransmitStatus transmitOK, to the broadcast address. Frames transmitted to multicast addresses are not broadcast frames and are excluded. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).;

30.3.1.1.20 aFramesWithExcessiveDeferral

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 412 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

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A count of frames that deferred for an excessive period of time. This counter may only be incremented once per upper client sublayer transmission. This counter is incremented when the excessDefer flag is set. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode and also when connected to a PHY utilizing the MAC-PHY Rate Matching defined in 61.2.1.1.;

30.3.1.1.21 aMulticastFramesReceivedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are successfully received and are directed to an active nonbroadcast group address. This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.22 aBroadcastFramesReceivedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are successfully received and are directed to the broadcast group address. This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.23 aInRangeLengthErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC frames received with a Length/Type field (see 3.2.6) value between the minimum MAC client data size that does not require padding and maxBasicDataSize (see 4.2.7.1) inclusive, that does not match the number of data octets received. The counter also increments for frames whose Length/Type field value is less than the minimum allowed MAC client data size that does not require padding and the number of data octets received is greater than the minimum MAC client data size that does not require padding. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.24 aOutOfRangeLengthField

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC frames received with a Length/Type field value that is greater than maxBasicDataSize (see 4.2.7.1). The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

NOTE—Before IEEE Std 802.3x-1997, this counter was incremented by frames containing “Type” fields. Due to the modification to legitimize “Type” fields, such frames will now increment aFramesReceivedOK and this counter may only increment with a Length/Type field value that is between maxBasicDataSize and minTypeValue, exclusive (see 4.2.7.1 and 4.2.9).;

30.3.1.1.25 aFrameTooLongErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 815 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC frames received that exceed maxFrameSizeLimit (see 4.2.7.1). This counter is incremented when the status of a frame reception is frameTooLong. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.26 aMACEnableStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

True if MAC sublayer is enabled and false if disabled. This is accomplished by setting or checking the values of the receiveEnabled and transmitEnabled variables. Setting to true provides a means to cause the MAC sublayer to enter the normal operational state at idle. The PLS is reset by this operation (see 7.2.2.2.1). This is accomplished by setting receiveEnabled and transmitEnabled to true.

Setting to false causes the MAC sublayer to end all transmit and receive operations, leaving it in a disabled state. This is accomplished by setting receiveEnabled and transmitEnabled to false.;

30.3.1.1.27 aTransmitEnableStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

True if transmission is enabled and false otherwise. This is accomplished by setting or checking the value of the transmitEnabled variable.

Setting this to true provides a means to enable MAC sublayer frame transmission (TransmitFrame function). This is accomplished by setting transmitEnabled to true.

Setting this to false will inhibit the transmission of further frames by the MAC sublayer (TransmitFrame function). This is accomplished by setting transmitEnabled to false.;

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30.3.1.1.28 aMulticastReceiveStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
True if multicast receive is enabled, and false otherwise. Setting this to true provides a means to cause the MAC sublayer to return to the normal operation of multicast frame reception. Setting this to false will inhibit the reception of further multicast frames by the MAC sublayer.;

30.3.1.1.29 aReadWriteMACAddress

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
Read the MAC station address or change the MAC station address to the one supplied (RecognizeAddress function). Note that the supplied station address shall not have the group bit set and shall not be the null address.;

30.3.1.1.30 aCollisionFrames

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of 32 generalized nonresettable counters. Each counter has a maximum increment rate of 13 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A histogram of collision activity. The indices of this array (1 to attemptLimit – 1) denote the number of collisions experienced in transmitting a frame. Each element of this array contains a counter that denotes the number of frames that have experienced a specific number of collisions. When the TransmitStatus is reported as transmitOK and the value of the attempts variable equals n, then collisionFrames[n–1] counter is incremented. The elements of this array are incremented in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.31 aMACCapabilities

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE that meets the requirements of the description below:

half duplex	Capable of operating in half duplex mode
full duplex	Capable of operating in full duplex mode

BEHAVIOUR DEFINED AS:
This indicates the duplex capabilities of the MAC.;

30.3.1.1.32 aDuplexStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

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An ENUMERATED VALUE that has one of the following entries:

half duplex	Half duplex mode
full duplex	Full duplex mode
unknown	Duplex status unknown

BEHAVIOUR DEFINED AS:

A GET operation returns the current mode of operation of the MAC entity, either half duplex, full duplex, or unknown. A SET operation changes the mode of operation of the MAC entity to the indicated value. A SET operation shall have no effect on a device whose mode cannot be changed through management or that can only operate in a single mode.;

30.3.1.1.33 aRateControlAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

"True" for operating speeds above 1000 Mb/s where Rate Control through lowering the average data rate of the MAC sublayer, with frame granularity, is supported (see 4.2.3.2.2), and "false" otherwise.;

30.3.1.1.34 aRateControlStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

rate control off	Rate control mode disabled
rate control on	Rate control mode enabled
unknown	Rate control mode unknown

BEHAVIOUR DEFINED AS:

A GET operation returns the current Rate Control mode of operation of the MAC sublayer.

A SET operation changes the mode of operation of the MAC sublayer to the indicated value. A SET operation shall have no effect on a device whose mode cannot be changed through management or that can only operate in a single mode.

This attribute maps to the variable ipgStretchMode (see 4.2.7.2).;

30.3.1.1.35 aDeferControlAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

The enumeration "true" is returned when the interframe spacing is accomplished within the MAC sublayer (see 4A.2.3.2.3), the enumeration "false" is returned otherwise.;

30.3.1.1.36 aDeferControlStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

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An ENUMERATED VALUE that has one of the following entries:

unknown	defer control mode unknown
defer control off	defer control mode disabled
defer control on	defer control mode enabled

BEHAVIOUR DEFINED AS:

A GET operation returns the current Defer Control mode of operation of the MAC. A SET operation changes the mode of operation of the MAC sublayer to the indicated value. A SET operation shall have no effect on a device whose mode cannot be changed through management or that can only operate in a single mode.

This attribute maps to the variable deferenceMode (see 4A.2.7.2).;

30.3.1.1.37 aMaxFrameLength

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	Frame length capability unknown
basicFrame	Capable of supporting maxBasicFrameSize (1518 octet frames)
qTaggedFrame	Capable of supporting maxBasicFrameSize + qTagPrefixSize (1522 octet frames)
envelopeFrame	Capable of supporting maxEnvelopeFrameSize (2000 octet frames)

BEHAVIOUR DEFINED AS:

This indicates the MAC frame length at which the aFramesTooLong counter is incremented.

30.3.1.1.38 aSlowProtocolFrameLimit

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The maximum number of Slow Protocol frames of a given subtype that can be transmitted in a one-second period. The default value is 10.;

30.3.1.2 MAC entity actions

30.3.1.2.1 acInitializeMAC

ACTION

APPROPRIATE SYNTAX:

None required

BEHAVIOUR DEFINED AS:

This action provides a means to call the Initialize procedure (4.2.7.4). This action also results in the initialization of the PLS.;

30.3.1.2.2 acAddGroupAddress

ACTION

APPROPRIATE SYNTAX:

MACAddress

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BEHAVIOUR DEFINED AS:

Add the supplied multicast group address to the address recognition filter (RecognizeAddress function).;

30.3.1.2.3 acDeleteGroupAddress

ACTION

APPROPRIATE SYNTAX:

MACAddress

BEHAVIOUR DEFINED AS:

Delete the supplied multicast group address from the address recognition filter (RecognizeAddress function).;

30.3.1.2.4 acExecuteSelfTest

ACTION

APPROPRIATE SYNTAX:

None required

BEHAVIOUR DEFINED AS:

Execute a self-test and report the results (success or failure). The actual mechanism employed to carry out the self-test is not defined in this standard. If PHY loopback is accessible through a Clause 22 MII, Clause 35 GMII, or Clause 45 MDIO interface, then this action shall also invoke a data integrity test using PHY loopback, returning to normal operation on completion of the test. In the case of a Clause 45 MDIO Interface where multiple loopbacks are available, the loopback in the MMD closest to the MDI should be used.;

30.3.2 PHY device managed object class

This subclause formally defines the behaviours for the oPHYEntity managed object class attributes, actions and notifications. Management of that portion of the physical sublayer whose physical containment within the DTE is optional is outside the scope of this clause.

30.3.2.1 PHY device attributes

30.3.2.1.1 aPHYID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aPHYID is assigned so as to uniquely identify a PHY, i.e., Physical Layer among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2:1992 [SMI], Definition of management information).;

30.3.2.1.2 aPhyType

ATTRIBUTE

APPROPRIATE SYNTAX:

other	Undefined
unknown	Initializing, true state or type not yet known
none	MII present and nothing connected

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2BASE-TL	Clause 61 0.5 Mb/s to 5.5 Mb/s 64/65-octet
10 Mb/s	Clause 7 10 Mb/s Manchester
10BASE-T1L	Clause 146 10 Mb/s PAM3
10BASE-T1S	Clause 147 10 Mb/s DME
10PASS-TS	Clause 61 2.5 Mb/s to 100 Mb/s 64/65-octet
100BASE-T1	Clause 96 100 Mb/s PAM3
100BASE-T2	Clause 32 100 Mb/s PAM5X5
100BASE-T4	Clause 23 100 Mb/s 8B/6T
100BASE-X	Clause 24 or subclause 66.1 100 Mb/s 4B/5B
1000BASE-H	Clause 115 1000 Mb/s PAM16-THP
1000BASE-T	Clause 40 1000 Mb/s 4D-PAM5
1000BASE-T1	Clause 97 1000 Mb/s PAM3
1000BASE-X	Clause 36 or subclause 66.2 1000 Mb/s 8B/10B
2.5GBASE-T	Clause 126 2.5 Gb/s PAM16
2.5GBASE-T1	Clause 149 2.5 Gb/s PAM4
2.5GBASE-X	Clause 127 2.5 Gb/s 8B/10B
5GBASE-R	Clause 129 5 Gb/s 64/66B
5GBASE-T	Clause 126 5 Gb/s PAM16
5GBASE-T1	Clause 149 5 Gb/s PAM4
10/1GBASE-PRX	Clause 76 10/1G-EPON 10 Gb/s 64B/66B downstream and 1 Gb/s 8B/10B upstream
10GBASE-PR	Clause 76 10/10G-EPON 10 Gb/s 64B/66B
10GBASE-R	Clause 49 10 Gb/s 64B/66B
10GBASE-T	Clause 55 10 Gb/s DSQ128
10GBASE-T1	Clause 149 10 Gb/s PAM4
10GBASE-W	Clause 49 10 Gb/s 64B/66B and Clause 50 WIS
10GBASE-X	Clause 48 10 Gb/s 4 lane 8B/10B
10GPASS-XR	Clause 101 PCS up to 10 Gb/s 64B/66B OFDM downstream and up to 1.6 Gb/s 64B/66B OFDMA upstream
25/10GBASE-PQ	Clause 142 25/10G-EPON 256B/257B
25GBASE-PQ	Clause 142 25/25G-EPON 256B/257B
25GBASE-R	Clause 107 25 Gb/s 64B/66B
25GBASE-T	Clause 113 25 Gb/s DSQ128
40GBASE-R	Clause 82 40 Gb/s multi-PCS lane 64B/66B
40GBASE-T	Clause 113 40 Gb/s DSQ128
50/10GBASE-PQ	Clause 142 50/10G-EPON 256B/257B
50/25GBASE-PQ	Clause 142 50/25G-EPON 256B/257B
50GBASE-PQ	Clause 142 50/50G-EPON 256B/257B
50GBASE-R	Clause 133 50 Gb/s multi-PCS lane 64B/66B
100GBASE-P	Clause 82 100 Gb/s multi-PCS lane using >2-level PAM
100GBASE-R	Clause 82 100 Gb/s multi-PCS lane using 2-level PAM
200GBASE-R	Clause 119 200 Gb/s multi-PCS lane 64B/66B
400GBASE-R	Clause 119 400 Gb/s multi-PCS lane 64B/66B

BEHAVIOUR DEFINED AS:

A read-only value that identifies the PHY type. The value of this attribute maps to the value of aMAUType. The enumeration “none” can only occur in a standard implementation where an MII exists and there is nothing connected. However, the attribute aMIIDetect should be used to determine whether an MII exists or not.;

30.3.2.1.3 aPhyTypeList

ATTRIBUTE

APPROPRIATE SYNTAX:

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A SEQUENCE that meets the requirements of the description below:

other	Undefined
unknown	Initializing, true state or type not yet known
none	MII present and nothing connected
2BASE-TL	Clause 61 0.5 Mb/s to 5.5 Mb/s 64/65-octet
10 Mb/s	Clause 7 10 Mb/s Manchester
10BASE-T1L	Clause 146 10 Mb/s PAM3
10BASE-T1S	Clause 147 10 Mb/s DME
10PASS-TS	Clause 61 2.5 Mb/s to 100 Mb/s 64/65-octet
100BASE-T1	Clause 96 100 Mb/s PAM3
100BASE-T2	Clause 32 100 Mb/s PAM5X5
100BASE-T4	Clause 23 100 Mb/s 8B/6T
100BASE-X	Clause 24 or subclause 66.1 100 Mb/s 4B/5B
1000BASE-H	Clause 115 1000 Mb/s PAM16-THP
1000BASE-T	Clause 40 1000 Mb/s 4D-PAM5
1000BASE-T1	Clause 97 1000 Mb/s PAM3
1000BASE-X	Clause 36 or subclause 66.2 1000 Mb/s 8B/10B
2.5GBASE-T	Clause 126 2.5 Gb/s PAM16
2.5GBASE-T1	Clause 149 2.5 Gb/s PAM4
2.5GBASE-X	Clause 127 2.5 Gb/s 8B/10B
5GBASE-R	Clause 129 5 Gb/s 64/66B
5GBASE-T	Clause 126 5 Gb/s PAM16
5GBASE-T1	Clause 149 5 Gb/s PAM4
10/1GBASE-PRX	Clause 76 10/1G-EPON 10 Gb/s 64B/66B downstream and 1 Gb/s 8B/10B upstream
10GBASE-PR	Clause 76 10/10G-EPON 10 Gb/s 64B/66B
10GBASE-R	Clause 49 10 Gb/s 64B/66B
10GBASE-T	Clause 55 10 Gb/s DSQ128
10GBASE-T1	Clause 149 10 Gb/s PAM4
10GBASE-W	Clause 49 10 Gb/s 64B/66B and Clause 50 WIS
10GBASE-X	Clause 48 10 Gb/s 4 lane 8B/10B
10GPASS-XR	Clause 101 PCS up to 10 Gb/s 64B/66B OFDM downstream and up to 1.6 Gb/s 64B/66B OFDMA upstream
25/10GBASE-PQ	Clause 142 25/10G-EPON 256B/257B
25GBASE-PQ	Clause 142 25/25G-EPON 256B/257B
25GBASE-R	Clause 107 25 Gb/s 64B/66B
25GBASE-T	Clause 113 25 Gb/s DSQ128
40GBASE-R	Clause 82 40 Gb/s multi-PCS lane 64B/66B
40GBASE-T	Clause 113 40 Gb/s DSQ128
50/10GBASE-PQ	Clause 142 50/10G-EPON 256B/257B
50/25GBASE-PQ	Clause 142 50/25G-EPON 256B/257B
50GBASE-PQ	Clause 142 50/50G-EPON 256B/257B
50GBASE-R	Clause 133 50 Gb/s multi-PCS lane 64B/66B
100GBASE-P	Clause 82 100 Gb/s multi-PCS lane using >2-level PAM
100GBASE-R	Clause 82 100 Gb/s multi-PCS lane using 2-level PAM
200GBASE-R	Clause 119 200 Gb/s multi-PCS lane 64B/66B
400GBASE-R	Clause 119 400 Gb/s multi-PCS lane 64B/66B

BEHAVIOUR DEFINED AS:

A read-only list of the possible types that the PHY could be, identifying the ability of the PHY. If Clause 28, Clause 37, or Clause 73 Auto-Negotiation is present, then this attribute will map to the local technology ability or advertised ability of the local device.;

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NOTE—At 10 Gb/s the ability of the PMD has to be taken into account when reporting the possible types that the PHY could be.;

30.3.2.1.4 aSQETestErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of times that the SQE_TEST_ERROR was received. The SQE_TEST_ERROR is set in accordance with the rules for verification of the SQE detection mechanism in the PLS Carrier Sense function (see 7.2.4.6). The SQE test function is not a part of 100 or 1000 Mb/s PHY operation, and so SQETestErrors will not occur in 100 or 1000 Mb/s PHYs. The contents of this attribute are undefined for full duplex operation.;

30.3.2.1.5 aSymbolErrorDuringCarrier

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 160 000 counts per second for 100 Mb/s implementations

BEHAVIOUR DEFINED AS:

For 100 Mb/s operation it is a count of the number of times when valid carrier was present and there was at least one occurrence of an invalid data symbol (see 23.2.1.4, 24.2.2.1.7, and 32.3.4.1).
For half duplex operation at 1000 Mb/s, it is a count of the number of times the receiving media is non-idle (a carrier event) for a period of time equal to or greater than slotTime (see 4.2.4), and during which there was at least one occurrence of an event that causes the PHY to indicate “Data reception error” or “Carrier Extend Error” on the GMII (see Table 35–2).
For full duplex operation at 1000 Mb/s, it is a count of the number of times the receiving media is non-idle (a carrier event) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate “Data reception error” on the GMII (see Table 35–2).
For operation at 5 Gb/s, 10 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, it is a count of the number of times the receiving media is non-idle (the time between the Start of Packet Delimiter and the End of Packet Delimiter as defined by 46.2.5 and 81.2.5) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate “Receive Error” on the media independent interface (see Table 46–4 and Table 81–4).
At all speeds this counter shall be incremented only once per valid CarrierEvent and if a collision is present this counter shall not increment.;

30.3.2.1.6 aMIIDetect

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
unknown
present, nothing connected
present, connected
absent

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BEHAVIOUR DEFINED AS:

An attribute of the PhyEntity managed object class indicating whether an MII connector is physically present, and if so whether it is detectably connected as specified in 22.2.2.14.;

30.3.2.1.7 aPhyAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:
disabled
enabled

BEHAVIOUR DEFINED AS:

A disabled PHY neither transmits nor receives. The PHY shall be explicitly enabled to restore operation. The acPhyAdminControl action provides this ability. The port enable/disable function as reported by this attribute is preserved across DTE reset including loss of power. Only one PHY per MAC can be enabled at any one time. Setting a PHY to the enabled state using the action acPhyAdminControl will result in all other instances of PHY (indicated by PhyID) instantiated within the same MAC to be disabled. If a Clause 22 MII or Clause 35 GMII is present then setting this attribute to “disabled” will result in electrical isolation as defined in 22.2.4.1.6, Isolate; and setting this attribute to “enabled” will result in normal operation as defined in 22.2.4.1.5, Power down; and 22.2.4.1.6, Isolate. For all MMDs that provide a Clause 45 MDIO Interface within the PHY, setting this attribute to “enabled” will result in the MMD Low-power bit being set for normal operation. MMDs that support Low Power are the PMA/PMD MMD (see 45.2.1.1.2 and 45.2.1.2.5), the WIS MMD (see 45.2.2.1.3 and 45.2.2.2.3), the PCS MMD (see 45.2.3.1.3 and 45.2.3.2.8), the PHY XS MMD (see 45.2.4.1.3 and 45.2.4.2.8) and the DTE XS MMD (see 45.2.5.1.3 and 45.2.5.2.8).;

30.3.2.1.8 aTransmitLPIMicroseconds

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 000 000 counts per second

BEHAVIOUR DEFINED AS:

A count reflecting the amount of time that the LPI_REQUEST parameter has the value ASSERT. The request is indicated to the PHY according to the requirements of the RS (see 22.7, 35.4, 46.4).;

30.3.2.1.9 aReceiveLPIMicroseconds

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 000 000 counts per second

BEHAVIOUR DEFINED AS:

A count reflecting the amount of time that the LPI_INDICATION parameter has the value ASSERT. The indication reflects the state of the PHY according to the requirements of the RS (see 22.7, 35.4, 46.4).;

30.3.2.1.10 aTransmitLPITransitions

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 50 000 counts per second at 100 Mb/s; 90 000 counts per second at 1000 Mb/s; and 230 000 counts per second at 10 Gb/s

BEHAVIOUR DEFINED AS:

A count of occurrences of the transition from state LPI_DEASSERTED to state LPI_ASSERTED of the LPI transmit state diagram is the RS. The state transition corresponds to the assertion of the LPI_REQUEST parameter. The request is indicated to the PHY according to the requirements of the RS (see 22.7, 35.4, 46.4).;

30.3.2.1.11 aReceiveLPITransitions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 50 000 counts per second at 100 Mb/s; 90 000 counts per second at 1000 Mb/s; and 230 000 counts per second at 10 Gb/s

BEHAVIOUR DEFINED AS:

A count of occurrences of the transition from DEASSERT to ASSERT of the LPI_INDICATE parameter. The indication reflects the state of the PHY according to the requirements of the RS (see 22.7, 35.4, 46.4).;

30.3.2.2 PHY device actions

30.3.2.2.1 acPhyAdminControl

ACTION

APPROPRIATE SYNTAX:

Same as aPortAdminState

BEHAVIOUR DEFINED AS:

This action provides a means to alter aPhyAdminState. Setting a PHY to the enabled state will result in all other instances of PHY being disabled.;

30.3.3 MAC control entity object class

This subclause formally defines the behaviours for the oMACControlEntity managed object class attributes.

30.3.3.1 aMACControlID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aMACControlID is assigned so as to uniquely identify a MAC Control entity among the subordinate managed objects of the containing object.;

30.3.3.2 aMACControlFunctionsSupported

ATTRIBUTE

APPROPRIATE SYNTAX:

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A SEQUENCE that meets the requirements of the description below:

PAUSE	PAUSE command implemented
MPCP	MPCP implemented
PFC	PFC implemented
EXTENSION	EXTENSION MAC Control frame supported

BEHAVIOUR DEFINED AS:

A read-write list of the possible MAC Control functions implemented within the device. Each function implemented will have an associated MAC Control Function Entity object class.;

30.3.3.3 aMACControlFramesTransmitted

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames passed to the MAC sublayer for transmission. This counter is incremented when a MA_CONTROL.request primitive is generated within the MAC Control sublayer.;

30.3.3.4 aMACControlFramesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames passed by the MAC sublayer to the MAC Control sublayer. This counter is incremented when a ReceiveFrame function call returns a valid frame with a lengthOrType field value equal to the assigned Type for 802.3_MAC_Control as specified in 31.4.1.3.;

30.3.3.5 aUnsupportedOpcodesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames received that contain an opcode from Table 31A–1 that is not supported by the device. This counter is incremented when a ReceiveFrame function call returns a valid frame with a lengthOrType field value equal to the assigned Type for 802.3_MAC_Control as specified in 31.4.1.3, and with an opcode for a function that is not supported by the device.;

30.3.3.6 aPFCEnableStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
enabled

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disabled

BEHAVIOUR DEFINED AS:

A read-only value that indicates whether PFC MAC Control operation is enabled. The value enabled indicates that operation of PFC MAC Control is enabled and operation of PAUSE MAC Control is disabled. The value disabled indicates that transmission and reception of PFC MAC Control is not enabled and PAUSE MAC Control may operate if it has been enabled through another mechanism.;

NOTE 1—aPFCEnableStatus is read-only to avoid the risk of it being set to a conflicting value with enablement of PFC in the MAC Control Client. It is intended that an implementation locally sets the value to enabled when the MAC Control Client has PFC enabled for any priority and to disabled when the MAC Control Client has PFC disabled for all priorities.

NOTE 2—There is no mechanism in this Clause to enable and disable PAUSE transmit and receive for PHYs without Auto-Negotiation. IEEE Std 802.3.1 provides dot3PauseAdminMode to enable and disable PAUSE in the absence of Auto-Negotiation.

30.3.4 PAUSE entity managed object class

This subclause formally defines the behaviours for the oMACControlFunctionEntity managed object class attributes.

30.3.4.1 aPAUSELinkDelayAllowance

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET operation returns the value, in bits, of the allowance made by the PAUSE MAC Control entity for round-trip propagation delay of the full duplex link. A SET operation changes the value of the allowance made by the PAUSE MAC Control entity for round-trip propagation delay of the full duplex link to the indicated value, in bits.;

30.3.4.2 aPAUSEMACCtrlFramesTransmitted

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of PAUSE frames passed to the MAC sublayer for transmission. This counter is incremented when a MA_CONTROL.request primitive is generated within the MAC Control sublayer with an opcode indicating the PAUSE operation.;

30.3.4.3 aPAUSEMACCtrlFramesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames passed by the MAC sublayer to the MAC Control sublayer. This

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counter is incremented when a ReceiveFrame function call returns a valid frame with: (1) a lengthOrType field value equal to the assigned Type for 802.3_MAC_Control as specified in 31.4.1.3, and (2) an opcode indicating the PAUSE operation.;

30.3.5 MPCP managed object class

This subclause formally defines the behaviours for the oMPCP managed object class attributes and actions.

30.3.5.1 MPCP Attributes

30.3.5.1.1 aMPCPID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aMPCPID is assigned so as to uniquely identify an MPCP entity among the subordinate managed objects of the containing object.;

30.3.5.1.2 aMPCPAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational state of the Multipoint MAC Control sublayer. An interface that can provide the Multipoint MAC Control sublayer functions specified in Clause 64, Clause 77, Clause 103, or Clause 144 is enabled to do so when this attribute has the enumeration "enabled". When this attribute has the enumeration "disabled", the interface acts as it would if it had no Multipoint MAC Control sublayer. The operational state of the Multipoint MAC Control sublayer can be changed using the acMPCPAdminControl action.;

30.3.5.1.3 aMPCPMode

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
OLT
ONU
CLT
CNU

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational mode of the Multipoint MAC Control sublayer. An interface that can provide the Multipoint MAC Control sublayer functions specified in Clause 64, Clause 77, Clause 103, or Clause 144. When this attribute has the enumeration "OLT", the interface acts as an OLT. When this attribute has the enumeration "ONU", the interface acts as an ONU. When this attribute has the enumeration "CLT", the interface acts as a CLT. When this attribute has the enumeration "CNU", the interface acts as a CNU.;

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30.3.5.1.4 aMPCPLinkID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A read-only value that identifies the Logical Link identity (LLID) associated with the MAC port as specified in 65.1.3.2.2, 76.2.6.1.3.2, or 144.3.4, as appropriate.;

30.3.5.1.5 aMPCPRemoteMACAddress

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
A read-only value that identifies the source_address parameter of the last MPCPDU passed to MAC Control.

This value is updated on reception of a valid frame with (1) a destinationField equal to the assigned multicast address for MAC Control specified in 31A, (2) lengthOrType field value equal to the assigned Type for MAC Control as specified in 31A, (3) an opcode value assigned for one of MPCP messages, as specified in 31A.;

30.3.5.1.6 aMPCPRegistrationState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:

unregistered	unregistered
registering	registering with link-partner
registered	registered with a link-partner

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational state of an individual instance of Multipoint MAC Control. When this attribute has the enumeration “unregistered” the interface is ready for registering a link partner. When this attribute has the enumeration “registering” the interface is in the process of registering a link-partner. When this attribute has the enumeration “registered” the interface has an established and operational link-partner.

NOTE—This attribute may be used by layer management mechanisms or OAM client to obtain the status of logical links in P2MP networks. Specifically, in implementations where the OAM sublayer is interfaced with Multipoint MAC Control, theOAM_CTRL.request (local_link_status) primitive specified in 57.2.5.3 should be mapped to this attribute as follows:

When the value of this attribute changes from “registering” to “registered”, an OAM_CTRL.request primitive with parameter local_link_status = OK is generated.

When the value of this attribute changes from “registered” to “unregistered”, an OAM_CTRL.request primitive with parameter local_link_status = FAIL is generated.;

30.3.5.1.7 aMPCPMACCtrlFramesTransmitted

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of MPCP frames passed to the MAC sublayer for transmission.

Increment counter by one when a MA_CONTROL.request service primitive is generated within the MAC Control sublayer with an opcode indicating an MPCP frame.;

30.3.5.1.8 aMPCPMACCtrlFramesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of MPCP frames passed by the MAC sublayer to the MAC Control sublayer.

Increment counter by one when a ReceiveFrame function call returns a valid frame with: (1) a lengthOrType field value equal to the assigned Type for 802.3_MAC_Control as specified in 31.4.1.3, and (2) an opcode indicating an MPCP frame.;

30.3.5.1.9 aMPCPTxGate

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a GATE MPCP frames transmission occurs.

Increment the counter by one when a MA_CONTROL.request service primitive is generated within the MAC Control sublayer with an opcode indicating a GATE MPCPDU.;

30.3.5.1.10 aMPCPTxRegAck

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REGISTER_ACK MPCP frames transmission occurs.

Increment the counter by one when a MA_CONTROL.request service primitive is generated within the MAC Control sublayer with an opcode indicating a REGISTER_ACK MPCPDU.;

30.3.5.1.11 aMPCPTxRegister

ATTRIBUTE

APPROPRIATE SYNTAX:

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Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REGISTER MPCP frames transmission occurs.

Increment the counter by one when a MA_CONTROL.request service primitive is generated within the MAC Control sublayer with an opcode indicating a REGISTER MPCPDU.;

30.3.5.1.12 aMPCPTxRegRequest

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REGISTER_REQ MPCP frames transmission occurs.

Increment the counter by one when a MA_CONTROL.request service primitive is generated within the MAC Control sublayer with an opcode indicating a REGISTER_REQ MPCPDU.;

30.3.5.1.13 aMPCPTxReport

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REPORT MPCP frames transmission occurs.

Increment the counter by one when a MA_CONTROL.request service primitive is generated within the MAC Control sublayer with an opcode indicating a REPORT MPCPDU.;

30.3.5.1.14 aMPCPRxGate

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a GATE MPCP frames reception occurs.

Increment the counter by one when a ReceiveFrame function call returns a valid frame with: (1) a destinationField equal to the assigned multicast address for MAC Control specified in 31A, or unique physical address associated with this station, (2) a lengthOrType field value equal to the assigned Type for 802.3_MAC_Control as specified in 31.4.1.3, (3) an opcode indicating a GATE MPCPDU.;

30.3.5.1.15 aMPCPRxRegAck

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REGISTER_ACK MPCP frames reception occurs.

Increment the counter by one when a ReceiveFrame function call returns a valid frame with: (1) a destinationField equal to the assigned multicast address for MAC Control specified in 31A, (2) a lengthOrType field value equal to the assigned Type for 802.3_MAC_Control as specified in 31.4.1.3, (3) an opcode indicating a REGISTER_ACK MPCPDU.;

30.3.5.1.16 aMPCPRxRegister

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REGISTER MPCP frames reception occurs.

Increment the counter by one when a ReceiveFrame function call returns a valid frame with: (1) a destinationField equal to the unique physical address associated with this station, (2) a lengthOrType field value equal to the assigned Type for 802.3_MAC_Control as specified in 31.4.1.3, (3) an opcode indicating a REGISTER MPCPDU.;

30.3.5.1.17 aMPCPRxRegRequest

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REGISTER_REQ MPCP frames reception occurs.

Increment the counter by one when a ReceiveFrame function call returns a valid frame with: (1) a destinationField equal to the assigned multicast address for MAC Control specified in 31A, (2) a lengthOrType field value equal to the assigned Type for 802.3_MAC_Control as specified in 31.4.1.3, (3) an opcode indicating a REGISTER_REQ MPCPDU.;

30.3.5.1.18 aMPCPRxReport

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REPORT MPCP frames reception occurs.

Increment the counter by one when a ReceiveFrame function call returns a valid frame with: (1) a destinationField equal to the assigned multicast address for MAC Control specified in 31A, (2) a

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lengthOrType field value equal to the assigned Type for 802.3_MAC_Control as specified in 31.4.1.3, (3) an opcode indicating a REPORT MPCPDU.;

30.3.5.1.19 aMPCPTransmitElapsed

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A read-only value that reports the interval from last MPCP frame transmission in increments of 16 ns. The value returned shall be (interval from last MPCP frame transmission in ns)/16, where this value exceeds (2^{32}–1) the value (2^{32}–1) shall be returned.;

30.3.5.1.20 aMPCPReceiveElapsed

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A read-only value that reports the interval from last MPCP frame reception in increments of 16 ns. The value returned shall be (interval from last MPCP frame reception in ns)/16, where this value exceeds (2^{32}–1) the value (2^{32}–1) shall be returned.;

30.3.5.1.21 aMPCPRoundTripTime

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A read-only value that reports the MPCP round trip time in increments of 16 ns. The value returned shall be (round trip time in ns)/16, where this value exceeds (2^{16}–1) the value (2^{16}–1) shall be returned. This value is only defined for an OLT. The contents of this attribute are undefined for an ONU.;

30.3.5.1.22 aMPCPDiscoveryWindowsSent

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 10 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:
A count of discovery windows generated. The counter is incremented by one for each generated discovery window.;

30.3.5.1.23 aMPCPDiscoveryTimeout

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 10 000 counts

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per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a discovery time-out occurs. The counter is incremented by one for each discovery processing state diagram reset resulting from time-out waiting for message arrival.;

30.3.5.1.24 aMPCPMaximumPendingGrants

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A read-only value that indicates the maximum number of grants an ONU can store. The maximum number of grants an ONU can store has a range of 0 to 255.;

30.3.5.1.25 aMPCPRecognizedMulticastIDs

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of INTEGERS

BEHAVIOUR DEFINED AS:

A An array of read-only values that identify the multicast Logical Link identities (LLID) associated with the MAC port as specified in 65.1.3.3.2 or 76.2.6.1.3.2, as appropriate.; These values are only defined for an ONU. The contents of this attribute are undefined for an OLT.;

30.3.5.2 MPCP Actions

30.3.5.2.1 acMPCPAdminControl

ACTION

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:

This action provides a means to alter aMPCPAdminState.;

30.3.6 OAM object class

This subclause formally defines the behaviours for the oOAM managed object class attributes.

30.3.6.1 OAM Attributes

30.3.6.1.1 aOAMID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aOAMID is assigned so as to uniquely identify an OAM entity among the subordinate

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managed objects of the containing object.;

30.3.6.1.2 aOAMAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational state of the OAM sublayer.

An interface which can provide the OAM sublayer functions specified in Clause 57 will be enabled to do so when this attribute has the enumeration “enabled”. When this attribute has the enumeration “disabled” the interface will act as it would if it had no OAM sublayer. The operational state of the OAM sublayer can be changed using the acOAMAdminControl action.;

30.3.6.1.3 aOAMMode

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

passive	passive OAM mode
active	active OAM mode

BEHAVIOUR DEFINED AS:
A GET operation returns the current mode of the OAM sublayer entity (see 57.2.9), either “passive” or “active”. A SET operation changes the mode of operation of the OAM entity to the indicated value. A SET operation shall have no effect on a device whose mode cannot be changed through management or that can only operate in a single mode.;

30.3.6.1.4 aOAMDiscoveryState

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
link fault
active send local
passive wait
send local remote
send local remote ok
send any

BEHAVIOUR DEFINED AS:
A read-only value that identifies the current state of the OAM Discovery function. The enumerations match the states within the Discovery state diagram Figure 57–5.;

30.3.6.1.5 aOAMRemoteMACAddress

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:

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The value of the source_address parameter of the last OAMPDU passed by the OAM subordinate sublayer to the OAM sublayer.

This value is updated on reception of a valid frame with (1) a destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3.;

30.3.6.1.6 aOAMLocalConfiguration

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (5)]

BEHAVIOUR DEFINED AS:
A string of five bits corresponding to the OAM Configuration field (see Table 57–8) in the most recently transmitted Information OAMPDU.;

The first bit corresponds to the OAM Mode bit in the OAM Configuration field. The second bit corresponds to the Unidirectional Support bit in the OAM Configuration field. The third bit corresponds to the Remote Loopback Support bit in the OAM Configuration field. The fourth bit corresponds to the Link Events bit in the OAM Configuration field. The fifth bit corresponds to the Variable Retrieval bit in the OAM Configuration field.;

30.3.6.1.7 aOAMRemoteConfiguration

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (5)]

BEHAVIOUR DEFINED AS:
A string of five bits corresponding to the OAM Configuration field (see Table 57–8) in the most recently received Information OAMPDU.

The first bit corresponds to the OAM Mode bit in the OAM Configuration field. The second bit corresponds to the Unidirectional Support bit in the OAM Configuration field. The third bit corresponds to the Remote Loopback Support bit in the OAM Configuration field.The fourth bit corresponds to the Link Events bit in the OAM Configuration field. The fifth bit corresponds to the Variable Retrieval bit in the OAM Configuration field.

This value is updated on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAM code equals the OAM Information code as specified in Table 57–4, (5) the frame contains a Local Information TLV (see 57.5.2.1).;

30.3.6.1.8 aOAMLocalPDUConfiguration

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:

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An eleven bit value corresponding to the Maximum OAMPDU Size value within the OAMPDU Configuration field (see Table 57–9) in the most recently transmitted OAMPDU.;

30.3.6.1.9 aOAMRemotePDUConfiguration

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
An eleven bit value corresponding to the Maximum OAMPDU Size value within the OAMPDU Configuration field (see Table 57–9) in the most recently received Information OAMPDU.

This value is updated on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAM code equals the OAM Information code as specified in Table 57–4, (5) the frame contains a Local Information TLV (see 57.5.2.1).;

30.3.6.1.10 aOAMLocalFlagsField

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (7)]

BEHAVIOUR DEFINED AS:
A string of seven bits corresponding to the Flags field (see Table 57–3) in the most recently transmitted OAMPDU.

The first bit corresponds to the Link Fault bit in the Flags field. The second bit corresponds to the Dying Gasp bit in the Flags field. The third bit corresponds to the Critical Event bit in the Flags field. The fourth bit corresponds to the Local Evaluating bit in the Flags field. The fifth bit corresponds to the Local Stable bit in the Flags field. The sixth bit corresponds to the Remote Evaluating bit in the Flags field. The seventh bit corresponds to the Remote Stable bit in the Flags field.;

30.3.6.1.11 aOAMRemoteFlagsField

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (7)]

BEHAVIOUR DEFINED AS:
A string of seven bits corresponding to the Flags field (see Table 57–3) in the most recently received OAMPDU.

The first bit corresponds to the Link Fault bit in the Flags field. The second bit corresponds to the Dying Gasp bit in the Flags field. The third bit corresponds to the Critical Event bit in the Flags field. The fourth bit corresponds to the Local Evaluating bit in the Flags field. The fifth bit corresponds to the Local Stable bit in the Flags field. The sixth bit corresponds to the Remote Evaluating bit in the Flags field. The seventh bit corresponds to the Remote Stable bit in the Flags field.

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This value is updated on reception of a valid frame with (1) a destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAM code equals one of the codes as specified in Table 57–4.;

30.3.6.1.12 aOAMLocalRevision

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of the Revision field (see 57.5.2.1) in the Local Information TLV of the most recently transmitted Information OAMPDU.;

30.3.6.1.13 aOAMRemoteRevision

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of the Revision field (see 57.5.2.1) in the Local Information TLV of the most recently received Information OAMPDU.

This value is updated on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAMPDU code equal to the Information code as specified in Table 57–4, (5) the frame contains a Local Information TLV (see 57.5.2.1).;

30.3.6.1.14 aOAMLocalState

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (3)]

BEHAVIOUR DEFINED AS:
A string of three bits corresponding to the State field (see Table 57–7) of the most recently transmitted Information OAMPDU. The first and second bits corresponds to the Parser Action bits in the State field. The third bit corresponds to the Multiplexer Action bit in the State field.;

30.3.6.1.15 aOAMRemoteState

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (3)]

BEHAVIOUR DEFINED AS:
A string of three bits corresponding to the State field (see Table 57–7) of the most recently received Information OAMPDU. The first and second bits corresponds to the Parser Action bits in the State field. The third bit corresponds to the Multiplexer Action bit in the State field.

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This value is updated on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAMPDU code equal to the Information code as specified in Table 57–4, (5) the frame contains a Local Information TLV (see 57.5.2.1).;

30.3.6.1.16 aOAMRemoteVendorOUI

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of the OUI/CID field (see Table 57–10) of the most recently received Information OAMPDU.

This value is updated on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) a OAMPDU code equal to the Information code as specified in Table 57–4, (5) the frame contains a Local Information TLV (see 57.5.2.1).;

30.3.6.1.17 aOAMRemoteVendorSpecificInfo

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of the Vendor Specific Information field (see Table 57–11) of the most recently received Information OAMPDU.

This value is updated on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAMPDU code equal to the Information code as specified in Table 57–4, (5) the frame contains a Local Information TLV (see 57.5.2.1).;

30.3.6.1.18 aOAMUnsupportedCodesTx

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:
A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that are not supported by the device. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAM code for a function that is not supported by the device.;

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30.3.6.1.19 aOAMUnsupportedCodesRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs received that contain an OAM code from Table 57–4 that are not supported by the device. This counter is incremented on reception of a valid frame with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) an OAMPDU code for a function that is not supported by the device.;

30.3.6.1.20 aOAMInformationTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the OAM Information code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAMPDU code indicating an Information OAMPDU.;

30.3.6.1.21 aOAMInformationRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs received that contain the OAM Information code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the OAM Information code and is supported by the device.;

30.3.6.1.22 aOAMUniqueEventNotificationTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the

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Event Notification code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Event Notification code, (5) the Sequence Number field is not equal to the Sequence Number field of the last transmitted Event Notification OAMPDU.;

30.3.6.1.23 aOAMDuplicateEventNotificationTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the Event Notification code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Event Notification code, (5) the Sequence Number field is equal to the Sequence Number field of the last transmitted Event Notification OAMPDU.;

30.3.6.1.24 aOAMUniqueEventNotificationRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of the OAMPDUs received that contain the Event Notification code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Event Notification code, (5) the Sequence Number field is not equal to the Sequence Number field of the last received Event Notification OAMPDU and is supported by the device.;

30.3.6.1.25 aOAMDuplicateEventNotificationRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of the OAMPDUs received that contain the Event Notification code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField

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equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Event Notification code, (5) the Sequence Number field is equal to the Sequence Number field of the last received Event Notification OAMPDU.;

30.3.6.1.26 aOAMLoopbackControlTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the Loopback Control code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAM code indicating a Loopback Control OAMPDU.;

30.3.6.1.27 aOAMLoopbackControlRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs received that contain the Loopback Control code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Loopback Control code and is supported by the device.;

30.3.6.1.28 aOAMVariableRequestTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the Variable Request code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAM code indicating a Variable Request OAMPDU.;

30.3.6.1.29 aOAMVariableRequestRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of

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Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs received that contain the Variable Request code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Variable Request code and is supported by the device.;

30.3.6.1.30 aOAMVariableResponseTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the Variable Response code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAM code indicating a Variable Response OAMPDU.;

30.3.6.1.31 aOAMVariableResponseRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs received that contain the Variable Response code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Variable Response code and is supported by the device.;

30.3.6.1.32 aOAMOrganizationSpecificTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of Organization Specific OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the Organization Specific code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAM code indicating an Organization Specific OAMPDU.;

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30.3.6.1.33 aOAMOrganizationSpecificRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs received that contain the Organization Specific code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Organization Specific code and is supported by the device.;

30.3.6.1.34 aOAMLocalErrSymPeriodConfig

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two instances of the type INTEGER

BEHAVIOUR DEFINED AS:

The first integer is an eight-octet value indicating the duration of the Errored Symbol Period Event (see 57.5.3.1) window, in terms of symbols.
The second integer is an eight-octet value indicating the number of errored symbols in the period that has to be met or exceeded in order for the Errored Symbol Period Event to be generated.;

30.3.6.1.35 aOAMLocalErrSymPeriodEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Symbol Window field
The third INTEGER represents the Errored Symbol Threshold field
The fourth INTEGER represents the Errored Symbols field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently transmitted Errored Symbol Period Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4 and Event TLV Type field equal to the Errored Symbol Period Event value as specified in Table 57–12.;

30.3.6.1.36 aOAMLocalErrFrameConfig

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two instances of the type INTEGER

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BEHAVIOUR DEFINED AS:

The first integer is a two-octet value indicating the duration of the Errored Frame Event (see 57.5.3.2) window, in terms of number of 100 ms intervals. The second integer is a four-octet value indicating the number of errored frames in the period that has to be met or exceeded in order for the Errored Frame Event to be generated.;

30.3.6.1.37 aOAMLocalErrFrameEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Frame Window field
The third INTEGER represents the Errored Frame Threshold field
The fourth INTEGER represents the Errored Frames field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently transmitted Errored Frame Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4 and Event TLV Type field equal to the Errored Frame Event value as specified in Table 57–12.;

30.3.6.1.38 aOAMLocalErrFramePeriodConfig

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two instances of the type INTEGER

BEHAVIOUR DEFINED AS:

The first integer is a four-octet value indicating the duration of the Errored Frame Period Event (see 57.5.3.3) window, in terms of the number of frames in the window.

The second integer is a four-octet value indicating the number of errored frames in the period that has to be met or exceeded in order for the Errored Frame Period Event to be generated.;

30.3.6.1.39 aOAMLocalErrFramePeriodEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Frame Window field
The third INTEGER represents the Errored Frame Threshold field
The fourth INTEGER represents the Errored Frames field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently transmitted

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Errored Frame Period Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4 and Event TLV Type field equal to the Errored Frame Period Event value as specified in Table 57–12.;

30.3.6.1.40 aOAMLocalErrFrameSecsSummaryConfig

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of two instances of the type INTEGER

BEHAVIOUR DEFINED AS:
The first integer is a two-octet value indicating the duration of the Errored Frame Seconds Summary Event (see 57.5.3.4) window, in terms of number of 100 ms intervals. The second integer is a two-octet value indicating the number of errored frame seconds in the period that has to be met or exceeded in order for the Errored Frame Seconds Summary Event to be generated.;

30.3.6.1.41 aOAMLocalErrFrameSecsSummaryEvent

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Frame Seconds Summary Window field
The third INTEGER represents the Errored Frame Seconds Summary Threshold field
The fourth INTEGER represents the Errored Frame Seconds Summary field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:
A sequence of six integers corresponding to the respective fields in the most recently transmitted Errored Frame Seconds Summary Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4 and Event TLV Type field equal to the Errored Frame Seconds Summary Event value as specified in Table 57–12.;

30.3.6.1.42 aOAMRemoteErrSymPeriodEvent

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Symbol Window field
The third INTEGER represents the Errored Symbol Threshold field
The fourth INTEGER represents the Errored Symbols field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:
A sequence of six integers corresponding to the respective fields in the most recently received

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Errored Symbol Period Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4, (5) an Event TLV Type field equal to the Errored Symbol Period Event value as specified in Table 57–12.

If more than one Event TLV of the same Event Type is present within an Event Notification OAMPDU, the Event with the most recent timestamp should be used.;

30.3.6.1.43 aOAMRemoteErrFrameEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Frame Window field
The third INTEGER represents the Errored Frame Threshold field
The fourth INTEGER represents the Errored Frames field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently received Errored Frame Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4, (5) an Event TLV Type field equal to the Errored Frame Event value as specified in Table 57–12.

If more than one Event TLV of the same Event Type is present within an Event Notification OAMPDU, the Event with the most recent timestamp should be used.;

30.3.6.1.44 aOAMRemoteErrFramePeriodEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Frame Window field
The third INTEGER represents the Errored Frame Threshold field
The fourth INTEGER represents the Errored Frames field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently received

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Errored Frame Period Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4, (5) an Event TLV Type field equal to the Errored Frame Period Event value as specified in Table 57–12.

If more than one Event TLV of the same Event Type is present within an Event Notification OAMPDU, the Event with the most recent timestamp should be used.;

30.3.6.1.45 aOAMRemoteErrFrameSecsSummaryEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Frame Seconds Summary Window field
The third INTEGER represents the Errored Frame Seconds Summary Threshold field
The fourth INTEGER represents the Errored Frame Seconds Summary field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently received Errored Frame Seconds Summary Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated on reception of a valid frame, with (1) destinationField equal to the assigned multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the assigned Type for Slow_Protocols as specified in Table 57A–2, (3) Slow_Protocols subtype value equal to the subtype assigned for OAM as specified in Table 57A–3, (4) OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4, (5) an Event TLV Type field equal to the Errored Frame Seconds Summary Event value as specified in Table 57–12.

If more than one Event TLV of the same Event Type is present within an Event Notification OAMPDU, the Event with the most recent timestamp should be used.;

30.3.6.1.46 aFramesLostDueToOAMError

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that would otherwise be transmitted by the OAM sublayer, but could not be due to an internal OAM sublayer transmit error. If this counter is incremented, then none of the other counters in this section are incremented. The exact meaning and mechanism for incrementing this counter is implementation dependent.;

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30.3.6.2 OAM Actions

30.3.6.2.1 acOAMAdminControl

ACTION

APPROPRIATE SYNTAX:
Same as aPortAdminState

BEHAVIOUR DEFINED AS:
This action provides a means to alter aOAMAdminState.;

30.3.7 OMPEmulation managed object class

This subclause formally defines the behaviours for the oOMPEmulation managed object class attributes.

30.3.7.1 OMPEmulation Attributes

30.3.7.1.1aOMPEmulationID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aOAMID is assigned so as to uniquely identify an OMPEmulation entity among the subordinate managed objects of the containing object.;

30.3.7.1.2aOMPEmulationType

ATTRIBUTE

APPROPRIATE SYNTAX:
A ENUMERATION that meets the requirements of the description below:

unknown	initializing, true state or type not yet known
OLT	sublayer operating in OLT mode
ONU	sublayer operating in ONU mode

BEHAVIOUR DEFINED AS:
A read only value that indicates that mode of operation of the Reconciliation Sublayer for Point to Point Emulation (see 65.1.3.1 or 76.2.6.1.1, as appropriate).;

30.3.7.1.3aSLDErrors

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 500 000 counts per second at 1000 Mb/s

BEHAVIOUR DEFINED AS:
A count of frames received that do not contain a valid SLD field as defined in 65.1.3.3.1or 76.2.6.1.3.1, as appropriate.;

30.3.7.1.4aCRC8Errors

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 500 000 counts per second at 1000 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames received that contain a valid SLD field, as defined in 65.1.3.3.1or 76.2.6.1.3.1, as appropriate, but do not pass the CRC-8 check as defined in 65.1.3.3.3 or 76.2.6.1.3.3, as appropriate.;

30.3.7.1.5aGoodLLID

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 500 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of frames received that contain a valid SLD field in an OLT, as defined in 65.1.3.3.1 or 76.2.6.1.3.1, as appropriate, and pass the CRC-8 check, as defined in 65.1.3.3.3 or 76.2.6.1.3.3, as appropriate.;

30.3.7.1.6aONUPONcastLLID

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 500 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of frames received that: 1) contain a valid SLD field in an ONU, 2) meet the rules for frame acceptance, and 3) pass the CRC-8 check. The SLD is defined in 65.1.3.3.1 or 76.2.6.1.3.1, as appropriate. The rules for LLID acceptance are defined in 65.1.3.3.2 or 76.2.6.1.3.2, as appropriate. The CRC-8 check is defined in 65.1.3.3.3 or 76.2.6.1.3.3, as appropriate.;

30.3.7.1.7aOLTPONcastLLID

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 500 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of frames received that contain a valid SLD field in an OLT, as defined in 65.1.3.3.1 or 76.2.6.1.3.1, as appropriate, passes the CRC-8 check, as defined in 65.1.3.3.3 or 76.2.6.1.3.3, as appropriate, and the frame meets the rule for acceptance defined in 65.1.3.3.2 or 76.2.6.1.3.2, as appropriate.;

30.3.7.1.8aBadLLID

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 500 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

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A count of frames received that contain a valid SLD field in an OLT, and pass the CRC-8 check, but are discarded due to the LLID check. The SLD is defined in 65.1.3.3.1 or 76.2.6.1.3.1, as appropriate. The CRC-8 check is defined in 65.1.3.3.3 or 76.2.6.1.3.3, as appropriate. The LLID check is defined in 65.1.3.3.2 or 76.2.6.1.3.2, as appropriate.;

30.3.8 EXTENSION entity managed object class

This subclause formally defines the behaviours for the oEXTENSION managed object class attributes.

30.3.8.1 aEXTENSIONMACCtrlFramesTransmitted

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s

BEHAVIOUR DEFINED AS:

A count of EXTENSION frames passed to the MAC sublayer for transmission. This counter is incremented when a MA_CONTROL.request primitive is generated within the MAC Control sublayer with an opcode indicating the EXTENSION operation.;

30.3.8.2 aEXTENSIONMACCtrlFramesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames passed by the MAC sublayer to the MAC Control sublayer. This counter is incremented when a ReceiveFrame function call returns a valid frame with: (1) a lengthOrType field value equal to the assigned Type for 802.3_MAC_Control as specified in 31.4.1.3, and (2) an opcode indicating the EXTENSION operation.;

30.3.8.3 aEXTENSIONMACCtrlStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries: enabled disabled

BEHAVIOUR DEFINED AS:

A read-write value that identifies the current (when read) or target (when set) operational state of the EXTENSION MAC Control function (when read), as specified in Annex 31C.;

30.4 Layer management for 10, 100, and 1000 Mb/s baseband repeaters

30.4.1 Repeater managed object class

This subclause formally defines the behaviours for the oRepeater managed object class, attributes, actions, and notifications.

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30.4.1.1 Repeater attributes

30.4.1.1.1 aRepeaterID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aRepeaterID is assigned so as to uniquely identify a repeater among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2:1992 [SMI], Definition of management information).;

30.4.1.1.2 aRepeaterType

ATTRIBUTE

APPROPRIATE SYNTAX:
An INTEGER that meets the requirements of the following description:

9	10 Mb/s Baseband
271	100 Mb/s Baseband, Class I
272	100 Mb/s Baseband, Class II
41	1000 Mb/s Baseband
other	See 30.2.5
unknown	Initializing, true state or type not yet known

BEHAVIOUR DEFINED AS:
Returns a value that identifies the CSMA/CD repeater type. The enumeration of the type is such that the value matches the clause number of the standard that specifies the particular repeater, with further numerical identification for the repeater classes within the same clause.;

30.4.1.1.3 aRepeaterGroupCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aRepeaterGroupCapacity is the number of groups that can be contained within the repeater. Within each managed repeater, the groups are uniquely numbered in the range from 1 to aRepeaterGroupCapacity.

Some groups may not be present in a given repeater instance, in which case the actual number of groups present is less than aRepeaterGroupCapacity. The number of groups present is never greater than aRepeaterGroupCapacity.;

30.4.1.1.4 aGroupMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
A string of bits which reflects the current configuration of units that are viewed by group managed objects. The length of the bitstring is “aRepeaterGroupCapacity” bits. The first bit relates to group

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1. A “1” in the bitstring indicates presence of the group, “0” represents absence of the group.;

30.4.1.1.5 aRepeaterHealthState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE LIST that has the following entries:

other	undefined or unknown
ok	no known failures
repeaterFailure	known to have a repeater related failure
groupFailure	known to have a group related failure
portFailure	known to have a port related failure
generalFailure	has a failure condition, unspecified type

BEHAVIOUR DEFINED AS:

The aRepeaterHealthState attribute indicates the operational state of the repeater. The aRepeaterHealthData and aRepeaterHealthText attributes may be consulted for more specific information about the state of the repeater’s health. In case of multiple kinds of failures (e.g., repeater failure and port failure), the value of this attribute shall reflect the highest priority in the following order:
repeater failure
group failure
port failure
general failure;

30.4.1.1.6 aRepeaterHealthText

ATTRIBUTE

APPROPRIATE SYNTAX:

A PrintableString, 255 characters max

BEHAVIOUR DEFINED AS:

The aRepeaterHealthText attribute is a text string that provides information relevant to the operational state of the repeater. Repeater vendors may use this mechanism to provide detailed failure information or instructions for problem resolution.

The contents are vendor specific.;

30.4.1.1.7 aRepeaterHealthData

ATTRIBUTE

APPROPRIATE SYNTAX:

OCTET STRING, 0–255

BEHAVIOUR DEFINED AS:

The aRepeaterHealthData attribute is a block of data octets that provides information relevant to the operational state of the repeater. The encoding of this data block is vendor dependent. Repeater vendors may use this mechanism to provide detailed failure information or instructions for problem resolution.;

30.4.1.1.8 aTransmitCollisions

ATTRIBUTE

APPROPRIATE SYNTAX:

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Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

For a Clause 9 repeater, the counter increments every time the repeater state diagram enters the TRANSMIT COLLISION state from any state other than ONE PORT LEFT (Figure 9–2). For a Clause 27 repeater, the counter increments every time the Repeater Core state diagram enters the JAM state as a result of Activity(ALL) > 1 (Figure 27–2). For a Clause 41 repeater, the counter increments every time the Repeater Unit state diagram enters the JAM state (Figure 41–2).

NOTE—Some non-collision events such as false carriers will cause the repeater unit to enter the JAM state and increment this counter.;

30.4.1.2 Repeater actions

30.4.1.2.1 acResetRepeater

ACTION

APPROPRIATE SYNTAX:

None required

BEHAVIOUR DEFINED AS:

This causes a transition to the START state of Figure 9–2 for a Clause 9 repeater, to the START state of Figure 27–2 for a Clause 27 repeater, or to the START state of Figure 41–2 for a Clause 41 repeater. The repeater performs a disruptive self-test that has the following characteristics:

1. The components are not specified
2. The test resets the repeater but without affecting management information about the repeater
3. The test does not inject packets onto any segment
4. Packets received during the test may or may not be transferred
5. The test does not interfere with management functions

This causes a nRepeaterReset notification to be sent.;

30.4.1.2.2 acExecuteNonDisruptiveSelfTest

ACTION

APPROPRIATE SYNTAX:

None required

BEHAVIOUR DEFINED AS:

The repeater performs a vendor-specific, non-disruptive self-test that has the following characteristics:

1. The components are not specified
2. The test does not change the state of the repeater or management information about the repeater
3. The test does not inject packets onto any segment
4. The test does not prevent the transfer of any packets
5. Completion of the test causes a nRepeaterHealth to be sent.;

30.4.1.3 Repeater notifications

30.4.1.3.1 nRepeaterHealth

NOTIFICATION

APPROPRIATE SYNTAX:

A SEQUENCE of three data types. The first is mandatory, the following two are optional. The first

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is the value of the attribute aRepeaterHealthState. The second is the value of the attribute aRepeaterHealthText. The third is the value of the attribute aRepeaterHealthData

BEHAVIOUR DEFINED AS:

This notification conveys information related to the operational state of the repeater. See the aRepeaterHealthState, aRepeaterHealthText, and aRepeaterHealthData attributes for descriptions of the information that is sent.

The nRepeaterHealth notification is sent only when the health state of the repeater changes. The nRepeaterHealth notification shall contain repeaterHealthState. repeaterHealthData and repeaterHealthText may or may not be included. The nRepeaterHealth notification is not sent as a result of powering up a repeater.;

30.4.1.3.2 nRepeaterReset

NOTIFICATION

APPROPRIATE SYNTAX:

A SEQUENCE of three data types. The first is mandatory, the following two are optional. The first is the value of the attribute aRepeaterHealthState. The second is the value of the attribute aRepeaterHealthText. The third is the value of the attribute aRepeaterHealthData

BEHAVIOUR DEFINED AS:

This notification conveys information related to the operational state of the repeater. The nRepeaterReset notification is sent when the repeater is reset as the result of a power-on condition or upon completion of the acResetRepeater action. The nRepeaterReset notification shall contain repeaterHealthState. repeaterHealthData and repeaterHealthText may or may not be included.;

30.4.1.3.3 nGroupMapChange

NOTIFICATION

APPROPRIATE SYNTAX:

BITSTRING

BEHAVIOUR DEFINED AS:

This notification is sent when a change occurs in the group structure of a repeater. This occurs only when a group is logically removed from or added to a repeater. The nGroupMapChange notification is not sent when powering up a repeater. The value of the notification is the updated value of the aGroupMap attribute.;

30.4.2 Group managed object class

This subclause formally defines the behaviours for the oGroup managed object class, attributes, actions, and notifications.

30.4.2.1 Group attributes

30.4.2.1.1 aGroupID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A value unique within the repeater. The value of aGroupID is assigned so as to uniquely identify

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a group among the subordinate managed objects of the containing object (oRepeater). This value is never greater than aRepeaterGroupCapacity.;

30.4.2.1.2 aGroupPortCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aGroupPortCapacity is the number of ports contained within the group. Valid range is 1–1024. Within each group, the ports are uniquely numbered in the range from 1 to aGroupPortCapacity. Some ports may not be present in a given group instance, in which case the actual number of ports present is less than aGroupPortCapacity. The number of ports present is never greater than aGroupPortCapacity.;

30.4.2.1.3 aPortMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BitString

BEHAVIOUR DEFINED AS:
A string of bits that reflects the current configuration of port managed objects within this group. The length of the bitstring is "aGroupPortCapacity" bits. The first bit relates to group 1. A "1" in the bitstring indicates presence of the port, "0" represents absence of the port.;

30.4.2.2 Group notifications

30.4.2.2.1 nPortMapChange

NOTIFICATION

APPROPRIATE SYNTAX:
BitString

BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the port structure of a group. This occurs only when a port is logically removed from or added to a group. The nPortMapChange notification is not sent when powering up a repeater. The value of the notification is the updated value of the aPortMap attribute.;

30.4.3 Repeater port managed object class

This subclause formally defines the behaviours for the oRepeaterPort managed object class, attributes, actions, and notifications.

30.4.3.1 Port attributes

30.4.3.1.1 aPortID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

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BEHAVIOUR DEFINED AS:

A value unique in the group. It is assumed that ports are partitioned into groups that also have IDs. The value of aPortID is assigned so as to uniquely identify a repeater port among the subordinate managed objects of the containing object (oGroup). This value can never be greater than aGroupPortCapacity.;

30.4.3.1.2 aPortAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE LIST that has the following entries:
disabled
enabled

BEHAVIOUR DEFINED AS:

A disabled port neither transmits nor receives. The port shall be explicitly enabled to restore operation. The acPortAdminControl action provides this ability. The port enable/disable function as reported by this attribute is preserved across repeater reset including loss of power. aPortAdminState takes precedence over auto-partition and functionally operates between the auto-partition mechanism and the AUI/PMA, PCS/PMA, or GMII/PCS as applicable. For a Clause 9 and Clause 27 repeater, the port auto-partition is reinitialized upon acPortAdminControl taking the value “enabled”. For a Clause 41 repeater, the port auto-partition, receive jabber and carrier integrity functions are reinitialized upon acPortAdminControl taking the value “enabled”.;

30.4.3.1.3 aAutoPartitionState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE LIST that has the following entries:
autoPartitioned
notAutoPartitioned

BEHAVIOUR DEFINED AS:

The aAutoPartitionState flag indicates whether the port is currently partitioned by the repeater’s auto-partition protection. The conditions that cause port partitioning are specified in partition state diagram in Clause 9, Clause 27, and Clause 41. They are not differentiated here. A Clause 27 and Clause 41 repeater port partitions on entry to the PARTITION WAIT state of the partition state diagram (Figure 27–8 and Figure 41–4).;

30.4.3.1.4 aReadableFrames

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 15 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A representation of the total frames of valid frame length. Increment counter by one for each frame whose OctetCount is greater than or equal to minFrameSize and for which the FCSError and CollisionEvent signals are not asserted, and for which the attribute aFramesTooLong has not been incremented. Additionally, for 1000 Mb/s repeaters, this count shall only be incremented for frames which are received within a CarrierEvent which has a ActivityDuration of greater than or equal to (slotTime + JamSize) BT (see 4.4.2).

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NOTE—This statistic provides one of the parameters necessary for obtaining the packet error ratio.;

30.4.3.1.5 aReadableOctets

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 240 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by OctetCount for each frame which has been determined to be a readable frame.

NOTE—This statistic provides an indicator of the total data transferred.;

30.4.3.1.6 aFrameCheckSequenceErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 15 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each frame with the FCSError signal asserted and the FramingError and CollisionEvent signals deasserted and whose OctetCount is greater than or equal to minFrameSize and for which the attribute aFramesTooLong has not been incremented.;

30.4.3.1.7 aAlignmentErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 15 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each frame with the FCSError and FramingError signals asserted and CollisionEvent signal deasserted and whose OctetCount is greater than or equal to minFrameSize and for which the attribute aFramesTooLong has not been incremented. If aAlignmentErrors is incremented then the aFrameCheckSequenceErrors attribute shall not be incremented for the same frame. This counter will not increment for 8 bit wide group encoding schemes.;

30.4.3.1.8 aFramesTooLong

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 815 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each frame whose OctetCount is greater than maxFrameSizeLimit (see 4.2.7.1 and 4.4.2). If aFrameTooLong is counted then neither the aAlignmentErrors nor the aFrameCheckSequenceErrors attribute shall be incremented for the frame.

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30.4.3.1.9 aShortEvents

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each CarrierEvent with ActivityDuration less than ShortEventMaxTime. In the 10 Mb/s case ShortEventMaxTime is greater than 74 BT and less than 82 BT. ShortEventMaxTime has tolerances included to provide for circuit losses between a conformance test point at the AUI and the measurement point within the state diagram. In the 100 Mb/s case ShortEventMaxTime is 84 bits (21 nibbles), and for the 1000 Mb/s case ShortEventMaxTime is 72 bits (9 octets).

NOTE 1—shortEvents may indicate externally generated noise hits which will cause the repeater to transmit Runts to its other ports, or propagate a collision (which may be late) back to the transmitting DTE and damaged frames to the rest of the network.

NOTE 2—implementers may wish to consider selecting the ShortEventMaxTime towards the lower end of the allowed tolerance range to accommodate bit losses suffered through physical channel devices not budgeted for within this standard.

NOTE 3—Note also that the significance of this attribute is different in 10, 100, and 1000 Mb/s collision domains. Clause 9 repeaters perform fragment extension of short events which would be counted as runts on the interconnect ports of other repeaters. Clause 27 repeaters do not perform fragment extension. Clause 41 repeaters support one repeater per collision domain and do not perform fragment extension.;

30.4.3.1.10 aRunts

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each CarrierEvent that meets one of the following two conditions. Only one test need be made. a) The ActivityDuration is greater than ShortEventMaxTime and less than ValidPacketMinTime and the CollisionEvent signal is deasserted. b) The OctetCount is less than 64, the ActivityDuration is greater than ShortEventMaxTime, and the CollisionEvent signal is deasserted. For 10 and 100 Mb/s repeaters, ValidPacketMinTime is greater than or equal to 552 BT and less than 565 BT. A CarrierEvent greater than or equal to 552 BT but less than 565 BT may or may not be counted as a runt. At 10 Mb/s an event whose length is greater than 74 BT but less than 82 BT shall increment either the aShortEvents attribute or the aRunts attribute, but not both. ValidPacketMinTime has tolerances included to provide for circuit losses between a conformance test point at the AUI and the measurement point within the state diagram.
For 1000 Mb/s repeaters, ValidPacketMinTime is 4136 BT.

NOTE—Runts usually indicate collision fragments, a normal network event. In certain situations associated with large diameter networks a percentage of runts may exceed ValidPacketMinTime.;

30.4.3.1.11 aCollisions

ATTRIBUTE

APPROPRIATE SYNTAX:

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Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

This counter increments for any CarrierEvent signal on any port in which the CollisionEvent signal on this port is asserted.;

30.4.3.1.12 aLateEvents

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

For a Clause 9 repeater port this counter increments for each CarrierEvent in which the CollIn(X) variable transitions to the value SQE (see 9.6.6.2) while the ActivityDuration is greater than the LateEventThreshold. For a Clause 27 and Clause 41 repeater port this counter increments for each CarrierEvent in which the CollisionEvent signal assertion occurs while the ActivityDuration is greater than the LateEventThreshold. In both cases such a CarrierEvent is counted twice, as both an aCollision and as an aLateEvent.

For 10 and 100 Mb/s repeaters, the LateEventThreshold is greater than 480 BT and less than 565 BT. LateEventThreshold has tolerances included to permit an implementation to build a single threshold to serve as both the LateEventThreshold and ValidPacketMinTime threshold. For 1000 Mb/s repeaters, the LateEventThreshold is equal to ValidPacketMinTime.;

30.4.3.1.13 aVeryLongEvents

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 250 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

For a Clause 9 repeater port this counter increments for each CarrierEvent whose ActivityDuration is greater than the MAU Jabber Lockup Protection timer TW3 (see 9.6.1, 9.6.5). For a Clause 27 and Clause 41 repeater port this counter increments on entry to the RX JABBER state of the receive timer state diagram (Figure 27–7 and Figure 41–3). Other counters may be incremented as appropriate.;

30.4.3.1.14 aDataRateMismatches

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter

BEHAVIOUR DEFINED AS:

Increment counter by one for each frame received by this port that meets all of the conditions required by only one of the following three measurement methods:

Measurement method A, which is valid for 10 and 100 Mb/s operation only: a) The CollisionEvent signal is not asserted. b) The ActivityDuration is greater than ValidPacketMinTime. c) The received frequency (data rate) is detectably mismatched from the local transmit frequency.

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Measurement method B, which is valid for 10 and 100 Mb/s operation only: a) The CollisionEvent signal is not asserted. b) The OctetCount is greater than 63. c) The received frequency (data rate) is detectably mismatched from the local transmit frequency.

Measurement method C, which is valid for 1000 Mb/s operation only: The received frequency (data rate) is detectably mismatched from the local transmit frequency.

The exact degree of mismatch is vendor specific and is to be defined by the vendor for conformance testing. When this event occurs, other counters whose increment conditions were satisfied may or may not also be incremented, at the implementer's discretion.

NOTE—Whether or not the repeater was able to maintain data integrity is beyond the scope of this standard.;

30.4.3.1.15 aAutoPartitions

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter

BEHAVIOUR DEFINED AS:
Increment counter by one for each time that the repeater has automatically partitioned this port. The conditions that cause a Clause 9 repeater port to partition are specified in the partition state diagram in Clause 9. They are not differentiated here. A Clause 27 and Clause 41 repeater port partitions on entry to the PARTITION WAIT state of the partition state diagram (Figure 27–8 and Figure 41–4).;

30.4.3.1.16 aIsolates

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 400 counts per second at 100 Mb/s

BEHAVIOUR DEFINED AS:
Increment counter by one each time that the repeater port automatically isolates as a consequence of false carrier events. The conditions that cause a port to automatically isolate are as defined by the transition from the FALSE CARRIER state to the LINK UNSTABLE state of the carrier integrity state diagram (Figure 27–9 and Figure 41–5).

NOTE—Isolates do not affect the value of aPortAdminState.;

30.4.3.1.17 aSymbolErrorDuringPacket

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 160 000 counts per second for 100 Mb/s implementations

BEHAVIOUR DEFINED AS:
A count of the number of times when valid length packet was received at the port and there was at least one occurrence of an invalid data symbol. This can increment only once per valid CarrierEvent. A collision presence at any port of the repeater containing port N, will not cause this attribute to increment.;

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30.4.3.1.18 aLastSourceAddress

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
The Source Address of the last readable Frame received by this port.;

30.4.3.1.19 aSourceAddressChanges

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 15 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
Increment counter by one each time that the aLastSourceAddress attribute has changed.

NOTE—This may indicate whether a link is connected to a single DTE or another multi-user segment.;

30.4.3.1.20 aBursts

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 235 000 counts per second at 1000 Mb/s

BEHAVIOUR DEFINED AS:
This counter is valid for 1000 Mb/s operation only. This counter increments by one for each CarrierEvent with ActivityDuration greater than or equal to slotTime during which the CollisionEvent signal has not been asserted. Note that this counter will not increment for a 10 or 100 Mb/s port as packet bursting is not supported at these speeds.;

30.4.3.2 Port actions

30.4.3.2.1 acPortAdminControl

ACTION

APPROPRIATE SYNTAX:
Same as aPortAdminState

BEHAVIOUR DEFINED AS:
This action provides a means to alter aPortAdminState. For a Clause 9 and Clause 27 repeater it should exert a BEGIN on the Partitioning state diagram (Figure 9–6 and Figure 27–8) upon taking the value “enabled”. For a Clause 41 repeater it shall exert a BEGIN on the receive timer, partition, and carrier integrity state diagrams (Figure 41–3, Figure 41–4, and Figure 41–5) upon taking the value “enabled”.;

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30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

This subclause formally defines the behaviours for the oMAU managed object class, attributes, actions, and notifications.

The sublayer that connects directly to the media is called MAU for 10 Mb/s operation and its equivalent is the combined PMA and PMD sublayers at higher operating speeds. Because this clause defines management for use at many speeds, it needs to be able to refer to MAUs and the PMA and PMD sublayers as a group. Therefore in this clause, the term MAU will include PMA and PMD sublayers, as well as MAUs, except in those instances where it is explicitly restricted to 10 Mb/s.

30.5.1.1 MAU attributes

30.5.1.1.1 aMAUID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aMAUID is assigned so as to uniquely identify a MAU among the subordinate managed objects of the containing object.;

30.5.1.1.2 aMAUType

ATTRIBUTE

APPROPRIATE SYNTAX:
A GET-SET ENUMERATION that meets the requirements of the following description:

global	undefined
other	See 30.2.5
unknown	Initializing, true state or type not yet known
AUI	no internal MAU, view from AUI
2BASE-TL	Voice grade twisted-pair cabling PHY as specified in Clause 61 and 63
10BASE2	Thin coax MAU as specified in Clause 10
10BASE5	Thick coax MAU as specified in Clause 8
10BASE-FB	Synchronous fiber MAU as specified in Clause 17
10BASE-FL	Asynchronous fiber MAU as specified in Clause 18, duplex mode unknown
10BASE-FLFD	Asynchronous fiber MAU as specified in Clause 18, full duplex mode
10BASE-FLHD	Asynchronous fiber MAU as specified in Clause 18, half duplex mode
10BASE-FP	Passive fiber MAU as specified in Clause 16
10BASE-T	Twisted-pair cabling MAU as specified in Clause 14, duplex mode unknown
10BASE-T1L	Single balanced pair PHY as specified in Clause 146
10BASE-T1SFD	Single balanced pair PHY as specified in Clause 147, full duplex mode
10BASE-T1SHD	Single balanced pair PHY as specified in Clause 147, half duplex mode
10BASE-T1SMD	Single balanced pair PHY as specified in Clause 147, multidrop mode
10BASE-TFD	Twisted-pair cabling MAU as specified in Clause 14, full duplex mode
10BASE-THD	Twisted-pair cabling MAU as specified in Clause 14, half duplex mode
10BROAD36	Broadband DTE MAU as specified in Clause 11
10PASS-TS	Voice grade twisted-pair cabling PHY as specified in Clause 61 and 62

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FOIRL	FOIRL MAU as specified in 9.9
100BASE-BX10D	One single-mode fiber OLT PHY as specified in Clause 58
100BASE-BX10U	One single-mode fiber ONU PHY as specified in Clause 58
100BASE-FX	X fiber over PMD as specified in Clause 26, duplex mode unknown
100BASE-FXFD	X fiber over PMD as specified in Clause 26, full duplex mode
100BASE-FXHD	X fiber over PMD as specified in Clause 26, half duplex mode
100BASE-LX10	Two fiber PHY as specified in Clause 58
100BASE-T1	Single balanced twisted-pair copper cabling PHY as specified in Clause 96
100BASE-T2	Two-pair Category 3 twisted-pair cabling as specified in Clause 32, duplex mode unknown
100BASE-T2FD	Two-pair Category 3 twisted-pair cabling as specified in Clause 32, full duplex mode
100BASE-T2HD	Two-pair Category 3 twisted-pair cabling as specified in Clause 32, half duplex mode
100BASE-T4	Four-pair Category 3 twisted-pair cabling as specified in Clause 23
100BASE-TX	Two-pair Category 5 twisted-pair cabling as specified in Clause 25, duplex mode unknown
100BASE-TXFD	Two-pair Category 5 twisted-pair cabling as specified in Clause 25, full duplex mode
100BASE-TXHD	Two-pair Category 5 twisted-pair cabling as specified in Clause 25, half duplex mode
1000BASE-BX10D	One single-mode fiber OLT PHY as specified in Clause 59
1000BASE-BX10U	One single-mode fiber ONU PHY as specified in Clause 59
1000BASE-CX	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, duplex mode unknown
1000BASE-CXFD	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, full duplex mode
1000BASE-CXHD	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, half duplex mode
1000BASE-KX	X PCS/PMA over an electrical backplane PMD as specified in Clause 70
1000BASE-LX	X fiber over long-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-LX10	Two fiber 10 km PHY as specified in Clause 59
1000BASE-LXFD	X fiber over long-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-LXHD	X fiber over long-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-PX10-D	One single-mode fiber OMP OLT PHY, as specified in Clause 60, supporting a distance of at least 10 km, and a split of at least 1:16
1000BASE-PX10-U	One single-mode fiber OMP ONU PHY, as specified in Clause 60, supporting a distance of at least 10 km, and a split of at least 1:16
1000BASE-PX20-D	One single-mode fiber OMP OLT PHY, as specified in Clause 60, supporting a distance of at least 20 km, and a split of at least 1:16
1000BASE-PX20-U	One single-mode fiber OMP ONU PHY, as specified in Clause 60, supporting a distance of at least 20 km, and a split of at least 1:16
1000BASE-PX30-D	One single-mode fiber OMP OLT PHY, as specified in Clause 60, supporting a distance of at least 20 km, and a split of at least 1:32
1000BASE-PX30-U	One single-mode fiber OMP ONU PHY, as specified in Clause 60, supporting a distance of at least 20 km, and a split of at least 1:32
1000BASE-PX40-D	One single-mode fiber OMP OLT PHY as specified in Clause 60, supporting a distance of at least 20 km, and a split of at least 1:64
1000BASE-PX40-U	One single-mode fiber OMP ONU PHY as specified in Clause 60, supporting a distance of at least 20 km, and a split of at least 1:64

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1000BASE-RHA	Plastic optical fiber PHY as specified in Clause 115.
1000BASE-RHB	Plastic optical fiber PHY as specified in Clause 115.
1000BASE-RHC	Plastic optical fiber PHY as specified in Clause 115.
1000BASE-SX	X fiber over short-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-SXFD	X fiber over short-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-SXHD	X fiber over short-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-T	Four-pair Category 5 twisted-pair cabling PHY as specified in Clause 40, duplex mode unknown
1000BASE-T1	Single twisted-pair copper cable PHY as specified in Clause 97
1000BASE-TFD	Four-pair Category 5 twisted-pair cabling PHY as specified in Clause 40, full duplex mode
1000BASE-THD	Four-pair Category 5 twisted-pair cabling PHY as specified in Clause 40, half duplex mode
1000BASE-X	X PCS/PMA as specified in Clause 36 over undefined PMD, duplex mode unknown
1000BASE-XFD	X PCS/PMA as specified in Clause 36 over undefined PMD, full duplex mode
1000BASE-XHD	X PCS/PMA as specified in Clause 36 over undefined PMD, half duplex mode
2.5GBASE-KX	2.5GBASE-X PMD as specified in Clause 128 over an electrical backplane as specified in Clause 128
2.5GBASE-T	Four-pair twisted-pair balanced copper cabling PHY as specified in Clause 126
2.5GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 149
2.5GBASE-X	2.5GBASE-X PCS/PMA as specified in Clause 127 over undefined PMD
5GBASE-KR	5GBASE-KR PMD as specified in Clause 130 over an electrical backplane as specified in Clause 130
5GBASE-R	5GBASE-R PCS/PMA as specified in Clause 129 over undefined PMD
5GBASE-T	Four-pair twisted-pair balanced copper cabling PHY as specified in Clause 126
5GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 149
10/1GBASE-PRX-D1	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream OLT PHY as specified in Clause 75
10/1GBASE-PRX-D2	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream OLT PHY as specified in Clause 75
10/1GBASE-PRX-D3	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream OLT PHY as specified in Clause 75
10/1GBASE-PRX-D4	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream OLT PHY as specified in Clause 75
10/1GBASE-PRX-U1	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream ONU PHY as specified in Clause 75
10/1GBASE-PRX-U2	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream ONU PHY as specified in Clause 75
10/1GBASE-PRX-U3	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream ONU PHY as specified in Clause 75
10/1GBASE-PRX-U4	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream ONU PHY as specified in Clause 75
10GBASE-BR10-D	One single-mode fiber OLT PHY supporting a distance of at least 10 km as specified in Clause 158
10GBASE-BR10-U	One single-mode fiber ONU PHY supporting a distance of at least

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	10 km as specified in Clause 158
10GBASE-BR20-D	One single-mode fiber OLT PHY supporting a distance of at least 20 km as specified in Clause 158
10GBASE-BR20-U	One single-mode fiber ONU PHY supporting a distance of at least 20 km as specified in Clause 158
10GBASE-BR40-D	One single-mode fiber OLT PHY upporting a distance of at least 40 km as specified in Clause 158
10GBASE-BR40-U	One single-mode fiber ONU PHY supporting a distance of at least 40 km as specified in Clause 158
10GBASE-CX4	X copper over 8 pair 100-Ohm balanced cable as specified in Clause 54
10GBASE-ER	R fiber over 1550nm optics as specified in Clause 52
10GBASE-EW	W fiber over 1550nm optics as specified in Clause 52
10GBASE-KR	R PCS/PMA over an electrical backplane PMD as specified in Clause 72
10GBASE-KX4	X PCS/PMA over an electrical backplane PMD as specified in Clause 71
10GBASE-LR	R fiber over 1310nm optics as specified in Clause 52
10GBASE-LRM	R fiber over 1310 nm optics as specified in Clause 68
10GBASE-LW	W fiber over 1310nm optics as specified in Clause 52
10GBASE-LX4	X fiber over 4 lane 1310nm optics as specified in Clause 53
10GBASE-PR-D1	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream OLT PHY as specified in Clause 75
10GBASE-PR-D2	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream OLT PHY as specified in Clause 75
10GBASE-PR-D3	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream OLT PHY as specified in Clause 75
10GBASE-PR-D4	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream OLT PHY as specified in Clause 75
10GBASE-PR-U1	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream ONU PHY as specified in Clause 75
10GBASE-PR-U3	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream ONU PHY as specified in Clause 75
10GBASE–PR–U4	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream ONU PHY as specified in Clause 75
10GBASE-R	R PCS/PMA as specified in Clause 49 over undefined PMD
10GBASE-SR	R fiber over 850nm optics as specified in Clause 52
10GBASE-SW	W fiber over 850nm optics as specified in Clause 52
10GBASE-T	Four-pair twisted-pair balanced copper cabling PHY as specified in Clause 55
10GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 149
10GBASE-W	W PCS/PMA as specified in Clause 49 and 50 over undefined PMD
10GBASE-X	X PCS/PMA as specified in Clause 48 over undefined PMD
10GPASS-XR	Coax cable distribution network PHY continuous downstream/burst mode upstream PHY as specified in Clause 100 and Clause 101
25/10GBASE-PQG-D2	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, medium power class, as specified in Clause 141
25/10GBASE-PQG-D3	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, high power class, as specified in Clause 141
25/10GBASE-PQG-U2	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, medium power class, as specified in Clause 141
25/10GBASE-PQG-U3	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, high power class, as specified in Clause 141

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25/10GBASE-PQX-D2	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, medium power class, as specified in Clause 141
25/10GBASE-PQX-D3	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, high power class, as specified in Clause 141
25/10GBASE-PQX-U2	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, medium power class, as specified in Clause 141
25/10GBASE-PQX-U3	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, high power class, as specified in Clause 141
25GBASE-BR10-D	One single-mode fiber OLT PHY supporting a distance of at least 10 km as specified in Clause 159
25GBASE-BR10-U	One single-mode fiber ONU PHY supporting a distance of at least 10 km as specified in Clause 159
25GBASE-BR20-D	One single-mode fiber OLT PHY supporting a distance of at least 20 km as specified in Clause 159
25GBASE-BR20-U	One single-mode fiber ONU PHY supporting a distance of at least 20 km as specified in Clause 159
25GBASE-BR40-D	One single-mode fiber OLT PHY supporting a distance of at least 40 km as specified in Clause 159
25GBASE-BR40-U	One single-mode fiber ONU PHY supporting a distance of at least 40 km as specified in Clause 159
25GBASE-CR	25GBASE-R PCS/PMA over shielded balanced copper cable PMD as specified in Clause 110
25GBASE-CR-S	25GBASE-R PCS/PMA over shielded balanced copper cable PMD as specified in Clause 110 without support for RS-FEC
25GBASE-ER	25GBASE-R PCS/PMA over single-mode fiber PMD, with extended reach, as specified in Clause 114
25GBASE-KR	25GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 111
25GBASE-KR-S	25GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 111 without support for RS-FEC
25GBASE-LR	25GBASE-R PCS/PMA over single-mode fiber PMD, with long reach, as specified in Clause 114
25GBASE-PQG-D2	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141
25GBASE-PQG-D3	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141
25GBASE-PQG-U2	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141
25GBASE-PQG-U3	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141
25GBASE-PQX-D2	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141
25GBASE-PQX-D3	One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141

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25GBASE-PQX-U2	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141
25GBASE-PQX-U3	One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141
25GBASE-R	PCS as specified in Clause 107 with PMA as specified in Clause 109 over undefined PMD
25GBASE-SR	25GBASE-R PCS/PMA over multimode fiber PMD as specified in Clause 112
25GBASE-T	Four-pair twisted-pair balanced copper cabling PHY as specified in Clause 113
40GBASE-CR4	40GBASE-R PCS/PMA over 4 lane shielded copper balanced cable PMD as specified in Clause 85
40GBASE-ER4	40GBASE-R PCS/PMA over 4 WDM lane single mode fiber PMD, with extended reach, as specified in Clause 87
40GBASE-FR	40GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 89
40GBASE-KR4	40GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 84
40GBASE-LR4	40GBASE-R PCS/PMA over 4 WDM lane single mode fiber PMD, with long reach, as specified in Clause 87
40GBASE-R	Multi-lane PCS as specified in Clause 82 over undefined PMA/PMD
40GBASE-SR4	40GBASE-R PCS/PMA over 4 lane multimode fiber PMD as specified in Clause 86
40GBASE-T	Four-pair twisted-pair balanced copper cabling PHY as specified in Clause 113
50/10GBASE-PQG-D2	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, medium power class, as specified in Clause 141
50/10GBASE-PQG-D3	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, high power class, as specified in Clause 141
50/10GBASE-PQG-U2	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, medium power class, as specified in Clause 141
50/10GBASE-PQG-U3	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, high power class, as specified in Clause 141
50/10GBASE-PQX-D2	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, medium power class, as specified in Clause 141
50/10GBASE-PQX-D3	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, high power class, as specified in Clause 141
50/10GBASE-PQX-U2	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, medium power class, as specified in Clause 141
50/10GBASE-PQX-U3	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, high power class, as specified in Clause 141
50/25GBASE-PQG-D2	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141

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50/25GBASE-PQG-D3	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141
50/25GBASE-PQG-U2	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141
50/25GBASE-PQG-U3	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141
50/25GBASE-PQX-D2	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141
50/25GBASE-PQX-D3	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141
50/25GBASE-PQX-U2	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141
50/25GBASE-PQX-U3	One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141
50GBASE-BR10-D	One single-mode fiber OLT PHY supporting a distance of at least 10 km as specified in Clause 160
50GBASE-BR10-U	One single-mode fiber ONU PHY supporting a distance of at least 10 km as specified in Clause 160
50GBASE-BR20-D	One single-mode fiber OLT PHY supporting a distance of at least 20 km as specified in Clause 160
50GBASE-BR20-U	One single-mode fiber ONU PHY supporting a distance of at least 20 km as specified in Clause 160
50GBASE-BR40-D	One single-mode fiber OLT PHY supporting a distance of at least 40 km as specified in Clause 160
50GBASE-BR40-U	One single-mode fiber ONU PHY supporting a distance of at least 40 km as specified in Clause 160
50GBASE-CR	50GBASE-R PCS/PMA over shielded copper balanced cable PMD as specified in Clause 136
50GBASE-ER	50GBASE-R PCS/PMA over single-mode fiber PMD with reach up to at least 40 km as specified in Clause 139
50GBASE-FR	50GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 139
50GBASE-KR	50GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
50GBASE-LR	50GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 139
50GBASE-PQG-D2	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 2 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141
50GBASE-PQG-D3	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 2 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141
50GBASE-PQG-U2	One single mode fiber, 2 × 25.78125 GBd continuous reception / 2 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141
50GBASE-PQG-U3	One single mode fiber, 2 × 25.78125 GBd continuous reception /

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	2 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141
50GBASE-PQX-D2	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 2 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141
50GBASE-PQX-D3	One single mode fiber, 2 × 25.78125 GBd continuous transmission / 2 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141
50GBASE-PQX-U2	One single mode fiber, 2 × 25.78125 GBd continuous reception / 2 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141
50GBASE-PQX-U3	One single mode fiber, 2 × 25.78125 GBd continuous reception / 2 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141
50GBASE-R	Multi-lane PCS as specified in Clause 133 with PMA as specified in Clause 135 over undefined PMD
50GBASE-SR	50GBASE-R PCS/PMA over multimode fiber PMD as specified in Clause 138
100GBASE-CR2	100GBASE-R PCS/PMA over 2 lane shielded copper balanced cable PMD as specified in Clause 136
100GBASE-CR4	100GBASE-R PCS/PMA over 4 lane shielded copper balanced cable PMD as specified in Clause 92
100GBASE-CR10	100GBASE-R PCS/PMA over 10 lane shielded copper balanced cable PMD as specified in Clause 85
100GBASE-DR	100GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 140
100GBASE-ER4	100GBASE-R PCS/PMA over 4 WDM lane single mode fiber PMD, with extended reach, as specified in Clause 88
100GBASE-FR1	100GBASE-R PCS/PMA over single-mode fiber PMD with reach up to at least 2 km as specified in Clause 140
100GBASE-KP4	100GBASE-P PCS/PMA over an electrical backplane PMD as specified in Clause 94
100GBASE-KR2	100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
100GBASE-KR4	100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 93
100GBASE-LR1	100GBASE-R PCS/PMA over single-mode fiber PMD with reach up to at least 10 km as specified in Clause 140
100GBASE-LR4	100GBASE-R PCS/PMA over 4 WDM lane single mode fiber PMD, with long reach, as specified in Clause 88
100GBASE-R	Multi-lane PCS as specified in Clause 82 over undefined 100GBASE-R or 100GBASE-P PMA/PMD
100GBASE-SR2	100GBASE-R PCS/PMA over 2 lane multimode fiber PMD as specified in Clause 138
100GBASE-SR4	100GBASE-R PCS/PMA over 4 lane multimode fiber PMD as specified in Clause 95
100GBASE-SR10	100GBASE-R PCS/PMA over 10 lane multimode fiber PMD as specified in Clause 86
100GBASE-ZR	100GBASE-R PCS/100GBASE-ZR PMA over a PMD with reach up to at least 80 km as specified in Clause 154
200GBASE-CR4	200GBASE-R PCS/PMA over 4 lane shielded copper balanced cable PMD as specified in Clause 136
200GBASE-DR4	200GBASE-R PCS/PMA over 4-lane single-mode fiber PMD as specified in Clause 121

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200GBASE-ER4	200GBASE-R PCS/PMA over 4 WDM lane single-mode fiber PMD with reach up to at least 40 km as specified in Clause 122
200GBASE-FR4	200GBASE-R PCS/PMA over 4 WDM lane single-mode fiber PMD with reach up to at least 2 km as specified in Clause 122
200GBASE-KR4	200GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
200GBASE-LR4	200GBASE-R PCS/PMA over 4 WDM lane single-mode fiber PMD with reach up to at least 10 km as specified in Clause 122
200GBASE-R	Multi-lane PCS as specified in Clause 119 over undefined PMA/PMD
200GBASE-SR4	200GBASE-R PCS/PMA over 4 lane multimode fiber PMD as specified in Clause 138
400GBASE-DR4	400GBASE-R PCS/PMA over 4-lane single-mode fiber PMD as specified in Clause 124
400GBASE-ER8	400GBASE-R PCS/PMA over 8 WDM lane single-mode fiber PMD with reach up to at least 40 km as specified in Clause 122
400GBASE-FR4	400GBASE-R PCS/PMA over 4 WDM lane single-mode fiber PMD with reach up to at least 2 km as specified in Clause 151
400GBASE-FR8	400GBASE-R PCS/PMA over 8 WDM lane single-mode fiber PMD with reach up to at least 2 km as specified in Clause 122
400GBASE-LR4-6	400GBASE-R PCS/PMA over 4 WDM lane single-mode fiber PMD with reach up to at least 6 km as specified in Clause 151
400GBASE-LR8	400GBASE-R PCS/PMA over 8 WDM lane single-mode fiber PMD with reach up to at least 10 km as specified in Clause 122
400GBASE-R	Multi-lane PCS as specified in Clause 119 over undefined PMA/PMD
400GBASE-SR4.2	400GBASE-R PCS/PMA over 8-lane multimode fiber PMD as specified in Clause 150
400GBASE-SR8	400GBASE-R PCS/PMA over 8-lane multimode fiber PMD as specified in Clause 138
400GBASE-SR16	400GBASE-R PCS/PMA over 16-lane multimode fiber PMD as specified in Clause 123
802.9a	Integrated services MAU as specified in IEEE Std 802.9a-1995 (withdrawn)

BEHAVIOUR DEFINED AS:

Returns a value that identifies the internal MAU type. If an AUI is to be identified to access an external MAU, the type “AUI” is returned. A SET operation to one of the possible enumerations indicated by aMAUTypeList will force the MAU into the new operating mode. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the mode force bits specified in 22.2.4.1. If a Clause 45 MDIO Interface is present, then this will map to the PCS type selection bit(s) in the 10G WIS Control 2 register specified in 45.2.2.6.6, the PCS Control 2 register specified in 45.2.3.6.1, the PMA/PMD type selection bits in the PMA/PMD Control 2 register specified in 45.2.1.6, the PMA/PMD control 1 register specified in 45.2.1.1, the RS-FEC Enable bit in the RS-FEC control register specified in 45.2.1.116.3, and the PCS control 1 register 45.2.3.1. If Clause 28, Clause 37, or Clause 73 Auto-Negotiation is operational, then this will change the advertised ability to the single enumeration specified in the SET operation, and cause an immediate link renegotiation. A change in the MAU type will also be reflected in aPHYType.

The enumerations 1000BASE-X, 1000BASE-XHD, 1000BASE-XFD, 2.5GBASE-X, 5GBASE-R, 10GBASE-X, 10GBASE-R, 10GBASE-W, 25GBASE-R, 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R shall only be returned if the underlying PMD type is unknown.;

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30.5.1.1.3 aMAUTypeList

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of ENUMERATIONS that match the syntax of aMAUType

BEHAVIOUR DEFINED AS:

A GET attribute that returns the possible types that the MAU could be, identifying the ability of the MAU. This attribute maps to aPHYTypeList.;

30.5.1.1.4 aMediaAvailable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	undefined
unknown	initializing, true state not yet known
available	link or light normal, loopback normal
available reduced	link normal, reduced bandwidth, applies only to 2BASE-TL and 10PASS-TS
not available	link loss or low light, no loopback
remote fault	remote fault with no detail
invalid signal	invalid signal, applies only to 10BASE-FB
remote jabber	remote fault, reason known to be jabber
remote link loss	remote fault, reason known to be far-end link loss
remote test	remote fault, reason known to be test
ready	at least one PME available, applies only to 2BASE-TL and 10PASS-TS
offline	offline, applies only to Clause 37 Auto-Negotiation
auto neg error	Auto-Negotiation Error, applies only to Clause 37 Auto-Negotiation
PMD link fault	PMD/PMA receive link fault
WIS frame loss	WIS loss of frame, applies only to 10GBASE-W
WIS signal loss	WIS loss of signal, applies only to 10GBASE-W
PCS link fault	PCS receive link fault
excessive BER	PCS Bit Error Ratio monitor reporting excessive error ratio
DXS link fault	DTE XGXS receive link fault, applies only to XAUI
PXS link fault	PHY XGXS transmit link fault, applies only to XAUI

BEHAVIOUR DEFINED AS:

If the MAU is a 10 Mb/s link or fiber type (FOIRL, 10BASE-T, 10BASE-F), then this is equivalent to the link test fail state/low light function. For an AUI, 10BASE2, 10BASE5, or 10BROAD36 MAU, this indicates whether or not loopback is detected on the DI circuit. The value of this attribute persists between packets for MAU types AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP.

At power-up or following a reset, the value of this attribute will be “unknown” for AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP MAUs. For these MAUs loopback will be tested on each transmission during which no collision is detected. If DI is receiving *input* when DO returns to IDL after a transmission and there has been no collision during the transmission, then loopback will be detected. The value of this attribute will only change during noncollided transmissions for AUI, 10BASE2, 10BASE5, 10BROAD36, and 10BASE-FP MAUs.

For 100BASE-T2 and 100BASE-T4 PHYs the enumerations match the states within the respective link integrity state diagrams, Figure 32-16 and Figure 23–12. For 100BASE-TX, 100BASE-FX, 100BASE-LX10 and 100BASE-BX10 PHYs the enumerations match the states within the link integrity state diagram Figure 24–15. For 1000BASE-RHx, a link_status (see 115.3.5.4 and 45.2.3.54) of OK maps to the enumeration “available” and a link_status of FAIL maps to the

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enumeration “not available”. For 10BASE-T1L and 100BASE-T1, a link_status of OK maps to the enumeration “available”. All other states of link_status map to the enumeration “not available”. For 1000BASE-T1, a link_status of OK maps to the enumeration “available”. All other states of link_status map to the enumeration “not available”. Any MAU that implements management of Clause 28, Clause 73, or Clause 98 Auto-Negotiation will map remote fault indication to MediaAvailable “remote fault”. Any MAU that implements management of Clause 37 Auto-Negotiation will map the received RF1 and RF2 bits as specified in Table 37–3, as follows. Offline maps to the enumeration “offline”, Link_Failure maps to the enumeration “remote fault” and Auto-Negotiation Error maps to the enumeration “auto neg error”.

The enumeration “remote fault” applies to 10BASE-FB remote fault indication, the 100BASE-X far-end fault indication and nonspecified remote faults from a system running Clause 28 Auto-Negotiation. The enumerations “remote jabber”, “remote link loss”, or “remote test” should be used instead of “remote fault” where the reason for remote fault is identified in the remote signaling protocol.

Where a Clause 22 MII or Clause 35 GMII is present, a one in the remote fault bit (22.2.4.2.11) maps to the enumeration “remote fault”, a zero in the link status bit (22.2.4.2.13) maps to the enumeration “not available”. The enumeration “not available” takes precedence over “remote fault”.

For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, the enumerations map to value of the link_fault variable (see 81.3.4.1) within the Link Fault Signaling state diagram (see Figure 81–11) as follows: the values OK and Link Interruption map to the enumeration “available”, the value Local Fault maps to the enumeration “not available” and the value Remote Fault maps to the enumeration “remote fault”.

For 2BASE-TL and 10PASS-TS PHYs, the enumeration “unknown” maps to the condition where the PHY is initializing, the enumeration “ready” maps to the condition where at least one PME is available and is ready for handshake, the enumeration “available” maps to the condition where, at the PCS, at least one PME is operationally linked, the enumeration “not available” maps to the condition where the PCS is not operationally linked, the enumeration “available reduced” maps to the condition where a link fault is detected at the receive direction by one or more PMEs in the aggregation group and the enumeration “PMD link fault” maps to the condition where a link fault is detected at the receive direction by all of the PMA/PMDs in the aggregation group.

For 2.5 Gb/s, 5 Gb/s, 10 Gb/s, and 25 Gb/s the enumerations map to value of the link_fault variable within the Link Fault Signaling state diagram (Figure 46–11) as follows: the values OK and Link Interruption map to the enumeration “available”, the value Local Fault maps to the enumeration “not available” and the value Remote Fault maps to the enumeration “remote fault”. The enumeration “PMD link fault”, “WIS frame loss”, “WIS signal loss”, “PCS link fault”, “excessive BER” or “DXS link fault” should be used instead of the enumeration “not available” where the reason for the Local Fault state can be identified through the use of the Clause 45 MDIO Interface. Where multiple reasons for the Local Fault state can be identified only the highest precedence error should be reported. This precedence in descending order is as follows: “PXS link fault”, “PMD link fault”, “WIS frame loss”, “WIS signal loss”, “PCS link fault”, “excessive BER”, “DXS link fault”. Where a Clause 45 MDIO interface is present a zero in the PMA/PMD Receive link status bit (45.2.1.2.4) maps to the enumeration “PMD link fault”, a one in the LOF status bit (45.2.2.10.4) maps to the enumeration “WIS frame loss”, a one in the LOS status bit (45.2.2.10.5) maps to the enumeration “WIS signal loss”, a zero in the PCS Receive link status bit (45.2.3.2.7 or 45.2.3.87.1) maps to the enumeration “PCS link fault”, a one in the 10/40/100GBASE-R PCS Latched high BER status bit (45.2.3.16.2) or a one in the MultiGBASE-T1 PCS status 2 Latched high BER status bit (45.2.3.87.4) maps to the enumeration “excessive BER”, a zero in the DTE XS receive link status bit (45.2.5.2.7) maps to the enumeration “DXS link fault” and a zero in the PHY XS transmit link status bit (45.2.4.2.7) maps to the enumeration “PXS link fault”.;

30.5.1.1.5 aLoseMediaCounter

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 10 counts per second

BEHAVIOUR DEFINED AS:

Counts the number of times that the MediaAvailable attribute changes from the enumeration "available" to any other enumeration. Mandatory for MAU type "AUI", optional for all others.;

30.5.1.1.6 aJabber

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two indications. The first, JabberFlag, consists of an ENUMERATED value list that has the following entries:

other	undefined
unknown	initializing, true state not yet known
normal	state is true or normal
fault	state is false, fault, or abnormal

The second, jabberCounter, is a generalized nonresettable counter. This counter has a maximum increment rate of 40 counts per second

BEHAVIOUR DEFINED AS:

If the MAU is in the JABBER state, the jabberFlag portion of the attribute is set to the "fault" value. The jabberCounter portion of the attribute is incremented each time the flag is set to the "fault" value. This attribute returns the value "other" for type AUI. Note that this counter will increment for a 10 Mb/s baseband and broadband MAUs only.;

30.5.1.1.7 aMAUAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	undefined
unknown	initializing, true state not yet known
operational	powered and connected
standby	inactive but on
shutdown	similar to power down

BEHAVIOUR DEFINED AS:

A MAU in management state "standby" forces DI and CI to idle and the media transmitter to idle or fault, if supported. The management state "standby" only applies to link type MAUs. The state of MediaAvailable is unaffected. A MAU or AUI in the management state "shutdown" assumes the same condition on DI, CI and the media transmitter as if it were powered down or not connected. For an AUI, this management state will remove power from the AUI. The MAU may return the value "undefined" for Jabber and MediaAvailable attributes when it is in this management state. A MAU in the management state "operational" is fully functional, and operates and passes signals to its attached DTE or repeater port in accordance with its specification.;

30.5.1.1.8 aBbMAUXmitRcvSplitType

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	undefined

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single	single-cable system
dual	dual-cable system, offset normally zero

BEHAVIOUR DEFINED AS:

Returns a value that indicates the type of frequency multiplexing/cabling system used to separate the transmit and receive paths for the 10BROAD36 MAU. All other types return “undefined”.;

30.5.1.1.9 aBroadbandFrequencies

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two instances of the type INTEGER.

The first INTEGER represents the Transmitter Carrier Frequency. The value of its INTEGER represents the frequency of the carrier divided by 250 kHz.

The second INTEGER represents the Translation Offset Frequency. The value of its INTEGER represents the frequency of the offset divided by 250 kHz

BEHAVIOUR DEFINED AS:

Returns a value that indicates the transmit carrier frequency and translation offset frequency in MHz/4 for the 10BROAD36 MAU. This allows the frequencies to be defined to a resolution of 250 kHz.;

30.5.1.1.10 aFalseCarriers

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 160 000 counts per second under maximum network load, and 10 counts per second under zero network load, for 100 Mb/s implementations. This counter has a maximum increment rate of 1 600 000 counts per second under maximum network load, and 100 000 counts per second under zero network load, for 1000 Mb/s implementations

BEHAVIOUR DEFINED AS:

A count of the number of false carrier events during IDLE in 100BASE-X and 1000BASE-X links. This counter does not increment at the symbol rate. For 100BASE-X, it can increment after a valid carrier completion at a maximum rate of once per 100 ms until the nextCarrierEvent. For 1000BASE-X, it can increment after a valid carrier completion at a maximum rate of once per 10 μs until the next CarrierEvent.

NOTE—The increased increment rate for this attribute at 1000 Mb/s relative to its increment rate at 100 Mb/s has been provided to improve its use as an indication of line quality.;

30.5.1.1.11 aBIPErrorCount

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 10 000 counts per second for 40 Gb/s and 50 Gb/s implementations and 5 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 40/50/100GBASE-R PHYs and 100GBASE-P PHYS, an array of BIP error counters. The counters do not increment for other PHY types. The indices of this array (0 to n – 1) denote the PCS lane number where n is the number of PCS lanes in use. Each element of this array contains

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a count of BIP errors for that PCS lane. Increment the counter by one for each BIP error detected during alignment marker removal in the PCS for the corresponding lane.
If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the BIP error counters (see 45.2.3.47 and 45.2.3.48).;

30.5.1.1.12 aLaneMapping

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of INTEGERs.

BEHAVIOUR DEFINED AS:
For 40/50/100/200/400GBASE-R PHYs and 100GBASE-P PHYs, an array of PCS lane identifiers. The indices of this array (0 to n – 1) denote the service interface lane number where n is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane that has been detected in the corresponding service interface lane.
If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the Lane mapping registers (see 45.2.3.49 and 45.2.3.50).;

30.5.1.1.13 aIdleErrorCount

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
This attribute takes the eight-bit value from the 100BASE-T2 Status register (MII management register 10) bits 7:0 “Idle Error Count” as described in 100BASE-T2, 32.5.3.2.6 and 40.5.;

30.5.1.1.14 aPCSCodingViolation

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 25 000 000 counts per second for 100 Mb/s implementations and 125 000 000 counts per second for 1000 Mb/s implementations.

BEHAVIOUR DEFINED AS:
For 100 Mb/s operation it is a count of the number of events that cause the PHY to indicate “Data reception with errors” on the MII (see Table 22–2). For 1000 Mb/s operation it is a count of the number of events that cause the PHY to indicate “Data reception error” or “Carrier Extend Error” on the GMII (see Table 35–1). The contents of this attribute is undefined when FEC is operating.;

30.5.1.1.15 aFECAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
supported	FEC supported
not supported	FEC not supported

BEHAVIOUR DEFINED AS:
A read-only value that indicates if the PHY supports an optional FEC sublayer for forward error

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correction across the MDI (see 65.2, Clause 74, Clause 91, and Clause 108).

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC capability register (see 45.2.10.2 or 45.2.1.107).;

30.5.1.1.16 aFECmode

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
disabled	FEC disabled
BASE-R enabled	BASE-R FEC enabled
RS-FEC enabled	RS-FEC enabled
enabled	FEC enabled

BEHAVIOUR DEFINED AS:

A read-write value for a PHY that supports an optional FEC sublayer that indicates the mode of operation of the FEC sublayer for forward error correction across the MDI (see 65.2, Clause 74, Clause 91, and Clause 108).

A GET operation returns the current mode of operation of the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. The enumerations “BASE-R enabled” and “RS-FEC enabled” are only used for 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, and 25GBASE-KR-S PHYs where operation in the no-FEC mode maps to the enumeration “disabled”, operation in the BASE-R FEC mode maps to the enumeration “BASE-R enabled”, and operation in the RS-FEC mode maps to the enumeration “RS-FEC enabled” (see 110.6 and 111.6).

When Clause 73 Auto-Negotiation is enabled for a 25GBASE-R PHY, a SET operation is not allowed and a GET operation maps to the variables FEC_enable in Clause 74 and FEC_enable in Clause 108. When Clause 73 Auto-Negotiation is enabled for a non-25GBASE-R PHY supporting Clause 74 FEC a SET operation is not allowed and a GET operation maps to the variable FEC_enable in Clause 74.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC enable bit or to the RS-FEC enable bit in the appropriate FEC control register based upon the PHY type and the FEC operating mode (see 45.2.10.3, 45.2.1.108, and 45.2.1.116).;

30.5.1.1.17 aFECCorrectedBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs that support FEC across the MDI, an array of corrected FEC block counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1)

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denote the FEC sublayer instance number where N is the number of FEC sublayer instances in use. The number of FEC sublayer instances in use is set to one for PHYs that do not use PCS lanes or use a single FEC instance for all lanes. Each element of this array contains a count of corrected FEC blocks for that FEC sublayer instance.

Increment the counter by one for each FEC block received across the MDI that is corrected by the FEC function in the PHY for the corresponding lane or FEC sublayer instance.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC corrected blocks counter(s) (see 45.2.10.5 and 45.2.1.109 for 10GBASE-R, 45.2.3.41 for 10GBASE-PR and 10/1GBASE-PRX, 45.2.1.131 for BASE-R, 45.2.1.118 for RS-FEC, 45.2.3.62 for PCS FEC, and 45.2.1.227 for SC-FEC).;

30.5.1.1.18 aFECUncorrectableBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs that support FEC across the MDI, an array of uncorrectable FEC block counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the FEC sublayer instance number where N is the number of FEC sublayer instances in use. The number of FEC sublayer instances in use is set to one for PHYs that do not use PCS lanes or use a single FEC instance for all lanes. Each element of this array contains a count of uncorrectable FEC blocks for that FEC sublayer instance.

Increment the counter by one for each FEC block received across the MDI that is determined to be uncorrectable by the FEC function in the PHY for the corresponding lane or FEC sublayer instance.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC uncorrectable blocks counter(s) (see 45.2.10.6 and 45.2.1.110 for 10GBASE-R, 45.2.3.42 for 10GBASE-PR and 10/1GBASE-PRX, 45.2.1.149 for BASE-R, 45.2.1.119 for RS-FEC, 45.2.3.63 for PCS FEC, and 45.2.1.228 for SC-FEC).;

30.5.1.1.19 aSNROpMarginChnlA

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current SNR operating margin measured at the slicer input for channel A for the MultiGBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel A register (see 45.2.1.81).;

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30.5.1.1.20 aSNROpMarginChnlB

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel B for the MultiGBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel B register (see 45.2.1.82).;

30.5.1.1.21 aSNROpMarginChnlC

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel C for the MultiGBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel C register (see 45.2.1.83).;

30.5.1.1.22 aSNROpMarginChnlD

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel D for the MultiGBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel D register (see 45.2.1.84).;

30.5.1.1.23 aEEESupportList

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of ENUMERATIONS that match the syntax of aMAUType

BEHAVIOUR DEFINED AS:
A read-only list of the possible PHY types for which the underlying system supports Energy-Efficient Ethernet (EEE) as defined in Clause 78. If Clause 28 or Clause 73 Auto-Negotiation is present, then this attribute will map to the local technology ability or advertised ability of the local device;

30.5.1.1.24 aLDFastRetrainCount

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1000 counts per

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second

BEHAVIOUR DEFINED AS:

A count of the number of fast retrains initiated by the local device. This counter can be derived from fr_tx_counter (see 55.4.5.4, 113.4.5.4, and 126.4.5.4). If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute can be derived from the LD fast retrain count register (see 45.2.1.94.2).;

30.5.1.1.25 aLPFastRetrainCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1000 counts per second

BEHAVIOUR DEFINED AS:

A count of the number of fast retrains initiated by the link partner. This counter can be derived from fr_rx_counter (see 55.4.5.4, 113.4.5.4, and 126.4.5.4). If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute can be derived from the LP fast retrain count register (see 45.2.1.94.1).

30.5.1.1.26 aRSFECBIPErrorCount

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresetable counters. Each counter has a maximum increment rate of 5 000 counts per second for 50 Gb/s and 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R, and 100GBASE-P PHYs that support RS-FEC across the MDI, an array of BIP error counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the PCS lane number where N is the number of PCS lanes in use. Each element of this array contains a count of BIP errors for that PCS lane.
Increment the counter by one for each BIP error across the MDI detected during alignment marker removal in the PCS for the corresponding lane.
If a Clause 45 MDIO Interface is present, then this attribute maps to the BIP error counters (see 45.2.1.123 and 45.2.1.124).;

30.5.1.1.27 aRSFECLaneMapping

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of INTEGERs.

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R, and 100GBASE-P PHYs that support RS-FEC across the MDI, an array of PCS lane identifiers. The indices of this array (0 to N – 1) denote the service interface lane number where N is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane across the MDI that has been detected in the corresponding service interface lane.
If a Clause 45 MDIO Interface is present, then this attribute maps to the Lane mapping registers (see 45.2.1.125 and 45.2.1.126).;

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30.5.1.1.28 aSCFECLaneMapping

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of INTEGERs.

BEHAVIOUR DEFINED AS:
For a 100GBASE-R PHY that supports SC-FEC (see Clause 153) across the MDI, an array of PCS lane identifiers. The indices of this array (0 to N – 1) denote the service interface lane number where N is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane across the MDI that has been detected in the corresponding service interface lane.
If a Clause 45 MDIO Interface is present, then this attribute maps to the Lane mapping registers (see 45.2.1.225 and 45.2.1.226).;

30.5.1.1.29 aRSFECBypassAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
supported	FEC bypass ability supported
not supported	FEC bypass ability not supported

BEHAVIOUR DEFINED AS:
A read-only value that indicates if a PHY that supports RS-FEC across the MDI supports the optional RS-FEC bypass ability (see 91.5.3.3).
For a PHY that does not support RS-FEC across the MDI, this attribute is not applicable.
If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC status register (see 45.2.1.117).;

30.5.1.1.30 aRSFECBypassIndicationAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
supported	FEC error indication bypass ability supported
not supported	FEC error indication bypass ability not supported

BEHAVIOUR DEFINED AS:
A read-only value that indicates if a PHY that supports RS-FEC across the MDI supports the optional RS-FEC error indication bypass ability.
For a PHY that does not support RS-FEC across the MDI, this attribute is not applicable.
If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC status register (see 45.2.1.117).;

30.5.1.1.31 aRSFECBypassEnable

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known

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disabled	FEC bypass disabled
enabled	FEC bypass enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC bypass function (see 91.5.3.3).

A GET operation returns the current mode of operation of the RS-FEC. A SET operation changes the mode of operation of the RS-FEC to the indicated value.

If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC control register (see 45.2.1.116).;

30.5.1.1.32 aRSFECBypassIndicationEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
disabled	FEC error indication bypass disabled
enabled	FEC error indication bypass enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC error indication bypass function.

A GET operation returns the current mode of operation of the RS-FEC. A SET operation changes the mode of operation of the RS-FEC to the indicated value.

If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC control register (see 45.2.1.116).;

30.5.1.1.33 aPCSFECBypassIndicationAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
supported	PCS FEC error indication bypass ability supported
not supported	PCS FEC error indication bypass ability not supported

BEHAVIOUR DEFINED AS:

For 200/400GBASE-R, a read-only value that indicates if a PHY that supports PCS-FEC across the MDI supports the optional PCS FEC error indication bypass ability (see 119.2.5.3).

For a PHY that does not support PCS-FEC across the MDI, this attribute is not applicable.

If a Clause 45 MDIO Interface is present, then this attribute maps to the PCS FEC status register (see 45.2.3.61).;

30.5.1.1.34 aPCSFECBypassIndicationEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
disabled	PCS FEC error indication bypass disabled
enabled	PCS FEC error indication bypass enabled

BEHAVIOUR DEFINED AS:

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A read-write value that indicates the mode of operation of the PCS FEC error indication bypass function (see 119.2.5.3).
A GET operation returns the current mode of operation of the PCS FEC. A SET operation changes the mode of operation of the PCS FEC to the indicated value.
If a Clause 45 MDIO Interface is present, then this attribute maps to the PCS FEC control register (see 45.2.3.60).;

30.5.1.2 MAU actions

30.5.1.2.1 acResetMAU

ACTION

APPROPRIATE SYNTAX:
None required

BEHAVIOUR DEFINED AS:
Resets the MAU in the same manner as would a power-off, power-on cycle of at least 0.5 s duration. During the 0.5 s DO, DI, and CI should be idle.;

30.5.1.2.2 acMAUAdminControl

ACTION

APPROPRIATE SYNTAX:
The same as used for aMAUAdminState

BEHAVIOUR DEFINED AS:
Executing an acMAUAdminControl action causes the MAU to assume the aMAUAdminState attribute value of one of the defined valid management states for control input. The valid inputs are “standby”, “operational”, and “shutdown” state (see the behaviour definition bMAUAdminState for the description of each of these states) except that a “standby” action to a mixing type MAU or an AUI will cause the MAU to enter the “shutdown” management state.;

30.5.1.3 MAU notifications

30.5.1.3.1 nJabber

NOTIFICATION

APPROPRIATE SYNTAX:
The same as used for aJabber

BEHAVIOUR DEFINED AS:
The notification is sent whenever a managed 10 Mb/s baseband or broadband MAU enters the JABBER state.;

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

This subclause formally defines the behaviours for the oAuto-Negotiation managed object class, attributes, actions, and notifications.

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30.6.1.1 Auto-Negotiation attributes

30.6.1.1.1 aAutoNegID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aAutoNegID is assigned so as to uniquely identify an Auto-Negotiation managed object among the subordinate managed objects of the containing object.;

30.6.1.1.2 aAutoNegAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:
An interface which has Auto-Negotiation signaling ability will be enabled to do so when this attribute is in the enabled state. If disabled then the interface will act as it would if it had no Auto-Negotiation signaling.;

30.6.1.1.3 aAutoNegRemoteSignaling

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
detected
notdetected

BEHAVIOUR DEFINED AS:
The value indicates whether the remote end of the link is operating Auto-Negotiation signaling or not. It shall take the value detected if, during the previous link negotiation, FLP Bursts, /C/ ordered sets (see 36.2.4.10) or DME signals (see 73.5 and 98.2.1.1) were received from the remote end.;

30.6.1.1.4 aAutoNegAutoConfig

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
other
configuring
complete
disabled
parallel detect fail

BEHAVIOUR DEFINED AS:
Indicates whether Auto-Negotiation signaling is in progress or has completed. The enumeration “parallel detect fail” maps to a failure in parallel detection as defined in 28.2.3.1 or 73.7.4.1.;

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30.6.1.1.5 aAutoNegLocalTechnologyAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

global	Reserved for future use
other	See 30.2.5
unknown	Initializing, true state or type not yet known
10BASE-T	10BASE-T half duplex as defined in Clause 14
10BASE-T1L	10BASE-T1L as specified in Clause 146
10BASE-T1S	10BASE-T1S as specified in Clause 147
10BASE-TFD	Full duplex 10BASE-T as defined in Clause 14 and Clause 31
100BASE-T4	100BASE-T4 half duplex as defined in Clause 23
100BASE-TX	100BASE-TX half duplex as defined in Clause 25
100BASE-TXFD	Full duplex 100BASE-TX as defined in Clause 25 and Clause 31
FDX PAUSE	PAUSE operation for full duplex links as defined in Annex 31B
FDX APAUSE	Asymmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
FDX SPAUSE	Symmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
FDX BPAUSE	Asymmetric and Symmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
100BASE-T2	100BASE-T2 half duplex as defined in Clause 32
100BASE-T2FD	Full duplex 100BASE-T2 as defined in Clause 31 and Clause 32
1000BASE-X	1000BASE-X half duplex as specified in Clause 36
1000BASE-XFD	Full duplex 1000BASE-X as specified in Clause 31 and Clause 36
1000BASE-T	1000BASE-T half duplex PHY as specified in Clause 40
1000BASE-TFD	Full duplex 1000BASE-T PHY as specified in Clause 31 and as specified in Clause 40
1000BASE-T1	1000BASE-T1 as specified in Clause 97
2.5GBASE-T	2.5GBASE-T PHY as specified in Clause 126
2.5GBASE-T1	2.5GBASE-T1 as specified in Clause 149
2.5GKX	2.5GBASE-KX as specified in Clause 128
5GBASE-T	5GBASE-T PHY as specified in Clause 126
5GBASE-T1	5GBASE-T1 as specified in Clause 149
5GKR	5GBASE-KR as specified in Clause 130
Rem Fault1	Remote fault bit 1 (RF1) as specified in Clause 37
Rem Fault2	Remote fault bit 2 (RF2) as specified in Clause 37
10GBASE-T	10GBASE-T PHY as specified in Clause 55
10GBASE-T1	10GBASE-T1 as specified in Clause 149
1000BASE-KXFD	Full duplex 1000BASE-KX as specified in Clause 70
10GBASE-KX4FD	Full duplex 10GBASE-KX4 as specified in Clause 71
10GBASE-KRFD	Full duplex 10GBASE-KR as specified in Clause 72
25GBASE-T	25GBASE-T as specified in Clause 113
25GR-S	25GBASE-CR-S as specified in Clause 110 or 25GBASE-KR-S as specified in Clause 111
25GR	25GBASE-CR as specified in Clause 110 or 25GBASE-KR as specified in Clause 111
40GBASE-KR4	40GBASE-KR4 as specified in Clause 84
40GBASE-CR4	40GBASE-CR4 as specified in Clause 85
40GBASE-T	40GBASE-T as specified in Clause 113
50GR	50GBASE-CR as specified in Clause 136 or 50GBASE-KR as specified in Clause 137

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100GBASE-CR10	100GBASE-CR10 as specified in Clause 85
100GBASE-CR4	100GBASE-CR4 as specified in Clause 92
100GBASE-KR4	100GBASE-KR4 as specified in Clause 93
100GBASE-KP4	100GBASE-KP4 as specified in Clause 94
100GR2	100GBASE-CR2 as specified in Clause 136 or 100GBASE-KR2 as specified in Clause 137
200GR4	200GBASE-CR4 as specified in Clause 136 or 200GBASE-KR4 as specified in Clause 137
Rem Fault	Remote fault bit (RF) as specified in Clause 73 and Clause 98
FEC Capable	FEC ability as specified in Clause 73 (see 73.6.5) and Clause 74
FEC Requested	FEC requested as specified in Clause 73 (see 73.6.5) and Clause 74
RS-FEC25G Req	25G RS-FEC requested as specified in Clause 73 (see 73.6.5) and Clause 108
BASE-RFEC25G Req	25G BASE-R FEC requested as specified in Clause 73 (see 73.6.5) and Clause 74
Force MS	Force MASTER-SLAVE as specified in Clause 98 (see 98.2.1.2.5)
isoethernet	IEEE Std 802.9 ISLAN-16T

BEHAVIOUR DEFINED AS:

This indicates the technology ability of the local device, as defined in Clause 28, Clause 37, Clause 73, and Clause 98.

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.;

30.6.1.1.6 aAutoNegAdvertisedTechnologyAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

Same as aAutoNegLocalTechnologyAbility

BEHAVIOUR DEFINED AS:

This GET-SET attribute maps to the technology ability of the local device, as defined in Clause 28, Clause 37, and Clause 98.

NOTE—This will in every case cause temporary link loss during link renegotiation. If set to a value incompatible with aAutoNegReceivedTechnologyAbility, link negotiation will not be successful and will cause permanent link loss.;

30.6.1.1.7 aAutoNegReceivedTechnologyAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

Same as aAutoNegLocalTechnologyAbility

BEHAVIOUR DEFINED AS:

Indicates the advertised technology ability of the remote hardware. For Clause 28 Auto-Negotiation, this attribute maps to the Technology Ability Field of the last received Auto-Negotiation link codeword(s). For Clause 37 Auto-Negotiation, this attribute maps to bits D0-D13 of the received Config_Reg Base Page (see 37.2.1). For Clause 73 Auto-Negotiation, this attribute maps to bits D10-D13 and D21-D47 of the last received link codeword Base Page (see 73.6). For Clause 98 Auto-Negotiation, this attribute maps to bits D10-D13 and D21-D47 of the last received link codeword Base Page (see 98.2.1.2).;

30.6.1.1.8 aAutoNegLocalSelectorAbility

ATTRIBUTE

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APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the selector field definitions in Annex 28A.

BEHAVIOUR DEFINED AS:

This indicates the value of the selector field of the local hardware. The Selector Field is defined in 28.2.1.2.1 for Clause 28 Auto-Negotiation, in 73.6.1 for Clause 73 Auto- Negotiation, and in 98.2.1.2.1 for Clause 98 Auto-Negotiation. The enumeration of the Selector Field indicates the standard that defines the remaining encodings for Auto-Negotiation using that value of enumeration. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration “ethernet”.;

30.6.1.1.9 aAutoNegAdvertisedSelectorAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

Same as aAutoNegLocalSelectorAbility

BEHAVIOUR DEFINED AS:

In the case of Clause 28 Auto-Negotiation, this GET-SET attribute maps to the Message Selector Field of the Auto-Negotiation link codeword. For Clause 73 Auto-Negotiation, this attribute maps to the Selector Field of the Clause 73 Auto-Negotiation link codeword (see 73.6.1). For Clause 98 Auto-Negotiation, this attribute maps to the Selector Field of the Clause 98 Auto-Negotiation link codeword (see 98.2.1.2.1). A SET operation to a value not available in aAutoNegLocalSelectorAbility will be rejected. A successful SET operation will result in immediate link renegotiation if aAutoNegAdminState is enabled. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration “ethernet”.

NOTE—This will in every case cause temporary link loss during link renegotiation. If set to a value incompatible with aAutoNegReceivedSelectorAbility, link negotiation will not be successful and will cause permanent link loss.;

30.6.1.1.10 aAutoNegReceivedSelectorAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

Same as aAutoNegLocalSelectorAbility

BEHAVIOUR DEFINED AS:

In the case of Clause 28 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware. It maps to the Message Selector Field of the last received Auto-Negotiation link codeword. For Clause 73 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware and maps to the Selector Field of the last received Clause 73 Auto-Negotiation link codeword (see 73.6.1). For Clause 98 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware and maps to the Selector Field of the last received Clause 98 Auto-Negotiation link codeword (see 98.2.1.2.1). For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration “ethernet”.;

30.6.1.2 Auto-Negotiation actions

30.6.1.2.1 acAutoNegRestartAutoConfig

ATTRIBUTE

APPROPRIATE SYNTAX:

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None required

BEHAVIOUR DEFINED AS:

Forces Auto-Negotiation to begin link renegotiation. Has no effect if Auto-Negotiation signaling is disabled.;

30.6.1.2.2 acAutoNegAdminControl

ATTRIBUTE

APPROPRIATE SYNTAX:

Same as aAutoNegAdminState

BEHAVIOUR DEFINED AS:

This action provides a means to turn Auto-Negotiation signaling on or off.;

30.7 Management for Link Aggregation

Subclause 30.7 is deprecated by IEEE Std 802.1AX-2008.

30.7.1 Aggregator managed object class

This subclause formally defines the behaviours for the oAggregator managed object class, attributes, and notifications.

Some of the attributes that are part of the definition of the oAggregator managed object class are derived by summing counter values from attributes of other objects; e.g., to generate a count of received frames for the Aggregator, the individual value for each Aggregation Port contributes to the sum. Where calculations of this form are used, the values that contribute to the Aggregator's attributes are *increments* in the values of the component attributes, not their absolute values. As any individual Aggregation Port is potentially only temporarily attached to its current Aggregator, the count values it contributes to the Aggregator's counters are the increments in its values that it has experienced during the period of time that it has been attached to that Aggregator.

The counter values defined for the Aggregator have been formulated as far as possible to make the Aggregator behave like an individual IEEE 802.3 MAC. The counts of frames received and transmitted are formulated to reflect the counts that would be expected by the MAC Client; they do not include frames transmitted and received as part of the operation of LACP or the Marker protocol, only frames that pass through the interface between the MAC Client and the Aggregator. However, as LACP and the Marker protocol are, as far as the individual MACs are concerned, part of their MAC Client, the RX/TX counters for the individual MACs will reflect both control and data traffic. As counts of errors at the port level cannot always be cleanly delineated between those that occurred as a result of aggregation activity and those that did not, no attempt has been made to separate these aspects of the port error counts. Therefore, there is not necessarily a direct correspondence between the individual MAC counters and the corresponding derived counters at the Aggregator level.

It should also be noted that the counters defined for the Aggregator include values that can only apply to half duplex links. This is consistent with the approach taken in Link Aggregation that a link that can only operate as an individual link is nonetheless considered as being attached to an Aggregator. This simplifies the modelling of managed objects for links that can operate in either half or full duplex, and ensures a consistent presentation of the attributes regardless of the type of links attached to the Aggregator.

NOTE—The operation of Auto-Negotiation may mean that a given link can operate in full duplex or half duplex, depending upon the capabilities of the device(s) connected to it. Keeping the management view the same regardless of a link's current mode of operation allows a consistent management approach to be taken across all types of links.

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30.7.1.1 Aggregator attributes

30.7.1.1.1 aAggID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The unique identifier allocated to this Aggregator by the local System. This attribute identifies an Aggregator instance among the subordinate managed objects of the containing object. This value is read-only.

30.7.1.1.2 aAggDescription

ATTRIBUTE

APPROPRIATE SYNTAX:
A PrintableString, 255 characters max.

BEHAVIOUR DEFINED AS:
A human-readable text string containing information about the Aggregator. This string could include information about the distribution algorithm in use on this Aggregator; for example, “Aggregator 1, Dist Alg=Dest MAC address”. This string is read-only. The contents are vendor specific.;

30.7.1.1.3 aAggName

ATTRIBUTE

APPROPRIATE SYNTAX:
A PrintableString, 255 characters max.

BEHAVIOUR DEFINED AS:
A human-readable text string containing a locally significant name for the Aggregator. This string is read-write.;

30.7.1.1.4 aAggActorSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
A 6-octet read-write MAC address value used as a unique identifier for the System that contains this Aggregator.

NOTE—From the perspective of the Link Aggregation mechanisms described in Clause 43, only a single combination of Actor’s System ID and System Priority are considered, and no distinction is made between the values of these parameters for an Aggregator and the port(s) that are associated with it (i.e., the protocol is described in terms of the operation of aggregation within a single System). However, the managed objects provided for the Aggregator and the port both allow management of these parameters. The result of this is to permit a single piece of equipment to be configured by management to contain more than one System from the point of view of the operation of Link Aggregation. This may be of particular use in the configuration of equipment that has limited aggregation capability (see 43.6).;

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30.7.1.1.5 aAggActorSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A 2-octet read-write value indicating the priority value associated with the Actor's System ID.;

30.7.1.1.6 aAggAggregateOrIndividual

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value indicating whether the Aggregator represents an Aggregate ("TRUE") or an Individual link ("FALSE").;

30.7.1.1.7 aAggActorAdminKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current administrative value of the Key for the Aggregator. The administrative Key value may differ from the operational Key value for the reasons discussed in 43.6.2. This is a 16-bit read-write value. The meaning of particular Key values is of local significance.;

30.7.1.1.8 aAggActorOperKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current operational value of the Key for the Aggregator. The administrative Key value may differ from the operational Key value for the reasons discussed in 43.6.2. This is a 16-bit read-only value. The meaning of particular Key values is of local significance.;

30.7.1.1.9 aAggMACAddress

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
A 6-octet read-only value carrying the individual MAC address assigned to the Aggregator.;

30.7.1.1.10 aAggPartnerSystemID

ATTRIBUTE

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APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
A 6-octet read-only MAC address value consisting of the unique identifier for the current protocol Partner of this Aggregator. A value of zero indicates that there is no known Partner. If the aggregation is manually configured, this System ID value will be a value assigned by the local System.;

30.7.1.1.11 aAggPartnerSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A 2-octet read-only value that indicates the priority value associated with the Partner's System ID. If the aggregation is manually configured, this System Priority value will be a value assigned by the local System.;

30.7.1.1.12 aAggPartnerOperKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current operational value of the Key for the Aggregator's current protocol Partner. This is a 16-bit read-only value. If the aggregation is manually configured, this Key value will be a value assigned by the local System.;

30.7.1.1.13 aAggAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
up
down

BEHAVIOUR DEFINED AS:
This read-write value defines the administrative state of the Aggregator. A value of "up" indicates that the operational state of the Aggregator (aAggOperState) is permitted to be either up or down. A value of "down" forces the operational state of the Aggregator to be down. Changes to the administrative state affect the operational state of the Aggregator only, not the operational state of the Aggregation Ports that are attached to the Aggregator. A GET operation returns the current administrative state. A SET operation changes the administrative state to a new value.;

30.7.1.1.14 aAggOperState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
up
down

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BEHAVIOUR DEFINED AS:

This read-only value defines the operational state of the Aggregator. The operational state is “up” if one or more of the Aggregation Ports that are attached to the Aggregator are collecting, or both collecting and distributing, and if the value of aAggAdminState for the Aggregator is also “up”. If none of the Aggregation Ports that are attached to the Aggregator are collecting and/or distributing, or if there are no Aggregation Ports attached to this Aggregator, then the operational state is “down”. An operational state of “up” indicates that the Aggregator is available for use by the MAC Client; a value of “down” indicates that the Aggregator is not available for use by the MAC Client.;

30.7.1.1.15 aAggTimeOfLastOperChange

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aTimeSinceSystemReset (Annex F.2.1) at the time the interface entered its current operational state. If the current state was entered prior to the last re-initialization of the local network management subsystem, then this object contains a value of zero. This value is read-only.;

30.7.1.1.16 aAggDataRate

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current data rate, in bits per second, of the aggregate link. The value is calculated as N times the data rate of a single link in the aggregation, where N is the number of active links. This attribute is read-only.;

30.7.1.1.17 aAggOctetsTxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data and padding octets transmitted by this Aggregator on all Aggregation Ports that are (or have been) members of the aggregation. The count does not include octets transmitted by the Aggregator in frames that carry LACPDUs or Marker PDUs (30.7.3.1.7, 30.7.3.1.8, 30.7.3.1.9). However, it includes frames discarded by the Distribution function of the Aggregator (30.7.1.1.25). This value is read-only.;

30.7.1.1.18 aAggOctetsRxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data and padding octets received by this Aggregator, from the Aggregation Ports

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that are (or have been) members of the aggregation. The count does not include octets received in frames that carry LACP or Marker PDUs (30.7.3.1.2, 30.7.3.1.3, 30.7.3.1.4), or frames discarded by the Collection function of the Aggregator (30.7.1.1.26). This value is read-only.;

30.7.1.1.19 aAggFramesTxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data frames transmitted by this Aggregator on all Aggregation Ports that are (or have been) members of the aggregation. The count does not include frames transmitted by the Aggregator that carry LACP or Marker PDUs (30.7.3.1.7, 30.7.3.1.8, 30.7.3.1.9). However, it includes frames discarded by the Distribution function of the Aggregator (30.7.1.1.25). This value is read-only.;

30.7.1.1.20 aAggFramesRxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data frames received by this Aggregator, from the Aggregation Ports that are (or have been) members of the aggregation. The count does not include frames that carry LACP or Marker PDUs (30.7.3.1.2, 30.7.3.1.3, 30.7.3.1.4), or frames discarded by the Collection function of the Aggregator (30.7.1.1.26). This value is read-only.;

30.7.1.1.21 aAggMulticastFramesTxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data frames transmitted by this Aggregator on all Aggregation Ports that are (or have been) members of the aggregation, to a group destination address other than the broadcast address. The count does not include frames transmitted by the Aggregator that carry LACP or Marker PDUs (30.7.3.1.7, 30.7.3.1.8, 30.7.3.1.9). However, it includes frames discarded by the Distribution function of the Aggregator (30.7.1.1.25). This value is read-only.;

30.7.1.1.22 aAggMulticastFramesRxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data frames received by this Aggregator, from the Aggregation Ports that are (or

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have been) members of the aggregation, that were addressed to an active group address other than the broadcast address. The count does not include frames that carry LACP or Marker PDUs (30.7.3.1.2, 30.7.3.1.3, 30.7.3.1.4), or frames discarded by the Collection function of the Aggregator (30.7.1.1.26). This value is read-only.;

30.7.1.1.23 aAggBroadcastFramesTxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the broadcast data frames transmitted by this Aggregator on all Aggregation Ports that are (or have been) members of the aggregation. The count does not include frames transmitted by the Aggregator that carry LACP or Marker PDUs (30.7.3.1.7, 30.7.3.1.8, 30.7.3.1.9). However, it includes frames discarded by the Distribution function of the Aggregator (30.7.1.1.25). This value is read-only.;

30.7.1.1.24 aAggBroadcastFramesRxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the broadcast data frames received by this Aggregator, from the Aggregation Ports that are (or have been) members of the aggregation. The count does not include frames that carry LACP or Marker PDUs (30.7.3.1.2, 30.7.3.1.3, 30.7.3.1.4), illegal or unknown protocol frames (30.7.3.1.5, 30.7.3.1.6), or frames discarded by the Collection function of the Aggregator (30.7.1.1.26). This value is read-only.;

30.7.1.1.25 aAggFramesDiscardedOnTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames requested to be transmitted by this Aggregator that were discarded by the Distribution function of the Aggregator when conversations are re-allocated to different ports, due to the requirement to ensure that the conversations are flushed on the old ports in order to maintain proper frame ordering (43A.3), or discarded as a result of excessive collisions by ports that are (or have been) members of the aggregation. This value is read-only.;

30.7.1.1.26 aAggFramesDiscardedOnRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

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BEHAVIOUR DEFINED AS:

A count of data frames, received on all ports that are (or have been) members of the aggregation, that were discarded by the Collection function of the Aggregator as they were received on ports whose Collection function was disabled. This value is read-only.;

30.7.1.1.27 aAggFramesWithTxErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames requested to be transmitted by this Aggregator that experienced transmission errors on ports that are (or have been) members of the aggregation. This count does not include frames discarded due to excess collisions. This value is read-only.;

30.7.1.1.28 aAggFramesWithRxErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames discarded on reception by all ports that are (or have been) members of the aggregation, or that were discarded by the Collection function of the Aggregator, or that were discarded by the Aggregator due to the detection of an illegal Slow Protocols PDU (30.7.3.1.6). This value is read-only.;

30.7.1.1.29 aAggUnknownProtocolFrames

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames discarded on reception by all ports that are (or have been) members of the aggregation, due to the detection of an unknown Slow Protocols PDU (30.7.3.1.5). This value is read-only.;

30.7.1.1.30 aAggPortList

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE OF INTEGERs that match the syntax of aAggPortID.

BEHAVIOUR DEFINED AS:

The value of this read-only attribute contains the list of Aggregation Ports that are currently attached to the Aggregator. An empty list indicates that there are no Aggregation Ports attached. Each integer value in the list carries an aAggPortID attribute value (30.7.2.1.1).;

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30.7.1.1.31 aAggLinkUpDownNotificationEnable

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:
When set to “enabled”, Link Up and Link Down notifications are enabled for this Aggregator. When set to “disabled”, Link Up and Link Down notifications are disabled for this Aggregator. This value is read-write.;

30.7.1.1.32 aAggCollectorMaxDelay

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of this 16-bit read-write attribute defines the maximum delay, in tens of microseconds, that may be imposed by the Frame Collector between receiving a frame from an Aggregator Parser, and either delivering the frame to its MAC Client or discarding the frame (see 43.2.3.1.1).;

30.7.1.2 Aggregator Notifications

30.7.1.2.1 nAggLinkUpNotification

NOTIFICATION

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
When aAggLinkUpDownNotificationEnable is set to “enabled”, a Link Up notification is generated when the Operational State of the aggregator changes from “down” to “up”. When aAggLinkUpDownNotificationEnable is set to “disabled”, no Link Up notifications are generated. The notification carries the identifier of the Aggregator whose state has changed.;

30.7.1.2.2 nAggLinkDownNotification

NOTIFICATION

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
When aAggLinkUpDownNotificationEnable is set to “enabled”, a Link Down notification is generated when the Operational State of the aggregator changes from “up” to “down”. When aAggLinkUpDownNotificationEnable is set to “disabled”, no Link Down notifications are generated. The notification carries the identifier of the Aggregator whose state has changed.;

30.7.2 Aggregation Port managed object class

This subclause formally defines the behaviours for the oAggregationPort managed object class attributes.

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30.7.2.1 Aggregation Port Attributes

30.7.2.1.1 aAggPortID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The unique identifier allocated to this Aggregation Port by the local System. This attribute identifies an Aggregation Port instance among the subordinate managed objects of the containing object. This value is read-only.

30.7.2.1.2 aAggPortActorSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A 2-octet read-write value used to define the priority value associated with the Actor's System ID.;

30.7.2.1.3 aAggPortActorSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
A 6-octet read-only MAC address value that defines the value of the System ID for the System that contains this Aggregation Port.;

30.7.2.1.4 aAggPortActorAdminKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current administrative value of the Key for the Aggregation Port. This is a 16-bit read-write value. The meaning of particular Key values is of local significance.;

30.7.2.1.5 aAggPortActorOperKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current operational value of the Key for the Aggregation Port. This is a 16-bit read-only value. The meaning of particular Key values is of local significance.;

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30.7.2.1.6 aAggPortPartnerAdminSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A 2-octet read-write value used to define the administrative value of priority associated with the Partner's System ID. The assigned value is used, along with the value of aAggPortPartnerAdminSystemID, aAggPortPartnerAdminKey, aAggPortPartnerAdminPort, and aAggPortPartnerAdminPortPriority, in order to achieve manually configured aggregation.;

30.7.2.1.7 aAggPortPartnerOperSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A 2-octet read-only value indicating the operational value of priority associated with the Partner's System ID. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminSystemPriority if there is no protocol Partner.;

30.7.2.1.8 aAggPortPartnerAdminSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
A 6-octet read-write MACAddress value representing the administrative value of the Aggregation Port's protocol Partner's System ID. The assigned value is used, along with the value of aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminKey, aAggPortPartnerAdminPort, and aAggPortPartnerAdminPortPriority, in order to achieve manually configured aggregation.;

30.7.2.1.9 aAggPortPartnerOperSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
A 6-octet read-only MACAddress value representing the current value of the Aggregation Port's protocol Partner's System ID. A value of zero indicates that there is no known protocol Partner. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminSystemID if there is no protocol Partner.;

30.7.2.1.10 aAggPortPartnerAdminKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

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BEHAVIOUR DEFINED AS:

The current administrative value of the Key for the protocol Partner. This is a 16-bit read-write value. The assigned value is used, along with the value of aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminSystemID, aAggPortPartnerAdminPort, and aAggPortPartnerAdminPortPriority, in order to achieve manually configured aggregation.;

30.7.2.1.11 aAggPortPartnerOperKey

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current operational value of the Key for the protocol Partner. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminKey if there is no protocol Partner. This is a 16-bit read-only value.;

30.7.2.1.12 aAggPortSelectedAggID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The identifier value of the Aggregator that this Aggregation Port has currently selected. Zero indicates that the Aggregation Port has not selected an Aggregator, either because it is in the process of detaching from an Aggregator or because there is no suitable Aggregator available for it to select. This value is read-only.;

30.7.2.1.13 aAggPortAttachedAggID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The identifier value of the Aggregator that this Aggregation Port is currently attached to. Zero indicates that the Aggregation Port is not currently attached to an Aggregator. This value is read-only.;

30.7.2.1.14 aAggPortActorPort

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The port number locally assigned to the Aggregation Port. The port number is communicated in LACPDUs as the Actor_Port. This value is read-only.;

30.7.2.1.15 aAggPortActorPortPriority

ATTRIBUTE

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APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The priority value assigned to this Aggregation Port. This 16-bit value is read-write.;

30.7.2.1.16 aAggPortPartnerAdminPort

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current administrative value of the port number for the protocol Partner. This is a 16-bit read-write value. The assigned value is used, along with the value of aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminSystemID, aAggPortPartnerAdminKey, and aAggPortPartnerAdminPortPriority, in order to achieve manually configured aggregation.;

30.7.2.1.17 aAggPortPartnerOperPort

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The operational port number assigned to this Aggregation Port by the Aggregation Port's protocol Partner. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminPort if there is no protocol Partner. This 16-bit value is read-only.;

30.7.2.1.18 aAggPortPartnerAdminPortPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current administrative value of the port priority for the protocol Partner. This is a 16-bit read-write value. The assigned value is used, along with the value of aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminSystemID, aAggPortPartnerAdminKey, and aAggPortPartnerAdminPort, in order to achieve manually configured aggregation.;

30.7.2.1.19 aAggPortPartnerOperPortPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The priority value assigned to this Aggregation Port by the Partner. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminPortPriority if there is no protocol Partner. This 16-bit value is read-only.;

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30.7.2.1.20 aAggPortActorAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1..8)]

BEHAVIOUR DEFINED AS:
A string of 8 bits, corresponding to the administrative values of Actor_State (43.4.2) as transmitted by the Actor in LACPDUs. The first bit corresponds to bit 0 of Actor_State (LACP_Activity), the second bit corresponds to bit 1 (LACP_Timeout), the third bit corresponds to bit 2 (Aggregation), the fourth bit corresponds to bit 3 (Synchronization), the fifth bit corresponds to bit 4 (Collecting), the sixth bit corresponds to bit 5 (Distributing), the seventh bit corresponds to bit 6 (Defaulted), and the eighth bit corresponds to bit 7 (Expired). These values allow administrative control over the values of LACP_Activity, LACP_Timeout, and Aggregation. This attribute value is read-write.;

30.7.2.1.21 aAggPortActorOperState

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1..8)]

BEHAVIOUR DEFINED AS:
A string of 8 bits, corresponding to the current operational values of Actor_State (43.4.2) as transmitted by the Actor in LACPDUs. The bit allocations are as defined in 30.7.2.1.20. This attribute value is read-only.;

30.7.2.1.22 aAggPortPartnerAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1..8)]

BEHAVIOUR DEFINED AS:
A string of 8 bits, corresponding to the current administrative value of Actor_State for the protocol Partner. The bit allocations are as defined in 30.7.2.1.20. This attribute value is read-write. The assigned value is used in order to achieve manually configured aggregation.;

30.7.2.1.23 aAggPortPartnerOperState

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1..8)]

BEHAVIOUR DEFINED AS:
A string of 8 bits, corresponding to the current values of Actor_State in the most recently received LACPDU transmitted by the protocol Partner. The bit allocations are as defined in 30.7.2.1.20. In the absence of an active protocol Partner, this value may reflect the manually configured value aAggPortPartnerAdminState. This attribute value is read-only.;

30.7.2.1.24 aAggPortAggregateOrIndividual

ATTRIBUTE

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APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value indicating whether the Aggregation Port is able to Aggregate ("TRUE") or is only able to operate as an Individual link ("FALSE").;

30.7.3 Aggregation Port Statistics managed object class

This subclause formally defines the behaviours for the oAggPortStats managed object class attributes.

30.7.3.1 Aggregation Port Statistics attributes

30.7.3.1.1 aAggPortStatsID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
This read-only attribute identifies an Aggregation Port Statistics object instance among the subordinate managed objects of the containing object. The value allocated to this attribute shall be the same as the containing oAggregationPort managed object.;

30.7.3.1.2 aAggPortStatsLACPDUsRx

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:
The number of valid LACPDUs received on this Aggregation Port. This value is read-only.;

30.7.3.1.3 aAggPortStatsMarkerPDUsRx

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:
The number of valid Marker PDUs received on this Aggregation Port. This value is read-only.;

30.7.3.1.4 aAggPortStatsMarkerResponsePDUsRx

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:
The number of valid Marker Response PDUs received on this Aggregation Port. This value is read-only.;

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30.7.3.1.5 aAggPortStatsUnknownRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 50 counts per second.

BEHAVIOUR DEFINED AS:

The number of frames received that either

— Carry the Slow Protocols Ethernet Type value (43B.4), but contain an unknown PDU, or

— Are addressed to the Slow Protocols group MAC Address (43B.3), but do not carry the Slow Protocols Ethernet Type. This value is read-only.;

30.7.3.1.6 aAggPortStatsIllegalRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 50 counts per second.

BEHAVIOUR DEFINED AS:

The number of frames received that carry the Slow Protocols Ethernet Type value (43B.4), but contain a badly formed PDU or an illegal value of Protocol Subtype (43B.3). This value is read-only.;

30.7.3.1.7 aAggPortStatsLACPDUsTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

The number of LACPDUs transmitted on this Aggregation Port. This value is read-only.;

30.7.3.1.8 aAggPortStatsMarkerPDUsTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

The number of Marker PDUs transmitted on this Aggregation Port. This value is read-only.;

30.7.3.1.9 aAggPortStatsMarkerResponsePDUsTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

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BEHAVIOUR DEFINED AS:

The number of Marker Response PDUs transmitted on this Aggregation Port. This value is read-only.;

30.7.4 Aggregation Port Debug Information managed object class

This subclause formally defines the behaviours for the oAggPortDebugInformation managed object class attributes.

30.7.4.1 Aggregation Port Debug Information attributes

30.7.4.1.1 aAggPortDebugInformationID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

This read-only attribute identifies an LACP Debug Information object instance among the subordinate managed objects of the containing object. The value allocated to this attribute shall be the same as the containing oAggregationPort managed object.;

30.7.4.1.2 aAggPortDebugRxState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
current
expired
defaulted
initialize
lacpDisabled
portDisabled

BEHAVIOUR DEFINED AS:

This attribute holds the value “current” if the Receive state machine for the Aggregation Port is in the CURRENT state, “expired” if the Receive state machine is in the EXPIRED state, “defaulted” if the Receive state machine is in the DEFAULTED state, “initialize” if the Receive state machine is in the INITIALIZE state, “lacpDisabled” if the Receive state machine is in the LACP_DISABLED state, or “portDisabled” if the Receive state machine is in the PORT_DISABLED state. This value is read-only.;

30.7.4.1.3 aAggPortDebugLastRxTime

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aTimeSinceSystemReset (F.2.1) when the last LACPDU was received by this Aggregation Port. This value is read-only.;

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30.7.4.1.4 aAggPortDebugMuxState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
detached
waiting
attached
collecting
distributing
collecting_distributing

BEHAVIOUR DEFINED AS:

This attribute holds the value “detached” if the Mux state machine (43.4.15) for the Aggregation Port is in the DETACHED state, “waiting” if the Mux state machine for the Aggregation Port is in the WAITING state, “attached” if the Mux state machine for the Aggregation Port is in the ATTACHED state, “collecting” if the Mux state machine for the Aggregation Port is in the COLLECTING state, “distributing” if the Mux state machine for the Aggregation Port is in the DISTRIBUTING state, and “collecting_distributing” if the Mux state machine for the Aggregation Port is in the COLLECTING_DISTRIBUTING state. This value is read-only.;

30.7.4.1.5 aAggPortDebugMuxReason

ATTRIBUTE

APPROPRIATE SYNTAX:

A PrintableString, 255 characters max.

BEHAVIOUR DEFINED AS:

A human-readable text string indicating the reason for the most recent change of Mux machine state. This value is read-only.;

30.7.4.1.6 aAggPortDebugActorChurnState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
noChurn
churn

BEHAVIOUR DEFINED AS:

The state of the Actor Churn Detection machine (43.4.17) for the Aggregation Port. A value of “noChurn” indicates that the state machine is in either the NO_ACTOR_CHURN or the ACTOR_CHURN_MONITOR state, and “churn” indicates that the state machine is in the ACTOR_CHURN state. This value is read-only.;

30.7.4.1.7 aAggPortDebugPartnerChurnState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
noChurn
churn

BEHAVIOUR DEFINED AS:

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The state of the Partner Churn Detection machine (43.4.17) for the Aggregation Port. A value of "noChurn" indicates that the state machine is in either the NO_PARTNER_CHURN or the PARTNER_CHURN_MONITOR state, and "churn" indicates that the state machine is in the PARTNER_CHURN state. This value is read-only.;

30.7.4.1.8 aAggPortDebugActorChurnCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Actor Churn state machine has entered the ACTOR_CHURN state. This value is read-only.;

30.7.4.1.9 aAggPortDebugPartnerChurnCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Partner Churn state machine has entered the PARTNER_CHURN state. This value is read-only.;

30.7.4.1.10 aAggPortDebugActorSyncTransitionCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Actor's Mux state machine (43.4.15) has entered the IN_SYNC state. This value is read-only.;

30.7.4.1.11 aAggPortDebugPartnerSyncTransitionCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Partner's Mux state machine (43.4.15) has entered the IN_SYNC state. This value is read-only.;

30.7.4.1.12 aAggPortDebugActorChangeCount

ATTRIBUTE

APPROPRIATE SYNTAX:

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Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Actor's perception of the LAG ID for this Aggregation Port has changed. This value is read-only.;

30.7.4.1.13 aAggPortDebugPartnerChangeCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Partner's perception of the LAG ID (43.3.6.1) for this Aggregation Port has changed. This value is read-only.;

30.8 Management for WAN Interface Sublayer (WIS)

30.8.1 WIS managed object class

This subclause formally defines the behaviours for the oWIS managed object class and attributes.

30.8.1.1 WIS attributes

The attributes in 30.8.1.1.1 through 30.8.1.1.28 may be used, possibly in conjunction with other attributes, to derive various system performance monitoring parameters and information.

30.8.1.1.1 aWISID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aWISID is assigned so as to uniquely identify a WIS among the subordinate managed objects of the containing object.;

30.8.1.1.2 aSectionStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A string of 2 bits corresponding to the Section Status (50.3.2.5). The first bit corresponds to the Loss of Signal flag and maps to the LOS bit in the WIS Status 3 register. The second bit corresponds to the Loss of Frame flag and maps to the LOF bit in the WIS Status 3 register. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS Status 3 register specified in 45.2.2.10.;

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30.8.1.1.3 aSectionSESThreshold

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET operation returns the value for *x* for Section SES definition (30.8.1.1.4). A SET operation changes the value for *x* for Section SES definition. After reset (or power-off, power-on cycle), *x* for Section SES returns to the default value 8554.

NOTE—8554 is selected to reflect the number of Section BIP-8 Errors that would occur with a random bit error ratio of 1×10^{-6} (see Annex 50A).;

30.8.1.1.4 aSectionSESs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:
Increment counter by one in a "Severely Errored Second" (SES), i.e., a second that had *x* or more Section BIP-8 Errors (50.3.2.5) or one or more Section Defects, i.e., the LOS flag (50.3.2.5) was equal to 1 or the LOF flag (50.3.2.5) was equal to 1, where *x* is the Section SES threshold defined by aSectionSESThreshold (30.8.1.1.3).;

30.8.1.1.5 aSectionESs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:
Increment counter by one in an "Errored Second" (ES), i.e., a second that had one or more Section BIP-8 Errors (50.3.2.5) or one or more Section Defects, i.e., the LOS flag (50.3.2.5) was equal to 1 or the LOF flag (50.3.2.5) was equal to 1.;

30.8.1.1.6 aSectionSEFSs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:
Increment counter by one in a "Severely Errored Framing Second" (SEFS), i.e., a second containing one or more SEF events (50.3.2.5).;

30.8.1.1.7 aSectionCVs

ATTRIBUTE

APPROPRIATE SYNTAX:

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Generalized nonresettable counter. This counter has a maximum increment rate of 64 000 counts per second.

BEHAVIOUR DEFINED AS:

For every received B1 octet, increment counter by the number of detected Section BIP-8 Errors (50.3.2.5).;

30.8.1.1.8 aJ0ValueTX

ATTRIBUTE

APPROPRIATE SYNTAX:

OCTET STRING, 15

BEHAVIOUR DEFINED AS:

An 16 octet value defining the transmitter's Section Trace message as defined in 50.3.2.3. The first octet of the string is transmitted first, and the last octet is transmitted last. A SET operation changes the Section Trace message value. A GET operation returns the current Section Trace message value. The default transmitter's Section Trace message is the hexadecimal value 89, followed by 15 NULL characters, the hexadecimal value 00. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS J0 transmit registers specified in 45.2.2.18.;

30.8.1.1.9 aJ0ValueRX

ATTRIBUTE

APPROPRIATE SYNTAX:

OCTET STRING, 15

BEHAVIOUR DEFINED AS:

An 16 octet value indicating the received Section Trace message as defined in 50.3.2.4. The first octet in this string was received first, and the last octet received last. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS J0 receive registers specified in 45.2.2.19.;

30.8.1.1.10 aLineStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A string of 2 bits reflecting the Line status (50.3.2.5). The first bit corresponds to the Line Alarm Indication Signal flag and maps to the AIS-L bit. The second bit corresponds to the Line Remote Defect Indication flag and maps to the RDI-L bit. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS Status 3 register specified in 45.2.2.10;

30.8.1.1.11 aLineSESThreshold

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET operation returns the value for *x* for Line SES definition (30.8.1.1.12). A SET operation changes the value for x for Line SES definition. After WIS reset (or power-off, power-on cycle),

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x for Line SES returns to the default value 9835.;

NOTE—9835 is selected to reflect the number of Line BIP Errors that would occur with a random bit error ratio of 1×10^{-6} (see Annex 50A).;

30.8.1.1.12 aLineSESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in a "Severely Errored Second" (SES), i.e., a second that had *x* or more Line BIP Errors (50.3.2.5) or an AIS-L defect was present, i.e., the AIS-L flag (50.3.2.5) was equal to 1, where *x* is the Line SES threshold defined by aLineSESThreshold (30.8.1.1.11).;

30.8.1.1.13 aLineESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in an "Errored Second" (ES), i.e., a second that had one or more Line BIP Errors (50.3.2.5) or an AIS-L defect was present, i.e., the AIS-L flag (50.3.2.5) was equal to 1.;

30.8.1.1.14 aLineCVs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 12 288 000 counts per second at 10 Gb/s.

BEHAVIOUR DEFINED AS:

For every received WIS frame (50.3.2), increment counter by the number of detected Line BIP Errors (50.3.2.5).;

30.8.1.1.15 aFarEndLineSESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in a "Severely Errored Second" (SES), i.e., a second that had *x* or more Far End Line BIP Errors (50.3.2.5) or an RDI-L defect was present, i.e., the RDI-L flag (50.3.2.5) was equal to 1, where *x* is the Line SES threshold defined by aLineSESThreshold (30.8.1.1.11).;

30.8.1.1.16 aFarEndLineESs

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in an “Errored Second” (ES), i.e., a second that had one or more Far End Line BIP Errors (50.3.2.5) or an RDI-L defect was present, i.e., the RDI-L flag (50.3.2.5) was equal to 1.;

30.8.1.1.17 aFarEndLineCVs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 040 000 counts per second at 10 Gb/s.

BEHAVIOUR DEFINED AS:

For every received WIS frame (50.3.2), increment counter by the number of reported Far End Line BIP Errors (50.3.2.5).;

30.8.1.1.18 aPathStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (4)]

BEHAVIOUR DEFINED AS:

A string of 4 bits corresponding to the Path Status (50.3.2.5). The first bit corresponds to the Loss of Pointer flag and maps to the LOP-P bit, the second bit corresponds to the Alarm Indication Signal and maps to the AIS-P bit, the third bit corresponds to the Path Label Mismatch flag and maps to the PLM-P bit and the fourth bit corresponds to the Path Loss of Cell Delineation flag and maps to the LCD-P bit. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS Status 3 register specified in 45.2.2.10;

30.8.1.1.19 aPathSESThreshold

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET operation returns the value for *x* for Path SES definition (30.8.1.1.20). A SET operation changes the value for *x* for Path SES definition. After reset (or power-off, power-on cycle), *x* for Path SES is set to the default value 2400.

NOTE—2400 is selected to reflect the point where 30% of all SPEs have a Path Block Error (see Annex 50A).;

30.8.1.1.20 aPathSESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

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BEHAVIOUR DEFINED AS:

Increment counter by one in a “Severely Errored Second” (SES), i.e., a second that had *x* or more Path Block Errors (Annex 50A) or one or more Path Defects, i.e., the LOP-P flag (50.3.2.5) was equal to 1, the AIS-P flag (50.3.2.5) was equal to 1, the PLM-P flag (50.3.2.5) was equal to 1, or the LCD-P flag (50.3.2.5) was equal to 1, where *x* is the Path SES threshold defined by aPathSESThreshold (30.8.1.1.19).;

30.8.1.1.21 aPathESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in an Errored Second (ES), i.e., a second that had one or more Path Block Errors (Annex 50A) or one or more Path Defects, i.e., the LOP-P flag (50.3.2.5) was equal to 1, the AIS-P flag (50.3.2.5) was equal to 1, the PLM-P flag (50.3.2.5) was equal to 1, or the LCD-P flag (50.3.2.5) was equal to 1.;

30.8.1.1.22 aPathCVs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 8000 counts per second.

BEHAVIOUR DEFINED AS:

Increment counter by one for every received B3 indicating a Path Block Error (Annex 50A).;

30.8.1.1.23 aJ1ValueTX

ATTRIBUTE

APPROPRIATE SYNTAX:

OCTET STRING, 15

BEHAVIOUR DEFINED AS:

An 16 octet value defining the transmitter’s Path Trace message as defined in 50.3.2.1. The first octet of the string is transmitted first, and the last octet is transmitted last. A SET operation changes the Path Trace message value. A GET operation returns the current Path Trace message value. The default transmitter’s Path Trace message is the hexadecimal value 89, followed by 15 NULL characters, the hexadecimal value 00. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS J1 transmit registers specified in 45.2.2.12.;

30.8.1.1.24 aJ1ValueRX

ATTRIBUTE

APPROPRIATE SYNTAX:

OCTET STRING, 15

BEHAVIOUR DEFINED AS:

An 16 octet value indicating the received Path Trace message as defined in 50.3.2.4. The first octet in this string was received first, and the last octet received last. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS J1 receive registers specified in

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45.2.2.13.;

30.8.1.1.25 aFarEndPathStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A string of 2 bits corresponding to the Far End Path Status (50.3.2.5). The first bit corresponds to the Far End Path Label Mismatch/Path Loss of Cell Delineation flag and maps to the Far End PLM-P/LCD-P bit, and the second bit corresponds to the Far End Path Alarm Indication Signal/Path Loss of Pointer flag and maps to the Far End AIS-P/LOP-P bit. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS Status 3 register specified in 45.2.2.10;

30.8.1.1.26 aFarEndPathSESs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:
Increment counter by one in a “Severely Errored Second” (SES), i.e., a second that had *x* or more Far End Path Block Errors or one or more Far End Path Defects reported in the Far End PLM-P/LCD-P, AIS-P, and LOP-P bits (50.3.2.5), where *x* is the Path SES threshold defined by aPathSESThreshold (30.8.1.1.19).;

30.8.1.1.27 aFarEndPathESs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:
Increment counter by one in an “Errored Second” (ES), i.e., a second that had one or more Far End Path Block Errors or one or more Far End Path Defects reported in the Far End PLM-P/LCD-P, AIS-P, and LOP-P bits (50.3.2.5).;

30.8.1.1.28 aFarEndPathCVs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 8000 counts per second.

BEHAVIOUR DEFINED AS:
Increment counter by one for each received G1 octet indicating a Far End Path Block Error reported in REI-P (50.3.2.5).;

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30.9 Management for Power over Ethernet

30.9.1 PSE managed object class

This subclause formally defines the behaviours for the oPSE managed object class attributes and actions.

30.9.1.1 PSE attributes

30.9.1.1.1 aPSEID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aPSEID is assigned so as to uniquely identify a PSE among the subordinate managed objects of the containing object.;

30.9.1.1.2 aPSEAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

enabled	PSE functions enabled
disabled	PSE functions disabled

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational state of the PSE functions. An interface which can provide the PSE functions specified in Clause 33 will be enabled to do so when this attribute has the enumeration “enabled”. When this attribute has the enumeration “disabled” the interface will act as it would if it had no PSE function. The operational state of the PSE function can be changed using the acPSEAdminControl action. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the PSE Enable bit specified in 33.5.1.1.5.;

30.9.1.1.3 aPSEPowerPairsControlAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
Indicates the ability to control which PSE Pinout Alternative (see 33.2.3 and 145.2.4) is used for PD detection and power. When “true” the PSE Pinout Alternative used can be controlled through the aPSEPowerPairs attribute. When “false”, the PSE Pinout Alternative used cannot be controlled through the aPSEPowerPairs attribute. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the Pair Control Ability bit specified in 33.5.1.2.12.;

30.9.1.1.4 aPSEPowerPairs

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

signal	PSE Pinout Alternative A

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spare	PSE Pinout Alternative B
both	PSE Pinout Alternative A and Alternative B

BEHAVIOUR DEFINED AS:

A read-write value that identifies the supported PSE Pinout Alternative specified in 33.2.3 and 145.2.4. A GET operation returns the PSE Pinout Alternative in use. If the attribute aPSEPowerPairsControlAbility is “true”, a SET operation will cause the PSE functions to be disabled, the PSE Pinout Alternative used to be changed to the value indicated if supported, and then the PSE functions to be enabled. If the attribute aPSEPowerPairsControlAbility is “false”, a SET operation has no effect.

The enumeration “signal” indicates that PSE Pinout Alternative A is used for PD detection and power. The enumeration “spare” indicates that PSE Pinout Alternative B is used for PD detection and power. The enumeration “both” indicates that the PSE Pinout uses both Alternative A and Alternative B for detection and power. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the Pair Control bits specified in 33.5.1.1.4.;

30.9.1.1.5 aPSEPowerDetectionStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

disabled	PSE disabled
searching	PSE searching
deliveringPower	PSE delivering power
test	PSE test mode
fault	PSE fault detected
otherFault	PSE implementation specific fault detected

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 33.2.5 and 145.2.6.

The enumeration “disabled” indicates that the PSE State diagram (Figure 33–9) is in the state DISABLED. The enumeration “deliveringPower” indicates that the PSE State diagram is in the state POWER_ON. The enumeration “test” indicates that the PSE State diagram is in the state TEST_MODE. The enumeration “fault” indicates that the PSE State diagram is in the state TEST_ERROR. The enumeration “otherFault” indicates that the PSE State diagram is in the state IDLE due to the variable error_condition = TRUE. The enumeration “searching” indicates the PSE State diagram is in a state other than those listed above. Type 3 and Type 4 PSEs do not use the values “test” or “fault”. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the PSE Status bits specified in 33.5.1.2.11.

NOTE—A derivative attribute may wish to apply a delay to the use of the “deliveringPower” enumeration as the PSE state diagram will enter and then quickly exit the POWER_ON state if a short-circuit or overcurrent condition is present when power is first applied.;

30.9.1.1.6 aPSEPowerDetectionStatusA

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

searchingAltA	PSE searching

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deliveringPowerAltA	PSE delivering power
faultAltA	PSE fault detected

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 145.2.6.

The enumeration “deliveringPowerAltA” indicates that the PSE State diagram is in the state POWER_ON_PRI if alt_pri=‘a’ or the state POWER_ON_SEC if alt_pri=‘b’. The enumeration “faultAltA” indicates that the PSE State diagram is in the state IDLE_PRI if alt_pri=‘a’ or the state IDLE_SEC if alt_pri=‘b’ due to the variable error_condition_pri = TRUE (if alt_pri=‘a’) or error_condition_sec = TRUE (if alt_pri=‘b’). The enumeration “searchingAltA” indicates the PSE State diagram is in a state other than those listed above.

NOTE—A derivative attribute may wish to apply a delay to the use of the “deliveringPowerAltA” enumeration as the PSE state diagram will enter and then quickly exit the POWER_ON_PRI (if alt_pri=‘a’) state or the POWER_ON_SEC (if alt_pri=‘b’) state if a short-circuit or overcurrent condition is present when power is first applied.;

30.9.1.1.7 aPSEPowerDetectionStatusB

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

searchingAltB	PSE searching
deliveringPowerAltB	PSE delivering power
faultAltB	PSE fault detected

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 145.2.6.

The enumeration “deliveringPowerAltB” indicates that the PSE State diagram is in the state POWER_ON_SEC if alt_pri=‘a’ or the state POWER_ON_PRI if alt_pri=‘b’. The enumeration “faultAltB” indicates that the PSE State diagram is in the state IDLE_SEC if alt_pri=‘a’ or the state IDLE_PRI if alt_pri=‘b’ due to the variable error_condition_sec = TRUE (if alt_pri=‘a’) or error_condition_pri = TRUE (if alt_pri=‘b’). The enumeration “searchingAltB” indicates the PSE State diagram is in a state other than those listed above.

NOTE—A derivative attribute may wish to apply a delay to the use of the “deliveringPowerAltB” enumeration as the PSE state diagram will enter and then quickly exit the POWER_ON_SEC (if alt_pri=‘a’) state or the POWER_ON_PRI (if alt_pri=‘b’) state if a short-circuit or overcurrent condition is present when power is first applied.;

30.9.1.1.8 aPSEPowerClassification

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

class0	Class 0 PD
class1	Class 1 PD
class2	Class 2 PD
class3	Class 3 PD
class4	Class 4 PD
class5	Class 5 PD

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class6	Class 6 PD
class7	Class 7 PD
class8	Class 8 PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the PD Class of a detected PD as specified in 33.2.6.1 and 145.2.8.1.

This value is only valid while a PD is being powered, that is the attribute aPSEPowerDetectionStatus reporting the enumeration “deliveringPower”. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the PD Class bits specified in 33.5.1.2.10.;

30.9.1.1.9 aPSEPowerClassificationA

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

class1	Class 1 PD
class2	Class 2 PD
class3	Class 3 PD
class4	Class 4 PD
class5	Class 5 PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the PD Class of a detected dual-signature PD as specified in 145.2.8.1.

This value is only valid while a PD is being powered, that is the attribute aPSEPowerDetectionStatusA reporting the enumeration “deliveringPowerAltA”.;

30.9.1.1.10 aPSEPowerClassificationB

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

class1	Class 1 PD
class2	Class 2 PD
class3	Class 3 PD
class4	Class 4 PD
class5	Class 5 PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the PD Class of a detected dual-signature PD as specified in 145.2.8.1.

This value is only valid while a PD is being powered, that is the attribute aPSEPowerDetectionStatusB reporting the enumeration “deliveringPowerAltB”.;

30.9.1.1.11 aPSEInvalidSignatureCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per

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second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the Type 1 and Type 2 PSE state diagram (Figure 33–9) enters the state SIGNATURE_INVALID. This counter is not defined for Type 3 and Type 4 PSEs. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the Invalid Signature bit specified in 33.5.1.2.6.;

30.9.1.1.12 aPSEInvalidSignatureCounterA

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the do_detect_pri or do_detect_sec function in Figure 145–13, Figure 145–15, and Figure 145–16, whichever corresponds to Alternative A depending on the value of alt_pri, returns ‘invalid’.;

30.9.1.1.13 aPSEInvalidSignatureCounterB

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the do_detect_pri or do_detect_sec function in Figure 145–13, Figure 145–15, and Figure 145–16, whichever corresponds to Alternative B depending on the value of alt_pri, returns ‘invalid’.;

30.9.1.1.14 aPSEPowerDeniedCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–9 and Figure 145–13) enters the state POWER_DENIED. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the Power Denied bit specified in 33.5.1.2.4.;

30.9.1.1.15 aPSEPowerDeniedCounterA

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 145–15 or Figure 145–16) enters

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the state POWER_DENIED_PRI if alt_pri='a' or enters the state POWER_DENIED_SEC if alt_pri='b'.;

30.9.1.1.16 aPSEPowerDeniedCounterB

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 145–15 or Figure 145–16) enters the state POWER_DENIED_SEC if alt_pri='a' or enters the state POWER_DENIED_PRI if alt_pri='b'.;

30.9.1.1.17 aPSEOverLoadCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–9 and Figure 145–13) enters the state ERROR_DELAY due to the ovld_detected variable being TRUE. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the Overload bit specified in 33.5.1.2.8.;

30.9.1.1.18 aPSEOverLoadCounterA

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 145–15 or Figure 145–16) enters the state ERROR_DELAY_PRI if alt_pri='a' or enters the state ERROR_DELAY_SEC if alt_pri='b'.;

30.9.1.1.19 aPSEOverLoadCounterB

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 145–15 or Figure 145–16) enters the state ERROR_DELAY_SEC if alt_pri='a' or enters the state ERROR_DELAY_PRI if alt_pri='b'.;

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30.9.1.1.20 aPSEMPSAbsentCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–9 and Figure 145–13) transitions directly from the state POWER_ON to the state IDLE due to tmpdo_timer_done being asserted. For Type 1 or Type 2 PSEs, if a Clause 22 MII or Clause 35 GMII is present, then this will map to the MPS Absent bit specified in 33.5.1.2.9.;

30.9.1.1.21 aPSEMPSAbsentCounterA

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 145–15 or Figure 145–16) transitions directly from the state POWER_ON_PRI to the state IDLE_PRI due to mpdo_timer_pri_done being asserted if alt_pri='a' or transitions directly from the state POWER_ON_SEC to the state IDLE_SEC due to mpdo_timer_sec_done being asserted if alt_pri='b'.;

30.9.1.1.22 aPSEMPSAbsentCounterB

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 145–15 or Figure 145–16) transitions directly from the state POWER_ON_SEC to the state IDLE_SEC due to mpdo_timer_sec_done being asserted if alt_pri='a' or transitions directly from the state POWER_ON_PRI to the state IDLE_PRI due to mpdo_timer_pri_done being asserted if alt_pri='b'.;

30.9.1.1.23 aPSEActualPower

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

An integer value indicating present (actual) power being supplied by the PSE as measured at the MDI in milliwatts. The behaviour is undefined if the state of aPSEPowerDetectionStatus is anything other than deliveringPower. The sampling frequency and averaging is vendor-defined.;

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30.9.1.1.24 aPSEPowerAccuracy

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
An integer value indicating the accuracy associated with aPSEActualPower in +/- milliwatts.;

30.9.1.1.25 aPSECumulativeEnergy

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. The counter has a maximum increment rate of 100 000 per second.

BEHAVIOUR DEFINED AS:
A count of the cumulative energy supplied by the PSE as measured at the MDI in millijoules.;

30.9.1.2 PSE actions

30.9.1.2.1 acPSEAdminControl

ACTION

APPROPRIATE SYNTAX:
Same as aPSEAdminState

BEHAVIOUR DEFINED AS:
This action provides a means to alter aPSEAdminState.;

30.10 Layer management for Midspan

30.10.1 Midspan managed object class

This subclause formally defines the behaviours for the oMidSpan managed object class, attributes, and notifications.

30.10.1.1 Midspan attributes

30.10.1.1.1 aMidSpanID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aMidSpanID is assigned so as to uniquely identify a Midspan device among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2:1992 [SMI]).;

30.10.1.1.2 aMidSpanPSEGroupCapacity

ATTRIBUTE

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APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aMidSpanPSEGroupCapacity is the number of PSE groups that can be contained within the Midspan device. Within each managed Midspan device, the PSE groups are uniquely numbered in the range from 1 to aMidSpanPSEGroupCapacity.

Some PSE groups may not be present in a given Midspan instance, in which case the actual number of PSE groups present is less than aMidSpanPSEGroupCapacity. The number of PSE groups present is never greater than aMidSpanPSEGroupCapacity.;

30.10.1.1.3 aMidSpanPSEGroupMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
A string of bits which reflects the current configuration of PSE groups that are viewed by PSE group managed objects. The length of the bitstring is “aMidSpanPSEGroupCapacity” bits. The first bit relates to PSE group 1. A “1” in the bitstring indicates presence of the PSE group, “0” represents absence of the PSE group.;

30.10.1.2 Midspan notifications

30.10.1.2.1 nMidSpanPSEGroupMapChange

NOTIFICATION

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the PSE group structure of a Midspan device. This occurs only when a PSE group is logically removed from or added to a Midspan device. The nMidSpanPSEGroupMapChange notification is not sent when powering up a Midspan device. The value of the notification is the updated value of the aMidSpanPSEGroupMap attribute.;

30.10.2 PSE Group managed object class

This subclause formally defines the behaviours for the oPSEGroup managed object class, attributes, actions, and notifications.

30.10.2.1 PSE Group attributes

30.10.2.1.1 aPSEGroupID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A value unique within the Midspan device. The value of aPSEGroupID is assigned so as to uniquely identify a PSE group among the subordinate managed objects of the containing object (oMidSpan). This value is never greater than aMidSpanPSEGroupCapacity.;

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30.10.2.1.2 aPSECapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aPSECapacity is the number of PSEs contained within the PSE group. Valid range is 1–1024. Within each PSE group, the PSEs are uniquely numbered in the range from 1 to aPSECapacity. Some PSEs may not be present in a given PSE group instance, in which case the actual number of PSEs present is less than aPSECapacity. The number of PSEs present is never greater than aPSECapacity.;

30.10.2.1.3 aPSEMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BitString

BEHAVIOUR DEFINED AS:
A string of bits that reflects the current configuration of PSE managed objects within this PSE group. The length of the bitstring is “aPSECapacity” bits. The first bit relates to PSE 1. A “1” in the bitstring indicates presence of the PSE, “0” represents absence of the PSE.;

30.10.2.2 PSE Group notifications

30.10.2.2.1 nPSEMapChange

NOTIFICATION

APPROPRIATE SYNTAX:
BitString

BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the PSE structure of a PSE group. This occurs only when a PSE is logically removed from or added to a PSE group. The nPSEMapChange notification is not sent when powering up a Midspan device. The value of the notification is the updated value of the aPSEMap attribute.;

30.11 Layer Management for Physical Medium Entity (PME)

30.11.1 PAF managed object class

This subclause formally defines the behaviours for the oPAF managed object class attributes.

30.11.1.1 PAFAttributes

30.11.1.1.1 aPAFID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aTCID is assigned so as to uniquely identify a PAF among the subordinate managed

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objects of the containing object.

30.11.1.1.2 aPhyEnd

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value that has one of the following entries:

subscriber	subscriber mode of operation
office	office mode of operation

BEHAVIOUR DEFINED AS:

A read-only value that indicates the subtype of the PHY (see 61.1). The enumeration “subscriber” indicates the PHY is operating as a -R subtype, the enumeration “office” indicates the PHY is operating as a -O subtype.;

30.11.1.1.3 aPHYCurrentStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:

noPMEAssigned	no PME assigned in case of PME aggregation
lossOfFraming	one or more PME in aggregation indicates Loss of Framing
lossOfSignal	one or more PME in aggregation indicates Loss of Signal
lossOfPower	one or more PME in aggregation indicates Loss of Power
configInitFailure	configuration initialization failure
noPeerPMEPresent	one or more PME in aggregation indicates no peer PME present
snrMarginViolation	one or more PME in aggregation indicates SNR Margin Violation
lineAttenViolation	one or more PME in aggregation indicates Loop Attenuation Violation

BEHAVIOUR DEFINED AS:

This read-only value indicates the current operational state of the PHY (see 62.3.4.8 and 63.2.2.3).

The enumeration “noPMEAssigned” indicates that the PAF is enabled but that there are no PMEs available for aggregation (no modems assigned), the enumeration “lossOfFraming” indicates one or more PMEs in the aggregation are reporting loss of framing, the enumeration “lossOfSignal” indicates one or more PMEs in the aggregation are reporting loss of signal, the enumeration “lossOfPower” indicates one or more PMEs in the aggregation are reporting loss of power, the enumeration “configInitFailure” indicates configuration initialization failure, the enumeration “noPeerPMEPresent” indicates one or more PMEs in the aggregation are reporting that there was no handshake message/tones send by the remote end during initialization, the enumeration “snrMarginViolation” indicates one or more PMEs in the aggregation are reporting a SNR margin violation and the enumeration “lineAttenViolation” indicates one or more PMEs in the aggregation are reporting a loop attenuation violation.;

30.11.1.1.4 aPAFSupported

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the TPS-TC supports the PME aggregation function (see 61.2.2). A TPS-TC that can perform PME aggregation on the available PMEs shall return the enumeration “true”. A TPS-TC that is incapable of PME aggregation shall return the enumeration

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"false".

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the PAF available bit in the 10P/2B capability register (see 45.2.3.27.1).;

30.11.1.1.5 aPAFAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:
A read-write value that indicates the state of the PME aggregation function (see 61.2.2). When "disabled", PME aggregation will not be performed, when "enabled", PME aggregation will be performed when the link is Up, even on a single PME. As changing the state of the PME aggregation function is a traffic disruptive operation this can only occur when the link is down.

A GET operation returns the current state of the PME aggregation function. A SET operation changes the state of the PME aggregation function to the indicated value only if the attribute aPAFSupported is "true" and the link is down. If the attribute aPAFSupported is "false", or the link is not down, a SET operation has no effect.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the PAF enable bit in the 10P/2B capability register (see 45.2.3.28.3).;

30.11.1.1.6 aLocalPAFCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aLocalPAFCapacity is the number of PMEs that can be aggregated by the PME aggregation function (PAF) of the PHY. Valid range is 1–32. Within each PHY, the PMEs are uniquely numbered in the range from 1 to aLocalPAFCapacity. Some PMEs may not be present in a given PHY instance, in which case the actual number of PMEs present is less than aLocalPAFCapacity. The number of PMEs present is never greater than aLocalPAFCapacity.;

30.11.1.1.7 aLocalPMEAvailable

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (32)]

BEHAVIOUR DEFINED AS:
A string of bits that indicates which PMEs are currently available for aggregation by the PME aggregation function (PAF) of the PHY (see 61.1.5.3) and therefore reflects the current configuration of PME managed objects within this PAF. The length of the bitstring is "aLocalPAFCapacity" bits. The first bit relates to PME[0]. A "1" in the bitstring indicates the PME is present and is available to the PAF for aggregation. A "0" in the bitstring indicates the PME is absent and not available to the PAF for aggregation.

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If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the 10P/2B PME available register (see 45.2.3.29).;

30.11.1.1.8 aLocalPMEAggregate

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (32)]

BEHAVIOUR DEFINED AS:
A string of bits that indicates which PMEs are in an active aggregation in the PHY. The length of the bitstring is "aLocalPAFCapacity" bits. The first bit relates to PME[0]. A "1" in the bitstring indicates the PME is in an active aggregation. A "0" in the bitstring indicates the PME is not in an active aggregation.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the 10P/2B PME available registers (see 45.2.3.30).;

30.11.1.1.9 aRemotePAFSupported

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:

unknown	initializing, true state not yet know
supported	PAF supported
not supported	PAF not supported

BEHAVIOUR DEFINED AS:
A read-only value that indicates if the link-partner PHY supports the PME aggregation function (see 61.2.2). When the link-partner PHY can perform PME aggregation on its available PMEs the enumeration "supported" shall be returned. When the link-partner PHY is incapable of PME aggregation the enumeration "not supported" shall be returned.

If a Clause 45 MDIO Interface to the local PCS is present, then this attribute will map to the Remote PAF supported bit in the 10P/2B capability register (see 45.2.3.27.2).;

30.11.1.1.10 aRemotePAFCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aRemotePAFCapacity indicates the number of PME that can be aggregated by the PME aggregation function (PAF) of the link-partner PHY. Valid range is 1–32. Within the link-partner PHY, the PMEs are uniquely numbered in the range from 1 to aRemotePAFCapacity. Some PMEs may not be present in a given PHY instance, in which case the actual number of PMEs present is less than aRemotePAFCapacity. The number of PMEs present is never greater than aRemotePAFCapacity.;

30.11.1.1.11 aRemotePMEAggregate

ATTRIBUTE

APPROPRIATE SYNTAX:

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BIT STRING [SIZE (32)]

BEHAVIOUR DEFINED AS:

A string of bits that indicates which PMEs are in an active aggregation in the link-partner PHY. The length of the bitstring is “aRemotePAFCapacity” bits. The first bit relates to PME[0]. A “1” in the bitstring indicates the PME is in an active aggregation. A “0” in the bitstring indicates the PME is not in an active aggregation.

If a Clause 45 MDIO Interface to the local PCS is present, then this attribute will map to the 10P/2B PME available registers (see 45.2.6.10).;

30.11.2 PME managed object class

This subclause formally defines the behaviours for the oPME managed object class attributes.

30.11.2.1 PME Attributes

30.11.2.1.1 aPMEID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A value unique within the PAF. The value of aPMEID is assigned so as to uniquely identify a PME among the subordinate managed objects of the containing object (oPAF). This value is never greater than aLocalPAFCapacity.;

30.11.2.1.2 aPMEAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the state of the PME. The enumeration “disabled” indicates that the PME is disabled, the enumeration “enabled” indicates that the PME is enabled.
A GET operation returns the current state of the PME. A SET operation changes the state of the PME to the indicated value. The PME is enabled and link initialization initiated when the a SET operation is performed with the value “enabled” when the current value is “disabled”. A SET operation performed with the value “enabled” when the current value is already “enabled” will have shall have no effect.

If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute will map to the PMA/PMD link control register (see 45.2.1.11).;

30.11.2.1.3 aPMEStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

A ENUMERATED VALUE that has the following entries:
down not ready link is down, not ready

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down ready	link is down, ready
initializing	link is initializing
10PASS-TS	link is up as 10PASS-TS
2BASE-TL	link is up as 2BASE-TL

BEHAVIOUR DEFINED AS:

A read-only value that indicates the PME status. The enumeration “not ready” indicates that the link is down and handshake tones are not being received from a link partner, the enumeration “ready” indicates that the link is down and that handshake tones are being received from a link partner, the enumeration “initializing” indicates that the link is initializing, the enumeration “10PASS-TS” indicates that the link is up and the remote PHY is a 10PASS-TS PHY and the enumeration “2BASE-TL” indicates that the link is up and the remote PHY is a 2BASE-TL PHY.

If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute will map to the PMA/PMD link status register (see 45.2.1.29.4).;

30.11.2.1.4 aPMESNRMgn

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A read-only value that indicates the PME current signal-to-noise ratio (SNR) Margin (see 62.3.4.7 and 63.2.2.3) with respect to the received signal in increments of dB rounded down to the nearest dB.

If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute will map to the 10P/2B RX SNR margin register (see 45.2.1.35).;

30.11.2.1.5 aTCCodingViolations

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 19 230 counts per second for 10 Mb/s implementations.

BEHAVIOUR DEFINED AS:

A count of 64/65-octet encapsulation error. Increment the counter by one for each 64/65-octet encapsulation error detected by the 64/65-octet receive function (see Figure 61–19).;

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the TC coding violations register (see 45.2.6.12).;

30.11.2.1.6 aProfileSelect

ATTRIBUTE

APPROPRIATE SYNTAX:

SEQUENCE of the type INTEGER

BEHAVIOUR DEFINED AS:

A SEQUENCE of read-write values that indicates the operating profile numbers (see 62A.3.7 and 63A.4) of the PME. A 2BASE-TL PME supports a maximum of six values, 10PASS-TS PME can only support one. The operating profile can only be changed in a PME that is operating within a -O PHY subtype (see 61.1). As changing the operating profile is a traffic disruptive operation

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this can only occur when the link is down.

A GET operation returns the current operating profile number(s). A SET operation changes the operating profile to the indicated profile number only if the attribute aPHYEnd is “office” and the link is down. If the attribute aPHYEnd is “subscriber”, or the link is not down, a SET operation has no effect. If all values are zero, the PME operation is defined via the Clause 45 register settings (Table 45–57 and Table 45–58) rather than a specific profile.

NOTE 1—The profile selected by a particular value is different for 10PASS-TS and 2BASE-TL PHY types.

NOTE 2—For a 2BASE-TL PHY six profiles per region can be chosen for handshake (see 61.4) and the one with the highest data rate will be used.;

30.11.2.1.7 aOperatingProfile

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two instances, the first instances PMEProfileState is an ENUMERATED VALUE that has the following entries:

no link	link is down
match	link up using a profile
no match	link up not using a profile
activate failure	link activate failure

The second instances is an INTEGER

BEHAVIOUR DEFINED AS:

The ProfileState portion of the attribute is a read-only value that indicates the state of the operating profile. The enumeration “no link” indicates that the link is down, the enumeration “match” indicates that the link is up and achieved operating parameters match a defined complete profile (63A.3 and Table 63A–1), the enumeration “no match” indicates that the link is up but the achieved operating parameters do not match a defined complete profile and the enumeration “activate failure” indicates that the link failed to come up in any of the selected profiles.

The integer portion of the attribute is a read-only value that indicates the operating profile number. This value is only valid when the ProfileState portion of the attribute is “match”;

30.11.2.1.8 aPMEFECCorrectedBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 10 000 counts per second for 10 Mb/s implementations.

BEHAVIOUR DEFINED AS:

For a 10PASS-TS PME, a count of corrected FEC blocks. This counter will not increment for other PHY types.

Increment the counter by one for each received block that is corrected by the FEC function in the PME.

If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute will map to the 10P FEC correctable errors (see 45.2.1.41).;

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30.11.2.1.9 aPMEFECUncorrectableBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 10 000 counts per second for 10 Mb/s implementations.

BEHAVIOUR DEFINED AS:
For a 10PASS-TS PME, a count of uncorrectable FEC blocks. This counter will not increment for other PME types.

Increment the counter by one for each FEC block that is determined to be uncorrectable by the FEC function in the PME.

If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute will map to the 10P FEC uncorrectable errors counter (see 45.2.1.42).;

30.11.2.1.10 aTCCRCErrors

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 19 230 counts per second for 10 Mb/s implementations.

BEHAVIOUR DEFINED AS:
A count of TC-CRC errors.

Increment the counter by one for each TC-CRC error detected by the 64/65-octet receive function (see 61.3.3 and Figure 61–19).;

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the TC CRC error register (see 45.2.6.11).;

30.12 Layer Management for Link Layer Discovery Protocol (LLDP)

30.12.1 LLDP Configuration managed object class

This subclause formally defines the behaviours for the oLldpXdot3Config managed object class attributes.

30.12.1.1 LLDP Configuration attributes

30.12.1.1.1 aLldpXdot3PortConfigTLVsTxEnable

ATTRIBUTE

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
A read-write string of 7 bits indicating, for each of the IEEE 802.3 optional LLDP TLVs, if transmit is enabled on the local LLDP agent by the network management. A “1” in the bitstring indicates transmit of the TLV is enabled, “0” indicates transmit of the TLV is disabled. The value of this attribute is preserved across reset including loss of power.

Each bit of the bit string indicates whether transmit is enabled for the TLV corresponding to the

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bit. The mapping of bits to TLVs is:

first	MAC/PHY configuration/status TLV
second	Power via MDI TLV
third	Link Aggregation TLV (deprecated)
fourth	Maximum Frame Size TLV
fifth	EEE TLV
sixth	EEE Fast Wake TLV
seventh	Additional Ethernet Capabilities TLV.;

30.12.2 LLDP Local System Group managed object class

This subclause formally defines the behaviours for the oLldpXdot3LocSystemsGroup managed object class attributes.

30.12.2.1 LLDP Local System Group attributes

30.12.2.1.1 aLldpXdot3LocPortAutoNegSupported

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether the given port (associated with the local system) supports Auto-negotiation.;

30.12.2.1.2 aLldpXdot3LocPortAutoNegEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether port Auto-negotiation is enabled on the given port associated with the local system.;

30.12.2.1.3 aLldpXdot3LocPortAutoNegAdvertisedCap

ATTRIBUTE

APPROPRIATE SYNTAX:
OCTET STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A read-only 2-octet value that contains the value (bitmap) of the ifMauAutoNegCapAdvertisedBits object (defined in IETF RFC 4836) which is associated with the given port on the local system.;

30.12.2.1.4 aLldpXdot3LocPortOperMauType

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:

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A read-only 32-bit integer value that indicates the operational MAU type of the given port on the local system.

This object contains an integer value derived from the list position of the corresponding dot3MauType as listed in IETF RFC 4836 (or subsequent revisions) and is equal to the last number in the respective dot3MauType Object Identifier (OID).

For example, if the ifMauType object is dot3MauType1000BaseTHD which corresponds to {dot3MauType 29}, the numerical value of this field is 29. For MAU types not listed in IETF RFC 4836 (or subsequent revisions), the value of this field shall be set to zero.;

30.12.2.1.5 aLldpXdot3LocPowerPortClass

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

pClassPSE	PSE
pClassPD	PD

BEHAVIOUR DEFINED AS:

A read-only value that identifies the port Class of the given port associated with the local system.;

30.12.2.1.6 aLldpXdot3LocPowerMDISupported

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

For a PSE, this attribute contains a read-only Boolean value used to indicate whether the MDI power is supported on the given port associated with the local system. For a PD, the value of this attribute is undefined.;

30.12.2.1.7 aLldpXdot3LocPowerMDIEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

For a PSE, this attribute contains a read-only Boolean value used to identify whether MDI power is enabled on the given port associated with the local system. For a PD, the value of this attribute is undefined.;

30.12.2.1.8 aLldpXdot3LocPowerPairControllable

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value used to indicate the ability to control which PSE Pinout Alternative (see 33.2.3 and 145.2.4) is used for PD detection and power. For a PSE, this attribute contains the value of the aPSEPowerPairsControlAbility attribute (see 30.9.1.1.3). For a PD, the contents of

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this attribute are undefined.;

30.12.2.1.9 aLldpXdot3LocPowerPairs

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

signal	PSE Pinout Alternative A
spare	PSE Pinout Alternative B

BEHAVIOUR DEFINED AS:

A read-only value that identifies the PSE Pinout Alternative (see 33.2.3 and 145.2.4) in use for detecting and supplying power to the PD. For a PSE, this attribute contains a value derived from the aPSEPowerPairs attribute (see 30.9.1.1.4). For a PD, the contents of this attribute are undefined. A Type 3 or Type 4 PSE detecting or supplying power on both PSE Pinout Alternatives may return either PSE Pinout Alternative as this configuration is communicated through the aLldpXdot3LocPowerPairsExt attribute. A Type 3 or Type 4 PSE supplying power on only one PSE Pinout Alternative returns that PSE Pinout Alternative. For a PD, the contents of this attribute are undefined.;

30.12.2.1.10 aLldpXdot3LocPowerClass

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

class0	Class 0 PD
class1	Class 1 PD
class2	Class 2 PD
class3	Class 3 PD
class4	Class 4 PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the requested Class of the PD as specified in 33.2.6 and 145.2.8. This attribute returns an enumeration of “class4” for a PD of Class 4 or higher as such PD Classes are identified through the aLldpXdot3LocPowerClassExt attribute.;

30.12.2.1.11 aLldpXdot3LocLinkAggStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BITSTRING

BEHAVIOUR DEFINED AS:

The bitmap value which contains the link aggregation capabilities and the current aggregation status of the link (see 79.3.3.1).;

30.12.2.1.12 aLldpXdot3LocLinkAggPortId

ATTRIBUTE

APPROPRIATE SYNTAX:

The same as used for aAggPortID

BEHAVIOUR DEFINED AS:

This object contains the IEEE 802.3 aggregated port identifier, aAggPortID (see 30.7.2.1.1),

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derived from the ifNumber of the ifIndex for the port component in link aggregation.

If the port is not in link aggregation state and/or it does not support link aggregation, this value should be set to zero.;

30.12.2.1.13 aLldpXdot3LocMaxFrameSize

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
An integer value indicating the maximum supported frame size in octets on the given port of the local system.;

30.12.2.1.14 aLldpXdot3LocPowerType

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A GET attribute that returns a bit string indicating whether the local system is a PSE or a PD and whether it is Type 1 or greater than Type 1. The first bit indicates Type 1 or greater than Type 1. The second bit indicates PSE or PD. A PSE sets this bit to indicate a PSE. A PD sets this bit to indicate a PD. See also aLldpXdot3LocPowerTypeExt.;

30.12.2.1.15 aLldpXdot3LocPowerSource

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A GET attribute that returns a bit string indicating the power sources of the local system. A PSE indicates whether it is being powered by a primary power source; a backup power source; or unknown. A PD indicates whether it is being powered by a PSE and locally; by a PSE only; or unknown.;

30.12.2.1.16 aLldpXdot3LocPowerPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED value list that has the following entries:

low	low priority PD
high	high priority PD
critical	critical priority PD
unknown	priority unknown

BEHAVIOUR DEFINED AS:
A GET attribute that returns the priority of a PD system. For a PSE, this is the priority that the PSE assigns to the PD. For a PD, this is the priority that the PD requests from the PSE.
A SET operation changes the priority of the PD system to the indicated value.;

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30.12.2.1.17 aLldpXdot3LocPDRequestedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PD requested power value in units of 0.1 W. For a PD, it is the power value that the PD has currently requested from the remote system. The PD requested power value is the maximum input average power the PD ever draws under this power allocation if accepted. For a PSE, it is the power value that the PSE echoes back to the remote system. This is the PD requested power value that was used by the PSE to compute the power it has currently allocated to the remote system.;

30.12.2.1.18 aLldpXdot3LocPDRequestedPowerValueA

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PD requested power value for the Mode A pairset in units of 0.1 W. For a PD, it is the power value that the PD has currently requested from the remote system for the Mode A pairset. For a PSE, it is the power value for the Alternative A pairset that the PSE echoes back to the remote system.;

30.12.2.1.19 aLldpXdot3LocPDRequestedPowerValueB

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PD requested power value for the Mode B pairset in units of 0.1 W. For a PD, it is the power value that the PD has currently requested from the remote system for the Mode B pairset. For a PSE, it is the power value for the Alternative B pairset that the PSE echoes back to the remote system.;

30.12.2.1.20 aLldpXdot3LocPSEAllocatedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PSE allocated power value in units of 0.1 W. For a PSE, it is the power value that the PSE has currently allocated to the remote system. The PSE allocated power value is the maximum input average power that the PSE wants the PD to ever draw under this allocation if it is accepted. For a PD, it is the power value that the PD echoed back to the remote system.;

30.12.2.1.21 aLldpXdot3LocPSEAllocatedPowerValueA

ATTRIBUTE

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APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PSE allocated power value for the Alternative A pairset in units of 0.1 W. For a PSE, it is the power value for the Alternative A pairset that the PSE has currently allocated to the remote system. For a PD, it is the power value for the Mode A pairset that the PD echoes back to the remote system.;

30.12.2.1.22 aLldpXdot3LocPSEAllocatedPowerValueB

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PSE allocated power value for the Alternative B pairset in units of 0.1 W. For a PSE, it is the power value for the Alternative B pairset that the PSE has currently allocated to the remote system. For a PD, it is the power value for the Mode B pairset that the PD echoes back to the remote system.;

30.12.2.1.23 aLldpXdot3LocPSEPoweringStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

4PdualsigPD	4-pair powering a dual-signature PD
4PsinglesigPD	4-pair powering a single-signature PD
2P	2-pair powering

BEHAVIOUR DEFINED AS:
A read only value that indicates the powering status of the PSE. For a PD, the contents of this attribute are undefined.;

30.12.2.1.24 aLldpXdot3LocPDPoweredStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

4PdualsigPD	4-pair powered dual-signature PD
2PdualsigPD	2-pair powered dual-signature PD
singlesigPD	powered single-signature PD

BEHAVIOUR DEFINED AS:
A read only value that indicates the powering status of the PD. For a PSE, the contents of this attribute are undefined.;

30.12.2.1.25 aLldpXdot3LocPowerPairsExt

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

altA	Alternative A

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altB	Alternative B
both	Both Alternatives

BEHAVIOUR DEFINED AS:

A read-only value that identifies the supported PSE Pinout Alternative specified in 145.2.4. For a PSE, this attribute contains the value of the aPSEPowerPairs attribute (see 30.9.1.1.4). For a PD, the contents of this attribute are undefined.;

30.12.2.1.26 aLldpXdot3LocPowerClassExtA

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

singlesig	Single-signature PD or 2-pair only PSE
class1	Class 1
class2	Class 2
class3	Class 3
class4	Class 4
class5	Class 5

BEHAVIOUR DEFINED AS:

For a dual-signature PD, a read-only value that indicates the requested Class for Mode A during Physical Layer Classification (see 145.3.6). For a single-signature PD, a read-only value set to ‘singlesig’.

For a PSE connected to a dual-signature PD, a read-only value that indicates the currently assigned Class for Mode A (see 145.2.8). For a PSE connected to a single-signature PD or a PSE that operates only in 2-pair mode, a read-only value set to ‘singlesig’.;

30.12.2.1.27 aLldpXdot3LocPowerClassExtB

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

singlesig	Single-signature PD or 2-pair only PSE
class1	Class 1
class2	Class 2
class3	Class 3
class4	Class 4
class5	Class 5

BEHAVIOUR DEFINED AS:

For a dual-signature PD, a read-only value that indicates the requested Class for Mode B during Physical Layer Classification (see 145.3.6). For a single-signature PD, a read-only value set to ‘singlesig’.

For a PSE connected to a dual-signature PD, a read-only value that indicates the currently assigned Class for Mode B (see 145.2.8). For a PSE connected to a single-signature PD or a PSE that operates only in 2-pair mode, a read-only value set to ‘singlesig’.;

30.12.2.1.28 aLldpXdot3LocPowerClassExt

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

dualsig	Dual-signature PD

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class1	Class 1
class2	Class 2
class3	Class 3
class4	Class 4
class5	Class 5
class6	Class 6
class7	Class 7
class8	Class 8

BEHAVIOUR DEFINED AS:

For a single-signature PD, a read-only value that indicates the requested Class during Physical Layer Classification (see 145.3.6). For a dual-signature PD, a read-only value set to ‘dualsig’. For a PSE connected to a single-signature PD or a PSE that operates only in 2-pair mode, a read-only value that indicates the currently assigned Class (see 145.2.8). For a PSE connected to a dual-signature PD, a read-only value set to ‘dualsig’.;

30.12.2.1.29 aLldpXdot3LocPowerTypeExt

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

type4dualsigPD	Type 4 dual-signature PD
type4singlesigPD	Type 4 single-signature PD
type3dualsigPD	Type 3 dual-signature PD
type3singlesigPD	Type 3 single-signature PD
type4PSE	Type 4 PSE
type3PSE	Type 3 PSE

BEHAVIOUR DEFINED AS:

A read-only attribute that returns a value to indicate if the local system is a Type 3 or Type 4 PSE or PD and, in the case of a Type 3 or Type 4 PD, if it is a single-signature PD or a dual-signature PD.;

30.12.2.1.30 aLldpXdot3LocPDLoad

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

For a dual-signature PD, a GET attribute that returns whether the load of a dual-signature PD is electrically isolated, as defined in 79.3.2.10.2. For a single-signature PD or a PSE, the value of this attribute is FALSE.;

30.12.2.1.31 aLldpXdot3LocPD4PID

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean attribute indicating whether the local PD system supports powering of both PD Modes.;

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30.12.2.1.32 aLldpXdot3LocPSEMaxAvailPower

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the local PSE maximum available power value in units of 0.1 W.;

30.12.2.1.33 aLldpXdot3LocPSEAutoclassSupport

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A read-only attribute that returns a bit string indicating whether the local PSE system supports Autoclass.;

30.12.2.1.34 aLldpXdot3LocAutoclassCompleted

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A read-only attribute that returns a bit string indicating whether the local PSE system has completed the Autoclass measurement.;

30.12.2.1.35 aLldpXdot3LocAutoclassRequest

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A read-only attribute that returns a bit string indicating whether the local PD system is requesting an Autoclass measurement and power budget adjustment.;

30.12.2.1.36 aLldpXdot3LocPowerDownRequest

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A SET attribute that indicates the local PD system is requesting a power down when the value is 0x1D.;

30.12.2.1.37 aLldpXdot3LocPowerDownTime

ATTRIBUTE

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APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A SET attribute that indicates the number of seconds the PD requests to stay powered off. A value of zero indicates an indefinite amount of time.;

30.12.2.1.38 aLldpXdot3LocMeasVoltageSupport

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the local device is capable of providing a voltage measurement.;

30.12.2.1.39 aLldpXdot3LocMeasCurrentSupport

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the local device is capable of providing a current measurement.;

30.12.2.1.40 aLldpXdot3LocMeasPowerSupport

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the local device is capable of providing a power measurement.;

30.12.2.1.41 aLldpXdot3LocMeasEnergySupport

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the local device is capable of providing an energy measurement.;

30.12.2.1.42 aLldpXdot3LocMeasurementSource

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A SET attribute value that indicates to local device on which Alternative or Mode the measurement is to be taken.;

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30.12.2.1.43 aLldpXdot3LocMeasVoltageRequest

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the local device is requesting a voltage measurement from the remote device.;

30.12.2.1.44 aLldpXdot3LocMeasCurrentRequest

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the local device is requesting a current measurement from the remote device.;

30.12.2.1.45 aLldpXdot3LocMeasPowerRequest

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the local device is requesting a power measurement from the remote device.;

30.12.2.1.46 aLldpXdot3LocMeasEnergyRequest

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the local device is requesting an energy measurement from the remote device.;

30.12.2.1.47 aLldpXdot3LocMeasVoltageValid

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the local device’s voltage measurement is valid.;

30.12.2.1.48 aLldpXdot3LocMeasCurrentValid

ATTRIBUTE

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APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the local device's current measurement is valid.;

30.12.2.1.49 aLldpXdot3LocMeasPowerValid

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the local device's power measurement is valid.;

30.12.2.1.50 aLldpXdot3LocMeasEnergyValid

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (1)]

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the local device's energy measurement is valid.;

30.12.2.1.51 aLldpXdot3LocMeasVoltageUncertainty

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the expanded uncertainty (coverage factor k = 2) for the device's voltage measurement. See Table 79–21.;

30.12.2.1.52 aLldpXdot3LocMeasCurrentUncertainty

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the expanded uncertainty (coverage factor k = 2) for the device's current measurement. See Table 79–21.;

30.12.2.1.53 aLldpXdot3LocMeasPowerUncertainty

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the expanded uncertainty (coverage factor k = 2) for the device's power measurement. See Table 79–21.;

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30.12.2.1.54 aLldpXdot3LocMeasEnergyUncertainty

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the expanded uncertainty (coverage factor k = 2) for the device's energy measurement. See Table 79–21.;

30.12.2.1.55 aLldpXdot3LocVoltageMeasurement

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the measured device voltage. See Table 79–21.;

30.12.2.1.56 aLldpXdot3LocCurrentMeasurement

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the measured device current. See Table 79–21.;

30.12.2.1.57 aLldpXdot3LocPowerMeasurement

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the measured device power. See Table 79–21.;

30.12.2.1.58 aLldpXdot3LocEnergyMeasurement

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the measured device energy. See Table 79–21.;

30.12.2.1.59 aLldpXdot3LocPSEPowerPriceIndex

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

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BEHAVIOUR DEFINED AS:

A GET attribute that returns an index of the price of power being sourced by the PSE. For a PD, this value is undefined.;

30.12.2.1.60 aLldpXdot3LocResponseTime

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the response time in seconds of the local system. For a PD, it is the maximum time required to update the value of attribute aLldpXdot3LocPDRequestedPowerValue when the remote system requests the PD to change its max power draw. For a PSE, it is the maximum time required to update the value of attribute aLldpXdot3LocPDRequestedPowerValue when the remote system requests of the PSE a new power value.;

30.12.2.1.61 aLldpXdot3LocReady

ATTRIBUTE

APPROPRIATE SYNTAX:

A BOOLEAN value:

FALSE:	Local system has not completed initialization of the Data Link Layer classification engine and is not ready to receive/transmit an LLDPDU containing a Power via MDI TLV.
TRUE:	Local system has initialized the Data Link Layer classification engine and is ready to receive/transmit an LLDPDU containing a Power via MDI TLV.

BEHAVIOUR DEFINED AS:

A GET operation returns the initialization status of the Data Link Layer classification engine on the local system.;

30.12.2.1.62 aLldpXdot3LocTxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the local system can support in the transmit direction. This attribute maps to the variable LocTxSystemValue as defined in 78.4.2.3;

30.12.2.1.63 aLldpXdot3LocTxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the remote system is advertising that it can support in the transmit direction and is echoed by the local system under the control of the EEE DLL receiver state diagram. This attribute maps to the variable LocTxSystemValueEcho as

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defined in 78.4.2.3;

30.12.2.1.64 aLldpXdot3LocRxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the local system is requesting in the receive direction. This attribute maps to the variable LocRxSystemValue as defined in 78.4.2.3;

30.12.2.1.65 aLldpXdot3LocRxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the remote system is advertising that it is requesting in the receive direction and is echoed by the local system under the control of the EEE DLL transmitter state diagram. This attribute maps to the variable LocRxSystemValueEcho as defined in 78.4.2.3;

30.12.2.1.66 aLldpXdot3LocFbTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of the fallback $T_{w\_sys\_tx}$ that the local system is advertising to the remote system. This attribute maps to the variable LocFbSystemValue as defined in 78.4.2.3;

30.12.2.1.67 aLldpXdot3TxDllReady

ATTRIBUTE

APPROPRIATE SYNTAX:
A BOOLEAN value:

FALSE:	Local system has not completed initialization of the EEE transmit Data Link Layer management function and is not ready to receive/transmit an LLDPDU containing a EEE TLV.
TRUE:	Local system has initialized the EEE transmit Data Link Layer management function and is ready to receive/transmit an LLDPDU containing a EEE TLV.

BEHAVIOUR DEFINED AS:
A GET operation returns the initialization status of the EEE transmit Data Link Layer management function on the local system.;

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30.12.2.1.68 aLldpXdot3RxDllReady

ATTRIBUTE

APPROPRIATE SYNTAX:
A BOOLEAN value:

FALSE:	Local system has not completed initialization of the EEE receive Data Link Layer management function and is not ready to receive/transmit an LLDPDU containing a EEE TLV.
TRUE:	Local system has initialized the EEE receive Data Link Layer management function and is ready to receive/transmit an LLDPDU containing a EEE TLV.

BEHAVIOUR DEFINED AS:
A GET operation returns the initialization status of the EEE receive Data Link Layer management function on the local system.;

30.12.2.1.69 aLldpXdot3LocDllEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:
A BOOLEAN value:

FALSE:	Local system has not completed auto-negotiation with a link partner that has indicated at least one EEE capability.
TRUE:	Local system has completed auto-negotiation with a link partner that has indicated at least one EEE capability.

BEHAVIOUR DEFINED AS:
A GET operation returns the status of the EEE capability negotiation on the local system.;

30.12.2.1.70 aLldpXdot3LocTxFw

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the local system can support in the transmit direction. This attribute maps to the variable LocTxSystemFW as defined in 78.4.2.3;

30.12.2.1.71 aLldpXdot3LocTxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the remote system is advertising that it can support in the transmit direction and is echoed by the local system under the control of the EEE DLL receiver state diagram. This attribute maps to the variable LocTxSystemFWEcho as defined in 78.4.2.3;

30.12.2.1.72 aLldpXdot3LocRxFw

ATTRIBUTE

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APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the local system is requesting in the receive direction. This attribute maps to the variable LocRxSystemFW as defined in 78.4.2.3;

30.12.2.1.73 aLldpXdot3LocRxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the remote system is advertising that it is requesting in the receive direction and is echoed by the local system under the control of the EEE DLL transmitter state diagram. This attribute maps to the variable LocRxSystemFWEcho as defined in 78.4.2.3;

30.12.2.1.74 aLldpXdot3LocPreemptSupported

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether the given port (associated with the local System) supports the preemption capability.;

30.12.2.1.75 aLldpXdot3LocPreemptEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether the preemption capability is enabled on the given port associated with the local System.;

30.12.2.1.76 aLldpXdot3LocPreemptActive

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether the preemption capability is active on the given port associated with the local System.;

30.12.2.1.77 aLldpXdot3LocAddFragSize

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

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BEHAVIOUR DEFINED AS:

A 2-bit integer value used to indicate the minimum size of non-final fragments supported by the receiver on the given port associated with the local System. This value is expressed in units of 64 octets of additional fragment length. The minimum non-final fragment size is (aLldpXdot3LocAddFragSize + 1) × 64 octets.;

30.12.3 LLDP Remote System Group managed object class

This subclause formally defines the behaviours for the oLldpXdot3RemSystemsGroup managed object class attributes.

30.12.3.1 LLDP Remote System Group attributes

30.12.3.1.1 aLldpXdot3RemPortAutoNegSupported

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value used to indicate whether the given port (associated with the remote system) supports Auto-negotiation.;

30.12.3.1.2 aLldpXdot3RemPortAutoNegEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value used to indicate whether port Auto-negotiation is enabled on the given port associated with the remote system.;

30.12.3.1.3 aLldpXdot3RemPortAutoNegAdvertisedCap

ATTRIBUTE

APPROPRIATE SYNTAX:

OCTET STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A read-only 2-octet value that contains the value (bitmap) of the ifMauAutoNegCapAdvertisedBits object (defined in IETF RFC 4836) which is associated with the given port on the remote system.;

30.12.3.1.4 aLldpXdot3RemPortOperMauType

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A read-only 32-bit integer value that indicates the operational MAU type of the given port on the remote system.

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This object contains an integer value derived from the list position of the corresponding dot3MauType as listed in IETF RFC 4836 (or subsequent revisions) and is equal to the last number in the respective dot3MauType OID.

For example, if the ifMauType object is dot3MauType1000BaseTHD which corresponds to {dot3MauType 29}, the numerical value of this field is 29. For MAU types not listed in IETF RFC 4836 (or subsequent revisions), the value of this field shall be set to zero.;

30.12.3.1.5 aLldpXdot3RemPowerPortClass

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

pClassPSE	PSE
pClassPD	PD

BEHAVIOUR DEFINED AS:

A read-only value that identifies the port Class of the given port associated with the remote system.;

30.12.3.1.6 aLldpXdot3RemPowerMDISupported

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

This attribute contains a read-only Boolean value used to indicate whether the MDI power is supported on the given port associated with the remote PSE system. When the remote system is a PD, the value of this attribute is undefined.;

30.12.3.1.7 aLldpXdot3RemPowerMDIEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

This attribute contains a read-only Boolean value used to identify whether MDI power is enabled on the given port associated with the remote PSE system. When the remote system is a PD, the value of this attribute is undefined.;

30.12.3.1.8 aLldpXdot3RemPowerPairControllable

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value used to indicate the ability to control which PSE Pinout Alternative (see 33.2.3 and 145.2.4) is used for PD detection and power on the given port on the remote system. For a PD, this attribute contains the value of the aPSEPowerPairsControlAbility attribute (see 30.9.1.1.3) on the given port on the remote system. For a PSE, the contents of this attribute are undefined.;

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30.12.3.1.9 aLldpXdot3RemPowerPairs

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

signal	PSE Pinout Alternative A
spare	PSE Pinout Alternative B

BEHAVIOUR DEFINED AS:

A read-only value that identifies the supported PSE Pinout Alternative (see 33.2.3 and 145.2.4) in use for supplying power to the PD on the given port on the remote system. For a PD, this attribute contains a value derived from the aPSEPowerPairs attribute (see 30.9.1.1.4) on the given port on the remote system. For a PSE, the contents of this attribute are undefined. When the remote system is a Type 3 or Type 4 PSE supplying power on both PSE Pinout Alternatives, the value of this attribute can indicate either pinout. If the aLldpXdot3RemPowerPairsExt attribute is available, it will report this configuration.;

30.12.3.1.10 aLldpXdot3RemPowerClass

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

class0	Class 0 PD
class1	Class 1 PD
class2	Class 2 PD
class3	Class 3 PD
class4	Class 4 PD

BEHAVIOUR DEFINED AS:

A read-only value that identifies the requested Class of the PD as specified in 33.2.6 and 145.2.8 on the given port on the remote system. This attribute will return an enumeration of “class4” for a PD of Class 4 or higher as such PD Classes are identified through the aLldpXdot3RemPowerClassExt attribute.;

30.12.3.1.11 aLldpXdot3RemLinkAggStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BITSTRING

BEHAVIOUR DEFINED AS:

The bitmap value which contains the link aggregation capabilities and the current aggregation status of the link (see 79.3.3.1).;

30.12.3.1.12 aLldpXdot3RemLinkAggPortId

ATTRIBUTE

APPROPRIATE SYNTAX:

The same as used for aAggPortID

BEHAVIOUR DEFINED AS:

This object contains the IEEE 802.3 aggregated port identifier, aAggPortID (see 30.7.2.1.1), derived from the ifNumber of the ifIndex for the port component in link aggregation.

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If the port is not in link aggregation state and/or it does not support link aggregation, this value should be set to zero.;

30.12.3.1.13 aLldpXdot3RemMaxFrameSize

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
An integer value indicating the maximum supported frame size in octets on the given port of the remote system.;

30.12.3.1.14 aLldpXdot3RemPowerType

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A GET attribute that returns a bit string indicating whether the remote system is a PSE or a PD and whether it is Type 1 or greater than Type 1. The first bit indicates Type 1 or greater than Type 1. The second bit indicates PSE or PD. See also aLldpXdot3RemPowerTypeExt.;

30.12.3.1.15 aLldpXdot3RemPowerSource

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A GET attribute that returns a bit string indicating the power sources of the remote system. When the remote system is a PSE, it indicates whether it is being powered by a primary power source; a backup power source; or unknown. When the remote system is a PD, it indicates whether it is being powered by a PSE and locally; locally only; by a PSE only; or unknown.;

30.12.3.1.16 aLldpXdot3RemPowerPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED value list that has the following entries:

low	low priority PD
high	high priority PD
critical	critical priority PD
unknown	priority unknown

BEHAVIOUR DEFINED AS:
A GET operation returns the priority of the PD system received from the remote system. For a PSE, this is the priority that the remote system requests from the PSE. For a PD, this is the priority that the remote system has assigned to the PD.;

30.12.3.1.17 aLldpXdot3RemPDRequestedPowerValue

ATTRIBUTE

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APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PD requested power value that was used by the remote system to compute the power value that it has currently allocated to the PD. For a PSE, it is the PD requested power value received from the remote system. The definition and encoding of PD requested power value is the same as described in aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17). For a PD, it is the mirrored copy of the requested power field echoed back by the remote PSE.;

30.12.3.1.18 aLldpXdot3RemPDRequestedPowerValueA

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PD requested power value for the Mode A pairset that was used by the remote system to compute the power value that it has currently allocated to the PD. For a PSE, it is the PD requested power value for the Alternative A pairset received from the remote system. For a PD, it is the PD requested power value for the Alternative A pairset that the PSE echoes back to the remote system. The definition and encoding of PD requested power value for the Mode A pairset is the same as described in aLldpXdot3LocPDRequestedPowerValueA (30.12.2.1.18).;

30.12.3.1.19 aLldpXdot3RemPDRequestedPowerValueB

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PD requested power value for the Mode B pairset that was used by the remote system to compute the power value that it has currently allocated to the PD. For a PSE, it is the PD requested power value for the Alternative B pairset received from the remote system. For a PD, it is the PD requested power value for the Alternative B pairset that the PSE echoes back to the remote system. The definition and encoding of PD requested power value for the Mode B pairset is the same as described in aLldpXdot3LocPDRequestedPowerValueB (30.12.2.1.19).;

30.12.3.1.20 aLldpXdot3RemPSEAllocatedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PSE allocated power value received from the remote system. For a PSE, it is the PSE allocated power value that was echoed back by the remote PD. For a PD, it is the PSE allocated power value received from the remote system. The definition and encoding of PSE allocated power value is the same as described in aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.20).;

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30.12.3.1.21 aLldpXdot3RemPSEAllocatedPowerValueA

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PSE allocated power value for the Alternative A pairset received from the remote system. For a PSE, it is the PSE allocated power value for the Alternative A pairset that was echoed back by the remote PD. For a PD, it is the PSE allocated power value for the Mode A pairset received from the remote system. The definition and encoding of PSE allocated power value for the Alternative A pairset is the same as described in aLldpXdot3LocPSEAllocatedPowerValueA (30.12.2.1.21).;

30.12.3.1.22 aLldpXdot3RemPSEAllocatedPowerValueB

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PSE allocated power value for the Alternative B pairset received from the remote system. For a PSE, it is the PSE allocated power value for the Alternative B pairset that was echoed back by the remote PD. For a PD, it is the PSE allocated power value for the Mode B pairset received from the remote system. The definition and encoding of PSE allocated power value for the Alternative B pairset is the same as described in aLldpXdot3LocPSEAllocatedPowerValueB (30.12.2.1.22).;

30.12.3.1.23 aLldpXdot3RemPSEPoweringStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

4PdualsigPD	4-pair powering a dual-signature PD
4PsinglesigPD	4-pair powering a single-signature PD
2P	2-pair powering

BEHAVIOUR DEFINED AS:
A read only value that indicates the powering status of the remote PSE. For a PSE, the contents of this attribute are undefined.;

30.12.3.1.24 aLldpXdot3RemPDPoweredStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

4PdualsigPD	4-pair powered dual-signature PD
2PdualsigPD	2-pair powered dual-signature PD
singlesigPD	powered single-signature PD

BEHAVIOUR DEFINED AS:
A read only value that indicates the powering status of the remote PD. For a PD, the contents of this attribute are undefined.;

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30.12.3.1.25 aLldpXdot3RemPowerPairsExt

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

altA	Alternative A
altB	Alternative B
both	Both Alternatives

BEHAVIOUR DEFINED AS:

A read-only value that identifies the supported PSE Pinout Alternative specified in 145.2.4. For a PD, this attribute contains the value of the aPSEPowerPairs attribute (see 30.9.1.1.4) as sent by the remote PSE. For a PSE, the contents of this attribute are undefined.;

30.12.3.1.26 aLldpXdot3RemPowerClassExtA

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

singlesig	Single-signature PD or 2-pair only PSE
class1	Class 1
class2	Class 2
class3	Class 3
class4	Class 4
class5	Class 5

BEHAVIOUR DEFINED AS:

For a dual-signature PD, a read-only value that indicates the currently assigned Class for Mode A by the remote 4-pair PSE. For a single-signature PD or a dual-signature PD connected to a 2-pair only PSE, a read-only value set to ‘singlesig’ by the remote PSE. For a PSE connected to a dual-signature PD, a read-only value that indicates the requested Class for Mode A during Physical Layer classification (see 145.2.8) by the remote PD. For a PSE connected to a single-signature PD, a read-only value set to ‘singlesig’ by the remote PD.;

30.12.3.1.27 aLldpXdot3RemPowerClassExtB

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

singlesig	Single-signature PD or 2-pair only PSE
class1	Class 1
class2	Class 2
class3	Class 3
class4	Class 4
class5	Class 5

BEHAVIOUR DEFINED AS:

For a dual-signature PD, a read-only value that indicates the currently assigned Class for Mode B by the remote 4-pair PSE. For a single-signature PD or a dual-signature PD connected to a 2-pair only PSE, a read-only value set to ‘singlesig’ by the remote PSE. For a PSE connected to a dual-signature PD, a read-only value that indicates the requested Class for Mode B during Physical Layer classification (see 145.2.8) by the remote PD. For a PSE connected to a single-signature PD, a read-only value set to ‘singlesig’ by the remote PD.;

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30.12.3.1.28 aLldpXdot3RemPowerClassExt

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

dualsig	Dual-signature PD
class1	Class 1
class2	Class 2
class3	Class 3
class4	Class 4
class5	Class 5
class6	Class 6
class7	Class 7
class8	Class 8

BEHAVIOUR DEFINED AS:

For a single-signature PD or a dual-signature PD connected to a 2-pair only PSE, a read-only value that indicates the currently assigned Class by the remote PSE. For a dual-signature PD connected to a 4-pair capable PSE, a read-only value set to ‘dualsig’ by the remote PSE. For a PSE connected to a single-signature PD, a read-only value that indicates the requested Class during Physical Layer classification (see 145.2.8) by the remote PD. For a PSE connected to a dual-signature PD, a read-only value set to ‘dualsig’ by the remote PD.;

30.12.3.1.29 aLldpXdot3RemPowerTypeExt

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

type4dualsigPD	Type 4 dual-signature PD
type4singlesigPD	Type 4 single-signature PD
type3dualsigPD	Type 3 dual-signature PD
type3singlesigPD	Type 3 single-signature PD
type4PSE	Type 4 PSE
type3PSE	Type 3 PSE

BEHAVIOUR DEFINED AS:

A read-only attribute that returns a value to indicate if the remote system is a Type 3 or Type 4 PSE or PD and, in the case of a Type 3 or Type 4 PD, if it is a single-signature PD or dual-signature PD.;

30.12.3.1.30 aLldpXdot3RemPDLoad

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

For a PSE, a GET attribute that returns whether the load of the remote dual-signature PD is electrically isolated, as defined in 79.3.2.10.2. For a PD, this attribute is set to FALSE.;

30.12.3.1.31 aLldpXdot3RemPD4PID

ATTRIBUTE

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APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean attribute indicating whether the remote PD system supports powering of both PD Modes.;

30.12.3.1.32 aLldpXdot3RemPSEMaxAvailPower

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the remote PSE maximum available power value in units of 0.1 W.;

30.12.3.1.33 aLldpXdot3RemPSEAutoclassSupport

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean attribute indicating whether the remote PSE system supports Autoclass.;

30.12.3.1.34 aLldpXdot3RemAutoclassCompleted

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean attribute indicating whether the remote PSE system has completed the Autoclass measurement.;

30.12.3.1.35 aLldpXdot3RemAutoclassRequest

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean attribute indicating whether the remote PD system is requesting an Autoclass measurement.;

30.12.3.1.36 aLldpXdot3RemPowerDownRequest

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A read-only attribute that indicates the remote PD system is requesting a power down when the value is 0x1D.;

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30.12.3.1.37 aLldpXdot3RemPowerDownTime

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the number of seconds the remote PD requests to stay powered off. A value of zero indicates an indefinite amount of time.;

30.12.3.1.38 aLldpXdot3RemMeasVoltageSupport

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that indicates if the remote device is capable of providing a voltage measurement.;

30.12.3.1.39 aLldpXdot3RemMeasCurrentSupport

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that indicates if the remote device is capable of providing a current measurement.;

30.12.3.1.40 aLldpXdot3RemMeasPowerSupport

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that indicates if the remote device is capable of providing a power measurement.;

30.12.3.1.41 aLldpXdot3RemMeasEnergySupport

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that indicates if the remote device is capable of providing an energy measurement.;

30.12.3.1.42 aLldpXdot3RemMeasurementSource

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

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BEHAVIOUR DEFINED AS:

A SET attribute value that indicates on which Alternative or Mode the measurement was taken by the remote device.;

30.12.3.1.43 aLldpXdot3RemMeasVoltageRequest

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device is requesting a voltage measurement from the local device.;

30.12.3.1.44 aLldpXdot3RemMeasCurrentRequest

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device is requesting a current measurement from the local device.;

30.12.3.1.45 aLldpXdot3RemMeasPowerRequest

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device is requesting a power measurement from the local device.;

30.12.3.1.46 aLldpXdot3RemMeasEnergyRequest

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device is requesting an energy measurement from the local device.;

30.12.3.1.47 aLldpXdot3RemMeasVoltageValid

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the remote device’s voltage measurement is valid.;

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30.12.3.1.48 aLldpXdot3RemMeasCurrentValid

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the remote device's current measurement is valid.;

30.12.3.1.49 aLldpXdot3RemMeasPowerValid

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the remote device's power measurement is valid.;

30.12.3.1.50 aLldpXdot3RemMeasEnergyValid

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the remote device's energy measurement is valid.;

30.12.3.1.51 aLldpXdot3RemMeasVoltageUncertainty

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the expanded uncertainty (coverage factor k = 2) for the remote device's voltage measurement. See Table 79–21.;

30.12.3.1.52 aLldpXdot3RemMeasCurrentUncertainty

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that indicates the expanded uncertainty (coverage factor k = 2) for the remote device's current measurement. See Table 79–21.;

30.12.3.1.53 aLldpXdot3RemMeasPowerUncertainty

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

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BEHAVIOUR DEFINED AS:

A GET attribute that indicates the expanded uncertainty (coverage factor k = 2) for the remote device's power measurement. See Table 79–21.;

30.12.3.1.54 aLldpXdot3RemMeasEnergyUncertainty

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that indicates the expanded uncertainty (coverage factor k = 2) for the remote device's energy measurement. See Table 79–21.;

30.12.3.1.55 aLldpXdot3RemVoltageMeasurement

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the measured remote device voltage. See Table 79–21.;

30.12.3.1.56 aLldpXdot3RemCurrentMeasurement

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the measured remote device current. See Table 79–21.;

30.12.3.1.57 aLldpXdot3RemPowerMeasurement

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the measured remote device power. See Table 79–21.;

30.12.3.1.58 aLldpXdot3RemEnergyMeasurement

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the measured remote device energy. See Table 79–21.;

30.12.3.1.59 aLldpXdot3RemPSEPowerPriceIndex

ATTRIBUTE

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APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns an index of the price of power being sourced by the remote PSE. For a PSE, this value is undefined.;

30.12.3.1.60 aLldpXdot3RemTxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the remote system can support in the transmit direction. This attribute maps to the variable RemTxSystemValue as defined in 78.4.2.3;

30.12.3.1.61 aLldpXdot3RemTxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the local system is advertising that it can support in the transmit direction as echoed by the remote system under the control of the EEE DLL receiver state diagram. This attribute maps to the variable RemTxSystemValueEcho as defined in 78.4.2.3;

30.12.3.1.62 aLldpXdot3RemRxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the remote system is requesting in the receive direction. This attribute maps to the variable RemRxSystemValue as defined in 78.4.2.3;

30.12.3.1.63 aLldpXdot3RemRxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the local system is advertising that it is requesting in the receive direction as echoed by the remote system under the control of the EEE DLL transmitter state diagram. This attribute maps to the variable RemRxSystemValueEcho as defined in 78.4.2.3;

30.12.3.1.64 aLldpXdot3RemFbTwSys

ATTRIBUTE

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APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of fallback $T_{w\_sys\_tx}$ that the remote system is advertising. This attribute maps to the variable RemFbSystemValue as defined in 78.4.2.3;

30.12.3.1.24 aLldpXdot3RemTxFw

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the remote system can support in the transmit direction. This attribute maps to the variable RemTxSystemFW as defined in 78.4.2.3;

30.12.3.1.25 aLldpXdot3RemTxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the local system is advertising that it can support in the transmit direction as echoed by the remote system under the control of the EEE DLL receiver state diagram. This attribute maps to the variable RemTxSystemFWEcho as defined in 78.4.2.3;

30.12.3.1.26 aLldpXdot3RemRxFw

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the remote system is requesting in the receive direction. This attribute maps to the variable RemRxSystemFW as defined in 78.4.2.3;

30.12.3.1.27 aLldpXdot3RemRxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the local system is advertising that it is requesting in the receive direction as echoed by the remote system under the control of the EEE DLL transmitter state diagram. This attribute maps to the variable RemRxSystemFWEcho as defined in 78.4.2.3;

30.12.3.1.28 aLldpXdot3RemPreemptSupported

ATTRIBUTE

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APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether the given port (associated with the remote system) supports the preemption capability.;

30.12.3.1.29 aLldpXdot3RemPreemptEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether the preemption capability is enabled on the given port associated with the remote system.;

30.12.3.1.30 aLldpXdot3RemPreemptActive

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether the preemption capability is active on the given port associated with the remote system.;

30.12.3.1.31 aLldpXdot3RemAddFragSize

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A 2-bit integer value used to indicate, in units of 64 octets, the minimum number of octets over 64 octets required in non-final fragments by the receiver on the given port associated with the remote system. The minimum non-final fragment size is (aLldpXdot3LocAddFragSize + 1) × 64 octets.;

30.13 Management for oTimeSync entity

If the optional TimeSync function is implemented, then the oTimeSync managed object class shall be implemented in its entirety. All attributes of this managed object class are mandatory. TimeSync management is optional with respect to all other CSMA/CD management.

30.13.1 TimeSync entity managed object class

This subclause formally defines the behaviours for the oTimeSync managed object class attributes.

30.13.1.1 aTimeSyncCapabilityTX

ATTRIBUTE

APPROPRIATE SYNTAX:

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BOOLEAN

BEHAVIOUR DEFINED AS:

True if the TimeSync capability is supported in the transmit path and false otherwise.
If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute is equal to the logical OR operation over the values stored in the following instantiated MDIO registers (for each MMD, in case of multiple instances) 1.1800.1, 2.1800.1, 3.1800.1, 4.1800.1, 5.1800.1, and 6.1800.1 (see 45.2.1.175, 45.2.2.20, 45.2.3.67, 45.2.4.28, 45.2.5.28, 45.2.6.14, respectively).

30.13.1.2 aTimeSyncCapabilityRX

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

True if the TimeSync capability is supported in the receive path and false otherwise.
If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute is equal to the logical OR operation over the values stored in the following instantiated MDIO registers (for each MMD, in case of multiple instances) 1.1800.0, 2.1800.0, 3.1800.0, 4.1800.0, 5.1800.0, and 6.1800.0 (see 45.2.1.175, 45.2.2.20, 45.2.3.67, 45.2.4.28, 45.2.5.28, 45.2.6.14, respectively).

30.13.1.3 aTimeSyncDelayTXmax

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The maximum data delay as specified in 90.7, expressed in units of ns.
If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute represents the maximum transmit path data delay values, consisting of the sum of the values of the registers in the instantiated sublayers (for each MMD, in case of multiple instances):

— for PMA/PMD: 1.1801 and 1.1802, see 45.2.1.176
— for WIS: 2.1801 and 2.1802, see 45.2.2.21
— for PCS: 3.1801 and 3.1802, see 45.2.3.68
— for PHY XS: 4.1801 and 4.1802, see 45.2.4.29
— for DTE XS: 5.1801 and 5.1802, see 45.2.5.29
— for TC: 6.1801 and 6.1802, see 45.2.6.15

30.13.1.4 aTimeSyncDelayTXmin

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The minimum data delay as specified in 90.7, expressed in units of ns.
If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present,

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then the value stored in this attribute represents the minimum transmit path data delay values, consisting of the sum of the values of the registers in the instantiated sublayers (for each MMD, in case of multiple instances):

— for PMA/PMD: 1.1803 and 1.1804, see 45.2.1.176
— for WIS: 2.1803 and 2.1804, see 45.2.2.21
— for PCS: 3.1803 and 3.1804, see 45.2.3.68
— for PHY XS: 4.1803 and 4.1804, see 45.2.4.29
— for DTE XS: 5.1803 and 5.1804, see 45.2.5.29
— for TC: 6.1803 and 6.1804, see 45.2.6.15

30.13.1.5 aTimeSyncDelayRXmax

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The maximum data delay as specified in 90.7, expressed in units of ns.
If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute represents the maximum receive path data delay values, consisting of the sum of the values of the registers in the instantiated sublayers (for each MMD, in case of multiple instances):

— for PMA/PMD: 1.1805 and 1.1806, see 45.2.1.177
— for WIS: 2.1805 and 2.1806, see 45.2.2.22
— for PCS: 3.1805 and 3.1806, see 45.2.3.69
— for PHY XS: 4.1805 and 4.1806, see 45.2.4.30
— for DTE XS: 5.1805 and 5.1806, see 45.2.5.30
— for TC: 6.1805 and 6.1806, see 45.2.6.16

30.13.1.6 aTimeSyncDelayRXmin

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The minimum data delay as specified in 90.7, expressed in units of ns.
If a Clause 45 MDIO Interface to to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute represents the minimum receive path data delay values, consisting of the sum of the values of the registers in the instantiated sublayers (for each MMD, in case of multiple instances):

— for PMA/PMD: 1.1807 and 1.1808, see 45.2.1.177
— for WIS: 2.1807 and 2.1808, see 45.2.2.22
— for PCS: 3.1807 and 3.1808, see 45.2.3.69
— for PHY XS: 4.1807 and 4.1808, see 45.2.4.30
— for DTE XS: 5.1807 and 5.1808, see 45.2.5.30
— for TC: 6.1807 and 6.1808, see 45.2.6.16

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30.14 Management for MAC Merge Sublayer

30.14.1 oMACMergeEntity managed object class

This subclause formally defines the behaviours for the oMACMergeEntity managed object class attributes.

30.14.1.1 aMACMergeSupport

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

supported	MAC Merge sublayer is supported on the device
not supported	MAC Merge sublayer is not supported on the device

BEHAVIOUR DEFINED AS:

This attribute indicates (when accessed via a GET operation) whether the given device supports a MAC Merge sublayer. The SET operation shall have no effect on a device.;

30.14.1.2 aMACMergeStatusVerify

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	verification status is unknown
initial	the Verify State diagram (Figure 99–8) is in the state INIT_VERIFICATION
verifying	the Verify State diagram is in the state VERIFICATION_IDLE, SEND_VERIFY or WAIT_FOR_RESPONSE
succeeded	indicates that the Verify State diagram is in the state VERIFIED
failed	the Verify State diagram is in the state VERIFY_FAIL
disabled	verification of preemption operation is disabled

BEHAVIOUR DEFINED AS:

This attribute indicates (when accessed via a GET operation) the status of the MAC Merge sublayer verification on the given device. The SET operation shall have no effect on a device.;

30.14.1.3 aMACMergeEnableTx

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

disabled	transmit preemption is disabled
enabled	transmit preemption is enabled

BEHAVIOUR DEFINED AS:

This attribute indicates (when accessed via a GET operation) the status of the MAC Merge sublayer on the given device in the transmit direction. The status of the MAC Merge sublayer may be modified to the indicated value via a SET operation. This attribute maps to the variable pEnable (see 99.4.7.3).;

30.14.1.4 aMACMergeVerifyDisableTx

ATTRIBUTE

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APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

disabled	verify is disabled
enabled	verify is enabled

BEHAVIOUR DEFINED AS:

This attribute indicates (when accessed via a GET operation) the status of the Verify function of MAC Merge sublayer on the given device in the transmit direction. The status of the Verify function may be modified to the indicated value via a SET operation. This attribute maps to the variable disableVerify (see 99.4.7.3).;

30.14.1.5 aMACMergeStatusTx

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	transmit preemption status is unknown
inactive	transmit preemption is inactive
active	transmit preemption is active

BEHAVIOUR DEFINED AS:

This attribute indicates (when accessed via a GET operation) the status of the MAC Merge sublayer on the given device in the transmit direction. The SET operation shall have no effect on a device. This attribute maps to the variable preempt (see 99.4.7.3).;

30.14.1.6 aMACMergeVerifyTime

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of this attribute defines the nominal wait time between verification attempts in milliseconds. Valid range is 1 to 128 inclusive. The default value is 10. This attribute maps to the variable verifyTime (see 99.4.7.3).;

30.14.1.7 aMACMergeAddFragSize

ATTRIBUTE

APPROPRIATE SYNTAX

INTEGER

BEHAVIOUR DEFINED AS:

A 2-bit integer value used to indicate the value of addFragSize variable used by the Transmit Processing State Diagram (see Figure 99–5).;

30.14.1.8 aMACMergeFrameAssErrorCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter.
This counter has a maximum increment rate of 160 000 counts per second at 100 Mb/s.

BEHAVIOUR DEFINED AS:

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A count of MAC frames with reassembly errors. The counter is incremented by one every time the ASSEMBLY_ERROR state in the Receive Processing State Diagram is entered (see Figure 99–6).;

30.14.1.9 aMACMergeFrameSmdErrorCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter.
This counter has a maximum increment rate of 160 000 counts per second at 100 Mb/s.

BEHAVIOUR DEFINED AS:

A count of received MAC frames / MAC frame fragments rejected due to unknown SMD value or arriving with an SMD-C when no frame is in progress. The counter is incremented by one every time the BAD_FRAG state in the Receive Processing State Diagram is entered and every time the WAIT_FOR_DV_FALSE state is entered due to the invocation of the SMD_DECODE function returning the value “ERR” (see Figure 99–6).;

30.14.1.10 aMACMergeFrameAssOkCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter.
This counter has a maximum increment rate of 160 000 counts per second at 100 Mb/s.

BEHAVIOUR DEFINED AS:

A count of MAC frames that were successfully reassembled and delivered to MAC. The counter is incremented by one every time the FRAME_COMPLETE state in the Receive Processing state diagram (see Figure 99–6) is entered if the state CHECK_FOR_RESUME was previously entered while processing the packet.;

30.14.1.11 aMACMergeFragCountRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter.
This counter has a maximum increment rate of 160 000 counts per second at 100 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of additional mPackets received due to preemption. The counter is incremented by one every time the state CHECK_FRAG_CNT in the Receive Processing State Diagram (see Figure 99–6) is entered.;

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30.14.1.12 aMACMergeFragCountTx

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter.
This counter has a maximum increment rate of 160 000 counts per second at 100 Mb/s

BEHAVIOUR DEFINED AS:
A count of the number of additional mPackets transmitted due to preemption. This counter is incremented by one every time the SEND_SMD_C state in the Transmit Processing State Diagram (see Figure 99–5) is entered.;

30.14.1.13 aMACMergeHoldCount

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter.
This counter has a maximum increment rate of 160 000 counts per second at 100 Mb/s.

BEHAVIOUR DEFINED AS:
A count of the number of times the variable hold (see 99.4.7.3) transitions from FALSE to TRUE.;

30.15 Layer management for Power over Data Lines (PoDL) of Single Pair Ethernet

30.15.1 PoDL PSE managed object class

This subclause formally defines the behaviours for the oPoDLPSE managed object class attributes and actions.

30.15.1.1 PoDL PSE attributes

30.15.1.1.1 aPoDLPSEID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aPoDLPSEID is assigned so as to uniquely identify a PoDL PSE among the subordinate managed objects of the containing object.;

30.15.1.1.2 aPoDLPSEAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

enabled	PoDL PSE functions enabled
disabled	PoDL PSE functions disabled

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational state of the PoDL PSE functions. An interface that can provide the PoDL PSE functions specified in Clause 104 is enabled to do so when this attribute has the enumeration “enabled”. When this attribute has the enumeration “disabled” the interface

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acts as if it had no PoDL PSE function. The operational state of the PSE function can be changed using the acPoDLPSEAdminControl action.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PSE Enable bit specified in 45.2.9.1.2.;

30.15.1.1.3 aPoDLPSEPowerDetectionStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	true state unknown
disabled	PoDL PSE disabled
searching	PoDL PSE searching
deliveringPower	PoDL PSE delivering power
sleep	PoDL PSE sleep
idle	PoDL PSE idle
error	PoDL PSE error

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PoDL PSE.

The enumeration “disabled” is asserted true when the PoDL PSE state diagram variable mr_pse_enable is false (see 104.4.4.3). The enumeration “deliveringPower” is asserted true when the PoDL PSE state diagram variable pi_powered is true. The enumeration “sleep” is asserted true when the PoDL PSE state diagram variable pi_sleeping is true. The enumeration “searching” is asserted true when either of the PSE state diagram variables pi_detecting or pi_classifying is true. The enumeration “idle” is asserted true when the logical combination of the PoDL PSE state diagram variables pi_prebiased*!pi_sleeping is true. The enumeration “error” is asserted true when the PoDL PSE state diagram variable overload_held is true.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PSE Status bits specified in 45.2.9.2.9.;

30.15.1.1.4 aPoDLPSEType

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	initializing, true state not yet known
typeA	Type A PoDL PSE
typeB	Type B PoDL PSE
typeC	Type C PoDL PSE
typeD	Type D PoDL PSE
typeE	Type E PoDL PSE
typeF	Type F PoDL PSE

BEHAVIOUR DEFINED AS:

A read-only value that identifies the PoDL PSE Type specified in 104.4.1.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PSE Type bits specified in 45.2.9.2.7.;

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30.15.1.1.5 aPoDLPSEDetectedPDType

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	initializing, true state not yet known
typeA	Type A PoDL PD
typeB	Type B PoDL PD
typeC	Type C PoDL PD
typeD	Type D PoDL PD
typeE	Type E PoDL PD
typeF	Type F PoDL PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the Type of the detected PoDL PD as specified in 104.5.1. This value is only valid while a PD is being powered, that is the attribute aPoDLPSEPowerDetectionStatus is reporting the enumeration “deliveringPower”.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PD Type bits specified in 45.2.9.3.3.;

30.15.1.1.6 aPoDLPSEDetectedPDPowerClass

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	initializing, true state not yet known
class0	Class 0 PoDL PD
class1	Class 1 PoDL PD
class2	Class 2 PoDL PD
class3	Class 3 PoDL PD
class4	Class 4 PoDL PD
class5	Class 5 PoDL PD
class6	Class 6 PoDL PD
class7	Class 7 PoDL PD
class8	Class 8 PoDL PD
class9	Class 9 PoDL PD
class10	Class 10 PoDL PD
class11	Class 11 PoDL PD
class12	Class 12 PoDL PD
class13	Class 13 PoDL PD
class14	Class 14 PoDL PD
class15	Class 15 PoDL PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the class of the detected PoDL PD as specified in Table 104–1 and Table 104–2. This value is only valid while a PD is being powered, that is the attribute aPoDLPSEPowerDetectionStatus is reporting the enumeration “deliveringPower”.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PD Class and PD Extended Class bits specified in 45.2.9.2.8 and 45.2.9.3.2.;

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30.15.1.1.7 aPoDLPSEInvalidSignatureCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PoDL PSE state diagram variable mr_invalid_signature transitions from false to true (see 104.4.4.3).

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the invalid signature bit specified in 45.2.9.2.3.;

30.15.1.1.8 aPoDLPSEInvalidClassCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PoDL PSE state diagram variable tclass_timer_done transitions from false to true or when the valid_class variable transitions from true to false (see 104.4.4.3).

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the class timeout bit specified in 45.2.9.2.4.;

30.15.1.1.9 aPoDLPSEPowerDeniedCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PoDL PSE state diagram variable power_available transitions from true to false (see 104.4.4.3).

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the power denied bit specified in 45.2.9.2.1.;

30.15.1.1.10 aPoDLPSEOverLoadCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 13 counts per 10 seconds.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram variable overload_held transitions from false to true (see 104.4.4.3).

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If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the overload bit specified in 45.2.9.2.5.;

30.15.1.1.11 aPoDLPSEMaintainFullVoltageSignatureAbsentCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 33 counts per 10 seconds.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PoDL PSE state diagram variable mfvs_timeout transitions from false to true (see 104.4.4.3).

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the Maintain Full Voltage Signature Absent bit specified in 45.2.9.2.6.;

30.15.1.1.12 aPoDLPSEActualPower

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

An integer value indicating present (actual) power being supplied by the PoDL PSE as measured at the MDI in milliwatts. The behaviour is undefined if the state of aPoDLPSEPowerDetectionStatus is anything other than “deliveringPower”. The sampling frequency and averaging are vendor-defined.;

30.15.1.1.13 aPoDLPSEPowerAccuracy

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A signed integer value indicating the accuracy associated with aPoDLPSEActualPower in milliwatts.;

30.15.1.1.14 aPoDLPSECumulativeEnergy

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. The counter has a maximum increment rate of 100 000 per second.

BEHAVIOUR DEFINED AS:

A count of the cumulative energy supplied by the PoDL PSE, measured at the MDI, and expressed in units of millijoules.;

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30.15.1.2 PoDL PSE actions

30.15.1.2.1 acPoDLPSEAdminControl

ACTION

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

enabled	PoDL PSE functions enabled
disabled	PoDL PSE functions disabled

BEHAVIOUR DEFINED AS:
This action provides a means to alter aPoDLPSEAdminState.;

30.16 Management for PLCA Reconciliation Sublayer

30.16.1 PLCA managed object class

This subclause formally defines the behaviours for the oPLCA managed object class attributes and actions.

30.16.1.1 PLCA attributes

30.16.1.1.1 aPLCAAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
disabled
enabled

BEHAVIOUR DEFINED AS:
A read-only value that indicates the mode of operation of the Reconciliation Sublayer for PLCA operation. When PLCA is enabled, the Reconciliation Sublayer functions in PLCA mode, whose operation is defined by Clause 148. When PLCA functions are not supported or are disabled by the management interface (plca_en = FALSE), RS operation shall conform to the RS definition in Clause 22. By default, PLCA is disabled.;

30.16.1.1.2 aPLCAStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
TRUE
FALSE

BEHAVIOUR DEFINED AS:
A read-only value that indicates whether PLCA Control state diagram is receiving BEACON indication or transmitting BEACON request. This parameter maps to the plca_status variable in 148.4.6.2.;

30.16.1.1.3 aPLCANodeCount

ATTRIBUTE

APPROPRIATE SYNTAX:

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INTEGER

BEHAVIOUR DEFINED AS:

This value is assigned to define the number of nodes getting a transmit opportunity before a new BEACON is generated. Valid range is 0 to 255, inclusive. The default value is 8.;

30.16.1.1.4 aPLCALocalNodeID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

This value is assigned to define the ID of the local node on the PLCA network. The default value is 255. Value range is 0 to 255, inclusive.;

30.16.1.1.5 aPLCATransmitOpportunityTimer

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

This value is assigned to define the time between PLCA transmit opportunities for the node. aPLCATransmitOpportunityTimer maps to the duration of the timer to_timer. The value of aPLCATransmitOpportunityTimer represents the duration of to_timer in bit times. Valid range is 1 to 255, inclusive. The default value is 32. See 148.4.4.4.;

30.16.1.1.6 aPLCAMaxBurstCount

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

Maximum number of additional packets the node is allowed to transmit in a single transmit opportunity as specified in 148.4.4.2. Valid range is 0 to 255, inclusive. The default value is 0.;

30.16.1.1.7 aPLCABurstTimer

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

This value sets the maximum number of bit-times PLCA waits for the MAC to send a new packet before yielding the transmit opportunity. See definition in 148.4.4.4. Valid range is 0 to 255, inclusive. The default value is 128.;

30.16.1.2 PLCA device actions

30.16.1.2.1 acPLCAAdminControl

ACTION

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APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:
disabled
enabled

BEHAVIOUR DEFINED AS:

This action provides a means to alter aPLCAAdminState. Setting acPLCAAdminControl to the disabled state sets the variable plca_en to FALSE and disables the PLCA functionality specified in Clause 148. Setting acPLCAAdminControl to the enabled state sets the variable plca_en to TRUE in Figure 148–3, Figure 148–4, Figure 148–5, Figure 148–6, and Figure 148–7.;

30.16.1.2.2 acPLCAReset

ACTION

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:
reset
normal

BEHAVIOUR DEFINED AS:

This action provides a means to reset the PLCA Reconciliation Sublayer functions. See 148.4.4.2.;

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31. MAC Control

31.1 Overview

This clause specifies an optional MAC Control sublayer (MAC Control) for use with the CSMA/CD MAC. MAC Control provides for real-time control and manipulation of MAC sublayer operation. This clause specifies a generalized architecture and protocol for MAC Control. Specific implementations of control functions using this protocol are specified in the normative annexes to this clause. The MAC Control protocol is specified such that it can support new functions to be implemented and added to this standard in the future.

Non-realtime, or quasistatic control (e.g., configuration of MAC operational parameters) is provided by Layer Management.

Operation of the MAC Control sublayer is transparent to the CSMA/CD MAC.

The body of this clause and its associated annexes contain state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram shall prevail. The notation used in the state diagrams follows the conventions of 21.5.

31.2 Layer architecture

The MAC Control sublayer is a client of the CSMA/CD MAC. Figure 31–1 depicts the architectural positioning of the MAC Control sublayer with respect to the CSMA/CD MAC and the MAC Control client. MAC Control clients may include the Bridge Relay Entity, LLC, or other applications.

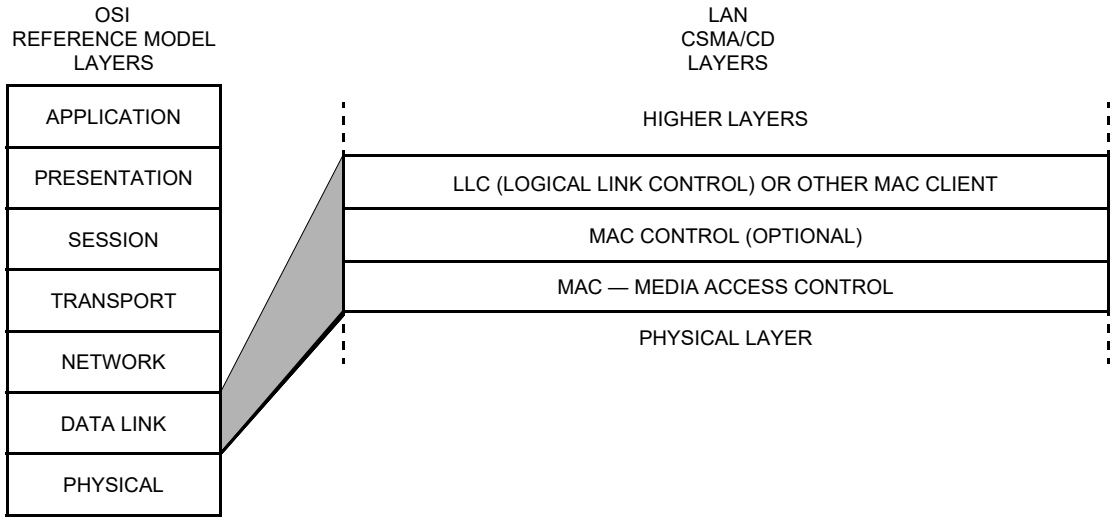

Figure 31–1—Architectural positioning of MAC Control sublayer

31.3 Support by interlayer interfaces

This subclause describes how the MAC Control sublayer uses the MAC service interface specified in Clause 2. The optional MAC Control sublayer is inserted between the MAC sublayer and its MAC client. The MAC Control sublayer uses the MAC service interface to interface to the MAC client and to the MAC.

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Figure 31–2 depicts the usage of interlayer interfaces by the MAC Control sublayer. Devices that implement the MAC Control sublayer shall support the MAC service primitives, MA_CONTROL.request and MA_-CONTROL.indication, as specified in this clause.

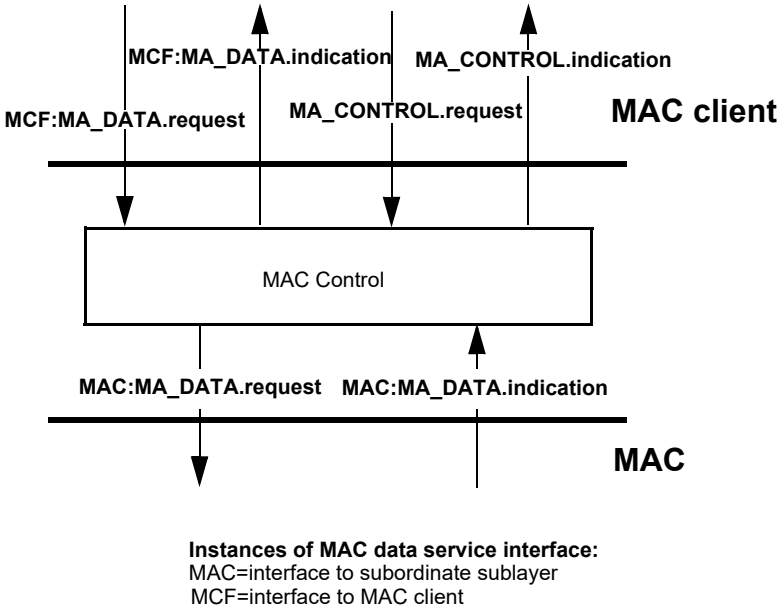

Figure 31–2—MAC Control sublayer support of interlayer service interfaces

Clients of the MAC Control sublayer may generate either MCF:MA_CONTROL.request or MCF:MA_-DATA.request primitives. MA_CONTROL.request primitives generated by MAC clients are interpreted by the MAC Control sublayer, and may result in the generation of MAC:MA_DATA.request calls to the MAC sublayer, or other actions as necessary to support the requested MAC Control sublayer function. Based upon the state of the MAC Control sublayer, MCF:MA_DATA.request primitives may cause the immediate generation of a MAC:MA_DATA.request call to the MAC sublayer, or be delayed, discarded, or modified in order to perform the requested MAC Control function.

All MAC frames validly received by the CSMA/CD MAC are passed to the MAC Control sublayer for interpretation. If the MAC frame is destined for the MAC client, the MAC Control sublayer generates an MCF:MA_DATA.indication primitive, providing complete transparency for normal data exchange between MAC clients. If the MAC frame is destined for the MAC Control sublayer entity, it is interpreted and acted on internal to the MAC Control sublayer. This may result in state changes within the MAC Control sublayer, the generation of MA_CONTROL.indication primitives, or other actions as necessary to support the MAC Control sublayer function. MAC Control sublayer functions shall always sink MAC Control frames.

In the MAC:MA_DATA.indication primitive, MAC frames destined for the MAC Control sublayer (MAC Control frames) are distinguished from MAC frames destined for MAC clients by a unique Length/Type field identifier.

The MAC Control sublayer generates MA_CONTROL.indication primitives to its client, signaling the current value of internal state variables. Each MAC Control function implemented may have its own function-specific state indications.

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31.3.1 MA_CONTROL.request

Implementation of the MA_CONTROL.request primitive is mandatory.

31.3.1.1 Function

This primitive defines the transfer of control commands from a MAC client entity to the local MAC Control sublayer entity.

31.3.1.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
MA_CONTROL.request      (
                        destination_address,
                        opcode,
                        request_operand_list
                        )
```

The destination_address parameter may specify either an individual or a group MAC entity address. It has to contain sufficient information to create the DA field that is prepended to the MAC frame by the local MAC sublayer entity. The opcode specifies the control operation requested by the MAC client entity. The request_operand_list is an opcode-specific set of parameters.

The valid opcodes and their respective meanings are defined in Annex 31A.

31.3.1.3 When generated

This primitive is generated by a MAC client whenever it wishes to use the services of the optional MAC Control sublayer entity.

31.3.1.4 Effect of receipt

The effect of receipt of this primitive by the MAC Control sublayer is opcode-specific. (See Annex 31A.)

31.3.2 MA_CONTROL.indication

Implementation of the MA_CONTROL.indication primitive is mandatory.

31.3.2.1 Function

This primitive defines the transfer of control status indications from the MAC Control sublayer entity to the MAC client entity.

31.3.2.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
MA_CONTROL.indication       (
                            opcode,
                            indication_operand_list
                            )
```

The elements of the indication_operand_list are opcode-specific, and specified in Annex 31A.

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31.3.2.3 When generated

The MA_CONTROL.indication is generated by the MAC Control sublayer under conditions specific to each MAC Control operation.

31.3.2.4 Effect of receipt

The effect of receipt of this primitive by the MAC client is not specified in this clause. See the list of MAC control functions in Annex 31A.

31.4 MAC Control frames

MAC Control frames comprise MAC client data for the CSMA/CD MAC, as specified in Clause 3. They are encapsulated by the CSMA/CD MAC; that is, they are prepended by a Preamble and Start-of-Frame delimiter and appended by an FCS.

MAC Control frames are distinguished from other MAC frames only by their Length/Type field identifier.

31.4.1 MAC Control frame format

For any particular implementation of this standard, MAC Control frames are fixed length, containing minFrameSize–32 bits. The underlying MAC prepends the Preamble and Start-of-Frame delimiter fields, and appends the FCS. Figure 31–3 depicts the MAC Control frame format.

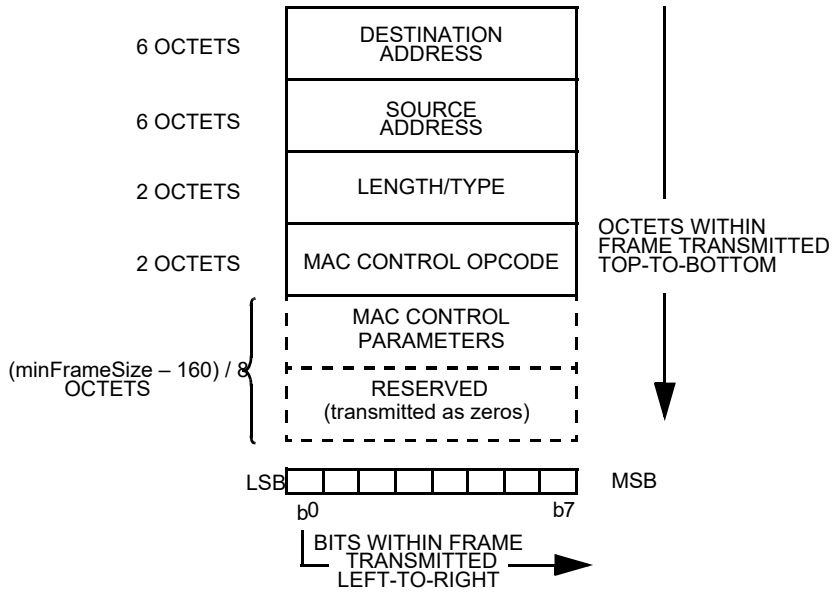

Figure 31–3—MAC Control frame format

31.4.1.1 Destination Address field

The Destination Address field of a MAC Control frame contains the 48-bit address of the station(s) for which the frame is intended. It may be an individual or multicast (including broadcast) address. Permitted values for the Destination Address field may be specified separately for each MAC Control opcode in the annexes to Clause 31.

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31.4.1.2 Source Address field

The Source Address field of a MAC Control frame contains the 48-bit individual address of the station sending the frame.

31.4.1.3 Length/Type field

The Length/Type field of a MAC Control frame is a 2-octet field that shall contain the hexadecimal value: 88-08. This value carries the EtherType interpretation (see 3.2.6), and has been universally assigned for MAC Control of CSMA/CD LANs.

31.4.1.4 MAC Control Opcode field

The MAC Control Opcode field shall contain a 2-octet operation code indicating the MAC Control function. It defines the semantics of the MAC Control Parameters field specified in 31.4.1.5. Annex 31A contains the list of defined MAC Control opcodes and interpretations.

A MAC Control frame shall contain exactly one MAC Control opcode.

31.4.1.5 MAC Control Parameters field

The MAC Control Parameters field shall contain MAC Control opcode-specific parameters. This field may contain none, one, or more parameters as defined by the MAC Control Opcode. The opcode-specific semantics of the MAC Control Parameters field are defined in the normative annex specifying each MAC Control function.

The MAC Control Parameters field shall contain an integral number of octets. The length of the MAC Control Parameters field varies from a minimum of zero, to a maximum of minFrameSize –160 bits. See 4.2.3.3 for a discussion of minFrameSize.

31.4.1.6 Reserved field

The Reserved field is used when the MAC Control parameters do not fill the fixed length MAC Control frame. The size of the Reserved field, if any, is determined by the size of the MAC Control Parameters field supplied by MAC Control and the minimum frame size parameter of the particular implementation.

The length of Reserved field required for a MAC Control Parameters field that is n octets long is [minFrameSize – $(8 \times n + 160)$] bits. See 4.2.3.3 for a discussion of minFrameSize. The Reserved field is transmitted as all zeros.

31.5 Opcode-independent MAC Control sublayer operation

The MAC passes to the MAC Control sublayer all valid MAC frames via the MA_DATA.indication primitive. Invalid MAC frames are not passed to the MAC Control sublayer (see 3.4).

31.5.1 Frame parsing and data frame reception

Upon receipt, the MAC Control sublayer parses the incoming MAC frame to determine whether it is destined for the MAC client (data frame) or for a specific function within the MAC Control sublayer entity itself (MAC Control frame). MAC Control frames with a length of minFrameSize and a supported opcode field are interpreted and acted upon by the MAC Control sublayer.

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A MAC frame that does not contain the unique Length/Type field specified in 31.4.1.3 is a data frame. The receipt of a data frame results in the generation of a MCF:MA_DATA.indication primitive by the MAC Control sublayer, with its parameters identical to the MAC:MA_DATA.indication primitive.

NOTE—For Length/Type field values in the range between maxBasicDataSize and minTypeValue, the behavior of the RemovePad function in the underlying MAC sublayer is unspecified. Frames with Length/Type field values in this range may or may not be passed up by the MAC sublayer.

MAC Control frames with a length greater than minFrameSize and a supported opcode field may be either discarded, or truncated to minFrameSize, interpreted, and acted upon. Unsupported MAC Control frames are discarded. Discarded frames are neither interpreted nor acted upon by the MAC Control sublayer.

31.5.2 Control frame reception

Validly received MAC Control frames are further parsed to determine the opcode. The location of the opcode within a valid MAC Control frame and its format are specified in 31.4.1.4 and Figure 31–3. If the MAC Control sublayer entity supports the function requested by the specified opcode, it interprets and acts upon the MAC Control frame in an opcode- and request_operand-specific manner. (See Annex 31A.) This action may change the state of the MAC Control sublayer, affecting its behavior with respect to data transmission requests by the MAC client, future control frame receptions, or control indications to the MAC client.

If the MAC Control sublayer entity does not support the function requested by the specified opcode, it discards the MAC Control frame. The discard of a frame in this manner may be reported to network management.

31.5.3 Opcode-independent MAC Control receive state diagram

The MAC Control sublayer shall implement the Receive state diagram specified in this subclause.

31.5.3.1 Constants

802.3_MAC_Control
: The 16-bit Length/Type field value used for CSMA/CD MAC Control, specified in 31.4.1.3.

31.5.3.2 Variables

receiveEnabled
: A Boolean set by Network Management to indicate that the station is permitted to receive from the network.

  Values: true; Receiver is enabled by management
  false; Receiver is disabled by management

DA
: The destination address field parsed from the received frame.

SA
: The source address field parsed from the received frame.

lengthOrType
: The lengthOrType field parsed from the received frame.

data
: The data payload field parsed from the received frame.

fcs
: The fcs field parsed from the received frame.

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fcsPresent
: A Boolean set by the MAC sublayer. See 4.3.2.

mac_service_data_unit
: The concatenation of lengthOrType, data.

ReceiveStatus
: Indicates the status of the received frame. See 4.3.2.

opcode
: The MAC Control opcode field parsed from the received frame.

31.5.3.3 Messages

MA_DATA.indication

The service primitive used to pass a validly received MAC frame between the MAC and the MAC Control sublayers, or between the MAC Control sublayer and the MAC client. When generated by the MAC sublayer, this message is used by the MAC Control Receive state diagram as the condition for transition between WAIT FOR RX and CHECK TYPE states. While in the PASS TO CLIENT state, the MAC Control Receive state diagram generates this message to the MAC client.

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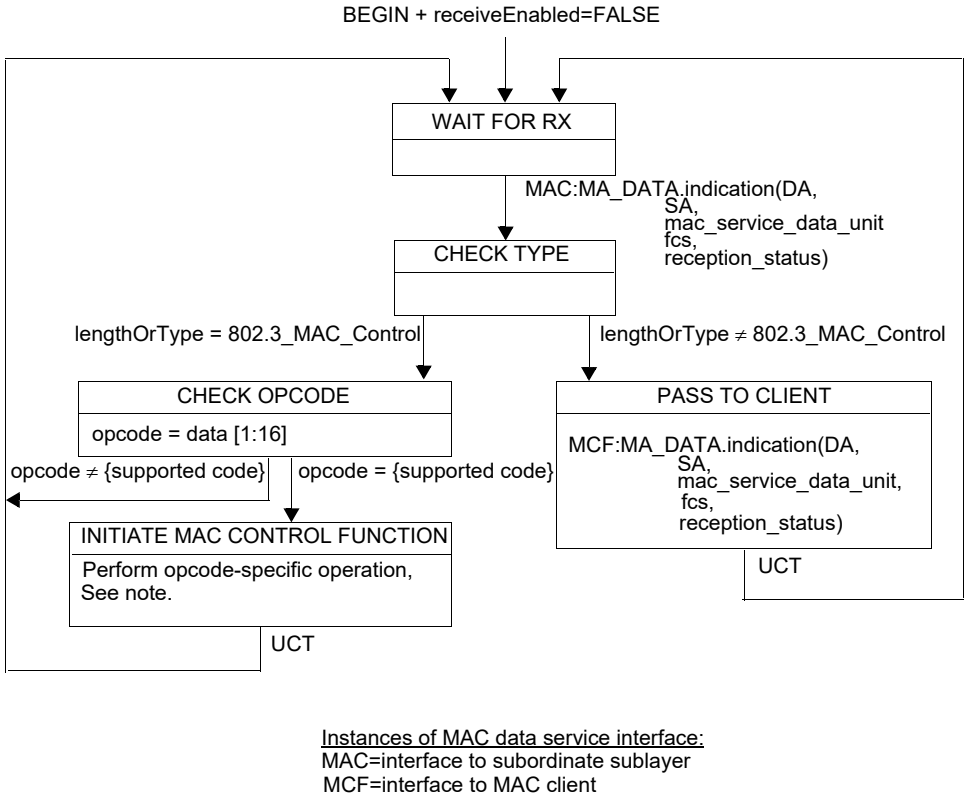
31.5.3.4 Opcode-independent MAC Control Receive state diagram



NOTE—The opcode-specific operation (see Annex 31A) is launched as a parallel process by the MAC Control sublayer, and not as a synchronous function. Progress of the generic MAC Control Receive state diagram (as shown in this figure) is not implicitly impeded by the launching of the opcode-specific function.

Figure 31–4—Generic MAC Control Receive state diagram

The functions performed in the INITIATE MAC CONTROL FUNCTION state are opcode-specific (see Annex 31A).

31.6 Compatibility requirements

An instantiation of the MAC Control sublayer is not required to implement all valid control functions specified in Annex 31A.

31.7 MAC Control client behavior

The MAC Control sublayer uses the services of the underlying connectionless-mode MAC sublayer to exchange both Data and Control frames. The MAC Control sublayer does not provide any mechanism for recovery from lost, discarded, damaged, or delayed frames. It is the responsibility of the MAC Control client to implement mechanisms for dealing with lost, discarded, damaged, and delayed frames, if necessary.

Since implementation of the MAC Control sublayer is optional, a MAC Control client cannot assume the existence of a MAC Control sublayer entity in a peer DTE.

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31.8 Protocol implementation conformance statement (PICS) proforma for Clause 31, MAC Control[64]

31.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 31, the optional MAC Control sublayer, shall complete the following PICS proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

31.8.2 Identification

31.8.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations, other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

31.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 31, MAC Control
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[64] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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31.8.3 PICS proforma for MAC Control frames

31.8.3.1 Support by interlayer interfaces

Item	Feature	Subclause	Value/Comment	Status	Support
SI1	Support for MAC service primitives, MA_-CONTROL.request and MA_CON-TROL.indication	31.3	Required	M	Yes [ ]

31.8.3.2 MAC Control frame format

Item	Feature	Subclause	Value/Comment	Status	Support
FF1	Length/Type field	31.4.1.3	2-octet field containing 88-08	M	Yes [ ]
FF2	MAC Control opcode	31.4.1.4	2-octet operation code	M	Yes [ ]
FF3	Number of opcodes	31.4.1.4	1	M	Yes [ ]
FF4	MAC Control parameters	31.4.1.5	MAC Control Parameter field as described	M	Yes [ ]

31.8.3.3 Opcode-independent MAC Control sublayer operation

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Generic MAC Control receive state diagram	31.5.3	Meets requirements of Figure 31–4	M	Yes [ ]
SD2	MAC Control frame action	31.3	Sink MAC Control frames	M	Yes [ ]

31.8.3.4 Control opcode assignments

Item	Feature	Subclause	Value/Comment	Status	Support
COA1	Opcode values and interpretations	31A	Reserved opcodes not used	M	Yes [ ]

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32. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2

NOTE—This PHY is not recommended for new installations. Since September 2003, maintenance changes are no longer being considered for this clause.

32.1 Overview

The 100BASE-T2 PHY is one of the 100BASE-T family of high-speed CSMA/CD network specifications. The 100BASE-T2 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and baseband medium specifications are aimed at users who want 100 Mb/s performance over basic data grade Category 3 twisted-pair cabling systems. 100BASE-T2 signaling requires two pairs of Category 3 cabling, or cabling with better transfer characteristics than Category 3, installed according to ISO/IEC 11801, as specified in 32.7. This type of cabling, and the connectors used with it, are simple to install and reconfigure.

This clause defines the type 100BASE-T2 PCS, type 100BASE-T2 PMA sublayer, and type 100BASE-T2 Medium Dependent Interface (MDI). Together, the PCS and the PMA sublayer comprise a 100BASE-T2 Physical Layer device (PHY). Control actions needed for correct PHY operations are specified by the 100BASE-T2 PHY Control function. Provided in this document are full functional, electrical, and mechanical specifications for the type 100BASE-T2 PHY Control function, PCS, PMA, and MDI. This clause also specifies the baseband medium used with 100BASE-T2.

The objectives of 100BASE-T2 are as follows:

a) To support the CSMA/CD MAC;

b) To support the 100BASE-T Media Independent Interface (MII), repeater, and Auto-Negotiation;

c) To support full duplex operations (Clause 31);

d) To provide 100 Mb/s data rate at the MII;

e) To provide for operating over two pairs of Category 3, 4, or 5 balanced twisted-pair cabling systems installed in accordance with ISO/IEC 11801, as specified in 32.7, at distances up to 100 m;

f) To support operation of other applications on adjacent pairs;

g) To allow for a nominal network extent of 200 m including

   1) Balanced cabling links of 100 m to support both half duplex and full duplex operation and

   2) Two-repeater networks of approximately 200 m span;

h) To provide a communication channel with a symbol error ratio of less than one part in 10^{10} at the PMA service interface.

32.1.1 Relation of 100BASE-T2 to other standards

Relations between the 100BASE-T2 PHY and the ISO/IEC Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model are shown in Figure 32–1. The PHY layers shown in Figure 32–1 connect one Clause 4 Media Access Control (MAC) layer to a Clause 27 repeater. This clause also discusses other variations of the basic configuration shown in Figure 32–1. This whole clause builds on Clauses 1, 2, 3, 4, 21, 22, 27, 28, 29, and 30 of this standard.

32.1.2 Operation of 100BASE-T2

The 100BASE-T2 PHY employs dual-duplex baseband transmission over two wire pairs BI_DA and BI_DB, whereby the aggregate data rate of 100 Mb/s is achieved by transmission at a modulation rate of

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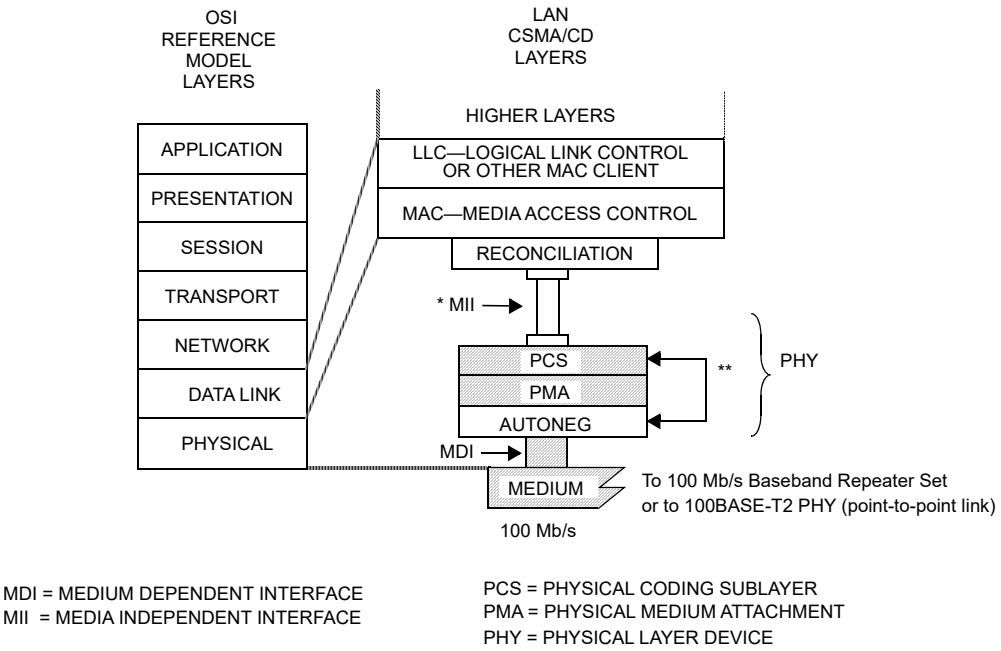

NOTE 1—* MII is optional.

NOTE 2—** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indication.

Figure 32–1—Type 100BASE-T2 PHY relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

25 MBd over each wire pair in each direction simultaneously (full duplex transmission), as shown in Figure 32–2. Transmitted symbols are selected from the two-dimensional 5 × 5 symbol constellation illustrated in Figure 32–3. Redundancy in the 5 × 5 constellation allows specific encoding rules to be employed to represent MII data streams, an idle mode or control signals as sequences of two-dimensional symbols. Each two-dimensional symbol can be viewed as a pair (A_n, B_n) of one-dimensional quinary symbols taken from the set {–2, –1, 0, +1, +2}. Five-level Pulse Amplitude Modulation is employed for transmission over each wire pair (PAM 5 × 5). The modulation rate of 25 MBd matches the MII clock rate of 25 MHz. The corresponding symbol period is 40 ns. This specification permits the use of Category 3, 4, or 5 balanced cabling, installed according to ISO/IEC 11801, as defined in 32.7.

A 100BASE-T2 PHY can be configured either as a *master* PHY or as a *slave* PHY. The master-slave relationship between two stations sharing a link segment is established during Auto-Negotiation (see Clause 28, 32.5, Annex 28C, and 32.5.2). The master PHY uses an external clock to determine the timing of transmitter and receiver operations. The slave PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in Figure 32–2. In a DTE to repeater connection, the repeater is typically set to be master and the DTE is typically set to be slave.

The following subclauses summarize the PCS, PMA, and PHY Control sections of this document. Figure 32–4 shows the division of responsibilities between the PCS, the PMA sublayer, and the PHY Control function.

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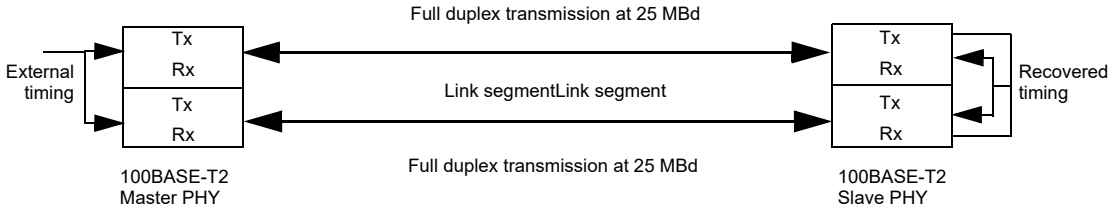

Figure 32–2—100BASE-T2 topology

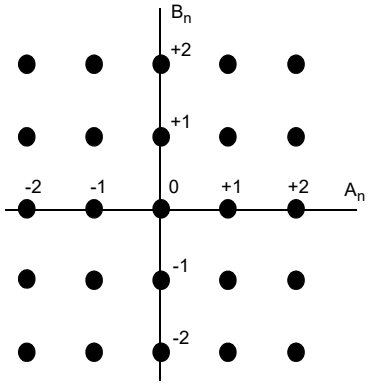

Figure 32–3—PAM5×5 symbol constellation

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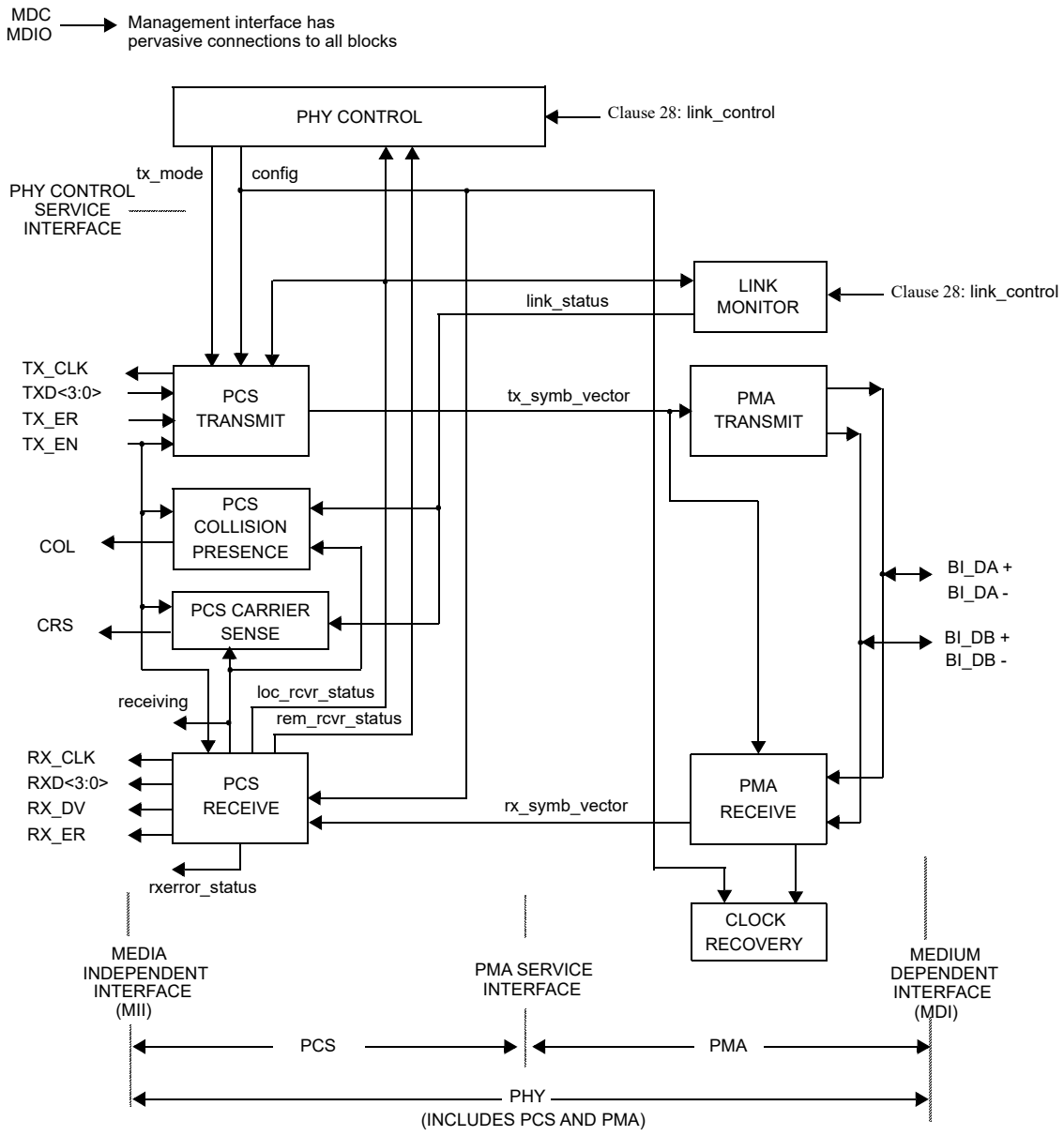

Figure 32–4—Division of responsibilities between 100BASE-T2 PCS, PMA, and PHY Control

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32.1.2.1 Physical coding sublayer (PCS)

The 100BASE-T2 PCS couples an MII, as described in Clause 22, to a PMA sublayer.

The functions performed by the PCS comprise the generation of continuous quinary symbol sequences to be transmitted over each wire pair. During *data mode*, i.e., when a data stream from the MII is transmitted, the four bits representing the TXD<3:0> data nibble are scrambled by a side-stream scrambler and encoded into a pair of quinary symbols. During *idle mode*, i.e., between transmission of consecutive data streams, the sequences of quinary symbols are generated with an encoding rule that differs from the encoding rule used in data mode. Through this technique, sequences of arbitrary quinary symbols that represent data can easily be distinguished from sequences that represent the idle mode. Furthermore, idle mode encoding takes into account the information of whether the local PHY is operating reliably or not and allows conveying this information to the remote station. A transition from the idle to the data mode is signaled by inserting a Start-of-Stream delimiter that consists of a pattern of two consecutive pairs of quinary symbols. Similarly, the end of a data stream transmission is signaled by inserting an End-of-Stream delimiter that also consists of a pattern of two consecutive pairs of quinary symbols. Further patterns are used for signaling a transmit error during transmission of a data stream.

PCS Receive processes pairs of quinary symbols provided by the PMA. It detects the beginning and the end of streams of data and, during the reception of a data stream, descrambles and decodes the received quinary symbol pairs into nibbles RXD<3:0> that are passed to the MII. PCS Receive also detects errors in the received sequences and signals them to the MII. Furthermore, the PCS contains a PCS Carrier Sense function, a PCS Collision Presence function, and a management interface.

The PCS functions and state diagrams are specified in 32.3. The signals provided by the PCS at the MII conform to the interface requirements of Clause 22. The PCS interfaces to PHY Control and to the PMA are abstract message-passing interfaces specified in 32.2 and 32.4, respectively.

32.1.2.2 PMA sublayer

The PMA couples messages from the PMA service interface onto the balanced cabling physical medium. The PMA provides dual-duplex communications at 25 MBd over two pairs of balanced cabling up to 100 m in length.

The PMA Transmit function comprises two independent transmitters to generate five-level pulse-amplitude modulated signals on each of the two pairs BI_DA and BI_DB, as described in 32.4.1.1.2.

The PMA Receive function comprises two independent receivers for five-level pulse-amplitude modulated signals on each of the two pairs BI_DA and BI_DB, as described in 32.4.1.1.3. The receivers are responsible for acquiring clock, and providing quinary symbol pairs to the PCS as defined by the PMA_UNITDATA.indication message. The PMA also contains functions for Link Monitor.

PMA functions and state diagrams are specified in 32.4. PMA electrical specifications are given in 32.6.

32.1.2.3 PHY Control function

PCS and PMA sublayer operations are controlled via signals generated by the PHY Control function. PHY Control does not itself represent a sublayer but rather a logical grouping of the control functions necessary for proper operations of a 100BASE-T2 transceiver.

PHY Control determines whether the PHY should operate in a normal state, where packets can be exchanged over the link segment, or whether the PHY should be forced to send quinary symbol sequences that represent the idle mode. The latter occurs when either one of the PHYs, or both PHYs, that share a link segment are not operating reliably.

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The PHY Control function and state diagram are specified in 32.2, prior to introducing the PCS and PMA functional specifications. The PHY Control interface to the PCS and PMA sublayer is an abstract message-passing interface also specified in 32.2.

32.1.3 Application of 100BASE-T2

32.1.3.1 Compatibility considerations

All implementations of the balanced cabling link shall be compatible at the MDI. The PCS, PMA, and the medium are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided the MDI and MII specifications are met.

32.1.3.2 Incorporating the 100BASE-T2 PHY into a DTE

When the PHY is incorporated within the physical bounds of a DTE, conformance to the MII is optional, provided that the observable behavior of the resulting system is identical to that of a system with a full MII implementation. For example, an integrated PHY may incorporate an interface between PCS and MAC that is logically equivalent to the MII, but does not have the full output current drive capability called for in the MII specification.

32.1.3.3 Use of 100BASE-T2 PHY for point-to-point communication

The 100BASE-T2 PHY, in conjunction with the MAC specified in Clause 1 through Clause 4 (including parameterized values in 4.4.2 to support 100 Mb/s operation) may be used at both ends of a link for point-to-point applications between two DTEs. Such a configuration does not require a repeater. In this case each PHY may connect through an MII to its respective DTE. Optionally, either PHY (or both PHYs) may be incorporated into the DTEs without an exposed MII.

32.1.3.4 Auto-Negotiation requirement

Full Auto-Negotiation, as specified in Clause 28, shall be included in all compliant implementations.

32.1.4 State diagram conventions

The body of this clause and its associated annexes contain state diagrams, including definitions of variables, constants and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram shall prevail. The notation used in the state diagrams follows the conventions of 21.5.

32.2 PHY Control functional specifications and service interface

32.2.1 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY in a mode of operation during which packets can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 32–5.

During Auto-Negotiation, PHY Control ensures that the transmitter is disabled. When the Auto-Negotiation process asserts link_control=ENABLE, PHY Control enters the TRAINING state. During training, PHY Control enforces transmission in the idle mode by setting tx_mode=SEND_I and the PHY transmits sequences of quinary symbols encoded with the parameter loc_rcvr_status=NOT_OK. When the PHY achieves successful training and establishes proper receiver operations, PCS Receive asserts the parameter loc_rcvr_status=OK, and PCS Transmit conveys this information to the link partner via idle transmission.

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The criterion for assertion of the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver or detecting errors during reception of symbol streams that represent the idle mode. Upon observation that the remote PHY also operates reliably (rem_rcvr_status=OK), the normal mode of operation is entered where transmission of packets over the link segment can take place.

The normal mode of operation corresponds to the SEND IDLE OR DATA state, where PHY Control asserts tx_mode=SEND_N. In this state, when no packets have to be sent, idle mode transmission takes place. Encoding of quinary symbols is realized with the parameter loc_rcvr_status = OK.

If during the normal mode of operation unsatisfactory receiver operations is detected (loc_rcvr_status=NOT_OK), transmission of the current packet, if any, is completed and PHY Control enters the TRAINING state.

Whenever a PHY that operates reliably detects unsatisfactory operation of the remote PHY (rem_rcvr_status=NOT_OK), it enters the SEND IDLE state where tx_mode=SEND_I is asserted and idle transmission takes place. In this state, encoding is performed with the parameter loc_rcvr_status=OK. As soon as the remote PHY signals satisfactory receiver operation (rem_rcvr_status=OK), the SEND IDLE OR DATA state is entered. Note that if in the SEND IDLE state loc_rcvr_status takes the value NOT_OK transition to the TRAINING state occurs.

PHY Control may force the transmit scrambler state to be initialized to a random value by requesting the execution of the PCS Reset function defined in 32.3.1.1.

32.2.2 PHY Control Service interface

The following specifies the services provided by PHY Control. These services are described in an abstract manner and do not imply any particular implementation.

The following primitives are defined:

PHYC_CONFIG.indication
PHYC_TXMODE.indication
PHYC_RXSTATUS.request
PHYC_REMRXSTATUS.request

The parameter link_control is identical to the link_control parameter defined for the PMA Service interface in 32.4.2.4.

32.2.2.1 PHYC_CONFIG.indication

Each PHY in a 100BASE-T2 link is configured as a master PHY or as a slave PHY. Master/slave configuration is determined during Auto-Negotiation (see 32.5). The result of this negotiation is provided to PHY Control.

32.2.2.1.1 Semantics of the primitive

PHYC_CONFIG.indication (config)

PHYC_CONFIG.indication specifies to PCS and PMA Clock Recovery via the parameter config whether the PHY operates as a master PHY or as a slave PHY. The parameter config can take on one of two values of the form:

MASTER This value is continuously asserted when the PHY operates as a master PHY.

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SLAVE This value is continuously asserted when the PHY operates as a slave PHY.

32.2.2.1.2 When generated

PHY Control shall generate PHYC_CONFIG.indication messages synchronously with every MII TX_CLK cycle.

32.2.2.1.3 Effect of receipt

Upon reception of this primitive, PCS and PMA Clock Recovery shall perform their functions in master or slave configuration according to the value assumed by the parameter config.

32.2.2.2 PHYC_TXMODE.indication

The transmitter in a 100BASE-T2 link normally sends over the two pairs quinary symbols that can represent an MII data stream or the idle mode.

32.2.2.2.1 Semantics of the primitive

PHYC_TXMODE.indication (tx_mode)

PHYC_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of quinary symbols the PCS should be transmitting. The parameter tx_mode can take on one of two values of the form:

SEND_N This value is continuously asserted when transmission of sequences of quinary symbols representing an MII data stream or the idle mode is to take place.

SEND_I This value is continuously asserted in case transmission of sequences of quinary symbols representing the idle mode is to take place.

32.2.2.2.2 When generated

PHY Control shall generate PHYC_TXMODE.indication messages synchronously with every MII TX_CLK cycle.

32.2.2.2.3 Effect of receipt

Upon receipt of this primitive, the PCS shall perform its Transmit function as described in 32.3.1.2.

32.2.2.3 PHYC_RXSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the receive link for the local PHY. The parameter loc_rcvr_status conveys to PHY Control and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by PCS Transmit encoding functions.

32.2.2.3.1 Semantics of the primitive

PHYC_RXSTATUS.request (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK This value is asserted and remains true during reliable operation of the receive link for

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the local PHY.

NOT_OK This value is asserted whenever operation of the receive link for the local PHY is unreliable.

32.2.2.3.2 When generated

PCS Receive shall generate PHYC_RXSTATUS.request messages synchronously with signals received at the MDI. It shall prevent that the value of the parameter loc_rcvr_status is modified while TX_EN=1 in order to avoid that a transition from data to idle mode or from idle to data mode occurs while a packet is being presented to the PCS at the MII.

32.2.2.3.3 Effect of receipt

The effect of receipt of this primitive is specified in 32.2.5 and 32.4.1.3.3.

32.2.2.4 PHYC_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link as communicated by the remote PHY. The parameter rem_rcvr_status conveys to PHY Control the information on whether reliable operation of the remote PHY is detected or not.

32.2.2.4.1 Semantics of the primitive

PHYC_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK The receive link for the remote PHY is operating reliably.

NOT_OK Reliable operation of the receive link for the remote PHY is not detected.

32.2.2.4.2 When generated

The PCS shall generate PHYC_REMRXSTATUS.request messages synchronously with signals received at the MDI.

32.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is specified in 32.2.5.

32.2.3 State diagram variables

link_control
: See 32.4.1.3.1.

link_status
: See 32.4.1.3.1.

loc_rcvr_status
: Variable set by the PCS Receive function to indicate correct or incorrect operation of the receive link for the local PHY.

  Values: OK: the receive link for the local PHY is operating reliably,
  NOT_OK: operation of the receive link for the local PHY is not reliable.

pma_reset
: Allows reset of all PMA functions.

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Values: ON and OFF

Set by: PMA Reset

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not.

Values: OK: the receive link for the remote PHY is operating reliably,
NOT_OK: reliable operation of the receive link for the remote PHY is not detected.

tx_mode

PCS Transmit shall send quinary symbols according to the value assumed by this variable.

Values: SEND_N: transmission of sequences of quinary symbols representing an MII data stream, the idle mode, or control signals shall take place,
SEND_I: transmission of sequences of quinary symbols representing the idle mode shall take place.

32.2.4 State diagram timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where “stop x_timer” is asserted.

maxwait_timer

A timer used to measure the amount of time during which a receiver dwells in the TRAINING state. The timer shall expire 2500 ms to 3000 ms after entering the TRAINING state.

minwait_timer

A timer used to measure the amount of time during which a receiver waits in the SEND IDLE OR DATA, the TRAINING, or the SEND IDLE state before being allowed to leave the current state. The timer shall expire 128T = 5.12 μs after being started.

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32.2.5 PHY Control state diagram

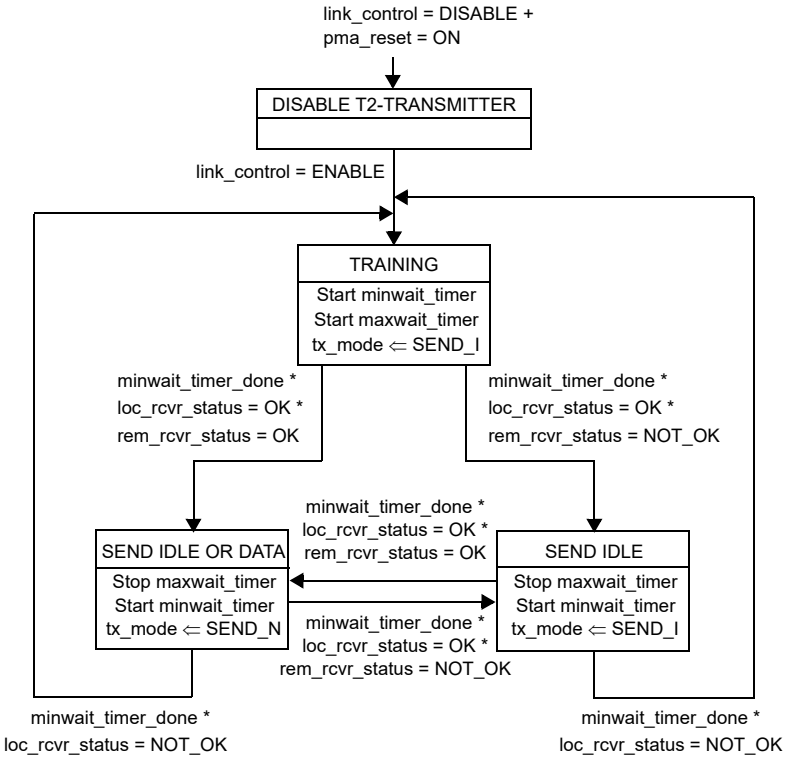

Figure 32–5—PHY Control state diagram

32.3 PCS functional specifications

The PCS comprises one PCS Reset function and four simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit, PCS Receive, PCS Carrier Sense, and PCS Collision Presence. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 32–5, shows how the four operating functions relate to the messages of the PCS-PMA and the PCS-PHY Control interfaces. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive, and are not shown in Figure 32–5. The management functions are specified in Clause 30. See also Figure 32–7, which presents a block diagram helpful for understanding the definitions of PCS Transmit function variables, and Figure 32–11, which defines the structure of frames passed from PCS to PMA.

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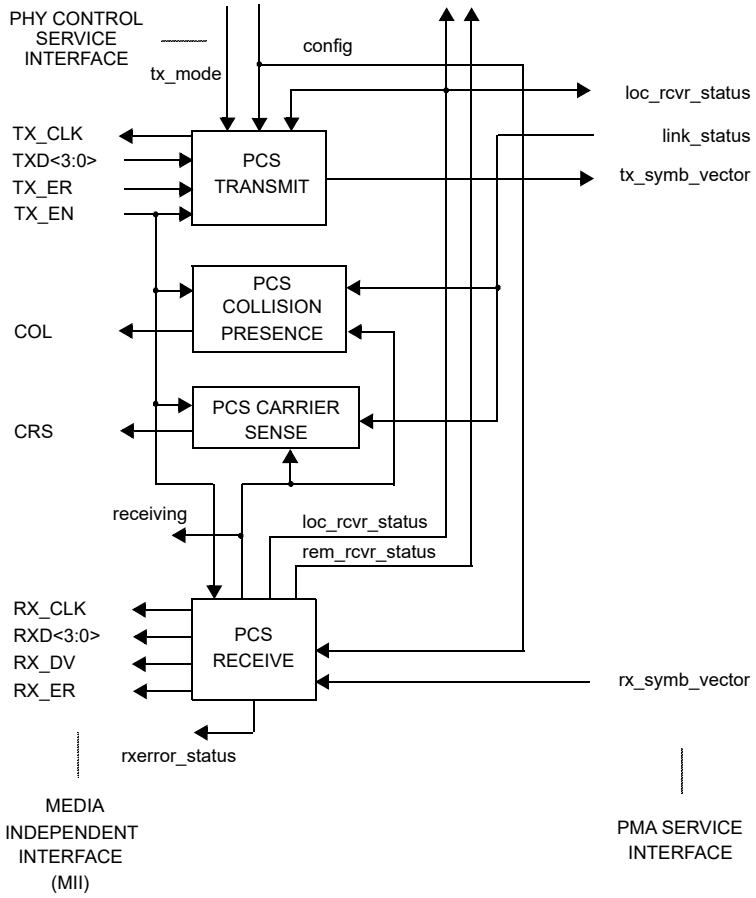

Figure 32-6—PCS reference diagram

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32.3.1 PCS functions

32.3.1.1 PCS Reset function

The PCS Reset function shall be executed any time one of three conditions occurs. These three conditions are “power on,” the receipt of a request for reset from the management entity, and the receipt of a request for reset from PHY Control. PCS Reset initializes all PCS functions. PCS Reset sets pcs_reset = ON for the duration of its Reset function. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

32.3.1.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 32–12.

In normal mode of operation, the tx_mode parameter, which is transferred from PHY Control to the PCS via the PHYC_TXMODE.indication message, assumes the value tx_mode=SEND_N, and the PCS Transmit function generates at each symbol period pairs of quinary symbols that represent data or the idle mode. A symbol period T is equal to 40 ns. A time index n, where n is an integer, is introduced to establish a temporal relationship between different symbol periods. The tx_symb_vector parameter at time n is a two-element vector of quinary symbols (A_n, B_n) that is transferred to the PMA via PMA_UNITDATA.request. The PMA shall transmit symbols A_n and B_n over wire pairs BI_DA and BI_DB, respectively. During transmission of data, the four bits representing the TXD<3:0> data nibble are scrambled by the OCS using a side-stream scrambler then encoded into a pair of quinary symbols and transferred to the PMA. The idle mode is signaled by a sequence of pairs of quinary symbols that are also generated using the side-stream transmit scrambler. However, the encoding rules by which the quinary symbols are obtained are different for the data and the idle modes. This allows, at the receiver, sequences of quinary symbol pairs that represent data to be distinguished from sequences of quinary symbol pairs that represent the idle mode. A transition from the idle mode to the data mode is signalled by inserting a Start-of-Stream delimiter that consists of a pattern of two consecutive pairs of quinary symbols. Similarly, the end of transmission of data is signalled by an End-of-Stream delimiter that also consists of a pattern of two consecutive pairs of quinary symbols. Further patterns are used for signaling the assertion of TX_ER within a stream of data.

If tx_mode = SEND_I is asserted, PCS Transmit generates sequences of symbol pairs (A_n, B_n) according to the encoding rule in idle mode. Idle mode encoding takes into account the value of the parameter loc_rcvr_status. By this mechanism, a PHY indicates during idle transmission the status of its own receiver to the link partner.

The PCS Transmit reference diagram is shown in Figure 32–7. PCS encoding involves the generation of the three-bit words Sa_n[2:0], Sb_n[2:0], Ta_n[2:0], and Tb_n[2:0], from which the pairs of quinary symbols (A_n, B_n) are obtained. The three-bit words Sa_n[2:0] and Sb_n[2:0] are determined first, as explained in 32.3.1.2.2, from sequences of random binary symbols derived from the transmit side-stream scrambler. The generation of Ta_n[2:0] and Tb_n[2:0] and the quinary symbols A_n and B_n is given in 32.3.1.2.3. The physical structure represented in Figure 32–7 is not required. Implementers are free to construct any logical devices having functionality identical to that described by the following specifications and the PCS Transmit state diagram.

32.3.1.2.1 Side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PHY Control function via the PHYC_CONFIG.indication message assumes the value MASTER, PCS Transmit shall employ

$$g_M(x) = 1 + x^{13} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. If config = SLAVE, PCS Transmit shall employ

$$g_S(x) = 1 + x^{20} + x^{33}$$

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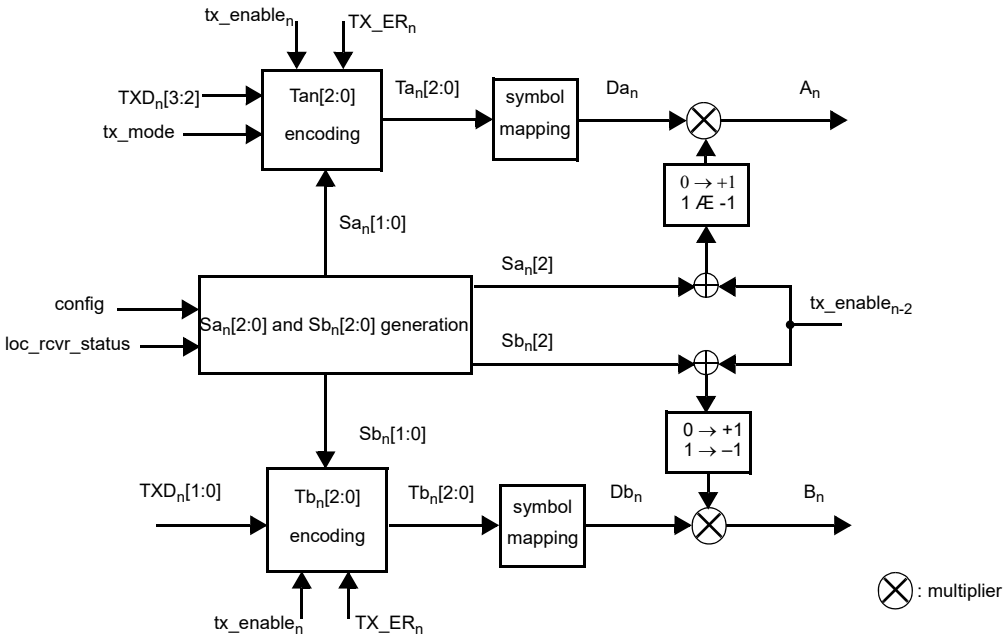
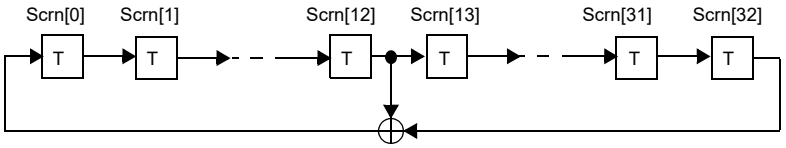
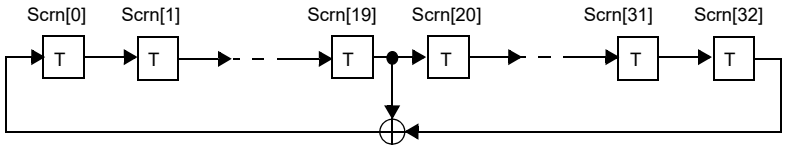


Figure 32–7—PCS Transmit reference diagram

as transmitter side-stream scrambler generator polynomial. The implementation of master and slave PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 32–8. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are randomly set. The generation of the random bits is left to the implementer.



a) Side-stream scrambler employed by the master PHY



b) Side-stream scrambler employed by the slave PHY

Figure 32–8—Realization of side-stream scramblers by linear feedback shift registers

32.3.1.2.2 Generation of bits $Sa_n[2:0]$ and $Sb_n[2:0]$

PCS Transmit encoding rules are based on the generation, at time n, of the four bits Sx_n, Sy_n, $Sa_n[2]$, and $Sb_n[2]$. These four bits are mutually uncorrelated and also uncorrelated with the bit $Scr_n[0]$ in data and idle

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modes. For both master and slave PHYs, they are obtained by the same linear combinations of bits stored in the transmit scrambler shift register delay line. The four bits are elements of the same maximum-length shift register sequence of length $2^{33} - 1$ as $Scr_n[0]$, but shifted in time. The associated delays are all large and different, such that there is no apparent correlation among the five bits $Scr_n[0]$, Sx_n, Sy_n, $Sa_n[2]$, and $Sb_n[2]$. The bits Sx_n and Sy_n are given by

$$Sx_n = Scr_n[3] \oplus Scr_n[8]$$

$$Sy_n = Scr_n[4] \oplus Scr_n[6]$$

where $\oplus$ denotes the XOR logic operator. Four bits $X_n[1:0]$ and $Y_n[1:0]$ are obtained by

$$X_n[0] = \begin{cases} Sx_n & \text{if } \{n - n_0 = 0 \text{ (mod 2) or loc\_rcvr\_status = OK }\} \\ Sx_n \oplus 1 & \text{else} \end{cases}$$

$$X_n[1] = X_n[0] \oplus 1$$

$$Y_n[0] = \begin{cases} Sy_n & \text{if } n - n_0 = 0 \text{ (mod 2)} \\ Sy_{n-1} \oplus 1 & \text{else} \end{cases}$$

$$Y_n[1] = Y_n[0]$$

where n_0 denotes the time index of the last transmitter side-stream scrambler reset.

The bits San[2:0] and Sbn[2:0] are given by

$$Sa_n[2] = Scr_n[1] \oplus Scr_n[5]$$

$$Sa_n[1:0] = \begin{cases} X_n[1:0] & \text{if } Scr_n[0] = 1 \\ Y_n[1:0] & \text{else} \end{cases}$$

$$Sb_n[2] = Scr_n[2] \oplus Scr_n[12]$$

$$Sb_n[1:0] = \begin{cases} Y_n[1:0] & \text{if } Scr_n[0] = 1 \\ X_n[1:0] & \text{else} \end{cases}$$

32.3.1.2.3 Generation of sequences A_n and B_n

If tx_mode = SEND_N, the PCS Transmit function generates sequences A_n and B_n that represent either a stream of data or an idle mode. If tx_mode = SEND_I, idle transmission is enforced. The encoding rule is determined by the value of the signal tx_enable_n, given by

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$$\text{tx\_enable}_n = \begin{cases} TX\_EN_n & \text{if tx\_mode = SEND\_N} \\ 0 & \text{else} \end{cases}$$

where TX_EN_n represents the MII signal TX_EN at time n. If $tx\_enable_n = 1$, transmission of a stream of data takes place. As illustrated in Figure 32–11, the definition of a Start-of-Stream Delimiter ("SSD") is related to the condition $SSD_n = (tx\_enable_n) * (! tx\_enable_{n-2}) = 1$, where "*" and "!" denote the logic AND and NOT operators, respectively. For the generation of "SSD", PCS Transmit replaces the first two nibbles of the preamble in a data stream with the symbols defined below. Similarly, the definition of an End-of-Stream Delimiter (ESD) is related to the condition $ESD_n = (! tx\_enable) * (tx\_enable_{n-2}) = 1$. This occurs during the first two symbol periods after transmission of the last nibble of a data stream.

The symbols A_n and B_n are obtained from the three-bit words $Ta_n[2:0]$ and $Tb_n[2:0]$ whose definitions in the data and the idle modes are given below.

Data mode (tx_enable_n=1):

Definition of "SSD":

$Ta_n[2:0] = [1, 0, 0]$

$Tb_n[2:0] = [!tx\_enable_{n-1}, tx\_enable_{n-2}, tx\_enable_{n-2}]$

A most significant bit $Ta_n[2]=1$ or $Tb_n[2]=1$ results in the transmission of a symbol that can be interpreted as an ESC symbol.

Encoding of data nibbles:

$$Ta_n[2:0] = [0,(Sa_n[1] \oplus TXD_n[3]),(Sa_n[0] \oplus TXD_n[2] \oplus 1)]$$

$$Tb_n[2:0] = [0, (Sb_n[1] \oplus TXD_n[1]),(Sb_n[0] \oplus TXD_n[0] \oplus 1)]$$

where $TXD_n[3:0]$ denotes the data nibble TXD[3:0] at time n.

Encoding of error indication:

If $TX\_ER_n=1$ is asserted, where TX_ER_n denotes the value of the signal TX_ER at time n, error indication is signaled by means of the ESC and 0 symbols. The encoding rule is given by

$$Ta_n[2:0] = [(Sa_n[1] \oplus Sa_n[0]),0,0]$$

$$Tb_n[2:0] = [(Sb_n[1] \oplus Sb_n[0]),0,0]$$

Idle mode (tx_enable_n=0):

Definition of "ESD":

$Ta_n[2:0] = [1, 0, 0]$

$Tb_n[2:0] = [tx\_enable_{n-1}, !tx\_enable_{n-2}, !tx\_enable_{n-2}]$

Encoding in the idle mode:

$$Ta_n[2:0] = [0,Sa_n[1],Sa_n[0]]$$

$$Tb_n[2:0] = [0,Sb_n[1],Sb_n[0]]$$

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The mapping of $Ta_n[2:0]$ and $Tb_n[2:0]$ into quinary symbols Da_n and Db_n is given in Figure 32–9. This mapping ensures that the symbols representing data are Gray coded. The quinary symbols A_n and B_n are obtained from Da_n and Db_n by

Symbol mapping	
Ta/Tb	Da/Db
000	0
001	+1
010	-1
011	-2
100 (ESC)	+2

Idle or data	
Da_n:	0, +1, -1, or -2
Db_n:	0, +1, -1, or -2

Data stream delimiters	
Da_n: ESC	Dan+1: ESC
Db_n: ESC	Dbn+1: 0

Error indication	
Da_n: ESC	Da_n: 0
or	
Db_n: 0	Db_n: ESC

Figure 32–9—Symbol mapping and encoding rule summary

$$A_n = \begin{cases} Da_n & \text{if } \text{Sa}_n[2] \oplus \text{tx\_enable}_{n-2} = 0 \\ -Da_n & \text{else} \end{cases}$$

$$B_n = \begin{cases} Db_n & \text{if } \text{Sb}_n[2] \oplus \text{tx\_enable}_{n-2} = 0 \\ -Db_n & \text{else} \end{cases}$$

With the rules defined in this subclause, if in idle mode a transmitted symbol on one wire pair belongs to the set {–2,0,+2}, the symbol on the other wire pair belongs to the set {–1,+1}. Moreover, one of the quinary symbols that are transmitted at time $2(n–n_0)$ and $2(n–n_0)+1$ is guaranteed to be either +2 or –2. Both in data and idle modes, the symbol sequences on each wire pair can be modeled as sequences of independent and identically distributed quinary symbols. The symbol constellations and symbol probabilities for these two modes are shown in Figure 32–10. The average symbol energy is the same in data and idle modes.

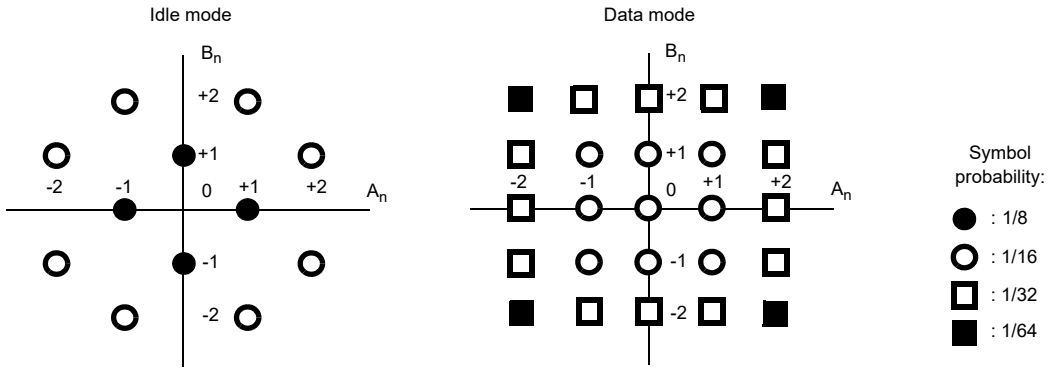

Figure 32–10—Symbol constellations in idle and data modes

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32.3.1.3 PCS Receive function

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 32–13.

The PCS Receive function accepts pairs of detected quinary symbols provided by the PMA Receive function via the parameter rx_symb_vector. To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode. For example, the property that in the idle mode if A_n belongs to the set {–2,0,+2} then B_n belongs to the set {–1,+1}, and vice versa, can be used to acquire the correct state for the receiver side-stream descrambler, and to determine which detected quinary symbol was transmitted on wire pair BI_DA and which on wire pair BI_DB. Also, correct polarity of the detected quinary symbols can reliably be obtained by ensuring in the idle mode that the encoding rule holds whenever a –2 symbol is received. PCS Receive generates the sequence of vectors of two quinary symbols (RA_n, RB_n) and indicates the reliability of receiver operations by setting the parameter loc_rcvr_status to OK (logic high) or NOT_OK (logic low). The sequence (RA_n, RB_n) is processed to generate the signals RXD<3:0>, RX_DV, and RX_ER, which are presented to the MII. PCS Receive detects the transmission of a stream of data from the remote station and conveys this information to the PCS Carrier Sense and PCS Collision Presence functions via the parameter receiving.

32.3.1.3.1 Receiver descrambler polynomials

For side-stream descrambling, the master PHY shall employ the receiver descrambler generator polynomial $g'_M(x) = 1 + x^{20} + x^{33}$, and the slave PHY shall employ the receiver descrambler generator polynomial $g'_S(x) = 1 + x^{13} + x^{33}$.

32.3.1.3.2 Decoding of quinary symbols

At the beginning of a stream of data, PCS Receive detects “SSD” and asserts the signal RX_DV. Detection of “SSD” is achieved by processing two consecutive vectors ($RA_{n–1}$, $RB_{n–1}$) and (RA_n, RB_n) at each time n. Upon detection of “SSD,” PCS Receive also assigns the value TRUE to the parameter receiving that is provided to the PCS Carrier Sense and Collision Presence functions.

Table 32–1 shows the mapping of symbols RA_n and RB_n into two-bit words Qa_n[1:0] and Qb_n[1:0] that are descrambled and decoded to generate nibbles of data RXD[3:0].

Table 32–1—Inverse quinary symbol mapping

RA_n/RB_n	$Qa_n[1:0]/Qb_n[1:0]$
0	00
+1	01 or 10
–1	01 or 10
± 2	11

The mapping shown in Table 32–1 corresponds to the inverse of the encoding function employed by PCS Transmit. For example, a symbol $A_n = +1$ is generated by Ta_n[1:0] being equal to “01” or “10.” Hence, in the above table the value of Qa_n[1:0] for $RA_n = +1$ is specified as being equal to “01 or 10.” Similarly for other entries in the table.

During reception of a stream of data, PCS Receive checks that the symbols RA_n and RB_n follow the encoding rule defined in 32.3.1.2 whenever they assume values ± 2. PCS Receive processes two consecutive vectors at each time n to detect “ESD.” Upon detection of “ESD,” PCS Receive deasserts the signal RX_DV, and assigns the value FALSE to the parameter receiving. If a violation of the encoding rules is detected, PCS

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Receive asserts the signal RX_ER for at least one symbol period. During reception of an idle sequence, PCS Receive checks that the symbols RA_n and RB_n follow the encoding rule defined in 32.3.1.2.

32.3.1.4 PCS Carrier Sense function

The PCS Carrier Sense function shall conform to the PCS Carrier Sense state diagram in Figure 32–14.

The PCS Carrier Sense function controls the MII signal CRS according to the rules presented in this clause. While link_status = OK, CRS is asserted whenever receiving=TRUE or TX_EN=1.

32.3.1.5 PCS Collision Presence function

A PCS collision is defined as the simultaneous occurrence of TX_EN=1 and the assertion of the parameter receiving=TRUE while link_status=OK. While a PCS collision is detected, the MII signal COL shall be asserted. At other times COL shall remain deasserted.

32.3.2 PCS interfaces

32.3.2.1 PCS–MII interface signals

The signals in Table 32–2 are formally defined in 22.2.2. Jabber detection as specified in 22.2.4.2.12 is not required by this standard.

Table 32–2—MII interface signals

Signal name	Meaning	Subclause
TX_CLK	Transmit clock	22.2.2.1
RX_CLK	Receive clock	22.2.2.2
TX_EN	Frames transmit data	22.2.2.3
TXD<3:0>	Transmit data	22.2.2.4
TX_ER	Forces transmission of illegal code	22.2.2.5
RX_DV	Frames receive SFD and DATA	22.2.2.7
RXD<3:0>	Receive data	22.2.2.8
RX_ER	Receive error indication	22.2.2.10
CRS	Non-idle medium indication	22.2.2.11
COL	Collision indication	22.2.2.12
MDC	Management data clock	22.2.2.13
MDIO	Management data	22.2.2.14

32.3.2.2 PCS–management entity signals

The management interface has pervasive connections to all functions. Operation of the management control lines MDC and MDIO, and requirements for managed objects inside the PCS and PMA, are specified in Clause 22 and Clause 30, respectively.

No spurious signals shall be emitted onto the MDI when the PHY is held in power down mode as defined in 22.2.4.1.5, independently of the value of TX_EN, or when released from power down mode, or when external power is first applied to the PHY.

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32.3.3 Frame structure

Frames passed from the PCS to the PMA sublayer shall have the structure shown in Figure 32–11. This figure shows the temporal relationship between the signals tx_enable_n, and TXD[3:0] and the sequences of quinary symbol pairs (A_n, B_n) in correspondence of transitions from the idle mode to transmission of data and vice versa. Time proceeds from left to right in the figure.

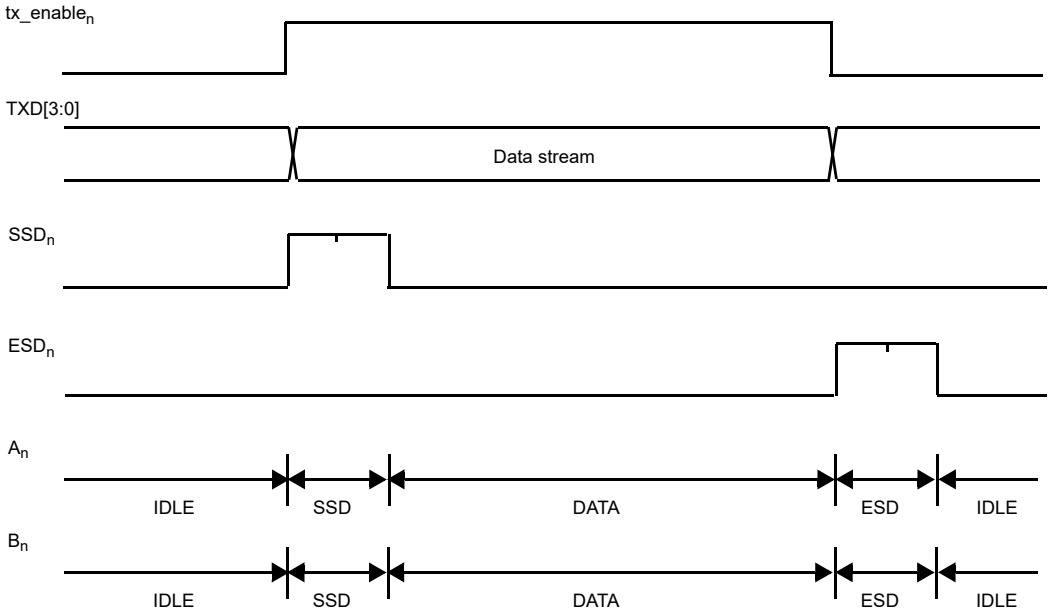

Figure 32–11—PCS sublayer to PMA sublayer frame structure

32.3.4 State variables

32.3.4.1 Variables

COL

The COL signal of the MII as specified in Clause 22.

config

The config parameter set by PHY Control and passed to the PCS via the PHYC_CONFIG.indication primitive.
Values: MASTER and SLAVE.

CRS

The CRS signal of the MII as specified in Clause 22.

DATA

A sequence of vectors of two quinary symbols corresponding to valid data, as specified in 32.3.1.2.

ESD

Two consecutive vectors of two quinary symbols corresponding to the End-of-Stream delimiter, as specified in 32.3.1.2.

IDLE

A sequence of vectors of two quinary symbols generated in idle mode, as specified in 32.3.1.2.

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link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK, READY, and FAIL

loc_rcvr_status

The loc_rcvr_status parameter generated by PCS Receive.
Values: OK and NOT_OK

pcs_reset

The pcs_reset parameter set by the PCS Reset function.
Values: ON and OFF

(RA_n, RB_n)

The vector of the two correctly aligned most recently received quinary symbols generated by PCS Receive.

receiving

The receiving parameter generated by the PCS Receive function.
Values: TRUE and FALSE

rxerror_status

The rxerror_status parameter set by the PCS Receive function. Although this variable is set by PCS Receive, it achieves the same function as the variable rxerror_status of Clause 24 that is set by PMA and communicated through the PMA_RXERROR.indication primitive.
Values: ERROR and NO_ERROR

RX_DV

The RX_DV signal of the MII as specified in Clause 22.

RX_ER

The RX_ER signal of the MII as specified in Clause 22.

rx_symb_vector

A vector of two quinary symbols received by the PMA and passed to the PCS via the PMA_UNITDATA.indication primitive.
Value: SYMB_PAIR

RXD[3:0]

The RXD<3:0> signal of the MII as specified in Clause 22.

SSD

Two consecutive vectors of two quinary symbols corresponding to the Start-of-Stream delimiter, as specified in 32.3.1.2.

tx_enable

The tx_enable parameter generated by PCS Transmit as specified in 32.3.1.2.3.

TX_ER

The TX_ER signal of the MII as specified in Clause 22.

tx_mode

The tx_mode parameter set by PHY Control and passed to the PCS via the

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PHYC_TXMODE.indication primitive.
Values: SEND_N and SEND_I

tx_symb_vector

A vector of two quinary symbols generated by the PCS Transmit function and passed to the PMA via the PMA_UNITDATA.request primitive.
Value: SYMB_PAIR

32.3.4.2 Timer

symb_timer

A continuous free-running timer. The condition symb_timer_done becomes true upon timer expiration.

Restart time: Immediately after expiration; timer restart resets the condition symb_timer_done.

Duration: 40 ns nominal.

TX_CLK shall be generated synchronously with symb_timer (see tolerance required for TX_CLK in 32.6.1.2.6). In the PCS Transmit state diagram, the message PMA_UNITDATA.request is issued concurrently with symb_timer_done.

32.3.4.3 Messages

PMA_UNITDATA.indication (rx_symb_vector)
A signal sent by PMA Receive indicating that a vector of two quinary symbols is available in rx_symb_vector.

PMA_UNITDATA.request (tx_symb_vector)
A signal sent to PMA Transmit indicating that a vector of two quinary symbols is available in tx_symb_vector.

32.3.5 State diagrams

32.3.5.1 PCS Transmit

PCS Transmit sends vectors of two quinary symbols to the PMA via the tx_symb_vector parameter. In normal mode of operation, between streams indicated by the parameter tx_enable, PCS Transmit generates sequences of vectors using the encoding rules defined for the idle mode. Upon assertion of tx_enable, PCS Transmit passes an “SSD” of two consecutive vectors of two quinary symbols to the PMA replacing the preamble bits of a stream of data during these two symbol periods. Following the “SSD,” each TXD<3:0> nibble is encoded into a vector of two quinary symbols until tx_enable is deasserted. If, while tx_enable is asserted, the TX_ER signal is also asserted, PCS Transmit passes to the PMA vectors indicating a transmit error. Note that if the signal TX_ER is asserted while “SSD” is being sent, the transmission of the error condition is delayed until transmission of “SSD” has been completed. Following the deassertion of tx_enable, an “ESD” of two consecutive vectors of two quinary symbols is generated, after which the transmission of a sequence indicating the idle mode is resumed.

Collision detection is implemented by noting the occurrence of carrier receptions during transmissions, following the model of 10BASE-T. The PCS shall implement the Transmit process as depicted in Figure 32–12 including compliance with the associated state variables as specified in 32.3.4.

32.3.5.2 PCS Receive

PCS Receive accepts vectors of two quinary symbols from the PMA via the rx_symb_vector parameter. After correct receiver operation has been achieved, the loc_rcvr_status parameter assumes the value OK, and PCS

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Receive continuously checks that the received sequence satisfies the encoding rule used in idle mode. As soon as a violation is detected, PCS Receive asserts the parameter receiving and determines whether the violation is due to reception of "SSD" or to a receiver error by examining the last two received vectors (RA_{n-1}, RB_{n-1}) and (RA_n, RB_n). In the first case, during the two symbol periods corresponding to "SSD," PCS Receive replaces "SSD" by preamble bits. Following "SSD," the signal RX_DV is asserted and each received vector is decoded into a data nibble RXD<3:0> until "ESD" is detected. Deassertion of RX_DV and transition to the IDLE state take place upon detection of "ESD". The signal RX_ER is asserted if a receiver error occurs before proper stream termination. In the second case, the signal RX_ER is asserted and the parameter rxerror_status assumes the value ERROR. Deassertion of RX_DV and transition to the IDLE state (rxerror_status=NO_ERROR) takes place upon detection of a sequence generated in idle mode.

A premature stream termination is caused by the detection of four consecutive vectors satisfying the encoding rule used in idle mode prior to the detection of "ESD", provided that the first vector is not a valid data vector. Note that RX_DV remains asserted during the symbol periods corresponding to the first three idle vectors, while RX_ER=TRUE is signaled on the MII. The signal RX_ER is also asserted in the LINK FAILED state, which ensures that RX_ER remains asserted for at least one symbol period. The PCS shall implement the Receive process as depicted in Figure 32–13 including compliance with the associated state variables as specified in 32.3.4.

The parameters receiving and rxerror_status are communicated to the PCS's clients by the following primitives:

PCS_CARRIER.indication (carrier_status)
: A signal generated by PCS Receive to indicate reception of non-idle quinary symbols. The purpose of this primitive is to give clients indication of activity on the underlying continuous-signaling channel.

PCS_RXERROR.indication (rxerror_status)
: A signal generated by PCS Receive to indicate a reception of non-idle symbols that does not start with "SSD."

32.3.5.3 PCS Carrier Sense

The PCS Carrier Sense process generates the signal CRS on the MII, which the MAC uses via the Reconciliation sublayer for frame receptions and for deferral. The process operates by performing logical operations on TX_EN and receiving. The PCS shall implement the Carrier Sense process as depicted in Figure 32–14 including compliance with the associated state variables as specified in 32.3.4.

32.3.6 PCS electrical specifications

The interface between PCS, PMA and PHY Control is an abstract message-passing interface, having no specified electrical properties. Electrical characteristics of the signals passing between the PCS and MII may be found in Clause 22.

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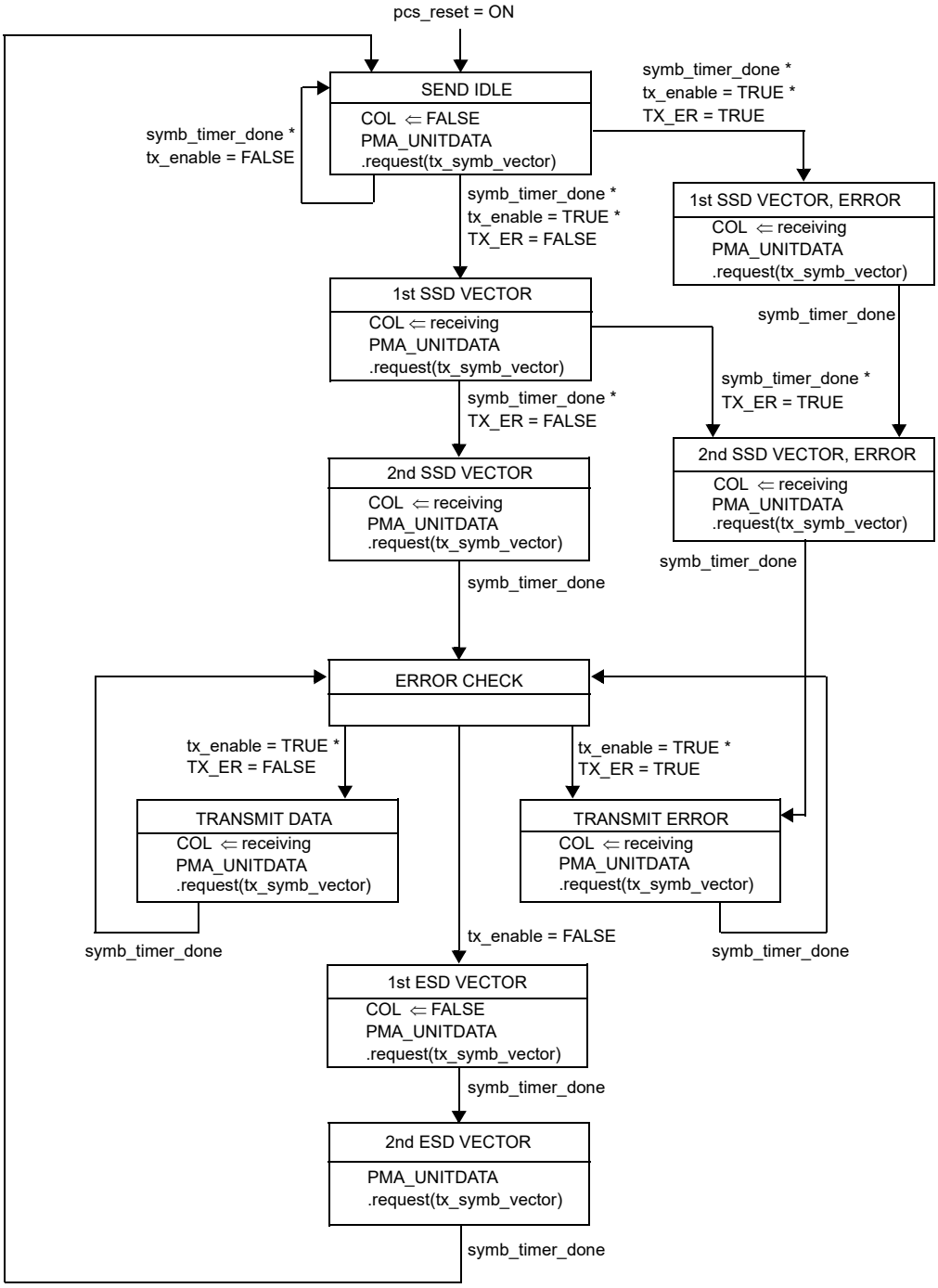

NOTE—The generation of PMA_UNITDATA.request(tx_symb_vector) depends on the parameters config, tx_mode, and loc_rcvr_status as defined in 32.3.1.2 and is not shown explicitly in the state diagram.

Figure 32–12—PCS Transmit state diagram

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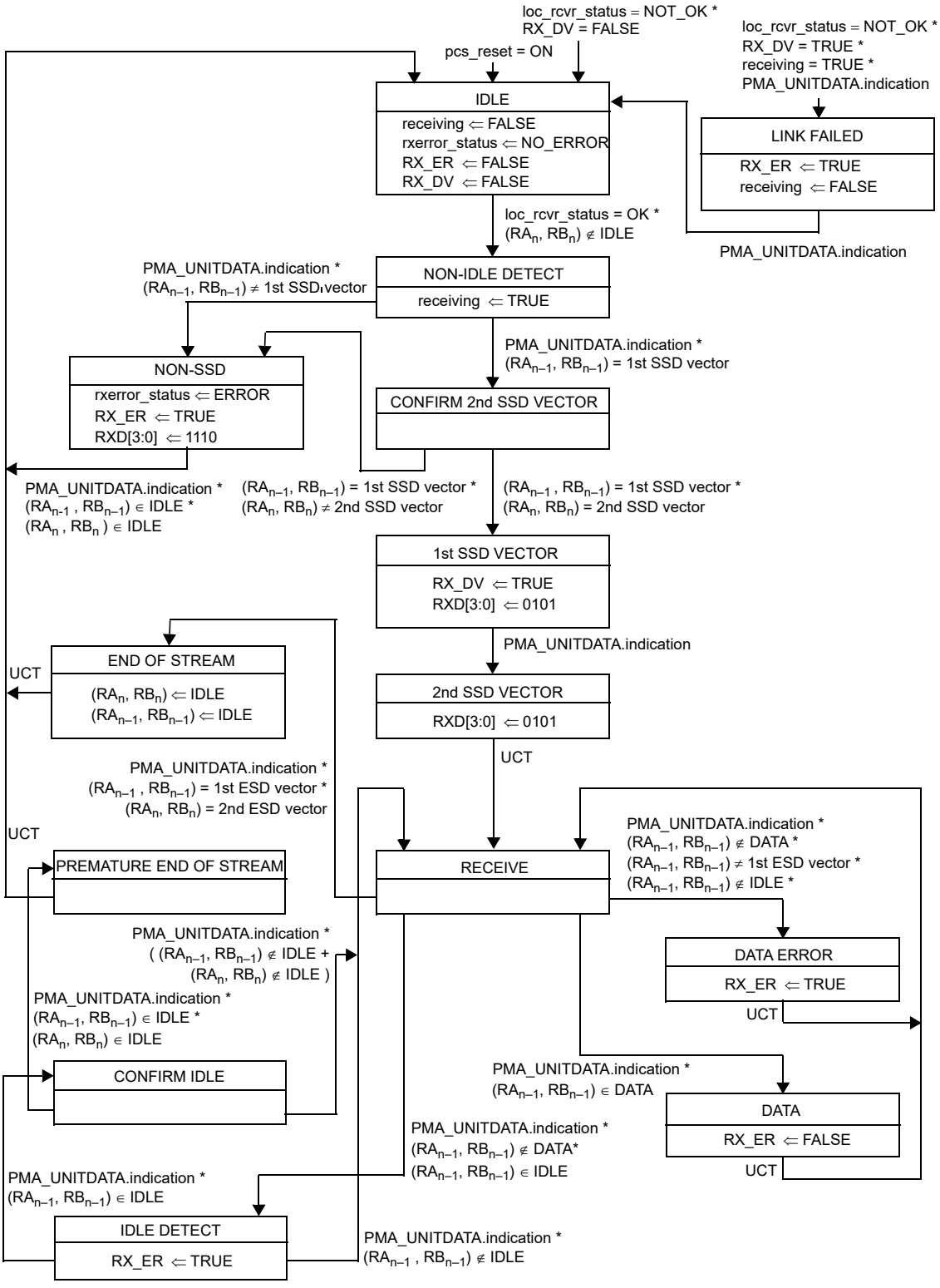

Figure 32–13—PCS Receive state diagram

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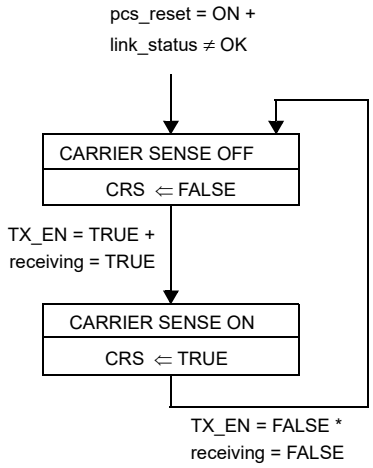

Figure 32–14—PCS Carrier Sense state diagram

32.4 PMA functional specifications and service interface

32.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 32.4.2 to the 100BASE-T2 baseband medium, specified in 32.7. The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), specified in 32.8.

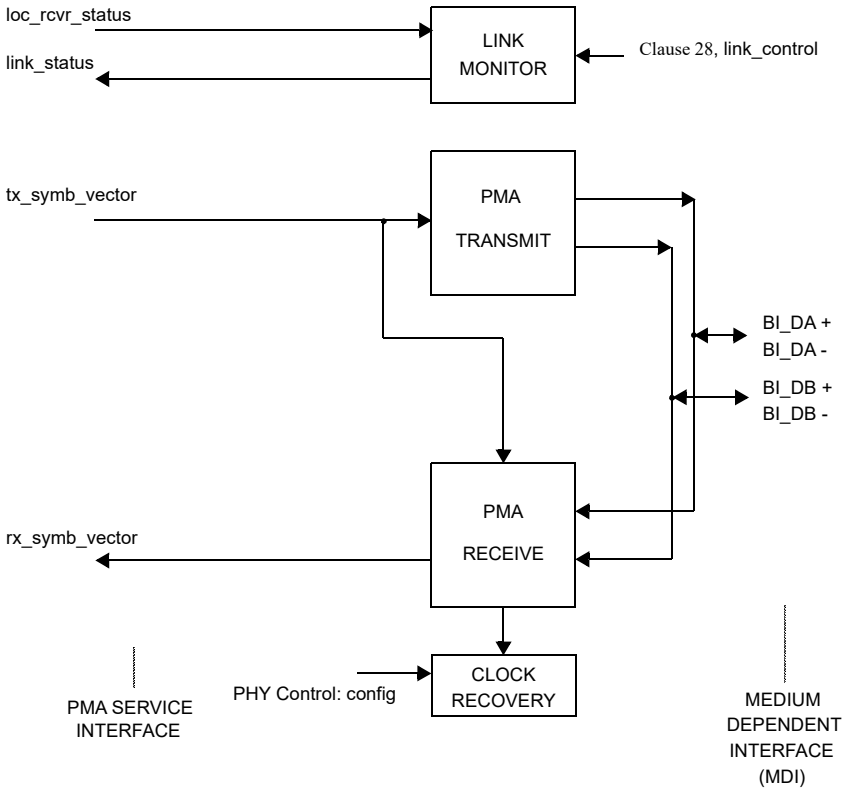

Figure 32–15—PMA reference diagram

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32.4.1.1 PMA functions

The PMA sublayer comprises one PMA Reset function and four simultaneous and asynchronous operating functions. The PMA operating functions are PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function. The Reset function may be shared between PMA and PCS sublayers.

The PMA reference diagram, Figure 32–15, shows how the operating functions relate to the messages of the PMA Service interface, PHY Control Service interface, and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive, and are not shown in Figure 32–15. The management interface and its functions are specified in Clause 22.

32.4.1.1.1 PMA Reset function

The PMA Reset function shall be executed any time either of two conditions occurs. These two conditions are "power on" and the receipt of a reset request from the management entity. The PMA Reset function initializes all PMA functions and forces Auto-Negotiation to be executed. The PMA Reset function sets pma_reset = ON for the duration of its reset function. All state diagrams take the open ended pma_reset branch upon execution of the PMA Reset function. The reference diagrams do not explicitly show the PMA Reset function.

32.4.1.1.2 PMA Transmit function

The PMA Transmit function comprises two independent transmitters to generate five-level pulse-amplitude modulated signals on each of the two pairs BI_DA and BI_DB. PMA Transmit shall continuously transmit onto the MDI pulses modulated by the quinary symbols given by tx_symb_vector[BI_DA] and tx_symb_vector[BI_DB], respectively. The two transmitters shall be driven by the same transmit clock. The signals generated by PMA Transmit will follow the mathematical description given in 32.4.1.2.1, and shall comply with the electrical specifications given in 32.6.

32.4.1.1.3 PMA Receive function

The PMA Receive function comprises two independent receivers for quinary pulse-amplitude modulated signals on each of the two pairs BI_DA and BI_DB. PMA Receive contains the circuits necessary to detect quinary symbol sequences from the signals received at the MDI over receive pairs BI_DA and BI_DB and present these sequences to the PCS Receive function. The signals received at the MDI are described mathematically in 32.4.1.2.2. The PHY shall translate the signals received on pairs BI_DA and BI_DB into the PMA_UNITDATA.indication parameter rx_symb_vector with a symbol error ratio of less than one part in 10^{10}.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization, suppression of cyclo-stationary interference signals created by alien near-end crosstalk sources, and echo and self near-end crosstalk cancellation. The sequence of quinary transmitted symbols tx_symb_vector is needed to perform echo and self near-end crosstalk cancellation.

32.4.1.1.4 Link Monitor function

Link Monitor determines the status of the underlying receive channel. Failure of the underlying receive channel typically causes the PMA's clients to suspend normal operation.

The Auto-Negotiation process notifies Link Monitor whether the device connected to the far end is of type 100BASE-T2. Based on this and other information, Link Monitor sets two important internal variables:

a) The pma_type variable that indicates whether the remote station is of type 100BASE-T2 or not,
b) The link_status variable that is sent across the PMA Service interface.

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The Link Monitor function shall comply with the state diagram of Figure 32-16.

Upon power-on, reset, or release from power-down, the Auto-Negotiation algorithm sets link_control=SCAN_FOR_CARRIER and sends during this period fast link pulses to signal its presence to a remote station. If the presence of a remote station is sensed through reception of fast link pulses, the Auto-Negotiation algorithm sets link_control=DISABLE and exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. If the presence of a remote 100BASE-T2 station is established, the Auto-Negotiation algorithm permits full operation by setting link_control=ENABLE. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

32.4.1.1.5 Clock Recovery function

The Clock Recovery function couples to both receive pairs. It provides a synchronous clock for sampling the signals on the two pairs.

The Clock Recovery function shall provide a clock suitable for synchronous signal sampling on each line so that the symbol error ratio indicated in 32.4.1.1.3 is achieved. The received clock signal has to be stable and ready for use when training has been completed (loc_rcvr_status=OK).

32.4.1.2 PMA interface messages

The messages between the PMA, PCS, and PHY Control are defined in 32.4.2, PMA Service Interface. Communication through the MDI is summarized below.

32.4.1.2.1 MDI signals transmitted by the PHY

The quinary symbols to be transmitted by the PMA on the two pairs BI_DA and BI_DB are denoted by tx_symb_vector[BI_DA] and tx_symb_vector[BI_DB], respectively. Five-level Pulse Amplitude Modulation over each pair (PAM5×5) is the modulation scheme employed in 100BASE-T2. It is the function of PMA Transmit to generate on each pair a pulse-amplitude modulated signal of the form

$$s(t) = \sum_k a_k h_1(t - kT)$$

where a_k represents the quinary symbol from the set {–2, –1, 0, +1, +2} to be transmitted at time kT, and $h_1(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 32.6.

32.4.1.2.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise:

$$r(t) = \sum_k a_k h_2(t - kT) + w(t)$$

In this equation, $h_2(t)$ denotes the impulse response of the overall channel from the transmit side up to the MDI at the receive side, and $w(t)$ is a term that includes the contribution of various noise sources. The two signals received on pair BI_DA and BI_DB shall be processed within the PMA Receive function to yield the quinary received symbols rx_symb_vector[BI_DA] and rx_symb_vector[BI_DB].

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32.4.1.3 PMA state diagram

32.4.1.3.1 State diagram variables

link_control
: The link_control parameter as communicated by the PMA_LINK.request primitive.
Values: See 32.4.2.4.

link_status
: The link_status parameter as communicated by the Link Monitor function through the PMA_LINK.indication primitive.
Values: See 32.4.2.5.

loc_rcvr_status
: The loc_rcvr_status parameter as communicated by the PMA_RXSTATUS.request primitive.
Values: See 32.2.2.3.1.

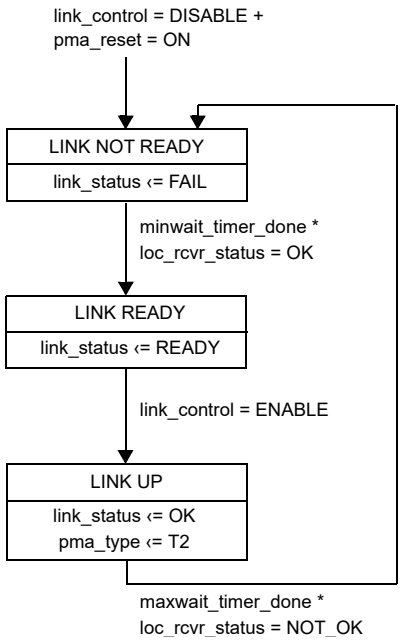
pma_reset
: Allows reset of all PMA functions.
Values: ON and OFF
Set by: PMA Reset

32.4.1.3.2 Timers

maxwait_timer
: Values: See 32.2.4.

minwait_timer
: Values: See 32.2.4.

32.4.1.3.3 Link Monitor state diagram



NOTE—The variables link_control and link_status are designated as link_control_[T2] and link_status_[T2], respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

Figure 32-16—Link Monitor state diagram

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32.4.2 PMA service interface

This subclause specifies the services provided by the PMA. These services are described in an abstract manner and do not imply any particular implementation. The PMA Service Interface supports the exchange of symbol vectors, status indications, and control signals between the PMA, the PCS, and PHY Control. The following primitives are defined:

PMA_TYPE.indication
PMA_UNITDATA.request
PMA_UNITDATA.indication
PMA_LINK.request
PMA_LINK.indication
PMA_CARRIER.indication
PMA_RXERROR.indication

The parameter config is passed from PHY Control to the PMA via the primitive PHYC_CONFIG.indication. The definition of this parameter is given for the PHY Control Service interface in 32.2.2.1 and is not repeated here for the PMA Service interface.

32.4.2.1 PMA_TYPE.indication

This primitive is generated by the PMA to indicate the nature of the PMA instantiation. Its purpose is to allow clients to support connections to the various types of 100BASE-T PMA entities in a generalized manner.

32.4.2.1.1 Semantics of the service primitive

PMA_TYPE.indication (pma_type)

The pma_type parameter for use with the 100BASE-T2 PMA is T2.

32.4.2.1.2 When generated

The PMA shall continuously generate this primitive to indicate the value of pma_type.

32.4.2.1.3 Effect of receipt

The client uses the value of pma_type to define the semantics of the primitives defined at the PMA service interface.

32.4.2.2 PMA_UNITDATA.request

This primitive defines the transfer of pairs of quinary symbols in the form of the tx_symb_vector parameter from the PCS to the PMA. The quinary symbols are obtained in the PCS Transmit function using the encoding rules defined in 32.3.1.2 to represent MII data streams, an idle mode, or other sequences.

32.4.2.2.1 Semantics of the service primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission using 100BASE-T2 signaling, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the two transmit pairs BI_DA and BI_DB. The tx_symb_vector parameter takes on the form:

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SYMB_PAIR A vector of two quinary symbols, one for each of the two transmit pairs BI_DA and BI_DB. Each quinary symbol may take on one of the values –2, –1, 0, +1 or +2.

The quinary symbols that are elements of tx_symb_vector are called, according to the pair on which each will be transmitted, tx_symb_vector[BI_DA] and tx_symb_vector[BI_DB].

32.4.2.2.2 When generated

The PCS generates PMA_UNITDATA.request (SYMB_PAIR) synchronously with every MII TX_CLK cycle.

32.4.2.2.3 Effect of receipt

Upon receipt of this primitive, the PMA transmits on the MDI the signals corresponding to the indicated quinary symbols. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pairs BI_DA and BI_DB.

32.4.2.3 PMA_UNITDATA.indication

This primitive defines the transfer of pairs of quinary symbols in the form of the rx_symb_vector parameter from the PMA to the PCS.

32.4.2.3.1 Semantics of the service primitive

PMA_UNITDATA.indication (rx_symb_vector)

During reception of PAM5×5 signals using 100BASE-T2 signaling, the PMA_UNITDATA.indication simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on each of the two receive pairs BI_DA and BI_DB. The rx_symbol_vector parameter takes on the form:

SYMB_PAIR A vector of two quinary symbols, one for each of the two receive pairs BI_DA and BI_DB. Each quinary symbol may take on one of the values –2, –1, 0, +1 or +2.

The quinary symbols that are elements of rx_symb_vector are called, according to the pair upon which each symbol was received, rx_symbol_vector[BI_DA] and rx_symb_vector[BI_DB].

32.4.2.3.2 When generated

The PMA shall generate PMA_UNITDATA.indication (SYMB_PAIR) messages synchronously with signals received at the MDI.

32.4.2.3.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

32.4.2.4 PMA_LINK.request

This primitive allows the Auto-Negotiation algorithm to enable and disable operation of the PMA.

32.4.2.4.1 Semantics of the service primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

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SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PMA reports link_status=FAIL. PHY processes are disabled.
DISABLE	Set by the Auto-Negotiation algorithm in the event fast link pulses are detected. *PHY processes are disabled.* This allows the Auto-Negotiation algorithm to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions.

32.4.2.4.2 When generated

Upon power on, reset, or release from power down, the Auto-Negotiation algorithm issues the message PMA_LINK.request (SCAN_FOR_CARRIER).

32.4.2.4.3 Effect of receipt

While link_control=SCAN_FOR_CARRIER or link_control=DISABLE, the PMA shall report link_status=FAIL. While link_control=ENABLE, PHY Control determines the operations to be performed by the PHY.

32.4.2.5 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium. This primitive informs the PCS, PHY Control and the Auto-Negotiation algorithm about the status of the underlying link.

32.4.2.5.1 Semantics of the service primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK.

FAIL	No valid link established.
READY	Training completed after Auto-Negotiation.
OK	The Link Monitor function indicates that a valid 100BASE-T2 link is established. Reliable reception of signals transmitted from the remote PHY is possible.

32.4.2.5.2 When generated

The PMA shall generate this primitive to indicate the value of link_status in compliance with the state diagrams given in Figure 32-16.

32.4.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 32.2 and 32.3.

32.4.2.6 PMA_CARRIER.indication

This primitive is identical to PCS_CARRIER.indication defined in 32.3.5.2. It is not explicitly shown in the PMA reference diagram.

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32.4.2.7 PMA_RXERROR.indication

This primitive is identical to PCS_RXERROR.indication defined in 32.3.5.2. It is not explicitly shown in the PMA reference diagram.

32.4.2.8 PMA_RXSTATUS.request

This primitive allows the Link Monitor to determine via the parameter loc_rcvr_status generated by the PCS Receive function whether reliable receiver operations are established. The parameter loc_rcvr_status is also passed from the PCS Receive function to the PHY Control Service interface via the primitive PHYC_RXSTATUS.request. The definition of this parameter is given for the PHY Control Service interface in 32.2.2.3 and is not repeated here for the PMA Service interface.

32.5 Management functions

100BASE-T2 makes extensive use of the management functions provided by the Media Independent Interface (Clause 22) and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28.)

In addition to the provision of MII registers 0, 1, 4, 5, 6, and 7, it is required that implementations that support 100BASE-T2 also provide equivalents to MII registers 8, 9, and 10 (Clause 22). Register 8 is used to provide the Auto-Negotiation Link Partner NEXT Page Register, register 9 is used to provide the MASTER-SLAVE Control Register, and register 10 is used to provide the MASTER-SLAVE Status Register. These registers are used to configure PHYs for testing, to manually configure PHYs for MASTER-SLAVE negotiation, to store the contents of Next Pages during the Auto-Negotiation process, and to store information reporting the results of the master/slave configuration process as described in the next subclause.

32.5.1 100BASE-T2 Use of Auto-Negotiation and MII Registers 8, 9, and 10

On power-up, before Auto-Negotiation starts, the Auto-Negotiation Advertisement register shall have the following configuration: The Selector Field (4.4:0) is set to an appropriate code as specified in Annex 28A. The Acknowledge bit (4.14) is set to logic zero. The Technology Ability Field (4:9:5) is set based on the values set in the MII Status Register (register 1) (1.15:11) or equivalent and (4.11:10) is set based on the values set in the MII Status Register (register 1) (1.10:9) or equivalent.

When Auto-Negotiation begins, 100BASE-T2 implementations send an Auto-Negotiation Base Page with bit D15 set to logical one to indicate that a Next Page follows (see 28.2.1.2.)

The Base Page is followed by a formatted Next Page containing the 100BASE-T2 Technology Ability Message Code (7), which indicates that two Unformatted Next Pages containing the 100BASE-T2 Technology Ability fields follow (see Table 28C–1.)

Two Unformatted Next Pages are sent using the 100BASE-T2 Technology Ability fields shown in Table 32–6 Register 8 will be used to store the transmitted information while it is being processed as described below.

Bit U0 of page 1 shall be copied from MII register 4.10 to indicate 100BASE-T2FD advertised ability.

Bit U1 of page 1 shall be copied from MII register 4.11 to indicate 100BASE-T2HD advertised ability.

Bit U2 of page 1 shall be copied from MASTER-SLAVE control register 9.10 to indicate that the PHY device is a repeater port or DTE for 100BASE-T2.

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Bits U3 and U4 shall be copied from MASTER-SLAVE control register (bits 9.12 and 9.11) for use by the MASTER-SLAVE negotiation process as described below.

Bits U5-U10 of page 1 and U0-U9 of page 2 shall be used to define the seed used for the MASTER-SLAVE negotiation process described as follows.

Using the information described above, the PHY performs a MASTER-SLAVE configuration process as defined in 32.5.4.3. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown Auto-Negotiation Arbitration State Diagram (Figure 28–18.)

If the local device detects that both the local device and the remote device are of the same type (either repeater or DTE) and that both have generated the same random seed, it sets the Ack2 bit of register 8 to logical zero and generates and transmits a new random seed for MASTER-SLAVE negotiation.

The MASTER-SLAVE configuration process returns one of the three following outcomes.

Successful: Bit 10:15 of the MASTER-SLAVE Status Register is set to logical zero and bit 10.14 is set to logical one. 100BASE-T2 returns control to Auto-Negotiation (at the entrance to the FLP LINK GOOD CHECK state in Figure 28–18) and passes the value of MASTER or SLAVE to PHYC_CONFIG.indication (see 32.2.2.)

Unsuccessful: link_status_T2 is set to FAIL and Auto-Negotiation restarts (see Figure 28–18.)

Fault detected: (This happens when both end stations are set for manual configuration and both are set to MASTER or both are set to SLAVE.) Bit 10.15 of the MASTER-SLAVE Status Register is set to logical one to indicate that a manual configuration fault has been detected and bit 10.14 is set to logical one to indicate that MASTER-SLAVE resolution completed with a fault. Because the MASTER-SLAVE relationship was not established, link_status_T2 is set to FAIL, causing Auto-Negotiation to restart.

32.5.2 Management functions

The management interface specified in Clause 22 provides a simple, two-wire, serial interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY. This interface is referred to as the MII Management Interface. The register definition specifies a basic register set with an extension mechanism.

100BASE-T2 requires the basic register set that consists of two registers referred to as the Control Register (register 0) and the Status Register (register 1) and of some PHY-specific registers. The detailed definitions of these registers are given in 22.2.4.

The full set of management registers is listed in Table 22–6 and 100BASE-T2 PHY specific registers are given in Table 32–3.

Table 32–3—100BASE-T2 Control and Status registers

Register address	Register name	Basic/Extended
9	MASTER-SLAVE Control register	E
10	MASTER-SLAVE Status register	E

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32.5.3 PHY specific registers for 100BASE-T2

Some of the extended registers (registers with addresses 2 to 15) are used as PHY specific registers as described in 22.2.4.3. A 100BASE-T2 PHY shall use register addresses 9 and 10 for its control and status functions. The bits in the 100BASE-T2 Control register are used to place the PHY into several possible test modes and to determine the MASTER-SLAVE relationship during Auto-Negotiation. The bits in the 100BASE-T2 Status register are used to report the MASTER-SLAVE relationship determined during Auto-Negotiation, the local and remote receiver status, and provide an idle error counter.

32.5.3.1 100BASE-T2 Control register (Register 9)

Register 9 shall provide the following values for 100BASE-T2. The assignment of bits in the register is shown in Table 32–4. The default value for each bit of the register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

Table 32–4—100BASE-T2 Control register (MII management Register 9) bit definition

Bit(s)	Name	Description	R/W
9.15:14	Transmitter test mode	Default bit values are “00”	R/W
9.13	Receiver test mode	Default bit value is “0”	R/W
9.12	MASTER-SLAVE Manual Configuration Enable	1 = Enable MASTER-SLAVE Manual Configuration value 0 = Disable MASTER-SLAVE Manual Configuration value (default)	R/W
9.11	MASTER-SLAVE Manual Configuration Value	1 = Configure PHY as MASTER during MASTER-SLAVE negotiation, only when 9.12 is set to logical one. 0 = Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when 9.12 is set to logical one.	R/W
9.10	T2_Repeater/DTE bit	1 = Repeater device port 0 = DTE device	R/W
9.9:0	Reserved		

32.5.3.1.1 Transmitter test mode

For a PHY with 100BASE-T2 capability, the PHY shall be placed in transmitter test mode 1 operation (described in 32.6.1.2.1) when bit 9.15 is set to logical zero and bit 9.14 is set to logical one. When bit 9.15 is set to logical one and bit 9.14 is set to logical zero, the PHY shall be placed in transmitter test mode 2 operation as described in 32.6.1.2.1. When bit 9.15 is set to logical one and bit 9.14 is set to logical one, the PHY shall be placed in the transmitter test mode 3 operation as described in 32.6.1.2.1.

The default value for bits 9.15:14 are all zero.

32.5.3.1.2 Receive test mode

The PHY shall be placed in the receiver test mode as described in 32.6.1.3.2 when the bit 9.13 is set to logical one.

The default value for bit 9.13 is zero.

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32.5.3.1.3 MASTER-SLAVE Manual Configuration Enable

The MASTER-SLAVE relationship is established during Auto-Negotiation via either automatic MASTER-SLAVE configuration or manual configuration. If bit 9.12 is set to logical zero, then the MASTER-SLAVE configuration negotiation function will determine the PHY configuration. If bit 9.12 is set to logical one, then manual MASTER-SLAVE configuration is enabled, using 9.11 to specify the value. (Usage of this bit is further described in 32.5.3.1.)

The default value of bit 9.12 is zero.

32.5.3.1.4 MASTER-SLAVE Manual Configuration Value

MASTER-SLAVE Manual configuration is enabled by setting bit 9.12 to logical one. When manual configuration mode is enabled, setting bit 9.11 to logical one configures the PHY as MASTER, and setting bit 9.11 to logic zero configures the PHY as SLAVE during MASTER-SLAVE negotiation process and shall be used to report the result of the MASTER-SLAVE configuration resolution for that PHY. Detailed description of the use of this bit in MASTER-SLAVE configuration resolution is provided in 32.5.3.1.

The default value of bit 9.11 is zero.

32.5.3.1.5 T2_Repeater/DTE Bit

Bit 9.10 shall be set to logical zero if the PHY is a DTE device and shall be set to a logical one if the PHY is a repeater device port (usage of this bit is described in 32.5.2.)

32.5.3.1.6 Reserved bits

Bits 9.9:0 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

32.5.3.2 100BASE-T2 Status register (Register 10)

Register 10 shall provide the following values for 100BASE-T2. The assignment of bits in the register is shown in Table 32–5. The default value for each bit of the register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

Table 32–5—100BASE-T2 Status register (MII management Register 10) bit definition

Bit(s)	Name	Description	R/W[a]
10.15	MASTER-SLAVE manual configuration fault	1 = MASTER-SLAVE manual configuration fault detected 0 = No MASTER-SLAVE manual configuration fault detected	RO/SC
10.14	MASTER-SLAVE configuration resolution complete	1 = MASTER-SLAVE configuration resolution has completed 0 = MASTER-SLAVE configuration resolution has not completed	RO
10.13	Local Receiver Status	1 = Local Receiver OK 0 = Local Receiver not OK	RO
10.12	Remote Receiver Status	1 = Remote Receiver OK 0 = Remote Receiver not OK	RO
10.11:8	Reserved		
10.7:0	Idle Error Count	Idle Error count	RO/SC

[a]R/W = Read/Write, SC = Self Clearing, RO = Read Only

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32.5.3.2.1 MASTER-SLAVE Manual Configuration Fault

When read as a logical one, bit 10.15 indicates that a MASTER-SLAVE Manual Configuration Fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The MASTER-SLAVE Manual Configuration Fault bit shall be implemented with a latching function, such that the occurrence of a MASTER-SLAVE Manual Configuration Fault will cause the MASTER-SLAVE Manual Configuration Fault bit to be set and remain set until it is cleared. The MASTER-SLAVE Manual Configuration Fault bit shall be cleared each time register 10 is read via the management interface and shall also be cleared by a 100BASE-T2 PMA reset.

For 100BASE-T2, this fault condition will occur when both PHYs are forced to be MASTER or SLAVE at the same time using bits 9.12 and 9.11. Bit 10.15 should be set via the MASTER-SLAVE Configuration Resolution function described in 32.5.4.

32.5.3.2.2 MASTER-SLAVE Configuration Resolution Complete

When read as a logical one, bit 10.14 indicates that the MASTER-SLAVE Resolution process has been completed and that the contents of registers 9 and 10 related to MASTER-SLAVE are valid. When read as a logic zero, bit 10.14 indicates that the MASTER-SLAVE Configuration Resolution process has not been completed and that the contents of registers 9 and 10 which are related to MASTER-SLAVE resolution are invalid. Bit 10.14 should be set via the MASTER-SLAVE Configuration Resolution function described in 32.5.4.

32.5.3.2.3 Local Receiver Status

Bit 10.13 indicates the status of the local receiver. Local receiver status is defined by the value of the loc_rcvr_status variable described in 32.2.3.

32.5.3.2.4 Remote Receiver Status

Bit 10.12 indicates the status of the remote receiver. Remote receiver status is defined by the value of the rem_rcvr_status variable described in 32.2.3.

32.5.3.2.5 Reserved bits

Bit 10.11:8 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

32.5.3.2.6 Idle Error count

Bits 10.7:0 indicate the Idle Error count, where 10.7 is the most significant bit. During normal operation these bits contain a cumulative count of the errors detected when the receiver is receiving idles and the PHY Control parameter tx_mode is equal to SEND_N (indicating that both local and remote receiver status have been detected to be OK). When the PHY has receiver test mode (bit 9.13) enabled, these bits contain a cumulative count of the errors detected at all times when the local receiver status is OK. These bits are reset to all zeros when the error count is read by the management function or upon execution of the PCS Reset function and they are held at all ones in case of overflow (see 30.5.1.1.13).

32.5.4 Changes and additions to Auto-Negotiation (Clause 28)

32.5.4.1 Change to 28.2.4.1.3 (Auto-Negotiation Advertisement register)

For implementations which support 100BASE-T2, the Technology Ability Field (4:9:5) is set based on the values set in the MII Status Register (register 1) (1.15:11) or equivalent and (4.11:10) is set based on the values set in the MII Status Register (register 1) (1.10:9) or equivalent. Use of register 4 is defined in 28.2.4.1.3.

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32.5.4.2 Use of Auto-Negotiation Next Page codes for 100BASE-T2 PHYs

For a PHY capable of 100BASE-T2 transmission, during Auto-Negotiation the Base Page will be followed by a Next Page with a message code containing the 100BASE-T2 Technology Ability Message Code (7) as shown in Table 28C–1. This Message Next Page indicates that two Unformatted Message Next Pages will follow which contain the 100BASE-T2 Technology Ability Fields as described in Table 32–6.

Table 32–6—Bit assignments for Unformatted Next Pages containing 100BASE-T2 Technology Ability Field

Bit	Technology	MII register bit/source
PAGE 1		
U0	100BASE-T2 Half Duplex (1 = Half Duplex and 0 = no Half Duplex)	MII register 4.10
U1	100BASE-T2 Full Duplex (1=Full Duplex and 0 = no Full Duplex)	MII register 4.11
U2	100BASE-T2 Repeater/DTE bit (1 = Repeater and 0 = DTE)	MII register 9.10 (MASTER-SLAVE Control register)
U3	100BASE-T2 MASTER-SLAVE Manual Configuration Enable (1 = Manual Configuration Enable); intended to be used for manual selection in a particular MASTER-SLAVE mode. To be used in conjunction with bit U4	MII register 9.12 (MASTER-SLAVE Control register)
U4	100BASE-T2 MASTER-SLAVE Manual Configuration value 1 = MASTER and 0 = SLAVE. This bit is ignored if U3 = 0.	MII register 9.11 (MASTER-SLAVE Control register)
U5	100BASE-T2 MASTER-SLAVE Seed Bit 0 (SB0) (LSB)	MASTER-SLAVE seed value (15.0)
U6	100BASE-T2 MASTER-SLAVE Seed Bit 1 (SB1)	
U7	100BASE-T2 MASTER-SLAVE Seed Bit 2 (SB2)	
U8	100BASE-T2 MASTER-SLAVE Seed Bit 3 (SB3)	
U9	100BASE-T2 MASTER-SLAVE Seed Bit 4 (SB4)	
U10	100BASE-T2 MASTER-SLAVE Seed Bit 5 (SB5)	
PAGE 2		
U0	100BASE-T2 MASTER-SLAVE Seed Bit 6 (SB6)	
U1	100BASE-T2 MASTER-SLAVE Seed Bit 7 (SB7)	
U2	100BASE-T2 MASTER-SLAVE Seed Bit 8 (SB8)	
U3	100BASE-T2 MASTER-SLAVE Seed Bit 9 (SB9)	
U4	100BASE-T2 MASTER-SLAVE Seed Bit 10 (SB10)	
U5	100BASE-T2 MASTER-SLAVE Seed Bit 11 (SB11)	
U6	100BASE-T2 MASTER-SLAVE Seed Bit 12 (SB12)	
U7	100BASE-T2 MASTER-SLAVE Seed Bit 13 (SB13)	
U8	100BASE-T2 MASTER-SLAVE Seed Bit 14 (SB14)	
U9	100BASE-T2 MASTER-SLAVE Seed Bit 15 (SB15)	
U10	unused	

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32.5.4.3 MASTER-SLAVE Configuration Resolution

Since both PHYs that share a link segment are capable of being MASTER or SLAVE, a prioritization scheme exists to ensure that the correct mode is chosen. The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using Table 32–7 with the 100BASE-T2 Technology Ability Next Page bit values specified in Table 32–7 and information received from the link partner.

Table 32–7—100BASE-T2 MASTER-SLAVE Configuration Resolution table

Local Device Type	Remote Link Partner Type	Resolution Function result	
		Local Device	Remote Link Partner
DTE (U2=0 & U3=0) or Manual SLAVE (U3=1 & U4=0)	Repeater (U2=1 & U3=0) or Manual MASTER (U3=1 & U4=1)	SLAVE	MASTER
Repeater (U2=1 & U3=0)	Manual MASTER (U3=1 & U4=1)		
Manual SLAVE (U3=1 & U4=0)	DTE (U2=0 & U3=0)		
Repeater (U2=1 & U3=0) or Manual MASTER (U3=1 & U4=1)	DTE (U2=0 & U3=0) or Manual SLAVE (U3=1 & U4=0)	MASTER	SLAVE
DTE (U2=0 & U3=0)	Manual Slave (U3=1 & U4=0)		
Manual Master (U3=1 & U4=1)	Repeater (U2=1 & U3=0)		
Repeater (U2=1 & U3=0)	Repeater (U2=1 & U3=0)	PHY with higher seed value is the MASTER. If the seeds are equal, the MASTER-SLAVE resolution is unsuccessful, set link_status_T2=FAIL, causing Auto-Negotiation to restart.	
DTE (U2=0 & U3=0)	DTE (U2=0 & U3=0)		
Manual SLAVE (U3=1 & U4=0)	Manual SLAVE (U3=1 & U4=0)	Fault detected Set link_status_T2=FAIL, forcing Auto-Negotiation to restart.	
Manual MASTER (U3=1 & U4=1)	Manual MASTER (U3=1 & U4=1)		

The rationale for this hierarchy is straightforward. A 100BASE-T2 repeater has higher priority than a DTE to become the MASTER. In the case where both devices are of the same type, e.g., both devices are Repeaters, the device with the higher MASTER-SLAVE seed bits (SB0..SB15), where SB15 is the MSB, becomes the MASTER and the device with the lower seed value becomes the SLAVE. In case both devices have the same seed value, both should assert link_status_T2=FAIL (as defined in 28.3.1) and restart Auto-Negotiation. Successful completion of the MASTER-SLAVE resolution shall be treated as MASTER-SLAVE configuration resolution complete and the 100BASE-T2 Status Register bit 10.14 shall be set to logical one.

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The method of generating a random seed is left to the implementer. The generated random seeds should belong to a sequence of independent, identically distributed integer numbers with a uniform distribution in the range of 0 to 65535. The algorithm used to generate the integer should be designed to minimize the correlation between the number generated by any two devices at any given time. A seed counter shall be provided to track the number of seed attempts. The seed counter shall be set to zero at startup and shall be incremented each time a seed is generated. A MASTER-SLAVE resolution fault shall be declared if resolution is not reached after the generation of seven seeds.

The MASTER-SLAVE Manual Configuration Enable bit (control register bit 9.12) is used to manually set a device to become the MASTER or the SLAVE. In case both devices are manually set to become the MASTER or the SLAVE, this condition shall be flagged as a MASTER-SLAVE Manual Configuration fault condition, thus the MASTER-SLAVE Manual Configuration fault bit (status register bit 10.15) shall be set to logical one. The MASTER-SLAVE Manual Configuration fault condition shall be treated as MASTER-SLAVE configuration resolution complete and status register bit 10.14 shall be set to logical one. In this case, link_status_T2 will be set to FAIL, because the MASTER-SLAVE relationship was not resolved. This will force Auto-Negotiation to restart after the link_fail_inhibit_timer has expired. Determination of MASTER-SLAVE values occur on the entrance to the FLP LINK GOOD CHECK state (Figure 28–18) when the highest common denominator (HCD) technology is 100BASE-T2. The resulting MASTER-SLAVE value is used by the 100BASE-T2 PHY control (32.2.2.1).

32.6 PMA electrical specifications

This clause defines the electrical characteristics of the PHY at the MDI.

The ground reference point for all common-mode tests is the MII ground circuit. Implementations without an MII use the chassis ground. The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

32.6.1 PMA-to-MDI interface characteristics

32.6.1.1 Isolation requirement

NOTE—Since September 2003, maintenance changes are no longer being considered for this clause. Since February 2021, electrical isolation requirements are in J.1.

The PHY shall provide electrical isolation between the DTE or repeater circuits, including frame ground and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50–60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC 60950
b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC 60950, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

32.6.1.2 Transmitter electrical specifications

The PMA shall provide the Transmit function specified in 32.4.1.1.2 in accordance with the electrical specifications of this clause.

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Where a load is not specified, the transmitter shall meet requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.

The tolerance on the poles of the test filters used in this clause shall be ±1%.

32.6.1.2.1 Transmitter test modes

Since the 100BASE-T2 PCS employs scrambling, synchronization of data at the MII to the scrambled state is virtually impossible. Therefore a special transmit test mode shall be required to allow for testing of the transmitter waveform. Additionally, a test mode for measuring transmitter output jitter is also required.

For a PHY with a MII interface, these modes shall be enabled by setting bits 9.14 and 9.15 (MASTER-SLAVE Control Register) of the MII Management register set as shown in Table 32–8. These test modes shall only change the data symbols provided to the transmitter circuitry and may not alter the electrical characteristics of the transmitter. A PHY without an MII shall provide a means to provide these functions. The vendor shall provide a means to enable these modes for conformance testing.

Table 32–8—MII management register set

Bit 9.15	Bit 9.14	Mode
0	0	Normal operation
0	1	TX Test mode 1—waveform test
1	0	TX Test mode 2—jitter test
1	1	TX Test mode 3—idle

When transmit test mode 1 is enabled, the PHY shall transmit the following sequence of data symbols (A_n and B_n of 32.3.1.2.3) continually from both transmitters:

{{+2 followed by 127 0 symbols}, {-2 followed by 127 0 symbols},{+1 followed by 127 0 symbols}, {–1 followed by 127 0 symbols}, {16 +2 symbols, 16 –2 symbols followed by 224 0 symbols}}

This sequence is repeated continually without breaks between the repetitions when the transmit test mode is enabled. A typical transmitter output is shown below in Figure 32–17. The transmitter shall time the transmitted symbols from a 25.000 MHz ± 0.01% clock.

When transmit test mode 2 is enabled, the PHY shall transmit the data symbol sequence {+2,–2} repeatedly on both channels. The transmitter shall time the transmitted symbols from a 25.000 MHz ± 0.01% clock.

When transmit test mode 3 is enabled, the PHY shall transmit idle data compliant with the idle signaling specified in 32.3 with loc_rcvr_status=OK.

32.6.1.2.2 Peak differential output voltage and level distortion

When in transmit test mode 1 and observing the differential signal output at the MDI terminated in 100 Ω, preprocessed by the high pass filter defined below, for each pair, with no intervening cable, the absolute value of the peak of the waveform at points A and B as defined in Figure 32–17 shall fall within 1.71 V to 1.91 V (1.81 V ± 0.5 dB).

The absolute value of the peak of the waveforms at points A and B shall differ by less than 1%.

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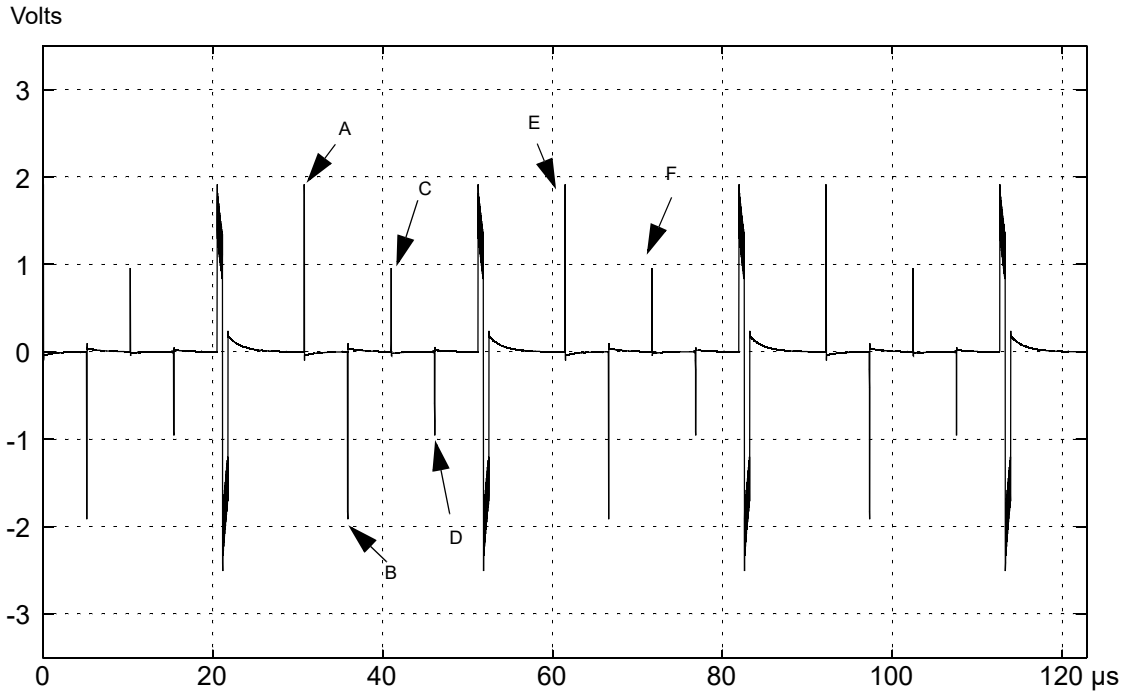
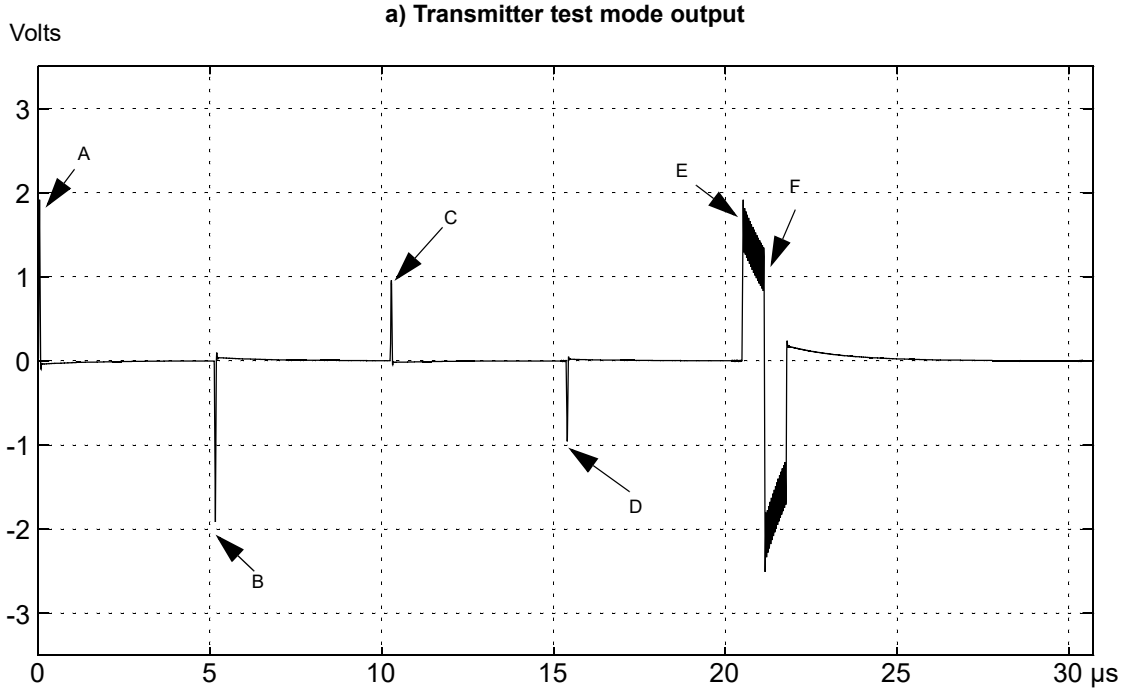


a) Transmitter test mode output



b) Expanded view of partial cycle of transmitter test mode output

Figure 32–17—Example transmitter test mode transmitter

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The absolute value of the peak of the waveform at points C and D as defined in Figure 32–17 shall differ from 0.5 times the average of the absolute values of the peaks of the waveform at points A and B by less than 2%.

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The preprocessing filter shall have the following transfer function:[65]

$$H_{\text{preprocess}}(f) = \frac{\mathrm{j}f}{\mathrm{j}f + 200 \times 10^3} \quad f \text{ in Hz}$$

32.6.1.2.3 Maximum output droop

When in transmit test mode 1 and observing the differential signal output at the MDI, for either pair, with no intervening cable, the peak value of the waveform at point F as defined in Figure 32–17 shall be greater than 70.5% of the peak value of the waveform at point E. A preprocessing filter is not used for this measurement.

32.6.1.2.4 Differential output templates

The transmitter differential output voltage shall be measured at the output of the high pass preprocessing filter defined in 32.6.1.2.2, with no intervening cables. The voltage waveforms A, B, C and D defined in Figure 32–17, after normalization by their respective peak values, shall lie within the time domain template defined in Figure 32–18 and the piecewise linear interpolation between the points in Table 32–9. The waveforms may be shifted in time as appropriate to fit within the template.

Additionally, the magnitude in dB of the Fourier transform of the preprocessed waveforms A, B, C and D shall lie within the frequency domain template defined in Figure 32–18 and the piecewise linear interpolation between the points in Table 32–9. The time span of the waveforms so processed shall be –80 ns to +2000 ns with the 0 ns point of the waveform aligned as for the time domain mask shown in Figure 32–18 and the magnitude of the Fourier transform should be normalized so that the maximum value is at 0 dB.[66]

[65]"j" denotes the positive square root of –1.

[66]A sampling rate of 100 MHz is adequate to generate the frequency domain mask.

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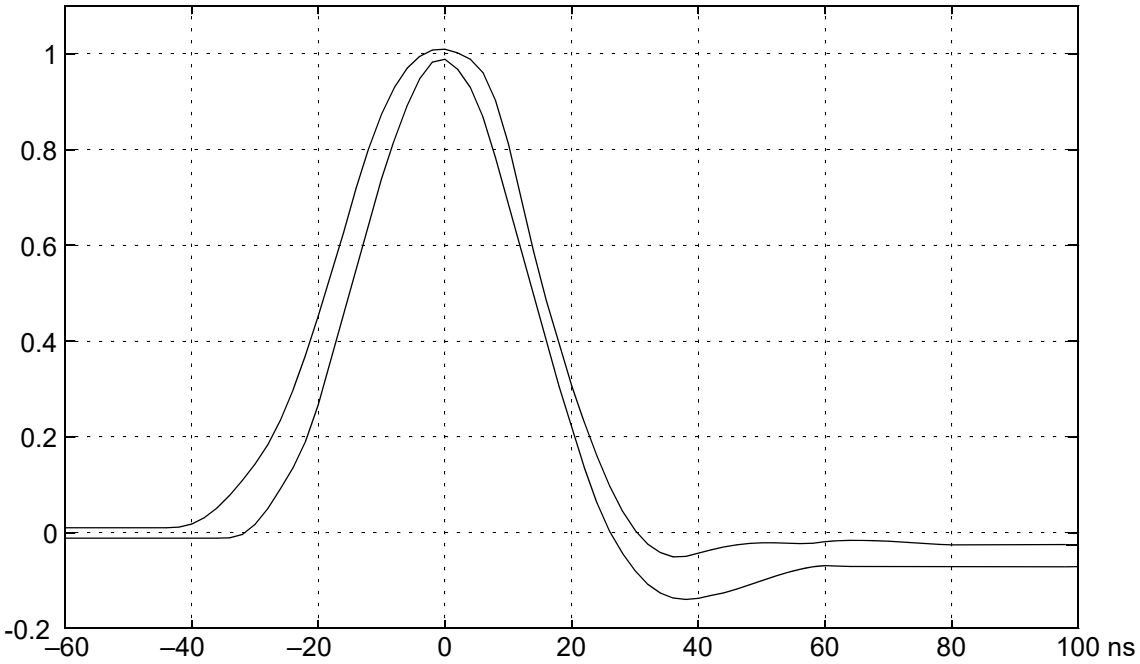
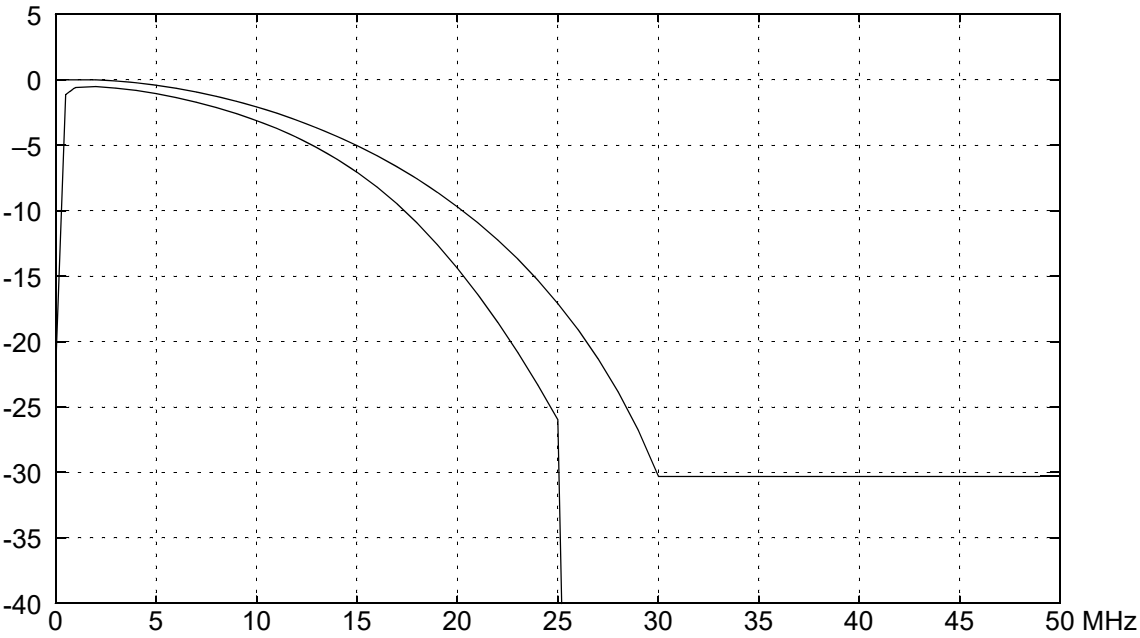


a) Normalized time domain transmit template



b) Normalized frequency domain transmit template

NOTE—The frequency domain transmit template is not intended to address electromagnetic radiation limits.

Figure 32–18—Normalized transmit templates as measured at MDI through preprocessing filter

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Table 32–9—Normalized time domain voltage template

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
–60	0.010	–0.011	22	0.230	0.136
–58	0.010	–0.011	24	0.160	0.062
–56	0.010	–0.011	26	0.097	0.002
–54	0.010	–0.011	28	0.045	–0.042
–52	0.010	–0.011	30	0.005	–0.079
–50	0.010	–0.011	32	–0.024	–0.108
–48	0.010	–0.011	34	–0.042	–0.126
–46	0.010	–0.011	36	–0.051	–0.136
–44	0.010	–0.011	38	–0.050	–0.139
–42	0.012	–0.011	40	–0.043	–0.137
–40	0.018	–0.011	42	–0.036	–0.131
–38	0.031	–0.011	44	–0.030	–0.126
–36	0.052	–0.011	46	–0.025	–0.118
–34	0.078	–0.011	48	–0.023	–0.109
–32	0.109	–0.004	50	–0.021	–0.100
–30	0.143	0.017	52	–0.021	–0.091
–28	0.184	0.050	54	–0.022	–0.084
–26	0.235	0.092	56	–0.023	–0.077
–24	0.298	0.136	58	–0.022	–0.071
–22	0.372	0.192	60	–0.019	–0.069
–20	0.453	0.268	62	–0.017	–0.070
–18	0.538	0.360	64	–0.016	–0.070
–16	0.627	0.461	66	–0.016	–0.071
–14	0.720	0.558	68	–0.017	–0.071
–12	0.804	0.650	70	–0.018	–0.071
–10	0.874	0.739	72	–0.020	–0.071
–8	0.930	0.820	74	–0.021	–0.071
–6	0.969	0.891	76	–0.023	–0.071
–4	0.995	0.948	78	–0.024	–0.070
–2	1.008	0.982	80	–0.026	–0.070
0	1.009	0.988	82	–0.025	–0.070

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Table 32–9—Normalized time domain voltage template *(continued)*

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
2	1.002	0.967	84	–0.025	–0.070
4	0.989	0.930	86	–0.025	–0.071
6	0.961	0.868	88	–0.025	–0.071
8	0.902	0.782	90	–0.025	–0.072
10	0.812	0.685	92	–0.025	–0.072
12	0.703	0.585	94	–0.025	–0.072
14	0.587	0.489	96	–0.025	–0.071
16	0.485	0.396	98	–0.025	–0.071
18	0.394	0.306	100	–0.025	–0.071
20	0.307	0.221			

Table 32–10—Normalized frequency domain amplitude spectrum template

Frequency, MHz	Normalized transmit frequency domain template, upper limit, dB	Normalized transmit frequency domain template, lower limit, dB	Frequency, MHz	Normalized transmit frequency domain template, upper limit, dB	Normalized transmit frequency domain template, lower limit, dB
0.1	0.00	–17.88	22	–12.24	–18.52
0.2	0.00	–13.49	23	–13.70	–20.84
0.3	0.00	–9.09	24	–15.31	–23.32
0.4	0.00	–4.70	25	–17.09	–25.97
0.5	0.00	–1.13	26	–19.08	
0.6	0.00	–1.01	27	–21.31	
0.7	0.00	–0.90	28	–23.84	
0.8	0.00	–0.78	29	–26.78	
0.9	0.00	–0.66	30	–30.29	
1	0.00	–0.59	31	–30.29	
2	–0.00	–0.52	32	–30.29	
3	–0.08	–0.63	33	–30.29	
4	–0.23	–0.82	34	–30.29	

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Table 32–10—Normalized frequency domain amplitude spectrum template *(continued)*

Frequency, MHz	Normalized transmit frequency domain template, upper limit, dB	Normalized transmit frequency domain template, lower limit, dB	Frequency, MHz	Normalized transmit frequency domain template, upper limit, dB	Normalized transmit frequency domain template, lower limit, dB
5	–0.42	–1.06	35	–30.29	
6	–0.65	–1.36	36	–30.29	
7	–0.93	–1.71	37	–30.29	
8	–1.26	–2.12	38	–30.29	
9	–1.64	–2.59	39	–30.29	
10	–2.07	–3.12	40	–30.29	
11	–2.55	–3.72	41	–30.29	
12	–3.08	–4.40	42	–30.29	
13	–3.67	–5.17	43	–30.29	
14	–4.31	–6.05	44	–30.29	
15	–5.03	–7.06	45	–30.29	
16	–5.80	–8.20	46	–30.29	
17	–6.65	–9.50	47	–30.29	
18	–7.58	–10.96	48	–30.29	
19	–8.59	–12.59	49	–30.29	
20	–9.70	–14.39	50	–30.29	
21	–10.91	–16.37			

32.6.1.2.5 Transmitter timing jitter

When in transmit test mode 2, the peak-to-peak jitter of the zero crossings of the differential signal output at the MDI shall be less than 0.5 ns.

32.6.1.2.6 Transmit clock frequency

The quinary symbol transmission rate on each pair shall be 25.000 MHz ± 0.01%.

32.6.1.3 Receiver electrical specifications

The PMA shall provide the Receive function specified in 32.4.1.1.3 in accordance with the electrical specifications of this clause. The patch cabling and interconnecting hardware used in test configurations shall meet or exceed ISO/IEC 11801, Category 3 specifications.

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32.6.1.3.1 Test channel

To perform the Receiver Alien NEXT Tolerance test and Receiver timing jitter test described in this clause, a test channel including transmitter, cabling and NEXT models is required. This test channel is shown conceptually in Figure 32–19.

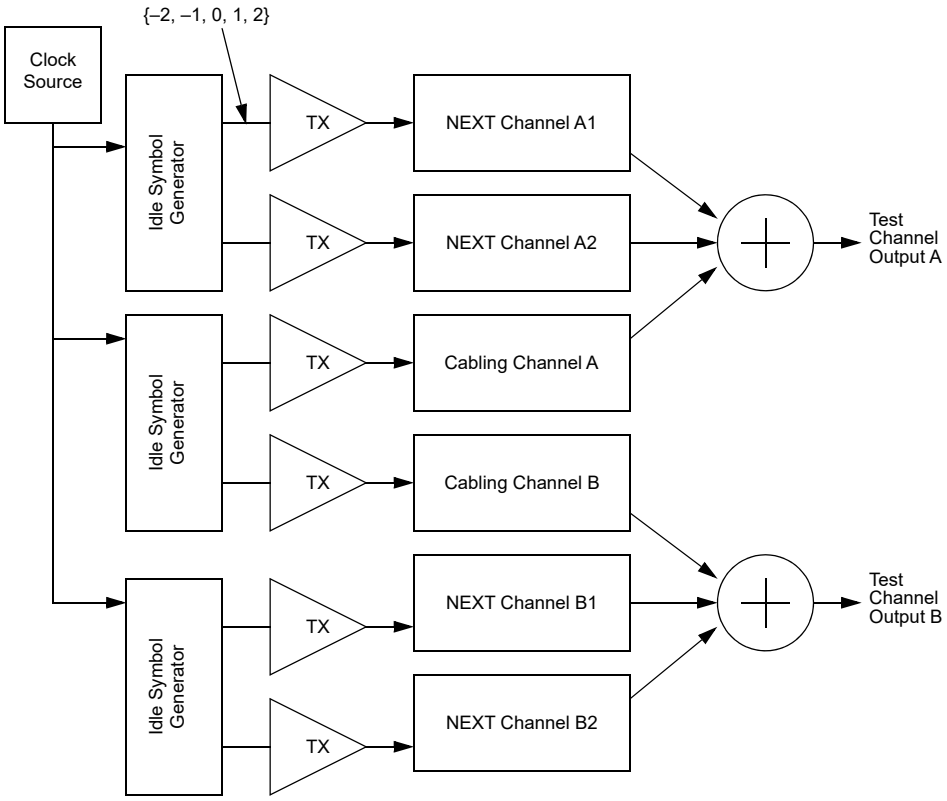

Figure 32–19—Conceptual diagram of test channel

The combined responses of the TX block and NEXT or cabling channel blocks shall be those defined in Table 32–8. The responses of Table 32–10 are shown in Figure 32–20. The responses represent the response of the test channel to isolated "1" symbols in a stream of "0" symbols at the input to the transmitter blocks. The test channel may also include a first order high pass filter with 3 dB cutoff frequency of less than 100 kHz in addition to the tabulated responses. The output impedance of the test channel shall be consistent with 32.6.1.4.1. The idle symbol generator outputs shall be conformant with the idle signaling specified in 32.3 with loc_rcvr_status=OK. The clock source shall result in a quinary symbol transmission rate conformant with 32.6.1.2.6. The peak-to-peak jitter on the clock source shall be less than 0.2 ns.

The test channel may be implemented in any fashion consistent with the above specifications and with the further constraint that the ratio of the squared error between the implemented NEXT channel symbol responses and the specified NEXT channel symbol responses to the energy in the specified NEXT channel symbol responses shall be less than 5% and the energy of the implemented NEXT channel symbol responses and the energy of the specified NEXT channel symbol responses shall differ by less than ± 0.25 dB. If digital filters are used to generate the channel characteristics, care has to be taken to ensure that the signal to quantization noise at the channel output is greater than 35 dB.

The NEXT channel impulse responses defined in Table 32–11 have been developed to simulate the attenuation and phase characteristics of worst case 100BASE-T2 alien NEXT.

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The cabling attenuation and group delay characteristics used to derive the cable symbol responses specified in Table 32–8 at 0 m and 100 m are obtained from the following worst-case model of the cabling attenuation. The model includes 1.2 dB of flat loss simulating three worst-case Category 3 connectors. The group delay of the model is relative and does not include the fixed delay associated with 100 m of Category 3 cabling. An additional 570 ns of fixed delay should be added in order to obtain the absolute group delay; however, it is not necessary to add this fixed delay to the test channel.

$$\gamma(f) = -\left(1.537\times10^{-6}\sqrt{\pi f} + j1.537\times10^{-6}\sqrt{\pi f} + 44.5\times10^{-12}2\pi f\right)$$

$$H(f, l) = e^{\gamma(f)l}10^{-1.2/20}$$

f in Hz

Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.000	4.23e-06	1.48e-03	1.62e-05	1.19e-05	–5.05e-06	3.70e-05
0.004	–4.87e-06	1.55e-03	–5.97e-05	1.67e-05	6.71e-05	2.02e-05
0.008	–6.84e-06	1.62e-03	–8.19e-05	1.15e-05	9.78e-05	1.20e-05
0.012	–1.28e-05	1.69e-03	–3.79e-05	7.58e-06	6.43e-05	1.50e-05
0.016	3.56e-06	1.77e-03	4.53e-05	–1.47e-05	1.52e-06	6.51e-06
0.020	6.97e-06	1.86e-03	1.40e-04	–1.73e-05	–9.59e-05	–8.16e-06
0.024	1.68e-05	1.96e-03	1.86e-04	3.46e-05	–2.01e-04	–3.64e-05
0.028	8.73e-06	2.07e-03	1.07e-04	1.67e-04	–2.67e-04	–8.81e-05
0.032	–1.98e-05	2.19e-03	–2.56e-04	3.80e-04	–1.52e-04	–2.18e-04
0.036	–2.24e-05	2.33e-03	–1.10e-03	5.84e-04	3.94e-04	–5.53e-04
0.040	–2.95e-05	2.48e-03	–2.53e-03	7.54e-04	1.49e-03	–1.14e-03
0.044	3.65e-05	2.64e-03	–4.46e-03	8.74e-04	3.09e-03	–1.95e-03
0.048	7.11e-05	2.83e-03	–6.54e-03	9.73e-04	4.89e-03	–2.83e-03
0.052	6.30e-05	3.04e-03	–8.29e-03	1.13e-03	6.41e-03	–3.56e-03
0.056	–1.42e-04	3.27e-03	–9.25e-03	1.38e-03	7.24e-03	–3.97e-03
0.060	–4.49e-04	3.53e-03	–9.04e-03	1.93e-03	6.96e-03	–3.84e-03
0.064	–2.89e-04	3.87e-03	–7.53e-03	2.90e-03	5.37e-03	–3.06e-03
0.068	–2.72e-04	4.22e-03	–4.73e-03	4.32e-03	2.51e-03	–1.69e-03
0.072	–3.87e-04	4.55e-03	–9.82e-04	5.95e-03	–1.15e-03	–5.29e-05
0.076	–1.39e-04	5.09e-03	3.14e-03	7.23e-03	–4.72e-03	1.19e-03
0.080	4.92e-04	5.83e-03	6.98e-03	7.68e-03	–7.33e-03	1.50e-03
0.084	1.50e-03	6.70e-03	9.98e-03	6.90e-03	–8.27e-03	5.20e-04
0.088	9.97e-04	7.69e-03	1.19e-02	4.74e-03	–7.36e-03	–1.68e-03

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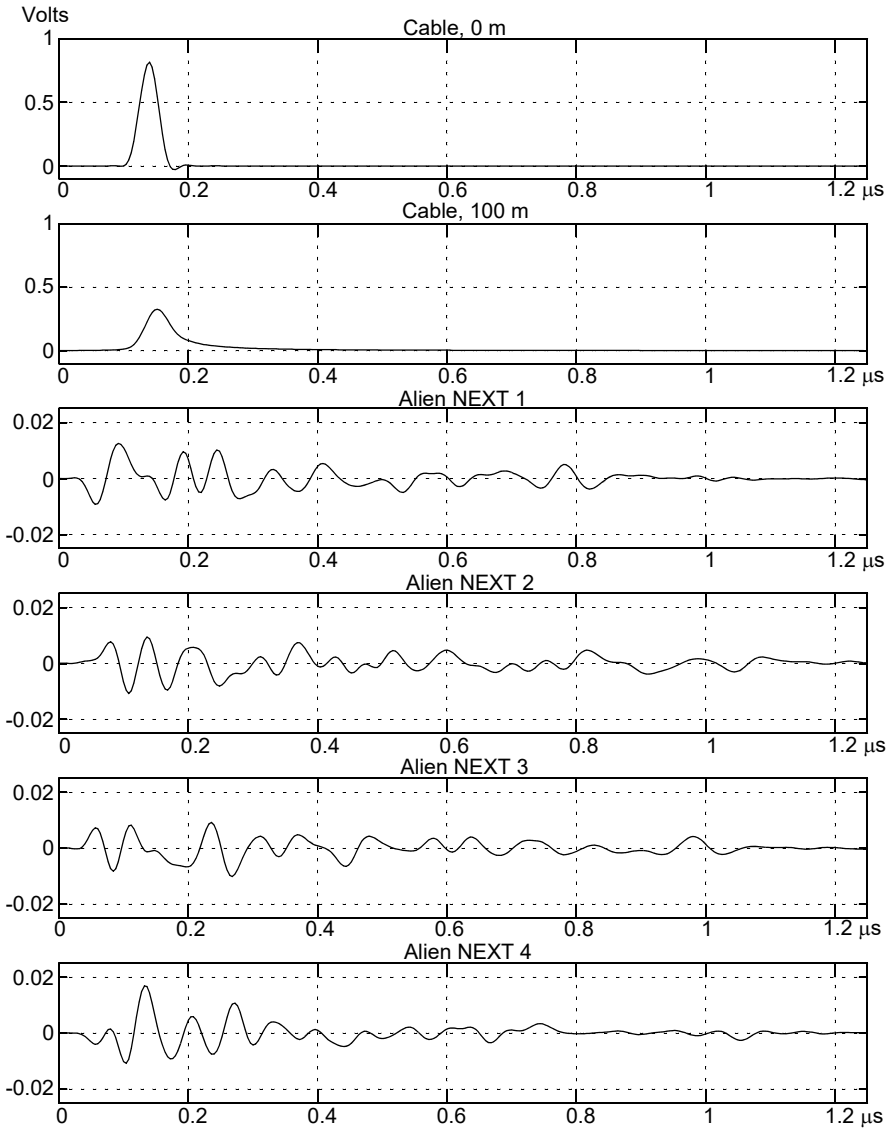

Figure 32–20—Test channel responses

Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (µs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.092	–1.45e-03	8.81e-03	1.26e-02	1.43e-03	–4.82e-03	–4.65e-03
0.096	–3.84e-03	1.04e-02	1.22e-02	–2.63e-03	–1.17e-03	–7.77e-03
0.100	–1.58e-03	1.27e-02	1.10e-02	–6.60e-03	2.75e-03	–1.01e-02
0.104	1.30e-02	1.64e-02	9.20e-03	–9.57e-03	6.05e-03	–1.08e-02
0.108	4.64e-02	2.27e-02	7.06e-03	–1.08e-02	7.97e-03	–9.32e-03
0.112	1.05e-01	3.30e-02	4.91e-03	–9.84e-03	8.20e-03	–5.54e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.116	1.95e-01	4.93e-02	3.07e-03	–7.06e-03	7.00e-03	–2.20e-04
0.120	3.14e-01	7.28e-02	1.72e-03	–3.05e-03	4.92e-03	5.68e-03
0.124	4.54e-01	1.04e-01	9.15e-04	1.34e-03	2.63e-03	1.10e-02
0.128	5.95e-01	1.42e-01	6.23e-04	5.31e-03	6.32e-04	1.50e-02
0.132	7.15e-01	1.84e-01	6.67e-04	8.16e-03	–7.36e-04	1.69e-02
0.136	7.93e-01	2.28e-01	8.34e-04	9.39e-03	–1.30e-03	1.66e-02
0.140	8.15e-01	2.68e-01	7.62e-04	8.84e-03	–1.25e-03	1.44e-02
0.144	7.77e-01	3.01e-01	1.20e-04	6.66e-03	–9.31e-04	1.08e-02
0.148	6.83e-01	3.21e-01	–1.23e-03	3.32e-03	–8.01e-04	6.60e-03
0.152	5.49e-01	3.27e-01	–3.18e-03	–5.48e-04	–1.13e-03	2.50e-03
0.156	3.96e-01	3.20e-01	–5.26e-03	–4.29e-03	–1.86e-03	–1.22e-03
0.160	2.50e-01	3.01e-01	–6.94e-03	–7.31e-03	–2.84e-03	–4.34e-03
0.164	1.30e-01	2.73e-01	–7.68e-03	–9.17e-03	–3.84e-03	–6.80e-03
0.168	4.47e-02	2.40e-01	–7.12e-03	–9.59e-03	–4.72e-03	–8.47e-03
0.172	–5.75e-03	2.06e-01	–5.15e-03	–8.55e-03	–5.39e-03	–9.25e-03
0.176	–2.72e-02	1.75e-01	–1.95e-03	–6.26e-03	–5.80e-03	–9.17e-03
0.180	–2.85e-02	1.49e-01	1.90e-03	–3.26e-03	–6.01e-03	–8.19e-03
0.184	–1.82e-02	1.28e-01	5.60e-03	–1.83e-04	–6.13e-03	–6.35e-03
0.188	–5.94e-03	1.11e-01	8.37e-03	2.37e-03	–6.29e-03	–3.77e-03
0.192	2.81e-03	9.82e-02	9.58e-03	4.08e-03	–6.50e-03	–7.34e-04
0.196	6.25e-03	8.84e-02	9.06e-03	5.05e-03	–6.67e-03	2.21e-03
0.200	5.54e-03	8.06e-02	6.92e-03	5.49e-03	–6.65e-03	4.54e-03
0.204	3.70e-03	7.39e-02	3.66e-03	5.66e-03	–6.24e-03	5.81e-03
0.208	1.64e-03	6.80e-02	6.86e-05	5.68e-03	–5.26e-03	5.91e-03
0.212	5.59e-05	6.26e-02	–3.01e-03	5.52e-03	–3.62e-03	4.88e-03
0.216	–1.02e-03	5.77e-02	–4.83e-03	5.16e-03	–1.33e-03	2.95e-03
0.220	–1.53e-03	5.34e-02	–4.97e-03	4.40e-03	1.42e-03	4.48e-04
0.224	–9.73e-04	4.96e-02	–3.46e-03	3.07e-03	4.28e-03	–2.25e-03
0.228	–3.20e-04	4.63e-02	–6.22e-04	1.04e-03	6.85e-03	–4.71e-03
0.232	2.89e-05	4.33e-02	2.90e-03	–1.55e-03	8.65e-03	–6.56e-03
0.236	1.73e-04	4.06e-02	6.35e-03	–4.20e-03	9.24e-03	–7.53e-03
0.240	1.33e-04	3.83e-02	8.95e-03	–6.40e-03	8.35e-03	–7.48e-03
0.244	1.39e-04	3.62e-02	1.02e-02	–7.73e-03	5.99e-03	–6.40e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.248	9.80e-05	3.42e-02	9.77e-03	–8.11e-03	2.56e-03	–4.30e-03
0.252	4.22e-05	3.25e-02	7.90e-03	–7.70e-03	–1.34e-03	–1.35e-03
0.256	–2.56e-06	3.08e-02	4.95e-03	–6.76e-03	–5.02e-03	2.14e-03
0.260	–3.84e-05	2.93e-02	1.50e-03	–5.62e-03	–7.91e-03	5.67e-03
0.264	–2.83e-05	2.80e-02	–1.85e-03	–4.58e-03	–9.67e-03	8.59e-03
0.268	–2.41e-05	2.67e-02	–4.54e-03	-3.89e-03	–1.01e-02	1.04e-02
0.272	–8.46e-06	2.55e-02	–6.29e-03	–3.61e-03	–9.30e-03	1.08e-02
0.276	4.04e-07	2.44e-02	–7.13e-03	–3.62e-03	–7.62e-03	9.78e-03
0.280	4.91e-06	2.34e-02	–7.25e-03	–3.70e-03	–5.51e-03	7.51e-03
0.284	1.01e-05	2.24e-02	–6.97e-03	–3.61e-03	–3.40e-03	4.44e-03
0.288	3.79e-06	2.15e-02	–6.54e-03	–3.18e-03	–1.47e-03	1.18e-03
0.292	2.18e-06	2.07e-02	–6.11e-03	–2.37e-03	2.01e-04	–1.65e-03
0.296	–2.23e-06	1.99e-02	–5.78e-03	–1.23e-03	1.62e-03	–3.54e-03
0.300	–1.74e-06	1.92e-02	–5.43e-03	6.10e-05	2.78e-03	–4.28e-03
0.304	4.33e-07	1.85e-02	–4.87e-03	1.26e-03	3.62e-03	–3.93e-03
0.308	2.19e-07	1.79e-02	–3.88e-03	2.10e-03	4.14e-03	–2.74e-03
0.312	1.40e-06	1.73e-02	–2.42e-03	2.37e-03	4.25e-03	–1.08e-03
0.316	–5.61e-07	1.67e-02	–7.17e-04	1.97e-03	3.87e-03	6.99e-04
0.320	–4.40e-07	1.62e-02	9.57e-04	9.16e-04	2.95e-03	2.25e-03
0.324	–4.37e-07	1.56e-02	2.28e-03	–5.89e-04	1.53e-03	3.34e-03
0.328	–3.68e-08	1.51e-02	3.07e-03	–2.20e-03	–8.99e-05	3.92e-03
0.332	9.92e-07	1.47e-02	3.23e-03	–3.52e-03	–1.59e-03	4.04e-03
0.336	5.29e-07	1.43e-02	2.74e-03	–4.19e-03	–2.63e-03	3.85e-03
0.340	5.69e-07	1.38e-02	1.73e-03	–4.00e-03	–3.00e-03	3.44e-03
0.344	–1.87e-07	1.34e-02	4.38e-04	–2.97e-03	–2.62e-03	2.85e-03
0.348	–3.47e-07	1.31e-02	–8.80e-04	–1.22e-03	–1.53e-03	2.11e-03
0.352	–9.04e-08	1.27e-02	–2.04e-03	9.56e-04	5.06e-05	1.27e-03
0.356	8.10e-08	1.24e-02	–3.01e-03	3.22e-03	1.79e-03	3.65e-04
0.360	5.29e-07	1.20e-02	–3.78e-03	5.22e-03	3.32e-03	–5.53e-04
0.364	3.23e-07	1.17e-02	–4.36e-03	6.64e-03	4.36e-03	–1.41e-03
0.368	1.82e-07	1.14e-02	–4.67e-03	7.34e-03	4.82e-03	–2.03e-03
0.372	–6.93e-08	1.11e-02	–4.60e-03	7.31e-03	4.75e-03	–2.26e-03
0.376	–1.46e-07	1.09e-02	–4.11e-03	6.65e-03	4.31e-03	–1.98e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.380	6.66e-08	1.06e-02	–3.17e-03	5.50e-03	3.64e-03	–1.29e-03
0.384	1.71e-07	1.03e-02	–1.84e-03	4.02e-03	2.88e-03	–3.97e-04
0.388	3.12e-07	1.01e-02	–2.24e-04	2.44e-03	2.18e-03	4.68e-04
0.392	1.95e-07	9.86e-03	1.51e-03	9.58e-04	1.59e-03	1.07e-03
0.396	5.86e-08	9.64e-03	3.13e-03	–2.37e-04	1.17e-03	1.30e-03
0.400	–2.48e-08	9.43e-03	4.40e-03	–1.02e-03	8.60e-04	1.08e-03
0.404	–3.03e-08	9.22e-03	5.16e-03	–1.34e-03	5.83e-04	4.43e-04
0.408	1.02e-07	9.02e-03	5.37e-03	–1.16e-03	2.87e-04	–4.57e-04
0.412	1.68e-07	8.83e-03	5.08e-03	–5.37e-04	-8.75e-05	–1.43e-03
0.416	1.93e-07	8.64e-03	4.41e-03	4.06e-04	–5.80e-04	–2.27e-03
0.420	1.20e-07	8.46e-03	3.49e-03	1.39e-03	–1.26e-03	–2.94e-03
0.424	3.01e-08	8.29e-03	2.45e-03	2.10e-03	–2.18e-03	–3.47e-03
0.428	5.52e-09	8.12e-03	1.40e-03	2.28e-03	–3.31e-03	–3.92e-03
0.432	2.95e-08	7.96e-03	4.39e-04	1.83e-03	–4.53e-03	–4.33e-03
0.436	1.05e-07	7.80e-03	–4.02e-04	8.46e-04	–5.62e-03	–4.64e-03
0.440	1.40e-07	7.65e-03	–1.11e-03	–4.79e-04	–6.34e-03	–4.79e-03
0.444	1.27e-07	7.51e-03	–1.71e-03	–1.86e-03	–6.51e-03	–4.72e-03
0.448	7.69e-08	7.37e-03	–2.18e-03	–2.95e-03	–6.01e-03	–4.34e-03
0.452	2.73e-08	7.23e-03	–2.53e-03	–3.49e-03	–4.88e-03	–3.66e-03
0.456	2.59e-08	7.10e-03	–2.75e-03	–3.31e-03	–3.20e-03	–2.68e-03
0.460	5.54e-08	6.97e-03	–2.83e-03	–2.57e-03	–1.24e-03	–1.56e-03
0.464	9.74e-08	6.85e-03	–2.80e-03	–1.60e-03	7.13e-04	–5.10e-04
0.468	1.11e-07	6.73e-03	–2.65e-03	–7.72e-04	2.36e-03	2.70e-04
0.472	8.93e-08	6.61e-03	–2.40e-03	–3.48e-04	3.50e-03	6.40e-04
0.476	5.48e-08	6.49e-03	–2.08e-03	–3.49e-04	4.12e-03	6.10e-04
0.480	3.08e-08	6.39e-03	–1.72e-03	–6.97e-04	4.26e-03	2.42e-04
0.484	3.87e-08	6.28e-03	–1.36e-03	–1.18e-03	4.05e-03	–3.37e-04
0.488	6.37e-08	6.17e-03	–1.02e-03	–1.52e-03	3.61e-03	–9.74e-04
0.492	8.60e-08	6.07e-03	–7.22e-04	–1.45e-03	3.03e-03	–1.52e-03
0.496	8.68e-08	5.98e-03	–5.08e-04	–7.85e-04	2.45e-03	–1.85e-03
0.500	6.64e-08	5.88e-03	–4.43e-04	4.01e-04	1.89e-03	–1.94e-03
0.504	4.41e-08	5.79e-03	–6.03e-04	1.84e-03	1.38e-03	–1.81e-03
0.508	3.47e-08	5.70e-03	–1.02e-03	3.19e-03	9.06e-04	–1.54e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.512	4.54e-08	5.61e-03	–1.69e-03	4.14e-03	4.56e-04	–1.20e-03
0.516	6.35e-08	5.52e-03	–2.55e-03	4.57e-03	6.45e-05	–7.70e-04
0.520	7.41e-08	5.44e-03	–3.47e-03	4.40e-03	–2.43e-04	–2.64e-04
0.524	6.88e-08	5.36e-03	–4.30e-03	3.69e-03	–4.49e-04	3.11e-04
0.528	5.25e-08	5.28e-03	–4.86e-03	2.59e-03	–5.97e-04	9.07e-04
0.532	3.91e-08	5.20e-03	–4.98e-03	1.30e-03	–7.31e-04	1.46e-03
0.536	3.76e-08	5.13e-03	–4.57e-03	4.15e-05	–8.65e-04	1.90e-03
0.540	4.78e-08	5.05e-03	–3.67e-03	–1.04e-03	–9.88e-04	2.14e-03
0.544	5.97e-08	4.98e-03	–2.47e-03	–1.87e-03	–1.04e-03	2.11e-03
0.548	6.32e-08	4.91e-03	–1.16e-03	–2.42e-03	–9.79e-04	1.74e-03
0.552	5.59e-08	4.84e-03	4.24e-05	–2.70e-03	–7.35e-04	1.07e-03
0.556	4.40e-08	4.78e-03	9.93e-04	–2.70e-03	–2.60e-04	2.15e-04
0.560	3.68e-08	4.71e-03	1.60e-03	–2.43e-03	4.47e-04	–6.81e-04
0.564	3.90e-08	4.65e-03	1.85e-03	–1.93e-03	1.33e-03	–1.46e-03
0.568	4.74e-08	4.59e-03	1.86e-03	–1.22e-03	2.25e-03	–2.02e-03
0.572	5.44e-08	4.53e-03	1.78e-03	–3.47e-04	3.03e-03	–2.28e-03
0.576	5.40e-08	4.47e-03	1.74e-03	6.36e-04	3.49e-03	–2.22e-03
0.580	4.68e-08	4.41e-03	1.79e-03	1.66e-03	3.55e-03	–1.86e-03
0.584	3.86e-08	4.36e-03	1.86e-03	2.66e-03	3.17e-03	–1.27e-03
0.588	3.55e-08	4.30e-03	1.85e-03	3.54e-03	2.41e-03	–5.17e-04
0.592	3.92e-08	4.25e-03	1.67e-03	4.23e-03	1.41e-03	2.65e-04
0.596	4.55e-08	4.19e-03	1.23e-03	4.64e-03	3.37e-04	9.51e-04
0.600	4.89e-08	4.14e-03	5.18e-04	4.74e-03	-6.03e-04	1.45e-03
0.604	4.65e-08	4.09e-03	–4.25e-04	4.50e-03	–1.23e-03	1.72e-03
0.608	4.03e-08	4.04e-03	–1.43e-03	3.96e-03	–1.42e-03	1.79e-03
0.612	3.52e-08	3.99e-03	–2.30e-03	3.21e-03	–1.13e-03	1.73e-03
0.616	3.46e-08	3.95e-03	–2.85e-03	2.33e-03	–4.11e-04	1.62e-03
0.620	3.84e-08	3.90e-03	–2.96e-03	1.44e-03	6.15e-04	1.56e-03
0.624	4.26e-08	3.86e-03	–2.66e-03	6.40e-04	1.76e-03	1.61e-03
0.628	4.37e-08	3.81e-03	–2.01e-03	1.25e-05	2.81e-03	1.78e-03
0.632	4.06e-08	3.77e-03	–1.16e-03	–4.14e-04	3.60e-03	2.01e-03
0.636	3.58e-08	3.72e-03	–2.62e-04	–6.60e-04	4.00e-03	2.11e-03
0.640	3.29e-08	3.68e-03	5.11e-04	–7.79e-04	3.95e-03	1.94e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.644	3.37e-08	3.64e-03	1.04e-03	–8.48e-04	3.47e-03	1.38e-03
0.648	3.69e-08	3.60e-03	1.32e-03	–9.56e-04	2.68e-03	4.76e-04
0.652	3.95e-08	3.56e-03	1.38e-03	–1.17e-03	1.71e-03	–6.44e-04
0.656	3.91e-08	3.52e-03	1.32e-03	–1.52e-03	7.06e-04	–1.80e-03
0.660	3.60e-08	3.48e-03	1.24e-03	–1.97e-03	–2.19e-04	–2.78e-03
0.664	3.25e-08	3.45e-03	1.22e-03	–2.47e-03	–1.02e-03	–3.39e-03
0.668	3.12e-08	3.41e-03	1.34e-03	–2.93e-03	–1.66e-03	–3.51e-03
0.672	3.26e-08	3.38e-03	1.58e-03	–3.22e-03	–2.14e-03	–3.12e-03
0.676	3.51e-08	3.34e-03	1.92e-03	–3.27e-03	–2.45e-03	–2.36e-03
0.680	3.64e-08	3.31e-03	2.26e-03	–3.01e-03	–2.58e-03	–1.40e-03
0.684	3.52e-08	3.27e-03	2.53e-03	–2.48e-03	–2.54e-03	–4.72e-04
0.688	3.24e-08	3.24e-03	2.67e-03	–1.77e-03	–2.30e-03	2.96e-04
0.692	3.01e-08	3.21e-03	2.66e-03	–1.04e-03	–1.85e-03	8.20e-04
0.696	2.98e-08	3.17e-03	2.47e-03	–4.69e-04	–1.20e-03	1.07e-03
0.700	3.13e-08	3.14e-03	2.17e-03	–1.76e-04	–4.09e-04	1.10e-03
0.704	3.31e-08	3.11e-03	1.78e-03	–2.25e-04	4.27e-04	9.85e-04
0.708	3.34e-08	3.08e-03	1.38e-03	–6.12e-04	1.21e-03	8.49e-04
0.712	3.19e-08	3.05e-03	9.74e-04	–1.24e-03	1.87e-03	7.97e-04
0.716	2.96e-08	3.02e-03	5.40e-04	–1.94e-03	2.35e-03	8.91e-04
0.720	2.83e-08	2.99e-03	4.50e-05	–2.52e-03	2.66e-03	1.15e-03
0.724	2.86e-08	2.96e-03	–5.39e-04	–2.82e-03	2.80e-03	1.56e-03
0.728	2.99e-08	2.94e-03	–1.21e-03	–2.76e-03	2.82e-03	2.06e-03
0.732	3.10e-08	2.91e-03	–1.93e-03	–2.34e-03	2.78e-03	2.56e-03
0.736	3.07e-08	2.88e-03	–2.63e-03	–1.64e-03	2.70e-03	2.99e-03
0.740	2.91e-08	2.86e-03	–3.19e-03	–8.03e-04	2.59e-03	3.27e-03
0.744	2.75e-08	2.83e-03	–3.49e-03	2.08e-05	2.40e-03	3.36e-03
0.748	2.68e-08	2.80e-03	–3.41e-03	6.61e-04	2.08e-03	3.25e-03
0.752	2.74e-08	2.78e-03	–2.90e-03	9.96e-04	1.62e-03	2.96e-03
0.756	2.85e-08	2.75e-03	–1.98e-03	9.72e-04	1.01e-03	2.54e-03
0.760	2.89e-08	2.73e-03	–7.19e-04	6.06e-04	3.03e-04	2.04e-03
0.764	2.83e-08	2.71e-03	7.27e-04	–1.29e-05	–4.51e-04	1.55e-03
0.768	2.69e-08	2.68e-03	2.19e-03	–7.52e-04	–1.17e-03	1.09e-03
0.772	2.57e-08	2.66e-03	3.49e-03	–1.45e-03	–1.76e-03	6.97e-04

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.776	2.55e-08	2.64e-03	4.45e-03	–1.95e-03	–2.16e-03	3.84e-04
0.780	2.62e-08	2.61e-03	4.96e-03	–2.13e-03	–2.35e-03	1.50e-04
0.784	2.70e-08	2.59e-03	4.94e-03	–1.91e-03	–2.33e-03	–9.21e-06
0.788	2.70e-08	2.57e-03	4.41e-03	–1.30e-03	–2.16e-03	–1.09e-04
0.792	2.62e-08	2.55e-03	3.43e-03	–3.53e-04	–1.88e-03	–1.67e-04
0.796	2.50e-08	2.53e-03	2.14e-03	7.94e-04	–1.52e-03	–1.97e-04
0.800	2.43e-08	2.51e-03	6.97e-04	1.99e-03	–1.11e-03	–2.12e-04
0.804	2.44e-08	2.48e-03	–7.29e-04	3.07e-03	–6.76e-04	–2.16e-04
0.808	2.50e-08	2.46e-03	–1.98e-03	3.92e-03	–2.42e-04	–2.11e-04
0.812	2.55e-08	2.44e-03	–2.95e-03	4.47e-03	1.71e-04	–1.93e-04
0.816	2.52e-08	2.43e-03	–3.56e-03	4.69e-03	5.47e-04	–1.58e-04
0.820	2.44e-08	2.41e-03	–3.79e-03	4.59e-03	8.49e-04	–1.06e-04
0.824	2.35e-08	2.39e-03	–3.68e-03	4.24e-03	1.04e-03	–4.15e-05
0.828	2.31e-08	2.37e-03	–3.29e-03	3.71e-03	1.09e-03	3.17e-05
0.832	2.34e-08	2.35e-03	–2.72e-03	3.10e-03	9.78e-04	1.09e-04
0.836	2.38e-08	2.33e-03	–2.02e-03	2.46e-03	7.26e-04	1.89e-04
0.840	2.40e-08	2.31e-03	–1.28e-03	1.85e-03	3.61e-04	2.70e-04
0.844	2.36e-08	2.29e-03	–5.54e-04	1.30e-03	–7.48e-05	3.50e-04
0.848	2.29e-08	2.28e-03	9.66e-05	8.67e-04	–5.29e-04	4.35e-04
0.852	2.22e-08	2.26e-03	6.28e-04	5.63e-04	–9.51e-04	5.28e-04
0.856	2.21e-08	2.24e-03	1.02e-03	3.91e-04	–1.30e-03	6.25e-04
0.860	2.24e-08	2.23e-03	1.26e-03	3.27e-04	–1.54e-03	7.05e-04
0.864	2.27e-08	2.21e-03	1.35e-03	3.18e-04	–1.67e-03	7.38e-04
0.868	2.27e-08	2.19e-03	1.32e-03	3.13e-04	–1.71e-03	7.00e-04
0.872	2.22e-08	2.18e-03	1.20e-03	2.49e-04	–1.65e-03	5.79e-04
0.876	2.15e-08	2.16e-03	1.06e-03	6.50e-05	–1.54e-03	3.86e-04
0.880	2.11e-08	2.15e-03	9.49e-04	–2.75e-04	–1.39e-03	1.42e-04
0.884	2.11e-08	2.13e-03	9.05e-04	–7.77e-04	–1.23e-03	–1.19e-04
0.888	2.14e-08	2.11e-03	9.32e-04	–1.40e-03	–1.08e-03	–3.50e-04
0.892	2.16e-08	2.10e-03	1.01e-03	–2.06e-03	–9.51e-04	–5.12e-04
0.896	2.14e-08	2.08e-03	1.10e-03	–2.69e-03	–8.58e-04	–5.74e-04
0.900	2.09e-08	2.07e-03	1.17e-03	–3.22e-03	–8.19e-04	–5.37e-04
0.904	2.04e-08	2.06e-03	1.17e-03	–3.60e-03	–8.53e-04	–4.30e-04

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.908	2.02e-08	2.04e-03	1.07e-03	–3.81e-03	–9.70e-04	–2.86e-04
0.912	2.02e-08	2.03e-03	8.84e-04	–3.86e-03	–1.17e-03	–1.38e-04
0.916	2.05e-08	2.01e-03	6.43e-04	–3.76e-03	–1.43e-03	–3.73e-06
0.920	2.05e-08	2.00e-03	4.00e-04	–3.57e-03	–1.72e-03	1.07e-04
0.924	2.03e-08	1.99e-03	2.04e-04	–3.32e-03	–2.00e-03	1.97e-04
0.928	1.98e-08	1.97e-03	8.04e-05	–3.05e-03	–2.21e-03	2.83e-04
0.932	1.94e-08	1.96e-03	3.54e-05	–2.77e-03	–2.31e-03	3.84e-04
0.936	1.93e-08	1.95e-03	6.11e-05	–2.49e-03	–2.25e-03	5.12e-04
0.940	1.94e-08	1.93e-03	1.19e-04	–2.19e-03	–2.02e-03	6.60e-04
0.944	1.96e-08	1.92e-03	1.68e-04	–1.87e-03	–1.61e-03	7.99e-04
0.948	1.95e-08	1.91e-03	1.69e-04	–1.51e-03	–1.04e-03	8.98e-04
0.952	1.92e-08	1.90e-03	1.12e-04	–1.11e-03	–3.35e-04	9.23e-04
0.956	1.88e-08	1.88e-03	3.20e-05	–6.75e-04	4.63e-04	8.56e-04
0.960	1.86e-08	1.87e-03	–3.29e-05	–2.21e-04	1.31e-03	6.88e-04
0.964	1.85e-08	1.86e-03	–3.97e-05	2.28e-04	2.16e-03	4.27e-04
0.968	1.86e-08	1.85e-03	3.82e-05	6.47e-04	2.94e-03	1.05e-04
0.972	1.87e-08	1.84e-03	2.03e-04	1.01e-03	3.58e-03	–2.35e-04
0.976	1.86e-08	1.82e-03	4.37e-04	1.30e-03	4.03e-03	–5.42e-04
0.980	1.83e-08	1.81e-03	6.79e-04	1.50e-03	4.23e-03	–7.76e-04
0.984	1.80e-08	1.80e-03	8.54e-04	1.61e-03	4.14e-03	–9.10e-04
0.988	1.78e-08	1.79e-03	8.92e-04	1.65e-03	3.77e-03	–9.27e-04
0.992	1.78e-08	1.78e-03	7.59e-04	1.61e-03	3.13e-03	–8.27e-04
0.996	1.79e-08	1.77e-03	4.78e-04	1.51e-03	2.31e-03	–6.23e-04
1.000	1.79e-08	1.76e-03	9.92e-05	1.35e-03	1.38e-03	–3.43e-04
1.004	1.77e-08	1.75e-03	–3.03e-04	1.14e-03	4.42e-04	–2.81e-05
1.008	1.74e-08	1.74e-03	–6.46e-04	8.71e-04	–4.26e-04	2.80e-04
1.012	1.72e-08	1.73e-03	–8.64e-04	5.31e-04	–1.16e-03	5.35e-04
1.016	1.71e-08	1.71e-03	–9.09e-04	1.17e-04	–1.71e-03	6.95e-04
1.020	1.71e-08	1.70e-03	–7.85e-04	–3.71e-04	–2.06e-03	7.20e-04
1.024	1.72e-08	1.69e-03	–5.39e-04	–9.22e-04	–2.21e-03	5.83e-04
1.028	1.71e-08	1.68e-03	–2.39e-04	–1.51e-03	–2.20e-03	2.80e-04
1.032	1.69e-08	1.67e-03	4.62e-05	–2.08e-03	–2.04e-03	–1.70e-04
1.036	1.67e-08	1.66e-03	2.68e-04	–2.58e-03	–1.78e-03	–7.21e-04

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
1.040	1.65e-08	1.66e-03	3.93e-04	–2.92e-03	–1.45e-03	–1.31e-03
1.044	1.65e-08	1.65e-03	4.08e-04	–3.07e-03	–1.08e-03	–1.86e-03
1.048	1.65e-08	1.64e-03	3.24e-04	–2.97e-03	–6.97e-04	–2.29e-03
1.052	1.65e-08	1.63e-03	1.64e-04	-2.62e-03	-3.38e-04	-2.53e-03
1.056	1.64e-08	1.62e-03	–2.93e-05	–2.04e-03	–2.07e-05	–2.54e-03
1.060	1.62e-08	1.61e-03	–2.24e-04	–1.30e-03	2.39e-04	–2.32e-03
1.064	1.60e-08	1.60e-03	–3.91e-04	–4.72e-04	4.34e-04	–1.91e-03
1.068	1.59e-08	1.59e-03	–5.13e-04	3.49e-04	5.60e-04	–1.37e-03
1.072	1.59e-08	1.58e-03	–5.79e-04	1.08e-03	6.21e-04	–7.75e-04
1.076	1.59e-08	1.57e-03	–5.84e-04	1.66e-03	6.27e-04	–2.13e-04
1.080	1.59e-08	1.56e-03	–5.35e-04	2.04e-03	5.90e-04	2.42e-04
1.084	1.57e-08	1.56e-03	–4.46e-04	2.24e-03	5.24e-04	5.43e-04
1.088	1.55e-08	1.55e-03	–3.40e-04	2.26e-03	4.42e-04	6.80e-04
1.092	1.54e-08	1.54e-03	–2.40e-04	2.14e-03	3.58e-04	6.70e-04
1.096	1.53e-08	1.53e-03	–1.64e-04	1.95e-03	2.82e-04	5.53e-04
1.100	1.53e-08	1.52e-03	–1.21e-04	1.72e-03	2.23e-04	3.73e-04
1.104	1.53e-08	1.51e-03	–1.09e-04	1.48e-03	1.90e-04	1.72e-04
1.108	1.53e-08	1.51e-03	–1.19e-04	1.27e-03	1.85e-04	–1.10e-05
1.112	1.51e-08	1.50e-03	–1.38e-04	1.09e-03	2.03e-04	–1.51e-04
1.116	1.49e-08	1.49e-03	–1.54e-04	9.49e-04	2.33e-04	–2.31e-04
1.120	1.48e-08	1.48e-03	–1.57e-04	8.36e-04	2.60e-04	–2.52e-04
1.124	1.48e-08	1.47e-03	–1.42e-04	7.46e-04	2.72e-04	–2.18e-04
1.128	1.48e-08	1.47e-03	–1.14e-04	6.77e-04	2.53e-04	–1.33e-04
1.132	1.48e-08	1.46e-03	–8.40e-05	6.30e-04	1.95e-04	–6.35e-06
1.136	1.47e-08	1.45e-03	–6.31e-05	6.05e-04	9.72e-05	1.50e-04
1.140	1.45e-08	1.44e-03	–5.84e-05	5.99e-04	–2.78e-05	3.12e-04
1.144	1.44e-08	1.44e-03	–7.04e-05	6.01e-04	–1.58e-04	4.51e-04
1.148	1.43e-08	1.43e-03	–9.63e-05	6.02e-04	–.69e-04	5.45e-04
1.152	1.43e-08	1.42e-03	–1.29e-04	5.87e-04	–3.41e-04	5.76e-04
1.156	1.43e-08	1.42e-03	–1.60e-04	5.43e-04	–3.62e-04	5.36e-04
1.160	1.42e-08	1.41e-03	–1.81e-04	4.58e-04	–3.29e-04	4.30e-04
1.164	1.41e-08	1.40e-03	–1.83e-04	3.30e-04	–2.48e-04	2.72e-04
1.168	1.40e-08	1.39e-03	–1.65e-04	1.72e-04	–1.35e-04	9.19e-05

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
1.172	1.39e-08	1.39e-03	–1.28e-04	4.95e-06	–1.13e-05	–7.86e-05
1.176	1.38e-08	1.38e-03	–7.75e-05	–1.48e-04	1.02e-04	–2.10e-04
1.180	1.38e-08	1.37e-03	–1.90e-05	–2.62e-04	1.90e-04	–2.83e-04
1.184	1.38e-08	1.37e-03	4.03e-05	-3.19e-04	2.48e-04	-2.93e-04
1.188	1.37e-08	1.36e-03	9.40e-05	–3.07e-04	2.73e-04	–2.43e-04
1.192	1.36e-08	1.35e-03	1.37e-04	–2.28e-04	2.68e-04	–1.50e-04
1.196	1.35e-08	1.35e-03	1.66e-04	–9.21e-05	2.37e-04	–3.64e-05
1.200	1.34e-08	1.34e-03	1.80e-04	7.95e-05	1.86e-04	7.45e-05
1.204	1.34e-08	1.34e-03	1.79e-04	2.63e-04	1.22e-04	1.62e-04
1.208	1.34e-08	1.33e-03	1.62e-04	4.36e-04	5.03e-05	2.17e-04
1.212	1.33e-08	1.32e-03	1.27e-04	5.81e-04	–2.48e-05	2.37e-04
1.216	1.33e-08	1.32e-03	7.69e-05	6.83e-04	–9.88e-05	2.28e-04
1.220	1.32e-08	1.31e-03	1.24e-05	7.35e-04	–1.66e-04	2.01e-04
1.224	1.31e-08	1.30e-03	–6.03e-05	7.34e-04	–2.22e-04	1.66e-04
1.228	1.30e-08	1.30e-03	–1.36e-04	6.87e-04	–2.61e-04	1.35e-04
1.232	1.29e-08	1.29e-03	–2.14e-04	6.00e-04	–2.84e-04	1.13e-04
1.236	1.29e-08	1.29e-03	–2.89e-04	4.86e-04	–2.93e-04	1.02e-04
1.240	1.29e-08	1.28e-03	–3.66e-04	3.57e-04	–2.97e-04	9.58e-05
1.244	1.29e-08	1.27e-03	–4.41e-04	2.30e-04	–3.00e-04	9.07e-05
1.248	1.29e-08	1.27e-03	–5.17e-04	1.15e-04	–3.10e-04	7.92e-05

32.6.1.3.2 Receiver test mode

To facilitate the testing of the receiver in the presence of synchronous 100BASE-T2 alien NEXT, a special receiver test mode shall be required to allow for receiver alien NEXT tolerance and jitter testing. For a PHY with an MII, this mode shall be enabled by setting bit 9.13 (MASTER-SLAVE Control register) of the MII management register set to a 1. A PHY without an MII shall provide a means to enable this test mode. This mode shall not be overridden except by clearing bit 9.13 or resetting the PHY.

When the receive test mode is enabled, the receiver shall configure itself in SLAVE mode, continually attempt to bring its receiver up until successful receiver operation is achieved and transmit symbols in idle mode. For a PHY with an MII, when the receiver is properly detecting the received data (loc_rcvr_status=OK), it shall set bit 10.13 of the MII management register to 1 and reset the error count in bits 10.0 through 10.7 (MSB) to zero. The error count shall be incremented for every symbol error detected in the received idle sequence (where rem_rcvr_status is assumed to be OK). Upon loss of proper data reception, the receiver shall clear bit 10.13. A PHY without an MII shall provide a means to realize this function. The vendor shall provide a means to enable this mode for conformance testing.

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32.6.1.3.3 Receiver differential input signals

Differential signals received on the receive inputs that were transmitted within the specifications given in 32.6.1.2, and have then passed through a link as defined in 32.7, shall be translated into one of the PMA_UNITDATA.indication messages with an symbol error ratio less than 10^{-10} and sent to the PCS after link bring-up.

Performance shall be tested in at least two configurations: using a 100 m link segment conformant to 32.7 and with a link segment less than 1 m in length between transmitter and receiver.

32.6.1.3.4 Receiver Alien NEXT tolerance

Differential signals received from the test channel defined in 32.6.1.3.1 shall be detected with a symbol error ratio less than 10^{-8} when the PHY is in receiver test mode for the following combinations of channel and worst-case alien NEXT responses, as shown in Table 32-13.

Table 32-13—Receiver Alien NEXT test cases

Case	Cable channels	NEXT Channels			
		A1	A2	B1	B2
1	0 m	Alien NEXT 1	Alien NEXT 3	Alien NEXT 4	Alien NEXT 2
2	0 m	Alien NEXT 1	Alien NEXT 4	Alien NEXT 3	Alien NEXT 2
3	100 m	Alien NEXT 1	Alien NEXT 3	Alien NEXT 4	Alien NEXT 2
4	100 m	Alien NEXT 1	Alien NEXT 4	Alien NEXT 3	Alien NEXT 2

NOTE—Implementers will find it practically impossible to meet the requirements of this subclause without using some form of adaptive equalization and cyclostationary interference suppression.

32.6.1.3.5 Receiver timing jitter

For the test channels described below, the peak-to-peak value of RX_CLK zero-crossing jitter shall be less than 1.3 ns after the receiver is properly receiving the data and has set bit 9.13 of the MII management register set to 1. When the jitter waveform on RX_CLK is filtered by a high pass filter having the transfer function below,[67] the peak-to-peak value of the resulting filtered timing jitter shall be less than 0.8 ns.

Test channels:

Channels 1–4 are the test channels described in 32.6.1.3.1 with the four combinations of worst-case channel and alien NEXT responses tabulated in 32.6.1.3.4.

Channels 5–6 are the test channels described in 32.6.1.3.1 with the combinations of worst-case channel and alien NEXT responses tabulated in cases 1 and 2 of 32.6.1.3.4 plus the addition of 100 m of Category 3 compliant cable between the test channel fixture and the PHY under test.

$$H_{\text{jitterfilter}}(f) = \frac{jf}{jf + 1000} \qquad f \text{ in Hz}$$

The RX_CLK of the MII shall be made available for this test. A PHY without an MII shall provide an equivalent clock.

[67] "j" denotes the positive square root of –1.

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32.6.1.3.6 Common-mode noise rejection

While receiving packets from a compliant 100BASE-T2 transmitter, connected to all MDI pins, a receiver shall send the proper PMA_UNITDATA.indication messages to the PCS for any differential input signal E_s that results in a signal E_{dif} that meets 32.6.1.3.3 even in the presence of common-mode voltages E_{cm} (applied as shown in Figure 32–21). E_{cm} shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%-80%), connected to each of the pairs (BI_DA+, BI_DA-) and (BI_DB+, BI_DB-).

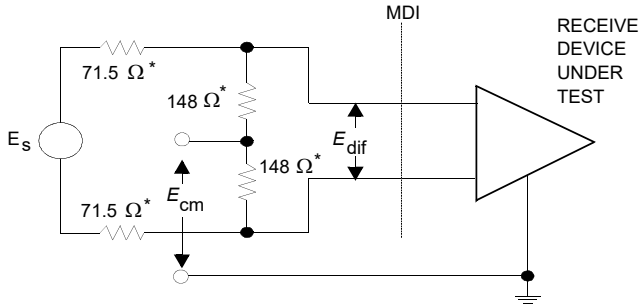

Figure 32–21—Receiver common-mode noise rejection test circuit

32.6.1.3.7 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a 5-level symbol rate within the range 25.000 MHz ± 0.01%.

32.6.1.4 MDI Specifications

32.6.1.4.1 MDI differential impedance

The differential impedance as measured at the MDI for each transmit/receive channel shall be such that any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 Ω is at least 17 dB below the incident signal over the frequency range 2.0 MHz to 6.5 MHz and at least 12.9–20 $\log_{10}(f/10)$ dB over the frequency range 6.5 MHz to 25 MHz (f in MHz). This return loss shall be maintained at all times when the PHY is transmitting data.

32.6.1.4.2 MDI impedance balance

Over the frequency range 2.0 MHz to 25.0 MHz, the common-mode to differential-mode impedance balance of each channel of the MDI shall exceed

$$29 - 17\log\left(\frac{f}{10}\right) \text{ dB}$$

where f is the frequency in MHz when the transmitter is transmitting idle mode data (transmit test mode 3).

The balance is defined as

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$$20\log\left(\frac{E_{cm}}{E_{dif}}\right)$$

where E_{cm} is an externally applied sine wave voltage as shown in Figure 32–22 and E_{dif} is the resulting waveform due only to the applied sine wave and not the transmitted data.[68]

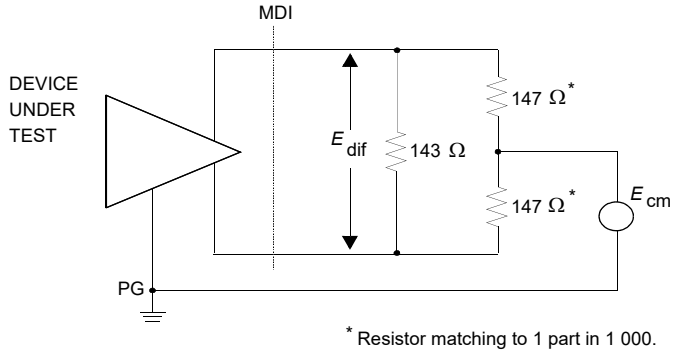

Figure 32–22—MDI impedance balance test circuit

NOTE—The balance of the test equipment (such as the matching of the test resistors) has to be insignificant relative to the balance requirements.

32.6.1.4.3 MDI common-mode output voltage

The implementer should consider any applicable local, national, or international regulations. Driving balanced cable pairs with high-frequency common-mode voltages may cause radiated emissions that may result in interference to other equipment. FCC conducted and radiated emissions tests may require that the magnitude of the total common-mode output voltage, E_{cm_out}, on any transmit circuit, when measured as shown in Figure 32–23, be less than a few millivolts when transmitting data.

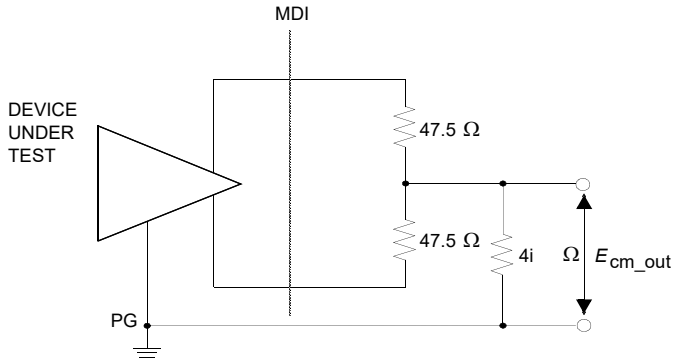

Figure 32–23—Common-mode output voltage test circuit

NOTE—The balance of the test equipment (such as the matching of the test resistors) has to be insignificant relative to the balance requirements.

[68]Triggered averaging can be used to separate the component due to the applied common-mode sine wave from the transmitted data component.

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32.6.1.4.4 MDI fault tolerance

Transmitters and receivers shall withstand without damage the application of short circuits across any MDI port for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Transmitters shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 32–24). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

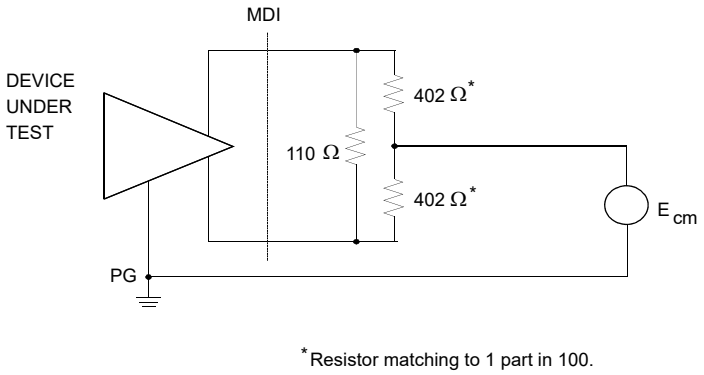

Figure 32–24—MDI fault tolerance test circuit

32.6.2 Power consumption

After 100 ms following PowerOn, the current drawn by the PHY shall not exceed 1.0 A when powered through the MII.

The PHY shall be capable of operating from all voltage sources allowed by Clause 22, including those current limited to 1.0 A, as supplied by the DTE or repeater through the resistance of all permissible MII cabling.

The PHY shall not introduce extraneous signals on the MII control circuits during normal power-up and power-down.

While in power-down mode, the PHY is not required to meet any of the 100BASE-T2 performance requirements.

32.7 Link segment characteristics

100BASE-T2 employs a dual duplex transmission system, i.e., two full duplex channels are used simultaneously to transmit data. The use of the term *link segment* in this clause refers to two duplex channels and the specifications for a link segment apply individually to each of the two duplex channels. Furthermore, the term duplex channel will be used to refer a single channel of the dual duplex link segment.

100BASE-T2 is designed to allow use of the pairs of the cabling other than the two used for the full duplex channels of the 100BASE-T2 service. Services supported for use in the other pairs are as follows:

a) 100BASE-T2
b) 10BASE-T
c) Digital phone services compliant with the ITU-T Recommendation I.430 and ATIS-0600605 and ATIS-0600601

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32.7.1 Cabling

Cabling and installation practices generally suitable for use with this standard appear in ISO/IEC 11801. Exceptions, notes, and additional requirements are as listed below.

a) 100BASE-T2 uses a star topology. Balanced cabling is used to connect PHY entities.
b) 100BASE-T2 is an ISO 11801 class C application, with additional installation requirements and transmission parameters specified in 32.7.2–32.7.4. The width of the PAM5 × 5 transmit spectrum is approximately 25 MHz (as shown in Figure 32–19). The aggregate data rate for two pairs using PAM5 × 5 coding is 100 Mb/s.
c) 100BASE-T2 shall use 2 pairs of balanced cabling, Category 3 or better, with a nominal characteristic impedance of 100 Ω.
d) When using Category 3 cabling for the link segment, Clause 32 recommends, but does not require, the use of Category 4 or better connecting hardware, patch cords and jumpers. The use of Category 4 or better connecting hardware increases the link segment composite NEXT loss, composite ELFEXT loss and reduces the link segment insertion loss. This lowers the link segment crosstalk noise which in turn decreases the probability of errors.
e) The use of shielding is outside the scope of this standard.
f) The use of other cabling systems is discussed in Annex 32A.

32.7.2 Link transmission parameters

Unless otherwise specified, link segment testing shall be conducted using source and load impedances of 100 Ω.

The tolerance on the poles of the test filter used in this clause shall be ± 1%.

32.7.2.1 Insertion loss

The insertion loss of a link segment shall be no more than 14.6 dB at all frequencies between 2 and 16 MHz. This consists of the attenuation of the balanced cabling pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the link segment. The insertion loss specification shall be met when the link segment is terminated in source and load impedances that satisfy 32.6.1.4.1.

NOTE—The loss of PVC-insulated cabling exhibits significant temperature dependence. At temperatures greater than 40 ^{o}C, it may be necessary to use a less temperature-dependent cabling, such as many Fluorinated Ethylene Propylene (FEP), Polytetrafluoroethylene (PTFE), or Perfluoroalkoxy (PFA) plenum-rated cabling.

32.7.2.2 Differential characteristic impedance

The cable used in the links shall meet the requirements for characteristic impedance specified in ISO/IEC 11801. Connecting hardware shall meet the return loss requirements for connecting hardware specified in ISO/IEC 11801.

32.7.2.3 Coupling parameters

In order to limit the noise coupled into a duplex channel from an adjacent duplex channel, Near-End Crosstalk (NEXT) loss and Equal Level Far-End Crosstalk (ELFEXT) loss are specified for each link segment. In addition, since two dual-duplex connections may co-exist in a 4-pair cabling and a receiver on a duplex channel will be disturbed by crosstalk from one to three other duplex (or simplex) channels, Multiple-Disturber NEXT loss and Multiple-Disturber ELFEXT loss are also specified. When a 10BASE-T service is used within the same cabling, a restriction on the allowable NEXT loss to Insertion Loss (NIR) of the cabling is required and is specified in 32.7.2.3.5.

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32.7.2.3.1 Differential near-end crosstalk (NEXT) loss

The differential Near-End Crosstalk (NEXT) loss between the two duplex channels of a link segment is specified in order to limit the crosstalk noise at the near end of a link segment to meet the symbol error ratio objective specified in 32.1 and the noise specifications of 32.7.3. The NEXT loss between the two duplex channels of a link segment shall be at least $19.3 - 16.6\log_{10}(f/16)$ (where f is the frequency in MHz) over the frequency range 2 MHz to 16 MHz.

32.7.2.3.2 Multiple-disturber NEXT (MDNEXT) loss

Since two dual duplex applications (connections) may exist in a 4-pair cabling system, a received signal may be disturbed by multiple alien NEXT signals. The MDNEXT loss between each link segment duplex channel and the two alien data carrying duplex channels shall be at least $19.0 - 16.6\log_{10}(f/16)$ dB (where f is the frequency in MHz) over the frequency range 2.0 MHz to 16 MHz. MDNEXT is computed as the power sum of the individual NEXT losses. This specification is consistent with two disturbers, each with a NEXT loss of at least $22.0 - 16.6\log_{10}(f/16)$.

NOTE—Since the self NEXT noise from the other duplex channel of a connection can be cancelled using digital signal processing techniques whereas the alien NEXT noise from an alien connection can not be cancelled in the same fashion, the self NEXT noise is treated differently than the alien NEXT noise and is not included in the MDNEXT calculation.

32.7.2.3.3 Equal level far-end crosstalk loss (ELFEXT)

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk noise at the far end of a link segment to meet the symbol error ratio objective specified in 32.1 and the noise specifications of 32.7.3. Far-End Crosstalk (FEXT) noise is the crosstalk noise that appears at the far end of one of the duplex channels which is coupled from one of the duplex channels with the noise source (transmitters) at the near end. ELFEXT loss is the ratio of the data signal to FEXT noise at the far end output of a duplex channel. To limit the FEXT noise from an adjacent duplex channel, the ELFEXT loss between each duplex channel shall be greater than $20.9 - 20\log_{10}(f/16)$ dB (where f is the frequency in MHz) over the frequency range 2 MHz to16 MHz. ELFEXT loss at frequency f and distance l is defined as

$$ELFEXT\_Loss(f,l) = 20\log_{10}(V\text{pds}/V\text{pcn}) - SLS\_Loss(\text{dB})$$

where Vpds = peak voltage of disturbing signal (near-end transmitter), Vpcn = peak crosstalk noise at far-end of disturbed channel, and SLS_Loss = insertion loss of the disturbing channel.

32.7.2.3.4 Multiple-disturber ELFEXT (MDELFEXT) loss

Since two duplex channels are used to transfer data between PHYs and two connections can exist in a 4-pair cabling, the FEXT noise that is coupled into a data carrying duplex channel is from one to three disturbers. The MDELFEXT loss between a duplex channel and the other data carrying duplex channels shall be greater than $19.9 - 20\log_{10}(f/16)$ (where f is the frequency in MHz) over the frequency range 2 MHz to 16 MHz.This specification is consistent with three disturbers, one with a FEXT loss of at least $20.9 - 20\log_{10}(f/16)$ and two with a FEXT loss of at least $27.0 - 20\log_{10}(f/16)$.

MDELNEXT is computed as the power sum of the individual FEXT losses.

32.7.2.3.5 10BASE-T NEXT loss to insertion loss ratio requirement

The objective of this specification is to support the coexistence of a 100BASE-T2 link segment and a 10BASE-T link segment in a 4-pair cable. When a 100BASE-T2 link segment operates in the same 4-pair cable with a 10BASE-T link segment, each 100BASE-T2 duplex channel will receive alien NEXT noise signals from the 10BASE-T link segment. To ensure reliable operation, a minimum signal-to-noise ratio has to

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be maintained. This minimum signal-to-noise ratio is assured by meeting the following NEXT loss to insertion loss ratio (NIR).

NIR is defined by the following equation:

$$NIR\ (\text{dB}) = (AdjustedNEXTLoss - InsertionLoss_{6\ \text{MHz}})$$

where $InsertionLoss_{6\ \text{MHz}}$ is the maximum of the insertion loss at 6 MHz of the two duplex channels of the 100BASE-T2 link segment and *AdjustedNEXTLoss* is determined by the following algorithm:

AdjustedNEXTLoss Algorithm

Step 1. Measure the NEXT loss as a function of frequency over the range 1 MHz to 16 MHz for each of the six pair combinations between the four pairs of the cabling. The maximum spacing in frequency of the samples shall be 250 kHz.

Step 2. Add $16.6\log_{10}(f/16)$ to the NEXT loss measurements (where f is frequency in MHz) to normalize the NEXT loss as a function of frequency.

Step 3. Determine the minimum value of the normalized NEXT loss across the frequency range over all pair combinations. The minimum value is the AdjustedNEXTLoss.

The NIR shall be greater than 19.4 dB.

32.7.2.4 Delay

Since 100BASE-T2 sends information over two duplex channels in parallel, the propagation delay of each channel and the difference in delay are specified to comply with network round-trip delay of the two channels and ensure proper decoding by receivers, respectively.

32.7.2.4.1 Maximum link delay

The propagation delay of a link segment shall not exceed 5.7 ns/m at all frequencies between 2 MHz and 25 MHz.

32.7.2.4.2 Difference in link delays

The difference in propagation delay, or skew, under all conditions, between the two duplex channels of a link segment shall not exceed 90 ns at all frequencies between 2 MHz and 25 MHz. It is a further functional requirement that, once installed, the skew between the duplex links due to environmental conditions shall not vary more than ± 20 ns, within the above requirement.

32.7.3 Noise

The noise level on the link segments shall be such that the cabling noise requirements which follow are met. The noise environment consists generally of a main contributor, self-induced and alien near-end crosstalk noise, and a lessor contributor, far-end crosstalk noise.

The noise environment for 100BASE-T2 can consist of the following elements:

a) Echo from the local transmitter on the same pair (duplex channel). Echo is caused by the hybrid used to achieve simultaneous bidirectional transmission of data in the T2 system and by impedance mismatches in the link segment. It is practically impossible to achieve robust performance without using echo cancellation to reduce this noise to a small residual. Echo cancellation is possible since the symbols transmitted from the disturbing local transmitter are available to the cancellation processor.

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b) Near-end crosstalk (NEXT) noise from the local transmitter on the other pair (duplex channel) of the link segment. This is often referred to as self NEXT noise since the source is from the same link segment. NEXT noise cancellation is typically used to reduce this noise to a small residual. NEXT noise cancellation is possible since the symbols transmitted from the disturbing local transmitter are available to the cancellation processor.

c) Far-end crosstalk (FEXT) noise from the remote transmitters on the other pair (duplex channel) of the link segment. This is often referred to as self FEXT noise since the source is from the same link segment. Self FEXT noise can not be cancelled in the same way as echo and self NEXT noise since the symbols from the remote transmitter are not immediately available; however, in the link configurations used for 100BASE-T2, self FEXT noise is much smaller than self NEXT noise and can generally be neglected.[69]

d) Noise from non-idealities in the duplex channels, transmitters and receivers; for example, DAC/ADC non-linearity, electrical noise (shot and thermal) and non-linear channel characteristics.

e) Noise from sources outside the cabling which couple into the link segment via electric and magnetic fields.

f) Noise from services in adjacent wire pairs in the same cable sheath. These services generate near- and far-end crosstalk and are often referred to as alien NEXT noise and alien FEXT noise since the sources are not from the link segment of the disturbed duplex channel. Since the transmitted symbols from an alien NEXT noise source are not available to the PHY of the disturbed duplex channel, it is not possible to cancel the alien NEXT noise as can be done for self NEXT noise. If the alien NEXT noise is from a 100BASE-T2 transceiver, a technique termed cyclostationary interference suppression can be used to suppress the alien NEXT noise. It will be practically impossible achieve reliable operation in the presence of alien NEXT noise meeting the limits of the specifications in subclause 32.6 without using some form of cyclostationary interference suppression. 10BASE-T can not be suppressed and therefore an additional constraint has been placed on the link (see subclause 32.7.2.3.5) to ensure adequate signal to noise levels for reliable performance. Digital phone services compliant with the ITU-T Recommendation I.430 and ATIS-0600605 and ATIS-0600601 also can not be suppressed but produce substantially smaller crosstalk than 10BASE-T and thus do not require any additional constraints on the link.

100BASE-T2 supports three types of service in adjacent pairs of the same cable: 100BASE-T2, 10BASE-T, and digital phone service compliant with the ISDN-BR U and S/T interfaces. Analog phone service is not supported since the noise generated during off-hook transitions and ringing source from older PBX equipment can cause bit errors to occur.

NOTE—Due to the use of noise cancellation, cyclostationary interference suppression and the use of adaptive equalization, there is no meaningful way to add up the noises at the input to the receiver into an overall noise level and simulation of a design is required to determine the contribution of each source to the final error at the symbol decision point.

32.7.3.1 Near-end crosstalk noise

The MDNEXT (Multiple-Disturber Near-End Crosstalk) noise on a duplex channel from an alien connection depends on the signal spectrum on the alien channels and the crosstalk between the alien channels and the disturbed channel.

The MDNEXT noise on each duplex link of a link segment shall not exceed 182 mVp.

This specification is compatible with the following assumptions:

[69]Additionally, FEXT noise may be suppressed to some degree via cyclostationary interference suppression; however, in the presence of alien NEXT noise, the equalizer will be primarily suppressing the alien NEXT noise.

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a) Two disturbing alien pairs with a NEXT loss greater than 22.0 dB at 16 MHz
b) All disturbers combined on a power sum basis

The MDNEXT noise is the noise measured at the output of a filter connected to the output of the near end of a disturbed link segment using maximum level 100BASE-T2 transmitters attached to the near end of an alien disturbing link segment. Each continuous transmit signal is generated by a transceiver in idle mode meeting the data scrambling and encoding rules in 32.3, e.g., a transmitter in transmit test mode 3.

32.7.3.2 Far-end crosstalk noise

The MDFEXT (Multiple-Disturber Far-End Crosstalk) noise on a duplex channel depends on the signal spectrum on the disturbing channels and the various crosstalk losses between those channels and the disturbed channel.

The MDFEXT noise on a link segment shall not exceed 54.4 mVp.

This specification is compatible with the following assumptions:

a) One disturbing pair with ELFEXT (Equal Level Far-End Crosstalk) loss greater than 20.9 dB at 16 MHz
b) Two additional disturbers with ELFEXT (Equal Level Far-End Crosstalk) loss greater than 27.0 dB at 16 MHz
c) All disturbers combined on a power sum basis

The MDFEXT noise is the noise measured at the output of a filter connected to the output of the far end of a disturbed link segment using maximum level 100BASE-T2 transmitters attached to the near end of the other duplex channel of the link segment and both duplex channels of an alien disturbing link segment. Each continuous transmit signal is generated by a transceiver in idle mode meeting the data scrambling and encoding rules in 32.3, e.g., a transmitter in transmit test mode 3.

The filter is a 5th order Butterworth filter with a 3 dB cutoff at 23 MHz.

32.7.3.3 External coupled noise

Noise coupled from external sources, measured at the output of a filter connected to the output of the near end of a disturbed link segment shall not exceed 25 mV peak.[70]

The filter is a 5th order Butterworth filter with a 3 dB cutoff at 23 MHz.

32.7.4 Installation practice

32.7.4.1 Connector installation practices

The amount of untwisting in a pair as a result of termination to connecting hardware should be no greater than 25 mm (1.0 in.) for Category 3 cabling. This is the same value recommended in ISO/IEC 11801 for Category 4 connectors.

32.7.4.2 Restrictions on use of Category 3 cabling with more than four pairs

Jumper cabling, or horizontal runs, made from more than four pairs of Category 3 cabling shall not be used.

[70]This assumes the link has worst-case attenuation and alien NEXT and that the noise has the worst possible properties. In the absence of alien NEXT the tolerance to external noise sources is substantially increased. Tolerance to stationary noise such as continuous wave interference from AM radio can be substantially higher since the equalizer can notch out frequencies with poor signal-to-noise ratios. Tolerance to isolated impulse noise events is also typically much higher and dependent on the shape of the impulse.

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32.7.4.3 Restrictions on use of Category 5 cabling with up to 25 pairs

Cables made from up to 25 pairs of Category 5 cable are allowed. Such cables, if used, shall be limited in length to no more than 90 m total. The services in the cable shall be limited to any combination 100BASE-T2, 10BASE-T and digital phone services compliant with the ITU-T Recommendation I.430 and ATIS-0600605 and ATIS-0600601 interfaces up to a total of 12 services in the cable.

32.8 MDI specification

This subclause defines the MDI. The link topology requires a crossover function between PMAs. Implementation and location of this crossover are also defined in this subclause.

32.8.1 MDI connectors

Eight-pin connectors meeting the requirements of section 3 and Figures 1–4 of IEC 60603-7, Detail Specification for Connectors, 8-Way shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figures 32–25 and 32–26. Table 32–14 shows the assignment of PMA signals to connector contacts for PHYs.

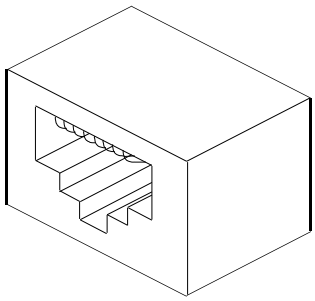

Figure 32–25—MDI connector

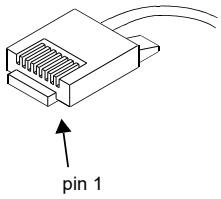

Figure 32–26—Balanced cabling connector

32.8.2 Crossover function

Although the crossover function is not required for successful operation of 100BASE-T2, it is a functional requirement that a crossover function be implemented in every link segment to support the operation of Auto-Negotiation. The crossover function connects the transmitters of one PHY to the receivers of the PHY at the other end of the link segment. Crossover functions may be implemented internally to a PHY or elsewhere in the link segment. For a PHY that does not implement the crossover function, the MDI labels in the last column of Table 32–14 refer to its own internal circuits (second column). For PHYs that do implement the internal crossover, the MDI labels in the last column of Table 32–14 refer to the internal circuits of the remote PHY of the link segment. Additionally, the MDI connector for a PHY that implements the crossover function shall be marked with the graphical symbol X. The crossover function specified here is compatible with the crossover function specified in 14.5.2 for pairs TD and RD.

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Table 32–14—Assignment of PMA signals to MDI pin-outs

Contact	PHY without internal crossover (100BASE-T2 operation)	PHY with internal crossover (Auto-Negotiation operation)	MDI labeling requirement
1	BI_DA+	BI_DB+	BI_DA+
2	BI_DA-	BI_DB-	BI_DA-
3	BI_DB+	BI_DA+	BI_DB+
4	Not used	Not used	
5	Not used	Not used	
6	BI_DB-	BI_DA-	BI_DB-
7	Not used	Not used	
8	Not used	Not used	

When a link segment connects a DTE to a repeater, it is recommended the crossover be implemented in the PHY local to the repeater. If both PHYs of a link segment contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the PHYs. When both PHYs contain internal crossovers, it is further recommended in networks in which the topology identifies either a central backbone segment or a central repeater that the PHY furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable, or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

32.9 System considerations

The repeater unit specified in Clause 27 forms the central unit for interconnecting 100BASE-T2 twisted-pair links in networks of more than two nodes. It also provides the means for connecting 100BASE-T2 balanced cabling links to other 100 Mb/s baseband segments. The proper operation of a CSMA/CD network requires that network size be limited to control round-trip propagation delay as specified in Clause 29.

When operated in Full Duplex mode where CSMA/CD requirements do not apply, 100BASE-T2 balanced cabling links are limited to 100 m as per ISO/IEC 11801.

32.10 Environmental specifications

32.10.1 General safety

NOTE—Since September 2003, maintenance changes are no longer being considered for this clause. Since February 2021, safety information is in J.2.

All equipment meeting this standard shall conform to IEC 60950.

32.10.2 Network safety

This clause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

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a) Direct contact between LAN components and power, lighting, or communications circuits
b) Static charge buildup on LAN cabling and components
c) High-energy transients coupled onto the LAN cabling system
d) Voltage potential differences between safety grounds to which various LAN components are connected

Such electrical safety hazards have to be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures have to be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

32.10.2.1 Installation

It is a mandatory functional requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

32.10.2.2 Grounding

Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection.

WARNING

It is assumed that the equipment to which the PHY is attached is properly grounded, and not left floating nor serviced by a "doubly insulated, ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety, are beyond the scope of this standard.

32.10.2.3 Installation and maintenance guidelines

It is a mandatory functional requirement that, during installation and maintenance of the cabling plant, care be taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

32.10.2.4 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 100BASE-T2 equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply.

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.

Ringing voltage is a composite signal consisting of an AC component and a DC component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The DC component is 56 Vdc with 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 100BASE-T2 equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 100BASE-T2 transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. There-

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fore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

32.10.3 Environment

32.10.3.1 Electromagnetic emission

The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

32.10.3.2 Temperature and humidity

The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

32.10.4 Cabling specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801.

32.11 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability in Mb/s
b) Power level in terms of maximum current drain (for external PHYs)
c) Port type (i.e., 100BASE-T2)
d) Any applicable safety warnings

See also 32.8.2.

32.12 Delay constraints

Proper operation of a CSMA/CD LAN, operating in half duplex mode, demands that there be an upper bound on the propagation delays through the network. This implies that MAC, PHY and repeater implementations conform to certain delay minima and maxima, and that network planners and administrators conform to constraints regarding the cabling topology and concatenation of devices. MAC constraints are contained in Clause 21. Topological constraints are contained in Clause 29. In the full duplex mode of operation, DTEs are not required to conform to the constraints specified in this clause.

The reference point for all MDI measurements is the peak point of the mid-cell transition corresponding to the reference code-bit, as measured at the MDI. Although 100BASE-T2 output is scrambled, it is assumed that these measurements are made via apparatuses that appropriately account for this.

32.12.1 PHY delay constraints (exposed MII)

Every 100BASE-T2 PHY with an exposed MII shall comply with the bit delay constraints specified in Table 32–15. These figures apply for all 100BASE-T2 PMDs.

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Table 32–15—MDI to MII delay constraints (exposed MII)

Sublayer Measurement Points	Event	Min (bits)	Max (bits)	Input Timing Reference	Output Timing Reference
MII ⇔ MDI	TX_EN Sampled to MDI Output	7	9	TX_CLK rising	1st symbol of SSD
	MDI input to CRS assert		25	1st symbol of SSD	
	MDI input to CRS deassert		29	1st ONE	
	MDI input to COL assert		25	1st symbol of SSD	
	MDI input to COL deassert		29	1st symbol of SSD	
	TX_EN sampled to CRS assert	0	4	TX_CLK rising	
	TX_EN sampled to CRS deassert	0	16	TX_CLK rising	

32.12.2 DTE delay constraints (unexposed MII)

Every 100BASE-T2 DTE with no exposed MII shall comply with the bit delay constraints specified in Table 32–16. These figures apply for all 100BASE-T2 PMDs.

Table 32–16—DTE delay constraints (unexposed MII)

Sublayer Measurement Points	Event	Min (bits)	Max (bits)	Input Timing Reference	Output Timing Reference
MAC ⇔ MDI	MAC transmit start to MDI output		13		1st symbol of SSD
	MDI input to MDI output (worst-case non-deferred transmit)		50	1st symbol of SSD	1st symbol of SSD
	MDI input to collision detect		33	1st symbol of SSD	
	MDI input to MDI output = Jam (worst-case collision response)		50	1st symbol of SSD	1st symbol of SSD

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32.13 Protocol implementation conformance statement (PICS) proforma for Clause 32, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2[71]

The supplier of a protocol implementation that is claimed to conform to Clause 32, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2, shall complete the following protocol implementation conformance statement (PICS) proforma.

Instructions for interpreting and filling out the PICS proforma may be found in Clause 21.

32.13.1 Identification

32.13.1.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1— Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

32.13.1.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2018, Clause 32, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exceptions items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2018.)	

Date of Statement	

[71] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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32.13.2 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*MII	Exposed MII interface	32.1.3.2	O	Yes [ ] No [ ]	Devices supporting this option also have to support the PCS option.
PC	PHY Control functions	32.2	M	Yes [ ]	Required for proper operation of the PHY.
*PCS	PCS functions	32.3	O	Yes [ ] No [ ]	Required for integration with DTE or MII.
*PMA	Exposed PMA service interface	32.4.2	O	Yes [ ] No [ ]	Required for integration into symbol level repeater core.
NWY	Support for Auto-Negotiation (Clause 28)	32.1.3.4	M	Yes [ ]	Required
*INS	Installation/cabling	32.7.4	O	Yes [ ] No [ ]	Items marked with INS include installation practices and cabling specifications not applicable to a PHY manufacturer.

32.13.3 Compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
CCO1	Compatibility at the MDI	32.1.3.1	M	Yes [ ]	
CCO2	Auto-Negotiation required	32.1.3.4	M	Yes [ ]	
CCO3	State diagrams prevail	32.1.4	M	Yes [ ]	In discrepancy between text and state diagram.

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32.13.4 PHY control function

Item	Feature	Subclause	Status	Support	Value/Comment
PC01	PHY Control shall	32.2.1	M	Yes [ ]	Comply with the state diagram descriptions given in Figure 32–5.
PC02	PHY Control shall	32.2.2.1.2	M	Yes [ ]	Generate PHYC_CONFIG.indication messages synchronously with every MII TX_CLK cycle.
PC03	Upon receipt of the PHYC_CONFIG primitive, PCS Transmit and PMA Clock Recovery shall	32.2.2.1.3	M	Yes [ ]	Perform their functions in master or slave configuration according to the value of the parameter config.
PC04	PHY Control shall	32.2.2.2.2	M	Yes [ ]	Generate PHYC_LOCRXSTATUS.indication messages synchronously with every MII TX_CLK cycle.
PC05	Upon reception of the PHYC_LOCRXSTATUS.indication primitive, PCS Transmit shall	32.2.2.2.3	M	Yes [ ]	Perform its function according to the value assumed by the parameter loc_cvr_status.
PC06	PHY Control shall	32.2.2.3.2	M	Yes [ ]	Generate PHYC_TXMODE.indication messages synchronously with every MII TX_CLK cycle.
PC07	Upon receipt of the PHYC_TXMODE.indication primitive, the PCS shall	32.2.2.3.3	M	Yes [ ]	Perform its Transmit function as described in 32.3.1.2.
PC8	The PCS shall	32.2.2.3.2	M	Yes [ ]	Generate PHYC_RXSTATUS.request messages synchronously with signals received at the MDI.
PC9	The PCS shall	32.2.2.4.2	M	Yes [ ]	Generate PHYC_REMRXSTATUS.request messages synchronously with signals received at the MDI.
PC10	PCS Transmit shall	32.2.3	M	Yes [ ]	Send quinary symbols according to the value assumed by tx_mode.
PC11	When tx_mode assumes the value of SEND_N	32.2.3	M	Yes [ ]	Transmission of sequences of quinary symbols representing an MII data stream, the idle mode, or control sequences shall take place.
PC12	When tx_mode assumes the value of SEND_I	32.2.3	M	Yes [ ]	Transmission of sequences of quinary symbols representing the idle mode shall take place.

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32.13.5 Physical Coding Sublayer (PCS) or Physical Medium Attachment (PMA) sublayer

32.13.5.1 PCS transmit functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCT01	The PCS shall	32.3.5.1	M	Yes [ ]	Implement the Transmit process as depicted in Figure 32–12 including compliance with the associated state variables specified in 32.3.4.
PCT02	PCS Transmit function shall	32.3.1.2	M	Yes [ ]	Conform to the PCS Transmit state diagram in Figure 32–12.
PCT03	If the parameter config provided to the PCS by the PHY Control function via the PHY-C_CONFIG.indication message assumes the value MASTER, PCS Transmit shall	32.3.1.2.1	M	Yes [ ]	Employ the transmitter side-stream scrambler generator polynomial specified for use with MASTER in 32.3.1.2.1.
PCT04	If the parameter config provided to the PCS by the PHY Control function via the PHY-C_CONFIG.indication message assumes the value SLAVE, PCS Transmit shall	32.3.1.2.1	M	Yes [ ]	Employ the transmitter side-stream scrambler generator polynomial specified for use with SLAVE in 32.3.1.2.1.
PCT05	Transmission of quinary symbol pairs over wire pairs	32.3.1.2	M	Yes [ ]	Symbols A_n and B_n are transmitted over BI_DA and BI_DB respectively.

32.13.5.2 PCS receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR01	The PCS shall	32.3.5.2	M	Yes [ ]	Implement the Receive process as depicted in Figure 32–13 including compliance with the associated state variables as specified in 32.3.4.
PCR02	PCS Receive function shall	32.3.1.3	M	Yes [ ]	Conform to the PCS Receive state diagram shown in Figure 32–13.
PCR03	For side-stream descrambling, the MASTER PHY shall employ	32.3.1.3.1	M	Yes [ ]	The receiver scrambler generator polynomial specified for MASTER operation in 32.3.1.3.1.
PCR04	For side-stream descrambling, the SLAVE PHY shall employ	32.3.1.3.1	M	Yes [ ]	The receiver scrambler generator polynomial specified for SLAVE operation in 32.3.1.3.1.

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32.13.5.3 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	The PCS Reset function shall	32.3.1.1	M	Yes [ ]	Be executed any time “power on,” receipt of a request for reset from the management entity, or receipt of a request for reset from the PHY Control occur.
PCO2	THE PCS shall	32.3.1.4	M	Yes [ ]	Implement the PCS Carrier Sense function shown in Figure 32–14.
PCO3	PCS Carrier Sense function shall	32.3.5.3	M	Yes [ ]	Comply with the PCS Carrier Sense state diagram shown in Figure 32–14 including compliance with the associated state variables specified in 32.3.4.
PCO4	MII COL signal shall be asserted while	32.3.1.5	M	Yes [ ]	A PCS collision is being detected.
PCO5	The MII signal COL shall remain deasserted.	32.3.1.5	M	Yes [ ]	A PCS collision is not being detected.
PCO6	No spurious PCS management entity signals shall be emitted onto the MDI while the PHY is held in power down mode as defined in 22.2.4.1.5, independently of the value of TX_EN, or when released from power down mode, or when power is first applied to the PHY.	32.3.2.2	M	Yes [ ]	
PCO7	Frames passed from the PCS to the PMA sublayer shall	32.3.3	M	Yes [ ]	Have the structure shown in Figure 32–11.
PCO8	TX_CLK shall be generated	32.3.4.2	M	Yes [ ]	Synchronously with symb_-timer with tolerance as specified in 32.6.1.2.6.

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32.13.5.4 PMA functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMF1	PMA Reset function shall be executed	32.4.1.1.1	M	Yes [ ]	At power on and upon receipt of a reset request from the management entity.
PMF2	PMA transmit shall continuously transmit	32.3.1.2	M	Yes [ ]	Onto the MDI pulses modulated by the quinary symbols given by tx_symb_vector[BI_DA] and tx_symb_vector[BI_DB] respectively.
PMF3	The two transmitters shall be driven by the same transmit clock.	32.4.1.1.2	M	Yes [ ]	
PMF4	PMA Transmit function will follow	32.4.1.1.2	M	Yes [ ]	The mathematical description given in 32.4.1.2.1.
PMF5	PMA Transmit shall comply with	32.4.1.1.2	M	Yes [ ]	The electrical specifications given in 32.6.
PMF6	PMA Receive function shall translate	32.4.1.1.3	M	Yes [ ]	The signals received on pairs BI_DA and BI_DB into the PMA_UNITDATA.indication parameter rx_symb_vector with a symbol error ratio of less than one part in 10^{10}.
PMF7	The Link Monitor function shall	32.4.1.1.4	M	Yes [ ]	Comply with the state diagram shown in Figure 32–17.
PMF8	Clock Recovery function shall provide	32.4.1.1.5	M	Yes [ ]	A clock suitable for synchronous signal sampling on each line so that the symbol error ratio indicated in 32.4.1.1.3 is achieved.
PMF9	The waveform obtained at the MDI shall comply with	32.4.1.2.1	M	Yes [ ]	The electrical specifications given in 32.6.
PMF10	The two signals received on pair BI_DA and BI_DB shall be processed within the PMA Receive function to yield	32.4.1.2.2	M	Yes [ ]	The quinary received symbols rx_symb_vector[BI_DA] and rx_symb_vector[BI_DB].

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32.13.5.5 PMA service interface

Item	Feature	Subclause	Status	Support	Value/Comment
PMS1	Continuous generation of PMA_TYPE	32.4.1.2.2	M	Yes [ ]	
PMS2	Generation of PMA_UNIT-DATA.indication (SYM-B_PAIR) messages	32.4.2.3.2	M	Yes [ ]	Synchronous with data received at the MDI.
PMS3	The PMA shall generate	32.4.2.5.2	M	Yes [ ]	PMA_LINK.indication to indicate the value of link_status.
PMS4	Effect of receipt of PMA_LINK.request messages	32.4.2.4.3	M	Yes [ ]	While link_control=SCAN_-FOR_CARRIER or link_control=DISABLE, the PMA shall report link_status=fail; while link_control=ENABLE, PHY determines operations to be performed by the PHY.

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32.13.5.6 Management functions

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	A 100BASE-T2 PHY shall	32.5	M	Yes [ ]	Use register addresses 9 and 10 for its control and status functions.
MF2	Register 9 shall	32.5.3.1	M	Yes [ ]	Provide values as specified in Table 32–4.
MF3	A PHY with 100BASE-T2 capability shall	32.5.3.1.1	M	Yes [ ]	Be placed in transmitter test mode 1 when bit 9.15 is set to logic zero and bit 9.14 is set to logic one.
MF4	A PHY with 100BASE-T2 capability shall	32.5.3.1.1	M	Yes [ ]	Be placed in transmitter test mode 2 when bit 9.15 is set to logic one and bit 9.14 is set to logic zero.
MF5	A PHY with 100BASE-T2 capability shall	32.5.3.1.1	M	Yes [ ]	Be placed in transmitter test mode 3 when bit 9.15 is set to logic one and bit 9.14 is set to logic one.
MF6	A PHY with 100BASE-T2 capability shall	32.5.3.1.2	M	Yes [ ]	Be placed in receiver test mode when bit 9.13 is set to logic one.
MF7	MASTER-SLAVE configuration negotiation will determine PHY configuration if	32.5.3.1.3	M	Yes [ ]	Bit 9.12 is set to logic zero.
MF8	Manual MASTER-SLAVE configuration will be set manually using bit 9.11 to set the value if	32.5.3.1.3	M	Yes [ ]	Bit 9.12 is set to logic one.
MF9	Bit 9.11 shall be used to report the results of manual MASTER-SLAVE configuration.	32.5.3.1.4	M	Yes [ ]	
MF10	Bit 9.10 shall	32.5.3.1.5	M	Yes [ ]	Be set to logic zero if the PHY is a DTE device and be set to logic one if the PHY is a repeater device port.
MF11	Bits 9.9:0 shall	32.5.3.1.6	M	Yes [ ]	Be set to logic zero.
MF12	Bits 9.9:0 shall be ignored when read	32.5.3.1.6	M	Yes [ ]	
MF13	A PHY shall return a value of zero for bits 9.9:0.	32.5.3.1.6	M	Yes [ ]	
MF14	Register 10 shall	32.5.3.1.2	M	Yes [ ]	Be used as shown in Table 32–5.
MF15	Bits 10.11:8 shall	32.5.3.2.5	M	Yes [ ]	Be set to logic zeros by default.
MF16	The MASTER-SLAVE Manual Configuration Fault bit shall be implemented	32.5.3.2.1	M	Yes [ ]	With a latching function, such that the occurrence of a MASTER-SLAVE Manual Configuration Fault will cause the MASTER-SLAVE Manual Configuration Fault bit to be set and remain set until cleared.

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32.13.5.6 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF17	The MASTER-SLAVE Manual Configuration Fault bit shall be cleared	32.5.3.2.1	M	Yes [ ]	Each time register 10 is read by the management interface.
MF18	The MASTER-SLAVE Management Configuration Fault bit shall also be cleared by	32.5.3.2.1	M	Yes [ ]	A 100BASE-T2 PMA reset.
MF19	Bits 10:11:8 shall	32.5.3.2.5	M	Yes [ ]	Be ignored when read.
MF20	A PHY shall return a value of zero for bits10.11:8.	32.5.3.2.5	M	Yes [ ]	

32.13.5.7 100BASE-T2 specific Auto-Negotiation requirements

Item	Feature	Subclause	Status	Support	Value/Comment
AN1	Base Page will be followed with	32.5.4.2	M	Yes [ ]	A Next Page with a message code containing the 100BASE-T2 Technology Ability Message Code (7).
AN2	Message Next Page shall be followed with	32.5.4.2	M	Yes [ ]	Unformatted Message Next Page containing the 100BASE-T2 Technology Ability Fields as described in Table 32–6.
AN3	MASTER-SLAVE relationship shall be determined by	32.5.4.3	M	Yes [ ]	Using Table 32–7with the 100BASE-T2 Technology Ability Next Page bit values specified in Table 32–6.
AN4	A seed counter shall be provided to	32.5.4.3	M	Yes [ ]	Track the generation of seeds.
AN5	At startup, the seed counter shall be set to	32.5.4.3	M	Yes [ ]	Zero.
AN6	The seed counter shall be incremented	32.5.4.3	M	Yes [ ]	Every time a new random seed is sent.
AN7	Maximum seed attempts before declaring a MASTER_SLAVE configuration Resolution Fault	32.5.4.3	M	Yes [ ]	Seven.
AN8	During MASTER_SLAVE configuration, the device with the lower seed value shall	32.5.4.3	M	Yes [ ]	Become the SLAVE.

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32.13.5.7 100BASE-T2 specific Auto-Negotiation requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
AN9	Both PHYs set in manual mode to be either MASTER or SLAVE shall be treated as	32.5.4.3	M	Yes [ ]	MASTER-SLAVE resolution fault (Failure) condition
AN10	MASTER-SLAVE resolution fault (failure) condition shall result in	32.5.4.3	M	Yes [ ]	MASTER-SLAVE Configuration Resolution Fault bit (10.15) to be set
AN11	MASTER-SLAVE Configuration resolution fault condition shall be treated as	32.5.4.3	M	Yes [ ]	MASTER-SLAVE Configuration Resolution complete

32.13.5.8 PMA electrical specifications

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	The value of all components in test circuits shall be accurate to within	32.6	M	Yes [ ]	±1%.
PME2	The PHY shall provide electrical isolation between	32.6.1.1	M	Yes [ ]	The DTE or repeater circuits including frame ground, and all MDI leads.
PME3	PHY-provided electrical separation shall withstand at least one of three electrical strength tests	32.6.1.1	M	Yes [ ]	a) 1500 V rms at 50–60Hz for 60 s, applied as specified in section 5.3.2 of IEC 60950. b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950. c) a sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs. (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60950.
PME4	There shall be no insulation breakdown as defined in Section 5.3.2 of IEC 60950, during the test.	32.6.1.1	M	Yes [ ]	
PME5	The resistance after the test shall be at least	32.6.1.1	M	Yes [ ]	2 MΩ, measured at 500 Vdc.
PME6	The PMA shall provide the Transmit function specified in 32.4.1.1.2 in accordance with the electrical specifications of this clause.	32.6.1.2	M	Yes [ ]	

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME7	Where a load is not specified, the transmitter shall meet all the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.	32.6.1.2	M	Yes [ ]	
PME8	The tolerance on the poles of the test filters used in 32.6 shall be	32.6.1.2	M	Yes [ ]	±1%
PME9	A special transmit test mode shall be required to allow for testing of the transmitter waveform	32.6.1.2.1	M	Yes [ ]	
PME10	A test mode for measuring transmitter output jitter is required.	32.6.1.2.1	M	Yes [ ]	
PME11	For a PHY with a MII interface, the transmit test mode shall be enabled by	32.6.1.2.1	M	Yes [ ]	Setting bit 9.15 and 9.14 (MASTER-SLAVE Control register) of the MII management register set as shown in Table 32–6.
PME12	These test modes shall only change the data symbols provided to the transmitter circuitry and may not alter the electrical characteristics of the transmitter	32.6.1.2.1	M	Yes [ ]	
PME13	When transmit test mode 1 is enabled, the PHY shall transmit	32.6.1.2.1	M	Yes [ ]	The sequence of data symbols specified in 32.6.1.2.1 continuously from both transmitters.
PME14	When in test mode 1, the transmitter shall time the transmitted symbols	32.6.1.2.1	M	Yes [ ]	From a 25.000 MHz ± 0.01% clock.
PME15	When test mode 2 is enabled, the PHY shall transmit	32.6.1.2.1	M	Yes [ ]	The data symbol sequence {+2,–2} repeatedly on both channels.
PME16	When in test mode 2, the transmitter shall time the transmitted symbols	32.6.1.2.1	M	Yes [ ]	From a 25.000 MHz ± 0.01% clock.
PME17	A PHY without a MII shall provide a means to enter this test mode.	32.6.1.2.1	M	Yes [ ]	
PME18	The vendor shall	32.6.1.2.1	M	Yes [ ]	Provide a means to enable these modes for testing.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME19	When in transmit test mode 1 and observing the differential signal output at the MDI, terminated in 100 Ω, preprocessed by the high pass filter defined below, for either pair, with no intervening cable, the absolute value of the peak of the waveform at points A and B as defined in Figure 32–18 shall fall within	32.6.1.2.2	M	Yes [ ]	The range of 1.71V to 1.91 V (1.81 V ± 0.5 dB).
PME20	The absolute value of the peak of the waveforms at points A and B shall	32.6.1.2.2	M	Yes [ ]	Differ by less than 2%.
PME21	The absolute value of the peak of the waveform at points C and D as defined in Figure 32–18 shall differ	32.6.1.2.2	M	Yes [ ]	From 0.5 times the average of the absolute values of the peaks of the waveform at points A and B by less than 2%.
PME22	The preprocessing filter shall have	32.6.1.2.2	M	Yes [ ]	The transfer function specified in 32.6.1.2.2.
PME23	When in transmit test mode 1 and observing the differential transmitted output at the MDI, for either pair, with no intervening cabling, the peak value of the waveform at point F as defined in Figure 32–17 shall be	32.6.1.2.3	M	Yes [ ]	Greater than 70.5% of the peak value of the waveform at point E. A preprocessing filter is not used for this measurement.
PME24	The transmitter differential output voltage shall be measured at the output of the high pass filter defined in 32.6.1.2.2 with no intervening cables.	32.6.1.2.4	M	Yes [ ]	
PME25	The voltage waveforms at points A, B, C and D as defined in Figure 32–17,when normalized by their respective peak values, shall	32.6.1.2.4	M	Yes [ ]	Lie within the time domain template defined in Figure 32–18 and the piecewise linear interpolation between the points in Table 32–6
PME26	The magnitude in dB of the Fourier transform of the waveforms at points A, B, C and D shall	32.6.1.2.4	M	Yes [ ]	Lie within the transmit frequency domain template defined in Figure 32–18 and the piecewise linear interpolation between the points in Table 32–7.
PME27	The time span of the waveforms so processed shall be	32.6.1.2.4	M	Yes [ ]	–80 ns to +2000 ns with the 0 ns point of the waveform aligned as for the time domain mask shown in Figure 32–18 and the magnitude of the Fourier transform should be normalized so that the maximum value is at 0 dB.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME28	When in transmit mode 2, the peak-to-peak jitter of the zero crossings of the differential signal output at the MDI shall	32.6.1.2.5	M	Yes [ ]	Be less than 0.5 ns.
PME29	The quinary symbol transmission rate on each pair shall be	32.6.1.2.6	M	Yes [ ]	25.000 MHz ± 0.01%.
PME30	The PMA shall provide	32.6.1.3	M	Yes [ ]	The Receive function specified in 32.4.1.3 in accordance with the electrical specifications of this clause.
PME31	The patch cabling and interconnecting hardware used in test configurations shall	32.6.1.3	M	Yes [ ]	Meet or exceed ISO/IEC 11801 Category 3 specifications.
PME32	The combined responses of the test fixture TX block and NEXT or cabling channel blocks shall be	32.6.1.3.1	M	Yes [ ]	Those defined in Table 32–8.
PME33	The output impedance of the test channel shall be	32.6.1.3	M	Yes [ ]	Consistent with 32.6.1.4.1.
PME34	The idle symbol generator outputs shall be	32.6.1.3	M	Yes [ ]	Conformant with the idle signaling specified in 32.3 with loc_rcvr_status=OK.
PME35	The clock source shall	32.6.1.3	M	Yes [ ]	Result in a quinary symbol transmission rate conformant with 32.6.1.2.6.
PME36	The jitter on the clock source shall be	32.6.1.3	M	Yes [ ]	Less than 0.2 ns.
PME37	The test channel implementation shall ensure that the ratio of the squared error between the implemented NEXT channel symbol responses and the specified NEXT channel symbol responses to the energy in the specified NEXT channel symbol responses shall be	32.6.1.3	M	Yes [ ]	Less than 5%.
PME38	The test channel implementation shall ensure that the energy of the implemented NEXT channel impulse responses and the energy of the specified NEXT channel impulse responses shall	32.6.1.3	M	Yes [ ]	Differ by less than ±0.25 dB.
PME39	A special receiver test mode shall be required to allow for receiver alien NEXT tolerance and jitter testing.	32.6.1.3.2	M	Yes [ ]	
PME40	For a PHY with a MII interface, this mode shall be enabled by	32.6.1.3.2	M	Yes [ ]	Setting bit 9.13 (MASTER-SLAVE Control Register) of the MII management register set to a 1.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME41	A PHY without an MII shall provide	32.6.1.3.2	M	Yes [ ]	A means to enable this test mode.
PME42	This mode shall not be overridden except by	32.6.1.3.2	M	Yes [ ]	Clearing bit 9.13 or resetting the PHY.
PME43	When the receive test mode is enabled, the receiver shall	32.6.1.3.2	M	Yes [ ]	Configure itself in SLAVE mode, continually attempt to bring its receiver up until successful receiver operation is achieved and transmit symbols in idle mode.
PME44	For a PHY with a MII interface, when the receiver is properly detecting the received data, it shall set	32.6.1.3.2	M	Yes [ ]	Bit 10.13 of the MII management register set to 1 and reset the error count in bit 10.0–10.7 (MSB) to zero.
PME45	The error count shall be incremented	32.6.1.3.2	M	Yes [ ]	For every symbol error detected in the received idle sequence.
PME46	Upon loss of proper data reception, the receiver shall	32.6.1.3.2	M	Yes [ ]	Clear bit 10.13.
PME47	A PHY without an MII shall provide	32.6.1.3.2	M	Yes [ ]	A means to provide the functions defined in PME43 through PME46.
PME48	The vendor shall provide a means to enable this mode for conformance testing.	32.6.1.3.2	M	Yes [ ]	
PME49	Differential signals received on the receive inputs that were transmitted within the constraints of 32.6.1.2, and have then passed through a link as defined in 32.7, shall be translated into	32.6.1.3.3	M	Yes [ ]	One of the PMA_UNITDATA.indication messages with an bit error ratio less than 10^{-10} and sent to the PCS after link bring-up.
PME50	Performance shall be tested	32.6.1.3.3	M	Yes [ ]	In at least two configurations: using a 100 m link segment conformant to 32.7 and with a link segment less than one meter in length between transmitter and receiver.
PME51	Differential signals received from the test channel defined in 32.6.1.3.1 shall be detected	32.6.1.3.4	M	Yes [ ]	With a symbol error ratio less than 10^{-10} when the PHY is in receiver test mode for the combinations of channel and worst-case alien NEXT responses specified in 32.6.1.2.
PME52	In the test configuration described in 32.6.1.3.1 and for all combinations of worst-case channel and alien NEXT coefficients tabulated in 32.6.1.3.4, the peak-to-peak value of the RX_CLK zero-crossing jitter shall be less than	32.6.1.3.5	M	Yes [ ]	1.3 ns after the receiver is properly receiving the data and has set bit 9.13 of the MII management register set to 1.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME53	When the jitter waveform is filtered by a high pass filter having the transfer function specified in 32.6.1.3.4, the peak-to-peak value of the jitter waveform shall be less than	32.6.1.3.5	M	Yes [ ]	0.8 ns.
PME54	The RX_CLK of the MII shall be made available for the receiver jitter test specified in 32.6.1.3.5.	32.6.1.3.5	M	Yes [ ]	
PME55	A PHY without an MII shall provide an equivalent to the MII RX-CLK clock for the receiver jitter test specified in 32.6.1.3.5.	32.6.1.3.5	M	Yes [ ]	
PME56	While receiving packets from a compliant 100BASE-T2 transmitter connected to all MDI pins, a receiver shall send the	32.6.1.3.6	M	Yes [ ]	Proper PMA_UNITDATA.indication messages to the PCS for any differential input signal E_s that results in a signal E_{dif} that meets 32.6.1.3.3 even in the presence of common-mode voltages E_{cm} (applied as shown in Figure 32–21).
PME57	E_{cm} shall be	32.6.1.3.6	M	Yes [ ]	A 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%–80%), connected to each of the pairs BI_DA+, BI_DA-, BI_DB+ and BI_DB-.
PME58	The receive feature shall properly receive	32.6.1.3.7	M	Yes [ ]	Incoming data with a 5-level symbol rate within the range 25.000 MHz ± 0.01%.
PME59	The differential impedance as measured at the MDI for each transmit/receive channel shall be such that	32.6.1.4.1	M	Yes [ ]	Any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 Ω is at least 17 dB below the incident signal, over the frequency range of 2.0 MHz to 25.0 MHz and at least $12.9–20\log_{10}(f/10)$ dB over the frequency range 6.5 MHz to 25 MHz (f in MHz).
PME60	This return loss shall be maintained	32.6.1.4.1	M	Yes [ ]	At all times when the PHY is transmitting data.
PME61	The common-mode to differential-mode impedance balance of each transmit output shall exceed	32.6.1.4.2	M	Yes [ ]	The value specified by the equations specified in 32.6.1.2.6 over the range 2.0–25.0 MHz.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME62	Transmitters and receivers shall tolerate	32.6.1.4.4	M	Yes [ ]	The application of short circuits between the leads of any receive input for an indefinite period of time without damage.
PME63	Transmitters and receivers shall resume	32.6.1.4.4	M	Yes [ ]	Normal operation after such faults are removed.
PME64	The magnitude of the current through the short circuit specified in PME62 shall not exceed	32.6.1.4.4	M	Yes [ ]	300 mA.
PME65	Transmitters shall withstand without damage	32.6.1.4.4	M	Yes [ ]	A 1000 V common-mode impulse of either polarity (E_{cm} as indicated in Figure 32–24).
PME66	The shape of the impulse shall be	32.6.1.4.4	M	Yes [ ]	0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.
PME67	After 100 ms following PowerOn, the current drawn by the PHY shall not exceed	32.6.2	M	Yes [ ]	1.0 A when powered through the MII.
PME68	The PHY shall	32.6.2	M	Yes [ ]	Be capable of operating from all voltage sources allowed by Clause 22, including those current limited to1.0 A, as supplied by the DTE or repeater through the resistance of all permissible MII cabling.
PME69	The PHY shall not introduce	32.6.2	M	Yes [ ]	Extraneous signals on the MII control circuits during normal power-up and power-down.

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32.13.5.9 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	100BASE-T2 links shall use	32.7.1	M	Yes [ ]	2 pair of balanced cabling, CAT 3 or better, with a nominal impedance of 100 Ω.
LKS2	Unless otherwise specified, link segment testing shall be conducted using	32.7.2	M	Yes [ ]	Source and load impedances of 100 Ω.
LKS3	The tolerance on the poles of the test filter used in this section shall be	32.7.2	M	Yes [ ]	± 1%.
LKS4	The insertion loss of a link segment shall be no more than	32.7.2.1	M	Yes [ ]	14.6 dB at all frequencies between 2 and 16 MHz.
LKS5	The insertion loss specification shall be met when	32.7.2.1	M	Yes [ ]	The link segment is terminated in source and load impedances that satisfy 32.6.1.4.1.
LKS6	The magnitude of the differential characteristic impedance of a 3 m segment of balanced cabling pair used in a link shall be	32.7.2.2	M	Yes [ ]	Between 85 and 115 Ω for all frequencies between 2 and 16 MHz.
LKS7	The NEXT loss between each of the two duplex channels of a link segment shall be	32.7.2.3.1	M	Yes [ ]	At least $19.3–16.6\log_{10}(f/16)$ (where f is the frequency in MHz) over the frequency range 2.0 to 16 MHz.
LKS8	The NEXT loss between link segments of two different connections shall be	32.7.2.3.1	M	Yes [ ]	At least $22.0 –16.6\log_{10}(f/16)$ (where f is the frequency in MHz) over the frequency range 2.0 to 16 MHz.
LKS9	The MDNEXT loss between a link segment and the two alien data carrying channels shall be	32.7.2.3.2	M	Yes [ ]	At least $19.0–16.6\log_{10}(f/16)$ dB (where f is the frequency in MHz) over the frequency range 2.0 to 16 MHz.
LKS10	To limit the FEXT noise from an adjacent channel, the ELFEXT loss between channels shall be	32.7.2.3.3	M	Yes [ ]	Greater than $20.9–20\log_{10}(f/16)$ dB as defined in 32.7.2.3.3
LKS11	The MDELFEXT loss between a duplex channel and the other data carrying duplex channels shall be	32.7.2.3.4	M	Yes [ ]	Greater than $19.9–20\log10(f/16)$ (where f is the frequency in MHz) over the frequency range 2.0 to 16 MHz.
LKS12	The maximum spacing of the frequency in the sample shall be	32.7.2.3.5	M	Yes [ ]	250 kHz.

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32.13.5.9 Characteristics of the link segment *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
LKS13	When 10BASE-T service is used in adjacent pairs, the channel shall provide	32.7.2.3.5	M	Yes [ ]	A NEXT loss to Insertion loss Ratio (NIR) greater than 19.4 dB.
LKS14	The propagation delay of a link segment shall not exceed	32.7.2.4.1	M	Yes [ ]	5.7 ns/meter at all frequencies between 2.0–25.0 MHz.
LKS15	The difference in propagation delay, or skew, under all conditions, between the fastest and the slowest channel in a link segment shall not exceed	32.7.2.4.2	M	Yes [ ]	50 ns at all frequencies between 2.0–25.0 MHz.
LKS16	Once installed, the skew between pairs due to environmental conditions shall not vary	32.7.2.4.2	M	Yes [ ]	More than ± 10 ns.
LKS17	The noise level on the link segments shall be such that	32.7.3	M	Yes [ ]	The objective error ratio is met.
LKS18	The MDNEXT noise on a link segment shall not exceed	32.7.3.1	M	Yes [ ]	182 mVp.
LKS19	The MDFEXT noise on a link segment shall not exceed	32.7.3.2	M	Yes [ ]	54.4 mVp.
LKS20	Cables made from up to 25 pairs of Category 5 cabling, if used, shall be limited in length to no more than	32.7.4.3	O	Yes [ ]	90 m total.
LKS21	The services in 25 pair Category 5 cabling shall be limited to any combination of 100BASE-T2, 10BASE-T and digital phone service compliant with the ISDN-BR U and S/T interfaces up to a total of 12 services in the cable.	32.7.4.3	M	Yes [ ]	
LKS22	Jumper cabling, or horizontal runs, made from more than 4 pairs of Category 3 cabling shall not be used	32.7.4.3	M	Yes [ ]	

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32.13.5.10 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	32.8.1	M	Yes [ ]	8-Way connector as per IEC 60603-7.
MDI2	Connector used on cabling	32.8.1	M	Yes [ ]	Plug.
MDI3	Connector used on PHY	32.8.1	M	Yes [ ]	Jack (as opposed to plug).
MDI4	AN MDI connector for the PHY that implements the crossover function shall be marked	32.8.2	M	Yes [ ]	With the graphical symbol “X”.

32.13.5.11 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ENV1	Conformance to safety specifications	32.10.1	M	Yes [ ]	IEC 60950.
ENV2	Installation practice	32.10.2.1	M	Yes [ ]	Sound practice, as defined by applicable local codes.
ENV3	Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection.	32.10.2.2	M	Yes [ ]	
ENV4	Care taken during installation to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.	32.10.2.3	M	Yes [ ]	
ENV5	Application of voltages specified in 32.10.2.4 does not result in any safety hazard.	32.10.2.4	M	Yes [ ]	
ENV6	Conformance with local and national codes for the limitation of electromagnetic interference.	32.10.3.1	M	Yes [ ]	
ENV7	All equipment subject to this clause shall conform to	32.10.4	M	Yes [ ]	The requirements of 14.7 and the applicable sections of ISO/IEC 11801.

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32.13.5.12 Timing requirements exposed MII

Item	Feature	Subclause	Status	Support	Value/Comment
TME1	TX-EN (sampled to MDI output)	32.12.1	M	Yes [ ]	7–9 bit times
TME2	MDI input to CRS assert	32.12.1	M	Yes [ ]	25 bit times
TME3	MDI input to CRS deassert	32.12.1	M	Yes [ ]	29 bit times
TME4	MDI input to COL assert	32.12.1	M	Yes [ ]	25 bit times
TME5	MDI input to COL deassert	32.12.1	M	Yes [ ]	29 bit times
TME6	TX_EN sampled to CRS assert	32.12.1	M	Yes [ ]	0–4 bit times
TME7	TX_EN sampled to CRS deassert	32.12.1	M	Yes [ ]	0–16 bit times

32.13.5.13 Timing requirements unexposed MII

Item	Feature	Subclause	Status	Support	Value/Comment
TMU1	MAC transmit start to MDI output	32.12.2	M	Yes [ ]	13 bit times
TMU2	MDI input to MDI output (worst-case non-deferred transmit)	32.12.2	M	Yes [ ]	50 bit times
TMU3	MDI input to collision detect	32.12.2	M	Yes [ ]	33 bit times
TMU4	MDI input to MDI output = Jam (worst-case collision response)	32.12.2	M	Yes [ ]	50 bit times

32.13.5.14 Timing requirements: carrier assertion/deassertion constraint

Item	Feature	Subclause	Status	Support	Value/Comment
TMC1	Each DTE shall satisfy the relationship	36.5.3	M	Yes [ ]	(MAX MDI to MAC Carrier Deassert Detect)–(MIN MDI to MAC Carrier Assert Detect).

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33. Power over Ethernet over 2 Pairs

33.1 Overview

This clause defines the functional and electrical characteristics for providing a Power over Ethernet (PoE) system. The system consists of two optional power (non-data) entities, a Powered Device (PD) and Power Sourcing Equipment (PSE), for use with the MAU defined in Clause 14 and the PHYs defined in Clause 25, Clause 40, Clause 55, and Clause 126. These entities allow devices to draw/supply power using the same generic cabling as is used for data transmission.

This clause specifies Type 1 and Type 2 devices. References to PSEs and PDs without a Type qualifier refer to Type 1 and Type 2 devices. See Clause 145 for the specification of Type 3 and Type 4 devices.

Power over Ethernet is intended to provide a 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T device with a single interface to both the data it requires and the power to process this data. This clause specifies the following:

a) A power source to add power to the 100 Ω balanced cabling system
b) The characteristics of a powered device's load on the power source and the structured cabling
c) A protocol allowing the detection of a device that requests power from a PSE
d) Methods to classify devices based on their power needs
e) A method for powered devices and power sourcing equipment to dynamically negotiate and allocate power
f) A method for scaling supplied power back to the detect level when power is no longer requested or required

The importance of item c) above should not be overlooked. Given the large number of legacy devices (both IEEE 802.3 and other types of devices) that could be connected to a 100 Ω balanced cabling system, and the possible consequences of applying power to such devices, the protocol to distinguish compatible devices and non-compatible devices is important to prevent damage to non-compatible devices.

The detection and powering algorithms are likely to be compromised by cabling that is not point-to-point, resulting in unpredictable performance and possibly damaged equipment.

This clause differentiates between the two ends of the powered portion of the link, defining the PSE and the PD as separate but related devices.

33.1.1 Objectives

The following are objectives of Power via MDI:

a) *Power*—A PD designed to the standard, and within its range of available power, can obtain both power and data for operation through the MDI and therefore needs no additional connections.
b) *Safety*—A PSE designed to the standard does not introduce non-SELV (Safety Extra Low Voltage) power, as defined by IEC 60950-1, into the wiring plant.
c) *Compatibility*—Clause 33 utilizes the MDIs of 10BASE-T, 100BASE-TX, and 1000BASE-T without modification. Type 1 operation adds no significant requirements to the cabling. Type 2 operation requires ISO/IEC 11801:1995 Class D or better cabling and a derating of the cabling maximum ambient operating temperature.

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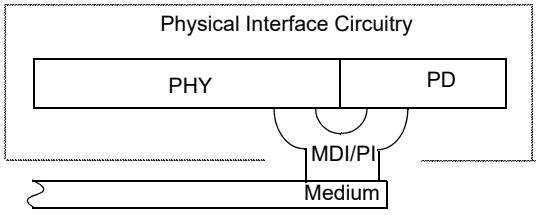
d) *Simplicity*—The powering system described here is no more burdensome on the end users than the requirements of 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T.

33.1.2 Compatibility considerations

All implementations of PD and PSE systems shall be compatible at their respective Power Interfaces (PIs) when used in accordance with the restrictions of Clause 33 where appropriate. Designers are free to implement circuitry within the PD and PSE in an application-dependent manner provided that the respective PI specifications are satisfied.

33.1.3 Relationship of Power over Ethernet to the IEEE 802.3 Architecture

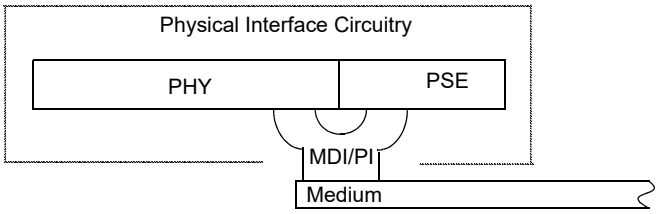
Power over Ethernet comprises an optional non-data entity. As a non-data entity, it does not appear in a depiction of the OSI Reference Model. Figure 33–1 depicts the positioning of Power over Ethernet (PoE) in the case of the PD.



MDI = Medium Dependent Interface
PD = Powered Device
PHY = Physical Layer Device
PI = Power Interface

Figure 33–1—PoE powered device relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

Figure 33–2 and Figure 33–3 depict the positioning of Power over Ethernet in the cases of the Endpoint PSE and the Midspan PSE, respectively.



MDI = Medium Dependent Interface
PHY = Physical Layer Device
PI = Power Interface
PSE = Power Sourcing Equipment

Figure 33–2—PoE Endpoint power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

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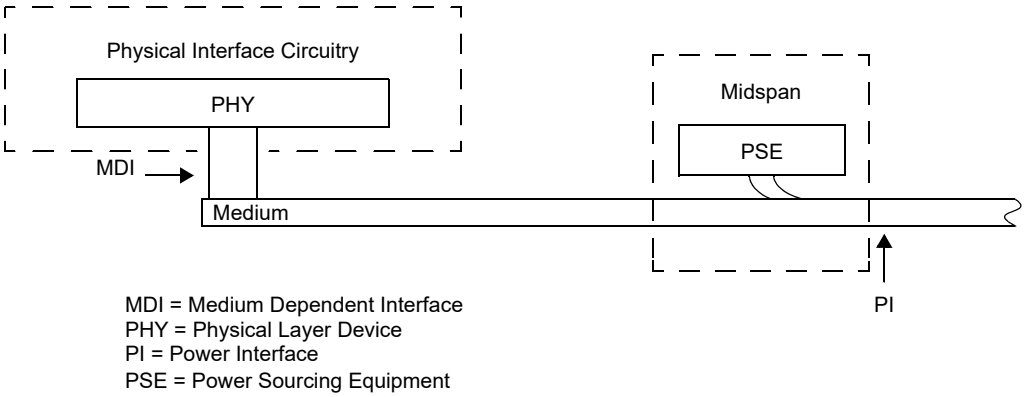

Figure 33–3—PoE Midspan power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

The Power Interface (PI), as defined in 1.4.484, is the mechanical and electrical interface between the Power Sourcing Equipment (PSE) or Powered Device (PD) and the transmission medium.

The PI in both an Endpoint PSE and in a PD is the MDI as defined in 1.4.395.

PSE power interface specifications that are defined at the MDI apply to an Endpoint PSE. They may or may not apply to a Midspan PSE PI.

33.1.4 Type 1 and Type 2 system parameters

A power system, consisting of a single PSE, link section, and a single PD, defined as either Type 1 or Type 2, has certain basic parameters defined according to Table 33–1. These parameters define not only certain performance characteristics of the system, but are also used in calculating the various electrical characteristics of PSEs and PDs as described in 33.2 and 33.3.

Table 33–1—Type 1 and Type 2 system parameters

Parameter	Symbol	Units	Type 1 value	Type 2 value	Additional information
Nominal highest DC current per pair	I_{Cable}	A	0.350	0.600	
Channel maximum DC pair loop resistance	R_{Ch}	Ω	20.0	12.5	
Minimum cable type			twisted-pair cabling per 14.4 and 14.5[a]	Class D	See 33.1.4.1, 33.1.4.2

[a]Class D recommended.

I_{Cable} is the current on one twisted pair in the multi-twisted pair cable. Two twisted pairs are required to source I_{Cable}—one carrying (+ I_{Cable}) and one carrying (– I_{Cable}), from the perspective of the PI.

It should be noted that the cable references use “DC loop resistance,” which refers to a single conductor. This clause uses “DC pair loop resistance,” which refers to a pair of conductors in parallel. Therefore, R_{Ch} is related to, but not equivalent to, the “DC loop resistance” called out in the cable references.

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I_{Port} is the current on either powered pair.

V_{PD} is the voltage at the PD PI, measured between any positive conductor and any negative conductor of the powered pairs.

V_{PSE} is the voltage at the PSE PI, measured between any positive conductor and any negative conductor of the powered pairs.

33.1.4.1 Type 2 cabling requirement

Type 2 operation requires Class D, or better, cabling as specified in ISO/IEC 11801:1995 with the additional requirement that channel DC loop resistance shall be 25 Ω or less. These requirements are also met by Category 5e or better cable and components as specified in ANSI/TIA-568-C.2; or Category 5 cable and components as specified in ANSI/TIA/EIA-568-A.

Under worst-case conditions, Type 2 operation requires a 10 °C reduction in the maximum ambient operating temperature of the cable when all cable pairs are energized at I_{Cable} (see Table 33–1), or a 5 °C reduction in the maximum ambient operating temperature of the cable when half of the cable pairs are energized at I_{Cable}. Additional cable ambient operating temperature guidelines for Type 2 operation are provided in ISO/IEC TR 29125 [B44][72] and TIA TSB-184 [B65].

33.1.4.2 Type 1 and Type 2 channel requirement

Type 1 and Type 2 operation requires that the resistance unbalance shall be 3% or less. Resistance unbalance is a measure of the difference between the two conductors of a twisted pair in the 100 Ω balanced cabling system. Resistance unbalance is defined as in Equation (33–1):

$$\left.\frac{(R_{max} - R_{min})}{(R_{max} + R_{min})} \times 100 \right\}_{\%} \tag{33–1}$$

where

R_{max} is the resistance of the channel conductor with the highest resistance
R_{min} is the resistance of the channel conductor with the lowest resistance

33.2 Power sourcing equipment (PSE)

The PSE is the portion of the end station or midspan equipment that provides the power to a single PD. The PSE's main functions are as follows:

— To search the link section for a PD
— To supply power to the detected PD through the link section
— To monitor the power on the link section
— To remove power when no longer requested or required, returning to the searching state

An unplugged link section is one instance when power is no longer required. In addition, power classification mechanisms exist to provide the PSE with detailed information regarding the power needs of the PD.

A PSE is electrically specified at the point of the physical connection to the cabling.

[72]The numbers in brackets correspond to those of the bibliography in Annex A.

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33.2.1 PSE location

PSEs may be placed in two locations with respect to the link segment, either coincident with the DTE/Repeater or midspan. A PSE that is coincident with the DTE/Repeater is an “Endpoint PSE.” A PSE that is located within a link segment that is distinctly separate from and between the MDIs is a “Midspan PSE.” The requirements of this document shall apply equally to Endpoint and Midspan PSEs unless the requirement contains an explicit statement that it applies to only one implementation. The location of Alternative A and Alternative B Endpoint PSEs and Midspan PSEs are illustrated in Figure 33–4, Figure 33–5, Figure 33–6, and Figure 33–7.

The PSE specification is designed to be compatible with any of the following: 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, 10GBASE-T. PSEs may support either Alternative A, Alternative B, or both.

33.2.2 Midspan PSE types

There are several variants of Midspan PSEs defined:

10BASE-T/100BASE-TX Midspan PSE:
: A Midspan PSE that results in a link that can support only 10BASE-T and 100BASE-TX operation (see Figure 33–6). Note that this limitation is due to the presence of the Midspan PSE whether it is supplying power or not.

1000BASE-T Midspan PSE:
: A Midspan PSE that results in a link that can support 10BASE-T, 100BASE-TX, and 1000BASE-T operation (see Figure 33–7).

2.5GBASE-T Midspan PSE:
: A Midspan PSE that results in a link that can support 1000BASE-T and 2.5GBASE-T operation and optionally support 10BASE-T and 100BASE-TX operation (see Figure 33–7).

5GBASE-T Midspan PSE:
: A Midspan PSE that results in a link that can support 1000BASE-T, 2.5GBASE-T, and 5GBASE-T operation and optionally support 10BASE-T and 100BASE-TX operation (see Figure 33–7).

10GBASE-T Midspan PSE:
: A Midspan PSE that results in a link that can support 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T operation and optionally support 10BASE-T and 100BASE-TX operation (see Figure 33–7).

NOTE—See 33.4.9.4 for Alternative A Midspan PSEs.

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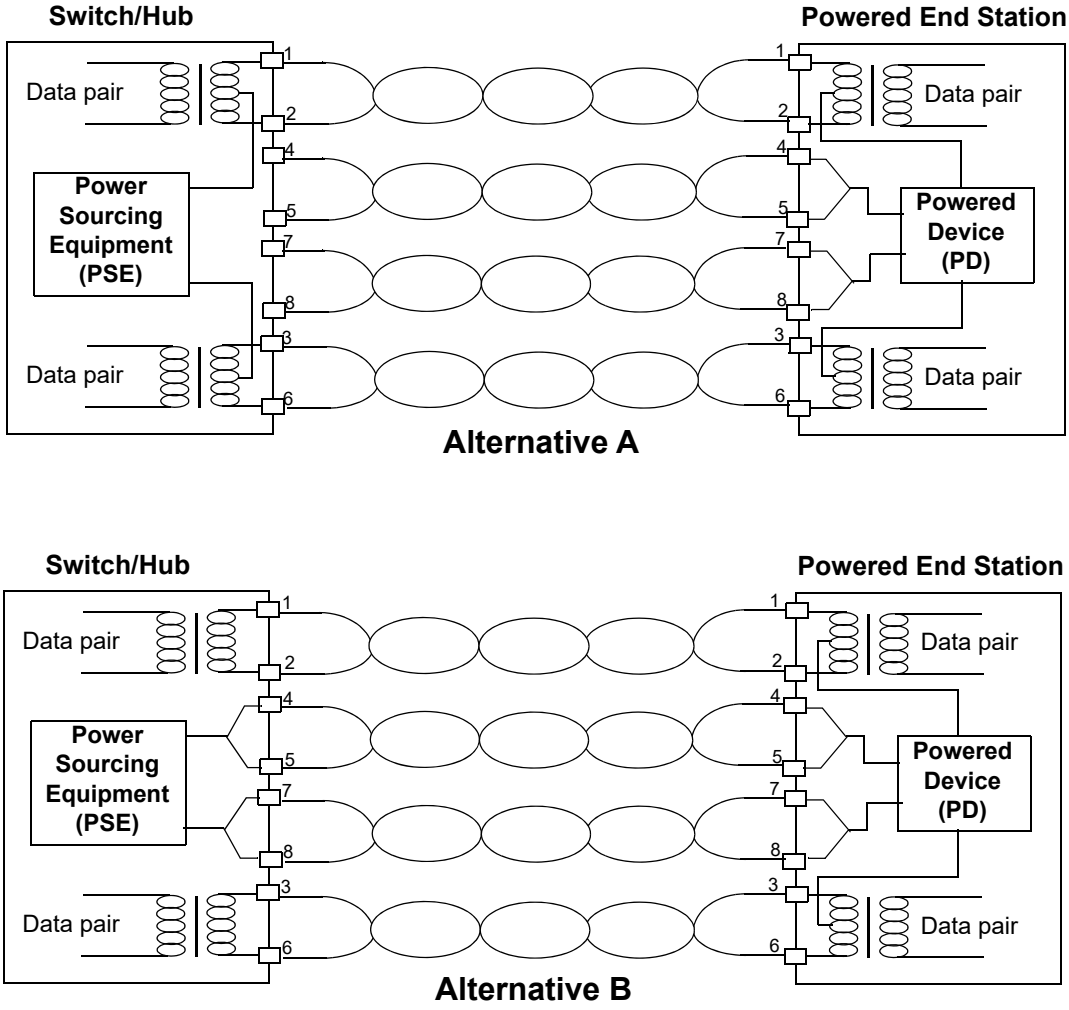

Figure 33–4—10BASE-T/100BASE-TX Endpoint PSE location overview

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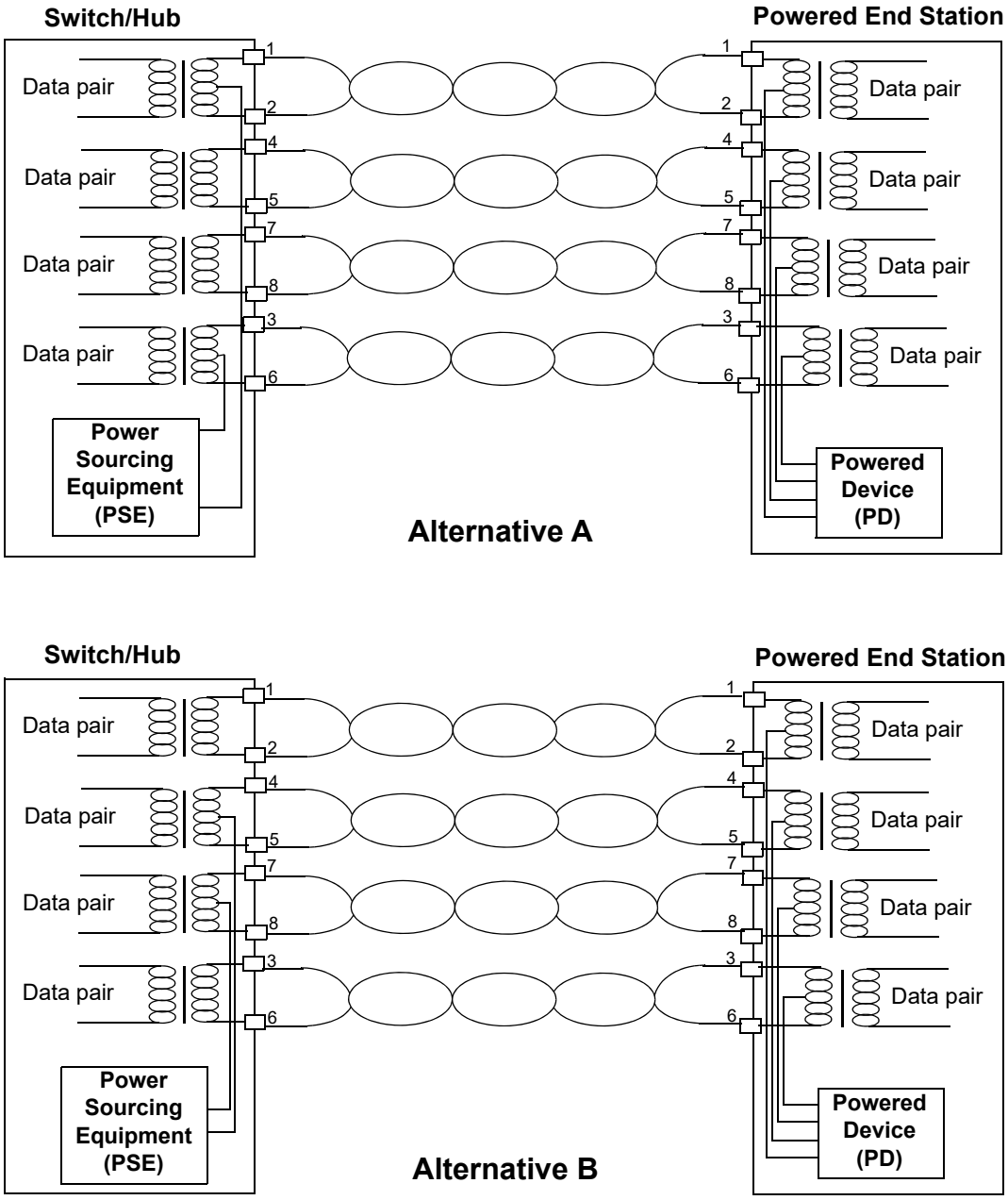

Figure 33–5—1000/2.5G/5G/10GBASE-T Endpoint PSE location overview

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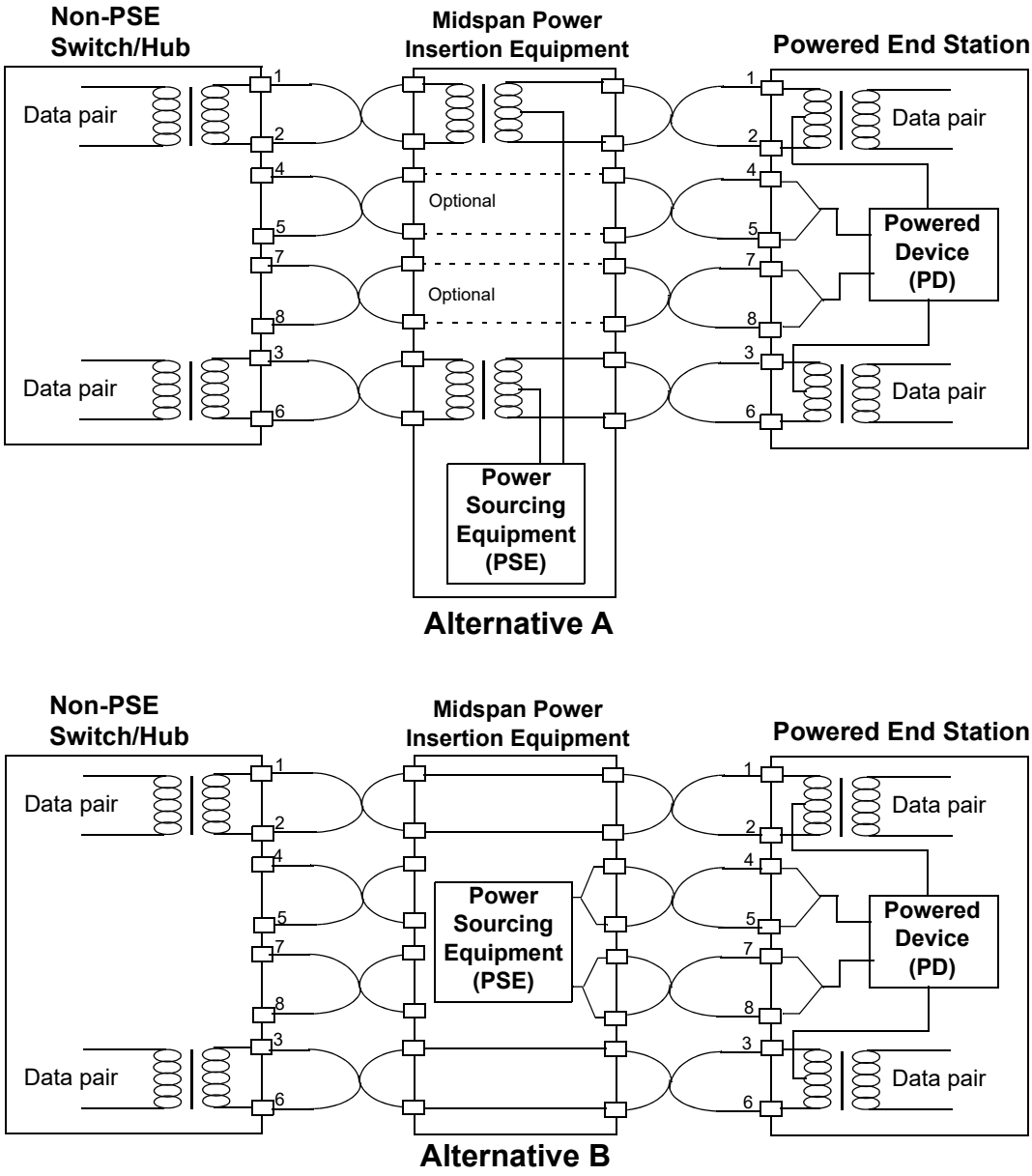

Figure 33–6—10BASE-T/100BASE-TX Midspan PSE location overview

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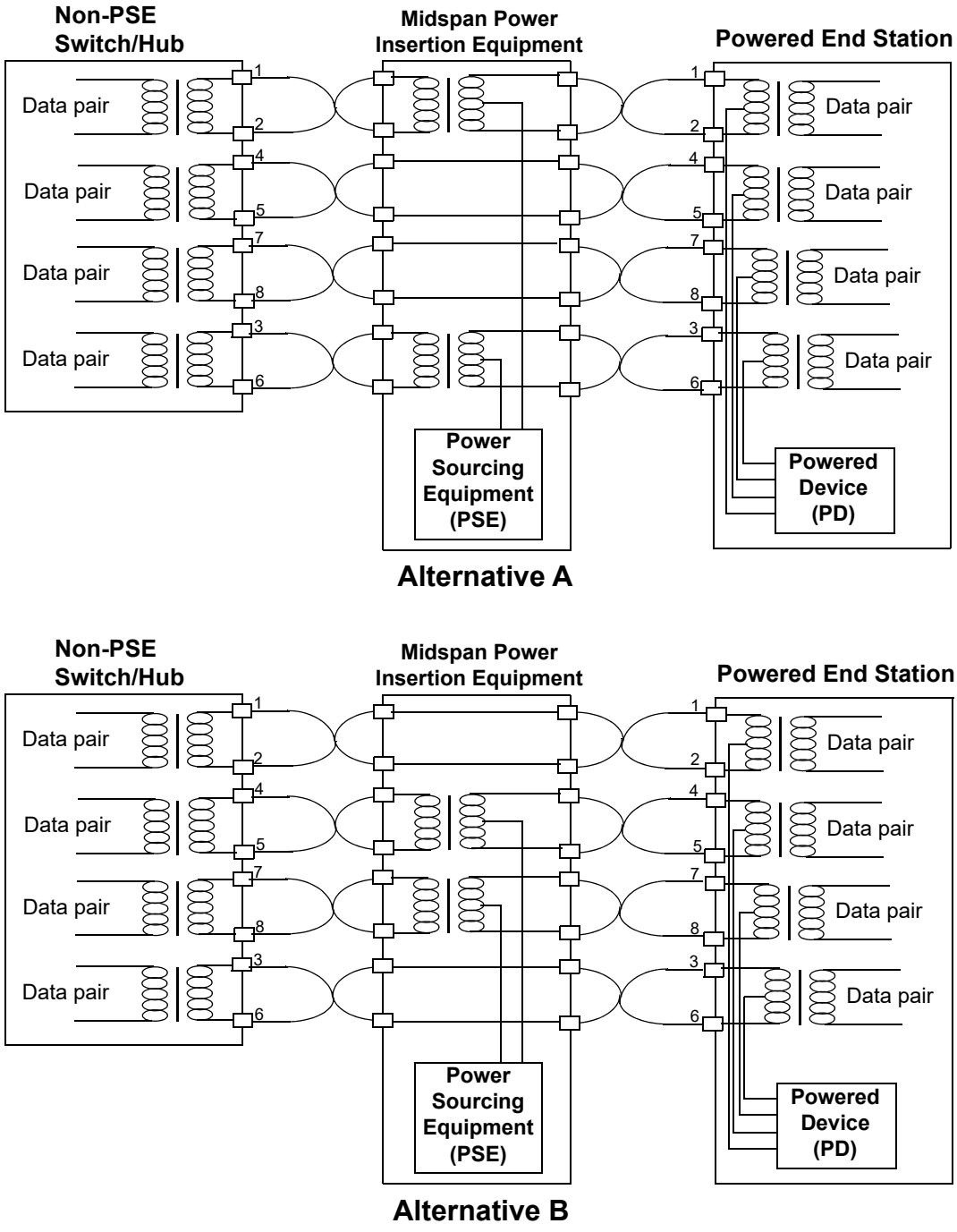

Figure 33–7—1000/2.5G/5G/10GBASE-T Midspan PSE location overview

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33.2.3 PI pin assignments

A PSE device may provide power via one of two valid four-wire connections. In each four-wire connection, the two conductors associated with a pair each carry the same nominal current in both magnitude and polarity. Figure 33–8, in conjunction with Table 33–2, illustrates the valid alternatives.

Table 33–2—PSE Pinout alternatives

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B (All)
1	Negative V_{PSE}	Positive V_{PSE}	
2	Negative V_{PSE}	Positive V_{PSE}	
3	Positive V_{PSE}	Negative V_{PSE}	
4			Positive V_{PSE}
5			Positive V_{PSE}
6	Positive V_{PSE}	Negative V_{PSE}	
7			Negative V_{PSE}
8			Negative V_{PSE}

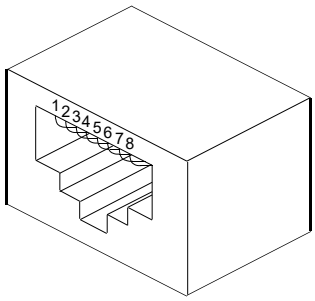

Figure 33–8—PD and PSE eight-pin modular jack

For the purposes of data transfer, the type of PSE data port is relevant to the far-end PD, and in some cases, to the cabling system between them. Therefore, Alternative A matches the positive voltage to the transmit pair of the PSE. PSEs that use automatically-configuring MDI/MDI-X ("Auto MDI-X") ports may choose either polarity choice associated with Alternative A configurations. For further information on the placement of MDI vs. MDI-X, see 14.5.2.

A PSE shall implement Alternative A, Alternative B, or both. While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link section simultaneously.

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33.2.4 PSE state diagrams

The PSE shall provide the behavior of the state diagrams shown in Figure 33–9, Figure 33–9 continued, and Figure 33–10.

33.2.4.1 Overview

Detection, classification, and power turn-on timing shall meet the specifications in Table 33–4, Table 33–10, and Table 33–11.

If power is to be applied, the PSE turns on power after a valid detection in less than T_{pon} as specified in Table 33–11. If the PSE cannot supply power within T_{pon}, it initiates and successfully completes a new detection cycle before applying power.

It is possible that two separate PSEs, one that implements Alternative A and one that implements Alternative B (see 33.2.1), may be attached to the same link segment. In such a configuration, and without the required backoff algorithm, the PSEs could prevent each other from ever detecting a PD by interfering with the detection process of the other.

A PSE performing detection using Alternative B may fail to detect a valid PD detection signature. When this occurs, the PSE backs off for at least T_{dbo} as specified in Table 33–11 before attempting another detection. During this backoff, the PSE shall not apply a voltage greater than V_{Off} to the PI.

If a PSE performing detection using Alternative B detects an open circuit (see 33.2.5.5) on the link section, then that PSE may optionally omit the detection backoff.

If a PSE performing detection using Alternative A detects an invalid signature, it should complete a second detection in less than T_{dbo} min after the beginning of the first detection attempt. This allows an Alternative A PSE to complete a successful detection cycle prior to an Alternative B PSE present on the same link section that may have caused the invalid signature.

NOTE—A Type 1 PSE performing detection using Alternative A may need to have its DTE powering ability disabled when it is attached to the same link segment as a Type 2 Midspan PSE performing detection using Alternative B. This allows the Midspan PSE to successfully complete a detection cycle.

33.2.4.2 Conventions

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

33.2.4.3 Constants

The PSE state diagrams use the following constants:

PSE_TYPE
: A constant indicating the type of the PSE
Values: 1: Type 1 PSE
2: Type 2 PSE

33.2.4.4 Variables

The PSE state diagrams use the following variables:

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class_num_events

A variable indicating the number of classification events performed by the PSE. A variable that is set in an implementation-dependent manner.

Values:0: PSE does not perform Physical Layer classification.
1: PSE performs 1-Event Physical Layer classification.
2: PSE performs 2-Event Physical Layer classification.

error_condition

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 33–11 and that require the PSE not to source power. These error conditions are different from those monitored by the state diagrams in Figure 33–10.

Values:FALSE:No fault indication.
TRUE:A fault indication exists.

I_{Inrush}

Output current during POWER_UP (see Table 33–11 and Figure 33–13).

I_{Port}

Output current (see 33.2.7.6).

legacy_powerup

This variable is provided for PSEs that monitor the PI voltage output and use that information to indicate the completion of PD inrush current during POWER_UP operation. Using only the PI voltage information may be insufficient to determine the true end of PD inrush current; use of a fixed T_{Inrush} period is recommended. A variable that is set in an implementation-dependent manner.

Values:TRUE:The PSE supports legacy power up; this value is not recommended.
FALSE:The PSE does not support legacy power up. It is highly recommended that new equipment use this value.

mr_mps_valid

The PSE monitors either the DC or AC Maintain Power Signature (MPS, see 33.2.9.1). This variable indicates the presence or absence of a valid MPS.

Values:FALSE:If monitoring both components of the MPS, the DC component of MPS is absent or the AC component of MPS is absent. If monitoring only one component of MPS, that component of MPS is absent.
TRUE: If monitoring both components of the MPS, the DC component of MPS and the AC component of MPS are both present. If monitoring only one component of MPS, that component of MPS is present.

mr_pse_alternative

This variable indicates which Pinout Alternative the PSE uses to apply power to the link (see Table 33–2). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bits (11.3:2) or other equivalent function.

Values:A: The PSE uses PSE pinout Alternative A.
B: The PSE uses PSE pinout Alternative B.

mr_pse_enable

A control variable that selects PSE operation and test functions. This variables is provided by a management interface that may be mapped to the PSE Control register PSE Enable bits (11.1:0), as described below, or other equivalent functions.

Values:disable: All PSE functions disabled (behavior is as if there was no PSE functionality). This value corresponds to MDIO register bits 11.1:0 = '00'.
enable: Normal PSE operation. This value corresponds to MDIO register bits 11.1:0 = '01'.
force_power: Test mode selected that causes the PSE to apply power to the PI when there are no detected error conditions. This value corresponds to MDIO register bits 11.1:0 = '10'.

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option_detect_ted

This variable indicates if detection can be performed by the PSE during the ted_timer interval.

Values:FALSE:Do not perform detection during ted_timer interval.

TRUE:Perform detection during ted_timer interval.

option_vport_lim

This optional variable indicates if V_{PSE} is out of the operating range during normal operating state.

Values:FALSE:V_{PSE} is within the V_{Port_PSE} operating range as defined in Table 33–11.

TRUE:V_{PSE} is outside of the V_{Port_PSE} operating range as defined in Table 33–11.

ovld_detected

A variable indicating if the PSE output current has been in an overload condition (see 33.2.7.6) for at least T_{CUT} of a one second sliding time.

Values:FALSE:The PSE has not detected an overload condition.

TRUE:The PSE has detected an overload condition.

pd_dll_power_type

A control variable initially output by the PSE power control state diagram (Figure 33–27), which can be updated by LLDP (see Table 33–26), that indicates the type of PD as advertised through Data Link Layer classification.

Values:1: PD is a Type 1 PD (default)

2: PD is a Type 2 PD

pi_powered

A variable that controls the circuitry that the PSE uses to power the PD.

Values:FALSE:The PSE is not to apply power to the link (default).

TRUE:The PSE has detected a PD, classified it if applicable, and determined the PD is to be powered; or power is being forced on in TEST_MODE.

power_applied

A variable indicating that the PSE has begun steady state operation by having asserted pi_powered, completed the ramp of voltage, is not in a current limiting mode, and is operating beyond the POWER_UP requirements of 33.2.7.5.

Values:FALSE:The PSE is either not applying power or has begun applying power but is still in POWER_UP.

TRUE:The PSE has begun steady state operation.

power_not_available

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power to support the attached PD. Sufficient power is defined by classification; see 33.2.6.

Values:FALSE:PSE is capable to continue to source power to a PD.

TRUE:PSE is no longer capable of sourcing power to a PD.

pse_available_power

This variable indicates the highest power PD Class that could be supported. The value is determined in an implementation-specific manner.

Values:0: Class 1

1: Class 2

2: Class 0 and Class 3

3: Class 4

pse_dll_capable

This variable indicates whether the PSE is capable of performing optional Data Link Layer classification. See 33.6. This variable is provided by a management interface that may be mapped to the PSE Control register Data Link Layer Classification Capability bit (11.5), as described below, or other equivalent functions. A variable that is set in an implementation-dependent manner.

Values:FALSE:The PSE’s Data Link Layer classification capability is not enabled.

TRUE:The PSE’s Data Link Layer classification capability is enabled.

pse_dll_enabled

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A variable indicating whether the Data Link Layer classification mechanism is enabled. See 33.6.
Values:FALSE:Data Link Layer classification is not enabled.
TRUE:Data Link Layer classification is enabled.

pse_ready
Variable that is asserted in an implementation-dependent manner to probe the link segment.
Values:FALSE:PSE is not ready to probe the link segment.
TRUE:PSE is ready to probe the link segment.

NOTE—Care should be taken when negating this variable in a PSE performing detection using Alternative A after an invalid signature is detected due to the delay it introduces between detection attempts (see 33.2.4.1).

pse_reset
Controls the resetting of the PSE state diagram. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE functionality.
Values:FALSE:Do not reset the PSE state diagram.
TRUE:Reset the PSE state diagram.

pse_skips_event2
The PSE can choose to bypass a portion of the classification state flow. A variable that is set in an implementation-dependent manner.
Values:FALSE:The PSE does not bypass MARK_EV1.
TRUE:The PSE does bypass MARK_EV1.

short_detected
A variable indicating if the PSE output current has been in a short circuit condition for T_{LIM} within a sliding window (see 33.2.7.7).
Values:FALSE:The PSE has not detected a short circuit condition.
TRUE:The PSE has detected qualified short circuit condition.

temp_var
A temporary variable used to store the value of the state variable mr_pd_class_detected.

PSEs shall meet at least one of the allowable variable definition permutations described in Table 33–3.

Table 33–3—Allowed PSE variable definition permutations

PSE Type	Variables	
	class_num_events	**pse_dll_capable**
Type 2	2	FALSE
		TRUE
	1	TRUE
Type 1	1	FALSE
		TRUE
	0	FALSE
		TRUE

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33.2.4.5 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops counting upon entering a state where “stop x_timer” is asserted.

tcle1_timer
: A timer used to limit the first classification event time in 2-Event classification; see T_{CLE1} in Table 33–10.

tcle2_timer
: A timer used to limit the second classification event time in 2-Event classification; see T_{CLE2} in Table 33–10.

tdbo_timer
: A timer used to regulate backoff upon detection of an invalid signature; see T_{dbo} in Table 33–11.

tdet_timer
: A timer used to limit an attempt to detect a PD; see T_{det} in Table 33–11.

ted_timer
: A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal; see T_{ed} in Table 33–11. The default state of this timer is ted_timer_done.

tinrush_timer
: A timer used to monitor the duration of the inrush event; see T_{Inrush} in Table 33–11.

tme1_timer
: A timer used to limit the first mark event time in 2-Event classification; see T_{ME1} in Table 33–10.

tme2_timer
: A timer used to limit the second mark event time in 2-Event classification; see T_{ME2} in Table 33–10.

tmpdo_timer
: A timer used to monitor the dropout of the MPS; see T_{MPDO} in Table 33–11.

tpdc_timer
: A timer used to limit the classification time; see T_{pdc} in Table 33–10.

tpon_timer
: A timer used to limit the time for power turn-on; see T_{pon} in Table 33–11.

33.2.4.6 Functions

do_classification
: This function returns the following variables:

  pd_requested_power: This variable indicates the power class requested by the PD. A Type 1 PSE that measures a Class 4 signature assigns that PD to Class 0. See 33.2.6.

  Values:
  - 0: Class 1
  - 1: Class 2
  - 2: Class 0 or Class 3
  - 3: Class 4

  mr_pd_class_detected: The class of the PD associated with the PD classification signature; see Table 33–7 and 33.2.6.

  Values:
  - 0: Class 0
  - 1: Class 1
  - 2: Class 2
  - 3: Class 3
  - 4: Class 4

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do_detection

This function returns the following variables:

signature:

This variable indicates the presence or absence of a PD.

Values: open_circuit: The PSE has detected an open circuit. This value is optionally returned by a PSE performing detection using Alternative B.
valid: The PSE has detected a PD requesting power.
invalid: Neither open_circuit, nor valid PD detection signature has been found.

mr_valid_signature:

This variable indicates that the PSE has detected a valid signature.

Values: FALSE: No valid signature detected.
TRUE: Valid signature detected.

do_mark

This function produces the classification mark event voltage. This function does not return any variables.

set_parameter_type

This function is used by a Type 2 PSE to evaluate the type of PD connected to the link based on Physical Layer classification or Data Link Layer classification results. The PSE's PI electrical requirements defined in Table 33–11 are set to values corresponding to either a Type 1 or Type 2 PSE. This function returns the following variable:

parameter_type: A variable used by a Type 2 PSE to pick between Type 1 and Type 2 PI electrical requirement parameter values defined in Table 33–11.

Values: 1: Type 1 PSE parameter values (default)
2: Type 2 PSE parameter values

When a Type 2 PSE powers a Type 2 PD, the PSE may choose to assign a value of '1' to parameter_type if mutual identification is not complete (see 33.2.6) and shall assign a value of '2' to parameter_type if mutual identification is complete.

When a Type 2 PSE powers a Type 1 PD, the PSE shall meet the PI electrical requirements of a Type 1 PSE, but may choose to meet the electrical requirements of a Type 2 PSE for I_{Con}, I_{LIM}, T_{LIM}, and P_{Type} (see Table 33–11).

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33.2.4.7 State diagrams

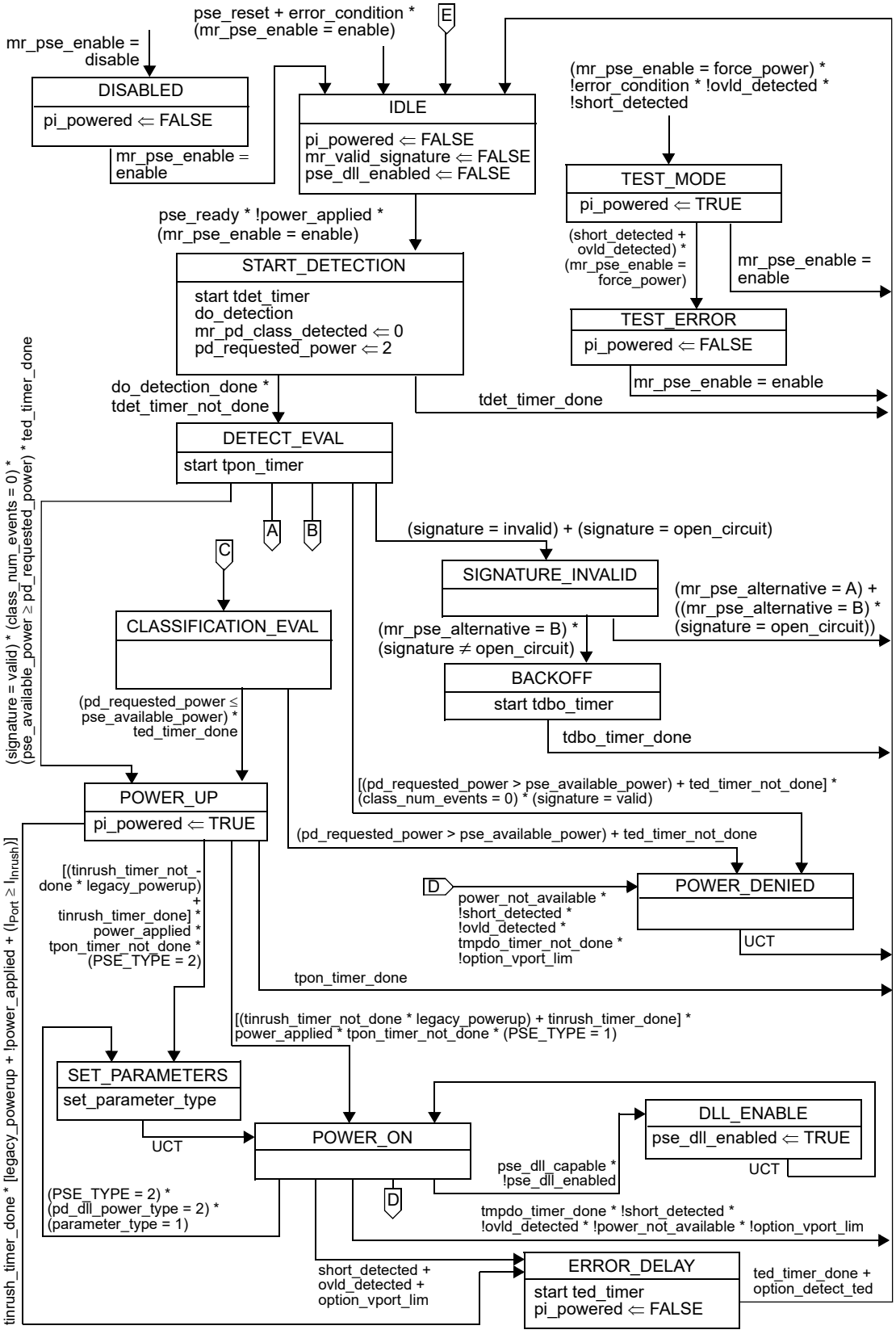

Figure 33–9—PSE state diagram

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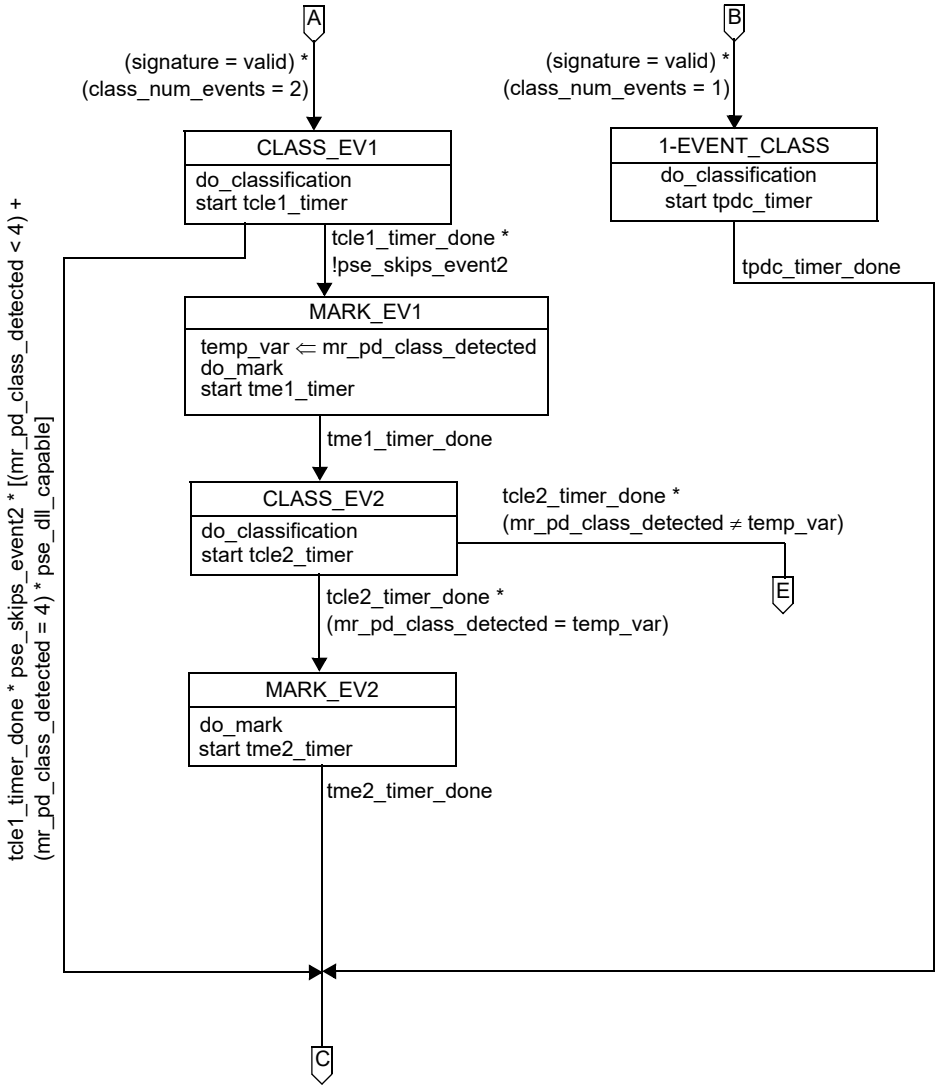

Figure 33–9—PSE state diagram *(continued)*

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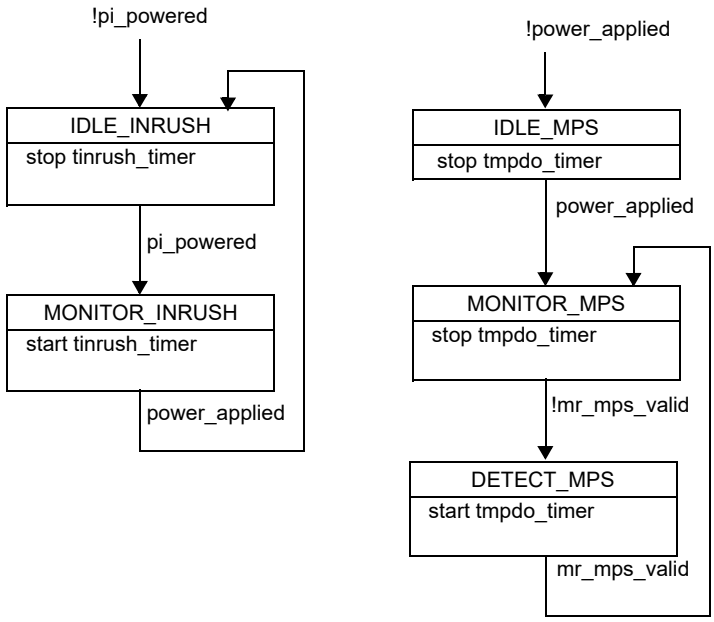

Figure 33–10—PSE monitor inrush and monitor MPS state diagrams

33.2.5 PSE detection of PDs

In any operational state, the PSE shall not apply operating power to the PI until the PSE has successfully detected a PD requesting power.

The PSE probes the link section in order to detect a valid PD detection signature. The PSE PI is connected to a PD through a link section. In the following subclauses, the link is not called out to preserve clarity.

The PSE is not required to continuously probe to detect a PD signature. The period of time when a PSE is not attempting to detect a PD signature is implementation dependent. Also, a PSE may successfully detect a PD but then opt not to power the detected PD.

The PSE shall turn on power only on the same pairs as those used for detection.

33.2.5.1 PSE detection validation circuit

The PSE shall detect the PD by probing via the PSE PI. The PSE shall present a non-valid PD detection signature as defined in Table 33–15 when probed in either polarity by another PSE. An illustrative embodiment of a detection circuit is shown in Figure 33–11.

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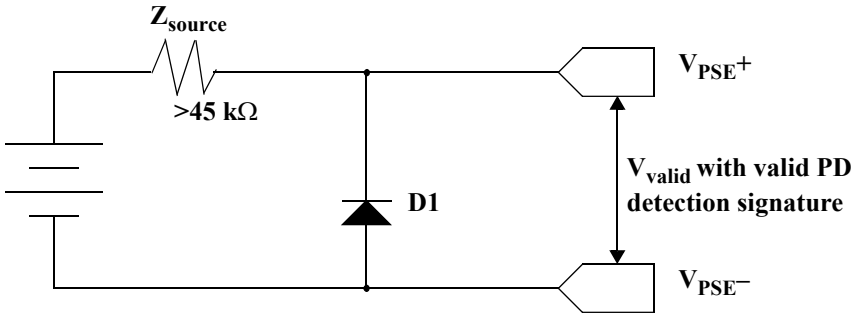

Figure 33–11—PSE detection source

A functional equivalent of the detection circuit that has no source impedance limitation but restricts the PSE detection circuit to the first quadrant is shown in Figure 33–12.

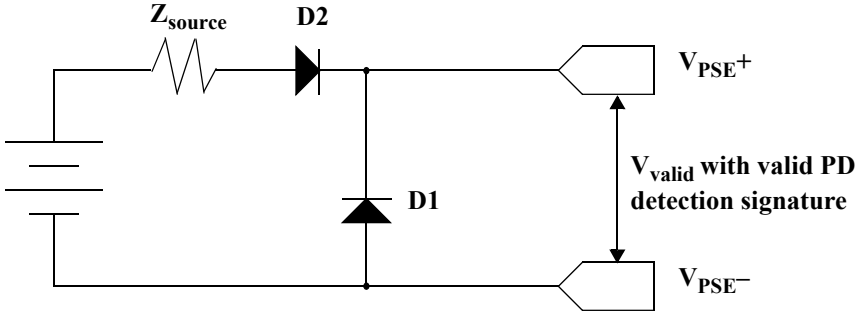

Figure 33–12—Alternative PSE detection source

In Figure 33–11 and Figure 33–12, the diode D1 presents a non-valid PD detection signature for a reversed voltage PSE to PSE connection.

The open circuit voltage and short circuit current shall meet the specifications in Table 33–4. The PSE shall not be damaged by up to 5 mA backdriven current over the range of V_{oc} as specified in Table 33–4. Output capacitance shall be as specified in Table 33–11.

Table 33–4—PSE PI detection state electrical requirements

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Open circuit voltage	V_{oc}	V		30.0	In detection state only
2	Short circuit current	I_{sc}	A		0.005	In detection state only
3	Valid test voltage	V_{valid}	V	2.80	10.0	—
4	Voltage difference between test points	ΔV_{test}	V	1.00		—
5	Slew rate	V_{slew}	V/μs		0.100	—

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33.2.5.2 Detection probe requirements

The detection voltage at the PSE PI shall be within the V_{valid} voltage range (as specified in Table 33–4) with a valid PD detection signature connected (as specified in Table 33–14).

In evaluating the presence of a valid PD, the PSE shall make at least two measurements with V_{PSE} values that create at least a ΔV_{test} difference as specified in Table 33–4. An effective resistance is calculated from two voltage/current measurements made during the detection process.

The resistance is calculated with Equation (33–2):

$$R = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \tag{33–2}$$

where

V_1 and V_2	are the first and second voltage measurements made at the PSE PI, respectively
I_1 and I_2	are the first and second current measurements made at the PSE PI, respectively
R	is the effective resistance

Attached PI capacitance may be determined using these measurements and the port RC time-constant charging characteristics.

NOTE—Settling time before voltage or current measurement: the voltage or current measurement should be taken after V_{PSE} has settled to within 1% of its steady state condition with a valid PD detection signature connected (as specified in Table 33–14).

The PSE shall control the slew rate of the probing detection voltage when switching between detection voltages to be less than V_{slew} as specified in Table 33–4.

33.2.5.3 Detection criteria

A PSE shall accept as a valid signature a link section with both of the following characteristics between the powering pairs with an offset voltage up to V_{os} max and an offset current up to I_{os} max, as specified in Table 33–5:

a) Signature resistance R_{good}, and
b) Parallel signature capacitance C_{good}.

Table 33–5—Valid PD detection signature electrical characteristics

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Accept signature resistance	R_{good}	kΩ	19.0	26.5	—
2	Accept signature capacitance	C_{good}	µF		0.150	—
3	Signature offset voltage tolerance	V_{os}	V	0	2.00	—
4	Signature offset current tolerance	I_{os}	µA	0	12.0	—

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CAUTION

In a multiport system, the implementer should maintain DC isolation through the termination circuitry to eliminate cross-port leakage currents.

33.2.5.4 Rejection criteria

The PSE shall reject link sections as having an invalid signature, when those link sections exhibit any of the following characteristics between the powering pairs, as specified in Table 33–6:

a) Resistance less than or equal to R_{bad} min, or
b) Resistance greater than or equal to R_{bad} max, or
c) Capacitance greater than or equal to C_{bad} min.

A PSE may accept or reject a signature resistance in the band between R_{good} min and R_{bad} min, and in the band between R_{good} max and R_{bad} max. A PSE may accept or reject a parallel signature capacitance in the band between C_{good} max and C_{bad} min.

In instances where the resistance and capacitance meet the detection criteria, but one or both of the offset tolerances are exceeded, the detection behavior of the PSE is undefined.

Table 33–6—Invalid PD detection signature electrical characteristics

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Reject signature resistance	R_{bad}	kΩ	15.0	33.0	—
2	Reject signature capacitance	C_{bad}	μF	10.0		—
3	Open circuit resistance	R_{open}	MΩ	0.500		—

33.2.5.5 Open circuit criteria

If a PSE that is performing detection using Alternative B (see 33.2.3) determines that the impedance at the PI is greater than R_{open} as defined in Table 33–4, it may optionally consider the link to be open circuit and omit the tdbo_timer interval.

33.2.6 PSE classification of PDs and mutual identification

The ability for the PSE to query the PD in order to determine the power requirements of that PD is called classification. The interrogation and power classification function is intended to establish mutual identification and is intended for use with advanced features such as power management.

Mutual identification is the mechanism that allows a Type 2 PD to differentiate Type 1 PSEs from Type 2 PSEs. Additionally, mutual identification allows Type 2 PSEs to differentiate between Type 1 and Type 2 PDs. PDs or PSEs that do not implement classification will not be able to complete mutual identification and can only perform as Type 1 devices.

There are two forms of classification: Physical Layer classification and Data Link Layer classification.

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Physical Layer classification occurs before a PSE supplies power to a PD when the PSE asserts a voltage onto the PI and the PD responds with a current representing a limited number of power classifications. Based on the response of the PD, the minimum power level at the output of the PSE is P_{Class} as shown in Equation (33–3). Physical Layer classification encompasses two methods, known as 1-Event Physical Layer classification (see 33.2.6.1) and 2-Event Physical Layer classification (see 33.2.6.2).

The minimum power output by the PSE for a particular PD class is defined by Equation (33–3). Alternatively, PSE implementations may use $V_{PSE} = V_{Port\_PSE}$ min and $R_{Chan} = R_{Ch}$ max to arrive at over-margined values as shown in Table 33–7.

$$P_{Class} = \left\{ V_{PSE} \times \left(\frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan} \times P_{Class\_PD}}}{2 \times R_{Chan}} \right) \right\}_W \quad (33–3)$$

where

V_{PSE} is the voltage at the PSE PI as defined in 33.1.4
R_{Chan} is the channel DC pair loop resistance
P_{Class_PD} is the PD's power classification (see Table 33–18)

Table 33–7—Physical Layer power classifications (P_{Class})

Class	Minimum power levels at output of PSE (P_{Class})
0	15.4 Watts
1	4.00 Watts
2	7.00 Watts
3	15.4 Watts
4	P_{Type} as defined in Table 33–11
NOTE 1—This is the minimum power at the PSE PI. For maximum power available to PDs, see Table 33–18. NOTE 2—Data Link Layer classification takes precedence over Physical Layer classification.	

With Data Link Layer classification, the PSE and PD communicate using the Data Link Layer Protocol (see 33.6) after the data link is established. The Data Link Layer classification has finer power resolution and the ability for the PSE and PD to participate in dynamic power allocation wherein allocated power to the PD may change one or more times during PD operation.

A PSE shall meet one of the allowable classification permutations listed in Table 33–8.

Subsequent to successful detection, a Type 1 PSE may optionally classify a PD using 1-Event Physical Layer classification. Valid classification results are Classes 0, 1, 2, 3, and 4, as listed in Table 33–7. If a Type 1 PSE does not implement classification, then the Type 1 PSE shall assign all PDs to Class 0. A Type 1 PSE may optionally implement Data Link Layer classification.

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Table 33–8—PSE and PD classification permutations

Permutations			PSE allowed?	PD allowed?
PSE/PD Type	Physical Layer classification	Data Link Layer classification		
Type 2	2-Event	No	Yes	No
		Yes	Yes	Yes
	1-Event	No	No	No
		Yes	Yes	No
	None	No	No	No
		Yes	No	No
Type 1	2-Event	No	No	Yes
		Yes	No	Yes
	1-Event	No	Yes	Yes
		Yes	Yes	Yes
	None	No	Yes	No
		Yes	Yes	No

Subsequent to successful detection, all Type 2 PSEs perform classification using at least one of the following: 2-Event Physical Layer classification; 2-Event Physical Layer classification and Data Link Layer classification; or 1-Event Physical Layer classification and Data Link Layer classification.

If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of a PD, then a Type 1 PSE shall either return to the IDLE state or assign the PD to Class 0; a Type 2 PSE shall return to the IDLE state.

33.2.6.1 PSE 1-Event Physical Layer classification

When 1-Event Physical Layer classification is implemented, classification consists of the application of V_{Class} and the measurement of I_{Class} in a single classification event—1-EVENT_CLASS—as defined in the state diagram in Figure 33–9.

The PSE shall provide to the PI V_{Class} with a current limitation of I_{Class_LIM}, as defined in Table 33–10. Polarity shall be the same as defined for V_{Port_PSE} in 33.2.3 and timing specifications shall be as defined by T_{pdc} in Table 33–10.

The PSE shall measure the resultant I_{Class} and classify the PD based on the observed current according to Table 33–9. All measurements of I_{Class} shall be taken after the minimum relevant class event timing in Table 33–10. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

If the result of the class event is Class 4, a Type 1 PSE shall assign the PD to Class 0; a Type 2 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the measured I_{Class} is within the range of I_{Class_LIM}, a Type 1 PSE shall either return to the IDLE state or classify the PD as Class 0; a Type 2 PSE shall return to the IDLE state.

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33.2.6.2 PSE 2-Event Physical Layer classification

When 2-Event Physical Layer classification is implemented, classification consists of the application of V_{Class} and the measurement of I_{Class} in a series of classification and mark events—CLASS_EV1, MARK_EV1, CLASS_EV2, and MARK_EV2—as defined in the state diagram in Figure 33–9.

The PSE in the state CLASS_EV1 shall provide to the PI V_{Class} as defined in Table 33–10. The timing specification shall be as defined by T_{CLE1} in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9.

When the PSE is in the state MARK_EV1, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME1} in Table 33–10.

When the PSE is in the state CLASS_EV2, the PSE shall provide to the PI V_{Class}, subject to the T_{CLE2} timing specification, as defined in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9.

When the PSE is in the state MARK_EV2, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME2} in Table 33–10.

The mark event states, MARK_EV1 and MARK_EV2, commence when the PI voltage falls below V_{Class} min and end when the PI voltage exceeds V_{Class} min. The V_{Mark} requirement is to be met with load currents in the range of I_{Mark} as defined in Table 33–17.

NOTE—In a properly operating system, the port may or may not discharge to the V_{Mark} range due to the combination of channel and PD capacitance and PD current loading. This is normal and acceptable system operation. For compliance testing, it is necessary to discharge the port in order to observe the V_{Mark} voltage. Discharge can be accomplished with a 2 mA load for 3 ms, after which V_{Mark} can be observed with minimum and maximum load current.

If any measured I_{Class} is equal to or greater than I_{Class_LIM} min as defined in Table 33–10, a Type 2 PSE shall return to the IDLE state. The class events shall meet the I_{Class_LIM} current limitation. The mark events shall meet the I_{Mark_LIM} current limitation. All measurements of I_{Class} shall be taken after the minimum relevant class event timing of Table 33–10. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

All class event voltages and mark event voltages shall have the same polarity as defined for V_{Port_PSE} in 33.2.3. The PSE shall complete 2-Event Physical Layer classification and transition to the POWER_ON state without allowing the voltage at the PI to go below V_{Mark} min. If the PSE returns to the IDLE state, it shall maintain the PI voltage at V_{Reset} for a period of at least T_{Reset} min before starting a new detection cycle.

If the result of the first class event is Class 4, the PSE may omit the subsequent mark and class events only if the PSE implements Data Link Layer classification. In this case, a Type 2 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the result of the first class event is any of Classes 0, 1, 2, or 3, the PSE treats the PD as a Type 1 PD and may omit the subsequent mark and class events and classify the PD according to the result of the first class event.

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Table 33–9—PD classification

Measured I_{Class}	Classification
0 mA to 5.00 mA	Class 0
> 5.00 mA and < 8.00 mA	May be Class 0 or 1
8.00 mA to 13.0 mA	Class 1
> 13.0 mA and < 16.0 mA	Either Class 1 or 2
16.0 mA to 21.0 mA	Class 2
> 21.0 mA and < 25.0 mA	Either Class 2 or 3
25.0 mA to 31.0 mA	Class 3
> 31.0 mA and < 35.0 mA	Either Class 3 or 4
35.0 mA to 45.0 mA	Class 4
> 45.0 mA and < 51.0 mA	Either Class 4 or invalid class

NOTE—A Type 1 PSE may ignore I_{Class} and report Class 0.

Table 33–10—PSE Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	1- or 2-Event	Additional information
1	Class event voltage	V_{Class}	V	15.5	20.5	1, 2	
2	Class event current limitation	I_{Class_LIM}	A	0.051	0.100	1, 2	
3	Mark event voltage	V_{Mark}	V	7.00	10.0	2	
4	Mark event current limitation	I_{Mark_LIM}	A	0.005	0.100	2	
5	1st class event timing	T_{CLE1}	ms	6.00	30.0	2	
6	1st mark event timing	T_{ME1}	ms	6.00	12.0	2	
7	2nd class event timing	T_{CLE2}	ms	6.00	30.0	2	
8	2nd mark event timing	T_{ME2}	ms	6.00		2	Time from end of detection until power-on is limited by 33.2.7.12.
9	Classification reset voltage	V_{Reset}	V	0	2.80	2	
10	Classification reset timing	T_{Reset}	ms	15.0		2	
11	1-Event Physical Layer classification timing	T_{pdc}	ms	6.00	75.0	1	

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33.2.7 Power supply output

PSE behavior conforms to the state diagrams in Figure 33–9, Figure 33–9 continued, and Figure 33–10. When the PSE provides power to the PI, it shall conform with Table 33–11.

Table 33–11 limits show values that support worst-case operating limits. These ranges may be narrowed when additional information is known and applied in accordance with this specification.

Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
1	Output voltage in the POWER_ON state	V_{Port_PSE}	V	44.0	57.0	1	See 33.2.7.1.
				50.0	57.0	2	
2	Voltage transient below V_{Port_PSE} min	K_{Tran_lo}	%		7.6	2	See 33.2.7.2.
3	Power feeding ripple and noise:						
	f < 500 Hz		V_{pp}		0.500	1, 2	See 33.2.7.3.
	500 Hz to 150 kHz				0.200		
	150 kHz to 500 kHz				0.150		
	500 kHz to 1 MHz				0.100		
4	Continuous output current capability in POWER_ON state	I_{Con}	A	P_{Class} / V_{Port_PSE}		1, 2	See 33.2.7.4.
5	Output current in POWER_UP state	I_{Inrush}	A	0.400	See info	1, 2	See 33.2.7.5. Max value defined by Figure 33–13.
6	Inrush time	T_{Inrush}	s	0.050	0.075	1, 2	See 33.2.7.5
7	Overload current detection range	I_{CUT}	A	P_{Class} / V_{Port_PSE}	I_{LIM}	1,2	Optional limit; see 33.2.7.6, Table 33–7.
8	Overload time limit	T_{CUT}	s	0.050	0.075	1, 2	See 33.2.7.7.
9	Output current – at short circuit condition	I_{LIM}	A	0.400	See info	1	See 33.2.7.7. Max value defined by Figure 33–14.
				1.14 × I_{Cable}		2	
10	Short circuit time limit	T_{LIM}	s	0.050	See info	1	See 33.2.7.7.
				0.010		2	
11	Continuous output power capability in POWER_ON state	P_{Con}	W	P_{Class}		1, 2	See 33.2.7.10, Table 33–7.
12	PSE Type power minimum	P_{Type}	W	I_{Cable} × (V_{Port_PSE} min)		1, 2	See 33.1.4.
13	Power turn on time	T_{pon}	s		0.400	1, 2	See 33.2.7.12.

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Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
14	Turn on rise time	T_{Rise}	µs	15.0		1, 2	From 10 % to 90 % of the voltage difference at the PI in POWER_ON state from the beginning of POWER_UP.
15	Turn off time	T_{Off}	s		0.500	1, 2	See 33.2.7.8.
16	Turn off voltage	V_{Off}	V		2.80	1, 2	See 33.2.7.9.
17	DC MPS current	I_{Hold}	A	0.005	0.010	1, 2	See 33.2.9.1.2.
18	PD Maintain Power Signature dropout time limit	T_{MPDO}	s	0.300	0.400	1, 2	See 33.2.9.
19	PD Maintain Power Signature time for validity	T_{MPS}	s	0.060		1, 2	See 33.2.9.
20	Current unbalance	I_{unb}	A		3 % × I_{Cable}	1	See 33.2.7.11, 33.4.8. NOTE—For practical implementations, it is recommended that Type 1 PSEs support Type 2 I_{unb} requirements.
					3 % × I_{Peak}	2	
21	Alternative B detection backoff time	T_{dbo}	s	2.00		1, 2	
22	Output capacitance during detection state	C_{out}	µF		0.520	1, 2	
23	Detection timing	T_{det}	s		0.500	1, 2	Time to complete detection of a PD.
24	Error delay timing	T_{ed}	s	0.750		1, 2	Delay before PSE may attempt subsequent powering after power removal because of error condition.

33.2.7.1 Output voltage in the POWER_ON state

The specification for V_{Port_PSE} in Table 33–11 shall be met with a (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min load step at a rate of change of up to 15 mA/µs. The voltage transients as a result of load changes up to 35 mA/µs shall be limited to 3.5 V/µs max.

A PSE in the POWER_ON state may remove power from the PI when the PI voltage no longer meets the V_{Port_PSE} specification.

33.2.7.2 Voltage transients

A Type 2 PSE shall maintain an output voltage no less than K_{Tran_lo} below V_{Port_PSE} min for transient conditions lasting more than 30 µs and less than 250 µs, and meet the requirements of 33.2.7.7.

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Transients less than 30 µs in duration may cause the voltage at the PI to fall more than K_{Tran_lo}. The minimum PD input capacitance allows the PD to operate for any input voltage transient lasting less than 30 µs. Transients lasting more than 250 µs shall meet the V_{Port_PSE} specification.

33.2.7.3 Power feeding ripple and noise

The specification for power feeding ripple and noise in Table 33–11 shall be met for common-mode and/or pair-to-pair noise values for power outputs from (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min for PSEs at static operating $V_{Port\_PSE.}$ The limits are meant to preserve data integrity. To meet EMI standards, lower values may be needed. For higher frequencies, see 33.4.4 and 33.4.5.

33.2.7.4 Continuous output current capability in the POWER_ON state

In addition to I_{Con} as specified in Table 33–11, the PSE shall support the following AC current waveform parameters, while within the operating voltage range of V_{Port_PSE}:

I_{Peak} minimum for T_{CUT} minimum and 5 % duty cycle minimum, where

$$I_{\text{Peak}} = \left\{ \frac{V_{\text{PSE}} - \sqrt{V_{\text{PSE}}^2 - 4(R_{\text{Chan}})(P_{\text{Peak\_PD}})}}{2(R_{\text{Chan}})} \right\}_{\text{A}} \tag{33–4}$$

where

V_{PSE} is the voltage at the PSE PI as defined in 33.1.4

R_{Chan} is the channel loop resistance as defined in 33.1.4; this parameter has a worst-case value of R_{Ch}, defined in Table 33–1

$P_{\text{Peak\_PD}}$ is the peak power a PD may draw for its class; see Table 33–18

33.2.7.5 Output current in POWER_UP mode

POWER_UP mode occurs between the PSE's transition to the POWER_UP state and either the expiration of T_{Inrush} or the conclusion of PD inrush currents (see 33.3.7.3). However, for practical implementations, it is recommended that the POWER_UP mode persist for the complete duration of T_{Inrush}, as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior.

The PSE shall limit the maximum current sourced at the PI during POWER_UP. The maximum inrush current sourced by the PSE shall not exceed the PSE inrush template in Figure 33–13.

a) During POWER_UP, for PI voltages between 0 V and 10 V, the minimum I_{Inrush} requirement is 5 mA.
b) During POWER_UP, for PI voltages between 10 V and 30 V, the minimum I_{Inrush} requirement is 60 mA.
c) During POWER_UP, for PI voltages above 30 V, the minimum I_{Inrush} requirement is as specified in Table 33–11.
d) For Type 1 PSE, measurement of minimum I_{Inrush} requirement to be taken after 1 ms to allow startup transients. A Type 2 PSE that uses 1-Event physical layer classification, and requires the 1 ms settling time, shall power up a class 4 PD as if it used 2-Event physical layer classification.

The PSE inrush template, I_{PSEIT}, is defined by the following segments:

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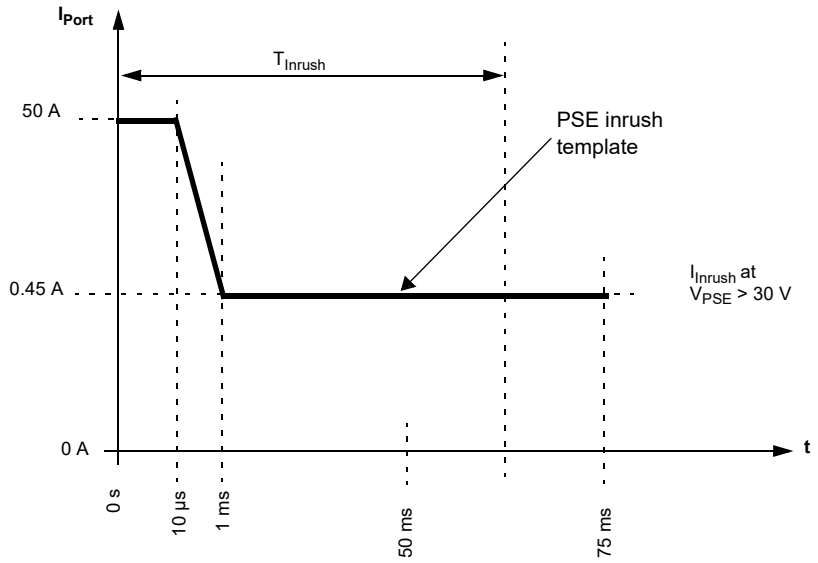

Figure 33–13—I_{Inrush} current and timing limits in POWER_UP state

$$I_{\mathrm{PSEIT}}(t) = \begin{cases} 50.0 & \text{for } 0 < t < 10.0\times10^{-6} \\ 50.0 - \dfrac{\left(t - 10.0\times10^{-6}\right) \times 49.6}{0.990\times10^{-6}} & \text{for } 10.0\times10^{-6} \le t < 0.001 \\ 0.450 & 0.001 \le t < 0.075 \end{cases} \quad (33\text{–}5)$$

where

t is the time in seconds

33.2.7.6 Overload current

If I_{Port}, the current supplied by the PSE to the PI, exceeds I_{CUT} for longer than T_{CUT}, the PSE may remove power from the PI. The cumulative duration of T_{CUT} is measured with a sliding window of at least 1 second width.

The I_{CUT} threshold may equal the I_{Peak} value determined by Equation (33–4).

33.2.7.7 Output current—at short circuit condition

A PSE may remove power from the PI if the PI current meets or exceeds the “PSE lowerbound template” in Figure 33–14. Power shall be removed from the PI of a PSE before the PI current exceeds the “PSE upperbound template” in Figure 33–14.

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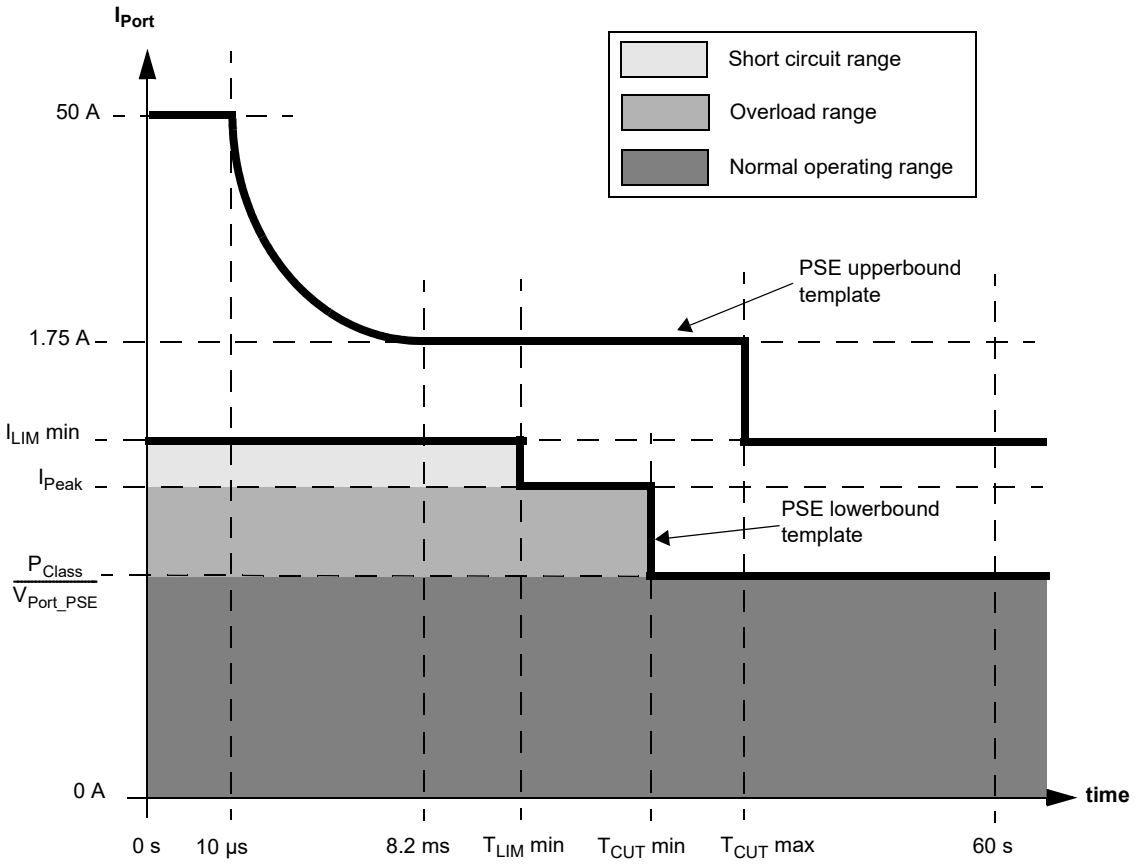

Figure 33–14—POWER_ON state PI operating current templates

The maximum value of I_{LIM} is the PSE upperbound template described by Equation (33–6) and Figure 33–14.

The PSE upperbound template, I_{PSEUT}, is defined by the following segments:

$$I_{\mathrm{PSEUT}}(t) = \left\{ \begin{array}{ll} 50.0 & \text{for } \left(0 \le t < 10.0\times10^{-6}\right) \\ \sqrt{\frac{K}{t}} & \text{for } \left(10.0\times10^{-6} \le t < 8.20\times10^{-3}\right) \\ 1.75 & \text{for } \left(8.20\times10^{-3} \le t < T_{\mathrm{cutmax}}\right) \\ I_{\mathrm{limmin}} & \text{for } \left(T_{\mathrm{cutmax}} \le t\right) \end{array} \right\} \quad (33\text{–}6)$$

where

t	is the duration in seconds that the PSE sources I_{Port}
K	is 0.025 A^2s, an energy limitation constant for the port current when it is not in steady state normal operation
T_{cutmax}	is T_{CUT} max, as defined in Table 33–11
I_{limmin}	is I_{LIM} min, as defined in Table 33–11

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The PSE shall limit the current to I_{LIM} for a duration of up to T_{LIM} in order to account for PSE dV/dt transients at the PI. The cumulative duration of T_{LIM} may be measured with a sliding window.

The PSE lowerbound template, I_{PSELT}, is defined by the following segments:

$$I_{PSELT}(t) = \left\{ \begin{array}{ll} I_{LIMmin} & \text{for } (0 \le t < T_{limmin}) \\ I_{Peak} & \text{for } (T_{limmin} \le t < T_{cutmin}) \\ \dfrac{P_{Class}}{V_{PSE}} & \text{for } (T_{cutmin} \le t) \end{array} \right\}_{A} \quad (33\text{–}7)$$

where

I_{LIMmin} is the I_{LIM} min value for the PSE (see Table 33–11)
t is the duration that the PI sources I_{Port}
T_{limmin} is T_{LIM} min as defined in Table 33–11
T_{cutmin} is T_{CUT} min, as defined in Table 33–11
I_{Peak} is I_{Peak}, as defined in Equation (33–4)
P_{Class} is P_{Class}, as defined in Table 33–7
V_{PSE} is the voltage at the PSE PI

If a short circuit condition is detected, power removal from the PI shall begin within T_{LIM} as specified in Table 33–11. If I_{Port} exceeds the PSE lowerbound template, the PSE output voltage may drop below V_{Port_PSE} min.

33.2.7.8 Turn off time

The specification for T_{Off} in Table 33–11 shall apply to the discharge time from V_{Port_PSE} to V_{Off} with a test resistor of 320 kΩ attached to the PI. In addition, it is recommended that the PI be discharged when turned off. T_{Off} starts when V_{PSE} drops 1 V below the steady-state value after the pi_powered variable is cleared (see Figure 33–9). T_{Off} ends when $V_{PSE} \le V_{Off}$ max. The IDLE state is the state when the PSE is not in detection, classification, or normal powering states.

33.2.7.9 Turn off voltage

The specification for V_{Off} in Table 33–11 shall apply to the PI voltage in the IDLE State.

33.2.7.10 Continuous output power capability in POWER_ON state

P_{Class} is the class power defined in 33.2.6 and Equation (33–3), or PSE allocated power (as defined in 79.3.2.6) added to the channel power loss.

P_{Con} is valid over the range of V_{Port_PSE} defined in Table 33–11. Measurement of P_{Con} should be averaged using any sliding window with a width of 1 s.

A PSE may remove power from a PD that causes the PSE to source more than P_{Class}.

33.2.7.11 Current unbalance

The specification for I_{unb} in Table 33–11 shall apply to the current unbalance between the two conductors of a power pair over the current load range.

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Type 2 Endpoint PSEs shall meet the requirements of 25.4.5 in the presence of (I_{unb} / 2).

33.2.7.12 Power turn on time

The specification for T_{pon} in Table 33–11 applies to the PSE power up time for a PD after completion of detection. If power is not applied as specified, a new detection cycle is initiated (see 33.2.4.1).

33.2.7.13 PSE stability

When connected together as a system, the PSE and PD might exhibit instability at the PSE side or the PD side or both due to the presence of negative impedance at the PD input. See Annex 33A for PSE design guidelines for stable operation.

33.2.8 Power supply allocation

A PSE does not initiate power provision to a link if the PSE has less than Class 3 power available and the connected PD requests more than the available power.

The PSE may manage the allocation of power based on additional information beyond the classification of the attached PD. Allocating power based on additional information about the attached PD, and the mechanism for obtaining that additional information, is beyond the scope of this standard with the exception that the allocation of power shall not be based solely on the historical data of the power consumption of the attached PD.

See 33.6 for a description of Data Link Layer classification.

If the system implements a power allocation algorithm, no additional behavioral requirement is placed on the system as it approaches or reaches its maximum power subscription. Specifically, the interaction between one PSE PI and another PSE PI in the same system is beyond the scope of this standard.

33.2.9 PSE power removal

Figure 33–10 shows the PSE monitor state diagrams. These state diagrams monitor for inrush current and the absence of the Maintain Power Signature (MPS).

If any of these conditions exist for longer than its related time limit, the power is removed from the PI.

33.2.9.1 PSE Maintain Power Signature (MPS) requirements

The MPS consists of two components, an AC MPS component and a DC MPS component.

The PSE shall monitor either the DC MPS component, the AC MPS component, or both.

33.2.9.1.1 PSE AC MPS component requirements

A PSE that monitors the AC MPS component shall meet the “AC Signal parameters” and “PSE PI voltage during AC disconnect detection” parameters in Table 33–12.

A PSE shall consider the AC MPS component to be present when it detects an AC impedance at the PI equal to or lower than $|Z_{ac1}|$ as defined in Table 33–12.

A PSE shall consider the AC MPS component to be absent when it detects an AC impedance at the PI equal to or greater than $|Z_{ac2}|$ as defined in Table 33–12. Power shall be removed from the PI when AC MPS has been absent for a time duration greater than T_{MPDO}.

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A PSE may consider the AC MPS component to be either present or absent when it detects a AC impedance between the values $|Z_{ac1}|$ max and $|Z_{ac2}|$ min.

33.2.9.1.2 PSE DC MPS component requirements

A PSE shall consider the DC MPS component to be present if I_{Port} is greater than or equal to I_{Hold} max for a minimum of T_{MPS}. A PSE shall consider the DC MPS component to be absent if I_{Port} is less than or equal to I_{Hold} min. A PSE may consider the DC MPS component to be either present or absent if I_{Port} is in the range of I_{Hold}.

Power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component. In addition to the requirements on T_{MPS} and T_{MPDO} in Table 33–11, the PSE shall use values for T_{MPS} and T_{MPDO} that meet Equation (33–8).

$$T_{MPDO} - T_{MPS} \geq 250 \text{ ms} \tag{33–8}$$

The PSE shall not remove power from the port when less than T_{MPDO} has passed since MPS was last present. This allows a PD to minimize its power consumption.

Table 33–12—PSE PI parameters for AC disconnect-detection function

Item	Parameter	Symbol	Unit	Min	Max	Additional information
	AC signal parameters					
1a	PI probing AC voltage	V_open	V_{pp}	1.90	10% of the average value of V_{Port_PSE} within the limits of Table 33–11	Includes noise, ripple, etc. V_open is the AC voltage across the PI when the PD is not connected to the PI and before the detection of this condition by the PSE.
		V_open1	V_p		30.0 V, $V_{PSE} \leq$ 44.0 V	V_open1 is the AC voltage across the PI when the PD is not connected to the PI and after the detection of this condition by the PSE and the removal of power from the PI.
1b	AC probing signal frequency	F_p	kHz		0.500	
1c	AC probing signal slew rate	SR	V/µs		0.100	Positive or negative.
	AC source output impedance					
2a	Source output current during the operation of the AC disconnect detection function	I_sac	mA		5.00	During operation of the AC disconnect detection function.

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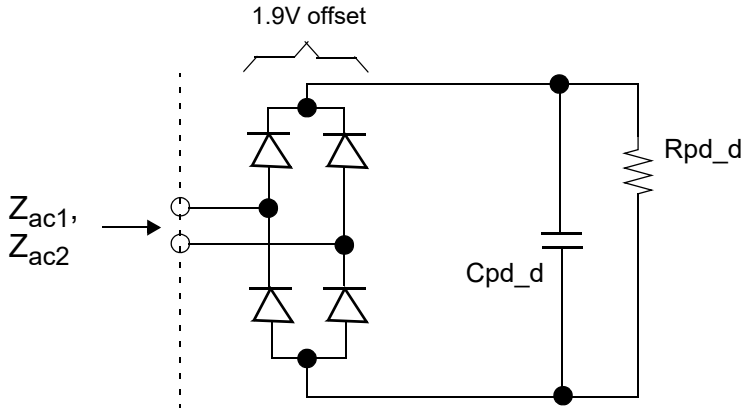
Table 33–12—PSE PI parameters for AC disconnect-detection function *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Additional information
2b	PSE PI impedance during PD detection when measured at the PSE PI	R_rev	kΩ	45.0		Specified in 33.2.5.1 and Figure 33–11. Shown here to clarify the difference in PI impedance during the signature detection function.
	PSE PI voltage during AC disconnect detection					
3a	PI AC voltage when PD is connected	V_{CLOSE}	V_{pp}			See Table 33–11, item 3.
3b	PI voltage when PD is disconnected	V_{PSE}	V_p		60.0	
	AC Maintain Power Signature					
4a	Valid impedance	$\lvert Z_{ac1} \rvert$	kΩ		27.0	F_p = 5 Hz, Testing voltage >2.5 V. See Figure 33–15.
4b	Invalid impedance	$\lvert Z_{ac2} \rvert$	kΩ	1980		See Figure 33–15.



NOTE—Rpd_d and Cpd_d are specified in Table 33–19. Cpd_d may be located either in parallel with Z_{ac1} or as shown above.

Figure 33–15—Z_{ac1} and Z_{ac2} definition as indicated in Table 33–12

33.3 Powered devices (PDs)

A PD is the portion of a device that is either drawing power or requesting power by participating in the PD detection algorithm. A device that is capable of becoming a powered device may or may not have the ability to draw power from an alternate power source and, if doing so, may or may not require power from the PI. PD capable devices that are neither drawing nor requesting power are also covered in this subclause.

A PD is specified at the point of the physical connection to the cabling. Characteristics such as the losses due to voltage correction circuits, power supply inefficiencies, separation of internal circuits from external

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ground or other characteristics induced by circuits after the PI connector are not specified. Limits defined for the PD are specified at the PI, not at any point internal to the PD, unless specifically stated.

33.3.1 PD PI

The PD shall be capable of accepting power on either of two sets of PI conductors. The two conductor sets are named Mode A and Mode B. In each four-wire connection, the two wires associated with a pair are at the same nominal average voltage. Figure 33–8 in conjunction with Table 33–13 illustrates the two power modes.

Table 33–13—PD pinout

Conductor	Mode A	Mode B
1	Positive V_{PD}, Negative V_{PD}	
2	Positive V_P, Negative V_{PD}	
3	Negative V_{PD}, Positive V_{PD}	
4		Positive V_{PD}, Negative V_{PD}
5		Positive V_{PD}, Negative V_{PD}
6	Negative V_{PD}, Positive V_{PD}	
7		Negative V_{PD}, Positive V_{PD}
8		Negative V_{PD}, Positive V_{PD}

The PD shall be implemented to be insensitive to the polarity of the power supply and shall be able to operate per the PD Mode A column and the PD Mode B column in Table 33–13.

NOTE—PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this clause. A PD may indicate the ability to accept power on both pairsets from a Clause 145 PSE using TLV variable PD 4PID; see 79.3.2.4.3.

The PD shall not source power on its PI.

The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.

33.3.2 PD type descriptions

PDs can be categorized as either Type 1 or Type 2.

Type 1 PDs implement a minimum of 1-Event Physical Layer classification and advertise a 1-Event class signature of 0, 1, 2, or 3.

Type 2 PDs implement both 2-Event Physical Layer classification (see 33.3.5.2) and Data Link Layer classification (see 33.6) and advertise a 2-Event class signature of 4.

The maximum power a PD expects to draw from a PSE is P_{Class_PD} max as defined in Table 33–18.

A Type 2 PD that does not successfully observe a 2-Event Physical Layer classification or Data Link Layer classification shall conform to Type 1 PD power restrictions and shall provide the user with an active indication if underpowered. The method of active indication is left to the implementer.

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Type 2 PDs shall meet the requirements of 25.4.5 in the presence of (I_{unb} / 2).

33.3.3 PD state diagram

The PD state diagram specifies the externally observable behavior of a PD. The PD shall provide the behavior of the state diagram shown in Figure 33–16.

33.3.3.1 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in 21.5.

33.3.3.2 Constants

The PD state diagram uses the following constants:

V_{Reset_th}
: Reset voltage threshold (see Table 33–17)

V_{Mark_th}
: Mark event voltage threshold (see Table 33–17)

class_sig
: PD classification, one of either 0, 1, 2, 3, or 4 (see Table 33–16)

33.3.3.3 Variables

The PD state diagram uses the following variables:

mdi_power_required
: A control variable indicating the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner.
Values:FALSE:PD functionality is disabled.
TRUE:PD functionality is enabled.

pd_2-event
: A control variable indicating whether the PD presents a 2-Event class signature.
Values:FALSE:PD does not present a 2-Event class signature.
TRUE:PD does present a 2-Event class signature.

pd_dll_capable
: This variable indicates whether the PD implements Data Link Layer classification.
Values:FALSE:The PD does not implement Data Link Layer classification.
TRUE:The PD does implement Data Link Layer classification.

pd_dll_enabled
: A variable indicating whether the Data Link Layer classification mechanism is enabled.
Values:FALSE:Data Link Layer classification is not enabled.
TRUE:Data Link Layer classification is enabled.

pd_max_power
: A control variable indicating the max power that the PD may draw from the PSE. See power classifications in Table 33–18.
Values:0: PD may draw Class 0 power
1: PD may draw Class 1 power
2: PD may draw Class 2 power
3: PD may draw Class 3 power
4: PD may draw Class 4 power

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pd_reset
: An implementation-specific control variable that unconditionally resets the PD state diagram to the OFFLINE state.
Values:FALSE:The device has not been reset (default).
TRUE:The device has been reset.

power_received
: An indication from the circuitry that power is present on the PD's PI.
Values:FALSE:The input voltage does not meet the requirements of V_{Port_PD} in Table 33–18.
TRUE:The input voltage meets the requirements of V_{Port_PD}.

present_class_sig
: Controls presenting the classification signature (see 33.3.5) by the PD.
Values:FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

present_det_sig
: Controls presenting the detection signature (see 33.3.4) by the PD.
Values:FALSE:A non-valid PD detection signature is to be applied to the link.
TRUE:A valid PD detection signature is to be applied to the link.

present_mark_sig
: Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD.
Values:FALSE:The PD does not present mark event behavior.
TRUE:The PD does present mark event behavior.

present_mps
: Controls applying MPS (see 33.3.8) to the PD's PI.
Values:FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
TRUE:The MPS is to be applied to the PD's PI.

pse_dll_power_type
: A control variable initially output by the PD power control state diagram (Figure 33–28), which can be updated by LLDP (see Table 33–26), that indicates the type of PSE by which the PD is being powered.
Values:1: The PSE is a Type 1 PSE (default).
2: The PSE is a Type 2 PSE.

pse_power_type
: A control variable that indicates to the PD the type of PSE by which it is being powered.
Values:1: The PSE is a Type 1 PSE.
2: The PSE is a Type 2 PSE.

V_{PD}
: Voltage at the PD PI as defined in 33.1.4.

33.3.3.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

tpowerdly_timer
: A timer used to prevent the Type 2 PD from drawing more than inrush current during the PSE's inrush period; see T_{delay} in Table 33–18.

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33.3.3.5 State diagrams

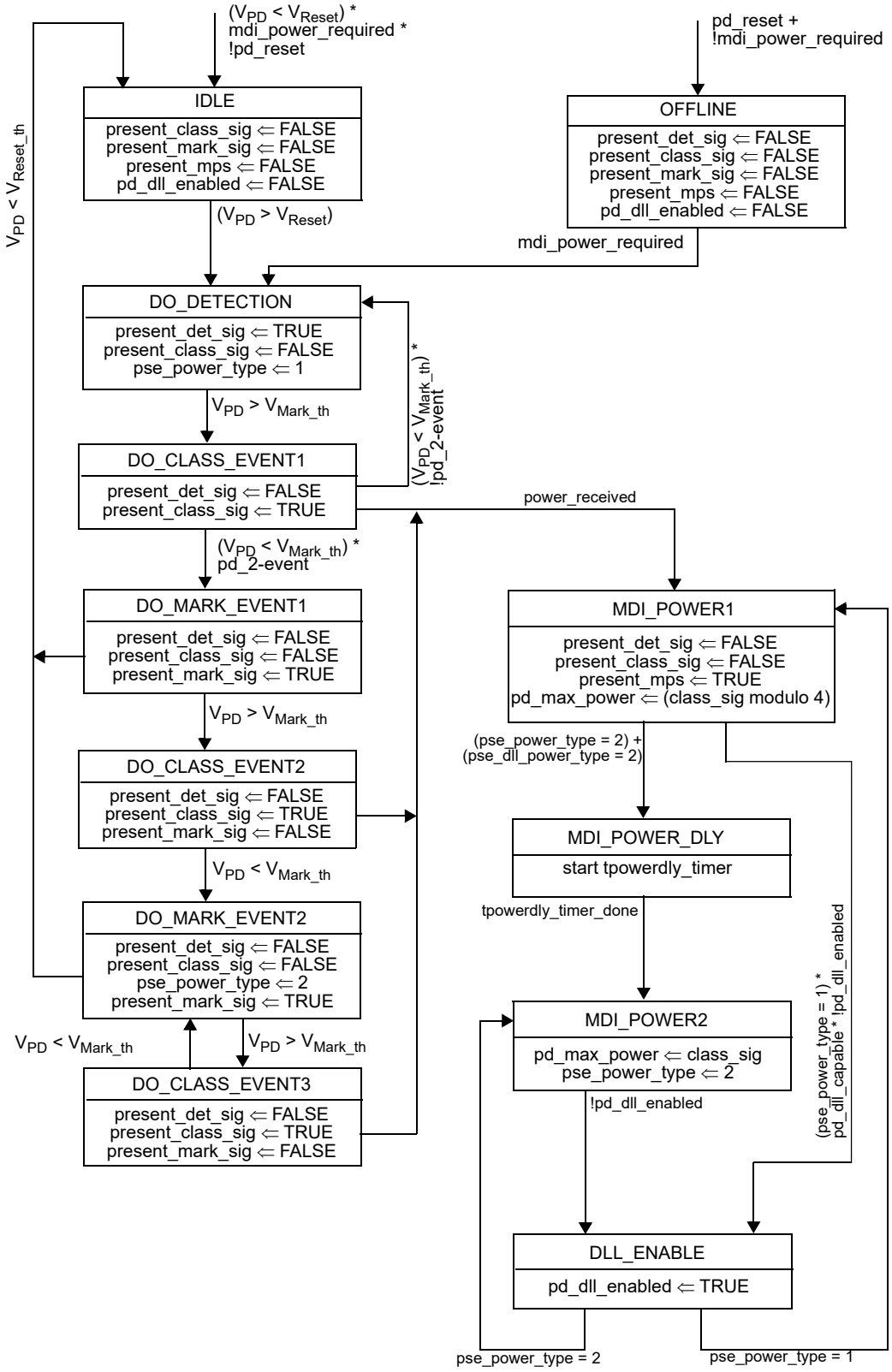

Figure 33–16—PD state diagram

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NOTE 1—DO_CLASS_EVENT3 creates a defined behavior for a Type 2 PD that is brought into the classification range repeatedly.

NOTE 2—In general, there is no requirement for a PD to respond with a valid classification signature for any DO_CLASS_EVENT duration less than T_{class}.

33.3.4 PD valid and non-valid detection signatures

A PD presents a valid detection signature while it is in a state where it accepts power via the PI, but is not powered via the PI per Figure 33–16.

A PD presents a non-valid detection signature at the PI while it is in a state where it does not accept power via the PI per Figure 33–16.

A Type 2 PD presents a non-valid detection signature when in a mark event state per Figure 33–16.

When a PD presents a valid or non-valid detection signature, it shall present the detection signature at the PI between Positive V_{PD} and Negative V_{PD} of PD Mode A and PD Mode B as defined in 33.3.1. When a PD becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs from which it is not drawing power.

A PD may or may not present a valid detection signature when in the IDLE state.

The detection signature is a resistance calculated from two voltage/current measurements made during the detection process.

$$R_{\text{detect}} = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \tag{33–9}$$

where

V_1 and V_2	are the first and second voltage measurements made at the PD PI, respectively
I_1 and I_2	are the first and second current measurements made at the PD PI, respectively
R_{detect}	is the effective resistance

A valid PD detection signature shall have the characteristics of Table 33–14.

A non-valid detection signature shall have one or both of the characteristics in Table 33–15.

A PD that presents a signature outside of Table 33–14 is non-compliant, while a PD that present the signature of Table 33–15 is assured to fail detection.

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Table 33–14—Valid PD detection signature characteristics, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
R_{detect} (at any 1 V or greater chord within the voltage range conditions)	2.70 V to 10.1 V	23.7	26.3	kΩ
V offset	See Figure 33–17	0	1.90	V
Voltage at the PI	I_{Port} = 124 μA	2.70		V
Input capacitance	2.70 V to 10.1 V	0.050	0.120	μF
Series input inductance	2.70 V to 10.1 V		0.100	mH

Table 33–15—Non-valid PD detection signature characteristics, measured at PD input connector

Parameter	Conditions	Range of values	Unit
R_{detect}	V < 10.1 V	Either greater than 45.0 or less than 12.0	kΩ
Input capacitance	V < 10.1 V	Greater than 10.0	μF

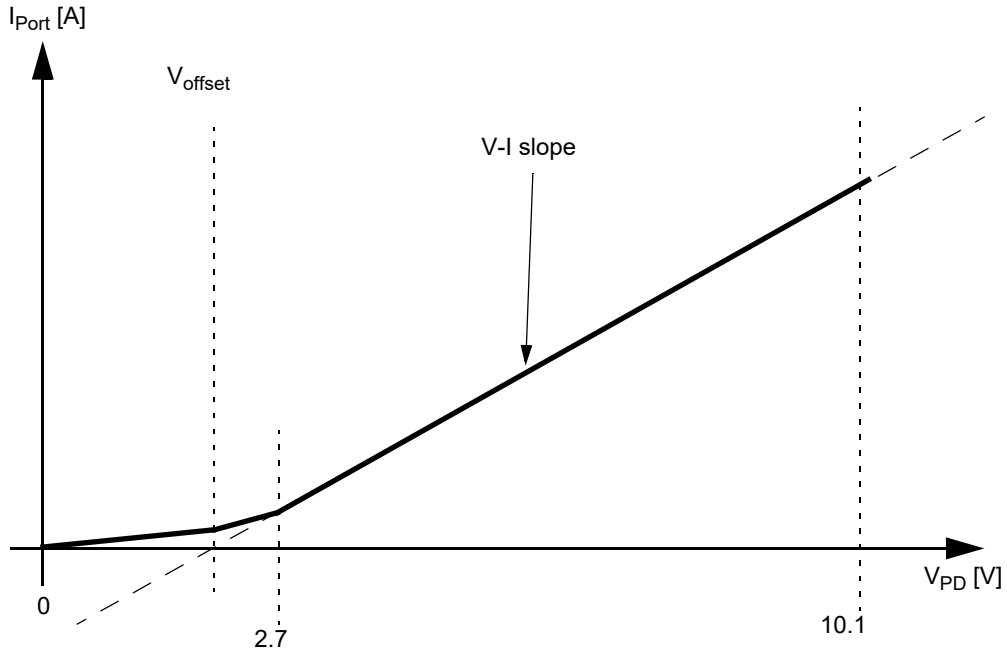

Figure 33–17—Valid PD detection signature offset

33.3.5 PD classifications

See 33.2.6 for a general description of classification mechanisms.

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A PD may be classified by the PSE based on the Physical Layer classification information, Data Link Layer classification, or a combination of both provided by the PD. The intent of PD classification is to provide information about the maximum power required by the PD during operation. Additionally, classification is used to establish mutual identification between Type 2 PSEs and Type 2 PDs.

The method of classification depends on the type of the PD and the type of the attached PSE.

A PD shall meet at least one of the allowable classification permutations listed in Table 33–8.

A Type 1 PD may implement any of the class signatures in 33.3.5 and 33.6.

Type 2 PDs implement both 2-Event class signature (see 33.3.5.2) and Data Link Layer classification (see 33.6).

PD classification behavior conforms to the state diagram in Figure 33–16.

33.3.5.1 PD 1-Event class signature

Class 0 is the default for PDs. However, to improve power management at the PSE, a Type 1 PD may opt to provide a signature for Class 1 to 3.

The PD is classified based on power. The Physical Layer classification of the PD is the maximum power that the PD draws across all input voltages and operational modes.

PDs implementing a 2-Event class signature shall return Class 4 in accordance with the maximum power draw, P_{Class_PD}, as specified in Table 33–18. Since 1-Event classification is a subset of 2-Event classification, Type 2 PDs respond to 1-Event classification with a Class 4 signature. Type 1 PDs may choose to implement a 2-Event class signature and return Class 0, 1, 2, or 3 in accordance with the maximum power draw, P_{Class_PD}. The Type 2 PD's classification behavior shall conform to the electrical specifications defined by Table 33–17.

In addition to a valid detection signature, PDs shall provide the characteristics of a classification signature as specified in Table 33–16. A PD shall present one, and only one, classification signature during classification.

Table 33–16—Classification signature, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
Current for Class 0	14.5 V to 20.5 V	0	4.00	mA
Current for Class 1	14.5 V to 20.5 V	9.00	12.0	mA
Current for Class 2	14.5 V to 20.5 V	17.0	20.0	mA
Current for Class 3	14.5 V to 20.5 V	26.0	30.0	mA
Current for Class 4	14.5 V to 20.5 V	36.0	44.0	mA

33.3.5.2 PD 2-Event class signature

PDs implementing a 2-Event class signature shall return a Class 4 classification signature in accordance with the maximum power draw, P_{Class_PD}, as specified by Table 33–18. The PD's classification behavior shall conform to the electrical specifications defined by Table 33–17.

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Until successful 2-Event Physical Layer classification or Data Link Layer classification has completed, a Type 2 PD's pse_power_type state variable is set to '1.' A Type 2 PD shall conform to the electrical requirements as defined by Table 33–18 for the type defined in its pse_power_type state variable.

Table 33–17—2-Event Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional information
1	Class event voltage	V_{Class}	V	14.5	20.5	
2	Mark event voltage	V_{Mark}	V	6.90	10.1	
3	Mark event current	I_{Mark}	mA	0.250	4.00	See 33.3.5.2.1
4	Mark event threshold	V_{Mark_th}	V	10.1	14.5	See 33.3.5.2.1
5	Classification reset threshold	V_{Reset_th}	V	2.81	6.90	See 33.3.5.2.1
6	Classification reset voltage	V_{Reset}	V	0	2.81	See 33.3.5.2.1

33.3.5.2.1 Mark Event behavior

When the PD is presenting a mark event signature as shown in the state diagram of Figure 33–16, the PD shall draw I_{Mark} as defined in Table 33–17 and present a non-valid detection signature as defined in Table 33–15.

The PD shall not exceed the I_{Mark} current limits when voltage at the PI enters the V_{Mark} specification as defined in Table 33–17.

V_{Mark_th} is the PI voltage threshold at which the PD implementing 2-Event class signature transitions into and out of the DO_CLASS_EVENT1 or DO_CLASS_EVENT2 states as shown in Figure 33–16.

The PD shall draw I_{Mark} until the PD transitions from a DO_MARK_EVENT state to the IDLE state.

V_{Reset_th} is the PI voltage threshold at which the PD implementing 2-Event class signature transitions from a DO_MARK_EVENT state to the IDLE state as shown in Figure 33–16.

33.3.6 PSE Type identification

A Type 2 PD shall identify the PSE Type as either Type 1 or Type 2 (see Figure 33–16).

The default value of pse_power_type is 1. After a successful 2-Event Physical Layer classification or Data Link Layer classification has completed, the pse_power_type is set to 2.

The PD resets the pse_power_type to '1' when the PD enters the DO_DETECTION state.

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33.3.7 PD power

The power supply of the PD shall operate within the characteristics in Table 33–18.

The PD may be capable of drawing power from a local power source. When a local power source is provided, the PD may draw some, none, or all of its power from the PI.

Table 33–18—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
1	Input voltage	V_{Port_PD}	V	37.0	57.0	1	See 33.3.7.1, Table 33–1
				42.5	57.0	2	
2	Transient operating input voltage	V_{Tran_lo}	V	36.0		2	For time duration defined in 33.2.7.2
3	Input voltage range during overload	$V_{Overload}$	V	36.0	57.0	1	See 33.3.7.4, Table 33–1
				41.4	57.0	2	
4	Input average power, Class 0 and Class 3	P_{Class_PD}	W		13.0	1	See 33.3.7.2, Table 33–1
	Input average power, Class 1				3.84	1	
	Input average power, Class 2				6.49	1	
	Input average power, Class 4				25.5	2	
5	Input inrush current	I_{Inrush_PD}	A		0.400	1, 2	Peak value—See 33.3.7.3
6	Inrush to operating state delay	T_{delay}	s	0.080		2	See 33.3.7.3
7	Peak operating power, Class 0 and Class 3	P_{Peak_PD}	W		14.4	1	See 33.3.7.4
	Peak operating power, Class 1				5.00	1	
	Peak operating power, Class 2				8.36	1	
	Peak operating power, Class 4				$1.11 \times P_{Class\_PD}$	2	
8	Input current transient (absolute value)		mA/µs		4.70	1, 2	See 33.3.7.5
9	PI capacitance during MDI_POWER states	C_{Port}	µF	5.00		1, 2	See 33.3.7.6, 33.3.7.3

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Table 33–18—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
10	Ripple and noise, < 500 Hz		V_{PP}		0.500	1, 2	See 33.3.7.7. Balanced source impedance: R_{Ch}
	Ripple and noise, 500 Hz to 150 kHz				0.200		
	Ripple and noise, 150 kHz to 500 kHz				0.150		
	Ripple and noise, 500 kHz to 1 MHz				0.100		
11	a) PD Power supply turn on voltage	V_{On}	V	30.0	42.0	1, 2	See 33.3.7.1
	b) PD power supply turn off voltage	V_{Off}	V	30.0		1, 2	
12	PD classification stability time	T_{class}	s		0.005		See 33.3.7.8
13	Backfeed voltage	V_{bfd}	V		2.80		See 33.3.7.9

33.3.7.1 Input voltage

The specification for V_{Port_PD} in Table 33–18 is for the input voltage range after startup (see 33.3.7.3), and accounts for loss in the cabling plant. Note, $V_{PD} = V_{PSE} - (R_{Chan} \times I_{Port})$.

The PD shall turn on at a voltage less than or equal to V_{On}. After the PD turns on, the PD shall stay on over the entire V_{Port_PD} range. The PD shall turn off at a voltage less than V_{Port_PD} minimum and greater than or equal to V_{Off}.

The PD shall turn on or off without startup oscillation and within the first trial at any load value when fed by V_{Port_PSE} min to V_{Port_PSE} max (as defined in Table 33–11) with a series resistance within the range of valid Channel Resistance.

33.3.7.2 Input average power

The maximum average power, P_{Class_PD} in Table 33–18 or PDMaxPowerValue in 33.6.3.3, is calculated over a 1 second interval. PDs may dynamically adjust their maximum required operating power below P_{Class_PD} as described in 33.6.

NOTE—Average power is calculated using any sliding window with a width of 1 s.

33.3.7.2.1 System stability test conditions during startup and steady state operation

When the PD is fed by V_{Port_PSE} min to V_{Port_PSE} max with R_{Ch} (as defined in Table 33–1) in series, P_{Port_PD} shall be defined as shown in Equation (33–10):

$$P_{Port\_PD} = \{V_{Port\_PD} \times I_{Port}\}_W \quad (33–10)$$

where

P_{Port_PD} is the average input power at the PD PI

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V_{Port_PD} is the static input voltage at the PD PI
I_{Port} is the input current, either DC or RMS

NOTE—When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input. See Annex 33A for PD design guidelines for stable operation.

33.3.7.3 Input inrush current

The PD inrush time duration is defined as beginning with the application of input voltage at the PI when V_{PD} crosses the PD power supply turn on voltage, V_{On} as defined in Table 33–18, and ends after T_{delay}.

The inrush current is the initial current drawn by the PD, which is used to charge C_{Port}. A PD may limit the inrush current below I_{Inrush_PD} to allow for large values of C_{Port}.

The PSE either uses the legacy power up method, whereby it limits the inrush current to I_{Inrush} until the PD input voltage reaches 99% of steady state, or it limits the inrush current for a fixed amount of time, T_{Inrush}, as defined in Table 33–11. See legacy_powerup in 33.2.4.4.

PDs shall draw less than I_{Inrush_PD} from T_{Inrush} min until T_{delay}, when connected to a source that meets the requirements of 33.2.7.5. This delay is required so that the PD does not enter a high power state before the PSE has had time to change the available current from the POWER_UP to the POWER_ON limits. A PD can meet this requirement by either having C_{Port} charged within T_{Inrush} min or by limiting the input inrush current.

PDs with pse_power_type set to 1 shall conform to P_{Class_PD} and P_{Peak_PD} requirements within T_{Inrush} min as defined in Table 33–11. PDs with pse_power_type set to 2 shall not exceed Class 3 P_{Peak_PD}, as defined in Table 33–18, from T_{Inrush} min until T_{delay}.

33.3.7.4 Peak operating power

$V_{Overload}$ is the PD PI voltage when the PD is drawing the permissible P_{Peak_PD}.

At any static voltage at the PI, and any PD operating condition, the peak power shall not exceed P_{Class_PD} max for more than T_{CUT} min, as defined in Table 33–11 and 5% duty cycle. Peak operating power shall not exceed P_{Peak_PD} max.

Ripple current content (I_{Port_ac}) superimposed on the DC current level (I_{Port_dc}) is allowed if the total input power is less than or equal to P_{Class_PD} max.

The RMS, DC and ripple current shall be bounded by Equation (33–11):

$$I_{Port} = \left\{ \sqrt{(I_{Port\_dc})^2 + (I_{Port\_ac})^2} \right\}_A \quad (33–11)$$

where
I_{Port} is the RMS input current
I_{Port_dc} is the DC component of the input current
I_{Port_ac} is the RMS value of the AC component of the input current

The maximum I_{Port} value for all operating V_{Port_PD} range shall be defined by the following equation:

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$$I_{\text{portmax}} = \left\{ \frac{P_{\text{Class\_PD}}}{V_{\text{Port\_PD}}} \right\}_{\text{A}} \quad (33\text{–}12)$$

where

I_{portmax}	is the maximum DC and RMS input current
$V_{\text{Port\_PD}}$	is the static input voltage at the PD PI
$P_{\text{Class\_PD}}$	is the maximum power, $P_{\text{Class\_PD}}$ max, as defined in Table 33–18

Peak power, $P_{\text{Peak\_PD}}$, for Class 4 is based on Equation (33–13), which approximates the ratiometric peak powers of Class 0 through Class 3. This equation may be used to calculate peak operating power for $P_{\text{Peak\_PD}}$ values obtained via Data Link Layer classification.

$$P_{\text{Peak\_PD}} = \{1.11 \times P_{\text{Class\_PD}}\}_{\text{W}} \quad (33\text{–}13)$$

where

$P_{\text{Peak\_PD}}$	is the peak operating power
$P_{\text{Class\_PD}}$	is the input average power

NOTE—The duty cycle of the peak current is calculated using any sliding window with a width of 1 s.

33.3.7.5 Peak transient current

When the input voltage at the PI is static and in the range of $V_{\text{Port\_PD}}$ defined by Table 33–18, the transient current drawn by the PD shall not exceed 4.70 mA/µs in either polarity. This limitation applies after inrush has completed (33.3.7.3) and before the PD has disconnected.

Under normal operating conditions when there are no transients applied at the PD PI, the PD shall operate below the PD upperbound template defined in Figure 33–18.

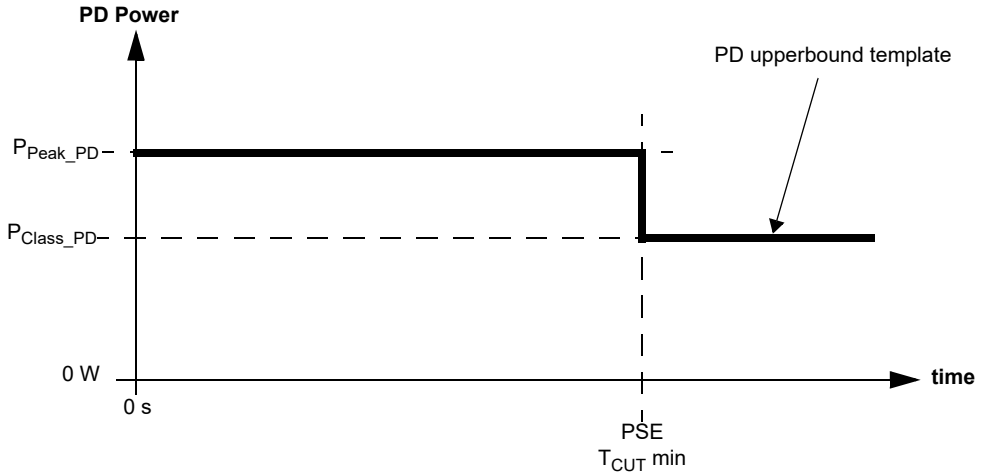

Figure 33–18—PD static operating mask

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The PD upperbound template in Figure 33–18, P_{PDUT}, is described by Equation (33–14):

$$P_{PDUT}(t) = \left\{ \begin{array}{ll} P_{Peak\_PD} & \text{for } (0 \le t < T_{cutmin}) \\ P_{Class\_PD} & \text{for } (T_{cutmin} \le t) \end{array} \right\}_{W} \quad (33–14)$$

where

t	is the duration in seconds that the PD sinks I_{Port}
P_{Peak_PD}	is the peak operating power, P_{Peak_PD} max, as defined in Table 33–18
P_{Class_PD}	is the maximum power, P_{Class_PD} max, as defined in Table 33–18
T_{cutmin}	is T_{CUT} min, as defined in Table 33–11

During PSE transient conditions in which the voltage at the PI is undergoing dynamic change, the PSE is responsible for limiting the transient current drawn by the PD for at least T_{LIM} min as defined in Table 33–11.

33.3.7.6 PD behavior during transients at the PSE PI

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. A Type 2 PD with peak power draw that does not exceed P_{Class_PD} max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

— A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–18) after T_{LIM} min (see Table 33–11 for a Type 1 PSE) when the following input voltage is applied. A current limited voltage source is applied to the PI through a R_{Ch} resistance (see Table 33–1). The current limit meets Equation (33–15) and the voltage ramps from V_{Port_PSE} min to V_{Port_PSE} max at 2250 V/s.

A Type 2 PD shall meet both of the following:

a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/µs, a source impedance of 1.5 Ω, and a source that supports a current greater than 2.5 A.
b) The PD shall not exceed the PD upperbound template beyond T_{LIM} min under worst-case current draw under the following conditions. The input voltage source drives V_{PD} from V_{Port_PSE} min to 56 V at 2250 V/s, the source impedance is R_{Ch} (see Table 33–1), and the voltage source limits the current to MDI I_{LIM} per Equation (33–15).

The current limit at the MDI (MDI I_{LIM}) is defined by Equation (33–15):

$$\{pse_{ILIMmin}\}_{mA} < \{mdi_{ILIM}\}_{mA} \le \{pse_{ILIMmin}\}_{mA} + 5.00 \quad (33–15)$$

where

$pse_{ILIMmin}$	is the PSE I_{LIM} min as defined in Table 33–11
mdi_{ILIM}	is the current limit at the MDI (MDI I_{LIM})

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33.3.7.7 Ripple and noise

The specification for ripple and noise in Table 33–18 shall be for the common-mode and/or differential pair-to-pair noise at the PD PI generated by the PD circuitry. The ripple and noise specification shall be for all operating voltages in the range of V_{Port_PD}, and over the range of input power of the device.

The PD shall operate correctly in the presence of ripple and noise generated by the PSE that appears at the PD PI. These levels are specified in Table 33–11, item 3.

Limits are provided to preserve data integrity. To meet EMI standards, lower values may be needed.

The system designer is advised to assume the worst-case condition in which both PSE and PD generate the maximum noise allowed by Table 33–11 and Table 33–18, which may cause a higher noise level to appear at the PI than the standalone case as specified by this clause.

33.3.7.8 PD classification stability time

Following a valid detection and a rising voltage transition from V_{valid} to V_{Class}, the PD Physical Layer classification signature shall be valid within T_{class} as specified in Table 33–18 and remain valid for the duration of the classification period.

33.3.7.9 Backfeed voltage

When any voltage in the range of 0 V to V_{Port_PD} max is applied across the PI at either polarity specified on the conductors for Mode A according to Table 33–13, the voltage measured across the PI for Mode B with a 100 kΩ load resistor connected across Mode B shall not exceed V_{bfd} max as specified in Table 33–18.

When any voltage in the range of 0 V to V_{Port_PD} max is applied across the PI at either polarity specified on the conductors for Mode B according to Table 33–13, the voltage measured across the PI for Mode A with a 100 kΩ load resistor connected across Mode A shall not exceed V_{bfd} max as specified in Table 33–18.

33.3.8 PD Maintain Power Signature

In order to maintain power, the PD shall provide a valid Maintain Power Signature (MPS) at the PI. The MPS shall be both:

a) Current draw equal to or above the minimum input current (I_{Port_MPS} min) as specified in Table 33–19 for a minimum duration of 75 ms followed by an optional MPS dropout for no longer than 250 ms, and
b) Input impedance with resistive and capacitive components as defined in Table 33–19.

A PD that does not maintain the MPS components in a) and b) above may have its power removed within the limits of T_{MPDO} as specified in Table 33–11.

Powered PDs that no longer require power shall remove both components a) and b) of the MPS. To cause PSE power removal, the impedance of the PI should rise above Z_{ac2} as specified in Table 33–12.

NOTE—A PD with $C_{port} > 180$ µF may not be able to meet the I_{Port_MPS} specification in Table 33–19 during the maximum allowed port voltage droop (V_{Port_PSE} max to V_{Port_PSE} min with series resistance R_{Ch}). Such a PD should increase its I_{Port} min or make other such provisions to meet the Maintain Power Signature.

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Table 33–19—PD Maintain Power Signature

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Input current	I_{Port_MPS}	A	0.010		See 33.3.8
2	Input resistance	R_{pd_d}	kΩ		26.3	
3	Input capacitance	C_{pd_d}	μF	0.050		See Table 33–12

33.4 Additional electrical specifications

This clause defines additional electrical specifications for both the PSE and PD. The specifications apply for all PSE and PD operating conditions at the cabling side of the mated connection of the PI. The requirements apply during data transmission only when specified as an operating condition.

The requirements of 33.4 are consistent with the requirements of the 10BASE-T MAU and the 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T PHYs.

33.4.1 Electrical isolation

PDs and PSEs shall provide isolation between all accessible external conductors, including frame ground (if any), and all MDI leads including those not used by the PD or PSE. Any equipment that can be connected to a PSE or PD through a non-MDI connector that is not isolated from the MDI leads needs to provide isolation between all accessible external conductors, including frame ground (if any), and the non-MDI connector.

This electrical isolation shall meet the isolation requirements as specified in J.1 with electrical strength test c) details being replaced by: “An impulse test consisting of a 1500 V, 10/700 waveform, applied 10 times, with a 60 s interval between pulses. The shape of the impulses is 10/700 (10 μs virtual front time, 700 μs virtual time to half value), as defined in ITU-T Recommendation K.44.”

Conductive link segments that have differing isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of network interface devices (NID).

33.4.1.1 Electrical isolation environments

There are two electrical power distribution environments to be considered that require different electrical isolation properties. They are as follows:

— **Environment A:** When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.
— **Environment B:** When a LAN crosses the boundary between separate power distribution systems or the boundaries of a single building.

33.4.1.1.1 Environment A requirements

Attachment of network segments via NIDs that have multiple instances of a twisted pair MDI requires electrical isolation between each segment and the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or PHY (see 14.3.1.1, 25.4.6, and 40.6.1.1.). Equipment with multiple instances of PSE, PD, or both shall meet or exceed the isolation requirement of the MAU/PHY with which they are associated.

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A multiport NID complying with Environment A requirements does not require electrical power isolation between link segments.

An Environment A PSE shall switch the more negative conductor. It is allowable to switch both conductors.

33.4.1.1.2 Environment B requirements

The attachment of network segments that cross Environment A boundaries requires electrical isolation between each segment and all other attached segments as well as to the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or PHY (see 14.3.1.1, 25.4.6, and 40.6.1.1.). Equipment with multiple instances of PSE, PD, or both shall meet or exceed the isolation requirement of the MAU/PHY with which each is associated.

The requirements for interconnected electrically conducting link segments that are partially or fully external to a single building environment may require additional protection against lightning strikes or other hazards. Protection requirements for such hazards are beyond the scope of this standard. Guidance on these requirements may be found in Section 6 of IEC 60950-1:2001, as well as any local and national codes related to safety.

33.4.2 Fault tolerance

Each wire pair of the PI, when it is also an MDI (e.g., an Endpoint PSE or PD), shall meet the fault tolerance requirements of the appropriate specifying clause. (See 14.3.1.2.7, 25.4, 40.8.3.4, 55.8.2.3, and 126.8.2.4.) When a PI is not an MDI (e.g., a Midspan PSE), the PSE PI shall meet the fault tolerance requirements of this subclause.

The PSE PI shall withstand without damage the application of short circuits of any wire to any other wire within the cable for an indefinite period of time. The magnitude of the current through such a short circuit shall not exceed I_{LIM} max as defined in Table 33–11.

Each wire pair shall withstand, without damage, a 1000 V common-mode impulse applied at E_{cm} of either polarity. The shape of the impulse shall be (0.3/50) μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060, where E_{cm} is an externally applied AC voltage as shown in Figure 33–19.

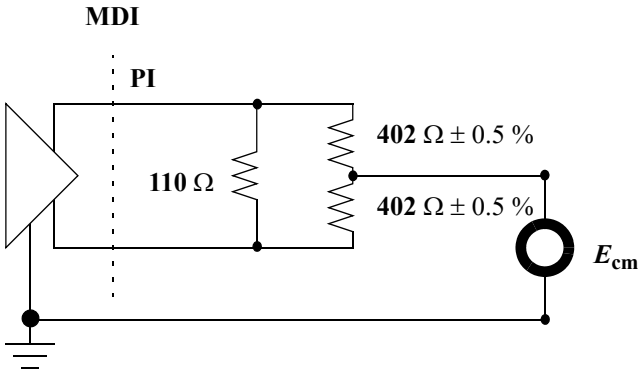

Figure 33–19—PI fault tolerance test circuit

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33.4.3 Impedance balance

Impedance balance is a measurement of the common-mode-to-differential-mode offset of the PI. The common-mode-to-differential-mode impedance balance for the transmit and receive pairs shall exceed the limits in Table 33–20 for all supported PHY speeds.

Table 33–20—Impedance balance limits for supported speeds

Supported speed	Impedance balance limit (dB)	Frequency range
10 Mb/s MAU	$29 - 17 \times \log_{10}(f/10)$	$1 \le f \le 20$ MHz
100 Mb/s or 1000 Mb/s PHY	$34 - 19.2 \times \log_{10}(f/50)$	$1 \le f \le 100$ MHz
2.5 Gb/s PHY	48	$1 \le f < 10$ MHz
	$48 - 20 \times \log_{10}(f/10)$	$10 \le f < 20$ MHz
	$42 - 15 \times \log_{10}(f/20)$	$20 \le f \le 125$ MHz
5 Gb/s PHY	48	$1 \le f < 30$ MHz
	$44 - 19.2 \times \log_{10}(f/50)$	$30 \le f \le 250$ MHz
10 Gb/s PHY	48	$1 \le f < 30$ MHz
	$44 - 19.2 \times \log_{10}(f/50)$	$30 \le f \le 500$ MHz

The impedance balance is defined as shown in Equation (33–16):

$$\left\{20.0 \times \log_{10}\left(\frac{E_{\text{cm}}}{E_{\text{dif}}}\right)\right\}_{\text{dB}} \tag{33–16}$$

where

E_{cm} is an externally applied sinusoidal voltage as shown in Figure 33–20

E_{dif} is the voltage of the resulting waveform due only to the applied sine wave measured as shown in Figure 33–20

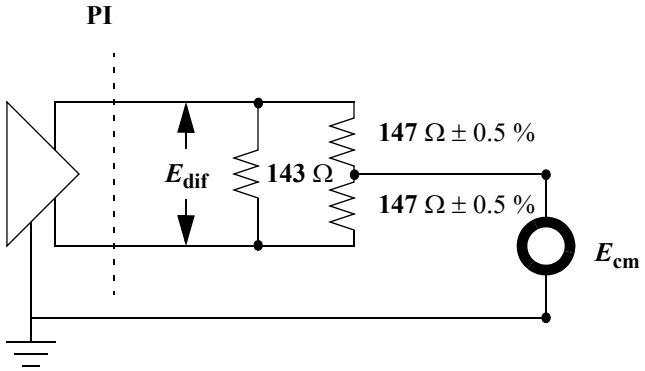

Figure 33–20—PI impedance balance test circuit

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33.4.4 Common-mode output voltage

The magnitude of the common-mode AC output voltage measured according to Figure 33–21 and Figure 33–22 at the transmit PI while transmitting data and with power applied, E_{cm_out}, shall not exceed the values in Table 33–21 while operating at the specified speed, when measured over the specified bandwidth.

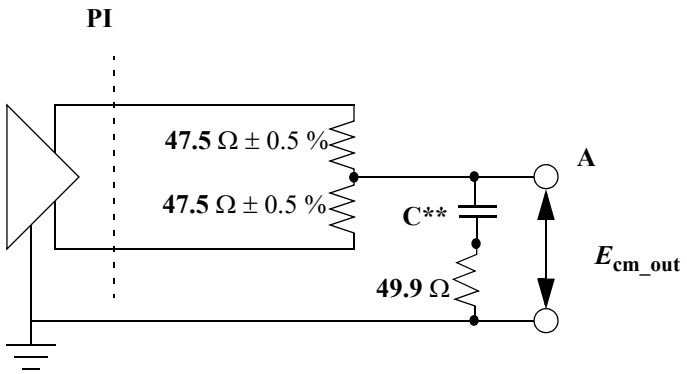

Figure 33–21—Common-mode output voltage test

The common-mode AC output voltage shall be measured while the PHY is transmitting data, the PSE or PD is operating with the following PSE load or PD source:

1) For a PSE, the PI that supplies power is terminated as illustrated in Figure 33–22. The PSE load, R, in Figure 33–22 is adjusted so that the PSE output current, I_{out}, is 10 mA and then 350 mA, while measuring E_{cm_out} on the PI.
2) For a PD, the PI that requires power shall be terminated as illustrated in Figure 33–22. V_{source} in Figure 33–22 is adjusted to 36 Vdc and 57 Vdc, while measuring E_{cm_out} on the PI.

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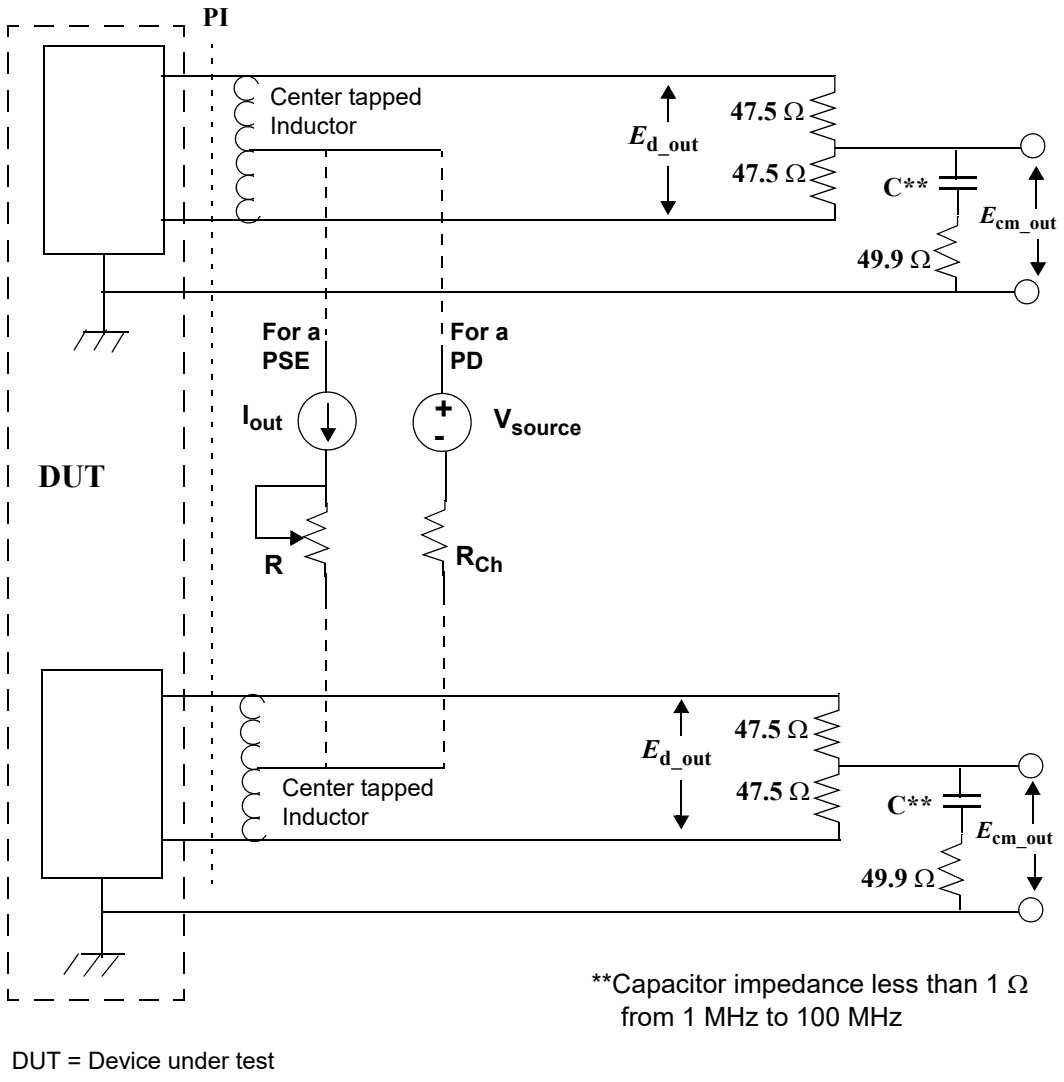

Figure 33–22—PSE and PD terminations for common-mode output voltage test

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Table 33–21—Common-mode output voltage for given operating speed

Operating speed	Common-mode output voltage (E_{cm_out})	Measurement bandwidth
10 Mb/s MAU	50 mV peak	$1 \leq f \leq 100$ MHz
100 Mb/s or 1000 Mb/s PHY	50 mV_{pp}	$1 \leq f \leq 100$ MHz
2.5 Gb/s PHY	50 mV_{pp}	$1 \leq f \leq 100$ MHz
5 Gb/s PHY	50 mV_{pp}	$1 \leq f \leq 250$ MHz
10 Gb/s PHY	50 mV_{pp}	$1 \leq f \leq 500$ MHz

NOTE—The implementer should consider any applicable local, national, or international regulations that may require more stringent specifications. One such specification can be found in the European Standard EN 55022:1998.

33.4.5 Pair-to-pair output noise voltage

The pair-to-pair output noise voltage (see Figure 33–23) is limited by the resulting electromagnetic interference due to this AC voltage. This AC voltage can be ripple from the power supply (Table 33–11, item 3) or from any other source. A system integrating a PSE shall comply with applicable local and national codes for the limitation of electromagnetic interference.

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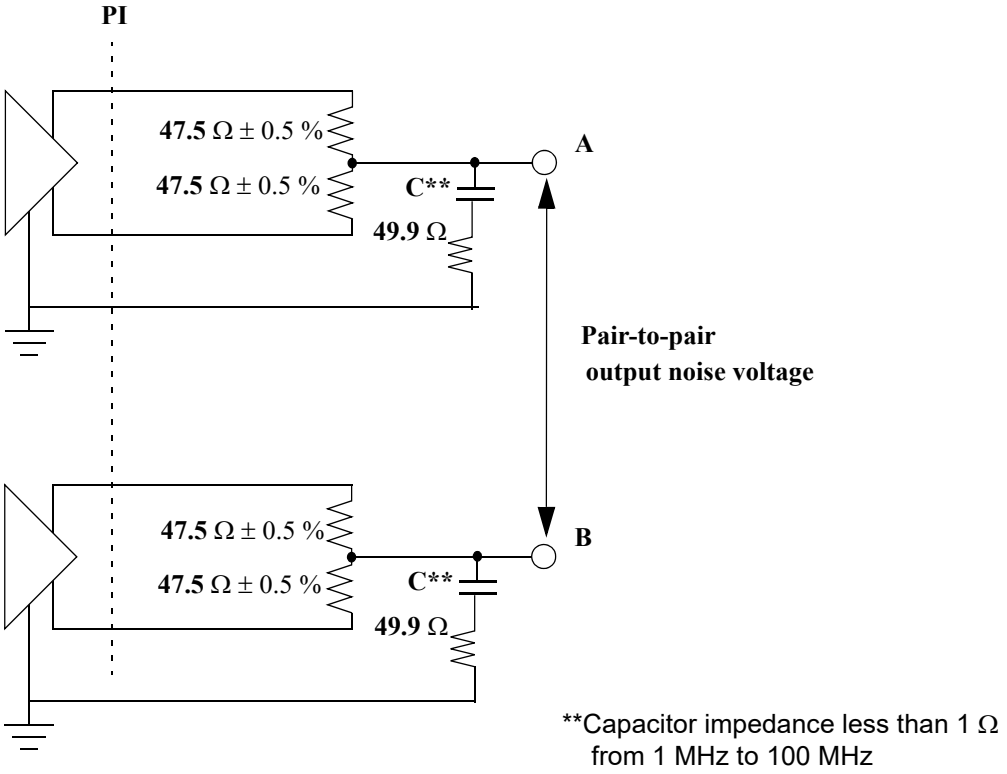

Figure 33–23—Pair-to-pair output noise voltage test

33.4.6 Differential noise voltage

For 10/100/1000 Mb/s, the coupled noise, E_{d_out} in Figure 33–22, from a PSE or PD to the differential transmit and receive pairs shall not exceed 10 mV peak-to-peak when measured from 1 MHz to 100 MHz under the conditions specified in 33.4.4, item 1) and item 2).

For 2.5GBASE-T, 5GBASE-T, or 10GBASE-T, the coupled noise, E_{d_out} in Figure 33–22, from a PSE or PD to the differential transmit and receive pairs shall not exceed 10 mV peak-to-peak when measured in the band from 1 MHz to 10 MHz and shall not exceed 1 mV peak-to-peak when measured in the band from 10 MHz to 100 MHz for 2.5GBASE-T, 10 MHz to 250 MHz for 5GBASE-T, and 10 MHz to 500 MHz for 10GBASE-T under the conditions specified in 33.4.4, item 1) and item 2).

33.4.7 Return loss

The differential impedance of the transmit and receive pairs at the PHY's MDI shall be such that any reflection shall meet the return loss requirements as specified in 14.3.1.3.4 for a 10 Mb/s PHY, in ANSI INCITS 263-1995 for a 100 Mb/s PHY, in 40.8.3.1 for a 1000 Mb/s PHY, in 126.8.2.2 for a 2.5 Gb/s or 5 Gb/s PHY, and in 55.8.2.1 for a 10 Gb/s PHY. In addition, all pairs terminated at an MDI should maintain a nominal common-mode impedance of 75 Ω. The common-mode termination is affected by the presence of the power supply, and this should be considered to determine proper termination.

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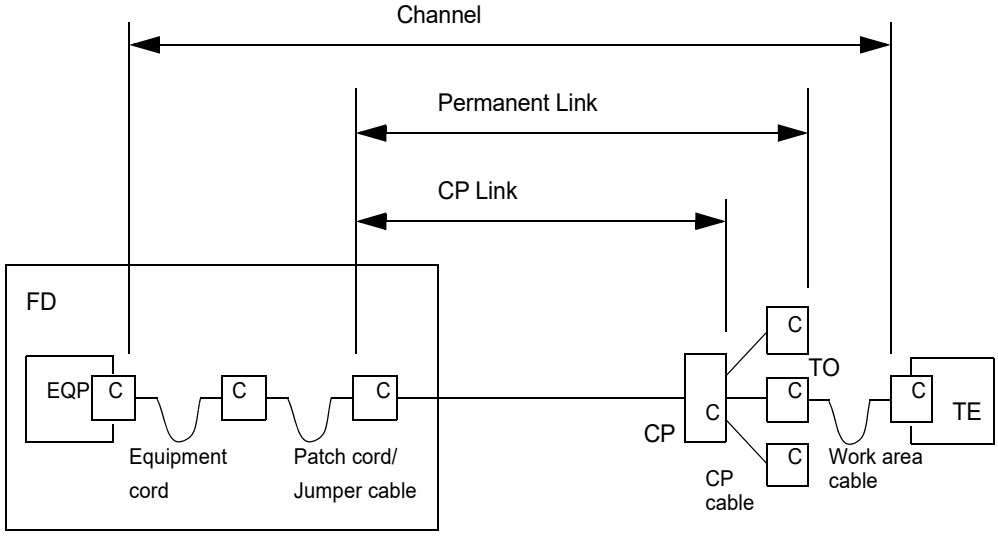
33.4.8 100BASE-TX transformer droop

100BASE-TX systems may contain a legacy PHY receiver that expects to be connected to a PHY transmitter with 350 μH open circuit inductance (OCL). Alternative A Type 2 Midspan PSEs that support 100BASE-TX shall enforce channel unbalance currents less than or equal to Type 1 I_{unb} (see Table 33–11) or meet 33.4.9.4.

100BASE-TX Type 2 Endpoint PSEs and 100BASE-TX Type 2 PDs shall meet the requirements of Clause 25 in the presence of (I_{unb}/2).

33.4.9 Midspan PSE device additional requirements

The cabling specifications for 100 Ω balanced cabling are described in ISO/IEC 11801-2002. Cable conforming to ANSI/TIA-568-C.2 also meets these requirements. Some cable category specifications that only appear in earlier editions are also supported. The configuration of "channel" and "permanent link" is defined in Figure 33–24. Type 2 Midspan PSE cabling system requirements are specified in 33.1.4.1.



FD = floor distributor; EQP = equipment; C = connection (mated pair);
CP = consolidation point; TO = telecommunications outlet;
TE = terminal equipment

Figure 33–24—Floor distributor channel configuration

ISO/IEC 11801 defines in 5.6.1 two types of Equipment interface to the cabling system: "Interconnect model" and the "cross-connect model." An equivalent "Interconnect model" and "cross-connect model" can be found in ANSI/TIA-568-C.0, 4.2. See Figure 33–25.

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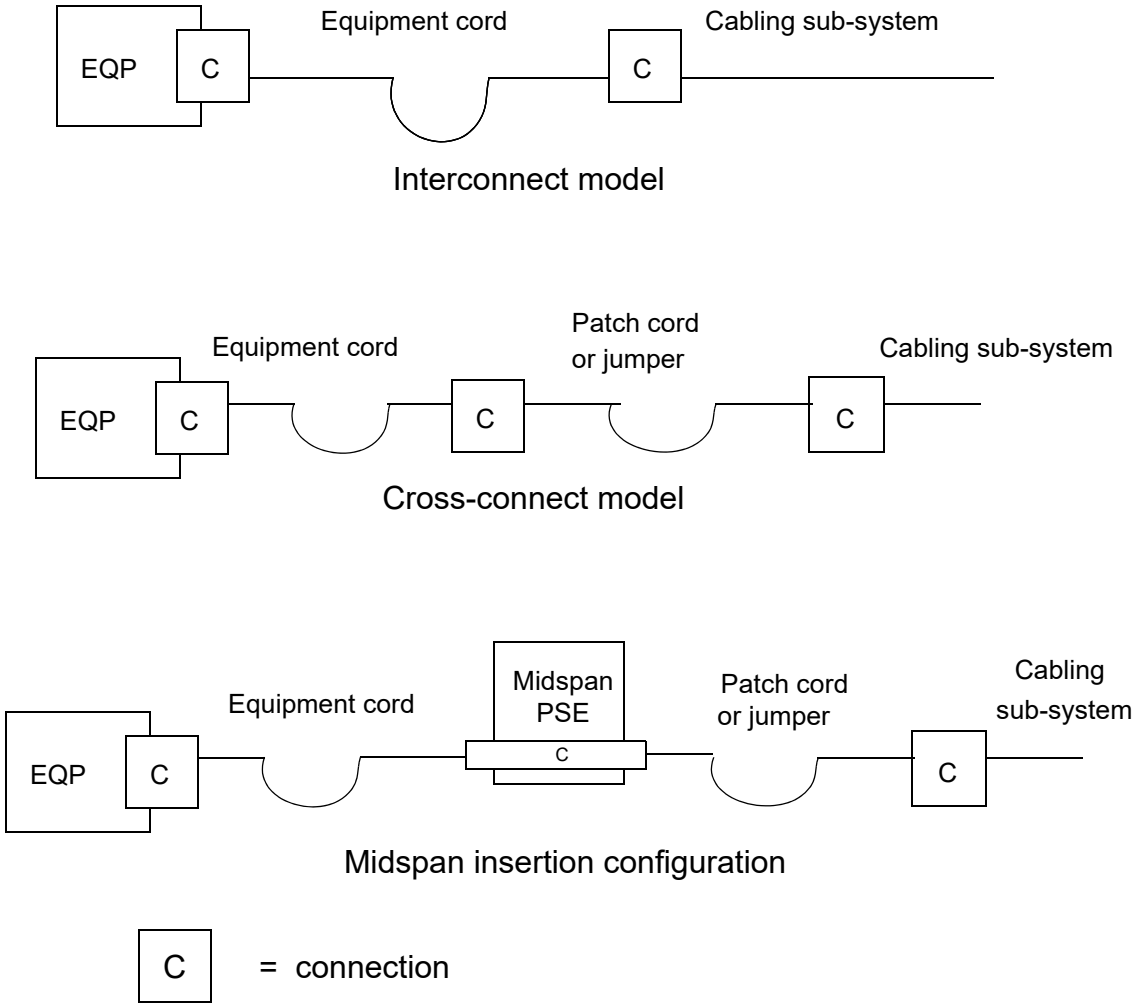

Figure 33–25—Interconnect model, cross-connect model, and midspan insertion configuration

The insertion of a Midspan PSE at the Floor Distributor (FD) shall comply with the following guidelines:

a) If the existing FD configuration is of the “Interconnect model” type, the Midspan PSE can be added, provided it does not increase the insertion loss of the resulting “channel” to more than that specified for the same Class or category 100 m channel defined in ISO/IEC 11801 or ANSI/TIA-568-C.0.

b) If the existing FD configuration is of the “Cross-connect model” type, the Midspan PSE can be installed instead of one of the connection pairs in the FD. In addition, the installation of the Midspan PSE shall not increase the insertion loss of the resulting “channel” to more than that specified for the same Class or category 100 m channel defined in ISO/IEC 11801 or ANSI/TIA-568-C.0.

c) For a 10GBASE-T midspan PSE, in meeting either of the above requirements, the Midspan PSE may be substituted for up to two connection pairs in the FD.

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Configurations with the Midspan PSE in the cabling channel shall not alter the transmission requirements of the "permanent link." A Midspan PSE shall not provide DC continuity between the two sides of the segment for the pairs that inject power.

The requirements for the two pair Category 5 channel are found in 25.4.9. The specification of Midspan PSE operation on a two pair cable is beyond the scope of this document.

NOTE—Appropriate terminations may be applied to the interrupted pairs on both sides of the Midspan device.

33.4.9.1 Connector Midspan PSE device transmission requirements

The Midspan PSE to be inserted as a connection or telecommunications outlet shall meet the following transmission parameters. These parameters should be measured using the test procedures of ISO 11801:2002 or ANSI/TIA-568-C.2 for connecting hardware.

There are five variants of Midspan PSEs defined with respect to transmission requirements:

1) 10BASE-T/100BASE-TX connector Midspan PSE
2) 1000BASE-T connector Midspan PSE
3) 2.5GBASE-T connector Midspan PSE
4) 5GBASE-T connector Midspan PSE
5) 10GBASE-T connector Midspan PSE

33.4.9.1.1 Near End Crosstalk (NEXT)

NEXT loss is a measure of the unwanted signal coupling from a transmitter at the near-end into neighboring pairs measured at the near-end. NEXT loss is expressed in dB relative to the received signal level. For operation with 1000BASE-T and lower rates, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–17) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. For operation with 5GBASE-T and lower rates, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB.

$$\{NEXTconn\}_{\mathrm{dB}} \geq 40.0 - 20.0 \times \log_{10}\left(\frac{f}{100}\right) \tag{33–17}$$

where

NEXTconn is the Near End Crosstalk loss
f is the frequency expressed in MHz

For 2.5GBASE-T, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–18) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. For 5GBASE-T, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–18) when measured for the transmit and receive pairs from 1 MHz to 250 MHz. For operation with 2.5GBASE-T and 5GBASE-T, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB.

$$\{NEXTconn\}_{\mathrm{dB}} \geq 43 - 20 \times \log_{10}\left(\frac{f}{100}\right) \tag{33–18}$$

where

NEXTconn is the Near End Crosstalk loss
f is the frequency expressed in MHz

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For 10GBASE-T operation, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–19) when measured for the transmit and receive pairs from 1 MHz to 500 MHz. However, for frequencies that correspond to calculated values greater than 75 dB, the requirement reverts to the minimum requirement of 75 dB.

$$\{NEXTconn\}_{\text{dB}} \leq \left\{ \begin{array}{ll} 54 - 20 \times \log_{10}\left(\frac{f}{100}\right) & \text{for } (1 \leq f \leq 250) \\ 46.04 - 40 \times \log_{10}\left(\frac{f}{250}\right) & \text{for } (250 < f \leq 500) \end{array} \right\}_{dB} \quad (33\text{–}19)$$

where

NEXTconn is the Near End Crosstalk loss in dB
f is the frequency expressed in MHz

33.4.9.1.2 Insertion loss

Insertion loss is a measure of the signal loss between the transmitter and receiver, expressed in dB relative to the received signal level. For other than 5GBASE-T or 10GBASE-T operation, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33–20) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. For 5GBASE-T capable midspans, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33–20) when measured for the transmit and receive pairs from 1 MHz to 250 MHz. For frequencies that correspond to calculated values less than 0.1 dB, the requirement reverts to the maximum requirement of 0.1 dB. For 10GBASE-T operation, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33–20) when measured from the transmit and receive pairs from 1 MHz to 500 MHz.

$$\{ILconn\}_{\text{dB}} \leq 0.040 \times \sqrt{f} \quad (33\text{–}20)$$

where

ILconn is the insertion loss
f is the frequency expressed in MHz

33.4.9.1.3 Return loss

Return loss is a measure of the reflected energy caused by impedance mismatches in the cabling system and is expressed in dB relative to the reflected signal level. Return loss for Midspan PSE devices shall meet or exceed the values specified in Table 33–22.

Table 33–22—Connector return loss

Midspan PSE variant	Frequency	Return loss
10/100/1000BASE-T	1 MHz ≤ *f* < 20 MHz	23 dB
	20 MHz ≤ *f* ≤ 100 MHz	14 dB
2.5GBASE-T	1 MHz ≤ *f* < 31.5 MHz	30 dB
	31.5 MHz ≤ *f* < 100 MHz	20 – 20 $\log_{10}$(f / 100)

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Table 33–22—Connector return loss *(continued)*

Midspan PSE variant	Frequency	Return loss
5GBASE-T	1 MHz ≤ f < 31.5 MHz	30 dB
	31.5 MHz ≤ f ≤ 250 MHz	20 – 20 $\log_{10}$(f / 100)
10GBASE-T	1 MHz ≤ f < 79 MHz	30 dB
	79 MHz ≤ f ≤ 500 MHz	28 – 20 $\log_{10}$(f / 100)

33.4.9.2 Cord Midspan PSE

Replacing the work area or equipment cable with a cable that includes a Midspan PSE should not alter the requirements of the cable. This cable shall meet the requirements of this clause and the specifications for a (jumper) cord for insertion loss, NEXT, and return loss for the transmit and receive pairs, as shown in Table 33–23.

There are five variants of Midspan PSEs defined with respect to transmission requirements:

1) 10BASE-T/100BASE-TX cord Midspan PSE
2) 1000BASE-T cord Midspan PSE
3) 2.5GBASE-T cord Midspan PSE
4) 5GBASE-T cord Midspan PSE
5) 10GBASE-T cord Midspan PSE

Table 33–23—Cord specifications for use with Midspan PSEs

Highest PHY rate supported	Cord specification	Frequency range
Up to 1000BASE-T	Category 5 cord in ISO/IEC 11801:2002 or ANSI/TIA-568-A:1995	1 MHz ≤ f ≤ 100 MHz
Up to 2.5GBASE-T	Category 5e cord in ISO/IEC 11801:2002 or ANSI/TIA-568-C.2	1 MHz ≤ f ≤ 100 MHz
Up to 5GBASE-T	Category 6 cord in ISO/IEC 11801:2002 or ANSI/TIA-568-C.2	1 MHz ≤ f ≤ 250 MHz
Up to 10GBASE-T	Category 6A cord in ISO/IEC 11801-1 or ANSI/TIA-568-C.2	1 MHz ≤ f ≤ 500 MHz

33.4.9.2.1 Maximum link delay

The propagation delay contribution of the Midspan PSE device shall not exceed 2.5 ns from 1 MHz to the highest referenced frequency.

33.4.9.2.2 Maximum link delay skew

The propagation delay skew of the Midspan PSE device shall not exceed 1.25 ns from 1 MHz to the highest referenced frequency.

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33.4.9.3 Coupling parameters between link segments

Midspan PSEs intended for operation with 2.5G/5G/10GBASE-T (variants 3 through 5 in 33.4.9.1 and 33.4.9.2) are additionally required to meet the following parameters for coupling signals between ports relating to different link segments. Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. To bound the total alien NEXT loss and alien FEXT loss coupled between link segments, multiple disturber alien near-end crosstalk (MDANEXT) loss and multiple disturber alien FEXT (MDAFEXT) loss are specified.

33.4.9.3.1 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

PSANEXT loss for 2.5G/5G/10GBASE-T capable Midspan PSE devices shall meet or exceed the values determined using Equation (33–21). For other than 5GBASE-T or 10GBASE-T operation, PSANEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–21) from 1 MHz to 100 MHz. For 5GBASE-T capable midspans, PSANEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–21) from 1 MHz to 250 MHz. For 10GBASE-T capable midspans, PSANEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–21) from 1 MHz to 500 MHz. When the computed PSANEXT value at a certain frequency exceeds 67 dB, the PSANEXT result at that frequency is for information only.

$$\text{PSANEXT Loss} = 70.5 - 20\log_{10}(f/100) \tag{33–21}$$

33.4.9.3.2 Multiple disturber power sum alien far-end crosstalk (PSAFEXT) loss

PSAFEXT loss for 2.5G/5G/10GBASE-T capable Midspan PSE devices shall meet or exceed the values determined using Equation (33–22). For other than 5GBASE-T or 10GBASE-T operation, PSAFEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–22) from 1 MHz to 100 MHz. For 5GBASE-T capable midspans, PSAFEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–22) from 1 MHz to 250 MHz. For 10GBASE-T capable midspans, PSAFEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–22) from 1 MHz to 500 MHz. When the computed PSAFEXT value at a certain frequency exceeds 67 dB, the PSANEXT result at that frequency is for information only.

$$\text{PSAFEXT Loss} = 67 - 20\log_{10}(f/100) \tag{33–22}$$

33.4.9.4 Midspan signal path requirements

An Alternative A Midspan PSE transfer function gain shall be greater than that expressed by Equation (33–23) for the frequency range from 0.1 MHz to 1 MHz, at the pins of the PI used as 100BASE-TX transmit pins.

$$\left\{ -0.100 + 37.5 \times \log_{10}\left(\frac{22.4 \times f}{\sqrt{1.00 + 521 \times f^2}} \right) \right\} \text{dB} \tag{33–23}$$

where

f is the frequency expressed in MHz.

The requirements shall be met with a DC bias current, I_{bias}, between 0 mA and (I_{unb}/2) mA (I_{unb} is defined in Table 33–11).

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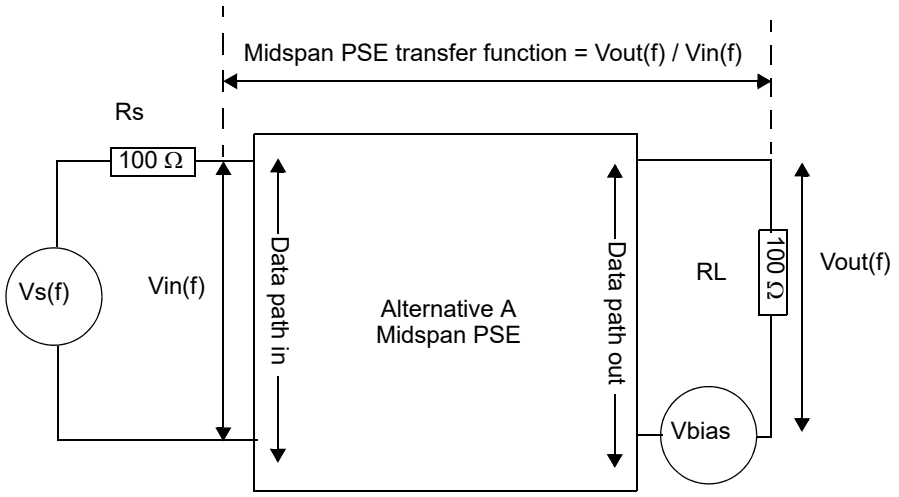
33.4.9.4.1 Alternative A Midspan PSE signal path transfer function

The transfer function is measured by applying a test signal to the Midspan PSE signal input through a source impedance of 100 Ω ± 1 %. The Midspan PSE signal input and output may be connected to a 0.5 m maximum length of cable, meeting the requirements of 25.4.9, terminated with 100 Ω ± 1 %.

The transfer function is defined from the output termination to the Midspan PSE input. See Figure 33–26.



Vin(f) is the sine wave signal to be used to measure the Midspan PSE transfer function.
Vbias is the DC offset voltage to be applied in series with RL in order to generate I_{bias}.
Vout(f) is the Midspan PSE response to Vin(f).
Some test equipment may require isolation between measurement ports.

Figure 33–26—Measurement setup for Alternative A Midspan PSE transfer function

33.5 Management function requirements

NOTE—33.5 has been deprecated. Since May 2019, maintenance changes are no longer being considered for this subclause.

If the PSE is implemented with a management interface described in 22.2.4 or 45.2 (MDIO), then the management access shall use the PSE register definitions shown in 33.5.1. Where no physical embodiment of the Clause 22 or Clause 45 management is supported, equivalent management capability shall be provided. Managed objects corresponding to PSE and PD control parameters and states are described in Clause 30.

33.5.1 PSE registers

A PSE implementing either Clause 22 or Clause 45 management interface shall use register address 11 for its control and register address 12 for its status functions. The full set of management registers is listed in Table 22–6.

Some of the bits within registers are defined as latching high (LH). When a bit is defined as latching high and the condition for the bit to be high has occurred, the bit shall remain high until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors.

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33.5.1.1 PSE Control register (Register 11) (R/W)

The assignment of bits in the PSE Control register is shown in Table 33–24. The default value for each bit of the PSE Control register should be chosen so that the initial state of the PSE upon power up or reset is a normal operational state without management intervention.

Table 33–24—PSE Control register bit definitions

Bit(s)	Name	Description	R/W[a]
11.15:6	Reserved	Ignore when read	RO
11.5	Data Link Layer Classification Capability	1 = Data Link Layer classification capability enabled 0 = Data Link Layer classification capability disabled	R/W
11.4	Enable Physical Layer Classification	1 = Physical Layer classification enabled 0 = Physical Layer classification disabled	R/W
11.3:2	Pair Control	(11.3) (11.2) 1 1 = Reserved 1 0 = PSE pinout Alternative B 0 1 = PSE pinout Alternative A 0 0 = Reserved	R/W
11.1:0	PSE Enable	(11.1) (11.0) 1 1 = Reserved 1 0 = Force Power Test Mode 0 1 = PSE Enabled 0 0 = PSE Disabled	R/W

[a]R/W = Read/Write, RO = Read Only

33.5.1.1.1 Reserved bits (11.15:6)

Bits 11.15:6 are reserved for future standardization. They shall not be affected by writes and shall return a value of zero when read. For compatibility with future use of reserved bits and registers, if the management entity writes to a reserved bit, it should use a value of zero. If it reads a reserved bit, it should ignore the results.

33.5.1.1.2 Data Link Layer Classification capability (11.5)

Bit 11.5 controls a PSEs capability of performing Data Link Layer classification as specified in 33.6.

A PSE that does not support Data Link Layer classification shall ignore writes to bit 11.5 and shall return a value of zero when read. A PSE that supports Data Link Layer classification, but does not allow the capability to be disabled, shall ignore writes to bit 11.5 and shall return a value of one when read.

A PSE that supports Data Link Layer classification and supports the ability to enable and disable it shall enable Data Link Layer classification by setting bit 11.5 to one and disable it by setting bit 11.5 to zero.

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33.5.1.1.3 Enable Physical Layer classification (11.4)

Bit 11.4 controls Physical Layer classification as specified in 33.2.6. A PSE that indicates support for Physical Layer classification in register 12.13 may also provide the option of disabling Physical Layer classification through bit 11.4.

A PSE that does not support Physical Layer classification shall ignore writes to bit 11.4 and shall return a value of zero when read. A PSE that supports Physical Layer classification, but does not allow the function to be disabled, shall ignore writes to bit 11.4 and shall return a value of one when read.

The Physical Layer classification function shall be enabled by setting bit 11.4 to one and disabled by setting bit 11.4 to zero.

33.5.1.1.4 Pair Control (11.3:2)

Bits 11.3:2 report the supported PSE Pinout Alternative specified in 33.2.1. A PSE may also provide the option of controlling the PSE Pinout Alternative through these bits. Provision of this option is indicated through the Pair Control Ability (12.0) bit. A PSE that does not support this option shall ignore writes to these bits and shall return the value that reports the supported PSE Pinout Alternative.

When read as ‘01’, bits 11.3:2 indicate that only PSE Pinout Alternative A is supported by the PSE. When read as ‘10’, bits 11.3:2 indicate that only PSE Pinout Alternative B is supported by the PSE.

Where the option of controlling the PSE Pinout Alternative through these bits is provided, setting bits 11.3:2 to ‘01’ shall force the PSE to use only PSE Pinout Alternative A and setting bits 11.3:2 to ‘10’ shall force the PSE to use only PSE Pinout Alternative B.

If bit 12.0 is one, writing to these register bits shall set mr_pse_alternative to the corresponding value: ‘01’ = A and ‘10’ = B. The combinations ‘00’ and ‘11’ for bits 11.3:2 are reserved and will never be assigned. Reading bits 11.3:2 returns an unambiguous result of ‘01’ or ‘10’ that may be used to determine the presence of the PSE Control register.

33.5.1.1.5 PSE enable (11.1:0)

The PSE function shall be disabled by setting bit 11.1 to zero and bit 11.0 to zero. When the PSE function is disabled, the MDI shall function as it would if it had no PSE function. The PSE function shall be enabled by setting bits 11.1 to a zero and 11.0 to a one. When bit 11.1 is a one, and bit 11.0 is a zero, a test mode is enabled. This test mode supplies power without regard to PD detection.

Writing to these register bits shall set mr_pse_enable to the corresponding value: ‘00’ = disable, ‘01’ = enable and ‘10’ = force power. The combination ‘11’ for bits 11.1:0 has been reserved for future use.

CAUTION

Test mode may damage connected non-PD, legacy, twisted pair Ethernet devices, or other non-Ethernet devices, especially in split application wiring schemes.

33.5.1.2 PSE Status register (Register 12) (R/W)

The assignment of bits in the PSE Status register is shown in Table 33–25.

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Table 33–25—PSE Status register bit definitions

Bit(s)	Name	Description	R/W[a]
12.15	PSE Type Electrical Parameters	1 = PSE is using Type 2 PSE electrical parameters 0 = PSE is using Type 1 PSE electrical parameters	RO
12.14	Data Link Layer Classification Enabled	1 = Data Link Layer classification is enabled 0 = Data Link Layer classification is not supported or is not enabled	RO
12.13	Physical Layer Classification Supported	1 = PSE supports Physical Layer classification 0 = PSE does not support Physical Layer classification	RO
12.12	Power Denied or Removed	1 = Power has been denied or removed due to fault 0 = Power has not been denied or removed	RO/ LH
12.11	Valid Signature	1 = Valid PD signature detected 0 = No valid PD signature detected	RO/ LH
12.10	Invalid Signature	1 = Invalid PD signature detected 0 = No invalid PD signature detected	RO/ LH
12.9	Short Circuit	1 = Short circuit condition detected 0 = No short circuit condition detected	RO/ LH
12.8	Overload	1 = Overload condition detected 0 = No overload condition detected	RO/ LH
12.7	MPS Absent	1 = MPS absent condition detected 0 = No MPS absent condition detected	RO/ LH
12.6:4	PD Class	(12.6) (12.5) (12.4) 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Invalid Class 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Class 0	RO
12.3:1	PSE Status	(12.3) (12.2) (12.1) 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = implementation-specific fault 1 0 0 = Test error 0 1 1 = Test mode 0 1 0 = Delivering power 0 0 1 = Searching 0 0 0 = Disabled	RO
12.0	Pair Control Ability	1 = PSE pinout controllable by Pair Control bits 0 = PSE Pinout Alternative fixed	RO

[a]RO = Read Only, LH = Latched High

33.5.1.2.1 PSE Type electrical parameters (12.15)

When read as a zero, bit 12.15 indicates that the PSE is operating with Type 1 PSE electrical parameters. When read as a one, bit 12.15 indicates that the PSE is operating with Type 2 PSE electrical parameters. This

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bit shall be set to zero when the PSE state diagram sets the state variable set_parameter_type to 1. This bit shall be set to one when the PSE state diagram sets set_parameter_type to 2.

33.5.1.2.2 Data Link Layer Classification Enabled (12.14)

When read as a one, bit 12.14 indicates the PSE supports Data Link Layer classification as defined in 33.2.6 and that it is enabled. When read as a zero, bit 12.14 indicates that the PSE lacks support for Data Link Layer classification or that Data Link Layer classification is not enabled. If supported, the Data Link Layer classification may be enabled or disabled through the state diagram variable pse_dll_enabled (see 33.2.4.4).

This bit shall be set to one when the PSE state diagram (Figure 33–9) sets true the state variable pse_dll_enabled. This bit shall be set to zero when the PSE state diagram sets false the state variable pss_dll_enabled.

33.5.1.2.3 Physical Layer Classification Supported (12.13)

When read as a one, bit 12.13 indicates that the PSE supports Physical Layer classification as defined in 33.2.6. When read as a zero, bit 12.13 indicates that the PSE lacks support for Physical Layer classification. If supported, the function may be enabled or disabled through the Enable Physical Layer Classification bit (11.4).

33.5.1.2.4 Power Denied or Removed (12.12)

When read as a one, bit 12.12 indicates that power has been denied or has been removed due to a fault condition. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the states ‘POWER_DENIED’ or ‘ERROR_DELAY.’ The Power Denied bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.5 Valid Signature (12.11)

When read as a one, bit 12.11 indicates that a valid signature has been detected. This bit shall be set to one when mr_valid_signature transitions from FALSE to TRUE. The Valid Signature bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.6 Invalid Signature (12.10)

When read as a one, bit 12.10 indicates that an invalid signature has been detected. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the state ‘SIGNATURE_INVALID’. The Invalid Signature bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.7 Short Circuit (12.9)

When read as a one, bit 12.9 indicates that a short circuit condition has been detected. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the state ‘ERROR_DELAY’ due to the short_detected variable being TRUE. The Short Circuit bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.8 Overload (12.8)

When read as a one, bit 12.8 indicates that an overload condition has been detected. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the state ‘ERROR_DELAY’ due to the ovld_detected variable being TRUE. The Overload bit shall be implemented with latching high behavior as defined in 33.5.1.

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33.5.1.2.9 MPS Absent (12.7)

When read as a one, bit 12.7 indicates that an MPS Absent condition has been detected. The MPS Absent bit shall be set to one when the PSE state diagram (Figure 33–9) transitions directly from the state POWER_ON to IDLE due to tmpdo_timer_done being asserted. The MPS Absent bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.10 PD Class (12.6:4)

Bits 12.6:4 report the PD Class of a detected PD as specified in 33.2.5 and 33.2.6. The value in this register is valid while a PD is connected, i.e., while the PSE Status (12.3:1) bits are reporting "delivering power." The combinations '110' and '111' for bits 12.6:4 have been reserved for future use.

33.5.1.2.11 PSE Status (12.3:1)

Bits 12.3:1 report the current status of the PSE. When read as '000', bits 12.3:1 indicate that the PSE state diagram (Figure 33–9) is in the state DISABLED. When read as '010', bits 12.3:1 indicate that the PSE state diagram is in the state POWER_ON. When read as '011', bits 12.3:1 indicate that the PSE state diagram is in the state TEST_MODE. When read as '100', bits 12.3:1 indicate that the PSE state diagram is in the state TEST_ERROR. When read as '101', bits 12.3:1 indicate that the PSE state diagram is in the state IDLE due to the variable error_condition = true. When read as '001', bits 12.3:1 indicate that the PSE state diagram is in a state other than those listed above.

The combinations '111' and '110' for bits 12.3:1 have been reserved for future use.

33.5.1.2.12 Pair Control Ability (12.0)

When read as a one, bit 12.0 indicates that the PSE supports the option to control which PSE Pinout Alternative (see 33.2.1) is used for PD detection and power through the Pair Control (11.3:2) bits. When read as a zero, bit 12.0 indicates that the PSE lacks support of the option to control which PSE Pinout Alternative is used for PD detection and power through the Pair Control (11.3:2) bits.

33.6 Data Link Layer classification

Additional control and classification functions are supported using Data Link Layer classification using frames based on the IEEE 802.3 Organizationally Specific TLVs defined in Clause 79. Type 2 PDs that require more than 13.0 W support Data Link Layer classification (see 33.3.5). Data Link Layer classification is optional for all other devices.

All reserved fields in transmitted Power via MDI TLVs shall contain zero, and all reserved fields in received Power via MDI TLVs shall be ignored.

33.6.1 TLV frame definition

Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB-2009; shall support the Power via MDI Type, Length, Value (TLV) defined in 79.3.2; and shall support the control state diagrams defined in 33.6.3.

33.6.2 Data Link Layer classification timing requirements

A Type 2 PSE shall send an LLDPDU containing a Power via MDI TLV within 10 seconds of Data Link Layer classification being enabled in the PSE as indicated by the variable pse_dll_enabled (33.2.4.4, 33.6.3.3).

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A Type 1 PSE that implements Data Link Layer classification shall send an LLDPDU containing a Power via MDI TLV when the PSE Data Link Layer classification engine is ready as indicated by the variable pse_dll_ready (33.6.3.3).

All Type 1 PDs that implement Data Link Layer classification and Type 2 PDs shall set the state variable pd_dll_ready within 5 minutes of Data Link Layer classification being enabled in a PD as indicated by the variable pd_dll_enabled (33.3.3.3, 33.6.3.3).

Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the “PSE allocated power value” field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the “PD requested power value” field is different from the previously communicated value.

Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the “PD requested power value” field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the “PSE allocated power value” field is different from the previously communicated value.

33.6.3 Power control state diagrams

The power control state diagrams for PSEs and PDs specify the externally observable behavior of a PSE and PD Data Link Layer classification respectively. PSE Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–27. PD Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–28.

33.6.3.1 Conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

33.6.3.2 Constants

PD_DLLMAX_VALUE

This value is derived from pd_max_power variable (33.3.3.3) described as follows:

pd_max_power	PD_DLLMAX_VALUE
0	130
1	39
2	65
3	130
4	255

PD_INITIAL_VALUE

This value is derived as follows from the pd_max_power (33.3.3.3) variable used in the PD state diagram (Figure 33–16):

pd_max_power	PD_INITIAL_VALUE
0	≤ 130
1	≤ 39
2	≤ 65
3	≤ 130
4	≤ 255

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PSE_INITIAL_VALUE

This value is derived as follows from parameter_type and the mr_pd_class_detected (33.2.4.6) variable used in the PSE state diagram (Figure 33–9):

parameter_type	mr_pd_class_detected	PSE_INITIAL_VALUE
1	0	130
1	1	39
1	2	65
1	3	130
1	4	130
2	4	255

33.6.3.3 Variables

The PSE power control state diagram (Figure 33–27) and PD power control state diagram (Figure 33–28) use the following variables:

MirroredPDRequestedPowerValue

The copy of PDRequestedPowerValue that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17). Power numbers are represented using an integer value in units of 0.1 W.

Values: 1 through 255

MirroredPDRequestedPowerValueEcho

The copy of PDRequestedPowerValueEcho that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17).

MirroredPSEAllocatedPowerValue

The copy of PSEAllocatedPowerValue that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.20). Power numbers are represented using an integer value in units of 0.1 W.

Values: 1 through 255

MirroredPSEAllocatedPowerValueEcho

The copy of PSEAllocatedPowerValue that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.20).

PDRequestedPowerValueEcho

This variable is updated by the PSE state diagram. This variable maps into the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).

Values: 1 through 255

PDMaxPowerValue

Integer that indicates the actual PD power value of the local system. The actual PD power value for a PD is the maximum input average power (see 33.3.7.2) the PD ever draws under the current power allocation. Power numbers are represented using an integer value in units of 0.1 W.

PDRequestedPowerValue

Integer that indicates the PD requested power value in the PD. The value is the maximum input average power (see 33.3.7.2) the PD requests. Power numbers are represented using an integer value in units of 0.1 W. This variable is mapped from the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).

Values: 1 through PD_DLLMAX_VALUE

PSEAllocatedPowerValue

Integer that indicates the PSE allocated power value in the PSE. Power numbers are represented using an integer value in units of 0.1 W. This variable is mapped from the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.20).

Values: 1 through 255

PSEAllocatedPowerValueEcho

This variable is updated by the PD state diagram. This variable maps into the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.20).

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Values: 1 through 255

TempVar

A temporary variable used to store Power Value, represented by an integer value in units of 0.1 W.

local_system_change

An implementation-specific control variable that indicates that the local system wants to change the allocated power value. In a PSE, this indicates it is going to change the power allocated to the PD. In a PD, this indicates it is going to request a new power allocation from the PSE.

Values:FALSE:The local system does not wants to change the power allocation.
TRUE:The local system wants to change the power allocation.

parameter_type

A control variable output by the PSE state diagram (Figure 33–9) used by a Type 2 PSE to choose operation with Type 1 or Type 2 PSE output PI electrical requirement parameter values defined in Table 33–11.

Values: 1: Type 1 PSE parameter values (default).
2: Type 2 PSE parameter values.

pd_dll_enabled

A variable output by the PD state diagram (Figure 33–16) to indicate if the PD Data Link Layer classification mechanism is enabled.

Values: FALSE:PD Data Link Layer classification is not enabled.
TRUE:PD Data Link Layer classification is enabled.

pd_dll_power_type

A control variable that indicates the type of PD that is connected to the PSE as advertised through Data Link Layer classification.

Values: 1: PD is a Type 1 PD (default).
2: PD is a Type 2 PD.

pd_dll_ready

An implementation-specific control variable that indicates that the PD has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.61).

Values:FALSE:Data Link Layer classification has not completed initialization.
TRUE:Data Link Layer classification has completed initialization.

pse_dll_enabled

A variable output by the PSE state diagram (Figure 33–9) to indicate if the PSE Data Link Layer classification mechanism is enabled.

Values: FALSE:PSE Data Link Layer classification is not enabled.
TRUE:PSE Data Link Layer classification is enabled.

pse_dll_power_type

A control variable that indicates the type of the PSE by which the PD is being powered.

Values: 1: PSE is a Type 1 PSE (default).
2: PSE is a Type 2 PSE.

pse_dll_ready

An implementation-specific control variable that indicates that the PSE has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.61).

Values:FALSE:Data Link Layer classification has not completed initialization.
TRUE:Data Link Layer classification has completed initialization.

pse_power_type

A control variable output by the PD state diagram (Figure 33–16) to indicate the type of PSE by which it is being powered.

A summary cross-references between the Power over Ethernet classification local and remote object class attributes and the PSE and PD power control state diagrams, including the direction of the mapping, is provided in Table 33–26.

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Table 33–26—Attribute to state diagram variable cross-reference

Entity	Attribute	Mapping	State diagram variable
oLldpXdot3LocSystemsGroup Object Class			
PSE	aLldpXdot3LocPDRequestedPowerValue	⇐	PDRequestedPowerValueEcho
	aLldpXdot3LocPSEAllocatedPowerValue	⇐	PSEAllocatedPowerValue
	aLldpXdot3LocReady	⇐	pse_dll_ready
PD	aLldpXdot3LocPDRequestedPowerValue	⇐	PDRequestedPowerValue
	aLldpXdot3LocPSEAllocatedPowerValue	⇐	PSEAllocatedPowerValueEcho
	aLldpXdot3LocReady	⇐	pd_dll_ready
oLldpXdot3RemSystemsGroup Object Class			
PSE	aLldpXdot3RemPDRequestedPowerValue	⇒	MirroredPDRequestedPowerValue
	aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValueEcho
	aLldpXdot3RemPowerType Value[a] 11 01	 ⇒ ⇒	pd_dll_power_type Value[a] 01 10
PD	aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValue
	aLldpXdot3RemPDRequestedPowerValue	⇒	MirroredPDRequestedPowerValueEcho
	aLldpXdot3RemPowerType Value[a] 10 00	 ⇒ ⇒	pse_dll_power_type Value[a] 01 10

[a]Other value combinations mapping from aLldpXdot3RemPowerType to pd_dll_power_type or pse_dll_power_type are not possible.

33.6.3.4 Functions

pse_power_review

This function evaluates the power allocation or budget of the PSE based on local system changes. The function returns the following variables:

PSE_NEW_VALUE:

The new maximum power value that the PSE expects the PD to draw. Power numbers are represented using an integer value in units of 0.1 W.

pd_power_review

This function evaluates the power requirements of the PD based on local system changes and/or changes in the PSE allocated power value. The function returns the following variables:

PD_NEW_VALUE:

The new maximum power value that the PD wants to draw. Power numbers are represented using an integer value in units of 0.1 W.

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33.6.3.5 State diagrams

The general state change procedure for PSEs is shown in Figure 33–27.

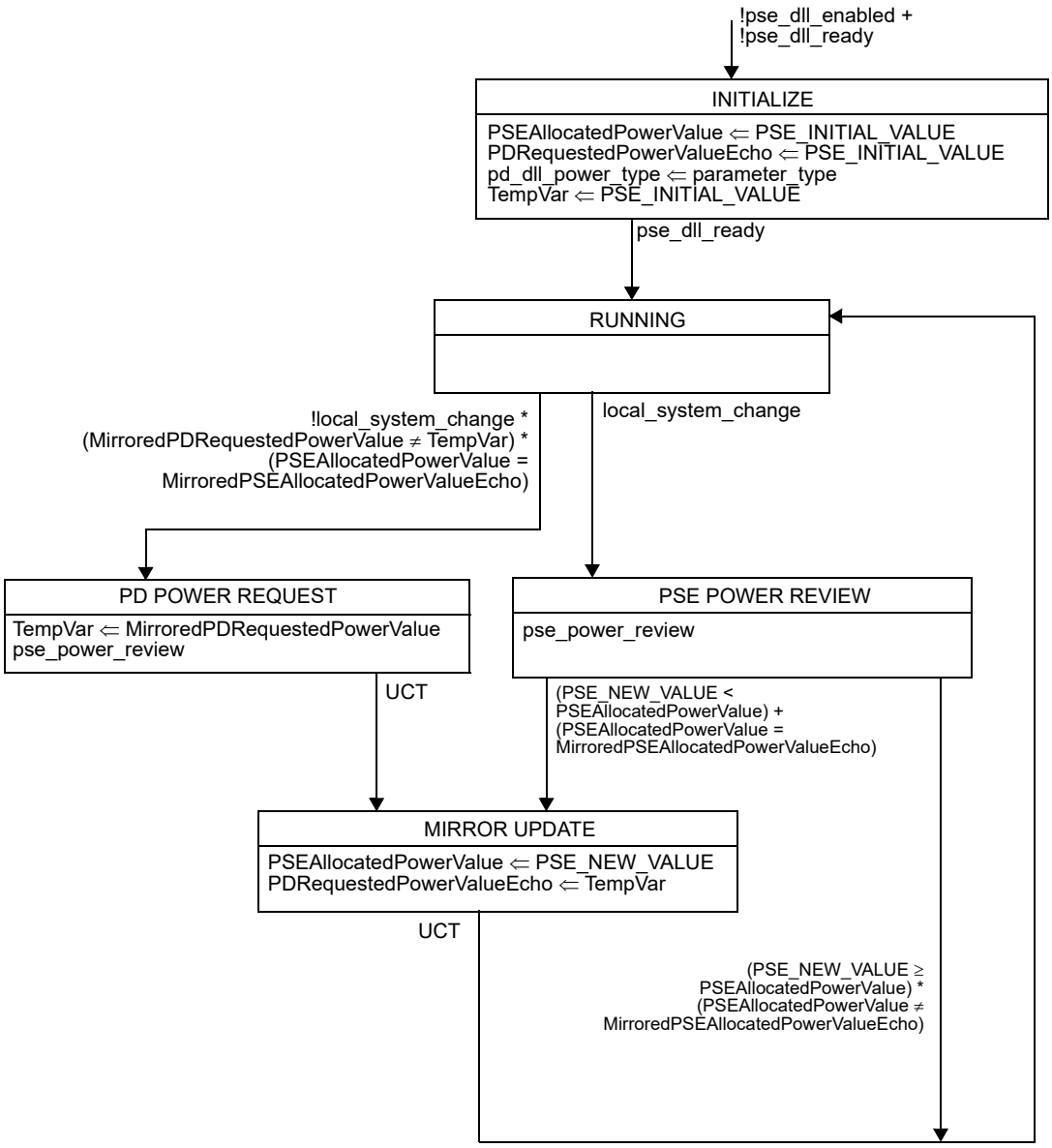

Figure 33–27—PSE power control state diagram

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The general state change procedure for PDs is shown in Figure 33–28.

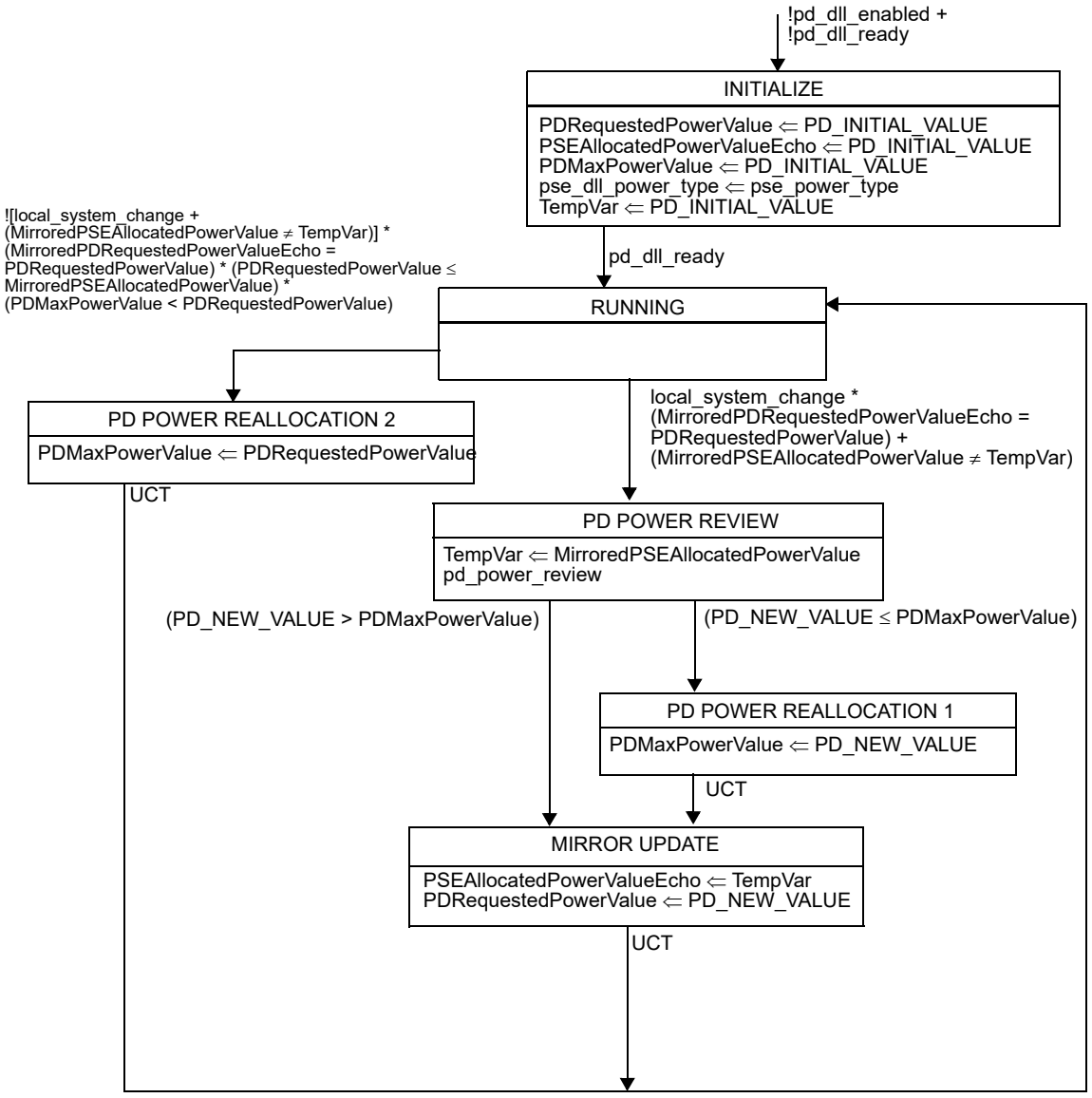

Figure 33–28—PD power control state diagram

33.6.4 State change procedure across a link

The PSE and PD utilize the LLDPDUs to advertise their various attributes to the other entity.

The PD may request a new power value through the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE responds to the PD's request through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.20) attribute in the oLldpXdot3LocSystemsGroup object class. The PSE also copies the value of the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) in the oLldpXdot3RemSystemsGroup object class

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to the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) in the oLldpXdot3LocSystemsGroup object class. This appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.20) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE may allocate a new power value through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.20) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.20) attribute in the oLldpXdot3RemSystemsGroup object class. The PD responds to a PSE's request through the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The PD also copies the value of the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.20) attribute in the oLldpXdot3RemSystemsGroup object class to the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.20) attribute in the oLldpXdot3LocSystemsGroup object class. This appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup object class.

The state diagrams describe the behavior above.

33.6.4.1 PSE state change procedure across a link

A PSE is considered to be in sync with the PD when the value of PSEAllocatedPowerValue matches the value of MirroredPSEAllocatedPowerValueEcho. When the PSE is not in sync with the PD, the PSE is only allowed to decrease its power allocation.

During normal operation, the PSE is in the RUNNING state. If the PSE wants to initiate a change in the PD allocation, the local_system_change is asserted and the PSE enters the PSE POWER REVIEW state, where a new power allocation value, PSE_NEW_VALUE, is computed. If the PSE is in sync with the PD or if PSE_NEW_VALUE is smaller than PSEAllocatedPowerValue, it enters the MIRROR UPDATE state where PSE_NEW_VALUE is assigned to PSEAllocatedPowerValue. It also updates PDRequestedPowerValueEcho and returns to the RUNNING state.

If the PSE sees a change to the previously stored MirroredPDRequestedPowerValue, it recognizes a request by the PD to change its power allocation. It entertains this request only when it is in sync with the PD. The PSE examines the request by entering the PD POWER REQUEST state. A new power allocation value, PSE_NEW_VALUE, is computed. It then enters the MIRROR UPDATE state where PSE_NEW_VALUE is assigned to PSEAllocatedPowerValue. It also updates PDRequestedPowerValueEcho and returns to the RUNNING state.

33.6.4.2 PD state change procedure across a link

A PD is considered to be in sync with the PSE when the value of PDRequestedPowerValue matches the value of MirroredPDRequestedPowerValueEcho. The PD is not allowed to change its maximum power draw or the requested power value when it is not in sync with the PSE.

During normal operation, the PD is in the RUNNING state. If the PD sees a change to the previously stored MirroredPSEAllocatedPowerValue or local_system_change is asserted by the PD so as to change its power allocation, it enters the PD POWER REVIEW state. In this state, the PD evaluates the change and generates an updated power value called PD_NEW_VALUE. If PD_NEW_VALUE is less than PDMaxPowerValue, it updates PDMaxPowerValue in the PD POWER REALLOCATION 1 state. The PD finally enters the MIRROR UPDATE state where PD_NEW_VALUE is assigned to PDRequestedPowerValue. It also updates PSEAllocatedPowerValueEcho and returns to the RUNNING state.

In the above flow, if PD_NEW_VALUE is greater than PDMaxPowerValue, the PD waits until it is in sync with the PSE and the PSE grants the higher power value. When this condition arises, the PD enters the PD

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POWER REALLOCATION 2 state. In this state, the PD assigns PDMaxPowerValue to PDRequestedPowerValue and returns to the RUNNING state.

33.7 Environmental

33.7.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2. The PSE shall be classified as a Limited Power Source in accordance with Annex Q of IEC 62368-1:2018, as applicable.

Equipment shall comply with all applicable local and national codes related to safety.

33.7.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns. The list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to verify compliance with the appropriate requirements. LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards should be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures should be taken to verify that the intended safety features are not negated during installation of a new network or during modification of an existing network.

33.7.3 Installation and maintenance guidelines

It is a mandatory requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

It is a mandatory requirement that, during installation of the cabling plant, care be taken to verify that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

33.7.4 Patch panel considerations

It is possible that the current carrying capability of a cabling cross-connect may be exceeded by a PSE. The designer should consult the manufacturers' specifications to verify compliance with the appropriate requirements.

33.7.5 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to a PSE or PD. Other than voice signals, the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply:

Battery voltage to a telephone line is generally 56 Vdc, applied to the line through a balanced 400 Ω source impedance. Ringing voltage is a composite signal consisting of an AC component and a DC component. The

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AC component is up to 175 Vp at 20 Hz to 60 Hz with a 100 Ω source resistance. The DC component is 56 Vdc with 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Application of any of the above voltages to the PI of a PSE or a PD shall not result in any safety hazard.

33.7.6 Electromagnetic emissions

The PD and PSE powered cabling link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

33.7.7 Temperature and humidity

The PD and PSE powered cabling link segment is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling. Specific requirements and values for these parameters are beyond the scope of this standard.

33.7.8 Labeling

It is recommended that the PSE or PD (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Power classification and power level in terms of maximum current drain over the operating voltage range, 36 V to 57 V, applies for PD only
b) Port type (e.g., 100BASE-TX, TIA Category, or ISO Class)
c) Any applicable safety warnings
d) “PSE” or “PD” as appropriate
e) Type (e.g., “Type 1” or “Type 2”)

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33.8 Protocol implementation conformance statement (PICS) proforma for Clause 33, Power over Ethernet over 2 Pairs[73]

33.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 33, Power over Ethernet over 2 Pairs, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

33.8.2 Identification

33.8.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

33.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 33, Power over Ethernet over 2 Pairs
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[73] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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33.8.2.3 PD Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PDT2	Type 2 PD implementation	33.3.2	PD is Type 2	O	Yes [ ] No [ ]
*PDCL	PD Classification	33.3.5	PD supports classification	PDT2:M	Yes [ ] No [ ]
*PDCL2	Implementation supports 2-Event class signature	33.3.5	PD supports 2-Event class signature	PDT2:M	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	33.6	PD supports Data Link Layer classification	PDT2:M	Yes [ ] No [ ]

33.8.2.4 PSE Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PSET1	Type 1 PSE implementation	33.1.4	Optional	O	Yes [ ] No [ ]
*PSET2	Type 2 PSE implementation	33.1.4	Optional	O	Yes [ ] No [ ]
*MID	Midspan PSE	33.2.1	PSE implemented as a midspan device	O/1	Yes [ ] No [ ]
*MIDA	Alternative A Midspan PSE	33.2.2	Midspan PSE implements Alternative A	MID:O:2	Yes [ ] No [ ]
*MAN	PSE supports management registers accessed through MII Management Interface	33.5	Optional	O	Yes [ ] No [ ]
*CL	Implementation supports Physical Layer classification	33.2.6	Optional	O/1	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	33.6	PSE supports Data Link Layer classification	O	Yes [ ] No [ ]
*1EPLC	Implementation supports 1-Event Physical Layer classification	33.2.6.1	Optional	O	Yes [ ] No [ ]
*2EPLC	Implementation supports 2-Event Physical Layer classification	33.2.6.2	Optional	O	Yes [ ] No [ ]
*PA	Power Allocation	33.2.8	PSE implements power supply allocation	O	Yes [ ] No [ ]
*PCA	Pair control ability—PSE supports the option to control which PSE Pinout is used	33.5.1.1.5	Optional	O	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
*AC	Monitor AC MPS	33.2.9.1.1	PSE monitors for AC MPS	O.3	Yes [ ] No [ ]
*DC	Monitor DC MPS	33.2.9.1.2	PSE monitors for DC MPS	O.3	Yes [ ] No [ ]

33.8.3 PICS proforma tables for Power over Ethernet over 2 Pairs

33.8.3.1 Common device features

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Compatibility considerations.	33.1.2	PDs and PSEs compatible at their PIs	M	Yes [ ]
COM2	Type 2 operation cabling	33.1.4.1	DC loop resistance 25 Ω or less. Requirement satisfied by category 5e components (cables, cords, and connectors)	M	Yes [ ]
COM3	Resistance unbalance	33.1.4.2	3 % or less	M	Yes [ ]

33.8.3.2 Power sourcing equipment

Item	Feature	Subclause	Value/Comment	Status	Support
PSE1	PSE location	33.2.1	Requirements apply equally to Endpoint and Midspan PSE unless otherwise stated	M	Yes [ ]
PSE2	Alternative A and Alternative B	33.2.3	Implement either Alternative A or Alternative B or both but not operate on same link section simultaneously	M	Yes [ ]
PSE3	PSE behavior	33.2.4	In accordance with state diagrams shown in Figure 33–9, Figure 33–9 continued, and Figure 33–10	M	Yes [ ]
PSE4	Detection, classification, and turn on timing	33.2.4.1	In accordance with Table 33–4, Table 33–10, and Table 33–11	M	Yes [ ]
PSE5	Backoff voltage	33.2.4.1	Not greater than V_{Off}	M	Yes [ ]
PSE6	PSE variable definition permutations	33.2.4.4	Meet at least one allowable definition described in Table 33–3	M	Yes [ ]
PSE7	Type 2 PSE mutual identification	33.2.4.6	When powering a Type 2 PD, assigns a value of ‘2’ to parameter_type if mutual identification is complete	PSET2: M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE8	Type 2 PSE powering a Type 1 PD	33.2.4.6	Meets the PI electrical requirements of a Type 1 PSE, but may choose to meet the electrical requirements of a Type 2 PSE for I_{Con}, I_{LIM}, T_{LIM}, and P_{Type}	PSET2: M	Yes [ ] N/A [ ]
PSE9	Applying power	33.2.5	Not until a PD requesting power has been successfully detected	M	Yes [ ]
PSE10	Power pairs	33.2.5	Power supplied on the same pairs as those used for detection	M	Yes [ ]
PSE11	Detecting PDs	33.2.5.1	Performed via the PSE PI	M	Yes [ ]
PSE12	PSE presents non-valid signature	33.2.5.1	As defined in Table 33–15	M	Yes [ ]
PSE13	Open circuit voltage and short circuit current	33.2.5.1	Meet specifications for V_{oc} and I_{sc} in Table 33–4	M	Yes [ ]
PSE14	Backdriven current	33.2.5.1	Not be damaged by up to 5 mA over the range of V_{Port_PSE}	M	Yes [ ]
PSE15	Output capacitance	33.2.5.1	C_{out} in Table 33–11	M	Yes [ ]
PSE16	Detection voltage with a valid PD signature connected	33.2.5.2	Meets V_{valid} in Table 33–4	M	Yes [ ]
PSE17	Detection voltage measurements	33.2.5.2	At least two that create at least ΔV_{test} difference	M	Yes [ ]
PSE18	Control slew rate when switching detection voltages	33.2.5.2	Less than V_{slew} in Table 33–4	M	Yes [ ]
PSE19	Accept as a valid signature	33.2.5.3	R_{good} and C_{good}, with up to V_{os} max and I_{os} max as defined in Table 33–5	M	Yes [ ]
PSE20	Reject as an invalid signature	33.2.5.4	Resistance less than R_{bad} min, resistance greater than R_{bad} max, or capacitance greater than C_{bad} min	M	Yes [ ]
PSE21	Classification permutations	33.2.6	Meet one allowable permutation in Table 33–8	M	Yes [ ]
PSE22	Type 1 PSE does not implement Physical Layer classification	33.2.6	Assign all PDs to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE23	Type 1 PSE failure to complete classification	33.2.6	Return to IDLE state or assign PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE24	Type 2 PSE failure to complete classification	33.2.6	Return to IDLE state	PSET2: M	Yes [ ] N/A [ ]
PSE25	Provide V_{Class} for 1-Event Physical Layer classification	33.2.6.1	Limited to I_{Class_LIM} as defined by Table 33–10	1EPLC: M	Yes [ ] N/A [ ]
PSE26	Classification polarity for 1-Event Physical Layer classification	33.2.6.1	Same as V_{Port_PSE}	1EPLC: M	Yes [ ] N/A [ ]
PSE27	Classification timing for 1-Event Physical Layer classification	33.2.6.1	In accordance with T_{pdc} in Table 33–10	1EPLC: M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE28	Measurement result of 1-Event Physical Layer classification I_{Class}	33.2.6.1	Classify PD according to observed current based on Table 33–9	1EPLC: M	Yes [ ] N/A [ ]
PSE29	Measurement timing of 1-Event Physical Layer classification I_{Class}	33.2.6.1	Measurement taken after the minimum relevant class event timing in Table 33–10	1EPLC: M	Yes [ ] N/A [ ]
PSE30	Class 4 result for 1-Event Physical Layer classification with a Type 1 PSE	33.2.6.1	Assign the PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE31	Type 1 PSE 1-Event Physical Layer classification if I_{Class} is in the range of I_{Class_LIM}	33.2.6.1	Return to IDLE state or assign PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE32	Type 2 PSE 1-Event Physical Layer classification if I_{Class} is in the range of I_{Class_LIM}	33.2.6.1	Return to IDLE state	PSET2: M	Yes [ ] N/A [ ]
PSE33	In the CLASS_EV1 and CLASS_EV2 states, provide V_{Class}	33.2.6.2	As defined in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE34	Classification timing in CLASS_EV1 state	33.2.6.2	In accordance with T_{CLE1} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE35	In the CLASS_EV1 and CLASS_EV2 states, measurement result I_{Class}	33.2.6.2	Classify PD according to Table 33–9	2EPLC: M	Yes [ ] N/A [ ]
PSE36	In the MARK_EV1 and MARK_EV2 states, provide V_{Mark}	33.2.6.2	In accordance with Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE37	Classification timing in MARK_EV1	33.2.6.2	In accordance with T_{ME1} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE38	Classification timing in CLASS_EV2 state	33.2.6.2	In accordance with T_{CLE2} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE39	Classification timing in MARK_EV2 state	33.2.6.2	In accordance with T_{ME2} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE40	Type 2 PSE 2-Event Physical Layer classification if I_{Class} is greater than or equal to I_{Class_LIM} min	33.2.6.2	Returns to IDLE state	2EPLC: M	Yes [ ] N/A [ ]
PSE41	Current limitation during class events	33.2.6.2	Meet I_{Class_LIM}	2EPLC: M	Yes [ ] N/A [ ]
PSE42	Current limitation during mark events	33.2.6.2	Meet I_{Mark_LIM}	2EPLC: M	Yes [ ] N/A [ ]
PSE43	Measurement timing of 2-Event Physical Layer classification I_{Class}	33.2.6.2	Taken after the minimum relevant class event timing in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE44	Class event and mark event voltages polarity	33.2.6.2	Same as V_{Port_PSE}	2EPLC: M	Yes [ ] N/A [ ]
PSE45	Voltage level at PI when transition to POWER_ON state	33.2.6.2	Completes 2-Event classification and transitions to POWER_ON with PI voltage greater than or equal to V_{Mark} min	2EPLC: M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE46	Return to IDLE state	33.2.6.2	Maintains PI voltage at V_{Reset} for at least T_{Reset} min before starting new detection cycle	2EPLC: M	Yes [ ] N/A [ ]
PSE47	Power supply output	33.2.7	When the PSE provides power to the PI, conforms with Table 33–11	M	Yes [ ]
PSE48	Load regulation	33.2.7.1	Met with (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min load step at a rate of change of up to 15 mA/µs max	M	Yes [ ]
PSE49	Voltage transients	33.2.7.1	Limited to 3.5 V/µs max for load changes up to 35 mA/µs	M	Yes [ ]
PSE50	Voltage transients (30 µs to 250 µs)	33.2.7.2	No less than K_{Tran_lo} below V_{Port_PSE} min and meet requirements of 33.2.7.7.	PSET2: M	Yes [ ]
PSE51	Voltage transients (greater than 250 µs)	33.2.7.2	Meet V_{Port_PSE} specification	M	Yes [ ]
PSE52	Power feeding ripple and noise	33.2.7.3	Met for common-mode and/or pair-to-pair noise values for power outputs from (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min at static operating V_{Port_PSE}	M	Yes [ ]
PSE53	AC current waveform parameters	33.2.7.4	I_{Peak} minimum equals Equation (33–4) for T_{CUT} minimum and 5% duty cycle minimum.	M	Yes [ ]
PSE54	Inrush current limit	33.2.7.5	PSE limits the maximum current sourced at the PI	M	Yes [ ]
PSE55	Inrush current template	33.2.7.5	Current sourced does not exceed the PSE inrush template in Figure 33–13	M	Yes [ ]
PSE56	Short circuit condition	33.2.7.7	Remove power from PI before I_{PSEUT} is exceeded. Equation (33–6) and Figure 33–14.	M	Yes [ ]
PSE57	Short circuit current and time	33.2.7.7	In accordance with I_{LIM} and T_{LIM} in Table 33–11	M	Yes [ ]
PSE58	Short circuit power removal	33.2.7.7	Begins within T_{LIM} in Table 33–11	M	Yes [ ]
PSE59	Turn off time	33.2.7.8	Applies to the discharge time from V_{Port_PSE} to V_{Off} with a test resistor of 320 kΩ attached to the PI.	M	Yes [ ]
PSE60	Turn off voltage	33.2.7.9	Applies to the PI voltage in the IDLE state	M	Yes [ ]
PSE61	Current unbalance	33.2.7.11	Applies to the two conductors of a power pair over the current load range in accordance with I_{unb} in Table 33–11.	M	Yes [ ]
PSE62	Type 2 PSEs in the presence of (I_{unb} / 2)	33.2.7.11	Meet the requirements of 25.4.5	PSET2: M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE63	Power allocation	33.2.8	Not be based solely on historical data of power consumption of the attached PD	PA:M	Yes [ ] N/A [ ]
PSE64	PSE monitoring AC MPS component	33.2.9.1.1	Meets “AC Signal parameters” and “PSE PI voltage during AC disconnect detection” parameters in Table 33–12	AC:M	Yes [ ] N/A [ ]
PSE65	PSE AC MPS component present	33.2.9.1.1	When AC impedance at the PI is equal to or lower than $\|Z_{ac1}\|$ in Table 33–12	AC:M	Yes [ ] N/A [ ]
PSE66	PSE AC MPS component absent	33.2.9.1.1	When AC impedance at the PI equal to or greater than $\|Z_{ac2}\|$ in Table 33–12	AC:M	Yes [ ] N/A [ ]
PSE67	Power removal	33.2.9.1.1	When AC MPS has been absent for a time duration greater than T_{MPDO}	AC:M	Yes [ ] N/A [ ]
PSE68	PSE DC MPS component present	33.2.9.1.2	I_{Port} is greater than or equal to I_{Hold} max for at least T_{MPS} min as specified in Table 33–11	DC:M	Yes [ ] N/A [ ]
PSE69	PSE DC MPS component absent	33.2.9.1.2	I_{Port} is less than or equal to I_{Hold} min as specified in Table 33–11	DC:M	Yes [ ] N/A [ ]
PSE70	Power removal	33.2.9.1.2	When DC MPS has been absent for a time duration greater than T_{MPDO}	DC:M	Yes [ ] N/A [ ]
PSE71	T_{MPS} and T_{MPDO} values	33.2.9.1.2	Meet Equation (33–8)	DC:M	Yes [ ] N/A [ ]
PSE72	Not remove power	33.2.9.1.2	When less than T_{MPDO} has passed since MPS was last present	DC:M	Yes [ ] N/A [ ]

33.8.3.3 Powered devices

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Accept power	33.3.1	On either set of PI conductors	M	Yes [ ]
PD2	Polarity insensitive	33.3.1	Both Mode A and Mode B per Table 33–13	M	Yes [ ]
PD3	Source power	33.3.1	The PD does not source power on its PI	M	Yes [ ]
PD4	Voltage tolerance	33.3.1	Withstand 0 V to 57 V at the PI indefinitely without permanent damage	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD5	Underpowered Type 2 PD	33.3.2	If PD does not successfully observe 2-Event Physical Layer classification or Data Link Layer classification, conforms to Type 1 PD power restrictions and provides the user with an active indication if underpowered	PDT2:M	Yes [ ] N/A [ ]
PD6	Current unbalance	33.3.2	Type 2 PDs meet the requirements of 25.4.5 in presence of (I_{unb}/2)	PDT2:M	Yes [ ] N/A [ ]
PD7	PD behavior	33.3.3	According to state diagram shown in Figure 33–16	M	Yes [ ]
PD8	Valid and non-valid detection signatures	33.3.4	Presented between positive V_{PD} and negative V_{PD} on each set of pairs defined in 33.3.1	M	Yes [ ]
PD9	Non-valid detection signature	33.3.4	When powered, present an invalid signature on the set of pairs not drawing power	M	Yes [ ]
PD10	Valid detection signature	33.3.4	Characteristics defined in Table 33–14	M	Yes [ ]
PD11	Non-valid detection signature	33.3.4	Exhibit one or both of the characteristics described in Table 33–15	M	Yes [ ]
PD12	PD classifications	33.3.5	Meets at least one permutation listed in Table 33–8	PDCL:M	Yes [ ]
PD13	PD implementing 2-Event class signature	33.3.5.1	Returns Class 4	PDCL2:M	Yes [ ] N/A [ ]
PD14	Type 2 PD classification behavior	33.3.5.1	Conforms to electrical specifications in Table 33–17	PDT2:M	Yes [ ] N/A [ ]
PD15	Classification signature	33.3.5.1	As defined in Table 33–16	PDCL:M	Yes [ ] N/A [ ]
PD16	Classification signature	33.3.5.1	One classification signature during classification	PDCL:M	Yes [ ] N/A [ ]
PD17	2-Event class signature	33.3.5.2	Class 4 in accordance with the maximum power draw as specified in Table 33–18	PDCL2:M	Yes [ ] N/A [ ]
PD18	2-Event class signature behavior	33.3.5.2	As defined in Table 33–17	PDCL2:M	Yes [ ] N/A [ ]
PD19	Type 2 PD electrical requirements	33.3.5.2	As defined by Table 33–18 of the Type defined in its pse_power_type state variable	PDT2:M	Yes [ ] N/A [ ]
PD20	Mark event current and 2-Event class signature	33.3.5.2.1	Draw I_{Mark} and present a non-valid detection signature as defined in Table 33–15	PDCL2:M	Yes [ ] N/A [ ]
PD21	Mark event current limits	33.3.5.2.1	Not exceed I_{Mark} when voltage at the PI enters V_{Mark} as defined in Table 33–17	PDCL2:M	Yes [ ] N/A [ ]
PD22	PD current draw	33.3.5.2.1	I_{Mark} until the PD transitions from DO_MARK_EVENT state to the IDLE state	PDCL2:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD23	PSE identification	33.3.6	Identify as Type 1 or Type 2 (see Figure 33–16)	PDT2:M	Yes [ ]
PD24	PD power supply	33.3.7	Operate within the characteristics in Table 33–18	M	Yes [ ]
PD25	PD turn on voltage	33.3.7.1	PD turns on at a voltage less than or equal to V_{On}	M	Yes [ ]
PD26	PD stay on voltage	33.3.7.1	Stay on for all voltages in the range of V_{Port_PD}	M	Yes [ ]
PD27	PD turn off voltage	33.3.7.1	Turn off at a voltage less than V_{Port_PD} min and greater than V_{Off}	M	Yes [ ]
PD28	Startup oscillations	33.3.7.1	Shall turn on or off without startup oscillations and within the first trial at any load value	M	Yes [ ]
PD29	P_{Port_PD} definition	33.3.7.2.1	When PD is fed by V_{Port_PD} min to V_{Port_PD} max with R_{Ch} (as defined in Table 33–1) in series	M	Yes [ ]
PD30	PD input inrush current	33.3.7.3	Draw less than I_{Inrush_PD} from T_{Inrush} min until T_{delay}	M	Yes [ ]
PD31	Power limits when pse_power_type = 1	33.3.7.3	Conform to P_{Class_PD} and P_{Peak_PD} within T_{Inrush} min	M	Yes [ ]
PD32	Power limits when pse_power_type = 2	33.3.7.3	Conform to Class 3 P_{Peak_PD} from T_{Inrush} min until T_{delay}	PDT2:M	Yes [ ] N/A [ ]
PD33	Peak power	33.3.7.4	Not to exceed P_{Class_PD} max for more than T_{CUT} min and 5% duty cycle	M	Yes [ ]
PD34	Peak operating power	33.3.7.4	Not to exceed P_{Peak_PD} max	M	Yes [ ]
PD35	RMS, DC, and ripple current	33.3.7.4	Bounded by Equation (33–11)	M	Yes [ ]
PD36	Maximum I_{Port} for all operating V_{Port_PD}	33.3.7.4	Defined by Equation (33–12)	M	Yes [ ]
PD37	Peak transient current	33.3.7.5	Not to exceed 4.70 mA/µs in either polarity	M	Yes [ ]
PD38	Specifications for I_{PDUT}	33.3.7.5	Operate below upperbound template defined in Figure 33–18	M	Yes [ ]
PD39	Behavior during transients at the PSE PI	33.3.7.6	As specified in 33.3.7.6	M	Yes [ ]
PD40	Ripple and noise	33.3.7.7	As specified in Table 33–18 for the common-mode and/or differential pair-to-pair noise at the PD PI	M	Yes [ ]
PD41	Ripple and noise specification	33.3.7.7	For all operating voltages in the range defined by V_{Port_PD} in Table 33–18	M	Yes [ ]
PD42	Ripple and noise presence	33.3.7.7	Operates in the presence of ripple and noise generated by the PSE that appears at the PD PI	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD43	Classification stability	33.3.7.8	Class signature valid within T_{class} and remains valid for the duration of the classification period	M	Yes [ ]
PD44	Backfeed voltage for Mode A	33.3.7.9	As specified in 33.3.7.9	M	Yes [ ]
PD45	Backfeed voltage for Mode B	33.3.7.9	As specified in 33.3.7.9	M	Yes [ ]
PD46	Maintain power signature	33.3.8	PD provides a valid MPS at the PI as defined in 33.3.8	M	Yes [ ]
PD47	No longer require power	33.3.8	Remove both components of the Maintain Power Signature	M	Yes [ ]

33.8.3.4 Electrical specifications applicable to the PSE and PD

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Conductor isolation	33.4.1	Conforms to J.1 with electrical strength test c) details as specified in 33.4.1	M	Yes [ ]
EL2	Isolation and grounding requirements	33.4.1	Conductive link segments that have different requirements have those requirements provided by the port-to-port isolation of the NID	M	Yes [ ]
EL3	Environment A requirements for multiple instances of PSE and/or PD	33.4.1.1.1	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL4	Environment A requirement	33.4.1.1.1	Switch more negative conductor	M	Yes [ ] N/A [ ]
EL5	Environment B requirements for multiple instances of PSE and/or PD	33.4.1.1.2	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL6	Fault tolerance for PIs encompassed within the MDI	33.4.2	Meet requirements of the appropriate specifying clause	!MID:M	Yes [ ] N/A [ ]
EL7	Fault tolerance for PSE PIs not encompassed within an MDI	33.4.2	Meet the requirements of 33.4.2	M	Yes [ ] N/A [ ]
EL8	Common-mode fault tolerance	33.4.2	Each wire pair withstands without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity	M	Yes [ ]
EL9	The shape of the impulse for item common-mode fault tolerance	33.4.2	0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value)	M	Yes [ ]
EL10	Common-mode to differential-mode impedance balance for transmit and receive pairs	33.4.3	Exceeds value in Table 33–20 for all supported PHY speeds	M	Yes [ ]
EL11	Common-mode AC output voltage	33.4.4	Not to exceed the values in Table 33–21	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
EL12	Common-mode AC output voltage measurement	33.4.4	While the PHY is transmitting data, the PSE or PD is operating, and with the enumerated PSE load or PD source	M	Yes [ ]
EL13	Noise from an operating PSE or PD to the differential transmit and receive pairs	33.4.6	Does not exceed 10 mV peak-to-peak measured from 1 MHz to 100 MHz under the conditions specified in 33.4.4	M	Yes [ ]
EL14	Coupled noise E_{d_out}	33.4.6	Not to exceed 10 mV peak-to-peak in the band from 1 MHz to 10 MHz	M	Yes [ ]
EL15	Coupled noise E_{d_out}	33.4.6	Not to exceed 10 mV peak-to-peak in the band from 10 MHz to 100 MHz (for 2.5GBASE-T), 10 MHz to 250 MHz (for 5GBASE-T), and 10 MHz to 500 MHz (for 10GBASE-T) under the conditions specified in 33.4.4.	M	Yes [ ]
EL16	Return loss requirements	33.4.7	Specified in 14.3.1.3.4 for a 10 Mb/s PHY, in ANSI INCITS 263-1995 for a 100 Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY	M	Yes [ ]
EL17	100BASE-TX Type 2 Endpoint PSE and PD channel unbalance	33.4.8	Meet requirements of Clause 25 in the presence of (I_{unb}/2)	M	Yes [ ] N/A [ ]

33.8.3.5 Electrical specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL1	Short circuit fault tolerance	33.4.2	Any wire pair withstands any short circuit to any other pair for an indefinite amount of time	M	Yes [ ]
PSEEL2	Magnitude of short circuit current	33.4.2	Does not exceed I_{LIM} max	M	Yes [ ]
PSEEL3	Limitation of electromagnetic interference.	33.4.5	PSE complies with applicable local and national codes	M	Yes [ ]
PSEEL4	Alternative A Type 2 Midspan PSEs that support 100BASE-TX	33.4.8	Enforce channel unbalance currents less than or equal to Type 1 Iunb (see Table 33–11) or meet 33.4.9.4.	MIDA: M	Yes [ ] N/A [ ]
PSEEL5	Insertion of Midspan at FD	33.4.9	Comply with the guidelines specified in 33.4.9 items a) and b)	MID:M	Yes [ ] N/A [ ]
PSEEL6	Resulting “channel”	33.4.9	Installation of a Midspan PSE does not increase the length to more than 100 m as defined in ISO/IEC 11801.	MID:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL7	Configurations with Midspan PSE	33.4.9	Not alter transmission requirements of the "permanent link"	MID:M	Yes [ ] N/A [ ]
PSEEL8	DC continuity in power injecting pairs	33.4.9	Does not provide DC continuity between the two sides of the segment for the pairs that inject power	MID:M	Yes [ ] N/A [ ]
PSEEL9	Midspan PSE inserted as a connection or telecommunications outlet	33.4.9.1	Meet transmission parameters NEXT, insertion loss, and return loss	MID:M	Yes [ ] N/A [ ]
PSEEL10	Midspan PSE NEXT	33.4.9.1.1	Meet values detemined by Equation (33–17) from 1 MHz to 100 MHz, but not greater than 65 dB	MID:M	Yes [ ] N/A [ ]
PSEEL11	Midspan PSE Insertion Loss	33.4.9.1.2	Meet values determined by Equation (33–20) from 1 MHz to 100 MHz, but not less than 0.1 dB	MID:M	Yes [ ] N/A [ ]
PSEEL12	Midspan PSE Return Loss	33.4.9.1.3	Meet or exceed values in Table 33–22 for transmit and receive pairs from 1 MHz to 100 MHz	MID:M	Yes [ ] N/A [ ]
PSEEL13	Work area or equipment cable Midspan PSE	33.4.9.2	Meet the requirements of this clause and the specifications for a Category 5 (jumper) cord as specified in ISO/IEC 11801-2002 or ANSI/TIA-568-C.2 for insertion loss, NEXT, and return loss for transmit and receive pairs	MID:M	Yes [ ] N/A [ ]
PSEEL14	Alternative A Midspan PSE signal path requirements	33.4.9.4	Exceed transfer function gain expressed in Equation (33–23) from 0.10 MHz to 1 MHz at the pins of the PI used as 100BASE-TX transmit pins	MIDA: M	Yes [ ] N/A [ ]
PSEEL15	Alternative A Midspan PSE signal path requirements bias current	33.4.9.4	Met with DC bias current between 0 mA and (I_{unb}/2)	MIDA: M	Yes [ ] N/A [ ]

33.8.3.6 Electrical specifications applicable to the PD

Item	Feature	Subclause	Value/Comment	Status	Support
PDEL1	PD common-mode test requirement	33.4.4	The PIs that require power terminated as illustrated in Figure 33–22	M	Yes [ ]

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33.8.3.7 Management function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Management capability	33.5	Access to register definitions defined in 33.5.1 via interface described in 22.2.4 or 45.2 or equivalent.	MAN:M	Yes [ ] N/A [ ]
MF2	PSE registers	33.5.1	Register address 11 for control functions and register address 12 for status functions.	MAN:M	Yes [ ] N/A [ ]
MF3	Register bits latching high (LH)	33.5.1	Remain high until read via the management interface.	MAN:M	Yes [ ] N/A [ ]
MF4	Latching register bit after read	33.5.1	Assumes a value based on the current state of the condition it monitors.	MAN:M	Yes [ ] N/A [ ]
MF5	PSE Control register reserved bits (11.15:6)	33.5.1.1.1	Not affected by writes and return a value of zero when read.	MAN:M	Yes [ ] N/A [ ]
MF6	Data Link Layer classification not supported	33.5.1.1.2	Ignore writes to bit 11.5 and return a value of zero when read.	MAN* !DLLC: M	Yes [ ] N/A [ ]
MF7	Data Link Layer classification supported	33.5.1.1.2	Ignore writes to bit 11.5 and return a value of one when function cannot be disabled.	MAN* DLLC: M	Yes [ ] N/A [ ]
MF8	Enable/disable Data Link Layer classification capability	33.5.1.1.2	Capability enabled by setting bit 11.5 to one and disabled by setting bit 11.5 to zero.	MAN* DLLC: M	Yes [ ] N/A [ ]
MF9	Physical Layer classification not supported	33.5.1.1.3	Ignore writes to bit 11.4 and return a value of zero when read.	MAN* !CL:M	Yes [ ] N/A [ ]
MF10	Physical Layer classification supported	33.5.1.1.3	Ignore writes to bit 11.4 and return a value of one when function cannot be disabled.	MAN* CL:M	Yes [ ] N/A [ ]
MF11	Enable/disable Physical Layer classification	33.5.1.1.3	Function enabled by setting bit 11.4 to one and disabled by setting bit 11.5 to zero.	MAN* CL:M	Yes [ ] N/A [ ]
MF12	Pair Control Ability not supported	33.5.1.1.4	Ignore writes to bits 11.3:2.	MAN* !PCA:M	Yes [ ] N/A [ ]
MF13	Writes to 11.3:2 when Pair Control Ability not supported	33.5.1.1.4	Return the value that reports the supported PSE Pinout Alternative.	MAN* !PCA:M	Yes [ ] N/A [ ]
MF14	Bits 11.3:2 set to '01'	33.5.1.1.4	Forces the PSE to use Alternative A.	MAN* PCA:M	Yes [ ] N/A [ ]
MF15	Bits 11.3:2 set to '10'	33.5.1.1.4	Forces the PSE to use Alternative B.	MAN* PCA:M	Yes [ ] N/A [ ]
MF16	Pair control ability bit (12.0)	33.5.1.1.4	A value of one sets the mr_pse_alternative variable.	MAN* PCA:M	Yes [ ] N/A [ ]
MF17	PSE function disabled	33.5.1.1.5	Setting PSE Enable bits 11.1:0 to a ‘00’, also the MDI shall function as it would if it had no PSE function.	MAN:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MF18	PSE function enabled	33.5.1.1.5	Setting PSE Enable bits 11.1:0 to a '01'.	MAN:M	Yes [ ] N/A [ ]
MF19	PSE enable bits (11.1:0)	33.5.1.1.5	Writing to these register bits shall set mr_pse_enable to the corresponding value: '00' = disable, '01' = enable and '10' = force power.	MAN:M	Yes [ ] N/A [ ]
MF20	PSE Type electrical parameters bit (12.15)	33.5.1.2.1	Set to zero when the PSE state diagram sets the state variable set_parameter_type to 1. Set to one when set_parameter_type is set to 2.	MAN:M	Yes [ ] N/A [ ]
MF21	Data Link Layer classification enabled bit (12.14)	33.5.1.2.2	Set to one when the PSE state diagram sets true pse_dll_enabled. Set to zero when the PSE state diagram sets false pss_dll_enabled.	MAN:M	Yes [ ] N/A [ ]
MF22	Power denied bit (12.12)	33.5.1.2.4	A value of one indicates power has been denied or removed due to an error condition.	MAN:M	Yes [ ] N/A [ ]
MF23	Power denied bit implementation	33.5.1.2.4	Implemented with a latching high behavior as defined in 33.5.1.	MAN:M	Yes [ ] N/A [ ]
MF24	Valid signature bit (12.11)	33.5.1.2.5	One indicates a valid signature has been detected. Set to one when mr_valid_signature transitions from FALSE to TRUE.	MAN:M	Yes [ ] N/A [ ]
MF25	Valid signature bit implementation	33.5.1.2.5	Implemented with a latching high behavior as defined in 33.5.1.	MAN:M	Yes [ ] N/A [ ]
MF26	Invalid signature bit (12.10)	33.5.1.2.6	One indicates an invalid signature has been detected. Set to one entering SIGNATURE_INVALID state.	MAN:M	Yes [ ] N/A [ ]
MF27	Invalid signature bit implementation	33.5.1.2.6	Implemented with a latching high behavior as defined in 33.5.1.	MAN:M	Yes [ ] N/A [ ]
MF28	Short circuit bit (12.9)	33.5.1.2.7	Bit indicates a short circuit condition has been detected. Set to one entering ERROR_DELAY state due to the short_detected variable being TRUE.	MAN:M	Yes [ ] N/A [ ]
MF29	Short circuit bit implementation	33.5.1.2.7	Implemented with a latching high behavior as defined in 33.5.1.	MAN:M	Yes [ ] N/A [ ]
MF30	Overload bit (12.8)	33.5.1.2.8	Bit indicates an overload condition has been detected. Set to one when entering the ERROR_DELAY state due to the ovld_detected variable being TRUE.	MAN:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MF31	Overload bit implementation	33.5.1.2.8	Implemented with a latching high behavior as defined in 33.5.1.	MAN:M	Yes [ ] N/A [ ]
MF32	MPS absent bit (12.7)	33.5.1.2.9	Bit indicates an MPS Absent condition has been detected. Set to one when transitions directly from POWER_ON to IDLE state when MPS is absent for a duration greater than T_{MPDO} as specified in 33.2.9.	MAN:M	Yes [ ] N/A [ ]
MF33	MPS Absent bit implementation	33.5.1.2.9	Implemented with a latching high behavior as defined in 33.5.1.	MAN:M	Yes [ ] N/A [ ]

33.8.3.8 Data Link Layer classification requirements

Item	Feature	Subclause	Value/Comment	Status	Support
DLL1	Reserved fields	33.6	Reserved fields in Power via MDI TLV transmitted as zeroes and ignored upon receipt	M	Yes [ ] N/A [ ]
DLL2	Data Link Layer classification standards compliance	33.6.1	Meet mandatory parts of IEEE Std 802.1AB-2009	DLLC:M	Yes [ ] N/A [ ]
DLL3	TLV frame definitions	33.6.1	Meet requirements for Type, Length, and Value (TLV) defined in 79.3.2	DLLC:M	Yes [ ] N/A [ ]
DLL4	Control state diagrams	33.6.1	Meet state diagrams defined in 33.6.3	DLLC:M	Yes [ ] N/A [ ]
DLL5	Type 2 PSE LLDPDU	33.6.2	Transmitted within 10 seconds of Data Link Layer classification being enabled as indicated by pse_dll_enabled	DLLC:M	Yes [ ] N/A [ ]
DLL6	Type 1 PSE LLDPDU	33.6.2	Transmitted when Data Link Layer classification is ready as indicated by pse_dll_ready	DLLC:M	Yes [ ] N/A [ ]
DLL7	PD Data Link Layer classification ready	33.6.2	Set state variable pd_dll_ready within 5 min of Data Link Layer classification being enabled as indicated by pd_dll_enabled	DLLC:M	Yes [ ] N/A [ ]
DLL8	PD requested power value change	33.6.2	LLDPDU with updated “PSE allocated power value” sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DLL9	PSE allocated power value change	33.6.2	LLDPDU with updated “PD requested power value” sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL10	PSE power control state diagrams	33.6.3	Meet the behavior shown in Figure 33–27	DLLC:M	Yes [ ] N/A [ ]
DLL11	PD power control state diagrams	33.6.3	Meet the behavior shown in Figure 33–28	DLLC:M	Yes [ ] N/A [ ]

33.8.3.9 Environmental specifications applicable to PSEs and PDs

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Safety	33.7.1	Conforms to J.2	M	Yes [ ]
ES2	Safety	33.7.1	Comply with all applicable local and national codes	M	Yes [ ]
ES3	Telephony voltages	33.7.5	Application thereof described in 33.7.5 not result in any safety hazard	M	Yes [ ]
ES4	Limitation of electromagnetic interference	33.7.6	PD and PSE powered cabling comply with applicable local and national codes	M	Yes [ ]

33.8.3.10 Environmental specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEES1	Safety	33.7.1	Limited Power Source in accordance with Annex Q of IEC 62368-1:2018, as applicable	M	Yes [ ]

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34. Introduction to 1000 Mb/s baseband networks

34.1 Overview

Gigabit Ethernet couples an extended version of Ethernet to a family of 1000 Mb/s Physical Layers. The relationships among Gigabit Ethernet, the extended Ethernet, and the ISO/IEC Open System Interconnection (OSI) reference model are shown in Figure 34–1.

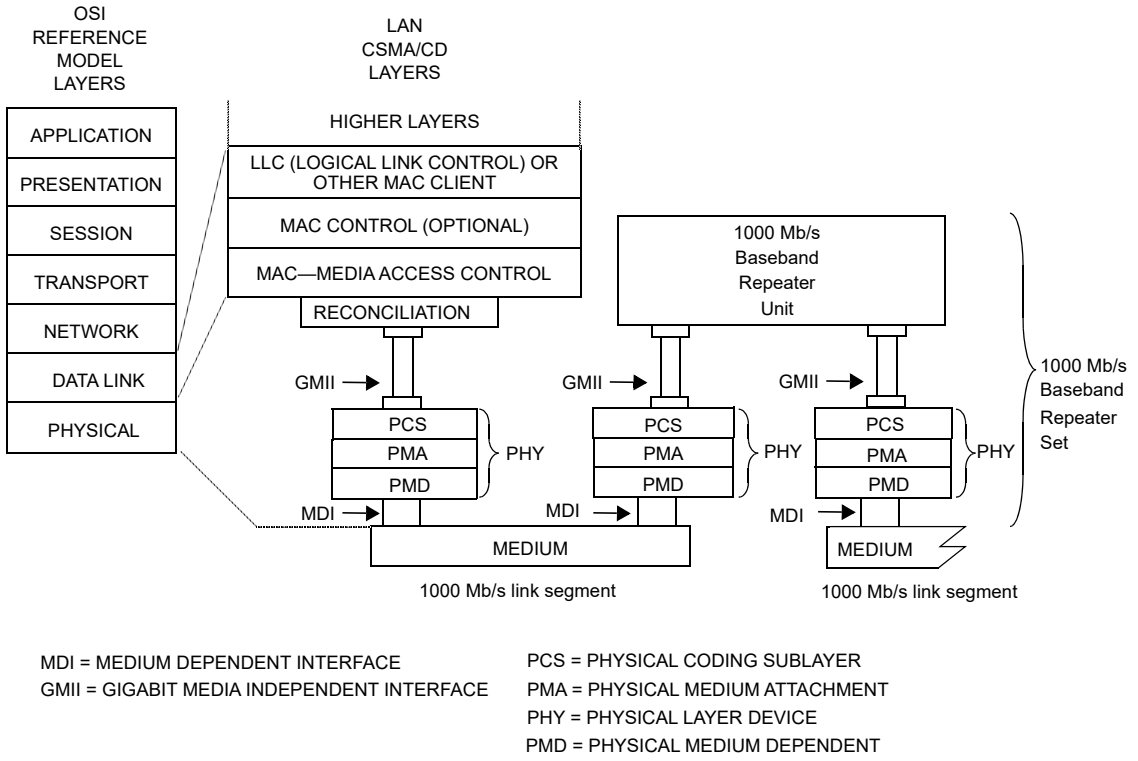

Figure 34–1—Architectural positioning of Gigabit Ethernet (1000 Mb/s operation)

The Gigabit Ethernet MAC layer interface connects through a Gigabit Media Independent Interface layer to Physical Layer entities (PHY sublayers). The set of PHY sublayer specifications include operation over multiple media (e.g., copper cables, fiber optic cables and backplanes).

Gigabit Ethernet extends the Ethernet MAC beyond 100 Mb/s to 1000 Mb/s. The bit rate is faster, and the bit times are shorter—both in proportion to the change in bandwidth. In full duplex mode, the minimum packet transmission time has been reduced by a factor of ten. Achievable topologies for 1000 Mb/s full duplex operation are comparable to those found in 100BASE-T full duplex mode. In half duplex mode, the minimum packet transmission time has been reduced, but not by a factor of ten. Cable delay budgets are similar to those in 100BASE-T. The resulting achievable topologies for the half duplex 1000 Mb/s CSMA/CD MAC are similar to those found in half duplex 100BASE-T.

34.1.1 Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)

The Gigabit Media Independent Interface (Clause 35) provides an interconnection between the Media Access Control (MAC) sublayer and Physical Layer device (PHY) and between PHY Layer and Station

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Management (STA) entities. This GMII supports 1000 Mb/s operation through its eight bit wide (octet wide) transmit and receive paths. The Reconciliation sublayer provides a mapping between the signals provided at the GMII and the MAC/PLS service definition.

34.1.2 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. The generic term 1000 Mb/s MAC refers to any use of the 1000 Mb/s IEEE 802.3 MAC (the Gigabit Ethernet MAC) coupled with any Physical Layer implementation.

Various clauses of this standard comprise a family of Physical Layer implementations for operation at 1000 Mb/s. Each PHY type includes specifications for encoding and decoding of information, and how those encoded data are transmitted on the supported transmission medium or media. These PHY types may share some PHY sublayer components and signaling methods, or may use signaling methods specific to the supported media and applications.

34.1.3 Repeater

A repeater set (Clause 41) is an integral part of any half duplex Gigabit Ethernet network with more than two DTEs in a collision domain. A repeater set extends the physical system topology by coupling two or more segments. Only one repeater is permitted within a single collision domain. Some Gigabit Ethernet PHY types only support full duplex operation. Topologies composed of full duplex only devices do not allow repeaters.

34.1.4 Auto-Negotiation, type 1000BASE-X

Auto-Negotiation (Clause 37) provides a 1000BASE-X device with the capability to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of a special sequence of link codewords. Clause 37 adopts the basic architecture and algorithms from Clause 28, but not the use of fast link pulses. Auto-Negotiation for 1000BASE-KX is defined in Clause 73.

34.1.5 Auto-Negotiation, type 1000BASE-T

Auto-Negotiation (Clause 28) is used by 1000BASE-T devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of a special sequence of fast link pulses.

34.1.6 Auto-Negotiation, type 1000BASE-T1

Auto-Negotiation (Clause 98) may be used by 1000BASE-T1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding.

The use of Clause 98 Auto-Negotiation is optional for a 1000BASE-T1 PHY.

34.1.7 Management

Managed objects, attributes, and actions are defined for all Gigabit Ethernet components (Clause 30).

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34.2 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

34.3 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE 802.3, Clause 35 through Clause 41, shall complete a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the Gigabit Ethernet PICS conforms to the same notation and conventions used in 100BASE-T (see 21.6).

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35. Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)

35.1 Overview

This clause defines the logical and electrical characteristics for the Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII) between CSMA/CD media access controllers and various PHYs. Figure 35–1 shows the relationship of the Reconciliation sublayer and GMII to the ISO/IEC OSI reference model.

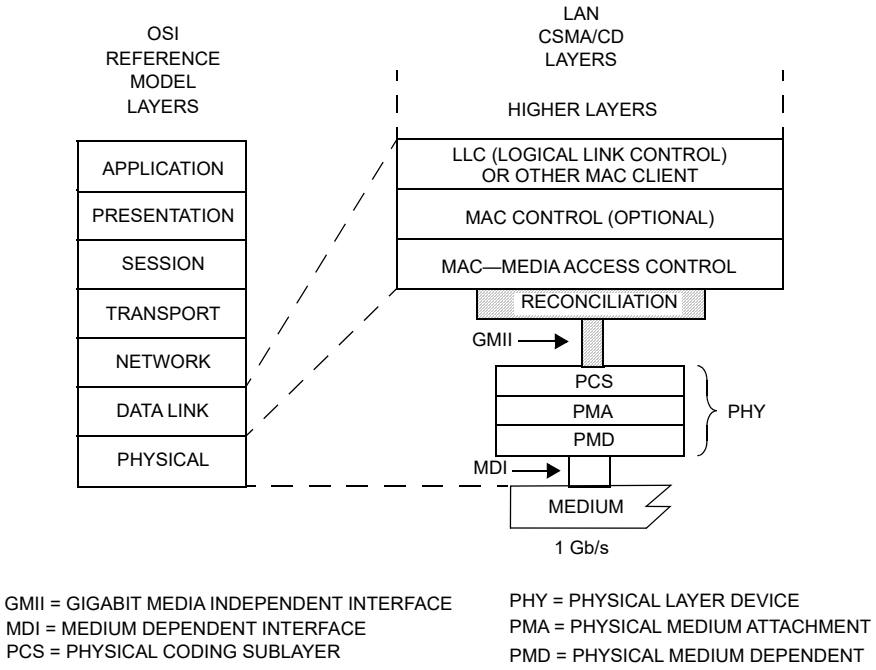

Figure 35–1—GMII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

The purpose of this interface is to provide a simple, inexpensive, and easy-to-implement interconnection between Media Access Control (MAC) sublayer and PHYs, and between PHYs and Station Management (STA) entities.

This interface has the following characteristics:

a) It is capable of supporting 1000 Mb/s operation.
b) Data and delimiters are synchronous to clock references.
c) It provides independent eight-bit-wide transmit and receive data paths.
d) It provides a simple management interface.
e) It uses signal levels, compatible with common CMOS digital ASIC processes and some bipolar processes.
f) It provides for full duplex operation.

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35.1.1 Summary of major concepts

a) The GMII is based on the MII defined in Clause 22.
b) Each direction of data transfer is serviced by Data (an eight-bit bundle), Delimiter, Error, and Clock signals.
c) Two media status signals are provided. One indicates the presence of carrier, and the other indicates the occurrence of a collision.
d) The GMII uses the MII management interface composed of two signals that provide access to management parameters and services as specified in Clause 22.
e) MII signal names have been retained and the functions of most signals are the same, but additional valid combinations of signals have been defined for 1000 Mb/s operation.
f) The Reconciliation sublayer maps the signal set provided at the GMII to the PLS service primitives provided to the MAC.
g) GMII signals are defined such that an implementation may multiplex most GMII signals with the similar PMA service interface defined in Clause 36 and Clause 97.
h) The GMII may also support Low Power Idle (LPI) signaling as defined for Energy-Efficient Ethernet in Clause 78 for certain PHY types.

35.1.2 Application

This clause applies to the interface between the MAC and PHYs, and between PHYs and Station Management entities. The implementation of the interface is primarily intended as a chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board. A motherboard-to-daughterboard interface between two or more printed circuit boards is not precluded. The use of parts of the GMII (e.g., data paths, but not the Clause 22 management interface or associated management registers), and the use of the GMII as an interface between logic modules on the same chip is not precluded.

This interface is used to provide media independence so that an identical media access controller may be used with any of the copper and optical PHY types.

35.1.3 Rate of operation

The GMII supports only 1000 Mb/s operation and is defined within this clause. Operation at 10 Mb/s and 100 Mb/s is supported by the MII defined in Clause 22.

PHYs that provide a GMII shall support 1000 Mb/s operation, and may support additional rates using other interfaces (e.g., MII). PHYs have to report the rates at which they are capable of operating via the management interface. Reconciliation sublayers that provide a GMII shall support 1000 Mb/s and may support additional rates using other interfaces.

35.1.4 Allocation of functions

The allocation of functions at the GMII balances the need for media independence with the need for a simple and cost-effective interface.

While the Attachment Unit Interface (AUI) was defined to exist between the Physical Signaling (PLS) and Physical Medium Attachment (PMA) sublayers for 10 Mb/s DTEs, the GMII (like the Clause 22 MII) maximizes media independence by cleanly separating the Data Link and Physical Layers of the ISO/IEC seven-layer reference model. This allocation also recognizes that implementations can benefit from a close coupling between the PLS or PCS sublayer and the PMA sublayer.

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35.2 Functional specifications

The GMII is designed to make the differences among the various media transparent to the MAC sublayer. The selection of logical control signals and the functional procedures are all designed to this end.

35.2.1 Mapping of GMII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the GMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the Reconciliation sublayer, and described here, behave in exactly the same manner as defined in Clause 6. The mapping is changed for EEE capability (see 78.3), as described in 35.4.

An LPI_IDLE.request primitive with value ASSERT shall not be generated unless the attached link is operational (i.e., link_status = OK, according to the underlying PCS/PMA). The PHY shall not cause an LP_IDLE.request primitive with value ASSERT to be generated for at least one second following a link_status change to OK (see 78.1.2.1.2).

EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

Figure 35–2 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the GMII management interface is controlled by the Station Management entity (STA).

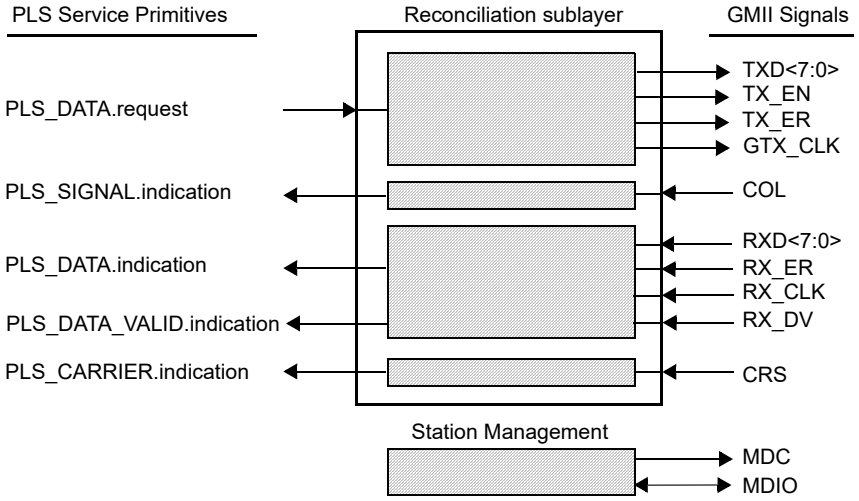

Figure 35–2—Reconciliation Sublayer (RS) inputs and outputs and STA connections to GMII

35.2.1.1 Mapping of PLS_DATA.request

35.2.1.1.1 Function

Map the primitive PLS_DATA.request to the GMII signals TXD<7:0>, TX_EN, TX_ER, and GTX_CLK.

35.2.1.1.2 Semantics of the service primitive

PLS_DATA.request (OUTPUT_UNIT)

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The OUTPUT_UNIT parameter can take one of five values: ONE, ZERO, DATA_COMPLETE, EXTEND, or EXTEND_ERROR. It represents or is equivalent to a single data bit. These values are conveyed by the signals TX_EN, TX_ER, TXD<7>, TXD<6>, TXD<5>, TXD<4>, TXD<3>, TXD<2>, TXD<1>, and TXD<0>.

Each of the eight TXD signals conveys either a ONE or ZERO of data while TX_EN is asserted. Eight data bit equivalents of EXTEND or EXTEND_ERROR are conveyed by a specific encoding of the TXD<7:0> signals when TX_EN is not asserted, and TX_ER is asserted, see Table 35–1. Synchronization between the Reconciliation sublayer and the PHY is achieved by way of the GTX_CLK signal. The value DATA_COMPLETE is conveyed by the deassertion of either TX_EN or TX_ER at the end of a MAC's transmission.

35.2.1.1.3 When generated

The GTX_CLK signal is generated by the Reconciliation sublayer. The TXD<7:0>, TX_EN and TX_ER signals are generated by the Reconciliation sublayer after every group of eight PLS_DATA.request transactions from the MAC sublayer to request the transmission of eight data bits on the physical medium, to extend the carrier event the equivalent of eight bits, or to stop transmission.

35.2.1.2 Mapping of PLS_DATA.indication

35.2.1.2.1 Function

Map the primitive PLS_DATA.indication to the GMII signals RXD<7:0>, RX_DV, RX_ER, and RX_CLK.

35.2.1.2.2 Semantics of the service primitive

PLS_DATA.indication (INPUT_UNIT)

The INPUT_UNIT parameter can take one of three values: ONE, ZERO or EXTEND. It represents or is equivalent to a single data bit. These values are derived from the signals RX_DV, RX_ER, RXD<7>, RXD<6>, RXD<5>, RXD<4>, RXD<3>, RXD<2>, RXD<1>, and RXD<0>. The value of the data transferred to the MAC is controlled by GMII error indications, see 35.2.1.5.

Each of the eight RXD signals conveys either a ONE or ZERO of data while RX_DV is asserted. Eight data bit equivalents of EXTEND are conveyed by a specific encoding of the RXD<7:0> signals when RX_DV is not asserted, and RX_ER is asserted; see Table 35–2. Synchronization between the Reconciliation sublayer and the PHY is achieved by way of the RX_CLK signal.

35.2.1.2.3 When generated

This primitive is generated to all MAC sublayer entities in the network after a PLS_DATA.request is issued. Each octet transferred on RXD<7:0> will result in the generation of eight PLS_DATA.indication transactions.

35.2.1.3 Mapping of PLS_CARRIER.indication

35.2.1.3.1 Function

Map the primitive PLS_CARRIER.indication to the GMII signal CRS.

35.2.1.3.2 Semantics of the service primitive

PLS_CARRIER.indication (CARRIER_STATUS)

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The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. CARRIER_STATUS assumes the value CARRIER_ON when the GMII signal CRS is asserted and assumes the value CARRIER_OFF when CRS is deasserted.

35.2.1.3.3 When generated

The PLS_CARRIER.indication service primitive is generated by the Reconciliation sublayer whenever the CARRIER_STATUS parameter changes from CARRIER_ON to CARRIER_OFF or vice versa.

35.2.1.4 Mapping of PLS_SIGNAL.indication

35.2.1.4.1 Function

Map the primitive PLS_SIGNAL.indication to the GMII signal COL.

35.2.1.4.2 Semantics of the service primitive

PLS_SIGNAL.indication (SIGNAL_STATUS)

The SIGNAL_STATUS parameter can take one of two values: SIGNAL_ERROR or NO_SIGNAL_ERROR. SIGNAL_STATUS assumes the value SIGNAL_ERROR when the GMII signal COL is asserted, and assumes the value NO_SIGNAL_ERROR when COL is deasserted.

35.2.1.4.3 When generated

The PLS_SIGNAL.indication service primitive is generated whenever SIGNAL_STATUS makes a transition from SIGNAL_ERROR to NO_SIGNAL_ERROR or vice versa.

35.2.1.5 Response to error indications from GMII

If, during frame reception, both RX_DV and RX_ER are asserted, the Reconciliation sublayer shall ensure that the MAC will detect a FrameCheckError in that frame.

Carrier is extended when RX_DV is not asserted and RX_ER is asserted with a proper encoding of RXD<7:0>. When a Carrier Extend Error is received during the extension, the Reconciliation sublayer shall send PLS_DATA.indication values of ONE or ZERO and ensure that the MAC will detect a FrameCheckError in the sequence.

These requirements may be met by incorporating a function in the Reconciliation sublayer that produces a received frame data sequence delivered to the MAC sublayer that is guaranteed to not yield a valid CRC result, as specified by the algorithm in 3.2.9. This data sequence may be produced by substituting data delivered to the MAC.

Other techniques may be employed to respond to Data Reception Error or Carrier Extend Error provided that the result is that the MAC sublayer behaves as though a FrameCheckError occurred in the received frame.

35.2.1.6 Conditions for generation of TX_ER

If, during the process of transmitting a frame, it is necessary to request that the PHY deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability, then Transmit Error Propagation shall be asserted by the appropriate encoding of TX_ER, and TX_EN. Similarly, if during the process of transmitting carrier extension to a frame, it is necessary to request that the PHY deliberately corrupt the contents of the carrier extension in such a manner that a receiver will detect

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the corruption with the highest degree of probability, then Carrier Extend Error shall be signaled by the appropriate encoding of TXD<7:0>.

This capability has additional use within a repeater. For example, a repeater that detects an RX_ER during frame reception on an input port may propagate that error indication to its output ports by asserting TX_ER during the process of transmitting that frame.

35.2.1.7 Mapping of PLS_DATA_VALID.indication

35.2.1.7.1 Function

Map the primitive PLS_DATA_VALID.indication to the GMII signals RX_DV, RX_ER, and RXD<7:0>.

35.2.1.7.2 Semantics of the service primitive

PLS_DATA_VALID.indication (DATA_VALID_STATUS)

The DATA_VALID_STATUS parameter can take one of two values: DATA_VALID or DATA_NOT_VALID. DATA_VALID_STATUS assumes the value DATA_VALID when the GMII signal RX_DV is asserted, or when RX_DV is not asserted, RX_ER is asserted and the values of RXD<7:0> indicate Carrier Extend or Carrier Extend Error. DATA_VALID_STATUS assumes the value DATA_NOT_VALID at all other times.

35.2.1.7.3 When generated

The PLS_DATA_VALID.indication service primitive is generated by the Reconciliation sublayer whenever DATA_VALID_STATUS parameter changes from DATA_VALID to DATA_NOT_VALID or vice versa.

35.2.2 GMII signal functional specifications

35.2.2.1 GTX_CLK (1000 Mb/s transmit clock)

GTX_CLK is a continuous clock used for operation at 1000 Mb/s. GTX_CLK provides the timing reference for the transfer of the TX_EN, TX_ER, and TXD signals from the Reconciliation sublayer to the PHY. The values of TX_EN, TX_ER, and TXD are sampled by the PHY on the rising edge of GTX_CLK. GTX_CLK is sourced by the Reconciliation sublayer.

The GTX_CLK frequency is nominally 125 MHz, one-eighth of the transmit data rate.

NOTE—For EEE capability, GTX_CLK may be halted according to 35.2.2.6.

35.2.2.2 RX_CLK (receive clock)

RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV, RX_ER and RXD signals from the PHY to the Reconciliation sublayer. RX_DV, RX_ER and RXD are sampled by the Reconciliation sublayer on the rising edge of RX_CLK. RX_CLK is sourced by the PHY.

The frequency of RX_CLK may be derived from the received data or it may be that of a nominal clock (e.g., GTX_CLK). When the received data rate at the PHY is within tolerance, the RX_CLK frequency shall be 125MHz ±0.01%, one-eighth of the MAC receive data rate.

There is no need to transition between the recovered clock reference and a nominal clock reference on a frame-by-frame basis. If loss of received signal from the medium causes a PHY to lose the recovered RX_CLK reference, the PHY shall source the RX_CLK from a nominal clock reference. Transitions from nominal clock to recovered clock or from recovered clock to nominal clock shall not decrease the period, or time between

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adjacent edges, of RX_CLK below the limits specified in Table 35–8, and shall not increase the time between adjacent edges of RX_CLK more than twice the nominal clock period.

Transitions from local clock to recovered clock or from recovered clock to local clock shall be made only while RX_DV and RX_ER are deasserted. During the interval between the assertion of CRS and the assertion of RX_DV at the beginning of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition until the PHY has successfully locked onto the recovered clock. Following the deassertion of RX_DV at the end of a frame, or the deassertion of RX_ER at the end of carrier extension, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition for an interval that shall not exceed twice the nominal clock period.

NOTE 1—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and GTX_CLK signals. See additional information in 35.5.

NOTE 2—For EEE capability, RX_CLK may be halted during periods of low utilization according to 35.2.2.10.

35.2.2.3 TX_EN (transmit enable)

TX_EN in combination with TX_ER indicates the Reconciliation sublayer is presenting data on the GMII for transmission. It shall be asserted by the Reconciliation sublayer synchronously with the first octet of the preamble and shall remain asserted while all octets to be transmitted are presented to the GMII. TX_EN shall be negated prior to the first rising edge of GTX_CLK following the final data octet of a frame. TX_EN is driven by the Reconciliation sublayer and shall transition synchronously with respect to the GTX_CLK.

Figure 35–3 depicts TX_EN behavior during a frame transmission with no collisions and without carrier extension or errors.

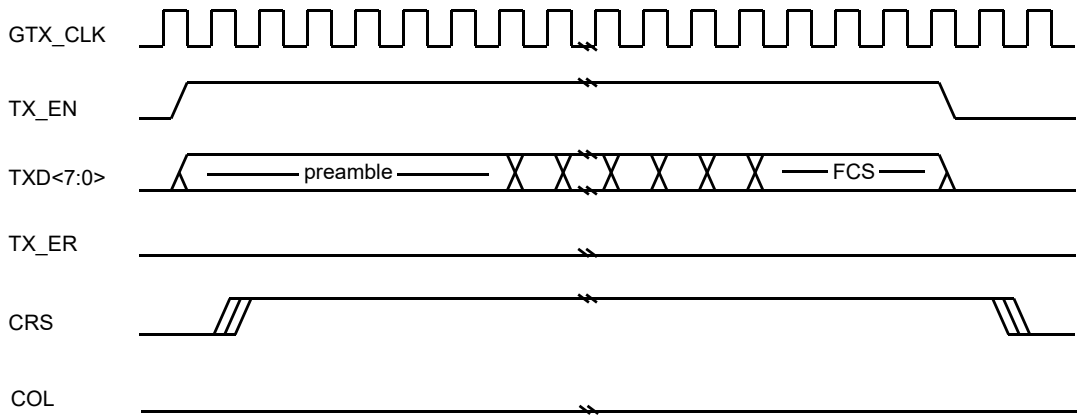

Figure 35–3—Basic frame transmission

35.2.2.4 TXD (transmit data)

TXD is a bundle of eight data signals (TXD<7:0>) that are driven by the Reconciliation sublayer. TXD<7:0> shall transition synchronously with respect to the GTX_CLK. For each GTX_CLK period in which TX_EN is asserted and TX_ER is deasserted, data are presented on TXD<7:0> to the PHY for transmission. TXD<0> is the least significant bit. While TX_EN and TX_ER are both deasserted, TXD<7:0> shall have no effect upon the PHY.

While TX_EN is deasserted and TX_ER is asserted, TXD<7:0> are used to request the PHY to generate LPI, Carrier Extend, or Carrier Extend Error code-groups. The use of TXD<7:0> during the transmission of a frame

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with carrier extension is described in 35.2.2.5. Carrier extension shall only be signaled immediately following the data portion of a frame. The use of TXD<7:0> to signal LPI transitions is described in 35.2.2.6.

For EEE capability, the RS shall use the combination of TX_EN deasserted, TX_ER asserted, and TXD<7:0> equal to 0x01 as shown in Table 35–1 as a request to enter, or remain in the LPI state. Transition into and out of the LPI state is shown in Figure 35–8.

Table 35–1 specifies the permissible encodings of TXD<7:0>, TX_EN, and TX_ER.

Table 35–1—Permissible encodings of TXD<7:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<7:0>	Description	PLS_DATA.request parameter
0	0	00 through FF	Normal inter-frame	DATA_COMPLETE
0	1	00	Reserved	—
0	1	01	Assert LPI	—
0	1	02 through 0E	Reserved	—
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	1	00 through FF	Transmit error propagation	No applicable parameter
NOTE—Values in TXD<7:0> column are in hexadecimal.				

35.2.2.5 TX_ER (transmit coding error)

TX_ER is driven by the Reconciliation Sublayer and shall transition synchronously with respect to the GTX_CLK. When TX_ER is asserted for one or more TX_CLK periods while TX_EN is also asserted, the PHY shall emit one or more code-groups that are not part of the valid data or delimiter set somewhere in the frame being transmitted. The relative position of the error within the frame need not be preserved. Figure 35–4 shows the behavior of TX_ER during the transmission of a frame propagating an error.

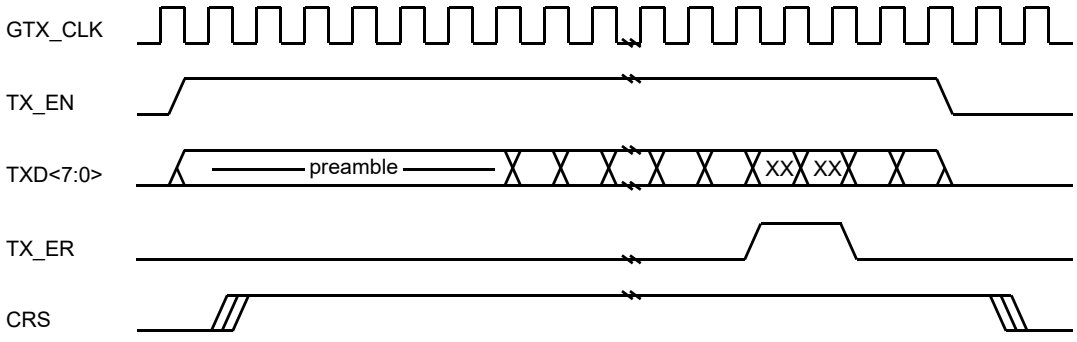

Figure 35–4—Propagating an error within a frame

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Assertion of appropriate TXD values when TX_EN is deasserted and TX_ER is asserted will cause the PHY to generate either Carrier Extend or Carrier Extend Error code-groups. The transition from TX_EN asserted and TX_ER deasserted to TX_EN deasserted and TX_ER asserted with TXD specifying Carrier Extend shall result in the PHY transmitting an end-of-packet delimiter as the initial code-groups of the carrier extension. Figure 35–5 and Figure 35–6 show the behavior of TX_ER during the transmission of carrier extension. The propagation of an error in carrier extension is requested by holding TX_EN deasserted and TX_ER asserted along with the appropriate value of TXD<7:0>.

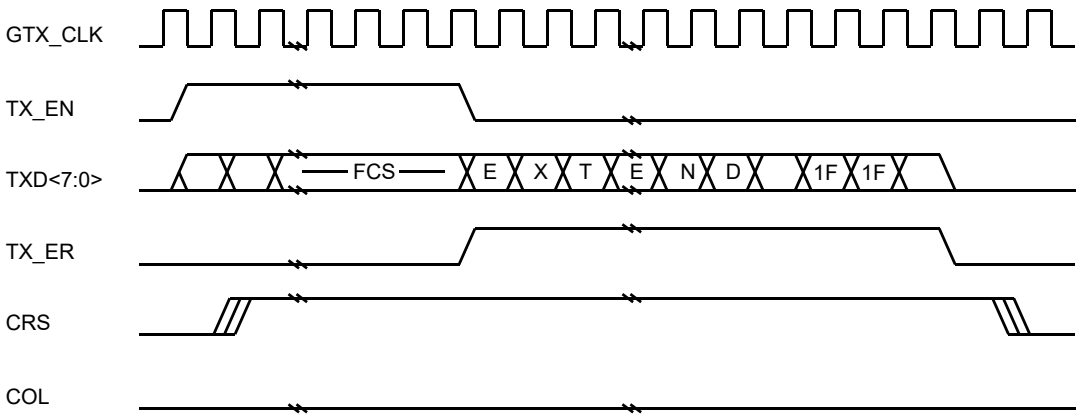

Figure 35–5—Propagating an error within carrier extension

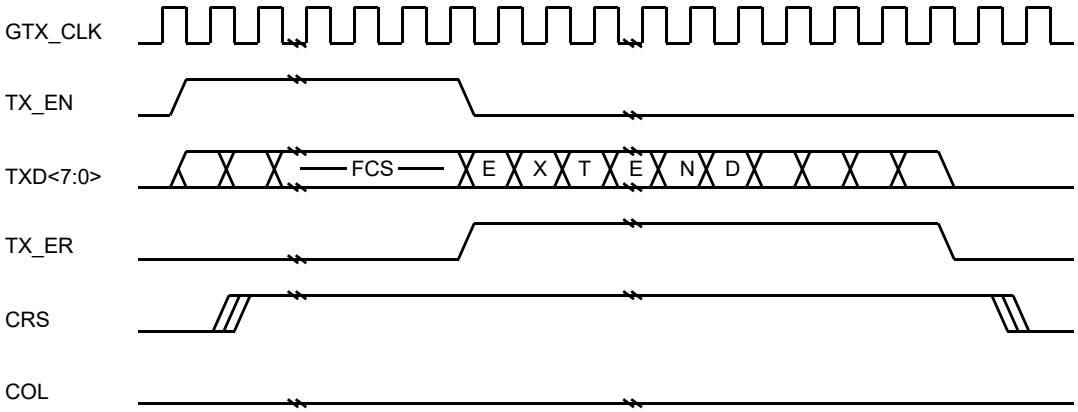

Figure 35–6—Transmission with carrier extension

Burst transmission of frames also uses carrier extension between frames of the burst. Figure 35–7 shows the behavior of TX_ER and TX_EN during burst transmission.

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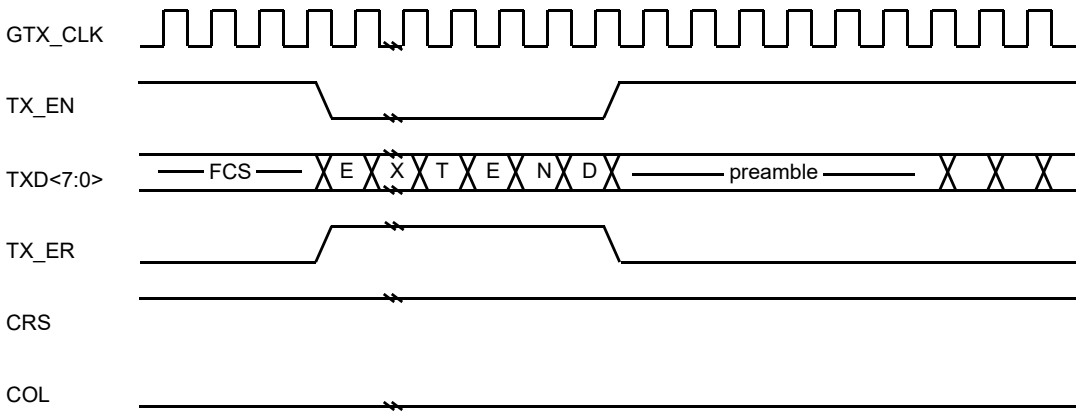

Figure 35–7—Burst transmission

35.2.2.6 Transmit direction LPI transition

EEE capability and the LPI client are described in 78.1. The LPI client requests the PHY to transition to its low power state by asserting TX_ER and setting TXD<7:0> to 0x01. The LPI client maintains the same state for these signals for the entire time that the PHY is to remain in the low power state.

The LPI client may halt GTX_CLK at any time more than 9 clock cycles after the start of the LPI state as shown in Figure 35–8 if and only if the Clock stop capable bit is asserted (45.2.3.1.4).

The LPI client requests the PHY to transition out of its low power state by deasserting TX_ER and TXD. The LPI client should not assert TX_EN for valid transmit data until after the wake-up time specified for the PHY.

Figure 35–8 shows the behavior of TX_EN, TX_ER and TXD<7:0> during the transition into and out of the LPI state.

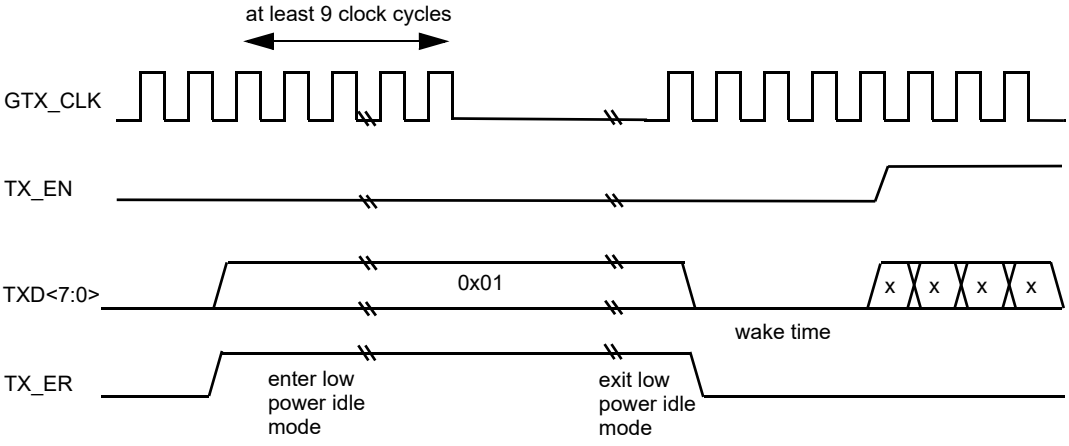

Figure 35–8—LPI transition

Table 35–1 summarizes the permissible encodings of TXD<7:0>, TX_EN, and TX_ER.

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35.2.2.7 RX_DV (receive data valid)

RX_DV is driven by the PHY to indicate that the PHY is presenting recovered and decoded data on the RXD<7:0> bundle. RX_DV shall transition synchronously with respect to the RX_CLK. RX_DV shall be asserted continuously from the first recovered octet of the frame through the final recovered octet and shall be negated prior to the first rising edge of RX_CLK that follows the final octet. In order for a received frame to be correctly interpreted by the Reconciliation sublayer and the MAC sublayer, RX_DV has to encompass the frame, starting no later than the Start Frame Delimiter (SFD) and excluding any End-of-Frame delimiter.

Figure 35–9 shows the behavior of RX_DV during frame reception with no errors or carrier extension.

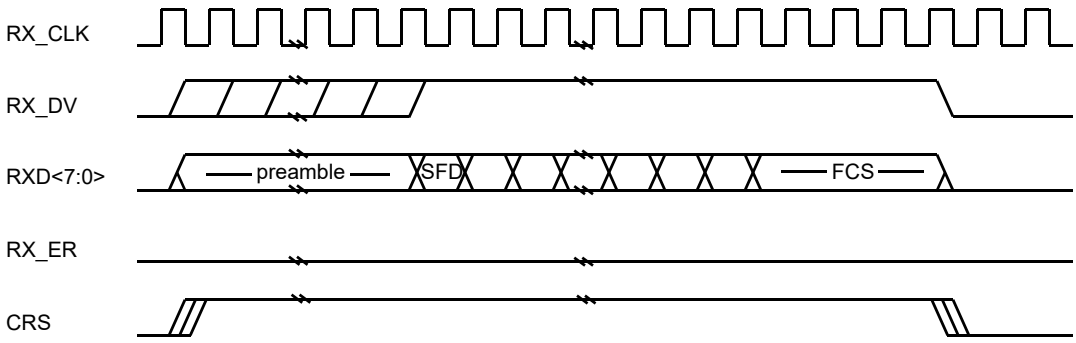

Figure 35–9—Basic frame reception

35.2.2.8 RXD (receive data)

RXD is a bundle of eight data signals (RXD<7:0>) that are driven by the PHY. RXD<7:0> shall transition synchronously with respect to RX_CLK. For each RX_CLK period in which RX_DV is asserted, RXD<7:0> transfer eight bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the least significant bit. Figure 35–9 shows the behavior of RXD<7:0> during frame reception.

While RX_DV is deasserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal while driving the specific value listed in Table 35–2 onto RXD<7:0>. See 36.2.5.2.3 for a description of the conditions under which a PHY will provide a False Carrier indication. LPI transitions are described in 35.2.2.10.

While RX_DV is deasserted, the PHY may indicate that it is receiving LPI by asserting the RX_ER signal while driving the value 0x01 onto RXD<7:0>.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD has to be passed across the GMII.

In a DTE operating in half duplex mode, a PHY is not required to loop data transmitted on TXD<7:0> back to RXD<7:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2. In a DTE operating in full duplex mode, data transmitted on TXD <7:0> shall not be looped back to RXD <7:0> unless the loopback mode of operation is selected.

While RX_DV is deasserted and RX_ER is asserted, a specific RXD<7:0> value is used to transfer recovered Carrier Extend from the PHY to the Reconciliation sublayer. A Carrier Extend Error is indicated by another specific value of RXD<7:0>. Figure 35–10 shows the behavior of RX_DV during frame reception with carrier extension. Carrier extension shall only be signaled immediately following frame reception.

Burst transmission of frames also uses carrier extension between frames of the burst. Figure 35–11 shows the behavior of RX_ER and RX_DV during burst reception.

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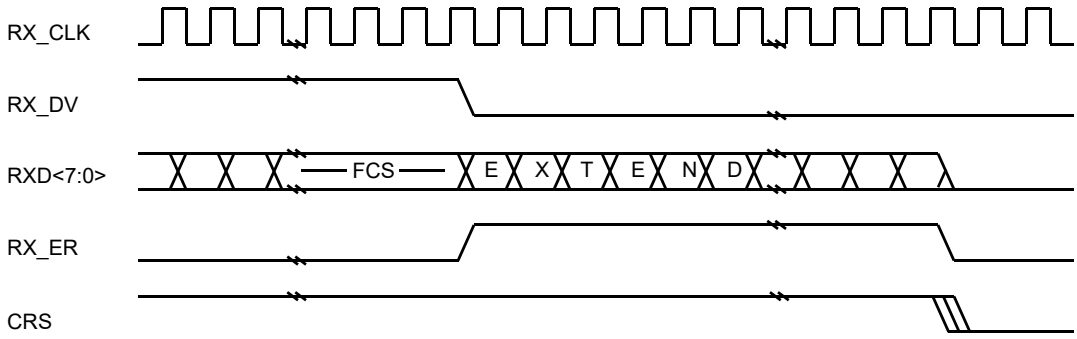

Figure 35–10—Frame reception with carrier extension

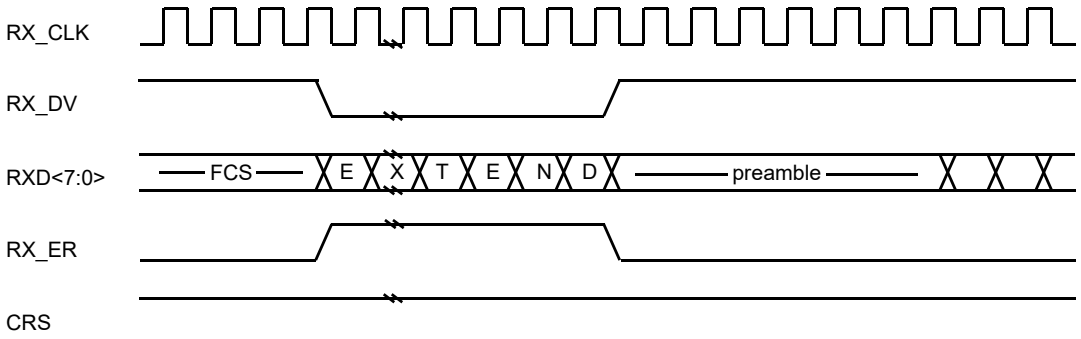

Figure 35–11—Burst reception

Table 35–2 specifies the permissible encoding of RXD<7:0>, RX_ER, and RX_DV, along with the specific indication that shall be interpreted by the RS.

Table 35–2—Permissible encoding of RXD<7:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<7:0>	Description	PLS_DATA.indication parameter
0	0	00 through FF	Normal inter-frame	No applicable parameter
0	1	00	Normal inter-frame	No applicable parameter

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Table 35–2—Permissible encoding of RXD<7:0>, RX_ER, and RX_DV *(continued)*

RX_DV	RX_ER	RXD<7:0>	Description	PLS_DATA.indication parameter
0	1	01	Assert LPI	No applicable parameter
0	1	02 through 0D	Reserved	—
0	1	0E	False Carrier indication	No applicable parameter
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1	1	00 through FF	Data reception error	ZERO, ONE (eight bits)
NOTE—Values in RXD<7:0> column are in hexadecimal.				

35.2.2.9 RX_ER (receive error)

RX_ER is driven by the PHY and shall transition synchronously with respect to RX_CLK. When RX_DV is asserted, RX_ER shall be asserted for one or more RX_CLK periods to indicate to the Reconciliation sublayer that an error (e.g., a coding error, or another error that the PHY is capable of detecting that may otherwise be undetectable at the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY to the Reconciliation sublayer.

The effect of RX_ER on the Reconciliation sublayer is defined in 35.2.1.5. Figure 35–12 shows the behavior of RX_ER during the reception of a frame with errors. Two independent error cases are illustrated. When RX_DV is asserted, assertion of RX_ER indicates an error within the data octets of a frame. An error within carrier extension is indicated by driving the appropriate value on RXD<7:0> while keeping RX_ER asserted.

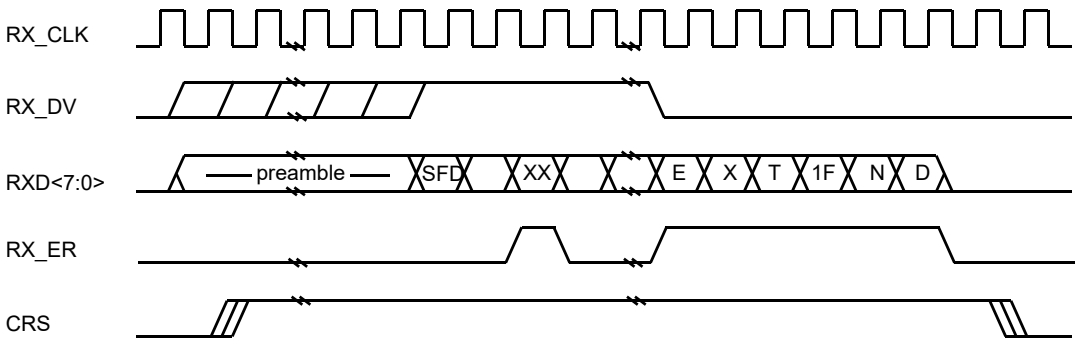

Figure 35–12—Two examples of reception with error

Assertion of RX_ER when RX_DV is deasserted with specific RXD values indicates the decode of carrier extension by the PHY. The transition from RX_DV asserted and RX_ER deasserted to RX_DV deasserted and RX_ER asserted with RXD specifying Carrier Extend shall result in the Reconciliation sublayer indicating EXTEND INPUT_UNITs to the MAC. Figure 35–10 shows the behavior of RX_DV and RX_ER during frame reception with carrier extension.

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While RX_DV is deasserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal for at least one cycle of the RX_CLK while driving the appropriate value onto RXD<7:0>, as defined in Table 35–2. See 36.2.5.2.3 for a description of the conditions under which a PHY will provide a False Carrier indication. Figure 35–13 shows the behavior of RX_ER, RX_DV and RXD<7:0> during a False Carrier indication.

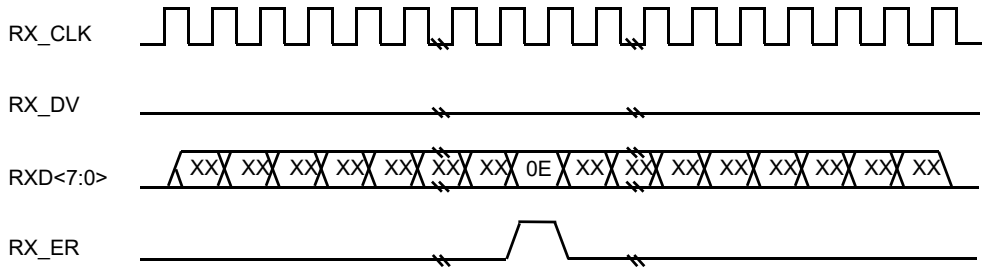

Figure 35–13—False Carrier indication

35.2.2.10 Receive direction LPI transition

EEE capability and the LPI client are described in 78.1. When the PHY receives signals from the link partner indicating LPI, it signals this to the LPI client by asserting RX_ER and setting RXD<7:0> to 0x01 while keeping RX_DV deasserted. The PHY maintains these signals in this state while it remains in the low power state. When the PHY receives signals from the link partner indicating its transition out of the low power state, it signals this to the LPI client by deasserting RX_ER and returning to normal interframe encoding.

While the PHY device is indicating LPI, the PHY device may halt the RX_CLK as shown in Figure 35–14 if and only if the Clock stop enable bit is asserted (see 45.2.3.1.4). The PHY may restart RX_CLK at any time while it is asserting LPI, but shall restart RX_CLK so that at least one positive transition occurs before it deasserts LPI.

Figure 35–14 shows the behavior of RX_ER, RX_DV, and RXD<7:0> during LPI transitions.

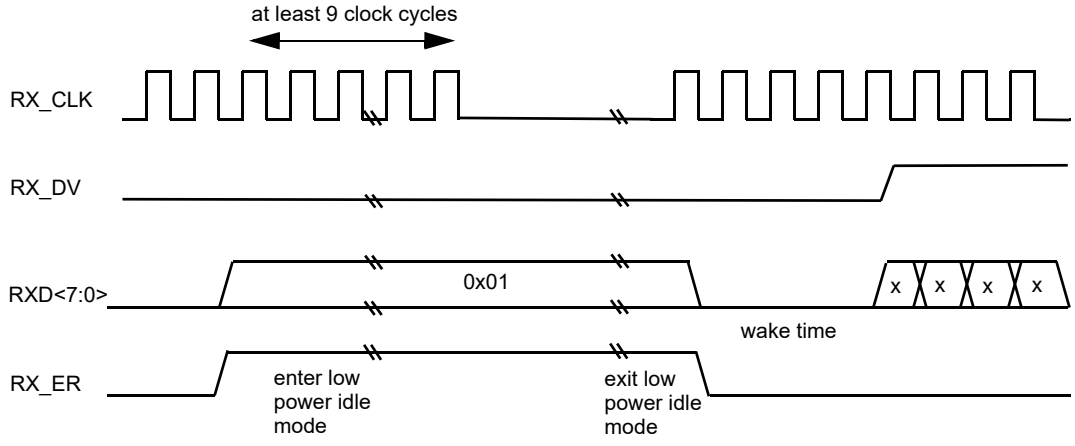

Figure 35–14—LPI transitions (receive)

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35.2.2.11 CRS (carrier sense)

CRS is driven by the PHY. Except when used in a repeater, a PHY in half duplex mode shall assert CRS when either the transmit or receive medium is non-idle and shall deassert CRS when both the transmit and receive media are idle. The PHY shall ensure that CRS remains asserted throughout the duration of a collision condition.

When used in a repeater, a PHY shall assert CRS when the receive medium is non-idle and shall deassert CRS when the receive medium is idle.

CRS is not required to transition synchronously with respect to either the GTX_CLK or the RX_CLK.

The behavior of CRS is unspecified when the PHY is in full duplex mode.

Figure 35–3 and Figure 35–5 show the behavior of CRS during a frame transmission without a collision, while Figure 35–15 and Figure 35–16 show the behavior of CRS during a frame transmission with a collision.

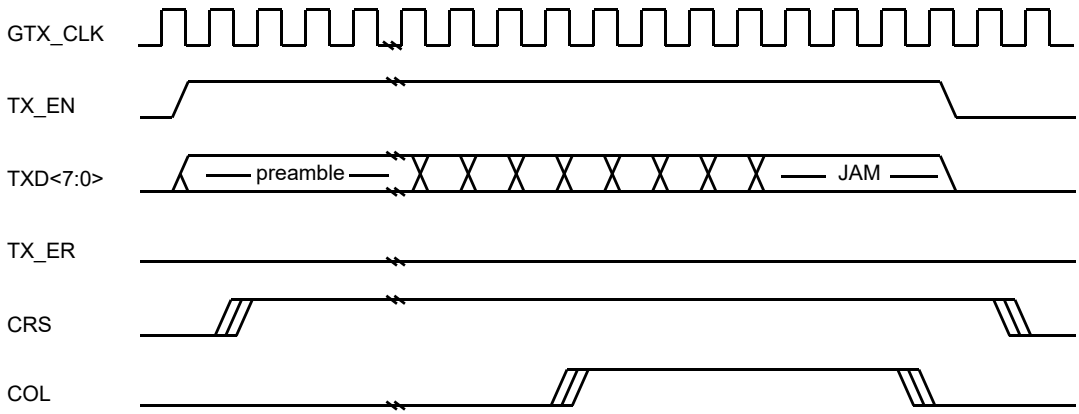

Figure 35–15—Transmission with collision

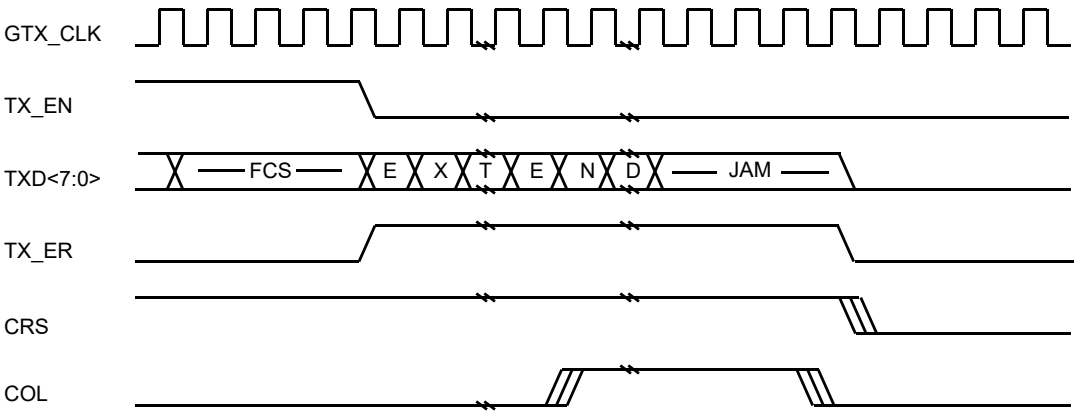

Figure 35–16—Transmission with collision in carrier extension

35.2.2.12 COL (collision detected)

COL is driven by the PHY and shall be asserted upon detection of a collision on the medium, and shall remain asserted while the collision condition persists.

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COL is not required to transition synchronously with respect to either the GTX_CLK or the RX_CLK.

The behavior of the COL signal is unspecified when the PHY is in full duplex mode.

Figure 35–15 and Figure 35–16 show the behavior of COL during a frame transmission with a collision.

35.2.2.13 MDC (management data clock)

MDC is specified in 22.2.2.13.

35.2.2.14 MDIO (management data input/output)

MDIO is specified in 22.2.2.14.

35.2.3 GMII data stream

Packets transmitted through the GMII shall be transferred within the data stream shown in Figure 35–17.

<inter-frame><preamble><sfd><data><efd><extend>

Figure 35–17—GMII data stream

For the GMII, transmission and reception of each octet of data shall be as shown in Figure 35–18.

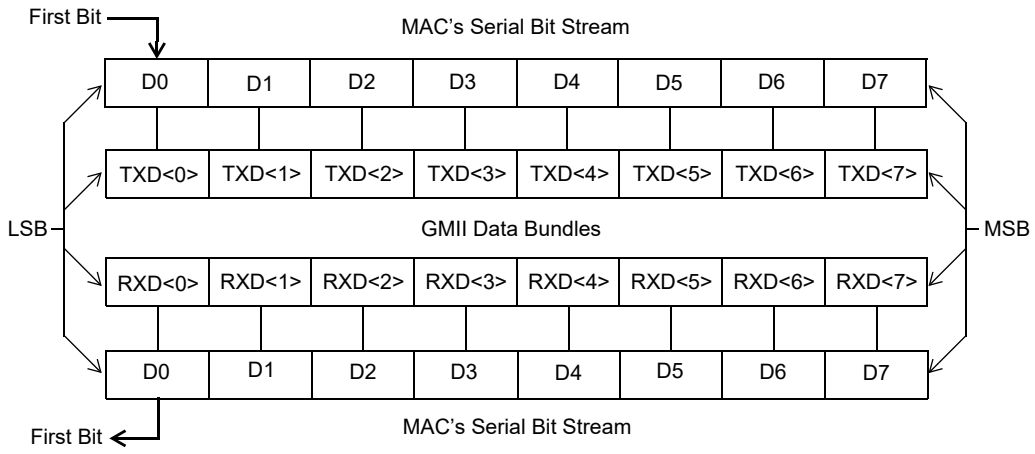

Figure 35–18—Relationship of data bundles to MAC serial bit stream

35.2.3.1 Inter-frame <inter-frame>

The inter-frame <inter-frame> period on a GMII transmit or receive path is an interval during which no data activity occurs on the path. Between bursts or single frame transmissions, the absence of data activity on the receive path is indicated by the deassertion of both RX_DV and RX_ER or the deassertion of the RX_DV signal with an RXD<7:0> value of 00 hexadecimal. On the transmit path the absence of data activity is indicated by the deassertion of both TX_EN and TX_ER.

Between frames within a burst, the inter-frame period is signaled as Carrier Extend on the GMII. As shown in Figure 35–7, this is done by asserting TX_ER with the appropriate encoding of TXD<7:0> simultaneous with

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the deassertion of TX_EN on the transmit path; and, as shown in Figure 35–11, by asserting RX_ER with the appropriate encoding of RXD<7:0> simultaneous with the deassertion of RX_DV on the receive path.

Within a burst, the MAC interFrameSpacing parameter defined in Clause 4, is measured from the deassertion of the TX_EN signal to the assertion of the TX_EN signal, and between bursts measured from the deassertion of the CRS signal to the assertion of the CRS signal.

35.2.3.2 Preamble <preamble> and start of frame delimiter <sfd>

35.2.3.2.1 Transmit case

The preamble <preamble> begins a frame transmission. The bit value of the preamble field at the GMII is unchanged from that specified in 4.2.5 and when generated by a MAC shall consist of 7 octets with the following bit values:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

The SFD (Start Frame Delimiter) <sfd> indicates the start of a frame and immediately follows the preamble. The bit value of the SFD at the GMII is unchanged from that specified in 4.2.6, and is the following bit sequence:

10101011

The preamble and SFD are shown above with their bits ordered for serial transmission from left to right. As shown, the leftmost bit of each octet is the LSB of the octet and the rightmost bit of each octet is the MSB of the octet.

The preamble and SFD shall be transmitted through the GMII as octets starting from the assertion of TX_EN.

35.2.3.2.2 Receive case

The conditions for assertion of RX_DV are defined in 35.2.2.7. The operation of 1000 Mb/s PHYs can result in shrinkage of the preamble between transmission at the source GMII and reception at the destination GMII. Table 35–3 depicts the case where no preamble bytes are conveyed across the GMII. This case may not be possible with a specific PHY, but illustrates the minimum preamble with which MAC shall be able to operate. Table 35–4 depicts the case where the entire preamble is conveyed across the GMII.

Table 35–3—Start of receive with no preamble preceding SFD

Signal	Bit values of octets received through GMII[a]			
RXD0	X	X	1[b]	D0[c]
RXD1	X	X	0	D1
RXD2	X	X	1	D2
RXD3	X	X	0	D3
RXD4	X	X	1	D4
RXD5	X	X	0	D5
RXD6	X	X	1	D6
RXD7	X	X	1	D7
RX_DV	0	0	1	1

[a]Leftmost octet is the first received.
[b]Start Frame Delimiter octet.
[c]D0 through D7 is the first octet of the PDU (first octet of the Destination Address).

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Table 35–4—Start of receive with entire preamble preceding SFD

Signal	Bit values of octets received through GMII[a]									
RXD0	X	1	1	1	1	1	1	1	1[b]	D0[c]
RXD1	X	0	0	0	0	0	0	0	0	D1
RXD2	X	1	1	1	1	1	1	1	1	D2
RXD3	X	0	0	0	0	0	0	0	0	D3
RXD4	X	1	1	1	1	1	1	1	1	D4
RXD5	X	0	0	0	0	0	0	0	0	D5
RXD6	X	1	1	1	1	1	1	1	1	D6
RXD7	X	0	0	0	0	0	0	0	1	D7
RX_DV	0	1	1	1	1	1	1	1	1	1

[a]Leftmost octet is the first received.
[b]Start Frame Delimiter octet.
[c]D0 through D7 is the first octet of the PDU (first octet of the Destination Address).

35.2.3.3 Data <data>

The data <data> in a well-formed frame shall consist of a set of data octets.

35.2.3.4 End-of-Frame delimiter <efd>

Deassertion of the TX_EN signal constitutes an End-of-Frame delimiter <efd> for data conveyed on TXD<7:0>, and deassertion of RX_DV constitutes an End-of-Frame delimiter for data conveyed on RXD<7:0>.

35.2.3.5 Carrier extension <extend>

The Reconciliation sublayer signals carrier extension <extend> on the transmit path by the assertion of the TX_ER signal with the appropriate value of TXD<7:0> simultaneous with the deassertion of the TX_EN signal. Carrier extension is signaled on the receive path by the assertion of the RX_ER signal with the appropriate encoding on RXD<7:0> simultaneous with the deassertion of RX_DV. Carrier extension may not be present on all frames.

35.2.3.6 Definition of Start of Packet and End of Packet Delimiters

For the purposes of Clause 30 layer management, the Start of Packet delimiter is defined as the rising edge of RX_DV; and the End of Packet delimiter is defined as the falling edge of RX_DV. (See 30.2.2.2.2.)

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35.2.4 MAC delay constraints (with GMII)

A Gigabit Ethernet MAC with a GMII shall comply with the delay constraints in Table 35–5.

Table 35–5—MAC delay constraints (with GMII)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MAC ⇔ GMII	MAC transmit start to TX_EN = 1 sampled		48		GTX_CLK rising
	CRS assert to MAC detect[a]	0	48		
	CRS deassert to MAC detect[a]	0	48		
	CRS assert to TX_EN = 1 sampled (worst-case nondeferred transmit)		112		GTX_CLK rising
	COL assert to MAC detect	0	48		
	COL deassert to MAC detect	0	48		
	COL assert to TXD = Jam sampled (worst-case collision response)		112		GTX_CLK rising; first octet of Jam

[a]For any given implementation: Max deassert – Min. assert ≤ 16 bits.

35.2.5 Management functions

The GMII shall use the MII management register set specified in 22.2.4. The detailed description of some management registers is dependent on the PHY type and is specified in either 22.2.4 or 37.2.5.

35.3 Signal mapping

The GMII is specified such that implementers may share pins for implementation of the GMII, the MII specified in Clause 22 and the TBI specified in Clause 36. A recommended mapping of the signals for the GMII, MII, and TBI is shown in Table 35–6. Implementers using this recommended mapping are to comply with the GMII electrical characteristics in 35.5, MII electrical characteristics in 22.3, and the TBI electrical characteristics in 36.3 as appropriate for the implemented interfaces.

In an implementation supporting the MII and GMII, some signal pins are not used in both interfaces. For example, the TXD and RXD data bundles are four bits wide for the MII and eight bits wide for the GMII. Also, the GTX_CLK is only used when operating as a GMII while TX_CLK is used when operating as an MII.

Similarly, an implementation supporting both the GMII and TBI interfaces will map TBI signals onto the GMII control signal pins of TX_ER, TX_EN, RX_ER, and RX_DV. The COL and CRS signals of the GMII have no corollary in the TBI.

It is recommended that unused signal pins be driven to a valid logic state.

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Table 35–6—Signal mapping

GMII	MII	TBI
TX_ER	TX_ER	TX<9>
TX_EN	TX_EN	TX<8>
TXD<7>		TX<7>
TXD<6>		TX<6>
TXD<5>		TX<5>
TXD<4>		TX<4>
TXD<3>	TXD<3>	TX<3>
TXD<2>	TXD<2>	TX<2>
TXD<1>	TXD<1>	TX<1>
TXD<0>	TXD<0>	TX<0>
COL	COL	

GMII	MII	TBI
RX_ER	RX_ER	RX<9>
RX_DV	RX_DV	RX<8>
RXD<7>		RX<7>
RXD<6>		RX<6>
RXD<5>		RX<5>
RXD<4>		RX<4>
RXD<3>	RXD<3>	RX<3>
RXD<2>	RXD<2>	RX<2>
RXD<1>	RXD<1>	RX<1>
RXD<0>	RXD<0>	RX<0>
CRS	CRS	

35.4 LPI Assertion and Detection

Certain PHYs support Energy-Efficient Ethernet (see Clause 78). PHYs with EEE capability support LPI assertion and detection. LPI operation and the LPI client are described in 78.1. LPI signaling allows the LPI client to signal to the PHY and to the link partner that a break in the data stream is expected and components may use this information to enter power-saving modes that require additional time to resume normal operation. Similarly, it allows the LPI client to understand that the link partner has sent such an indication.

The LPI assertion and detection mechanism fits conceptually between the PLS Service Primitives and the GMII signals as shown in Figure 35–19.

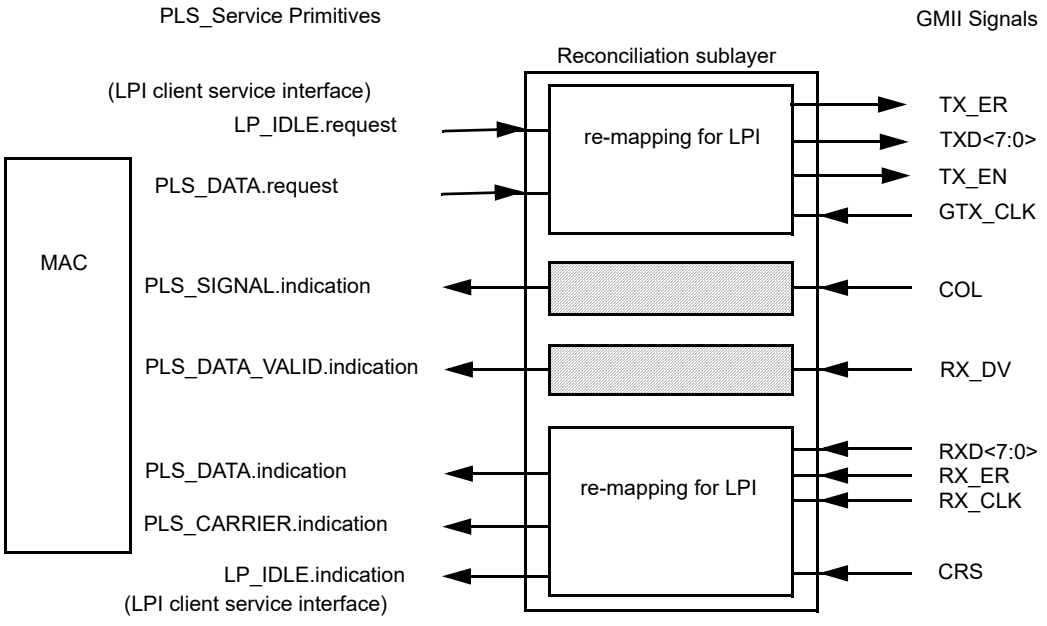

Figure 35–19—LPI assertion and detection mechanism

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The definition of TX_EN, TX_ER and TXD<7:0> is derived from the state of PLS_DATA.request (35.2.1.1), except when it is overridden by an assertion of LP_IDLE.request.

Similarly, RX_ER and RXD<7:0> are mapped to PLS_DATA.indication except when LP_IDLE is detected

CRS is mapped to PLS_CARRIER.indication except when LP_IDLE.request is asserted or the wake timer has yet to expire.

The timing of PLS_CARRIER.indication when used for the LPI function is controlled by the LPI transmit state diagram.

35.4.1 LPI messages

LP_IDLE.indication(LPI_INDICATION)

A primitive that indicates to the LPI client that the PHY has detected the assertion or deassertion of LPI from the link partner.

Values:DEASSERT: The link partner is operating with normal interframe behavior (default).
ASSERT: The link partner has asserted LPI.

LP_IDLE.request(LPI_REQUEST)

The LPI_REQUEST parameter can take one of two values: ASSERT or DEASSERT. ASSERT initiates the signaling of LPI to the link partner. DEASSERT stops the signaling of LPI to the link partner. The effect of receipt of this primitive is undefined if link_status is not OK (see 28.2.6.1.1) or if LPI_REQUEST=ASSERT within 1 s of the change of link_status to OK.

35.4.2 Transmit LPI state diagram

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been deasserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake-up time is enforced by the transmit LPI state diagram and the rules mapping CARRIER_SENSE.indication defined in 35.2.1. The implementation shall conform to the behavior described by the transmit LPI state diagram shown in Figure 35–20.

35.4.2.1 Conventions

The notation used in the state diagram follows the conventions of 34.2.

35.4.2.2 Variables and counters

The transmit LPI state diagram uses the following variables and counters:

power_on

Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.

Values:FALSE: The device is completely powered (default).
TRUE: The device has not been completely powered.

rs_reset

Used by management to control the resetting of the RS.

Values:FALSE: Do not reset the RS (default).
TRUE: Reset the RS.

tw_timer

A timer that counts the time since the deassertion of LPI. The terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2 and 78.4. The minimum value of $T_{w\_sys\_tx}$ shall be 16.5 μs for 1000BASE-T and 13.26 μs for 1000BASE-KX. Signal tw_timer_done is asserted on reaching its terminal count.

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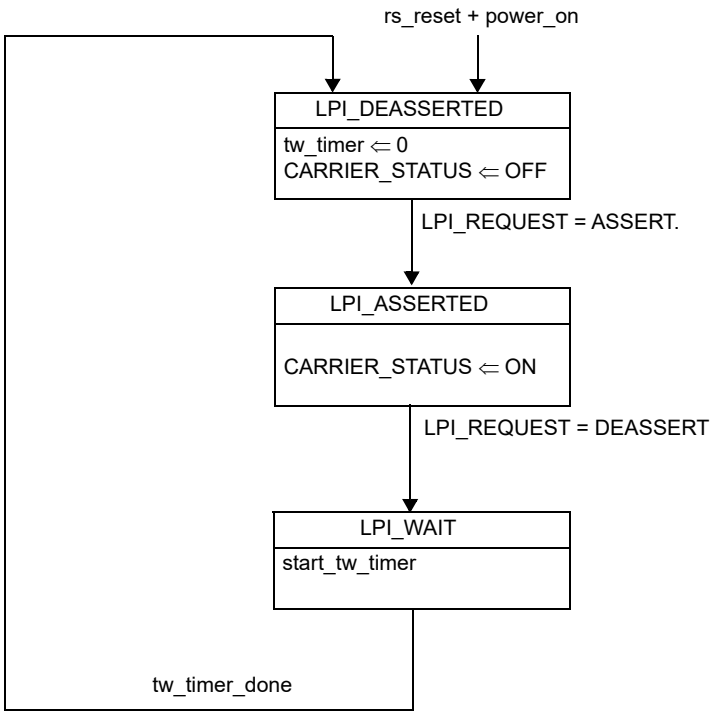

Figure 35–20—Transmit LPI state diagram

35.4.2.3 State diagram

35.4.3 Considerations for transmit system behavior

The transmit system should expect that egress data flow will be halted for at least resolved $T_{w\_sys\_tx}$ (see 78.2) time, in microseconds, after it requests the deassertion of LPI. Buffering and queue management should be designed to accommodate this.

35.4.3.1 Considerations for receive system behavior

The mapping function of the Reconciliation Sublayer shall continue to signal IDLE on PLS_DATA.indicate while it is detecting LP_IDLE on the GMII. The receive system should be aware that data frames may arrive at the GMII following the deassertion of LPI_INDICATION with a delay corresponding to the link partner's resolved $T_{w\_sys\_rx}$ (as specified in 78.5) time, in microseconds.

35.5 Electrical characteristics

The electrical characteristics of the GMII are specified such that the GMII can be applied within a variety of 1000 Mb/s equipment types. The electrical specifications are optimized for an integrated circuit to integrated circuit application environment. This includes applications where a number of PHY integrated circuits may be connected to a single integrated circuit as may be found in a repeater. Though specified for use on a single circuit board, applications to a motherboard-to-daughterboard interconnection are not precluded.

The electrical characteristics specified in this clause apply to all GMII signals except MDIO and MDC. The electrical characteristics for MDIO and MDC are specified in 22.3.4.

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35.5.1 DC characteristics

All GMII drivers and receivers shall comply with the dc parametric attributes specified in Table 35–7.

The potential applied to the input of a GMII receiver may exceed the potential of the receiver's power supply (i.e., a GMII driver powered from a 3.6 V supply driving V_{OH} into a GMII receiver powered from a 2.5 V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications.

Table 35–7—DC specifications

Symbol	Parameter	Conditions		Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	V_{CC} = Min	2.10	3.60	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0 mA	V_{CC} = Min	GND	0.50	V
V_{IH}	Input High Voltage			1.70	—	V
V_{IL}	Input Low Voltage			—	0.90	V
I_{IH}	Input High Current	V_{CC} = Max	V_{IN} = 2.1 V	—	40	µA
I_{IL}	Input Low Current	V_{CC} = Max	V_{IN} = 0.5 V	–600	—	µA

35.5.2 AC characteristics

The GMII ac electrical characteristics are specified in a manner that allows the implementer flexibility in selecting the GMII topologies its devices support and the techniques used to achieve the specified characteristics.

All GMII devices are required to support point-to-point links. The electrical length of the circuit board traces used to implement these links can be long enough to exhibit transmission line effects and require some form of termination. The implementer is allowed the flexibility to select the driver output characteristics and the termination technique and components to be used with its drivers for point-to-point links.

Implementers may elect to support other GMII topologies in addition to the point-to-point topology and may specify different termination techniques and components for each supported topology.

Since the output characteristics and output voltage waveforms of GMII drivers depend on the termination technique and the location of the termination components, the ac output characteristics of GMII drivers are not explicitly specified. Rather, the ac characteristics of the signal delivered to a GMII receiver are specified. These characteristics are independent of the topology and termination technique and apply uniformly to all GMII applications.

35.5.2.1 Signal Timing measurements

All GMII ac timing measurements are made at the GMII receiver input and are specified relative to the $V_{IL\_AC(\max)}$ and $V_{IH\_AC(\min)}$ thresholds.

The GTX_CLK and RX_CLK parameters t_{PERIOD}, t_{HIGH}, and t_{LOW} are defined in Figure 35–21. The GTX_CLK and RX_CLK parameters t_R and t_F and other transient performance specifications are defined in Figure 35–22. These parameters and the GTX_CLK and RX_CLK rising and falling slew rates are measured using the GMII point-to-point test circuit shown in Figure 35–24.

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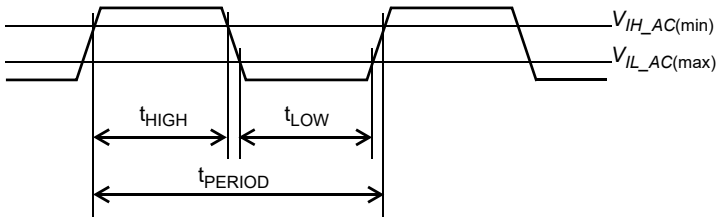
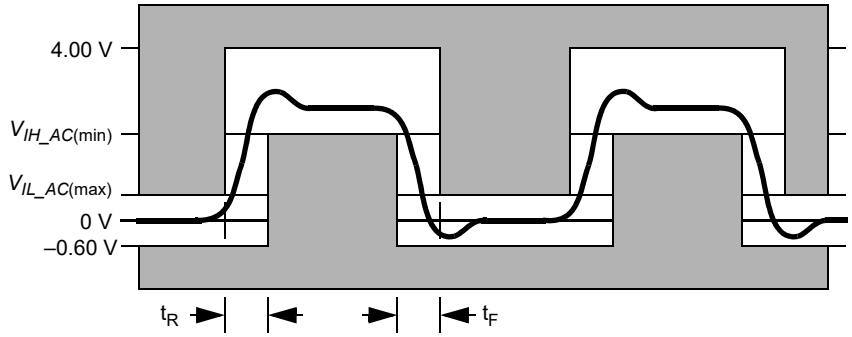


Figure 35–21—GTX_CLK and RX_CLK timing parameters at receiver input



NOTE—As measured at input measurement point

Figure 35–22—GMII receiver input potential template

The t_{SETUP} and t_{HOLD} parameters are defined in Figure 35–23. These parameters are measured using the GMII setup and hold time test circuit shown in Figure 35–25.

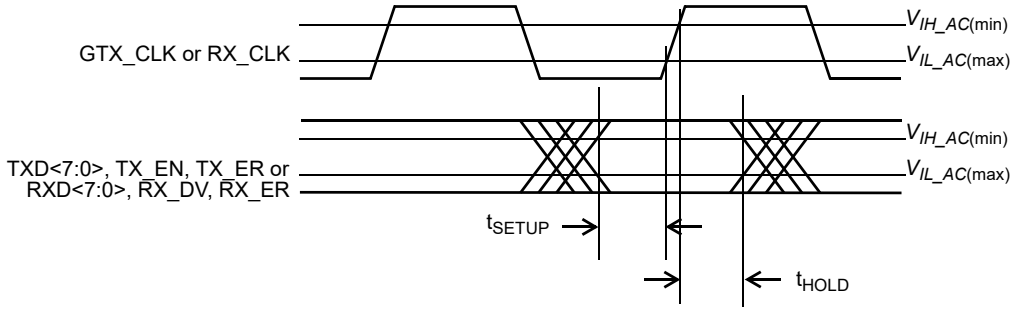


Figure 35–23—GMII signal timing at receiver input

35.5.2.2 GMII test circuit topology

The GMII point-to-point test circuit is defined in Figure 35–24. All parameter measurements made with this circuit are made at the Input Measurement Point defined in Figure 35–24. The 5 pF capacitor is included to approximate the input load of a GMII receiver. The termination networks used to implement the GMII point-to-point test circuit shall be those specified by the implementer of the GMII driver for 50 Ω ± 15% impedance transmission line point-to-point links. One or both of the termination networks specified by the implementer of the GMII driver may be straight-through connections if the networks are not needed to comply with the GMII ac and transient performance specifications.

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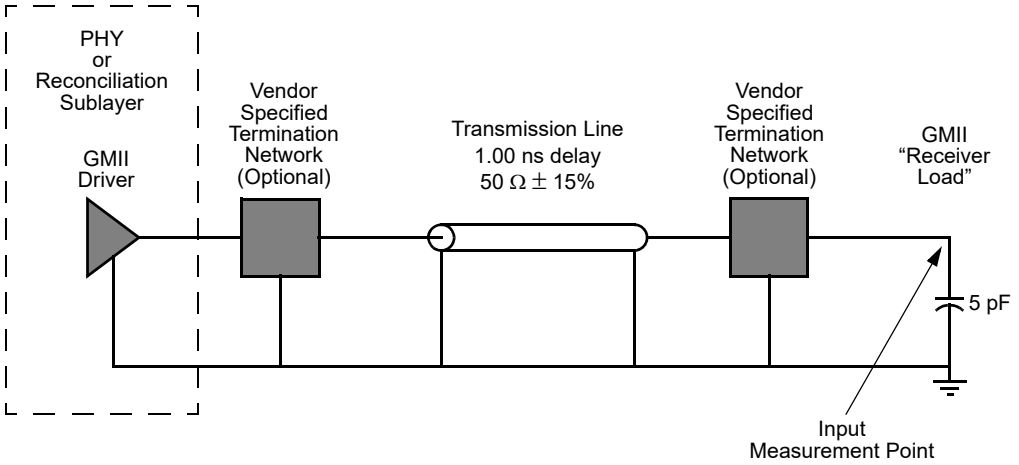

Figure 35–24—GMII point-to-point test circuit

The GMII point-to-point test circuit specifies a 1 ns transmission line. In a GMII implementation, the circuit board traces between the PHY and Reconciliation sublayer are not restricted to a delay of 1 ns.

The GMII setup and hold time test circuit is defined in Figure 35–25. The circuit is composed of the source of the synchronous GMII signal under test and its clock (the Reconciliation Layer or the PHY) and two GMII point-to-point test circuits. One of the test circuits includes the GMII driver for the signal under test, the other test circuit includes the GMII driver for the clock that provides timing for the signal under test. The signal under test is measured at the "Signal Measurement Point" relative to its clock, which is measured at the Clock Measurement Point as defined in Figure 35–25.

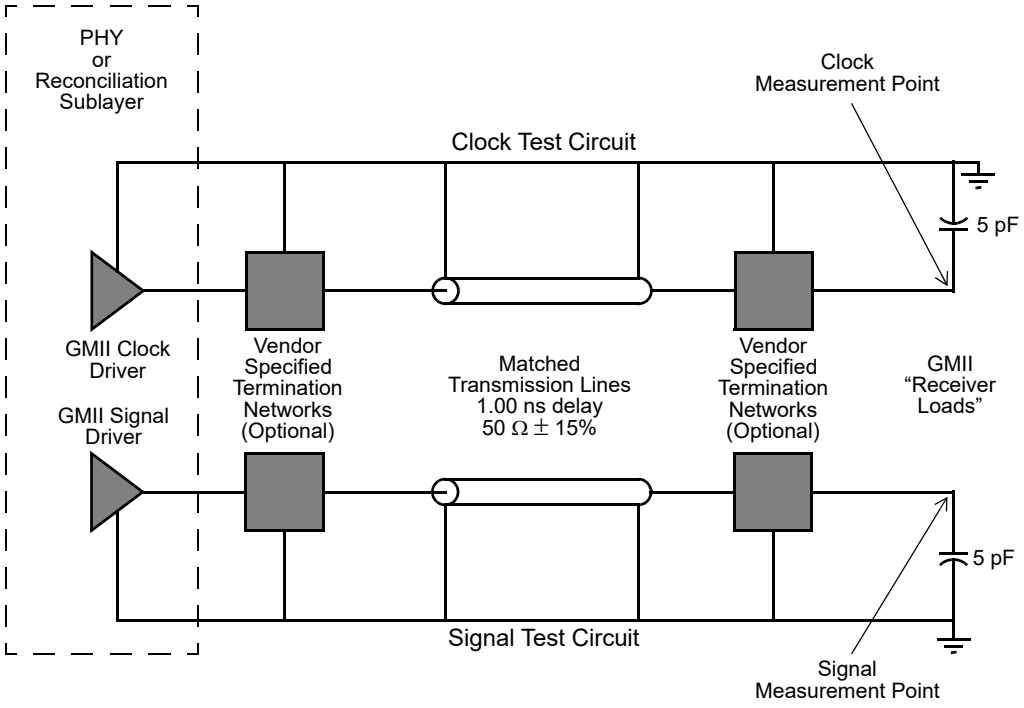

Figure 35–25—GMII setup and hold time test circuit

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35.5.2.3 GMII ac specifications

A GMII driver, when used in combination with the termination networks specified by the implementer of the driver for a specific GMII topology, shall produce a potential at the input pin of any GMII receiver in that topology that complies with the input potential template shown in Figure 35–22. This requirement applies for all GMII signals and any GMII topology.

To ensure that all GMII devices support point-to-point links, a GMII driver, when driving the GMII point-to-point test circuit shown in Figure 35–24, shall produce a potential at the Input Measurement Point of the GMII point-to-point test circuit that complies with the input potential template shown in Figure 35–22.

All GMII signal sources, including the GMII drivers, GMII receivers and GMII signals shall comply with the ac specifications in Table 35–8.

Table 35–8—AC specifications

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL_AC}	Input Low Voltage ac	—	—	0.70	V
V_{IH_AC}	Input High Voltage ac	—	1.90	—	V
f_{FREQ}	GTX_CLK Frequency	—	125 – 100 ppm	125 + 100 ppm	MHz
t_{PERIOD}	GTX_CLK Period	—	7.50	8.50	ns
t_{PERIOD}	RX_CLK Period	—	7.50	—	ns
t_{HIGH}	GTX_CLK, RX_CLK Time High	—	2.50	—	ns
t_{LOW}	GTX_CLK, RX_CLK Time Low	—	2.50	—	ns
t_R	GTX_CLK, RX_CLK Rise Time	V_{IL_AC}(max) to V_{IH_AC}(min)	—	1.00	ns
t_F	GTX_CLK, RX_CLK Fall Time	V_{IH_AC}(min) to V_{IL_AC}(max)	—	1.00	ns
—	Magnitude of GTX_CLK, RX_CLK Slew Rate (rising)[a]	V_{IL_AC}(max) to V_{IH_AC}(min)	0.6	—	V/ns
—	Magnitude of GTX_CLK, RX_CLK Slew Rate (falling)[a]	V_{IH_AC}(min) to V_{IL_AC}(max)	0.6	—	V/ns
t_{SETUP}	TXD, TX_EN, TX_ER Setup to ↑ GTX_CLK and RXD, RX_DV, RX_ER Setup to ↑ RX_CLK	—	2.50	—	ns
t_{HOLD}	TXD, TX_EN, TX_ER Hold from ↑ GTX_CLK and RXD, RX_DV, RX_ER Hold from ↑ RX_CLK	—	0.50	—	ns
t_{SETUP} (RCVR)	TXD, TX_EN, TX_ER Setup to ↑ GTX_CLK and RXD, RX_DV, RX_ER Setup to ↑ RX_CLK	—	2.00	—	ns
t_{HOLD} (RCVR)	TXD, TX_EN, TX_ER Hold from ↑ GTX_CLK and RXD, RX_DV, RX_ER Hold from ↑ RX_CLK	—	0.00	—	ns

[a]Clock Skew rate is the instantaneous rate of change of the clock potential with respect to time (dV/dt), not an average value over the entire rise or fall time interval. Conformance with this specification guarantees that the clock signals will rise and fall monotonically through the switching region.

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Two sets of setup and hold time parameters are specified in Table 35–8. The first set, t_{SETUP} and t_{HOLD}, applies to the source of a synchronous GMII signal and its clock and is measured using the "GMII Setup and Hold Time Test Circuit," which has transmission lines with matched propagation delays in the "clock" and "signal" paths. The second set, $t_{SETUP(RCVR)}$ and $t_{HOLD(RCVR)}$, applies to the GMII receiver and specifies the minimum setup and hold times available to the GMII receiver at its input pins. The difference between the two sets of setup and hold time parameters provides margin for a small amount of mismatch in the propagation delays of the "clock" path and the "signal" paths in GMII applications.

The GMII ac specifications in Table 35–8 and the transient performance specifications in Figure 35–22 shall be met under all combination of worst-case GMII driver process and supply potential variation, ambient temperature, transmission line impedance variation, and termination network component impedance variation.

Designers of components containing GMII receivers should note that there is no upper bound specified on the magnitude of the slew rate of signals that may be applied to the input of a GMII receiver. The high-frequency energy in a high slew rate (short rise time) signal can excite the parasitic reactances of the receiver package and input pad to such a degree that the signal at the receiver input pin and the signal at the input pad differ significantly. This is particularly true for GTX_CLK and RX_CLK, which transition at twice the rate of other signals in the interface.

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35.6 Protocol implementation conformance statement (PICS) proforma for Clause 35, Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)[74]

35.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 35, Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

35.6.2 Identification

35.6.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

35.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 35, Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[74] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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35.6.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*EL	GMII electrical interface	35.5		O	Yes [ ] No [ ]
*G1	PHY support of GMII	35.1.3		O	Yes [ ] No [ ]
G2	Reconciliation sublayer support of GMII	35.1.3		O	Yes [ ] No [ ]
*HD	Half duplex capability	35.2.2.7		O	Yes [ ] No [ ]
*LPI	Implementation of LPI	35.2.2		O	Yes [ ] No [ ]

35.6.3 PICS proforma tables for reconciliation sublayer and Gigabit Media Independent Interface

35.6.3.1 Mapping of PLS service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
PL1	Response to error in frame	35.2.1.5	Produce FrameCheckError when RX_DV and RX_ER are asserted	M	Yes [ ]
PL2	Response to error in extension	35.2.1.5	Produce FrameCheckError on received Carrier Extend Error	M	Yes [ ]
PL2a	Propagation of errors in frame	35.2.1.6	Assert TX_ER while TX_EN asserted	O	Yes [ ]
PL3	Propagation of errors in extension	35.2.1.6	Send ONE or ZERO and assert Carrier Extend Error to propagate error within carrier extension	O	Yes [ ] No [ ]

35.6.3.2 GMII signal functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
SF1					
SF2	RX_CLK frequency	35.2.2.2	125 MHz ±0.01% when received data rate is within tolerance	M	Yes [ ]
SF3	Loss of signal	35.2.2.2	Source RX_CLK from nominal clock	M	Yes [ ]
SF4	RX_CLK min high/low time during transitions between clock sources	35.2.2.2	No decrease of period, or time between adjacent edges, of RX_CLK below limits specified in Table 35–8	M	Yes [ ]

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35.6.3.2 GMII signal functional specifications *(continued)*

Item	Feature	Subclause	Value/Comment	Status	Support
SF5	RX_CLK max high/low time during transitions between clock sources	35.2.2.2	No increase greater than two nominal clock periods between adjacent edges of RX_CLK	M	Yes [ ]
SF6	TX_EN assertion	35.2.2.3	On first octet of preamble	M	Yes [ ]
SF7	TX_EN remains asserted	35.2.2.3	Stay asserted while all octets are transmitted over GMII	M	Yes [ ]
SF8	TX_EN negation	35.2.2.3	Before first GTX_CLK after final octet of frame	M	Yes [ ]
SF9	TX_EN transitions	35.2.2.3	Synchronous with GTX_CLK	M	Yes [ ]
SF10	TXD <7:0> transitions	35.2.2.4	Synchronous with GTX_CLK	M	Yes [ ]
SF11	TXD <7:0> effect on PHY while TX_EN and TX_ER are deasserted	35.2.2.4	No effect	M	Yes [ ]
SF12	Signaling carrier extension	35.2.2.4	Only immediately following frame	M	Yes [ ]
SF13	TX_ER transitions	35.2.2.5	Synchronous with GTX_CLK	M	Yes [ ]
SF14	TX_ER effect on PHY while TX_EN is asserted	35.2.2.5	Cause PHY to emit invalid code-group	M	Yes [ ]
SF15	Transmission of end-of-packet delimiter	35.2.2.5	On deassertion of TX_EN and simultaneous assertion of TX_ER	M	Yes [ ]
SF16	TX_ER implementation	35.2.2.5	At GMII of PHY	M	Yes [ ]
SF17	TX_ER implementation	35.2.2.5	Implemented if half duplex operation supported.	HD:M	Yes [ ] N/A [ ]
SF18	TX_ER driven	35.2.2.5	To valid state even if constant	M	Yes [ ]
SF19	RX_DV transitions	35.2.2.7	Synchronous with RX_CLK	M	Yes [ ]
SF20	RX_DV assertion	35.2.2.7	From first recovered octet to final octet of a frame	M	Yes [ ]
SF21	RX_DV negation	35.2.2.7	Before the first RX_CLK following the final octet of the frame	M	Yes [ ]
SF22	RXD <7:0> transitions	35.2.2.8	Synchronous with RX_CLK	M	Yes [ ]
SF22a	RXD loopback	35.2.2.8	No loopback unless loopback mode selected	M	Yes [ ]
SF23	Signaling carrier extension	35.2.2.8	Only immediately following frame	M	Yes [ ]
SF24	RX_ER transitions	35.2.2.9	Synchronous with RX_CLK	M	Yes [ ]
SF25	RX_ER assertion	35.2.2.9	By PHY to indicate error	M	Yes [ ]
SF26	Generation of EXTEND	35.2.2.9	In response to simultaneous deassertion of RX_DV and assertion of RX_ER by PHY	M	Yes [ ]

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35.6.3.2 GMII signal functional specifications *(continued)*

Item	Feature	Subclause	Value/Comment	Status	Support
SF27	CRS assertion	35.2.2.11	By PHY when either transmit or receive is NON-IDLE	M	Yes [ ]
SF28	CRS deassertion	35.2.2.11	By PHY when both transmit and receive are IDLE	M	Yes [ ]
SF29	CRS assertion during collision	35.2.2.11	Remain asserted throughout	M	Yes [ ]
SF30	CRS assertion—repeater	35.2.2.11	By repeater when receive is NON-IDLE	M	Yes [ ]
SF31	CRS deassertion—repeater	35.2.2.11	By repeater when medium is IDLE	M	Yes [ ]
SF32	COL assertion	35.2.2.12	By PHY upon collision on medium	M	Yes [ ]
SF33	COL remains asserted while collision persists	35.2.2.12		M	Yes [ ]

35.6.3.3 Data stream structure

Item	Feature	Subclause	Value/Comment	Status	Support
DS1	Format of transmitted data stream	35.2.3	Per Figure 35–17	M	Yes [ ]
DS2	Transmission order	35.2.3	Per Figure 35–18	M	Yes [ ]
DS3	Preamble 7 octets long	35.2.3.2	10101010 10101010 10101010 10101010 10101010 10101010 10101010	M	Yes [ ]
DS4	Preamble and SFD transmission	35.2.3.2	Starting at assertion of TX_EN	M	Yes [ ]
DS5	Minimum preamble	35.2.3.2	MAC operates with minimum preamble	M	Yes [ ]
DS6	Data length	35.2.3.3	Set of octets	M	Yes [ ]

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35.6.3.4 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Assertion of LPI in Tx direction	35.2.2.4	As defined in Table 35–1	LPI:M	Yes [ ]
L2	Assertion of LPI in Rx direction	35.2.2.8	As defined in Table 35–2	LPI:M	Yes [ ]
L3	GTX_CLK stoppable during LPI	35.2.2.6	At least 9 cycles after LPI assertion	LPI:O	Yes [ ]
L4	RX_CLK stoppable during LPI	35.2.2.10		LPI:O	Yes [ ]
L5	Terminal count for tw_timer	35.4.2.2	Based on resolved $T_{w\_sys\_tx}$	LPI:M	Yes [ ]

35.6.3.5 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	MAC delay	35.2.4	Comply with Table 35–5	M	Yes [ ]

35.6.3.6 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Management registers	35.2.5	Use register set specified in 22.2.4	M	Yes [ ]

35.6.3.7 Electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
EC1	DC specifications	35.5.1	All drivers and receivers per Table 35–7	EL:M	Yes [ ] N/A [ ]
EC3	AC and transient specifications	35.5.2.3	Under all combinations of worst case parameters	EL:M	Yes [ ] N/A [ ]
EC4	Topology input potential	35.5.2.3	Complies with Figure 35–22 at each receiver of topology	EL:M	Yes [ ] N/A [ ]
EC5	Tested driver input potential	35.5.2.3	Complies with Figure 35–22 as tested per Figure 35–24	EL:M	Yes [ ] N/A [ ]
EC6	Test circuit termination	35.5.2.2	As specified by GMII driver implementer	EL:M	Yes [ ] N/A [ ]
EC7	AC specifications	35.5.2.3	Per Table 35–8	EL:M	Yes [ ] N/A [ ]

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36. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X

36.1 Overview

36.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer that are common to a family of 1000 Mb/s Physical Layer implementations, collectively known as 1000BASE-X.

1000BASE-X is based on the Physical Layer standards developed by ANSI INCITS 230-1994 (Fibre Channel Physical and Signaling Interface). In particular, this standard uses the same 8B/10B coding as Fibre Channel, a PMA sublayer compatible with speed-enhanced versions of the ANSI 10-bit serializer chip, and similar optical and electrical specifications.

1000BASE-X PCS and PMA sublayers map the interface characteristics of the PMD sublayer (including MDI) to the services expected by the Reconciliation sublayer. 1000BASE-X can be extended to support any other full duplex medium requiring only that the medium be compliant at the PMD level.

36.1.2 Objectives

The following are the objectives of 1000BASE-X:

a) To support the CSMA/CD MAC
b) To support the 1000 Mb/s repeater
c) To provide for Auto-Negotiation among like 1000 Mb/s PMDs
d) To provide 1000 Mb/s data rate at the GMII
e) To support cable plants using 150 Ω balanced copper cabling, or cabled optical fiber compliant with ISO/IEC 11801:1995
f) To allow for a nominal network extent of up to 5 km, including
    1) 150 Ω balanced links of 25 m span
    2) one-repeater networks of 50 m span (using all 150 Ω balanced copper cabling)
    3) one-repeater networks of 200 m span (using fiber)
    4) DTE/DTE links of 5000 m (using fiber)
g) To preserve full duplex behavior of underlying PMD channels
h) To support a BER objective of 10^{-12}

NOTE—The 1000BASE-X PCS and PMA do not constrain the extent of a full duplex network. PMDs in Clause 59 and Clause 60 have ranges beyond 5 km.

36.1.3 Relationship of 1000BASE-X to other standards

Figure 36–1 depicts the relationships among the 1000BASE-X sublayers (shown shaded), the CSMA/CD MAC and reconciliation layers, and upper layer clients such as the ISO/IEC 8802-2 LLC.

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36.1.4 Summary of 1000BASE-X sublayers

The following provides an overview of the 1000BASE-X sublayers.[75]

36.1.4.1 Physical Coding Sublayer (PCS)

The PCS interface is the Gigabit Media Independent Interface (GMII) that provides a uniform interface to the Reconciliation sublayer for all 1000 Mb/s PHY implementations (e.g., not only 1000BASE-X but also other possible types of gigabit PHY entities). 1000BASE-X provides services to the GMII in a manner analogous to how 100BASE-X provides services to the 100 Mb/s MII.

The 1000BASE-X PCS provides all services required by the GMII, including

a) Encoding (decoding) of GMII data octets to (from) ten-bit code-groups (8B/10B) for communication with the underlying PMA
b) Generating Carrier Sense and Collision Detect indications for use by PHY's half duplex clients
c) Managing the Auto-Negotiation process, and informing the management entity via the GMII when the PHY is ready for use

36.1.4.2 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS to support the use of a range of serial-bit-oriented physical media. The 1000BASE-X PMA performs the following functions:

a) Mapping of transmit and receive code-groups between the PCS and PMA via the PMA Service Interface
b) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMD
c) Recovery of clock from the 8B/10B-coded data supplied by the PMD
d) Mapping of transmit and receive bits between the PMA and PMD via the PMD Service Interface
e) Data loopback at the PMD Service Interface

36.1.4.3 Physical Medium Dependent (PMD) sublayer

1000BASE-X Physical Layer signaling for fiber and copper media is adapted from ANSI INCITS 230-1994 (FC-PH), Clauses 6 and 7 respectively. These clauses define 1062.5 Mb/s, full duplex signaling systems that accommodate single-mode optical fiber, multimode optical fiber, and 150 Ω balanced copper cabling. 1000BASE-X adapts these basic Physical Layer specifications for use with the PMD sublayer and media specified in Clause 38 and Clause 39.

The MDI, logically subsumed within each PMD subclause, is the actual medium attachment, including connectors, for the various supported media.

Figure 36–1 depicts the relationship between 1000BASE-X and its associated PMD sublayers.

36.1.5 Inter-sublayer interfaces

There are a number of interfaces employed by 1000BASE-X. Some (such as the PMA Service Interface) use an abstract service model to define the operation of the interface. An optional physical instantiation of the PCS Interface has been defined. It is called the GMII (Gigabit Media Independent Interface). An optional

[75]The 1000BASE-X PHY consists of that portion of the Physical Layer between the MDI and GMII consisting of the PCS, PMA, and PMD sublayers. The 1000BASE-X PHY is roughly analogous to the 100BASE-X PHY.

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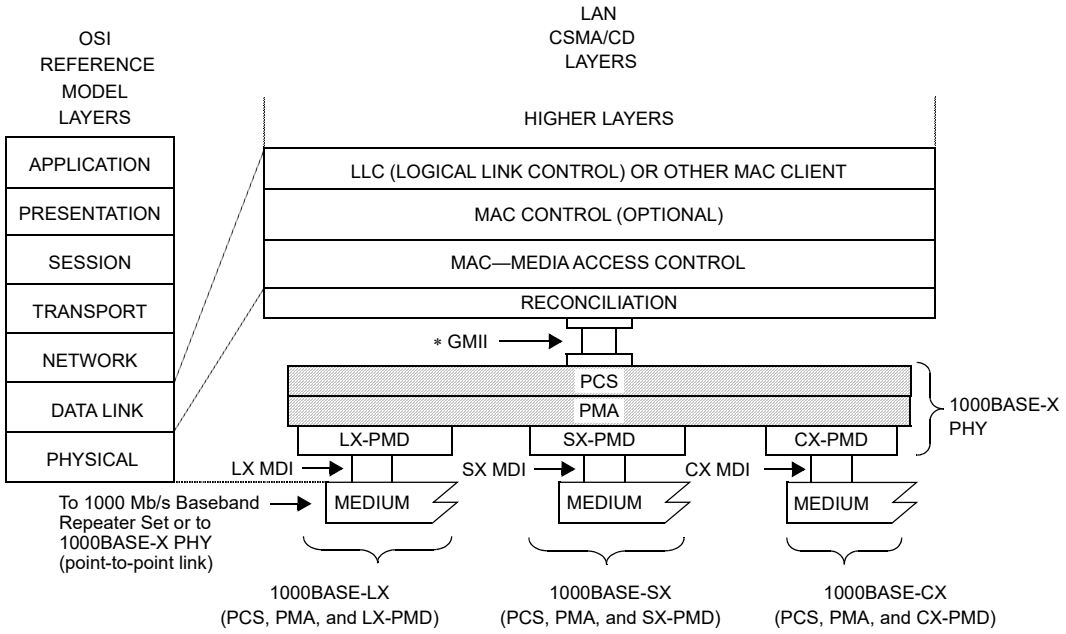

MDI=MEDIUM DEPENDENT INTERFACE
GMII=GIGABIT MEDIA INDEPENDENT INTERFACE
PCS=PHYSICAL CODING SUBLAYER
PMA=PHYSICAL MEDIUM ATTACHMENT
PHY=PHYSICAL LAYER DEVICE
PMD=PHYSICAL MEDIUM DEPENDENT
LX-PMD=PMD FOR FIBER—LONG WAVELENGTH, Clause 38
SX-PMD=PMD FOR FIBER—SHORT WAVELENGTH, Clause 38
CX-PMD=PMD FOR 150 Ω BALANCED COPPER CABLING, Clause 39

NOTE—The PMD sublayers are mutually independent.

* GMII is optional.

Figure 36–1—Relationship of 1000BASE-X and the PMDs

physical instantiation of the PMA Service Interface has also been defined (see 36.3.3). It is adapted from ANSI Technical Report TR/X3.18-1997 (Fibre Channel—10-bit Interface). Figure 36–2 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 1000BASE-X.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and code-groups, implementers may choose other data path widths for implementation convenience. The only exceptions are a) the GMII, which, when implemented at an observable interconnection port, uses an octet-wide data path as specified in Clause 35, b) the PMA Service Interface, which, when physically implemented as the TBI (Ten-Bit Interface) at an observable interconnection port, uses a 10-bit wide data path as specified in 36.3.3, and c) the MDI, which uses a serial, physical interface.

36.1.6 Functional block diagram

Figure 36–2 provides a functional block diagram of the 1000BASE-X PHY.

36.1.7 State diagram conventions

The body of this standard is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

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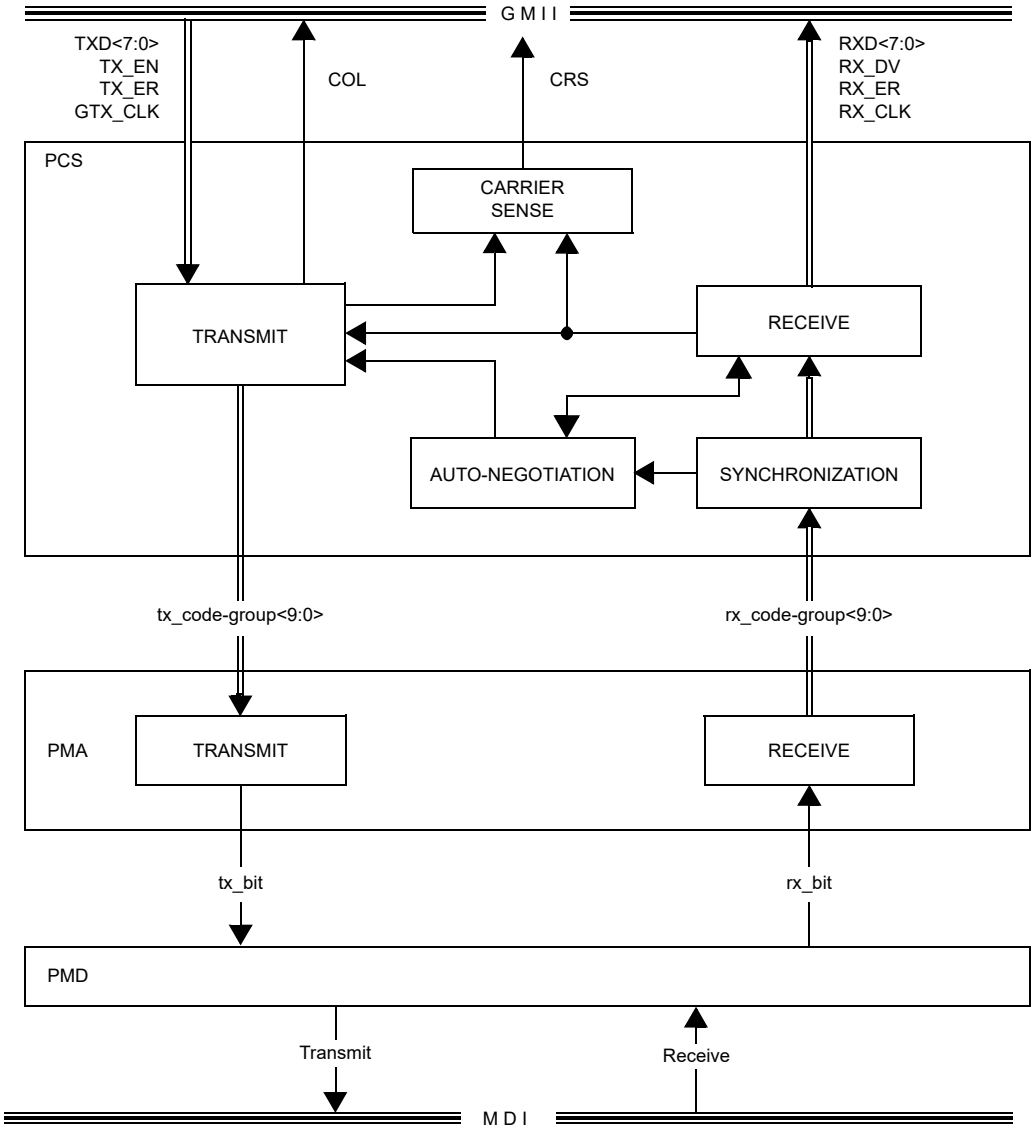

Figure 36–2—Functional block diagram

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2.

36.2 Physical Coding Sublayer (PCS)

36.2.1 PCS Interface (GMII)

The PCS Service Interface allows the 1000BASE-X PCS to transfer information to and from a PCS client. PCS clients include the MAC (via the Reconciliation sublayer) and repeater. The PCS Interface is precisely defined as the Gigabit Media Independent Interface (GMII) in Clause 35.

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In this clause, the setting of GMII variables to TRUE or FALSE is equivalent, respectively, to “asserting” or “deasserting” them as specified in Clause 35.

36.2.2 Functions within the PCS

The PCS comprises the PCS Transmit, Carrier Sense, Synchronization, PCS Receive, and Auto-Negotiation processes for 1000BASE-X. The PCS shields the Reconciliation sublayer (and MAC) from the specific nature of the underlying channel. When communicating with the GMII, the PCS uses an octet-wide, synchronous data path, with packet delimiting being provided by separate transmit control signals (TX_EN and TX_ER) and receive control signals (RX_DV and RX_ER). When communicating with the PMA, the PCS uses a ten-bit wide, synchronous data path, which conveys ten-bit code-groups. At the PMA Service Interface, code-group alignment and MAC packet delimiting are made possible by embedding special non-data code-groups in the transmitted code-group stream. The PCS provides the functions necessary to map packets between the GMII format and the PMA Service Interface format.

The PCS Transmit process continuously generates code-groups based upon the TXD <7:0>, TX_EN, and TX_ER signals on the GMII, sending them immediately to the PMA Service Interface via the PMA_UNITDATA.request primitive. The PCS Transmit process generates the GMII signal COL based on whether a reception is occurring simultaneously with transmission. Additionally, it generates the internal flag, transmitting, for use by the Carrier Sense process. The PCS Transmit process monitors the Auto-Negotiation process xmit flag to determine whether to transmit data or reconfigure the link.

The Carrier Sense process controls the GMII signal CRS (see Figure 36–8).

The PCS Synchronization process continuously accepts code-groups via the PMA_UNITDATA.indication primitive and conveys received code-groups to the PCS Receive process via the SYNC_UNITDATA.indicate primitive. The PCS Synchronization process sets the sync_status flag to indicate whether the PMA is functioning dependably (as well as can be determined without exhaustive error-ratio analysis).

The PCS Receive process continuously accepts code-groups via the SYNC_UNITDATA.indicate primitive. The PCS Receive process monitors these code-groups and generates RXD <7:0>, RX_DV, and RX_ER on the GMII, and the internal flag, receiving, used by the Carrier Sense and Transmit processes.

The PCS Auto-Negotiation process sets the xmit flag to inform the PCS Transmit process to either transmit normal idles interspersed with packets as requested by the GMII or to reconfigure the link. The PCS Auto-Negotiation process is specified in Clause 37.

36.2.3 Use of code-groups

The PCS maps GMII signals into ten-bit code groups, and vice versa, using an 8B/10B block coding scheme. Implicit in the definition of a code-group is an establishment of code-group boundaries by a PMA code-group alignment function as specified in 36.3.2.4. Code-groups are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret code-groups as provided by the rules in 36.2.4.

36.2.4 8B/10B transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link. The encodings defined by the transmission code ensure that sufficient transitions are present in the PHY bit stream to make clock recovery possible at the receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some of the special code-groups of the transmission code contain a distinct and easily recognizable bit pattern that assists a receiver in achieving code-group alignment on the

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incoming PHY bit stream. The 8B/10B transmission code specified for use in this standard has a high transition density, is a run-length-limited code, and is DC-balanced. The transition density of the 8B/10B symbols ranges from 3 to 8 transitions per symbol.

The definition of the 8B/10B transmission code in this standard is identical to that specified in ANSI INCITS 230-1994 (FC-PH), Clause 11. The relationship of code-group bit positions to PMA and other PCS constructs is illustrated in Figure 36–3.

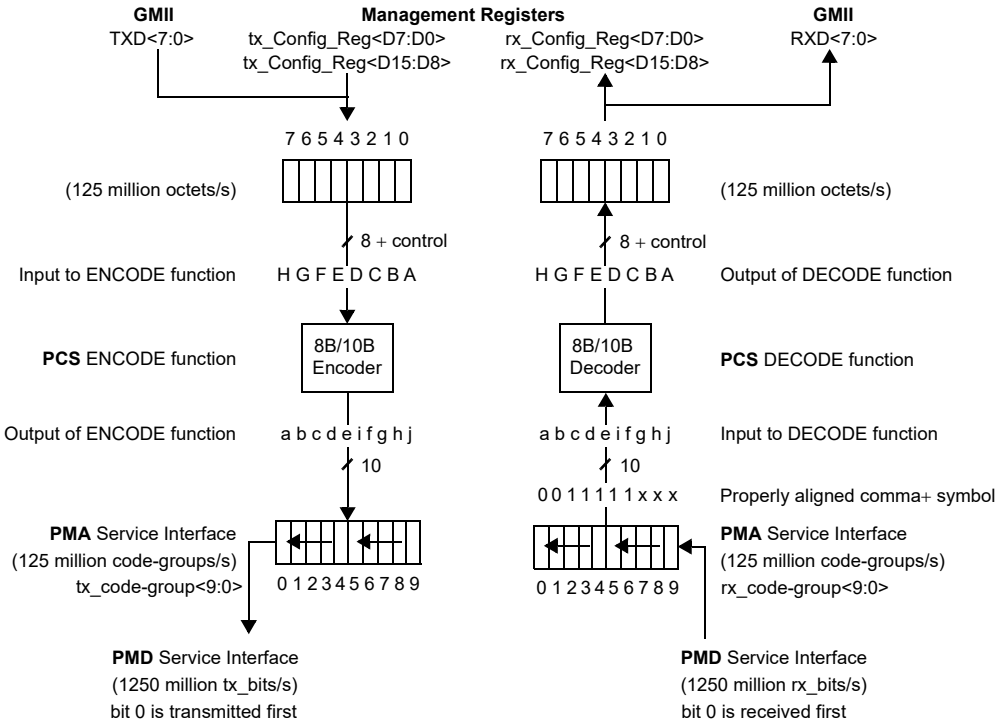

Figure 36–3—PCS reference diagram

36.2.4.1 Notation conventions

8B/10B transmission code uses letter notation for describing the bits of an unencoded information octet and a single control variable. Each bit of the unencoded information octet contains either a binary zero or a binary one. A control variable, Z, has either the value D or the value K. When the control variable associated with an unencoded information octet contains the value D, the associated encoded code-group is referred to as a data code-group. When the control variable associated with an unencoded information octet contains the value K, the associated encoded code-group is referred to as a special code-group.

The bit notation of A,B,C,D,E,F,G,H for an unencoded information octet is used in the description of the 8B/10B transmission code. The bits A,B,C,D,E,F,G,H are translated to bits a,b,c,d,e,i,f,g,h,j of 10-bit transmission code-groups. 8B/10B code-group bit assignments are illustrated in Figure 36–3. Each valid code-group has been given a name using the following convention: /Dx.y/ for the 256 valid data code-groups, and /Kx.y/ for special control code-groups, where x is the decimal value of bits EDCBA, and y is the decimal value of bits HGF.

36.2.4.2 Transmission order

Code-group bit transmission order is illustrated in Figure 36–3.

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Code-groups within multi-code-group ordered sets (as specified in Table 36–3) are transmitted sequentially beginning with the special code-group used to distinguish the ordered set (e.g., /K28.5/) and proceeding code-group by code-group from left to right within the definition of the ordered set until all code-groups of the ordered set are transmitted.

The first code-group of every multi-code-group ordered set is transmitted in an even-numbered code-group position counting from the first code-group after a reset or power-on. Subsequent code-groups continuously alternate as odd and even-numbered code-groups.

The contents of a packet are transmitted sequentially beginning with the ordered set used to denote the Start_of_Packet (the SPD delimiter) and proceeding code-group by code-group from left to right within the definition of the packet until the ordered set used to denote the End_of_Packet (the EPD delimiter) is transmitted.

36.2.4.3 Valid and invalid code-groups

Table 36–1a–e defines the valid data code-groups (D code-groups) of the 8B/10B transmission code. Table 36–2 defines the valid special code-groups (K code-groups) of the code. The tables are used for both generating valid code-groups (encoding) and checking the validity of received code-groups (decoding). In the tables, each octet entry has two columns that represent two (not necessarily different) code-groups. The two columns correspond to the valid code-group based on the current value of the running disparity (Current RD – or Current RD +). Running disparity is a binary parameter with either the value negative (–) or the value positive (+). Annex 36B provides several 8B/10B transmission code running disparity calculation examples.

36.2.4.4 Running disparity rules

After powering on or exiting a test mode, the transmitter shall assume the negative value for its initial running disparity. Upon transmission of any code-group, the transmitter shall calculate a new value for its running disparity based on the contents of the transmitted code-group.

After powering on or exiting a test mode, the receiver should assume either the positive or negative value for its initial running disparity. Upon the reception of any code-group, the receiver determines whether the code-group is valid or invalid and calculates a new value for its running disparity based on the contents of the received code-group.

The following rules for running disparity shall be used to calculate the new running disparity value for code-groups that have been transmitted (transmitter's running disparity) and that have been received (receiver’s running disparity).

Running disparity for a code-group is calculated on the basis of sub-blocks, where the first six bits (abcdei) form one sub-block (six-bit sub-block) and the second four bits (fghj) form the other sub-block (four-bit sub-block). Running disparity at the beginning of the six-bit sub-block is the running disparity at the end of the last code-group. Running disparity at the beginning of the four-bit sub-block is the running disparity at the end of the six-bit sub-block. Running disparity at the end of the code-group is the running disparity at the end of the four-bit sub-block.

Running disparity for the sub-blocks is calculated as follows:

a) Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the six-bit sub-block if the six-bit sub-block is 000111, and it is positive at the end of the four-bit sub-block if the four-bit sub-block is 0011.

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b) Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the six-bit sub-block if the six-bit sub-block is 111000, and it is negative at the end of the four-bit sub-block if the four-bit sub-block is 1100.

c) Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

NOTE—All sub-blocks with equal numbers of zeros and ones are disparity neutral. In order to limit the run length of 0's or 1's between sub-blocks, the 8B/10B transmission code rules specify that sub-blocks encoded as 000111 or 0011 are generated only when the running disparity at the beginning of the sub-block is positive; thus, running disparity at the end of these sub-blocks is also positive. Likewise, sub-blocks containing 111000 or 1100 are generated only when the running disparity at the beginning of the sub-block is negative; thus, running disparity at the end of these sub-blocks is also negative.

36.2.4.5 Generating code-groups

The appropriate entry in either Table 36–1a–e or Table 36–2 is found for each octet for which a code-group is to be generated (encoded). The current value of the transmitter's running disparity shall be used to select the code-group from its corresponding column. For each code-group transmitted, a new value of the running disparity is calculated. This new value is used as the transmitter's current running disparity for the next octet to be encoded and transmitted.

36.2.4.6 Checking the validity of received code-groups

The following rules shall be used to determine the validity of received code groups:

a) The column in Table 36–1a–e and Table 36–2 corresponding to the current value of the receiver's running disparity is searched for the received code-group.

b) If the received code-group is found in the proper column, according to the current running disparity, then the code-group is considered valid and, for data code-groups, the associated data octet determined (decoded).

c) If the received code-group is not found in that column, then the code-group is considered invalid.

d) Independent of the code-group's validity, the received code-group is used to calculate a new value of running disparity. The new value is used as the receiver's current running disparity for the next received code-group.

Detection of an invalid code-group does not necessarily indicate that the code-group in which the invalid code-group was detected is in error. Invalid code-groups may result from a prior error which altered the running disparity of the PHY bit stream but which did not result in a detectable error at the code-group in which the error occurred.

The number of invalid code-groups detected is proportional to the bit error ratio (BER) of the link. Link error monitoring may be performed by counting invalid code-groups.

36.2.4.7 Ordered sets

Eight ordered sets, consisting of a single special code-group or combinations of special and data code-groups are specifically defined. Ordered sets which include /K28.5/ provide the ability to obtain bit and code-group synchronization and establish ordered set alignment (see 36.2.4.9 and 36.3.2.4). Ordered sets provide for the delineation of a packet and synchronization between the transmitter and receiver circuits at opposite ends of a link. Table 36–3 lists the defined ordered sets. Certain PHYs include an option (see 78.3) to transmit or receive /LI/, /LI1/ and /LI2/ to support Energy-Efficient Ethernet (see Clause 78).

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Table 36–1a—Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +
			abcdei fghj	abcdei fghj
D0.0	00	000 00000	100111 0100	011000 1011
D1.0	01	000 00001	011101 0100	100010 1011
D2.0	02	000 00010	101101 0100	010010 1011
D3.0	03	000 00011	110001 1011	110001 0100
D4.0	04	000 00100	110101 0100	001010 1011
D5.0	05	000 00101	101001 1011	101001 0100
D6.0	06	000 00110	011001 1011	011001 0100
D7.0	07	000 00111	111000 1011	000111 0100
D8.0	08	000 01000	111001 0100	000110 1011
D9.0	09	000 01001	100101 1011	100101 0100
D10.0	0A	000 01010	010101 1011	010101 0100
D11.0	0B	000 01011	110100 1011	110100 0100
D12.0	0C	000 01100	001101 1011	001101 0100
D13.0	0D	000 01101	101100 1011	101100 0100
D14.0	0E	000 01110	011100 1011	011100 0100
D15.0	0F	000 01111	010111 0100	101000 1011
D16.0	10	000 10000	011011 0100	100100 1011
D17.0	11	000 10001	100011 1011	100011 0100
D18.0	12	000 10010	010011 1011	010011 0100
D19.0	13	000 10011	110010 1011	110010 0100
D20.0	14	000 10100	001011 1011	001011 0100
D21.0	15	000 10101	101010 1011	101010 0100
D22.0	16	000 10110	011010 1011	011010 0100
D23.0	17	000 10111	111010 0100	000101 1011
D24.0	18	000 11000	110011 0100	001100 1011
D25.0	19	000 11001	100110 1011	100110 0100
D26.0	1A	000 11010	010110 1011	010110 0100
D27.0	1B	000 11011	110110 0100	001001 1011
D28.0	1C	000 11100	001110 1011	001110 0100
D29.0	1D	000 11101	101110 0100	010001 1011
D30.0	1E	000 11110	011110 0100	100001 1011
D31.0	1F	000 11111	101011 0100	010100 1011
D0.1	20	001 00000	100111 1001	011000 1001
D1.1	21	001 00001	011101 1001	100010 1001
D2.1	22	001 00010	101101 1001	010010 1001
D3.1	23	001 00011	110001 1001	110001 1001
D4.1	24	001 00100	110101 1001	001010 1001
D5.1	25	001 00101	101001 1001	101001 1001
D6.1	26	001 00110	011001 1001	011001 1001
D7.1	27	001 00111	111000 1001	000111 1001
D8.1	28	001 01000	111001 1001	000110 1001
D9.1	29	001 01001	100101 1001	100101 1001
D10.1	2A	001 01010	010101 1001	010101 1001
D11.1	2B	001 01011	110100 1001	110100 1001
D12.1	2C	001 01100	001101 1001	001101 1001
D13.1	2D	001 01101	101100 1001	101100 1001
D14.1	2E	001 01110	011100 1001	011100 1001
D15.1	2F	001 01111	010111 1001	101000 1001
D16.1	30	001 10000	011011 1001	100100 1001
D17.1	31	001 10001	100011 1001	100011 1001
D18.1	32	001 10010	010011 1001	010011 1001
D19.1	33	001 10011	110010 1001	110010 1001
D20.1	34	001 10100	001011 1001	001011 1001
D21.1	35	001 10101	101010 1001	101010 1001
D22.1	36	001 10110	011010 1001	011010 1001
D23.1	37	001 10111	111010 1001	000101 1001
D24.1	38	001 11000	110011 1001	001100 1001
D25.1	39	001 11001	100110 1001	100110 1001
D26.1	3A	001 11010	010110 1001	010110 1001
D27.1	3B	001 11011	110110 1001	001001 1001

(continued)

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Table 36–1b—Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +
			abcdei fghj	abcdei fghj
D28.1	3C	001 11100	001110 1001	001110 1001
D29.1	3D	001 11101	101110 1001	010001 1001
D30.1	3E	001 11110	011110 1001	100001 1001
D31.1	3F	001 11111	101011 1001	010100 1001
D0.2	40	010 00000	100111 0101	011000 0101
D1.2	41	010 00001	011101 0101	100010 0101
D2.2	42	010 00010	101101 0101	010010 0101
D3.2	43	010 00011	110001 0101	110001 0101
D4.2	44	010 00100	110101 0101	001010 0101
D5.2	45	010 00101	101001 0101	101001 0101
D6.2	46	010 00110	011001 0101	011001 0101
D7.2	47	010 00111	111000 0101	000111 0101
D8.2	48	010 01000	111001 0101	000110 0101
D9.2	49	010 01001	100101 0101	100101 0101
D10.2	4A	010 01010	010101 0101	010101 0101
D11.2	4B	010 01011	110100 0101	110100 0101
D12.2	4C	010 01100	001101 0101	001101 0101
D13.2	4D	010 01101	101100 0101	101100 0101
D14.2	4E	010 01110	011100 0101	011100 0101
D15.2	4F	010 01111	010111 0101	101000 0101
D16.2	50	010 10000	011011 0101	100100 0101
D17.2	51	010 10001	100011 0101	100011 0101
D18.2	52	010 10010	010011 0101	010011 0101
D19.2	53	010 10011	110010 0101	110010 0101
D20.2	54	010 10100	001011 0101	001011 0101
D21.2	55	010 10101	101010 0101	101010 0101
D22.2	56	010 10110	011010 0101	011010 0101
D23.2	57	010 10111	111010 0101	000101 0101
D24.2	58	010 11000	110011 0101	001100 0101
D25.2	59	010 11001	100110 0101	100110 0101
D26.2	5A	010 11010	010110 0101	010110 0101
D27.2	5B	010 11011	110110 0101	001001 0101
D28.2	5C	010 11100	001110 0101	001110 0101
D29.2	5D	010 11101	101110 0101	010001 0101
D30.2	5E	010 11110	011110 0101	100001 0101
D31.2	5F	010 11111	101011 0101	010100 0101
D0.3	60	011 00000	100111 0011	011000 1100
D1.3	61	011 00001	011101 0011	100010 1100
D2.3	62	011 00010	101101 0011	010010 1100
D3.3	63	011 00011	110001 1100	110001 0011
D4.3	64	011 00100	110101 0011	001010 1100
D5.3	65	011 00101	101001 1100	101001 0011
D6.3	66	011 00110	011001 1100	011001 0011
D7.3	67	011 00111	111000 1100	000111 0011
D8.3	68	011 01000	111001 0011	000110 1100
D9.3	69	011 01001	100101 1100	100101 0011
D10.3	6A	011 01010	010101 1100	010101 0011
D11.3	6B	011 01011	110100 1100	110100 0011
D12.3	6C	011 01100	001101 1100	001101 0011
D13.3	6D	011 01101	101100 1100	101100 0011
D14.3	6E	011 01110	011100 1100	011100 0011
D15.3	6F	011 01111	010111 0011	101000 1100
D16.3	70	011 10000	011011 0011	100100 1100
D17.3	71	011 10001	100011 1100	100011 0011
D18.3	72	011 10010	010011 1100	010011 0011
D19.3	73	011 10011	110010 1100	110010 0011
D20.3	74	011 10100	001011 1100	001011 0011
D21.3	75	011 10101	101010 1100	101010 0011
D22.3	76	011 10110	011010 1100	011010 0011
D23.3	77	011 10111	111010 0011	000101 1100

(continued)

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Table 36–1c—Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +
			abcdei fghj	abcdei fghj
D24.3	78	011 11000	110011 0011	001100 1100
D25.3	79	011 11001	100110 1100	100110 0011
D26.3	7A	011 11010	010110 1100	010110 0011
D27.3	7B	011 11011	110110 0011	001001 1100
D28.3	7C	011 11100	001110 1100	001110 0011
D29.3	7D	011 11101	101110 0011	010001 1100
D30.3	7E	011 11110	011110 0011	100001 1100
D31.3	7F	011 11111	101011 0011	010100 1100
D0.4	80	100 00000	100111 0010	011000 1101
D1.4	81	100 00001	011101 0010	100010 1101
D2.4	82	100 00010	101101 0010	010010 1101
D3.4	83	100 00011	110001 1101	110001 0010
D4.4	84	100 00100	110101 0010	001010 1101
D5.4	85	100 00101	101001 1101	101001 0010
D6.4	86	100 00110	011001 1101	011001 0010
D7.4	87	100 00111	111000 1101	000111 0010
D8.4	88	100 01000	111001 0010	000110 1101
D9.4	89	100 01001	100101 1101	100101 0010
D10.4	8A	100 01010	010101 1101	010101 0010
D11.4	8B	100 01011	110100 1101	110100 0010
D12.4	8C	100 01100	001101 1101	001101 0010
D13.4	8D	100 01101	101100 1101	101100 0010
D14.4	8E	100 01110	011100 1101	011100 0010
D15.4	8F	100 01111	010111 0010	101000 1101
D16.4	90	100 10000	011011 0010	100100 1101
D17.4	91	100 10001	100011 1101	100011 0010
D18.4	92	100 10010	010011 1101	010011 0010
D19.4	93	100 10011	110010 1101	110010 0010
D20.4	94	100 10100	001011 1101	001011 0010
D21.4	95	100 10101	101010 1101	101010 0010
D22.4	96	100 10110	011010 1101	011010 0010
D23.4	97	100 10111	111010 0010	000101 1101
D24.4	98	100 11000	110011 0010	001100 1101
D25.4	99	100 11001	100110 1101	100110 0010
D26.4	9A	100 11010	010110 1101	010110 0010
D27.4	9B	100 11011	110110 0010	001001 1101
D28.4	9C	100 11100	001110 1101	001110 0010
D29.4	9D	100 11101	101110 0010	010001 1101
D30.4	9E	100 11110	011110 0010	100001 1101
D31.4	9F	100 11111	101011 0010	010100 1101
D0.5	A0	101 00000	100111 1010	011000 1010
D1.5	A1	101 00001	011101 1010	100010 1010
D2.5	A2	101 00010	101101 1010	010010 1010
D3.5	A3	101 00011	110001 1010	110001 1010
D4.5	A4	101 00100	110101 1010	001010 1010
D5.5	A5	101 00101	101001 1010	101001 1010
D6.5	A6	101 00110	011001 1010	011001 1010
D7.5	A7	101 00111	111000 1010	000111 1010
D8.5	A8	101 01000	111001 1010	000110 1010
D9.5	A9	101 01001	100101 1010	100101 1010
D10.5	AA	101 01010	010101 1010	010101 1010
D11.5	AB	101 01011	110100 1010	110100 1010
D12.5	AC	101 01100	001101 1010	001101 1010
D13.5	AD	101 01101	101100 1010	101100 1010
D14.5	AE	101 01110	011100 1010	011100 1010
D15.5	AF	101 01111	010111 1010	101000 1010
D16.5	B0	101 10000	011011 1010	100100 1010
D17.5	B1	101 10001	100011 1010	100011 1010
D18.5	B2	101 10010	010011 1010	010011 1010
D19.5	B3	101 10011	110010 1010	110010 1010

(continued)

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Table 36–1d—Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +
			abcdei fghj	abcdei fghj
D20.5	B4	101 10100	001011 1010	001011 1010
D21.5	B5	101 10101	101010 1010	101010 1010
D22.5	B6	101 10110	011010 1010	011010 1010
D23.5	B7	101 10111	111010 1010	000101 1010
D24.5	B8	101 11000	110011 1010	001100 1010
D25.5	B9	101 11001	100110 1010	100110 1010
D26.5	BA	101 11010	010110 1010	010110 1010
D27.5	BB	101 11011	110110 1010	001001 1010
D28.5	BC	101 11100	001110 1010	001110 1010
D29.5	BD	101 11101	101110 1010	010001 1010
D30.5	BE	101 11110	011110 1010	100001 1010
D31.5	BF	101 11111	101011 1010	010100 1010
D0.6	C0	110 00000	100111 0110	011000 0110
D1.6	C1	110 00001	011101 0110	100010 0110
D2.6	C2	110 00010	101101 0110	010010 0110
D3.6	C3	110 00011	110001 0110	110001 0110
D4.6	C4	110 00100	110101 0110	001010 0110
D5.6	C5	110 00101	101001 0110	101001 0110
D6.6	C6	110 00110	011001 0110	011001 0110
D7.6	C7	110 00111	111000 0110	000111 0110
D8.6	C8	110 01000	111001 0110	000110 0110
D9.6	C9	110 01001	100101 0110	100101 0110
D10.6	CA	110 01010	010101 0110	010101 0110
D11.6	CB	110 01011	110100 0110	110100 0110
D12.6	CC	110 01100	001101 0110	001101 0110
D13.6	CD	110 01101	101100 0110	101100 0110
D14.6	CE	110 01110	011100 0110	011100 0110
D15.6	CF	110 01111	010111 0110	101000 0110
D16.6	D0	110 10000	011011 0110	100100 0110
D17.6	D1	110 10001	100011 0110	100011 0110
D18.6	D2	110 10010	010011 0110	010011 0110
D19.6	D3	110 10011	110010 0110	110010 0110
D20.6	D4	110 10100	001011 0110	001011 0110
D21.6	D5	110 10101	101010 0110	101010 0110
D22.6	D6	110 10110	011010 0110	011010 0110
D23.6	D7	110 10111	111010 0110	000101 0110
D24.6	D8	110 11000	110011 0110	001100 0110
D25.6	D9	110 11001	100110 0110	100110 0110
D26.6	DA	110 11010	010110 0110	010110 0110
D27.6	DB	110 11011	110110 0110	001001 0110
D28.6	DC	110 11100	001110 0110	001110 0110
D29.6	DD	110 11101	101110 0110	010001 0110
D30.6	DE	110 11110	011110 0110	100001 0110
D31.6	DF	110 11111	101011 0110	010100 0110
D0.7	E0	111 00000	100111 0001	011000 1110
D1.7	E1	111 00001	011101 0001	100010 1110
D2.7	E2	111 00010	101101 0001	010010 1110
D3.7	E3	111 00011	110001 1110	110001 0001
D4.7	E4	111 00100	110101 0001	001010 1110
D5.7	E5	111 00101	101001 1110	101001 0001
D6.7	E6	111 00110	011001 1110	011001 0001
D7.7	E7	111 00111	111000 1110	000111 0001
D8.7	E8	111 01000	111001 0001	000110 1110
D9.7	E9	111 01001	100101 1110	100101 0001
D10.7	EA	111 01010	010101 1110	010101 0001
D11.7	EB	111 01011	110100 1110	110100 1000
D12.7	EC	111 01100	001101 1110	001101 0001
D13.7	ED	111 01101	101100 1110	101100 1000
D14.7	EE	111 01110	011100 1110	011100 1000
D15.7	EF	111 01111	010111 0001	101000 1110

(continued)

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Table 36–1e—Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +
			abcdei fghj	abcdei fghj
D16.7	F0	111 10000	011011 0001	100100 1110
D17.7	F1	111 10001	100011 0111	100011 0001
D18.7	F2	111 10010	010011 0111	010011 0001
D19.7	F3	111 10011	110010 1110	110010 0001
D20.7	F4	111 10100	001011 0111	001011 0001
D21.7	F5	111 10101	101010 1110	101010 0001
D22.7	F6	111 10110	011010 1110	011010 0001
D23.7	F7	111 10111	111010 0001	000101 1110
D24.7	F8	111 11000	110011 0001	001100 1110
D25.7	F9	111 11001	100110 1110	100110 0001
D26.7	FA	111 11010	010110 1110	010110 0001
D27.7	FB	111 11011	110110 0001	001001 1110
D28.7	FC	111 11100	001110 1110	001110 0001
D29.7	FD	111 11101	101110 0001	010001 1110
D30.7	FE	111 11110	011110 0001	100001 1110
D31.7	FF	111 11111	101011 0001	010100 1110

(concluded)

Table 36–2—Valid special code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +	Notes
			abcdei fghj	abcdei fghj	
K28.0	1C	000 11100	001111 0100	110000 1011	1
K28.1	3C	001 11100	001111 1001	110000 0110	1,2
K28.2	5C	010 11100	001111 0101	110000 1010	1
K28.3	7C	011 11100	001111 0011	110000 1100	1
K28.4	9C	100 11100	001111 0010	110000 1101	1
K28.5	BC	101 11100	001111 1010	110000 0101	2
K28.6	DC	110 11100	001111 0110	110000 1001	1
K28.7	FC	111 11100	001111 1000	110000 0111	1,2
K23.7	F7	111 10111	111010 1000	000101 0111	
K27.7	FB	111 11011	110110 1000	001001 0111	
K29.7	FD	111 11101	101110 1000	010001 0111	
K30.7	FE	111 11110	011110 1000	100001 0111	

NOTE 1—Reserved.

NOTE 2—Contains a comma.

36.2.4.7.1 Ordered set rules

Ordered sets are specified according to the following rules:

a) Ordered sets consist of either one, two, or four code-groups.
b) The first code-group of all ordered sets is always a special code-group.
c) The second code-group of all multi-code-group ordered sets is always a data code-group. The second code-group is used to distinguish the ordered set from all other ordered sets. The second code-group provides a high bit transition density.

Table 36–3 lists the defined ordered sets.

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Table 36–3—Defined ordered sets

Code	Ordered Set	Number of Code-Groups	Encoding
/C/	**Configuration**		Alternating /C1/ and /C2/
/C1/	Configuration 1	4	/K28.5/D21.5/Config_Reg[a]
/C2/	Configuration 2	4	/K28.5/D2.2/Config_Reg[a]
/I/	**IDLE**		Correcting /I1/, Preserving /I2/
/I1/	IDLE 1	2	/K28.5/D5.6/
/I2/	IDLE 2	2	/K28.5/D16.2/
	Encapsulation		
/R/	Carrier_Extend	1	/K23.7/
/S/	Start_of_Packet	1	/K27.7/
/T/	End_of_Packet	1	/K29.7/
/V/	Error_Propagation	1	/K30.7/
/LI/	**LPI**		Correcting /LI1/, Preserving /LI2/
/LI1/	LPI 1	2	/K28.5/D6.5/
/LI2/	LPI 2	2	/K28.5/D26.4/

[a]Two data code-groups representing the Config_Reg value.

36.2.4.8 /K28.5/ code-group considerations

The /K28.5/ special code-group is chosen as the first code-group of all ordered sets that are signaled repeatedly and for the purpose of allowing a receiver to synchronize to the incoming bit stream (i.e., /C/ and /I/), for the following reasons:

a) Bits abcdeif make up a comma. The comma can be used to easily find and verify code-group and ordered set boundaries of the rx_bit stream.
b) Bits ghj of the encoded code-group present the maximum number of transitions, simplifying receiver acquisition of bit synchronization.

36.2.4.9 Comma considerations

The seven bit comma string is defined as either b'0011111' (comma+) or b'1100000' (comma-). The /I/ and /C/ ordered sets and their associated protocols are specified to ensure that comma+ is transmitted with either equivalent or greater frequency than comma- for the duration of their transmission. This is done to ensure compatibility with common components.

The comma contained within the /K28.1/, /K28.5/, and /K28.7/ special code-groups is a singular bit pattern, which, in the absence of transmission errors, cannot appear in any other location of a code-group and cannot be generated across the boundaries of any two adjacent code-groups with the following exception:

The /K28.7/ special code-group is used by 1000BASE-X for diagnostic purposes only (see Annex 36A). This code-group, if followed by any of the following special or data code-groups: /K28.x/, /D3.x/, /D11.x/, /D12.x/, /D19.x/, /D20.x/, or /D28.x/, where x is a value in the range 0 to 7, inclusive, causes a comma to be

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generated across the boundaries of the two adjacent code-groups. A comma across the boundaries of any two adjacent code-groups may cause code-group realignment (see 36.3.2.4).

36.2.4.10 Configuration (/C/)

Configuration, defined as the continuous repetition of the ordered sets /C1/ and /C2/, is used to convey the 16-bit Configuration Register (Config_Reg) to the link partner. See Clause 37 for a description of the Config_Reg contents.

The ordered sets, /C1/ and /C2/, are defined in Table 36–3. The /C1/ ordered set is defined such that the running disparity at the end of the first two code-groups is opposite that of the beginning running disparity. The /C2/ ordered set is defined such that the running disparity at the end of the first two code-groups is the same as the beginning running disparity. For a constant Config_Reg value, the running disparity after transmitting the sequence /C1/C2/ will be the opposite of what it was at the start of the sequence. This ensures that K28.5s containing comma+ will be sent during configuration.

36.2.4.11 Data (/D/)

A data code-group, when not used to distinguish or convey information for a defined ordered set, conveys one octet of arbitrary data between the GMII and the PCS. The sequence of data code-groups is arbitrary, where any data code-group can be followed by any other data code-group. Data code-groups are coded and decoded but not interpreted by the PCS. Successful decoding of the data code-groups depends on proper receipt of the Start_of_Packet delimiter, as defined in 36.2.4.14 and the checking of validity, as defined in 36.2.4.6.

36.2.4.12 IDLE (/I/)

IDLE ordered sets (/I/) are transmitted continuously and repetitively whenever the GMII is idle (TX_EN and TX_ER are both inactive). /I/ provides a continuous fill pattern to establish and maintain clock synchronization. /I/ is emitted from, and interpreted by, the PCS. /I/ consists of one or more consecutively transmitted /I1/ or /I2/ ordered sets, as defined in Table 36–3.

The /I1/ ordered set is defined such that the running disparity at the end of the transmitted /I1/ is opposite that of the beginning running disparity. The /I2/ ordered set is defined such that the running disparity at the end of the transmitted /I2/ is the same as the beginning running disparity. The first /I/ following a packet or Configuration ordered set restores the current positive or negative running disparity to a negative value. All subsequent /I/s are /I2/ to ensure negative ending running disparity.

Distinct carrier events are separated by /I/s.

Implementations of this standard may benefit from the ability to add or remove /I2/ from the code-group stream one /I2/ at a time without altering the beginning running disparity associated with the code-group subsequent to the removed /I2/.

A received ordered set that consists of two code-groups, the first of which is /K28.5/ and the second of which is a data code-group other than /D21.5/ or /D2.2/ (or /D6.5/ or /D26.4/ to support EEE capability), is treated as an /I/ ordered set.

36.2.4.13 Low Power Idle (LPI)

LPI is transmitted in the same manner as IDLE. LPI ordered sets (/LI/) are transmitted continuously and repetitively whenever the GMII is indicating “Assert LPI”. See 35.2.2.6 and 35.2.2.10 for corresponding GMII definitions.

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36.2.4.14 Start_of_Packet (SPD) delimiter

A Start_of_Packet delimiter (SPD) is used to delineate the starting boundary of a data transmission sequence and to authenticate carrier events. Upon each fresh assertion of TX_EN by the GMII, and subsequent to the completion of PCS transmission of the current ordered set, the PCS replaces the current octet of the MAC preamble with SPD. Upon initiation of packet reception, the PCS replaces the received SPD delimiter with the data octet value associated with the first preamble octet. A SPD delimiter consists of the code-group /S/, as defined in Table 36–3.

SPD follows /I/ for a single packet or the first packet in a burst.

SPD follows /R/ for the second and subsequent packets of a burst.

36.2.4.15 End_of_Packet delimiter (EPD)

An End_of_Packet delimiter (EPD) is used to delineate the ending boundary of a packet. The EPD is transmitted by the PCS following each deassertion of TX_EN on the GMII, which follows the last data octet comprising the FCS of the MAC packet. On reception, EPD is interpreted by the PCS as terminating a packet. A EPD delimiter consists of the code-groups /T/R/R/ or /T/R/K28.5/. The code-group /T/ is defined in Table 36–3. See 36.2.4.16 for the definition of code-groups used for /R/. /K28.5/ normally occurs as the first code-group of the /I/ ordered set. See 36.2.4.12 for the definition of code-groups used for /I/.

The receiver considers the MAC interpacket gap (IPG) to have begun two octets prior to the transmission of /I/. For example, when a packet is terminated by EPD, the /T/R/ portion of the EPD occupies part of the region considered by the MAC to be the IPG.

36.2.4.15.1 EPD rules

a) The PCS transmits a /T/R/ following the last data octet from the MAC;
b) If the MAC indicates carrier extension to the PCS, Carrier_Extend rules are in effect. See 36.2.4.16.1;
c) If the MAC does not indicate carrier extension to the PCS, perform the following:
    1) If /R/ is transmitted in an even-numbered code-group position, the PCS appends a single additional /R/ to the code-group stream to ensure that the subsequent /I/ is aligned on an even-numbered code-group boundary and EPD transmission is complete;
    2) The PCS transmits /I/.

36.2.4.16 Carrier_Extend (/R/)

Carrier_Extend (/R/) is used for the following purposes:

a) Carrier extension: Used by the MAC to extend the duration of the carrier event. When used for this purpose, carrier extension is emitted from and interpreted by the MAC and coded to and decoded from the corresponding code-group by the PCS. In order to extend carrier, the GMII has to deassert TX_EN. The deassertion of TX_EN and simultaneous assertion of TX_ER causes the PCS to emit an /R/ with a two-octet delay, which gives the PCS time to complete its EPD before commencing transmissions. The number of /R/ code-groups emitted from the PCS equals the number of GMII GTX_CLK periods during which it extends carrier;
b) Packet separation: Carrier extension is used by the MAC to separate packets within a burst of packets. When used for this purpose, carrier extension is emitted from and interpreted by the MAC and coded to and decoded from the corresponding code-group by the PCS;
c) EPD2: The first /R/ following the /T/ in the End_of_Packet delimiters /T/R/I/ or /T/R/R/I/;

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d) EPD3: The second /R/ following the /T/ in the End_of_Packet delimiter /T/R/R/I/. This /R/ is used, if necessary, to pad the only or last packet of a burst of packets so that the subsequent /I/ is aligned on an even-numbered code-group boundary. When used for this purpose, Carrier_Extend is emitted from, and interpreted by, the PCS. An EPD of /T/R/R/ results in one /R/ being delivered to the PCS client (see 36.2.4.15.1).

Carrier_Extend consists of one or more consecutively transmitted /R/ ordered sets, as defined in Table 36–3.

36.2.4.16.1 Carrier_Extend rules

a) If the MAC indicates carrier extension to the PCS, the initial /T/R/ is followed by one /R/ for each octet of carrier extension received from the MAC;
b) If the last /R/ is transmitted in an even-numbered code-group position, the PCS appends a single additional /R/ to the code-group stream to ensure that the subsequent /I/ is aligned on an even-numbered code-group boundary.

36.2.4.17 Error_Propagation (/V/)

Error_Propagation (/V/) indicates that the PCS client wishes to indicate a transmission error to its peer entity. The normal use of Error_Propagation is for repeaters to propagate received errors. /V/ is emitted from the PCS, at the request of the PCS client through the use of the TX_ER signal, as described in Clause 35. Error_Propagation is emitted from, and interpreted by, the PCS. Error_Propagation consists of the ordered set /V/, as defined in Table 36–3.

The presence of Error_Propagation or any invalid code-group on the medium denotes a collision artifact or an error condition. Invalid code-groups are not intentionally transmitted onto the medium by DTEs. The PCS processes and conditionally indicates the reception of /V/ or an invalid code-group on the GMII as false carrier, data errors, or carrier extend errors, depending on its current context.

36.2.4.18 Encapsulation

The 1000BASE-X PCS accepts packets from the MAC through the Reconciliation sublayer and GMII. Due to the continuously signaled nature of the underlying PMA, and the encoding performed by the PCS, the 1000BASE-X PCS encapsulates MAC frames into a code-group stream. The PCS decodes the code-group stream received from the PMA, extracts packets from it, and passes the packets to the MAC via the Reconciliation sublayer and GMII.

Figure 36–4 depicts the PCS encapsulation of a MAC packet based on GMII signals.

36.2.4.19 Mapping between GMII, PCS and PMA

Figure 36–3 depicts the mapping of the octet-wide data path of the GMII to the ten-bit-wide code-groups of the PCS, and the one-bit paths of the PMA/PMD interface.

The PCS encodes an octet received from the GMII into a ten-bit code-group, according to Figure 36–3. Code-groups are serialized into a tx_bit stream by the PMA and passed to the PMD for transmission on the underlying medium, according to Figure 36–3. The first transmitted tx_bit is tx_code-group<0>, and the last tx_bit transmitted is tx_code-group<9>. There is no numerical significance ascribed to the bits within a code-group; that is, the code-group is simply a ten-bit pattern that has some predefined interpretation.

Similarly, the PMA deserializes rx_bits received from the PMD, according to Figure 36–3. The PCS Receive process converts rx_code-group<9:0>'s into GMII data octets, according to 36.2.5.2.2.

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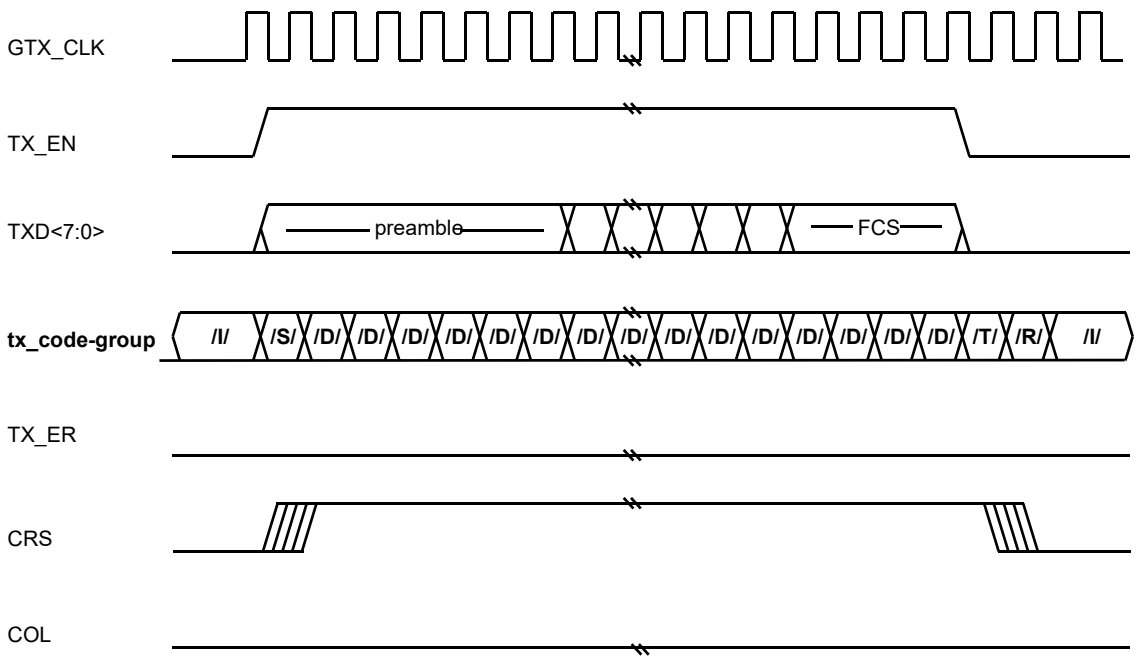

Figure 36–4—PCS encapsulation

36.2.5 Detailed functions and state diagrams

The notation used in the state diagrams in this clause follow the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

Timeless states are employed as an editorial convenience to facilitate the distribution of transition conditions from prior states. No actions are taken within these states. Exit conditions are evaluated for timeless states. Timeless states are as follows:

a) PCS transmit ordered set state TX_PACKET;
b) PCS transmit code-group state GENERATE_CODE_GROUPS;
c) PCS transmit code-group state IDLE_DISPARITY_TEST;
d) PCS receive state RECEIVE;
e) PCS receive state EPD2_CHECK_END.

36.2.5.1 State variables

36.2.5.1.1 Notation conventions

/x/

Denotes the constant code-group specified in 36.2.5.1.2 (valid code-groups have to follow the rules of running disparity as per 36.2.4.5 and 36.2.4.6).

[/x/]

Denotes the latched received value of the constant code-group (/x/) specified in 36.2.5.1.2 and conveyed by the SYNC_UNITDATA.indicate message described in 36.2.5.1.6.

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36.2.5.1.2 Constants

/C/
: The Configuration ordered set group, comprising either the /C1/ or /C2/ ordered set, as specified in 36.2.4.10. Conveys the Config_Reg value as tx_Config_Reg<D15:D0> for the PCS Transmit process and rx_Config_Reg<D15:D0> for the PCS Receive process.

/COMMA/
: The set of special code-groups which include a comma as specified in 36.2.4.9 and listed in Table 36–2.

/D/
: The set of 256 code-groups corresponding to valid data, as specified in 36.2.4.11.

/Dx.y/
: One of the set of 256 code-groups corresponding to valid data, as specified in 36.2.4.11.

/I/
: The IDLE ordered set group, comprising either the /I1/ or /I2/ ordered sets, as specified in 36.2.4.12.

/INVALID/
: The set of invalid data or special code-groups, as specified in 36.2.4.6.

/Kx.y/
: One of the set of 12 code-groups corresponding to valid special code-groups, as specified in Table 36–2.

/R/
: The code-group used as either: End_of_Packet delimiter part 2; End_of_Packet delimiter part 3; Carrier_Extend; and /I/ alignment.

/S/
: The code-group corresponding to the Start_of_Packet delimiter (SPD) as specified in 36.2.4.14.

/T/
: The code-group used for the End_of_Packet delimiter part 1.

/V/
: The Error_Propagation code-group, as specified in 36.2.4.17.

The following constant is used only for the EEE capability:

/LI/
: The LP_IDLE ordered set group, comprising either the /LI1/ or /LI2/ ordered sets, as specified in 36.2.4.13.

36.2.5.1.3 Variables

cgbad
: Alias for the following terms: ((rx_code-group∈/INVALID/) + (rx_code-group=/COMMA/ *rx_even=TRUE)) * PMA_UNITDATA.indication

cggood
: Alias for the following terms: !((rx_code-group∈/INVALID/) + (rx_code-group=/COMMA/ *rx_even=TRUE)) * PMA_UNITDATA.indication

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COL

The COL signal of the GMII as specified in Clause 35.

CRS

The CRS signal of the GMII as specified in Clause 35.

EVEN

The latched state of the rx_even variable, when rx_even=TRUE, as conveyed by the SYNC_UNITDATA.indicate message described in 36.2.5.1.6.

mr_loopback

A Boolean that indicates the enabling and disabling of data being looped back through the PHY. Loopback of data through the PHY is enabled when Control register bit 0.14 is set to one.

Values: FALSE; Loopback through the PHY is disabled.
TRUE; Loopback through the PHY is enabled.

mr_main_reset

Controls the resetting of the PCS via Control Register bit 0.15.

Values: FALSE; Do not reset the PCS.
TRUE; Reset the PCS.

ODD

The latched state of the rx_even variable, when rx_even=FALSE, as conveyed by the SYNC_UNITDATA.indicate message described in 36.2.5.1.6.

power_on

Condition that is true until such time as the power supply for the device that contains the PCS has reached the operating region. The condition is also true when the device has low power mode set via Control register bit 0.11.

Values: FALSE; The device is completely powered (default).
TRUE; The device has not been completely powered.

NOTE—Power_on evaluates to its default value in each state where it is not explicitly set.

receiving

A Boolean set by the PCS Receive process to indicate carrier activity. Used by the Carrier Sense process, and also interpreted by the PCS Transmit process for indicating a collision. (See also 36.2.5.1.4, carrier_detect(x).)

Values: TRUE; Carrier being received.
FALSE; Carrier not being received.

repeater_mode

A Boolean used to make the assertion of Carrier Sense occur only in response to receive activity when the PCS is used in a CSMA/CD repeater. This variable is set to TRUE in a repeater application, and set to FALSE in all other applications.

Values: TRUE; Allows the assertion of CRS in response to receive activity only.
FALSE; Allows the assertion of CRS in response to either transmit or receive activity.

rx_bit

A binary parameter conveyed by the PMD_UNITDATA.indication service primitive, as specified in 38.1.1.2, to the PMA.

Values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

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rx_code-group<9:0>

A 10-bit vector represented by the most recently received code-group from the PMA. The element rx_code-group<0> is the least recently received (oldest) rx_bit; rx_code-group<9> is the most recently received rx_bit (newest). When code-group alignment has been achieved, this vector contains precisely one code-group.

rx_Config_Reg<D15:D0>

A 16-bit array that contains the data bits received from a /C/ ordered set as defined in 36.2.4.10. Conveyed by the PCS Receive process to the PCS Auto-Negotiation process. The format of the data bits is context dependent, relative to the state of the Auto-Negotiation function, and is presented in 37.2.1.1 and 37.2.4.3.1. For each element within the array:

Values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

RX_DV

The RX_DV signal of the GMII as specified in Clause 35. Set by the PCS Receive process.

RX_ER

The RX_ER signal of the GMII as specified in Clause 35. Set by the PCS Receive process.

rx_even

A Boolean set by the PCS Synchronization process to designate received code-groups as either even- or odd-numbered code-groups as specified in 36.2.4.2.

Values: TRUE; Even-numbered code-group being received.
FALSE; Odd-numbered code-group being received.

RXD<7:0>

The RXD<7:0> signal of the GMII as specified in Clause 35. Set by the PCS Receive process.

signal_detect

A Boolean set by the PMD continuously via the PMD_SIGNAL.indication(signal_detect) message to indicate the status of the incoming link signal.

Values: FAIL; A signal is not present on the link.
OK; A signal is present on the link.

sync_status

A parameter set by the PCS Synchronization process to reflect the status of the link as viewed by the receiver. The values of the parameter are defined for code_sync_status. The equation for this parameter is

sync_status = code_sync_status + rx_lpi_active

NOTE—If EEE is not supported, the variable rx_lpi_active is always false, and this variable is identical to code_sync_status controlled by the synchronization state diagram.

transmitting

A Boolean set by the PCS Transmit process to indicate that packet transmission is in progress. Used by the Carrier Sense process and internally by the PCS Transmit process for indicating a collision.

Values: TRUE; The PCS is transmitting a packet.
FALSE; The PCS is not transmitting a packet.

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tx_bit

A binary parameter used to convey data from the PMA to the PMD via the PMD_UNITDATA.request service primitive as specified in 38.1.1.1.

Values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

tx_code-group<9:0>

A vector of bits representing one code-group, as specified in Tables 36–1a–e or 36–2, which has been prepared for transmission by the PCS Transmit process. This vector is conveyed to the PMA as the parameter of a PMD_UNITDATA.request(tx_bit) service primitive. The element tx_code-group<0> is the first tx_bit transmitted; tx_code-group<9> is the last tx_bit transmitted.

tx_Config_Reg<D15:D0>

A 16-bit array that contains the data bits to be transmitted in a /C/ ordered set as defined in 36.2.4.10. Conveyed by the PCS Auto-Negotiation process to the PCS Transmit process. The format of the data bits is context dependent, relative to the state of the Auto-Negotiation function, and is presented in 37.2.1.1 and 37.2.4.3.1. For each element within the array:

Values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

tx_disparity

A Boolean set by the PCS Transmit process to indicate the running disparity at the end of code-group transmission as a binary value. Running disparity is described in 36.2.4.3.

Values: POSITIVE
NEGATIVE

TX_EN

The TX_EN signal of the GMII as specified in Clause 35.

TX_ER

The TX_ER signal of the GMII as specified in Clause 35.

tx_even

A Boolean set by the PCS Transmit process to designate transmitted code-groups as either even- or odd-numbered code-groups as specified in 36.2.4.2.

Values: TRUE; Even-numbered code-group being transmitted.
FALSE; Odd-numbered code-group being transmitted.

tx_o_set

One of the following defined ordered sets: /C/, /T/, /R/, /I/, /LI/, /S/, /V/, or the code-group /D/.

TXD<7:0>

The TXD<7:0> signal of the GMII as specified in Clause 35.

xmit

Defined in 37.3.1.1.

The following variables are used only for the EEE capability:

assert_lpidle

Alias used for the optional LPI function, consisting of the following terms:

(TX_EN=FALSE * TX_ER=TRUE * (TXD<7:0>=0x01))

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code_sync_status

A parameter set by the PCS Synchronization process to reflect the status of the link as viewed by the receiver.

Values: FAIL; The receiver is not synchronized to code-group boundaries.
OK; The receiver is synchronized to code-group boundaries.

idle_d

Alias for the following terms:

SUDI(![/D21.5/] * ![/D2.2/])
that uses an alternate form to support the EEE capability:
SUDI(![/D21.5/] * ![/D2.2/] * ![/D6.5/] * ![/D26.4/])

rx_lpi_active

A Boolean variable that is set to TRUE when the receiver is in a low power state and set to FALSE when it is in an active state and capable of receiving data.

rx_quiet

A Boolean variable set to TRUE while in the RX_QUIET state and set to FALSE otherwise.

tx_quiet

A Boolean variable set to TRUE when the transmitter is in the TX_QUIET state and set to FALSE otherwise. When set to TRUE, the PMD will disable the transmitter as described in 70.6.5.

36.2.5.1.4 Functions

carrier_detect

In the PCS Receive process, this function uses for input the latched code-group ([/x/]) and latched rx_even (EVEN/ODD) parameters of the SYNC_UNITDATA.indicate message from the PCS Synchronization process. When SYNC_UNITDATA.indicate message indicates EVEN, the carrier_detect function detects carrier when either:

a) A two or more bit difference between [/x/] and both /K28.5/ encodings exists (see Table 36–2); or

b) A two to nine bit difference between [/x/] and the expected /K28.5/ (based on current running disparity) exists.

Values: TRUE; Carrier is detected.
FALSE; Carrier is not detected.

check_end

Prescient End_of_Packet and Carrier_Extend function used by the PCS Receive process to set RX_ER and RXD<7:0> signals. The check_end function returns the current and next two code-groups in rx_code-group<9:0>.

DECODE ([/x]/)

In the PCS Receive process, this function takes as its argument the latched value of rx_code-group<9:0> ([/x/]) and the current running disparity, and returns the corresponding GMII RXD<7:0>, rx_Config_Reg<D7:D0>, or rx_Config_Reg<D15:D8> octet, per Table 36–1a–e. DECODE also updates the current running disparity per the running disparity rules outlined in 36.2.4.4.

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ENCODE(x)

In the PCS Transmit process, this function takes as its argument (x), where x is a GMII TXD<7:0>, tx_Config_Reg<D7:D0>, or tx_Config_Reg<D15:D8> octet, and the current running disparity, and returns the corresponding ten-bit code-group per Table 36–1a–e. ENCODE also updates the current running disparity per Table 36–1a–e.

signal_detectCHANGE

In the PCS Synchronization process, this function monitors the signal_detect variable for a state change. The function is set upon state change detection.

Values: TRUE; A signal_detect variable state change has been detected.
FALSE; A signal_detect variable state change has not been detected (default).

NOTE—Signal_detectCHANGE is set by this function definition; it is not set explicitly in the state diagrams. Signal_detectCHANGE evaluates to its default value upon state entry.

VOID(x)

x ∈ /D/, /T/, /R/, /K28.5/. Substitutes /V/ on a per code-group basis as requested by the GMII.

If [TX_EN=FALSE * TX_ER=TRUE * TXD≠(0000 1111)],

then return /V/;

Else if [TX_EN=TRUE * TX_ER=TRUE],

then return /V/;

Else return x.

xmitCHANGE

In the PCS Transmit process, this function monitors the xmit variable for a state change. The function is set upon state change detection.

Values: TRUE; An xmit variable state change has been detected.
FALSE; An xmit variable state change has not been detected (default).

NOTE—XmitCHANGE is set by this function definition; it is not set explicitly in the state diagrams. XmitCHANGE evaluates to its default value upon entry to state TX_TEST_XMIT.

36.2.5.1.5 Counters

good_cgs

Count of consecutive valid code-groups received.

The following counter is used only for the EEE capability:

wake_error_counter

A counter that is incremented each time that the LPI receive state diagram enters the RX_WTF state indicating that a wake time fault has been detected. The counter is reflected in register 3.22 (see 45.2.3.12).

36.2.5.1.6 Messages

PMA_UNITDATA.indication(rx_code-group<9:0>)

A signal sent by the PMA Receive process conveying the next code-group received over the medium (see 36.3.1.2).

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PMA_UNITDATA.request(tx_code-group<9:0>)
A signal sent to the PMA Transmit process conveying the next code-group ready for transmission over the medium (see 36.3.1.1).

PMD_SIGNAL.indication(signal_detect)
A signal sent by the PMD to indicate the status of the signal being received on the MDI.

PUDI
Alias for PMA_UNITDATA.indication(rx_code-group<9:0>).

PUDR
Alias for PMA_UNITDATA.request(tx_code-group<9:0>).

RUDI
Alias for RX_UNITDATA.indicate(parameter).

RX_UNITDATA.indicate(parameter)
A signal sent by the PCS Receive process to the PCS Auto_Negotiation process conveying the following parameters:

Parameters: INVALID; indicates that an error condition has been detected while receiving /C/ or /I/ ordered sets;
/C/; the /C/ ordered set has been received;
/I/; the /I/ ordered set has been received.

SUDI
Alias for SYNC_UNITDATA.indicate(parameters).

SYNC_UNITDATA.indicate(parameters)
A signal sent by the PCS Synchronization process to the PCS Receive process conveying the following parameters:

Parameters: [/x/]; the latched value of the indicated code-group (/x/);
EVEN/ODD; The latched state of the rx_even variable;

Value: EVEN; Passed when the latched state of rx_even=TRUE.
ODD; Passed when the latched state of rx_even=FALSE.

TX_OSET.indicate
A signal sent to the PCS Transmit ordered set process from the PCS Transmit code-group process signifying the completion of transmission of one ordered set.

The following messages are used only for the EEE capability:

PMD_RXQUIET.request(rx_quiet)
A signal sent by the PCS/PMA LPI receive state diagram to the PMD. Note that this message is ignored by devices that do not support EEE capability.

Values: TRUE: The receiver is in a quiet state and is not expecting incoming data.
FALSE: The receiver is ready to receive data.

PMD_TXQUIET.request(tx_quiet)
A signal sent by the PCS/PMA LPI transmit state diagram to the PMD. Note that this message is ignored by devices that do not support the optional LPI mechanism.

Values: TRUE: The transmitter is in a quiet state and may cease to transmit a signal on the medium.
FALSE: The transmitter is ready to transmit data.

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36.2.5.1.7 Timers

cg_timer
: A continuous free-running timer.

  Values: The condition cg_timer_done becomes true upon timer expiration.

  Restart when: immediately after expiration; restarting the timer resets the condition cg_timer_done.

  Duration: 8 ns nominal.

  If the GMII is implemented, cg_timer shall expire synchronously with the rising edge of GTX_CLK (see tolerance required for GTX_CLK in 35.5.2.3). In the absence of a GMII, cg_timer shall expire every 8 ns ± 0.01%. In the PCS transmit code-group state diagram, the message PMA_UNITDATA.request is issued concurrently with cg_timer_done.

The following timers are used only for the EEE capability:

rx_tq_timer
: This timer is started when the PCS receiver enters the START_TQ_TIMER state. The timer terminal count is set to T_{QR}. When the timer reaches terminal count, it will set the rx_tq_timer_done = TRUE.

rx_tw_timer
: This timer is started when the PCS receiver enters the RX_WAKE state. The timer terminal count shall not exceed the maximum value of T_{WR} in Table 36–9. When the timer reaches terminal count, it will set the rx_tw_timer_done = TRUE.

rx_wf_timer
: This timer is started when the PCS receiver enters the RX_WTF state, indicating that the receiver has encountered a wake time fault. The rx_wf_timer allows the receiver an additional period in which to synchronize or return to the quiescent state before a link failure is indicated. The timer terminal count is set to T_{WTF}. When the timer reaches terminal count, it will set the rx_wf_timer_done = TRUE.

tx_ts_timer
: This timer is started when the PCS transmitter enters the TX_SLEEP state. The timer terminal count is set to T_{SL}. When the timer reaches terminal count, it will set the tx_ts_timer_done = TRUE.

tx_tq_timer
: This timer is started when the PCS transmitter enters the TX_QUIET state. The timer terminal count is set to T_{QL}. When the timer reaches terminal count, it will set the tx_tq_timer_done = TRUE.

tx_tr_timer
: This timer is started when the PCS transmitter enters the TX_REFRESH state. The timer terminal count is set to T_{UL}. When the timer reaches terminal count, it will set the tx_tr_timer_done = TRUE.

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36.2.5.2 State diagrams

36.2.5.2.1 Transmit

The PCS Transmit process is depicted in two state diagrams: PCS Transmit ordered set and PCS Transmit code-group. The PCS shall implement its Transmit process as depicted in Figure 36–5 and Figure 36–6, including compliance with the associated state variables as specified in 36.2.5.1.

The Transmit ordered set process continuously sources ordered sets to the Transmit code-group process. When initially invoked, and when the Auto-Negotiation process xmit flag indicates CONFIGURATION, the Auto-Negotiation process is invoked. When the Auto-Negotiation process xmit flag indicates IDLE, and between packets (as delimited by the GMII), /I/ is sourced. Upon the assertion of TX_EN by the GMII when the Auto-Negotiation process xmit flag indicates DATA, the SPD ordered set is sourced. Following the SPD, /D/ code-groups are sourced until TX_EN is deasserted. Following the deassertion of TX_EN, EPD ordered sets are sourced. If TX_ER is asserted when TX_EN is deasserted and carrier extend error is not indicated by TXD, /R/ ordered sets are sourced for as many GTX_CLK periods as TX_ER is asserted with a delay of two GTX_CLK periods to first source the /T/ and /R/ ordered sets. If carrier extend error is indicated by TXD during carrier extend, /V/ ordered sets are sourced. If TX_EN and TX_ER are both deasserted, the /R/ ordered set may be sourced, after which the sourcing of /I/ is resumed. If, while TX_EN is asserted, the TX_ER signal is asserted, the /V/ ordered set is sourced except when the SPD ordered set is selected for sourcing.

Collision detection is implemented by noting the occurrence of carrier receptions during transmissions, following the models of 10BASE-T and 100BASE-X.

The Transmit code-group process continuously sources tx_code-group<9:0> to the PMA based on the ordered sets sourced to it by the Transmit ordered set process. The Transmit code-group process determines the proper code-group to source based on even/odd-numbered code-group alignment, running disparity requirements, and ordered set format.

36.2.5.2.2 Receive

The PCS shall implement its Receive process as depicted in Figure 36–7a and Figure 36–7b, including compliance with the associated state variables as specified in 36.2.5.1.

The PCS Receive process continuously passes RXD<7:0> and sets the RX_DV and RX_ER signals to the GMII based on the received code-group from the PMA.

When the Auto-Negotiation process xmit flag indicates CONFIGURATION or IDLE, the PCS Receive process continuously passes /C/ and /I/ ordered sets and rx_Config_Reg<D15:D0> to the Auto-Negotiation process.

36.2.5.2.3 State variable function carrier_detect(x)

The detection of carrier on the underlying channel is used both by the MAC (via the GMII CRS signal and the Reconciliation sublayer) for deferral purposes, and by the PCS Transmit process for collision detection. A carrier event, signaled by the assertion of receiving, is indicated by the detection of a difference between the received code-group and /K28.5/ as specified in 36.2.5.1.4.

A carrier event is in error if it does not start with an SPD. The PCS Receive process performs this function by continuously monitoring incoming code-groups for specific patterns that indicate non-/I/ activity such as SPD. The detection of an SPD carrier event causes the PCS to substitute the value (01010101) for the SPD, set RXD<7:0> to this value, and assert RX_DV. The pattern substituted for the SPD is consistent with the preamble pattern expected by the MAC. The detection of a non-SPD carrier event (false carrier) causes the PCS to substitute the value (00001110) for the code-group received, set RXD<7:0> to this value, and assert RX_ER.

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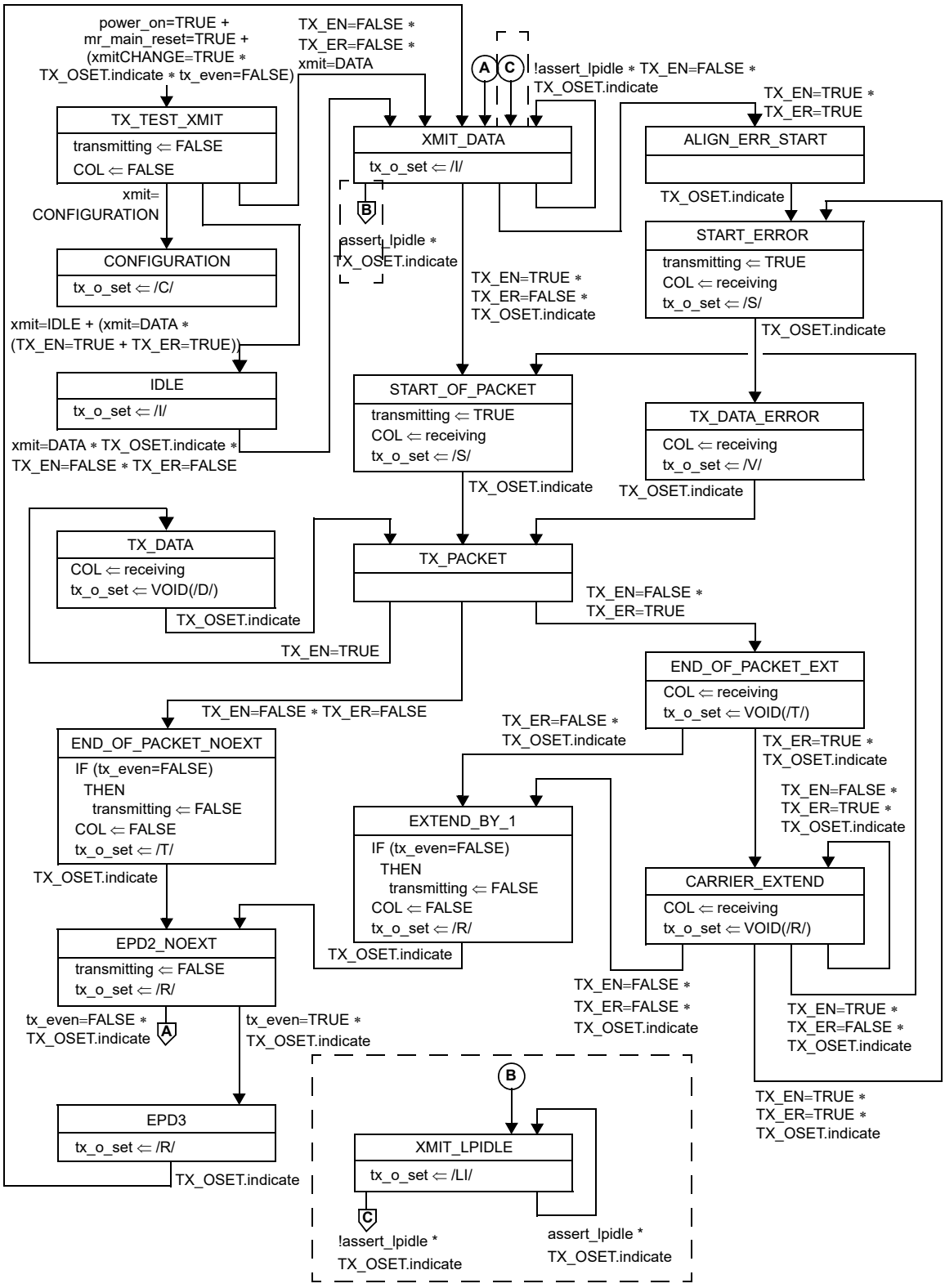

NOTE—Transitions B and C are only required for the EEE capability.

Figure 36–5—PCS transmit ordered set state diagram

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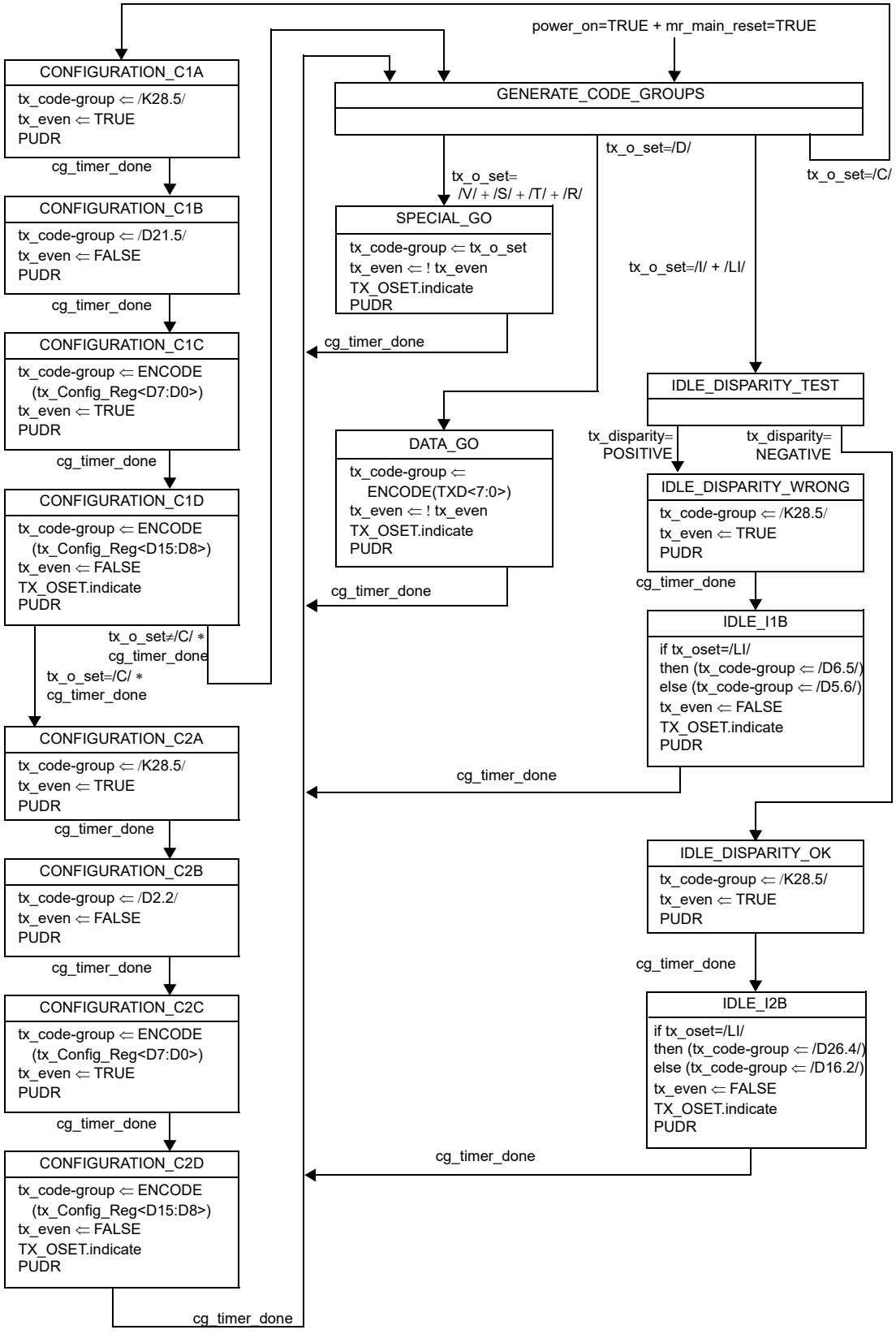

Figure 36–6—PCS transmit code-group state diagram

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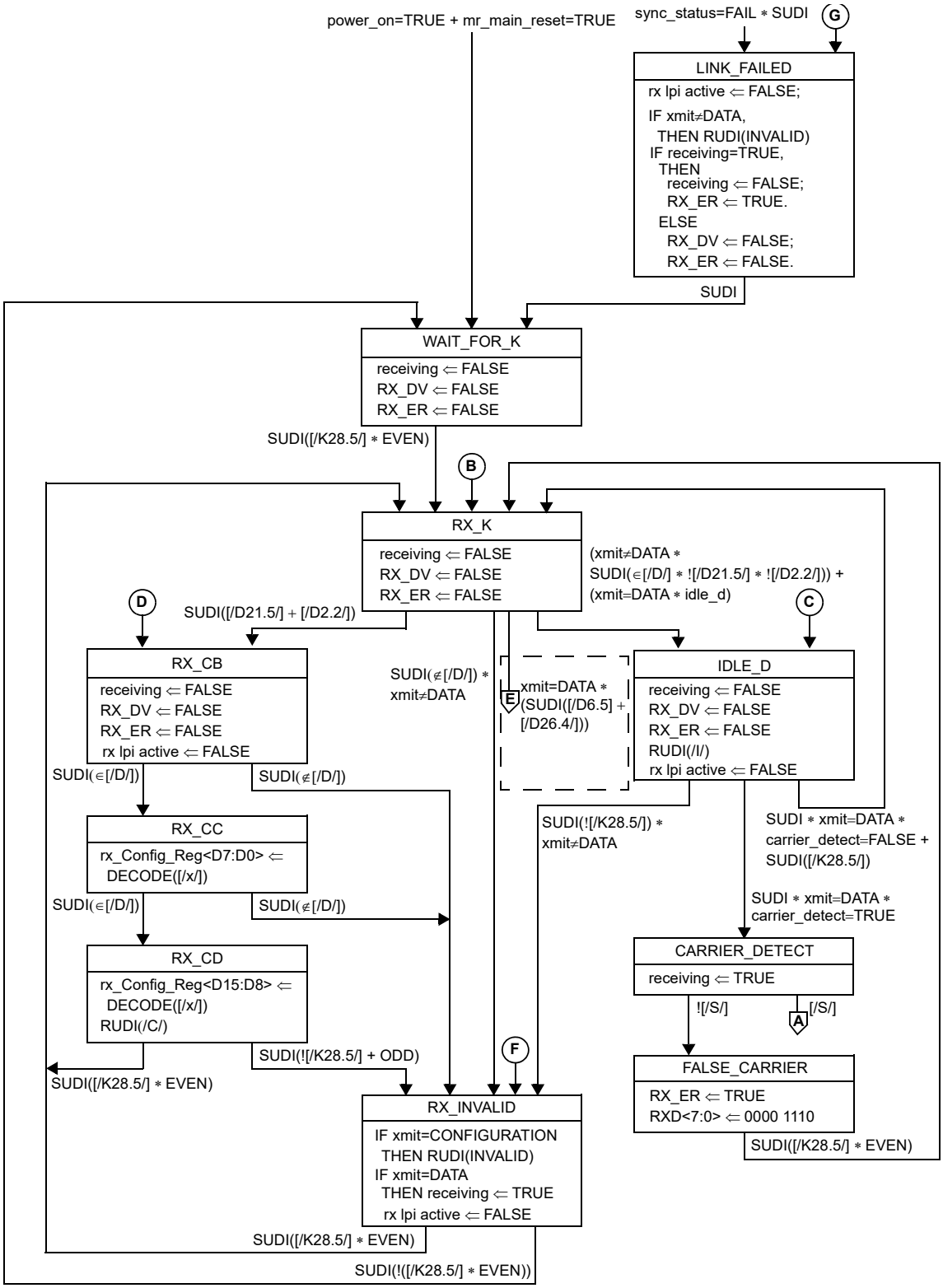

NOTE—Outgoing arcs leading to labeled polygons flow offpage to corresponding incoming arcs leading from labeled circles on Figure 36–7b and Figure 36–7c, and vice versa.

Figure 36–7a—PCS receive state diagram, part a

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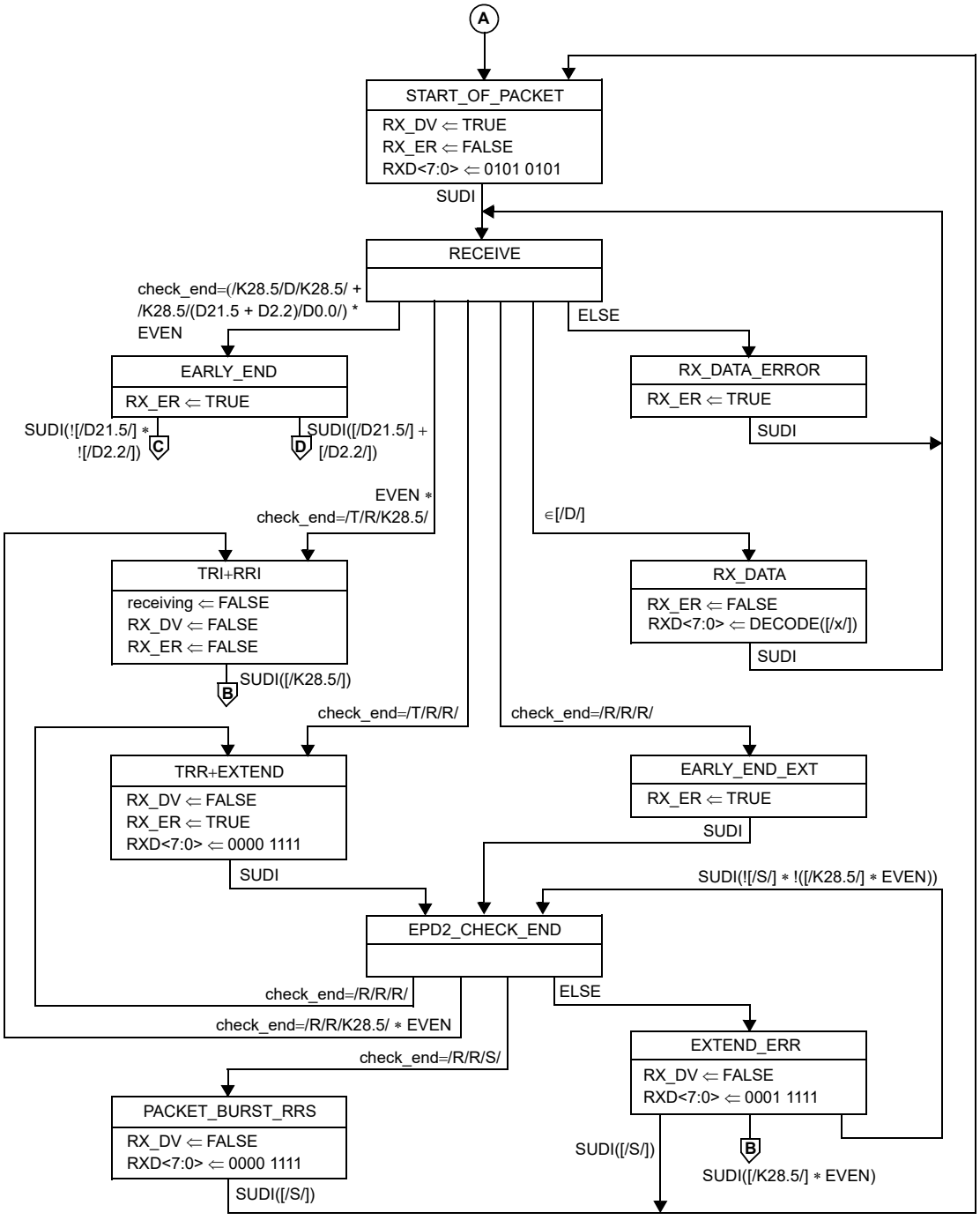

NOTE 1—Outgoing arcs leading to labeled polygons flow offpage to corresponding incoming arcs leading from labeled circles on Figure 36–7a, and vice versa.

NOTE 2—In the transition from RECEIVE to RX_DATA state the transition condition is a test against the code-group obtained from the SUDI that caused the transition to RECEIVE state.

Figure 36–7b—PCS receive state diagram, part b

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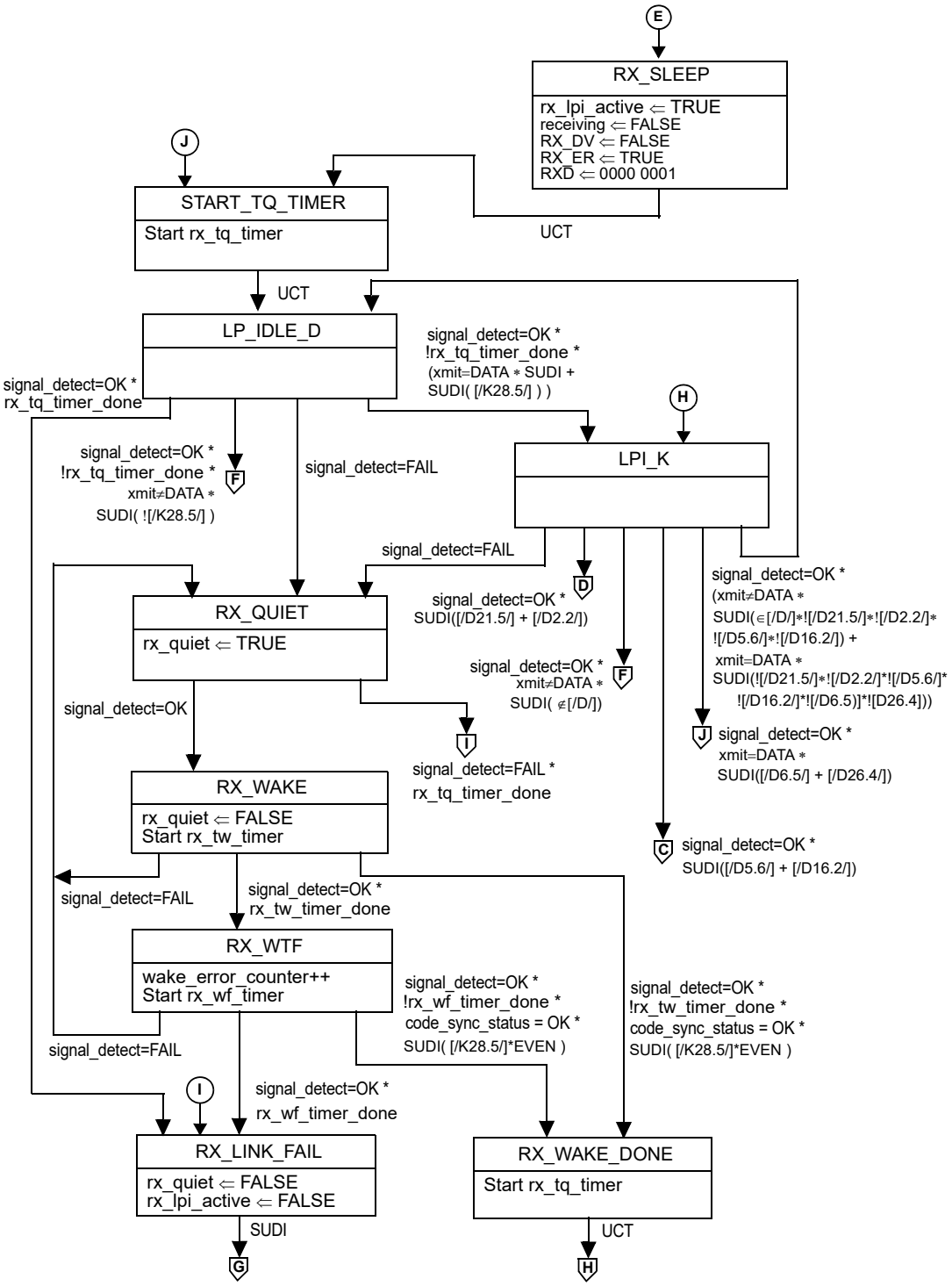

NOTE—Outgoing arcs leading to labeled polygons flow off page to corresponding incoming arcs leading from labeled circles on Figure 36–7a, and vice versa.

Figure 36–7c—PCS Receive state diagram, part c
(only required for the optional EEE capability)

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36.2.5.2.4 Code-group stream decoding

Subsequent to the detection of an SPD carrier event, the PCS Receive process performs the DECODE function on the incoming code-groups, passing decoded data to the GMII, including those corresponding to the remainder of the MAC preamble and SFD. The GMII signal RX_ER is asserted upon decoding any code-group following the SPD that neither is a valid /D/ code-group nor follows the EPD rules in 36.2.4.15.1.

Packets are terminated with an EPD as specified in 36.2.4.15. The PCS Receive process performs the check_end function to preserve the ability of the MAC to properly delimit the FCS at the end of a packet.

Detection of /T/R/R/ or /T/R/K28.5/ by the check_end function denotes normal (i.e., non-error) packet termination. Detection of /R/R/R/ by the check_end function denotes packet termination with error and Carrier_Extend processing. Detection of /K28.5/D/K28.5/ by the check_end function denotes packet termination with error. Detection of /K28.5/(D21.5 or D2.2)/D0.0 by the check_end function denotes packet termination with error.

36.2.5.2.5 Carrier sense

The Carrier Sense process generates the signal CRS on the GMII, which (via the Reconciliation sublayer) the MAC uses for deferral.

The PCS shall implement the Carrier Sense process as depicted in Figure 36–8 including compliance with the associated state variables as specified in 36.2.5.1.

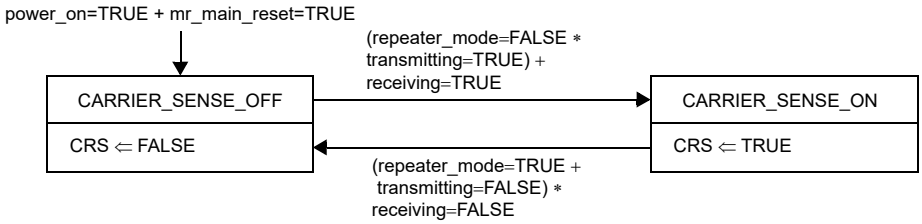

Figure 36–8—Carrier sense state diagram

36.2.5.2.6 Synchronization

The PCS shall implement the Synchronization process as depicted in Figure 36–9 including compliance with the associated state variables as specified in 36.2.5.1. The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PMA client to suspend normal actions.

A receiver that is in the LOSS_OF_SYNC state and that has acquired bit synchronization attempts to acquire code-group synchronization via the Synchronization process. Code-group synchronization is acquired by the detection of three ordered sets containing commas in their leftmost bit positions without intervening invalid code-group errors. Upon acquisition of code-group synchronization, the receiver enters the SYNC_ACQUIRED_1 state. Acquisition of synchronization ensures the alignment of multi-code-group ordered sets to even-numbered code-group boundaries.

Once synchronization is acquired, the Synchronization process tests received code-groups in sets of four code-groups and employs multiple sub-states, effecting hysteresis, to move between the SYNC_ACQUIRED_1 and LOSS_OF_SYNC states.

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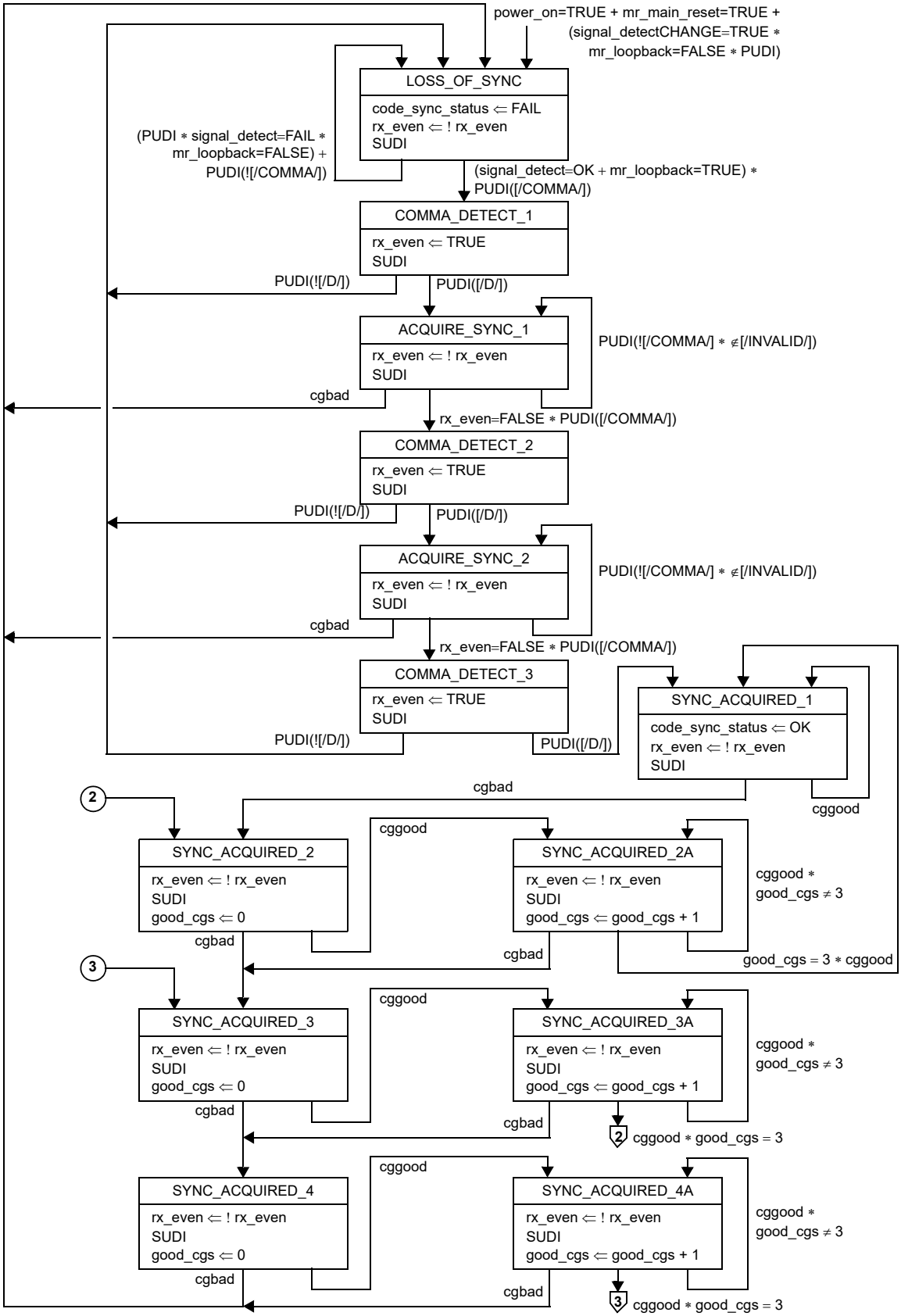

Figure 36–9—Synchronization state diagram

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For EEE capability the relationship between sync_status and code_sync_status is given by Figure 36–7c; otherwise sync_status is identical to code_sync_status.

The condition sync_status=FAIL existing for ten ms or more causes the PCS Auto-Negotiation process to begin and the PCS Transmit process to begin transmission of /C/. Upon reception of three matching /C/s from the link partner, the PCS Auto-Negotiation process begins. The internal signal receiving is deasserted in the PCS Receive process LINK_FAILED state when sync_status=FAIL and a code-group is received.

36.2.5.2.7 Auto-Negotiation process

The Auto-Negotiation process shall provide the means to exchange configuration information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. When the PCS is used with a PMD other than 1000BASE-KX, see Clause 37 for a description of the Auto-Negotiation process and Config_Reg contents.

Upon successful completion of the Clause 37 Auto-Negotiation process, the xmit flag is set to DATA and normal link operation is enabled. The Clause 37 Auto-Negotiation process utilizes the PCS Transmit and Receive processes to convey Config_Reg contents.

When the PCS is used with a 1000BASE-KX PMD, see Clause 73 for a description of the Auto-Negotiation process. The following requirements apply to a PCS used with a 1000BASE-KX PMD. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when sync_status=FAIL and the value OK when sync_status=OK. The primitive shall be generated when the value of link_status changes. If Clause 37 Auto-Negotiation is not present, xmit shall be DATA. If Clause 37 Auto-Negotiation is present the variable mr_an_enable should be false when 1000BASE-KX operation is negotiated through Clause 73 Auto-Negotiation.

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36.2.5.2.8 LPI state diagram

A PCS that supports the EEE capability shall implement the LPI transmit process as shown in Figure 36–10. The transmit LPI state diagram controls tx_quiet, which disables the transmitter when true.

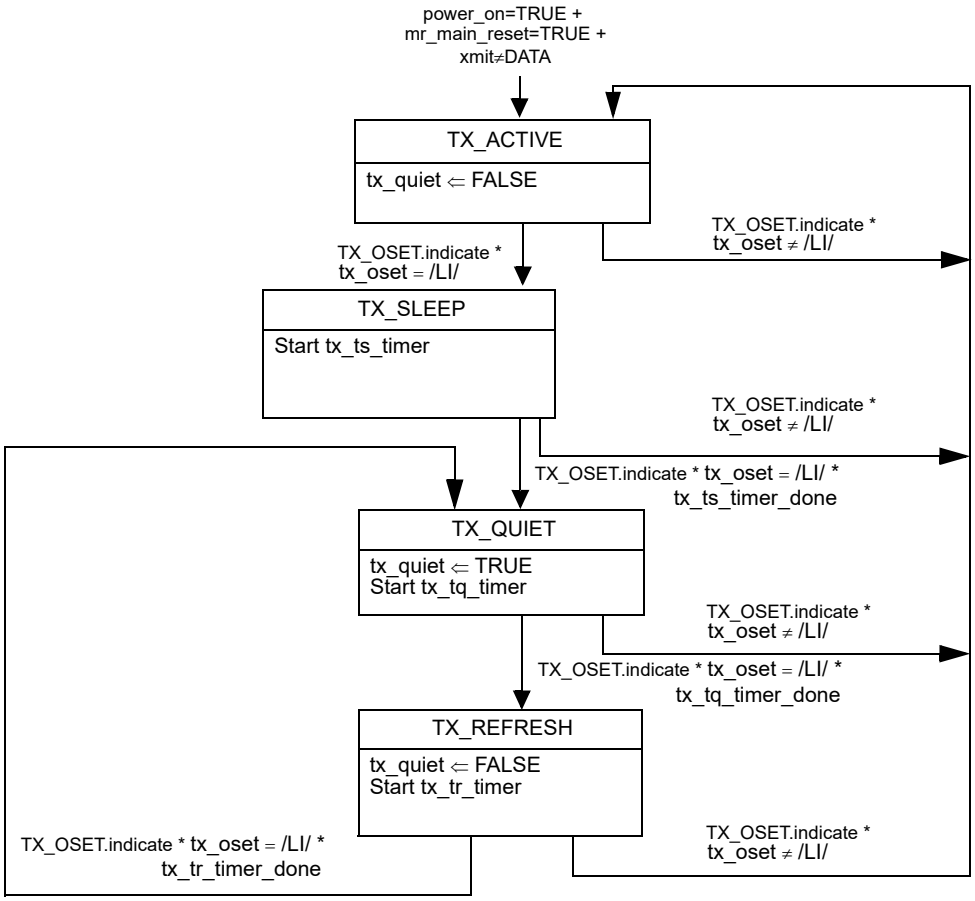

Figure 36–10—LPI Transmit state diagram

The timer values for these state diagrams are shown in Table 36–8 for transmit and Table 36–9 for receive.

Table 36–8—Transmitter LPI timing parameters

Parameter	Description	Min	Max	Units
T_{SL}	Local Sleep Time from entering the TX_SLEEP state to when tx_quiet is set to TRUE	19.9	20.1	µs
T_{QL}	Local Quiet Time from when tx_quiet is set to TRUE to entry into the TX_REFRESH state	2.5	2.6	ms
T_{UL}	Local Refresh Time from entry into the TX_REFRESH state to entry into the TX_QUIET state	19.9	20.1	µs

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Table 36–9—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for signal detect to be set to OK while in the LP_IDLE_D, LPI_K and RX_QUIET states before asserting a rx_fault	3	4	ms
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault (WTF)		11	µs
T_{WTF}	Wake time fault recovery time		1	ms

36.2.5.2.9 LPI status and management

For EEE capability, the PCS indicates to the management system that LPI is currently active in the receive and transmit directions using the status variables shown in Table 36–10.

Table 36–10—MDIO status indications

MDIO status variable	Register name	Register address	Note
Tx LPI received	PCS status register 1	3.1.11	Latched version of 3.1.9
Rx LPI received	PCS status register 1	3.1.10	Latched version of 3.1.8
Tx LPI indication	PCS status register 1	3.1.9	TRUE when not in state TX_ACTIVE
Rx LPI indication	PCS status register 1	3.1.8	TRUE when not in state RX_ACTIVE

36.3 Physical Medium Attachment (PMA) sublayer

36.3.1 Service Interface

The PMA provides a Service Interface to the PCS. These services are described in an abstract manner and do not imply any particular implementation. The PMA Service Interface supports the exchange of code-groups between PCS entities. The PMA converts code-groups into bits and passes these to the PMD, and vice versa. It also generates an additional status indication for use by its client.

The following primitives are defined:

PMA_UNITDATA.request(tx_code-group<9:0>)
PMA_UNITDATA.indication(rx_code-group<9:0>)

36.3.1.1 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of code-groups) from the PCS to the PMA. PMA_UNITDATA.request is generated by the PCS Transmit process.

36.3.1.1.1 Semantics of the service primitive

PMA_UNITDATA.request(tx_code-group<9:0>)

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The data conveyed by PMA_UNITDATA.request is the tx_code-group<9:0> parameter defined in 36.2.5.1.3.

36.3.1.1.2 When generated

The PCS continuously sends, at a nominal rate of 125 MHz, as governed by GTX_CLK, tx_code-group<9:0> to the PMA.

36.3.1.1.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a series of ten PMD_UNITDATA.request primitives, requesting transmission of the indicated tx_bit to the PMD.

36.3.1.2 PMA_UNITDATA.indication

This primitive defines the transfer of data (in the form of code-groups) from the PMA to the PCS. PMA_UNITDATA.indication is used by the PCS Synchronization process.

36.3.1.2.1 Semantics of the service primitive

PMA_UNITDATA.indication(rx_code-group<9:0>)

The data conveyed by PMA_UNITDATA.indication is the rx_code-group<9:0> parameter defined in 36.2.5.1.3.

36.3.1.2.2 When generated

The PMA continuously sends one rx_code-group<9:0> to the PCS corresponding to the receipt of each code-group aligned set of ten PMD_UNITDATA.indication primitives received from the PMD. The nominal rate of the PMA_UNITDATA.indication primitive is 125 MHz, as governed by the recovered bit clock.

36.3.1.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

36.3.2 Functions within the PMA

Figure 36–3 depicts the mapping of the octet-wide data path of the GMII to the ten-bit-wide code-groups of the PMA Service Interface, and on to the serial PMD Service Interface. The PMA comprises the PMA Transmit and PMA Receive processes for 1000BASE-X.

The PMA Transmit process serializes tx_code-groups into tx_bits and passes them to the PMD for transmission on the underlying medium, according to Figure 36–3. Similarly, the PMA Receive process deserializes rx_bits received from the PMD according to Figure 36–3. The PMA continuously conveys ten-bit code-groups to the PCS, independent of code-group alignment. After code-group alignment is achieved, based on comma detection, the PCS converts code-groups into GMII data octets, according to 36.2.5.2.2.

The proper alignment of a comma used for code-group synchronization is depicted in Figure 36–3.

NOTE—Strict adherence to manufacturer-supplied guidelines for the operation and use of PMA serializer components is required to meet the jitter specifications of Clause 38 and Clause 39. The supplied guidelines should address the quality of power supply filtering associated with the transmit clock generator, and also the purity of the reference clock fed to the transmit clock generator.

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36.3.2.1 Data delay

The PMA maps a nonaligned one-bit data path from the PMD to an aligned, ten-bit-wide data path to the PCS, on the receive side. Logically, received bits have to be buffered to facilitate proper code-group alignment. These functions necessitate an internal PMA delay of at least ten bit times. In practice, code-group alignment may necessitate even longer delays of the incoming rx_bit stream.

36.3.2.2 PMA transmit function

The PMA Transmit function passes data unaltered (except for serializing) from the PCS directly to the PMD. Upon receipt of a PMA_UNITDATA.request primitive, the PMA Transmit function shall serialize the ten bits of the tx_code-group<9:0> parameter and transmit them to the PMD in the form of ten successive PMD_UNITDATA.request primitives, with tx_code-group<0> transmitted first, and tx_code-group<9> transmitted last.

36.3.2.3 PMA receive function

The PMA Receive function passes data unaltered (except for deserializing and possible code-group slipping upon code-group alignment) from the PMD directly to the PCS. Upon receipt of ten successive PMD_UNITDATA.indication primitives, the PMA shall assemble the ten received rx_bits into a single ten-bit value and pass that value to the PCS as the rx_code-group<9:0> parameter of the primitive PMA_UNITDATA.indication, with the first received bit installed in rx_code-group<0> and the last received bit installed in rx_code-group<9>. An exception to this operation is specified in 36.3.2.4.

36.3.2.4 Code-group alignment

In the event the PMA sublayer detects a comma+ within the incoming rx_bit stream, it may realign its current code-group boundary, if necessary, to that of the received comma+ as shown in Figure 36–3. This process is referred to in this document as code-group alignment. The code-group alignment function shall be operational when the EN_CDET signal is active (see 36.3.3.1). During the code-group alignment process, the PMA sublayer may delete or modify up to four, but shall delete or modify no more than four, ten-bit code-groups in order to align the correct receive clock and code-group containing the comma+. This process is referred to as code-group slipping.

In addition, the PMA sublayer is permitted to realign the current code-group boundary upon receipt of a comma-pattern.

36.3.3 A physical instantiation of the PMA Service Interface

The ten-bit interface (TBI) is defined to provide compatibility among devices designed by different manufacturers. There is no requirement for a compliant device to implement or expose the TBI. A TBI implementation shall behave as described in 36.3.3 through 36.3.6.

Figure 36–11 illustrates the TBI functions and interfaces.

As depicted in Figure 36–11, the TBI connects the PCS and PMD sublayers. It is equipped for full duplex transmission of code-groups at 125 MHz. The PCS provides code-groups on tx_code-group<9:0> to the PMA transmit function, which latches the data on the rising edge of the 125 MHz PMA_TX_CLK. An internal Clock Multiplier Unit uses PMA_TX_CLK to generate the internal 1250 MHz bit clock that is used to serialize the latched data out of the PMA outputs, if EWRAP is Low, or internally loop it back to the Receive function input, if EWRAP is High.

The PMA Receive function accepts 1250 Mb/s serial data from either the PMD, if EWRAP is Low, or the PMA transmit function, if EWRAP is High, and extracts a bit clock and recovered data from the serial inputs

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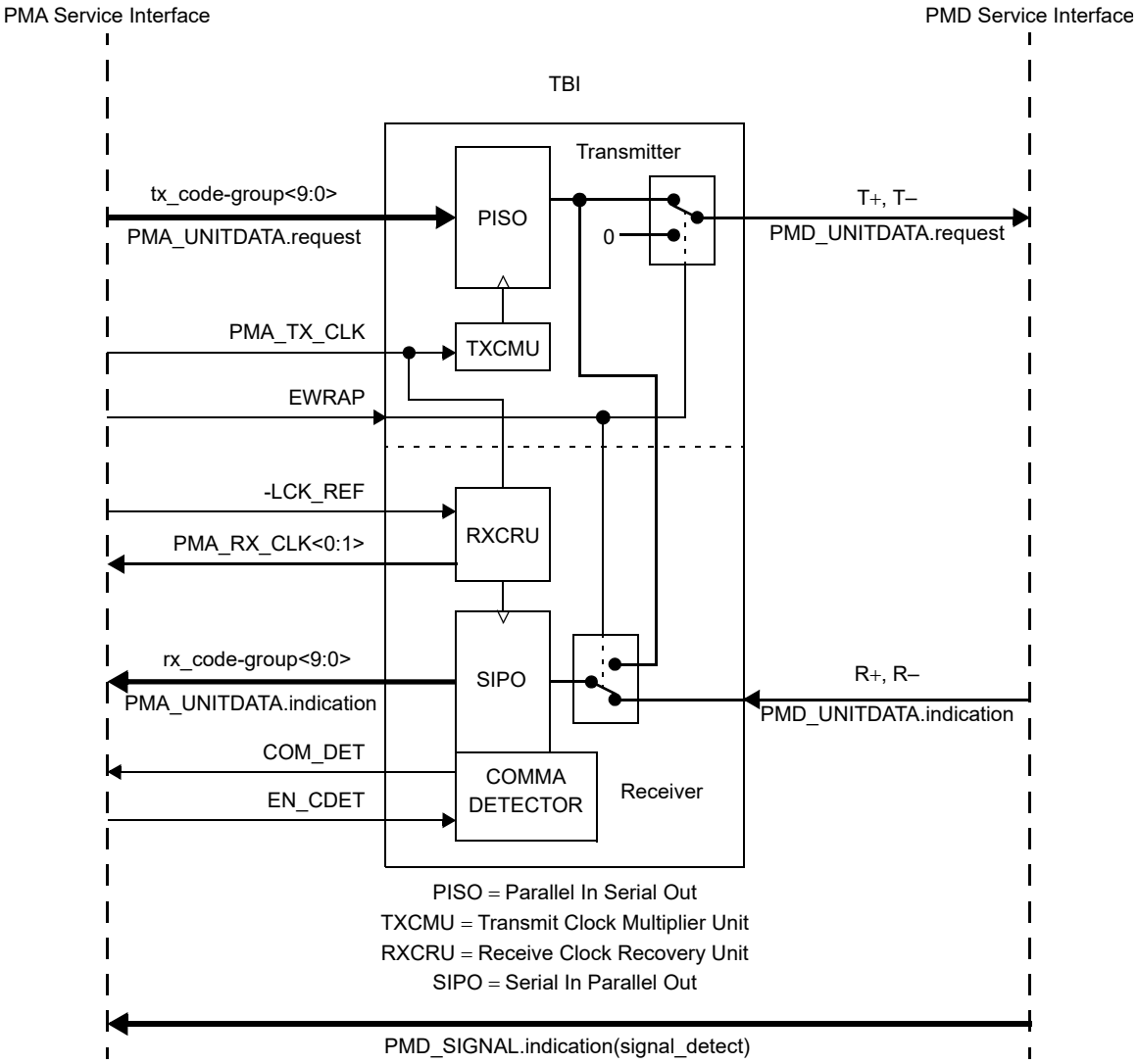

Figure 36–11—TBI reference diagram

in a clock recovery unit. The recovered data is deserialized and conveyed to the PCS on rx_code-group<9:0>. Two recovered clocks, PMA_RX_CLK<0> and PMA_RX_CLK<1>, which are at 1/20th the baud (62.5 MHz), and 180° out-of-phase with one another, are used by the PMA to latch the received 10-bit code-groups. Even and odd-numbered code-groups are latched on successive rising edges of PMA_RX_CLK<1> and PMA_RX_CLK<0>, respectively.

Code-group alignment occurs in the PMA Receive function, if enabled by EN_CDET, when a comma pattern occurs in the PHY bit stream. Upon recognition of the comma pattern, the PMA Receive function outputs the ten-bit code-group containing the comma on rx_code-group<9:0> with the alignment specified in Figure 36–3, and clocked on the rising edge of PMA_RX_CLK<1>.

This TBI provides a Lock_to_Reference_Clock (LCK_REF) input, which may be used to lock the clock recovery unit to PMA_TX_CLK rather than incoming serial data. In the absence of serial data or invalid serial data, the PMA Receive function passes many 8B/10B invalid code-groups across to the PCS. A circuit may be constructed to detect those errors and, using LCK_REF, re-center the receiver clock recovery unit to PMA_TX_CLK in preparation for reacquiring lock on the incoming PHY bit stream.

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36.3.3.1 Required signals

In the event this TBI is made accessible, the signals listed in Table 36–11 are provided, with the meanings described elsewhere in this section. Note that not all of these signals are used by the PCS.

Table 36–11—TBI required signals

Symbol	Signal Name	Signal Type	Active Level
tx_code-group<9:0>	Transmit Data	Input	H
PMA_TX_CLK	Transmit Clock	Input	↑
EWRAP	Enable Wrap	Input	H
rx_code-group<9:0>	Receive Data	Output	H
PMA_RX_CLK<0>	Receive Clock 0	Output	↑
PMA_RX_CLK<1>	Receive Clock 1	Output	↑
COM_DET	Comma Detect	Output	H
-LCK_REF	Lock to Reference	Input	L
EN_CDET	Enable Comma Detect	Input	H

tx_code-group<9:0>
: The 10-bit parallel transmit data presented to the PMA for serialization and transmission onto the media. The order of transmission is tx_bit<0> first, followed by tx_bit<1> through tx_bit<9>.

PMA_TX_CLK
: The 125 MHz transmit code-group clock. This code-group clock is used to latch data into the PMA for transmission. PMA_TX_CLK is also used by the transmitter clock multiplier unit to generate the 1250 MHz bit rate clock. PMA_TX_CLK is also used by the receiver when -LCK_REF is active. PMA_TX_CLK has a ±100 ppm tolerance. PMA_TX_CLK is derived from GMII GTX_CLK.

EWRAP
: EWRAP enables the TBI to electrically loop transmit data to the receiver. The serial outputs on the transmitter are held in a static state during EWRAP operation. EWRAP may optionally be tied low (function disabled).

rx_code-group<9:0>
: Presents the 10-bit parallel receive code-group data to the PCS for further processing. When code-groups are properly aligned, any received code-group containing a comma is clocked by PMA_RX_CLK<1>.

PMA_RX_CLK<0>
: The 62.5 MHz receive clock that the protocol device uses to latch odd-numbered code-groups in the received PHY bit stream. This clock may be stretched during code-group alignment, and is not shortened.

PMA_RX_CLK<1>
: The 62.5 MHz receive clock that the protocol device uses to latch even-numbered code-groups in the received PHY bit stream. PMA_RX_CLK<1> is 180° out-of-phase with PMA_RX_CLK<0>. This clock may be stretched during code-group alignment, and is not shortened.

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COM_DET

An indication that the code-group associated with the current PMA_RX_CLK<1> contains a valid comma. When EN_CDET is asserted, the TBI is required to detect and code-group-align to the comma+ bit sequence. Optionally, the TBI may also detect and code-group-align to the comma- bit sequence. The TBI provides this signal as an output, but it may not be used by the PCS.

-LCK_REF

Causes the TBI clock recovery unit to lock to PMA_TX_CLK. The TBI attains frequency lock within 500 ms. This function is not used by the PCS.

NOTE—Implementers may find it necessary to use this signal in order to meet the clock recovery requirements of the PMA sublayer.

EN_CDET

Enables the TBI to perform the code-group alignment function on a comma (see 36.2.4.9, 36.3.2.4). When EN_CDET is asserted the code-group alignment function is operational. This signal is optionally generated by the PMA client. The PMA sublayer may leave this function always enabled.

36.3.3.2 Summary of control signal usage

Table 36–12 lists all possible combinations of control signals on this TBI, including the valid combinations as well as the undefined combinations.

Table 36–12—TBI combinations of control signals

EWRAP	-LCK_REF	EN_CDET	Interpretation
L	L	L	Undefined
L	L	H	Lock receiver clock recovery unit to PMA_TX_CLK
L	H	L	Normal operation; COM_DET disabled
L	H	H	Normal operation; COM_DET enabled
H	L	L	Undefined
H	L	H	Undefined
H	H	L	Loop transmit data to receiver; COM_DET disabled
H	H	H	Loop transmit data to receiver; COM_DET enabled

36.3.4 General electrical characteristics of the TBI

In the event this TBI is made accessible, the following subclauses specify the general electrical characteristics of the TBI.

36.3.4.1 DC characteristics

Table 36–13 documents the required dc parametric attributes required of all inputs to the TBI and the dc parametric attributes associated with the outputs of the TBI. The inputs levels to the TBI may be greater than the power supply level (i.e., 5 V output driving V_{OH} into a 3.3 V input), tolerance to mismatched input levels is optional. TBI devices not tolerant of mismatched inputs levels that meet Table 36–13 requirements are still regarded as compliant.

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Table 36–13—DC specifications

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output High Voltage	I_{OH} = –400 µA	V_{CC} = Min	2.2	3.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA	V_{CC} = Min	GND	0.25	0.6	V
V_{IH}	Input High Voltage			2.0	—	V_{CC}[a] + 10%	V
V_{IL}	Input Low Voltage			GND	—	0.8	V
I_{IH}	Input High Current	V_{CC} = Max	V_{IN} = 2.4 V	—	—	40	µA
I_{IL}	Input Low Current	V_{CC} = Max	V_{IN} = 0.4 V	—	—	600	µA
C_{IN}	Input Capacitance			—	—	4.0	pf
t_R	Clock Rise Time	0.8 V to 2.0 V		0.7	—	2.4	ns
t_F	Clock Fall Time	2.0 V to 0.8 V		0.7	—	2.4	ns
t_R	Data Rise Time	0.8 V to 2.0 V		0.7	—	—	ns
t_F	Data Fall Time	2.0 V to 0.8 V		0.7	—	—	ns

[a]Refers to the driving device power supply.

36.3.4.2 Valid signal levels

All ac measurements are made from the 1.4 V level of the clock to the valid input or output data levels as shown in Figure 36–12.

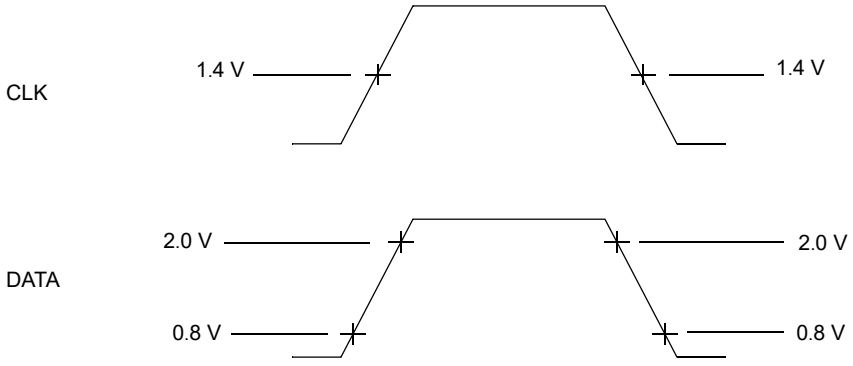

Figure 36–12—Input/output valid level for ac measurements

36.3.4.3 Rise and fall time definition

The rise and fall time definition for PMA_TX-CLK, PMA_RX_CLK<0>, PMA_RX_CLK<1>, and DATA is shown in Figure 36–13.

36.3.4.4 Output load

All ac measurements are assumed to have the output load of 10 pF.

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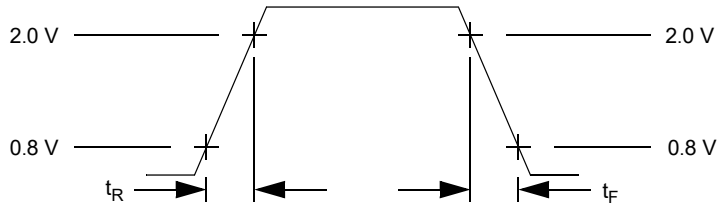

Figure 36–13—Rise and fall time definition

36.3.5 TBI transmit interface electrical characteristics

In the event this TBI is made accessible, the electrical characteristics of the TBI transmit interface are specified in the following subclauses.

36.3.5.1 Transmit data (tx_code-group<9:0>)

The tx_code-group<9:0> signals carry data from the PCS to PMA to be serialized to the PMD in accordance with the transmission order shown in Figure 36–3. All tx_code-group<9:0> data conforms to valid code-groups.

36.3.5.2 TBI transmit interface timing

The TBI transmit interface timings in Table 36–14 defines the TBI input. All transitions in Figure 36–14 are specified from the PMA_TX_CLK reference level (1.4 V), to valid input signal levels.

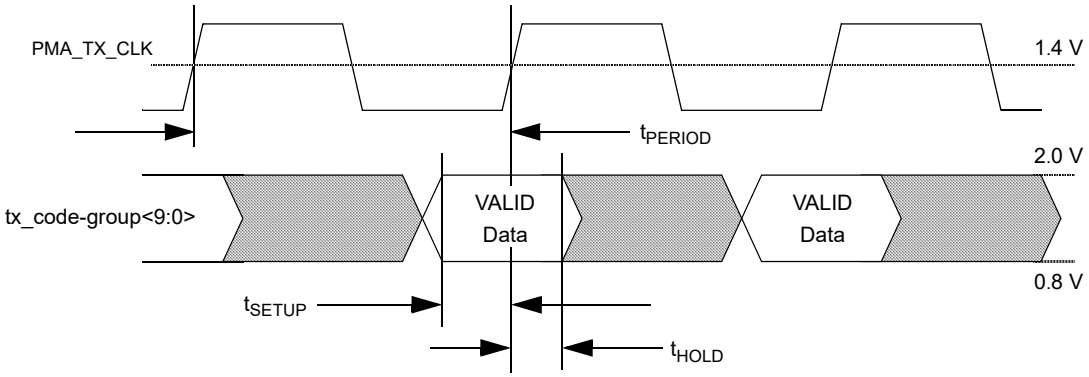

Figure 36–14—TBI transmit interface timing diagram

Table 36–14—Transmit AC specification

Parameter	Description	Min	Typ	Max	Units
t_{PERIOD}	PMA_TX_CLK Period[a]	—	8	—	ns
t_{SETUP}	Data Setup to ↑ PMA_TX_CLK	2.0	—	—	ns
t_{HOLD}	Data Hold from ↑ PMA_TX_CLK	1.0	—	—	ns
t_{DUTY}	PMA_TX_CLK Duty Cycle	40		60	%

[a] ±100 ppm tolerance on PMA_TX_CLK frequency.

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36.3.6 TBI receive interface electrical characteristics

In the event this TBI is made accessible, the electrical characteristics of the TBI receive interface are specified in the following subclauses.

The TBI receive interface timings in Table 36–15 define the TBI output. All transitions in Figure 36–15 are specified from the Receive Clock reference level (1.4 V) to valid output signal levels.

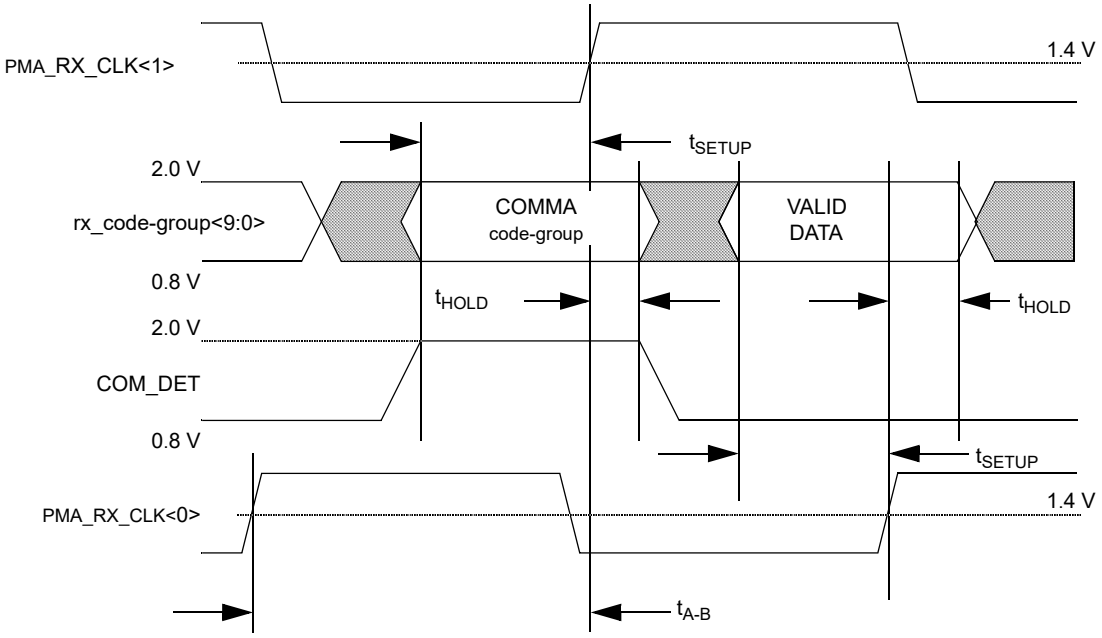

Figure 36–15—TBI receive interface timing diagram

36.3.6.1 Receive data (rx_code-group<9:0>)

The 10 receive data signals rx_code-group<9:0> carry parallel data from the PMA sublayer to the PCS sublayer during the rising edge of the receive clock (i.e., PMA_RX_CLK<1> transitions from Low to High). When properly locked and aligned, data transferred across this interface conforms to valid code-groups.

36.3.6.2 Receive clock (PMA_RX_CLK<0>, PMA_RX_CLK<1>)

The receive clocks supplied to the PCS and GMII are derived from the recovered bit clock. PMA_RX_CLK<0> is 180° out-of-phase with PMA_RX_CLK<1>.

Table 36–15 specifies a receive clock drift (t_{DRIFT}), which is applicable under all input conditions to the receiver (including invalid or absent input signals). However, the restriction does not apply when the receiver is realigning to a new code-group boundary and the receive clocks are being stretched to a new code-group boundary to avoid short pulses. During the code-group alignment process the receive clocks may slow a fixed amount, depending on the bit offset of the new comma and then return to the nominal frequency.

36.3.7 Loopback mode

Loopback mode shall be provided, as specified in this subclause, by the transmitter and receiver of a device as a test function to the device. When Loopback mode is selected, transmission requests passed to the

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Table 36–15—Receive bus AC specification

Parameter	Description	Min	Typ	Max	Units
t_{FREQ}	PMA_RX_CLK Frequency	—	62.5	—	MHz
t_{DRIFT}	PMA_RX_CLK Drift Rate[a]	0.2	—	—	µs/MHz
t_{SETUP}	Data Setup Before ↑PMA_RX_CLK	2.5	—	—	ns
t_{HOLD}	Data Hold After ↑PMA_RX_CLK	1.5	—	—	ns
t_{DUTY}	PMA_RX_CLK Duty Cycle	40	—	60	%
t_{A-B}	PMA_RX_CLK Skew	7.5	—	8.5	ns

[a]t_{DRIFT} is the (minimum) time for PMA_RX_CLK to drift from 63.5 MHz to 64.5 MHz or 60 MHz to 59 MHz from the PMA_RX_CLK lock value. It is applicable under all input signal conditions (except where noted in 36.3.2.4), including invalid or absent input signals, provided that the receiver clock recovery unit was previously locked to PMA_TX_CLK or to a valid input signal.

transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. A device is explicitly placed in Loopback mode (i.e., Loopback mode is not the normal mode of operation of a device). The method of implementing Loopback mode is not defined by this standard.

NOTE—Loopback mode may be implemented either in the parallel or the serial circuitry of a device.

36.3.7.1 Receiver considerations

A receiver may be placed in Loopback mode. Entry into or exit from Loopback mode may result in a temporary loss of synchronization.

36.3.7.2 Transmitter considerations

A transmitter may be placed in Loopback mode. The external behavior of a transmitter (i.e., the activity of a transmitter with respect to its attached link) in Loopback mode is specified in 22.2.4.1.2.

36.3.8 Test functions

A limited set of test functions may be provided as an implementation option for testing of the transmitter function.

Some test functions that are not defined by this standard may be provided by certain implementations. Compliance with the standard is not affected by the provision or exclusion of such functions by an implementation. Random jitter test patterns for 1000BASE-X are specified in Annex 36A.

A typical test function is the ability to transmit invalid code-groups within an otherwise valid PHY bit stream. Certain invalid PHY bit streams may cause a receiver to lose word and/or bit synchronization. See ANSI INCITS 230-1994 (FC-PH), subclause 5.4, for a more detailed discussion of receiver and transmitter behavior under various test conditions.

36.4 Compatibility considerations

There is no requirement for a compliant device to implement or expose any of the interfaces specified for the PCS or PMA. Implementations of a GMII shall comply with the requirements as specified in Clause 35. Implementations of a TBI shall comply with the requirements as specified in 36.3.3.

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36.5 Delay constraints

In half duplex mode, proper operation of a CSMA/CD LAN demands that there be an upper bound on the propagation delays through the network. This implies that MAC, PHY, and repeater implementations conform to certain delay minima and maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. MAC constraints are contained in 35.2.4 and Table 35–5. Topological constraints are contained in Clause 42.

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The reference point for all MDI measurements is the 50% point of the mid-cell transition corresponding to the reference bit, as measured at the MDI.

36.5.1 MDI to GMII delay constraints

Every 1000BASE-X PHY associated with a GMII shall comply with the bit time delay constraints specified in Table 36–16 for half duplex operation and Table 36–17 for full duplex operation. These figures apply for all 1000BASE-X PMDs. For any given implementation, the assertion and deassertion delays on CRS shall be equal.

Table 36–16—MDI to GMII delay constraints (half duplex mode)

Sublayer measurement points	Event	Min (bit time)	Max (bit time)	Input timing reference	Output timing reference
GMII ⇔ MDI	TX_EN=1 sampled to MDI output	—	136	PMA_TX_CLK rising	1st bit of /S/
	MDI input to CRS assert	—	192	1st bit of /S/	
	MDI input to CRS deassert	—	192	1st bit of /K28.5/	
	MDI input to COL assert	—	192	1st bit of /S/	
	MDI input to COL deassert	—	192	1st bit of /K28.5/	
	TX_EN=1 sampled to CRS assert	—	16	PMA_TX_CLK rising	
	TX_EN=0 sampled to CRS deassert	—	16	PMA_TX_CLK rising	

Table 36–17—MDI to GMII delay constraints (full duplex mode)

Sublayer measurement points	Event	Min (bit time)	Max (bit time)	Input timing reference	Output timing reference
GMII ⇔ MDI	TX_EN=1 sampled to MDI output	—	136	PMA_TX_CLK rising	1st bit of /S/
	MDI input to RX_DV deassert	—	192	1st bit of /T/	RX_CLK rising

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36.5.2 DTE delay constraints (half duplex mode)

Every DTE with a 1000BASE-X PHY shall comply with the bit time delay constraints specified in Table 36–18 for half duplex operation. These figures apply for all 1000BASE-X PMDs.

Table 36–18—DTE delay constraints (half duplex mode)

Sublayer measurement points	Event	Min (bit time)	Max (bit time)	Input timing reference	Output timing reference
MAC ⇔ MDI	MAC transmit start to MDI output	—	184		1st bit of /S/
	MDI input to MDI output (worst-case nondeferred transmit)	—	440	1st bit of /S/	1st bit of /S/
	MDI input to collision detect	—	240	1st bit of /S/	
	MDI input to MDI output = Jam (worst-case collision response)	—	440	1st bit of /S/	1st bit of jam

36.5.3 Carrier deassertion/assertion constraint (half duplex mode)

To ensure fair access to the network, each DTE operating in half duplex mode shall, additionally, satisfy the following:

(MAX MDI to MAC Carrier Deassert Detect) – (MIN MDI to MAC Carrier Assert Detect) < 16 bits

36.6 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801:1995.

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36.7 Protocol implementation conformance statement (PICS) proforma for Clause 36, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X[76]

36.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 36, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

36.7.2 Identification

36.7.2.1 Implementation identification

Supplier (Note 1)	
Contact point for inquiries about the PICS (Note 1)	
Implementation Name(s) and Version(s) (Notes 1 and 3)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) (Note 2)	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

36.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 36, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[76] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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36.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PMA	Ten-bit interface (TBI)	36.4		O	Yes [ ] No [ ]
*GMII	PHY associated with GMII	36.4		O	Yes [ ] No [ ]
*DTE	DTE with PHY not associated with GMII	36.5.2		O	Yes [ ] No [ ]
*FDX	PHY supports full duplex mode	36.5		O	Yes [ ] No [ ]
*HDX	PHY supports half duplex mode	36.5		O	Yes [ ] No [ ]
*LPI	Implementation of LPI	36.2.4.13		O	Yes [ ] No [ ]
NOTE—The following abbreviations are used: *HDGM: HDX and GMII *FDGM: FDX and GMII *HDTE: HDX and DTE					

36.7.4 PICS proforma tables for the PCS and PMA sublayer, type 1000BASE-X

36.7.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Test functions Annex 36A support	36.3.8		O	Yes [ ] No [ ]
CC2	Environmental specifications	36.6		M	Yes [ ]

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36.7.4.2 Code-group functions

Item	Feature	Subclause	Value/Comment	Status	Support
CG1	Transmitter initial running disparity	36.2.4.4	Transmitter initial running disparity assumes negative value	M	Yes [ ]
CG2	Transmitter running disparity calculation	36.2.4.4	Running disparity is calculated after each code-group transmitted	M	Yes [ ]
CG3	Validating received code-groups	36.2.4.6		M	Yes [ ]
CG4	Running disparity rules	36.2.4.4	Running disparity is calculated after each code-group reception	M	Yes [ ]
CG5	Transmitted code-group is chosen from the corresponding running disparity	36.2.4.5		M	Yes [ ]

36.7.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Transmit ordered set	36.2.5.2.1	Meets the requirements of Figure 36–5	M	Yes [ ]
SD2	Transmit code-group	36.2.5.2.1	Meets the requirements of Figure 36–6	M	Yes [ ]
SD3	Receive	36.2.5.2.2	Meets the requirements of Figures 36–7a and 36–7b	M	Yes [ ]
SD4	Carrier sense	36.2.5.2.5	Meets the requirements of Figure 36–8	M	Yes [ ]
SD5	Synchronization	36.2.5.2.6	Meets the requirements of Figure 36–9	M	Yes [ ]
SD6	Auto-Negotiation	36.2.5.2.7	Described in Clause 37	M	Yes [ ]
SD7*	Support for use with a 1000BASE-KX PMD	36.2.5.2.7	AN technology dependent interface described in Clause 73	O	Yes [ ]
SD8	AN_LINK.indication primitive	36.2.5.2.7	Support of the primitive AN_LINK.indication(link_status), when the PCS is used with 1000BASE-KX PMD	SD7:M	Yes [ ]
SD9	link_status parameter	36.2.5.2.7	Takes the value OK or FAIL, as described in 36.2.5.2.7	SD7:M	Yes [ ]
SD10	Generation of AN_LINK.indication primitive	36.2.5.2.7	Generated when the value of link_status changes	SD7:M	Yes [ ]
SD11	Value of xmit, when the PCS is used with 1000BASE-KX PMD	36.2.5.2.7	The value of xmit is DATA, when Clause 37 Auto-Negotiation is not present as described in 36.2.5.2.7	SD7:M	Yes [ ]

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36.7.4.4 PMA functions

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	Transmit function	36.3.2.2		M	Yes [ ]
PMA2	Receive function	36.3.2.3		M	Yes [ ]
PMA3	Code-group alignment	36.3.2.4	When EN_CDET is active	M	Yes [ ]
PMA4	Loopback mode	36.3.7		M	Yes [ ]

36.7.4.5 PMA transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
PMT1	cg_timer expiration	36.2.5.1.7	See 35.5.2.3	GMII:M	Yes [ ] N/A [ ]
PMT2	cg_timer expiration	36.2.5.1.7	8 ns ± 0.01%	!GMII: M	Yes [ ] N/A [ ]

36.7.4.6 PMA code-group alignment function

Item	Feature	Subclause	Value/Comment	Status	Support
CDT1	Code-group alignment to comma-	36.3.2.4		O	Yes [ ] N/A [ ]
CDT2	Code-group slipping limit	36.3.2.4	Deletion or modification of no more than four code-groups	M	Yes [ ]
CDT3	Code-group alignment to comma+	36.3.2.4		O	Yes [ ] N/A [ ]

36.7.4.7 TBI

Item	Feature	Subclause	Value/Comment	Status	Support
TBI1	TBI requirements	36.3.3		PMA:M	Yes [ ] N/A [ ]

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36.7.4.8 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	Equal carrier deassertion and assertion delay on CRS	36.5.1		HDGM:M	Yes [ ] N/A [ ]
TIM2	MDI to GMII delay constraints for half duplex	36.5.1	Table 36–16	HDGM:M	Yes [ ] N/A [ ]
TIM3	MDI to GMII delay constraints for full duplex	36.5.1	Table 36–17	FDGM:M	Yes [ ] N/A [ ]
TIM4	DTE delay constraints for half duplex	36.5.2	Table 36–18	HDTE:M	Yes [ ] N/A [ ]
TIM5	Carrier deassertion/assertion constraints	36.5.3		HDTE:M	Yes [ ] N/A [ ]

36.7.4.9 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
LP-01	Transmit ordered set state diagram	36.2.5.2.1	Support additions to Figure 36–5 for LPI operation	LPI:M	Yes [ ] No [ ]
LP-02	Receive state diagram	36.2.5.2.2	Support additions to Figure 36–7a, Figure 36–7b for LPI operation	LPI:M	Yes [ ] No [ ]
LP-03	LPI transmit state diagram	36.2.5.2.8	Meets the requirements of Figure 36–10	LPI:M	Yes [ ] No [ ]
LP-04	LPI receive state diagram	36.2.5.2.8	Meets the requirements of Figure 36–7c	LPI:M	Yes [ ] No [ ]
LP-03	LPI transmit timing	36.2.5.2.8	Meets the requirements of Table 36–8	LPI:M	Yes [ ] No [ ]
LP-04	LPI receive timing	36.2.5.2.8	Meets the requirements of Table 36–9	LPI:M	Yes [ ] No [ ]

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37. Auto-Negotiation function, type 1000BASE-X

37.1 Overview

37.1.1 Scope

Clause 37 describes the 1000BASE-X Auto-Negotiation (AN) function that allows a device (local device) to advertise modes of operation it possesses to a device at the remote end of a link segment (link partner) and to detect corresponding operational modes that the link partner may be advertising. Backplane Auto-Negotiation defined in Clause 73 applies to 1000BASE-KX.

The Auto-Negotiation function exchanges information between two devices that share a link segment and automatically configures both devices to take maximum advantage of their abilities. Auto-Negotiation is performed with /C/ and /I/ ordered sets defined in Clause 36, such that no packet or upper layer protocol overhead is added to the network devices. Auto-Negotiation does not test the link segment characteristics (see 37.1.4).

The function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and understanding of the common mode(s) of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function (see 37.2.4.2). The Auto-Negotiation function allows the devices to switch between the various operational modes in an ordered fashion, permits management to disable or enable the Auto-Negotiation function, and allows management to select a specific operational mode.

The basic mechanism to achieve Auto-Negotiation is to pass information encapsulated within /C/ ordered sets. /C/ ordered sets are directly analogous to FLP Bursts as defined in Clause 28 that accomplish the same function. Each device issues /C/ ordered sets at power up, on command from management, upon detection of a PHY error, or due to user interaction.

37.1.2 Application perspective/objectives

This Auto-Negotiation function is designed to be expandable and allows 1000BASE-X devices to self-configure a jointly compatible operating mode.

The following are the objectives of Auto-Negotiation:

a) To be reasonable and cost-effective to implement;
b) Provide a sufficiently extensible code space to
    1) Meet existing and future requirements;
    2) Allow simple extension without impacting the installed base;
    3) Accommodate remote fault signals; and
    4) Accommodate link partner ability detection.
c) Allow manual or Network Management configuration to override the Auto-Negotiation;
d) Capable of operation in the absence of Network Management;
e) Allow the ability to renegotiate;
f) Operate when
    1) The link is initially connected;
    2) A device at either end of the link is powered up, reset, or a renegotiation request is made.
g) May be enabled by automatic, manual, or Network Management intervention;
h) To complete the base page Auto-Negotiation function in a bounded time period;

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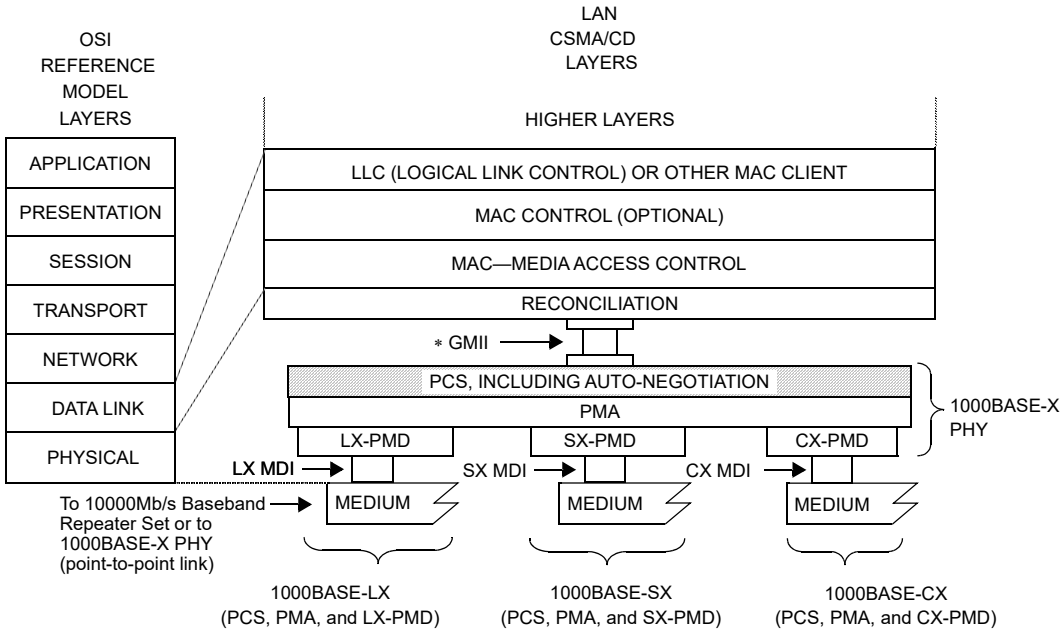
i) To operate using a peer-to-peer exchange of information with no requirement for a master device (not master-slave);
j) To be robust in the 1000BASE-X MDI cable noise environment;
k) To not significantly impact EMI/RFI emissions.

37.1.3 Relationship to architectural layering

The Auto-Negotiation function is provided at the PCS sublayer of the Physical Layer of the OSI reference model as shown in Figure 36–1. Devices that support multiple modes of operation may advertise this fact using this function. The transfer of information is observable only at the MDI or on the medium.



MDI=MEDIUM DEPENDENT INTERFACE
GMII=GIGABIT MEDIA INDEPENDENT INTERFACE
PCS=PHYSICAL CODING SUBLAYER
PMA=PHYSICAL MEDIUM ATTACHMENT
PHY=PHYSICAL LAYER DEVICE
PMD=PHYSICAL MEDIUM DEPENDENT
LX-PMD=PMD FOR FIBER—LONG WAVELENGTH, Clause 38
SX-PMD=PMD FOR FIBER—SHORT WAVELENGTH, Clause 38
CX-PMD=PMD FOR 150 Ω BALANCED COPPER CABLING, Clause 39

NOTE—The PMD sublayers are mutually independent.
∗ GMII is optional.

Figure 37–1—Location of the Auto-Negotiation function

37.1.4 Compatibility considerations

37.1.4.1 Auto-Negotiation

1000BASE-X devices provide the Auto-Negotiation function. Auto-Negotiation does not perform cable tests, such as cable performance measurements. Some PHYs that explicitly require use of high-performance cables, may require knowledge of the cable type, or additional robustness tests (such as monitoring invalid code-groups, CRC, or framing errors) to determine if the link segment is adequate.

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37.1.4.2 Management interface

Manual or automatic invocation of Auto-Negotiation may result in frame loss. Exit from Auto-Negotiation to normal MAC frame processing may also result in frame loss as one link end may resume normal MAC frame processing ahead of its link partner.

37.1.4.2.1 GMII management interface

Auto-Negotiation signaling does not occur across the GMII. Control of the Auto-Negotiation function may be supported through the Management Interface of the GMII or equivalent. If an explicit embodiment of the GMII is supported, the Control and Status registers to support the Auto-Negotiation function shall be implemented in accordance with the definitions in Clause 22 and 37.2.5.

37.1.4.3 Interoperability between Auto-Negotiation compatible devices

An Auto-Negotiation compatible device decodes the Base Page from the received /C/ ordered sets and examines the contents for the highest common ability that both devices share. Both devices acknowledge correct receipt of each other's Base Page by responding with Base Pages containing the Acknowledge Bit set. After both devices complete acknowledgment, and any desired Next Page exchange, both devices enable the highest common mode negotiated. The highest common mode is resolved using the priority resolution hierarchy specified in 37.2.4.2.

37.1.4.4 User Configuration with Auto-Negotiation

Rather than disabling Auto-Negotiation, the following behavior is suggested in order to improve interoperability with other Auto-Negotiation devices. When a device is configured for one specific mode of operation (e.g. 1000BASE-X Full Duplex), it is recommended to continue using Auto-Negotiation but only advertise the specifically selected ability or abilities. This can be done by the Management agent only setting the bits in the advertisement registers that correspond to the selected abilities.

37.2 Functional specifications

The Auto-Negotiation function includes the Auto-Negotiation Transmit, Receive, and Arbitration functions specified in the state diagram of Figure 37–6 and utilizes the PCS Transmit and Receive state diagrams of Clause 36.

The Auto-Negotiation function provides an optional Management function that provides a control and status mechanism. Management may provide additional control of Auto-Negotiation through the Management function, but the presence of a management agent is not required.

37.2.1 Config_Reg encoding

The Config_Reg Base Page, transmitted by a local device or received from a link partner, is encapsulated within a /C/ ordered set and shall convey the encoding shown in Figure 37–2. Auto-Negotiation supports additional pages using the Next Page function. Encodings for the Config_Reg(s) used in Next Page exchange are defined in 37.2.4.3.1. Config_Reg bits labeled as "rsvd" are reserved and shall be set to a logic zero.

37.2.1.1 Base Page to management register mapping

Several Base Page bits shown in Figure 37–2 indicate capabilities that are sourced from management registers. Table 37–1 describes how the management registers map to the management function interface signals. The bit format of the rx_Config_Reg<D15:D0> and tx_Config_Reg<D15:D0> variables is context dependent, relative to the state of the Auto-Negotiation function, and is presented here and in 37.2.4.3.1.

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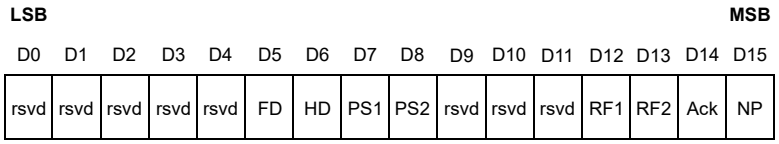

Figure 37–2—Config_Reg Base Page encoding

Table 37–1—Config_Reg Base Page to management register mapping

Config_Reg Base Page bits	Management register bit
Full Duplex (FD)	4.5 Full Duplex
Half Duplex (HD)	4.6 Half Duplex
PAUSE (PS1)	4.7 PAUSE
ASM_DIR (PS2)	4.8 ASM_DIR
Remote Fault (RF2, RF1)	4.13:12 Remote Fault

37.2.1.2 Full duplex

Full Duplex (FD) is encoded in bit D5 of the base Config_Reg.

37.2.1.3 Half duplex

Half Duplex (HD) is encoded in bit D6 of the base Config_Reg.

37.2.1.4 Pause

Pause (PS1, PS2) is encoded in bits D7 and D8 of the base Config_Reg. Pause provides a pause capability exchange mechanism. Pause encoding is specified in Table 37–2.

Table 37–2—Pause encoding

PAUSE (D7)	ASM_DIR(D8)	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. The ASM_DIR bit indicates that asymmetric PAUSE operation is supported. The value of the PAUSE bit when the ASM_DIR bit is set indicates the direction PAUSE frames are supported for flow

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across the link. Asymmetric PAUSE configuration results in independent enabling of the PAUSE receive and PAUSE transmit functions as defined by Annex 31B. See 37.2.4.2 for PAUSE configuration resolution.

37.2.1.5 Remote fault

Sensing of faults in a device as well as subsequent association of faults with the Remote Fault function encodings is optional. Remote Fault (RF) is encoded in bits D12 and D13 of the Base Page. The default value is 0b00. Remote Fault provides a standard transport mechanism for the transmission of simple fault and error information. The Remote Fault function may indicate to the link partner that a fault or error condition has occurred. The two Remote Fault bits, RF1 and RF2, shall be encoded as specified in Table 37–3.

Table 37–3—Remote Fault encoding

RF1	RF2	Description
0	0	No error, link OK (default)
0	1	Offline
1	0	Link_Failure
1	1	Auto-Negotiation_Error

If the local device has no mechanism to detect a fault or associate a fault condition with the received Remote Fault function encodings, then it shall transmit the default Remote Fault encoding of 0b00.

A local device may indicate it has sensed a fault to its link partner by setting a nonzero Remote Fault encoding in its Base Page and renegotiating.

If the local device sets the Remote Fault encoding to a nonzero value, it may also use the Next Page function to specify information about the fault that has occurred. Remote Fault Message Page Codes may be specified for this purpose (see Annex 28C).

The Remote Fault encoding shall remain set until after the Auto-Negotiation process transitions into IDLE_DETECT state with the Base Page, at which time the Remote Fault encoding is reset to 0b00. On receipt of a Base Page with a nonzero Remote Fault encoding, the device shall set the Remote Fault bit in the Status register (1.4) to logic one if the GMII management function is present.

37.2.1.5.1 No error, link OK

A Remote Fault encoding of 0b00 indicates that no remote fault or error condition has been detected by the local device.

37.2.1.5.2 Offline

A Remote Fault encoding of 0b01 indicates that the local device is going Offline. A local device may indicate Offline prior to powering off, running transmitter tests, or removing the local device from the active configuration. A local device need not successfully complete the Auto-Negotiation function from the receive perspective after completing the Auto-Negotiation function indicating Offline from its transmit perspective before further action is taken (e.g., powering off, running transmitter tests, removing the local device from the active configuration, etc.).

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37.2.1.5.3 Link_Failure

A Remote Fault encoding of 0b10 indicates that the local device has detected a Link_Failure condition indicated by loss of synchronization. While sync_status = FAIL, remote fault information is not signaled. When sync_status becomes OK, stored remote fault information is signaled (see 36.2.5.1.3 and 36.2.5.2.6). Another indication of a link failure condition is provided by the reception of /C/ ordered sets having rx_Config_Reg<D15:D0> = 0 for a duration exceeding link_timer.

37.2.1.5.4 Auto-Negotiation_Error

A Remote Fault encoding of 0b11 indicates that the local device has detected a Auto-Negotiation_Error. Resolution which precludes operation between a local device and link partner shall be reflected to the link partner by the local device by indicating a Remote Fault code of Auto-Negotiation_Error.

37.2.1.6 Acknowledge

Acknowledge (Ack) is encoded in bit D14 of the base and Next Pages (see Figures 37–2, 37–3, and 37–4). The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's base or Next Page.

This bit is set to logic one after the device has successfully received at least three consecutive and matching rx_Config_Reg<D15:D0> values (ignoring the Acknowledge bit value), and, for Next Page exchanges, remains set until the Next Page information has been loaded into the AN Next Page transmit register (register 7). After the Auto-Negotiation process COMPLETE_ACKNOWLEDGE state has been entered, the tx_Config_Reg<D15:D0> value is transmitted for the link_timer duration.

37.2.1.7 Next Page

The Base Page and subsequent Next Pages may set the NP bit to a logic one to request Next Page transmission. Subsequent Next Pages may set the NP bit to a logic zero in order to communicate that there is no more Next Page information to be sent (see 37.2.4.3). A device may implement Next Page ability and choose not to engage in a Next Page exchange by setting the NP bit to a logic zero.

37.2.2 Transmit function requirements

The Transmit function provides the ability to transmit /C/ ordered sets. After Power-On, link restart, or renegotiation, the Transmit function transmits /C/ ordered sets containing zeros indicating the restart condition. After sending sufficient zeros, the /C/ ordered sets contain the Config_Reg Base Page value defined in 37.2.1. The local device may modify the Config_Reg value to disable an ability it possesses, but shall not transmit an ability it does not possess. This makes possible the distinction between local abilities and advertised abilities so that devices capable of multiple modes may negotiate to a mode lower in priority than the highest common local ability.

The Transmit function shall utilize the PCS Transmit process specified in 36.2.5.2.1.

37.2.2.1 Transmit function to Auto-Negotiation process interface requirements

The variable tx_Config_Reg<D15:D0> is derived from mr_adv_abilities<16:1> or mr_np_tx<16:1>. This variable is the management representation of the AN advertisement register during Base Page exchange and the AN Next Page transmit register during Next Page exchange.

When the xmit variable is set to CONFIGURATION by the Auto-Negotiation process, the PCS Transmit function encodes the contents of the tx_Config_Reg<D15:D0> into the appropriate /C/ ordered set for transmission onto the MDI. When the xmit variable is set to IDLE by the Auto-Negotiation process, the PCS

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Transmit function transmits /I/ ordered sets onto the MDI. When the xmit variable is set to DATA by the Auto-Negotiation process, the PCS Transmit function transmits /I/ ordered sets interspersed with packets onto the MDI.

37.2.3 Receive function requirements

The PCS Receive function detects /C/ and /I/ ordered sets. For received /C/, the PCS Receive function decodes the information contained within, and stores the data in rx_Config_Reg<D15:D0>.

The Receive function shall utilize the PCS Receive process specified in 36.2.5.2.2.

37.2.3.1 Receive function to Auto-Negotiation process interface requirements

The PCS Receive function provides the Auto-Negotiation process and management function with the results of rx_Config_Reg<D15:D0>. The PCS Auto-Negotiation function generates the ability_match, acknowledge_match, consistency_match, and idle_match signals.

The PCS Receive process sets the RX_UNITDATA.indicate(/C/) message when a /C/ ordered set is received.

The PCS Receive process sets the RX_UNITDATA.indicate(/I/) message when a /I/ ordered set is received.

The PCS Receive process sets the RX_UNITDATA.indicate(INVALID) message when an error condition is detected while not in normal receive processing (when the xmit variable is set to CONFIGURATION). The error conditions are specified in the PCS Receive state diagram of Figure 36–7a.

37.2.4 Arbitration process requirements

The Arbitration process ensures proper sequencing of the Auto-Negotiation function using the Transmit function and Receive function. The Arbitration process enables the Transmit function to advertise and acknowledge abilities. Upon completion of Auto-Negotiation information exchange, the Arbitration process determines the highest common mode using the priority resolution function and enables the appropriate functions.

37.2.4.1 Renegotiation function

A renegotiation request from any entity, such as a management agent, causes the Auto-Negotiation function to be restarted from Auto-Negotiation process state AN_ENABLE.

37.2.4.2 Priority resolution function

Since a local device and a link partner may have multiple common abilities, a mechanism to resolve which mode to configure is necessary. Auto-Negotiation shall provide the Priority Resolution function that defines the hierarchy of supported technologies.

Priority resolution is supported for pause and half/full duplex modes of operation. Full duplex shall have priority over half duplex mode. Priority resolution for pause capability shall be resolved as specified by Table 37–4. Resolution that precludes operation between a local device and link partner is reflected to the link partner by the local device by indicating a Remote Fault code of Auto-Negotiation_Error, if the remote fault function is supported (see 37.2.1.5).

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Table 37–4—Pause priority resolution

Local Device		Link Partner		Local Resolution	Link Partner Resolution
PAUSE	ASM_DIR	PAUSE	ASM_DIR		
0	0	—	—	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	0	—	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	1	Enable PAUSE transmit, Disable PAUSE receive	Enable PAUSE receive, Disable PAUSE transmit
1	0	0	—	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	0	1	—	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive
1	1	0	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	1	0	1	Enable PAUSE receive, Disable PAUSE transmit	Enable PAUSE transmit, Disable PAUSE receive
1	1	1	—	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive

37.2.4.3 Next Page function

Support for transmission and reception of additional page encodings beyond the Base Page (Next Pages) is optional. The Next Page function enables the exchange of user or application specific data. Data is carried by Next Pages of information, which follow the transmission and acknowledgment procedures used for the Base Pages. Two types of Next Page encodings are defined:

a) Message Pages (contain an eleven-bit formatted Message Code Field);
b) Unformatted Pages (contain an eleven-bit Unformatted Code Field).

A dual acknowledgment system is used. Acknowledge (Ack) is used to acknowledge receipt of the information (see 37.2.1.6). Acknowledge 2 (Ack2) is used to indicate that the receiver is able to act on the information (or perform the task) defined in the message (see 37.2.4.3.5).

Next Page operation is controlled by the same two mandatory control bits, NP and Ack, used in the Base Page. The Toggle bit is used to ensure proper synchronization between the local device and the link partner.

Next Page exchange occurs after the Base Page exchange has been completed. Next Page exchange consists of using the Auto-Negotiation arbitration process to send Message or Unformatted Next Pages. Unformatted Pages can be combined to send extended messages. Any number of Next Pages may be sent in any order.

Subsequent to Base Page exchange, a Next Page exchange is invoked only if both the local device and its link partner have advertised Next Page ability during the Base Page exchange.

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If the Next Page function is supported by both link ends and a Next Page exchange has been invoked by both link ends, the Next Page exchange ends when both ends of a link segment set their NP bits to logic zero, indicating that neither link end has further pages to transmit. It is possible for the link partner to have more Next Pages to transmit than the local device. Once a local device has completed transmission of its Next Page information, if any, it shall transmit Message Pages with a Null message code (see Annex 28C) and the NP bit set to logic zero while its link partner continues to transmit valid Next Pages. A device shall recognize reception of Message Pages with a Null message code and the NP bit set to logic zero as the end of its link partner's Next Page information. If both the local device and its link partner advertise Next Page ability in their Base Pages, then both devices shall send at least one Next Page. If a device advertises Next Page ability and has no Next Page information to send but is willing to receive Next Pages, and its link partner also advertises Next Page ability, it shall send a Message Page with a Null message code. The variable mr_np_loaded is set to TRUE to indicate that the local device has loaded its Auto-Negotiation Next Page transmit register with Next Page information for transmission.

A local device that requires or expects an Ack2 response from its link partner (to indicate a Next Page transaction has been received and can be acted upon), has to terminate the Next Page sequence with a Null message code, in order to allow the link partner to transport the final Ack2 status.

37.2.4.3.1 Next Page encodings

The Next Page shall use the encoding shown in Figure 37–3 and Figure 37–4 for the NP, Ack, MP, Ack2, and T bits. The eleven-bit field <D10:D0> is encoded as a Message Code Field if the MP bit is logic one and an Unformatted Code Field if MP is set to logic zero. The bit format of the rx_Config_Reg<D15:D0> and tx_Config_Reg<D15:D0> variables is context dependent, relative to the state of the Auto-Negotiation function, and is presented here and in 37.2.1.1.

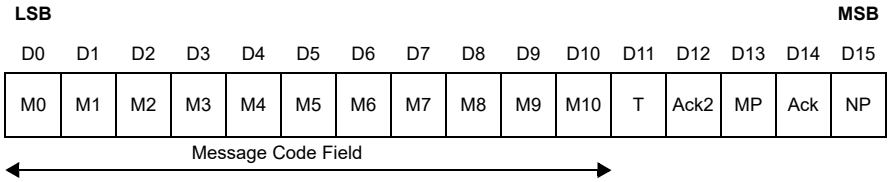

Figure 37–3—Message page encoding

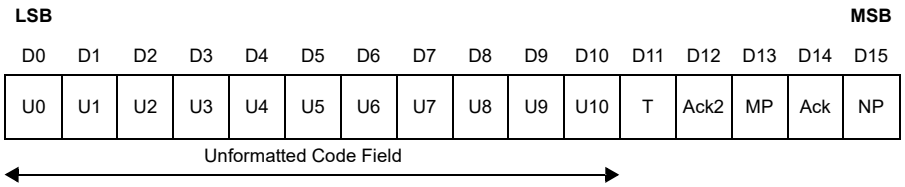

Figure 37–4—Unformatted page encoding

37.2.4.3.2 Next Page

The Next Page (NP) bit is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. NP shall be set as follows:

logic zero = Last page.
logic one = Additional Next Page(s) to follow.

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37.2.4.3.3 Acknowledge

As defined in 37.2.1.6.

37.2.4.3.4 Message page

The Message Page (MP) bit is used by the Next Page function to differentiate a Message Page from an Unformatted Page. MP shall be set as follows:

logic zero = Unformatted Page.
logic one = Message Page.

37.2.4.3.5 Acknowledge 2

The Acknowledge 2 (Ack2) bit is used by the Next Page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows:

logic zero = Cannot comply with message.
logic one = Can comply with message.

37.2.4.3.6 Toggle

The Toggle (T) bit is used by the Arbitration function to ensure synchronization with the link partner during Next Page exchange. This bit takes the opposite value of the Toggle bit in the previously exchanged page. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of tx_Config_Reg<D11> in the Base Page that preceded the Next Page exchange and, therefore, may assume a value of logic one or zero. The Toggle bit is set as follows:

logic zero = Previous value of tx_Config_Reg<D11> equalled logic one.
logic one = Previous value of tx_Config_Reg<D11> equalled logic zero.

37.2.4.3.7 Message page encoding

Message Pages are formatted pages that carry a single predefined message code, which is enumerated in Annex 28C. There are 2048 message codes available. The allocation of these codes is specified in Annex 28C. If the Message Page bit is set to logic one, the bit encoding of the Config_Reg value is interpreted as a Message Page.

37.2.4.3.8 Message Code Field

Message Code Field (M<10:0>) is an eleven-bit wide field, encoding 2048 possible messages. Message Code Field definitions are shown in Annex 28C. Combinations not specified are reserved for future use. Reserved combinations of the Message Code Field shall not be transmitted.

37.2.4.3.9 Unformatted page encoding

Unformatted Pages carry the messages indicated by Message Pages. Five control bits are predefined, the remaining eleven bits are interpreted based on the preceding message page. If the Message Page bit is set to logic zero, then the bit encoding of the Config_Reg value is interpreted as an Unformatted Page.

37.2.4.3.10 Unformatted Code Field

Unformatted Code Field (U<10:0>) is an eleven-bit wide field, which may contain an arbitrary value.

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37.2.4.3.11 Use of Next Pages

The following rules for Next Page usage shall be observed:

a) A Next Page exchange is invoked when the local device and the link partner advertise (in their Base Pages) that they have Next Page information to transmit;
b) Next Page exchange continues until neither device on a link has more pages to transmit as indicated by the NP bit. A Message Page with a Null Message Code Field value is sent if the device has no other information to transmit;
c) A message code can carry either a specific message or information that defines how following Unformatted Page(s) should be interpreted;
d) If a message code references Unformatted Pages, the Unformatted Pages immediately follow the referencing message code in the order specified by the message code;
e) Unformatted Page users are responsible for controlling the format and sequencing for their Unformatted Pages.

37.2.4.3.12 Management register requirements

The AN Next Page transmit register defined in 37.2.5.1.6 holds the Next Page to be sent by Auto-Negotiation. Received Next Pages are stored in the AN link partner ability Next Page register defined in 37.2.5.1.7.

37.2.5 Management function requirements

The management interface is used to communicate Auto-Negotiation information to the management entity. Mandatory functions specified here reference bits in GMII registers 0, 1, 4, 5, 6, 7, 8, 15. Where an implementation does not use a GMII, equivalent functions to these bits have to be included.

37.2.5.1 Management registers

The Auto-Negotiation function shall utilize six dedicated management registers:

a) Control register (Register 0);
b) Status register (Register 1);
c) AN advertisement register (Register 4);
d) AN link partner ability Base Page register (Register 5);
e) AN expansion register (Register 6);
f) Extended Status register (Register 15).

If Next Page is supported, the Auto-Negotiation function shall utilize an additional two management registers:

g) AN Next Page transmit register (Register 7);
h) AN link partner ability Next Page register (Register 8).

37.2.5.1.1 Control register (Register 0)

This register provides the mechanism to enable or disable Auto-Negotiation, restart Auto-Negotiation, and allow for manual configuration when Auto-Negotiation is not enabled. The definition for this register is provided in Clause 22.

When manual configuration is in effect at a local device, manual configuration should also be effected for the link partner to ensure predictable configuration. When manual configuration is in effect, values for the PAUSE bits (PS1, PS2) should result in a valid operational mode between the local device and the link partner.

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37.2.5.1.2 Status register (Register 1)

This register includes information about all modes of operations supported by the local device and the status of Auto-Negotiation. The definition for this register is provided in Clause 22.

37.2.5.1.3 AN advertisement register (Register 4) (R/W)

This register contains the advertised ability of the local device (see Table 37–5). Before Auto-Negotiation starts, this register is configured to advertise the abilities of the local device.

Table 37–5—AN advertisement register bit definitions

Bit(s)	Name	Description	R/W
4.15	Next Page	See 37.2.1.7	R/W
4.14	Reserved	Write as zero, ignore on read	RO
4.13:12	Remote Fault	See 37.2.1.5	R/W
4.11:9	Reserved	Write as zero, ignore on read	RO
4.8:7	Pause	See 37.2.1.4	R/W
4.6	Half Duplex	See 37.2.1.3	R/W
4.5	Full Duplex	See 37.2.1.2	R/W
4.4:0	Reserved	Write as zero, ignore on read	RO

37.2.5.1.4 AN link partner ability Base Page register (Register 5) (RO)

All of the bits in the AN link partner ability Base Page register are read only. A write to the AN link partner ability Base Page register has no effect.

This register contains the advertised ability of the link partner (see Table 37–6). The bit definitions are a direct representation of the link partner's Base Page. Upon successful completion of Auto-Negotiation, the Status register Auto-Negotiation Complete bit (1.5) is set to logic one.

The values contained in this register are guaranteed to be valid either once Auto-Negotiation has successfully completed, as indicated by bit 1.5 or when the Page Received bit (6.1) is set to logic one to indicate that a new Base Page has been received and stored in the Auto-Negotiation link partner ability base register.

37.2.5.1.5 AN expansion register (Register 6) (RO)

All of the bits in the Auto-Negotiation expansion register are read only; a write to the Auto-Negotiation expansion register has no effect.

Bits 6.15:3 and 6.0 are reserved for future Auto-Negotiation expansion.

The Next Page Able bit (6.2) is set to logic one to indicate that the local device supports the Next Page function. The Next Page Able bit is set to logic zero if the Next Page function is not supported by the local device.

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Table 37–6—AN link partner ability Base Page register bit definitions

Bit(s)	Name	Description	R/W
5.15	Next Page	See 37.2.1.7	RO
5.14	Acknowledge	See 37.2.1.6	RO
5.13:12	Remote Fault	See 37.2.1.5	RO
5.11:9	Reserved	Ignore on read	RO
5.8:7	Pause	See 37.2.1.4	RO
5.6	Half Duplex	See 37.2.1.3	RO
5.5	Full Duplex	See 37.2.1.2	RO
5.4:0	Reserved	Ignore on read	RO

Table 37–7—AN expansion register bit definitions

Bit(s)	Name	Description	R/W	Default
6.15:3	Reserved	Ignore on read	RO	0
6.2	Next Page Able	1 = Local device is Next Page able 0 = Local device is not Next Page able	RO	0
6.1	Page Received	1 = A new page has been received 0 = A new page has not been received	RO/ LH	0
6.0	Reserved	Ignore on read	RO	0

The Page Received bit (6.1) is set to logic one to indicate that a new page has been received and stored in the applicable AN link partner ability base or Next Page register.

The Page Received bit shall be reset to logic zero on a read of the AN expansion register (Register 6). Subsequent to the setting of the Page Received bit, and in order to prevent overlay of the AN link partner ability Next Page register, the AN link partner ability Next Page register should be read before the AN Next Page transmit register is written.

37.2.5.1.6 AN Next Page transmit register (Register 7)

This register contains the Next Page value to be transmitted, if required. The definition for this register is provided in 22.2.4.1.6.

37.2.5.1.7 AN link partner ability Next Page register (Register 8)

This register contains the advertised ability of the link partner's Next Page. The definition for this register is provided in 32.5.4.2 for changes to 28.2.4.1.4.

37.2.5.1.8 Extended status register (Register 15)

This register includes additional information about all modes of operations supported by the local device. The definition for this register is provided in Clause 22.

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37.2.5.1.9 State diagram variable to management register mapping

The state diagram of Figure 37–6 generates and accepts variables of the form "mr_x," where x is an individual signal name. These variables comprise a management interface that may be connected to the GMII management function or other equivalent function. Table 37–8 describes how PCS state diagram variables in both Clauses 36 and 37 map to management register bits.

Table 37–8—PCS state diagram variable to management register mapping

State diagram variable	Management register bit
mr_adv_ability<16:1>	4.15:0 Auto-Negotiation advertisement register
mr_an_complete	1.5 Auto-Negotiation complete
mr_an_enable	0.12 Auto-Negotiation enable
mr_loopback	0.14 Loopback (see 36.2.5.1.3)
mr_lp_adv_ability<16:1>	5.15:0 AN link partner ability register
mr_lp_np_rx<16:1>	8.15:0 AN link partner Next Page ability register
mr_main_reset	0.15 Reset
mr_np_able	6.2 Next Page Able
mr_np_loaded	Set on write to the AN Next Page transmit register; cleared by Auto-Negotiation state diagram
mr_np_tx<16:1>	7.15:0 AN Next Page transmit register
mr_page_rx	6.1 Page received
mr_restart_an	0.9 Auto-Negotiation restart
xmit=DATA	1.2 Link status

37.2.5.2 Auto-Negotiation managed object class

The Auto-Negotiation Managed Object Class is defined in Clause 30.

37.2.6 Absence of management function

In the absence of any management function, the advertised abilities shall be provided through a logical equivalent of mr_adv_ability<16:1>.

37.3 Detailed functions and state diagrams

The notation used in the state diagram in Figure 37–6 follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set. Variables using the "mr_x" notation do not have state diagram defaults; however, their appropriate initialization conditions when mapped to the management interface are covered in 22.2.4. The variables, timers, and counters used in the state diagrams are defined in 37.3.1.

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Auto-Negotiation shall implement the Auto-Negotiation state diagram and meet the Auto-Negotiation state diagram interface requirements of the Receive and Transmit functions. Additional requirements to these state diagrams are made in the respective functional requirements sections. In the case of any ambiguity between stated requirements and the state diagrams, the state diagrams take precedence. A functional reference diagram of Auto-Negotiation is shown in Figure 37–5.

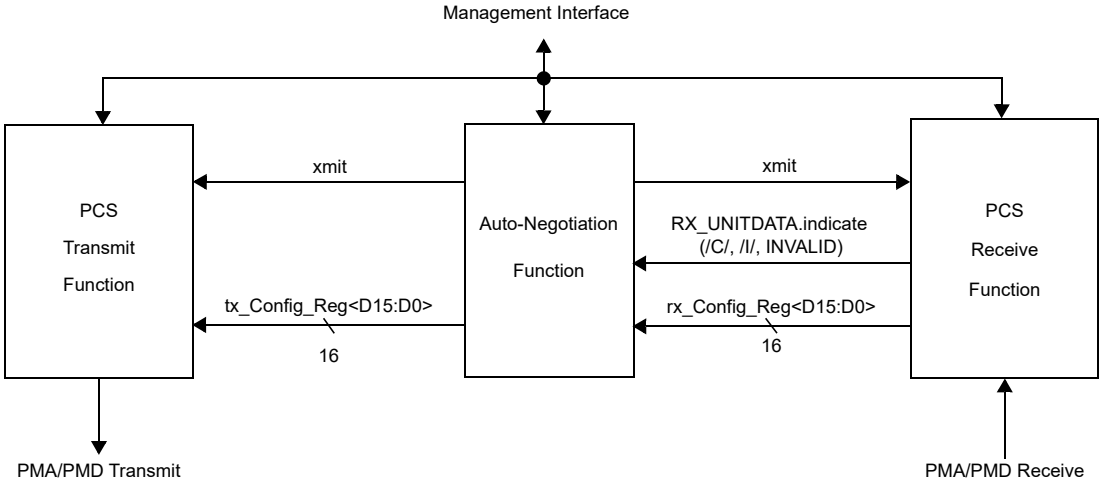

Figure 37–5—Functional reference diagram

37.3.1 State diagram variables

Variables with <16:1> or <D15:D0> appended to the end of the variable name indicate arrays that can be mapped to 16-bit management registers. For these variables, "<x>" indexes an element or set of elements in the array, where "x" may be as follows:

— Any integer or set of integers.
— Any variable that takes on integer values.
— NP; represents the index of the Next Page bit.
— ACK; represents the index of the Acknowledge bit.
— RF; represents the index of the Remote Fault bits.

Variables of the form "mr_x," where x is a label, comprise a management interface that is intended to be connected to the GMII Management function. However, an implementation-specific management interface may provide the control and status function of these bits.

37.3.1.1 Variables

an_sync_status

Qualified version of sync_status for use by Auto-Negotiation to detect a sync_status timeout condition.

Values: OK; The variable sync_status defined in 36.2.5.1.3 is OK.
FAIL; The variable sync_status defined in 36.2.5.1.3 is FAIL for a duration greater than or equal to the link timer.

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mr_adv_ability<16:1>

A 16-bit array that contains the advertised ability Base Page of the local device to be conveyed to tx_Config_Reg<D15:D0> for transmission to the link partner. For each element within the array:

Values: ZERO; Data bit is logical zero.
ONE; Data bit is logical one.

mr_an_complete

Status indicating whether Auto-Negotiation has completed or not.

Values: FALSE; Auto-Negotiation has not completed.
TRUE; Auto-Negotiation has completed.

mr_an_enable

Controls the enabling and disabling of the Auto-Negotiation function for 1000BASE-X. Auto-Negotiation function for 1000BASE-X is enabled when Control register bit 0.12 is set to one.

Values: FALSE; Auto-Negotiation is disabled.
TRUE; Auto-Negotiation is enabled.

mr_lp_adv_ability<16:1>

A 16-bit array that contains the advertised ability Base Page of the link partner conveyed from rx_Config_Reg<D15:D0>. For each element within the array:

Values: ZERO; Data bit is logical zero.
ONE; Data bit is logical one.

mr_lp_np_rx<16:1>

A 16-bit array that contains the advertised ability of the link partner's Next Page conveyed from rx_Config_Reg<D15:D0>. For each element within the array:

Values: ZERO; Data bit is logical zero.
ONE; Data bit is logical one.

mr_main_reset

Controls the resetting of the Auto-Negotiation function.

Values: FALSE; Do not reset the Auto-Negotiation function.
TRUE; Reset the Auto-Negotiation function.

mr_np_able

Status indicating whether the local device supports Next Page exchange.

Values: FALSE; The local device does not support Next Page exchange.
TRUE; The local device supports Next Page exchange.

mr_np_loaded

Status indicating whether a new page has been loaded into the AN Next Page transmit register (register 7).

Values: FALSE; A new page has not been loaded.
TRUE; A new page has been loaded.

mr_np_tx<16:1>

A 16-bit array that contains the new Next Page to transmit. If a Next Page exchange is invoked, this array is conveyed to tx_Config_Reg<D15:D0> for transmission to the link partner. For each element within the array:

Values: ZERO; Data bit is logical zero.
ONE; Data bit is logical one.

mr_page_rx

Status indicating whether a new page has been received. A new page has been successfully received when acknowledge_match=TRUE and consistency_match=TRUE and the

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rx_Config_Reg<D15:D0> value has been written to mr_lp_adv_ability<16:1> or mr_lp_np_rx<16:1>, depending on whether the page received was a base or Next Page, respectively.

Values: FALSE; A new page has not been received.
TRUE; A new page has been received.

NOTE—For the first setting of mr_page_rx, mr_lp_adv_ability is valid but need not be read as it is preserved through a Next Page operation. On subsequent settings of mr_page_rx, mr_lp_np_rx should be read prior to loading mr_np_tx register in order to avoid the overlay of Next Page information.

mr_restart_an

Controls renegotiation via management control.

Values: FALSE; Do not restart Auto-Negotiation.
TRUE; Restart Auto-Negotiation.

np_rx

Flag to hold value of rx_Config_Reg<NP> upon entry to state COMPLETE ACKNOWLEDGE. This value is associated with the value of rx_Config_Reg<NP> when acknowledge_match was last set.

Values: ZERO; The local device np_rx bit equals logic zero.
ONE; The local device np_rx bit equals logic one.

power_on

Condition that is true until such time as the power supply for the device that contains the Auto-Negotiation function has reached the operating region. The condition is also true when the device has low power mode set via Control register bit 0.11.

Values: FALSE; The device is completely powered (default).
TRUE; The device has not been completely powered.

NOTE—Power_on evaluates to its default value in each state where it is not explicitly set.

resolve_priority

Controls the invocation of the priority resolution function specified in Table 37–4.

Values: OFF; The priority resolution function is not invoked (default).
ON; The priority resolution function is invoked.

NOTE—Resolve_priority evaluates to its default value in each state where it is not explicitly set.

rx_Config_Reg<D15:D0>

Defined in 36.2.5.1.3.

sync_status

Defined in 36.2.5.1.3.

toggle_rx

Flag to keep track of the state of the link partner Toggle bit.

Values: ZERO; The link partner Toggle bit equals logic zero.
ONE; The link partner Toggle bit equals logic one.

toggle_tx

Flag to keep track of the state of the local device Toggle bit.

Values: ZERO; The local device Toggle bit equals logic zero.
ONE; The local device Toggle bit equals logic one.

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tx_Config_Reg<D15:D0>

Defined in 36.2.5.1.3. This array may be loaded from mr_adv_ability or mr_np_tx.

xmit

A parameter set by the PCS Auto-Negotiation process to reflect the source of information to the PCS Transmit process.

Values: CONFIGURATION: Tx_Config_Reg<D15:D0> information is being sourced from the PCS Auto-Negotiation process.
DATA: /I/, sourced from the PCS, is interspersed with packets sourced from the MAC.
IDLE: /I/ is being sourced from the PCS Auto-Negotiation process.

37.3.1.2 Functions

ability_match

For a stream of /C/ and /I/ ordered sets, this function continuously indicates whether the last three consecutive rx_Config_Reg<D15,D13:D0> values match. Three consecutive rx_Config_Reg<D15,D13:D0> values are any three rx_Config_Reg<D15,D13:D0> values received one after the other, regardless of whether the rx_Config_Reg<D15,D13:D0> value has already been used in a rx_Config_Reg<D15,D13:D0> match comparison or not. The match count is reset upon receipt of /I/. The match count is reset upon receipt of a second or third consecutive rx_Config_Reg<D15,D13:D0> value which does not match the rx_Config_Reg<D15,D13:D0> values for which the match count was set to one.

Values: FALSE; Three matching consecutive rx_Config_Reg<D15,D13:D0> values have not been received (default).
TRUE; Three matching consecutive rx_Config_Reg<D15,D13:D0> values have been received.

NOTE—Ability_match is set by this function definition; it is not set explicitly in the state diagrams. Ability_match evaluates to its default value upon state entry.

acknowledge_match

For a stream of /C/ and /I/ ordered sets, this function continuously indicates whether the last three consecutive rx_Config_Reg<D15:D0> values match and have the Acknowledge bit set. Three consecutive rx_Config_Reg<D15:D0> values are any three rx_Config_Reg<D15:D0> values contained within three /C/ ordered sets received one after the other, regardless of whether the rx_Config_Reg<D15:D0> value has already been used in a rx_Config_Reg<D15:D0> match comparison or not. The match count is reset upon receipt of /I/. The match count is reset upon receipt of a second or third consecutive rx_Config_Reg<D15:D0> value which does not match the rx_Config_Reg<D15:D0> values for which the match count was set to one.

Values: FALSE; Three matching and consecutive rx_Config_Reg<D15:D0> values have not been received with the Acknowledge bit set (default).
TRUE; Three matching and consecutive rx_Config_Reg<D15:D0> values have been received with the Acknowledge bit set.

NOTE—Acknowledge_match is set by this function definition; it is not set explicitly in the state diagrams. Acknowledge_match evaluates to its default value upon state entry.

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an_enableCHANGE

This function monitors the mr_an_enable variable for a state change. The function is set to TRUE on state change detection.

Values: TRUE; A mr_an_enable variable state change has been detected.
FALSE; A mr_an_enable variable state change has not been detected (default).

NOTE—An_enableCHANGE is set by this function definition; it is not set explicitly in the state diagrams. An_enableCHANGE evaluates to its default value upon state entry.

consistency_match

Indicates that the rx_Config_Reg<D15,D13:D0> value that caused ability_match to be set, for the transition from states ABILITY_DETECT or NEXT_PAGE_WAIT to state ACKNOWLEDGE_DETECT, is the same as the rx_Config_Reg<D15,D13:D0> value that caused acknowledge_match to be set.

Values: FALSE; The rx_Config_Reg<D15,D13:D0> value that caused ability_match to be set is not the same as the rx_Config_Reg<D15,D13:D0> value that caused acknowledge_match to be set, ignoring the Acknowledge bit value.
TRUE; The rx_Config_Reg<D15,D13:D0> value that caused ability_match to be set is the same as the rx_Config_Reg<D15,D13:D0> value that caused acknowledge_match to be set, independent of the Acknowledge bit value.

NOTE—Consistency_match is set by this function definition; it is not set explicitly in the state diagrams.

idle_match

For a stream of /C/ and /I/ ordered sets, this function continuously indicates whether three consecutive /I/ ordered sets have been received. The match count is reset upon receipt of /C/.

Values: FALSE; Three consecutive /I/ ordered sets have not been received (default).
TRUE; Three consecutive /I/ ordered sets have been received.

NOTE—Idle_match is set by this function definition; it is not set explicitly in the state diagrams. Idle_match evaluates to its default value upon state entry.

37.3.1.3 Messages

RUDI

Alias for RX_UNITDATA.indicate(parameter). Defined in 36.2.5.1.6.

RX_UNITDATA.indicate

Defined in 36.2.5.1.6.

37.3.1.4 Timers

All timers operate in the manner described in 14.2.3.2.

link_timer

Timer used to ensure Auto-Negotiation protocol stability and register read/write by the management interface.

Duration: 10 ms, tolerance +10 ms, –0 s.

37.3.1.5 State diagrams

The Auto-Negotiation state diagram is specified in Figure 37–6.

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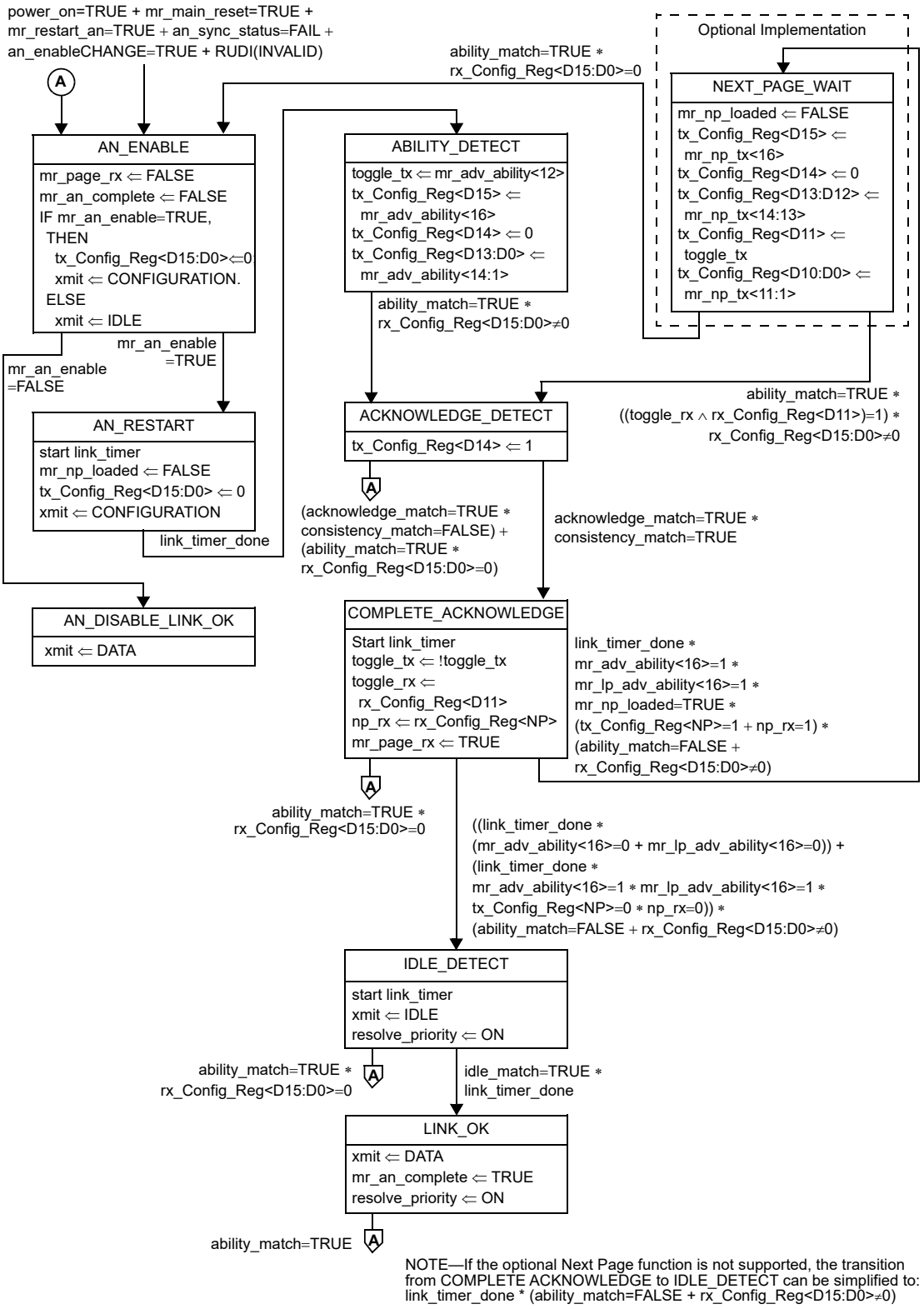

Figure 37–6—Auto-Negotiation state diagram

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37.4 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801:1995.

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37.5 Protocol implementation conformance statement (PICS) proforma for Clause 37, Auto-Negotiation function, type 1000BASE-X[77]

37.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 37, Auto-Negotiation function, type 1000BASE-X, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

37.5.2 Identification

37.5.2.1 Implementation identification

Supplier (Note 1)	
Contact point for inquiries about the PICS (Note 1)	
Implementation Name(s) and Version(s) (Notes 1 and 3)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) (Note 2)	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

37.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 37, Auto-Negotiation function, type 1000BASE-X
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[77] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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37.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*GMII	GMII Management Interface	37.1.4.2.1		O	Yes [ ] No [ ]
*RF	Remote Fault function	37.2.1.5		O	Yes [ ] No [ ]
*NP	Next Page function	37.2.4.3		O	Yes [ ] No [ ]

In addition, the following predicate name is defined for use when different implementations from the set above have common parameters:

*NPM: GMII and NP

37.5.4 PICS proforma tables for the Auto-Negotiation function, type 1000BASE-X

37.5.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Provision of logical equivalent of mr_adv_ability<16:1>	37.2.6	In the absence of any management function	M	Yes [ ]
CC2	Environmental specifications	37.4		M	Yes [ ]

37.5.4.2 Auto-Negotiation functions

Item	Feature	Subclause	Value/Comment	Status	Support
AN1	Config_Reg encoding	37.2.1		M	Yes [ ]
AN2	Priority Resolution function	37.2.4.2		M	Yes [ ]
AN3	Auto-Negotiation state diagram	37.3		M	Yes [ ]

37.5.4.2.1 Config_Reg

Item	Feature	Subclause	Value/Comment	Status	Support
CR1	Reserved bits	37.2.1	Set to zero	M	Yes [ ]
CR2	Default encoding of Remote Fault bits	37.2.1.5	0b00	M	Yes [ ]

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37.5.4.2.2 Remote Fault functions

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Remote Fault encoding	37.2.1.5		RF:M	Yes [ ] N/A [ ]
RF2	Use of Remote Fault Message Page code	37.2.1.5	To signal additional fault information	RF:O	Yes [ ] No [ ]
RF3	Notification duration	37.2.1.5	Remains set until transition to IDLE_DETECT state, then reset to 0b00	RF:M	Yes [ ] N/A [ ]
RF4	Status Register RF bit (1.4)	37.2.1.5	Upon detection of nonzero Remote Fault encoding	RF:M	Yes [ ] N/A [ ]
RF5	Offline indication	37.2.1.5.2	0b01	RF:O	Yes [ ] No [ ]
RF6	Link_Failure indication	37.2.1.5.3	0b10	RF:O	Yes [ ] No [ ]
RF7	Auto-Negotiation_Error	37.2.1.5.4	0b11	RF:M	Yes [ ] N/A [ ]

37.5.4.2.3 AN transmit functions

Item	Feature	Subclause	Value/Comment	Status	Support
TX1	PCS Transmit function support	37.2.2		M	Yes [ ]
TX2	Transmission of non-possessive abilities	37.2.2	A device shall not transmit an ability it does not possess.	M	Yes [ ]

37.5.4.2.4 AN receive functions

Item	Feature	Subclause	Value/Comment	Status	Support
RX1	PCS Receive function support	37.2.3		M	Yes [ ]

37.5.4.2.5 Priority resolution functions

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	Full duplex priority over half duplex	37.2.4.2		M	Yes [ ]
PR2	Priority resolution for pause capability	37.2.4.2	Specified in Table 37–4	M	Yes [ ]

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37.5.4.2.6 Next Page functions

Item	Feature	Subclause	Value/Comment	Status	Support
NP1	Transmission of Message Pages with a Null message code	37.2.4.3	Upon local device completion of Next Page requests	NP:M	Yes [ ] N/A [ ]
NP2	Recognition of Message Pages with a Null message code	37.2.4.3	Signifies the end of link partner Next Page information	NP:M	Yes [ ] N/A [ ]
NP3	Initial Next Page exchange	37.2.4.3	Upon advertisement of NP ability by both devices	NP:M	Yes [ ] N/A [ ]
NP4	Next Page Receipt Ability	37.2.4.3	Indicated by advertising NP ability via the NP bit	NP:M	Yes [ ] N/A [ ]
NP5	Next Page Config_Reg encoding	37.2.4.3.1		NP:M	Yes [ ] N/A [ ]
NP6	Next Page (NP) bit setting	37.2.4.3.2	For link_timer after entry into COMPLETE_ACKNOWL-EDGE state	NP:M	Yes [ ] N/A [ ]
NP7	Message Page (MP) bit setting	37.2.4.3.4		NP:M	Yes [ ] N/A [ ]
NP8	Acknowledge 2 (Ack2) bit setting	37.2.4.3.5		NP:M	Yes [ ] N/A [ ]
NP9	Message Code Field combinations	37.2.4.3.8	Reserved combinations shall not be transmitted.	NP:M	Yes [ ] N/A [ ]
NP10	Next Page usage rules	37.2.4.3.11		NP:M	Yes [ ] N/A [ ]

37.5.4.2.7 Management registers

Item	Feature	Subclause	Value/Comment	Status	Support
MR1	Control and Status registers	37.1.4.2.1		GMII:M	Yes [ ] N/A [ ]
MR2	Register usage	37.2.5.1	Logical equivalent of Registers 0, 1, 4, 5, 6 and 15	GMII:M	Yes [ ] N/A [ ]
MR3	Next Page Register usage	37.2.5.1	Logical equivalent of Registers 7 and 8	NPM:M	Yes [ ] N/A [ ]
MR4	Page Received resetting	37.2.5.1.5	Reset upon read to AN expansion register	M	Yes [ ]

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38. Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-LX (long wavelength laser) and 1000BASE-SX (short wavelength laser)

38.1 Overview

This clause specifies the 1000BASE-SX PMD and the 1000BASE-LX PMD (including MDI) and baseband medium for multimode and single-mode fiber. In order to form a complete Physical Layer, it shall be integrated with the 1000BASE-X PCS and PMA of Clause 36, and integrated with the management functions which are accessible through the Management Interface defined in Clause 35, which are hereby incorporated by reference.

38.1.1 Physical Medium Dependent (PMD) sublayer service interface

The following specifies the services provided by the 1000BASE-SX and 1000BASE-LX PMD. These PMD sublayers are described in an abstract manner and do not imply any particular implementation. It should be noted that these services are based on similar interfaces defined in ANSI INCITS 230-1994 (FC-PH).

The PMD Service Interface supports the exchange of encoded 8B/10B characters between PMA entities. The PMD translates the encoded 8B/10B characters to and from signals suitable for the specified medium.

The following primitives are defined:

PMD_UNITDATA.request
PMD_UNITDATA.indication
PMD_SIGNAL.indication

NOTE—Delay requirements from the MDI to GMII that include the PMD layer are specified in Clause 36. Of this budget, 4 ns is allocated for each of the transmit and receive functions of the PMD.

38.1.1.1 PMD_UNITDATA.request

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMA to the PMD.

38.1.1.1.1 Semantics of the service primitive

PMD_UNITDATA.request (tx_bit)

The data conveyed by PMD_UNITDATA.request is a continuous sequence of encoded 8B/10B characters. The tx_bit parameter can take one of two values: ONE or ZERO.

38.1.1.1.2 When generated

The PMA continuously sends the appropriate encoded 8B/10B characters to the PMD for transmission on the medium, at a nominal 1.25 GBd signaling speed.

38.1.1.1.3 Effect of receipt

Upon receipt of this primitive, the PMD converts the specified encoded 8B/10B characters into the appropriate signals on the MDI.

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38.1.1.2 PMD_UNITDATA.indication

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMD to the PMA.

38.1.1.2.1 Semantics of the service primitive

PMD_UNITDATA.indication (rx_bit)

The data conveyed by PMD_UNITDATA.indication is a continuous sequence of encoded 8B/10B characters. The rx_bit parameter can take one of two values: ONE or ZERO.

38.1.1.2.2 When generated

The PMD continuously sends encoded 8B/10B characters to the PMA corresponding to the signals received from the MDI.

38.1.1.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

38.1.1.3 PMD_SIGNAL.indication

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

38.1.1.3.1 Semantics of the service primitive

PMD_SIGNAL.indication(SIGNAL_DETECT)

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting light at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, then rx_bit is undefined, but consequent actions based on PMD_UNITDATA.indication, where necessary, interpret rx_bit as a logic ZERO.

NOTE—SIGNAL_DETECT = OK does not guarantee that rx_bit is known good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the 10^{-12} BER objective.

38.1.1.3.2 When generated

The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT.

38.1.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

38.1.2 Medium Dependent Interface (MDI)

The MDI, a physical interface associated with a PMD, is composed of an electrical or optical medium connection.

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38.2 PMD functional specifications

The 1000BASE-X PMDs perform the Transmit and Receive functions that convey data between the PMD service interface and the MDI.

38.2.1 PMD block diagram

For purposes of system conformance, the PMD sublayer is standardized at the following points. The optical transmit signal is defined at the output end of a patch cord (TP2), between 2 and 5 m in length, of a type consistent with the link type connected to the transmitter receptacle defined in 38.11.2. If a single-mode fiber offset-launch mode-conditioning patch cord is used, the optical transmit signal is defined at the end of this single-mode fiber offset-launch mode-conditioning patch cord at TP2. Unless specified otherwise, all transmitter measurements and tests defined in 38.6 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) connected to the receiver receptacle defined in 38.11.2. Unless specified otherwise, all receiver measurements and tests defined in 38.6 are made at TP3.

TP1 and TP4 are standardized reference points for use by implementers to certify component conformance. The electrical specifications of the PMD service interface (TP1 and TP4) are not system compliance points (these are not readily testable in a system implementation). It is expected that in many implementations, TP1 and TP4 will be common between 1000BASE-SX, 1000BASE-LX, and 1000BASE-CX (Clause 39).

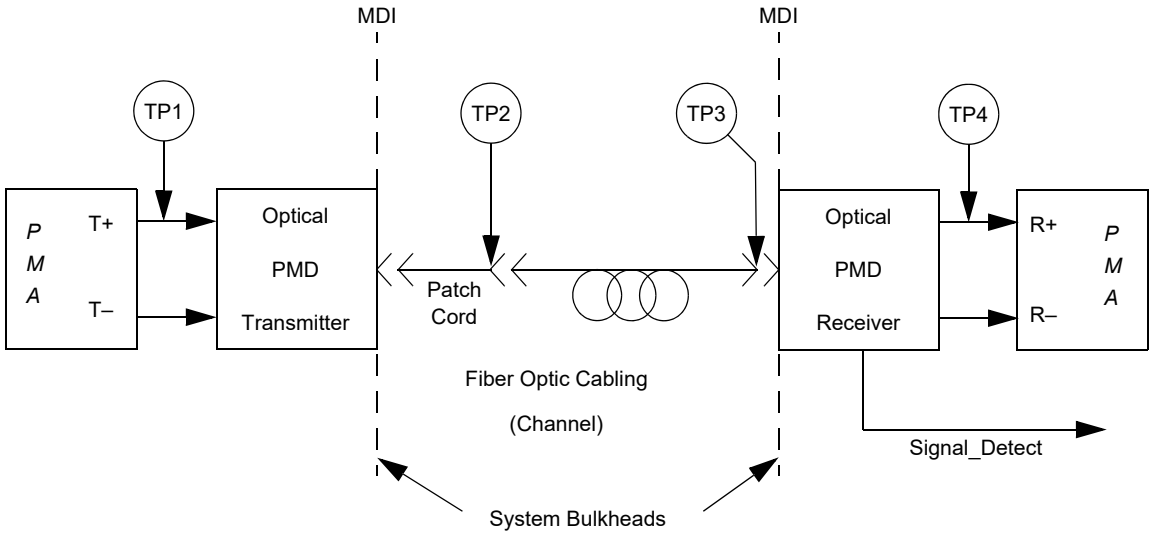

Figure 38–1—1000BASE-X block diagram

38.2.2 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the optical specifications in this clause. The higher optical power level shall correspond to tx_bit = ONE.

38.2.3 PMD receive function

The PMD Receive function shall convey the bits received from the MDI according to the optical specifications in this clause to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). The higher optical power level shall correspond to rx_bit = ONE.

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38.2.4 PMD signal detect function

The PMD Signal Detect function shall report to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indication is intended to be an indicator of optical signal presence.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 38–1. The PMD receiver is not required to verify whether a compliant 1000BASE-X signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 38–1—SIGNAL_DETECT value definition

Receive conditions	Signal detect value
Input_optical_power ≤ –30 dBm	FAIL
Input_optical_power ≥ Receive sensitivity AND compliant 1000BASE-X signal input	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD due to cross talk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations which generate the SIGNAL_DETECT parameter values in response to the amplitude of the 8B/10B modulation of the optical signal and implementations that respond to the average optical power of the 8B/10B-modulated optical signal.

38.3 PMD to MDI optical specifications for 1000BASE-SX

The operating range for 1000BASE-SX is defined in Table 38–2. A 1000BASE-SX compliant transceiver supports both multimode fiber media types listed in Table 38–2 (i.e., both 50 μm and 62.5 μm multimode fiber) according to the specifications defined in 38.11. A transceiver that exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a 50 μm solution operating at 600 m meets the minimum range requirement of 2 to 550 m).

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Table 38–2—Operating range for 1000BASE-SX over each optical fiber type

Fiber type	Modal bandwidth @ 850 nm (min. overfilled launch) (MHz · km)	Minimum range (m)
62.5 μm MMF	160	2 to 220
62.5 μm MMF	200	2 to 275
50 μm MMF	400	2 to 500
50 μm MMF	500	2 to 550
SMF	N/A	Not supported

38.3.1 Transmitter optical specifications

The 1000BASE-SX transmitter shall meet the specifications defined in Table 38–3 per measurement techniques defined in 38.6. It shall also meet a transmit mask of the eye measurement as defined in 38.6.5.

Table 38–3—1000BASE-SX transmit characteristics

Description	62.5 μm MMF	50 μm MMF	Unit
Transmitter type	Shortwave Laser		
Signaling speed (range)	1.25 ± 100 ppm		GBd
Wavelength (λ, range)	770 to 860		nm
T_{rise}/T_{fall} (max; 20%-80%; λ > 830 nm)	0.26		ns
T_{rise}/T_{fall} (max; 20%-80%; λ ≤ 830 nm)	0.21		ns
RMS spectral width (max)	0.85		nm
Average launch power (max)	See footnote [a]		dBm
Average launch power (min)	–9.5		dBm
Average launch power of OFF transmitter (max)[b]	–30		dBm
Extinction ratio (min)	9		dB
RIN (max)	–117		dB/Hz
Coupled Power Ratio (CPR) (min)[c]	9 < CPR		dB

[a]The 1000BASE-SX launch power shall be the lesser of the Hazard Level 1 safety limit as defined by 38.7.2 or the average receive power (max) defined by Table 38–4.
[b]Examples of an OFF transmitter are: no power supplied to the PMD, laser shutdown for safety conditions, activation of a "transmit disable" or other optional module laser shut down conditions. During all conditions when the PMA is powered, the ac signal (data) into the transmit port will be valid encoded 8B/10B patterns (this is a requirement of the PCS layers) except for short durations during system power-on-reset or diagnostics when the PMA is placed in a loopback mode.
[c]Radial overfilled launches as described in 38A.2, while they may meet CPR ranges, should be avoided.

The CPR specification provides sufficient mode volume so that individual multimode fiber (MMF) modes do not dominate fiber performance. This reduces the effect of peak-to-peak differential mode delay (DMD) between the launched mode groups and diminishes the resulting pulse-splitting-induced nulls in the frequency response.

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38.3.2 Receive optical specifications

The 1000BASE-SX receiver shall meet the specifications defined in Table 38–4 per measurement techniques defined in 38.6. The sampling instant is defined to occur at the eye center. The receive sensitivity includes the extinction ratio penalty.

Table 38–4—1000BASE-SX receive characteristics

Description	62.5 μm MMF	50 μm MMF	Unit
Signaling Speed (range)	1.25 ± 100 ppm		GBd
Wavelength (range)	770 to 860		nm
Average receive power (max)	0		dBm
Receive sensitivity	–17		dBm
Return loss (min)	12		dB
Stressed receive sensitivity[a, b]	–12.5	–13.5	dBm
Vertical eye-closure penalty[c]	2.60	2.20	dB
Receive electrical 3 dB upper cutoff frequency (max)	1500		MHz

[a]Measured with conformance test signal at TP3 (see 38.6.11) for BER = 10^{-12} at the eye center.
[b]Measured with a transmit signal having a 9 dB extinction ratio. If another extinction ratio is used, the stressed receive sensitivity should be corrected for the extinction ratio penalty.
[c]Vertical eye-closure penalty is a test condition for measuring stressed receive sensitivity. It is not a required characteristic of the receiver.

38.3.3 Illustrative 1000BASE-SX link power budget and penalties

The worst-case power budget and link penalties for a 1000BASE-SX channel are shown in Table 38–5.

Table 38–5—Worst-case 1000BASE-SX link power budget and penalties[a]

Parameter	62.5 μm MMF		50 μm MMF		Unit
Modal bandwidth as measured at 850 nm (minimum, overfilled launch)	160	200	400	500	MHz · km
Link power budget	7.5	7.5	7.5	7.5	dB
Operating distance	220	275	500	550	m
Channel insertion loss[b, c]	2.38	2.60	3.37	3.56	dB
Link power penalties[c]	4.27	4.29	4.07	3.57	dB
Unallocated margin in link power budget[c]	0.84	0.60	0.05	0.37	dB

[a]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[b]Operating distances used to calculate the channel insertion loss (see 1.4) are the maximum values specified in Table 38–2.
[c]A wavelength of 830 nm is used to calculate channel insertion loss, link power penalties, and unallocated margin.

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38.4 PMD to MDI optical specifications for 1000BASE-LX

The operating range for 1000BASE-LX is defined in Table 38–6. A 1000BASE-LX compliant transceiver supports all media types listed in Table 38–6 (i.e., 50 μm and 62.5 μm multimode fiber, and single-mode fiber) according to the specifications defined in 38.11. A transceiver which exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a single-mode solution operating at 5500 m meets the minimum range requirement of 2 to 5000 m).

Table 38–6—Operating range for 1000BASE-LX over each optical fiber type

Fiber type	Modal bandwidth @ 1300 nm (min. overfilled launch) (MHz · km)	Minimum range (m)
62.5 μm MMF	500	2 to 550
50 μm MMF	400	2 to 550
50 μm MMF	500	2 to 550
SMF	N/A	2 to 5000

38.4.1 Transmitter optical specifications

The 1000BASE-LX transmitter shall meet the specifications defined in Table 38–7 per measurement techniques defined in 38.6. It shall also meet a transmit mask of the eye measurement as defined in 38.6.5. To ensure that the specifications of Table 38–7 are met with MMF links, the 1000BASE-LX transmitter output shall be coupled through a single-mode fiber offset-launch mode-conditioning patch cord, as defined in 38.11.4.

Table 38–7—1000BASE-LX transmit characteristics

Description	62.5 μm MMF	50 μm MMF	SMF	Unit
Transmitter type	Longwave Laser			
Signaling speed (range)	1.25 ± 100 ppm			GBd
Wavelength (range)	1270 to 1355			nm
T_{rise}/T_{fall} (max, 20-80% response time)	0.26			ns
RMS spectral width (max)	4			nm
Average launch power (max)	–3			dBm
Average launch power (min)	–11.5	–11.5	–11.0	dBm
Average launch power of OFF transmitter (max)	–30			dBm
Extinction ratio (min)	9			dB
RIN (max)	–120			dB/Hz
Coupled Power Ratio (CPR)[a]	28 < CPR< 40	12 < CPR < 20	N/A	dB

[a]Due to the dual media (single-mode and multimode) support of the LX transmitter, fulfillment of this specification requires a single-mode fiber offset-launch mode-conditioning patch cord described in 38.11.4 for MMF operation. This patch cord is not used for single-mode operation.

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Conditioned launch (CL) produces sufficient mode volume so that individual multimode fiber (MMF) modes do not dominate fiber performance. This reduces the effect of peak-to-peak differential mode delay (DMD) between the launched mode groups and diminishes the resulting pulse-splitting-induced nulls in the frequency response.

A CL is produced by using a single-mode fiber offset-launch mode-conditioning patch cord, inserted at both ends of a full duplex link, between the optical PMD MDI and the remainder of the link segment. The single-mode fiber offset-launch mode-conditioning patch cord contains a fiber of the same type as the cable (i.e., 62.5 μm or 50 μm fiber) connected to the optical PMD receiver input MDI and a specialized fiber/connector assembly connected to the optical PMD transmitter output.

38.4.2 Receive optical specifications

The 1000BASE-LX receiver shall meet the specifications defined in Table 38–8 per measurement techniques defined in 38.6. The sampling instant is defined to occur at the eye center. The receive sensitivity includes the extinction ratio penalty.

Table 38–8—1000BASE-LX receive characteristics

Description	Value	Unit
Signaling speed (range)	1.25 ± 100 ppm	GBd
Wavelength (range)	1270 to 1355	nm
Average receive power (max)	–3	dBm
Receive sensitivity	–19	dBm
Return loss (min)	12	dB
Stressed receive sensitivity[a, b]	–14.4	dBm
Vertical eye-closure penalty[c]	2.60	dB
Receive electrical 3 dB upper cutoff frequency (max)	1500	MHz

[a]Measured with conformance test signal at TP3 (see 38.6.11) for BER = 10^{-12} at the eye center.
[b]Measured with a transmit signal having a 9 dB extinction ratio. If another extinction ratio is used, the stressed receive sensitivity should be corrected for the extinction ratio penalty.
[c]Vertical eye-closure penalty is a test condition for measuring stressed receive sensitivity. It is not a required characteristic of the receiver.

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38.4.3 Illustrative 1000BASE-LX link power budget and penalties

The worst-case power budget and link penalties for a 1000BASE-LX channel are shown in Table 38–9.

Table 38–9—Worst-case 1000BASE-LX link power budget and penalties[a]

Parameter	62.5 μm MMF	50 μm MMF		SMF	Unit
Modal bandwidth as measured at 1300 nm (minimum, overfilled launch)	500	400	500	N/A	MHz · km
Link power budget	7.5	7.5	7.5	8.0	dB
Operating distance	550	550	550	5000	m
Channel insertion loss[b, c]	2.35	2.35	2.35	4.57	dB
Link power penalties[c]	3.48	5.08	3.96	3.27	dB
Unallocated margin in link power budget[c]	1.67	0.07	1.19	0.16	dB

[a]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[b]Operating distances used to calculate the channel insertion loss (see 1.4) are the maximum values specified in Table 38–6.
[c]A wavelength of 1270 nm is used to calculate channel insertion loss, link power penalties, and unallocated margin.

38.5 Jitter specifications for 1000BASE-SX and 1000BASE-LX

Numbers in the Table 38–10 represent high-frequency jitter (above 637 kHz) and do not include low-frequency jitter or wander. Implementations shall conform to the normative values highlighted **in bold** in Table 38–10 (see measurement procedure in 38.6.8). All other values are optional.

Table 38–10—1000BASE-SX and 1000BASE-LX jitter budget

Compliance point	Total jitter[a]		Deterministic jitter	
	UI	ps	UI	ps
TP1	**0.240**	**192**	0.100	80
TP1 to TP2	0.284	227	0.100	80
TP2	**0.431**	**345**	0.200	160
TP2 to TP3	0.170	136	0.050	40
TP3	**0.510**	**408**	0.250	200
TP3 to TP4	0.332	266	0.212	170
TP4[b]	**0.749**	**599**	0.462	370

[a] Total jitter is composed of both deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter at that point.
[b]Measured with a conformance test signal at TP3 (see 38.6.11) set to an average optical power 0.5 dB greater than the stressed receive sensitivity from Table 38–4 for 1000BASE-SX and Table 38–8 for 1000BASE-LX.

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38.6 Optical measurement requirements

All optical measurements shall be made through a short patch cable, between 2 and 5 m in length. If a single-mode fiber offset-launch mode-conditioning patch cord is used, the optical transmit signal is defined at the output end (TP2) of the single-mode fiber offset-launch mode-conditioning patch cord.

38.6.1 Center wavelength and spectral width measurements

The center wavelength and spectral width (RMS) shall be measured using an optical spectrum analyzer per the centroidal wavelength and RMS spectral width definitions in IEC 61280-1-3. Center wavelength and spectral width shall be measured under modulated conditions using a valid 1000BASE-X signal.

38.6.2 Optical power measurements

Optical power shall be measured using the methods specified in ANSI/TIA/EIA-455-95. This measurement may be made with the node transmitting any valid encoded 8B/10B data stream.

38.6.3 Extinction ratio measurements

Extinction ratio shall be measured using the methods specified in IEC 61280-2-2. This measurement may be made with the node transmitting a data pattern defined in 36A.2. This is a repeating K28.7 data pattern. The extinction ratio is measured under fully modulated conditions with worst-case reflections.

NOTE—A repeating K28.7 data pattern generates a 125 MHz square wave.

38.6.4 Relative Intensity Noise (RIN)

This procedure describes a component test which may not be appropriate for a system level test depending on the implementation. RIN shall be measured according to 58.7.7 with the following exceptions:

1) the low pass filter bandwidth is 937.5 MHz
2) step d) of the test procedure is replaced by measuring the value of the photocurrent of the optical to electrical converter I_{oe}
3) step e) of the test procedure is replaced by using the following equation to evaluate RIN:

$$\mathrm{RIN} = 10\log_{10}\frac{P_N}{BW \times I_{oe}^2 \times R} - G \ \text{(dB/Hz)}$$

where:

RIN	is the relative intensity noise,
P_N	is the electrical noise power in Watts with modulation off,
BW	is the low-pass bandwidth of apparatus – high-pass bandwidth of apparatus due to DC-blocking capacitor,
I_{oe}	is the photocurrent of the optical to electrical converter,
R	is the effective load impedance of the optical to electrical converter (for example, a 50 Ω detector load in parallel with a 50 Ω power meter would give R equal to 25),
G	is the Gain in dB of any amplifier in the noise measurement path.

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38.6.5 Transmitter optical waveform (transmit eye)

The required transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 38–2. The transmit mask is not used for response time and jitter specification.

Normalized amplitudes of 0.0 and 1.0 represent the amplitudes of logic ZERO and ONE, respectively.

The eye shall be measured with respect to the mask of the eye using a fourth-order Bessel-Thomson filter having a transfer function given by

$$H(p) = \frac{105}{105 + 105y + 45y^2 + 10y^3 + y^4}$$

where

$$y = 2.114p\ ; \quad p = \frac{j\omega}{\omega_r}\ ; \quad \omega_r = 2\pi f_r\ ; \quad f_r = 0.9375\text{GHz}$$

and where the filter response vs. frequency range for this fourth order Bessel-Thomson filter is defined in ITU-T G.957, along with the allowed tolerances (STM-16 values) for its physical implementation.

NOTE 1—This Bessel-Thomson filter is not intended to represent the noise filter used within an optical receiver, but is intended to provide uniform measurement conditions at the transmitter.

NOTE 2—The fourth-order Bessel-Thomson filter is reactive. In order to suppress reflections, a 6 dB attenuator may be required at the filter input and/or output.

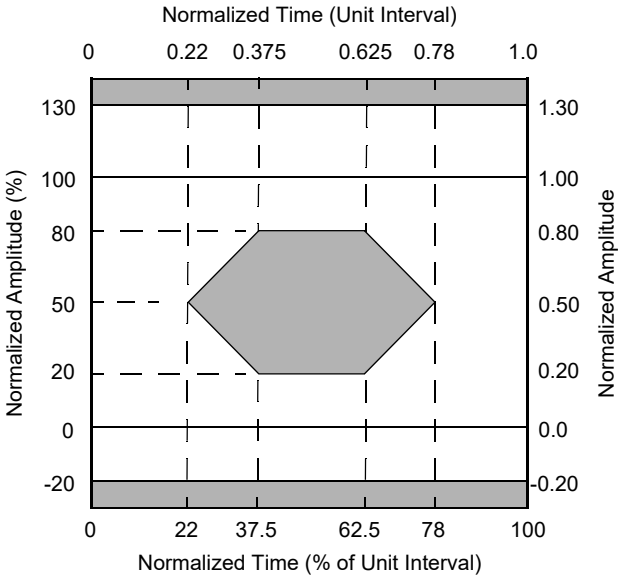

Figure 38–2—Transmitter eye mask definition

38.6.6 Transmit rise/fall characteristics

Optical response time specifications are based on unfiltered waveforms. Some lasers have overshoot and ringing on the optical waveforms which, if unfiltered, reduce the accuracy of the measured 20–80%

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response times. For the purpose of standardizing the measurement method, measured waveforms shall conform to the mask defined in Figure 38–2. If a filter is needed to conform to the mask, the filter response should be removed using the equation:

$$T_{\text{rise,fall}} = \sqrt{(T_{\text{rise,fall\_measured}})^2 - (T_{\text{rise,fall\_filter}})^2}$$

where the filter may be different for rise and fall. Any filter should have an impulse response equivalent to a fourth order Bessel-Thomson filter. The fourth-order Bessel-Thomson filter defined in 38.6.5 may be a convenient filter for this measurement; however, its low bandwidth adversely impacts the accuracy of the $T_{\text{rise,fall}}$ measurements.

38.6.7 Receive sensitivity measurements

The receive sensitivity shall be measured using a worst-case extinction ratio penalty while sampling at the eye center.

The stressed receive sensitivity shall be measured using the conformance test signal at TP3, as specified in 38.6.11. After correcting for the extinction ratio of the source, the stressed receive sensitivity shall meet the conditions specified in Table 38–4 for 1000BASE-SX and in Table 38–8 for 1000BASE-LX.

38.6.8 Total jitter measurements

All total jitter measurements shall be made according to the method in ANSI INCITS 230-1994 (FC-PH), Annex A, A.4.2, *Active output interface eye opening measurement*. Total jitter at TP2 shall be measured utilizing a BERT (Bit Error Ratio Test) test set. References to use of the Bessel-Thomson filter shall substitute use of the Bessel-Thomson filter defined in this clause (see 38.6.5). The test shall utilize the mixed frequency test pattern specified in 36A.3.

Total jitter at TP4 shall be measured using the conformance test signal at TP3, as specified in 38.6.11. The optical power shall be 0.5 dB greater than (to account for eye opening penalty) the stressed receive sensitivity level in Table 38–4 for 1000BASE-SX and in Table 38–8 for 1000BASE-LX. This power level shall be corrected if the extinction ratio differs from the specified extinction ratio (min) of 9 dB. Measurements shall be taken directly at TP4 without additional Bessel-Thomson filters.

Jitter measurement may use a clock recovery unit (commonly referred to in the industry as a “golden PLL”) to remove low-frequency jitter from the measurement as shown in Figure 38–3. The clock recovery unit has a low-pass filter with 20 dB/decade rolloff with –3 dB point of 637 kHz. For this measurement, the recovered clock will run at the signaling speed. The golden PLL is used to approximate the PLL in the deserializer function of the PMA. The PMA deserializer is able to track a large amount of low-frequency jitter (such as drift or wander) below its bandwidth. This low-frequency jitter would create a large measurement penalty, but does not affect operation of the link.

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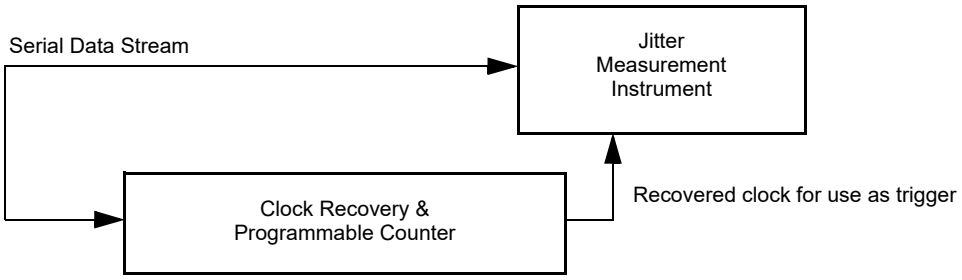

Figure 38–3—Utilization of clock recovery unit during measurement

38.6.9 Deterministic jitter measurement (optional)

Deterministic jitter should be measured according to ANSI INCITS 230-1994 (FC-PH), Annex A, A.4.3, *DJ Measurement.* The test utilizes the mixed frequency test pattern specified in 36A.3. This method utilizes a digital sampling scope to measure actual vs. predicted arrival of bit transitions of the 36A.3 data pattern (alternating K28.5 code-groups).

It is convenient to use the clock recovery unit described in 38.6.8 for purposes of generating a trigger for the test equipment. This recovered clock should have a frequency equivalent to 1/20th of the signaling speed.

38.6.10 Coupled Power Ratio (CPR) measurements

Coupled Power Ratio (CPR) is measured in accordance with ANSI/EIA/TIA-526-14A [B12]. Measured CPR values are time averaged to eliminate variation from speckle fluctuations. The coupled power ratio shall be measured for compliance with Table 38–3 and Table 38–7.

38.6.11 Conformance test signal at TP3 for receiver testing

Receivers being tested for conformance to the stressed receive sensitivity requirements of 38.6.7 and the total jitter requirements of 38.6.8 shall be tested using a conformance test signal at TP3 conforming to the requirements described in Figure 38–4. The conformance test signal shall be generated using the short continuous random test pattern defined in 36A.5. The conformance test signal is conditioned by applying deterministic jitter (DJ) and intersymbol interference (ISI). The conditioned conformance test signal is shown schematically in Figure 38–4. The horizontal eye closure (reduction of pulse width) caused by the duty cycle distortion (DCD) component of DJ shall be no less than 65 ps. The vertical eye-closure penalty shall be greater than or equal to the value specified in Table 38–4 for 1000BASE-SX and Table 38–8 for 1000BASE-LX. The DJ cannot be added with a simple phase modulation, which does not account for the DCD component of DJ.

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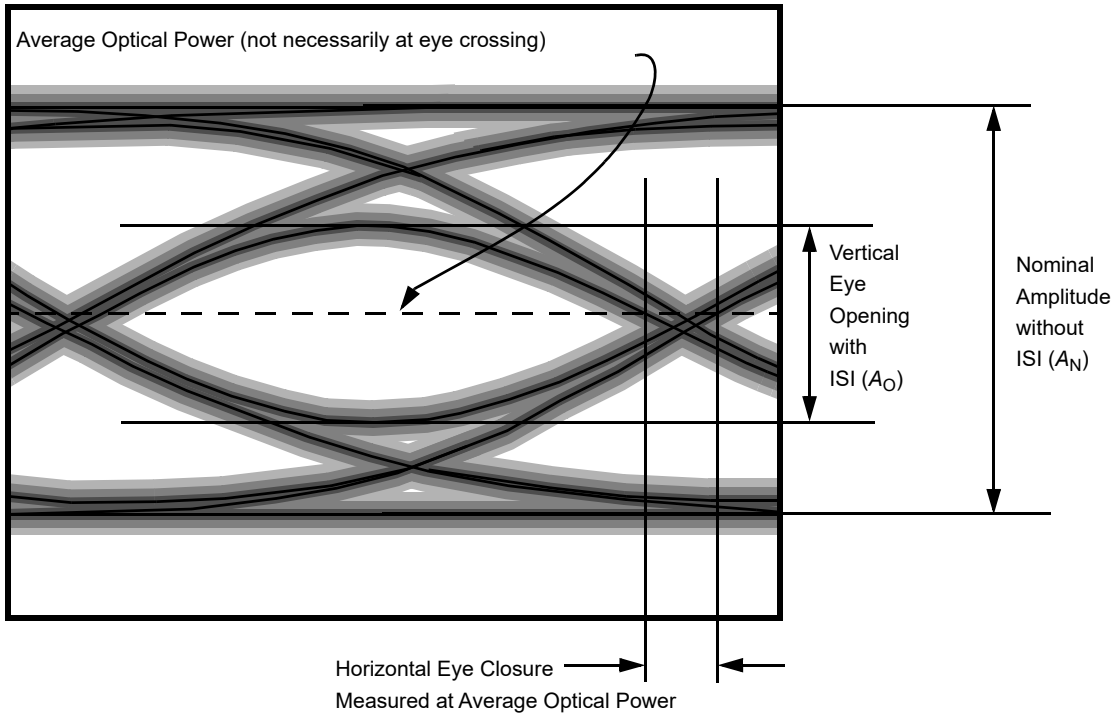

Figure 38–4—Required characteristics of the conformance test signal at TP3

The vertical eye-closure penalty is given by

$$\text{Vertical eye-closure penalty [dB]} = 10\log\frac{A_N}{A_O}$$

where A_O is the amplitude of the eye opening, and A_N is the normal amplitude without ISI, as measured in Figure 38–4.

Figure 38–5 shows the recommended test set up for producing the conformance test signal at TP3. The coaxial cable is adjusted in length to produce the correct DCD component of DJ. Since the coaxial cable can produce the incorrect ISI, a limiting amplifier is used to restore fast rise and fall times. A Bessel-Thomson filter is selected to produce the minimum ISI induced eye closure as specified per Table 38–4 for 1000BASE-SX and Table 38–8 for 1000BASE-LX. This conditioned signal is used to drive a high bandwidth linearly modulated laser source.

The vertical and horizontal eye closures to be used for receiver conformance testing are verified using a fast photodetector and amplifier. The bandwidth of the photodetector shall be at least 2.5 GHz and be coupled through a 1.875 GHz fourth-order Bessel-Thomson filter to the oscilloscope input. Special care should be taken to ensure that all the light from the fiber is collected by the fast photodetector and that there is negligible mode selective loss, especially in the optical attenuator.

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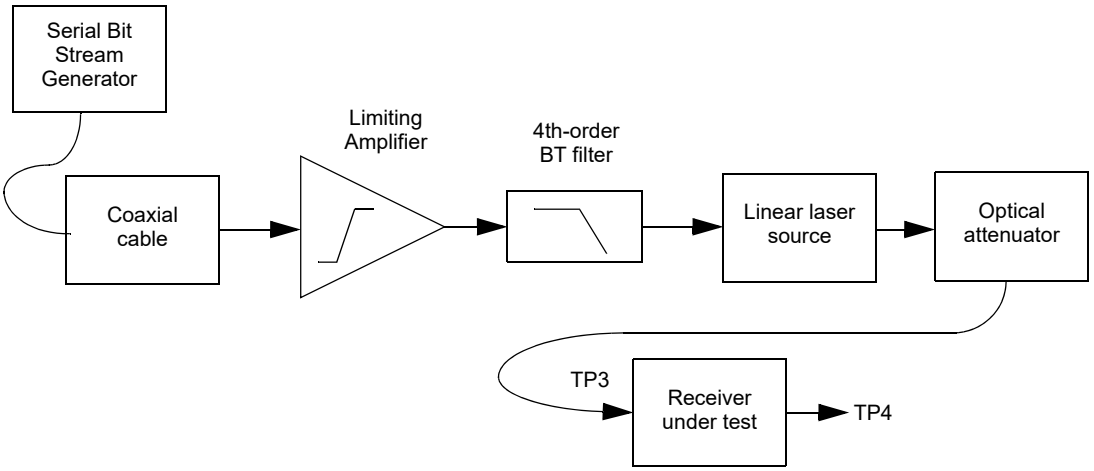

Figure 38–5—Apparatus for generating receiver conformance test signal at TP3

38.6.12 Measurement of the receiver 3 dB electrical upper cutoff frequency

The receiver 3 dB electrical upper cutoff frequency shall be measured as described below. The test setup is shown in Figure 38–6. The test is performed with a laser that is suitable for analog signal transmission. The laser is modulated by a digital data signal. In addition to the digital modulation, the laser is modulated with an analog signal. The analog and digital signals should be asynchronous. The data pattern to be used for this test is the short continuous random test pattern defined in 36A.5. The frequency response of the laser needs to be sufficient to allow it to respond to both the digital modulation and the analog modulation. The laser should be biased so that it remains linear when driven by the combined signals.

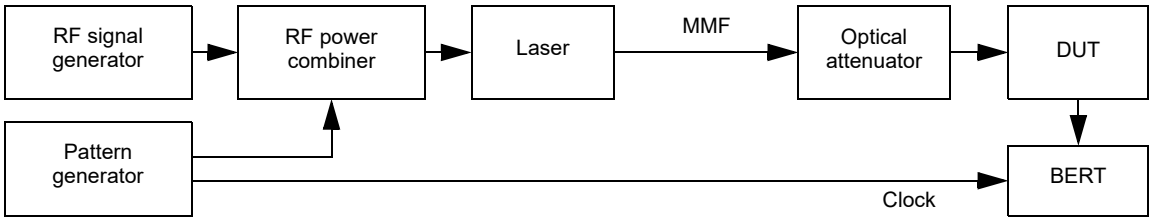

Figure 38–6—Test setup for receiver bandwidth measurement

The 3 dB upper cutoff frequency is measured using the following steps a) through e):

a) Calibrate the frequency response characteristics of the test equipment including the analog radio frequency (RF) signal generator, RF power combiner, and laser source. Measure the laser's extinction ratio according to 38.6.3. With the exception of extinction ratio, the optical source shall meet the requirements of Clause 38.
b) Configure the test equipment as shown in Figure 38–6. Take care to minimize changes to the signal path that could affect the system frequency response after the calibration in step a. Connect the laser output with no RF modulation applied to the receiver under test through an optical attenuator and taking into account the extinction ratio of the source, set the optical power to a level that approximates the stressed receive sensitivity level in Table 38–4 for 1000BASE-SX and in Table 38–8 for 1000BASE-LX.

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c) Locate the center of the eye with the BERT. Turn on the RF modulation while maintaining the same average optical power established in step b.
d) Measure the necessary RF modulation amplitude (in dBm) required to achieve a constant BER (e.g., 10^{-8}) for a number of frequencies.
e) The receiver 3 dB electrical upper cutoff frequency is that frequency where the corrected RF modulation amplitude (the measured amplitude in "d" corrected with the calibration data in "a") increases by 3 dB (electrical). If necessary, interpolate between the measured response values.

38.7 Environmental specifications

38.7.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

38.7.2 Laser safety

1000BASE-X optical transceivers shall be Hazard Level 1 laser certified under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore. Transceivers shall be certified to be in conformance with IEC 60825-1 and IEC 60825-2.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance and service. This documentation shall explicitly define requirements and usage restrictions on the host system necessary to meet these safety certifications.[78]

38.7.3 Installation

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

38.8 Environment

Normative specifications in this clause shall be met by a system integrating a 1000BASE-X PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

38.8.1 Electromagnetic emission

A system integrating a 1000BASE-X PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

[78]A host system that fails to meet the manufacturers requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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38.8.2 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

38.9 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters, according to the PMD-MDI type.

PMD MDI type 1000BASE-SX:

a) 1000BASE-SX
b) Applicable safety warnings

PMD MDI type 1000BASE-LX:

c) 1000BASE-LX
d) Applicable safety warnings

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 38.7.2.

38.10 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 38–7.

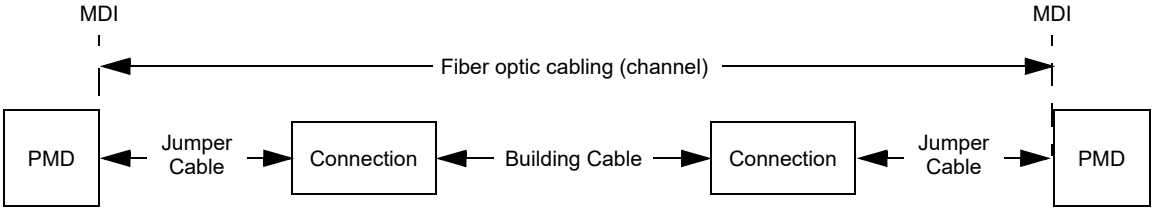

Figure 38–7—Fiber optic cabling model

The channel insertion loss is given in Table 38–11. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1 one-cord method for multimode cabling and IEC 61280-4-2 one-cord reference method for single-mode cabling. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

38.11 Characteristics of the fiber optic cabling

The 1000BASE-SX and 1000BASE-LX fiber optic cabling shall meet the specifications defined in Table 38–12. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. It also includes a connector plug at each end to connect to the MDI. The fiber optic cabling spans from one MDI to another MDI, as shown in Figure 38–7.

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Table 38–11—Channel insertion loss

Description	62.5 μm MMF			50 μm MMF			SMF	Unit
Wavelength	850	850	1300	850	850	1300	1310	nm
Modal bandwidth (min; overfilled launch)	160	200	500	400	500	400 or 500	N/A	MHz · km
Operating distance	220	275	550	500	550	550	5000	m
Channel insertion loss[a] [b]	2.33	2.53	2.32	3.25	3.43	2.32	4.5	dB

[a]These channel insertion loss numbers are based on the nominal operating wavelength.
[b]Operating distances used to calculate channel insertion loss are those listed in this table.

38.11.1 Optical fiber and cable

The fiber optic cable requirements are satisfied by the fibers specified in IEC 60793-2:1992. Types A1a (50/125 μm multimode), A1b (62.5/125 μm multimode), and B1 (single-mode) with the exceptions noted in Table 38–12.

Table 38–12—Optical fiber and cable characteristics

Description	62.5 μm MMF		50 μm MMF		SMF	Unit
Nominal fiber specification wavelength	**850**	**1300**	**850**	**1300**	**1310**	**nm**
Fiber cable attenuation (max)	3.75[a]	1.5	3.5	1.5	0.5	dB/km
Modal Bandwidth (min; overfilled launch)	160	500	400	400	N/A	MHz · km
	200	500	500	500	N/A	MHz · km
Zero dispersion wavelength (λ_0)	$1320 \le \lambda_0 \le 1365$		$1295 \le \lambda_0 \le 1320$		$1300 \le \lambda_0 \le 1324$	nm
Dispersion slope (max) (S_0)	0.11 for $1320 \le \lambda_0 \le 1348$ and $0.001(1458 - \lambda_0)$ for $1348 \le \lambda_0 \le 1365$		0.11 for $1300 \le \lambda_0 \le 1320$ and $0.001(\lambda_0 - 1190)$ for $1295 \le \lambda_0 \le 1300$		0.093	ps / nm^2 · km

[a]This value of attenuation is a relaxation of the standard (IEC 60793-2, type A1b, category less than or equal to 3.5 dB/km).

38.11.2 Optical fiber connection

An optical fiber connection as shown in Figure 38–7 consists of a mated pair of optical connectors. The 1000BASE-SX or 1000BASE-LX PMD is coupled to the fiber optic cabling through a connector plug into the MDI optical receptacle, as shown in 38.11.3.

38.11.2.1 Connection insertion loss

The insertion loss is specified for a connection, which consists of a mated pair of optical connectors.

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The maximum link distances for multimode fiber are calculated based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an average insertion loss equal to 0.5 dB (or less) per connection, or two connections (as shown in Figure 38–7) with a maximum insertion loss of 0.75 dB. Connections with different loss characteristics may be used provided the requirements of Table 38–11 and Table 38–12 are met.

The maximum link distances for single-mode fiber are calculated based on an allocation of 2.0 dB total connection and splice loss. For example, this allocation supports four connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 38–11 and Table 38–12 are met.

38.11.2.2 Connection return loss

The return loss for multimode connections shall be greater than 20 dB.

The return loss for single-mode connections shall be greater than 26 dB.

38.11.3 Medium Dependent Interface (MDI)

The 1000BASE-SX and 1000BASE-LX PMD is coupled to the fiber optic cabling through a connector plug into the MDI optical receptacle. The 1000BASE-SX and 1000BASE-LX MDI optical receptacles shall be the duplex SC, meeting the following requirements:

a) Meet the dimension and interface specifications of IEC 61754-4 [B33] and IEC 61754-4, Interface 4-2.
b) Meet the performance specifications as specified in ISO/IEC 11801.
c) Ensure that polarity is maintained.
d) The receive side of the receptacle is located on the left when viewed looking into the transceiver optical ports with the keys on the bottom surface.

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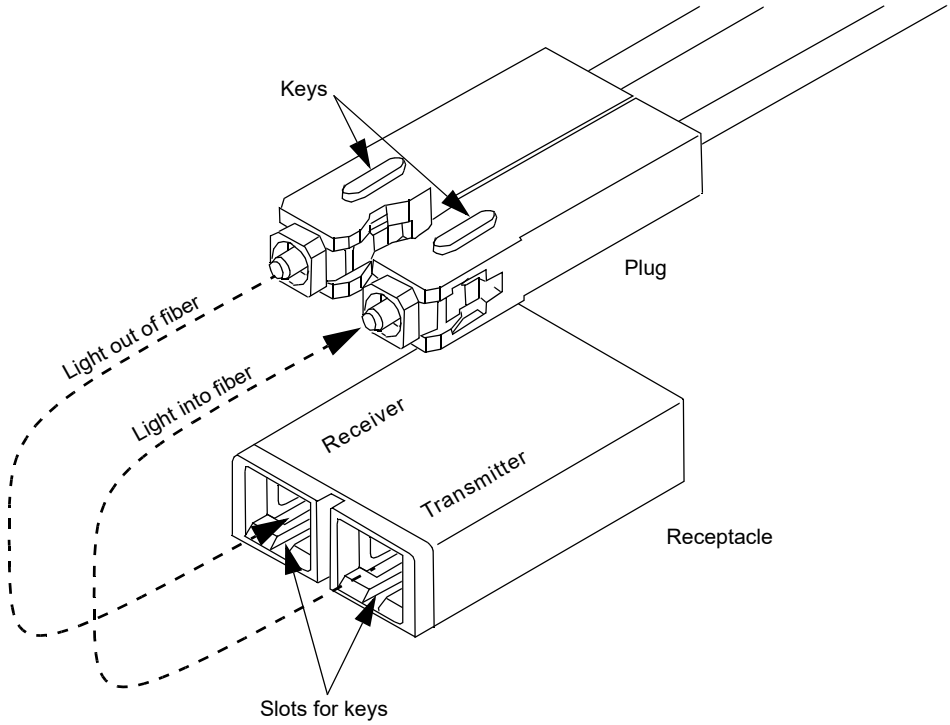
A sample drawing of a duplex SC connector and receptacle is provided in Figure 38–8.



NOTE—Connector keys are used for transmit/receive polarity only. The connector keys do not differentiate between single-mode and multimode connectors.

Figure 38–8—Duplex SC connector and receptacle (example)

38.11.4 Single-mode fiber offset-launch mode-conditioning patch cord for MMF operation of 1000BASE-LX

This subclause specifies an example embodiment of a mode conditioner for 1000BASE-LX operation with MMF cabling. The MMF cabling should meet all of the specifications of 38.10. For 1000BASE-LX the mode conditioner consists of a single-mode fiber permanently coupled off-center to a graded index fiber. This example embodiment of a patch cord is not intended to exclude other physical implementations of offset-launch mode conditioners. However, any implementation of an offset-launch mode conditioner used for 1000BASE-LX shall meet the specifications of Table 38–13. The offset launch has to be contained within the patch cord assembly and is not adjustable by the user.

Table 38–13—Single-mode fiber offset-launch mode conditioner specifications

Description	62.5 μm MMF	50 μm MMF	Unit
Maximum insertion loss	0.5	0.5	dB
Coupled Power Ratio (CPR)	28 < CPR < 40	12 < CPR < 20	dB
Optical center offset between SMF and MMF	17 < Offset < 23	10 < Offset < 16	μm
Maximum angular offset	1	1	degree

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All patch cord connecting ferrules containing the single-mode-to-multimode offset launch shall have single-mode tolerances (IEC 61754-4 [B33] grade 1 ferrule).

The single-mode fiber used in the construction of the single-mode fiber offset-launch mode conditioner shall meet the requirements of 38.11.1. The multimode fiber used in the construction of the single-mode fiber offset-launch mode conditioner shall be of the same type as the cabling over which the 1000BASE-LX link is to be operated. If the cabling is 62.5 μm MMF then the MMF used in the construction of the mode conditioner should be of type 62.5 μm MMF. If the cabling is 50 μm MMF, then the MMF used in the construction of the mode conditioner should be of type 50 μm MMF.

Figure 38–9 shows the preferred embodiment of the single-mode fiber offset-launch mode-conditioning patch cord. This patch cord consists of duplex fibers including a single-mode-to-multimode offset launch fiber connected to the transmitter MDI and a second conventional graded index MMF connected to the receiver MDI. The preferred configuration is a plug-to-plug patch cord since it maximizes the power budget margin of the 1000BASE-LX link. The single-mode end of the patch cord shall be labeled “To Equipment”. The multimode end of the patch cord shall be labeled “To Cable”. The color identifier of the single-mode fiber connector shall be blue. The color identifier of all multimode fiber connector plugs shall be beige. The patch cord assembly is labeled “Offset-launch mode-conditioning patch cord assembly”. Labelling identifies which size multimode fiber is used in the construction of the patch cord. The keying of the SC duplex optical plug ensures that the single-mode fiber end is automatically aligned to the transmitter MDI.

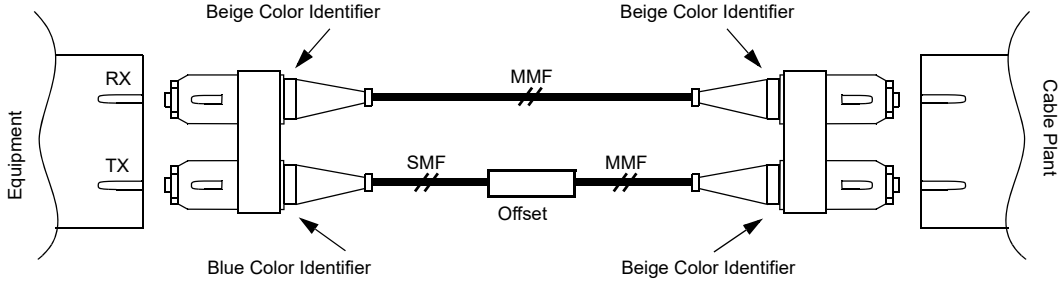

Figure 38–9—1000BASE-LX single-mode fiber offset-launch mode-conditioning patch cord assembly

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38.12 Protocol implementation conformance statement (PICS) proforma for Clause 38, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-LX (Long Wavelength Laser) and 1000BASE-SX (Short Wavelength Laser)[79]

38.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 38, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-LX (Long Wavelength Laser) and 1000BASE-SX (Short Wavelength Laser), shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

38.12.2 Identification

38.12.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

38.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 38, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-LX (Long Wavelength Laser) and 1000BASE-SX (Short Wavelength Laser)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[79] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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38.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*LX	1000BASE-LX PMD	38.1	Device supports long wavelength operation (1270–1355 nm).	O/1	Yes [ ] No [ ]
*SX	1000BASE-SX PMD	38.1	Device supports short wavelength operation (770–860 nm). Either this option, or option LX, has to be checked.	O/1	Yes [ ] No [ ]
*INS	Installation / cable	38.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]
*OFP	Single-mode offset-launch mode-conditioning patch cord	38.11.4	Items marked with OFP include installation practices and cable specifications not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]
*TP1	Standardized reference point TP1 exposed and available for testing.	38.2.1	This point may be made available for use by implementers to certify component conformance.	O	Yes [ ] No [ ]
*TP4	Standardized reference point TP4 exposed and available for testing.	38.2.1	This point may be made available for use by implementers to certify component conformance.	O	Yes [ ] No [ ]

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38.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-LX (Long Wavelength Laser) and 1000BASE-SX (Short Wavelength Laser)

38.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FN1	Integration with 1000BASE-X PCS and PMA and management functions	38.1		M	Yes [ ]
FN2	Transmit function	38.2.2	Convey bits requested by PMD_UNITDATA.request() to the MDI	M	Yes [ ]
FN3	Mapping between optical signal and logical signal for transmitter	38.2.2	Higher optical power is a logical 1.	M	Yes [ ]
FN4	Receive function	38.2.3	Convey bits received from the MDI to PMD_UNITDATA.indication()	M	Yes [ ]
FN5	Mapping between optical signal and logical signal for receiver	38.2.3	Higher optical power is a logical 1.	M	Yes [ ]
FN6	Signal detect function	38.2.4	Report to the PMD service interface the message PMD_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
FN7	Signal detect behavior	38.2.4	Meets requirements of Table 38–1	M	Yes [ ]

38.12.4.2 PMD to MDI optical specifications for 1000BASE-SX

Item	Feature	Subclause	Value/Comment	Status	Support
PMS1	Transmitter meets specifications in Table 38–3	38.3.1	Per measurement techniques in 38.6	SX:M	Yes [ ] N/A [ ]
PMS2	Transmitter eye measurement	38.3.1	Per 38.6.5	SX:M	Yes [ ] N/A [ ]
PMS3	Launch power	38.3.1	Lesser of Hazard Level 1 safety limit per 38.7.2 or maximum receive power in Table 38–4	SX:M	Yes [ ] N/A [ ]
PMS4	Receiver meets specifications in Table 38–4	38.3.2	Per measurement techniques in 38.6	SX:M	Yes [ ] N/A [ ]

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38.12.4.3 PMD to MDI optical specifications for 1000BASE-LX

Item	Feature	Subclause	Value/Comment	Status	Support
PML1	Transmitter meets specifications in Table 38–7	38.4.1	Per measurement techniques in 38.6	LX:M	Yes [ ] N/A [ ]
PML2	Transmitter eye measurement	38.4.1	Per 38.6.5	LX:M	Yes [ ] N/A [ ]
PML3	Offset-launch mode-conditioning patch cord	38.4.1	Required for LX multimode operation	LX:M	Yes [ ] N/A [ ]
PML4	Receiver meets specifications in Table 38–8	38.4.2	Per measurement techniques in 38.6	LX:M	Yes [ ] N/A [ ]

38.12.4.4 Jitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Total jitter specification at TP1	38.5	Meets specification of bold entries in Table 38–10	TP1:M	Yes [ ] N/A [ ]
JT2	Total jitter specification at TP2	38.5	Meets specification of bold entries in Table 38–10	M	Yes [ ]
JT3	Total jitter specification at TP3	38.5	Meets specification of bold entries in Table 38–10	INS:M	Yes [ ] N/A [ ]
JT4	Total jitter specification at TP4	38.5	Meets specification of bold entries in Table 38–10	TP4:M	Yes [ ] N/A [ ]

38.12.4.5 Optical measurement requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OR1	Length of patch cord used for measurements	38.6	2 to 5 m	M	Yes [ ]
OR2	Center wavelength and spectral width measurement conditions	38.6.1	Using optical spectrum analyzer per the centroidal wavelength and RMS spectral width definitions in IEC 61280-1-3	M	Yes [ ]
OR3	Center wavelength and spectral width measurement conditions	38.6.1	Under modulated conditions using a valid 1000BASE-X signal	M	Yes [ ]
OR4	Optical power measurement conditions	38.6.2	Per ANSI/TIA/EIA-455-95	M	Yes [ ]
OR5	Extinction ratio measurement conditions	38.6.3	Per IEC 61280-2-2 using patch cable per 38.6	M	Yes [ ]
OR6	RIN test methods	38.6.4	58.7.7 as modified by 38.6.4 using patch cable per 38.6	M	Yes [ ]

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38.12.4.5 Optical measurement requirements *(continued)*

Item	Feature	Subclause	Value/Comment	Status	Support
OR7	Transmit eye mask measurement conditions	38.6.5	Using fourth-order Bessel-Thomson filter per 38.6.5, using patch cable per 38.6	M	Yes [ ]
OR8	Transmit rise/fall measurement conditions	38.6.6	Waveforms conform to mask in Figure 38–2, measure from 20% to 80%, using patch cable per 38.6	M	Yes [ ]
OR9	Receive sensitivity measurement conditions	38.6.7	Worst-case extinction ratio penalty while sampling at the eye center using patch cable per 38.6	M	Yes [ ]
OR10	Stressed receive sensitivity	38.6.7	Per 38.6.11, using patch cable per 38.6	M	Yes [ ]
OR11	Stressed receive sensitivity	38.6.7	Meet Table 38–4	SX:M	Yes [ ] N/A [ ]
OR12	Stressed receive sensitivity	38.6.7	Meet Table 38–8	LX:M	Yes [ ] N/A [ ]
OR13	Total jitter measurement conditions	38.6.8	ANSI INCITS 230-1994 (FC-PH), Annex A, Subclause A.4.2	M	Yes [ ]
OR14	Total jitter measurement conditions at TP2	38.6.8	Using BERT	M	Yes [ ]
OR15	Total jitter measurement conditions at TP2	38.6.8	Using Bessel-Thomson filter defined in 38.6.5	M	Yes [ ]
OR16	Total jitter measurement conditions	38.6.8	Using mixed frequency pattern specified in 36A.3	M	Yes [ ]
OR17	Total jitter measurement conditions at TP4	38.6.8	Using conformance test signal at TP3 (see 38.6.11)	M	Yes [ ]
OR18	Optical power used for total jitter measurement at TP4	38.6.8	0.5 dB greater than stressed receive sensitivity given in Table 38–4 (for SX) or (for LX)	M	Yes [ ]
OR19	Optical power used for total jitter measurement at TP4	38.6.8	Corrected for extinction ratio	M	Yes [ ]
OR20	Total jitter measurement conditions at TP4	38.6.8	Measured without Bessel-Thomson filters	M	Yes [ ]
OR21	Coupled power ratio	38.6.10	Measured using TIA/EIA-526-14A [B12], meets values in Table 38–3 (for SX) or (for LX)	M	Yes [ ]
OR22	Compliance test signal at TP3	38.6.11	Meets requirements of Figure 38–4	M	Yes [ ]
OR23	Compliance test signal at TP3	38.6.11	Pattern specified in 36A.5	M	Yes [ ]
OR24	Compliance test signal at TP3	38.6.11	DJ eye closure no less than 65 ps	M	Yes [ ]

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38.12.4.5 Optical measurement requirements *(continued)*

Item	Feature	Subclause	Value/Comment	Status	Support
OR25	Compliance test signal at TP3	38.6.11	Vertical eye-closure penalty meets requirements of Table 38–4	SX:M	Yes [ ] N/A [ ]
OR26	Compliance test signal at TP3	38.6.11	Vertical eye-closure penalty meets requirements of Table 38–8	LX:M	Yes [ ] N/A [ ]
OR27	Compliance test signal at TP3	38.6.11	Bandwidth of photodetector >2.5 GHz, and couple through 4th order Bessel-Thomson filter	M	Yes [ ]
OR28	Receiver electrical cutoff frequency measurement procedure	38.6.12	As described in 38.6.12	M	Yes [ ]
OR29	Optical source used for cutoff frequency measurement	38.6.12	With the exception of extinction ratio, meets requirements of Clause 38	M	Yes [ ]
OR30	General safety	38.7.1	Conforms to J.2	M	Yes [ ]
OR31	Laser safety compliance	38.7.2	Hazard Level 1	M	Yes [ ]
OR32	Laser safety compliance test conditions	38.7.2	IEC 60825-1 and IEC 60825-2	M	Yes [ ]
OR33	Documentation explicitly defines requirements and usage restrictions on the host system necessary to meet after certifications	38.7.2		M	Yes [ ]
OR34	Sound installation practices	38.7.3		INS:M	Yes [ ] N/A [ ]
OR35	Compliance with all requirements over the life of the product	38.8		M	Yes [ ]
OR36	Compliance with applicable local and national codes for the limitation of electromagnetic interference	38.8.1		M	Yes [ ]

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38.12.4.6 Characteristics of the fiber optic cabling

Item	Feature	Subclause	Value/Comment	Status	Support
LI1	Fiber optic cabling	38.11	Meets specifications in Table 38–11	INS:M	Yes [ ] N/A [ ]
LI2	Return loss for multimode connections	38.11.2.2	> 20 dB	INS:M	Yes [ ] N/A [ ]
LI3	Return loss for single-mode connections	38.11.2.2	> 26 dB	INS:M	Yes [ ] N/A [ ]
LI4	MDI optical plug	38.11.3	Duplex SC meeting IEC 61754-4, IEC 61754-4:1997 [B33] Interface 4-2, and ISO/IEC 11801, maintains polarity and ensures orientation.	INS:M	Yes [ ]
LI5	MDI optical receptacle	38.11.3	Duplex SC meeting IEC 61754-4:1997 [B33] Interface 4-2, and ISO/IEC 11801, maintains polarity and ensures orientation.	M	Yes [ ]
LI6	Offset-launch mode-conditioning patch cord	38.11.4	Meet conditions of Table 38–13	OFP:M	Yes [ ] N/A [ ]
LI7	Single-mode ferrules in offset-launch mode-conditioning patch cords	38.11.4	IEC 61754-4:1997 [B33] grade 1 ferrule	OFP:M	Yes [ ] N/A [ ]
LI8	Single-mode fiber in offset-launch mode-conditioning patch cords	38.11.4	Per 38.11.1	OFP:M	Yes [ ] N/A [ ]
LI9	Multimode fiber in offset-launch mode-conditioning patch cords	38.11.4	Same type as used in LX cable plant	OFP:M	Yes [ ] N/A [ ]
LI10	Label on single-mode end of offset-launch mode-conditioning patch cords	38.11.4	Labeled “To Equipment”	OFP:M	Yes [ ] N/A [ ]
LI11	Label on multimode end of offset-launch mode-conditioning patch cords	38.11.4	Labeled “To Cable”	OFP:M	Yes [ ] N/A [ ]
LI12	Color identifier of single-mode fiber connector	38.11.4	Blue	OFP:M	Yes [ ] N/A [ ]
LI13	Color identifier of multimode fiber connector	38.11.4	Beige	OFP:M	Yes [ ] N/A [ ]

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39. Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-CX (short-haul copper)

39.1 Overview

This clause specifies the 1000BASE-CX PMD (including MDI) and baseband medium for short-haul copper. In order to form a complete 1000BASE-CX Physical Layer it shall be integrated with the 1000BASE-X PCS of Clause 36 and the PMD of Clause 38, which are hereby incorporated by reference. As such, the 1000BASE-CX PMD shall comply with the PMD service interface specified in 38.1.1.

1000BASE-CX has a minimum operating range of 0.1 to 25 m. Jumper cables, described in 39.4, are used to interconnect 1000BASE-CX PMDs. These cables shall not be concatenated to achieve longer distances. A 1000BASE-CX jumper cable assembly consists of a continuous shielded balanced cable terminated at each end with a polarized shielded plug described in 39.5.1. The jumper cable assembly provides an output signal on contacts R+/R– meeting the requirements shown in Figure 39–5 when a transmit signal compliant with Figures 39–3 and 39–4 is connected to the T+/T– contacts at the near-end MDI connector.

The links described in this clause are applied only to homogenous ground applications such as between devices within a cabinet or rack, or between cabinets interconnected by a common ground return or ground plane. This restriction minimizes safety and interference concerns caused by any voltage differences that could otherwise exist between equipment grounds.

39.2 Functional specifications

The 1000BASE-CX PMD performs three functions, Transmit, Receive, and Signal Status according to the service interface definition in 38.1.

39.2.1 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according electrical specifications in 39.3.1. The higher output voltage of T+ minus T– (differential voltage) shall correspond to tx_bit = ONE.

39.2.2 PMD receive function

The PMD Receive function shall convey the bits received at the MDI in accordance with the electrical specifications of 39.3.2 to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). The higher output voltage of R+ minus R– (differential voltage) shall correspond to rx_bit = ONE.

39.2.3 PMD signal detect function

The PMD Signal Detect function shall report to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indication is intended to be an indicator of electrical signal presence.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 39–1. The PMD receiver is not required to verify whether a compliant 1000BASE-X signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

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Table 39–1—SIGNAL_DETECT value definition

Receive Conditions	Signal Detect Value
V_{input}, Receiver < (receiver sensitivity + worst-case local system noise)[a]	FAIL
Minimum differential sensitivity ≤ $V_{input,}$ Receiver ≤ Maximum differential input AND compliant 1000BASE-X signal input	OK
All other conditions	Unspecified

[a]Worst-case local system noise includes all receiver coupled noise sources (NEXT, power supply noise, and any reflected signals). Receive sensitivity is the actual sensitivity of the specific port (as opposed to the minimum differential sensitivity).

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input signal level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD due to cross talk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations which generate the SIGNAL_DETECT parameter values in response to the amplitude of the 8B/10B modulation of the electrical signal

39.3 PMD to MDI electrical specifications

All interface specifications are valid only at the point of entry and exit from the equipment. These points are identified as points TP2 and TP3 as shown in Figure 39–1. The specifications assume that all measurements are made after a mated connector pair, relative to the source or destination.

TP1 and TP4 are standardized reference points for use by implementers to certify component conformance. The electrical specifications of the PMD service interface (TP1 and TP4) are not system compliance points (these are not readily testable in a system implementation). It is expected that in many implementations TP1 and TP4 will be common between 1000BASE-SX (Clause 38), 1000BASE-LX (Clause 38), and 1000BASE-CX.

PMD specifications shall be measured using the measurement techniques defined in 39.6.

The reference points for all connections are those points TP2 and TP3 where the cabinet Faraday shield transitions between the cabinet and the jumper cable shield. If sections of transmission line exist within the Faraday shield, they are considered to be part of the associated transmit or receive network, and not part of the jumper cable assembly.

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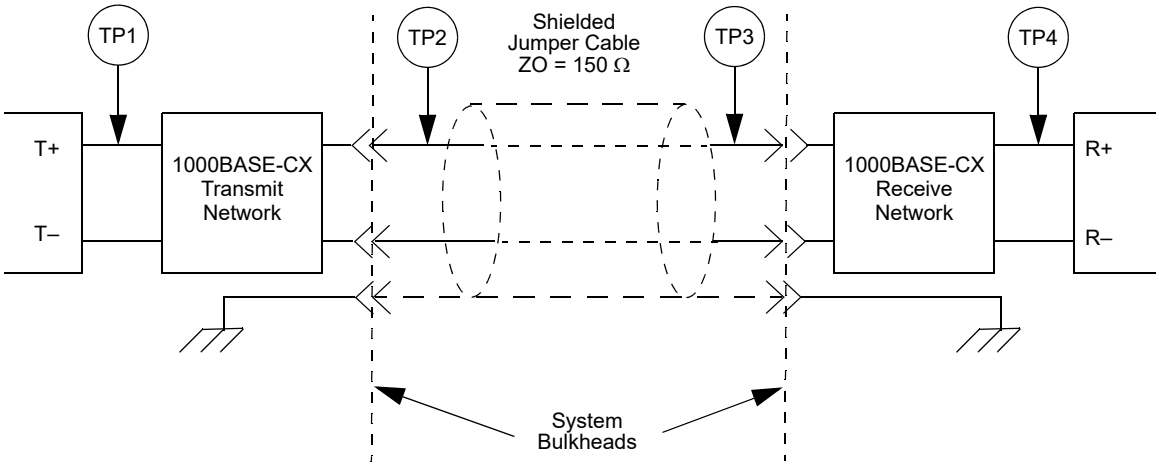

NOTE—Jumper cable assembly shielding is attached to the system chassis via the connector shroud.

Figure 39–1—1000BASE-CX link (half link is shown)

Schematics in the diagrams in this clause are for illustration only and do not represent the only feasible implementation.

39.3.1 Transmitter electrical specifications

The output driver is assumed to have output levels approximating those of Emitter Coupled Logic (ECL), as measured at TP1. The transmitter shall meet the specifications in Table 39–2.

Table 39–2—Transmitter characteristics at TP2

Description	Value	Unit
Type	(P)ECL	
Data rate	1000	Mb/s
Clock tolerance	±100	ppm
Nominal signaling speed	1250	MBd
Differential amplitude (p-p)		
Max (worst case p-p)	2000	mV
Min (opening)	1100	mV
Max (OFF)[a]	170	mV
Rise/Fall time (20-80%)		
maximum	327	ps
minimum	85	ps
Differential skew (max)	25	ps

[a]Examples of an OFF transmitter are no power supplied to the PMD and PMA transmit output being driven to a static state during loopback.

For all links, the output driver shall be AC-coupled to the jumper cable assembly through a transmission network, and have output levels, measured at the input to the jumper cable assembly (TP2), meeting the eye diagram requirements of Figure 39–3 and Figure 39–4, when terminated as shown in Figure 39–2. The symbols X1 and X2 in Figure 39–3 and Figure 39–4 are defined in Table 39–3.

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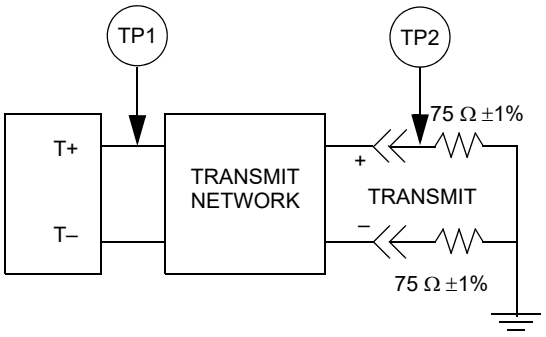

Figure 39–2—Balanced transmitter test load

The normalized amplitude limits in Figure 39–3 are set to allow signal overshoot of 10% and undershoot of 20%, relative to the amplitudes determined to be a logic 1 and 0. The absolute transmitter output timing and amplitude requirements are specified in Table 39–2, Table 39–3, and Figure 39–4. The normalized transmitter output timing and amplitude requirements are specified in Table 39–2, Table 39–3, and Figure 39–3. The transmit masks of Figure 39–3 and Figure 39–4 are not used for response time and jitter specifications.

NOTE 1—The relationship between Figure 39–3 and Figure 39–4 can best be explained by a counter example. If a transmitter outputs a nominal 600 mV-ppd logic one level with overshoot to 900 mV-ppd, it will pass the absolute mask of Figure 39–4 but will not pass the normalized mask of Figure 39–3. Normalized, this signal would have 50% overshoot. This exceeds the 10% overshoot limit defined by the normalized eye mask.

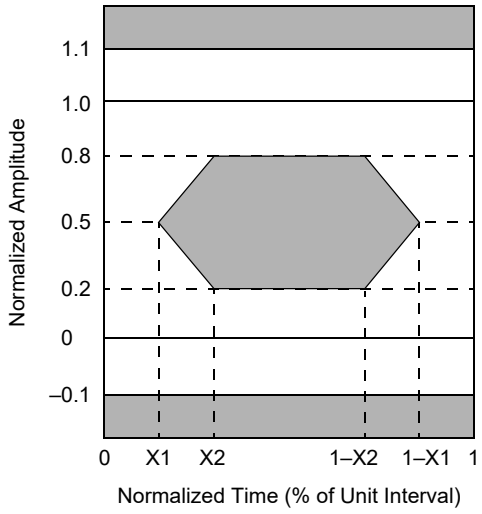

Figure 39–3—Normalized eye diagram mask at TP2

Table 39–3—Normalized time intervals for TP2

Symbol	Value	Units
X1	0.14	Unit Intervals (UI)
X2	0.34	Unit Intervals (UI)

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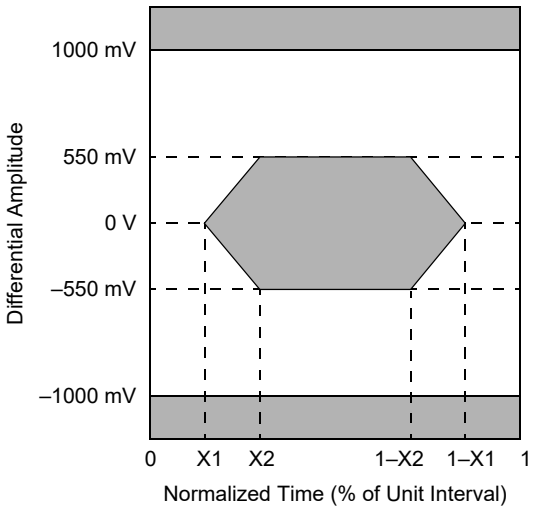

Figure 39–4—Absolute eye diagram mask at TP2

The recommended interface to electrical transmission media is via transformer or capacitive coupling.

NOTE 2—All specifications, unless specifically listed otherwise, are based on differential measurements.

NOTE 3—All times indicated for TDR measurements are recorded times. Recorded times are twice the transit time of the TDR signal.

NOTE 4—The transmit differential skew is the maximum allowed time difference (on both low-to-high and high-to low transitions) as measured at TP2, between the true and complement signals. This time difference is measured at the midway point on the signal swing of the true and complement signals. These are single-ended measurements.

NOTE 5—The transmitter amplitude maximum specification identifies the maximum p-p signal that can be delivered into a resistive load matching that shown in Figure 39–2.

NOTE 6—The transmitter amplitude minimum specification identifies the minimum allowed p-p eye amplitude opening that can be delivered into a resistive load matching that shown in Figure 39–2.

NOTE 7—The normalized 1 is that amplitude determined to be the average amplitude when driving a logic 1. The normalized 0 is that amplitude determined to be the average amplitude when driving a logic 0.

NOTE 8—Eye diagram assumes the presence of only high-frequency jitter components that are not tracked by the clock recovery circuit. For this standard the lower cutoff frequency for jitter is 637 kHz.

39.3.2 Receiver electrical specifications

The receiver shall be AC-coupled to the media through a receive network located between TP3 and TP4 as shown in Figure 39–1. The receiver shall meet the signal requirements listed in Table 39–4.

The minimum input amplitude to the receiver listed in Table 39–4 and Figure 39–5 is a worst case specification across all environmental conditions. Restricted environments may allow operation at lower minimum differential voltages, allowing significantly longer operating distances.

NOTE 1—All specifications, unless specifically listed otherwise, are based on differential measurements.

NOTE 2—The receiver minimum differential sensitivity identifies the minimum p-p eye amplitude at TP3 to meet the BER objective.

NOTE 3—Eye diagrams assume the presence of only high-frequency jitter components that are not tracked by the clock recovery circuit. For this standard the lower cutoff frequency for jitter is 637 kHz.

NOTE 4—All times indicated for TDR measurements are recorded times. Recorded times are twice the transit time of the TDR signal.

NOTE 5—Through_Connection impedance describes the impedance tolerance through a mated connector. This tolerance is greater than the termination or cable impedance due to limits in the technology of the connectors.

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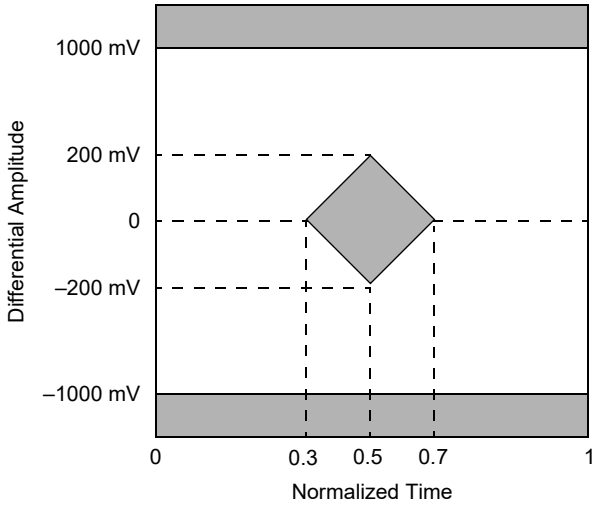

Figure 39–5—Eye diagram mask at point-TP3

Table 39–4—Receiver characteristics (TP3)

Description	Value	Units
Data rate	1000	Mb/s
Nominal signaling speed	1250	MBd
Tolerance	±100	ppm
Minimum differential sensitivity (peak-peak)	400	mV
Maximum differential input (peak-peak)	2000	mV
Input Impedance @ TP3		
TDR Rise Time	85	ps
Exception_window[a]	700	ps
Through_connection	150 ± 30	Ω
At Termination[b]	150 ± 10	Ω
Differential Skew	175	ps

[a]Within the Exception_window no single impedance excursion shall exceed the Through_Connection-impedance tolerance for a period of twice the TDR rise time specification.

[b]The input impedance at TP3, for the termination, shall be recorded 4.0 ns following the reference location determined by an open connector between TP3 and TP4.

39.3.3 Jitter specifications for 1000BASE-CX

The 1000BASE-CX PMD shall meet the total jitter specifications defined in Table 38–10. Normative values are highlighted **in bold.** All other values are optional. Compliance points are defined in 39.3.

Jitter shall be measured as defined in 38.6.8 with the exception that no measurement will require the use of an optical to electrical converter (O/E).

Deterministic jitter budgetary specifications are included here to assist implementers in specifying components. Measurements for DJ are described in 38.6.9 with the exception that no measurement will require the use of an O/E.

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Table 39–5—1000BASE-CX jitter budget

Compliance point	Total jitter[a]		Deterministic jitter	
	UI	ps	UI	ps
TP1	**0.240**	**192**	0.120	96
TP1 to TP2	0.090	72	0.020	16
TP2	**0.279**	**223**	0.140	112
TP2 to TP3	0.480	384	0.260	208
TP3	**0.660**	**528**	0.400	320
TP3 to TP4	0.050	40	0.050	40
TP4	**0.710**	**568**	0.450	360

[a]Total jitter is composed of both deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter at that point.

39.4 Jumper cable assembly characteristics

A 1000BASE-CX compliant jumper cable assembly shall consist of a continuous shielded balanced cable terminated at each end with a polarized shielded plug as described in 39.5.1. The jumper cable assembly shall provide an output signal on contacts R+/R– meeting the requirements shown in Figure 39–5 when a transmit signal compliant with Figures 39–3 and 39–4 is connected to the T+/T– contacts at the near-end MDI connector. This jumper cable assembly shall have electrical and performance characteristics as described in Table 39–6. Jumper cable assembly specifications shall be measured using the measurement techniques defined in 39.6. The jumper cable assembly may have integrated compensation networks.

NOTE 1—Jumper cable assemblies that meet the requirements for ANSI INCITS 230-1994 (FC-PH) may not meet the requirements of this clause.

NOTE 2—Through_Connection impedance describes the impedance tolerance through a mated connector. This tolerance is greater than the termination or cable impedance due to limits in the technology of the connectors.

To produce jumper cable assemblies capable of delivering signals compliant with the requirements of 39.4, the assemblies should generally have characteristics equal to or better than those in Table 39–7.

39.4.1 Compensation networks

A jumper cable assembly may include an equalizer network to meet the specifications and signal quality requirements (e.g., receiver eye mask at TP3) of this clause. The equalizer shall need no adjustment. All jumper cable assemblies containing such circuits shall be marked with information identifying the specific designed operational characteristics of the jumper cable assembly.

39.4.2 Shielding

The jumper cable assembly shall provide class 2 or better shielding in accordance with IEC 61196-1.

39.5 MDI specification

This clause defines the Media Dependent Interface (MDI). The 1000BASE-CX PMD of 39.3 is coupled to the jumper cable assembly by the media dependent interface (MDI).

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Table 39–6—Jumper cable assembly characteristics (normative)

Description	Value	Unit
Differential skew (max)	150	ps
Link Impedance @ TP2/TP3[a] Through_connection Cable	 150 ± 30 150 ± 10	 W W
TDR rise time Exception_window[b]	85 700	ps ps
Round-trip delay (max)[c]	253 253	bit times ns

[a]The link impedance measurement identifies the impedance mismatches present in the jumper cable assembly when terminated in its characteristic impedance. This measurement includes mated connectors at both ends of the Jumper cable assembly (points TP2 and TP3). The link impedance for the jumper cable assembly, shall be recorded 4.0 ns following the reference location determined by an open connector at TP2 and TP3.

[b]Within the Exception_window no single impedance excursion shall exceed the Through_Connection-impedance tolerance for a period of twice the TDR rise time specification. The Exception_window (used with specific impedance measurements) identifies the maximum time period during which the measured impedance is allowed to exceed the listed impedance tolerance. The maximum excursion within the Exception_window at TP3 shall not exceed ±33% of the nominal cable impedance.

[c]Used in Clause 42. This delay is a budgetary requirement of the upper layers. It is easily met by the jumper cable delay characteristics in this clause.

Table 39–7—Jumper cable assembly characteristics (recommended)

Description	Value	Unit
Attenuation (max.) at 625 MHz	8.8	dB
Minimum NEXT loss @ 85 ps Tr (max)	6 24.5	% dB

39.5.1 MDI connectors

Connectors meeting the requirements of 39.5.1.1 (Style-1) and 39.5.1.2 (Style-2) shall be used as the mechanical interface between the PMD of 39.3 and the jumper cable assembly of 39.4. The plug connector shall be used on the jumper cable assembly and the receptacle on the PHY. Style-1 or style-2 connectors may be used as the MDI interface. To limit possible cross-plugging with non-1000BASE-CX interfaces that make use of the Style-1 connector, it is recommended that the Style-2 connector be used as the MDI connector.

39.5.1.1 Style-1 connector specification

The style-1 balanced connector for balanced jumper cable assemblies shall be the 9-pin shielded D-subminiature connector, with the mechanical mating interface defined by IEC 60807-3, having pinouts matching those in Figure 39–6, and the signal quality and electrical requirements of this clause. The style-1 connector pin assignments are shown in Figure 39–6 and Table 39–8.

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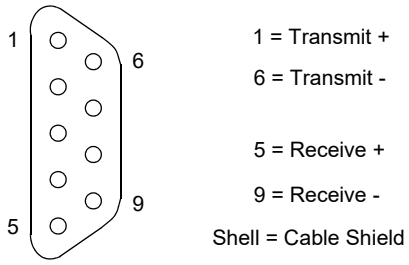

Figure 39–6—Style-1 balanced connector receptacle pin assignments

39.5.1.2 Style-2 connector specification

The style-2 balanced cable connector is the 8-pin shielded ANSI Fibre Channel style-2 connector with the mechanical mating interface defined by IEC 61076-3-103, having pinouts matching those shown in Figure 39–7, and conforming to the signal quality and electrical requirements of this clause.

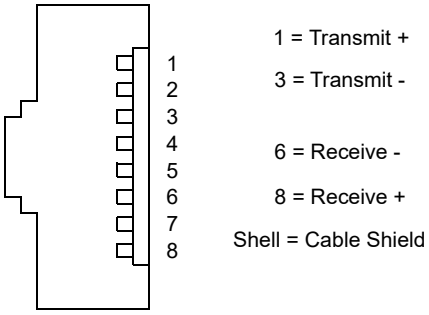

Figure 39–7—Style-2 balanced connector receptacle pin assignments

The style-1 or style-2 connector may be populated with optional contacts to support additional functions. The presence of such contacts in the connector assemblies does not imply support for these additional functions.

NOTE 1—Style-1 pins 2 and 8 (Style-2 pins 7 and 2) are reserved for applications that assign these pins to power and ground.

NOTE 2—Style-1 pin 3 (Style-2 pin 4) is reserved for applications that assign this pin to a Fault Detect function.

NOTE 3—Style-1 pin 7 (Style-2 pin 5) is reserved for applications that assign this pin to an Output Disable function.

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Table 39–8—MDI contact assignments

Contact		PMD MDI signal
Style-1	Style-2	
1	1	Transmit +
2	7	Reserved
3	4	Reserved
4		Mechanical key
5	8	Receive +
6	3	Transmit –
7	5	Reserved
8	2	Reserved
9	6	Receive –

39.5.1.3 Style-2 connector example drawing

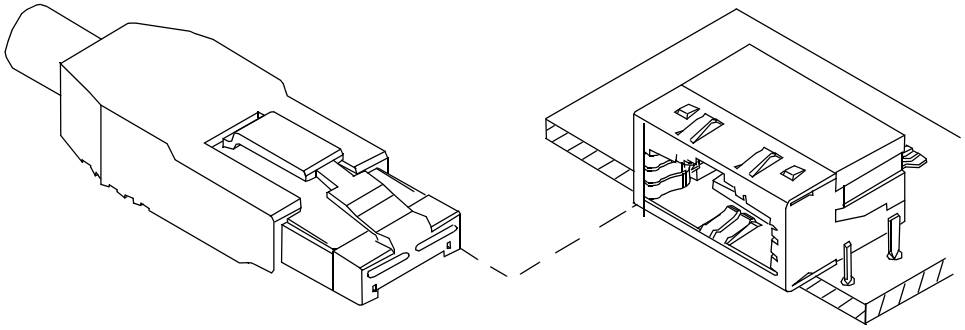

Figure 39–8—Style-2 connector, example drawing

39.5.2 Crossover function

The default jumper cable assembly shall be wired in a crossover fashion as shown in Figure 39–9, with each pair being attached to the transmitter contacts at one end and the receiver contacts at the other end.

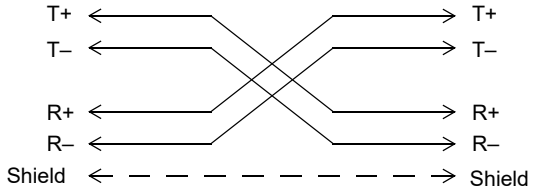

Figure 39–9—Balanced cable wiring

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39.6 Electrical measurement requirements

Electrical measurements shall be performed as described in this subclause.

39.6.1 Transmit rise/fall time

Rise time is a differential measurement across the T+ and T– outputs with a load present (including test equipment) equivalent to that shown in Figure 39–2. Both rising and falling edges are measured. The 100% and 0% levels are the normalized 1 and 0 levels present when sending an alternating K28.5 character stream.

Once the normalized amplitude is determined, the data pattern is changed to a continuous D21.5 character stream. The rise time specification is the time interval between the normalized 20% and 80% amplitude levels.

39.6.2 Transmit skew measurement

The transmitter skew is the time difference between the T+ and T– outputs measured at the normalized 50% crossover point with a load present (including test equipment) equivalent to that shown in Figure 39–2. This measurement is taken using two single ended probes. Skew in the test set-up has to be calibrated out.

Normalized amplitudes can be determined using the method described in 39.6.1.

A continuous D21.5 or K28.7 data pattern is transmitted by the device under test. The data is averaged using an averaging scope. An easy method to view and measure the skew between these signals is to invert one.

39.6.3 Transmit eye (normalized and absolute)

This test is made as a differential measurement at the bulkhead connector. The scope trigger has to either be a recovered clock as defined in 38.6.8 or a character clock internal to the equipment. The data pattern for this is the alternating K28.5.

If a character trigger is used, the overshoot/undershoot percentages have to be measured at all ten bit positions. The load for this test is that shown in Figure 39–2.

39.6.4 Through_connection impedance

This is a differential TDR or equivalent measurement that has to be made through a mated connector pair or pairs. Any lead-in trace or cable to the connector that is part of the test fixture should provide a reasonable impedance match so as to not effect the actual measurement. All TDR measurements have to be filtered to the TDR rise time specification. Any test fixture used with these TDR tests has to be calibrated to remove the effects of the test fixture, and verified to produce accurate results.

The impedance Through_connection interval starts at the first point where the measured impedance exceeds the limits for the termination and ends at the point that the impedance returns to within the termination impedance limits and remains there.

Within this Through_connection interval, an Exception_window exists where the impedance is allowed to exceed the Through_connection impedance limits up to a maximum deviation of ±33% of the nominal link impedance. The Exception_window begins at the point where the measured impedance first exceeds the impedance tolerance limits for Through_connection.

39.6.5 Jumper cable intra-pair differential skew

The jumper cable intra-pair differential skew measurement is conducted to determine the skew, or difference in velocity, of each wire in a cable pair when driven with a differential source. This measurement requires two

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mated connectors, one at the signal source and one at the opposite end of the cable. A pair of matched, complimentary signals (S+, S–) are driven into the T+ and T– contacts of the connector. These signals are time conditioned to start at the same point. This test shall be performed at both ends of the jumper cable assembly.

The jumper cable intra-pair skew is the time difference between the R+ and R– outputs of the excited pair within the jumper cable assembly measured at the normalized 50% crossover point with a load present (including test equipment) equivalent to that shown in Figure 39–2. This measurement is taken using two single ended probes. Skew in the test set-up has to be calibrated out.

Normalized amplitudes can be determined using the method described in 39.6.1.

A continuous square wave is used for S+, S–. The data is averaged using an averaging scope. An easy method to view and measure the skew between these signals is to invert one. A differential TDR can provide a convenient method to time condition the input signals.

39.6.6 Receiver link signal

This differential measurement is made at the end of the jumper cable assembly, through mated connectors with a load present (including test equipment) equivalent to that shown in Figure 39–2. The signal is measured with an alternating K28.5 character stream and is tested to the mask requirements of Figure 39–5.

39.6.7 Near-End Cross Talk (NEXT)

NEXT Loss tests are conducted using a differential TDR (or equivalent) filtered to the rise time limit (near-end cross talk at a maximum T_r of 85 ps) in Table 39–6. The T+ and T– inputs of the jumper cable connector are excited to create a disturber pair while the R+ and R– contacts of the disturbed pair are measured within the same connector. The far-end R+/R– outputs of the disturber pair are terminated per Figure 39–2. The R+ and R– signals of the disturbed pair are terminated with a load (including test equipment) equivalent to that shown in Figure 39–2. The T+ and T– inputs of disturbed pair shall be terminated per Figure 39–2. This test shall be performed at both ends of the jumper cable assembly.

39.6.8 Differential time-domain reflectometry (TDR) measurement procedure

The differential TDR test setup measures the reflected waveform returned from a load when driven with a step input. It is obtained by driving the load under test with a step waveform using a driver with a specified source impedance and rise time. The reflected waveform is the difference between (a) the observed waveform at the device under test when driven with the specified test signal, and (b) the waveform that results when driving a standard test load with the same specified test signal. From this measured result we can infer the impedance of the device under test. The derivative of a time-domain reflectometry measurement is the time-domain equivalent of S_{11} parameter testing used in carrier-based systems.

For the measurement of 1000BASE-CX jumper cables, the following test conditions apply:

a) The driving waveform is sourced from a balanced, differential 150 Ω source with an 85 ps rise time (see 39.6.8.1).
b) The test setup is calibrated (see 39.6.8.2).

39.6.8.1 Driving waveform

If the natural differential output impedance of the driving waveform is not 75 Ω, it may be adjusted to within 75 Ω ± 5 Ω by an attenuating resistive pad. When the driving point resistance is 100 Ω (as would be the case with a differential signal source having two independent, antipodal, 50 Ω sources), a good pad design is shown in Figure 39–10, where R1 = 173.2 Ω and R2 = 43.3 Ω. All resistors are surface-mount packages

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soldered directly to the test fixture with no intervening leads or traces, and the whole structure is mounted on a solid ground plane (used in three places).

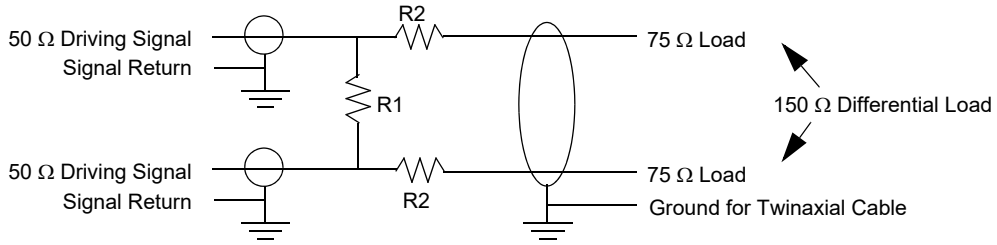

Figure 39–10—Differential TDR pad adapter

If the natural rise time of the driver is less than 85 ps, the resulting measured time-waveforms have to be filtered to reduce the apparent rise time to 85 ps ± 10 ps.

39.6.8.2 Calibration of the test setup

Three measurements are made, with a short, and open, and a known test load. The value of the test resistance should be constant to within 1% over the frequency range dc to 6 GHz, and of known value. The value of the test resistance should be within the range 75 Ω ± 5 Ω.

The differential voltages measured across the device-under-test terminals in these three cases are called V_{short}, V_{open}, and V_{test}, respectively. From these three measurements we will compute three intermediate quantities:

$$A = (V_{open} - V_{short}) /2$$

$$B = (V_{open} + V_{short}) /2$$

$$Z_0 = Z_{test} \times (V_{open} - V_{test})/(V_{test} - V_{short})$$

The value of Z_0 is the actual driving point impedance of the tester. It has to be within 75 Ω ± 5 Ω.

For any device under test, the conversion from measured voltage $V_{measured}$ to impedance is as follows:

Measured impedance = $Z_0 \times (1 + V')/(1 - V')$

where $V' = (V_{measured} - B)/A$.

39.7 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801:1995. References to the MAU or AUI should be replaced with PHY or DTE and AUI to jumper cable assembly, as appropriate. Subclause 14.7.2.4, *Telephony voltage*, should be ignored. Should a case occur where, through a cabling error, two transmitters or receivers are directly connected, no damage shall occur to any transmitter, receiver, or other link component in the system. The link shall be able to withstand such an invalid connection without component failure or degradation for an indefinite period of time.

Systems connected with 1000BASE-CX links shall meet the bonding requirements (common ground connection) of ISO/IEC 11801:1995, subclause 9.2, for shielded cable assemblies. Cable shield(s) shall be

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earthed (chassis ground) through the bulkhead connector shell(s) on both ends of the jumper cable assembly as shown in Figure 39–1.

39.8 Protocol implementation conformance statement (PICS) proforma for Clause 39, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-CX[80]

39.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 39, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-CX, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

39.8.2 Identification

39.8.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

39.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 39, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-CX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[80] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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39.8.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*INS	Installation / cable	39.4	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
*STY1	Style-1 MDI	39.5	Either the style-1 or the style-2 MDI has to be provided	O/1	Yes [ ] No [ ]
*STY2	Style-2 MDI	39.5		O/1	Yes [ ] No [ ]
*TP1	Standardized reference point TP1 exposed and available for testing.	39.3	This point may be made available for use by implementers to certify component conformance.	O	Yes [ ] No [ ]
*TP4	Standardized reference point TP4 exposed and available for testing.	39.3	This point may be made available for use by implementers to certify component conformance.	O	Yes [ ] No [ ]

39.8.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-CX (short-haul copper)

39.8.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FN1	Integration with 1000BASE-X PCS and PMA	39.1		M	Yes [ ]
FN2	Complies with PMD service interface of 38.2	39.1		M	Yes [ ]
FN3	Jumper cables not concatenated	39.1		INS:M	Yes [ ] N/A [ ]
FN5	Transmit function	39.2.1	Convey bits requested by PMD_UNITDATA.request() to the MDI	M	Yes [ ]
FN6	Transmitter logical to electrical mapping	39.2.1;	Logical one equates to electrical high	M	Yes [ ]
FN7	Receive function	39.2.2	Convey bits received from the MDI to PMD_UNITDATA.indication()	M	Yes [ ]
FN8	Receiver logical to electrical mapping	39.2.2	Logical one equates to electrical high.	M	Yes [ ]
FN9	Signal detect function	39.2.3	Report to the PMD service interface the message PMD_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
FN10	Signal detect behavior	39.2.3	Meets requirements of Table 39–1	M	Yes [ ]

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39.8.4.2 PMD to MDI electrical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PM1	Measurement requirements	39.3	Electrical measurements are made according to the tests specified in 39.6.	M	Yes [ ]
PM2	Transmitter characteristics	39.3.1	Transmitters meets requirements of Table 39–2	M	Yes [ ]
PM3	Transmitter coupling	39.3.1	AC-coupled	M	Yes [ ]
PM4	Transmitter eye diagram	39.3.1	Meets requirements of Figure 39–3 and Figure 39–4 when terminated as shown in Figure 39–2	M	Yes [ ]
PM5	Receiver coupling	39.3.2	AC-coupled	M	Yes [ ]
PM6	Receiver characteristics	39.3.2	Meet requirements of Table 39–4	M	Yes [ ]
PM7	Measurement conditions for input impedance at TP3	39.3.2	4 ns following reference location	M	Yes [ ]
PM8	Total jitter specification at TP1	39.3.3	Meets specification of bold entries in Table 38–10	TP1:M	Yes [ ] N/A [ ]
PM9	Total jitter specification at TP2	39.3.3	Meets specification of bold entries in Table 38–10	M	Yes [ ]
PM10	Total jitter specification at TP3	39.3.3	Meets specification of bold entries in Table 38–10	INS:M	Yes [ ] N/A [ ]
PM11	Total jitter specification at TP4	39.3.3	Meets specification of bold entries in Table 38–10	TP4:M	Yes [ ] N/A [ ]
PM12	Measurement conditions for jitter	39.3.3	Per 38.6.8 (with exceptions)	M	Yes [ ]

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39.8.4.3 Jumper cable assembly characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
LI1	Two polarized, shielded plug per 39.5.1 and shielded with electrical characteristics per Table 39–6	39.4	As defined in Table 39–6	INS:M	Yes [ ]
LI2	Delivers compliant signal when driven with worst case source signal	39.4	Transmit signal compliant with Figures 39–3 and 39–4, receive signal complaint with Figure 39–5, into a load compliant with Figure 39–2	INS:M	Yes [ ]
LI3	Measurement requirements	39.4	Electrical measurements are made according to the tests specified in 39.6	INS:M	Yes [ ]
LI4	Maximum excursion during Exception_window of cable impedance measurement	39.4	± 33% of nominal cable impedance	INS:M	Yes [ ]
LI5	Measurement conditions for link impedance	39.4	4 ns following the reference location between TP3 and TP4	INS:M	Yes [ ]
LI6	Equalizer needs no adjustment	39.4.1		INS:M	Yes [ ] N/A [ ]
LI7	Cables containing equalizers shall be marked	39.4.1		INS:M	Yes [ ] N/A [ ]
LI8	Cable shielding	39.4.2	Class 2 or better per IEC 61196-1	INS:M	Yes [ ]

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39.8.4.4 Other requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OR1	Style-1 connector	39.5.1.1	9-pin shielded D-subminiature with the mechanical mating interface defined by IEC 60807-3.	STY1:M	Yes [ ] N/A [ ]
OR2	Style-2 connector	39.5.1.2	8-pin ANSI Fibre Channel style-2 connector with mechanical mating interface defined by IEC 61076-3-103.	STY2:M	Yes [ ] N/A [ ]
OR3	Default cable assembly wired in a crossover assembly	39.5.2		INS:M	Yes [ ]
OR4	Transmit rise/fall time measurement	39.6.1	Meet requirements of Table 39–2 with load equivalent to Figure 39–2	M	Yes [ ]
OR5	Transmit skew measurement	39.6.2	Meet requirements of Table 39–2 with load equivalent to Figure 39–2	M	Yes [ ]
OR6	Transmit eye measurement	39.6.3	Meet requirements of Figure 39–3 and Figure 39–4 with load equivalent to Figure 39–2	M	Yes [ ]
OR7	Through_connection impedance measurement	39.6.4	Meet requirements of Table 39–4 with load equivalent to Figure 39–2	M	Yes [ ]
OR8	Jumper cable assembly differential skew measurement	39.6.5	Meet requirements of Table 39–6 with load equivalent to Figure 39–2	M	Yes [ ]
OR9	Receiver link signal	39.6.6	Meet requirements of Figure 39–5 with load equivalent to Figure 39–2	M	Yes [ ]
OR10	NEXT Loss measurement	39.6.7	Meet requirements of Table 39–6 with load equivalent to Figure 39–2	M	Yes [ ]
OR11	Conformance to 14.7 and applicable sections of ISO/IEC 11801:1995.	39.7		M	Yes [ ]
OR12	Cabling errors shall cause no damage to transmitter, receiver, or other link components	39.7		M	Yes [ ]
OR13	Withstand invalid connection for indefinite period	39.7		M	Yes [ ]
OR14	System meets common ground requirements of ISO/IEC 11801	39.7	Per ISO/IEC 11801, subclause 9.2	INS:M	Yes [ ]
OR15	Cable shields earthed on both ends of cable	39.7		INS:M	Yes [ ]

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40. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 1000BASE-T

40.1 Overview

The 1000BASE-T PHY is one of the Gigabit Ethernet family of high-speed CSMA/CD network specifications. The 1000BASE-T Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) and baseband medium specifications are intended for users who want 1000 Mb/s performance over Category 5 balanced twisted-pair cabling systems. 1000BASE-T signaling requires four pairs of balanced cabling, as specified in ISO/IEC 11801:1995 (Class D) and ANSI/EIA/TIA-568-A-1995 (Category 5), and tested for the additional performance parameters specified in ANSI/EIA/TIA-568-B1 Annex D.

NOTE—ISO/IEC 11801:2002 provides a specification (Class D) for media that exceeds the minimum requirements of this standard.

This clause defines the type 1000BASE-T PCS, type 1000BASE-T PMA sublayer, and type 1000BASE-T Medium Dependent Interface (MDI). Together, the PCS and the PMA sublayer comprise a 1000BASE-T Physical Layer device (PHY). Provided in this document are fully functional, electrical, and mechanical specifications for the type 1000BASE-T PCS, PMA, and MDI. This clause also specifies the baseband medium used with 1000BASE-T.

40.1.1 Objectives

The following are the objectives of 1000BASE-T:

a) Support the CSMA/CD MAC
b) Comply with the specifications for the GMII (Clause 35)
c) Support the 1000 Mb/s repeater (Clause 41)
d) Provide line transmission that supports full and half duplex operation
e) Meet or exceed FCC Class A/CISPR or better operation
f) Support operation over 100 meters of copper balanced cabling as defined in 40.7
g) Bit Error Ratio of less than or equal to 10^{-10}
h) Support Auto-Negotiation (Clause 28)

40.1.2 Relationship of 1000BASE-T to other standards

Relations between the 1000BASE-T PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 CSMA/CD LAN Model are shown in Figure 40–1. The PHY sublayers (shown shaded) in Figure 40–1 connect one Clause 4 Media Access Control (MAC) layer to the medium.

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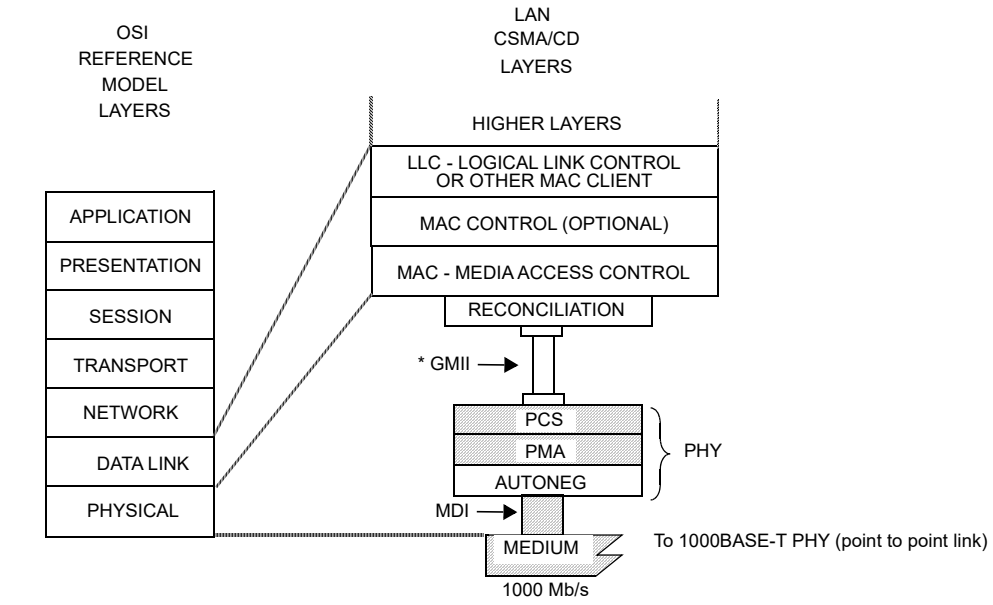

Figure 40–1—Type 1000BASE-T PHY relationship to the ISO Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model

40.1.3 Operation of 1000BASE-T

The 1000BASE-T PHY employs full duplex baseband transmission over four pairs of Category 5 balanced cabling. The aggregate data rate of 1000 Mb/s is achieved by transmission at a data rate of 250 Mb/s over each wire pair, as shown in Figure 40–2. The use of hybrids and cancellers enables full duplex transmission by allowing symbols to be transmitted and received on the same wire pairs at the same time. Baseband signaling with a modulation rate of 125 MBd is used on each of the wire pairs. The transmitted symbols are selected from a four-dimensional 5-level symbol constellation. Each four-dimensional symbol can be viewed as a 4-tuple (A_n, B_n, C_n, D_n) of one-dimensional quinary symbols taken from the set {2, 1, 0, –1, –2}. 1000BASE-T uses a continuous signaling system; in the absence of data, Idle symbols are transmitted. Idle mode is a subset of code-groups in that each symbol is restricted to the set {2, 0, –2}to improve synchronization. Five-level Pulse Amplitude Modulation (PAM5) is employed for transmission over each wire pair. The modulation rate of 125 MBd matches the GMII clock rate of 125 MHz and results in a symbol period of 8 ns.

A 1000BASE-T PHY can be configured either as a MASTER PHY or as a SLAVE PHY. The MASTER-SLAVE relationship between two stations sharing a link segment is established during Auto-Negotiation (see Clause 28, 40.5, and Annex 28C). The MASTER PHY uses a local clock to determine the timing of transmitter operations. The SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in Figure 40–3. In

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a multiport to single-port connection, the multiport device is typically set to be MASTER and the single-port device is set to be SLAVE.

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

The PCS and PMA subclauses of this document are summarized in 40.1.3.1 and 40.1.3.2. Figure 40–3 shows the functional block diagram.

A 1000BASE-T PHY with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization. The “Assert LPI” request at the GMII is encoded in the transmitted symbols. Detection of LPI signaling in the received symbols is indicated as “Assert LPI” at the GMII. When LPI signaling is simultaneously transmitted and received, an energy-efficient 1000BASE-T PHY ceases transmission and deactivates transmit and receive functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g., timing recovery, adaptive filter coefficients) and thereby track long-term variation in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal interframe is asserted at the GMII, the PHY reactivates transmit and receive functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the LPI mode.

The conditions for supporting the optional EEE capability are defined in 78.3.

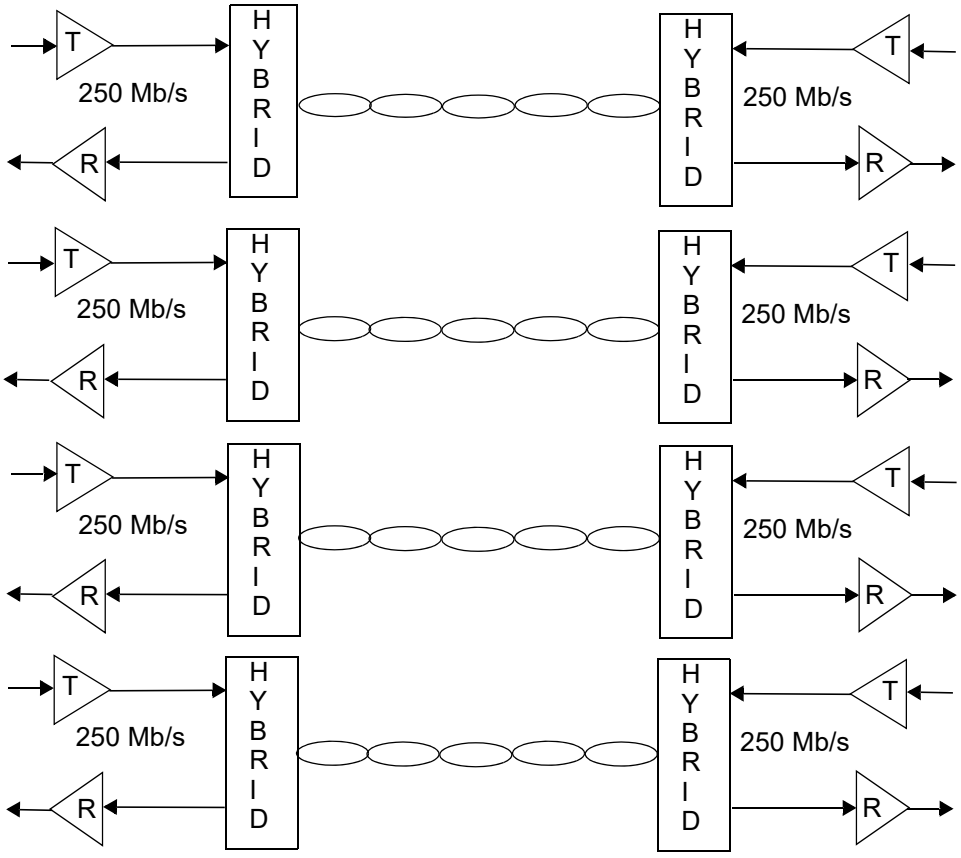

Figure 40–2—1000BASE-T topology

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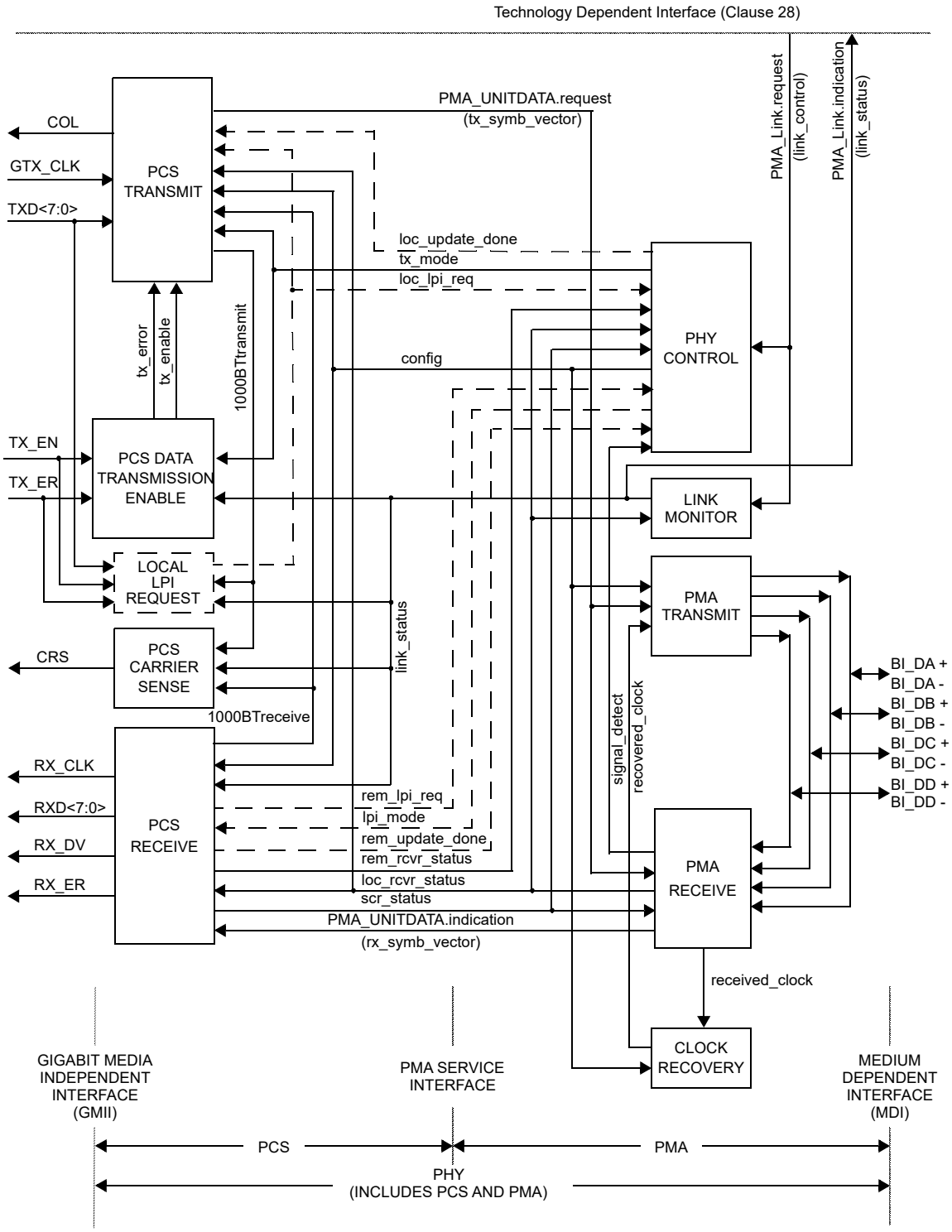

NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing

NOTE—Signals and functions shown with dashed lines are only required for the EEE capability.

Figure 40–3—Functional block diagram

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40.1.3.1 Physical Coding Sublayer (PCS)

The 1000BASE-T PCS couples a Gigabit Media Independent Interface (GMII), as described in Clause 35, to a Physical Medium Attachment (PMA) sublayer.

The functions performed by the PCS comprise the generation of continuous code-groups to be transmitted over four channels and the processing of code-groups received from the remote PHY. The process of converting data bits to code-groups is called 4D-PAM5, which refers to the four-dimensional 5-level Pulse Amplitude Modulation coding technique used. Through this coding scheme, eight bits are converted to one transmission of four quinary symbols.

During the beginning of a frame's transmission, when TX_EN is asserted from the GMII, two code-groups representing the Start-of-Stream delimiter are transmitted followed by code-groups representing the octets coming from the GMII. Immediately following the data octets, the GMII sets TX_EN=FALSE, upon which the end of a frame is transmitted. The end of a frame consists of two convolutional state reset symbol periods and two End-of-Stream delimiter symbol periods. This is followed by an optional series of carrier extend symbol periods and, possibly, the start of a new frame during frame bursting. Otherwise, the end of a frame is followed by a series of symbols encoded in the idle mode. The nature of the encoding that follows the end of a frame is determined by the GMII signals TX_ER and TXD<7:0> as specified in Clause 35.

Between frames, a special subset of code-groups using only the symbols {2, 0, –2} is transmitted. This is called idle mode. Idle mode encoding takes into account the information of whether the local PHY is operating reliably or not (see 40.4.2.4) and allows this information to be conveyed to the remote station. During normal operation, idle mode is followed by a data mode that begins with a Start-of-Stream delimiter.

When the PHY supports the optional EEE capability, Idle mode encoding also conveys to the remote PHY information of whether the local PHY is requesting entry into the LPI mode or not. Such requests are a direct translation of "Assert LPI" at the GMII. In addition, Idle mode encoding conveys to the remote PHY whether the local PHY has completed the update of its receiver state or not, as indicated by the PMA PHY Control function.

Further patterns are used for signaling a transmit error and other control functions during transmission of a data stream.

The PCS Receive processes code-groups provided by the PMA. The PCS Receive detects the beginning and the end of frames of data and, during the reception of data, descrambles and decodes the received code-groups into octets RXD<7:0> that are passed to the GMII. The conversion of code-groups to octets uses an 8B1Q4 data decoding technique. PCS Receive also detects errors in the received sequences and signals them to the GMII. Furthermore, the PCS contains a PCS Carrier Sense function, a PCS Collision Presence function, and a management interface.

The PCS functions and state diagrams are specified in 40.3. The signals provided by the PCS at the GMII conform to the interface requirements of Clause 35. The PCS Service Interfaces to the GMII and the PMA are abstract message-passing interfaces specified in 40.2.

40.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PMA service interface onto the balanced cabling physical medium and provides the link management and PHY Control functions. The PMA provides full duplex communications at 125 MBd over four pairs of balanced cabling up to 100 m in length.

The PMA Transmit function comprises four independent transmitters to generate five-level, pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD, as described in 40.4.3.1.

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The PMA Receive function comprises four independent receivers for five-level pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD, as described in 40.4.3.2. This signal encoding technique is referred to as 4D-PAM5. The receivers are responsible for acquiring clock and providing code-groups to the PCS as defined by the PMA_UNITDATA.indication message. The PMA also contains functions for Link Monitor.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control begins following the completion of Auto-Negotiation and provides the startup functions required for successful 1000BASE-T operation. It determines whether the PHY operates in a normal state, enabling data transmission over the link segment, or whether the PHY sends special code-groups that represent the idle mode. The latter occurs when either one or both of the PHYs that share a link segment are not operating reliably.

When the PHY supports the optional EEE capability, the PMA PHY Control function also coordinates transitions between the LPI mode and the normal operating mode.

PMA functions and state diagrams are specified in 40.4. PMA electrical specifications are given in 40.6.

40.1.4 Signaling

1000BASE-T signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over each wire pair. The signaling scheme achieves a number of objectives including

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping and inverse mapping from octet data to a quartet of quinary symbols and back.
c) Uncorrelated symbols in the transmitted symbol stream.
d) No correlation between symbol streams traveling both directions on any pair combination.
e) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
f) Idle mode uses a subset of code-groups in that each symbol is restricted to the set {2, 0, –2}to ease synchronization, startup, and retraining.
g) Ability to rapidly or immediately determine if a symbol stream represents data or idle or carrier extension.
h) Robust delimiters for Start-of-Stream delimiter (SSD), End-of-Stream delimiter (ESD), and other control signals.
i) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
j) Optionally, ability to signal to the remote PHY a request to enter the LPI mode and to exit the LPI mode and return to normal operation.
k) Optionally, ability to signal to the remote PHY that the update of the local receiver state (e.g., timing recovery, adaptive filter coefficients) has completed.
l) Ability to automatically detect and correct for pair swapping and unexpected crossover connections.
m) Ability to automatically detect and correct for incorrect polarity in the connections.
n) Ability to automatically correct for differential delay variations across the wire-pairs.

The PHY may operate in three basic modes, normal mode, training mode, or an optional LPI mode. In normal mode, PCS generates code-groups that represent data, control, or idles for transmission by the PMA. In training mode, the PCS is directed to generate only idle code-groups for transmission by the PMA, which enable the receiver at the other end to train until it is ready to operate in normal mode. In LPI mode, the PCS is directed to generate only idle code-groups encoded with LPI request and update status indications, or zeros as dictated by the PMA PHY Control function. (See the PCS reference diagram in 40.2.)

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40.1.5 Inter-sublayer interfaces

All implementations of the balanced cabling link are compatible at the MDI. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and GMII (if the GMII is implemented) specifications are met. When the PHY is incorporated within the physical bounds of a single-port device or a multiport device, implementation of the GMII is optional. System operation from the perspective of signals at the MDI and management objects are identical whether the GMII is implemented or not.

40.1.6 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

Default initializations, unless specifically specified, are left to the implementer.

40.2 1000BASE-T Service Primitives and Interfaces

1000BASE-T transfers data and control information across the following four service interfaces:

a) Gigabit Media Independent Interface (GMII)
b) PMA Service Interface
c) Medium Dependent Interface (MDI)
d) Technology-Dependent Interface

The GMII is specified in Clause 35; the Technology-Dependent Interface is specified in Clause 28. The PMA Service Interface is defined in 40.2.2 and the MDI is defined in 40.8.

40.2.1 Technology-Dependent Interface

1000BASE-T uses the following service primitives to exchange status indications and control signals across the Technology-Dependent Interface as specified in Clause 28:

PMA_LINK.request (link_control)

PMA_LINK.indication (link_status)

40.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation algorithm to enable and disable operation of the PMA as specified in 28.2.6.2.

40.2.1.1.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

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SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PMA reports link_status=FAIL.PHY processes are disabled.
DISABLE	Set by the Auto-Negotiation algorithm in the event fast link pulses are detected. PHY processes are disabled. This allows the Auto-Negotiation algorithm to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions.

40.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in Clause 28.

40.2.1.1.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as defined in 40.4.2.5.

40.2.1.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 28.2.6.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation algorithm about the status of the underlying link.

40.2.1.2.1 Semantics of the primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK.

FAIL	No valid link established.
READY	The Link Monitor function indicates that a 1000BASE-T link is intact and ready to be established.
OK	The Link Monitor function indicates that a valid 1000BASE-T link is established. Reliable reception of signals transmitted from the remote PHY is possible.

40.2.1.2.2 When generated

The PMA generates this primitive continuously to indicate the value of link_status in compliance with the state diagram given in Figure 40–17.

40.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 40.3.3.1.

40.2.2 PMA Service Interface

1000BASE-T uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication (tx_mode)

PMA_CONFIG.indication (config)

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PMA_UNITDATA.request (tx_symb_vector)

PMA_UNITDATA.indication (rx_symb_vector)

PMA_SCRSTATUS.request (scr_status)

PMA_RXSTATUS.indication (loc_rcvr_status)

PMA_REMRXSTATUS.request (rem_rcvr_status)

PMA_LPIMODE.indication(lpi_mode)

PMA_LPIREQ.request(loc_lpi_req)

PMA_REMLPIREQ.request(rem_lpi_req)

PMA_UPDATE.indication(loc_update_done)

PMA_REMUPDATE.request(rem_update_done)

The use of these primitives is illustrated in Figure 40–4.

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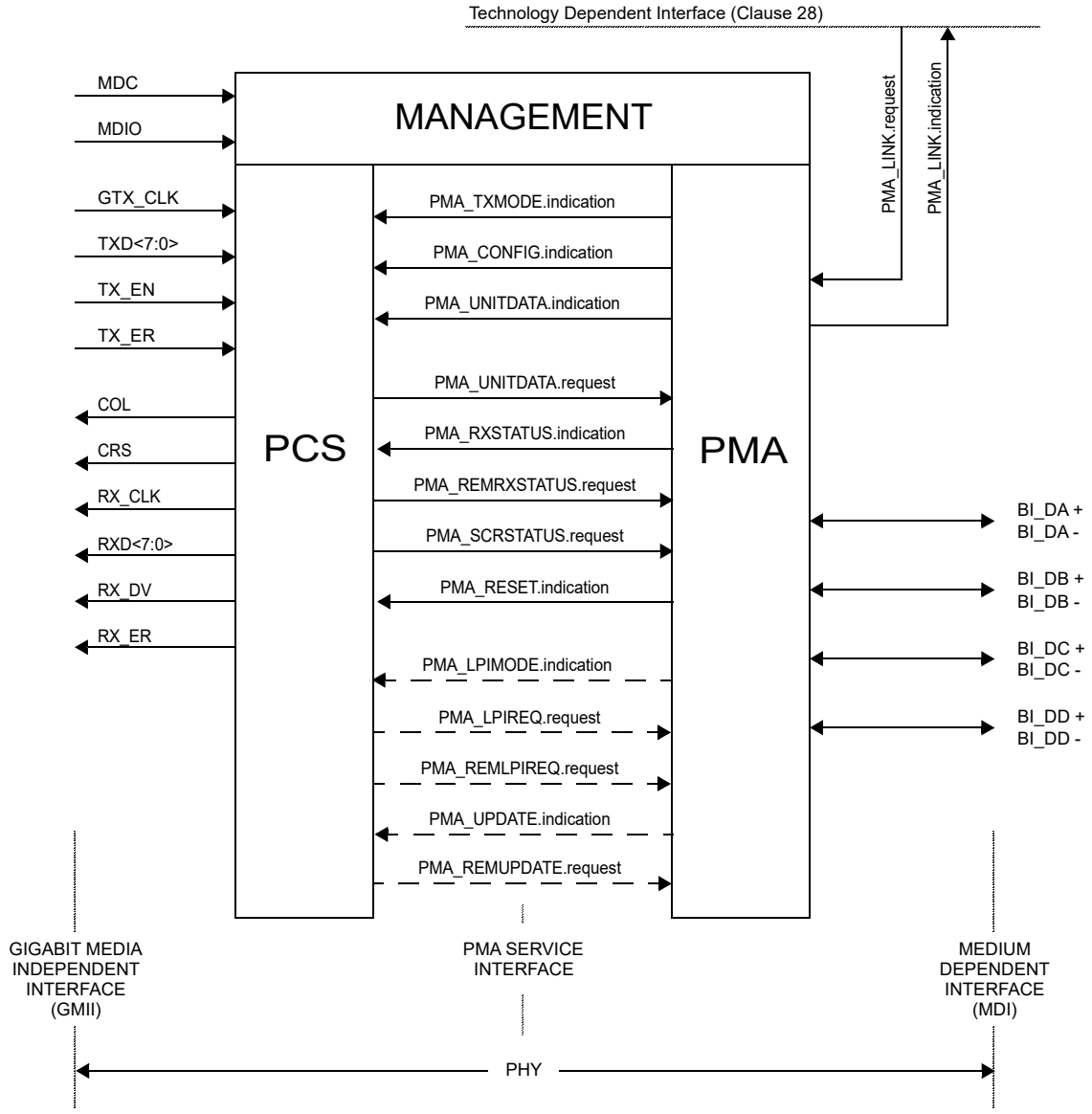

NOTE—Service interface primitives shown with dashed lines are only required for the EEE capability.

Figure 40–4—1000BASE-T service interfaces

40.2.3 PMA_TXMODE.indication

The transmitter in a 1000BASE-T link normally sends over the four pairs, code-groups that can represent a GMII data stream, control information, or idles.

40.2.3.1 Semantics of the primitive

PMA_TXMODE.indication (tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of code-groups the PCS should be transmitting. The parameter tx_mode can take on one of the following three values of the form:

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SEND_N This value is continuously asserted when transmission of sequences of code-groups representing a GMII data stream (data mode), control mode or idle mode is to take place.

SEND_I This value is continuously asserted in case transmission of sequences of code-groups representing the idle mode is to take place.

SEND_Z This value is continuously asserted in case transmission of zeros is required.

40.2.3.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages continuously.

40.2.3.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Transmit function as described in 40.3.1.3.

40.2.4 PMA_CONFIG.indication

Each PHY in a 1000BASE-T link is capable of operating as a MASTER PHY and as a SLAVE PHY. MASTER-SLAVE configuration is determined during Auto-Negotiation (40.5). The result of this negotiation is provided to the PMA.

40.2.4.1 Semantics of the primitive

PMA_CONFIG.indication (config)

PMA_CONFIG.indication specifies to PCS and PMA Transmit via the parameter config whether the PHY operates as a MASTER PHY or as a SLAVE PHY. The parameter config can take on one of the following two values of the form:

MASTER This value is continuously asserted when the PHY operates as a MASTER PHY.

SLAVE This value is continuously asserted when the PHY operates as a SLAVE PHY.

40.2.4.2 When generated

PMA generates PMA_CONFIG.indication messages continuously.

40.2.4.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter config.

40.2.5 PMA_UNITDATA.request

This primitive defines the transfer of code-groups in the form of the tx_symb_vector parameter from the PCS to the PMA. The code-groups are obtained in the PCS Transmit function using the encoding rules defined in 40.3.1.3 to represent GMII data streams, an idle mode, or other sequences.

40.2.5.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

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During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. The tx_symb_vector parameter takes on the form:

SYMB_4D A vector of four quinary symbols, one for each of the four transmit pairs
BI_DA, BI_DB, BI_DC, and BI_DD. Each quinary symbol may take on
one of the values –2, –1, 0, +1, or +2.

The quinary symbols that are elements of tx_symb_vector are called, according to the pair on which each will be transmitted, tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD].

40.2.5.2 When generated

The PCS generates PMA_UNITDATA.request (SYMB_4D) synchronously with every transmit clock cycle.

40.2.5.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated quinary symbols. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD.

40.2.6 PMA_UNITDATA.indication

This primitive defines the transfer of code-groups in the form of the rx_symb_vector parameter from the PMA to the PCS.

40.2.6.1 Semantics of the primitive

PMA_UNITDATA.indication (rx_symb_vector)

During reception the PMA_UNITDATA.indication simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on each of the four receive pairs BI_DA, BI_DB, BI_DC, and BI_DD. The rx_symbol_vector parameter takes on the form:

SYMB_4DA vector of four quinary symbols, one for each of the four receive pairs
BI_DA, BI_DB, BI_DC, and BI_DD. Each quinary symbol may take on
one of the values –2, –1, 0, +1, or +2.

The quinary symbols that are elements of rx_symb_vector are called, according to the pair upon which each symbol was received, rx_symbol_vector[BI_DA], rx_symbol_vector[BI_DB], rx_symbol_vector[BI_DC], and rx_symb_vector[BI_DD].

40.2.6.2 When generated

The PMA generates PMA_UNITDATA.indication (SYMB_4D) messages synchronously with signals received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is 125 MHz, as governed by the recovered clock.

40.2.6.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

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40.2.7 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the descrambler has achieved synchronization.

40.2.7.1 Semantics of the primitive

PMA_SCRSTATUS.request (scr_status)

The scr_status parameter can take on one of two values of the form:

OK The descrambler has achieved synchronization.
NOT_OK The descrambler is not synchronized.

40.2.7.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages continuously.

40.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in 40.4.2.3, 40.4.2.4, and 40.4.6.1.

40.2.8 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol streams that represent the idle mode.

40.2.8.1 Semantics of the primitive

PMA_RXSTATUS.indication (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OKThis value is asserted whenever operation of the link for the local PHY is unreliable.

40.2.8.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages continuously on the basis of signals received at the MDI.

40.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 40–16a and in subclauses 40.2 and 40.4.6.2.

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40.2.9 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The criterion for setting the parameter rem_rcvr_status is left to the implementer. It can be based, for example, on asserting rem_rcvr_status is NOT_OK until loc_rcvr_status is OK and then asserting the detected value of rem_rcvr_status after proper PCS receive decoding is achieved.

40.2.9.1 Semantics of the primitive

PMA_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK The receive link for the remote PHY is operating reliably.
NOT_OKReliable operation of the receive link for the remote PHY is not detected.

40.2.9.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages continuously on the basis on signals received at the MDI.

40.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 40–16a.

40.2.10 PMA_RESET.indication

This primitive is used to pass the PMA Reset function to the PCS (pcs_reset=ON) when reset is enabled.

The PMA_RESET.indication primitive can take on one of two values:

TRUE Reset is enabled.
FALSE Reset is not enabled.

40.2.10.1 When generated

The PMA Reset function is executed as described in 40.4.2.1.

40.2.10.2 Effect of receipt

The effect of receipt of this primitive is specified in 40.4.2.1.

40.2.11 PMA_LPIMODE.indication

This primitive is generated by the PMA to indicate that the PHY has entered the LPI mode of operation.

40.2.11.1 Semantics of the primitive

PMA_LPIMODE.indication(lpi_mode)

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PMA_LPIMODE.indication specifies to the PCS Receive function, via the parameter lpi_mode, whether or not the PHY has entered LPI mode. The parameter lpi_mode can take on one of the following values of the form:

ON	This value is asserted with the PHY is operating in LPI mode.
OFF	This value is asserted during normal operation.

40.2.11.2 When generated

The PMA PHY Control function generates PMA_LPIMODE.indication messages continuously.

40.2.11.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Receive function as described in 40.3.1.4.

40.2.12 PMA_LPIREQ.request

This primitive is generated by the PCS to indicate a request to enter the LPI mode.

40.2.12.1 Semantics of the primitive

PMA_LPIREQ.request (loc_lpi_req)

PMA_LPIREQ.request specifies to the PMA PHY Control, via the parameter loc_lpi_req, whether or not the PHY is requested to enter the LPI mode. The parameter loc_lpi_req can take on one of the following values of the form:

TRUE	This value is continuously asserted when “Assert LPI” is present on the GMII. Note that “Assert LPI” at the GMII implies that no frame transmission is in progress hence 1000BTtransmit (see 40.3.3.1) will be set to FALSE by the PCS Transmit state diagram.
FALSE	This value is continuously asserted when “Assert LPI” is not present at the GMII.

40.2.12.2 When generated

The PCS Local LPI Request function generates PMA_LPIREQ.request messages continuously.

40.2.12.3 Effect of receipt

Upon receipt of this primitive, the PMA performs its PHY Control function as described in 40.4.2.4.

40.2.13 PMA_REMLPIREQ.request

This primitive is generated by the PCS to indicate a request to enter LPI mode as communicated by the remote PHY via its encoding of its loc_lpi_req parameter.

40.2.13.1 Semantics of the primitive

PMA_REMLPIREQ.request (rem_lpi_req)

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PMA_REMLPIREQ.request specifies to the PMA PHY Control, via the parameter rem_lpi_req, whether or not the remote PHY is requesting entry into the LPI mode. The parameter rem_lpi_req can take on one of the following values of the form:

TRUE	This value is continuously asserted when LPI is encoded in the received symbols.
FALSE	This value is continuously asserted when LPI is not encoded in the received symbols.

40.2.13.2 When generated

The PCS Receive function generates PMA_REMLPIREQ.request messages continuously on the basis of the signals received at the MDI.

40.2.13.3 Effect of receipt

Upon receipt of this primitive, the PMA performs its PHY Control function as described in 40.4.2.4.

40.2.14 PMA_UPDATE.indication

This primitive is generated by the PMA to indicate that the PHY has completed the update of its receiver state (e.g., timing recovery, adaptive filter coefficients).

40.2.14.1 Semantics of the primitive

PMA_UPDATE.indication(loc_update_done)

PMA_UPDATE.indication specifies to the PCS Transmit functions, via the parameter loc_update_done, whether or not the PHY has completed the update of its receiver state. The parameter loc_update_done can take on one of the following values of the form:

TRUE	This value is asserted when the PHY has completed the current update.
FALSE	This value is asserted when the PHY is ready for the next update or when the current update is still in progress.

40.2.14.2 When generated

The PMA PHY Control function generates PMA_UPDATE.indication messages continuously.

40.2.14.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Transmit function as described in 40.3.1.3 and 40.3.1.4.

40.2.15 PMA_REMUPDATE.request

This primitive is generated by the PCS to indicate that the remote PHY has completed the update of its receiver state (e.g., timing recovery, adaptive filter coefficients).

40.2.15.1 Semantics of the primitive

PMA_REMUPDATE.request(rem_update_done)

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PMA_REMUPDATE.indication specifies to the PMA PHY Control function, via the parameter rem_update_done, whether or not the remote PHY has completed the update of its receiver state. The parameter rem_update_done can take on one of the following values of the form:

TRUE	This value is asserted when the remote PHY has completed the current update.
FALSE	This value is asserted to when the remote PHY is ready for the next update or when the current update is still in progress.

40.2.15.2 When generated

The PCS Receive function generates PMA_REMUDPATE.request messages continuously.

40.2.15.3 Effect of receipt

Upon receipt of this primitive, the PMA performs its PHY Control function as described in 40.4.2.4.

40.3 Physical Coding Sublayer (PCS)

The PCS comprises one PCS Reset function and four simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit Enable, PCS Transmit, PCS Receive, and PCS Carrier Sense. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 40–5, shows how the four operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive, and are not shown in Figure 40–5. Management is specified in Clause 30. See also Figure 40–7, which defines the structure of frames passed from PCS to PMA.

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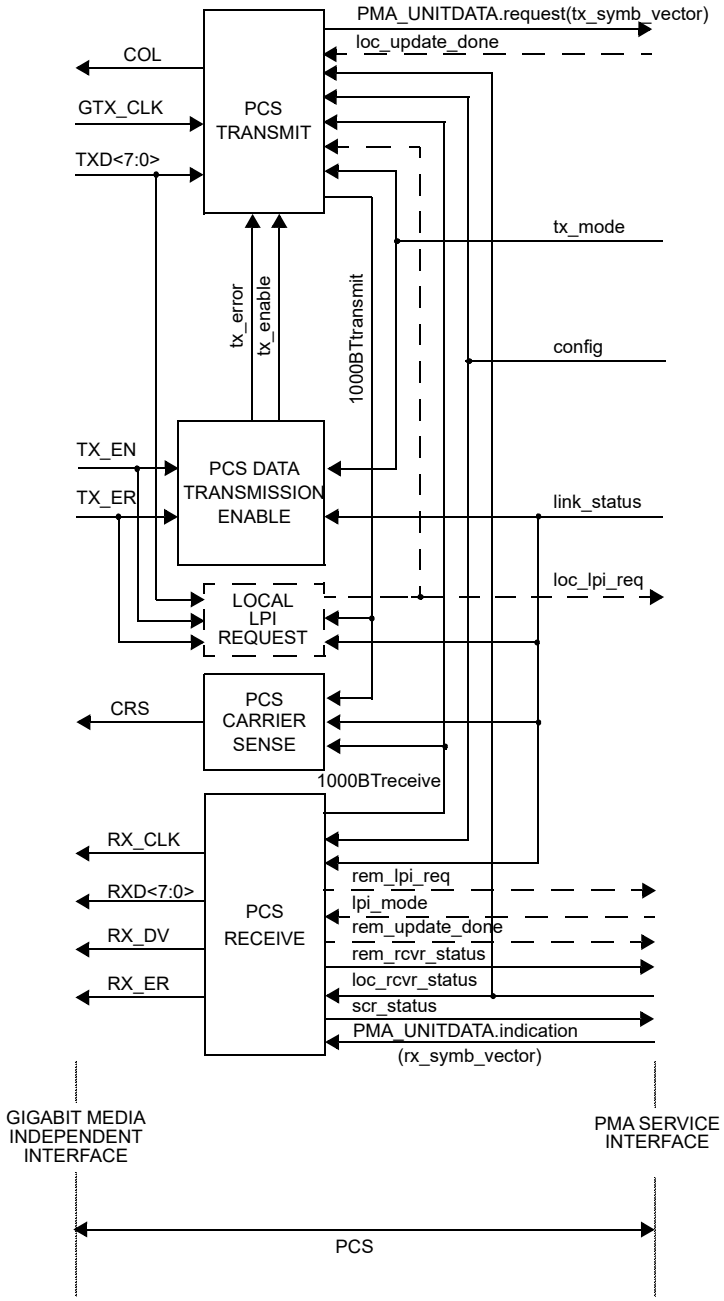

NOTE—Signals and functions shown with dashed lines are only required for the EEE capability.

Figure 40–5—PCS reference diagram

40.3.1 PCS functions

40.3.1.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

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a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset=ON while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

40.3.1.2 PCS Data Transmission Enable

The PCS Data Transmission Enabling process generates the signals tx_enable and tx_error, which PCS Transmit uses for data and carrier extension encoding. The process uses logical operations on tx_mode, TX_ER, TX_EN, and TXD<7:0>. The PCS shall implement the Data Transmission Enabling process as depicted in Figure 40–8 including compliance with the associated state variables as specified in 40.3.3.

40.3.1.3 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 40–10.

The PCS Transmit function generates the GMII signal COL based on whether a reception is occurring simultaneously with transmission. The PCS Transmit function is not required to generate the GMII signal COL in a 1000BASE-T PHY that does not support half duplex operation.

In each symbol period, PCS Transmit generates a code-group (A_n, B_n, C_n, D_n) that is transferred to the PMA via the PMA_UNITDATA.request primitive. The PMA transmits symbols A_n, B_n, C_n, D_n over wire-pairs BI_DA, BI_DB, BI_DC, and BI_DD respectively. The integer, n, is a time index that is introduced to establish a temporal relationship between different symbol periods. A symbol period, T, is nominally equal to 8 ns. In normal mode of operation, between streams of data indicated by the parameter tx_enable, PCS Transmit generates sequences of vectors using the encoding rules defined for the idle mode. Upon assertion of tx_enable, PCS Transmit passes a SSD of two consecutive vectors of four quinary symbols to the PMA, replacing the first two preamble octets. Following the SSD, each TXD<7:0> octet is encoded using an 4D-PAM5 technique into a vector of four quinary symbols until tx_enable is de-asserted. If TX_ER is asserted while tx_enable is also asserted, then PCS Transmit passes to the PMA vectors indicating a transmit error. Note that if the signal TX_ER is asserted while SSD is being sent, the transmission of the error condition is delayed until transmission of SSD has been completed. Following the de-assertion of tx_enable, a Convolutional State Reset (CSReset) of two consecutive code-groups, followed by an ESD of two consecutive code-groups, is generated, after which the transmission of idle or control mode is resumed.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_I, PCS Transmit generates sequences of code-groups according to the encoding rule in training mode. Special code-groups that use only the values {+2, 0, –2} are transmitted in this case. Training mode encoding also takes into account the value of the parameter loc_rcvr_status. By this mechanism, a PHY indicates the status of its own receiver to the link partner during idle transmission.

When the PHY supports the optional EEE capability, the LPI mode encoding also takes into account the value of the parameter loc_lpi_req. By this mechanism, the PHY indicates whether it requests to operate in LPI mode or return to the normal mode of operation. In addition, LPI mode encoding takes into account the value of loc_update_done. By this mechanism, the PHY indicates whether it has completed the update of its receiver state (e.g., timing recovery, adaptive filter coefficients) or not, as indicated by the PMA PHY Control function.

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In the normal mode of operation, the PMA_TXMODE.indication message has the value SEND_N, and the PCS Transmit function uses an 8B1Q4 coding technique to generate at each symbol period code-groups that represent data, control or idle based on the code-groups defined in Table 40–1 and Table 40–2. During transmission of data, the TXD<7:0> bits are scrambled by the PCS using a side-stream scrambler, then encoded into a code-group of quinary symbols and transferred to the PMA. During data encoding, PCS Transmit utilizes a three-state convolutional encoder.

The transition from idle or carrier extension to data is signaled by inserting a SSD, and the end of transmission of data is signaled by an ESD. Further code-groups are used for signaling the assertion of TX_ER within a stream of data, carrier extension, CSReset, and other control functions. During idle and carrier extension encoding, special code-groups with symbol values restricted to the set {2, 0, –2} are used. These code-groups are also generated using the transmit side-stream scrambler. However, the encoding rules for the idle, SSD, and carrier extend code-groups are different from the encoding rules for data, CSReset, CSExtend, and ESD code-groups. During idle, SSD, and carrier extension, the PCS Transmit function reverses the sign of the transmitted symbols. This allows, at the receiver, sequences of code-groups that represent data, CSReset, CSExtend, and ESD to be easily distinguished from sequences of code-groups that represent SSD, carrier extension, and idle.

PCS encoding involves the generation of the four-bit words $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$ from which the quinary symbols (A_n, B_n, C_n, D_n) are obtained. The four-bit words $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$ are determined (as explained in 40.3.1.3.2) from sequences of pseudorandom binary symbols derived from the transmit side-stream scrambler.

40.3.1.3.1 Side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indication message assumes the value MASTER, PCS Transmit shall employ

$$g_M(x) = 1 + x^{13} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. If the PMA_CONFIG.indication message assumes the value of SLAVE, PCS Transmit shall employ

$$g_S(x) = 1 + x^{20} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. An implementation of master and slave PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 40–6. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

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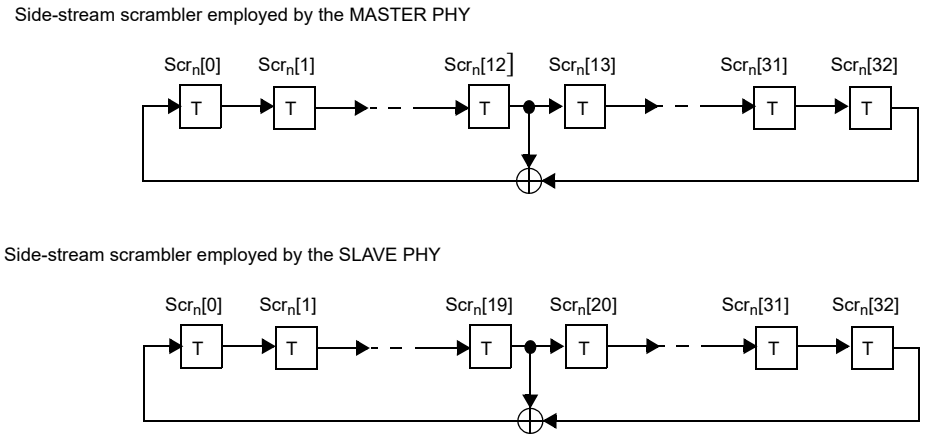

Figure 40–6—A realization of side-stream scramblers by linear feedback shift registers

40.3.1.3.2 Generation of bits $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$

PCS Transmit encoding rules are based on the generation, at time n, of the twelve bits $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$. The eight bits, $Sx_n[3:0]$ and $Sy_n[3:0]$, are used to generate the scrambler octet $Sc_n[7:0]$ for decorrelating the GMII data word TXD<7:0> during data transmission and for generating the idle and training symbols. The four bits, $Sg_n[3:0]$, are used to randomize the signs of the quinary symbols (A_n, B_n, C_n, D_n) so that each symbol stream has no dc bias. These twelve bits are generated in a systematic fashion using three bits, X_n, Y_n, and $Scr_n[0]$, and an auxiliary generating polynomial, g(x). The two bits, X_n and Y_n, are mutually uncorrelated and also uncorrelated with the bit $Scr_n[0]$. For both master and slave PHYs, they are obtained by the same linear combinations of bits stored in the transmit scrambler shift register delay line. These two bits are derived from elements of the same maximum-length shift register sequence of length $2^{33} - 1$ as $Scr_n[0]$, but shifted in time. The associated delays are all large and different so that there is no short-term correlation among the bits $Scr_n[0]$, X_n, and Y_n. The bits X_n and Y_n are generated as follows:

$$X_n = Scr_n[4] \wedge Scr_n[6]$$

$$Y_n = Scr_n[1] \wedge Scr_n[5]$$

where ^ denotes the XOR logic operator. From the three bits X_n, Y_n, and $Scr_n[0]$, further mutually uncorrelated bit streams are obtained systematically using the generating polynomial

$$g(x) = x^3 \wedge x^8$$

The four bits $Sy_n[3:0]$ are generated using the bit $Scr_n[0]$ and g(x) as in the following equations:

$$Sy_n[0] = Scr_n[0]$$

$$Sy_n[1] = g(Scr_n[0]) = Scr_n[3] \wedge Scr_n[8]$$

$$Sy_n[2] = g^2(Scr_n[0]) = Scr_n[6] \wedge Scr_n[16]$$

$$Sy_n[3] = g^3(Scr_n[0]) = Scr_n[9] \wedge Scr_n[14] \wedge Scr_n[19] \wedge Scr_n[24]$$

The four bits $Sx_n[3:0]$ are generated using the bit X_n and g(x) as in the following equations:

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$Sx_n[0] = X_n = Scr_n[4] \wedge Scr_n[6]$

$Sx_n[1] = g(X_n) = Scr_n[7] \wedge Scr_n[9] \wedge Scr_n[12] \wedge Scr_n[14]$

$Sx_n[2] = g^2(X_n) = Scr_n[10] \wedge Scr_n[12] \wedge Scr_n[20] \wedge Scr_n[22]$

$Sx_n[3] = g^3(X_n) = Scr_n[13] \wedge Scr_n[15] \wedge Scr_n[18] \wedge Scr_n[20] \wedge Scr_n[23] \wedge Scr_n[25] \wedge Scr_n[28] \wedge Scr_n[30]$

The four bits $Sg_n[3:0]$ are generated using the bit Y_n and g(x) as in the following equations:

$Sg_n[0] = Y_n = Scr_n[1] \wedge Scr_n[5]$

$Sg_n[1] = g(Y_n) = Scr_n[4] \wedge Scr_n[8] \wedge Scr_n[9] \wedge Scr_n[13]$

$Sg_n[2] = g^2(Y_n) = Scr_n[7] \wedge Scr_n[11] \wedge Scr_n[17] \wedge Scr_n[21]$

$Sg_n[3] = g^3(Y_n) = Scr_n[10] \wedge Scr_n[14] \wedge Scr_n[15] \wedge Scr_n[19] \wedge Scr_n[20] \wedge Scr_n[24] \wedge Scr_n[25] \wedge Scr_n[29]$

By construction, the twelve bits $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$ are derived from elements of the same maximum-length shift register sequence of length $2^{33}-1$ as $Scr_n[0]$, but shifted in time by varying delays. The associated delays are all large and different so that there is no apparent correlation among the bits.

40.3.1.3.3 Generation of bits $Sc_n[7:0]$

The bits $Sc_n[7:0]$ are used to scramble the GMII data octet TXD[7:0] and for control, idle, and training mode quartet generation. The definition of these bits is dependent upon the bits $Sx_n[3:0]$ and $Sy_n[3:0]$ that are specified in 40.3.1.3.2, the variable tx_mode that is obtained through the PMA Service Interface, the variable tx_enable_n that is defined in Figure 40–8, and the time index n.

The four bits $Sc_n[7:4]$ are defined as

$$Sc_n[7:4] = \begin{cases} Sx_n[3:0] & \text{if } (tx\_enable_{n-2} = 1) \\ [0\ 0\ 0\ 0] & \text{else} \end{cases}$$

The bits $Sc_n[3:1]$ are defined as

$$Sc_n[3:1] = \begin{cases} [0\ 0\ 0] & \text{if } (tx\_mode = SEND\_Z) \\ Sy_n[3:1] & \text{else if } (n\text{-}n_0) = 0 \pmod 2 \\ (Sy_{n-1}[3:1] \wedge [1\ 1\ 1]) & \text{else} \end{cases}$$

where n_0 denotes the time index of the last transmitter side-stream scrambler reset.

The bit $Sc_n[0]$ is defined as

$$Sc_n[0] = \begin{cases} 0 & \text{if } (tx\_mode = SEND\_Z) \\ Sy_n[0] & \text{else} \end{cases}$$

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40.3.1.3.4 Generation of bits $Sd_n[8:0]$

The PCS Transmit function generates a nine-bit word $Sd_n[8:0]$ from Sc_n that represents either a convolutionally encoded stream of data, control, or idle mode code-groups. The convolutional encoder uses a three-bit word $cs_n[2:0]$, which is defined as

$$cs_n[1] = \begin{cases} Sd_n[6] \wedge cs_{n-1}[0] & \text{if } (tx\_enable_{n-2} = 1) \\ 0 & \text{else} \end{cases}$$

$$cs_n[2] = \begin{cases} Sd_n[7] \wedge cs_{n-1}[1] & \text{if } (tx\_enable_{n-2} = 1) \\ 0 & \text{else} \end{cases}$$

$$cs_n[0] = cs_{n-1}[2]$$

from which $Sd_n[8]$ is obtained as

$$Sd_n[8] = cs_n[0]$$

The convolutional encoder bits are non-zero only during the transmission of data. Upon the completion of a frame, the convolutional encoder bits are reset using the bit $csreset_n$. The bit $csreset_n$ is defined as

$$csreset_n = (tx\_enable_{n-2}) \text{ and } (\text{not } tx\_enable_n)$$

The bits $Sd_n[7:6]$ are derived from the bits $Sc_n[7:6]$, the GMII data bits $TXD_n[7:6]$, and from the convolutional encoder bits as

$$Sd_n[7] = \begin{cases} Sc_n[7] \wedge TXD_n[7] & \text{if } (csreset_n = 0 \text{ and } tx\_enable_{n-2} = 1) \\ cs_{n-1}[1] & \text{else if } (csreset_n = 1) \\ Sc_n[7] & \text{else} \end{cases}$$

$$Sd_n[6] = \begin{cases} Sc_n[6] \wedge TXD_n[6] & \text{if } (csreset_n = 0 \text{ and } tx\_enable_{n-2} = 1) \\ cs_{n-1}[0] & \text{else if } (csreset_n = 1) \\ Sc_n[6] & \text{else} \end{cases}$$

The bits $Sd_n[5:4]$ are derived from the bits $Sc_n[5:4]$ and the GMII data bits $TXD_n[5:4]$ as

$$Sd_n[5:4] = \begin{cases} Sc_n[5:4] \wedge TXD_n[5:4] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[5:4] & \text{else} \end{cases}$$

The bit $Sd_n[3]$ is used to scramble the GMII data bit $TXD_n[3]$ during data mode and to encode loc_lpi_req otherwise. It is defined as

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$$Sd_n[3] = \begin{cases} Sc_n[3] \wedge TXD_n[3] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[3] \wedge 1 & \text{else if } ((loc\_lpi\_req = \text{TRUE}) \text{ and } (tx\_mode \neq \text{SEND\_Z})) \\ Sc_n[3] & \text{else} \end{cases}$$

The bit $Sd_n[2]$ is used to scramble the GMII data bit $TXD_n[2]$ during data mode and to encode loc_rcvr_status otherwise. It is defined as

$$Sd_n[2] = \begin{cases} Sc_n[2] \wedge TXD_n[2] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[2] \wedge 1 & \text{else if } ((loc\_rcvr\_status = \text{OK}) \text{ and } (tx\_mode \neq \text{SEND\_Z})) \\ Sc_n[2] & \text{else} \end{cases}$$

The bits $Sd_n[1:0]$ are used to transmit carrier extension information during tx_mode=SEND_N and are thus dependent upon the bits $cext_n$ and $cext\_err_n$. In addition, bit $Sd_n[1]$ is used to encode loc_update_done. These bits are dependent on the variable tx_error_n, which is defined in Figure 40–8. These bits are defined as

$$cext_n = \begin{cases} tx\_error_n & \text{if } ((tx\_enable_n = 0) \text{ and } (TXD_n[7:0] = 0\text{x}0\text{F})) \\ 0 & \text{else} \end{cases}$$

$$cext\_err_n = \begin{cases} tx\_error_n & \text{if } ((tx\_enable_n = 0) \text{ and } (TXD_n[7:0] \neq 0\text{x}0\text{F}) \text{ and } (loc\_lpi\_req = FALSE)) \\ 0 & \text{else} \end{cases}$$

$$Sd_n[1] = \begin{cases} Sc_n[1] \wedge TXD_n[1] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[1] \wedge 1 & \text{else if } ((loc\_update\_done = \text{TRUE}) \text{ and } (tx\_mode \neq \text{SEND\_Z})) \\ Sc_n[1] \wedge cext\_err_n & \text{else} \end{cases}$$

$$Sd_n[0] = \begin{cases} Sc_n[0] \wedge TXD_n[0] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[0] \wedge cext_n & \text{else} \end{cases}$$

40.3.1.3.5 Generation of quinary symbols TA_n, TB_n, TC_n, TD_n

The nine-bit word $Sd_n[8:0]$ is mapped to a quartet of quinary symbols (TA_n, TB_n, TC_n, TD_n) according to Table 40–1 and Table 40–2 shown as $Sd_n[6:8] + Sd_n[5:0]$.

Encoding of error indication:

If tx_error_n=1 when (tx_enable_n * tx_enable_{n-2}) = 1, error indication is signaled by means of symbol substitution. In this condition, the values of $Sd_n[5:0]$ are ignored during mapping and the symbols corresponding to the row denoted as “xmt_err” in Table 40–1 and Table 40–2 shall be used.

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Encoding of Convolutional Encoder Reset:

If tx_error_n=0 when the variable $csreset_n$ = 1, the convolutional encoder reset condition is normal. This condition is indicated by means of symbol substitution, where the values of $Sd_n[5:0]$ are ignored during mapping and the symbols corresponding to the row denoted as "CSReset" in Table 40–1 and Table 40–2 shall be used.

Encoding of Carrier Extension during Convolutional Encoder Reset:

If tx_error_n=1 when the variable $csreset_n$ = 1, the convolutional encoder reset condition indicates carrier extension. In this condition, the values of $Sd_n[5:0]$ are ignored during mapping and the symbols corresponding to the row denoted as "CSExtend" in Table 40–1 and Table 40–2 shall be used when TXD_n = 0x0F, and the row denoted as "CSExtend_Err" in Table 40–1 and Table 40–2 shall be used when $TXD_n \neq$ 0x0F. The latter condition denotes carrier extension with error. In case carrier extension with error is indicated during the first octet of CSReset, the error condition shall be encoded during the second octet of CSReset, and during the subsequent two octets of the End-of-Stream delimiter as well. Thus, the error condition is assumed to persist during the symbol substitutions at the End-of-Stream.

Encoding of Start-of-Stream delimiter:

The Start-of-Stream delimiter (SSD) is related to the condition SSD_n, which is defined as $(tx\_enable_n) * (!tx\_enable_{n-2}) = 1$, where "*" and "!" denote the logic AND and NOT operators, respectively. For the generation of SSD, the first two octets of the preamble in a data stream are mapped to the symbols corresponding to the rows denoted as SSD1 and SSD2 respectively in Table 40–1. The symbols corresponding to the SSD1 row shall be used when $(tx\_enable_n) * (!tx\_enable_{n-1}) = 1$. The symbols corresponding to the SSD2 row shall be used when $(tx\_enable_{n-1}) * (!tx\_enable_{n-2}) = 1$.

Encoding of End-of-Stream delimiter:

The definition of an End-of-Stream delimiter (ESD) is related to the condition ESD_n, which is defined as $(!tx\_enable_{n-2}) * (tx\_enable_{n-4}) = 1$. This occurs during the third and fourth symbol periods after transmission of the last octet of a data stream.

If carrier extend error is indicated during ESD, the symbols corresponding to the ESD_Ext_Err row shall be used. The two conditions upon which this may occur are

$(tx\_error_n) * (tx\_error_{n-1}) * (tx\_error_{n-2}) * (TXD_n \neq 0x0F) = 1$, and
$(tx\_error_n) * (tx\_error_{n-1}) * (tx\_error_{n-2}) * (tx\_error_{n-3}) * (TXD_n \neq 0x0F) = 1$.

The symbols corresponding to the ESD1 row in Table 40–1 shall be used when $(!tx\_enable_{n-2}) * (tx\_enable_{n-3}) = 1$, in the absence of carrier extend error indication at time n.

The symbols corresponding to the ESD2_Ext_0 row in Table 40–1 shall be used when $(!tx\_enable_{n-3}) * (tx\_enable_{n-4}) * (!tx\_error_n) * (!tx\_error_{n-1}) = 1$.

The symbols corresponding to the ESD2_Ext_1 row in Table 40–1 shall be used when $(!tx\_enable_{n-3}) * (tx\_enable_{n-4}) * (!tx\_error_n) * (tx\_error_{n-1}) * (tx\_error_{n-2}) * (tx\_error_{n-3}) = 1$.

The symbols corresponding to the ESD2_Ext_2 row in Table 40–1 shall be used when $(!tx\_enable_{n-3}) * (tx\_enable_{n-4}) * (tx\_error_n) * (tx\_error_{n-1}) * (tx\_error_{n-2}) * (tx\_error_{n-3}) * (TXD_n = 0x0F) = 1$, in the absence of carrier extend error indication.

NOTE—The ASCII for Table 40–1 and Table 40–2 is available at https://standards.ieee.org/downloads/802.3/.[81]

[81] *Copyright release for symbol codes:* Users of this standard may freely reproduce the symbol codes in this subclause so it can be used for its intended purpose.

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Table 40–1—Bit-to-symbol mapping (even subsets)

		$Sd_n[6:8] = [000]$	$Sd_n[6:8] = [010]$	$Sd_n[6:8] = [100]$	$Sd_n[6:8] = [110]$
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**
Normal	000000	0, 0, 0, 0	0, 0,+1,+1	0,+1,+1, 0	0,+1, 0,+1
Normal	000001	–2, 0, 0, 0	–2, 0,+1,+1	–2,+1,+1, 0	–2,+1, 0,+1
Normal	000010	0,–2, 0, 0	0,–2,+1,+1	0,–1,+1, 0	0,–1, 0,+1
Normal	000011	–2,–2, 0, 0	–2,–2,+1,+1	–2,–1,+1, 0	–2,–1, 0,+1
Normal	000100	0, 0,–2, 0	0, 0,–1,+1	0,+1,–1, 0	0,+1,–2,+1
Normal	000101	–2, 0,–2, 0	–2, 0,–1,+1	–2,+1,–1, 0	–2,+1,–2,+1
Normal	000110	0,–2,–2, 0	0,–2,–1,+1	0,–1,–1, 0	0,–1,–2,+1
Normal	000111	–2,–2,–2, 0	–2,–2,–1,+1	–2,–1,–1, 0	–2,–1,–2,+1
Normal	001000	0, 0, 0,–2	0, 0,+1,–1	0,+1,+1,–2	0,+1, 0,–1
Normal	001001	–2, 0, 0,–2	–2, 0,+1,–1	–2,+1,+1,–2	–2,+1, 0,–1
Normal	001010	0,–2, 0,–2	0,–2,+1,–1	0,–1,+1,–2	0,–1, 0,–1
Normal	001011	–2,–2, 0,–2	–2,–2,+1,–1	–2,–1,+1,–2	–2,–1, 0,–1
Normal	001100	0, 0,–2,–2	0, 0,–1,–1	0,+1,–1,–2	0,+1,–2,–1
Normal	001101	–2, 0,–2,–2	–2, 0,–1,–1	–2,+1,–1,–2	–2,+1,–2,–1
Normal	001110	0,–2,–2,–2	0,–2,–1,–1	0,–1,–1,–2	0,–1,–2,–1
Normal	001111	–2,–2,–2,–2	–2,–2,–1,–1	–2,–1,–1,–2	–2,–1,–2,–1
Normal	010000	+1,+1,+1,+1	+1,+1, 0, 0	+1, 0, 0,+1	+1, 0,+1, 0
Normal	010001	–1,+1,+1,+1	–1,+1, 0, 0	–1, 0, 0,+1	–1, 0,+1, 0
Normal	010010	+1,–1,+1,+1	+1,–1, 0, 0	+1,–2, 0,+1	+1,–2,+1, 0
Normal	010011	–1,–1,+1,+1	–1,–1, 0, 0	–1,–2, 0,+1	–1,–2,+1, 0
Normal	010100	+1,+1,–1,+1	+1,+1,–2, 0	+1, 0,–2,+1	+1, 0,–1, 0
Normal	010101	–1,+1,–1,+1	–1,+1,–2, 0	–1, 0,–2,+1	–1, 0,–1, 0
Normal	010110	+1,–1,–1,+1	+1,–1,–2, 0	+1,–2,–2,+1	+1,–2,–1, 0
Normal	010111	–1,–1,–1,+1	–1,–1,–2, 0	–1,–2,–2,+1	–1,–2,–1, 0
Normal	011000	+1,+1,+1,–1	+1,+1, 0,–2	+1, 0, 0,–1	+1, 0,+1,–2
Normal	011001	–1,+1,+1,–1	–1,+1, 0,–2	–1, 0, 0,–1	–1, 0,+1,–2
Normal	011010	+1,–1,+1,–1	+1,–1, 0,–2	+1,–2, 0,–1	+1,–2,+1,–2
Normal	011011	–1,–1,+1,–1	–1,–1, 0,–2	–1,–2, 0,–1	–1,–2,+1,–2
Normal	011100	+1,+1,–1,–1	+1,+1,–2,–2	+1, 0,–2,–1	+1, 0,–1,–2
Normal	011101	–1,+1,–1,–1	–1,+1,–2,–2	–1, 0,–2,–1	–1, 0,–1,–2
Normal	011110	+1,–1,–1,–1	+1,–1,–2,–2	+1,–2,–2,–1	+1,–2,–1,–2

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Table 40–1—Bit-to-symbol mapping (even subsets) *(continued)*

		$Sd_n[6:8] = [000]$	$Sd_n[6:8] = [010]$	$Sd_n[6:8] = [100]$	$Sd_n[6:8] = [110]$
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**
Normal	011111	–1,–1,–1,–1	–1,–1,–2,–2	–1,–2,–2,–1	–1,–2,–1,–2
Normal	100000	+2, 0, 0, 0	+2, 0,+1,+1	+2,+1,+1, 0	+2,+1, 0,+1
Normal	100001	+2,–2, 0, 0	+2,–2,+1,+1	+2,–1,+1, 0	+2,–1, 0,+1
Normal	100010	+2, 0,–2, 0	+2, 0,–1,+1	+2,+1,–1, 0	+2,+1,–2,+1
Normal	100011	+2,–2,–2, 0	+2,–2,–1,+1	+2,–1,–1, 0	+2,–1,–2,+1
Normal	100100	+2, 0, 0,–2	+2, 0,+1,–1	+2,+1,+1,–2	+2,+1, 0,–1
Normal	100101	+2,–2, 0,–2	+2,–2,+1,–1	+2,–1,+1,–2	+2,–1, 0,–1
Normal	100110	+2, 0,–2,–2	+2, 0,–1,–1	+2,+1,–1,–2	+2,+1,–2,–1
Normal	100111	+2,–2,–2,–2	+2,–2,–1,–1	+2,–1,–1,–2	+2,–1,–2,–1
Normal	101000	0, 0,+2, 0	+1,+1,+2, 0	+1, 0,+2,+1	0,+1,+2,+1
Normal	101001	–2, 0,+2, 0	–1,+1,+2, 0	–1, 0,+2,+1	–2,+1,+2,+1
Normal	101010	0,–2,+2, 0	+1,–1,+2, 0	+1,–2,+2,+1	0,–1,+2,+1
Normal	101011	–2,–2,+2, 0	–1,–1,+2, 0	–1,–2,+2,+1	–2,–1,+2,+1
Normal	101100	0, 0,+2,–2	+1,+1,+2,–2	+1, 0,+2,–1	0,+1,+2,–1
Normal	101101	–2, 0,+2,–2	–1,+1,+2,–2	–1, 0,+2,–1	–2,+1,+2,–1
Normal	101110	0,–2,+2,–2	+1,–1,+2,–2	+1,–2,+2,–1	0,–1,+2,–1
Normal	101111	–2,–2,+2,–2	–1,–1,+2,–2	–1,–2,+2,–1	–2,–1,+2,–1
Normal	110000	0,+2, 0, 0	0,+2,+1,+1	+1,+2, 0,+1	+1,+2,+1, 0
Normal	110001	–2,+2, 0, 0	–2,+2,+1,+1	–1,+2, 0,+1	–1,+2,+1, 0
Normal	110010	0,+2,–2, 0	0,+2,–1,+1	+1,+2,–2,+1	+1,+2,–1, 0
Normal	110011	–2,+2,–2, 0	–2,+2,–1,+1	–1,+2,–2,+1	–1,+2,–1, 0
Normal	110100	0,+2, 0,–2	0,+2,+1,–1	+1,+2, 0,–1	+1,+2,+1,–2
Normal	110101	–2,+2, 0,–2	–2,+2,+1,–1	–1,+2, 0,–1	–1,+2,+1,–2
Normal	110110	0,+2,–2,–2	0,+2,–1,–1	+1,+2,–2,–1	+1,+2,–1,–2
Normal	110111	–2,+2,–2,–2	–2,+2,–1,–1	–1,+2,–2,–1	–1,+2,–1,–2
Normal	111000	0, 0, 0,+2	+1,+1, 0,+2	0,+1,+1,+2	+1, 0,+1,+2
Normal	111001	–2, 0, 0,+2	–1,+1, 0,+2	–2,+1,+1,+2	–1, 0,+1,+2
Normal	111010	0,–2, 0,+2	+1,–1, 0,+2	0,–1,+1,+2	+1,–2,+1,+2
Normal	111011	–2,–2, 0,+2	–1,–1, 0,+2	–2,–1,+1,+2	–1,–2,+1,+2
Normal	111100	0, 0,–2,+2	+1,+1,–2,+2	0,+1,–1,+2	+1, 0,–1,+2
Normal	111101	–2, 0,–2,+2	–1,+1,–2,+2	–2,+1,–1,+2	–1, 0,–1,+2
Normal	111110	0,–2,–2,+2	+1,–1,–2,+2	0,–1,–1,+2	+1,–2,–1,+2

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Table 40–1—Bit-to-symbol mapping (even subsets) *(continued)*

		$Sd_n[6:8] = [000]$	$Sd_n[6:8] = [010]$	$Sd_n[6:8] = [100]$	$Sd_n[6:8] = [110]$
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**
Normal	111111	–2,–2,–2,+2	–1,–1,–2,+2	–2,–1,–1,+2	–1,–2,–1,+2
xmt_err	XXXXXX	0,+2,+2,0	+1,+1,+2,+2	+2,+1,+1,+2	+2,+1,+2,+1
CSExtend_Err	XXXXXX	–2,+2,+2,–2	–1,–1,+2,+2	+2,–1,–1,+2	+2,–1,+2,–1
CSExtend	XXXXXX	+2, 0, 0,+2	+2,+2,+1,+1	+1,+2,+2,+1	+1,+2,+1,+2
CSReset	XXXXXX	+2,–2,–2,+2	+2,+2,–1,–1	–1,+2,+2,–1	–1,+2,–1,+2
SSD1	XXXXXX	+2,+2,+2,+2	—	—	—
SSD2	XXXXXX	+2,+2,+2,–2	—	—	—
ESD1	XXXXXX	+2,+2,+2,+2	—	—	—
ESD2_Ext_0	XXXXXX	+2,+2,+2,–2	—	—	—
ESD2_Ext_1	XXXXXX	+2,+2, –2,+2	—	—	—
ESD2_Ext_2	XXXXXX	+2,–2,+2,+2	—	—	—
ESD_Ext_Err	XXXXXX	–2,+2,+2,+2	—	—	—
Idle/Carrier Extension	000000	0, 0, 0, 0	—	—	—
Idle/Carrier Extension	000001	–2, 0, 0, 0	—	—	—
Idle/Carrier Extension	000010	0,–2, 0, 0	—	—	—
Idle/Carrier Extension	000011	–2,–2, 0, 0	—	—	—
Idle/Carrier Extension	000100	0, 0,–2, 0	—	—	—
Idle/Carrier Extension	000101	–2, 0,–2, 0	—	—	—
Idle/Carrier Extension	000110	0,–2,–2, 0	—	—	—
Idle/Carrier Extension	000111	–2,–2,–2, 0	—	—	—
Idle/Carrier Extension	001000	0, 0, 0,–2	—	—	—
Idle/Carrier Extension	001001	–2, 0, 0,–2	—	—	—
Idle/Carrier Extension	001010	0,–2, 0,–2	—	—	—
Idle/Carrier Extension	001011	–2,–2, 0,–2	—	—	—
Idle/Carrier Extension	001100	0, 0,–2,–2	—	—	—

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Table 40–1—Bit-to-symbol mapping (even subsets) *(continued)*

		$Sd_n[6:8] = [000]$	$Sd_n[6:8] = [010]$	$Sd_n[6:8] = [100]$	$Sd_n[6:8] = [110]$
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**
Idle/Carrier Extension	001101	–2, 0,–2,–2	—	—	—
Idle/Carrier Extension	001110	0,–2,–2,–2	—	—	—
Idle/Carrier Extension	001111	–2,–2,–2,–2	—	—	—

Table 40–2—Bit-to-symbol mapping (odd subsets)

		$Sd_n[6:8] = [001]$	$Sd_n[6:8] = [011]$	$Sd_n[6:8] = [101]$	$Sd_n[6:8] = [111]$
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**
Normal	000000	0, 0, 0,+1	0, 0,+1, 0	0,+1,+1,+1	0,+1, 0, 0
Normal	000001	–2, 0, 0,+1	–2, 0,+1, 0	–2,+1,+1,+1	–2,+1, 0, 0
Normal	000010	0,–2, 0,+1	0,–2,+1, 0	0,–1,+1,+1	0,–1, 0, 0
Normal	000011	–2,–2, 0,+1	–2,–2,+1, 0	–2,–1,+1,+1	–2,–1, 0, 0
Normal	000100	0, 0,–2,+1	0, 0,–1, 0	0,+1,–1,+1	0,+1,–2, 0
Normal	000101	–2, 0,–2,+1	–2, 0,–1, 0	–2,+1,–1,+1	–2,+1,–2, 0
Normal	000110	0,–2,–2,+1	0,–2,–1, 0	0,–1,–1,+1	0,–1,–2, 0
Normal	000111	–2,–2,–2,+1	–2,–2,–1, 0	–2,–1,–1,+1	–2,–1,–2, 0
Normal	001000	0, 0, 0,–1	0, 0,+1,–2	0,+1,+1,–1	0,+1, 0,–2
Normal	001001	–2, 0, 0,–1	–2, 0,+1,–2	–2,+1,+1,–1	–2,+1, 0,–2
Normal	001010	0,–2, 0,–1	0,–2,+1,–2	0,–1,+1,–1	0,–1, 0,–2
Normal	001011	–2,–2, 0,–1	–2,–2,+1,–2	–2,–1,+1,–1	–2,–1, 0,–2
Normal	001100	0, 0,–2,–1	0, 0,–1,–2	0,+1,–1,–1	0,+1,–2,–2
Normal	001101	–2, 0,–2,–1	–2, 0,–1,–2	–2,+1,–1,–1	–2,+1,–2,–2
Normal	001110	0,–2,–2,–1	0,–2,–1,–2	0,–1,–1,–1	0,–1,–2,–2
Normal	001111	–2,–2,–2,–1	–2,–2,–1,–2	–2,–1,–1,–1	–2,–1,–2,–2
Normal	010000	+1,+1,+1, 0	+1,+1, 0,+1	+1, 0, 0, 0	+1, 0,+1,+1
Normal	010001	–1,+1,+1, 0	–1,+1, 0,+1	–1, 0, 0, 0	–1, 0,+1,+1
Normal	010010	+1,–1,+1, 0	+1,–1, 0,+1	+1,–2, 0, 0	+1,–2,+1,+1
Normal	010011	–1,–1,+1, 0	–1,–1, 0,+1	–1,–2, 0, 0	–1,–2,+1,+1
Normal	010100	+1,+1,–1, 0	+1,+1,–2,+1	+1, 0,–2, 0	+1, 0,–1,+1
Normal	010101	–1,+1,–1, 0	–1,+1,–2,+1	–1, 0,–2, 0	–1, 0,–1,+1

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Table 40–2—Bit-to-symbol mapping (odd subsets) *(continued)*

		$Sd_n[6:8] = [001]$	$Sd_n[6:8] = [011]$	$Sd_n[6:8] = [101]$	$Sd_n[6:8] = [111]$
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**
Normal	010110	+1,–1,–1, 0	+1,–1,–2,+1	+1,–2,–2, 0	+1,–2,–1,+1
Normal	010111	–1,–1,–1, 0	–1,–1,–2,+1	–1,–2,–2, 0	–1,–2,–1,+1
Normal	011000	+1,+1,+1,–2	+1,+1, 0,–1	+1, 0, 0,–2	+1, 0,+1,–1
Normal	011001	–1,+1,+1,–2	–1,+1, 0,–1	–1, 0, 0,–2	–1, 0,+1,–1
Normal	011010	+1,–1,+1,–2	+1,–1, 0,–1	+1,–2, 0,–2	+1,–2,+1,–1
Normal	011011	–1,–1,+1,–2	–1,–1, 0,–1	–1,–2, 0,–2	–1,–2,+1,–1
Normal	011100	+1,+1,–1,–2	+1,+1,–2,–1	+1, 0,–2,–2	+1, 0,–1,–1
Normal	011101	–1,+1,–1,–2	–1,+1,–2,–1	–1, 0,–2,–2	–1, 0,–1,–1
Normal	011110	+1,–1,–1,–2	+1,–1,–2,–1	+1,–2,–2,–2	+1,–2,–1,–1
Normal	011111	–1,–1,–1,–2	–1,–1,–2,–1	–1,–2,–2,–2	–1,–2,–1,–1
Normal	100000	+2, 0, 0,+1	+2, 0,+1, 0	+2,+1,+1,+1	+2,+1, 0, 0
Normal	100001	+2,–2, 0,+1	+2,–2,+1, 0	+2,–1,+1,+1	+2,–1, 0, 0
Normal	100010	+2, 0,–2,+1	+2, 0,–1, 0	+2,+1,–1,+1	+2,+1,–2, 0
Normal	100011	+2,–2,–2,+1	+2,–2,–1, 0	+2,–1,–1,+1	+2,–1,–2, 0
Normal	100100	+2, 0, 0,–1	+2, 0,+1,–2	+2,+1,+1,–1	+2,+1, 0,–2
Normal	100101	+2,–2, 0,–1	+2,–2,+1,–2	+2,–1,+1,–1	+2,–1, 0,–2
Normal	100110	+2, 0,–2,–1	+2, 0,–1,–2	+2,+1,–1,–1	+2,+1,–2,–2
Normal	100111	+2,–2,–2,–1	+2,–2,–1,–2	+2,–1,–1,–1	+2,–1,–2,–2
Normal	101000	0, 0,+2,+1	+1,+1,+2,+1	+1, 0,+2, 0	0,+1,+2, 0
Normal	101001	–2, 0,+2,+1	–1,+1,+2,+1	–1, 0,+2, 0	–2,+1,+2, 0
Normal	101010	0,–2,+2,+1	+1,–1,+2,+1	+1,–2,+2, 0	0,–1,+2, 0
Normal	101011	–2,–2,+2,+1	–1,–1,+2,+1	–1,–2,+2, 0	–2,–1,+2, 0
Normal	101100	0, 0,+2,–1	+1,+1,+2,–1	+1, 0,+2,–2	0,+1,+2,–2
Normal	101101	–2, 0,+2,–1	–1,+1,+2,–1	–1, 0,+2,–2	–2,+1,+2,–2
Normal	101110	0,–2,+2,–1	+1,–1,+2,–1	+1,–2,+2,–2	0,–1,+2,–2
Normal	101111	–2,–2,+2,–1	–1,–1,+2,–1	–1,–2,+2,–2	–2,–1,+2,–2
Normal	110000	0,+2, 0,+1	0,+2,+1, 0	+1,+2, 0, 0	+1,+2,+1,+1
Normal	110001	–2,+2, 0,+1	–2,+2,+1, 0	–1,+2, 0, 0	–1,+2,+1,+1
Normal	110010	0,+2,–2,+1	0,+2,–1, 0	+1,+2,–2, 0	+1,+2,–1,+1
Normal	110011	–2,+2,–2,+1	–2,+2,–1, 0	–1,+2,–2, 0	–1,+2,–1,+1
Normal	110100	0,+2, 0,–1	0,+2,+1,–2	+1,+2, 0,–2	+1,+2,+1,–1

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Table 40–2—Bit-to-symbol mapping (odd subsets) *(continued)*

		$Sd_n[6:8]$ = [001]	$Sd_n[6:8]$ = [011]	$Sd_n[6:8]$ = [101]	$Sd_n[6:8]$ = [111]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**
Normal	110101	–2,+2, 0,–1	–2,+2,+1,–2	–1,+2, 0,–2	–1,+2,+1,–1
Normal	110110	0,+2,–2,–1	0,+2,–1,–2	+1,+2,–2,–2	+1,+2,–1,–1
Normal	110111	–2,+2,–2,–1	–2,+2,–1,–2	–1,+2,–2,–2	–1,+2,–1,–1
Normal	111000	+1,+1,+1,+2	0, 0,+1,+2	+1, 0, 0,+2	0,+1, 0,+2
Normal	111001	–1,+1,+1,+2	–2, 0,+1,+2	–1, 0, 0,+2	–2,+1, 0,+2
Normal	111010	+1,–1,+1,+2	0,–2,+1,+2	+1,–2, 0,+2	0,–1, 0,+2
Normal	111011	–1,–1,+1,+2	–2,–2,+1,+2	–1,–2, 0,+2	–2,–1, 0,+2
Normal	111100	+1,+1,–1,+2	0, 0,–1,+2	+1, 0,–2,+2	0,+1,–2,+2
Normal	111101	–1,+1,–1,+2	–2, 0,–1,+2	–1, 0,–2,+2	–2,+1,–2,+2
Normal	111110	+1,–1,–1,+2	0,–2,–1,+2	+1,–2,–2,+2	0,–1,–2,+2
Normal	111111	–1,–1,–1,+2	–2,–2,–1,+2	–1,–2,–2,+2	–2,–1,–2,+2
xmt_err	XXXXXX	+2,+2, 0,+1	0,+2,+1,+2	+1,+2,+2, 0	+2,+1,+2, 0
CSExtend_Err	XXXXXX	+2,+2, –2,–1	–2,+2,–1,+2	–1,+2,+2,–2	+2,–1,+2,–2
CSExtend	XXXXXX	+2, 0,+2,+1	+2, 0,+1,+2	+1, 0,+2,+2	+2,+1, 0,+2
CSReset	XXXXXX	+2,–2,+2,–1	+2,–2,–1,+2	–1,–2,+2,+2	+2,–1,–2,+2

40.3.1.3.6 Generation of A_n, B_n, C_n, D_n

The four bits $Sg_n[3:0]$ are used to randomize the signs of the quinary symbols (A_n, B_n, C_n, D_n) so that each symbol stream has no dc bias. The bits are used to generate binary symbols (SnA_n, SnB_n, SnC_n, SnD_n) that, when multiplied by the quinary symbols (TA_n, TB_n, TC_n, TD_n), result in (A_n, B_n, C_n, D_n).

PCS Transmit ensures a distinction between code-groups transmitted during idle mode plus SSD and those transmitted during other symbol periods. This distinction is accomplished by reversing the mapping of the sign bits when (tx_enable_{n-2} + tx_enable_{n-4}) = 1. This sign reversal is controlled by the variable $Srev_n$ defined as

$$Srev_n = tx\_enable_{n-2} + tx\_enable_{n-4}$$

The binary symbols SnA_n, SnB_n, SnC_n, and SnD_n are defined using $Sg_n[3:0]$ as

$$SnA_n = \begin{cases} +1 \text{ if } [(Sg_n[0] \wedge Srev_n) = 0] \\ -1 \text{ else} \end{cases}$$

$$SnB_n = \begin{cases} +1 \text{ if } [(Sg_n[1] \wedge Srev_n) = 0] \\ -1 \text{ else} \end{cases}$$

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$$SnC_n = \begin{cases} +1 \text{ if } [(Sg_n[2] \wedge Srev_n) = 0] \\ -1 \text{ else} \end{cases}$$

$$SnD_n = \begin{cases} +1 \text{ if } [(Sg_n[3] \wedge Srev_n) = 0] \\ -1 \text{ else} \end{cases}$$

The quinary symbols (A_n, B_n, C_n, D_n) are generated as the product of (SnA_n, SnB_n, SnC_n, SnD_n) and (TA_n, TB_n, TC_n, TD_n) respectively.

$$A_n = TA_n \times SnA_n$$

$$B_n = TB_n \times SnB_n$$

$$C_n = TC_n \times SnC_n$$

$$D_n = TD_n \times SnD_n$$

40.3.1.4 PCS Receive function

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 40–11a including compliance with the associated state variables as specified in 40.3.3.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb_vector. To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode. PCS Receive generates the sequence of vectors of four quinary symbols (RA_n, RB_n, RC_n, RD_n) and indicates the reliable acquisition of the descrambler state by setting the parameter scr_status to OK. The sequence (RA_n, RB_n, RC_n, RD_n) is processed to generate the signals RXD<7:0>, RX_DV, and RX_ER, which are presented to the GMII. PCS Receive detects the transmission of a stream of data from the remote station and conveys this information to the PCS Carrier Sense and PCS Transmit functions via the parameter 1000BTreceive.

When the PHY supports the optional EEE capability, the PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode to derive the values of the variables rem_lpi_req and rem_update_done.

40.3.1.4.1 Decoding of code-groups

When the PMA indicates that correct receiver operation has been achieved by setting the loc_rcvr_status parameter to the value OK, the PCS Receive continuously checks that the received sequence satisfies the encoding rule used in idle mode. When a violation is detected, PCS Receive assigns the value TRUE to the parameter 1000BTreceive and, by examining the last two received vectors (RA_{n-1}, RB_{n-1}, RC_{n-1}, RD_{n-1}) and (RA_n, RB_n, RC_n, RD_n), determines whether the violation is due to reception of SSD or to a receiver error.

Upon detection of SSD, PCS Receive also assigns the value TRUE to the parameter 1000BTreceive that is provided to the PCS Carrier Sense and Collision Presence functions. During the two symbol periods corresponding to SSD, PCS Receive replaces SSD by preamble bits. Upon the detection of SSD, the signal RX_DV is asserted and each received vector is decoded into a data octet RXD<7:0> until ESD is detected.

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Upon detection of a receiver error, the signal RX_ER is asserted and the parameter rxerror_status assumes the value ERROR. De-assertion of RX_ER and transition to the IDLE state (rxerror_status=NO_ERROR) takes place upon detection of four consecutive vectors satisfying the encoding rule used in idle mode.

During reception of a stream of data, PCS Receive checks that the symbols RA_n, RB_n, RC_n, RD_n follow the encoding rule defined in 40.3.1.3.5 for ESD whenever they assume values ± 2. PCS Receive processes two consecutive vectors at each time n to detect ESD. Upon detection of ESD, PCS Receive de-asserts the signal RX_DV on the GMII. If the last symbol period of ESD indicates that a carrier extension is present, PCS Receive will assert the RX_ER signal on the GMII. If no extension is indicated in the ESD2 quartet, PCS Receive assigns the value FALSE to the parameter receiving. If an extension is present, the transition to the IDLE state occurs after detection of a valid idle symbol period and the parameter receiving remains TRUE until check_idle is TRUE. If a violation of the encoding rules is detected, PCS Receive asserts the signal RX_ER for at least one symbol period.

A premature stream termination is caused by the detection of invalid symbols during the reception of a data stream. Then, PCS Receive waits for the reception of four consecutive vectors satisfying the encoding rule used in idle mode prior to de-asserting the error indication. Note that RX_DV remains asserted during the symbol periods corresponding to the first three idle vectors, while RX_ER=TRUE is signaled on the GMII. The signal RX_ER is also asserted in the LINK FAILED state, which ensures that RX_ER remains asserted for at least one symbol period.

40.3.1.4.2 Receiver descrambler polynomials

The PHY shall descramble the data stream and return the proper sequence of code-groups to the decoding process for generation of RXD<7:0> to the GMII. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial $g'_M(x) = 1 + x^{20} + x^{33}$ and the SLAVE PHY shall employ the receiver descrambler generator polynomial $g'_S(x) = 1 + x^{13} + x^{33}$.

40.3.1.5 PCS Carrier Sense function

The PCS Carrier Sense function generates the GMII signal CRS, which the MAC uses for deferral in half duplex mode. The PCS shall conform to the Carrier Sense state diagram as depicted in Figure 40–12 including compliance with the associated state variables as specified in 40.3.3. The PCS Carrier Sense function is not required in a 1000BASE-T PHY that does not support half duplex operation.

40.3.1.6 PCS Local LPI Request function

The PCS Local LPI Request function generates the signal loc_lpi_req, which indicates to the PMA PHY Control function whether or not the local PHY is requested to enter the LPI mode. When the PHY supports the optional EEE capability, the PCS shall conform to the Local LPI Request state diagram as depicted in Figure 40–9 including compliance with the associated state variables as specified in 40.3.3.

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40.3.2 Stream structure

The tx_symb_vector and rx-symb_vector structure is shown in Figure 40–7.

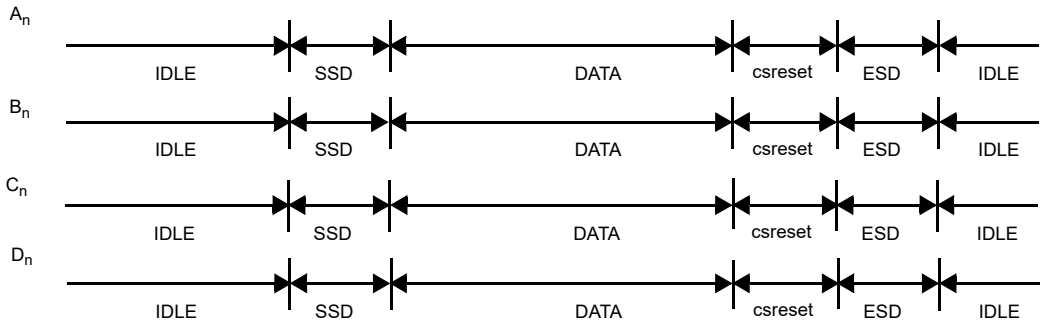

Figure 40–7—The tx_symb_vector and rx-symb_vector structure

40.3.3 State variables

40.3.3.1 Variables

CEXT
: A sequence of vectors of four quinary symbols corresponding to the code-group generated in idle mode to denote carrier extension, as specified in 40.3.1.3.

CEXT_Err
: A sequence of vectors of four quinary symbols corresponding to the code-group generated in idle mode to denote carrier extension with error indication, as specified in 40.3.1.3.

COL
: The COL signal of the GMII as specified in 35.2.2.12.

config
: The config parameter set by PMA and passed to the PCS via the PMA_CONFIG.indication primitive.
Values: MASTER, SLAVE.

CRS
: The CRS signal of the GMII as specified in 35.2.2.11.

CSExtend
: A vector of four quinary symbols corresponding to the code-group indicating convolutional encoder reset condition during carrier extension, as specified in 40.3.1.3.

CSExtend_Err
: A vector of four quinary symbols corresponding to the code-group indicating convolutional encoder reset condition during carrier extension with error indication, as specified in 40.3.1.3.

CSReset
: A vector of four quinary symbols corresponding to the code-group indicating convolutional encoder reset condition in the absence of carrier extension, as specified in 40.3.1.3.

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DATA
: A vector of four quinary symbols corresponding to the code-group indicating valid data, as specified in 40.3.1.3.

ESD1
: A vector of four quinary symbols corresponding to the first code-group of End-of-Stream delimiter, as specified in 40.3.1.3.

ESD2_Ext_0
: A vector of four quinary symbols corresponding to the second code-group of End-of-Stream delimiter in the absence of carrier extension over the two ESD symbol periods, as specified in 40.3.1.3.

ESD2_Ext_1
: A vector of four quinary symbols corresponding to the second code-group of End-of-Stream delimiter when carrier extension is indicated during the first symbol period of the End-of-Stream delimiter, but not during the second symbol period, as specified in 40.3.1.3.

ESD2_Ext_2
: A vector of four quinary symbols corresponding to the second code-group of End-of-Stream delimiter when carrier extension is indicated during the two symbol periods of the End-of-Stream delimiter, as specified in 40.3.1.3.

ESD_Ext_Err
: A vector of four quinary symbols corresponding to either the first or second code-group of End-of-Stream delimiter when carrier extension with error is indicated during the End-of-Stream delimiter, as specified in 40.3.1.3.

IDLE
: A sequence of vectors of four quinary symbols representing the special code-group generated in idle mode in the absence of carrier extension or carrier extension with error indication, as specified in 40.3.1.3.

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

loc_rcvr_status
: The loc_rcvr_status parameter set by the PMA Receive function and passed to the PCS via the PMA_RXSTATUS.indication primitive.
Values: OK or NOT_OK

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: ON or OFF

(RA_n, RB_n, RC_n, RD_n)
: The vector of the four correctly aligned most recently received quinary symbols generated by PCS Receive at time n.

1000BTreceive
: The receiving parameter generated by the PCS Receive function.
Values: TRUE or FALSE

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rem_rcvr_status
: The rem_rcvr_status parameter generated by PCS Receive.
Values: OK or NOT_OK

repeater_mode
: See 36.2.5.1.3

Rx_n
: Alias for rx_symb_vector (a vector RA_n, RB_n, RC_n, RD_n) at time n.

rxerror_status
: The rxerror_status parameter set by the PCS Receive function.
Values: ERROR or NO_ERROR

RX_DV
: The RX_DV signal of the GMII as specified in 35.2.2.7.

RX_ER
: The RX_ER signal of the GMII as specified in 35.2.2.9.

rx_symb_vector
: A vector of four quinary symbols received by the PMA and passed to the PCS via the PMA_UNITDATA.indication primitive.
Value: SYMB_4D

RXD[7:0]
: The RXD<7:0> signal of the GMII as specified in 35.2.2.8.

SSD1
: A vector of four quinary symbols corresponding to the first code-group of the Start-of-Stream delimiter, as specified in 40.3.1.3.5.

SSD2
: A vector of four quinary symbols corresponding to the second code-group of the Start-of-Stream delimiter, as specified in 40.3.1.3.5.

1000BTtransmit
: A Boolean used by the PCS Transmit Process to indicate whether a frame transmission is in progress. Also used by the Carrier Sense and Local LPI Request processes.
Values: TRUE: The PCS is transmitting a stream
FALSE: The PCS is not transmitting a stream

TXD[7:0]
: The TXD<7:0> signal of the GMII as specified in 35.2.2.4.

tx_enable
: The tx_enable parameter generated by PCS Transmit as specified in Figure 40–8.
Values: TRUE or FALSE

tx_error
: The tx_error parameter generated by PCS Transmit as specified in Figure 40–8.
Values: TRUE or FALSE

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TX_EN
: The TX_EN signal of the GMII as specified in 35.2.2.3.

TX_ER
: The TX_ER signal of the GMII as specified in 35.2.2.5.

tx_mode
: The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

Tx_n
: Alias for tx_symb_vector at time n.

tx_symb_vector
: A vector of four quinary symbols generated by the PCS Transmit function and passed to the PMA via the PMA_UNITDATA.request primitive.
Value: SYMB_4D

xmt_err
: A vector of four quinary symbols corresponding to a transmit error indication during normal data transmission or reception, as specified in 40.3.1.3.

The following state variables are only required for the optional EEE capability:

loc_lpi_req
: The loc_lpi_req variable is set by the PCS Local LPI Request function and indicates whether or not the local PHY is requested to enter the LPI mode. It is passed to the PMA PHY Control function via the PMA_LPIREQ.request primitive. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.
Values: TRUE or FALSE

lpi_mode
: The lpi_mode variable is generated by the PMA PHY Control function and indicates whether or not the local PHY has entered LPI mode. It is passed to the PCS Receive function via the PMA_LPIMODE.indication primitive. In the absence of the optional EEE capability, the PHY operates as if the value of this variable is OFF.
Values: ON or OFF

rem_lpi_req
: The rem_lpi_req variable is generated by the PCS Receive function and indicates whether or not the remote PHY is requesting entry into LPI mode. It is passed to the PMA PHY Control function via the PMA_REMLPIREQ.request primitive. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.
Values: TRUE or FALSE

40.3.3.2 Functions

check_end
: A function used by the PCS Receive process to detect the reception of valid ESD symbols. The check_end function operates on the next two rx_symb_vectors, (Rx_{n+1}) and (Rx_{n+2}), available via PMA_UNITDATA.indication, and returns a Boolean value indicating whether these two consecutive vecctors contain symbols corresponding to a legal ESD encoding or not, as specified in 40.3.1.3.

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check_idle
: A function used by the PCS Receive process to detect the reception of valid idle code-groups after an error condition during the process. The check_idle function operates on the current rx_symb_vector and the next three rx_symb_vectors available via PMA_UNITDATA.indication and returns a Boolean value indicating whether the four consecutive vectors contain symbols corresponding to the idle mode encoding or not, as specified in 40.3.1.3.

DECODE
: In the PCS Receive process, this function takes as its argument the value of rx_symb_vector and returns the corresponding GMII RXD<7:0> octet. DECODE follows the rules outlined in 40.2.6.1.

ENCODE
: In the PCS Transmit process, this function takes as its argument GMII TXD <7:0> and returns the corresponding tx_symb_vector. ENCODE follows the rules outlined in 40.2.5.1.

40.3.3.3 Timer

symb_timer
: Continuous timer: The condition symb_timer_done becomes true upon timer expiration.

  Restart time: Immediately after expiration; timer restart resets the condition symb_timer_done.

  Duration: 8 ns nominal. (See clock tolerance in 40.6.1.2.6.)

  Symb-timer shall be generated synchronously with TX_TCLK. In the PCS Transmit state diagram, the message PMA_UNITDATA.request is issued concurrently with symb_timer_done.

40.3.3.4 Messages

PMA_UNITDATA.indication (rx_symb_vector)
: A signal sent by PMA Receive indicating that a vector of four quinary symbols is available in rx_symb_vector. (See 40.2.6.)

PMA_UNITDATA.request (tx_symb_vector)
: A signal sent to PMA Transmit indicating that a vector of four quinary symbols is available in tx_symb_vector. (See 40.2.5.)

PUDI
: Alias for PMA_UNITDATA.indication (rx_symb_vector).

PUDR
: Alias for PMA_UNITDATA.request (tx_symb_vector).

STD
: Alias for symb_timer_done.

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40.3.4 State diagrams

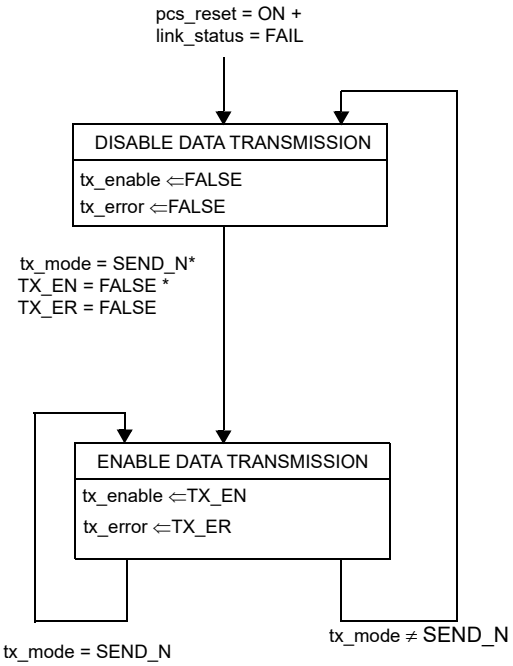

Figure 40–8—PCS Data Transmission Enabling state diagram

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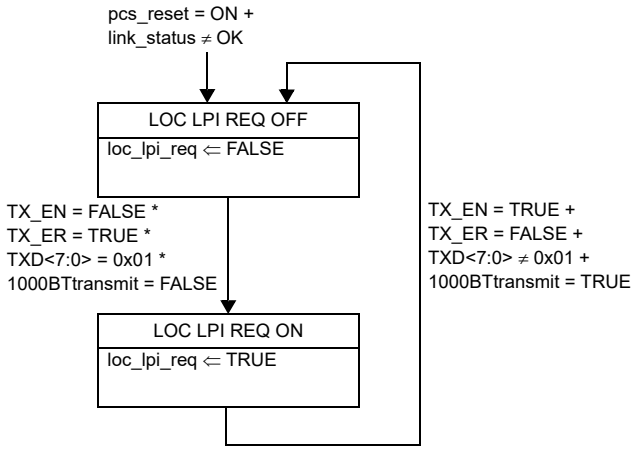

Figure 40–9—PCS Local LPI Request state diagram (optional)

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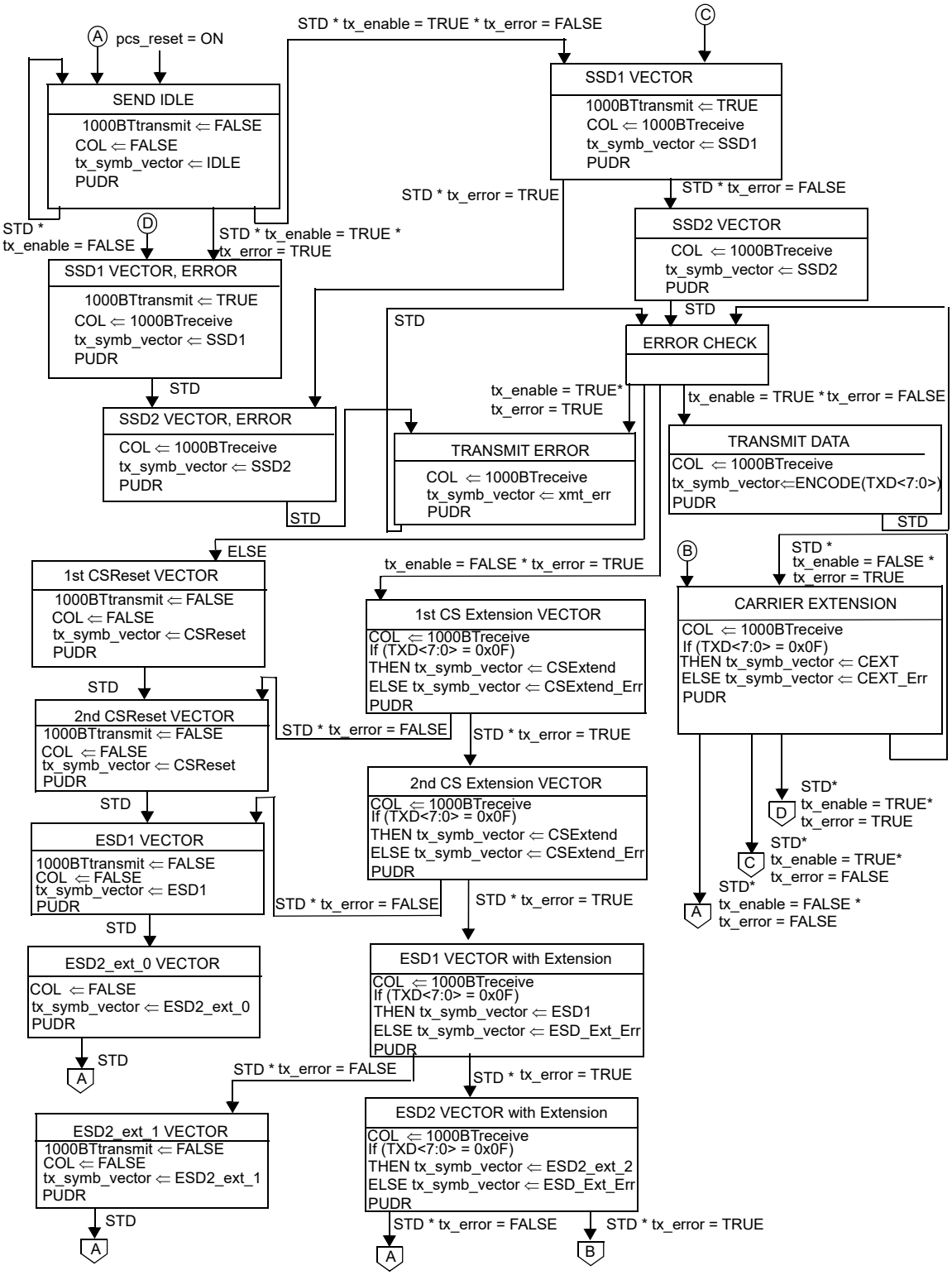

Figure 40–10—PCS Transmit state diagram

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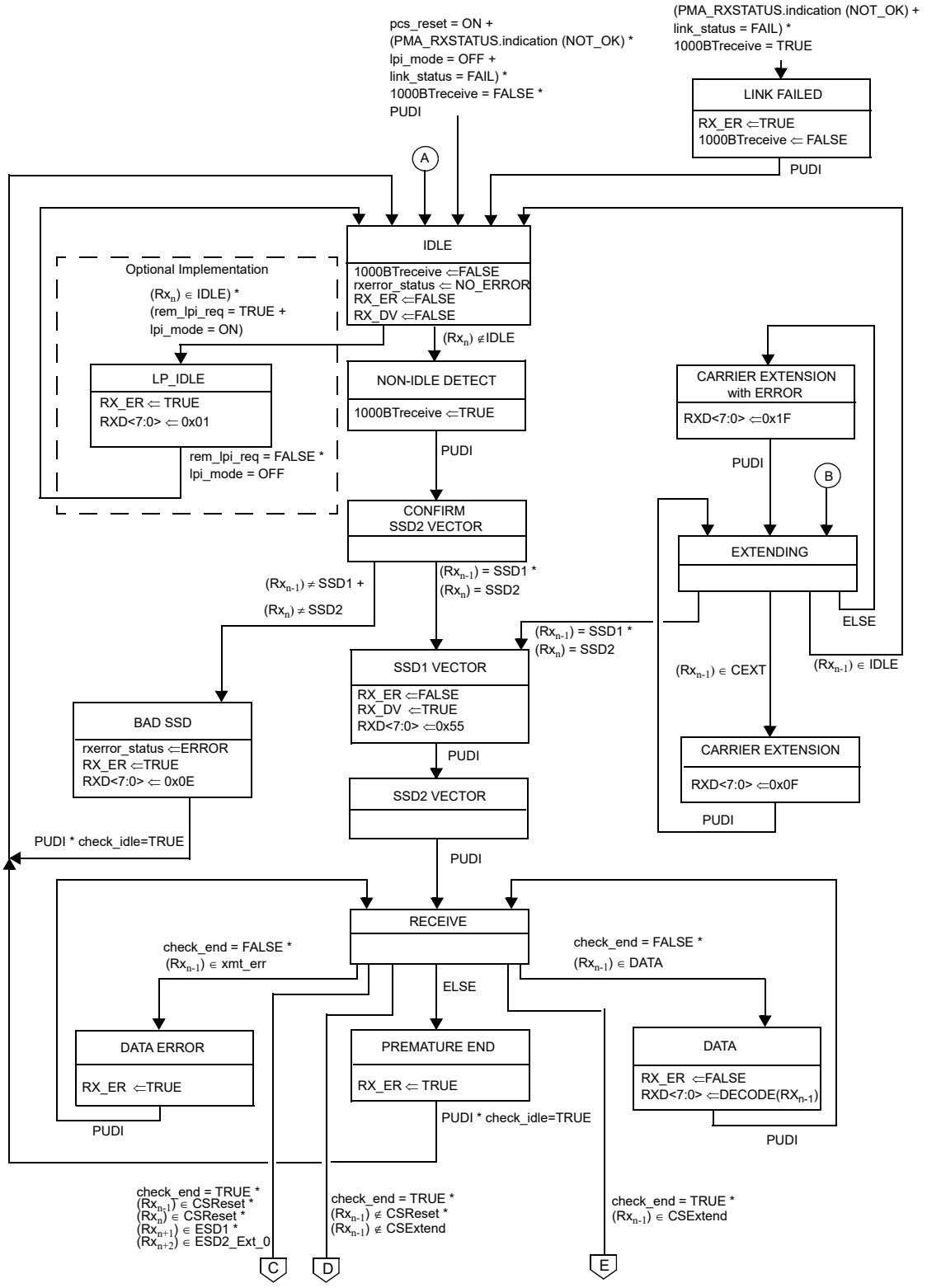

Figure 40–11a—PCS Receive state diagram, part a

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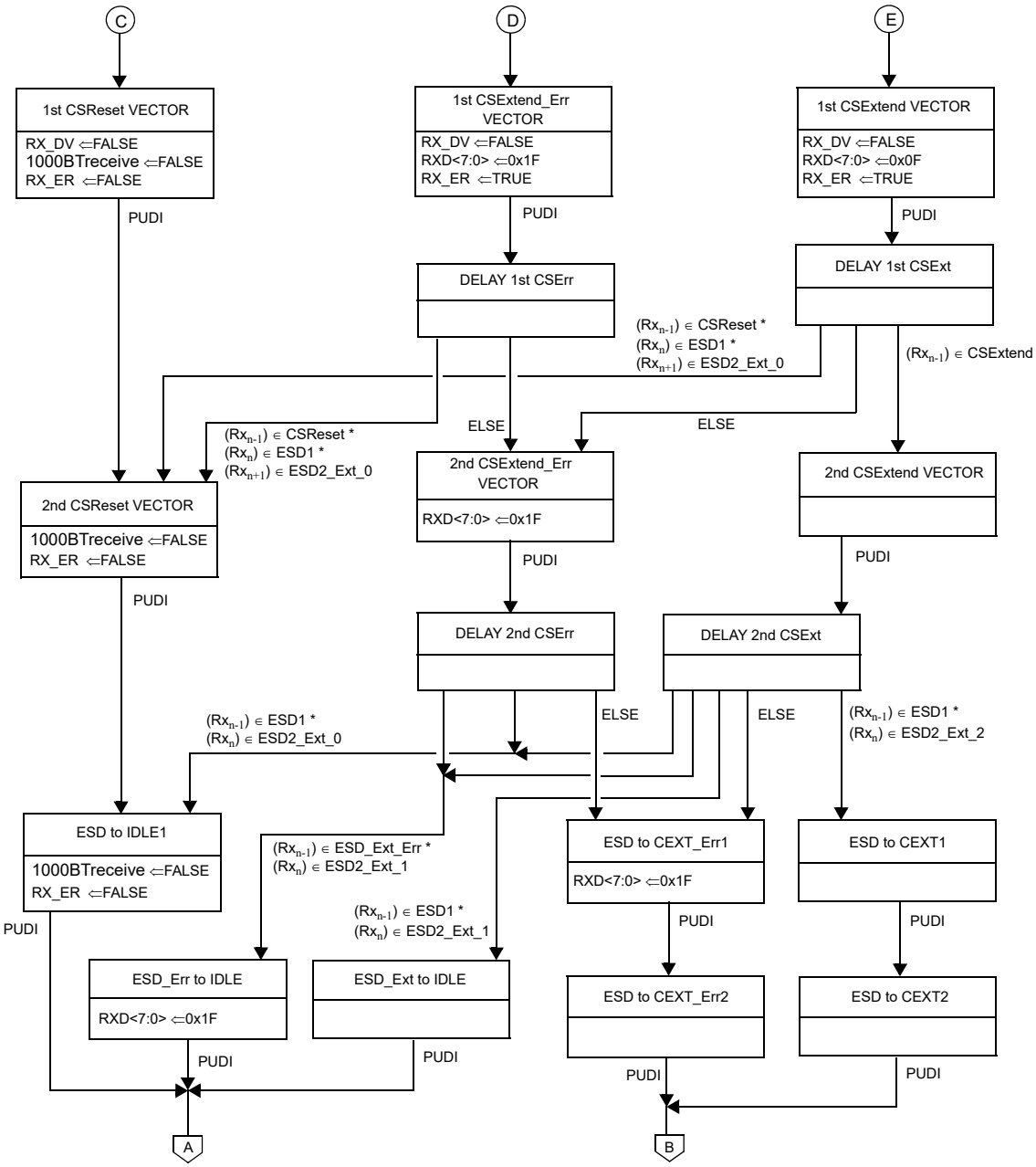

Figure 40–11b—PCS Receive state diagram, part b

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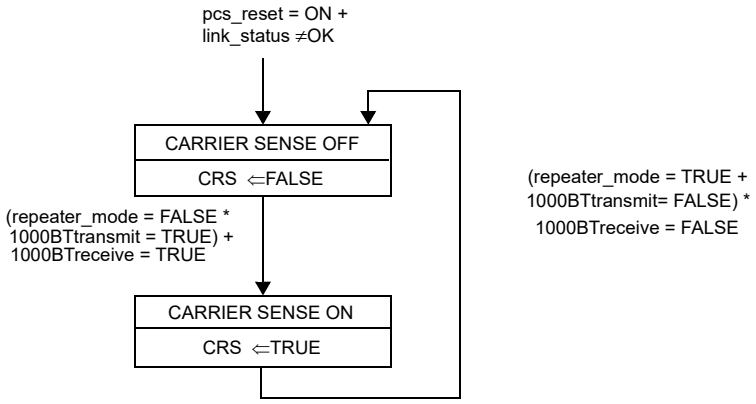

Figure 40–12—PCS Carrier Sense state diagram

40.3.4.1 Supplement to state diagram

Figure 40–13 reiterates the information shown in Figure 40–10 in timing diagram format. It is illustrative only. Time proceeds from left to right in the figure.

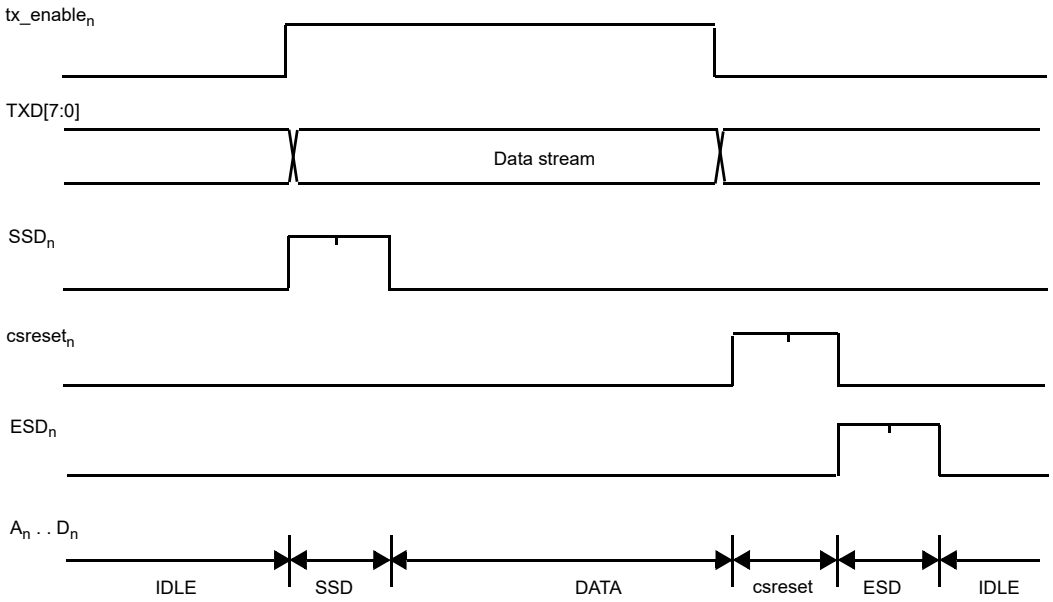

Figure 40–13—PCS sublayer to PMA timing

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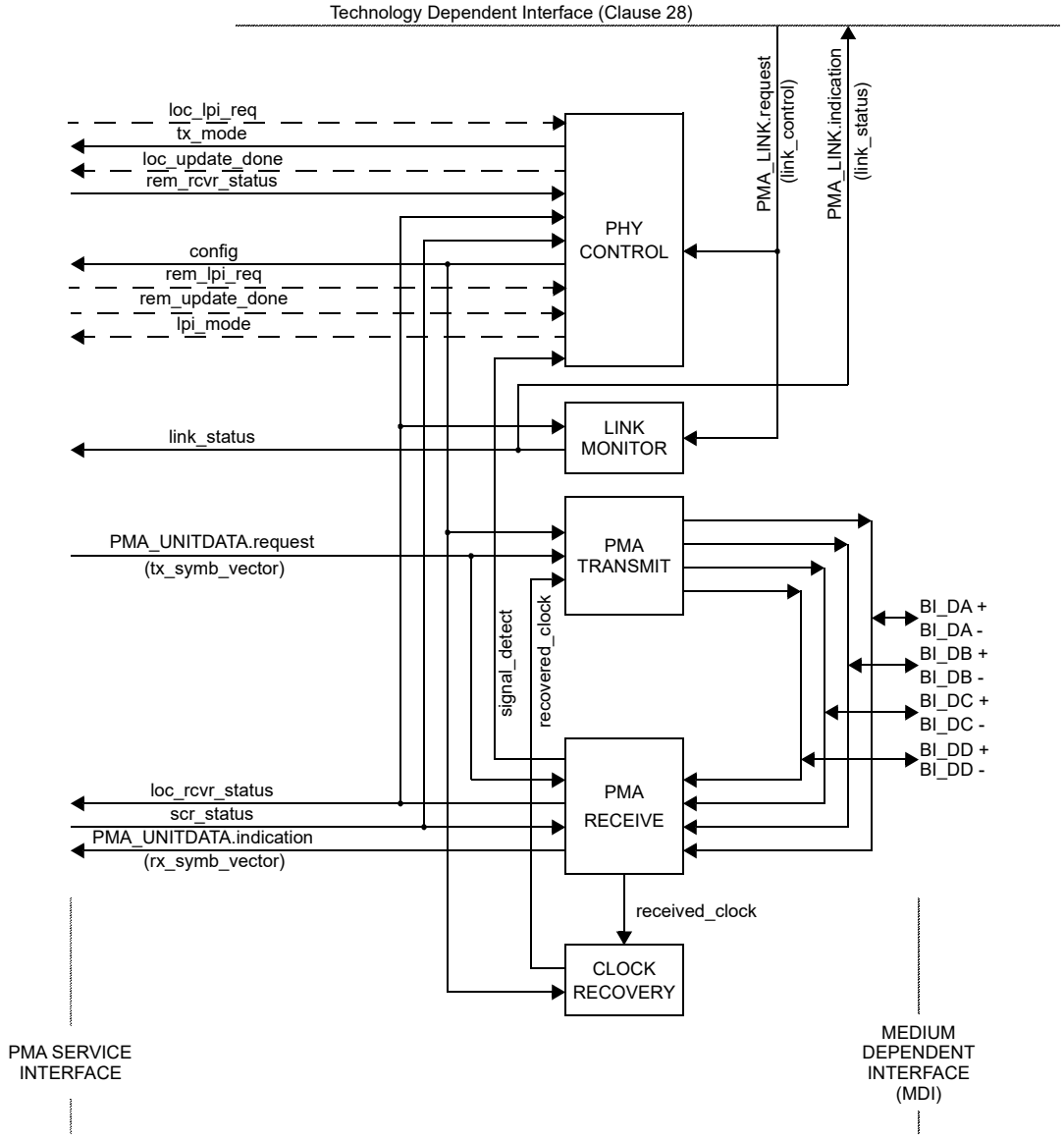
40.4 Physical Medium Attachment (PMA) sublayer

40.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 40.2.2 to the 1000BASE-T baseband medium, specified in 40.7.

The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 40.8.



NOTE 1—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

NOTE 2—Signals and functions shown with dashed lines are only required for the EEE capability.

Figure 40–14—PMA reference diagram

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40.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 40–14, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 40–14. The management interface and its functions are specified in Clause 22.

40.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power on (see 36.2.5.1.3)
b) The receipt of a request for reset from the management entity

PMA Reset sets pcs_reset=ON while any of the above reset conditions hold true. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

40.4.2.2 PMA Transmit function

The PMA Transmit function comprises four synchronous transmitters to generate four 5-level pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. PMA Transmit shall continuously transmit onto the MDI pulses modulated by the quinary symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC] and tx_symb_vector[BI_DD], respectively. The four transmitters shall be driven by the same transmit clock, TX_TCLK. The signals generated by PMA Transmit shall follow the mathematical description given in 40.4.3.1, and shall comply with the electrical specifications given in 40.6.

When the PMA_CONFIG.indication parameter config is MASTER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 40.6.1.2.5. When the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 40.4.2.6 while meeting the jitter requirements of 40.6.1.2.5.

40.4.2.3 PMA Receive function

The PMA Receive function comprises four independent receivers for quinary pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. PMA Receive contains the circuits necessary to both detect quinary symbol sequences from the signals received at the MDI over receive pairs BI_DA, BI_DB, BI_DC, and BI_DD and to present these sequences to the PCS Receive function. The signals received at the MDI are described mathematically in 40.4.3.2. The PMA shall translate the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DB into the PMA_UNITDATA.indication parameter rx_symb_vector with a symbol error ratio of less than 10^{-10} over a channel meeting the requirements of 40.7.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization, echo and crosstalk cancellation, and sequence estimation. The sequence of code-groups assigned to tx_symb_vector is needed to perform echo and self near-end crosstalk cancellation.

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The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, and estimation functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

40.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 40–16a and Figure 40–16b.

During Auto-Negotiation PHY Control is in the DISABLE 1000BASE-T TRANSMITTER state and the transmitters are disabled. When the Auto-Negotiation process asserts link_control=ENABLE, PHY Control enters the SLAVE SILENT state. Upon entering this state, the maxwait timer is started and PHY Control forces transmission of zeros by setting tx_mode=SEND_Z. The transition out of the SLAVE SILENT state depends on whether the PHY is operating in MASTER or SLAVE mode. In MASTER mode, PHY Control transitions immediately to the TRAINING state. In SLAVE mode, PHY Control transitions to the TRAINING state only after the SLAVE PHY converges its decision feedback equalizer (DFE), acquires timing, and acquires its descrambler state, and sets scr_status=OK**.**

For the SLAVE PHY, the final convergence of the adaptive filter parameters is completed in the TRAINING state. The MASTER PHY performs all its receiver convergence functions in the TRAINING state. Upon entering the TRAINING state, the minwait_timer is started and PHY Control forces transmission into the idle mode by asserting tx_mode=SEND_I. After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter loc_rcvr_status. (See Sd_n[2] in 40.3.1.3.4.) The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr status. When the minwait_timer expires and the condition loc_rcvr_status=OK is satisfied, PHY Control transitions into either the SEND IDLE OR DATA state if rem_rcvr_status=OK or the SEND IDLE state if rem_rcvr_status=NOT_OK. On entry into either the SEND IDLE or SEND IDLE OR DATA states, the maxwait_timer is stopped and the minwait_timer is started.

The normal mode of operation corresponds to the SEND IDLE OR DATA state, where PHY Control asserts tx_mode=SEND_N and transmission of data over the link can take place. In this state, when no frames have to be sent, idle transmission takes place.

If unsatisfactory receiver operation is detected in the SEND IDLE OR DATA or SEND IDLE states (loc_rcvr_status=NOT_OK) and the minwait_timer has expired, transmission of the current frame is completed and PHY Control enters the SLAVE SILENT state. In the SEND IDLE OR DATA state, whenever a PHY that operates reliably detects unsatisfactory operation of the remote PHY (rem_rcvr_status=NOT_OK) and the minwait_timer has expired, it enters the SEND IDLE state where tx_mode=SEND_I is asserted and idle transmission takes place. In this state, encoding is performed with the parameter loc_rcvr_status=OK. As soon as the remote PHY signals satisfactory receiver operation (rem_rcvr_status=OK) and the minwait_timer has expired, the SEND IDLE OR DATA state is entered.

When the PHY supports the optional EEE capability, PHY Control will transition to the LPI mode in response to concurrent requests for LPI mode from the local PHY (loc_lpi_req = TRUE) and remote PHY (rem_lpi_req = TRUE).

Upon activation of the LPI mode, the PHY Control asserts tx_mode = SEND_I for a period of time defined by lpi_update_timer, which allows the remote PHY to prepare for cessation of transmission. When lpi_update_timer expires, PHY Control transitions to the POST_UPDATE state, signals to the remote PHY that is has completed the update by setting loc_update_done = TRUE, and starts the lpi_postupdate_timer. When lpi_postupdate_timer expires, PHY Control transitions to the WAIT_QUIET state. If there is a request to wake (loc_lpi_req = FALSE or rem_lpi_req = FALSE) while in the POST_UPDATE state, PHY Control

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will wait for confirmation that the remote PHY has completed the update (rem_update_done = TRUE) and is prepared for cessation of transmission before proceeding to the WAIT_QUIET state.

Upon entry into the WAIT_QUIET state, PHY Control asserts tx_mode = SEND_Z and transmission ceases. During the WAIT_QUIET and QUIET states, the PHY may deactivate transmit and receive functions in order to conserve energy. However, in the WAIT_QUIET state, the PHY shall be capable of correctly decoding rem_lpi_req. The PHY will remain in the QUIET state no longer than the time implied by lpi_quiet_timer.

When lpi_quiet_timer expires, the PHY initiates a wake sequence. The wake sequence begins with a transition to the WAKE state where the PHY will transmit (tx_mode = SEND_I) for the period lpi_waketx_timer and simultaneously start a parallel timer, lpi_wakemz_timer. Since it is likely that transmit circuits were deactivated while in the QUIET state, this transmission is not expected to be compliant 1000BASE-T signaling, but rather of sufficient quality and duration to be detected by the remote PHY receiver and initiate the wake sequence in the remote PHY.

Upon expiration of lpi_waketx_timer, the PHY will enter the WAKE_SILENT state and cease transmission (tx_mode = SEND_Z). The PHY will remain in the WAKE_SILENT state until lpi_wakemz_timer has expired, at which point it is assumed that the transmitter circuits have stabilized and compliant 1000BASE-T signaling can be transmitted. At this point the MASTER transitions to the WAKE_TRAINING state and transmits to the SLAVE PHY.

The remaining wake sequence is essentially an accelerated training mode sequence leading to entry into the UPDATE state.

Once scrambler synchronization is achieved, the incoming value of rem_lpi_req can be determined. If the LPI mode is no longer requested by either the local or remote PHY, then both PHYs return to the SEND IDLE OR DATA state and the normal mode of operation (tx_mode = SEND_N). If both PHYs continue to request the LPI mode, then both PHYs remain in the UPDATE state and continue to transmit for a time defined by lpi_update_timer. This time is intended to allow the remote PHY to refresh its receiver state (e.g., timing recovery, adaptive filter coefficients) and thereby track long-term variation in the timing of the link or the underlying channel characteristics. If lpi_update_timer expires and both PHYs continue to request the LPI mode, then the PHY transitions to the POST_UPDATE state.

PHY Control may force the transmit scrambler state to be initialized to an arbitrary value by requesting the execution of the PCS Reset function defined in 40.3.1.1.

40.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel typically causes the PMA’s clients to suspend normal operation.

The Link Monitor function shall comply with the state diagram of Figure 40–17.

Upon power on, reset, or release from power down, the Auto-Negotiation algorithm sets link_control=SCAN_FOR_CARRIER and, during this period, sends fast link pulses to signal its presence to a remote station. If the presence of a remote station is sensed through reception of fast link pulses, the Auto-Negotiation algorithm sets link_control=DISABLE and exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. If the presence of a remote 1000BASE-T station is established, the Auto-Negotiation algorithm permits full operation by setting link_control=ENABLE. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

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40.4.2.6 Clock Recovery function

The Clock Recovery function couples to all four receive pairs. It may provide independent clock phases for sampling the signals on each of the four pairs.

The Clock Recovery function shall provide clocks suitable for signal sampling on each line so that the symbol error ratio indicated in 40.4.2.3 is achieved. The received clock signal has to be stable and ready for use when training has been completed (loc_rcvr_status=OK). The received clock signal is supplied to the PMA Transmit function by received_clock.

40.4.3 MDI

Communication through the MDI is summarized in 40.4.3.1 and 40.4.3.2.

40.4.3.1 MDI signals transmitted by the PHY

The quinary symbols to be transmitted by the PMA on the four pairs BI_DA, BI_DB, BI_DC, and BI_DD are denoted by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively. The modulation scheme used over each pair is 5-level Pulse Amplitude Modulation. PMA Transmit generates a pulse-amplitude modulated signal on each pair in the following form:

$$s(t) = \sum_k a_k h_1(t - kT)$$

In the above equation, a_k represents the quinary symbol from the set {2, 1, 0, –1, –2} to be transmitted at time kT, and $h_1(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 40.6.

40.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise as follows:

$$r(t) = \sum_k a_k h_2(t - kT) + w(t)$$

In this equation, $h_2(t)$ denotes the impulse response of the overall channel between the transmit symbol source and the receive MDI and $w(t)$ is a term that represents the contribution of various noise sources. The four signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD shall be processed within the PMA Receive function to yield the quinary received symbols rx_symb_vector[BI_DA], rx_symb_vector[BI_DB], rx_symb_vector[BI_DC], and rx_symb_vector[BI_DD].

40.4.4 Automatic MDI/MDI-X Configuration

Automatic MDI/MDI-X Configuration is intended to eliminate the need for crossover cables between similar devices. Implementation of an automatic MDI/MDI-X configuration is optional for 1000BASE-T devices. If an automatic configuration method is used, it shall comply with the following specifications. The assignment of pin-outs for a 1000BASE-T crossover function cable is shown in Table 40–12 in 40.8.

40.4.4.1 Description of Automatic MDI/MDI-X state diagram

The Automatic MDI/MDI-X state diagram facilitates switching the BI_DA(C)+ and BI_DA(C)– with the BI_DB(D)+ and BI_DB(D)– signals respectively prior to the auto-negotiation mode of operation so that FLPs can be transmitted and received in compliance with Clause 28 Auto-Negotiation specifications. The

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correct polarization of the crossover circuit is determined by an algorithm that controls the switching function. This algorithm uses an 11-bit linear feedback shift register (LFSR) to create a pseudo-random sequence that each end of the link uses to determine its proposed configuration. Upon making the selection to either MDI or MDI-X, the node waits for a specified amount of time while evaluating its receive channel to determine whether the other end of the link is sending link pulses or PHY-dependent data. If link pulses or PHY-dependent data are detected, it remains in that configuration. If link pulses or PHY-dependent data are not detected, it increments its LFSR and makes a decision to switch based on the value of the next bit. The state diagram does not move from one state to another while link pulses are being transmitted.

40.4.4.2 Pseudo-random sequence generator

One possible implementation of the pseudo-random sequence generator using a linear-feedback shift register is shown in Figure 40–15. The bits stored in the shift register delay line at time n are denoted by S[10:0]. At each sample period, the shift register is advanced by one bit and one new bit represented by S[0] is generated. Switch control is determined by S[10].

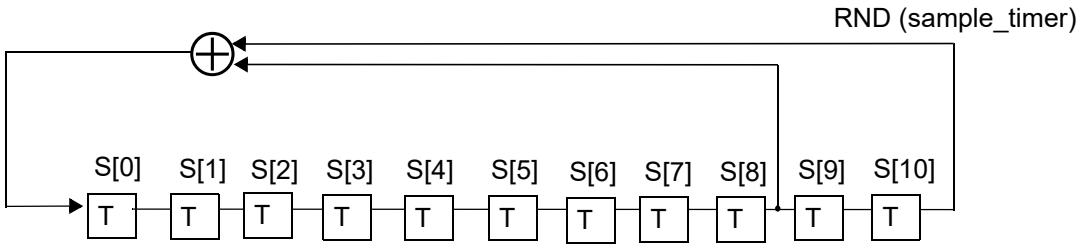

Figure 40–15—Automatic MDI/MDI-X linear-feedback shift register

40.4.5 State variables

40.4.5.1 State diagram variables

config
: The PMA shall generate this variable continuously and pass it to the PCS via the PMA_CONFIG.indication primitive.

  Values: MASTER or SLAVE

link_control
: This variable is defined in 28.2.6.2.

Link_Det
: This variable indicates linkpulse = true or link_status = READY or OK has occurred at the receiver since the last time sample_timer has been started.

  Values: TRUE: linkpulse = true or link_status = READY or OK has occurred since the last time sample_timer has been started.

  FALSE: otherwise

linkpulse
: This variable is defined in 28.2.6.3.

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link_status
: This variable is defined in 28.2.6.1.

loc_rcvr_status
: Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY.

Values: OK: The receive link for the local PHY is operating reliably.
NOT_OK: Operation of the receive link for the local PHY is unreliable.

MDI_Status
: This variable defines the condition of the Automatic MDI/MDI-X physical connection.

Values: MDI: The BI_DA, BI_DB, BI_DC, and BI_DD pairs follow the connections as described in the MDI column of Table 40–12.

MDI-X: The BI_DA, BI_DB, BI_DC, and BI_DD pairs follow the connections as described in the MDI-X column of Table 40–12.

pma_reset
: Allows reset of all PMA functions.

Values: ON or OFF

Set by: PMA Reset

rem_rcvr_status
: Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not.

Values: OK: The receive link for the remote PHY is operating reliably.

NOT_OK: Reliable operation of the receive link for the remote PHY is not detected.

RND (sample_timer)
: This variable is defined as bit S[10] of the LSFR described in 40.4.4.2

scr_status
: The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.

Values: OK: The descrambler has achieved synchronization.

NOT_OK: The descrambler is not synchronized. Note that when the PHY supports the optional EEE capability and signal_detect is FALSE, scr_status is set to NOT_OK.

T_Pulse
: This variable indicates that a linkpulse is being transmitted to the MDI.

Values: TRUE: Pulse being transmitted to the MDI

FALSE: Otherwise

tx_enable
: The tx_enable parameter generated by PCS Transmit as specified in Figure 40–8.

Values: TRUE or FALSE as per 40.3.3.1.

tx_mode
: PCS Transmit sends code-groups according to the value assumed by this variable.

Values: SEND_N: This value is continuously asserted when transmission of sequences of code-groups representing a GMII data stream, control information, or idle mode is to take place.

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SEND_I: This value is continuously asserted when transmission of sequences of code-groups representing the idle mode is to take place.

SEND_Z: This value is asserted when transmission of zero code-groups is to take place.

The following state variables are only required for the optional EEE capability:

loc_lpi_req

The loc_lpi_req variable is set by the PCS Local LPI Request function and indicates whether or not the local PHY is requested to enter the LPI mode. It is passed to the PMA PHY Control function via the PMA_LPIREQ.request primitive. In the absence of the optional EEE capability, the PHY operates as if the value of this variable is FALSE.

Values: TRUE: "Assert LPI" is present at the GMII.
FALSE: "Assert LPI" is not present at the GMII.

loc_udpate_done

The loc_update_done variable is generated by the PMA PHY Control function and indicates whether or not the local PHY has completed the update of its receiver state. It is passed to the PCS Transmit function via the PMA_UPDATE.indication primitive. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.

Values: TRUE: The PHY has completed the current update.
FALSE: The PHY is ready for the next update or the current update is still in progress.

lpi_mode

The lpi_mode variable is generated by the PMA PHY Control function and indicates whether or not the local PHY has entered the LPI mode. It is passed to the PCS Receive function via the PMA_LPIMODE.indication primitive. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is OFF.

Values: ON: The PHY is operating in LPI mode.
OFF: The PHY is in normal operation.

rem_lpi_req

The rem_lpi_req variable is generated by the PCS Receive function and indicates whether or not the remote PHY is requesting entry into LPI mode. It is passed to the PMA PHY Control function via the PMA_REMLPIREQ.request primitive. In the absence of the optional EEE capability, the PHY operates as if the value of this variable is FALSE.

Values: TRUE: LPI is encoded in the received symbols.
FALSE: LPI is not encoded in the received symbols.

rem_update_done

The rem_update_done variable is generated by the PCS Receive function and indicates whether or not the remote PHY has completed the update of its receiver state. It is passed to the PMA PHY Control function via the PMA_REMUPDATE.request primitive. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.

Values: TRUE: The remote PHY has completed the current update.
FALSE: The remote PHY is ready for the next update or the current update is still in progress.

signal_detect

The signal_detect variable is set by the PMA Receive function and indicates the presence of a signal at the MDI, as defined in 40.6.1.3.5.

Values: TRUE: There is a signal present at the MDI.
FALSE: There is no signal present at the MDI.

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40.4.5.2 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where “stop timer” is asserted.

A_timer

An asynchronous (to the Auto-Crossover state diagram) free-running timer that provides for a relatively arbitrary reset of the state diagram to its initial state. This timer is used to reduce the probability of a lock-up condition where both nodes have the same identical seed initialization at the same point in time.

Values: The condition A_timer_done becomes true upon timer expiration.

Duration: This timer shall have a period of 1.3 s ± 25%.

Initialization of A_timer is implementation specific.

maxwait_timer

A timer used to limit the amount of time during which a receiver dwells in the SLAVE SILENT and TRAINING states. The timer shall expire 750 ms ± 10 ms if config = MASTER or 350 ms ± 5 ms if config = SLAVE. This timer is used jointly in the PHY Control and Link Monitor state diagrams. The maxwait_timer is tested by the Link Monitor to force link_status to be set to FAIL if the timer expires and loc_rcvr_status is NOT_OK. See Figure 40–16a.

minwait_timer

A timer used to determine the minimum amount of time the PHY Control stays in the TRAINING, SEND IDLE, or DATA states. The timer shall expire 1 μs ± 0.1μs after being started.

sample_timer

This timer provides a long enough sampling window to ensure detection of Link Pulses or link_status, if they exist at the receiver.

Values: The condition sample_timer_done becomes true upon timer expiration.

Duration: This timer shall have a period of 62 ms ± 2 ms.

stabilize_timer

A timer used to control the minimum time that loc_rcvr_status has to be OK before a transition to Link Up can occur. The timer shall expire 1 μs ± 0.1 μs after being started.

The following timers are only required for the optional EEE capability:

lpi_link_fail_timer

This timer defines the maximum time the PHY allows between entry into the WAKE state and subsequent entry into the UPDATE or SEND IDLE OR DATA states before forcing the link to restart.

Values: The condition lpi_link_fail_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 90 μs and 110 μs.

lpi_postupdate_timer

This timer defines the maximum time the PHY dwells in the POST_UPDATE state before proceeding to the WAIT_QUIET state.

Values: The condition lpi_postupdate_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 2.0 μs and 3.2 μs.

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lpi_quiet_timer

This timer defines the maximum time the PHY remains quiet before initiating transmission to refresh the remote PHY.

Values: The condition lpi_quiet_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 20 ms and 24 ms.

lpi_waitwq_timer

This timer defines the maximum time the PHY dwells in the WAIT_QUIET state before forcing the link to restart.

Values: The condition lpi_waitwq_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 10 µs and 12 µs.

lpi_wake_timer

This timer defines the expected time for the PHY to transition from the LPI mode to normal operation.

Values: The condition lpi_wake_timer_done becomes true upon timer expiration. For each transition of lpi_wake_timer_done from false to true, the wake error counter (see 40.5.1.1) shall be incremented.
Duration: This timer shall have a period that does not exceed 16.5 µs.

lpi_waketx_timer

This timer defines the time the PHY transmits to ensure detection by the remote PHY receiver and trigger an exit from the low power state.

Values: The condition lpi_waketx_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 1.2 µs and 1.4 µs.

lpi_wakemz_timer

This timer defines the time allowed for the PHY transmitter to achieve compliant operation following activation.

Values: The condition lpi_wakemz_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 4.25 µs and 5.00 µs.

lpi_update_timer

This timer defines the time the PHY transmits to facilitate a refresh of the remote PHY receiver.

Values: The condition lpi_update_timer_done becomes true upon timer expiration.
Duration: For a PHY configured as the MASTER, this timer shall have a period between 0.23 ms and 0.25 ms. For a PHY configured as the SLAVE, this timer shall have a period between 0.18 ms and 0.20 ms.

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40.4.6 State Diagrams

40.4.6.1 PHY Control state diagram

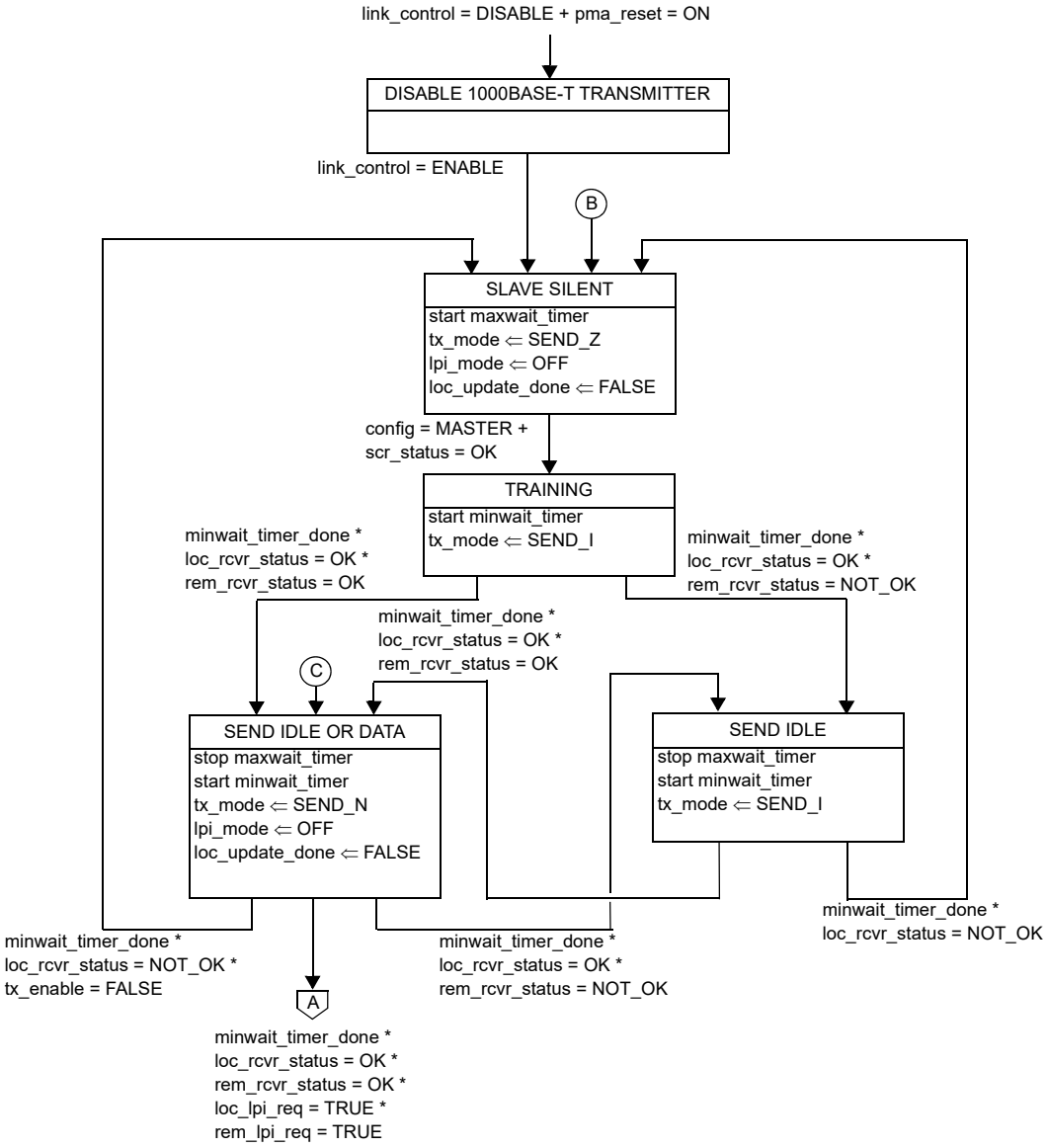

Figure 40–16a—PHY Control state diagram, part a

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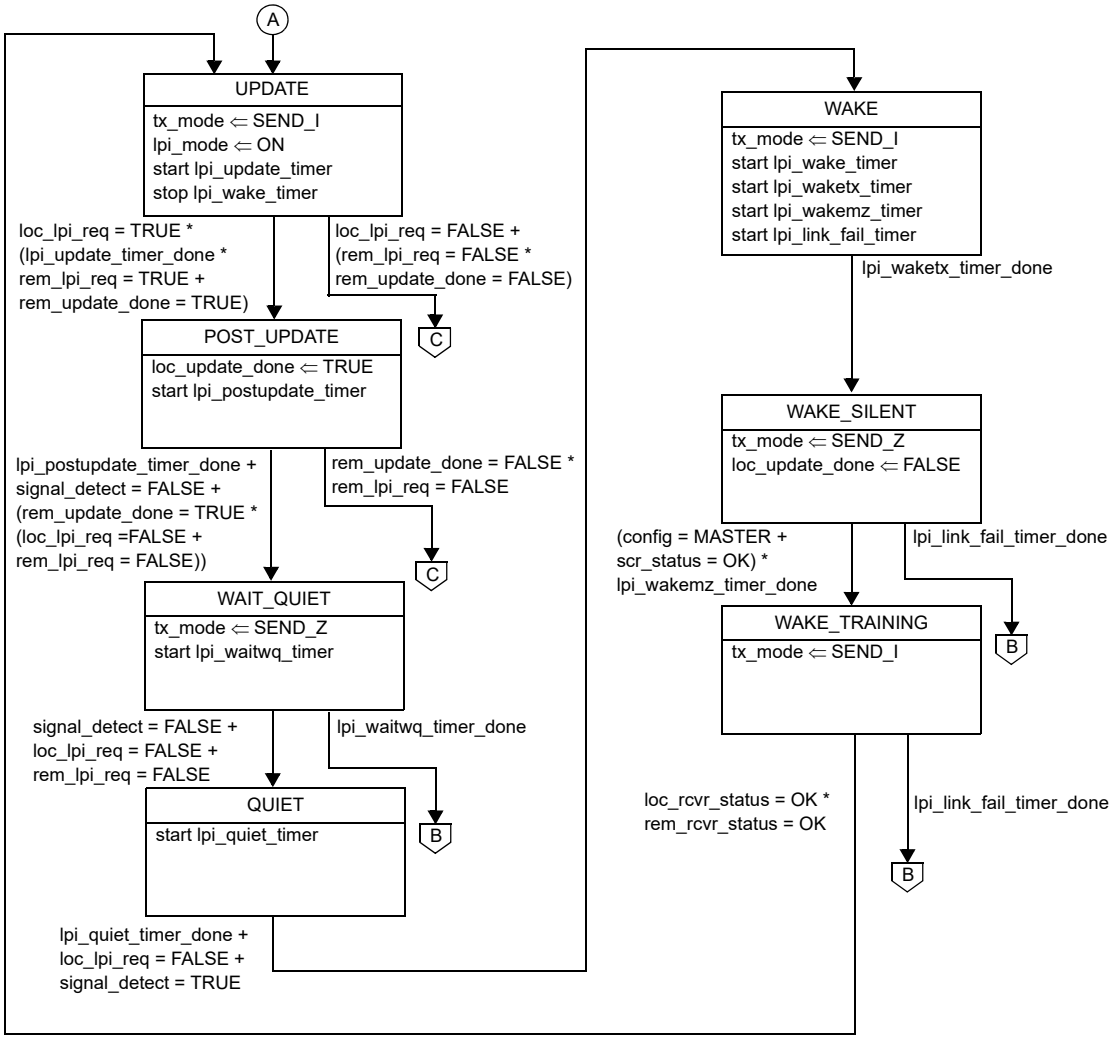

Figure 40–16b—PHY Control state diagram, part b (optional)

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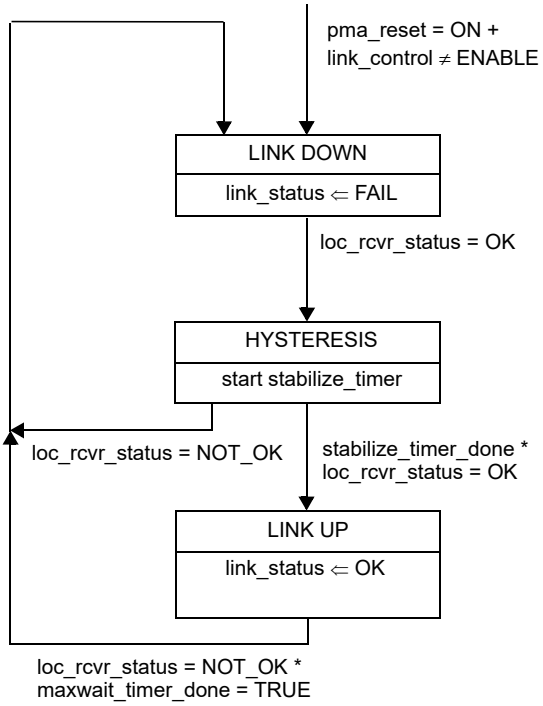
40.4.6.2 Link Monitor state diagram



NOTE 1—maxwait_timer is started in PHY Control state diagram (see Figure 40–16a).
NOTE 2—The variables link_control and link_status are designated as link_control_(1GigT) and link_status_(1GigT), respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

Figure 40–17—Link Monitor state diagram

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40.4.6.2.1 Auto Crossover state diagram

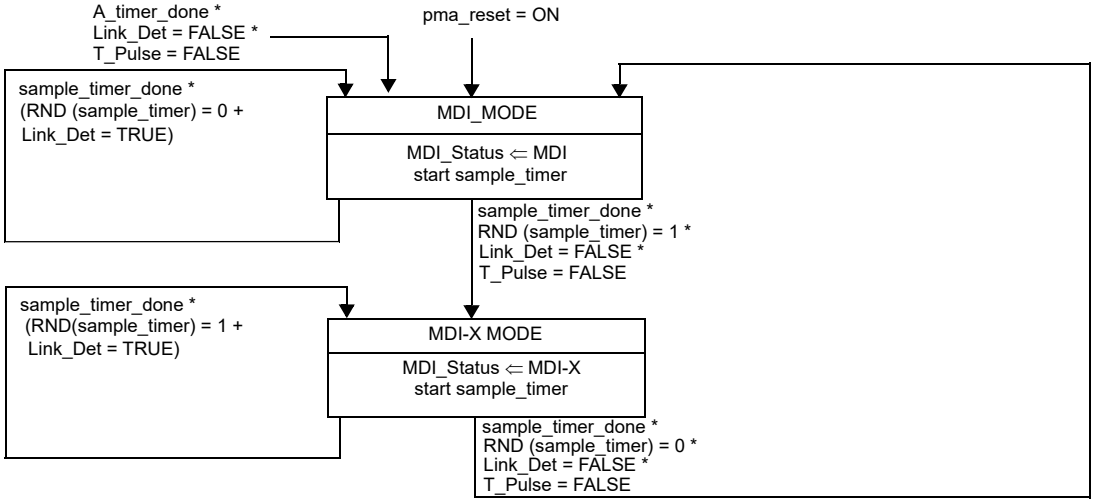

Figure 40–18—Auto Crossover state diagram

40.5 Management interface

1000BASE-T makes extensive use of the management functions provided by the MII Management Interface (see 22.2.4), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28).

40.5.1 Support for Auto-Negotiation

All 1000BASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE.

Auto-Negotiation is performed as part of the initial set-up of the link, and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-negotiation signaling is used for the following two primary purposes for 1000BASE-T:

a) To negotiate that the PHY is capable of supporting 1000BASE-T half duplex or full duplex transmission.
b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.
c) To negotiate EEE capabilities as specified in 28C.12.

This relationship is necessary for establishing the timing control of each PHY. The 1000BASE-T MASTER PHY is clocked from a local source. The SLAVE PHY uses loop timing where the clock is recovered from the received data stream.

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40.5.1.1 1000BASE-T use of registers during Auto-Negotiation

A 1000BASE-T PHY shall use the management register definitions and values specified in Table 40–3.

Table 40–3—1000BASE-T Registers

Register	Bit	Name	Description	Type [a]
0	0.15:0	MII control register	Defined in 28.2.4.1.1	RO
1	1.15:0	MII status register	Defined in 28.2.4.1.2	RO
4	4.15:0	Auto-Negotiation advertisement register	The Selector Field (4.4:0) is set to the appropriate code as specified in Annex 28A. The Technology Ability Field bits 4.12:5 are set to the appropriate code as specified in Annexes 28B and 28D. Bit 4.15 is set to logical one to indicate the desired exchange of Next Pages describing the gigabit extended capabilities.	R/W
5	5.15:0	Auto-Negotiation link partner ability register	Defined in 28.2.4.1.4. 1000BASE-T implementations do not use this register to store Auto-Negotiation Link Partner Next Page data.	RO
6	6.15:0	Auto-Negotiation expansion register	Defined in 28.2.4.1.5	RO
7	7.15:0	Auto-Negotiation Next Page transmit register	Defined in 28.2.4.1.6	R/W
8	8.15:0	Auto-Negotiation link partner Next Page register	Defined in 28.2.4.1.8	RO
9	9.15:13	Test mode bits	Transmitter test mode operations are defined by bits 9.15:13 as described in 40.6.1.1.2 and Table 40–7. The default values for bits 9.15:13 are all zero.	R/W
9	9.12	MASTER-SLAVE Manual Config Enable	1=Enable MASTER-SLAVE Manual configuration value 0=Disable MASTER-SLAVE Manual configuration value Default bit value is 0.	R/W
9	9.11	MASTER-SLAVE Config Value	1=Configure PHY as MASTER during MASTER-SLAVE negotiation, only when 9.12 is set to logical one. 0=Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when 9.12 is set to logical one. Default bit value is 0.	R/W
9	9.10	Port type	Bit 9.10 is to be used to indicate the preference to operate as MASTER (multiport device) or as SLAVE (single-port device) if the MASTER-SLAVE Manual Configuration Enable bit, 9.12, is not set. Usage of this bit is described in 40.5.2. 1=Multiport device 0=single-port device	R/W
9	9.9	1000BASE-T Full Duplex	1 = Advertise PHY is 1000BASE-T full duplex capable. 0 = Advertise PHY is not 1000BASE-T full duplex capable.	R/W
9	9.8	1000BASE-T Half Duplex	1 = Advertise PHY is 1000BASE-T half duplex capable. 0 = Advertise PHY is not 1000BASE-T half duplex capable.	R/W
9	9.7:0	Reserved	Write as 0, ignore on read.	R/W

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Table 40–3—1000BASE-T Registers *(continued)*

Register	Bit	Name	Description	Type [a]
10	10.15	MASTER-SLAVE configuration fault	Configuration fault, as well as the criteria and method of fault detection, is PHY specific. The MASTER-SLAVE Configuration Fault bit will be cleared each time register 10 is read via the management interface and will be cleared by a 1000BASE-T PMA reset. This bit will self clear on Auto-Negotiation enable or Auto-Negotiation complete.This bit will be set if the number of failed MASTER-SLAVE resolutions reaches 7. For l000BASE-T, the fault condition will occur when both PHYs are forced to be MASTERs or SLAVEs at the same time using bits 9.12 and 9.11. Bit 10.15 should be set via the MASTER-SLAVE Configuration Resolution function described in 40.5.2. 1 = MASTER-SLAVE configuration fault detected 0 = No MASTER-SLAVE configuration fault detected	RO/LH/SC
10	10.14	MASTER-SLAVE configuration resolution	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	RO
10	10.13	Local Receiver Status	1 = Local Receiver OK (loc_rcvr_status=OK) 0 = Local Receiver not OK (loc_rcvr_status=NOT_OK) Defined by the value of loc_rcvr_status as per 40.4.5.1.	RO
10	10.12	Remote Receiver Status	1 = Remote Receiver OK (rem_rcvr_status=OK) 0 = Remote Receiver not OK (rem_rcvr_status=NOT_OK) Defined by the value of rem_rcvr_status as per 40.4.5.1.	RO
10	10.11	LP 1000T FD	1 = Link Partner is capable of 1000BASE-T full duplex 0 = Link Partner is not capable of 1000BASE-T full duplex This bit is guaranteed to be valid only when the Page received bit (6.1) has been set to 1.	RO
10	10.10	LP 1000T HD	1 = Link Partner is capable of 1000BASE-T half duplex 0 = Link Partner is not capable of 1000BASE-T half duplex This bit is guaranteed to be valid only when the Page received bit (6.1) has been set to 1.	RO
10	10.9:8	Reserved	Reserved	RO
10	10.7:0	Idle Error Count	Bits 10.7:0 indicate the Idle Error count, where 10.7 is the most significant bit. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE.indication is equal to SEND_N (indicating that both local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rxerror_status is equal to ERROR. These bits are reset to all zeros when the error count is read by the management function or upon execution of the PCS Reset function and are to be held at all ones in case of overflow (see 30.5.1.1.13).	RO/SC
15	15.15:12	Extended status register	See 22.2.4.4	RO

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Table 40–3—1000BASE-T Registers *(continued)*

Register	Bit	Name	Description	Type [a]
3.0[b]	3.0.10	Clock stop enable	Defined in 45.2.3.1.4. When the PHY supports the optional EEE capability, it may stop the derived GMII receive clock while it is signaling LPI in the receive direction. If this bit is set to 1, then the PHY may stop the receive GMII clock while it is signaling LPI; otherwise it keeps the clock active.	R/W
3.1	3.1.11	Transmit LPI received	Defined in 45.2.3.2.1.	RO/LH
3.1	3.1.10	Receive LPI received	Defined in 45.2.3.2.2.	RO/LH
3.1	3.1.9	Transmit LPI indication	Defined in 45.2.3.2.3.	RO
3.1	3.1.8	Receive LPI indication	Defined in 45.2.3.2.4.	RO
3.1	3.1.6	Clock stop capable	Defined in 45.2.3.2.6. When the PHY supports the optional EEE capability, this bit may be set to 1 to allow the MAC to stop the GMII clock while it is signaling LPI in the transmit direction. If this bit is 0, then the MAC keeps the clock active.	RO
3.20	3.20.2	1000BASE-T EEE supported	If the local device supports the optional EEE capability for 1000BASE-T, this bit is set to 1.	RO
3.22	3.22.15:0	EEE wake error counter	This counter is incremented for each transition of lpi_wake_timer_done from FALSE to TRUE (see 40.4.5.2).	RO, NR
7.60	7.60.2	1000BASE-T EEE advertisement	If the local device supports the optional EEE capability for 1000BASE-T and EEE is desired, this bit is set to 1.	R/W
7.61	7.61.2	LP 1000BASE-T EEE advertisement	If the link partner supports the optional EEE capability for 1000BASE-T and EEE is desired, this bit is set to 1.	RO

[a] R/W = Read/Write, RO = Read only, SC = Self-clearing, LH = Latching high.
[b] This register resides in the Clause 45 management space and is designated by the format M.R.B where M is the MDIO manageable device address (MMD), R is the register address, and B is the bit.

40.5.1.2 1000BASE-T Auto-Negotiation page use

1000BASE-T PHYs shall exchange one Auto-Negotiation Base Page, a 1000BASE-T formatted Next Page, and two 1000BASE-T Unformatted Next Pages in sequence, without interruption, as specified in Table 40–4. Additional Next Pages can be exchanged as described in Annex 40C.

Note that the Acknowledge 2 bit is not utilized and has no meaning when used for the 1000BASE-T message page exchange.

When the PHY supports the optional EEE capability, a 1000BASE-T PHY shall exchange an additional formatted Next Page and Unformatted Next Page in sequence, without interruption, as specified in Table 40–4.

40.5.1.3 Sending Next Pages

Implementers who do not wish to send additional Next Pages (i.e., Next Pages in addition to those required to perform PHY configuration as defined in this clause) can use Auto-Negotiation as defined in Clause 28 and the Next Pages defined in 40.5.1.2. Implementers who wish to send additional Next Pages are advised to consult Annex 40C.

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Table 40–4—1000BASE-T Base and Next Pages bit assignments

Bit	Bit definition	Register location
Base Page		
D15	1 (to indicate that Next Pages follow)	
D14:D1	As specified in 28.2.1.2	Management register 4
PAGE 0 (Message Next Page)		
M10:M0	8	
PAGE 1 (Unformatted Next Page)		
U10:U5	Reserved transmit as 0	
U4	1000BASE-T half duplex (1 = half duplex and 0 = no half duplex)	GMII register 9.8 (MASTER-SLAVE Control register)
U3	1000BASE-T full duplex (1 = full duplex and 0 = no full duplex)	GMII register 9.9 (MASTER-SLAVE Control register)
U2	1000BASE-T port type bit (1 = multiport device and 0 = single-port device)	GMII register 9.10 (MASTER-SLAVE Control register)
U1	1000BASE-T MASTER-SLAVE Manual Configuration value (1 = MASTER and 0 = SLAVE.) This bit is ignored if 9.12 = 0.	GMII register 9.11 (MASTER-SLAVE Control register)
U0	1000BASE-T MASTER-SLAVE Manual Configuration Enable (1 = Manual Configuration Enable.) This bit is intended to be used for manual selection in a particular MASTER-SLAVE mode and is to be used in conjunction with bit 9.11.	GMII register 9.12 (MASTER-SLAVE Control register)
PAGE 2 (Unformatted Next Page)		
U10	1000BASE-T MASTER-SLAVE Seed Bit 10 (SB10) (MSB)	MASTER-SLAVE Seed Value (10:0)
U9	1000BASE-T MASTER-SLAVE Seed Bit 9 (SB9)	
U8	1000BASE-T MASTER-SLAVE Seed Bit 8 (SB8)	
U7	1000BASE-T MASTER-SLAVE Seed Bit 7 (SB7)	
U6	1000BASE-T MASTER-SLAVE Seed Bit 6 (SB6)	
U5	1000BASE-T MASTER-SLAVE Seed Bit 5 (SB5)	
U4	1000BASE-T MASTER-SLAVE Seed Bit 4 (SB4)	
U3	1000BASE-T MASTER-SLAVE Seed Bit 3 (SB3)	
U2	1000BASE-T MASTER-SLAVE Seed Bit 2 (SB2)	
U1	1000BASE-T MASTER-SLAVE Seed Bit 1 (SB1)	
U0	1000BASE-T MASTER-SLAVE Seed Bit 0 (SB0)	
PAGE 3 (Message page)		
M10:M0	10	
PAGE 4 (Unformatted Next Page)		
U10:U3	As specified in 45.2.7.14.	
U2	1000BASE-T EEE (1 = EEE is supported for 1000BASE-T, 0 = EEE is not supported for 1000BASE-T)	Management register 7.60.2[a]
U1:U0	As specified in 45.2.7.14.	

[a]This register resides in the Clause 45 management space and is designated by the format M.R.B where M is the MDIO manageable device address (MMD), R is the register address, and B is the bit.

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40.5.2 MASTER-SLAVE configuration resolution

Since both PHYs that share a link segment are capable of being MASTER or SLAVE, a prioritization scheme exists to ensure that the correct mode is chosen. The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using Table 40–5 with the 1000BASE-T Technology Ability Next Page bit values specified in Table 40–4 and information received from the link partner. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown in the Arbitration state diagram (Figure 28–15.)

The following four equations are used to determine these relationships:

manual_MASTER = U0 * U1
manual_SLAVE = U0 * !U1
single-port device = !U0 * !U2,
multiport device = !U0 * U2

where

U0 is bit 0 of unformatted page 1,
U1 is bit 1 of unformatted page 1, and
U2 is bit 2 of unformatted page 1 (see Table 40–4).

A 1000BASE-T PHY is capable of operating either as the MASTER or SLAVE. In the scenario of a link between a single-port device and a multiport device, the preferred relationship is for the multiport device to be the MASTER PHY and the single-port device to be the SLAVE. However, other topologies may result in contention. The resolution function of Table 40–5 is defined to handle any relationship conflicts.

Table 40–5—1000BASE-T MASTER-SLAVE configuration resolution table

Local device type	Remote device type	Local device resolution	Remote device resolution
single-port device	multiport device	SLAVE	MASTER
single-port device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	manual_MASTER	SLAVE	MASTER
manual_SLAVE	multiport device	SLAVE	MASTER
multiport device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	single-port device	SLAVE	MASTER
multiport device	single-port device	MASTER	SLAVE
multiport device	manual_SLAVE	MASTER	SLAVE

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Table 40–5—1000BASE-T MASTER-SLAVE configuration resolution table *(continued)*

Local device type	Remote device type	Local device resolution	Remote device resolution
manual_MASTER	manual_SLAVE	MASTER	SLAVE
manual_MASTER	single-port device	MASTER	SLAVE
single-port device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	multiport device	MASTER	SLAVE
multiport device	multiport device	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.
single-port device	single-port device	The device with the higher SEED value is configured as MASTER, otherwise SLAVE	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.
manual_SLAVE	manual_SLAVE	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault
manual_MASTER	manual_MASTER	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault

The rationale for the hierarchy illustrated in Table 40–5 is straightforward. A 1000BASE-T multiport device has higher priority than a single-port device to become the MASTER. In the case where both devices are of the same type, e.g., both devices are multiport devices, the device with the higher MASTER-SLAVE seed bits (SB0...SB10), where SB10 is the MSB, shall become the MASTER and the device with the lower seed value shall become the SLAVE. In case both devices have the same seed value, both should assert link_status_1GigT=FAIL (as defined in 28.3.1) to force a new cycle through Auto-Negotiation. Successful completion of the MASTER-SLAVE resolution shall be treated as MASTER-SLAVE configuration resolution complete.

The method of generating a random or pseudorandom seed is left to the implementer. The generated random seeds should belong to a sequence of independent, identically distributed integer numbers with a uniform distribution in the range of 0 to 2^{11}– 2. The algorithm used to generate the integer should be designed to minimize the correlation between the number generated by any two devices at any given time. A seed counter shall be provided to track the number of seed attempts. The seed counter shall be set to zero at startup and shall be incremented each time a seed is generated. When MASTER-SLAVE resolution is complete, the seed counter shall be reset to 0 and bit 10.15 shall be set to logical zero. A MASTER-SLAVE resolution fault shall be declared if resolution is not reached after the generation of seven seeds.

The MASTER-SLAVE Manual Configuration Enable bit (control register bit 9.12) and the MASTER-SLAVE Config Value bit (control register bit 9.11) are used to manually set a device to become the MASTER or the SLAVE. In case both devices are manually set to become the MASTER or the SLAVE, this condition shall be flagged as a MASTER-SLAVE Configuration fault condition, thus the MASTER-SLAVE Configuration fault bit (status register bit 10.15) shall be set to logical one. The MASTER-SLAVE Configuration fault condition shall be treated as MASTER-SLAVE configuration resolution complete and link_status_1GigT shall be set to FAIL, because the MASTER-SLAVE relationship was not resolved. This will force a new cycle through Auto-Negotiation after the link_fail_inhibit_timer has expired. Determination of MASTER-SLAVE values occur on the entrance to the FLP LINK GOOD CHECK state (Figure 28–18) when the highest common denominator (HCD) technology is 1000BASE-T. The resulting MASTER-SLAVE value is used by the 1000BASE-T PHY control (40.4.2.4).

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If MASTER-SLAVE Manual Configuration is disabled (bit 9.12 is set to 0) and the local device detects that both the local device and the remote device are of the same type (either multiport device or single-port device) and that both have generated the same random seed, it generates and transmits a new random seed for MASTER-SLAVE negotiation by setting link_status to FAIL and cycling through the Auto-Negotiation process again.

The MASTER-SLAVE configuration process returns one of the three following outcomes:

a) *Successful:* Bit 10.15 of the 1000BASE-T Status Register is set to logical zero and bit 10.14 is set to logical one for MASTER resolution or for logical zero for SLAVE resolution. 1000BASE-T returns control to Auto_Negotiation (at the entrance to the FLP LINK GOOD CHECK state in Figure 28–18) and passes the value MASTER or SLAVE to PMA_CONFIG.indication (see 40.2.4.)
b) *Unsuccessful:* link_status_1GigT is set to FAIL and Auto-Negotiation restarts (see Figure 28–18.)
c) *Fault detected:* (This happens when both end stations are set for manual configuration and both are set to MASTER or both are set to SLAVE.) Bit 10.15 of the 1000BASE-T Status Register is set to logical one to indicate that a configuration fault has been detected. This bit also is set when seven attempts to configure the MASTER SLAVE relationship via the seed method have failed. When a fault is detected, link_status_1GigT is set to FAIL, causing Auto-Negotiation to cycle through again.

NOTE—MASTER-SLAVE arbitration only occurs if 1000BASE-T is selected as the highest common denominator; otherwise, it is assumed to have passed this condition.

40.6 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA.

Common-mode tests use the common-mode return point as a reference.

40.6.1 PMA-to-MDI interface tests

40.6.1.1 Electrical isolation

A PHY with a MDI that is a PI (see 33.1.3) shall meet the isolation requirements defined in 33.4.1 or 145.4.1.

A PHY with a MDI that is not a PI shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical isolation shall meet the isolation requirements as specified in J.1.

40.6.1.1.1 Test channel

To perform the transmitter MASTER-SLAVE timing jitter tests described in this clause, a test channel is required to ensure that jitter is measured under conditions of poor signal to echo ratio. This test channel shall be constructed by combining 100 and 120 Ω cable segments that both meet or exceed ISO/IEC 11801 Category 5 specifications for each pair, as shown in Figure 40–19, with the lengths and additional restrictions on parameters described in Table 40–6. The ends of the test channel shall be terminated with connectors meeting or exceeding ISO/IEC 11801:1995 Category 5 specifications. The return loss of the resulting test channel shall meet the return loss requirements of 40.7.2.3 and the crosstalk requirements of 40.7.3.

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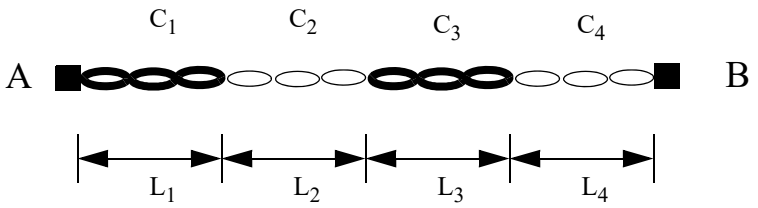

Identical for each of the four pairs.

Figure 40–19—Test channel topology for each cable pair

Table 40–6—Test channel cable segment specifications

Cable segment	Length (meters)	Characteristic impedance (at frequencies > 1 MHz)	Attenuation (per 100 meters at 31.25 MHz)
1	L_1=1.20	120 Ω ± 5 Ω	7.8 to 8.8 dB
2	L_2=x	100 Ω ± 5 Ω	10.8 to 11.8 dB
3	L_3=1.48	120 Ω ± 5 Ω	7.8 to 8.8 dB
4	L_4=y	100 Ω ± 5 Ω	10.8 to 11.8 dB

NOTE—x is chosen so that the total delay of segments C1, C2, and C3, averaged across all pairs, is equal to 570 ns at 31.25 MHz; however, if this would cause the total attenuation of segments C1, C2, and C3, averaged across all pairs, to exceed the worst case insertion loss specified in 40.7.2.1 then x is chosen so that the total attenuation of segments C1, C2, and C3, averaged across all pairs, does not violate 40.7.2.1 at any frequencies. The value of y is chosen so that the total attenuation of segments C1, C2, C3, and C4, averaged across all pairs, does not violate 40.7.2.1 at any frequency (y may be 0).

40.6.1.1.2 Test modes

The test modes described below shall be provided to allow for testing of the transmitter waveform, transmitter distortion, and transmitted jitter.

For a PHY with a GMII interface, these modes shall be enabled by setting bits 9.13:15 (1000BASE-T Control Register) of the GMII Management register set as shown in Table 40–7. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation. PHYs without a GMII shall provide a means to enable these modes for conformance testing.

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Table 40–7—GMII management register settings for test modes

Bit 1 (9.15)	Bit 2 (9.14)	Bit 3 (9.13)	Mode
0	0	0	Normal operation
0	0	1	Test mode 1—Transmit waveform test
0	1	0	Test mode 2—Transmit jitter test in MASTER mode
0	1	1	Test mode 3—Transmit jitter test in SLAVE mode
1	0	0	Test mode 4—Transmitter distortion test
1	0	1	Reserved, operations not identified.
1	1	0	Reserved, operations not identified.
1	1	1	Reserved, operations not identified.

When test mode 1 is enabled, the PHY shall transmit the following sequence of data symbols A_n, B_n, C_n, D_n, of 40.3.1.3.6 continually from all four transmitters:

{{+2 followed by 127 0 symbols}, {–2 followed by 127 0 symbols},{+1 followed by 127 0 symbols}, {–1 followed by 127 0 symbols}, {128 +2 symbols, 128 –2 symbols, 128 +2 symbols, 128 –2 symbols}, {1024 0 symbols}}

This sequence is repeated continually without breaks between the repetitions when the test mode is enabled. A typical transmitter output is shown in Figure 40–20. The transmitter shall time the transmitted symbols from a 125.00 MHz ± 0.01% clock in the MASTER timing mode.

When test mode 2 is enabled, the PHY shall transmit the data symbol sequence {+2, –2} repeatedly on all channels. The transmitter shall time the transmitted symbols from a 125.00 MHz ± 0.01% clock in the MASTER timing mode.

When test mode 3 is enabled, the PHY shall transmit the data symbol sequence {+2, –2} repeatedly on all channels. The transmitter shall time the transmitted symbols from a 125.00 MHz ± 0.01% clock in the SLAVE timing mode. A typical transmitter output for transmitter test modes 2 and 3 is shown in Figure 40–21.

When test mode 4 is enabled, the PHY shall transmit the sequence of symbols generated by the following scrambler generator polynomial, bit generation, and level mappings:

$$g_{s1} = 1 + x^9 + x^{11}$$

The maximum-length shift register used to generate the sequences defined by this polynomial shall be updated once per symbol interval (8 ns). The bits stored in the shift register delay line at a particular time n are denoted by $Scr_n[10:0]$. At each symbol period the shift register is advanced by one bit and one new bit represented by $Scr_n[0]$ is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive OR'd together to generate the next $Scr_n[0]$ bit. The bit sequences, $x0_n$, $x1_n$, and $x2_n$, generated from combinations of the scrambler bits as shown in the following equations, shall be used to generate the quinary symbols, s_n, as shown in Table 40–8. The quinary symbol sequence shall be presented simultaneously to all transmitters. The transmitter shall time the transmitted symbols from a 125.00 MHz ± 0.01% clock in the MASTER timing mode. A typical transmitter output for transmitter test mode 4 is shown in Figure 40–22.

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$$x0_n = Scr_n[0]$$

$$x1_n = Scr_n[1] \wedge Scr_n[4]$$

$$x2_n = Scr_n[2] \wedge Scr_n[4]$$

Table 40–8—Transmitter test mode 4 symbol mapping

x2n	x1n	x0n	quinary symbol, s_n
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	–1
1	0	0	0
1	0	1	1
1	1	0	–2
1	1	1	–1

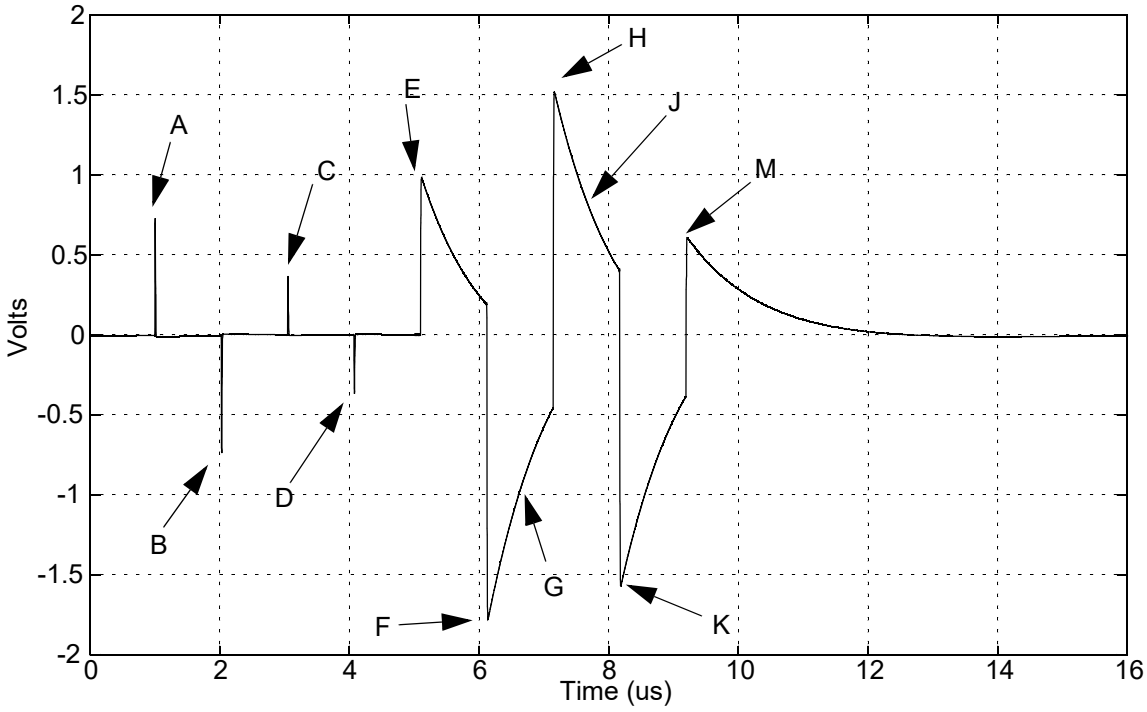

Figure 40–20—Example of transmitter test mode 1 waveform (1 cycle)

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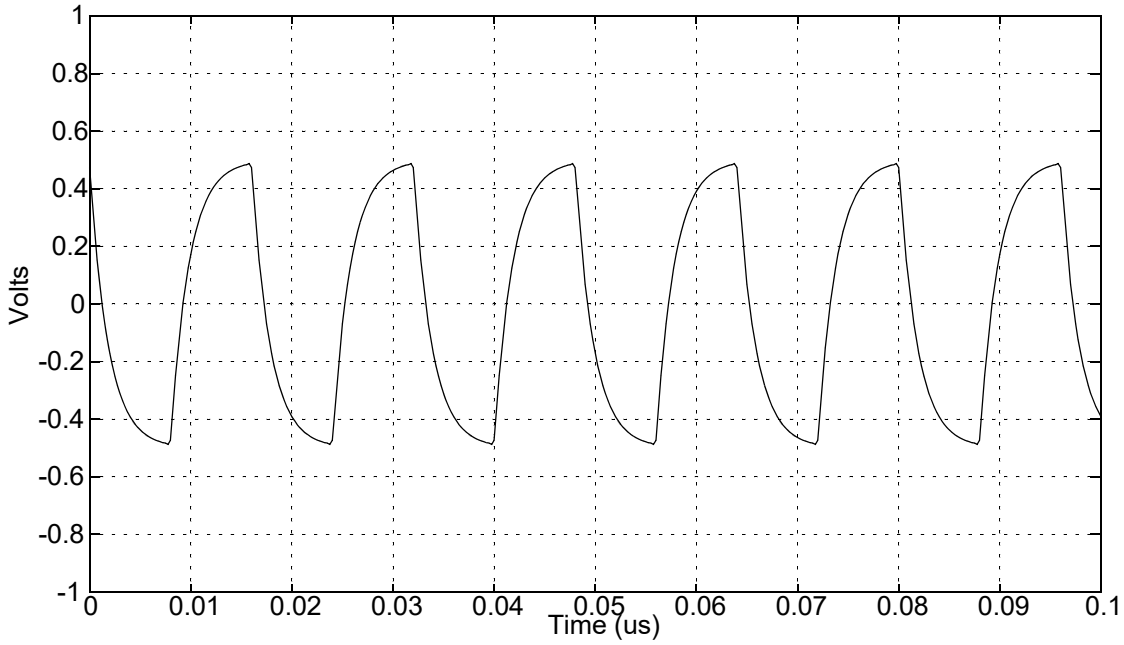

Figure 40–21—Example of transmitter test modes 2 and 3 waveform

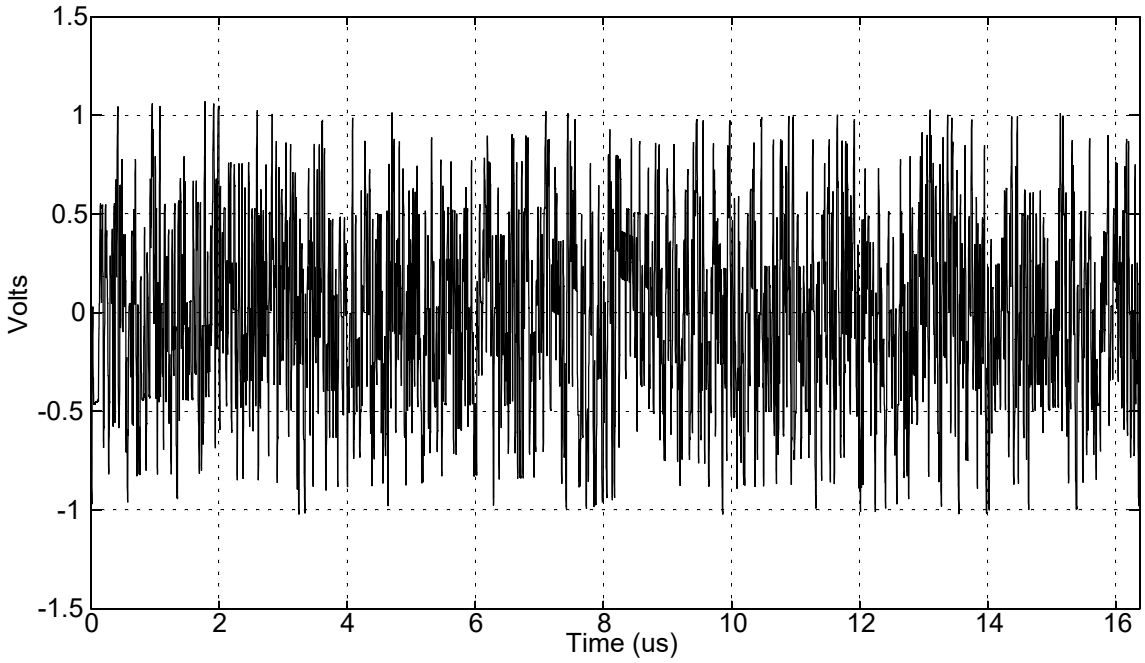

Figure 40–22—Example of Transmitter Test Mode 4 waveform (1 cycle)

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40.6.1.1.3 Test Fixtures

The following fixtures (illustrated by Figure 40–23, Figure 40–24, Figure 40–25, and Figure 40–26), or their functional equivalents, shall be used for measuring the transmitter specifications described in 40.6.1.2.

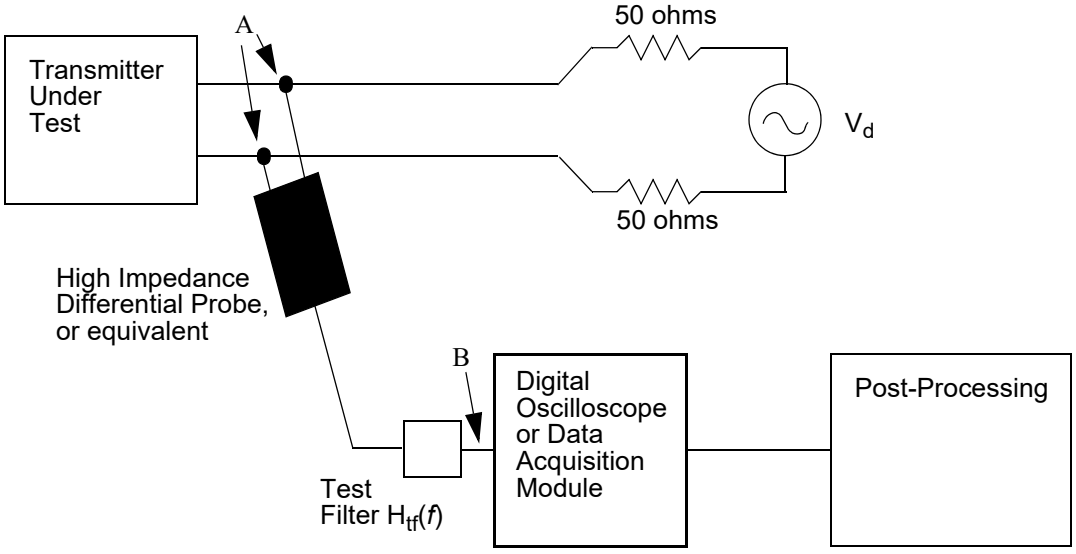

Figure 40–23—Transmitter test fixture 1 for template measurement

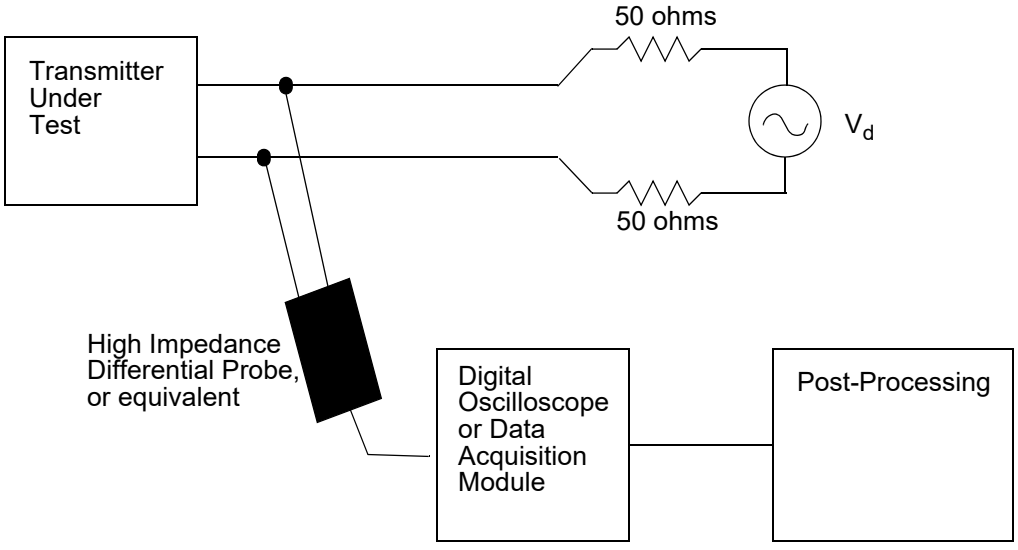

Figure 40–24—Transmitter test fixture 2 for droop measurement

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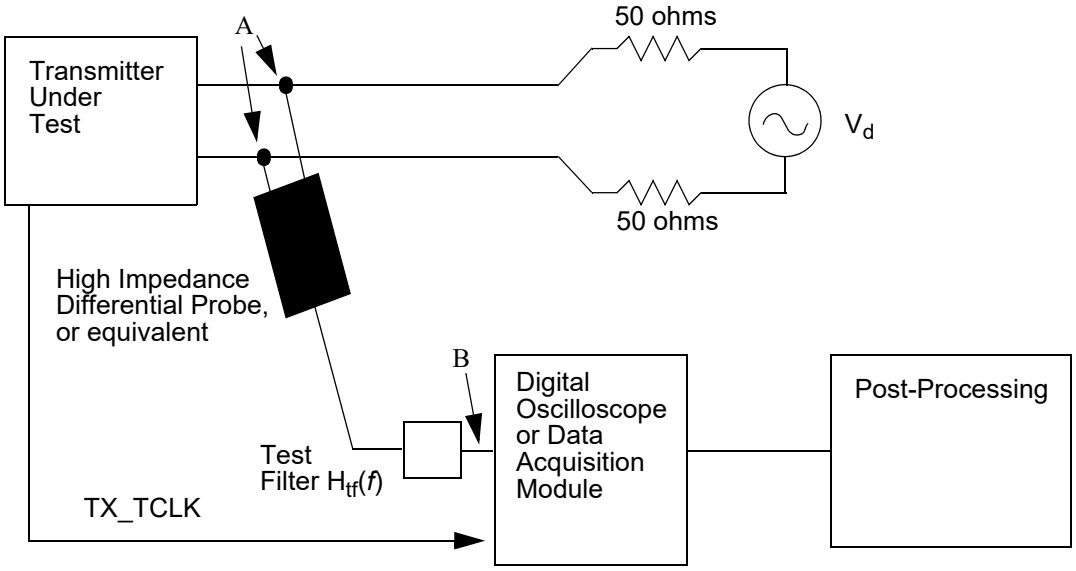

Figure 40–25—Transmitter test fixture 3 for distortion measurement

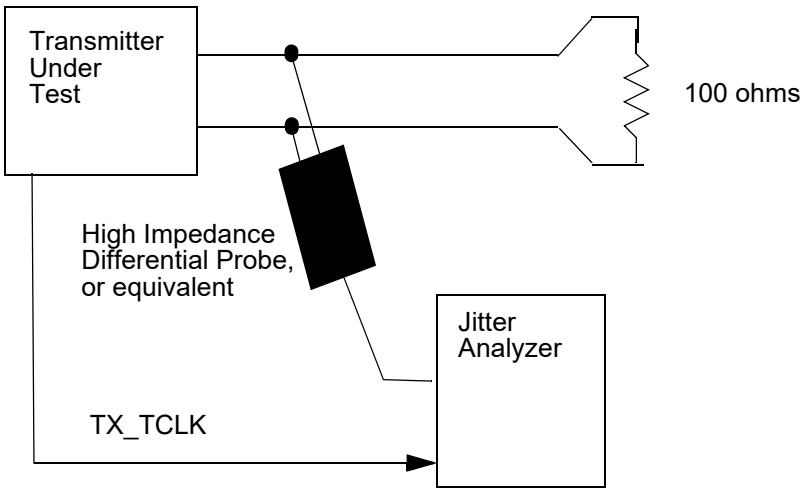

Figure 40–26—Transmitter test fixture 4 for transmitter jitter measurement

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The test filter, $H_{tf}(f)$, used in transmitter test fixtures 1 and 3 may be located between the points A and B as long as the test filter does not significantly alter the impedance seen by the transmitter. The test filter may instead be implemented as a digital filter in the post processing block. The test filter shall have the following continuous time transfer function or its discrete time equivalent:

$$H_{tf}(f) = \frac{jf}{jf + 2\times10^{6}} \qquad f \text{ in Hz}$$

NOTE—j denotes the square root of –1.

The disturbing signal, V_d, shall have the characteristics listed in Table 40–9.

Table 40–9—V_d Characteristics

Characteristic	Transmit test fixture 1	Transmit test fixture 2	Transmit test fixture 3
Waveform	Sine wave		
Amplitude	2.8 volts peak-to-peak	2.8 volts peak-to-peak	5.4 volts peak-to-peak
Frequency	31.25 MHz	31.25 MHz	20.833 MHz (125/6 MHz)
Purity	All harmonics >40 dB below fundamental		

The post-processing block has two roles. The first is to remove the disturbing signal from the measurement. A method of removing the disturbing signal is to take a single shot acquisition of the transmitted signal plus test pattern, then remove the best fit of a sine wave at the fundamental frequency of the disturbing signal from the measurement. It will be necessary to allow the fitting algorithm to adjust the frequency, phase, and amplitude parameters of the sine wave to achieve the best fit.

The second role of the post-processing block is to compare the measured data with the templates, droop specification, or distortion specification.

Trigger averaging of the transmitter output to remove measurement noise and increase measurement resolution is acceptable provided it is done in a manner that does not average out possible distortions caused by the interaction of the transmitter and the disturbing voltage. For transmitter template and droop measurements, averaging can be done by ensuring the disturbing signal is exactly synchronous to the test pattern so that the phase of the disturbing signal at any particular point in the test pattern remains constant. Trigger averaging also requires a triggering event that is synchronous to the test pattern. A trigger pulse generated by the PHY would be ideal for this purpose; however, in practice, triggering off the waveform generated by one of the other transmitter outputs that does not have the disturbing signal present may be possible.

NOTE—The disturbing signal may be made synchronous to the test pattern by creating the disturbing signal using a source of the transmit clock for the PHY under test, dividing it down to the proper frequency for the disturbing signal, passing the result through a high Q bandpass filter to eliminate harmonics and then amplifying the result to the proper amplitude.

The generator of the disturbing signal should have sufficient linearity and range that it does not introduce any appreciable distortion when connected to the transmitter output (see Table 40–9). This may be verified by replacing the transmitter under test with another identical disturbing signal generator having a different frequency output and verifying that the resulting waveform's spectrum does not show significant distortion products.

Additionally, to allow for measurement of transmitted jitter in master and slave modes, the PHY shall provide access to the 125 MHz symbol clock, TX_TCLK, that times the transmitted symbols (see 40.4.2.2). The PHY shall provide a means to enable this clock output if it is not normally enabled.

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40.6.1.2 Transmitter electrical specifications

The PMA shall provide the Transmit function specified in 40.4.2.2 in accordance with the electrical specifications of this clause.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.

The tolerance on the poles of the test filters used in this subclause shall be ±1%.

Practical considerations prevent measurement of the local transmitter performance in the presence of the remotely driven signal in this standard; however, the design of the transmitter to tolerate the presence of the remotely driven signal with acceptable distortion or other changes in performance is a critical issue and needs to be addressed by the implementer. To this end, a disturbing sine wave is used to simulate the presence of a remote transmitter for a number of the transmitter tests described in the following subordinate subclauses.

40.6.1.2.1 Peak differential output voltage and level accuracy

The absolute value of the peak of the waveform at points A and B, as defined in Figure 40–20, shall fall within the range of 0.67 V to 0.82 V (0.75 V ± 0.83 dB). These measurements are to be made for each pair while operating in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1 with no intervening cable.

The absolute value of the peak of the waveforms at points A and B shall differ by less than 1% from the average of the absolute values of the peaks of the waveform at points A and B.

The absolute value of the peak of the waveform at points C and D as defined in Figure 40–20 shall differ by less than 2% from 0.5 times the average of the absolute values of the peaks of the waveform at points A and B.

40.6.1.2.2 Maximum output droop

The magnitude of the negative peak value of the waveform at point G, as defined in Figure 40–20, shall be greater than 73.1% of the magnitude of the negative peak value of the waveform at point F. These measurements are to be made for each pair while in test mode 1 and observing the differential signal output at the MDI using transmit test fixture 2 with no intervening cable. Point G is defined as the point exactly 500 ns after point F. Point F is defined as the point where the waveform reaches its minimum value at the location indicated in Figure 40–20. Additionally, the magnitude of the peak value of the waveform at point J as defined in Figure 40–20 shall be greater than 73.1% of the magnitude of the peak value of the waveform at point H. Point J is defined as the point exactly 500 ns after point H. Point H is defined as the point where the waveform reaches its maximum value at the location indicated in Figure 40–20.

40.6.1.2.3 Differential output templates

The voltage waveforms around points A, B, C, D defined in Figure 40–20, after the normalization described herein, shall lie within the time domain template 1 defined in Figure 40–27 and the piecewise linear interpolation between the points in Table 40–10. These measurements are to be made for each pair while in test mode 1 and while observing the differential signal output at the MDI using transmitter test fixture 1 with no intervening cable. The waveforms may be shifted in time as appropriate to fit within the template.

The waveform around point A is normalized by dividing by the peak value of the waveform at A.

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The waveform around point B is normalized by dividing by the negative of the peak value of the waveform at A.

The waveform around point C is normalized by dividing by 1/2 the peak value of the waveform at A.

The waveform around point D is normalized by dividing by the negative of 1/2 the peak value of the waveform at A.

The voltage waveforms around points F and H defined in Figure 40–20, after the normalization described herein, shall lie within the time domain template 2 defined in Figure 40–27 and the piecewise linear interpolation between the points in Table 40–11. These measurements are to be made for each pair while in test mode 1 and while observing the differential signal output at the MDI using transmitter test fixture 1 with no intervening cable. The waveforms may be shifted in time as appropriate to fit within the template.

The waveform around point F is normalized by dividing by the peak value of the waveform at F.

The waveform around point H is normalized by dividing by the peak value of the waveform at H.

NOTE 1—The templates were created with the following assumptions about the elements in the transmit path:

1) Digital Filter: $0.75 + 0.25\ z^{-1}$
2) Ideal DAC
3) Single pole continuous time low-pass filter with pole varying from 70.8 MHz to 117 MHz or linear rise/fall time of 5 ns.
4) Single pole continuous time high-pass filter (transformer high pass) with pole varying from 1 Hz to 100 kHz.
5) Single pole continuous time high-pass filter (test filter) with pole varying from 1.8 MHz to 2.2 MHz.
6) Additionally, +0.025 was added to the upper template and –0.025 was added to the lower template to allow for noise and measurement error.

NOTE 2—The transmit templates are not intended to address electromagnetic radiation limits.

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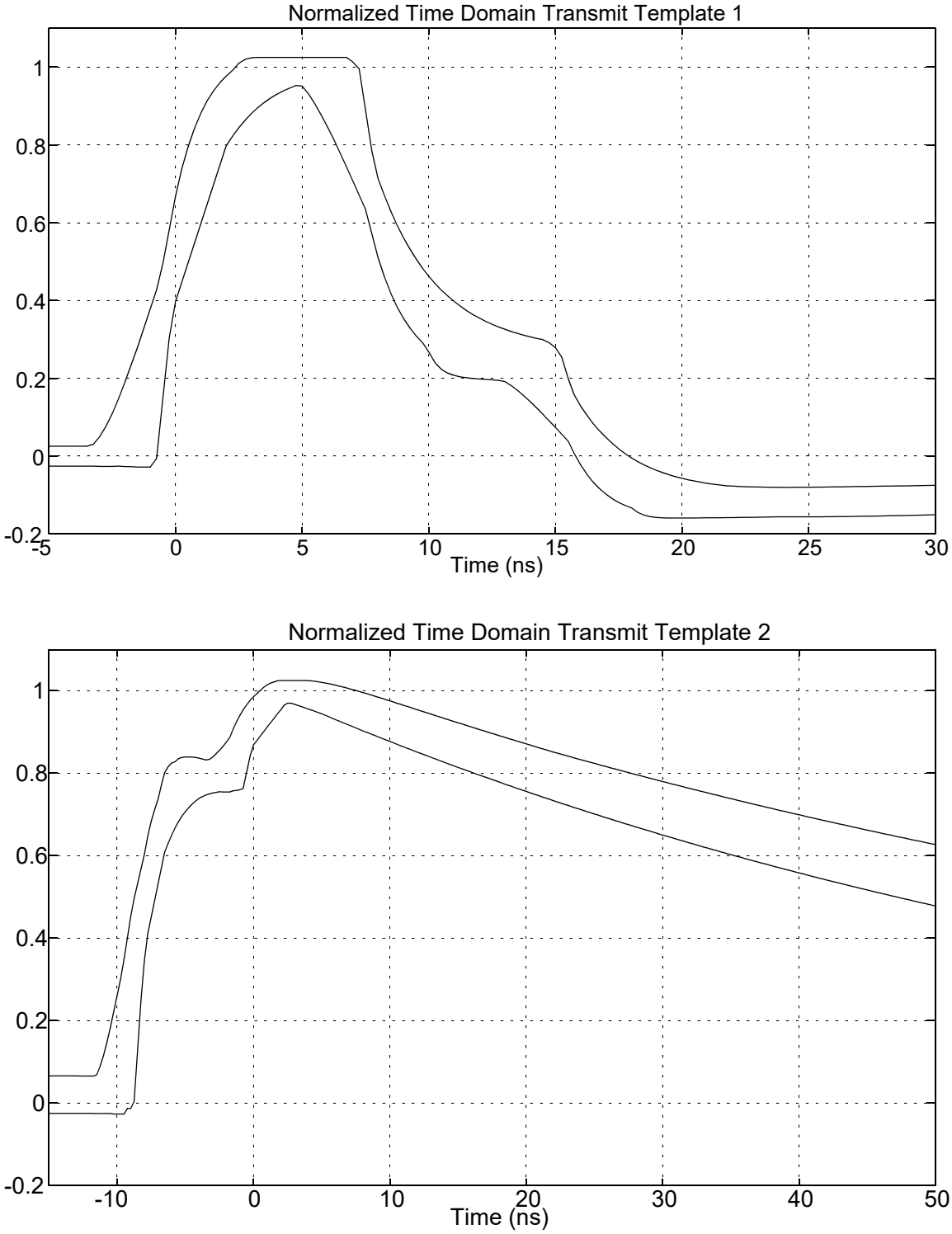

Figure 40–27—Normalized transmit templates as measured at MDI using transmit test fixture 1

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NOTE 3—The ASCII for Tables 40–10 and 40–11 is available at https://standards.ieee.org/downloads/802.3/.[82]

Table 40–10—Normalized time domain voltage template 1

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
–5.00	0.025	–0.026	12.75	0.332	0.195
–4.75	0.025	–0.026	13.00	0.326	0.192
–4.50	0.025	–0.026	13.25	0.320	0.181
–4.25	0.025	–0.026	13.50	0.315	0.169
–4.00	0.025	–0.026	13.75	0.311	0.155
–3.75	0.025	–0.026	14.00	0.307	0.140
–3.50	0.025	–0.026	14.25	0.303	0.124
–3.25	0.031	–0.026	14.50	0.300	0.108
–3.00	0.050	–0.026	14.75	0.292	0.091
–2.75	0.077	–0.026	15.00	0.278	0.074
–2.50	0.110	–0.026	15.25	0.254	0.056
–2.25	0.148	–0.026	15.50	0.200	0.039
–2.00	0.190	–0.027	15.75	0.157	0.006
–1.75	0.235	–0.027	16.00	0.128	–0.023
–1.50	0.281	–0.028	16.25	0.104	–0.048
–1.25	0.329	–0.028	16.50	0.083	–0.068
–1.00	0.378	–0.028	16.75	0.064	–0.084
–0.75	0.427	–0.006	17.00	0.047	–0.098
–0.50	0.496	0.152	17.25	0.032	–0.110
–0.25	0.584	0.304	17.50	0.019	–0.119
0.00	0.669	0.398	17.75	0.007	–0.127
0.25	0.739	0.448	18.00	–0.004	–0.133
0.50	0.796	0.499	18.25	–0.014	–0.145
0.75	0.844	0.550	18.50	–0.022	–0.152
1.00	0.882	0.601	18.75	–0.030	–0.156
1.25	0.914	0.651	19.00	–0.037	–0.158
1.50	0.940	0.701	19.25	–0.043	–0.159

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Table 40–10—Normalized time domain voltage template 1 *(continued)*

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
1.75	0.960	0.751	19.50	–0.048	–0.159
2.00	0.977	0.797	19.75	–0.053	–0.159
2.25	0.992	0.822	20.00	–0.057	–0.159
2.50	1.010	0.845	20.25	–0.061	–0.159
2.75	1.020	0.864	20.50	–0.064	–0.159
3.00	1.024	0.881	20.75	–0.067	–0.159
3.25	1.025	0.896	21.00	–0.070	–0.159
3.50	1.025	0.909	21.25	–0.072	–0.159
3.75	1.025	0.921	21.50	–0.074	–0.158
4.00	1.025	0.931	21.75	–0.076	–0.158
4.25	1.025	0.939	22.00	–0.077	–0.158
4.50	1.025	0.946	22.25	–0.078	–0.158
4.75	1.025	0.953	22.50	–0.079	–0.158
5.00	1.025	0.951	22.75	–0.079	–0.157
5.25	1.025	0.931	23.00	–0.079	–0.157
5.50	1.025	0.905	23.25	–0.080	–0.157
5.75	1.025	0.877	23.50	–0.080	–0.157
6.00	1.025	0.846	23.75	–0.080	–0.156
6.25	1.025	0.813	24.00	–0.080	–0.156
6.50	1.025	0.779	24.25	–0.080	–0.156
6.75	1.025	0.743	24.50	–0.080	–0.156
7.00	1.014	0.707	24.75	–0.080	–0.156
7.25	0.996	0.671	25.00	–0.080	–0.156
7.50	0.888	0.634	25.25	–0.080	–0.156
7.75	0.784	0.570	25.50	–0.080	–0.156
8.00	0.714	0.510	25.75	–0.079	–0.156
8.25	0.669	0.460	26.00	–0.079	–0.156
8.50	0.629	0.418	26.25	–0.079	–0.156
8.75	0.593	0.383	26.50	–0.079	–0.155

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Table 40–10—Normalized time domain voltage template 1 *(continued)*

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
9.00	0.561	0.354	26.75	–0.079	–0.155
9.25	0.533	0.330	27.00	–0.078	–0.155
9.50	0.507	0.309	27.25	–0.078	–0.155
9.75	0.483	0.292	27.50	–0.078	–0.154
10.00	0.462	0.268	27.75	–0.078	–0.154
10.25	0.443	0.239	28.00	–0.077	–0.154
10.50	0.427	0.223	28.25	–0.077	–0.153
10.75	0.411	0.213	28.50	–0.077	–0.153
11.00	0.398	0.208	28.75	–0.076	–0.153
11.25	0.385	0.204	29.00	–0.076	–0.152
11.50	0.374	0.201	29.25	–0.076	–0.152
11.75	0.364	0.199	29.50	–0.076	–0.152
12.00	0.355	0.198	29.75	–0.075	–0.151
12.25	0.346	0.197	30.00	–0.075	–0.151
12.50	0.339	0.196			

Table 40–11—Normalized time domain voltage template 2

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
–15.00	0.066	–0.025	18.00	0.891	0.779
–14.50	0.066	–0.025	18.50	0.886	0.773
–14.00	0.066	–0.025	19.00	0.881	0.767
–13.50	0.066	–0.025	19.50	0.876	0.762
–13.00	0.066	–0.025	20.00	0.871	0.756
–12.50	0.066	–0.025	20.50	0.866	0.750
–12.00	0.066	–0.025	21.00	0.861	0.745
–11.50	0.069	–0.025	21.50	0.856	0.739
–11.00	0.116	–0.025	22.00	0.852	0.734
–10.50	0.183	–0.025	22.50	0.847	0.728

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Table 40–11—Normalized time domain voltage template 2 *(continued)*

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
–10.00	0.261	–0.027	23.00	0.842	0.723
–9.50	0.348	–0.027	23.50	0.838	0.717
–9.00	0.452	–0.013	24.00	0.833	0.712
–8.50	0.535	0.130	24.50	0.828	0.707
–8.00	0.604	0.347	25.00	0.824	0.701
–7.50	0.683	0.451	25.50	0.819	0.696
–7.00	0.737	0.531	26.00	0.815	0.691
–6.50	0.802	0.610	26.50	0.811	0.686
–6.00	0.825	0.651	27.00	0.806	0.680
–5.50	0.836	0.683	27.50	0.802	0.675
–5.00	0.839	0.707	28.00	0.797	0.670
–4.50	0.839	0.725	28.50	0.793	0.665
–4.00	0.837	0.739	29.00	0.789	0.660
–3.50	0.832	0.747	29.50	0.784	0.655
–3.00	0.839	0.752	30.00	0.780	0.650
–2.50	0.856	0.755	30.50	0.776	0.645
–2.00	0.875	0.755	31.00	0.772	0.641
–1.50	0.907	0.758	31.50	0.767	0.636
–1.00	0.941	0.760	32.00	0.763	0.631
–0.50	0.966	0.803	32.50	0.759	0.626
0.00	0.986	0.869	33.00	0.755	0.621
0.50	1.001	0.890	33.50	0.751	0.617
1.00	1.014	0.912	34.00	0.747	0.612
1.50	1.022	0.933	34.50	0.743	0.607
2.00	1.025	0.954	35.00	0.739	0.603
2.50	1.025	0.970	35.50	0.734	0.598
3.00	1.025	0.967	36.00	0.730	0.594
3.50	1.025	0.962	36.50	0.727	0.589
4.00	1.025	0.956	37.00	0.723	0.585

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Table 40–11—Normalized time domain voltage template 2 *(continued)*

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
4.50	1.023	0.950	37.50	0.719	0.580
5.00	1.020	0.944	38.00	0.715	0.576
5.50	1.017	0.937	38.50	0.711	0.571
6.00	1.014	0.931	39.00	0.707	0.567
6.50	1.010	0.924	39.50	0.703	0.563
7.00	1.005	0.917	40.00	0.699	0.558
7.50	1.001	0.910	40.50	0.695	0.554
8.00	0.996	0.903	41.00	0.692	0.550
8.50	0.991	0.897	41.50	0.688	0.546
9.00	0.986	0.890	42.00	0.684	0.541
9.50	0.981	0.884	42.50	0.680	0.537
10.00	0.976	0.877	43.00	0.677	0.533
10.50	0.970	0.871	43.50	0.673	0.529
11.00	0.965	0.864	44.00	0.669	0.525
11.50	0.960	0.858	44.50	0.666	0.521
12.00	0.954	0.852	45.00	0.662	0.517
12.50	0.949	0.845	45.50	0.659	0.513
13.00	0.944	0.839	46.00	0.655	0.509
13.50	0.938	0.833	46.50	0.651	0.505
14.00	0.933	0.827	47.00	0.648	0.501
14.50	0.928	0.820	47.50	0.644	0.497
15.00	0.923	0.814	48.00	0.641	0.493
15.50	0.917	0.808	48.50	0.637	0.490
16.00	0.912	0.802	49.00	0.634	0.486
16.50	0.907	0.796	49.50	0.631	0.482
17.00	0.902	0.791	50.00	0.627	0.478
17.50	0.897	0.785			

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40.6.1.2.4 Transmitter distortion

When in test mode 4 and observing the differential signal output at the MDI using transmitter test fixture 3, for each pair, with no intervening cable, the peak distortion as defined below shall be less than 10 mV.

The peak distortion is determined by sampling the differential signal output with the symbol rate TX_TCLK at an arbitrary phase and processing a block of any 2047 consecutive samples with the code listed below.[83] Note that this code assumes that the differential signal has already been filtered by the test filter. A PHY is considered to pass this test if the peak distortion is below 10 mV for at least 60% of the UI within the eye opening.

NOTE—The ASCII for the following code is available at https://standards.ieee.org/downloads/802.3/.[84]

Code for Distortion Post Processing is as follows:

```
%
% Distortion Specification Post Processing
%

% Initialize Variables
clear
symbolRate=125e6;                                % symbol rate
dataFile=input('Data file name: ','s')

% Generate test pattern symbol sequence

scramblerSequence=ones(1,2047);
for i=12:2047
  scramblerSequence(i)=mod(scramblerSequence(i-11) + scramblerSequence(i-9),2);
end

for i=1:2047
  temp=scramblerSequence(mod(i-1,2047)+1) + ...
      2*mod(scramblerSequence(mod(i-2,2047)+1) + scramblerSequence(mod(i-
5,2047)+1),2) + ...
      4*mod(scramblerSequence(mod(i-3,2047)+1) + scramblerSequence(mod(i-
5,2047)+1),2);
  switch temp
    case 0,
      testPattern(i)=0;
    case 1,
      testPattern(i)=1;
    case 2,
      testPattern(i)=2;
    case 3,
      testPattern(i)=-1;
    case 4,
      testPattern(i)=0;
    case 5,
      testPattern(i)=1;
    case 6,
      testPattern(i)=-2;
    case 7,
      testPattern(i)=-1;
  end
end
```

[83]This code is written in the MATLAB programming language (see 1.3); however, use of this language does not indicate an endorsement of MATLAB by IEEE and, as such, any tool can be used to perform this calculation.

[84]*Copyright release for MATLAB code*: Users of this standard may freely reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

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```
% Input data file
fid=fopen(dataFile,'r');
sampledData=fscanf(fid,'%f');
fclose(fid);
sampledData=sampledData.';


if (length(sampledData) < 2047)
  error('Need to have 2047 consecutive samples for processing');
elseif (length(sampledData) > 2047)
  fprintf(1,'\n Warning - only using first 2047 samples in data file');
  sampledData=sampledData(1:2047);
end


% Fit a sine wave to the data and temporarily remove it to yield processed data

options=foptions;
options(1)=0;
options(2)=1e-8;
options(3)=1e-8;
options(14)=2000;
gradfun=zeros(0);
P=fmins('sinefit',[2.0 0 125/6.],options,gradfun,sampledData,symbolRate);

P

processedData=sampledData - ...
    P(1)*sin(2*pi*(P(3)*1e6*[0:2046]/symbolRate + P(2)*1e-9*symbolRate));



% LMS Canceller

numberCoeff=70;  % Number of coefficients in canceller
coefficients=zeros(1,numberCoeff);
delayLine=testPattern;

% Align data in delayLine to sampled data pattern
temp=xcorr(processedData,delayLine);
index=find(abs(temp)==max(abs(temp)));
index=mod(mod(length(processedData) - index(1),2047)+numberCoeff-10,2047);
delayLine=[delayLine((end-index):end) delayLine(1:(end-index-1))];


% Compute coefficients that minimize squared error in cyclic block

for i=1:2047
  X(i,:)=delayLine(mod([0:(numberCoeff-1)]+i-1,2047)+1);
end
coefficients=(inv(X.' * X)*(processedData*X).').';



% Canceller
for i=1:2047
  err(i)=processedData(i) - sum(delayLine(1+mod((i-1):(i+numberCoeff-
2),2047)).*coefficients);
end

% Add back temporarily removed sine wave

err=err+P(1)*sin(2*pi*(P(3)*1e6*[0:2046]./symbolRate + P(2)*1e-9*symbolRate));
```


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```
% Re-fit sine wave and do a final removal

options=foptions;
options(1)=0;
options(2)=1e-12;
options(3)=1e-12;
options(14)=10000;
gradfun=zeros(0);
P=fmins('sinefit',[2.0 0 125/6.],options,gradfun,err,symbolRate);

P

processedData=sampledData - ...
    P(1)*sin(2*pi*(P(3)*1e6*[0:2046]/symbolRate + P(2)*1e-9*symbolRate));


% Compute coefficients that minimize squared error in cyclic block

coefficients=(inv(X.' * X)*(processedData*X).').';



% Canceller
for i=1:2047
  err(i)=processedData(i) - sum(delayLine(1+mod((i-1):(i+numberCoeff-
2),2047)).*coefficients);
end

% SNR Calculation
signal=0.5;
noise=mean(err.^2);

SNR=10*log10(signal./noise);

% Output Peak Distortion

peakDistortion=max(abs(err))


% Function for fitting sine wave
function err=sinefit(parameters,data,symbolRate)
err=sum((data- ...
    parameters(1)*sin(2*pi*(parameters(3)*1e6*[0:(length(data)-1)]/symbolRate +
parameters(2)*1e-9*symbolRate))).^2);
```

40.6.1.2.5 Transmitter timing jitter

When in test mode 2 or test mode 3, the peak-to-peak jitter J_{txout} of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of TX_TCLK is measured. The corresponding edge of TX_TCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.

When in the normal mode of operation as the MASTER, the peak-to-peak value of the MASTER TX_TCLK jitter relative to an unjittered reference shall be less than 1.4 ns. When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf1}(f)$, having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus J_{txout} shall be less than 0.3 ns.

$$H_{jf1}(f) = \frac{jf}{jf + 5000} \qquad f \text{ in Hz}$$

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When in the normal mode of operation as the SLAVE, receiving valid signals from a compliant PHY operating as the MASTER using the test channel defined in 40.6.1.1.1, with test channel port A connected to the SLAVE, the peak-to-peak value of the SLAVE TX_TCLK jitter relative to the MASTER TX_TCLK shall be less than 1.4 ns after the receiver is properly receiving the data and has set bit 10.13 of the GMII management register set to 1. When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf2}(f)$, having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus J_{txout} shall be no more than 0.4 ns greater than the simultaneously measured peak-to-peak value of the MASTER jitter filtered by $H_{jf1}(f)$.

$$H_{jf2}(f) = \frac{jf}{jf + 32000} \qquad f \text{ in Hz}$$

NOTE—j denotes the square root of –1.

For all high-pass filtered jitter measurements, the peak-to-peak value shall be measured over an unbiased sample of at least 10^5 clock edges. For all unfiltered jitter measurements, the peak-to-peak value shall be measured over an interval of not less than 100 ms and not more than 1 second.

When the PHY supports the optional EEE capability, the unfiltered jitter requirements shall also be satisfied during the LPI mode, with the exception that clock edges corresponding to the WAIT_QUIET, QUIET, WAKE, and WAKE_SILENT states are not considered in the measurement. The PHY may turn off TX_TCLK during these states. For a MASTER PHY operating in the LPI mode, the unjittered reference shall be continuous.

40.6.1.2.6 Transmit clock frequency

The quinary symbol transmission rate on each pair of the master PHY shall be 125.00 MHz ± 0.01%.

40.6.1.2.7 Transmitter operation following a transition from the QUIET to the WAKE state

When the PHY supports the optional EEE capability, it transmits Idle symbols while in the WAKE state (see Figure 40–16b). This signal may be transmitted during reactivation of the PHY analog front-end and is not guaranteed or intended to be compliant.

The transmit levels of the Idle symbols transmitted during the WAKE state shall exceed 65% of the transmit levels of compliant Idle symbols for a period of at least 500 ns.

The PHY shall achieve compliant operation upon entry to the WAKE_TRAINING state (see Figure 40–16b).

40.6.1.3 Receiver electrical specifications

The PMA shall provide the Receive function specified in 40.4.2.3 in accordance with the electrical specifications of this clause. The patch cabling and interconnecting hardware used in test configurations shall be within the limits specified in 40.7.

40.6.1.3.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 40.6.1.2 and have passed through a link specified in 40.7 are translated into one of the PMA_UNITDATA.indication messages with a bit error ratio less than 10^{-10} and sent to the PCS after link reset completion. Since the 4-D symbols are not accessible, this specification shall be satisfied by a frame error ratio less than 10^{-7} for 125 octet frames.

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40.6.1.3.2 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a 5-level symbol rate within the range 125.00 MHz ± 0.01%.

40.6.1.3.3 Common-mode noise rejection

This specification is provided to limit the sensitivity of the PMA receiver to common-mode noise from the cabling system. Common-mode noise generally results when the cabling system is subjected to electromagnetic fields. Figure 40–28 shows the test configuration, which uses a capacitive cable clamp, that injects common-mode signals into a cabling system.

A 100-meter, 4-pair Category 5 cable that meets the specification of 40.7 is connected between two 1000BASE-T PHYs and inserted into the cable clamp. The cable should be terminated on each end with an MDI connector plug specified in 40.8.1. The clamp should be located a distance of ~20 cm from the receiver. It is recommended that the cable between the transmitter and the cable clamp be installed either in a linear run or wrapped randomly on a cable rack. The cable rack should be at least 3 m from the cable clamp. In addition, the cable clamp and 1000BASE-T receiver should be placed on a common copper ground plane and the ground of the receiver should be in contact with the ground plane. The chassis grounds of all test equipment used should be connected to the copper ground plane. No connection is required between the copper ground plane and an external reference. A description of the cable clamp, as well as the validation procedure, can be found in Annex 40B.

A signal generator with a 50 Ω impedance is connected to one end of the clamp and an oscilloscope with a 50 Ω input is connected to the other end of the clamp. The signal generator shall be capable of providing a sine wave signal of 1 MHz to 250 MHz. The output of the signal generator is adjusted for a voltage of 1.0 Vrms (1.414 Vpeak) on the oscilloscope.

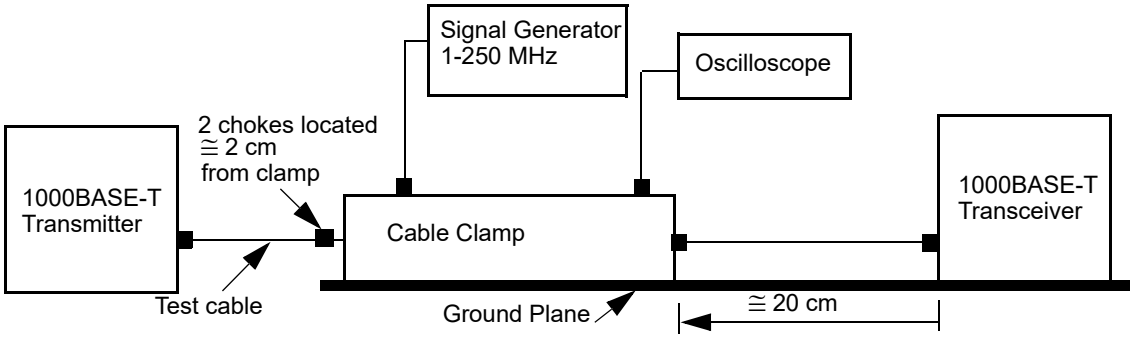

Figure 40–28—Receiver common-mode noise rejection test

While sending data from the transmitter, the receiver shall send the proper PMA_UNITDATA.indication messages to the PCS as the signal generator frequency is varied from 1 MHz to 250 MHz.

NOTE—Although the signal specification is constrained within the 1–100 MHz band, this test is performed up to 250 MHz to ensure the receiver under test can tolerate out-of-band (100–250 MHz) noise.

40.6.1.3.4 Alien Crosstalk noise rejection

While receiving data from a transmitter specified in 40.6.1.2 through a link segment specified in 40.7 connected to all MDI duplex channels, a receiver shall send the proper PMA_UNITDATA.indication message to the PCS when any one of the four pairs is connected to a noise source as described in Figure 40–29. Because symbol encoding is employed, this specification shall be satisfied by a frame error ratio of less than 10^{-7} for 125 octet frames. The level of the noise signal at the MDI is nominally 25 mV

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peak-to-peak. (Measurements are to be made on each of the four pairs.) The noise source shall be connected to one of the MDI inputs using Category 5 balanced cable of a maximum length of 0.5 m.

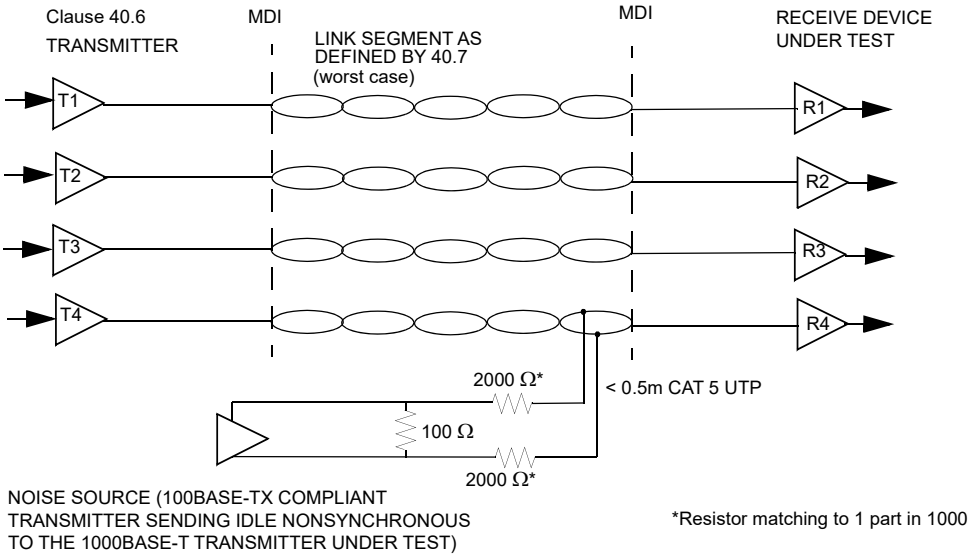

Figure 40–29—Differential mode noise rejection test

40.6.1.3.5 Signal_detect

When the PHY supports the optional EEE capability, the PMA Receive function shall convey an indicator of signal presence, referred to as signal_detect, to the PMA PHY Control function. The value of signal_detect shall be set to TRUE within 0.5 µs of the receipt of a wake signal meeting the requirements of 40.6.1.2.7. The value of signal_detect shall be set to FALSE within 0.5 µs of the receipt of a continuous sequence of zeros.

40.7 Link segment characteristics

1000BASE-T is designed to operate over a 4-pair Category 5/Class D balanced cabling system. Each of the four pairs supports an effective data rate of 250 Mb/s in each direction simultaneously. The term “link segment” used in this clause refers to four duplex channels. The term “duplex channel” will be used to refer to a single channel with full duplex capability. Specifications for a link segment apply equally to each of the four duplex channels. All implementations of the balanced cabling link shall be compatible at the MDI.

40.7.1 Cabling system characteristics

1000BASE-T requires 4-pair Class D cabling with a nominal impedance of 100 Ω, as specified in ISO/IEC 11801:1995. The cabling system components (cables, cords, and connectors) used to provide the link segment shall consist of Category 5 components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995. Additionally:

a) 1000BASE-T is an ISO/IEC 11801 Class D application, with additional installation requirements and transmission parameters specified in Annex 40A.
b) The width of the PMD transmit signal spectrum is approximately 80 MHz.
c) The use of shielding is outside the scope of this standard.

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40.7.2 Link transmission parameters

The transmission parameters contained in this subclause are specified to ensure that a Class D link segment of up to at least 100 m will provide a reliable medium. The transmission parameters of the link segment include insertion loss, delay parameters, characteristic impedance, NEXT loss, ELFEXT loss, and return loss.

Link segment testing shall be conducted using source and load impedances of 100 Ω. The tolerance on the poles of the test filter used in this subclause shall be no worse than 1%.

40.7.2.1 Insertion loss

The insertion loss of each duplex channel shall be less than

$$Insertion\_Loss(f) < 2.1\,f^{0.529} + 0.4/f \quad \text{(dB)}$$

at all frequencies from 1 MHz to 100 MHz. This includes the attenuation of the balanced cabling pairs, including work area and equipment cables plus connector losses within each duplex channel. The insertion loss specification shall be met when the duplex channel is terminated in 100 Ω.

NOTE—The above equation approximates the insertion loss specification at discrete frequencies for Class D 100 m channels specified by ISO/IEC 11801:1995.

40.7.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each link segment duplex channel, which includes cable cords and connecting hardware, is 100 Ω for all frequencies between 1 MHz and 100 MHz.

40.7.2.3 Return loss

Each link segment duplex channel shall meet or exceed the return loss specified in the following equation at all frequencies from 1 MHz to 100 MHz.

$$Return\_Loss(f) \begin{cases} 15 & (1 - 20\ \text{MHz}) \\ 15 - 10\log_{10}(f/20) & (20 - 100\ \text{MHz}) \end{cases} \text{(dB)}$$

where f is the frequency in MHz. The reference impedance shall be 100 Ω.

40.7.3 Coupling parameters

In order to limit the noise coupled into a duplex channel from adjacent duplex channels, Near-End Crosstalk (NEXT) loss and Equal Level Far-End Crosstalk (ELFEXT) loss are specified for each link segment. Each duplex channel can be disturbed by more than one duplex channel. Requirements for Multiple Disturber Near-End Crosstalk (MDNEXT) are satisfied even when worst case conditions of differential pair-to-pair NEXT as specified under 40.7.3.1.1 occur. Therefore, there are no separate requirements for MDNEXT. Requirements for Multiple Disturber Equal-Level Far-End Crosstalk (MDELFEXT) loss are specified in 40.7.3.2.2.

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40.7.3.1 Near-End Crosstalk (NEXT)

40.7.3.1.1 Differential Near-End Crosstalk

In order to limit the crosstalk at the near end of a link segment, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between a duplex channel and the other three duplex channels is specified to meet the symbol error ratio objective specified in 40.1. The NEXT loss between any two duplex channels of a link segment shall be at least

$$27.1 - 16.8\log_{10}(f/100)$$

where f is the frequency over the range of 1 MHz to 100 MHz.

NOTE—The previous equation approximates the NEXT loss specification at discrete frequencies for Class D 100 m channels specified by ISO/IEC 11801:1995.

40.7.3.2 Far-End Crosstalk (FEXT)

40.7.3.2.1 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk at the far end of each link segment duplex channel and meet the BER objective specified in 40.6.1.3.1. Far-End Crosstalk (FEXT) is crosstalk that appears at the far end of a duplex channel (disturbed channel), which is coupled from another duplex channel (disturbing channel) with the noise source (transmitters) at the near end. FEXT loss is defined as

$$FEXT\_Loss(f) = 20\log_{10}[V\text{pds}(f)/V\text{pcn}(f)]$$

and ELFEXT_Loss is defined as

$$ELFEXT\_Loss(f) = 20\log_{10}[V\text{pds}(f)/V\text{pcn}(f)] - SLS\_Loss(f)$$

where

Vpds	is the peak voltage of disturbing signal (near-end transmitter)
Vpcn	is the peak crosstalk noise at far end of disturbed channel
SLS_Loss	is the insertion loss of disturbed channel in dB

The worst pair ELFEXT loss between any two duplex channels shall be greater than $17 - 20\log_{10}(f/100)$ dB where f is the frequency over the range of 1 MHz to 100 MHz.

40.7.3.2.2 Multiple Disturber Equal Level Far-End Crosstalk (MDELFEXT) loss

Since four duplex channels are used to transfer data between PMDs, the FEXT that is coupled into a data carrying channel will be from the three adjacent disturbing duplex channels. This specification is consistent with three channel-to-channel disturbers—one with a ELFEXT loss of at least $17 - 20\log_{10}(f/100)$ dB, one with a ELFEXT loss of at least $19.5 - 20\log_{10}(f/100)$ dB, and one with a ELFEXT loss of at least $23 - 20\log_{10}(f/100)$ dB. To ensure the total FEXT coupled into a duplex channel is limited, multiple disturber ELFEXT loss is specified as the power sum of the individual ELFEXT losses.

The Power Sum loss between a duplex channel and the three adjacent disturbers shall be

$$PSELFEXT\ loss > 14.4 - 20\log_{10}(f/100)\ \text{dB}$$

where f is the frequency over the range of 1 MHz to 100 MHz.

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40.7.3.2.3 Multiple-Disturber Power Sum Equal Level Far-End Crosstalk (PSELFEXT) loss

PSELFEXT loss is determined by summing the magnitude of the three individual pair-to-pair differential ELFEXT loss values over the frequency range 1 to 100 MHz as follows:

$$\text{PSELFEXT\_Loss(f)} = -10\log_{10}\sum_{i=1}^{i=3} 10^{-(NL(f)i)/10}$$

where

NL(*f*)i is the magnitude of ELFEXT loss at frequency *f* of pair combination *i*
i is the 1, 2, or 3 (pair-to-pair combination)

40.7.4 Delay

In order to simultaneously send data over four duplex channels in parallel, the propagation delay of each duplex channel as well as the difference in delay between any two of the four channels are specified. This ensures the 1000 Mb/s data that is divided across four channels can be properly reassembled at the far-end receiver. This also ensures the round-trip delay requirement for effective collision detection is met.

40.7.4.1 Maximum link delay

The propagation delay of a link segment shall not exceed 570 ns at all frequencies between 2 MHz and 100 MHz.

40.7.4.2 Link delay skew

The difference in propagation delay, or skew, between all duplex channel pair combinations of a link segment, under all conditions, shall not exceed 50 ns at all frequencies from 2 MHz to 100 MHz. It is a further functional requirement that, once installed, the skew between any two of the four duplex channels due to environmental conditions shall not vary more than 10 ns within the above requirement.

40.7.5 Noise environment

The 1000BASE-T noise environment consists of noise from many sources. The primary noise sources that impact the objective BER are NEXT and echo interference, which are reduced to a small residual noise using cancelers. The remaining noise sources, which are secondary sources, are discussed in the following list.

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The 1000BASE-T noise environment consists of the following:

a) Echo from the local transmitter on the same duplex channel (cable pair). Echo is caused by the hybrid function used to achieve simultaneous bidirectional transmission of data and by impedance discontinuities in the link segment. It is impractical to achieve the objective BER without using echo cancellation. Since the symbols transmitted by the local disturbing transmitter are available to the cancellation processor, echo interference can be reduced to a small residual noise using echo cancellation methods.

b) Near-End Crosstalk (NEXT) interference from the local transmitters on the duplex channels (cable pairs) of the link segment. Each receiver will experience NEXT interference from three adjacent transmitters. NEXT cancelers are used to reduce the interference from each of the three disturbing transmitters to a small residual noise. NEXT cancellation is possible since the symbols transmitted by the three disturbing local transmitters are available to the cancellation processor. NEXT cancelers can reduce NEXT interference by at least 20 dB.

c) Far-End Crosstalk (FEXT) noise at a receiver is from three disturbing transmitters at the far end of the duplex channel (cable pairs) of the link segment. FEXT noise can be cancelled in the same way as echo and NEXT interference although the symbols from the remote transmitters are not immediately available. However, FEXT noise is much smaller than NEXT interference and can generally be tolerated.

d) Intersymbol interference (ISI). ISI is the extraneous energy from one signaling symbol that interferes with the reception of another symbol on the same channel.

e) Noise from non-idealities in the duplex channel, transmitters, and receivers; for example, DAC/ADC non-linearity, electrical noise (shot and thermal), and non-linear channel characteristics.

f) Noise from sources outside the cabling that couple into the link segment via electric and magnetic fields.

g) Noise from signals in adjacent cables. This noise is referred to as alien NEXT noise and is generally present when cables are bound tightly together. Since the transmitted symbols from the alien NEXT noise source are not available to the cancellation processor (they are in another cable), it is not possible to cancel the alien NEXT noise. To ensure robust operation the alien NEXT noise has to meet the specification of 40.7.6.

40.7.6 External coupled noise

The noise coupled from external sources that is measured at the output of a filter connected to the output of the near end of a disturbed duplex channel should not exceed 40 mV peak-to-peak. The filter for this measurement is a fifth order Butterworth filter with a 3 dB cutoff at 100MHz.

40.8 MDI specification

This subclause defines the MDI. The link topology requires a crossover function in a DTE-to-DTE connection. See 40.4.4 for a description of the automatic MDI/MDI-X configuration.

40.8.1 MDI connectors

Eight-pin connectors meeting the requirements of subclause 3 and Figures 1 through 4 of IEC 60603-7:1990 shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figure 40–30 and Figure 40–31. The assignment of PMA signals to connector contacts for PHYs is shown in Table 40–12.

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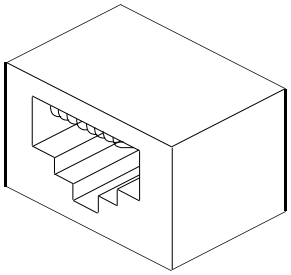

Figure 40–30—MDI connector

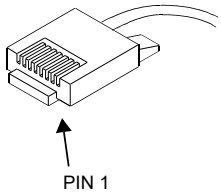

Figure 40–31—Balanced cabling connector

Table 40–12—Assignment of PMA signal to MDI and MDI-X pin-outs

Contact	MDI	MDI-X
1	BI_DA+	BI_DB+
2	BI_DA–	BI_DB–
3	BI_DB+	BI_DA+
4	BI_DC+	BI_DD+
5	BI_DC–	BI_DD–
6	BI_DB–	BI_DA–
7	BI_DD+	BI_DC+
8	BI_DD–	BI_DC–

40.8.2 Crossover function

Although the automatic MDI/MDI-X configuration (see 40.4.4) is not required for successful operation of 1000BASE-T, a crossover function has to be implemented for every link segment to support the operation of Auto-Negotiation. The crossover function connects the transmitters of one PHY to the receivers of the PHY at the other end of the link segment. Crossover functions may be implemented internally to a PHY or elsewhere in the link segment. For a PHY that does not implement the crossover function, the MDI labels in the middle column of Table 40–12 refer to its own internal circuits. For PHYs that do implement the internal crossover, the MDI labels in the last column of Table 40–12 refer to the internal circuits of the remote PHY of the link segment. Additionally, the MDI connector for a PHY that implements the crossover function shall be marked with the graphical symbol X. The crossover function specified here is not compatible with the crossover function specified in 14.5.2 for pairs TD and RD.

When a link segment connects a single-port device to a multiport device, it is recommended that the crossover be implemented in the PHY local to the multiport device. If neither or both PHYs of a link segment contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the PHYs. When both PHYs contain

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internal crossovers, it is further recommended that, in networks in which the topology identifies either a central backbone segment or a central device, the PHY furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

40.8.3 MDI electrical specifications

The MDI connector (jack) when mated with a specified balanced cabling connector (plug) shall meet the electrical requirements for Category 5 connecting hardware for use with 100-ohm Category 5 cable as specified in ISO/IEC 11801:1995.

The mated MDI/balanced cabling connector pair shall have a FEXT loss not less than $40 - 20\log_{10}(f/100)$ (where f is the frequency over the range 1 MHz to 100 MHz) between all contact pair combinations shown in Table 40–12.

No spurious signals shall be emitted onto the MDI when the PHY is held in power-down mode (as defined in 22.2.4.1.5) independent of the value of TX_EN, when released from power-down mode, or when external power is first applied to the PHY.

40.8.3.1 MDI return loss

The differential impedance at the MDI for each transmit/receive channel shall be such that any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 Ω ± 15% is attenuated, relative to the incident signal, at least 16 dB over the frequency range of 1.0 MHz to 40 MHz and at least $10 - 20\log_{10}(f/80)$ dB over the frequency range 40 MHz to 100 MHz (f in MHz). This return loss shall be maintained at all times when the PHY is transmitting data or control symbols.

40.8.3.2 MDI impedance balance

Impedance balance is a measurement of the impedance-to-ground difference between the two MDI contacts used by a duplex link channel and is referred to as common-mode-to-differential-mode impedance balance. Over the frequency range 1.0 MHz to 100.0 MHz, the common-mode-to-differential-mode impedance balance of each channel of the MDI shall exceed

$$34 - 19.2\log_{10}\left(\frac{f}{50}\right) \quad \text{dB}$$

where f is the frequency in MHz when the transmitter is transmitting random or pseudo random data. Test-mode 4 may be used to generate an appropriate transmitter output.

The balance is defined as

$$20\log_{10}\left(\frac{E_{cm}}{E_{dif}}\right)$$

where E_{cm} is an externally applied sine wave voltage as shown in Figure 40–32 and E_{dif} is the resulting waveform due only to the applied sine wave and not the transmitted data.

NOTE 1—Triggered averaging can be used to separate the component due to the applied common-mode sine wave from the transmitted data component.

NOTE 2—The imbalance of the test equipment (such as the matching of the test resistors) has to be insignificant relative to the balance requirements.

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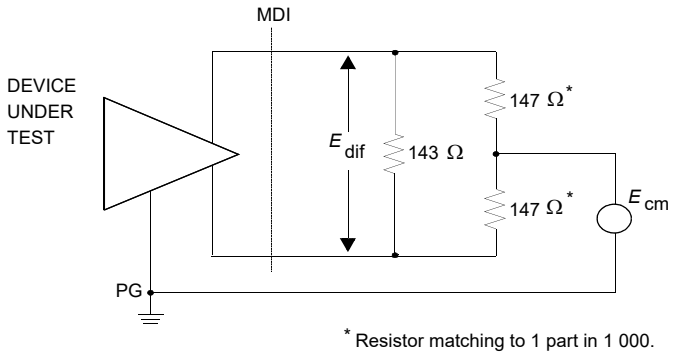

Figure 40–32—MDI impedance balance test circuit

40.8.3.3 MDI common-mode output voltage

The magnitude of the total common-mode output voltage, E_{cm_out}, on any transmit circuit, when measured as shown in Figure 40–33, shall be less than 50 mV peak-to-peak when transmitting data at frequencies above 1 MHz.

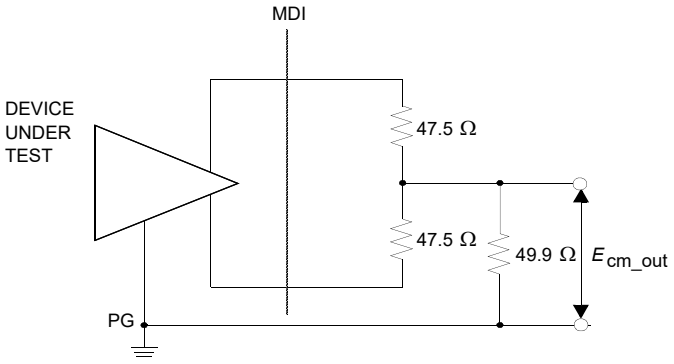

Figure 40–33—Common-mode output voltage test circuit

NOTE—The imbalance of the test equipment (such as the matching of the test resistors) should be insignificant relative to the balance requirements.

40.8.3.4 MDI fault tolerance

Each wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to any other wire within the 4-pair cable for an indefinite period of time and shall resume normal operation after the short circuit(s) are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Each wire pair shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 40–34). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

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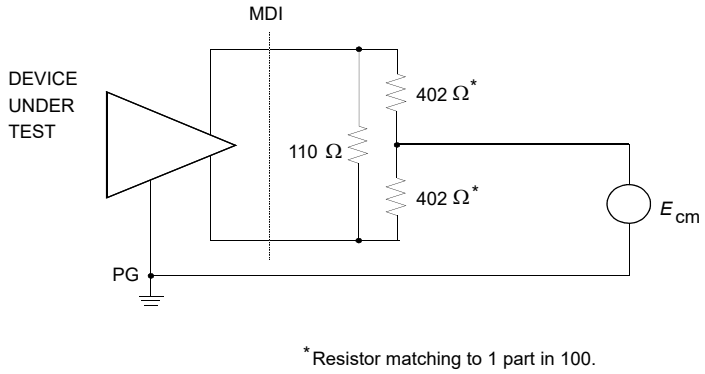

Figure 40–34—MDI fault tolerance test circuit

40.9 Environmental specifications

40.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

40.9.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cabling systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards have to be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures have to be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

40.9.2.1 Installation

It is a mandatory requirement that sound installation practice, as defined by applicable local codes and regulations, is followed in every instance in which such practice is applicable.

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40.9.2.2 Installation and maintenance guidelines

It is a mandatory requirement that, during installation and maintenance of the cabling plant, care is taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

40.9.2.3 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 1000BASE-T equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the “battery” and ringing voltages. Although there is no universal standard, the following maximums generally apply:

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.

Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 Vdc with a 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 1000BASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 1000BASE-T transmitters or receivers. Because the termination resistance likely to be present across a receiver’s input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

40.9.3 Environment

40.9.3.1 Electromagnetic emission

A system integrating the 1000BASE-T PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

40.9.3.2 Temperature and humidity

A system integrating the 1000BASE-T PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

40.10 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability in Mb/s
b) Power level in terms of maximum current drain (for external PHYs)

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c) Port type (i.e., 1000BASE-T)

d) Any applicable safety warnings

40.11 Delay constraints

In half duplex mode, proper operation of a CSMA/CD LAN demands that there be an upper bound on the propagation delays through the network. This implies that MAC, PHY, and repeater implementations conform to certain delay minima and maxima, and that network planners and administrators conform to constraints regarding the cabling topology and concatenation of devices. MAC constraints are specified in 35.2.4. Topological constraints are contained in Clause 42.

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The reference point for all MDI measurements is the peak point of the mid-cell transition corresponding to the reference code-bit, as measured at the MDI.

40.11.1 MDI to GMII delay constraints

Every 1000BASE-T PHY associated with a GMII shall comply with the bit delay constraints specified in Table 40–13 for half duplex operation and Table 40–14 for full duplex operation. These constraints apply for all 1000BASE-T PHYs. For any given implementation, the assertion and de-assertion delays on CRS shall be equal.

Table 40–13—MDI to GMII delay constraints (half duplex mode)

Sublayer measurement points	Event	Min (bit times)	Max (bit times)	Input timing reference	Output timing reference
GMII ⇔ MDI	TX_EN Sampled to MDI Output	—	84	GTX_CLK rising	1st symbol of SSD/CSReset/ CSExtend/ CSExtend_Err
	MDI input to CRS assert	—	244	1st symbol of SSD/CSReset	—
	MDI input to CRS de-assert	—	244	1st symbol of SSD/CSReset	—
	MDI input to COL assert	—	244	1st symbol of SSD/CSReset	—
	MDI input to COL de-assert	—	244	1st symbol of SSD/CSReset	—
	TX_EN sampled to CRS assert	—	16	GTX_CLK rising	—
	TX_EN sampled to CRS de-assert	—	16	GTX_CLK rising	—

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Table 40–14—MDI to GMII delay constraints (full duplex mode)

Sublayer measurement points	Event	Min (bit times)	Max (bit times)	Input timing reference	Output timing reference
GMII ⇔ MDI	TX_EN Sampled to MDI Output	—	84	GTX_CLK rising	1st symbol of SSD/CSReset/ CSExtend/ CSExtend_Err
	MDI input to RX_DV de-assert	—	244	1st symbol of CSReset	—

40.11.2 DTE delay constraints (half duplex only)

Every DTE with a 1000BASE-T PHY shall comply with the bit delay constraints specified in Table 40–15 for half duplex operation.

Table 40–15— DTE delay constraints (half duplex mode)

Sublayer measurement points	Event	Min (bit times)	Max (bit times)	Input timing reference	Output timing reference
MAC ⇔ MDI	MAC transmit start to MDI output	—	132	—	1st symbol of SSD
	MDI input to collision detect	—	292	1st symbol of SSD	—
	MDI input to MDI output (nondeferred or Jam)	—	440	1st symbol of SSD	1st symbol of SSD
	MDI Input to MDI output (worst-case non-deferred transmit)	—	440	1st symbol of SSD	1st symbol of SSD

40.11.3 Carrier de-assertion/assertion constraint (half duplex mode)

To ensure fair access to the network, each DTE operating in half duplex mode shall, additionally, satisfy the following: (MAX MDI to MAC Carrier De-assert Detect) – (MIN MDI to MAC Carrier Assert Detect) < 16 Bit Times.

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40.12 Protocol implementation conformance statement (PICS) proforma for Clause 40—Physical coding sublayer (PCS), physical medium attachment (PMA) sublayer and baseband medium, type 1000BASE-T[85]

The supplier of a protocol implementation that is claimed to conform to this clause shall complete the protocol implementation conformance statement (PICS) proforma listed in the following subclauses.

Instructions for interpreting and filling out the PICS proforma may be found in Clause 21.

40.12.1 Identification

40.12.1.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

40.12.1.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 40, Physical coding sublayer (PCS), physical medium attachment (PMA) sublayer, and baseband medium, type 1000BASE-T
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exceptions items been required? No [ ] Yes [ ] (See Clause 21—The answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

40.12.2 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*GMII	PHY associated with GMII	40.1	O	Yes [ ] No [ ]	
*DTE	DTE with PHY not associated with GMII	40.1	O	Yes [ ] No [ ]	
*EEE	EEE	40.1.3	O	Yes [ ] No [ ]	
AN	Support for Auto-Negotiation (Clause 28)	40.5.1	M	Yes [ ]	Required

[85] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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Item	Feature	Subclause	Status	Support	Value/Comment
OMS	Operation as MASTER or SLAVE	40.5.1	M	Yes [ ]	Required
*FDX	PHY supports full duplex mode	40.1	O	Yes [ ] No [ ]	
*HDX	PHY support half duplex mode	40.1	O	Yes [ ] No [ ]	
*INS	Installation / cabling	40.7	O	Yes [ ] No [ ]	Items marked with INS include installation practices and cabling specifications not applicable to a PHY manufacturer.
*AXO	Auto-Crossover	40.4.4	O	Yes [ ] No [ ]	PHY supports auto-crossover
*PD	Powered Device	40.6.1.1	O	Yes [ ] No [ ]	PHY encompasses the PI of a PD within its MDI.

40.12.3 Clause conventions

Item	Feature	Subclause	Status	Support	Value/Comment
CCO1	The values of all components in test circuits shall be	40.1.6	M	Yes [ ]	Accurate to within ±1% unless otherwise stated.

40.12.4 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Status	Support	Value/Comment
PCT1	The PCS shall	40.3.1.2	M	Yes [ ]	Implement the Data Transmission Enabling process as depicted in Figure 40–8 including compliance with the associated state variables specified in 40.3.3.
PCT2	PCS Transmit function shall	40.3.1.3	M	Yes [ ]	Conform to the PCS Transmit state diagram in Figure 40–10.
PCT3	PCS Transmit shall	40.4.5.1	M	Yes [ ]	Send code-groups according to the value assumed by the tx_mode variable.
PCT4	If the parameter config provided to the PCS by the PHY Control function via the PMA_CONFIG.indication message assumes the value MASTER, PCS Transmit shall	40.3.1.3.1	M	Yes [ ]	Employ the transmitter side-stream scrambler generator polynomial specified for use with MASTER in 40.3.1.3.1.

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Item	Feature	Subclause	Status	Support	Value/Comment
PCT5	If the parameter config provided to the PCS by the PHY Control function via the PMA_CONFIG.indication message assumes the value SLAVE, PCS Transmit shall	40.3.1.3.1	M	Yes [ ]	Employ the transmitter side-stream scrambler generator polynomial specified for use with SLAVE in 40.3.1.3.1.
PCT6	In no case shall	40.3.1.3.1	M	Yes [ ]	The scrambler state be initialized to all zeros.
PCT7	If tx_error_n=1 when (tx_enable_n * tx_enable_{n-2}) = 1, error indication is signaled by means of symbol substitution, wherein the values of Sd_n[5:0] are ignored during mapping and the symbols corresponding to the row denoted as “xmt_err” in Table 40–1 and Table 40–2 shall be used.	40.3.1.3.5	M	Yes [ ]	
PCT8	If tx_error_n=0 when the variable $csreset_n$ = 1, the convolutional encoder reset condition is normal. This condition is indicated by means of symbol substitution, where the values of Sd_n[5:0] are ignored during mapping and the symbols corresponding to the row denoted as “CSReset” in Table 40–1 and Table 40–2 shall be used.	40.3.1.3.5	M	Yes [ ]	
PCT9	If tx_error_n=1 is asserted when the variable $csreset_n$ = 1, the convolutional encoder reset indicates carrier extension. In this condition, the values of Sd_n[5:0] are ignored during mapping and the symbols corresponding to the row denoted as “CSExtend” in Table 40–1 and Table 40–2 shall be used when TXD_n = 0x0F, and the row denoted as “CSExtend_Err” in Table 40–1 and Table 40–2 shall be used when $TXD_n \neq$ 0x0F.	40.3.1.3.5	M	Yes [ ]	
PCT10	In case carrier extension with error is indicated during the first octet of CSReset, the error condition shall be encoded during the second octet of CSReset, and during the subsequent two octets of the End-of-Stream delimiter.	40.3.1.3.5	M	Yes [ ]	

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Item	Feature	Subclause	Status	Support	Value/Comment
PCT11	The symbols corresponding to the SSD1 row in Table 40–1 shall be used when (tx_enable_n) * (!tx_enable_{n-1}) = 1.	40.3.1.3.5	M	Yes [ ]	
PCT12	The symbols corresponding to the SSD2 row in Table 40–1 shall be used when (tx_enable_{n-1})* (!tx_enable_{n-2}) = 1.	40.3.1.3.5	M	Yes [ ]	
PCT13	If carrier extend error is indicated during ESD, the symbols corresponding to the ESD_Ext_Err row in Table 40–1 shall be used.	40.3.1.3.5	M	Yes [ ]	
PCT14	The symbols corresponding to the ESD1 row in Table 40–1 shall be used when (!tx_enable_{n-2}) * (tx_enable_{n-3}) = 1, in the absence of carrier extend error indication at time n.	40.3.1.3.5	M	Yes [ ]	
PCT15	The symbols corresponding to the ESD2_Ext_0 row in shall be used when (!tx_enable_{n-3}) * (tx_enable_{n-4}) * (!tx_error_n) * (!tx_error_{n-1}) = 1.	40.3.1.3.5	M	Yes [ ]	
PCT16	The symbols corresponding to the ESD2_Ext_1 row in Table 40–1 shall be used when (!tx_enable_{n-3}) * (tx_enable_{n-4}) * (!tx_error_n) * (tx_error_{n-1}) * (tx_error_{n-2}) * (tx_error_{n-3})= 1.	40.3.1.3.5	M	Yes [ ]	
PCT17	The symbols corresponding to the ESD2_Ext_2 row in Table 40–1 shall be used when (!tx_enable_{n-3}) * (tx_enable_{n-4}) * (tx_error_n) * (tx_error_{n-1}) * (tx_error_{n-2}) * (tx_error_{n-3}) * (TXD_n=0x0F)= 1, in the absence of carrier extend error indication.	40.3.1.3.5	M	Yes [ ]	
PCT18	The PCS shall	40.3.1.6	EEE:M	Yes [ ]	Conform to the Local LPI Request state diagram as depicted in Figure 40–9 including compliance with the associated state variables specified in 40.3.3.
PCT19	In the absence of the optional EEE capability, the PHY shall	40.3.3.1	!EEE:M	Yes [ ]	Operate as if the value of loc_lpi_req is FALSE.

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40.12.4.1 PCS receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR1	PCS Receive function shall	40.3.1.4	M	Yes [ ]	Conform to the PCS Receive state diagram shown in Figure 40–11a including compliance with the associated state variables as specified in 40.3.3.
PCR2	The PHY shall	40.3.1.4.2	M	Yes [ ]	Descramble the data stream and return the proper sequence of data bits RXD<7:0> to the GMII.
PCR3	For side-stream descrambling, the MASTER PHY shall employ	40.3.1.4.2	M	Yes [ ]	The receiver scrambler generator polynomial specified for MASTER operation in 40.3.1.4.2.
PCR4	For side-stream descrambling, the SLAVE PHY shall employ	40.3.1.4.2	M	Yes [ ]	The receiver scrambler generator polynomial specified for SLAVE operation in 40.3.1.4.2.
PCR5	In the absence of the optional EEE capability, the PHY shall	40.3.3.1	!EEE:M	Yes [ ]	Operate as if the value of rem_lpi_req is FALSE.

40.12.4.2 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	The PCS Reset function shall	40.3.1.1	M	Yes [ ]	Be executed any time “power on” or receipt of a request for reset from the management entity occurs, including compliance with the associated state variables as specified in 40.3.3.
PCO2	The PCS shall	40.3.1.5	M	Yes [ ]	Implement the Carrier Sense process as depicted in Figure 40–12, including compliance with the associated state variables as specified in 40.3.3.
PCO3	Symb-timer shall be generated	40.3.3.3	M	Yes [ ]	Synchronously with TX_TCLK.

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40.12.5 Physical Medium Attachment (PMA)

Item	Feature	Subclause	Status	Support	Value/Comment
PMF1	PMA Reset function shall be executed	40.4.2.1	M	Yes [ ]	At power on and upon receipt of a reset request from the management entity or from PHY Control.
PMF2	PMA Transmit shall	40.4.2.2	M	Yes [ ]	Continuously transmit onto the MDI pulses modulated by the quinary symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively.
PMF3	The four transmitters shall be driven by the same transmit clock, TX_TCLK	40.4.2.2	M	Yes [ ]	
PMF4	PMA Transmit shall	40.4.2.2	M	Yes [ ]	Follow the mathematical description given in 40.4.3.1.
PMF5	PMA Transmit shall comply with	40.4.2.2	M	Yes [ ]	The electrical specifications given in 40.6.
PMF6	When the PMA_CONFIG.indication parameter config is MASTER, the PMA Transmit function shall	40.4.2.2	M	Yes [ ]	Source the transmit clock TX_TCLK from a local clock source while meeting the transmit jitter requirements of 40.6.1.2.5.
PMF7	When the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall	40.4.2.2	M	Yes [ ]	Source the transmit clock TX_TCLK from the recovered clock of 40.4.2.5 while meeting the jitter requirements of 40.6.1.2.5.
PMF8	PMA Receive function shall translate	40.4.2.3	M	Yes [ ]	The signals received on pairs BI_DA BI_DB, BI_DC and BI_DD into the PMA_UNITDATA.indication parameter rx_symb_vector with a symbol error ratio of less than one part in 10^{10}.
PMF9	PHY Control function shall	40.4.2.4	M	Yes [ ]	Comply with the state diagram descriptions given in Figure 40–16a.
PMF10	The Link Monitor function shall	40.4.2.5	M	Yes [ ]	Comply with the state diagram shown in Figure 40–17.
PMF11	Clock Recovery function shall provide	40.4.2.6	M	Yes [ ]	Clocks suitable for signal sampling on each line so that the symbol error ratio indicated in 40.4.2.3 is achieved.
PMF12	The symbol response shall comply with	40.4.3.1	M	Yes [ ]	The electrical specifications given in 40.6.

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Item	Feature	Subclause	Status	Support	Value/Comment
PMF13	The four signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD shall be processed within the PMA Receive function to yield	40.4.3.2	M	Yes [ ]	The quinary received symbols rx_symb_vector[BI_DA], rx_symb_vector[BI_DB], rx_symb_vector[BI_DC], and rx_symb_vector[BI_DD].
PMF14	If an automatic configuration method is used, it shall	40.4.4	M	Yes [ ]	Comply with the specifications of 40.4.4.
PMF15	The PMA shall	40.4.5.1	M	Yes [ ]	Generate the config variable continuously and pass it to the PCS via the PMA_CONFIG.indication primitive.
PMF16	The variable link_det shall take the value	40.4.5.1	AXO:M	N/A [ ] Yes [ ]	TRUE or FALSE as per 40.4.4.1.
PMF17	The variable MDI_status shall take the value	40.4.5.1	AXO:M	N/A [ ] Yes [ ]	MDI or MDI-X as per Table 40–12.
PMF18	PCS Transmit shall	40.4.5.1	M	Yes [ ]	Send code-groups according to the value assumed by tx_mode.
PMF19	The A_timer shall have a period of	40.4.5.2	AXO:M	N/A [ ] Yes [ ]	1.3s ± 25%.
PMF20	The maxwait_timer timer shall expire	40.4.5.2	M	Yes [ ]	750 ms ± 10 ms if config = MASTER or 350 ms ± 5ms if config = SLAVE
PMF21	The minwait_timer timer shall expire	40.4.5.2	M	Yes [ ]	1 µs ±0.1µs after being started.
PMF22	The sample_timer shall have a period of	40.4.5.2	AXO:M	N/A [ ] Yes [ ]	62 ms ± 2ms.
PMF23	The stabilize_timer shall expire	40.4.5.2	M	Yes [ ]	1 µs ± 0.1 µs after being started.
PMF24	PHY Control shall	40.4.2.4	EEE:M	Yes [ ]	Comply with the state diagram description given in Figure 40–16a and Figure 40–16b.
PMF25	In the WAIT_QUIET state, the PHY shall	40.4.2.4	EEE:M	Yes [ ]	Be capable of correctly decoding rem_lpi_req.
PMF26	In the absence of the optional EEE capability, the PHY shall	40.4.5.1	EEE:M	Yes [ ]	Operate as if the value of loc_update_done is FALSE.
PMF27	In the absence of the optional EEE capability, the PHY shall	40.4.5.1	EEE:M	Yes [ ]	Operate as if the value of lpi_mode is OFF.
PMF28	In the absence of the optional EEE capability, the PHY shall	40.4.5.1	EEE:M	Yes [ ]	Operate as if the value of rem_lpi_req is FALSE.
PMF29	lpi_link_fail_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 90 µs and 110 µs.
PMF30	lpi_postupdate_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 2.0 µs and 3.2 µs.

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Item	Feature	Subclause	Status	Support	Value/Comment
PMF31	lpi_quiet_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 20 ms and 24 ms.
PMF32	lpi_waitwq_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 10 µs and 12 µs.
PMF33	For each transition of lpi_wake_timer_done from false to true, the wake error counter shall	40.4.5.2	EEE:M	Yes [ ]	Be incremented.
PMF34	lpi_wake_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period that does not exceed 16.5 µs.
PMF35	lpi_waketx_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 1.2_µs and 1.4 µs.
PMF36	lpi_wakemz_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 4.25 µs and 5.00 µs.
PMF37	lpi_update_timer shall	40.4.5.2	EEE:M	Yes [ ]	Have a period between 0.23 ms and 0.25 ms for a PHY configured as the MASTER and a period between 0.18 ms and 0.20 ms for a PHY configured as the SLAVE.

40.12.6 Management interface

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	All 1000BASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE.	40.5.1	M	Yes [ ]	
MF2	A 100BASE-T PHY shall	40.5.1.1	M	Yes [ ]	Use the management register definitions and values specified in Table 40–3.

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40.12.6.1 1000BASE-T Specific Auto-Negotiation Requirements

Item	Feature	Subclause	Status	Support	Value/Comment
AN1	1000BASE-T PHYs shall	40.5.1.2	M	Yes [ ]	Exchange one Auto-Negotiation Base Page, a 1000BASE-T formatted Next Page, and two 1000BASE-T Unformatted Next Pages in sequence, without interruption, as specified in Table 40–4.
AN2	The MASTER-SLAVE relationship shall be determined during Auto-Negotiation	40.5.2	M	Yes [ ]	Using Table 40–5 with the 1000BASE-T Technology Ability Next Page bit values specified in Table 40–4 and information received from the link partner.
AN3	Successful completion of the MASTER-SLAVE resolution shall	40.5.2	M	Yes [ ]	Be treated as MASTER-SLAVE configuration resolution complete.
AN4	A seed counter shall be provided to	40.5.2	M	Yes [ ]	Track the number of seed attempts.
AN5	At startup, the seed counter shall be set to	40.5.2	M	Yes [ ]	Zero.
AN6	The seed counter shall be incremented	40.5.2	M	Yes [ ]	Every time a new random seed is sent.
AN7	When MASTER-SLAVE resolution is complete, the seed counter shall be reset to 0 and bit 10.15 shall be set to logical zero.	40.5.2	M	Yes [ ]	
AN8	Maximum seed attempts before declaring a MASTER_SLAVE configuration Resolution Fault	40.5.2	M	Yes [ ]	Seven.
AN9	During MASTER_SLAVE configuration, the device with the higher seed value shall	40.5.2	M	Yes [ ]	Become the MASTER.
AN10	During MASTER_SLAVE configuration, the device with the lower seed value shall	40.5.2	M	Yes [ ]	Become the SLAVE.
AN11	Both PHYs set in manual mode to be either MASTER or SLAVE shall be treated as	40.5.2	M	Yes [ ]	MASTER-SLAVE resolution fault (failure) condition.
AN12	MASTER-SLAVE resolution fault (failure) condition shall result in	40.5.2	M	Yes [ ]	MASTER-SLAVE Configuration Resolution Fault bit (10.15) to be set to logical one.

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Item	Feature	Subclause	Status	Support	Value/Comment
AN13	MASTER-SLAVE Configuration resolution fault condition shall be treated as	40.5.2	M	Yes [ ]	MASTER-SLAVE Configuration Resolution complete.
AN14	MASTER-SLAVE Configuration resolution fault condition shall	40.5.2	M	Yes [ ]	Cause link_status_1000BASE-T to be set to FAIL.
AN15	When EEE is supported, a 1000BASE-T PHY shall	40.5.1.2	EEE:M	Yes [ ]	Exchange an additional formatted Next Page and Unformatted Next Page in sequence, without interruption, as specified in Table 40–4.

40.12.7 PMA Electrical Specifications

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	Electrical isolation	40.6.1.1	!PD:M	Yes [ ] N/A [ ]	Conforms to J.1.
PME2	The PHY shall provide electrical isolation between	40.6.1.1	PD:M	Yes [ ] N/A [ ]	All external conductors, including frame ground, and all MDI leads.
PME3	The transmitter MASTER-SLAVE timing jitter test channel shall	40.6.1.1.1	M	Yes [ ]	Be constructed by combining 100 Ω and 120 Ω cable segments that meet or exceed ISO/IEC 11801 Category 5 specifications for each pair as shown in Figure 40–19 with the lengths and additional restrictions on parameters described in Table 40–6.
PME4	The ends of the MASTER-SLAVE timing jitter test channel shall	40.6.1.1.1	M	Yes [ ]	Be connectorized with connectors meeting or exceeding ISO/IEC 11801:1995 Category 5 specifications.
PME5	The return loss of the MASTER-SLAVE timing jitter test channel shall	40.6.1.1.1	M	Yes [ ]	Meet the return loss requirements of 40.7.2.3.
PME6	The return loss of the MASTER-SLAVE timing jitter test channel shall	40.6.1.1.1	M	Yes [ ]	Meet the crosstalk requirements of 40.7.3 on each pair.
PME7	The test modes described in 40.6.1.1.2 shall be provided for testing of the transmitted waveform, transmitter distortion and transmitted jitter.	40.6.1.1.2	M	Yes [ ]	
PME8	For a PHY with a GMII interface the test modes shall be enabled by	40.6.1.1.2	M	Yes [ ]	Setting bits 9:13-15 (1000BASE-T Control Register) of the GMII Management register set as shown in Table 40–7.

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Item	Feature	Subclause	Status	Support	Value/Comment
PME9	The test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal operation.	40.6.1.1.2	M	Yes [ ]	
PME10	A PHY without a GMII shall provide a means to enable the test modes for conformance testing.	40.6.1.1.2	M	Yes [ ]	
PME11	When transmit test mode 1 is enabled, the PHY shall transmit	40.6.1.1.2	M	Yes [ ]	The sequence of data symbols specified in 40.6.1.1.2 continuously from all four transmitters.
PME12	When in test mode 1, the transmitter shall time the transmitted symbols	40.6.1.1.2	M	Yes [ ]	From a 125.00 MHz ± 0.01% clock in the MASTER timing mode.
PME13	When test mode 2 is enabled, the PHY shall transmit	40.6.1.1.2	M	Yes [ ]	The data symbol sequence {+2,–2} repeatedly on all four channels.
PME14	When in test mode 2, the transmitter shall time the transmitted symbols	40.6.1.1.2	M	Yes [ ]	From a 125.00 MHz ± 0.01% clock in the MASTER timing mode.
PME15	When transmit test mode 3 is enabled, the PHY shall transmit	40.6.1.1.2	M	Yes [ ]	The data symbol sequence {+2,–2} repeatedly on all four channels.
PME16	When in test mode 3, the transmitter shall time the transmitted symbols	40.6.1.1.2	M	Yes [ ]	From a 125 MHz ± 1% clock in the SLAVE timing mode.
PME17	When test mode 4 is enabled, the PHY shall transmit	40.6.1.1.2	M	Yes [ ]	The data symbols generated by the scrambler polynomial specified in 40.6.1.1.2.
PME18	When test mode 4 is enabled, the PHY shall	40.6.1.1.2	M	Yes [ ]	Use the bit sequences generated by the scrambler bits shown in 40.6.1.1.2 to generate the quinary symbols, s_n, as shown in Table 40–8.
PME19	When test mode 4 is enabled, the maximum-length shift register used to generate the sequences defined by this polynomial shall be	40.6.1.1.2	M	Yes [ ]	Updated once per symbol interval (8 ns).
PME20	When test mode 4 is enabled, the bit sequences, $x0_n$, $x1_n$, and $x2_n$, generated from combinations of the scrambler bits shown in 40.6.1.1.2 shall be	40.6.1.1.2	M	Yes [ ]	Used to generate the quinary symbols, s_n, as shown in Table 40–8.

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Item	Feature	Subclause	Status	Support	Value/Comment
PME21	When test mode 4 is enabled, the quinary symbol sequence shall be	40.6.1.1.2	M	Yes [ ]	Presented simultaneously to all transmitters.
PME22	When in test mode 4, the transmitter shall time the transmitted symbols	40.6.1.1.2	M	Yes [ ]	From a 125.00 MHz ± 0.01% clock in the MASTER timing mode.
PME23	The test fixtures defined in Figure 40–23, Figure 40–24, Figure 40–25, and Figure 40–26 or their functional equivalents shall be used for measuring transmitter specifications.	40.6.1.1.3	M	Yes [ ]	
PME24	The test filter used in transmitter test fixtures 1 and 3 shall	40.6.1.1.3	M	Yes [ ]	Have the continuous time transfer function specified in 40.6.1.1.3 or its discrete time equivalent.
PME25	The disturbing signal V_d shall	40.6.1.1.3	M	Yes [ ]	Have the characteristics listed in Table 40–9.
PME26	To allow for measurement of transmitted jitter in MASTER and SLAVE modes the PHY shall provide access to the 125 MHz symbol clock, TX_TCLK that times the transmitted symbols.	40.6.1.1.3	M	Yes [ ]	
PME27	To allow for measurement of transmitted jitter in MASTER and SLAVE modes the PHY shall provide a means to enable the TX_TCLK output if it is not normally enabled.	40.6.1.1.3	M	Yes [ ]	
PME28	The PMA shall	40.6.1.2	M	Yes [ ]	Provide the Transmit function specified in 40.4.2.2 in accordance with the electrical specifications of this clause.
PME29	Where a load is not specified, the transmitter shall	40.6.1.2	M	Yes [ ]	Meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.
PME30	The tolerance on the poles of the test filters used in 40.6 shall be ± 1%.	40.6.1.2	M	Yes [ ]	
PME31	When in transmit test mode 1 and observing the differential signal output at the MDI using test fixture 1, for each pair, with no intervening cable, the absolute value of the peak of the waveform at points A and B as defined in Figure 40–20 shall fall within	40.6.1.2.1	M	Yes [ ]	The range of 0.67 V to 0.82 V (0.75 V ± 0.83 dB).

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Item	Feature	Subclause	Status	Support	Value/Comment
PME32	The absolute value of the peak of the waveforms at points A and B shall	40.6.1.2.1	M	Yes [ ]	Differ by less than 1%.
PME33	The absolute value of the peak of the waveform at points C and D as defined in Figure 40–20 shall differ	40.6.1.2.1	M	Yes [ ]	From 0.5 times the average of the absolute values of the peaks of the waveform at points A and B by less than 2%.
PME34	When in transmit test mode 1 and observing the differential transmitted output at the MDI, for either pair, with no intervening cabling, the peak value of the waveform at point F as defined in Figure 40–20 shall be	40.6.1.2.2	M	Yes [ ]	Greater than 73.1% of the magnitude of the negative peak value of the waveform at point F. Point G is defined as the point exactly 500 ns after point F. Point F is defined as the point where the waveform reaches its minimum value at the location indicated in Figure 40–20.
PME35	When in transmit test mode 1 and observing the differential transmitted output at the MDI, for either pair, with no intervening cabling, the peak value of the waveform at point J as defined in Figure 40–20 shall be	40.6.1.2.2	M	Yes [ ]	Greater than 73.1% of the magnitude of the peak value of the waveform at point H. Point J is defined as the point exactly 500 ns after point H. Point H is defined as the point where the waveform reaches its maximum value at the location indicated in Figure 40–20.
PME36	When in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1, for each pair, with no intervening cable, the voltage waveforms at points A, B, C, D defined in Figure 40–20, after the normalization described within the referenced subclause, shall	40.6.1.2.3	M	Yes [ ]	Lie within the time domain template 1 defined in Figure 40–27 and the piecewise linear interpolation between the points in Table 40–10. The waveforms may be shifted in time as appropriate to fit within the template.
PME37	When in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1, for each pair, with no intervening cable, the voltage waveforms at points F and H defined in Figure 40–20, after the normalization described within the referenced subclause, shall	40.6.1.2.3	M	Yes [ ]	Lie within the time domain template 2 defined in Figure 40–27 and the piecewise linear interpolation between the points in Table 40–11. The waveforms may be shifted in time as appropriate to fit within the template.
PME38	When in test mode 4 and observing the differential signal output at the MDI using transmitter test fixture 3, for each pair, with no intervening cable, the peak distortion as defined below shall be	40.6.1.2.4	M	Yes [ ]	Less than 10 mV.

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Item	Feature	Subclause	Status	Support	Value/Comment
PME39	When in the normal mode of operation as the MASTER, the peak-to-peak value of the MASTER TX_TCLK jitter relative to an unjittered reference shall be	40.6.1.2.5	M	Yes [ ]	Less than 1.4 ns.
PME40	When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf1}(f)$ having the transfer function specified in 40.6.1.2.5, the peak-to-peak value of the resulting filtered timing jitter plus J_{txout}, shall be	40.6.1.2.5	M	Yes [ ]	Less than 0.3 ns.
PME41	When in the normal mode of operation as the SLAVE, receiving valid signals from a compliant PHY operating as the MASTER using the test channel defined in 40.6.1.1.1, with test channel port A connected to the SLAVE, the peak-to-peak value of the SLAVE TX_TCLK jitter relative to the MASTER TX_TCLK shall be	40.6.1.2.5	M	Yes [ ]	Less than 1.4 ns after the receiver is properly receiving the data and has set bit 10.13 of the GMII management register set to 1.
PME42	When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf2}(f)$, having the transfer function specified in 40.6.1.2.5, the peak-to-peak value of the resulting filtered timing jitter plus J_{txout} shall be	40.6.1.2.5	M	Yes [ ]	No more than 0.4 ns greater than the simultaneously measured peak-to-peak value of the MASTER jitter filtered by $H_{jf1}(f)$
PME43	For all jitter measurements the peak-to-peak value shall be	40.6.1.2.5	M	Yes [ ]	Measured over an unbiased sample of at least 10^5 clock edges.
PME44	For all unfiltered jitter measurements the peak-to-peak value shall be	40.6.1.2.5	M	Yes [ ]	Measured over an interval of not less than 100 ms and not more than 1 second.
PME45	The quinary symbol transmission rate on each pair of the MASTER PHY shall be	40.6.1.2.6	M	Yes [ ]	125.00 MHz ± 0.01%
PME46	The PMA shall provide the Receive function specified in 40.3.1.4 in accordance with the electrical specifications of this clause.	40.6.1.3	M	Yes [ ]	
PME47	The patch cabling and interconnecting hardware used in test configurations shall be	40.6.1.3	M	Yes [ ]	Within the limits specified in 40.7.

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Item	Feature	Subclause	Status	Support	Value/Comment
PME48	Differential signals received on the receive inputs that were transmitted within the specifications given in 40.6.1.2 and have then passed through a link compatible with 40.7, shall be translated into	40.6.1.3.1	M	Yes [ ]	One of the PMA_UNITDATA.indication messages with a 4-D symbol rate error less than 10^{-10} and sent to the PCS after link bring-up. Since the 4-D symbols are not accessible, this specification shall be satisfied by a frame error ratio less than 10^{-7} for 125 octet frames.
PME49	The receive feature shall	40.6.1.3.2	M	Yes [ ]	Properly receive incoming data with a 5-level symbol rate within the range 125.00 MHz ± 0.01%.
PME50	The signal generator for the common-mode test shall be	40.6.1.3.3	M	Yes [ ]	Capable of providing a sine wave signal of 1 MHz to 250 MHz.
PME51	While sending data from the transmitter the receiver shall	40.6.1.3.3	M	Yes [ ]	Send the proper PMA_UNITDATA.indication messages to the PCS as the signal generator frequency is varied from 1 MHz to 250 MHz.
PME52	While receiving data from a transmitter specified in 40.6.1.2 through a link segment specified in 40.7 connected to all MDI duplex channels, a receiver shall	40.6.1.3.4	M	Yes [ ]	Send the proper PMA_UNITDATA.indication message to the PCS when any one of the four pairs is connected to a noise source as described in Figure 40–29.
PME53	The alien crosstalk test specified in 40.6.1.3.4 shall be satisfied by	40.6.1.3.4	M	Yes [ ]	A frame error ratio of less than 10^{-7} for 125 octet frames
PME54	The noise source shall be	40.6.1.3.4	M	Yes [ ]	Connected to one of the MDI inputs using Category 5 balanced cable of a maximum length of 0.5 m.
PME55	The unfiltered jitter requirements shall	40.6	EEE:M	Yes [ ]	Be satisfied during the LPI mode, with the exception that clock edges corresponding to the WAIT_QUIET, QUIET, WAKE, and WAKE_SILENT states are not considered in the measurement.
PME56	For a MASTER PHY operating in the LPI mode, the unjittered reference shall	40.6	EEE:M	Yes [ ]	Be continuous.
PME57	The transmit levels of the Idle symbols transmitted during the WAKE state shall	40.6.1.2.7	EEE:M	Yes [ ]	Exceed 65% of the transmit levels of compliant Idle symbols for a period of at least 500 ns.

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Item	Feature	Subclause	Status	Support	Value/Comment
PME58	The PHY shall	40.6.1.2.7	EEE:M	Yes [ ]	Achieve compliant operation upon entry to the WAKE_TRAINING state (see Figure 40–16b).
PME59	PMA Receive function shall	40.6.1.3.5	EEE:M	Yes [ ]	Convey an indicator of signal presence, referred to as signal_detect, to the PMA PHY Control function.
PME60	The value of signal_detect shall	40.6.1.3.5	EEE:M	Yes [ ]	Be set to TRUE within 0.5 µs of the receipt of a wake signal meeting the requirements of 40.6.1.2.7.
PME61	The value of signal_detect shall	40.6.1.3.5	EEE:M	Yes [ ]	Be set to FALSE within 0.5 µs of the receipt of a continuous sequence of zeros.

40.12.8 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	All implementations of the balanced cabling link shall	40.7.1	INS:M	N/A [ ] Yes [ ]	Be compatible at the MDI.
LKS2	1000BASE-T links shall be compliant	40.7.1	INS:M	N/A [ ] Yes [ ]	With Class D performance requirements, as specified by ISO/IEC 11801:1995.
LKS3	Link segment testing shall be conducted using	40.7.2	INS:M	N/A [ ] Yes [ ]	Source and load impedances of 100 Ω.
LKS4	The tolerance on the poles of the test filter used in this section shall be	40.7.2	INS:M	N/A [ ] Yes [ ]	± 1%.
LKS5	The insertion loss of each duplex channel shall be	40.7.2.1	INS:M	N/A [ ] Yes [ ]	Less than $2.1 f^{0.529} + 0.4/f$ (dB) at all frequencies from 1 MHz to 100 MHz. This includes the attenuation of the balanced cabling pairs, connector losses, and patch cord losses of the duplex channel.
LKS6	The insertion loss specification shall be met when	40.7.2.1	INS:M	N/A [ ] Yes [ ]	The duplex channel is terminated in 100 Ω.
LKS7	The return loss of each duplex channel shall be	40.7.2.3	INS:M	N/A [ ] Yes [ ]	As specified in 40.7.2.3 at all frequencies from 1 MHz to 100 MHz.
LKS8	The reference impedance for return loss measurement shall be	40.7.2.3	INS:M	N/A [ ] Yes [ ]	100 Ω.

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Item	Feature	Subclause	Status	Support	Value/Comment
LKS9	The NEXT loss between duplex channel pairs of a link segment shall be	40.7.3.1.1	INS:M	N/A [ ] Yes [ ]	At least $27.1 - 16.8\log_{10}(f/100)$ (where f is the frequency in MHz over the frequency range 1 MHz to 100 MHz.)
LKS10	The worst case ELFEXT loss between duplex channel pairs of a link segment shall be	40.7.3.2	INS:M	N/A [ ] Yes [ ]	Greater than $17 - 20\log_{10}(f/100)$ dB (where f is the frequency in MHz) over the frequency range 1 MHz to 100 MHz.
LKS11	The Power Sum loss between a duplex channel and the three adjacent disturbers shall be	40.7.3.2.2	INS:M	N/A [ ] Yes [ ]	Greater than $14.4 - 20\log_{10}(f/100)$ dB where f is the frequency in MHz over the frequency range of 1 MHz to 100 MHz.
LKS12	The propagation delay of a link segment shall	40.7.4.1	INS:M	N/A [ ] Yes [ ]	Not exceed 570 ns at all frequencies from 2 MHz to 100 MHz.
LKS13	The difference in propagation delay, or skew, between all duplex channel pair combinations of a link segment under all conditions shall not exceed	40.7.4.2	INS:M	N/A [ ] Yes [ ]	50 ns at all frequencies between 2 MHz and 100 MHz.
LKS14	Once installed, the skew between pairs due to environmental conditions shall not vary	40.7.4.2	INS:M	N/A [ ] Yes [ ]	More than ± 10 ns.

40.12.9 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	40.8.1	M	Yes [ ]	8-Way connector as per IEC 60603-7:1990.
MDI2	Connector used on cabling	40.8.1	INS:M	N/A [ ] Yes [ ]	Plug.
MDI3	Connector used on PHY	40.8.1	M	Yes [ ]	Jack (as opposed to plug).
MDI4	MDI connector	40.8.2	M	Yes [ ]	A PHY that implements the crossover function shall be marked with the graphical symbol X.
MDI5	The MDI connector (jack) when mated with a balanced cabling connector (plug) shall meet	40.8.3	INS:M	N/A [ ] Yes [ ]	The electrical requirements for Category 5 connecting hardware for use with 100 Ω Category 5 cable as specified in ISO/IEC 11801:1995.

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Item	Feature	Subclause	Status	Support	Value/Comment
MDI6	The mated MDI connector and balanced cabling connector shall	40.8.3	INS:M	N/A [ ] Yes [ ]	Not have a FEXT loss greater than $40 - 20\log_{10}(f/100)$ over the frequency range 1 MHz to 100 MHz between all contact pair combinations shown in Table 40–12.
MDI7	No spurious signals shall be emitted onto the MDI when the PHY is held in power down mode as defined in 22.2.4.1.5, independent of the value of TX_EN, when released from power down mode, or when external power is first applied to the PHY.	40.8.3	M	Yes [ ]	
MDI8	The differential impedance as measured at the MDI for each transmit/receive channel shall be such that	40.8.3.1	M	Yes [ ]	Any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 Ω ± 15% is at least 16 dB over the frequency range of 2.0 MHz to 40 MHz and at least $10 - 20\log_{10}(f/80)$ dB over the frequency range 40 MHz to 100 MHz (f in MHz).
MDI9	This return loss shall be maintained	40.8.3.1	M	Yes [ ]	At all times when the PHY is transmitting data or control symbols.
MDI10	The common-mode to differential-mode impedance balance of each transmit output shall exceed	40.8.3.2	M	Yes [ ]	The value specified by the equations specified in 40.8.3.2. Test mode 4 may be used to generate an appropriate transmitter output.
MDI11	The magnitude of the total common-mode output voltage, E_{cm_out}, on any transmit circuit, when measured as shown in Figure 40–33, shall be	40.8.3.3	M	Yes [ ]	Less than 50 mv peak-to-peak when transmitting data.
MDI12	Each wire pair of the MDI shall	40.8.3.4	M	Yes [ ]	Withstand without damage the application of short circuits across the MDI port for an indefinite period of time without damage.
MDI13	Each wire pair of the MDI shall resume	40.8.3.4	M	Yes [ ]	Normal operation after such faults are removed.

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Item	Feature	Subclause	Status	Support	Value/Comment
MDI14	The magnitude of the current through the short circuit specified in PME64 shall not exceed	40.8.3.4	M	Yes [ ]	300 mA.
MDI15	Each wire pair shall withstand without damage	40.8.3.4	M	Yes [ ]	A 1000 V common-mode impulse of either polarity (E_{cm} as indicated in Figure 40–34).
MDI16	The shape of the impulse shall be	40.8.3.4	M	Yes [ ]	0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

40.12.10 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ENV1	Conformance to safety specifications	40.9.1	M	Yes [ ]	Conforms to J.2.
ENV2	Installation practice	40.9.2.1	INS:M	N/A [ ] Yes [ ]	Sound practice, as defined by applicable local codes.
ENV3	Care taken during installation to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.	40.9.2.2	INS:M	N/A [ ] Yes [ ]	
ENV4	1000BASE-T equipment shall be capable of withstanding a telephone battery supply from the outlet as described in 40.9.2.3.	40.9.2.3	M	Yes [ ]	
ENV5	A system integrating the 1000BASE-T PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.	40.9.3.1	INS:M	N/A [ ] Yes [ ]	

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40.12.11 Timing requirements

Item	Feature	Subclause	Status	Support	Value/Comment
TR1	Every 1000BASE-T PHY associated with a GMII shall	40.11.1	M	Yes [ ]	Comply with the bit delay constraints specified in Table 40–13 for half duplex operation and Table 40–14 for full duplex operation. These constraints apply for all 1000BASE-T PHYs.
TR2	For any given implementation, the assertion delays on CRS shall	40.11.1	M	Yes [ ]	Be equal.
TR3	Every DTE with a 1000BASE-T PHY shall	40.11.2	M	Yes [ ]	Comply with the bit delay constraints specified in Table 40–15.
TR4	To ensure fair access to the network, each DTE operating in half duplex mode shall, additionally, satisfy the following:	40.11.3	M	Yes [ ]	(MAX MDI to MAC Carrier De-assert Detect) – (MIN MDI to MAC Carrier Assert Detect) < 16 Bit Times.

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41. Repeater for 1000 Mb/s baseband networks

NOTE—This repeater is not recommended for new installations. Since September 2011, maintenance changes are no longer being considered for this clause.

41.1 Overview

41.1.1 Scope

Clause 41 defines the functional and electrical characteristics of a repeater for use with Ethernet 1000 Mb/s baseband networks. A repeater for any other Ethernet network type is beyond the scope of this clause. The relationship of this standard to the OSI Reference Model is shown in Figure 41–1. The purpose of the repeater is to provide a simple, inexpensive, and flexible means of coupling two or more segments.

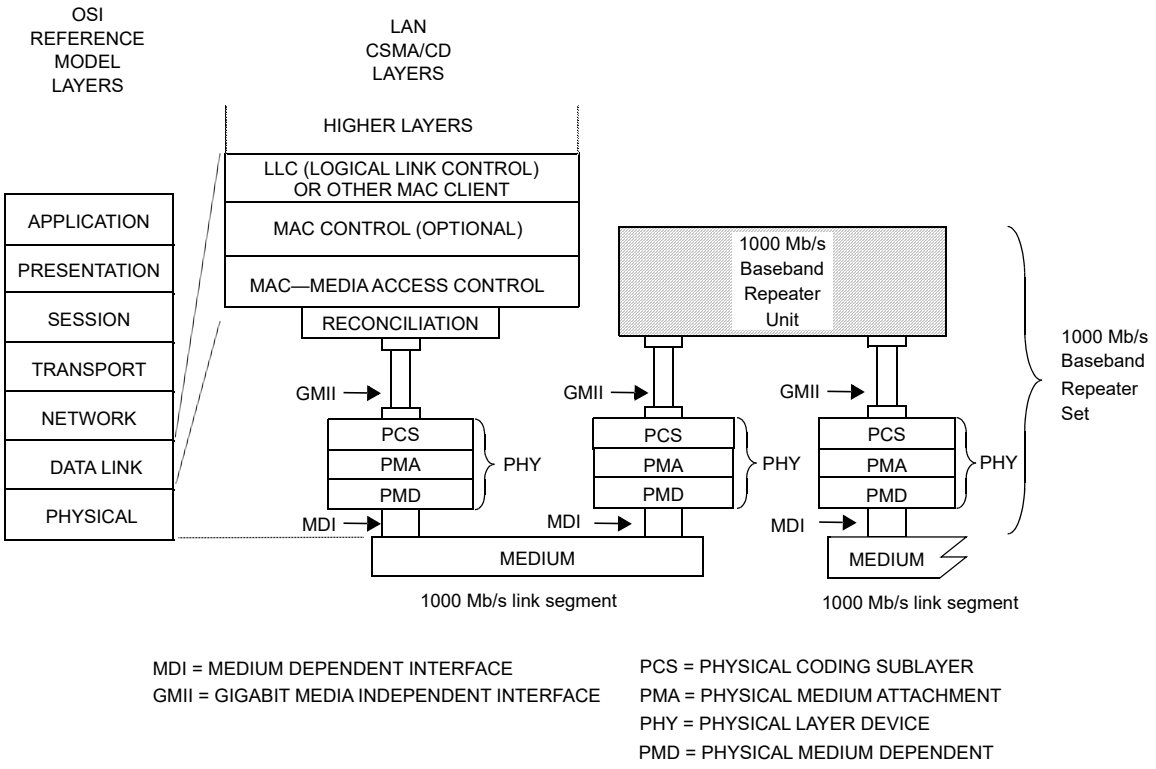

Figure 41–1—1000 Mb/s repeater set relationship to the ISO/IEC OSI reference model

41.1.1.1 Repeater set

Repeater sets are an integral part of all 1000 Mb/s baseband networks with more than two DTEs and are used to extend the physical system topology by providing a means of coupling two or more segments. A single repeater set is permitted within a single collision domain to provide the maximum connection path length. Allowable topologies contain only one operative signal path between any two points on the network. A repeater set is not a station and does not count toward the overall limit of 1024 stations on a network.

A repeater set can receive and decode data from any segment under worst-case noise, timing, and signal amplitude conditions. It retransmits the data to all other segments attached to it with timing, amplitude, and coding restored. The retransmission of data occurs simultaneously with reception. If a collision occurs, the repeater set propagates the collision event throughout the network by transmitting a Jam signal. A repeater

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set also provides a degree of protection to a network by isolating a faulty segment's carrier activity from propagating through the network.

41.1.1.2 Repeater unit

A repeater unit is a subset of a repeater set containing all the repeater-specific components and functions, exclusive of PHY components and functions. A repeater unit connects to the PHYs using the Gigabit Media Independent Interface (GMII) defined in Clause 35.

41.1.2 Application perspective

This subclause states the broad objectives and assumptions underlying the specification defined through Clause 41.

41.1.2.1 Objectives

a) Provide physical means for coupling two or more LAN segments at the Physical Layer.
b) Support interoperability of independently developed physical, electrical, and optical interfaces.
c) Provide a communication channel with a mean bit error ratio, at the physical service interface equivalent to that for the attached PHY.
d) Provide for ease of installation and service.
e) Ensure that fairness of DTE access is not compromised.
f) Provide for low-cost networks, as related to both equipment and cabling.

41.1.2.2 Compatibility considerations

All implementations of the repeater set shall be compatible at the MDI. The repeater set is defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the repeater set in an application-dependent manner provided the appropriate PHY specifications are met.

41.1.2.2.1 Internal segment compatibility

Implementations of the repeater set that contain a MAC layer for network management or other purposes, irrespective of whether they are connected through an exposed repeater port or are internally ported, shall conform to the requirements of Clause 30 on that port if repeater management is implemented.

41.1.3 Relationship to PHY

A close relationship exists between Clause 41 and the GMII clause (Clause 35) and the PHY clauses (Clauses 36–39 for 1000BASE-X PHYs and Clause 40 for 1000BASE-T PHYs). The PHY's PMA, PCS, and MDI specification provide the actual medium attachment, including drivers, receivers, and Medium Interface Connectors for the various supported media. The repeater clause does not define a new PHY; it utilizes the existing PHYs complete and without modification. The repeater_mode variable in each PHY is set, so that the CRS signal of the GMII is asserted only in response to receive activity (see 36.2.5.1.3).

41.2 Repeater functional specifications

A repeater set provides the means whereby data from any segment can be received under worst-case noise, timing, and amplitude conditions and then retransmitted with timing and amplitude restored to all other attached segments. Retransmission of data occurs simultaneously with reception. If a collision occurs, the repeater set propagates the collision event throughout the network by transmitting a Jam signal. If an error is

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received by the repeater set, no attempt is made to correct it and it is propagated throughout the network by transmitting an explicit error code.

The repeater set provides the following functional capability to handle data flow between ports:

a) *Signal restoration.* Provides the ability to restore the timing and amplitude of the received signal prior to retransmission.
b) *Transmit function.* Provides the ability to output signals on the appropriate port and encoded appropriately for that port. Details of signal processing are described in the specifications for the PHYs.
c) *Receive function.* Provides the ability to receive input signals presented to the ports. Details of signal processing are described in the specifications for the PHYs.
d) *Data-Handling function.* Provides the ability to transfer code-elements between ports in the absence of a collision.
e) *Received Event-Handling requirement.* Provides the ability to derive a carrier signal from the input signals presented to the ports.
f) *Collision-Handling function.* Provides the ability to detect the simultaneous reception of frames at two or more ports and then to propagate a Jam message to all connected ports.
g) *Error-Handling function.* Provides the ability to prevent substandard links from generating streams of false carrier and interfering with other links.
h) *Partition function.* Provides the ability to prevent a malfunctioning port from generating an excessive number of consecutive collisions and indefinitely disrupting data transmission on the network.
i) *Receive Jabber function.* Provides the ability to interrupt the reception of abnormally long streams of input data.

41.2.1 Repeater functions

The repeater set shall provide the Signal Restoration, Transmit, Receive, Data Handling, Received Event Handling, Collision Handling, Error Handling, Partition, and Receive Jabber functions. The repeater is transparent to all network acquisition activity and to all DTEs. The repeater will not alter the basic fairness criterion for all DTEs to access the network or weigh it toward any DTE or group of DTEs regardless of network location.

The Transmit and Receive functional requirements are specified by the PHY clauses, Clause 40 for 1000BASE-T and Clauses 36 to 39 for 1000BASE-X.

41.2.1.1 Signal restoration functional requirements

41.2.1.1.1 Signal amplification

The repeater set (including its integral PHYs) shall ensure that the amplitude characteristics of the signals at the MDI outputs of the repeater set are within the tolerances of the specification for the appropriate PHY type. Therefore, any loss of signal-to-noise ratio due to cable loss and noise pickup is regained at the output of the repeater set as long as the incoming data is within system specification.

41.2.1.1.2 Signal wave-shape restoration

The repeater set (including its integral PHYs) shall ensure that the wave-shape characteristics of the signals at the MDI outputs of a repeater set are within the specified tolerance for the appropriate PHY type. Therefore, any loss of wave-shape due to PHYs and media distortion is restored at the output of the repeater set.

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41.2.1.1.3 Signal retiming

The repeater set (including its integral PHYs) shall ensure that the timing of the encoded data output at the MDI outputs of a repeater set are within the specified tolerance for the appropriate PHY type. Therefore, any receive jitter from the media is removed at the output of the repeater set.

41.2.1.2 Data-handling functional requirements

41.2.1.2.1 Data frame forwarding

The repeater set shall ensure that the data frame received on a single input port is distributed to all other output ports in a manner appropriate for the PHY type of that port. The data frame is that portion of the packet after the SFD and before the end-of-frame delimiter. The only exceptions to this rule are when contention exists among any of the ports, when the receive port is partitioned as defined in 41.2.1.6, when the receive port is in the Jabber state as defined in 41.2.1.7, or when the receive port is in the Link Unstable state as defined in 41.2.1.5.1. Between unpartitioned ports, the rules for collision handling (see 41.2.1.4) take precedence.

41.2.1.2.2 Received code violations

The repeater set shall ensure that any code violations received while forwarding a packet are propagated to all outgoing segments. These code violations shall be replaced by a code-group that provide an explicit indication that an error was received, as appropriate for the outgoing PHY type. Once a received code violation has been replaced by a code-group indicating a receive error, this substitution shall continue for the remainder of the received event regardless of its content. The only exception to this rule is when contention exists among any of the ports, where the rules for collision handling (see 41.2.1.4) then take precedence.

41.2.1.3 Received event-handling functional requirements

41.2.1.3.1 Received event handling

For all its ports, the repeater set shall detect received events by monitoring the port for any assertion of the GMII CRS signal that is the result of receive activity. The repeater_mode variable in the PHY shall be set to ensure that the CRS signal is not asserted in response to transmit activity. Received events include both the data frame and any encapsulation of the data frame such as Preamble, SFD, start and end of packet delimiters, carrier extension symbols, and error propagation symbols. A received event is exclusive of the IDLE pattern. Upon detection of a received event from one port, the repeater set shall repeat all received signals in the data frame from that port to the other ports as described in Figure 41–2.

41.2.1.3.2 Preamble regeneration

The repeater set shall output preamble as appropriate for the outgoing PHY type followed by the SFD. The duration of the output preamble shall not vary more than 8 bit times from the duration of the received preamble.

41.2.1.3.3 Start-of-packet propagation delay

The start-of-packet propagation delay for a repeater set is the time delay between the start of a received event on a repeated-from (input) port to the start of transmit on the repeated-to (output) port (or ports). This parameter is referred to as the SOP delay, and is measured at the MDI of the repeater ports. The maximum value of this delay is constrained such that the sum of the SOP delay and SOJ delay shall not exceed the value specified in 41.2.1.4.3.

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41.2.1.3.4 Start-of-packet variability

The start-of-packet variability for a repeater set is defined as the total worst-case difference between start-of-packet propagation delays for successive received events separated by 112 bit times or less at the same input port. The variability shall be less than or equal to 16 bit times.

41.2.1.4 Collision-handling functional requirements

41.2.1.4.1 Collision detection

The repeater performs collision detection by monitoring all its enabled input ports for received events. When the repeater detects received events on more than one input port, it shall enter a collision state and transmit the Jam message to all of its output ports.

41.2.1.4.2 Jam generation

While a collision is occurring between any of its ports, the repeater unit shall transmit the Jam message to all of the ports. The Jam message shall be transmitted in accordance with the repeater state diagram in Figure 41–2. The Jam message is signaled across the GMII using the Transmit Error Propagation encoding if the collision is detected during Normal Data Transmission, or using the Carrier Extend Error encoding if the collision is detected during Carrier Extension.

41.2.1.4.3 Start-of-collision-jam propagation delay

The start-of-collision Jam propagation delay for a repeater set is the time delay between the start of the second received event (that results in a collision) to arrive at its port and the start of Jam out on all ports. This parameter is referred to as the SOJ delay, and is measured at the MDI of the repeater ports. The sum of the SOP delay and SOJ delay shall not exceed 976 bit times (BT).

41.2.1.4.4 Cessation-of-collision Jam propagation delay

The cessation-of-collision Jam propagation delay for a repeater set is the time delay between the end of the received event that creates a state such that Jam should end at a port and the end of Jam at that port. The states of the input signals that should cause Jam to end are covered in detail in the repeater state diagram in Figure 41–2. This parameter is referred to as the EOJ delay. This delay shall not exceed the SOP delay.

41.2.1.5 Error-handling functional requirements

41.2.1.5.1 Carrier integrity functional requirements

It is desirable that the repeater set protect the network from some transient fault conditions that would disrupt network communications. Potential likely causes of such conditions are DTE and repeater power-up and power-down transients, cable disconnects, and faulty wiring.

The repeater unit shall provide a self-interrupt capability at each port, as described in Figure 41–5, to prevent a segment's spurious carrier activity from propagating through the network.

At each port the repeater shall count consecutive false carrier events signaled across the GMII. The count shall be incremented on each false carrier event and shall be reset on reception of a valid carrier event. In addition, each port shall have a false carrier timer, which is enabled at the beginning of a false carrier event and reset at the conclusion of such an event. A repeater unit shall transmit the Jam signals to all ports for the duration of the false carrier event or until the duration of the event exceeds the time specified by the false_carrier_timer (see 41.2.2.1.4), whichever is shorter. The Jam message shall be transmitted in accordance with the repeater state diagram in Figure 41–2. The LINK UNSTABLE condition shall be

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detected when the False Carrier Event Count equals the value FCELimit (see 41.2.2.1.1) or the duration of a false carrier event exceeds the time specified by the false_carrier_timer. In addition, the LINK UNSTABLE condition shall be detected upon power-up reset.

Upon detection of LINK UNSTABLE at a port, the repeater unit shall perform the following:

a) Inhibit sending further messages from that port to the repeater unit.
b) Inhibit sending further output messages to that port from the repeater unit.
c) Continue to monitor activity on that port.

The repeater unit shall exit the LINK UNSTABLE condition at the port when one of the following is met:

a) The repeater has detected no activity (Idle) for more than the time specified by ipg_timer plus idle_timer (see 41.2.2.1.4) on port X.
b) A valid carrier event with a duration greater than the time specified by valid_carrier_timer (see 41.2.2.1.4) has been received, preceded by no activity (Idle) for more than the time specified by ipg_timer (see 41.2.2.1.4) on port X.

The false_carrier_timer duration is longer than the maximum round-trip latency from a repeater to a DTE, but less than a slot time. This allows a properly functioning DTE to respond to the Jam message by detecting collision and terminating the transmission prior to the expiration of the timer. The upper limit on the false_carrier_timer prevents the Jam message from exceeding the maximum fragment size.

The combination of the ipg_timer, idle_timer, and valid_carrier_timer filter transient activity that can occur on a link during power cycles or mechanical connection. The duration of the ipg_timer is greater than two-thirds of the minimum IPG, and less than the minimum IPG less some shrinkage. The idle_timer is specified as approximately 320 μs based upon empirical data on such transients. The valid_carrier_timer duration is less than the duration of a minimum valid carrier event, but long enough to filter most spurious carrier events (note that there can be no valid collision fragments on an isolated link in a single repeater topology). The range of the valid_carrier_timer is specified to be the same as the false_carrier_timer range for the convenience of implementations.

41.2.1.5.2 Speed handling

If the PHY has the capability of detecting speeds other than 1000 Mb/s, then the repeater set shall have the capability of blocking the flow of non-1000 Mb/s signals. The incorporation of 1000 Mb/s and 100 Mb/s or 10 Mb/s repeater functionality within a single repeater set is beyond the scope of this standard.

41.2.1.6 Partition functional requirements

It is desirable that the repeater set protect the network from some fault conditions that would disrupt network communications. A potentially likely cause of this condition could be due to a cable fault.

The repeater unit shall provide a self-interrupt capability at each port, as described in Figure 41–4, to prevent a faulty segment's carrier activity from propagating through the network. The repeater unit shall count consecutive collision events at each port. The count shall be incremented on each transmission that suffers a collision and shall be reset on a successful transmission or reception. If this count equals or exceeds the value CELimit (see 41.2.2.1.1), the Partition condition shall be detected. In addition, the partition condition shall be detected due to a carrier event of duration in excess of jabber_timer in which a collision has occurred.

Upon detection of Partition at a port, the repeater unit shall perform the following:

a) Inhibit sending further input messages from that port to the repeater unit.

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b) Continue to output messages to that port from the repeater unit.
c) Continue to monitor activity on that port.

The repeater unit shall reset the Partition function at the port when one of the following conditions is met:

— On power-up reset.
— The repeater has detected activity on the port for more than the number of bits specified for no_collision_timer (see 41.2.2.1.4) without incurring a collision.
— The repeater has transmitted on the port for more than the number of bits specified for no_collision_timer (see 41.2.2.1.4) without incurring a collision.

The no_collision_timer duration is longer than the maximum round-trip latency from a repeater to a DTE (maximum time required for a repeater to detect a collision), and less than the minimum valid carrier event duration (slot time plus header_size minus preamble shrinkage).

41.2.1.7 Receive jabber functional requirements

The repeater unit shall provide a self-interrupt capability at each port, as described in Figure 41–3, to prevent an illegally long reception of data from propagating through the network. The repeater unit shall provide a window of duration jabber_timer bit times (see 41.2.2.1.4) during which the input messages from a port may be passed on to other repeater unit functions. If a reception exceeds this duration, the jabber condition shall be detected.

Upon detection of the jabber condition at a port, the repeater unit shall perform the following:

a) Inhibit sending further input messages from that port to the repeater unit.
b) Inhibit sending further output messages to that port from the repeater unit.

The repeater shall reset the Jabber function at the port, and re-enable data transmission and reception, when either one of the following conditions is met:

— On power-up reset.
— When carrier is no longer detected at that port.

The lower bound of the jabber_timer is longer than the carrier event of a maximum length burst. The upper bound is large enough to permit a wide variety of implementations.

41.2.2 Detailed repeater functions and state diagrams

A precise algorithmic definition is given in this subclause, providing a complete procedural model for the operation of a repeater, in the form of state diagrams. Note that whenever there is any apparent ambiguity concerning the definition of repeater operation, the state diagrams should be consulted for the definitive statement.

The model presented in this subclause is intended as a primary specification of the functions to be provided by any repeater unit. It is important to distinguish, however, between the model and a real implementation. The model is optimized for simplicity and clarity of presentation, while any realistic implementation should place heavier emphasis on such constraints as efficiency and suitability to a particular implementation technology.

It is the functional behavior of any repeater set implementation that is expected to match the standard, not the internal structure. The internal details of the procedural model are useful only to the extent that they help specify the external behavior clearly and precisely. For example, the model uses a separate Receive Port Jabber state diagram for each port. However, in actual implementation, the hardware may be shared.

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The notation used in the state diagram follows the conventions of 1.2.1. Note that transitions shown without source states are evaluated at the completion of every state and take precedence over other transition conditions.

41.2.2.1 State diagram variables

41.2.2.1.1 Constants

CELimit

The number of consecutive Collision Events that have to occur before a segment is partitioned.

Values: Positive integer greater than 60.

FCELimit

The number of consecutive False Carrier Events that have to occur before a segment is isolated.

Value: 2.

41.2.2.1.2 Variables

begin

The Interprocess flag controlling state diagram initialization values.

Values: true
false

CRS(X), RXD(X), RX_DV(X), RX_ER(X), TXD(X), TX_EN(X), TX_ER(X)

GMII signals received from or sent to the PHY at port X (see Clause 35). The repeater_mode variable in the PHY is set to ensure that the CRS(X) signal is asserted in response to receive activity only.

RXERROR(X)

A combination of the GMII signal encodings indicating that the PHY has detected a Data Error, Carrier Extend Error, or False Carrier Error.

Value: RXERROR(X) ⇐ ((RX_ER(X) = true) *
((RX_DV(X) = true) + (RXD(X) = FalseCarrier) + (RXD(X) = CarrierExtendError)))

TX(X)

A combination of the GMII signal encodings indicating that port X is transmitting a frame.

Value: TX(X) ⇐ ((TX_EN(X) = true) + (TX_ER(X) = true))

isolate(X)

Flag from Carrier Integrity state diagram for port X, which determines whether a port should be enabled or disabled.

Values: true; the Carrier Integrity Monitor has determined the port should be disabled.
false; the Carrier Integrity Monitor has determined the port should be enabled.

force_jam(X)

Flag from Carrier Integrity state diagram for port X, which causes the Repeater Unit to enter the Jam state.

Values: true; the port is in the False Carrier state.
false; the port is not in the False Carrier state.

jabber(X)

Flag from Receive Timer state diagram for port X which indicates that the port has received

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excessive length activity.

Values: true; port has exceeded the continuous activity limit.
false; port has not exceeded the continuous activity limit.

link_status(X)

Indication from the Auto-Negotiation process (Clauses 28 and 37) that Auto-Negotiation has completed and the priority resolution function has determined that the link will be operated in half duplex mode.

Values: OK; the link is operational in half duplex mode.
FAIL; the link is not operational in half duplex mode.

partition(X)

Flag from Partition state diagram for port X, which determines whether a port receive path should be enabled or disabled.

Values: true; port has exceeded the consecutive collision limit.
false; port has not exceeded the consecutive collision limit.

41.2.2.1.3 Functions

port(Test)

A function that returns the designation of a port passing the test condition. For example, port(CRS = true) returns the designation: X for a port for which CRS is asserted. If multiple ports meet the test condition, the Port function will be assigned one and only one of the acceptable values.

41.2.2.1.4 Timers

All timers operate in the same fashion. A timer is reset and starts timing upon entering a state where “start x_timer” is asserted. At time “x” after the timer has been started, “x_timer_done” is asserted and remains asserted until the timer is reset. At all other times, “x_timer_not_done” is asserted.

When entering a state where “start x_timer” is asserted, the timer is reset and restarted even if the entered state is the same as the exited state.

The timers used in the repeater state diagrams are defined as follows:

false_carrier_timer

Timer for length of false carrier (41.2.1.5.1) that has to be present to set isolate(X) to true. The timer is done when it reaches 3600–4000 BT.

idle_timer

Timer for length of time without carrier activity that has to be present to set isolate(X) to false. The timer is done when it reaches 240 000–400 000 BT.

ipg_timer

Timer for length of time without carrier activity that has to be present before carrier integrity tests (41.2.1.5.1) are re-enabled. The timer is done when it reaches 64–86 BT.

jabber_timer

Timer for length of carrier which has to be present before the Jabber state is entered (41.2.1.7). The timer is done when it reaches 80 000–150 000 BT.

no_collision_timer

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Timer for length of packet without collision before partition(X) is set to false (41.2.1.6). The timer is done when it reaches 3600–4144 BT.

valid_carrier_timer

Timer for length of valid carrier that has to be present to cause isolate(X) to be set to false at the end of the carrier event. The timer is done when it reaches 3600–4000 BT.

41.2.2.1.5 Counters

CE(X)

Consecutive port Collision Event count for port X. Partitioning occurs on a terminal count of CELimit being reached.

Values: Non-negative integers up to a terminal count of CELimit.

FCE(X)

False Carrier Event count for port X. Isolation occurs on a terminal count of FCELimit being reached.

Values: Non-negative integers up to a terminal count of FCELimit.

41.2.2.1.6 Port designation

Ports are referred to by number. Port information is obtained by replacing the X in the desired function with the number of the port of interest. Ports are referred to in general as follows:

X

Generic port designator. When X is used in a state diagram, its value is local to that diagram and not global to the set of state diagrams.

N

Identifies the port that caused the exit from the IDLE or JAM states of Figure 41–2. The value is assigned in the term assignment statement on the transition out of these states (see 1.2.1 for State Diagram Conventions).

ALL

Indicates all repeater ports are to be considered. The test passes when all ports meet the test conditions.

ALLXJIPN

The test passes when all ports, excluding those indicated by J, I, P, or N, meet the test conditions. One or more of the J, I, P, or N indications are used to exclude from the test ports with Jabber = true, Isolate = true, Partition = true, or port N, respectively.

ANY

Indicates all ports are to be considered. The test passes when one or more ports meet the test conditions.

ANYXJIPN

The test passes when one or more ports, excluding those indicated by J, I, P, or N, meet the test conditions. One or more of the J, I, P, or N indications are used to exclude from the test ports with Jabber = true, Isolate = true, Partition = true, or port N, respectively.

ONLY1

Indicates all ports except those with Jabber = true, Isolate = true, or Partition = true are to be considered. The test passes when one and only one port meet the test conditions.

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41.2.2.2 State diagrams

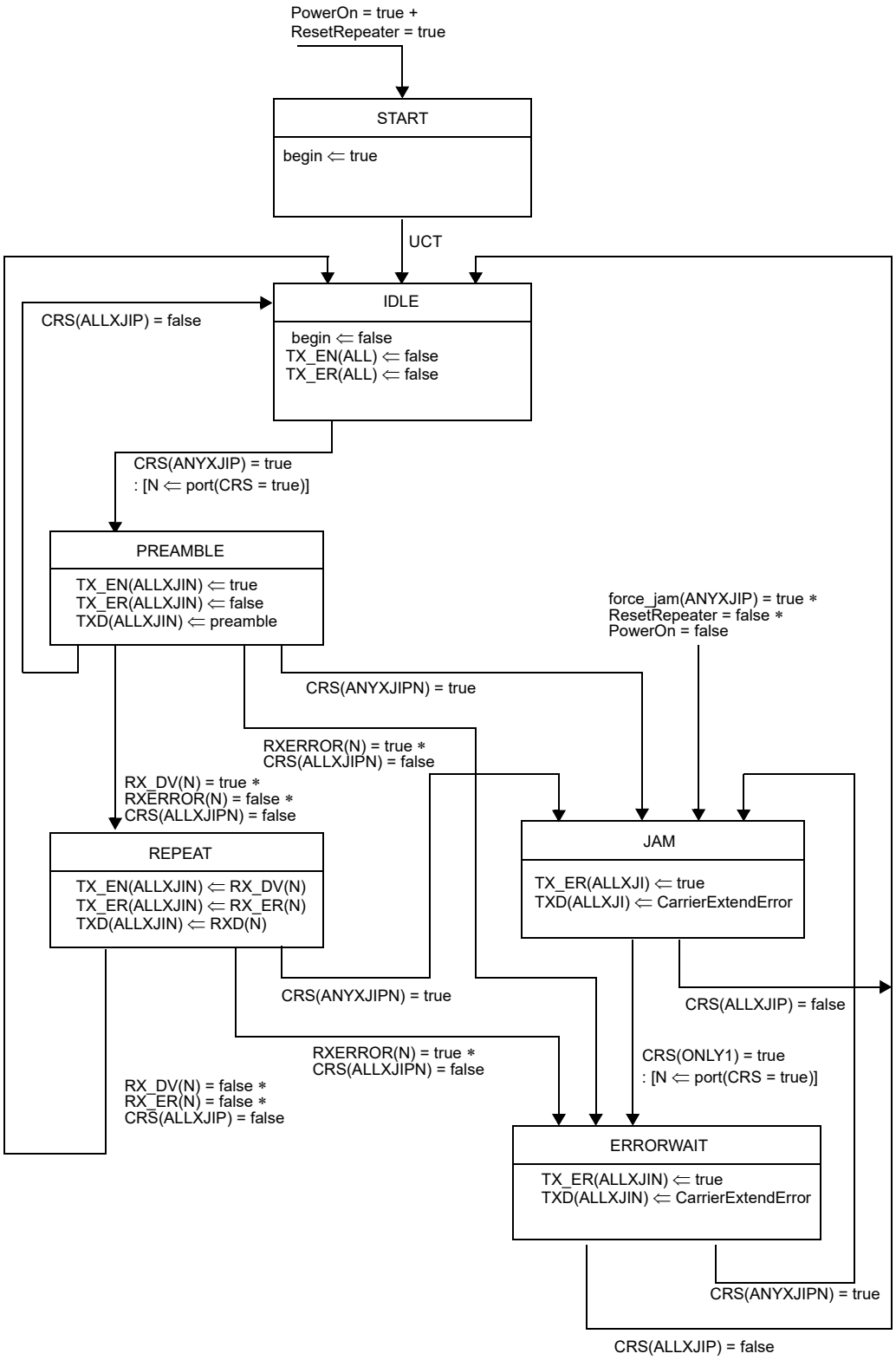

Figure 41–2—Repeater unit state diagram

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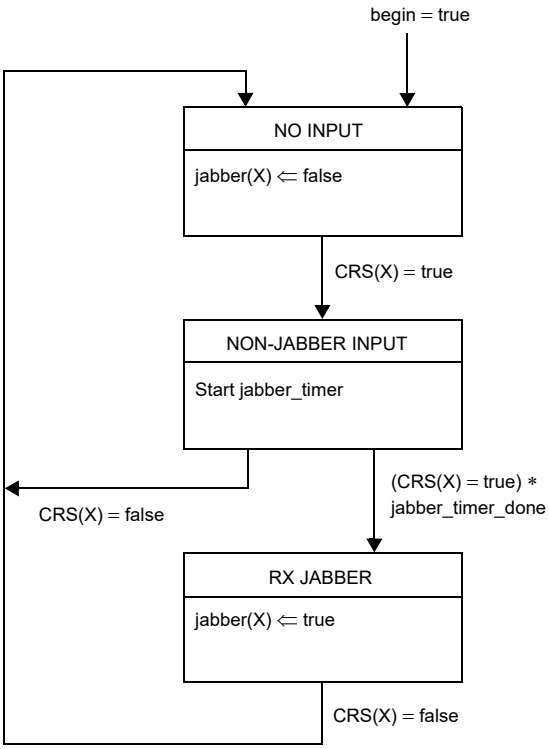

Figure 41–3—Receive timer state diagram for port X

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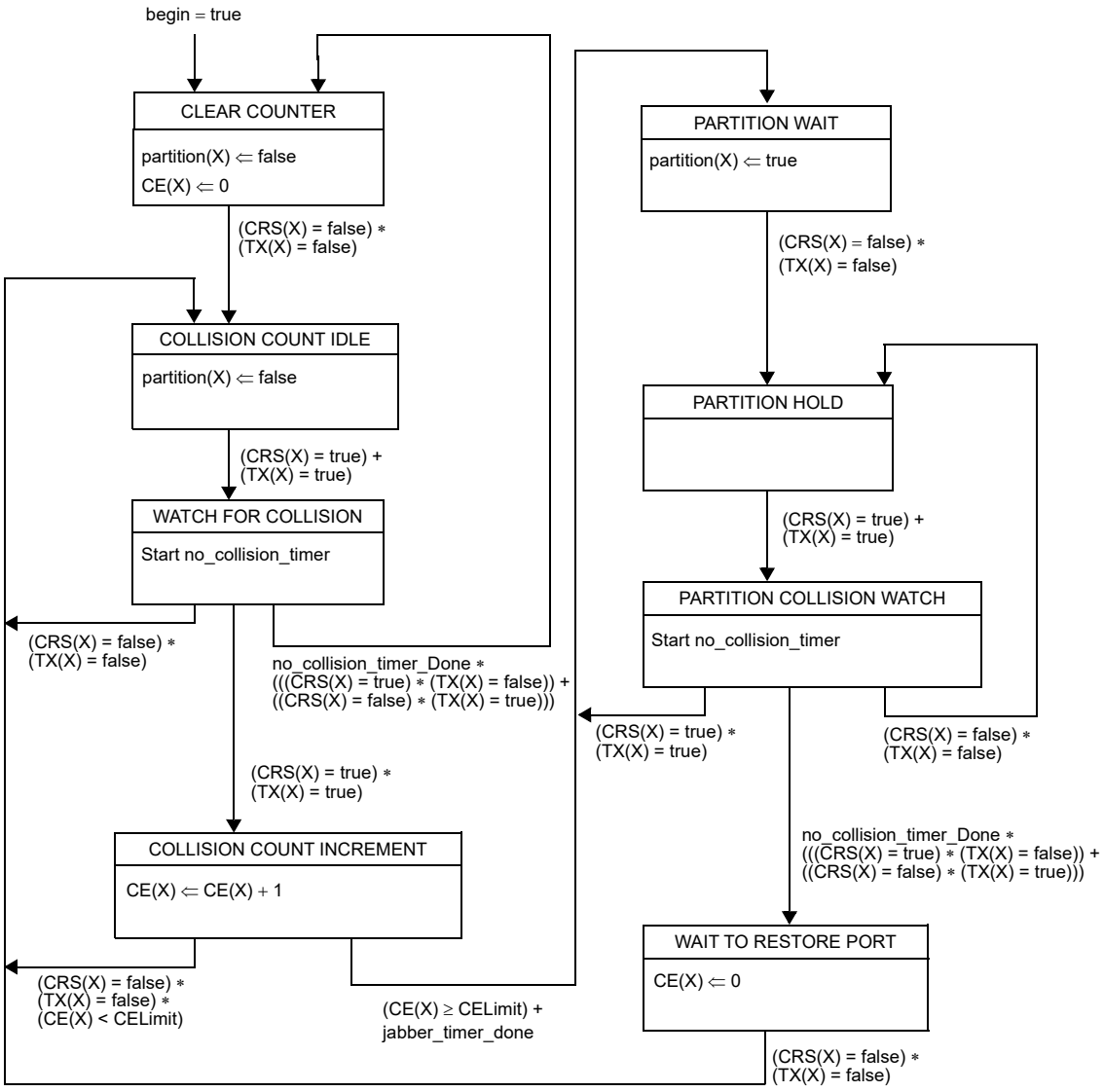

Figure 41–4—Partition state diagram for port X

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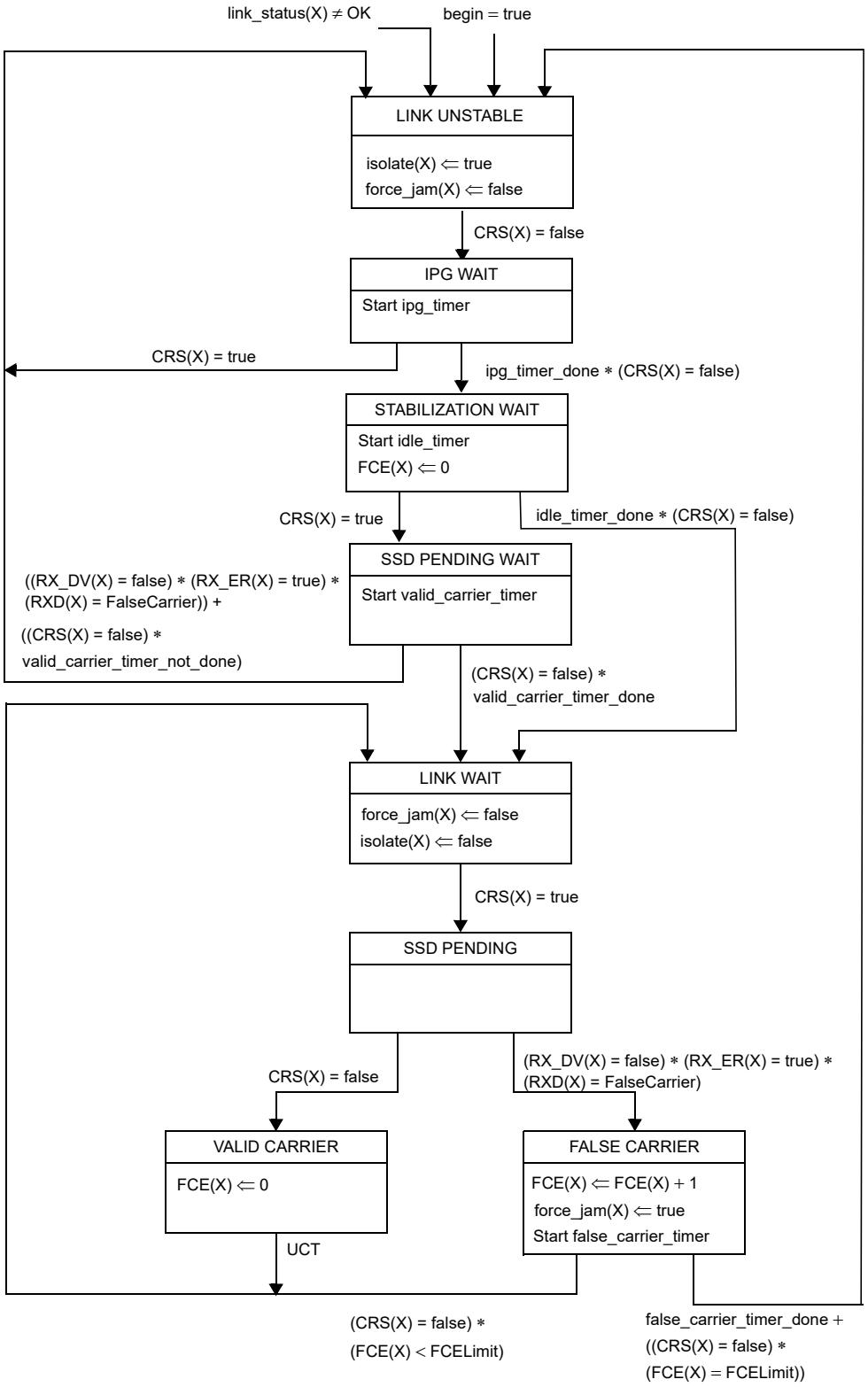

Figure 41–5—Carrier integrity monitor state diagram for port X

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41.3 Repeater electrical specifications

41.3.1 Electrical isolation

Network segments that have different isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of the repeater set.

41.4 Environmental specifications

41.4.1 General safety

NOTE—Since September 2011, maintenance changes are no longer being considered for this clause. Since February 2021, safety information is in J.2.

All equipment meeting this standard shall conform to IEC 60950: 1991.

41.4.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cables and components.
c) High-energy transients coupled onto the LAN cable system.
d) Voltage potential differences between safety grounds to which the various LAN components are connected.

Such electrical safety hazards have to be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures have to be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network. Isolation requirements are defined in 41.4.3.

41.4.2.1 Installation

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

41.4.2.2 Grounding

The safety ground, or chassis ground for the repeater set, shall be provided through the main ac power cord via the third wire ground as defined by applicable local codes and regulations.

If the MDI connector should provide a shield connection, the shield may be connected to the repeater safety ground. A network segment connected to the repeater set through the MDI may use a shield. If both ends of the network segment have a shielded MDI connector available, then the shield may be grounded at both ends according to local regulations and ISO/IEC 11801: 1995, and as long as the ground potential difference between both ends of the network segment is less than 1 V rms.

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WARNING

It is assumed that the equipment to which the repeater is attached is properly grounded and not left floating nor serviced by a "doubly insulated ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety, are beyond the scope of this standard.

41.4.2.3 Installation and maintenance guidelines

During installation and maintenance of the cable plant, care should be taken to ensure that uninsulated network cable connectors do not make electrical contact with unintended conductors or ground.

41.4.3 Electrical isolation

There are two electrical power distribution environments to be considered that require different electrical isolation properties:

a) *Environment A.* When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.
b) *Environment B.* When a LAN crosses the boundary between separate power distribution systems or the boundary of a single building.

41.4.3.1 Environment A requirements

Attachment of network segments via repeater sets requires electrical isolation of 500 V rms, one-minute withstand, between the segment and the protective ground of the repeater unit.

41.4.3.2 Environment B requirements

The attachment of network segments that cross environment B boundaries requires electrical isolation of 1500 Vrms, one-minute withstand, between each segment and all other attached segments and also the protective ground of the repeater unit.

The requirements for interconnected electrically conducting LAN segments that are partially or fully external to a single building environment may require additional protection against lightning strike hazards. Such requirements are beyond the scope of this standard. It is recommended that the above situation be handled by the use of nonelectrically conducting segments (e.g., fiber optic).

It is assumed that any nonelectrically conducting segments will provide sufficient isolation within that media to satisfy the isolation requirements of environment B.

41.4.4 Reliability

A two-port repeater set shall be designed to provide a mean time between failure (MTBF) of at least 50 000 hours of continuous operation without causing a communications failure among stations attached to the network medium. Repeater sets with more than two ports shall add no more than 3.46×10^{-6} failures per hour for each additional port.

The repeater set electronics should be designed to minimize the probability of component failures within the repeater electronics that prevent communications among other PHYs on the individual segments. Connectors and other passive components comprising the means of connecting the repeater to the cable should be designed to minimize the probability of total network failure.

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41.4.5 Environment

41.4.5.1 Electromagnetic emission

The repeater shall comply with applicable local and national codes for the limitation of electromagnetic interference.

41.4.5.2 Temperature and humidity

The repeater is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the repeater the operating environmental conditions to facilitate selection, installation, and maintenance.

41.5 Repeater labeling

It is required that each repeater (and supporting documentation) shall be labeled in a manner visible to the user with these parameters:

a) Crossover ports appropriate to the respective PHY shall be marked with an X.

Additionally it is recommended that each repeater (and supporting documentation) also be labeled in a manner visible to the user with at least these parameters:

b) Data rate capability in Mb/s
c) Any applicable safety warnings
d) Port type, i.e., 1000BASE-CX, 1000BASE-SX, 1000BASE-LX, and 1000BASE-T
e) Worst-case bit time delays between any two ports appropriate for
    1) Start-of-packet propagation delay
    2) Start-of-collision Jam propagation delay
    3) Cessation-of-collision Jam propagation delay

41.6 Protocol implementation conformance statement (PICS) proforma for Clause 41, Repeater for 1000 Mb/s baseband networks[86]

41.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 41, Repeater for 1000 Mb/s baseband networks, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

[86] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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41.6.2 Identification

41.6.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

41.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2018, Clause 41, Repeater for 1000 Mb/s baseband networks
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2018.)	

Date of Statement	

41.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*SXP	Repeater supports 1000BASE-SX connections	41.1.2.2		O	Yes [ ] No [ ]
*LXP	Repeater supports 1000BASE-LX connections	41.1.2.2		O	Yes [ ] No [ ]
*CXP	Repeater supports 1000BASE-CX connections	41.1.2.2		O	Yes [ ] No [ ]
*TP	Repeater supports 1000BASE-T connections	41.1.2.2		O	Yes [ ] No [ ]
*PHYS	PHYs capable of detecting non 1000 Mb/s signals	41.2.1.5.2		O	Yes [ ] No [ ]

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In addition, the following predicate name is defined for use when different implementations from the set above have common parameters:

*XP:SXP or LXP or CXP

41.6.4 PICS proforma tables for the Repeater for 1000 Mb/s baseband networks

41.6.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	1000BASE-SX port compatible at the MDI	41.1.2.2		SXP:M	Yes [ ] N/A [ ]
CC2	1000BASE-LX port compatible at the MDI	41.1.2.2		LXP:M	Yes [ ] N/A [ ]
CC3	1000BASE-CX port compatible at the MDI	41.1.2.2		CXP:M	Yes [ ] N/A [ ]
CC4	1000BASE-T port compatible at the MDI	41.1.2.2		TP:M	Yes [ ] N/A [ ]
CC5	Internal segment compatibility	41.1.2.2.1	Internal port meets Clause 30 when repeater management implemented	M	Yes [ ]

41.6.4.2 Repeater functions

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Signal Restoration	41.2.1		M	Yes [ ]
RF2	Data Handling	41.2.1		M	Yes [ ]
RF3	Received Event Handling	41.2.1		M	Yes [ ]
RF4	Collision Handling	41.2.1		M	Yes [ ]
RF5	Error Handling	41.2.1		M	Yes [ ]
RF6	Partition	41.2.1		M	Yes [ ]
RF7	Received Jabber	41.2.1		M	Yes [ ]
RF8	Transmit	41.2.1		M	Yes [ ]
RF9	Receive	41.2.1		M	Yes [ ]

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41.6.4.3 Signal restoration function

Item	Feature	Subclause	Value/Comment	Status	Support
SR1	Output amplitude as required by 1000BASE-SX	41.2.1.1.1		SXP:M	Yes [ ] N/A [ ]
SR2	Output amplitude as required by 1000BASE-LX	41.2.1.1.1		LXP:M	Yes [ ] N/A [ ]
SR3	Output amplitude as required by 1000BASE-CX	41.2.1.1.1		CXP:M	Yes [ ] N/A [ ]
SR4	Output amplitude as required by 1000BASE-T	41.2.1.1.1		TP:M	Yes [ ] N/A [ ]
SR5	Output signal wave-shape as required by 1000BASE-SX	41.2.1.1.2		SXP:M	Yes [ ] N/A [ ]
SR6	Output signal wave-shape as required by 1000BASE-LX	41.2.1.1.2		LXP:M	Yes [ ] N/A [ ]
SR7	Output signal wave-shape as required by 1000BASE-CX	41.2.1.1.2		CXP:M	Yes [ ] N/A [ ]
SR8	Output signal wave-shape as required by 1000BASE-T	41.2.1.1.2		TP:M	Yes [ ] N/A [ ]
SR9	Output data timing as required by 1000BASE-SX	41.2.1.1.3		SXP:M	Yes [ ] N/A [ ]
SR10	Output data timing as required by 1000BASE-LX	41.2.1.1.3		LXP:M	Yes [ ] N/A [ ]
SR11	Output data timing as required by 1000BASE-CX	41.2.1.1.3		CXP:M	Yes [ ] N/A [ ]
SR12	Output data timing as required by 1000BASE-T	41.2.1.1.3		TP:M	Yes [ ] N/A [ ]

41.6.4.4 Data-Handling function

Item	Feature	Subclause	Value/Comment	Status	Support
DH1	Data frames forwarded to all ports except receiving port	41.2.1.2.1		M	Yes [ ]
DH2	Code Violations forwarded to all transmitting ports	41.2.1.2.2		M	Yes [ ]
DH3	Received Code Violation forwarded as code-group explicitly indicating received error	41.2.1.2.2		M	Yes [ ]
DH4	Code element substitution for remainder of packet after received Code Violation	41.2.1.2.2		M	Yes [ ]

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41.6.4.5 Receive Event-Handling function

Item	Feature	Subclause	Value/Comment	Status	Support
RE1	Detect all received events	41.2.1.3.1		M	Yes [ ]
RE2	Repeat all received signals	41.2.1.3.1		M	Yes [ ]
RE3	Preamble repeated as required	41.2.1.3.2		M	Yes [ ]
RE4	Start-of-packet propagation delay	41.2.1.3.3	SOP + SOJ ≤ 976 BT	M	Yes [ ]
RE5	Start-of-packet variability	41.2.1.3.4	SOP variation ≤ 16 BT	M	Yes [ ]
RE6	PHY repeater_mode variable	41.2.1.3.1	Shall be set to ensure CRS signal not asserted in response to transmit activity	M	Yes [ ]
RE7	Output preamble variation	41.2.1.3.2	Variation between received and transmitted preamble ≤ 8 BT	M	Yes [ ]

41.6.4.6 Collision-Handling function

Item	Feature	Subclause	Value/Comment	Status	Support
CO1	Collision Detection	41.2.1.4.1	Receive event on more than one port	M	Yes [ ]
CO2	Jam Generation	41.2.1.4.2	Transmit Jam message while collision is detected	M	Yes [ ]
CO3	Collision-Jam Propagation delay	41.2.1.4.3	SOP + SOJ ≤ 976 BT	M	Yes [ ]
CO4	Cessation of Collision Propagation delay	41.2.1.4.4	EOJ ≤ SOP	M	Yes [ ]

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41.6.4.7 Error-Handling function

Item	Feature	Subclause	Value/Comment	Status	Support
EH1	Carrier Integrity function implementation	41.2.1.5.1	Self-interrupt of data reception	M	Yes [ ]
EH2	False Carrier Event count for Link Unstable detection	41.2.1.5.1	False Carrier Event count equals FCELimit	M	Yes [ ]
EH3	False carrier count reset	41.2.1.5.1	Count reset on valid carrier	M	Yes [ ]
EH4	False carrier timer for Link Unstable detection	41.2.1.5.1	False carrier of length in excess of false_carrier_timer	M	Yes [ ]
EH5	Jam message duration	41.2.1.5.1	Equals duration of false carrier event, but not greater than duration of false_carrier_timer	M	Yes [ ]
EH6	Link Unstable detection	41.2.1.5.1	False Carrier Event count equals FCELimit or False carrier exceeds the false_carrier_timer or power-up reset	M	Yes [ ]
EH7	Messages sent to repeater unit in Link Unstable state	41.2.1.5.1	Inhibited sending messages to repeater unit	M	Yes [ ]
EH8	Messages sent from repeater unit in Link Unstable state	41.2.1.5.1	Inhibited sending output messages	M	Yes [ ]
EH9	Monitoring activity on a port in Link Unstable state	41.2.1.5.1	Continue monitoring activity at that port	M	Yes [ ]
EH10	Reset of Link Unstable state	41.2.1.5.1	No activity for more than ipg_timer plus idle_timer or Valid carrier event of duration greater than valid_carrier_timer preceded by Idle of duration greater than ipg_timer	M	Yes [ ]
EH11	Block flow of non-1000 Mb/s signals	41.2.1.5.2		M	Yes [ ]

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41.6.4.8 Partition function

Item	Feature	Subclause	Value/Comment	Status	Support
PA1	Partition function implementation	41.2.1.6	Self-interrupt of data reception	M	Yes [ ]
PA2	Consecutive Collision Event count for entry into partition state	41.2.1.6	Consecutive Collision Event count equals or exceeds CELimit	M	Yes [ ]
PA3	Excessive receive duration with collision for entry into partition state.	41.2.1.6	Reception duration in excess of jabber_timer with collision	M	Yes [ ]
PA4	Consecutive Collision Event counter incrementing	41.2.1.6	Count incremented on each transmission that suffers a collision	M	Yes [ ]
PA5	Consecutive Collision Event counter reset	41.2.1.6	Count reset on successful transmission or reception	M	Yes [ ]
PA6	Messages sent to repeater unit in Partition state	41.2.1.6	Inhibited sending messages to repeater unit	M	Yes [ ]
PA7	Messages sent from repeater unit in Partition state	41.2.1.6	Continue sending output messages	M	Yes [ ]
PA8	Monitoring activity on a port in Partition state	41.2.1.6	Continue monitoring activity at that port	M	Yes [ ]
PA9	Reset of Partition state	41.2.1.6	Power-up reset or transmitting or detecting activity for greater than duration no_collision_-timer without a collision	M	Yes [ ]

41.6.4.9 Receive Jabber function

Item	Feature	Subclause	Value/Comment	Status	Support
RJ1	Receive Jabber function implementation	41.2.1.7	Self-interrupt of data reception	M	Yes [ ]
RJ2	Excessive receive duration timer for Receive Jabber detection	41.2.1.7	Reception duration in excess of jabber_timer	M	Yes [ ]
RJ3	Messages sent to repeater unit in Receive Jabber state	41.2.1.7	Inhibit sending input messages to repeater unit	M	Yes [ ]
RJ4	Messages sent from repeater unit in Receive Jabber state	41.2.1.7	Inhibit sending output mes-sages	M	Yes [ ]
RJ5	Reset of Receive Jabber state	41.2.1.7	Power-up reset or Carrier no longer detected	M	Yes [ ]

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41.6.4.10 Repeater state diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Repeater unit state diagram	41.2.2.2	Meets the requirements of Figure 41–2	M	Yes [ ]
SD2	Receive timer for port X state diagram	41.2.2.2	Meets the requirements of Figure 41–3	M	Yes [ ]
SD3	Repeater partition state diagram for port X	41.2.2.2	Meets the requirements of Figure 41–4	M	Yes [ ]
SD4	Carrier integrity monitor for port X state diagram	41.2.2.2	Meets the requirements of Figure 41–5	M	Yes [ ]

41.6.4.11 Repeater electrical

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Port-to-port isolation	41.3.1	Satisfies isolation and grounding requirements for attached network segments	M	Yes [ ]
EL2	Safety	41.4.1	IEC 60950:1991	M	Yes [ ]
EL3	Installation practices	41.4.2.1	Sound, as defined by local code and regulations	M	Yes [ ]
EL4	Grounding	41.4.2.2	Chassis ground provided through ac mains cord	M	Yes [ ]
EL5	Two-port repeater set MTBF	41.4.4	At least 50 000 hours	M	Yes [ ]
EL6	Additional port effect on MTBF	41.4.4	No more than 3.46×10^{-6} increase in failures per hour	M	Yes [ ]
EL7	Electromagnetic interference	41.4.5.1	Comply with local or national codes	M	Yes [ ]

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41.6.4.12 Repeater labeling

Item	Feature	Subclause	Value/Comment	Status	Support
LB1	Crossover ports	41.5	Marked with an X	M	Yes [ ]
LB2	Data Rate	41.5	1000 Mb/s	O	Yes [ ] No [ ]
LB3	Safety warnings	41.5	Any applicable	O	Yes [ ] No [ ]
LB4	Port Types	41.5	1000BASE-SX, 1000BASE-LX, 1000BASE-CX, or 1000BASE-T	O	Yes [ ] No [ ]
LB5	Worst-case start-of-packet propagation delay	41.5	Value in bit times (BT)	O	Yes [ ] No [ ]
LB6	Worst-case start-of-collision-Jam propagation delay	41.5	Value in BT	O	Yes [ ] No [ ]
LB7	Worst-case Cessation-of-Collision Jam propagation delay	41.5	Value in BT	O	Yes [ ] No [ ]

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42. System considerations for multisegment 1000 Mb/s networks

42.1 Overview

This clause provides information on building 1000 Mb/s networks. The 1000 Mb/s technology is designed to be deployed in both homogenous 1000 Mb/s networks and 10/100/1000 Mb/s mixed networks using bridges and/or routers. Network topologies can be developed within a single 1000 Mb/s collision domain, but maximum flexibility is achieved by designing multiple collision domain networks that are joined by bridges and/or routers configured to provide a range of service levels to DTEs. For example, a combined 1000BASE-T/100BASE-T/10BASE-T system built with repeaters and bridges can deliver dedicated or shared service to DTEs at 1000 Mb/s, 100 Mb/s, or 10 Mb/s.

Linking multiple collision domains with bridges maximizes flexibility. Bridged topology designs can provide single data rate (Figure 42–1) or multiple data rate (Figure 42–2) services.

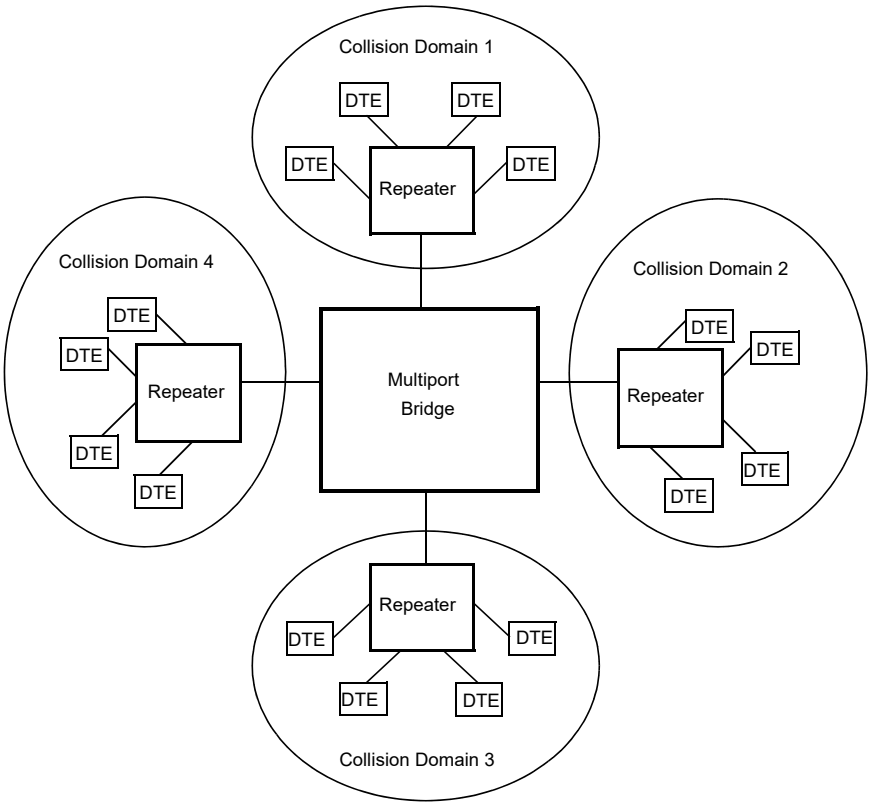

Figure 42–1—1000 Mb/s multiple collision domain topology using multiport bridge

Individual collision domains can be linked by single devices (as shown in Figure 42–1 and Figure 42–2) or by multiple devices from any of several transmission systems. The design of multiple-collision-domain networks is governed by the rules defining each of the transmission systems incorporated into the design.

The design of shared bandwidth 10 Mb/s collision domains is defined in Clause 13; the design of shared bandwidth 100 Mb/s CSMA/CD collision domains is defined in Clause 29; the design of shared bandwidth 1000 Mb/s CSMA/CD collision domains is defined in the following subclauses.

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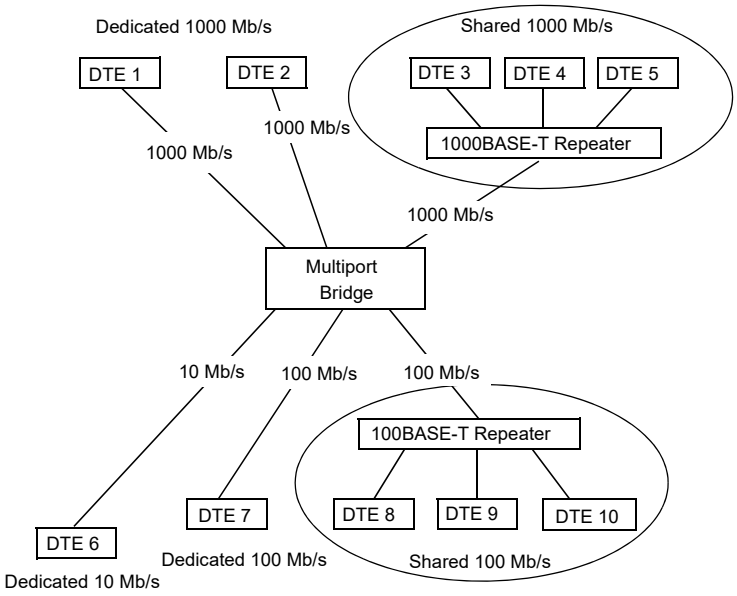

Figure 42–2—Multiple data rate, multiple collision domain topology using multiport bridge

42.1.1 Single collision domain multisegment networks

This clause provides information on building 1000 Mb/s CSMA/CD multisegment networks within a single collision domain. The proper operation of a CSMA/CD network requires the physical size of the collision domain to be limited in order to meet the round-trip propagation delay requirements of 4.2.3.2.3 and 4.4.2, and requires the number of repeaters to be limited to one so as not to exceed the InterFrameGap shrinkage noted in 4.4.2.

This clause provides two network models. Transmission System Model 1 is a set of configurations that have been validated under conservative rules and have been qualified as meeting the requirements set forth above. Transmission System Model 2 is a set of calculation aids that allow those configuring a network to test a proposed configuration against a simple set of criteria that allows it to be qualified. Transmission System Model 2 validates an additional broad set of topologies that are fully functional and do not fit within the simpler, but more restrictive rules of Model 1.

The physical size of a CSMA/CD network is limited by the characteristics of individual network components. These characteristics include the following:

a) Media lengths and their associated propagation time delay.
b) Delay of repeater units (startup, steady-state, and end of event).
c) Delay of MAUs and PHYs (startup, steady-state, and end of event).
d) Interpacket gap shrinkage due to repeater units.
e) Delays within the DTE associated with the CSMA/CD access method.
f) Collision detect and deassertion times associated with the MAUs and PHYs.

Table 42–1 summarizes the delays, measured in Bit Times (BTs), for 1000 Mb/s media segments.

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Table 42–1—Delays for network media segments Model 1

Media type	Maximum number of PHYs per segment	Maximum segment length (m)	Maximum medium round-trip delay per segment (BT)
Category 5 Link Segment (1000BASE-T)	2	100	1112
Shielded Jumper Cable Link Segment (1000BASE-CX)	2	25	253
Optical Fiber Link Segment (1000BASE-SX, 1000BASE-LX)	2	316[a]	3192

[a]May be limited by the maximum transmission distance of the link.

42.1.2 Repeater usage

Repeaters are the means used to connect segments of a network medium together into a single collision domain. Different physical signaling systems (e.g., 1000BASE-CX, 1000BASE-SX, 1000BASE-LX, 1000BASE-T) can be joined into a common collision domain using a repeater. Bridges can also be used to connect different signaling systems; however, if a bridge is so used, each LAN connected to the bridge will comprise a separate collision domain.

42.2 Transmission System Model 1

The following network topology constraints apply to networks using Transmission System Model 1.

a) Single repeater topology maximum.
b) Link distances not to exceed the lesser of 316 m or the segment lengths as shown in Table 42–1.

42.3 Transmission System Model 2

Transmission System Model 2 is a single repeater topology with the physical size limited primarily by round-trip collision delay. A network configuration has to be validated against collision delay using a network model for a 1000 Mb/s collision domain. The modeling process is quite straightforward and can easily be done either manually or with a spreadsheet.

The model proposed here is derived from the one presented in 13.4. Modifications have been made to accommodate adjustments for DTE, repeater, and cable speeds.

For a network consisting of two 1000BASE-T DTEs as shown in Figure 42–3, a crossover connection may be required if the auto-crossover function is not implemented. See 40.4 and 40.8.

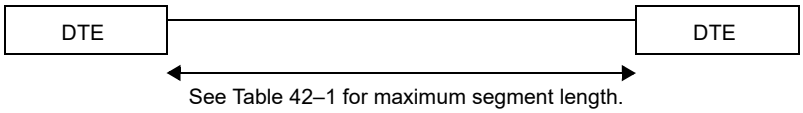

Figure 42–3—Model 1: Two DTEs, no repeater

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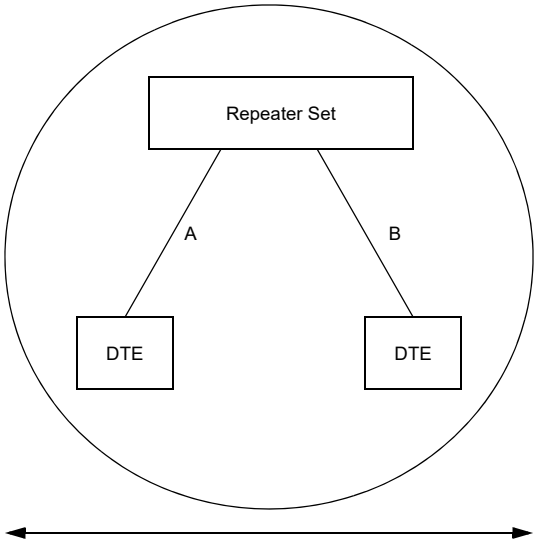

Figure 42–4—Model 1: Single repeater

Table 42–2—Maximum Model 1 collision domain diameter[a]

Configuration	Category 5 Twisted-Pair (T)	Shielded Jumper Cable (CX)	Optical Fiber (SX/LX)	Mixed Category 5 and Fiber (T and SX/LX)	Mixed Shielded Jumper and Fiber (CX and SX/LX)
DTE-DTE (see Figure 42–3)	100	25	316[b]	NA	NA
One repeater (see Figure 42–4)	200	50	220	210[c]	220[d]

[a]In meters.
[b]May be limited by the maximum transmission distance of the link.
[c]Assumes 100 m of Category 5 twisted-pair and one Optical Fiber link of 110 m.
[d]Assumes 25 m of Shielded Jumper Cable and one Optical Fiber link of 195 m.

42.3.1 Round-trip collision delay

For a network configuration to be valid, it has to be possible for any two DTEs on the network to properly arbitrate for the network. When two or more stations attempt to transmit within a slot time interval, each station has to be notified of the contention by the returned “collision” signal within the “collision window” (see 4.1.2.2). Additionally, the maximum length fragment created on a 1000 Mb/s network has to contain less than 512 bytes after the Start Frame Delimiter (SFD). These requirements limit the physical diameter (maximum distance between DTEs) of a network. The maximum round-trip delay has to be qualified between all pairs of DTEs in the network. In practice this means that the qualification has to be done between those that, by inspection of the topology, are candidates for the longest delay. The following network modeling methodology is provided to assist that calculation.

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42.3.1.1 Worst-case path delay value (PDV) selection

The worst-case path through a network to be validated is identified by examination of aggregate DTE delays, cable delays, and repeater delay. The worst case consists of the path between the two DTEs at opposite ends of the network that have the longest round-trip time. Figure 42–5 shows a schematic representation of a one-repeater path.

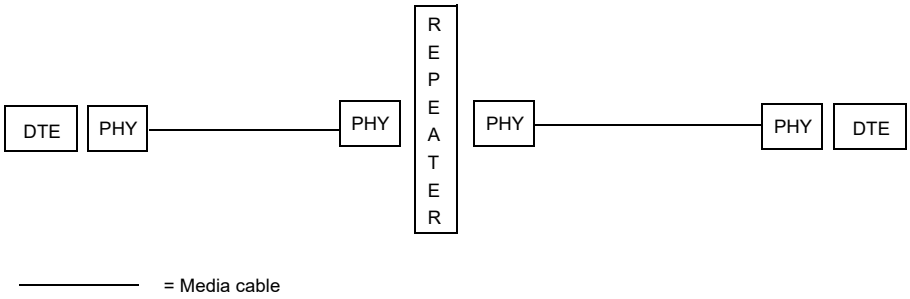

Figure 42–5—System Model 2: Single repeater

42.3.1.2 Worst-case PDV calculation

Once a set of paths is chosen for calculation, each is checked for validity against the following formula:

PDV = ∑link delays (LSDV) + repeater delay + DTE delays + safety margin

Values for the formula variables are determined by the following method:

a) Determine the delay for each link segment (Link Segment Delay Value, or LSDV), using the formula

LSDV=2 (for round-trip delay) × segment length × cable delay for this segment

NOTE 1—Length is the sum of the cable lengths between the PHY interfaces at the repeater and PHY interfaces at the farthest DTE. All measurements are in meters.

NOTE 2—Cable delay is the delay specified by the manufacturer or the maximum value for the type of cable used as shown in Table 42–3. For this calculation, cable delay needs to be specified in bit times per meter (BT/m). Table 42–4 can be used to convert values specified relative to the speed of light (%c) or nanoseconds per meter (ns/m).

NOTE 3—When actual cable lengths or propagation delays are not known, use the Max delay in bit times as specified in Table 42–3 for copper cables. Delays for fiber should be calculated, as the value found in Table 42–3 will be too large for most applications.

NOTE 4—The value found in Table 42–3 for Shielded Jumper Cable is the maximum delay for cable with solid dielectric. Cables with foam dielectric may have a significantly smaller delay.

b) Sum together the LSDVs for all segments in the path.
c) Determine the delay for the repeater. If model-specific data is not available from the manufacturer, enter the appropriate default value from Table 42–3.
d) Use the DTE delay value shown in Table 42–3 unless your equipment manufacturer defines a different value. If the manufacturer's supplied values are used, the DTE delays of both ends of the worst- case path should be summed together.
e) Decide on appropriate safety margin—0 to 40 bit times—for the PDV calculation. Safety margin is used to provide additional margin to accommodate unanticipated delay elements, such as extra-long connecting cable runs between wall jacks and DTEs. (A safety margin of 32 BT is recommended.)

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f) Insert the values obtained through the calculations above into the following formula to calculate the PDV. (Some configurations may not use all the elements of the formula.)

$$PDV = \sum \text{link delays (LSDV)} + \text{repeater delay} + \text{DTE delay} + \text{safety margin}$$

g) If the PDV is less than 4096, the path is qualified in terms of worst-case delay.
h) Late collisions and/or CRC errors may be indications that path delays exceed 4096 BT.

Table 42–3—Network component delays, Transmission System Model 2

Component	Round-trip delay in bit times per meter (BT/m)	Maximum round-trip delay in bit times (BT)
Two DTEs		864
Category 5 Cable segment	11.12	1112 (100 m)
Shielded Jumper Cable segment	10.10	253 (25 m)
Optical Fiber Cable segment	10.10	1111 (110 m)
Repeater		976

Table 42–4—Conversion table for cable delays

Speed relative to c	ns/m	BT/m
0.4	8.34	8.34
0.5	6.67	6.67
0.51	6.54	6.54
0.52	6.41	6.41
0.53	6.29	6.29
0.54	6.18	6.18
0.55	6.06	6.06
0.56	5.96	5.96
0.57	5.85	5.85
0.58	5.75	5.75
0.5852	5.70	5.70
0.59	5.65	5.65
0.6	5.56	5.56
0.61	5.47	5.47

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Table 42–4—Conversion table for cable delays *(continued)*

Speed relative to c	ns/m	BT/m
0.62	5.38	5.38
0.63	5.29	5.29
0.64	5.21	5.21
0.65	5.13	5.13
0.654	5.10	5.10
0.66	5.05	5.05
0.666	5.01	5.01
0.67	4.98	4.98
0.68	4.91	4.91
0.69	4.83	4.83
0.7	4.77	4.77
0.8	4.17	4.17
0.9	3.71	3.71

42.4 Full duplex 1000 Mb/s topology limitations

Unlike half duplex CSMA/CD networks, the physical size of full duplex 1000 Mb/s networks is not limited by the round-trip collision propagation delay. Instead, the maximum link length between DTEs is limited only by the signal transmission characteristics of the specific link.

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43. Content moved to IEEE Std 802.1AX-2008

NOTE—The Link Aggregation specification was moved to IEEE Std 802.1AX™-2008 during the IEEE Std 802.3-2008 revision.

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44. Introduction to 10 Gb/s baseband networks

44.1 Overview

44.1.1 Scope

10 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer, connected through a 10 Gigabit Media Independent Interface (XGMII) to Physical Layer devices (PHYs) such as 10GBASE-SR, 10GBASE-LX4, 10GBASE-CX4, 10GBASE-LRM, 10GBASE-LR, 10GBASE-ER, 10GBASE-SW, 10GBASE-LW, 10GBASE-EW, 10GBASE-T, and 10GBASE-T1.

10 Gigabit Ethernet extends the IEEE 802.3 MAC beyond 1000 Mb/s to 10 Gb/s. The bit rate is faster and the bit times are shorter—both in proportion to the change in bandwidth. The minimum packet transmission time has been reduced by a factor of ten. A rate control mode (see 4.2.3.2.2) is added to the MAC to adapt the average MAC data rate to the SONET/SDH data rate for WAN-compatible applications of this standard. Achievable topologies for 10 Gb/s operation are comparable to those found in 1000BASE-X full duplex mode and equivalent to those found in WAN applications.

10 Gigabit Ethernet is defined for full duplex mode of operation only.

44.1.2 Objectives

The following are the objectives of 10 Gigabit Ethernet:

a) Support the full duplex Ethernet MAC.
b) Provide 10 Gb/s data rate at the XGMII.
c) Support LAN PMDs operating at 10 Gb/s, and WAN PMDs operating at SONET STS-192c/SDH VC-4-64c rate.
d) Support cable plants using cabled optical fiber compliant with ISO/IEC 11801:1995.
e) Allow for a nominal network extent of up to 40 km.
f) Support operation over a twinaxial cable assembly for wiring closet and data center applications.
g) Support operation over selected copper media from ISO/IEC 11801:2002.
h) Support operation over a single balanced pair of conductors.
i) Support a BER objective of 10^{-12}.

44.1.3 Relationship of 10 Gigabit Ethernet to the ISO OSI reference model

10 Gigabit Ethernet couples the IEEE 802.3 MAC to a family of 10 Gb/s Physical Layers. The relationships among 10 Gigabit Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 44–1.

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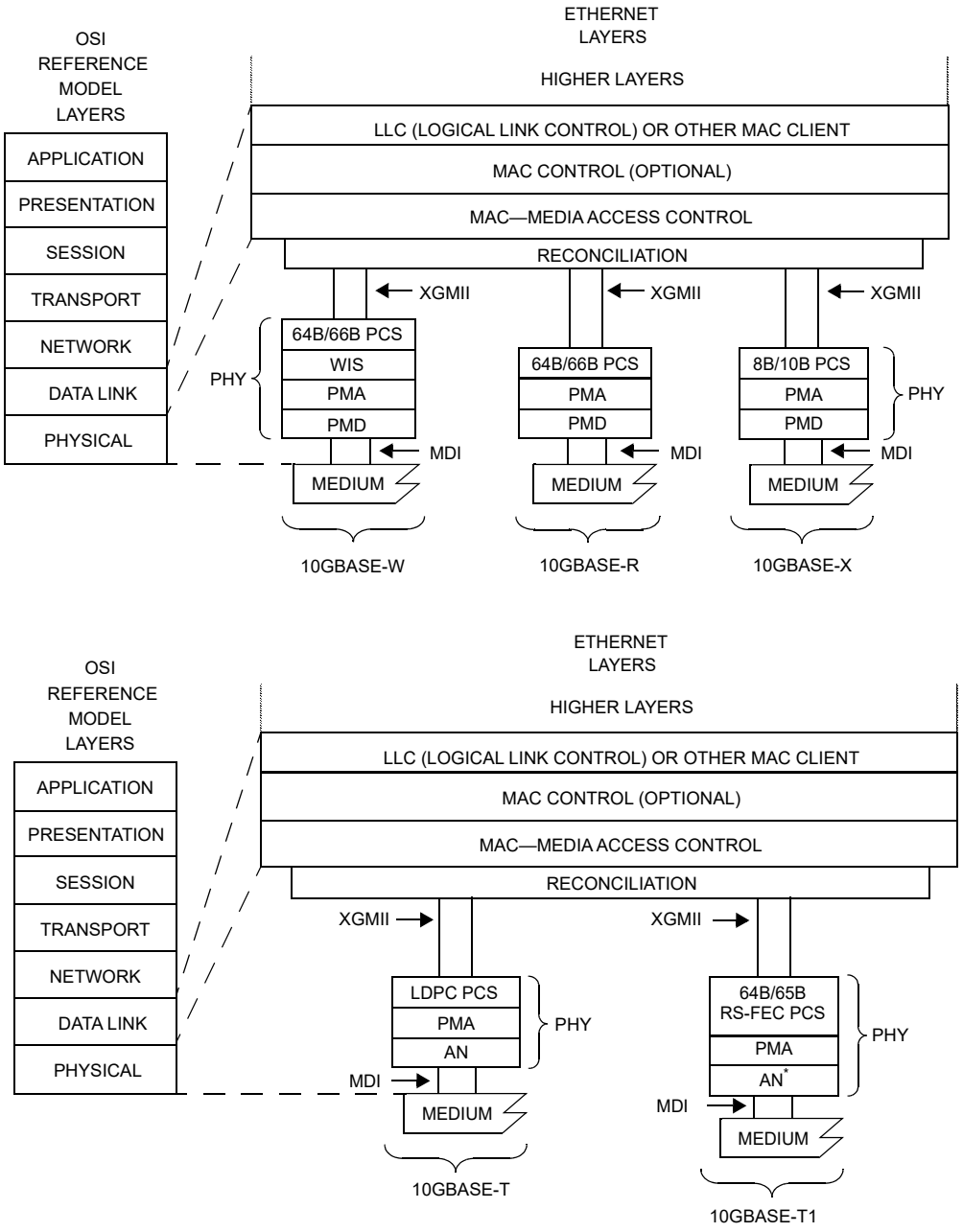

AN = AUTO-NEGOTIATION SUBLAYER
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
WIS = WAN INTERFACE SUBLAYER
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
* AUTO-NEGOTIATION IS OPTIONAL

Figure 44–1—Architectural positioning of 10 Gigabit Ethernet

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It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The XGMII, which, when implemented at an observable interconnection port, uses a four octet-wide data path as specified in Clause 46.
b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.
c) The PMA Service Interface, which, when physically implemented as the XSBI (10 Gigabit Sixteen Bit Interface) at an observable interconnection port, uses a 16-bit-wide data path as specified in Clause 51.
d) The MDI as specified in Clause 53 for 10GBASE-LX4, in Clause 54 for 10GBASE-CX4, in Clause 55 for 10GBASE-T, in Clause 68 for 10GBASE-LRM, in Clause 149 for 10GBASE-T1, and in Clause 52 for other PMD types.

44.1.4 Summary of 10 Gigabit Ethernet sublayers

44.1.4.1 Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

The 10 Gigabit Media Independent Interface (Clause 46) provides an interconnection between the Media Access Control (MAC) sublayer and Physical Layer devices (PHYs). This XGMII supports 10 Gb/s operation through its 32-bit-wide transmit and receive data paths. The Reconciliation Sublayer provides a mapping between the signals provided at the XGMII and the MAC/PLS service definition.

While the XGMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for Clause 47, Clause 48, Clause 49, Clause 55, and Clause 149.

44.1.4.2 XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI)

The 10 Gigabit Attachment Unit Interface (Clause 47) provides an interconnection between two XGMII Extender sublayers to increase the reach of the XGMII. This XAUI supports 10 Gb/s operation through its four-lane, differential-pair transmit and receive paths. The XGXS provides a mapping between the signals provided at the XGMII and the XAUI.

44.1.4.3 Management interface (MDIO/MDC)

The MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMD) and Station Management (STA) entities.

44.1.4.4 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. The generic term 10 Gigabit Ethernet refers to any use of the 10 Gb/s IEEE 802.3 MAC (the 10 Gigabit Ethernet MAC) coupled with any IEEE 802.3 10GBASE Physical Layer implementation. Table 44–1 specifies the correlation between nomenclature and clauses. Implementations conforming to one or more nomenclatures shall meet the requirements of the corresponding clauses.

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Table 44–1—Nomenclature and clause correlation

Nomenclature	Clause[a]											
	48	49	50	51	52			53	54	55	68	149
	8B/10B PCS & PMA	64B/66B PCS	WIS	Serial PMA	850 nm Serial PMD	1310 nm Serial PMD	1550 nm Serial PMD	1310 nm WDM PMD	4-Lane electrical PMD	LDPC PCS & 4-pair PMA	1310 nm Serial MMF PMD	RS–FEC PCS & 1-pair PMA
10GBASE-CX4	M								M			
10GBASE-T1												M
10GBASE-T										M		
10GBASE-LRM		M		M							M	
10GBASE-SR		M		M	M							
10GBASE-SW		M	M	M	M							
10GBASE-LX4	M							M				
10GBASE-LR		M		M		M						
10GBASE-LW		M	M	M		M						
10GBASE-ER		M		M			M					
10GBASE-EW		M	M	M			M					

[a] M = Mandatory

The term 10GBASE-X, specified in Clause 48, Clause 53, and Clause 54, refers to a specific family of Physical Layer implementations based upon 8B/10B data coding method. The 10GBASE-X family of Physical Layer implementations is composed of 10GBASE-LX4 and 10GBASE-CX4.

The term 10GBASE-R refers to a specific family of Physical Layer implementations. The 10GBASE-R family of Physical Layer implementations based upon 64B/66B data coding method is composed of 10GBASE-SR, 10GBASE-LR, 10GBASE-ER, and 10GBASE-LRM.

The term 10GBASE-W, specified in Clause 49 through Clause 52, refers to a specific family of Physical Layer implementations based upon STS-192c/SDH VC-4-64c encapsulation of 64B/66B encoded data. The 10GBASE-W family of Physical Layer standards has been adapted from the ATIS-0600416.1999(R2010) (SONET STS-192c/SDH VC-4-64c) Physical Layer specifications. The 10GBASE-W family of Physical Layer implementations is composed of 10GBASE-SW, 10GBASE-LW, and 10GBASE-EW.

All 10GBASE-R and 10GBASE-W PHY devices share a common PCS specification (see Clause 49). The 10GBASE-W PHY devices also require the use of the WAN Interface Sublayer, (WIS) (Clause 50).

The term 10GBASE-T, specified in Clause 55, refers to a specific Physical Layer implementation based upon 64B/65B data coding placed in a low density parity check (LDPC) frame that is mapped to a 128 double-square (DSQ128) constellation for transmission on 4-pair, twisted-pair copper cabling.

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The term 10GBASE-T1, specified in Clause 149, refers to a specific Physical Layer implementation based upon 64B/65B data coding method placed in an RS-FEC frame that is Gray-code mapped to PAM4 for transmission over a single balanced pair of conductors.

Physical Layer device specifications are contained in Clause 52, Clause 53, Clause 54, Clause 55, Clause 68, and Clause 149.

Annex 44A contains diagrams of the data flow between the MAC and the MDI, as well as information on the relation between data valid signals and loopback.

44.1.4.5 WAN Interface Sublayer (WIS), type 10GBASE-W

The WIS provides a 10GBASE-W device with the capability to transmit and receive IEEE 802.3 MAC frames within the payload envelope of a SONET STS-192c/SDH VC-4-64c frame.

44.1.5 Management

Managed objects, attributes, and actions are defined for all 10 Gigabit Ethernet components. These items are defined in Clause 30.

44.2 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

44.3 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. Table 44–2 contains the values of maximum sublayer round-trip (sum of transmit and receive) delay in bit time as specified in 1.4 and pause_quanta as specified in 31B.2.

Equation (44–1) specifies the calculation of bit time per meter of fiber or electrical cable based upon the parameter *n*, which represents the ratio of the speed of electromagnetic propagation in the fiber or electrical cable to the speed of light in a vacuum. The value of *n* should be available from the fiber or electrical cable manufacturer, but if no value is known then a conservative delay estimate can be calculated using a default value of $n = 0.66$. The speed of light in a vacuum is $c = 3 \times 10^8$ m/s. Table 44–3 can be used to convert fiber or electrical cable delay values specified relative to the speed of light or in nanoseconds per meter.

$$\text{cable delay} = \frac{10^{10}}{nc} \text{ BT/m} \tag{44–1}$$

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Table 44–2—Round-trip delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Notes[a]
MAC, RS, and MAC Control	8 192	16	See 46.1.4.
XGXS and XAUI	4 096	8	Round-trip of 2 XGXS and trace for both directions. See 47.2.2.
10GBASE-X PCS and PMA	2 048	4	See 48.5.
10GBASE-R PCS	3 584	7	See 49.2.15.
WIS	14 336	28	See 50.3.7.
LX4 PMD	512	1	Includes 2 m of fiber. See 53.2.
CX4 PMD	512	1	See 54.3.
Serial PMA and PMD (except LRM)	512	1	Includes 2 m of fiber. See 52.2.
LRM PMA and PMD	9 216	18	Includes 2 m of fiber. See 68.2.
10GBASE-T PHY	25 600	50	See 55.11.
10GBASE-T1 no interleave	10 240	20	See 149.10.
10GBASE-T1 2x interleave	13 824	27	See 149.10.
10GBASE-T1 4x interleave	20 480	40	See 149.10.
10GBASE-BRx RS-FEC	24 576	48	See 108.4.

[a] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

Table 44–3—Conversion table for cable delays

Speed relative to *c*	ns/m	BT/m
0.40	8.33	83.3
0.50	6.67	66.7
0.51	6.54	65.4
0.52	6.41	64.1
0.53	6.29	62.9
0.54	6.17	61.7
0.55	6.06	60.6
0.56	5.95	59.5
0.57	5.85	58.5

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Table 44–3—Conversion table for cable delays *(continued)*

Speed relative to *c*	ns/m	BT/m
0.58	5.75	57.5
0.5852	5.70	57.0
0.59	5.65	56.5
0.60	5.56	55.6
0.61	5.46	54.6
0.62	5.38	53.8
0.63	5.29	52.9
0.64	5.21	52.1
0.65	5.13	51.3
0.654	5.10	51.0
0.66	5.05	50.5
0.666	5.01	50.1
0.67	4.98	49.8
0.68	4.90	49.0
0.69	4.83	48.3
0.7	4.76	47.6
0.8	4.17	41.7
0.9	3.70	37.0

44.4 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 45 through Clause 55, Clause 68, and Clause 149, demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the 10 Gigabit Ethernet PICS conforms to the same notation and conventions used in 100BASE-T (see 21.6).

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45. Management Data Input/Output (MDIO) Interface

45.1 Overview

This clause defines the logical and electrical characteristics of an extension to the two signal Management Data Input/Output (MDIO) Interface specified in Clause 22.

The purpose of this extension is to provide the ability to access more device registers while still retaining logical compatibility with the MDIO interface defined in Clause 22. Clause 22 specifies the MDIO frame format and uses an ST code of 01 to access registers. In this clause, additional registers are added to the address space by defining MDIO frames that use an ST code of 00.

This extension to the MDIO interface is applicable to the following:

— Implementations that operate at speeds of 2.5 Gb/s and above.
— Implementations of 10PASS-TS and 2BASE-TL subscriber network Physical Layer devices.
— Implementations of 10, 100, or 1000 Mb/s with additional management functions beyond those defined in Clause 22.

The MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

Throughout this clause, an “a.b.c” format is used to identify register bits, where “a” is the device address, “b” is the register address, and “c” is the bit number within the register.

45.1.1 Summary of major concepts

The following are major concepts of the MDIO Interface:

a) Preserve the management frame structure defined in 22.2.4.5.
b) Define a mechanism to address more registers than specified in 22.2.4.5.
c) Define ST and OP codes to identify and control the extended access functions.
d) Provide an electrical interface specification that is compatible with common digital CMOS ASIC processes.

45.1.2 Application

This clause defines a management interface between Station Management (STA) and the sublayers that form a Physical Layer device (PHY) entity. Where a sublayer, or grouping of sublayers, is an individually manageable entity, it is known as an MDIO Manageable Device (MMD). This clause allows a single STA, through a single MDIO interface, to access up to 32 PHYs (defined as PRTAD in the frame format defined in 45.3) consisting of up to 32 MMDs as shown in Figure 45–1. The MDIO interface can support up to a maximum of 65 536 registers in each MMD.

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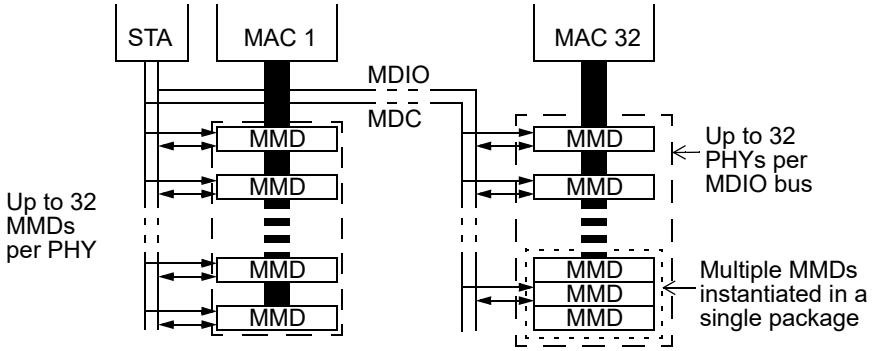

Figure 45–1—DTE and MMD devices

45.2 MDIO Interface registers

The management interface specified in Clause 22 provides a simple, two signal, serial interface to connect a Station Management entity and a managed PHY for providing access to management parameters and services. The interface is referred to as the MII management interface.

The MDIO interface is based on the MII management interface, but differs from it in several ways. The MDIO interface uses indirect addressing to create an extended address space allowing a much larger number of registers to be accessed within each MMD. The MDIO address space is orthogonal to the MII management interface address space. The mechanism for the addressing is defined in 45.3. The MDIO electrical interface operates at lower voltages than those specified for the MII management interface. The electrical interface is specified in 45.4. For cases where a single entity combines Clause 45 MMDs with Clause 22 registers, then the Clause 22 registers may be accessed using the Clause 45 electrical interface and the Clause 22 management frame structure. The list of possible MMDs is shown in Table 45–1. The PHY XS and DTE XS devices are the two partner devices used to extend the interface that sits immediately below the Reconciliation Sublayer. For 10 Gigabit Ethernet, the interface extenders are defined as the XGXS devices. For 10PASS-TS and 2BASE-TL, control and monitoring of the TC sublayer is defined in the TC MMD. For 10, 100 and 1000 Mb/s PHYs, further management capability is defined in the Clause 22 extension MMD.

Table 45–1—MDIO Manageable Device addresses

Device address	MMD name
0	Reserved
1	PMA/PMD
2	WIS
3	PCS
4	PHY XS
5	DTE XS
6	TC

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Table 45–1—MDIO Manageable Device addresses *(continued)*

Device address	MMD name
7	Auto-Negotiation
8	Separated PMA (1)
9	Separated PMA (2)
10	Separated PMA (3)
11	Separated PMA (4)
12	OFDM PMA/PMD
13	Power Unit
14 through 28	Reserved
29	Clause 22 extension
30	Vendor specific 1
31	Vendor specific 2

10PASS-TS and 2BASE-TL each have two port subtypes, 10PASS-TS-O, 10PASS-TS-R, 2BASE-TL-O and 2BASE-TL-R. Hereafter, referred to generically as -O and -R. The -O subtype corresponds to the port located at the service provider end of a subscriber link (the central office end). The -R subtype corresponds to the port located at the subscriber end of a subscriber link (the remote end). See 61.1 for more information.

Some register behavior may differ based on the port subtype. In the case where a register's behavior or definition differs between port subtypes, it is noted in the register description and in the bit definition tables (denoted by "O:" and "R:" in the R/W column).

The Clause 22 extension MMD allows new features to be added to 10, 100, and 1000 Mb/s PHYs beyond those already defined in Clause 22.

If a device supports the MDIO interface it shall respond to all possible register addresses for the device and return a value of zero for undefined and unsupported registers. Writes to undefined registers and read-only registers shall have no effect. The operation of an MMD shall not be affected by writes to reserved and unsupported register bits, and such register bits shall return a value of zero when read.

In the case of two registers that together form a 32-bit counter, whenever the most significant 16-bit register of the counter is read, the 32-bit counter value is latched into the register pair, the value being latched before the contents of the most significant 16 bits are driven on the MDIO interface and the contents of both registers are cleared to all zeros. A subsequent read from the least significant 16-bit register will return the least significant 16 bits of the latched value, but will not change the contents of the register pair. Writing to these registers has no effect. Counters that adhere to this behavior are marked in their bit definition tables with the tag "MW = Multi-word".

To ensure compatibility with future use of reserved bits and registers, the Management Entity should write to reserved bits with a value of zero and ignore reserved bits on read.

Some of the bits within MMD registers are defined as latching low (LL) or latching high (LH). When a bit is defined as latching low and the condition for the bit to be low has occurred, the bit shall remain low until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors. When a bit is defined as latching high and the condition for the bit to be high has occurred, the bit shall remain high until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors.

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For multi-bit fields, the lowest numbered bit of the field in the register corresponds to the least significant bit of the field.

Figure 45–2 describes the signal terminology used for the MMDs.

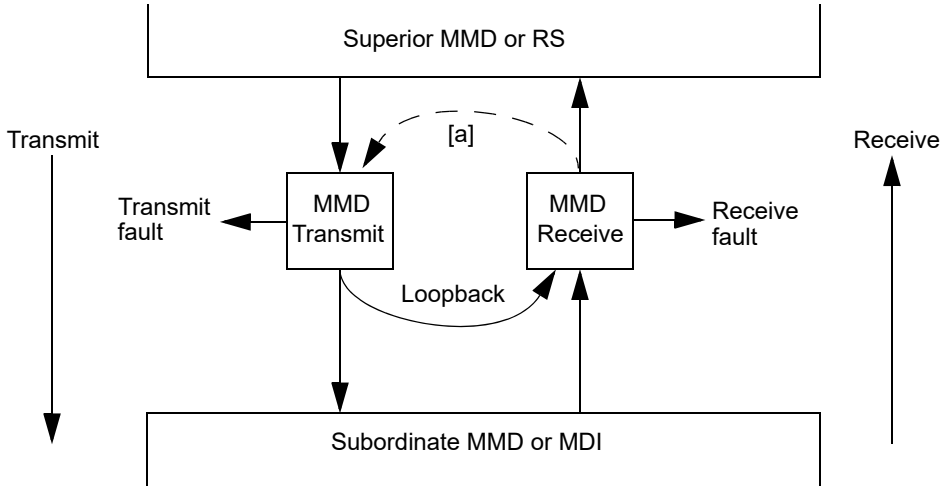

Figure 45–2—MMD signal terminology

[a] Direction of the optional PHY XS loopback

Each MMD contains registers 5 and 6, as defined in Table 45–2. Bits read as a one in this register indicate which MMDs are instantiated within the same package as the MMD being accessed. Bit 5.0 is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. Bit 6.13 indicates that Clause 22 functionality is extended using the Clause 45 electrical interface through MMD 29. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

Table 45–2—Devices in package registers bit definitions

Bit(s)[a]	Name	Description	R/W[b]
m.6.15	Vendor-specific device 2 present	1 = Vendor-specific device 2 present in package 0 = Vendor-specific device 2 not present in package	RO
m.6.14	Vendor-specific device 1 present	1 = Vendor-specific device 1 present in package 0 = Vendor-specific device 1 not present in package	RO
m.6.13	Clause 22 extension present	1 = Clause 22 extension present in package 0 = Clause 22 extension not present in package	RO
m.6.12:0	Reserved	Value always 0	RO
m.5.15:14	Reserved	Value always 0	RO
m.5.13	Power Unit present	1 = Power Unit present in package 0 = Power Unit not present in package	RO
m.5.12	OFDM	1 = OFDM present in package 0 = OFDM not present in package	RO

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Table 45–2—Devices in package registers bit definitions *(continued)*

Bit(s)[a]	Name	Description	R/W[b]
m.5.11	Separated PMA (4) present	1 = Separated PMA[c] (4) present in package 0 = Separated PMA (4) not present in package	RO
m.5.10	Separated PMA (3) present	1 = Separated PMA (3) present in package 0 = Separated PMA (3) not present in package	RO
m.5.9	Separated PMA (2) present	1 = Separated PMA (2) present in package 0 = Separated PMA (2) not present in package	RO
m.5.8	Separated PMA (1) present	1 = Separated PMA (1) present in package 0 = Separated PMA (1) not present in package	RO
m.5.7	Auto-Negotiation present	1 = Auto-Negotiation present in package 0 = Auto-Negotiation not present in package	RO
m.5.6	TC present	1 = TC present in package 0 = TC not present in package	RO
m.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
m.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
m.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
m.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
m.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
m.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

[a]m = address of MMD accessed (see Table 45–1)
[b]RO = Read only
[c]Separated PMAs are defined in 45.2.1

45.2.1 PMA/PMD registers

For devices operating at 25 Gb/s or higher speeds, the PMA may be instantiated as multiple sublayers (see 83.1.4, 109.1.4, and 120.1.4 for how MMD addresses are allocated to multiple PMA sublayers for the respective speeds). A PMA sublayer that is packaged with the PMD is addressed as MMD 1. More addressable instances of PMA sublayers, each one separated from lower addressable instances, may be implemented and addressed as MMD 8, 9, 10, and 11 where MMD 8 is the closest to the PMD and MMD 11 is the furthest from the PMD. The addresses and functions of all registers in MMD 8, 9, 10, and 11 are defined identically to MMD 1, except registers m.5 and m.6 as defined in Table 45–2.

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The assignment of registers in the PMA/PMD is shown in Table 45–3.

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.0	PMA/PMD control 1	45.2.1.1
1.1	PMA/PMD status 1	45.2.1.2
1.2, 1.3	PMA/PMD device identifier	45.2.1.3
1.4	PMA/PMD speed ability	45.2.1.4
1.5, 1.6	PMA/PMD devices in package	45.2.1.5
1.7	PMA/PMD control 2	45.2.1.6
1.8	PMA/PMD status 2	45.2.1.7
1.9	PMA/PMD transmit disable	45.2.1.8
1.10	PMD receive signal detect	45.2.1.9
1.11	PMA/PMD extended ability	45.2.1.10
1.12	10G-EPON PMA/PMD ability	45.2.1.11
1.13	40G/100G PMA/PMD extended ability	45.2.1.12
1.14, 1.15	PMA/PMD package identifier	45.2.1.13
1.16	EEE capability	45.2.1.14
1.17	EPoC PMA/PMD ability	45.2.1.15
1.18	BASE-T1 PMA/PMD extended ability	45.2.1.16
1.19	25G PMA/PMD extended ability	45.2.1.17
1.20	50G PMA/PMD extended ability	45.2.1.18
1.21	2.5G/5G PMA/PMD extended ability	45.2.1.19
1.22	BASE-H PMA/PMD extended ability	45.2.1.20
1.23	200G PMA/PMD extended ability	45.2.1.21
1.24	400G PMA/PMD extended ability	45.2.1.22
1.25	PMA/PMD extended ability 2	45.2.1.23
1.26	40G/100G PMA/PMD extended ability 2	45.2.1.24
1.27	PMD transmit disable extension	45.2.1.25
1.28	PMD receive signal detect extension	45.2.1.26
1.29	PMA/PMD control 3	45.2.1.27
1.30	10P/2B PMA/PMD control	45.2.1.28
1.31	10P/2B PMA/PMD status	45.2.1.29
1.32	10P/2B link partner PMA/PMD control[a]	45.2.1.30
1.33	10P/2B link partner PMA/PMD status[a]	45.2.1.31
1.34	BiDi PMA/PMD extended ability 1	45.2.1.32
1.35	BiDi PMA/PMD extended ability 2	45.2.1.33
1.36	10P/2B link loss counter	45.2.1.34
1.37	10P/2B RX SNR margin	45.2.1.35

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Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name	Subclause
1.38	10P/2B link partner RX SNR margin[a]	45.2.1.36
1.39	10P/2B line attenuation	45.2.1.37
1.40	10P/2B link partner line attenuation[a]	45.2.1.38
1.41	10P/2B line quality thresholds	45.2.1.39
1.42	2B link partner line quality thresholds[a]	45.2.1.40
1.43	10P FEC correctable errors counter	45.2.1.41
1.44	10P FEC uncorrectable errors counter	45.2.1.42
1.45	10P link partner FEC correctable errors[a]	45.2.1.43
1.46	10P link partner FEC uncorrectable errors[a]	45.2.1.44
1.47	10P electrical length	45.2.1.45
1.48	10P link partner electrical length[a]	45.2.1.46
1.49	10P PMA/PMD general configuration[a]	45.2.1.47
1.50	10P PSD configuration[a]	45.2.1.48
1.51, 1.52	10P downstream data rate configuration[a]	45.2.1.49
1.53	10P downstream Reed-Solomon configuration[a]	45.2.1.50
1.54, 1.55	10P upstream data rate[a]	45.2.1.51
1.56	10P upstream Reed-Solomon configuration[a]	45.2.1.52
1.57, 1.58	10P tone group	45.2.1.53
1.59, 1.60, 1.61, 1.62, 1.63	10P tone control parameters[a]	45.2.1.54
1.64	10P tone control action[a]	45.2.1.55
1.65, 1.66, 1.67	10P tone status	45.2.1.56
1.68	10P outgoing indicator bits	45.2.1.57
1.69	10P incoming indicator bits	45.2.1.58
1.70	10P cyclic extension configuration	45.2.1.59
1.71	10P attainable downstream data rate	45.2.1.60
1.72 through 1.79	Reserved	
1.80	2B general parameter	45.2.1.61
1.81 through 1.88	2B PMD parameters	45.2.1.62
1.89	2B code violation errors counter	45.2.1.63
1.90	2B link partner code violation errors[a]	45.2.1.64
1.91	2B errored seconds counter	45.2.1.65
1.92	2B link partner errored seconds[a]	45.2.1.66
1.93	2B severely errored seconds counter	45.2.1.67
1.94	2B link partner severely errored seconds[a]	45.2.1.68
1.95	2B LOSW counter	45.2.1.69
1.96	2B link partner LOSW[a]	45.2.1.70
1.97	2B unavailable seconds counter	45.2.1.71

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Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name	Subclause
1.98	2B link partner unavailable seconds[a]	45.2.1.72
1.99	2B state defects	45.2.1.73
1.100	2B link partner state defects[a]	45.2.1.74
1.101	2B negotiated constellation	45.2.1.75
1.102 through 1.109	2B extended PMD parameters	45.2.1.76
1.110 through 1.128	Reserved	
1.129	MultiGBASE-T status	45.2.1.77
1.130	MultiGBASE-T pair swap and polarity	45.2.1.78
1.131	MultiGBASE-T TX power backoff and PHY short reach setting	45.2.1.79
1.132	MultiGBASE-T test mode	45.2.1.80
1.133	SNR operating margin channel A	45.2.1.81
1.134	SNR operating margin channel B	45.2.1.82
1.135	SNR operating margin channel C	45.2.1.83
1.136	SNR operating margin channel D	45.2.1.84
1.137	Minimum margin channel A	45.2.1.85
1.138	Minimum margin channel B	45.2.1.86
1.139	Minimum margin channel C	45.2.1.87
1.140	Minimum margin channel D	45.2.1.88
1.141	RX signal power channel A	45.2.1.89
1.142	RX signal power channel B	45.2.1.90
1.143	RX signal power channel C	45.2.1.91
1.144	RX signal power channel D	45.2.1.92
1.145 through 1.146	MultiGBASE-T skew delay	45.2.1.93
1.147	MultiGBASE-T fast retrain status and control	45.2.1.94
1.148 through 1.149	Reserved	
1.150	BASE-R PMD control	45.2.1.95
1.151	BASE-R PMD status	45.2.1.96
1.152	BASE-R LP coefficient update, lane 0	45.2.1.97
1.153	BASE-R LP status report, lane 0	45.2.1.98
1.154	BASE-R LD coefficient update, lane 0	45.2.1.99
1.155	BASE-R LD status report, lane 0	45.2.1.100
1.156	BASE-R PMD status 2	45.2.1.101
1.157	BASE-R PMD status 3	45.2.1.102
1.158 through 1.159	Reserved	
1.160	1000BASE-KX/2.5GBASE-KX control	45.2.1.103
1.161	1000BASE-KX/2.5GBASE-KX status	45.2.1.104
1.162 through 1.164	PMA overhead control 1, 2, and 3	45.2.1.105

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Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name	Subclause
1.165, 1.166	PMA overhead status 1 and 2	45.2.1.106
1.167 through 1.169	Reserved	
1.170	BASE-R FEC ability	45.2.1.107
1.171	BASE-R FEC control	45.2.1.108
1.172 through 1.173	Single-lane PHY BASE-R FEC corrected blocks counter	45.2.1.109
1.174 through 1.175	Single-lane PHY BASE-R FEC uncorrected blocks counter	45.2.1.110
1.176 through 1.178	Reserved	
1.179	CAUI-4 C2M and 25GAUI C2M recommended CTLE	45.2.1.111
1.180	25GAUI C2C and lane 0 CAUI-4 C2C transmitter equalization, receive direction	45.2.1.112
1.181 through 1.183	CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 1 through lane 3	45.2.1.113
1.184	25GAUI C2C and lane 0 CAUI-4 C2C transmitter equalization, transmit direction	45.2.1.114
1.185 through 1.187	CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 3	45.2.1.115
1.188 through 1.199	Reserved	
1.200	RS-FEC control	45.2.1.116
1.201	RS-FEC status	45.2.1.117
1.202, 1.203	RS-FEC corrected codewords counter	45.2.1.118
1.204, 1.205	RS-FEC uncorrected codewords counter	45.2.1.119
1.206	RS-FEC lane mapping	45.2.1.120
1.207 through 1.209	Reserved	
1.210 through 1.217	RS-FEC symbol error counter, lane 0 to 3	45.2.1.121, 45.2.1.122
1.218 through 1.229	Reserved	
1.230 through 1.249	RS-FEC BIP error counter, lane 0 to 19	45.2.1.123, 45.2.1.124
1.250 through 1.269	RS-FEC PCS lane mapping, lane 0 to 19	45.2.1.125, 45.2.1.126
1.270 through 1.279	Reserved	
1.280 through 1.283	RS-FEC PCS alignment status 1 through 4	45.2.1.127 to 45.2.1.130
1.284 through 1.299	Reserved	
1.300 through 1.339	BASE-R FEC corrected blocks counter, lanes 0 through 19	45.2.1.131
1.340 through 1.399	Reserved	
1.400 through 1.407	200GAUI-8 and 400GAUI-16 chip-to-module recommended CTLE, lane 0 through lane 7	45.2.1.132, 45.2.1.133
1.408 through 1.415	400GAUI-16 chip-to-module recommended CTLE, lane 8 through lane 15	45.2.1.134
1.416 through 1.499	Reserved	

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Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name	Subclause
1.500 through 1.515	50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 through lane 15	45.2.1.135, 45.2.1.136
1.516 through 1.531	50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 through lane 15	45.2.1.137, 45.2.1.138
1.532 through 1.599	Reserved	
1.600	PMA precoder control Tx output	45.2.1.139
1.601	PMA precoder control Rx input	45.2.1.140
1.602	PMA precoder control Rx output	45.2.1.141
1.603	PMA precoder control Tx input	45.2.1.142
1.604	PMA precoder request flag	45.2.1.143
1.605	PMA precoder request Rx input status	45.2.1.144
1.606	PMA precoder request Tx input status	45.2.1.145
1.607 through 1.649	Reserved	
1.650, 1.651	RS-FEC degraded SER activate threshold	45.2.1.146
1.652, 1.653	RS-FEC degraded SER deactivate threshold	45.2.1.147
1.654, 1.655	RS-FEC degraded SER interval	45.2.1.148
1.656 through 1.699	Reserved	
1.700 through 1.739	BASE-R FEC uncorrected blocks counter, lanes 0 through 19	45.2.1.149
1.740 through 1.799	Reserved	
1.800	Tx optical channel control	45.2.1.150
1.801	Tx optical channel ability 1	45.2.1.151
1.802	Tx optical channel ability 2	45.2.1.152
1.803	Tx optical channel ability 3	45.2.1.153
1.804 through 1.819	Reserved	
1.820	Rx optical channel control	45.2.1.154
1.821	Rx optical channel ability 1	45.2.1.155
1.822	Rx optical channel ability 2	45.2.1.156
1.823	Rx optical channel ability 3	45.2.1.157
1.824 through 1.899	Reserved	
1.900	BASE-H PMA/PMD control	45.2.1.158
1.901 through 1.999	Reserved	
1.1000 through 1.1002	Nx25G-EPON PMA/PMD extended ability	45.2.1.159
1.1003 through 1.1099	Reserved	
1.1100	BASE-R LP coefficient update, lane 0 (copy)	45.2.1.97
1.1101 through 1.1109	BASE-R LP coefficient update, lanes 1 through 9	45.2.1.160
1.1110 through 1.1119	Reserved	
1.1120 through 1.1123	BASE-R PAM4 PMD training LP control, lane 0 through lane 3	45.2.1.161
1.1124 through 1.1199	Reserved	

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Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name	Subclause
1.1200	BASE-R LP status report, lane 0 (copy)	45.2.1.98
1.1201 through 1.1209	BASE-R LP status report, lanes 1 through 9	45.2.1.162
1.1210 through 1.1219	Reserved	
1.1220 through 1.1223	BASE-R PAM4 PMD training LP status, lane 0 through lane 3	45.2.1.163
1.1224 through 1.1299	Reserved	
1.1300	BASE-R LD coefficient update, lane 0 (copy)	45.2.1.99
1.1301 through 1.1309	BASE-R LD coefficient update, lanes 1 through 9	45.2.1.164
1.1310 through 1.1319	Reserved	
1.1320 through 1.1323	BASE-R PAM4 PMD training LD control, lane 0 through lane 3	45.2.1.165
1.1324 through 1.1399	Reserved	
1.1400	BASE-R LD status report, lane 0 (copy)	45.2.1.100
1.1401 through 1.1409	BASE-R LD status report, lanes 1 through 9	45.2.1.166
1.1410 through 1.1419	Reserved	
1.1420 through 1.1423	BASE-R PAM4 PMD training LD status, lane 0 through lane 3	45.2.1.167
1.1424 through 1.1449	Reserved	
1.1450 through 1.1453	PMD training pattern, lanes 0 to 3	45.2.1.168
1.1454 through 1.1499	Reserved	
1.1500	Test-pattern ability	45.2.1.169
1.1501	PRBS pattern testing control	45.2.1.170
1.1502 through 1.1509	Reserved	
1.1510	Square wave testing control	45.2.1.171
1.1511	Reserved	
1.1512	PRBS13Q testing control	45.2.1.172
1.1513 through 1.1599	Reserved	
1.1600 through 1.1615	PRBS Tx error counters, lane 0 through lane 15	45.2.1.173
1.1616 through 1.1699	Reserved	
1.1700 through 1.1715	PRBS Rx error counters, lane 0 through lane 15	45.2.1.174
1.1716 through 1.1799	Reserved	
1.1800	TimeSync PMA/PMD capability	45.2.1.175
1.1801 through 1.1804	TimeSync PMA/PMD transmit path data delay	45.2.1.176
1.1805 through 1.1808	TimeSync PMA/PMD receive path data delay	45.2.1.177
1.1809 through 1.1899	Reserved	
1.1900	10GPASS-XR control and status	45.2.1.178
1.1901	DS OFDM control	45.2.1.179
1.1902 through 1.1906	DS OFDM channel frequency control	45.2.1.180
1.1907	US OFDM control	45.2.1.181
1.1908	US OFDM channel frequency control	45.2.1.182

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Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name	Subclause
1.1909	US OFDMA pilot pattern	45.2.1.183
1.1910	Profile control	45.2.1.184
1.1911	DS PHY Link control	45.2.1.185
1.1912	US PHY Link control	45.2.1.186
1.1913 and 1.1914	PHY Discovery control	45.2.1.187
1.1915	New CNU control	45.2.1.188
1.1916 through 1.1920	New CNU info	45.2.1.189
1.1921	DS PHY Link frame counter	45.2.1.190
1.1922 and 1.1923	PMA/PMD timing offset	45.2.1.191
1.1924	PMA/PMD power offset	45.2.1.192
1.1925 and 1.1926	PMA/PMD ranging offset	45.2.1.193
1.1927 through 1.1929	DS PMA/PMD data rate	45.2.1.194
1.1930 through 1.1932	US PMA/PMD data rate	45.2.1.195
1.1933 and 1.1934	10GPASS-XR FEC codeword counter	45.2.1.196
1.1935 and 1.1936	10GPASS-XR FEC codeword success counter	45.2.1.197
1.1937 and 1.1938	10GPASS-XR FEC codeword fail counter	45.2.1.198
1.1939	PHY Link EPFH counter	45.2.1.199
1.1940	PHY Link EPFH error counter	45.2.1.200
1.1941	PHY Link EPCH counter	45.2.1.201
1.1942	PHY Link EPCH error counter	45.2.1.202
1.1943	PHY Link EMB counter	45.2.1.203
1.1944	PHY Link EMB error counter	45.2.1.204
1.1945	PHY Link FPMB counter	45.2.1.205
1.1946	PHY Link FPMB error counter	45.2.1.206
1.1947	US PHY Link response time	45.2.1.207
1.1948	10GPASS-XR modulation ability	45.2.1.208
1.1949	PHY Discovery Response power control	45.2.1.209
1.1950	US target receive power	45.2.1.210
1.1951 through 1.1955	DS transmit power	45.2.1.211
1.1956 and 1.1957	US receive power measurement	45.2.1.212
1.1958	Reported power	45.2.1.213
1.1959 through 1.2099	Reserved	
1.2100	BASE-T1 PMA/PMD control	45.2.1.214
1.2101	Reserved	
1.2102	100BASE-T1 PMA/PMD test control	45.2.1.215
1.2103 through 1.2199	Reserved	
1.2200	IFEC control	45.2.1.216

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Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name	Subclause
1.2201	IFEC status	45.2.1.217
1.2202, 1.2203	IFEC corrected codewords counter	45.2.1.218
1.2204, 1.2205	IFEC uncorrected codewords counter	45.2.1.219
1.2206	IFEC lane mapping	45.2.1.220
1.2207 through 1.2209	Reserved	
1.2210 through 1.2217	IFEC symbol error counter, lane 0 to 3	45.2.1.221, 45.2.1.222
1.2218 through 1.2245	Reserved	
1.2246	SC-FEC alignment status 1	45.2.1.223
1.2247	SC-FEC alignment status 2	45.2.1.224
1.2248, 1.2249	Reserved	
1.2250 through 1.2269	SC-FEC lane mapping, lane 0 through 19	45.2.1.225, 45.2.1.226
1.2270 through 1.2275	Reserved	
1.2276, 12277	SC-FEC corrected codewords counter	45.2.1.227
1.2278, 1.2279	SC-FEC uncorrected codewords counter	45.2.1.228
1.2280 through 1.2283	SC-FEC total bits	45.2.1.229
1.2284 through 1.2287	SC-FEC corrected bits	45.2.1.230
1.2288 through 1.2293	Reserved	
1.2294	10BASE-T1L PMA control	45.2.1.231
1.2295	10BASE-T1L PMA status	45.2.1.232
1.2296	10BASE-T1L test mode control	45.2.1.233
1.2297	10BASE-T1S PMA control	45.2.1.234
1.2298	10BASE-T1S PMA status	45.2.1.235
1.2299	10BASE-T1S test mode control	45.2.1.236
1.2300 through 1.2303	Reserved	
1.2304	1000BASE-T1 PMA control	45.2.1.237
1.2305	1000BASE-T1 PMA status	45.2.1.238
1.2306	1000BASE-T1 training	45.2.1.239
1.2307	1000BASE-T1 link partner training	45.2.1.240
1.2308	1000BASE-T1 test mode control	45.2.1.241
1.2309	MultiGBASE-T1 PMA control	45.2.1.242
1.2310	MultiGBASE-T1 PMA status	45.2.1.243
1.2311	MultiGBASE-T1 training	45.2.1.244
1.2312	MultiGBASE-T1 link partner training	45.2.1.245
1.2313	MultiGBASE-T1 test mode control	45.2.1.246
1.2314	MultiGBASE-T1 SNR operating margin	45.2.1.247
1.2315	MultiGBASE-T1 minimum SNR margin	45.2.1.248

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Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name	Subclause
1.2316	MultiGBASE-T1 user defined data	45.2.1.249
1.2317	MultiGBASE-T1 link partner user defined data	45.2.1.250
1.2318 through 1.32767	Reserved	
1.32 768 through 1.65 535	Vendor specific	

[a]Register is defined only for -O port types and is reserved for -R ports.

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

The assignment of bits in the PMA/PMD control 1 register is shown in Table 45–4. The default value for each bit of the PMA/PMD control 1 register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.0.15	Reset	1 = PMA/PMD reset 0 = Normal operation	R/W SC
1.0.14	Reserved	Value always 0	RO
1.0.13	Speed selection (LSB)	1.0.6 1.0.13 1 1 = bits 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
1.0.12	Reserved	Value always 0	RO
1.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
1.0.10:7	Reserved	Value always 0	RO
1.0.6	Speed selection (MSB)	1.0.6 1.0.13 1 1 = bits 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W

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Table 45–4—PMA/PMD control 1 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = 400 Gb/s 1 0 0 0 = 200 Gb/s 0 1 1 1 = 5 Gb/s 0 1 1 0 = 2.5 Gb/s 0 1 0 1 = 50 Gb/s 0 1 0 0 = 25 Gb/s 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
1.0.1	PMA remote loopback	1 = Enable PMA remote loopback mode 0 = Disable PMA remote loopback mode	R/W
1.0.0	PMA local loopback	1 = Enable PMA local loopback mode 0 = Disable PMA local loopback mode	R/W

[a]R/W = Read/Write, SC = Self-clearing, RO = Read only

45.2.1.1.1 Reset (1.0.15)

Resetting a PMA/PMD is accomplished by setting bit 1.0.15 to a one. This action shall set all PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PMA/PMD shall return a value of one in bit 1.0.15 when a reset is in progress; otherwise, it shall return a value of zero. A PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.0.15. During a reset, a PMD/PMA shall respond to reads from register bits 1.0.15 and 1.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication. The data path of a PMD, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

45.2.1.1.2 Low power (1.0.11)

A PMA/PMD may be placed into a low-power mode by setting bit 1.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PMA/PMD. The behavior of the PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.0.11 is zero.

NOTE—This operation will interrupt data communication. The data path of a PMD, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

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45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

For devices operating at 10 Mb/s, 100 Mb/s, or 1000 Mb/s the speed of the PMA/PMD may be selected using bits 13 and 6. The speed abilities of the PMA/PMD are advertised in the PMA/PMD speed ability register. These two bits use the same definition as the speed selection bits defined in Clause 22.

For devices not operating at 10 Mb/s, 100 Mb/s, or 1000 Mb/s, the speed of the PMA/PMD may be selected using bits 5 through 2. When bits 5 through 2 are set to 0000 the use of a 10G PMA/PMD is selected. More specific selection is performed using the PMA/PMD control 2 register (register 1.7) (see 45.2.1.6). The speed abilities of the PMA/PMD are advertised in the PMA/PMD speed ability register. A PMA/PMD may ignore writes to the PMA/PMD speed selection bits that select speeds it has not advertised in the PMA/PMD speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PMA/PMD speed selection defaults to a supported ability.

When set to 0001, bits 5:2 select the use of the 10PASS-TS or 2BASE-TL PMA/PMD. More specific mode selection is performed using the 10P/2B PMA control register (45.2.1.28).

When bits 5 through 2 are set to 0010 the use of a 40G PMA/PMD is selected; when set to 0011 the use of a 100G PMA/PMD is selected; when set to 0100 the use of a 25G PMA/PMD is selected; when set to 0101 the use of a 50G PMA/PMD is selected; when set to 0110 the use of a 2.5G PMA/PMD is selected; when set to 0111 the use of a 5G PMA/PMD is selected; when set to 1000 the use of a 200G PMA/PMD is selected; when set to 1001 the use of a 400G PMA/PMD is selected. More specific selection is performed using the PMA/PMD control 2 register (register 1.7) (see 45.2.1.6.3).

45.2.1.1.4 PMA remote loopback (1.0.1)

The PMA shall be placed in a remote loopback mode of operation when bit 1.0.1 is set to a one. When bit 1.0.1 is set to a one, the PMA shall accept data on the receive path and return it on the transmit path.

The remote loopback function is optional for all port types, except 2BASE-TL and 10PASS-TS, which do not support loopback. A device's ability to perform the remote loopback function is advertised in the remote loopback ability bit of the related speed-dependent status register. A PMA that is unable to perform the remote loopback function shall ignore writes to this bit and shall return a value of zero when read. For 25/40/100 Gb/s operation, the remote loopback ability bit is specified in register 1.13. For 200 Gb/s and 400 Gb/s operation, the remote loopback ability bit is specified in registers 1.23 and 1.24, respectively.

The default value of bit 1.0.1 is zero.

45.2.1.1.5 PMA local loopback (1.0.0)

The PMA shall be placed in a local loopback mode of operation when bit 1.0.0 is set to a one. When bit 1.0.0 is set to a one, the PMA shall accept data on the transmit path and return it on the receive path.

The local loopback function is mandatory for the 1000BASE-KX, 2.5GBASE-X, 5GBASE-R, 10GBASE-KR, 10GBASE-X, 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10 port type and optional for all other port types, except 2BASE-TL, 10PASS-TS, and 10/1GBASE-PRX, which do not support loopback. A PMA that is unable to perform the local loopback function shall ignore writes to this bit and shall return a value of zero when read. The local loopback functionality is detailed in the relevant PMA clause. For 10/25/40/100/200/400 Gb/s operation, the local loopback ability bit is specified in the PMA/PMD status 2 register.

The default value of bit 1.0.0 is zero.

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NOTE—The signal path through the PMA that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PMA circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.1.2 PMA/PMD status 1 register (Register 1.1)

The assignment of bits in the PMA/PMD status 1 register is shown in Table 45–5. All the bits in the PMA/PMD status 1 register are read only; therefore, a write to the PMA/PMD status 1 register shall have no effect.

Table 45–5—PMA/PMD status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1.15:10	Reserved	Value always 0	RO
1.1.9	PIASA	PMA ingress AUI stop ability	RO
1.1.8	PEASA	PMA egress AUI stop ability	RO
1.1.7	Fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.1.6:3	Reserved	Value always 0	RO
1.1.2	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL
1.1.1	Low-power ability	1 = PMA/PMD supports low-power mode 0 = PMA/PMD does not support low-power mode	RO
1.1.0	Reserved	Value always 0	RO

[a]RO = Read only, LL = Latching low

45.2.1.2.1 PMA ingress AUI stop ability (1.1.9)

If bit 1.1.9 is set to one, then the PMA is indicating that the PMA sublayer attached by the ingress AUI is permitted to stop signaling during LPI. If the bit is set to zero, then the PMA is indicating that the PMA sublayer attached by the ingress AUI is not permitted to stop signaling during LPI. If the PMA sublayer attached by the ingress AUI does not support EEE capability or is not capable to stop signaling, then this bit has no effect.

45.2.1.2.2 PMA egress AUI stop ability (1.1.8)

If bit 1.1.8 is set to one, then the PMA is indicating that the PMA sublayer attached by the egress AUI is permitted to stop signaling during LPI. If the bit is set to zero, then the PMA is indicating that the PMA sublayer attached by the egress AUI is not permitted to stop signaling during LPI. If the PMA sublayer attached by the egress AUI does not support EEE capability or is not capable to stop signaling, then this bit has no effect.

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45.2.1.2.3 Fault (1.1.7)

Fault is a global PMA/PMD variable. When read as a one, bit 1.1.7 indicates that either (or both) the PMA or the PMD has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 1.1.7 indicates that neither the PMA nor the PMD has detected a fault condition. For 10/25/40/50/100/200/400 Gb/s operation, bit 1.1.7 is set to a one when either of the fault bits (1.8.11, 1.8.10) located in register 1.8 are set to a one. For 10PASS-TS or 2BASE-TL operations, when read as a one, a fault has been detected and more detailed information is conveyed in 45.2.1.34, 45.2.1.57, 45.2.1.58, and 45.2.1.73.

45.2.1.2.4 Receive link status (1.1.2)

When read as a one, bit 1.1.2 indicates that the PMA/PMD receive link is up. When read as a zero, bit 1.1.2 indicates that the PMA/PMD receive link is down. The receive link status bit shall be implemented with latching low behavior.

While a 10PASS-TS or 2BASE-TL PMA/PMD is initializing, this bit shall indicate receive link down (see 45.2.1.29).

45.2.1.2.5 Low-power ability (1.1.1)

When read as a one, bit 1.1.1 indicates that the PMA/PMD supports the low-power feature. When read as a zero, bit 1.1.1 indicates that the PMA/PMD does not support the low-power feature. If a PMA/PMD supports the low-power feature, then it is controlled using the low-power bit 1.0.11.

45.2.1.3 PMA/PMD device identifier (Registers 1.2 and 1.3)

Registers 1.2 and 1.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PMA/PMD. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number.

A PMA/PMD may return a value of zero in each of the 32 bits of the PMA/PMD device identifier to indicate that a unique identifier as described above is not provided.

The format of the PMA/PMD device identifier is specified in 22.2.4.3.1.

NOTE—The use of only 22 bits of the OUI as described here has been deprecated by the IEEE Registration Authority. In this case, Company ID (CID) is not an acceptable alternative to OUI due to the possibility that a CID and OUI could be identical in the 22-bit subset. The definition of vendor-specific device identifiers for other applications is expected to use the full 24 bits to accommodate the use of either an OUI or CID.

45.2.1.4 PMA/PMD speed ability (Register 1.4)

The assignment of bits in the PMA/PMD speed ability register is shown in Table 45–6.

45.2.1.4.1 400G capable (1.4.15)

When read as a one, bit 1.4.15 indicates that the PMA/PMD is able to operate at a data rate of 400 Gb/s. When read as a zero, bit 1.4.15 indicates that the PMA/PMD is not able to operate at a data rate of 400 Gb/s.

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Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.4.15	400G capable	1 = PMA/PMD is capable of operating at 400 Gb/s 0 = PMA/PMD is not capable of operating at 400 Gb/s	RO
1.4.14	5G capable	1 = PMA/PMD is capable of operating at 5 Gb/s 0 = PMA/PMD is not capable of operating as 5 Gb/s	RO
1.4.13	2.5G capable	1 = PMA/PMD is capable of operating at 2.5 Gb/s 0 = PMA/PMD is not capable of operating as 2.5 Gb/s	RO
1.4.12	200G capable	1 = PMA/PMD is capable of operating at 200 Gb/s 0 = PMA/PMD is not capable of operating at 200 Gb/s	RO
1.4.11	25G capable	1 = PMA/PMD is capable of operating at 25 Gb/s 0 = PMA/PMD is not capable of operating at 25 Gb/s	RO
1.4.10	10GPASS-XR capable	1 = PMA/PMD is capable of operating as 10GPASS-XR 0 = PMA/PMD is not capable of operating as 10GPASS-XR	RO
1.4.9	100G capable	1 = PMA/PMD is capable of operating at 100 Gb/s 0 = PMA/PMD is not capable of operating as 100 Gb/s	RO
1.4.8	40G capable	1 = PMA/PMD is capable of operating at 40 Gb/s 0 = PMA/PMD is not capable of operating as 40 Gb/s	RO
1.4.7	10/1G capable	1 = PMA/PMD is capable of operating at 10 Gb/s downstream and 1 Gb/s upstream 0 = PMA/PMD is not capable of operating at 10 Gb/s downstream and 1 Gb/s upstream.	RO
1.4.6	10M capable	1 = PMA/PMD is capable of operating at 10 Mb/s 0 = PMA/PMD is not capable of operating as 10 Mb/s	RO
1.4.5	100M capable	1 = PMA/PMD is capable of operating at 100 Mb/s 0 = PMA/PMD is not capable of operating at 100 Mb/s	RO
1.4.4	1000M capable	1 = PMA/PMD is capable of operating at 1000 Mb/s 0 = PMA/PMD is not capable of operating at 1000 Mb/s	RO
1.4.3	50G capable	1 = PMA/PMD is capable of operating at 50 Gb/s 0 = PMA/PMD is not capable of operating at 50 Gb/s	RO
1.4.2	10PASS-TS capable	1 = PMA/PMD is capable of operating as 10PASS-TS 0 = PMA/PMD is not capable of operating as 10PASS-TS	RO
1.4.1	2BASE-TL capable	1 = PMA/PMD is capable of operating as 2BASE-TL 0 = PMA/PMD is not capable of operating as 2BASE-TL	RO
1.4.0	10G capable	1 = PMA/PMD is capable of operating at 10 Gb/s 0 = PMA/PMD is not capable of operating at 10 Gb/s	RO

[a]RO = Read only

45.2.1.4.2 5G capable (1.4.14)

When read as a one, bit 1.4.14 indicates that the PMA/PMD is able to operate at a data rate of 5 Gb/s. When read as a zero, bit 1.4.14 indicates that the PMA/PMD is not able to operate at a data rate of 5 Gb/s.

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45.2.1.4.3 2.5G capable (1.4.13)

When read as a one, bit 1.4.13 indicates that the PMA/PMD is able to operate at a data rate of 2.5 Gb/s. When read as a zero, bit 1.4.13 indicates that the PMA/PMD is not able to operate at a data rate of 2.5 Gb/s.

45.2.1.4.4 200G capable (1.4.12)

When read as a one, bit 1.4.12 indicates that the PMA/PMD is able to operate at a data rate of 200 Gb/s. When read as a zero, bit 1.4.12 indicates that the PMA/PMD is not able to operate at a data rate of 200 Gb/s.

45.2.1.4.5 25G capable (1.4.11)

When read as a one, bit 1.4.11 indicates that the PMA/PMD is able to operate at a data rate of 25 Gb/s. When read as a zero, bit 1.4.11 indicates that the PMA/PMD is not able to operate at a data rate of 25 Gb/s.

45.2.1.4.6 10GPASS-XR capable (1.4.10)

When read as one, bit 1.4.10 indicates that the PMA/PMD is able to operate as 10GPASS-XR. When read as zero, bit 1.4.10 indicates that the PMA/PMD is not able to operate as 10GPASS-XR.

45.2.1.4.7 100G capable (1.4.9)

When read as a one, bit 1.4.9 indicates that the PMA/PMD is able to operate at a data rate of 100 Gb/s. When read as a zero, bit 1.4.9 indicates that the PMA/PMD is not able to operate at a data rate of 100 Gb/s.

45.2.1.4.8 40G capable (1.4.8)

When read as a one, bit 1.4.8 indicates that the PMA/PMD is able to operate at a data rate of 40 Gb/s. When read as a zero, bit 1.4.8 indicates that the PMA/PMD is not able to operate at a data rate of 40 Gb/s.

45.2.1.4.9 10/1G capable (1.4.7)

When read as a one, bit 1.4.7 indicates that the PMA/PMD is able to operate at a data rate of 10 Gb/s in the downstream direction and 1 Gb/s in the upstream direction. When read as a zero, bit 1.4.7 indicates that the PMA/PMD is not able to operate at a data rate of 10 Gb/s in the downstream direction and 1 Gb/s in the upstream direction.

45.2.1.4.10 10M capable (1.4.6)

When read as a one, bit 1.4.6 indicates that the PMA/PMD is able to operate at a data rate of 10 Mb/s. When read as a zero, bit 1.4.6 indicates that the PMA/PMD is not able to operate at a data rate of 10 Mb/s.

45.2.1.4.11 100M capable (1.4.5)

When read as a one, bit 1.4.5 indicates that the PMA/PMD is able to operate at a data rate of 100 Mb/s. When read as a zero, bit 1.4.5 indicates that the PMA/PMD is not able to operate at a data rate of 100 Mb/s.

45.2.1.4.12 1000M capable (1.4.4)

When read as a one, bit 1.4.4 indicates that the PMA/PMD is able to operate at a data rate of 1000 Mb/s. When read as a zero, bit 1.4.4 indicates that the PMA/PMD is not able to operate at a data rate of 1000 Mb/s.

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45.2.1.4.13 50G capable (1.4.3)

When read as a one, bit 1.4.3 indicates that the PMA/PMD is able to operate at a data rate of 50 Gb/s. When read as a zero, bit 1.4.3 indicates that the PMA/PMD is not able to operate at a data rate of 50 Gb/s.

45.2.1.4.14 10PASS-TS capable (1.4.2)

When read as a one, bit 1.4.2 indicates that the PMA/PMD is able to operate as 10PASS-TS. When read as a zero, bit 1.4.2 indicates that the PMA/PMD is not able to operate as 10PASS-TS.

45.2.1.4.15 2BASE-TL capable (1.4.1)

When read as a one, bit 1.4.1 indicates that the PMA/PMD is able to operate as 2BASE-TL. When read as a zero, bit 1.4.1 indicates that the PMA/PMD is not able to operate as 2BASE-TL.

45.2.1.4.16 10G capable (1.4.0)

When read as a one, bit 1.4.0 indicates that the PMA/PMD is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 1.4.0 indicates that the PMA/PMD is not able to operate at a data rate of 10 Gb/s.

45.2.1.5 PMA/PMD devices in package (Registers 1.5 and 1.6)

The PMA/PMD devices in package registers are defined in Table 45–2.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

The assignment of bits in the PMA/PMD control 2 register is shown in Table 45–7.

45.2.1.6.1 PMA ingress AUI stop enable (1.7.9)

If bit 1.7.9 is set to one then the PMA may stop the ingress direction AUI signaling during LPI otherwise it shall keep active signaling on that AUI. If the PMA does not support EEE capability or is not able to stop the ingress direction AUI signaling (see 45.2.1.2.1) then this bit has no effect.

45.2.1.6.2 PMA egress AUI stop enable (1.7.8)

If bit 1.7.8 is set to one then the PMA may stop the egress direction AUI signaling during LPI otherwise it shall keep active signaling on that AUI. If the PMA does not support EEE capability or is not able to stop the egress direction AUI signaling (see 45.2.1.2.2) then this bit has no effect.

45.2.1.6.3 PMA/PMD type selection (1.7.6:0)

The PMA/PMD type of the PMA/PMD shall be selected using bits 6 to 0. The PMA/PMD type abilities of the PMA/PMD are advertised in bits 9 and 7 through 0 of the PMA/PMD status 2 register; the PMA/PMD extended ability register; the 40G/100G PMA/PMD extended ability register; the 50G PMA/PMD extended ability register; the 200G PMA/PMD extended ability register; and the 400G PMA/PMD extended ability register. A PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

The PMA/PMD type selection defaults to a supported ability.

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Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:10	Reserved	Value always 0	RO
1.7.9	PIASE	PMA ingress AUI stop enable	R/W
1.7.8	PEASE	PMA egress AUI stop enable	R/W
1.7.7	Reserved	Value always 0	RO
1.7.6:0	PMA/PMD type selection	6 5 4 3 2 1 0 1 1 1 1 1 x x = reserved 1 1 1 1 0 1 x = reserved 1 1 1 1 0 0 1 = reserved 1 1 1 1 0 0 0 = 50GBASE-BR40-U PMA/PMD 1 1 1 0 1 1 1 = 50GBASE-BR20-U PMA/PMD 1 1 1 0 1 1 0 = 50GBASE-BR10-U PMA/PMD 1 1 1 0 1 0 1 = 50GBASE-BR40-D PMA/PMD 1 1 1 0 1 0 0 = 50GBASE-BR20-D PMA/PMD 1 1 1 0 0 1 1 = 50GBASE-BR10-D PMA/PMD 1 1 1 0 0 1 0 = 25GBASE-BR40-U PMA/PMD 1 1 1 0 0 0 1 = 25GBASE-BR20-U PMA/PMD 1 1 1 0 0 0 0 = 25GBASE-BR10-U PMA/PMD 1 1 0 1 1 1 1 = 25GBASE-BR40-D PMA/PMD 1 1 0 1 1 1 0 = 25GBASE-BR20-D PMA/PMD 1 1 0 1 1 0 1 = 25GBASE-BR10-D PMA/PMD 1 1 0 1 1 0 0 = 10GBASE-BR40-U PMA/PMD 1 1 0 1 0 1 1 = 10GBASE-BR20-U PMA/PMD 1 1 0 1 0 1 0 = 10GBASE-BR10-U PMA/PMD 1 1 0 1 0 0 1 = 10GBASE-BR40-D PMA/PMD 1 1 0 1 0 0 0 = 10GBASE-BR20-D PMA/PMD 1 1 0 0 1 1 1 = 10GBASE-BR10-D PMA/PMD 1 1 0 0 1 1 0 = reserved 1 1 0 0 1 0 x = reserved 1 1 0 0 0 1 1 = 400GBASE-ER8 PMA/PMD 1 1 0 0 0 1 0 = 400GBASE-LR4-6 PMA/PMD 1 1 0 0 0 0 1 = 400GBASE-FR4 PMA/PMD 1 1 0 0 0 0 0 = 400GBASE-SR4.2 PMA/PMD 1 0 1 1 1 1 1 = 400GBASE-SR8 PMA/PMD 1 0 1 1 1 1 0 = reserved 1 0 1 1 1 0 1 = reserved 1 0 1 1 1 0 0 = 400GBASE-LR8 PMA/PMD 1 0 1 1 0 1 1 = 400GBASE-FR8 PMA/PMD 1 0 1 1 0 1 0 = 400GBASE-DR4 PMA/PMD 1 0 1 1 0 0 1 = 400GBASE-SR16 PMA/PMD 1 0 1 1 0 0 0 = 200GBASE-ER4 PMA/PMD 1 0 1 0 1 1 x = reserved 1 0 1 0 1 0 1 = 200GBASE-LR4 PMA/PMD 1 0 1 0 1 0 0 = 200GBASE-FR4 PMA/PMD 1 0 1 0 0 1 1 = 200GBASE-DR4 PMA/PMD 1 0 1 0 0 1 0 = 200GBASE-SR4 PMA/PMD 1 0 1 0 0 0 1 = 200GBASE-CR4 PMA/PMD 1 0 1 0 0 0 0 = 200GBASE-KR4 PMA/PMD 1 0 0 1 1 1 1 = reserved 1 0 0 1 1 1 0 = 100GBASE-ZR PMA/PMD 1 0 0 1 1 0 1 = 100GBASE-LR1 PMA/PMD 1 0 0 1 1 0 0 = 100GBASE-FR1 PMA/PMD 1 0 0 1 0 1 1 = 100GBASE-DR PMA/PMD 1 0 0 1 0 1 0 = 100GBASE-SR2 PMA/PMD 1 0 0 1 0 0 1 = 100GBASE-CR2 PMA/PMD	R/W

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Table 45–7—PMA/PMD control 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.7.6:0 (*continued*)	PMA/PMD type selection (*continued*)	1 0 0 1 0 0 0 = 100GBASE-KR2 PMA/PMD 1 0 0 0 1 1 x = reserved 1 0 0 0 1 0 1 = 50GBASE-ER PMA/PMD 1 0 0 0 1 0 0 = 50GBASE-LR PMA/PMD 1 0 0 0 0 1 1 = 50GBASE-FR PMA/PMD 1 0 0 0 0 1 0 = 50GBASE-SR PMA/PMD 1 0 0 0 0 0 1 = 50GBASE-CR PMA/PMD 1 0 0 0 0 0 0 = 50GBASE-KR PMA/PMD 0 1 1 1 1 1 x = reserved 0 1 1 1 1 0 1 = BASE-T1 PMA/PMD[b] 0 1 1 1 1 0 0 = 5GBASE-KR PMA/PMD 0 1 1 1 0 1 1 = 2.5GBASE-KX PMA/PMD 0 1 1 1 0 1 0 = 25GBASE-SR PMA/PMD 0 1 1 1 0 0 1 = 25GBASE-KR or 25GBASE-KR-S PMA/PMD 0 1 1 1 0 0 0 = 25GBASE-CR or 25GBASE-CR-S PMA/PMD 0 1 1 0 1 1 1 = 25GBASE-T PMA 0 1 1 0 1 1 0 = 25GBASE-ER PMA/PMD 0 1 1 0 1 0 1 = 25GBASE-LR PMA/PMD 0 1 1 0 1 0 0 = BASE-H PMA/PMD[c] 0 1 1 0 0 1 1 = 10GPASS-XR-U PMA/PMD 0 1 1 0 0 1 0 = 10GPASS-XR-D PMA/PMD 0 1 1 0 0 0 1 = 5GBASE-T PMA 0 1 1 0 0 0 0 = 2.5GBASE-T PMA 0 1 0 1 1 1 1 = 100GBASE-SR4 PMA/PMD 0 1 0 1 1 1 0 = 100GBASE-CR4 PMA/PMD 0 1 0 1 1 0 1 = 100GBASE-KR4 PMA/PMD 0 1 0 1 1 0 0 = 100GBASE-KP4 PMA/PMD 0 1 0 1 0 1 1 = 100GBASE-ER4 PMA/PMD 0 1 0 1 0 1 0 = 100GBASE-LR4 PMA/PMD 0 1 0 1 0 0 1 = 100GBASE-SR10 PMA/PMD 0 1 0 1 0 0 0 = 100GBASE-CR10 PMA/PMD 0 1 0 0 1 1 1 = reserved 0 1 0 0 1 1 0 = 40GBASE-T PMA 0 1 0 0 1 0 1 = 40GBASE-ER4 PMA/PMD 0 1 0 0 1 0 0 = 40GBASE-FR PMA/PMD 0 1 0 0 0 1 1 = 40GBASE-LR4 PMA/PMD 0 1 0 0 0 1 0 = 40GBASE-SR4 PMA/PMD 0 1 0 0 0 0 1 = 40GBASE-CR4 PMA/PMD 0 1 0 0 0 0 0 = 40GBASE-KR4 PMA/PMD 0 0 1 1 1 1 1 = 10/1GBASE-PRX-U4 0 0 1 1 1 1 0 = 10GBASE-PR-U4 0 0 1 1 1 0 1 = 10/1GBASE-PRX-D4 0 0 1 1 1 0 0 = 10GBASE-PR-D4 0 0 1 1 0 1 1 = reserved 0 0 1 1 0 1 0 = 10GBASE-PR-U3 0 0 1 1 0 0 1 = 10GBASE-PR-U1 0 0 1 1 0 0 0 = 10/1GBASE-PRX-U3 0 0 1 0 1 1 1 = 10/1GBASE-PRX-U2 0 0 1 0 1 1 0 = 10/1GBASE-PRX-U1 0 0 1 0 1 0 1 = 10GBASE-PR-D3 0 0 1 0 1 0 0 = 10GBASE-PR-D2 0 0 1 0 0 1 1 = 10GBASE-PR-D1 0 0 1 0 0 1 0 = 10/1GBASE-PRX-D3 0 0 1 0 0 0 1 = 10/1GBASE-PRX-D2 0 0 1 0 0 0 0 = 10/1GBASE-PRX-D1 0 0 0 1 1 1 1 = 10BASE-T PMA/PMD 0 0 0 1 1 1 0 = 100BASE-TX PMA/PMD 0 0 0 1 1 0 1 = 1000BASE-KX PMA/PMD 0 0 0 1 1 0 0 = 1000BASE-T PMA/PMD	R/W

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Table 45–7—PMA/PMD control 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.7.6:0 (*continued*)	PMA/PMD type selection (*continued*)	0 0 0 1 0 1 1 = 10GBASE-KR PMA/PMD 0 0 0 1 0 1 0 = 10GBASE-KX4 PMA/PMD 0 0 0 1 0 0 1 = 10GBASE-T PMA 0 0 0 1 0 0 0 = 10GBASE-LRM PMA/PMD 0 0 0 0 1 1 1 = 10GBASE-SR PMA/PMD 0 0 0 0 1 1 0 = 10GBASE-LR PMA/PMD 0 0 0 0 1 0 1 = 10GBASE-ER PMA/PMD 0 0 0 0 1 0 0 = 10GBASE-LX4 PMA/PMD 0 0 0 0 0 1 1 = 10GBASE-SW PMA/PMD 0 0 0 0 0 1 0 = 10GBASE-LW PMA/PMD 0 0 0 0 0 0 1 = 10GBASE-EW PMA/PMD 0 0 0 0 0 0 0 = 10GBASE-CX4 PMA/PMD	

[a]R/W = Read/Write, RO = Read only
[b]If BASE-T1 is selected, bits 1.2100.3:0 are used to differentiate which BASE-T1 PMA/PMD is selected.
[c]If BASE-H PMA/PMD is selected, register 1.900 is used to differentiate which BASE-H PMA/PMD is selected.

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

The assignment of bits in the PMA/PMD status 2 register is shown in Table 45–8. All the bits in the PMA/PMD status 2 register are read only; a write to the PMA/PMD status 2 register shall have no effect.

Table 45–8—PMA/PMD status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
1.8.13	Transmit fault ability	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path	RO
1.8.12	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
1.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
1.8.9	Extended abilities	1 = PMA/PMD has extended abilities listed in register 1.11 0 = PMA/PMD does not have extended abilities	RO
1.8.8	PMD transmit disable ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO
1.8.7	10GBASE-SR ability	1 = PMA/PMD is able to perform 10GBASE-SR 0 = PMA/PMD is not able to perform 10GBASE-SR	RO

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Table 45–8—PMA/PMD status 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.8.6	10GBASE-LR ability	1 = PMA/PMD is able to perform 10GBASE-LR 0 = PMA/PMD is not able to perform 10GBASE-LR	RO
1.8.5	10GBASE-ER ability	1 = PMA/PMD is able to perform 10GBASE-ER 0 = PMA/PMD is not able to perform 10GBASE-ER	RO
1.8.4	10GBASE-LX4 ability	1 = PMA/PMD is able to perform 10GBASE-LX4 0 = PMA/PMD is not able to perform 10GBASE-LX4	RO
1.8.3	10GBASE-SW ability	1 = PMA/PMD is able to perform 10GBASE-SW 0 = PMA/PMD is not able to perform 10GBASE-SW	RO
1.8.2	10GBASE-LW ability	1 = PMA/PMD is able to perform 10GBASE-LW 0 = PMA/PMD is not able to perform 10GBASE-LW	RO
1.8.1	10GBASE-EW ability	1 = PMA/PMD is able to perform 10GBASE-EW 0 = PMA/PMD is not able to perform 10GBASE-EW	RO
1.8.0	PMA local loopback ability	1 = PMA has the ability to perform a local loopback function 0 = PMA does not have the ability to perform a local loopback function	RO

[a]RO = Read only, LH = Latching high

45.2.1.7.1 Device present (1.8.15:14)

When read as <10>, bits 1.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 1.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.1.7.2 Transmit fault ability (1.8.13)

When read as a one, bit 1.8.13 indicates that the PMA/PMD has the ability to detect a fault condition on the transmit path. When read as a zero, bit 1.8.13 indicates that the PMA/PMD does not have the ability to detect a fault condition on the transmit path.

45.2.1.7.3 Receive fault ability (1.8.12)

When read as a one, bit 1.8.12 indicates that the PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.8.12 indicates that the PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.7.4 Transmit fault (1.8.11)

When read as a one, bit 1.8.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.8.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.8.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The description of the transmit fault function for the various PMA/PMDs is given in Table 45–9.

The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 1.8.11 is zero.

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Table 45–9—Transmit fault description location

PMA/PMD	Description location
10BASE-T1L	146.4.2
100BASE-T1	96.4.2
2.5GBASE-KX	128.6.8
2.5GBASE-T, 5GBASE-T	126.4.2.2
2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1	149.4.2.2
5GBASE-KR	130.6.8
10GBASE-BR10, 10GBASE-BR20, 10GBASE-BR40	158.5.8
10GBASE-KR	72.6.8
10GBASE-LRM	68.4.8
10GBASE-S, 10GBASE-L, 10GBASE-E	52.4.8
10GBASE-LX4	53.4.10
10GBASE-CX4	54.5.10
10GBASE-T	55.4.2.2
10GBASE-KX4	71.6.10
25GBASE-KR, 25GBASE-KR-S	111.7.8
25GBASE-CR, 25GBASE-CR-S	110.7.8
25GBASE-SR	112.5.8
25GBASE-LR, 25GBASE-ER	114.5.8
25GBASE-BR10, 25GBASE-BR20, 25GBASE-BR40	159.5.8
25GBASE-T	113.4.2.2
40GBASE-KR4	84.7.10
40GBASE-CR4, 100GBASE-CR10	85.7.10
40GBASE-SR4, 100GBASE-SR10	86.5.10
40GBASE-LR4, 40GBASE-ER4	87.5.10
40GBASE-FR	89.5.8
40GBASE-T	113.4.2.2
50GBASE-KR, 100GBASE-KR2, 200GBASE-KR4	137.8.9
50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4	136.8.9
50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, 400GBASE-SR8	138.5.10
50GBASE-FR, 50GBASE-LR, 50GBASE-ER	139.5.8
50GBASE-BR10, 50GBASE-BR20, 50GBASE-BR40	160.5.8
100GBASE-KP4	94.3.8
100GBASE-KR4	93.7.10

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Table 45–9—Transmit fault description location *(continued)*

PMA/PMD	Description location
100GBASE-CR4	92.7.10
100GBASE-SR4	95.5.10
100GBASE-DR, 100GBASE-FR1, 100GBASE-LR1	140.5.8
100GBASE-LR4, 100GBASE-ER4	88.5.10
100GBASE-ZR	154.5.8
200GBASE-DR4	121.5.10
200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, 400GBASE-ER8	122.5.10
400GBASE-SR16	123.5.10
400GBASE-SR4.2	150.5.10
400GBASE-DR4	124.5.10
400GBASE-FR4, 400GBASE-LR4-6	151.5.10

45.2.1.7.5 Receive fault (1.8.10)

When read as a one, bit 1.8.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.8.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.8.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The description of the receive fault function for the various PMA/PMDs is given in Table 45–10.

Table 45–10—Receive fault description location

PMA/PMD	Description location
10BASE-T1L	146.4.3
100BASE-T1	96.4.3
2.5GBASE-KX	128.6.9
2.5GBASE-T, 5GBASE-T	126.4.2.4
2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1	149.4.2.3
5GBASE-KR	130.6.9
10GBASE-BR10, 10GBASE-BR20, 10GBASE-BR40	158.5.9
10GBASE-KR	72.6.9
10GBASE-LRM	68.4.9
10GBASE-S, 10GBASE-L, 10GBASE-E	52.4.9
10GBASE-LX4	53.4.11

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Table 45–10—Receive fault description location *(continued)*

PMA/PMD	Description location
10GBASE-CX4	54.5.11
10GBASE-T	55.4.2.4
10GBASE-KX4	71.6.11
25GBASE-KR, 25GBASE-KR-S	111.7.9
25GBASE-CR, 25GBASE-CR-S	110.7.9
25GBASE-SR	112.5.9
25GBASE-LR, 25GBASE-ER	114.5.9
25GBASE-BR10, 25GBASE-BR20, 25GBASE-BR40	159.5.9
25GBASE-T	113.4.2.4
40GBASE-KR4	84.7.11
40GBASE-CR4, 100GBASE-CR10	85.7.11
40GBASE-SR4, 100GBASE-SR10	86.5.11
40GBASE-LR4, 40GBASE-ER4	87.5.11
40GBASE-FR	89.5.9
40GBASE-T	113.4.2.4
50GBASE-KR, 100GBASE-KR2, 200GBASE-KR4	137.8.10
50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4	136.8.10
50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, 400GBASE-SR8	138.5.11
50GBASE-FR, 50GBASE-LR, 50GBASE-ER	139.5.9
50GBASE-BR10, 50GBASE-BR20, 50GBASE-BR40	160.5.9
100GBASE-KP4	94.3.9
100GBASE-KR4	93.7.11
100GBASE-CR4	92.7.11
100GBASE-SR4	95.5.11
100GBASE-DR, 100GBASE-FR1, 100GBASE-LR1	140.5.9
100GBASE-LR4, 100GBASE-ER4	88.5.11
100GBASE-ZR	154.5.9
200GBASE-DR4	121.5.11
200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, 400GBASE-ER8	122.5.11
400GBASE-SR16	123.5.11
400GBASE-SR4.2	150.5.11
400GBASE-DR4	124.5.11
400GBASE-FR4, 400GBASE-LR4-6	151.5.11

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The receive fault bit shall be implemented with latching high behavior.

45.2.1.7.6 PMA/PMD extended abilities (1.8.9)

When read as a one, bit 1.8.9 indicates that the PMA/PMD has extended abilities listed in register 1.11. When read as a zero, bit 1.8.9 indicates that the PMA/PMD does not have extended abilities.

45.2.1.7.7 PMD transmit disable ability (1.8.8)

When read as a one, bit 1.8.8 indicates that the PMD is able to perform the transmit disable function. When read as a zero, bit 1.8.8 indicates that the PMD is not able to perform the transmit disable function. If a PMD is able to perform the transmit disable function, then it is controlled using the PMD transmit disable register.

45.2.1.7.8 10GBASE-SR ability (1.8.7)

When read as a one, bit 1.8.7 indicates that the PMA/PMD is able to support a 10GBASE-SR PMA/PMD type. When read as a zero, bit 1.8.7 indicates that the PMA/PMD is not able to support a 10GBASE-SR PMA/PMD type.

45.2.1.7.9 10GBASE-LR ability (1.8.6)

When read as a one, bit 1.8.6 indicates that the PMA/PMD is able to support a 10GBASE-LR PMA/PMD type. When read as a zero, bit 1.8.6 indicates that the PMA/PMD is not able to support a 10GBASE-LR PMA/PMD type.

45.2.1.7.10 10GBASE-ER ability (1.8.5)

When read as a one, bit 1.8.5 indicates that the PMA/PMD is able to support a 10GBASE-ER PMA/PMD type. When read as a zero, bit 1.8.5 indicates that the PMA/PMD is not able to support a 10GBASE-ER PMA/PMD type.

45.2.1.7.11 10GBASE-LX4 ability (1.8.4)

When read as a one, bit 1.8.4 indicates that the PMA/PMD is able to support a 10GBASE-LX4 PMA/PMD type. When read as a zero, bit 1.8.4 indicates that the PMA/PMD is not able to support a 10GBASE-LX4 PMA/PMD type.

45.2.1.7.12 10GBASE-SW ability (1.8.3)

When read as a one, bit 1.8.3 indicates that the PMA/PMD is able to support a 10GBASE-SW PMA/PMD type. When read as a zero, bit 1.8.3 indicates that the PMA/PMD is not able to support a 10GBASE-SW PMA/PMD type.

45.2.1.7.13 10GBASE-LW ability (1.8.2)

When read as a one, bit 1.8.2 indicates that the PMA/PMD is able to support a 10GBASE-LW PMA/PMD type. When read as a zero, bit 1.8.2 indicates that the PMA/PMD is not able to support a 10GBASE-LW PMA/PMD type.

45.2.1.7.14 10GBASE-EW ability (1.8.1)

When read as a one, bit 1.8.1 indicates that the PMA/PMD is able to support a 10GBASE-EW PMA/PMD type. When read as a zero, bit 1.8.1 indicates that the PMA/PMD is not able to support a 10GBASE-EW PMA/PMD type.

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45.2.1.7.15 PMA local loopback ability (1.8.0)

When read as a one, bit 1.8.0 indicates that the PMA is able to perform the local loopback function. When read as a zero, bit 1.8.0 indicates that the PMA is not able to perform the local loopback function. If a PMA is able to perform the local loopback function, then it is controlled using the PMA local loopback bit 1.0.0.

45.2.1.8 PMD transmit disable register (Register 1.9)

The assignment of bits in the PMD transmit disable register is shown in Table 45–11. The transmit disable functionality is optional and a PMD's ability to perform the transmit disable functionality is advertised in the PMD transmit disable ability bit 1.8.8. A PMD that does not implement the transmit disable functionality shall ignore writes to the PMD transmit disable register and may return a value of zero for all bits. A PMD device that operates using a single lane and has implemented the transmit disable function shall use bit 1.9.0 to control the function. Such devices shall ignore writes to bits 1.9.15:1 and return a value of zero for those bits when they are read. The description of the transmit disable function for the various PMA/PMDs is given in Table 45–12.

NOTE 1—This register is extended by the PMD transmit disable extension register (see 45.2.1.25).

NOTE 2—Disabling the transmitter on one or more lanes stops the entire link from carrying data.

Table 45–11—PMD transmit disable register bit definitions

Bit(s)	Name	Description	R/W[a]
1.9.15	PMD transmit disable 14	1 = Disable output on transmit lane 14 0 = Enable output on transmit lane 14	R/W
1.9.14	PMD transmit disable 13	1 = Disable output on transmit lane 13 0 = Enable output on transmit lane 13	R/W
1.9.13	PMD transmit disable 12	1 = Disable output on transmit lane 12 0 = Enable output on transmit lane 12	R/W
1.9.12	PMD transmit disable 11	1 = Disable output on transmit lane 11 0 = Enable output on transmit lane 11	R/W
1.9.11	PMD transmit disable 10	1 = Disable output on transmit lane 10 0 = Enable output on transmit lane 10	R/W
1.9.10	PMD transmit disable 9	1 = Disable output on transmit lane 9 0 = Enable output on transmit lane 9	R/W
1.9.9	PMD transmit disable 8	1 = Disable output on transmit lane 8 0 = Enable output on transmit lane 8	R/W
1.9.8	PMD transmit disable 7	1 = Disable output on transmit lane 7 0 = Enable output on transmit lane 7	R/W
1.9.7	PMD transmit disable 6	1 = Disable output on transmit lane 6 0 = Enable output on transmit lane 6	R/W
1.9.6	PMD transmit disable 5	1 = Disable output on transmit lane 5 0 = Enable output on transmit lane 5	R/W
1.9.5	PMD transmit disable 4	1 = Disable output on transmit lane 4 0 = Enable output on transmit lane 4	R/W
1.9.4	PMD transmit disable 3	1 = Disable output on transmit lane 3 0 = Enable output on transmit lane 3	R/W

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Table 45–11—PMD transmit disable register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.9.3	PMD transmit disable 2	1 = Disable output on transmit lane 2 0 = Enable output on transmit lane 2	R/W
1.9.2	PMD transmit disable 1	1 = Disable output on transmit lane 1 0 = Enable output on transmit lane 1	R/W
1.9.1	PMD transmit disable 0	1 = Disable output on transmit lane 0 0 = Enable output on transmit lane 0	R/W
1.9.0	Global PMD transmit disable	1 = Disable transmitter output 0 = Enable transmitter output	R/W

[a]R/W = Read/Write

45.2.1.8.1 PMD transmit disable 14 (1.9.15)

When bit 1.9.15 is set to a one, the PMD shall disable output on lane 14 of the transmit path. When bit 1.9.15 is set to zero, the PMD shall enable output on lane 14 of the transmit path.

The default value for bit 1.9.15 is zero.

NOTE—Transmission will not be enabled when this bit is set to zero unless the global PMD transmit disable bit is also zero.

Table 45–12—Transmit disable description location

PMA/PMD	Description location
2.5GBASE-KX	128.6.5
2.5GBASE-T and 5GBASE-T	126.4.2.3
5GBASE-KR	130.6.5
10GBASE-BR10, 10GBASE-BR20, and 10GBASE-BR40	158.5.6
10GBASE-KR	72.6.5
10GBASE-LRM	68.4.7
Other 10GBASE-R	52.4.7
10GBASE-LX4	53.4.7
10GBASE-CX4	54.5.6
10GBASE-T	55.4.2.3
10GBASE-KX4	71.6.6
25GBASE-KR and 25GBASE-KR-S	111.7.5
25GBASE-CR and 25GBASE-CR-S	110.7.5
25GBASE-SR	112.5.6
25GBASE-LR and 25GBASE-ER	114.5.6

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Table 45–12—Transmit disable description location *(continued)*

PMA/PMD	Description location
25GBASE-BR10, 25GBASE-BR20, and 25GBASE-BR40	159.5.6
25GBASE-T	113.4.2.3
40GBASE-KR4	84.7.6
40GBASE-CR4 and 100GBASE-CR10	85.7.6
40GBASE-SR4 and 100GBASE-SR10	86.5.7
40GBASE-LR4 and 40GBASE-ER4	87.5.7
40GBASE-FR	89.5.6
40GBASE-T	113.4.2.3
50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4	137.8.6
50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4	136.8.6
50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8	138.5.7
50GBASE-FR, 50GBASE-LR, and 50GBASE-ER	139.5.6
50GBASE-BR10, 50GBASE-BR20, and 50GBASE-BR40	160.5.6
100GBASE-KP4	94.3.6.6
100GBASE-KR4	93.7.6
100GBASE-CR4	92.7.6
100GBASE-SR4	95.5.7
100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1	140.5.6
100GBASE-LR4 and 100GBASE-ER4	88.5.7
100GBASE-ZR	154.5.6
200GBASE-DR4	121.5.7
200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8	122.5.7
400GBASE-SR16	123.5.7
400GBASE-SR4.2	150.5.7
400GBASE-DR4	124.5.7
400GBASE-FR4 and 400GBASE-LR4-6	151.5.7

45.2.1.8.2 PMD transmit disable 4 through 14 (1.9.5 through 1.9.14)

Bits 1.9.5 through 1.9.14 are defined similarly to bit 1.9.15 for lanes 4 through 13, respectively.

45.2.1.8.3 PMD transmit disable 3 (1.9.4)

When bit 1.9.4 is set to a one, the PMD shall disable output on lane 3 of the transmit path. When bit 1.9.4 is set to a zero, the PMD shall enable output on lane 3 of the transmit path.

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The default value for bit 1.9.4 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.4 PMD transmit disable 2 (1.9.3)

When bit 1.9.3 is set to a one, the PMD shall disable output on lane 2 of the transmit path. When bit 1.9.3 is set to a zero, the PMD shall enable output on lane 2 of the transmit path.

The default value for bit 1.9.3 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.5 PMD transmit disable 1 (1.9.2)

When bit 1.9.2 is set to a one, the PMD shall disable output on lane 1 of the transmit path. When bit 1.9.2 is set to a zero, the PMD shall enable output on lane 1 of the transmit path.

The default value for bit 1.9.2 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.6 PMD transmit disable 0 (1.9.1)

When bit 1.9.1 is set to a one, the PMD shall disable output on lane 0 of the transmit path. When bit 1.9.1 is set to a zero, the PMD shall enable output on lane 0 of the transmit path.

The default value for bit 1.9.1 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.7 Global PMD transmit disable (1.9.0)

When bit 1.9.0 is set to a one, the PMD shall disable output on the transmit path. When bit 1.9.0 is set to a zero, the PMD shall enable output on the transmit path.

For single wavelength PMD types, transmission will be disabled when this bit is set to one. When this bit is set to zero, transmission is enabled.

For multiple wavelength or lane PMD types, transmission will be disabled on all lanes when this bit is set to one. When this bit is set to zero, the lanes are individually controlled by their corresponding transmit disable bits 1.9.4:1.

The default value for bit 1.9.0 is zero.

45.2.1.9 PMD receive signal detect register (Register 1.10)

The assignment of bits in the PMD receive signal detect register is shown in Table 45–13. The PMD receive signal detect register is mandatory. PMD types that use only a single lane indicate the status of the receive signal detect using bit 1.10.0 and return a value of zero for bits 1.10.15:1. PMD types that use multiple

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wavelengths or lanes indicate the status of each lane in bits 1.10.15:1 and the logical AND of those bits in bit 1.10.0.

NOTE—This register is extended by the PMD receive signal detect extension register (see 45.2.1.26).

Table 45–13—PMD receive signal detect register bit definitions

Bit(s)	Name	Description	R/W[a]
1.10.15	PMD receive signal detect 14	1 = Signal detected on receive lane 14 0 = Signal not detected on receive lane 14	RO
1.10.14	PMD receive signal detect 13	1 = Signal detected on receive lane 13 0 = Signal not detected on receive lane 13	RO
1.10.13	PMD receive signal detect 12	1 = Signal detected on receive lane 12 0 = Signal not detected on receive lane 12	RO
1.10.12	PMD receive signal detect 11	1 = Signal detected on receive lane 11 0 = Signal not detected on receive lane 11	RO
1.10.11	PMD receive signal detect 10	1 = Signal detected on receive lane 10 0 = Signal not detected on receive lane 10	RO
1.10.10	PMD receive signal detect 9	1 = Signal detected on receive lane 9 0 = Signal not detected on receive lane 9	RO
1.10.9	PMD receive signal detect 8	1 = Signal detected on receive lane 8 0 = Signal not detected on receive lane 8	RO
1.10.8	PMD receive signal detect 7	1 = Signal detected on receive lane 7 0 = Signal not detected on receive lane 7	RO
1.10.7	PMD receive signal detect 6	1 = Signal detected on receive lane 6 0 = Signal not detected on receive lane 6	RO
1.10.6	PMD receive signal detect 5	1 = Signal detected on receive lane 5 0 = Signal not detected on receive lane 5	RO
1.10.5	PMD receive signal detect 4	1 = Signal detected on receive lane 4 0 = Signal not detected on receive lane 4	RO
1.10.4	PMD receive signal detect 3	1 = Signal detected on receive lane 3 0 = Signal not detected on receive lane 3	RO
1.10.3	PMD receive signal detect 2	1 = Signal detected on receive lane 2 0 = Signal not detected on receive lane 2	RO
1.10.2	PMD receive signal detect 1	1 = Signal detected on receive lane 1 0 = Signal not detected on receive lane 1	RO
1.10.1	PMD receive signal detect 0	1 = Signal detected on receive lane 0 0 = Signal not detected on receive lane 0	RO
1.10.0	Global PMD receive signal detect	1 = Signal detected on receive 0 = Signal not detected on receive	RO

[a]RO = Read only

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45.2.1.9.1 PMD receive signal detect 14 (1.10.15)

When bit 1.10.15 is read as a one, a signal has been detected on lane 14 of the PMD receive path. When bit 1.10.15 is read as a zero, a signal has not been detected on lane 14 of the PMD receive path.

45.2.1.9.2 PMD receive signal detect 4 through 13 (1.10.5 through 1.10.14)

Bits 1.10.5 through 1.10.14 are defined similarly to bit 1.10.15 for lanes 4 through 13, respectively.

45.2.1.9.3 PMD receive signal detect 3 (1.10.4)

When bit 1.10.4 is read as a one, a signal has been detected on lane 3 of the PMD receive path. When bit 1.10.4 is read as a zero, a signal has not been detected on lane 3 of the PMD receive path.

45.2.1.9.4 PMD receive signal detect 2 (1.10.3)

When bit 1.10.3 is read as a one, a signal has been detected on lane 2 of the PMD receive path. When bit 1.10.3 is read as a zero, a signal has not been detected on lane 2 of the PMD receive path.

45.2.1.9.5 PMD receive signal detect 1 (1.10.2)

When bit 1.10.2 is read as a one, a signal has been detected on lane 1 of the PMD receive path. When bit 1.10.2 is read as a zero, a signal has not been detected on lane 1 of the PMD receive path.

45.2.1.9.6 PMD receive signal detect 0 (1.10.1)

When bit 1.10.1 is read as a one, a signal has been detected on lane 0 of the PMD receive path. When bit 1.10.1 is read as a zero, a signal has not been detected on lane 0 of the PMD receive path.

45.2.1.9.7 Global PMD receive signal detect (1.10.0)

When bit 1.10.0 is read as a one, a signal has been detected on all the PMD receive paths. When bit 1.10.0 is read as a zero, a signal has not been detected on at least one of the PMD receive paths.

Single wavelength PMD types indicate the status of their receive path signal using this bit.

Multiple wavelength or multiple lane PMD types indicate the global status of the lane-by-lane signal detect indications using this bit. This bit is read as a one when all the lane signal detect indications are one; otherwise, this bit is read as a zero.

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45.2.1.10 PMA/PMD extended ability register (Register 1.11)

The assignment of bits in the PMA/PMD extended ability register is shown in Table 45–14. All of the bits in the PMA/PMD extended ability register are read only; a write to the PMA/PMD extended ability register shall have no effect.

Table 45–14—PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.11.15	BASE-H extended abilities	1 = PMA/PMD has BASE-H extended abilities listed in register 1.22 0 = PMA/PMD does not have BASE-H extended abilities	RO
1.11.14	2.5G/5G extended abilities	1 = PMA/PMD has 2.5G/5G extended abilities listed in register 1.21 0 = PMA/PMD does not have 2.5G/5G extended abilities	RO
1.11.13	200G/400G extended abilities	1 = PMA/PMD has 200G/400G extended abilities listed in register 1.23 or register 1.24 0 = PMA/PMD does not have 200G/400G extended abilities	RO
1.11.12	25G extended abilities	1 = PMA/PMD has 25G extended abilities listed in register 1.19 0 = PMA/PMD does not have 25G extended abilities	RO
1.11.11	BASE-T1 extended abilities	1 = PMA/PMD has BASE-T1 extended abilities listed in register 1.18 0 = PMA/PMD does not have BASE-T1 extended abilities	RO
1.11.10	40G/100G extended abilities	1 = PMA/PMD has 40G/100G extended abilities listed in register 1.13 0 = PMA/PMD does not have 40G/100G extended abilities	RO
1.11.9	P2MP ability	1 = PMA/PMD has P2MP abilities listed in register 1.12 0 = PMA/PMD does not have P2MP abilities	RO
1.11.8	10BASE-T ability	1 = PMA/PMD is able to perform 10BASE-T 0 = PMA/PMD is not able to perform 10BASE-T	RO
1.11.7	100BASE-TX ability	1 = PMA/PMD is able to perform 100BASE-TX 0 = PMA/PMD is not able to perform 100BASE-TX	RO
1.11.6	1000BASE-KX ability	1 = PMA/PMD is able to perform 1000BASE-KX 0 = PMA/PMD is not able to perform 1000BASE-KX	RO
1.11.5	1000BASE-T ability	1 = PMA/PMD is able to perform 1000BASE-T 0 = PMA/PMD is not able to perform 1000BASE-T	RO
1.11.4	10GBASE-KR ability	1 = PMA/PMD is able to perform 10GBASE-KR 0 = PMA/PMD is not able to perform 10GBASE-KR	RO
1.11.3	10GBASE-KX4 ability	1 = PMA/PMD is able to perform 10GBASE-KX4 0 = PMA/PMD is not able to perform 10GBASE-KX4	RO

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Table 45–14—PMA/PMD Extended Ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.11.2	10GBASE-T ability	1 = PMA/PMD is able to perform 10GBASE-T 0 = PMA/PMD is not able to perform 10GBASE-T	RO
1.11.1	10GBASE-LRM ability	1 = PMA/PMD is able to perform 10GBASE-LRM 0 = PMA/PMD is not able to perform 10GBASE-LRM	RO
1.11.0	10GBASE-CX4 ability	1 = PMA/PMD is able to perform 10GBASE-CX4 0 = PMA/PMD is not able to perform 10GBASE-CX4	RO

[a]RO = Read only

45.2.1.10.1 BASE-H extended abilities (1.11.15)

When read as one, bit 1.11.15 indicates that the PMA/PMD has BASE-H extended abilities listed in register 1.22. When read as zero, bit 1.11.15 indicates that the PMA/PMD does not have BASE-H extended abilities.

45.2.1.10.2 2.5G/5G extended abilities (1.11.14)

When read as a one, bit 1.11.14 indicates that the PMA/PMD has 2.5G/5G extended abilities listed in register 1.21. When read as a zero, bit 1.11.14 indicates that the PMA/PMD does not have 2.5G/5G extended abilities.

45.2.1.10.3 200G/400G extended abilities (1.11.13)

When read as a one, bit 1.11.13 indicates that the PMA/PMD has 200G extended abilities listed in register 1.23 or 400G extended abilities listed in register 1.24. When read as a zero, bit 1.11.13 indicates that the PMA/PMD does not have 200G or 400G extended abilities.

45.2.1.10.4 25G extended abilities (1.11.12)

When read as a one, bit 1.11.12 indicates that the PMA/PMD has 25G extended abilities listed in register 1.19. When read as a zero, bit 1.11.12 indicates that the PMA/PMD does not have 25G extended abilities.

45.2.1.10.5 BASE-T1 extended abilities (1.11.11)

When read as a one, bit 1.11.11 indicates that the PMA/PMD has BASE-T1 extended abilities listed in register 1.18. When read as a zero, bit 1.11.11 indicates that the PMA/PMD does not have BASE-T1 extended abilities.

45.2.1.10.6 40G/100G extended abilities (1.11.10)

When read as a one, bit 1.11.10 indicates that the PMA/PMD has 40G/100G extended abilities listed in register 1.13. When read as a zero, bit 1.11.10 indicates that the PMA/PMD does not have 40G/100G extended abilities.

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45.2.1.10.7 P2MP ability (1.11.9)

When read as a one, bit 1.11.9 indicates that the PMA/PMD has P2MP abilities listed in register 1.12. When read as a zero, bit 1.11.9 indicates that the PMA/PMD does not have P2MP abilities.

45.2.1.10.8 10BASE-T ability (1.11.8)

When read as a one, bit 1.11.8 indicates that the PMA/PMD is able to operate as a 10BASE-T PMA/PMD type. When read as a zero, bit 1.11.8 indicates that the PMA/PMD is not able to operate as a 10BASE-T PMA/PMD type.

45.2.1.10.9 100BASE-TX ability (1.11.7)

When read as a one, bit 1.11.7 indicates that the PMA/PMD is able to operate as a 100BASE-TX PMA/PMD type. When read as a zero, bit 1.11.7 indicates that the PMA/PMD is not able to operate as a 100BASE-TX PMA/PMD type.

45.2.1.10.10 1000BASE-KX ability (1.11.6)

When read as a one, bit 1.11.6 indicates that the PMA/PMD is able to operate as 1000BASE-KX. When read as a zero, bit 1.11.6 indicates that the PMA/PMD is not able to operate as 1000BASE-KX.

45.2.1.10.11 1000BASE-T ability (1.11.5)

When read as a one, bit 1.11.5 indicates that the PMA/PMD is able to operate as a 1000BASE-T PMA/PMD type. When read as a zero, bit 1.11.5 indicates that the PMA/PMD is not able to operate as a 1000BASE-T PMA/PMD type.

45.2.1.10.12 10GBASE-KR ability (1.11.4)

When read as a one, bit 1.11.4 indicates that the PMA/PMD is able to operate as 10GBASE-KR. When read as a zero, bit 1.11.4 indicates that the PMA/PMD is not able to operate as 10GBASE-KR.

45.2.1.10.13 10GBASE-KX4 ability (1.11.3)

When read as a one, bit 1.11.3 indicates that the PMA/PMD is able to operate as 10GBASE-KX4. When read as a zero, bit 1.11.3 indicates that the PMA/PMD is not able to operate as 10GBASE-KX4.

45.2.1.10.14 10GBASE-T ability (1.11.2)

When read as a one, bit 1.11.2 indicates that the PMA/PMD is able to operate as a 10GBASE-T PMA/PMD type. When read as a zero, bit 1.11.2 indicates that the PMA/PMD is not able to operate as a 10GBASE-T PMA/PMD type.

45.2.1.10.15 10GBASE-LRM ability (1.11.1)

When read as a one, bit 1.11.1 indicates that the PMA/PMD is able to operate as 10GBASE-LRM. When read as a zero, bit 1.11.1 indicates that the PMA/PMD is not able to operate as 10GBASE-LRM.

45.2.1.10.16 10GBASE-CX4 ability (1.11.0)

When read as a one, bit 1.11.0 indicates that the PMA/PMD is able to operate as a 10GBASE-CX4 PMA/PMD type. When read as a zero, bit 1.11.0 indicates that the PMA/PMD is not able to operate as a 10GBASE-CX4 PMA/PMD type.

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45.2.1.11 10G-EPON PMA/PMD ability register (Register 1.12)

The assignment of bits in the 10G-EPON PMA/PMD ability register is shown in Table 45–15. All of the bits in the 10G-EPON PMA/PMD ability register are read only; a write to the 10G-EPON PMA/PMD ability register shall have no effect.

Table 45–15—10G-EPON PMA/PMD ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.12.15	Reserved	Value always 0	RO
1.12.14	10GBASE-PR-D4 ability	1 = PMA/PMD is able to perform 10GBASE-PR-D4 0 = PMA/PMD is not able to perform 10GBASE-PR-D4	RO
1.12.13	10GBASE-PR-U4 ability	1 = PMA/PMD is able to perform 10GBASE-PR-U4 0 = PMA/PMD is not able to perform 10GBASE-PR-U4	RO
1.12.12	10/1GBASE-PRX-D4 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-D4 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-D4	RO
1.12.11	10/1GBASE-PRX-U4 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-U4 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-U4	RO
1.12.10	10/1GBASE-PRX-D1 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-D1 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-D1	RO
1.12.9	10/1GBASE-PRX-D2 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-D2 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-D2	RO
1.12.8	10/1GBASE-PRX-D3 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-D3 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-D3	RO
1.12.7	10GBASE-PR-D1 ability	1 = PMA/PMD is able to perform 10GBASE-PR-D1 0 = PMA/PMD is not able to perform 10GBASE-PR-D1	RO
1.12.6	10GBASE-PR-D2 ability	1 = PMA/PMD is able to perform 10GBASE-PR-D2 0 = PMA/PMD is not able to perform 10GBASE-PR-D2	RO
1.12.5	10GBASE-PR-D3 ability	1 = PMA/PMD is able to perform 10GBASE-PR-D3 0 = PMA/PMD is not able to perform 10GBASE-PR-D3	RO
1.12.4	10/1GBASE-PRX-U1 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-U1 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-U1	RO
1.12.3	10/1GBASE-PRX-U2 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-U2 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-U2	RO
1.12.2	10/1GBASE-PRX-U3 ability	1 = PMA/PMD is able to perform 10/1GBASE-PRX-U3 0 = PMA/PMD is not able to perform 10/1GBASE-PRX-U3	RO
1.12.1	10GBASE-PR-U1 ability	1 = PMA/PMD is able to perform 10GBASE-PR-U1 0 = PMA/PMD is not able to perform 10GBASE-PR-U1	RO
1.12.0	10GBASE-PR-U3 ability	1 = PMA/PMD is able to perform 10GBASE-PR-U3 0 = PMA/PMD is not able to perform 10GBASE-PR-U3	RO

[a]RO = Read only

45.2.1.11.1 10GBASE-PR-D4 ability (1.12.14)

When read as a one, bit 1.12.14 indicates that the PMA/PMD is able to operate as a 10GBASE-PR-D4 PMA/PMD type. When read as a zero, bit 1.12.14 indicates that the PMA/PMD is not able to operate as a 10GBASE-PR-D4 PMA/PMD type.

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45.2.1.11.2 10GBASE-PR-U4 ability (1.12.13)

When read as a one, bit 1.12.13 indicates that the PMA/PMD is able to operate as a 10GBASE-PR-U4 PMA/PMD type. When read as a zero, bit 1.12.13 indicates that the PMA/PMD is not able to operate as a 10GBASE-PR-U4 PMA/PMD type.

45.2.1.11.3 10/1GBASE-PRX-D4 ability (1.12.12)

When read as a one, bit 1.12.12 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-D4 PMA/PMD type. When read as a zero, bit 1.12.12 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-D4 PMA/PMD type.

45.2.1.11.4 10/1GBASE-PRX-U4 ability (1.12.11)

When read as a one, bit 1.12.11 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-U4 PMA/PMD type. When read as a zero, bit 1.12.11 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-U4 PMA/PMD type.

45.2.1.11.5 10/1GBASE-PRX-D1 ability (1.12.10)

When read as a one, bit 1.12.10 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-D1 PMA/PMD type. When read as a zero, bit 1.12.10 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-D1 PMA/PMD type.

45.2.1.11.6 10/1GBASE-PRX-D2 ability (1.12.9)

When read as a one, bit 1.12.9 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-D2 PMA/PMD type. When read as a zero, bit 1.12.9 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-D2 PMA/PMD type.

45.2.1.11.7 10/1GBASE-PRX-D3 ability (1.12.8)

When read as a one, bit 1.12.8 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-D3 PMA/PMD type. When read as a zero, bit 1.12.8 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-D3 PMA/PMD type.

45.2.1.11.8 10GBASE-PR-D1 ability (1.12.7)

When read as a one, bit 1.12.7 indicates that the PMA/PMD is able to operate as a 10GBASE-PR-D1 PMA/PMD type. When read as a zero, bit 1.12.7 indicates that the PMA/PMD is not able to operate as a 10GBASE-PR-D1 PMA/PMD type.

45.2.1.11.9 10GBASE-PR-D2 ability (1.12.6)

When read as a one, bit 1.12.6 indicates that the PMA/PMD is able to operate as a 10GBASE-PR-D2 PMA/PMD type. When read as a zero, bit 1.12.6 indicates that the PMA/PMD is not able to operate as a 10GBASE-PR-D2 PMA/PMD type.

45.2.1.11.10 10GBASE-PR-D3 ability (1.12.5)

When read as a one, bit 1.12.5 indicates that the PMA/PMD is able to operate as a 10GBASE-PR-D3 PMA/PMD type. When read as a zero, bit 1.12.5 indicates that the PMA/PMD is not able to operate as a 10GBASE-PR-D3 PMA/PMD type.

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45.2.1.11.11 10/1GBASE-PRX-U1 ability (1.12.4)

When read as a one, bit 1.12.4 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-U1 PMA/PMD type. When read as a zero, bit 1.12.4 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-U1 PMA/PMD type.

45.2.1.11.12 10/1GBASE-PRX-U2 ability (1.12.3)

When read as a one, bit 1.12.3 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-U2 PMA/PMD type. When read as a zero, bit 1.12.3 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-U2 PMA/PMD type.

45.2.1.11.13 10/1GBASE-PRX-U3 ability (1.12.2)

When read as a one, bit 1.12.2 indicates that the PMA/PMD is able to operate as a 10/1GBASE-PRX-U3 PMA/PMD type. When read as a zero, bit 1.12.2 indicates that the PMA/PMD is not able to operate as a 10/1GBASE-PRX-U3 PMA/PMD type.

45.2.1.11.14 10GBASE-PR-U1 ability (1.12.1)

When read as a one, bit 1.12.1 indicates that the PMA/PMD is able to operate as a 10GBASE-PR-U1 PMA/PMD type. When read as a zero, bit 1.12.1 indicates that the PMA/PMD is not able to operate as a 10GBASE-PR-U1 PMA/PMD type.

45.2.1.11.15 10GBASE-PR-U3 ability (1.12.0)

When read as a one, bit 1.12.0 indicates that the PMA/PMD is able to operate as a 10GBASE-PR-U3 PMA/PMD type. When read as a zero, bit 1.12.0 indicates that the PMA/PMD is not able to operate as a 10GBASE-PR-U3 PMA/PMD type.

45.2.1.12 40G/100G PMA/PMD extended ability register (Register 1.13)

The assignment of bits in the 40G/100G PMA/PMD extended ability register is shown in Table 45–16. All of the bits in the PMA/PMD extended ability register are read only; a write to the PMA/PMD extended ability register shall have no effect.

Table 45–16—40G/100G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.13.15	PMA remote loopback ability	1 = PMA has the ability to perform a remote loopback function 0 = PMA does not have the ability to perform a remote loopback function	RO
1.13.14	100GBASE-CR4 ability	1 = PMA/PMD is able to perform 100GBASE-CR4 0 = PMA/PMD is not able to perform 100GBASE-CR4	RO
1.13.13	100GBASE-KR4 ability	1 = PMA/PMD is able to perform 100GBASE-KR4 0 = PMA/PMD is not able to perform 100GBASE-KR4	RO
1.13.12	100GBASE-KP4 ability	1 = PMA/PMD is able to perform 100GBASE-KP4 0 = PMA/PMD is not able to perform 100GBASE-KP4	RO
1.13.11	100GBASE-ER4 ability	1 = PMA/PMD is able to perform 100GBASE-ER4 0 = PMA/PMD is not able to perform 100GBASE-ER4	RO

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Table 45–16—40G/100G PMA/PMD extended ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.13.10	100GBASE-LR4 ability	1 = PMA/PMD is able to perform 100GBASE-LR4 0 = PMA/PMD is not able to perform 100GBASE-LR4	RO
1.13.9	100GBASE-SR10 ability	1 = PMA/PMD is able to perform 100GBASE-SR10 0 = PMA/PMD is not able to perform 100GBASE-SR10	RO
1.13.8	100GBASE-CR10 ability	1 = PMA/PMD is able to perform 100GBASE-CR10 0 = PMA/PMD is not able to perform 100GBASE-CR10	RO
1.13.7	100GBASE-SR4 ability	1 = PMA/PMD is able to perform 100GBASE-SR4 0 = PMA/PMD is not able to perform 100GBASE-SR4	RO
1.13.6	40GBASE-T ability	1 = PMA/PMD is able to perform 40GBASE-T 0 = PMA/PMD is not able to perform 40GBASE-T	RO
1.13.5	40GBASE-ER4 ability	1 = PMA/PMD is able to perform 40GBASE-ER4 0 = PMA/PMD is not able to perform 40GBASE-ER4	RO
1.13.4	40GBASE-FR ability	1 = PMA/PMD is able to perform 40GBASE-FR 0 = PMA/PMD is not able to perform 40GBASE-FR	RO
1.13.3	40GBASE-LR4 ability	1 = PMA/PMD is able to perform 40GBASE-LR4 0 = PMA/PMD is not able to perform 40GBASE-LR4	RO
1.13.2	40GBASE-SR4 ability	1 = PMA/PMD is able to perform 40GBASE-SR4 0 = PMA/PMD is not able to perform 40GBASE-SR4	RO
1.13.1	40GBASE-CR4 ability	1 = PMA/PMD is able to perform 40GBASE-CR4 0 = PMA/PMD is not able to perform 40GBASE-CR4	RO
1.13.0	40GBASE-KR4 ability	1 = PMA/PMD is able to perform 40GBASE-KR4 0 = PMA/PMD is not able to perform 40GBASE-KR4	RO

[a]RO = Read only

45.2.1.12.1 PMA remote loopback ability (1.13.15)

When read as a one, bit 1.13.15 indicates that the PMA is able to perform the remote loopback function. When read as a zero, bit 1.13.15 indicates that the PMA is not able to perform the remote loopback function. If a PMA is able to perform the remote loopback function, then it is controlled using the PMA remote loopback bit 1.0.1 (see 45.2.1.1.4).

45.2.1.12.2 100GBASE-CR4 ability (1.13.14)

When read as a one, bit 1.13.14 indicates that the PMA/PMD is able to operate as a 100GBASE-CR4 PMA/PMD type. When read as a zero, bit 1.13.14 indicates that the PMA/PMD is not able to operate as a 100GBASE-CR4 PMA/PMD type.

45.2.1.12.3 100GBASE-KR4 ability (1.13.13)

When read as a one, bit 1.13.13 indicates that the PMA/PMD is able to operate as a 100GBASE-KR4 PMA/PMD type. When read as a zero, bit 1.13.13 indicates that the PMA/PMD is not able to operate as a 100GBASE-KR4 PMA/PMD type.

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45.2.1.12.4 100GBASE-KP4 ability (1.13.12)

When read as a one, bit 1.13.12 indicates that the PMA/PMD is able to operate as a 100GBASE-KP4 PMA/PMD type. When read as a zero, bit 1.13.12 indicates that the PMA/PMD is not able to operate as a 100GBASE-KP4 PMA/PMD type.

45.2.1.12.5 100GBASE-ER4 ability (1.13.11)

When read as a one, bit 1.13.11 indicates that the PMA/PMD is able to operate as a 100GBASE-ER4 PMA/PMD type. When read as a zero, bit 1.13.11 indicates that the PMA/PMD is not able to operate as a 100GBASE-ER4 PMA/PMD type.

45.2.1.12.6 100GBASE-LR4 ability (1.13.10)

When read as a one, bit 1.13.10 indicates that the PMA/PMD is able to operate as a 100GBASE-LR4 PMA/PMD type. When read as a zero, bit 1.13.10 indicates that the PMA/PMD is not able to operate as a 100GBASE-LR4 PMA/PMD type.

45.2.1.12.7 100GBASE-SR10 ability (1.13.9)

When read as a one, bit 1.13.9 indicates that the PMA/PMD is able to operate as a 100GBASE-SR10 PMA/PMD type. When read as a zero, bit 1.13.9 indicates that the PMA/PMD is not able to operate as a 100GBASE-SR10 PMA/PMD type.

45.2.1.12.8 100GBASE-CR10 ability (1.13.8)

When read as a one, bit 1.13.8 indicates that the PMA/PMD is able to operate as a 100GBASE-CR10 PMA/PMD type. When read as a zero, bit 1.13.8 indicates that the PMA/PMD is not able to operate as a 100GBASE-CR10 PMA/PMD type.

45.2.1.12.9 100GBASE-SR4 ability (1.13.7)

When read as a one, bit 1.13.7 indicates that the PMA/PMD is able to operate as a 100GBASE-SR4 PMA/PMD type. When read as a zero, bit 1.13.7 indicates that the PMA/PMD is not able to operate as a 100GBASE-SR4 PMA/PMD type.

45.2.1.12.10 40GBASE-T ability (1.13.6)

When read as a one, bit 1.13.6 indicates that the PMA/PMD is able to operate as a 40GBASE-T PMA type. When read as a zero, bit 1.13.6 indicates that the PMA/PMD is not able to operate as a 40GBASE-T PMA type.

45.2.1.12.11 40GBASE-ER4 ability (1.13.5)

When read as a one, bit 1.13.5 indicates that the PMA/PMD is able to operate as a 40GBASE-ER4 PMA/PMD type. When read as a zero, bit 1.13.5 indicates that the PMA/PMD is not able to operate as a 40GBASE-ER4 PMA/PMD type.

45.2.1.12.12 40GBASE-FR ability (1.13.4)

When read as a one, bit 1.13.4 indicates that the PMA/PMD is able to operate as a 40GBASE-FR PMA/PMD type. When read as a zero, bit 1.13.4 indicates that the PMA/PMD is not able to operate as a 40GBASE-FR PMA/PMD type.

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45.2.1.12.13 40GBASE-LR4 ability (1.13.3)

When read as a one, bit 1.13.3 indicates that the PMA/PMD is able to operate as a 40GBASE-LR4 PMA/PMD type. When read as a zero, bit 1.13.3 indicates that the PMA/PMD is not able to operate as a 40GBASE-LR4 PMA/PMD type.

45.2.1.12.14 40GBASE-SR4 ability (1.13.2)

When read as a one, bit 1.13.2 indicates that the PMA/PMD is able to operate as a 40GBASE-SR4 PMA/PMD type. When read as a zero, bit 1.13.2 indicates that the PMA/PMD is not able to operate as a 40GBASE-SR4 PMA/PMD type.

45.2.1.12.15 40GBASE-CR4 ability (1.13.1)

When read as a one, bit 1.13.1 indicates that the PMA/PMD is able to operate as a 40GBASE-CR4 PMA/PMD type. When read as a zero, bit 1.13.1 indicates that the PMA/PMD is not able to operate as a 40GBASE-CR4 PMA/PMD type.

45.2.1.12.16 40GBASE-KR4 ability (1.13.0)

When read as a one, bit 1.13.0 indicates that the PMA/PMD is able to operate as a 40GBASE-KR4 PMA/PMD type. When read as a zero, bit 1.13.0 indicates that the PMA/PMD is not able to operate as a 40GBASE-KR4 PMA/PMD type.

45.2.1.13 PMA/PMD package identifier (Registers 1.14 and 1.15)

Registers 1.14 and 1.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PMA/PMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PMA/PMD may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the package identifier is specified in 22.2.4.3.1.

45.2.1.14 EEE capability (Register 1.16)

This register is used to indicate the capability of the PMA/PMD to support EEE functions for each PHY type. The assignment of bits in the EEE capability register is shown in Table 45–17.

Table 45–17—EEE capability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.16.15:12	Reserved	Value always 0	RO
1.16.11	100GBASE-CR4 deep sleep	1 = EEE deep sleep is supported for 100GBASE-CR4 0 = EEE deep sleep is not supported for 100GBASE-CR4	RO
1.16.10	100GBASE-KR4 deep sleep	1 = EEE deep sleep is supported for 100GBASE-KR4 0 = EEE deep sleep is not supported for 100GBASE-KR4	RO

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Table 45–17—EEE capability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.16.9	100GBASE-KP4 deep sleep	1 = EEE deep sleep is supported for 100GBASE-KP4 0 = EEE deep sleep is not supported for 100GBASE-KP4	RO
1.16.8	100GBASE-CR10 deep sleep	1 = EEE deep sleep is supported for 100GBASE-CR10 0 = EEE deep sleep is not supported for 100GBASE-CR10	RO
1.16.7:3	Reserved	Value always 0	RO
1.16.2	25GBASE-R deep sleep	1 = EEE deep sleep is supported for 25GBASE-R 0 = EEE deep sleep is not supported for 25GBASE-R	RO
1.16.1	40GBASE-CR4 deep sleep	1 = EEE deep sleep is supported for 40GBASE-CR4 0 = EEE deep sleep is not supported for 40GBASE-CR4	RO
1.16.0	40GBASE-KR4 deep sleep	1 = EEE deep sleep is supported for 40GBASE-KR4 0 = EEE deep sleep is not supported for 40GBASE-KR4	RO

[a] RO = Read only

45.2.1.14.1 100GBASE-CR4 EEE deep sleep supported (1.16.11)

If the device supports EEE deep sleep operation for 100GBASE-CR4 as defined in 92.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.1.14.2 100GBASE-KR4 EEE deep sleep supported (1.16.10)

If the device supports EEE deep sleep operation for 100GBASE-KR4 as defined in 93.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.1.14.3 100GBASE-KP4 EEE deep sleep supported (1.16.9)

If the device supports EEE deep sleep operation for 100GBASE-KP4 as defined in 94.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.1.14.4 100GBASE-CR10 EEE deep sleep supported (1.16.8)

If the device supports EEE deep sleep operation for 100GBASE-CR10 as defined in 85.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.1.14.5 25GBASE-R deep sleep (1.16.2)

If the device supports EEE deep sleep operation for 25GBASE-R, bit 1.16.2 shall be set to a one; otherwise this bit is set to a zero.

45.2.1.14.6 40GBASE-CR4 EEE deep sleep supported (1.16.1)

If the device supports EEE deep sleep operation for 40GBASE-CR4 as defined in 85.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

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45.2.1.14.7 40GBASE-KR4 EEE deep sleep supported (1.16.0)

If the device supports EEE deep sleep operation for 40GBASE-KR4 as defined in 84.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.1.15 EPoC PMA/PMD ability register (Register 1.17)

The assignment of bits in the EPoC PMA/PMD ability register is shown in Table 45–18. All of the bits in the EPoC PMA/PMD ability register are read only; a write to the EPoC PMA/PMD ability register shall have no effect.

Table 45–18—EPoC PMA/PMD ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.17.15:2	Reserved	Value always 0	RO
1.17.1	10GPASS-XR-D ability	1 = PMA/PMD is able to perform 10GPASS-XR-D 0 = PMA/PMD is not able to perform 10GPASS-XR-D	RO
1.17.0	10GPASS-XR-U ability	1 = PMA/PMD is able to perform 10GPASS-XR-U 0 = PMA/PMD is not able to perform 10GPASS-XR-U	RO

[a]RO = Read only

45.2.1.15.1 10GPASS-XR-D ability (1.17.1)

When read as one, bit 1.17.1 indicates that the PMA/PMD is able to operate as a 10GPASS-XR-D PMA/PMD type. When read as zero, bit 1.17.1 indicates that the PMA/PMD is not able to operate as a 10GPASS-XR-D PMA/PMD type.

45.2.1.15.2 10GPASS-XR-U ability (1.17.0)

When read as one, bit 1.17.0 indicates that the PMA/PMD is able to operate as a 10GPASS-XR-U PMA/PMD type. When read as zero, bit 1.17.0 indicates that the PMA/PMD is not able to operate as a 10GPASS-XR-U PMA/PMD type.

45.2.1.16 BASE-T1 PMA/PMD extended ability register (1.18)

The assignment of bits in the BASE-T1 PMA/PMD extended ability register is shown in Table 45–19. All of the bits in the PMA/PMD extended ability register are read only; a write to the PMA/PMD extended ability register shall have no effect.

45.2.1.16.1 10GBASE-T1 ability (1.18.6)

When read as a one, bit 1.18.6 indicates that the PMA/PMD is able to operate as a 10GBASE-T1 PMA type. When read as a zero, bit 1.18.6 indicates that the PMA/PMD is not able to operate as a 10GBASE-T1 PMA type.

45.2.1.16.2 5GBASE-T1 ability (1.18.5)

When read as a one, bit 1.18.5 indicates that the PMA/PMD is able to operate as a 5GBASE-T1 PMA type. When read as a zero, bit 1.18.5 indicates that the PMA/PMD is not able to operate as a 5GBASE-T1 PMA type.

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Table 45–19—BASE-T1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.18.15:7	Reserved	Value always 0	RO
1.18.6	10GBASE-T1 ability	1 = PMA/PMD is able to perform 10GBASE-T1 0 = PMA/PMD is not able to perform 10GBASE-T1	RO
1.18.5	5GBASE-T1 ability	1 = PMA/PMD is able to perform 5GBASE-T1 0 = PMA/PMD is not able to perform 5GBASE-T1	RO
1.18.4	2.5GBASE-T1 ability	1 = PMA/PMD is able to perform 2.5GBASE-T1 0 = PMA/PMD is not able to perform 2.5GBASE-T1	RO
1.18.3	10BASE-T1S ability	1 = PMA/PMD is able to perform 10BASE-T1S 0 = PMA/PMD is not able to perform 10BASE-T1S	RO
1.18.2	10BASE-T1L ability	1 = PMA/PMD is able to perform 10BASE-T1L 0 = PMA/PMD is not able to perform 10BASE-T1L	RO
1.18.1	1000BASE-T1 ability	1 = PMA/PMD is able to perform 1000BASE-T1 0 = PMA/PMD is not able to perform 1000BASE-T1	RO
1.18.0	100BASE-T1 ability	1 = PMA/PMD is able to perform 100BASE-T1 0 = PMA/PMD is not able to perform 100BASE-T1	RO

[a]RO = Read only

45.2.1.16.3 2.5GBASE-T1 ability (1.18.4)

When read as a one, bit 1.18.4 indicates that the PMA/PMD is able to operate as a 2.5GBASE-T1 PMA type. When read as a zero, bit 1.18.4 indicates that the PMA/PMD is not able to operate as a 2.5GBASE-T1 PMA type.

45.2.1.16.4 10BASE-T1S ability (1.18.3)

When read as a one, bit 1.18.3 indicates that the PMA/PMD is able to operate as a 10BASE-T1S PMA type. When read as a zero, bit 1.18.3 indicates that the PMA/PMD is not able to operate as a 10BASE-T1S PMA type.

45.2.1.16.5 10BASE-T1L ability (1.18.2)

When read as a one, bit 1.18.2 indicates that the PMA/PMD is able to operate as a 10BASE-T1L PMA type. When read as a zero, bit 1.18.2 indicates that the PMA/PMD is not able to operate as a 10BASE-T1L PMA type.

45.2.1.16.6 1000BASE-T1 ability (1.18.1)

When read as a one, bit 1.18.1 indicates that the PMA/PMD is able to operate as a 1000BASE-T1 PMA type. When read as a zero, bit 1.18.1 indicates that the PMA/PMD is not able to operate as a 1000BASE-T1 PMA type.

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45.2.1.16.7 100BASE-T1 ability (1.18.0)

When read as a one, bit 1.18.0 indicates that the PMA/PMD is able to operate as a 100BASE-T1 PMA type. When read as a zero, bit 1.18.0 indicates that the PMA/PMD is not able to operate as a 100BASE-T1 PMA type.

45.2.1.17 25G PMA/PMD extended ability register (Register 1.19)

The assignment of bits in the 25G PMA/PMD extended ability register is shown in Table 45–20.

Table 45–20—25G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.19.15:8	Reserved	Value always 0	RO
1.19.7	25GBASE-ER ability	1 = PMA/PMD is able to perform 25GBASE-ER 0 = PMA/PMD is not able to perform 25GBASE-ER	RO
1.19.6	25GBASE-LR ability	1 = PMA/PMD is able to perform 25GBASE-LR 0 = PMA/PMD is not able to perform 25GBASE-LR	RO
1.19.5	25GBASE-T ability	1 = PMA/PMD is able to perform 25GBASE-T 0 = PMA/PMD is not able to perform 25GBASE-T	RO
1.19.4	25GBASE-SR ability	1 = PMA/PMD is able to perform 25GBASE-SR 0 = PMA/PMD is not able to perform 25GBASE-SR	RO
1.19.3	25GBASE-CR ability	1 = PMA/PMD is able to perform 25GBASE-CR 0 = PMA/PMD is not able to perform 25GBASE-CR	RO
1.19.2	25GBASE-CR-S ability	1 = PMA/PMD is able to perform 25GBASE-CR-S 0 = PMA/PMD is not able to perform 25GBASE-CR-S	RO
1.19.1	25GBASE-KR ability	1 = PMA/PMD is able to perform 25GBASE-KR 0 = PMA/PMD is not able to perform 25GBASE-KR	RO
1.19.0	25GBASE-KR-S ability	1 = PMA/PMD is able to perform 25GBASE-KR-S 0 = PMA/PMD is not able to perform 25GBASE-KR-S	RO

[a]RO = Read only

45.2.1.17.1 25GBASE-ER ability (1.19.7)

When read as a one, bit 1.19.7 indicates that the PMA/PMD is able to operate as a 25GBASE-ER PMA/PMD type. When read as a zero, bit 1.19.7 indicates that the PMA/PMD is not able to operate as a 25GBASE-ER PMA/PMD type.

45.2.1.17.2 25GBASE-LR ability (1.19.6)

When read as a one, bit 1.19.6 indicates that the PMA/PMD is able to operate as a 25GBASE-LR PMA/PMD type. When read as a zero, bit 1.19.6 indicates that the PMA/PMD is not able to operate as a 25GBASE-LR PMA/PMD type.

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45.2.1.17.3 25GBASE-T ability (1.19.5)

When read as a one, bit 1.19.5 indicates that the PMA/PMD is able to operate as a 25GBASE-T PMA type. When read as a zero, bit 1.19.5 indicates that the PMA/PMD is not able to operate as a 25GBASE-T PMA type.

45.2.1.17.4 25GBASE-SR ability (1.19.4)

When read as a one, bit 1.19.4 indicates that the PMA/PMD is able to operate as a 25GBASE-SR PMA/PMD type. When read as a zero, bit 1.19.4 indicates that the PMA/PMD is not able to operate as a 25GBASE-SR PMA/PMD type.

45.2.1.17.5 25GBASE-CR ability (1.19.3)

When read as a one, bit 1.19.3 indicates that the PMA/PMD is able to operate as a 25GBASE-CR PMA/PMD type. When read as a zero, bit 1.19.3 indicates that the PMA/PMD is not able to operate as a 25GBASE-CR PMA/PMD type.

45.2.1.17.6 25GBASE-CR-S ability (1.19.2)

When read as a one, bit 1.19.2 indicates that the PMA/PMD is able to operate as a 25GBASE-CR-S PMA/PMD type. When read as a zero, bit 1.19.2 indicates that the PMA/PMD is not able to operate as a 25GBASE-CR-S PMA/PMD type.

45.2.1.17.7 25GBASE-KR ability (1.19.1)

When read as a one, bit 1.19.1 indicates that the PMA/PMD is able to operate as a 25GBASE-KR PMA/PMD type. When read as a zero, bit 1.19.1 indicates that the PMA/PMD is not able to operate as a 25GBASE-KR PMA/PMD type.

45.2.1.17.8 25GBASE-KR-S ability (1.19.0)

When read as a one, bit 1.19.0 indicates that the PMA/PMD is able to operate as a 25GBASE-KR-S PMA/PMD type. When read as a zero, bit 1.19.0 indicates that the PMA/PMD is not able to operate as a 25GBASE-KR-S PMA/PMD type.

45.2.1.18 50G PMA/PMD extended ability (Register 1.20)

The assignment of bits in the 50G PMA/PMD extended ability register is shown in Table 45–21.

Table 45–21—50G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.20.15	50G PMA remote loopback ability	1 = 50G PMA has the ability to perform a remote loopback function 0 = 50G PMA does not have the ability to perform a remote loopback function	RO
1.20.14:6	Reserved	Value always 0	RO
1.20.5	50GBASE-ER ability	1 = PMA/PMD is able to perform 50GBASE-ER 0 = PMA/PMD is not able to perform 50GBASE-ER	RO

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Table 45–21—50G PMA/PMD extended ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.20.4	50GBASE-LR ability	1 = PMA/PMD is able to perform 50GBASE-LR 0 = PMA/PMD is not able to perform 50GBASE-LR	RO
1.20.3	50GBASE-FR ability	1 = PMA/PMD is able to perform 50GBASE-FR 0 = PMA/PMD is not able to perform 50GBASE-FR	RO
1.20.2	50GBASE-SR ability	1 = PMA/PMD is able to perform 50GBASE-SR 0 = PMA/PMD is not able to perform 50GBASE-SR	RO
1.20.1	50GBASE-CR ability	1 = PMA/PMD is able to perform 50GBASE-CR 0 = PMA/PMD is not able to perform 50GBASE-CR	RO
1.20.0	50GBASE-KR ability	1 = PMA/PMD is able to perform 50GBASE-KR 0 = PMA/PMD is not able to perform 50GBASE-KR	RO

[a]RO = Read only

45.2.1.18.1 50G PMA remote loopback ability (1.20.15)

When read as a one, bit 1.20.15 indicates that the 50G PMA is able to perform the remote loopback function. When read as a zero, bit 1.20.15 indicates that the 50G PMA is not able to perform the remote loopback function. If a PMA is able to perform the remote loopback function, then it is controlled using the PMA remote loopback bit 1.0.1 (see 45.2.1.1.4).

45.2.1.18.2 50GBASE-ER ability (1.20.5)

When read as a one, bit 1.20.5 indicates that the PMA/PMD is able to operate as a 50GBASE-ER PMA/PMD type. When read as a zero, bit 1.20.5 indicates that the PMA/PMD is not able to operate as a 50GBASE-ER PMA/PMD type.

45.2.1.18.3 50GBASE-LR ability (1.20.4)

When read as a one, bit 1.20.4 indicates that the PMA/PMD is able to operate as a 50GBASE-LR PMA/PMD type. When read as a zero, bit 1.20.4 indicates that the PMA/PMD is not able to operate as a 50GBASE-LR PMA/PMD type.

45.2.1.18.4 50GBASE-FR ability (1.20.3)

When read as a one, bit 1.20.3 indicates that the PMA/PMD is able to operate as a 50GBASE-FR PMA/PMD type. When read as a zero, bit 1.20.3 indicates that the PMA/PMD is not able to operate as a 50GBASE-FR PMA/PMD type.

45.2.1.18.5 50GBASE-SR ability (1.20.2)

When read as a one, bit 1.20.2 indicates that the PMA/PMD is able to operate as a 50GBASE-SR PMA/PMD type. When read as a zero, bit 1.20.2 indicates that the PMA/PMD is not able to operate as a 50GBASE-SR PMA/PMD type.

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45.2.1.18.6 50GBASE-CR ability (1.20.1)

When read as a one, bit 1.20.1 indicates that the PMA/PMD is able to operate as a 50GBASE-CR PMA/PMD type. When read as a zero, bit 1.20.1 indicates that the PMA/PMD is not able to operate as a 50GBASE-CR PMA/PMD type.

45.2.1.18.7 50GBASE-KR ability (1.20.0)

When read as a one, bit 1.20.0 indicates that the PMA/PMD is able to operate as a 50GBASE-KR PMA/PMD type. When read as a zero, bit 1.20.0 indicates that the PMA/PMD is not able to operate as a 50GBASE-KR PMA/PMD type.

45.2.1.19 2.5G/5G PMA/PMD extended ability register (Register 1.21)

The assignment of bits in the 2.5G/5G PMA/PMD extended ability register is shown in Table 45–22. All of the bits in the PMA/PMD extended ability register are read only; a write to the PMA/PMD extended ability register shall have no effect.

Table 45–22—2.5G/5G PMA/PMD extended ability register bit definitions

Bit	Name	Description	R/W[a]
1.21.15:4	Reserved	Value always 0	RO
1.21.3	5GBASE-KR ability	1 = PMA/PMD is able to perform 5GBASE-KR 0 = PMA/PMD is not able to perform 5GBASE-KR	RO
1.21.2	2.5GBASE-KX ability	1 = PMA/PMD is able to perform 2.5GBASE-KX 0 = PMA/PMD is not able to perform 2.5GBASE-KX	RO
1.21.1	5GBASE-T ability	1 = PMA/PMD is able to perform 5GBASE-T 0 = PMA/PMD is not able to perform 5GBASE-T	RO
1.21.0	2.5GBASE-T ability	1 = PMA/PMD is able to perform 2.5GBASE-T 0 = PMA/PMD is not able to perform 2.5GBASE-T	RO

[a]RO = Read only

NOTE—2.5GBASE-T1 and 5GBASE-T1 PMA/PMD extended abilities can be found in register 1.18, see Table 45–19.

45.2.1.19.1 5GBASE-KR ability (1.21.3)

When read as a one, bit 1.21.3 indicates that the PMA/PMD is able to operate as a 5GBASE-KR PMA/PMD type. When read as a zero, bit 1.21.3 indicates that the PMA/PMD is not able to operate as a 5GBASE-KR PMA/PMD type.

45.2.1.19.2 2.5GBASE-KX ability (1.21.2)

When read as a one, bit 1.21.2 indicates that the PMA/PMD is able to operate as a 2.5GBASE-KX PMA/PMD type. When read as a zero, bit 1.21.2 indicates that the PMA/PMD is not able to operate as a 2.5GBASE-KX PMA/PMD type.

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45.2.1.19.3 5GBASE-T ability (1.21.1)

When read as a one, bit 1.21.1 indicates that the PMA/PMD is able to operate as a 5GBASE-T PMA type. When read as a zero, bit 1.21.1 indicates that the PMA is not able to operate as a 5GBASE-T PMA type.

45.2.1.19.4 2.5GBASE-T ability (1.21.0)

When read as a one, bit 1.21.0 indicates that the PMA/PMD is able to operate as a 2.5GBASE-T PMA type. When read as a zero, bit 1.21.0 indicates that the PMA/PMD is not able to operate as a 2.5GBASE-T PMA type.

45.2.1.20 BASE-H PMA/PMD extended ability register (Register 1.22)

The assignment of bits in the BASE-H PMA/PMD extended ability register is shown in Table 45–23. All of the bits in the BASE-H PMA/PMD extended ability register are read only; a write to the BASE-H PMA/PMD extended ability register shall have no effect.

Table 45–23—BASE-H PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.22.15:3	Reserved	Value always 0	RO
1.22.2	1000BASE-RHC ability	1 = PMA/PMD is able to perform 1000BASE-RHC 0 = PMA/PMD is not able to perform 1000BASE-RHC	RO
1.22.1	1000BASE-RHB ability	1 = PMA/PMD is able to perform 1000BASE-RHB 0 = PMA/PMD is not able to perform 1000BASE-RHB	RO
1.22.0	1000BASE-RHA ability	1 = PMA/PMD is able to perform 1000BASE-RHA 0 = PMA/PMD is not able to perform 1000BASE-RHA	RO

[a]RO = Read Only

45.2.1.21 200G PMA/PMD extended ability register (Register 1.23)

The assignment of bits in the 200G PMA/PMD extended ability register is shown in Table 45–24.

Table 45–24—200G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.23.15	200G PMA remote loopback ability	1 = 200G PMA has the ability to perform a remote loopback function 0 = 200G PMA does not have the ability to perform a remote loopback function	RO
1.23.14:7	Reserved	Value always 0	RO
1.23.6	200GBASE-ER4 ability	1 = PMA/PMD is able to perform 200GBASE-ER4 0 = PMA/PMD is not able to perform 200GBASE-ER4	RO
1.23.5	200GBASE-LR4 ability	1 = PMA/PMD is able to perform 200GBASE-LR4 0 = PMA/PMD is not able to perform 200GBASE-LR4	RO
1.23.4	200GBASE-FR4 ability	1 = PMA/PMD is able to perform 200GBASE-FR4 0 = PMA/PMD is not able to perform 200GBASE-FR4	RO

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Table 45–24—200G PMA/PMD extended ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.23.3	200GBASE-DR4 ability	1 = PMA/PMD is able to perform 200GBASE-DR4 0 = PMA/PMD is not able to perform 200GBASE-DR4	RO
1.23.2	200GBASE-SR4 ability	1 = PMA/PMD is able to perform 200GBASE-SR4 0 = PMA/PMD is not able to perform 200GBASE-SR4	RO
1.23.1	200GBASE-CR4 ability	1 = PMA/PMD is able to perform 200GBASE-CR4 0 = PMA/PMD is not able to perform 200GBASE-CR4	RO
1.23.0	200GBASE-KR4 ability	1 = PMA/PMD is able to perform 200GBASE-KR4 0 = PMA/PMD is not able to perform 200GBASE-KR4	RO

[a]RO = Read only

45.2.1.21.1 200G PMA remote loopback ability (1.23.15)

When read as a one, bit 1.23.15 indicates that the 200G PMA is able to perform the remote loopback function. When read as a zero, bit 1.23.15 indicates that the 200G PMA is not able to perform the remote loopback function. If a PMA is able to perform the remote loopback function, then it is controlled using the PMA remote loopback bit 1.0.1 (see 45.2.1.1.4).

45.2.1.21.2 200GBASE-ER4 ability (1.23.6)

When read as a one, bit 1.23.6 indicates that the PMA/PMD is able to operate as a 200GBASE-ER4 PMA/PMD type. When read as a zero, bit 1.23.6 indicates that the PMA/PMD is not able to operate as a 200GBASE-ER4 PMA/PMD type.

45.2.1.21.3 200GBASE-LR4 ability (1.23.5)

When read as a one, bit 1.23.5 indicates that the PMA/PMD is able to operate as a 200GBASE-LR4 PMA/PMD type. When read as a zero, bit 1.23.5 indicates that the PMA/PMD is not able to operate as a 200GBASE-LR4 PMA/PMD type.

45.2.1.21.4 200GBASE-FR4 ability (1.23.4)

When read as a one, bit 1.23.4 indicates that the PMA/PMD is able to operate as a 200GBASE-FR4 PMA/PMD type. When read as a zero, bit 1.23.4 indicates that the PMA/PMD is not able to operate as a 200GBASE-FR4 PMA/PMD type.

45.2.1.21.5 200GBASE-DR4 ability (1.23.3)

When read as a one, bit 1.23.3 indicates that the PMA/PMD is able to operate as a 200GBASE-DR4 PMA/PMD type. When read as a zero, bit 1.23.3 indicates that the PMA/PMD is not able to operate as a 200GBASE-DR4 PMA/PMD type.

45.2.1.21.6 200GBASE-SR4 ability (1.23.2)

When read as a one, bit 1.23.2 indicates that the PMA/PMD is able to operate as a 200GBASE-SR4 PMA/PMD type. When read as a zero, bit 1.23.2 indicates that the PMA/PMD is not able to operate as a 200GBASE-SR4 PMA/PMD type.

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45.2.1.21.7 200GBASE-CR4 ability (1.23.1)

When read as a one, bit 1.23.1 indicates that the PMA/PMD is able to operate as a 200GBASE-CR4 PMA/PMD type. When read as a zero, bit 1.23.1 indicates that the PMA/PMD is not able to operate as a 200GBASE-CR4 PMA/PMD type.

45.2.1.21.8 200GBASE-KR4 ability (1.23.0)

When read as a one, bit 1.23.0 indicates that the PMA/PMD is able to operate as a 200GBASE-KR4 PMA/PMD type. When read as a zero, bit 1.23.0 indicates that the PMA/PMD is not able to operate as a 200GBASE-KR4 PMA/PMD type.

45.2.1.22 400G PMA/PMD extended ability register (Register 1.24)

The assignment of bits in the 400G PMA/PMD extended ability register is shown in Table 45–25.

Table 45–25—400G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.24.15	400G PMA remote loopback ability	1 = 400G PMA has the ability to perform a remote loopback function 0 = 400G PMA does not have the ability to perform a remote loopback function	RO
1.24.14:11	Reserved	Value always 0	RO
1.24.10	400GBASE-ER8 ability	1 = PMA/PMD is able to perform 400GBASE-ER8 0 = PMA/PMD is not able to perform 400GBASE-ER8	RO
1.24.9	400GBASE-LR4-6 ability	1 = PMA/PMD is able to perform 400GBASE-LR4-6 0 = PMA/PMD is not able to perform 400GBASE-LR4-6	RO
1.24.8	400GBASE-FR4 ability	1 = PMA/PMD is able to perform 400GBASE-FR4 0 = PMA/PMD is not able to perform 400GBASE-FR4	RO
1.24.7	400GBASE-SR4.2 ability	1 = PMA/PMD is able to perform 400GBASE-SR4.2 0 = PMA/PMD is not able to perform 400GBASE-SR4.2	RO
1.24.6	400GBASE-SR8 ability	1 = PMA/PMD is able to perform 400GBASE-SR8 0 = PMA/PMD is not able to perform 400GBASE-SR8	RO
1.24.5	400GBASE-LR8 ability	1 = PMA/PMD is able to perform 400GBASE-LR8 0 = PMA/PMD is not able to perform 400GBASE-LR8	RO
1.24.4	400GBASE-FR8 ability	1 = PMA/PMD is able to perform 400GBASE-FR8 0 = PMA/PMD is not able to perform 400GBASE-FR8	RO
1.24.3	400GBASE-DR4 ability	1 = PMA/PMD is able to perform 400GBASE-DR4 0 = PMA/PMD is not able to perform 400GBASE-DR4	RO
1.24.2	400GBASE-SR16 ability	1 = PMA/PMD is able to perform 400GBASE-SR16 0 = PMA/PMD is not able to perform 400GBASE-SR16	RO
1.24.1:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.1.22.1 400G PMA remote loopback ability (1.24.15)

When read as a one, bit 1.24.15 indicates that the 400G PMA is able to perform the remote loopback function. When read as a zero, bit 1.24.15 indicates that the 400G PMA is not able to perform the remote

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loopback function. If a PMA is able to perform the remote loopback function, then it is controlled using the PMA remote loopback bit 1.0.1 (see 45.2.1.1.4).

45.2.1.22.2 400GBASE-ER8 ability (1.24.10)

When read as a one, bit 1.24.10 indicates that the PMA/PMD is able to operate as a 400GBASE-ER8 PMA/PMD type. When read as a zero, bit 1.24.10 indicates that the PMA/PMD is not able to operate as a 400GBASE-ER8 PMA/PMD type.

45.2.1.22.3 400GBASE-LR4-6 ability (1.24.9)

When read as a one, bit 1.24.9 indicates that the PMA/PMD is able to operate as a 400GBASE-LR4-6 PMA/PMD type. When read as a zero, bit 1.24.9 indicates that the PMA/PMD is not able to operate as a 400GBASE-LR4-6 PMA/PMD type.

45.2.1.22.4 400GBASE-FR4 ability (1.24.8)

When read as a one, bit 1.24.8 indicates that the PMA/PMD is able to operate as a 400GBASE-FR4 PMA/PMD type. When read as a zero, bit 1.24.8 indicates that the PMA/PMD is not able to operate as a 400GBASE-FR4 PMA/PMD type.

45.2.1.22.5 400GBASE-SR4.2 ability (1.24.7)

When read as a one, bit 1.24.7 indicates that the PMA/PMD is able to operate as a 400GBASE-SR4.2 PMA/PMD type. When read as a zero, bit 1.24.7 indicates that the PMA/PMD is not able to operate as a 400GBASE-SR4.2 PMA/PMD type.

45.2.1.22.6 400GBASE-SR8 ability (1.24.6)

When read as a one, bit 1.24.6 indicates that the PMA/PMD is able to operate as a 400GBASE-SR8 PMA/PMD type. When read as a zero, bit 1.24.6 indicates that the PMA/PMD is not able to operate as a 400GBASE-SR8 PMA/PMD type.

45.2.1.22.7 400GBASE-LR8 ability (1.24.5)

When read as a one, bit 1.24.5 indicates that the PMA/PMD is able to operate as a 400GBASE-LR8 PMA/PMD type. When read as a zero, bit 1.24.5 indicates that the PMA/PMD is not able to operate as a 400GBASE-LR8 PMA/PMD type.

45.2.1.22.8 400GBASE-FR8 ability (1.24.4)

When read as a one, bit 1.24.4 indicates that the PMA/PMD is able to operate as a 400GBASE-FR8 PMA/PMD type. When read as a zero, bit 1.24.4 indicates that the PMA/PMD is not able to operate as a 400GBASE-FR8 PMA/PMD type.

45.2.1.22.9 400GBASE-DR4 ability (1.24.3)

When read as a one, bit 1.24.3 indicates that the PMA/PMD is able to operate as a 400GBASE-DR4 PMA/PMD type. When read as a zero, bit 1.24.3 indicates that the PMA/PMD is not able to operate as a 400GBASE-DR4 PMA/PMD type.

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45.2.1.22.10 400GBASE-SR16 ability (1.24.2)

When read as a one, bit 1.24.2 indicates that the PMA/PMD is able to operate as a 400GBASE-SR16 PMA/PMD type. When read as a zero, bit 1.24.5 indicates that the PMA/PMD is not able to operate as a 400GBASE-SR16 PMA/PMD type.

45.2.1.23 PMA/PMD extended ability 2 (Register 1.25)

The assignment of bits in the PMA/PMD extended ability 2 register is shown in Table 45–26.

Table 45–26—PMA/PMD extended ability 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.25.15:1	Reserved	Value always 0	RO
1.25.0	50G extended abilities	1 = PMA/PMD has 50G extended abilities listed in register 1.20 0 = PMA/PMD does not have 50G extended abilities	RO

[a]RO = Read only

45.2.1.23.1 50G extended abilities (1.25.0)

When read as a one, bit 1.25.0 indicates that the PMA/PMD has 50G extended abilities listed in register 1.20. When read as a zero, bit 1.25.0 indicates that the PMA/PMD does not have 50G extended abilities.

45.2.1.24 40G/100G PMA/PMD extended ability 2 (Register 1.26)

The assignment of bits in the 40G/100G PMA/PMD extended ability 2 register is shown in Table 45–27.

Table 45–27—40G/100G PMA/PMD extended ability 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.26.15:10	Reserved	Value always 0	RO
1.26.9	100GBASE-SR2 ability	1 = PMA/PMD is able to perform 100GBASE-SR2 0 = PMA/PMD is not able to perform 100GBASE-SR2	RO
1.26.8	100GBASE-CR2 ability	1 = PMA/PMD is able to perform 100GBASE-CR2 0 = PMA/PMD is not able to perform 100GBASE-CR2	RO
1.26.7	100GBASE-KR2 ability	1 = PMA/PMD is able to perform 100GBASE-KR2 0 = PMA/PMD is not able to perform 100GBASE-KR2	RO
1.26.6	100GBASE-ZR ability	1 = PMA/PMD is able to perform 100GBASE-ZR 0 = PMA/PMD is not able to perform 100GBASE-ZR	RO
1.26.5	100GBASE-LR1 ability	1 = PMA/PMD is able to perform 100GBASE-LR1 0 = PMA/PMD is not able to perform 100GBASE-LR1	RO
1.26.4	100GBASE-FR1 ability	1 = PMA/PMD is able to perform 100GBASE-FR1 0 = PMA/PMD is not able to perform 100GBASE-FR1	RO

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Table 45–27—40G/100G PMA/PMD extended ability 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.26.3	100GBASE-DR ability	1 = PMA/PMD is able to perform 100GBASE-DR 0 = PMA/PMD is not able to perform 100GBASE-DR	RO
1.26.2:0	Reserved	Value always 0	RO

[a] RO = Read only

45.2.1.24.1 100GBASE-SR2 ability (1.26.9)

When read as a one, bit 1.26.9 indicates that the PMA/PMD is able to operate as a 100GBASE-SR2 PMA/PMD type. When read as a zero, bit 1.26.9 indicates that the PMA/PMD is not able to operate as a 100GBASE-SR2 PMA/PMD type.

45.2.1.24.2 100GBASE-CR2 ability (1.26.8)

When read as a one, bit 1.26.8 indicates that the PMA/PMD is able to operate as a 100GBASE-CR2 PMA/PMD type. When read as a zero, bit 1.26.8 indicates that the PMA/PMD is not able to operate as a 100GBASE-CR2 PMA/PMD type.

45.2.1.24.3 100GBASE-KR2 ability (1.26.7)

When read as a one, bit 1.26.7 indicates that the PMA/PMD is able to operate as a 100GBASE-KR2 PMA/PMD type. When read as a zero, bit 1.26.7 indicates that the PMA/PMD is not able to operate as a 100GBASE-KR2 PMA/PMD type.

45.2.1.24.4 100GBASE-ZR ability (1.26.6)

When read as a one, bit 1.26.6 indicates that the PMA/PMD is able to operate as a 100GBASE-ZR PMA/PMD type. When read as a zero, bit 1.26.6 indicates that the PMA/PMD is not able to operate as a 100GBASE-ZR PMA/PMD type.

45.2.1.24.5 100GBASE-LR1 ability (1.26.5)

When read as a one, bit 1.26.5 indicates that the PMA/PMD is able to operate as a 100GBASE-LR1 PMA/PMD type. When read as a zero, bit 1.26.5 indicates that the PMA/PMD is not able to operate as a 100GBASE-LR1 PMA/PMD type.

45.2.1.24.6 100GBASE-FR1 ability (1.26.4)

When read as a one, bit 1.26.4 indicates that the PMA/PMD is able to operate as a 100GBASE-FR1 PMA/PMD type. When read as a zero, bit 1.26.4 indicates that the PMA/PMD is not able to operate as a 100GBASE-FR1 PMA/PMD type.

45.2.1.24.7 100GBASE-DR ability (1.26.3)

When read as a one, bit 1.26.3 indicates that the PMA/PMD is able to operate as a 100GBASE-DR PMA/PMD type. When read as a zero, bit 1.26.3 indicates that the PMA/PMD is not able to operate as a 100GBASE-DR PMA/PMD type.

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45.2.1.25 PMD transmit disable extension register (Register 1.27)

The assignment of bits in the PMD transmit disable extension register is shown in Table 45–28. The transmit disable functionality is optional and a PMD's ability to perform the transmit disable functionality is advertised in the PMD transmit disable ability bit 1.8.8. A PMD that does not implement the transmit disable functionality shall ignore writes to the PMD transmit disable extension register and may return a value of zero for all bits. A PMD device that operates using a single lane and has implemented the transmit disable function shall use bit 1.9.0 to control the function. Such devices shall ignore writes to bit 1.27.0 and return a value of zero for that bit when read.

NOTE 1—This register is an extension of the PMD transmit disable register (see 45.2.1.8).

NOTE 2—Disabling the transmitter on one or more lanes stops the entire link from carrying data.

Table 45–28—PMD transmit disable extension register bit definitions

Bit(s)	Name	Description	R/W[a]
1.27.15:1	Reserved	Value always 0	RO
1.27.0	PMD transmit disable 15	1 = Disable output on transmit lane 15 0 = Enable output on transmit lane 15	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.25.1 PMD transmit disable 15 (1.27.0)

When bit 1.27.0 is set to a one, the PMD shall disable output on lane 15 of the transmit path. When bit 1.27.0 is set to a zero, the PMD shall enable output on lane 15 of the transmit path.

The default value for bit 1.27.0 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.26 PMD receive signal detect extension register (Register 1.28)

The assignment of bits in the PMD receive signal detect extension register is shown in Table 45–29. PMD types that use only a single lane indicate the status of the receive signal detect using bit 1.10.0 and return a value of zero for bit 1.28.0. PMD types that use multiple wavelengths or lanes indicate the status of each lane in bits 1.10.15:1 and 1.28.0 (if needed) and the logical AND of those bits in bit 1.10.0.

NOTE—This register is an extension of the PMD receive signal detect register (see 45.2.1.9).

Table 45–29—PMD receive signal detect extension register bit definitions

Bit(s)	Name	Description	R/W[a]
1.28.15:1	Reserved	Value always 0	RO
1.28.0	PMD receive signal detect 15	1 = Signal detected on receive lane 15 0 = Signal not detected on receive lane 15	RO

[a]RO = Read only

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45.2.1.26.1 PMD receive signal detect 15 (1.28.0)

When bit 1.28.0 is read as a one, a signal has been detected on lane 15 of the PMD receive path. When bit 1.28.0 is read as a zero, a signal has not been detected on lane 15 of the PMD receive path.

45.2.1.27 PMA/PMD control 3 register (Register 1.29)

The assignment of bits in the PMA/PMD control 3 register is shown in Table 45–30.

45.2.1.27.1 Downstream differential encoding (1.29.15)

Downstream differential encoding is selected using bit 1.29.15. This bit is read/write in the OLT and read only in the ONU with the default value of 0 (indicating that downstream differential encoding is not enabled).

In the OLT, this bit controls whether downstream differential encoding is selected for the transmit PMA output.

In the ONU, this bit indicates whether the downstream differential decoding is enabled in the ONU receive PMA.

45.2.1.27.2 PMA/PMD type selection (1.29.5:0)

The PMA/PMD type of the PMA/PMD is selected using bits 5 to 0. The PMA/PMD type abilities of the PMA/PMD are advertised in the Nx25G-EPON PMA/PMD extended ability registers (registers 1.1000 through 1.1002, see 45.2.1.159). A PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

45.2.1.28 10P/2B PMA/PMD control register (Register 1.30)

The assignment of bits in the 10P/2B PMA control register is shown in Table 45–31.

45.2.1.28.1 PMA/PMD link control (1.30.15)

The STA may enable the PMA/PMD link and initiate link initialization by writing this bit to a one. While link is initializing or up, this bit shall remain a one and writing a one to this bit shall be ignored. The STA may force the link down by writing a zero to this bit. While this bit is set to zero, the PHY shall not send G.994.1 handshake tones. For -O subtypes, upon link drop or MMD reset, the PMA/PMD shall set these bits to zero. For -R subtypes, upon link drop or MMD reset, the PMA/PMD shall set these bits to one.

45.2.1.28.2 STFU (1.30.14)

When this bit is set to a one, the PMA/PMD sends a message to the link partner instructing it to be silent for the silence time (see 45.2.1.28.3). Writing to this bit is valid only when the PMA/PMD link status bits in the PMA/PMD status register (see 45.2.1.29.4) are set to “link is down (ready)”. Writes are otherwise ignored.

This bit clears to zero when the silence command is sent, or upon the execution of an MMD reset.

45.2.1.28.3 Silence time (1.30.13:8)

The value of these bits sets the silence time conveyed in a STFU operation (see 45.2.1.28.2). The silence time is encoded according to Equation (45–1), where x is the decimal value of the bits:

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Table 45–30—PMA/PMD control 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.29.15	Downstream differential encoding	1 = Downstream differential encoding enabled 0 = Downstream differential encoding disabled	R/W in OLT RO in ONU
1.29.14:6	Reserved	Value always 0	RO
1.29.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 x x x x = Reserved 1 0 1 x x x = Reserved 1 0 0 1 1 1 = 50GBASE-PQX-U3 1 0 0 1 1 0 = 50GBASE-PQX-U2 1 0 0 1 0 1 = 50GBASE-PQX-D3 1 0 0 1 0 0 = 50GBASE-PQX-D2 1 0 0 0 1 1 = 50GBASE-PQG-U3 1 0 0 0 1 0 = 50GBASE-PQG-U2 1 0 0 0 0 1 = 50GBASE-PQG-D3 1 0 0 0 0 0 = 50GBASE-PQG-D2 0 1 1 1 1 1 = 50/25GBASE-PQX-U3 0 1 1 1 1 0 = 50/25GBASE-PQX-U2 0 1 1 1 0 1 = 50/25GBASE-PQX-D3 0 1 1 1 0 0 = 50/25GBASE-PQX-D2 0 1 1 0 1 1 = 50/25GBASE-PQG-U3 0 1 1 0 1 0 = 50/25GBASE-PQG-U2 0 1 1 0 0 1 = 50/25GBASE-PQG-D3 0 1 1 0 0 0 = 50/25GBASE-PQG-D2 0 1 0 1 1 1 = 50/10GBASE-PQX-U3 0 1 0 1 1 0 = 50/10GBASE-PQX-U2 0 1 0 1 0 1 = 50/10GBASE-PQX-D3 0 1 0 1 0 0 = 50/10GBASE-PQX-D2 0 1 0 0 1 1 = 50/10GBASE-PQG-U3 0 1 0 0 1 0 = 50/10GBASE-PQG-U2 0 1 0 0 0 1 = 50/10GBASE-PQG-D3 0 1 0 0 0 0 = 50/10GBASE-PQG-D2 0 0 1 1 1 1 = 25GBASE-PQX-U3 0 0 1 1 1 0 = 25GBASE-PQX-U2 0 0 1 1 0 1 = 25GBASE-PQX-D3 0 0 1 1 0 0 = 25GBASE-PQX-D2 0 0 1 0 1 1 = 25GBASE-PQG-U3 0 0 1 0 1 0 = 25GBASE-PQG-U2 0 0 1 0 0 1 = 25GBASE-PQG-D3 0 0 1 0 0 0 = 25GBASE-PQG-D2 0 0 0 1 1 1 = 25/10GBASE-PQX-U3 0 0 0 1 1 0 = 25/10GBASE-PQX-U2 0 0 0 1 0 1 = 25/10GBASE-PQX-D3 0 0 0 1 0 0 = 25/10GBASE-PQX-D2 0 0 0 0 1 1 = 25/10GBASE-PQG-U3 0 0 0 0 1 0 = 25/10GBASE-PQG-U2 0 0 0 0 0 1 = 25/10GBASE-PQG-D3 0 0 0 0 0 0 = 25/10GBASE-PQG-D2	R/W

[a]R/W = Read/Write, RO = Read only

$$\text{time} = 10 \times (x + 1) \text{ seconds} \quad (45–1)$$

45.2.1.28.4 Port subtype select (1.30.7)

This register bit selects the port subtype for PMA/PMD operation. The bit defaults to a supported mode. The PHY shall ignore writes that select an unsupported mode (see 45.2.1.28).

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Table 45–31—10P/2B PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.30.15	PMA/PMD link control	1 = begin initialization, enable link (-R default) 0 = force link down (-O default)	R/W
1.30.14	STFU	Silence the far unit 1 = send silence command 0 = silence command inactive (default)	R/W
1.30.13:8	Silence time	Silence time = 10 × (value of bits + 1) seconds	R/W
1.30.7	Port subtype select	1 = port operates as an -O subtype 0 = port operates as a -R subtype	R/W
1.30.6	Handshake cleardown	1 = send cleardown command 0 = idle (default)	R/W, SC
1.30.5	Ignore incoming handshake	1 = PMA/PMD does not respond to handshake tones 0 = PMA/PMD responds to handshake tones	R/W
1.30.4:0	PMA/PMD type selection	4 3 2 1 0 0 0 0 0 0 = 10PASS-TS PMA/PMD type 0 0 0 0 1 = 2BASE-TL PMA/PMD type 0 0 0 1 0 = 2BASE-TL or 10PASS-TS (-R only) 0 0 0 1 1 = 2BASE-TL preferred, or 10PASS-TS (-O only) 0 0 1 0 0 = 10PASS-TS preferred, or 2BASE-TL (-O only) all other values are reserved	R/W

[a]R/W = Read/Write, SC = Self-clearing

Changing this bit alters the fundamental operation of the PMA/PMD, therefore, writes to change this bit shall be ignored if the link is up or initializing (see 45.2.1.29.4).

45.2.1.28.5 Handshake cleardown (1.30.6)

Setting this bit to a one shall cause the PMA/PMD to issue a G.994.1 cleardown command to the link partner (see 61.4.3). The PMA/PMD shall clear this bit to zero after the cleardown command has been sent or upon MMD reset. If the PMA/PMD link is not in the “link down (ready)” state (see 45.2.1.29.4), writes to this register shall be ignored.

45.2.1.28.6 Ignore incoming handshake (1.30.5)

When set to a one, the PMA/PMD shall not respond to received handshake tones (see 61.4.3). When set to a zero, the PMA/PMD shall respond to received handshake tones normally, according to 61.4.3 and G.994.1. Upon MMD reset, this bit shall be cleared to zero.

45.2.1.28.7 PMA/PMD type selection (1.30.4:0)

The PMA/PMD type of a 10P/2B PHY may be selected using bits 4 through 0. A PHY shall ignore writes to the type selection bits that select PMA/PMD types it has not advertised in the speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable port types are applied consistently across all the MMDs on a particular PHY.

A value of 00010 may be set in -R subtype PMA/PMDs that have both 2BASE-TL and 10PASS-TS capability set in the PMA/PMD speed ability register. The PMA/PMD type of the -R is set upon link initialization by the -O.

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Values of 00011 and 00100 may be set in -O subtype PMA/PMDs that have both 2BASE-TL and 10PASS-TS capabilities set in the PMA/PMD speed ability register. These values indicate whether the -R is set to 10PASS-TS or 2BASE-TL respectively. If the -R is not capable of the "preferred" mode, the -R is set to 10PASS-TS or 2BASE-TL respectively.

The selection is advertised during link initialization G.994 handshake.

The PMA/PMD type selection defaults to a supported ability.

45.2.1.29 10P/2B PMA/PMD status register (Register 1.31)

The assignment of bits in the 10P/2B PMA/PMD status register is shown in Table 45–32.

Table 45–32—10P/2B PMA/PMD status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.31.15:5	Data rate	Current operating bit rate of the PMD *n* = the value of the bits Data rate = 64*n* kb/s	RO
1.31.4	CO supported	1 = -O subtype operation supported 0 = -O subtype operation not supported	RO
1.31.3	CPE supported	1 = -R subtype operation supported 0 = -R subtype operation not supported	RO
1.31.2:0	PMA/PMD link status	2 1 0 0 0 0 = link is down (not ready) 1 0 0 = link is down (ready) 0 0 1 = link is initializing 0 1 0 = link is up, 10PASS-TS 0 1 1 = link is up, 2BASE-TL all other values reserved	RO

[a]RO = Read only

45.2.1.29.1 Data rate (1.31.15:5)

These bits indicate the current bit rate of an operational PMA/PMD link. These bits shall be set to all zeros when the link is down or initializing.

45.2.1.29.2 CO supported (1.31.4)

This bit indicates that the PMA/PMD supports operation as a -O subtype. This bit is set to a one when the capability is supported and zero otherwise. This bit reflects the signal PMA_PMD_type in 61.3.2.1.

45.2.1.29.3 CPE supported (1.31.3)

This bit indicates that the PMA/PMD supports operation as a -R subtype. This bit is set to a one when the capability is supported and zero otherwise. This bit reflects the signal PMA_PMD_type in 61.3.2.1.

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45.2.1.29.4 PMA/PMD link status (1.31.2:0)

The overall state of the PMA/PMD link is reflected in bits 2:0. After the PMA/PMD is linked to the remote PHY, the PHY shall set these bits to indicate the PMA/PMD port type that is linked (010 for 10PASS-TS and 011 for 2BASE-TL). The corresponding signal, PMA_received_synchronized, is defined in 61.3.2.1.

While the link is initializing, these bits shall be set to 001.

When read as 000, these bits shall indicate that PMA/PMD link is down and the PMA/PMD is not detecting handshake tones from a link partner. This state is known as “not ready”.

When read as 100, these bits shall indicate that the PMA/PMD link is down and the PMA/PMD is detecting handshake tones from a link partner. This state is known as “ready”.

45.2.1.30 Link partner PMA/PMD control register (Register 1.32)

The 10PASS-TS-O and 2BASE-TL-O PMA/PMDs allow access to certain register values of their link partner via the local MDIO interface. A summary of link partner parameters that may be sent or retrieved is provided in Table 45–33.

Table 45–33—Link partner PMA/PMD registers and PMA/PMD register duals

	Register type	Link partner register	Local register counterpart	
	PHY subtype	-O	-O	-R
Link partner register name		**Address and access type[a]**		
10P/2B link partner RX SNR margin		1.38 RO	1.37 RO	1.37 RO
10P/2B link partner line attenuation		1.40 RO	1.39 RO	1.39 RO
10P/2B link partner line quality thresholds		1.42 R/W	1.41 R/W	n/a
10P link partner FEC correctable errors		1.45 RO	1.43 RO	1.43 RO
10P link partner FEC uncorrectable errors		1.46 RO	1.44 RO	1.44 RO
10P link partner electrical length		1.48 RO	1.47 RO	1.47 RO
2B link partner code violation errors		1.90 RO	1.89 RO	1.89 RO
2B link partner errored seconds		1.92 RO	1.91 RO	1.91 RO
2B link partner severely errored seconds		1.94 RO	1.93 RO	1.93 RO
2B link partner LOSW		1.96 RO	1.95 RO	1.95 RO
2B link partner unavailable seconds		1.98 RO	1.97 RO	1.97 RO
2B link partner state defects register		1.100 RO	1.99 RO	1.99 RO

[a]R/W = Read/Write, RO = read only, n/a = undefined

The Link partner PMA/PMD control register allows the -O STA to control the transmission and retrieval of parameters from its -R link partner.

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The -R STA may read values exchanged by the -O STA in the local register counterpart to the link partner register. For example, the -O 10P link partner electrical length register will be populated with the contents of the -R 10P electrical length register upon a successful “Get link partner parameters” command. Similarly, the -R 10P/2B line quality thresholds register will contain the values sent by the -O in the 10P/2B link partner line quality thresholds register, after a successful “Send link partner parameters” command.

The link partner registers listed in Table 45–33 have the same behavior upon being read or reset as their local register counterparts.

This register is defined for -O port subtypes only.

Bit definitions for the Link partner PMA/PMD control register are found in Table 45–34.

Table 45–34—Link partner PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.32.15	Get link partner parameters	1 = get link partner parameters 0 = operation complete, ready	R/W, SC
1.32.14	Reserved	Value always 0	RO
1.32.13	Send link partner parameters	1 = send link partner parameters 0 = operation complete, ready	R/W, SC
1.32.12:0	Reserved	Value always 0	RO

[a]R/W = Read/Write, SC = Self-clearing, RO = read only

45.2.1.30.1 Get link partner parameters (1.32.15)

When this bit is set to a one, the -O PHY updates its link partner registers shown in Table 45–33 with values from the link partner. While the operation is in progress, the PHY shall keep the bit set as one. If the “Get link partner parameters” operation does not complete within 10 seconds, its result shall be marked as “failed” (see 45.2.1.31) and the operation marked as “complete”. After completion of the operation or upon reset, the PHY shall reset the bit to zero. A write to this bit when link is down shall cause the result to be marked as “failed” and the operation marked as “complete”.

45.2.1.30.2 Send link partner parameters (1.32.13)

When this bit is set to a one, the -O PHY sends the contents of the 2B link partner line quality thresholds register (see 45.2.1.39) to the link partner. While the operation is in progress, the PHY shall keep the bit set as one. The “Send link partner parameters” operation has to complete within 10 seconds, or its result shall be marked as “failed” (see 45.2.1.30) and the operation marked as “complete”. After completion of the operation or upon reset, the PHY shall reset the bit to zero. A write to this bit when link is down shall cause the result to be marked as “failed” and the operation marked as “complete”.

45.2.1.31 Link partner PMA/PMD status register (Register 1.33)

The Link partner PMA/PMD status register reflects the result of the operations that are performed using the Link Partner PMA/PMD control register (1.32).

This register is defined for -O port subtypes only.

Bit definitions for the Link partner PMA/PMD status register are found in Table 45–35.

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Table 45–35—Link Partner PMA/PMD status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.33.15	Reserved	Value always 0	RO
1.33.14	Get link partner result	1 = operation failed 0 = operation successful	RO, LH
1.33.13	Reserved	Value always 0	RO
1.33.12	Send link partner result	1 = operation failed 0 = operation successful	RO, LH
1.33.11:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

45.2.1.31.1 Get link partner result (1.33.14)

After a "Get link partner parameters" operation terminates, this bit reflects the result of the operation. If the operation did not complete successfully, the PHY shall set this bit to a one. Upon being read or a reset, the PHY shall set the bit to zero.

The definition of an unsuccessful "Get link partner parameters" operation is unspecified and left to the implementation.

45.2.1.31.2 Send link partner result (1.33.12)

After a "Send link partner parameters" operation terminates, this bit reflects the result of the operation. If the operation did not complete successfully, the PHY shall set this bit to a one. Upon being read or a reset, the PHY resets the bit to zero.

The definition of an unsuccessful "Send link partner parameters" operation is unspecified and left to the implementation.

45.2.1.32 BiDi PMA/PMD extended ability 1 (Register 1.34)

The assignment of bits in the BiDi PMA/PMD extended ability 1 register is shown in Table 45–36.

Table 45–36—BiDi PMA/PMD extended ability 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.34.15:12	Reserved	Value always 0	RO
1.34.11	25GBASE-BR40-U ability	1 = PMA/PMD is able to perform 25GBASE-BR40-U 0 = PMA/PMD is not able to perform 25GBASE-BR40-U	RO
1.34.10	25GBASE-BR40-D ability	1 = PMA/PMD is able to perform 25GBASE-BR40-D 0 = PMA/PMD is not able to perform 25GBASE-BR40-D	RO
1.34.9	25GBASE-BR20-U ability	1 = PMA/PMD is able to perform 25GBASE-BR20-U 0 = PMA/PMD is not able to perform 25GBASE-BR20-U	RO
1.34.8	25GBASE-BR20-D ability	1 = PMA/PMD is able to perform 25GBASE-BR20-D 0 = PMA/PMD is not able to perform 25GBASE-BR20-D	RO

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Table 45–36—BiDi PMA/PMD extended ability 1 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.34.7	25GBASE-BR10-U ability	1 = PMA/PMD is able to perform 25GBASE-BR10-U 0 = PMA/PMD is not able to perform 25GBASE-BR10-U	RO
1.34.6	25GBASE-BR10-D ability	1 = PMA/PMD is able to perform 25GBASE-BR10-D 0 = PMA/PMD is not able to perform 25GBASE-BR10-D	RO
1.34.5	10GBASE-BR40-U ability	1 = PMA/PMD is able to perform 10GBASE-BR40-U 0 = PMA/PMD is not able to perform 10GBASE-BR40-U	RO
1.34.4	10GBASE-BR40-D ability	1 = PMA/PMD is able to perform 10GBASE-BR40-D 0 = PMA/PMD is not able to perform 10GBASE-BR40-D	RO
1.34.3	10GBASE-BR20-U ability	1 = PMA/PMD is able to perform 10GBASE-BR20-U 0 = PMA/PMD is not able to perform 10GBASE-BR20-U	RO
1.34.2	10GBASE-BR20-D ability	1 = PMA/PMD is able to perform 10GBASE-BR20-D 0 = PMA/PMD is not able to perform 10GBASE-BR20-D	RO
1.34.1	10GBASE-BR10-U ability	1 = PMA/PMD is able to perform 10GBASE-BR10-U 0 = PMA/PMD is not able to perform 10GBASE-BR10-U	RO
1.34.0	10GBASE-BR10-D ability	1 = PMA/PMD is able to perform 10GBASE-BR10-D 0 = PMA/PMD is not able to perform 10GBASE-BR10-D	RO

[a]RO = Read only

45.2.1.32.1 25GBASE-BR40-U ability (1.34.11)

When read as a one, bit 1.34.11 indicates that the PMA/PMD is able to operate as a 25GBASE-BR40-U PMA/PMD type. When read as a zero, bit 1.34.11 indicates that the PMA/PMD is not able to operate as a 25GBASE-BR40-U PMA/PMD type.

45.2.1.32.2 25GBASE-BR40-D ability (1.34.10)

When read as a one, bit 1.34.10 indicates that the PMA/PMD is able to operate as a 25GBASE-BR40-D PMA/PMD type. When read as a zero, bit 1.34.10 indicates that the PMA/PMD is not able to operate as a 25GBASE-BR40-D PMA/PMD type.

45.2.1.32.3 25GBASE-BR20-U ability (1.34.9)

When read as a one, bit 1.34.9 indicates that the PMA/PMD is able to operate as a 25GBASE-BR20-U PMA/PMD type. When read as a zero, bit 1.34.9 indicates that the PMA/PMD is not able to operate as a 25GBASE-BR20-U PMA/PMD type.

45.2.1.32.4 25GBASE-BR20-D ability (1.34.8)

When read as a one, bit 1.34.8 indicates that the PMA/PMD is able to operate as a 25GBASE-BR20-D PMA/PMD type. When read as a zero, bit 1.34.8 indicates that the PMA/PMD is not able to operate as a 25GBASE-BR20-D PMA/PMD type.

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45.2.1.32.5 25GBASE-BR10-U ability (1.34.7)

When read as a one, bit 1.34.7 indicates that the PMA/PMD is able to operate as a 25GBASE-BR10-U PMA/PMD type. When read as a zero, bit 1.34.7 indicates that the PMA/PMD is not able to operate as a 25GBASE-BR10-U PMA/PMD type.

45.2.1.32.6 25GBASE-BR10-D ability (1.34.6)

When read as a one, bit 1.34.6 indicates that the PMA/PMD is able to operate as a 25GBASE-BR10-D PMA/PMD type. When read as a zero, bit 1.34.6 indicates that the PMA/PMD is not able to operate as a 25GBASE-BR10-D PMA/PMD type.

45.2.1.32.7 10GBASE-BR40-U ability (1.34.5)

When read as a one, bit 1.34.5 indicates that the PMA/PMD is able to operate as a 10GBASE-BR40-U PMA/PMD type. When read as a zero, bit 1.34.5 indicates that the PMA/PMD is not able to operate as a 10GBASE-BR40-U PMA/PMD type.

45.2.1.32.8 10GBASE-BR40-D ability (1.34.4)

When read as a one, bit 1.34.4 indicates that the PMA/PMD is able to operate as a 10GBASE-BR40-D PMA/PMD type. When read as a zero, bit 1.34.4 indicates that the PMA/PMD is not able to operate as a 10GBASE-BR40-D PMA/PMD type.

45.2.1.32.9 10GBASE-BR20-U ability (1.34.3)

When read as a one, bit 1.34.3 indicates that the PMA/PMD is able to operate as a 10GBASE-BR20-U PMA/PMD type. When read as a zero, bit 1.34.3 indicates that the PMA/PMD is not able to operate as a 10GBASE-BR20-U PMA/PMD type.

45.2.1.32.10 10GBASE-BR20-D ability (1.34.2)

When read as a one, bit 1.34.2 indicates that the PMA/PMD is able to operate as a 10GBASE-BR20-D PMA/PMD type. When read as a zero, bit 1.34.2 indicates that the PMA/PMD is not able to operate as a 10GBASE-BR20-D PMA/PMD type.

45.2.1.32.11 10GBASE-BR10-U ability (1.34.1)

When read as a one, bit 1.34.1 indicates that the PMA/PMD is able to operate as a 10GBASE-BR10-U PMA/PMD type. When read as a zero, bit 1.34.1 indicates that the PMA/PMD is not able to operate as a 10GBASE-BR10-U PMA/PMD type.

45.2.1.32.12 10GBASE-BR10-D ability (1.34.0)

When read as a one, bit 1.34.0 indicates that the PMA/PMD is able to operate as a 10GBASE-BR10-D PMA/PMD type. When read as a zero, bit 1.34.0 indicates that the PMA/PMD is not able to operate as a 10GBASE-BR10-D PMA/PMD type.

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45.2.1.33 BiDi PMA/PMD extended ability 2 (Register 1.35)

The assignment of bits in the BiDi PMA/PMD extended ability 2 register is shown in Table 45–37.

Table 45–37—BiDi PMA/PMD extended ability 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.35.15:6	Reserved	Value always 0	RO
1.35.5	50GBASE-BR40-U ability	1 = PMA/PMD is able to perform 50GBASE-BR40-U 0 = PMA/PMD is not able to perform 50GBASE-BR40-U	RO
1.35.4	50GBASE-BR40-D ability	1 = PMA/PMD is able to perform 50GBASE-BR40-D 0 = PMA/PMD is not able to perform 50GBASE-BR40-D	RO
1.35.3	50GBASE-BR20-U ability	1 = PMA/PMD is able to perform 50GBASE-BR20-U 0 = PMA/PMD is not able to perform 50GBASE-BR20-U	RO
1.35.2	50GBASE-BR20-D ability	1 = PMA/PMD is able to perform 50GBASE-BR20-D 0 = PMA/PMD is not able to perform 50GBASE-BR20-D	RO
1.35.1	50GBASE-BR10-U ability	1 = PMA/PMD is able to perform 50GBASE-BR10-U 0 = PMA/PMD is not able to perform 50GBASE-BR10-U	RO
1.35.0	50GBASE-BR10-D ability	1 = PMA/PMD is able to perform 50GBASE-BR10-D 0 = PMA/PMD is not able to perform 50GBASE-BR10-D	RO

[a]RO = Read only

45.2.1.33.1 50GBASE-BR40-U ability (1.35.5)

When read as a one, bit 1.35.5 indicates that the PMA/PMD is able to operate as a 50GBASE-BR40-U PMA/PMD type. When read as a zero, bit 1.35.5 indicates that the PMA/PMD is not able to operate as a 50GBASE-BR40-U PMA/PMD type.

45.2.1.33.2 50GBASE-BR40-D ability (1.35.4)

When read as a one, bit 1.35.4 indicates that the PMA/PMD is able to operate as a 50GBASE-BR40-D PMA/PMD type. When read as a zero, bit 1.35.4 indicates that the PMA/PMD is not able to operate as a 50GBASE-BR40-D PMA/PMD type.

45.2.1.33.3 50GBASE-BR20-U ability (1.35.3)

When read as a one, bit 1.35.3 indicates that the PMA/PMD is able to operate as a 50GBASE-BR20-U PMA/PMD type. When read as a zero, bit 1.35.3 indicates that the PMA/PMD is not able to operate as a 50GBASE-BR20-U PMA/PMD type.

45.2.1.33.4 50GBASE-BR20-D ability (1.35.2)

When read as a one, bit 1.35.2 indicates that the PMA/PMD is able to operate as a 50GBASE-BR20-D PMA/PMD type. When read as a zero, bit 1.35.2 indicates that the PMA/PMD is not able to operate as a 50GBASE-BR20-D PMA/PMD type.

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45.2.1.33.5 50GBASE-BR10-U ability (1.35.1)

When read as a one, bit 1.35.1 indicates that the PMA/PMD is able to operate as a 50GBASE-BR10-U PMA/PMD type. When read as a zero, bit 1.35.1 indicates that the PMA/PMD is not able to operate as a 50GBASE-BR10-U PMA/PMD type.

45.2.1.33.6 50GBASE-BR10-D ability (1.35.0)

When read as a one, bit 1.35.0 indicates that the PMA/PMD is able to operate as a 50GBASE-BR10-D PMA/PMD type. When read as a zero, bit 1.35.0 indicates that the PMA/PMD is not able to operate as a 50GBASE-BR10-D PMA/PMD type.

45.2.1.34 10P/2B PMA/PMD link loss register (Register 1.36)

The 10P/2B PMA/PMD link loss register is a 16 bit counter that contains the number of times the PMA/PMD link is lost. Link is considered lost when the PMA_receive_synchronized signal (see 61.3.2.1) transitions from up to down. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PMA/PMD link loss register is shown in Table 45–38.

Table 45–38—10P/2B PMA/PMD link loss register bit definitions

Bit(s)	Name	Description	R/W[a]
1.36.15:0	Link lost events	The bytes of the counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.35 10P/2B RX SNR margin register (Register 1.37)

For further information on 2BASE-TL SNR margin, see 63.3. For 10PASS-TS SNR margin, see 62.3.

The bit definitions for the 10P/2B RX SNR margin register are found in Table 45–39.

Table 45–39—10P/2B RX SNR margin register bit definition

Bit(s)	Name	Description	R/W[a]
1.37.15:8	Reserved	Value always 0	RO
1.37.7:0	RX SNR margin	Value of SNR margin in dB	RO

[a]RO = Read only

45.2.1.36 10P/2B link partner RX SNR margin register (Register 1.38)

The 10P/2B link partner RX SNR margin register provides access to the link partner's receive SNR margin. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link partner PMA/PMD control register (see 45.2.1.30) and the command completes successfully (see 45.2.1.31.1).

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This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–39.

45.2.1.37 10P/2B line attenuation register (Register 1.39)

This register reports the line attenuation as measured by the PMA/PMD. For more information, see the reference documents in 63.3 and 62.3.

The bit definitions for the 10P/2B line attenuation register are found in Table 45–40.

Table 45–40—10P/2B line attenuation register bit definitions

Bit(s)	Name	Description	R/W[a]
1.39.15:0	Line attenuation	The value of the line attenuation in dB, as perceived by the local PMD.	RO

[a]RO = Read only

45.2.1.38 10P/2B link partner line attenuation register (Register 1.40)

The 10P/2B link partner line attenuation register provides access to the link partner's perceived line attenuation margin. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link partner PMA/PMD control register (see 45.2.1.30) and the command completes successfully (see 45.2.1.31.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–40.

45.2.1.39 10P/2B line quality thresholds register (Register 1.41)

The 10P/2B line quality thresholds register sets the target environment for the 10PASS-TS/2BASE-TL connection. The line quality is defined by the SNR margin and line attenuation values.

Bit definitions for the 10P/2B line quality threshold register are found in Table 45–41.

Table 45–41—10P/2B line quality thresholds register bit definition

Bit(s)	Name	Description	R/W[a]
1.41.15:8	Loop attenuation threshold	Attenuation threshold in dB	O: R/W R: RO
1.41.7:4	SNR margin threshold	SNR margin threshold in dB	O: R/W R: RO
1.41.3:0	Reserved	Value always 0	RO

[a]R/W = Read/Write, RO = Read only

45.2.1.39.1 Loop attenuation threshold (1.41.15:8)

These bits set the loop attenuation threshold for 2BASE-TL PMA/PMDs. Writing to these bits on a 10PASS-TS PMA/PMD shall have no effect. The threshold value is in units of dB. For more information on the loop attenuation threshold, see 63.2.2.3.

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45.2.1.39.2 SNR margin threshold (1.41.7:4)

These bits set the SNR margin threshold for 10PASS-TS and 2BASE-TL PMA/PMDs. The threshold is expressed in units of dB. For more information of the SNR margin threshold, see 63.2.2.3 for 2BASE-TL and Section 10 of the document referenced in 62.1.3 for 10PASS-TS.

45.2.1.40 2B link partner line quality thresholds register (Register 1.42)

The 2B link partner line quality thresholds register allows the -O STA to set its -R link partner's line quality thresholds. The contents of this register are transmitted to the -R when the STA activates the "Send link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.30) and the command completes successfully (see 45.2.1.31.2).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–41.

45.2.1.41 10P FEC correctable errors counter (Register 1.43)

The 10P FEC correctable errors counter is a 16 bit counter that contains the number of FEC codewords that have been received and corrected. For more information on 10PASS-TS FEC, see 62.2.4.2. These bits shall be reset to all zeros upon execution of the MMD reset and upon being read. The assignment of bits in the 10P FEC correctable error counter is shown in Table 45–42.

Table 45–42—10P FEC correctable errors counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.43.15:0	Correctable codewords [15:0]	The bytes of the counter	RO

[a]RO = Read only

45.2.1.42 10P FEC uncorrectable errors counter (Register 1.44)

The 10P FEC uncorrectable errors counter is a 16 bit counter that contains the number of FEC codewords that have been received and are uncorrectable. For more information on 10PASS-TS FEC, see 62.2.4.2. These bits shall be reset to all zeros upon execution of the MMD reset and upon being read. The assignment of bits in the 10P FEC uncorrectable error counter is shown in Table 45–43.

Table 45–43—10P FEC uncorrectable errors counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.44.15:0	Uncorrectable codewords [15:0]	The bytes of the counter	RO

[a]RO = Read only

45.2.1.43 10P link partner FEC correctable errors register (Register 1.45)

The 10P link partner FEC correctable errors register provides the -O STA with a snapshot of the -R link partner's FEC correctable errors counter. Because this register is not a counter, its value will increment only

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when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.30) and the command completes successfully (see 45.2.1.31.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–42 and 45.2.1.41.

45.2.1.44 10P link partner FEC uncorrectable errors register (Register 1.46)

The 10P link partner FEC uncorrectable errors register provides the -O STA a snapshot of the -R link partner's FEC uncorrectable errors counter. Because this register is not a counter, its value will increment only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.30) and the command completes successfully (see 45.2.1.31.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–43 and 45.2.1.42.

45.2.1.45 10P electrical length register (Register 1.47)

The bit definitions for the 10P electrical length register are found in Table 45–44.

Table 45–44—10P electrical length register bit definitions

Bit(s)	Name	Description	R/W[a]
1.47.15:0	Electrical length	The electrical length of the medium (in meters), as perceived at the local PMD	RO

[a]RO = Read only

45.2.1.45.1 Electrical length (1.47.15:0)

After the link is established, these bits contain the measured electrical length (in meters) of the medium as measured by the PMD. If the link is down or the PMD is unable to determine the electrical length, these bits shall be set to all ones (see 62.3.2).

45.2.1.46 10P link partner electrical length register (Register 1.48)

The 10P link partner electrical length register provides access to the link partner's electrical length measurement. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.30) and the command completes successfully (see 45.2.1.31.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–44 and 45.2.1.45.1.

45.2.1.47 10P PMA/PMD general configuration register (Register 1.49)

The 10P PMA/PMD general configuration register is defined for -O port types only.

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The 10P PMA/PMD general configuration register bit definitions are found in Table 45–45.

Table 45–45—10P PMA/PMD general configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.49.15:8	Reserved	Value always 0	RO
1.49.7:0	TX window length	Transmit window length	O: R/W R: undefined

[a]RO = Read only, R/W = Read/Write

45.2.1.47.1 TX window length (1.49.7:0)

Bits 7:0 control the PMD transmit window length within the cyclic prefix and suffix in units of number of samples, as defined in 62.3.2.

45.2.1.48 10P PSD configuration register (Register 1.50)

This register is defined for -O port subtypes only.

The 10P PSD configuration register bit definitions may be found in Table 45–46.

Table 45–46—10P PSD configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.50.15:9	Reserved	Value always 0	RO
1.50.8	PBO disable	1 = PBO disabled 0 = PBO normal operation	O: R/W R: undefined
1.50.7:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

45.2.1.48.1 PBO disable (1.50.8)

Setting this bit to a one disables UPBO for performance testing purposes. Refer to 62.3.4.4.

45.2.1.49 10P downstream data rate configuration (Registers 1.51, 1.52)

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The bit definitions for the 10P downstream data rate configuration registers are found in Table 45–47.

Table 45–47—10P downstream data rate configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.51.15:0	Minimum downstream data rate	Sets the minimum required downstream payload data rate *M* = value of bits Data rate = *M* × 64000 b/s	O: R/W R: undefined
1.52.15:0	Maximum downstream data rate	Sets the maximum downstream payload data rate *M* = value of bits Data rate = *M* × 64000 b/s	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.50 10P downstream Reed-Solomon configuration (Register 1.53)

This register is defined for -O port subtypes only.

The bit definitions for 10P downstream Reed-Solomon configuration are found in Table 45–48.

Table 45–48—10P downstream Reed-Solomon configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.53.15:1	Reserved	Value always 0	RO
1.53.0	RS codeword length	1 = codeword length of 144 0 = codeword length of 240	O: R/W R: undefined

[a]RO = Read only, R/W = Read/Write

45.2.1.50.1 RS codeword length (1.53.0)

This bit selects the Reed-Solomon forward error correction codeword length used in the downstream direction. For more information, see 62.2.4.2.

45.2.1.51 10P upstream data rate configuration (Registers 1.54, 1.55)

These registers are defined for -O port subtypes only.

The bit definitions for 10P upstream data rate configuration are found in Table 45–49.

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Table 45–49—10P upstream data rate configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.54.15:0	Minimum upstream data rate	Sets the required upstream payload data rate *M* = value of bits Data rate = *M* × 64000 b/s	O: R/W R: undefined
1.55.15:0	Maximum upstream data rate	Sets the maximum upstream payload data rate *M* = value of bits Data rate = *M* × 64000 b/s	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.52 10P upstream 10P upstream Reed-Solomon configuration register (Register 1.56)

This register is defined for -O port subtypes only.

The bit definitions for the 10P upstream Reed-Solomon configuration are found in Table 45–50.

Table 45–50—10P upstream Reed-Solomon configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.56.15:1	Reserved	Value always 0	RO
1.56.0	RS codeword length	1 = codeword length = 144 0 = codeword length = 240	O: R/W R: undefined

[a]RO = Read only, R/W = Read/Write

45.2.1.52.1 RS codeword length (1.56.0)

This bit selects the Reed-Solomon forward error correction codeword length used in the upstream direction. For more information, see 62.2.4.2.

45.2.1.53 10P tone group registers (Registers 1.57, 1.58)

10PASS-TS operates by modulating 4096 individual tones across the transmission spectrum. Each tone can be assigned a PSD level, desired SNR margin and transmission direction (downstream or upstream). To reduce the complexity of addressing individual tones, tones are addressed by group. The STA sets the lower and upper tones in a group, sets the parameters for that group, and issues a command to activate those parameters for that group. See 62.3.4.7 for details on the mechanism that transfers tone information across the link to and from the -R link partner.

This register allows the STA to specify the range of tones to control. The bit definitions for the 10P tone group register are defined in Table 45–51.

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Table 45–51—10P tone group register bit definitions

Bit(s)	Name	Description	R/W[a]
1.57.15:0	Lower tone	The number of the lower frequency tone in the group. Valid when ≤ the Upper tone.	R/W
1.58.15:0	Upper tone	The number of the higher frequency tone in the group. Valid when ≥ the Lower tone.	R/W

[a]R/W = Read/Write

45.2.1.54 10P tone control parameters (Registers 1.59, 1.60, 1.61, 1.62, 1.63)

These registers allow the STA to specify parameters for the tones selected in the 10P tone group registers. These values do not take effect until the corresponding activation commands are issued in the 10P tone control action register. The bit definitions for the 10P tone control parameters are shown in Table 45–52.

These registers are defined for -O port subtypes only.

Table 45–52—10P tone control parameters register bit definitions

Bit(s)	Name	Description	R/W[a]
1.59.15	Tone active	1 = selected tones are active 0 = selected tones are disabled	R/W
1.59.14	Tone direction	1 = selected tones assigned to upstream communication 0 = selected tones assigned to downstream communication	R/W
1.59.13:5	Max SNR margin	Assigns the maximum SNR margin the PMD may achieve *M* = value of bits Max SNR margin = *M*/4 dB	R/W
1.59.4:0	Reserved	Value always 0	RO
1.60:15:9	Reserved	Value always 0	RO
1.60.8:0	Target SNR margin	Assigns the target SNR margin for the selected tones *M* = value of bits Target SNR margin = *M*/4 dB	R/W
1.61:15:9	Reserved	Value always 0	RO
1.61.8:0	Min SNR margin	Assigns the minimum SNR margin for the selected tones *M* = value of bits Min SNR margin = *M*/4 dB	R/W
1.62.15:9	Reserved	Value always 0	RO
1.62.8:0	PSD level	Assigns a TX PSD level for the selected tones in dBm/Hz *P* = value of bits (2's complement) PSD level = *P*/4 – 100 dBm/Hz	R/W
1.63.15:9	Reserved	Value always 0	RO
1.63.8:0	USPBO reference	Assigns the level of the USPBO reference at the points represented by the selected tones *P* = value of bits (2's complement) PSD level = *P*/4 – 100 dBm/Hz	R/W

[a]R/W = Read/Write, RO = Read only

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45.2.1.54.1 Tone active (1.59.15)

These bits are used to control the activity of the selected tones. When the "Change tone activity" command is issued (1.64.4), the selected tones will be either activated or deactivated based on the value set in these bits.

45.2.1.54.2 Tone direction (1.59.14)

These bits are used to control the direction of the selected tones. When the "Change tone direction" command is issued (1.64.3), the selected tones will adopt the direction set in these bits.

45.2.1.54.3 Max SNR margin (1.59.13:5)

These bits control the maximum SNR margin for the selected tones. When the "Change SNR margin" command is issued (1.64.2), the PMA/PMD will use the value set in these bits in calculations related to maximum SNR margin. The SNR margin is in units of dB, derived by dividing the value of bits 13:5 by 4.

45.2.1.54.4 Target SNR margin (1.60.8:0)

These bits control the target SNR margin for the selected tones. When the "Change SNR margin" command is issued (1.64.2), the PMA/PMD will use the value set in these bits in calculations related to target SNR margin. The target SNR margin is in units of dB, derived by dividing the value of bits 8:0 by 4.

45.2.1.54.5 Minimum SNR margin (1.61.8:0)

These bits control the minimum SNR margin for the selected tones. When the "Change SNR margin" command is issued (1.64.2), the PMA/PMD will use the value set in these bits in calculations related to minimum SNR margin. The minimum SNR margin is in units of dB, derived by dividing the value of bits 8:0 by 4.

45.2.1.54.6 PSD level (1.62.8:0)

These bits control the transmit PSD level of the selected tones. When the "Change PSD level" command is issued (1.64.1), the PMA/PMD will set the PSD level of the selected tones to according to Equation (45–2), where x is the value of bits 8:0:

$$power = \frac{x}{4} - 100\frac{\text{dBm}}{\text{Hz}} \tag{45–2}$$

45.2.1.54.7 USPBO reference (1.63.8:0)

These bits control the reference level for the upstream power back-off function of the PMA/PMD. When the "Change USPBO reference PSD" command (1.64.0) is issued, the portion of the USPBO reference curve that corresponds to the selected tones is changed to the value specified by these bits. The USPBO reference level is specified according to Equation (45–3), where x is the value of bits 8:0:

$$power = \frac{x}{4} - 100\frac{\text{dBm}}{\text{Hz}} \tag{45–3}$$

45.2.1.55 10P tone control action register (Register 1.64)

The operations in this register apply to the tones selected in the 10P tone group registers (1.57, 1.58).

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This register is defined for -O port subtypes only.

The bit definitions for the 10P tone control action register are shown in Table 45–53.

Table 45–53—10P tone control action register bit definitions

Bit(s)	Name	Description	R/W[a]
1.64.15:6	Reserved	Value always 0	RO
1.64.5	Refresh tone status	1 = refresh selected tones for the 10P tone status registers 0 = ready, operation complete	R/W, SC
1.64.4	Change tone activity	1 = activate tone active setting as in tone control parameter register 0 = ready, operation complete	R/W, SC
1.64.3	Change tone direction	1 = activate tone direction setting as in tone control parameter register 0 = ready, operation complete	R/W, SC
1.64.2	Change SNR margin	1 = activate min, max and target SNR margin settings as in tone control parameter register 0 = ready, operation complete	R/W, SC
1.64.1	Change PSD level	1 = activate PSD level setting as in tone control parameter register 0 = ready, operation complete	R/W, SC
1.64.0	Change UPBO reference PSD	1 = activate UPBO reference PSD settings as in tone control parameter register 0 = ready, operation complete	R/W, SC

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.1.55.1 Refresh tone status (1.64.5)

When this bit is set to a one, the tone status information from the local and link partner is gathered so that it may be read using the 10P tone status registers (1.65, 1.66, and 1.67). While the tones are being refreshed, this bit shall remain set as one. This bit shall be reset to zero when the refresh operation is over or upon reset.

NOTE—Refreshing a large number of tones may take a long time to complete.

45.2.1.55.2 Change tone activity (1.64.4)

When this bit is set to a one, the selected tones are enabled or disabled according to the assignment in the tone active bit of the 10P tone control parameters register (1.59.15). While the tones are being activated/deactivated, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.55.3 Change tone direction (1.64.3)

When this bit is set to a one, the transmission direction of selected tones is changed according to the assignment in the tone direction bit of the 10P tone control parameters register (1.59.14). While the tones are being assigned, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

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45.2.1.55.4 Change SNR margin (1.64.2)

When this bit is set to a one, the SNR margin parameters for the selected tones are loaded according the assignment in the Minimum, Target and Maximum SNR margin bits of the 10P tone control parameters register (1.59.13:5, 1.60.8:0, 1.61.8:0). While the parameters are being loaded, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.55.5 Change PSD level (1.64.1)

When this bit is set to a one, the PSD level for the selected tones is set according to the value in the PSD level bits of the 10P tone control parameters register (1.62.8:0). While the PSD is being set, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.55.6 Change USPBO reference PSD (1.64.0)

When this bit is set to a one, the upstream power back-off reference PSD level for the selected tones is set according to the value in the USPBO PSD reference bits of the 10P tone control parameters register (1.63.8:0). While the reference PSD is being set, this bit shall remain set as one. This bit shall be reset to zero when the operation is over or upon reset.

45.2.1.56 10P tone status registers (Registers 1.65, 1.66, 1.67)

The 10P tone status registers allow the STA to query the status of any individual tone in the link. The values read in the 10P tone status register correspond to the tone whose number is set in the “Lower tone” of the 10P tone group registers (see 45.2.1.53).

The status of some tones is read from the link partner. Because the constant update of these values would be a strain on channel resources, these values are only updated for selected tones when the “Refresh tone table” command is issued in the 10P tone control action register (1.64).

The 10P tone status registers bit definitions are given in Table 45–54.

Table 45–54—10P tone status registers bit definitions

Bit(s)	Name	Description	R/W[a]
1.65.15	Refresh status	1 = tone entry has been refreshed 0 = tone entry has not been refreshed since last read	RO
1.65.14	Active	1 = tone is disabled 0 = tone is active	RO
1.65.13	Direction	1 = tone is assigned to upstream communication 0 = tone is assigned to downstream communication	RO
1.65.12:8	Reserved	Value always 0	RO
1.65.7:0	RX PSD	PSD of the tone at the receiver in dBm/Hz	RO
1.66.15:8	TX PSD	PSD of the tone at the transmitter in dBm/Hz	RO
1.66.7:3	Bit load	The number of bits currently loaded on the tone	RO
1.66.2:0	Reserved	Value always 0	RO
1.67.15:10	Reserved	Value always 0	RO
1.67.9:0	SNR margin	Current SNR margin for the tone *R* = value of bits SNR Margin = *R*/4 dB	RO

[a]RO = Read only

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45.2.1.56.1 Refresh status (1.65.15)

When read as a one, bit 1.65.15 indicates that the values for this tone table have not been read since the last "Refresh tone status" command was issued by the 10P tone control action register (1.64). Upon reading this bit or upon reset, the bit shall be reset to zero.

45.2.1.56.2 Active (1.65.14)

When read as a one, this bit indicates that the selected tone is disabled (i.e., powered off and not carrying data).

45.2.1.56.3 Direction (1.65.13)

When read as a one, this bit indicates that the selected tone is assigned to upstream communication. When read as a zero, the tone is assigned to downstream communication.

45.2.1.56.4 RX PSD (1.65.7:0)

These bits report the PSD of the selected tone as perceived at the receiver in units of dBm/Hz.

45.2.1.56.5 TX PSD (1.66.15:8)

These bits report the PSD of the selected tone as output by the transmitter in units of dBm/Hz.

45.2.1.56.6 Bit load (1.66.7:3)

These bits report the number of bits encoded on the selected tone.

45.2.1.56.7 SNR margin (1.67.9:0)

These bits report the current SNR margin for the selected tone, as perceived by the receiver, in units of dB. The value of the SNR margin is obtained by dividing the decimal value of bits 9:0 by 4.

45.2.1.57 10P outgoing indicator bits status register (Register 1.68)

The 10P outgoing indicator bits status register conveys the current state of the indicator bits being sent to the link partner (See 62.3.4.7). The bit definitions for the 10P indicator bits status register are shown in Table 45–55.

Table 45–55—10P outgoing indicator bits status register bit definition

Bit(s)	Name	Description	R/W[a]
1.68.15:9	Reserved	Value always 0	RO
1.68.8	LoM	1 = received signal below SNR margin threshold 0 = normal state	RO
1.68.7	lpr	1 = power supply voltage invalid 0 = normal state	RO
1.68.6	po	1 = PMA/PMD is being powered off 0 = normal state	RO
1.68.5	Rdi	1 = severely errored frames have been received 0 = normal state	RO
1.68.4	los	1 = signal power is lower than the threshold 0 = normal state	RO

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Table 45–55—10P outgoing indicator bits status register bit definition *(continued)*

Bit(s)	Name	Description	R/W[a]
1.68.3:2	Reserved	Value always 0	RO
1.68.1	fec-s	1 = corrected errors have been detected in the received FEC block of slow data 0 = normal state	RO
1.68.0	be-s	1 = non-corrected errors have been detected in the received block of slow data 0 = normal state	RO

[a]RO = Read only

NOTE—These bit refer to “slow” data. 10PASS-TS uses the slow data channel as referenced in ATIS-0600424. The name is kept here to simplify a comparison between the two documents.

45.2.1.57.1 LoM (1.68.8)

When read as a one, this bit indicates that the PMA/PMD is receiving a signal whose SNR margin is below the set threshold (see 45.2.1.39). The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.57.2 lpr (1.68.7)

When read as a one, this bit indicates that the PMA/PMD is not receiving sufficient power supply input for proper operation. The specific conditions that cause this bit to be set are implementation specific. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.57.3 po (1.68.6)

When read as a one, this bit indicates that the PMA/PMD has been instructed to power off. The specific conditions that cause this bit to be set are implementation specific. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.57.4 Rdi (1.68.5)

When read as a one, this bit indicates that the PMA/PMD has received PMA/PMD frames containing severe errors. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.57.5 los (1.68.4)

When read as a one, this bit indicates that the PMA/PMD is not receiving a valid signal. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.57.6 fec-s (1.68.1)

When read as a one, this bit indicates that the PMA/PMD is receiving FEC blocks with one or more correctable errors. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

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45.2.1.57.7 be-s (1.68.0)

When read as a one, this bit indicates that the PMA/PMD is receiving FEC blocks with one or more uncorrectable errors. The status of this condition is reported to the link partner PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.58 10P incoming indicator bits status register (Register 1.69)

The 10P indicator bits status register conveys the current state of the indicator bits being received from the link partner's PMA (see 62.3.4.7). The bit definitions for the 10P incoming indicator bits status register are shown in Table 45–56.

Table 45–56—10P incoming indicator bits status register bit definition

Bit(s)	Name	Description	R/W[a]
1.69.15:9	Reserved	Value always 0	RO
1.69.8	LoM	1 = received signal below SNR margin threshold 0 = normal state	RO
1.69.7	Flpr	1 = power supply voltage invalid 0 = normal state	RO
1.69.6	Fpo	1 = PMA/PMD is being powered off 0 = normal state	RO
1.69.5	Rdi	1 = severely errored frames have been received 0 = normal state	RO
1.69.4	Flos	1 = signal power is lower than the threshold 0 = normal state	RO
1.69.3:2	Reserved	Value always 0	RO
1.69.1	Ffec-s	1 = corrected errors have been detected in the received FEC block of slow data 0 = normal state	RO
1.69.0	Febe-s	1 = non-corrected errors have been detected in the received block of slow data 0 = normal state	RO

[a]RO = Read only

NOTE—These bit refer to "slow" data. 10PASS-TS uses the slow data channel as referenced in ATIS-0600424. The name is kept here to simplify a comparison between the two documents.

45.2.1.58.1 LoM (1.69.8)

When read as a one, this bit indicates that the link partner PMA/PMD is receiving a signal whose SNR margin is below the set threshold (see 45.2.1.39). The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.58.2 Flpr (1.69.7)

When read as a one, this bit indicates that the link partner PMA/PMD is not receiving sufficient power supply input for proper operation. The specific conditions that cause this bit to be set are implementation specific. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

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45.2.1.58.3 Fpo (1.69.6)

When read as a one, this bit indicates that the link partner PMA/PMD has been instructed to power off. The specific conditions that cause this bit to be set are implementation specific. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.58.4 Rdi (1.69.5)

When read as a one, this bit indicates that the link partner PMA/PMD has received PMA/PMD frames containing severe errors. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.58.5 Flos (1.69.4)

When read as a one, this bit indicates that the link partner PMA/PMD has is not receiving a valid signal. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.58.6 Ffec-s (1.69.1)

When read as a one, this bit indicates that the link partner PMA/PMD is receiving FEC blocks with one or more correctable errors. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.58.7 Febe-s (1.69.0)

When read as a one, this bit indicates that the link partner PMA/PMD is receiving FEC blocks with one or more uncorrectable errors. The status of this condition is reported to the local PMA/PMD via the 10PASS-TS indicator bits.

45.2.1.59 10P cyclic extension configuration register (Register 1.70)

The 10P cyclic extension configuration register controls the length of the cyclic extension for the 10P PMD. For more information, see 62.3.4.2. The value of the cyclic extension is equal to the decimal value set in bits 15:0. Values of decimal 10, 20 and 40 are valid. Writes to set any other values shall be ignored. Upon reset, the PMD shall set these bits to a decimal value of 20.

The bit definitions for this register are shown in Table 45–57.

Table 45–57—10P cyclic extension configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.70.15:0	Cyclic extension	The value of the cyclic extension	O: R/W R: RO

[a]R/W = Read/Write, RO = Read only

45.2.1.60 10P attainable downstream data rate register (Register 1.71)

The 10P attainable downstream data rate register reports the data rate that the -R link partner measures to be the highest data rate for downstream transmission. The data rate is encoded as 1 kb/s times the decimal value of the register bits 15:0. The value of the register bits are not valid until after link is “up” (see 45.2.1.29.4).

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The bit definitions for this register are found in Table 45–58.

Table 45–58—10P attainable downstream data rate register bit definitions

Bit(s)	Name	Description	R/W[a]
1.71.15:0	Attainable downstream data rate	Data rate in 1 kb/s increments	RO

[a]RO = Read only

45.2.1.61 2B general parameter register (Register 1.80)

The 2B general parameter register controls various parameters for the operation of the 2BASE-TL PMA/PMD.

This register is read only for -R ports which may be read so the STA may know the mode selected by the -O port. The selected parameters on the -O are sent to the -R link partner on link initialization. For more information on how these parameters are passed across the physical link using G.994.1 signaling, see 61B.3.2.

The bit definitions for the 2B general parameter register are found in Table 45–59.

Table 45–59— 2B general parameter register bit definition

Bit(s)	Name	Description	R/W[a]
1.80.15	Reserved	Value always 0	RO
1.80.14:10	PMMS target margin	margin = 14:10 - 10dB	R/W
1.80.9	Line probing control	1 = use line probing 0 = do not use line probing (default)	R/W
1.80.8	Noise environment	1 = current condition 0 = worst case (default)	R/W
1.80.7:2	Reserved	Value always 0	RO
1.80.1:0	Region	Selects the regional annex to operate under 00 = Annex A 01 = Annex B 10 = Annex C 11 = reserved, writes ignored	O: R/W R: RO

[a]R/W = Read/Write, RO = Read only

45.2.1.61.1 PMMS target margin (1.80.14:10)

The PMMS target margin specified in bits 14:10 specifies the noise margin that the PMMS procedure tries to attain. The margin is expressed in dB as the decimal value of bits 14:10 minus 10 dB. The margin specified is measured either against either worst case or current line conditions, based on the value set in bit 1.80.8.

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The PMMS margin value is transferred during 2BASE-TL initialization via the worst case PMMS margin bits in Table 61B–57 and Table 61B–43, or the current condition PMMS margin bits in Table 61B–48 and Table 61B–44.

45.2.1.61.2 Line probing control (1.80.9)

When set to a one, this bit tells the PMA/PMD to perform line probing the next time link is initialized. When set to a zero, the PMA/PMD does not use line probing. Line probing causes the PMA/PMD to select probe duration and the link data rate. For more information, see the documents referenced in 63.3.

45.2.1.61.3 Noise environment (1.80.8)

This bit controls the reference noise used during line probing. When set to a one, the noise environment is based on the current line conditions. When set to a zero, the noise environment is based on worst case models. For more information, see the documents referenced in 63.3.

45.2.1.61.4 Region (1.80.1:0)

These bits select the regional annex that is used for the operation of the 2BASE-TL PMA/PMD. These annexes refer to clauses in documents referenced by the 2BASE-TL PMA/PMD specification. These are not annexes in IEEE Std 802.3. For details on each annex, see the document referenced in 63.1.3.

45.2.1.62 2B PMD parameters registers (Registers 1.81 through 1.88)

The 2B PMD parameters registers set the transmission parameters for an individual 2BASE-TL PMA/PMD link. When the link is initialized, these parameters are used by the link partner PMA/PMDs in an attempt to achieve specified settings.

These registers allow one to specify a single fixed data rate or up to four data rate ranges at the -O PMA/PMD. An additional set of four data ranges are found in the 2B extended PMD parameters registers (1.102 through 1.109). Bit descriptions for the 2B extended PMD parameters registers are found in 45.2.1.76. Together these sets allow up to eight data rate ranges to be specified.

If at least one data rate range is specified with different Minimum and Maximum data rates, the link is trained with the highest attainable rate. If line probing is enabled, the highest rate is determined by the result of line probing and the “Data rate step” value is ignored. If line probing is disabled, the minimum and maximum rate, “Data rate step” and “Power” values are used to determine the highest attainable rate.

In the case of a single fixed rate specified (Minimum data rate1 equals Maximum data rate1, Data rate step[1:8] set to zero, Minimum/Maximum data rate[2:8] set to zero), the link is trained at the specified rate.

When multiple ranges are specified, the PMD selects the first attainable range, starting sequentially from the first range.

Since writing to this register does not have an immediate effect, reading this register returns the desired parameters, which are not necessarily the current operating parameters.

For more information on how these parameters are passed across the physical link using G.994.1 signaling (see 61B.3.2).

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The bit definitions for the 2B PMD parameters register are found in Table 45–60.

Table 45–60— 2B PMD parameters registers bit definition

Bit(s)	Name	Description	R/W[a]
1.81.15	Reserved	Value always 0	RO
1.81.14:8	Min data rate1	Min data rate of the first range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.81.7	Reserved	Value always 0	RO
1.81.6:0	Max data rate1	Max data rate of the first range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.82.15:14	Reserved	Value always 0	RO
1.82.13:7	Data rate step1	Data rate step of the first range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.82.6:2	Power1	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.82.1:0	Constellation1	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.83.15	Reserved	Value always 0	RO
1.83.14:8	Min data rate2	Min data rate of the second range *n* = value of the bits, *n* valid 3 to 89 Data Rate =64*n* kb/s	O: R/W R: RO
1.83.7	Reserved	Value always 0	RO
1.83.6:0	Max data rate2	Max data rate of the second range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.84.15:14	Reserved	Value always 0	RO
1.84.13:7	Data rate step2	Data rate step of the second range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.84.6:2	Power2	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.84.1:0	Constellation2	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.85.15	Reserved	Value always 0	RO
1.85.14:8	Min data rate3	Min data rate of the third range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.85.7	Reserved	Value always 0	RO

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Table 45–60— 2B PMD parameters registers bit definition *(continued)*

Bit(s)	Name	Description	R/W[a]
1.85.6:0	Max data rate3	Max data rate of the third range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.86.15:14	Reserved	Value always 0	RO
1.86.13:7	Data rate step3	Data rate step of the third range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.86.6:2	Power3	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.86.1:0	Constellation3	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.87.15	Reserved	Value always 0	RO
1.87.14:8	Min data rate4	Min data rate of the fourth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.87.7	Reserved	Value always 0	RO
1.87.6:0	Max data rate4	Max data rate of the fourth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.88.15:14	Reserved	Value always 0	RO
1.88.13:7	Data rate step4	Data rate step of the fourth range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.88.6:2	Power4	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.88.1:0	Constellation4	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO

[a]R/W = Read/Write, RO = Read only

45.2.1.62.1 Minimum data rate (1.81, 1.83, 1.85, 1.87. Bits 14:8)

Bits 14:8 in registers 1.81 through 1.87 set the minimum data rate for each of the four ranges. Valid values for these bits are decimal 3 through 89, writes to set an invalid value shall be ignored. The rate is expressed in units of kb/s and is derived by multiplying the decimal value of bits 14:8 by 64.

45.2.1.62.2 Max data rate (1.81, 1.83, 1.85, 1.87. Bits 6:0)

Bits 6:0 in registers 1.81 through 1.87 set the maximum data rate for each of the four ranges. Valid values for these bits are decimal 3 through 89, writes to set an invalid value shall be ignored. The rate is expressed in units of kb/s and is derived by multiplying the decimal value of bits 6:0 by 64.

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45.2.1.62.3 Data rate step (1.82, 1.84, 1.86, 1.88. Bits 13:7)

Bits 13:7 in registers 1.82 through 1.88 set the granularity used by the PMA/PMD when determining the line rate. Valid values for these bits are decimal 1 through 86, writes to set an invalid value shall be ignored. The data rate step is expressed in units of kb/s and is derived by multiplying the decimal value of bits 13:7 by 64.

45.2.1.62.4 Power (1.82, 1.84, 1.86, 1.88. Bits 6:2)

Bits 6:2 in registers 1.82 through 1.88 set the allowed power level for each data rate range. The power levels set in these bits override those of the annex selected in the 2B general parameter register (1.80). The power level is expressed in units of dBm and is derived by Equation (45–4), where *x* equals the value of bits 6:2.

$$power = \left(5 + \frac{x}{2}\right) \text{ dBm} \tag{45–4}$$

45.2.1.62.5 Constellation (1.82, 1.84, 1.86, 1.88. Bits 1:0)

Bits 1:0 in registers 1.82 through 1.88 set the allowed constellation for each data rate range. Setting a value of 10 or 01 restricts the constellation to 16- or 32-TCPAM respectively. When set to a value of 00, the PMD automatically determines the constellation during initialization. Attempts to set a value of 11 shall be ignored.

45.2.1.63 2B code violation errors counter (Register 1.89)

The 2B code violation errors counter is a 16-bit counter that contains the number of the 2BASE-TL CRC anomalies. See 63.2.2.3 for more information. These bits shall be set to all zeros upon an MMD reset and upon being read.

Bit definitions for the 2B code violation errors counter are found in Table 45–61.

Table 45–61—2B code violation errors counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.89.15:0	Code violations [15:0]	The bytes of the counter	RO

[a]RO = Read only

45.2.1.64 2B link partner code violations register (Register 1.90)

The 2B link partner code violations register provides the -O STA with a snapshot of the -R link partner's 2B code violations counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.30) and the command completes successfully (see 45.2.1.31.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–61.

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45.2.1.65 2B errored seconds counter (Register 1.91)

This 8-bit counter contains the number of errored seconds (see 63.2.2.3) These bits shall be set to all zeros when the register is read by management or upon an MMD reset.

Bit definitions for the 2B errored seconds counter are found in Table 45–62.

Table 45–62—2B errored seconds counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.91.15:8	Reserved	Value always 0	RO
1.91.7:0	Errored seconds [7:0]	The byte of the counter	RO

[a]RO = Read only

45.2.1.66 2B link partner errored seconds register (Register 1.92)

The 2B link partner errored seconds register provides the -O STA with a snapshot of the -R link partner's 2B errored seconds counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.30) and the command completes successfully (see 45.2.1.31.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–62.

45.2.1.67 2B severely errored seconds counter (Register 1.93)

This 8-bit counter contains the number severely errored seconds (see 63.2.2.3). These bits shall be set to all zeros when the register is read by management or upon an MMD reset.

Bit definitions for the 2B severely errored seconds register are found in Table 45–63.

Table 45–63—2B severely errored counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.93.15:8	Reserved	Value always 0	RO
1.93.7:0	Severely errored seconds [7:0]	The byte of the counter	RO

[a]RO = Read only

45.2.1.68 2B link partner severely errored seconds register (Register 1.94)

The 2B link partner severely errored seconds register provides the -O STA with a snapshot of the -R link partner's 2B severely errored seconds counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.30) and the command completes successfully (see 45.2.1.31.1).

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This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–63.

45.2.1.69 2B LOSW counter (Register 1.95)

This 8-bit counter contains the number of loss of sync seconds (see 63.2.2.3). These bits shall be set to all zeros when the register is read by management or upon an MMD reset.

Bit definitions for the 2B LOSW counter are found in Table 45–64.

Table 45–64—2B LOSW counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.95.15:8	Reserved	Value always 0	RO
1.95.7:0	Loss of sync seconds [7:0]	The byte of the counter	RO

[a]RO = Read only

45.2.1.70 2B link partner LOSW register (Register 1.96)

The 2B link partner LOSW register provides the -O STA with a snapshot of the -R link partner's 2B LOSW counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link partner PMA/PMD control register (see 45.2.1.30) and the command completes successfully (see 45.2.1.31.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–64.

45.2.1.71 2B unavailable seconds counter (Register 1.97)

This 8-bit counter contains the number of unavailable seconds (see 63.2.2.3). These bits shall be set to all zeros when the register is read by management or upon an MMD reset.

Bit definitions for the 2B unavailable seconds counter are found in Table 45–65.

Table 45–65—2B unavailable seconds counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.97.15:8	Reserved	Value always 0	RO
1.97.7:0	unavailable seconds [7:0]	The byte of the counter	RO

[a]RO = Read only

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45.2.1.72 2B link partner unavailable seconds register (Register 1.98)

The 2B link partner unavailable seconds register provides the -O STA with a snapshot of the -R link partner's 2B unavailable seconds counter. Because this register is not a counter, its value will be updated only when refreshed. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.30) and the command completes successfully (see 45.2.1.31.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–65.

45.2.1.73 2B state defects register (Register 1.99)

The 2B state defects register is used to communicate defect states from the 2BASE-TL PMD (see 63.2.2.3). The thresholds for these defects are set using the 2B line quality threshold register (see 45.2.1.39). The register bits are cleared to zero when read by the STA or upon MMD reset. On a -R PMA/PMD, these bits are also cleared to zero upon the successful reception of a "Get link partner parameters" command (see 45.2.1.29.1).

Bit definitions for the 2B state defects register are found in Table 45–66.

Table 45–66—2B state defects register bit definitions

Bit(s)	Name	Description	R/W[a]
1.99.15	Segment defect	1 = segment defect detected 0 = normal condition	RO, LH
1.99.14	SNR margin defect	1 = SNR margin defect detected 0 = normal condition	RO, LH
1.99.13	Loop attenuation defect	1 = loop attenuation defect detected 0 = normal condition	RO, LH
1.99.12	Loss of sync word	1 = loss of sync word detected 0 = normal condition	RO, LH
1.99.11:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

45.2.1.73.1 Segment defect (1.99.15)

When read as a one, this bit indicates that the local PMA/PMD has detected a segment defect.

45.2.1.73.2 SNR margin defect (1.99.14)

When read as a one, this bit indicates that the local PMA/PMD has received a signal whose SNR is below the set threshold (see 45.2.1.39).

45.2.1.73.3 Loop attenuation defect (1.99.13)

When read as a one, this bit indicates that the PMA/PMD has detected that the loop attenuation is below the set threshold (see 45.2.1.39).

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45.2.1.73.4 Loss of sync word (1.99.12)

When read as a one, this bit indicates that the PMA/PMD has lost PMA/PMD frame sync.

45.2.1.74 2B link partner state defects register (Register 1.100)

The 2B link partner state defects register provides the -O STA with a snapshot of the -R link partner's 2B state defects register. The contents of this register are refreshed when the STA activates the "Get link partner parameter" command in the Link Partner PMA/PMD control register (see 45.2.1.30) and the command completes successfully (see 45.2.1.31.1).

This register is defined for -O port subtypes only.

The bit definitions for this register are found in Table 45–66.

45.2.1.75 2B negotiated constellation register (Register 1.101)

The bit definitions for this register are shown in Table 45–67.

Table 45–67—2B register bit definition

Bit(s)	Name	Description	R/W[a]
1.101.15:2	Reserved	Value always 0	RO
1.101.1:0	Negotiated constellation	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = undetermined	RO

[a]RO = Read only

45.2.1.75.1 Negotiated constellation (1.101.1:0)

These bits report the resulting constellation that was obtained after initialization. For more information on configuring 2BASE-TL PMA/PMD link initialization, see the 2B PMD parameter registers (see 45.2.1.62). When read as 10 or 01, the constellation has been set as either 16- or 32-TCPAM respectively. When read as 00, the local PMD has not arrived at a constellation with its link partner (as may be the case while link is down or initializing, after reset or upon a failed initialization).

45.2.1.76 2B extended PMD parameters registers (Registers 1.102 through 1.109)

The 2B extended PMD parameters registers define four additional data range sets to be used in conjunction with the 2B PMD parameters registers when additional PMD configuration detail is desired. For a complete description of the use of these registers, see 45.2.1.62.

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Bit definitions for these registers can be found in Table 45–68.

Table 45–68— 2B extended PMD parameters registers bit definition

Bit(s)	Name	Description	R/W[a]
1.102.15	Reserved	Value always 0	RO
1.102.14:8	Min data rate5	Min data rate of the fifth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.102.7	Reserved	Value always 0	RO
1.102.6:0	Max data rate5	Max data rate of the fifth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.103.15:14	Reserved	Value always 0	RO
1.103.13:7	Data rate step5	Data rate step of the fifth range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.103.6:2	Power5	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.103.1:0	Constellation5	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.104.15	Reserved	Value always 0	RO
1.104.14:8	Min data rate6	Min data rate of the sixth range *n* = value of the bits, *n* valid 3 to 89 Data Rate =64*n* kb/s	O: R/W R: RO
1.104.7	Reserved	Value always 0	RO
1.104.6:0	Max data rate6	Max data rate of the sixth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.105.15:14	Reserved	Value always 0	RO
1.105.13:7	Data rate step6	Data rate step of the sixth range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.105.6:2	Power6	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.105.1:0	Constellation6	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.106.15	Reserved	Value always 0	RO
1.106.14:8	Min data rate7	Min data rate of the seventh range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.106.7	Reserved	Value always 0	RO

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Table 45–68— 2B extended PMD parameters registers bit definition *(continued)*

Bit(s)	Name	Description	R/W[a]
1.106.6:0	Max data rate7	Max data rate of the seventh range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.107.15:14	Reserved	Value always 0	RO
1.107.13:7	Data rate step7	Data rate step of the seventh range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.107.6:2	Power7	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.107.1:0	Constellation7	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO
1.108.15	Reserved	Value always 0	RO
1.108.14:8	Min data rate8	Min data rate of the eighth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.108.7	Reserved	Value always 0	RO
1.108.6:0	Max data rate8	Max data rate of the eighth range *n* = value of the bits, *n* valid 3 to 89 Data Rate = 64*n* kb/s	O: R/W R: RO
1.109.15:14	Reserved	Value always 0	RO
1.109.13:7	Data rate step8	Data rate step of the eighth range *n* = value of the bits, *n* valid 1 to 86 Data Rate = 64*n* kb/s	O: R/W R: RO
1.109.6:2	Power8	*x* = multiple of 0.5 dBm to add to 5 dBm offset Power = (5 + 0.5*x*) dBm	O: R/W R: RO
1.109.1:0	Constellation8	11 = reserved 10 = 16-TCPAM 01 = 32-TCPAM 00 = automatically set by the PHY	O: R/W R: RO

[a]R/W = Read/Write, RO = Read only

45.2.1.76.1 Minimum data rate (1.102, 1.104, 1.106, 1.108. Bits 14:8)

Bits 14:8 in registers 1.102, 1.104, 1.106, and 1.108 set the minimum data rate for each of the four extended ranges. Valid values for these bits are decimal 3 through 89. writes to set an invalid value shall be ignored. The rate is expressed in units of kb/s and is derived by multiplying the decimal value of bits 14:8 by 64.

45.2.1.76.2 Max data rate (1.102, 1.104, 1.106, 1.108. Bits 6:0)

Bits 6:0 in registers 1.102, 1.104, 1.106, and 1.108 set the maximum data rate for each of the four extended ranges. Valid values for these bits are decimal 3 through 89, writes to set an invalid value shall be ignored. The rate is expressed in units of kb/s and is derived by multiplying the decimal value of bits 6:0 by 64.

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45.2.1.76.3 Data rate step (1.103, 1.105, 1.107, 1.109. Bits 13:7)

Bits 13:7 in registers 1.103, 1.105, 1.107 and 1.109 set the granularity used by the PMA/PMD when determining the line rate. Valid values for these bits are decimal 1 through 86, writes to set an invalid value shall be ignored. The data rate step is expressed in units of kb/s and is derived by multiplying the decimal value of bits 13:7 by 64.

45.2.1.76.4 Power (1.103, 1.105, 1.107, 1.109. Bits 6:2)

Bits 6:2 in registers 1.103, 1.105, 1.107 and 1.109 set the allowed power level for each extended data rate range. The power levels set in these bits override those of the annex selected in the 2B general parameter register (1.80). The power level is expressed in units of dBm and is derived by Equation (45–5), where *x* equals the value of bits 6:2.

$$\text{power} = \left(5 + \frac{x}{2}\right) \text{ dBm} \tag{45–5}$$

45.2.1.76.5 Constellation (1.103, 1.105, 1.107, 1.109. Bits 1:0)

Bits 1:0 in registers 1.103, 1.105, 1.107 and 1.109 set the allowed constellation for each extended data rate range. Setting a value of 10 or 01 restricts the constellation to 16- or 32-TCPAM respectively. When set to a value of 00, the PMD automatically determines the constellation during initialization. Attempts to set a value of 11 shall be ignored.

45.2.1.77 MultiGBASE-T status (Register 1.129)

The assignment of bits in the MultiGBASE-T status register is shown in Table 45–69.

Table 45–69—MultiGBASE-T status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.129.15:1	Reserved	Value always 0	RO
1.129.0	LP information valid	1 = Link partner information is valid 0 = Link partner information is invalid	RO

[a]RO = Read only

45.2.1.77.1 LP information valid (1.129.0)

When read as a one, bit 1.129.0 indicates that the startup protocol defined in 55.4.2.5 (for 10GBASE-T), 113.4.2.5 (for 25G/40GBASE-T), or 126.4.2.5 (for 2.5G/5GBASE-T) has been completed, and that the contents of bits 1.130.11:0, 1.131.15:10, 1.145.14:8, 1.146.14:8, and 1.146.6:0, which are established during the startup protocol, are valid. When read as a zero, bit 1.129.0 indicates that the startup process has not been completed, and that the contents of these bits that are established during the startup protocol are invalid. A PMA in the MultiGBASE-T set shall return a value of zero in bit 1.129.0 if PMA link_status=FAIL.

45.2.1.78 MultiGBASE-T pair swap and polarity register (Register 1.130)

Register 1.130 reflects the status of the pair-to-pair connectivity between the local device and the link partner (see Table 45–70). The polarity of each individual pair is also indicated.

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Table 45–70—MultiGBASE-T pair swap and polarity register bit definitions

Bit(s)	Name	Description	R/W[a]
1.130.15:12	Reserved	Value always 0	RO
1.130.11	Pair D polarity	1 = Polarity of pair D is reversed 0 = Polarity of pair D is not reversed	RO
1.130.10	Pair C polarity	1 = Polarity of pair C is reversed 0 = Polarity of pair C is not reversed	RO
1.130.9	Pair B polarity	1 = Polarity of pair B is reversed 0 = Polarity of pair B is not reversed	RO
1.130.8	Pair A polarity	1 = Polarity of pair A is reversed 0 = Polarity of pair A is not reversed	RO
1.130.7:2	Reserved	Value always 0	RO
1.130.1:0	MDI/MDI-X connection	1 0 1 1 = No crossover 1 0 = Reserved 0 1 = Reserved 0 0 = Pair A/B and pair C/D crossover	RO

[a]RO = Read only

45.2.1.78.1 Pair D polarity (1.130.11)

When read as zero, bit 1.130.11 indicates that the polarity within pair D is not reversed. When read as one, bit 1.130.11 indicates that the polarity of pair D is reversed.

45.2.1.78.2 Pair C polarity (1.130.10)

When read as zero, bit 1.130.10 indicates that the polarity within pair C is not reversed. When read as one, bit 1.130.10 indicates that the polarity of pair C is reversed.

45.2.1.78.3 Pair B polarity (1.130.9)

When read as zero, bit 1.130.9 indicates that the polarity within pair B is not reversed. When read as one, bit 1.130.9 indicates that the polarity of pair B is reversed.

45.2.1.78.4 Pair A polarity (1.130.8)

When read as zero, bit 1.130.8 indicates that the polarity within pair A is not reversed. When read as one, bit 1.130.8 indicates that the polarity of pair A is reversed.

45.2.1.78.5 MDI/MDI-X connection (1.130.1:0)

Bits 1.130.1:0 indicate the resolution of the automatic MDI/MDI-X configuration defined in 55.4.4. This function is intended to eliminate the need for crossover cables between similar devices. The automatic configuration method used shall comply with 40.4.4.1 and 40.4.4.2.

45.2.1.79 MultiGBASE-T TX power backoff and PHY short reach setting (Register 1.131)

The complete assignment of bits in the MultiGBASE-T TX power backoff and short reach mode settings register is shown in Table 45–71.

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Table 45–71—MultiGBASE-T TX power backoff and PHY short reach setting register bit definitions

Bit(s)	Name	Description	R/W[a]
1.131.15:13	Link partner TX power backoff setting	15 14 13 1 1 1 = 14 dB 1 1 0 = 12 dB 1 0 1 = 10 dB 1 0 0 = 8 dB 0 1 1 = 6 dB 0 1 0 = 4 dB 0 0 1 = 2 dB 0 0 0 = 0 dB	RO
1.131.12:10	TX power backoff setting	12 11 10 1 1 1 = 14 dB 1 1 0 = 12 dB 1 0 1 = 10 dB 1 0 0 = 8 dB 0 1 1 = 6 dB 0 1 0 = 4 dB 0 0 1 = 2 dB 0 0 0 = 0 dB	RO
1.131.9:1	Reserved	Value always 0	RO
1.131.0	Short reach mode	1 = PHY is operating in short reach mode 0 = PHY is not operating in short reach mode	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.79.1 MultiGBASE-T TX power backoff settings (1.131.15:10)

The MultiGBASE-T TX power backoff settings reflects the TX power backoff selected during the startup negotiation process. The 10GBASE-T startup negotiation process and all TX power backoff settings are defined in 55.4.2.5 and 55.4.5.1. The 25GBASE-T and 40GBASE-T startup negotiation process and all TX power backoff settings are defined in 113.4.2.5 and 113.4.5.1. For 2.5GBASE-T and 5GBASE-T, startup negotiation process and all TX power backoff settings are defined in 126.4.2.5 and 126.4.5.1. If LP information valid bit, 1.129.0, is set to one then bits 1.131.15:13 indicates the TX power backoff setting of the link partner and bits 1.131.12:10 indicates the TX power backoff setting of the local device.

45.2.1.79.2 PHY short reach mode (1.131.0)

The short reach mode of the 10GBASE-T PHY provides a means for operation on a cable plant that has parametric performance equivalent to 30 m of Class F and Class E_A cabling as defined in 55.5.4.5. The short reach mode of the 25GBASE-T and 40GBASE-T PHYs provides for operation on a direct attach link segment that has parametric performance defined in 113.7.4. Setting bit 1.131.0 to a one puts the PHY in short reach mode, and setting bit 1.131.0 to a zero puts the PHY into normal (non-short reach) mode. The default value for this bit is zero.

45.2.1.80 MultiGBASE-T test mode register (Register 1.132)

The assignment of bits in the MultiGBASE-T test mode register is shown in Table 45–72. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

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Table 45–72—MultiGBASE-T test mode register bit definitions

Bit(s)	Name	Description	R/W[a]
1.132.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal operation	R/W
1.132.12:10	Transmitter test frequencies	12 11 10 1 1 1 = Reserved 1 1 0 = Dual tone 5 1 0 1 = Dual tone 4 1 0 0 = Dual tone 3 0 1 1 = Reserved 0 1 0 = Dual tone 2 0 0 1 = Dual tone 1 0 0 0 = Reserved	R/W
1.132.9:0	Reserved	Value always 0	RO

[a]R/W = Read/Write, RO = Read only

45.2.1.80.1 Test mode control (1.132.15:13)

Transmitter test mode operations defined by bits 1.132.15:13 are described for 10GBASE-T in 55.5.2 and Table 55–12, for 2.5G/5GBASE-T in 126.5.2 and Table 126–13, and for 25G/40GBASE-T in 113.5.2 and Table 113–16. The default value for bits 1.132.15:13 is zero.

45.2.1.80.2 Transmitter test frequencies (1.132.12:10)

When test mode 4 is selected by setting bits 1.132.15:13 to one, zero, zero respectively, bits 1.132.12:10 select the transmit test frequency as shown in Table 45–72. Detailed use and operation of these transmitter test frequencies is described in 55.5.2, 113.5.2, and 126.5.2.

45.2.1.81 SNR operating margin channel A register (Register 1.133)

Register 1.133 contains the current SNR operating margin measured at the slicer input for channel A for the PMAs in the MultiGBASE-T set. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.82 SNR operating margin channel B register (Register 1.134)

Register 1.134 contains the current SNR operating margin measured at the slicer input for channel B for the PMAs in the MultiGBASE-T set. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

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45.2.1.83 SNR operating margin channel C register (Register 1.135)

Register 1.135 contains the current SNR operating margin measured at the slicer input for channel C for the PMAs in the MultiGBASE-T set. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.84 SNR operating margin channel D register (Register 1.136)

Register 1.136 contains the current SNR operating margin measured at the slicer input for channel D for the PMAs in the MultiGBASE-T set. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.85 Minimum margin channel A register (Register 1.137)

The Minimum margin channel A register contains a latched copy of the lowest value observed in the SNR operating margin channel A register (1.133) since the last read. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.86 Minimum margin channel B register (Register 1.138)

The Minimum margin channel B register contains a latched copy of the lowest value observed in the SNR operating margin channel B register (1.134) since the last read. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.87 Minimum margin channel C register (Register 1.139)

The Minimum margin channel C register contains a latched copy of the lowest value observed in the SNR operating margin channel C register (1.135) since the last read. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.88 Minimum margin channel D register (Register 1.140)

The Minimum margin channel D register contains a latched copy of the lowest value observed in the SNR operating margin channel D register (1.136) since the last read. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.89 RX signal power channel A register (Register 1.141)

The RX signal power channel A register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1, 113.4.3.1, and 126.4.3.1. The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or PMA_Training_Init_S (as appropriate, see 55.4.6.1, 113.4.6.1, and 126.4.6.1), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset binary notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

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45.2.1.90 RX signal power channel B register (Register 1.142)

The RX signal power channel B register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1, 113.4.3.1, and 126.4.3.1. The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or PMA_Training_Init_S (as appropriate, see 55.4.6.1, 113.4.6.1, and 126.4.6.1), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset binary notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.91 RX signal power channel C register (Register 1.143)

The RX signal power channel C register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1, 113.4.3.1, and 126.4.3.1. The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or PMA_Training_Init_S (as appropriate, see 55.4.6.1, 113.4.6.1, and 126.4.6.1), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset binary notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.92 RX signal power channel D register (Register 1.144)

The RX signal power channel D register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1, 113.4.3.1, and 126.4.3.1. The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or PMA_Training_Init_S (as appropriate, see 55.4.6.1, 113.4.6.1, and 126.4.6.1), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset binary notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.93 MultiGBASE-T skew delay register (Registers 1.145 and 1.146)

The skew delay register reports the current skew delay on each of the pair with respect to physical pair A (see Table 45–73). It is reported with resolution equal to one symbol period (see 55.1.3, 113.1.3, and 126.1.3) of the PHY (e.g., 1.25 ns for 10GBASE-T) to an accuracy of two symbol periods (e.g., 2.5 ns for 10GBASE-T). The number reported is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceeds the maximum amount that can be represented by the range (–64 symbols to +63 symbols), the field displays the maximum respective value. The value shall be updated at least once per second.

Table 45–73—MultiGBASE-T skew delay register bit definitions

Bit(s)	Name	Description	R/W[a]
1.145.15	Reserved	Value always 0	RO
1.145.14:8	Skew delay B	Skew delay for pair B	RO
1.145.7:0	Reserved	Value always 0	RO
1.146.15	Reserved	Value always 0	RO
1.146.14:8	Skew delay D	Skew delay for pair D	RO

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Table 45–73—MultiGBASE-T skew delay register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.146.7	Reserved	Value always 0	RO
1.146.6:0	Skew delay C	Skew delay for pair C	RO

[a]RO = Read only

45.2.1.94 MultiGBASE-T fast retrain status and control register (Register 1.147)

The assignment of bits in the MultiGBASE-T fast retrain status and control register is shown in Table 45–74.

Table 45–74—MultiGBASE-T fast retrain status and control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.147.15:11	LP fast retrain count	Counts the number of fast retrains requested by the link partner	RO/NR
1.147.10:6	LD fast retrain count	Counts the number of fast retrains requested by the local device	RO/NR
1.147.5	Reserved	Value always 0	RO
1.147.4	Fast retrain ability	1 = Fast retrain capability is supported 0 = Fast retrain capability is not supported	RO
1.147.3	Fast retrain negotiated	1 = Fast retrain capability was negotiated 0 = Fast retrain capability was not negotiated	RO
1.147.2:1	Fast retrain signal type	11 = Reserved 10 = PHY signals Link Interruption during fast retrain 01 = PHY signals Local Fault during fast retrain 00 = PHY signals IDLE during fast retrain	R/W
1.147.0	Fast retrain enable	1 = Fast retrain capability is enabled 0 = Fast retrain capability is disabled	R/W

[a] RO = Read only, R/W = Read/Write, NR = Non Roll-over

45.2.1.94.1 LP fast retrain count (1.147.15:11)

These bits map to fr_rx_counter as defined in 55.4.5.4 for 10GBASE-T, 113.4.5.4 for 25GBASE-T and 40GBASE-T, and 126.4.5.4 for 2.5GBASE-T and 5GBASE-T. The counter is a 5-bit count of the number of fast retrains requested by the link partner. These bits shall be reset to all zeros when read or upon execution of the PMA reset. These bits shall be held at all ones in the case of overflow.

45.2.1.94.2 LD fast retrain count (1.147.10:6)

These bits map to fr_tx_counter as defined in 55.4.5.4 for 10GBASE-T, 113.4.5.4 for 25GBASE-T and 40GBASE-T, and 126.4.5.4 for 2.5GBASE-T and 5GBASE-T. The counter is a 5-bit count of the number of fast retrains requested by the local device. These bits shall be reset to all zeros when read or upon execution of the PMA reset. These bits shall be held at all ones in the case of overflow.

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45.2.1.94.3 Fast retrain ability (1.147.4)

When read as a one, bit 1.147.4 indicates that the PHY supports fast retrain, as defined in 55.4.2.5.15. When read as a zero, bit 1.147.4 indicates that the PHY does not support fast retrain.

45.2.1.94.4 Fast retrain negotiated (1.147.3)

When read as a one, bit 1.147.3 indicates that the PHY negotiated fast retrain, as defined in 55.4.2.5.15 during the most recent auto-negotiation. This is the condition where both the local device indicated fast retrain ability (bit 7.32.1 is one) and the link partner indicated fast retrain ability (bit 7.33.1 is one). When read as a zero, bit 1.147.3 indicates that the PHY did not negotiate fast retrain. See 45.2.7.10.14.

45.2.1.94.5 Fast retrain signal type (1.147.2:1)

For PHYs that support fast retrain, these bits map to fr_sigtype as defined in 55.3.6.2.2, 113.3.6.2.2, and 126.3.6.2.2. When Fast retrain signal type is set to 00, the PMA sends IDLE characters on the receive path during fast retrain. When Fast retrain signal type is set to 01, the PMA sends Local Fault on the receive path during fast retrain. When Fast retrain signal type is set to 10, the PMA sends Link Interruption on the receive path during fast retrain.

45.2.1.94.6 Fast retrain enable (1.147.0)

For PHYs that support fast retrain, bit 1.147.0 controls fr_enable as defined in 55.4.5.1, 113.4.5.1, and 126.4.5.1. When PMA reset is executed, this bit is set to one.

NOTE—Setting this bit to zero while a link is up will cause the PHY to stop supporting fast retrain, and the link will drop if the link partner initiates a fast retrain.

45.2.1.95 BASE-R PMD control register (Register 1.150)

The BASE-R PMD control register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, Clause 85, Clause 92, Clause 93, Clause 94, Clause 110, Clause 111, Clause 136, or Clause 137.

The BASE-R PMD control register is also used by 5GBASE-KR described in Clause 130 to disable the transmitter equalizer for test purposes. 5GBASE-KR does not use the startup protocol.

The assignment of bits in the BASE-R PMD control register is shown in Table 45–75.

Table 45–75—BASE-R PMD control register

Bit(s)	Name	Description	R/W[a]
1.150.15:3	Reserved	Value always 0	RO
1.150.2	Transmitter equalizer disable	1 = Disable the 5GBASE-KR transmitter equalizer 0 = Normal operation	R/W
1.150.1	Training enable	1 = Enable the BASE-R startup protocol 0 = Disable the BASE-R startup protocol	R/W
1.150.0	Restart training	1 = Restart BASE-R startup protocol 0 = Normal operation	R/W SC

[a]R/W = Read/Write, SC = Self-clearing, RO = Read only

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45.2.1.95.1 Restart training (1.150.0)

This bit maps to the state variable mr_restart_training as defined in 72.6.10.3.1.

45.2.1.95.2 Training enable (1.150.1)

This bit maps to the state variable mr_training_enable as defined in 72.6.10.3.1.

45.2.1.95.3 Transmitter equalizer disable (1.150.2)

When bit 1.150.2 is set to one, 5GBASE-KR transmitter equalization is disabled. The default value of bit 1.150.2 is zero.

45.2.1.96 BASE-R PMD status register (Register 1.151)

The BASE-R PMD status register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, Clause 85, Clause 92, Clause 93, Clause 94, Clause 110, Clause 111, Clause 136, or Clause 137. The assignment of bits in the BASE-R PMD status register is shown in Table 45–76.

Table 45–76—BASE-R PMD status register

Bit(s)	Name	Description	R/W[a]
1.151.15	Training failure 3	1 = Training failure has been detected for lane 3 0 = Training failure has not been detected for lane 3	RO
1.151.14	Startup protocol status 3	1 = Startup protocol in progress for lane 3 0 = Startup protocol complete for lane 3	RO
1.151.13	Frame lock 3	1 = Training frame delineation detected for lane 3 0 = Training frame delineation not detected for lane 3	RO
1.151.12	Receiver status 3	1 = Receiver trained and ready to receive data for lane 3 0 = Receiver training for lane 3	RO
1.151.11	Training failure 2	1 = Training failure has been detected for lane 2 0 = Training failure has not been detected for lane 2	RO
1.151.10	Startup protocol status 2	1 = Startup protocol in progress for lane 2 0 = Startup protocol complete for lane 2	RO
1.151.9	Frame lock 2	1 = Training frame delineation detected for lane 2 0 = Training frame delineation not detected for lane 2	RO
1.151.8	Receiver status 2	1 = Receiver trained and ready to receive data for lane 2 0 = Receiver training for lane 2	RO
1.151.7	Training failure 1	1 = Training failure has been detected for lane 1 0 = Training failure has not been detected for lane 1	RO
1.151.6	Startup protocol status 1	1 = Startup protocol in progress for lane 1 0 = Startup protocol complete for lane 1	RO
1.151.5	Frame lock 1	1 = Training frame delineation detected for lane 1 0 = Training frame delineation not detected for lane 1	RO
1.151.4	Receiver status 1	1 = Receiver trained and ready to receive data for lane 1 0 = Receiver training for lane 1	RO
1.151.3	Training failure 0	1 = Training failure has been detected for lane 0 0 = Training failure has not been detected for lane 0	RO

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Table 45–76—BASE-R PMD status register *(continued)*

Bit(s)	Name	Description	R/W[a]
1.151.2	Startup protocol status 0	1 = Startup protocol in progress for lane 0 0 = Startup protocol complete for lane 0	RO
1.151.1	Frame lock 0	1 = Training frame delineation detected for lane 0 0 = Training frame delineation not detected for lane 0	RO
1.151.0	Receiver status 0	1 = Receiver trained and ready to receive data for lane 0 0 = Receiver training for lane 0	RO

[a]RO = Read only

45.2.1.96.1 Receiver status 0 (1.151.0)

This bit maps to the state variable rx_trained as defined in 72.6.10.3.1 and local_trained in 136.8.11.7.1.

45.2.1.96.2 Frame lock 0 (1.151.1)

This bit maps to the state variable frame_lock as defined in 72.6.10.3.1 and local_tf_lock in 136.8.11.7.1.

45.2.1.96.3 Startup protocol status 0 (1.151.2)

This bit maps to the state variable training as defined in 72.6.10.3.1 and 136.8.11.7.1.

45.2.1.96.4 Training failure 0 (1.151.3)

This bit maps to the state variable training_failure as defined in 72.6.10.3.1 and 136.8.11.7.1.

45.2.1.96.5 Receiver status 1, 2, 3 (1.151.4, 1.151.8, 1.151.12)

These bits are defined identically to 1.151.0 for lanes 1, 2, and 3 respectively.

45.2.1.96.6 Frame lock 1, 2, 3 (1.151.5, 1.151.9, 1.151.13)

These bits are defined identically to 1.151.1 for lanes 1, 2, and 3 respectively.

45.2.1.96.7 Startup protocol status 1, 2, 3 (1.151.6, 1.151.10, 1.151.14)

These bits are defined identically to 1.151.2 for lanes 1, 2, and 3 respectively.

45.2.1.96.8 Training failure 1, 2, 3 (1.151.7, 1.151.11, 1.151.15)

These bits are defined identically to 1.151.3 for lanes 1, 2, and 3 respectively.

45.2.1.97 BASE-R LP coefficient update, lane 0 register (Register 1.152)

The BASE-R LP coefficient update, lane 0 register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, Clause 85, Clause 92, Clause 93, Clause 94, Clause 110, or Clause 111. The BASE-R LP coefficient update, lane 0 register reflects the contents of the first 16-bit word of the training frame most recently received from the control channel for lane 0 or for a single-lane PHY.

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The assignment of bits in the BASE-R LP coefficient update, lane 0 register is shown in Table 45–77. Normally the bits in this register are read only; however, when training is disabled by setting low bit 1 in the BASE-R PMD control register, the BASE-R LP coefficient update, lane 0 register becomes writeable.

A copy of this register may be implemented at address 1.1100 to assist PHY access for devices using post-read-increment-address access for a multi-lane PCS. If implemented, all accesses to the copy have identical behavior as accesses to the original register.

Table 45–77—BASE-R LP coefficient update, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.152.15:14	Reserved	Value always 0	RO
1.152.13	Preset	1 = Preset coefficients 0 = Normal operation	R/W
1.152.12	Initialize	1 = Initialize coefficients 0 = Normal operation	R/W
1.152.11:6	Reserved	Value always 0	RO
1.152.5:4	Coefficient (+1) update	5 4 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	R/W
1.152.3:2	Coefficient (0) update	3 2 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	R/W
1.152.1:0	Coefficient (–1) update	1 0 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.97.1 Preset (1.152.13)

The preset control bit requests that the coefficients be set to a state where equalization is turned off. The function and values of the preset bit is defined in 72.6.10.2.3.1.

45.2.1.97.2 Initialize (1.152.12)

The initialize control is sent to request that the coefficients be set to configure the transmit equalizer to its INITIALIZE state. The function and values of the initialize bit is defined in 72.6.10.2.3.2.

45.2.1.97.3 Coefficient (k) update (1.152.5:0)

Each coefficient, k, is assigned a 2-bit field describing a requested update. Three request encodings are defined: increment, decrement, and hold. The valid range for k is –1 to +1 where k = 0 denotes the main, or gain, tap. The function and values of the coefficient (k) update bits are defined in 72.6.10.2.3.3.

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45.2.1.98 BASE-R LP status report, lane 0 register (Register 1.153)

The BASE-R LP status report, lane 0 register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, Clause 85, Clause 92, Clause 93, Clause 94, Clause 110, or Clause 111. The BASE-R LP status report, lane 0 register reflects the contents of the second 16-bit word of the training frame most recently received from the control channel for lane 0 or for a single-lane PHY

The assignment of bits in the BASE-R LP status report, lane 0 register is shown in Table 45–78.

A copy of this register may be implemented at address 1.1200 to assist PHY access for devices using post-read-increment-address access for a multi-lane PCS. If implemented, all accesses to the copy have identical behavior as the original register.

Table 45–78—BASE-R LP status report, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.153.15	Receiver ready	1 = The LP receiver has determined that training is complete and is prepared to receive data 0 = The LP receiver is requesting that training continue	RO
1.153.14:6	Reserved	Value always 0	RO
1.153.5:4	Coefficient (+1) status	5 4 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.153.3:2	Coefficient (0) status	3 2 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.153.1:0	Coefficient (–1) status	1 0 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO

[a]RO = Read only

45.2.1.98.1 Receiver ready (1.153.15)

The function and values for the receiver ready bit are defined in 72.6.10.2.4.4.

45.2.1.98.2 Coefficient (k) status (1.153.5:0)

The function and values for the coefficient status bits are defined in 72.6.10.2.4.5.

45.2.1.99 BASE-R LD coefficient update, lane 0 register (Register 1.154)

The BASE-R LD coefficient update, lane 0 register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, Clause 85, Clause 92, Clause 93, Clause 94, Clause 110, or Clause 111. The BASE-R LD coefficient update, lane 0 register reflects the contents of the first 16-bit word

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of the outgoing training frame as defined by the LD receiver adaptation process in 72.6.10.2.5 for lane 0 or for a single-lane PHY.

The assignment of bits in the BASE-R LD coefficient update, lane 0 register is shown in Table 45–79.

A copy of this register may be implemented at address 1.1300 to assist PHY access for devices using post-read-increment-address access for a multi-lane PCS. If implemented, all accesses to the copy have identical behavior as the original register.

Table 45–79—BASE-R LD coefficient update, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.154.15:14	Reserved	Value always 0	RO
1.154.13	Preset	1 = Preset coefficients 0 = Normal operation	RO
1.154.12	Initialize	1 = Initialize coefficients 0 = Normal operation	RO
1.154.11:6	Reserved	Value always 0	RO
1.154.5:4	Coefficient (+1) update	5 4 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	RO
1.154.3:2	Coefficient (0) update	3 2 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	RO
1.154.1:0	Coefficient (–1) update	1 0 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	RO

[a]RO = Read only

45.2.1.99.1 Preset (1.154.13)

The function and values of the preset bit is defined in 72.6.10.2.3.1.

45.2.1.99.2 Initialize (1.154.12)

The function and values of the initialize bit is defined in 72.6.10.2.3.2.

45.2.1.99.3 Coefficient (k) update(1.154.5:0)

The function and values of the coefficient (k) update bits are defined in 72.6.10.2.3.3.

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45.2.1.100 BASE-R LD status report, lane 0 register (Register 1.155)

The BASE-R LD status report, lane 0 register is used for 10GBASE-KR and other PHY types using the PMDs described in Clause 72, Clause 84, Clause 85, Clause 92, Clause 93, Clause 94, Clause 110, or Clause 111. The BASE-R LD status report, lane 0 register reflects the contents of the second 16-bit word of the current outgoing training frame, as defined in the training state diagram in Figure 72–5 for lane 0 or for a single-lane PHY.

The assignment of bits in the BASE-R LD status report, lane 0 register is shown in Table 45–80.

A copy of this register may be implemented at address 1.1400 to assist PHY access for devices using post-read-increment-address access for a multi-lane PCS. If implemented, all accesses to the copy have identical behavior as the original register.

Table 45–80—BASE-R LD status report, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.155.15	Receiver ready	1 = The LD receiver has determined that training is complete and is prepared to receive data 0 = The LD receiver is requesting that training continue	RO
1.155.14:6	Reserved	Value always 0	RO
1.155.5:4	Coefficient (+1) status	5 4 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.155.3:2	Coefficient (0) status	3 2 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.155.1:0	Coefficient (–1) status	1 0 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO

[a]RO = Read only

45.2.1.100.1 Receiver ready (1.155.15)

The function and values for the receiver ready bit are defined in 72.6.10.2.4.4.

45.2.1.100.2 Coefficient (k) status (1.155.5:0)

The function and values for the coefficient status bits are defined in 72.6.10.2.4.5.

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45.2.1.101 BASE-R PMD status 2 register (Register 1.156)

The BASE-R PMD status 2 register is used for 100GBASE-CR10 and other PHY types using the PMDs described in Clause 72, Clause 84, or Clause 85 over more than 4 lanes. The assignment of bits in the BASE-R PMD status 2 register is shown in Table 45–81.

Table 45–81—BASE-R PMD status 2 register

Bit(s)	Name	Description	R/W[a]
1.156.15	Training failure 7	1 = Training failure has been detected for lane 7 0 = Training failure has not been detected for lane 7	RO
1.156.14	Startup protocol status 7	1 = Startup protocol in progress for lane 7 0 = Startup protocol complete for lane 7	RO
1.156.13	Frame lock 7	1 = Training frame delineation detected for lane 7 0 = Training frame delineation not detected for lane 7	RO
1.156.12	Receiver status 7	1 = Receiver trained and ready to receive data for lane 7 0 = Receiver training for lane 7	RO
1.156.11	Training failure 6	1 = Training failure has been detected for lane 6 0 = Training failure has not been detected for lane 6	RO
1.156.10	Startup protocol status 6	1 = Startup protocol in progress for lane 6 0 = Startup protocol complete for lane 6	RO
1.156.9	Frame lock 6	1 = Training frame delineation detected for lane 6 0 = Training frame delineation not detected for lane 6	RO
1.156.8	Receiver status 6	1 = Receiver trained and ready to receive data for lane 6 0 = Receiver training for lane 6	RO
1.156.7	Training failure 5	1 = Training failure has been detected for lane 5 0 = Training failure has not been detected for lane 5	RO
1.156.6	Startup protocol status 5	1 = Startup protocol in progress for lane 5 0 = Startup protocol complete for lane 5	RO
1.156.5	Frame lock 5	1 = Training frame delineation detected for lane 5 0 = Training frame delineation not detected for lane 5	RO
1.156.4	Receiver status 5	1 = Receiver trained and ready to receive data for lane 5 0 = Receiver training for lane 5	RO
1.156.3	Training failure 4	1 = Training failure has been detected for lane 4 0 = Training failure has not been detected for lane 4	RO
1.156.2	Startup protocol status 4	1 = Startup protocol in progress for lane 4 0 = Startup protocol complete for lane 4	RO
1.156.1	Frame lock 4	1 = Training frame delineation detected for lane 4 0 = Training frame delineation not detected for lane 4	RO
1.156.0	Receiver status 4	1 = Receiver trained and ready to receive data for lane 4 0 = Receiver training for lane 4	RO

[a]RO = Read only

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45.2.1.101.1 Receiver status 4, 5, 6, 7 (1.156.0, 1.156.4, 1.156.8, 1.156.12)

These bits are defined identically to 1.151.0 for lanes 4, 5, 6, and 7 respectively.

45.2.1.101.2 Frame lock 4, 5, 6, 7 (1.156.1, 1.156.5, 1.156.9, 1.156.13)

These bits are defined identically to 1.151.1 for lanes 4, 5, 6, and 7 respectively.

45.2.1.101.3 Startup protocol status 4, 5, 6, 7 (1.156.2, 1.156.6, 1.156.10, 1.156.14)

These bits are defined identically to 1.151.2 for lanes 4, 5, 6, and 7 respectively.

45.2.1.101.4 Training failure 4, 5, 6, 7 (1.156.3, 1.156.7, 1.156.11, 1.156.15)

These bits are defined identically to 1.151.3 for lanes 4, 5, 6, and 7 respectively.

45.2.1.102 BASE-R PMD status 3 register (Register 1.157)

The BASE-R PMD status 3 register is used for 100GBASE-CR10 and other PHY types using the PMDs described in Clause 72, Clause 84, or Clause 85 over more than 8 lanes. The assignment of bits in the BASE-R PMD status 3 register is shown in Table 45–82.

Table 45–82—BASE-R PMD status 3 register

Bit(s)	Name	Description	R/W[a]
1.157.15:8	Reserved	Value always 0	RO
1.157.7	Training failure 9	1 = Training failure has been detected for lane 9 0 = Training failure has not been detected for lane 9	RO
1.157.6	Startup protocol status 9	1 = Startup protocol in progress for lane 9 0 = Startup protocol complete for lane 9	RO
1.157.5	Frame lock 9	1 = Training frame delineation detected for lane 9 0 = Training frame delineation not detected for lane 9	RO
1.157.4	Receiver status 9	1 = Receiver trained and ready to receive data for lane 9 0 = Receiver training for lane 9	RO
1.157.3	Training failure 8	1 = Training failure has been detected for lane 8 0 = Training failure has not been detected for lane 8	RO
1.157.2	Startup protocol status 8	1 = Startup protocol in progress for lane 8 0 = Startup protocol complete for lane 8	RO
1.157.1	Frame lock 8	1 = Training frame delineation detected for lane 8 0 = Training frame delineation not detected for lane 8	RO
1.157.0	Receiver status 8	1 = Receiver trained and ready to receive data for lane 8 0 = Receiver training for lane 8	RO

[a]RO = Read only

45.2.1.102.1 Receiver status 8, 9 (1.157.0, 1.157.4)

These bits are defined identically to 1.151.0 for lanes 8 and 9 respectively.

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45.2.1.102.2 Frame lock 8, 9 (1.157.1, 1.157.5)

These bits are defined identically to 1.151.1 for lanes 8 and 9 respectively.

45.2.1.102.3 Startup protocol status 8, 9 (1.157.2, 1.157.6)

These bits are defined identically to 1.151.2 for lanes 8 and 9 respectively.

45.2.1.102.4 Training failure 8, 9 (1.157.3, 1.157.7)

These bits are defined identically to 1.151.3 for lanes 8 and 9 respectively.

45.2.1.103 1000BASE-KX/2.5GBASE-KX control register (Register 1.160)

The assignment of bits in the 1000BASE-KX/2.5GBASE-KX control register is shown in Table 45–83.

Table 45–83—1000BASE-KX/2.5GBASE-KX control register

Bit(s)	Name	Description	R/W[a]
1.160.15:1	Reserved	Value always 0	RO
1.160.0	PMD transmit disable	1 = Disable transmitter output 0 = Enable transmitter output	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.103.1 PMD transmit disable (1.160.0)

This bit disables the 1000BASE-KX transmitter as defined in 70.6.5 or the 2.5GBASE-KX transmitter as defined in 128.6.5.

45.2.1.104 1000BASE-KX/2.5GBASE-KX status register (Register 1.161)

The assignment of bits in the 1000BASE-KX/2.5GBASE-KX status register is shown in Table 45–84.

Table 45–84—1000BASE-KX/2.5GBASE-KX status register

Bit(s)	Name	Description	R/W[a]
1.161.15:14	Reserved	Value always 0	RO
1.161.13	Transmit fault ability	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/ PMD does not have the ability to detect a fault condition on the transmit path	RO
1.161.12	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/ PMD does not have the ability to detect a fault condition on the receive path	RO
1.161.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	LH

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Table 45–84—1000BASE-KX/2.5GBASE-KX status register *(continued)*

Bit(s)	Name	Description	R/W[a]
1.161.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	LH
1.161.9	Reserved	Value always 0	RO
1.161.8	PMD transmit disable ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO
1.161.7:1	Reserved	Value always 0	RO
1.161.0	Signal detect signal from PMD	1 = PMD has asserted signal detect 0 = PMD has not asserted signal detect	RO

[a]RO = Read only, LH = Latching high

45.2.1.104.1 PMD transmit fault ability (1.161.13)

When read as a one, bit 1.161.13 indicates that the PMA/PMD has the ability to detect a fault condition on the transmit path. When read as a zero, bit 1.161.13 indicates that the PMA/PMD does not have the ability to detect a fault condition on the transmit path.

45.2.1.104.2 PMD receive fault ability (1.161.12)

When read as a one, bit 1.161.12 indicates that the PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.161.12 indicates that the PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.104.3 PMD transmit fault (1.161.11)

When read as a one, bit 1.161.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.161.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.161.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 1.161.11 is zero.

45.2.1.104.4 PMD receive fault (1.161.10)

When read as a one, bit 1.161.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.161.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.161.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 1.161.10 is zero.

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45.2.1.104.5 PMD transmit disable ability (1.161.8)

When read as a one, bit 1.161.8 indicates that the PMD is able to perform the transmit disable function. When read as a zero, bit 1.161.8 indicates that the PMD is not able to perform the transmit disable function.

45.2.1.104.6 1000BASE-KX/2.5GBASE-KX signal detect (1.161.0)

The PMD signal detect function for both 1000BASE-KX PMD (see 70.6.4) and 2.5GBASE-KX PMD (see 128.6.4) is mandatory if EEE is implemented and optional otherwise. The 1000BASE-X PCS and 2.5GBASE-X PCS require signal detect to be one before synchronization can occur. If the signal detect function is not implemented this bit is set to one.

45.2.1.105 PMA overhead control 1, 2, and 3 registers (Register 1.162 through 1.164)

Assignment of bits in the PMA overhead control 1, 2, and 3 registers is shown in Table 45–85. These bits shall be reset to the default values indicated in Table 45–85 upon PHY reset. For the 100GBASE-KP4 PHY the use of these registers is specified in 94.2.2.3 and 94.2.3.1.

Table 45–85—PMA overhead control 1, 2, and 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.162.15:13	Reserved	Value always 0	RO
1.162.12:8	PMA transmit overhead sequence 0	Sequence of overhead groups for lane 0 Default = 00110	R/W
1.162.7:0	PMA transmit overhead pattern	Bit pattern for 8-bit transmit overhead group Default = 01100110	R/W
1.163.15	Reserved	Value always 0	RO
1.163.14:10	PMA transmit overhead sequence 3	Sequence of overhead groups for lane 3 Default = 11001	R/W
1.163.9:5	PMA transmit overhead sequence 2	Sequence of overhead groups for lane 2 Default = 10101	R/W
1.163.4:0	PMA transmit overhead sequence 1	Sequence of overhead groups for lane 1 Default = 01010	R/W
1.164.15:8	Reserved	Value always 0	RO
1.164.7:0	PMA receive overhead pattern	Bit pattern for 8-bit receive overhead group Default = 01100110	R/W

[a]R/W = Read/Write, RO = Read only

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45.2.1.106 PMA overhead status 1 and 2 registers (Register 1.165, 1.166)

Assignment of bits in the PMA overhead status 1 and 2 registers is shown in Table 45–86. These bits shall be reset to all zeros upon PHY reset. For the 100GBASE-KP4 PHY the use of these registers is specified in 94.2.3.1.

Table 45–86—PMA overhead status 1 and 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.165.15:12	Reserved	Value always 0	RO
1.165.11:6	PMA receive overhead sequence 1	Sequence of overhead groups for lane 1	RO
1.165.5:0	PMA receive overhead sequence 0	Sequence of overhead groups for lane 0	RO
1.166.15:12	Reserved	Value always 0	RO
1.166.11:6	PMA receive overhead sequence 3	Sequence of overhead groups for lane 3	RO
1.166.5:0	PMA receive overhead sequence 2	Sequence of overhead groups for lane 2	RO

[a]RO = Read only

45.2.1.107 BASE-R FEC ability register (Register 1.170)

The assignment of bits in the BASE-R FEC ability register is shown in Table 45–87.

Table 45–87—BASE-R FEC ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.170.15:2	Reserved	Value always 0	RO
1.170.1	BASE-R FEC error indication ability	A read of one in this bit indicates that the sublayer is able to report FEC decoding errors to the PCS layer	RO
1.170.0	BASE-R FEC ability	A read of one in this bit indicates that the sublayer supports FEC	RO

[a]RO Read only

45.2.1.107.1 BASE-R FEC ability (1.170.0)

When read as a one, this bit indicates that the sublayer supports forward error correction (FEC). When read as a zero, the sublayer does not support forward error correction.

45.2.1.107.2 BASE-R FEC error indication ability (1.170.1)

When read as a one, this bit indicates that the BASE-R FEC sublayer is able to indicate decoding errors to the PCS layer (see 74.8.3). When read as a zero, the BASE-R FEC sublayer is not able to indicate decoding errors to the PCS layer. BASE-R FEC error indication is controlled by the FEC enable error indication bit in the BASE-R FEC control register (see 45.2.1.108.2).

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45.2.1.108 BASE-R FEC control register (Register 1.171)

The assignment of bits in the BASE-R FEC control register is shown in Table 45–88.

Table 45–88—BASE-R FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.171.15:2	Reserved	Value always 0	RO
1.171.1	FEC enable error indication	A write of one to this bit configures the FEC decoder to indicate errors to the PCS layer	R/W
1.171.0	FEC enable	A write of one to this bit enables FEC A write of zero to this bit disables FEC	R/W

[a]R/W = Read/Write, RO Read only

45.2.1.108.1 FEC enable (1.171.0)

When written as a one, this bit enables FEC for the BASE-R PHY. When written as a zero, FEC is disabled in the BASE-R PHY. This bit shall be set to zero upon execution of PHY reset.

45.2.1.108.2 FEC enable error indication (1.171.1)

This bit enables the BASE-R FEC decoder to indicate decoding errors to the upper layers (PCS) through the sync bits for the BASE-R PHY in the Local Device. When written as a one, this bit enables indication of decoding errors through the sync bits to the PCS layer. When written as zero the error indication function is disabled. Writes to this bit are ignored and reads return a zero if the BASE-R FEC does not have the ability to indicate decoding errors to the PCS layer (see 45.2.1.107.2 and 74.8.3).

45.2.1.109 Single-lane PHY BASE-R FEC corrected blocks counter (Register 1.172, 1.173)

The assignment of bits in the single-lane PHY BASE-R FEC corrected blocks counter register is shown in Table 45–89. See 74.8.4.1 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.172, 1.173 are used to read the value of a 32-bit counter. When registers 1.172 and 1.173 are used to read the 32-bit counter value, the register 1.172 is read first, the value of the register 1.173 is latched when (and only when) register 1.172 is read and reads of register 1.173 returns the latched value rather than the current value of the counter.

Table 45–89—Single-lane PHY BASE-R FEC corrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.172.15:0	FEC corrected blocks lower	FEC_corrected_blocks_counter[15:0]	RO, NR
1.173.15:0	FEC corrected blocks upper	FEC_corrected_blocks_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

For a multi-PCS lane PHY, this register may be a copy of register 1.300 BASE-R FEC corrected blocks counter, lane 0. If implemented, all accesses to the copy shall have identical behavior as the original register.

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45.2.1.110 Single-lane PHY BASE-R FEC uncorrected blocks counter (Register 1.174, 1.175)

The assignment of bits in the single-lane PHY BASE-R FEC uncorrected blocks counter register is shown in Table 45–90. See 74.8.4.2 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.174, 1.175 are used to read the value of a 32-bit counter. When registers 1.174 and 1.175 are used to read the 32-bit counter value, the register 1.174 is read first, the value of the register 1.175 is latched when (and only when) register 1.174 is read and reads of register 1.175 returns the latched value rather than the current value of the counter.

Table 45–90—Single-lane PHY BASE-R FEC uncorrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.174.15:0	FEC uncorrected blocks lower	FEC_uncorrected_blocks_counter[15:0]	RO, NR
1.175.15:0	FEC uncorrected blocks upper	FEC_uncorrected_blocks_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

For a multi-PCS lane PHY, this register may be a copy of register 1.700 BASE-R FEC uncorrected blocks counter, lane 0. If implemented, all accesses to the copy shall have identical behavior as the original register.

45.2.1.111 CAUI-4 C2M and 25GAUI C2M recommended CTLE register (Register 1.179)

The assignment of bits in the CAUI-4 C2M and 25GAUI C2M recommended CTLE register is shown in Table 45–91.

Table 45–91—CAUI-4 C2M and 25GAUI C2M recommended CTLE register bit definitions

Bit(s)	Name	Description	R/W[a]
1.179.15:5	Reserved	Value always 0	RO
1.179.4:1	Recommended CTLE peaking	4 3 2 1 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = 9 dB 1 0 0 0 = 8 dB 0 1 1 1 = 7 dB 0 1 1 0 = 6 dB 0 1 0 1 = 5 dB 0 1 0 0 = 4 dB 0 0 1 1 = 3 dB 0 0 1 0 = 2 dB 0 0 0 1 = 1 dB 0 0 0 0 = Reserved	R/W
1.179.0	Reserved	Value always 0	RO

[a]R/W = Read/Write, RO = Read only

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45.2.1.111.1 Recommended CTLE peaking (1.179.4:1)

The value of these bits sets the CTLE peaking value recommended by a host that implements the optional CAUI-4 C2M and 25GAUI C2M interface defined in Annex 83E and Annex 109B, respectively (see 83E.3.1.6). The module may optionally use this information to adjust its CTLE setting.

45.2.1.112 25GAUI C2C and lane 0 CAUI-4 C2C transmitter equalization, receive direction register (Register 1.180)

The assignment of bits in the 25GAUI C2C and lane 0 CAUI-4 C2C transmitter equalization, receive direction register is shown in Table 45–92. The transmitter, receive direction, is the transmitter that sends data towards the PCS.

Table 45–92—25GAUI C2C and lane 0 CAUI-4 C2C transmitter equalization, receive direction register bit definitions

Bit(s)	Name	Description	R/W[a]
1.180.15	Request flag	1 = Change in equalization is requested 0 = No change in equalization is requested	RO
1.180.14:12	Post-cursor request	14 13 12 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Requested_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Requested_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Requested_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Requested_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Requested_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Requested_eq_c1* = 0 (c(1) ratio 0)	RO
1.180.11:10	Pre-cursor request	11 10 1 1 *Requested_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Requested_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Requested_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Requested_eq_cm1* = 0 (c(–1) ratio 0)	RO
1.180.9:7	Post-cursor remote setting	9 8 7 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Remote_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Remote_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Remote_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Remote_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Remote_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Remote_eq_c1* = 0 (c(1) ratio 0)	R/W
1.180.6:5	Pre-cursor remote setting	6 5 1 1 *Remote_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Remote_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Remote_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Remote_eq_cm1* = 0 (c(–1) ratio 0)	R/W

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Table 45–92—25GAUI C2C and lane 0 CAUI-4 C2C transmitter equalization, receive direction register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.180.4:2	Post-cursor local setting	4 3 2 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Local_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Local_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Local_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Local_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Local_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Local_eq_c1* = 0 (c(1) ratio 0)	R/W
1.180.1:0	Pre-cursor local setting	1 0 1 1 *Local_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Local_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Local_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Local_eq_cm1* = 0 (c(–1) ratio 0)	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.112.1 Request flag (1.180.15)

The value of this bit indicates the value of the variable *Request_flag* in the 25GAUI or lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). This indicates whether the 25GAUI or CAUI-4 C2C device is issuing a request to change the remote transmitter equalization in the 25GAUI or lane 0 CAUI-4 C2C transmitter in the receive direction. If a 25GAUI or lane 0 CAUI-4 receiver in the receive direction is not present in the package, then the value returned for this bit should be zero.

45.2.1.112.2 Post-cursor request (1.180.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the 25GAUI or lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). When *Request_flag* is equal to one, this value indicates the ratio of the post-cursor coefficient c(1), which is requested for the transmitter equalization in the 25GAUI or lane 0 CAUI-4 C2C transmitter in the receive direction.

45.2.1.112.3 Pre-cursor request (1.180.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the 25GAUI or lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). When *Request_flag* is equal to one, this value indicates the ratio of the pre-cursor coefficient c(–1), which is requested for the transmitter equalization in the 25GAUI or lane 0 CAUI-4 C2C transmitter in the receive direction.

45.2.1.112.4 Post-cursor remote setting (1.180.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the 25GAUI or lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). This is used by a 25GAUI or CAUI-4 receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient c(1) being used in the 25GAUI or lane 0 of the CAUI-4 transmitter in the receive direction (see 83D.3.1.1). It may be used to generate values for the request flag and the request bits. If a 25GAUI or lane 0 CAUI-4 receiver in the receive direction is not present in the package, then these bits have no effect.

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45.2.1.112.5 Pre-cursor remote setting (1.180.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the 25GAUI or lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). This is used by a 25GAUI or CAUI-4 receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient c(–1) being used in the 25GAUI or lane 0 of the CAUI-4 transmitter in the receive direction (see 83D.3.1.1). It may be used to generate values for the request flag and the request bits. If a 25GAUI or lane 0 CAUI-4 receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.112.6 Post-cursor local setting (1.180.4:2)

The value of these bits sets the variable *Local_eq_c1* for the 25GAUI or lane 0 CAUI-4 transmitter in the receive direction (see 83D.3.1.1 and Table 83D–3), which controls the weight of the transmitter equalization post-cursor coefficient c(1). If a 25GAUI or lane 0 CAUI-4 transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.112.7 Pre-cursor local setting (1.180.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the 25GAUI or lane 0 CAUI-4 transmitter in the receive direction (see 83D.3.1.1 and Table 83D–2), which controls the weight of the transmitter equalization pre-cursor coefficient c(–1). If a 25GAUI or lane 0 CAUI-4 transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.113 CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 1 through lane 3 registers (Registers 1.181, 1.182, 1.183)

The CAUI-4 chip-to-chip transmitter equalization, receive direction, lane 1 through lane 3 registers are defined similarly to register 1.180 (which is used for lane 0, see 45.2.1.112) but for lanes 1 through 3, respectively. The transmitter, receive direction, is the transmitter that sends data towards the PCS.

45.2.1.114 25GAUI C2C and lane 0 CAUI-4 C2C transmitter equalization, transmit direction register (Register 1.184)

The assignment of bits in the 25GAUI C2C and lane 0 CAUI-4 C2C transmitter equalization, transmit direction register is shown in Table 45–93. The transmitter, transmit direction, is the transmitter that sends data towards the PMD.

45.2.1.114.1 Request flag (1.184.15)

The value of this bit indicates the value of the variable *Request_flag* in the 25GAUI or lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). This indicates whether the 25GAUI or CAUI-4 C2C device is issuing a request to change the remote transmitter equalization in the 25GAUI or lane 0 CAUI-4 C2C transmitter in the transmit direction. If a 25GAUI or lane 0 CAUI-4 receiver in the transmit direction is not present in the package, then the value returned for this bit should be zero.

45.2.1.114.2 Post-cursor request (1.184.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the 25GAUI or lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). When *Request_flag* is equal to one, this value indicates the ratio of the post-cursor coefficient c(1), which is requested for the transmitter equalization in the 25GAUI or lane 0 CAUI-4 C2C transmitter in the transmit direction.

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Table 45–93—25GAUI C2C and lane 0 CAUI-4 C2C transmitter equalization, transmit direction register bit definitions

Bit(s)	Name	Description	R/W[a]
1.184.15	Request flag	1 = Change in equalization is requested 0 = No change in equalization is requested	RO
1.184.14:12	Post-cursor request	14 13 12 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Requested_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Requested_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Requested_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Requested_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Requested_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Requested_eq_c1* = 0 (c(1) ratio 0)	RO
1.184.11:10	Pre-cursor request	11 10 1 1 *Requested_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Requested_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Requested_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Requested_eq_cm1* = 0 (c(–1) ratio 0)	RO
1.184.9:7	Post-cursor remote setting	9 8 7 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Remote_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Remote_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Remote_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Remote_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Remote_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Remote_eq_c1* = 0 (c(1) ratio 0)	R/W
1.184.6:5	Pre-cursor remote setting	6 5 1 1 *Remote_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Remote_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Remote_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Remote_eq_cm1* = 0 (c(–1) ratio 0)	R/W
1.184.4:2	Post-cursor local setting	4 3 2 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Local_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Local_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Local_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Local_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Local_eq_c1* = 1 (c(1) ratio–0.05) 0 0 0 *Local_eq_c1* = 0 (c(1) ratio 0)	R/W
1.184.1:0	Pre-cursor local setting	1 0 1 1 *Local_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Local_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Local_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Local_eq_cm1* = 0 (c(–1) ratio 0)	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.114.3 Pre-cursor request (1.184.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the 25GAUI or lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). When *Request_flag* is equal to one, this value

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indicates the ratio of the pre-cursor coefficient c(–1), which is requested for the transmitter equalization in the 25GAUI or lane 0 CAUI-4 C2C transmitter in the transmit direction.

45.2.1.114.4 Post-cursor remote setting (1.184.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the 25GAUI or lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). This is used by a 25GAUI or CAUI-4 receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient c(1) being used in the 25GAUI or lane 0 of the CAUI-4 transmitter in the transmit direction (see 83D.3.1.1). It may be used to generate values for the request flag and the request bits. If a 25GAUI or lane 0 CAUI-4 receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.114.5 Pre-cursor remote setting (1.184.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the 25GAUI or lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). This is used by a 25GAUI or CAUI-4 receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient c(–1) being used in the 25GAUI or lane 0 of the CAUI-4 transmitter in the transmit direction (see 83D.3.1.1). It may be used to generate values for the request flag and the request bits. If a 25GAUI or lane 0 CAUI-4 receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.114.6 Post-cursor local setting (1.184.4:2)

The value of these bits sets the variable *Local_eq_c1* for the 25GAUI or lane 0 CAUI-4 transmitter in the transmit direction (see 83D.3.1.1 and Table 83D–3), which controls the weight of the transmitter equalization post-cursor coefficient c(1). If a 25GAUI or lane 0 CAUI-4 transmitter in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.114.7 Pre-cursor local setting (1.184.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the 25GAUI or lane 0 CAUI-4 transmitter in the transmit direction (see 83D.3.1.1 and Table 83D–2), which controls the weight of the transmitter equalization pre-cursor coefficient c(–1). If a 25GAUI or lane 0 CAUI-4 transmitter in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.115 CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 3 registers (Registers 1.185, 1.186, 1.187)

The CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 3 registers are defined similarly to register 1.184 (which is used for lane 0, see 45.2.1.114) but for lanes 1 through 3, respectively. The transmitter, transmit direction, is the transmitter that sends data towards the PMD.

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45.2.1.116 RS-FEC control register (Register 1.200)

The assignment of bits in the RS-FEC control register is shown in Table 45–94.

Table 45–94—RS-FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.200.15:5	Reserved	Value always 0	RO
1.200.4	FEC degraded SER enable	1 = FEC decoder indicates degraded SER 0 = FEC decoder does not indicate degraded SER	R/W
1.200.3	Four lane PMD indication	1 = FEC is not being used with a four-lane PMD (the four_lane_pmd variable defined in 91.6.1 is set to zero) 0 = FEC is being used with a four-lane PMD (the four_lane_pmd variable defined in 91.6.1 is set to one)	R/W
1.200.2	RS-FEC Enable	1 = Clause 108 Reed-Solomon FEC is enabled 0 = Clause 108 Reed-Solomon FEC is disabled	R/W
1.200.1	FEC bypass indication enable	1 = FEC decoder does not indicate errors to the PCS 0 = FEC decoder indicates errors to the PCS layer	R/W
1.200.0	FEC bypass correction enable	1 = FEC decoder performs error detection without error correction 0 = FEC decoder performs error detection and error correction	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.116.1 FEC degraded SER enable (1.200.4)

This bit enables the RS-FEC decoder to indicate the presence of a degraded SER (see 91.5.3.3.1 and 134.5.3.3.2). When set to a one, this bit enables degraded SER detection. When set to a zero, degraded SER detection is disabled. Writes to this bit are ignored and reads return a zero if the FEC does not have the ability to signal the presence of a degraded SER.

45.2.1.116.2 Four-lane PMD (1.200.3)

This bit enables the alignment marker mapping function in the RS-FEC to substitute the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16 (see 91.5.2.6). When this bit is set to zero, the alignment markers corresponding to PCS lanes 17, 18, and 19 are passed through unmodified. The default value of this bit is zero.

45.2.1.116.3 RS-FEC enable (1.200.2)

Bit 1.200.2 enables the Reed-Solomon FEC described in Clause 108. When set to a one, this bit enables the Reed-Solomon FEC. When set to a zero, bit 1.200.2 disables the Reed-Solomon FEC (see 108.6.3). Writes to bit 1.200.2 are ignored and reads return a one if the RS-FEC does not have the ability to disable the RS-FEC function.

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45.2.1.116.4 FEC bypass indication enable (1.200.1)

This bit enables the RS-FEC decoder to bypass error indication to the upper layers (PCS) through the sync bits for the BASE-R PHY in the Local Device. When set to a one, this bit enables bypass of the error indication. When set to a zero, errors are indicated to the PCS through the sync bits. Writes to bit 1.200.1 are ignored and reads return a zero if the RS-FEC does not have the ability to bypass indicating decoding errors to the PCS layer (see 91.5.3.3, 108.5.3.2, and 134.5.3.3.1).

45.2.1.116.5 FEC bypass correction enable (1.200.0)

When bit 1.200.0 is set to one the Reed-Solomon decoder performs error detection without error correction (see 91.5.3.3 and 108.5.3.2). When this bit is set to zero, the decoder also performs error correction. Writes to this bit are ignored and reads return a zero if the RS-FEC does not have the ability to bypass correction.

45.2.1.117 RS-FEC status register (Register 1.201)

The assignment of bits in the RS-FEC status register is shown in Table 45–95.

Table 45–95—RS-FEC status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.201.15	PCS align status	1 = FEC encoder has locked and aligned all PCS lanes 0 = FEC encoder has not locked and aligned all PCS lanes	RO
1.201.14	RS-FEC align status	1 = RS-FEC receive lanes locked and aligned 0 = RS-FEC receive lanes not locked and aligned	RO
1.201.13:12	Reserved	Value always 0	RO
1.201.11	FEC AM lock 3	1 = RS-FEC receive lane 3 locked and aligned 0 = RS-FEC receive lane 3 not locked and aligned	RO
1.201.10	FEC AM lock 2	1 = RS-FEC receive lane 2 locked and aligned 0 = RS-FEC receive lane 2 not locked and aligned	RO
1.201.9	FEC AM lock 1	1 = RS-FEC receive lane 1 locked and aligned 0 = RS-FEC receive lane 1 not locked and aligned	RO
1.201.8	FEC AM lock 0	1 = RS-FEC receive lane 0 locked and aligned 0 = RS-FEC receive lane 0 not locked and aligned	RO
1.201.7	FEC optional states supported	1 = RS-FEC supports optional states in Figure 91–8 0 = RS-FEC does not support optional states in Figure 91–8	RO
1.201.6:5	Reserved	Value always 0	RO
1.201.4	FEC degraded SER	1 = SER is degraded 0 = SER is not degraded	RO
1.201.3	FEC degraded SER ability	1 = RS-FEC decoder has the ability to indicate the presence of a degraded SER 0 = RS-FEC decoder does not have the ability to indicate the presence of a degraded SER	RO
1.201.2	RS-FEC high SER	1 = FEC errors have exceeded threshold 0 = FEC errors have not exceeded threshold	RO/LH

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Table 45–95—RS-FEC status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.201.1	FEC bypass indication ability	1 = FEC decoder has the ability to bypass error indication 0 = FEC decoder does not have the ability to bypass error indication	RO
1.201.0	FEC bypass correction ability	1 = FEC decoder has the ability to bypass error correction 0 = FEC decoder does not have the ability to bypass error correction	RO

[a]RO = Read only, LH = Latching high

45.2.1.117.1 PCS align status (1.201.15)

Bit 1.201.15 indicates the PCS alignment status of the RS-FEC. For the RS-FEC described in Clause 91 or Clause 134, PCS alignment is defined as block lock, alignment marker lock, and deskew of all transmit PCS lanes. For the RS-FEC described in Clause 108, PCS alignment is defined as block lock of the transmit PCS signal. When read as a zero, bit 1.201.15 indicates that the RS-FEC has not obtained PCS alignment. When read as a one, bit 1.201.15 indicates that the RS-FEC has obtained PCS alignment.

45.2.1.117.2 RS-FEC align status (1.201.14)

Bit 1.201.14 indicates the PMA alignment status of the RS-FEC. For the RS-FEC described in Clause 91 or Clause 134, PMA alignment is defined as alignment marker lock and deskew of all lanes on the PMA service interface. For the RS-FEC described in Clause 108, PMA alignment is defined as codeword marker lock on the PMA service interface. When read as a zero, bit 1.201.14 indicates that the RS-FEC has not obtained PMA alignment. When read as a one, bit 1.201.14 indicates that the RS-FEC has obtained PMA alignment.

45.2.1.117.3 FEC AM lock 3 (1.201.11)

When read as a one, bit 1.201.11 indicates that the RS-FEC described in Clause 91 has locked and aligned lane 3 of the PMA service interface. When read as a zero, bit 1.201.11 indicates that the RS-FEC has not locked and aligned lane 3 of the PMA service interface. This bit reflects the state of amps_lock[3] (see 91.5.3.1).

45.2.1.117.4 FEC AM lock 2 (1.201.10)

When read as a one, bit 1.201.10 indicates that the RS-FEC described in Clause 91 has locked and aligned lane 2 of the PMA service interface. When read as a zero, bit 1.201.10 indicates that the RS-FEC has not locked and aligned lane 2 of the PMA service interface. This bit reflects the state of amps_lock[2] (see 91.5.3.1).

45.2.1.117.5 FEC AM lock 1 (1.201.9)

When read as a one, bit 1.201.9 indicates that the RS-FEC described in Clause 91 or Clause 134 has locked and aligned lane 1 of the PMA service interface. When read as a zero, bit 1.201.9 indicates that the RS-FEC has not locked and aligned lane 1 of the PMA service interface. This bit reflects the state of amps_lock[1] (see 91.5.3.1).

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45.2.1.117.6 FEC AM lock 0 (1.201.8)

When read as a one, bit 1.201.8 indicates that the RS-FEC described in Clause 91 or Clause 134 has locked and aligned lane 0 of the PMA service interface. When read as a zero, bit 1.201.8 indicates that the RS-FEC has not locked and aligned lane 0 of the PMA service interface. This bit reflects the state of amps_lock[0] (see 91.5.3.1).

45.2.1.117.7 FEC optional states supported (1.201.7)

When read as a one, bit 1.201.7 indicates that the RS-FEC described in Clause 91 implements the optional states in Figure 91–8. When read as a zero, bit 1.201.7 indicates that the optional states are not implemented.

45.2.1.117.8 FEC degraded SER (1.201.4)

This bit (1.201.4) reflects the state of the variable FEC_degraded_SER (see 91.6.12 and 134.6.9). When read as a one, bit 1.201.4 indicates the presence of a degraded received signal.

45.2.1.117.9 FEC degraded SER ability (1.201.3)

This bit is set to one to indicate that the decoder has the ability to indicate the presence of a degraded SER (see 91.5.3.3.1 and 134.5.3.3.2). This bit is set to zero if this ability is not supported.

45.2.1.117.10 RS-FEC high SER (1.201.2)

When FEC_bypass_indication_enable is set to one, bit 1.201.2 is set to one if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 91.5.3.3, 108.5.3.2, and 134.5.3.3.1) and is set to zero otherwise. The bit is set to zero if FEC_bypass_indication_enable is set to zero. This bit shall be implemented with latching high behavior.

45.2.1.117.11 FEC bypass indication ability (1.201.1)

The Reed-Solomon decoder may have the option to perform error detection without error indication (see 91.5.3.3, 108.5.3.2, and 134.5.3.3.1) to reduce the delay contributed by the RS-FEC sublayer. This bit is set to one to indicate that the decoder has this ability to bypass error indication. The bit is set to zero if this ability is not supported.

45.2.1.117.12 FEC bypass correction ability (1.201.0)

The Reed-Solomon decoder may have the option to perform error detection without error correction (see 91.5.3.3 and 108.5.3.2) to reduce the delay contributed by the RS-FEC sublayer. This bit is set to one to indicate that the decoder has this ability to bypass error correction. The bit is set to zero if this ability is not supported.

45.2.1.118 RS-FEC corrected codewords counter (Register 1.202, 1.203)

The assignment of bits in the RS-FEC corrected codewords counter register is shown in Table 45–96. See 91.6.16 and 108.6.7 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.202, 1.203 are used to read the value of a 32-bit counter. When registers 1.202 and 1.203 are used to read the 32-bit counter value, the register 1.202 is read first, the value of the register 1.203 is

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latched when (and only when) register 1.202 is read, and reads of register 1.203 return the latched value rather than the current value of the counter.

Table 45–96—RS-FEC corrected codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.202.15:0	FEC corrected codewords lower	FEC_corrected_cw_counter[15:0]	RO, NR
1.203.15:0	FEC corrected codewords upper	FEC_corrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.119 RS-FEC uncorrected codewords counter (Register 1.204, 1.205)

The assignment of bits in the RS-FEC uncorrected codewords counter register is shown in Table 45–97. See 91.6.17 and 108.6.8 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.204, 1.205 are used to read the value of a 32-bit counter. When registers 1.204 and 1.205 are used to read the 32-bit counter value, the register 1.204 is read first, the value of the register 1.205 is latched when (and only when) register 1.204 is read, and reads of register 1.205 return the latched value rather than the current value of the counter.

Table 45–97—RS-FEC uncorrected codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.204.15:0	FEC uncorrected codewords lower	FEC_uncorrected_cw_counter[15:0]	RO, NR
1.205.15:0	FEC uncorrected codewords upper	FEC_uncorrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.120 RS-FEC lane mapping register (Register 1.206)

The assignment of bits in the RS-FEC lane mapping register is shown in Table 45–98. When the RS-FEC detects and locks the RS-FEC for PMA service interface lane 0, the detected RS-FEC lane number is recorded bits 1:0 in this register. Similarly, the detected RS-FEC lane numbers for PMA service lanes 1, 2, and 3 are recorded in register bits 3:2, 5:4, and 7:6, respectively. The contents of the RS-FEC lane mapping register bits 7:0 are valid when RS-FEC align status (1.201.14) is set to one and are invalid otherwise.

Table 45–98—RS-FEC lane mapping register

Bit(s)	Name	Description	R/W[a]
1.206.15:8	Reserved	Value always 0	RO
1.206.7:6	RS-FEC lane 3 mapping	RS-FEC lane mapped to PMA lane 3	RO
1.206.5:4	RS-FEC lane 2 mapping	RS-FEC lane mapped to PMA lane 2	RO

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Table 45–98—RS-FEC lane mapping register *(continued)*

Bit(s)	Name	Description	R/W[a]
1.206.3:2	RS-FEC lane 1 mapping	RS-FEC lane mapped to PMA lane 1	RO
1.206.1:0	RS-FEC lane 0 mapping	RS-FEC lane mapped to PMA lane 0	RO

[a]RO = Read only

45.2.1.121 RS-FEC symbol error counter lane 0 (Register 1.210, 1.211)

The assignment of bits in the RS-FEC symbol error counter lane 0 register is shown in Table 45–99. Symbol errors detected in FEC lane 0 are counted and shown in register 1.210.15:0 and 1.211.15:0. See 91.6.19 and 108.6.9 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.210, 1.211 are used to read the value of a 32-bit counter. When registers 1.210 and 1.211 are used to read the 32-bit counter value, the register 1.210 is read first, the value of the register 1.211 is latched when (and only when) register 1.210 is read, and reads of register 1.211 return the latched value rather than the current value of the counter.

Table 45–99—RS-FEC symbol error counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.210.15:0	FEC symbol errors, lane 0 lower	FEC_symbol_error_counter_0[15:0]	RO, NR
1.211.15:0	FEC symbol errors, lane 0 upper	FEC_symbol_error_counter_0[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.122 RS-FEC symbol error counter lane 1 through 3 (Register 1.212, 1.213, 1.214, 1.215, 1.216, 1.217)

The behavior of the RS-FEC symbol error counters, lane 1 through 3 is identical to that described for FEC lane 0 in 45.2.1.121. Errors detected in each FEC lane are counted and shown in the corresponding register. FEC lane 1, lower 16 bits are shown in register 1.212; FEC lane 1, upper 16 bits are shown in register 1.213; FEC lane 2, lower 16 bits are shown in register 1.214; through register 1.217 for FEC lane 3, upper 16 bits.

45.2.1.123 RS-FEC BIP error counter lane 0 (Register 1.230)

The assignment of bits in the RS-FEC BIP error counter lane 0 is shown in Table 45–100. The RS-FEC described in Clause 91 or Clause 134 calculates a BIP value for each PCS lane (see 91.5.2.4, 91.6.8). Errors detected in PCS lane 0 are counted and shown in register 1.230.15:0. The 16-bit counter shall be reset to all zeros when register 1.230 is read or upon PMA/PMD reset. The 16-bit counter shall be held at all ones in the case of overflow. A device that does not implement a separated RS-FEC shall return a zero for all bits in the RS-FEC BIP error counter, lane 0 register.

45.2.1.124 RS-FEC BIP error counter, lane 1 through 19 (Registers 1.231 through 1.249)

The behavior of the RS-FEC BIP error counters, lane 1 through 19 is identical to that described for lane 0 in 45.2.1.123. Errors detected in each PCS lane are counted and shown in register bits 15:0 in the

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Table 45–100—RS-FEC BIP error counter lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.230.15:0	BIP error counter, lane 0	Errors detected by BIP in PCS lane 0	RO, NR

[a]RO = Read only, NR = Non Roll-over

corresponding register. PCS lane 1 is shown in register 1.231; PCS lane 2 is shown in register 1.232; through register 1.249 for PCS lane 19.

45.2.1.125 RS-FEC PCS lane 0 mapping register (Register 1.250)

The assignment of bits in the RS-FEC PCS lane 0 mapping register is shown in Table 45–101. When the RS-FEC instance of the multi-lane PCS described in Clause 82 detects and locks the alignment marker for service interface lane 0, the detected PCS lane number is recorded in this register. The contents of the Lane 0 mapping register is valid when the transmit PCS align status bit (register 1.201.15) is set to one and is invalid otherwise (see 45.2.1.117). A device that does not implement a separated RS-FEC shall return a zero for all bits in the RS-FEC PCS lane 0 mapping register.

Table 45–101—RS-FEC PCS lane 0 mapping register bit definitions

Bit(s)	Name	Description	R/W[a]
1.250.15:5	Reserved	Value always 0	RO
1.250.4:0	Lane 0 mapping	PCS lane received in service interface lane 0	RO

[a]RO = Read only

45.2.1.126 RS-FEC PCS lanes 1 through 19 mapping registers (Registers 1.251 through 1.269)

The definition of Lanes 1 through 19 mapping registers is identical to that described for lane 0 in 45.2.1.125. The lane mapping for lane 1 is in register 1.251; lane 2 is in register 1.252; etc.

45.2.1.127 RS-FEC PCS alignment status 1 register (Register 1.280)

The assignment of bits in the RS-FEC PCS alignment status 1 register is shown in Table 45–252. All the bits in the RS-FEC PCS alignment status 1 register are read only; a write to the RS-FEC PCS alignment status 1 register shall have no effect. A device that does not implement a separated RS-FEC shall return a zero for all

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bits in the RS-FEC PCS alignment status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–102—RS-FEC PCS alignment status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.280.15:8	Reserved	Value always 0	RO
1.280.7	Block lock 7	1 = Lane 7 is locked 0 = Lane 7 is not locked	RO
1.280.6	Block lock 6	1 = Lane 6 is locked 0 = Lane 6 is not locked	RO
1.280.5	Block lock 5	1 = Lane 5 is locked 0 = Lane 5 is not locked	RO
1.280.4	Block lock 4	1 = Lane 4 is locked 0 = Lane 4 is not locked	RO
1.280.3	Block lock 3	1 = Lane 3 is locked 0 = Lane 3 is not locked	RO
1.280.2	Block lock 2	1 = Lane 2 is locked 0 = Lane 2 is not locked	RO
1.280.1	Block lock 1	1 = Lane 1 is locked 0 = Lane 1 is not locked	RO
1.280.0	Block lock 0	1 = Lane 0 is locked 0 = Lane 0 is not locked	RO

[a]RO = Read only

45.2.1.127.1 Block lock 7 (1.280.7)

When read as a one, bit 1.280.7 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 7. When read as a zero, bit 1.280.7 indicates that the RS-FEC transmit function lane 7 has not achieved block lock. This bit reflects the state of block_lock[7] (see 91.5.2.1).

45.2.1.127.2 Block lock 6 (1.280.6)

When read as a one, bit 1.280.6 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 6. When read as a zero, bit 1.280.6 indicates that the RS-FEC transmit function lane 6 has not achieved block lock. This bit reflects the state of block_lock[6] (see 91.5.2.1).

45.2.1.127.3 Block lock 5 (1.280.5)

When read as a one, bit 1.280.5 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 5. When read as a zero, bit 1.280.5 indicates that the RS-FEC transmit function lane 5 has not achieved block lock. This bit reflects the state of block_lock[5] (see 91.5.2.1).

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45.2.1.127.4 Block lock 4 (1.280.4)

When read as a one, bit 1.280.4 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 4. When read as a zero, bit 1.280.4 indicates that the RS-FEC transmit function lane 4 has not achieved block lock. This bit reflects the state of block_lock[4] (see 91.5.2.1).

45.2.1.127.5 Block lock 3 (1.280.3)

When read as a one, bit 1.280.3 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 3. When read as a zero, bit 1.280.3 indicates that the RS-FEC transmit function lane 3 has not achieved block lock. This bit reflects the state of block_lock[3] (see 91.5.2.1).

45.2.1.127.6 Block lock 2 (1.280.2)

When read as a one, bit 1.280.2 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 2. When read as a zero, bit 1.280.2 indicates that the RS-FEC transmit function lane 2 has not achieved block lock. This bit reflects the state of block_lock[2] (see 91.5.2.1).

45.2.1.127.7 Block lock 1 (1.280.1)

When read as a one, bit 1.280.1 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 1. When read as a zero, bit 1.280.1 indicates that the RS-FEC transmit function lane 1 has not achieved block lock. This bit reflects the state of block_lock[1] (see 91.5.2.1).

45.2.1.127.8 Block lock 0 (1.280.0)

When read as a one, bit 1.280.0 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 0. When read as a zero, bit 1.280.0 indicates that the RS-FEC transmit function lane 0 has not achieved block lock. This bit reflects the state of block_lock[0] (see 91.5.2.1).

45.2.1.128 RS-FEC PCS alignment status 2 register (Register 1.281)

The assignment of bits in the RS-FEC PCS alignment status 2 register is shown in Table 45–253. All the bits in the RS-FEC PCS alignment status 2 register are read only; a write to the RS-FEC PCS alignment status 2 register shall have no effect. A device that does not implement a separated RS-FEC shall return a zero for all bits in the RS-FEC PCS alignment status 2 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–103—RS-FEC PCS alignment status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.281.15:12	Reserved	Value always 0	RO
1.281.11	Block lock 19	1 = Lane 19 is locked 0 = Lane 19 is not locked	RO
1.281.10	Block lock 18	1 = Lane 18 is locked 0 = Lane 18 is not locked	RO
1.281.9	Block lock 17	1 = Lane 17 is locked 0 = Lane 17 is not locked	RO

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Table 45–103—RS-FEC PCS alignment status 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.281.8	Block lock 16	1 = Lane 16 is locked 0 = Lane 16 is not locked	RO
1.281.7	Block lock 15	1 = Lane 15 is locked 0 = Lane 15 is not locked	RO
1.281.6	Block lock 14	1 = Lane 14 is locked 0 = Lane 14 is not locked	RO
1.281.5	Block lock 13	1 = Lane 13 is locked 0 = Lane 13 is not locked	RO
1.281.4	Block lock 12	1 = Lane 12 is locked 0 = Lane 12 is not locked	RO
1.281.3	Block lock 11	1 = Lane 11 is locked 0 = Lane 11 is not locked	RO
1.281.2	Block lock 10	1 = Lane 10 is locked 0 = Lane 10 is not locked	RO
1.281.1	Block lock 9	1 = Lane 9 is locked 0 = Lane 9 is not locked	RO
1.281.0	Block lock 8	1 = Lane 8 is locked 0 = Lane 8 is not locked	RO

[a]RO = Read only

45.2.1.128.1 Block lock 19 (1.281.11)

When read as a one, bit 1.281.11 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 19. When read as a zero, bit 1.281.11 indicates that the RS-FEC transmit function lane 19 has not achieved block lock. This bit reflects the state of block_lock[19] (see 91.5.2.1).

45.2.1.128.2 Block lock 18 (1.281.10)

When read as a one, bit 1.281.10 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 18. When read as a zero, bit 1.281.10 indicates that the RS-FEC transmit function lane 18 has not achieved block lock. This bit reflects the state of block_lock[18] (see 91.5.2.1).

45.2.1.128.3 Block lock 17 (1.281.9)

When read as a one, bit 1.281.9 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 17. When read as a zero, bit 1.281.9 indicates that the RS-FEC transmit function lane 17 has not achieved block lock. This bit reflects the state of block_lock[17] (see 91.5.2.1).

45.2.1.128.4 Block lock 16 (1.281.8)

When read as a one, bit 1.281.8 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 16. When read as a zero, bit 1.281.8 indicates that the RS-FEC transmit function lane 16 has not achieved block lock. This bit reflects the state of block_lock[16] (see 91.5.2.1).

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45.2.1.128.5 Block lock 15 (1.281.7)

When read as a one, bit 1.281.7 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 15. When read as a zero, bit 1.281.7 indicates that the RS-FEC transmit function lane 15 has not achieved block lock. This bit reflects the state of block_lock[15] (see 91.5.2.1).

45.2.1.128.6 Block lock 14 (1.281.6)

When read as a one, bit 1.281.6 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 14. When read as a zero, bit 1.281.6 indicates that the RS-FEC transmit function lane 14 has not achieved block lock. This bit reflects the state of block_lock[14] (see 91.5.2.1).

45.2.1.128.7 Block lock 13 (1.281.5)

When read as a one, bit 1.281.5 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 13. When read as a zero, bit 1.281.5 indicates that the RS-FEC transmit function lane 13 has not achieved block lock. This bit reflects the state of block_lock[13] (see 91.5.2.1).

45.2.1.128.8 Block lock 12 (1.281.4)

When read as a one, bit 1.281.4 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 12. When read as a zero, bit 1.281.4 indicates that the RS-FEC transmit function lane 12 has not achieved block lock. This bit reflects the state of block_lock[12] (see 91.5.2.1).

45.2.1.128.9 Block lock 11 (1.281.3)

When read as a one, bit 1.281.3 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 11. When read as a zero, bit 1.281.3 indicates that the RS-FEC transmit function lane 11 has not achieved block lock. This bit reflects the state of block_lock[11] (see 91.5.2.1).

45.2.1.128.10 Block lock 10 (1.281.2)

When read as a one, bit 1.281.2 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 10. When read as a zero, bit 1.281.2 indicates that the RS-FEC transmit function lane 10 has not achieved block lock. This bit reflects the state of block_lock[10] (see 91.5.2.1).

45.2.1.128.11 Block lock 9 (1.281.1)

When read as a one, bit 1.281.1 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 9. When read as a zero, bit 1.281.1 indicates that the RS-FEC transmit function lane 9 has not achieved block lock. This bit reflects the state of block_lock[9] (see 91.5.2.1).

45.2.1.128.12 Block lock 8 (1.281.0)

When read as a one, bit 1.281.0 indicates that the RS-FEC transmit function has achieved block lock for service interface lane 8. When read as a zero, bit 1.281.0 indicates that the RS-FEC transmit function lane 8 has not achieved block lock. This bit reflects the state of block_lock[8] (see 91.5.2.1).

45.2.1.129 RS-FEC PCS alignment status 3 register (Register 1.282)

The assignment of bits in the RS-FEC PCS alignment status 3 register is shown in Table 45–104. All the bits in the RS-FEC PCS alignment status 3 register are read only; a write to the RS-FEC PCS alignment status 3 register shall have no effect. A device that does not implement a separated RS-FEC shall return a zero for all

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bits in the RS-FEC PCS alignment status 3 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–104—RS-FEC PCS alignment status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.282.15:8	Reserved	Value always 0	RO
1.282.7	Lane 7 aligned	1 = Lane 7 alignment marker is locked 0 = Lane 7 alignment marker is not locked	RO
1.282.6	Lane 6 aligned	1 = Lane 6 alignment marker is locked 0 = Lane 6 alignment marker is not locked	RO
1.282.5	Lane 5 aligned	1 = Lane 5 alignment marker is locked 0 = Lane 5 alignment marker is not locked	RO
1.282.4	Lane 4 aligned	1 = Lane 4 alignment marker is locked 0 = Lane 4 alignment marker is not locked	RO
1.282.3	Lane 3 aligned	1 = Lane 3 alignment marker is locked 0 = Lane 3 alignment marker is not locked	RO
1.282.2	Lane 2 aligned	1 = Lane 2 alignment marker is locked 0 = Lane 2 alignment marker is not locked	RO
1.282.1	Lane 1 aligned	1 = Lane 1 alignment marker is locked 0 = Lane 1 alignment marker is not locked	RO
1.282.0	Lane 0 aligned	1 = Lane 0 alignment marker is locked 0 = Lane 0 alignment marker is not locked	RO

[a]RO = Read only

45.2.1.129.1 Lane 7 aligned (1.282.7)

When read as a one, bit 1.282.7 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 7. When read as a zero, bit 1.282.7 indicates that the RS-FEC transmit function lane 7 has not achieved alignment marker lock. This bit reflects the state of am_lock[7] (see 91.5.2.2).

45.2.1.129.2 Lane 6 aligned (1.282.6)

When read as a one, bit 1.282.6 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 6. When read as a zero, bit 1.282.6 indicates that the RS-FEC transmit function lane 6 has not achieved alignment marker lock. This bit reflects the state of am_lock[6] (see 91.5.2.2).

45.2.1.129.3 Lane 5 aligned (1.282.5)

When read as a one, bit 1.282.5 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 5. When read as a zero, bit 1.282.5 indicates that the RS-FEC transmit function lane 5 has not achieved alignment marker lock. This bit reflects the state of am_lock[5] (see 91.5.2.2).

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45.2.1.129.4 Lane 4 aligned (1.282.4)

When read as a one, bit 1.282.4 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 4. When read as a zero, bit 1.282.4 indicates that the RS-FEC transmit function lane 4 has not achieved alignment marker lock. This bit reflects the state of am_lock[4] (see 91.5.2.2).

45.2.1.129.5 Lane 3 aligned (1.282.3)

When read as a one, bit 1.282.3 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 3. When read as a zero, bit 1.282.3 indicates that the RS-FEC transmit function lane 3 has not achieved alignment marker lock. This bit reflects the state of am_lock[3] (see 91.5.2.2).

45.2.1.129.6 Lane 2 aligned (1.282.2)

When read as a one, bit 1.282.2 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 2. When read as a zero, bit 1.282.2 indicates that the RS-FEC transmit function lane 2 has not achieved alignment marker lock. This bit reflects the state of am_lock[2] (see 91.5.2.2).

45.2.1.129.7 Lane 1 aligned (1.282.1)

When read as a one, bit 1.282.1 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 1. When read as a zero, bit 1.282.1 indicates that the RS-FEC transmit function lane 1 has not achieved alignment marker lock. This bit reflects the state of am_lock[1] (see 91.5.2.2).

45.2.1.129.8 Lane 0 aligned (1.282.0)

When read as a one, bit 1.282.0 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 0. When read as a zero, bit 1.282.0 indicates that the RS-FEC transmit function lane 0 has not achieved alignment marker lock. This bit reflects the state of am_lock[0] (see 91.5.2.2).

45.2.1.130 RS-FEC PCS alignment status 4 register (Register 1.283)

The assignment of bits in the RS-FEC PCS alignment status 4 register is shown in Table 45–105. All the bits in the RS-FEC PCS alignment status 4 register are read only; a write to the RS-FEC PCS alignment status 4 register shall have no effect. A device that does not implement a separated RS-FEC shall return a zero for all bits in the RS-FEC PCS alignment status 4 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–105—RS-FEC PCS alignment status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.283.15:12	Reserved	Value always 0	RO
1.283.11	Lane 19 aligned	1 = Lane 19 alignment marker is locked 0 = Lane 19 alignment marker is not locked	RO
1.283.10	Lane 18 aligned	1 = Lane 18 alignment marker is locked 0 = Lane 18 alignment marker is not locked	RO
1.283.9	Lane 17 aligned	1 = Lane 17 alignment marker is locked 0 = Lane 17 alignment marker is not locked	RO

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Table 45–105—RS-FEC PCS alignment status 4 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.283.8	Lane 16 aligned	1 = Lane 16 alignment marker is locked 0 = Lane 16 alignment marker is not locked	RO
1.283.7	Lane 15 aligned	1 = Lane 15 alignment marker is locked 0 = Lane 15 alignment marker is not locked	RO
1.283.6	Lane 14 aligned	1 = Lane 14 alignment marker is locked 0 = Lane 14 alignment marker is not locked	RO
1.283.5	Lane 13 aligned	1 = Lane 13 alignment marker is locked 0 = Lane 13 alignment marker is not locked	RO
1.283.4	Lane 12 aligned	1 = Lane 12 alignment marker is locked 0 = Lane 12 alignment marker is not locked	RO
1.283.3	Lane 11 aligned	1 = Lane 11 alignment marker is locked 0 = Lane 11 alignment marker is not locked	RO
1.283.2	Lane 10 aligned	1 = Lane 10 alignment marker is locked 0 = Lane 10 alignment marker is not locked	RO
1.283.1	Lane 9 aligned	1 = Lane 9 alignment marker is locked 0 = Lane 9 alignment marker is not locked	RO
1.283.0	Lane 8 aligned	1 = Lane 8 alignment marker is locked 0 = Lane 8 alignment marker is not locked	RO

[a]RO = Read only

45.2.1.130.1 Lane 19 aligned (1.283.11)

When read as a one, bit 1.283.11 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 19. When read as a zero, bit 1.283.11 indicates that the RS-FEC transmit function lane 19 has not achieved alignment marker lock. This bit reflects the state of am_lock[19] (see 91.5.2.2).

45.2.1.130.2 Lane 18 aligned (1.283.10)

When read as a one, bit 1.283.10 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 18. When read as a zero, bit 1.283.10 indicates that the RS-FEC transmit function lane 18 has not achieved alignment marker lock. This bit reflects the state of am_lock[18] (see 91.5.2.2).

45.2.1.130.3 Lane 17 aligned (1.283.9)

When read as a one, bit 1.283.9 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 17. When read as a zero, bit 1.283.9 indicates that the RS-FEC transmit function lane 17 has not achieved alignment marker lock. This bit reflects the state of am_lock[17] (see 91.5.2.2).

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45.2.1.130.4 Lane 16 aligned (1.283.8)

When read as a one, bit 1.283.8 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 16. When read as a zero, bit 1.283.8 indicates that the RS-FEC transmit function lane 16 has not achieved alignment marker lock. This bit reflects the state of am_lock[16] (see 91.5.2.2).

45.2.1.130.5 Lane 15 aligned (1.283.7)

When read as a one, bit 1.283.7 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 15. When read as a zero, bit 1.283.7 indicates that the RS-FEC transmit function lane 15 has not achieved alignment marker lock. This bit reflects the state of am_lock[15] (see 91.5.2.2).

45.2.1.130.6 Lane 14 aligned (1.283.6)

When read as a one, bit 1.283.6 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 14. When read as a zero, bit 1.283.6 indicates that the RS-FEC transmit function lane 14 has not achieved alignment marker lock. This bit reflects the state of am_lock[14] (see 91.5.2.2).

45.2.1.130.7 Lane 13 aligned (1.283.5)

When read as a one, bit 1.283.5 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 13. When read as a zero, bit 1.283.5 indicates that the RS-FEC transmit function lane 13 has not achieved alignment marker lock. This bit reflects the state of am_lock[13] (see 91.5.2.2).

45.2.1.130.8 Lane 12 aligned (1.283.4)

When read as a one, bit 1.283.4 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 12. When read as a zero, bit 1.283.4 indicates that the RS-FEC transmit function lane 12 has not achieved alignment marker lock. This bit reflects the state of am_lock[12] (see 91.5.2.2).

45.2.1.130.9 Lane 11 aligned (1.283.3)

When read as a one, bit 1.283.3 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 11. When read as a zero, bit 1.283.3 indicates that the RS-FEC transmit function lane 11 has not achieved alignment marker lock. This bit reflects the state of am_lock[11] (see 91.5.2.2).

45.2.1.130.10 Lane 10 aligned (1.283.2)

When read as a one, bit 1.283.2 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 10. When read as a zero, bit 1.283.2 indicates that the RS-FEC transmit function lane 10 has not achieved alignment marker lock. This bit reflects the state of am_lock[10] (see 91.5.2.2).

45.2.1.130.11 Lane 9 aligned (1.283.1)

When read as a one, bit 1.283.1 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 9. When read as a zero, bit 1.283.1 indicates that the RS-FEC transmit function lane 9 has not achieved alignment marker lock. This bit reflects the state of am_lock[9] (see 91.5.2.2).

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45.2.1.130.12 Lane 8 aligned (1.283.0)

When read as a one, bit 1.283.0 indicates that the RS-FEC transmit function has achieved alignment marker lock for service interface lane 8. When read as a zero, bit 1.283.0 indicates that the RS-FEC transmit function lane 8 has not achieved alignment marker lock. This bit reflects the state of am_lock[8] (see 91.5.2.2).

45.2.1.131 BASE-R FEC corrected blocks counter, lanes 0 through 19

(Register 1.300, 1.301, 1.302, 1.303, 1.304, 1.305, 1.306, 1.307, 1.308, 1.309, 1.310, 1.311, 1.312, 1.313, 1.314, 1.315, 1.316, 1.317, 1.318, 1.319, 1.320, 1.321, 1.322, 1.323, 1.324, 1.325, 1.326, 1.327, 1.328, 1.329, 1.330, 1.331, 1.332, 1.333, 1.334, 1.335, 1.336, 1.337, 1.338, 1.339)

For multi-PCS lane BASE-R PHYs, the even-numbered registers in this set are defined similarly to register 1.172 (see 45.2.1.109) but for lanes 0 through 19 respectively of multi-PCS lane PHYs. The odd-numbered registers in this set are defined similarly to register 1.173 (see 45.2.1.109) but for lanes 0 through 19 respectively of multilane PHYs. Note that the lane numbers refer to the service interface lanes and do not necessarily correspond to the PCS lane numbers.

Registers corresponding to lanes that are not used for the selected PHY shall return all zeros.

45.2.1.132 200GAUI-8 and 400GAUI-16 chip-to-module recommended CTLE, lane 0 register (Register 1.400)

The assignment of bits in the 200GAUI-8 and 400GAUI-16 chip-to-module recommended CTLE, lane 0 register is shown in Table 45–106.

Table 45–106—200GAUI-8 and 400GAUI-16 chip-to-module recommended CTLE, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.400.15:5	Reserved	Value always 0	RO
1.400.4:1	Recommended CTLE peaking	4 3 2 1 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = 9 dB 1 0 0 0 = 8 dB 0 1 1 1 = 7 dB 0 1 1 0 = 6 dB 0 1 0 1 = 5 dB 0 1 0 0 = 4 dB 0 0 1 1 = 3 dB 0 0 1 0 = 2 dB 0 0 0 1 = 1 dB 0 0 0 0 = Reserved	R/W
1.400.0	Reserved	Value always 0	RO

[a]R/W = Read/Write, RO = Read only

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45.2.1.132.1 Recommended CTLE peaking (1.400.4:1)

The value of these bits sets the CTLE peaking value recommended for lane 0 by a host that implements the optional 200GAUI-8 or 400GAUI-16 chip-to-module interface defined in Annex 120C (see 120C.3.1). The module may optionally use this information to adjust its CTLE setting.

45.2.1.133 200GAUI-8 and 400GAUI-16 chip-to-module recommended CTLE, lane 1 through lane 7 registers (Registers 1.401 through 1.407)

The 200GAUI-8 and 400GAUI-16 chip-to-module recommended CTLE, lane 1 through lane 7 registers are defined similarly to register 1.400 (which is used for lane 0, see 45.2.1.111) but for lanes 1 through 7, respectively.

45.2.1.134 400GAUI-16 chip-to-module recommended CTLE, lane 8 through lane 15 registers (Registers 1.408 through 1.415)

The 400GAUI-16 chip-to-module recommended CTLE, lane 8 through lane 15 registers are defined similarly to register 1.400 (which is used for lane 0, see 45.2.1.111) but for lanes 8 through 15, respectively.

45.2.1.135 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register (Register 1.500)

The assignment of bits in the 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register is shown in Table 45–107. The transmitter, receive direction, is the transmitter that sends data towards the MAC.

Table 45–107—50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.500.15	Request flag	1 = Change in equalization is requested 0 = No change in equalization is requested	RO
1.500.14:12	Post-cursor request	14 13 12 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Requested_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Requested_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Requested_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Requested_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Requested_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Requested_eq_c1* = 0 (c(1) ratio 0)	RO
1.500.11:10	Pre-cursor request	11 10 1 1 *Requested_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Requested_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Requested_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Requested_eq_cm1* = 0 (c(–1) ratio 0)	RO

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Table 45–107—50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.500.9:7	Post-cursor remote setting	9 8 7 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Remote_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Remote_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Remote_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Remote_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Remote_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Remote_eq_c1* = 0 (c(1) ratio 0)	R/W
1.500.6:5	Pre-cursor remote setting	6 5 1 1 *Remote_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Remote_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Remote_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Remote_eq_cm1* = 0 (c(–1) ratio 0)	R/W
1.500.4:2	Post-cursor local setting	4 3 2 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Local_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Local_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Local_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Local_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Local_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Local_eq_c1* = 0 (c(1) ratio 0)	R/W
1.500.1:0	Pre-cursor local setting	1 0 1 1 *Local_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Local_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Local_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Local_eq_cm1* = 0 (c(–1) ratio 0)	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.135.1 Request flag (1.500.15)

The value of this bit indicates the value of the variable *Request_flag* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). This indicates whether the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip device is issuing a request to change the remote transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the receive direction. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction is not present in the package, then the value returned for this bit should be zero.

45.2.1.135.2 Post-cursor request (1.500.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to one, this value indicates the ratio of the post-cursor coefficient c(1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the receive direction.

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45.2.1.135.3 Pre-cursor request (1.500.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to one, this value indicates the ratio of the pre-cursor coefficient c(–1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the receive direction.

45.2.1.135.4 Post-cursor remote setting (1.500.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient c(1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and 120D.3.1.5). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.135.5 Pre-cursor remote setting (1.500.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient c(–1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and 120D.3.1.5). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.135.6 Post-cursor local setting (1.500.4:2)

The value of these bits sets the variable *Local_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and 120D.3.1.5), which controls the weight of the transmitter equalization post-cursor coefficient c(1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.135.7 Pre-cursor local setting (1.500.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction (see 120B.3.1 and 120D.3.1.5), which controls the weight of the transmitter equalization pre-cursor coefficient c(–1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.136 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 1 through lane 15 registers (Registers 1.501 through 1.515)

The 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 1 through lane 15 registers are defined similarly to register 1.500 (which is used for lane 0, see 45.2.1.135) but for lanes 1 through 15, respectively. The transmitter, receive direction, is the transmitter that sends data towards the MAC.

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45.2.1.137 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register (Register 1.516)

The assignment of bits in the 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register is shown in Table 45–108. The transmitter, transmit direction, is the transmitter that sends data towards the PMD.

Table 45–108—50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.516.15	Request flag	1 = Change in equalization is requested 0 = No change in equalization is requested	RO
1.516.14:12	Post-cursor request	14 13 12 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Requested_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Requested_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Requested_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Requested_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Requested_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Requested_eq_c1* = 0 (c(1) ratio 0)	RO
1.516.11:10	Pre-cursor request	11 10 1 1 *Requested_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Requested_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Requested_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Requested_eq_cm1* = 0 (c(–1) ratio 0)	RO
1.516.9:7	Post-cursor remote setting	9 8 7 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Remote_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Remote_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Remote_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Remote_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Remote_eq_c1* = 1 (c(1) ratio –0.05) 0 0 0 *Remote_eq_c1* = 0 (c(1) ratio 0)	R/W
1.516.6:5	Pre-cursor remote setting	6 5 1 1 *Remote_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Remote_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Remote_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Remote_eq_cm1* = 0 (c(–1) ratio 0)	R/W
1.516.4:2	Post-cursor local setting	4 3 2 1 1 1 Reserved 1 1 0 Reserved 1 0 1 *Local_eq_c1* = 5 (c(1) ratio –0.25) 1 0 0 *Local_eq_c1* = 4 (c(1) ratio –0.2) 0 1 1 *Local_eq_c1* = 3 (c(1) ratio –0.15) 0 1 0 *Local_eq_c1* = 2 (c(1) ratio –0.1) 0 0 1 *Local_eq_c1* = 1 (c(1) ratio–0.05) 0 0 0 *Local_eq_c1* = 0 (c(1) ratio 0)	R/W
1.516.1:0	Pre-cursor local setting	1 0 1 1 *Local_eq_cm1* = 3 (c(–1) ratio –0.15) 1 0 *Local_eq_cm1* = 2 (c(–1) ratio –0.1) 0 1 *Local_eq_cm1* = 1 (c(–1) ratio –0.05) 0 0 *Local_eq_cm1* = 0 (c(–1) ratio 0)	R/W

[a]R/W = Read/Write, RO = Read only

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45.2.1.137.1 Request flag (1.516.15)

The value of this bit indicates the value of the variable *Request_flag* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). This indicates whether the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip device is issuing a request to change the remote transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the transmit direction. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction is not present in the package, then the value returned for this bit should be zero.

45.2.1.137.2 Post-cursor request (1.516.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to one, this value indicates the ratio of the post-cursor coefficient c(1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the transmit direction.

45.2.1.137.3 Pre-cursor request (1.516.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). When *Request_flag* is equal to one, this value indicates the ratio of the pre-cursor coefficient c(–1), which is requested for the transmitter equalization in the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n chip-to-chip lane 0 transmitter in the transmit direction.

45.2.1.137.4 Post-cursor remote setting (1.516.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient c(1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.5). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.137.5 Pre-cursor remote setting (1.516.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction (see 120B.3.2 and 120D.3.2.3). This is used by a 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient c(–1) being used in lane 0 of the 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.5). It may be used to generate values for the request flag and the request bits. If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.137.6 Post-cursor local setting (1.516.4:2)

The value of these bits sets the variable *Local_eq_c1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.5), which controls the weight of the transmitter equalization post-cursor coefficient c(1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n,

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or 400GAUI-n transmitter in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.137.7 Pre-cursor local setting (1.516.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction (see 120B.3.1 and 120D.3.1.5), which controls the weight of the transmitter equalization pre-cursor coefficient c(–1). If a lane 0 50GAUI-n, 100GAUI-2, 200GAUI-n, or 400GAUI-n transmitter in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.138 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 15 registers (Registers 1.517 through 1.531)

The 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 15 registers are defined similarly to register 1.516 (which is used for lane 0, see 45.2.1.137) but for lanes 1 through 15, respectively. The transmitter, transmit direction, is the transmitter that sends data towards the PMD.

45.2.1.139 PMA precoder control Tx output (Register 1.600)

The assignment of bits in the PMA precoder control Tx output register is shown in Table 45–109.

Table 45–109—PMA precoder control Tx output register bit definitions

Bit(s)	Name	Description	R/W[a]
1.600.15:4	Reserved	Value always 0	RO
1.600.3	Lane 3 Tx output precoder enable	1 = Lane 3 Tx output precoder enabled 0 = Lane 3 Tx output precoder disabled	R/W
1.600.2	Lane 2 Tx output precoder enable	1 = Lane 2 Tx output precoder enabled 0 = Lane 2 Tx output precoder disabled	R/W
1.600.1	Lane 1 Tx output precoder enable	1 = Lane 1 Tx output precoder enabled 0 = Lane 1 Tx output precoder disabled	R/W
1.600.0	Lane 0 Tx output precoder enable	1 = Lane 0 Tx output precoder enabled 0 = Lane 0 Tx output precoder disabled	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.139.1 Lane 3 Tx output precoder enable (1.600.3)

This bit enables the lane 3 Tx output precoder.

45.2.1.139.2 Lane 2 Tx output precoder enable (1.600.2)

This bit enables the lane 2 Tx output precoder.

45.2.1.139.3 Lane 1 Tx output precoder enable (1.600.1)

This bit enables the lane 1 Tx output precoder.

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45.2.1.139.4 Lane 0 Tx output precoder enable (1.600.0)

This bit enables the lane 0 Tx output precoder.

45.2.1.140 PMA precoder control Rx input (Register 1.601)

The assignment of bits in the precoder control Rx input register is shown in Table 45–110.

Table 45–110—PMA precoder control Rx input register bit definitions

Bit(s)	Name	Description	R/W[a]
1.601.15:4	Reserved	Value always 0	RO
1.601.3	Lane 3 Rx input precoder enable	1 = Lane 3 Rx input precoder enabled 0 = Lane 3 Rx input precoder disabled	R/W
1.601.2	Lane 2 Rx input precoder enable	1 = Lane 2 Rx input precoder enabled 0 = Lane 2 Rx input precoder disabled	R/W
1.601.1	Lane 1 Rx input precoder enable	1 = Lane 1 Rx input precoder enabled 0 = Lane 1 Rx input precoder disabled	R/W
1.601.0	Lane 0 Rx input precoder enable	1 = Lane 0 Rx input precoder enabled 0 = Lane 0 Rx input precoder disabled	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.140.1 Lane 3 Rx input precoder enable (1.601.3)

This bit enables the lane 3 Rx input precoder.

45.2.1.140.2 Lane 2 Rx input precoder enable (1.601.2)

This bit enables the lane 2 Rx input precoder.

45.2.1.140.3 Lane 1 Rx input precoder enable (1.601.1)

This bit enables the lane 1 Rx input precoder.

45.2.1.140.4 Lane 0 Rx input precoder enable (1.601.0)

This bit enables the lane 0 Rx input precoder.

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45.2.1.141 PMA precoder control Rx output (Register 1.602)

The assignment of bits in the precoder control Rx output register is shown in Table 45–111.

Table 45–111—PMA precoder control Rx output register bit definitions

Bit(s)	Name	Description	R/W[a]
1.602.15:2	Reserved	Value always 0	RO
1.602.1	Lane 1 Rx output precoder enable	1 = Lane 1 Rx output precoder enabled 0 = Lane 1 Rx output precoder disabled	R/W
1.602.0	Lane 0 Rx output precoder enable	1 = Lane 0 Rx output precoder enabled 0 = Lane 0 Rx output precoder disabled	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.141.1 Lane 1 Rx output precoder enable (1.602.1)

This bit enables the lane 1 Rx output precoder.

45.2.1.141.2 Lane 0 Rx output precoder enable (1.602.0)

This bit enables the lane 0 Rx output precoder.

45.2.1.142 PMA precoder control Tx input (Register 1.603)

The assignment of bits in the precoder control Tx input register is shown in Table 45–112.

Table 45–112—PMA precoder control Tx input register bit definitions

Bit(s)	Name	Description	R/W[a]
1.603.15:2	Reserved	Value always 0	RO
1.603.1	Lane 1 Tx input precoder enable	1 = Lane 1 Tx input precoder enabled 0 = Lane 1 Tx input precoder disabled	R/W
1.603.0	Lane 0 Tx input precoder enable	1 = Lane 0 Tx input precoder enabled 0 = Lane 0 Tx input precoder disabled	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.142.1 Lane 1 Tx input precoder enable (1.603.1)

This bit enables the lane 1 Tx input precoder.

45.2.1.142.2 Lane 0 Tx input precoder enable (1.603.0)

This bit enables the lane 0 Tx input precoder.

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45.2.1.143 PMA precoder request flag (Register 1.604)

The assignment of bits in the precoder request flag register is shown in Table 45–113.

Table 45–113—PMA precoder request flag register bit definitions

Bit(s)	Name	Description	R/W[a]
1.604.15:2	Reserved	Value always 0	RO
1.604.1	Tx input precoder request flag	1 = Tx input precoding change requested 0 = Tx input precoding no change requested	RO
1.604.0	Rx input precoder request flag	1 = Rx input precoding change requested 0 = Rx input precoding no change requested	RO

[a]RO = Read only

45.2.1.143.1 Tx input precoder request flag (1.604.1)

This bit indicates the Tx input precoder request flag.

45.2.1.143.2 Rx input precoder request flag (1.604.0)

This bit indicates the Rx input precoder request flag.

45.2.1.144 PMA precoder request Rx input status (Register 1.605)

The assignment of bits in the precoder request Rx input status register is shown in Table 45–114.

Table 45–114—PMA precoder request Rx input status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.605.15:2	Reserved	Value always 0	RO
1.605.1	Lane 1 Rx input precoder request status	1 = Lane 1 precoder Rx input requested 0 = Lane 1 precoder Rx input not requested	RO
1.605.0	Lane 0 Rx input precoder request status	1 = Lane 0 precoder Rx input requested 0 = Lane 0 precoder Rx input not requested	RO

[a]RO = Read only

45.2.1.144.1 Lane 1 Rx input precoder request status (1.605.1)

This bit indicates the Rx input precoder request status for lane 1.

45.2.1.144.2 Lane 0 Rx input precoder request status (1.605.0)

This bit indicates the Rx input precoder request status for lane 0.

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45.2.1.145 PMA precoder request Tx input status (Register 1.606)

The assignment of bits in the precoder request Tx input status register is shown in Table 45–115.

Table 45–115—PMA precoder request Tx input status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.606.15:2	Reserved	Value always 0	RO
1.606.1	Lane 1 Tx input precoder request status	1 = Lane 1 precoder Tx input requested 0 = Lane 1 precoder Tx input not requested	RO
1.606.0	Lane 0 Tx input precoder request status	1 = Lane 0 precoder Tx input requested 0 = Lane 0 precoder Tx input not requested	RO

[a]RO = Read only

45.2.1.145.1 Lane 1 Tx input precoder request status(1.606.1)

This bit indicates the Tx input precoder request status for lane 1.

45.2.1.145.2 Lane 0 Tx input precoder request status (1.606.0)

This bit indicates the Tx input precoder request status for lane 0.

45.2.1.146 RS-FEC degraded SER activate threshold register (Register 1.650, 1.651)

The assignment of bits in the RS-FEC degraded SER activate threshold register is shown in Table 45–116. The value controls the threshold used to set the FEC degraded SER bit (1.201.4) as defined in 91.5.3.3.1 and 134.5.3.3.2.

Table 45–116—RS-FEC degraded SER activate threshold register bit definitions

Bit(s)	Name	Description	R/W[a]
1.650.15:0	FEC degraded SER activate threshold lower	FEC_degraded_SER_activate_threshold[15:0]	R/W
1.651.15:0	FEC degraded SER activate threshold upper	FEC_degraded_SER_activate_threshold[31:16]	R/W

[a]R/W = Read/Write

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45.2.1.147 RS-FEC degraded SER deactivate threshold register (Register 1.652, 1.653)

The assignment of bits in the RS-FEC degraded SER deactivate threshold register is shown in Table 45–117. The value controls the threshold used to clear the FEC degraded SER bit (1.201.4) as defined in 91.5.3.3.1 and 134.5.3.3.2.

Table 45–117—RS-FEC degraded SER deactivate threshold register bit definitions

Bit(s)	Name	Description	R/W[a]
1.652.15:0	FEC degraded SER deactivate threshold lower	FEC_degraded_SER_deactivate_threshold[15:0]	R/W
1.653.15:0	FEC degraded SER deactivate threshold upper	FEC_degraded_SER_deactivate_threshold[31:16]	R/W

[a]R/W = Read/Write

45.2.1.148 RS-FEC degraded SER interval register (Register 1.654, 1.655)

The assignment of bits in the RS-FEC degraded SER interval register is shown in Table 45–118. The value controls the interval used to set and clear the FEC degraded SER bit (1.201.4) as defined in 91.5.3.3.1 and 134.5.3.3.2.

Table 45–118—RS-FEC degraded SER interval register bit definitions

Bit(s)	Name	Description	R/W[a]
1.654.15:0	FEC degraded SER interval lower	FEC_degraded_SER_interval[15:0]	R/W
1.655.15:0	FEC degraded SER interval upper	FEC_degraded_SER_interval[31:16]	R/W

[a]R/W = Read/Write

45.2.1.149 BASE-R FEC uncorrected blocks counter, lanes 0 through 19

(Register 1.700, 1.701, 1.702, 1.703, 1.704, 1.705, 1.706, 1.707, 1.708, 1.709, 1.710, 1.711, 1.712, 1.713, 1.714, 1.715, 1.716, 1.717, 1.718, 1.719, 1.720, 1.721, 1.722, 1.723, 1.724, 1.725, 1.726, 1.727, 1.728, 1.729, 1.730, 1.731, 1.732, 1.733, 1.734, 1.735, 1.736, 1.737, 1.738, 1.739)

For multi-PCS lane BASE-R PHYs, the even-numbered registers in this set are defined similarly to register 1.174 (see 45.2.1.110) but for lanes 0 through 19 respectively of multi-PCS lane PHYs. The odd-numbered registers in this set are defined similarly to register 1.175 (see 45.2.1.110) but for lanes 0 through 19 respectively of multilane PHYs. Note that the lane numbers refer to the service interface lanes and do not necessarily correspond to the PCS lane numbers.

Registers corresponding to lanes that are not used for the selected PHY shall return all zeros.

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45.2.1.150 Tx optical channel control register (Register 1.800)

The assignment of bits in the Tx optical channel control register is shown in Table 45–119.

Table 45–119—Tx optical channel control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.800.15:6	Reserved	Value always 0	RO
1.800.5:0	Tx optical channel index	Integer value of the Tx optical channel index	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.150.1 Tx optical channel index (1.800.5:0)

Bits 1.800.5:0 set the value of the Tx optical channel index (which directly relates to the optical channel and transmitter center frequency) with bit 1.800.0 being the LSB and bit 1.800.5 being the MSB. The channel index number indicates the corresponding optical frequency. For 100GBASE-ZR the specific optical frequency corresponding to each channel index number is listed in Table 154–5.

45.2.1.151 Tx optical channel ability 1 register (Register 1.801)

The assignment of bits in the Tx optical channel ability 1 register is shown in Table 45–120.

Table 45–120—Tx optical channel ability 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.801.15	Tx index ability 15	1 = PMD is able to operate with Tx optical channel index = 15 0 = PMD is not able to operate with Tx optical channel index = 15	RO
1.801.14	Tx index ability 14	1 = PMD is able to operate with Tx optical channel index = 14 0 = PMD is not able to operate with Tx optical channel index = 14	RO
1.801.13	Tx index ability 13	1 = PMD is able to operate with Tx optical channel index = 13 0 = PMD is not able to operate with Tx optical channel index = 13	RO
1.801.12	Tx index ability 12	1 = PMD is able to operate with Tx optical channel index = 12 0 = PMD is not able to operate with Tx optical channel index = 12	RO
1.801.11	Tx index ability 11	1 = PMD is able to operate with Tx optical channel index = 11 0 = PMD is not able to operate with Tx optical channel index = 11	RO
1.801.10	Tx index ability 10	1 = PMD is able to operate with Tx optical channel index = 10 0 = PMD is not able to operate with Tx optical channel index = 10	RO
1.801.9	Tx index ability 9	1 = PMD is able to operate with Tx optical channel index = 9 0 = PMD is not able to operate with Tx optical channel index = 9	RO
1.801.8	Tx index ability 8	1 = PMD is able to operate with Tx optical channel index = 8 0 = PMD is not able to operate with Tx optical channel index = 8	RO
1.801.7	Tx index ability 7	1 = PMD is able to operate with Tx optical channel index = 7 0 = PMD is not able to operate with Tx optical channel index = 7	RO
1.801.6	Tx index ability 6	1 = PMD is able to operate with Tx optical channel index = 6 0 = PMD is not able to operate with Tx optical channel index = 6	RO

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Table 45–120—Tx optical channel ability 1 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.801.5	Tx index ability 5	1 = PMD is able to operate with Tx optical channel index = 5 0 = PMD is not able to operate with Tx optical channel index = 5	RO
1.801.4	Tx index ability 4	1 = PMD is able to operate with Tx optical channel index = 4 0 = PMD is not able to operate with Tx optical channel index = 4	RO
1.801.3	Tx index ability 3	1 = PMD is able to operate with Tx optical channel index = 3 0 = PMD is not able to operate with Tx optical channel index = 3	RO
1.801.2	Tx index ability 2	1 = PMD is able to operate with Tx optical channel index = 2 0 = PMD is not able to operate with Tx optical channel index = 2	RO
1.801.1	Tx index ability 1	1 = PMD is able to operate with Tx optical channel index = 1 0 = PMD is not able to operate with Tx optical channel index = 1	RO
1.801.0	Tx index ability 0	1 = PMD is able to operate with Tx optical channel index = 0 0 = PMD is not able to operate with Tx optical channel index = 0	RO

[a]RO = Read only

45.2.1.151.1 Tx index ability 0 through 15 (1.801.0 through 1.801.15)

When read as a one, bit 1.801.0 indicates that the PMD selected by bits 1.7.6:0 is able to operate with a Tx optical channel index of 0. When read as a zero, bit 1.801.0 indicates that the PMD is not able to operate with a Tx optical channel index of 0. Bits 1.801.1 through 1.801.15 indicate the equivalent for index values 1 through 15, respectively. The optical frequencies that correspond to these index values are given in the appropriate PMD clause. For 100GBASE-ZR see Table 154–5.

45.2.1.152 Tx optical channel ability 2 register (Register 1.802)

The assignment of bits in the Tx optical channel ability 2 register is shown in Table 45–121.

Table 45–121—Tx optical channel ability 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.802.15	Tx index ability 31	1 = PMD is able to operate with Tx optical channel index = 31 0 = PMD is not able to operate with Tx optical channel index = 31	RO
1.802.14	Tx index ability 30	1 = PMD is able to operate with Tx optical channel index = 30 0 = PMD is not able to operate with Tx optical channel index = 30	RO
1.802.13	Tx index ability 29	1 = PMD is able to operate with Tx optical channel index = 29 0 = PMD is not able to operate with Tx optical channel index = 29	RO
1.802.12	Tx index ability 28	1 = PMD is able to operate with Tx optical channel index = 28 0 = PMD is not able to operate with Tx optical channel index = 28	RO
1.802.11	Tx index ability 27	1 = PMD is able to operate with Tx optical channel index = 27 0 = PMD is not able to operate with Tx optical channel index = 27	RO
1.802.10	Tx index ability 26	1 = PMD is able to operate with Tx optical channel index = 26 0 = PMD is not able to operate with Tx optical channel index = 26	RO
1.802.9	Tx index ability 25	1 = PMD is able to operate with Tx optical channel index = 25 0 = PMD is not able to operate with Tx optical channel index = 25	RO

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Table 45–121—Tx optical channel ability 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.802.8	Tx index ability 24	1 = PMD is able to operate with Tx optical channel index = 24 0 = PMD is not able to operate with Tx optical channel index = 24	RO
1.802.7	Tx index ability 23	1 = PMD is able to operate with Tx optical channel index = 23 0 = PMD is not able to operate with Tx optical channel index = 23	RO
1.802.6	Tx index ability 22	1 = PMD is able to operate with Tx optical channel index = 22 0 = PMD is not able to operate with Tx optical channel index = 22	RO
1.802.5	Tx index ability 21	1 = PMD is able to operate with Tx optical channel index = 21 0 = PMD is not able to operate with Tx optical channel index = 21	RO
1.802.4	Tx index ability 20	1 = PMD is able to operate with Tx optical channel index = 20 0 = PMD is not able to operate with Tx optical channel index = 20	RO
1.802.3	Tx index ability 19	1 = PMD is able to operate with Tx optical channel index = 19 0 = PMD is not able to operate with Tx optical channel index = 19	RO
1.802.2	Tx index ability 18	1 = PMD is able to operate with Tx optical channel index = 18 0 = PMD is not able to operate with Tx optical channel index = 18	RO
1.802.1	Tx index ability 17	1 = PMD is able to operate with Tx optical channel index = 17 0 = PMD is not able to operate with Tx optical channel index = 17	RO
1.802.0	Tx index ability 16	1 = PMD is able to operate with Tx optical channel index = 16 0 = PMD is not able to operate with Tx optical channel index = 16	RO

[a]RO = Read only

45.2.1.152.1 Tx index ability 16 through 31 (1.802.0 through 1.802.15)

When read as a one, bit 1.802.0 indicates that the PMD selected by bits 1.7.6:0 is able to operate with a Tx optical channel index of 16. When read as a zero, bit 1.802.0 indicates that the PMD is not able to operate with a Tx optical channel index of 16. Bits 1.802.1 through 1.802.15 indicate the equivalent for index values 17 through 31, respectively. The optical frequencies that correspond to these index values are given in the appropriate PMD clause. For 100GBASE-ZR see Table 154–5.

45.2.1.153 Tx optical channel ability 3 register (Register 1.803)

The assignment of bits in the Tx optical channel ability 3 register is shown in Table 45–122.

Table 45–122—Tx optical channel ability 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.803.15	Tx index ability 47	1 = PMD is able to operate with Tx optical channel index = 47 0 = PMD is not able to operate with Tx optical channel index = 47	RO
1.803.14	Tx index ability 46	1 = PMD is able to operate with Tx optical channel index = 46 0 = PMD is not able to operate with Tx optical channel index = 46	RO
1.803.13	Tx index ability 45	1 = PMD is able to operate with Tx optical channel index = 45 0 = PMD is not able to operate with Tx optical channel index = 45	RO
1.803.12	Tx index ability 44	1 = PMD is able to operate with Tx optical channel index = 44 0 = PMD is not able to operate with Tx optical channel index = 44	RO

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Table 45–122—Tx optical channel ability 3 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.803.11	Tx index ability 43	1 = PMD is able to operate with Tx optical channel index = 43 0 = PMD is not able to operate with Tx optical channel index = 43	RO
1.803.10	Tx index ability 42	1 = PMD is able to operate with Tx optical channel index = 42 0 = PMD is not able to operate with Tx optical channel index = 42	RO
1.803.9	Tx index ability 41	1 = PMD is able to operate with Tx optical channel index = 41 0 = PMD is not able to operate with Tx optical channel index = 41	RO
1.803.8	Tx index ability 40	1 = PMD is able to operate with Tx optical channel index = 40 0 = PMD is not able to operate with Tx optical channel index = 40	RO
1.803.7	Tx index ability 39	1 = PMD is able to operate with Tx optical channel index = 39 0 = PMD is not able to operate with Tx optical channel index = 39	RO
1.803.6	Tx index ability 38	1 = PMD is able to operate with Tx optical channel index = 38 0 = PMD is not able to operate with Tx optical channel index = 38	RO
1.803.5	Tx index ability 37	1 = PMD is able to operate with Tx optical channel index = 37 0 = PMD is not able to operate with Tx optical channel index = 37	RO
1.803.4	Tx index ability 36	1 = PMD is able to operate with Tx optical channel index = 36 0 = PMD is not able to operate with Tx optical channel index = 36	RO
1.803.3	Tx index ability 35	1 = PMD is able to operate with Tx optical channel index = 35 0 = PMD is not able to operate with Tx optical channel index = 35	RO
1.803.2	Tx index ability 34	1 = PMD is able to operate with Tx optical channel index = 34 0 = PMD is not able to operate with Tx optical channel index = 34	RO
1.803.1	Tx index ability 33	1 = PMD is able to operate with Tx optical channel index = 33 0 = PMD is not able to operate with Tx optical channel index = 33	RO
1.803.0	Tx index ability 32	1 = PMD is able to operate with Tx optical channel index = 32 0 = PMD is not able to operate with Tx optical channel index = 32	RO

[a]RO = Read only

45.2.1.153.1 Tx index ability 32 through 47 (1.803.0 through 1.803.15)

When read as a one, bit 1.803.0 indicates that the PMD selected by bits 1.7.6:0 is able to operate with a Tx optical channel index of 32. When read as a zero, bit 1.803.0 indicates that the PMD is not able to operate with a Tx optical channel index of 32. Bits 1.803.1 through 1.803.15 indicate the equivalent for index values 33 through 47, respectively. The optical frequencies that correspond to these index values are given in the appropriate PMD clause. For 100GBASE-ZR see Table 154–5.

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45.2.1.154 Rx optical channel control register (Register 1.820)

The assignment of bits in the Rx optical channel control register is shown in Table 45–123.

Table 45–123—Rx optical channel control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.820.15	Tx Rx different optical channel ability	1 = PMD is able to operate with different Tx and Rx optical channels 0 = PMD is not able to operate with different Tx and Rx optical channels	RO
1.820.14:6	Reserved	Value always 0	RO
1.820.5:0	Rx optical channel index	Integer value of the Rx optical channel index	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.154.1 Tx Rx different optical channel ability (1.820.15)

When read as a one, bit 1.820.15 indicates that the PMD is able to operate with an Rx optical channel index that is different from the Tx optical channel index. When read as a zero, bit 1.820.15 indicates that the PMD is not able to operate with an Rx optical channel index that is different from the Tx optical channel index.

45.2.1.154.2 Rx optical channel index (1.820.5:0)

If the PMD is able to operate with an Rx optical channel index number that is different from the Tx optical channel index number (bit 1.820.15 is one), bits 1.820.5:0 set the value of the Rx optical channel index number (and hence the receiver optical frequency) with bit 1.820.0 being the LSB and bit 1.820.5 being the MSB. The channel index number indicates the corresponding optical frequency. For 100GBASE-ZR the specific optical frequency corresponding to each channel index number is listed in Table 154–5. If the PMD is not able to operate with an Rx optical channel index that is different from the Tx optical channel index (bit 1.820.15 is zero), bits 1.820.5:0 have no effect and the value of the Rx optical channel index is the same as the value of the Tx optical channel index as set by bits 1.800.5:0.

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45.2.1.155 Rx optical channel ability 1 register (Register 1.821)

The assignment of bits in the Rx optical channel ability 1 register is shown in Table 45–124.

Table 45–124—Rx optical channel ability 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.821.15	Rx index ability 15	1 = PMD is able to operate with Rx optical channel index = 15 0 = PMD is not able to operate with Rx optical channel index = 15	RO
1.821.14	Rx index ability 14	1 = PMD is able to operate with Rx optical channel index = 14 0 = PMD is not able to operate with Rx optical channel index = 14	RO
1.821.13	Rx index ability 13	1 = PMD is able to operate with Rx optical channel index = 13 0 = PMD is not able to operate with Rx optical channel index = 13	RO
1.821.12	Rx index ability 12	1 = PMD is able to operate with Rx optical channel index = 12 0 = PMD is not able to operate with Rx optical channel index = 12	RO
1.821.11	Rx index ability 11	1 = PMD is able to operate with Rx optical channel index = 11 0 = PMD is not able to operate with Rx optical channel index = 11	RO
1.821.10	Rx index ability 10	1 = PMD is able to operate with Rx optical channel index = 10 0 = PMD is not able to operate with Rx optical channel index = 10	RO
1.821.9	Rx index ability 9	1 = PMD is able to operate with Rx optical channel index = 9 0 = PMD is not able to operate with Rx optical channel index = 9	RO
1.821.8	Rx index ability 8	1 = PMD is able to operate with Rx optical channel index = 8 0 = PMD is not able to operate with Rx optical channel index = 8	RO
1.821.7	Rx index ability 7	1 = PMD is able to operate with Rx optical channel index = 7 0 = PMD is not able to operate with Rx optical channel index = 7	RO
1.821.6	Rx index ability 6	1 = PMD is able to operate with Rx optical channel index = 6 0 = PMD is not able to operate with Rx optical channel index = 6	RO
1.821.5	Rx index ability 5	1 = PMD is able to operate with Rx optical channel index = 5 0 = PMD is not able to operate with Rx optical channel index = 5	RO
1.821.4	Rx index ability 4	1 = PMD is able to operate with Rx optical channel index = 4 0 = PMD is not able to operate with Rx optical channel index = 4	RO
1.821.3	Rx index ability 3	1 = PMD is able to operate with Rx optical channel index = 3 0 = PMD is not able to operate with Rx optical channel index = 3	RO
1.821.2	Rx index ability 2	1 = PMD is able to operate with Rx optical channel index = 2 0 = PMD is not able to operate with Rx optical channel index = 2	RO
1.821.1	Rx index ability 1	1 = PMD is able to operate with Rx optical channel index = 1 0 = PMD is not able to operate with Rx optical channel index = 1	RO
1.821.0	Rx index ability 0	1 = PMD is able to operate with Rx optical channel index = 0 0 = PMD is not able to operate with Rx optical channel index = 0	RO

[a]RO = Read only

45.2.1.155.1 Rx index ability 0 through 15 (1.821.0 through 1.821.15)

When read as a one, bit 1.821.0 indicates that the PMD selected by bits 1.7.6:0 is able to operate with an Rx optical channel index of 0. When read as a zero, bit 1.821.0 indicates that the PMD is not able to operate with an Rx optical channel index of 0. Bits 1.821.1 through 1.821.15 indicate the equivalent for index values

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1 through 15, respectively. The optical frequencies that correspond to these index values are given in the appropriate PMD clause. For 100GBASE-ZR see Table 154–5.

45.2.1.156 Rx optical channel ability 2 register (Register 1.822)

The assignment of bits in the Rx optical channel ability 2 register is shown in Table 45–125.

Table 45–125—Rx optical channel ability 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.822.15	Rx index ability 31	1 = PMD is able to operate with Rx optical channel index = 31 0 = PMD is not able to operate with Rx optical channel index = 31	RO
1.822.14	Rx index ability 30	1 = PMD is able to operate with Rx optical channel index = 30 0 = PMD is not able to operate with Rx optical channel index = 30	RO
1.822.13	Rx index ability 29	1 = PMD is able to operate with Rx optical channel index = 29 0 = PMD is not able to operate with Rx optical channel index = 29	RO
1.822.12	Rx index ability 28	1 = PMD is able to operate with Rx optical channel index = 28 0 = PMD is not able to operate with Rx optical channel index = 28	RO
1.822.11	Rx index ability 27	1 = PMD is able to operate with Rx optical channel index = 27 0 = PMD is not able to operate with Rx optical channel index = 27	RO
1.822.10	Rx index ability 26	1 = PMD is able to operate with Rx optical channel index = 26 0 = PMD is not able to operate with Rx optical channel index = 26	RO
1.822.9	Rx index ability 25	1 = PMD is able to operate with Rx optical channel index = 25 0 = PMD is not able to operate with Rx optical channel index = 25	RO
1.822.8	Rx index ability 24	1 = PMD is able to operate with Rx optical channel index = 24 0 = PMD is not able to operate with Rx optical channel index = 24	RO
1.822.7	Rx index ability 23	1 = PMD is able to operate with Rx optical channel index = 23 0 = PMD is not able to operate with Rx optical channel index = 23	RO
1.822.6	Rx index ability 22	1 = PMD is able to operate with Rx optical channel index = 22 0 = PMD is not able to operate with Rx optical channel index = 22	RO
1.822.5	Rx index ability 21	1 = PMD is able to operate with Rx optical channel index = 21 0 = PMD is not able to operate with Rx optical channel index = 21	RO
1.822.4	Rx index ability 20	1 = PMD is able to operate with Rx optical channel index = 20 0 = PMD is not able to operate with Rx optical channel index = 20	RO
1.822.3	Rx index ability 19	1 = PMD is able to operate with Rx optical channel index = 19 0 = PMD is not able to operate with Rx optical channel index = 19	RO
1.822.2	Rx index ability 18	1 = PMD is able to operate with Rx optical channel index = 18 0 = PMD is not able to operate with Rx optical channel index = 18	RO
1.822.1	Rx index ability 17	1 = PMD is able to operate with Rx optical channel index = 17 0 = PMD is not able to operate with Rx optical channel index = 17	RO
1.822.0	Rx index ability 16	1 = PMD is able to operate with Rx optical channel index = 16 0 = PMD is not able to operate with Rx optical channel index = 16	RO

[a]RO = Read only

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45.2.1.156.1 Rx index ability 16 through 31 (1.822.0 through 1.822.15)

When read as a one, bit 1.822.0 indicates that the PMD selected by bits 1.7.6:0 is able to operate with an Rx optical channel index of 16. When read as a zero, bit 1.822.0 indicates that the PMD is not able to operate with an Rx optical channel index of 16. Bits 1.822.1 through 1.822.15 indicate the equivalent for index values 17 through 31, respectively. The optical frequencies that correspond to these index values are given in the appropriate PMD clause. For 100GBASE-ZR see Table 154–5.

45.2.1.157 Rx optical channel ability 3 register (Register 1.823)

The assignment of bits in the Rx optical channel ability 3 register is shown in Table 45–126.

Table 45–126—Rx optical channel ability 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.823.15	Rx index ability 47	1 = PMD is able to operate with Rx optical channel index = 47 0 = PMD is not able to operate with Rx optical channel index = 47	RO
1.823.14	Rx index ability 46	1 = PMD is able to operate with Rx optical channel index = 46 0 = PMD is not able to operate with Rx optical channel index = 46	RO
1.823.13	Rx index ability 45	1 = PMD is able to operate with Rx optical channel index = 45 0 = PMD is not able to operate with Rx optical channel index = 45	RO
1.823.12	Rx index ability 44	1 = PMD is able to operate with Rx optical channel index = 44 0 = PMD is not able to operate with Rx optical channel index = 44	RO
1.823.11	Rx index ability 43	1 = PMD is able to operate with Rx optical channel index = 43 0 = PMD is not able to operate with Rx optical channel index = 43	RO
1.823.10	Rx index ability 42	1 = PMD is able to operate with Rx optical channel index = 42 0 = PMD is not able to operate with Rx optical channel index = 42	RO
1.823.9	Rx index ability 41	1 = PMD is able to operate with Rx optical channel index = 41 0 = PMD is not able to operate with Rx optical channel index = 41	RO
1.823.8	Rx index ability 40	1 = PMD is able to operate with Rx optical channel index = 40 0 = PMD is not able to operate with Rx optical channel index = 40	RO
1.823.7	Rx index ability 39	1 = PMD is able to operate with Rx optical channel index = 39 0 = PMD is not able to operate with Rx optical channel index = 39	RO
1.823.6	Rx index ability 38	1 = PMD is able to operate with Rx optical channel index = 38 0 = PMD is not able to operate with Rx optical channel index = 38	RO
1.823.5	Rx index ability 37	1 = PMD is able to operate with Rx optical channel index = 37 0 = PMD is not able to operate with Rx optical channel index = 37	RO
1.823.4	Rx index ability 36	1 = PMD is able to operate with Rx optical channel index = 36 0 = PMD is not able to operate with Rx optical channel index = 36	RO
1.823.3	Rx index ability 35	1 = PMD is able to operate with Rx optical channel index = 35 0 = PMD is not able to operate with Rx optical channel index = 35	RO
1.823.2	Rx index ability 34	1 = PMD is able to operate with Rx optical channel index = 34 0 = PMD is not able to operate with Rx optical channel index = 34	RO
1.823.1	Rx index ability 33	1 = PMD is able to operate with Rx optical channel index = 33 0 = PMD is not able to operate with Rx optical channel index = 33	RO
1.823.0	Rx index ability 32	1 = PMD is able to operate with Rx optical channel index = 32 0 = PMD is not able to operate with Rx optical channel index = 32	RO

[a]RO = Read only

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45.2.1.157.1 Rx index ability 32 through 47 (1.823.0 through 1.823.15)

When read as a one, bit 1.823.0 indicates that the PMD selected by bits 1.7.6:0 is able to operate with an Rx optical channel index of 32. When read as a zero, bit 1.823.0 indicates that the PMD is not able to operate with an Rx optical channel index of 32. Bits 1.823.1 through 1.823.15 indicate the equivalent for index values 33 through 47, respectively. The optical frequencies that correspond to these index values are given in the appropriate PMD clause. For 100GBASE-ZR see Table 154–5.

45.2.1.158 BASE-H PMA/PMD control register (Register 1.900)

The assignment of bits in the BASE-H PMA/PMD control register is shown in Table 45–127.

Table 45–127—BASE-H PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.900.15:4	Reserved	Value always 0	RO
1.900.3:0	Type selection	3 2 1 0 1 x x x = Reserved 0 1 x x = Reserved 0 0 1 1 = Reserved 0 0 1 0 = 1000BASE-RHC 0 0 0 1 = 1000BASE-RHB 0 0 0 0 = 1000BASE-RHA	R/W

[a]RO = Read Only, R/W = Read Write

45.2.1.158.1 Type selection (1.900.3:0)

Bits 1.900.3:0 are used to set the mode of operation. When these bits are set to 0000, the mode of operation is 1000BASE-RHA. When these bits are set to 0001, the mode of operation is 1000BASE-RHB. When these bits are set to 0010, the mode of operation is 1000BASE-RHC. Any attempt to configure a different value or a mode of operation not supported per register 1.22 shall have no effect.

45.2.1.159 Nx25G-EPON PMA/PMD extended ability register (Registers 1.1000 through 1.1002)

The assignment of bits in the Nx25G-EPON PMA/PMD extended ability register is shown in Table 45–128.

Table 45–128—Nx25G-EPON PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1000.15	25GBASE-PQX-U3	1 = PMA/PMD is able to perform 25GBASE-PQX-U3 0 = PMA/PMD is not able to perform 25GBASE-PQX-U3	RO
1.1000.14	25GBASE-PQX-U2	1 = PMA/PMD is able to perform 25GBASE-PQX-U2 0 = PMA/PMD is not able to perform 25GBASE-PQX-U2	RO
1.1000.13	25GBASE-PQX-D3	1 = PMA/PMD is able to perform 25GBASE-PQX-D3 0 = PMA/PMD is not able to perform 25GBASE-PQX-D3	RO
1.1000.12	25GBASE-PQX-D2	1 = PMA/PMD is able to perform 25GBASE-PQX-D2 0 = PMA/PMD is not able to perform 25GBASE-PQX-D2	RO

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Table 45–128—Nx25G-EPON PMA/PMD extended ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.1000.11	25GBASE-PQG-U3	1 = PMA/PMD is able to perform 25GBASE-PQG-U3 0 = PMA/PMD is not able to perform 25GBASE-PQG-U3	RO
1.1000.10	25GBASE-PQG-U2	1 = PMA/PMD is able to perform 25GBASE-PQG-U2 0 = PMA/PMD is not able to perform 25GBASE-PQG-U2	RO
1.1000.9	25GBASE-PQG-D3	1 = PMA/PMD is able to perform 25GBASE-PQG-D3 0 = PMA/PMD is not able to perform 25GBASE-PQG-D3	RO
1.1000.8	25GBASE-PQG-D2	1 = PMA/PMD is able to perform 25GBASE-PQG-D2 0 = PMA/PMD is not able to perform 25GBASE-PQG-D2	RO
1.1000.7	25/10GBASE-PQX-U3	1 = PMA/PMD is able to perform 25/10GBASE-PQX-U3 0 = PMA/PMD is not able to perform 25/10GBASE-PQX-U3	RO
1.1000.6	25/10GBASE-PQX-U2	1 = PMA/PMD is able to perform 25/10GBASE-PQX-U2 0 = PMA/PMD is not able to perform 25/10GBASE-PQX-U2	RO
1.1000.5	25/10GBASE-PQX-D3	1 = PMA/PMD is able to perform 25/10GBASE-PQX-D3 0 = PMA/PMD is not able to perform 25/10GBASE-PQX-D3	RO
1.1000.4	25/10GBASE-PQX-D2	1 = PMA/PMD is able to perform 25/10GBASE-PQX-D2 0 = PMA/PMD is not able to perform 25/10GBASE-PQX-D2	RO
1.1000.3	25/10GBASE-PQG-U3	1 = PMA/PMD is able to perform 25/10GBASE-PQG-U3 0 = PMA/PMD is not able to perform 25/10GBASE-PQG-U3	RO
1.1000.2	25/10GBASE-PQG-U2	1 = PMA/PMD is able to perform 25/10GBASE-PQG-U2 0 = PMA/PMD is not able to perform 25/10GBASE-PQG-U2	RO
1.1000.1	25/10GBASE-PQG-D3	1 = PMA/PMD is able to perform 25/10GBASE-PQG-D3 0 = PMA/PMD is not able to perform 25/10GBASE-PQG-D3	RO
1.1000.0	25/10GBASE-PQG-D2	1 = PMA/PMD is able to perform 25/10GBASE-PQG-D2 0 = PMA/PMD is not able to perform 25/10GBASE-PQG-D2	RO
1.1001.15	50/25GBASE-PQX-U3	1 = PMA/PMD is able to perform 50/25GBASE-PQX-U3 0 = PMA/PMD is not able to perform 50/25GBASE-PQX-U3	RO
1.1001.14	50/25GBASE-PQX-U2	1 = PMA/PMD is able to perform 50/25GBASE-PQX-U2 0 = PMA/PMD is not able to perform 50/25GBASE-PQX-U2	RO
1.1001.13	50/25GBASE-PQX-D3	1 = PMA/PMD is able to perform 50/25GBASE-PQX-D3 0 = PMA/PMD is not able to perform 50/25GBASE-PQX-D3	RO
1.1001.12	50/25GBASE-PQX-D2	1 = PMA/PMD is able to perform 50/25GBASE-PQX-D2 0 = PMA/PMD is not able to perform 50/25GBASE-PQX-D2	RO
1.1001.11	50/25GBASE-PQG-U3	1 = PMA/PMD is able to perform 50/25GBASE-PQG-U3 0 = PMA/PMD is not able to perform 50/25GBASE-PQG-U3	RO
1.1001.10	50/25GBASE-PQG-U2	1 = PMA/PMD is able to perform 50/25GBASE-PQG-U2 0 = PMA/PMD is not able to perform 50/25GBASE-PQG-U2	RO
1.1001.9	50/25GBASE-PQG-D3	1 = PMA/PMD is able to perform 50/25GBASE-PQG-D3 0 = PMA/PMD is not able to perform 50/25GBASE-PQG-D3	RO
1.1001.8	50/25GBASE-PQG-D2	1 = PMA/PMD is able to perform 50/25GBASE-PQG-D2 0 = PMA/PMD is not able to perform 50/25GBASE-PQG-D2	RO
1.1001.7	50/10GBASE-PQX-U3	1 = PMA/PMD is able to perform 50/10GBASE-PQX-U3 0 = PMA/PMD is not able to perform 50/10GBASE-PQX-U3	RO

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Table 45–128—Nx25G-EPON PMA/PMD extended ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.1001.6	50/10GBASE-PQX-U2	1 = PMA/PMD is able to perform 50/10GBASE-PQX-U2 0 = PMA/PMD is not able to perform 50/10GBASE-PQX-U2	RO
1.1001.5	50/10GBASE-PQX-D3	1 = PMA/PMD is able to perform 50/10GBASE-PQX-D3 0 = PMA/PMD is not able to perform 50/10GBASE-PQX-D3	RO
1.1001.4	50/10GBASE-PQX-D2	1 = PMA/PMD is able to perform 50/10GBASE-PQX-D2 0 = PMA/PMD is not able to perform 50/10GBASE-PQX-D2	RO
1.1001.3	50/10GBASE-PQG-U3	1 = PMA/PMD is able to perform 50/10GBASE-PQG-U3 0 = PMA/PMD is not able to perform 50/10GBASE-PQG-U3	RO
1.1001.2	50/10GBASE-PQG-U2	1 = PMA/PMD is able to perform 50/10GBASE-PQG-U2 0 = PMA/PMD is not able to perform 50/10GBASE-PQG-U2	RO
1.1001.1	50/10GBASE-PQG-D3	1 = PMA/PMD is able to perform 50/10GBASE-PQG-D3 0 = PMA/PMD is not able to perform 50/10GBASE-PQG-D3	RO
1.1001.0	50/10GBASE-PQG-D2	1 = PMA/PMD is able to perform 50/10GBASE-PQG-D2 0 = PMA/PMD is not able to perform 50/10GBASE-PQG-D2	RO
1.1002.15:8	Reserved	Value always 0	RO
1.1002.7	50GBASE-PQX-U3	1 = PMA/PMD is able to perform 50GBASE-PQX-U3 0 = PMA/PMD is not able to perform 50GBASE-PQX-U3	RO
1.1002.6	50GBASE-PQX-U2	1 = PMA/PMD is able to perform 50GBASE-PQX-U2 0 = PMA/PMD is not able to perform 50GBASE-PQX-U2	RO
1.1002.5	50GBASE-PQX-D3	1 = PMA/PMD is able to perform 50GBASE-PQX-D3 0 = PMA/PMD is not able to perform 50GBASE-PQX-D3	RO
1.1002.4	50GBASE-PQX-D2	1 = PMA/PMD is able to perform 50GBASE-PQX-D2 0 = PMA/PMD is not able to perform 50GBASE-PQX-D2	RO
1.1002.3	50GBASE-PQG-U3	1 = PMA/PMD is able to perform 50GBASE-PQG-U3 0 = PMA/PMD is not able to perform 50GBASE-PQG-U3	RO
1.1002.2	50GBASE-PQG-U2	1 = PMA/PMD is able to perform 50GBASE-PQG-U2 0 = PMA/PMD is not able to perform 50GBASE-PQG-U2	RO
1.1002.1	50GBASE-PQG-D3	1 = PMA/PMD is able to perform 50GBASE-PQG-D3 0 = PMA/PMD is not able to perform 50GBASE-PQG-D3	RO
1.1002.0	50GBASE-PQG-D2	1 = PMA/PMD is able to perform 50GBASE-PQG-D2 0 = PMA/PMD is not able to perform 50GBASE-PQG-D2	RO

[a]RO = Read only

45.2.1.159.1 25GBASE-PQX-U3 (1.1000.15)

When read as a one, bit 1.1000.15 indicates that the PMA/PMD is able to support a 25GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1000.15 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-U3 PMA/PMD type.

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45.2.1.159.2 25GBASE-PQX-U2 (1.1000.14)

When read as a one, bit 1.1000.14 indicates that the PMA/PMD is able to support a 25GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1000.14 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-U2 PMA/PMD type.

45.2.1.159.3 25GBASE-PQX-D3 (1.1000.13)

When read as a one, bit 1.1000.13 indicates that the PMA/PMD is able to support a 25GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1000.13 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-D3 PMA/PMD type.

45.2.1.159.4 25GBASE-PQX-D2 (1.1000.12)

When read as a one, bit 1.1000.12 indicates that the PMA/PMD is able to support a 25GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1000.12 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-D2 PMA/PMD type.

45.2.1.159.5 25GBASE-PQG-U3 (1.1000.11)

When read as a one, bit 1.1000.11 indicates that the PMA/PMD is able to support a 25GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1000.11 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-U3 PMA/PMD type.

45.2.1.159.6 25GBASE-PQG-U2 (1.1000.10)

When read as a one, bit 1.1000.10 indicates that the PMA/PMD is able to support a 25GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1000.10 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-U2 PMA/PMD type.

45.2.1.159.7 25GBASE-PQG-D3 (1.1000.9)

When read as a one, bit 1.1000.9 indicates that the PMA/PMD is able to support a 25GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1000.9 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-D3 PMA/PMD type.

45.2.1.159.8 25GBASE-PQG-D2 (1.1000.8)

When read as a one, bit 1.1000.8 indicates that the PMA/PMD is able to support a 25GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1000.8 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-D2 PMA/PMD type.

45.2.1.159.9 25/10GBASE-PQX-U3 (1.1000.7)

When read as a one, bit 1.1000.7 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1000.7 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-U3 PMA/PMD type.

45.2.1.159.10 25/10GBASE-PQX-U2 (1.1000.6)

When read as a one, bit 1.1000.6 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1000.6 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-U2 PMA/PMD type.

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45.2.1.159.11 25/10GBASE-PQX-D3 (1.1000.5)

When read as a one, bit 1.1000.5 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1000.5 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-D3 PMA/PMD type.

45.2.1.159.12 25/10GBASE-PQX-D2 (1.1000.4)

When read as a one, bit 1.1000.4 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1000.4 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-D2 PMA/PMD type.

45.2.1.159.13 25/10GBASE-PQG-U3 (1.1000.3)

When read as a one, bit 1.1000.3 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1000.3 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-U3 PMA/PMD type.

45.2.1.159.14 25/10GBASE-PQG-U2 (1.1000.2)

When read as a one, bit 1.1000.2 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1000.2 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-U2 PMA/PMD type.

45.2.1.159.15 25/10GBASE-PQG-D3 (1.1000.1)

When read as a one, bit 1.1000.1 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1000.1 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-D3 PMA/PMD type.

45.2.1.159.16 25/10GBASE-PQG-D2 (1.1000.0)

When read as a one, bit 1.1000.0 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1000.0 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-D2 PMA/PMD type.

45.2.1.159.17 50/25GBASE-PQX-U3 (1.1001.15)

When read as a one, bit 1.1001.15 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1001.15 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-U3 PMA/PMD type.

45.2.1.159.18 50/25GBASE-PQX-U2 (1.1001.14)

When read as a one, bit 1.1001.14 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1001.14 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-U2 PMA/PMD type.

45.2.1.159.19 50/25GBASE-PQX-D3 (1.1001.13)

When read as a one, bit 1.1001.13 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1001.13 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-D3 PMA/PMD type.

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45.2.1.159.20 50/25GBASE-PQX-D2 (1.1001.12)

When read as a one, bit 1.1001.12 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1001.12 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-D2 PMA/PMD type.

45.2.1.159.21 50/25GBASE-PQG-U3 (1.1001.11)

When read as a one, bit 1.1001.11 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1001.11 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-U3 PMA/PMD type.

45.2.1.159.22 50/25GBASE-PQG-U2 (1.1001.10)

When read as a one, bit 1.1001.10 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1001.10 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-U2 PMA/PMD type.

45.2.1.159.23 50/25GBASE-PQG-D3 (1.1001.9)

When read as a one, bit 1.1001.9 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1001.9 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-D3 PMA/PMD type.

45.2.1.159.24 50/25GBASE-PQG-D2 (1.1001.8)

When read as a one, bit 1.1001.8 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1001.8 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-D2 PMA/PMD type.

45.2.1.159.25 50/10GBASE-PQX-U3 (1.1001.7)

When read as a one, bit 1.1001.7 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1001.7 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-U3 PMA/PMD type.

45.2.1.159.26 50/10GBASE-PQX-U2 (1.1001.6)

When read as a one, bit 1.1001.6 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1001.6 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-U2 PMA/PMD type.

45.2.1.159.27 50/10GBASE-PQX-D3 (1.1001.5)

When read as a one, bit 1.1001.5 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1001.5 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-D3 PMA/PMD type.

45.2.1.159.28 50/10GBASE-PQX-D2 (1.1001.4)

When read as a one, bit 1.1001.4 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1001.4 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-D2 PMA/PMD type.

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45.2.1.159.29 50/10GBASE-PQG-U3 (1.1001.3)

When read as a one, bit 1.1001.3 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1001.3 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-U3 PMA/PMD type.

45.2.1.159.30 50/10GBASE-PQG-U2 (1.1001.2)

When read as a one, bit 1.1001.2 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1001.2 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-U2 PMA/PMD type.

45.2.1.159.31 50/10GBASE-PQG-D3 (1.1001.1)

When read as a one, bit 1.1001.1 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1001.1 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-D3 PMA/PMD type.

45.2.1.159.32 50/10GBASE-PQG-D2 (1.1001.0)

When read as a one, bit 1.1001.0 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1001.0 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-D2 PMA/PMD type.

45.2.1.159.33 50GBASE-PQX-U3 (1.1002.7)

When read as a one, bit 1.1002.7 indicates that the PMA/PMD is able to support a 50GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1002.7 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-U3 PMA/PMD type.

45.2.1.159.34 50GBASE-PQX-U2 (1.1002.6)

When read as a one, bit 1.1002.6 indicates that the PMA/PMD is able to support a 50GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1002.6 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-U2 PMA/PMD type.

45.2.1.159.35 50GBASE-PQX-D3 (1.1002.5)

When read as a one, bit 1.1002.5 indicates that the PMA/PMD is able to support a 50GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1002.5 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-D3 PMA/PMD type.

45.2.1.159.36 50GBASE-PQX-D2 (1.1002.4)

When read as a one, bit 1.1002.4 indicates that the PMA/PMD is able to support a 50GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1002.4 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-D2 PMA/PMD type.

45.2.1.159.37 50GBASE-PQG-U3 (1.1002.3)

When read as a one, bit 1.1002.3 indicates that the PMA/PMD is able to support a 50GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1002.3 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-U3 PMA/PMD type.

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45.2.1.159.38 50GBASE-PQG-U2 (1.1002.2)

When read as a one, bit 1.1002.2 indicates that the PMA/PMD is able to support a 50GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1002.2 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-U2 PMA/PMD type.

45.2.1.159.39 50GBASE-PQG-D3 (1.1002.1)

When read as a one, bit 1.1002.1 indicates that the PMA/PMD is able to support a 50GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1002.1 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-D3 PMA/PMD type.

45.2.1.159.40 50GBASE-PQG-D2 (1.1002.0)

When read as a one, bit 1.1002.0 indicates that the PMA/PMD is able to support a 50GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1002.0 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-D2 PMA/PMD type.

45.2.1.160 BASE-R LP coefficient update register, lanes 1 through 9 (Register 1.1101, 1.1102, 1.1103, 1.1104, 1.1105, 1.1106, 1.1107, 1.1108, 1.1109)

For multi-PCS lane BASE-R PHYs, these registers are defined similarly to register 1.152 (which is used for lane 0, see 45.2.1.97) but for lanes 1 through 9 respectively of multi-PCS lane PHYs.

Registers corresponding to lanes that are not used for the selected PHY shall return all zeros.

45.2.1.161 BASE-R PAM4 PMD training LP control, lane 0 through lane 3 registers (Register 1.1120 through 1.1123)

The BASE-R PAM4 PMD training LP control, lane 0 through lane 3 registers reflect the contents of the first 16-bit word of the training frame most recently received for each lane. Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, and lane 3 maps to register 1.1123.

The assignment of bits in the BASE-R PAM4 PMD training LP control, lane 0 register is shown in Table 45–129. The assignment of bits in the registers for lane 1 through lane 3 is equivalent to the assignment for lane 0. When training is not disabled, the bits in registers 1.1120 through 1.1123 are read only; however, when training is disabled the R/W bits become writeable.

Table 45–129—BASE-R PAM4 PMD training LP control, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1120.15:14	Reserved	Value always 0	RO
1.1120.13:12	Initial condition request	13 12 1 1 = Preset 3 1 0 = Preset 2 0 1 = Preset 1 0 0 = Individual coefficient control	R/W
1.1120.11:10	Reserved	Value always 0	RO

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Table 45–129—BASE-R PAM4 PMD training LP control, lane 0 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.1120.9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	R/W
1.1120.7:5	Reserved	Value always 0	RO
1.1120.4:2	Coefficient select	4 3 2 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	R/W
1.1120.1:0	Coefficient request	1 0 1 1 = No equalization 1 0 = Decrement 0 1 = Increment 0 0 = Hold	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.162 BASE-R LP status report register, lanes 1 through 9 (Register 1.1201, 1.1202, 1.1203, 1.1204, 1.1205, 1.1206, 1.1207, 1.1208, 1.1209)

For multi-PCS lane BASE-R PHYs, these registers are defined similarly to register 1.153 (which is used for lane 0, see 45.2.1.98) but for lanes 1 through 9 respectively of multi-PCS lane PHYs.

Registers corresponding to lanes that are not used for the selected PHY shall return all zeros.

45.2.1.163 BASE-R PAM4 PMD training LP status, lane 0 through lane 3 registers (Register 1.1220 through 1.1223)

The BASE-R PAM4 PMD training LP status, lane 0 through lane 3 registers reflect the contents of the second 16-bit word of the training frame most recently received for each lane. Lane 0 maps to register 1.1220, lane 1 maps to register 1.1221, lane 2 maps to register 1.1222, and lane 3 maps to register 1.1223.

The assignment of bits in the BASE-R PAM4 PMD training LP status, lane 0 register is shown in Table 45–130. The assignment of bits in the registers for lane 1 through lane 3 is equivalent to the assignment for lane 0.

45.2.1.164 BASE-R LD coefficient update register, lanes 1 through 9 (Register 1.1301, 1.1302, 1.1303, 1.1304, 1.1305, 1.1306, 1.1307, 1.1308, 1.1309)

For multi-PCS lane BASE-R PHYs, these registers are defined similarly to register 1.154 (which is used for lane 0, see 45.2.1.99) but for lanes 1 through 9 respectively of multi-PCS lane PHYs.

Registers corresponding to lanes that are not used for the selected PHY shall return all zeros.

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Table 45–130—BASE-R PAM4 PMD training LP status, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1220.15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue	RO
1.1220.14:12	Reserved	Value always 0	RO
1.1220.11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RO
1.1220.9	Receiver frame lock	1 = Frame boundaries identified 0 = Frame boundaries not identified	RO
1.1220.8	Initial condition status	1 = Updated 0 = Not updated	RO
1.1220.7	Parity	Even parity bit	RO
1.1220.6	Reserved	Value always 0	RO
1.1220.5:3	Coefficient select echo	5 4 3 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	RO
1.1220.2:0	Coefficient status	2 1 0 1 1 1 = Reserved 1 1 0 = Coefficient at limit and equalization limit 1 0 1 = Reserved 1 0 0 = Equalization limit 0 1 1 = Coefficient not supported 0 1 0 = Coefficient at limit 0 0 1 = Updated 0 0 0 = Not updated	RO

[a]RO = Read only

45.2.1.165 BASE-R PAM4 PMD training LD control, lane 0 through lane 3 registers (Register 1.1320 through 1.1323)

The BASE-R PAM4 PMD training LD control, lane 0 through lane 3 registers reflect the contents of the control field of the outgoing training frame for each lane. Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, and lane 3 maps to register 1.1323.

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The assignment of bits in the BASE-R PAM4 PMD training LP control, lane 0 register is shown in Table 45–131. The assignment of bits in the registers for lane 1 through lane 3 is equivalent to the assignment for lane 0.

Table 45–131—BASE-R PAM4 PMD training LD control, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1320.15:14	Reserved	Value always 0	RO
1.1320.13:12	Initial condition request	13 12 1 1 = Preset 3 1 0 = Preset 2 0 1 = Preset 1 0 0 = Individual coefficient control	R/W
1.1320.11:10	Reserved	Value always 0	RO
1.1320.9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	R/W
1.1320.7:5	Reserved	Value always 0	RO
1.1320.4:2	Coefficient select	4 3 2 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	R/W
1.1320.1:0	Coefficient request	1 0 1 1 = No equalization 1 0 = Decrement 0 1 = Increment 0 0 = Hold	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.166 BASE-R LD status report register, lanes 1 through 9 (Register 1.1401, 1.1402, 1.1403, 1.1404, 1.1405, 1.1406, 1.1407, 1.1408, 1.1409)

For multi-PCS lane BASE-R PHYs, these registers are defined similarly to register 1.155 (which is used for lane 0, see 45.2.1.100) but for lanes 1 through 9 respectively of multi-PCS lane PHYs.

Registers corresponding to lanes that are not used for the selected PHY shall return all zeros.

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45.2.1.167 BASE-R PAM4 PMD training LD status, lane 0 through lane 3 registers (Register 1.1420 through 1.1423)

The BASE-R PAM4 PMD training LD status, lane 0 through lane 3 registers reflect the contents of the status field of the outgoing training frame for each lane. Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to register 1.1422, and lane 3 maps to register 1.1423.

The assignment of bits in the BASE-R PAM4 PMD training LD status, lane 0 register is shown in Table 45–132. The assignment of bits in the registers for lane 1 through lane 3 is equivalent to the assignment for lane 0.

Table 45–132—BASE-R PAM4 PMD training LD status, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1420.15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue	RO
1.1420.14:12	Reserved	Value always 0	RO
1.1420.11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RO
1.1420.9	Receiver frame lock	1 = Frame boundaries identified 0 = Frame boundaries not identified	RO
1.1420.8	Initial condition status	1 = Updated 0 = Not updated	RO
1.1420.7	Parity	Even parity bit	RO
1.1420.6	Reserved	Value always 0	RO
1.1420.5:3	Coefficient select echo	5 4 3 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$	RO
1.1420.2:0	Coefficient status	2 1 0 1 1 1 = Reserved 1 1 0 = Coefficient at limit and equalization limit 1 0 1 = Reserved 1 0 0 = Equalization limit 0 1 1 = Coefficient not supported 0 1 0 = Coefficient at limit 0 0 1 = Updated 0 0 0 = Not updated	RO

[a]RO = Read only

45.2.1.168 PMD training pattern lanes 0 through 3 (Register 1.1450 through 1.1453)

The assignment of bits in the PMD training pattern lane 0 register is shown in Table 45–133. The assignment of bits in the PMD training pattern lanes 1 through 3 registers are defined similarly to lane 0. Register 1.1450

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controls the PMD training pattern for PMD lane 0; register 1.1451 controls the PMD training pattern for PMD lane 1; etc.

Table 45–133—PMD training pattern lane 0 bit definitions

Bit(s)	Name	Description	R/W[a]
1.1450.15:14	Seed	Two most significant bits of PRBS13 seed	R/W
1.1450.13	Reserved	Value always 0	RO
1.1450.12:11	Polynomial identifier	Identifier (0, 1, 2, or 3) selecting polynomial for PRBS	R/W
1.1450.10:0	Seed	11 bit, binary seed for sequence	R/W

[a]R/W = Read/Write, RO = Read only

Register bits 12:11 contain a 2-bit identifier that selects the polynomial used for training in the particular PMD lane according to the definition in 92.7.12. The polynomial identifier for each lane should be unique; two lanes having the same identifier could impair operation of the PMD control function. The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11.

For PHYs that use a PRBS11 training pattern, register bits 10:0 contain the 11-bit seed for the sequence, where register bit 0 gives seed bit S0; register bit 1 gives seed bit S1; etc., through register bit 10 gives seed bit S10. The default seeds are (binary, S0 is left-most bit): for lane 0, 10101111110; for lane 1, 11001000101; for lane 2, 11100101101; for lane 3, 11110110110. This produces the following initial output (hexadecimal representation where the hex symbols are transmitted from left to right and the most significant bit of each hex symbol is transmitted first): for lane 0, 0xFBF1CB3E; for lane 1, 0xFBB1E665; for lane 2, 0xF3FDAE46; for lane 3, 0xF2FFA46B.

For PHYs that use a PRBS13 training pattern, the 13-bit seed value is composed from register bits 15:14 and register bits 10:0, where register bit 0 gives seed bit S0; register bit 1 gives seed bit S1; etc., through register bit 10 gives seed bit S10, register bit 14 gives seed bit S11 and register bit 15 gives seed bit S12. The default PRBS13 seed values are given in Table 136–8.

45.2.1.169 Test-pattern ability (Register 1.1500)

The test-pattern ability register is used for PHY types that implement SSPRQ, square wave, and PRBS testing in the PMA. These functions are described in 127.3.4.1, 83.5.10, and 120.5.11. The assignment of bits in the test-pattern ability register is shown in Table 45–134.

Table 45–134—Test-pattern ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1500.15:14	Reserved	Value always 0	RO
1.1500.13	SSPRQ Tx generator ability	1 = SSPRQ transmit direction pattern generator supported 0 = SSPRQ transmit direction pattern generator not supported	RO
1.1500.12	Square wave test ability	1 = Square wave testing supported 0 = Square wave testing not supported	RO

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Table 45–134—Test-pattern ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.1500.11	PRBS13Q Tx generator ability	1 = PRBS13Q transmit direction pattern generator supported 0 = PRBS13Q transmit direction pattern generator not supported	RO
1.1500.10	PRBS13Q Rx generator ability	1 = PRBS13Q receive direction pattern generator supported 0 = PRBS13Q receive direction pattern generator not supported	RO
1.1500.9	PRBS31Q Tx generator ability	1 = PRBS31Q transmit direction pattern generator supported 0 = PRBS31Q transmit direction pattern generator not supported	RO
1.1500.8	PRBS31Q Tx checker ability	1 = PRBS31Q transmit direction pattern checker supported 0 = PRBS31Q transmit direction pattern checker not supported	RO
1.1500.7	PRBS31Q Rx generator ability	1 = PRBS31Q receive direction pattern generator supported 0 = PRBS31Q receive direction pattern generator not supported	RO
1.1500.6	PRBS31Q Rx checker ability	1 = PRBS31Q receive direction pattern checker supported 0 = PRBS31Q receive direction pattern checker not supported	RO
1.1500.5	PRBS9 Tx generator ability	1 = PRBS9 transmit direction pattern generator supported 0 = PRBS9 transmit direction pattern generator not supported	RO
1.1500.4	PRBS9 Rx generator ability	1 = PRBS9 receive direction pattern generator supported 0 = PRBS9 receive direction pattern generator not supported	RO
1.1500.3	PRBS31 Tx generator ability	1 = PRBS31 transmit direction pattern generator supported 0 = PRBS31 transmit direction pattern generator not supported	RO
1.1500.2	PRBS31 Tx checker ability	1 = PRBS31 transmit direction pattern checker supported 0 = PRBS31 transmit direction pattern checker not supported	RO
1.1500.1	PRBS31 Rx generator ability	1 = PRBS31 receive direction pattern generator supported 0 = PRBS31 receive direction pattern generator not supported	RO
1.1500.0	PRBS31 Rx checker ability	1 = PRBS31 receive direction pattern checker supported 0 = PRBS31 receive direction pattern checker not supported	RO

[a]RO = Read only

If SSPRQ pattern testing is supported and register 1.1500 is implemented then bit 1.1500.13 shall indicate the generation ability in the transmit direction. The SSPRQ pattern test is controlled by register 1.1501 (see 45.2.1.170).

If square wave testing is supported and register 1.1500 is implemented then bit 1.1500.12 shall be set to one. The square wave test is controlled by register 1.1510 (see 45.2.1.171).

If PRBS13Q pattern testing is supported and register 1.1500 is implemented then bit 1.1500.11 shall indicate the generation ability in the transmit direction and bit 1.1500.10 shall indicate the generation ability in the receive direction. The PRBS13Q pattern test is controlled by register 1.1512 (see 45.2.1.172).

If PRBS31Q pattern testing is supported and register 1.1500 is implemented then bit 1.1500.9 shall indicate the generation ability in the transmit direction and bit 1.1500.7 shall indicate the generation ability in the receive direction. Bit 1.1500.8 shall indicate the checker ability in the transmit direction and bit 1.1500.6

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shall indicate the checker ability in the receive direction. The PRBS31Q pattern test is controlled by register 1.1501 (see 45.2.1.170).

If PRBS9 pattern testing is supported and register 1.1500 is implemented then bit 1.1500.5 shall indicate the generation ability in the transmit direction and bit 1.1500.4 shall indicate the generation ability in the receive direction. The PRBS pattern test is controlled by register 1.1501 (see 45.2.1.170).

If PRBS31 pattern testing is supported and register 1.1500 is implemented then bit 1.1500.3 shall indicate the generation ability in the transmit direction and bit 1.1500.1 shall indicate the generation ability in the receive direction. Bit 1.1500.2 shall indicate the checker ability in the transmit direction and bit 1.1500.0 shall indicate the checker ability in the receive direction. The PRBS pattern test is controlled by register 1.1501 (see 45.2.1.170).

45.2.1.170 PRBS pattern testing control (Register 1.1501)

The PRBS pattern testing control register is used for PHY types that implement PRBS pattern testing in the PMA. This function is described in 83.5.10 and 120.5.11. The assignment of bits in the PRBS pattern testing control register is shown in Table 45–135.

Table 45–135—PRBS pattern testing control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1501.15	Reserved	Value always 0	RO
1.1501.14	SSPRQ pattern enable	1 = Enable SSPRQ test-pattern 0 = Disable SSPRQ test-pattern	R/W
1.1501.13	PRBS31Q pattern enable	1 = Enable PRBS31Q test-pattern 0 = Disable PRBS31Q test-pattern	R/W
1.1501.12	Reserved	Value always 0	RO
1.1501.11	Transmitter linearity test pattern enable	1 = Enable transmitter linearity test-pattern 0 = Disable transmitter linearity test-pattern	R/W
1.1501.10	QPRBS13 pattern enable	1 = Enable QPRBS13 test-pattern 0 = Disable QPRBS13 test-pattern	R/W
1.1501.9	JP03B pattern enable	1 = Enable JP03B test-pattern 0 = Disable JP03B test-pattern	R/W
1.1501.8	JP03A pattern enable	1 = Enable JP03A test-pattern 0 = Disable JP03A test-pattern	R/W
1.1501.7	PRBS31 pattern enable	1 = Enable PRBS31 test-pattern 0 = Disable PRBS31 test-pattern	R/W
1.1501.6	PRBS9 pattern enable	1 = Enable PRBS9 test-pattern 0 = Disable PRBS9 test-pattern	R/W
1.1501.5:4	Reserved	Value always 0	RO
1.1501.3	Tx generator enable	1 = Enable transmit direction test-pattern generator 0 = Disable transmit direction test-pattern generator	R/W

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Table 45–135—PRBS pattern testing control register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.1501.2	Tx checker enable	1 = Enable transmit direction test-pattern checker 0 = Disable transmit direction test-pattern checker	R/W
1.1501.1	Rx generator enable	1 = Enable receive direction test-pattern generator 0 = Disable receive direction test-pattern generator	R/W
1.1501.0	Rx checker enable	1 = Enable receive direction test-pattern checker 0 = Disable receive direction test-pattern checker	R/W

[a]R/W = Read/Write, RO = Read only

Register 1.1501, bit 7 enables testing with the PRBS31 pattern defined in 83.5.10. Register 1.1501, bit 6 enables testing with the PRBS9 pattern defined in 83.5.10. The assertion of register 1.1501 bits 7 and 6 is mutually exclusive. If both bits are asserted the behavior is undefined. The assertion of register 1.1501, bits 7 and 6 works in conjunction with register 1.1501, bits 3:0. If none of the bits 3:0 are asserted then bits 7 and 6 have no effect.

Register 1.1501, bit 3 enables pattern generation in the transmit direction. Register 1.1501, bit 2 enables pattern checking in the transmit direction. Register 1.1501, bit 1 enables pattern generation in the receive direction. Register 1.1501, bit 0 enables pattern checking in the receive direction. If none of the bits 3:0 are asserted then bits 7 and 6 have no effect.

Register 1.1501 bit 8 enables testing with the JP03A pattern defined in 94.2.9.1 for 100GBASE-KP4 PMA/PMD. Register 1.1501 bit 9 enables testing with the JP03B pattern defined in 94.2.9.2 for 100GBASE-KP4 PMA/PMD. Register 1.1501 bit 10 enables testing with the QPRBS13 pattern defined in 94.2.9.3 for 100GBASE-KP4 PMA/PMD. Register 1.1501 bit 11 enables the transmitter linearity test pattern defined in 94.2.9.4 for 100GBASE-KP4 PMA/PMD. Register 1.1501 bit 13 enables the PRBS31Q test pattern defined in 120.5.11.2.2. Register 1.1501 bit 14 enables the SSPRQ test pattern defined in 120.5.11.2.3. The assertion of bits 1.1501.8, 1.1501.9, 1.1501.10, 1.1501.11, 1.1501.13, and 1.1501.14 are mutually exclusive. If more than one bit is asserted, the behavior is undefined. The assertion of 1.1501.8, 1.1501.9, 1.501.10, and 1.1501.11 operates in conjunction with register 1.1501 bit 3 for 100GBASE-KP4 PMA/PMD. For other PMA/PMD types or if bit 1.1501.3 is not asserted, then 1.1501.8, 1.1501.9, 1.501.10, and 1.1501.11 have no effect. For the 50GBASE-R, 100GBASE-R PAM4, 200GBASE-R, and 400GBASE-R PMAs, the assertion of register 1.1501 bit 13 operates in conjunction with register 1.1501 bits 3 and 1. If neither bit is asserted, then register 1.1501 bit 13 has no effect. Also for the 50GBASE-R, 100GBASE-R PAM4, 200GBASE-R, and 400GBASE-R PMAs, the assertion of register 1.1501 bit 14 operates in conjunction with register 1.1501 bit 3. If bit 1.1501.3 is not asserted, then register 1.1501 bit 14 has no effect. For other PMA/PMD types register 1.1501 bits 13 and 14 have no effect.

45.2.1.171 Square wave testing control (Register 1.1510)

The square wave testing control register is used for PHY types that implement transmit square wave testing in the PMA. This function is described in 83.5.10 and 120.5.11. The assignment of bits in the square wave testing control register is shown in Table 45–136.

Register 1.1510, bits 0 through 15 enable square wave output on PMA lanes 0 through 15 respectively. Lanes for which a square wave pattern is not enabled act as determined by other registers.

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Table 45–136—Square wave testing control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1510.15	Lane 15 SW enable	1 = Enable square wave on lane 15 0 = Disable square wave on lane 15	R/W
1.1510.14	Lane 14 SW enable	1 = Enable square wave on lane 14 0 = Disable square wave on lane 14	R/W
1.1510.13	Lane 13 SW enable	1 = Enable square wave on lane 13 0 = Disable square wave on lane 13	R/W
1.1510.12	Lane 12 SW enable	1 = Enable square wave on lane 12 0 = Disable square wave on lane 12	R/W
1.1510.11	Lane 11 SW enable	1 = Enable square wave on lane 11 0 = Disable square wave on lane 11	R/W
1.1510.10	Lane 10 SW enable	1 = Enable square wave on lane 10 0 = Disable square wave on lane 10	R/W
1.1510.9	Lane 9 SW enable	1 = Enable square wave on lane 9 0 = Disable square wave on lane 9	R/W
1.1510.8	Lane 8 SW enable	1 = Enable square wave on lane 8 0 = Disable square wave on lane 8	R/W
1.1510.7	Lane 7 SW enable	1 = Enable square wave on lane 7 0 = Disable square wave on lane 7	R/W
1.1510.6	Lane 6 SW enable	1 = Enable square wave on lane 6 0 = Disable square wave on lane 6	R/W
1.1510.5	Lane 5 SW enable	1 = Enable square wave on lane 5 0 = Disable square wave on lane 5	R/W
1.1510.4	Lane 4 SW enable	1 = Enable square wave on lane 4 0 = Disable square wave on lane 4	R/W
1.1510.3	Lane 3 SW enable	1 = Enable square wave on lane 3 0 = Disable square wave on lane 3	R/W
1.1510.2	Lane 2 SW enable	1 = Enable square wave on lane 2 0 = Disable square wave on lane 2	R/W
1.1510.1	Lane 1 SW enable	1 = Enable square wave on lane 1 0 = Disable square wave on lane 1	R/W
1.1510.0	Lane 0 SW enable	1 = Enable square wave on lane 0 0 = Disable square wave on lane 0	R/W

[a]R/W = Read/Write

45.2.1.172 PRBS13Q testing control (Register 1.1512)

The PRBS13Q testing control register is used for PHY types that implement PRBS13Q testing in the PMA. This function is described in 120.5.11.2.1. The assignment of bits in the PRBS13Q testing control register is shown in Table 45–137.

Register 1.1512, bits 0 through 7 enable PRBS13Q output on PMA lanes 0 through 7 respectively. The assertion of register 1.1512 bits 0 through 7 operates in conjunction with register 1.1501 bits 3 and 1. If

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Table 45–137—PRBS13Q testing control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1512.15:8	Reserved	Value always 0	RO
1.1512.7	Lane 7 PRBS13Q enable	1 = Enable PRBS13Q on lane 7 0 = Disable PRBS13Q on lane 7	R/W
1.1512.6	Lane 6 PRBS13Q enable	1 = Enable PRBS13Q on lane 6 0 = Disable PRBS13Q on lane 6	R/W
1.1512.5	Lane 5 PRBS13Q enable	1 = Enable PRBS13Q on lane 5 0 = Disable PRBS13Q on lane 5	R/W
1.1512.4	Lane 4 PRBS13Q enable	1 = Enable PRBS13Q on lane 4 0 = Disable PRBS13Q on lane 4	R/W
1.1512.3	Lane 3 PRBS13Q enable	1 = Enable PRBS13Q on lane 3 0 = Disable PRBS13Q on lane 3	R/W
1.1512.2	Lane 2 PRBS13Q enable	1 = Enable PRBS13Q on lane 2 0 = Disable PRBS13Q on lane 2	R/W
1.1512.1	Lane 1 PRBS13Q enable	1 = Enable PRBS13Q on lane 1 0 = Disable PRBS13Q on lane 1	R/W
1.1512.0	Lane 0 PRBS13Q enable	1 = Enable PRBS13Q on lane 0 0 = Disable PRBS13Q on lane 0	R/W

[a]R/W = Read/Write, RO = Read only

neither bit is asserted, then register 1.1512 bits 0 through 7 have no effect. Lanes for which a PRBS13Q pattern is not enabled act as determined by other registers.

45.2.1.173 PRBS Tx pattern testing error counter (Register 1.1600 through 1.1615)

The PRBS Tx pattern testing error counter registers are used for PHY types that implement PRBS Tx pattern testing in the PMA. This function is described in 83.5.10 and 120.5.11. The assignment of bits in the PRBS Tx pattern testing error counter registers are shown in Table 45–138. Register 1.1600 contains the PRBS Tx pattern testing error counter for lane 0, register 1.1601 contains the PRBS Tx pattern testing error counter for lane 1, and registers 1.1602 through 1.1609 contain the PRBS Tx pattern testing error counters for lanes 2 through 15 respectively. Counters corresponding to lanes that are not implemented in a PMA shall read all zeros.

Table 45–138—PRBS Tx pattern testing error counter

Bit(s)	Name	Description	R/W[a]
1.1600[b].15:0	Error counter		RO, NR

[a]RO = Read only, NR = Non Roll-over.
[b]All instances of address 1.1600 also apply to addresses 1.1601 through 1.1615.

The PRBS Tx pattern testing error counter is a 16-bit counter as defined in 83.5.10 and 120.5.11. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the PMA reset. These bits shall be held at all ones in the case of overflow.

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45.2.1.174 PRBS Rx pattern testing error counter (Register 1.1700 through 1.1715)

The PRBS Rx pattern testing error counter registers are used for PHY types that implement PRBS Rx pattern testing in the PMA. This function is described in 83.5.10 and 120.5.11. The assignment of bits in the PRBS Rx pattern testing error counter registers is identical to the PRBS Tx pattern testing error counter as shown in Table 45–138. Register 1.1700 contains the PRBS Rx pattern testing error counter for lane 0, register 1.1701 contains the PRBS Rx pattern testing error counter for lane 1, and registers 1.1702 through 1.1715 contain the PRBS Rx pattern testing error counters for lanes 2 through 15 respectively. Counters corresponding to lanes that are not implemented in a PMA shall read all zeros.

The PRBS Rx pattern testing error counter is a 16-bit counter as defined in 83.5.10 and 120.5.11. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the PMA reset. These bits shall be held at all ones in the case of overflow.

45.2.1.175 TimeSync PMA/PMD capability (Register 1.1800)

The TimeSync PMA/PMD capability register (see Table 45–139) indicates the capability of the PMA/PMD to report the transmit and receive data delay, stored in registers 1.1801 and 1.1805 through 1.1808 respectively.

Table 45–139—TimeSync PMA/PMD capability

Bit(s)	Name	Description	R/W[a]
1.1800.15:2	Reserved	Value always 0	RO
1.1800.1	TimeSync transmit path data delay	1 = PMA/PMD provides information on transmit path data delay in registers 1.1801 through 1.1804 0 = PMA/PMD does not provide information on transmit path data delay	RO
1.1800.0	TimeSync receive path data delay	1 = PMA/PMD provides information on receive path data delay in registers 1.1805 through 1.1808 0 = PMA/PMD does not provide information on receive path data delay	RO

[a]RO = Read only.

45.2.1.176 TimeSync PMA/PMD transmit path data delay (Registers 1.1801, 1.1802, 1.1803, 1.1804)

The TimeSync PMA/PMD transmit path data delay register contains the maximum (registers 1.1801, 1.1802, see Table 45–140) and minimum (registers 1.1803, 1.1804, see Table 45–140) values of the transmit

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path data delay. The transmit path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in register 1.1 (see 45.2.1.2.4).

Table 45–140—TimeSync PMA/PMD transmit path data delay register

Bit(s)	Name	Description	R/W[a]
1.1801.15:0	Maximum PMA/PMD transmit path data delay, lower	PMA/PMD_delay_TX_max [15:0]	RO, MW
1.1802.15:0	Maximum PMA/PMD transmit path data delay, upper	PMA/PMD_delay_TX_max [31:16]	RO, MW
1.1803.15:0	Minimum PMA/PMD transmit path data delay, lower	PMA/PMD_delay_TX_min [15:0]	RO, MW
1.1804.15:0	Minimum PMA/PMD transmit path data delay, upper	PMA/PMD_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word.

45.2.1.177 TimeSync PMA/PMD receive path data delay (Registers 1.1805, 1.1806, 1.1807, 1.1808)

The TimeSync PMA/PMD receive path data delay register contains the maximum (registers 1.1805, 1.1806, see Table 45–141) and minimum (registers 1.1807, 1.1808, see Table 45–141) values of the receive path data delay. The receive path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in register 1.1 (see 45.2.1.2.4).

Table 45–141—TimeSync PMA/PMD receive path data delay register

Bit(s)	Name	Description	R/W[a]
1.1805.15:0	Maximum PMA/PMD receive path data delay, lower	PMA/PMD_delay_RX_max [15:0]	RO, MW
1.1806.15:0	Maximum PMA/PMD receive path data delay, upper	PMA/PMD_delay_RX_max [31:16]	RO, MW
1.1807.15:0	Minimum PMA/PMD receive path data delay, lower	PMA/PMD_delay_RX_min [15:0]	RO, MW
1.1808.15:0	Minimum PMA/PMD receive path data delay, upper	PMA/PMD_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word.

45.2.1.178 10GPASS-XR control and status register (Register 1.1900)

The assignment of bits in the 10GPASS-XR control and status register is shown in Table 45–142.

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Table 45–142—10GPASS-XR control and status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1900.15:14	Reserved	Value always 0	RO
1.1900.13	Time synch capable	1 = The CNU supports time synchronization variables 0 = The CNU does not support time synchronization variables	RO
1.1900.12	US rate mismatch	1 = the upstream rate calculated at the CNU and the CLT matches within 10 b/s 0 = the upstream rate calculated at the CNU and the CLT is mismatched by greater than 10 b/s	RO
1.1900.11	DS rate mismatch	1 = the downstream rate calculated at the CNU and the CLT matches within 10 b/s 0 = the downstream rate calculated at the CNU and the CLT is mismatched by greater than 10 b/s	RO
1.1900.10	Link up ready	1 = the CNU is ready to enter the Link-Up state 0 = the CNU is not ready to enter the Link-Up state	R/W
1.1900.9:3	Continuous pilot scaling factor	Number of continuous pilots in the downstream OFDM channels	R/W
1.1900.2	CRC40 errored blocks	1 = 65-bit blocks with detected CRC40 errors are labeled as errored 0 = 65-bit blocks with detected CRC40 errors are not labeled as errored	R/W
1.1900.1	PHY Discovery complete	1 = The PMA/PMD has completed PHY Discovery on the coaxial cable distribution network 0 = The PMA/PMD has not completed PHY Discovery on the coaxial cable distribution network	R/W
1.1900.0	PHY Discovery enable	1 = PMA/PMD is permitted to transmit on the media 0 = PMA/PMD is not permitted to transmit on the media	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.178.1 Time sync capable (1.1900.13)

When read as one, bit 1.1900.13 indicates that the 10G-PASS-XR PMA/PMD is capable of supporting the time synchronization variables PHY differential delay and PHY differential delay tolerance reflected in registers 1.1949 and 1.1950. This bit is a reflection of the *TimeSyncCapable* variable defined in 101.1.3.

45.2.1.178.2 US rate mismatch (1.1900.12)

When read as one, bit 1.1900.12 indicates that the upstream rate calculated at the CNU and the CLT is mismatched by greater than 10 b/s. This bit is defined in 10GPASS-XR-U PMA/PMD only, in 10GPASS-XR-D always read as zero. This bit is a reflection of the *US_RateMatchFail* variable defined in 100.3.2.3.

45.2.1.178.3 DS rate mismatch (1.1900.11)

When read as one, bit 1.1900.11 indicates that the downstream rate calculated at the CNU and the CLT is mismatched by greater than 10 b/s. This bit is defined in 10GPASS-XR-U PMA/PMD only, in 10GPASS-XR-D always read as zero. This bit is a reflection of the *DS_RateMatchFail* variable defined in 100.3.2.3.

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45.2.1.178.4 Link up ready (1.1900.10)

Bit 1.1900.10 indicates that the CNU is ready for the link-up state. This bit is a reflection of the *LinkUpRdy* variable defined in 102.4.1.8.

45.2.1.178.5 Continuous pilot scaling factor (1.1900.9:3)

Bits 1.1900.9:3 form an unsigned integer that is used to determine the number of continuous pilots in the downstream OFDM channels. These bits are a reflection of the variable *CntPltSF* defined in 101.4.3.6.5.

45.2.1.178.6 CRC40 errored blocks (1.1900.2)

Bit 1.1900.2 is used to control whether 65-bit blocks with detected CRC40 errors are labeled as errored before being passed higher layers as described in 101.3.3.1.4. This bit is a reflection of the variable *CRC40ErrCtrl* defined in 101.3.3.1.6.

45.2.1.178.7 PHY Discovery complete (1.1900.1)

When read as one, bit 1.1900.1 indicates that the 10GPASS-XR PMA/PMD has completed PHY Discovery (see 102.4.1) on the coaxial cable distribution network. When read as zero, bit 1.1900.1 indicates that the PMA/PMD has not completed PHY Discovery on the coaxial cable distribution network. This bit is defined in 10GPASS-XR-U PMA/PMD only, in 10GPASS-XR-D always read as one. This bit is a reflection of the variable *PhyDiscCmplt* defined in 102.4.1.8.

The default value for bit 1.1900.1 is zero.

45.2.1.178.8 PHY Discovery enable (1.1900.0)

When read as one, bit 1.1900.0 indicates that the 10GPASS-XR PMA/PMD is permitted to transmit on the media. When read as zero, bit 1.1900.0 indicates that the PMA/PMD is not permitted to transmit on the media. This bit is a reflection of the variable *PD_Enable* defined in 102.2.7.3.

The default value for bit 1.1900.0 is zero.

45.2.1.179 DS OFDM control register (Register 1.1901)

The assignment of bits in the DS OFDM control register is shown in Table 45–143.

Table 45–143—DS OFDM control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1901.15	CLT tx mute	1 = CLT PHY muted state for test purposes 0 = CLT PHY not muted (normal operation)	R/W
1.1901.14:12	DS OFDM channels	Indicates the number of OFDM channels the PMA/PMD is operating in the downstream direction	R/W
1.1901.11:7	DS time interleaving	Indicates the number of OFDM symbols the PMA/PMD is time interleaving in the downstream direction	R/W

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Table 45–143—DS OFDM control register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.1901.6:4	DS windowing	Indicates the size of the windowing control for the PMA/PMD in the downstream direction	R/W
1.1901.3:0	DS cyclic prefix	Indicates the size of the cyclic prefix for the PMA/PMD in the downstream direction	R/W

[a]R/W = Read/Write

45.2.1.179.1 CLT tx mute (1.1901.15)

When bit 1.1901.15 is set to one, the CLT PMD transmitter enters the test mode and it is muted. When bit 1.1901.15 is set to a zero, the CLT PMD enters the normal operating state. This bit has no effect in the CNU. This bit is a reflection of the variable *CLT_TxMute* defined in 100.4.1.

45.2.1.179.2 DS OFDM channels (1.1901.14:12)

Bits 1.1901.14:12 indicate the integer number of downstream OFDM channels in use. The number is between 1 and 5; where bit 1.1901.12 is the LSB and bit 1.1901.14 is the MSB. These bits are a reflection of the counter *DS_ChCnt* defined in 100.3.2.3.

45.2.1.179.3 DS time interleaving (1.1901.11:7)

Bits 1.1901.11:7 indicate the integer number of time interleaved OFDM symbols in the downstream direction. The number is between 1 and 32; where bit 1.1901.7 is the LSB and bit 1.1901.11 is the MSB. These bits are a reflection of the variable *DS_TmIntrlv* defined in 101.4.3.9.5.

45.2.1.179.4 DS windowing (1.1901.6:4)

Bits 1.1901.6:4 indicate the size, in OFDM Clock periods (1/204.8 MHz), of the windowing control for the 10GPASS-XR PMA/PMD in the downstream direction. These bits are a reflection of the variable *DSNrp* defined in 101.4.3.12.1 with bits 1.1901.6:4 mapping to bits 2:0 of *DSNrp*, respectively.

45.2.1.179.5 DS cyclic prefix (1.1901.3:0)

Bits 1.1901.3:0 indicate the size, in OFDM Clock periods (1/204.8 MHz), of the cyclic prefix control for the 10GPASS-XR PMA/PMD in the downstream direction. These bits are a reflection of the variable *DSNcp* defined in 101.4.3.12.1 with bits 1.1901.3:0 mapping to bits 3:0 of *DSNcp*, respectively.

45.2.1.180 DS OFDM channel frequency control register 1 through 5 (Register 1.1902 through 1.1906)

The assignment of bits in the DS OFDM channel frequency control register 1 through 5 is shown in Table 45–144.

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Table 45–144—DS OFDM channel frequency control register 1 through 5 bit definitions

Bit(s)	Name	Description	R/W[a]
1.1902.15:0	DS OFDM freq ch 1	This register specifies the center frequency of subcarrier 0 of downstream OFDM channel number 1.	R/W
1.1903.15:0	DS OFDM freq ch 2	This register specifies the center frequency of subcarrier 0 of downstream OFDM channel number 2.	R/W
1.1904.15:0	DS OFDM freq ch 3	This register specifies the center frequency of subcarrier 0 of downstream OFDM channel number 3.	R/W
1.1905.15:0	DS OFDM freq ch 4	This register specifies the center frequency of subcarrier 0 of downstream OFDM channel number 4.	R/W
1.1906.15:0	DS OFDM freq ch 5	This register specifies the center frequency of subcarrier 0 of downstream OFDM channel number 5.	R/W

[a]R/W = Read/Write

45.2.1.180.1 DS OFDM freq ch 1 (1.1902.15:0)

Register 1.1902 specifies the center frequency for OFDM channel number 1 in units of 50 kHz. This register is a reflection of the variable *DS_FreqCh(1)* defined in 100.3.2.3.

45.2.1.180.2 DS OFDM freq ch 2 (1.1903.15:0)

Register 1.1903 specifies the center frequency of OFDM channel number 2 in units of 50 kHz. This register is a reflection of the variable *DS_FreqCh(2)* defined in 100.3.2.3.

45.2.1.180.3 DS OFDM freq ch 3 (1.1904.15:0)

Register 1.1904 specifies the center frequency of OFDM channel number 3 in units of 50 kHz. This register is a reflection of the variable *DS_FreqCh(3)* defined in 100.3.2.3.

45.2.1.180.4 DS OFDM freq ch 4 (1.1905.15:0)

Register 1.1905 specifies the center frequency of OFDM channel number 4 in units of 50 kHz. This register is a reflection of the variable *DS_FreqCh(4)* defined in 100.3.2.3.

45.2.1.180.5 DS OFDM freq ch 5 (1.1906.15:0)

Register 1.1906 specifies the center frequency of OFDM channel number 5 in units of 50 kHz. This register is a reflection of the variable *DS_FreqCh(5)* defined in 100.3.2.3.

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45.2.1.181 US OFDM control register (Register 1.1907)

The assignment of bits in the US OFDM control register is shown in Table 45–145.

Table 45–145—US OFDM control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1907.15:8	Random seed	Random back-off seed for PHY Discovery	R/W
1.1907.7	Resource Block size	1 = 16 OFDMA symbols in the upstream OFDMA Resource Block 0 = 8 OFDMA symbols in the upstream OFDMA Resource Block	R/W
1.1907.6:4	US windowing	Indicates the size of the windowing control for the PMA/PMD in the upstream direction	R/W
1.1907.3:0	US cyclic prefix	Indicates the size of the cyclic prefix for the PMA/PMD in the upstream direction	R/W

[a]R/W = Read/Write

45.2.1.181.1 Random seed (1.1907.15:8)

Bits 1.1907.15:8 form an 8-bit integer that is used by the CNU for the seed of the PHY Discovery back-off algorithm. These bits are a reflection of the *Rnd* variable defined in 102.4.1.9.2.

45.2.1.181.2 Resource Block size (1.1907.7)

Bit 1.1907.7 indicates the number of OFDM symbols in a Resource Block in the upstream direction. This bit is a reflection of the variable *RBsize* defined in 101.4.4.3.5.

45.2.1.181.3 US windowing (1.1907.6:4)

Bits 1.1907.6:4 indicate the size, in units of OFDM Clock periods (1/204.8 MHz), of the windowing control for the 10GPASS-XR PMA/PMD in the upstream direction. These bits are a reflection of the variable *USNrp* defined in 101.4.4.10.1 with bits 1.1907.6:4 mapping to bits 2:0 of *USNrp*, respectively.

45.2.1.181.4 US cyclic prefix (1.1907.3:0)

Bits 1.1907.3:0 indicate the size, in units of OFDM Clock periods (1/204.8 MHz), of the cyclic prefix control for the 10GPASS-XR PMA/PMD in the upstream direction. These bits are a reflection of the variable *USNcp* defined in 101.4.4.10.1 with bits 1.1907.3:0 mapping to bits 3:0 of *USNcp*, respectively.

45.2.1.182 US OFDM channel frequency control register (Register 1.1908)

The assignment of bits in the US OFDM channel frequency control register is shown in Table 45–146.

Register 1.1908 indicates the center frequency, in units of 50 kHz, of subcarrier 0 for the upstream OFDM channel. This register is a reflection of the variable *US_FreqCh1* defined in 100.3.2.3.

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Table 45–146—US OFDM channel frequency control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1908.15:0	US OFDM freq	This specifies the center frequency of subcarrier 0 of the upstream OFDM channel.	R/W

[a]R/W = Read/Write

45.2.1.183 US OFDMA pilot pattern register (Register 1.1909)

The assignment of bits in the US OFDMA pilot pattern register is shown in Table 45–147. For additional information on the use of the parameters in this register see 101.4.4.6.

Table 45–147—US OFDMA pilot pattern register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1909.15	Reserved	Value always 0	RO
1.1909.14:12	Type 2 repeat	Indicates the number of subcarriers between Type 2 Pilots	R/W
1.1909.11:8	Type 2 start	Indicates the number of the subcarrier on which the Type 2 Pilot pattern starts	R/W
1.1909.7	Reserved	Value always 0	RO
1.1909.6:4	Type 1 repeat	Indicates the number of subcarriers between Type 1 Pilots	R/W
1.1909.3:0	Type 1 start	Indicates the number of the subcarrier on which the Type 1 Pilot pattern starts	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.183.1 Type 2 repeat (1.1909.14:12)

Bits 1.1909.14:12 indicate the number of subcarriers between repeating Type 2 Pilots. Additional information on pilot patterns and encoding for these bits is located in 101.4.4.6 and Table 101–14. These bits are a reflection of the variable *Type2_Repeat* defined in 101.4.4.6.1.

45.2.1.183.2 Type 2 start (1.1909.11:8)

Bits 1.1909.11:8 indicate the number of the first subcarrier designated as a Type 2 Pilot. These bits are a reflection of the variable *Type2_Start* defined in 101.4.4.6.1.

45.2.1.183.3 Type 1 repeat (1.1909.6:4)

Bits 1.1909.6:4 indicate the number of subcarriers between repeating Type 1 Pilots. Additional information on pilot patterns and encoding for these bits is located in 101.4.4.6 and Table 101–14. These bits are a reflection of the variable *Type1_Repeat* defined in 101.4.4.6.1.

45.2.1.183.4 Type 1 start (1.1909.3:0)

Bits 1.1909.3:0 indicate the number of the first subcarrier designated as a Type 1 Pilot. These bits are a reflection of the variable *Type1_Start* defined in 101.4.4.6.1.

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45.2.1.184 Profile control register (Register 1.1910)

The assignment of bits in the Profile control register is shown in Table 45–148. See 102.4.5 for additional information on the profile copy functionality.

Table 45–148—Profile control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1910.15:12	Reserved	Value always 0	RO
1.1910.11	US copy in process	1 = the active upstream profile is being copied to the off-line profile 0 = the upstream off-line profile is not being modified by a profile copy	RO
1.1910.10	US profile copy	1 = initiates a copy of the active upstream profile to the off-line profile 0 = no copy initiated	R/W, SC
1.1910.9:8	US configuration ID	Controls switching the active upstream profile	RO
1.1910.7	Reserved	Value always 0	RO
1.1910.6:4	DS copy channel ID	Indicates which of the 5 downstream OFDM channel profiles is to be copied	
1.1910.3	DS copy in process	1 = the active downstream profile is being copied to the off-line profile 0 = the downstream off-line profile is not being modified by a profile copy	RO
1.1910.2	DS profile copy	1 = initiates a copy of the active downstream profile to the off-line profile 0 = normal	R/W, SC
1.1910.1:0	DS configuration ID	Controls switching the active downstream profile	RO

[a]R/W = Read/Write, RO = Read only, SC = Self-clearing

45.2.1.184.1 US copy in process (1.1910.11)

When read as one, bit 1.1910.11 indicates that a copy of the currently active upstream profile to the inactive profile is in process, writes to all upstream profile descriptors and their respective registers (see 45.2.8.3 and 102.4.5) are ignored, and switching between profiles (see 102.2.3.1.1) is prohibited. This bit is a reflection of the variable *US_CpyInP* defined in 102.4.5.1.

45.2.1.184.2 US profile copy (1.1910.10)

When bit 1.1910.10 is set to one, a copy of the currently active upstream profile to the inactive profile is initiated and will continue to completion. This bit is set to zero by the PMA/PMD on or before completion of the profile copy. This bit is a reflection of the variable *US_PrflCpy* defined in 102.4.5.1.

45.2.1.184.3 US configuration ID (1.1910.9:8)

Bits 1.1910.9:8 indicate the value of the most recently received upstream Configuration ID bits (see 102.2.3.1). These bits are a reflection of the variable *US_CID* defined in 102.2.7.3.

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45.2.1.184.4 DS copy channel ID (1.1910.6:4)

Bits 1.1910.6:4 indicate which one of the five downstream ODFM channel profiles is to be copied. These bits are a reflection of the *DS_CpyCh* variable defined in 102.4.5.1.

45.2.1.184.5 DS copy in process (1.1910.3)

When read as one, bit 1.1910.3 indicates that a copy of the currently active downstream profile to the inactive profile is in process, writes to all downstream profile descriptors and their respective registers (see 45.2.8.2 and 102.4.5) are ignored, and switching between profiles (see 102.2.3.1.1) is prohibited. This bit is a reflection of the variable *DS_CpyInP* defined in 102.4.5.1.

45.2.1.184.6 DS profile copy (1.1910.2)

When bit 1.1910.2 is set to one, a copy of the currently active downstream profile to the inactive profile is initiated and will continue to completion. This bit is set to zero by the PMA/PMD on or before completion of the profile copy. This bit is a reflection of the variable *DS_PrflCpy* defined in 102.4.5.1.

45.2.1.184.7 DS configuration ID (1.1910.1:0)

Bits 1.1910.1:0 indicate the value of the most recently received downstream Configuration ID bits (see 102.2.3.1). These bits are a reflection of the variable *DS_CID* defined in 102.2.7.3.

45.2.1.185 DS PHY Link control register (Register 1.1911)

The assignment of bits in the DS PHY Link control register is shown in Table 45–149.

Table 45–149—DS PHY Link control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1911.15:12	Reserved	Value always 0	RO
1.1911.11:0	DS PHY Link start	DS PHY Link starting subcarrier	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.185.1 DS PHY Link start (1.1911.11:0)

Bits 1.1911.11:0 set the starting subcarrier number of the downstream 10GPASS-XR PHY Link. They indicate the lowest frequency subcarrier of the downstream PHY Link used to carry PHY Link information bits. See 102.2 for additional details on the downstream PHY Link. These bits are a reflection of the variable *DS_PhyLinkStrt* defined in 102.2.6.

45.2.1.186 US PHY Link control register (Register 1.1912)

The assignment of bits in the US PHY Link control register is shown in Table 45–150.

45.2.1.186.1 US PHY Link modulation (1.1912.15:12)

Bits 1.1912.15:12 are used to set the modulation type of the upstream PHY Link. These bits are a reflection of the *US_PhyLinkMod* variable defined in 102.3.5.3 with bits 1.1912.15:12 mapping to bits 3:0 of *US_PhyLinkMod*, respectively.

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Table 45–150—US PHY Link control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1912.15:12	US PHY Link modulation	US PHY Link modulation type	R/W
1.1912.11:0	US PHY Link start	US PHY Link starting subcarrier	R/W

[a]R/W = Read/Write

45.2.1.186.2 US PHY Link start (1.1912.11:0)

Bits 1.1912.11:0 set the starting subcarrier number of the upstream 10GPASS-XR PHY Link. They indicate the lowest frequency subcarrier of the upstream PHY Link used to carry PHY Link information bits. See 102.3 for additional details on the upstream PHY Link. These bits are a reflection of the variable *US_PhyLinkStrt* defined in 102.3.5.3.

45.2.1.187 PHY Discovery control registers (Registers 1.1913 and 1.1914)

The PHY Discovery process is used to bring up new CNUs on the EPoC coax cable distribution network. Registers 1.1913 and 1.1914 indicate when the next PHY Discovery window is opened relative to the downstream Timestamp with bit 1.1913.0 being the LSB and bit 1.1914.15 being the MSB. Setting the PHY Discovery start parameter to zero disables the PHY Discovery window. The PHY Discovery control registers direct this process, which is described in 102.4.1. The assignment of bits in the PHY Discovery control registers is shown in Table 45–151. These registers are a reflection of the *DiscStrt* variable defined in 102.2.3.2.4.

Table 45–151—PHY Discovery control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1913.15:0	PHY Discovery start lower	Time of next open PHY Discovery window bits [15:0]	R/W, MW
1.1914.15:0	PHY Discovery start upper	Time of next open PHY Discovery window bits [31:16]	R/W, MW

[a] R/W = Read/Write, MW = Multi-word

45.2.1.188 New CNU control register (Register 1.1915)

The assignment of bits in the New CNU control register is shown in Table 45–152. Additional information on the use of the New CNU control register can be found in 102.4.1.6 and 102.4.3.

45.2.1.188.1 CNU_ID assigned flag 1 (1.1915.15)

Bit 1.1915.15 indicates if the associated CNU_ID value has been assigned to a CNU by the PHY. When this bit is set to one, the associated CNU_ID has been assigned to a CNU. When this bit is set to zero the associated CNU_ID has not been assigned. See 102.4.1.6 and 102.4.3 for additional details on the use of this flag. This bit is a reflection of the variable *AssgndCNU_ID* defined in 102.4.1.8.

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Table 45–152—New CNU control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1915.15	CNU_ID assigned flag	1 = the allowed CNU_ID value has been assigned to a CNU 0 = the allowed CNU_ID value has not been assigned to a CNU	R/W
1.1915.14:0	Allowed CNU_ID	A new CNU may be assigned this value for CNU_ID if the CNU_ID assigned flag is FALSE	R/W

[a]R/W = Read/Write

45.2.1.188.2 Allowed CNU_ID (1.1915.14:0)

Bits 1.1915.14:0 indicate to the 10GPASS-XR PHY a valid CNU_ID value. The value may be assigned to a new CNU when the CNU_ID assigned flag (bit 1.1915.15) is set to zero, when the flag is set to one it is an indication that this value has already been assigned to a CNU and it should not be use for another CNU. These bits are a reflection of the *AllwdCNU_ID* variable defined in 102.4.1.8.

45.2.1.189 New CNU info registers 1 through 5 (Registers 1.1916 through 1.1920)

The assignment of bits in the New CNU info registers 1 through 5 is shown in Table 45–153. Additional information on the use of the New CNU info registers see 102.4.3.

Table 45–153—New CNU info registers 1 through 5 bit definitions

Bit(s)	Name	Description	R/W[a]
1.1916.15:0	New CNU range	The range of the CNU corresponding to Allowed CNU_ID	RO
1.1917.15:0	New CNU MAC 0	MAC address bits [15:0] of the CNU corresponding to Allowed CNU_ID	RO, MW
1.1918.15:0	New CNU MAC 1	MAC address bits [31:16] of the CNU corresponding to Allowed CNU_ID	RO, MW
1.1919.15:0	New CNU MAC 2	MAC address bits [47:32] of the CNU corresponding to Allowed CNU_ID	RO, MW
1.1920.15:0	Reserved	Value always 0	RO

[a]RO = Read only, MW = Multi-word

45.2.1.189.1 New CNU range (1.1916.15:0)

Register 1.1916 forms an integer that indicates the range of the CNU corresponding to Allowed CNU_ID (see 102.4.1.6) in units of OFDM Clock periods (1/204.8 MHz). This register is a reflection of the variable *NewCNU_Rng* defined in 102.4.1.8.

45.2.1.189.2 New CNU MAC 0 through 2 (1.1917.15:0 through 1.1919.15:0)

Registers 1.1917 through 1.1919 hold the MAC address of the CNU, as determined by the PHY Discovery process, corresponding to Allowed CNU_ID (see 45.2.1.188) with bit 1.1917.0 being the LSB and 1.1919.15 being the MSB. These registers are a reflection of the variable *New_MAC* defined in 102.4.1.9.2.

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45.2.1.190 DS PHY Link frame counter (Register 1.1921)

Register 1.1921 represents the DS PHY Link frame count. This counter is incremented at the beginning of the PHY Link frame and, on terminal count, rolls over to zero. The assignment of bits in the DS PHY Link frame counter is shown in Table 45–154.

Table 45–154—DS PHY Link frame counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.1921.15:0	PHY Link frame counter	Counter that indicates the PHY Link frame currently being processed by the PHY. This counter rolls over to zero and is incremented at the beginning of each PHY Link frame	RO

[a]RO = Read only

45.2.1.191 PMA/PMD timing offset register (Registers 1.1922 and 1.1923)

The assignment of bits in the PMA/PMD timing offset registers is shown in Table 45–155. Registers 1.1923 and 1.1922 form an offset, in units of OFDM Clock periods (1/204.8 MHz), used to align the CNU to the upstream OFDM timing. For more information on the use of this register see 102.4.1.6. These registers are a reflection of the variable *PhyTimingOffset* defined in 102.4.1.8.

Table 45–155—PMA/PMD timing offset register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1922.15:0	PMA/PMD timing offset lower	Transmit timing offset [15:0]	R/W, MW
1.1923.15:0	PMA/PMD timing offset upper	Transmit timing offset [31:16]	R/W, MW

[a]R/W = Read/Write, MW = Multi-word

45.2.1.192 PMA/PMD power offset register (Register 1.1924)

The assignment of bits in the PMA/PMD power offset register is shown in Table 45–156.

Table 45–156—PMA/PMD power offset register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1924.15:8	Reserved	Value always 0	RO
1.1924.7:0	PMA/PMD power offset	TX Power offset	R/W

[a] RO = Read Only, R/W = Read/Write

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45.2.1.192.1 PMA/PMD power offset (1.1924.7:0)

Bits 1.1924.7:0 represent a power offset, in units of 0.25 dB, the CNU is to make in order that transmissions arrive at the CLT at the desired power level. For more information on the use of these bits see 102.4.1.6. These bits are a reflection of the variable *PhyPowerOffset* defined in 102.4.1.8.

45.2.1.193 PMA/PMD ranging offset registers (Registers 1.1925 and 1.1926)

Registers 1.1925 and 1.1926 represent the PMA/PMD ranging offset parameter, in units of OFDM Clock periods (1/204.8 MHz). The assignment of bits in the PMA/PMD ranging offset register is shown in Table 45–157. These registers are a reflection of the variable *PhyRngOffset* defined in 102.4.1.8.

Table 45–157—PMA/PMD ranging offset registers bit definitions

Bit(s)	Name	Description	R/W[a]
1.1925.15:0	PMA/PMD ranging offset lower	PMA/PMD ranging offset register bits [15:0]	R/W, MW
1.1926.15:0	PMA/PMD ranging offset upper	PMA/PMD ranging offset register bits [31:16]	R/W, MW

[a]R/W = Read/Write, MW = Multi-word

45.2.1.194 DS PMA/PMD data rate registers (Registers 1.1927, 1.1928 and 1.1929)

Registers 1.1927, 1.1928, and 1.1929 represent the downstream data rate, in units of b/s. Bit 1.1929.4 is the MSB and bit 1.1927.0 is the LSB of the value. The bit assignments for the DS Data Rate registers is illustrated in Table 45–158. These registers are a reflection of the variable *DS_DataRate* defined in 100.3.2.3.

Table 45–158—DS PMA/PMD data rate register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1927.15:3	DS PMA/PMD data rate lower	The downstream PMA/PMD data rate bits [15:3] of a UQ34.3 formatted number	RO, MW
1.1927.2:0	DS PMA/PMD data rate fractional	The downstream PMA/PMD data rate bits [2:0] of a UQ34.3 formatted number	RO, MW
1.1928.15:0	DS PMA/PMD data rate mid	The downstream PMA/PMD data rate bits [31:16] of a UQ34.3 formatted number	RO, MW
1.1929.15:5	Reserved	Value always 0	RO
1.1929.4:0	DS PMA/PMD data rate upper	The downstream PMA/PMD data rate bits [36:32] of a UQ34.3 formatted number	RO, MW

[a]RO = read only, MW = Multi-word

45.2.1.195 US PMA/PMD data rate registers (Registers 1.1930, 1.1931 and 1.1932)

Registers 1.1930, 1.1931, and 1.1932 represent the upstream data rate in units of b/s. Bit 1.1932.4 is the MSB and bit 1.1930.0 is the LSB of the value. The bit assignments for the US Data Rate registers is illustrated in Table 45–159. These registers are a reflection of the variable *US_DataRate* defined in 100.3.2.3.

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Table 45–159—US PMA/PMD data rate register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1930.15:3	US PMA/PMD data rate lower	The upstream PMA/PMD data rate bits [15:3] of a UQ34.3 formatted number	RO, MW
1.1930.2:0	US PMA/PMD data rate fractional	The upstream PMA/PMD data rate bits [2:0] of a UQ34.3 formatted number	RO, MW
1.1931.15:0	US PMA/PMD data rate mid	The upstream PMA/PMD data rate bits [31:16] of a UQ34.3 formatted number	RO, MW
1.1932.15:5	Reserved	Value always 0	RO
1.1932.4:0	US PMA/PMD data rate upper	The upstream PMA/PMD data rate bits [36:32] of a UQ34.3 formatted number	RO, MW

[a]RO = read only, MW = Multi-word

45.2.1.196 10GPASS-XR FEC codeword counter (Registers 1.1933, 1.1934)

The assignment of bits in the 10GPASS-XR FEC codeword counter is shown in Table 45–160. Registers 1.1933 and 1.1934 are used to read the value of a 32-bit counter. When registers 1.1933 and 1.1934 are used to read the 32-bit counter value, the register 1.1933 is read first, the value of the register 1.1934 is latched when (and only when) register 1.1933 is read and reads of register 1.1934 return the latched value rather than the current value of the counter. These registers are a reflection of the variable *FecCodeWordCount* defined in 101.3.3.1.6.

Table 45–160—10GPASS-XR FEC codeword counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.1933.15:0	FEC codeword counter lower	Total FEC codewords counter [15:0]	RO, MW
1.1934.15:0	FEC codeword counter upper	Total FEC codewords counter [31:0]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.1.197 10GPASS-XR FEC codeword success counter (Registers 1.1935 and 1.1936)

The assignment of bits in the 10GPASS-XR FEC codeword success counter is shown in Table 45–161. Registers 1.1935 and 1.1936 are used to read the value of a 32-bit counter. When registers 1.1935 and 1.1936 are used to read the 32-bit counter value, the register 1.1935 is read first, the value of the register 1.1936 is latched when (and only when) register 1.1935 is read and reads of register 1.1936 return the latched value

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rather than the current value of the counter. These registers are a reflection of the variable *FecCodeWordSuccess* defined in 101.3.3.1.6.

Table 45–161—10GPASS-XR FEC codeword success counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.1935.15:0	FEC codeword success counter lower	Total FEC codewords successfully decoded counter bits [15:0]	RO, MW
1.1936.15:0	FEC codeword success counter upper	Total FEC codewords successfully decoded counter bits [31:0]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.1.198 10GPASS-XR FEC codeword fail counter (Registers 1.1937 and 1.1938)

The assignment of bits in the 10GPASS-XR FEC codeword fail counter is shown in Table 45–162. Registers 1.1937 and 1.1938 are used to read the value of a 32-bit counter. When registers 1.1937 and 1.1938 are used to read the 32-bit counter value, the register 1.1937 is read first, the value of the register 1.1938 is latched when (and only when) register 1.1937 is read and reads of register 1.1938 return the latched value rather than the current value of the counter. These registers are a reflection of the variable *FecCodeWordFail* defined in 101.3.3.1.6.

Table 45–162—10GPASS-XR FEC codeword fail counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.1937.15:0	FEC codeword fail counter lower	Total FEC codewords unsuccessfully decoded counter bits [15:0]	RO, MW
1.1938.15:0	FEC codeword fail counter upper	Total FEC codewords unsuccessfully decoded counter bits [31:0]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.1.199 PHY Link EPFH counter (Register 1.1939)

The assignment of bits in the PHY Link EPFH counter is shown in Table 45–163. This register is reset to all zeros when read by the management function or upon PMA/PMD reset. These bits are held at all ones in the case of overflow. This register is a reflection of the counter *EPFHcnt* defined in 102.2.7.2.

Table 45–163—PHY Link EPFH counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.1939.15:0	PHY Link EPFH counter	Total PHY Link EPFH message blocks received [15:0]	RO, NR

[a]RO = Read only, NR = Non Roll-over

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45.2.1.200 PHY Link EPFH error counter (Register 1.1940)

The assignment of bits in the PHY Link EPFH error counter is shown in Table 45–164. This register is reset to all zeros when read by the management function or upon PMA/PMD reset. These bits are held at all ones in the case of overflow. This register is a reflection of the counter *EPFHerr* defined in 102.2.7.2.

Table 45–164—PHY Link EPFH error counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.1940.15:0	PHY Link EPFH error counter	Total PHY Link EPFH message blocks received with CRC32 errors [15:0]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.201 PHY Link EPCH counter (Register 1.1941)

The assignment of bits in the PHY Link EPCH counter is shown in Table 45–165. This register is reset to all zeros when read by the management function or upon PMA/PMD reset. These bits are held at all ones in the case of overflow. This register is a reflection of the counter *EPCHcnt* defined in 102.2.7.2.

Table 45–165—PHY Link EPCH counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.1941.15:0	PHY Link EPCH counter	Total PHY Link EPCH message blocks received [15:0]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.202 PHY Link EPCH error counter (Register 1.1942)

The assignment of bits in the PHY Link EPCH error counter is shown in Table 45–166. This register is reset to all zeros when read by the management function or upon PMA/PMD reset. These bits are held at all ones in the case of overflow. This register is a reflection of the counter *EPCHerr* defined in 102.2.7.2.

Table 45–166—PHY Link EPCH error counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.1942.15:0	PHY Link EPCH error counter	Total PHY Link EPCH message blocks received with CRC32 errors [15:0]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.203 PHY Link EMB counter (Register 1.1943)

The assignment of bits in the PHY Link EMB counter is shown in Table 45–167. This register is reset to all zeros when read by the management function or upon PMA/PMD reset. These bits are held at all ones in the case of overflow. This register is a reflection of the counter *EMBcnt* defined in 102.2.7.2.

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Table 45–167—PHY Link EMB counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.1943.15:0	PHY Link EMB counter	Total PHY Link EMB message blocks received [15:0]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.204 PHY Link EMB error counter (Register 1.1944)

The assignment of bits in the PHY Link EMB error counter is shown in Table 45–168. This register is reset to all zeros when read by the management function or upon PMA/PMD reset. These bits are held at all ones in the case of overflow. This register is a reflection of the counter *EMBerr* defined in 102.2.7.2.

Table 45–168—PHY Link EMB error counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.1944.15:0	PHY Link EMB error counter	Total PHY Link EMB message blocks received with CRC32 errors [15:0]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.205 PHY Link FPMB counter (Register 1.1945)

The assignment of bits in the PHY Link FPMB counter is shown in Table 45–169. This register is reset to all zeros when read by the management function or upon PMA/PMD reset. These bits are held at all ones in the case of overflow. This register is a reflection of the counter *FPMBcnt* defined in 102.1.8.

Table 45–169—PHY Link FPMB counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.1945.15:0	PHY Link FPMB counter	Total PHY Link FPMB message blocks received [15:0]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.206 PHY Link FPMB error counter (Register 1.1946)

The assignment of bits in the PHY Link FPMB error counter is shown in Table 45–170. This register is reset to all zeros when read by the management function or upon PMA/PMD reset. These bits are held at all ones in the case of overflow. This register is a reflection of the counter *FPMBerr* defined in 102.1.8.

Table 45–170—PHY Link FPMB error counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.1946.15:0	PHY Link FPMB error counter	Total PHY Link FPMB message blocks received with CRC32 errors [15:0]	RO, NR

[a]RO = Read only, NR = Non Roll-over

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45.2.1.207 US PHY Link response time register (Register 1.1947)

The assignment of bits in the US PHY Link response time register is shown in Table 45–171. These bits indicate the time, in units of OFDM Clock periods (1/204.8 MHz), required by a CNU to respond to an EPoC message block received on the PHY Link and are a reflection of the variable *PhyLinkRspTm* defined in 102.2.7.3.

Table 45–171—US PHY Link response time register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1947.15:0	US PHY Link response time	Time required by a CNU to respond to an EPoC message block	RO

[a]RO = Read only

45.2.1.208 10GPASS-XR modulation ability register (Register 1.1948)

The assignment of bits in the 10GPASS-XR modulation ability register is shown in Table 45–172.

Table 45–172—10GPASS-XR modulation ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1948.15:10	Reserved	Value always 0	RO
1.1948.9:8	US modulation ability	Indicates the PHYs ability to support optional upstream modulation types	RO
1.1948.7:5	DS OFDM channel ability	Indicates the number of downstream ODFM channels supported	RO
1.1948.4:0	DS modulation ability	Indicates the PHYs ability to support optional downstream modulation types	RO

[a]RO = Read only

45.2.1.208.1 US modulation ability (1.1948.9:8)

Bits 1.1948.9:8 indicate the ability of the PHY to support optional upstream modulation formats 4096-QAM and 2048-QAM. These bits are a reflection of the variable *US_ModAbility* defined in 101.4.4.4.4.

45.2.1.208.2 DS OFDM channel ability (1.1948.7:5)

Bits 1.19487:5 indicate the number of OFDM channels the PMA/PMD is able to support in the downstream direction. The value of these bits is between 1 and 5 inclusive. These bits are a reflection of the variable *DS_OFDM_ChAbility* defined in 101.4.3.4.5.

45.2.1.208.3 DS modulation ability (1.1948.4:0)

Bits 1.1948.4:0 indicate the ability of the PHY to support optional downstream modulation formats 16384-QAM, 8192-QAM, 32-QAM, 16-QAM, and 8-QAM. These bits are a reflection of variable *DS_ModAbility* defined in 101.4.3.4.5.

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45.2.1.209 PHY Discovery Response power control register (Register 1.1949)

The assignment of bits in the PHY Discovery Response power control register is shown in Table 45–173.

Table 45–173—PHY Discovery Response power control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1949.15:8	PHY Discovery Response power step	Indicate the power increase of the PHY Discovery Response if there is no acknowledgment	R/W
1.1949.7:0	PHY Discover Response initial power	Initial power for CNU PHY Discovery Response	R/W

[a]R/W = Read/Write

45.2.1.209.1 PHY Discovery Response power step (1.1949.15:8)

Bits 1.1949.15:8 indicate to the CNU the amount of power to increase, in units of 0.25 dB, the PHY Discovery Response by if there is no acknowledgment from the CLT to a PHY Discovery Response from the CNU. These bits are a reflection of the *PdRespPwrStep* variable defined in 102.4.1.8.

45.2.1.209.2 PHY Discover Response initial power (1.1949.7:0)

Bits 1.1949.7:0 indicate to the CNU the initial power to be used when transmitting the PHY Discovery Response in units of 0.25 dBmV/1.6 MHz. These bits are a reflection of the *PdRespInitPwr* variable defined in 102.4.1.8.

45.2.1.210 US target receive power register (Register 1.1950)

The assignment of bits in the US target receive power register is shown in Table 45–174. Bits 1.1950.9:0 are used to set the target upstream receive power, in units of 0.1 dBmV/6.4 MHz, and are a reflection of the *CLT_TargetReceivePower* variable defined in 100.3.5.1. These bits are valid only for 10GPASS-XR-D PMA/PMD and are reserved for 10GPASS-XR-U PMA/PMD and always read as zero.

Table 45–174—US target receive power register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1950.15:10	Reserved	Value always 0	RO
1.1950.9:0	US target receive power	Sets the target upstream receive power	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.211 DS transmit power registers (Registers 1.1951 through 1.1955)

The assignment of bits in the DS transmit power registers is shown in Table 45–175.

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Table 45–175—DS transmit power registers bit definitions

Bit(s)	Name	Description	R/W[a]
1.1951.15:9	Reserved	Value always 0	RO
1.1951.8:0	DS transmit power Ch 1	Sets the transmit power for OFDM channel 1	R/W
1.1952.15:9	Reserved	Value always 0	RO
1.1952.8:0	DS transmit power Ch 2	Sets the transmit power for OFDM channel 2	R/W
1.1953.15:9	Reserved	Value always 0	RO
1.1953.8:0	DS transmit power Ch 3	Sets the transmit power for OFDM channel 3	R/W
1.1954.15:9	Reserved	Value always 0	RO
1.1954.8:0	DS transmit power Ch 4	Sets the transmit power for OFDM channel 4	R/W
1.1955.15:9	Reserved	Value always 0	RO
1.1955.8:0	DS transmit power Ch 5	Sets the transmit power for OFDM channel 5	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.211.1 DS transmit power Ch1 (1.1951.8:0)

Bits 1.1951.8:0 are used to set the transmit level of the downstream OFDM channel 1, in units of 0.2 dBmV/6 MHz. These bits are a reflection of the *DS_PowerCh(1)* variable defined in 100.3.3.2.1. These bits are valid only for 10GPASS-XR-D PMA/PMD and are reserved for 10GPASS-XR-U PMA/PMD and always read as zero.

45.2.1.211.2 DS transmit power Ch2 (1.1952.8:0)

Bits 1.1952.8:0 are used to set the transmit level of the downstream OFDM channel 2, in units of 0.2 dBmV/6 MHz. These bits are a reflection of the *DS_PowerCh(2)* variable defined in 100.3.3.2.1. These bits are valid only for 10GPASS-XR-D PMA/PMD and are reserved for 10GPASS-XR-U PMA/PMD and always read as zero.

45.2.1.211.3 DS transmit power Ch3 (1.1953.8:0)

Bits 1.1953.8:0 are used to set the transmit level of the downstream OFDM channel 3, in units of 0.2 dBmV/6 MHz. These bits are a reflection of the *DS_PowerCh(3)* variable defined in 100.3.3.2.1. These bits are valid only for 10GPASS-XR-D PMA/PMD and are reserved for 10GPASS-XR-U PMA/PMD and always read as zero.

45.2.1.211.4 DS transmit power Ch4 (1.1954.8:0)

Bits 1.1954.8:0 are used to set the transmit level of the downstream OFDM channel 4, in units of 0.2 dBmV/6 MHz. These bits are a reflection of the *DS_PowerCh(4)* variable defined in 100.3.3.2.1. These bits are valid only for 10GPASS-XR-D PMA/PMD and are reserved for 10GPASS-XR-U PMA/PMD and always read as zero.

45.2.1.211.5 DS transmit power Ch5 (1.1955.8:0)

Bits 1.1955.8:0 are used to set the transmit level of the downstream OFDM channel 5, in units of 0.2 dBmV/6 MHz. These bits are a reflection of the *DS_PowerCh(5)* variable defined in 100.3.3.2.1. These

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bits are valid only for 10GPASS-XR-D PMA/PMD and are reserved for 10GPASS-XR-U PMA/PMD and always read as zero.

45.2.1.212 US receive power measurement registers (1.1956 through 1.1957)

The assignment of bits in the US receive power measurement registers is shown in Table 45–176.

Table 45–176—US receive power measurement registers bit definitions

Bit(s)	Name	Description	R/W[a]
1.1956.15	US receive power valid	Indicates the value in US receive power measurement is valid	RO
1.1956.14:9	Reserved	Value always 0	RO
1.1956.8:0	US receive power measurement	Indicate the measured receive power for the CNU identified by US receive power CNU	RO
1.1957:15	Reserved	Value always 0	RO
1.1957.14:0	US receive power CNU	Indicates the CNU on which to measure the receive power	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.212.1 US receive power valid (1.1956.15)

When read as one, bit 1.1956.15 indicates the value in the US receive power measurement is valid for the CNU identified by US receive power CNU. This bit is only valid for 10GPASS-XR-D PMA/PMD and is reserved for 10GPASS-XR-U PMA/PMD and always reads as zero. This bit is a reflection of the variable *RxPwrValid* defined in 100.4.3.1.

45.2.1.212.2 US receive power measurement (1.1956.8:0)

Bits 1.1956.8:0 report the received power, in units of 0.1 dBmV, for the CNU identified by US receive power CNU. These bits are only valid for 10GPASS-XR-D PMA/PMD and are reserved for 10GPASS-XR-U PMA/PMD and always read as zero. These bits are a reflection of the variable *RxPwr* defined in 100.4.3.1.

45.2.1.212.3 US receive power CNU (1.1957.14:0)

When set to a CNU_ID bits 1.1957.14:0 indicate which CNU the CLT is to measure the received power on. These bits are only valid for 10GPASS-XR-D PMA/PMD and are reserved for 10GPASS-XR-U PMA/PMD and always read as zero. These bits are a reflection of the variable *RxPwr_CNU_ID* defined in 100.4.3.1.

45.2.1.213 Reported power register (1.1958)

The assignment of bits in the Reported power register is shown in Table 45–177.

45.2.1.213.1 Reported power (1.1958.8:0)

Bits 1.1958.8:0 indicate the reported power output of the PMA/PMD in units of 0.25 dBmv. These bits are a reflection of the variable *ReportedPwr* defined in 100.3.4.3.1.

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Table 45–177—Reported power register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1958.15:9	Reserved	Value always 0	RO
1.1958.8:0	Reported power	The reported output power for the PMA/PMD	RO

[a]RO = Read only

45.2.1.214 BASE-T1 PMA/PMD control register (Register 1.2100)

The assignment of bits in the BASE-T1 PMA/PMD control register is shown in Table 45–178.

Table 45–178—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2100.15	Reserved	Value always 1	RO
1.2100.14	MASTER-SLAVE config value	1 = Configure PHY as MASTER 0 = Configure PHY as SLAVE	R/W
1.2100.13:4	Reserved	Value always 0	RO
1.2100.3:0	Type Selection	3 2 1 0 1 x x x = Reserved 0 1 1 1 = Reserved 0 1 1 0 = 10GBASE-T1 0 1 0 1 = 5GBASE-T1 0 1 0 0 = 2.5GBASE-T1 0 0 1 1 = 10BASE-T1S 0 0 1 0 = 10BASE-T1L 0 0 0 1 = 1000BASE-T1 0 0 0 0 = 100BASE-T1	R/W

[a]RO = Read only, R/W = Read/Write

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

45.2.1.214.1 MASTER-SLAVE config value (1.2100.14)

Bit 1.2100.14 is used to select MASTER or SLAVE operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. If bit 1.2100.14 is set to one the PHY shall operate as MASTER. If bit 1.2100.14 is set to zero the PHY shall operate as SLAVE. This bit shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

45.2.1.214.2 Type selection (1.2100.3:0)

Bits 1.2100.3:0 are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. When these bits are set to 0000, the mode of operation is 100BASE-T1. When these bits are set to 0001, the mode of operation is 1000BASE-T1. When these bits are set to 0010, the mode of operation is 10BASE-T1L. When these bits are set to 0011, the mode of operation is 10BASE-T1S. When these bits are set to 0100, the mode of operation is 2.5GBASE-T1. When these bits are

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set to 0101, the mode of operation is 5GBASE-T1. When these bits are set to 0110, the mode of operation is 10GBASE-T1. These bits shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

45.2.1.215 100BASE-T1 PMA/PMD test control register (Register 1.2102)

The assignment of bits in the 100BASE-T1 PMA/PMD test control register is shown in Table 45–179.

Table 45–179—100BASE-T1 PMA/PMD test control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2102.15:13	100BASE-T1 test mode control	15 14 13 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Reserved 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal operation	R/W
1.2102.12:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

45.2.1.215.1 100BASE-T1 test mode control (1.2102.15:13)

100BASE-T1 test mode control operations are selected using bits 1.2102.15:13. The default value for bits 1.2102.15:13 is 000.

45.2.1.216 IFEC control register (Register 1.2200)

The assignment of bits in the IFEC control register is shown in Table 45–180.

Table 45–180—IFEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2200.15:2	Reserved	Value always 0	RO
1.2200.1	IFEC bypass indication enable	1 = IFEC decoder does not indicate errors 0 = IFEC decoder indicates errors	R/W
1.2200.0	IFEC bypass correction enable	1 = IFEC decoder performs error detection without error correction 0 = IFEC decoder performs error detection and error correction	R/W

[a]R/W = Read/Write, RO = Read only

45.2.1.216.1 IFEC bypass indication enable (1.2200.1)

This bit enables the Inverse RS-FEC decoder to bypass error indication to the far end (PCS) through the sync bits for the BASE-R PHY in the remote device. When set to one, this bit enables bypass of the error indication function. When set to zero, errors are indicated to the remote PCS through the sync bits. Writes to

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bit 1.2200.1 are ignored and reads return a zero if the Inverse RS-FEC does not have the ability to bypass decoding error indications to the remote PCS layer (see 152.5.2.3).

45.2.1.216.2 IFEC bypass correction enable (1.2200.0)

When bit 1.2200.0 is set to one the Inverse RS-FEC decoder performs error detection without error correction (see 152.5.2.3). When this bit is set to zero, the decoder also performs error correction. Writes to this bit are ignored and reads return a zero if the Inverse RS-FEC does not have the ability to bypass error correction.

45.2.1.217 IFEC status register (Register 1.2201)

The assignment of bits in the IFEC status register is shown in Table 45–181.

Table 45–181—IFEC status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2201.15	PCS align status	1 = IFEC encoder has locked and aligned all PCS lanes 0 = IFEC encoder has not locked and aligned all PCS lanes	RO
1.2201.14	IFEC align status	1 = IFEC receive lanes locked and aligned 0 = IFEC receive lanes not locked and aligned	RO
1.2201.13:12	Reserved	Value always 0	RO
1.2201.11	IFEC AM lock 3	1 = IFEC lane 3 locked and aligned 0 = IFEC lane 3 not locked and aligned	RO
1.2201.10	IFEC AM lock 2	1 = IFEC lane 2 locked and aligned 0 = IFEC lane 2 not locked and aligned	RO
1.2201.9	IFEC AM lock 1	1 = IFEC lane 1 locked and aligned 0 = IFEC lane 1 not locked and aligned	RO
1.2201.8	IFEC AM lock 0	1 = IFEC lane 0 locked and aligned 0 = IFEC lane 0 not locked and aligned	RO
1.2201.7:3	Reserved	Value always 0	RO
1.2201.2	IFEC high SER	1 = IFEC errors have exceeded threshold 0 = IFEC errors have not exceeded threshold	RO/LH
1.2201.1	IFEC bypass indication ability	1 = IFEC decoder has the ability to bypass error indication 0 = IFEC decoder does not have the ability to bypass error indication	RO
1.2201.0	IFEC bypass correction ability	1 = IFEC decoder has the ability to bypass error correction 0 = IFEC decoder does not have the ability to bypass error correction	RO

[a]RO = Read only, LH = Latching high

45.2.1.217.1 PCS align status (1.2201.15)

Bit 1.2201.15 indicates the PCS alignment status of the Inverse RS-FEC. For the Inverse RS-FEC described in Clause 152, PCS alignment is defined as block lock, alignment marker lock, and deskew of all 20 receive PCS lanes. When read as a zero, bit 1.2201.15 indicates that the Inverse RS-FEC has not obtained PCS

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alignment. When read as a one, bit 1.2201.15 indicates that the Inverse RS-FEC has obtained PCS alignment.

45.2.1.217.2 IFEC align status (1.2201.14)

Bit 1.2201.14 indicates the alignment status of the Inverse RS-FEC. For the Inverse RS-FEC described in Clause 152, IFEC alignment is defined as alignment marker lock and deskew of all four lanes on the IFEC service interface. When read as a zero, bit 1.2201.14 indicates that the Inverse RS-FEC has not obtained IFEC alignment. When read as a one, bit 1.2201.14 indicates that the Inverse RS-FEC has obtained IFEC alignment.

45.2.1.217.3 IFEC AM lock 3 (1.2201.11)

When read as a one, bit 1.2201.11 indicates that the Inverse RS-FEC described in Clause 152 has locked and aligned lane 3 of the IFEC service interface. When read as a zero, bit 1.2201.11 indicates that the Inverse RS-FEC has not locked and aligned lane 3 of the IFEC service interface. This bit reflects the state of amps_lock[3] (see 152.5.2.1).

45.2.1.217.4 IFEC AM lock 2 (1.2201.10)

When read as a one, bit 1.2201.10 indicates that the Inverse RS-FEC described in Clause 152 has locked and aligned lane 2 of the IFEC service interface. When read as a zero, bit 1.2201.10 indicates that the Inverse RS-FEC has not locked and aligned lane 2 of the IFEC service interface. This bit reflects the state of amps_lock[2] (see 152.5.2.1).

45.2.1.217.5 IFEC AM lock 1 (1.2201.9)

When read as a one, bit 1.2201.9 indicates that the Inverse RS-FEC described in Clause 152 has locked and aligned lane 1 of the IFEC service interface. When read as a zero, bit 1.2201.9 indicates that the Inverse RS-FEC has not locked and aligned lane 1 of the IFEC service interface. This bit reflects the state of amps_lock[1] (see 152.5.2.1).

45.2.1.217.6 IFEC AM lock 0 (1.2201.8)

When read as a one, bit 1.2201.8 indicates that the Inverse RS-FEC described in Clause 152 has locked and aligned lane 0 of the IFEC service interface. When read as a zero, bit 1.2201.8 indicates that the Inverse RS-FEC has not locked and aligned lane 0 of the IFEC service interface. This bit reflects the state of amps_lock[0] (see 152.5.2.1).

45.2.1.217.7 IFEC high SER (1.2201.2)

When bit 1.2200.1 (IFEC bypass indication enable) is set to one, bit 1.2201.2 is set to one if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 152.5.2.3) and is set to zero otherwise. This bit is set to zero if bit 1.2200.1 (IFEC bypass indication enable) is set to zero. This bit shall be implemented with latching high behavior.

45.2.1.217.8 IFEC bypass indication ability (1.2201.1)

The Reed-Solomon decoder may have the option to perform error detection without error indication (see 152.5.2.3) to reduce the delay contributed by the Inverse RS-FEC sublayer. This bit is set to one to indicate that the decoder has this ability to bypass the error indication function. The bit is set to zero if this ability is not supported.

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45.2.1.217.9 IFEC bypass correction ability (1.2201.0)

The Reed-Solomon decoder may have the option to perform error detection without error correction (see 152.5.2.3) to reduce the delay contributed by the Inverse RS-FEC sublayer. This bit is set to one to indicate that the decoder has this ability to bypass error correction. The bit is set to zero if this ability is not supported.

45.2.1.218 IFEC corrected codewords counter (Register 1.2202, 1.2203)

The assignment of bits in the IFEC corrected codewords counter is shown in Table 45–182. See 152.6.8 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.2202 and 1.2203 are used to read the value of a 32-bit counter. When registers 1.2202 and 1.2203 are used to read the 32-bit counter value, register 1.2202 is read first, the value of the register 1.2203 is latched when (and only when) register 1.2202 is read, and reads of register 1.2203 return the latched value rather than the current value of the counter.

Table 45–182—IFEC corrected codewords counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.2202.15:0	IFEC corrected codewords lower	IFEC_corrected_cw_counter[15:0]	RO, NR
1.2203.15:0	IFEC corrected codewords upper	IFEC_corrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.219 IFEC uncorrected codewords counter (Register 1.2204, 1.2205)

The assignment of bits in the IFEC uncorrected codewords counter is shown in Table 45–183. See 152.6.9 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.2204 and 1.2205 are used to read the value of a 32-bit counter. When registers 1.2204 and 1.2205 are used to read the 32-bit counter value, register 1.2204 is read first, the value of the register 1.2205 is latched when (and only when) register 1.2204 is read, and reads of register 1.2205 return the latched value rather than the current value of the counter.

Table 45–183—IFEC uncorrected codewords counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.2204.15:0	IFEC uncorrected codewords lower	IFEC_uncorrected_cw_counter[15:0]	RO, NR
1.2205.15:0	IFEC uncorrected codewords upper	IFEC_uncorrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.220 IFEC lane mapping register (Register 1.2206)

The assignment of bits in the IFEC lane mapping register is shown in Table 45–184. When the RS-FEC detects and locks the RS-FEC for IFEC service interface lane 0, the detected RS-FEC lane number is recorded in bits 1:0 in this register. Similarly, the detected RS-FEC lane numbers for IFEC service lanes 1, 2,

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and 3 are recorded in bits 3:2, 5:4, and 7:6, respectively. The contents of the RS-FEC lane mapping register bits 7:0 are valid when Inverse RS-FEC align status (1.2201.14) is set to one and are invalid otherwise.

Table 45–184—IFEC lane mapping register

Bit(s)	Name	Description	R/W[a]
1.2206.15:8	Reserved	Value always 0	RO
1.2206.7:6	RS-FEC lane 3 mapping	RS-FEC lane mapped to IFEC lane 3	RO
1.2206.5:4	RS-FEC lane 2 mapping	RS-FEC lane mapped to IFEC lane 2	RO
1.2206.3:2	RS-FEC lane 1 mapping	RS-FEC lane mapped to IFEC lane 1	RO
1.2206.1:0	RS-FEC lane 0 mapping	RS-FEC lane mapped to IFEC lane 0	RO

[a]RO = Read only

45.2.1.221 IFEC symbol error counter, lane 0 (Register 1.2210, 1.2211)

The assignment of bits in the IFEC symbol error counter, lane 0 is shown in Table 45–185. Symbol errors detected in FEC lane 0 are counted and shown in bits 1.2210.15:0 and 1.2211.15:0. See 152.6.11 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.2210 and 1.2211 are used to read the value of a 32-bit counter. When registers 1.2210 and 1.2211 are used to read the 32-bit counter value, register 1.2210 is read first, the value of the register 1.2211 is latched when (and only when) register 1.2210 is read, and reads of register 1.2211 return the latched value rather than the current value of the counter.

Table 45–185—IFEC symbol error counter, lane 0 bit definitions

Bit(s)	Name	Description	R/W[a]
1.2210.15:0	IFEC symbol errors, lane 0 lower	IFEC_symbol_error_counter_0[15:0]	RO, NR
1.2211.15:0	IFEC symbol errors, lane 0 upper	IFEC_symbol_error_counter_0[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.222 IFEC symbol error counter, lane 1 through 3 (Register 1.2212, 1.2213, 1.2214, 1.2215, 1.2216, 1.2217)

The behavior of the IFEC symbol error counters, lane 1 through 3 is identical to that described for FEC lane 0 in 45.2.1.221. Errors detected in each FEC lane are counted and shown in the corresponding register. FEC lane 1, lower 16 bits are shown in register 1.2212; FEC lane 1, upper 16 bits are shown in register 1.2213; FEC lane 2, lower 16 bits are shown in register 1.2214; through register 1.2217 for FEC lane 3, upper 16 bits.

45.2.1.223 SC-FEC alignment status 1 register (Register 1.2246)

The assignment of bits in the staircase FEC (SC-FEC) alignment status 1 register is shown in Table 45–186.

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Table 45–186—SC-FEC alignment status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2246.15:13	Reserved	Value always 0	RO
1.2246.12	SC-FEC align status	1 = SC-FEC receive lanes locked and aligned 0 = SC-FEC receive lanes not locked and aligned	RO
1.2246.11:8	Reserved	Value always 0	RO
1.2246.7	SC-FEC FAS lock 7	1 = Lane 7 is locked 0 = Lane 7 is not locked	RO
1.2246.6	SC-FEC FAS lock 6	1 = Lane 6 is locked 0 = Lane 6 is not locked	RO
1.2246.5	SC-FEC FAS lock 5	1 = Lane 5 is locked 0 = Lane 5 is not locked	RO
1.2246.4	SC-FEC FAS lock 4	1 = Lane 4 is locked 0 = Lane 4 is not locked	RO
1.2246.3	SC-FEC FAS lock 3	1 = Lane 3 is locked 0 = Lane 3 is not locked	RO
1.2246.2	SC-FEC FAS lock 2	1 = Lane 2 is locked 0 = Lane 2 is not locked	RO
1.2246.1	SC-FEC FAS lock 1	1 = Lane 1 is locked 0 = Lane 1 is not locked	RO
1.2246.0	SC-FEC FAS lock 0	1 = Lane 0 is locked 0 = Lane 0 is not locked	RO

[a]RO = Read only

45.2.1.223.1 SC-FEC align status (1.2246.12)

When read as a one, bit 1.2246.12 indicates that the SC-FEC has locked and aligned all receive lanes. When read as a zero, bit 1.2246.12 indicates that the SC-FEC has not locked and aligned all receive lanes.

45.2.1.223.2 SC-FEC FAS lock 7 (1.2246.7)

When read as a one, bit 1.2246.7 indicates that the SC-FEC receiver has achieved frame alignment signal (FAS) lock for lane 7 of the PMA service interface. When read as a zero, bit 1.2246.7 indicates that the SC-FEC receiver has not achieved FAS lock for lane 7 of the PMA service interface. This bit reflects the state of fas_lock<7> (see 153.2.4.1.1).

45.2.1.223.3 SC-FEC FAS lock 6 (1.2246.6)

When read as a one, bit 1.2246.6 indicates that the SC-FEC receiver has achieved FAS lock for lane 6 of the PMA service interface. When read as a zero, bit 1.2246.6 indicates that the SC-FEC receiver has not achieved FAS lock for lane 6 of the PMA service interface. This bit reflects the state of fas_lock<6> (see 153.2.4.1.1).

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45.2.1.223.4 SC-FEC FAS lock 5 (1.2246.5)

When read as a one, bit 1.2246.5 indicates that the SC-FEC receiver has achieved FAS lock for lane 5 of the PMA service interface. When read as a zero, bit 1.2246.5 indicates that the SC-FEC receiver has not achieved FAS lock for lane 5 of the PMA service interface. This bit reflects the state of fas_lock<5> (see 153.2.4.1.1).

45.2.1.223.5 SC-FEC FAS lock 4 (1.2246.4)

When read as a one, bit 1.2246.4 indicates that the SC-FEC receiver has achieved FAS lock for lane 4 of the PMA service interface. When read as a zero, bit 1.2246.4 indicates that the SC-FEC receiver has not achieved FAS lock for lane 4 of the PMA service interface. This bit reflects the state of fas_lock<4> (see 153.2.4.1.1).

45.2.1.223.6 SC-FEC FAS lock 3 (1.2246.3)

When read as a one, bit 1.2246.3 indicates that the SC-FEC receiver has achieved FAS lock for lane 3 of the PMA service interface. When read as a zero, bit 1.2246.3 indicates that the SC-FEC receiver has not achieved FAS lock for lane 3 of the PMA service interface. This bit reflects the state of fas_lock<3> (see 153.2.4.1.1).

45.2.1.223.7 SC-FEC FAS lock 2 (1.2246.2)

When read as a one, bit 1.2246.2 indicates that the SC-FEC receiver has achieved FAS lock for lane 2 of the PMA service interface. When read as a zero, bit 1.2246.2 indicates that the SC-FEC receiver has not achieved FAS lock for lane 2 of the PMA service interface. This bit reflects the state of fas_lock<2> (see 153.2.4.1.1).

45.2.1.223.8 SC-FEC FAS lock 1 (1.2246.1)

When read as a one, bit 1.2246.1 indicates that the SC-FEC receiver has achieved FAS lock for lane 1 of the PMA service interface. When read as a zero, bit 1.2246.1 indicates that the SC-FEC receiver has not achieved FAS lock for lane 1 of the PMA service interface. This bit reflects the state of fas_lock<1> (see 153.2.4.1.1).

45.2.1.223.9 SC-FEC FAS lock 0 (1.2246.0)

When read as a one, bit 1.2246.0 indicates that the SC-FEC receiver has achieved FAS lock for lane 0 of the PMA service interface. When read as a zero, bit 1.2246.0 indicates that the SC-FEC receiver has not achieved FAS lock for lane 0 of the PMA service interface. This bit reflects the state of fas_lock<0> (see 153.2.4.1.1).

45.2.1.224 SC-FEC alignment status 2 register (Register 1.2247)

The assignment of bits in the SC-FEC alignment status 2 register is shown in Table 45–187.

45.2.1.224.1 SC-FEC FAS lock 19 (1.2247.11)

When read as a one, bit 1.2247.11 indicates that the SC-FEC receiver has achieved FAS lock for lane 19 of the PMA service interface. When read as a zero, bit 1.2247.11 indicates that the SC-FEC receiver has not achieved FAS lock for lane 19 of the PMA service interface. This bit reflects the state of fas_lock<19> (see 153.2.4.1.1).

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Table 45–187—SC-FEC alignment status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2247.15:12	Reserved	Value always 0	RO
1.2247.11	SC-FEC FAS lock 19	1 = Lane 19 is locked 0 = Lane 19 is not locked	RO
1.2247.10	SC-FEC FAS lock 18	1 = Lane 18 is locked 0 = Lane 18 is not locked	RO
1.2247.9	SC-FEC FAS lock 17	1 = Lane 17 is locked 0 = Lane 17 is not locked	RO
1.2247.8	SC-FEC FAS lock 16	1 = Lane 16 is locked 0 = Lane 16 is not locked	RO
1.2247.7	SC-FEC FAS lock 15	1 = Lane 15 is locked 0 = Lane 15 is not locked	RO
1.2247.6	SC-FEC FAS lock 14	1 = Lane 14 is locked 0 = Lane 14 is not locked	RO
1.2247.5	SC-FEC FAS lock 13	1 = Lane 13 is locked 0 = Lane 13 is not locked	RO
1.2247.4	SC-FEC FAS lock 12	1 = Lane 12 is locked 0 = Lane 12 is not locked	RO
1.2247.3	SC-FEC FAS lock 11	1 = Lane 11 is locked 0 = Lane 11 is not locked	RO
1.2247.2	SC-FEC FAS lock 10	1 = Lane 10 is locked 0 = Lane 10 is not locked	RO
1.2247.1	SC-FEC FAS lock 9	1 = Lane 9 is locked 0 = Lane 9 is not locked	RO
1.2247.0	SC-FEC FAS lock 8	1 = Lane 8 is locked 0 = Lane 8 is not locked	RO

[a]RO = Read only

45.2.1.224.2 SC-FEC FAS lock 18 (1.2247.10)

When read as a one, bit 1.2247.10 indicates that the SC-FEC receiver has achieved FAS lock for lane 18 of the PMA service interface. When read as a zero, bit 1.2247.10 indicates that the SC-FEC receiver has not achieved FAS lock for lane 18 of the PMA service interface This bit reflects the state of fas_lock<18> (see 153.2.4.1.1).

45.2.1.224.3 SC-FEC FAS lock 17 (1.2247.9)

When read as a one, bit 1.2247.9 indicates that the SC-FEC receiver has achieved FAS lock for lane 17 of the PMA service interface. When read as a zero, bit 1.2247.9 indicates that the SC-FEC receiver has not achieved FAS lock for lane 17 of the PMA service interface This bit reflects the state of fas_lock<17> (see 153.2.4.1.1).

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45.2.1.224.4 SC-FEC FAS lock 16 (1.2247.8)

When read as a one, bit 1.2247.8 indicates that the SC-FEC receiver has achieved FAS lock for lane 16 of the PMA service interface. When read as a zero, bit 1.2247.8 indicates that the SC-FEC receiver has not achieved FAS lock for lane 16 of the PMA service interface This bit reflects the state of fas_lock<16> (see 153.2.4.1.1).

45.2.1.224.5 SC-FEC FAS lock 15 (1.2247.7)

When read as a one, bit 1.2247.7 indicates that the SC-FEC receiver has achieved FAS lock for lane 15 of the PMA service interface. When read as a zero, bit 1.2247.7 indicates that the SC-FEC receiver has not achieved FAS lock for lane 15 of the PMA service interface This bit reflects the state of fas_lock<15> (see 153.2.4.1.1).

45.2.1.224.6 SC-FEC FAS lock 14 (1.2247.6)

When read as a one, bit 1.2247.6 indicates that the SC-FEC receiver has achieved FAS lock for lane 14 of the PMA service interface. When read as a zero, bit 1.2247.6 indicates that the SC-FEC receiver has not achieved FAS lock for lane 14 of the PMA service interface This bit reflects the state of fas_lock<14> (see 153.2.4.1.1).

45.2.1.224.7 SC-FEC FAS lock 13 (1.2247.5)

When read as a one, bit 1.2247.5 indicates that the SC-FEC receiver has achieved FAS lock for lane 13 of the PMA service interface. When read as a zero, bit 1.2247.5 indicates that the SC-FEC receiver has not achieved FAS lock for lane 13 of the PMA service interface This bit reflects the state of fas_lock<13> (see 153.2.4.1.1).

45.2.1.224.8 SC-FEC FAS lock 12 (1.2247.4)

When read as a one, bit 1.2247.4 indicates that the SC-FEC receiver has achieved FAS lock for lane 12 of the PMA service interface. When read as a zero, bit 1.2247.4 indicates that the SC-FEC receiver has not achieved FAS lock for lane 12 of the PMA service interface This bit reflects the state of fas_lock<12> (see 153.2.4.1.1).

45.2.1.224.9 SC-FEC FAS lock 11 (1.2247.3)

When read as a one, bit 1.2247.3 indicates that the SC-FEC receiver has achieved FAS lock for lane 11 of the PMA service interface. When read as a zero, bit 1.2247.3 indicates that the SC-FEC receiver has not achieved FAS lock for lane 11 of the PMA service interface This bit reflects the state of fas_lock<11> (see 153.2.4.1.1).

45.2.1.224.10 SC-FEC FAS lock 10 (1.2247.2)

When read as a one, bit 1.2247.2 indicates that the SC-FEC receiver has achieved FAS lock for lane 10 of the PMA service interface. When read as a zero, bit 1.2247.2 indicates that the SC-FEC receiver has not achieved FAS lock for lane 10 of the PMA service interface This bit reflects the state of fas_lock<10> (see 153.2.4.1.1).

45.2.1.224.11 SC-FEC FAS lock 9 (1.2247.1)

When read as a one, bit 1.2247.1 indicates that the SC-FEC receiver has achieved FAS lock for lane 9 of the PMA service interface. When read as a zero, bit 1.2247.1 indicates that the SC-FEC receiver has not

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achieved FAS lock for lane 9 of the PMA service interface This bit reflects the state of fas_lock<9> (see 153.2.4.1.1).

45.2.1.224.12 SC-FEC FAS lock 8 (1.2247.0)

When read as a one, bit 1.2247.0 indicates that the SC-FEC receiver has achieved FAS lock for lane 8 of the PMA service interface. When read as a zero, bit 1.2247.0 indicates that the SC-FEC receiver has not achieved FAS lock for lane 8 of the PMA service interface This bit reflects the state of fas_lock<8> (see 153.2.4.1.1).

45.2.1.225 SC-FEC lane mapping, lane 0 register (Register 1.2250)

The assignment of bits in the SC-FEC lane mapping, lane 0 register is shown in Table 45–188. When the SC-FEC described in Clause 153 detects and locks the FAS on PMA service interface lane 0, the detected SC-FEC lane number is recorded in this register. The contents of the SC-FEC lane mapping, lane 0 register is valid when the SC-FEC FAS lock 0 bit (1.2246.0) is set to one and is invalid otherwise (see 45.2.1.223.9).

Table 45–188—SC-FEC lane mapping, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2250.15:5	Reserved	Value always 0	RO
1.2250.4:0	Lane 0 mapping	SC-FEC lane received on PMA service interface lane 0	RO

[a]RO = Read only

45.2.1.226 SC-FEC lane mapping, lane 1 through 19 registers (Registers 1.2251 through 1.2269)

The definition of the SC-FEC lane mapping, lane 1 through 19 registers is equivalent to that described for lane 0 in 45.2.1.225. The lane mapping for lane 1 is in register 1.2251; lane 2 is in register 1.2252; etc.

45.2.1.227 SC-FEC corrected codewords counter (Register 1.2276, 1.2277)

The assignment of bits in the SC-FEC corrected codewords counter is shown in Table 45–189. See 153.2.5.1 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.2276 and 1.2277 are used to read the value of a 32-bit counter. When registers 1.2276 and 1.2277 are used to read the 32-bit counter value, register 1.2276 is read first, the value of the register 1.2277 is latched when (and only when) register 1.2276 is read, and reads of register 1.2277 return the latched value rather than the current value of the counter.

Table 45–189—SC-FEC corrected codewords counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.2276.15:0	FEC corrected codewords lower	FEC_corrected_cw_counter[15:0]	RO, NR
1.2277.15:0	FEC corrected codewords upper	FEC_corrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

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45.2.1.228 SC-FEC uncorrected codewords counter (Register 1.2278, 1.2279)

The assignment of bits in the SC-FEC uncorrected codewords counter is shown in Table 45–190. See 153.2.5.2 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.2278 and 1.2279 are used to read the value of a 32-bit counter. When registers 1.2278 and 1.2279 are used to read the 32-bit counter value, register 1.2278 is read first, the value of the register 1.2279 is latched when (and only when) register 1.2278 is read, and reads of register 1.2279 return the latched value rather than the current value of the counter.

Table 45–190—SC-FEC uncorrected codewords counter bit definitions

Bit(s)	Name	Description	R/W[a]
1.2278.15:0	FEC uncorrected codewords lower	FEC_uncorrected_cw_counter[15:0]	RO, NR
1.2279.15:0	FEC uncorrected codewords upper	FEC_uncorrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.229 SC-FEC total bits register (Register 1.2280, 1.2281, 1.2282, 1.2283)

The assignment of bits in the SC-FEC total bits register is shown in Table 45–191. See 153.2.5.3 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.2280, 1.2281, 1.2282, and 1.2283 are used to read the value of a 64-bit counter. When registers 1.2280, 1.2281, 1.2282, and 1.2283 are used to read the 64-bit counter value, register 1.2280 is read first, the values of registers 1.2281, 1.2282, and 1.2283 are latched when (and only when) register 1.2280 is read, and reads of registers 1.2281, 1.2282, and 1.2283 return the latched value rather than the current value of the counter.

Table 45–191—SC-FEC total bits register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2280.15:0	FEC total bits lowest	FEC_total_bits[15:0]	RO, NR
1.2281.15:0	FEC total bits	FEC_total_bits[31:16]	RO, NR
1.2282.15:0	FEC total bits	FEC_total_bits[47:32]	RO, NR
1.2283.15:0	FEC total bits highest	FEC_total_bits[64:48]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.230 SC-FEC corrected bits register (Register 1.2284, 1.2285, 1.2286, 1.2287)

The assignment of bits in the SC-FEC corrected bits register is shown in Table 45–192. See 153.2.5.4 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.2284, 1.2285, 1.2286, and 1.2287 are used to read the value of a 64-bit counter. When registers 1.2284, 1.2285, 1.2286, and 1.2287 are used to read the 64-bit counter value, register 1.2284 is read first, the values of

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registers 1.2285, 1.2286, and 1.2287 are latched when (and only when) register 1.2284 is read, and reads of registers 1.2285, 1.2286, and 1.2287 return the latched value rather than the current value of the counter.

Table 45–192—SC-FEC corrected bits register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2284.15:0	FEC corrected bits lowest	FEC_corrected_bits[15:0]	RO, NR
1.2285.15:0	FEC corrected bits	FEC_corrected_bits[31:16]	RO, NR
1.2286.15:0	FEC corrected bits	FEC_corrected_bits[47:32]	RO, NR
1.2287.15:0	FEC corrected bits highest	FEC_corrected_bits[64:48]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.1.231 10BASE-T1L PMA control register (Register 1.2294)

The assignment of bits in the 10BASE-T1L PMA control register is shown in Table 45–193.

Table 45–193—10BASE-T1L PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2294.15	PMA reset	1 = PMA reset 0 = Normal operation	R/W, SC
1.2294.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2294.13	Reserved	Value always zero	RO
1.2294.12	Transmit voltage amplitude control	1 = Enable 2.4 Vpp operating mode 0 = Enable 1.0 Vpp operating mode	R/W
1.2294.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2294.10	EEE enable	1 = Enable EEE mode 0 = Disable EEE mode	R/W
1.2294.9:1	Reserved	Value always 0	RO
1.2294.0	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.1.231.1 PMA reset (1.2294.15)

Resetting the 10BASE-T1L PMA is accomplished by setting bit 1.2294.15 to one. This action shall set all 10BASE-T1L PMA registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1L PMA and the state of the physical link. This action may also initiate a reset in any

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other MMDs that are instantiated in the same package. This bit is self-clearing, and the 10BASE-T1L PMA shall return a value of one in bit 1.2294.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1L PMA is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2294.15.

During a reset, the 10BASE-T1L PMA shall respond to reads from bits 1.2294.15, 1.8.15:14, and 1.0.15. Reads for all other bits are indeterminate, and the values are invalid.

NOTE—This operation may interrupt data communication.

Bit 1.2294.15 is a copy of bit 1.0.15, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1L PMA.

45.2.1.231.2 Transmit disable (1.2294.14)

When bit 1.2294.14 is set to one, the PMA shall disable output on the transmit path. When bit 1.2294.14 is set to zero, the PMA shall enable output on the transmit path.

Bit 1.2294.14 is a copy of bit 1.9.0, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.231.3 Transmit voltage amplitude control (1.2294.12)

Bit 1.2294.12 is used to set the 2.4 Vpp operating mode when Auto-Negotiation enable bit 7.512.12 is set to zero or if Auto-Negotiation is not implemented. If bit 1.2294.12 is set to one, the PHY shall operate in 2.4 Vpp operating mode according to 146.5.4.1. If bit 1.2294.12 is set to zero, the PHY shall operate in 1.0 Vpp operating mode according to 146.5.4.1. The default value of bit 1.2294.12 is zero. This bit shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

45.2.1.231.4 Low-power (1.2294.11)

When the low-power ability is supported, the 10BASE-T1L PMA may be placed into a low-power mode by setting bit 1.2294.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the 10BASE-T1L PMA. The behavior of the 10BASE-T1L PMA in transition to and from the low-power mode is implementation specific, and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2294.11 is zero.

NOTE—This operation may interrupt data communication. The data path of the 10BASE-T1L PMA, depending on implementation, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

Bit 1.2294.11 is a copy of bit 1.0.11, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the 10BASE-T1L PMA in low-power mode.

45.2.1.231.5 EEE enable (1.2294.10)

Bit 1.2294.10 is used to enable EEE functionality when Auto-Negotiation enable bit 7.512.12 is set to zero or if Auto-Negotiation is not implemented. If bit 1.2294.10 is set to one, the PHY shall operate with EEE enabled. If bit 1.2294.10 is set to zero, the PHY shall operate with EEE disabled. This bit shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one. The default value of bit 1.2294.10 is zero.

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45.2.1.231.6 Loopback (1.2294.0)

The 10BASE-T1L PMA shall be placed in near-end loopback mode of operation when bit 1.2294.0 is set to one. When in loopback mode, the 10BASE-T1L PMA shall accept data on the transmit path and return it on the receive path. The default value of bit 1.2294.0 is zero. Bit 1.2294.0 is a copy of 1.0.0, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.1.232 10BASE-T1L PMA status register (Register 1.2295)

The assignment of bits in the 10BASE-T1L PMA status register is shown in Table 45–194.

Table 45–194—10BASE-T1L PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2295.15:14	Reserved	Value always 0	RO
1.2295.13	Loopback ability	1 = PHY has loopback ability 0 = PHY has no loopback ability	RO
1.2295.12	2.4 Vpp operating mode ability	1 = PHY has 2.4 Vpp operating mode ability 0 = PHY does not have 2.4 Vpp operating mode ability	RO
1.2295.11	Low-power ability	1 = PMA has low-power ability 0 = PMA does not have low-power ability	RO
1.2295.10	EEE ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2295.9	Receive fault ability	1 = PMA has the ability to detect a fault condition on the receive path 0 = PMA does not have the ability to detect a fault condition on the receive path	RO
1.2295.8:3	Reserved	Value always 0	RO
1.2295.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2295.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH
1.2295.0	Receive link status	1 = PMA receive link up 0 = PMA receive link down	RO/LL

[a]RO = Read only, LL = Latching low, LH = Latching high

45.2.1.232.1 Loopback ability (1.2295.13)

When read as a one, this bit indicates that the 10BASE-T1L PHY supports PMA loopback. When read as a zero, this bit indicates that the 10BASE-T1L PHY does not support PMA loopback.

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45.2.1.232.2 2.4 Vpp operating mode ability (1.2295.12)

When read as a one, this bit indicates that the 10BASE-T1L PHY supports a transmit level of 2.4 Vpp. When read as a zero, this bit indicates that the 10BASE-T1L PHY does not support a transmit level of 2.4 Vpp.

45.2.1.232.3 Low-power ability (1.2295.11)

When read as a one, bit 1.2295.11 indicates that the 10BASE-T1L PMA supports the low-power ability. When read as a zero, bit 1.2295.11 indicates that the 10BASE-T1L PMA does not support the low-power ability. If the 10BASE-T1L PMA supports the low-power ability, then it is controlled using either bit 1.2294.11 or bit 1.0.11.

45.2.1.232.4 EEE ability (1.2295.10)

When read as a one, this bit indicates that the 10BASE-T1L PHY supports EEE. When read as a zero, this bit indicates that the 10BASE-T1L PHY does not support EEE.

45.2.1.232.5 Receive fault ability (1.2295.9)

When read as a one, bit 1.2295.9 indicates that the 10BASE-T1L PMA has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2295.9 indicates that the 10BASE-T1L PMA does not have the ability to detect a fault condition on the receive path.

45.2.1.232.6 Receive polarity (1.2295.2)

When read as a zero, bit 1.2295.2 indicates that the polarity of the receiver is not reversed. When read as a one, bit 1.2295.2 indicates that the polarity of the receiver is reversed.

45.2.1.232.7 Receive fault (1.2295.1)

When read as a one, bit 1.2295.1 indicates that the 10BASE-T1L PMA has detected a fault condition on the receive path. When read as a zero, bit 1.2295.1 indicates that the 10BASE-T1L PMA has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional, and the ability to detect such a condition is advertised by bit 1.2295.9. The 10BASE-T1L PMA that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The receive fault bit shall be implemented with latching high behavior.

45.2.1.232.8 Receive link status (1.2295.0)

When read as a one, bit 1.2295.0 indicates that the 10BASE-T1L PMA receive link is up. When read as a zero, bit 1.2295.0 indicates that the 10BASE-T1L PMA receive link has been down one or more times since the register was last read. The receive link status bit shall be implemented with latching low behavior.

45.2.1.233 10BASE-T1L test mode control register (Register 1.2296)

The assignment of bits in the 10BASE-T1L test mode control register is shown in Table 45–195. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

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Table 45–195—10BASE-T1L test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2296.15:13	Test mode control	15 14 13 1 x x = Reserved 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2296.12:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

45.2.1.233.1 Test mode control (1.2296.15:13)

Transmitter test mode operations defined by bits 1.2296.15:13 are described in 146.5.2. The default value for bits 1.2296.15:13 is zero.

45.2.1.234 10BASE-T1S PMA control register (Register 1.2297)

The assignment of bits in the 10BASE-T1S PMA control register is shown in Table 45–196.

Table 45–196—10BASE-T1S PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2297.15	PMA reset	1 = PMA reset 0 = Normal operation	R/W, SC
1.2297.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2297.13:12	Reserved	Value always 0	RO
1.2297.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2297.10	Multidrop mode	1 = Enable operation over mixing segment network 0 = Disable operation over mixing segment network	R/W
1.2297.9:1	Reserved	Value always 0	RO
1.2297.0	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.1.234.1 PMA reset (1.2297.15)

Resetting the 10BASE-T1S PMA is accomplished by setting bit 1.2297.15 to one. This action shall set all 10BASE-T1S PMA registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1S PMA and the state of the physical link. This action may also initiate a reset in any

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other MMDs that are instantiated in the same package. This bit is self-clearing, and the 10BASE-T1S PMA shall return a value of one in bit 1.2297.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1S PMA is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2297.15.

During a reset, the 10BASE-T1S PMA shall respond to reads from bits 1.2297.15, 1.8.15:14, and 1.0.15. All other register bits should be ignored.

NOTE—This operation may interrupt communication.

Bit 1.2297.15 is a copy of 1.0.15, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1S PMA.

45.2.1.234.2 Transmit disable (1.2297.14)

When bit 1.2297.14 is set to one, the PMA shall disable output on the transmit path. When bit 1.2297.14 is set to zero, the PMA shall enable output on the transmit path.

Bit 1.2297.14 is a copy of bit 1.9.0, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.234.3 Low-power (1.2297.11)

When the low-power ability is supported, the 10BASE-T1S PMA may be placed into a low-power mode by setting bit 1.2297.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the 10BASE-T1S PMA. The behavior of the 10BASE-T1S PMA in transition to and from the low-power mode is implementation specific, and any interface signals should not be relied upon. While in the low-power mode, the device shall respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2297.11 is zero.

NOTE—The time from low-power mode to full operation is implementation specific.

Bit 1.2297.11 is a copy of bit 1.0.11, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the 10BASE-T1S PMA in low-power mode.

45.2.1.234.4 Multidrop mode (1.2297.10)

When Auto-Negotiation is implemented and enabled, writing to this bit shall have no effect on the PHY, and the PCS multidrop variable shall be set to FALSE. If multidrop mode is not supported according to bit 1.2298.10, then writing to bit 1.2297.10 shall have no effect, and the multidrop variable shall be set to FALSE. Otherwise, if bit 1.2297.10 is set to one, the 10BASE-T1S PMA shall operate in multidrop mode, and the multidrop variable is set to TRUE; and if bit 1.2297.10 is set to zero, the multidrop variable is set to FALSE. If multidrop mode is supported according to bit 1.2298.10, then the default value of bit 1.2297.10 should be one.

45.2.1.234.5 Loopback (1.2297.0)

The 10BASE-T1S PMA shall be placed in loopback mode of operation when loopback bit 1.2297.0 is set to one. When in loopback mode, the 10BASE-T1S PMA shall accept data on the transmit path and return it on the receive path. The default value of bit 1.2297.0 is zero. Bit 1.2297.0 is a copy of 1.0.0, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

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45.2.1.235 10BASE-T1S PMA status register (Register 1.2298)

The assignment of bits in the 10BASE-T1S PMA status register is shown in Table 45–197.

Table 45–197—10BASE-T1S PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2298.15:14	Reserved	Value always 0	RO
1.2298.13	Loopback ability	1 = PHY has loopback ability 0 = PHY has no loopback ability	RO
1.2298.12	Reserved	Value always 0	RO
1.2298.11	Low-power ability	1 = PMA has low-power ability 0 = PMA does not have low-power ability	RO
1.2298.10	Multidrop mode ability	1 = PMA has the ability to operate over a mixing segment network 0 = PMA does not have the ability to operate over a mixing segment network	RO
1.2298.9	Receive fault ability	1 = PMA has the ability to detect a fault condition on the receive path 0 = PMA does not have the ability to detect a fault condition on the receive path	RO
1.2298.8:2	Reserved	Value always 0	RO
1.2298.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH
1.2298.0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

45.2.1.235.1 10BASE-T1S loopback ability (1.2298.13)

When read as a one, this bit indicates that the 10BASE-T1S PHY supports PMA loopback. When read as a zero, this bit indicates that the 10BASE-T1S PHY does not support PMA loopback.

45.2.1.235.2 Low-power ability (1.2298.11)

When read as a one, bit 1.2298.11 indicates that the 10BASE-T1S PMA supports the low-power ability. When read as a zero, bit 1.2298.11 indicates that the 10BASE-T1S PMA does not support the low-power feature. If the 10BASE-T1S PMA supports the low-power feature, then it is controlled using either bit 1.2297.11 or bit 1.0.11.

45.2.1.235.3 Multidrop ability (1.2298.10)

When read as a one, bit 1.2298.10 indicates that the 10BASE-T1S PMA supports multidrop mode (see Clause 147). When read as a zero, bit 1.2298.10 indicates that the 10BASE-T1S PMA does not support multidrop mode. If the 10BASE-T1S PMA supports multidrop mode, then it is controlled using bit 1.2297.10; otherwise, bit 1.2297.10 has no effect.

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45.2.1.235.4 Receive fault ability (1.2298.9)

When read as a one, bit 1.2298.9 indicates that the 10BASE-T1S PMA has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2298.9 indicates that the 10BASE-T1S PMA does not have the ability to detect a fault condition on the receive path.

45.2.1.235.5 Receive fault (1.2298.1)

When read as a one, bit 1.2298.1 indicates that the 10BASE-T1S PMA has detected a fault condition on the receive path. When read as a zero, bit 1.2298.1 indicates that the 10BASE-T1S PMA has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional, and the ability to detect such a condition is advertised by bit 1.2298.9. The 10BASE-T1S PMA that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. This bit shall be implemented with latching high behavior.

45.2.1.236 10BASE-T1S test mode control register (Register 1.2299)

The assignment of bits in the 10BASE-T1S test mode control register is shown in Table 45–198. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–198—10BASE-T1S test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2299.15:13	Test mode control	15 14 13 1 1 x = Reserved 1 0 1 = Reserved 1 0 0 = Test mode 4 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2299.12:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

45.2.1.236.1 Test mode control (1.2299.15:13)

Transmitter test mode operations defined by bits 1.2299.15:13 are described in 147.5.2. The default value for bits 1.2299.15:13 is zero.

45.2.1.237 1000BASE-T1 PMA control register (Register 1.2304)

The assignment of bits in the 1000BASE-T1 PMA control register is shown in Table 45–199.

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Table 45–199—1000BASE-T1 PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2304.15	PMA/PMD reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2304.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2304.13:12	Reserved	Value always 0	RO
1.2304.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2304.10:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.1.237.1 PMA/PMD reset (1.2304.15)

Resetting the 1000BASE-T1 PMA/PMD is accomplished by setting bit 1.2304.15 to a one. This action shall set all 1000BASE-T1 PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the 1000BASE-T1 PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 1000BASE-T1 PMA/PMD shall return a value of one in bit 1.2304.15 when a reset is in progress; otherwise, it shall return a value of zero. The 1000BASE-T1 PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface is restored to operation as defined in 97.4.2.1, starting when bit 1.2304.15 is set.

During a reset, the 1000BASE-T1 PMD/PMA shall respond to reads from register bits 1.2304.15, 1.8.15:14, and 1.0.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 1.2304.15 is a copy of 1.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 1000BASE-T1 PMA/PMD.

45.2.1.237.2 Transmit disable (1.2304.14)

When bit 1.2304.14 is set to a one, the PMA shall disable output on the transmit path. When bit 1.2304.14 is set to a zero, the PMA shall enable output on the transmit path.

Bit 1.2304.14 is a copy of 1.9.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.237.3 Low power (1.2304.11)

When the low-power ability is supported, the 1000BASE-T1 PMA/PMD may be placed into a low-power mode by setting bit 1.2304.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the 1000BASE-T1 PMA/PMD. The behavior of the 1000BASE-T1 PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2304.11 is zero.

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This operation interrupts data communication. The data path of the 1000BASE-T1 PMD, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

Bit 1.2304.11 is a copy of 1.0.11 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the 1000BASE-T1 PMA/PMD in low-power mode.

45.2.1.238 1000BASE-T1 PMA status register (Register 1.2305)

The assignment of bits in the 1000BASE-T1 PMA status register is shown in Table 45–200.

Table 45–200—1000BASE-T1 PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2305.15:12	Reserved	Value always 0	RO
1.2305.11	1000BASE-T1 OAM Ability	1 = PHY has 1000BASE-T1 OAM ability 0 = PHY does not have 1000BASE-T1 OAM ability	RO
1.2305.10	EEE Ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2305.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2305.8	Low-power ability	1 = PMA/PMD has low-power ability 0 = PMA/PMD does not have low-power ability	RO
1.2305.7:3	Reserved	Value always 0	RO
1.2305.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2305.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.2305.0	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

[a]RO = Read only, LL = Latching Low

45.2.1.238.1 1000BASE-T1 OAM ability (1.2305.11)

When read as a one, this bit indicates that the 1000BASE-T1 PHY supports 1000BASE-T1 OAM (see 97.3.8). When read as a zero, this bit indicates that the 1000BASE-T1 PHY does not support 1000BASE-T1 OAM.

45.2.1.238.2 EEE ability (1.2305.10)

When read as a one, this bit indicates that the 1000BASE-T1 PHY supports EEE. When read as a zero, this bit indicates that the 1000BASE-T1 PHY does not support EEE.

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45.2.1.238.3 Receive fault ability (1.2305.9)

When read as a one, bit 1.2305.9 indicates that the 1000BASE-T1 PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2305.9 indicates that the 1000BASE-T1 PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.238.4 Low-power ability (1.2305.8)

When read as a one, bit 1.2305.8 indicates that the 1000BASE-T1 PMA/PMD supports the low-power feature. When read as a zero, bit 1.2305.8 indicates that the 1000BASE-T1 PMA/PMD does not support the low-power feature. If the 1000BASE-T1 PMA/PMD supports the low-power feature, then it is controlled using either bit 1.2304.11 or bit 1.0.11.

45.2.1.238.5 Receive polarity (1.2305.2)

When read as zero, bit 1.2305.2 indicates that the polarity of the receiver is not reversed. When read as one, bit 1.2305.2 indicates that the polarity of receiver is reversed.

45.2.1.238.6 Receive fault (1.2305.1)

When read as a one, bit 1.2305.1 indicates that the 1000BASE-T1 PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2305.1 indicates that the 1000BASE-T1 PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2305.9. The 1000BASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit.

45.2.1.238.7 Receive link status (1.2305.0)

When read as a one, bit 1.2305.0 indicates that the 1000BASE-T1 PMA/PMD receive link is up. When read as a zero, bit 1.2305.0 indicates that the 1000BASE-T1 PMA/PMD receive link has been down one or more times since the register was last read. The receive link status bit shall be implemented with latching low behavior.

45.2.1.239 1000BASE-T1 training register (Register 1.2306)

The assignment of bits in the 1000BASE-T1 training register is shown in Table 45–201.

Table 45–201—1000BASE-T1 training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2306.15:11	Reserved	Value always 0	RO
1.2306.10:4	User field	7-bit user defined field to send to the link partner	R/W
1.2306.3:2	Reserved	Value always 0	RO
1.2306.1	1000BASE-T1 OAM advertisement	1 = 1000BASE-T1 OAM ability advertised to link partner 0 = 1000BASE-T1 OAM ability not advertised to link partner	R/W
1.2306.0	EEE advertisement	1 = EEE ability advertised to link partner 0 = EEE ability not advertised to link partner	R/W

[a]RO = Read only, R/W = Read/Write

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45.2.1.239.1 User field (1.2306.10:4)

This register is a user defined 7-bit field that is transmitted to the link partner during training.

45.2.1.239.2 1000BASE-T1 OAM advertisement (1.2306.1)

When set as a one, this bit indicates to the link partner that the 1000BASE-T1 PHY is advertising 1000BASE-T1 OAM capability. When set as a zero, this bit indicates to the link partner that the 1000BASE-T1 PHY is not advertising 1000BASE-T1 OAM capability. This bit shall be set to zero if the 1000BASE-T1 PHY does not support 1000BASE-T1 OAM.

45.2.1.239.3 EEE advertisement (1.2306.0)

When set as a one, this bit indicates to the link partner that the 1000BASE-T1 PHY is advertising EEE capability. When set as a zero, this bit indicates to the link partner that the 1000BASE-T1 PHY is not advertising EEE capability. This bit shall be set to zero if the 1000BASE-T1 PHY does not support EEE.

45.2.1.240 1000BASE-T1 link partner training register (Register 1.2307)

The assignment of bits in the 1000BASE-T1 link partner training register is shown in Table 45–202. The values in this register are not valid until link is up.

Table 45–202—1000BASE-T1 link partner training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2307.15:11	Reserved	Value always 0	RO
1.2307.10:4	Link partner user field	7-bit user defined field received from the link partner	RO
1.2307.3:2	Reserved	Value always 0	RO
1.2307.1	Link partner 1000BASE-T1 OAM advertisement	1 = Link partner has 1000BASE-T1 OAM ability 0 = Link partner does not have 1000BASE-T1 OAM ability	RO
1.2307.0	Link partner EEE advertisement	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability	RO

[a]RO = Read only

45.2.1.240.1 Link partner user field (1.2307.10:4)

This register is a user defined 7-bit field that is received from the link partner during training.

45.2.1.240.2 Link partner 1000BASE-T1 OAM advertisement (1.2307.1)

When read as a one, this bit indicates the link partner is advertising 1000BASE-T1 OAM capability. When read as a zero, this bit indicates the link partner is not advertising 1000BASE-T1 OAM capability. 1000BASE-T1 OAM capability shall be enabled only when both the local device and its link partner are advertising 1000BASE-T1 OAM capability.

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45.2.1.240.3 Link partner EEE advertisement (1.2307.0)

When read as a one, this bit indicates the link partner is advertising EEE capability. When read as a zero, this bit indicates the link partner is not advertising EEE capability. EEE capability shall be enabled only when both the local device and its link partner are advertising EEE capability.

45.2.1.241 1000BASE-T1 test mode control register (Register 1.2308)

The assignment of bits in the 1000BASE-T1 test mode control register is shown in Table 45–203. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–203—1000BASE-T1 test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2308.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Reserved 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2308.12:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.1.241.1 Test mode control (1.2308.15:13)

Transmitter test mode operations defined by bits 1.2308.15:13, are described in 97.5.2 and Table 97–12. The default value for bits 1.2308.15:13 is zero.

45.2.1.242 MultiGBASE-T1 PMA control register (Register 1.2309)

The assignment of bits in the MultiGBASE-T1 PMA control register is shown in Table 45–204.

Table 45–204—MultiGBASE-T1 PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2309.15	PMA/PMD reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2309.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2309.13:12	Reserved	Value always 0	RO

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Table 45–204—MultiGBASE-T1 PMA control register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.2309.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2309.10:0	Reserved	Value always 0	RO

[a]R/W = Read/Write, RO = Read only, SC = Self-clearing

45.2.1.242.1 PMA/PMD reset (1.2309.15)

Resetting the MultiGBASE-T1 PMA/PMD is accomplished by setting bit 1.2309.15 to a one. This action shall set all PMA/PMD registers to their default states. As a consequence, this action may change the internal state of a MultiGBASE-T1 PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. Bit 1.2309.15 is self-clearing, and the MultiGBASE-T1 PMA/PMD shall return a value of one in bit 1.2309.15 when a reset is in progress; otherwise, it shall return a value of zero. The MultiGBASE-T1 PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface is restored to operation as defined in 149.4.2.1, starting when bit 1.2309.15 is set.

During a reset, the MultiGBASE-T1 PMA/PMD shall respond to reads from register bits 1.2309.15, 1.8.15:14, and 1.0.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 1.2309.15 is a copy of bit 1.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the MultiGBASE-T1 PMA/PMD.

45.2.1.242.2 Transmit disable (1.2309.14)

When bit 1.2309.14 is set to a one, the PMA shall disable output on the transmit path. When bit 1.2309.14 is set to a zero, the PMA shall enable output on the transmit path.

Bit 1.2309.14 is a copy of bit 1.9.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.242.3 Low power (1.2309.11)

When the low-power ability is supported, the MultiGBASE-T1 PMA/PMD may be placed into a low-power mode by setting bit 1.2309.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the MultiGBASE-T1 PMA/PMD. The behavior of the MultiGBASE-T1 PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, at a minimum, respond to management transactions necessary to exit the low-power mode.

The default value of bit 1.2309.11 is zero.

This operation interrupts data communication.

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Bit 1.2309.11 is a copy of bit 1.0.11 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the MultiGBASE-T1 PMA/PMD in low-power mode.

45.2.1.243 MultiGBASE-T1 PMA status register (1.2310)

The assignment of bits in the MultiGBASE-T1 PMA status register is shown in Table 45–205.

Table 45–205—MultiGBASE-T1 PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2310.15:12	Reserved	Value always 0	RO
1.2310.11	MultiGBASE-T1 OAM ability	1 = PHY has MultiGBASE-T1 OAM ability 0 = PHY does not have MultiGBASE-T1 OAM ability	RO
1.2310.10	EEE ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2310.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2310.8	Low-power ability	1 = PMA/PMD has low-power ability 0 = PMA/PMD does not have low-power ability	RO
1.2310.7:5	Reserved	Value always 0	RO
1.2310.4:3	PrecodeSel	4 3 0 0 = no precoder requested 0 1 = 1–D precoder requested 1 0 = 1+D precoder requested 1 1 = $1–D^2$ precoder requested	RO
1.2310.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2310.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH
1.2310.0	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

[a]RO = Read only, LH = Latching High, LL = Latching Low

45.2.1.243.1 MultiGBASE-T1 OAM ability (1.2310.11)

When read as a one, bit 1.2310.11 indicates that the MultiGBASE-T1 PHY supports MultiGBASE-T1 OAM (see 149.3.9). When read as a zero, bit 1.2310.11 indicates that the MultiGBASE-T1 PHY does not support MultiGBASE-T1 OAM.

45.2.1.243.2 EEE ability (1.2310.10)

When read as a one, bit 1.2310.10 indicates that the MultiGBASE-T1 PHY supports EEE. When read as a zero, bit 1.2310.10 indicates that the MultiGBASE-T1 PHY does not support EEE.

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45.2.1.243.3 Receive fault ability (1.2310.9)

When read as a one, bit 1.2310.9 indicates that the MultiGBASE-T1 PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2310.9 indicates that the MultiGBASE-T1 PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.243.4 Low-power ability (1.2310.8)

When read as a one, bit 1.2310.8 indicates that the MultiGBASE-T1 PMA/PMD supports the low-power feature. When read as a zero, bit 1.2310.8 indicates that the MultiGBASE-T1 PMA/PMD does not support the low-power feature. If the MultiGBASE-T1 PMA/PMD supports the low-power feature, then it is controlled using either bit 1.2309.11 or bit 1.0.11.

45.2.1.243.5 PrecodeSel (1.2310.4:3)

Bits 1.2310.4:3 contain the requested precoder setting communicated by the PHY to the link partner via the PrecodeSel bits in the Infofield (see 149.4.2.4.5).

45.2.1.243.6 Receive polarity (1.2310.2)

When read as zero, bit 1.2310.2 indicates that the polarity of the receiver is not reversed. When read as one, bit 1.2310.2 indicates that the polarity of the receiver is reversed.

45.2.1.243.7 Receive fault (1.2310.1)

When read as a one, bit 1.2310.1 indicates that the MultiGBASE-T1 PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2310.1 indicates that the MultiGBASE-T1 PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2310.9. A MultiGBASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for bit 1.2310.1. The receive fault bit shall be implemented with latching high behavior.

45.2.1.243.8 Receive link status (1.2310.0)

When read as a one, bit 1.2310.0 indicates that the MultiGBASE-T1 PMA/PMD receive link is up. When read as a zero, bit 1.2310.0 indicates that the MultiGBASE-T1 PMA/PMD receive link has been down one or more times since the register was last read. The receive link status bit shall be implemented with latching low behavior.

45.2.1.244 MultiGBASE-T1 training register (1.2311)

The assignment of bits in the MultiGBASE-T1 training register is shown in Table 45–206.

45.2.1.244.1 Interleave request (1.2311.12:11)

Bits 1.2311.12:11 control the Reed-Solomon interleave setting of this PHY. Reed-Solomon interleaving is described in 149.3.2.2.15. This is communicated to the link partner via Infofields as specified in 149.4.2.4.5.

The values of L = 2 and L = 4 are not defined for 2.5GBASE-T1 PHYs, and the value of L = 4 is not defined for 5GBASE-T1 PHYs. If bits 1.2311.12:11 are set to these undefined values, the PHY will communicate these values to the link partner, but the requested interleaver depth is out of scope of this standard and may not be supported by the link partner.

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Table 45–206—MultiGBASE-T1 training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2311.15:13	Reserved	Value always 0	RO
1.2311.12:11	Interleave request	12 11 0 0: L=1, no interleaving, default for 2.5GBASE-T1 0 1: L=2, RS-FEC interleaving factor two, default for 5GBASE-T1, undefined for 2.5GBASE-T1 1 0: L=4, RS-FEC interleaving factor four, default for 10GBASE-T1, undefined for 2.5GBASE-T1 and 5GBASE-T1 1 1: Reserved	R/W
1.2311.10:6	Reserved	Value always 0	RO
1.2311.5	Precoder selection	Controls requested precoder setting 0 = PHY 1 = User	R/W
1.2311.4	Slow Wake request	1 = Alert window start is only immediate frame after refresh 0 = Alert window start is every 8th RS frame after refresh	R/W
1.2311.3:2	User precoder selection	3 2 0 0 = no precoder requested 0 1 = 1–D precoder requested 1 0 = 1+D precoder requested 1 1 = $1–D^2$ precoder requested	R/W
1.2311.1	MultiGBASE-T1 OAM advertisement	1 = MultiGBASE-T1 OAM ability advertised to link partner 0 = MultiGBASE-T1 OAM ability not advertised to link partner	R/W
1.2311.0	EEE advertisement	1 = EEE ability advertised to link partner 0 = EEE ability not advertised to link partner	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.244.2 Precoder selection (1.2311.5)

When bit 1.2311.5 is set to a one, the PHY shall use bits 1.2311.3:2 for the value of PrecodeSel, and when set to a zero the PHY controls the value of PrecodeSel. PrecodeSel is the desired precoder setting communicated to the link partner via the Infofield specified in 149.4.2.4.5.

45.2.1.244.3 Slow Wake request (1.2311.4)

When set as a one, bit 1.2311.4 indicates to the link partner that the local MultiGBASE-T1 PHY may only transmit alert immediately following refresh. When set as a zero, bit 1.2311.4 indicates to the link partner that the local MultiGBASE-T1 PHY may transmit an alert at any eighth RS-FEC frame after a refresh.

45.2.1.244.4 User precoder selection (1.2311.3:2)

When bit 1.2311.5 is a one, bits 1.2311.3:2 are the requested precoder setting communicated by the PHY to the link partner via the PrecodeSel bits in the Infofield (see 149.4.2.4.5).

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45.2.1.244.5 MultiGBASE-T1 OAM advertisement (1.2311.1)

Support for MultiGBASE-T1 OAM capability shall be advertised if bit 1.2311.1 is set to one. Support for MultiGBASE-T1 OAM capability shall not be advertised if bit 1.2311.1 is set to zero. Support for MultGBASE-T1 OAM capability should only be advertised if it is supported by the PHY.

45.2.1.244.6 EEE advertisement (1.2311.0)

Support for EEE capability shall be advertised if bit 1.2311.0 is set to one. Support for EEE capability shall not be advertised if bit 1.2311.0 is set to zero. Support for EEE operation should only be advertised if it is supported by the PHY.

45.2.1.245 MultiGBASE-T1 link partner training register (1.2312)

The assignment of bits in the MultiGBASE-T1 link partner training register is shown in Table 45–207. The values in this register are not valid when the link is down.

Table 45–207—MultiGBASE-T1 link partner training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2312.15:13	Reserved	Value always 0	RO
1.2312.12:11	Link partner interleave request	12 11 0 0: L=1, no interleaving, default for 2.5GBASE-T1 0 1: L=2, RS-FEC interleaving factor two, default for 5GBASE-T1, undefined for 2.5GBASE-T1 1 0: L=4, RS-FEC interleaving factor four, default for 10GBASE-T1, undefined for 2.5GBASE-T1 and 5GBASE-T1 1 1: Reserved	RO
1.2312.10:5	Reserved	Value always 0	RO
1.2312.4	Link partner Slow Wake requested	1 = Alert window start is only immediate frame after refresh 0 = Alert window start is every 8th RS frame after refresh	RO
1.2312.3:2	Link partner precoder requested	3 2 0 0 = no precoder requested 0 1 = 1–D precoder requested 1 0 = 1+D precoder requested 1 1 = $1–D^2$ precoder requested	RO
1.2312.1	Link partner MultiGBASE-T1 OAM advertisement	1 = Link partner has MultiGBASE-T1 OAM ability 0 = Link partner does not have MultiGBASE-T1 OAM ability	RO
1.2312.0	Link partner EEE advertisement	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability	RO

[a]RO = Read only

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45.2.1.245.1 Link partner interleave request (1.2312.12:11)

Bits 1.2312.12:11 contain the Reed-Solomon interleave setting requested by the link partner. Reed-Solomon interleaving is described in 149.3.2.2.15. This is communicated by the link partner via Infofields as specified in 149.4.2.4.5.

The values of L = 2 and L = 4 are not defined for 2.5GBASE-T1 PHYs, and the value of L = 4 is not defined for 5GBASE-T1 PHYs. Bits 1.2312.12:11 will indicate whatever value is received from the link partner, but if the undefined values are received, the requested interleaver depth is out of scope of this standard and may not be supported by the local PHY.

45.2.1.245.2 Link partner Slow Wake requested (1.2312.4)

Bit 1.2312.4 contains the Slow Wake setting received from the link partner. When set as a one, the link partner may only transmit alert immediately following refresh. When set as a zero, the link partner may only transmit an alert at any eighth RS-FEC frame after a refresh.

45.2.1.245.3 Link partner precoder requested (1.2312.3:2)

Bits 1.2312.3:2 contain the precoder setting requested by the link partner. The precoder requested is encoded as the value of precoder_type defined in 149.3.2.2.20.

45.2.1.245.4 Link partner MultiGBASE-T1 OAM advertisement (1.2312.1)

When read as a one, bit 1.2312.1 indicates the link partner is advertising MultiGBASE-T1 OAM capability. When read as a zero, bit 1.2312.1 indicates the link partner is not advertising MultiGBASE-T1 OAM capability. MultiGBASE-T1 OAM capability shall be enabled only when both the local PHY and its link partner are advertising MultiGBASE-T1 OAM capability.

45.2.1.245.5 Link partner EEE advertisement (1.2312.0)

When read as a one, bit 1.2312.0 indicates the link partner is advertising EEE capability. When read as a zero, bit 1.2312.0 indicates the link partner is not advertising EEE capability. EEE capability shall be enabled only when both the local PHY and its link partner are advertising EEE capability.

45.2.1.246 MultiGBASE-T1 test mode control register (1.2313)

The assignment of bits in the MultiGBASE-T1 test mode control register is shown in Table 45–208. The default values for each bit are chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

45.2.1.246.1 Test mode control (1.2313.15:13)

Transmitter test mode operations defined by bits 1.2313.15:13, are described in 149.5.1 and Table 149–17. The default value for bits 1.2313.15:13 is zero.

45.2.1.246.2 Local transmitter precoder override (1.2313.11)

When bit 1.2313.11 is set to one, the local transmitter's precoder shall be controlled by the value of bits 1.2313.10:9, and the precoder requested by the link partner in PrecodeSel shall be ignored. When bit 1.2313.11 is set to zero, the transmitter shall ignore bits 1.2313.10:9, and the precoder is set according to the value of PrecodeSel received from the link partner as specified in 149.3.2.2.20. The default value of 1.2313.11 is zero.

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Table 45–208—MultiGBASE-T1 test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2313.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2313.12	Reserved	Value always 0	RO
1.2313.11	Local transmitter precoder override	0 = Normal operation 1 = User override	R/W
1.2313.10:9	Local transmit precoder setting	10 9 0 0 = transmit with no precoder 0 1 = transmit with 1–D precoder 1 0 = transmit with 1+D precoder 1 1 = transmit with $1–D^2$ precoder	R/W
1.2313.8:2	Reserved	Value always 0	RO
1.2313.1:0	Jitter test control	1 0 0 0 = Square wave 0 1 = JP03A Pattern 1 0 = JP03B Pattern 1 1 = Reserved	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.246.3 Local transmit precoder setting (1.2313.10:9)

When bit 1.2313.11 is set to one, bits 1.2313.10:9 control the precoder setting of the local transmitter, as defined in 149.3.2.2.20 in the variable precoder_type.

45.2.1.246.4 Jitter test control (1.2313.1:0)

When the transmitter is in test mode 2, bits 1.2313.1:0 control the pattern of the jitter test signal. When the transmitter is not in test mode 2, the setting of bits 1.2313.1:0 has no effect. A value of 00 transmits a square wave from the transmitter, a value of 01 transmits the JP03A pattern, and a value of 10 transmits the JP03B pattern. See 149.5.2.3.1 and 149.5.2.3.2 for more information.

45.2.1.247 MultiGBASE-T1 SNR operating margin register (Register 1.2314)

Register 1.2314 contains the current SNR operating margin measured at the slicer input for the PMAs in the MultiGBASE-T1 set. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x80, 12.7 dB represented by 0xFF, and –12.7 dB represented by 0x01. Implementation of this register is optional.

The assignment of bits in the MultiGBASE-T1 SNR operating margin register is shown in Table 45–209.

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Table 45–209—MultiGBASE-T1 SNR operating margin register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2314.15:8	MultiGBASE-T1 SNR operating margin	Value of current SNR operating margin in dB	RO
1.2314.7:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.1.248 MultiGBASE-T1 minimum SNR margin register (Register 1.2315)

Register 1.2315 contains a latched copy of the lowest value observed in the MultiGBASE-T1 SNR operating margin register (1.2314) since the last read. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x80, 12.7 dB represented by 0xFF, and –12.7 dB represented by 0x01. Implementation of this register is optional.

The assignment of bits in the MultiGBASE-T1 minimum SNR margin register is shown in Table 45–210.

Table 45–210—MultiGBASE-T1 minimum SNR margin register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2315.15:8	MultiGBASE-T1 minimum SNR margin	Value of minimum observed SNR margin in dB	RO
1.2315.7:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.1.249 MultiGBASE-T1 user defined data (Register 1.2316)

The assignment of bits for the MultiGBASE-T1 user defined data register is shown in Table 45–211. The values of the bits in this register are outside the scope of this standard.

Table 45–211—MultiGBASE-T1 user defined data register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2316.15:0	MultiGBASE-T1 user defined data	16 bits of vendor specific data that the PHY sends to its link partner	R/W

[a]R/W = Read/Write

45.2.1.249.1 MultiGBASE-T1 user defined data (1.2316.15:0)

Bits 1.2316.15:0 contain vendor specific data that the PHY may communicate to its link partner during training.

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45.2.1.250 MultiGBASE-T1 link partner user defined data register (Register 1.2317)

The assignment of bits for the MultiGBASE-T1 link partner user defined data register is shown in 45–212. The values of the bits in this register are outside the scope of this standard.

Table 45–212—MultiGBASE-T1 link partner user defined data register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2317.15:0	MultiGBASE-T1 link partner user defined data	16 bits of vendor specific data that the PHY may receive from its link partner	RO

[a]RO = Read only

45.2.1.250.1 MultiGBASE-T1 link partner user defined data register (1.2317.15:0)

Bits 1.2317.15:0 contain vendor specific data that the PHY may receive from its link partner during training.

45.2.2 WIS registers

The assignment of registers in the WIS is shown in Table 45–213. For the WIS octet fields, bit 8 of the corresponding field in the WIS frame maps to the lowest numbered bit of the field in the register.

Table 45–213—WIS registers

Register address	Register name	Subclause
2.0	WIS control 1	45.2.2.1
2.1	WIS status 1	45.2.2.2
2.2, 2.3	WIS device identifier	45.2.2.3
2.4	WIS speed ability	45.2.2.4
2.5, 2.6	WIS devices in package	45.2.2.5
2.7	10G WIS control 2	45.2.2.6
2.8	10G WIS status 2	45.2.2.7
2.9	10G WIS test-pattern error counter	45.2.2.8
2.10 through 2.13	Reserved	
2.14, 2.15	WIS package identifier	45.2.2.9
2.16 through 2.32	Reserved	
2.33	10G WIS status 3	45.2.2.10
2.34 through 2.36	Reserved	

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Table 45–213—WIS registers *(continued)*

Register address	Register name	Subclause
2.37	10G WIS far end path block error count	45.2.2.11
2.38	Reserved	
2.39 through 2.46	10G WIS J1 transmit	45.2.2.12
2.47 through 2.54	10G WIS J1 receive	45.2.2.13
2.55, 2.56	10G WIS far end line BIP errors	45.2.2.14
2.57, 2.58	10G WIS line BIP errors	45.2.2.15
2.59	10G WIS path block error count	45.2.2.16
2.60	10G WIS section BIP error count	45.2.2.17
2.61 through 2.63	Reserved	
2.64 through 2.71	10G WIS J0 transmit	45.2.2.18
2.72 through 2.79	10G WIS J0 receive	45.2.2.19
2.80 through 2.1799	Reserved	
2.1800	TimeSync WIS capability	45.2.2.20
2.1801 through 2.1804	TimeSync WIS transmit path data delay	45.2.2.21
2.1805 through 2.1808	TimeSync WIS receive path data delay	45.2.2.22
2.1809 through 2.32767	Reserved	
2.32 768 through 2.65 535	Vendor specific	

45.2.2.1 WIS control 1 register (Register 2.0)

The assignment of bits in the WIS control 1 register is shown in Table 45–214. The default value for each bit of the WIS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–214—WIS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.0.15	Reset	1 = WIS reset 0 = Normal operation	R/W SC
2.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W

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Table 45–214—WIS control 1 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
2.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
2.0.12	Reserved	Value always 0	RO
2.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
2.0.10:7	Reserved	Value always 0	RO
2.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
2.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
2.0.1:0	Reserved	Value always 0	RO

[a]R/W = Read/Write, SC = Self-clearing, RO = Read only

45.2.2.1.1 Reset (2.0.15)

Resetting a WIS is accomplished by setting bit 2.0.15 to a one. This action shall set all to their default states. As a consequence, this action may change the internal state of the WIS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a WIS shall return a value of one in bit 2.0.15 when a reset is in progress and a value of zero otherwise. A WIS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 2.0.15. During a reset, a WIS shall respond to reads from register bits 2.0.15 and 2.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.2.1.2 Loopback (2.0.14)

The WIS shall be placed in a loopback mode of operation when bit 2.0.14 is set to a one. When bit 2.0.14 is set to a one, the WIS shall ignore all data presented to it by the PMA sublayer. When bit 2.0.14 is set to a one, the WIS shall accept data on the transmit path and return it on the receive path. For 10 Gb/s operation, the detailed behavior of the WIS during loopback is specified in 50.3.9.

The default value of bit 2.0.14 is zero.

NOTE—The signal path through the WIS that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the WIS circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

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45.2.2.1.3 Low power (2.0.11)

A WIS may be placed into a low-power mode by setting bit 2.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the WIS. The behavior of the WIS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 2.0.11 is zero.

45.2.2.1.4 Speed selection (2.0.13, 2.0.6, and 2.0.5:2)

Speed selection bits 2.0.13 and 2.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the WIS may be selected using bits 5 through 2. The speed abilities of the WIS are advertised in the WIS speed ability register. A WIS may ignore writes to the WIS speed selection bits that select speeds it has not advertised in the WIS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The WIS speed selection defaults to a supported ability.

45.2.2.2 WIS status 1 register (Register 2.1)

The assignment of bits in the WIS status 1 register is shown in Table 45–215. All the bits in the WIS status 1 register are read only; a write to the WIS status 1 register shall have no effect.

Table 45–215—WIS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.1.15:8	Reserved	Value always 0	RO
2.1.7	Fault	1 = Fault condition 0 = No fault condition	RO/LH
2.1.6:3	Reserved	Value always 0	RO
2.1.2	Link status	1 = WIS link up 0 = WIS link down	RO/LL
2.1.1	Low-power ability	1 = WIS supports low-power mode 0 = WIS does not support low-power mode	RO
2.1.0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.2.2.1 Fault (2.1.7)

When read as a one, bit 2.1.7 indicates that the WIS has detected a fault condition. When read as a zero, bit 2.1.7 indicates that the WIS has not detected a fault condition. The fault bit shall be implemented with latching high behavior.

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The default value of bit 2.1.7 is zero.

45.2.2.2.2 Link status (2.1.2)

When read as a one, bit 2.1.2 indicates that the WIS receive link is up. When read as a zero, bit 2.1.2 indicates that the WIS receive link is down. The link status bit shall be implemented with latching low behavior.

45.2.2.2.3 Low-power ability (2.1.1)

When read as a one, bit 2.1.1 indicates that the WIS supports the low-power feature. When read as a zero, bit 2.1.1 indicates that the WIS does not support the low-power feature. If a WIS supports the low-power feature, then it is controlled using the low-power bit in the WIS control register.

45.2.2.3 WIS device identifier (Registers 2.2 and 2.3)

Registers 2.2 and 2.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of WIS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A WIS may return a value of zero in each of the 32 bits of the WIS device identifier.

The format of the WIS device identifier is specified in 22.2.4.3.1.

45.2.2.4 WIS speed ability (Register 2.4)

The assignment of bits in the WIS speed ability register is shown in Table 45–216.

Table 45–216—WIS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
2.4.15:1	Reserved for future speeds	Value always 0	RO
2.4.0	10G capable	1 = WIS is capable of operating at 10 Gb/s 0 = WIS is not capable of operating at 10 Gb/s	RO

[a]RO = Read only

45.2.2.4.1 10G capable (2.4.0)

When read as a one, bit 2.4.0 indicates that the WIS is able to operate at a data rate of 10 Gb/s (9.58 Gb/s payload rate). When read as a zero, bit 2.4.0 indicates that the WIS is not able to operate at a data rate of 10 Gb/s (9.58 Gb/s payload rate).

45.2.2.5 WIS devices in package (Registers 2.5 and 2.6)

The WIS devices in package registers are defined in Table 45–2.

45.2.2.6 10G WIS control 2 register (Register 2.7)

The assignment of bits in the 10G WIS control 2 register is shown in Table 45–217. The default value for each bit of the 10G WIS control 2 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

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Table 45–217—10G WIS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.7.15:6	Reserved	Value always 0	RO
2.7.5	PRBS31 receive test-pattern enable	1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path	R/W
2.7.4	PRBS31 transmit test-pattern enable	1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path	R/W
2.7.3	Test-pattern selection	1 = Select square wave test pattern 0 = Select mixed-frequency test pattern	R/W
2.7.2	Receive test-pattern enable	1 = Enable test-pattern mode on the receive path 0 = Disable test-pattern mode on the receive path	R/W
2.7.1	Transmit test-pattern enable	1 = Enable test-pattern mode on the transmit path 0 = Disable test-pattern mode on the transmit path	R/W
2.7.0	PCS type selection	1 = Select 10GBASE-W PCS type 0 = Select 10GBASE-R PCS type	R/W

[a]RO = Read only, R/W = Read/Write

45.2.2.6.1 PRBS31 receive test-pattern enable (2.7.5)

If the WIS supports the optional PRBS31 (see 49.2.8) pattern testing advertised in bit 2.8.1 and the mandatory receive test-pattern enable bit (2.7.2) is not one, setting bit 2.7.5 to a one shall set the receive path of the WIS into the PRBS31 test-pattern mode. Setting bit 2.7.5 to a zero shall disable the PRBS31 test-pattern mode on the receive path of the WIS. The behavior of the WIS when in PRBS31 test-pattern mode is specified in 50.3.8.2.

45.2.2.6.2 PRBS31 transmit test-pattern enable (2.7.4)

If the WIS supports the optional PRBS31 pattern testing advertised in bit 2.8.1 and the mandatory transmit test-pattern enable bit (2.7.1) is not one, then setting bit 2.7.4 to a one shall set the transmit path of the WIS into the PRBS31 test-pattern mode. Setting bit 2.7.4 to a zero shall disable the PRBS31 test-pattern mode on the transmit path of the WIS. The behavior of the WIS when in PRBS31 test-pattern mode is specified in 50.3.8.2.

45.2.2.6.3 Test-pattern selection (2.7.3)

Bit 2.7.3 controls the type of pattern sent by the transmitter when in test-pattern mode. Setting bit 2.7.3 to a one shall select the square wave test pattern. Setting bit 2.7.3 to a zero shall select the mixed-frequency test pattern. The details of the test patterns are specified in Clause 50.

45.2.2.6.4 Receive test-pattern enable (2.7.2)

Setting bit 2.7.2 to a one shall set the receive path of the WIS into the test-pattern mode. Setting bit 2.7.2 to a zero shall disable the test-pattern mode on the receive path of the WIS. The behavior of the WIS when in test-pattern mode is specified in Clause 50.

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45.2.2.6.5 Transmit test-pattern enable (2.7.1)

Setting bit 2.7.1 to a one shall set the transmit path of the WIS into the test-pattern mode. Setting bit 2.7.1 to a zero shall disable the test-pattern mode on the transmit path of the WIS. The behavior of the WIS when in test-pattern mode is specified in Clause 50.

45.2.2.6.6 PCS type selection (2.7.0)

Setting bit 2.7.0 to a one shall enable the 10GBASE-W logic and set the speed of the WIS-PMA interface to 9.95328 Gb/s. Setting bit 2.7.0 to a zero shall disable the 10GBASE-W logic, set the speed of the PCS-PMA interface to 10.3125 Gb/s and bypass the data around the 10GBASE-W logic. A WIS that is only capable of supporting 10GBASE-W operation and is unable to support 10GBASE-R operation shall ignore values written to this bit and shall return a value of one when read. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

45.2.2.7 10G WIS status 2 register (Register 2.8)

The assignment of bits in the 10G WIS status 2 register is shown in Table 45–218. All the bits in the 10G WIS status 2 register are read only; a write to the 10G WIS status 2 register shall have no effect.

Table 45–218—10G WIS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
2.8.13:2	Reserved	Value always 0	RO
2.8.1	PRBS31 pattern testing ability	1 = WIS is able to support PRBS31 pattern testing 0 = WIS is not able to support PRBS31 pattern testing	RO
2.8.0	10GBASE-R ability	1 = WIS is able to support 10GBASE-R port types 0 = WIS is not able to support 10GBASE-R port types	RO

[a]RO = Read only

45.2.2.7.1 Device present (2.8.15:14)

When read as <10>, bits 2.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 2.8.15:14 indicate that no device is present at this address or that the device is not functioning properly.

45.2.2.7.2 PRBS31 pattern testing ability (2.8.1)

When read as a one, bit 2.8.1 indicates that the WIS is able to support PRBS31 pattern testing. When read as a zero, bit 2.8.1 indicates that the WIS is not able to support PRBS31 pattern testing. If the WIS is able to support PRBS31 pattern testing, then the pattern generation and checking is controlled using bits 2.7.5:4.

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45.2.2.7.3 10GBASE-R ability (2.8.0)

When read as a one, bit 2.8.0 indicates that the WIS is able to bypass the WIS logic and adjust the XSBI interface speed to support 10GBASE-R port types. When read as a zero, bit 2.8.0 indicates that the WIS is not able to bypass the WIS logic and cannot support 10GBASE-R port types.

45.2.2.8 10G WIS test-pattern error counter register (Register 2.9)

The assignment of bits in the 10G WIS test-pattern error counter register is shown in Table 45–219. This register is only required when the PRBS31 pattern generation capability is supported.

Table 45–219—10G WIS test-pattern error counter register bit definitions

Bit(s)	Name	Description	R/W[a]
2.9.15:0	Test-pattern error counter	Error counter	RO

[a]RO = Read only

The test-pattern error counter is a sixteen bit counter that contains the number of errors received during a pattern test. These bits shall be reset to all zeros when the test-pattern error counter is read by the management function or upon execution of the WIS reset. These bits shall be held at all ones in the case of overflow. The test-pattern methodology is described in 49.2.8.

45.2.2.9 WIS package identifier (Registers 2.14 and 2.15)

Registers 2.14 and 2.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the WIS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A WIS may return a value of zero in each of the 32 bits of the WIS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the WIS package identifier is specified in 22.2.4.3.1.

45.2.2.10 10G WIS status 3 register (Register 2.33)

The assignment of bits in the 10G WIS status 3 register is shown in Table 45–220. All the bits in the 10G WIS status 3 register are read only; a write to the 10G WIS status 3 register shall have no effect.

45.2.2.10.1 SEF (2.33.11)

When read as a one, bit 2.33.11 indicates that the SEF flag has been raised by the WIS. When read as a zero, bit 2.33.11 indicates that the SEF flag is lowered. The SEF bit shall be implemented with latching high behavior.

The SEF functionality implemented by the WIS is described in 50.3.2.5.

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Table 45–220—10G WIS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.33.15:12	Reserved	Value always 0	RO
2.33.11	SEF	Severely errored frame	RO/LH
2.33.10	Far end PLM-P/LCD-P	1 = Far end path label mismatch / Loss of code-group delineation 0 = No far end path label mismatch / Loss of code-group delineation	RO/LH
2.33.9	Far end AIS-P/LOP-P	1 = Far end path alarm indication signal / Path loss of pointer 0 = No far end path alarm indication signal / Path loss of pointer	RO/LH
2.33.8	Reserved	Value always 0	RO
2.33.7	LOF	1 = Loss of frame flag raised 0 = Loss of frame flag lowered	RO/LH
2.33.6	LOS	1 = Loss of signal flag raised 0 = Loss of signal flag lowered	RO/LH
2.33.5	RDI-L	1 = Line remote defect flag raised 0 = Line remote defect flag lowered	RO/LH
2.33.4	AIS-L	1 = Line alarm indication flag raised 0 = Line alarm indication flag lowered	RO/LH
2.33.3	LCD-P	1 = Path loss of code-group delineation flag raised 0 = Path loss of code-group delineation flag lowered	RO/LH
2.33.2	PLM-P	1 = Path label mismatch flag raised 0 = Path label mismatch flag lowered	RO/LH
2.33.1	AIS-P	1 = Path alarm indication signal raised 0 = Path alarm indication signal lowered	RO/LH
2.33.0	LOP-P	1 = Loss of pointer flag raised 0 = Loss of pointer flag lowered	RO/LH

[a]RO = Read only, LH = Latching high

45.2.2.10.2 Far end PLM-P/LCD-P (2.33.10)

When read as a one, bit 2.33.10 indicates that the far end path label mismatch/loss of code-group delineation flag has been raised. When read as a zero, bit 2.33.10 indicates that the far end path label mismatch/loss of code-group delineation flag is lowered. The far end PLM-P/LCD-P bit shall be implemented with latching high behavior.

The far end path label mismatch/loss of code-group delineation functionality implemented by the WIS is described in 50.3.2.5.

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45.2.2.10.3 Far end AIS-P/LOP-P (2.33.9)

When read as a one, bit 2.33.9 indicates that the far end path alarm indication signal/path loss of pointer flag has been raised by the WIS. When read as a zero, bit 2.33.9 indicates that the far end path alarm indication signal/path loss of pointer flag is lowered. The far end AIS-P/LOP-P bit shall be implemented with latching high behavior.

The far end path alarm indication signal/path loss of pointer functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.4 LOF (2.33.7)

When read as a one, bit 2.33.7 indicates that the loss of frame flag has been raised. When read as a zero, bit 2.33.7 indicates that the loss of frame flag is lowered. The LOF bit shall be implemented with latching high behavior.

The LOF functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.5 LOS (2.33.6)

When read as a one, bit 2.33.6 indicates that the loss of signal flag has been raised. When read as a zero, bit 2.33.6 indicates that the loss of signal flag is lowered. The LOS bit shall be implemented with latching high behavior.

The LOS functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.6 RDI-L (2.33.5)

When read as a one, bit 2.33.5 indicates that the line remote defect flag has been raised. When read as a zero, bit 2.33.5 indicates that the line remote defect flag is lowered. The RDI-L bit shall be implemented with latching high behavior.

The RDI-L functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.7 AIS-L (2.33.4)

When read as a one, bit 2.33.4 indicates that the line alarm indication flag has been raised. When read as a zero, bit 2.33.4 indicates that the line alarm indication flag is lowered. The AIS-L bit shall be implemented with latching high behavior.

The AIS-L functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.8 LCD-P (2.33.3)

When read as a one, bit 2.33.3 indicates that the loss of code-group delineation flag has been raised. When read as a zero, bit 2.33.3 indicates that the loss of code-group delineation flag is lowered. The LCD-P bit shall be implemented with latching high behavior.

The loss of code-group delineation functionality implemented by the WIS is described in 50.3.2.5.

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45.2.2.10.9 PLM-P (2.33.2)

When read as a one, bit 2.33.2 indicates that the path label mismatch flag has been raised. When read as a zero, bit 2.33.2 indicates that the path label mismatch flag is lowered. The PLM-P bit shall be implemented with latching high behavior.

The PLM-P functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.10 AIS-P (2.33.1)

When read as a one, bit 2.33.1 indicates that the path alarm indication signal has been raised. When read as a zero, bit 2.33.1 indicates that the path alarm indication signal is lowered. The AIS-P bit shall be implemented with latching high behavior.

The path alarm indication signal functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.11 LOP-P (2.33.0)

When read as a one, bit 2.33.0 indicates that the loss of pointer flag has been raised. When read as a zero, bit 2.33.0 indicates that the loss of pointer flag is lowered. The LOP-P bit shall be implemented with latching high behavior.

The LOP-P functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.11 10G WIS far end path block error count (Register 2.37)

The assignment of bits in the 10G WIS far end path block error count register is shown in Table 45–221.

Table 45–221—10G WIS far end path block error count register bit definitions

Bit(s)	Name	Description	R/W[a]
2.37.15:0	Far end path block error count	Far end path block error count	RO

[a]RO = Read only,

The 10G WIS far end path block error count is incremented by one whenever a far end path block error, defined in Annex 50A, is detected as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

45.2.2.12 10G WIS J1 transmit (Registers 2.39 through 2.46)

The assignment of octets in the 10G WIS J1 transmit registers is shown in Table 45–222.

The first transmitted path trace octet is J1 transmit 15, which contains the delineation octet. The default value for the J1 transmit 15 octet is 137 (hexadecimal 89). The last transmitted path trace octet is J1 transmit 0. The default value for the J1 transmit 0 through 14 octets is 0. The transmitted path trace is described in 50.3.2.1.

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Table 45–222—10G WIS J1 transmit 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.46.15:8	J1 transmit 15	Transmitted path trace octet 15	R/W
2.46.7:0	J1 transmit 14	Transmitted path trace octet 14	R/W
2.45.15:8	J1 transmit 13	Transmitted path trace octet 13	R/W
2.45.7:0	J1 transmit 12	Transmitted path trace octet 12	R/W
2.44.15:8	J1 transmit 11	Transmitted path trace octet 11	R/W
2.44.7:0	J1 transmit 10	Transmitted path trace octet 10	R/W
2.43.15:8	J1 transmit 9	Transmitted path trace octet 9	R/W
2.43.7:0	J1 transmit 8	Transmitted path trace octet 8	R/W
2.42.15:8	J1 transmit 7	Transmitted path trace octet 7	R/W
2.42.7:0	J1 transmit 6	Transmitted path trace octet 6	R/W
2.41.15:8	J1 transmit 5	Transmitted path trace octet 5	R/W
2.41.7:0	J1 transmit 4	Transmitted path trace octet 4	R/W
2.40.15:8	J1 transmit 3	Transmitted path trace octet 3	R/W
2.40.7:0	J1 transmit 2	Transmitted path trace octet 2	R/W
2.39.15:8	J1 transmit 1	Transmitted path trace octet 1	R/W
2.39.7:0	J1 transmit 0	Transmitted path trace octet 0	R/W

[a]R/W = Read/Write

45.2.2.13 10G WIS J1 receive (Registers 2.47 through 2.54)

The assignment of octets in the 10G WIS J1 receive registers is shown in Table 45–223.

Table 45–223—10G WIS J1 receive 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.54.15:8	J1 receive 15	Received path trace octet 15	RO
2.54.7:0	J1 receive 14	Received path trace octet 14	RO
2.53.15:8	J1 receive 13	Received path trace octet 13	RO
2.53.7:0	J1 receive 12	Received path trace octet 12	RO
2.52.15:8	J1 receive 11	Received path trace octet 11	RO

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Table 45–223—10G WIS J1 receive 0–15 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
2.52.7:0	J1 receive 10	Received path trace octet 10	RO
2.51.15:8	J1 receive 9	Received path trace octet 9	RO
2.51.7:0	J1 receive 8	Received path trace octet 8	RO
2.50.15:8	J1 receive 7	Received path trace octet 7	RO
2.50.7:0	J1 receive 6	Received path trace octet 6	RO
2.49.15:8	J1 receive 5	Received path trace octet 5	RO
2.49.7:0	J1 receive 4	Received path trace octet 4	RO
2.48.15:8	J1 receive 3	Received path trace octet 3	RO
2.48.7:0	J1 receive 2	Received path trace octet 2	RO
2.47.15:8	J1 receive 1	Received path trace octet 1	RO
2.47.7:0	J1 receive 0	Received path trace octet 0	RO

[a]RO = Read only

The first received path trace octet is J1 receive 15. The last received path trace octet is J1 receive 0. The received path trace is described in 50.3.2.4.

45.2.2.14 10G WIS far end line BIP errors (Registers 2.55 and 2.56)

The assignment of octets in the 10G WIS far end line BIP errors registers is shown in Table 45–224.

Table 45–224—10G WIS far end line BIP errors 0–1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.56.15:0	WIS far end line BIP errors 0	Least significant word of the WIS far end line BIP errors counter	RO
2.55.15:0	WIS far end line BIP errors 1	Most significant word of the WIS far end line BIP errors counter	RO

[a]RO = Read only

The 10G WIS far end line BIP Errors register pair reflects the contents of the far end line BIP errors counter (as described in 50.3.11.3) that is incremented on each WIS frame by the number of far end line BIP errors reported by the far end, as described in 50.3.2.5. Whenever the most significant 16 bit register of the counter (2.55) is read, the 32 bit counter value is latched into the register pair, with the most significant bits appearing in 2.55 and the least significant 16 bits appearing in 2.56, the value being latched before the contents of 2.55 (the most significant 16 bits) are driven on the MDIO interface. A subsequent read from register 2.56 will return the least significant 16 bits of the latched value, but will not change the register contents. Writes to these registers have no effect.

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NOTE—These counters do not follow the behavior described in 45.2 for 32-bit counters.

45.2.2.15 10G WIS line BIP errors (Registers 2.57 and 2.58)

The assignment of octets in the 10G WIS line BIP errors registers is shown in Table 45–225.

Table 45–225—10G WIS line BIP errors 0–1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.58.15:0	WIS line BIP errors 0	Least significant word of the WIS line BIP errors counter	RO
2.57.15:0	WIS line BIP errors 1	Most significant word of the WIS line BIP errors counter	RO

[a]RO = Read only

The 10G WIS line BIP errors register pair reflects the contents of the line BIP errors counter (as described in 50.3.11.3) that is incremented on each WIS frame by the number of line BIP errors detected on the incoming data stream, as described in 50.3.2.5. Whenever the most significant 16 bit register of the counter (2.57) is read, the 32 bit counter value is latched into the register pair, with the most significant bits appearing in 2.57 and the least significant 16 bits appearing in 2.58, the value being latched before the contents of 2.57 (the most significant 16 bits) are driven on the MDIO interface. A subsequent read from register 2.58 will return the least significant 16 bits of the latched value, but will not change the register contents. Writes to these registers have no effect.

NOTE—These counters do not follow the behavior described in 45.2 for 32-bit counters.

45.2.2.16 10G WIS path block error count (Register 2.59)

The assignment of bits in the 10G WIS path block error count register is shown in Table 45–226.

Table 45–226—10G WIS path block error count register bit definitions

Bit(s)	Name	Description	R/W[a]
2.59.15:0	Path block error count	Path block error counter	RO

[a]RO = Read only

45.2.2.16.1 Path block error count (2.59.15:0)

The path block error count is incremented by one whenever a B3 parity error (defined in Annex 50A) is detected, as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

45.2.2.17 10G WIS section BIP error count (Register 2.60)

The assignment of bits in the 10G WIS section BIP error count register is shown in Table 45–227.

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Table 45–227—10G WIS section BIP error count register bit definitions

Bit(s)	Name	Description	R/W[a]
2.60.15:0	Section BIP error count	Section BIP error count	RO

[a]RO = Read only

45.2.2.17.1 Section BIP error count (2.60.15:0)

The section BIP error count is incremented by the number of section BIP errors detected within each WIS frame, as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

45.2.2.18 10G WIS J0 transmit (Registers 2.64 through 2.71)

The assignment of octets in the 10G WIS J0 transmit registers is shown in Table 45–228.

Table 45–228—10G WIS J0 transmit 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.71.15:8	J0 transmit 15	Transmitted section trace octet 15	R/W
2.71.7:0	J0 transmit 14	Transmitted section trace octet 14	R/W
2.70.15:8	J0 transmit 13	Transmitted section trace octet 13	R/W
2.70.7:0	J0 transmit 12	Transmitted section trace octet 12	R/W
2.69.15:8	J0 transmit 11	Transmitted section trace octet 11	R/W
2.69.7:0	J0 transmit 10	Transmitted section trace octet 10	R/W
2.68.15:8	J0 transmit 9	Transmitted section trace octet 9	R/W
2.68.7:0	J0 transmit 8	Transmitted section trace octet 8	R/W
2.67.15:8	J0 transmit 7	Transmitted section trace octet 7	R/W
2.67.7:0	J0 transmit 6	Transmitted section trace octet 6	R/W
2.66.15:8	J0 transmit 5	Transmitted section trace octet 5	R/W
2.66.7:0	J0 transmit 4	Transmitted section trace octet 4	R/W
2.65.15:8	J0 transmit 3	Transmitted section trace octet 3	R/W
2.65.7:0	J0 transmit 2	Transmitted section trace octet 2	R/W
2.64.15:8	J0 transmit 1	Transmitted section trace octet 1	R/W
2.64.7:0	J0 transmit 0	Transmitted section trace octet 0	R/W

[a]R/W = Read/Write

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The J0 transmit octets allow a receiver to verify its continued connection to the WIS transmitter. The first transmitted section trace octet is J0 transmit 15, which contains the delineation octet. The default value for the J0 transmit 15 octet is 137 (hexadecimal 89). The last transmitted section trace octet is J0 transmit 0. The default value for the J0 transmit 0 through 14 octets is 0. The transmitted section trace is described in 50.3.2.3.

45.2.2.19 10G WIS J0 receive (Registers 2.72 through 2.79)

The assignment of octets in the 10G WIS J0 receive registers is shown in Table 45–229.

Table 45–229— 10G WIS J0 receive 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.79.15:8	J0 receive 15	Received section trace octet 15	RO
2.79.7:0	J0 receive 14	Received section trace octet 14	RO
2.78.15:8	J0 receive 13	Received section trace octet 13	RO
2.78.7:0	J0 receive 12	Received section trace octet 12	RO
2.77.15:8	J0 receive 11	Received section trace octet 11	RO
2.77.7:0	J0 receive 10	Received section trace octet 10	RO
2.76.15:8	J0 receive 9	Received section trace octet 9	RO
2.76.7:0	J0 receive 8	Received section trace octet 8	RO
2.75.15:8	J0 receive 7	Received section trace octet 7	RO
2.75.7:0	J0 receive 6	Received section trace octet 6	RO
2.74.15:8	J0 receive 5	Received section trace octet 5	RO
2.74.7:0	J0 receive 4	Received section trace octet 4	RO
2.73.15:8	J0 receive 3	Received section trace octet 3	RO
2.73.7:0	J0 receive 2	Received section trace octet 2	RO
2.72.15:8	J0 receive 1	Received section trace octet 1	RO
2.72.7:0	J0 receive 0	Received section trace octet 0	RO

[a]RO = Read only

The first received section trace octet is J0 receive 15. The last received section trace octet is J0 receive 0. The J0 receive octets allow a WIS receiver to verify its continued connection to the intended transmitter. The received section trace is described in 50.3.2.4.

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45.2.2.20 TimeSync WIS capability (Register 2.1800)

The TimeSync WIS capability register (see Table 45–230) indicates the capability of the WIS to report the transmit and receive data delay, stored in registers 2.1801 through 2.1804 and 2.1805 through 2.1808, respectively.

Table 45–230—TimeSync WIS capability

Bit(s)	Name	Description	R/W[a]
2.1800.15:2	Reserved	Value always 0	RO
2.1800.1	TimeSync transmit path data delay	1 = WIS provides information on transmit path data delay in registers 2.1801 through 2.1804 0 = WIS does not provide information on transmit path data delay	RO
2.1800.0	TimeSync receive path data delay	1 = WIS provides information on receive path data delay in registers 2.1805 through 2.1808 0 = WIS does not provide information on receive path data delay	RO

[a]RO = Read only

45.2.2.21 TimeSync WIS transmit path data delay (Registers 2.1801, 2.1802, 2.1803, 2.1804)

The TimeSync WIS transmit path data delay register contains the maximum (registers 2.1801, 2.1802, see Table 45–231) and minimum (registers 2.1803, 2.1804, see Table 45–231) values of the transmit path data delay. The transmit path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in register 1.1 (see 45.2.1.2.4).

Table 45–231—TimeSync WIS transmit path data delay register

Bit(s)	Name	Description	R/W[a]
2.1801.15:0	Maximum WIS transmit path data delay, lower	WIS_delay_TX_max [15:0]	RO, MW
2.1802.15:0	Maximum WIS transmit path data delay, upper	WIS_delay_TX_max [31:16]	RO, MW
2.1803.15:0	Minimum WIS transmit path data delay, lower	WIS_delay_TX_min [15:0]	RO, MW
2.1804.15:0	Minimum WIS transmit path data delay, upper	WIS_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.2.22 TimeSync WIS receive path data delay (Registers 2.1805, 2.1806, 2.1807, 2.1808)

The TimeSync WIS receive path data delay register contains the maximum (registers 2.1805, 2.1806, see Table 45–232) and minimum (registers 2.1807, 2.1808, see Table 45–232) values of the receive path data delay. The receive path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in register 2.1 (see 45.2.2.2.2).

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Table 45–232—TimeSync WIS receive path data delay register

Bit(s)	Name	Description	R/W[a]
2.1805.15:0	Maximum WIS receive path data delay, lower	WIS_delay_RX_max [15:0]	RO, MW
2.1806.15:0	Maximum WIS receive path data delay, upper	WIS_delay_RX_max [31:16]	RO, MW
2.1807.15:0	Minimum WIS receive path data delay, lower	WIS_delay_RX_min [15:0]	RO, MW
2.1808.15:0	Minimum WIS receive path data delay, upper	WIS_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.3 PCS registers

The assignment of registers in the PCS is shown in Table 45–233.

Table 45–233—PCS registers

Register address	Register name	Subclause
3.0	PCS control 1	45.2.3.1
3.1	PCS status 1	45.2.3.2
3.2, 3.3	PCS device identifier	45.2.3.3
3.4	PCS speed ability	45.2.3.4
3.5, 3.6	PCS devices in package	45.2.3.5
3.7	PCS control 2	45.2.3.6
3.8	PCS status 2	45.2.3.7
3.9	PCS status 3	45.2.3.8
3.10 through 3.13	Reserved	
3.14, 3.15	PCS package identifier	45.2.3.9
3.16 through 3.19	Reserved	
3.20	EEE control and capability 1	45.2.3.10
3.21	EEE control and capability 2	45.2.3.11
3.22	EEE wake error counter	45.2.3.12
3.23	Reserved	
3.24	10GBASE-X PCS status	45.2.3.13
3.25	10GBASE-X PCS test control	45.2.3.14
3.26 through 3.31	Reserved	
3.32	BASE-R and MultiGBASE-T PCS status 1	45.2.3.15
3.33	BASE-R and MultiGBASE-T PCS status 2	45.2.3.16
3.34 through 3.37	5/10/25GBASE-R PCS test pattern seed A	45.2.3.17
3.38 through 3.41	5/10/25GBASE-R PCS test pattern seed B	45.2.3.18
3.42	BASE-R PCS test-pattern control	45.2.3.19
3.43	BASE-R PCS test-pattern error counter	45.2.3.20
3.44	BER high order counter	45.2.3.21
3.45	Errored blocks high order counter	45.2.3.22

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Table 45–233—PCS registers *(continued)*

Register address	Register name	Subclause
3.46 through 3.49	Reserved	
3.50 through 3.53	Multi-lane BASE-R PCS alignment status 1 through 4	45.2.3.23
3.54 through 3.59	Reserved	
3.60	10P/2B capability	45.2.3.27
3.61	10P/2B PCS control	45.2.3.28
3.62, 3.63	10P/2B PME available	45.2.3.29
3.64, 3.65	10P/2B PME aggregate	45.2.3.30
3.66	10P/2B PAF RX error counter	45.2.3.31
3.67	10P/2B PAF small fragment counter	45.2.3.32
3.68	10P/2B PAF large fragments counter	45.2.3.33
3.69	10P/2B PAF overflow counter	45.2.3.34
3.70	10P/2B PAF bad fragments counter	45.2.3.35
3.71	10P/2B PAF lost fragments counter	45.2.3.36
3.72	10P/2B PAF lost starts of fragments counter	45.2.3.37
3.73	10P/2B PAF lost ends of fragments counter	45.2.3.38
3.74	10GBASE-PR and 10/1GBASE-PRX FEC ability	45.2.3.39
3.75	10GBASE-PR and 10/1GBASE-PRX FEC control	45.2.3.40
3.76, 3.77	10G-EPON and Nx25G-EPON corrected FEC codewords counter	45.2.3.41
3.78, 3.79	10G-EPON and Nx25G-EPON uncorrected FEC codewords counter	45.2.3.42
3.80	10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval control	45.2.3.43
3.81	10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status	45.2.3.44
3.82	10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control	45.2.3.45
3.83 through 3.134	Nx25G-EPON synchronization pattern	45.2.3.46
3.135 through 3.199	Reserved	
3.200 through 3.219	BIP error counters, lanes 0 through 19	45.2.3.47
3.220 through 3.399	Reserved	
3.400 through 3.419	PCS lane mapping registers, lanes 0 through 19	45.2.3.49
3.420 through 3.499	Reserved	
3.500	1000BASE-H OAM transmit control	45.2.3.51
3.501 through 3.508	1000BASE-H OAM transmit message	45.2.3.51
3.509	1000BASE-H OAM receive control	45.2.3.52
3.510 through 3.517	1000BASE-H OAM receive message	45.2.3.52
3.518	1000BASE-H PCS control	45.2.3.53
3.519	1000BASE-H PCS status 1	45.2.3.54
3.520	1000BASE-H PCS status 2	45.2.3.55
3.521	1000BASE-H PCS status 3	45.2.3.56
3.522	1000BASE-H PCS status 4	45.2.3.57
3.523 through 3.599	Reserved	

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Table 45–233—PCS registers *(continued)*

Register address	Register name	Subclause
3.600 through 3.631	PCS FEC symbol error counter, lane 0 to 15	45.2.3.58, 45.2.3.59
3.632 through 3.799	Reserved	
3.800	PCS FEC control	45.2.3.60
3.801	PCS FEC status	45.2.3.61
3.802, 3.803	PCS FEC corrected codewords counter	45.2.3.62
3.804, 3.805	PCS FEC uncorrected codewords counter	45.2.3.63
3.806, 3.807	PCS FEC degraded SER activate threshold	45.2.3.64
3.808, 3.809	PCS FEC degraded SER deactivate threshold	45.2.3.65
3.810, 3.811	PCS FEC degraded SER interval	45.2.3.66
3.812 through 3.1799	Reserved	
3.1800	TimeSync PCS capability	45.2.3.67
3.1801 through 3.1804	TimeSync PCS transmit path data delay	45.2.3.68
3.1805 through 3.1808	TimeSync PCS receive path data delay	45.2.3.69
3.1809 through 3.2277	Reserved	
3.2278	10BASE-T1L PCS control	45.2.3.70
3.2279	10BASE-T1L PCS status	45.2.3.71
3.2280 through 3.2290	Reserved	
3.2291	10BASE-T1S PCS control	45.2.3.72
3.2292	10BASE-T1S PCS status	45.2.3.73
3.2293	10BASE-T1S PCS diagnostic 1	45.2.3.74
3.2294	10BASE-T1S PCS diagnostic 2	45.2.3.75
3.2295 through 3.2303	Reserved	
3.2304	1000BASE-T1 PCS control	45.2.3.76
3.2305	1000BASE-T1 PCS status 1	45.2.3.77
3.2306	1000BASE-T1 PCS status 2	45.2.3.78
3.2307	Reserved	
3.2308	BASE-T1 OAM transmit	45.2.3.79
3.2309 through 3.2312	BASE-T1 OAM message	45.2.3.80
3.2313	BASE-T1 OAM receive	45.2.3.81
3.2314 through 3.2317	Link partner BASE-T1 OAM message	45.2.3.82
3.2318 through 3.2319	MultiGBASE-T1 OAM status message	45.2.3.83
3.2320 through 3.2321	Link partner MultiGBASE-T1 OAM status message	45.2.3.84
3.2322	MultiGBASE-T1 PCS control	45.2.3.85
3.2323	MultiGBASE-T1 PCS status 1	45.2.3.86
3.2324	MultiGBASE-T1 PCS status 2	45.2.3.87
3.2325 through 3.32767	Reserved	
3.32 768 through 3.65 535	Vendor specific	

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45.2.3.1 PCS control 1 register (Register 3.0)

The assignment of bits in the PCS control 1 register is shown in Table 45–234. The default value for each bit of the PCS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–234—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.0.15	Reset	1 = PCS reset 0 = Normal operation	R/W SC
3.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.0.13	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
3.0.12	Reserved	Value always 0	RO
3.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
3.0.10	Clock stop enable	1 = The PHY may stop the clock during LPI 0 = Clock not stoppable	R/W
3.0.9:7	Reserved	Value always 0	RO
3.0.6	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
3.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 1 = 25/10 Gb/s 1 0 1 0 = 400 Gb/s 1 0 0 1 = 200 Gb/s 1 0 0 0 = 5 Gb/s 0 1 1 1 = 2.5 Gb/s 0 1 1 0 = 50 Gb/s 0 1 0 1 = 25 Gb/s 0 1 0 0 = 100 Gb/s 0 0 1 1 = 40 Gb/s 0 0 1 0 = 10/1 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
3.0.1:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

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45.2.3.1.1 Reset (3.0.15)

Resetting a PCS is accomplished by setting bit 3.0.15 to a one. This action shall set all PCS registers to their default states. As a consequence, this action may change the internal state of the PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PCS shall return a value of one in bit 3.0.15 when a reset is in progress and a value of zero otherwise. A PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 3.0.15. During a reset, a PCS shall respond to reads from register bits 3.0.15 and 3.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.3.1.2 Loopback (3.0.14)

When the 100BASE-T1, any MultiGBASE-T, or the 5/10GBASE-R mode of operation is selected for the PCS using the PCS type selection field (3.7.3:0), the PCS shall be placed in a loopback mode of operation when bit 3.0.14 is set to a one. When bit 3.0.14 is set to a one, the 100BASE-T1, 5/10GBASE-R, or any PCS in the MultiGBASE-T set shall accept data on the transmit path and return it on the receive path. The speed of the loopback is selected by the PCS control 1 (register 3.0) defined in 45.2.3.1. The specific behavior of the 100BASE-T1 PCS during loopback is specified in 96.3.5. The specific behavior of the 5/10GBASE-R PCS during loopback is specified in 49.2. The specific behavior for the 10GBASE-T PCS during loopback is specified in 55.3.7.3. The specific behavior for the 25GBASE-T and 40GBASE-T PCS during loopback is specified in 113.3.7.3. The specific behavior for the 2.5GBASE-T or 5GBASE-T PCS during loopback is specified in 126.3.7.3. For all other port types, the PCS loopback functionality is not applicable and writes to this bit shall be ignored and reads from this bit shall return a value of zero.

The default value of bit 3.0.14 is zero.

NOTE—The signal path through the PCS that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PCS circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.3.1.3 Low power (3.0.11)

A PCS may be placed into a low-power mode by setting bit 3.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PCS. The behavior of the PCS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 3.0.11 is zero.

45.2.3.1.4 Clock stop enable (3.0.10)

If bit 3.0.10 is set to one then the PHY may stop the receive xMII clock while it is signaling LPI otherwise it shall keep the clock active. If the PHY does not support EEE capability or is not able to stop the receive clock then this bit has no effect (see 22.2.2.2, 35.2.2.10, and 46.3.2.4).

45.2.3.1.5 Speed selection (3.0.13, 3.0.6, 3.0.5:2)

Speed selection bits 3.0.13 and 3.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

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The speed of the PCS may be selected using bits 5 through 2. The speed abilities of the PCS are advertised in the PCS speed ability register. A PCS may ignore writes to the PCS speed selection bits that select speeds it has not advertised in the PCS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PCS speed selection defaults to a supported ability.

The speed selection bits 3.0.5:2, when set to 0001, select the use of the 10PASS-TS and 2BASE-TL PCS.

45.2.3.2 PCS status 1 register (Register 3.1)

The assignment of bits in the PCS status 1 register is shown in Table 45–235. All the bits in the PCS status 1 register are read only; a write to the PCS status 1 register shall have no effect.

Table 45–235—PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.1.15:12	Reserved	Value always 0	RO
3.1.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.1.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.1.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.1.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.1.6	Clock stop capable	1 = The MAC may stop the clock during LPI 0 = Clock not stoppable	RO
3.1.5:3	Reserved	Value always 0	RO
3.1.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.1.1	Low-power ability	1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO
3.1.0	Reserved	Value always 0	RO

[a]RO = Read only, LL = Latching low, LH = Latching high

45.2.3.2.1 Transmit LPI received (3.1.11)

When read as a one, bit 3.1.11 indicates that the transmit PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.1.11 indicates that the PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

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45.2.3.2.2 Receive LPI received (3.1.10)

When read as a one, bit 3.1.10 indicates that the receive PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.1.10 indicates that the PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.2.3 Transmit LPI indication (3.1.9)

When read as a one, bit 3.1.9 indicates that the transmit PCS is currently receiving LPI signals. When read as a zero, bit 3.1.9 indicates that the PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.2.4 Receive LPI indication (3.1.8)

When read as a one, bit 3.1.8 indicates that the receive PCS is currently receiving LPI signals. When read as a zero, bit 3.1.8 indicates that the PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.2.5 Fault (3.1.7)

When read as a one, bit 3.1.7 indicates that the PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.1.7 indicates that the PCS has not detected a fault condition. For 10 Gb/s operation, bit 3.1.7 is read as a one when either of the fault bits (3.8.11, 3.8.10) located in register 3.8 are read as a one. For 10BASE-TS or 2BASE-TL operation, this bit shall become a one when any 10P/2B PCS registers indicate a fault (see 45.2.3.31 through 45.2.3.38).

45.2.3.2.6 Clock stop capable (3.1.6)

If bit 3.1.6 is set to one then the RS may stop the transmit xMII clock while it is signaling LPI otherwise it shall keep the clock active. If the RS does not support EEE capability or is not able to stop the transmit clock then this bit has no effect (see 22.2.2.6, 35.2.2.6, and 46.3.2.4).

45.2.3.2.7 PCS receive link status (3.1.2)

When read as a one, bit 3.1.2 indicates that the PCS receive link is up. When read as a zero, bit 3.1.2 indicates that the PCS receive link is down. When a 10/25/40/50/100/200/400GBASE-R, 10GBASE-W, or any MultiGBASE-T mode of operation is selected for the PCS using the PCS type selection field (3.7.3:0), this bit is a latching low version of bit 3.32.12. When a 10GBASE-X mode of operation is selected for the PCS using the PCS type selection field (3.7.3:0), this bit is a latching low version of bit 3.24.12. The receive link status bit shall be implemented with latching low behavior.

45.2.3.2.8 Low-power ability (3.1.1)

When read as a one, bit 3.1.1 indicates that the PCS supports the low-power feature. When read as a zero, bit 3.1.1 indicates that the PCS does not support the low-power feature. If a PCS supports the low-power feature then it is controlled using the low-power bit 3.0.11.

45.2.3.3 PCS device identifier (Registers 3.2 and 3.3)

Registers 3.2 and 3.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PCS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PCS may return a value of zero in each of the 32 bits of the PCS device identifier.

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The format of the PCS device identifier is specified in 22.2.4.3.1.

45.2.3.4 PCS speed ability (Register 3.4)

The assignment of bits in the PCS speed ability register is shown in Table 45–236.

Table 45–236—PCS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
3.4.15:10	Reserved for future speeds	Value always 0	RO
3.4.9	400G capable	1 = PCS is capable of operating at 400 Gb/s 0 = PCS is not capable of operating at 400 Gb/s	RO
3.4.8	200G capable	1 = PCS is capable of operating at 200 Gb/s 0 = PCS is not capable of operating at 200 Gb/s	RO
3.4.7	5G capable	1 = PCS is capable of operating at 5 Gb/s 0 = PCS is not capable of operating at 5 Gb/s	RO
3.4.6	2.5G capable	1 = PCS is capable of operating at 2.5 Gb/s 0 = PCS is not capable of operating at 2.5 Gb/s	RO
3.4.5	50G capable	1 = PCS is capable of operating at 50 Gb/s 0 = PCS is not capable of operating at 50 Gb/s	RO
3.4.4	25G capable	1 = PCS is capable of operating at 25 Gb/s 0 = PCS is not capable of operating at 25 Gb/s	RO
3.4.3	100G capable	1 = PCS is capable of operating at 100 Gb/s 0 = PCS is not capable of operating at 100 Gb/s	RO
3.4.2	40G capable	1 = PCS is capable of operating at 40 Gb/s 0 = PCS is not capable of operating at 40 Gb/s	RO
3.4.1	10PASS-TS/2BASE-TL capable	1 = PCS is capable of operating as the 10P/2B PCS 0 = PCS is not capable of operating as the 10P/2B PCS	RO
3.4.0	10G capable	1 = PCS is capable of operating at 10 Gb/s 0 = PCS is not capable of operating at 10 Gb/s	RO

[a]RO = Read only

45.2.3.4.1 10G capable (3.4.0)

When read as a one, bit 3.4.0 indicates that the PCS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 3.4.0 indicates that the PCS is not able to operate at a data rate of 10 Gb/s.

45.2.3.4.2 10PASS-TS/2BASE-TL capable

When read as a one, this bit indicates that the PCS is able to operate as the 10PASS-TS/2BASE-TL PCS, as specified in Clause 61.

45.2.3.4.3 40G capable (3.4.2)

When read as a one, bit 3.4.2 indicates that the PCS is able to operate at a data rate of 40 Gb/s. When read as a zero, bit 3.4.2 indicates that the PCS is not able to operate at a data rate of 40 Gb/s.

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45.2.3.4.4 100G capable (3.4.3)

When read as a one, bit 3.4.3 indicates that the PCS is able to operate at a data rate of 100 Gb/s. When read as a zero, bit 3.4.3 indicates that the PCS is not able to operate at a data rate of 100 Gb/s.

45.2.3.4.5 25G capable (3.4.4)

When read as a one, bit 3.4.4 indicates that the PCS is able to operate at a data rate of 25 Gb/s. When read as a zero, bit 3.4.4 indicates that the PCS is not able to operate at a data rate of 25 Gb/s.

45.2.3.4.6 50G capable (3.4.5)

When read as a one, bit 3.4.5 indicates that the PCS is able to operate at a data rate of 50 Gb/s. When read as a zero, bit 3.4.5 indicates that the PCS is not able to operate at a data rate of 50 Gb/s.

45.2.3.4.7 2.5G capable (3.4.6)

When read as a one, bit 3.4.6 indicates that the PCS is able to operate at a data rate of 2.5 Gb/s. When read as a zero, bit 3.4.6 indicates that the PCS is not able to operate at a data rate of 2.5 Gb/s.

45.2.3.4.8 5G Capable (3.4.7)

When read as a one, bit 3.4.7 indicates that the PCS is able to operate at a data rate of 5 Gb/s. When read as a zero, bit 3.4.7 indicates that the PCS is not able to operate at a data rate of 5 Gb/s.

45.2.3.4.9 200G capable (3.4.8)

When read as a one, bit 3.4.8 indicates that the PCS is able to operate at a data rate of 200 Gb/s. When read as a zero, bit 3.4.8 indicates that the PCS is not able to operate at a data rate of 200 Gb/s.

45.2.3.4.10 400G capable (3.4.9)

When read as a one, bit 3.4.9 indicates that the PCS is able to operate at a data rate of 400 Gb/s. When read as a zero, bit 3.4.9 indicates that the PCS is not able to operate at a data rate of 400 Gb/s.

45.2.3.5 PCS devices in package (Registers 3.5 and 3.6)

The PCS devices in package registers are defined in Table 45–2.

45.2.3.6 PCS control 2 register (Register 3.7)

The assignment of bits in the PCS control 2 register is shown in Table 45–237. The default value for each bit of the PCS control 2 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

45.2.3.6.1 PCS type selection (3.7.4:0)

The PCS type shall be selected using bits 4 through 0. The PCS type abilities of the PCS are advertised in bits 3.8.9:0 and 3.9.7:0. A PCS shall ignore writes to the PCS type selection bits that select PCS types it has not advertised in the PCS status 2 register or the PCS status 3 register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY. The PCS type selection defaults to a supported ability.

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Table 45–237—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.7.15:5	Reserved	Value always 0	RO
3.7.4:0	PCS type selection	4 3 2 1 0 1 1 x x x = reserved 1 0 1 x x = reserved 1 0 0 1 1 = Select 25GBASE-PQ PCS type 1 0 0 1 0 = Select 25/10GBASE-PQ PCS type 1 0 0 0 1 = Select 25GBASE-PQ PCS type, Tx only 1 0 0 0 0 = Select 25GBASE-PQ PCS type, Rx only 0 1 1 1 1 = Select 5GBASE-R PCS type 0 1 1 1 0 = Select 2.5GBASE-X PCS type 0 1 1 0 1 = Select 400GBASE-R PCS type 0 1 1 0 0 = Select 200GBASE-R PCS type 0 1 0 1 1 = Select 5GBASE-T PCS type 0 1 0 1 0 = Select 2.5GBASE-T PCS type 0 1 0 0 1 = Select 25GBASE-T PCS type 0 1 0 0 0 = Select 50GBASE-R PCS type 0 0 1 1 1 = Select 25GBASE-R PCS type 0 0 1 1 0 = Select 40GBASE-T PCS type 0 0 1 0 1 = Select 100GBASE-R PCS type 0 0 1 0 0 = Select 40GBASE-R PCS type 0 0 0 1 1 = Select 10GBASE-T PCS type 0 0 0 1 0 = Select 10GBASE-W PCS type 0 0 0 0 1 = Select 10GBASE-X PCS type 0 0 0 0 0 = Select 10GBASE-R PCS type	R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.7 PCS status 2 register (Register 3.8)

The assignment of bits in the PCS status 2 register is shown in Table 45–238. All the bits in the PCS status 2 register are read only; a write to the PCS status 2 register shall have no effect.

Table 45–238—PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
3.8.13	5GBASE-T capable	1 = PCS is able to support 5GBASE-T PCS type 0 = PCS is not able to support 5GBASE-T PCS type	RO
3.8.12	2.5GBASE-T capable	1 = PCS is able to support 2.5GBASE-T PCS type 0 = PCS is not able to support 2.5GBASE-T PCS type	RO
3.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
3.8.10	Receive fault	1 = Fault condition on the receive path 0 = No fault condition on the receive path	RO/LH

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Table 45–238—PCS status 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.8.9	25GBASE-T capable	1 = PCS is able to support 25GBASE-T PCS type 0 = PCS is not able to support 25GBASE-T PCS type	RO
3.8.8	50GBASE-R capable	1 = PCS is able to support 50GBASE-R PCS type 0 = PCS is not able to support 50GBASE-R PCS type	RO
3.8.7	25GBASE-R capable	1 = PCS is able to support 25GBASE-R PCS type 0 = PCS is not able to support 25GBASE-R PCS type	RO
3.8.6	40GBASE-T capable	1 = PCS is able to support 40GBASE-T PCS type 0 = PCS is not able to support 40GBASE-T PCS type	RO
3.8.5	100GBASE-R capable	1 = PCS is able to support 100GBASE-R PCS type 0 = PCS is not able to support 100GBASE-R PCS type	RO
3.8.4	40GBASE-R capable	1 = PCS is able to support 40GBASE-R PCS type 0 = PCS is not able to support 40GBASE-R PCS type	RO
3.8.3	10GBASE-T capable	1 = PCS is able to support 10GBASE-T PCS type 0 = PCS is not able to support 10GBASE-T PCS type	RO
3.8.2	10GBASE-W capable	1 = PCS is able to support 10GBASE-W PCS type 0 = PCS is not able to support 10GBASE-W PCS type	RO
3.8.1	10GBASE-X capable	1 = PCS is able to support 10GBASE-X PCS type 0 = PCS is not able to support 10GBASE-X PCS type	RO
3.8.0	10GBASE-R capable	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types	RO

[a]RO = Read only, LH = Latching high

45.2.3.7.1 Device present (3.8.15:14)

When read as <10>, bits 3.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 3.8.15:14 indicate that no device is present at this address or that the device is not functioning properly.

45.2.3.7.2 5GBASE-T capable (3.8.13)

When read as a one, bit 3.8.13 indicates that the PCS is able to support the 5GBASE-T PCS type. When read as a zero, bit 3.8.13 indicates that the PCS is not able to support the 5GBASE-T PCS type.

45.2.3.7.3 2.5GBASE-T capable (3.8.12)

When read as a one, bit 3.8.12 indicates that the PCS is able to support the 2.5GBASE-T PCS type. When read as a zero, bit 3.8.12 indicates that the PCS is not able to support the 2.5GBASE-T PCS type.

45.2.3.7.4 Transmit fault (3.8.11)

When read as a one, bit 3.8.11 indicates that the PCS has detected a fault condition on the transmit path. When read as a zero, bit 3.8.11 indicates that the PCS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

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The default value of bit 3.8.11 is zero.

45.2.3.7.5 Receive fault (3.8.10)

When read as a one, bit 3.8.10 indicates that the PCS has detected a fault condition on the receive path. When read as a zero, bit 3.8.10 indicates that the PCS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 3.8.10 is zero.

45.2.3.7.6 25GBASE-T capable (3.8.9)

When read as a one, bit 3.8.9 indicates that the PCS is able to support the 25GBASE-T PCS type. When read as a zero, bit 3.8.9 indicates that the PCS is not able to support the 25GBASE-T PCS type.

45.2.3.7.7 50GBASE-R capable (3.8.8)

When read as a one, bit 3.8.8 indicates that the PCS is able to support the 50GBASE-R PCS type. When read as a zero, bit 3.8.8 indicates that the PCS is not able to support the 50GBASE-R PCS type.

45.2.3.7.8 25GBASE-R capable (3.8.7)

When read as a one, bit 3.8.7 indicates that the PCS is able to support the 25GBASE-R PCS type. When read as a zero, bit 3.8.7 indicates that the PCS is not able to support the 25GBASE-R PCS type.

45.2.3.7.9 40GBASE-T capable (3.8.6)

When read as a one, bit 3.8.6 indicates that the PCS is able to support the 40GBASE-T PCS type. When read as a zero, bit 3.8.6 indicates that the PCS is not able to support the 40GBASE-T PCS type.

45.2.3.7.10 100GBASE-R capable (3.8.5)

When read as a one, bit 3.8.5 indicates that the PCS is able to support the 100GBASE-R PCS type. When read as a zero, bit 3.8.5 indicates that the PCS is not able to support the 100GBASE-R PCS type.

45.2.3.7.11 40GBASE-R capable (3.8.4)

When read as a one, bit 3.8.4 indicates that the PCS is able to support the 40GBASE-R PCS type. When read as a zero, bit 3.8.4 indicates that the PCS is not able to support the 40GBASE-R PCS type.

45.2.3.7.12 10GBASE-T capable (3.8.3)

When read as a one, bit 3.8.3 indicates that the PCS is able to support the 10GBASE-T PCS type. When read as a zero, bit 3.8.3 indicates that the PCS is not able to support the 10GBASE-T PCS type.

45.2.3.7.13 10GBASE-W capable (3.8.2)

When read as a one, bit 3.8.2 indicates that the 64B/66B PCS is able to support operation in a 10GBASE-W PHY (that is, supports operation with a WIS). When read as a zero, bit 3.8.2 indicates that the 64B/66B PCS is not able to support operation with a WIS in a 10GBASE-W PHY.

NOTE—This bit does not indicate that the PCS is performing the functionality contained in the WIS. This bit indicates whether the 64B/66B PCS would be able to support a WIS if it were to be attached.

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45.2.3.7.14 10GBASE-X capable (3.8.1)

When read as a one, bit 3.8.1 indicates that the PCS is able to support the 10GBASE-X PCS type. When read as a zero, bit 3.8.1 indicates that the PCS is not able to support the 10GBASE-X PCS type.

45.2.3.7.15 10GBASE-R capable (3.8.0)

When read as a one, bit 3.8.0 indicates that the PCS is able to support operation in a 10GBASE-R PHY. When read as a zero, bit 3.8.0 indicates that the PCS is not able to support operation in a 10GBASE-R PHY.

45.2.3.8 PCS status 3 register (Register 3.9)

The assignment of bits in the PCS status 3 register is shown in Table 45–239. All the bits in the PCS status 3 register are read only; a write to the PCS status 3 register shall have no effect.

Table 45–239—PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.9.15:8	Reserved	Value always 0	RO
3.9.7	25GBASE-PQ capable	1 = PCS is able to support 25GBASE-PQ PCS type 0 = PCS is not able to support 25GBASE-PQ PCS type	RO
3.9.6	25/10GBASE-PQ capable	1 = PCS is able to support25/10GBASE-PQ PCS type 0 = PCS is not able to support 25/10GBASE-PQ PCS type	RO
3.9.5	25GBASE-PQ Rx only capable	1 = PCS is able to support 25GBASE-PQ Rx only PCS type 0 = PCS is not able to support 25GBASE-PQ Rx only PCS type	RO
3.9.4	25GBASE-PQ Tx only capable	1 = PCS is able to support 25GBASE-PQ Tx only PCS type 0 = PCS is not able to support 25GBASE-PQ Tx only PCS type	RO
3.9.3	5GBASE-R capable	1 = PCS is able to support 5GBASE-R PCS type 0 = PCS is not able to support 5GBASE-R PCS type	RO
3.9.2	2.5GBASE-X capable	1 = PCS is able to support 2.5GBASE-X PCS type 0 = PCS is not able to support 2.5GBASE-X PCS type	RO
3.9.1	400GBASE-R capable	1 = PCS is able to support 400GBASE-R PCS type 0 = PCS is not able to support 400GBASE-R PCS type	RO
3.9.0	200GBASE-R capable	1 = PCS is able to support 200GBASE-R PCS type 0 = PCS is not able to support 200GBASE-R PCS type	RO

[a]RO = Read only

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45.2.3.8.1 25GBASE-PQ capable (3.9.7)

When read as a one, bit 3.9.7 indicates that the PCS is able to support the 25GBASE-PQ PCS type. When read as a zero, bit 3.9.7 indicates that the PCS is not able to support the 25GBASE-PQ PCS type.

45.2.3.8.2 25/10GBASE-PQ capable (3.9.6)

When read as a one, bit 3.9.6 indicates that the PCS is able to support the 25/10GBASE-PQ PCS type. When read as a zero, bit 3.9.6 indicates that the PCS is not able to support the 25/10GBASE-PQ PCS type.

45.2.3.8.3 25GBASE-PQ Rx only capable (3.9.5)

When read as a one, bit 3.9.5 indicates that the PCS is able to support the 25GBASE-PQ Rx only PCS type. When read as a zero, bit 3.9.5 indicates that the PCS is not able to support the 25GBASE-PQ Rx only PCS type.

45.2.3.8.4 25GBASE-PQ Tx only capable (3.9.4)

When read as a one, bit 3.9.4 indicates that the PCS is able to support the 25GBASE-PQ Tx only PCS type. When read as a zero, bit 3.9.4 indicates that the PCS is not able to support the 25GBASE-PQ Tx only PCS type.

45.2.3.8.5 5GBASE-R capable (3.9.3)

When read as a one, bit 3.9.3 indicates that the PCS is able to support the 5GBASE-R PCS type. When read as a zero, bit 3.9.3 indicates that the PCS is not able to support the 5GBASE-R PCS type.

45.2.3.8.6 2.5GBASE-X capable (3.9.2)

When read as a one, bit 3.9.2 indicates that the PCS is able to support operation in a 2.5GBASE-X PCS type. When read as a zero, bit 3.9.2 indicates that the PCS is not able to support operation in a 2.5GBASE-X PCS type.

45.2.3.8.7 400GBASE-R capable (3.9.1)

When read as a one, bit 3.9.1 indicates that the PCS is able to support the 400GBASE-R PCS type. When read as a zero, bit 3.9.1 indicates that the PCS is not able to support the 400GBASE-R PCS type.

45.2.3.8.8 200GBASE-R capable (3.9.0)

When read as a one, bit 3.9.0 indicates that the PCS is able to support the 200GBASE-R PCS type. When read as a zero, bit 3.9.0 indicates that the PCS is not able to support the 200GBASE-R PCS type.

45.2.3.9 PCS package identifier (Registers 3.14 and 3.15)

Registers 3.14 and 3.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PCS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PCS may return a value of zero in each of the 32 bits of the PCS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

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The format of the package identifier is specified in 22.2.4.3.1.

45.2.3.10 EEE control and capability 1 (Register 3.20)

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type. The assignment of bits in the EEE capability 1 register is shown in Table 45–240.

Table 45–240—EEE control and capability 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.20.15	Reserved	Value always 0	RO
3.20.14	50GBASE-R fast wake	1 = EEE fast wake is supported for 50GBASE-R 0 = EEE fast wake is not supported for 50GBASE-R	RO
3.20.13	100GBASE-R deep sleep	1 = EEE deep sleep is supported for 100GBASE-R 0 = EEE deep sleep is not supported for 100GBASE-R	RO
3.20.12	100GBASE-R fast wake	1 = EEE fast wake is supported for 100GBASE-R 0 = EEE fast wake is not supported for 100GBASE-R	RO
3.20.11	25GBASE-R deep sleep	1 = EEE deep sleep is supported for 25GBASE-R 0 = EEE deep sleep is not supported for 25GBASE-R	RO
3.20.10	25GBASE-R fast wake	1 = EEE fast wake is supported for 25GBASE-R 0 = EEE fast wake is not supported for 25GBASE-R	RO
3.20.9	40GBASE-R deep sleep	1 = EEE deep sleep is supported for 40GBASE-R 0 = EEE deep sleep is not supported for 40GBASE-R	RO
3.20.8	40GBASE-R fast wake	1 = EEE fast wake is supported for 40GBASE-R 0 = EEE fast wake is not supported for 40GBASE-R	RO
3.20.7	40GBASE-T EEE	1 = EEE is supported for 40GBASE-T 0 = EEE is not supported for 40GBASE-T	RO
3.20.6	10GBASE-KR EEE	1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR	RO
3.20.5	10GBASE-KX4 EEE	1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 10GBASE-KX4	RO
3.20.4	1000BASE-KX EEE	1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX	RO
3.20.3	10GBASE-T EEE	1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T	RO
3.20.2	1000BASE-T EEE	1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T	RO
3.20.1	100BASE-TX EEE	1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX	RO
3.20.0	LPI_FW	1 = Fast wake mode is used for LPI function 0 = Deep sleep is used for LPI function	R/W

[a]R/W = Read/Write, RO = Read only

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45.2.3.10.1 50GBASE-R EEE fast wake supported (3.20.14)

If the PCS supports EEE fast wake operation for 50GBASE-R, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.10.2 100GBASE-R EEE deep sleep supported (3.20.13)

If the PCS supports EEE deep sleep operation for 100GBASE-R, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.10.3 100GBASE-R EEE fast wake supported (3.20.12)

If the PCS supports EEE fast wake operation for 100GBASE-R, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.10.4 25GBASE-R deep sleep (3.20.11)

If the device supports EEE deep sleep operation for 25GBASE-R bit 3.20.11 shall be set to a one; otherwise this bit is set to a zero.

45.2.3.10.5 25GBASE-R fast wake (3.20.10)

If the device supports EEE fast wake operation for 25GBASE-R bit 3.20.10 shall be set to a one; otherwise this bit is set to a zero.

45.2.3.10.6 40GBASE-R EEE deep sleep supported (3.20.9)

If the PCS supports EEE deep sleep operation for 40GBASE-R, as defined in 78.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.10.7 40GBASE-R EEE fast wake supported (3.20.8)

If the PCS supports EEE fast wake operation for 40GBASE-R, as defined in 78.1, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.10.8 40GBASE-T EEE supported (3.20.7)

If the device supports EEE operation for 40GBASE-T as defined in 113.1.3.3, this bit shall be set to one.

45.2.3.10.9 10GBASE-KR EEE supported (3.20.6)

If the device supports EEE operation for 10GBASE-KR as defined in 72.1, this bit shall be set to one.

45.2.3.10.10 10GBASE-KX4 EEE supported (3.20.5)

If the device supports EEE operation for 10GBASE-KX4 as defined in 71.2, this bit shall be set to one.

45.2.3.10.11 1000BASE-KX EEE supported (3.20.4)

If the device supports EEE operation for 1000BASE-KX as defined in 70.1, this bit shall be set to one.

45.2.3.10.12 10GBASE-T EEE supported (3.20.3)

If the device supports EEE operation for 10GBASE-T as defined in 55.1.3.3, this bit shall be set to one.

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45.2.3.10.13 1000BASE-T EEE supported (3.20.2)

If the device supports EEE operation for 1000BASE-T as defined in 40.1.3, this bit shall be set to one.

45.2.3.10.14 100BASE-TX EEE supported (3.20.1)

If the device supports EEE operation for 100BASE-TX as defined in 24.1.1, this bit shall be set to one.

45.2.3.10.15 LPI_FW (3.20.0)

If the device supports fast wake as defined in 78.5, this bit selects fast wake or deep sleep operation. Setting 3.20.0 to one selects fast wake, setting to zero selects deep sleep. This bit is ignored by devices that do not support fast wake, and this bit defaults to one for devices that support fast wake.

45.2.3.11 EEE control and capability 2 (Register 3.21)

Register 3.21 extends register 3.20 and is used to indicate the capability of the PCS to support EEE functions for each PHY type. The assignment of bits in the EEE control and capability 2 register is shown in Table 45–241.

Table 45–241—EEE control and capability 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.21.15:9	Reserved	Value always 0	RO
3.21.8	5GBASE-KR EEE	1 = EEE is supported for 5GBASE-R 0 = EEE is not supported for 5GBASE-R	RO
3.21.7	2.5GBASE-KX EEE	1 = EEE is supported for 2.5GBASE-X 0 = EEE is not supported for 2.5GBASE-X	RO
3.21.6	Reserved	Value always 0	RO
3.21.5	400GBASE-R fast wake	1 = EEE fast wake is supported for 400GBASE-R 0 = EEE fast wake is not supported for 400GBASE-R	RO
3.21.4	Reserved	Value always 0	RO
3.21.3	200GBASE-R fast wake	1 = EEE fast wake is supported for 200GBASE-R 0 = EEE fast wake is not supported for 200GBASE-R	RO
3.21.2	25GBASE-T EEE	1 = EEE is supported for 25GBASE-T 0 = EEE is not supported for 25GBASE-T	RO
3.21.1	5GBASE-T EEE	1 = EEE is supported for 5GBASE-T 0 = EEE is not supported for 5GBASE-T	RO
3.21.0	2.5GBASE-T EEE	1 = EEE is supported for 2.5GBASE-T 0 = EEE is not supported for 2.5GBASE-T	RO

[a] RO = Read only

45.2.3.11.1 5GBASE-KR EEE supported (3.21.8)

If the device supports EEE operation for 5GBASE-KR as defined in 130.1, this bit shall be set to one.

45.2.3.11.2 2.5GBASE-KX EEE supported (3.21.7)

If the device supports EEE operation for 2.5GBASE-KX as defined in 128.1, this bit shall be set to one.

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45.2.3.11.3 400GBASE-R EEE fast wake supported (3.21.5)

If the PCS supports EEE fast wake operation for 400GBASE-R, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.11.4 200GBASE-R EEE fast wake supported (3.21.3)

If the PCS supports EEE fast wake operation for 200GBASE-R, this bit shall be set to a one; otherwise this bit shall be set to a zero.

45.2.3.11.5 25GBASE-T EEE supported (3.21.2)

If the device supports EEE operation for 25GBASE-T as defined in 113.1.3.3, this bit shall be set to one.

45.2.3.11.6 5GBASE-T EEE supported (3.21.1)

If the device supports EEE operation for 5GBASE-T as defined in 126.1.3.3, bit 3.21.1 shall be set to one.

45.2.3.11.7 2.5GBASE-T EEE supported (3.21.0)

If the device supports EEE operation for 2.5GBASE-T as defined in 126.1.3.3, bit 3.21.0 shall be set to one.

45.2.3.12 EEE wake error counter (Register 3.22)

This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and may occur during a refresh or a wake-up as defined by the PHY. This 16-bit counter shall be reset to all zeros when the EEE wake error counter is read by the management function or upon execution of the PCS reset. This counter shall be held at all ones in the case of overflow.

45.2.3.13 10GBASE-X PCS status register (Register 3.24)

The assignment of bits in the 10GBASE-X PCS status register is shown in Table 45–242. All the bits in the 10GBASE-X PCS status register are read only; a write to the 10GBASE-X PCS status register shall have no effect. A PCS device that does not implement 10GBASE-X shall return a zero for all bits in the 10GBASE-X PCS status register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–242—10GBASE-X PCS status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.24.15:13	Reserved	Value always 0	RO
3.24.12	10GBASE-X lane alignment status	1 = 10GBASE-X PCS receive lanes aligned 0 = 10GBASE-X PCS receive lanes not aligned	RO
3.24.11	Pattern testing ability	1 = 10GBASE-X PCS is able to generate test patterns 0 = 10GBASE-X PCS is not able to generate test patterns	RO
3.24.10:4	Reserved	Value always 0	RO

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Table 45–242—10GBASE-X PCS status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
3.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
3.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
3.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read only

45.2.3.13.1 10GBASE-X receive lane alignment status (3.24.12)

When read as a one, bit 3.24.12 indicates that the 10GBASE-X PCS has synchronized and aligned all four receive lanes. When read as a zero, bit 3.24.12 indicates that the 10GBASE-X PCS has not synchronized and aligned all four receive lanes.

45.2.3.13.2 Pattern testing ability (3.24.11)

When read as a one, bit 3.24.11 indicates that the 10GBASE-X PCS is able to generate test patterns. When read as a zero, bit 3.24.11 indicates that the 10GBASE-X PCS is not able to generate test patterns. If the 10GBASE-X PCS is able to generate test patterns, then the functionality is controlled using the transmit test-pattern enable bit in register 3.25.

45.2.3.13.3 Lane 3 sync (3.24.3)

When read as a one, bit 3.24.3 indicates that the 10GBASE-X PCS receive lane 3 is synchronized. When read as a zero, bit 3.24.3 indicates that the 10GBASE-X PCS receive lane 3 is not synchronized.

45.2.3.13.4 Lane 2 sync (3.24.2)

When read as a one, bit 3.24.2 indicates that the 10GBASE-X PCS receive lane 2 is synchronized. When read as a zero, bit 3.24.2 indicates that the 10GBASE-X PCS receive lane 2 is not synchronized.

45.2.3.13.5 Lane 1 sync (3.24.1)

When read as a one, bit 3.24.1 indicates that the 10GBASE-X PCS receive lane 1 is synchronized. When read as a zero, bit 3.24.1 indicates that the 10GBASE-X PCS receive lane 1 is not synchronized.

45.2.3.13.6 Lane 0 sync (3.24.0)

When read as a one, bit 3.24.0 indicates that the 10GBASE-X PCS receive lane 0 is synchronized. When read as a zero, bit 3.24.0 indicates that the 10GBASE-X PCS receive lane 0 is not synchronized.

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45.2.3.14 10GBASE-X PCS test control register (Register 3.25)

The assignment of bits in the 10GBASE-X PCS test control register is shown in Table 45–243. The default value for each bit of the 10GBASE-X PCS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–243—10GBASE-X PCS test control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.25.15:3	Reserved	Value always 0	RO
3.25.2	Transmit test-pattern enable	1 = Transmit test pattern enabled 0 = Transmit test pattern not enabled	R/W
3.25.1:0	Test pattern select	1 0 1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.14.1 Transmit test-pattern enable (3.25.2)

When bit 3.25.2 is set to a one, pattern testing is enabled on the transmit path. When bit 3.25.2 is set to a zero, pattern testing is disabled on the transmit path. Pattern testing is optional, and the ability of the 10GBASE-X PCS to generate test patterns is advertised by the pattern testing ability bit in register 3.24. A 10GBASE-X PCS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 3.25.2 is zero.

45.2.3.14.2 Test pattern select (3.25.1:0)

The test pattern to be used when pattern testing is enabled using bit 3.25.2 is selected using bits 3.25.1:0. When bits 3.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 3.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 3.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

45.2.3.15 BASE-R and MultiGBASE-T PCS status 1 register (Register 3.32)

The assignment of bits in the BASE-R and MultiGBASE-T PCS status 1 register is shown in Table 45–244. All the bits in the BASE-R and MultiGBASE-T PCS status 1 register are read only; a write to the BASE-R and MultiGBASE-T PCS status 1 register shall have no effect. A PCS device that implements neither BASE-R nor any member of the MultiGBASE-T set shall return a zero for all bits in the BASE-R and MultiGBASE-T PCS status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.32 are undefined when the BASE-R or MultiGBASE-T PCS is operating in seed test-pattern mode, PRBS31 test-pattern mode, or PRBS9 test-pattern mode.

45.2.3.15.1 BASE-R and MultiGBASE-T receive link status (3.32.12)

When read as a one, bit 3.32.12 indicates that the PCS is in a fully operational state. When read as a zero, bit 3.32.12 indicates that the PCS is not fully operational. This bit is a reflection of the PCS_status variable

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Table 45–244—BASE-R and MultiGBASE-T PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.32.15:13	Reserved	Value always 0	RO
3.32.12	BASE-R and MultiGBASE-T receive link status	1 = BASE-R or any MultiGBASE-T PCS receive link up 0 = BASE-R or any MultiGBASE-T PCS receive link down	RO
3.32.11:4	Reserved	Value always 0	RO
3.32.3	10GBASE-R PRBS9 pattern testing ability	1 = PCS is able to support PRBS9 pattern testing 0 = PCS is not able to support PRBS9 pattern testing	RO
3.32.2	10GBASE-R PRBS31 pattern testing ability	1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 pattern testing	RO
3.32.1	BASE-R and MultiGBASE-T PCS high BER	1 = BASE-R or any MultiGBASE-T PCS reporting a high BER 0 = BASE-R or any MultiGBASE-T PCS not reporting a high BER	RO
3.32.0	BASE-R and MultiGBASE-T PCS block lock	1 = BASE-R or any MultiGBASE-T PCS locked to received blocks 0 = BASE-R or any MultiGBASE-T PCS not locked to received blocks	RO

[a]RO = Read only

defined in 49.2.14.1 for 5/10/25GBASE-R, in 126.3.7.1 for 2.5GBASE-T and 5GBASE-T, in 55.3.7.1 for 10GBASE-T, in 113.3.7.1 for 25GBASE-T and 40GBASE-T, in 82.3.1 for 40/50/100GBASE-R, and in 119.3 for 200/400GBASE-R.

45.2.3.15.2 PRBS9 pattern testing ability (3.32.3)

When read as a one, bit 3.32.3 indicates that the PCS is able to support PRBS9 pattern testing of its transmitter. When read as a zero, bit 3.32.3 indicates that the PCS is not able to support PRBS9 pattern testing of its transmitter. If the PCS is able to support PRBS9 pattern testing of its transmitter then the pattern generation is controlled using bit 3.42.6.

45.2.3.15.3 PRBS31 pattern testing ability (3.32.2)

When read as a one, bit 3.32.2 indicates that the PCS is able to support PRBS31 pattern testing. When read as a zero, bit 3.32.2 indicates that the PCS is not able to support PRBS31 pattern testing. If the PCS is able to support PRBS31 pattern testing then the pattern generation and checking is controlled using bits 3.42.5:4.

45.2.3.15.4 BASE-R and MultiGBASE-T PCS high BER (3.32.1)

For BASE-R, when read as a one, bit 3.32.1 indicates that the 64B/66B receiver is detecting a BER of $\geq 10^{-4}$. When read as a zero, bit 3.32.1 indicates that the 64B/66B receiver is detecting a BER of $< 10^{-4}$. This bit is a direct reflection of the state of the hi_ber variable in the BER monitor state diagrams as defined in 49.2.13.2.2 for 5/10/25GBASE-R and in 82.2.19.2.2 for 40/50/100GBASE-R.

For any member of the MultiGBASE-T set, when read as a one, bit 3.32.1 indicates that the 64B/65B receiver is detecting a BER of $\geq 10^{-4}$. When read as a zero, bit 3.32.1 indicates that the 64B/65B receiver is

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detecting a BER of $< 10^{-4}$. This bit is a direct reflection of the state of the hi_lfer variable in the LFER monitor state diagrams as defined in 126.3.6.2.2 for 2.5GBASE-T and 5GBASE-T, in 55.3.6.2.2 for 10GBASE-T, and in 113.3.6.2.2 for 25GBASE-T and 40GBASE-T.

45.2.3.15.5 BASE-R and MultiGBASE-T PCS block lock (3.32.0)

When read as a one, bit 3.32.0 indicates that the 64B/66B receiver for BASE-R or the 64B/65B receiver for a member of the MultiGBASE-T set has block lock. When read as a zero, bit 3.32.0 indicates that the 64B/66B receiver for BASE-R or the 64B/65B receiver for the member of the MultiGBASE-T set has not achieved block lock. For a 5/10/25GBASE-R PCS, this bit is a direct reflection of the state of the block_lock variable defined in 49.2.13.2.2. For a 40/50/100GBASE-R PCS, this bit reflects the logical AND of the state of the block_lock<x> variables defined in 82.2.19.2.2. For a MultiGBASE-R PCS, this bit is a direct reflection of the state of the block_lock variable defined in 126.3.6.2.2 for 2.5GBASE-T and 5GBASE-T, in 55.3.2.3 for 10GBASE-T, and in 113.3.6.2.2 for 25GBASE-T and 40GBASE-T. For a multi-lane PCS, this bit indicates that the receiver has both block lock and alignment for all lanes and is identical to 3.50.12 (see 45.2.3.23.1).

45.2.3.16 BASE-R and MultiGBASE-T PCS status 2 register (Register 3.33)

The assignment of bits in the BASE-R and MultiGBASE-T PCS status 2 register is shown in Table 45–245. All the bits in the BASE-R and MultiGBASE-T PCS status 2 register are read only; a write to the BASE-R and MultiGBASE-T PCS status 2 register shall have no effect. A PCS device that implements neither BASE-R nor any member of the MultiGBASE-T set shall return a zero for all bits in the BASE-R and MultiGBASE-T PCS status 2 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.33 are undefined when the BASE-R or the MultiGBASE-T set PCS is operating seed test-pattern mode, PRBS31 test-pattern mode, or PRBS9 test-pattern mode.

Table 45–245—BASE-R and MultiGBASE-T PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.33.15	Latched block lock	1 = BASE-R or any MultiGBASE-T PCS has block lock 0 = BASE-R or any MultiGBASE-T PCS does not have block lock	RO/LL
3.33.14	Latched high BER	1 = BASE-R or any MultiGBASE-T PCS has reported a high BER 0 = BASE-R or any MultiGBASE-T PCS has not reported a high BER	RO/LH
3.33.13:8	BER	BER counter	RO/NR
3.33.7:0	Errored blocks	Errored blocks counter	RO/NR

[a]RO = Read only, LL = Latching low, LH = Latching high, NR = Non Roll-over

45.2.3.16.1 Latched block lock (3.33.15)

When read as a one, bit 3.33.15 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has achieved block lock. When read as a zero, bit 3.33.15 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has lost block lock.

The latched block lock bit shall be implemented with latching low behavior.

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This bit is a latching low version of the 5/10/25/40/50/100GBASE-R and MultiGBASE-T PCS block lock status bit (3.32.0).

45.2.3.16.2 Latched high BER (3.33.14)

When read as a one, bit 3.33.14 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has detected a high BER. When read as a zero, bit 3.33.14 indicates that the 5/10/25/40/50/100GBASE-R or a member of the MultiGBASE-T set PCS has not detected a high BER.

The latched high BER bit shall be implemented with latching high behavior.

This bit is a latching high version of the 5/10/25/40/50/100GBASE-R and MultiGBASE-T PCS high BER status bit (3.32.1).

45.2.3.16.3 BER (3.33.13:8)

The BER counter is a six bit count as defined by the ber_count variable in 49.2.14.2 and 82.2.19.2.4 for 5/10/25/40/50/100GBASE-R and defined by counter lfer_count in 126.3.7.2 for 2.5GBASE-T and 5GBASE-T, in 55.3.7.2 for 10GBASE-T, and in 113.3.7.2 for 25GBASE-T and 40GBASE-T. These bits shall be reset to all zeros when the BASE-R and MultiGBASE-T PCS status 2 register is read by the management function or upon execution of the PCS reset. If the BER high order counter, 3.44 (see 45.2.3.21) is not implemented then these bits shall be held at all ones in the case of overflow.

45.2.3.16.4 Errored blocks (3.33.7:0)

The errored blocks counter is an eight bit count defined by the counter errored_block_count specified in 49.2.14.2 for 5/10/25GBASE-R, in 82.3.1 for 40/50/100GBASE-R, in 126.3.7.2 for 2.5GBASE-T and 5GBASE-T, in 55.3.7.2 for 10GBASE-T, and in 113.3.7.2 for 25GBASE-T and 40GBASE-T. These bits shall be reset to all zeros when the errored blocks count is read by the management function or upon execution of the PCS reset. If the Errored blocks high order counter, 3.45 (see 45.2.3.22) is not implemented then these bits shall be held at all ones in the case of overflow.

45.2.3.17 5/10/25GBASE-R PCS test pattern seed A (Registers 3.34 through 3.37)

The assignment of bits in the 5/10/25GBASE-R PCS test pattern seed A registers is shown in Table 45–246. This register is only required when the 5GBASE-R, 10GBASE-R, or 25GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. For each seed register, seed bits are assigned to register bits in order with the lowest numbered seed bit for that register being assigned to register bit 0.

Table 45–246—5/10/25GBASE-R PCS test pattern seed A 0-3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.37.15:10	Reserved	Value always 0	RO
3.37.9:0	Test pattern seed A 3	Test pattern seed A bits 48-57	R/W
3.36.15:0	Test pattern seed A 2	Test pattern seed A bits 32-47	R/W

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Table 45–246—5/10/25GBASE-R PCS test pattern seed A 0-3 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.35.15:0	Test pattern seed A 1	Test pattern seed A bits 16-31	R/W
3.34.15:0	Test pattern seed A 0	Test pattern seed A bits 0-15	R/W

[a]RO = Read only, R/W = Read/Write

The A seed for the pseudo random test pattern is held in registers 3.34 through 3.37. The test-pattern methodology is described in 49.2.8.

45.2.3.18 5/10/25GBASE-R PCS test pattern seed B (Registers 3.38 through 3.41)

The assignment of bits in the 5/10/25GBASE-R PCS test pattern seed B registers is shown in Table 45–247. This register is only required when the 5GBASE-R, 10GBASE-R, or 25GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. For each seed register, seed bits are assigned to register bits in order with the lowest numbered seed bit for that register being assigned to register bit 0.

Table 45–247—5/10/25GBASE-R PCS test pattern seed B 0-3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.41.15:10	Reserved	Value always 0	RO
3.41.9:0	Test pattern seed B 3	Test pattern seed B bits 48-57	R/W
3.40.15:0	Test pattern seed B 2	Test pattern seed B bits 32-47	R/W
3.39.15:0	Test pattern seed B 1	Test pattern seed B bits 16-31	R/W
3.38.15:0	Test pattern seed B 0	Test pattern seed B bits 0-15	R/W

[a]RO = Read only, R/W = Read/Write

The B seed for the pseudo random test pattern is held in registers 3.38 through 3.41. The test-pattern methodology is described in 49.2.8.

45.2.3.19 BASE-R PCS test-pattern control register (Register 3.42)

The assignment of bits in the BASE-R PCS test-pattern control register is shown in Table 45–248. This register is only required when the BASE-R capability is supported. If both BASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for BASE-R. PRBS9, PRBS31, pseudo random, and square wave test patterns are defined for 10GBASE-R PCS only. Scrambled idle test patterns are defined for 25/40/50/100/200/400GBASE-R PCS only. The test-pattern methodology is described in 49.2.8 and 82.2.11.

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Table 45–248—BASE-R PCS test-pattern control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.42.15:8	Reserved	Value always 0	RO
3.42.7	Scrambled idle test-pattern enable	1 = Enable scrambled idle test-pattern mode 0 = Disable scrambled idle test-pattern mode	R/W
3.42.6	Single Lane PHY BASE-R PRBS9 transmit test-pattern enable	1 = Enable PRBS9 test-pattern mode on the transmit path 0 = Disable PRBS9 test-pattern mode on the transmit path	R/W
3.42.5	Single Lane PHY BASE-R PRBS31 receive test-pattern enable	1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path	R/W
3.42.4	Single Lane PHY BASE-R PRBS31 transmit test-pattern enable	1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path	R/W
3.42.3	Transmit test-pattern enable	1 = Enable transmit test pattern 0 = Disable transmit test pattern	R/W
3.42.2	Receive test-pattern enable	1 = Enable receive test-pattern testing 0 = Disable receive test-pattern testing	R/W
3.42.1	Test-pattern select	1 = Square wave test pattern 0 = Pseudo random test pattern	R/W
3.42.0	Data pattern select	1 = Zeros data pattern 0 = LF data pattern	R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.19.1 Scrambled idle test-pattern enable (3.42.7)

When bit 3.42.7 is set to a one, scrambled idle pattern testing is enabled. When bit 3.42.7 is set to zero, scrambled idle pattern testing is disabled.

The default value for bit 3.42.3 is zero.

45.2.3.19.2 Single Lane PHY BASE-R PRBS9 transmit test-pattern enable (3.42.6)

If the PCS supports the optional PRBS9 pattern testing (indicated by bit 3.32.3), the mandatory transmit test-pattern enable bit (3.42.3) is not one, and the optional PRBS31 transmit test-pattern enable bit (3.42.4) is not one, then when bit 3.42.6 is set to one the PCS shall transmit PRBS9. When bit 3.42.6 is set to zero, the PCS shall not generate PRBS9. The PRBS9 test-pattern is specified in 68.6.1. The behavior of the PCS when in PRBS9 test-pattern mode is specified in Clause 49.

45.2.3.19.3 Single Lane PHY BASE-R PRBS31 receive test-pattern enable (3.42.5)

If the PCS supports the optional PRBS31 pattern testing advertised in bit 3.32.2 and the mandatory receive test-pattern enable bit (3.42.2) is not one, setting bit 3.42.5 to a one shall set the receive path of the PCS into the PRBS31 test-pattern mode. The number of errors received during a PRBS31 pattern test are recorded in register 3.43. Setting bit 3.42.5 to a zero shall disable the PRBS31 test-pattern mode on the receive path of the PCS. The behavior of the PCS when in PRBS31 test-pattern mode is specified in Clause 49.

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45.2.3.19.4 Single Lane PHY BASE-R PRBS31 transmit test-pattern enable (3.42.4)

If the PCS supports the optional PRBS31 pattern testing advertised in bit 3.32.2 and the mandatory transmit test-pattern enable bit (3.42.3) is not one, then setting bit 3.42.4 to a one shall set the transmit path of the PCS into the PRBS31 test-pattern mode. Setting bit 3.42.4 to a zero shall disable the PRBS31 test-pattern mode on the transmit path of the PCS. The behavior of the PCS when in PRBS31 test-pattern mode is specified in Clause 49.

45.2.3.19.5 Transmit test-pattern enable (3.42.3)

When bit 3.42.3 is set to a one, pattern testing is enabled on the transmit path. When bit 3.42.3 is set to a zero, pattern testing is disabled on the transmit path.

The default value for bit 3.42.3 is zero.

45.2.3.19.6 Receive test-pattern enable (3.42.2)

When bit 3.42.2 is set to a one, pattern testing is enabled on the receive path. When bit 3.42.2 is set to a zero, pattern testing is disabled on the receive path.

The default value for bit 3.42.2 is zero.

45.2.3.19.7 Test-pattern select (3.42.1)

When bit 3.42.1 is set to a one, the square wave test pattern is used for pattern testing. When bit 3.42.1 is set to a zero, the pseudo random test pattern is used for pattern testing.

The default value for bit 3.42.1 is zero.

45.2.3.19.8 Data pattern select (3.42.0)

When bit 3.42.0 is set to a one, the zeros data pattern is used for pattern testing. When bit 3.42.0 is set to a zero, the LF data pattern is used for pattern testing.

The default value for bit 3.42.0 is zero.

45.2.3.20 BASE-R PCS test-pattern error counter register (Register 3.43)

The assignment of bits in the BASE-R PCS test-pattern error counter register is shown in Table 45–249. This register is only required when the BASE-R capability is supported. If both BASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode, or may function as defined for BASE-R.

Table 45–249—BASE-R PCS test-pattern error counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.43.15:0	Test-pattern error counter	Error counter	RO

[a]RO = Read only

The test-pattern error counter is a sixteen bit counter that contains the number of errors received during a pattern test. These bits shall be reset to all zeros when the test-pattern error counter is read by the

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management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow. The test-pattern methodology is described in 49.2.12 and 82.2.11. This counter will count either block errors or bit errors dependent on the test mode (see 49.2.12).

45.2.3.21 BER high order counter (Register 3.44)

The assignment of bits in the BER high order counter register is shown in Table 45–250. This register is mandatory when the 40/100GBASE-R capability is supported and optional for other PHY types that implement register 3.33.

Table 45–250—BER high order counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.44.15:0	BER high order	Bits 21:6 of BER counter	RO

[a]RO = Read only

Bits 15:0 of this register are concatenated with bits 13:8 of register 3.33 (see 45.2.3.16) to read the value of a twenty-two bit BER counter. When registers 3.44 and 3.33 are used to read the 22-bit counter value, the register 3.33 is read first (indicating the lower 6 bits). The remaining 16 bits shall be latched when register 3.33 is read and reads to register 3.44 return the latched value. The counter continues to function as defined in 45.2.3.16.3 regardless of the state of the latched register. The 22-bit counter shall be reset to all zeros when register 3.33 is read or upon PCS reset. The 22-bit counter shall be held at all ones in the case of overflow.

45.2.3.22 Errored blocks high order counter (Register 3.45)

The assignment of bits in the Errored blocks high order counter register is shown in Table 45–251. This register is mandatory when the 40/100GBASE-R capability is supported and optional for other PHY types that implement register 3.33. If this register is implemented then bit 3.45.15 shall be set to one.

Table 45–251—Errored blocks high order counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.45.15	High order counter present	Always reads as one if this register is implemented	RO
3.45.14	Reserved	Value always 0	RO
3.45.13:0	Errored blocks high order	Bits 21:8 of errored blocks counter	RO

[a]RO = Read only

Bits 13:0 of this register are concatenated with bits 7:0 of register 3.33 (see 45.2.3.16) to read the value of a twenty-two bit errored blocks counter. When registers 3.45 and 3.33 are used to read the 22-bit counter value, the register 3.33 is read first (indicating the lower 8 bits). The remaining 14 bits shall be latched when register 3.33 is read and reads to register 3.45 return the latched value. The counter continues to function as defined in 45.2.3.16.4 regardless of the state of the latched register. The 22-bit counter shall be reset to all zeros when register 3.33 is read or upon PCS reset. The 22-bit counter shall be held at all ones in the case of overflow.

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45.2.3.23 Multi-lane BASE-R PCS alignment status 1 register (Register 3.50)

The assignment of bits in the multi-lane BASE-R PCS alignment status 1 register is shown in Table 45–252. All the bits in the multi-lane BASE-R PCS alignment status 1 register are read only; a write to the multi-lane BASE-R PCS alignment status 1 register shall have no effect. A PCS device that does not implement multi-lane BASE-R PCS shall return a zero for all bits in the multi-lane BASE-R PCS alignment status 1 register. A device that implements multi-lane BASE-R PCS shall return a zero for all bits in the multi-lane BASE-R PCS alignment status 1 register that are not required for the PCS configuration. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–252—Multi-lane BASE-R PCS alignment status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.50.15:13	Reserved	Value always 0	RO
3.50.12	PCS lane alignment status	1 = PCS receive lanes locked and aligned 0 = PCS receive lanes not locked and aligned	RO
3.50.11:8	Reserved	Value always 0	RO
3.50.7	Block lock 7	1 = Lane 7 is locked 0 = Lane 7 is not locked	RO
3.50.6	Block lock 6	1 = Lane 6 is locked 0 = Lane 6 is not locked	RO
3.50.5	Block lock 5	1 = Lane 5 is locked 0 = Lane 5 is not locked	RO
3.50.4	Block lock 4	1 = Lane 4 is locked 0 = Lane 4 is not locked	RO
3.50.3	Block lock 3	1 = Lane 3 is locked 0 = Lane 3 is not locked	RO
3.50.2	Block lock 2	1 = Lane 2 is locked 0 = Lane 2 is not locked	RO
3.50.1	Block lock 1	1 = Lane 1 is locked 0 = Lane 1 is not locked	RO
3.50.0	Block lock 0	1 = Lane 0 is locked 0 = Lane 0 is not locked	RO

[a]RO = Read only

45.2.3.23.1 Multi-lane BASE-R PCS alignment status (3.50.12)

When read as a one, bit 3.50.12 indicates that the PCS has locked and aligned all receive lanes. When read as a zero, bit 3.50.12 indicates that the PCS has not locked and aligned all receive lanes.

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45.2.3.23.2 Block lock 7 (3.50.7)

When read as a one, bit 3.50.7 indicates that the PCS receiver has achieved block lock for service interface lane 7. When read as a zero, bit 3.50.7 indicates that the PCS receiver lane 7 has not achieved block lock. This bit reflects the state of block_lock[7] (see 82.2.19.2.2).

45.2.3.23.3 Block lock 6 (3.50.6)

When read as a one, bit 3.50.6 indicates that the PCS receiver has achieved block lock for service interface lane 6. When read as a zero, bit 3.50.6 indicates that the PCS receiver lane 6 has not achieved block lock. This bit reflects the state of block_lock[6] (see 82.2.19.2.2).

45.2.3.23.4 Block lock 5 (3.50.5)

When read as a one, bit 3.50.5 indicates that the PCS receiver has achieved block lock for service interface lane 5. When read as a zero, bit 3.50.5 indicates that the PCS receiver lane 5 has not achieved block lock. This bit reflects the state of block_lock[5] (see 82.2.19.2.2).

45.2.3.23.5 Block lock 4 (3.50.4)

When read as a one, bit 3.50.4 indicates that the PCS receiver has achieved block lock for service interface lane 4. When read as a zero, bit 3.50.4 indicates that the PCS receiver lane 4 has not achieved block lock. This bit reflects the state of block_lock[4] (see 82.2.19.2.2).

45.2.3.23.6 Block lock 3 (3.50.3)

When read as a one, bit 3.50.3 indicates that the PCS receiver has achieved block lock for service interface lane 3. When read as a zero, bit 3.50.3 indicates that the PCS receiver lane 3 has not achieved block lock. This bit reflects the state of block_lock[3] (see 82.2.19.2.2).

45.2.3.23.7 Block lock 2 (3.50.2)

When read as a one, bit 3.50.2 indicates that the PCS receiver has achieved block lock for service interface lane 2. When read as a zero, bit 3.50.2 indicates that the PCS receiver lane 2 has not achieved block lock. This bit reflects the state of block_lock[2] (see 82.2.19.2.2).

45.2.3.23.8 Block lock 1 (3.50.1)

When read as a one, bit 3.50.1 indicates that the PCS receiver has achieved block lock for service interface lane 1. When read as a zero, bit 3.50.1 indicates that the PCS receiver lane 1 has not achieved block lock. This bit reflects the state of block_lock[1] (see 82.2.19.2.2).

45.2.3.23.9 Block lock 0 (3.50.0)

When read as a one, bit 3.50.0 indicates that the PCS receiver has achieved block lock for service interface lane 0. When read as a zero, bit 3.50.0 indicates that the PCS receiver lane 0 has not achieved block lock. This bit reflects the state of block_lock[0] (see 82.2.19.2.2).

45.2.3.24 Multi-lane BASE-R PCS alignment status 2 register (Register 3.51)

The assignment of bits in the multi-lane BASE-R PCS alignment status 2 register is shown in Table 45–253. All the bits in the multi-lane BASE-R PCS alignment status 2 register are read only; a write to the multi-lane BASE-R PCS alignment status 2 register shall have no effect. A PCS device that does not implement multi-lane BASE-R PCS shall return a zero for all bits in the multi-lane BASE-R PCS alignment status 2

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register. A device that implements multi-lane BASE-R PCS shall return a zero for all bits in the multi-lane BASE-R PCS alignment status 2 register that are not required for the PCS configuration. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–253—Multi-lane BASE-R PCS alignment status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.51.15:12	Reserved	Value always 0	RO
3.51.11	Block lock 19	1 = Lane 19 is locked 0 = Lane 19 is not locked	RO
3.51.10	Block lock 18	1 = Lane 18 is locked 0 = Lane 18 is not locked	RO
3.51.9	Block lock 17	1 = Lane 17 is locked 0 = Lane 17 is not locked	RO
3.51.8	Block lock 16	1 = Lane 16 is locked 0 = Lane 16 is not locked	RO
3.51.7	Block lock 15	1 = Lane 15 is locked 0 = Lane 15 is not locked	RO
3.51.6	Block lock 14	1 = Lane 14 is locked 0 = Lane 14 is not locked	RO
3.51.5	Block lock 13	1 = Lane 13 is locked 0 = Lane 13 is not locked	RO
3.51.4	Block lock 12	1 = Lane 12 is locked 0 = Lane 12 is not locked	RO
3.51.3	Block lock 11	1 = Lane 11 is locked 0 = Lane 11 is not locked	RO
3.51.2	Block lock 10	1 = Lane 10 is locked 0 = Lane 10 is not locked	RO
3.51.1	Block lock 9	1 = Lane 9 is locked 0 = Lane 9 is not locked	RO
3.51.0	Block lock 8	1 = Lane 8 is locked 0 = Lane 8 is not locked	RO

[a]RO = Read only

45.2.3.24.1 Block lock 19 (3.51.11)

When read as a one, bit 3.51.11 indicates that the PCS receiver has achieved block lock for service interface lane 19. When read as a zero, bit 3.51.11 indicates that the PCS receiver lane 19 has not achieved block lock. This bit reflects the state of block_lock[19] (see 82.2.19.2.2).

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45.2.3.24.2 Block lock 18 (3.51.10)

When read as a one, bit 3.51.10 indicates that the PCS receiver has achieved block lock for service interface lane 18. When read as a zero, bit 3.51.10 indicates that the PCS receiver lane 18 has not achieved block lock This bit reflects the state of block_lock[18] (see 82.2.19.2.2).

45.2.3.24.3 Block lock 17 (3.51.9)

When read as a one, bit 3.51.9 indicates that the PCS receiver has achieved block lock for service interface lane 17. When read as a zero, bit 3.51.9 indicates that the PCS receiver lane 17 has not achieved block lock This bit reflects the state of block_lock[17] (see 82.2.19.2.2).

45.2.3.24.4 Block lock 16 (3.51.8)

When read as a one, bit 3.51.8 indicates that the PCS receiver has achieved block lock for service interface lane 16. When read as a zero, bit 3.51.8 indicates that the PCS receiver lane 16 has not achieved block lock This bit reflects the state of block_lock[16] (see 82.2.19.2.2).

45.2.3.24.5 Block lock 15 (3.51.7)

When read as a one, bit 3.51.7 indicates that the PCS receiver has achieved block lock for service interface lane 15. When read as a zero, bit 3.51.7 indicates that the PCS receiver lane 15 has not achieved block lock This bit reflects the state of block_lock[15] (see 82.2.19.2.2).

45.2.3.24.6 Block lock 14 (3.51.6)

When read as a one, bit 3.51.6 indicates that the PCS receiver has achieved block lock for service interface lane 14. When read as a zero, bit 3.51.6 indicates that the PCS receiver lane 14 has not achieved block lock This bit reflects the state of block_lock[14] (see 82.2.19.2.2).

45.2.3.24.7 Block lock 13 (3.51.5)

When read as a one, bit 3.51.5 indicates that the PCS receiver has achieved block lock for service interface lane 13. When read as a zero, bit 3.51.5 indicates that the PCS receiver lane 13 has not achieved block lock This bit reflects the state of block_lock[13] (see 82.2.19.2.2).

45.2.3.24.8 Block lock 12 (3.51.4)

When read as a one, bit 3.51.4 indicates that the PCS receiver has achieved block lock for service interface lane 12. When read as a zero, bit 3.51.4 indicates that the PCS receiver lane 12 has not achieved block lock This bit reflects the state of block_lock[12] (see 82.2.19.2.2).

45.2.3.24.9 Block lock 11 (3.51.3)

When read as a one, bit 3.51.3 indicates that the PCS receiver has achieved block lock for service interface lane 11. When read as a zero, bit 3.51.3 indicates that the PCS receiver lane 11 has not achieved block lock This bit reflects the state of block_lock[11] (see 82.2.19.2.2).

45.2.3.24.10 Block lock 10 (3.51.2)

When read as a one, bit 3.51.2 indicates that the PCS receiver has achieved block lock for service interface lane 10. When read as a zero, bit 3.51.2 indicates that the PCS receiver lane 10 has not achieved block lock This bit reflects the state of block_lock[10] (see 82.2.19.2.2).

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45.2.3.24.11 Block lock 9 (3.51.1)

When read as a one, bit 3.51.1 indicates that the PCS receiver has achieved block lock for service interface lane 9. When read as a zero, bit 3.51.1 indicates that the PCS receiver lane 9 has not achieved block lock This bit reflects the state of block_lock[9] (see 82.2.19.2.2).

45.2.3.24.12 Block lock 8 (3.51.0)

When read as a one, bit 3.51.0 indicates that the PCS receiver has achieved block lock for service interface lane 8. When read as a zero, bit 3.51.0 indicates that the PCS receiver lane 8 has not achieved block lock This bit reflects the state of block_lock[8] (see 82.2.19.2.2).

45.2.3.25 Multi-lane BASE-R PCS alignment status 3 register (Register 3.52)

The assignment of bits in the multi-lane BASE-R PCS alignment status 3 register is shown in Table 45–254. All the bits in the multi-lane BASE-R PCS alignment status 3 register are read only; a write to the multi-lane BASE-R PCS alignment status 3 register shall have no effect. A PCS device that does not implement multi-lane BASE-R PCS shall return a zero for all bits in the multi-lane BASE-R PCS alignment status 3 register. A device that implements multi-lane BASE-R PCS shall return a zero for all bits in the multi-lane BASE-R PCS alignment status 3 register that are not required for the PCS configuration. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–254—Multi-lane BASE-R PCS alignment status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.52.15:8	Reserved	Value always 0	RO
3.52.7	Lane 7 aligned	1 = Lane 7 alignment marker is locked 0 = Lane 7 alignment marker is not locked	RO
3.52.6	Lane 6 aligned	1 = Lane 6 alignment marker is locked 0 = Lane 6 alignment marker is not locked	RO
3.52.5	Lane 5 aligned	1 = Lane 5 alignment marker is locked 0 = Lane 5 alignment marker is not locked	RO
3.52.4	Lane 4 aligned	1 = Lane 4 alignment marker is locked 0 = Lane 4 alignment marker is not locked	RO
3.52.3	Lane 3 aligned	1 = Lane 3 alignment marker is locked 0 = Lane 3 alignment marker is not locked	RO
3.52.2	Lane 2 aligned	1 = Lane 2 alignment marker is locked 0 = Lane 2 alignment marker is not locked	RO
3.52.1	Lane 1 aligned	1 = Lane 1 alignment marker is locked 0 = Lane 1 alignment marker is not locked	RO
3.52.0	Lane 0 aligned	1 = Lane 0 alignment marker is locked 0 = Lane 0 alignment marker is not locked	RO

[a]RO = Read only

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45.2.3.25.1 Lane 7 aligned (3.52.7)

When read as a one, bit 3.52.7 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 7. When read as a zero, bit 3.52.7 indicates that the PCS receiver lane 7 has not achieved alignment marker lock. This bit reflects the state of am_lock[7] (see 82.2.19.2.2).

45.2.3.25.2 Lane 6 aligned (3.52.6)

When read as a one, bit 3.52.6 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 6. When read as a zero, bit 3.52.6 indicates that the PCS receiver lane 6 has not achieved alignment marker lock. This bit reflects the state of am_lock[6] (see 82.2.19.2.2).

45.2.3.25.3 Lane 5 aligned (3.52.5)

When read as a one, bit 3.52.5 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 5. When read as a zero, bit 3.52.5 indicates that the PCS receiver lane 5 has not achieved alignment marker lock. This bit reflects the state of am_lock[5] (see 82.2.19.2.2).

45.2.3.25.4 Lane 4 aligned (3.52.4)

When read as a one, bit 3.52.4 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 4. When read as a zero, bit 3.52.4 indicates that the PCS receiver lane 4 has not achieved alignment marker lock. This bit reflects the state of am_lock[4] (see 82.2.19.2.2).

45.2.3.25.5 Lane 3 aligned (3.52.3)

When read as a one, bit 3.52.3 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 3. When read as a zero, bit 3.52.3 indicates that the PCS receiver lane 3 has not achieved alignment marker lock. This bit reflects the state of am_lock[3] (see 82.2.19.2.2).

45.2.3.25.6 Lane 2 aligned (3.52.2)

When read as a one, bit 3.52.2 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 2. When read as a zero, bit 3.52.2 indicates that the PCS receiver lane 2 has not achieved alignment marker lock. This bit reflects the state of am_lock[2] (see 82.2.19.2.2).

45.2.3.25.7 Lane 1 aligned (3.52.1)

When read as a one, bit 3.52.1 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 1. When read as a zero, bit 3.52.1 indicates that the PCS receiver lane 1 has not achieved alignment marker lock. This bit reflects the state of am_lock[1] (see 82.2.19.2.2).

45.2.3.25.8 Lane 0 aligned (3.52.0)

When read as a one, bit 3.52.0 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 0. When read as a zero, bit 3.52.0 indicates that the PCS receiver lane 0 has not achieved alignment marker lock. This bit reflects the state of am_lock[0] (see 82.2.19.2.2).

45.2.3.26 Multi-lane BASE-R PCS alignment status 4 register (Register 3.53)

The assignment of bits in the multi-lane BASE-R PCS alignment status 4 register is shown in Table 45–255. All the bits in the multi-lane BASE-R PCS alignment status 4 register are read only; a write to the multi-lane BASE-R PCS alignment status 4 register shall have no effect. A PCS device that does not implement multi-lane BASE-R PCS shall return a zero for all bits in the multi-lane BASE-R PCS alignment status 4

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register. A device that implements multi-lane BASE-R PCS shall return a zero for all bits in the multi-lane BASE-R PCS alignment status 4 register that are not required for the PCS configuration. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–255—Multi-lane BASE-R PCS alignment status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.53.15:12	Reserved	Value always 0	RO
3.53.11	Lane 19 aligned	1 = Lane 19 alignment marker is locked 0 = Lane 19 alignment marker is not locked	RO
3.53.10	Lane 18 aligned	1 = Lane 18 alignment marker is locked 0 = Lane 18 alignment marker is not locked	RO
3.53.9	Lane 17 aligned	1 = Lane 17 alignment marker is locked 0 = Lane 17 alignment marker is not locked	RO
3.53.8	Lane 16 aligned	1 = Lane 16 alignment marker is locked 0 = Lane 16 alignment marker is not locked	RO
3.53.7	Lane 15 aligned	1 = Lane 15 alignment marker is locked 0 = Lane 15 alignment marker is not locked	RO
3.53.6	Lane 14 aligned	1 = Lane 14 alignment marker is locked 0 = Lane 14 alignment marker is not locked	RO
3.53.5	Lane 13 aligned	1 = Lane 13 alignment marker is locked 0 = Lane 13 alignment marker is not locked	RO
3.53.4	Lane 12 aligned	1 = Lane 12 alignment marker is locked 0 = Lane 12 alignment marker is not locked	RO
3.53.3	Lane 11 aligned	1 = Lane 11 alignment marker is locked 0 = Lane 11 alignment marker is not locked	RO
3.53.2	Lane 10 aligned	1 = Lane 10 alignment marker is locked 0 = Lane 10 alignment marker is not locked	RO
3.53.1	Lane 9 aligned	1 = Lane 9 alignment marker is locked 0 = Lane 9 alignment marker is not locked	RO
3.53.0	Lane 8 aligned	1 = Lane 8 alignment marker is locked 0 = Lane 8 alignment marker is not locked	RO

[a]RO = Read only

45.2.3.26.1 Lane 19 aligned (3.53.11)

When read as a one, bit 3.53.11 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 19. When read as a zero, bit 3.53.11 indicates that the PCS receiver lane 19 has not achieved alignment marker lock. This bit reflects the state of am_lock[19] (see 82.2.19.2.2).

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45.2.3.26.2 Lane 18 aligned (3.53.10)

When read as a one, bit 3.53.10 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 18. When read as a zero, bit 3.53.10 indicates that the PCS receiver lane 18 has not achieved alignment marker lock. This bit reflects the state of am_lock[18] (see 82.2.19.2.2).

45.2.3.26.3 Lane 17 aligned (3.53.9)

When read as a one, bit 3.53.9 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 17. When read as a zero, bit 3.53.9 indicates that the PCS receiver lane 17 has not achieved alignment marker lock. This bit reflects the state of am_lock[17] (see 82.2.19.2.2).

45.2.3.26.4 Lane 16 aligned (3.53.8)

When read as a one, bit 3.53.8 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 16. When read as a zero, bit 3.53.8 indicates that the PCS receiver lane 16 has not achieved alignment marker lock. This bit reflects the state of am_lock[16] (see 82.2.19.2.2).

45.2.3.26.5 Lane 15 aligned (3.53.7)

When read as a one, bit 3.53.7 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 15. When read as a zero, bit 3.53.7 indicates that the PCS receiver lane 15 has not achieved alignment marker lock. This bit reflects the state of am_lock[15] (see 82.2.19.2.2).

45.2.3.26.6 Lane 14 aligned (3.53.6)

When read as a one, bit 3.53.6 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 14. When read as a zero, bit 3.53.6 indicates that the PCS receiver lane 14 has not achieved alignment marker lock. This bit reflects the state of am_lock[14] (see 82.2.19.2.2).

45.2.3.26.7 Lane 13 aligned (3.53.5)

When read as a one, bit 3.53.5 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 13. When read as a zero, bit 3.53.5 indicates that the PCS receiver lane 13 has not achieved alignment marker lock. This bit reflects the state of am_lock[13] (see 82.2.19.2.2).

45.2.3.26.8 Lane 12 aligned (3.53.4)

When read as a one, bit 3.53.4 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 12. When read as a zero, bit 3.53.4 indicates that the PCS receiver lane 12 has not achieved alignment marker lock. This bit reflects the state of am_lock[12] (see 82.2.19.2.2).

45.2.3.26.9 Lane 11 aligned (3.53.3)

When read as a one, bit 3.53.3 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 11. When read as a zero, bit 3.53.3 indicates that the PCS receiver lane 11 has not achieved alignment marker lock. This bit reflects the state of am_lock[11] (see 82.2.19.2.2).

45.2.3.26.10 Lane 10 aligned (3.53.2)

When read as a one, bit 3.53.2 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 10. When read as a zero, bit 3.53.2 indicates that the PCS receiver lane 10 has not achieved alignment marker lock. This bit reflects the state of am_lock[10] (see 82.2.19.2.2).

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45.2.3.26.11 Lane 9 aligned (3.53.1)

When read as a one, bit 3.53.1 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 9. When read as a zero, bit 3.53.1 indicates that the PCS receiver lane 9 has not achieved alignment marker lock. This bit reflects the state of am_lock[9] (see 82.2.19.2.2).

45.2.3.26.12 Lane 8 aligned (3.53.0)

When read as a one, bit 3.53.0 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 8. When read as a zero, bit 3.53.0 indicates that the PCS receiver lane 8 has not achieved alignment marker lock. This bit reflects the state of am_lock[8] (see 82.2.19.2.2).

45.2.3.27 10P/2B capability register (3.60)

The 10P/2B capability register reports which functions are supported by the PCS. This register is present at the PCS layer for each PHY. The bit definitions of the 10P/2B capability register are shown in Table 45–256.

Table 45–256—10P/2B capability register bit definitions

Bit(s)	Name	Description	R/W[a]
3.60.15:13	Reserved	Value always 0	RO
3.60.12	PAF available	1 = PAF supported 0 = PAF not supported	RO
3.60.11	Remote PAF supported	1 = link partner supports PAF 0 = link partner does not support PAF	RO
3.60.10:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.3.27.1 PAF available (3.60.12)

This bit indicates that the PHY supports the PME aggregation function. The PHY sets this bit to a one when the capability is supported and zero otherwise. This bit reflects the signal PAF_available in 61.2.3.

45.2.3.27.2 Remote PAF supported (3.60.11)

This bit indicates that the remote, link-partner PHY supports the PME aggregation function. The PHY sets this bit to a one when the capability is supported and zero otherwise. This bit does not accurately report the capability of the remote PCS until a remote discovery operation has been completed by the -O PHY. In this case, this bit is set if the “Ethernet bonding” NPar(2) bit is set in the capabilities exchange message received from the other device. See 61.4.7, which discusses use of G.994.1 to access remote registers.

45.2.3.28 10P/2B PCS control register (Register 3.61)

The assignment of bits in the 10P/2B PCS control register is shown in Table 45–257.

45.2.3.28.1 MII receive during transmit (3.61.15)

This register bit is used to tell the PHY-MAC rate matching function if the MAC is capable of receiving frames from the PHY while the MAC is transmitting (i.e., sending frames to the PHY). The variable

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Table 45–257—10B/2B PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.61.15	MII receive during transmit	1 = MII can TX/RX simultaneously 0 = MII cannot TX/RX simultaneously (default)	R/W
3.61.14	TX_EN and CRS infer a collision	1 = MII uses TX_EN and CRS to infer a collision 0 = MII uses COL to indicate a collision (default)	R/W
3.61.13:1	Reserved	Value always 0	RO
3.61.0	PAF enable	1 = use PAF 0 = do not use PAF	O: R/W R: RO

[a]R/W = Read/Write, RO = Read only

tx_rx_simultaneously for the PHY-MAC Rate-Matching function takes on the value of this bit as defined in 61.2.3.

45.2.3.28.2 TX_EN and CRS infer a collision (3.61.14)

This bit is set by the STA to tell the MAC-PHY rate matching function that the MAC-PHY interface does not have a separate collision signal but instead infers a collision when TX_EN and CRS are asserted simultaneously. The variable crs_and_tx_en_infer_col in the PHY-MAC Rate-Matching function takes on the value of this bit as in 61.2.3. This bit will default to a supported mode, and writes to unsupported modes will be ignored.

45.2.3.28.3 PAF enable (3.61.0)

Setting this bit to a one shall activate the PME aggregation function of the PCS when the link is established. Writes to this bit while link is up or initializing (see 45.2.1.28) or if the PAF is not supported shall be ignored. When link is established, handshake indicates the use of PAF to the -R PHY. This bit reflects the signal PAF_enable in 61.2.3.

45.2.3.29 10P/2B PME available (Registers 3.62 and 3.63)

The 10P/2B PME available registers are used to indicate which PMEs in the aggregation group are available to be attached to the queried PCS. A PME is marked as unavailable if the PME does not support PME aggregation or if the PME is currently marked to be aggregated with another PMD. For a device that does not support aggregation of multiple PMEs, a single bit of this register shall be set to one and all other bits cleared to zero.

These registers may be writeable for -R ports. For PMEs that may be accessed through more than one MII, the availability is limited such that no PME may be mapped to more than one MII prior to enabling the links. In this case, the reset state of the 10P/2B PME available registers shall reflect the capabilities of the device, the management entity should reset appropriate bits to meet the restriction described.

If the -R device is not capable of aggregating PMEs to multiple MIIs then these registers may be read only.

The 10P/2B PME available register shall be available per PCS. For example, a package implementing four PMEs and one MII would have only one set of 10P/2B PME available registers, addressed by a read or write to 3.62 and 3.63 on any of those PHYs.

For more information, see 61.2.2.8.3.

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The assignment of bits in the 10P/2B PME available registers is shown in Table 45–258.

Table 45–258—10P/2B PME available register bit definitions

Bit(s)	Name	Description	R/W[a]
3.62.15:0	PME [p = 31:16] available	For each bit in the sequence: 1 = PME[p] is available for aggregating 0 = PME[p] is unavailable	O: RO R: R/W
3.63.15:0	PME [p = 15:0] available	For each bit in the sequence: 1 = PME[p] is available for aggregating 0 = PME[p] is unavailable	O: RO R: R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.30 10P/2B PME aggregate registers (Registers 3.64 and 3.65)

The 10P/2B PME aggregate registers are used to select PMEs for aggregation. Attempts to activate aggregation with an unavailable PME (see 45.2.3.29) are ignored. The PCS shall use PME aggregation if one or more bits are set to a one and if PME aggregation is supported.

The 10P/2B PME aggregate register shall be available per PCS. For example, a package implementing four PMEs and one MII would have only one set of 10P/2B PME aggregate registers, accessed by a read or write to 3.64, 3.65 on any of those PHYs.

Upon MMD reset, these registers shall be reset to all zeros.

For more information, see 61.2.2.8.3.

The assignment of bits for the 10P/2B PME aggregate registers is shown in Table 45–259.

Table 45–259—10P/2B PME aggregate register bit definitions

Bit(s)	Name	Description	R/W[a]
3.64.15:0	Aggregate with PME [p = 31:16]	For each bit in the sequence: 1 = activate aggregation with PME[p] 0 = deactivate aggregation with PME[p]	R/W
3.65.15:0	Aggregate with PME [p = 15:0]	For each bit in the sequence: 1 = activate aggregation with PME[p] 0 = deactivate aggregation with PME[p]	R/W

[a]R/W = Read/Write

45.2.3.31 10P/2B PAF RX error register (Register 3.66)

The 10P/2B PAF RX error register is a 16 bit counter that contains the number of fragments that have been received across the gamma interface with RxErr asserted. The corresponding signal, TC_PAF_RxErrorReceived, is defined in 61.2.3. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be reset to all zeros

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when the 10P/2B PAF RX error register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF RX error register is shown in Table 45–260.

Table 45–260—10P/2B PAF RX error register bit definitions

Bit(s)	Name	Description	R/W[a]
3.66.15:0	PAF RX errors[15:0]	The bytes of the counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.32 10P/2B PAF small fragments register (Register 3.67)

The 10P/2B PAF small fragments register is a 16 bit counter that contains the number of small fragments that have been received across the gamma interface. The corresponding signal, TC_PAF_FragmentTooSmall, is defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF small fragment register is shown in Table 45–261.

Table 45–261—10P/2B PAF small fragments register bit definitions

Bit(s)	Name	Description	R/W[a]
3.67.15:0	PAF small fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.33 10P/2B PAF large fragments register (Register 3.68)

The 10P/2B PAF large fragments register is a 16 bit counter that contains the number of large fragments that have been received across the gamma interface. The corresponding signal, TC_PAF_FragmentTooLarge, is defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF large fragments register is shown in Table 45–262.

Table 45–262—10P/2B PAF large fragments register bit definitions

Bit(s)	Name	Description	R/W[a]
3.68.15:0	PAF large fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.34 10P/2B PAF overflow register (Register 3.69)

The 10P/2B PAF overflow register is a 16 bit counter that contains the number of fragments that have been received across the gamma interface which would have caused the receive buffer to overflow. The

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corresponding signal, TC_PAF_Overflow, is defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF overflow register is shown in Table 45–263.

Table 45–263—10P/2B PAF overflow register bit definitions

Bit(s)	Name	Description	R/W[a]
3.69.15:0	PAF overflow fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.35 10P/2B PAF bad fragments register (Register 3.70)

The 10P/2B PAF bad fragments register is a 16 bit counter that contains the number of bad fragments that have been received across the gamma interface. The corresponding signal, TC_PAF_BadFragmentReceived, is defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF bad fragments register is shown in Table 45–264.

Table 45–264—P10P/2B AF bad fragments register bit definitions

Bit(s)	Name	Description	R/W[a]
3.70.15:0	PAF bad fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.36 10P/2B PAF lost fragments register (Register 3.71)

The 10P/2B PAF lost fragments register is a 16 bit counter that contains the number of gaps in the sequence of fragments that have been received across the gamma interface. The corresponding signal, TC_PAF_LostFragment, is defined in 61.2.3.

These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF lost fragments register is shown in Table 45–265.

Table 45–265—10P/2B PAF lost fragments register bit definitions

Bit(s)	Name	Description	R/W[a]
3.71.15:0	PAF lost fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

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45.2.3.37 10P/2B PAF lost starts of fragments register (Register 3.72)

The 10P/2B PAF lost starts of fragments register is a 16-bit counter that contains the number of missing start of fragment indicators expected by the frame assembly function. The corresponding signal, TC_PAF_LostStart, is defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF lost starts of fragments register is shown in Table 45–266.

Table 45–266—10P/2B PAF lost starts of fragments register bit definitions

Bit(s)	Name	Description	R/W[a]
3.72.15:0	PAF lost starts of fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.38 10P/2B PAF lost ends of fragments register (Register 3.73)

The 10P/2B PAF lost ends of fragments register is a 16 bit counter that contains the number of missing end of fragment indicators expected by the frame assembly function. The corresponding signal, TC_PAF_LostEnd, is defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. This counter is inactive when the PAF is unsupported or disabled. Upon disabling the PAF, the register retains its previous value. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PAF lost ends of fragments register is shown in Table 45–267.

Table 45–267—10P/2B PAF lost ends of fragments register bit definitions

Bit(s)	Name	Description	R/W[a]
3.73.15:0	PAF lost ends of fragments[15:0]	The bytes of the counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.39 10GBASE-PR and 10/1GBASE-PRX FEC ability register (Register 3.74)

The assignment of bits in the 10GBASE-PR and 10/1GBASE-PRX FEC ability register is shown in Table 45–268.

Table 45–268—10GBASE-PR and 10/1GBASE-PRX FEC ability register bit definitions

Bit(s)	Name	Description	R/W[a]
3.74.15:1	Reserved	Value always 0	RO
3.74.0	10 Gb/s FEC ability	A read of one in this bit indicates that the PCS supports the 10/1GBASE-PRX or 10GBASE-PR 10 Gb/s FEC (always reads as one for 10/1GBASE-PRX or 10GBASE-PR).	RO

[a]RO = Read only

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45.2.3.40 10GBASE-PR and 10/1GBASE-PRX FEC control register (Register 3.75)

The assignment of bits in the 10GBASE-PR FEC control register is shown in Table 45–269.

Table 45–269—10GBASE-PR and 10/1GBASE-PRX FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.75.15:2	Reserved	Value always 0	RO
3.75.1	Enable FEC error indication	A write of one to this bit configures the 10 Gb/s FEC decoder to indicate uncorrectable codeword errors to the higher layer. In a 10/1GBASE-PRX OLT, this bit is undefined.	R/W
3.75.0	10 Gb/s FEC enable	Always reads as one for 10/1GBASE-PRX or 10GBASE-PR since 10 Gb/s FEC is always enabled.	RO

[a]RO = Read only, R/W = Read/Write

45.2.3.40.1 FEC enable error indication (3.75.1)

This bit instructs the 10 Gb/s FEC decoder component of the 10GBASE-PR and 10/1GBASE-PRX PCS to indicate decoding errors to the upper layers (see 45.2.3.40 and 76.3.3.3).

When written as a one, the receiving PCS invalidates 66 bit blocks received in uncorrectable FEC codewords. As a consequence, the receiving MAC discards any packet which includes data that was received in an uncorrectable FEC codeword (even though the packet itself might or might not contain errors).

When written as a zero, the receiving PCS does not modify 66 bit blocks received in uncorrectable FEC codewords. As a consequence, the receiving MAC performs regular processing on a packet that includes data that was received in an uncorrectable FEC codeword (though the packet itself may contain errors which might or might not be detected by the MAC FCS)

45.2.3.40.2 10 Gb/s FEC Enable (3.75.0)

This bit indicates whether 10 Gb/s FEC is enabled in the 10GBASE-PR and 10/1GBASE-PRX PCS and always reads as one.

The register for enabling and disabling forward error correction in the 10/1GBASE-PRX upstream is specified in 45.2.10.3.

45.2.3.41 10G-EPON and Nx25G-EPON corrected FEC codewords counter (Register 3.76, 3.77)

The assignment of bits in the 10G-EPON and Nx25G-EPON corrected FEC codewords counter register is shown in Table 45–270. See 76.3.3.3.2 for a definition of the 10G-EPON counters and 142.3.5.2 for the definition of the Nx25-EPON counters. These bits shall be reset to all zeros when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

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Table 45–270—10G-EPON and Nx25G-EPON corrected FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.76.15:0	corrected FEC codewords lower	corrected_FEC_codewords_counter[15:0]	RO, MW, NR
3.77.15:0	corrected FEC codewords upper	corrected_FEC_codewords_counter[31:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

45.2.3.42 10G-EPON and Nx25G-EPON uncorrected FEC codewords counter (Register 3.78, 3.79)

The assignment of bits in the 10G-EPON and Nx25G-EPON uncorrected FEC codewords counter register is shown in Table 45–271. See 76.3.3.3.2 for a definition of the 10G-EPON counters and 142.3.5.2 for the definition of the Nx25-EPON counters. These bits shall be reset to all zeros when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–271—10G-EPON and Nx25G-EPON uncorrected FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.78.15:0	uncorrected FEC codewords lower	uncorrected_FEC_codewords_counter[15:0]	RO, MW, NR
3.79.15:0	uncorrected FEC codewords lower	uncorrected_FEC_codewords_counter[32:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

45.2.3.43 10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval control register (Register 3.80)

The assignment of bits in the 10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval control register is shown in Table 45–272. This register is defined only when 10GBASE-PR,

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10/1GBASE-PRX, or Nx25G-EPON ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4. The Nx25G-EPON QC-LDPC BER Monitor is described in 142.3.5.6.

Table 45–272—10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.80.15:8	Reserved	Value always 0	RO
3.80.7:0	EPON BER monitor interval	For 10GBASE-PR and 10/1GBASE-PRX: Duration (in units of 5 microseconds) of the timer used by the BER monitor function. Default value is 25 (i.e., 125 microseconds). A value of zero indicates that the BER monitor function is disabled. For Nx25G-EPON: QC-LDPC codeword count (in units of 16 codewords) of the monitoring interval used by the BER Monitor function. Default value is 12 (i.e., 192 codewords).	R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.44 10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status (Register 3.81)

The assignment of bits in the 10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status register is shown in Table 45–273. This register is defined only when 10GBASE-PR, 10/1GBASE-PRX, or Nx25G-EPON ONU capability is supported.

Table 45–273—10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.81.15:2	Reserved	Value always 0	RO
3.81.1	Latched high BER	10GBASE-PR, 10/1GBASE-PRX, or Nx25G-EPON PCS: 1 = reported a high BER. 0 = did not report a high BER.	RO, LH
3.81.0	high BER	10GBASE-PR, 10/1GBASE-PRX, or Nx25G-EPON PCS: 1 = reporting a high BER. 0 = not reporting a high BER.	RO

[a]RO Read only, LH = Latching high

45.2.3.44.1 10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON PCS high BER (3.81.0)

In the 10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON PCS, when read as a one, bit 3.81.0 indicates that the receiver is detecting a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.0 indicates that the receiver is detecting a BER lower than the configurable threshold (low BER state). This bit mirrors the state of the hi_ber variable, defined in 76.3.3.4 for 10GBASE-PR and 10/1GBASE-PRX, and the HiBer variable in 142.3.5.2 for Nx25G-EPON.

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45.2.3.44.2 10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON PCS latched high BER (3.81.1)

In the 10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON PCS, when read as a one, bit 3.81.1 indicates that the receiver detected a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.1 indicates that the receiver detected BER lower than the configurable threshold (low BER state).

This bit is a latching high version of the 10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON high BER status bit (3.81.0).

45.2.3.45 10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control (Register 3.82)

The assignment of bits in the 10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control register is shown in Table 45–274. This register is defined only when 10GBASE-PR, 10/1GBASE-PRX, or Nx25G-EPON ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4. The Nx25G-EPON QC-LDPC BER Monitor is described in 142.3.5.6.

Table 45–274—10GBASE-PR, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.82.15:0	EPON BER monitor threshold	For 10G-EPON: number of sync header errors within a timer interval that triggers a high BER condition for the BER monitor function. Default value is 1600. A value of zero indicates that the BER monitor function is disabled. For Nx25G-EPON: number of invalid QC-LDPC codeword parity checks within a BER monitor interval that triggers a high BER condition for the BER Monitor function. Default value is 18. A value of zero indicates that the BER Monitor function is disabled.	R/W

[a]R/W = Read/Write

45.2.3.46 Nx25G-EPON synchronization pattern registers (Registers 3.83 through 3.134)

The assignment of bits in registers 3.83 through 3.134 is shown in Table 45–275. The Nx25G-EPON synchronization pattern (see 142.1.3 and 144.3.6.7) is used in the upstream data transmissions to facilitate the OLT in locking to the incoming data burst.

Table 45–275—Nx25G-EPON synchronization pattern registers bit definitions

Bit(s)	Name	Description	R/W[a]
3.83.15:6	Reserved	Value always 0	RO
3.83.5	SP3 bit 257	The MSB of the 257-bit SP3.	R/W
3.83.4	SP3 balanced	Balance setting for SP3.	R/W
3.83.3	SP2 bit 257	The MSB of the 257-bit SP2.	R/W
3.83.2	SP2 balanced	Balance setting for SP2.	R/W

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Table 45–275—Nx25G-EPON synchronization pattern registers bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.83.1	SP1 bit 257	The MSB of the 257-bit SP1.	R/W
3.83.0	SP1 balanced	Balance setting for SP1.	R/W
3.99.15 through 3.84.0	SP1 pattern	The lower 256 bits of SP1. Bit 0 is stored in 3.84.0, and bit 255 is stored in 3.99.15.	R/W
3.100.15:0	SP1 length	The number of times SP1 is to be repeated.	R/W
3.116.15 through 3.101.0	SP2 pattern	The lower 256 bits of SP2. Bit 0 is stored in 3.101.0, and bit 255 is stored in 3.116.15.	R/W
3.117.15:0	SP2 length	The number of times SP2 is to be repeated.	R/W
3.133.15 through 3.118.0	SP3 pattern	The lower 256 bits of SP3. Bit 0 is stored in 3.118.0, and bit 255 is stored in 3.133.15.	R/W
3.134.15:0	SP3 length	The number of times SP3 is to be repeated.	R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.46.1 SP3 bit 257 (3.83.5)

In the Nx25G-EPON PCS, bit 3.83.5 indicates the value to be used for the 257th bit of SP3. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.46.2 SP3 balanced (3.83.4)

In the Nx25G-EPON PCS, bit 3.83.4 indicates that repeating SP3 synchronization patterns are to have a balanced number of one and zero bits transmitted. When this bit is set to a zero then SP3 is to remain unbalanced, i.e., SP3 is always transmitted using the values from 3.83.5 and 3.118.0 through 3.133.15. When this bit is set to a one SP3 is to be balanced, i.e., each 257-bit block of SP3 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.46.3 SP2 bit 257 (3.83.3)

In the Nx25G-EPON PCS, bit 3.83.3 indicates the value to be used for the 257th bit of SP2. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.46.4 SP2 balanced (3.83.2)

In the Nx25G-EPON PCS, bit 3.83.2 indicates that repeating SP2 synchronization patterns are to have a balanced number of one and zero bits transmitted. When this bit is set to a zero then SP2 is to remain unbalanced, i.e., SP2 is always transmitted using the values from 3.83.3 and 3.101.0 through 3.116.15. When this bit is set to a one SP2 is to be balanced, i.e., each 257-bit block of SP2 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.46.5 SP1 bit 257 (3.83.1)

In the Nx25G-EPON PCS, bit 3.83.1 indicates the value to be used for the 257th bit of SP1. See 142.1.3 and 144.3.6.7 for additional details.

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45.2.3.46.6 SP1 balanced (3.83.0)

In the Nx25G-EPON PCS, bit 3.83.0 indicates that repeating SP1 synchronization patterns are to have a balanced number of one and zero bits transmitted. When this bit is set to a zero then SP1 is to remain unbalanced, i.e., SP1 is always transmitted using the values from 3.83.1 and 3.84.0 through 3.99.15. When this bit is set to a one SP1 is to be balanced, i.e., each 257-bit block of SP1 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.46.7 SP1 pattern (3.84.0 through 3.99.15)

In the Nx25G-EPON PCS, bits 3.84.0 through 3.99.15 indicate the value to be used for the lower 256 bits of the initial SP1 transmitted in a burst. If present, subsequent transmissions of the lower 256 bits of SP1 are determined by bit 3.83.0. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.46.8 SP1 length (3.100.15:0)

In the Nx25G-EPON PCS, bits 3.100.15:0 indicate the number of times the 257-bit SP1 is transmitted in a given burst. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.46.9 SP2 pattern (3.101.0 through 3.116.15)

In the Nx25G-EPON PCS, bits 3.101.0 through 3.116.15 indicate the value to be used for the lower 256 bits of the initial SP2 transmitted in a burst. If present, subsequent transmissions of the lower 256 bits of SP2 are determined by bit 3.100.15:0. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.46.10 SP2 length (3.117.15:0)

In the Nx25G-EPON PCS, bits 3.117.15:0 indicate the number of times the 257-bit SP2 is transmitted in a given burst. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.46.11 SP3 pattern (3.118.0 through 3.133.15)

In the Nx25G-EPON PCS, bits 3.118.0 through 3.133.15 indicate the value to be used for the lower 256 bits of the initial SP3 transmitted in a burst. If present, subsequent transmissions of the lower 256 bits of SP3 are determined by bit 3.117.15:0. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.46.12 SP3 length (3.134.15:0)

In the Nx25G-EPON PCS, bits 3.134.15:0 indicate the number of times the 257-bit SP3 is transmitted in a given burst. See 142.1.3 and 144.3.6.7 for additional details.

45.2.3.47 BIP error counter lane 0 (Register 3.200)

The assignment of bits in the BIP error counter lane 0 is shown in Table 45–276. The multi-lane PCS described in Clause 82 calculates a BIP value for each PCS lane (see 82.2.8, 82.2.15). Errors detected in PCS lane 0 are counted and shown in register 3.200.15:0. The 16-bit counter shall be reset to all zeros when register 3.200 is read or upon PCS reset. The 16-bit counter shall be held at all ones in the case of overflow.

45.2.3.48 BIP error counter, lanes 1 through 19 (Registers 3.201 through 3.219)

The behavior of the BIP error counters, lanes 1 through 19 is identical to that described for PCS lane 0 in 45.2.3.47. Errors detected in each PCS lane are counted and shown in register bits 15:0 in the corresponding register. PCS lane 1 is shown in register 3.201; PCS lane 2 is shown in register 3.202; through register 3.219 for PCS lane 19.

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Table 45–276—BIP error counter, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.200.15:0	BIP error counter, lane 0	Errors detected by BIP in PCS lane 0	RO

[a]RO = Read only

45.2.3.49 Lane 0 mapping register (Register 3.400)

The assignment of bits in the Lane 0 mapping register is shown in Table 45–277. When the multi-lane PCS described in Clause 82 or Clause 119 detects and locks the alignment marker for service interface lane 0, the detected PCS lane number is recorded in this register. The contents of the Lane 0 mapping register is valid when Lane 0 aligned bit (3.52.0) is set to one and is invalid otherwise.

Table 45–277—Lane 0 mapping register bit definitions

Bit(s)	Name	Description	R/W[a]
3.400.15:5	Reserved	Value always 0	RO
3.400.4:0	Lane 0 mapping	PCS lane received in service interface lane 0	RO

[a]RO = Read only

45.2.3.50 Lanes 1 through 19 mapping registers (Registers 3.401 through 3.419)

The definition of lanes 1 through 19 mapping registers is identical to that described for lane 0 in 45.2.3.49. The lane mapping for lane 1 is in register 3.401; lane 2 is in register 3.402; etc.

45.2.3.51 1000BASE-H OAM transmit registers (Registers 3.500 through 3.508)

Registers 3.500 through 3.508 are used to transmit messages over the 1000BASE-H OAM channel established between two link partners (see 115.9.1). The 1000BASE-H OAM message is part of the physical header data (PHD) defined for 1000BASE-H (see Table 115–6).

The transmit registers are used to compose a 1000BASE-H OAM message and to control its transmission to the link partner. Register 3.500 contains control, status, identification, and the beginning of a 1000BASE-H OAM message. Eight additional registers (3.501 through 3.508) hold the remainder of the 1000BASE-H OAM message.

The assignment of bits in the 1000BASE-H OAM transmit registers is shown in Table 45–278.

45.2.3.51.1 TXO_REQ (3.500.15)

Bit 3.500.15 set to one requests the 1000BASE-H based PHY to transmit the 1000BASE-H OAM message written to registers 3.500 through 3.508. Bit 3.500.15 is set to zero by the 1000BASE-H based PHY to indicate that the 1000BASE-H OAM message has been accepted for transmission, and that the 1000BASE-H OAM transmit message registers are free to accept a new 1000BASE-H OAM message.

Bit 3.500.15, together with bits 3.500.14 (TXO_PHYT), 3.500.13 (TXO_MERT), and 3.500.12 (TXO_MSGT), indicates the status of the 1000BASE-H OAM transmission channel (see 115.9.2).

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Table 45–278—1000BASE-H OAM transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
3.500.15	TXO_REQ	1 = Transmission of a 1000BASE-H OAM message is pending; write as one to request transmission 0 = 1000BASE-H transmit registers are available for a new 1000BASE-H OAM message	R/W, SC
3.500.14	TXO_PHYT	The identifier of the last 1000BASE-H OAM message received by the remote PHY	RO
3.500.13	TXO_MERT	The identifier of the last 1000BASE-H OAM message read by the STA attached to the remote PHY	RO
3.500.12	TXO_MSGT	1000BASE-H OAM message identifier; its value change with each new transmitted message	RO
3.500.11:0	TXO_DATA0	Transmit 1000BASE-H OAM message first 12 bits	R/W
3.501.15:0	TXO_DATA1	Transmit 1000BASE-H OAM message 16-bit data word 1	R/W
3.502.15:0	TXO_DATA2	Transmit 1000BASE-H OAM message 16-bit data word 2	R/W
3.503.15:0	TXO_DATA3	Transmit 1000BASE-H OAM message 16-bit data word 3	R/W
3.504.15:0	TXO_DATA4	Transmit 1000BASE-H OAM message 16-bit data word 4	R/W
3.505.15:0	TXO_DATA5	Transmit 1000BASE-H OAM message 16-bit data word 5	R/W
3.506.15:0	TXO_DATA6	Transmit 1000BASE-H OAM message 16-bit data word 6	R/W
3.507.15:0	TXO_DATA7	Transmit 1000BASE-H OAM message 16-bit data word 7	R/W
3.508.15:0	TXO_DATA8	Transmit 1000BASE-H OAM message 16-bit data word 8	R/W

[a]R/W = Read/Write, RO = Read only, SC = Self-clearing

45.2.3.51.2 TXO_PHYT (3.500.14)

Bit 3.500.14 reflects the value of the bit TXO_MSGT in the last 1000BASE-H OAM message received by the remote 1000BASE-H based PHY.

45.2.3.51.3 TXO_MERT (3.500.13)

Bit 3.500.13 reflects the value of the bit TXO_MSGT in the last 1000BASE-H OAM message read by the STA attached to the remote 1000BASE-H based PHY.

45.2.3.51.4 TXO_MSGT (3.500.12)

Bit 3.500.12 is used for 1000BASE-H OAM message identification. Bit 3.500.12 is changed by the 1000BASE-H based PHY when it accepts a new 1000BASE-H OAM message for transmission (simultaneously setting bit 3.500.15 to zero), acting as a 1-bit sequence number.

45.2.3.51.5 TXO_DATAx (Bits 3.500.11:0 and registers 3.501 through 3.508)

Bits 3.500.11:0 (TXO_DATA0) contains the first 12 bits of a 1000BASE-H OAM message and registers 3.501 through 3.508 (TXO_DATA1 through TXO_DATA8) the remaining 128 bits of that 1000BASE-H OAM message.

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TXO_DATA0 and TXO_DATA1 shall be a 28-bit 1000BASE-H OAM protocol identifier composed of a 24-bit Organizationally Unique Identifier (OUI) or Company ID (CID) followed by a 4-bit protocol number; where TXO_DATA0[10:0] = OUI[23:12], TXO_DATA1[15:3] = OUI[11:0], and TXO_DATA1[3:0] = protocol number. The content of TXO_DATA2 to TXO_DATA8 is vendor specific to the assignee of the OUI or CID.

45.2.3.52 1000BASE-H OAM receive registers (Registers 3.509 through 3.517)

Registers 3.509 through 3.517 store messages received over the 1000BASE-H OAM channel established between two link partners (see 115.9.3). Register 3.509 contains status information, identification, and the first 12 bits of a 1000BASE-H OAM message, and registers 3.510 through 3.517 the following 128 bits of the received 1000BASE-H OAM message.

The assignment of bits in the 1000BASE-H OAM receive registers is shown in Table 45–279.

Table 45–279—1000BASE-H OAM receive register bit definitions

Bit(s)	Name	Description	R/W[a]
3.509.15	RXO_VAL	1 = A new 1000BASE-H OAM message has arrived 0 = No new 1000BASE-H OAM message arrived since either last message was read or PMA reset	RO
3.509.14:13	Reserved	Value always 0	RO
3.509.12	RXO_MSGT	Identifier of the received 1000BASE-H OAM message	RO
3.509.11:0	RXO_DATA0	Receive 1000BASE-H OAM message first 12 bits	RO
3.510.15:0	RXO_DATA1	Receive 1000BASE-H OAM message 16-bit data word 1	RO
3.511.15:0	RXO_DATA2	Receive 1000BASE-H OAM message 16-bit data word 2	RO
3.512.15:0	RXO_DATA3	Receive 1000BASE-H OAM message 16-bit data word 3	RO
3.513.15:0	RXO_DATA4	Receive 1000BASE-H OAM message 16-bit data word 4	RO
3.514.15:0	RXO_DATA5	Receive 1000BASE-H OAM message 16-bit data word 5	RO
3.515.15:0	RXO_DATA6	Receive 1000BASE-H OAM message 16-bit data word 6	RO
3.516.15:0	RXO_DATA7	Receive 1000BASE-H OAM message 16-bit data word 7	RO
3.517.15:0	RXO_DATA8	Receive 1000BASE-H OAM message 16-bit data word 8	RO

[a]RO = Read only

45.2.3.52.1 RXO_VAL (3.509.15)

The 1000BASE-H based PHY sets bit 3.509.15 to one to indicate the reception of a new 1000BASE-H OAM message. The 1000BASE-H based PHY sets bit 3.509.15 to zero when the last register (3.517) containing the 1000BASE-H OAM message is read (see Figure 115–43). The 1000BASE-H based PHY does not update the receive message registers until the message is read by STA as indicated by a read of register 3.517.

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45.2.3.52.2 RXO_MSGT (3.509.12)

Bit 3.509.12 is used for message identification. Bit 3.509.12 changes with every new received 1000BASE-H OAM message, acting as a 1-bit sequence number.

45.2.3.52.3 RXO_DATAx (Bits 3.509.11:0 and registers 3.510 through 3.517)

Bits 3.509.11:0 (RXO_DATA0) contains the first 12 bits of a received 1000BASE-H OAM message, and registers 3.510 through 3.517 (RXO_DATA1 through RXO_DATA8) the remaining 128 bits of that received 1000BASE-H OAM message.

45.2.3.53 1000BASE-H PCS control register (Register 3.518)

The assignment of bits in the 1000BASE-H PCS control register is shown in Table 45–280.

Table 45–280—1000BASE-H PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.518.15:13	Operation mode	15 14 13 0 0 0 = Normal operation 0 0 1 = Test mode 1 0 1 0 = Test mode 2 0 1 1 = Test mode 3 1 0 0 = Test mode 4 1 0 1 = Test mode 5 1 1 0 = Test mode 6 1 1 1 = Reserved	R/W
3.518.12:10	Loopback mode	12 11 10 0 0 0 = No loopback 0 0 1 = GMII level loopback 0 1 0 = PMD interface level loopback 0 1 1 = Line loopback 1 x x = Reserved	R/W
3.518.9:2	Reserved	Value always 0	RO
3.518.1	1000BASE-H OAM enable	1 = Enable 1000BASE-H OAM functionality 0 = Disable 1000BASE-H OAM functionality	R/W
3.518.0	EEE enable	1 = Enable LPI mode 0 = Disable LPI mode	R/W

[a]R/W = Read/Write, RO = Read only

45.2.3.53.1 Operation mode (3.518.15:13)

Bits 3.518.15:13 shall have a default value of binary 000, selecting normal 1000BASE-H operation. A value of binary 001 through binary 110 in bits 3.518.15:13 shall select the test mode as specified in Table 45–280 with behavior as defined in 115.5.

45.2.3.53.2 Loopback mode (3.518.12:10)

Bits 3.518.12:10 shall select one of the loopback modes defined in 115.10. Bits 3.518.12:10 shall have a default value of binary 000 (no loopback operation). Loopback modes are only available when a 1000BASE-H based PHY is in the normal operation mode (no test mode is selected in 3.518.15:13).

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45.2.3.53.3 1000BASE-H OAM enable (3.518.1)

Bit 3.518.1 controls establishing the 1000BASE-H OAM channel with the link partner (115.9). If the 1000BASE-H based PHY does not have 1000BASE-H OAM ability (bit 3.519.1 = 0), setting bit 3.518.1 shall have no effect. Setting bit 3.518.1 to zero shall prevent establishment of a 1000BASE-H OAM channel with the link partner. Changes in a 1000BASE-H OAM enable value shall only take effect after a PMA reset. Bit 3.518.1 has no specified default value.

45.2.3.53.4 EEE enable (3.518.0)

Setting bit 3.518.0 to one enables 1000BASE-H based PHY EEE capability (see 115.4). Setting bit 3.518.0 to zero shall prevent establishment of EEE operation with the link partner. If the 1000BASE-H based PHY does not have EEE ability (bit 3.519.0 = 0), setting bit 3.518.0 shall have no effect. Changes in EEE enable value shall only take effect after a PMA reset. Bit 3.518.0 has no specified default value.

45.2.3.54 1000BASE-H PCS status 1 register (Register 3.519)

The assignment of bits in the 1000BASE-H PCS status 1 register is shown in Table 45–281.

Table 45–281— 1000BASE-H PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.519.15	Local receiver status	1 = The local receive operation is reliable 0 = The local receive operation is unreliable	RO
3.519.14	Remote receiver status	1 = The receive operation of the remote PHY is reliable 0 = The receive operation of the remote PHY is unreliable	RO
3.519.13	Link status	1 = A bidirectional reliable link is established 0 = A bidirectional reliable link is not established	RO, LL
3.519.12	Local PHD reception status	1 = PHD reception is reliable for the local PHY 0 = PHD reception is unreliable for the local PHY	RO
3.519.11	Remote PHD reception status	1 = PHD reception is reliable for the remote PHY 0 = PHD reception is unreliable for the remote PHY	RO
3.519.10	PHD lock status	1 = PHD transmission and reception are reliable 0 = PHD transmission or reception are unreliable	RO, LL
3.519.9	THP lock status	1 = THP is initialized; payload data is received with THP processing 0 = THP is not initialized	RO
3.519.8	Tx Assert LPI received	1 = Tx PCS has received LPI 0 = LPI not received by Tx PCS	RO, LH
3.519.7	Rx Assert LPI generated	1 = Rx PCS has generated LPI 0 = LPI not generated by Rx PCS	RO, LH
3.519.6	Tx LPI indication	1 = Tx PCS is currently transmitting LPI 0 = Tx PCS is not currently transmitting LPI	RO
3.519.5	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = Rx PCS is not currently receiving LPI	RO
3.519.4	Reserved	Value always 0	RO

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Table 45–281— 1000BASE-H PCS status 1 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.519.3	Remote 1000BASE-H OAM ability	1 = The remote PHY has 1000BASE-H OAM ability and it is enabled 0 = The remote PHY does not have 1000BASE-H OAM ability or it is disabled	RO
3.519.2	Remote EEE ability	1 = The remote PHY has EEE ability and it is enabled 0 = The remote PHY does not have EEE ability or it is disabled	RO
3.519.1	1000BASE-H OAM ability	1 = The PHY has 1000BASE-H OAM ability 0 = The PHY does not have 1000BASE-H OAM ability	RO
3.519.0	EEE ability	1 = The PHY has EEE ability 0 = The PHY does not have EEE ability	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.3.54.1 Local receiver status (3.519.15)

Bit 3.519.15 reflects the value of the state variable loc_rcvr_status as determined by the PHY quality monitor state diagram (see 115.3.5.1).

45.2.3.54.2 Remote receiver status (3.519.14)

Bit 3.519.14 reflects the value of the state variable rem_rcvr_status as determined by the link monitor state diagram (see 115.3.5.1).

45.2.3.54.3 Link status (3.519.13)

Bit 3.519.13 reflects the value of the state variable link_status as determined by the link monitor state diagram (see 115.3.5.1). Bit 3.519.13 shall have latching low behavior. Bit 1.1.2, bit 3.1.2, and bit 3.519.13 are identical for 1000BASE-H; a read to any of these three bits shall release the latch for all the bits.

45.2.3.54.4 Local PHD reception status (3.519.12)

Bit 3.519.12 reflects the value of the state variable loc_rcvr_hdr_lock as determined by the local PHD reception monitor state diagram (see 115.3.5.1).

45.2.3.54.5 Remote PHD reception status (3.519.11)

Bit 3.519.11 reflects the value of the state variable rem_rcvr_hdr_lock as determined by the remote PHD reception monitor state diagram (see 115.3.5.1).

45.2.3.54.6 PHD lock status (3.519.10)

Bit 3.519.10 reflects the value of the state variable rcvr_hdr_lock as determined by the PHD monitor state diagram (see 115.3.5.1). Bit 3.519.10 shall have latching low behavior.

45.2.3.54.7 THP lock status (3.519.9)

Bit 3.519.9 reflects the value of the state variable rcvr_thp_lock as determined by the adaptive THP REQ state diagram (see 115.3.6.1).

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45.2.3.54.8 Tx Assert LPI received (3.519.8)

When read as a one, bit 3.519.8 indicates that the transmit 1000BASE-H PCS has received Assert LPI signaling from the TX GMII one or more times since the register was last read. When read as a zero, bit 3.519.8 indicates that the 1000BASE-H PCS transmitter has not received Assert LPI. Bit 3.519.8 shall have latching high behavior. Bit 3.519.8 is a copy of bit 3.1.11; a read of either bit shall release the latch for all the bits.

45.2.3.54.9 Rx Assert LPI generated (3.519.7)

When read as a one, bit 3.519.7 indicates that the receive 1000BASE-H PCS has generated Assert LPI on the RX GMII one or more times since the register was last read. When read as a zero, bit 3.519.7 indicates that the 1000BASE-H PCS receiver has not generated Assert LPI on the RX GMII. Bit 3.519.7 shall have latching high behavior. Bit 3.519.7 is a copy of bit 3.1.10; a read of either bit shall release the latch for all the bits.

45.2.3.54.10 Tx LPI indication (3.519.6)

Bit 3.519.6 indicates the current LPI mode status of the local 1000BASE-H based PHY transmit path. When read as one, the PHY transmitter is currently in LPI mode (transmitting refresh and quiet). When read as zero, the PHY transmitter is not in LPI mode (see 115.4.1). Bit 3.519.6 is a copy of bit 3.1.9.

45.2.3.54.11 Rx LPI indication (3.519.5)

Bit 3.519.5 indicates the current LPI mode status of the local 1000BASE-H based PHY receive path. When read as a one, the PHY is receiving LPI mode signals (refresh and quiet). When read as a zero, the PHY is not receiving LPI mode signals (see 115.4.2). Bit 3.519.5 is a copy of bit 3.1.8.

45.2.3.54.12 Remote 1000BASE-H OAM ability (3.519.3)

Bit 3.519.3 indicates the 1000BASE-H OAM ability of the remote PHY received in the PHD field PHD.CAP.OAM (see Table 115–6). When read as one, bit 3.519.3 indicates the remote PHY has both 1000BASE-H OAM ability and the 1000BASE-H OAM is enabled. When read as zero, bit 3.519.3 indicates that the remote PHY either does not have 1000BASE-H OAM ability or 1000BASE-H OAM is disabled.

45.2.3.54.13 Remote EEE ability (3.519.2)

Bit 3.519.2 indicates the EEE ability of the remote PHY received in the PHD field PHD.CAP.LPI (see Table 115–6). When read as one, bit 3.519.2 indicates the remote PHY has both EEE ability and EEE is enabled. When read as zero, bit 3.519.2 indicates that the remote PHY either does not have EEE ability or EEE is disabled.

45.2.3.54.14 1000BASE-H OAM ability (3.519.1)

Bit 3.519.1 indicates the 1000BASE-H OAM ability of the 1000BASE-H based PHY (see 115.9). When read as one, bit 3.519.1 indicates that the 1000BASE-H based PHY supports the 1000BASE-H OAM protocol. When read as zero, bit 3.519.1 indicates the 1000BASE-H based PHY does not support the 1000BASE-H OAM protocol.

A PHY indicating in bit 3.519.1 support of 1000BASE-H OAM shall provide the functions of registers 3.500 through 3.517 as specified in 115.9.

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45.2.3.54.15 EEE ability (3.519.0)

Bit 3.519.0 indicates the EEE ability of the 1000BASE-H based PHY. When read as one, bit 3.519.0 indicates that the 1000BASE-H based PHY implements EEE, and is able to enter LPI mode (see 115.4). When read as zero, bit 3.519.0 indicates the 1000BASE-H based PHY does not implement EEE operation.

45.2.3.55 1000BASE-H PCS status 2 register (Register 3.520)

The assignment of bits in the 1000BASE-H PCS status 2 register is shown in Table 45–282.

Table 45–282—1000BASE-H PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.520.15:8	Reserved	Value always 0	RO
3.520.7:0	Local link margin	Reports the local link margin	RO

[a]RO = Read only

45.2.3.55.1 Local link margin (3.520.7:0)

Bits 3.520.7:0 indicate the link margin of the receiver. Link margin is defined in 115.3.7.2 and is fixed-point formatted (8,3). See 115.3.8 for fixed-point format definition.

45.2.3.56 1000BASE-H PCS status 3 register (Register 3.521)

The assignment of bits in the 1000BASE-H PCS status 3 register is shown in Table 45–283.

Table 45–283—1000BASE-H PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.521.15:8	Reserved	Value always 0	RO
3.521.7:0	Remote link margin	Link margin reported by the link partner	RO

[a]RO = Read only

45.2.3.56.1 Remote link margin (3.521.7:0)

Bits 3.521.7:0 report the link margin of the remote PHY receiver as it is received in the PHD field PHD.RX.LINKMARGIN (see Table 115–6). Link margin is defined in 115.3.7.2 and is fixed-point formatted (8,3). See 115.3.8 for fixed-point format definition.

45.2.3.57 1000BASE-H PCS status 4 register (Register 3.522)

The assignment of bits in the 1000BASE-H PCS status 4 register is shown in Table 45–284.

Bits 3.522.15:0 are a 16-bit counter that counts the number of bits received with value 1 at the output of the binary descrambler, when the 1000BASE-H based PHY receiver is operating in test mode 1. These bits shall be reset to all zeros when the counter is read. The counter shall be held at all ones in the case of overflow.

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Table 45–284—1000BASE-H PCS status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.522.15:0	BER test mode counter	A 16-bit counter used when operating in test mode 1	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.58 PCS FEC symbol error counter lane 0 (Register 3.600, 3.601)

The assignment of bits in the PCS FEC symbol error counter lane 0 register is shown in Table 45–285. See 119.3.4 for a definition of this counter. Symbol errors detected in PCS lane 0 are counted and shown in register 3.600.15:0 and 3.601.15:0. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 3.600, 3.601 are used to read the value of a 32-bit counter. When registers 3.600 and 3.601 are used to read the 32-bit counter value, the register 3.600 is read first, the value of the register 3.601 is latched when (and only when) register 3.600 is read, and reads of register 3.601 return the latched value rather than the current value of the counter.

Table 45–285—PCS FEC symbol error counter lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.600.15:0	PCS FEC symbol errors, lane 0 lower	FEC_symbol_error_counter_0[15:0]	RO, NR
3.601.15:0	PCS FEC symbol errors, lane 0 upper	FEC_symbol_error_counter_0[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.59 PCS FEC symbol error counter lane 1 through 15 (Registers 3.602 through 3.631)

The behavior of the PCS FEC symbol error counters, lane 1 through 15 is identical to that described for PCS lane 0 in 45.2.3.58. Errors detected in each PCS lane are counted and shown in the corresponding register. PCS lane 1, lower 16 bits are shown in register 3.602; PCS lane 1, upper 16 bits are shown in register 3.603; PCS lane 2, lower 16 bits are shown in register 3.604; through register 3.631 for PCS lane 15, upper 16 bits.

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45.2.3.60 PCS FEC control register (Register 3.800)

The assignment of bits in the PCS FEC control register is shown in Table 45–286.

Table 45–286—PCS FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.800.15:3	Reserved	Value always 0	RO
3.800.2	PCS FEC degraded SER enable	1 = FEC decoder signals degraded SER 0 = FEC decoder does not signal degraded SER	R/W
3.800.1	PCS FEC bypass indication enable	1 = FEC decoder does not indicate errors 0 = FEC decoder indicates errors	R/W
3.800.0	Reserved	Value always 0	RO

[a]R/W = Read/Write, RO = Read only

45.2.3.60.1 PCS FEC degraded SER enable (3.800.2)

This bit enables the PCS FEC decoder to signal the presence of a degraded SER. When set to a one, this bit enables degraded SER signaling. When set to a zero, degraded SER signaling is disabled. Writes to this bit are ignored and reads return a zero if the PCS FEC does not have the ability to signal the presence of a degraded SER (see 119.2.5.3).

45.2.3.60.2 PCS FEC bypass indication enable (3.800.1)

This bit enables the PCS FEC decoder to bypass error indication to the upper layers through the sync bits. When set to a one, this bit enables bypass of the error indication. When set to a zero, errors are indicated to the upper layers through the sync bits. Writes to this bit are ignored and reads return a zero if the PCS FEC does not have the ability to bypass indicating decoding errors (see 119.2.5.3).

45.2.3.61 PCS FEC status register (Register 3.801)

The assignment of bits in the PCS FEC status register is shown in Table 45–287.

Table 45–287—PCS FEC status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.801.15:7	Reserved	Value always 0	RO
3.801.6	Local degraded SER received	1 = local degraded SER received 0 = no local degraded SER received	RO
3.801.5	Remote degraded SER received	1 = remote degraded SER received 0 = no remote degraded SER received	RO
3.801.4	PCS FEC degraded SER	1 = SER is degraded 0 = SER is not degraded	RO

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Table 45–287—PCS FEC status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.801.3	PCS FEC degraded SER ability	1 = FEC decoder has the ability to signal the presence of a degraded SER 0 = FEC decoder does not have the ability to signal the presence of a degraded SER	RO
3.801.2	PCS FEC high SER	1 = FEC errors have exceeded threshold 0 = FEC errors have not exceeded threshold	RO/LH
3.801.1	PCS FEC bypass indication ability	1 = FEC decoder has the ability to bypass error indication 0 = FEC decoder does not have the ability to bypass error indication	RO
3.801.0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

45.2.3.61.1 Local degraded SER received (3.801.6)

When read as a one, bit 3.801.6 indicates that the local degraded SER signal has been received. This bit reflects the state of rx_local_degraded (see 119.2.6.2.2).

45.2.3.61.2 Remote degraded SER received (3.801.5)

When read as a one, bit 3.801.5 indicates that the remote degraded SER signal has been received. This bit reflects the state of rx_rm_degraded (see 119.2.6.2.2).

45.2.3.61.3 PCS FEC degraded SER (3.801.4)

When read as a one, bit 3.801.4 indicates that the local PCS has detected a degradation of the received signal. This bit reflects the state of the variable FEC_degraded_SER (see 119.2.5.3). The value of bit 3.801.4 is unspecified if the value of the PCS FEC degraded SER activate threshold (registers 3.806 and 3.807) is less than the value of the PCS FEC degraded SER deactivate threshold (registers 3.808 and 3.809).

45.2.3.61.4 PCS FEC degraded SER ability (3.801.3)

The PCS FEC decoder may have the option to signal the presence of a degraded SER (see 119.2.5.3). This bit is set to one to indicate that the decoder has the ability to signal the presence of a degraded SER. The bit is set to zero if this ability is not supported.

45.2.3.61.5 PCS FEC high SER (3.801.2)

When PCS FEC bypass indication enable (bit 3.800.1) is set to one, this bit is set to one if the number of FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 119.2.5.3) and is set to zero otherwise. The bit is set to zero if PCS FEC bypass indication enable (bit 3.800.1) is set to zero. This bit shall be implemented with latching high behavior.

45.2.3.61.6 PCS FEC bypass indication ability (3.801.1)

The PCS FEC decoder may have the option to perform error detection without error indication (see 119.2.5.3) to reduce the delay contributed by the FEC decoder. This bit is set to one to indicate that the decoder has this ability to bypass error indication. The bit is set to zero if this ability is not supported.

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45.2.3.62 PCS FEC corrected codewords counter (Register 3.802, 3.803)

The assignment of bits in the PCS FEC corrected codewords counter register is shown in Table 45–288. See 119.3.2 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 3.802, 3.803 are used to read the value of a 32-bit counter. When registers 3.802 and 3.803 are used to read the 32-bit counter value, the register 3.802 is read first, the value of the register 3.803 is latched when (and only when) register 3.802 is read, and reads of register 3.803 return the latched value rather than the current value of the counter.

Table 45–288—PCS FEC corrected codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.802.15:0	FEC corrected codewords lower	FEC_corrected_cw_counter[15:0]	RO, NR
3.803.15:0	FEC corrected codewords upper	FEC_corrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.63 PCS FEC uncorrected codewords counter (Register 3.804, 3.805)

The assignment of bits in the PCS FEC uncorrected codewords counter register is shown in Table 45–289. See 119.3.3 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 3.804, 3.805 are used to read the value of a 32-bit counter. When registers 3.804 and 3.805 are used to read the 32-bit counter value, the register 3.804 is read first, the value of the register 3.805 is latched when (and only when) register 3.804 is read, and reads of register 3.805 return the latched value rather than the current value of the counter.

Table 45–289—PCS FEC uncorrected codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.804.15:0	FEC uncorrected codewords lower	FEC_uncorrected_cw_counter[15:0]	RO, NR
3.805.15:0	FEC uncorrected codewords upper	FEC_uncorrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.3.64 PCS FEC degraded SER activate threshold register (Register 3.806, 3.807)

The assignment of bits in the PCS FEC degraded SER activate threshold register is shown in Table 45–290. The value controls the threshold used to set the PCS FEC degraded SER bit (3.801.4) as defined in 119.2.5.3.

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Table 45–290—PCS FEC degraded SER activate threshold register bit definitions

Bit(s)	Name	Description	R/W[a]
3.806.15:0	PCS FEC degraded SER activate threshold lower	FEC_degraded_SER_activate_threshold[15:0]	R/W
3.807.15:0	PCS FEC degraded SER activate threshold upper	FEC_degraded_SER_activate_threshold[31:16]	R/W

[a]R/W = Read/Write

45.2.3.65 PCS FEC degraded SER deactivate threshold register (Register 3.808, 3.809)

The assignment of bits in the PCS FEC degraded SER deactivate threshold register is shown in Table 45–291. The value controls the threshold used to clear the PCS FEC degraded SER bit (3.801.4) as defined in 119.2.5.3.

Table 45–291—PCS FEC degraded SER deactivate threshold register bit definitions

Bit(s)	Name	Description	R/W[a]
3.808.15:0	PCS FEC degraded SER deactivate threshold lower	FEC_degraded_SER_deactivate_threshold[15:0]	R/W
3.809.15:0	PCS FEC degraded SER deactivate threshold upper	FEC_degraded_SER_deactivate_threshold[31:16]	R/W

[a]R/W = Read/Write

45.2.3.66 PCS FEC degraded SER interval register (Register 3.810, 3.811)

The assignment of bits in the PCS FEC degraded SER interval register is shown in Table 45–292. The value controls the interval used to set and clear the PCS FEC degraded SER bit (3.801.4) as defined in 119.2.5.3.

Table 45–292—PCS FEC degraded SER interval register bit definitions

Bit(s)	Name	Description	R/W[a]
3.810.15:0	PCS FEC degraded SER interval lower	FEC_degraded_SER_interval[15:0]	R/W
3.811.15:0	PCS FEC degraded SER interval upper	FEC_degraded_SER_interval[31:16]	R/W

[a]R/W = Read/Write

45.2.3.67 TimeSync PCS capability (Register 3.1800)

The TimeSync PCS capability register (see Table 45–293) indicates the capability of the PCS to report the transmit and receive data delay, stored in registers 3.1801 through 3.1804 and 3.1805 through 3.1808, respectively.

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Table 45–293—TimeSync PCS capability

Bit(s)	Name	Description	R/W[a]
3.1800.15:2	Reserved	Value always 0	RO
3.1800.1	TimeSync transmit path data delay	1 = PCS provides information on transmit path data delay in registers 3.1801 through 3.1804 0 = PCS does not provide information on transmit path data delay	RO
3.1800.0	TimeSync receive path data delay	1 = PCS provides information on receive path data delay in registers 3.1805 through 3.1808 0 = PCS does not provide information on receive path data delay	RO

[a]RO = Read only

45.2.3.68 TimeSync PCS transmit path data delay (Registers 3.1801, 3.1802, 3.1803, 3.1804)

The TimeSync PCS transmit path data delay register contains the maximum (registers 3.1801, 3.1802, see Table 45–294) and minimum (registers 3.1803, 3.1804, see Table 45–294) values of the transmit path data delay. The transmit path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in register 1.1 (see 45.2.1.2.4).

Table 45–294—TimeSync PCS transmit path data delay register

Bit(s)	Name	Description	R/W[a]
3.1801.15:0	Maximum PCS transmit path data delay, lower	PCS_delay_TX_max [15:0]	RO, MW
3.1802.15:0	Maximum PCS transmit path data delay, upper	PCS_delay_TX_max [31:16]	RO, MW
3.1803.15:0	Minimum PCS transmit path data delay, lower	PCS_delay_TX_min [15:0]	RO, MW
3.1804.15:0	Minimum PCS transmit path data delay, upper	PCS_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.3.69 TimeSync PCS receive path data delay (Registers 3.1805, 3.1806, 3.1807, 3.1808)

The TimeSync PCS receive path data delay register contains the maximum (registers 3.1805, 3.1806, see Table 45–295) and minimum (registers 3.1807, 3.1808, see Table 45–295) values of the receive path data delay. The receive path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in register 1.1 (see 45.2.1.2.4).

Table 45–295—TimeSync PCS receive path data delay register

Bit(s)	Name	Description	R/W[a]
3.1805.15:0	Maximum PCS receive path data delay, lower	PCS_delay_RX_max [15:0]	RO, MW
3.1806.15:0	Maximum PCS receive path data delay, upper	PCS_delay_RX_max [31:16]	RO, MW
3.1807.15:0	Minimum PCS receive path data delay, lower	PCS_delay_RX_min [15:0]	RO, MW
3.1808.15:0	Minimum PCS receive path data delay, upper	PCS_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

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45.2.3.70 10BASE-T1L PCS control register (Register 3.2278)

The assignment of bits in the 10BASE-T1L PCS control register is shown in Table 45–296. The default value for each bit of the 10BASE-T1L PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–296—10BASE-T1L PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2278.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2278.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2278.13:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.70.1 PCS reset (3.2278.15)

Resetting the 10BASE-T1L PCS is accomplished by setting bit 3.2278.15 to one. This action shall set all 10BASE-T1L PCS registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1L PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 10BASE-T1L PCS shall return a value of one in bit 3.2278.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1L PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 3.2278.15. During a reset, a PCS shall respond to reads from bits 3.0.15, 3.8.15:14, and 3.2278.15. Reads for all other bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2278.15 is a copy of 3.0.15, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1L PCS.

45.2.3.70.2 Loopback (3.2278.14)

The 10BASE-T1L PCS shall be placed in a loopback mode of operation when bit 3.2278.14 is set to one. When in loopback mode, the 10BASE-T1L PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2278.14 is zero.

Bit 3.2278.14 is a copy of 3.0.14, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.3.71 10BASE-T1L PCS status register (Register 3.2279)

The assignment of bits in the 10BASE-T1L PCS status register is shown in Table 45–297. All the bits in the 10BASE-T1L PCS status register are read only; a write to the 10BASE-T1L PCS status register shall have no effect.

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Table 45–297—10BASE-T1L PCS status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2279.15:12	Reserved	Value always 0	RO
3.2279.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2279.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2279.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2279.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2279.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO/LH
3.2279.6:3	Reserved	Value always 0	RO
3.2279.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2279.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.3.71.1 Tx LPI received (3.2279.11)

When read as a one, bit 3.2279.11 indicates that the transmit 10BASE-T1L PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2279.11 indicates that the 10BASE-T1L PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.71.2 Rx LPI received (3.2279.10)

When read as a one, bit 3.2279.10 indicates that the receive 10BASE-T1L PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2279.10 indicates that the 10BASE-T1L PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.71.3 Tx LPI indication (3.2279.9)

When read as a one, bit 3.2279.9 indicates that the transmit 10BASE-T1L PCS is currently receiving LPI signals. When read as a zero, bit 3.2279.9 indicates that the 10BASE-T1L PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.71.4 Rx LPI indication (3.2279.8)

When read as a one, bit 3.2279.8 indicates that the receive 10BASE-T1L PCS is currently receiving LPI signals. When read as a zero, bit 3.2279.8 indicates that the 10BASE-T1L PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

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45.2.3.71.5 Fault (3.2279.7)

When read as a one, bit 3.2279.7 indicates that the 10BASE-T1L PCS has detected a fault condition on either the transmit or receive path. When read as a zero, bit 3.2279.7 indicates that the 10BASE-T1L PCS has not detected a fault condition. This bit shall be implemented with latching high behavior.

45.2.3.71.6 PCS receive link status (3.2279.2)

When read as a one, bit 3.2279.2 indicates that the 10BASE-T1L PCS receive link is up. When read as a zero, bit 3.2279.2 indicates that the 10BASE-T1L PCS receive link was down since the last read from this bit. This bit shall be implemented with latching low behavior and is a reflection of the variable scr_status. If the bit is read while scr_status = OK, then this bit is set. If scr_status = NOT_OK, then this bit is reset.

45.2.3.72 10BASE-T1S PCS control register (Register 3.2291)

The assignment of bits in the 10BASE-T1S PCS control register is shown in Table 45–298. The default value for each bit of the 10BASE-T1S PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–298—10BASE-T1S PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2291.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2291.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2291.13:9	Reserved	Value always 0	RO
3.2291.8	Duplex mode	1 = Set to half duplex 0 = Set to full duplex	R/W
3.2291.7:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.72.1 PCS reset (3.2291.15)

Resetting the 10BASE-T1S PCS is accomplished by setting bit 3.2291.15 to one. This action shall set all 10BASE-T1S PCS registers to their default states. As a consequence, this action may change the internal state of the 10BASE-T1S PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 10BASE-T1S PCS shall return a value of one in bit 3.2291.15 when a reset is in progress; otherwise, it shall return a value of zero. The 10BASE-T1S PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 3.2291.15. During a reset, a PCS shall respond to reads from bits 3.0.15, 3.8.15:14, and 3.2291.15. Reads for all other bits shall be ignored.

NOTE—This operation may interrupt data communication.

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Bit 3.2291.15 is a copy of 3.0.15, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 10BASE-T1S PCS.

45.2.3.72.2 Loopback (3.2291.14)

The 10BASE-T1S PCS shall be placed in a loopback mode of operation when bit 3.2291.14 is set to one. When in loopback mode, the 10BASE-T1S PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2291.14 is zero.

Bit 3.2291.14 is a copy of 3.0.14, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.3.72.3 Duplex mode (3.2291.8)

Bit 3.2291.8 is used to configure the PCS duplex_mode variable when not operating in Multidrop mode and when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. If bit 3.2291.8 is set to one, then duplex_mode is set to DUPLEX_HALF. If bit 3.2291.8 is set to zero, then duplex_mode is set to DUPLEX_FULL. This bit shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one or when bit 3.2292.6 indicates the PHY is not capable of full-duplex operation. If the PHY reports via bit 3.2292.6 that it is not capable of operating in full-duplex mode, the value of bit 3.2291.8 is undefined.

Bit 3.2291.8 is an inverted copy of bit 0.8 (see Table 22–7). When the PHY reports via bit 3.2292.6 that it is capable of operating in full-duplex mode, setting bit 0.8 or bit 3.2291.8 shall clear the other bit, and clearing bit 0.8 or bit 3.2291.8 shall set the other bit.

45.2.3.73 10BASE-T1S PCS status register (Register 3.2292)

The assignment of bits in the 10BASE-T1S PCS status register is shown in Table 45–299. All the bits in the 10BASE-T1S PCS status register are read only; a write to the 10BASE-T1S PCS status register shall have no effect.

Table 45–299—10BASE-T1S PCS status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2292.15:8	Reserved	Value always 0	RO
3.2292.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO/LH
3.2292.6	Full-duplex capability	1 = PHY capable of full-duplex operation 0 = PHY not capable of full-duplex operation	RO
3.2292.5:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

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45.2.3.73.1 Fault (3.2292.7)

When read as a one, bit 3.2292.7 indicates that the 10BASE-T1S PCS has detected a fault condition on either the transmit or receive path. When read as a zero, bit 3.2292.7 indicates that the 10BASE-T1S PCS has not detected a fault condition. This bit shall be implemented with latching high behavior.

45.2.3.73.2 Full-duplex capability (3.2292.6)

When read as a one, bit 3.2292.6 indicates that the 10BASE-T1S PHY is capable of full-duplex operation. When read as a zero, bit 3.2292.6 indicates that the 10BASE-T1S PHY is not capable of full-duplex operation.

45.2.3.74 10BASE-T1S PCS diagnostic 1 (Register 3.2293)

The assignment of bits in the 10BASE-T1S PCS diagnostic 1 register is shown in Table 45–300. All the bits in the 10BASE-T1S PCS diagnostic 1 register are read only and self-clear on read; a write to the 10BASE-T1S PCS diagnostic 1 register shall have no effect.

Table 45–300—10BASE-T1S PCS diagnostic 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2293.15:0	Remote jabber count	16-bit field counting the number of remote jabber errors received since last read of this register	RO, SC

[a]RO = Read only, SC = Self-clearing

45.2.3.74.1 Remote jabber count (3.2293.15:0)

Bits 3.2293.15:0 report the number of received jabber events since the last time register 3.2293 was read. The remote jabber count shall not wrap. When the maximum allowed value (65 535) is reached, the count stops until this register is cleared by a read operation.

45.2.3.75 10BASE-T1S PCS diagnostic 2 (Register 3.2294)

The assignment of bits in the 10BASE-T1S PCS diagnostic 2 register is shown in Table 45–301. All the bits in the 10BASE-T1S PCS diagnostic 2 register are read only and self-clear on read; a write to the 10BASE-T1S PCS diagnostic 2 register shall have no effect.

Table 45–301—10BASE-T1S PCS diagnostic 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2294.15:0	CorruptedTxCnt	16-bit field counting each time a transmission initiated locally results in a corrupted signal at the MDI since last read of this register	RO, SC

[a]RO = Read only, SC = Self-clearing

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45.2.3.75.1 CorruptedTxCnt (3.2294.15:0)

Bits 3.2294.15:0 count up at each positive edge of the MII signal COL. When the maximum allowed value (65 535) is reached, the count stops until this register is cleared by a read operation.

45.2.3.76 1000BASE-T1 PCS control register (Register 3.2304)

The assignment of bits in the 1000BASE-T1 PCS control register is shown in Table 45–302. The default value for each bit of the 1000BASE-T1 PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–302—1000BASE-T1 PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2304.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2304.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2304.13:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.76.1 PCS reset (3.2304.15)

Resetting the 1000BASE-T1 PCS is accomplished by setting bit 3.2304.15 to a one. This action shall set all 1000BASE-T1 PCS registers to their default states. As a consequence, this action may change the internal state of the 1000BASE-T1 PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 1000BASE-T1 PCS shall return a value of one in bit 3.2304.15 when a reset is in progress; otherwise, it shall return a value of zero. The 1000BASE-T1 PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface is restored to operation as defined in 97.3.2.1, starting when bit 3.2304.15 is set. During a reset, a PCS shall respond to reads from register bits 3.0.15, 3.8.15:14, and 3.2304.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2304.15 is a copy of 3.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 1000BASE-T1 PCS.

45.2.3.76.2 Loopback (3.2304.14)

The 1000BASE-T1 PCS shall be placed in a loopback mode of operation when bit 3.2304.14 is set to a one. When bit 3. 2304.14 is set to a one, the 1000BASE-T1 PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2304.14 is zero.

Bit 3.2304.14 is a copy of 3.0.14 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

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45.2.3.77 1000BASE-T1 PCS status 1 register (Register 3.2305)

The assignment of bits in the 1000BASE-T1 PCS status 1 register is shown in Table 45–303. All the bits in the 1000BASE-T1 PCS status 1 register are read only; a write to the 1000BASE-T1 PCS status 1 register shall have no effect.

Table 45–303—1000BASE-T1 PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2305.15:12	Reserved	Value always 0	RO
3.2305.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2305.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2305.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2305.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2305.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2305.6:3	Reserved	Value always 0	RO
3.2305.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2305.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.3.77.1 Tx LPI received (3.2305.11)

When read as a one, bit 3.2305.11 indicates that the transmit 1000BASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2305.11 indicates that the 1000BASE-T1 PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.77.2 Rx LPI received (3.2305.10)

When read as a one, bit 3.2305.10 indicates that the receive 1000BASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2305.10 indicates that the 1000BASE-T1 PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.77.3 Tx LPI indication (3.2305.9)

When read as a one, bit 3.2305.9 indicates that the transmit 1000BASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2305.9 indicates that the 1000BASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

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45.2.3.77.4 Rx LPI indication (3.2305.8)

When read as a one, bit 3.2305.8 indicates that the receive 1000BASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2305.8 indicates that the 1000BASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.77.5 Fault (3.2305.7)

When read as a one, bit 3.2305.7 indicates that the 1000BASE-T1 PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.2305.7 indicates that the 1000BASE-T1 PCS has not detected a fault condition.

45.2.3.77.6 PCS receive link status (3.2305.2)

When read as a one, bit 3.2305.2 indicates that the 1000BASE-T1 PCS receive link is up. When read as a zero, bit 3.2305.2 indicates that the 1000BASE-T1 PCS receive link was down since the last read from this register. This bit is a latching low version of bit 3.2306.10. The PCS receive link status bit shall be implemented with latching low behavior.

45.2.3.78 1000BASE-T1 PCS status 2 register (Register 3.2306)

The assignment of bits in the 1000BASE-T1 PCS status 2 register is shown in Table 45–304. All the bits in the 1000BASE-T1 PCS status 2 register are read only; a write to the 1000BASE-T1 PCS status 2 register shall have no effect.

Table 45–304—1000BASE-T1 PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2306.15:11	Reserved	Value always 0	RO
3.2306.10	Receive link status	1 = PCS receive link up 0 = PCS receive link down	RO
3.2306.9	PCS high BER	1 = PCS reporting a high BER 0 = PCS not reporting a high BER	RO
3.2306.8	PCS block lock	1 = PCS locked to received blocks 0 = PCS not locked to received blocks	RO
3.2306.7	Latched high BER	1 = PCS has reported a high BER 0 = PCS has not reported a high BER	RO/LH
3.2306.6	Latched block lock	1 = PCS has block lock 0 = PCS does not have block lock	RO/LL
3.2306.5:0	BER count	BER counter	RO/NR

[a]RO = Read only, LH = Latching High, LL = Latching Low, NR = Non Roll-over

45.2.3.78.1 Receive link status (3.2306.10)

When read as a one, bit 3.2306.10 indicates that the 1000BASE-T1 PCS is in a fully operational state. When read as a zero, bit 3.2306.10 indicates that the 1000BASE-T1 PCS is not fully operational. This bit is a reflection of the PCS_status variable defined in 97.3.7.1.

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45.2.3.78.2 PCS high BER (3.2306.9)

When read as a one, bit 3.2306.9 indicates that the 1000BASE-T1 PCS receiver is detecting a BER of $> 4 \times 10^{-4}$. When read as a zero, bit 3.2306.9 indicates that the 1000BASE-T1 PCS is not detecting a BER of $> 4 \times 10^{-4}$. This bit is a reflection of the state of the hi_rfer variable defined in 97.3.7.1.

45.2.3.78.3 PCS block lock (3.2306.8)

When read as a one, bit 3.2306.8 indicates that the 1000BASE-T1 PCS receiver has block lock. When read as a zero, bit 3.2306.8 indicates that the 1000BASE-T1 PCS receiver has not achieved block lock. This bit is a reflection of the state of the block_lock variable defined in 97.3.7.1.

45.2.3.78.4 Latched high BER (3.2306.7)

When read as a one, bit 3.2306.7 indicates that the 1000BASE-T1 PCS has detected a high BER one or more times since the register was last read. When read as a zero, bit 3.2306.7 indicates that the 1000BASE-T1 PCS has not detected a high BER. The latched high BER bit shall be implemented with latching high behavior. This bit is a latching high version of the 1000BASE-T1 PCS high BER status bit (3.2306.9).

45.2.3.78.5 Latched block lock (3.2306.6)

When read as a one, bit 3.2306.6 indicates that the 1000BASE-T1 PCS has achieved block lock. When read as a zero, bit 3.2306.6 indicates that the 1000BASE-T1 PCS has lost block lock one or more times since the register was last read. The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 1000BASE-T1 PCS block lock status bit (3.2306.8).

45.2.3.78.6 BER count (3.2306.5:0)

The BER counter formed by bits 3.2306.5:0 is a six bit count as defined by RFER_count in 97.3.7.2. These bits shall be reset to all zeros when the 1000BASE-T1 PCS status 2 register is read by the management function or upon execution of the 1000BASE-T1 PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.79 BASE-T1 OAM transmit register (Register 3.2308)

The assignment of bits in the BASE-T1 OAM transmit register is shown in Table 45–305.

Table 45–305—BASE-T1 OAM transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2308.15	BASE-T1 OAM message valid	This bit is used to indicate message data in registers 3.2308.11:8, 3.2309, 3.2310, 3.2311, and 3.2312 are valid and ready to be loaded. This bit self-clears when registers are loaded by the OAM transmit state diagram. 1 = Message data in registers are valid 0 = Message data in registers are not valid	R/W, SC
3.2308.14	Toggle value	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.	RO

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Table 45–305—BASE-T1 OAM transmit register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.2308.13	BASE-T1 OAM message received	This bit shall self clear on read. 1 = BASE-T1 OAM message received by link partner 0 = BASE-T1 OAM message not received by link partner	RO, LH
3.2308.12	Received message toggle value	Toggle value of message that was received by link partner as indicated in 3.2308.13.	RO
3.2308.11:8	Message number	User-defined message number to send	R/W
3.2308.7:4	Reserved	Value always 0	RO
3.2308.3	Ping received	Received PingTx value from latest good BASE-T1 OAM frame received	RO
3.2308.2	Ping transmit	Ping value to send to link partner	R/W
3.2308.1:0	Local SNR	00 = PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.	RO

[a]RO = Read only, R/W = Read/Write, LH = Latching High, SC = Self-clearing

45.2.3.79.1 BASE-T1 OAM message valid (3.2308.15)

Bit 3.2308.15 shall be set to one when the BASE-T1 OAM message to be transmitted in registers 3.2309, 3.2310, 3.2311, and 3.2312 and the message number in 3.2308.11:8 are properly configured to be transmitted. Bit 3.2308.15 self-clears to indicate whether the next BASE-T1 OAM message can be written into the registers.

45.2.3.79.2 Toggle value (3.2308.14)

The state machine shall assign a value alternating between zero and one to associate with the 8-octet BASE-T1 OAM message transmitted by the PHY. Bit 3.2308.14 should be read and recorded prior to setting 3.2308.15 to one. The recorded value can be correlated with 3.2308.12 as a confirmation that the BASE-T1 OAM message is received by the link partner.

45.2.3.79.3 BASE-T1 OAM message received (3.2308.13)

Bit 3.2308.13 shall indicate whether the most recently transmitted BASE-T1 OAM message with a toggle bit value in 3.2308.12 was received, read, and acknowledged by the link partner. This variable shall clear on read.

45.2.3.79.4 Received message toggle value (3.2308.12)

Bit 3.2308.12 indicates the toggle bit value of the BASE-T1 OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if 3.2308.13 is one.

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45.2.3.79.5 Message number (3.2308.11:8)

Bits 3.2308.11:8 contain the BASE-T1 OAM message number to be transmitted. This field is user defined but it is recommended that it be used to indicate the meaning of the 8-octet BASE-T1 OAM message. If used this way, up to 16 different 8-octet messages can be exchanged. The message number is user defined and its definition is outside the scope of this standard.

45.2.3.79.6 Ping received (3.2308.3)

Bit 3.2308.3 represents the value of the most recent Ping RX received from the link partner (see 97.3.8.2.3).

45.2.3.79.7 Ping transmit (3.2308.2)

Bit 3.2308.2 represents the value to be sent to the link partner via the Ping TX function (see 97.3.8.2.4).

45.2.3.79.8 Local SNR (3.2308.1:0)

Bits 3.2308.1:0 are set by the BASE-T1 PHY to indicate the status of the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.80 BASE-T1 OAM message register (Registers 3.2309 to 3.2312)

The BASE-T1 OAM message register contains the 8-octet BASE-T1 OAM message data to be transmitted. The 8-octet message data is user defined and its definition is outside the scope of this standard. See Table 45–306.

Table 45–306—BASE-T1 OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2309.15:8	BASE-T1 OAM message 1	Message octet 1. LSB transmitted first.	R/W
3.2309.7:0	BASE-T1 OAM message 0	Message octet 0. LSB transmitted first.	R/W
3.2310.15:8	BASE-T1 OAM message 3	Message octet 3. LSB transmitted first.	R/W
3.2310.7:0	BASE-T1 OAM message 2	Message octet 2. LSB transmitted first.	R/W
3.2311.15:8	BASE-T1 OAM message 5	Message octet 5. LSB transmitted first.	R/W
3.2311.7:0	BASE-T1 OAM message 4	Message octet 4. LSB transmitted first.	R/W
3.2312.15:8	BASE-T1 OAM message 7	Message octet 7. LSB transmitted first.	R/W
3.2312.7:0	BASE-T1 OAM message 6	Message octet 6. LSB transmitted first.	R/W

[a]R/W = Read/Write

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45.2.3.81 BASE-T1 OAM receive register (Register 3.2313)

The assignment of bits in the BASE-T1 OAM receive register is shown in Table 45–307.

Table 45–307—BASE-T1 OAM receive register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2313.15	Link partner BASE-T1 OAM message valid	This bit is used to indicate message data in registers 3.2313.11:8, 3.2314, 3.2315, 3.2316, and 3.2317 are stored and ready to be read. See 45.2.3.81.1 for self-clearing behavior. 1 = Message data in registers are valid 0 = Message data in registers are not valid	RO, SC
3.2313.14	Link partner toggle value	Toggle value received with message.	RO
3.2313.13:12	Reserved	Value always 0	RO
3.2313.11:8	Link partner message number	Message number from link partner	RO
3.2313.7:2	Reserved	Value always 0	RO
3.2313.1:0	Link partner SNR	00 = Link partner link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain link partner SNR. Link partner requests local PHY to exit LPI and send idles (used only when EEE is enabled). 10 = Link partner SNR is marginal. 11 = Link partner SNR is good.	RO

[a]RO = Read only, SC = Self-clearing

45.2.3.81.1 Link partner BASE-T1 OAM message valid (3.2313.15)

Bit 3.2313.15 shall be set to one when the BASE-T1 OAM message from the link partner is stored into registers 3.2314, 3.2315, 3.2316, and 3.2317 and the message number in 3.2313.11:8. Bit 3.2313.15 shall self-clear when register 3.2317 is read.

45.2.3.81.2 Link partner toggle value (3.2313.14)

Bit 3.2313.14 indicates the toggle value associated with the 8-octet BASE-T1 OAM message from the link partner.

45.2.3.81.3 Link partner message number (3.2313.11:8)

Bits 3.2313.11:8 contain the BASE-T1 OAM message number from the link partner.

45.2.3.81.4 Link partner SNR (3.2313.1:0)

Bits 3.2313.1:0 indicate the status of the link partner receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

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45.2.3.82 Link partner BASE-T1 OAM message register (Registers 3.2314 to 3.2317)

The link partner BASE-T1 OAM message register contains the 8-octet BASE-T1 OAM message data from the link partner. See Table 45–308.

Table 45–308—Link partner BASE-T1 OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2314.15:8	Link partner BASE-T1 OAM message 1	Message octet 1. LSB received first.	RO
3.2314.7:0	Link partner BASE-T1 OAM message 0	Message octet 0. LSB received first.	RO
3.2315.15:8	Link partner BASE-T1 OAM message 3	Message octet 3. LSB received first.	RO
3.2315.7:0	Link partner BASE-T1 OAM message 2	Message octet 2. LSB received first.	RO
3.2316.15:8	Link partner BASE-T1 OAM message 5	Message octet 5. LSB received first.	RO
3.2316.7:0	Link partner BASE-T1 OAM message 4	Message octet 4. LSB received first.	RO
3.2317.15:8	Link partner BASE-T1 OAM message 7	Message octet 7. LSB received first.	RO
3.2317.7:0	Link partner BASE-T1 OAM message 6	Message octet 6. LSB received first.	RO

[a]RO = Read only

45.2.3.83 MultiGBASE-T1 OAM status message register (Register 3.2318 and 3.2319)

The MultiGBASE-T1 OAM status message register contains octets 8 through 11 of the MultiGBASE-T1 OAM message data to be transmitted. See 149.3.9.2.12 for details on the OAM status message definition. See Table 45–309.

Table 45–309—MultiGBASE-T1 OAM status message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2318.15:8	MultiGBASE-T1 OAM status message 9	Message octet 9. LSB transmitted first.	R/W
3.2318.7:0	MultiGBASE-T1 OAM status message 8	Message octet 8. LSB transmitted first.	R/W
3.2319.15:8	MultiGBASE-T1 OAM status message 11	Message octet 11. LSB transmitted first.	R/W
3.2319.7:0	MultiGBASE-T1 OAM status message 10	Message octet 10. LSB transmitted first.	R/W

[a]R/W = Read/Write

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45.2.3.84 Link partner MultiGBASE-T1 OAM status message register (Register 3.2320 and 3.2321)

The link partner MultiGBASE-T1 OAM status message register contains octets 8 through 11 of the MultiGBASE-T1 OAM message data from the link partner. See 149.3.9.2.12 for details on the OAM status message definition. See Table 45–310.

Table 45–310—Link partner MultiGBASE-T1 OAM status message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2320.15:8	Link partner MultiGBASE-T1 OAM status message 9	Message octet 9. LSB received first.	RO
3.2320.7:0	Link partner MultiGBASE-T1 OAM status message 8	Message octet 8. LSB received first.	RO
3.2321.15:8	Link partner MultiGBASE-T1 OAM status message 11	Message octet 11. LSB received first.	RO
3.2321.7:0	Link partner MultiGBASE-T1 OAM status message 10	Message octet 10. LSB received first.	RO

[a]RO = Read only

45.2.3.85 MultiGBASE-T1 PCS control register (Register 3.2322)

The assignment of bits in the MultiGBASE-T1 PCS control register is shown in Table 45–311. The default value for each bit of the MultiGBASE-T1 PCS control register is chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–311—MultiGBASE-T1 PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2322.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2322.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2322.13:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.85.1 PCS reset (3.2322.15)

Resetting the MultiGBASE-T1 PCS is accomplished by setting bit 3.2322.15 to a one. This action shall set all MultiGBASE-T1 PCS registers to their default states. As a consequence, this action may change the internal state of the MultiGBASE-T1 PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. Bit 3.2322.15 is self-clearing, and the MultiGBASE-T1 PCS shall return a value of one in bit 3.2322.15 when a reset is in progress; otherwise, it shall return a value of zero. The MultiGBASE-T1 PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface is restored to

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operation as defined in 149.3.2.1 starting when bit 3.2322.15 is set. During a reset, a PCS shall respond to reads from register bits 3.0.15, 3.8.15:14, and 3.2322.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2322.15 is a copy of 3.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the MultiGBASE-T1 PCS.

45.2.3.85.2 Loopback (3.2322.14)

The MultiGBASE-T1 PCS shall be placed in a loopback mode of operation when bit 3.2322.14 is set to a one. When bit 3.2322.14 is set to a one, the MultiGBASE-T1 PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2322.14 is zero.

Bit 3.2322.14 is a copy of 3.0.14 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.3.86 MultiGBASE-T1 PCS status 1 register (Register 3.2323)

The assignment of bits in the MultiGBASE-T1 PCS status 1 register is shown in Table 45–312. All the bits in the MultiGBASE-T1 PCS status 1 register are read only; a write to the MultiGBASE-T1 PCS status 1 register shall have no effect.

Table 45–312—MultiGBASE-T1 PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2323.15:12	Reserved	Value always 0	RO
3.2323.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2323.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2323.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2323.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2323.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2323.6:3	Reserved	Value always 0	RO
3.2323.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2323.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

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45.2.3.86.1 Tx LPI received (3.2323.11)

When read as a one, bit 3.2323.11 indicates that the transmit MultiGBASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2323.11 indicates that the transmit MultiGBASE-T1 PCS has not received LPI signaling. Bit 3.2323.11 shall be implemented with latching high behavior.

45.2.3.86.2 Rx LPI received (3.2323.10)

When read as a one, bit 3.2323.10 indicates that the receive MultiGBASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2323.10 indicates that the receive MultiGBASE-T1 PCS has not received LPI signaling. Bit 3.2323.10 shall be implemented with latching high behavior.

45.2.3.86.3 Tx LPI indication (3.2323.9)

When read as a one, bit 3.2323.9 indicates that the transmit MultiGBASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2323.9 indicates that the transmit MultiGBASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.86.4 Rx LPI indication (3.2323.8)

When read as a one, bit 3.2323.8 indicates that the receive MultiGBASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2323.8 indicates that the receive MultiGBASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.86.5 Fault (3.2323.7)

When read as a one, bit 3.2323.7 indicates that the MultiGBASE-T1 PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.2323.7 indicates that the MultiGBASE-T1 PCS has not detected a fault condition.

45.2.3.86.6 PCS receive link status (3.2323.2)

When read as a one, bit 3.2323.2 indicates that the MultiGBASE-T1 PCS receive link is up. When read as a zero, bit 3.2323.2 indicates that the MultiGBASE-T1 PCS receive link was down since the last read from this register. Bit 3.2323.2 is a latching low version of bit 3.2324.10. The PCS receive link status bit shall be implemented with latching low behavior.

45.2.3.87 MultiGBASE-T1 PCS status 2 register (Register 3.2324)

The assignment of bits in the MultiGBASE-T1 PCS status 2 register is shown in Table 45–313. All the bits in the MultiGBASE-T1 PCS status 2 register are read only; a write to the MultiGBASE-T1 PCS status 2 register shall have no effect.

45.2.3.87.1 Receive link status (3.2324.10)

When read as a one, bit 3.2324.10 indicates that the MultiGBASE-T1 PCS is in a fully operational state. When read as a zero, bit 3.2324.10 indicates that the MultiGBASE-T1 PCS is not fully operational. Bit 3.2324.10 is a reflection of the pcs_status variable defined in 149.3.8.1.

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Table 45–313—MultiGBASE-T1 PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2324.15:11	Reserved	Value always 0	RO
3.2324.10	Receive link status	1 = PCS receive link up 0 = PCS receive link down	RO
3.2324.9	PCS high RFER	1 = PCS reporting a high RFER 0 = PCS not reporting a high RFER	RO
3.2324.8	PCS block lock	1 = PCS locked to received blocks 0 = PCS not locked to received blocks	RO
3.2324.7	Latched high BER	1 = PCS has reported a high BER 0 = PCS has not reported a high BER	RO/LH
3.2324.6	Latched block lock	1 = PCS has block lock 0 = PCS does not have block lock	RO/LL
3.2324.5:0	BER count	Count of RS-FEC frame errors since last read	RO/NR

[a]RO = Read only, LH = Latching High, LL = Latching Low, NR = Non Roll-over

45.2.3.87.2 PCS high RFER (3.2324.9)

When read as a one, bit 3.2324.9 indicates that the MultiGBASE-T1 PCS receiver is detecting 16 or more RS-FEC errored blocks in 312 500 bit times (one rfer_timer interval). When read as a zero, bit 3.2324.9 indicates that the MultiGBASE-T1 PCS is detecting fewer than 16 RS-FEC errored blocks in 312 500 bit times. Bit 3.2324.9 is a reflection of the state of the hi_rfer variable defined in 149.3.8.1.

45.2.3.87.3 PCS block lock (3.2324.8)

When read as a one, bit 3.2324.8 indicates that the MultiGBASE-T1 PCS receiver has block lock. When read as a zero, bit 3.2324.8 indicates that the MultiGBASE-T1 PCS receiver has not achieved block lock. Bit 3.2324.8 is a reflection of the state of the block_lock variable defined in 149.3.8.1.

45.2.3.87.4 Latched high BER (3.2324.7)

When read as a one, bit 3.2324.7 indicates that the MultiGBASE-T1 PCS has detected a high BER one or more times since the register was last read. When read as a zero, bit 3.2324.7 indicates that the MultiGBASE-T1 PCS has not detected a high BER. The latched high BER bit shall be implemented with latching high behavior. Bit 3.2324.7 is a latching high version of the MultiGBASE-T1 PCS high RFER status bit (3.2324.9).

45.2.3.87.5 Latched block lock (3.2324.6)

When read as a one, bit 3.2324.6 indicates that the MultiGBASE-T1 PCS has achieved block lock. When read as a zero, bit 3.2324.6 indicates that the MultiGBASE-T1 PCS has lost block lock one or more times since the register was last read. The latched block lock bit shall be implemented with latching low behavior.

Bit 3.2324.6 is a latching low version of the MultiGBASE-T1 PCS block lock status bit (3.2324.8).

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45.2.3.87.6 BER count (3.2324.5:0)

The BER counter formed by bits 3.2324.5:0 is a six bit counter as defined by RFER_count in 149.3.8.2. These bits shall be reset to all zeros when the MultiGBASE-T1 PCS status 2 register is read by the management function or upon execution of the MultiGBASE-T1 PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.4 PHY XS registers

The assignment of registers in the PHY XS is shown in Table 45–314.

Table 45–314—PHY XS registers

Register address	Register name	Subclause
4.0	PHY XS control 1	45.2.4.1
4.1	PHY XS status 1	45.2.4.2
4.2, 4.3	PHY XS device identifier	45.2.4.3
4.4	PHY XS speed ability	45.2.4.4
4.5, 4.6	PHY XS devices in package	45.2.4.5
4.7	Reserved	
4.8	PHY XS status 2	45.2.4.6
4.9 through 4.13	Reserved	
4.14, 4.15	PHY XS package identifier	45.2.4.7
4.16 through 4.19	Reserved	
4.20	EEE capability	45.2.4.8
4.21	Reserved	
4.22	EEE wake error counter	45.2.4.9
4.23	Reserved	
4.24	10G PHY XGXS lane status	45.2.4.10
4.25	10G PHY XGXS test control	45.2.4.11
4.26 through 4.31	Reserved	
4.32	BASE-R PHY XS status 1	45.2.4.12
4.33 through 4.41	Reserved	
4.42	BASE-R PHY XS test pattern control	45.2.4.13
4.43 through 4.49	Reserved	
4.50	Multi-lane BASE-R PHY XS alignment status 1	45.2.4.14
4.51	Reserved	
4.52	Multi-lane BASE-R PHY XS alignment status 3	45.2.4.15
4.53	Multi-lane BASE-R PHY XS alignment status 4	45.2.4.16
4.54	Reserved	

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Table 45–314—PHY XS registers *(continued)*

Register address	Register name	Subclause
4.400 through 4.415	PHY XS lane mapping, lane 0 through 15	45.2.4.17, 45.2.4.18
4.415 through 4.599	Reserved	
4.600 through 4.631	PHY XS FEC symbol error counter, lane 0 to 15	45.2.4.19, 45.2.4.20
4.632 through 4.799	Reserved	
4.800	PHY XS FEC control	45.2.4.21
4.801	PHY XS FEC status	45.2.4.22
4.802, 4.803	PHY XS FEC corrected codewords counter	45.2.4.23
4.804, 4.805	PHY XS FEC uncorrected codewords counter	45.2.4.24
4.806, 4.807	PHY XS FEC degraded SER activate threshold	45.2.4.25
4.808, 4.809	PHY XS FEC degraded SER deactivate threshold	45.2.4.26
4.810, 4.811	PHY XS FEC degraded SER interval	45.2.4.27
4.812 through 4.1799	Reserved	
4.1800	TimeSync PHY XS capability	45.2.4.28
4.1801 through 4.1804	TimeSync PHY XS transmit path data delay	45.2.4.29
4.1805 through 4.1808	TimeSync PHY XS receive path data delay	45.2.4.30
4.1809 through 4.32767	Reserved	
4.32 768 through 4.65 535	Vendor specific	

45.2.4.1 PHY XS control 1 register (Register 4.0)

The assignment of bits in the PHY XS control 1 register is shown in Table 45–315. The default value for each bit of the PHY XS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–315—PHY XS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.0.15	Reset	1 = PHY XS reset 0 = Normal operation	R/W SC
4.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
4.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
4.0.12	Reserved	Value always 0	RO

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Table 45–315—PHY XS control 1 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
4.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
4.0.10	Clock stop enable	1 = The PHY XS may stop the clock during LPI 0 = Clock not stoppable	R/W
4.0.9	XAUI stop enable	1 = The PHY XS may stop XAUI signals during LPI 0 = XAUI not stoppable	R/W
4.0.8:7	Reserved	Value always 0	RO
4.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
4.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 1 = Reserved 1 0 1 0 = 400 Gb/s 1 0 0 1 = 200 Gb/s 1 0 0 0 = Reserved 0 1 x x = Reserved 0 0 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
4.0.1:0	Reserved	Value always 0	RO

[a]R/W = Read/Write, SC = Self-clearing, RO = Read only

45.2.4.1.1 Reset (4.0.15)

Resetting a PHY XS is accomplished by setting bit 4.0.15 to a one. This action shall set all PHY XS registers to their default states. As a consequence, this action may change the internal state of the PHY XS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PHY XS shall return a value of one in bit 4.0.15 when a reset is in progress and a value of zero otherwise. A PHY XS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 4.0.15. During a reset, a PHY XS shall respond to reads from register bits 4.0.15 and 4.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.4.1.2 Loopback (4.0.14)

The PHY XS shall be placed in a loopback mode of operation when bit 4.0.14 is set to a one. When bit 4.0.14 is set to a one, the PHY XS shall accept data on the receive path and return it on the transmit path. The direction of the loopback path for the PHY XS is opposite to all other MMD loopbacks.

The loopback function is optional. A device's ability to perform the loopback function is advertised in the loopback ability bit of the related speed-dependent status register. A PHY XS that is unable to perform the loopback function shall ignore writes to this bit and return a value of zero when read. For 10 Gb/s operation,

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the loopback functionality is detailed in 48.3.3 and the loopback ability bit is specified in the 10G PHY XGXS Lane status register.

The default value of bit 4.0.14 is zero.

NOTE—The signal path through the PHY XS that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PHY XS circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.4.1.3 Low power (4.0.11)

A PHY XS may be placed into a low-power mode by setting bit 4.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PHY XS. The behavior of the PHY XS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 4.0.11 is zero.

45.2.4.1.4 Clock stop enable (4.0.10)

If bit 4.0.10 is set to one, then the PHY XS may stop the transmit direction xMII clock while it is signaling LPI, otherwise it shall keep the clock active. If the PHY XS does not support EEE capability or is not able to stop the transmit clock, then this bit has no effect (see 46.3.2.4).

45.2.4.1.5 XAUI stop enable (4.0.9)

If bit 4.0.9 is set to one, then the PHY XS may stop signaling on the XAUI in the receive direction during LPI, otherwise the PHY XS shall keep the XAUI signals active. If the PHY XS does not support EEE capability or is not able to stop the receive path XAUI signals, then this bit has no effect.

45.2.4.1.6 Speed selection (4.0.13, 4.0.6, 4.0.5:2)

Speed selection bits 4.0.13 and 4.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PHY XS may be selected using bits 5 through 2. The speed abilities of the PHY XS are advertised in the PHY XS speed ability register. A PHY XS may ignore writes to the PHY XS speed selection bits that select speeds it has not advertised in the PHY XS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PHY XS speed selection defaults to a supported ability.

45.2.4.2 PHY XS status 1 register (Register 4.1)

The assignment of bits in the PHY XS status 1 register is shown in Table 45–316. All the bits in the PHY XS status 1 register are read only; a write to the PHY XS status 1 register shall have no effect.

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Table 45–316—PHY XS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.1.15:12	Reserved	Value always 0	RO
4.1.11	Tx LPI received	1 = Tx PHY XS has received LPI 0 = LPI not received	RO/LH
4.1.10	Rx LPI received	1 = Rx PHY XS has received LPI 0 = LPI not received	RO/LH
4.1.9	Tx LPI indication	1 = Tx PHY XS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
4.1.8	Rx LPI indication	1 = Rx PHY XS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
4.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
4.1.6	Clock stop capable	1 = The attached PHY may stop the clock during LPI 0 = Clock not stoppable	RO
4.1.5:3	Reserved	Value always 0	RO
4.1.2	PHY XS transmit link status	1 = The PHY XS transmit link is up 0 = The PHY XS transmit link is down	RO/LL
4.1.1	Low-power ability	1 = PHY XS supports low-power mode 0 = PHY XS does not support low-power mode	RO
4.1.0	Reserved	Value always 0	RO

[a]RO = Read only, LL = Latching low, LH = Latching high

45.2.4.2.1 Transmit LPI received (4.1.11)

When read as a one, bit 4.1.11 indicates that the transmit PHY XS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 4.1.11 indicates that the PHY XS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.4.2.2 Receive LPI received (4.1.10)

When read as a one, bit 4.1.10 indicates that the receive PHY XS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 4.1.10 indicates that the PHY XS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.4.2.3 Transmit LPI indication (4.1.9)

When read as a one, bit 4.1.9 indicates that the transmit PHY XS is currently receiving LPI signals. When read as a zero, bit 4.1.9 indicates that the PHY XS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

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45.2.4.2.4 Receive LPI indication (4.1.8)

When read as a one, bit 4.1.8 indicates that the receive PHY XS is currently receiving LPI signals. When read as a zero, bit 4.1.8 indicates that the PHY XS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.4.2.5 Fault (4.1.7)

When read as a one, bit 4.1.7 indicates that the PHY XS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 4.1.7 indicates that the PHY XS has not detected a fault condition. Bit 4.1.7 is set to a one when either of the fault bits (4.8.11, 4.8.10) located in register 4.8 are set to a one.

45.2.4.2.6 Clock stop capable (4.1.6)

If bit 4.1.6 is set to one then the PHY XS is indicating that the attached PHY is permitted to stop the receive direction xMII clock while it is signaling LPI. If the bit is set to zero then the PHY XS is indicating that the attached PHY is not permitted to stop the receive xMII clock while it is signaling LPI. If the attached PHY does not support EEE capability or is not able to stop the receive direction xMII clock then this bit has no effect (see 46.3.2.4).

45.2.4.2.7 PHY XS transmit link status (4.1.2)

When read as a one, bit 4.1.2 indicates that the PHY XS transmit link is aligned. When read as a zero, bit 4.1.2 indicates that the PHY XS transmit link is not aligned. The transmit link status bit shall be implemented with latching low behavior.

For 10 Gb/s operation, bit 4.1.2 is a latching low version of bit 4.24.12.

45.2.4.2.8 Low-power ability (4.1.1)

When read as a one, bit 4.1.1 indicates that the PHY XS supports the low-power feature. When read as a zero, bit 4.1.1 indicates that the PHY XS does not support the low-power feature. If a PHY XS supports the low-power feature then it is controlled using the low-power bit in the PHY XS control register.

45.2.4.3 PHY XS device identifier (Registers 4.2 and 4.3)

Registers 4.2 and 4.3 provide a 32-bit value, which may constitute a unique identifier for a PHY XS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PHY XS may return a value of zero in each of the 32 bits of the PHY XS device identifier.

The format of the PHY XS device identifier is specified in 22.2.4.3.1.

45.2.4.4 PHY XS speed ability (Register 4.4)

The assignment of bits in the PHY XS speed ability register is shown in Table 45–317.

45.2.4.4.1 400G capable (4.4.9)

When read as a one, bit 4.4.9 indicates that the PHY XS is able to operate at a data rate of 400 Gb/s. When read as a zero, bit 4.4.9 indicates that the PHY-XS is not able to operate at a data rate of 400 Gb/s.

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Table 45–317—PHY XS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
4.4.15:10	Reserved	Value always 0	RO
4.4.9	400G capable	1 = PHY XS is capable of operating at 400 Gb/s 0 = PHY XS is not capable of operating at 400 Gb/s	RO
4.4.8	200G capable	1 = PHY XS is capable of operating at 200 Gb/s 0 = PHY XS is not capable of operating at 200 Gb/s	RO
4.4.7:1	Reserved	Value always 0	RO
4.4.0	10G capable	1 = PHY XS is capable of operating at 10 Gb/s 0 = PHY XS is not capable of operating at 10 Gb/s	RO

[a]RO = Read only

45.2.4.4.2 200G capable (4.4.8)

When read as a one, bit 4.4.8 indicates that the PHY XS is able to operate at a data rate of 200 Gb/s. When read as a zero, bit 4.4.8 indicates that the PHY-XS is not able to operate at a data rate of 200 Gb/s.

45.2.4.4.3 10G capable (4.4.0)

When read as a one, bit 4.4.0 indicates that the PHY XS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 4.4.0 indicates that the PHY-XS is not able to operate at a data rate of 10 Gb/s.

45.2.4.5 PHY XS devices in package (Registers 4.5 and 4.6)

The PHY XS devices in package registers are defined in Table 45–2.

45.2.4.6 PHY XS status 2 register (Register 4.8)

The assignment of bits in the PHY XS status 2 register is shown in Table 45–318. All the bits in the PHY XS status 2 register are read only; a write to the PHY XS status 2 register shall have no effect.

Table 45–318—PHY XS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
4.8.13:12	Reserved	Value always 0	RO
4.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH

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Table 45–318—PHY XS status 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
4.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
4.8.9:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

45.2.4.6.1 Device present (4.8.15:14)

When read as <10>, bits 4.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 4.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.4.6.2 Transmit fault (4.8.11)

When read as a one, bit 4.8.11 indicates that the PHY XS has detected a fault condition on the transmit path. When read as a zero, bit 4.8.11 indicates that the PHY XS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

The default value for bit 4.8.11 is zero.

45.2.4.6.3 Receive fault (4.8.10)

When read as a one, bit 4.8.10 indicates that the PHY XS has detected a fault condition on the receive path. When read as a zero, bit 4.8.10 indicates that the PHY XS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 4.8.10 is zero.

45.2.4.7 PHY XS package identifier (Registers 4.14 and 4.15)

Registers 4.14 and 4.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PHY XS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PHY XS may return a value of zero in each of the 32 bits of the PHY XS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the PHY XS package identifier is specified in 22.2.4.3.1.

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45.2.4.8 EEE capability (Register 4.20)

This register is used to indicate the capability of the PHY XS to support EEE functions. The assignment of bits in the EEE capability register is shown in Table 45–319.

Table 45–319—EEE capability register bit definitions

Bit(s)	Name	Description	R/W[a]
4.20.15:5	Reserved	Value always 0	RO
4.20.4	PHY XS EEE	1 = EEE is supported for PHY XS 0 = EEE is not supported for PHY XS	RO
4.20.3:1	Reserved	Value always 0	RO
4.20.0	XAUI stop capable	1 = The DTE XS may stop XAUI signals during LPI 0 = XAUI signals not stoppable	RO

[a] RO = Read only

45.2.4.8.1 PHY XS EEE supported (4.20.4)

If the device supports EEE operation for PHY XS as defined in 48.2, this bit shall be set to one.

45.2.4.8.2 XAUI stop capable (4.20.0)

If bit 4.20.0 is set to one, then the PHY XS is indicating that the attached DTE XS is permitted to stop transmitting XAUI signals during LPI. If the bit is set to zero then the PHY XS is indicating that the attached DTE XS is not permitted to stop transmitting XAUI signals during LPI. If the DTE XS does not support EEE capability or is not able to stop the transmit direction XAUI, then this bit has no effect.

45.2.4.9 EEE wake error counter (Register 4.22)

This register is used by PHY XS that support EEE to count wake time faults where the PHY XS fails to complete its normal wake sequence after a period of quiescence for XAUI transmit signals. The fault event to be counted may occur during a refresh or a wake-up. This 16-bit counter shall be reset to all zeros when the EEE wake error counter is read by the management function or upon execution of the PHY XS reset. This counter shall be held at all ones in the case of overflow.

45.2.4.10 10G PHY XGXS lane status register (Register 4.24)

The assignment of bits in the 10G PHY XGXS lane status register is shown in Table 45–320. All the bits in the 10G PHY XGXS lane status register are read only; a write to the 10G PHY XGXS lane status register shall have no effect.

45.2.4.10.1 PHY XGXS transmit lane alignment status (4.24.12)

When read as a one, bit 4.24.12 indicates that the PHY XGXS has synchronized and aligned all four transmit lanes. When read as a zero, bit 4.24.12 indicates that the PHY XGXS has not synchronized and aligned all four transmit lanes.

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Table 45–320—10G PHY XGXS lane status register bit definitions

Bit(s)	Name	Description	R/W[a]
4.24.15:13	Reserved	Value always 0	RO
4.24.12	PHY XGXS lane alignment status	1 = PHY XGXS transmit lanes aligned 0 = PHY XGXS transmit lanes not aligned	RO
4.24.11	Pattern testing ability	1 = PHY XGXS is able to generate test patterns 0 = PHY XGXS is not able to generate test patterns	RO
4.24.10	PHY XGXS loopback ability	1 = PHY XGXS has the ability to perform a loopback function 0 = PHY XGXS does not have the ability to perform a loopback function	RO
4.24.9:4	Reserved	Value always 0	RO
4.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
4.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
4.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
4.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read only

45.2.4.10.2 Pattern testing ability (4.24.11)

When read as a one, bit 4.24.11 indicates that the 10G PHY XGXS is able to generate test patterns. When read as a zero, bit 4.24.11 indicates that the 10G PHY XGXS is not able to generate test patterns. If the 10G PHY XGXS is able to generate test patterns, then the functionality is controlled using the transmit test-pattern enable bit in register 4.25.

45.2.4.10.3 PHY XS loopback ability (4.24.10)

When read as a one, bit 4.24.10 indicates that the PHY XGXS is able to perform the loopback function. When read as a zero, bit 4.24.10 indicates that the PHY XGXS is not able to perform the loopback function. If a 10G PHY XGXS is able to perform the loopback function, then it is controlled using the PHY XGXS loopback bit 4.0.14.

45.2.4.10.4 Lane 3 sync (4.24.3)

When read as a one, bit 4.24.3 indicates that the 10G PHY XGXS transmit lane 3 is synchronized. When read as a zero, bit 4.24.3 indicates that the 10G PHY XGXS transmit lane 3 is not synchronized.

45.2.4.10.5 Lane 2 sync (4.24.2)

When read as a one, bit 4.24.2 indicates that the 10G PHY XGXS transmit lane 2 is synchronized. When read as a zero, bit 4.24.2 indicates that the 10G PHY XGXS transmit lane 2 is not synchronized.

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45.2.4.10.6 Lane 1 sync (4.24.1)

When read as a one, bit 4.24.1 indicates that the 10G PHY XGXS transmit lane 1 is synchronized. When read as a zero, bit 4.24.1 indicates that the 10G PHY XGXS transmit lane 1 is not synchronized.

45.2.4.10.7 Lane 0 sync (4.24.0)

When read as a one, bit 4.24.0 indicates that the 10G PHY XGXS transmit lane 0 is synchronized. When read as a zero, bit 4.24.0 indicates that the 10G PHY XGXS transmit lane 0 is not synchronized.

45.2.4.11 10G PHY XGXS test control register (Register 4.25)

The assignment of bits in the 10G PHY XGXS test control register is shown in Table 45–321. The default value for each bit of the 10G PHY XGXS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–321—10G PHY XGXS test control register bit definitions

Bit(s)	Name	Description	R/W[a]
4.25.15:3	Reserved	Value always 0	RO
4.25.2	Receive test-pattern enable	1 = Receive test pattern enabled 0 = Receive test pattern not enabled	R/W
4.25.1:0	Test-pattern select	1 0 1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	R/W

[a]RO = Read only, R/W = Read/Write

45.2.4.11.1 10G PHY XGXS test-pattern enable (4.25.2)

When bit 4.25.2 is set to a one, pattern testing is enabled on the receive path. When bit 4.25.2 is set to a zero, pattern testing is disabled on the receive path. Pattern testing is optional, and the ability of the 10G PHY XGXS to generate test patterns is advertised by the pattern testing ability bit in register 4.24. A 10G PHY XGXS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 4.25.2 is zero.

45.2.4.11.2 10G PHY XGXS test-pattern select (4.25.1:0)

The test pattern to be used when pattern testing is enabled using bit 4.25.2 is selected using bits 4.25.1:0. When bits 4.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 4.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 4.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

45.2.4.12 BASE-R PHY XS status 1 register (Register 4.32)

The assignment of bits in the BASE-R PHY XS status 1 register is shown in Table 45–322. A PHY XS device that does not implement BASE-R shall return a zero for all bits in the BASE-R PHY XS status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

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Table 45–322—BASE-R PHY XS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.32.15:13	Reserved	Value always 0	RO
4.32.12	BASE-R PHY XS receive link status	1 = BASE-R PHY XS receive link up 0 = BASE-R PHY XS receive link down	RO
4.32.11:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.4.12.1 BASE-R PHY XS receive link status (4.32.12)

When read as a one, bit 4.32.12 indicates that the PHY XS is in a fully operational state. When read as a zero, bit 4.32.12 indicates that the PHY XS is not fully operational. This bit is a reflection of the PHY XS equivalent of the PCS_status variable defined in 119.3 for 200/400GBASE-R.

45.2.4.13 BASE-R PHY XS test-pattern control register (Register 4.42)

The assignment of bits in the BASE-R PHY XS test-pattern control register is shown in Table 45–323. This register is only required when the 200/400GBASE-R capability is supported. The test-pattern methodology is described in 119.2.4.9.

Table 45–323—BASE-R PHY XS test-pattern control register bit definitions

Bit(s)	Name	Description	R/W[a]
4.42.15:4	Reserved	Value always 0	RO
4.42.3	Transmit test-pattern enable	1 = Enable transmit test pattern 0 = Disable transmit test pattern	R/W
4.42.2:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

45.2.4.13.1 Transmit test-pattern enable (4.42.3)

When bit 4.42.3 is set to a one, pattern testing is enabled on the transmit path. When bit 4.42.3 is set to a zero, pattern testing is disabled on the transmit path.

The default value for bit 4.42.3 is zero.

45.2.4.14 Multi-lane BASE-R PHY XS alignment status 1 register (Register 4.50)

The assignment of bits in the multi-lane BASE-R PHY XS alignment status 1 register is shown in Table 45–324. A PHY XS device that does not implement multi-lane BASE-R PHY XS shall return a zero for all bits in the multi-lane BASE-R PHY XS alignment status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

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Table 45–324—Multi-lane BASE-R PHY XS alignment status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.50.15:13	Reserved	Value always 0	RO
4.50.12	PHY XS lane alignment status	1 = PHY XS receive lanes locked and aligned 0 = PHY XS receive lanes not locked and aligned	RO
4.50.11:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.4.14.1 PHY XS lane alignment status (4.50.12)

When read as a one, bit 4.50.12 indicates that the PHY XS has locked and aligned all receive lanes. When read as a zero, bit 4.50.12 indicates that the PHY XS has not locked and aligned all receive lanes.

45.2.4.15 Multi-lane BASE-R PHY XS alignment status 3 register (Register 4.52)

The assignment of bits in the multi-lane BASE-R PHY XS alignment status 3 register is shown in Table 45–325. A PHY XS device that does not implement multi-lane BASE-R PHY XS shall return a zero for all bits in the multi-lane BASE-R PHY XS alignment status 3 register. A device that implements multi-lane BASE-R PHY XS shall return a zero for all bits in the multi-lane BASE-R PHY XS alignment status 3 register that are not required for the PHY XS configuration. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–325—Multi-lane BASE-R PHY XS alignment status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.52.15:8	Reserved	Value always 0	RO
4.52.7	Lane 7 aligned	1 = Lane 7 alignment marker is locked 0 = Lane 7 alignment marker is not locked	RO
4.52.6	Lane 6 aligned	1 = Lane 6 alignment marker is locked 0 = Lane 6 alignment marker is not locked	RO
4.52.5	Lane 5 aligned	1 = Lane 5 alignment marker is locked 0 = Lane 5 alignment marker is not locked	RO
4.52.4	Lane 4 aligned	1 = Lane 4 alignment marker is locked 0 = Lane 4 alignment marker is not locked	RO
4.52.3	Lane 3 aligned	1 = Lane 3 alignment marker is locked 0 = Lane 3 alignment marker is not locked	RO
4.52.2	Lane 2 aligned	1 = Lane 2 alignment marker is locked 0 = Lane 2 alignment marker is not locked	RO

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Table 45–325—Multi-lane BASE-R PHY XS alignment status 3 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
4.52.1	Lane 1 aligned	1 = Lane 1 alignment marker is locked 0 = Lane 1 alignment marker is not locked	RO
4.52.0	Lane 0 aligned	1 = Lane 0 alignment marker is locked 0 = Lane 0 alignment marker is not locked	RO

[a]RO = Read only

45.2.4.15.1 Lane 7 aligned (4.52.7)

When read as a one, bit 4.52.7 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 7. When read as a zero, bit 4.52.7 indicates that the PHY XS receiver lane 7 has not achieved alignment marker lock. This bit reflects the state of amps_lock[7] (see 119.2.6.2.2).

45.2.4.15.2 Lane 6 aligned (4.52.6)

When read as a one, bit 4.52.6 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 6. When read as a zero, bit 4.52.6 indicates that the PHY XS receiver lane 6 has not achieved alignment marker lock. This bit reflects the state of amps_lock[6] (see 119.2.6.2.2).

45.2.4.15.3 Lane 5 aligned (4.52.5)

When read as a one, bit 4.52.5 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 5. When read as a zero, bit 4.52.5 indicates that the PHY XS receiver lane 5 has not achieved alignment marker lock. This bit reflects the state of amps_lock[5] (see 119.2.6.2.2).

45.2.4.15.4 Lane 4 aligned (4.52.4)

When read as a one, bit 4.52.4 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 4. When read as a zero, bit 4.52.4 indicates that the PHY XS receiver lane 4 has not achieved alignment marker lock. This bit reflects the state of amps_lock[4] (see 119.2.6.2.2).

45.2.4.15.5 Lane 3 aligned (4.52.3)

When read as a one, bit 4.52.3 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 3. When read as a zero, bit 4.52.3 indicates that the PHY XS receiver lane 3 has not achieved alignment marker lock. This bit reflects the state of amps_lock[3] (see 119.2.6.2.2).

45.2.4.15.6 Lane 2 aligned (4.52.2)

When read as a one, bit 4.52.2 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 2. When read as a zero, bit 4.52.2 indicates that the PHY XS receiver lane 2 has not achieved alignment marker lock. This bit reflects the state of amps_lock[2] (see 119.2.6.2.2).

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45.2.4.15.7 Lane 1 aligned (4.52.1)

When read as a one, bit 4.52.1 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 1. When read as a zero, bit 4.52.1 indicates that the PHY XS receiver lane 1 has not achieved alignment marker lock. This bit reflects the state of amps_lock[1] (see 119.2.6.2.2).

45.2.4.15.8 Lane 0 aligned (4.52.0)

When read as a one, bit 4.52.0 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 0. When read as a zero, bit 4.52.0 indicates that the PHY XS receiver lane 0 has not achieved alignment marker lock. This bit reflects the state of amps_lock[0] (see 119.2.6.2.2).

45.2.4.16 Multi-lane BASE-R PHY XS alignment status 4 register (Register 4.53)

The assignment of bits in the multi-lane BASE-R PHY XS alignment status 4 register is shown in Table 45–326. A PHY XS device that does not implement multi-lane BASE-R PHY XS shall return a zero for all bits in the multi-lane BASE-R PHY XS alignment status 4 register. A device that implements multi-lane BASE-R PHY XS shall return a zero for all bits in the multi-lane BASE-R PHY XS alignment status 4 register that are not required for the PHY XS configuration. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–326—Multi-lane BASE-R PHY XS alignment status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.53.15:8	Reserved	Value always 0	RO
4.53.7	Lane 15 aligned	1 = Lane 15 alignment marker is locked 0 = Lane 15 alignment marker is not locked	RO
4.53.6	Lane 14 aligned	1 = Lane 14 alignment marker is locked 0 = Lane 14 alignment marker is not locked	RO
4.53.5	Lane 13 aligned	1 = Lane 13 alignment marker is locked 0 = Lane 13 alignment marker is not locked	RO
4.53.4	Lane 12 aligned	1 = Lane 12 alignment marker is locked 0 = Lane 12 alignment marker is not locked	RO
4.53.3	Lane 11 aligned	1 = Lane 11 alignment marker is locked 0 = Lane 11 alignment marker is not locked	RO
4.53.2	Lane 10 aligned	1 = Lane 10 alignment marker is locked 0 = Lane 10 alignment marker is not locked	RO
4.53.1	Lane 9 aligned	1 = Lane 9 alignment marker is locked 0 = Lane 9 alignment marker is not locked	RO
4.53.0	Lane 8 aligned	1 = Lane 8 alignment marker is locked 0 = Lane 8 alignment marker is not locked	RO

[a]RO = Read only

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45.2.4.16.1 Lane 15 aligned (4.53.7)

When read as a one, bit 4.53.7 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 15. When read as a zero, bit 4.53.7 indicates that the PHY XS receiver lane 15 has not achieved alignment marker lock. This bit reflects the state of amps_lock[15] (see 119.2.6.2.2).

45.2.4.16.2 Lane 14 aligned (4.53.6)

When read as a one, bit 4.53.6 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 14. When read as a zero, bit 4.53.6 indicates that the PHY XS receiver lane 14 has not achieved alignment marker lock. This bit reflects the state of amps_lock[14] (see 119.2.6.2.2).

45.2.4.16.3 Lane 13 aligned (4.53.5)

When read as a one, bit 4.53.5 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 13. When read as a zero, bit 4.53.5 indicates that the PHY XS receiver lane 13 has not achieved alignment marker lock. This bit reflects the state of amps_lock[13] (see 119.2.6.2.2).

45.2.4.16.4 Lane 12 aligned (4.53.4)

When read as a one, bit 4.53.4 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 12. When read as a zero, bit 4.53.4 indicates that the PHY XS receiver lane 12 has not achieved alignment marker lock. This bit reflects the state of amps_lock[12] (see 119.2.6.2.2).

45.2.4.16.5 Lane 11 aligned (4.53.3)

When read as a one, bit 4.53.3 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 11. When read as a zero, bit 4.53.3 indicates that the PHY XS receiver lane 11 has not achieved alignment marker lock. This bit reflects the state of amps_lock[11] (see 119.2.6.2.2).

45.2.4.16.6 Lane 10 aligned (4.53.2)

When read as a one, bit 4.53.2 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 10. When read as a zero, bit 4.53.2 indicates that the PHY XS receiver lane 10 has not achieved alignment marker lock. This bit reflects the state of amps_lock[10] (see 119.2.6.2.2).

45.2.4.16.7 Lane 9 aligned (4.53.1)

When read as a one, bit 4.53.1 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 9. When read as a zero, bit 4.53.1 indicates that the PHY XS receiver lane 9 has not achieved alignment marker lock. This bit reflects the state of amps_lock[9] (see 119.2.6.2.2).

45.2.4.16.8 Lane 8 aligned (4.53.0)

When read as a one, bit 4.53.0 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 8. When read as a zero, bit 4.53.0 indicates that the PHY XS receiver lane 8 has not achieved alignment marker lock. This bit reflects the state of amps_lock[8] (see 119.2.6.2.2).

45.2.4.17 PHY XS lane mapping, lane 0 register (Register 4.400)

The assignment of bits in the PHY XS lane mapping, lane 0 register is shown in Table 45–327. When the multi-lane PHY XS described in Clause 118 detects and locks the alignment marker for service interface lane 0, the detected PCS lane number is recorded in this register. The contents of the PHY XS lane mapping, lane 0 register is valid when Lane 0 aligned bit (4.52.0) is set to one and is invalid otherwise.

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Table 45–327—PHY XS lane mapping, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.400.15:5	Reserved	Value always 0	RO
4.400.4:0	Lane 0 mapping	PHY XS lane received in service interface lane 0	RO

[a]RO = Read only

45.2.4.18 PHY XS lane mapping, lane 1 through lane 15 registers (Registers 4.401 through 4.415)

The definition of the PHY XS lane mapping, lane 1 through 15 registers is identical to that described for lane 0 in 45.2.4.17. The lane mapping for lane 1 is in register 4.401; lane 2 is in register 4.402; etc.

45.2.4.19 PHY XS FEC symbol error counter lane 0 (Register 4.600, 4.601)

The assignment of bits in the PHY XS FEC symbol error counter lane 0 register is shown in Table 45–328. See 119.3.4 for a definition of this counter. Symbol errors detected in PHY XS FEC lane 0 are counted and shown in register 4.600.15:0 and 4.601.15:0. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 4.600, 4.601 are used to read the value of a 32-bit counter. When registers 4.600 and 4.601 are used to read the 32-bit counter value, the register 4.600 is read first, the value of the register 4.601 is latched when (and only when) register 4.600 is read, and reads of register 4.601 return the latched value rather than the current value of the counter.

Table 45–328—PHY XS FEC symbol error counter lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.600.15:0	PHY XS FEC symbol errors, lane 0 lower	FEC_symbol_error_counter_0[15:0]	RO, NR
4.601.15:0	PHY XS FEC symbol errors, lane 0 upper	FEC_symbol_error_counter_0[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.4.20 PHY XS FEC symbol error counter lane 1 through 15 (Registers 4.602 through 4.631)

The behavior of the PHY XS FEC symbol error counters, lane 1 through 15 is identical to that described for PHY XS FEC lane 0 in 45.2.4.19. Errors detected in each PHY XS FEC lane are counted and shown in the corresponding register. PHY XS FEC lane 1, lower 16 bits are shown in register 4.602; PHY XS FEC lane 1, upper 16 bits are shown in register 4.603; PHY XS FEC lane 2, lower 16 bits are shown in register 4.604; through register 4.631 for PHY XS FEC lane 15, upper 16 bits.

45.2.4.21 PHY XS FEC control register (Register 4.800)

The assignment of bits in the PHY XS FEC control register is shown in Table 45–329.

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Table 45–329—PHY XS FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
4.800.15:3	Reserved	Value always 0	RO
4.800.2	PHY XS FEC degraded SER enable	1 = FEC decoder signals degraded SER 0 = FEC decoder does not signal degraded SER	R/W
4.800.1	PHY XS FEC bypass indication enable	1 = FEC decoder does not indicate errors 0 = FEC decoder indicates errors	R/W
4.800.0	Reserved	Value always 0	RO

[a]R/W = Read/Write, RO = Read only

45.2.4.21.1 PHY XS FEC degraded SER enable (4.800.2)

This bit enables the PHY XS FEC decoder to signal the presence of a degraded SER. When set to a one, this bit enables degraded SER signaling. When set to a zero, degraded SER signaling is disabled. Writes to this bit are ignored and reads return a zero if the PHY XS FEC does not have the ability to signal the presence of a degraded SER (see 119.2.5.3 for equivalent PCS behavior).

45.2.4.21.2 PHY XS FEC bypass indication enable (4.800.1)

This bit enables the PHY XS FEC decoder to bypass error indication to the upper layers through the sync bits. When set to a one, this bit enables bypass of the error indication. When set to a zero, errors are indicated to the upper layers through the sync bits. Writes to this bit are ignored and reads return a zero if the PHY XS FEC does not have the ability to bypass indicating decoding errors (see 119.2.5.3 for equivalent PCS behavior).

45.2.4.22 PHY XS FEC status register (Register 4.801)

The assignment of bits in the PHY XS FEC status register is shown in Table 45–330.

Table 45–330—PHY XS FEC status register bit definitions

Bit(s)	Name	Description	R/W[a]
4.801.15:6	Reserved	Value always 0	RO
4.801.5	Remote degraded SER received	1 = remote degraded SER received 0 = no remote degraded SER received	RO
4.801.4	PHY XS FEC degraded SER	1 = SER is degraded 0 = SER is not degraded	RO
4.801.3	PHY XS FEC degraded SER ability	1 = FEC decoder has the ability to signal the presence of a degraded SER 0 = FEC decoder does not have the ability to signal the presence of a degraded SER	RO

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Table 45–330—PHY XS FEC status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
4.801.2	PHY XS FEC high SER	1 = FEC errors have exceeded threshold 0 = FEC errors have not exceeded threshold	RO/LH
4.801.1	PHY XS FEC bypass indication ability	1 = FEC decoder has the ability to bypass error indication 0 = FEC decoder does not have the ability to bypass error indication	RO
4.801.0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

45.2.4.22.1 Remote degraded SER received (4.801.5)

When read as a one, bit 4.801.5 indicates that the remote degraded SER signal has been received. This bit reflects the state of rx_rm_degraded for the PHY XS (see 119.2.6.2.2 for equivalent PCS behavior).

45.2.4.22.2 PHY XS FEC degraded SER (4.801.4)

When PHY XS FEC degraded SER enable (bit 4.800.2) is set to one, bit 4.801.4 is set to one if the number of FEC symbol errors in a window of PHY XS FEC degraded SER interval (registers 4.810 and 4.811) codewords exceeds the PHY XS FEC degraded SER activate threshold (registers 4.806 and 4.807) and is cleared if the number of FEC symbol errors in the same window is below the PHY XS FEC degraded SER deactivate threshold (registers 4.808 and 4.809). If the number of FEC symbol errors in the window is between the two thresholds, then bit 4.801.4 remains in its previous state. The bit is set to zero if PHY XS FEC degraded SER enable (bit 4.800.2) is set to zero (see 119.2.5.3 for equivalent PCS behavior). The value of bit 4.801.4 is undefined if the value of the PHY XS FEC degraded SER activate threshold is less than the value of the PHY XS FEC degraded SER deactivate threshold.

45.2.4.22.3 PHY XS FEC degraded SER ability (4.801.3)

The PHY XS FEC decoder may have the option to signal the presence of a degraded SER (see 119.2.5.3 for equivalent PCS behavior). This bit is set to one to indicate that the decoder has the ability to signal the presence of a degraded SER. The bit is set to zero if this ability is not supported.

45.2.4.22.4 PHY XS FEC high SER (4.801.2)

When PHY XS FEC bypass indication enable (bit 4.800.1) is set to one, this bit is set to one if the number of FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 119.2.5.3 for equivalent PCS behavior) and is set to zero otherwise. The bit is set to zero if PHY XS FEC bypass indication enable (bit 4.800.1) is set to zero. This bit shall be implemented with latching high behavior.

45.2.4.22.5 PHY XS FEC bypass indication ability (4.801.1)

The PHY XS FEC decoder may have the option to perform error detection without error indication (see 119.2.5.3 for equivalent PCS behavior) to reduce the delay contributed by the FEC decoder. This bit is set to one to indicate that the decoder has this ability to bypass error indication. The bit is set to zero if this ability is not supported.

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45.2.4.23 PHY XS FEC corrected codewords counter (Register 4.802, 4.803)

The assignment of bits in the PHY XS FEC corrected codewords counter register is shown in Table 45–331. See 119.3.2 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 4.802, 4.803 are used to read the value of a 32-bit counter. When registers 4.802 and 4.803 are used to read the 32-bit counter value, the register 4.802 is read first, the value of the register 4.803 is latched when (and only when) register 4.802 is read, and reads of register 4.803 return the latched value rather than the current value of the counter.

Table 45–331—PHY XS FEC corrected codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
4.802.15:0	FEC corrected codewords lower	FEC_corrected_cw_counter[15:0]	RO, NR
4.803.15:0	FEC corrected codewords upper	FEC_corrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.4.24 PHY XS FEC uncorrected codewords counter (Register 4.804, 4.805)

The assignment of bits in the PHY XS FEC uncorrected codewords counter register is shown in Table 45–332. See 119.3.3 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 4.804, 4.805 are used to read the value of a 32-bit counter. When registers 4.804 and 4.805 are used to read the 32-bit counter value, the register 4.804 is read first, the value of the register 4.805 is latched when (and only when) register 4.804 is read, and reads of register 4.805 return the latched value rather than the current value of the counter.

Table 45–332—PHY XS FEC uncorrected codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
4.804.15:0	FEC uncorrected codewords lower	FEC_uncorrected_cw_counter[15:0]	RO, NR
4.805.15:0	FEC uncorrected codewords upper	FEC_uncorrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

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45.2.4.25 PHY XS FEC degraded SER activate threshold register (Register 4.806, 4.807)

The assignment of bits in the PHY XS FEC degraded SER activate threshold register is shown in Table 45–333. The value controls the threshold used to set the PHY XS FEC degraded SER bit (4.801.4) in an equivalent manner to that defined for the FEC_degraded_SER bit in 119.2.5.3.

Table 45–333—PHY XS FEC degraded SER activate threshold register bit definitions

Bit(s)	Name	Description	R/W[a]
4.806.15:0	PHY XS FEC degraded SER activate threshold lower	FEC_degraded_SER_activate_threshold[15:0]	R/W
4.807.15:0	PHY XS FEC degraded SER activate threshold upper	FEC_degraded_SER_activate_threshold[31:16]	R/W

[a]R/W = Read/Write

45.2.4.26 PHY XS FEC degraded SER deactivate threshold register (Register 4.808, 4.809)

The assignment of bits in the PHY XS FEC degraded SER deactivate threshold register is shown in Table 45–334. The value controls the threshold used to clear the PHY XS FEC degraded SER bit (4.801.4) in an equivalent manner to that defined for the FEC_degraded_SER bit in 119.2.5.3.

Table 45–334—PHY XS FEC degraded SER deactivate threshold register bit definitions

Bit(s)	Name	Description	R/W[a]
4.808.15:0	PHY XS FEC degraded SER deactivate threshold lower	FEC_degraded_SER_deactivate_threshold[15:0]	R/W
4.809.15:0	PHY XS FEC degraded SER deactivate threshold upper	FEC_degraded_SER_deactivate_threshold[31:16]	R/W

[a]R/W = Read/Write

45.2.4.27 PHY XS FEC degraded SER interval register (Register 4.810, 4.811)

The assignment of bits in the PHY XS FEC degraded SER interval register is shown in Table 45–335. The value controls the interval used to set and clear the PHY XS FEC degraded SER bit (4.801.4) in an equivalent manner to that defined for the FEC_degraded_SER bit in 119.2.5.3.

Table 45–335—PHY XS FEC degraded SER interval register bit definitions

Bit(s)	Name	Description	R/W[a]
4.810.15:0	PHY XS FEC degraded SER interval lower	FEC_degraded_SER_interval[15:0]	R/W
4.811.15:0	PHY XS FEC degraded SER interval upper	FEC_degraded_SER_interval[31:16]	R/W

[a]R/W = Read/Write

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45.2.4.28 TimeSync PHY XS capability (Register 4.1800)

The TimeSync PHY XS capability register (see Table 45–336) indicates the capability of the PHY XS to report the transmit and receive data delay, stored in registers 4.1801 through 4.1804 and 4.1805 through 4.1808, respectively.

Table 45–336—TimeSync PHY XS capability

Bit(s)	Name	Description	R/W[a]
4.1800.15:2	Reserved	Value always 0	RO
4.1800.1	TimeSync transmit path data delay	1 = PHY XS provides information on transmit path data delay in registers 4.1801 through 4.1804 0 = PHY XS does not provide information on transmit path data delay	RO
4.1800.0	TimeSync receive path data delay	1 = PHY XS provides information on receive path data delay in registers 4.1805 through 4.1808 0 = PHY XS does not provide information on receive path data delay	RO

[a]RO = Read only

45.2.4.29 TimeSync PHY XS transmit path data delay (Registers 4.1801, 4.1802, 4.1803, 4.1804)

The TimeSync PHY XS transmit path data delay register contains the maximum (registers 4.1801, 4.1802, see Table 45–337) and minimum (registers 4.1803, 4.1804, see Table 45–337) values of the transmit path data delay. The transmit path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in register 1.1 (see 45.2.1.2.4).

Table 45–337—TimeSync PHY XS transmit path data delay register

Bit(s)	Name	Description	R/W[a]
4.1801.15:0	Maximum PHY XS transmit path data delay, lower	PHY_XS_delay_TX_max [15:0]	RO, MW
4.1802.15:0	Maximum PHY XS transmit path data delay, upper	PHY_XS_delay_TX_max [31:16]	RO, MW
4.1803.15:0	Minimum PHY XS transmit path data delay, lower	PHY_XS_delay_TX_min [15:0]	RO, MW
4.1804.15:0	Minimum PHY XS transmit path data delay, upper	PHY_XS_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.4.30 TimeSync PHY XS receive path data delay (Registers 4.1805, 4.1806, 4.1807, 4.1808)

The TimeSync PHY XS receive path data delay register contains the maximum (registers 4.1805, 4.1806, see Table 45–338) and minimum (registers 4.1807, 4.1808, see Table 45–338) values of the receive path data delay. The receive path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in register 4.1 (see 45.2.4.2.7).

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Table 45–338—TimeSync PHY XS receive path data delay register

Bit(s)	Name	Description	R/W[a]
4.1805.15:0	Maximum PHY XS receive path data delay, lower	PHY_XS_delay_RX_max [15:0]	RO, MW
4.1806.15:0	Maximum PHY XS receive path data delay, upper	PHY_XS_delay_RX_max [31:16]	RO, MW
4.1807.15:0	Minimum PHY XS receive path data delay, lower	PHY_XS_delay_RX_min [15:0]	RO, MW
4.1808.15:0	Minimum PHY XS receive path data delay, upper	PHY_XS_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.5 DTE XS registers

The assignment of registers in the DTE XS is shown in Table 45–339.

Table 45–339—DTE XS registers

Register address	Register name	Subclause
5.0	DTE XS control 1	45.2.5.1
5.1	DTE XS status 1	45.2.5.2
5.2, 5.3	DTE XS device identifier	45.2.5.3
5.4	DTE XS speed ability	45.2.5.4
5.5, 5.6	DTE XS devices in package	45.2.5.5
5.7	Reserved	
5.8	DTE XS status 2	45.2.5.6
5.9 through 5.13	Reserved	
5.14, 5.15	DTE XS package identifier	45.2.5.7
5.16 through 5.19	Reserved	
5.20	EEE capability	45.2.5.8
5.21	Reserved	
5.22	EEE wake error counter	45.2.5.9
5.23	Reserved	
5.24	10G DTE XGXS lane status	45.2.5.10
5.25	10G DTE XGXS test control	45.2.5.11
5.26 through 5.31	Reserved	

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Table 45–339—DTE XS registers *(continued)*

Register address	Register name	Subclause
5.32	BASE-R DTE XS status 1	45.2.5.12
5.33 through 5.41	Reserved	
5.42	BASE-R DTE XS test pattern control	45.2.5.13
5.43 through 5.49	Reserved	
5.50	Multi-lane BASE-R DTE XS alignment status 1	45.2.5.14
5.51	Reserved	
5.52	Multi-lane BASE-R DTE XS alignment status 3	45.2.5.15
5.53	Multi-lane BASE-R DTE XS alignment status 4	45.2.5.16
5.54	Reserved	
5.400 through 5.415	DTE XS lane mapping, lane 0 through 15	45.2.5.17, 45.2.5.18
5.415 through 5.599	Reserved	
5.600 through 5.631	DTE XS FEC symbol error counter, lane 0 to 15	45.2.5.19, 45.2.5.20
5.632 through 5.799	Reserved	
5.800	DTE XS FEC control	45.2.5.21
5.801	DTE XS FEC status	45.2.5.22
5.802, 5.803	DTE XS FEC corrected codewords counter	45.2.5.23
5.804, 5.805	DTE XS FEC uncorrected codewords counter	45.2.5.24
5.806, 5.807	DTE XS FEC degraded SER activate threshold	45.2.5.25
5.808, 5.809	DTE XS FEC degraded SER deactivate threshold	45.2.5.26
5.810, 5.811	DTE XS FEC degraded SER interval	45.2.5.27
5.812 through 5.1799	Reserved	
5.1800	TimeSync DTE XS capability	45.2.5.28
5.1801 through 5.1804	TimeSync DTE XS transmit path data delay	45.2.5.29
5.1805 through 5.1808	TimeSync DTE XS receive path data delay	45.2.5.30
5.1809 through 5.32767	Reserved	
5.32 768 through 5.65 535	Vendor specific	

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45.2.5.1 DTE XS control 1 register (Register 5.0)

The assignment of bits in the DTE XS control 1 register is shown in Table 45–340. The default value for each bit of the DTE XS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–340—DTE XS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.0.15	Reset	1 = DTE XS reset 0 = Normal operation	R/W SC
5.0.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
5.0.13	Speed selection	1 = Operation at 10 Gbp/s and above 0 = Unspecified	R/W
5.0.12	Reserved	Value always 0	RO
5.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
5.0.10	Clock stop enable	1 = The DTE XS may stop the clock during LPI 0 = Clock not stoppable	R/W
5.0.9	XAUI stop enable	1 = The DTE XS may stop XAUI signals during LPI 0 = XAUI not stoppable	R/W
5.0.8:7	Reserved	Value always 0	RO
5.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
5.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 1 = Reserved 1 0 1 0 = 400 Gb/s 1 0 0 1 = 200 Gb/s 1 0 0 0 = Reserved 0 1 x x = Reserved 0 0 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
5.0.1:0	Reserved	Value always 0	RO

[a]R/W = Read/Write, SC = Self-clearing, RO = Read only

45.2.5.1.1 Reset (5.0.15)

Resetting a DTE XS is accomplished by setting bit 5.0.15 to a one. This action shall set all DTE XS registers to their default states. As a consequence, this action may change the internal state of the DTE XS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a DTE XS shall return a value of one in bit 5.0.15 when a reset is

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in progress and a value of zero otherwise. A DTE XS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 5.0.15. During a reset, a DTE XS shall respond to reads to register bits 5.0.15 and 5.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.5.1.2 Loopback (5.0.14)

The DTE XS shall be placed in a loopback mode of operation when bit 5.0.14 is set to a one. When bit 5.0.14 is set to a one, the DTE XS shall accept data on the transmit path and return it on the receive path. For 10 Gb/s operation, the specific behavior of a DTE XS during loopback is specified in 48.3.3.

The default value of bit 5.0.14 is zero.

NOTE—The signal path through the DTE XS that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the DTE XS circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.5.1.3 Low power (5.0.11)

A DTE XS may be placed into a low-power mode by setting bit 5.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the DTE XS. The behavior of the DTE XS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 5.0.11 is zero.

45.2.5.1.4 Clock stop enable (5.0.10)

If bit 5.0.10 is set to one, then the DTE XS may stop the receive xMII clock while it is signaling LPI, otherwise it shall keep the clock active. If the DTE XS does not support EEE capability or is not able to stop the receive clock, then this bit has no effect (see 46.3.2.4).

45.2.5.1.5 XAUI stop enable (5.0.9)

If bit 5.0.9 is set to one, then the DTE XS may stop signaling on the XAUI in the transmit direction during LPI, otherwise the DTE XS shall keep the XAUI signals active. If the DTE XS does not support EEE capability or is not able to stop the transmit path XAUI signals, then this bit has no effect.

45.2.5.1.6 Speed selection (5.0.13, 5.0.6, 5.0.5:2)

Speed selection bits 5.0.13 and 5.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the DTE XS may be selected using bits 5 through 2. The speed abilities of the DTE XS are advertised in the DTE XS speed ability register. A DTE XS may ignore writes to the DTE XS speed selection bits that select speeds it has not advertised in the DTE XS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The DTE XS speed selection defaults to a supported ability.

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45.2.5.2 DTE XS status 1 register (Register 5.1)

The assignment of bits in the DTE XS status 1 register is shown in Table 45–341. All the bits in the DTE XS status 1 register are read only; a write to the DTE XS status 1 register shall have no effect.

Table 45–341—DTE XS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.1.15:12	Reserved	Value always 0	RO
5.1.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
5.1.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
5.1.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
5.1.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
5.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
5.1.6	Clock stop capable	1 = The MAC may stop the clock during LPI 0 = Clock not stoppable	RO
5.1.5:3	Reserved	Value always 0	RO
5.1.2	DTE XS receive link status	1 = The DTE XS receive link is up 0 = The DTE XS receive link is down	RO/LL
5.1.1	Low-power ability	1 = DTE XS supports low-power mode 0 = DTE XS does not support low-power mode	RO
5.1.0	Reserved	Value always 0	RO

[a]RO = Read only, LL = Latching low, LH = Latching high

45.2.5.2.1 Transmit LPI received (5.1.11)

When read as a one, bit 5.1.11 indicates that the transmit DTE XS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 5.1.11 indicates that the DTE XS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.5.2.2 Receive LPI received (5.1.10)

When read as a one, bit 5.1.10 indicates that the receive DTE XS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 5.1.10 indicates that the DTE XS has not received LPI signaling. This bit shall be implemented with latching high behavior.

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45.2.5.2.3 Transmit LPI indication (5.1.9)

When read as a one, bit 5.1.9 indicates that the transmit DTE XS is currently receiving LPI signals. When read as a zero, bit 5.1.9 indicates that the DTE XS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.5.2.4 Receive LPI indication (5.1.8)

When read as a one, bit 5.1.8 indicates that the receive DTE XS is currently receiving LPI signals. When read as a zero, bit 5.1.8 indicates that the DTE XS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.5.2.5 Fault (5.1.7)

When read as a one, bit 5.1.7 indicates that the DTE XS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 5.1.7 indicates that the DTE XS has not detected a fault condition. Bit 5.1.7 is set to a one when either of the fault bits (5.8.11, 5.8.10) located in register 5.8 are set to a one.

45.2.5.2.6 Clock stop capable (5.1.6)

If bit 5.1.6 is set to one, then the DTE XS is indicating that the attached RS is permitted to stop the transmit xMII clock while it is signaling LPI. If the bit is set to zero, then the DTE XS is indicating that the attached RS is not permitted to stop the transmit xMII clock while it is signaling LPI. If the RS does not support EEE capability or is not able to stop the transmit direction xMII clock, then this bit has no effect (see 46.3.2.4).

45.2.5.2.7 DTE XS receive link status (5.1.2)

When read as a one, bit 5.1.2 indicates that the DTE XS receive link is aligned. When read as a zero, bit 5.1.2 indicates that the DTE XS receive link is not aligned. The receive link status bit shall be implemented with latching low behavior.

For 10 Gb/s operation, this bit is a latching low version of bit 5.24.12.

45.2.5.2.8 Low-power ability (5.1.1)

When read as a one, bit 5.1.1 indicates that the DTE XS supports the low-power feature. When read as a zero, bit 5.1.1 indicates that the DTE XS does not support the low-power feature. If a DTE XS supports the low-power feature then it is controlled using the low-power bit in the DTE XS control register.

45.2.5.3 DTE XS device identifier (Registers 5.2 and 5.3)

Registers 5.2 and 5.3 provide a 32-bit value, which may constitute a unique identifier for a DTE XS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A DTE XS may return a value of zero in each of the 32 bits of the DTE XS device identifier.

The format of the DTE XS device identifier is specified in 22.2.4.3.1.

45.2.5.4 DTE XS speed ability (Register 5.4)

The assignment of bits in the DTE XS speed ability register is shown in Table 45–342.

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Table 45–342— DTE XS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
5.4.15:10	Reserved	Value always 0	RO
5.4.9	400G capable	1 = DTE XS is capable of operating at 400 Gb/s 0 = DTE XS is not capable of operating at 400 Gb/s	RO
5.4.8	200G capable	1 = DTE XS is capable of operating at 200 Gb/s 0 = DTE XS is not capable of operating at 200 Gb/s	RO
5.4.7:1	Reserved	Value always 0	RO
5.4.0	10G capable	1 = DTE XS is capable of operating at 10 Gb/s 0 = DTE XS is not capable of operating at 10 Gb/s	RO

[a]RO = Read only

45.2.5.4.1 400G capable (5.4.9)

When read as a one, bit 5.4.9 indicates that the DTE XS is able to operate at a data rate of 400 Gb/s. When read as a zero, bit 5.4.9 indicates that the DTE XS is not able to operate at a data rate of 400 Gb/s.

45.2.5.4.2 200G capable (5.4.8)

When read as a one, bit 5.4.8 indicates that the DTE XS is able to operate at a data rate of 200 Gb/s. When read as a zero, bit 5.4.8 indicates that the DTE XS is not able to operate at a data rate of 200 Gb/s.

45.2.5.4.3 10G capable (5.4.0)

When read as a one, bit 5.4.0 indicates that the DTE XS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 5.4.0 indicates that the DTE XS is not able to operate at a data rate of 10 Gb/s.

45.2.5.5 DTE XS devices in package (Registers 5.5 and 5.6)

The DTE XS devices in package registers are defined in Table 45–2.

45.2.5.6 DTE XS status 2 register (Register 5.8)

The assignment of bits in the DTE XS status 2 register is shown in Table 45–343. All the bits in the DTE XS status 2 register are read only; a write to the DTE XS status 2 register shall have no effect.

Table 45–343—DTE XS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
5.8.13:12	Reserved	Value always 0	RO

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Table 45–343—DTE XS status 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
5.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
5.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
5.8.9:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

45.2.5.6.1 Device present (5.8.15:14)

When read as <10>, bits 5.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 5.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.5.6.2 Transmit fault (5.8.11)

When read as a one, bit 5.8.11 indicates that the DTE XS has detected a fault condition on the transmit path. When read as a zero, bit 5.8.11 indicates that the DTE XS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 5.8.11 is zero.

45.2.5.6.3 Receive fault (5.8.10)

When read as a one, bit 5.8.10 indicates that the DTE XS has detected a fault condition on the receive path. When read as a zero, bit 5.8.10 indicates that the DTE XS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 5.8.10 is zero.

45.2.5.7 DTE XS package identifier (Registers 5.14 and 5.15)

Registers 5.14 and 5.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the DTE XS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A DTE XS may return a value of zero in each of the 32 bits of the DTE XS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the DTE XS package identifier is specified in 22.2.4.3.1.

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45.2.5.8 EEE capability (Register 5.20)

This register is used to indicate the capability of the DTE XS to support EEE functions. The assignment of bits in the EEE capability register is shown in Table 45–344.

Table 45–344—EEE capability register bit definitions

Bit(s)	Name	Description	R/W[a]
5.20.15:5	Reserved	Value always 0	RO
5.20.4	DTE XS EEE	1 = EEE is supported for DTE XS 0 = EEE is not supported for DTE XS	RO
5.20.3:1	Reserved	Value always 0	RO
5.20.0	XAUI stop capable	1 = The PHY XS may stop XAUI signals during LPI 0 = XAUI signals not stoppable	RO

[a] RO = Read only

45.2.5.8.1 PHY XS EEE supported (5.20.4)

If the device supports EEE operation for DTE XS as defined in 48.2, this bit shall be set to one.

45.2.5.8.2 XAUI stop capable (5.20.0)

If bit 5.20.0 is set to one, then the DTE XS is indicating that the attached PHY XS is permitted to stop signaling the XAUI in the receive direction during LPI. If the bit is set to zero, then the DTE XS is indicating that the attached PHY XS is not permitted to stop signaling the XAUI in the receive direction during LPI. If the PHY XS does not support EEE capability or is not able to stop the receive direction XAUI, then this bit has no effect.

45.2.5.9 EEE wake error counter (Register 5.22)

This register is used by DTE XS that support EEE to count wake time faults where the DTE XS fails to complete its normal wake sequence after a period of quiescence for XAUI receive signals. The fault event to be counted may occur during a refresh or a wake-up. This 16-bit counter shall be reset to all zeros when the EEE wake error counter is read by the management function or upon execution of the DTE XS reset. This counter shall be held at all ones in the case of overflow.

45.2.5.10 10G DTE XGXS lane status register (Register 5.24)

The assignment of bits in the 10G DTE XGXS lane status register is shown in Table 45–345. All the bits in the 10G DTE XGXS lane status register are read only; a write to the 10G DTE XGXS lane status register shall have no effect.

45.2.5.10.1 DTE XGXS receive lane alignment status (5.24.12)

When read as a one, bit 5.24.12 indicates that the DTE XGXS has synchronized and aligned all four receive lanes. When read as a zero, bit 5.24.12 indicates that the DTE XGXS has not synchronized and aligned all four receive lanes.

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Table 45–345—10G DTE XGXS lane status register bit definitions

Bit(s)	Name	Description	R/W[a]
5.24.15:13	Reserved	Value always 0	RO
5.24.12	DTE XGXS lane alignment status	1 = DTE XGXS receive lanes aligned 0 = DTE XGXS receive lanes not aligned	RO
5.24.11	Pattern testing ability	1 = DTE XGXS is able to generate test patterns 0 = DTE XGXS is not able to generate test patterns	RO
5.24.10	Ignored	Value 0 or 1, writes ignored	RO
5.24.9:4	Reserved	Value always 0	RO
5.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
5.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
5.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
5.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read only

45.2.5.10.2 Pattern testing ability (5.24.11)

When read as a one, bit 5.24.11 indicates that the 10G DTE XGXS is able to generate test patterns. When read as a zero, bit 5.24.11 indicates that the 10G DTE XGXS is not able to generate test patterns. If the 10G DTE XGXS is able to generate test patterns then the functionality is controlled using the transmit test-pattern enable bit in register 5.25.

45.2.5.10.3 Ignored (5.24.10)

So that a single device can implement either register 4.24 or register 5.24, bit 5.24.10 can return either a one or a zero and should be ignored.

45.2.5.10.4 Lane 3 sync (5.24.3)

When read as a one, bit 5.24.3 indicates that the XGXS receive lane 3 is synchronized. When read as a zero, bit 5.24.3 indicates that the XGXS receive lane 3 is not synchronized.

45.2.5.10.5 Lane 2 sync (5.24.2)

When read as a one, bit 5.24.2 indicates that the XGXS receive lane 2 is synchronized. When read as a zero, bit 5.24.2 indicates that the XGXS receive lane 2 is not synchronized.

45.2.5.10.6 Lane 1 sync (5.24.1)

When read as a one, bit 5.24.1 indicates that the XGXS receive lane 1 is synchronized. When read as a zero, bit 5.24.1 indicates that the XGXS receive lane 1 is not synchronized.

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45.2.5.10.7 Lane 0 sync (5.24.0)

When read as a one, bit 5.24.0 indicates that the XGXS receive lane 0 is synchronized. When read as a zero, bit 5.24.0 indicates that the XGXS receive lane 0 is not synchronized.

45.2.5.11 10G DTE XGXS test control register (Register 5.25)

The assignment of bits in the 10G DTE XGXS test control register is shown in Table 45–346. The default value for each bit of the 10G DTE XGXS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–346—10G DTE XGXS test control register bit definitions

Bit(s)	Name	Description	R/W[a]
5.25.15:3	Reserved	Value always 0	RO
5.25.2	Transmit test-pattern enable	1 = Transmit test pattern enabled 0 = Transmit test pattern not enabled	R/W
5.25.1:0	Test-pattern select	1 0 1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	R/W

[a]RO = Read only, R/W = Read/Write

45.2.5.11.1 10G DTE XGXS test-pattern enable (5.25.2)

When bit 5.25.2 is set to a one, pattern testing is enabled on the transmit path. When bit 5.25.2 is set to a zero, pattern testing is disabled on the transmit path. Pattern testing is optional, and the ability of the 10G DTE XGXS to generate test patterns is advertised by the pattern testing ability bit in register 5.24. A 10G DTE XGXS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 5.25.2 is zero.

45.2.5.11.2 10G DTE XGXS test-pattern select (5.25.1:0)

The test pattern to be used when pattern testing is enabled using bit 5.25.2 is selected using bits 5.25.1:0. When bits 5.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 5.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 5.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

45.2.5.12 BASE-R DTE XS status 1 register (Register 5.32)

The assignment of bits in the BASE-R DTE XS status 1 register is shown in Table 45–347. A DTE XS device that does not implement BASE-R shall return a zero for all bits in the BASE-R DTE XS status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

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Table 45–347—BASE-R DTE XS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.32.15:13	Reserved	Value always 0	RO
5.32.12	BASE-R DTE XS receive link status	1 = BASE-R DTE XS receive link up 0 = BASE-R DTE XS receive link down	RO
5.32.11:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.5.12.1 BASE-R DTE XS receive link status (5.32.12)

When read as a one, bit 5.32.12 indicates that the DTE XS is in a fully operational state. When read as a zero, bit 5.32.12 indicates that the DTE XS is not fully operational. This bit is a reflection of the DTE XS equivalent of the PCS_status variable defined in 119.3 for 200/400GBASE-R.

45.2.5.13 BASE-R DTE XS test-pattern control register (Register 5.42)

The assignment of bits in the BASE-R DTE XS test-pattern control register is shown in Table 45–348. This register is only required when the 200/400GBASE-R capability is supported. The test-pattern methodology is described in 119.2.4.9.

Table 45–348—BASE-R DTE XS test-pattern control register bit definitions

Bit(s)	Name	Description	R/W[a]
5.42.15:4	Reserved	Value always 0	RO
5.42.3	Transmit test-pattern enable	1 = Enable transmit test pattern 0 = Disable transmit test pattern	R/W
5.42.2:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

45.2.5.13.1 Transmit test-pattern enable (5.42.3)

When bit 5.42.3 is set to a one, pattern testing is enabled on the transmit path. When bit 5.42.3 is set to a zero, pattern testing is disabled on the transmit path.

The default value for bit 5.42.3 is zero.

45.2.5.14 Multi-lane BASE-R DTE XS alignment status 1 register (Register 5.50)

The assignment of bits in the multi-lane BASE-R DTE XS alignment status 1 register is shown in Table 45–349. A DTE XS device that does not implement multi-lane BASE-R DTE XS shall return a zero for all bits in the multi-lane BASE-R DTE XS alignment status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

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Table 45–349—Multi-lane BASE-R DTE XS alignment status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.50.15:13	Reserved	Value always 0	RO
5.50.12	DTE XS lane alignment status	1 = DTE XS receive lanes locked and aligned 0 = DTE XS receive lanes not locked and aligned	RO
5.50.11:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.5.14.1 DTE XS lane alignment status (5.50.12)

When read as a one, bit 5.50.12 indicates that the DTE XS has locked and aligned all receive lanes. When read as a zero, bit 5.50.12 indicates that the DTE XS has not locked and aligned all receive lanes.

45.2.5.15 Multi-lane BASE-R DTE XS alignment status 3 register (Register 5.52)

The assignment of bits in the multi-lane BASE-R DTE XS alignment status 3 register is shown in Table 45–350. A DTE XS device that does not implement multi-lane BASE-R DTE XS shall return a zero for all bits in the multi-lane BASE-R DTE XS alignment status 3 register. A device that implements multi-lane BASE-R DTE XS shall return a zero for all bits in the multi-lane BASE-R DTE XS alignment status 3 register that are not required for the DTE XS configuration. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–350—Multi-lane BASE-R DTE XS alignment status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.52.15:8	Reserved	Value always 0	RO
5.52.7	Lane 7 aligned	1 = Lane 7 alignment marker is locked 0 = Lane 7 alignment marker is not locked	RO
5.52.6	Lane 6 aligned	1 = Lane 6 alignment marker is locked 0 = Lane 6 alignment marker is not locked	RO
5.52.5	Lane 5 aligned	1 = Lane 5 alignment marker is locked 0 = Lane 5 alignment marker is not locked	RO
5.52.4	Lane 4 aligned	1 = Lane 4 alignment marker is locked 0 = Lane 4 alignment marker is not locked	RO
5.52.3	Lane 3 aligned	1 = Lane 3 alignment marker is locked 0 = Lane 3 alignment marker is not locked	RO
5.52.2	Lane 2 aligned	1 = Lane 2 alignment marker is locked 0 = Lane 2 alignment marker is not locked	RO

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Table 45–350—Multi-lane BASE-R DTE XS alignment status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.52.1	Lane 1 aligned	1 = Lane 1 alignment marker is locked 0 = Lane 1 alignment marker is not locked	RO
5.52.0	Lane 0 aligned	1 = Lane 0 alignment marker is locked 0 = Lane 0 alignment marker is not locked	RO

[a]RO = Read only

45.2.5.15.1 Lane 7 aligned (5.52.7)

When read as a one, bit 5.52.7 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 7. When read as a zero, bit 5.52.7 indicates that the DTE XS receiver lane 7 has not achieved alignment marker lock. This bit reflects the state of amps_lock[7] (see 119.2.6.2.2).

45.2.5.15.2 Lane 6 aligned (5.52.6)

When read as a one, bit 5.52.6 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 6. When read as a zero, bit 5.52.6 indicates that the DTE XS receiver lane 6 has not achieved alignment marker lock. This bit reflects the state of amps_lock[6] (see 119.2.6.2.2).

45.2.5.15.3 Lane 5 aligned (5.52.5)

When read as a one, bit 5.52.5 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 5. When read as a zero, bit 5.52.5 indicates that the DTE XS receiver lane 5 has not achieved alignment marker lock. This bit reflects the state of amps_lock[5] (see 119.2.6.2.2).

45.2.5.15.4 Lane 4 aligned (5.52.4)

When read as a one, bit 5.52.4 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 4. When read as a zero, bit 5.52.4 indicates that the DTE XS receiver lane 4 has not achieved alignment marker lock. This bit reflects the state of amps_lock[4] (see 119.2.6.2.2).

45.2.5.15.5 Lane 3 aligned (5.52.3)

When read as a one, bit 5.52.3 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 3. When read as a zero, bit 5.52.3 indicates that the DTE XS receiver lane 3 has not achieved alignment marker lock. This bit reflects the state of amps_lock[3] (see 119.2.6.2.2).

45.2.5.15.6 Lane 2 aligned (5.52.2)

When read as a one, bit 5.52.2 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 2. When read as a zero, bit 5.52.2 indicates that the DTE XS receiver lane 2 has not achieved alignment marker lock. This bit reflects the state of amps_lock[2] (see 119.2.6.2.2).

45.2.5.15.7 Lane 1 aligned (5.52.1)

When read as a one, bit 5.52.1 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 1. When read as a zero, bit 5.52.1 indicates that the DTE XS receiver lane 1 has not achieved alignment marker lock. This bit reflects the state of amps_lock[1] (see 119.2.6.2.2).

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45.2.5.15.8 Lane 0 aligned (5.52.0)

When read as a one, bit 5.52.0 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 0. When read as a zero, bit 5.52.0 indicates that the DTE XS receiver lane 0 has not achieved alignment marker lock. This bit reflects the state of amps_lock[0] (see 119.2.6.2.2).

45.2.5.16 Multi-lane BASE-R DTE XS alignment status 4 register (Register 5.53)

The assignment of bits in the multi-lane BASE-R DTE XS alignment status 4 register is shown in Table 45–351. A DTE XS device that does not implement multi-lane BASE-R DTE XS shall return a zero for all bits in the multi-lane BASE-R DTE XS alignment status 4 register. A device that implements multi-lane BASE-R DTE XS shall return a zero for all bits in the multi-lane BASE-R DTE XS alignment status 4 register that are not required for the DTE XS configuration. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–351—Multi-lane BASE-R DTE XS alignment status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.53.15:8	Reserved	Value always 0	RO
5.53.7	Lane 15 aligned	1 = Lane 15 alignment marker is locked 0 = Lane 15 alignment marker is not locked	RO
5.53.6	Lane 14 aligned	1 = Lane 14 alignment marker is locked 0 = Lane 14 alignment marker is not locked	RO
5.53.5	Lane 13 aligned	1 = Lane 13 alignment marker is locked 0 = Lane 13 alignment marker is not locked	RO
5.53.4	Lane 12 aligned	1 = Lane 12 alignment marker is locked 0 = Lane 12 alignment marker is not locked	RO
5.53.3	Lane 11 aligned	1 = Lane 11 alignment marker is locked 0 = Lane 11 alignment marker is not locked	RO
5.53.2	Lane 10 aligned	1 = Lane 10 alignment marker is locked 0 = Lane 10 alignment marker is not locked	RO
5.53.1	Lane 9 aligned	1 = Lane 9 alignment marker is locked 0 = Lane 9 alignment marker is not locked	RO
5.53.0	Lane 8 aligned	1 = Lane 8 alignment marker is locked 0 = Lane 8 alignment marker is not locked	RO

[a]RO = Read only

45.2.5.16.1 Lane 15 aligned (5.53.7)

When read as a one, bit 5.53.7 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 15. When read as a zero, bit 5.53.7 indicates that the DTE XS receiver lane 15 has not achieved alignment marker lock. This bit reflects the state of amps_lock[15] (see 119.2.6.2.2).

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45.2.5.16.2 Lane 14 aligned (5.53.6)

When read as a one, bit 5.53.6 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 14. When read as a zero, bit 5.53.6 indicates that the DTE XS receiver lane 14 has not achieved alignment marker lock. This bit reflects the state of amps_lock[14] (see 119.2.6.2.2).

45.2.5.16.3 Lane 13 aligned (5.53.5)

When read as a one, bit 5.53.5 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 13. When read as a zero, bit 5.53.5 indicates that the DTE XS receiver lane 13 has not achieved alignment marker lock. This bit reflects the state of amps_lock[13] (see 119.2.6.2.2).

45.2.5.16.4 Lane 12 aligned (5.53.4)

When read as a one, bit 5.53.4 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 12. When read as a zero, bit 5.53.4 indicates that the DTE XS receiver lane 12 has not achieved alignment marker lock. This bit reflects the state of amps_lock[12] (see 119.2.6.2.2).

45.2.5.16.5 Lane 11 aligned (5.53.3)

When read as a one, bit 5.53.3 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 11. When read as a zero, bit 5.53.3 indicates that the DTE XS receiver lane 11 has not achieved alignment marker lock. This bit reflects the state of amps_lock[11] (see 119.2.6.2.2).

45.2.5.16.6 Lane 10 aligned (5.53.2)

When read as a one, bit 5.53.2 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 10. When read as a zero, bit 5.53.2 indicates that the DTE XS receiver lane 10 has not achieved alignment marker lock. This bit reflects the state of amps_lock[10] (see 119.2.6.2.2).

45.2.5.16.7 Lane 9 aligned (5.53.1)

When read as a one, bit 5.53.1 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 9. When read as a zero, bit 5.53.1 indicates that the DTE XS receiver lane 9 has not achieved alignment marker lock. This bit reflects the state of amps_lock[9] (see 119.2.6.2.2).

45.2.5.16.8 Lane 8 aligned (5.53.0)

When read as a one, bit 5.53.0 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 8. When read as a zero, bit 5.53.0 indicates that the DTE XS receiver lane 8 has not achieved alignment marker lock. This bit reflects the state of amps_lock[8] (see 119.2.6.2.2).

45.2.5.17 DTE XS lane mapping, lane 0 register (Register 5.400)

The assignment of bits in the DTE XS lane mapping, lane 0 register is shown in Table 45–352. When the multi-lane DTE XS described in Clause 118 detects and locks the alignment marker for service interface lane 0, the detected PCS lane number is recorded in this register. The contents of the DTE XS lane mapping, lane 0 register is valid when Lane 0 aligned bit (5.52.0) is set to one and is invalid otherwise.

45.2.5.18 DTE XS lane mapping, lane 1 through lane 15 registers (Registers 5.401 through 5.415)

The definition of the DTE XS lane mapping, lane 1 through 15 registers is identical to that described for lane 0 in 45.2.5.17. The lane mapping for lane 1 is in register 5.401; lane 2 is in register 5.402; etc.

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Table 45–352—DTE XS lane mapping, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.400.15:5	Reserved	Value always 0	RO
5.400.4:0	Lane 0 mapping	DTE XS lane received in service interface lane 0	RO

[a]RO = Read only

45.2.5.19 DTE XS FEC symbol error counter lane 0 (Register 5.600, 5.601)

The assignment of bits in the DTE XS FEC symbol error counter lane 0 register is shown in Table 45–353. See 119.3.4 for a definition of this counter. Symbol errors detected in DTE XS FEC lane 0 are counted and shown in register 5.600.15:0 and 5.601.15:0. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 5.600, 5.601 are used to read the value of a 32-bit counter. When registers 5.600 and 5.601 are used to read the 32-bit counter value, the register 5.600 is read first, the value of the register 5.601 is latched when (and only when) register 5.600 is read, and reads of register 5.601 return the latched value rather than the current value of the counter.

Table 45–353—DTE XS FEC symbol error counter lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.600.15:0	DTE XS FEC symbol errors, lane 0 lower	FEC_symbol_error_counter_0[15:0]	RO, NR
5.601.15:0	DTE XS FEC symbol errors, lane 0 upper	FEC_symbol_error_counter_0[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.5.20 DTE XS FEC symbol error counter lane 1 through 15 (Registers 5.602 through 5.631)

The behavior of the DTE XS FEC symbol error counters, lane 1 through 15 is identical to that described for DTE XS FEC lane 0 in 45.2.5.19. Errors detected in each DTE XS FEC lane are counted and shown in the corresponding register. DTE XS FEC lane 1, lower 16 bits are shown in register 5.602; DTE XS FEC lane 1, upper 16 bits are shown in register 5.603; DTE XS FEC lane 2, lower 16 bits are shown in register 5.604; through register 5.631 for DTE XS FEC lane 15, upper 16 bits.

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45.2.5.21 DTE XS FEC control register (Register 5.800)

The assignment of bits in the DTE XS FEC control register is shown in Table 45–354.

Table 45–354—DTE XS FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
5.800.15:2	Reserved	Value always 0	RO
5.800.2	DTE XS FEC degraded SER enable	1 = FEC decoder signals degraded SER 0 = FEC decoder does not signal degraded SER	R/W
5.800.1	DTE XS FEC bypass indication enable	1 = FEC decoder does not indicate errors 0 = FEC decoder indicates errors	R/W
5.800.0	Reserved	Value always 0	RO

[a]R/W = Read/Write, RO = Read only

45.2.5.21.1 DTE XS FEC degraded SER enable (5.800.2)

This bit enables the DTE XS FEC decoder to signal the presence of a degraded SER. When set to a one, this bit enables degraded SER signaling. When set to a zero, degraded SER signaling is disabled. Writes to this bit are ignored and reads return a zero if the DTE XS FEC does not have the ability to signal the presence of a degraded SER (see 119.2.5.3 for equivalent PCS behavior).

45.2.5.21.2 DTE XS FEC bypass indication enable (5.800.1)

This bit enables the DTE XS FEC decoder to bypass error indication to the upper layers through the sync bits. When set to a one, this bit enables bypass of the error indication. When set to a zero, errors are indicated to the upper layers through the sync bits. Writes to this bit are ignored and reads return a zero if the DTE XS FEC does not have the ability to bypass indicating decoding errors (see 119.2.5.3 for equivalent PCS behavior).

45.2.5.22 DTE XS FEC status register (Register 5.801)

The assignment of bits in the DTE XS FEC status register is shown in Table 45–355.

Table 45–355—DTE XS FEC status register bit definitions

Bit(s)	Name	Description	R/W[a]
5.801.15:7	Reserved	Value always 0	RO
5.801.6	Local degraded SER received	1 = local degraded SER received 0 = no local degraded SER received	RO
5.801.5	Remote degraded SER received	1 = remote degraded SER received 0 = no remote degraded SER received	RO
5.801.4	DTE XS FEC degraded SER	1 = SER is degraded 0 = SER is not degraded	RO

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Table 45–355—DTE XS FEC status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
5.801.3	DTE XS FEC degraded SER ability	1 = FEC decoder has the ability to signal the presence of a degraded SER 0 = FEC decoder does not have the ability to signal the presence of a degraded SER	RO
5.801.2	DTE XS FEC high SER	1 = FEC errors have exceeded threshold 0 = FEC errors have not exceeded threshold	RO/LH
5.801.1	DTE XS FEC bypass indication ability	1 = FEC decoder has the ability to bypass error indication 0 = FEC decoder does not have the ability to bypass error indication	RO
5.801.0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high

45.2.5.22.1 Local degraded SER received (5.801.6)

When read as a one, bit 5.801.6 indicates that the local degraded SER signal has been received. This bit reflects the state of rx_local_degraded (see 118.2.1) for the DTE XS.

45.2.5.22.2 Remote degraded SER received (5.801.5)

When read as a one, bit 5.801.5 indicates that the remote degraded SER signal has been received. This bit reflects the state of rx_rm_degraded for the DTE XS (see 119.2.6.2.2 for equivalent PCS behavior).

45.2.5.22.3 DTE XS FEC degraded SER (5.801.4)

When DTE XS FEC degraded SER enable (bit 5.800.2) is set to one, bit 5.801.4 is set to one if the number of FEC symbol errors in a window of DTE XS FEC degraded SER interval (registers 5.810 and 5.811) codewords exceeds the DTE XS FEC degraded SER activate threshold (registers 5.806 and 5.807) and is cleared if the number of FEC symbol errors in the same window is below the DTE XS FEC degraded SER deactivate threshold (registers 5.808 and 5.809). If the number of FEC symbol errors in the window is between the two thresholds, then bit 5.801.4 remains in its previous state. The bit is set to zero if DTE XS FEC degraded SER enable (bit 5.800.2) is set to zero (see 119.2.5.3 for equivalent PCS behavior). The value of bit 5.801.4 is undefined if the value of the DTE XS FEC degraded SER activate threshold is less than the value of the DTE XS FEC degraded SER deactivate threshold.

45.2.5.22.4 DTE XS FEC degraded SER ability (5.801.3)

The DTE XS FEC decoder may have the option to signal the presence of a degraded SER (see 119.2.5.3 for equivalent PCS behavior). This bit is set to one to indicate that the decoder has the ability to signal the presence of a degraded SER. The bit is set to zero if this ability is not supported.

45.2.5.22.5 DTE XS FEC high SER (5.801.2)

When DTE XS FEC bypass indication enable (bit 5.800.1) is set to one, this bit is set to one if the number of FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 119.2.5.3) and is set to zero otherwise. The bit is set to zero if DTE XS FEC bypass indication enable (bit 5.800.1) is set to zero. This bit shall be implemented with latching high behavior.

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45.2.5.22.6 DTE XS FEC bypass indication ability (5.801.1)

The DTE XS FEC decoder may have the option to perform error detection without error indication (see 119.2.5.3) to reduce the delay contributed by the FEC decoder. This bit is set to one to indicate that the decoder has this ability to bypass error indication. The bit is set to zero if this ability is not supported.

45.2.5.23 DTE XS FEC corrected codewords counter (Register 5.802, 5.803)

The assignment of bits in the DTE XS FEC corrected codewords counter register is shown in Table 45–356. See 119.3.2 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 5.802, 5.803 are used to read the value of a 32-bit counter. When registers 5.802 and 5.803 are used to read the 32-bit counter value, the register 5.802 is read first, the value of the register 5.803 is latched when (and only when) register 5.802 is read, and reads of register 5.803 return the latched value rather than the current value of the counter.

Table 45–356—DTE XS FEC corrected codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
5.802.15:0	FEC corrected codewords lower	FEC_corrected_cw_counter[15:0]	RO, NR
5.803.15:0	FEC corrected codewords upper	FEC_corrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.5.24 DTE XS FEC uncorrected codewords counter (Register 5.804, 5.805)

The assignment of bits in the DTE XS FEC uncorrected codewords counter register is shown in Table 45–357. See 119.3.3 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 5.804, 5.805 are used to read the value of a 32-bit counter. When registers 5.804 and 5.805 are used to read the 32-bit counter value, the register 5.804 is read first, the value of the register 5.805 is latched when (and only when) register 5.804 is read, and reads of register 5.805 return the latched value rather than the current value of the counter.

Table 45–357—DTE XS FEC uncorrected codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
5.804.15:0	FEC uncorrected codewords lower	FEC_uncorrected_cw_counter[15:0]	RO, NR
5.805.15:0	FEC uncorrected codewords upper	FEC_uncorrected_cw_counter[31:16]	RO, NR

[a]RO = Read only, NR = Non Roll-over

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45.2.5.25 DTE XS FEC degraded SER activate threshold register (Register 5.806, 5.807)

The assignment of bits in the DTE XS FEC degraded SER activate threshold register is shown in Table 45–358. The value controls the threshold used to set the DTE XS FEC degraded SER bit (5.801.4) in an equivalent manner to that defined for the FEC_degraded_SER bit in 119.2.5.3.

Table 45–358—DTE XS FEC degraded SER activate threshold register bit definitions

Bit(s)	Name	Description	R/W[a]
5.806.15:0	DTE XS FEC degraded SER activate threshold lower	FEC_degraded_SER_activate_threshold[15:0]	R/W
5.807.15:0	DTE XS FEC degraded SER activate threshold upper	FEC_degraded_SER_activate_threshold[31:16]	R/W

[a]R/W = Read/Write

45.2.5.26 DTE XS FEC degraded SER deactivate threshold register (Register 5.808, 5.809)

The assignment of bits in the DTE XS FEC degraded SER deactivate threshold register is shown in Table 45–359. The value controls the threshold used to clear the DTE XS FEC degraded SER bit (5.801.4) in an equivalent manner to that defined for the FEC_degraded_SER bit in 119.2.5.3.

Table 45–359—DTE XS FEC degraded SER deactivate threshold register bit definitions

Bit(s)	Name	Description	R/W[a]
5.808.15:0	DTE XS FEC degraded SER deactivate threshold lower	FEC_degraded_SER_deactivate_threshold[15:0]	R/W
5.809.15:0	DTE XS FEC degraded SER deactivate threshold upper	FEC_degraded_SER_deactivate_threshold[31:16]	R/W

[a]R/W = Read/Write

45.2.5.27 DTE XS FEC degraded SER interval register (Register 5.810, 5.811)

The assignment of bits in the DTE XS FEC degraded SER interval register is shown in Table 45–360. The value controls the interval used to set and clear the DTE XS FEC degraded SER bit (5.801.4) in an equivalent manner to that defined for the FEC_degraded_SER bit in 119.2.5.3.

Table 45–360—DTE XS FEC degraded SER interval register bit definitions

Bit(s)	Name	Description	R/W[a]
5.810.15:0	DTE XS FEC degraded SER interval lower	FEC_degraded_SER_interval[15:0]	R/W
5.811.15:0	DTE XS FEC degraded SER interval upper	FEC_degraded_SER_interval[31:16]	R/W

[a]R/W = Read/Write

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45.2.5.28 TimeSync DTE XS capability (Register 5.1800)

The TimeSync DTE XS capability register (see Table 45–361) indicates the capability of the DTE XS to report the transmit and receive data delay, stored in registers 5.1801 through 5.1804 and 5.1805 through 5.1808, respectively.

Table 45–361—TimeSync DTE XS capability

Bit(s)	Name	Description	R/W[a]
5.1800.15:2	Reserved	Value always 0	RO
5.1800.1	TimeSync transmit path data delay	1 = DTE XS provides information on transmit path data delay in registers 5.1801 through 5.1804 0 = DTE XS does not provide information on transmit path data delay	RO
5.1800.0	TimeSync receive path data delay	1 = DTE XS provides information on receive path data delay in registers 5.1805 through 5.1808 0 = DTE XS does not provide information on receive path data delay	RO

[a]RO = Read only

45.2.5.29 TimeSync DTE XS transmit path data delay (Registers 5.1801, 5.1802, 5.1803, 5.1804)

The TimeSync DTE XS transmit path data delay register contains the maximum (registers 5.1801, 5.1802, see Table 45–362) and minimum (registers 5.1803, 5.1804, see Table 45–362) values of the transmit path data delay. The transmit path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in register 1.1 (see 45.2.1.2.4).

Table 45–362—TimeSync DTE XS transmit path data delay register

Bit(s)	Name	Description	R/W[a]
5.1801.15:0	Maximum DTE XS transmit path data delay, lower	DTE_XS_delay_TX_max [15:0]	RO, MW
5.1802.15:0	Maximum DTE XS transmit path data delay, upper	DTE_XS_delay_TX_max [31:16]	RO, MW
5.1803.15:0	Minimum DTE XS transmit path data delay, lower	DTE_XS_delay_TX_min [15:0]	RO, MW
5.1804.15:0	Minimum DTE XS transmit path data delay, upper	DTE_XS_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.5.30 TimeSync DTE XS receive path data delay (Registers 5.1805, 5.1806, 5.1807, 5.1808)

The TimeSync DTE XS receive path data delay register contains the maximum (registers 5.1805, 5.1806, see Table 45–363) and minimum (registers 5.1807, 5.1808, see Table 45–363) values of the receive path

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data delay. The receive path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in register 5.1 (see 45.2.5.2.7).

Table 45–363—TimeSync DTE XS receive path data delay register

Bit(s)	Name	Description	R/W[a]
5.1805.15:0	Maximum DTE XS receive path data delay, lower	DTE_XS_delay_RX_max [15:0]	RO, MW
5.1806.15:0	Maximum DTE XS receive path data delay, upper	DTE_XS_delay_RX_max [31:16]	RO, MW
5.1807.15:0	Minimum DTE XS receive path data delay, lower	DTE_XS_delay_RX_min [15:0]	RO, MW
5.1808.15:0	Minimum DTE XS receive path data delay, upper	DTE_XS_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.6 TC registers

The assignment of registers in the TC MMD is shown in Table 45–364.

Table 45–364—TC registers

Register address	Register name	Subclause
6.0	TC control	45.2.6.1
6.1	Reserved	
6.2, 6.3	TC device identifier	45.2.6.2
6.4	TC speed ability	45.2.6.3
6.5, 6.6	TC devices in package	45.2.6.4
6.7 through 6.13	Reserved	
6.14, 6.15	TC package identifier	45.2.6.5
6.16	10P/2B aggregation discovery control[a]	45.2.6.6
6.17	10P/2B aggregation and discovery status[a]	45.2.6.7
6.18, 6.19, 6.20	10P/2B aggregation discovery code[a]	45.2.6.8
6.21	10P/2B link partner PME aggregate control[a]	45.2.6.9
6.22, 6.23	10P/2B link partner PME aggregate data[a]	45.2.6.10
6.24	10P/2B TC CRC error counter	45.2.6.11
6.25, 6.26	10P/2B TPS-TC coding violations counter	45.2.6.12
6.27	10P/2B TC indications	45.2.6.13

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Table 45–364—TC registers *(continued)*

Register address	Register name	Subclause
6.28 through 6.1799	Reserved	
6.1800	TimeSync TC capability	45.2.6.14
6.1801 through 6.1804	TimeSync TC transmit path data delay	45.2.6.15
6.1805 through 6.1808	TimeSync TC receive path data delay	45.2.6.16
6.1809 through 6.32767	Reserved	
6.32 768 through 6.65 535	Vendor specific	

[a]Register is defined only for -O port types and is reserved for -R ports

45.2.6.1 TC control register (Register 6.0)

The assignment of bits in the TC control register is shown in Table 45–365. The default value for each bit of the TC control register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45–365—TC control register bit definitions

Bit(s)	Name	Description	R/W[a]
6.0.15	Reset	1 = TC reset 0 = Normal operation	R/W SC
6.0.14	Reserved	Value always 0	RO
6.0.13	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
6.0.12:7	Reserved	Value always 0	RO
6.0.6	Speed selection	13 6 1 1 = bits 5:2 select speed 0 x = unspecified x 0 = unspecified	R/W
6.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = Reserved	R/W
6.0.1:0	Reserved	Value always 0	RO

[a]R/W = Read/Write, SC = Self-clearing, RO = Read only

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45.2.6.1.1 Reset (6.0.15)

Resetting a TC is accomplished by setting bit 6.0.15 to a one. This action shall set all TC registers to their default states. As a consequence, this action may change the internal state of the TC and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a TC shall return a value of one in bit 6.0.15 when a reset is in progress; otherwise, it shall return a value of zero. A TC is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 6.0.15. During a reset, a TC shall respond to reads from register bit 6.0.15.

NOTE—This operation may interrupt data communication. The data path of a TC, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset.

45.2.6.1.2 Speed selection (6.0.13, 6.0.6, 6.0.5:2)

Speed selection bits 6.0.13 and 6.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The operating mode of the TC may be selected using bits 5 through 2. The abilities of the TC are advertised in the TC speed ability register. A TC may ignore writes to the TC speed selection bits that select speeds it has not advertised in the TC speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The speed selection bits 6.0.5:2, when set to 0001, select the use of the 10PASS-TS and 2BASE-TL TC.

The TC speed selection defaults to a supported ability.

45.2.6.2 TC device identifier (Registers 6.2 and 6.3)

Registers 6.2 and 6.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of TC. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A TC may return a value of zero in each of the 32 bits of the TC device identifier.

The format of the TC device identifier is specified in 22.2.4.3.1.

45.2.6.3 TC speed ability (Register 6.4)

The assignment of bits in the TC speed ability register is shown in Table 45–366.

Table 45–366—TC speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
6.4.15:1	Reserved for future speeds	Value always 0	RO
6.4.1	10PASS-TS/2BASE-TL capable	1 = TC is capable of operating as the 10P/2B TC 0 = TC is not capable of operating as the 10P/2B TC	RO
6.4.0	Reserved	Value always 0	RO

[a]RO = Read only

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45.2.6.3.1 10PASS-TS/2BASE-TL capable (6.4.1)

When read as a one, this bit indicates that the TC is able to operate as the 10PASS-TS/2BASE-TL TC, as specified in Clause 61.

45.2.6.4 TC devices in package registers (Registers 6.5, 6.6)

The TC devices in package registers are defined in Table 45–2.

45.2.6.5 TC package identifier registers (Registers 6.14, 6.15)

Registers 6.14 and 6.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the TC MMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A TC may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the package identifier is specified in 22.2.4.3.1.

45.2.6.6 10P/2B aggregation discovery control register (Register 6.16)

The 10P/2B aggregation discovery control register allows the STA of an -O port to determine the aggregation capabilities of an -R link-partner.

The 10P/2B aggregation discovery control register shall be implemented as a unique register for each TC MMD in a package. For example, a package implementing four PHYs would have four independent instances of the 10P/2B aggregation discovery control register, accessed by a read or write to each PHY.

For information on the encoding of this function on the physical link, see 61.4.7.

This register is defined for -O port subtypes only. The register bit definitions for the 10P/2B aggregation discovery control register are shown in Table 45–367.

Table 45–367—10P/2B aggregation discovery control register bit definitions

Bit(s)	Name	Description	R/W[a]
6.16.15:2	Reserved	Value always 0	RO
6.16.1:0	Discovery operation	01 = Ready (default) 00 = Set if clear 11 = Clear if same 10 = Get	R/W

[a]RO = Read only, R/W = Read/Write

45.2.6.6.1 Discovery operation (6.16.1:0)

The Discovery operation bits are used to query and manipulate the remote discovery register. The remote discover register is not a Clause 45 object, but a variable of the PME aggregation PCS function on -R ports. The Discovery operation makes use of G.994.1 handshaking messages, therefore valid only when the link

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status is down (i.e., neither Initializing nor Up). Attempts to perform an operation while the link is Initializing or Up shall be ignored.

The default state of these bits is “Ready”. The bits shall indicate “Ready” any time the PME aggregation function is capable of performing an operation on the remote discovery register. If PAF is not supported, the discovery operation bits shall indicate “Ready” and ignore writes. These bits shall return to the “Ready” state upon MMD Reset.

If the STA sets the bits to “Get,” the PME aggregation function queries the remote discovery register and returns its contents to the aggregation discovery code register.

If the STA sets the bits to “Set if clear,” the PME aggregation function passes a message to the -R PCS instructing it to set the remote discovery register to the contents of the aggregation discovery code register, but only if the remote discovery register is all zeros.

If the STA sets the bits to “Clear if same,” the PME aggregation function passes a message to the -R PCS instructing it to clear the remote discovery register, but only if the contents of the remote discovery register currently match the contents of the aggregation discovery code register.

While the requested operation is in progress, the PHY maintains the operation value in the bits. After the operation is complete, the PHY shall set the bits to indicate “Ready”. If the operation does not complete within a 255 second time-out, the discovery operation result bit (6.17.0) will be set to “1” (operation unsuccessful), and the discovery operation bits will be set to “Ready”.

45.2.6.7 10P/2B aggregation and discovery status register (Register 6.17)

The 10P/2B aggregation and discovery status register is defined for -O port subtypes only.

The assignment of bits in the 10P/2B aggregation and discovery status register is shown in Table 45–368.

Table 45–368—10P/2B aggregation and discovery status register bit definitions

Bit(s)	Name	Description	R/W[a]
6.17.15:2	Reserved	Value always 0	RO
6.17.1	Link partner aggregate operation result	1 = operation unsuccessful 0 = operation completed successfully (default)	RO, LH
6.17.0	Discovery operation result	1 = operation unsuccessful 0 = discovery operation completed successfully (default)	RO, LH

[a]RO = Read only, LH = Latching high

45.2.6.7.1 Link partner aggregate operation result (6.17.1)

When a link partner aggregate operation is complete, the PHY sets this bit to indicate the result of the operation. A “1” indicates that the operation could not be completed. This may be for a variety of reasons:

a) PMA/PMD link status is initializing or up.
b) The link partner is not present or not responding.

If PAF is not supported, this bit shall remain set to zero.

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45.2.6.7.2 Discovery operation result (6.17.0)

When a discovery operation is complete, the PHY sets this bit to indicate the result of the operation. A "1" indicates that the operation could not be completed. This may be for a variety of reasons:

a) PMA/PMD link status is initializing or up.
b) A "Set if clear" operation was requested but the remote discovery register was not clear.
c) A "Clear if same" operation was requested but the remote discovery register did not match the aggregation discovery code register.
d) The link partner is not present or not responding.

If PAF is not supported, this bit shall read as zero.

45.2.6.8 10P/2B aggregation discovery code (Registers 6.18, 6.19, 6.20)

The 10P/2B aggregation discovery code registers store the value of the remote_discovery_register exchanged with the -R link partner.

This register is defined for -O port subtypes only.

These registers shall be implemented as unique registers for each TC MMD in a package. For example, a package implementing four TCs would have four independent instances of the 10P/2B aggregation discovery code registers, accessed by a read or write to each PHY.

For information on the encoding of this function on the physical link, please see 61.4.7.

The assignment of bits for the 10P/2B aggregation discovery code registers are shown in Table 45–369.

Table 45–369—10P/2B aggregation discovery code bit definitions

Bit(s)	Name	Description	R/W[a]
6.18.15:0	Code [47:32]	The two most significant octets of the aggregation discovery code	R/W
6.19.15:0	Code [31:16]	The two middle octets of the aggregation discovery code	R/W
6.20.15:0	Code [15:0]	The two least significant octets of the aggregation discovery code	R/W

[a]R/W = Read/Write

45.2.6.9 10P/2B link partner PME aggregate control register (Register 6.21)

The 10P/2B link partner PME aggregate control register allows the STA of an -O port to read and write the remote PME_Aggregate_register (see 61.2.2.8.3).

The 10P/2B link partner PME aggregate control register shall be implemented as a unique register for each TC MMD in a package. For example, a package implementing four TCs would have four independent instances of the 10P/2B link partner PME aggregate control register, accessed by a read or write to each PHY.

This register is defined for -O port subtypes only.

The register bit definitions for the 10P/2B link partner PME aggregate control register are shown in Table 45–370.

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Table 45–370—10P/2B link partner PME aggregate control register bit definitions

Bit(s)	Name	Description	R/W[a]
6.21.15:2	Reserved	Value always 0	RO
6.21.1:0	Link partner aggregate operation	01 = Ready (default) 00 = Set 11 = invalid 10 = Get	R/W

[a]RO = Read only, R/W = Read/Write

45.2.6.9.1 Link partner aggregate operation (6.21.1:0)

The Link partner aggregate operation bits are used to query and manipulate the remote PME_Aggregate_register. This operation makes use of G.994.1 handshaking messages and therefore is performed only when the link status is down (i.e., neither Initializing nor Up). Attempts to perform an operation while the link is Initializing or Up shall be ignored.

The default state of these bits is "Ready." The bits shall indicate "Ready" any time the PME aggregation function is capable of performing an operation on the remote PME_Aggregate_register. If PAF is not supported, the link partner aggregate operation bits shall indicate "Ready" ignore writes. These bits shall return to the "Ready" state upon MMD Reset.

If the STA sets the bits to "Get," the PME aggregation function queries the remote PME_Aggregate_register and returns its contents to the 10P/2B link partner PME aggregate data register (see 45.2.6.10).

If the STA sets the bits to "Set," the PME aggregation function passes a message to the -R PCS instructing it to set the bit location in the remote PME_Aggregate_register corresponding to the TC on which the message was received to the contents of bit 0 of the 10P/2B link partner PME aggregate data register.

While the requested operation is in progress, the PHY maintains the operation value in the bits. After the operation is complete, the PHY shall set the bits to indicate "Ready".

45.2.6.10 10P/2B link partner PME aggregate data (Registers 6.22, 6.23)

The 10P/2B link partner PME aggregate data registers store the data for the link partner aggregate operation. This register either contains the result of a "Get" operation, the data sent in a "Set" operation, or all zeros following an MMD reset.

These registers are defined for -O port subtypes only.

These registers shall be implemented as unique registers for each TC MMD in a package. For example, a package implementing four TCs would have four independent instances of the registers, accessed by a read or write to each PHY.

The assignment of bits for the 10P/2B link partner PME aggregate data registers are shown in Table 45–371.

Table 45–371—10P/2B link partner PME aggregate data registers bit definitions

Bit(s)	Name	Description	R/W[a]
6.22.15:0	Data[31:16]	The two most significant octets of the link partner PME aggregate data	R/W
6.23.15:0	Data[15:0]	The two least significant octets of the link partner PME aggregate data	R/W

[a]R/W = Read/Write

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45.2.6.11 10P/2B TC CRC error register (Register 6.24)

The 10P/2B TC CRC error register is a 16 bit counter that contains the number of TC frames received with the TC_CRC_error primitive asserted, defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B TC CRC error register are shown in Table 45–372.

Table 45–372—10P/2B TC CRC error register bit definitions

Bit(s)	Name	Description	R/W[a]
6.24.15:0	CRC errors[15:0]	The bytes of the counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.6.12 10P/2B TPS-TC coding violations counter (Registers 6.25, 6.26)

The 10P/2B TPS-TC coding violations counter is a 32-bit counter that contains the number of 64/64-octet encapsulation errors, defined in 61.3.3.1. This counter increments for each 64/65-octet received with the TC_coding_error signal asserted. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B TPS-TC coding violations counter are shown in Table 45–373.

Table 45–373—10P/2B TPS-TC coding violations counter bit definitions

Bit(s)	Name	Description	R/W[a]
6.25.15:0	Coding violations[31:16]	The high order bytes of the counter	RO, MW
6.26.15:0	Coding violations[15:0]	The low order bytes of the counter	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.6.13 10P/2B TC indications register (Register 6.27)

The 10P/2B TC indications register reflects the state of the TC sync detect state diagram and the state of the link partner TC sync detect state diagram (if present) (see 61.3.3.5). The assignment of bits in the 10P/2B TC indications register is shown in Table 45–374.

Table 45–374—10P/2B TC indications register bit definitions

Bit(s)	Name	Description	R/W[a]
6.27.15:9	Reserved	Value always 0	RO
6.27.8	Local TC synchronized	1 = TC_synchronized is TRUE 0 = TC_synchronized is FALSE	RO
6.27.7:1	Reserved	Value always 0	RO
6.27.0	Remote TC synchronized	1 = remote_TC_out_of_sync is FALSE 0 = remote_TC_out_of_sync is TRUE	RO

[a]RO = Read only

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45.2.6.13.1 Local TC synchronized (6.27.8)

This bit is read as a one when the TC_synchronized variable in the TC sync detect state diagram is TRUE (see 61.3.3.8). In all other cases, this bit is read as zero.

45.2.6.13.2 Remote TC synchronized (6.27.0)

This bit is read as a one when the remote_TC_out_of_sync variable in the link partner TC sync detect state diagram is FALSE (see 61.3.3.8). In all other cases, this bit is read as zero.

45.2.6.14 TimeSync TC capability (Register 6.1800)

The TimeSync TC capability register (see Table 45–375) indicates the capability of the TC to report the transmit and receive data delay, stored in registers 6.1801 through 6.1804 and 6.1805 through 6.1808, respectively.

Table 45–375—TimeSync TC capability

Bit(s)	Name	Description	R/W[a]
6.1800.15:2	Reserved	Value always 0	RO
6.1800.1	TimeSync transmit path data delay	1 = TC provides information on transmit path data delay in registers 6.1801 through 6.1804 0 = TC does not provide information on transmit path data delay	RO
6.1800.0	TimeSync receive path data delay	1 = TC provides information on receive path data delay in registers 6.1805 through 6.1808 0 = TC does not provide information on receive path data delay	RO

[a]RO = Read only

45.2.6.15 TimeSync TC transmit path data delay (Registers 6.1801, 6.1802, 6.1803, 6.1804)

The TimeSync TC transmit path data delay register contains the maximum (registers 6.1801, 6.1802, see Table 45–376) and minimum (registers 6.1803, 6.1804, see Table 45–376) values of the transmit path data delay. The transmit path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in register 1.1 (see 45.2.1.2.4).

Table 45–376—TimeSync TC transmit path data delay register

Bit(s)	Name	Description	R/W[a]
6.1801.15:0	Maximum TC transmit path data delay, lower	TC_delay_TX_max [15:0]	RO, MW
6.1802.15:0	Maximum TC transmit path data delay, upper	TC_delay_TX_max [31:16]	RO, MW
6.1803.15:0	Minimum TC transmit path data delay, lower	TC_delay_TX_min [15:0]	RO, MW
6.1804.15:0	Minimum TC transmit path data delay, upper	TC_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

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45.2.6.16 TimeSync TC receive path data delay (Registers 6.1805, 6.1806, 6.1807, 6.1808)

The TimeSync TC receive path data delay register contains the maximum (registers 6.1805, 6.1806, see Table 45–377) and minimum (registers 6.1807, 6.1808, see Table 45–377) values of the receive path data delay. The receive path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in register 1.1 (see 45.2.1.2.4).

Table 45–377—TimeSync TC receive path data delay register

Bit(s)	Name	Description	R/W[a]
6.1805.15:0	Maximum TC receive path data delay, lower	TC_delay_RX_max [15:0]	RO, MW
6.1806.15:0	Maximum TC receive path data delay, upper	TC_delay_RX_max [31:16]	RO, MW
6.1807.15:0	Minimum TC receive path data delay, lower	TC_delay_RX_min [15:0]	RO, MW
6.1808.15:0	Minimum TC receive path data delay, upper	TC_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

45.2.7 Auto-Negotiation registers

The assignment of registers in the Auto-Negotiation (AN) MMD is shown in Table 45–378.

Table 45–378—Auto-Negotiation MMD registers

Register address	Register name	Subclause
7.0	AN control	45.2.7.1
7.1	AN status	45.2.7.2
7.2, 7.3	AN device identifier	45.2.7.3
7.4	Reserved	
7.5, 7.6	AN devices in package	45.2.7.4
7.7 through 7.13	Reserved	
7.14, 7.15	AN package identifier	45.2.7.5
7.16 through 7.18	AN advertisement	45.2.7.6
7.19 through 7.21	AN LP Base Page ability	45.2.7.7
7.22 through 7.24	AN XNP transmit	45.2.7.8
7.25 through 7.27	AN LP XNP ability	45.2.7.9
7.28 through 7.31	Reserved	
7.32	MultiGBASE-T AN control 1	45.2.7.10
7.33	MultiGBASE-T AN status 1	45.2.7.11
7.34 through 7.47	Reserved	
7.48	Backplane Ethernet, BASE-R copper status	45.2.7.12
7.49	Backplane Ethernet, BASE-R copper status 2	45.2.7.13
7.50 through 7.59	Reserved	

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Table 45–378—Auto-Negotiation MMD registers *(continued)*

Register address	Register name	Subclause
7.60	EEE advertisement 1	45.2.7.14
7.61	EEE link partner ability 1	45.2.7.15
7.62	EEE advertisement 2	45.2.7.16
7.63	EEE link partner ability 2	45.2.7.17
7.64	MultiGBASE-T AN control 2	45.2.7.18
7.65	MultiGBASE-T AN status 2	45.2.7.19
7.66 through 7.511	Reserved	
7.512	BASE-T1 AN control	45.2.7.20
7.513	BASE-T1 AN status	45.2.7.21
7.514 through 7.516	BASE-T1 AN advertisement	45.2.7.22
7.517 through 7.519	BASE-T1 AN LP Base Page ability	45.2.7.23
7.520 through 7.522	BASE-T1 AN Next Page transmit	45.2.7.24
7.523 through 7.525	BASE-T1 AN LP Next Page ability	45.2.7.25
7.526	10BASE-T1 AN control	45.2.7.26
7.527	10BASE-T1 AN status	45.2.7.27
7.528 through 7.32767	Reserved	
7.32768 through 7.65535	Vendor specific	

45.2.7.1 AN control register (Register 7.0)

The assignment of bits in the AN control register is shown in Table 45–379. The default value for each bit of the AN control register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45–379—AN control register bit definitions

Bit(s)	Name	Description	R/W[a]
7.0.15	AN reset	1 = AN reset 0 = AN normal operation	R/W SC
7.0.14	Reserved	Value always 0	RO
7.0.13	Extended Next Page control	1 = Extended Next Pages are enabled 0 = Extended Next Pages are disabled	R/W
7.0.12	Auto-Negotiation enable	1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	R/W
7.0.11:10	Reserved	Value always 0	RO

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Table 45–379—AN control register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
7.0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation process 0 = Auto-Negotiation in process, disabled, or not supported	R/W SC
7.0.8:0	Reserved	Value always 0	RO

[a]R/W = Read/Write, SC = Self-clearing, RO = Read only

A device that supports multiple port types may implement both Clause 22 control register operation and Clause 45 control register operation. Some control functions have been duplicated in both definitions. The register bits to control these functions are simply echoed in both locations; any reads or writes to these bits behave identically whether made through the Clause 22 location or the Clause 45 location.

45.2.7.1.1 AN reset (7.0.15)

Resetting AN is accomplished by setting bit 7.0.15 to a one. This action shall set all AN registers to their default states. As a consequence, this action may change the internal state of AN and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and AN shall return a value of one in bit 7.0.15 when a reset is in progress and a value of zero otherwise. AN is not required to accept a write transaction to any of its registers until the reset process is complete. The reset process shall be completed within 0.5 s from the setting of bit 7.0.15. During an AN reset, AN shall respond to reads from register bit 7.0.15. All other register bits should be ignored.

The default value for bit 7.0.15 is zero. See 22.2.4.1.1.

NOTE—This operation may interrupt data communication.

45.2.7.1.2 Extended Next Page control (7.0.13)

When bit 7.0.13 is set to one, Extended Next Page(s) are exchanged if the device(s) is/are capable. If a device intends to enable the exchange of Extended Next Page, it shall set bit 7.0.13 to one. A device may choose not to exchange Extended Next Page by setting bit 7.0.13 to zero. The Extended Next Page function is defined in 28.2.3.4. Setting of this bit shall have no effect if Extended Next Page ability bit 7.16.12 is set to zero.

The default value for bit 7.0.13 is one if bit 7.16.12 is one. Otherwise, bit 7.0.13 defaults to zero.

45.2.7.1.3 Auto-Negotiation enable (7.0.12)

The Auto-Negotiation function shall be enabled by setting bit 7.0.12 to a one. If bit 7.0.12 is set to one, then speed selection bits 1.0.13, 1.0.6, and bits 1.0.5:2 in PHY control register 1 and PHY type selection bits 1.7.3:0 in PHY control register 2 shall have no effect on the link configuration, and the Auto-Negotiation process determines the link configuration. If bit 7.0.12 is cleared to zero, then bits 1.0.13, 1.0.6, and bits 1.0.5:2 in control register 1 and type selection bit 1.7.3:0 in control register 2 determines the link configuration regardless of the prior state of the link configuration and the Auto-Negotiation process. Bit 7.0.12 is a copy of bit 0.12 in register 0 if present (see 22.2.4.1.4).

The default value of bit 7.0.12 is one, unless the PHY reports via bit 7.1.3 or 1.3 if present (see 22.2.4.2.12) that it lacks the ability to perform Auto-Negotiation, in which case the default value of bit 7.0.12 is zero (see 22.2.4.1.4).

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45.2.7.1.4 Restart Auto-Negotiation (7.0.9)

If the PMA/PMD reports (via bit 7.1.3) that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the PMA/PMD shall return a value of zero in bit 7.0.9 and any attempt to write a one to bit 7.0.9 shall be ignored.

Otherwise, the Auto-Negotiation process shall be restarted by setting bit 7.0.9 to one. This bit is self-clearing, and a PMA/PMD shall return a value of one in bit 7.0.9 until the Auto-Negotiation process has been initiated. If Auto-Negotiation was completed prior to this bit being set, the process shall be reinitiated. The Auto-Negotiation process shall not be affected by clearing this bit to zero. Bit 7.0.9 is a copy of 0.9 in register 0, if present (see 22.2.4.1.7).

The default value for 7.0.9 is zero (see 22.2.4.1.7).

45.2.7.2 AN status (Register 7.1)

The assignment of bits in the AN status register is shown in Table 45–380. All the bits in the AN status register are read only; therefore, a write to the AN status register shall have no effect.

Table 45–380—AN status register

Bit(s)	Name	Description	R/W[a]
7.1.15:10	Reserved	Value always 0	RO
7.1.9	Parallel detection fault	1 = A fault has been detected via the parallel detection function. 0 = A fault has not been detected via the parallel detection function.	RO LH
7.1.8	Reserved	Value always 0	RO
7.1.7	Extended Next Page status	1 = Extended Next Page format is used 0 = Extended Next Page is not allowed	RO
7.1.6	Page received	1 = A page has been received 0 = A page has not been received	RO LH
7.1.5	Auto-Negotiation complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
7.1.4	Remote fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO LH
7.1.3	Auto-Negotiation ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
7.1.2	Link status	1 = Link is up 0 = Link is down	RO LL
7.1.1	Reserved	Value always 0	RO
7.1.0	Link partner Auto-Negotiation ability	1 = LP is able to perform Auto-Negotiation 0 = LP is not able to perform Auto-Negotiation	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.7.2.1 Parallel detection fault (7.1.9)

The parallel detection Fault bit (7.1.9) shall be set to one to indicate that more than one of 1000BASE-KX, 2.5GBASE-KX, or 10GBASE-KX4 PMAs have indicated link_status=OK when the autoneg_wait_timer expires. The parallel detection fault bit shall be reset to zero on a read of the AN status register (register 7.1).

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45.2.7.2.2 Extended Next Page status (7.1.7)

When set to one, bit 7.1.7 indicates that both the local device and the link partner have indicated support for Extended Next Page. When set to zero, bit 7.1.7 indicates that Extended Next Page shall not be used. If bit 7.0.13 or bit 7.16.12 are set to zero then this bit shall not be set to one.

45.2.7.2.3 Page received (7.1.6)

The Page received bit (7.1.6) shall be set to one to indicate that a new link codeword has been received and stored in the AN LP Base Page ability registers 7.19 to 7.21 or AN LP XNP ability registers 7.25 to 7.27. The contents of the AN LP Base Page ability registers 7.19 to 7.21 are valid when bit 7.1.6 is set the first time during the Auto-Negotiation. The Page received bit shall be reset to zero on a read of the AN status register (register 7.1) or if present, the Auto-Negotiation expansion register 6 (see 28.2.4.1.5). This bit is a copy of bit 6.1 in register 6, if present (see 28.2.4.1.5).

45.2.7.2.4 Auto-Negotiation complete (7.1.5)

When read as a one, bit 7.1.5 indicates that the Auto-Negotiation process has been completed, and that the contents of the Auto-Negotiation register 7.16 and 7.19 are valid. When read as a zero, bit 7.1.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of 7.19, 7.22 through 7.27, and 7.33 registers are as defined by the current state of the Auto-Negotiation protocol, or as written for manual configuration. A PMA/PMD shall return a value of zero in bit 7.1.5 if Auto-Negotiation is disabled by clearing bit 7.0.12. A PMA/PMD shall also return a value of zero in bit 7.1.5 if it lacks the ability to perform Auto-Negotiation. Bit 7.1.5 is a copy of bit 1.5 in register 1, if present (see 22.2.4).

45.2.7.2.5 Remote fault (7.1.4)

When read as one, bit 7.1.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is AN specific. The remote fault bit shall be implemented with a latching function, such that the occurrence of a remote fault causes the bit 7.1.4 to become set and remain set until it is cleared. Bit 7.1.4 shall be cleared each time register 7.1 is read via the management interface, and shall also be cleared by a AN reset. Bit 7.1.4 is a copy of bit 1.4 in register 1, if present (see 22.2.4).

45.2.7.2.6 Auto-Negotiation ability (7.1.3)

When read as a one, bit 7.1.3 indicates that the PMA/PMD has the ability to perform Auto-Negotiation. When read as a zero, bit 7.1.3 indicates that the PMA/PMD lacks the ability to perform Auto-Negotiation. Bit 7.1.3 is a copy of bit 1.3 in register 1, if present (see 22.2.4).

45.2.7.2.7 Link status (7.1.2)

When read as a one, bit 7.1.2 indicates that the PMA/PMD has determined that a valid link has been established. When read as a zero, bit 7.1.2 indicates that the link has been invalid after this bit was last read. Bit 7.1.2 is set to one when the variable link_status equals OK and is cleared to zero when the variable link_status equals FAIL. The link status bit shall be implemented with a latching function, such that the occurrence of a link_status equals FAIL condition causes the link status bit to become cleared and remain cleared until it is read via the management interface. Bit 7.1.2 shall be cleared upon AN reset. This status indication is intended to support the management attribute defined in 30.5.1.1.4, aMediaAvailable.

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45.2.7.2.8 Link partner Auto-Negotiation ability (7.1.0)

The link partner Auto-Negotiation ability bit shall be set to one to indicate that the link partner is able to participate in the Auto-Negotiation function. This bit shall be reset to zero if the link partner is not Auto-Negotiation able.

45.2.7.3 Auto-Negotiation device identifier (Registers 7.2 and 7.3)

Registers 7.2 and 7.3 provide a 32-bit value, which may constitute a unique identifier for an Auto-Negotiation. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a 4-bit revision number. An Auto-Negotiation may return a value of zero in each of the 32 bits of the Auto-Negotiation device identifier.

The format of the Auto-Negotiation device identifier is specified in 22.2.4.3.1.

45.2.7.4 AN devices in package (Registers 7.5 and 7.6)

The AN devices in package registers are defined in Table 45–2.

45.2.7.5 AN package identifier (Registers 7.14 and 7.15)

Registers 7.14 and 7.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the Auto-Negotiation is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the OUI assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. An Auto-Negotiation MMD may return a value of zero in each of the 32 bits of the Auto-Negotiation package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the Auto-Negotiation package identifier is specified in 22.2.4.3.1.

45.2.7.6 AN advertisement register (7.16, 7.17, and 7.18)

If the BP AN ability bit (7.48.0) in the BP Ethernet status register is set to zero then only sixteen bits of the AN advertisement register are used and they are defined in 28.2.1.2.

If the BP AN ability bit (7.48.0) in the BP Ethernet status register is set to one then all forty eight bits are used and they are defined in 73.6.

The Selector field (7.16.4:0) is set to the IEEE 802.3 code as specified in Annex 28A. The Acknowledge bit (7.16.14) is set to zero.

The technology ability field, as defined in 28.2.1.2 and 73.6, represents the technologies supported by the local device. Only bits representing supported technologies may be set. Management may clear bits in the technology ability field and restart Auto-Negotiation to negotiate an alternate common mode.

The management entity initiates renegotiation with the link partner using alternate abilities by setting the Restart Auto-Negotiation bit (7.0.9) in the AN control register to one.

Any writes to this register prior to completion of Auto-Negotiation, as indicated by bit 7.1.5, should be followed by a renegotiation for the new values to take effect. Once Auto-Negotiation has completed, software may examine this register along with the LP Base Page ability register to determine the highest common denominator technology.

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If the Auto-Negotiation advertisement register (register 4) is present, (see 28.2.4.1.3), then this register is a copy of the Auto-Negotiation advertisement register (register 4). In this case, reads to the AN advertisement register (7.16) report the value of the Auto-Negotiation advertisement register (register 4); writes to the AN advertisement register (7.16) cause a write to occur to the Auto-Negotiation advertisement register.

The Base Page value is transferred to mr_adv_ability when register 7.16 is written. Therefore, if used, registers 7.17 and 7.18 should be written before 7.16.

Table 45–381—AN advertisement register bit definitions

Bit(s)	Name	Description	R/W[a]
7.16.15	Next Page	See 28.2.1.2 and 73.6.9	R/W
7.16.14	Acknowledge	Value always 0, writes ignored	RO
7.16.13	Remote fault	See 28.2.1.2 and 73.6.7	R/W
7.16.12:5	D12:D5	See 28.2.1.2 and 73.6	R/W
7.16.4:0	Selector field	See Annex 28A	R/W
7.17.15:0	D31:D16	See 73.6	R/W
7.18.15:0	D47:D32	See 73.6	R/W

[a]R/W = Read/Write, RO = Read only

NOTE 1—Auto-Negotiation that supports a 48-bit Base Page uses registers 7.16, 7.17, and 7.18 for storing Base Page information; Auto-Negotiation that supports a 16-bit Base Page only uses register 7.16 for storing Base Page information.

NOTE 2—Clause 37 1000BASE-X Auto-Negotiation is controlled through Clause 22 registers.

45.2.7.7 AN LP Base Page ability register (7.19, 7.20, and 7.21)

All of the bits in the AN LP Base Page ability register are read only. A write to the AN LP Base Page ability register shall have no effect.

Register 7.19 is a copy of register 5, if present (see 28.2.4.1).

When registers 7.20 and 7.21 are used, the value of the registers 7.20 and 7.21 is latched when register 7.19 is read and reads of registers 7.20 and 7.21 return the latched value rather than the current value.

Bit 7.19.12 is reserved for Backplane Ethernet port types as they do not use Extended Next Pages.

Table 45–382—AN LP Base Page ability register bit definitions

Bit(s)	Name	Description	R/W[a]
7.19.15:0	D15:D0	See 28.2.1.2 and 73.6	RO
7.20.15:0	D31:D16	See 73.6	RO
7.21.15:0	D47:D32	See 73.6	RO

[a]RO = Read only

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NOTE—Auto-Negotiation that supports a 48-bit Base Page uses registers 7.19, 7.20, and 7.21 for storing LP Base Page information; Auto-Negotiation that supports a 16-bit Base Page only use register 7.19 for storing LP Base Page information.

45.2.7.8 AN XNP transmit register (7.22, 7.23, and 7.24)

If the BP AN ability bit (7.48.0) in the BP Ethernet status register is set to zero then Extended Next Pages are enabled by setting bit 7.0.13 to one and the AN XNP transmit register contains the Next Page link codeword to be transmitted as defined in 28.2.3.4.

If the BP AN ability bit (7.48.0) is set to one then Next Page transmission is always enabled and the register contains the AN LD Next Page link codeword of the BP Ethernet PHY as defined in 73.7.7.1. Even though Backplane Ethernet does not use Extended Next Pages XNP is still used in the register name.

On power-up or AN reset, this register shall contain the default value, which represents a Message Page with the message code set to Null Message. This value may be replaced by any valid Extended Next Page message code that the device intends to transmit.

A write to register 7.23 or 7.24 does not set mr_next_page_loaded. Only a write to register 7.22 sets mr_next_page_loaded true as described in 28.2.4.1.8. Therefore registers 7.23 and 7.24 register should be written before register 7.22.

Table 45–383—AN XNP transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
7.22.15	Next Page	See 28.2.3.4 and 73.7.7.1	R/W
7.22.14	Reserved	Value always 0	RO
7.22.13	Message Page	See 28.2.3.4 and 73.7.7.1	R/W
7.22.12	Acknowledge 2	See 28.2.3.4 and 73.7.7.1	R/W
7.22.11	Toggle	See 28.2.3.4 and 73.7.7.1	RO
7.22.10:0	Message/Unformatted Code Field	See 28.2.3.4 and 73.7.7.1	R/W
7.23.15:0	Unformatted Code Field 1	See 28.2.3.4 and 73.7.7.1	R/W
7.24.15:0	Unformatted Code Field 2	See 28.2.3.4 and 73.7.7.1	R/W

[a]R/W = Read/Write, RO = Read only

45.2.7.9 AN LP XNP ability register (7.25, 7.26, and 7.27)

AN LP XNP ability register (registers 7.25, 7.26, and 7.27) store link partner Extended Next Pages as shown in Table 45–384. All of the bits in the AN LP XNP ability register are read only. A write to the AN LP XNP ability register shall have no effect.

The value of registers 7.26 and 7.27 is latched when register 7.25 is read and reads of registers 7.26 and 7.27 return the latched value rather than the current value.

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NOTE—If this register is used to store multiple link partner Extended Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent link partner Extended Next Pages.

Table 45–384—AN LP XNP ability register bit definitions

Bit(s)	Name	Description	R/W[a]
7.25.15	Next Page	See 28.2.3.4 and 73.7.7.1	RO
7.25.14	Acknowledge	See 28.2.3.4 and 73.7.7.1	RO
7.25.13	Message Page	See 28.2.3.4 and 73.7.7.1	RO
7.25.12	Acknowledge 2	See 28.2.3.4 and 73.7.7.1	RO
7.25.11	Toggle	See 28.2.3.4 and 73.7.7.1	RO
7.25.10:0	Message/Unformatted Code Field	See 28.2.3.4 and 73.7.7.1	RO
7.26.15:0	Unformatted Code Field 1	See 28.2.3.4 and 73.7.7.1	RO
7.27.15:0	Unformatted Code Field 2	See 28.2.3.4 and 73.7.7.1	RO

[a]RO = Read only

45.2.7.10 MultiGBASE-T AN control 1 register (Register 7.32)

The assignment of bits in the MultiGBASE-T AN control 1 register is shown in Table 45–385. The default values for each bit of the MultiGBASE-T AN control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–385—MultiGBASE-T AN control 1 register

Bit(s)	Name	Description	R/W[a]
7.32.15	MASTER-SLAVE manual config enable	1=Enable MASTER-SLAVE manual configuration 0=Disable MASTER-SLAVE manual configuration Default value is 0	R/W
7.32.14	MASTER-SLAVE config value	1=Configure PHY as MASTER 0=Configure PHY as SLAVE Default value is 0	R/W
7.32.13	Port type	1=Multiport device 0=single-port device	R/W
7.32.12	10GBASE-T ability	1 = Advertise PHY as 10GBASE-T capable. 0 = Do not advertise the PHY as 10GBASE-T capable	R/W
7.32.11	40GBASE-T ability	1 = Advertise PHY as 40GBASE-T capable 0 = Do not advertise the PHY as 40GBASE-T capable	R/W
7.32.10	25GBASE-T ability	1 = Advertise PHY as 25GBASE-T capable 0 = Do not advertise the PHY as 25GBASE-T capable	R/W
7.32.9	25GBASE-T Fast retrain ability	1 = Advertise PHY as 25GBASE-T fast retrain capable 0 = Do not advertise PHY as 25GBASE-T fast retrain capable	R/W
7.32.8	5GBASE-T ability	1 = Advertise PHY as 5GBASE-T capable 0 = Do not advertise PHY as 5GBASE-T capable	R/W
7.32.7	2.5GBASE-T ability	1 = Advertise PHY as 2.5GBASE-T capable 0 = Do not advertise PHY as 2.5GBASE-T capable	R/W

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Table 45–385—MultiGBASE-T AN control 1 register *(continued)*

Bit(s)	Name	Description	R/W[a]
7.32.6	5GBASE-T Fast retrain ability	1 = Advertise PHY as 5GBASE-T fast retrain capable 0 = Do not advertise PHY as 5GBASE-T fast retrain capable	R/W
7.32.5	2.5GBASE-T Fast retrain ability	1 = Advertise PHY as 2.5GBASE-T fast retrain capable 0 = Do not advertise PHY as 2.5GBASE-T fast retrain capable	R/W
7.32.4	Reserved	Value always 0	RO
7.32.3	40GBASE-T Fast retrain ability	1 = Advertise PHY as 40GBASE-T fast retrain capable 0 = Do not advertise PHY as 40GBASE-T fast retrain capable	R/W
7.32.2	10GBASE-T LD PMA training reset request	1 = Local device requests that link partner reset PMA training PRBS every frame 0 = Local device requests that link partner run PMA training PRBS continuously NOTE—the periodic training sequence request functionality is deprecated. Link partners may ignore a value of one in this bit. It is recommended to always set this bit to zero.	R/W
7.32.1	10GBASE-T Fast retrain ability	1 = Advertise PHY as 10GBASE-T fast retrain capable 0 = Do not advertise PHY as 10GBASE-T fast retrain capable	R/W
7.32.0	10GBASE-T LD loop timing ability	1 = Advertise PHY as capable of 10GBASE-T loop timing 0 = Do not advertise PHY as capable of 10GBASE-T loop timing	R/W

[a]R/W = Read/Write, RO = Read only

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

45.2.7.10.1 MASTER-SLAVE manual config enable (7.32.15)

If bit 7.32.15 is set to one then MASTER-SLAVE config value bit 7.32.14 is used to determine if the PHY operates as MASTER or SLAVE. If bit 7.32.15 is set to zero the PHY shall use Auto-Negotiation to determine the selection of MASTER or SLAVE. This bit is a copy of 9.12, if present (see 40.5.1.1), and any write to either 7.32.15 or 9.12 is reflected in both. Additional information regarding the resolution and selection of MASTER-SLAVE and bit 7.32.15 is contained in 55.6.2. The default value for bit 7.32.15 is zero.

45.2.7.10.2 MASTER-SLAVE config value (7.32.14)

Bit 7.32.14 is used to select MASTER or SLAVE operation if MASTER-SLAVE manual config bit 7.32.15 is set to one. If bit 7.32.14 is set to one the PHY shall operate as MASTER. If bit 7.32.14 is set to zero the PHY shall operate as SLAVE. This bit is a copy of 9.11 (see 40.5.1.1), if present, and any write to either 7.32.14 or 9.11 is reflected in both. Additional information regarding the resolution and selection of MASTER-SLAVE and bit 7.32.14 is contained in 55.6.2. The default value for bit 7.32.14 is zero.

45.2.7.10.3 Port type (7.32.13)

Bit 7.32.13 is to be used to indicate the preference during Auto-Negotiation to operate as MASTER (multiport device) or as SLAVE (single-port device) if the MASTER-SLAVE manual configuration enable bit 7.32.15 is zero. If bit 7.32.13 is set to one a preference to operate as MASTER is indicated. If bit 7.32.13 is set to zero a preference to operate as SLAVE is indicated. This bit is a copy of 9.10 (see 40.5.1.1), if present, and any write to either 7.32.13 or 9.10 is reflected in both. Subclause 55.6.2 contains additional information regarding the resolution and selection of MASTER-SLAVE and this bit.

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45.2.7.10.4 10GBASE-T capability (7.32.12)

Bit 7.32.12 is to be used to select whether or not Auto-Negotiation advertises the ability to operate as a 10GBASE-T PHY. If bit 7.32.12 is set to one the PHY shall advertise 10GBASE-T PHY capability. If bit 7.32.12 is set to zero the PHY shall not advertise 10GBASE-T PHY capability.

45.2.7.10.5 40GBASE-T capability (7.32.11)

Bit 7.32.11 is used to select whether or not Auto-Negotiation advertises the ability to operate as a 40GBASE-T PHY. If bit 7.32.11 is set to one the PHY shall advertise 40GBASE-T PHY capability. If bit 7.32.11 is set to zero the PHY shall not advertise 40GBASE-T PHY capability.

45.2.7.10.6 25GBASE-T capability (7.32.10)

Bit 7.32.10 is used to select whether or not Auto-Negotiation advertises the ability to operate as a 25GBASE-T PHY. If bit 7.32.10 is set to one the PHY shall advertise 25GBASE-T PHY capability. If bit 7.32.10 is set to zero the PHY shall not advertise 25GBASE-T PHY capability.

45.2.7.10.7 25GBASE-T Fast retrain ability (7.32.9)

Bit 7.32.9 is used to select whether or not the 25GBASE-T PHY advertises the ability to support 25GBASE-T fast retrain. Fast retrain ability is exchanged during link training, see 113.4.2.5.10. If bit 7.32.9 is set to one, the PHY shall advertise fast retrain ability. If bit 7.32.9 is set to zero, the PHY shall not advertise fast retrain ability.

45.2.7.10.8 5GBASE-T capability (7.32.8)

Bit 7.32.8 is used to select whether or not Auto-Negotiation advertises the ability to operate as a 5GBASE-T PHY. If bit 7.32.8 is set to one the PHY shall advertise 5GBASE-T PHY capability. If bit 7.32.8 is set to zero the PHY shall not advertise 5GBASE-T PHY capability.

45.2.7.10.9 2.5GBASE-T capability (7.32.7)

Bit 7.32.7 is used to select whether or not Auto-Negotiation advertises the ability to operate as a 2.5GBASE-T PHY. If bit 7.32.7 is set to one the PHY shall advertise 2.5GBASE-T PHY capability. If bit 7.32.7 is set to zero the PHY shall not advertise 2.5GBASE-T PHY capability.

45.2.7.10.10 5GBASE-T Fast retrain ability (7.32.6)

Bit 7.32.6 is used to select whether or not the 5GBASE-T PHY advertises the ability to support 5GBASE-T fast retrain. Fast retrain ability is exchanged during link training, see 126.4.2.5.10. If bit 7.32.6 is set to one, the PHY shall advertise fast retrain ability. If bit 7.32.6 is set to zero, the PHY shall not advertise fast retrain ability.

45.2.7.10.11 2.5GBASE-T Fast retrain ability (7.32.5)

Bit 7.32.5 is used to select whether or not the 2.5GBASE-T PHY advertises the ability to support 2.5GBASE-T fast retrain. Fast retrain ability is exchanged during link training, see 126.4.2.5.10. If bit 7.32.5 is set to one, the PHY shall advertise fast retrain ability. If bit 7.32.5 is set to zero, the PHY shall not advertise fast retrain ability.

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45.2.7.10.12 40GBASE-T Fast retrain ability (7.32.3)

Bit 7.32.3 is used to select whether or not the 40GBASE-T PHY advertises the ability to support 40GBASE-T fast retrain. Fast retrain ability is exchanged during link training, see 113.4.2.5.10. If bit 7.32.3 is set to one, the PHY shall advertise fast retrain ability. If bit 7.32.3 is set to zero, the PHY shall not advertise fast retrain ability.

45.2.7.10.13 10GBASE-T LD PMA training reset request (7.32.2)

For 10GBASE-T, if bit 7.32.2 is set to one then the local device expects the link partner to reset the PMA training PRBS for every PMA training frame. If bit 7.32.2 is zero then the local device expects link partner to run PMA training PRBS continuously through every PMA training frame.

The periodic training sequence request functionality is deprecated and may be unsupported by some implementations. The link partner may ignore a request caused by setting this bit to one. It is recommended to always set this bit to zero.

45.2.7.10.14 10GBASE-T Fast retrain ability (7.32.1)

Bit 7.32.1 is used to select whether or not Auto-Negotiation advertises the ability to support 10GBASE-T fast retrain. If bit 7.32.1 is set to one, the PHY shall advertise fast retrain ability. If bit 7.32.1 is set to zero, the PHY shall not advertise fast retrain ability.

45.2.7.10.15 10GBASE-T LD loop timing ability (7.32.0)

Bit 7.32.0 is to be used to select whether or not Auto-Negotiation advertises the ability to perform loop timing. If bit 7.32.0 is set to one the PHY shall advertise loop timing capability. If bit 7.32.0 is set to zero the PHY shall not advertise loop timing capability.

45.2.7.11 MultiGBASE-T AN status 1 register (Register 7.33)

The assignment of bits in the MultiGBASE-T AN status 1 register is shown in Table 45–386. All the bits in the MultiGBASE-T AN status 1 register are read only; a write shall have no effect.

45.2.7.11.1 MASTER-SLAVE configuration fault (7.33.15)

MASTER-SLAVE configuration fault bit 7.33.15 shall be set in the event that determination of the MASTER-SLAVE cannot be successfully concluded. MASTER-SLAVE configuration fault, as well as the criteria and method of fault detection, is PHY specific. Additional information regarding the resolution and selection of MASTER-SLAVE and bit 7.33.15 for 10GBASE-T is contained in 55.6.2. Additional information regarding the resolution and selection of MASTER-SLAVE and bit 7.33.15 for 25GBASE-T and 40GBASE-T is contained in 113.6.2. Additional information regarding the resolution and selection of MASTER-SLAVE and bit 7.33.15 for 2.5GBASE-T and 5GBASE-T is contained in 126.6.2. The MASTER-SLAVE configuration fault bit 7.33.15 shall be cleared each time the MultiGBASE-T status register 7.33 is read via the management interface and shall be cleared by a PMA reset of a PHY in the MultiGBASE-T set. Bit 7.33.15 shall self clear upon Auto-Negotiation enable.

45.2.7.11.2 MASTER-SLAVE configuration resolution (7.33.14)

Bit 7.33.14 is determined by the MASTER-SLAVE configuration resolution function. These are described in 126.6.2, 55.6.2, and 113.6.2, for 2.5G/5GBASE-T, 10GBASE-T, and 25G/40GBASE-T, respectively. If the MASTER-SLAVE configuration resolution bit 7.33.14 is set to one and the Auto-Negotiation complete bit 7.1.5 is set and MASTER-SLAVE configuration fault bit 7.33.15 in the MultiGBASE-T status register is zero, then MASTER mode of operation has been selected. If the MASTER-SLAVE configuration resolution

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Table 45–386—MultiGBASE-T AN status 1 register

Bit(s)	Name	Description	R/W[a]
7.33.15	MASTER-SLAVE configuration fault	1 = MASTER-SLAVE configuration fault detected 0 = No MASTER-SLAVE configuration fault detected.	RO LH SC
7.33.14	MASTER-SLAVE configuration resolution	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	RO
7.33.13	Local receiver status	1 = Local receiver OK 0 = Local receiver not OK	RO
7.33.12	Remote receiver status	1 = Remote receiver OK 0 = Remote receiver not OK	RO
7.33.11	Link partner 10GBASE-T capability	1 = Link partner is able to operate as 10GBASE-T 0 = Link partner is not able to operate as 10GBASE-T This bit is guaranteed to be valid only when the Page received bit (7.1.6) has been set to one.	RO
7.33.10	LP loop timing ability	1 = Link partner is capable of loop timing 0 = Link partner is not capable of loop timing	RO
7.33.9	10GBASE-T LP PMA training reset request	1 = Link partner requests that local device reset PMA training PRBS every frame 0 = Link partner requests that local device run PMA training PRBS continuously See NOTE	RO
7.33.8	Link partner 40GBASE-T capability	1 = Link partner is able to operate as 40GBASE-T 0 = Link partner is not able to operate as 40GBASE-T	RO
7.33.7	Link partner 25GBASE-T capability	1 = Link partner is able to operate as 25GBASE-T 0 = Link partner is not able to operate as 25GBASE-T	RO
7.33.6	Link partner 5GBASE-T capability	1 = Link partner is able to operate as 5GBASE-T 0 = Link partner is not able to operate as 5GBASE-T	RO
7.33.5	Link partner 2.5GBASE-T capability	1 = Link partner is able to operate as 2.5GBASE-T 0 = Link partner is not able to operate as 2.5GBASE-T	RO
7.33.4	5GBASE-T Fast retrain ability	1 = Link partner is capable of 5GBASE-T fast retrain 0 = Link partner is not capable of 5GBASE-T fast retrain	RO
7.33.3	2.5GBASE-T Fast retrain ability	1 = Link partner is capable of 2.5GBASE-T fast retrain 0 = Link partner is not capable of 2.5GBASE-T fast retrain	RO
7.33.2	25GBASE-T Fast retrain ability	1 = Link partner is capable of 25GBASE-T fast retrain 0 = Link partner is not capable of 25GBASE-T fast retrain	RO
7.33.1	10GBASE-T Fast retrain ability	1 = Link partner is capable of 10GBASE-T fast retrain 0 = Link partner is not capable of 10GBASE-T fast retrain	RO
7.33.0	40GBASE-T Fast retrain ability	1 = Link partner is capable of 40GBASE-T fast retrain 0 = Link partner is not capable of 40GBASE-T fast retrain	RO
NOTE—The periodic training sequence request functionality is deprecated. Implementations may ignore a value of one in this bit or have it always read as zero.			

[a]RO = Read only, SC = Self-clearing, LH = Latching high

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bit 7.33.14 is set to zero and the Auto-Negotiation complete bit 7.1.5 is set and MASTER-SLAVE configuration fault bit 7.33.15 in the MultiGBASE-T status register is zero, then SLAVE mode of operation has been selected. In all other cases, neither SLAVE mode nor MASTER mode has been selected.

45.2.7.11.3 Local receiver status (7.33.13)

Local receiver status bit 7.33.13 shall be set if the local receiver status is OK as defined in 55.2.2.7. If the local receiver status bit 7.33.13 is zero, the local receiver status is not OK as defined in 55.2.2.7.

45.2.7.11.4 Remote receiver status (7.33.12)

Remote receiver status bit 7.33.12 shall be set if the remote receiver status is OK as defined in 55.2.2.8. If the remote receiver status bit 7.33.12 is zero, the remote receiver status is not OK as defined in 55.2.2.8.

45.2.7.11.5 Link partner 10GBASE-T capability (7.33.11)

The bit is only valid when page receive bit 7.1.6 in is set to one. When read as a one, bit 7.33.11 indicates that the link partner is able to operate as 10GBASE-T. When read as a zero, bit 7.33.11 indicates that the link partner is not able to operate as 10GBASE-T.

45.2.7.11.6 Link partner loop timing ability (7.33.10)

When read as a one, bit 7.33.10 indicates that the link partner has the ability to support loop timing as specified in 55.1.3. When read as a zero, bit 7.33.10 indicates that the link partner lacks the ability to support loop timing.

45.2.7.11.7 10GBASE-T Link partner PMA training reset request (7.33.9)

If bit 7.33.9 is set to one then the link partner is expecting the local device to reset the PMA training PRBS for every PMA training frame. If bit 7.33.9 is zero then the link partner expects the local device to run PMA training PRBS continuously through every PMA training frame. The periodic training sequence request functionality is deprecated. Implementations may ignore a value of one in this bit or have it always read as zero.

45.2.7.11.8 Link partner 40GBASE-T capability (7.33.8)

Bit 7.33.8 is only valid when page received bit 7.1.6 is set to one. When read as a one, bit 7.33.8 indicates that the link partner is able to operate as 40GBASE-T. When read as a zero, bit 7.33.8 indicates that the link partner is not able to operate as 40GBASE-T.

45.2.7.11.9 Link partner 25GBASE-T capability (7.33.7)

Bit 7.33.7 is only valid when page received bit 7.1.6 is set to one. When read as a one, bit 7.33.7 indicates that the link partner is able to operate as 25GBASE-T. When read as a zero, bit 7.33.7 indicates that the link partner is not able to operate as 25GBASE-T.

45.2.7.11.10 Link partner 5GBASE-T capability (7.33.6)

Bit 7.33.6 is only valid when page received bit 7.1.6 is set to one. When read as a one, bit 7.33.6 indicates that the link partner is able to operate as 5GBASE-T. When read as a zero, bit 7.33.6 indicates that the link partner is not able to operate as 5GBASE-T.

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45.2.7.11.11 Link partner 2.5GBASE-T capability (7.33.5)

Bit 7.33.5 is only valid when page received bit 7.1.5 is set to one. When read as a one, bit 7.33.5 indicates that the link partner is able to operate as 2.5GBASE-T. When read as a zero, bit 7.33.5 indicates that the link partner is not able to operate as 2.5GBASE-T.

45.2.7.11.12 5GBASE-T Fast retrain ability (7.33.4)

When read as a one, bit 7.33.4 indicates that the link partner has the ability to support the 5GBASE-T fast retrain capability as specified in 126.4.2.5.16. When read as a zero, bit 7.33.4 indicates that the PHY lacks the ability to support the 5GBASE-T fast retrain capability. This bit is only valid after link is established.

45.2.7.11.13 2.5GBASE-T Fast retrain ability (7.33.3)

When read as a one, bit 7.33.3 indicates that the link partner has the ability to support the 2.5GBASE-T fast retrain capability as specified in 126.4.2.5.16. When read as a zero, bit 7.33.3 indicates that the PHY lacks the ability to support the 2.5GBASE-T fast retrain capability. This bit is only valid after link is established.

45.2.7.11.14 25GBASE-T Fast retrain ability (7.33.2)

When read as a one, bit 7.33.2 indicates that the link partner has the ability to support the 25GBASE-T fast retrain capability as specified in 113.4.2.5.16. When read as a zero, bit 7.33.2 indicates that the PHY lacks the ability to support the 25GBASE-T fast retrain capability. This bit is valid only after link is established.

45.2.7.11.15 10GBASE-T Fast retrain ability (7.33.1)

When read as a one, bit 7.33.1 indicates that the link partner has the ability to support the 10GBASE-T fast retrain capability as specified in 55.4.2.5.15. When read as a zero, bit 7.33.1 indicates that the PHY lacks the ability to support the 10GBASE-T fast retrain capability.

45.2.7.11.9 40GBASE-T Fast retrain ability (7.33.0)

When read as a one, bit 7.33.0 indicates that the link partner has the ability to support the 40GBASE-T fast retrain capability as specified in 113.4.2.5.16. When read as a zero, bit 7.33.0 indicates that the PHY lacks the ability to support the 40GBASE-T fast retrain capability. This bit is valid only after link is established.

45.2.7.12 Backplane Ethernet, BASE-R copper status (Register 7.48)

The assignment of bits in the Backplane Ethernet, BASE-R copper status register is shown in Table 45–387.

Table 45–387—Backplane Ethernet, BASE-R copper status register (register 7.48) bit definitions

Bit(s)	Name	Description	R/W[a]
7.48.15	5GBASE-KR	1 = PMA/PMD is negotiated to perform 5GBASE-KR 0 = PMA/PMD is not negotiated to perform 5GBASE-KR	RO
7.48.14	2.5GBASE-KX	1 = PMA/PMD is negotiated to perform 2.5GGBASE-KX 0 = PMA/PMD is not negotiated to perform 2.5GGBASE-KX	RO

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Table 45–387—Backplane Ethernet, BASE-R copper status register (register 7.48) bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
7.48.13	25GBASE-KR or 25GBASE-CR	1 = PMA/PMD is negotiated to perform 25GBASE-KR or 25GBASE-CR 0 = PMA/PMD is not negotiated to perform 25GBASE-KR or 25GBASE-CR	RO
7.48.12	25GBASE-KR-S or 25GBASE-CR-S	1 = PMA/PMD is negotiated to perform 25GBASE-KR-S or 25GBASE-CR-S 0 = PMA/PMD is not negotiated to perform 25GBASE-KR-S or 25GBASE-CR-S	RO
7.48.11	100GBASE-CR4	1 = PMA/PMD is negotiated to perform 100GBASE-CR4 0 = PMA/PMD is not negotiated to perform 100GBASE-CR4	RO
7.48.10	100GBASE-KR4	1 = PMA/PMD is negotiated to perform 100GBASE-KR4 0 = PMA/PMD is not negotiated to perform 100GBASE-KR4	RO
7.48.9	100GBASE-KP4	1 = PMA/PMD is negotiated to perform 100GBASE-KP4 0 = PMA/PMD is not negotiated to perform 100GBASE-KP4	RO
7.48.8	100GBASE-CR10	1 = PMA/PMD is negotiated to perform 100GBASE-CR10 0 = PMA/PMD is not negotiated to perform 100GBASE-CR10	RO
7.48.7	RS-FEC negotiated	1 = PMA/PMD is negotiated to perform RS-FEC 0 = PMA/PMD is not negotiated to perform RS-FEC	RO
7.48.6	40GBASE-CR4	1 = PMA/PMD is negotiated to perform 40GBASE-CR4 0 = PMA/PMD is not negotiated to perform 40GBASE-CR4	RO
7.48.5	40GBASE-KR4	1 = PMA/PMD is negotiated to perform 40GBASE-KR4 0 = PMA/PMD is not negotiated to perform 40GBASE-KR4	RO
7.48.4	BASE-R FEC negotiated	1 = PMA/PMD is negotiated to perform BASE-R FEC 0 = PMA/PMD is not negotiated to perform BASE-R FEC	RO
7.48.3	10GBASE-KR	1 = PMA/PMD is negotiated to perform 10GBASE-KR 0 = PMA/PMD is not negotiated to perform 10GBASE-KR	RO
7.48.2	10GBASE-KX4	1 = PMA/PMD is negotiated to perform 10GBASE-KX4 or CX4 0 = PMA/PMD is not negotiated to perform 10GBASE-KX4/CX4	RO
7.48.1	1000BASE-KX	1 = PMA/PMD is negotiated to perform 1000BASE-KX 0 = PMA/PMD is not negotiated to perform 1000BASE-KX	RO
7.48.0	BP AN ability	If a Backplane, BASE-R copper PHY type is implemented, this bit is set to one	RO

[a]RO = Read only

45.2.7.12.1 BASE-R FEC negotiated (7.48.4)

When the Auto-Negotiation process has completed as indicated by the AN complete bit (7.1.5), bit 7.48.4 indicates that BASE-R FEC operation has been negotiated. This bit is set only if a BASE-R PHY supporting FEC operation has also been negotiated.

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45.2.7.12.2 RS-FEC negotiated (7.48.7)

When the Auto-Negotiation process has completed as indicated by the AN complete bit (7.1.5), bit 7.48.7 indicates that RS-FEC operation has been negotiated. This bit is set only if RS-FEC operation has been negotiated for a BASE-R PHY supporting negotiation of RS-FEC operation.

45.2.7.12.3 Negotiated Port Type (7.48.1, 7.48.2, 7.48.3, 7.48.5, 7.48.6, 7.48.8, 7.48.9, 7.48.10, 7.48.11, 7.48.12, 7.48.13, 7.48.14, 7.48.15, 7.49.0, 7.49.1, 7.49.2)

When the AN process has been completed as indicated by the AN complete bit, these bits in register 7.48 and register 7.49 indicate the negotiated port type. Only one of these bits is set depending on the priority resolution function. System developers need to distinguish between parallel detection of 10GBASE-KX4 and 10GBASE-CX4 based on the MDI and media type present.

45.2.7.12.4 Backplane Ethernet, BASE-R copper AN ability (7.48.0)

If a Backplane, BASE-R copper PHY type is implemented, this bit shall be set to one.

When read as a one, bit 7.48.0 indicates that the PMA/PMD has the ability to perform Backplane Ethernet, BASE-R copper AN. When read as a zero, bit 7.48.0 indicates that the PMA/PMD lacks the ability to perform Backplane Ethernet BASE-R copper AN.

45.2.7.13 Backplane Ethernet, BASE-R copper status 2 (Register 7.49)

The assignment of bits in the Backplane Ethernet, BASE-R copper status 2 register is shown in Table 45–388.

Table 45–388—Backplane Ethernet, BASE-R copper status 2 register (register 7.49) bit definitions

Bit(s)	Name	Description	RO[a]
7.49.15:3	Reserved	Value always 0	RO
7.49.2	200GBASE-KR4 or 200GBASE-CR4	1 = PMA/PMD is negotiated to perform 200GBASE-KR4 or 200GBASE-CR4 0 = PMA/PMD is not negotiated to perform 200GBASE-KR4 or 200GBASE-CR4	RO
7.49.1	100GBASE-KR2 or 100GBASE-CR2	1 = PMA/PMD is negotiated to perform 100GBASE-KR2 or 100GBASE-CR2 0 = PMA/PMD is not negotiated to perform 100GBASE-KR2 or 100GBASE-CR2	RO
7.49.0	50GBASE-KR or 50GBASE-CR	1 = PMA/PMD is negotiated to perform 50GBASE-KR or 50GBASE-CR 0 = PMA/PMD is not negotiated to perform 50GBASE-KR or 50GBASE-CR	RO

[a]RO = Read only

45.2.7.13.1 Negotiated Port Type

See 45.2.7.12.3.

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45.2.7.14 EEE advertisement 1 (Register 7.60)

This register defines the EEE advertisement for several device types. Devices that use Clause 28 Auto-Negotiation send EEE advertisement in the Unformatted Next Page following a EEE technology message code as defined in 28C.12 or as part of the 10GBASE-T and 1000BASE-T technology message code as defined in 28C.11. Devices that use Clause 73 Auto-Negotiation send EEE advertisement in the unformatted code field of Message Next Page with EEE technology message code as defined in 73A.4. 25GBASE-T and 40GBASE-T EEE advertisement is exchanged in the Infofield during training as defined in 113.4.2.5.10. For 2.5GBASE-T and 5GBASE-T, the EEE advertisement is exchanged in the Infofield during training as defined in 126.4.2.5.10. The assignment of bits in the EEE advertisement 1 register and the correspondence with the bits in the Next Page messages or in the training Infofield are shown in Table 45–389.

Bits 10:0 of register 7.60 map to bits U10 through U0 respectively of the Unformatted Next Page following a EEE technology message code as defined in 28C.12. Bits 15:0 of register 7.60 map to bits U15 through U0 respectively of the unformatted code field of Message Next Page with EEE technology message code as defined in 73A.4. Bits 3:1 of register 7.60 also map to bits U24 through U22 respectively of the 10GBASE-T and 1000BASE-T technology message code as defined in 28C.11. Devices using Clause 28 auto-negotiation may ignore bits defined for Clause 73 auto-negotiation, and devices using Clause 73 auto-negotiation may ignore bits defined for Clause 28 auto-negotiation.

Table 45–389—EEE advertisement register 1 (register 7.60) bit definitions

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W[a]
7.60.15	Reserved	Value always 0		RO
7.60.14	25GBASE-R EEE	1 = Advertise that the 25GBASE-R PHY has EEE deep sleep capability 0 = Do not advertise that the 25GBASE-R PHY has EEE deep sleep capability	73.7.7.1;U14	R/W
7.60.13	100GBASE-CR4 EEE	1 = Advertise that the 100GBASE-CR4 has EEE deep sleep capability 0 = Do not advertise that the 100GBASE-CR4 has EEE deep sleep capability	73.7.7.1; U13	R/W
7.60.12	100GBASE-KR4 EEE	1 = Advertise that the 100GBASE-KR4 has EEE deep sleep capability 0 = Do not advertise that the 100GBASE-KR4 has EEE deep sleep capability	73.7.7.1; U12	R/W
7.60.11	100GBASE-KP4 EEE	1 = Advertise that the 100GBASE-KP4 has EEE deep sleep capability 0 = Do not advertise that the 100GBASE-KP4 has EEE deep sleep capability	73.7.7.1; U11	R/W
7.60.10	100GBASE-CR10 EEE	1 = Advertise that the 100GBASE-CR10 has EEE deep sleep capability 0 = Do not advertise that the 100GBASE-CR10 has EEE deep sleep capability	73.7.7.1; U10	R/W

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Table 45–389—EEE advertisement register 1 (register 7.60) bit definitions *(continued)*

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W[a]
7.60.9	40GBASE-T EEE	1 = Advertise that the 40GBASE-T has EEE capability 0 = Do not advertise that the 40GBASE-T has EEE capability	113.4.2.5.10; Infofield Octet 12 bit 7	R/W
7.60.8	40GBASE-CR4 EEE	1 = Advertise that the 40GBASE-CR4 has EEE deep sleep capability 0 = Do not advertise that the 40GBASE-CR4 has EEE deep sleep capability	73.7.7.1; U8	R/W
7.60.7	40GBASE-KR4 EEE	1 = Advertise that the 40GBASE-KR4 has EEE deep sleep capability 0 = Do not advertise that the 40GBASE-KR4 has EEE deep sleep capability	73.7.7.1; U7	R/W
7.60.6	10GBASE-KR EEE	1 = Advertise that the 10GBASE-KR has EEE capability 0 = Do not advertise that the 10GBASE-KR has EEE capability	73.7.7.1; U6	R/W
7.60.5	10GBASE-KX4 EEE	1 = Advertise that the 10GBASE-KX4 has EEE capability 0 = Do not advertise that the 10GBASE-KX4 has EEE capability	73.7.7.1; U5	R/W
7.60.4	1000BASE-KX EEE	1 = Advertise that the 1000BASE-KX has EEE capability 0 = Do not advertise that the 1000BASE-KX has EEE capability	73.7.7.1; U4	R/W
7.60.3	10GBASE-T EEE	1 = Advertise that the 10GBASE-T has EEE capability 0 = Do not advertise that the 10GBASE-T has EEE capability	28.2.3.4.1; U3 / 28.2.3.4.2; U24	R/W
7.60.2	1000BASE-T EEE	1 = Advertise that the 1000BASE-T has EEE capability 0 = Do not advertise that the 1000BASE-T has EEE capability	28.2.3.4.1; U2 / 28.2.3.4.2; U23	R/W
7.60.1	100BASE-TX EEE	1 = Advertise that the 100BASE-TX has EEE capability 0 = Do not advertise that the 100BASE-TX has EEE capability	28.2.3.4.1; U1 / 28.2.3.4.2; U22	R/W
7.60.0	25GBASE-T EEE	1 = Advertise that the 25GBASE-T has EEE capability 0 = Do not advertise that the 25GBASE-T has EEE capability	113.4.2.5.10; Infofield Octet 12 bit 7	R/W

[a]R/W = Read/Write, RO = Read only

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45.2.7.14.1 25GBASE-R EEE supported (7.60.14)

If set to a one, bit 7.60.14 indicates that the technologies advertised in bits A9 and A10 of Table 73–4 are capable of supporting EEE deep sleep operation. If set to a zero, EEE deep sleep operation is not supported for 25GBASE-R.

45.2.7.14.2 100GBASE-CR4 EEE supported (7.60.13)

Support for EEE deep sleep operation for 100GBASE-CR4, as defined in 92.1, shall be advertised if this bit is set to one. Support for EEE deep sleep operation should only be advertised if it is supported on all sublayers of the PHY as well as physical instantiations of the PMA service interface as appropriate.

45.2.7.14.3 100GBASE-KR4 EEE supported (7.60.12)

Support for EEE deep sleep operation for 100GBASE-KR4, as defined in 93.1, shall be advertised if this bit is set to one. Support for EEE deep sleep operation should only be advertised if it is supported on all sublayers of the PHY as well as physical instantiations of the PMA service interface as appropriate.

45.2.7.14.4 100GBASE-KP4 EEE supported (7.60.11)

Support for EEE deep sleep operation for 100GBASE-KP4, as defined in 94.1, shall be advertised if this bit is set to one. Support for EEE deep sleep operation should only be advertised if it is supported on all sublayers of the PHY as well as physical instantiations of the PMA service interface as appropriate.

45.2.7.14.5 100GBASE-CR10 EEE supported (7.60.10)

Support for EEE deep sleep operation for 100GBASE-CR10, as defined in 85.1, shall be advertised if this bit is set to one. Support for EEE deep sleep operation should only be advertised if it is supported on all sublayers of the PHY as well as physical instantiations of the PMA service interface as appropriate.

45.2.7.14.6 40GBASE-T EEE supported (7.60.9)

If the device supports EEE operation for 40GBASE-T as defined in 113.1.3.3, and EEE operation is desired, this bit shall be set to one.

45.2.7.14.7 40GBASE-CR4 EEE supported (7.60.8)

Support for EEE deep sleep operation for 40GBASE-CR4, as defined in 85.1, shall be advertised if this bit is set to one. Support for EEE deep sleep operation should only be advertised if it is supported on all sublayers of the PHY as well as physical instantiations of the PMA service interface as appropriate.

45.2.7.14.8 40GBASE-KR4 EEE supported (7.60.7)

Support for EEE deep sleep operation for 40GBASE-KR4, as defined in 84.1, shall be advertised if this bit is set to one. Support for EEE deep sleep operation should only be advertised if it is supported on all sublayers of the PHY as well as physical instantiations of the PMA service interface as appropriate.

45.2.7.14.9 10GBASE-KR EEE supported (7.60.6)

If the device supports EEE operation for 10GBASE-KR as defined in 72.1, and EEE operation is desired, this bit shall be set to one.

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45.2.7.14.10 10GBASE-KX4 EEE supported (7.60.5)

If the device supports EEE operation for 10GBASE-KX4 as defined in 71.2, and EEE operation is desired, this bit shall be set to one.

45.2.7.14.11 1000BASE-KX EEE supported (7.60.4)

If the device supports EEE operation for 1000BASE-KX as defined in 70.1, and EEE operation is desired, this bit shall be set to one.

45.2.7.14.12 10GBASE-T EEE supported (7.60.3)

If the device supports EEE operation for 10GBASE-T as defined in 55.1.3.3, and EEE operation is desired, this bit shall be set to one.

45.2.7.14.13 1000BASE-T EEE supported (7.60.2)

If the device supports EEE operation for 1000BASE-T as defined in 40.2.11, and EEE operation is desired, this bit shall be set to one.

45.2.7.14.14 100BASE-TX EEE supported (7.60.1)

If the device supports EEE operation for 100BASE-TX as defined in 25.5, and EEE operation is desired, this bit shall be set to one.

45.2.7.14.15 25GBASE-T EEE supported (7.60.0)

If the device supports EEE operation for 25GBASE-T as defined in 113.1.3.3, and EEE operation is desired, this bit shall be set to one.

45.2.7.15 EEE link partner ability 1 (Register 7.61)

All of the bits in the EEE LP ability 1 register are read-only. A write to the EEE LP ability 1 register shall have no effect. Except for 10GBASE-T, members of the MultiGBASE-T PHY set exchange the EEE ability in the Infofield during link training. For these PHYs, the EEE LP ability register is updated after link is established. For all other PHYs, when the AN process has been completed, this register shall reflect the contents of the link partner's EEE advertisement 1 register. The assignment of bits in the EEE link partner ability 1 register and the correspondence with the bits in the Next Page messages are shown in Table 45–390.

Table 45–390—EEE link partner ability 1 (register 7.61) bit definitions

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W[a]
7.61.15	Reserved	Value always 0		RO
7.61:14	25GBASE-R EEE	1 = Link partner is advertising EEE deep sleep capability for 25GBASE-R 0 = Link partner is not advertising EEE deep sleep capability for 25GBASE-R	73.7.7.1;U14	RO

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Table 45–390—EEE link partner ability 1 (register 7.61) bit definitions *(continued)*

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W[a]
7.61.13	100GBASE-CR4 EEE	1 = Link partner is advertising EEE deep sleep capability for 100GBASE-CR4 0 = Link partner is not advertising EEE deep sleep capability for 100GBASE-CR4	73.7.7.1; U13	RO
7.61.12	100GBASE-KR4 EEE	1 = Link partner is advertising EEE deep sleep capability for 100GBASE-KR4 0 = Link partner is not advertising EEE deep sleep capability for 100GBASE-KR4	73.7.7.1; U12	RO
7.61.11	100GBASE-KP4 EEE	1 = Link partner is advertising EEE deep sleep capability for 100GBASE-KP4 0 = Link partner is not advertising EEE deep sleep capability for 100GBASE-KP4	73.7.7.1; U11	RO
7.61.10	100GBASE-CR10 EEE	1 = Link partner is advertising EEE deep sleep capability for 100GBASE-CR10 0 = Link partner is not advertising EEE deep sleep capability for 100GBASE-CR10	73.7.7.1; U10	RO
7.61.9	40GBASE-T EEE	1 = Link partner is advertising EEE capability for 40GBASE-T 0 = Link partner is not advertising EEE capability for 40GBASE-T	113.4.2.5.10; Infofield Octet 12 bit 7	RO
7.61.8	40GBASE-CR4 EEE	1 = Link partner is advertising EEE deep sleep capability for 40GBASE-CR4 0 = Link partner is not advertising EEE deep sleep capability for 40GBASE-CR4	73.7.7.1; U8	RO
7.61.7	40GBASE-KR4 EEE	1 = Link partner is advertising EEE deep sleep capability for 40GBASE-KR4 0 = Link partner is not advertising EEE deep sleep capability for 40GBASE-KR4	73.7.7.1; U7	RO
7.61.6	10GBASE-KR EEE	1 = Link partner is advertising EEE capability for 10GBASE-KR 0 = Link partner is not advertising EEE capability for 10GBASE-KR	73.7.7.1; U6	RO
7.61.5	10GBASE-KX4 EEE	1 = Link partner is advertising EEE capability for 10GBASE-KX4 0 = Link partner is not advertising EEE capability for 10GBASE-KX4	73.7.7.1; U5	RO
7.61.4	1000BASE-KX EEE	1 = Link partner is advertising EEE capability for 1000BASE-KX 0 = Link partner is not advertising EEE capability for 1000BASE-KX	73.7.7.1; U4	RO
7.61.3	10GBASE-T EEE	1 = Link partner is advertising EEE capability for 10GBASE-T 0 = Link partner is not advertising EEE capability for 10GBASE-T	28.2.3.4.1; U3 / 55.6.1; U24	RO

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Table 45–390—EEE link partner ability 1 (register 7.61) bit definitions *(continued)*

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W[a]
7.61.2	1000BASE-T EEE	1 = Link partner is advertising EEE capability for 1000BASE-T 0 = Link partner is not advertising EEE capability for 1000BASE-T	28.2.3.4.1; U2 / 55.6.1; U23	RO
7.61.1	100BASE-TX EEE	1 = Link partner is advertising EEE capability for 100BASE-TX 0 = Link partner is not advertising EEE capability for 100BASE-TX	28.2.3.4.1; U1 / 55.6.1; U22	RO
7.61.0	25GBASE-T EEE	1 = Link partner is advertising EEE capability for 25GBASE-T 0 = Link partner is not advertising EEE capability for 25GBASE-T	113.4.2.5.10; Infofield Octet 12 bit 7	RO

[a]RO = Read only

The definitions for the contents of the EEE LP ability register are given by the definitions for the contents on the link partner's EEE advertisement 1 register, 7.60 (see 45.2.7.14).

45.2.7.16 EEE advertisement 2 (Register 7.62)

EEE advertisement 2 register is a continuation of EEE advertisement 1 register. The assignment of bits in the EEE advertisement 2 register are shown in Table 45–391.

Table 45–391—EEE advertisement 2 register (register 7.62) bit definitions

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W[a]
7.62.15:4	Reserved	Value always 0		RO
7.62.3	5GBASE-KR EEE	1 = Advertise that the 5GBASE-KR has EEE capability 0 = Do not advertise that the 5GBASE-KR has EEE capability	73.7.7.1; U17	R/W
7.62.2	2.5GBASE-KX EEE	1 = Advertise that the 2.5GBASE-KX has EEE capability 0 = Do not advertise that the 2.5GBASE-KX has EEE capability	73.7.7.1; U16	R/W
7.62.1	5GBASE-T EEE	1 = Advertise that the 5GBASE-T has EEE capability 0 = Do not advertise that the 5GBASE-T has EEE capability	126.4.2.5.10	R/W
7.62.0	2.5GBASE-T EEE	1 = Advertise that the 2.5GBASE-T has EEE capability 0 = Do not advertise that the 2.5GBASE-T has EEE capability	126.4.2.5.10	R/W

[a]R/W = Read/Write, RO = Read only

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45.2.7.16.1 5GBASE-KR EEE (7.62.3)

If the device supports EEE operation for 5GBASE-KR as defined in 130.1 and EEE operation is desired, this bit shall be set to one.

45.2.7.16.2 2.5GBASE-KX EEE (7.62.2)

If the device supports EEE operation for 2.5GBASE-KX as defined in 128.1 and EEE operation is desired, this bit shall be set to one.

45.2.7.16.3 5GBASE-T EEE (7.62.1)

If the device supports EEE operation for 5GBASE-T as defined in 126.6.1, and EEE operation is desired, bit 7.62.1 shall be set to one.

45.2.7.16.4 2.5GBASE-T EEE (7.62.0)

If the device supports EEE operation for 2.5GBASE-T as defined in 126.6.1, and EEE operation is desired, bit 7.62.0 shall be set to one.

45.2.7.17 EEE link partner ability 2 (Register 7.63)

All of the bits in the EEE link partner ability 2 register are read-only. A write to the EEE link partner ability 2 register shall have no effect. When the AN and training processes have been completed, this register shall reflect the contents of the link partner's EEE advertisement 2 register. The assignment of bits in the EEE link partner ability 2 register and the correspondence with the bits in the Next Page messages (for PHYs that exchange EEE abilities during Auto-Negotiation) are shown in Table 45–392.

The definitions for the contents of the EEE link partner ability 2 register are given by the definitions for the contents on the link partner's EEE advertisement 2 register, 7.62 (see 45.2.7.16).

Table 45–392—EEE link partner ability 2 (register 7.63) bit definitions

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W[a]
7.63.15:4	Reserved	Value always 0		RO
7.63.3	5GBASE-KR EEE	1 = Link partner is advertising that the 5GBASE-KR has EEE capability 0 = Link partner is not advertising that the 5GBASE-KR has EEE capability	73.7.7.1; U17	RO
7.63.2	2.5GBASE-KX EEE	1 = Link partner is advertising that the 2.5GBASE-KX has EEE capability 0 = Link partner is not advertising that the 2.5GBASE-KX has EEE capability	73.7.7.1; U16	RO

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Table 45–392—EEE link partner ability 2 (register 7.63) bit definitions *(continued)*

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W[a]
7.63.1	5GBASE-T EEE	1 = Link partner is advertising that the 5GBASE-T has EEE capability 0 = Link partner is not advertising that the 5GBASE-T has EEE capability	126.4.2.5.10	RO
7.63.0	2.5GBASE-T EEE	1 = Link partner is advertising that the 2.5GBASE-T has EEE capability 0 = Link partner is not advertising that the 2.5GBASE-T has EEE capability	126.4.2.5.10	RO

[a]RO = Read only

45.2.7.18 MultiGBASE-T AN control 2 (Register 7.64)

Register 7.64 is a continuation of register 7.32. The assignment of bits in the MultiGBASE-T AN control 2 register is shown in Table 45–393. The default values of each bit of the MultiGBASE-T AN control 2 register should be chosen so that the initial state of the devices upon power up or reset is a normal operational state without management intervention.

Table 45–393—MultiGBASE-T AN control 2 (register 7.64) bit definitions

Bit(s)	Name	Description	R/W[a]
7.64.15:4	Reserved	Value always 0	RO
7.64.3	2.5GBASE-T THP Bypass Request	1 = Local device requests link partner to initially reset THP during fast retrain 0= Local device requests link partner not to initially reset THP during fast retrain	R/W
7.64.2	5GBASE-T THP Bypass Request	1 = Local device requests link partner to initially reset THP during fast retrain 0= Local device requests link partner not to initially reset THP during fast retrain	R/W
7.64.1	25GBASE-T THP Bypass Request	1 = Local device requests link partner to initially reset THP during fast retrain 0 = Local device requests link partner not to initially reset THP during fast retrain	R/W
7.64.0	40GBASE-T THP Bypass Request	1 = Local device requests link partner to initially reset THP during fast retrain 0 = Local device requests link partner not to initially reset THP during fast retrain	R/W

[a]R/W = Read/Write, RO = Read only

45.2.7.18.1 2.5GBASE-T THP Bypass Request

Bit 7.64.3 is valid only if 7.32.5 is set to one advertising fast retrain ability, and is used to request the link partner whether to initially reset the THP during fast retrain. THP Bypass Request is exchanged during link training, see 126.4.2.5.10. If bit 7.64.3 is set to zero the local device requests link partner not to reset THP

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during fast retrain. If bit 7.64.3 is set to one the local device requests link partner to initially reset THP during fast retrain.

45.2.7.18.2 5GBASE-T THP Bypass Request

Bit 7.64.2 is valid only if 7.32.6 is set to one advertising fast retrain ability, and is used to request the link partner whether to initially reset the THP during fast retrain. THP Bypass Request is exchanged during link training, see 126.4.2.5.10. If bit 7.64.2 is set to zero the local device requests link partner not to reset THP during fast retrain. If bit 7.64.2 is set to one the local device requests link partner to initially reset THP during fast retrain.

45.2.7.18.3 25GBASE-T THP Bypass Request

Bit 7.64.1 is valid only if 7.32.9 is set to one advertising fast retrain ability, and is used to request the link partner whether to initially reset the THP during fast retrain. THP Bypass Request is exchanged during link training, see 113.4.2.5.10. If bit 7.64.1 is set to zero the local device requests link partner not to reset THP during fast retrain. If bit 7.64.1 is set to one the local device requests link partner to initially reset THP during fast retrain.

45.2.7.18.4 40GBASE-T THP Bypass Request

Bit 7.64.0 is valid only if 7.32.3 is set to one advertising fast retrain ability, and is used to request the link partner whether to initially reset the THP during fast retrain. THP Bypass Request is exchanged during link training, see 113.4.2.5.10. If bit 7.64.0 is set to zero the local device requests link partner not to reset THP during fast retrain. If bit 7.64.0 is set to one the local device requests link partner to initially reset THP during fast retrain.

45.2.7.19 MultiGBASE-T AN status 2 (Register 7.65)

Register 7.65 is a continuation of register 7.33. The assignment of bits in the MultiGBASE-T AN status 2 register is shown in Table 45–394. All the bits in the MultiGBASE-T AN status 2 register are read only; a write shall have no effect.

Table 45–394—MultiGBASE-T AN status 2 (register 7.65) bit definitions

Bit(s)	Name	Description	R/W[a]
7.65.15:4	Reserved	Value always 0	RO
7.65.3	2.5GBASE-T Link Partner THP Bypass Request	1 = Link partner requests local device to initially reset THP during fast retrain 0= Link partner requests local device not to initially reset THP during fast retrain	RO
7.65.2	5GBASE-T Link Partner THP Bypass Request	1 = Link partner requests local device to initially reset THP during fast retrain 0= Link partner requests local device not to initially reset THP during fast retrain	RO

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Table 45–394—MultiGBASE-T AN status 2 (register 7.65) bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
7.65.1	25GBASE-T Link Partner THP Bypass Request	1 = Link partner requests local device to initially reset THP during fast retrain 0 = Link partner requests local device not to initially reset THP during fast retrain	RO
7.65.0	40GBASE-T Link Partner THP Bypass Request	1 = Link partner requests local device to initially reset THP during fast retrain 0 = Link partner requests local device not to initially reset THP during fast retrain	RO

[a]RO = Read only

45.2.7.19.1 2.5GBASE-T Link Partner THP Bypass Request

Bit 7.65.3 is valid only if 7.33.3 is set to one indicating that the link partner has fast retrain ability. THP Bypass Request is exchanged during link training, see 126.4.2.5.10. Bit 7.65.3 is updated after link is established. When read as a zero, the link partner requests local device not to reset THP during fast retrain. When read as a one, the link partner requests local device to initially reset THP during fast retrain.

45.2.7.19.2 5GBASE-T Link Partner THP Bypass Request

Bit 7.65.2 is valid only if 7.33.0 is set to one indicating that the link partner has fast retrain ability. THP Bypass Request is exchanged during link training, see 126.4.2.5.10. Bit 7.65.2 is updated after link is established. When read as a zero, the link partner requests local device not to reset THP during fast retrain. When read as a one, the link partner requests local device to initially reset THP during fast retrain.

45.2.7.19.3 25GBASE-T Link Partner THP Bypass Request

Bit 7.65.1 is valid only if 7.33.2 is set to one indicating that the link partner has fast retrain ability. THP Bypass Request is exchanged during link training, see 113.4.2.5.10. Bit 7.65.1 is updated after link is established. When read as a zero, the link partner requests local device not to reset THP during fast retrain. When read as a one, the link partner requests local device to initially reset THP during fast retrain.

45.2.7.19.4 40GBASE-T Link Partner THP Bypass Request

Bit 7.65.0 is valid only if 7.33.0 is set to one indicating that the link partner has fast retrain ability. THP Bypass Request is exchanged during link training, see 113.4.2.5.10. Bit 7.65.0 is updated after link is established. When read as a zero, the link partner requests local device not to reset THP during fast retrain. When read as a one, the link partner requests local device to initially reset THP during fast retrain.

45.2.7.20 BASE-T1 AN control register (Register 7.512)

The assignment of bits in the BASE-T1 AN control register is shown in Table 45–395. The default value for each bit of the BASE-T1 AN control register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

45.2.7.20.1 AN reset (7.512.15)

Resetting AN is accomplished by setting bit 7.512.15 to a one. This action shall set all BASE-T1 AN registers to their default states. As a consequence, this action may change the internal state of AN and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the

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Table 45–395—BASE-T1 AN control register bit definitions

Bit(s)	Name	Description	R/W[a]
7.512.15	AN reset	1 = AN reset 0 = AN normal operation	R/W, SC
7.512.14:13	Reserved	Value always 0	RO
7.512.12	Auto-Negotiation enable	1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	R/W
7.512.11:10	Reserved	Value always 0	RO
7.512.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation process 0 = Auto-Negotiation in process, disabled, or not supported	R/W, SC
7.512.8:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

same package. This bit is self-clearing, and AN shall return a value of one in bit 7.512.15 when a reset is in progress and a value of zero otherwise. AN is not required to accept a write transaction to any of its registers until the reset process is complete. The reset process shall be completed within 0.5 s from the setting of bit 7.512.15. During an AN reset, AN shall respond to reads from register bit 7.512.15. All other register bits shall be ignored.

The default value for bit 7.512.15 is zero.

NOTE—This operation may interrupt data communication.

45.2.7.20.2 Auto-Negotiation enable (7.512.12)

The Auto-Negotiation function shall be enabled by setting bit 7.512.12 to a one. If bit 7.512.12 is set to one, then type selection bits 1.2100.3:0 and MASTER-SLAVE bits 1.2100.14 shall have no effect on the link configuration, and the Auto-Negotiation process determines the link configuration. If bit 7.512.12 is cleared to zero, then bits 1.2100.3:0 and bit 1.2100.14 determine the link configuration regardless of the prior state of the link configuration and the Auto-Negotiation process.

If the BASE-T1 PHY reports via bit 7.513.3 that it lacks the ability to perform Auto-Negotiation, then the value of bit 7.512.12 shall be zero.

45.2.7.20.3 Restart Auto-Negotiation (7.512.9)

If the BASE-T1 PMA/PMD reports (via bit 7.513.3) that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the BASE-T1 PMA/PMD shall return a value of zero in bit 7.512.9 and any attempt to write a one to bit 7.512.9 shall be ignored.

Otherwise, the Auto-Negotiation process shall be restarted by setting bit 7.512.9 to one. This bit is self-clearing, and the BASE-T1 PMA/PMD shall return a value of one in bit 7.512.9 until the Auto-Negotiation process has been initiated. If Auto-Negotiation was completed prior to this bit being set, the process shall be reinitialized. The Auto-Negotiation process shall not be affected by clearing this bit to zero.

The default value for 7.512.9 is zero.

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45.2.7.21 BASE-T1 AN status (Register 7.513)

The assignment of bits in the BASE-T1 AN status register is shown in Table 45–396. All the bits in the BASE-T1 AN status register are read only; therefore, a write to the BASE-T1 AN status register shall have no effect.

Table 45–396—BASE-T1 AN status register bit definitions

Bit(s)	Name	Description	R/W[a]
7.513.15:7	Reserved	Value always 0	RO
7.513.6	Page received	1 = A page has been received 0 = A page has not been received	RO, LH
7.513.5	Auto-Negotiation complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
7.513.4	Remote fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO, LH
7.513.3	Auto-Negotiation ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
7.513.2	Link status	1 = Link is up 0 = Link is down	RO, LL
7.513.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching High, LL = Latching Low

45.2.7.21.1 Page received (7.513.6)

The Page received bit (7.513.6) shall be set to one to indicate that a new link codeword has been received and stored in the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 or the BASE-T1 AN LP Next Page ability registers 7.523 to 7.525. The contents of the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 are valid when bit 7.513.6 is set the first time during the Auto-Negotiation. The Page received bit shall be reset to zero on a read of the BASE-T1 AN status register (register 7.513).

45.2.7.21.2 Auto-Negotiation complete (7.513.5)

When read as a one, bit 7.513.5 indicates that the Auto-Negotiation process has been completed, and that the contents of the Auto-Negotiation registers 7.514 to 7.516 and 7.517 to 7.519 are valid. When read as a zero, bit 7.513.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of 7.517 through 7.525 registers are as defined by the current state of the Auto-Negotiation protocol, or as written for manual configuration. The BASE-T1 PMA/PMD shall return a value of zero in bit 7.513.5 if Auto-Negotiation is disabled by clearing bit 7.512.12. The BASE-T1 PMA/PMD shall also return a value of zero in bit 7.513.5 if it lacks the ability to perform Auto-Negotiation.

45.2.7.21.3 Remote fault (7.513.4)

When read as one, bit 7.513.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is AN specific. The remote fault bit shall be implemented with a latching function, such that the occurrence of a remote fault causes the bit 7.513.4 to become set and

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remain set until it is cleared. Bit 7.513.4 shall be cleared each time register 7.513 is read via the management interface, and shall also be cleared by a AN reset.

45.2.7.21.4 Auto-Negotiation ability (7.513.3)

When read as a one, bit 7.513.3 indicates that the BASE-T1 PMA/PMD has the ability to perform BASE-T1 Auto-Negotiation. When read as a zero, bit 7.513.3 indicates that the BASE-T1 PMA/PMD lacks the ability to perform BASE-T1 Auto-Negotiation.

45.2.7.21.5 Link status (7.513.2)

When read as a one, bit 7.513.2 indicates that the BASE-T1 PMA/PMD has determined that a valid link has been established. When read as a zero, bit 7.513.2 indicates that the link has been invalid after this bit was last read. Bit 7.513.2 is set to one when the variable link_status equals OK and is cleared to zero when the variable link_status equals FAIL. The link status bit shall be implemented with a latching function, such that the occurrence of a link_status equals FAIL condition causes the link status bit to become cleared and remain cleared until it is read via the management interface. Bit 7.513.2 shall be cleared upon AN reset. This status indication is intended to support the management attribute defined in 30.5.1.1.4, aMediaAvailable.

45.2.7.22 BASE-T1 AN advertisement register (Registers 7.514, 7.515, and 7.516)

The assignment of bits in the BASE-T1 AN advertisement register is shown in Table 45–397.

The Selector field (7.514.4:0) shall be set to the IEEE 802.3 code as specified in Annex 98A. The Acknowledge bit (7.514.14) is set to zero.

The technology ability field, as defined in 98.2.1.2, represents the technologies supported by the local device. Only bits representing supported technologies may be set. Management may clear bits in the technology ability field and restart Auto-Negotiation to negotiate an alternate common mode.

The management entity initiates renegotiation with the link partner using alternate abilities by setting the Restart Auto-Negotiation bit (7.512.9) in the AN control register to one.

Any writes to this register prior to completion of Auto-Negotiation, as indicated by bit 7.513.5, should be followed by a renegotiation for the new values to take effect. Once Auto-Negotiation has completed, software may examine this register along with the LP Base Page ability register to determine the highest common denominator technology.

The Base Page value is transferred to mr_adv_ability when register 7.514 is written. Therefore, registers 7.515 and 7.516 should be written before 7.514.

Table 45–397—BASE-T1 AN advertisement register bit definitions

Bit(s)	Name	Description	R/W[a]
7.514.15	Next Page	See 98.2.1.2.9	R/W
7.514.14	Acknowledge	Value always 0	RO
7.514.13	Remote fault	See 98.2.1.2.7	R/W
7.514.12:5	D12:D5	See 98.2.1.2	R/W

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Table 45–397—BASE-T1 AN advertisement register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
7.514.4:0	Selector field	See Annex 98A	R/W
7.515.15:0	D31:D16	See 98.2.1.2	R/W
7.516.15:0	D47:D32	See 98.2.1.2	R/W

[a]RO = Read only, R/W = Read/Write

45.2.7.23 BASE-T1 AN LP Base Page ability register (Registers 7.517, 7.518, and 7.519)

The assignment of bits in the BASE-T1 AN LP Base Page ability register is shown in Table 45–398.

All of the bits in the BASE-T1 AN LP Base Page ability register are read only. A write to the BASE-T1 AN LP Base Page ability register shall have no effect.

The value of the registers 7.518 and 7.519 is latched when register 7.517 is read and reads of registers 7.518 and 7.519 return the latched value rather than the current value.

Table 45–398—BASE-T1 AN LP Base Page ability register bit definitions

Bit(s)	Name	Description	R/W[a]
7.517.15:0	D15:D0	See 98.2.1.2	RO
7.518.15:0	D31:D16	See 98.2.1.2	RO
7.519.15:0	D47:D32	See 98.2.1.2	RO

[a]RO = Read only

45.2.7.24 BASE-T1 AN Next Page transmit register (Registers 7.520, 7.521, and 7.522)

The assignment of bits in the BASE-T1 AN Next Page transmit register is shown in Table 45–399.

The register contains the BASE-T1 AN Next Page link codeword as defined in 98.2.4.3.

On power-up or AN reset, this register shall contain the default value, which represents a Message Page with the message code set to Null Message. This value may be replaced by any valid Next Page Message Code that the device intends to transmit. The BASE-T1 AN shall use Next Page Message Codes as defined in Annex 98C.

A write to register 7.521 or 7.522 does not set mr_next_page_loaded. Only a write to register 7.520 sets mr_next_page_loaded true as described in 98.5.1. Therefore registers 7.521 and 7.522 should be written before register 7.520.

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Table 45–399—BASE-T1 AN Next Page transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
7.520.15	Next page	See 98.2.4.3	R/W
7.520.14	Reserved	Value always 0	RO
7.520.13	Message page	See 98.2.4.3	R/W
7.520.12	Acknowledge 2	See 98.2.4.3	R/W
7.520.11	Toggle	See 98.2.4.3	RO
7.520.10:0	Message/Unformatted code field	See 98.2.4.3	R/W
7.521.15:0	Unformatted code field 1	See 98.2.4.3	R/W
7.522.15:0	Unformatted code field 2	See 98.2.4.3	R/W

[a]RO = Read only, R/W = Read/Write

45.2.7.25 BASE-T1 AN LP Next Page ability register (Registers 7.523, 7.524, and 7.525)

BASE-T1 AN LP Next Page ability register (registers 7.523, 7.524, and 7.525) store BASE-T1 link partner Next Pages as shown in Table 45–400. All of the bits in the BASE-T1 AN LP Next Page ability register are read only. A write to the BASE-T1 AN LP Next Page ability register shall have no effect.

Table 45–400—BASE-T1 AN LP Next Page ability register bit definitions

Bit(s)	Name	Description	R/W[a]
7.523.15	Next Page	See 98.2.4.3	RO
7.523.14	Acknowledge	See 98.2.4.3	RO
7.523.13	Message page	See 98.2.4.3	RO
7.523.12	Acknowledge 2	See 98.2.4.3	RO
7.523.11	Toggle	See 98.2.4.3	RO
7.523.10:0	Message/Unformatted code field	See 98.2.4.3	RO
7.524.15:0	Unformatted code field 1	See 98.2.4.3	RO
7.525.15:0	Unformatted code field 2	See 98.2.4.3	RO

[a]RO = Read only

The value of registers 7.524 and 7.525 is latched when register 7.523 is read and reads of registers 7.524 and 7.525 return the latched value rather than the current value.

NOTE—If this register is used to store multiple link partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent link partner Next Pages.

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45.2.7.26 10BASE-T1 AN control register (Register 7.526)

The assignment of bits in the 10BASE-T1 AN control register is shown in Table 45–401. The default value for each bit of the 10BASE-T1 AN control register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45–401—10BASE-T1 AN control register bit definitions

Bit(s)	Name	Description	R/W[a]
7.526.15	10BASE-T1L capability advertisement	1 = Advertise PHY as 10BASE-T1L capable 0 = Do not advertise PHY as 10BASE-T1L capable	R/W
7.526.14	10BASE-T1L EEE ability advertisement	1 = Advertise that the 10BASE-T1L PHY has EEE ability 0 = Do not advertise that the 10BASE-T1L PHY has EEE ability (default)	R/W
7.526.13	10BASE-T1L increased transmit/receive level ability advertisement	1 = Advertise that the 10BASE-T1L PHY has increased transmit/receive level ability 0 = Do not advertise that the 10BASE-T1L PHY has increased transmit/receive level ability (default)	R/W
7.526.12	10BASE-T1L increased transmit level request	1 = Request 10BASE-T1L increased transmit level 0 = Do not request 10BASE-T1L increased transmit level (default)	R/W
7.526.11:8	Reserved	Value always 0	RO
7.526.7	10BASE-T1S full duplex ability advertisement	1 = Advertise that the 10BASE-T1S PHY has full duplex ability 0 = Do not advertise that the 10BASE-T1S PHY has full duplex ability	R/W
7.526.6	10BASE-T1S half duplex capability advertisement	1 = Advertise PHY as 10BASE-T1S half duplex capable 0 = Do not advertise PHY as 10BASE-T1S half duplex capable	R/W
7.526.5:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

45.2.7.26.1 10BASE-T1L capability advertisement (7.526.15)

Bit 7.526.15 is used to select whether Auto-Negotiation advertises the capability to operate as a 10BASE-T1L PHY. If bit 7.526.15 is set to one, the PHY shall advertise 10BASE-T1L capability. If bit 7.526.15 is set to zero, the PHY shall not advertise the capability to operate as a 10BASE-T1L PHY.

45.2.7.26.2 10BASE-T1L EEE ability advertisement (7.526.14)

If the device supports EEE ability for 10BASE-T1L, as defined in 146.1.2.3, and EEE operation is desired, bit 7.526.14 shall be set to one.

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45.2.7.26.3 10BASE-T1L increased transmit/receive level ability advertisement (7.526.13)

If the device supports the 2.4 Vpp operating mode for 10BASE-T1L, as defined in 146.5.4.1, bit 7.526.13 shall be set to one.

45.2.7.26.4 10BASE-T1L increased transmit level request (7.526.12)

If the device supports the 2.4 Vpp operating mode for 10BASE-T1L, as defined in 146.5.4.1, and the 2.4 Vpp transmit voltage operation is desired, bit 7.526.12 is set to one. Bit 7.526.12 is used to select whether Auto-Negotiation advertises a request to operate the 10BASE-T1L PHY in increased transmit level mode. If bit 7.526.12 is set to one, the PHY shall advertise a request to operate the 10BASE-T1L PHY in increased transmit level mode. If bit 7.526.12 is set to zero, the PHY shall not advertise a request to operate the 10BASE-T1L PHY in increased transmit level mode.

45.2.7.26.5 10BASE-T1S full duplex ability advertisement (7.526.7)

Bit 7.526.7 is used to select whether Auto-Negotiation advertises the ability to operate the 10BASE-T1S PHY in full duplex mode. If bit 7.526.7 is set to one, the PHY shall advertise 10BASE-T1S full duplex capability. If bit 7.526.7 is set to zero, the PHY shall not advertise the ability to operate in 10BASE-T1S full duplex mode.

45.2.7.26.6 10BASE-T1S half duplex capability advertisement (7.526.6)

Bit 7.526.6 is used to select whether Auto-Negotiation advertises the capability to operate the 10BASE-T1S PHY in half duplex mode. If bit 7.526.6 is set to one, the PHY shall advertise 10BASE-T1S half duplex capability. If bit 7.526.6 is set to zero, the PHY shall not advertise the capability to operate in 10BASE-T1S half duplex mode.

45.2.7.27 10BASE-T1 AN status register (Register 7.527)

The assignment of bits in the 10BASE-T1 AN status register is shown in Table 45–402. All the bits in the 10BASE-T1 AN status register are read only; therefore, a write to the 10BASE-T1 AN status register shall have no effect.

When the AN process has been completed, this register shall reflect the contents of the link partner's 10BASE-T1 AN control register. The definitions for the contents of the 10BASE-T1 AN status register are given by the definitions for the contents on the link partner's 10BASE-T1 control register, 7.526 (see 45.2.7.26).

Table 45–402—10BASE-T1 AN status register bit definitions

Bit(s)	Name	Description	R/W[a]
7.527.15	10BASE-T1L link partner capability advertisement	1 = Link partner is advertising PHY as 10BASE-T1L capable 0 = Link partner is not advertising PHY as 10BASE-T1L capable	RO
7.527.14	10BASE-T1L link partner EEE ability advertisement	1 = Link partner is advertising that the 10BASE-T1L PHY has EEE ability 0 = Link partner is not advertising that the 10BASE-T1L PHY has EEE ability	RO

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Table 45–402—10BASE-T1 AN status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
7.527.13	10BASE-T1L link partner increased transmit/receive level ability advertisement	1 = Link partner is advertising that the 10BASE-T1L PHY has increased transmit/receive level ability 0 = Link partner is not advertising that the 10BASE-T1L PHY has increased transmit/receive level ability	RO
7.527.12	10BASE-T1L link partner increased transmit level request	1 = Link partner is requesting 10BASE-T1L link partner increased transmit level 0 = Link partner is not requesting 10BASE-T1L link partner increased transmit level	RO
7.527.11:8	Reserved	Value always 0	RO
7.527.7	10BASE-T1S link partner full duplex ability advertisement	1 = Link partner is advertising that the 10BASE-T1S PHY has full duplex ability 0 = Link partner is not advertising that the 10BASE-T1S PHY has full duplex ability	RO
7.527.6	10BASE-T1S link partner half duplex capability advertisement	1 = Link partner is advertising PHY as 10BASE-T1S half duplex capable 0 = Link partner is not advertising PHY as 10BASE-T1S half duplex capable	RO
7.527.5:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.8 OFDM PMA/PMD registers

The assignment of registers in the OFDM PMA/PMD MMD is shown in Table 45–403.

Table 45–403—OFDM PMA/PMD registers

Register address	Register name	Subclause
12.0	10GPASS-XR DS OFDM channel ID	45.2.8.1
12.1 through 12.1023	10GPASS-XR DS profile descriptor control	45.2.8.2
12.1024 through 12.2047	10GPASS-XR US profile descriptor control	45.2.8.3
12.2048 through 12.10239	10GPASS-XR US pre-equalizer coefficients	45.2.8.4
12.10240 through 12.10241	10GPASS-XR receive MER control	45.2.8.5
12.10242 through 12.12287	10GPASS-XR receive MER measurement	45.2.8.6
12.12288 through 12.32767	Reserved	

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45.2.8.1 10GPASS-XR DS OFDM channel ID register (Register 12.0)

The assignment of bits in the DS OFDM channel ID register is shown in Table 45–404.

Table 45–404—10GPASS-XR DS OFDM channel ID register bit definitions

Bit(s)	Name	Description	R/W[a]
12.0.15:3	Reserved	Value always 0	RO
12.0.2:0	DS OFDM channel ID	Identifies to which OFDM channel (1 to 5) registers 12.1 through 12.1023 currently apply	R/W

[a]RO = Read only, R/W = Read/Write

45.2.8.1.1 DS OFDM channel ID (12.0.2:0)

Bits 12.0.2:0 form a pointer to one of the five possible OFDM channels in the downstream EPoC network. Thus when this register is set to a value of one registers 12.1 through 12.1023 reflect the OFDM profile descriptor for OFDM channel one. When this register is set to a value of two registers 12.1 through 12.1023 reflect the OFDM profile descriptor for OFDM channel two, etc. These bits are a reflection of the *DS_OFDM_ID* variable defined in 101.4.3.4.5.

45.2.8.2 10GPASS-XR DS profile descriptor control 1 through 1023 (Registers 12.1 through 12.1023)

The 10GPASS-XR DS profile descriptor control registers determine the modulation parameters for each downstream OFDM subcarrier. Each register in the group controls 4 of the 4096 subcarriers that are transmitted over the OFDM channel. Register 12.1 describes modulation parameters for downstream OFDM subcarriers number 4 through 7. Register 12.2 describes modulation parameters for downstream OFDM subcarriers number 8 through 11. Finally, register 12.1023 describes modulation parameters for downstream OFDM subcarriers number 4092 through 4095. Note that the first four subcarriers (i.e., subcarriers number 0 through 3) are not specified and are always excluded.

The assignment of bits in register 12.1 is shown in Table 45–405. The remaining registers 12.2 through 12.1023 have the same bit structure as that of register 12.1. Changing registers 12.1 through 12.1023 does not affect the active profile, only the inactive profile (see 102.2.3.1.1 for a description of the Configuration ID bits in the PHY Link frame for information on active profile control). Registers 12.1 through 12.1023 are a reflection of variables *DS_ModTypeSC(n)* defined in 101.4.3.4.5.

Table 45–405—10GPASS-XR DS profile descriptor control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
12.1.15:12	DS modulation type SC7	Modulation profile for subcarrier 7	R/W
12.1.11:8	DS modulation type SC6	Modulation profile for subcarrier 6	R/W
12.1.7:4	DS modulation type SC5	Modulation profile for subcarrier 5	R/W
12.1.3:0	DS modulation type SC4	Modulation profile for subcarrier 4	R/W

[a]R/W = Read/Write

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45.2.8.2.1 DS modulation type SC7 (12.1.15:12)

Bits 12.1.15:12 indicate the modulation profile for downstream OFDM subcarrier number 7. These bits are a reflection of variable *DS_ModTypeSC(7)* defined in 101.4.3.4.5. See the variable definition for interpretation of individual bits.

45.2.8.2.2 DS modulation type SC6 (12.1.11:8)

Bits 12.1.11:8 indicate the modulation profile for downstream OFDM subcarrier number 6. These bits are a reflection of variable *DS_ModTypeSC(6)* defined in 101.4.3.4.5. See the variable definition for interpretation of individual bits.

45.2.8.2.3 DS modulation type SC5 (12.1.7:4)

Bits 12.1.7:4 indicate the modulation profile for downstream OFDM subcarrier number 5. These bits are a reflection of variable *DS_ModTypeSC(5)* defined in 101.4.3.4.5. See the variable definition for interpretation of individual bits.

45.2.8.2.4 DS modulation type SC4 (12.1.3:0)

Bits 12.1.3:0 indicate the modulation profile for downstream OFDM subcarrier number 4. These bits are a reflection of variable *DS_ModTypeSC(4)* defined in 101.4.3.4.5. See the variable definition for interpretation of individual bits.

45.2.8.3 10GPASS-XR US profile descriptor control 0 through 1023 registers (Registers 12.1024 through 12.2047)

The 10GPASS-XR US profile descriptor control 0 through 1023 registers determine the inactive modulation settings for the upstream OFDMA spectrum. Each register in the group controls 4 subcarriers of the 4096 subcarriers that are transmitted over the OFDMA channel, with the first register in the group (12.1024) controlling subcarriers 0 through 3 and the second register controlling subcarriers 4 through 7, etc. The assignment of bits in the first 10GPASS-XR US profile descriptor control register (register 12.1024) is shown in Table 45–406. Bit assignment per subcarrier for the remaining registers is identical to that of register 12.1024. See 101.4.5 for details on each modulation type. Registers 12.1024 through 12.2047 are a reflection of variables *US_ModTypeSC(n)* defined in 101.4.4.4.4.

Table 45–406—10GPASS-XR US profile descriptor control 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
12.1024.15:12	US modulation type SC3	Modulation profile for subcarrier 3	R/W
12.1024.11:8	US modulation type SC2	Modulation profile for subcarrier 2	R/W
12.1024.7:4	US modulation type SC1	Modulation profile for subcarrier 1	R/W
12.1024.3:0	US modulation type SC0	Modulation profile for subcarrier 0	R/W

[a]R/W = Read/Write

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45.2.8.3.1 US modulation type SC3 (12.1024.15:12)

Bits 12.1024.15:12 indicate the modulation profile for upstream OFDM subcarrier number 3. These bits are a reflection of variable *US_ModTypeSC(3)* defined in 101.4.4.4.4. See the variable definition for interpretation of individual bits.

45.2.8.3.2 US modulation type SC2 (12.1024.11:8)

Bits 12.1024.11:8 indicate the modulation profile for upstream OFDM subcarrier number 2. These bits are a reflection of variable *US_ModTypeSC(2)* defined in 101.4.4.4.4. See the variable definition for interpretation of individual bits.

45.2.8.3.3 US modulation type SC1 (12.1024.7:4)

Bits 12.1024.7:4 indicate the modulation profile for upstream OFDM subcarrier number 1. These bits are a reflection of variable *US_ModTypeSC(1)* defined in 101.4.4.4.4. See the variable definition for interpretation of individual bits.

45.2.8.3.4 US modulation type SC0 (12.1024.3:0)

Bits 12.1024.3:0 indicate the modulation profile for upstream OFDM subcarrier number 0. These bits are a reflection of variable *US_ModTypeSC(0)* defined in 101.4.4.4.4. See the variable definition for interpretation of individual bits.

45.2.8.4 10GPASS-XR US pre-equalizer coefficients 0 through 4095 (Registers 12.2048 through 12.10239)

The 10GPASS-XR US pre-equalizer coefficients 0 through 4095 registers determine the real and imaginary parts of the pre-equalizer settings for the upstream transmitter. Each register pair in the group controls one subcarrier of the 4096 subcarriers that are transmitted over the OFDMA channel, with the first register in the group (12.2048) controlling the real number setting for subcarrier 0 and the second register (12.2049) controlling the imaginary number setting for subcarrier 0. The second register pair (12.2050 and 12.2051) respectively controls the real and imaginary settings for subcarrier 1. Thus the last register pair (12.10238 and 12.10239) controls the real and imaginary settings for subcarrier 4095. The value in each register is in a Q2.14 format. The assignment of bits in the first and second 10GPASS-XR US pre-equalizer coefficients registers (registers 12.2048 and 12.2049) is shown in Table 45–407. Bit assignment per subcarrier for the remaining even and odd registers is identical to that of registers 12.2048 and 12.2049, respectively. See 101.4.4.9 for details on use of these registers. These registers are a reflection of the variables *EQ_CoefR(n)* and *EQ_CoefI(n)* defined in 101.4.4.9.2.

Table 45–407—10GPASS-XR US pre-equalizer coefficients registers bit definitions

Bit(s)	Name	Description	R/W[a]
12.2048.15:0	Real pre-equalizer coefficient SC0	Real part of the pre-equalizer coefficient for subcarrier 0	R/W
12.2049.15:0	Imaginary pre-equalizer coefficient SC0	Imaginary part of the pre-equalizer coefficient for subcarrier 0	R/W

[a]R/W = Read/Write

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45.2.8.4.1 Real pre-equalizer coefficient SC0 (12.2048.15:0)

Bits 12.2048.15:0 indicate the real part of the pre-equalizer coefficient for subcarrier 0 for the upstream OFDMA channel. These bits are a reflection of the variable *EQ_CoefR(0)* defined in 101.4.4.9.2.

45.2.8.4.2 Imaginary pre-equalizer coefficient SC0 (12.2049.15:0)

Bits 12.2049.15:0 indicate the imaginary part of the pre-equalizer coefficient for subcarrier 0 for the upstream OFDMA channel. These bits are a reflection of the variable *EQ_CoefI(0)* defined in 101.4.4.9.2.

45.2.8.5 10GPASS-XR receive MER control registers (Registers 12.10240 and 12.10241)

The assignment of bits in the 10GPASS-XR receive MER control registers is shown in Table 45–408.

Table 45–408—10GPASS-XR receive MER control register bit definitions

Bit(s)	Name	Description	R/W[a]
12.10240.15:4	Reserved	Value always 0	RO
12.10240.3	MER measurement valid	1 = all values in the 10GPASS-XR receive MER measurement registers are valid 0 = some values in the 10GPASS-XR receive MER measurement registers are invalid	RO
12.10240.2:0	Receive MER channel ID	Identifies to which OFDM channel (1 to 5) registers 12.10242 through 12.12287 currently apply	R/W[b]
12.10241.15	Reserved	Value always 0	RO
12.10241.14:0	Receive MER CNU ID	Identifies to which CNU registers 12.10242 through 12.12287 currently apply	

[a]RO = Read only, R/W = Read/Write
[b]These bits are valid only in the CNU; in the CLT these bits are reserved and always 0.

45.2.8.5.1 MER measurement valid (12.10240.3)

When read as one, bit 12.10240.3 indicates the 10GPASS-XR receive MER measurement registers are valid. When read as zero, this bit indicates that the 10GPASS-XR receive MER measurement registers are not valid. This bit is a reflection of the variable *RxMER_Valid* defined in 100.3.5.3.1.

45.2.8.5.2 Receive MER Channel ID (12.10240.2:0)

Bits 12.10240.2:0 form a pointer to one of the five possible OFDM channels in the EPoC network. These bits are only valid for 10GPASS-XR-U PMA/PMD and are reserved for 10GPASS-XR-D PMA/PMD and always read as zero. These bits are a reflection of the variable *RxMER_ChID* defined in 100.3.5.3.1.

45.2.8.5.3 Receive MER CNU ID (12.10241.14:0)

Bits 12.10241.14:0 indicate the CNU_ID of the CNU on which to measure the MER and report in registers 12.10242 through 12.12287. These bits are only valid for 10GPASS-XR-D PMA/PMD and are reserved for 10GPASS-XR-U PMA/PMD and always read as zero. These bits are a reflection of the variable *RxMER_CNU_ID* defined in 100.3.5.3.1.

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45.2.8.6 10GPASS-XR receive MER measurement registers (Registers 12.10242 through 12.12287)

The 10GPASS-XR receive MER measurement registers reflect the MER measured on each OFDM subcarrier for the OFDM channel indicated by the Receive MER Channel ID except subcarriers zero through three. Each register in the group reflects two of the 4096 subcarriers that are transmitted over the OFDM channel. Register 12.10242 reflects the receive MER measured on OFDM subcarriers number 4 and 5. Register 12.10243 reflects the receive MER measured on OFDM subcarriers number 6 and 7. Finally, register 12.12287 reflects the receive MER measured on OFDM subcarriers number 4094 and 4095. Note that the first four subcarriers (i.e., subcarriers number 0 through 3) are not reflected in register group 12.10242 through 12.12287 (10GPASS-XR receive MER measurement registers).

The assignment of individual bits in register 12.10242 is shown in Table 45–409. The remaining registers 12.10243 through 12.12287 have the same bit structure as that of register 12.10242. These registers are a reflection of the variable *RxMER_SC(n)* defined in 100.3.5.3.1.

Table 45–409—10GPASS-XR receive MER measurement register bit definitions

Bit(s)	Name	Description	R/W[a]
12.10242.15:8	Receive MER SC5	Receive MER measurement for subcarrier 5 on the OFDM channel indicated by the Receive MER Channel ID	RO
12.10242.7:0	Receive MER SC4	Receive MER measurement for subcarrier 4 on the OFDM channel indicated by the Receive MER Channel ID	RO

[a]RO = Read only

45.2.8.6.1 Receive MER SC5 (12.10242.15:8)

Bits 12.10242.15:8 reflect the MER measured on OFDM subcarrier 5 for the OFDM channel indicated by the Receive MER channel ID.

45.2.8.6.2 Receive MER SC4 (12.10242.7:0)

Bits 12.10242.7:0 reflect the MER measured on OFDM subcarrier 4 for the OFDM channel indicated by the Receive MER channel ID.

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45.2.9 Power Unit registers

The assignment of registers in the Power Unit MMD is shown in Table 45–410.

Table 45–410—Power Unit MMD registers

Register address	Register name	Subclause
13.0	PoDL PSE Control	45.2.9.1
13.1	PoDL PSE Status 1	45.2.9.2
13.2	PoDL PSE Status 2	45.2.9.3
13.3	PoDL PSE Status 3	45.2.9.4
13.4	PoDL PSE Status 4	45.2.9.5

45.2.9.1 PoDL PSE Control register (Register 13.0)

The assignment of bits in the PoDL PSE Control register is shown in Table 45–411. The default value for each bit of the PoDL PSE Control register should be chosen so that the initial state of the PSE upon power up or reset is a normal operational state without management intervention.

Table 45–411—PoDL PSE Control register bit definitions

Bit(s)	Name	Description	R/W[a]
13.0.15:3	Reserved	Value always 0	RO
13.0.2	Enable cable resistance measurement	1 = Cable resistance measurement enabled 0 = Cable resistance measurement disabled	R/W
13.0.1	Enable power classification	1 = Power classification enabled 0 = Power classification disabled	R/W
13.0.0	PSE Enable	1 = PSE Enabled 0 = PSE Disabled	R/W

[a]R/W = Read/Write, RO = Read Only

45.2.9.1.1 Enable power classification (13.0.1)

The power classification function is enabled by setting bit 13.0.1 to one and disabled by setting bit 13.0.1 to zero. This bit maps to the mr_sccp_enabled variable (see 104.4.4.3).

45.2.9.1.2 PSE Enable (13.0.0)

When bit 13.0.0 is set to zero, the PSE function shall be disabled. When bit 13.0.0 is set to one, the PSE function shall be enabled. This register bit maps to the mr_pse_enable variable (see 104.4.4.3).

45.2.9.2 PoDL PSE Status 1 register (Register 13.1)

The assignment of bits in the PoDL PSE Status 1 register is shown in Table 45–412.

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Table 45–412—PoDL PSE Status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
13.1.15	Power Denied	1 = Power has been denied due to power not available 0 = Power has not been denied due to power not available	RO/ LH
13.1.14	Valid Signature	1 = Valid PD signature detected 0 = No valid PD signature detected	RO/ LH
13.1.13	Invalid Signature	1 = Invalid PD signature detected 0 = No invalid PD signature detected	RO/ LH
13.1.12	Class Timeout	1 = Classification timeout condition detected 0 = No Classification timeout condition detected	RO/ LH
13.1.11	Overload	1 = Overload condition detected 0 = No overload condition detected	RO/ LH
13.1.10	MFVS Absent	1 = MFVS absent condition detected 0 = No MFVS absent condition detected	RO/ LH
13.1.9:7	PSE Type	9 8 7 1 1 x = Reserved 1 0 1 = Type F PSE 1 0 0 = Type E PSE 0 1 1 = Type D PSE 0 1 0 = Type C PSE 0 0 1 = Type B PSE 0 0 0 = Type A PSE	RO
13.1.6:3	PD Class	6 5 4 3 1 1 1 1 = Extend to PoDL PSE status 2 register 1 1 1 0 = Class code 14 1 1 0 1 = Class code 13 1 1 0 0 = Class code 12 1 0 1 1 = Class code 11 1 0 1 0 = Class code 10 1 0 0 1 = Class code 9 1 0 0 0 = Class code 8 0 1 1 1 = Class code 7 0 1 1 0 = Class code 6 0 1 0 1 = Class code 5 0 1 0 0 = Class code 4 0 0 1 1 = Class code 3 0 0 1 0 = Class code 2 0 0 0 1 = Class code 1 0 0 0 0 = Class code 0	RO
13.1.2:0	PSE Status	2 1 0 1 1 1 = Unknown 1 1 0 = Reserved 1 0 1 = Idle 1 0 0 = Error 0 1 1 = Searching 0 1 0 = Delivering power 0 0 1 = Sleep 0 0 0 = Disabled	RO

[a]RO = Read Only, LH = Latching High

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45.2.9.2.1 Power Denied (13.1.15)

When read as a one, bit 13.1.15 indicates that application of full operating voltage at the PI has been denied. This bit shall be set to one when power_available transitions from true to false (see 104.4.4.3). The Power Denied bit shall be implemented with latching high behavior as defined in 45.2.

45.2.9.2.2 Valid Signature (13.1.14)

When read as a one, bit 13.1.14 indicates that a valid signature has been detected. This bit shall be set to one when mr_valid_signature transitions from false to true (see 104.4.4.3). The Valid Signature bit shall be implemented with latching high behavior as defined in 45.2.

45.2.9.2.3 Invalid Signature (13.1.13)

When read as a one, bit 13.1.13 indicates that an invalid signature has been detected. This bit maps to the PSE state diagram variable mr_invalid_signature, and latches high when mr_invalid_signature transitions from false to true (see 104.4.4.3). The Invalid Signature bit shall be implemented with latching high behavior as defined in 45.2.

45.2.9.2.4 Class Timeout (13.1.12)

When read as a one, bit 13.1.12 indicates that a Classification timeout condition has been detected. The Class Timeout bit shall be set to one when tclass_timer_done transitions from false to true (see 104.4.4.3). The Class Timeout bit shall be implemented with latching high behavior as defined in 45.2.

45.2.9.2.5 Overload (13.1.11)

When read as a one, bit 13.1.11 indicates that an overload condition has been detected. This bit shall be set to one when the PSE state diagram variable overload_held transitions from false to true (see 104.4.4.3). The Overload bit shall be implemented with latching high behavior as defined in 45.2.

45.2.9.2.6 MFVS Absent (13.1.10)

When read as a one, bit 13.1.10 indicates that an MFVS Absent condition has been detected. The MFVS Absent bit shall be set to one when mfvs_timeout transitions from false to true (see 104.4.4.3). The MFVS Absent bit shall be implemented with latching high behavior as defined in 45.2.

45.2.9.2.7 PSE Type (13.1.9:7)

Bits 13.1.9:7 report the PSE Type of the PSE as specified in 104.4.1. When read as 000, bits 13.1.9:7 indicate a Type A PSE; when read as 001, a Type B PSE is indicated; when read as 010, a Type C PSE is indicated; when read as 011, a Type D PSE is indicated; when read as 100, a Type E PSE is indicated; and when read as 101, a Type F PSE is indicated. Values of 11x are reserved.

45.2.9.2.8 PD Class (13.1.6:3)

Bits 13.1.6:3 report the PD Class of a detected PD as specified in 104.5.3. The value in this register is valid while a PD is connected, i.e., while the PSE Status (13.1.2:0) bits are reporting “delivering power”. When read as 0000, a Class 0 PD is indicated; when read as 0001, a Class 1 PD is indicated; when read as 0010, a Class 2 PD is indicated; when read as 0011, a Class 3 PD is indicated; when read as 0100, a Class 4 PD is indicated; when read as 0101, a Class 5 PD is indicated; when read as 0110, a Class 6 PD is indicated; when read as 0111, a Class 7 PD is indicated; when read as 1000, a Class 8 PD is indicated; when read as 1001, a Class 9 PD is indicated; when read as 1010, a Class 10 PD is indicated; when read as 1011, a Class 11 PD is indicated; when read as 1100, a Class 12 PD is indicated; when read as 1101, a Class 13 PD is indicated;

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when read as 1110, a Class 14 PD is indicated; and when read as 1111, the Class is indicated by the PD Extended Class (13.2.10:9) bits.

45.2.9.2.9 PSE Status (13.1.2:0)

Bits 13.1.2:0 report the current status of the PSE. When read as 000, bits 13.1.2:0 indicate that mr_pse_enable is asserted false (see 104.4.4.3). When read as 001, bits 13.1.2:0 indicate that pi_sleeping is asserted true. When read as 010, bits 13.1.2:0 indicate that pi_powered is asserted true. When read as 011, bits 13.1.2:0 indicate that either pi_detecting or pi_classifying is are asserted true. When read as 100, bits 13.1.2:0 indicate that overload_held is asserted true. When read as 101, bits 13.1.2:0 indicate that the logical combination pi_prebiased*!pi_sleeping is true. When read as 111, bits 13.1.2:0 indicate that the PSE status is unkown. Bit combination 110 is reserved.

45.2.9.3 PoDL PSE Status 2 register (Register 13.2)

The PoDL PSE Status 2 register is an extension of the PoDL PSE Status 1 register. Assignment of bits in the PoDL PSE Status 2 register is shown in Table 45–413.

Table 45–413—PoDL PSE Status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
13.2.15	Invalid Class	1 = Invalid PD class detected 0 = No invalid PD class detected	RO/LH
13.2.14:11	Reserved	Value always 0	RO
13:2.10:9	PD Extended Class	10 9 1 1 = Reserved 1 0 = Reserved 0 1 = Reserved 0 0 = Class code 15	RO
13.2.8:3	Reserved	Value always 0	RO
13.2.2:0	PD Type	2 1 0 1 1 1 = Unknown 1 1 0 = Reserved 1 0 1 = Type F PD 1 0 0 = Type E PD 0 1 1 = Type D PD 0 1 0 = Type C PD 0 0 1 = Type B PD 0 0 0 = Type A PD	RO

[a]RO = Read Only, LH = Latching High

45.2.9.3.1 Invalid Class (13.2.15)

When read as a one, bit 13.2.15 indicates that an invalid class has been detected. This bit maps to the PSE state diagram variable valid_class, and latches high when do_classification_done is true and valid_class is false (see 104.4.4.3). The Invalid Class bit shall be implemented with latching high behavior as defined in 45.2.

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45.2.9.3.2 PD Extended Class (13.2.10:9)

When bits 13.2.10:9 are read as 00, a Class 15 PD is indicated. Values of 01 and 1x are reserved.

45.2.9.3.3 PD Type (13.2.2:0)

Bits 13.2.2:0 report a value of 111 until a valid classification has taken place, or if no PD is present. A value of 111 indicates that the PSE has not performed classification and therefore cannot indicate the proper value for the PD Type. Once a valid classification has occurred, the value of these bits reflect the PD Type of an attached PD as specified in 104.5.1. When read as 000, bits 13.2.2:0 indicate a Type A PD; when read as 001, a Type B PD is indicated; when read as 010, a Type C PD is indicated; when read as 011, a Type D PD is indicated; when read as 100, a Type E PD is indicated; and when read as 101, a Type F PD is indicated. A value of 110 is reserved.

45.2.9.4 PoDL PSE Status 3 register (Register 13.3)

The PoDL PSE Status 3 register is defined if cable resistance measurement is supported.

Table 45–414—PoDL PSE Status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
13.3.15:12	Reserved	Value always 0	RO
13.3.11:0	PD Assigned Power	PD Assigned Power, 0.025 W per LSB	RO

[a]RO = Read only

45.2.9.4.1 PD Assigned Power (13.3.11:0)

The PD Assigned Power is the maximum average available power at the PD PI.

45.2.9.5 PoDL PSE Status 4 register (Register 13.4)

The PoDL PSE Status 4 register is defined if cable resistance measurement is supported.

Table 45–415—PoDL PSE Status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
13.4.15:12	Reserved	Value always 0	RO
13.4.11:0	PD Requested Power	PD Requested Power, 0.025 W per LSB	RO

[a]RO = Read only

45.2.9.5.1 PD Requested Power (13.4.11:0)

The PD Requested Power is the requested average available power at the PD PI.

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45.2.10 Clause 22 extension registers

As new management features are added to 10, 100, and 1000 Mb/s PHYs, more register space is required beyond that defined in Clause 22. The Clause 22 extension MMD provides this space. This MMD is defined only for 10, 100, and 1000 Mb/s PHYs. Since these PHYs do not segment their management by their sublayers, all management extensions to these PHYs will appear in the Clause 22 extension MMD.

The assignment of registers in the Clause 22 extension MMD is shown in Table 45–416.

Table 45–416—Clause 22 extension registers

Register address	Register name	Subclause
29.0 through 29.4	Reserved	
29.5, 29.6	Clause 22 extension devices in package	45.2.10.1
29.7	FEC capability	45.2.10.2
29.8	FEC control	45.2.10.3
29.9	FEC buffer head coding violation counter	45.2.10.4
29.10	FEC corrected blocks counter	45.2.10.5
29.11	FEC uncorrected blocks counter	45.2.10.6
29.12 through 29.32 767	Reserved	

45.2.10.1 Clause 22 extension devices in package registers (Registers 29.5, 29.6)

The Clause 22 extension devices in package registers are defined in Table 45–2.

45.2.10.2 FEC capability register (Register 29.7)

The assignment of bits in the FEC capability register is shown in Table 45–417.

Table 45–417—FEC capability register bit definitions

Bit(s)	Name	Description	R/W[a]
29.7.15:1	Reserved	Value always 0	RO
29.7.0	FEC capable	1 = FEC supported 0 = FEC unsupported	RO

[a]RO = Read only

45.2.10.2.1 FEC capable (29.7.0)

When read as a one, this bit indicates that the PHY supports forward error correction. When read as a zero, the PHY does not support forward error correction.

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45.2.10.3 FEC control register (Register 29.8)

The assignment of bits in the FEC control register is shown in Table 45–418.

Table 45–418—FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
29.8.15:1	Reserved	Value always 0	RO
29.8.0	FEC enable	1 = FEC enabled 0 = FEC disabled	R/W

[a]RO = Read only, R/W = Read/Write

45.2.10.3.1 FEC enable (29.8.0)

When written as a one, this bit enables the PHY's forward error correction. When written as a zero, FEC is disabled. This bit shall be set to zero upon execution of a PHY reset.

45.2.10.4 FEC buffer head coding violation counter (Register 29.9)

The assignment of bits in the FEC buffer head coding violation counter register is shown in Table 45–419. See 65.2.3.6.1 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow.

Table 45–419—FEC buffer head coding violation counter register bit definitions

Bit(s)	Name	Description	R/W[a]
29.9.15:0	FEC buffer head coding violation counter	Error counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.10.5 FEC corrected blocks counter (Register 29.10)

The assignment of bits in the FEC corrected blocks counter register is shown in Table 45–420. See 65.2.3.6.2 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow.

Table 45–420—FEC corrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
29.10.15:0	FEC corrected blocks counter	Error counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

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45.2.10.6 FEC uncorrected blocks counter (Register 29.11)

The assignment of bits in the FEC uncorrected blocks counter register is shown in Table 45–421. See 65.2.3.6.3 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow.

Table 45–421—FEC uncorrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
29.11.15:0	FEC uncorrected blocks counter	Error counter	RO, NR

[a]RO = Read only, NR = Non Roll-over

45.2.11 Vendor specific MMD 1 registers

The assignment of registers in the vendor specific MMD 1 is shown in Table 45–422. A vendor specific MMD may have a device address of either 30 or 31. It is recommended that the device address is configurable and that the configuration is performed by some means other than via the MDIO.

Table 45–422—Vendor specific MMD 1 registers

Register address	Register name
30.0, 30.1	Vendor specific
30.2, 30.3	Vendor specific MMD 1 device identifier
30.4 through 30.7	Vendor specific
30.8	Vendor specific MMD 1 status register
30.9 through 30.13	Vendor specific
30.14, 30.15	Vendor specific MMD 1 package identifier
30.16 through 30.65 535	Vendor specific

45.2.11.1 Vendor specific MMD 1 device identifier (Registers 30.2 and 30.3)

Registers 30.2 and 30.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of vendor-specific device. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor-specific device may return a value of zero in each of the 32 bits of the vendor specific MMD 1 device identifier.

The format of the vendor specific MMD 1 device identifier is specified in 22.2.4.3.1.

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45.2.11.2 Vendor specific MMD 1 status register (Register 30.8)

The assignment of bits in the vendor specific MMD 1 status register is shown in Table 45–423. All the bits in the vendor specific MMD 1 status register are read only; a write to the vendor specific MMD 1 status register shall have no effect.

Table 45–423—Vendor specific MMD 1 status register bit definitions

Bit(s)	Name	Description	R/W[a]
30.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
30.8.13:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.11.2.1 Device present (30.8.15:14)

When read as <10>, bits 30.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 30.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.11.3 Vendor specific MMD 1 package identifier (Registers 30.14 and 30.15)

Registers 30.14 and 30.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the vendor specific MMD 1 is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific MMD 1 may return a value of zero in each of the 32 bits of the vendor specific MMD 1 package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the vendor specific MMD 1 package identifier is specified in 22.2.4.3.1.

45.2.12 Vendor specific MMD 2 registers

The assignment of registers in the vendor specific MMD 2 is shown in Table 45–424. A vendor specific MMD may have a device address of either 30 or 31. It is recommended that the device address is configurable and that the configuration is performed by some means other than via the MDIO.

Table 45–424—Vendor specific MMD 2 registers

Register address	Register name	Subclause
31.0, 31.1	Vendor specific	
31.2, 31.3	Vendor specific MMD 2 device identifier	45.2.12.1

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Table 45–424—Vendor specific MMD 2 registers *(continued)*

Register address	Register name	Subclause
31.4 through 31.7	Vendor specific	
31.8	Vendor specific MMD 2 status register	45.2.12.2
31.9 through 31.13	Vendor specific	
31.14, 30.15	Vendor specific MMD 2 package identifier	45.2.12.3
31.16 through 31.65 535	Vendor specific	

45.2.12.1 Vendor specific MMD 2 device identifier (Registers 31.2 and 31.3)

Registers 31.2 and 31.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of vendor-specific device. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor-specific device may return a value of zero in each of the 32 bits of the vendor specific MMD 2 device identifier.

The format of the vendor specific MMD 2 device identifier is specified in 22.2.4.3.1.

45.2.12.2 Vendor specific MMD 2 status register (Register 31.8)

The assignment of bits in the vendor specific MMD 2 status register is shown in Table 45–425. All the bits in the vendor specific MMD 2 status register are read only; a write to the vendor specific MMD status register shall have no effect.

Table 45–425—Vendor specific MMD 2 status register bit definitions

Bit(s)	Name	Description	R/W[a]
31.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
31.8.13:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.12.2.1 Device present (31.8.15:14)

When read as <10>, bits 31.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 31.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

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45.2.12.3 Vendor specific MMD 2 package identifier (Registers 31.14 and 31.15)

Registers 31.14 and 31.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the vendor specific MMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific MMD may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the vendor specific MMD 2 package identifier is specified in 22.2.4.3.1.

45.3 Management frame structure

The MDIO interface frame structure is compatible with the one defined in 22.2.4.5 such that the two systems can co-exist on the same MDIO bus. The electrical specification for the MDIO interface is incompatible to that defined in 22.2.4.5; therefore, if the two systems are to co-exist on the same bus, a voltage translation device is required (see Annex 45A). The extensions that are used for MDIO indirect register accesses are specified in Table 45–426.

Table 45–426—Extensions to management frame format for indirect access

	Management frame fields							
Frame	**PRE**	**ST**	**OP**	**PRTAD**	**DEVAD**	**TA**	**ADDRESS / DATA**	**IDLE**
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Post-read-increment-address	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

Each MMD shall implement a sixteen bit address register that stores the address of the register to be accessed by data transaction frames. The address register shall be overwritten by address frames. At power up or device reset, the contents of the address register are undefined.

Write, read, and post-read-increment-address frames shall access the register whose address is stored in the address register. Write and read frames shall not modify the contents of the address register.

Upon receiving a post-read-increment-address frame and having completed the read operation, the MMD shall increment the address register by one. For the case where the MMD's address register contains 65 535, the MMD shall not increment the address register.

Implementations that incorporate several MMDs within a single component shall implement separate address registers so that the MMD's address registers operate independently of one another.

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45.3.1 IDLE (idle condition)

The idle condition on MDIO is a high-impedance state. All three state drivers shall be disabled and the MMD's pull-up resistor will pull the MDIO line to a one.

45.3.2 PRE (preamble)

At the beginning of each transaction, the station management entity shall send a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC to provide the MMD with a pattern that it can use to establish synchronization. An MMD shall observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

45.3.3 ST (start of frame)

The start of frame for indirect access cycles is indicated by the <00> pattern. This pattern assures a transition from the default one and identifies the frame as an indirect access. Frames that contain the ST=<01> pattern defined in Clause 22 shall be ignored by the devices specified in Clause 45.

45.3.4 OP (operation code)

The operation code field indicates the type of transaction being performed by the frame. A <00> pattern indicates that the frame payload contains the address of the register to access. A <01> pattern indicates that the frame payload contains data to be written to the register whose address was provided in the previous address frame. A <11> pattern indicates that the frame is read operation. A <10> pattern indicates that the frame is a post-read-increment-address operation.

45.3.5 PRTAD (port address)

The port address is five bits, allowing 32 unique port addresses. The first port address bit to be transmitted and received is the MSB of the address. A station management entity has to have a priori knowledge of the appropriate port address for each port to which it is attached, whether connected to a single port or to multiple ports.

45.3.6 DEVAD (device address)

The device address is five bits, allowing 32 unique MMDs per port. The first device address bit transmitted and received is the MSB of the address.

45.3.7 TA (turnaround)

The turnaround time is a 2 bit time spacing between the device address field and the data field of a management frame to avoid contention during a read transaction. For a read or post-read-increment-address transaction, both the STA and the MMD shall remain in a high-impedance state for the first bit time of the turnaround. The MMD shall drive a zero bit during the second bit time of the turnaround of a read or post-read-increment-address transaction. During a write or address transaction, the STA shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround. Figure 22–15 shows the behavior of the MDIO signal during the turnaround field of a read or post-read-increment-address transaction.

45.3.8 ADDRESS / DATA

The address/data field is 16 bits. For an address cycle, it contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, the field contains the data to be written to the register.

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For a read or post-read-increment-address frame, the field contains the contents of the register. The first bit transmitted and received shall be bit 15.

45.4 Electrical interface

45.4.1 Electrical specification

The electrical characteristics of the MDIO interface are shown in Table 45–427. The MDIO uses signal levels that are compatible with devices operating at a nominal supply voltage of 1.2 V. More information on the electrical interface is given in Annex 45A. Voltage translators between the Clause 22 electrical interface and the Clause 45 electrical interface are described in 45A.3 and 45A.4.

NOTE—It is possible to implement the MDIO electrical interface using open drain buffers and a resistive pull-up to a V_{DD} of 1.2 V (see 45A.1).

Table 45–427—MDIO electrical interface characteristics

Symbol	Parameter	Condition	Min.	Max.
V_{IH}	Input high voltage		0.84 V	1.5 V
V_{IL}	Input low voltage		–0.3 V	0.36 V
V_{OH}	Output high voltage	I_{OH} = –100 uA	1.0 V	1.5 V
V_{OL}	Output low voltage	I_{OL} = 100 uA	–0.3 V	0.2 V
I_{OH}[a]	Output high current	V_{OH} = 1.0 V		–4 mA
I_{OL}	Output low current	V_{OL} = 0.2 V	+4 mA	
C_i	Input capacitance			10 pF
C_L	Total capacitive load			470 pF

[a]I_{OH} parameter is not applicable to open drain drivers.

45.4.2 Timing specification

MDIO is a bidirectional signal that can be sourced by the Station Management Entity (STA) or the MMD. When the STA sources the MDIO signal, the STA shall provide a minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC, as shown in Figure 45–3, measured at the MMD.

When the MDIO signal is sourced by the MMD, it is sampled by the STA synchronously with respect to the beginning of the rising edge of MDC. The clock to output delay from the MMD, as measured at the STA, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in Figure 45–4.

The timing specification for the MDC signal is given in 22.2.2.13.

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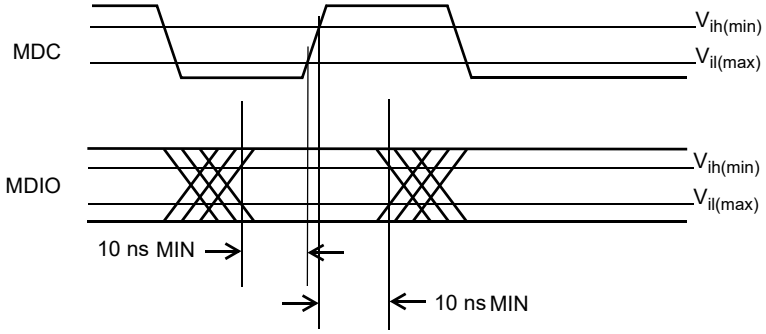

Figure 45–3—MDIO sourced by STA

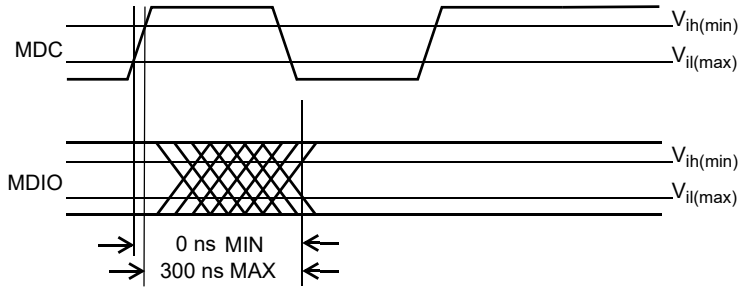

Figure 45–4—MDIO sourced by MMD

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45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) Interface[87]

45.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 45, MDIO interface, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

45.5.2 Identification

45.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

45.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 45, Management Data Input/Output (MDIO) Interface
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[87] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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45.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PMA	Implementation of PMA/PMD MMD	45.2.1		O	Yes [ ] No [ ]
*WIS	Implementation of WIS MMD	45.2.2		O	Yes [ ] No [ ]
*PCS	Implementation of PCS MMD	45.2.3		O	Yes [ ] No [ ]
*PX	Implementation of PHY XS MMD	45.2.4		O	Yes [ ] No [ ]
*DX	Implementation of DTE XS MMD	45.2.5		O	Yes [ ] No [ ]
*VSA	Implementation of Vendor specific MMD 1	45.2.11		O	Yes [ ] No [ ]
*VSB	Implementation of Vendor specific MMD 2	45.2.12		O	Yes [ ] No [ ]
*TC	Implementation of the TC MMD	45.2.6		10P*2B:M	Yes [ ] No [ ]
*CTT	Implementation of the Clause 22 extension MMD	45.2.10		O	Yes [ ] No [ ]
*ODB	Open drain buffer	45.4.1		O	Yes [ ] No [ ]
*AN	Implementation of Auto-Negotiation MMD	45.2.7		O	Yes [ ] No [ ]
*BTC	Implementation of BASE-T1 PMA/PMD	45.2.1.214.1		PMA:O	Yes [ ] No [ ] N/A[ ]
*EO	Implementation of OFDM MMD	45.2.8		O	Yes [ ] No [ ]
*PODL	Implementation of Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet	45.2.9		O	Yes [ ] No [ ]

45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) Interface

45.5.3.1 MDIO signal functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
SF1	MDIO uses three-state drivers	45.4.1		M	Yes [ ]

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45.5.3.2 PMA/PMD MMD options

Item	Feature	Subclause	Value/Comment	Status	Support
*ALB	Implementation of PMA local loopback function	45.2.1.1.5		PMA:O	Yes [ ] No [ ] N/A [ ]
*RLB	Implementation of PMA remote loopback function	45.2.1.1.4		PMA:O	Yes [ ] No [ ] N/A [ ]
*PLF	Implementation of fault detection	45.2.1.7		PMA:O	Yes [ ] No [ ] N/A [ ]
*ALP	Implementation of PMA/PMD low power ability	45.2.1.2.5		PMA:O	Yes [ ] No [ ] N/A [ ]
*PTD	Implementation of transmit disable function	45.2.1.8		PMA:O	Yes [ ] No [ ] N/A [ ]
*2.5T	Implementation of a 2.5GBASE-T PMA	45.2.1.19		PMA:O	Yes [ ] No [ ]
*2.5GKX	Implementation of 2.5GBASE-KX PMA/PMD	45.2.1.19.2		PMA:O	Yes [ ] No [ ]
*5GKR	Implementation of 5GBASE-KR PMA/PMD	45.2.1.19.1		PMA:O	Yes [ ] No [ ]
*5T	Implementation of a 5GBASE-T PMA	45.2.1.19		PMA:O	Yes [ ] No [ ]
*10T	Implementation of the 10GBASE-T PMA	45.2.1.6		PMA:O	Yes [ ] No [ ]
*25T	Implementation of the 25GBASE-T PMA	45.2.1.17		PMA:O	Yes [ ] No [ ]
*40T	Implementation of the 40GBASE-T PMA	45.2.1.12		PMA:O	Yes [ ] No [ ]
*40G	Implementation of 40 Gb/s PMA/PMD	45.2.1.4		PMA:O	Yes [ ] No [ ]
*100G	Implementation of 100 Gb/s PMA/PMD	45.2.1.4		PMA:O	Yes [ ] No [ ]
*10M	Implementation of 10 Mb/s PMA/PMD	45.2.1.4		PMA:O	Yes [ ] No [ ]
*100M	Implementation of 100 Mb/s PMA/PMD	45.2.1.4		PMA:O	Yes [ ] No [ ]
*1G	Implementation of 1000 Mb/s PMA/PMD	45.2.1.4		PMA:O	Yes [ ] No [ ]
*10P	Implementation of the 10PASS-TS PMA/PMD	45.2.1.4		PMA:O	Yes [ ] No [ ]
*2B	Implementation of the 2BASE-TL PMA/PMD	45.2.1.4		PMA:O	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
*2.5G	Implementation of a 2.5 Gb/s PMA/PMD	45.2.1.4		PMA:O	Yes [ ] No [ ]
*5G	Implementation of a 5 Gb/s PMA/PMD	45.2.1.4		PMA:O	Yes [ ] No [ ]
*10G	Implementation of 10 Gb/s PMA/PMD	45.2.1.4		PMA:O	Yes [ ] No [ ]
10XR	Implementation of 10GPASS-XR PMA/PMD	45.2.1.4		PMA:O	Yes [ ] No [ ]
*KX	Implementation of 1000BASE-KX PMA/PMD	45.2.1.6		PMA:O	Yes [ ] No [ ]
*KX4	Implementation of 10GBASE-KX4 PMA/PMD	45.2.1.6		PMA:O	Yes [ ] No [ ]
*KR	Implementation of 10GBASE-KR PMA/PMD	45.2.1.6		PMA:O	Yes [ ] No [ ]
*PXAR	Implementation of PMA/PMD Extended Ability register	45.2.1.10	Required for certain abilities	PMA:O	Yes [ ] No [ ]
*40XAR	Implementation of 40G/100G PMA/PMD Extended Ability register	45.2.1.12	Required for certain abilities	PMA:O	Yes [ ] No [ ]
10XRAR	Implementation of EPoC PMA/PMD ability register	45.2.1.15		PMA:O	Yes [ ] No [ ]
*MMD8	Implementation of separately addressable instance, address 8	45.2.1	All register definitions as for address 1	PMA:O	Yes [ ] No [ ]
*MMD9	Implementation of separately addressable instance, address 9	45.2.1	All register definitions as for address 1	PMA:O	Yes [ ] No [ ]
*MMD10	Implementation of separately addressable instance, address 10	45.2.1	All register definitions as for address 1	PMA:O	Yes [ ] No [ ]
*MMD11	Implementation of separately addressable instance, address 11	45.2.1	All register definitions as for address 1	PMA:O	Yes [ ] No [ ]
*FEC-R	Implementation of BASE-R FEC	45.2.1.107		PMA:O	Yes [ ] No [ ]
*RS-FEC	Implementation of RS-FEC	45.2.1.117		PMA:O	Yes [ ] No [ ]
*BH	Implementation of a BASE-H PMA/PMD			PMA:O	Yes [ ] No [ ]

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45.5.3.3 PMA/PMD management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MM1	Device responds to all register addresses for that device	45.2		PMA:M	Yes [ ] N/A [ ]
MM2	Writes to undefined and read-only registers have no effect	45.2		PMA:M	Yes [ ] N/A [ ]
MM3	Operation is not affected by writes to reserved and unsupported bits.	45.2		PMA:M	Yes [ ] N/A [ ]
MM4	Reserved and unsupported bits return a value of zero	45.2		PMA:M	Yes [ ] N/A [ ]
MM5	Latching low bits remain low until after they have been read via the management interface	45.2		PMA:M	Yes [ ] N/A [ ]
MM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PMA:M	Yes [ ] N/A [ ]
MM7	Latching high bits remain high until after they have been read via the management interface	45.2		PMA:M	Yes [ ] N/A [ ]
MM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PMA:M	Yes [ ] N/A [ ]
MM9	Action on reset	45.2.1.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PMA:M	Yes [ ] N/A [ ]
MM10	Return 1 until reset completed	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM11	Control and management interfaces are restored to operation within 0.5 s of reset	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM12	Responds to reads of bit 15 and 1.8.15:14 during reset	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM13	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.1.1.2		PMA:M	Yes [ ] N/A [ ]
MM14	Invalid writes to speed selection bits are ignored	45.2.1.1.3		PMA:M	Yes [ ] N/A [ ]
MM15	PMA is set into local loopback mode when bit 0 is set to a one	45.2.1.1.5		ALB:M	Yes [ ] N/A [ ]
MM16	PMA transmit data is returned on receive path when in local loopback	45.2.1.1.5		ALB:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MM17	PMA ignores writes to this bit if it does not support local loopback.	45.2.1.1.5		PMA*!ALB:M	Yes [ ] N/A [ ]
MM18	PMA returns a value of zero when read if it does not support local loopback.	45.2.1.1.5		PMA*!ALB:M	Yes [ ] N/A [ ]
MM19	PMA is set into remote loopback mode when bit 1 is set to a one	45.2.1.1.4		RLB:M	Yes [ ] N/A [ ]
MM20	PMA receive data is returned on transmit path when in remote loopback	45.2.1.1.4		RLB:M	Yes [ ] N/A [ ]
MM21	PMA ignores writes to this bit if it does not support remote loopback.	45.2.1.1.4		PMA*!RLB:M	Yes [ ] N/A [ ]
MM22	PMA returns a value of zero when read if it does not support remote loopback.	45.2.1.1.4		PMA*!RLB:M	Yes [ ] N/A [ ]
MM23	Writes to status 1 register have no effect	45.2.1.2		PMA:M	Yes [ ] N/A [ ]
MM24	Receive link status implemented with latching low behavior	45.2.1.2.4		PMA:M	Yes [ ] N/A [ ]
MM25	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.1.3		PMA:M	Yes [ ] N/A [ ]
MM26	PMA/PMD type is selected using bits 5:0	45.2.1.6.3		PMA:M	Yes [ ] N/A [ ]
MM27	PMA/PMD ignores writes to type selection bits that select types that it has not advertised	45.2.1.6.3		PMA:M	Yes [ ] N/A [ ]
MM28	Writes to the status 2 register have no effect	45.2.1.7		PMA:M	Yes [ ] N/A [ ]
MM29	PMA/PMD returns a value of zero for transmit fault if it is unable to detect a transmit fault	45.2.1.7.4		PMA:M	Yes [ ] N/A [ ]
MM30	Transmit fault is implemented using latching high behavior	45.2.1.7.4		PMA*PLF:M	Yes [ ] N/A [ ]
MM31	PMA/PMD returns a value of zero for receive fault if it is unable to detect a receive fault	45.2.1.7.5		PMA*!PLF:M	Yes [ ] N/A [ ]
MM32	Receive fault is implemented using latching high behavior	45.2.1.7.5		PMA*PLF:M	Yes [ ] N/A [ ]
MM33	Writes to register 9 are ignored by device that does not implement transmit disable	45.2.1.8		PMA*!PTD:M	Yes [ ] N/A [ ]
MM34	Single wavelength device uses bit 1.9.0 for transmit disable	45.2.1.8		PMA*PTD:M	Yes [ ] N/A [ ]

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MM35	Single wavelength device ignores writes to bits 10:1 and returns a value of zero for them	45.2.1.8		PTD:M	Yes [ ] N/A [ ]
MM36	Bits 1 to 10, set to one disables transmission on corresponding lane	45.2.1.8		PTD:M	Yes [ ] No [ ] N/A [ ]
MM37	Bits 1 to 10, set to zero enables transmission on corresponding lane	45.2.1.8		PTD:M	Yes [ ] No [ ] N/A [ ]
MM38	Setting bit 0 to a one disables transmission	45.2.1.8.7		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM39	Setting bit 0 to a zero enables transmission	45.2.1.8.7	Only if all lane transmit disables are zero	PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM40	Receive signal detect register behaves as described	45.2.1.9		PMA:M	Yes [ ] N/A [ ]
MM41	Writes to the extended ability register have no effect	45.2.1.10		PMA:M	Yes [ ] N/A [ ]
MM42	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.1.11		PMA:M	Yes [ ] N/A [ ]
MM43	Writes to the 40G/100G PMA/PMD extended ability register have no effect	45.2.1.12		PMA:M	Yes [ ] N/A [ ]
MM44	Bit indicates link down while initializing	45.2.1.2.4		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM45	Bit remains a one and writing a one is ignored when link is up or initializing	45.2.1.11		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM46	PRBS pattern testing implemented	45.2.1.169	Ability indicated in register 1.1500	PMA:O	Yes [ ] N/A [ ]
MM47	Square wave testing implemented	45.2.1.169	Bit 1.1500.12 is set to one	PMA:O	Yes [ ] N/A [ ]
MM48	Counters corresponding to lanes that are not implemented return all zeros	45.2.1.173		MM46:M	Yes [ ] N/A [ ]
MM49	Counters are reset to zero by read or PMA reset	45.2.1.173		MM46:M	Yes [ ] N/A [ ]
MM50	Counters are held at all ones in the case of overflow	45.2.1.173		MM46:M	Yes [ ] N/A [ ]
MM51	Bit set to zero upon reset or upon link down	45.2.1.28.1	-O subtypes only	PMA*10P*2B:M	Yes [ ] N/A [ ]
MM52	Bit set to one upon reset or upon link down	45.2.1.28.1	-R subtypes only	PMA*10P*2B:M	Yes [ ] N/A [ ]
MM53	Handshake tones not sent while bit is set to zero	45.2.1.28.1		PMA*10P*2B:M	Yes [ ] N/A [ ]

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MM54	Writes to set unsupported modes or when link is not down are ignored	45.2.1.28.4		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM55	Setting bit to one to one issues a cleardown command	45.2.1.28.5		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM56	MMD clears bit to zero when cleardown command is issued or on reset	45.2.1.28.5		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM57	Writes ignored if link is not in “Link down (ready)” state	45.2.1.28.5	Link state described in 45.2.1.29.4	PMA*10P*2B:M	Yes [ ] N/A [ ]
MM58	PMA/PMD does not respond to handshake tones while bit is set to one	45.2.1.28.6		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM59	PMA/PMD responds to handshake tones properly when bit is set to zero	45.2.1.28.6		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM60	Bit set to zero upon MMD reset	45.2.1.28.6		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM61	Writes to set unsupported modes are ignored	45.2.1.28.7		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM62	Bits zero when link is down or initializing	45.2.1.29.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM63	Bits set indicate linked port type or link status	45.2.1.29.4		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM64	Bits indicate 001 while link is initializing	45.2.1.29.4		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM65	Bits indicate 000 when link is down and handshake tones are not detected	45.2.1.29.4		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM66	Bits indicate 100 when link is down and handshake tones are detected	45.2.1.29.4		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM67	Bit held as one during operation, clears to zero after	45.2.1.30.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM68	Result = failed after 10 second timeout	45.2.1.30.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM69	Writes to one while link is down are marked completed and failed	45.2.1.30.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM70	Bit held as one during operation, clears to zero after	45.2.1.30.2		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM71	Result = failed after 10 second timeout	45.2.1.30.2		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM72	Writes to one while link is down are marked completed and failed	45.2.1.30.2		PMA*10P*2B:M	Yes [ ] N/A [ ]

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MM73	Bit set to result of the “Get” operation	45.2.1.31.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM74	Bit set to zero on read or reset	45.2.1.31.1		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM75	Bit set to result of the “Send” operation	45.2.1.31.2		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM76	Bits are reset to zero when read or on reset	45.2.1.34		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM77	Bits are held to all ones upon counter overflow	45.2.1.34		PMA*10P*2B:M	Yes [ ] N/A [ ]
MM78	Bits are reset to zero when read or reset	45.2.1.41		PMA*10P:M	Yes [ ] N/A [ ]
MM79	Bits are reset to zero when read or reset	45.2.1.42		PMA*10P:M	Yes [ ] N/A [ ]
MM80	Bits are held at all ones when PHY cannot determine value	45.2.1.45.1	ex: While link is down	PMA*10P:M	Yes [ ] N/A [ ]
MM81	Bit remain as one while tones are being refreshed	45.2.1.55.1		PMA*10P:M	Yes [ ] N/A [ ]
MM82	Bit set to zero when operation completes or upon reset	45.2.1.55.1		PMA*10P:M	Yes [ ] N/A [ ]
MM83	Bit remain as one while tones are being activated/deactivated	45.2.1.55.2		PMA*10P:M	Yes [ ] N/A [ ]
MM84	Bit set to zero when operation completes or upon reset	45.2.1.55.2		PMA*10P:M	Yes [ ] N/A [ ]
MM85	Bit remain as one while tone direction is being changed	45.2.1.55.3		PMA*10P:M	Yes [ ] N/A [ ]
MM86	Bit set to zero when operation completes or upon reset	45.2.1.55.3		PMA*10P:M	Yes [ ] N/A [ ]
MM87	Bit remain as one while SNR margins parameters are loaded	45.2.1.55.4		PMA*10P:M	Yes [ ] N/A [ ]
MM88	Bit set to zero when operation completes or upon reset	45.2.1.55.4		PMA*10P:M	Yes [ ] N/A [ ]
MM89	Bit remain as one while PSD level is set	45.2.1.55.5		PMA*10P:M	Yes [ ] N/A [ ]
MM90	Bit set to zero when operation completes or upon reset	45.2.1.55.5		PMA*10P:M	Yes [ ] N/A [ ]
MM91	Bit remain as one while reference PSD level is set	45.2.1.55.6		PMA*10P:M	Yes [ ] N/A [ ]
MM92	Bit set to zero when operation completes or upon reset	45.2.1.55.6		PMA*10P:M	Yes [ ] N/A [ ]
MM93	Bits are reset to zero when read or upon reset	45.2.1.56.1		PMA*10P:M	Yes [ ] N/A [ ]
MM94	Bits read as zero	45.2.1.57.6		PMA*10P:M	Yes [ ] N/A [ ]

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MM95	Bits read as zero	45.2.1.57.7		PMA*10P:M	Yes [ ] N/A [ ]
MM96	Writes to an invalid value are ignored	45.2.1.59	Valid values are decimal 10, 20, or 40	PMA*10P:M	Yes [ ] N/A [ ]
MM97	Bits set to default value on MMD reset	45.2.1.59	Default value is decimal 20	PMA*10P:M	Yes [ ] N/A [ ]
MM98	Writes to set an invalid value are ignored	45.2.1.62.1	Valid values are decimal 3 through 89	PMA*10P:M	Yes [ ] N/A [ ]
MM99	Writes to set an invalid value are ignored	45.2.1.62.2	Valid values are decimal 3 through 89	PMA*10P:M	Yes [ ] N/A [ ]
MM100	Writes to set an invalid value are ignored	45.2.1.62.3	Valid values are decimal 1 through 86	PMA*10P:M	Yes [ ] N/A [ ]
MM101	Writes to set an invalid value are ignored	45.2.1.62.5	Invalid value is 11	PMA*10P:M	Yes [ ] N/A [ ]
MM102	Bits set to zero when read or reset	45.2.1.63		PMA*2B:M	Yes [ ] N/A [ ]
MM103	Bits set to zero when read or reset	45.2.1.65		PMA*2B:M	Yes [ ] N/A [ ]
MM104	Bits set to zero when read or reset	45.2.1.67		PMA*2B:M	Yes [ ] N/A [ ]
MM105	Bits set to zero when read or reset	45.2.1.69		PMA*2B:M	Yes [ ] N/A [ ]
MM106	Bits set to zero when read or reset	45.2.1.71		PMA*2B:M	Yes [ ] N/A [ ]
MM107	Writes to set an invalid value are ignored	45.2.1.76.1	Valid values are decimal 3 through 89	PMA*10P:M	Yes [ ] N/A [ ]
MM108	Writes to set an invalid value are ignored	45.2.1.76.2	Valid values are decimal 3 through 89	PMA*10P:M	Yes [ ] N/A [ ]
MM109	Writes to set an invalid value are ignored	45.2.1.76.3	Valid values are decimal 1 through 86	PMA*10P:M	Yes [ ] N/A [ ]
MM110	Writes to set an invalid value are ignored	45.2.1.76.5	Invalid value is 11	PMA*10P:M	Yes [ ] N/A [ ]
MM111	Bit set to zero if PMA link_status=FAIL	45.2.1.77.1		PMA*2.5T:M PMA*5T:M PMA*10T:M PMA*25T:M PMA*40T:M	Yes [ ] N/A [ ]
MM112	Skew delay register update rate.	45.2.1.93	At least once per second	PMA*2.5T:M PMA*5T:M PMA*10T:M PMA*25T:M PMA*40T:M	Yes [ ] N/A [ ]
MM113	A PMA/PMD that is unable to detect a transmit fault returns a value of zero for the transmit fault bit.	45.2.1.104.3		KX:M	Yes [ ] N/A [ ]

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MM114	The transmit fault bit is implemented with latching high behavior.	45.2.1.104.3		KX:M	Yes [ ] N/A [ ]
MM115	A PMA/PMD that is unable to detect a receive fault returns a value of zero for the receive fault bit.	45.2.1.104.4		KX:M	Yes [ ] N/A [ ]
MM116	The receive fault bit is implemented with latching high behavior.	45.2.1.104.4		KX:M	Yes [ ] N/A [ ]
MM117	FEC enable is set to zero upon execution of PHY reset	45.2.1.108.1		FEC-R:M	Yes [ ] N/A [ ]
MM118	RS-FEC counters are reset when read or upon PHY reset.	45.2.1.118, 45.2.1.119, 45.2.1.120, 45.2.1.122, 45.2.1.123, 45.2.1.124		RS-FEC:M	Yes [ ] N/A [ ]
MM119	RS-FEC counters are held at all ones in the case of overflow	45.2.1.118, 45.2.1.119, 45.2.1.120, 45.2.1.122, 45.2.1.123, 45.2.1.124		RS-FEC:M	Yes [ ] N/A [ ]
MM120	FEC corrected blocks counters are reset when read or upon PHY reset.	45.2.1.109, 45.2.1.131		FEC-R:M	Yes [ ] N/A [ ]
MM121	FEC corrected blocks counters are held at all ones in the case of overflow	45.2.1.109, 45.2.1.131		FEC-R:M	Yes [ ] N/A [ ]
MM122	FEC uncorrected blocks counters are reset when read or upon PHY reset.	45.2.1.110, 45.2.1.149		FEC-R:M	Yes [ ] N/A [ ]
MM123	FEC uncorrected blocks counters are held at all ones in the case of overflow	45.2.1.110, 45.2.1.149		FEC-R:M	Yes [ ] N/A [ ]
MM124	Backplane Ethernet AN ability bit is set to one for 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR,10GBASE-KX4 and 10GBASE-KR PHYs.	45.2.7.12.4		KX:M 2.5GKX:M 5GKR:M KX4:M KR:M	Yes [ ] N/A [ ]
MM125	Writes to this register have no effect	45.2.1.11		PMA:M	Yes [ ] N/A [ ]
MM126	Writes to the BASE-T1 PMA/PMD extended ability register have no effect	45.2.1.16		PMA:M	Yes [ ] N/A [ ]
MM127	BASE-T1 MASTER config	45.2.1.214.1	PHY operates as MASTER when bit 1.2100.14 is set to one	BTC:M	Yes [ ] N/A [ ]

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MM128	BASE-T1 SLAVE config	45.2.1.214.1	PHY operates as SLAVE when bit 1.2100.14 is set to zero	BTC:M	Yes [ ] N/A [ ]
MM129	EEE deep sleep capability indicated for each port type	45.2.1.14		EEE:M	Yes [ ] N/A [ ]
MM130	A reset sets all 1000BASE-T1 PMA/PMD registers to their default states	45.2.1.237.1		PMA:M	Yes [ ] N/A [ ]
MM131	1000BASE-T1 PMA/PMD returns a one in bit 1.2304.15 when a reset is in progress	45.2.1.237.1		PMA:M	Yes [ ] N/A [ ]
MM132	1000BASE-T1 PMA/PMD returns a zero in bit 1.2304.15 when a reset is complete	45.2.1.237.1		PMA:M	Yes [ ] N/A [ ]
MM133	During a reset, the 1000BASE-T1 PMD/PMA responds to reads from register bits 1.2304.15, 1.8.15:14, and 1.0.15.	45.2.1.237.1		PMA:M	Yes [ ] N/A [ ]
MM134	During a reset, the 1000BASE-T1 PMD/PMA register bits are ignored.	45.2.1.237.1		PMA:M	Yes [ ] N/A [ ]
MM135	Setting either 1.2304.15 or 1.0.15 resets the 1000BASE-T1 PMA/PMD.	45.2.1.237.1		PMA:M	Yes [ ] N/A [ ]
MM136	When bit 1.2304.14 is set to a one, the PMA disables output on the transmit path.	45.2.1.237.2		PMA:M	Yes [ ] N/A [ ]
MM137	When bit 1.2304.14 is set to a zero, the PMA enables output on the transmit path.	45.2.1.237.2		PMA:M	Yes [ ] N/A [ ]
MM138	Setting either bit 1.2304.14 or 1.9.0 disables the 1000BASE-T1 PMA transmit path.	45.2.1.237.2		PMA:M	Yes [ ] N/A [ ]
MM139	While in the low-power mode, the device, as a minimum, responds to management transactions necessary to exit the low-power mode.	45.2.1.237.3		PMA:M	Yes [ ] N/A [ ]
MM140	Setting either 1.2304.11 or 1.0.11 puts the 1000BASE-T1 PMA/PMD in low-power mode.	45.2.1.237.3		PMA:M	Yes [ ] N/A [ ]
MM141	The 1000BASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path returns a value of zero for bit 1.2305.1.	45.2.1.238.6		PMA:M	Yes [ ] N/A [ ]

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MM142	Bit 1.2305.0 is implemented with latching low behavior.	45.2.1.238.6		PMA:M	Yes [ ] N/A [ ]
MM143	Bit 1.2306.1 is set to zero if the 1000BASE-T1 PHY does not support OAM.	45.2.1.239.2		PMA:M	Yes [ ] N/A [ ]
MM144	Bit 1.2306.0 is set to zero if the 1000BASE-T1 PHY does not support EEE.	45.2.1.239.3		PMA:M	Yes [ ] N/A [ ]
MM145	OAM capability is enabled only when both the 1000BASE-T1 PHY and link partner are advertising OAM capability.	45.2.1.240.2		PMA:M	Yes [ ] N/A [ ]
MM146	EEE capability is enabled only when both the 1000BASE-T1 PHY and link partner are advertising EEE capability	45.2.1.240.3		PMA:M	Yes [ ] N/A [ ]
MM147	Bit 1.2100.14 is ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.	45.2.1.214.1		PMA:M	Yes [ ] N/A [ ]
MM148	Bits 1.2100.3:0 is ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.	45.2.1.214.2		PMA:M	Yes [ ] N/A [ ]
MM149	Writes to the register 1.22 have no effect	45.2.1.20		PMA:O	Yes [ ] No [ ] N/A [ ]
MM150	Writes of reserved values or modes of operation different of those advertised by register 1.22, to bits 1.900.3:0 have no effect	45.2.1.158		BH:M	Yes [ ] N/A [ ]
MM151	Bits 1.2100.3:0 are ignored when Auto-Negotiation enable bit 7.512.12 is set to one	45.2.1.214.2		PMA:M	Yes [ ] N/A [ ]
MM152	A reset sets all 10BASE-T1L PMA registers to their default states	45.2.1.231.1		PMA:M	Yes [ ] N/A [ ]
MM153	10BASE-T1L PMA returns a one in bit 1.2294.15 when a reset is in progress; otherwise, it returns a value of zero	45.2.1.231.1		PMA:M	Yes [ ] N/A [ ]
MM154	The control and management interface is restored to operation within 0.5 s from the setting of bit 1.2294.15	45.2.1.231.1		PMA:M	Yes [ ] N/A [ ]
MM155	During a reset, the 10BASE-T1L PMA responds to reads from register bits 1.2294.15, 1.8.15:14, and 1.0.15	45.2.1.231.1		PMA:M	Yes [ ] N/A [ ]

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MM156	Setting either 1.2294.15 or 1.0.15 sets the other	45.2.1.231.1		PMA:M	Yes [ ] N/A [ ]
MM157	Clearing either 1.2294.15 or 1.0.15 clears the other	45.2.1.231.1		PMA:M	Yes [ ] N/A [ ]
MM158	Setting either 1.2294.15 or 1.0.15 resets the 10BASE-T1L PMA	45.2.1.231.1		PMA:M	Yes [ ] N/A [ ]
MM159	When bit 1.2294.14 is set to one, the 10BASE-T1L PMA disables output on the transmit path	45.2.1.231.2		PMA:M	Yes [ ] N/A [ ]
MM160	When bit 1.2294.14 is set to zero, the 10BASE-T1L PMA enables output on the transmit path	45.2.1.231.2		PMA:M	Yes [ ] N/A [ ]
MM161	Setting either 1.2294.14 or 1.9.0 sets the other	45.2.1.231.2		PMA:M	Yes [ ] N/A [ ]
MM162	Clearing either 1.2294.14 or 1.9.0 clears the other	45.2.1.231.2		PMA:M	Yes [ ] N/A [ ]
MM163	Setting either 1.2294.14 or 1.9.0 disables the transmitter	45.2.1.231.2		PMA:M	Yes [ ] N/A [ ]
MM164	10BASE-T1L Transmit voltage amplitude control when Auto-Negotiation is not implemented or is not enabled	45.2.1.231.3	1 = 10BASE-T1L PMA transmits using 2.4 Vpp operating mode 0 = 10BASE-T1L PMA transmits using 1.0 Vpp operating mode	PMA:M	Yes [ ] N/A [ ]
MM165	When Auto-Negotiation is implemented and enabled, setting bit 1.2294.12 has no effect	45.2.1.231.3		PMA:M	Yes [ ] N/A [ ]
MM166	While in low-power mode, the device responds to management transactions necessary to exit the low-power mode	45.2.1.231.4		PMA:M	Yes [ ] N/A [ ]
MM167	Setting either 1.2294.11 or 1.0.11 sets the other	45.2.1.231.4		PMA:M	Yes [ ] N/A [ ]
MM168	Clearing either 1.2294.11 or 1.0.11 clears the other	45.2.1.231.4		PMA:M	Yes [ ] N/A [ ]
MM169	Setting either 1.2294.11 or 1.0.11 puts the 10BASE-T1L PMA in low-power mode	45.2.1.231.4		PMA:M	Yes [ ] N/A [ ]
MM170	10BASE-T1L EEE functionality when Auto-Negotiation is not implemented or is not enabled	45.2.1.231.5	1 = PHY operates with EEE enabled 0 = PHY operates with EEE disabled	PMA:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MM171	When Auto-Negotiation is implemented and enabled, setting bit 1.2294.10 has no effect	45.2.1.231.5		PMA:M	Yes [ ] N/A [ ]
MM172	When bit 1.2294.0 is set to one, the 10BASE-T1L PMA is placed into near-end loopback mode, and it accepts data on the transmit path and returns it on the receive path	45.2.1.231.6		PMA:M	Yes [ ] N/A [ ]
MM173	Setting either 1.2294.0 or 1.0.0 sets the other	45.2.1.231.6		PMA:M	Yes [ ] N/A [ ]
MM174	Clearing either 1.2294.0 or 1.0.0 clears the other	45.2.1.231.6		PMA:M	Yes [ ] N/A [ ]
MM175	Setting either 1.2294.0 or 1.0.0 enables loopback	45.2.1.231.6		PMA:M	Yes [ ] N/A [ ]
MM176	The 10BASE-T1L PMA that is unable to detect a fault condition on the receive path returns a value of zero for bit 1.2295.1	45.2.1.232.7		PMA:M	Yes [ ] N/A [ ]
MM177	The 10BASE-T1L PMA receive fault bit is implemented with latching high behavior	45.2.1.232.7		PMA:M	Yes [ ] N/A [ ]
MM178	The 10BASE-T1L PMA receive link status bit is implemented with latching low behavior	45.2.1.232.8		PMA:M	Yes [ ] N/A [ ]
MM179	A reset sets all 10BASE-T1S PMA registers to their default states	45.2.1.234.1		PMA:M	Yes [ ] N/A [ ]
MM180	10BASE-T1S PMA returns a one in bit 1.2297.15 when a reset is in progress; otherwise, it returns a value of zero	45.2.1.234.1		PMA:M	Yes [ ] N/A [ ]
MM181	The control and management interface is restored to operation within 0.5 s from the setting of bit 1.2297.15	45.2.1.234.1		PMA:M	Yes [ ] N/A [ ]
MM182	During a reset, the 10BASE-T1S PMA responds to reads from register bits 1.2297.15, 1.8.15:14, and 1.0.15	45.2.1.234.1		PMA:M	Yes [ ] N/A [ ]
MM183	Setting either 1.2297.15 or 1.0.15 sets the other	45.2.1.234.1		PMA:M	Yes [ ] N/A [ ]
MM184	Clearing either 1.2297.15 or 1.0.15 clears the other	45.2.1.234.1		PMA:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MM185	Setting either 1.2297.15 or 1.0.15 resets the 10BASE-T1S PMA	45.2.1.234.1		PMA:M	Yes [ ] N/A [ ]
MM186	When bit 1.2297.14 is set to one, the 10BASE-T1S PMA disables output on the transmit path	45.2.1.234.2		PMA:M	Yes [ ] N/A [ ]
MM187	When bit 1.2297.14 is set to zero, the 10BASE-T1S PMA enables output on the transmit path	45.2.1.234.2		PMA:M	Yes [ ] N/A [ ]
MM188	Setting either 1.2297.14 or 1.0.14 sets the other	45.2.1.234.2		PMA:M	Yes [ ] N/A [ ]
MM189	Clearing either 1.2297.14 or 1.0.14 clears the other	45.2.1.234.2		PMA:M	Yes [ ] N/A [ ]
MM190	Setting either 1.2297.14 or 1.0.14 disables the transmitter	45.2.1.234.2		PMA:M	Yes [ ] N/A [ ]
MM191	While in low-power mode, the device responds to management transactions necessary to exit the low-power mode	45.2.1.234.3		PMA:M	Yes [ ] N/A [ ]
MM192	Setting either 1.2297.11 or 1.0.11 sets the other	45.2.1.234.3		PMA:M	Yes [ ] N/A [ ]
MM193	Clearing either 1.2297.11 or 1.0.11 clears the other	45.2.1.234.3		PMA:M	Yes [ ] N/A [ ]
MM194	Setting either 1.2297.11 or 1.0.11 puts the 10BASE-T1S PMA in low-power mode	45.2.1.234.3		PMA:M	Yes [ ] N/A [ ]
MM195	When bit 1.2297.10 is set to one, the 10BASE-T1S PMA is configured to operate in multidrop mode	45.2.1.234.4		PMA:M	Yes [ ] N/A [ ]
MM196	If multidrop mode is not supported according to bit 1.2298.10, writing to bit 1.2297.10 has no effect, and the PCS operates in half duplex mode with bits 3.2291.8 and 0.8 set to one	45.2.1.234.4		PMA:M	Yes [ ] N/A [ ]
MM197	When bit 1.2297.0 is set to one, the 10BASE-T1S PMA is placed into loopback mode, and it accepts data on the transmit path and returns it on the receive path	45.2.1.234.5		PMA:M	Yes [ ] N/A [ ]
MM198	Setting either 1.2297.0 or 1.0.0 sets the other	45.2.1.234.5		PMA:M	Yes [ ] N/A [ ]
MM199	Clearing either 1.2297.0 or 1.0.0 clears the other	45.2.1.234.5		PMA:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MM200	Setting either 1.2297.0 or 1.0.0 enables loopback	45.2.1.234.5		PMA:M	Yes [ ] N/A [ ]
MM201	The 10BASE-T1S PMA that is unable to detect a fault condition on the receive path returns a value of zero for bit 1.2298.1	45.2.1.235.5		PMA:M	Yes [ ] N/A [ ]
MM202	The 10BASE-T1S PMA receive fault bit is implemented with latching high behavior	45.2.1.235.5		PMA:M	Yes [ ] N/A [ ]
MM203	Setting bit 1.2309.15 sets all MultiGBASE-T1 PMA/PMD registers to their default states.	45.2.1.242.1		PMA:M	Yes [ ] N/A [ ]
MM204	The MultiGBASE-T1 PMA/PMD returns a value of one in bit 1.2309.15 when a reset is in progress.	45.2.1.242.1		PMA:M	Yes [ ] N/A [ ]
MM205	The MultiGBASE-T1 PMA/PMD returns a value of zero in bit 1.2309.15 when a reset is complete.	45.2.1.242.1		PMA:M	Yes [ ] N/A [ ]
MM206	During a reset, the MultiGBASE-T1 PMA/PMD responds to reads from register bits 1.2309.15, 1.8.15:14, and 1.0.15.	45.2.1.242.1		PMA:M	Yes [ ] N/A [ ]
MM207	During a reset, all MultiGBASE-T1 PMA/PMD register bits are ignored.	45.2.1.242.1		PMA:M	Yes [ ] N/A [ ]
MM208	Setting or clearing either bit 1.2309.15 or 1.0.15 sets or clears the other bit.	45.2.1.242.1		PMA:M	Yes [ ] N/A [ ]
MM209	Setting either bit 1.2309.15 or 1.0.15 resets the MultiGBASE-T1 PMA/PMD.	45.2.1.242.1		PMA:M	Yes [ ] N/A [ ]
MM210	When bit 1.2309.14 is set to a one, the PMA disables output on the transmit path.	45.2.1.242.2		PMA:M	Yes [ ] N/A [ ]
MM211	When bit 1.2309.14 is zero, the PMA enables output on the transmit path.	45.2.1.242.2		PMA:M	Yes [ ] N/A [ ]
MM212	Setting or clearing either bit 1.2309.14 or 1.0.14 sets or clears the other bit.	45.2.1.242.2		PMA:M	Yes [ ] N/A [ ]
MM213	Setting either bit 1.2309.14 or 1.0.14 disables the MultiGBASE-T1 transmit path.	45.2.1.242.2		PMA:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MM214	While in low-power mode, the device, at a minimum, responds to management transactions necessary to exit the low-power mode.	45.2.1.242.3		PMA:M	Yes [ ] N/A [ ]
MM215	Setting or clearing either bit 1.2309.11 or 1.0.11 sets or clears the other bit.	45.2.1.242.3		PMA:M	Yes [ ] N/A [ ]
MM216	Setting either bit 1.2309.11 or 1.0.11 puts the MultiGBASE-T1 PMA/PMD in low-power mode.	45.2.1.242.3		PMA:M	Yes [ ] N/A [ ]
MM217	A MultiGBASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path returns a value of zero for bit 1.2310.1.	45.2.1.243.7		PMA:M	Yes [ ] N/A [ ]
MM218	The receive fault bit (1.2310.1) is implemented with latching high behavior.	45.2.1.243.7		PMA:M	Yes [ ] N/A [ ]
MM219	The link status bit (1.2310.0) is implemented with latching low behavior.	45.2.1.243.8		PMA:M	Yes [ ] N/A [ ]
MM220	When bit 1.2311.5 is set to a one, the PHY uses 1.23.11.3:2 for the value of PrecodeSel.	45.2.1.244.2		PMA:M	Yes [ ] N/A [ ]
MM221	When bit 1.2311.5 is set to a zero, the PHY controls the value of PrecodeSel.	45.2.1.244.2		PMA:M	Yes [ ] N/A [ ]
MM222	Advertisement of support for MultiGBASE-T1 OAM.	45.2.1.244.5	Support is advertised if bit 1.2311.1 is set to one, and not advertised if bit 1.2311.1 is set to zero.	PMA:M	Yes [ ] N/A [ ]
MM223	Advertisement of support for MultiGBASE-T1 EEE.	45.2.1.244.6	Support is advertised if bit 1.2311.0 is set to one, and not advertised if bit 1.2311.0 is set to zero.	PMA:M	Yes [ ] N/A [ ]
MM224	OAM capability is enabled only when both the local PHY and its link partner are advertising OAM capability.	45.2.1.245.4		PMA:M	Yes [ ] N/A [ ]
MM225	EEE capability is enabled only when both the local PHY and its link partner are advertising EEE capability.	45.2.1.245.5		PMA:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MM226	When bit 1.2313.11 is set to one, the local transmitter's precoder shall be controlled by the value of bits 1.2313.10:9, and the precoder requested by the link partner in PrecodeSel shall be ignored.	45.2.1.246.2		PMA:M	Yes [ ] N/A [ ]
MM227	When bit 1.2313.11 is set to zero, the transmitter shall ignore bits 1.2313.10:9, and the precoder is set according to the value of PrecodeSel.	45.2.1.246.2		PMA:M	Yes [ ] N/A [ ]
MM228	PMA/PMD type selection	45.2.1.27.2	Device ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised	M	Yes [ ]

45.5.3.4 WIS options

Item	Feature	Subclause	Value/Comment	Status	Support
*WPT	Implementation of PRBS31 pattern testing	45.2.2		WIS:O	Yes [ ] No [ ] N/A [ ]

45.5.3.5 WIS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
WM1	Device responds to all register addresses for that device	45.2		WIS:M	Yes [ ] N/A [ ]
WM2	Writes to undefined and read-only registers have no effect	45.2		WIS:M	Yes [ ] N/A [ ]
WM3	Operation is not affected by writes to reserved and unsupported bits.	45.2		WIS:M	Yes [ ] N/A [ ]
WM4	Reserved and unsupported bits return a value of zero	45.2		WIS:M	Yes [ ] N/A [ ]
WM5	Latching low bits remain low until after they have been read via the management interface	45.2		WIS:M	Yes [ ] N/A [ ]
WM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	WIS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
WM7	Latching high bits remain high until after they have been read via the management interface	45.2		WIS:M	Yes [ ] N/A [ ]
WM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	WIS:M	Yes [ ] N/A [ ]
WM9	Action on reset	45.2.2.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	WIS:M	Yes [ ] N/A [ ]
WM10	Return 1 until reset completed	45.2.2.1.1		WIS:M	Yes [ ] N/A [ ]
WM11	Reset completes within 0.5 s	45.2.2.1.1		WIS:M	Yes [ ] N/A [ ]
WM12	Responds to reads of bits 2.0.15 and 2.8.15:14 during reset	45.2.2.1.1		WIS:M	Yes [ ] N/A [ ]
WM13	Loopback mode	45.2.2.1.2	Whenever bit 2.0.14 is set to a one	WIS:M	Yes [ ] N/A [ ]
WM14	Data received from PMA ignored during loopback	45.2.2.1.2		WIS:M	Yes [ ] N/A [ ]
WM15	Transmit data returned on receive path during loopback	45.2.2.1.2		WIS:M	Yes [ ] N/A [ ]
WM16	Device responds to transactions necessary to exit low-power mode while in low- power state	45.2.2.1.3		WIS:M	Yes [ ] N/A [ ]
WM17	Speed selection bits 13 and 6 are written as one	45.2.2.1.4		WIS:M	Yes [ ] N/A [ ]
WM18	Invalid writes to speed selection bits are ignored	45.2.2.1.4		WIS:M	Yes [ ] N/A [ ]
WM19	Writes to status 1 register have no effect	45.2.2.2		WIS:M	Yes [ ] N/A [ ]
WM20	Fault bit implemented using latching high behavior	45.2.2.2.1		WIS:M	Yes [ ] N/A [ ]
WM21	Link status bit implemented using latching low behavior	45.2.2.2.2		WIS:M	Yes [ ] N/A [ ]
WM22	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.2.3		WIS:M	Yes [ ] N/A [ ]
WM23	Setting bit 2.7.5 to a one enables PRBS31 receive pattern testing if bit 2.8.1 is a one and bit 2.7.2 is not a one	45.2.2.6.1		WIS* WPT:M	Yes [ ] N/A [ ]
WM24	Setting bit 2.7.5 to a zero disables PRBS31 receive pattern testing	45.2.2.6.1		WIS* WPT:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
WM25	Setting bit 2.7.4 to a one enables PRBS31 transmit pattern testing if bit 2.8.1 is a one and bit 2.7.1 is not a one	45.2.2.6.2		WIS* WPT:M	Yes [ ] N/A [ ]
WM26	Setting bit 2.7.4 to a zero disables PRBS31 transmit pattern testing	45.2.2.6.2		WIS* WPT:M	Yes [ ] N/A [ ]
WM27	Setting bit 3 to one selects the square wave test pattern	45.2.2.6.3		WIS:M	Yes [ ] N/A [ ]
WM28	Setting bit 3 to zero selects the pseudo random test pattern	45.2.2.6.3		WIS:M	Yes [ ] N/A [ ]
WM29	Setting bit 2 to one enables receive pattern testing	45.2.2.6.4		WIS:M	Yes [ ] N/A [ ]
WM30	Setting bit 2 to zero disables receive pattern testing	45.2.2.6.4		WIS:M	Yes [ ] N/A [ ]
WM31	Setting bit 1 to one enables transmit pattern testing	45.2.2.6.5		WIS:M	Yes [ ] N/A [ ]
WM32	Setting bit 1 to zero disables transmit pattern testing	45.2.2.6.5		WIS:M	Yes [ ] N/A [ ]
WM33	Setting bit 0 to a one enables 10GBASE-W logic and sets interface speed	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM34	Setting bit 0 to a zero disables 10GBASE-W logic, sets interface speed. and bypasses data	45.2.2.6.6		WIS:O	Yes [ ] N/A [ ]
WM35	Writes to bit are ignored by WIS not capable of supporting 10GBASE-R	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM36	Bit returns one when read if WIS is not capable of supporting 10GBASE-R	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM37	Writes to status 2 register have no effect	45.2.2.7		WIS:M	Yes [ ] N/A [ ]
WM38	Counter is reset to all zeros when read or reset	45.2.2.8		WIS* WPT:M	Yes [ ] N/A [ ]
WM39	Counter is held at all ones at overflow	45.2.2.8		WIS* WPT:M	Yes [ ] N/A [ ]
WM40	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.2.9		WIS:M	Yes [ ] N/A [ ]
WM41	Writes to Status 3 register have no effect	45.2.2.10		WIS:M	Yes [ ] N/A [ ]
WM42	SEF bit implemented using latching high behavior	45.2.2.10.1		WIS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
WM43	Far end PLM-P/LCD-P bit implemented using latching high behavior	45.2.2.10.2		WIS:M	Yes [ ] N/A [ ]
WM44	Far end AIS-P/LOP-P bit implemented using latching high behavior	45.2.2.10.3		WIS:M	Yes [ ] N/A [ ]
WM45	LOF bit implemented using latching high behavior	45.2.2.10.4		WIS:M	Yes [ ] N/A [ ]
WM46	LOS bit implemented using latching high behavior	45.2.2.10.5		WIS:M	Yes [ ] N/A [ ]
WM47	RDI-L bit implemented using latching high behavior	45.2.2.10.6		WIS:M	Yes [ ] N/A [ ]
WM48	AIS-L bit implemented using latching high behavior	45.2.2.10.7		WIS:M	Yes [ ] N/A [ ]
WM49	LCD-P bit implemented using latching high behavior	45.2.2.10.8		WIS:M	Yes [ ] N/A [ ]
WM50	PLM-P bit implemented using latching high behavior	45.2.2.10.9		WIS:M	Yes [ ] N/A [ ]
WM51	AIS-P bit implemented using latching high behavior	45.2.2.10.10		WIS:M	Yes [ ] N/A [ ]
WM52	LOP-P bit implemented using latching high behavior	45.2.2.10.11		WIS:M	Yes [ ] N/A [ ]

45.5.3.6 PCS options

Item	Feature	Subclause	Value/Comment	Status	Support
*100CR	Implementation of 100GBASE-R PCS	45.2.3.7		PCS:O	Yes [ ] No [ ] N/A [ ]
*40CR	Implementation of 40GBASE-R PCS	45.2.3.7		PCS:O	Yes [ ] No [ ] N/A [ ]
*CR	Implementation of 10GBASE-R PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*XCR	Implementation of 10/40/100GBASE-R PCS	45.2.3.7		100CR:M 40CR:M 10CR:M	Yes [ ] No [ ] N/A [ ]
*CT	Implementation of the 10GBASE-T PCS or the PCS of any other member of the MultiGBASE-T set	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*CX	Implementation of 10GBASE-X PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
*XP	Implementation of 10GBASE-X pattern testing	45.2.3		CX:O	Yes [ ] No [ ] N/A [ ]
*PPT	Implementation of PRBS31 pattern testing	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*PTT	Implementation of PRBS9 pattern testing	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*EPC	Implementation of the 10BASE-TS/2BASE-TL PCS	45.2.3.27		PCS:O	Yes [ ] No [ ] N/A [ ]
*PAF	Implementation of the PME aggregation function	45.2.3.27		EPC:O	Yes [ ] No [ ] N/A [ ]
*CPR	Implementation of 10GBASE-PR or 10/1GBASE-PRX PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*EEE	Implementation of EEE			O	Yes [ ] N/A [ ]
*BHOAM	1000BASE-H OAM channel implementation	45.2.3.51 and 45.2.3.52		PCS:O	Yes [ ] No [ ] N/A [ ]
2.5GX	Implementation of 2.5GBASE-X PCS	45.2.3.8		PCS:O	Yes [ ] No [ ] N/A [ ]
5GR	Implementation of 5GBASE-R PCS	45.2.3.8		PCS:O	Yes [ ] No [ ] N/A [ ]

45.5.3.7 PCS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Device responds to all register addresses for that device	45.2		PCS:M	Yes [ ] N/A [ ]
RM2	Writes to undefined and read-only registers have no effect	45.2		PCS:M	Yes [ ] N/A [ ]
RM3	Operation is not affected by writes to reserved and unsupported bits	45.2		PCS:M	Yes [ ] N/A [ ]
RM4	Reserved and unsupported bits return a value of zero	45.2		PCS:M	Yes [ ] N/A [ ]
RM5	Latching low bits remain low until after they have been read via the management interface	45.2		PCS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PCS:M	Yes [ ] N/A [ ]
RM7	Latching high bits remain high until after they have been read via the management interface	45.2		PCS:M	Yes [ ] N/A [ ]
RM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PCS:M	Yes [ ] N/A [ ]
RM9	Action on reset	45.2.3.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PCS:M	Yes [ ] N/A [ ]
RM10	Return 1 until reset completed	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM11	Reset completes within 0.5 s	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM12	Device responds to reads of register bits 3.0.15 and 3.5.15:14 during reset	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM13	Loopback mode	45.2.3.1.2	Whenever bit 3.0.14 is set to a one	PCS:M	Yes [ ] N/A [ ]
RM14	Transmit data is returned on the receive path during loopback	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM15	Writes to loopback bit are ignored with port type selections other than 100BASE-T1, 10GBASE-R, or 10GBASE-T	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM16	Loopback bit returns zero with port type selections other than 100BASE-T1, 10GBASE-R, or 10GBASE-T	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM17	Device responds to transactions necessary to exit low-power mode while in low- power state	45.2.3.1.3		PCS:M	Yes [ ] N/A [ ]
RM18	Speed selection bits 13 and 6 are written as one	45.2.3.1.5		PCS:M	Yes [ ] N/A [ ]
RM19	Invalid writes to speed selection bits are ignored	45.2.3.1.5		PCS:M	Yes [ ] N/A [ ]
RM20	Writes to PCS status 1 register have no effect	45.2.3.2		PCS:M	Yes [ ] N/A [ ]
RM21	Receive link status implemented using latching low behavior	45.2.3.2.7		PCS:M	Yes [ ] N/A [ ]
RM22	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.3.3		PCS:M	Yes [ ] N/A [ ]
RM23	PCS type is selected using bits 4 through 0	45.2.3.6.1		PCS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM24	Writes to the type selection bits that select types that have not been advertised are ignored	45.2.3.6.1		PCS:M	Yes [ ] N/A [ ]
RM25	Writes to PCS status 2 register have no effect	45.2.3.7		PCS:M	Yes [ ] N/A [ ]
RM26	Transmit fault implemented with latching high behavior	45.2.3.7.4		PCS:M	Yes [ ] N/A [ ]
RM27	Receive fault implemented with latching high behavior	45.2.3.7.5		PCS:M	Yes [ ] N/A [ ]
RM28	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.3.9		PCS:M	Yes [ ] N/A [ ]
RM29	Writes to 10GBASE-X PCS status register have no effect	45.2.3.13		PCS* CX:M	Yes [ ] N/A [ ]
RM30	Register returns zero if the PCS does not implement the 10GBASE-X port type	45.2.3.13		PCS* !CX:M	Yes [ ] N/A [ ]
RM31	EEE capability indicated for each port type	45.2.3.10		EEE:M	Yes [ ] N/A [ ]
RM32	EEE wake error counter behavior as specified	45.2.3.12		EEE:M	Yes [ ] N/A [ ]
RM33	Writes to bit are ignored and reads return a value of zero	45.2.3.14.1		PCS* PX:M	Yes [ ] N/A [ ]
RM34	Setting the bits to <10> selects the mixed frequency pattern	45.2.3.14.2		PCS* PX:M	Yes [ ] N/A [ ]
RM35	Setting the bits to <01> selects the low-frequency pattern	45.2.3.14.2		PCS* PX:M	Yes [ ] N/A [ ]
RM36	Setting the bits to <00> selects the high-frequency pattern	45.2.3.14.2		PCS* PX:M	Yes [ ] N/A [ ]
RM37	Writes to BASE-R and MultiGBASE-T PCS status 1 register have no effect	45.2.3.15		CR:M CT:M	Yes [ ] N/A [ ]
RM38	Reads from BASE-R and MultiGBASE-T PCS status 1 register return zero for PCS that does not support 10GBASE-R	45.2.3.15		CR:M CT:M	Yes [ ] N/A [ ]
RM39	Writes to BASE-R and MultiGBASE-T PCS status 2 register have no effect	45.2.3.16		XCR:M CT:M	Yes [ ] N/A [ ]
RM40	Reads from BASE-R and MultiGBASE-T PCS status 2 register return zero for PCS that does not support 10/40/100GBASE-R or any MultiGBASE-T	45.2.3.16		XCR:M CT:M	Yes [ ] N/A [ ]
RM41	Latched block lock implemented with latching low behavior	45.2.3.16.1		XCR:M CT:M	Yes [ ] N/A [ ]

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RM42	Latched high BER implemented with latching high behavior	45.2.3.16.2		XCR:M CT:M	Yes [ ] N/A [ ]
RM43	BER counter resets to all zeros on read or reset	45.2.3.16.3		XCR:M CT:M	Yes [ ] N/A [ ]
RM44	BER counter holds at all ones at overflow	45.2.3.16.3		!RM53:M	Yes [ ] N/A [ ]
RM45	Errored blocks counter implemented as a non roll over counter	45.2.3.16.4		!RM57:M	Yes [ ] N/A [ ]
RM46	Errored blocks counter resets to all zeros on read	45.2.3.16.4		XCR:M CT:M	Yes [ ] N/A [ ]
RM47	Setting bit 3.42.5 to a one enables PRBS31 receive pattern testing if bit 3.32.2 is a one and bit 3.42.2 is not a one	45.2.3.19.3		PCS* PPT:M	Yes [ ] N/A [ ]
RM48	Setting bit 3.42.5 to a zero disables PRBS31 receive pattern testing	45.2.3.19.3		PCS* PPT:M	Yes [ ] N/A [ ]
RM49	Setting bit 3.42.4 to a one enables PRBS31 transmit pattern testing if bit 3.32.2 is a one and bit 3.42.3 is not a one	45.2.3.19.4		PCS* PPT:M	Yes [ ] N/A [ ]
RM50	Setting bit 3.42.4 to a zero disables PRBS31 transmit pattern testing	45.2.3.19.4		PCS* PPT:M	Yes [ ] N/A [ ]
RM51	Test-pattern error counter resets to all zeros on read or reset	45.2.3.20		XCR:M	Yes [ ] N/A [ ]
RM52	Test-pattern error counter holds at all ones at overflow	45.2.3.20		XCR:M	Yes [ ] N/A [ ]
RM53	BER high order counter implemented	45.2.3.21		CR:O 40CR:M 100CR:M	Yes [ ] N/A [ ]
RM54	High order bits latched on read to 3.33	45.2.3.21		RM53:M	Yes [ ] N/A [ ]
RM55	Counter reset on read to 3.33 or PCS reset	45.2.3.21		RM53:M	Yes [ ] N/A [ ]
RM56	Counter held at all ones in the case of an overflow	45.2.3.21		RM53:M	Yes [ ] N/A [ ]
RM57	Errored blocks high order counter implemented	45.2.3.22		CR:O 40CR:M 100CR:M	Yes [ ] N/A [ ]
RM58	Register bit 3.45.15 set to one	45.2.3.22		RM57:M	Yes [ ] N/A [ ]
RM59	High order bits latched on read to 3.33	45.2.3.22		RM57:M	Yes [ ] N/A [ ]
RM60	Counter reset on read to 3.33 or PCS reset	45.2.3.22		RM57:M	Yes [ ] N/A [ ]

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RM61	Counter held at all ones in the case of an overflow	45.2.3.22		RM57:M	Yes [ ] N/A [ ]
RM62	Bit indicates fault when any PCS register indicates fault	45.2.3.2.5	If subtype is supported	PCS*EPC:O	Yes [ ] No [ ] N/A [ ]
RM63	Writes to multi-lane BASE-R PCS alignment status 1 register have no effect	45.2.3.23		XCR:M	Yes [ ] N/A [ ]
RM64	Non multi-lane BASE-R device shall return all zeros	45.2.3.23		!XCR:M	Yes [ ] N/A [ ]
RM65	Device shall return a zero for lanes not required	45.2.3.23		XCR:M	Yes [ ] N/A [ ]
RM66	Writes to multi-lane BASE-R PCS alignment status 2 register have no effect	45.2.3.24		XCR:M	Yes [ ] N/A [ ]
RM67	Non multi-PCS lane BASE-R device shall return all zeros	45.2.3.24		!XCR:M	Yes [ ] N/A [ ]
RM68	Device shall return a zero for lanes not required	45.2.3.24		XCR:M	Yes [ ] N/A [ ]
RM69	Writes to multi-lane BASE-R PCS alignment status 3 register have no effect	45.2.3.25		XCR:M	Yes [ ] N/A [ ]
RM70	Non multi-PCS lane BASE-R device shall return all zeros	45.2.3.25		!XCR:M	Yes [ ] N/A [ ]
RM71	Device shall return a zero for lanes not required	45.2.3.25		XCR:M	Yes [ ] N/A [ ]
RM72	Writes to multi-lane BASE-R PCS alignment status 4 register have no effect	45.2.3.26		XCR:M	Yes [ ] N/A [ ]
RM73	Non multi-PCS lane BASE-R device shall return all zeros	45.2.3.26		!XCR:M	Yes [ ] N/A [ ]
RM74	Device shall return a zero for lanes not required	45.2.3.26		XCR:M	Yes [ ] N/A [ ]
RM75	Counters reset on read to 3.200 through 3.219 or PCS reset	45.2.3.47		XCR:M	Yes [ ] N/A [ ]
RM76	Counters held at all ones in the case of an overflow	45.2.3.47		XCR:M	Yes [ ] N/A [ ]
RM77	Writing this bit to a one activates the PAF when link is established	45.2.3.28.3		PCS*PAF:M	Yes [ ] N/A [ ]
RM78	Writes to bit are ignored while link is active or initializing or if PAF is not supported	45.2.3.28.3		PCS*PAF:M	Yes [ ] N/A [ ]
RM79	Bits indicate device capabilities upon reset	45.2.3.29		PCS*PAF:M	Yes [ ] N/A [ ]

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RM80	Writes to the register through any PCS MMD in the same package effect the register equally	45.2.3.29		PCS*PAF:M	Yes [ ] N/A [ ]
RM81	Single bit set to one and all others cleared to zero when device does not support aggregation of multiple PMEs	45.2.3.29		PCS:M	Yes [ ] N/A [ ]
RM82	PME aggregation used if one or more bits set	45.2.3.30		PCS*PAF:M	Yes [ ] N/A [ ]
RM83	Registers set to all zeros upon reset	45.2.3.30		PCS*PAF:M	Yes [ ] N/A [ ]
RM84	Writes to the register through any PCS MMD in the same package effect the register equally	45.2.3.30		PCS*PAF:M	Yes [ ] N/A [ ]
RM85	Bits reset to zero when read or upon MMD reset	45.2.3.31		PCS*PAF:M	Yes [ ] N/A [ ]
RM86	Bits held to one upon overflow	45.2.3.31		PCS*PAF:M	Yes [ ] N/A [ ]
RM87	Bits reset to zero when read or upon MMD reset	45.2.3.32		PCS*PAF:M	Yes [ ] N/A [ ]
RM88	Bits held to one upon overflow	45.2.3.32		PCS*PAF:M	Yes [ ] N/A [ ]
RM89	Bits reset to zero when read or upon MMD reset	45.2.3.33		PCS*PAF:M	Yes [ ] N/A [ ]
RM90	Bits held to one upon overflow	45.2.3.33		PCS*PAF:M	Yes [ ] N/A [ ]
RM91	Bits reset to zero when read or upon MMD reset	45.2.3.34		PCS*PAF:M	Yes [ ] N/A [ ]
RM92	Bits held to one upon overflow	45.2.3.34		PCS*PAF:M	Yes [ ] N/A [ ]
RM93	Bits reset to zero when read or upon MMD reset	45.2.3.35		PCS*PAF:M	Yes [ ] N/A [ ]
RM94	Bits held to one upon overflow	45.2.3.35		PCS*PAF:M	Yes [ ] N/A [ ]
RM95	Bits reset to zero when read or upon MMD reset	45.2.3.36		PCS*PAF:M	Yes [ ] N/A [ ]
RM96	Bits held to one upon overflow	45.2.3.36		PCS*PAF:M	Yes [ ] N/A [ ]
RM97	Bits reset to zero when read or upon MMD reset	45.2.3.37		PCS*PAF:M	Yes [ ] N/A [ ]
RM98	Bits held to one upon overflow	45.2.3.37		PCS*PAF:M	Yes [ ] N/A [ ]
RM99	Bits reset to zero when read or upon MMD reset	45.2.3.38		PCS*PAF:M	Yes [ ] N/A [ ]

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RM100	Bits held to one upon overflow	45.2.3.38		PCS*PAF:M	Yes [ ] N/A [ ]
RM101	Setting bit 3.42.6 to a one enables PRBS9 transmit pattern testing if bit 3.32.3 is a one and bit 3.42.3 is not a one and bit 3.42.4 is not a one	45.2.3.19.2		PCS* PTT:M	Yes [ ] N/A [ ]
RM102	Setting bit 3.42.6 to a zero disables PRBS9 transmit pattern testing	45.2.3.19.2		PCS* PTT:M	Yes [ ] N/A [ ]
RM103	Corrected FEC codeword counter is reset when read or upon PHY reset	45.2.3.41		CPR:M	Yes [ ] No [ ] N/A [ ]
RM104	Corrected FEC codeword counter is held at all ones in the case of overflow	45.2.3.41		CPR:M	Yes [ ] No [ ] N/A [ ]
RM105	Uncorrected FEC codeword counter is reset when read or upon PHY reset	45.2.3.42		CPR:M	Yes [ ] No [ ] N/A [ ]
RM106	Uncorrected FEC codeword counter is held at all ones in the case of overflow	45.2.3.42		CPR:M	Yes [ ] No [ ] N/A [ ]
RM107	This action sets all 1000BASE-T1 PCS registers to their default states.	45.2.3.76.1		PCS:M	Yes [ ] N/A [ ]
RM108	Bit 3.2304.15 is self-clearing, and the 1000BASE-T1 PCS returns a value of one in bit 3.2304.15 when a reset is in progress.	45.2.3.76.1		PCS:M	Yes [ ] N/A [ ]
RM109	Otherwise, bit 3.2304.15 returns a value of zero.	45.2.3.76.1		PCS:M	Yes [ ] N/A [ ]
RM110	During a reset, the 1000BASE-T1 PCS responds to reads from register bits 3.0.15, 3.8.15:14, and 3.2304.15.	45.2.3.76.1		PCS:M	Yes [ ] N/A [ ]
RM111	All other register bits are ignored during a reset.	45.2.3.76.1		PCS:M	Yes [ ] N/A [ ]
RM112	Setting either bit 3.2304.15 or 3.0.15 resets the 1000BASE-T1 PCS.	45.2.3.76.1		PCS:M	Yes [ ] N/A [ ]
RM113	The 1000BASE-T1 PCS is placed in a loopback mode of operation when bit 3.2304.14 is set to a one.	45.2.3.76.2		PCS:M	Yes [ ] N/A [ ]
RM114	When bit 3. 2304.14 is set to a one, the 1000BASE-T1 PCS accepts data on the transmit path and return it on the receive path.	45.2.3.76.2		PCS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM115	Setting either bit 3.2304.14 or 3.0.14 enables loopback.	45.2.3.76.2		PCS:M	Yes [ ] N/A [ ]
RM116	All the bits in the 1000BASE-T1 PCS status 1 register are read only; a write to the 1000BASE-T1 PCS status 1 register has no effect.	45.2.3.77		PCS:M	Yes [ ] N/A [ ]
RM117	Bit 3.2305.11 is implemented with latching high behavior.	45.2.3.77.1		PCS:M	Yes [ ] N/A [ ]
RM118	Bit 3.2305.10 is implemented with latching high behavior.	45.2.3.77.2		PCS:M	Yes [ ] N/A [ ]
RM119	All the bits in the 1000BASE-T1 PCS status 2 register are read only; a write to the 1000BASE-T1 PCS status 2 register has no effect.	45.2.3.78		PCS:M	Yes [ ] N/A [ ]
RM120	Bit 3.2306.7 is implemented with latching high behavior.	45.2.3.78.4		PCS:M	Yes [ ] N/A [ ]
RM121	Bit 3.2306.6 is implemented with latching low behavior.	45.2.3.78.5		PCS:M	Yes [ ] N/A [ ]
RM122	Bits 3.2306.5:0 are reset to all zeros when the 1000BASE-T1 PCS status 2 register is read by the management function or upon execution of the 1000BASE-T1 PCS reset.	45.2.3.78.6		PCS:M	Yes [ ] N/A [ ]
RM123	Bits 3.2306.5:0 are held at all ones in the case of overflow.	45.2.3.78.6		PCS:M	Yes [ ] N/A [ ]
RM124	The state machine assigns a value alternating between zero and one to associate with the 8-octet OAM message transmitted by the BASE-T1 PHY.	45.2.3.79.2		PCS:M	Yes [ ] N/A [ ]
RM125	Bit 3.2308.14 is read and recorded prior to setting 3.2308.15 to one.	45.2.3.79.2		PCS:O	Yes [ ] No [ ]
RM126	Bit 3.2308.14 self clears on read.	45.2.3.79		PCS:M	Yes [ ] N/A [ ]
RM127	Bit 3.2308.13 indicates whether the most recently transmitted OAM message with a toggle bit value in 3.2308.12 was received, read, and acknowledged by the link partner.	45.2.3.79.3		PCS:M	Yes [ ] N/A [ ]
RM128	Bit 3.2308.13 clears on read.	45.2.3.79.3		PCS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM129	Bit 3.2313.15 is set to one when the OAM message from the link partner is stored into registers 3.2314, 3.2315, 3.2316, and 3.2317 and the message number in 3.2313.11:8.	45.2.3.81.1		PCS:M	Yes [ ] N/A [ ]
RM130	Bit 3.2313.15 self-clears when register 3.2317 is read.	45.2.3.81.1		PCS:M	Yes [ ] N/A [ ]
RM131	1000BASE-H OAM message format to be transmitted	45.2.3.51.5	TXO_DATA0[10:0] = OUI[23:12], TXO_DATA1[15:3] = OUI[11:0], and TXO_DATA1[3:0] = protocol number. Content of TXO_DATA2 to TXO_DATA8 is vendor specific per OUI or Company ID	PCS *BHOAM:M	Yes [ ] N/A [ ]
RM132	Default operation mode	45.2.3.53.1	Default value of bits 3.518.15:13 is binary 000 (normal mode)	PCS:M	Yes [ ] N/A [ ]
RM133	Test operation modes	45.2.3.53.1	Values binary 001 through binary 110 of bits 3.518.15:13 select test modes of Table 45–280, with behavior per 115.5	PCS:M	Yes [ ] N/A [ ]
RM134	Default loopback mode	45.2.3.53.2	Default value of bits 3.518.12:10 is binary 000 (no loopback operation)	PCS:M	Yes [ ] N/A [ ]
RM135	Loopback modes	45.2.3.53.2	Bits 3.518.12:10 select loopback modes with behavior per 115.10	PCS:M	Yes [ ] N/A [ ]
RM136	1000BASE-H OAM conditional enable	45.2.3.53.3	Write a one to bit 3.518.1 only produces effect if bit 3.519.1 is read as one	PCS *BHOAM:M	Yes [ ] N/A [ ]
RM137	1000BASE-H OAM disable	45.2.3.53.3	Write a zero to bit 3.518.1 prevents 1000BASE-H OAM channel establishment with link partner	PCS *BHOAM:M	Yes [ ] N/A [ ]
RM138	1000BASE-H OAM enable change effect	45.2.3.53.3	Changes in the value of bit 3.518.1 only takes effect after PMA reset	PCS *OAM:M	Yes [ ] N/A [ ]
RM139	EEE conditional enable	45.2.3.53.4	Write a one to bit 3.518.0 only produces effect if bit 3.519.0 is read as one	PCS *EEE:M	Yes [ ] N/A [ ]
RM140	EEE disable	45.2.3.53.4	Write a zero to bit 3.518.0 prevents EEE operation with link partner	PCS *EEE:M	Yes [ ] N/A [ ]
RM141	EEE enable change effect	45.2.3.53.4	Changes in the value of bit 3.518.0 only takes effect after PMA reset	PCS *EEE:M	Yes [ ] N/A [ ]

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RM142	Link status behavior	45.2.3.54.3	Bit 3.519.13 has latching low behavior	PCS:M	Yes [ ] N/A [ ]
RM143	Link status mirroring	45.2.3.54.3	Bit 1.1.2, bit 3.1.2, and bit 3.519.13 reflect same state variable link_status and a read of any of them releases the latch of all the bits	PCS:M	Yes [ ] N/A [ ]
RM144	PHD lock status behavior	45.2.3.54.6	Bit 3.519.10 has latching low behavior	PCS:M	Yes [ ] N/A [ ]
RM145	Tx Assert LPI received behavior	45.2.3.54.8	Bit 3.519.8 has latching high behavior	PCS *EEE:M	Yes [ ] N/A [ ]
RM146	Tx Assert LPI received mirroring	45.2.3.54.8	Bit 3.519.8 is a copy of bit 3.1.11 and a read of any of them releases the latch of all the bits	PCS *EEE:M	Yes [ ] N/A [ ]
RM147	Rx Assert LPI generated behavior	45.2.3.54.9	Bit 3.519.7 has latching high behavior	PCS *EEE:M	Yes [ ] N/A [ ]
RM148	Rx Assert LPI generated mirroring	45.2.3.54.9	Bit 3.519.7 is a copy of bit 3.1.10 and a read of any of them releases the latch of all the bits	PCS *EEE:M	Yes [ ] N/A [ ]
RM149	1000BASE-H OAM ability	45.2.3.54.14	Registers 3.500 through 3.517 are implemented and 3.519.1 reads as one	PCS *BHOAM:M	Yes [ ] N/A [ ]
RM150	BER test mode counter is reset to all zeros when read	45.2.3.57		PCS:M	Yes [ ] N/A [ ]
RM151	BER test mode counter holds all ones in case of overflow	45.2.3.57		PCS:M	Yes [ ] N/A [ ]
RM152	This action sets all 10BASE-T1L PCS registers to their default states	45.2.3.70.1		PCS:M	Yes [ ] N/A [ ]
RM153	The 10BASE-T1L PCS returns a value of one in bit 3.2278.15 when a reset is in progress; otherwise, returns a value of zero	45.2.3.70.1		PCS:M	Yes [ ] N/A [ ]
RM154	The control and management interface is restored to operation within 0.5 s from the setting of bit 3.2278.15	45.2.3.70.1		PCS:M	Yes [ ] N/A [ ]
RM155	During a reset, the 10BASE-T1L PCS responds to reads from register bits 3.0.15, 3.8.15:14, and 3.2278.15; reads for all other bits are ignored	45.2.3.70.1		PCS:M	Yes [ ] N/A [ ]
RM156	Setting either 3.2278.15 or 3.0.15 sets the other	45.2.3.70.1		PCS:M	Yes [ ] N/A [ ]
RM157	Clearing either 3.2278.15 or 3.0.15 clears the other	45.2.3.70.1		PCS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM158	Setting either 3.2278.15 or 3.0.15 resets the 10BASE-T1L PCS	45.2.3.70.1		PCS:M	Yes [ ] N/A [ ]
RM159	When bit 3.2278.14 is set to one, the 10BASE-T1L PCS is set to loopback mode, and it accepts data on the transmit path and returns it on the receive path	45.2.3.70.2		PCS:M	Yes [ ] N/A [ ]
RM160	Setting either 3.2278.14 or 3.0.14 sets the other	45.2.3.70.2		PCS:M	Yes [ ] N/A [ ]
RM161	Clearing either 3.2278.14 or 3.0.14 clears the other	45.2.3.70.2		PCS:M	Yes [ ] N/A [ ]
RM162	Setting either 3.2278.14 or 3.0.14 enables loopback	45.2.3.70.2		PCS:M	Yes [ ] N/A [ ]
RM163	A write to the 10BASE-T1L PCS status 1 register has no effect	45.2.3.71		PCS:M	Yes [ ] N/A [ ]
RM164	Bit 3.2279.11 is implemented with latching high behavior	45.2.3.71.1		PCS:M	Yes [ ] N/A [ ]
RM165	Bit 3.2279.10 is implemented with latching high behavior	45.2.3.71.2		PCS:M	Yes [ ] N/A [ ]
RM166	Bit 3.2279.7 is implemented with latching high behavior	45.2.3.71.5		PCS:M	Yes [ ] N/A [ ]
RM167	Bit 3.2279.2 is implemented with latching low behavior	45.2.3.71.6		PCS:M	Yes [ ] N/A [ ]
RM168	This action sets all 10BASE-T1S PCS registers to their default states	45.2.3.72.1		PCS:M	Yes [ ] N/A [ ]
RM169	The 10BASE-T1S PCS returns a value of one in bit 3.2291.15 when a reset is in progress; otherwise, returns a value of zero	45.2.3.72.1		PCS:M	Yes [ ] N/A [ ]
RM170	The control and management interface is restored to operation within 0.5 s from the setting of bit 3.2291.15	45.2.3.72.1		PCS:M	Yes [ ] N/A [ ]
RM171	During a reset, the 10BASE-T1S PCS responds to reads from register bits 3.0.15, 3.8.15:14, and 3.2291.15; reads for all other bits are ignored	45.2.3.72.1		PCS:M	Yes [ ] N/A [ ]
RM172	Setting either 3.2291.15 or 3.0.15 sets the other	45.2.3.72.1		PCS:M	Yes [ ] N/A [ ]
RM173	Clearing either 3.2291.15 or 3.0.15 clears the other	45.2.3.72.1		PCS:M	Yes [ ] N/A [ ]
RM174	Setting either 3.2291.15 or 3.0.15 resets the 10BASE-T1S PCS	45.2.3.72.1		PCS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM175	When bit 3.2291.14 is set to one, the 10BASE-T1S PCS is set to loopback mode, and it accepts data on the transmit path and returns it on the receive path	45.2.3.72.2		PCS:M	Yes [ ] N/A [ ]
RM176	Setting either 3.2291.14 or 3.0.14 sets the other	45.2.3.72.2		PCS:M	Yes [ ] N/A [ ]
RM177	Clearing either 3.2291.14 or 3.0.14 clears the other	45.2.3.72.2		PCS:M	Yes [ ] N/A [ ]
RM178	Setting either 3.2291.14 or 3.0.14 enables loopback	45.2.3.72.2		PCS:M	Yes [ ] N/A [ ]
RM179	Bit 3.2291.8 or 0.8 is ignored when the Auto-Negotiation enable bit 7.512.12 is set to one	45.2.3.72.3		PCS:M	Yes [ ] N/A [ ]
RM180	Setting either 3.2291.8 or 0.8 sets the other	45.2.3.72.3		PCS:M	Yes [ ] N/A [ ]
RM181	Clearing either 3.2291.8 or 0.8 clears the other	45.2.3.72.3		PCS:M	Yes [ ] N/A [ ]
RM182	The 10BASE-T1S PCS fault bit is implemented with latching high behavior	45.2.3.73.1		PCS:M	Yes [ ] N/A [ ]
RM183	A write to the 10BASE-T1S PCS status register has no effect	45.2.3.73		PCS:M	Yes [ ] N/A [ ]
RM184	A write to the 10BASE-T1S PCS diagnostic register has no effect	45.2.3.74		PCS:M	Yes [ ] N/A [ ]
RM185	Remote jabber count does not wrap	45.2.3.74.1		PCS:M	Yes [ ] N/A [ ]
RM186	Writes to PCS diagnostic 2 register have no effect	45.2.3.75		PCS:M	Yes [ ] N/A [ ]
RM187	Setting bit 3.2322.15 sets all MultiGBASE-T1 PCS registers to their default states.	45.2.3.85.1		PCS:M	Yes [ ] N/A [ ]
RM188	Bit 3.2322.15 is self-clearing, and the MultiGBASE-T1 PCS returns a value of one in bit 3.2322.15 when a reset is in progress.	45.2.3.85.1		PCS:M	Yes [ ] N/A [ ]
RM189	Otherwise, bit 3.2322.15 returns a value of zero.	45.2.3.85.1		PCS:M	Yes [ ] N/A [ ]
RM190	During a reset, the MultiGBASE-T1 PCS responds to reads from register bits 3.0.15, 3.8.15:14, and 3.2322.15.	45.2.3.85.1		PCS:M	Yes [ ] N/A [ ]
RM191	All other register bits are ignored during a reset.	45.2.3.85.1		PCS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM192	Setting or clearing either bit 3.2322.15 or 3.0.15 sets or clears the other bit.	45.2.3.85.1		PCS:M	Yes [ ] N/A [ ]
RM193	Setting either bit 3.2322.15 or 3.0.15 resets the MultiGBASE-T1 PCS.	45.2.3.85.1		PCS:M	Yes [ ] N/A [ ]
RM194	The MultiGBASE-T1 PCS is placed in a loopback mode of operation when bit 3.2322.14 is set to a one.	45.2.3.85.2		PCS:M	Yes [ ] N/A [ ]
RM195	When bit 3.2322.14 is set to a one, the MultiGBASE-T1 PCS accepts data on the transmit path and returns it on the receive path.	45.2.3.85.2		PCS:M	Yes [ ] N/A [ ]
RM196	Setting or clearing either bit 3.2322.14 or 3.0.14 sets or clears the other bit.	45.2.3.85.2		PCS:M	Yes [ ] N/A [ ]
RM197	Setting either bit 3.2322.14 or 3.0.14 enables loopback.	45.2.3.85.2		PCS:M	Yes [ ] N/A [ ]
RM198	All bits in the MultiGBASE_T1 PCS status 1 register are read only; a write to the MultiGBASE-T1 PCS status 1 register has no effect.	45.2.3.86		PCS:M	Yes [ ] N/A [ ]
RM199	Bit 3.2323.11 is implemented with latching high behavior.	45.2.3.86.1		PCS:M	Yes [ ] N/A [ ]
RM200	Bit 3.2323.10 is implemented with latching high behavior.	45.2.3.86.2		PCS:M	Yes [ ] N/A [ ]
RM201	Bit 3.2323.2 is implemented with latching low behavior.	45.2.3.86.6		PCS:M	Yes [ ] N/A [ ]
RM202	All bits in the MultiGBASE_T1 PCS status 2 register are read only; a write to the the MultiGBASE-T1 PCS status 2 register has no effect.	45.2.3.87		PCS:M	Yes [ ] N/A [ ]
RM203	Bit 3.2324.7 is implemented with latching high behavior.	45.2.3.87.4		PCS:M	Yes [ ] N/A [ ]
RM204	Bit 3.2324.6 is implemented with latching low behavior.	45.2.3.87.5		PCS:M	Yes [ ] N/A [ ]
RM205	Bits 3.2324.5:0 are reset to all zeros when the MultiGBASE-T1 PCS 2 register is read by management function or upon execution of the MultiGBASE-T1 reset.	45.2.3.87.6		PCS:M	Yes [ ] N/A [ ]
RM206	Bits 3.2324.5:0 are held at all ones in case of overflow.	45.2.3.87.6		PCS:M	Yes [ ] N/A [ ]

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45.5.3.8 Auto-Negotiation options

Item	Feature	Subclause	Value/Comment	Status	Support
*AT	Implementation of MultiGBASE-T Auto-Negotiation	45.2.7		AN:O	Yes [ ] No [ ] N/A [ ]
*AB	Implementation of Backplane Ethernet Auto-negotiation	45.2.7		AN:M	Yes [ ] No [ ] N/A [ ]
*ABN	Implementation of Next Page support for Backplane Ethernet Auto-negotiation	45.2.7		AB:M	Yes [ ] No [ ] N/A [ ]
*EEE	Implementation of EEE			O	Yes [ ] N/A [ ]

45.5.3.9 Auto-Negotiation management functions

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	Device responds to all register addresses for that device	45.2		AN:M	Yes [ ] N/A [ ]
AM2	Writes to undefined and read-only registers have no effect	45.2		AN:M	Yes [ ] N/A [ ]
AM3	Operation is not affected by writes to reserved and unsupported bits	45.2		AN:M	Yes [ ] N/A [ ]
AM4	Reserved and unsupported bits return a value of zero	45.2		AN:M	Yes [ ] N/A [ ]
AM5	Latching low bits remain low until after they have been read via the management interface	45.2		AN:M	Yes [ ] N/A [ ]
AM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	AN:M	Yes [ ] N/A [ ]
AM7	Latching high bits remain high until after they have been read via the management interface	45.2		AN:M	Yes [ ] N/A [ ]
AM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	AN:M	Yes [ ] N/A [ ]
AM9	Action on reset	45.2.7.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	AN:M	Yes [ ] N/A [ ]
AM10	Return 1 until reset completed	45.2.7.1.1		AN:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
AM11	Reset completes within 0.5 s	45.2.7.1.1		AN:M	Yes [ ] N/A [ ]
AM12	Device responds to reads of register bit 7.0.15	45.2.7.1.1	All other register bits should be ignored	AN:M	Yes [ ] N/A [ ]
AM13	Bit set enables Extended Next Page exchange	45.2.7.1.2		AN:M	Yes [ ] N/A [ ]
AM14	Bit 7.0.13 has no effect unless bit 7.16.12 is set	45.2.7.1.2		AN:M	Yes [ ] N/A [ ]
AM15	Auto-Negotiation enabled by setting bit 7.0.12	45.2.7.1.3		AN:M	Yes [ ] N/A [ ]
AM16	Bits 1.0.13, 1.0.6, 1.0.5:2, and 1.7.3:0 have no effect and Auto-Negotiation determines link configuration	45.2.7.1.3		AN:M	Yes [ ] N/A [ ]
AM17	Writes are ignored and bit is set to zero if Auto-Negotiation is disabled or unsupported	45.2.7.1.4		AN:M	Yes [ ] N/A [ ]
AM18	Setting bit to one restarts Auto-Negotiation if supported and enabled	45.2.7.1.4		AN:M	Yes [ ] N/A [ ]
AM19	Bit set until Auto-Negotiation started then self cleared to zero	45.2.7.1.4		AN:M	Yes [ ] N/A [ ]
AM20	Setting this bit restarts Auto-Negotiation if previously completed	45.2.7.1.4		AN:M	Yes [ ] N/A [ ]
AM21	Setting the bit to zero has no effect on Auto-Negotiation process	45.2.7.1.4		AN:M	Yes [ ] N/A [ ]
AM22	Writing the bit to one is ignored if 7.1.3 = 0 or Auto-Negotiation is disabled	45.2.7.1.4		AN:M	Yes [ ] N/A [ ]
AM23	Writes to register ignored	45.2.7.2		AN:M	Yes [ ] N/A [ ]
AM24	Bit set to zero when bits 7.0.13 or 7.16.12 are set to zero	45.2.7.2.2		AN:M	Yes [ ] N/A [ ]
AM25	Extended Next Page not used when bit set to zero	45.2.7.2.2		AN:M	Yes [ ] N/A [ ]
AM26	Bit set to one with link codeword received and stored	45.2.7.2.3		AN:M	Yes [ ] N/A [ ]
AM27	Bit set to zero upon read of register 7.1	45.2.7.2.3		AN:M	Yes [ ] N/A [ ]
AM28	Bit set to zero when bit 7.0.12 is set to zero	45.2.7.2.4		AN:M	Yes [ ] N/A [ ]
AM29	Bit set to zero if device does not support Auto-Negotiation	45.2.7.2.4		AN:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
AM30	Bit remains set until cleared	45.2.7.2.5		AN:M	Yes [ ] N/A [ ]
AM31	Bit cleared to zero upon reset or read of register	45.2.7.2.5		AN:M	Yes [ ] N/A [ ]
AM32	Bit remains set until cleared by register read	45.2.7.2.7		AN:M	Yes [ ] N/A [ ]
AM33	Bit cleared upon AN reset	45.2.7.2.7		AN:M	Yes [ ] N/A [ ]
AM34	Bit set to one if link partner is able to participate in Auto-Negotiation	45.2.7.2.8		AN:M	Yes [ ] N/A [ ]
AM35	Bit set to zero if link partner is not able to participate in Auto-Negotiation	45.2.7.2.8		AN:M	Yes [ ] N/A [ ]
AM36	Unique Identifier is composed of 22 bits of OUI, model number and revision	45.2.7.5		AN:M	Yes [ ] N/A [ ]
AM37	Prior to Auto-Negotiation bits 7.16.12:5 accurately reflect device capability	45.2.7.6		AN:M	Yes [ ] N/A [ ]
AM38	Write has no effect	45.2.7.7		AN:M	Yes [ ] N/A [ ]
AM39	At power up or AN reset message code set to null message	45.2.7.8		AN:M	Yes [ ] N/A [ ]
AM40	Write has no effect	45.2.7.9		AN:M	Yes [ ] N/A [ ]
AM41	Auto-Negotiation used to determine MASTER or SLAVE when bit set to zero	45.2.7.10.1		AN:M	Yes [ ] N/A [ ]
AM42	Operates as MASTER when bit set to one	45.2.7.10.2		AN:M	Yes [ ] N/A [ ]
AM43	Operates as SLAVE when bit set to zero	45.2.7.10.2		AN:M	Yes [ ] N/A [ ]
AM44	Advertise 10GBASE-T PHY capability when bit is set to one	45.2.7.10.4		AN:M	Yes [ ] N/A [ ]
AM45	10GBASE-T PHY capability not advertised when bit is set to zero	45.2.7.10.4		AN:M	Yes [ ] N/A [ ]
AM46	Advertise loop timing capability when bit is set to one	45.2.7.10.15		AN:M	Yes [ ] N/A [ ]
AM47	Loop timing capability not advertised when bit is set to zero	45.2.7.10.15		AN:M	Yes [ ] N/A [ ]
AM48	Write has no effect	45.2.7.11		AN:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
AM49	Bit set if MASTER-SLAVE cannot be successfully concluded	45.2.7.11.1		AN:M	Yes [ ] N/A [ ]
AM50	Bit set to zero on read of register 7.33	45.2.7.11.1		AN:M	Yes [ ] N/A [ ]
AM51	Bit set to zero by MultiGBASE-T PMA reset	45.2.7.11.1		AN:M	Yes [ ] N/A [ ]
AM52	Bit set to zero when Auto-Negotiation is enabled	45.2.7.11.1		AN:M	Yes [ ] N/A [ ]
AM53	Bit set to one if local receiver is OK as defined in 55.2.2.7	45.2.7.11.3		AN:M	Yes [ ] N/A [ ]
AM54	Bit is set to one if the remote receiver status is OK as defined in 55.2.2.8	45.2.7.11.4		AN:M	Yes [ ] N/A [ ]
AM55	Parallel detection fault (7.1.9)	45.2.7.2.1	ONE to indicate more than one Backplane Ethernet PMA indicates link_status of OK when autoneg_wait_timer expires	AB:M	Yes [ ] N/A [ ]
AM56	Parallel detection fault clearing	45.2.7.2.1	ZERO on read of the AN status register.	AN:M	Yes [ ] N/A [ ]
AM57	Bit 7.48.0 set to one	45.2.7.12.4	Set to one if KX, KX4, or KR PHY is implemented	AB:M	Yes [ ] N/A [ ]
AM58	EEE capability in advertisement register for each port type	45.2.7.14		AN:EEE:M	Yes [ ] N/A [ ]
AM59	EEE LP advertisement register reflects link partner's capabilities	45.2.7.15		AN:EEE:M	Yes [ ] N/A [ ]
AM60	Writes to EEE LP advertisement register have no effect	45.2.7.15		AN:EEE:M	Yes [ ] N/A [ ]
AM61	Advertise 40GBASE-T PHY capability when bit is set to one	45.2.7.10.5		AN:M	Yes [ ] N/A [ ]
AM62	40GBASE-T PHY capability not advertised when bit is set to zero	45.2.7.10.5		AN:M	Yes [ ] N/A [ ]
AM63	Advertise 25GBASE-T PHY capability when bit is set to one	45.2.7.10.6		AN:M	Yes [ ] N/A [ ]
AM64	25GBASE-T PHY capability not advertised when bit is set to zero	45.2.7.10.6		AN:M	Yes [ ] N/A [ ]
AM65	Advertise 5GBASE-T PHY capability when bit is set to one	45.2.7.10.8		AN:M	Yes [ ] N/A [ ]
AM66	5GBASE-T PHY capability not advertised when bit is set to zero	45.2.7.10.8		AN:M	Yes [ ] N/A [ ]
AM67	Advertise 2.5GBASE-T PHY capability when bit is set to one	45.2.7.10.9		AN:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
AM68	2.5GBASE-T PHY capability not advertised when bit is set to zero	45.2.7.10.9		AN:M	Yes [ ] N/A [ ]
AM69	Setting bit 7.512.15 to a one sets all BASE-T1 AN registers to their default states.	45.2.7.20.1		AN:M	Yes [ ] N/A [ ]
AM70	Bit 7.512.15 is self-clearing, and AN shall return a value of one in bit 7.512.15 when a reset is in progress and a value of zero otherwise.	45.2.7.20.1		AN:M	Yes [ ] N/A [ ]
AM71	The reset process is completed within 0.5 s from the setting of bit 7.512.15.	45.2.7.20.1		AN:M	Yes [ ] N/A [ ]
AM72	During an AN reset, AN responds to reads from register bit 7.512.15.	45.2.7.20.1		AN:M	Yes [ ] N/A [ ]
AM73	All other register bits are ignored.	45.2.7.20.1		AN:M	Yes [ ] N/A [ ]
AM74	The Auto-Negotiation function is enabled by setting bit 7.512.12 to a one.	45.2.7.20.2		AN:M	Yes [ ] N/A [ ]
AM75	If bit 7.512.12 is set to one, then PHY type bits 1.2100.3:0 and MASTER-SLAVE bits 1.2100.14 has no effect on the link configuration, and the Auto-Negotiation process determines the link configuration.	45.2.7.20.2		AN:M	Yes [ ] N/A [ ]
AM76	If the BASE-T1 PHY reports via bit 7.513.3 that it lacks the ability to perform Auto-Negotiation, then the value of bit 7.512.12 is zero.	45.2.7.20.2		AN:M	Yes [ ] N/A [ ]
AM77	If the BASE-T1 PMA/PMD reports (via bit 7.513.3) that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the BASE-T1 PMA/PMD returns a value of zero in bit 7.512.9 and any attempt to write a one to bit 7.512.9 are ignored.	45.2.7.20.3		AN:M	Yes [ ] N/A [ ]
AM78	Otherwise, the Auto-Negotiation process is restarted by setting bit 7.512.9 to one.	45.2.7.20.3		AN:M	Yes [ ] N/A [ ]
AM79	Bit 7.512.9 is self-clearing, and the BASE-T1 PMA/PMD shall return a value of one in bit 7.512.9 until the Auto-Negotiation process has been initiated.	45.2.7.20.3		AN:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
AM80	If Auto-Negotiation was completed prior to this bit being set, the process is reinitialized.	45.2.7.20.3		AN:M	Yes [ ] N/A [ ]
AM81	The Auto-Negotiation process is affected by clearing this bit to zero.	45.2.7.20.3		AN:M	Yes [ ] N/A [ ]
AM82	All the bits in the BASE-T1 AN status register are read only; therefore, a write to the BASE-T1 AN status register has no effect.	45.2.7.21		AN:M	Yes [ ] N/A [ ]
AM83	The Page received bit (7.513.6) is set to one to indicate that a new link codeword has been received and stored in the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 or the BASE-T1 AN LP Next Page ability registers 7.523 to 7.525.	45.2.7.21.1		AN:M	Yes [ ] N/A [ ]
AM84	The Page received bit is reset to zero on a read of the BASE-T1 AN status register (register 7.513).	45.2.7.21.1		AN:M	Yes [ ] N/A [ ]
AM85	The BASE-T1 PMA/PMD returns a value of zero in bit 7.513.5 if Auto-Negotiation is disabled by clearing bit 7.512.12.	45.2.7.21.2		AN:M	Yes [ ] N/A [ ]
AM86	The BASE-T1 PMA/PMD also returns a value of zero in bit 7.513.5 if it lacks the ability to perform Auto-Negotiation.	45.2.7.21.2		AN:M	Yes [ ] N/A [ ]
AM87	The remote fault bit is implemented with a latching function, such that the occurrence of a remote fault causes the bit 7.513.4 to become set and remain set until it is cleared.	45.2.7.21.3		AN:M	Yes [ ] N/A [ ]
AM88	Bit 7.513.4 is cleared each time register 7.513 is read via the management interface, and is also cleared by a AN reset.	45.2.7.21.3		AN:M	Yes [ ] N/A [ ]
AM89	The link status bit is implemented with a latching function, such that the occurrence of a link_status equals FAIL condition causes the link status bit to become cleared and remain cleared until it is read via the management interface.	45.2.7.21.5		AN:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
AM90	Bit 7.513.2 is cleared upon AN reset.	45.2.7.21.5		AN:M	Yes [ ] N/A [ ]
AM91	A write to the BASE-T1 AN LP Base Page ability register has no effect.	45.2.7.23		AN:M	Yes [ ] N/A [ ]
AM92	On power-up or AN reset, registers 7.520, 7.521, and 7.522 contain the default value, which represents a Message Page with the message code set to Null Message.	45.2.7.24		AN:M	Yes [ ] N/A [ ]
AM93	A write to the BASE-T1 AN LP Next Page ability register has no effect.	45.2.7.25		AN:M	Yes [ ] N/A [ ]
AM94	When bit 7.526.15 is set to one, the PHY advertises 10BASE-T1L capability	45.2.7.26.1		AN:M	Yes [ ] N/A [ ]
AM95	When bit 7.526.15 is set to zero, the PHY does not advertise 10BASE-T1L capability	45.2.7.26.1		AN:M	Yes [ ] N/A [ ]
AM96	If a 10BASE-T1L PHY supports EEE ability and desires to operate in EEE mode, bit 7.526.14 is set to one	45.2.7.26.2		AN:M	Yes [ ] N/A [ ]
AM97	If a 10BASE-T1L PHY supports the 2.4 Vpp operating mode, bit 7.526.13 is set to one	45.2.7.26.3		AN:M	Yes [ ] N/A [ ]
AM98	When bit 7.526.12 is set to one, a request to operate the 10BASE-T1L PHY in increased transmit level mode is advertised	45.2.7.26.4		AN:M	Yes [ ] N/A [ ]
AM99	When bit 7.526.12 is set to zero, a request to operate the 10BASE-T1L PHY in increased transmit level mode is not advertised	45.2.7.26.4		AN:M	Yes [ ] N/A [ ]
AM100	When bit 7.526.7 is set to one, the PHY advertises 10BASE-T1S full duplex ability	45.2.7.26.5		AN:M	Yes [ ] N/A [ ]
AM101	When bit 7.526.7 is set to zero, the PHY does not advertise 10BASE-T1S full duplex ability	45.2.7.26.5		AN:M	Yes [ ] N/A [ ]
AM102	When bit 7.526.6 is set to one, the PHY advertises 10BASE-T1S half duplex capability	45.2.7.26.6		AN:M	Yes [ ] N/A [ ]
AM103	When bit 7.526.6 is set to zero, the PHY does not advertise 10BASE-T1S half duplex capability	45.2.7.26.6		AN:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
AM104	Writing to the 10BASE-T1 AN status register has no effect	45.2.7.27		AN:M	Yes [ ] N/A [ ]
AM105	When the AN process is complete, the 10BASE-T1 AN status register reflects the contents of the link partner's 10BASE-T1 AN control register	45.2.7.27		AN:M	Yes [ ] N/A [ ]

45.5.3.10 PHY XS options

Item	Feature	Subclause	Value/Comment	Status	Support
*PL	Implementation of loopback	45.2.4		PX:O	Yes [ ] No [ ] N/A [ ]
*PT	Implementation of pattern testing	45.2.4		PX:O	Yes [ ] No [ ] N/A [ ]

45.5.3.11 PHY XS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
PM1	Device responds to all register addresses for that device	45.2		PX:M	Yes [ ] N/A [ ]
PM2	Writes to undefined and read-only registers have no effect	45.2		PX:M	Yes [ ] N/A [ ]
PM3	Operation is not affected by writes to reserved and unsupported bits	45.2		PX:M	Yes [ ] N/A [ ]
PM4	Reserved and unsupported bits return a value of zero	45.2		PX:M	Yes [ ] N/A [ ]
PM5	Latching low bits remain low until after they have been read via the management interface	45.2		PX:M	Yes [ ] N/A [ ]
PM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PX:M	Yes [ ] N/A [ ]
PM7	Latching high bits remain high until after they have been read via the management interface	45.2		PX:M	Yes [ ] N/A [ ]
PM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PX:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PM9	Action on reset	45.2.4.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PX:M	Yes [ ] N/A [ ]
PM10	Return 1 until reset completed	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM11	Reset completes within 0.5 s	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM12	Device responds to reads of bits 4.0.15 and 4.8.15:14 during reset	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM13	Loopback mode	45.2.4.1.2	Whenever bit 4.0.14 is set to a one	PX*PL:M	Yes [ ] N/A [ ]
PM14	Receive data is returned on transmit path during loopback	45.2.4.1.2		PX*PL:M	Yes [ ] N/A [ ]
PM15	Writes to loopback bit are ignored and reads return zero	45.2.4.1.2		PX*!PL:M	Yes [ ] N/A [ ]
PM16	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.4.1.3		PX:M	Yes [ ] N/A [ ]
PM17	Speed selection bits 13 and 6 are written as one	45.2.4.1.6		PX:M	Yes [ ] N/A [ ]
PM18	Invalid writes to speed selection bits are ignored	45.2.4.1.6		PX:M	Yes [ ] N/A [ ]
PM19	Writes to status 1 register have no effect	45.2.4.2		PX:M	Yes [ ] N/A [ ]
PM20	Transmit link status implemented using latching low behavior	45.2.4.2.7		PX:M	Yes [ ] N/A [ ]
PM21	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.4.3		PX:M	Yes [ ] N/A [ ]
PM22	Writes to status 2 register have no effect	45.2.4.6		PX:M	Yes [ ] N/A [ ]
PM23	Transmit fault implemented with latching high behavior	45.2.4.6.2		PX:M	Yes [ ] N/A [ ]
PM24	Receive fault implemented with latching high behavior	45.2.4.6.3		PX:M	Yes [ ] N/A [ ]
PM25	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.4.7		PX:M	Yes [ ] N/A [ ]
PM26	Writes to 10G PHY XGXS Lane status register have no effect	45.2.4.10		PX:M	Yes [ ] N/A [ ]
PM27	Writes to bit are ignored and reads return a value of zero	45.2.4.11.1		PX*!PT:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PM28	Setting the bits to <10> selects the mixed frequency pattern	45.2.4.11.2		PX*PT:M	Yes [ ] N/A [ ]
PM29	Setting the bits to <01> selects the low-frequency pattern	45.2.4.11.2		PX*PT:M	Yes [ ] N/A [ ]
PM30	Setting the bits to <00> selects the high-frequency pattern	45.2.4.11.2		PX*PT:M	Yes [ ] N/A [ ]

45.5.3.12 DTE XS options

Item	Feature	Subclause	Value/Comment	Status	Support
*DT	Implementation of pattern testing	45.2.5		DX:O	Yes [ ] No [ ] N/A [ ]

45.5.3.13 DTE XS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
DM1	Device responds to all register addresses for that device	45.2		DX:M	Yes [ ] N/A [ ]
DM2	Writes to undefined and read-only registers have no effect	45.2		DX:M	Yes [ ] N/A [ ]
DM3	Operation is not affected by writes to reserved and unsupported bits	45.2		DX:M	Yes [ ] N/A [ ]
DM4	Reserved and unsupported bits return a value of zero	45.2		DX:M	Yes [ ] N/A [ ]
DM5	Latching low bits remain low until after they have been read via the management interface	45.2		DX:M	Yes [ ] N/A [ ]
DM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	DX:M	Yes [ ] N/A [ ]
DM7	Latching high bits remain high until after they have been read via the management interface	45.2		DX:M	Yes [ ] N/A [ ]
DM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	DX:M	Yes [ ] N/A [ ]
DM9	Action on reset	45.2.5.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	DX:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DM10	Return 1 until reset completed	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM11	Reset completes within 0.5 s	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM12	Device responds to reads of bits 5.0.15 and 5.8.15:14 during reset	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM13	Loopback mode	45.2.5.1.2	Whenever bit 5.0.14 is set to a one	DX:M	Yes [ ] N/A [ ]
DM14	Transmit data is returned on receive path during loopback	45.2.5.1.2		DX:M	Yes [ ] N/A [ ]
DM15	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.5.1.3		DX:M	Yes [ ] N/A [ ]
DM16	Speed selection bits 13 and 6 are written as one	45.2.5.1.6		DX:M	Yes [ ] N/A [ ]
DM17	Invalid writes to speed selection bits are ignored	45.2.5.1.6		DX:M	Yes [ ] N/A [ ]
DM18	Writes to status 1 register have no effect	45.2.5.2		DX:M	Yes [ ] N/A [ ]
DM19	Receive link status implemented using latching low behavior	45.2.5.2.7		DX:M	Yes [ ] N/A [ ]
DM20	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.5.3		DX:M	Yes [ ] N/A [ ]
DM21	Writes to status 2 register have no effect	45.2.5.6		DX:M	Yes [ ] N/A [ ]
DM22	Transmit fault implemented with latching high behavior	45.2.5.6.2		DX:M	Yes [ ] N/A [ ]
DM23	Receive fault implemented with latching high behavior	45.2.5.6.3		DX:M	Yes [ ] N/A [ ]
DM24	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.5.7		DX:M	Yes [ ] N/A [ ]
DM25	Writes to 10G DTE XGXS Lane status register have no effect	45.2.5.10		DX:M	Yes [ ] N/A [ ]
DM26	Writes to bit are ignored and reads return a value of zero	45.2.5.11.1		DX*!DT:M	Yes [ ] N/A [ ]
DM27	Setting the bits to <10> selects the mixed frequency pattern	45.2.5.11.2		DX*DT:M	Yes [ ] N/A [ ]
DM28	Setting the bits to <01> selects the low-frequency pattern	45.2.5.11.2		DX*DT:M	Yes [ ] N/A [ ]
DM29	Setting the bits to <00> selects the high-frequency pattern	45.2.5.11.2		DX*DT:M	Yes [ ] N/A [ ]

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45.5.3.14 OFDM management functions

Item	Feature	Subclause	Value/Comment	Status	Support
OFM1	Implementation of 10GPASS-XR DS OFDM channel ID	45.2.8.1		EO:M	Yes [ ] N/A [ ]
OFM2	Implementation of 10GPASS-XR DS profile descriptor control	45.2.8.2		EO:M	Yes [ ] N/A [ ]
OFM3	Implementation of 10GPASS-XR US profile descriptor control	45.2.8.3		EO:M	Yes [ ] N/A [ ]
OFM4	Implementation of 10GPASS-XR US pre-equalizer coefficients	45.2.8.4		EO:M	Yes [ ] N/A [ ]
OFM5	Implementation of 10GPASS-XR receive MER control	45.2.8.5		EO:M	Yes [ ] N/A [ ]
OFM6	Implementation of 10GPASS-XR receive MER measurement	45.2.8.6		EO:M	Yes [ ] N/A [ ]

45.5.3.15 Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet management functions

Item	Feature	Subclause	Value/Comment	Status	Support
PODLM1	PSE Enable bit	45.2.9.1.2	PSE function enabled when set to one and disabled when set to zero	PODL: M	Yes [ ] N/A[ ]
PODLM2	Power Denied bit	45.2.9.2.1	Implemented with latching high behavior and set to one when power_available transitions from true to false	PODL: M	Yes [ ] N/A[ ]
PODLM3	Valid Signature bit	45.2.9.2.2	Implemented with latching high behavior and set to one when mr_valid_signature transitions from false to true	PODL: M	Yes [ ] N/A[ ]
PODLM4	Invalid Signature bit	45.2.9.2.3	Implemented with latching high behavior and set to one when mr_valid_signature transitions from false to true	PODL: M	Yes [ ] N/A[ ]
PODLM5	Class Timeout bit	45.2.9.2.4	Implemented with latching high behavior and set to one when tclass_timer_done transitions from false to true	PODL: M	Yes [ ] N/A[ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PODLM6	Overload bit	45.2.9.2.5	Implemented with latching high behavior and set to one when overload_held transitions from false to true	PODL: M	Yes [ ] N/A[ ]
PODLM7	MFVS Absent bit	45.2.9.2.6	Implemented with latching high behavior and set to one when mfvs_timeout transitions from false to true	PODL: M	Yes [ ] N/A[ ]
PODLM8	Invalid Class bit	45.2.9.3.1	Implemented with latching high behavior as defined in 45.2	PODL: M	Yes [ ] N/A[ ]

45.5.3.16 Vendor specific MMD 1 management functions

Item	Feature	Subclause	Value/Comment	Status	Support
VSA1	Device responds to all register addresses for that device	45.2		VSA:M	Yes [ ] N/A [ ]
VSA2	Writes to undefined and read-only registers have no effect	45.2		VSA:M	Yes [ ] N/A [ ]
VSA3	Operation is not affected by writes to reserved and unsupported bits	45.2		VSA:M	Yes [ ] N/A [ ]
VSA4	Reserved and unsupported bits return a value of zero	45.2		VSA:M	Yes [ ] N/A [ ]
VSA5	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.11.1		VSA:M	Yes [ ] N/A [ ]
VSA6	Writes to status register have no effect	45.2.11.2		VSA:M	Yes [ ] N/A [ ]
VSA7	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.11.3		VSA:M	Yes [ ] N/A [ ]

45.5.3.17 Vendor specific MMD 2 management functions

Item	Feature	Subclause	Value/Comment	Status	Support
VSB1	Device responds to all register addresses for that device	45.2		VSB:M	Yes [ ] N/A [ ]
VSB2	Writes to undefined and read-only registers have no effect	45.2		VSB:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
VSB3	Operation is not affected by writes to reserved and unsupported bits	45.2		VSB:M	Yes [ ] N/A [ ]
VSB4	Reserved and unsupported bits return a value of zero	45.2		VSB:M	Yes [ ] N/A [ ]
VSB5	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.12.1		VSB:M	Yes [ ] N/A [ ]
VSB6	Writes to status register have no effect	45.2.12.2		VSB:M	Yes [ ] N/A [ ]
VSB7	Unique identifier is composed of 22 bits of OUI, model number and revision	45.2.12.3		VSB:M	Yes [ ] N/A [ ]

45.5.3.18 Management frame structure

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Device has implemented sixteen bit address register	45.3		M	Yes [ ]
MF2	Address register is overwritten by address frames	45.3		M	Yes [ ]
MF3	Write, read, and post-read-increment-address frames access the register whose address is held in the address register	45.3		M	Yes [ ]
MF4	Write and read frames do not modify the address register	45.3		M	Yes [ ]
MF5	Post-read-increment-address frames increment the address register by one unless the address register contains 65 535	45.3		M	Yes [ ]
MF6	Components containing several MMDs implement separate address registers	45.3		M	Yes [ ]
MF7	Tri state drivers are disabled during idle	45.3.1		M	Yes [ ]
MF8	STA sources 32 contiguous ones at the beginning of each transaction	45.3.2		M	Yes [ ]
MF9	MMD observes 32 contiguous ones at the beginning of each transaction	45.3.2		M	Yes [ ]
MF10	Frames containing ST=<01> sequence are ignored	45.3.3		M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MF11	STA tri state driver is high impedence during first bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF12	MMD tri state driver is high impedence during first bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF13	MMD tri state driver drives a zero bit during second bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF14	STA tri state driver drives a one bit followed by a zero bit for the TA during write or address frames	45.3.7		M	Yes [ ]
MF15	First bit transmitted and received is bit 15	45.3.8		M	Yes [ ]

45.5.3.19 TC management functions

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Device responds to all register addresses for that device	45.2		TC:M	Yes [ ] N/A [ ]
TC2	Writes to undefined and read only register have no effect	45.2		TC:M	Yes [ ] N/A [ ]
TC3	Operation is not affected by writes to reserved and unsupported bits	45.2		TC:M	Yes [ ] N/A [ ]
TC4	Reserved and unsupported bits return a value of zero	45.2		TC:M	Yes [ ] N/A [ ]
TC5	Setting bit to a one sets all TC registers to their default states	45.2.6.1.1		TC:M	Yes [ ] N/A [ ]
TC6	Bit reads one while reset is in progress otherwise reads zero	45.2.6.1.1		TC:M	Yes [ ] N/A [ ]
TC7	Control and management interface is restored within 0.5s from setting bit to a one	45.2.6.1.1		TC:M	Yes [ ] N/A [ ]
TC8	During reset, TC responds to reads from bit	45.2.6.1.1		TC:M	Yes [ ] N/A [ ]
TC9	Writes that would select an unsupported speed are ignored	45.2.6.1.2		TC:M	Yes [ ] N/A [ ]
TC10	Identifier composed properly	45.2.6.2		TC:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC11	Identifier composed properly	45.2.6.5		TC:M	Yes [ ] N/A [ ]
TC12	Register is unique across all PCS MMDs in a package	45.2.6.6		TC:M	Yes [ ] N/A [ ]
TC13	Operation ignored when link is up or initializing	45.2.6.6.1		TC:M	Yes [ ] N/A [ ]
TC14	Bits indicate “Ready” when PAF is capable	45.2.6.6.1		TC:M	Yes [ ] N/A [ ]
TC15	Writes ignored and “Ready” indicated if PAF is unsupported	45.2.6.6.1		TC:M	Yes [ ] N/A [ ]
TC16	Bits indicate “Ready” when operation is complete or upon reset	45.2.6.6.1		TC:M	Yes [ ] N/A [ ]
TC17	Bits read as zero if PAF is unsupported	45.2.6.7.1		TC:M	Yes [ ] N/A [ ]
TC18	Bits read as zero if PAF is unsupported	45.2.6.7.2		TC:M	Yes [ ] N/A [ ]
TC19	Register is unique across all PCS MMDs in a package	45.2.6.8		TC:M	Yes [ ] N/A [ ]
TC20	Register is unique across all PCS MMDs in a package	45.2.6.9		TC:M	Yes [ ] N/A [ ]
TC21	Operation ignored when link is up or initializing	45.2.6.9.1		TC:M	Yes [ ] N/A [ ]
TC22	Bits indicate “Ready” when PAF is capable	45.2.6.9.1		TC:M	Yes [ ] N/A [ ]
TC23	Writes ignored and “Ready” indicated if PAF is unsupported	45.2.6.9.1		TC:M	Yes [ ] N/A [ ]
TC24	Bits indicate “Ready” when operation is complete or on reset	45.2.6.9.1		TC:M	Yes [ ] N/A [ ]
TC25	Register is unique across all PCS MMDs in a package	45.2.6.10		TC:M	Yes [ ] N/A [ ]
TC26	Bits reset to zero when read or reset	45.2.6.11		TC:M	Yes [ ] N/A [ ]
TC27	Bits held to one upon overflow	45.2.6.11		TC:M	Yes [ ] N/A [ ]
TC28	Bits reset to zero when read or reset	45.2.6.12		TC:M	Yes [ ] N/A [ ]
TC29	Bits held to one upon overflow	45.2.6.12		TC:M	Yes [ ] N/A [ ]

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45.5.3.20 Clause 22 extension options

Item	Feature	Subclause	Value/Comment	Status	Support
*FEC	Implementation of PHY FEC	65.4.4.6		CTT:O	Yes [ ] No [ ] N/A [ ]

45.5.3.21 Clause 22 extension management functions

Item	Feature	Subclause	Value/Comment	Status	Support
CT1	Device responds to all register addresses for that device	45.2		CTT:M	Yes [ ] N/A [ ]
CT2	Writes to undefined and read only register have no effect	45.2		CTT:M	Yes [ ] N/A [ ]
CT3	Operation is not affected by writes to reserved and unsupported bits	45.2		CTT:M	Yes [ ] N/A [ ]
CT4	Reserved and unsupported bits return a value of zero	45.2		CTT:M	Yes [ ] N/A [ ]
CT5	Bits set to zero upon PHY reset	45.2.10.3.1		CTT*FEC:M	Yes [ ] N/A [ ]
CT6	Bits reset to all zeros when the register is read by the management function or upon PHY reset.	45.2.10.4		CTT*FEC:M	Yes [ ] N/A [ ]
CT7	Bits held at all ones in the case of overflow	45.2.10.4		CTT*FEC:M	Yes [ ] N/A [ ]
CT8	Bits reset to all zeros when the register is read by the management function or upon PHY reset.	45.2.10.5		CTT*FEC:M	Yes [ ] N/A [ ]
CT9	Bits held at all ones in the case of overflow	45.2.10.5		CTT*FEC:M	Yes [ ] N/A [ ]
CT10	Bits reset to all zeros when the register is read by the management function or upon PHY reset.	45.2.10.6		CTT*FEC:M	Yes [ ] N/A [ ]
CT11	Bits held at all ones in the case of overflow	45.2.10.6		CTT*FEC:M	Yes [ ] N/A [ ]

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45.5.3.22 Signal timing characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
ST1	MDIO setup and hold time	45.4.2	Setup min = 10 ns; Hold min = 10 ns per Figure 45–3	M	Yes [ ]
ST2	MDIO clock to output delay	45.4.2	Min = 0 ns; Max = 300 ns per Figure 45–4	M	Yes [ ]
ST3	MDC min high/low time	45.4.2	160 ns	M	Yes [ ]
ST4	MDC min period	45.4.2	400 ns	M	Yes [ ]

45.5.3.23 Electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
EC1	V_{OH}	45.4.1	≥ 1.0 V (I_{OH} = –100 uA) ≤ 1.5 V (I_{OH} = –100 uA)	M	Yes [ ]
EC2	V_{OL}	45.4.1	≥ –0.3 V (I_{OL} = 100 uA) ≤ 0.2 V (I_{OL} = 100 uA)	M	Yes [ ]
EC3	V_{IH}	45.4.1	0.84 V ≤ V_{IH} ≤ 1.5 V	M	Yes [ ]
EC4	V_{IL}	45.4.1	–0.3 ≤ V_{IL} ≤ 0.36 V	M	Yes [ ]
EC5	Input capacitance for MDIO	45.4.1	≤ 10 pF	M	Yes [ ]
EC6	Total capacitive load	45.4.1	≤ 470 pF	M	Yes [ ]
EC7	I_{OH}	45.4.1	≤ –4 mA at V_{OH} = 1.0 V	!ODB:M	Yes [ ] N/A[ ]
EC8	I_{OL}	45.4.1	≥ +4 mA at V_{OL} = 0.2 V	M	Yes [ ]

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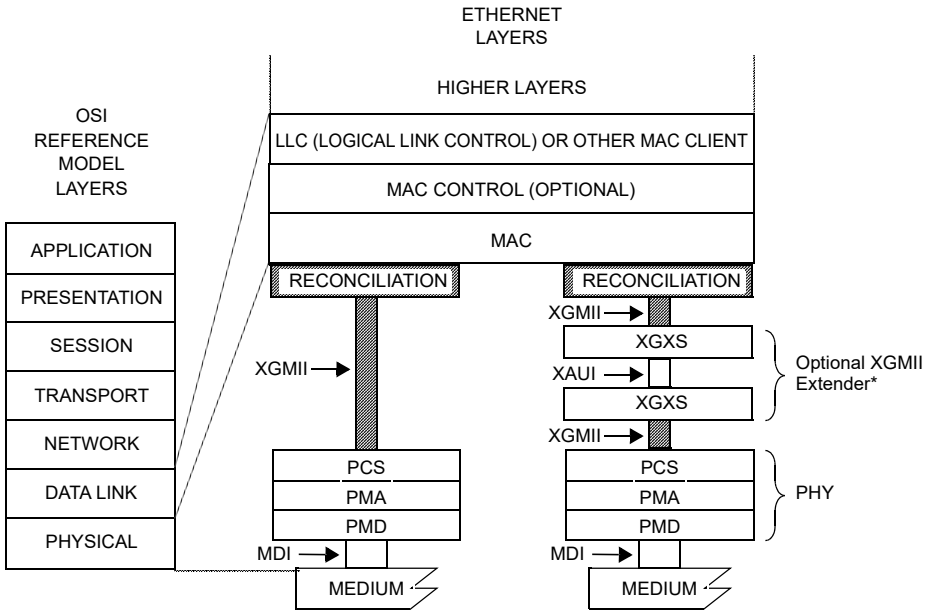
46. Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

46.1 Overview

This clause defines the logical and electrical characteristics for the Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII) between Ethernet media access controllers and various PHYs. Figure 46–1 shows the relationship of the RS and XGMII to the ISO/IEC (IEEE) OSI reference model.



MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XAUI = 10 GIGABIT ATTACHMENT UNIT INTERFACE
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
XGXS = XGMII EXTENDER SUBLAYER

*specified in Clause 47

Figure 46–1—XGMII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The purpose of the XGMII is to provide a simple, inexpensive, and easy-to-implement interconnection between the Media Access Control (MAC) sublayer and the Physical Layer device (PHY). The 10 Gigabit Attachment Unit Interface (XAUI) may optionally be used to extend the operational distance of the XGMII with reduced pin count (see Clause 47).

The RS adapts the bit serial protocols of the MAC to the parallel encodings of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s PHYs. Though the XGMII is an optional interface, it is used extensively in this standard as a basis for specification. The 2.5 Gb/s, 5 Gb/s, and 10 Gb/s Physical Coding Sublayers (PCS) are specified to the XGMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and XGMII were implemented.

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The XGMII has the following characteristics:

a) It is capable of supporting at least one of the following rates of operation: 2.5 Gb/s, 5 Gb/s, or 10 Gb/s.
b) Data and delimiters are synchronous to clock reference.
c) It provides independent 32-bit-wide transmit and receive data paths.
d) It uses signal levels compatible with common digital ASIC processes.
e) It provides for full duplex operation only.

46.1.1 Summary of major concepts

The following are the major concepts of XGMII:

a) The XGMII is functionally similar to the MII defined in Clause 22 and GMII defined in Clause 35 as they all define an interface allowing independent development of MAC and PHY logic.
b) The RS converts between the MAC serial data stream and the parallel data paths of the XGMII.
c) The RS maps the signal set provided at the XGMII to the PLS service primitives provided at the MAC.
d) Each direction of data transfer is independent and serviced by data, control, and clock signals.
e) The RS generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.
f) The RS participates in link fault detection and reporting by monitoring the receive path for status reports that indicate an unreliable link, and generating status reports on the transmit path to report detected link faults to the DTE on the remote end of the connecting link.
g) When the XGMII is optionally extended with XAUI, two XGMII interfaces logically exist (see Figure 46–1). The transmit path signals are from the RS to the DTE (top) XGXS of the XAUI via one XGMII and from the PHY (bottom) XGXS to the PCS via the other XGMII. The receive path signals are from the PCS to the PHY XGXS of the XAUI via one XGMII and from the DTE XGXS to the RS via the other XGMII. The descriptions of the XGMII as between the RS and the PCS are, therefore, equally applicable between the RS and the DTE XGXS or the PHY XGXS and the PCS.
h) The XGMII may also support Low Power Idle (LPI) signaling for PHY types supporting Energy-Efficient Ethernet (EEE) (see Clause 78).
i) The XGMII is rate scalable and may support rates of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s.

46.1.2 Application

This clause applies to the interface between the MAC and PHY. The physical implementation of the interface is primarily intended as a chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board. The XGMII may also be used in other ways, for example, as a logical interface between ASIC logic modules within an integrated circuit.

This interface is used to provide media independence so that an identical media access controller may be used with all 2.5GBASE, 5GBASE, and 10GBASE PHY types.

46.1.3 Rate of operation

The XGMII supports MAC data rates of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s as defined within this clause. A compliant device may implement any subset of these rates. Operation at 10 Mb/s and 100 Mb/s is supported by the MII defined in Clause 22 and operation at 1000 Mb/s by the GMII defined in Clause 35.

10GBASE-X and 10GBASE-R PHYs operate at a 10 Gb/s data rate. 10GBASE-W PHYs operate at the STS-192/VC-4-64c line rate of 9.95328 Gb/s, mapping the encoded data stream at a 9.58464 Gb/s payload rate. On transmit, this mapping is performed by discarding Idle control characters corresponding to the

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stretched interpacket gap created by the MAC in this mode of operation, and on receive, by adding interpacket gap Idle control characters as required to adapt to the XGMII RX_CLK rate.

46.1.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. The maximum cumulative MAC Control, MAC and RS round-trip (sum of transmit and receive) delay shall meet the values specified in Table 46–1. Bit time is specified in 1.4, and pause_quanta is specified in 31B.2.

Table 46–1—Round-trip delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)
MAC, RS, and MAC Control	8192	16

46.1.5 Allocation of functions

The allocation of functions at the XGMII balances the need for media independence with the need for a simple and cost-effective interface. The bus width and signaling rate are applicable to short distance chip-to-chip interconnect with printed circuit board trace lengths electrically limited to approximately 7 cm. The XGMII (like the MII and GMII) maximizes media independence by cleanly separating the Data Link and Physical Layers of the ISO (IEEE) seven-layer reference model. This allocation also recognizes that implementations can benefit from a close coupling between the PLS sublayer or PCS and the PMA sublayer.

46.1.6 XGMII structure

The XGMII is composed of independent transmit and receive paths. Each direction uses 32 data signals (TXD<31:0> and RXD<31:0>), four control signals (TXC<3:0> and RXC<3:0>), and a clock (TX_CLK and RX_CLK). Figure 46–2 depicts a schematic view of the RS inputs and outputs.

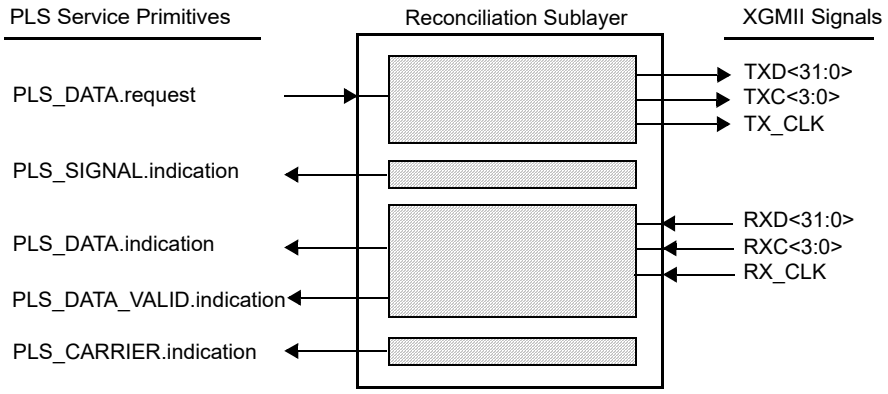

Figure 46–2—Reconciliation Sublayer (RS) inputs and outputs

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The 32 TXD and four TXC signals shall be organized into four data lanes, as shall the 32 RXD and four RXC signals (see Table 46–2). The four lanes in each direction share a common clock—TX_CLK for transmit and RX_CLK for receive. The four lanes are used in round-robin sequence to carry an octet stream. On transmit, each eight PLS_DATA.request transactions represent an octet transmitted by the MAC. The first octet is aligned to lane 0, the second to lane 1, the third to lane 2 the fourth to lane 3, then repeating with the fifth to lane 0, etc. Delimiters and interframe idle characters are encoded on the TXD and RXD signals with the control code indicated by assertion of TXC and RXC, respectively.

Table 46–2—Transmit and receive lane associations

TXD RXD	TXC RXC	Lane
<7:0>	<0>	0
<15:8>	<1>	1
<23:16>	<2>	2
<31:24>	<3>	3

46.1.7 Mapping of XGMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the XGMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 2.5 Gb/s, 5 Gb/s, and 10 Gb/s; therefore, PLS service primitives supporting CSMA/CD operation are not mapped through the RS to the XGMII. The mapping is changed if EEE capability is supported (see 78.3). This behavior and restrictions are the same as described in 22.7, with the details of the signaling described in 46.3. LPI_REQUEST shall not be set to ASSERT unless the attached link has been operational for at least one second (i.e., link_status = OK, according to the underlying PCS/PMA).

EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

Mappings for the following primitives are defined for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation:

PLS_DATA.request
PLS_DATA.indication
PLS_CARRIER.indication
PLS_SIGNAL.indication
PLS_DATA_VALID.indication

46.1.7.1 Mapping of PLS_DATA.request

46.1.7.1.1 Function

Map the primitive PLS_DATA.request to the XGMII signals TXD<31:0>, TXC<3:0>, and TX_CLK.

46.1.7.1.2 Semantics of the service primitive

PLS_DATA.request (OUTPUT_UNIT)

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The OUTPUT_UNIT parameter can take one of three values: ONE, ZERO, or DATA_COMPLETE. It represents a single data bit. The DATA_COMPLETE value signifies that the Media Access Control sublayer has no more data to output.

46.1.7.1.3 When generated

This primitive is generated by the MAC sublayer to request the transmission of a single data bit on the physical medium or to stop transmission.

46.1.7.1.4 Effect of receipt

The OUTPUT_UNIT values are conveyed to the PHY by the signals TXD<31:0> and TXC<3:0> on each TX_CLK edge. Each PLS_DATA.request transaction shall be mapped to a TXD signal in sequence (TXD<0>, TXD<1>,... TXD<31>, TXD<0>) as described in 46.2. After 32 PLS_DATA.request transactions from the MAC sublayer (four octets of eight PLS_DATA.request transactions each), the RS requests transmission of 32 data bits by the PHY. The first octet of preamble shall be converted to a Start control character and aligned to lane 0. The TXD<31:0> and TXC<3:0> shall be generated by the RS for each 32 bit-times of the MAC sublayer.

The DATA_COMPLETE value shall be mapped to a Terminate control character encoded on the next eight TXD signals in sequence after the last data octet; and is transferred to the PHY at the next TX_CLK edge. This may be on the same TX_CLK edge as the last data octet or the subsequent TX_CLK edge. When the Terminate control character is in lane 0, 1, or 2, the lanes following in sequence are encoded with an Idle control character.

46.1.7.2 Mapping of PLS_DATA.indication

46.1.7.2.1 Function

Map the primitive PLS_DATA.indication to the XGMII signals RXD<31:0>, RXC<3:0> and RX_CLK.

46.1.7.2.2 Semantics of the service primitive

PLS_DATA.indication (INPUT_UNIT)

The INPUT_UNIT parameter can take one of two values: ONE or ZERO. It represents a single data bit.

46.1.7.2.3 When generated

The INPUT_UNIT values are derived from the signals RXC<3:0> and RXD<31:0> received from the PHY on each edge of RX_CLK. Each primitive generated to the MAC sublayer entity corresponds to a PLS_DATA.request issued by the MAC at the remote end of the link connecting two DTEs. For each RXD<31:0> during frame reception, the RS shall generate 32 PLS_DATA.indication transactions until the end of frame (Terminate control character), where 0, 8, 16, or 24 PLS_DATA.indication transactions will be generated from the RXD<31:0> containing the Terminate. During frame reception, each RXD signal shall be mapped in sequence into a PLS_DATA.indication transaction (RXD<0>, RXD<1>,... RXD<31>, RXD<0>) as described in 46.2.

The RS shall convert a valid Start control character to a preamble octet prior to generation of the associated PLS_DATA.indication transactions. The RS shall not generate any PLS_DATA.indication primitives for a Terminate control character. To assure robust operation, the value of the data transferred to the MAC may be changed by the RS as required by XGMII error indications (see 46.3.3). Sequence ordered sets are not indicated to the MAC (see 46.3.4).

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46.1.7.2.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is unspecified.

46.1.7.3 Mapping of PLS_CARRIER.indication

2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation supports full duplex operation only. The RS never generates this primitive for PHYs that do not support EEE or Link Interruption.

For PHYs that support EEE capability, CARRIER_STATUS is set in response to LPI_REQUEST as shown in Figure 46–13. For PHYs that support Link Interruption, CARRIER_STATUS may be set in response to link_fault. CARRIER_STATUS is set to CARRIER_ON if LPI_CARRIER_STATUS is TRUE or if link_fault is Link Interruption. CARRIER_STATUS is otherwise set to CARRIER_OFF. The deferral mechanism based upon the Link Interruption signal may be enabled or disabled by management.

46.1.7.4 Mapping of PLS_SIGNAL.indication

2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation supports full duplex operation only. The RS never generates this primitive.

46.1.7.5 Mapping of PLS_DATA_VALID.indication

46.1.7.5.1 Function

Map the primitive PLS_DATA_VALID.indication to the XGMII signals RXC<3:0> and RXD<31:0>.

46.1.7.5.2 Semantics of the service primitive

PLS_DATA_VALID.indication (DATA_VALID_STATUS)

The DATA_VALID_STATUS parameter can take one of two values: DATA_VALID or DATA_NOT_VALID. The DATA_VALID value indicates that the INPUT_UNIT parameter of the PLS_DATA.indication primitive contains a valid data of an incoming frame. The DATA_NOT_VALID value indicates that the INPUT_UNIT parameter of the PLS_DATA.indication primitive does not contain valid data of an incoming frame.

46.1.7.5.3 When generated

The PLS_DATA_VALID.indication service primitive shall be generated by the RS whenever the DATA_VALID_STATUS parameter changes from DATA_VALID to DATA_NOT_VALID or vice versa.

DATA_VALID_STATUS shall assume the value DATA_VALID when a PLS_DATA.indication transaction is generated in response to reception of a Start control character on lane 0 if the prior RXC<3:0> and RXD<31:0> contained four Idle characters or a Sequence ordered set. DATA_VALID_STATUS shall assume the value DATA_NOT_VALID when RXC of the current lane in sequence is asserted for anything except an Error control character. In the absence of errors, DATA_NOT_VALID is caused by a Terminate control character. When DATA_VALID_STATUS changes from DATA_VALID to DATA_NOT_VALID because of a control character other than Terminate, the RS shall ensure that the MAC will detect a FrameCheckError prior to indicating DATA_NOT_VALID to the MAC (see 46.3.3.1).

46.1.7.5.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is unspecified.

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46.2 XGMII data stream

Packets transmitted through the XGMII shall be transferred within the XGMII data stream. The data stream is a sequence of bytes, where each byte conveys either a data octet or control character. The parts of the data stream are shown in Figure 46–3.

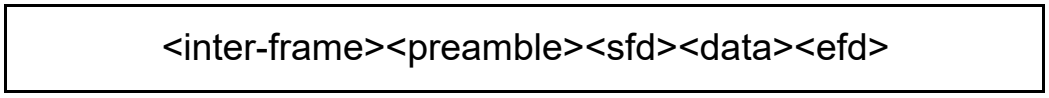

Figure 46–3—XGMII data stream

For the XGMII, transmission and reception of each bit and mapping of data octets to lanes shall be as shown in Figure 46–4.

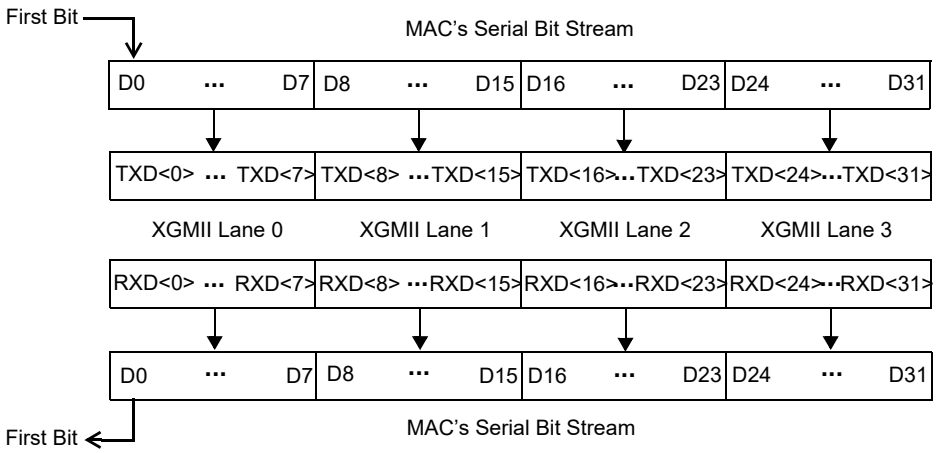

Figure 46–4—Relationship of data lanes to MAC serial bit stream

46.2.1 Inter-frame <inter-frame>

The inter-frame <inter-frame> period on an XGMII transmit or receive path is an interval during which no frame data activity occurs. The <inter-frame> corresponding to the MAC interpacket gap begins with the Terminate control character, continues with Idle control characters and ends with the Idle control character prior to a Start control character. The length of the interpacket gap may be changed between the transmitting MAC and receiving MAC by one or more functions (e.g., RS lane alignment, PHY clock rate compensation, or 10GBASE-W data rate adaptation functions). The minimum IPG at the XGMII of the receiving RS is five octets.

The signaling of link status information logically occurs in the <inter-frame> period (see 46.3.4). Subclause 46.3.3 describes frame processing when signaling of link status information is initiated or terminated.

46.2.2 Preamble <preamble> and start of frame delimiter <sfd>

The preamble <preamble> begins a frame transmission by a MAC as specified in 4.2.5 and when generated by a MAC consists of 7 octets with the following bit values:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

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The Start control character indicates the beginning of MAC data on the XGMII. On transmit, the RS converts the first data octet of preamble transferred from the MAC into a Start control character. On receive, the RS will convert the Start control character into a preamble data octet. The start control character is aligned to lane 0 of the XGMII by the RS on transmit and by the PHY on receive.

The start of frame delimiter <sfd> indicates the start of a frame and immediately follows the preamble. The bit value of <sfd> at the XGMII is unchanged from the Start Frame Delimiter (SFD) specified in 4.2.6 and is the bit sequence:

10101011

The preamble and SFD are shown previously with their bits ordered for serial transmission from left to right. As shown, the left-most bit of each octet is the LSB of the octet and the right-most bit of each octet is the MSB of the octet.

The preamble and SFD are transmitted through the XGMII as octets sequentially ordered on the lanes of the XGMII. The first preamble octet is replaced with a Start control character and it is aligned to lane 0, the second octet on lane 1, the third on lane 2 and the fourth on lane 3, and the four octets are transferred on the next edge of TX_CLK. The fifth octet is assigned to lane 0 with subsequent octets sequentially assigned to the lanes with the SFD assigned to lane 3. The XGMII <preamble> and <sfd> are as follows:

Lane 0	**Lane 1**	**Lane 2**	**Lane 3**
Start	10101010	10101010	10101010
10101010	10101010	10101010	10101011

46.2.3 Data <data>

The data <data> in a well-formed frame shall consist of a set of data octets.

46.2.4 End of frame delimiter <efd>

Assertion of TXC with the appropriate Terminate control character encoding of TXD on a lane constitutes an end of frame delimiter <efd> for the transmit data stream. Similarly, assertion of RXC with the appropriate Terminate control character encoding of RXD constitutes an end of frame delimiter for the receive data stream. The XGMII shall recognize the end of frame delimiter on any of the four lanes of the XGMII.

46.2.5 Definition of Start of Packet and End of Packet Delimiters

For the purposes of Clause 30, the Start of Packet delimiter is defined as the Start control character, and the End of Packet delimiter is defined as the end of the last sequential data octet preceding the Terminate control character or other control character causing a change from DATA_VALID to DATA_NOT_VALID. (See 46.1.7.5.2 and 30.3.2.1.5.)

46.3 XGMII functional specifications

The XGMII is designed to make the differences among the various media and transceiver combinations transparent to the MAC sublayer. The selection of logical control signals and the functional procedures are all designed to this end.

NOTE—No XGMII loopback is defined, but XGMII signals are specified such that transmit signals may be connected to receive signals to create a loopback path. To do this, TXD<0> is connected to RXD<0> ... TXD<31> to RXD<31>, TXC<0> to RXC<0> ... TXC<3> to RXC<3>, and TXCLK to RXCLK. Such a loopback does not test the Link Fault Signaling state diagram, nor any of the error handling functions of the receive RS.

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46.3.1 Transmit

46.3.1.1 TX_CLK (transmit clock)

TX_CLK is a continuous clock. TX_CLK provides the timing reference for the transfer of the TXC<3:0> and TXD<31:0> signals from the RS to the PHY. The values of TXC<3:0> and TXD<31:0> shall be sampled by the PHY on both the rising edge and falling edge of TX_CLK. TX_CLK is sourced by the RS.

The TX_CLK frequency shall be $1/64 \times f_{MAC} \pm 100$ ppm, where f_{MAC} is the frequency (in Hz) corresponding to the MAC's nominal bit rate.

NOTE—For EEE capability, TX_CLK may be halted according to 46.3.1.5.

46.3.1.2 TXC<3:0> (transmit control)

TXC<3:0> indicate that the RS is presenting either data or control characters on the XGMII for transmission. The TXC signal for a lane shall be de-asserted when a data octet is being sent on the corresponding lane and asserted when a control character is being sent. In the absence of errors, the TXC signals are de-asserted by the RS for each octet of the preamble (except the first octet that is replaced with a Start control character) and remain de-asserted while all octets to be transmitted are presented on the lanes of the XGMII. TXC<3:0> are driven by the RS and shall transition synchronously with respect to both the rising and falling edges of TX_CLK. Table 46–3 specifies the permissible encodings of TXD and TXC for a XGMII transmit lane. Additional requirements apply for proper code sequences and in which lanes particular codes are valid (e.g., Start control character is to be aligned to lane 0).

A PHY with EEE capability shall interpret the combination of TXC and TXD as shown in Table 46–3 as an assertion of LPI. Transition into and out of the LPI state is shown in Figure 46–7.

46.3.1.3 TXD<31:0> (transmit data)

TXD is a bundle of 32 data signals organized into four lanes of eight signals each (TXD<7:0>, TXD<15:8>, TXD<23:16>, and TXD<31:24>) that are driven by the RS. Each lane is associated with a TXC signal as shown in Table 46–2 and shall be encoded as shown in Table 46–3. TXD<31:0> shall transition synchronously with respect to both the rising and falling edges of TX_CLK. For each high or low TX_CLK transition, data and/or control are presented on TXD<31:0> to the PHY for transmission. TXD<0> is the least significant bit of lane 0, TXD<8> the least significant bit of lane 1, TXD<16> the least significant bit of lane 2, and TXD<24> the least significant bit of lane 3.

Assertion on a lane of appropriate TXD values when TXC is asserted will cause the PHY to generate code-groups associated with either Idle, Start, Terminate, Sequence, or Error control characters. While the TXC of a lane is de-asserted, TXD of the lane is used to request the PHY to generate code-groups corresponding to the data octet value of TXD. An example of normal frame transmission is illustrated in Figure 46–5.

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Table 46–3—Permissible encodings of TXC and TXD

TXC	TXD	Description	PLS_DATA.request parameter
0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	00 through 05	Reserved	—
1	06	Only valid on all four lanes simultaneously to request LPI	No applicable parameter (normal interframe)
1	07	Idle	No applicable parameter (Normal inter-frame)
1	08 through 9B	Reserved	—
1	9C	Sequence (only valid in lane 0)	No applicable parameter (Inter-frame status signal)
1	9D through FA	Reserved	—
1	FB	Start (only valid in lane 0)	No applicable parameter, replaces first eight ZERO, ONE of a frame (preamble octet)
1	FC	Reserved	—
1	FD	Terminate	DATA_COMPLETE
1	FE	Transmit error propagation	No applicable parameter
1	FF	Reserved	—
NOTE—Values in TXD column are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>).			

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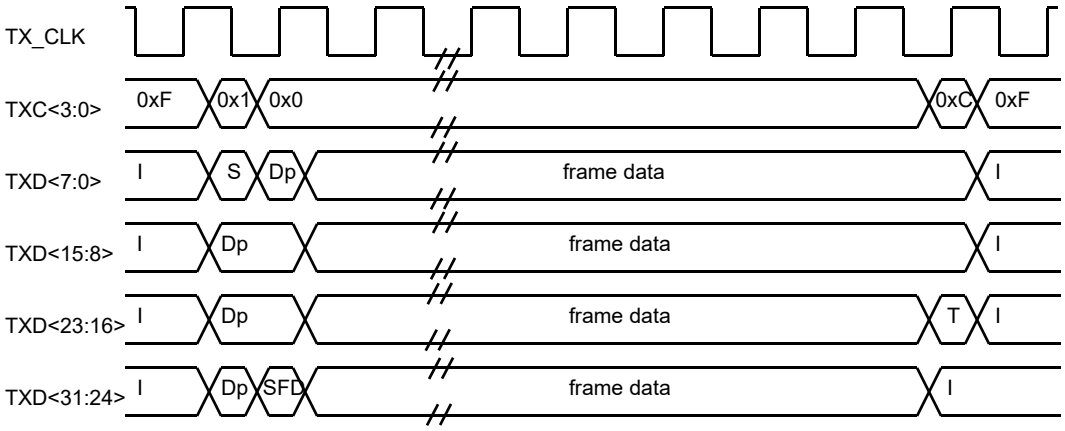
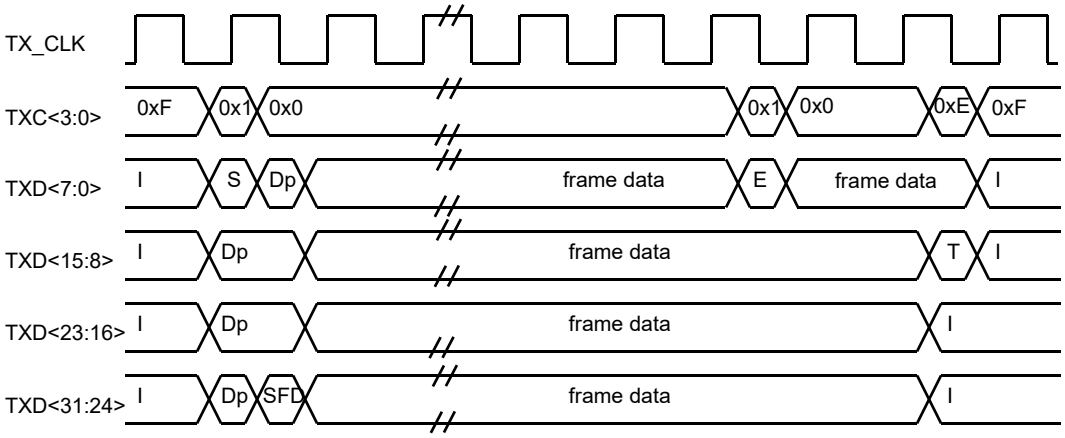
Figure 46–6 shows the behavior of TXD and TXC during an example transmission of a frame propagating an error.



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character

Figure 46–5—Normal frame transmission



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character, E: Error control character

Figure 46–6—Transmit Error Propagation

46.3.1.4 Start control character alignment

On transmit, it may be necessary for the RS to modify the length of the <inter-frame> in order to align the Start control character (first octet of preamble) on lane 0. This shall be accomplished in one of the following two ways:

1) A MAC implementation may incorporate this RS function into its design and always insert additional idle characters to align the start of preamble on a four byte boundary. Note that this will reduce the effective data rate for certain packet sizes separated with minimum inter-frame spacing.

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2) Alternatively, the RS may maintain the effective data rate by sometimes inserting and sometimes deleting idle characters to align the Start control character. When using this method the RS maintains a Deficit Idle Count (DIC) that represents the cumulative count of idle characters deleted or inserted. The DIC is incremented for each idle character deleted, decremented for each idle character inserted, and the decision of whether to insert or delete idle characters is constrained by bounding the DIC to a minimum value of zero and maximum value of three. Note that this may result in inter-frame spacing observed on the transmit XGMII that is up to three octets shorter than the minimum transmitted inter-frame spacing specified in Clause 4; however, the frequency of shortened inter-frame spacing is constrained by the DIC rules. The DIC is only reset at initialization and is applied regardless of the size of the IPG transmitted by the MAC sublayer. An equivalent technique may be employed to control RS alignment of the Start control character provided that the result is the same as if the RS implemented DIC as described.

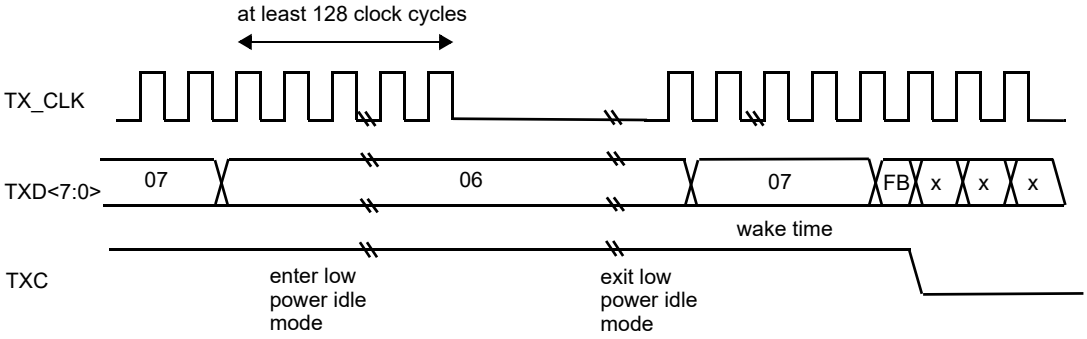
46.3.1.5 Transmit direction LPI transition

LPI operation and the LPI client are described in 78.1. The RS requests the PHY to transition to the LPI state by asserting TXC and setting TXD to 0x06 (in all lanes). The RS maintains the same state for these signals for the entire time that the PHY is to remain in the LPI state.

The RS may halt TX_CLK at any time more than 128 clock cycles after the start of the LPI state as shown in Figure 46–7 if the clock stop capable bit of the attached sublayer is asserted (see 45.2.3.2.1 and 45.2.5.2.1). It is the responsibility of the management entity to ensure that the RS does not halt the TX_CLK if the attached device does not have its stop clock capable bit set. The RS shall restart TX_CLK so that at least one positive transition occurs before it deaserts LPI.

The RS asserts TXC and asserts IDLE on lanes 0–3 in order to make the PHY transition out of the LPI state. The RS should not present a start code for valid transmit data until after the wake-up time specified for the PHY.

Figure 46–7 shows the behavior of TXC and TXD<7:0> during the transition into and out of the LPI state.



NOTE—TXC and TXD are shown for one lane, all four lanes behave identically during LPI.

Figure 46–7—LPI transition

Table 46–3 summarizes the permissible encodings of TXD<31:0>, TXC<3:0>.

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46.3.2 Receive

46.3.2.1 RX_CLK (receive clock)

RX_CLK is a continuous clock that provides the timing reference for the transfer of the RXC<3:0> and RXD<31:0> signals from the PHY to the RS. RXC<3:0> and RXD<31:0> shall be sampled by the RS on both the rising and falling edge of RX_CLK. RX_CLK is sourced by the PHY.

The frequency of RX_CLK may be derived from the received data or it may be that of a nominal clock (e.g., TX_CLK). When the received data rate at the PHY is within tolerance, the RX_CLK frequency shall be $1/64 \times f_{MAC} \pm 100$ ppm, where f_{MAC} is the frequency (in Hz) corresponding to the MAC's nominal bit rate.

There is no need to transition between the recovered clock reference and a nominal clock reference on a frame-by-frame basis. If loss of received signal from the medium causes a PHY to lose the recovered RX_CLK reference, the PHY shall source the RX_CLK from a nominal clock reference. Transitions from nominal clock to recovered clock or from recovered clock to nominal clock shall not decrease the time between adjacent edges of RX_CLK.

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. For EEE capability, RX_CLK may be halted according to 46.3.2.4.

46.3.2.2 RXC<3:0> (receive control)

RXC<3:0> indicate that the PHY is presenting either recovered and decoded data or control characters on the XGMII. The RXC signal for a lane shall be de-asserted when a data octet is being received on the corresponding lane and asserted when a control character is being received. In the absence of errors, the RXC signals are de-asserted by the PHY for each octet of the preamble (except the first octet that is replaced with a Start control character) and remain de-asserted while all octets to be received are presented on the lanes of the XGMII. RXC<3:0> are driven by the PHY and shall transition synchronously with respect to both the rising and falling edges of RX_CLK. Table 46–4 specifies the permissible encodings of RXD and RXC for a XGMII receive lane. Additional requirements apply for proper code sequences and in which lanes particular codes are valid (e.g., Start control character is to be aligned to lane 0).

Figure 46–8 shows the behavior of RXC<3:0> during an example frame reception with no errors.

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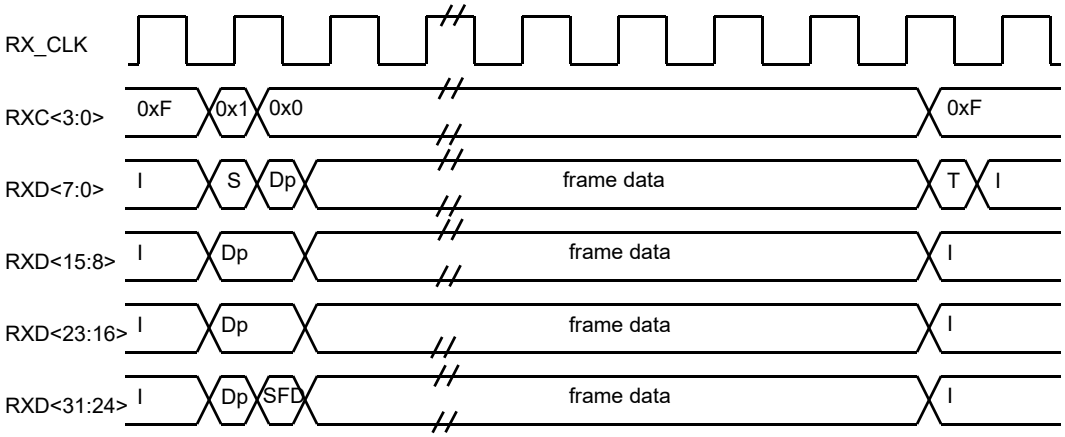
Table 46–4—Permissible lane encodings of RXD and RXC

RXC	RXD	Description	PLS_DATA.indication parameter
0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1	00 through 05	Reserved	—
1	06	Only valid on all four lanes simultaneously to indicate LP_IDLE is asserted	No applicable parameter (Normal interframe)
1	07	Idle	No applicable parameter (Normal inter-frame)
1	08 through 9B	Reserved	—
1	9C	Sequence (only valid in lane 0)	No applicable parameter (Inter-frame status signal)
1	9D through FA	Reserved	—
1	FB	Start (only valid in lane 0)	No applicable parameter, first eight ZERO, ONE of a frame (a preamble octet)
1	FC	Reserved	—
1	FD	Terminate	No applicable parameter (Start of inter-frame)
1	FE	Receive error	No applicable parameter
1	FF	Reserved	—
NOTE—Values in RXD column are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>).			



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character

Figure 46–8—Basic frame reception

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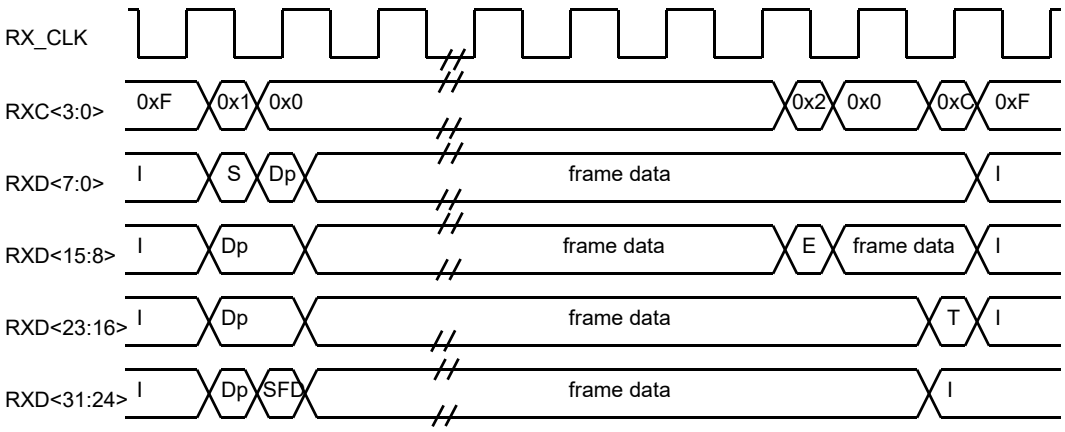
46.3.2.3 RXD (receive data)

RXD is a bundle of 32 data signals (RXD<31:0>) organized into four lanes of eight signals each (RXD<7:0>, RXD<15:8>, RXD<23:16>, and RXD<31:24>) that are driven by the PHY. Each lane is associated with a RXC signal as shown in Table 46–2 and shall be decoded by the RS as shown in Table 46–4. RXD<31:0> shall transition synchronously with respect to both the rising and falling edges of RX_CLK. For each high or low RX_CLK transition, received data and/or control are presented on RXD<31:0> for mapping by the RS. RXD<0> is the least significant bit of lane 0, RXD<8> the least significant bit of lane 1, RXD<16> the least significant bit of lane 2, and RXD<24> the least significant bit of lane 3. Figure 46–8 shows the behavior of RXD<31:0> during frame reception.

While the RXC of a lane is de-asserted, RXD of the lane is used by the RS to generate PLS_DATA.indication transactions. Assertion on a lane of appropriate RXD values when RXC is asserted indicates to the RS the Start control character, Terminate control character, Sequence control character, or Error control character that drive its mapping functions.

RXC of a lane is asserted with the appropriate Error control character encoding on RXD of the lane to indicate an error was detected somewhere in the frame presently being transferred from the PHY to the RS (e.g., a coding error, or any error that the PHY is capable of detecting, and that may otherwise be undetectable at the MAC sublayer).

The effect of an Error control character on the RS is defined in 46.3.3.1. Figure 46–9 shows the behavior of RXC and RXD during the reception of an example frame with an error.



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character, E: Error control character

Figure 46–9—Reception with error

46.3.2.4 Receive direction LPI transition

LPI operation and the LPI client are described in 78.1. When the PHY receives signals from the link partner to indicate transition into the low power state, it indicates this to the RS by asserting RXC and setting RXD to 0x06 (in all lanes). The PHY maintains these signals in this state while it remains in the LPI state. When the PHY receives signals from the link partner to indicate transition out of the LPI state, it indicates this to the RS by asserting RXC and asserting idle on lanes 0–3 to return to a normal interframe state. The RS shall interpret the LPI coding as shown in Table 46–4.

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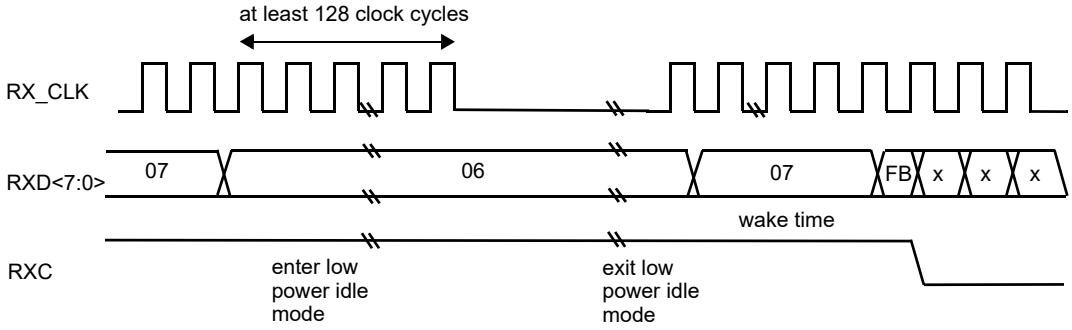
The PHY or DTE XS may halt RX_CLK at any time more than 128 clock cycles after the start of the LPI state as shown in Figure 46–10 if the clock stop enable bit is asserted (see 45.2.3.1.4 and 45.2.5.1.4). The PHY shall restart RX_CLK so that at least one positive transition occurs before it deasserts LPI.

Figure 46–10 shows the behavior of RXC and RXD<7:0> during LPI transitions.



NOTE 1—RXC and RXD are shown for one lane, all 4 lanes behave identically during LPI.
NOTE 2—In some instances, LPI may be followed by characters other than IDLE during wake time.

Figure 46–10—LPI transition

46.3.3 Error and fault handling

46.3.3.1 Response to error indications by the XGMII

If, during frame reception (i.e., when DATA_VALID_STATUS = DATA_VALID), a control character other than a Terminate control character is signaled on a received lane, the RS shall ensure that the MAC will detect a FrameCheckError in that frame. This requirement may be met by incorporating a function in the RS that produces a received frame data sequence delivered to the MAC sublayer that is guaranteed to not yield a valid CRC result, as specified by the frame check sequence algorithm (see 3.2.8). This data sequence may be produced by substituting data delivered to the MAC. The RS generates eight PLS_DATA.indication primitives for each Error control character received within a frame, and may generate eight PLS_DATA.indication primitives to ensure FrameCheckError when a control character other than Terminate causes the end of the frame.

Other techniques may be employed to respond to a received Error control character provided that the result is that the MAC sublayer behaves as though a FrameCheckError occurred in the received frame.

46.3.3.2 Conditions for generation of transmit Error control characters

If, during the process of transmitting a frame, it is necessary to request that the PHY deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability, then an Error control character may be asserted on a transmit lane by the appropriate encoding of the lane's TXD and TXC signals.

46.3.3.3 Response to received invalid frame sequences

The 2.5 Gb/s, 5 Gb/s, or 10 Gb/s PCS adjacent to this RS is required to either preserve the column alignment of the transmitting RS, or align the Start control character to lane 0. The RS shall not indicate DATA_VALID to the MAC for a Start control character received on any other lane. Error free 2.5 Gb/s, 5 Gb/s, or 10 Gb/s operation will not change the SFD alignment in lane 3. A 2.5 Gb/s, 5 Gb/s, or 10 Gb/s MAC/RS

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implementation is not required to process a packet that has an SFD in a position other than lane 3 of the column following the column containing the Start control character.

To support 2.5GBASE-X compatibility with a 1000BASE-X PCS/PMA running 2.5 times faster as described in Annex 127A, a 2.5 Gb/s MAC/RS implementation connected to a 2.5GBASE-X PHY is required to support an SFD received on either lane 2 or lane 3.

46.3.4 Link fault signaling

Link fault signaling operates between the remote RS and the local RS. Faults detected between the remote RS and the local RS are received by the local RS as Local Fault. Only an RS originates Remote Fault signals.

Sublayers within the PHY are capable of detecting faults that render a link unreliable for communication. Upon recognition of a fault condition a PHY sublayer indicates Local Fault status on the data path. When this Local Fault status reaches an RS, the RS stops sending MAC data or LPI, and continuously generates a Remote Fault status on the transmit data path (possibly truncating a MAC frame being transmitted). When Remote Fault or Link Interruption status is received by an RS, the RS stops sending MAC data or LPI, and continuously generates Idle control characters. When the RS no longer receives fault status messages, it returns to normal operation, sending MAC data or LPI.

Status is signaled in a four byte Sequence ordered set as shown in Table 46–5. The PHY indicates Local Fault with a Sequence control character in lane 0 and data characters of 0x00 in lanes 1 and 2 plus a data character of 0x01 in lane 3. The RS indicates a Remote Fault with a Sequence control character in lane 0 and data characters of 0x00 in lanes 1 and 2 plus a data character of 0x02 in lane 3. Though most fault detection is on the receive data path of a PHY, in some specific sublayers, faults can be detected on the transmit side of the PHY. This is also indicated by the PHY with a Local Fault status.

For operation with links that may be temporarily interrupted, optional detection of a third fault condition, Link Interruption, is provided. Link Interruption is indicated by the PHY receive function by continuously sending the Link Interruption ordered set as defined in Table 46–5.

Table 46–5—Sequence ordered sets

Lane 0	Lane 1	Lane 2	Lane 3	Description
Sequence	0x00	0x00	0x00	Reserved
Sequence	0x00	0x00	0x01	Local Fault
Sequence	0x00	0x00	0x02	Remote Fault
Sequence	0x00	0x00	0x03	Link Interruption
Sequence	≥ 0x00	≥ 0x00	≥ 0x04	Reserved
NOTE—Values in Lane 1, Lane 2, and Lane 3 columns are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>). The link fault signaling state diagram allows future standardization of reserved Sequence ordered sets for functions other than link fault indications				

The RS reports the fault status of the link. Local Fault indicates a fault detected on the receive data path between the remote RS and the local RS. Remote Fault indicates a fault on the transmit path between the

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local RS and the remote RS. The RS shall implement the link fault signaling state diagram (see Figure 46–11).

46.3.4.1 Conventions

The notation used in the state diagram follows the conventions of 21.5. The notation ++ after a counter indicates it is to be incremented.

46.3.4.2 Variables and counters

The link fault signaling state diagram uses the following variables and counters:

col_cnt
: A count of the number of columns received not containing a fault_sequence. This counter increments at RX_CLK rate (on both the rising and falling clock transitions) unless reset.

fault_sequence
: A new column received on RXC<3:0> and RXD<31:0> comprising a Sequence ordered set of four bytes and consisting of a Sequence control character in lane 0 and a seq_type in lanes 1, 2, and 3 indicating either Local Faut, Remote Fault, or Link Interruption.

last_seq_type
: The seq_type of the previous Sequence ordered set received
Values: Local Fault; 0x00 in lane 1, 0x00 in lane 2, 0x01 in lane 3.
Remote Fault; 0x00 in lane 1, 0x00 in lane 2, 0x02 in lane 3.
Link Interruption; 0x00 in lane 1, 0x00 in lane 2, 0x03 in lane 3.

link_fault
: An indicator of the fault status.
Values: OK; No fault.
Local Fault; fault detected by the PHY.
Remote Fault; fault detection signaled by the remote RS.
Link Interruption; link temporarily unavailable, signaled by the PHY.

reset
: Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.
Values: FALSE: The device is completely powered and has not been reset (default).
TRUE: The device has not been completely powered or has been reset.

seq_cnt
: A count of the number of received Sequence ordered sets of the same type.

seq_type
: The value received in the current Sequence ordered set
Values: Local Fault; 0x00 in lane 1, 0x00 in lane 2, 0x01 in lane 3.
Remote Fault; 0x00 in lane 1, 0x00 in lane 2, 0x02 in lane 3.
Link Interruption; 0x00 in lane 1, 0x00 in lane 2, 0x03 in lane 3.

46.3.4.3 State diagram

The link fault signaling state diagram specifies the RS monitoring of RXC<3:0> and RXD<31:0> for Sequence ordered sets. The variable link_fault is set to indicate the value of a received Sequence ordered set when four fault_sequences containing the same fault value have been received with each pair of fault sequences separated by less than 128 columns and no intervening fault_sequences of a different fault value.

The variable link_fault is set to OK following any interval of 128 columns not containing a Remote Fault, Local Fault, or Link Interruption Sequence ordered set.

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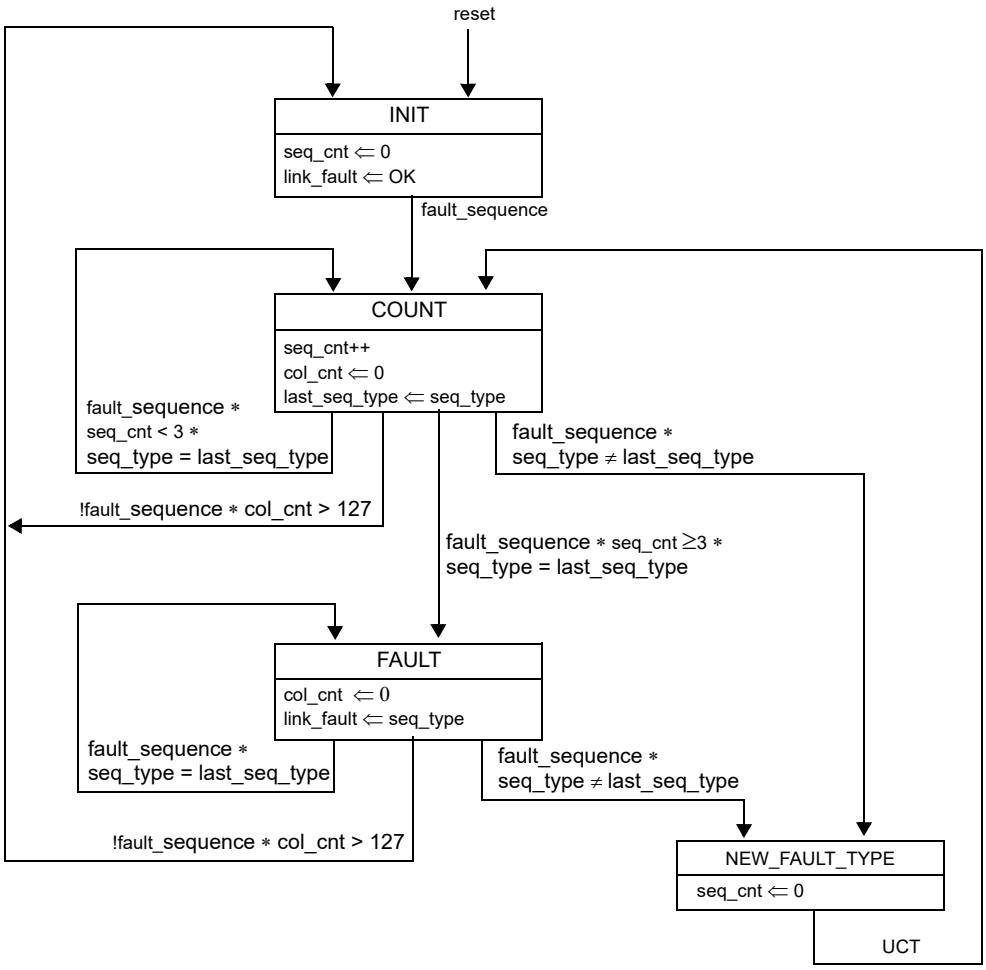

Figure 46–11—Link fault signaling state diagram

The RS output onto TXC<3:0> and TXD<31:0> is controlled by the variable link_fault.

a) link_fault = OK
   The RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.
b) link_fault = Local Fault
   The RS shall continuously generate Remote Fault Sequence ordered sets.
c) link_fault = Remote Fault or link_fault = Link Interruption
   The RS shall continuously generate Idle control characters.

46.4 LPI assertion and detection

Certain PHYs support Energy-Efficient Ethernet (see Clause 78). PHYs with EEE capability support LPI assertion and detection. LPI operation and the LPI client are described in 78.1. LPI signaling allows the RS to signal to the PHY and to the link partner that a break in the data stream is expected and components may use this information to enter power-saving modes that require additional time to resume normal operation. Similarly, it allows the LPI client to understand that the link partner has sent such an indication.

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The LPI assertion and detection mechanism fits conceptually between the PLS Service Primitives and the XGMII signals as shown in Figure 46–12.

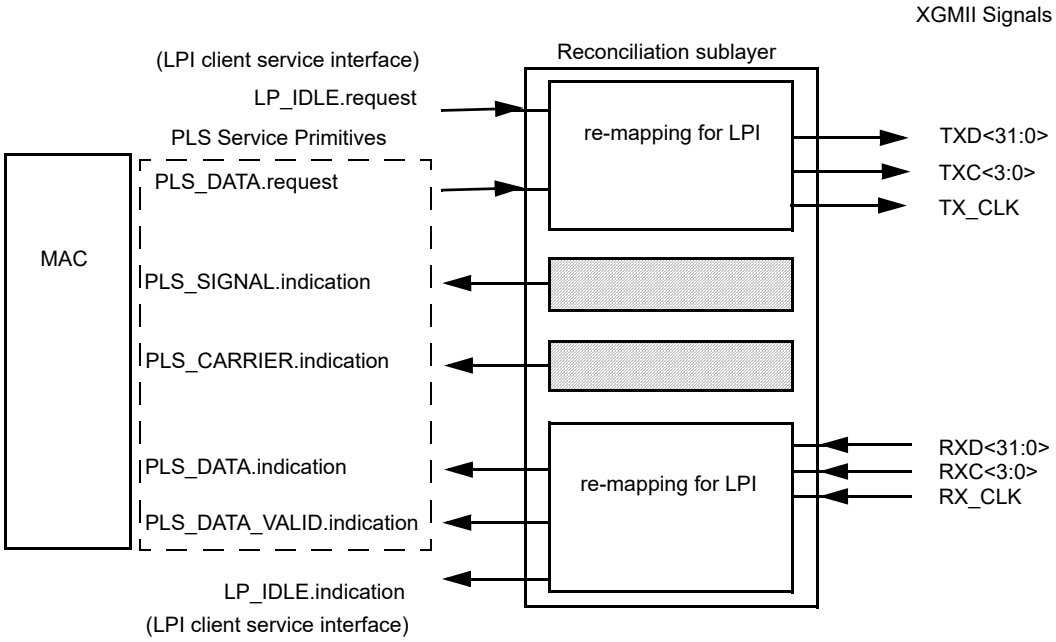

Figure 46–12—LPI assertion and detection mechanism

The definition of TXC<3:0> and TXD<31:0> is derived from the state of PLS_DATA.request (46.1.7), except when it is overridden by an assertion of LP_IDLE.request.

Similarly, RXC<3:0> and RXD<31:0> are mapped to PLS_DATA.indication except when LP_IDLE is detected

PLS_CARRIER.indication(CARRIER_STATUS) will be set to CARRIER_ON when the link is in LPI mode. See 46.1.7.3.

The timing of PLS_CARRIER.indication when used for the LPI function is controlled by the LPI transmit state diagram.

46.4.1 LPI messages

LP_IDLE.indication(LPI_INDICATION)

A primitive that indicates to the LPI client that the PHY has detected the assertion or de-assertion of LPI from the link partner.

Values: DEASSERT: The link partner is operating with normal interframe behavior (default).
ASSERT: The link partner has asserted LPI.

LP_IDLE.request(LPI_REQUEST)

The LPI_REQUEST parameter can take one of two values: ASSERT or DE-ASSERT. ASSERT initiates the signaling of LPI to the link partner. DE-ASSERT stops the signaling of LPI to the link partner. The effect of receipt of this primitive is undefined if link_status is not OK (see 28.2.6.1.1) or within 1 s of the change of link_status to OK.

46.4.2 Transmit LPI state diagram

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been de-asserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

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This wake-up time is enforced by the transmit LPI state diagram using CARRIER_SENSE.indication. The implementation shall conform to the behavior described by the transmit LPI state diagram shown in Figure 46–13.

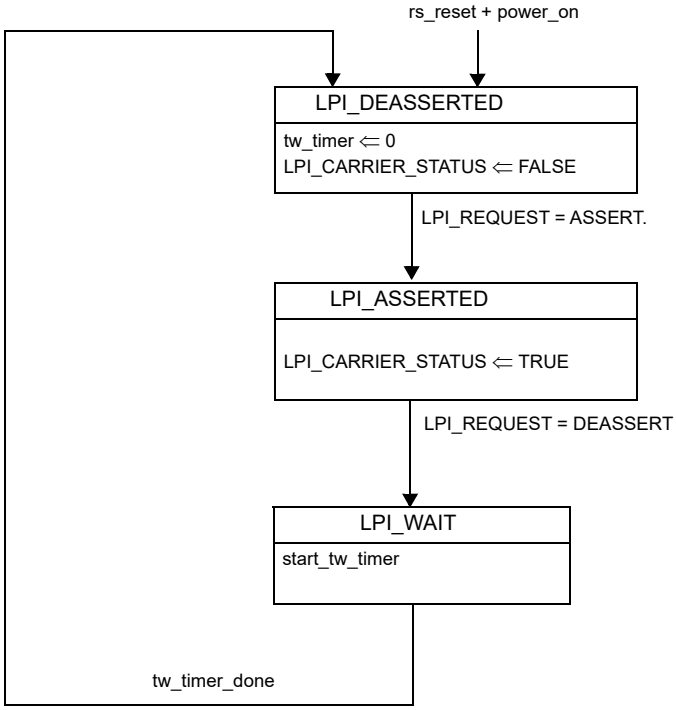

Figure 46–13—Transmit LPI state diagram

46.4.2.1 Variables and counters

The transmit LPI state diagram uses the following variables and counters:

LPI_CARRIER_STATUS
: The LPI_CARRIER_STATUS variable indicates how the CARRIER_STATUS parameter is controlled by the LPI_REQUEST parameter. The LPI_CARRIER_STATUS is either TRUE or FALSE as determined by the Transmit LPI state diagram in Figure 46–13.

power_on
: Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.
  Values: FALSE: The device is completely powered (default).
  TRUE: The device has not been completely powered.

rs_reset
: Used by management to control the resetting of the RS.
  Values: FALSE: Do not reset the RS (default).
  TRUE: Reset the RS.

tw_timer
: A timer that counts, in microseconds, the time since the de-assertion of LPI. The terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2. If DTE XS XAUI stop enable bit is asserted (5.0.9), the terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2 plus additional time equal to $T_{w\_sys\_tx} - T_{w\_sys\_rx}$ for the XGXS as shown in Table 78–4.

  The signal tw_timer_done is asserted when tw_timer reaches its terminal count.

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46.4.3 Considerations for transmit system behavior

The transmit system should expect that egress data flow will be halted for at least resolved $T_{w\_sys\_tx}$ (see 78.2) time, in microseconds, after it requests the de-assertion of LPI. Buffering and queue management should be designed to accommodate this.

46.4.4 Considerations for receive system behavior

The mapping function of the Reconciliation Sublayer shall continue to signal IDLE on PLS_DATA.indicate while it is detecting LP_IDLE on the XGMII. The receive system should be aware that data frames may arrive at the XGMII following the de-assertion of LPI_INDICATION with a delay corresponding to the link partner's resolved $T_{w\_sys\_rx}$ (as specified in 78.5) time, in microseconds.

If the PHY XS XAUI stop enable bit (4.0.9) is asserted, the PHY XS may stop signaling on the XAUI in the receive direction to conserve energy. The receiver should negotiate an additional 9.5 μs for the remote T_{w_sys} (equal to $T_{w\_sys\_tx} - T_{w\_sys\_rx}$ for the XGXS as shown in Table 78–4) before setting the PHY XS XAUI stop enable bit.

46.5 XGMII electrical characteristics

The electrical characteristics of the XGMII are specified such that the XGMII can be applied within a variety of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s equipment types. The electrical specifications are selected for an integrated circuit to integrated circuit application. The electrical characteristics specified in this clause apply to all XGMII signals.

When implemented as a chip-to-chip interface, the XGMII uses High Speed Transceiver Logic (HSTL), specified for a 1.5 volt output buffer supply voltage. XGMII chip-to-chip signals shall comply with EIA/JEDEC Standard EIA/JESD8-6 using Class I, output buffers. Output impedance shall be greater than 38Ω to assure acceptable overshoot and undershoot performance in an unterminated interconnection.

The thresholds and parametric values for HSTL XGMII signals are shown in the illustrative Figure 46–14 and example Table 46–6.

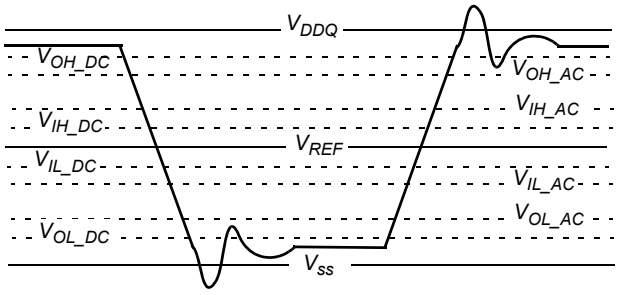

Figure 46–14—Electrical characteristics (illustrative)

The HSTL specification shows a number of termination options for different applications. Figure 46–15 illustrates a possible XGMII circuit topology. Unterminated interconnection is recommended.

The XGMII chip-to-chip signals shall meet the timing requirements shown in Figure 46–16. All XGMII timing measurements shall be made at the XGMII driver output with the optional termination shown in Figure 46–15 and with a capacitive load from all sources of 10pF and are specified relative to the $V_{IL\_AC(max)}$ and $V_{IH\_AC(min)}$ thresholds.

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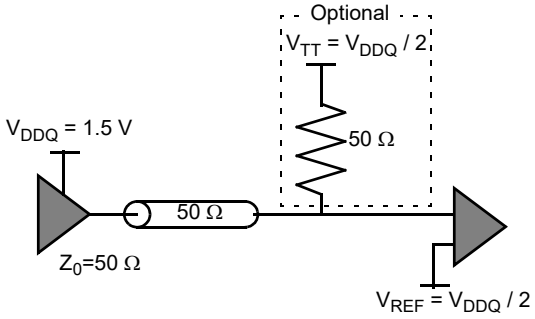
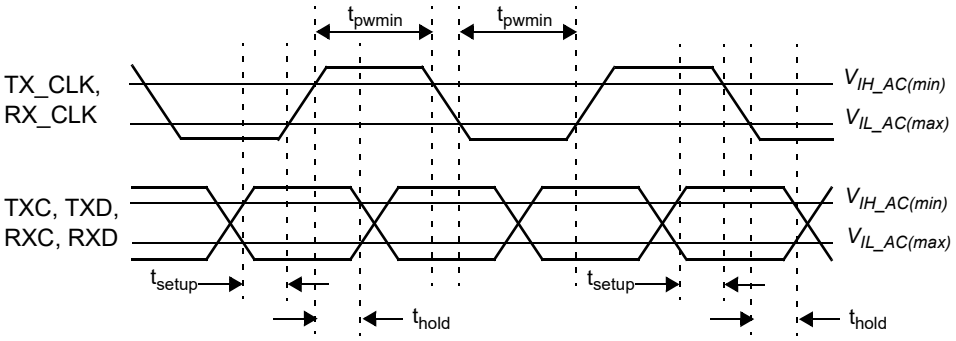


Figure 46–15—Circuit topology example



Symbol	Driver	Receiver	Units
t_{setup}	960	480	ps
t_{hold}	960	480	ps
t_{pwmin}	2.5	—	ns

Figure 46–16—TX_CLK and RX_CLK timing parameters

Table 46–6—Example DC and AC specifications

Symbol	Parameter	Min	Nom	Max	Units
V_{DDQ}	Output supply voltage	1.4	1.5	1.6	V
V_{REF}	Input reference voltage	0.68	0.75	0.90	V
V_{IH_DC}	DC input logic high	V_{REF}+0.10	—	V_{DDQ}+0.3	V
V_{IL_DC}	DC input logic low	–0.30	—	V_{REF}–0.1	V
V_{IH_AC}	AC input logic high	V_{REF}+0.20	—	—	V
V_{IL_AC}	AC input logic low	—	—	V_{REF}–0.20	V

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46.6 Protocol implementation conformance statement (PICS) proforma for Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)[88]

46.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

46.6.2 Identification

46.6.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

46.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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46.6.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PHY	PHY support of XGMII	46.2, 46.3		O	Yes [ ] No [ ]
*RS	Reconciliation Sublayer support of XGMII	46.2, 46.3		O	Yes [ ] No [ ]
*XGE	XGMII electrical interface	46.4		O	Yes [ ] No [ ]
*LPI	Implementation of LPI	46.1.7		O	Yes [ ] No [ ]

46.6.3 PICS proforma tables for Reconciliation Sublayer and 10 Gigabit Media Independent Interface

46.6.3.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	PHY support of 10 Gb/s MAC data rate	46.1.3	Support MAC data rate of 10 Gb/s	PHY:O.1	Yes [ ] N/A [ ]
G2	PHY support of 5 Gb/s MAC data rate	46.1.3	Support MAC data rate of 5 Gb/s	PHY:O.1	Yes [ ] N/A [ ]
G3	PHY support of 2.5 Gb/s MAC data rate	46.1.3	Support MAC data rate of 2.5 Gb/s	PHY:O.1	Yes [ ] N/A [ ]
G4	Cumulative MAC Control, MAC and RS round-trip delay	46.1.4	Per Table 46–1	RS:M	Yes [ ] N/A [ ]
G5	Lane structure	46.1.6	Per Table 46–2	M	Yes [ ]

46.6.3.2 Mapping of PLS service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
PL1	Mapping to Clause 6	46.1.7	RS implements mapping to Clause 6 PLS service primitives	RS:M	Yes [ ] N/A [ ]
PL2	Mapping of PLS_DATA.requests	46.1.7.1.4	In sequence TXD<0> to TXD<31>	RS:M	Yes [ ] N/A [ ]
PL3	Start control character creation	46.1.7.1.4	First octet of preamble converted to Start control character	RS:M	Yes [ ] N/A [ ]
PL4	TXD and TXC generation	46.1.7.1.4	For each 32 PLS_DATA.requests	RS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PL5	Terminate control character creation	46.1.7.1.4	DATA_COMPLETE causes creation of Terminate control character in next lane in sequence	RS:M	Yes [ ] N/A [ ]
PL6	Mapping RXD to PLS_DATA.incicates	46.1.7.2.3	Create PLS_DATA.increments in sequence from RXD<0> to RXD<31>	RS:M	Yes [ ] N/A [ ]
PL7	PLS_DATA.indication generation	46.1.7.2.3	Generate 32 PLS_DATA.indications for each RXD<0:31> until Terminate then generating 0, 8, 16, or 24	RS:M	Yes [ ] N/A [ ]
PL8	Start control character conversion	46.1.7.2.3	Convert valid Start control character to preamble before generating PLS_DATA.indications	RS:M	Yes [ ] N/A [ ]
PL9	Terminate control character	46.1.7.2.3	No PLS_DATA.indications generated	RS:M	Yes [ ] N/A [ ]
PL10	PLS_DATA_VALID.indicatio n generation	46.1.7.5.3	On change of value of DATA_VALID_STATUS	RS:M	Yes [ ] N/A [ ]
PL11	DATA_VALID_STATUS	46.1.7.5.3	Value of DATA_VALID on a lane 0 Start control character preceded by four idles or a Sequence ordered set	RS:M	Yes [ ] N/A [ ]
PL12	DATA_VALID_STATUS	46.1.7.5.3	Value of DATA_NOT_VALID on any control character but Error	RS:M	Yes [ ] N/A [ ]
PL13	Frame not ending with Terminate control character	46.1.7.5.3	Ensure MAC detects CRC error	RS:M	Yes [ ] N/A [ ]

46.6.3.3 Data stream structure

Item	Feature	Subclause	Value/Comment	Status	Support
DS1	Frame transfer	46.2	Within XGMII data stream	RS:M	Yes [ ] N/A [ ]
DS2	Bit mapping	46.2	Per Figure 46–4	RS:M	Yes [ ] N/A [ ]
DS3	Content of <data>	46.2.3	Consist of data octets	RS:M	Yes [ ] N/A [ ]
DS4	Recognition of <efd>	46.2.4	Terminate recognized in any lane	RS:M	Yes [ ] N/A [ ]

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46.6.3.4 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Assertion of LPI in Tx direction	46.3.1.2	As defined in Table 46–3	LPI:M	Yes [ ] N/A [ ]
L2	Assertion of LPI in Rx direction	46.3.2.2	As defined in Table 46–4	LPI:M	Yes [ ] N/A [ ]
*L3	TX_CLK stoppable during LPI	46.3.1.5	At least 128 cycles after LPI assertion	LPI:O	Yes [ ] No [ ]
L4	TX_CLK restart before LPI deassert	46.3.1.5	At least 1 positive edge before LPI deassertion	L3:M	Yes [ ] N/A [ ]
L5	RX_CLK stoppable during LPI	46.3.2.4		LPI:O	Yes [ ] No [ ]

46.6.3.5 Link Interruption

Item	Feature	Subclause	Value/Comment	Status	Support
LINT	Detection of Link Interruption	46.3.4		O	Yes [ ] No [ ]
LINT1	CARRIER_STATUS response to Link Interruption	46.1.7.3	Set to CARRIER_ON if link_fault is Link Interruption	LINT:O	Yes [ ] No [ ]

46.6.3.6 XGMII signal functional specifications

NOTE—An XGXS adjacent to an RS exhibits the characteristics of a PHY for the items in this subclause, and an XGXS adjacent to a PCS exhibits the characteristics of an RS for the items in this subclause.

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	TX_CLK active edges	46.3.1.1	TXD and TXC sampled on both edges of TX_CLK	XGE:M	Yes [ ] N/A [ ]
FS2	TX_CLK frequency	46.3.1.1	$1/64 \times f_{MAC} \pm 100$ ppm, where f_{MAC} is the frequency (in Hz) corresponding to the MAC's nominal bit rate	XGE:M	Yes [ ] N/A [ ]
FS3	TXC assertion and de-assertion	46.3.1.2	De-asserted for data, asserted for control character	RS:M	Yes [ ] N/A [ ]
FS4	TXC clock	46.3.1.2	Synchronous to TX_CLK	XGE:M	Yes [ ] N/A [ ]
FS5	TXD encoding	46.3.1.3	Per Table 46–3	RS:M	Yes [ ] N/A [ ]
FS6	TXD clock	46.3.1.3	Synchronous to TX_CLK	XGE:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
FS7	Start alignment	46.3.1.4	Start control character aligned to lane 0	RS:M	Yes [ ] N/A [ ]
FS8	RX_CLK active edges	46.3.2.1	RXD and RXC sampled on both edges of RX_CLK	XGE:M	Yes [ ] N/A [ ]
FS9	RX_CLK frequency	46.3.2.1	$1/64 \times f_{MAC} \pm 100$ ppm, where f_{MAC} is the frequency (in Hz) corresponding to the MAC's nominal bit rate when received data rate is within tolerance	XGE:M	Yes [ ] N/A [ ]
FS10	Loss of receive signal	46.3.2.1	Source RX_CLK from nominal clock	PHY:M	Yes [ ] N/A [ ]
FS11	Transition between clock sources	46.3.2.1	No decrease of RX_CLK period when switching sources	PHY:M	Yes [ ] N/A [ ]
FS12	RXC assertion and de-assertion	46.3.2.2	De-asserted for data, asserted for control character	PHY:M	Yes [ ] N/A [ ]
FS13	RXC clock	46.3.2.2	Synchronous to RX_CLK	XGE:M	Yes [ ] N/A [ ]
FS14	RXD decoding	46.3.2.3	Per Table 46–4	RS:M	Yes [ ] N/A [ ]
FS15	RXD clock	46.3.2.3	Synchronous to RX_CLK	XGE:M	Yes [ ] N/A [ ]
FS16	Received Error control character	46.3.3.1	RS cause MAC FrameCheckError	RS:M	Yes [ ] N/A [ ]
FS17	DATA_VALID assertion	46.3.3.3	RS not assert DATA_VALID unless Start control character in lane 0	RS:M	Yes [ ] N/A [ ]

46.6.3.7 Link fault signaling state diagram

Item	Feature	Subclause	Value/Comment	Status	Support
LF1	Link fault signaling state diagram	46.3.4	Implement per Figure 46–11	RS:M	Yes [ ] N/A [ ]
LF2	link_fault = OK and MAC frames	46.3.4.3	RS services MAC frame transmission requests	RS:M	Yes [ ] N/A [ ]
LF3	link_fault = OK and no MAC frames	46.3.4.3	In absence of MAC frames, RS transmits Idle control characters	RS:M	Yes [ ] N/A [ ]
LF4	link_fault = Local Fault	46.3.4.3	RS transmits continuous Remote Fault Sequence ordered sets	RS:M	Yes [ ] N/A [ ]
LF5	link_fault = Remote Fault	46.3.4.3	RS transmits continuous Idle control characters	RS:M	Yes [ ] N/A [ ]

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46.6.3.8 Electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
EC1	Referenced standard for signals	46.5	Signals to be compliant with EIA/JESD8-6 using Class I, output buffers	XGE:M	Yes [ ] N/A [ ]
EC2	Output impedance	46.5	Signal output impedance of at least 38 Ω	XGE:M	Yes [ ] N/A [ ]
EC3	Signal timing	46.5	Per Figure 46–16	XGE:M	Yes [ ] N/A [ ]
EC4	Signal measurement	46.5	At driver output with optional termination per Figure 46–15 and with a capacitive load from all sources of 10 pF	XGE:M	Yes [ ] N/A [ ]

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47. XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI)

47.1 Overview

This clause defines the functional and electrical characteristics for the optional XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI). Figure 47–1 shows the relationships of the XGMII, XGMII Extender, XGXS, and XAUI.

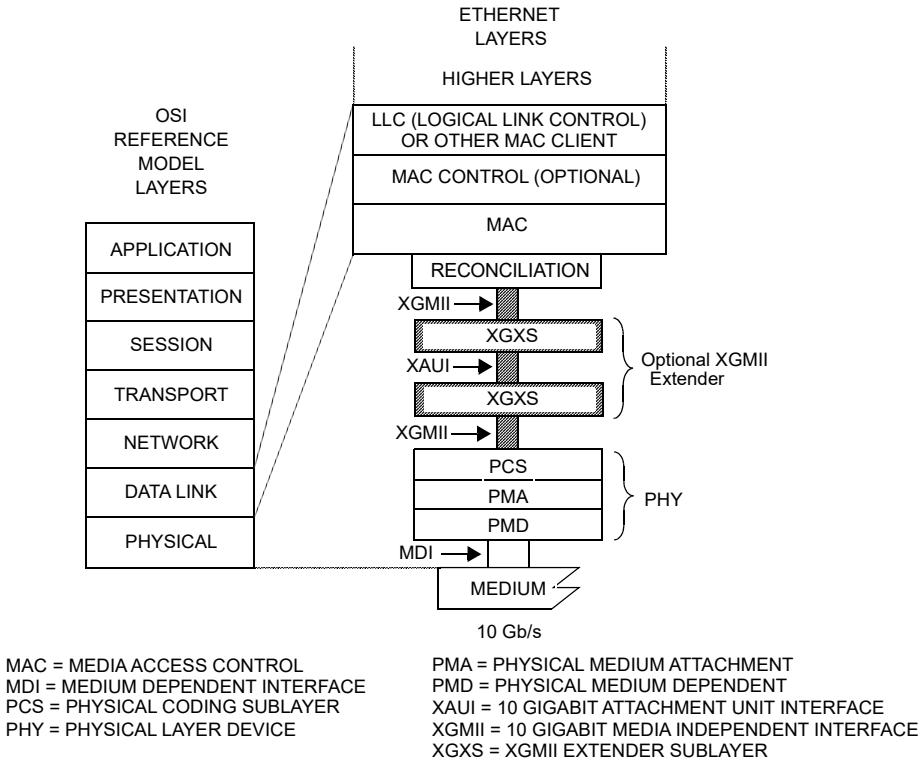

Figure 47–1—XAUI and XGXS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The purpose of the XGMII Extender, which is composed of an XGXS at the RS end (DTE XGXS), an XGXS at the PHY end (PHY XGXS) and a XAUI between them, is to extend the operational distance of the XGMII and to reduce the number of interface signals. Applications include extending the physical separation possible between MAC and PHY components in a 10 Gigabit Ethernet system distributed across a circuit board.

An XGMII Extender with the optional Energy-Efficient Ethernet (EEE) capability (see 78.3) may enter a low power state to conserve energy during periods of low link utilization. The ability to support transition to a low power state is indicated by register 4.20.0 (for a PHY XS) or 5.20.0 (for a DTE XS). Transition to the low power state is enabled by register 4.0.9 (for a PHY XS) or 5.0.9 (for a DTE XS). The assertion of Low Power Idle (LPI) at the XGMII is encoded in the transmitted symbols. Detection of LPI encoding in the received symbols is indicated as LPI at the XGMII. When LPI is received on the transmit XGMII, an energy-efficient XGMII Extender sends sleep symbols, then, if enabled, ceases transmission and deactivates XAUI transmit signals to conserve energy. When the receiver sees the sleep symbols it transitions to a quiet state. The XGMII Extender periodically transmits during the quiet period to allow the attached XGMII Extender to refresh its receiver state (e.g., timing recovery, adaptive filter coefficients) and thereby track

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long-term variation in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal interframe idle is asserted at the transmit XGMII, the XGMII Extender reactivates transmit functions and initiates transmission. This transmission will be detected by the attached XGMII Extender, causing it to also exit the low power state.

The optional XGMII Extender has the following characteristics:

a) Simple signal mapping to the XGMII
b) Independent transmit and receive data paths
c) Four lanes conveying the XGMII 32-bit data and control
d) Differential signaling with low voltage swing
e) Self-timed interface allows jitter control to the PCS
f) Shared technology with other 10 Gb/s interfaces
g) Shared functionality with other 10 Gb/s Ethernet blocks
h) Utilization of 8B/10B coding
i) Optionally extend LPI signaling to PHY for EEE
j) Optionally conserve energy during periods of low utilization

47.1.1 Summary of major concepts

The following is a list of the major concepts of XGXS and XAUI:

a) The optional XGMII Extender can be inserted between the Reconciliation Sublayer and the PHY to transparently extend the physical reach of the XGMII and reduce the interface pin count.
b) The XGMII is organized into four lanes with each lane conveying a data octet or control character on each edge of the associated clock. The source XGXS converts bytes on an XGMII lane into a self clocked, serial, 8B/10B encoded data stream. Each of the four XGMII lanes is transmitted across one of the four XAUI lanes.
c) The source XGXS converts XGMII Idle control characters (interframe) into an 8B/10B code sequence. The destination XGXS recovers clock and data from each XAUI lane and deskews the four XAUI lanes into the single-clock XGMII.
d) The destination XGXS adds to or deletes from the interframe as needed for clock rate disparity compensation prior to converting the interframe code sequence back into XGMII Idle control characters.
e) The XGXS uses the same code and coding rules as the 10GBASE-X PCS and PMA specified in Clause 48.

47.1.2 Application

This clause applies to the XGMII between the MAC and PHY. The implementation of the optional XGMII Extender is primarily intended as a chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board. Where the XGMII is electrically limited to distances of approximately 7 cm, the XGMII Extender allows distances up to approximately 50 cm.

47.1.3 Rate of operation

The XGMII Extender supports the 10 Gb/s data rate of the XGMII. The 10 Gb/s MAC data stream is converted into four lanes at the XGMII (by the Reconciliation Sublayer for transmit or the PHY for receive). The byte stream of each lane is 8B/10B encoded by the XGXS for transmission across the XAUI at a nominal rate of 3.125 GBd. The XGXS at the PHY end of the XGMII Extender (PHY XGXS) and the XGXS at the RS end (DTE XGXS) may operate on independent clocks.

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47.1.4 Allocation of functions

The XGMII Extender is transparent to the Reconciliation Sublayer and PHY device, and operates symmetrically with similar functions on the DTE transmit and receive data paths. The XGMII Extender is logically composed of two XGXSs interconnected with a XAUI data path in each direction. One XGXS acts as the source to the XAUI data path in the DTE transmit path and as the destination in the receive path. The other XGXS is the destination in the transmit path and source in the receive path. Each XAUI data path is composed of four serial lanes. All specifications for the XGMII Extender are written assuming conversion from XGMII to XAUI and back to XGMII, but other techniques may be employed provided that the result is that the XGMII Extender operates as if all specified conversions had been made. One example of this is the use of the optional XAUI with the 10GBASE-LX4 8B/10B PHY, where the XGXS interfacing to the Reconciliation Sublayer provides the PCS and PMA functionality required by the PHY. An XGXS layer is not required at the PHY end of the XAUI in this case. However, means may still be required to remove jitter introduced on the XAUI in order to meet PHY jitter requirements.

47.1.5 Global signal detect function

Global signal detect is mandatory for EEE capability, otherwise it is optional and its definition is beyond the scope of this standard. When global signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

For EEE capability, the global signal detect function shall control the PMA SIGNAL_DETECT parameter. The SIGNAL_DETECT parameter can take on one of two values, OK or FAIL, indicating whether the XGXS is detecting electrical energy at the XAUI receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMA parameter rx_lane<3:0> is undefined.

47.1.6 Global transmit disable function

Global transmit disable is mandatory for EEE capability. The transmit disable function shall turn off all transmitter lanes after tx_mode changes to QUIET within a time and voltage level specified in 47.3.3.2. The transmit disable function shall turn on all transmitter lanes after tx_mode changes to DATA within a time and voltage level specified in 47.3.3.2.

47.2 Functional specifications

At the source side of a XAUI, the XGXS takes XGMII data streams striped over four lanes as its input, maps XGMII data and control characters into XAUI code-groups, and encodes them for transmission. At the destination end of the XAUI, the XGXS decodes the code-groups, deskews the four lanes, compensates for clock rate disparity, and maps the XAUI code-groups back into XGMII data and control characters. Each XGXS is bidirectional, having both source and destination functionality. Figure 47–2 depicts a schematic representation of the XGXS inputs and outputs.

47.2.1 PCS and PMA functionality

The XGXS shall meet all mandatory portions of 48.2 and 48.3, and may meet any optional portions of 48.2 and 48.3. Since the PHY XGXS operates with the XGMII below the XAUI, the transmit requirements of 48.2 and 48.3 apply to the PHY XGXS receive requirements and the receive requirements apply to the PHY XGXS transmit functionality.

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47.2.2 Delay constraints

The XGMII Extender shall meet the delay constraints in 48.5. The contribution of the XAUI interconnect is included in these delay constraints.

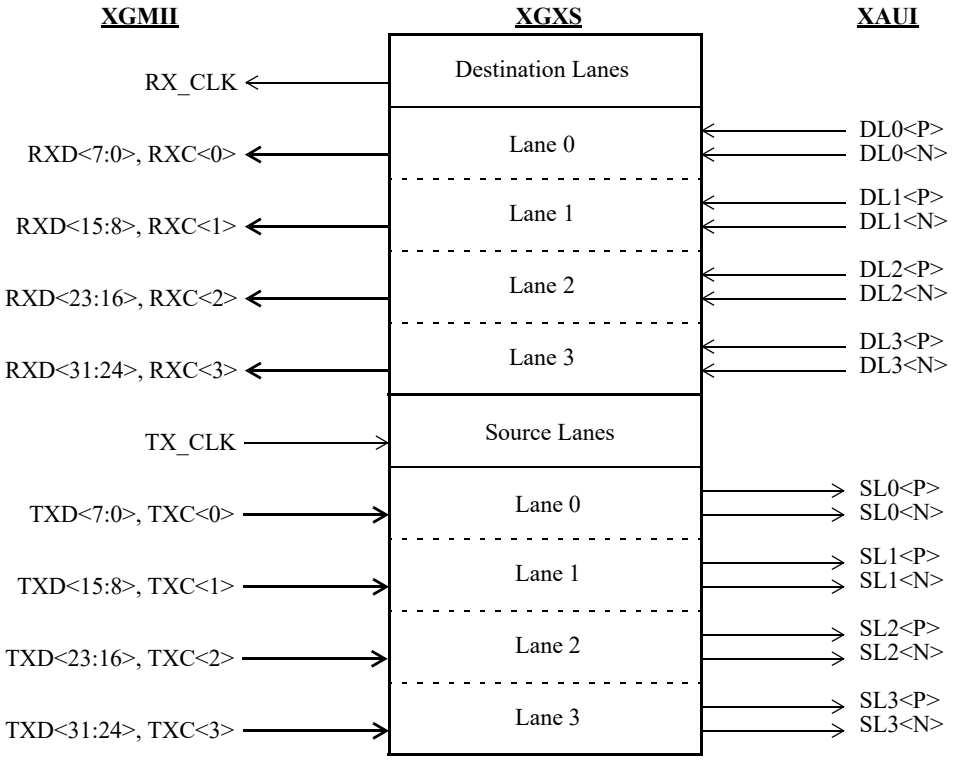

Figure 47–2—XGXS inputs and outputs

47.3 XAUI Electrical characteristics

The electrical characteristics of the XGMII Extender are specified such that it can be applied within a variety of 10 Gb/s Ethernet equipment types. There are two interface types associated with the XGMII Extender: the XGMII and XAUI. The electrical characteristics of both are selected for an integrated circuit to integrated circuit application. The electrical characteristics for the XGMII are specified in 46.5. The electrical characteristics for XAUI are specified in this subclause. Unless specified otherwise, the electrical characteristics defined in this subclause are applicable to all valid sequences of code-groups.

47.3.1 Signal levels

The XAUI is a low swing AC-coupled differential interface. AC-coupling allows for interoperability between components operating from different supply voltages. Low swing differential signaling provides noise immunity and improved electromagnetic interference (EMI). Differential signal swings defined in 47.3 depend on several factors, such as transmitter pre-equalization and transmission line losses.

47.3.2 Signal paths

The XAUI signal paths are point-to-point connections. Each path corresponds to a XAUI lane and is composed of two complementary signals making a balanced differential pair. There are four differential

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paths in each direction for a total of eight pairs, or sixteen connections. The signal paths are intended to operate up to approximately 50 cm over controlled impedance traces on standard FR4 printed circuit boards (PCBs).

47.3.3 Driver characteristics

The XAUI driver characteristics are summarized in Table 47–1. The XAUI Baud shall be 3.125 GBd ±100 ppm. The corresponding Baud period is nominally 320 ps.

Table 47–1—Driver characteristics

Parameter	Value	Units
Baud rate tolerance	3.125 GBd ± 100 ppm	GBd ppm
Unit interval nominal	320	ps
Differential amplitude maximum	1600	mV_{p-p}
Absolute output voltage limits maximum minimum	 2.3 –0.4	 V V
Differential output return loss minimum	[See Equation (47–1)]	dB
Output jitter Near-end maximums Total jitter Deterministic jitter Far-end maximums Total jitter Deterministic jitter	 ± 0.175 peak from the mean ± 0.085 peak from the mean ± 0.275 peak from the mean ± 0.185 peak from the mean	 UI UI UI UI

47.3.3.1 Load

The load is 100 Ω ± 5% differential to 2.5 GHz for these measurements, unless otherwise noted.

47.3.3.2 Amplitude and swing

Driver differential output amplitude shall be less than 1600 mV_{p-p} including any transmit equalization. DC-referenced logic levels are not defined since the receiver is AC-coupled. Absolute driver output voltage shall be between –0.4 V and 2.3 V with respect to ground. See Figure 47–3 for an illustration of absolute driver output voltage limits and definition of differential peak-to-peak amplitude.

For EEE capability, the transmitter lane's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of tx_quiet being asserted. Furthermore, the transmitter lane's differential peak-to-peak output voltage shall be greater than 800 mV within 500 ns of tx_quiet being de-asserted.

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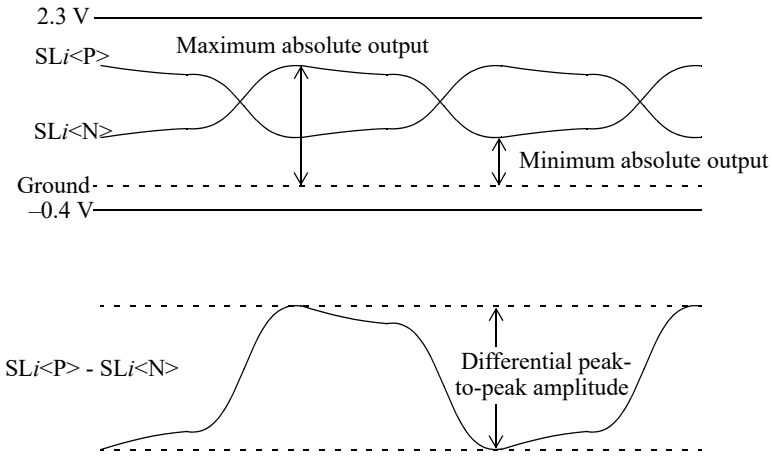

Figure 47–3—Driver output voltage limits and definitions
[L*i*<P> and L*i*<N> are the positive and negative sides of the differential signal pair for lane *i* (*i* = 0, 1, 2, 3)]

47.3.3.3 Transition time

Differential transition times between 60 and 130 ps are recommended, as measured between the 20% and 80% levels. Shorter transitions may result in excessive high-frequency components and increase EMI and crosstalk. The upper recommended limit of 130 ps corresponds to a sine wave at the half Baud.

47.3.3.4 Output impedance

For frequencies from 312.5 MHz to 3.125 GHz, the differential return loss of the driver shall exceed Equation (47–1). Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 Ω.

$$s_{11} = -10 \text{ dB for } 312.5 \text{ MHz} < \text{Freq } (f) < 625 \text{ MHz, and} \quad (47\text{–}1)$$
$$-10 + 10\log(f/625) \text{ dB for } 625 \text{ MHz} \leq \text{Freq } (f) \leq 3.125 \text{ GHz}$$

where f is frequency in MHz.

47.3.3.5 Driver template and jitter

The driver shall satisfy either the near-end eye template and jitter requirements, or the far-end eye template and jitter requirements. The eye templates are given in Figure 47–4 and Table 47–2. The template measurement requirements are specified in 47.4.2. The jitter requirements at the near end are for a maximum total jitter of ± 0.175 UI peak from the mean and a maximum deterministic component of ± 0.085 UI peak from the mean. The far-end requirements are for a maximum total jitter of ± 0.275 UI peak from the mean and a maximum deterministic component of ± 0.185 UI peak from the mean. Note that these values assume symmetrical jitter distributions about the mean. If a distribution is not symmetrical, its peak-to-peak total jitter value has to be less than these total jitter values to claim compliance to the template requirements per the methods of 47.4.2. Jitter specifications include all but 10^{-12} of the jitter population. The maximum random jitter is equal to the maximum total jitter minus the actual deterministic jitter. Jitter measurement requirements are described in 47.4.3.

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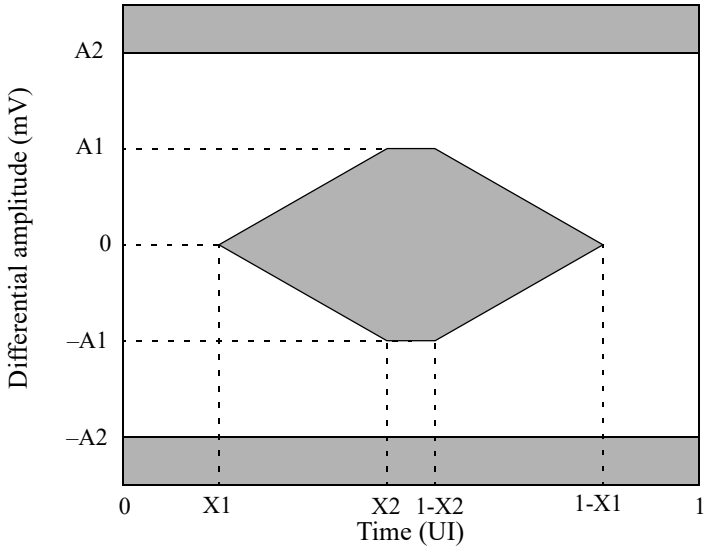

Figure 47–4—Driver template

Table 47–2—Driver template intervals

Symbol	Near-end value	Far-end value	Units
X1	0.175	0.275	UI
X2	0.390	0.400	UI
A1	400	100	mV
A2	800	800	mV

47.3.4 Receiver characteristics

Receiver characteristics are summarized in Table 47–3 and detailed in the following subclauses.

47.3.4.1 Bit error ratio

The receiver shall operate with a BER of better than 10^{-12} in the presence of a reference input signal as defined in 47.3.4.2.

47.3.4.2 Reference input signals

Reference input signals to a XAUI receiver have the characteristics determined by compliant XGXSs and XAUI drivers. Reference input signals satisfy the far-end template given in Figure 47–4 and Table 47–2 when the signal source impedance is 100 Ω ±5%. The template measurement requirements are specified in 47.4.2. Note that the input signal might not meet this template when this load is replaced by the actual receiver. Signal jitter does not exceed the jitter tolerance requirements specified in 47.3.4.6.

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Table 47–3—Receiver characteristics

Parameter	Value	Units
Baud rate tolerance	3.125 ±100	GBd ppm
Unit interval (UI) nominal	320	ps
Receiver coupling	AC	
EEE Signal Detect deactivation time (T_{SD}) from active to LPI quiet	750	ns
EEE Signal Detect activation time (T_{SA}) from LPI quiet to active	750	ns
Return loss[a] differential common-mode	 10 6	 dB dB
Jitter amplitude tolerance[b]	0.65	UI_{p-p}

[a]Relative to 100 Ω differential and 25 Ω common-mode. See 47.3.4.5 for input impedance details.
[b]See 47.3.4.6 for jitter tolerance details.

47.3.4.3 Input signal amplitude

XAUI receivers shall accept differential input signal amplitudes produced by compliant transmitters connected without attenuation to the receiver. Note that this may be larger than the 1600 mV_{p-p} maximum of 47.3.3.2 due to actual driver and receiver input impedances. The minimum input amplitude is defined by the far-end driver template and the actual receiver input impedance. Note that the far-end driver template is defined using a well controlled load impedance. The minimum signal amplitude into an actual receiver may vary from the minimum template height due to the actual receiver input impedance. Since the XAUI receiver is AC-coupled to the XAUI, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

47.3.4.4 AC-coupling

The XAUI receiver shall be AC-coupled to the XAUI to allow for maximum interoperability between various 10 Gb/s components. AC-coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC-coupling in actual implementations.

47.3.4.5 Input impedance

Receiver input impedance shall result in a differential return loss better than 10 dB and a common-mode return loss better than 6 dB from 100 MHz to 2.5 GHz. This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC-coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ω for differential return loss and 25 Ω for common-mode.

47.3.4.6 Jitter tolerance

The XAUI receiver shall have a peak-to-peak total jitter amplitude tolerance of at least 0.65 UI. This total jitter is composed of three components: deterministic jitter, random jitter, and an additional sinusoidal jitter. Deterministic jitter tolerance shall be at least 0.37 UI_{p-p}. Tolerance to the sum of deterministic and random jitter shall be at least 0.55 UI_{p-p}. The XAUI receiver shall tolerate an additional sinusoidal jitter with any

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frequency and amplitude defined by the mask of Figure 47–5. This additional component is intended to ensure margin for low-frequency jitter, wander, noise, crosstalk and other variable system effects. Jitter specifications include all but 10^{-12} of the jitter population. Jitter tolerance test requirements are specified in 47.4.3.

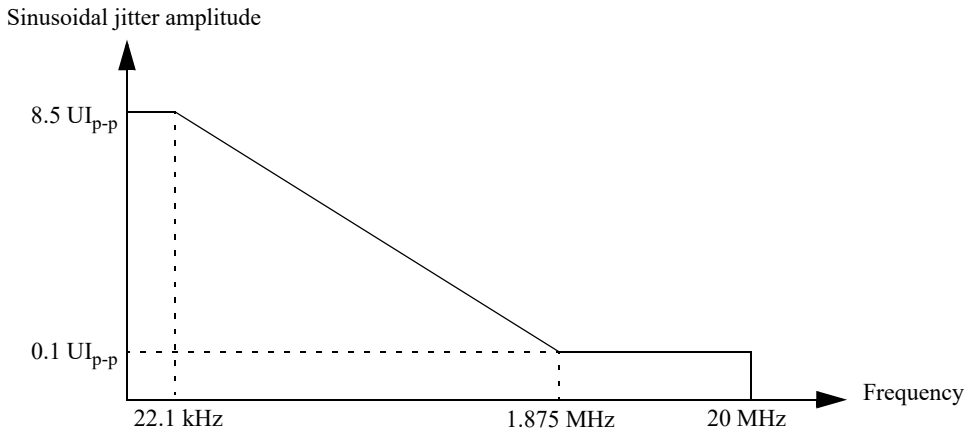

Figure 47–5—Single-tone sinusoidal jitter mask

47.3.4.7 EEE receiver timing

For EEE capability, the receiver shall meet the timing requirements shown in Table 47–3 for Signal_Detect activation and deactivation.

47.3.5 Interconnect characteristics

The XAUI is primarily intended as a point-to-point interface of up to approximately 50 cm between integrated circuits using controlled impedance traces on low-cost printed circuit boards (PCBs). Example loss and jitter budgets are presented in Table 47–4 to demonstrate the feasibility of standard FR4 epoxy PCBs. The performance of an actual XAUI interconnect is highly dependent on the implementation. The compliance interconnect limit of 47.4.1 represents the median performance of a range of interconnect designs. The range included designs from 46 to 56 cm in total length, having trace widths of 0.125 to 0.300 mm, and using different grades and thicknesses of FR4. Interconnect configurations ranged from single-board designs to systems of two daughter cards mating to a backplane through high-speed electrical connectors.

47.3.5.1 Characteristic impedance

The recommended differential characteristic impedance of circuit board trace pairs is 100 Ω ± 10% from 100 MHz to 2.5 GHz.

47.3.5.2 Connector impedance

The recommended impedance of any connectors, such as used between circuit board subsystems, is 100 Ω ± 30%.

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Table 47–4—Example XAUI loss, skew and jitter budget

	Loss (dB)[a]	Differential skew (ps_{p-p})	Total jitter (UI_{p-p})[c]	Deterministic jitter (UI_{p-p})[c]
Driver	0	15	0.35	0.17
Interconnect	7.5	60	0.20	0.20
Other[b]	4.5		0.10	0.10
Total	12.0	75	0.65	0.47

[a]Budgetary loss in height of eye opening.
[b]Includes such effects as crosstalk, noise, and interaction between jitter and eye height.
[c]Jitter specifications include all but 10^{-12} of the jitter population.

47.4 Electrical measurement requirements

47.4.1 Compliance interconnect definition

The compliance interconnect is a 100 Ω differential system specified with respect to transmission magnitude response and intersymbol interference (ISI) loss. The compliance interconnect limits have been chosen to allow a realistic differential interconnect of about 50 cm length on FR4 epoxy PCB. See 47.3.5 for a more detailed description of the target XAUI interconnect. The transmission magnitude response, $|s_{21}|$, of the compliance interconnect in dB satisfies Equation (47–2).

$$\left|s_{21}\right| \le \left|s_{21}\right|_{limit} = -20\log(e) \times [a_1\sqrt{f} + a_2 f + a_3 f^2] \quad (47\text{–}2)$$

where f is frequency in Hz, $a_1 = 6.5 \times 10^{-6}$, $a_2 = 2.0 \times 10^{-10}$, and $a_3 = 3.3 \times 10^{-20}$. This limit applies from DC to 3.125 GHz. The magnitude response above 3.125 GHz does not exceed –11.4 dB. The ISI loss, defined as the difference in magnitude response between two frequencies, is greater than 4.0 dB between 312.5 MHz and 1.5625 GHz. The magnitude response and ISI loss limits are illustrated in Figure 47–6.

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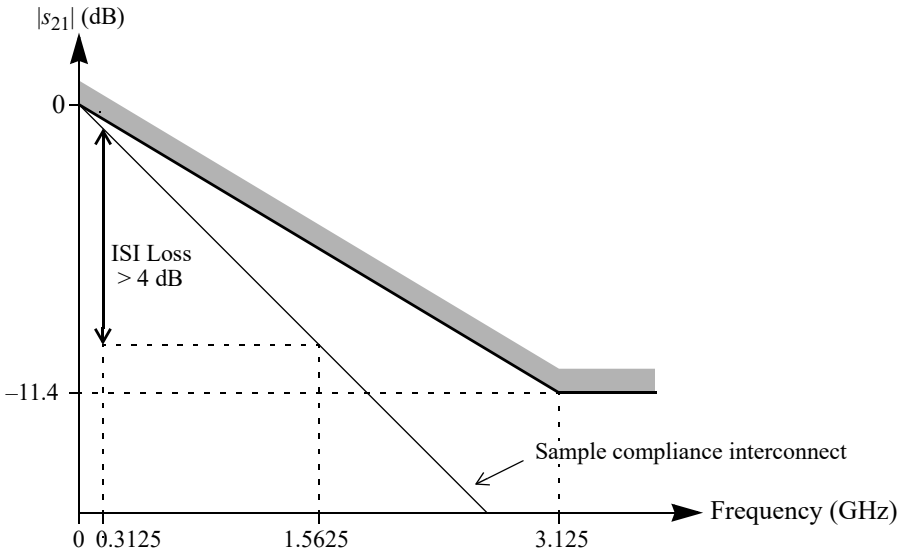

Figure 47–6—Compliance interconnect magnitude response and ISI loss

47.4.2 Eye template measurements

For the purpose of eye template measurements, the effect of a single-pole high-pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. See 48B.1.3 for an explanation of this technique. The data pattern for template measurements is the CJPAT pattern defined in Annex 48A. All XAUI lanes are active in both the transmit and receive directions, and opposite ends of the link use asynchronous clocks. The amount of data represented in the data eye needs to be adequate to ensure a bit error ratio of less than 10^{-12}. The eye template is measured with AC-coupling and centered at 0 volts differential. The left and right edges of the template are aligned with the mean zero crossing points of the measured data eye, as illustrated in Figure 47–7. The near-end load for this test is specified in 47.3.3.1. The far-end template is measured at the end of the compliance interconnect specified in 47.4.1. The far-end load for the compliance link is specified in 47.3.3.1.

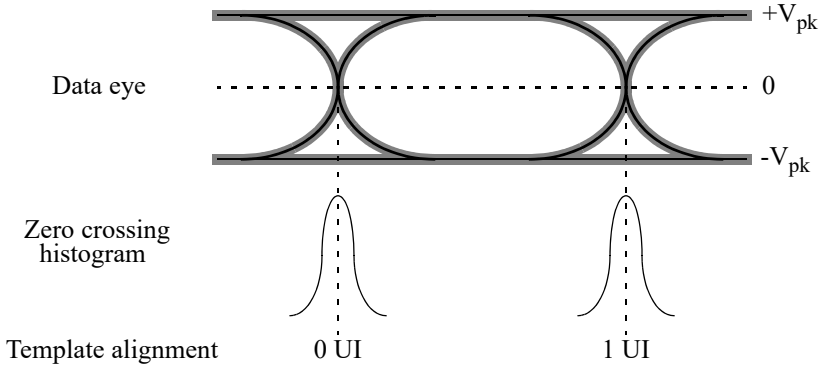

Figure 47–7—Eye template alignment

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47.4.3 Jitter test requirements

For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements is the CJPAT pattern defined in Annex 48A. All four lanes of XAUI are active in both directions, and opposite ends of the link use asynchronous clocks. Jitter is measured with AC-coupling and at 0 volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER bathtub curve such as that described in Annex 48B.

47.4.3.1 Transmit jitter

Transmit near-end jitter is measured at the driver output when terminated into the load specified in 47.3.3.1. Far-end jitter is measured at the end of a compliance interconnect specified in 47.4.1. The far-end load for the compliance link is specified in 47.3.3.1.

47.4.3.2 Jitter tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the required sum of deterministic and random jitter defined in 47.3.4.6 and then adjusting the signal amplitude until the data eye contacts the 6 points of the driver's template shown in Figure 47–4 and Table 47–2. Note that for this to occur, the test signal has to have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean of the zero crossing. If these symmetries are not achieved, then some portions of the test signal will encroach into the template and provide overstress of the receiver, and/or some points of the template may not be contacted, resulting in understress of the receiver. Eye template measurement requirements are given in 47.4.2. Random jitter is calibrated using a high-pass filter with a low-frequency corner of 20 MHz and 20 dB/decade rolloff below this. The required sinusoidal jitter specified in 47.3.4.6 is then added to the signal and the far-end load is replaced by the receiver being tested.

47.5 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801:1995.

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47.6 Protocol implementation conformance statement (PICS) proforma for Clause 47, XGMII Extender (XGMII) and 10 Gigabit Attachment Unit Interface (XAUI)[89]

47.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 47, XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI), shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

47.6.2 Identification

47.6.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

47.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 47, XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[89] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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47.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XGE	XGMII compatibility interface	46, 47.1.4	Compatibility interface is supported	O	Yes [ ] No [ ]
MD	MDIO	47.2	Registers and interface supported	O	Yes [ ] No [ ]
LPI	Implementation of LPI	47.1		O	Yes [ ] No [ ]

47.6.4 PICS proforma tables for XGXS and XAUI

47.6.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Environmental specifications	47.5		M	Yes [ ]

47.6.4.2 XGXS and XAUI functions

Item	Feature	Subclause	Value/Comment	Status	Support
F1	XGXS PCS and PMA requirements	47.2.1	Meet all mandatory requirements of 48.2 and 48.3	M	Yes [ ]
F2	XGXS PCS and PMA options	47.2.1	Meet optional clock rate compensation in unencoded data stream per 48.2.4.2.3	O	Yes [ ] No [ ]
F3	XGMII Extender delay	47.2.2	Meets delay constraints of 48.5	M	Yes [ ]

47.6.4.3 Electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
E1	XAUI Baud	47.3.3	3.125 GBd ± 100 ppm	M	Yes [ ]
E2	Driver output amplitude	47.3.3.2	Less than 1600 mV_{p-p}	M	Yes [ ]
E3	Driver output swing	47.3.3.2	Between –0.4 and +2.3 V	M	Yes [ ]
E4	Driver output impedance	47.3.3.4	s_{11} = –10 dB for 312.5 MHz < Freq (f) < 625 MHz, and –10 + 10log(f/625) dB for 625 MHz ≤ Freq (f)≤ 3.125 GHz (f is frequency in MHz)	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
E5	Driver near-end template and jitter	47.3.3.5	At driver output	O.1	Yes [ ] No [ ]
E6	Driver far-end template and jitter	47.3.3.5	At end of compliance interconnect	O.1	Yes [ ] No [ ]
E7	Receiver bit error ratio	47.3.4	Less than 10^{-12}	M	Yes [ ]
E8	Receive input amplitude tolerance	47.3.4.3	May be larger than 1600 mV_{p-p}	M	Yes [ ]
E9	Receiver coupling	47.3.4.4	AC-coupled	M	Yes [ ]
E10	Receiver input impedance	47.3.4.5	At least 10 dB differential and 6 dB common-mode return loss	M	Yes [ ]
E11	Total jitter tolerance	47.3.4.6	At least 0.65 UI	M	Yes [ ]
E12	Deterministic jitter tolerance	47.3.4.6	At least 0.37 UI	M	Yes [ ]
E13	Tolerance to sum of deterministic and random jitter	47.3.4.6	At least 0.55 UI	M	Yes [ ]
E14	Additional sinusoidal jitter tolerance	47.3.4.6	Per Figure 47–5	M	Yes [ ]
E15	Jitter measurement	47.4.3	Meet BER bathtub curve, See Annex 48B	M	Yes [ ]

47.6.4.4 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
LP-01	Global signal detect	47.1.5	Meets the requirements of 47.1.5	LPI:M	Yes [ ] No [ ]
LP-02	Global transmit disable	47.1.6	Meets the requirements of 47.1.6	LPI:M	Yes [ ] No [ ]
LP-03	Transmit amplitude	47.3.3.2	Meets the requirements of 47.3.3.2	LPI:M	Yes [ ] No [ ]
LP-04	Signal detect timing	47.3.4	Meets the requirements of Table 47–3	LPI:M	Yes [ ] No [ ]

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48. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X

48.1 Overview

This clause specifies the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer that are common to a family of 10 Gb/s Physical Layer implementations, collectively known as 10GBASE-X. The 10GBASE-X PHY family consists of 10GBASE-CX4 (see Clause 54), 10GBASE-KX4 (see Clause 71), and 10GBASE-LX4 (see Clause 53).

The 10GBASE-X PCS and PMA sublayers are also utilized by the XGXS specified in Clause 47.

10GBASE-X PCS and PMA sublayers map the interface characteristics of the PMD sublayer (including MDI) to the services expected by the Reconciliation Sublayer (RS) and the logical and electrical characteristics of the 10 Gigabit Media Independent Interface (XGMII). Although the XGMII is optional, it is used as the basis for the definition of the 10GBASE-X PCS and PMA sublayers.

10GBASE-X assumes the use of the MDIO interface and register set for communication between PHY and Station Management (STA) entities, see Clause 45.

10GBASE-X has the following characteristics:

a) The capability of supporting 10 Gb/s operation at the XGMII and RS
b) Clock references embedded in all data and control code-groups
c) Data paths consisting of independent serial links called lanes
d) Independent four-lane-wide transmit and receive data paths
e) Simple signal mapping to the XGMII and RS
f) Full duplex operation
g) Shared technology with other 10 Gb/s interfaces
h) Shared functionality with other 10 Gb/s Ethernet blocks

48.1.1 Objectives

The following are the objectives of 10GBASE-X:

a) Support the IEEE 802.3 MAC
b) Provide a data rate of 10 Gb/s at the XGMII
c) Support cable plants using cabled optical fiber compliant with second edition of ISO/IEC 11801:1995
d) Support a BER objective of 10^{-12}
e) Support the optional XAUI
f) Support link fault and error indications

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48.1.2 Relationship of 10GBASE-X to other standards

Figure 48–1 depicts the relationships among the 10GBASE-X sublayers (shown shaded), the IEEE 802.3 MAC and RS, and the IEEE 802.2 LLC.

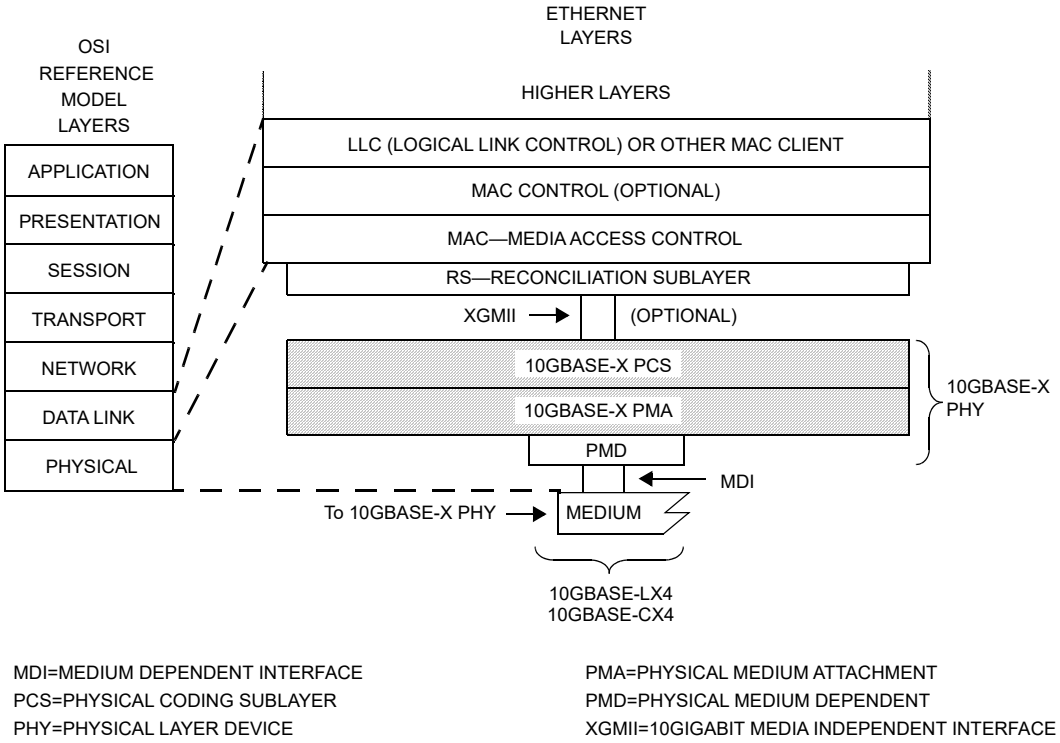

Figure 48–1—10GBASE-X PCS and PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE Ethernet Model

48.1.3 Summary of 10GBASE-X sublayers

The following provides an overview of the 10GBASE-X sublayers.[90]

48.1.3.1 Physical Coding Sublayer (PCS)

The interface between the PCS and the RS is the XGMII as specified in Clause 46. The 10GBASE-X PCS provides services to the XGMII in a manner analogous to how the 1000BASE-X PCS provides services to the 1000 Mb/s GMII.

The 10GBASE-X PCS provides all services required by the XGMII and in support of the 10GBASE-X PMA, including:

a) Encoding of 32 XGMII data bits and 4 XGMII control bits to four parallel lanes conveying 10-bit code-groups each, for communication with the underlying PMA.
b) Decoding of four PMA parallel lanes, conveying 10-bit code-groups each, to 32 XGMII data bits and 4 XGMII control bits.
c) Synchronization of code-groups on each lane to determine code-group boundaries.

[90] The 10GBASE-X PHY consists of that portion of the Physical Layer between the MDI and XGMII consisting of the PCS, PMA, and PMD sublayers. The 10GBASE-X PHY is roughly analogous to the 1000BASE-X PHY.

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d) Deskew of received code-groups from all lanes to an alignment pattern.
e) Support of the MDIO interface and register set as specified in Clause 45 to report status and enable control of the PCS.
f) Conversion of XGMII Idle control characters to (from) a randomized sequence of code-groups to enable serial lane synchronization, clock rate compensation and lane-to-lane alignment.
g) Clock rate compensation protocol.
h) Link Initialization based on the transmission and reception of the Idle sequence.
i) Link status reporting for fault conditions.

48.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS to support the use of a range of serial-bit-oriented physical media. The 10GBASE-X PMA performs the following functions:

a) Mapping of transmit and receive code-groups between the PCS and PMA via the PMA service interface.
b) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMD.
c) Clock recovery from the code-groups supplied by the PMD.
d) Mapping of transmit and receive bits between the PMA and PMD via the PMD service interface.
e) Direct passing of signal_detect from the PMD to the PCS through the PMA via the PMD and PMA service interfaces.

48.1.3.3 Physical Medium Dependent (PMD) sublayer

10GBASE-X uses the PMD sublayer and MDI specified in Clause 53, Clause 54, and Clause 71. The 10GBASE-CX4, 10GBASE-KX4, and 10GBASE-LX4 perform the following functions:

a) Transmission of quad serial bit streams on the underlying medium.
b) Reception of quad serial bit streams on the underlying medium.

48.1.4 Rate of operation

The 10GBASE-X PCS and PMA support the 10 Gb/s MAC data rate. The line rate of each of four PMA lanes is 3.125 GBd ± 100 ppm.

48.1.5 Allocation of functions

PCS and PMA functions directly map onto the 10GBASE-X PMD, MDI and medium which attach, in turn, to another 10GBASE-X PHY. In addition, 10GBASE-X PCS and PMA functions embodied in the XGXS described in Clause 47 may be used to attach to alternate 10 Gb/s PHYs such as 10GBASE-R or 10GBASE-W.

The longer interconnect distances afforded through the specification of a self-clocked serial architecture enable significant implementation flexibility while imposing a requirement on those implementations to ensure sufficient signal fidelity over the link. The implementer of this standard is expected to meet the required specifications in this and related clauses through implementation methods not specified by this standard.

Certain PHYs support Energy-Efficient Ethernet (EEE) (see Clause 78). PHYs that support EEE (see 78.3) use Low Power Idle (LPI) signaling to allow systems on both sides of the link to save power during periods of low link utilization. LPI signaling may optionally be used by XGXS to extend the EEE function to attached PHYs. Both PHY and DTE XGXS may optionally use LPI signaling to control the shutdown of signals on the XAUI to reduce power for PHY attachments.

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48.1.6 Inter-sublayer interfaces

There are a number of interfaces employed by 10GBASE-X. Some (such as the PMA service interface) use an abstract service model to define the operation of the interface. Figure 48–2 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 10GBASE-X.

Multiple optional physical instantiations of the PCS service interface have been defined. One is the XGMII described in Clause 46. The other is the interface to the XGXS described in Clause 47.

Physical instantiations of the 10GBASE-X PMA and PMD service interfaces are not defined in this standard.

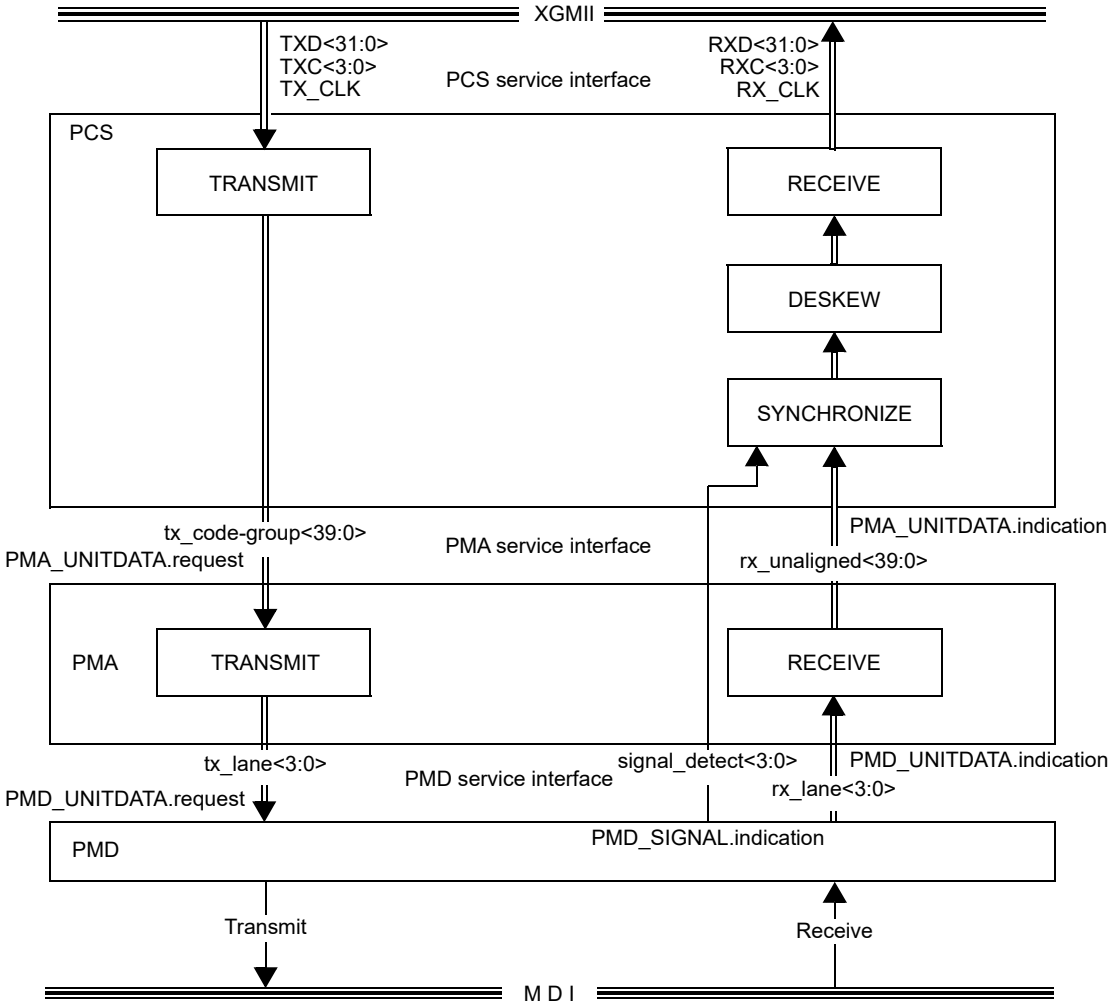

Figure 48–2—Functional block diagram

48.1.7 Functional block diagram

Figure 48–2 provides a functional block diagram of the 10GBASE-X PHY.

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48.1.8 Special symbols

/x/ The code-group x is represented by preceding and following slash characters.

||y|| Four code-groups, one each in lanes 0 through 3 inclusive, synchronous to each other and arranged in a column identified by the value y, is represented by preceding and following double bar characters.

48.2 Physical Coding Sublayer (PCS)

48.2.1 PCS service interface (XGMII)

The PCS service interface allows the 10GBASE-X PCS to transfer information to and from the PCS client. The PCS client is the RS defined in Clause 46, or the XGXS defined in Clause 47. An instantiation of the PCS service interface is the XGMII defined in Clause 46.

In the transmit direction, the 10GBASE-X PCS accepts packets from the PCS client on the XGMII. Due to the continuously signaled nature of the underlying PMA, and the encoding performed by the PCS, the 10GBASE-X PCS maps XGMII data and control characters into a code-group stream. In the receive direction, the PCS decodes the code-group stream received from the PMA, maps the code-groups to XGMII data and control characters and forwards the character stream to the XGMII to the PCS client for further processing.

48.2.2 Functions within the PCS

The PCS includes the Transmit, Receive, Synchronization, and Deskew processes for 10GBASE-X. The PCS shields the RS (and MAC) from the specific nature of the underlying channel.

When communicating with the XGMII, the PCS uses, in each direction, 32 data signals (TXD <31:0> and RXD <31:0>), four control signals (TXC <3:0> and RXC <3:0>), and a clock (TX_CLK and RX_CLK).

When communicating with the PMA, the PCS uses the data signals tx_code-group <39:0> in the transmit direction and rx_unaligned <39:0> in the receive direction. Each set of data signals conveys four lanes of 10-bit code-groups. At the PMA service interface, code-group alignment, lane-to-lane deskew, and provision for PHY clock rate compensation are made possible by embedding special non-data code-groups in the idle stream. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

The tx_code-group and rx_unaligned signals are organized into four lanes in a manner similar to that of the XGMII. On transmit, the first PCS code-group is aligned to lane 0, the second to lane 1, the third to lane 2, the fourth to lane 3, then repeating with the fifth to lane 0, etc. This lane-oriented organization extends through the PMA to the PMD service interface. (See Table 48–1.)

The PCS Transmit process continuously generates code-groups based upon the TXD <31:0> and TXC <3:0> signals on the XGMII, sending them to the PMA service interface via the PMA_UNITDATA.request primitive.

The PCS Synchronization process continuously accepts unaligned and unsynchronized code-groups via the PMA_UNITDATA.indication primitive, obtains 10-bit code-group synchronization, and conveys synchronized 10-bit code-groups to the PCS Deskew process via the SYNC_UNITDATA.indicate message. The PCS Synchronization process sets the lane_sync_status <3:0> flags to indicate whether the PMA is functioning dependably (as well as can be determined without exhaustive error-ratio analysis).

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Table 48–1—Transmit and receive lane associations

Lane	XGMII TXD RXD	XGMII TXC RXC	PMA tx_code-group rx_unaligned	PMD tx_lane rx_lane
0	<7:0>	<0>	<9:0>	<0>
1	<15:8>	<1>	<19:10>	<1>
2	<23:16>	<2>	<29:20>	<2>
3	<31:24>	<3>	<39:30>	<3>

The PCS Deskew process continuously accepts synchronized code-groups via the SYNC_UNITDATA.indicate message, aligns the code-groups to remove skew between the lanes that has been introduced by the link, and conveys aligned and synchronized code-groups to the PCS Receive process via the ALIGN_UNITDATA.indicate message. The PCS Deskew process asserts the align_status flag to indicate that the PCS has successfully deskewed and aligned code-groups on all PCS lanes. The PCS Deskew process attempts deskew and alignment whenever the align_status flag is de-asserted. The PCS Deskew process is otherwise idle.

The PCS Receive process continuously accepts code-groups from the PMA service interface via the ALIGN_UNITDATA.indicate message. The PCS Receive process monitors these code-groups and generates RXD and RXC on the XGMII. All code-groups received that represent idle are replaced with Idle characters prior to forwarding to the XGMII.

The PCS Transmit and Receive processes provide support for Link status reporting, which supports the transmit fault and receive fault conditions.

All PCS processes are described in detail in the state diagrams in 48.2.6.2.

48.2.3 Use of code-groups

The transmission code used by the PCS, referred to as 8B/10B, is identical to that specified in Clause 36. The PCS maps XGMII characters into 10-bit code-groups, and vice versa, using the 8B/10B block coding scheme. Implicit in the definition of a code-group is an establishment of code-group boundaries by a PCS Synchronization process. The 8B/10B transmission code as well as the rules by which the PCS ENCODE and DECODE functions generate, manipulate, and interpret code-groups are specified in 36.2.4. A 10GBASE-X PCS shall meet the requirements specified in 36.2.4.1 through 36.2.4.6, 36.2.4.8, and 36.2.4.9. PCS lanes are independent of one another. All code-group rules specified in 36.2.4 are applicable to each lane. The mapping of XGMII characters to PCS code-groups is specified in Table 48–2. The mapping of PCS code-groups to XGMII characters is specified in Table 48–3. PHYs that support EEE are able to transmit and receive LPI characters.

Figure 48–3 illustrates the mapping of an example XGMII character stream into a PCS code-group stream. Figure 48–4 illustrates the mapping during LPI.

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The relationship of code-group bit positions to XGMII, PCS and PMA constructs and PMD bit transmission order, exemplified for lane 0, is illustrated in Figure 48–5.

XGMII																		
T/RXD<7:0>	I	I	S	Dp	D	D	D	---	D	D	D	D	I	I	I	I	I	I
T/RXD<15:8>	I	I	Dp	Dp	D	D	D	---	D	D	D	T	I	I	I	I	I	I
T/RXD<23:16>	I	I	Dp	Dp	D	D	D	---	D	D	D	I	I	I	I	I	I	I
T/RXD<31:24>	I	I	Dp	Ds	D	D	D	---	D	D	D	I	I	I	I	I	I	I

PCS																		
LANE 0	K	R	S	Dp	D	D	D	---	D	D	D	D	A	R	R	K	K	R
LANE 1	K	R	Dp	Dp	D	D	D	---	D	D	D	T	A	R	R	K	K	R
LANE 2	K	R	Dp	Dp	D	D	D	---	D	D	D	K	A	R	R	K	K	R
LANE 3	K	R	Dp	Ds	D	D	D	---	D	D	D	K	A	R	R	K	K	R

Legend:
Dp represents a data character containing the preamble pattern
Ds represents a data character containing the SFD pattern

Figure 48–3—XGMII character stream to PCS code-group stream mapping example

			LPI sleep/quiet/refresh									wake time						
XGMII																		
T/RXD<7:0>	I	I	LI	LI	LI	LI	LI	---	LI	LI	LI	I	I	---	I	S	Dp	D
T/RXD<15:8>	I	I	LI	LI	LI	LI	LI	---	LI	LI	LI	I	I	---	I	Dp	Dp	D
T/RXD<23:16>	I	I	LI	LI	LI	LI	LI	---	LI	LI	LI	I	I	---	I	Dp	Dp	D
T/RXD<31:24>	I	I	LI	LI	LI	LI	LI	---	LI	LI	LI	I	I	---	I	Dp	Ds	D
	active time														active time			
PCS																		
LANE 0	K	R	R	K	R	A	K	---	LL	R	K	K	A	---	R	S	Dp	D
LANE 1	K	R	LL	K	R	A	K	---	R	R	K	K	A	---	R	Dp	Dp	D
LANE 2	K	R	R	K	LL	A	LL	---	R	R	LL	K	A	---	R	Dp	Dp	D
LANE 3	K	R	R	LL	R	A	K	---	R	LL	K	K	A	---	R	Dp	Ds	D

Legend:
LI represents the data character containing the XGMII LPI pattern (06)
LL represents the LPI indication code-group /D20.5/
Dp represents a data character containing the preamble pattern
Ds represents a data character containing the SFD pattern

Figure 48–4—XGMII and PCS mapping example with optional LPI

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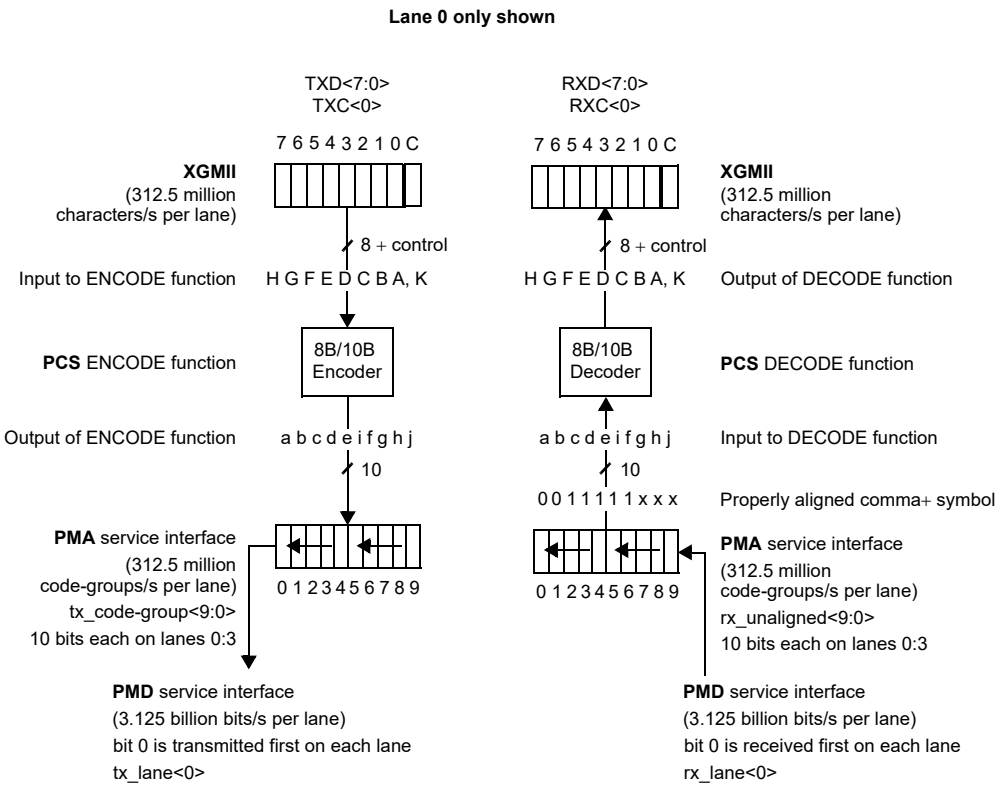

Figure 48–5—PCS reference diagram

48.2.4 Ordered sets and special code-groups

10GBASE-X PCS ordered sets consist of combinations of special and data code-groups (defined as a column of code-groups). All ordered sets are four code-groups in length and begin in lane 0. In addition to ordered sets, the PCS defines several special code-groups for control purposes. Ordered sets and special code-groups provide the following capabilities:

a) PCS Synchronization process ability to obtain bit and code-group synchronization
b) Packet delineation
c) Synchronization between the transmitter and receiver circuits at opposite ends of a link
d) Deskew of received code-groups from all serial lanes to an alignment pattern
e) Clock rate compensation protocol
f) Link status reporting protocol
g) Column fill
h) Error indication

Table 48–4 lists the defined ordered sets and special code-groups.

48.2.4.1 Data (/D/)

A data code-group, when not used to distinguish or convey information for a defined ordered set, conveys one octet of data between the XGMII and the PCS. Any data code-group can be followed by any other data code-group. Data code-groups are encoded and decoded but not interpreted by the PCS.

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Table 48–2—XGMII character to PCS code-group mapping

XGMII TXC	XGMII TXD	PCS code-group	Description
0	00 through FF	Dxx.y	Normal data transmission
1	06	K28.0 or K28.3 or K28.5 or D20.5[a]	Assert LPI
1	07	K28.0 or K28.3 or K28.5	Idle in ||I||
1	07	K28.5	Idle in ||T||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	Other value in Table 36–2	See Table 36–2	Reserved XGMII character
1	Any other value	K30.7	Invalid XGMII character
NOTE—Values in TXD column are in hexadecimal.			

[a]Insertion of /D20.5/ is per the rules described in 48.2.4.2.

Table 48–3—PCS code-group to XGMII character mapping

XGMII RXC	XGMII RXD	PCS code-group	Description
0	00 through FF	Dxx.y	Normal data reception
1	06	K28.0 or K28.3 or K28.5 or D20.5[a]	Assert LPI
1	07	K28.0 or K28.3 or K28.5	Idle in ||I||
1	07	K28.5	Idle in ||T||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	FE	Invalid code-group	Received code-group
1	See Table 36–2	Other valid code-group	Received reserved code-group
NOTE—Values in RXD column are in hexadecimal.			

[a]Insertion of /D20.5/ is per the rules described in 48.2.4.2.

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Table 48–4—Defined ordered sets and special code-groups

Code	Ordered set	Number of code-groups	Encoding
||I||	**Idle**		**Substitute for XGMII Idle**
||K||	Sync column	4	/K28.5/K28.5/K28.5/K28.5/
||R||	Skip column	4	/K28.0/K28.0/K28.0/K28.0/
||A||	Align column	4	/K28.3/K28.3/K28.3/K28.3/
	Encapsulation		
||S||	Start column	4	/K27.7/Dx.y/Dx.y/Dx.y/[a]
||T||	Terminate column	4	Terminate code-group in any lane
$\|\|T_0\|\|$	Terminate in Lane 0	4	/K29.7/K28.5/K28.5/K28.5/
$\|\|T_1\|\|$	Terminate in Lane 1	4	/Dx.y/K29.7/K28.5/K28.5/[a]
$\|\|T_2\|\|$	Terminate in Lane 2	4	/Dx.y/Dx.y/K29.7/K28.5/[a]
$\|\|T_3\|\|$	Terminate in Lane 3	4	/Dx.y/Dx.y/Dx.y/K29.7/[a]
	Control		
/E/	Error code-group	1	/K30.7/
	Link Status		
||Q||	Sequence ordered set	4	/K28.4/Dx.y/Dx.y/Dx.y/[a]
||LF||	Local Fault signal	4	/K28.4/D0.0/D0.0/D1.0/
||RF||	Remote Fault signal	4	/K28.4/D0.0/D0.0/D2.0/
||LINT||	Link Interruption signal	4	/K28.4/D0.0/D0.0/D3.0/
||Qrsvd||	Reserved	4	!||LF|| and !||RF|| and !||LINT||
	Reserved		
||Fsig||	Signal ordered set	4	/K28.2/Dx.y/Dx.y/Dx.y/[a,b]

[a]/Dx.y/ indicates any data code-group.
[b]Reserved for INCITS T11.

48.2.4.2 Idle (||I||) and Low Power Idle (||LPIDLE||)

Idle ordered sets (||I||) are transmitted in full columns continuously and repetitively whenever the XGMII is idle (TXD <31:0>=0x07070707 and TXC <3:0>=0xF). ||I|| provides a continuous fill pattern to establish and maintain lane synchronization, perform lane-to-lane deskew and perform PHY clock rate compensation. ||I|| is emitted from, and interpreted by, the PCS.

A sequence of ||I|| ordered sets consists of one or more consecutively transmitted ||K||, ||R||, or ||A|| ordered sets, as defined in Table 48–4. Rules for ||I|| ordered set sequencing shall be as follows:

a) ||I|| sequencing starts with the first column following a ||T||.
b) The first ||I|| following ||T|| alternates between ||A|| or ||K|| except if an ||A|| is to be sent and less than *r* [see item d)] columns have been sent since the last ||A||, a ||K|| is sent instead.

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c) ||R|| is chosen as the second ||I|| following ||T||.
d) Each ||A|| is sent after *r* non-||A|| columns where *r* is a randomly distributed number between 16 and 31, inclusive. The corresponding minimum spacing of 16 non-||A|| columns between two ||A|| columns provides a theoretical 85-bit deskew capability.
e) When not sending an ||A||, either ||K|| or ||R|| is sent with a random uniform distribution between the two.
f) Whenever sync_status=OK, all ||I|| received during idle are translated to XGMII Idle control characters for transmission over the XGMII. All other !||I|| received during idle are mapped directly to XGMII data or control characters on a lane by lane basis, with the following exceptions for PHYs with EEE capability:
    1) /D20.5/ (LPI) being detected in any lane and the rest of the lanes in the same column being detected /K/ only or /R/ only, which will result in reporting LP_IDLE characters in all lanes.
    2) ||A|| being detected and /D20.5/ (LPI) being detected in any lane of the previous column and the rest of the lanes in the previous column being detected /K/ only or /R/ only, which will result in reporting LP_IDLE characters in all lanes.

The purpose of randomizing the ||I|| sequence is to reduce 10GBASE-X electromagnetic interference (EMI) during idle. The randomized ||I|| sequence produces no discrete spectrum. Both ||A|| spacing as well as ||K||, ||R||, or ||A|| selection shall be based on the generation of a random integer *r* generated by a PRBS based on one of the 7th order polynomials listed in Figure 48–6. ||A|| spacing is set to the next generated value of *r*. The rate of generation of *r* is once per column, 312.5 MHz ± 100 ppm. Once the ||A|| spacing count goes to zero (A_CNT=0), ||A|| is selected for transmission at the next opportunity during the Idle sequence. ||K|| and ||R|| selection follows the value of code_sel, which is continuously set according to the even or odd value of *r*. The method of generating the random integer *r* is left to the implementer. PCS Idle randomizer logic is illustrated in Figure 48–6.

||LPIDLE|| is coded in the same manner as ||I|| except that the /D20.5/ code-group replaces one code-group in each ||K|| or ||R|| (not ||A||) column with a random uniform distribution across the lanes. Insertion of /D20.5/ does not alter the distribution of ||A||, ||K|| or ||R||. Clock compensation may be performed during LPI according to the rules described in 48.2.4.2.3.

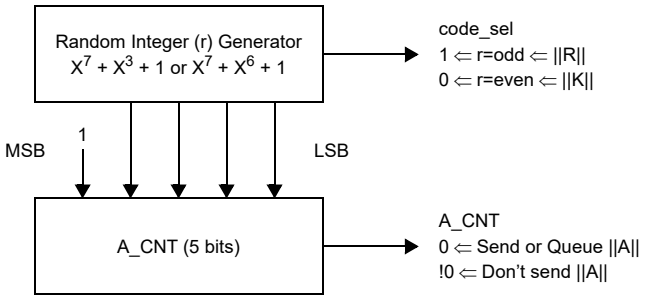

Figure 48–6—PCS idle randomizer

48.2.4.2.1 Sync ||K||

Code-group synchronization is the process by which the receiver detects code-group boundaries in the incoming bit stream of each lane. The detection of the comma pattern in the incoming bit stream identifies a code-group boundary. The proper alignment of a comma used for code-group synchronization is depicted in Figure 48–5. The Sync or ||K|| ordered set included in the PCS Idle sequence guarantees a sufficient frequency of commas in each lane. The comma pattern is defined in 36.2.4.9. The Sync ordered set is

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defined in Table 48–4. /K/ code-groups are interpreted per lane by the PCS Synchronization process, which is described in 48.2.6.2.2. Detection of both comma+ and comma- variants of /K/ shall be required.

48.2.4.2.2 Align ||A||

Skew is introduced between lanes by both active and passive elements of a 10GBASE-X link. The PCS deskew function compensates for all lane-to-lane skew observed at the receiver. The Align or ||A|| ordered set consists of a unique special code-group, also known as Align or /A/ in each lane. /A/ is not used in any other ordered set. The definition of a 10GBASE-X ordered set guarantees that /A/ code-groups are simultaneously initiated on all lanes at the transmitter, resulting in minimal lane-to-lane skew at the transmitter. The Align ordered set is defined in Table 48–4. Allowable skew for all link elements shall be as specified in Table 48–5.

Table 48–5—Skew budget

Skew Source	Occurences	Skew	Total Skew
PMA Tx	1	1 UI[a]	1 UI
PCB	2	1 UI	2 UI
Medium	1	<18 UI	<18 UI
PMA Rx[b]	1	20 UI	20 UI
Total			<41 UI

[a]UI represents unit interval. For 10GBASE-X, 1 UI = 320 ps.
[b]Includes deserialization function, physical deserializer skew and clock boundary transition.

48.2.4.2.3 Skip ||R||

The 10GBASE-X PHY allows for multiple clock domains along a single link. The Skip or ||R|| ordered set is included in the PCS Idle sequence to allow for clock rate compensation for the case of multiple clock domains. Clock rate compensation may be performed via insertion or removal of either Idle characters in the unencoded data stream or ||R|| in the encoded Idle stream. Any ||R|| may be removed. ||R|| may be inserted anywhere in the Idle stream with the exception of the first column following ||T||.

When clock compensation is done in the unencoded data stream, rules for idle insertion and deletion shall be as follows:

a) Idle insertion or deletion occurs in groups of four consecutive Idle characters.
b) Idle characters are added following idle or ordered sets.
c) Idle characters are not added while data is being received.
d) The four characters following a Terminate control character are not deleted.
e) Sequence ordered sets are deleted to adapt between clock rates.
f) Sequence ordered set deletion occurs only when two consecutive sequence ordered sets have been received and deletes only one of the two.
g) Only idles are inserted for clock compensation.

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The disparity of the /R/ code-group is neutral, allowing its removal or insertion without affecting the current running disparity of the serial stream. The correct current running disparity version of /R/ has to be inserted in each lane during Skip insertion (see Table 36–2). The Skip ordered set is defined in Table 48–4.

For EEE capability, a column containing three /R/ code-groups and one /D20.5/ code-group may be inserted or deleted in the same manner as four /R/ code-groups.

48.2.4.3 Encapsulation

The Start and Terminate ordered sets correspond to columns containing the XGMII Start and Terminate control characters, respectively.

48.2.4.3.1 Start ||S||

The Start or ||S|| ordered set directly maps to the XGMII Start control character in lane 0 followed by any three data characters in XGMII lanes 1 through 3. Normally, the three data characters will be the preamble pattern, but the PCS neither checks nor alters their contents. ||S|| indicates to the PCS that a packet has been initiated. The Start ordered set is defined in Table 48–4.

48.2.4.3.2 Terminate ||T||

The Terminate or ||T|| ordered set directly maps to the XGMII Terminate control character located in any lane, preceded by data characters if Terminate is not in lane 0, and followed by Idle characters if Terminate is not in lane 3. ||T|| indicates to the PCS that a packet has been terminated. All XGMII control characters following ||T|| are translated by the PCS until the recognition of the next XGMII Start control character. The PCS considers the MAC interpacket gap (IPG) to have begun with the reception of ||T||. The Terminate ordered set is defined in Table 48–4.

Unrecognized running disparity errors which propagate to any Idle code-groups in ||T|| or to the column following ||T|| are indicated as /E/ in the preceding column in the same lane in which the errors were recognized. All ||I|| ordered sets are selected to ensure that propagated code violations are recognized and not propagated further.

The cvtx_terminate function is used to convert all XGMII Idle control characters in the same column as the XGMII Terminate control character to /K/ code-groups. The cvrx_terminate function is used to convert all /K/ code-groups in ||T|| to XGMII Idle control characters.

48.2.4.4 Error /E/

The Error code-group is directly mapped to the XGMII Error control character. /E/ may also be generated by the PCS client to indicate a transmission error to its peer entity or deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability. Error is signaled per lane since code-violations are detected on a per lane basis. The Error code-group is defined in Table 48–4.

The presence of /E/ or any invalid code-group on the medium denotes an error condition. 10GBASE-X elements that detect code-group violations shall replace the invalid code-group with /E/ prior to retransmission.

48.2.4.5 Link status

Link status reporting uses the Sequence ordered-set to transport the transmit fault and receive fault link status conditions.

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48.2.4.5.1 Sequence ||Q||

The Sequence or ||Q|| ordered set directly maps to the XGMII Sequence control character on lane 0 followed by three data characters in XGMII lanes 1 through 3. ||Q|| indicates to the PCS that a link status message has been initiated. The PCS Receive process may also initiate Sequence ordered-sets upon detection of a link status condition. Sequence ordered-sets are always sent over the PMA service interface in the column that follows an ||A|| ordered-set. The Sequence ordered-sets do not otherwise interfere with the randomized ||I|| sequence. Sequence ordered-sets corresponding to Local Fault signal and Remote Fault signal are specified in Table 48–4.

48.2.5 Management function requirements

The 10GBASE-X PCS supports a set of required and optional management objects to permit it to be controlled by the Station Management entity (STA). Access to management objects within the 10GBASE-X sublayer is accomplished by means of a set of registers within the MDIO register space as defined in 45.2.4 and 45.2.5. The details of the register bit allocations and general usage are given in Clause 45. Table 48–6, Table 48–7, and Table 48–8 describe how the PCS state diagram variables map to management register bits. If an MDIO interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

Table 48–6—State diagram variable to management register mapping for PCS

State diagram variable	Management register bit
reset	3.0.15 Reset
sync_status	3.24.12 10GBASE-X lane alignment status
lane_sync_status<3>	3.24.3 Lane 3 sync
lane_sync_status<2>	3.24.2 Lane 2 sync
lane_sync_status<1>	3.24.1 Lane 1 sync
lane_sync_status<0>	3.24.0 Lane 0 sync

Table 48–7—State diagram variable to management register mapping for PHY XS

State diagram variable	Management register bit
reset	4.0.15 Reset
align_status	4.8.10 Receive fault
sync_status	4.24.12 PHY XGXS lane alignment status
lane_sync_status<3>	4.24.3 Lane 3 sync
lane_sync_status<2>	4.24.2 Lane 2 sync
lane_sync_status<1>	4.24.1 Lane 1 sync
lane_sync_status<0>	4.24.0 Lane 0 sync

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Table 48–8—State diagram variable to management register mapping for DTE XS

State diagram variable	Management register bit
reset	5.0.15 Reset
align_status	5.8.10 Receive fault
sync_status	5.24.12 PHY XGXS lane alignment status
lane_sync_status<3>	5.24.3 Lane 3 sync
lane_sync_status<2>	5.24.2 Lane 2 sync
lane_sync_status<1>	5.24.1 Lane 1 sync
lane_sync_status<0>	5.24.0 Lane 0 sync

48.2.6 Detailed functions and state diagrams

The body of this clause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams in this clause follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

Timeless states are employed as an editorial convenience to facilitate the distribution of transition conditions from prior states. No actions are taken within these states. Exit conditions are evaluated for timeless states. There is one timeless state. It is PCS Receive state RECEIVE.

48.2.6.1 State variables

48.2.6.1.1 Notation conventions

/x/
: Denotes the constant code-group specified in 48.2.6.1.2 (valid code-groups have to follow the rules of running disparity as per 36.2.4.5 and 36.2.4.6).

[/x/]
: Denotes the latched received value of the constant code-group (/x/) specified in 48.2.6.1.2 and conveyed by the SYNC_UNITDATA.indicate message described in 48.2.6.1.7.

||y||
: Denotes the column of constant code-groups in lanes 0 through 3, inclusively, specified in 48.2.6.1.2 (valid code-groups have to follow the rules of running disparity as per 36.2.4.5 and 36.2.4.6).

[||y||]
: Denotes the latched received value of the column of constant code-groups in lanes 0 through 3, inclusively (||y||), specified in 48.2.6.1.2 and conveyed by the SYNC_UNITDATA.indicate message described in 48.2.6.1.7 or the ALIGN_UNITDATA.indicate message described in 48.2.6.1.7.

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48.2.6.1.2 Constants

/A/
: The /K28.3/ code-group used in the Idle Align function specified in 48.2.4.2.2.

||A||
: The column of four identical Idle Align code-groups corresponding to the Idle Align function specified in 48.2.4.2.2.

/COMMA/
: The set of special code-groups which include a comma as specified in 36.2.4.9 and listed in Table 36–2.

/D/
: The set of 256 code-groups corresponding to valid data, as specified in 48.2.4.1 and listed in Table 36–1a–e.

||D||
: The column of four Data code-groups present during packet reception.

/Dx.y/
: One of the set of 256 code-groups corresponding to valid data, as specified in 48.2.4.1 and listed in Table 36–1a–e.

/E/
: The /K30.7/ code-group corresponding to the Error function specified in 48.2.4.4.

||I||
: The column of four identical Idle code-groups corresponding to the Idle function specified in 48.2.4.2. Also used to represent the corresponding XGMII control characters.

||IDLE||
: Alias for ||I||.

/INVALID/
: The set of invalid data or special code-groups, as specified in 36.2.4.6.

/K/
: The /K28.5/ code-group used in the Idle Sync function specified in 48.2.4.2.1. Also used in the Terminate function specified in 48.2.4.3.2.

||K||
: The column of four identical Idle Sync code-groups corresponding to the Idle Sync function specified in 48.2.4.2.1. For EEE capability, one lane of ||K|| is replaced by /D20.5/ during the assertion of LPI as defined in 48.2.4.2.

/Kx.y/
: One of the set of 12 code-groups corresponding to valid special code-groups, as specified in Table 36–2.

LFAULT
: A vector of bits RXD<31:0> and RXC<3:0> containing a Local Fault sequence ordered set. The Local Fault sequence ordered set is defined in 46.3.4.

||Q||
: The column of four code-groups corresponding to the Sequence function specified in 48.2.4.5.1. Also used to represent the corresponding set of XGMII control and data characters.

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/R/

The /K28.0/ code-group used for the Idle Skip function specified in 48.2.4.2.3.

||R||

The column of four identical Idle Skip code-groups corresponding to the Idle Skip function specified in 48.2.4.2.3. For EEE capability, one lane of ||R|| is replaced by /D20.5/ during the assertion of LPI as defined in 48.2.4.2.

||S||

The column of code-groups including the Start code-group as specified in 48.2.4.3.1. Also used to represent the corresponding set of XGMII control and data characters.

||T||

The column of code-groups including the Terminate code-group as specified in 48.2.4.3.2. Also used to represent the corresponding XGMII control and data characters.

The following constants are used only for the EEE capability:

||LPIDLE||

The column consisting of three /K/ characters and one of /D20.5/, or three /R/ characters and one /D20.5/, or a column of ||A|| preceded by a column containing three /K/ characters and one /D20.5/ or three /R/ characters and one /D20.5/ as specified in 48.2.4.2.

48.2.6.1.3 Variables

align_column <39:0>

A vector of bits represented by the most recently received column of aligned 10-bit code-groups on all four lanes from the PCS Deskew process. For lane 0, the element align_column <0> corresponds to the least recently received (oldest) rx_bit of the code-group; align_column <9> corresponds to the most recently received (newest) rx_bit of the code-group. The same bit aging is applicable to the bits in align_column <39:10> with respect to rx_lane <3:1>. Code-group to lane assignment is specified in Table 48–1.

align_status

A parameter set by the PCS Deskew process to reflect the status of the lane-to-lane code-group alignment.

Values: FAIL; The deskew process is not complete.
OK; All lanes are synchronized and aligned.

NOTE—For EEE capability, this variable is affected by the LPI receive state diagram. Without EEE capability this variable is identical to deskew_align_status controlled by the deskew state diagram.

code_sel

A Boolean derived from a uniformly distributed random integer *r* generated by a PRBS based on a 7th order polynomial.

Values: 0; LSB of random number is zero.
1; LSB of random number is one.

deskew_error

A Boolean used by the PCS Deskew process to indicate that a lane-to-lane alignment error has been detected.

Values: FALSE; /A/ not recognized in any lane or recognized in all lanes simultaneously.
TRUE; /A/ recognized in fewer than all lanes.

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enable_cgalign

A Boolean that indicates the enabling and disabling of code-group comma alignment. The code-group boundary may be changed whenever code-group comma alignment is enabled. This process is known as code-group alignment.

Values: FALSE; Code-group alignment is disabled.
TRUE; Code-group alignment is enabled.

enable_deskew

A Boolean that indicates the enabling and disabling of the deskew process. Code-groups may be discarded whenever deskew is enabled. This process is known as code-group slipping.

Values: FALSE; Deskew is disabled.
TRUE; Deskew is enabled.

IDLE

A vector of bits RXD<31:0> and RXC<3:0> containing Idle. Idle is defined in Table 46–4.

lane_sync_status <3:0>

A parameter set by the PCS Synchronization process to reflect the status of the link for each lane as viewed by the receiver. lane_sync_status <n> represents lane_sync_status on lane n where n=0:3.

Values: FAIL; The receiver is not synchronized to the code-group boundary.
OK; The receiver is synchronized to the code-group boundary.

next_ifg

Controls the ||IDLE|| pattern immediately following the next frame. It is used to ensure an equal and deterministic presence of both ||A|| and ||K||

Values: A; The first ||IDLE|| following the end of the next frame will be ||A||.
K; The first ||IDLE|| following the end of the next frame will be ||K||.

reset

Condition that is true until such time as the power supply for the device that contains the PCS has reached the operating region. The condition is also true when the device has low-power mode set via Control register bit 4.0.11 or 5.0.11. The condition is also true when a reset request is detected via Control register bit 4.0.15 or 5.0.15.

Values: FALSE; The device is completely powered and has not been reset (default).
TRUE; The device has not been completely powered or has been reset.

NOTE—Reset evaluates to its default value in each state where it is not explicitly set.

RX

Alias for RXD <31:0> and RXC <3:0> representing the XGMII Receive Data and Control signals.

RXC <3:0>

Receive Control signals of the XGMII as specified in Clause 46. Set by the PCS Receive process.

RXD <31:0>

Receive Data signals of the XGMII as specified in Clause 46. Set by the PCS Receive process.

rx_lane <3:0>

A vector of bits representing the serial lanes used to convey data from the PMD to the PMA via the PMD_UNITDATA.indication service primitive as specified in Clause 53 or Clause 54.

Bit values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

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rx_unaligned <39:0>

A vector of bits represented by the most recently received column of unaligned 10-bit code-groups on all four lanes from the PMA. For lane 0, the element rx_unaligned <0> is the least recently received (oldest) rx_bit from the PMD; rx_unaligned <9> is the most recently received (newest) rx_bit from the PMD. The same bit aging is applicable to the bits in rx_unaligned <39:10> with respect to rx_lane <3:1>. Code-group to lane assignment is specified in Table 48–1.

signal_detect <3:0>

A parameter set continuously and directly from the PMD_SIGNAL.indication(signal_detect <3:0>) primitive to reflect the status of the incoming link signal for each lane. Used by the PCS Synchronization process to validate the data received on rx_unaligned <39:0>. Signal_detect <n> represents signal_detect on lane n where n=0:3.

Values: FAIL; A signal is not present on the lane.
OK; A signal is present on the lane.

sync_code-group <39:0>

A vector of bits represented by the most recently received column of unaligned 10-bit code-groups on all four lanes from the PCS Synchronization process. For lane 0, the element sync_code-group <0> corresponds to the least recently received (oldest) rx_bit; sync_code-group <9> corresponds to the most recently received (newest) rx_bit. The same bit aging is applicable to the bits in sync_code-group<39:10> with respect to rx_lane <3:1>. Code-group to lane assignment is specified in Table 48–1.

sync_status

A Boolean that represents the following behavior: For all n in lane_sync_status<n>.

Values: FAIL; At least one lane is not in sync.
OK; All lanes are in sync.

TQMSG

A vector of bits representing the last link status message received over the XGMII once the link status message is recognized. Used by the PCS Transmit process to load tx_code-group <39:0>.

tx_code-group <39:0>

A vector of bits representing a column of four aligned 10-bit code-groups which has been prepared for transmission by the PCS Transmit process. This vector is conveyed to the PMA as the parameter of a PMA_UNITDATA.request(tx_lane <3:0>) service primitive. For lane 0, the element tx_code-group <0> is the first tx_bit transmitted; tx_code-group <9> is the last tx_bit transmitted. The same bit aging is applicable to the bits in tx_code-group <39:10> with respect to tx_lane <3:1>. Code-group to lane assignment is specified in Table 48–1.

TX

Alias for either TXD <31:0> and TXC <3:0> representing the XGMII Transmit Data and Control signals, or the Local Fault ordered set as defined in 46.3.4 when a fault condition is detected on the transmit path.

TXC <3:0>

Transmit Control signals of the XGMII as specified in Clause 46. Interpreted by the PCS Transmit process.

TXD <31:0>

Transmit Data signals of the XGMII as specified in Clause 46. Interpreted by the PCS Transmit process.

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tx_lane <3:0>

A vector of bits representing the serial lanes used to convey data from the PMA to the PMD via the PMD_UNITDATA.request service primitive as specified in Clause 53 or Clause 54.

Bit values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

The following variables are used only for the EEE capability:

deskew_align_status

Variable used by the deskew state diagram to reflect the status of the lane-to-lane code-group alignment.

Values: FAIL; The deskew process is not complete.
OK; All lanes are synchronized and aligned.

rx_lpi_active

A Boolean variable that is set to TRUE when the receiver is in a low power state and set to FALSE when it is in an active state and is not restricted by the LPI receive state diagram.

rx_quiet

A Boolean variable set to TRUE while in the RX_QUIET state and set to FALSE otherwise. When this variable is TRUE it indicates that receive PCS and PMD may power-down nonessential functions.

tx_quiet

A Boolean variable set to TRUE when the transmitter is in the TX_QUIET state and set to FALSE otherwise. When set to TRUE, the PMD will disable the transmitter as described in 71.6.6. When this variable is TRUE it indicates that transmit PCS and PMD may power-down nonessential functions.

48.2.6.1.4 Functions

check_end

Prescient Terminate function used by the PCS Receive process to set the RXD<31:0> and RXC<3:0> signals to indicate Error if a running disparity error was propagated to any Idle code-groups in ||T||, or to the column following ||T||. The XGMII Error control character is returned in all lanes less than n in ||T||, where n identifies the specific Terminate ordered-set $||T_n||$, for which a running disparity error or any code-groups other than /A/ or /K/ are recognized in the column following ||T||. The XGMII Error control character is also returned in all lanes greater than n in the column prior to ||T||, where n identifies the specific Terminate ordered-set $||T_n||$, for which a running disparity error or any code group other than /K/ is recognized in the corresponding lane of ||T||. For all other lanes the value set previously is retained.

cvrx_terminate

Conversion function used by the PCS Receive process when Terminate is indicated to convert all /K/ code-groups to Idle control characters signaled via RX. Conversion is performed for all lanes.

cvtx_terminate

Conversion function used by the PCS Transmit process when Terminate is indicated to convert all Idle control characters signaled via TX to /K/ code-groups. Conversion is performed for all lanes.

DECODE ([||y||])

Consists of four independent synchronous processes, one each per lane. In the PCS Receive process, this function takes as its arguments the latched value of align_column ([||y||]) and the current running disparity, and returns XGMII RX as specified in 48.2.3 and 48.2.4. When decoding

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||T||, the returned XGMII RX value is further modified by the cvrx_terminate and check_end functions, the result of the check_end function takes priority over the result of the cvrx_terminate function. DECODE also updates the current running disparity per the running disparity rules outlined in 36.2.4.4.

ENCODE(TX)
: Consists of four independent synchronous processes, one each per lane. In the PCS Transmit process, this function takes as its argument the XGMII TX signals and the current running disparity for each lane, and returns four corresponding 10-bit code-groups as specified in 48.2.3 and 48.2.4. When encoding ||T||, the XGMII TX values are modified by the result of the cvtx_terminate function. ENCODE also updates the current running disparity per Tables 36-1 or 36–2.

Q_det
: Function to determine the need to transmit sequence ordered sets. If TX=||Q|| then Q_det is set to true and TQMSG is set to the result of ENCODE(TX). Q_det remains true until set to false by the PCS transmit source state diagram. In the event that this function and the state diagram both attempt to modify Q_det, the setting of Q_det by this function to true will take priority.

signal_detectCHANGE <3:0>
: In the PCS Synchronization process, this function monitors the signal_detect parameter on a per lane basis for a state change. The function is set upon state change detection, which is required to detect signal_detect changes which occur asynchronously to PUDI. signal_detectCHANGE <n> represents signal_detectCHANGE on lane n where n=0:3.

  Values: TRUE; The output of this function changes to true when the function detects a change in signal_detect and stays true until the false condition is satisfied.
  FALSE; The output of this function changes to false when the LOSS_OF_SYNC state of the PCS synchronization state diagram is entered.

48.2.6.1.5 Counters

A_CNT
: A 5-bit down counter used to control Align code-group spacing. Loaded with a value between 16 and 31, inclusive, by a uniformly distributed random integer *r* generated by a PRBS based on a 7th order polynomial as described in 48.2.4.2. A_CNT is decremented once per PUDR. The count remains at zero until ||A|| is transmitted, at which time a new value is loaded.

good_cgs
: A 2-bit consecutive valid code-groups received counter.

The following counter is used only for the EEE capability:

wake_error_counter
: A counter that is incremented each time that the LPI receive state diagram enters the RX_WTF state indicating that a wake time fault has been detected. The counter is reflected in register 3.22 (see 45.2.3.12)

48.2.6.1.6 Timers

The following timers are used only for the EEE capability.

rx_tq_timer
: This timer is started when the PCS receiver enters the RX_SLEEP state. The timer terminal count is set to T_{QR}. When the timer reaches terminal count it will set the rx_tq_timer_done = TRUE.

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rx_tw_timer
: This timer is started when the PCS receiver enters the RX_WAKE state. The timer terminal count shall be set to a value no larger than the maximum value given for T_{WR} in Table 48–10. When the timer reaches terminal count it will set the rx_tw_timer_done = TRUE.

rx_wf_timer
: This timer is started when the PCS receiver enters the RX_WTF state, indicating that the receiver has encountered a wake time fault. The rx_wf_timer allows the receiver an additional period in which to synchronize or return to the QUIET state before a link failure is indicated. The timer terminal count is set to T_{WTF}. When the timer reaches terminal count it will set the rx_wf_timer_done = TRUE.

tx_ts_timer
: This timer is started when the PCS transmitter enters the TX_SLEEP state. The timer terminal count is set to T_{SL}. When the timer reaches terminal count it will set the tx_ts_timer_done = TRUE.

tx_tq_timer
: This timer is started when the PCS transmitter enters the TX_QUIET state. The timer terminal count is set to T_{QL}. When the timer reaches terminal count it will set the tx_tq_timer_done = TRUE.

tx_tr_timer
: This timer is started when the PCS transmitter enters the TX_REFRESH state. The timer terminal count is set to T_{UL}. When the timer reaches terminal count it will set the tx_tr_timer_done = TRUE.

48.2.6.1.7 Messages

AUDI([||y||])
: Alias for ALIGN_UNITDATA.indicate(parameters).

ALIGN_UNITDATA.indicate([align_column <39:0>])
: A signal sent by the PCS Deskew process to the PCS Receive process conveying the latched value of the indicated column of code-groups over each lane ([||y||]) (see 48.2.6.2.3).

PMA_UNITDATA.indication(rx_unaligned <39:0>)
: A signal sent by the PMA Receive process to the PCS Synchronization process conveying the next code-group set received over each lane of the medium (see 48.3.2.2).

PMA_UNITDATA.request(tx_code-group <39:0>)
: A signal sent by the PCS Transmit process conveying the next code-group set for all lanes ready for transmission over the medium (see 48.3.2.1).

PMD_SIGNAL.indication(signal_detect <3:0>)
: Indicates the status of the incoming link signal. A signal mapped to the PMD_SIGNAL.indication(SIGNAL_DETECT) service primitive specified in Clause 53 or Clause 54. signal_detect <n> is set to the same value for all lanes n where n=0:3.

  Values: FAIL; A signal is not present on the lane.
  OK; A signal is present on the lane.

PUDI
: Alias for PMA_UNITDATA.indication(parameters).

PUDR
: Alias for PMA_UNITDATA.request(parameters).

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SUDI
: Alias for SYNC_UNITDATA.indicate(parameters).

SYNC_UNITDATA.indicate(sync_code-group <39:0>)
: A signal sent by the PCS Synchronization process to the PCS Deskew process conveying code-groups over each lane (see 48.2.6.2.2).

The following messages are used only for the EEE capability:

PMD_RXQUIET.request(rx_quiet)
: A signal sent by the PCS LPI receive state diagram to the PMD. When TRUE this indicates that the receiver is in a quiet state and is not expecting incoming data.

PMD_TXQUIET.request(tx_quiet)
: A signal sent by the PCS LPI transmit state diagram to the PMD. When TRUE this indicates that the transmitter is in a quiet state and may cease to transmit a signal on the medium.

48.2.6.2 State diagrams

48.2.6.2.1 Transmit

The PCS shall implement its Transmit process as depicted in Figure 48–7, including compliance with the associated state variables as specified in 48.2.6.1. This state diagram makes exactly one transition for each transmitted ordered set that is processed.

The Transmit Source process determines whether XGMII data and control information should be passed through to the PMA for serialization or converted before passing to the PMA. In all cases, XGMII data and control information is encoded before it is passed to the PMA. Data and control information may be sourced either directly from the XGMII or generated by the PCS depending on whether packet or Idle is being sourced by the XGMII. The recognition of the XGMII Start, Terminate, Idle and Sequence control characters is used to determine whether packet, Idle, or link status is being sourced by the XGMII.

The detection of a link status condition including the receipt of link status messages over the XGMII causes the PCS Transmit process to generate link status messages interspersed in an Idle sequence.

The PCS Transmit process continuously sources tx_code-group<39:0> to the PMA. The Transmit process determines the proper code-group to source on each lane based on running disparity requirements.

48.2.6.2.2 Synchronization

The PCS shall implement four Synchronization processes as depicted in Figure 48–8 including compliance with the associated state variables as specified in 48.2.6.1. The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PMA client to suspend normal actions. A Synchronization process operates independently on each lane, and synchronization is complete only when synchronization is acquired on all lanes. The synchronization process described in the following paragraphs applies to each lane.

The PCS Synchronization process continuously accepts code-groups via the PMA_UNITDATA.indication primitive and conveys received code-groups to the PCS Deskew process via the SYNC_UNITDATA.indicate message.

When in the LOSS_OF_SYNC state, the PCS may attempt to realign its current code-group boundary to one which coincides with the code-group boundary defined by a comma (see 36.2.4.9). This process is referred to in this document as code-group alignment.

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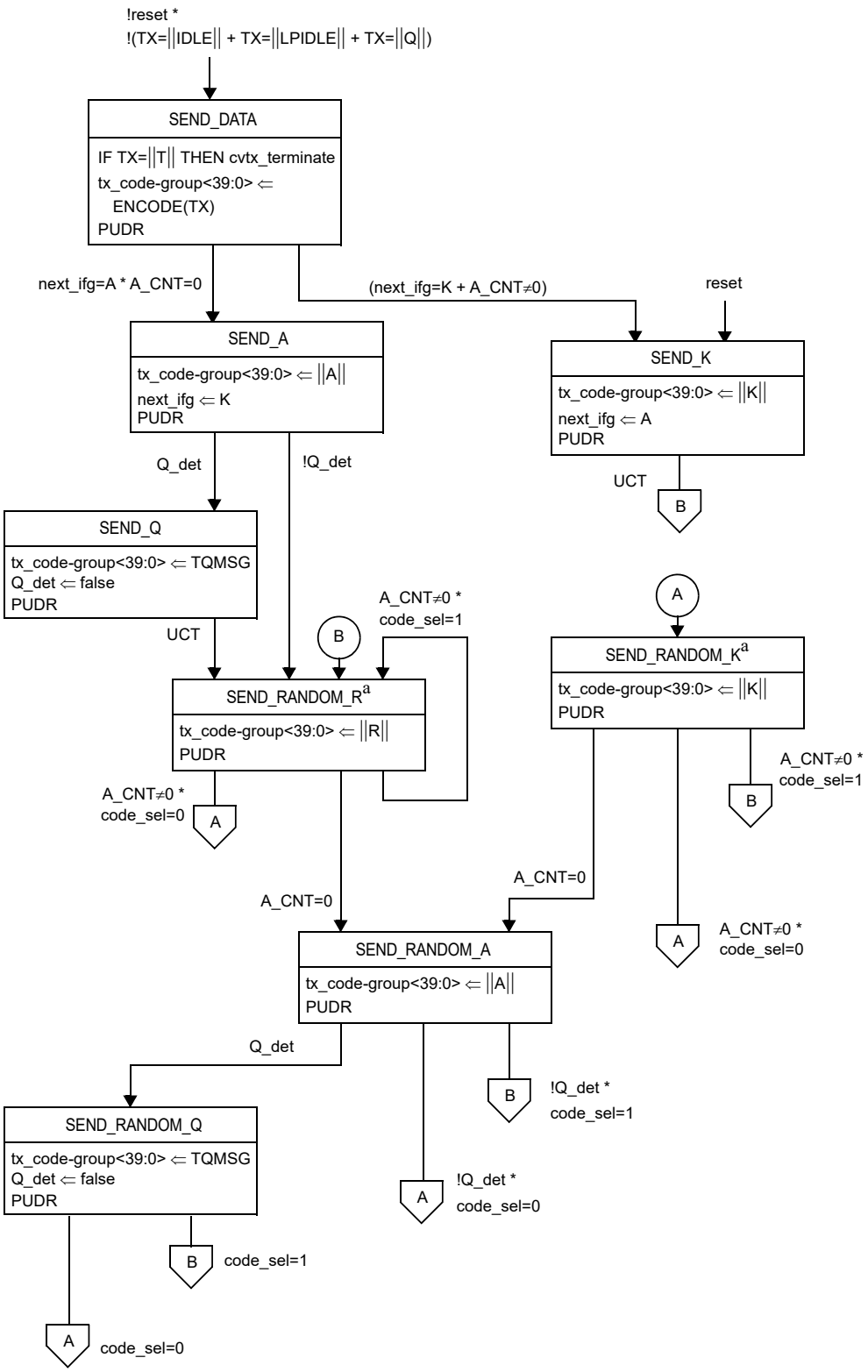

[a] If TX=||LPIDLE|| one lane is replaced by /D20.5/ as defined in 48.2.4.2.

NOTE—The state diagram makes exactly one transition for each transmit code-group processed.

Figure 48–7—PCS transmit source state diagram

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Once synchronization is acquired, the Synchronization process tests received code-groups in sets of four code-groups and employs multiple sub-states, effecting hysteresis, to move between the SYNC_ACQUIRED_1 and LOSS_OF_SYNC states. The Synchronization process sets the lane_sync_status <3:0> flags to indicate whether the PMA is functioning dependably (as well as can be determined without exhaustive error-ratio analysis). Whenever any PMA lane is not operating dependably, as indicated by the setting of lane_sync_status <3:0>, the deskew_align_status flag is set to FAIL.

48.2.6.2.3 Deskew

The PCS shall implement the Deskew process as depicted in Figure 48–9 including compliance with the associated state variables as specified in 48.2.6.1. The Deskew process is responsible for determining whether the underlying receive channel is capable of presenting coherent data to the XGMII. The Deskew process asserts the deskew_align_status flag to indicate that the PCS has successfully deskewed and aligned code-groups on all lanes. The Deskew process attempts deskew and alignment whenever the deskew_align_status flag is de-asserted. The Deskew process is otherwise idle. For the EEE capability the relationship between align_status and deskew_align_status is given by Figure 48–12, otherwise align_status is identical to deskew_align_status. Whenever the align_status flag is set to FAIL the condition is indicated as a link_status=FAIL condition in the status register bit 4.1.2 or 5.1.2.

Once alignment is acquired, the Deskew process tests received columns and employs multiple sub-states, effecting hysteresis, to move between the ALIGN_ACQUIRED_1 and LOSS_OF_ALIGNMENT states. These states monitor the link for continued alignment, tolerate alignment inconsistencies due to a reasonably low BER, and restart the Deskew process if alignment can not be reliably maintained.

48.2.6.2.4 Receive

The PCS shall implement its Receive process as depicted in Figure 48–10, including compliance with the associated state variables as specified in 48.2.6.1 and including the optional EEE capability.

The PCS Receive process continuously performs the DECODE function on the received code-groups from the PCS Deskew Process via the ALIGNED_UNITDATA.indicate message. The PCS Receive process generates the receive clock signal of the XGMII (RX_CLK) as specified in Clause 46. State transitions in the PCS Receive state diagram that generate the data and control characters (RXD<31:0> and RXC<3:0>) on the XGMII occur synchronous to RX_CLK. The Receive process operates in the following two modes:

a) Data mode during packet reception including Start and Terminate. Additionally, Data mode is active whenever !||I|| columns are received during the Idle sequence or !||I|| or !||Q|| columns are received during the Fault sequence signifying either an error or unusual or unsupported indication. Valid code-groups received while in Data mode are mapped to corresponding XGMII data or control characters regardless of whether or not the control characters are valid XGMII control characters. Invalid or Error code-groups are mapped directly to XGMII Error control characters. All code-groups are mapped on a lane by lane basis.
b) Idle mode during idle reception excluding Start and Terminate. Idle mode is active whenever ||I|| is received during idle reception. ||I|| is translated to XGMII Idle control characters.

48.2.6.2.5 LPI state diagrams

A PCS that supports the EEE capability shall implement the LPI transmit and receive processes as shown in Figure 48–11 and Figure 48–12. The transmit LPI state diagram controls tx_quiet, which disables the transmitter when TRUE. The receive LPI state diagram controls align_status during LPI and synchronizes the receive state diagram with the end of the LPI.

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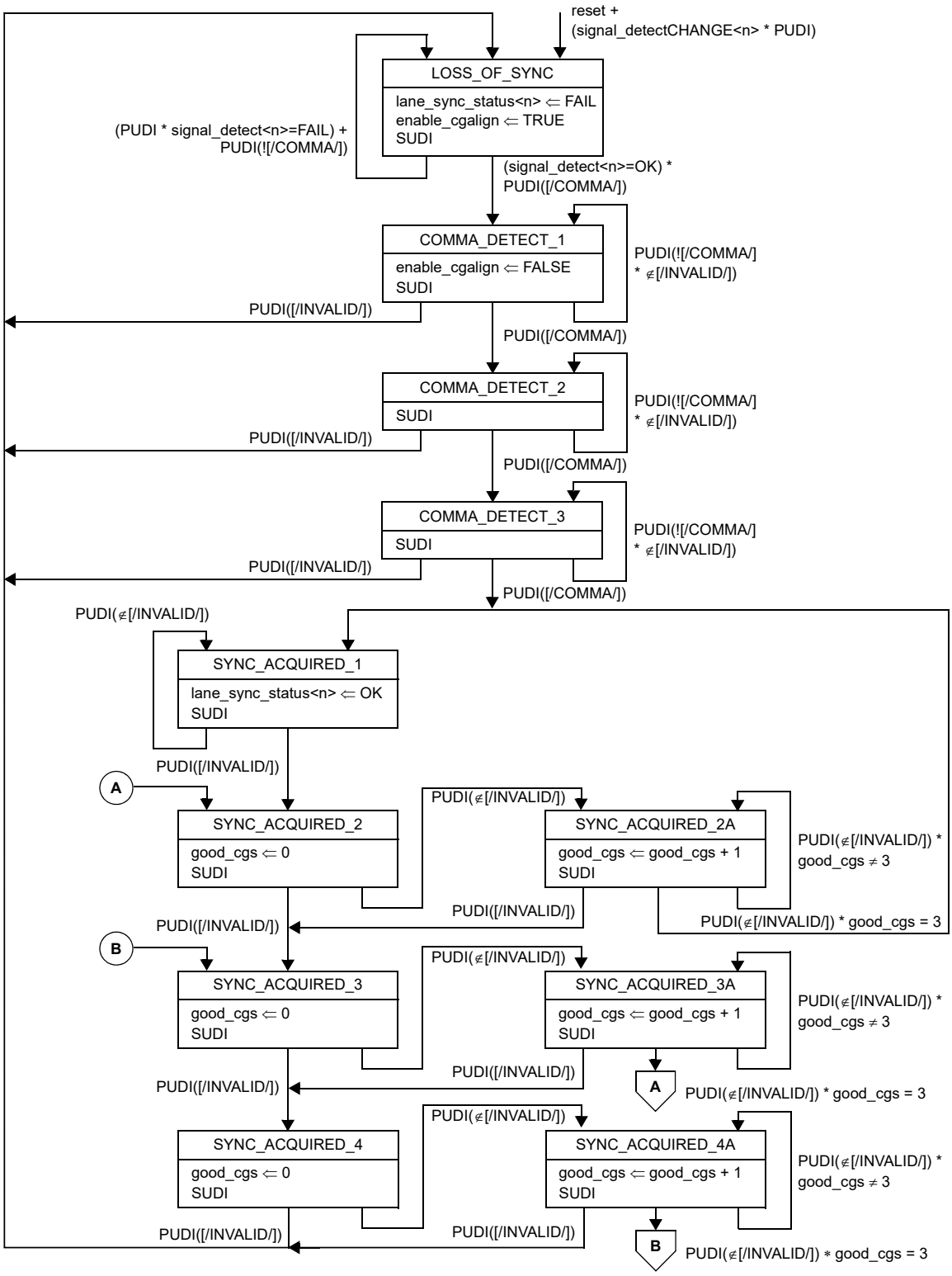

NOTE— lane_sync_status<n>, signal_detect<n> and signal_detectCHANGE<n>, refer to the number of the received lane n where n=0:3

Figure 48–8—PCS synchronization state diagram

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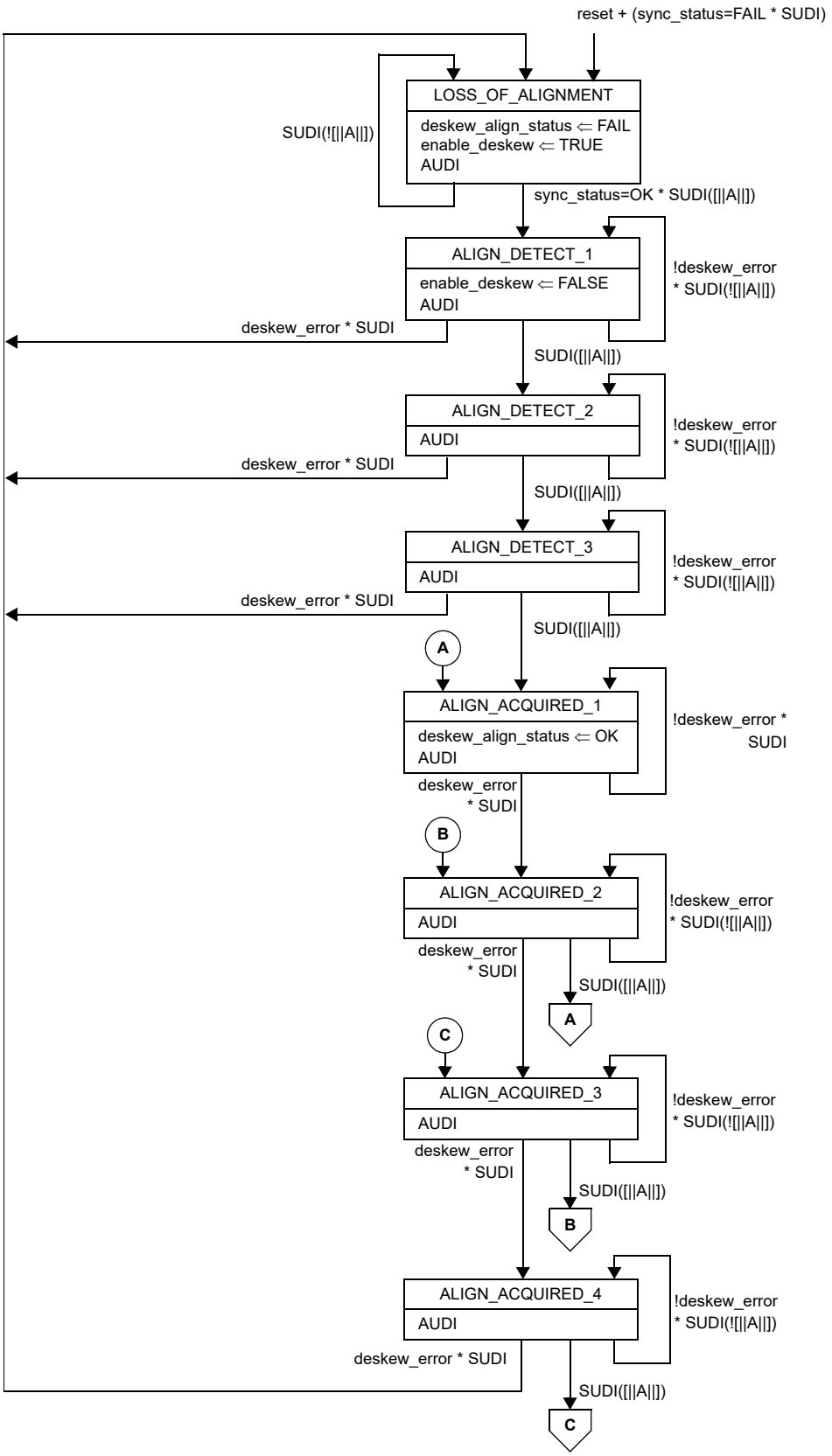

Figure 48–9—PCS deskew state diagram

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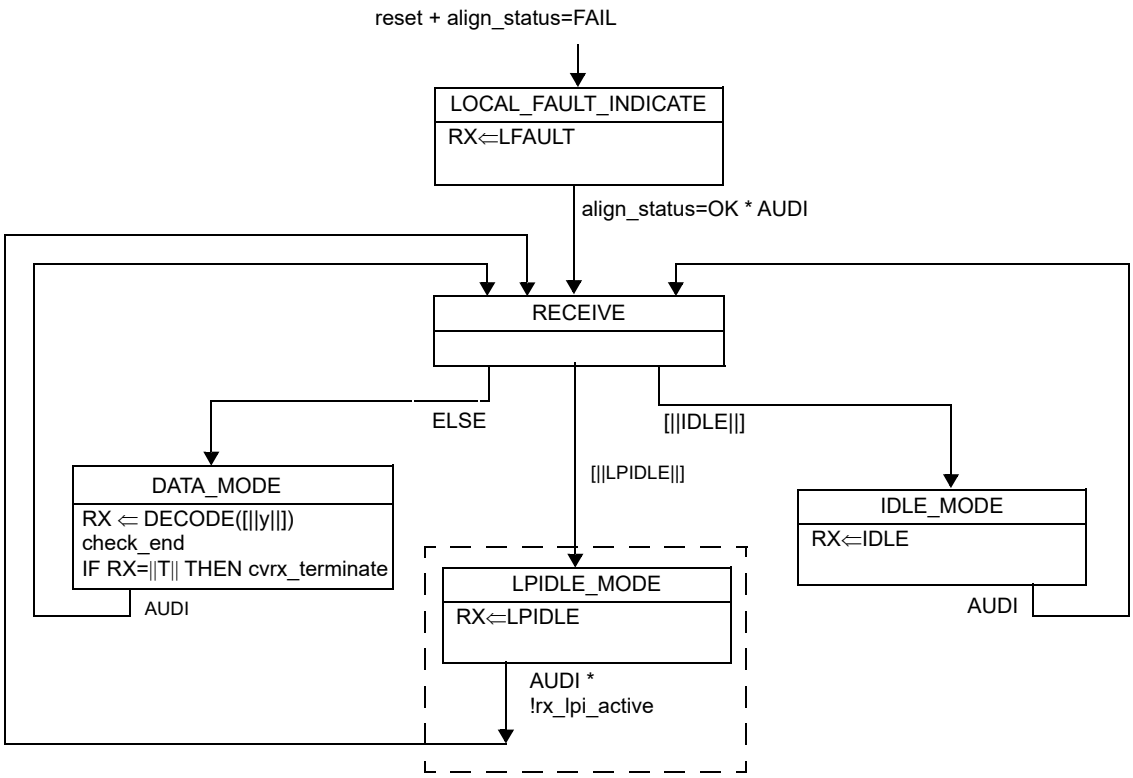

NOTE—Optional state to support LPI is shown inside the dotted box. The transition to the optional state is only possible with EEE capability.

Figure 48–10—PCS receive state diagram

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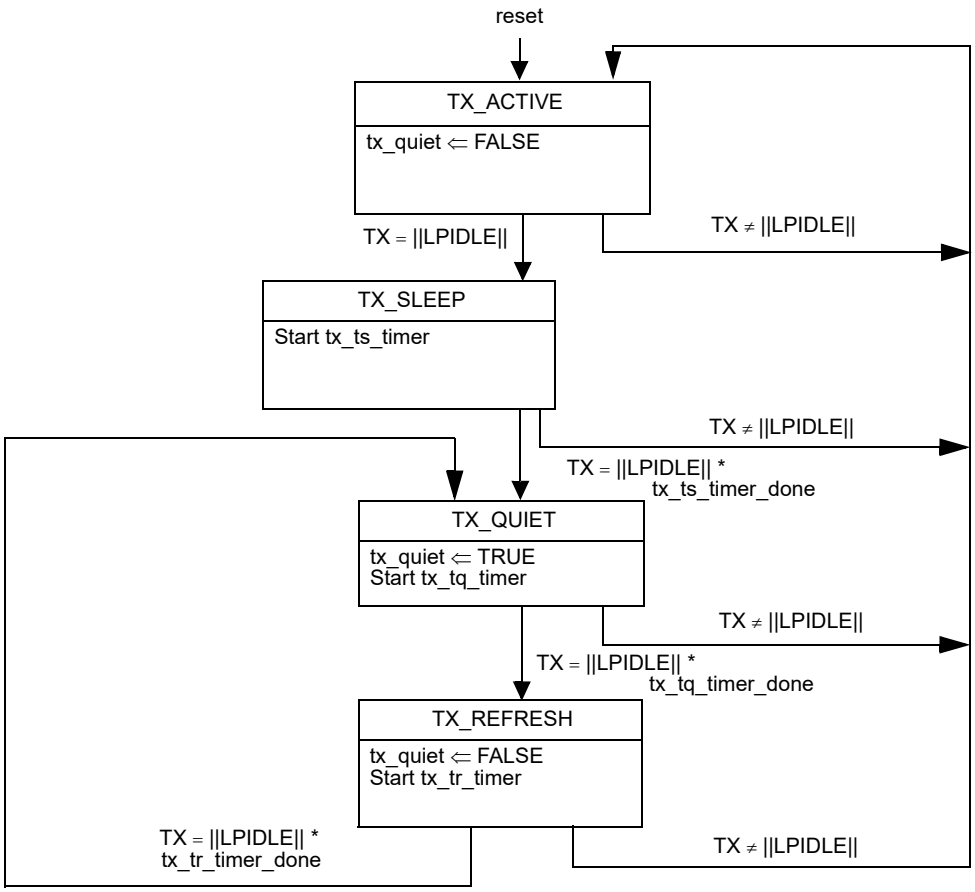

Figure 48–11—LPI Transmit state diagram

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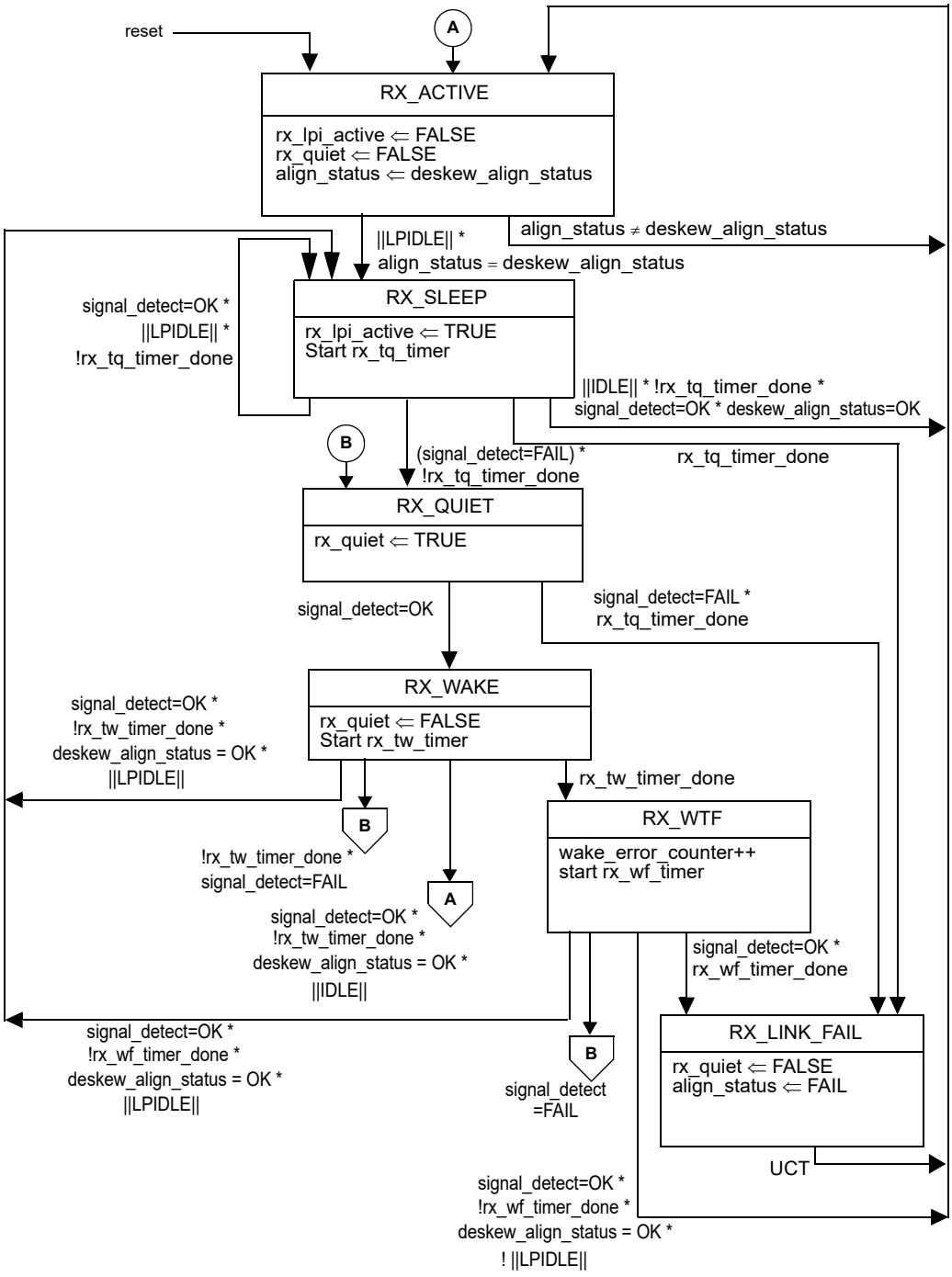

Figure 48–12—LPI Receive state diagram

The LPI functions shall use timer values for these state diagrams as shown in Table 48–9 for transmit and Table 48–10 for receive.

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Table 48–9—Transmitter LPI timing parameters

Parameter	Description	Min	Max	Units
T_{SL}	Local Sleep Time from entering the TX_SLEEP state to when tx_quiet is set to TRUE	19.9	20.1	μs
T_{QL}	Local Quiet Time from when tx_quiet is set to TRUE to entry into the TX_REFRESH state	2.5	2.6	ms
T_{UL}	Local Refresh Time from entry into the TX_REFRESH state to entry into the TX_QUIET state	19.9	20.1	μs

Table 48–10—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for signal detect to be set to OK while in the RX_SLEEP and RX_QUIET states before asserting rx_fault	3	4	ms
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault	—	9	μs
T_{WTF}	Wake time fault recovery time	—	1	ms

48.2.6.2.6 LPI status and management

For EEE capability, the PCS indicates to the management system that LPI is currently active in the receive and transmit directions using the status variable shown in Table 48–11.

Table 48–11—MDIO status indications

MDIO status variable	Register name	Register address	Note
Tx LPI received	PCS status register 1	3.1.11	Latched version of 3.1.9
Rx LPI received	PCS status register 1	3.1.10	Latched version of 3.1.8
Tx LPI indication	PCS status register 1	3.1.9	TRUE when not in state TX_ACTIVE
Rx LPI indication	PCS status register 1	3.1.8	TRUE when not in state RX_ACTIVE
Tx LPI received	PHY XS status register 1	4.1.11	Latched version of 4.1.9
Rx LPI received	PHY XS status register 1	4.1.10	Latched version of 4.1.8
Tx LPI indication	PHY XS status register 1	4.1.9	TRUE when not in state TX_ACTIVE
Rx LPI indication	PHY XS status register 1	4.1.8	TRUE when not in state RX_ACTIVE
Tx LPI received	DTE XS status register 1	5.1.11	Latched version of 5.1.9
Rx LPI received	DTE XS status register 1	5.1.10	Latched version of 5.1.8
Tx LPI indication	DTE XS status register 1	5.1.9	TRUE when not in state TX_ACTIVE
Rx LPI indication	DTE XS status register 1	5.1.8	TRUE when not in state RX_ACTIVE

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48.2.6.3 Initialization process

Link initialization involves the completion of the PCS Synchronization and Deskew processes and the ability to transmit and receive code-groups via the PCS Transmit and Receive processes, respectively. The status register link_status flag is set to OK whenever the align_status flag is set to OK and no errors preventing link operation are present in the PCS or PMA.

48.2.6.4 Link status reporting

Link status reporting involves detection of link status conditions and the signaling of link fault status. The purpose of link status reporting is to quickly identify and convey link status conditions to the RS which can take the necessary action to activate (deactivate) the link via the setting of the RS link_fault 2-bit variable. Link status reporting and MAC packet transmission is mutually exclusive.

48.2.6.4.1 Link status detection

10GBASE-X link status conditions include signal and deskew status conditions. Link status conditions include Local Fault and Remote Fault signals. A receive fault is recognized by the PCS Receive process whenever align_status=FAIL. Other fault conditions are not detected by the PCS or PMA and are detected only by the RS. A fault condition may also be recognized by any 10GBASE-X process upon detection of an error condition, which prevents continued reliable operation, but this is beyond the scope of this standard.

48.2.6.4.2 Link status signaling

Link status signaling follows the detection or recognition of a link status condition and involves the generation of Sequence ordered-sets (||Q||) by the PCS Transmit process. Link status signaling involves the transmission of ||Q|| following ||A|| transmission in the Idle sequence as specified in 48.2.4.2.

48.2.6.4.3 Link status messages

A 10GBASE-X link status message is a Sequence ordered-set. Ordered-sets associated with link status messages are specified in Table 48–4. Link status messages detected by the PCS Receive process are forwarded to the XGMII.

48.2.7 Auto-Negotiation for Backplane Ethernet

The following requirements apply to a PCS used with a 10GBASE-KX4 PMD. Support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when align_status=FAIL and the value OK when align_status=OK. The primitive shall be generated when the value of link_status changes.

48.3 Physical Medium Attachment (PMA) sublayer

The PMA is specified in the form of a service interface to the PCS. These services are described in an abstract manner and do not imply any particular implementation. The PMA service interface supports the exchange of code-group information between PCS entities. The PMA converts code-groups into bits and passes these to the PMD, and vice versa.

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48.3.1 Functions within the PMA

The PMA comprises the PMA Transmit process and PMA Receive process. Figure 48–5 depicts the mapping of the 36-bit-wide data and control path of the XGMII to the forty-bit-wide code-groups of the PMA service interface, and on to the four lane serial PMD service interface.

NOTE—Strict adherence to manufacturer-supplied guidelines for the operation and use of PMA serializer components is required to meet the jitter specifications of Clause 47, Clause 53, and Clause 54. The supplied guidelines should address the quality of power supply filtering associated with the transmit clock generator, and also the purity of the reference clock fed to the transmit clock generator.

48.3.1.1 PMA transmit process

The PMA Transmit process passes data unaltered (except for serializing) from the PCS directly to the PMD. Upon receipt of the PMA_UNITDATA.request primitive, the PMA shall individually serialize the four aligned 10-bit code-groups, one from each of four lanes, and transmit them to the PMD in the form of forty PMD_UNITDATA.request primitives, 10 each on four lanes.

Within each lane for each 10-bit code-group, the lowest numbered bit of the PMA_UNITDATA.indication parameter corresponds to the first bit transmitted to the PMD and the highest numbered bit of the PMA_UNITDATA.indication parameter corresponds to the last bit transmitted to the PMD. There is no numerical significance ascribed to the bits within a PMA code-group; that is, the code-group is simply a bit pattern that has some predefined interpretation. PMA to PMD bit and lane association is illustrated in Table 48–1. PMA to PMD bit ordering is illustrated in Figure 48–5.

PMA_UNITDATA.request primitives shall be generated with a frequency of 312.5 MHz ± 100 ppm. An internal clock multiplier unit multiplies the frequency of the 10-bit code-group based PMA_UNITDATA.request primitives by a factor of 10 to serialize the latched data out of the PMA and into the PMD.

48.3.1.2 PMA receive process

The PMA Receive process passes data unaltered (except for deserializing) from the PMD directly to the PCS. Upon receipt of forty PMD_UNITDATA.indication primitives, 10 in succession from each of four lanes, the PMA shall assemble the bits received into a 40-bit vector representing four 10-bit unaligned code-groups and pass that vector to the PCS as the parameter of four PMA_UNITDATA.indication primitives.

Within each lane for each 10-bit code-group, the lowest numbered bit of the PMA_UNITDATA.indication parameter corresponds to the first bit received from the PMD and the highest numbered bit of the PMA_UNITDATA.indication parameter corresponds to the last bit received from the PMD. There is no numerical significance ascribed to the bits within a PMA code-group; that is, the code-group is simply a bit pattern that has some predefined interpretation. Receive code-group alignment is performed by the PCS and is not applicable to PMA. PMA to PMD bit and lane association is illustrated in Table 48–1. PMA to PMD bit ordering is illustrated in Figure 48–5.

PMA_UNITDATA.indication primitives shall be generated with a frequency of 312.5 MHz ± 100 ppm. The line rate of each of four PMD lanes is 3.125 GBd ± 100 ppm. The serial data stream of the PMD includes an embedded clock that nominally operates at a frequency 10 times higher than that of a single lane code-group stream. The PMA Receive process shall recover a clock from a valid 8B/10B received data stream if the stream is within tolerance.

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48.3.2 Service interface

The following primitives are defined:

PMA_UNITDATA.request(tx_code-group <39:0>)
PMA_UNITDATA.indication(rx_unaligned <39:0>)

48.3.2.1 PMA_UNITDATA.request

This primitive defines the transfer of data in the form of aligned code-groups from the PCS to the PMA. PMA_UNITDATA.request is generated by the PCS Transmit process.

48.3.2.1.1 Semantics of the service primitive

PMA_UNITDATA.request(tx_code-group <39:0>)

The data conveyed by PMA_UNITDATA.request is the tx_code-group <39:0> parameter defined in 48.2.6.1.3.

48.3.2.1.2 When generated

The PCS continuously sends tx_code-group <39:0> to the PMA at a nominal rate of 312.5 MHz ± 100 ppm, as governed by frequency and tolerance of XGMII TX_CLK.

48.3.2.1.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a series of forty PMD_UNITDATA.request primitives, 10 for each of the four PMD lanes, tx_lane <3:0>, requesting the four lane serial transmission of tx_code-group <39:0> to the PMD.

48.3.2.2 PMA_UNITDATA.indication

This primitive defines the transfer of data in the form of code-groups from the PMA to the PCS. PMA_UNITDATA.indication is used by the PCS Synchronization process.

48.3.2.2.1 Semantics of the service primitive

PMA_UNITDATA.indication(rx_unaligned <39:0>)

The data conveyed by PMA_UNITDATA.indication is the rx_unaligned <39:0> parameter defined in 48.2.6.1.3.

48.3.2.2.2 When generated

The PMA continuously sends rx_unaligned <39:0> to the PCS at a nominal rate of 312.5 MHz ± 100 ppm, as governed by frequency and tolerance of PMD_UNITDATA.indication.

48.3.2.2.3 Effect of receipt

Upon receipt of this primitive, the PCS Synchronization process attempts to achieve code-group synchronization on each lane (see 48.2.6.2.2).

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48.3.3 Loopback mode

Loopback mode shall be provided for the 10GBASE-X PMA and DTE XGXS, and optionally for the PHY XGXS, as specified in this subclause, by the transmitter and receiver of a device as a test function to the device. When Loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. A device is explicitly placed in Loopback mode (i.e., Loopback mode is not the normal mode of operation of a device). Loopback applies to all lanes as a group (i.e., the lane 0 transmitter is directly connected to the lane 0 receiver, the lane 1 transmitter is directly connected to the lane 1 receiver, etc.). The method of implementing Loopback mode is not defined by this standard.

Control of the Loopback function may be supported through the MDIO management interface of Clause 45 or equivalent.

NOTE—The signal path that is exercised in the Loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this Loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

48.3.3.1 Receiver considerations

Entry into or exit from Loopback mode may result in a temporary loss of synchronization.

48.3.3.2 Transmitter considerations

While in Loopback mode, the transmitter output is not defined.

48.3.4 Test functions

A limited set of test functions may be provided as an implementation option for testing of the transmitter function or for testing of an attached receiver.

Some test functions that are not defined by this standard may be provided by certain implementations. Compliance with the standard is not affected by the provision or exclusion of such functions by an implementation. Random jitter test patterns for 10GBASE-X are specified in Annex 48A. Test-pattern capability and selection is optional and supported via MDIO register bits defined in Clause 45. Jitter Test methodology for 10GBASE-X is specified in Annex 48B. It is recommended that the capability for generating the mixed-frequency, low frequency and high frequency patterns is implemented in the PCS.

A typical test function is the ability to transmit invalid code-groups within an otherwise valid PHY bit stream. Certain invalid PHY bit streams may cause a receiver to lose word and/or bit synchronization. See ANSI/INCITS 450 (FC-PI-4), subclause 5.4 for a more detailed discussion of receiver and transmitter behavior under various test conditions.

48.4 Compatibility considerations

There is no requirement for a compliant device to implement or expose any of the interfaces specified for the PCS or PMA. Implementations of an XGMII shall comply with the requirements as specified in Clause 46.

48.5 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control

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sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of transmit and receive delay contributed by the 10GBASE-X PCS shall be no more than 2048 BT.

The reference point for all MDI measurements is the 50% point of the mid-cell transition corresponding to the reference bit, as measured at the MDI.

48.6 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801:1995.

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48.7 Protocol implementation conformance statement (PICS) proforma for Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X[91]

48.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 48, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

48.7.2 Identification

48.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

48.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 48, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[91] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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48.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
MD	MDIO	45, 48.1.3.1	Registers and interface supported	O	Yes [ ] No [ ]
XGXS	Support of XAUI/XGXS	47, 48.1.5		O	Yes [ ] No [ ]
XGE	XGMII compatibility interface	46, 48.1.3.1	Compatibility interface is supported	O	Yes [ ] No [ ]
LX4	Support of 10GBASE-LX4 PMD	53, 48.1.3.3		O	Yes [ ] No [ ]
CX4	Support of 10GBASE-CX4 PMD	54, 48.1.3.3		O	Yes [ ] No [ ]
LPI	Implementation of LPI	48.2.3		O	Yes [ ] No [ ]

48.7.4 PICS proforma tables for the PCS and PMA sublayer, type 10GBASE-X

48.7.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Jitter test patterns	48.3.4	As per Annex 48A	O	Yes [ ] No [ ]
CC2	Environmental specifications	48.6		M	Yes [ ]

48.7.4.2 PCS functions

Item	Feature	Subclause	Value/Comment	Status	Support
CG	Code-group usage	48.2.3	PCS support of 8B/10B code-groups	M	Yes [ ]
IOS	||I|| sequencing rules	48.2.4.2	All rules apply	M	Yes [ ]
PRBS	Random integer generator	48.2.4.2	$X^7 + X^3 + 1$ or $X^7 + X^6 + 1$. Used for ||A|| spacing. Optional and ancillary use for testing	M	Yes [ ]
CMA	Comma detection	48.2.4.2.1	comma+ and comma- for /K/	M	Yes [ ]
CKCU	Clock rate compensation in unencoded idle stream	48.2.4.2.3	Meets the requirements of 48.2.4.2.3	O	Yes [ ] No [ ]
ERR	Error indication	48.2.4.4	Replacement of invalid code-groups with /E/	M	Yes [ ]
TSD	Transmit state diagrams	48.2.6.2.1	Meets the requirements of Figures 48–7	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
SSD	Synchronization state diagram	48.2.6.2.2	Meets the requirements of Figure 48–8	M	Yes [ ]
DSD	Deskew state diagrams	48.2.6.2.3	Meets the requirements of Figure 48–9	M	Yes [ ]
RSD	Receive state diagrams	48.2.6.2.4	Meets the requirements of Figure 48–10	M	Yes [ ]
AN1*	Support for use with a 10GBASE-KX4 PMD	48.2.7	AN technology dependent interface described in Clause 73	O	Yes [ ]
AN2	AN_LINK.indication primitive	48.2.7	Support of the primitive AN_LINK.indication(link_status), when the PCS is used with 10GBASE-KX4 PMD	AN1:M	Yes [ ]
AN3	link_status parameter	48.2.7	Takes the value OK or FAIL, as described in 48.2.7	AN1:M	Yes [ ]
AN4	Generation of AN_LINK.indication primitive	48.2.7	Generated when the value of link_status changes	AN1:M	Yes [ ]

48.7.4.3 PMA functions

Item	Feature	Subclause	Value/Comment	Status	Support
PMAT	Transmit function	48.3.1.1	PMA_UNITDATA.request	M	Yes [ ]
TXRT	Transmit rate	48.3.1.1	3.125 GBd ± 100 ppm	M	Yes [ ]
PMAR	Receive function	48.3.1.2	PMA_UNITDATA.indication	M	Yes [ ]
RXRT	Receive rate	48.3.1.2	3.125 GBd ± 100 ppm	M	Yes [ ]
CDR	Clock and data recovery	48.3.1.2	Required if line rate is within 3.125 GBd ± 100 ppm	M	Yes [ ]

48.7.4.4 Interface functions

Item	Feature	Subclause	Value/Comment	Status	Support
SKEW	Allowable lane skew	48.2.4.2.2	Table 48–5	M	Yes [ ]
LBXPMA	10GBASE-X PMA Loopback mode	48.3.3		M	Yes [ ]
LBDTE	DTE XGXS Loopback mode	48.3.3		M	Yes [ ]
LBPHY	PHY XGXS Loopback mode	48.3.3		O	Yes [ ]
DLY	Delay constraints	48.5	2048 BT	M	Yes [ ]

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48.7.4.5 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
LP-01	Receive state diagrams	48.2.6.2	Support additions to Figure 48–10 for LPI operation	LPI:M	Yes [ ] No [ ]
LP-02	LPI transmit state diagrams	48.2.6.2.5	Meet the requirements of Figure 48–11	LPI:M	Yes [ ] No [ ]
LP-03	LPI receive state diagrams	48.2.6.2.5	Meet the requirements of Figure 48–12	LPI:M	Yes [ ] No [ ]
LP-04	LPI transmit timing	48.2.6.2.5	Meet the requirements of Table 48–9	LPI:M	Yes [ ] No [ ]
LP-05	LPI receive timing	48.2.6.2.5	Meet the requirements of Table 48–10	LPI:M	Yes [ ] No [ ]

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49. Physical Coding Sublayer (PCS) for 64B/66B, type 10GBASE-R

49.1 Overview

49.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) that is used in the family of 10GBASE-R Physical Layer devices (PHYs): 10GBASE-SR, 10GBASE-LR, 10GBASE-ER, 10GBASE-LRM, and 10GBASE-KR. Alternatively, this PCS can connect to a WAN Interface Sublayer (WIS), which produces the 10GBASE-W encoding (10GBASE-R encoded data stream encapsulated into frames compatible with SONET and SDH networks) for transport by the 10GBASE-W Physical Layer devices: 10GBASE-SW, 10GBASE-LW, and 10GBASE-EW. The term 10GBASE-R is used when referring generally to Physical Layers using the PCS defined here.

The 10GBASE-R is based on a 64B/66B code. The 64B/66B code supports data and control characters, while maintaining robust error detection.

10GBASE-R PCS maps the interface characteristics of the WIS when present, and the PMA sublayer to the services expected by the Reconciliation and XGXS sublayers. 10GBASE-R can be extended to support any full duplex medium requiring only that the medium be compliant at the PMA level. 10GBASE-R PCS may be attached through the PMA sublayer to a LAN PMD sublayer supporting a data rate of 10 Gb/s or it may be attached to a WAN PMD through the WIS and PMA sublayers. When attached to a WAN sublayer, this PCS adapts the data stream to the WAN data rate.

49.1.2 Objectives

The following are the objectives of 10GBASE-R:

a) Support the full duplex Ethernet MAC.
b) Provide 10 Gb/s data rate at the XGMII.
c) Support LAN PMDs operating at 10 Gb/s and WAN PMDs operating at SONET STS-192c/SDH VC-4-64c rate.
d) Support cable plants using cabled optical fiber compliant with ISO/IEC 11801:1995 as specified in Clause 52 and Clause 68.
e) Allow for a nominal network extent of up to 40 km.
f) Support a BER objective of 10^{-12}.

49.1.3 Relationship of 10GBASE-R to other standards

Figure 49–1 depicts the relationships among the 10GBASE-R sublayers (shown shaded), the Ethernet MAC and reconciliation layers, and the higher layers.

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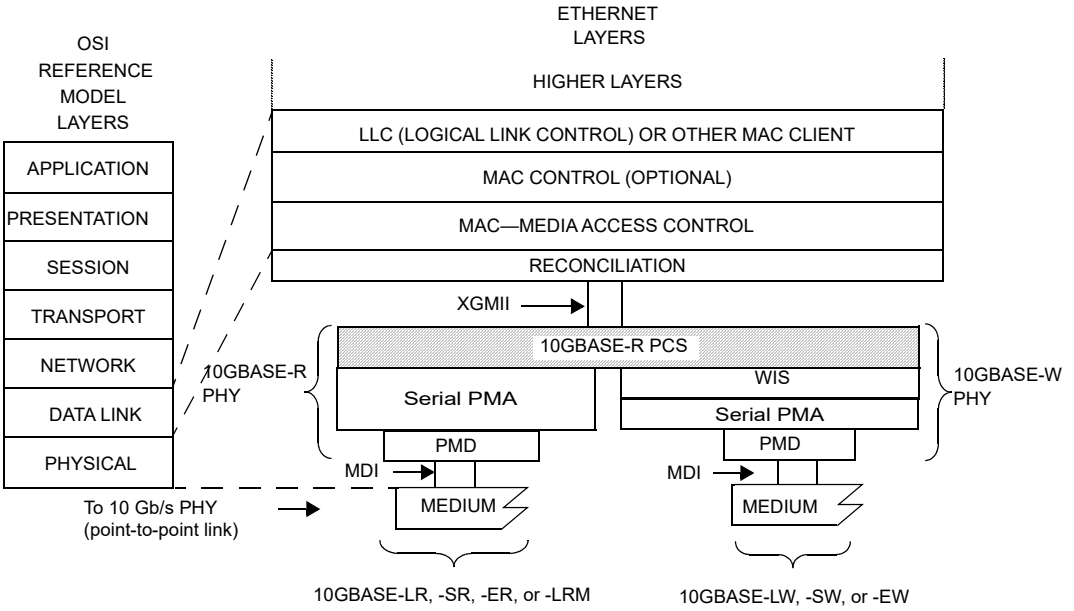
49.1.4 Summary of 10GBASE-R and 10GBASE-W sublayers

The following subclauses provide an overview of the 10GBASE-R and 10GBASE-W sublayers.[92] Figure 49–1 depicts the relationship between the 10GBASE-R PCS and its associated sublayers.



MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
WIS = WAN INTERFACE SUBLAYER
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE

NOTE—The PMD sublayers are mutually independent.

PMD TYPES:
Medium:
E = PMD FOR FIBER—1550 nm WAVELENGTH
L = PMD FOR FIBER—1310 nm WAVELENGTH
S = PMD FOR FIBER—850 nm WAVELENGTH
M = PMD WITH DISPERSION COMPENSATION FOR MULTI-MODE FIBER
Encoding:
R = 64B/66B ENCODED WITHOUT WIS
W = 64B/66B ENCODED WITH WIS

Figure 49–1—10GBASE-R PCS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

49.1.4.1 Physical Coding Sublayer (PCS)

The PCS service interface is the 10 Gigabit Media Independent Interface (XGMII), which is defined in Clause 46. The XGMII provides a uniform interface to the Reconciliation Sublayer for all 10 Gb/s PHY implementations (e.g., not only 10GBASE-R but also other types of 10 Gigabit PHY entities).

The 10GBASE-R PCS provides all services required by the XGMII, including the following:

a) Encoding (decoding) of eight XGMII data octets to (from) 66-bit blocks (64B/66B).
b) Transferring encoded data to (from) the PMA in 16 bit transfers.
c) When connected to a WAN PMD, deleting (inserting) idles to compensate for the rate difference between the MAC and PMD.

[92] The 10GBASE-R PHY consists of that portion of the Physical Layer between the MDI and XGMII consisting of the PCS, PMA, and PMD sublayers. The 10GBASE-R PHY is roughly analogous to the 100BASE-X PHY.

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d) Determining when a functional link has been established and informing the management entity via the MDIO when the PHY is ready for use.

49.1.4.2 WAN Interface Sublayer (WIS)

The WIS provides a medium-independent means for the PCS to operate over WAN links. It creates a 10GBASE-W encoding by encapsulating the encoded data steam from the 10GBASE-R PCS in frames compatible with SONET and SDH transmission formats. The WIS is specified in Clause 50.

49.1.4.3 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS to support the use of a range of physical media. The 10GBASE-R PMA performs the following functions:

a) Mapping of transmit and receive data streams between the PCS or WIS and PMA via the PMA service interface.
b) Serialization (deserialization) of bits for transmission (reception) on the underlying serial PMD.
c) Recovery of clock from the received data stream.
d) Mapping of transmit and receive bits between the PMA and PMD via the PMD service interface.
e) Optionally provides data loopback at the PMA service interface.

The PMA is specified in Clause 51.

49.1.4.4 Physical Medium Dependent (PMD) sublayer

The PMD and its media are specified in Clause 52 and Clause 68.

The MDI, logically subsumed within each PMD subclause, is the actual medium attachment for the various supported media.

49.1.4.5 Bit ordering across 10GBASE-R and 10GBASE-W sublayers.

The ordering of bits and octets for the case when no WIS is present between the PCS and PMA is shown in Figure 49–2. The diagram depicts the bit mappings for the data path at the service interfaces.

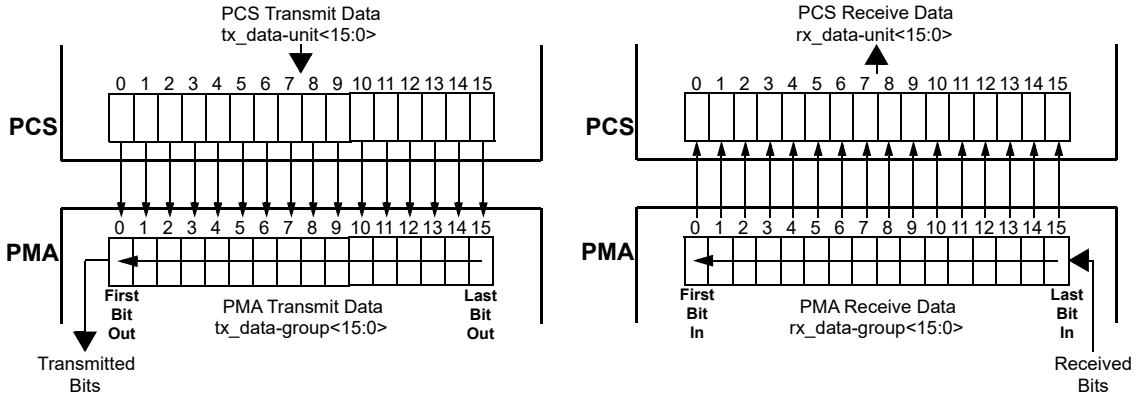

Figure 49–2—10GBASE-R PHY transmission order

The bit/octet ordering when a WIS is interposed between the PCS and PMA is shown in Figure 49–3. The details of WIS frame generation, as well as internal interfaces, have been omitted. Note that since SONET

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convention is to send the most significant bit (MSB) of each octet first and Ethernet convention is to send the least significant bit (LSB) of each octet first, the LSBs from the PCS octets are mapped into the MSBs of the WIS octets. It should be clear from the diagram that the Ethernet order of transmission (i.e., least-significant bit first), and hence the error detecting properties of the Ethernet CRC, are preserved in spite of the different bit ordering conventions followed by the WIS. Also, the SONET/SDH bit labeling conventions are different from the usual IEEE 802.3 bit labeling. The bits of a SONET/SDH octet are labeled from 1 to 8 with bit 1 being the MSB. Ethernet conventions label bits of an n-bit field from 0 to n–1 with bit 0 being the LSB. Figure 49–3 shows the results of these conventions. For example, tx_data-unit<0> through tx_data-unit<7> map to bits 1 through 8 respectively of a WIS octet.

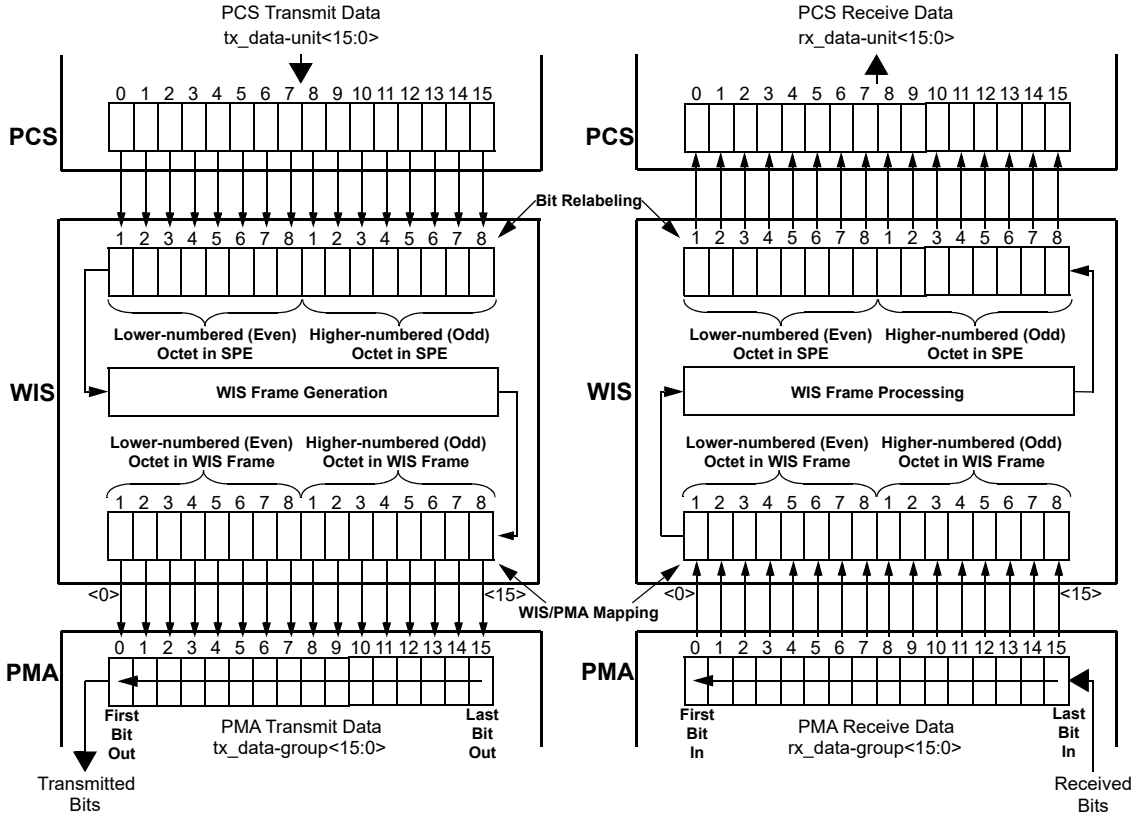

Figure 49–3—10GBASE-W PHY Transmission order

49.1.5 Inter-sublayer interfaces

There are a number of interfaces employed by 10GBASE-R. Some (such as the PMA service interface) use an abstract service model to define the operation of the interface. The PCS service interface is the XGMII that is defined in Clause 46. The XGMII has an optional physical instantiation. An optional physical instantiation of the PMA service interface has also been defined (see Clause 51). It is called XSBI (10 Gigabit Sixteen Bit Interface). Figure 49–4 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 10GBASE-R.

The upper interface of the PCS may connect to the Reconciliation Sublayer through the XGMII or the PCS may connect to an XGXS sublayer. The XGXS and the Reconciliation Sublayer provide the same service interface to the PCS. The lower interface of the PCS may connect to the WIS to support a WAN PMD or to the PMA sublayer to support a 10GBASE-R LAN PMD. The WIS and PMA interfaces are functionally

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equivalent except for data rate. When the PCS is connected directly to a LAN PMA, the nominal rate of the PMA service interface is 644.53125 Mtransfers/s, which provides capacity for the MAC data rate of 10 Gb/s. When the PCS is connected to a WAN PMA, the nominal rate of the WIS service interface is 599.04 Mtransfers/s and the MAC uses IFS stretch mode to ensure that there will be enough idle time that the PCS can delete idles to adjust to the lower rate. Since the data rates are different, WIS and PMA interface connections pose somewhat different constraints. The PCS shall support connection to either a WIS or to a PMA and may optionally support both.

If the optional Energy-Efficient Ethernet (EEE) capability is supported (see Clause 78, 78.3) then the interface with the PMA sublayer (or FEC sublayer) includes rx_mode and tx_mode to control power states in lower sublayers and energy_detect that indicates whether the PMD sublayer has detected a signal at the receiver. If the PHY includes an FEC sublayer, the interface includes rx_lpi_active to indicate that the LPI receive state diagram is not in RX_ACTIVE state.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

49.1.6 Functional block diagram

Figure 49–4 provides a functional block diagram of the 10GBASE-R PHY.

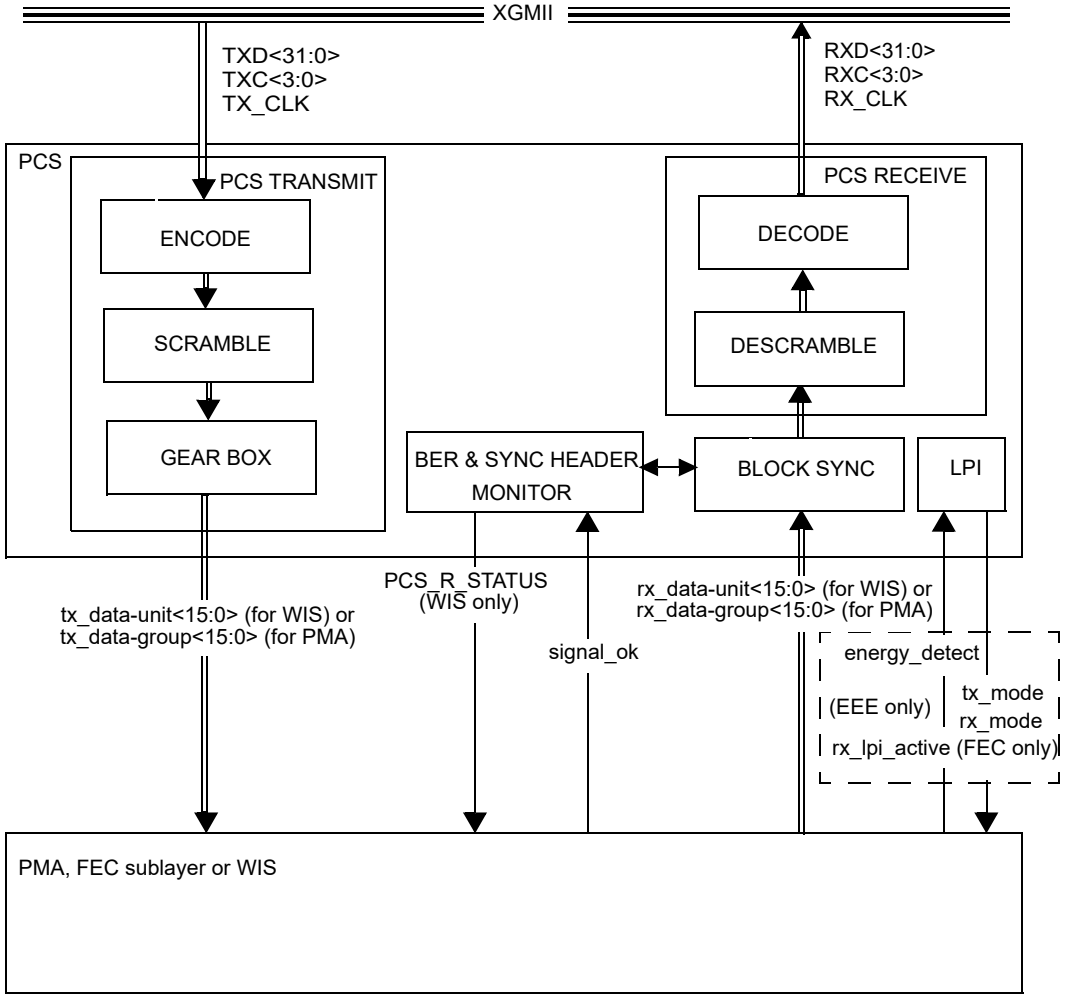

Figure 49–4—Functional block diagram

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49.2 Physical Coding Sublayer (PCS)

49.2.1 PCS service interface (XGMII)

The PCS service interface allows the 10GBASE-R PCS to transfer information to and from a PCS client. A PCS client is generally the Reconciliation Sublayer or an XGXS sublayer. The PCS Interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

49.2.2 Functions within the PCS

The PCS comprises the PCS Transmit, Block Synchronization, PCS Receive, and BER monitor processes for 10GBASE-R. The PCS shields the Reconciliation Sublayer (and MAC) from the specific nature of the underlying channel. The PCS transmit channel and receive channel can each operate in normal mode or, when not attached to a WIS, test-pattern mode. When the PCS is attached to a WIS, the WIS provides the test-pattern functionality.

When communicating with the XGMII, the PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals (TXCn = 1) and receive control signals (RXCn = 1). When communicating with the PMA, WIS, or FEC, the PCS uses a 16-bit wide, synchronous data path that conveys 16 encoded bits. Alignment to 64B/66B block is performed in the PCS. The WIS, PMA, and FEC sublayers operate independent of block and packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

When the transmit channel is in normal mode, the PCS Transmit process continuously generates blocks based upon the TXD <31:0> and TXC <3:0> signals on the XGMII. The Gearbox function of the PCS Transmit process then packs the resulting bits into 16-bit transmit data-units. Transmit data-units are sent to the PMA, WIS, or FEC service interface via the PMA_UNITDATA.request, WIS_UNITDATA.request, or FEC_UNITDATA.request primitive, respectively. When the WIS is present, the PCS Transmit process also adapts between the XGMII and WIS data rates by deleting idle characters.

When the transmit channel is in test-pattern mode, a test pattern is packed into the transmit data-units that are sent to the PMA service interface via the PMA_UNITDATA.request primitive.

When the receive channel is in normal mode, the PCS Synchronization process continuously monitors PMA_SIGNAL.indication(SIGNAL_OK), WIS_SIGNAL.indication(SIGNAL_OK), or FEC_SIGNAL.indication(SIGNAL_OK). When SIGNAL_OK indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive, the WIS_UNITDATA.indication primitive, or the FEC_UNITDATA.indication primitive. It attains block synchronization based on the 2-bit synchronization headers and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the sync_status flag to indicate whether the PCS has obtained synchronization.

When the PCS Synchronization process has obtained synchronization, the BER monitor process monitors the signal quality asserting hi_ber if excessive errors are detected. When sync_status is asserted and hi_ber is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII. When the WIS is present, the PCS Receive process also adapts between the WIS and XGMII data rates by inserting idle characters. The PCS Receive process also sends the WIS_SIGNAL.request(PCS_R_STATUS) primitive to the WIS to indicate its status. The primitive is sent when the value of PCS_R_STATUS changes. The value of PCS_R_STATUS shall be FAIL when the Receive state diagram is in the RX_INIT state and OK otherwise.

When the receive channel is in test-pattern mode, the BER monitor process is disabled. The Receive process will be held in the RX_INIT state. The received bits will be compared to the test pattern and errors counted.

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A PCS that supports direct connection to a PMA shall provide transmit test-pattern mode for the square wave and pseudo-random patterns, and shall provide receive test-pattern mode for the pseudo-random pattern. The PCS may provide support for the PRBS9 transmit test pattern. It may provide support for the PRBS31 test pattern. Support of the optional PRBS31 test pattern shall include both the transmit and the receive capability for that pattern. Test-pattern mode is activated separately for transmit and receive. A PCS that supports direct connection to a PMA shall support transmit test-pattern mode and receive test-pattern mode operating simultaneously (if applicable) so as to support loopback testing. Test-pattern mode is provided by the WIS when a WIS is present.

49.2.3 Use of blocks

The PCS maps XGMII signals into 66-bit blocks, and vice versa, using a 64B/66B coding scheme. The synchronization headers of the blocks allow establishment of block boundaries by the PCS Synchronization process. Blocks are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks as provided by the rules in 49.2.4.

49.2.4 64B/66B transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters. The encodings defined by the transmission code ensure that sufficient transitions are present in the PHY bit stream to make clock recovery possible at the receiver. The encoding also preserves the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, the synchronization headers of the code enable the receiver to achieve block alignment on the incoming PHY bit stream. The 64B/66B transmission code specified for use in this standard has a high transition density and is a run-length-limited code.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 49–5 for transmit and Figure 49–6 for receive. These figures illustrate the processing of a block containing 8 data octets. See 49.2.4.3 for information on how blocks containing control characters are mapped. Note that the sync header is generated by the encoder and bypasses the scrambler.

49.2.4.1 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/66B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. Control characters other than /O/, /S/ and /T/ are labeled C_0 to C_7. The control character for ordered set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7.

Two consecutive XGMII transfers provide eight characters that are encoded into one 66-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfers.

Contents of block type fields, data octets and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled TxB<65:0> and RxB<65:0> respectively where TxB<0> and RxB<0> represent the first transmitted bit. The value of the sync header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

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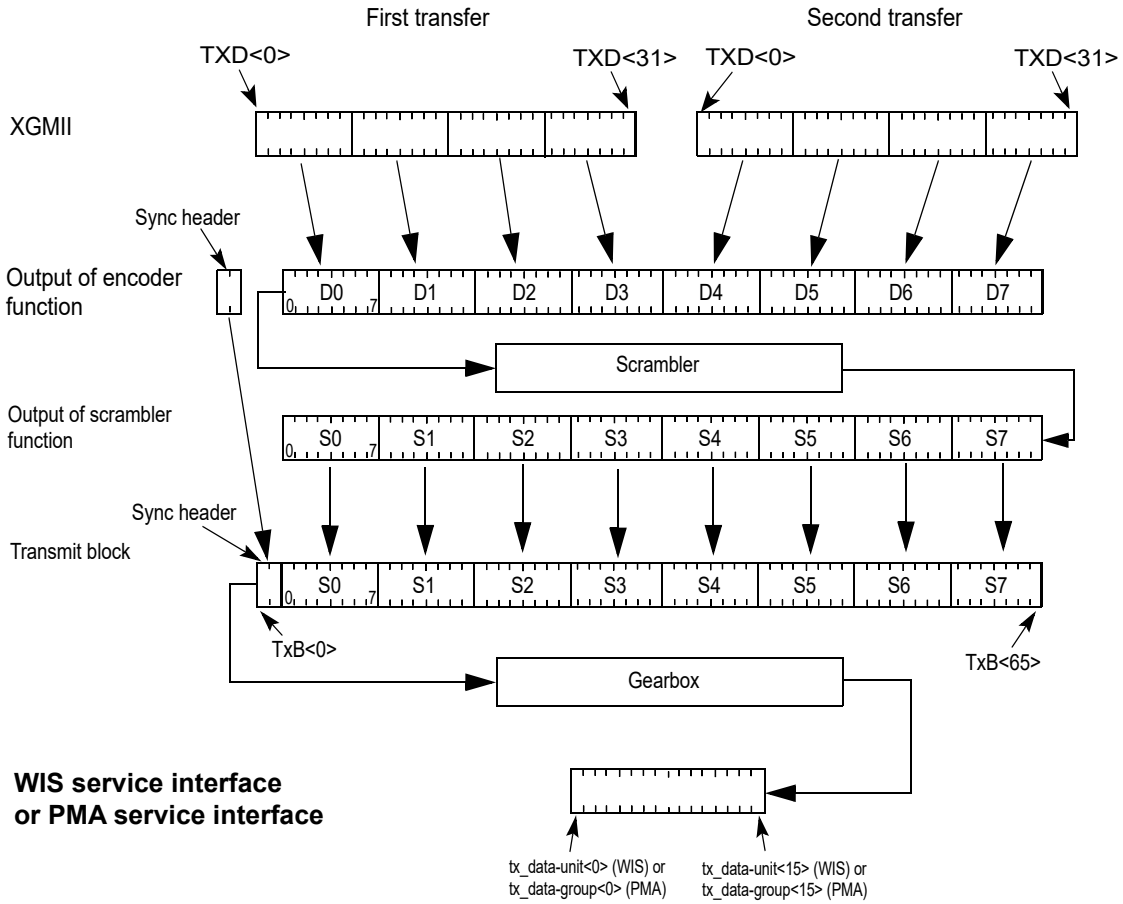

Figure 49–5—PCS Transmit bit ordering

49.2.4.2 Transmission order

Block bit transmission order is illustrated in Figure 49–5 and Figure 49–6. Note that these figures show the mapping from XGMII to 64B/66B block for a block containing eight data characters.

49.2.4.3 Block structure

Blocks consist of 66 bits. The first two bits of a block are the synchronization header (sync header). Blocks are either data blocks or control blocks. The sync header is 01 for data blocks and 10 for control blocks. Thus, there is always a transition between the first two bits of a block. The remainder of the block contains the payload. The payload is scrambled and the sync header bypasses the scrambler. Therefore, the sync header is the only position in the block that always contains a transition. This feature of the code is used to obtain block synchronization.

Data blocks contain eight data characters. Control blocks begin with an 8-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that character is implied by the block type field. Other control characters are encoded in a 7-bit control code or a 4-bit O Code. Each control block contains eight characters.

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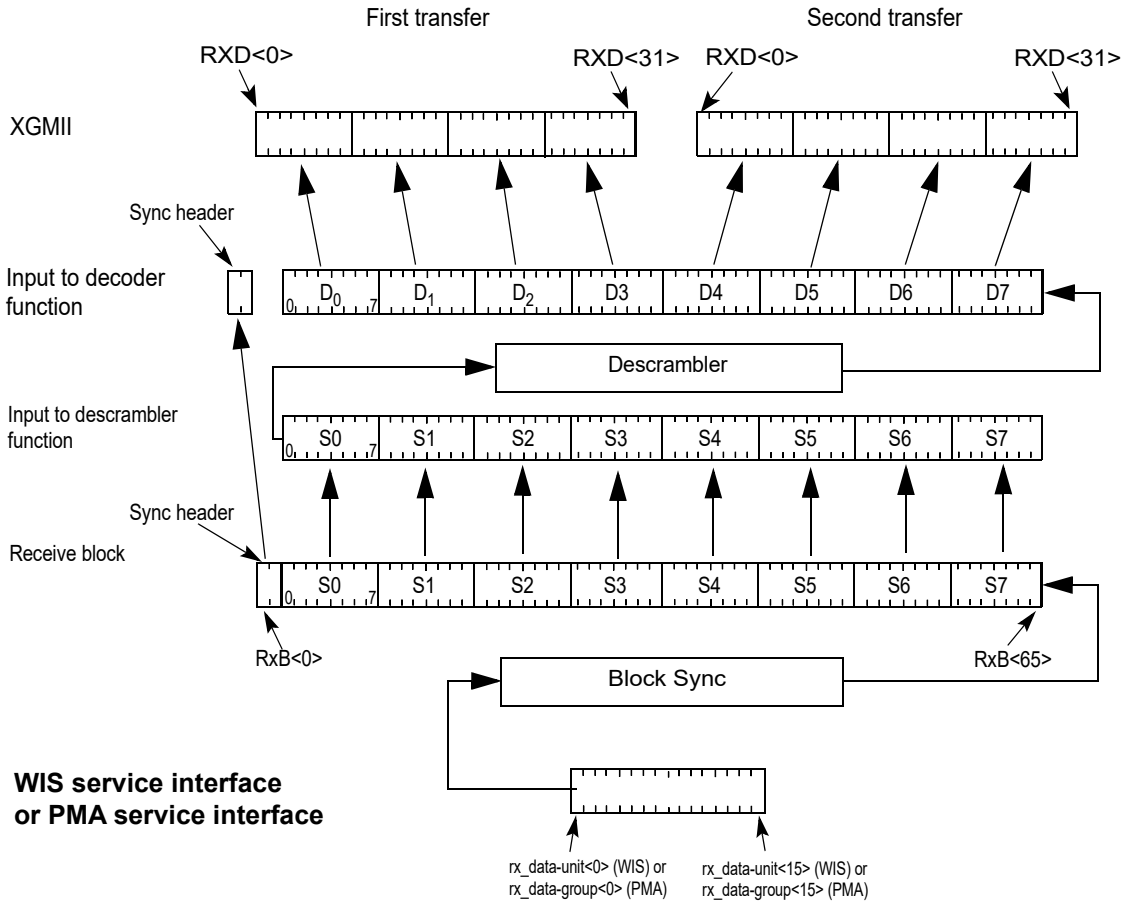

Figure 49–6—PCS Receive bit ordering

The format of the blocks is as shown in Figure 49–7. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 66-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the Input Data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt.

Bits and field positions are shown with the least significant bit on the left. Hexadecimal numbers are shown in normal hexadecimal. For example the block type field 0x1E is sent as 01111000 representing bits 2 through 9 of the 66 bit block. The least significant bit for each field is placed in the lowest numbered position of the field.

All unused values of block type field[93] are reserved.

[93]The block type field values have been chosen to have a 4-bit Hamming distance between them. The only unused value that maintains the Hamming distance is 0x00.

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49.2.4.4 Control codes

The same set of control characters are supported by the XGMII and the 10GBASE-R PCS. The representations of the control characters are the control codes. XGMII encodes a control character into an octet (an eight bit value). The 10GBASE-R PCS encodes the start and terminate control characters implicitly by the block type field. The 10GBASE-R PCS encodes the ordered set control codes using a combination of the block type field and a 4-bit O code for each ordered set. The 10GBASE-R PCS encodes each of the other control characters into a 7-bit C code.

The control characters and their mappings to 10GBASE-R control codes and XGMII control codes are specified in Table 49–1. All XGMII and 10GBASE-R control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received. The ability to transmit or receive Low Power Idle (LPI) is required for PHYs that support EEE (see Clause 78). If EEE is not supported, LPI shall not be transmitted and shall be treated as an error if received.

Input Data	**Sync**	**Block Payload**							
Bit Position: / **Data Block Format:**	0 1	2							65
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		**Block Type Field**							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	10	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	10	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	10	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	10	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	10	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	10	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	10	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	10	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	10	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	10	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	10	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 49–7—64B/66B block formats

49.2.4.5 Ordered sets

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and local fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the XGMII. 10 Gigabit Ethernet uses one kind of ordered set: the sequence ordered set (see 46.3.4). The sequence ordered set control character is denoted /Q/. An

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additional ordered set, the signal ordered set, has been reserved and it begins with another control code. The 4-bit O field encodes the control code. See Table 49–1 for the mappings.

49.2.4.6 Valid and invalid blocks

A block is invalid if any of the following conditions exists:

a) The sync field has a value of 00 or 11.
b) The block type field contains a reserved value.
c) Any control character contains a value not in Table 49–1.
d) Any O code contains a value not in Table 49–1, or the O code 0xF is received on an Ethernet PHY.
e) The set of eight XGMII characters does not have a corresponding block format in Figure 49–7.

49.2.4.7 Idle (/I/) and Low Power Idle (/LI/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

To communicate LPI, LPI control character /LI/ is sent continuously in place of /I/. LPI control characters are transmitted when LPI control characters are received from the XGMII. LPI characters may be added or deleted by the PCS to adapt between clock rates in a similar manner to idle control characters. /LI/ insertion and deletion shall occur in groups of four. /LI/s may only be added following other LPI characters.

Table 49–1—Control codes

Control character	Notation	XGMII Control Code	10GBASE-R Control Code	10GBASE-R O Code	8B/10B Code[a]
idle	/I/	0x07	0x00		K28.0 or K28.3 or K28.5
LPI	/LI/	0x06	0x06		K28.0 with D20.5 in one row or K28.3 or K28.5 with D20.5 in one row[b]
start	/S/	0xFB	Encoded by block type field		K27.7
terminate	/T/	0xFD	Encoded by block type field		K29.7
error	/E/	0xFE	0x1E		K30.7
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0	K28.4
reserved0	/R/[c]	0x1C	0x2D		K28.0
reserved1		0x3C	0x33		K28.1
reserved2	/A/	0x7C	0x4B		K28.3
reserved3	/K/	0xBC	0x55		K28.5

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Table 49–1—Control codes *(continued)*

Control character	Notation	XGMII Control Code	10GBASE-R Control Code	10GBASE-R O Code	8B/10B Code[a]
reserved4		0xDC	0x66		K28.6
reserved5		0xF7	0x78		K23.7
Signal ordered set[d]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF	K28.2

[a]For information only. The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48.
[b]See 48.2.4.2.
[c]The codes for /A/, /K/, and /R/ are used on the XAUI interface to signal idle. They are not present on the XGMII when no errors have occurred, but certain bit errors cause the XGXS to send them on the XGMII.
[d]Used by INCITS T11 Fibre Channel.

49.2.4.8 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<0:7> and RXD<0:7>). Receipt of an /S/ on any other octet of TxD indicates an error. Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

49.2.4.9 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and on any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

49.2.4.10 ordered set (/O/)

The ordered set control characters (/O/) indicate the start of an ordered set. There are two kinds of ordered sets: the sequence ordered set and the signal ordered set (which is reserved). When it is necessary to designate the control character for the sequence ordered set specifically, /Q/ will be used. /O/ is only valid on the first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered set.

Sequence ordered sets may be deleted by the PCS to adapt between clock rates. Such deletion shall only occur when two consecutive sequence ordered sets have been received and shall delete only one of the two. Only Idles may be inserted for clock compensation. Signal ordered sets are not deleted for clock compensation.

49.2.4.11 Error (/E/)

The /E/ is sent whenever an /E/ is received. It is also sent when invalid blocks are received. The /E/ allows physical sublayers such as the XGXS and PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 49.2.13.2.3 for further information.

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49.2.5 Transmit process

The transmit process generates blocks based upon the TXD<31:0> and TXC<3:0> signals received from the XGMII. Two XGMII data transfers are encoded into each block. It takes 4.125 PMA_UNITDATA or WIS_UNITDATA transfers to send a block of data. Therefore, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 16:33, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process will need to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates. The WIS data rate is always slower than the XGMII data rate and a PCS connected to a WIS deletes idles or sequence ordered sets to adapt between rates.

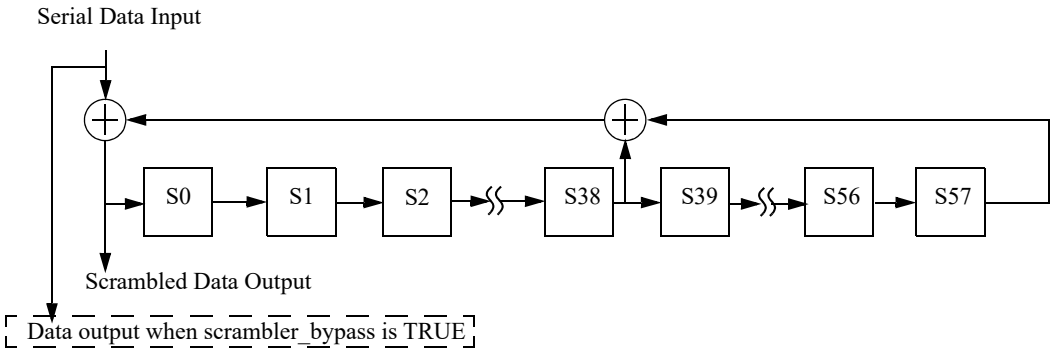
The transmit process generates blocks as specified in the transmit process state diagram. The contents of each block are contained in a vector tx_coded<65:0>, which is passed to the scrambler. tx_coded<1:0> contains the sync header and the remainder of the bits contain the block payload.

49.2.6 Scrambler

The payload of the block is scrambled with a self-synchronizing scrambler. The scrambler shall produce the same result as the implementation shown in Figure 49–8. This implements the scrambler polynomial:[94]

$$G(x) = 1 + x^{39} + x^{58} \tag{49–1}$$

There is no requirement on the initial value for the scrambler. The scrambler is run continuously on all payload bits. The sync header bits bypass the scrambler.



NOTE—Scrambler_bypass is only required to support EEE capability.

Figure 49–8—Scrambler

To aid block synchronization in the receiver for EEE capability when Clause 74 FEC is in use, when scrambler_bypass is TRUE the PCS shall pass the unscrambled data from the scrambler input rather than the scrambled data from the scrambler output. The scrambler shall continue to advance normally.

[94]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (49–1). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.

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49.2.7 Gearbox

The gearbox adapts between the 66-bit width of the blocks and the 16-bit width of the PMA or WIS interface. It receives the 66-bit blocks. When the transmit channel is operating in normal mode, the gearbox sends 16 bits of transmit data at a time via WIS_UNITDATA.request or PMA_UNITDATA.request primitives. The UNITDATA.request primitives are fully packed with bits. For example, if one block happened to start with the sync header on bits 0 and 1 of a PMA_UNITDATA.request, then the last two bits of that block would be on bits 0 and 1 of a PMA_UNITDATA.request and the next block would begin with a sync header on bits 2 and 3 of that PMA_UNITDATA.request. When a PMA_UNITDATA.request or WIS_UNITDATA.request contains bits from two blocks, then the bits from the first block shall be placed in the lowest numbered bits of tx_data-group<15:0>. The bits shall be packed into the tx_data-group in sequence with the lowest numbered bit of the block going into the lowest numbered bit of the part of tx_data-group<15:0> bits containing bits from that block (see Figure 49–5).

The gearbox functionality is necessary when the optional PMA compatibility interface, XSBI, is implemented since that interface passes data over a 16-bit wide path. It is also necessary when connecting to a WIS since the WIS processes the data stream with 8-bit granularity. When neither the WIS nor the XSBI is implemented, the internal data-path width between the PCS and PMA is an implementation choice. Depending on the path width, the gearbox functionality may not be necessary.

49.2.8 Test-pattern generators

When the transmit channel is operating in test-pattern mode, it sends 16 bits of test pattern at a time via PMA_UNITDATA.request primitives. When the PCS allows direct connection to the PMA, the test-pattern generator shall be implemented. The test-pattern generator does not apply to a PCS, which only supports connection to the WIS. A PCS which supports both WIS and direct PMA attachment may reject or allow an attempt to activate a transmit test-pattern mode when a WIS is attached.

There are two types of required transmit test patterns: square wave and pseudo-random. The square wave pattern is intended to aid in conducting certain transmitter tests. It is not intended for receiver tests and the receiver is not expected to receive this test pattern. The pseudo-random test-pattern mode is suitable for receiver tests and for certain transmitter tests. There is an optional PRBS9 transmit test pattern that may be used for some transmitter tests. There is also an optional PRBS31 test pattern, which may be used for some transmit and receiver tests. When this option is supported, both the PRBS31 test-pattern generator and the PRBS31 test-pattern checker shall be provided. See 52.9 and 68.6 for recommendations on the appropriate pattern for tests.

When square wave pattern is selected, the PCS will send a repeating pattern of n ones followed by n zeros where n may be any number between 4 and 11 inclusive. The value of n is an implementation choice.

When pseudo-random pattern is selected, the test pattern is generated by the scrambler using the seeds loaded through the MDIO registers and the selected data pattern. The scrambler is loaded with a seed or its inverse at the start of a block every 128 blocks. The seeds are loaded in the following pattern:

Seed A
Seed A Invert
Seed B
Seed B Invert

Invert indicates that the seed is inverted for that load. Either 64 zeros or the 64-bit encoding for two Local Fault ordered sets can be selected as the data pattern. After loading Seed A or Seed B, the scrambler input shall be driven with the data pattern. After loading Seed A Invert or Seed B Invert, the scrambler input shall be driven with the inverse of the data pattern. While in pseudo-random test-pattern mode, the sync headers will be the control sync header, 10. Thus the pseudo-random test pattern is a series of blocks with the control

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sync header and a pseudo-random payload. The characteristics of the pseudo-random test pattern can be varied by varying the seed values and data input.

When the optional PRBS31 mode is selected, the PRBS31 pattern generator sends 16 bits of PRBS31 test pattern at a time via PMA_UNITDATA.request primitives. The PRBS31 test pattern is the output of a Pseudo-Random Bit Sequence of order 31 (PRBS31) generator. The PRBS31 pattern generator shall produce the same result as the implementation shown in Figure 49–9. This implements the inverted version of the bit stream produced by the polynomial shown in Equation (49–2):[95]

$$G(x) = 1 + x^{28} + x^{31} \tag{49–2}$$

The initial value of the PRBS31 pattern generator shall not be all zeros. It may be any other value.

The optional PRBS9 pattern is defined in Table 68–6.

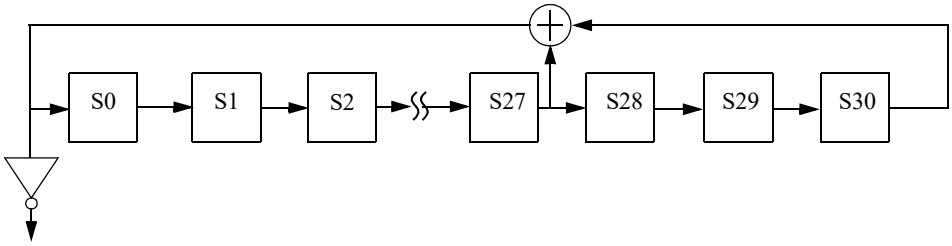

Figure 49–9—PRBS31 pattern generator

49.2.9 Block synchronization

When the receive channel is operating in normal mode, the block synchronization function receives data via 16-bit PMA_UNITDATA.request or WIS_UNITDATA.request primitives. It shall form a bit stream from the primitives by concatenating requests with the bits of each primitive in order from rx_data-group<0> to rx_data-group<15> (see Figure 49–6). It obtains lock to the 66-bit blocks in the bit stream using the sync headers and outputs 66-bit blocks. Lock is obtained as specified in the block lock state diagram shown in Figure 49–14.

If EEE is not supported then block_lock is identical to rx_block_lock. Otherwise the relationship between block_lock and rx_block_lock is given by Figure 49–13.

49.2.10 Descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. It shall produce the same result as the implementation shown in Figure 49–10.

49.2.11 Receive process

The receive process decodes blocks to produce RXD<31:0> and RXC<3:0> for transmission to the XGMII. Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized to a 16:33 ratio, the receive process will insert idles, delete idles, or delete sequence

[95]The convention here, which considers the most recent bit into the PRBS generator to be the lowest order term, is consistant with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the PRBS generator to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (49–2). In case of doubt, note that the conformance requirement is based on the representation in the figure rather than the polynomial equation.

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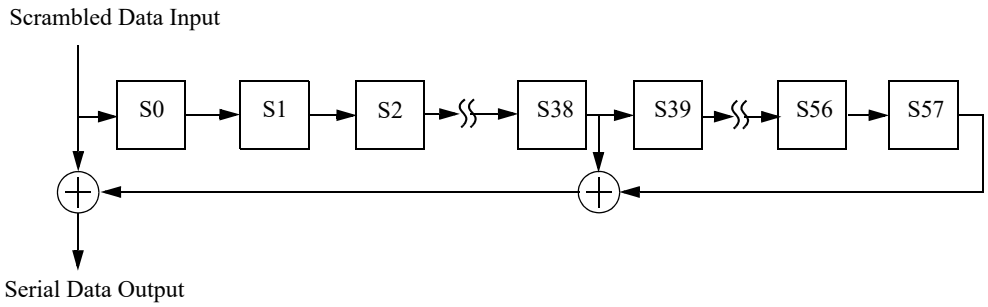

Figure 49–10—Descrambler

ordered sets to adapt between rates. The WIS data rate is always slower than the XGMII data rate and a PCS connected to a WIS will insert idles to adapt between the rates.

The receive process decodes blocks as specified in the receive state diagram shown in Figure 49–17.

49.2.12 Test-pattern checker

When the PCS allows direct connection to the PMA, the pseudo-random test-pattern checker shall be implemented. The pseudo-random test-pattern checker does not apply to a PCS, which only supports connection to the WIS. When the PRBS31 test-pattern option is supported, the PRBS31 receive test-pattern checker shall be implemented. A PCS that supports both WIS and direct PMA attachment may reject or allow an attempt to activate a receive test-pattern mode when a WIS is attached.

When the receive channel is operating in pseudo-random test-pattern mode, the pseudo-random test-pattern checker checks the bits received via PMA_UNITDATA.indication primitives.

The pseudo-random test-pattern checker utilizes the lock state diagram and the descrambler operating as they do during normal data reception. The hi_ber state diagram is disabled during receive test-pattern mode. When block_lock is true and the pseudo-random receive test-pattern mode is active, the pseudo-random test-pattern checker observes the output from the descrambler. When the output of the descrambler is the data pattern or its inverse, a match is detected. Since the transmitter's scrambler is loaded with a seed value every 128 blocks and the receiver's descrambler is running normally, a mismatch will be detected once every 128 blocks in the absence of errors. The pseudo-random test-pattern checker will count 128-block windows. When operating in pseudo-random test pattern, the test-pattern error counter counts blocks with a mismatch corrected to remove the effect of loading a new seed. The first block with a mismatch in a window shall not increment the test-pattern error counter. Any subsequent block with a mismatch in a window indicates an error and shall increment the test-pattern error counter.

When the receive channel is operating in PRBS31 test mode, the PRBS31 pattern checker checks the bits received in PMA_UNITDATA.indication primitives relative to the PRBS31 test pattern.

The PRBS31 pattern error checker is self-synchronizing. It compares each bit received to the result of the PRBS31 generator based on the prior 31 bits received. It shall produce the same result as the implementation shown in Figure 49–11. When no errors occur, the PRBS31 pattern error signal will be zero. When an isolated bit error occurs, it will cause the PRBS31 pattern error signal to go high three times; once when it is

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received and once when it is at each tap. The test-pattern error counter shall increment once for each bit time that the PRBS31 pattern error signal is high.

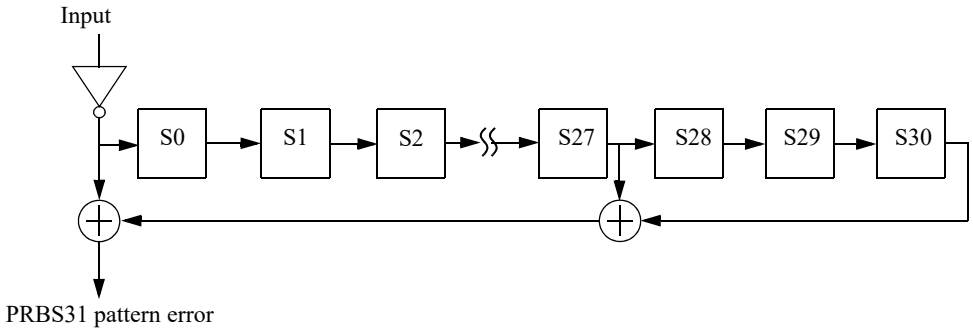

Figure 49–11—PRBS31 pattern checker

Note that the test-pattern error counter behavior is dependent on the test-pattern mode. In pseudo-random test mode, it is counting block errors. In PRBS31 test mode, it is counting bit errors at the PRBS31 pattern checker output.

49.2.13 Detailed functions and state diagrams

49.2.13.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

49.2.13.2 State variables

49.2.13.2.1 Constants

EBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<65:0>
: 66 bit vector to be sent to the PMA containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in 46.3.4.

LBLOCK_T<65:0>
: 66 bit vector to be sent to the PMA containing two Local Fault ordered sets.

49.2.13.2.2 Variables

ber_test_sh
: Boolean variable that is set true when a new sync header is available for testing and false when BER_TEST_SH state is entered. A new sync header is available for testing when the Block Sync process has accumulated enough bits from the PMA or the WIS to evaluate the header of the next block

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block_lock
: Boolean variable that is set true when receiver acquires block delineation

NOTE—If the EEE capability is supported, then this variable is affected by the LPI receive state diagram. If the EEE capability is not supported then this variable is identical to rx_block_lock controlled by the lock state diagram.

hi_ber
: Boolean variable which is asserted true when the ber_cnt equals 16 indicating a bit error ratio $>10^{-4}$

reset
: Boolean variable that controls the resetting of the PCS. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

r_test_mode
: Boolean variable that is asserted true when the receiver is in test-pattern mode.

rx_block_lock
: Variable used by the lock state diagram to reflect the status of the code-group delineation. This variable is set TRUE when the receiver acquires block delineation.

rx_coded<65:0>
: Vector containing the input to the 64B/66B decoder. The format for this vector is shown in Figure 49–7. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<65>.

rx_raw<71:0>
: Vector containing two successive XGMII transfers. RXC<0> through RXC<3> for the first transfer are placed in rx_raw<0> through rx_raw<3>, respectively. RXC<0> through RXC<3> for the second transfer are placed in rx_raw<4> through rx_raw<7>, respectively. RXD<0> through RXD<31> for the first transfer are placed in rx_raw<8> through rx_raw<39>, respectively. RXD<0> through RXD<31> for the second transfer are placed in rx_raw<40> through rx_raw<71>, respectively.

sh_valid
: Boolean indication that is set true if received block rx_coded has valid sync header bits. That is, sh_valid is asserted if rx_coded<0> ≠ rx_coded<1> and de-asserted otherwise.

signal_ok
: Boolean variable that is set based on the most recently received value of PMA_SIGNAL.indication(SIGNAL_OK), WIS_SIGNAL.indication(SIGNAL_OK), or FEC_SIGNAL.indication(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done
: Boolean variable that is asserted true when the SLIP requested by the Block Lock state diagram has been completed indicating that the next candidate block sync position can be tested.

test_sh
: Boolean variable that is set true when a new sync header is available for testing and false when TEST_SH state is entered. A new sync header is available for testing when the Block Sync process has accumulated enough bits from the PMA or the WIS to evaluate the header of the next block

tx_coded<65:0>
: Vector containing the output from the 64B/66B encoder. The format for this vector is shown in Figure 49–7. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<65>.

tx_raw<71:0>
: Vector containing two successive XGMII transfers. TXC<0> through TXC<3> for the first transfer are placed in tx_raw<0> through tx_raw<3>, respectively. TXC<0> through TXC<3> for the second transfer are placed in tx_raw<4> through tx_raw<7>, respectively. TXD<0> through TXD<31> for the first transfer are placed in tx_raw<8> through tx_raw<39>, respectively. TXD<0> through TXD<31> for the second transfer are placed in tx_raw<40> through tx_raw<71>, respectively.

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The following variables are used only for the EEE capability:

energy_detect
: A Boolean variable sent from the PMD that is set to TRUE when signal energy is detected at the receiver and is set to FALSE otherwise

rx_lpi_active
: A Boolean variable that is set to TRUE when the receiver is in a low power state and set to FALSE when it is in an active state and capable of receiving data.

rx_mode
: A variable set to QUIET while the receiver is in the RX_QUIET state and set to DATA otherwise

tx_mode
: A variable set to QUIET when the transmitter is in the TX_QUIET state, set to ALERT when the transmitter is in the TX_ALERT state, and set to DATA otherwise. When set to QUIET, the PMD disables the transmitter as described in 72.6.5. When set to ALERT, the PMD transmits a repeating pattern of eight ones and eight zeroes as described in 72.6.2. When set to DATA the PMD passes data as normal.

scrambler_bypass
: This Boolean variable is used to bypass the Tx PCS scrambler in order to assist rapid synchronization following low power idle. When set to TRUE, the PCS will pass the unscrambled data from the scrambler input rather than the scrambled data from the scrambler output. The scrambler will continue to operate normally, shifting input data into the delay line. When scrambler_bypass is set to FALSE the PCS will pass scrambled data from the scrambler output.

scr_bypass_enable
: A Boolean variable used to indicate to the transmit LPI state diagram that the scrambler bypass option is required. The PHY shall set scr_bypass_enable = TRUE if Clause 74 FEC is in use. The PHY shall set scr_bypass_enable = FALSE if this FEC is not in use.

49.2.13.2.3 Functions

DECODE(rx_coded<65:0>)
: Decodes the 66-bit vector returning rx_raw<71:0> that is sent to the XGMII. The DECODE function shall decode the block as specified in 49.2.4.

ENCODE(tx_raw<71:0>)
: Encodes the 72-bit vector returning tx_coded<65:0> of which tx_coded<63:0> is sent to the scrambler. The two high order sync bits bypass the scrambler. The ENCODE function shall encode the block as specified in 49.2.4.

R_BLOCK_TYPE = {C, S, T, D, E, LI}
: This function classifies each 66-bit rx_coded vector as belonging to one of the following types depending on its contents.

  Values: C; The vector contains a sync header of 10 and one of the following:
  a) A block type field of 0x1E and eight valid control characters other than /E/; and, if the EEE capability is supported, zero or four of the characters are /LI/;
  b) A block type field of 0x2D or 0x4B, a valid O code, and four valid control characters;
  c) A block type field of 0x55 and two valid O codes.

  LI; For EEE capability, the LI type is supported where the vector contains a sync header of 10, a block type field of 0x1E, and eight control characters of 0x06 (/LI/).

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S; The vector contains a sync header of 10 and one of the following:
a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.
T; The vector contains a sync header of 10, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.
D; The vector contains a sync header of 01.
E; The vector does not meet the criteria for any other value.

A valid control character is one containing a 10GBASE-R control code specified in Table 49–1. A valid O code is one containing an O code specified in Table 49–1.

NOTE—A PCS that does not support EEE classifies vectors containing one or more /LI/ control characters as type E.

R_TYPE(rx_coded<65:0>)

Returns the R_BLOCK_TYPE of the rx_coded<65:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

SLIP

Causes the next candidate block sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

T_BLOCK_TYPE = {C, S, T, D, E, LI}

This function classifies each 72-bit tx_raw vector as belonging to one of the following types depending on its contents.

Values: C; The vector contains one of the following:
a) eight valid control characters other than /O/, /S/, /T/ and /E/; and, if the EEE capability is supported, zero or four of the characters are /LI/;
b) one valid ordered set and four valid control characters other than /O/, /S/ and /T/;
c) two valid ordered sets.
LI; For EEE capability, this vector contains eight /LI/ characters.
S; The vector contains an /S/ in its first or fifth character, any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.
T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.
D; The vector contains eight data characters.
E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 49–1. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 49–1.

NOTE—A PCS that does not support EEE, classifies vectors containing one or more /LI/ control characters as type E.

T_TYPE(tx_raw<71:0>)

Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

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49.2.13.2.4 Counters

ber_cnt
: Count up to a maximum of 16 of the number of invalid sync headers within the current 125 μs period.

sh_cnt
: Count of the number of sync headers checked within the current 64 block window.

sh_invalid_cnt
: Count of the number of invalid sync headers within the current 64 block window.

The following counter is used only for the EEE capability.

wake_error_counter
: A counter that is incremented each time that the LPI receive state diagram enters the RX_WTF state indicating that a wake time fault has been detected. The counter is reflected in register 3.22 (see 45.2.3.12).

49.2.13.2.5 Timers

State diagram timers follow the conventions of 14.2.3.2.

125us_timer
: Timer that is triggered every 125 μs +1%, –25%.

The following timers are used only for the EEE capability:

one_us_timer
: A timer used to count approximately 1 μs intervals. The timer terminal count is set to T_{1U}. When the timer reaches terminal count it will set the one_us_timer_done = TRUE.

rx_tq_timer
: This timer is started when the PCS receiver enters the RX_SLEEP state. The timer terminal count is set to T_{QR}. When the timer reaches terminal count it will set the rx_tq_timer_done = TRUE.

rx_tw_timer
: This timer is started when the PCS receiver enters the RX_WAKE state. The timer terminal count shall be set to a value no larger than the maximum value given for T_{WR} in Table 49–3. When the timer reaches terminal count it will set the rx_tw_timer_done = TRUE.

rx_wf_timer
: This timer is started when the PCS receiver enters the RX_WTF state, indicating that the receiver has encountered a wake time fault. The rx_wf_timer allows the receiver an additional period in which to synchronize or return to the QUIET state before a link failure is indicated. The timer terminal count is set to T_{WTF}. When the timer reaches terminal count it will set the rx_wf_timer_done = TRUE.

tx_ts_timer
: This timer is started when the PCS transmitter enters the TX_SLEEP state. The timer terminal count is set to T_{SL}. When the timer reaches terminal count it will set the tx_ts_timer_done = TRUE.

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tx_tq_timer
: This timer is started when the PCS transmitter enters the TX_QUIET state. The timer terminal count is set to T_{QL}. When the timer reaches terminal count it will set the tx_tq_timer_done = TRUE.

tx_tw_timer
: This timer is started when the PCS transmitter enters the TX_WAKE state. The timer terminal count is set to T_{WL}. When the timer reaches terminal count it will set the tx_tw_timer_done = TRUE.

49.2.13.3 State diagrams

The Lock state diagram shown in Figure 49–14 determines when the PCS has obtained lock to the received data stream. The BER Monitor state diagram shown in Figure 49–15 monitors the received signal for high bit error ratio.

The Transmit state diagram shown in Figure 49–16 controls the encoding of transmitted blocks. It makes exactly one transition for each transmit block processed. Though the Transmit state diagram sends Local Fault ordered sets when reset is asserted, the scrambler and gearbox may not be operational during reset. Thus, the Local Fault ordered sets may not appear on the WIS or PMA service interface.

The Receive state diagram shown in Figure 49–17 controls the decoding of received blocks. It makes exactly one transition for each receive block processed.

The PCS shall perform the functions of Lock, BER Monitor, Transmit, and Receive as specified in these state diagrams, including the optional EEE capability if implemented.

49.2.13.3.1 LPI state diagrams

A PCS that supports the EEE capability shall implement the LPI transmit and receive processes as shown in Figure 49–12 and Figure 49–13. The transmit LPI state diagram controls tx_mode, which disables the transmitter when it is set to QUIET. The receive LPI state diagram controls block_lock during LPI and signals the end of LPI to the receive state diagram.

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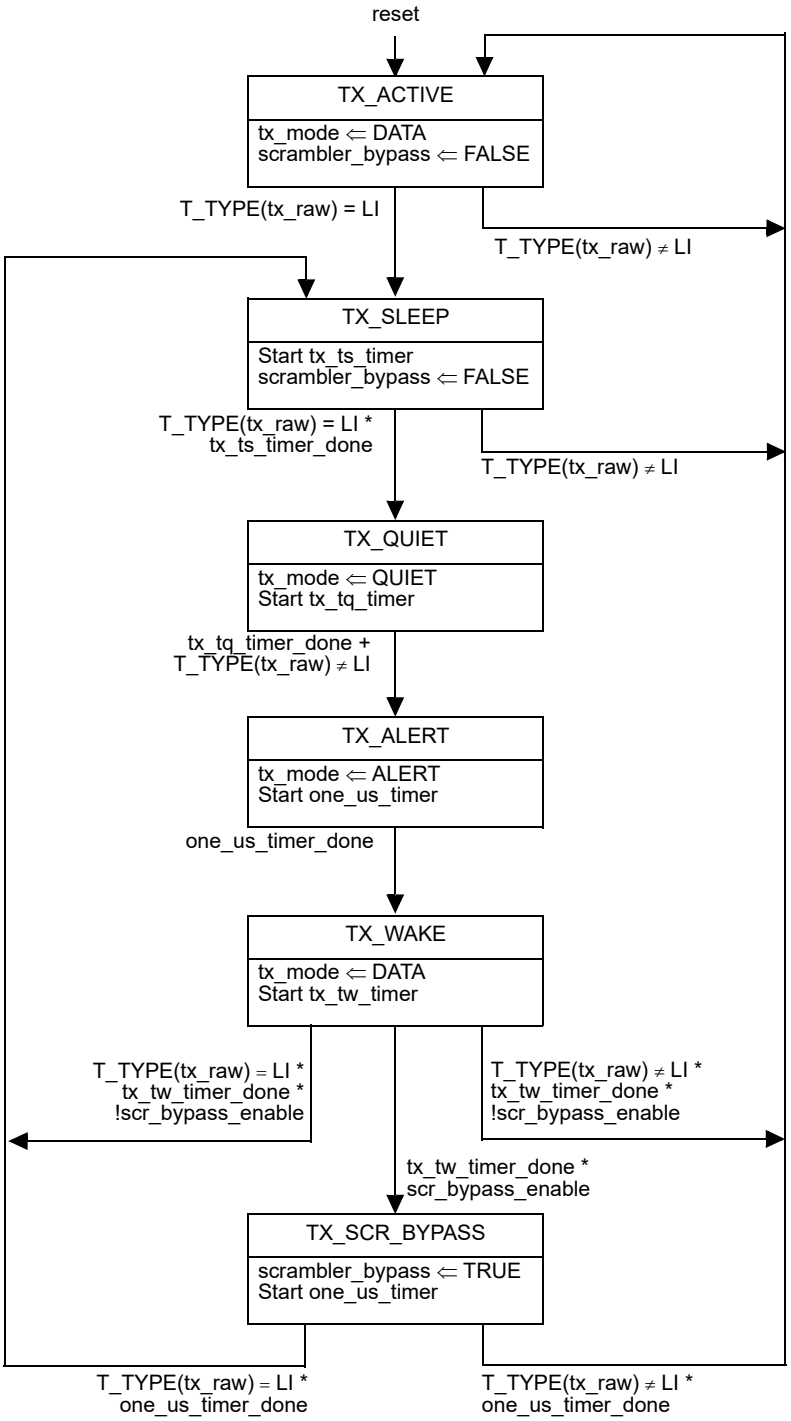

Figure 49–12—LPI Transmit state diagram

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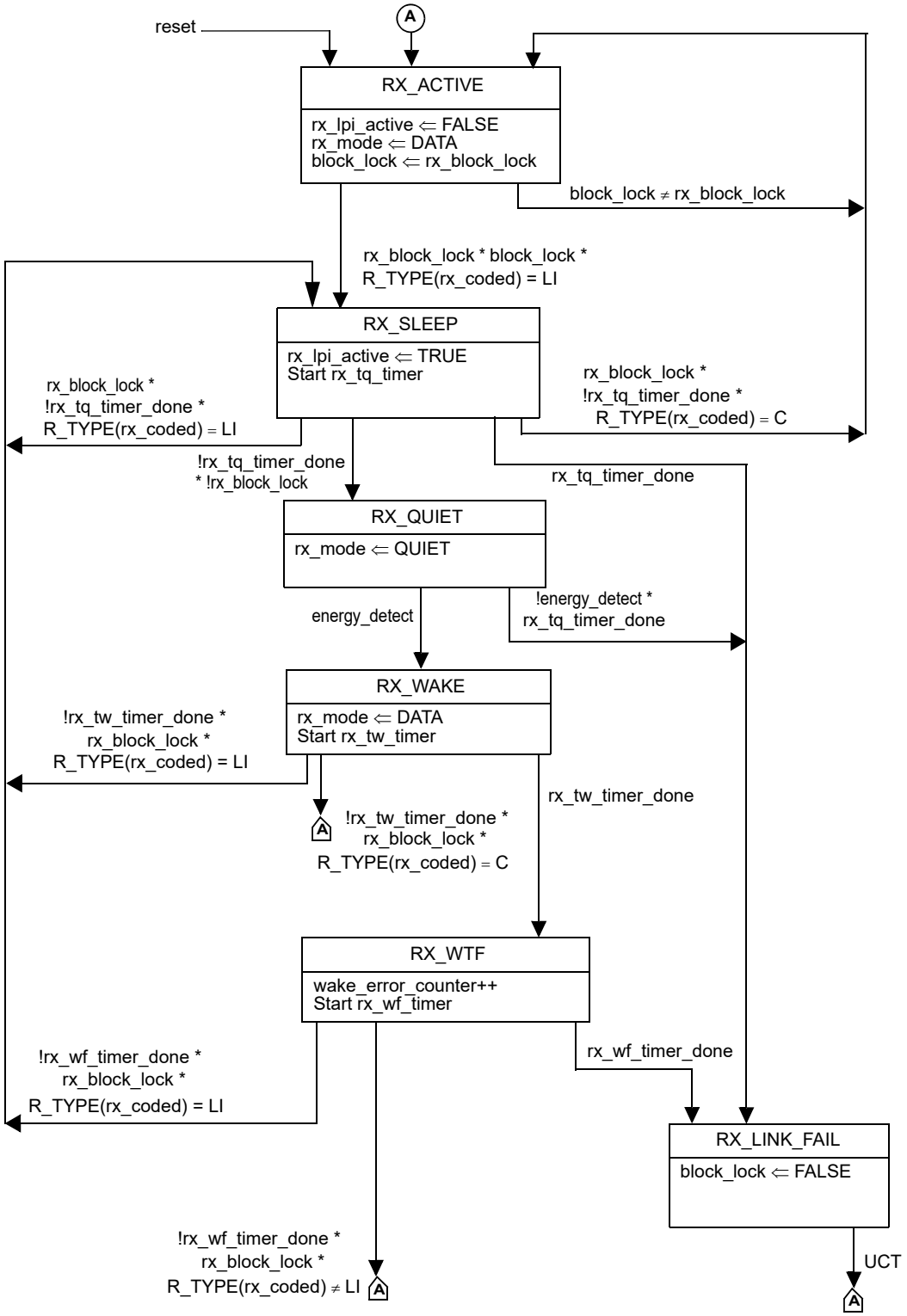

Figure 49–13—LPI Receive state diagram

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Following a period of LPI, the receiver is required to achieve block synchronization within the wake-up time specified (see Figure 49–13). The implementation of the block synchronization state diagram should use techniques to ensure that block lock is achieved with minimal numbers of slip attempts. When the Clause 74 FEC is enabled, the receiver may use the knowledge that the link partner's transmitter will bypass the scrambler as part of the wake sequence. The idle sequence following this event will form a fixed pattern for the duration of the wake period.

The LPI functions shall use timer values for these state diagrams as shown in Table 49–2 for transmit and Table 49–3 for receive.

Table 49–2—Transmitter LPI timing parameters

Parameter	Description	Min	Max	Units
T_{SL}	Local Sleep Time from entering the TX_SLEEP state to when tx_mode is set to QUIET	4.9	5.1	µs
T_{QL}	Local Quiet Time from when tx_mode is set to QUIET to entry into the TX_ALERT state	1.7	1.8	ms
T_{WL}	Time spent in the TX_WAKE state	10.9	11.1	µs
T_{1U}	Time spent in the TX_ALERT and TX_SCR_BYPASS states	1.1	1.3	µs

Table 49–3—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for energy_detect to be set to TRUE while in the RX_SLEEP and RX_QUIET states before asserting receive fault	2	3	ms
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault (when scr_bypass_enable = FALSE)	—	11.5	µs
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault (when scr_bypass_enable = TRUE)	—	13.7	µs
T_{WTF}	Wake time fault recovery time	—	10	ms

49.2.14 PCS Management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

49.2.14.1 Status

PCS_status:
: Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_ber is false. This status is reflected in MDIO register 3.32.12. A latch low view of this status is reflected in MDIO register 3.1.2 and a latch high of the inverse of this status, Receive fault, is reflected in MDIO register 3.8.10.

block_lock:
: Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.32.0. A latch low view of this status is reflected in MDIO register 3.33.15.

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hi_ber:
: Indicates the state of the hi_ber variable. This status is reflected in MDIO register 3.32.1. A latch high view of this status is reflected in MDIO register 3.33.14.

Rx LPI indication:
: For EEE capability, this variable indicates the current state of the receive LPI function. This flag is set to TRUE (register bit set to one) when the LPI receive state diagram is in any state other than RX_ACTIVE. This status is reflected in MDIO register 3.1.8. A latch high view of this status is reflected in MDIO register 3.1.10 (Rx LPI received).

Tx LPI indication:
: For EEE capability, this variable indicates the current state of the transmit LPI function. This flag is set to TRUE (register bit set to one) when the LPI transmit state diagram is in any state other than TX_ACTIVE. This status is reflected in MDIO register 3.1.9. A latch high view of this status is reflected in MDIO register 3.1.11 (Tx LPI received).

49.2.14.2 Counters

The following counters are reset to zero upon read and upon reset of the PCS. When they reach all ones, they stop counting. Their purpose is to help monitor the quality of the link.

ber_count:
: 6-bit counter that counts each time BER_BAD_SH state is entered. This counter is reflected in MDIO register bits 3.33.13:8. Note that this counter counts a maximum of 16 counts per 125 μs since the BER_BAD_SH can be entered a maximum of 16 times per 125 μs window.

errored_block_count:
: 8-bit counter. When the receiver is in normal mode, errored_block_count counts once for each time RX_E state is entered. This counter is reflected in MDIO register bits 3.33.7:0.

test_pattern_error_count:
: 16-bit counter. When the receiver is in test-pattern mode, the test_pattern_error_count counts errors as described in 49.2.12. This counter is reflected in MDIO register bits 3.43.15:0.

49.2.14.3 Test mode control

tx_test_mode:
: Boolean variable controlling transmit channel operating mode. When false, the transmit channel operates in normal mode. When true, the transmit channel operates in test-pattern mode.

rx_test_mode:
: Boolean variable controlling receive channel operating mode. When false, the receive channel operates in normal mode. When true, the receive channel operates in test-pattern mode.

49.2.14.4 Loopback

The PCS shall be placed in Loopback mode when the Loopback bit in MDIO register 3.0.14 is set to a logic one. In this mode, the PCS shall accept data on the transmit path from the XGMII and return it on the receive path to the XGMII. In addition, the PCS shall transmit a continuous stream of 0x00FF data words to the PMA or WIS sublayer, and shall ignore all data presented to it by the PMA or WIS sublayer.

49.2.15 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and

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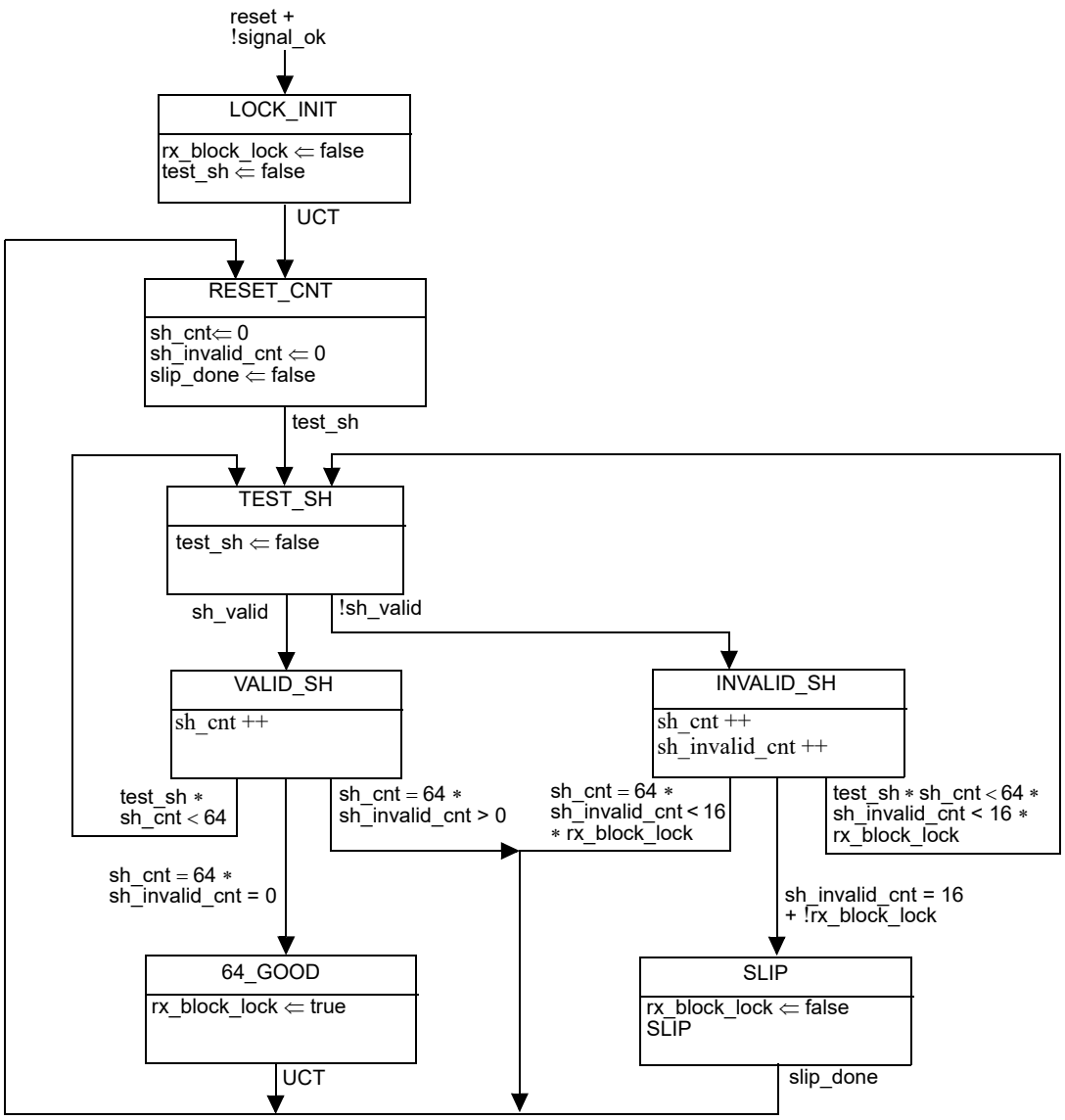

Figure 49–14—Lock state diagram

administrators conform to constraints regarding the cable topology and concatenation of devices. The sum of transmit and receive delay contributed by the 10GBASE-R PCS shall be no more than 3584 BT.

49.2.16 Auto-Negotiation for Backplane Ethernet

The following requirements apply to a PCS used with a 10GBASE-KR PMD. Support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

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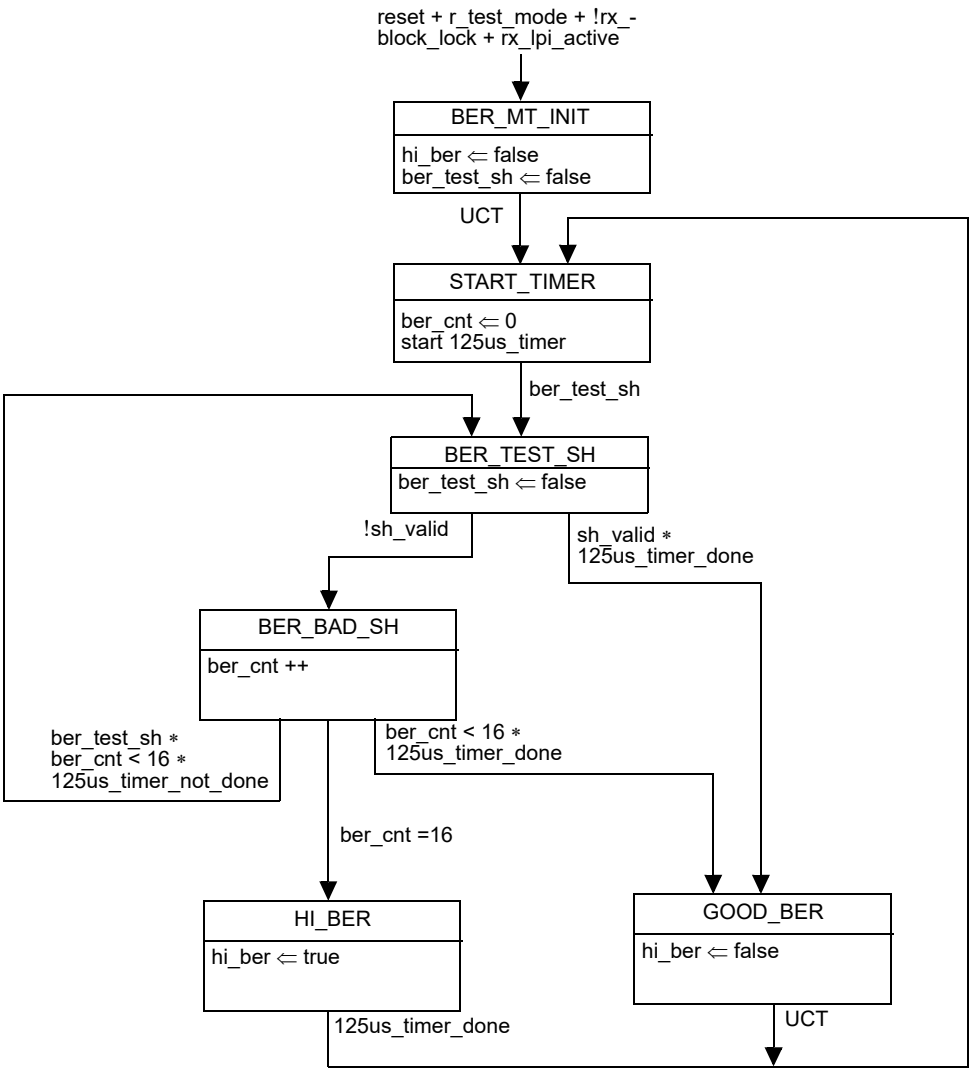

Figure 49–15—BER monitor state diagram

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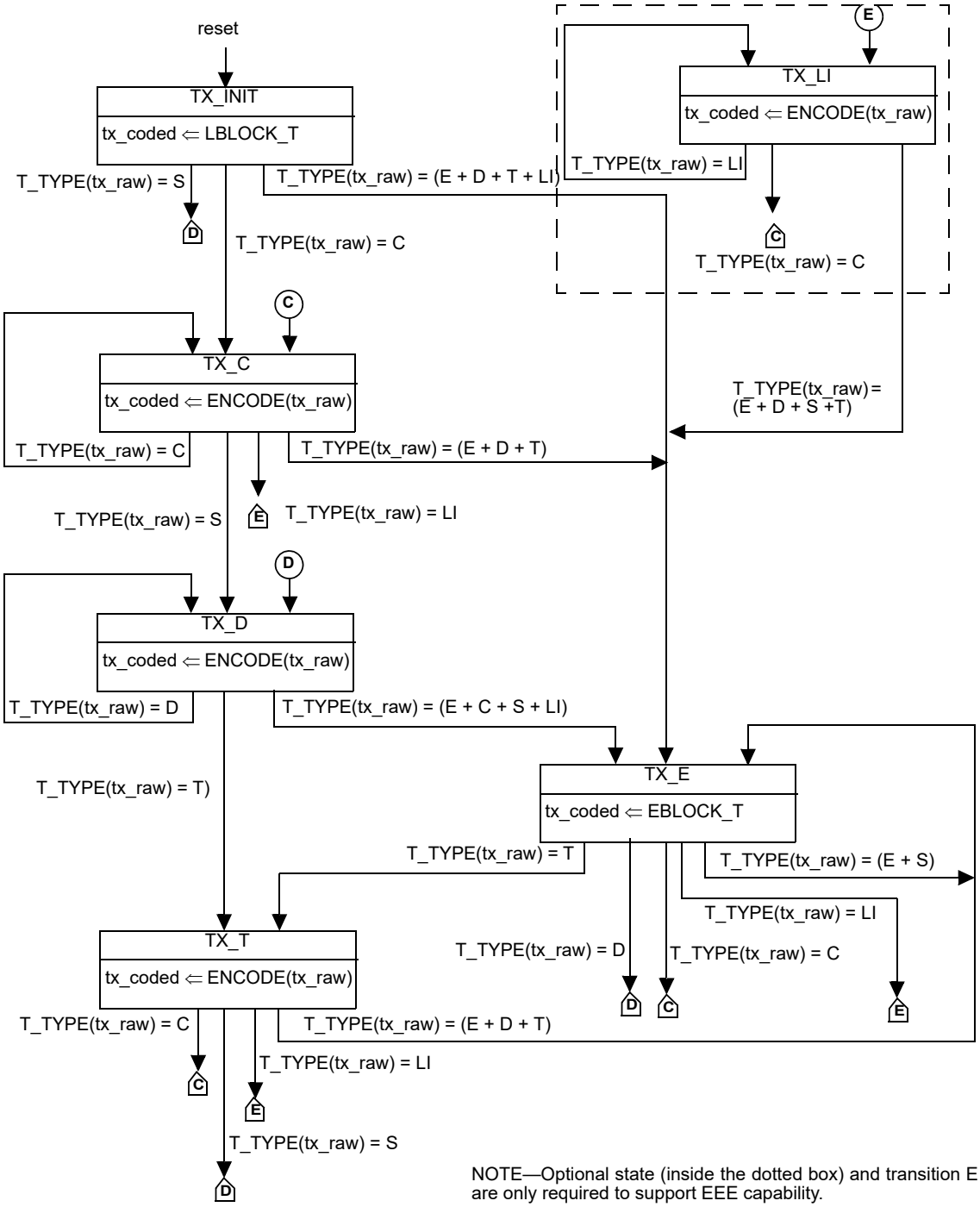

Figure 49–16—Transmit state diagram

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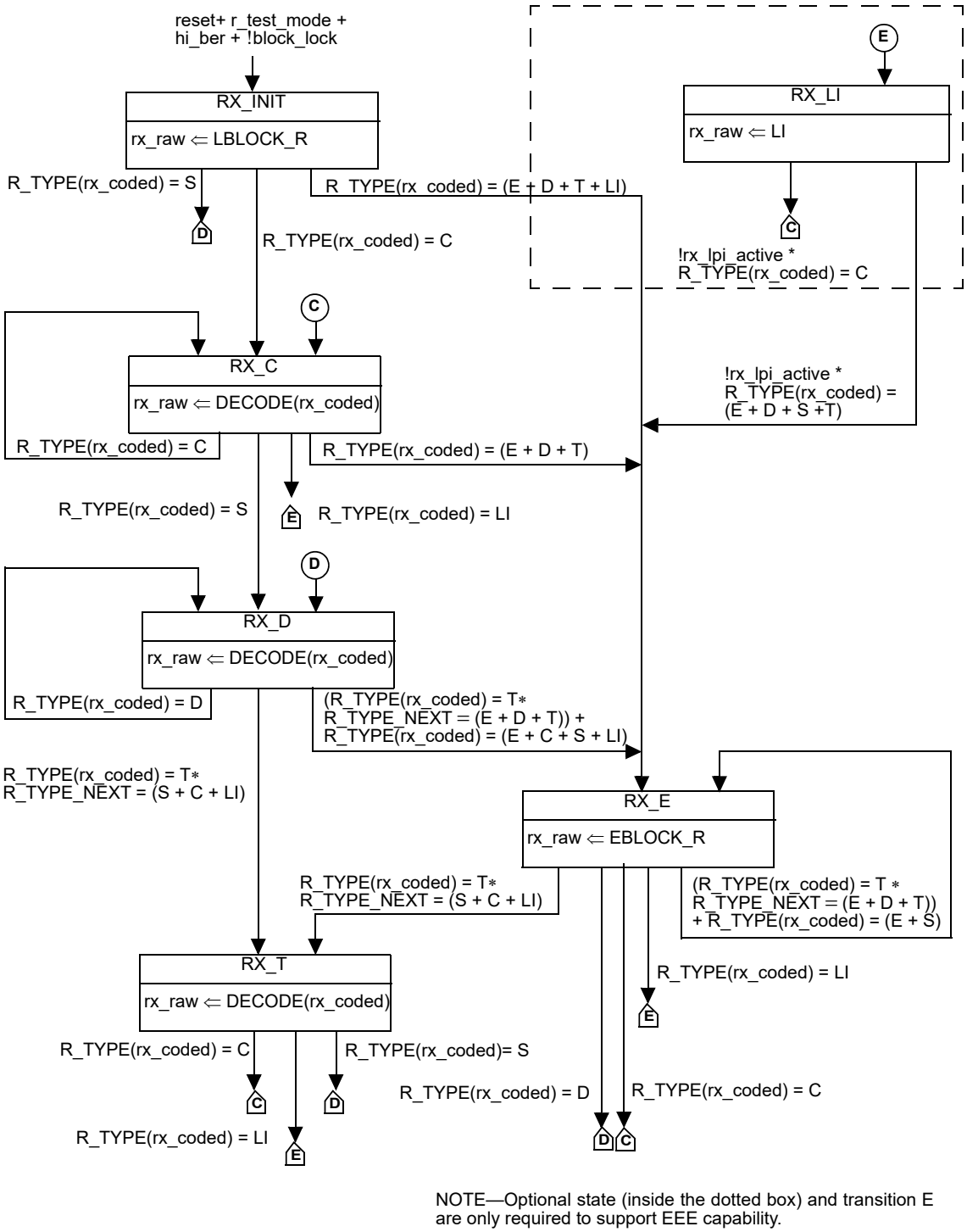

Figure 49–17—Receive state diagram

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49.3 Protocol implementation conformance statement (PICS) proforma for Clause 49, Physical Coding Sublayer (PCS) type 10GBASE-R[96]

49.3.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 49, Physical Coding Sublayer (PCS), type 10GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

49.3.2 Identification

49.3.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

49.3.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 49, Physical Coding Sublayer (PCS), type 10GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[96] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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49.3.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XSBI	XBSI compatibility interface	51, 49.1.5	Compatibility interface is supported	O	Yes [ ] No [ ]
XGE	XGMII compatibility interface	46, 49.1.5	Compatibility interface is supported	O	Yes [ ] No [ ]
*MD	MDIO	45, 49.2.14	Registers and interface supported	O	Yes [ ] No [ ]
*WIS	Supports operation with a WIS	49.1.5		O.1	Yes [ ] No [ ]
*PMA	Supports operation directly connected to a PMA	49.1.5		O.1	Yes [ ] No [ ]
*JTM	Supports test-pattern mode	49.2.2		PMA:M	Yes [ ] N/A[ ]
*LPI	Implementation of LPI	49.2.4.4		O	Yes [ ] No [ ]

49.3.4 PICS Proforma Tables for PCS, type 10GBASE-R

49.3.4.1 Coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder implements the code as specified	49.2.13.2.3 and 49.2.4		M	Yes [ ]
C2	Decoder implements the code as specified	49.2.13.2.3 49.2.4		M	Yes [ ]
C3	IDLE control code insertion and deletion	49.2.4.7	Insertion or Deletion in groups of 4 /I/s	M	Yes [ ]
C4	IDLE control code deletion	49.2.4.7	When deleting /I/s, the first four characters after a /T/ shall not be deleted.	M	Yes [ ]
C5	Sequence ordered set deletion	49.2.4.10	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ]

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49.3.4.2 Scrambler and Descrambler

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Scrambler	49.2.6	Performs as shown in Figure 49–8	M	Yes [ ]
S2	Descrambler	49.2.10	Performs as shown in Figure 49–10	M	Yes [ ]

49.3.5 Test-pattern modes

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Square wave and pseudo-random transmit test-pattern generators are implemented	49.2.8	Performs as in 49.2.8	JTM:M	Yes [ ] N/A[ ]
JT2	Pseudo-random receive test-pattern checker is implemented	49.2.12	Performs as in 49.2.12	JTM:M	Yes [ ] N/A[ ]
JT3	Transmit and receive test-pattern modes can operate simultaneously	49.2.2		JTM:M	Yes [ ] N/A[ ]
JT4	Reject transmit test-pattern mode when WIS is attached	49.2.8		JTM:O	Yes [ ] No [ ] N/A[ ]
JT5	Reject receive test-pattern mode when WIS is attached	49.2.12		JTM:O	Yes [ ] No [ ] N/A[ ]
*JT6	Support for PRBS31 test pattern	49.2.8		JTM:O	Yes [ ] No [ ] N/A[ ]
JT7	PRBS31 test-pattern generator is implemented	49.2.8	Performs as in 49.2.8	JT6:M	Yes [ ] N/A[ ]
JT8	PRBS31 test-pattern checker is implemented	49.2.12	Performs as in 49.2.12	JT6:M	Yes [ ] N/A[ ]
*JT9	Support for PRBS9 transmit test pattern	49.2.8		JTM:O	Yes [ ] No [ ] N/A[ ]
JT10	PRBS9 transmit test pattern is implemented	49.2.8	Performs as in 49.2.8	JT9:M	Yes [ ] N/A[ ]

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49.3.5.1 Bit order

Item	Feature	Subclause	Value/Comment	Status	Support
B1	Transmit bit order	49.2.7	Placement of bits into tx_data-group<15:0> as specified in 49.2.7	M	Yes [ ]
B2	Receive bit order	49.2.9	Placement of bits from rx_data-group<15:0> into blocks as specified in 49.2.9	M	Yes [ ]

49.3.6 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Equivalent access to PCS Management objects is provided	49.2.14		!MD:O	Yes [ ] No [ ] N/A [ ]

49.3.6.1 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Lock	49.2.13.3	Meets the requirements of Figure 49–14	M	Yes [ ]
SM2	BER Monitor	49.2.13.3	Meets the requirements of Figure 49–15	M	Yes [ ]
SM3	Transmit	49.2.13.3	Meets the requirements of Figure 49–16	M	Yes [ ]
SM4	Receive	49.2.13.3	Meets the requirements of Figure 49–17	M	Yes [ ]
SM5	PCS_R_Status	49.2.2	PCS_R_STATUS is FAIL in RX_INIT state; OK otherwise	M	Yes [ ]

49.3.6.2 WIS

Item	Feature	Subclause	Value/Comment	Status	Support
W1	Supports WIS_SIGNAL.request	49.2.2	PCS_R_STATUS is FAIL when in RX_INIT state	WIS:M	Yes [ ] N/A[ ]

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49.3.6.3 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports Loopback	49.2.14.4	Performs as in 49.2.14.4	M	Yes [ ]

49.3.6.4 Delay Constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS Delay Constraint	49.2.15	No more than 3584 BT for sum of transmit and receive path delays	M	Yes [ ]

49.3.6.5 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
*AN1	Support for use with a 10GBASE-KR PMD	49.2.16	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN2	AN_LINK.indication primitive	49.2.16	Support of the primitive AN_LINK.indication(link_status), when the PCS is used with 10GBASE-KR PMD	AN1:M	Yes [ ] N/A [ ]
AN3	link_status parameter	49.2.16	Takes the value OK or FAIL, as described in 49.2.16	AN1:M	Yes [ ] N/A [ ]
AN4	Generation of AN_LINK.indication primitive	49.2.16	Generated when the value of link_status changes	AN1:M	Yes [ ] N/A [ ]

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49.3.6.6 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
LP-01	Insertion and deletion of LPIs in groups of four	49.2.4.7		LPI:M	Yes [ ] N/A [ ]
LP-02	Unscrambled data transmitted when scrambler_bypass = TRUE	49.2.6		LPI:M	Yes [ ] N/A [ ]
LP-03	Scrambler continues to operate as normal when scrambler_bypass = TRUE	49.2.6		LPI:M	Yes [ ] N/A [ ]
LP-04	scr_bypass_enable = TRUE when FEC is in use	49.2.13.2.2		LPI:M	Yes [ ] N/A [ ]
LP-05	Transmit state diagrams	49.2.13.3	Support additions to Figure 49–16 for EEE capability	LPI:M	Yes [ ] N/A [ ]
LP-06	Receive state diagrams	49.2.13.3	Support additions to Figure 49–17 for EEE capability	LPI:M	Yes [ ] N/A [ ]
LP-07	LPI transmit state diagrams	49.2.13.3.1	Meets the requirements of Figure 49–12	LPI:M	Yes [ ] N/A [ ]
LP-08	LPI receive state diagrams	49.2.13.3.1	Meets the requirements of Figure 49–13	LPI:M	Yes [ ] N/A [ ]
LP-09	LPI transmit timing	49.2.13.3.1	Meets the requirements of Table 49–2	LPI:M	Yes [ ] N/A [ ]
LP-10	LPI receive timing	49.2.13.3.1	Meets the requirements of Table 49–3	LPI:M	Yes [ ] N/A [ ]

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50. WAN Interface Sublayer (WIS), type 10GBASE-W

50.1 Overview

The WAN Interface Sublayer (WIS) is an optional PHY sublayer that may be used to create a 10GBASE-W PHY that is data-rate and format compatible with the SONET STS-192c transmission format defined by ANSI, as well as the Synchronous Digital Hierarchy (SDH) VC-4-64c container specified by ITU. The purpose of the WIS is to allow 10GBASE-W equipment to generate Ethernet data streams that may be mapped directly to STS-192c or VC-4-64c streams at the PHY level, without requiring MAC or higher-layer processing. The WIS therefore specifies a subset of the logical frame formats in the SONET and SDH standards. In addition, the WIS constrains the effective data throughput at its service interface to the payload capacity of STS-192c / VC-4-64c, i.e., 9.58464 Gb/s. Multiplexed SONET/SDH formats are not supported.

The WIS does not render a 10GBASE-W PHY compliant with either SONET or SDH at any rate or format. A 10GBASE-W interface is not intended to interoperate directly with interfaces that comply with SONET or SDH standards, or other synchronous networks. Such interoperation would require full conformance to the optical, electrical, and logical requirements specified by SONET or SDH, and is outside the scope and intent of this standard. Operation over electrically multiplexed payloads of a transmission network is outside the scope of this standard.

From the perspective of the 10 Gb/s MAC layer, a 10GBASE-W PHY does not appear different (in either the functions or service interface) from a PHY without a WIS, with the exception of sustained data rate. However, a 10GBASE-W interface may interoperate only with another 10GBASE-W interface.

50.1.1 Scope

This clause specifies the functions, features, services, and protocol of the WIS. The WIS may be used with any of the PCS, PMA, and PMD sublayers that are defined for 10GBASE-W, as shown in Figure 50–1, it is placed between the PCS and PMA sublayers within the 10GBASE-W PHY. The WIS is common to all members of the family of 10GBASE-W WAN-compatible PHY implementations. There are currently three embodiments within this family: 10GBASE-SW, 10GBASE-LW, and 10GBASE-EW.

The definition of the WIS is based on the subset of signaling rates and data formats standardized by ATIS-0600416.1999(R2010), which in turn is based on ATIS-0900105.2008. The WIS maps the encoded Ethernet data received (transmitted) from (to) the PCS into a frame structure that has the same format as that defined by ATIS-0600416.1999(R2010), implementing a minimal number of the standard SONET overhead fields and functions. The WIS does not adhere to the electrical and optical aspects of SONET specified by ATIS-0600416.1999(R2010), as it is intended to be used with PHYs that conform to the corresponding parameters defined by the 10GBASE-W standard.

The WIS shall meet all requirements of ATIS-0600416.1999(R2010) except those that are specifically excluded by this clause. The following sections of ATIS-0600416.1999(R2010) are excluded in their entirety:

a) Section 5 (Jitter)
b) Section 6 (Synchronization)
c) Section 7.2.2 (VT1.5 rate—Electrical Interface)
d) Section 7.4.2 (VT1.5 rate)
e) Section 7.6 (Performance and failure alarm monitoring)
f) Section 7.7 (Performance monitoring functions)
g) Annex A (SONET VT1.5 Line Interface Common Criteria)
h) Annex B (SONET maintenance signals for the NI)

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i) Annex C (Receiver jitter tolerance and transfer)

For convenience and clarity of explanation, this clause employs the notational conventions, nomenclature, and acronyms of SONET as defined by ATIS-0600416.1999(R2010). This should not, however, be taken as implying that the WIS excludes compatibility with ITU-defined SDH rates and formats.

50.1.2 Objectives

The following are the objectives for the WIS:

a) To support the full duplex mode of operation of the Ethernet MAC
b) To support the PCS, PMA and PMD sublayers defined for 10GBASE-W
c) To provide a 9.95328 Gb/s effective data rate at the service interface presented by the PMA sublayer, conforming with the requirements of SONET STS-192c and SDH VC-4-64c frame rates
d) To implement the framing, scrambling, and defect/anomaly detection to allow minimal compatibility with the requirements of both SONET and SDH transmission networks
e) To preserve the full duplex behavior and BER objectives of the PCS and PMD sublayers with which it may be used

NOTE—This clause will always use the term “WIS frames” when referring to the SONET-compatible frame format that is generated and terminated by the WIS, in order to distinguish such frames from those generated and terminated by the MAC. The WIS has no involvement with, or visibility into, the MAC framing processes. The “WIS frames” handled by the WIS are not propagated to higher layers via the WIS service interface; they are only exchanged between WIS peer entities on either side of a point-to-point link, and are unobservable and have no meaning outside WIS entities.

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50.1.3 Relationship to other sublayers

Figure 50–1 depicts the relationships among the WIS (shown shaded), the 10 Gb/s MAC and Reconciliation Sublayers, the 10GBASE-R PCS and PMA, the ISO/IEC 8802-2 LLC, and the ISO/IEC Open System Interconnection (OSI) reference model.

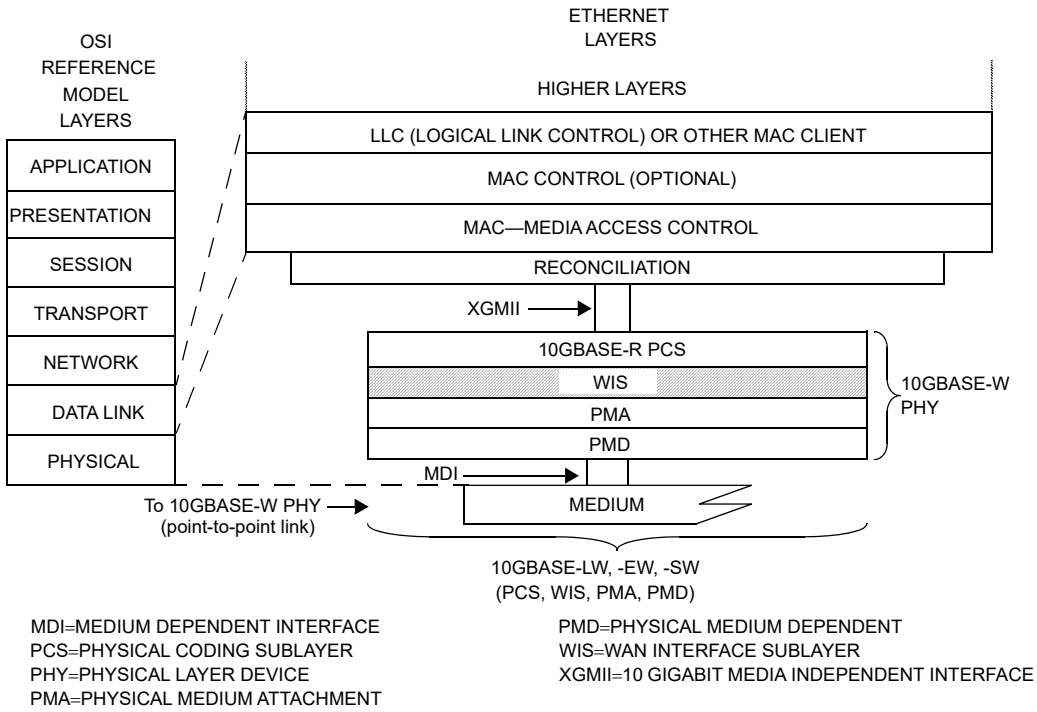

Figure 50–1—WIS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

50.1.4 Summary of functions

The following provides a summary of the principal functions implemented by the WIS.

In the transmit direction (i.e., when transferring data from the PCS to the PMA), the WIS performs the following functions:

a) Mapping of data-units received from the PCS via the WIS Service Interface to the payload capacity of the Synchronous Payload Envelope (SPE) defined for STS-192c
b) Addition of Path Overhead and fixed stuff octets to generate the actual SPE
c) Creation of frames consisting of Line Overhead and Section Overhead octets plus the SPE, and the generation and insertion of Section, Line, and Path Bit Interleaved Parity (BIP)
d) Scrambling of the generated WIS frames
e) Transmission of these frames to the PMA sublayer via the PMA Service Interface

In the receive direction, the functions performed by the WIS include the following:

f) Reception of data from the PMA sublayer via the PMA Service Interface
g) Delineation of octet boundaries as well as STS-192c frame boundaries within the unaligned data stream from the PMA
h) Descrambling of the payload and overhead fields within the incoming frames

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i) Processing of the pointer field within the Line Overhead, and delineation of the boundaries of the Synchronous Payload Envelopes (SPE) within the received WIS frames
j) Generation and checking of Bit Interleaved Parity (BIP) within the Section, Line, and Path Overheads
k) Removal of Line, Section, and Path Overhead columns, as well as fixed stuff columns, in order to extract the actual payload field
l) Handling of errors and exception conditions detected within the incoming WIS frame stream, and reporting these errors to Layer Management
m) Mapping of octets extracted from the payload capacity of the incoming SPE to data-units that are passed to the PCS via the WIS Service Interface

50.1.5 Sublayer interfaces

A WIS Service Interface is provided to allow the WIS to transfer information to and from the 10GBASE-R PCS, which is the sole WIS client. An abstract service model is used to define the operation of this interface. In addition, the WIS utilizes the service interface provided by the PMA sublayer to transfer information to and from the PMA. This standard defines these interfaces in terms of bits, octets, data-units and signals; however, implementers may choose other data-path widths and other control mechanisms for implementation convenience, provided that the logical models of the service interfaces are adhered to.

NOTE—The PMA service interface may be optionally instantiated as an actual physical interface, referred to as the XSBI; in this case, the WIS also implements the client portion of the XSBI, as defined in 51.4, and conform to its data-path widths and control mechanisms.

50.1.6 Functional block diagram

Figure 50–2 provides a functional block diagram of the WIS.

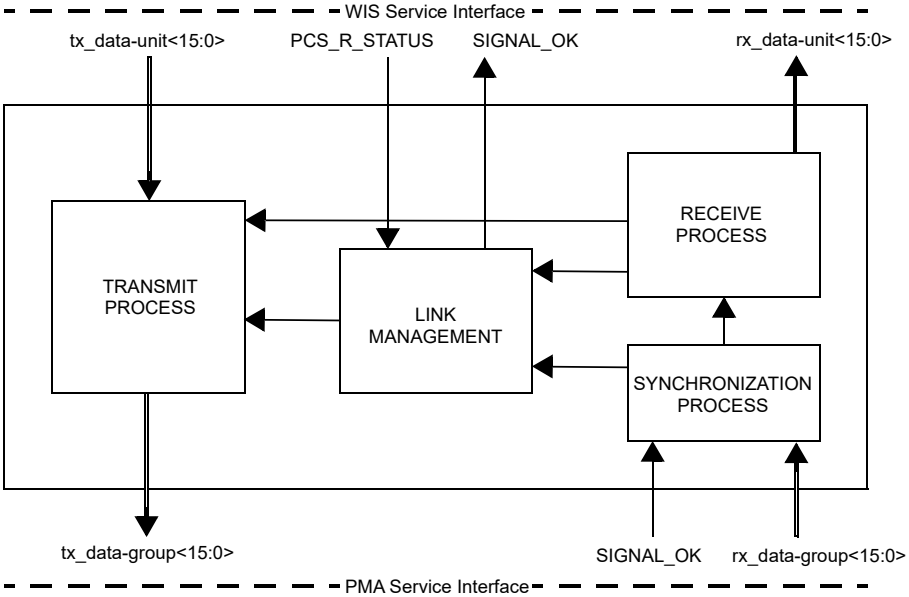

Figure 50–2—Functional block diagram

50.1.7 Notational conventions

The state diagrams within the body of this clause follow the notations and conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2.

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The Path, Line, and Section Overhead fields handled by the WIS are referenced using the standard terminology given in Section 4.2 of ATIS-0600416.1999(R2010). Nomenclature relating to SONET Defects and Anomalies that have to be processed by the WIS, as well as other definitions and abbreviations required by this clause, are defined by Section 3 of ATIS-0600416.1999(R2010).

The labeling and transmission order of bits within an octet is different between the SONET/SDH and Ethernet protocol families. SONET numbers bits within an octet from 1 to 8 inclusive, with the bit labeled 1 being the most-significant bit (MSB) and the bit labeled 8 being the least-significant bit (LSB); when serialized, bits are transmitted in order from MSB to LSB (i.e., the bit numbered 1 is transmitted first and the bit numbered 8 is transmitted last). The Ethernet numbering scheme, on the other hand, normally numbers bits from 0 to 7 inclusive, with bit 0 being the LSB and bit 7 being the MSB; bits are transmitted from LSB to MSB. This clause employs the SONET numbering scheme throughout, with the exception of the WIS service interface, which utilizes the Ethernet numbering scheme. Special provisions are made when mapping payload data into the WIS frame (see 50.3.1.1 and 50.3.1.2) to ensure that the reversed transmission order does not impact the properties of the Ethernet FCS.

50.2 WIS Service Interface

The WIS Service Interface is provided to allow the 10GBASE-R PCS to transfer information to and from the WIS. These services are defined in an abstract manner and do not imply any particular implementation. The WIS Service Interface supports the exchange of data-units between PCS entities on either side of a 10GBASE-W link using request and indicate primitives. Data-units are mapped into WIS frames by the WIS and passed to the PMA, and vice versa.

The following primitives are defined within the WIS Service Interface:

WIS_UNITDATA.request(tx_data-unit<15:0>)
WIS_UNITDATA.indication(rx_data-unit<15:0>)
WIS_SIGNAL.request(PCS_R_STATUS)
WIS_SIGNAL.indication(SIGNAL_OK)

50.2.1 WIS_UNITDATA.request

This primitive defines the transfer of data, in the form of constant-width data-units, from the PCS to the WIS. The data supplied via WIS_UNITDATA.request is mapped by the WIS Transmit process into the payload capacity of the outgoing WIS frame stream.

50.2.1.1 Semantics of the service primitive

WIS_UNITDATA.request(tx_data-unit<15:0>)

The data conveyed by WIS_UNITDATA.request is a 16-bit vector representing a single data-unit which has been prepared for transmission by the 10GBASE-R PCS Transmit process. The element tx_data-unit<0> shall be interpreted as the least significant bit of the vector, and tx_data-unit<7:0> shall be interpreted as the least significant octet of the vector. The least significant octet of the vector is assumed to be generated first by the PCS; when the WIS transfers the provided data to the PMA, it is mapped such that the least significant octet is also transmitted first.

50.2.1.2 When generated

The 10GBASE-R PCS sends tx_data-unit<15:0> to the WIS at a nominal rate of 599.04 Mtransfers/s, corresponding to the STS-192c payload rate of 9.58464 Gb/s.

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NOTE—The mapping of a constant-rate data stream into the payload capacity of a SONET-compatible SPE may require buffering in order to absorb the effects of periodically inserting overhead fields. In addition, the WIS and PCS may require some form of clock synchronization between the data-unit generation process and the normal SONET framing process. Both of these mechanisms are considered to be implementation-specific and outside the scope of this standard.

50.2.1.3 Effect of receipt

Upon receipt of this primitive, the WIS Transmit process maps the data conveyed by the tx_data-unit<15:0> parameter into the payload of the transmitted WIS frame stream, adds overhead octets as necessary, scrambles the data, and transfers the result to the PMA via one or more PMA_UNITDATA.request primitives.

50.2.2 WIS_UNITDATA.indication

This primitive defines the transfer of received data, in the form of constant-width data-units, from the WIS to the PCS. WIS_UNITDATA.indication is generated by the WIS Receive process in response to WIS frame data received from the PMA.

50.2.2.1 Semantics of the service primitive

WIS_UNITDATA.indication(rx_data-unit<15:0>)

The rx_data-unit<15:0> parameter is a 16-bit vector that represents the data-unit transferred by the WIS to the 10GBASE-R PCS. The element rx_data-unit<0> shall be interpreted as the least significant bit of the vector, and rx_data-unit<7:0> shall be interpreted as the least significant octet of the vector. The least significant octet of the vector is assumed to be processed first by the PCS; when the WIS obtains the data from the PMA, it is mapped such that the least significant octet was also received first.

50.2.2.2 When generated

The WIS sends one rx_data-unit<15:0> to the 10GBASE-R PCS whenever it has delineated exactly 16 bits of valid payload information from the incoming data stream received from the PMA sublayer. The nominal rate of generation of the WIS_UNITDATA.indication primitive is 599.04 Mtransfers/s, as governed by the recovered bit clock and the reduction in data rate imposed by the removal and discard of overhead fields from the incoming WIS frame stream. This corresponds to the STS-192c payload rate of 9.58464 Gb/s.

NOTE—The removal of overhead fields creates variations in data rate that may have to be removed by suitable buffering before data are transferred to the PCS. These buffering and rate adaptation mechanisms are implementation dependent and outside the scope of this standard.

50.2.2.3 Effect of receipt

The effect of receipt of this primitive by the WIS client is unspecified by the WIS.

50.2.3 WIS_SIGNAL.request

This primitive is sent by the 10GBASE-R PCS to the WIS to indicate when the PCS has acquired or lost frame delineation, i.e., synchronization with respect to the codewords present in the received data transferred from the WIS to the PCS.

50.2.3.1 Semantics of the service primitive

WIS_SIGNAL.request(PCS_R_STATUS)

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The PCS_R_STATUS parameter can take one of two values: OK or FAIL. A value of OK denotes that the PCS is successfully delineating valid codewords from the incoming data stream transferred to it by the WIS via the WIS_UNITDATA.indication primitive. A value of FAIL denotes that errors have been detected by the PCS that prevent synchronization to these codewords.

50.2.3.2 When generated

The 10GBASE-R PCS generates the WIS_SIGNAL.request primitive to the WIS whenever there is a change in the value of the PCS_R_STATUS parameter.

50.2.3.3 Effect of receipt

The receipt of this primitive causes the WIS to identify the presence or absence of a Loss of Code-group Delineation condition, and to report this condition to the remote WIS entity via an LCD-P defect indication, as described in 50.3.5.3.

50.2.4 WIS_SIGNAL.indication

This primitive is sent by the WIS to the PCS to indicate the status of the Receive process. WIS_SIGNAL.indication is generated by the WIS Receive process in order to propagate the detection of severe error conditions (e.g., no valid signal being received from the PMA sublayer) to the PCS.

50.2.4.1 Semantics of the service primitive

WIS_SIGNAL.indication(SIGNAL_OK)

The SIGNAL_OK parameter can take one of two values: OK or FAIL. A value of OK denotes that the WIS Receive process is successfully delineating valid payload information from the incoming data stream received from the PMA sublayer, and this payload information is being presented to the PCS via the WIS_UNITDATA.indication primitive. A value of FAIL denotes that errors have been detected by the Receive process that prevent valid data from being presented to the PCS, as described in 50.3.5; in this case the WIS_UNITDATA.indication primitive and its associated rx_data-unit<15:0> parameter are meaningless.

50.2.4.2 When generated

The WIS generates the WIS_SIGNAL.indication primitive to the 10GBASE-R PCS whenever there is a change in the value of the SIGNAL_OK parameter.

50.2.4.3 Effect of receipt

The effect of receipt of this primitive by the WIS client is unspecified by the WIS.

50.3 Functions within the WIS

As shown in Figure 50–2, the WIS comprises the WIS Transmit and WIS Receive processes for 10GBASE-W, together with a Synchronization process and a Link Management function. Figure 50–3 depicts a conceptual view of the functions within each of the Transmit and Receive processes. Note that the figure does not show the interfaces to the Link Management function.

The WIS Transmit process accepts fixed-width tx_data-units from the PCS via the WIS Service Interface, and maps them into the payload capacity of the transmitted WIS frame stream. Fixed stuff octets are added, together with a set of Path Overhead octets, to create a Synchronous Payload Envelope (SPE). Line and Section Overhead octets are combined with the SPE and then scrambled using a frame-synchronous

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scrambler to produce the final transmitted WIS frame. The WIS continuously generates one SONET-compatible WIS frame, comprising overhead fields, fixed stuff and payload, every 125 microseconds. No gaps are present between WIS frames. The data produced by the Transmit process, depicted as tx_data-group<15:0> in Figure 50–2, are passed to the PMA via the PMA Service Interface.

The WIS Synchronization process accepts data from the PMA (via the PMA Service Interface, depicted as rx_data-group<15:0> in Figure 50–2) and performs an alignment operation to delineate both octet and frame boundaries within the received data stream. Aligned and framed data are passed to the WIS Receive process (depicted as sync_bits<15:0> in Figure 50–3), where Section and Line Overhead octets are extracted from the WIS frames and processed after de-scrambling the frame data. The payload pointer within the Line Overhead is used to delineate the start and end of the received SPE, and the Path Overhead is extracted from the SPE and processed. Finally, the fixed stuff is removed from the SPE as well, and the resulting data stream is conveyed to the PCS via the WIS Service Interface. Severe errors detected by the Synchronization and Receive processes (e.g., loss of WIS frame synchronization) cause a WIS_SIGNAL.indication primitive to be sent to the PCS with a parameter of FAIL (see 50.2.4).

The WIS Link Management function implements the management registers defined in 45.2.2. These registers allow the local Station Management entity to control and monitor the operational status of the WIS Transmit and Receive processes. In addition, SONET Defects and Anomalies detected during the processing of the incoming data are sent to the management registers for reporting.

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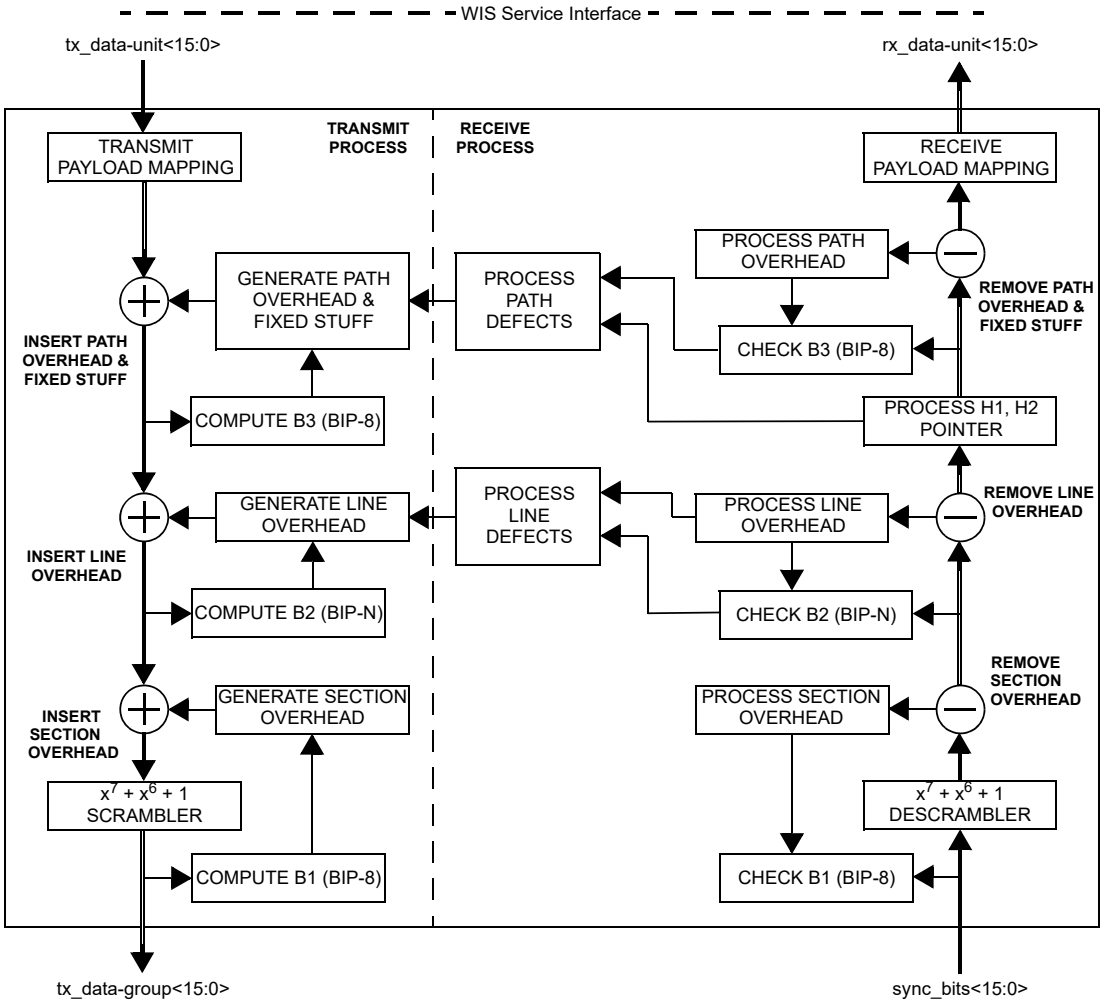

Figure 50–3—WIS Transmit and Receive processes

50.3.1 Payload mapping and data-unit delineation

The WIS maps the tx_data-unit<15:0> and rx_data-unit<15:0> parameters that are transferred via its service interface to/from the payload capacity of a standard STS-192c Synchronous Payload Envelope (SPE) structure. This structure is shown in Figure 50–4 for illustrative purposes. It is represented as a two-dimensional array with 9 rows and 16 704 columns, each row consisting of one octet of Path Overhead (added and removed as per 50.3.2.1 and 50.3.2.4), 63 octets of fixed stuff, and 16 640 octets of actual payload capacity.

The total payload capacity of the SPE comprises 149 760 octets (per WIS frame). As depicted in Figure 50–4, the octets of the payload capacity are numbered from left to right, starting at 0 (zero). The transmission order is also from left to right, i.e., lower-numbered octets are transmitted before higher-numbered octets.

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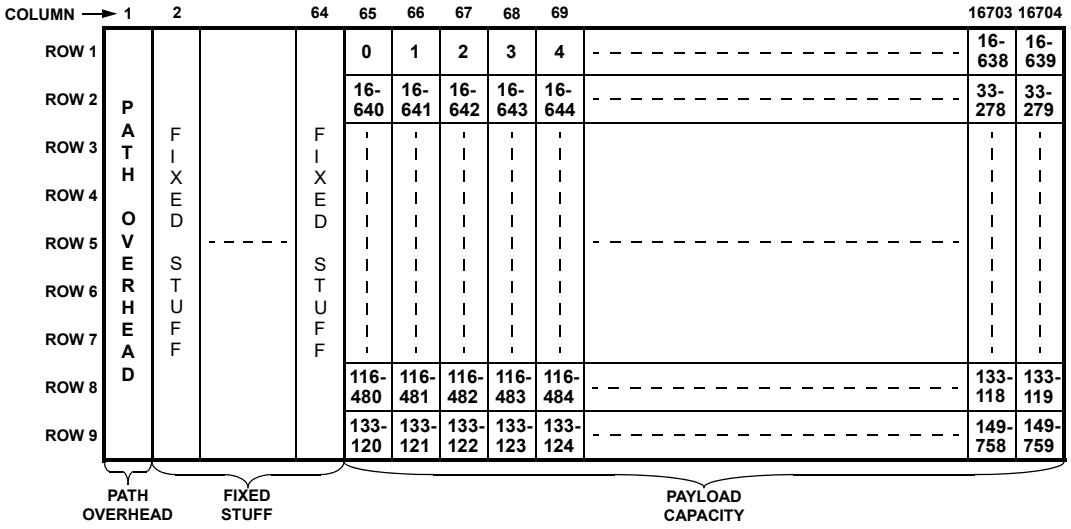

Figure 50–4—Structure of Synchronous Payload Envelope (illustrative)

50.3.1.1 Transmit payload mapping

The WIS Transmit function accepts a continuous stream of data-units from the PCS, conveyed by the tx_data-unit<15:0> parameter of the WIS_UNITDATA.request primitive of the WIS Service Interface. These data units shall be mapped to the SPE payload capacity and passed to the frame generation process described in 50.3.2 for insertion of the fixed stuff and Path Overhead columns. For each data-unit, tx_data-unit<7:0> shall be mapped to a lower-numbered (even) octet in the SPE payload capacity, and tx_data-unit<15:8> shall be mapped to the next higher-numbered (odd) octet.

A bit relabeling function is performed to map the bit numbering and ordering conventions followed by the WIS Service Interface to those implemented by the Transmit process (which follows the bit numbering and ordering conventions of SONET/SDH). The relabeling function shall be performed as shown in Figure 50–5. Bit 0 of tx_data-unit<15:0> is renumbered as bit 1 of the lower-numbered (even) octet within the SONET SPE, bit 15 of tx_data-unit<15:0> is renumbered as bit 8 of the higher-numbered octet within the SONET SPE, and the rest of the bits are renumbered in corresponding sequence.

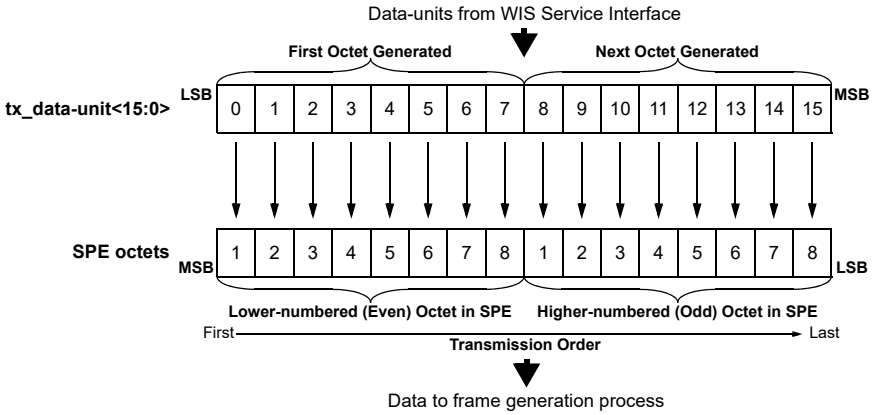

Figure 50–5—Transmit bit relabeling function

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NOTE—The transmit bit relabeling function is required because SONET transmission order is from MSB to LSB (i.e., bit 1 to bit 8 of each octet, in the SONET numbering convention) while the Ethernet transmission order is from LSB to MSB (i.e., bit 0 to bit 7 of each octet, in the Ethernet numbering convention). It is necessary to maintain the expected transmission order of Ethernet in order to preserve the error detection properties of the Ethernet FCS. Therefore, the renumbering scheme causes the payload portion of the SPE to be transmitted from LSB to MSB with reference to incoming data accepted from the WIS Service Interface, but the Path, Line, and Section Overhead octets are transmitted from MSB to LSB as required by SONET.

50.3.1.2 Receive payload mapping

The WIS Receive function accepts a continuous stream of octets from the frame reception process described in 50.3.2, corresponding to the payload capacity of the SPE as illustrated in Figure 50–4. It shall map the octets in the SPE payload capacity to a continuous stream of data-units that are supplied to the PCS via the rx_data-unit<15:0> parameter of the WIS_UNITDATA.indication primitive of the WIS Service Interface. Within each data-unit, rx_data-unit<7:0> shall be mapped to a lower-numbered (even) octet in the SPE payload capacity, and rx_data-unit<15:8> shall be mapped to the next higher-numbered (odd) octet.

A bit relabeling function is performed to map the bit numbering and ordering conventions followed by the Receive process (which follows the bit numbering and ordering conventions of SONET/SDH) to those required by the WIS Service Interface. The relabeling function shall be performed as shown in Figure 50–6. Bit 1 of the lower-numbered (even) octet within the received SONET SPE is renumbered as bit 0 of rx_data-unit<15:0> at the WIS Service Interface, bit 8 of the higher-numbered octet within the SONET SPE is renumbered as bit 15 of rx_data-unit<15:0>, and the rest of the bits are renumbered in corresponding sequence.

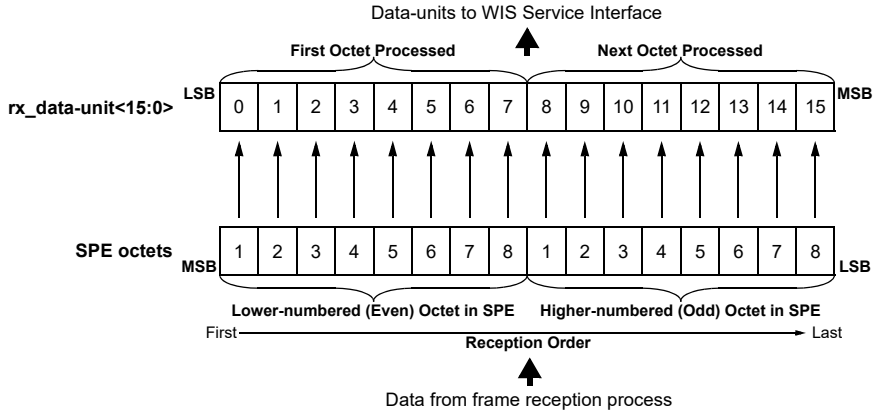

Figure 50–6—Receive bit relabeling function

NOTE—The receive bit relabeling function is required for the same reasons as the transmit bit relabeling function described in 50.3.1.1, i.e., to preserve the error detection properties of the Ethernet FCS in the face of the different transmission order required by SONET framing.

50.3.2 WIS frame generation

As part of the Transmit process, the WIS encapsulates the payload generated by the payload mapping function within a series of WIS frames. The Receive process performs the reverse operation, extracting payload from the incoming WIS frame stream and submitting it to the payload mapping function. SONET compatibility in the WIS follows ATIS-0600416.1999(R2010), with the exception of the superseding specifications in this document.

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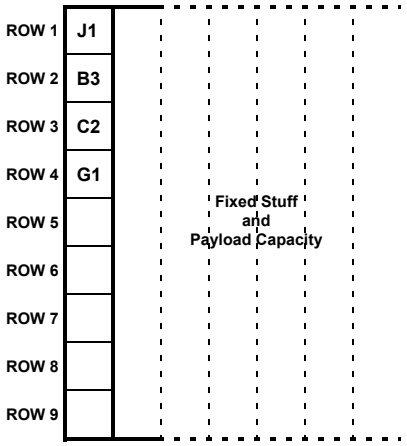
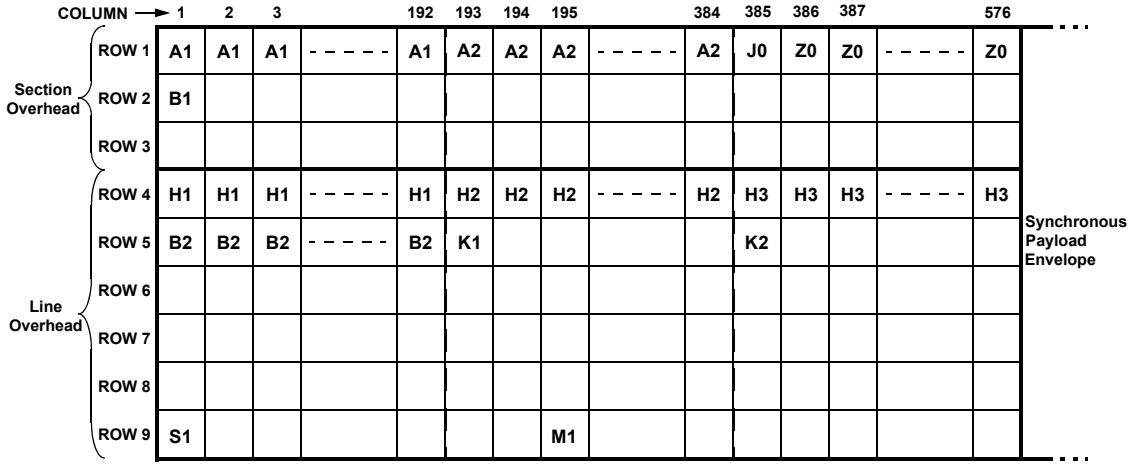
Frame generation in both the transmit and receive directions is performed in three stages. Figure 50–3 illustrates the sequence of stages. The relevant octets in the Path Overhead portion of the frame are shown in Figure 50–7, and Figure 50–8 illustrates the Section and Line Overhead generated by the WIS.



NOTE—The Path Overhead comprises 9 octets in total. Only 4 octets are defined for the WIS.
Octets that are undefined and unused by the WIS are indicated as blank boxes in this figure.

Figure 50–7—Structure of Path Overhead Generated by WIS (illustrative)



NOTE—The Section and Line Overhead comprise 5184 octets in total (576 x 9). Only 1349 octets are defined for the WIS.
Octets that are undefined and unused by the WIS are indicated as blank boxes in this figure.

Figure 50–8—Structure of Section and Line Overhead Generated by WIS (illustrative)

NOTE—Figures 50–8 and 50–7 are provided for illustrative purposes only. In the event of any discrepancy observed between the figures and the normative portions of ATIS-0600416.1999(R2010), the latter takes precedence.

50.3.2.1 Transmit Path Overhead insertion

The WIS Transmit process shall insert Path Overhead fields as defined in Section 4.2 of ATIS-0600416.1999(R2010), and specified in Table 50–1 of this standard. For the fields where the "Coding" column of Table 50–1 contains "per 416," the field is inserted according to the specifications of ATIS-0600416.1999(R2010). For the fields where the "Coding" column of Table 50–1 contains a specific value or "see text," this document supersedes the corresponding values in Table 1, "SONET overhead at NIs" in the ATIS document.

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Table 50–1—STS Path Overhead

Overhead octet	Function	Usage	Coding (bits 1..8)
B3	STS Path error monitoring (Path BIP-8)	supported	per 416
C2	STS Path signal label	specified value	00011010
F2	Path user channel	unsupported	00000000
G1	Path status	supported	per 416
H4	Multiframe indicator	unsupported	00000000
J1	STS Path trace	specified value	see text
N1	Tandem connection maintenance/Path data channel	unsupported	00000000
Z3-Z4	Reserved for Path growth	unsupported	00000000
NOTE—SONET/SDH and IEEE 802.3 differ in bit ordering conventions. The values in this table follow SONET bit ordering, in which bit index values range from 1 to 8, from left to right, and bit 8 is the least significant bit.			

NOTE—The value assigned to the C2 octet corresponds to the provisional Path signal label value assigned for 10 Gigabit Ethernet. The fixed stuff octets that follow the Path Overhead column in the SPE are transmitted as 00000000 and are not checked on receive.

The J1 octet shall transport a 16-octet continuously repeating Path Trace Message that is formatted as defined by Section 5 and Annex A of ATIS-0300269.2006(S2016). Each successive octet of the Path Trace Message, starting from the first, is placed in the J1 octet of a successive WIS frame; after all 16 octets have been transmitted in this way, the process repeats. The Station Management entity may modify the Path Trace Message being transmitted via the Link Management register facilities provided in 50.3.11.1. If the Station Management entity is not currently transmitting a Path Trace Message, a default Path Trace Message consisting of 15 octets of zeros and a header octet formatted according to Section 5 of ATIS-0300269.2006(S2016) shall be transmitted.

NOTE—The bit representation of the header octet of the default Path Trace Message is 10001001 (89 hexadecimal). This value is provided here for informational purposes only; ATIS-0300269.2006(S2016) takes precedence in case of any discrepancy.

50.3.2.2 Transmit Line Overhead insertion

The WIS Transmit process shall insert Line Overhead fields as defined in Section 4.2 of ATIS-0600416.1999(R2010), and specified in Table 50–2 of this document. For the fields where the “Coding” column of Table 50–2 contains “per 416,” the field is inserted according to the specifications of ATIS-0600416.1999(R2010). For the fields where the “Coding” column of Table 50–2 contains a specific value or “see text,” this document supersedes the corresponding values in Table 1, “SONET overhead at NIs” in the ATIS document. In addition, Line Overhead octets not listed in the latter table shall be set to 00000000 by the Transmit process.

The H1 and H2 pointer octets shall be set by the Transmit process, in accordance with the pointer mechanism defined by ATIS-0600416.1999(R2010), to indicate a constant pointer value of 522 decimal, and shall also indicate a concatenated payload.

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The K1 octet shall be set to 00000000 by the Transmit process. In addition, bits 1 to 5 inclusive of the K2 octet shall be set to 00000 binary. Bits 6 through 8 inclusive shall either transport an RDI-L encoding, as defined by Section 7.4.1 of ATIS-0600416.1999(R2010), or be set to 000 binary. No other encodings of the K2 octet are allowed to be transmitted by the WIS Transmit process.

Table 50–2—Line Overhead

Overhead octet	Function	Usage	Coding (bits 1..8)
B2	Line error monitoring (Line BIP-1536)	supported	per 416
D4-D12	Line Data Communications Channel (DCC)	unsupported	00000000
E2	Orderwire	unsupported	00000000
H1-H2	Pointer	specified value	See text.
H3	Pointer action	specified value	00000000
K1, K2	Automatic protection switch (APS) channel and Line Remote Defect Identifier (RDI-L)	specified value	See text.
M0	STS-1 Line Remote Error Indication (REI)	unsupported	00000000
M1	STS-*N* Line Remote Error Indication (REI)	supported	per 416
S1	Synchronization messaging	unsupported	00001111
Z1	Reserved for Line growth	unsupported	00000000
Z2	Reserved for Line growth	unsupported	00000000
NOTE—SONET/SDH and IEEE 802.3 differ in bit ordering conventions. The values in this table follow SONET bit ordering, in which bit index values range from 1 to 8, from left to right, and bit 8 is the least significant bit.			

NOTE—The setting of the constant portions of the K1 and K2 octets denotes that the interface containing the WIS is acting as a working channel. The RDI-L encoding within the K2 octet serves to support the fault processing specified in 50.3.2.5. The setting of the S1 octet signifies that the transmit clock should not be used for synchronization. The bit numbering for these octets follows the SONET convention, in which bit index values range from 1 to 8, from left to right, and bit 8 is the least significant bit.

50.3.2.3 Transmit Section Overhead insertion

The WIS Transmit process shall insert Section Overhead fields as defined in Section 4.2 of ATIS-0600416.1999(R2010), and specified in Table 50–3 of this document. For the fields where the “Coding” column of Table 50–3 contains “per 416,” the field is inserted according to the specifications of ATIS-0600416.1999(R2010). For the fields where the “Coding” column of Table 50–3 contains a specific value or “see text,” this document supersedes the corresponding values in Table 1, “SONET overhead at NIs” in the ATIS document. In addition, Section Overhead octets not listed in the latter table shall be set to 00000000 by the Transmit process.

The J0 octet shall transport a 16-octet continuously repeating Section Trace Message that is formatted as defined by Section 5 and Annex A of ATIS-0300269.2006(S2016). Each successive octet of the Section Trace Message, starting from the first, is placed in the J0 octet of a successive WIS frame; after all 16 octets

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have been transmitted in this way, the process repeats. The Station Management entity may modify the Section Trace Message being transmitted via the Link Management register facilities provided in 50.3.11.1. If the Station Management entity is not currently transmitting a Section Trace Message, a default Section Trace Message consisting of 15 octets of zeros and a header octet formatted according to Section 5 of ATIS-0300269.2006(S2016) shall be transmitted.

NOTE—The bit representation of the header octet of the default Section Trace Message is 10001001 (89 hexadecimal). This value is provided here for informational purposes only; ATIS-0300269.2006(S2016) takes precedence in case of any discrepancy.

Table 50–3—Section Overhead

Overhead octet	Function	Usage	Coding (bits 1..8)
A1	Frame alignment	supported	per 416
A2	Frame alignment	supported	per 416
B1	Section error monitoring (Section BIP-8)	supported	per 416
D1-D3	Section Data Communications Channel (DCC)	unsupported	00000000
E1	Orderwire	unsupported	00000000
F1	Section User Channel	unsupported	00000000
J0	Section trace	specified value	See text
Z0	Reserved for Section growth	unsupported	11001100
NOTE 1—The bit representations of the octet values assigned to A1 and A2 are 11110110 (F6 hexadecimal) and 00101000 (28 hexadecimal), respectively. These values are provided here for informational purposes only. ATIS-0600416.1999(R2010) takes precedence in case of any discrepancy. NOTE 2—SONET/SDH and IEEE 802.3 differ in bit ordering conventions. The values in this table follow SONET bit ordering, in which bit index values range from 1 to 8, from left to right, and bit 8 is the least significant bit.			

50.3.2.4 Receive Path, Line, and Section Overhead extraction

The WIS Receive process shall extract Path, Line and Section Overhead fields as defined in Section 4.2 of ATIS-0600416.1999(R2010), and specified in Table 50–1, Table 50–2, and Table 50–3 of this document. For the fields where the “Coding” columns of Table 50–1, Table 50–2, and Table 50–3 contain “per 416,” the field is extracted according to the specifications of ATIS-0600416.1999(R2010). For the fields where the “Coding” columns contain a specific value or “see text,” this document supersedes the corresponding values in Table 1, “SONET overhead at NIs” in the ATIS document. Overhead octets marked as unsupported in Table 50–1, Table 50–2, and Table 50–3 shall be ignored by the Receive process. In addition, overhead octets not listed in Table 1, “SONET overhead at NIs” in ATIS-0600416.1999(R2010) shall also be ignored by the Receive process.

The J0 octet in the received WIS frames shall be interpreted as transporting a 16-octet continuously repeating Section Trace Message. This Section Trace Message is extracted from the incoming WIS frame stream and passed to the Station Management entity via dedicated registers within the WIS MDIO register space (50.3.11.1). The WIS Receive process is not required to delineate Section Trace Message boundaries or process them in any way.

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Extraction of valid Section Trace Message data shall begin after the WIS Receive process has successfully synchronized to the incoming WIS frame stream. Each successive J0 octet received thereafter is placed in a successive octet of the WIS J0 receive register set, until 16 J0 octets have been received, after which the process repeats from the first octet of the register set. As the incoming Section Trace Message is 16 octets in size, the contents of the WIS J0 receive register set will remain static as long as the same message is being received. Extraction of Section Trace Messages in this fashion is performed continuously as long as valid WIS frames are being received. The WIS Receive process is not required to interpret or process the extracted message in any way.

The J1 octet in the received WIS frames shall be interpreted as transporting a 16-octet continuously repeating Path Trace Message. This Path Trace Message is extracted from the incoming WIS frame stream and passed to the Station Management entity via dedicated registers within the WIS MDIO register space (50.3.11.1). The WIS Receive process is not required to delineate Path Trace Message boundaries or process them in any way.

Extraction of valid Path Trace Message data shall begin after the WIS Receive process has successfully synchronized to the incoming WIS frame stream. Each successive J1 octet received thereafter is placed in a successive octet of the WIS J1 receive register set, until 16 J1 octets have been received, after which the process repeats from the first octet of the register set. As the incoming Path Trace Message is 16 octets in size, the contents of the WIS J1 receive register set will remain static as long as the same message is being received. Extraction of Path Trace Messages in this fashion is performed continuously as long as valid WIS frames are being received. The WIS Receive process is not required to interpret or process the extracted message in any way.

Bits 6 through 8, inclusive, of the K2 octet in the received Line Overhead shall be interpreted by the WIS Receive process as carrying the Line Alarm Indication Signal (AIS-L) or Line Remote Defect Indication (RDI-L) signals (see 50.3.2.5). All other encodings of these bits shall be ignored by the Receive process.

NOTE—Values of overhead fields encoded by the Transmit process within a WIS entity at one end of a link may be changed by intervening Line and Section equipment before it reaches the peer WIS entity at the other end of the link. In particular, the H1, H2, and H3 fields may take on values different from those originally encoded. The receive process handles these situations in accordance with ATIS-0600416.1999(R2010), and therefore contains a pointer interpreter function compliant with the latter. Bits 5 and 6 of the H1 octet are ignored by the receiver.

50.3.2.5 Fault processing

Defects and anomalies detected by the Receive process are classified as defined in Section 7.1 of ATIS-0600416.1999(R2010). Section, Line, and Path defects and anomalies listed in Table 50–4 of this document shall be detected and processed as defined by Sections 7.3, 7.4.1, and 7.5 of ATIS-0600416.1999(R2010). Defects and anomalies not listed in Table 50–4 are ignored.

NOTE—The description of the LOP-P defect in Section 7.5 of ATIS-0600416.1999(R2010) is in error, and deviates from the underlying definitive reference, which is ANSI T1.231-1997. The reader should therefore consult section 8.1.2.4.1 of ANSI T1.231-1997 for the specification of the LOP-P defect until ATIS-0600416.1999(R2010) has been corrected.

The WIS shall additionally support the PLM-P (Path Label Mismatch) and LCD-P (Loss of Code-group Delineation) defects. The detection and reporting of the PLM-P defect follows Section 7.5 of ATIS-0600416.1999(R2010). The LCD-P defect shares the same coding value and reporting method as the PLM-P defect, but is detected according to 50.3.5.3.

The Receive process shall detect a Loss Of Signal (LOS) defect as defined by Section 7.2.1 of ATIS-0600416.1999(R2010) without using any services provided by the PMA or PMD sublayers for this purpose. The parameters *T* and *T'* in Section 7.2.1 of ATIS-0600416.1999(R2010) shall both be set to a value ranging between 2.3 and 100 microseconds.

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Table 50–4—WIS supported Near end events and Far end reports

	Physical media	Section		Line		Path	
	Defect	Anomaly	Defect	Anomaly	Defect	Anomaly	Defect
Near end	LOS	BIP-N(S)	SEF/LOF	BIP-N(L)	AIS-L	BIP-N(P)	LOP-P AIS-P
Far end	N/A	N/A	N/A	REI-L	RDI-L	REI-P	ERDI-P

NOTE—Section 7.2.2, "VT1.5 rate–Electrical Interface," Section 7.4.2 "VT1.5 Rate," Section 7.6, "Performance and Failure Monitoring," and Section 7.7 "Performance Monitoring Functions" of ATIS-0600416.1999(R2010) are not applicable and are not supported. Also, the AIS-L defect is only processed and reported by the WIS Receive process; it is never transmitted by the WIS Transmit process. In addition, a PLM-P defect is indistinguishable from an LCD-P defect at the far end, as the two defects are coded identically in the outgoing WIS frame stream; however, as both defects indicate a payload defect, this is of no consequence. They are detected separately for local reporting purposes.

50.3.3 Scrambling

The WIS shall implement a frame-synchronous scrambler within the Transmit process, and shall also implement a frame-synchronous descrambler within the Receive processes, both of sequence length 127 and as specified by Section 10.3 of ATIS-0900105.2008. The use of the scrambler is intended to provide for DC balance (i.e., an equal number of 1's and 0's on average) and for sufficient transition density within the bit stream transmitted on the medium. The scrambler is run over each bit of the entire WIS frame prior to transmission to the PMA, with the exception of all the A1, A2, J0 and Z0 octets (576 octets in total, per WIS frame), which are transmitted and received unscrambled. The scrambling function implemented by the Transmit process is identical in logical construction to the corresponding descrambling function in the Receive process.

Figure 50–9 illustrates the functional diagram of the frame-synchronous scrambler, in bit-serial form.

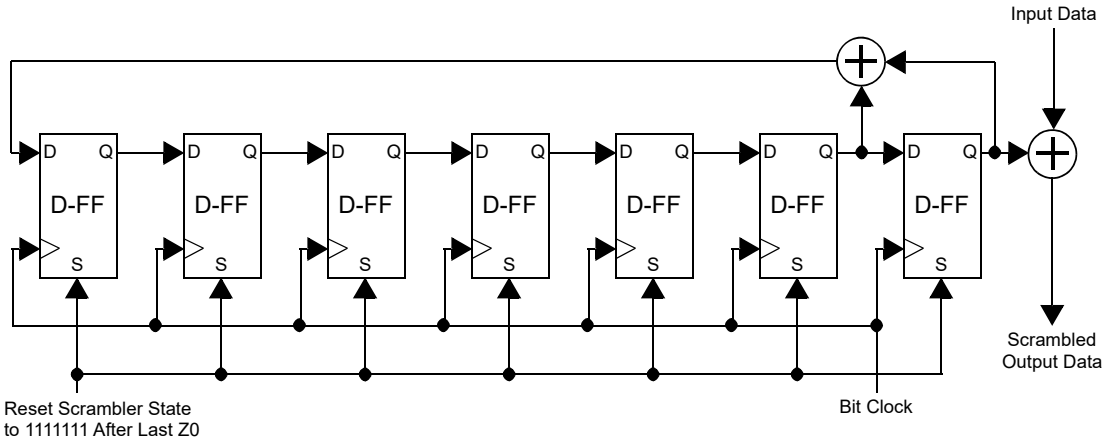

Figure 50–9—Scrambling function (illustrative)

NOTE—The diagram in Figure 50–9 is intended for reference and illustrative purposes only. Implementations may select any conforming means of realizing the scrambler function described herein. If a discrepancy is observed between the descriptions and diagram in this section and ATIS-0900105.2008, the latter takes precedence.

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50.3.3.1 Scrambler polynomial

The scrambler polynomial used follows that specified in Section 10.3 of ATIS-0900105.2008. The scrambler state is reset, as specified in the latter, to binary 1111111 prior to processing the octet immediately following the last Z0 octet in every WIS frame.

50.3.3.2 Scrambler bit ordering

The bit ordering considerations for the frame-synchronous scrambler in the WIS are illustrated in Figure 50–10. As shown, the scrambler in effect processes the transmitted (received) WIS frame octet-by-octet, starting with the most-significant (leftmost) bit of the first octet following the last Z0 octet in the WIS frame. The scrambler then proceeds bit-by-bit until the least-significant bit has been reached, after which it continues with the most-significant bit of the second octet.

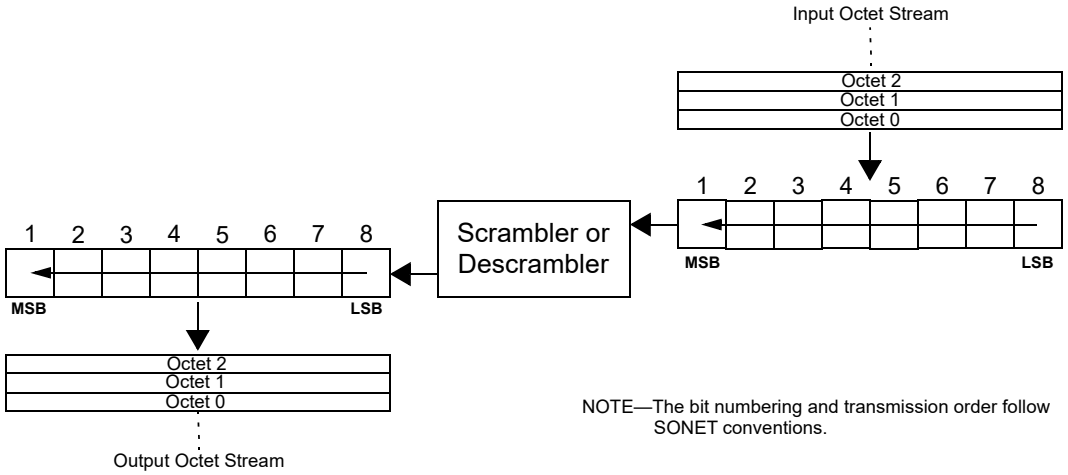

Figure 50–10—Scrambler bit ordering (illustrative)

NOTE—The above description and diagram are illustrative.

50.3.4 Octet and frame delineation

The WIS is required to delineate both octet and WIS frame boundaries within the stream of received data words presented by the PMA via its service interface to the Receive process. Delineation of these boundaries and alignment of the received data are done prior to performing the descrambling function (as opposed to the SPE delineation process, which is done after descrambling the received data). The delineation process employs the A1 and A2 octets in the Section Overhead portion of the received WIS frame stream, and searches for valid transitions between A1 and A2 patterns.

The WIS shall implement the synchronization process described in 50.4.2 to delineate octet and WIS frame boundaries. Failure to achieve or maintain synchronization shall result in Severely Errored Frame (SEF) or Loss Of Frame (LOF) Defects being indicated as described in 50.3.2.5.

50.3.5 Error propagation

The WIS Receive and Synchronization processes detect specific errors during reception that prevent delineation of valid data from the incoming WIS frame stream, and cause these errors to be propagated to the 10GBASE-R PCS. Error propagation shall be performed by generating a WIS_SIGNAL.indication primitive with the SIGNAL_OK parameter set to FAIL, regardless of the actual contents of any payload that may be extracted from the incoming WIS frame stream. A subsequent WIS_SIGNAL.indication primitive

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with SIGNAL_OK set to OK shall be issued only after the WIS determines that none of these particular errors exist, subject to the error propagation timing below.

In addition, the WIS Receive process detects a Loss of Code-group Delineation condition, and report it to the far end WIS as an LCD-P defect by the method described in 50.3.2.5.

50.3.5.1 Propagated errors

The following conditions shall be detected as errors and reported to the 10GBASE-R PCS via the mechanism of 50.3.5:

a) The Synchronization process is not in the SYNC state, as defined by the state diagram of 50.4.2.
b) A PLM-P defect is detected (50.3.2.5).
c) An AIS-P defect is detected (50.3.2.5).
d) An LOP-P defect is detected (50.3.2.5).

NOTE—The error propagation mechanism may also be used to indicate when the WIS is unable to supply valid data to the PCS for any other reason, such as an internal error, a reset condition, or when disabled via layer management. This is considered to be implementation specific and is outside the scope of this clause.

50.3.5.2 Error propagation timing

Propagation of errors to the PCS according to the mechanism of 50.3.5 begins as soon as possible after the detection of one or more of the error conditions specified in 50.3.5.1. Error propagation shall terminate, and valid data shall be transferred to the PCS, within 125 microseconds of the removal of all of the error conditions in 50.3.5.1.

50.3.5.3 Loss of Code-group Delineation

The WIS Receive process shall identify a Loss of Code-group Delineation condition if the 10GBASE-R PCS signals, via the WIS_SIGNAL.request(PCS_R_STATUS) primitive of the WIS Service Interface (50.2.3), that synchronization has been lost and valid code-groups are no longer being delineated from the received payload stream being passed to the PCS. The LCD-P defect shall be reported to the far end WIS if this condition persists continuously for at least 3 ms. In addition, re-initialization of the WIS shall cause the LCD-P defect to be reported, with the same timing specification, until the PCS signals that valid code-groups are being delineated. The 3 millisecond timer is not allowed to start timing the false condition of WIS_SIGNAL.request(PCS_R_STATUS) while WIS_SIGNAL.indication is false, thus inhibiting the reporting of the LCD-P defect whenever the WIS is unable to supply valid received data to the PCS.

The WIS Receive process shall identify the absence of a Loss of Code-group Delineation condition if the 10GBASE-R PCS signals, also via the WIS_SIGNAL.request(PCS_R_STATUS) primitive, that synchronization has been regained and valid code-groups are being delineated from the received payload stream. Reporting of the LCD-P defect to the far end WIS shall terminate if the condition has been absent continuously for at least 1 ms.

50.3.6 Mapping between WIS and PMA

As a client of the PMA sublayer, the WIS utilizes the PMA Service Interface to transfer transmitted (received) data-groups to (from) the PMA sublayer. The PMA Service Interface is described in 51.2. Note that the PMA Service Interface may optionally be instantiated as a physical interface, referred to as the XSBI. In this case, the WIS implements the client portion of the XSBI, including the logical formats and protocols as well as the physical signals and electrical timing, conforming with the XSBI specification in 51.4.

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The WIS Transmit process transfers a continuous stream of 16-bit data-groups, containing the transmit WIS frame data generated as in 50.3.2, to the PMA via the PMA Service Interface. The octet boundaries in the transmit WIS frames shall be aligned to those in the data-groups, and the first data-group transmitted shall contain the first two octets in the Section Overhead (i.e., the first two A1 octets, as illustrated in Figure 50–8). Figure 50–11 depicts the transmission order required from the PMA for the data-groups. Each 16-bit data-group shall be transmitted from left to right, with lower-numbered bits being transmitted before higher-numbered bits. The data-groups themselves shall be transmitted in the sequence in which they are presented to the PMA by the WIS Transmit process.

A similar ordering is required during the reception process, as shown in Figure 50–11. Successive received bits shall be ordered from left to right in the 16-bit data-groups that are passed to the WIS (i.e., lower-numbered bits are received before higher-numbered bits), and the data-groups have to be presented in the sequence in which they were received. The PMA sublayer is not required to align the data being presented to the WIS on any boundary.

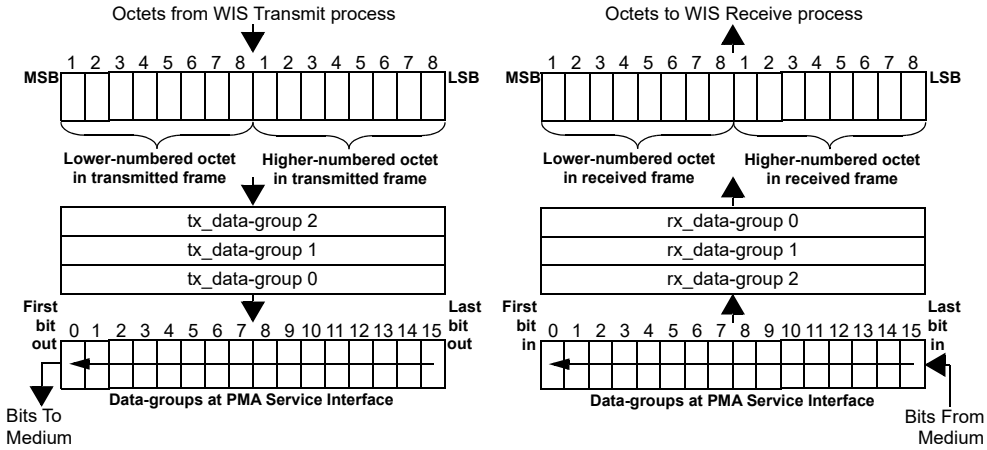

Figure 50–11—Transmission order

The WIS also utilizes the PMA_SIGNAL.indication primitive received from the PMA sublayer to determine when the PMA is unable to provide valid data to the WIS via its service interface. This primitive is used to unlock the state diagram implemented in the Synchronization process and force it to re-synchronize, as described in 50.4.

NOTE—The PMA_SIGNAL.indication primitive received from the PMA differs from the Loss of Signal (LOS) defect described in 50.3.2.5. LOS is a status condition that is reported to Layer Management for error monitoring purposes, but otherwise does not affect the internal functioning of the Receive Process or the Synchronization Process. The PMA primitive, however, acts as a control signal that directly affects all parts of the WIS receive functionality.

50.3.7 WIS data delay constraints

The sum of the transmit and receive data delays for any implementation of the WIS shall not exceed 14336 BT. Transmit data delay is measured from the input of a given unit of data by the PCS at the WIS service interface to the presentation of the same unit of data by the WIS to the PMA at the PMA service interface. Receive data delay is measured from the input of a given unit of data by the PMA at the PMA service interface to the presentation of the same unit of data by the WIS to the PCS at the WIS service interface. The time required to insert or process any necessary overhead or stuff octets has to be included as part of the data delay incurred by the WIS. No constraint is placed on the individual values of the transmit and receive data delays for a given implementation, provided their sum falls within the above limit.

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50.3.8 WIS test-pattern generator and checker

The WIS shall incorporate a test-pattern generator and a test-pattern checker to permit in-circuit testing using test patterns. These serial test patterns allow the 10GBASE-W PMA and PMD sublayers to be tested for compliance while in a system environment. Three patterns have been defined for testing: a fixed square wave pattern, an optional PRBS31 pattern, and a framed mixed frequency pattern. The patterns may be implemented at a bit or frame level and may be used for transmitter testing. The test-pattern checker has the ability to synchronize to the PRBS31 and mixed-frequency test patterns and report bit errors detected within the payload to the Station Management entity. The test-pattern checker is not required to synchronize to or analyze the square wave pattern.

The transmit and receive portions of the WIS can be placed in test-pattern mode separately by means of the WIS Transmit test-pattern enable and WIS Receive test-pattern enable control bits supported within its management registers (see 45.2.2.6). In addition, the three different types of transmit test pattern (square-wave, PRBS31 and mixed frequency) may be selected by means of the test-pattern control bits. (The test-pattern receiver only operates in PRBS31 and mixed-frequency test-pattern modes.) Errors detected during PRBS31 testing are recorded and provided to the Station Management entity via the 10G WIS test-pattern error counter register (45.2.2.8), while errors detected during mixed frequency testing are recorded and provided to the Station Management entity via the 10G WIS Section BIP Error Count register (45.2.2.17), the 10G WIS Line BIP Errors register (45.2.2.15), and the 10G WIS Path Block Error Count register (45.2.2.16). The WIS Service Interface is inoperative when either the WIS Transmit process or WIS Receive process is placed in test-pattern mode, regardless of the type of test pattern selected.

When the WIS transmit function is operating in test-pattern mode, the test-pattern generator produces a continuous test pattern that is sent 16 bits at a time to the underlying PMA sublayer via PMA_UNITDATA.request primitives. When the WIS receive function is operating in test-pattern mode, 16-bit data-groups received from the underlying PMA sublayer by means of PMA_UNITDATA.indication primitives are accepted and processed by the test-pattern checker.

50.3.8.1 Square wave test pattern

In the square-wave test-pattern mode, the WIS Transmit process is disabled or otherwise prevented from processing data, and a square wave as defined in 52.9.1 shall be continuously transferred to the PMA via the PMA Service Interface. No checking is performed on the 16-bit data-groups received from the PMA sublayer in this mode.

50.3.8.2 PRBS31 test pattern

The PRBS31 test-pattern mode is optional. When the transmit portion of the WIS is operating in PRBS31 test-pattern mode, the WIS Transmit process is disabled or otherwise prevented from processing data, and the output of a Pseudo-Random Bit Sequence (PRBS) generator shall be continuously transferred to the PMA via the PMA Service Interface. The PRBS generator functionality is described in 49.2.8.

When the receive portion of the WIS is operating in PRBS31 test-pattern mode, the WIS Receive Process is disabled or otherwise prevented from processing data, and a PRBS pattern checker shall check the bits received from the PMA via the PMA Service Interface. The PRBS checker functionality is described in 49.2.12.

If no errors have occurred, the test-pattern error signal from the pattern checker will be zero. An isolated bit error will cause the test-pattern error signal to be asserted three times; once when it is received and once when it is at each tap. The 10G WIS test-pattern error counter register (45.2.2.8) shall be incremented whenever the test-pattern error signal is asserted.

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50.3.8.3 Mixed-frequency test pattern

In the mixed-frequency test-pattern mode, the WIS Transmit process is utilized to generate a transmitted test pattern (if activated by the WIS Transmit test-pattern enable control bit) and the WIS Synchronization and Receive processes are utilized to check a received test pattern (if separately activated by the WIS Receive test-pattern enable control bit). Figure 50–12 provides a functional diagram of the WIS when operating in this mode.

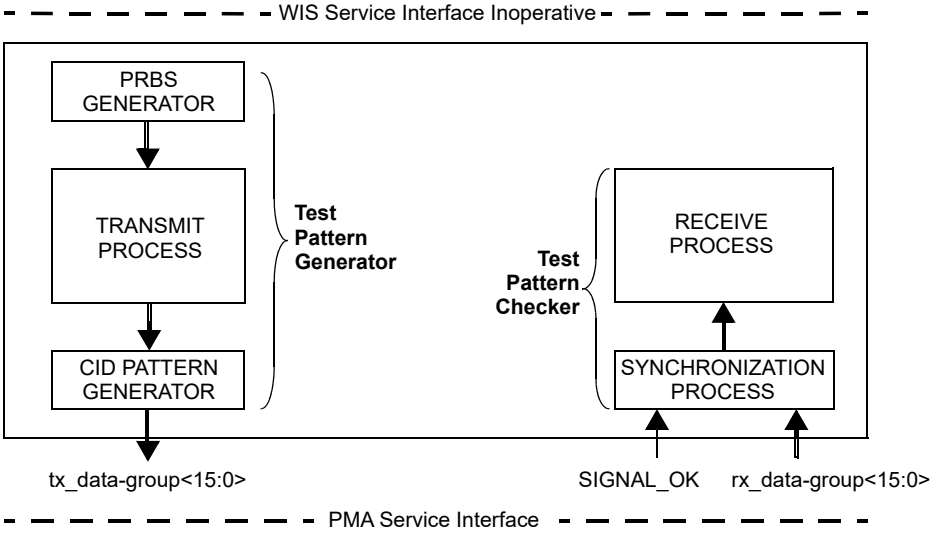

Figure 50–12—Mixed-frequency test-pattern mode operation

The mixed-frequency test pattern has the Test Signal Structure (TSS) described by 50.3.8.3.1, with a Consecutive Identical Digit (CID) pattern described by 50.3.8.3.2. The pattern is generated using the WIS Transmit process, with the SPE payload capacity being filled with a (2^{23}– 1) pseudo-random bit sequence (PRBS) as defined by ITU-T Recommendation O.150, 1996, in conjunction with a CID pattern generator that overwrites the last nine Z0 octets of the Section Overhead (see Figure 50–8) with an alternating pattern. The WIS Synchronization and Receive processes operate normally. Bit errors in the received pattern shall be detected by means of the Section, Line and Path BIP checking facilities, and reported to Station Management by means of the corresponding error counters within the MDIO register space (see 50.3.8).

NOTE 1—The PRBS is substituted for the payload data that would normally be sent to the WIS Transmit process from the 10GBASE-R PCS. The CID pattern is selected to stress the lock range of the receiver circuitry, and is placed in the Z0 octet locations as these are not scrambled by the WIS Transmit process. The values of the Z0 octets are required to be ignored by the WIS Receive process (see 50.3.2.4), and therefore no change to the latter is necessary.

The WIS Transmit, Receive and Synchronization processes shall function as described in 50.3.2, 50.3.3, and 50.3.4, with the exception that fault processing as per 50.3.2.5 and error propagation as per 50.3.5 shall not be carried out, the Z0 octets shall be overwritten with a CID pattern as specified, and the data output by the PRBS generator shall be used as the data source in place of the PCS.

NOTE 2—The implied re-use of the WIS Transmit, Receive, and Synchronization processes to implement the mixed-frequency test pattern functions is not a required attribute; implementations may select any physical means of realizing the test-pattern transmit and receive functionality, provided that the external behavior of the WIS conforms to that described herein.

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50.3.8.3.1 Test Signal Structure (TSS)

The TSS is defined as a repeating set of two consecutive WIS frames, i.e., 300 672 octets in length, and shall be formatted as shown in Figure 50–13. The first frame of the set has a CID pattern set to all zeros, and the second frame has the pattern set to all ones. The PRBS generator shall be reset to all ones prior to the start of the payload capacity of each SPE contained within the TSS. In addition, the PRBS generator output shall be placed directly into the payload capacity of the first SPE, and inverted before being placed into the second SPE. Both WIS frames include the Section, Line, and Path Overhead and fixed stuff as normally generated by the Transmit process. All overhead octets except for J1 shall be set to their default values.

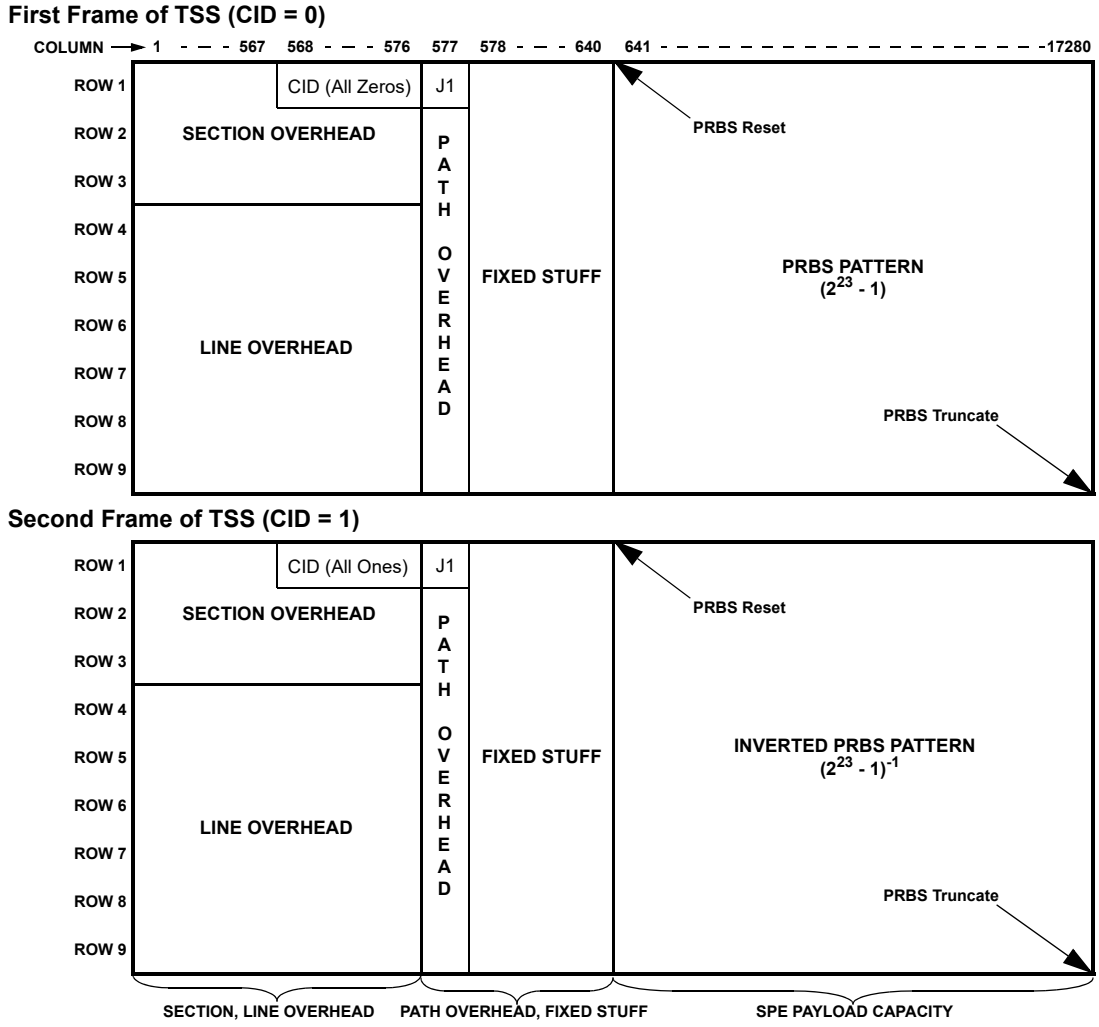

Figure 50–13—Test Signal Structure

As shown in Figure 50–13, the J1 octet of the Path Overhead is located immediately following the last octet of the CID pattern, and is hence the point of maximum stress with respect to the 10GBASE-W PMA and PMD. The J1 octet may therefore be programmed via the 10G WIS J1 transmit registers (45.2.2.12) to a fixed value that, after scrambling, provides optimal stress to the PMA/PMD transmitter and receiver. If not used for this purpose, it shall be set to a value of 89 hexadecimal in both the WIS frames comprising the TSS.

NOTE—Standard SONET test equipment may not support the WIS test-pattern generator and checker as the PRBS is re-synchronized on every WIS frame, instead of the free-running PRBS described in ITU-T Recommendation O.172. Pattern-based bit error ratio testers will require 300 672 bytes of pattern storage memory to hold the complete TSS.

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50.3.8.3.2 Continuous Identical Digits

The CID pattern shall comprise 9 octets (72 bits) overwriting the Z0 octets at the end of the first row of the Section Overhead, as shown in Figure 50–14. The pattern shall alternate in consecutive WIS frames; in the first frame of the TSS, the pattern consists of 72 bits of zeros, and in the second frame the pattern consists of 72 bits of all ones.

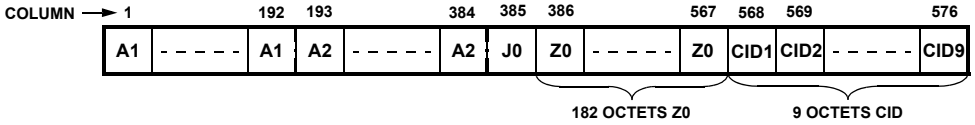

Figure 50–14—CID pattern structure

As the CID pattern is not scrambled, the string of ones (and, alternately, the string of zeros) forming the pattern produce transition-free areas within the TSS that stress the transmitter and receiver. Errors (eye closure at the transmitter or sampling errors at the receiver) are reflected as bit errors that are detected and reported via the BIP checking functionality in the WIS.

50.3.9 Loopback

The WIS is placed in Loopback mode when the Loopback bit in the WIS Control 1 register (45.2.2.1.2) is set to a logic one. In this mode, the WIS shall accept data on the transmit path from the 10GBASE-R PCS and return it on the receive path to the 10GBASE-R PCS. In addition, the WIS shall transmit a constant pattern to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer. The pattern output to the PMA transmit path at this time shall consist of a sequence of 8 logic zero bits and 8 logic one bits, forming the 16-bit word 00-FF hexadecimal. No SONET overhead or fixed stuff is output to the PMA at this time.

NOTE—The signal path through the WIS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that this signal path encompass as much of the WIS circuitry as is practical. The intention of providing this Loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data, while ensuring that remote entities do not interpret this test data as valid information. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

50.3.10 Link status

The WIS link status, as reported in the Link status bit of the WIS status 1 register (see 45.2.2.2.2), shall be set to down if a PLM-P, AIS-P, or LOP-P defect is detected (50.3.5.1), an AIS-L defect is detected (50.3.2.5), or the Synchronization process is not in the SYNC state (50.4.2). Otherwise, the WIS link status is set to up.

50.3.11 Management interface

The WIS supports a set of required and optional management objects to permit it to be controlled by the Station Management entity (STA). Access to management objects within the WIS is accomplished by means of a set of registers within the MDIO register space as defined in 45.2.2, which are implemented by the Link Management function depicted in Figure 50–2.

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50.3.11.1 Management registers

The WIS management interface function shall utilize the following dedicated management registers:

a) WIS Control 1 register (register 0)
b) WIS status 1 register (register 1)
c) WIS Control 2 register (register 7)
d) WIS status 2 register (register 8)
e) WIS test-pattern error counter register (register 9)
f) WIS Status 3 register (register 33)
g) WIS J0 transmit register (registers 64, 65, 66, 67, 68, 69, 70, 71)
h) WIS J0 receive register (registers 72, 73, 74, 75, 76, 77, 78, 79)
i) WIS Far End Path Block Error Count register (register 37)
j) WIS J1 transmit register (registers 39, 40, 41, 42, 43, 44, 45, 46)
k) WIS J1 receive register (registers 47, 48, 49, 50, 51, 52, 53, 54)
l) WIS Far End Line BIP Errors register pair (registers 55 and 56)
m) WIS Line BIP Errors register pair (register 57 and 58)
n) WIS Path Block Error Count register (register 59)
o) WIS Section BIP Error Count register (register 60)

These registers are implemented within the Device address space assigned to the WIS. The details of the register bit allocations and general usage are given in Clause 45. Note that Clause 45 also specifies several registers and register bits that are generic to every Device (e.g., Speed Ability and Identifier registers), and these are not covered by this clause.

NOTE—Clause 45 provides for additional vendor-specific registers within the address space assigned to the WIS. The presence, format, and function of these registers are implementation specific.

If the optional MDIO interface and associated register set are not implemented for the WIS, then equivalent capabilities are required to be provided.

50.3.11.2 WIS managed object class

The WIS Managed Object Class is defined in 30.8.1.

50.3.11.3 Management support objects

The following counters shall be provided to facilitate support of the WIS managed object class. If an MDIO interface is provided for the WIS, these counters are accessed via the WIS Far End Line BIP Errors and WIS Line BIP Errors registers, as described in 45.2.2.14 and 45.2.2.15 respectively. If no MDIO interface is implemented, these counters are to be accessible by equivalent means.

Far End Line BIP Errors

A 32-bit counter that is incremented by the number of Line BIP errors detected by the far-end WIS and reported via the M1 octet present in each received WIS frame (see 50.3.2.5). This counter has a maximum increment rate of 2 040 000 counts per second. The counter is cleared to zero when the WIS is reset, and wraps around to zero when it is incremented beyond the maximum count value. The contents of this counter are reflected in the WIS Far End Line BIP Errors register pair.

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Line BIP Errors

A 32-bit counter that is incremented by the number of Line BIP errors detected by the Receive process while processing each received WIS frame (see 50.3.2.5). This counter has a maximum increment rate of 12 288 000 counts per second. The counter is cleared to zero when the WIS is reset, and wraps around to zero when it is incremented beyond the maximum count value. The contents of this counter are reflected in the WIS Line BIP Errors register pair.

50.4 Synchronization state diagram

The WIS Synchronization process shall implement the state diagrams specified in this subclause and meet the corresponding state diagram interface requirements, also specified here. Additional requirements to this state diagrams are made in 50.3.4. In the case of any ambiguity between the text and the state diagrams, the state diagrams shall take precedence.

The notation used in the state diagrams is described in 21.5, and the conventions for state diagram timers in 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented by 1.

50.4.1 State diagram variables

Variables of the form name<x:0> indicate arrays or vectors of bits; for such variables, "<x>" indexes an element or set of elements in the array or vector, where "x" may be as follows:

— Any integer or set of integers.
— Any variable that takes on integer values.

In the variable and function descriptions in 50.4.1.2 and 50.4.1.3, the parameters *f*, *i*, *j*, *k*, *m*, and *n* are implementation-specific. Maximum and minimum values for these parameters are specified in 50.4.3.

50.4.1.1 Constants

A1

An octet value (bits 1:8) of 11110110 as assigned to the A1 framing character within the SONET Section Overhead, as specified in Table 1 of Section 4.2 of ATIS-0600416.1999(R2010). Used to obtain octet and WIS frame alignment.

A2

An octet value (bits 1:8) of 00101000 as assigned to the A2 framing character within the SONET Section Overhead, as specified in Table 1 of Section 4.2 of ATIS-0600416.1999(R2010). Used to obtain octet and WIS frame alignment.

Hunt_Pattern

A sequence of *i* consecutive A1 octets.

Presync_Pattern

A sequence of *j* consecutive A1 octets, immediately followed by a sequence of *k* consecutive A2 octets.

Sync_Pattern

A sequence of *f* consecutive A1 octets immediately followed by a sequence of *f* consecutive A2 octets.

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50.4.1.2 Variables

power_on

A condition that is true until such time as the power supply to the device containing the WIS has reached the operating region.

Values: FALSE; The device is completely powered and ready to operate.
TRUE; The device has not been completely powered.

reset

A Boolean variable that is true when a hardware reset has been applied to the WIS, and false otherwise.

Values: TRUE; A hardware reset is being applied.
FALSE; A hardware reset is not being applied.

signal_fail

A condition that is true whenever the underlying PMA sublayer indicates by means of the PMA_SIGNAL.indication primitive that valid data are not being supplied to the WIS. Once set to TRUE, signal_fail remains set until the PMA sublayer explicitly indicates that valid data are being recovered and supplied to the WIS, after which it is set to FALSE.

Values: FALSE; A PMA_SIGNAL.indication(SIGNAL_OK) primitive was received with SIGNAL_OK set to OK, indicating that the PMA has begun to provide valid data to the WIS Receive process.
TRUE; A PMA_SIGNAL.indication(SIGNAL_OK) primitive was received with SIGNAL_OK set to FAIL, indicating that the PMA is unable to provide valid data to the WIS Receive process.

in_HUNT

Boolean variable, set by the Primary Synchronization state diagram to indicate to the Interval Pattern Search state diagram to indicate that it has entered, or returned to, the HUNT state.

Values: TRUE; The Primary Synchronization state diagram is presently in the HUNT state.
FALSE; The Primary Synchronization state diagram is not in the HUNT state.

sync_start

Boolean variable, set by the Primary Synchronization state diagram to trigger the operation of the Interval Pattern Search state diagram.

Values: TRUE; The Interval Pattern Search state diagram should begin scanning for framing sequences.
FALSE; The Interval Pattern Search state diagram should not begin scanning.

50.4.1.3 Functions

found_Hunt

For each bit input to the Synchronization process, this function indicates whether the Hunt_Pattern pattern has been detected in the bit string formed by concatenating the current bit with the (i * 8 – 1) consecutive previously input bits. If the number of bits previously input is less than (i * 8 – 1), this function outputs a FALSE value. Note that this function inspects its input on a bit-by-bit basis.

Values: TRUE; The (i * 8) bits examined so far, consisting of the current bit plus previously input bits, matches Hunt_Pattern.
FALSE; The pattern is not matched, or less than (i * 8) bits have been input so far.

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found_Presync

For the last ($j + k$) sets of 8 bits (1 octet) input to the Synchronization process, this function indicates whether the Presync_Pattern pattern has been matched. If the number of octets previously input is less than ($j + k$), or the string match is still proceeding, this function outputs a WAIT value. Note that this function inspects its input on an octet-by-octet basis.

Values: TRUE; The octets examined so far, consisting of the current octet plus previously input bits, matches Presync_Pattern.
FALSE; The pattern is not matched.
WAIT; Insufficient data has been received so far to complete the match or declare failure.

found_Sync

For the last $2f$ sets of 8 bits (1 octet) input to the Synchronization process, this function indicates whether the Sync_Pattern pattern has been matched. If the number of octets previously input is less than $2f$, the function outputs a FALSE value. Note that this function inspects its input on an octet-by-octet basis.

Values: TRUE; The octets examined so far, consisting of the current octet plus previously input octets, matches Sync_Pattern.
FALSE; The pattern is not matched, or insufficient octets have been received so far.

50.4.1.4 Counters

good_sync_cnt

Count of the number of consecutive candidate Sync_Pattern pattern locations that contain a valid Sync_Pattern pattern. This counter is controlled by the Interval Pattern Search state diagram, and used to report the number of valid framing locations to the Primary Synchronization state diagram.

bad_sync_cnt

Count of the number of consecutive candidate Sync_Pattern pattern locations that have failed to contain a valid Sync_Pattern pattern. This counter is controlled by the Interval Pattern Search state diagram, and used to report the number of mismatched framing locations to the Primary Synchronization state diagram.

octet_cnt

Count of octets input to the Synchronization process; always increments for every octet input. This counter is forced to zero in specific states of the Interval Pattern Search state diagram, but for all other states it increments by 1 for each octet received. It is used to force the state diagram to wait in a given state until a required number of octets have been received.

50.4.2 State diagram

The Primary Synchronization state diagram is depicted in Figure 50–15, and the Interval Pattern Search state diagram in Figure 50–16. The WIS shall implement the Synchronization process according to these state diagrams, including compliance with the associated state variables as specified in 50.4.1. The Synchronization process is responsible for detecting octet and WIS frame boundaries and also for determining whether the underlying receive channel is ready for operation. Failure to achieve synchronization, as indicated by the Synchronization state diagram not being in the SYNC state, shall cause the WIS Receive process to suspend normal operation and propagate the error to the PCS as described in 50.3.5.

The function of the Primary Synchronization state diagram is to track the four phases through which the Synchronization process progresses in order to achieve and maintain lock to the incoming frame stream. In the first phase, the state diagram performs a bit-by-bit hunt over the input data for a string of A1 octets.

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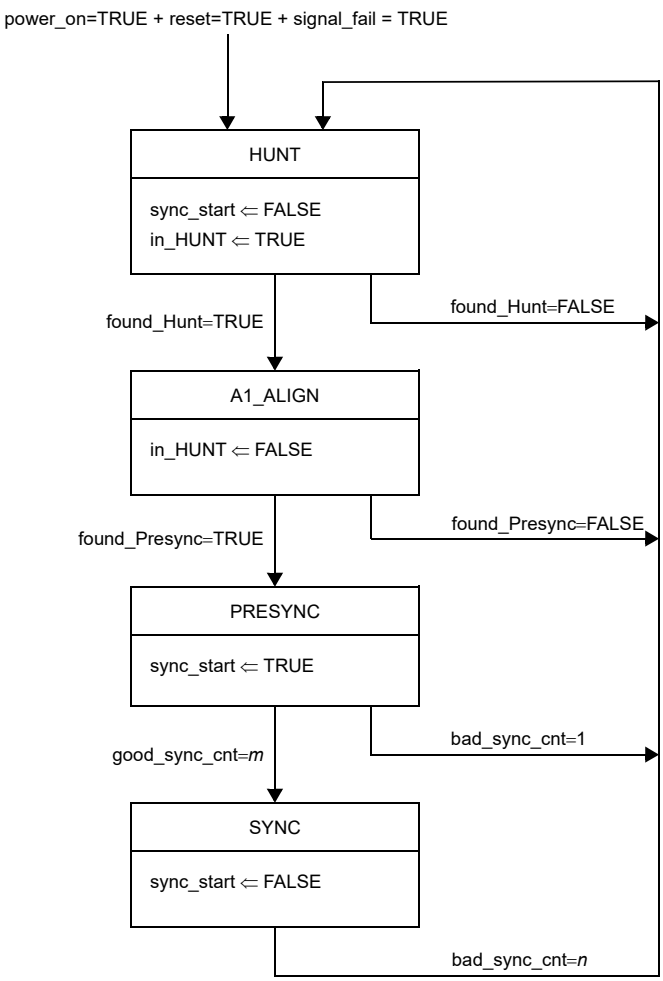

Figure 50–15—Primary Synchronization state diagram

Successful location of several A1 octets indicates both a candidate octet and a candidate frame boundary; this is validated by scanning for additional A1 octets followed immediately by another string of A2 octets, which corresponds to the framing pattern present at the start of every WIS frame. The candidate frame boundary is now confirmed by searching for several consecutive such patterns, each separated by a frame size; if successful, frame lock is deemed to have been achieved. The state diagram then remains in the frame lock state until a number of consecutive candidate pattern locations have failed to match the A1/A2 pattern. This behavior implements the necessary hysteresis required to reject transient bit errors.

The Interval Pattern Search state diagram is activated when the Synchronization process has successfully located the first occurrence of the framing pattern, and performs the actual function of searching for subsequent framing patterns that are located 155 520 octets apart, and counting failed and successful matches.

The functions fount_Hunt, found_Presync, and found_Sync implement bit and octet scanners that search through the incoming data stream for the respective data patterns that need to be matched.

NOTE—Implementations may choose any conforming means of realizing the state diagram described herein, provided that the external behavior of the Synchronization process is unchanged.

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50.4.3 Parameter values

Table 50–5 identifies the minimum and maximum values permissible for the parameters *f*, *i*, *j*, *k*, *m*, and *n* that are used in the preceding state diagram descriptions. Implementations shall set these parameters to values within the limits specified in the table.

Table 50–5—Minimum and maximum parameter values

Parameters	Minimum values	Maximum values	Purpose
f	2	192	Controls width of Sync_Pattern pattern
i	1	192	Controls width of Hunt_Pattern pattern
j	16	190	Controls width of Presync_Pattern pattern
k	16	192	Controls width of Presync_Pattern pattern
m	4	8	Controls hysteresis for SYNC state entry
n	1	8	Controls hysteresis for SYNC state exit

NOTE—The ranges for the parameters stipulated in Table 50–5 are intended to provide the implementer with latitude in creating implementations of the Synchronization process. However, adherence to the stipulated minimum values for the parameters will result in an implementation that provides the minimum time-to-frame (5 WIS frame periods) and required bit error tolerance at the normal BER (10^{-12}).

50.5 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801:1995.

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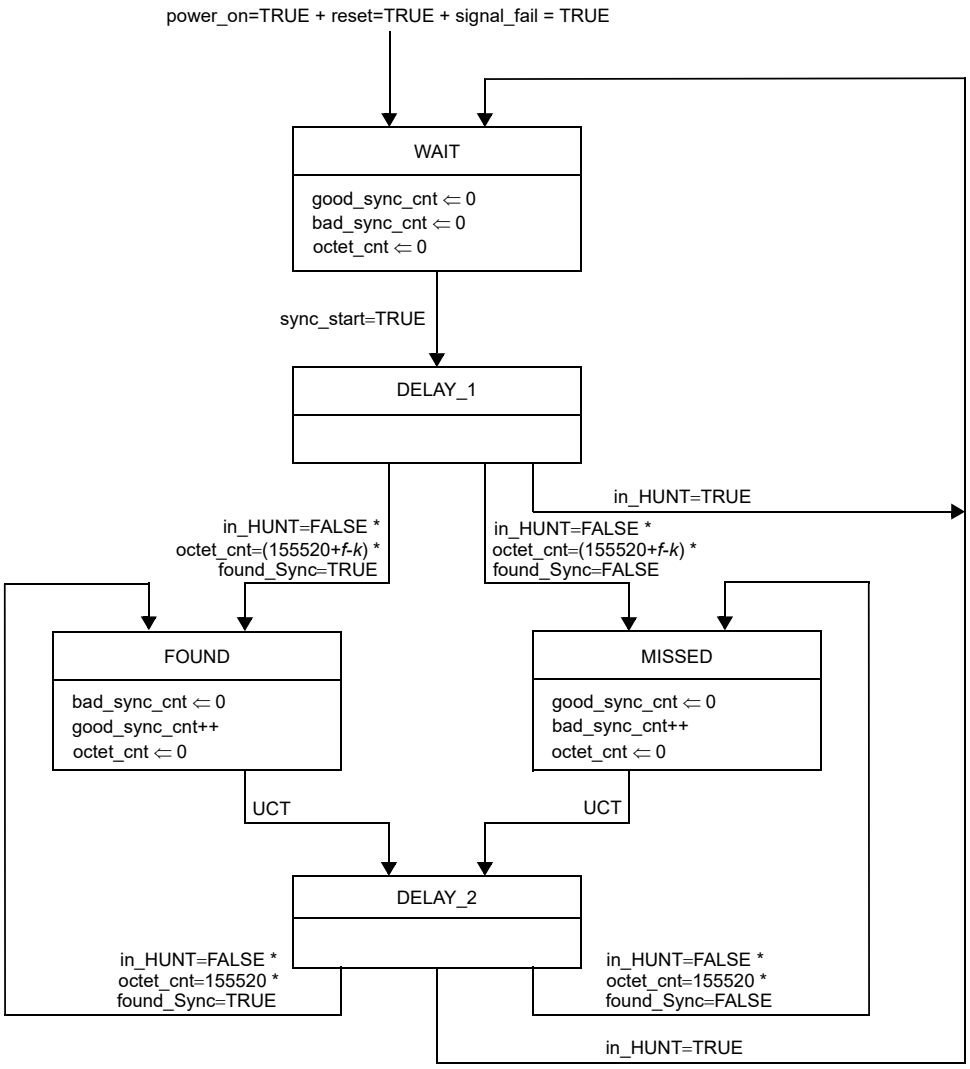

Figure 50–16—Interval Pattern Search state diagram

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50.6 Protocol implementation conformance statement (PICS) proforma for Clause 50, WAN Interface Sublayer (WIS), type 10GBASE-W[97]

50.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 50, WAN Interface Sublayer, type 10GBASE-W, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the same, can be found in Clause 21.

50.6.2 Identification

50.6.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

50.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, WAN Interface Sublayer (WIS), type 10GBASE-W
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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50.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XSBI	XSBI compatibility interface	51, 50.3.6	Compatibility interface supported	O	Yes [ ] No [ ]
*MD	MDIO	50.3.11.1	Registers and interface supported	O	Yes [ ] No [ ]
*PRBS	PRBS31 Test-pattern mode	50.3.8.2	Registers and functionality supported	O	Yes [ ] No [ ]

50.6.4 PICS proforma tables for the WAN Interface Sublayer (WIS), type 10GBASE-W

50.6.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Meets requirements of ATIS-0600416.1999(R2010)	50.1.1	Except as specifically excluded	M	
CC2	Precedence of ATIS-0600416.1999(R2010) and ATIS-0300269.2006(S2016) in case of discrepancies	50.3.2, 50.3.2.1, 50.3.2.3, 50.3.3	Unless specifically overridden by Clause 50	M	
CC3	Environmental specifications	50.5		M	Yes [ ]

50.6.4.2 WIS transmit functions

Item	Feature	Subclause	Value/Comment	Status	Support
WT1	Bit significance of data-unit vector from 10GBASE-R PCS	50.2.1.1	Data-unit<0> is interpreted as the least-significant bit	M	Yes [ ]
WT2	Payload mapping of octets from data-units to SPE by Transmit process	50.3.1.1	Tx_data-unit<7:0> mapped to lower-numbered (even) octet and tx_data-unit<15:8> to next higher-numbered (odd) octet	M	Yes [ ]
WT3	Bit relabeling during transmit mapping	50.3.1.1	Ethernet FCS error detection properties to be maintained	M	Yes [ ]
WT4	Path Overhead generation	50.3.2.1		M	Yes [ ]
WT5	J1 octet in Path Overhead	50.3.2.1	Transports a 16-octet repeating Path Trace Message	M	Yes [ ]
WT6	Default Path Trace Message	50.3.2.1	Consists of 15 octets of zeros and a header octet	M	Yes [ ]
WT7	Line Overhead generation	50.3.2.2		M	Yes [ ]
WT8	Unspecified Line Overhead octets	50.3.2.2	Set to 00000000 binary if not specifically listed	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
WT9	H1 and H2 octets in Line Overhead	50.3.2.2	Set to 522 decimal and also indicates concatenated payload	M	Yes [ ]
WT10	K1 octet in Line Overhead	50.3.2.2	Set to 00000000 binary	M	Yes [ ]
WT11	Bits 1 to 5 of K2 octet in Line Overhead	50.3.2.2	Set to 00000 binary	M	Yes [ ]
WT12	Bits 6 to 8 of K2 octet in Line Overhead	50.3.2.2	Set to either an RDI-L encoding, or 000 binary	M	Yes [ ]
WT13	Section Overhead generation	50.3.2.3		M	Yes [ ]
WT14	Unspecified Section Overhead octets	50.3.2.3	Set to 00000000 binary if not specifically listed	M	Yes [ ]
WT15	J0 octet in Section Overhead	50.3.2.3	Transports a 16-octet repeating Section Trace Message	M	Yes [ ]
WT16	Default Section Trace Message	50.3.2.3	Consists of 15 octets of zeros and a header octet	M	Yes [ ]
WT17	Frame scrambler	50.3.3		M	Yes [ ]
WT18	Octet ordering to PMA	50.3.6	First data-group transmitted contains the first two A1 octets	M	Yes [ ]
WT19	Bit ordering to PMA	50.3.6	Ethernet FCS error detection properties to be maintained	M	Yes [ ]
WT20	Data-group ordering to PMA	50.3.6		M	Yes [ ]
WT21	Transmit data delay constraint	50.3.7	Sum of transmit and receive data delays not to exceed 14336 BT	M	Yes [ ]

50.6.4.3 WIS receive functions

Item	Feature	Subclause	Value/Comment	Status	Support
WR1	Bit significance of data-unit vector to 10GBASE-R PCS	50.2.2.1	Data-unit<0> is interpreted as the least-significant bit	M	Yes [ ]
WR2	Payload mapping of octets from SPE to data-units	50.3.1.2	Rx_data-unit<7:0> mapped from lower-numbered (even) octet and rx_data-unit<15:8> from next higher-numbered (odd) octet	M	Yes [ ]
WR3	Bit relabeling during receive mapping	50.3.1.2	Ethernet FCS error detection properties to be maintained	M	Yes [ ]
WR4	Section, Line, and Path Overhead extraction and processing	50.3.2.4		M	Yes [ ]
WR5	Unsupported overhead octets	50.3.2.4	Ignored if marked as unsupported in Tables 50–1, 50–2, and 50–3	M	Yes [ ]
WR6	Unlisted overhead octets	50.3.2.4	Ignored if not listed in Table 1 of ATIS-0600416.1999(R2010)	M	Yes [ ]
WR7	Interpretation of J1 octet in Path Overhead	50.3.2.4	Interpreted as carrying a 16-byte repeating Path Trace Message	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
WR8	Extraction of valid Path Trace Message data	50.3.2.4	After receiver accomplishes synchronization	M	Yes [ ]
WR9	Interpretation of bits 6 through 8 of K2 octet in Line Overhead	50.3.2.4	Interpreted as carrying AIS-L or RDI-L	M	Yes [ ]
WR10	Unsupported encodings of bits 6 through 8 of K2 octet in Line Overhead	50.3.2.4	Ignored by receiver	M	Yes [ ]
WR11	Interpretation of J0 octet in Path Overhead	50.3.2.4	Interpreted as carrying a 16-byte repeating Section Trace Message	M	Yes [ ]
WR12	Extraction of valid Section Trace Message data	50.3.2.4	After receiver accomplishes synchronization	M	Yes [ ]
WR13	Detection of Section, Line and Path Defects and Anomalies	50.3.2.5	Only Defects and Anomalies listed in Table 50–4 processed	M	Yes [ ]
WR14	Support for PLM-P and LCD-P defects	50.3.2.5		M	Yes [ ]
WR15	Detection of LOS defect	50.3.2.5	No services provided by the PMA or PMD are used	M	Yes [ ]
WR16	LOS defect detection parameters	50.3.2.5	Parameters *T* and *T'* between 2.3 and 100 microseconds	M	Yes [ ]
WR17	Frame descrambler	50.3.3		M	Yes [ ]
WR18	Bit, octet and data-group ordering from PMA	50.3.6	Ethernet FCS error detection properties to be maintained	M	Yes [ ]
WR19	Delineation of octet and WIS frame boundaries	50.3.4	According to Synchronization process	M	Yes [ ]
WR20	Reporting of errors on synchronization failure	50.3.4	SEF or LOF defects reported on synchronization failure	M	Yes [ ]
WR21	Receive data delay constraint	50.3.7	Sum of transmit and receive data delays not to exceed 14336 BT	M	Yes [ ]

50.6.4.4 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Synchronization state diagram	50.4	Meets the requirements of Figures 50–15 and 50–16	M	Yes [ ]
SD2	Synchronization process	50.4.2		M	Yes [ ]
SD3	Receive process suspended upon failure to achieve synchronization	50.4.2		M	Yes [ ]
SD4	Synchronization parameters	50.4.3	Meets the requirements of Table 50–5	M	Yes [ ]

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50.6.4.5 Error notification

Item	Feature	Subclause	Value/Comment	Status	Support
EN1	Notification of fault presence to PCS	50.3.5	WIS_SIGNAL.indication SIGNAL_OK set to FAIL	M	Yes [ ]
EN2	Removal of fault notification to PCS in the absence of faults	50.3.5	WIS_SIGNAL.indication SIGNAL_OK set to OK	M	Yes [ ]
EN3	Faults notified to PCS	50.3.5.1	Detects and reports the following errors: Synchronization process not in SYNC state, PLM-P defect, AIS-P defect, and LOP-P defect	M	Yes [ ]
EN4	PCS fault notification timing	50.3.5.2	Error propagation terminates, and valid data transferred, within 125 microseconds after error conditions removed	M	Yes [ ]
EN5	Presence of Loss of Code-group Delineation condition	50.3.5.3	When indicated by the 10GBASE-R PCS	M	Yes [ ]
EN6	Reporting of Loss of Code-group Delineation presence	50.3.5.3	Reported only if condition persists for more than 3 ms	M	Yes [ ]
EN7	Reporting with respect to WIS re-initialization	50.3.5.3	Report Loss of Code-group Delineation on re-initialization	M	Yes [ ]
EN8	Absence of Loss of Code-group Delineation condition	50.3.5.3	When indicated by the 10GBASE-R PCS	M	Yes [ ]
EN9	Reporting of Loss of Code-group Delineation absence	50.3.5.3	Reported only if condition is absent for more than 1 ms	M	Yes [ ]

50.6.4.6 Management registers and functions

Item	Feature	Subclause	Value/Comment	Status	Support
MR1	Management registers	50.3.11.1	If management registers are not physically implemented, equivalent capabilities have to be provided	MD:M	Yes [ ]
MR2	Management support objects	50.3.11.3	If management interface is not physically implemented, equivalent capabilities have to be provided	MD:M	Yes [ ]
MR3	Loopback function	50.3.9	Data accepted on the transmit path from the 10GBASE-R PCS returned via the receive path	M	Yes [ ]
MR4	Data transmitted to PMA during loopback	50.3.9	The 16-bit pattern 00-FF hexadecimal is transmitted	M	Yes [ ]
MR5	Data received from PMA during loopback	50.3.9	All data received from PMA during loopback is ignored	M	Yes [ ]
MR6	WIS link status function	50.3.10	Set to up or down as defined	M	Yes [ ]

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50.6.4.7 WIS test-pattern generator and checker

Item	Feature	Subclause	Value/Comment	Status	Support
TP1	Test-pattern generator and checker	50.3.8	Separate generator and checker functionality for transmit and receive	M	Yes [ ]
TP2	Data pattern used in square-wave test-pattern mode	50.3.8.1	Data pattern as specified in 52.9.1	M	Yes [ ]
TP3	PRBS31 generator functionality	50.3.8.2		PRBS:M	Yes [ ]
TP4	PRBS31 checker functionality	50.3.8.2		PRBS:M	Yes [ ]
TP5	Bit error detection and reporting by PRBS31 checker	50.3.8.2	If management interface is not physically implemented, equivalent reporting capabilities have to be provided	PRBS:M	Yes [ ]
TP6	Bit error detection in received mixed-frequency test pattern	50.3.8.3	Detection by Section, Line and Path BIP checking facilities	M	Yes [ ]
TP7	Functionality of WIS Transmit, Receive and Synchronization processed in mixed-frequency test-pattern mode	50.3.8.3	With the exceptions that fault processing and error propagation are not carried out, the Z0 octets are overwritten with CID pattern, and a PRBS used in place of the PCS data	M	Yes [ ]
TP8	Format of TSS	50.3.8.3.1		M	Yes [ ]
TP9	PRBS generator reset in TSS	50.3.8.3.1	Reset to all-ones prior to start of SPE	M	Yes [ ]
TP10	PRBS generator invert in TSS	50.3.8.3.1	Invert PRBS pattern in second SPE	M	Yes [ ]
TP11	Overhead octets in TSS	50.3.8.3.1	Set to defaults except for J1	M	Yes [ ]
TP12	Default value for J1 in TSS	50.3.8.3.1	Set to 89 hexadecimal if not used for providing stress	M	Yes [ ]
TP13	CID pattern used in TSS	50.3.8.3.2	72 bits of ones and 72 bits of zeros	M	Yes [ ]
TP14	Alternating value for CID pattern	50.3.8.3.2	72 bits of zeros in first frame and 72 bits of ones in second	M	Yes [ ]

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51. Physical Medium Attachment (PMA) sublayer, type Serial

51.1 Overview

This clause defines the functional characteristics for the Physical Media Attachment (PMA) used in 10GBASE-R and 10GBASE-W. Figure 51–1 depicts the relationships of the serial PMA (shown shaded) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

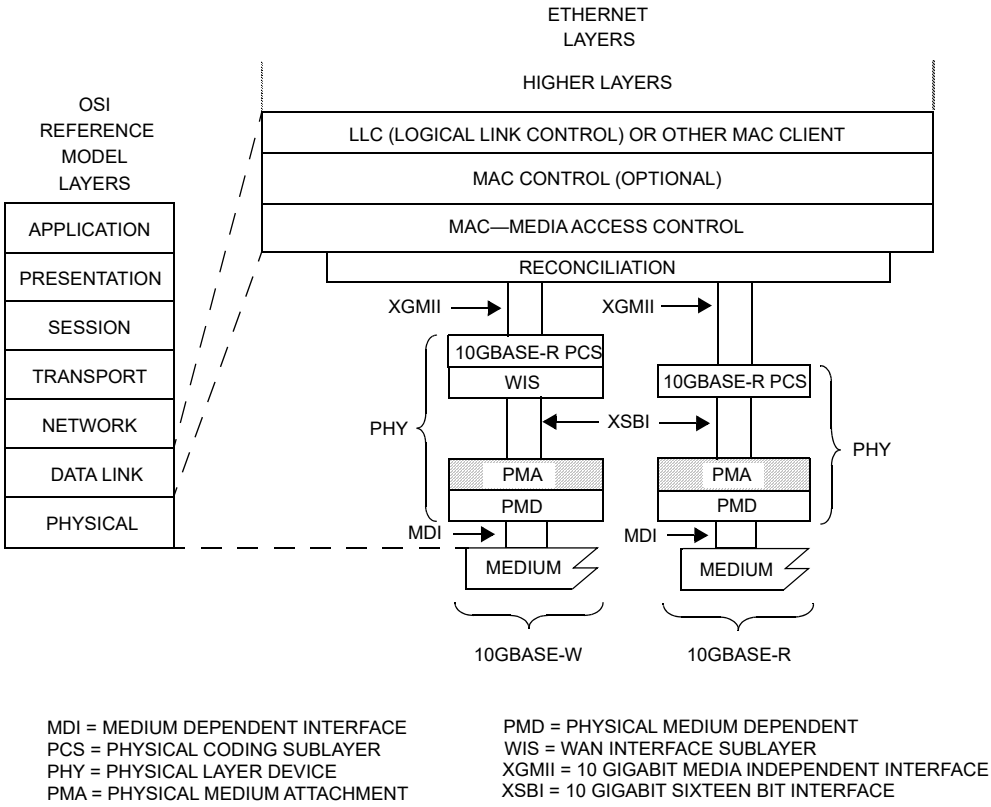

Figure 51–1—Relationship of serial PMA to PCS, WIS, and PMD

The purpose of the serial PMA is to attach the PMD of choice to its client, i.e., the PCS or WIS sublayer.

51.1.1 Scope

This clause specifies the functions, features, and services of the serial PMA sublayer, including electrical and timing specifications for the 10 Gigabit sixteen bit interface (XSBI). Specifications for the serial input and output of the PMA are left to the implementer with conformance and consideration of the serial PMD type. The serial PMA is used between the PMD and the PMA client as shown in Figure 51–1.

51.1.2 Summary of functions

The following is a summary of the principal functions implemented by the PMA.

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In the transmit direction (i.e., transmitting data from the PMA client to the PMD), the PMA performs the following functions:

a) Provide transmit source clock to PMA client.
b) Serialization of 16-bit data to serial bit stream.
c) Transmission of serial data to PMD.

In the receive direction (i.e., serial data from PMD to the PMA client), the PMA performs the following functions:

a1) Bit clock recovery of serial data from PMD.
b1) Provide receive clock to PMA client.
c1) Deserialization of serial data to16-bit parallel data.
d1) Transmission of parallel data to PMA client.
e1) Provide link status information.

51.2 PMA Service Interface

The Serial PMA provides a Service Interface to the 10G BASE-R PCS or WIS sublayer, i.e., the PMA client. These services are described in an abstract manner and do not imply any particular implementation. The PMA Service Interface shall support the exchange of data-groups between the PMA and the PMA client. The PMA converts data-groups into bits and passes these to the PMD, and vice versa. It also generates an additional status indication for use by its client.

The following primitives are defined:

PMA_UNITDATA.request(tx_data-group<15:0>)

PMA_UNITDATA.indication(rx_data-group<15:0>)

PMA_SIGNAL.indication(SIGNAL_OK)

PMA_RXMODE.request(rx_mode)

PMA_TXMODE.request(tx_mode)

PMA_ENERGY.indication(energy_detect)

51.2.1 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of data-groups) from the PMA client to the PMA. PMA_UNITDATA.request is generated by the PMA client's transmit process.

51.2.1.1 Semantics of the service primitive

PMA_UNITDATA.request(tx_data-group<15:0>)

The data conveyed by PMA_UNITDATA.request is a 16 bit vector representing a single data-unit which has been prepared for transmission by the PMA client.

51.2.1.2 When generated

The PMA client continuously sends tx_data-group<15:0> to the PMA at a nominal clock rate of 644.53125 MHz and 622.08 MHz in 10GBASE-R and 10GBASE-W operations, respectively.

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51.2.1.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a series of sixteen PMD_UNITDATA.request primitives, requesting transmission of the indicated tx_data-group bit to the PMD.

51.2.2 PMA_UNITDATA.indication

This primitive defines the transfer of data (in the form of data-groups) from the PMA to its client. PMA_UNITDATA.indication is used by the client's synchronization process.

51.2.2.1 Semantics of the service primitive

PMA_UNITDATA.indication(rx_data-group<15:0>)

The data conveyed by PMA_UNITDATA.indication is a 16 bit vector representing a single data-unit which has been prepared for transmission by the PMA receive process to the PMA client.

51.2.2.2 When generated

The PMA continuously sends one rx_data-group<15:0> to the PMA client corresponding to the receipt of each data-group of sixteen PMD_UNITDATA.indication primitives received from the PMD. The PMA sends the rx_data-group<15:0> at a nominal rate derived from the recovered bit clock.

51.2.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

51.2.3 PMA_SIGNAL.indication

This primitive is sent by the PMA to its client to indicate the status of the receive process. PMA_SIGNAL.indication is generated by the PMA receive process to propagate the detection of severe error conditions (e.g. no valid signal being received from the PMD sublayer) to the PMA client.

51.2.3.1 Semantics of the service primitive

PMA_SIGNAL.indication (SIGNAL_OK)

The SIGNAL_OK can take one of two values: OK or FAIL. A value of FAIL denotes that invalid data is being presented to the PMA client. A value of OK does not guarantee valid data is being presented to the PMA client.

51.2.3.2 When generated

The PMA generates a PMA_SIGNAL.indication primitive to the PMA client whenever there is change in the value of the SIGNAL_OK parameter.

51.2.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

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51.2.4 PMA_RXMODE.request

This primitive is generated by the PCS Receive Process for EEE capability (see 78.3) to indicate when the PMA and PMD receive functions may go into a low power mode, see 49.3.6.6. Without EEE capability, the primitive is never invoked and the PMA behaves as if rx_mode = DATA.

51.2.4.1 Semantics of the service primitive

PMA_RXMODE.request(rx_mode)

The rx_mode parameter takes on one of two values: QUIET or DATA.

51.2.4.2 When generated

The PCS generates this primitive to indicate the low power mode of the receive path.

51.2.4.3 Effect of receipt

When received the PMA receive is configured appropriately for the indicated state and the value is propagated to PMD_RX_MODE.request(rx_mode). When rx_mode is DATA, the PMA operates normally. When rx_mode is QUIET, the PMA may go into a low power mode.

51.2.5 PMA_TXMODE.request

This primitive is generated by the PCS Transmit Process for EEE capability to invoke the appropriate PMA and PMD transmit EEE states, see 49.2.13.3.1. Without EEE capability, the primitive is never invoked and the PMA behaves as if tx_mode = DATA.

51.2.5.1 Semantics of the service primitive

PMA_TXMODE.request(tx_mode)

The tx_mode parameter takes on one of three values: QUIET, ALERT, or DATA.

51.2.5.2 When generated

The PCS generates this primitive to indicate the low power mode of the transmit path.

51.2.5.3 Effect of receipt

When received the PMA transmit is configured appropriately for the indicated state and the value is propagated to PMD_TX_MODE.request(tx_mode). When tx_mode is DATA, the PMA operates normally. When tx_mode is QUIET, the PMA may go into a low power mode. When tx_mode is ALERT, the PMA operation is not defined.

51.2.6 PMA_ENERGY.indication

This primitive is sent by the PMA to its client to indicate the status of the receive process for EEE capability. PMA_ENERGY.indication is generated by the PMA receive process to propagate the energy detection indication from the PMD to the PMA client.

51.2.6.1 Semantics of the service primitive

PMA_ENERGY.indication(energy_detect)

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The energy_detect parameter is Boolean and reflects the state of the PMD_SIGNAL.-indication(SIGNAL_OK) received from the PMD.

51.2.6.2 When generated

The PMA generates this primitive whenever there is a change in the value of the SIGNAL_OK parameter.

51.2.6.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

51.3 Functions within the PMA

The PMA comprises the PMA Transmit and PMA Receive processes for 10GBASE-W and 10GBASE-R. The PMA Transmit process serializes the tx_data-groups and passes them to the PMD for transmission on the underlying medium. Similarly, the PMA Receive process deserializes received data from the PMD and presents the data as rx_data-groups to the PMA client. The PMA receiver continuously conveys sixteen-bit data-groups to the PMA client, independent of data-group alignment.

NOTE—Strict adherence to manufacturer-supplied guidelines for the operation and use of PMA serializer components is required to meet the jitter specifications of the respective PMD clause. The supplied guidelines should address the quality of power supply filtering associated with the transmit clock generator, and also the purity of reference clock fed to the transmit clock generator.

51.3.1 PMA transmit function

The PMA Transmit function passes data unaltered (except for serializing) from the PMA client directly to the PMD. Upon receipt of a PMA_UNITDATA.request primitive, the PMA Transmit function shall serialize the sixteen bits of the tx_data-group<15:0> parameter and transmit them to the PMD in the form of sixteen successive PMD_UNITDATA.request primitives.

51.3.2 PMA receive function

The PMA Receive function passes data unaltered from the PMD directly to the PMA client. Upon receipt of sixteen successive PMD_UNITDATA.indication primitives, the PMA shall assemble the sixteen received bits into a single sixteen-bit value and pass that value to the PMA client as the rx_data-group<15:0> parameter of the primitive PMA_UNITDATA.indication. The PMA receive function does not align rx_data-group<15:0> to the original tx_data-group<15:0> from the remote end of the link.

51.3.3 Delay Constraints

The PMA receives a one bit data stream from the PMD and presents a sixteen bit wide data unit to the PMA client. Received bits from the PMD are buffered to facilitate proper deserialization of the rx_data-group<15:0> to the PMA client. These functions necessitate an internal PMA delay of at least sixteen unit intervals. In practice, this serial to parallel conversion may necessitate even longer delays of the incoming data stream.

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. The sum of transmit and receive delay constraints for the serial PMA/PMD sublayer shall meet the requirements as specified in the respective PMD clause. The serial PMA/PMD sublayer includes the serial PMA, the serial PMD, and 2 m of fiber.

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51.4 Sixteen-Bit Interface (XSBI)

A physical instantiation of the sixteen-bit PMA service interface (XSBI) is defined to provide compatibility among devices designed by different manufacturers for the operation of PHY implementations in either the 10GBASE-R family or the 10GBASE-W family. There is no requirement for an integrated compliant device to implement or expose the XSBI. A XSBI implementation is described in 51.4 through 51.9. Though the XSBI is an optional interface, it is used extensively in this standard as a basis for specification. The PMA is specified to the XSBI interface, so if the XSBI is not physically implemented, a conforming implementation shall behave as if the XSBI functions were implemented.

Table 51–1 defines terms used within the description of the XSBI interface and the rest of this clause. For the XSBI instantiation of the PMA service interface, the mapping of bits between the PMA service interface and the XSBI physical interface is defined for transmit in Table 51–2 and for receive in Table 51–3. Figure 51–2 depicts the relationship between the XSBI physical instantiation and the service interface provided by the PMA to its client.

NOTE—Document OIF SFI-4-01.0, an implementer's agreement, was used as a basis for the development of the XSBI instantiation.

Table 51–1—Terms and definitions

Term	Definition
10GBASE-R nominal baud rate	10.3125 GBd
10GBASE-W nominal baud rate	9.95328 GBd
Data signals, data-group, clock signal	Operating rate is 1/16 of nominal baud rate
Differential signal name used without <P,N> (e.g., PMA_TX_CLK)	= signal<P> minus signal <N> (e.g., = PMA_TX_CLK<P-N>)

Table 51–2—Transmit bit mapping

	Name	Bit numbers															
PMA service interface	tx_data-group	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
XSBI physical interface	xsbi_tx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 51–3—Receive bit mapping

	Name	Bit numbers															
PMA service interface	rx_data-group	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
XSBI physical interface	xsbi_rx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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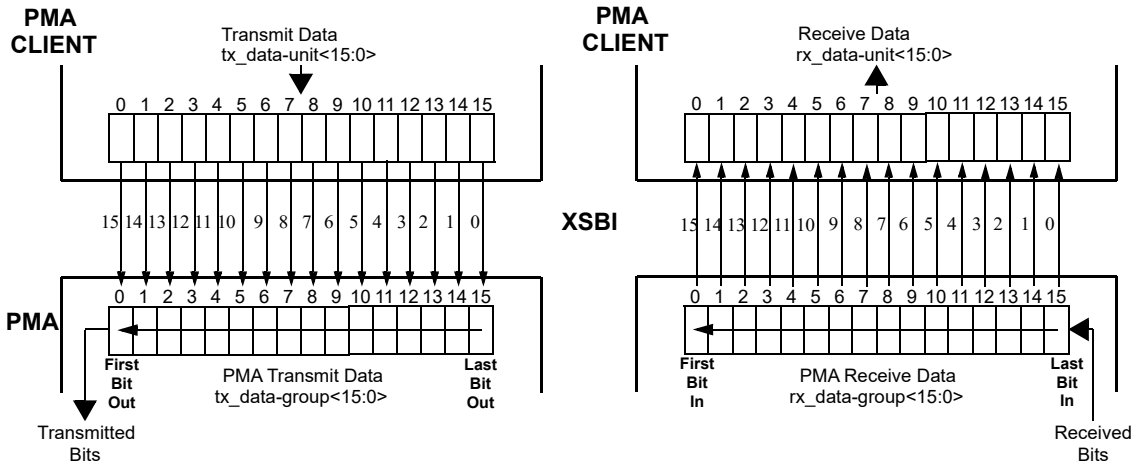

Figure 51–2—XSBI physical interface mapping into PMA service interface

As depicted in Figure 51–3, the XSBI connects the PMA to its client, the PCS or WIS sublayer. It is equipped for full duplex transmission of data-groups with associated data-group clock signals. The PMA client provides data-groups on xsbi_tx<15:0> to the XSBI transmit function which latches the data on the rising edge of the PMA_TX_CLK. See section 51.6.1.2 for details. The PMA_TX_CLK signal is derived from PMA_TXCLK_SRC as provided by the PMA. An internal Transmit Clock Generation Unit (TXCGU) uses REFCLK to generate the internal bit clock that is used to serialize the latched data out of the PMA outputs.

The PMA Receive function accepts serial data from the PMD and extracts a bit clock and recovered data from the serial inputs in the Receive Clock Recovery Unit (RXCRU). The recovered data is deserialized and conveyed to the PMA client on xsbi_rx<15:0>. The rising edge of the recovered clock, PMA_RX_CLK, which is at 1/16 the bit rate, is used by the PMA to send the received 16-bit data-groups to the PMA client.

The PMA_SIGNAL.indication is a function of PMD_SIGNAL.indication, the Sync_Err signal and the optional PMA loopback signal. These signals can be seen in context in Figure 44A–7 and Figure 51–3. In the case of PMA loopback being inactive, the PMA_SIGNAL will indicate a FAIL whenever the PMD_SIGNAL.indication indicates a FAIL. The PMA_SIGNAL will also indicate a FAIL when Sync_Err is valid, i.e., PMA unable to recover clock from the incoming data stream. If the PMA loopback function is implemented and activated, the PMA_SIGNAL.indication will ignore the PMD_SIGNAL.indication and behave as if PMD_SIGNAL.indication is valid.

PMA_RX_CLK is derived from the serial input data whenever possible. When there is no valid input signal or the optional Synchronization Error (Sync_Err) asserted or other conditions where the PMA cannot derive the clock from the serial input data, a valid PMA_RX_CLK is provided as described in 51.7.2.

51.4.1 Required signals

In the event this XSBI is made accessible, the signals listed in Table 51–4 are provided, with the meanings described elsewhere in this subclause.

xsbi_tx<15:0>
: The 16-bit parallel low-voltage differential signaling (LVDS) data presented to the XSBI for serialization and transmission onto the media. Bit xsbi_tx<15> shall be transmitted first, followed by xsbi_tx<14> through xsbi_tx<0>.

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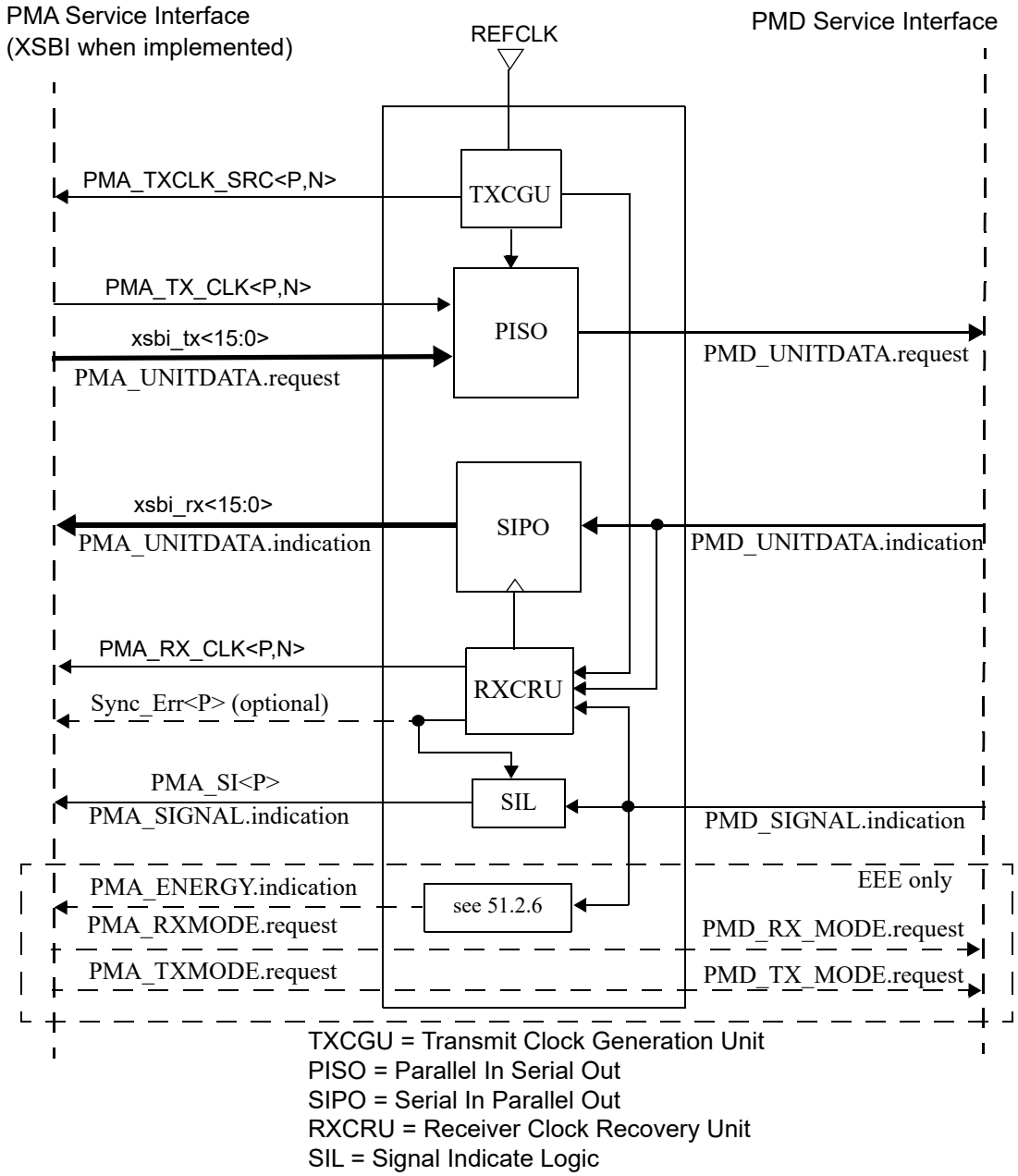

Figure 51–3—XSBI reference diagram

PMA_TX_CLK<P,N>

The LVDS transmit data-group clock. This data-group clock is used to latch data into the PMA for transmission. The PMA_TX_CLK<P,N> shall be derived from PMA_TXCLK_SRC<P,N>. The rising edge of PMA_TX_CLK is used to latch data into the PMA for transmission. Refer to 51.6.1.2 for details.

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Table 51–4—XSBI required signals

Symbol	Signal name	Signal type	Active level
xsbi_tx<15:0>	Transmit Data	Input	H
PMA_TX_CLK<P,N>	Transmit Clock	Input	↑
PMA_TXCLK_SRC<P,N>	Transmit Clock Source	Output	either edge
xsbi_rx<15:0>	Receive Data	Output	H
PMA_RX_CLK<P,N>	Receive Clock	Output	↑
PMA_SI<P>	PMA Signal Indicate	Output	H

PMA_TXCLK_SRC<P,N>

The LVDS transmit data-group clock source. The PMA derives the PMA_TXCLK_SRC<P,N> from the local REFCLK. The PMA_TXCLK_SRC<P,N> is used by the PMA client to derive PMA_TX_CLK<P,N>.

xsbi_rx<15:0>

The 16-bit parallel LVDS data transmitted by the PMA and presented to the PMA client for further processing. The PMA deserializes the incoming data to 16-bit wide data groups, xsbi_rx<15:0>. Bit xsbi_rx<15> shall be received first, followed by xsbi_rx<14> through xsbi_rx<0>. Data alignment is NOT performed by the PMA.

PMA_RX_CLK<P,N>

The LVDS receive data-group clock. The PMA derives the PMA_RX_CLK<P,N> from the line rate when the serial data from the PMD is present, or the REFCLK when the serial data from the PMD is absent, e.g. PMD_SI invalid or Sync_Err asserted. The xsbi_rx<15:0> data groups are presented to the PMA client on the rising edge of PMA_RX_CLK<P,N>.

PMA_SI<P>

A logic 0 on PMA Signal Indicate (PMA_SI) indicates that the receiver is unable to properly recover the receive data. The indicator is a function of the PMD_SIGNAL.indication status, the Sync_Err function and the optional PMA loopback signal. This signal is the physical instantiation of the SIGNAL_OK parameter as described in the PMA_SIGNAL.indication primitive. This signal shall be compliant with the EIA/JESD8-B Interface Standards for Nominal 3V/3.3V Supply Digital Integrated Circuits.

51.4.2 Optional Signals

Sync_Err<P>

This signal is used to indicate the inability of the PMA to recover the clock from the serial data stream. A logic high indicates that there is a synchronization error. A logic low does not guarantee synchronization. This signal shall be compliant with the EIA/JESD8-B Interface Standards for Nominal 3V/3.3V Supply Digital Integrated Circuits.

energy_detect

If the optional Energy-Efficient Ethernet (EEE) function is supported (see Clause 78) then the XSBI interface includes energy_detect as described in 51.2.

rx_quiet

If the optional EEE function is supported (see Clause 78) then the XSBI interface includes rx_quiet as described in 51.2.

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tx_quiet

If the optional EEE function is supported (see Clause 78) then the XSBI interface includes tx_quiet as described in 51.2.

51.5 General electrical characteristics of the XSBI

In the event this XSBI is made accessible, this subclause specifies the general electrical characteristics of the XSBI.

NOTE—All LVDS AC and DC parameters are required to conform to the TIA/EIA-644 LVDS specification with the exception of those parameters specified by the tables of this clause.

51.5.1 DC characteristics

Table 51–5 documents the required DC parametric attributes of all inputs and outputs of the XSBI. The signal specification is based on low voltage differential signals (LVDS) as described in ANSI/TIA-644 LVDS specifications. Unless otherwise stated, all terms and test conditions related to electrical parameters (AC or DC) are as specified in the TIA/EIA-644 LVDS document.

Table 51–5—Electrical specifications

Symbol	Parameter	Conditions	Min	Max	Units	Note
$\|V_{OD}\|$	Output differential voltage	Differential load, R_{load} = 100Ω ± 1%	250	400	mV	
V_{OS}	Output offset voltage	Differential load, R_{load} = 100Ω ± 1%	1125	1375	mV	
R_O	Output impedance, single ended		40	140	Ω	[a]
ΔR_O	R_O mismatch			10	%	*
$\|\Delta V_{OD}\|$	Change in VOD between “0” and “1”	Differential load, R_{load} = 100Ω ±1%		50	mV	
$\|\Delta V_{OS}\|$	Change in VOS between “0” and “1”	Differential load, R_{load} = 100Ω ±1%		50	mV	
V_I	Input voltage range	|Vgpd| < 50mV	900	1600	mV	[b]
V_{ID}	Input differential voltage	|Vgpd| < 50mV	100	600	mV	
R_{IN}	Receiver differential input impedance		70	130	Ω	*
t_R, t_F	20%-80% rise and fall times		100	400	ps	*

[a]Modified from or not specified in TIA/EIA-644 document.
[b]$|V_{gpd}|$ is the ground potential differential between PMA client and PMA.

51.5.2 Valid signal levels

All AC measurements are made from the cross-over level of the clock to the valid input or output data levels as shown in Figure 51–4. The CLK and DATA is defined to be the differential signal, i.e., <P-N>, of a clock or data signal.

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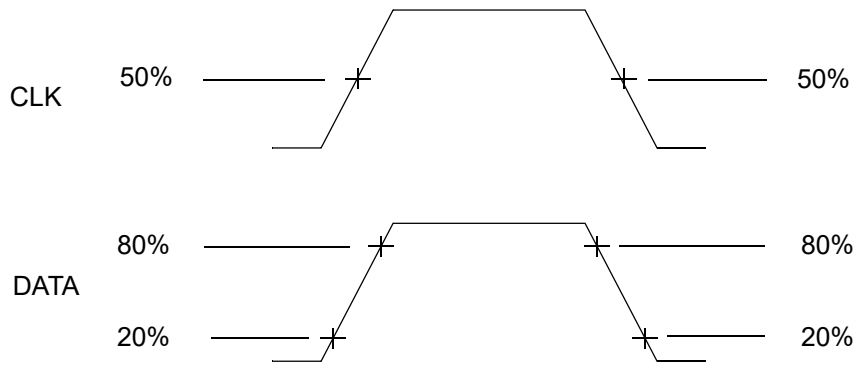

Figure 51–4—Input/output valid level for AC measurements

51.5.3 Rise and fall time definition

The rise and fall time definition for PMA_TX_CLK, PMA_TXCLK_SRC, PMA_RX_CLK, and DATA is shown below in Figure 51–5. All signals are measured differentially.

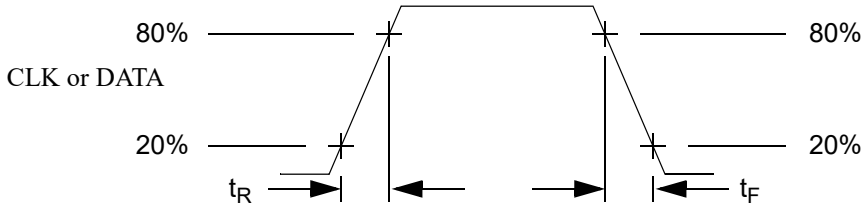

Figure 51–5—Rise and fall time definition

51.5.4 Output load

All AC measurements are assumed to have a differential output load of 100 Ω ± 1%.

51.6 XSBI transmit interface electrical characteristics

In the event this XSBI is made accessible, the electrical characteristics of the XSBI transmit interface are specified in this subclause. A XSBI receiver shall meet the specifications in sections 51.6.1 through 51.6.2.

NOTE—The following approach is taken for positioning clocks relative to the data. For both the PMA and PMA client drivers, the <P-N> clock edges are aligned to the data edges, to allow simplification of macro design. For both the PMA and PMA client receivers, the <P-N> clock edges are centered on the data bit, to allow simplification of macro design. The implementation to meet these requirements may be achieved on the system board. This can be done with either a delay of the clocks or by exchanging the positive and negative signals of the differential clock outputs.

51.6.1 XSBI transmit interface timing

The XSBI transmit interface timing specification consists of two separate specifications. The timing specifications at the PMA client output and the PMA input are described in 51.6.1.1 and 51.6.1.2, respectively. Data is latched into the PMA using rising edge of PMA_TX_CLK. The relationship between PMA_TX_CLK and PMA_TXCLK_SRC are described in 51.6.2. All transitions in Figure 51–6 and

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Figure 51–7 are specified from the PMA_TX_CLK reference level, to valid input signal levels (refer to 51.5.2).

51.6.1.1 PMA client output timing

Figure 51–6 and Table 51–6 detail the XSBI timing requirements for transmit data relative to PMA_TX_CLK at the PMA client outputs.

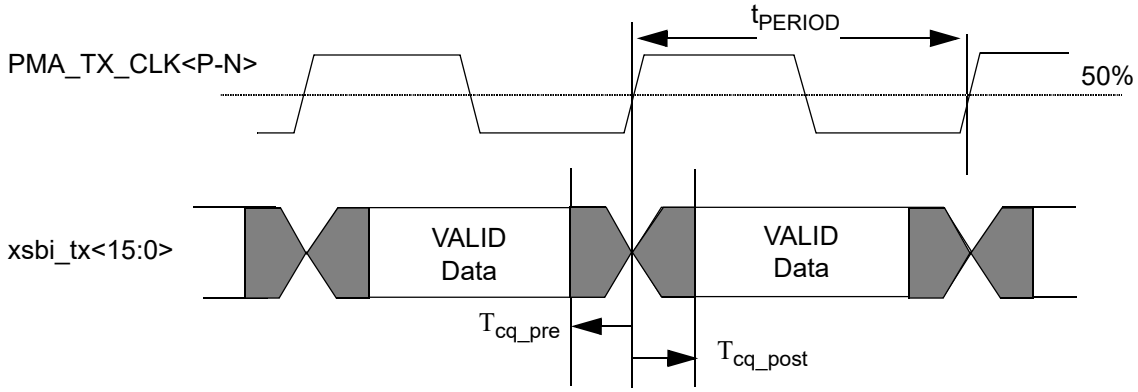

Figure 51–6—PMA client output timing

Table 51–6—PMA client output timing specifications

Parameter	Description	Min	Typ	Max	Units
t_{PERIOD}	PMA_TX_CLK Period 10GBASE-R 10GBASE-W		 1.55151 1.60751		ns[a]
T_{cq_pre}	data invalid window before ↑ PMA_TX_CLK<N-P>			200	ps
T_{cq_post}	data invalid window after ↑ PMA_TX_CLK<N-P>			200	ps
t_{DUTY}	PMA_TX_CLK Duty Cycle	40		60	%

[a]Period time value =1/644.53125 MHz for 10GBASE-R, similarly = 1/622.08 MHz for 10GBASE-W.

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51.6.1.2 PMA input timing

Figure 51–7 and Table 51–7 detail the XSBI timing requirements for transmit data relative to the PMA_TX_CLK at the PMA inputs.

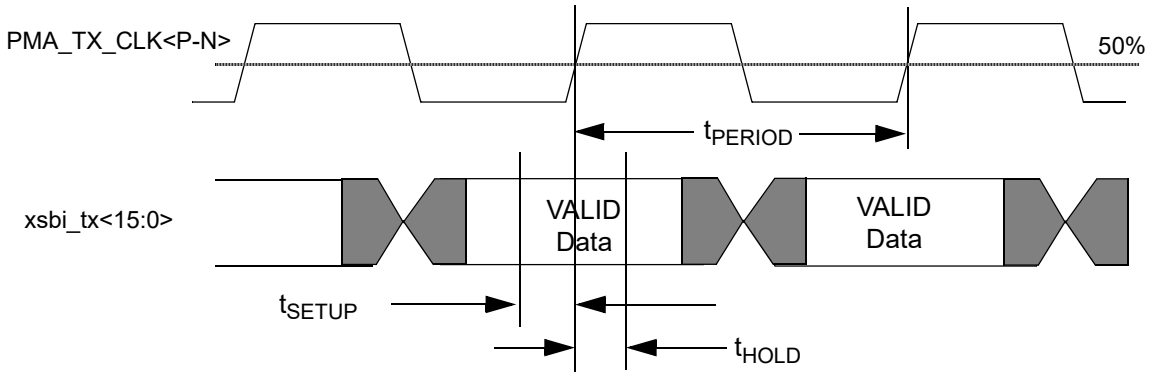

Figure 51–7—PMA input timing

Table 51–7—PMA input timing specifications

Parameter	Description	Min	Typ	Max	Units
t_{PERIOD}	PMA_TX_CLK period 10GBASE-R 10GBASE-W		 1.55151 1.60751		ns
t_{SETUP}	Data Setup to ↑ PMA_TX_CLK	300			ps
t_{HOLD}	Data Hold from ↑ PMA_TX_CLK	300			ps
t_{DUTY}	PMA_TX_CLK duty cycle	40		60	%

51.6.2 XSBI PMA_TX_CLK and PMA_TXCLK_SRC Specification

Table 51–8 specifies the XSBI interface transmit frequency. The frequency of xsbi_tx<15:0> and PMA_TX_CLK are derived from the frequency of PMA_TXCLK_SRC.

Table 51–9 specifies the phase variation between PMA_TX_CLK and PMA_TXCLK_SRC and the jitter requirements between PMA_TX_CLK and PMA_TXCLK_SRC. This specification describes the maximum delay variation through the PMA client (PMA_TXCLK_SRC to PMA_TX_CLK and xsbi_tx<15:0>). The absolute value of the delay is not specified, as it is not relevant to the operation of the interface.

Table 51–8—Transmit source clock specification

Parameter	Description	Value
$f_{PMA\_TXCLK\_SRC}$	PMA_TXCLK_SRC frequency 10GBASE-W 10GBASE-R	 622.08 MHz ± 20 ppm 644.53125 MHz ± 100 ppm

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Table 51–9—Transmitter clocks specification

Parameter	Description	Condition	**Value**(max)
TD	Variation of PMA_TXCLK_SRC to PMA_TX_CLK delay	frequency < 10 kHz	2ns(p-p)
CJ	Jitter between PMA_TXCLK_SRC and PMA_TX_CLK	frequency >10 kHz	175ps(p-p)

NOTE—The ± 20 ppm clock tolerance is not intended to interoperate directly with interfaces that comply with SONET of SDH standards, or other synchronous networks. Operation over electrically multiplexed payloads of a transmission network is outside the scope of this standard.

The TD parameter is defined to be the peak-to-peak variation of the phase offset measured in time between an arbitrary clock edge of the PMA_TXCLK_SRC clock and a selected clock edge on the PMA_TX_CLK. Letting "X" be the offset parameter, then TD = $X_{max} - X_{min}$.

51.7 XSBI receive interface electrical characteristics

In the event this XSBI is made accessible, the electrical characteristics of the XSBI receive interface are specified in this subclause. A XSBI receiver shall meet the specifications in 51.7.1 through 51.7.2.

NOTE—The following approach is taken for positioning clocks relative to the data. For both the PMA and PMA client drivers, the <P-N> clock edges are aligned to the data edges, to allow simplification of macro design. For both the PMA and PMA client receivers, the <P-N> clock edges are centered on the data bit, to allow simplification of macro design. The implementation to meet these requirements may be achieved on the system board. This can be done with either a delay of the clocks or by exchanging the positive and negative signals of the differential clock outputs.

51.7.1 XSBI receive interface timing

The XSBI receive interface timing specification consists of two separate specifications. The timing specifications at the PMA output and the PMA client input are described in 51.7.1.1 and 51.7.1.2, respectively. Data is latched into the PMA client using the rising edge of PMA_RX_CLK. All transitions in Figure 51–8 and Figure 51–9 are specified from the PMA_RX_CLK reference level, to valid output signal levels (refer to 51.5.2).

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51.7.1.1 PMA output timing

Figure 51–8 and Table 51–10 detail the XSBI timing requirements for receive data relative to the PMA_RX_CLK at the PMA outputs.

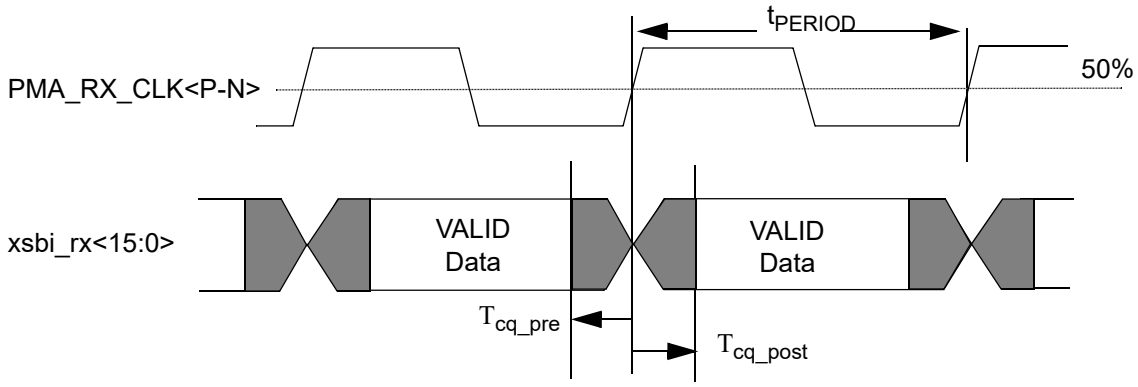

Figure 51–8—PMA output timing

Table 51–10—PMA output timing specifications

Parameter	Description	Min	Typical	Max	Units
t_{PERIOD}	PMA_RX_CLK period 10GBASE-R 10GBASE-W	—	 1.55151 1.60751	—	ns
T_{cq_pre}	data invalid window before ↑ PMA_RX_CLK<N-P>	—	—	200	ps
T_{cq_post}	data invalid window after ↑ PMA_RX_CLK<N-P>	—	—	200	ps
t_{DUTY}	PMA_RX_CLK duty cycle	45	—	55	%

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51.7.1.2 PMA client input timing

Figure 51–9 and Table 51–11 detail the XSBI timing requirements for receive data relative to the PMA_RX_CLK at the PMA client inputs.

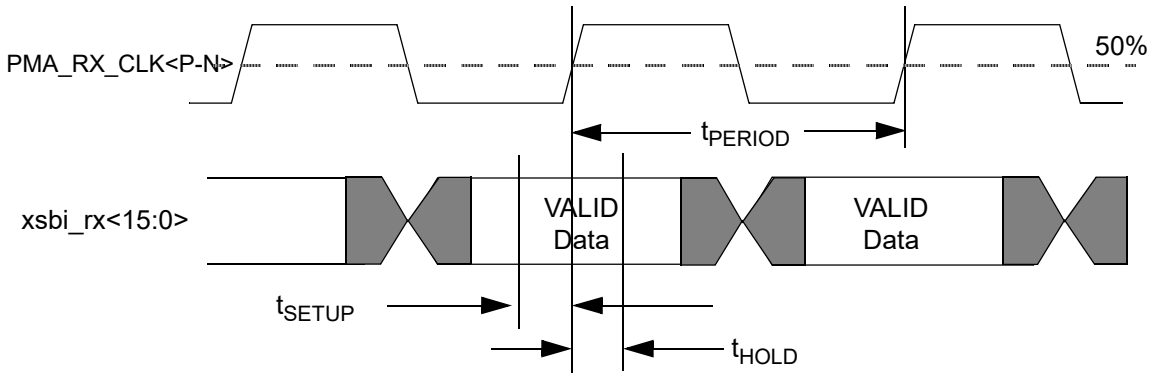

Figure 51–9—PMA client input timing

Table 51–11—PMA client input timing specifications

Parameter	Description	Min	Typical	Max	Units
t_{DUTY}	PMA_RX_CLK duty cycle	45	—	55	%
t_{SETUP}	Data Setup before ↑PMA_RX_CLK	300	—	—	ps
t_{HOLD}	Data Hold after ↑PMA_RX_CLK	300	—	—	ps

51.7.2 XSBI PMA_RX_CLK specification

Table 51–12 defines the PMA_RX_CLK frequency variation during PMA_SI valid and invalid conditions. PMA_RX_CLK is derived from the serial input data whenever possible. Under a loss-of-signal (LOS) or the optional Synchronization Error (Sync_Err) or other conditions where the PMA cannot derive the clock from the serial input data, a valid PMA_RX_CLK shall be provided with frequency characteristics as defined in Table 51–12. During the transitions from nominal clock to recovered clock or from recovered clock to nominal clock, the period and duty cycle requirements do not apply. However, the minimum pulse width should not change during the transitions between clock sources. During the transitions, the PMA_RX_CLK pulse width shall not be less than the minimum that is calculated by the period times the duty cycle as defined in Table 51–10 and Table 51–12.

51.8 PMA loopback mode (optional)

PMA loopback is optional. If PMA loopback is implemented it shall conform to the requirements of this subclause, i.e., 51.8.

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Table 51–12—Receiver clock specification

PMA_SI	Parameter	Description	Value
valid	$f_{PMA\_RX\_CLK}$	PMA_RX_CLK frequency 10GBASE-W 10GBASE-R	 622.08 MHz ± 20 ppm 644.53125 MHz ± 100 ppm
invalid	$f_{PMA\_RX\_CLK}$	PMA_RX_CLK frequency 10GBASE-W 10GBASE-R	 622.08 MHz ± 2500 ppm 644.53125 MHz ± 2500 ppm

If a Clause 45 MDIO is supported, then this function maps to the PMA loopback function as specified in 45.2.1.1.5. A device is placed in Loopback mode when the loopback bit in the PMA/PMD Control register 1 is set to a logic one. A device is removed from Loopback mode when this bit is set to a logic zero.

When loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. A device is explicitly placed in loopback mode (i.e., loopback mode is not the normal mode of operation of a device). The method of implementing loopback mode is not defined by this standard.

NOTE—Loopback mode may be implemented either in the parallel or the serial circuitry of a device.

51.9 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801:1995.

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51.10 Protocol implementation conformance statement (PICS) proforma for Clause 51, Physical Medium Attachment (PMA) sublayer, type Serial[98]

51.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 51, PMA Interface Sublayer, type Serial, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the same, can be found in Clause 21.

51.10.2 Identification

51.10.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

51.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 51, PMA Interface Sublayer (PMA), type Serial
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[98] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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51.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
LPI	Implementation of LPI	51.2		O	Yes [ ] No [ ]
*XSBI	XSBI interface	51.4	Physical instantiation of PMA service interface	O	Yes [ ] No [ ]
M1	XSBI functionality	51.4	Behave functionally as if the XSBI is implemented	M	Yes [ ]
M2	PMA Service Interface	51.2	Supports data group transfer between PMA and PMA client	M	Yes [ ]
M3	PMA_SI	51.4.1	EIA/JESD8-B compliance	M	Yes [ ]
M4	Sync_Err	51.4.2	Local PMA synchronization indicator and EIA/ JESD8-B compliance	O	Yes [ ] No [ ]
M5	Local PMA loopback	51.8		O	Yes [ ] No [ ]
MD	MDIO interface	51.8	Registers and interface supported	O	Yes [ ] No [ ]

51.10.4 PICS proforma tables for the PMA Interface Sublayer, type Serial

51.10.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Environmental specifications	51.9		M	Yes [ ]

51.10.4.2 PMA transmit functions

Item	Feature	Subclause	Value/Comment	Status	Support
PT1	Serialization and transmission of datagroup	51.3.1		M	Yes [ ]
PT2	Order of transmission	51.4.1	Bit xsbi_tx<15> shall be transmitted first	M	Yes [ ]
PT3	PMA_TX_CLK	51.4.1	PMA_TX_CLK derived from PMA_TXCLK_SRC	XSBI:M	Yes [ ] N/A[ ]
PT4	LVDS electrical compliance	51.5	Conformance to TIA/EIA644 LVDS specifications and to Table 51–5	XSBI:M	Yes [ ] N/A[ ]
PT5	Transmit electrical specifications	51.6	Electrical and timing specifications	XSBI:M	Yes [ ] N/A[ ]

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51.10.4.3 PMA receive functions

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	Deserialization and transmissions of datagroup to PMA client	51.3.2		M	Yes [ ]
PR2	Order of reception	51.4.1	Bit xsbi_rx<15> shall be received first	M	Yes [ ]
PR3	LVDS electrical compliance	51.5	conformance to TIA/EIA644 LVDS specifications and to Table 51–5	XSBI:M	Yes [ ] N/A:[ ]
PR4	Transmit electrical specifications	51.7	Electrical and timing specifications	XSBI:M	Yes [ ] N/A[ ]
PR5	Valid PMA_RX_CLK	51.7.2	A valid clock is provided as defined in Table 51–12	XSBI:M	Yes [ ] N/A[ ]
PR6	PMA_RX_CLK pulse width during valid and invalid transitions	51.7.2	Clock pulse width is greater than or equal to the period times the duty cycle	XSBI:M	Yes [ ] N/A[ ]

51.10.4.4 PMA delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Maximum delay for PMA/ PMD functions	51.3.3	Meets the requirements of the respective PMD clause	M	Yes [ ]

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52. Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-S (short wavelength serial), 10GBASE-L (long wavelength serial), and 10GBASE-E (extra long wavelength serial)

52.1 Overview

This clause specifies the PMDs and baseband media, including both single and multimode optical fiber, for the following 10GBASE serial PHYs, shown in Table 52–1.

Table 52–1—10GBASE serial PHYs

Name	Description
10GBASE-SR	850 nm serial LAN PHY
10GBASE-LR	1310 nm serial LAN PHY
10GBASE-ER	1550 nm serial LAN PHY
10GBASE-SW	850 nm serial WAN PHY
10GBASE-LW	1310 nm serial WAN PHY
10GBASE-EW	1550 nm serial WAN PHY

In order to form a complete Physical Layer, each PMD is combined with the appropriate physical sublayers indicated in Table 52–2 and optionally with the management functions that may be accessible through the management interface defined in Clause 45.

Table 52–2—PMD type and associated clauses

Associated clause	10GBASE-R	10GBASE-W
46—RS	Required	Required
46—XGMII	Optional	Optional
47—XGXS and XAUI	Optional	Optional
49—Type R PCS	Required	Required
50—WIS	N/A	Required
51—Serial PMA	Required	Required

Figure 52–1 depicts the relationships of the serial PMD (shown shaded) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

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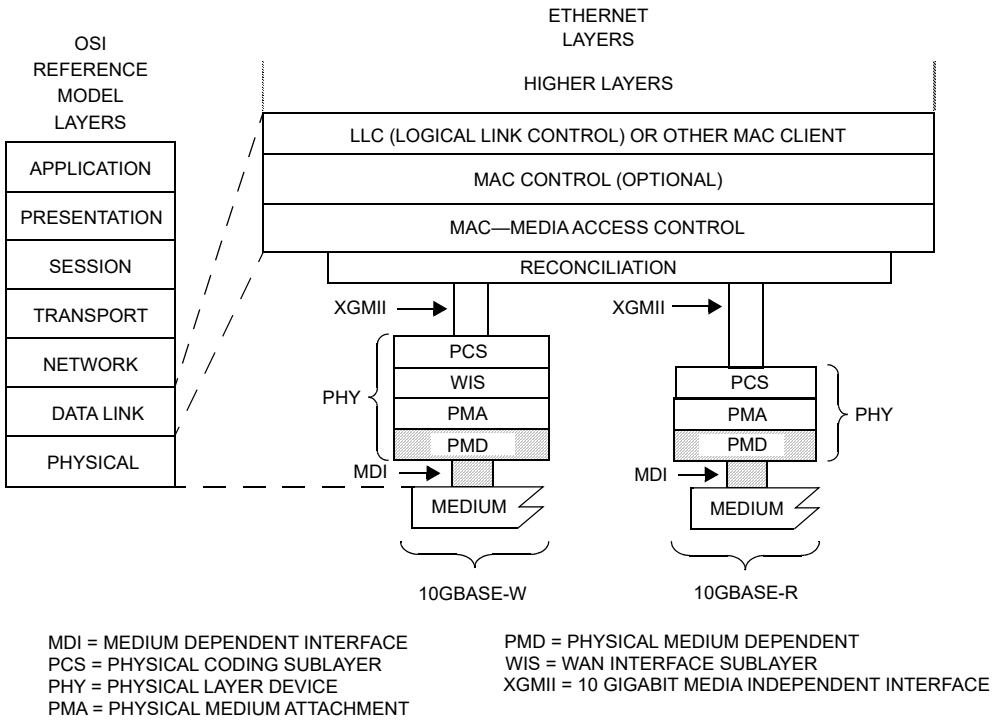

Figure 52–1—10GBASE-S, -L, and -E PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

52.1.1 Physical Medium Dependent (PMD) sublayer service interface

The following specifies the services provided by the 10GBASE-R and 10GBASE-W PMDs. These PMD sublayer service interfaces are described in an abstract manner and do not imply any particular implementation.

The PMD Service Interface supports the exchange of encoded and scrambled 64B/66B blocks between the PMA and PMD entities. In the case of the 10GBASE-W PMD types, these blocks are framed and scrambled by the WIS as described in Clause 50. The PMD translates the serialized data of the PMA to and from signals suitable for the specified medium.

The following primitives are defined:

PMD_UNITDATA.request

PMD_UNITDATA.indication

PMD_SIGNAL.indication

NOTE—Primitives are described in 1.2.2.

52.1.1.1 PMD_UNITDATA.request

This primitive defines the transfer of a serial data stream from the PMA to the PMD.

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52.1.1.1.1 Semantics of the service primitive

PMD_UNITDATA.request(tx_bit)

The data conveyed by PMD_UNITDATA.request is a continuous stream of bits. The tx_bit parameter can take one of two values: ONE or ZERO.

52.1.1.1.2 When generated

The PMA continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal 10.3125 GBd signaling speed for 10GBASE-R PMD types and 9.95328 GBd signaling speed for 10GBASE-W PMDs.

52.1.1.1.3 Effect of receipt

Upon receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals on the MDI.

52.1.1.2 PMD_UNITDATA.indication

This primitive defines the transfer of data (in the form of serialized data) from the PMD to the PMA.

52.1.1.2.1 Semantics of the service primitive

PMD_UNITDATA.indication(rx_bit)

The data conveyed by PMD_UNITDATA.indication is a continuous stream of bits. The rx_bit parameter can take one of two values: ONE or ZERO.

52.1.1.2.2 When generated

The PMD continuously sends stream of bits to the PMA corresponding to the signals received from the MDI.

52.1.1.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

52.1.1.3 PMD_SIGNAL.indication

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

52.1.1.3.1 Semantics of the service primitive

PMD_SIGNAL.indication(SIGNAL_DETECT)

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting light at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication(rx_bit) is undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that PMD_UNITDATA.indication(rx_bit) is known good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the 10^{-12} BER objective.

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52.1.1.3.2 When generated

The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT. If the MDIO interface is implemented, then PMD_global_signal_detect shall be continuously set to the value of SIGNAL_DETECT.

52.1.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

52.2 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation. The PMA and PMD shall incur a round-trip delay (transmit and receive) of not more than 512 bit-times, or 1 pause_quantum, including 2 m of fiber. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 44.3.

52.3 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control variables to PMD control variables as shown in Table 52–3, and MDIO status variables to PMD status variables as shown in Table 52–4.

Table 52–3—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
Global Transmit Disable	Transmit disable register	1.9.0	PMD_global_transmit_disable

Table 52–4—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD Receive signal detect	Receive signal detect register	1.10.0	PMD_global_signal_detect

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52.4 PMD functional specifications

The 10GBASE-R and 10GBASE-W PMDs perform the Transmit and Receive functions that convey data between the PMD service interface and the MDI.

52.4.1 PMD block diagram

For purposes of system conformance, the PMD sublayer is standardized at test points TP2 and TP3 as shown in Figure 52–2. The optical transmit signal is defined at the output end of a patch cord (TP2), between 2 and 5 m in length, of a type consistent with the link type connected to the transmitter. Unless specified otherwise, all transmitter measurements and tests defined in 52.9 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) connected to the receiver. Unless specified otherwise, all receiver measurements and tests defined in 52.9 are made at TP3.

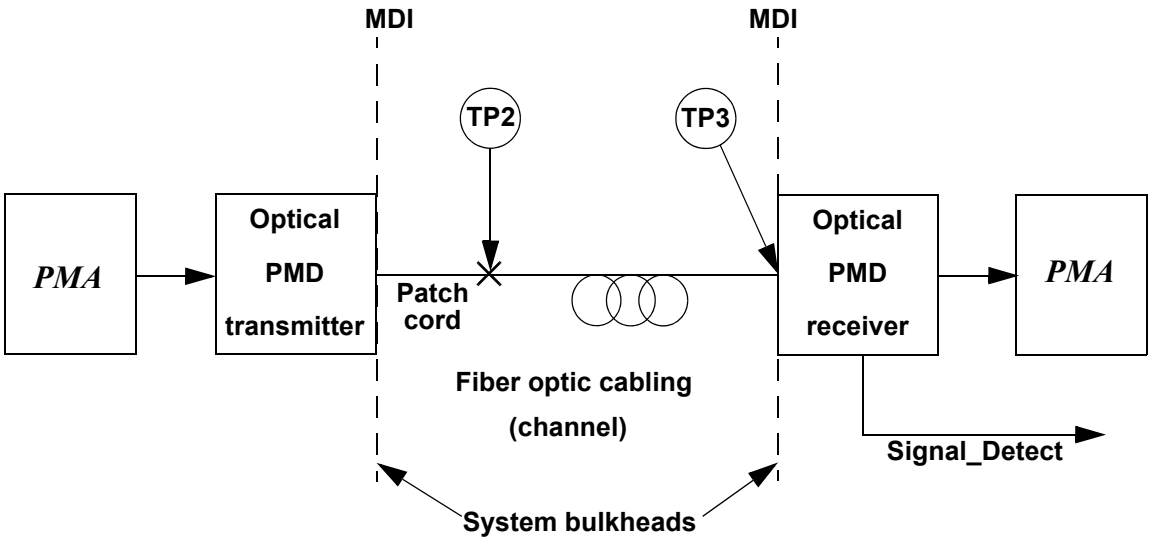

Figure 52–2—Block diagram

52.4.2 PMD Transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the optical specifications in this clause. The higher optical power level shall correspond to tx_bit = ONE.

52.4.3 PMD Receive function

The PMD Receive function shall convey the bits received from the MDI according to the optical specifications in this clause to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). The higher optical power level shall correspond to rx_bit = ONE.

52.4.4 PMD Signal Detect function

The PMD Signal Detect function shall report to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT) which is signaled continuously. PMD_SIGNAL.indication is intended to be an indicator of optical signal presence. If the MDIO interface is implemented, then

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PMD_global_signal_detect (1.10.0) shall be continuously set to the value of SIGNAL_DETECT as described in 45.2.1.9.7.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 52–5. The PMD receiver is not required to verify whether a compliant 10GBASE-R or 10GBASE-W signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD due to cross talk, power supply noise, etc.

Table 52–5—SIGNAL_DETECT value definition

Receive conditions	Signal Detect value
Input_optical_power ≤ -30 dBm average power	FAIL
Input_optical_power ≥ Receiver sensitivity (max) in OMA in Table 52–9, Table 52–13, or Table 52–17 AND compliant 10GBASE-R or 10GBASE-W signal input	OK
All other conditions	Unspecified

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

52.4.5 PMD_reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

52.4.6 PMD_fault function

If the MDIO is implemented, PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault and any other implementation specific fault.

52.4.7 PMD_global_transmit_disable function

The PMD_global_transmit_disable function is optional. When asserted, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of OFF Transmitter in Table 52–7, Table 52–12, or Table 52–16.

If a PMD_transmit_fault (optional) is detected, then the PMD_global_transmit_disable function should also be asserted.

If the MDIO interface is implemented, then this function shall map to the PMD_global_transmit_disable bit as specified in 45.2.1.8.7.

NOTE—PMD Transmit Disable 0 is not used for serial PMDs.

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52.4.8 PMD_transmit_fault function

The PMD_transmit_fault function is optional. The faults detected by this function are implementation specific, but should not include the assertion of the PMD_global_transmit_disable function.

If a PMD_transmit_fault (optional) is detected, then the PMD_global_transmit_disable function should also be asserted.

If the MDIO interface is implemented, then this function shall be mapped to the PMD_transmit_fault bit as specified in 45.2.1.7.4.

52.4.9 PMD_receive_fault function

The PMD_receive_fault function is optional. PMD_receive_fault is the logical OR of NOT SIGNAL_DETECT and any implementation specific fault.

If the MDIO interface is implemented, then this function shall contribute to PMA/PMD receive fault bit as specified in 45.2.1.7.5.

52.5 PMD to MDI optical specifications for 10GBASE-S

The operating ranges for 10GBASE-S are defined in Table 52–6. A 10GBASE-S compliant PMD supports multimode fiber media types listed in Table 52–6 according to the specifications defined in 52.14. A PMD that exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a 400 MHz km 50 μm solution operating at 80 m meets the operating range requirement of 2 m to 66 m).

Table 52–6—10GBASE-S operating range for each optical fiber type

Fiber type	Minimum modal bandwidth @ 850 nm (MHz•km)	Operating range (m)
62.5 μm MMF	160	2 to 26
	200	2 to 33
50 μm MMF	400	2 to 66
	500	2 to 82
	2000	2 to 300
	4700	2 to 400

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52.5.1 10GBASE-S transmitter optical specifications

The 10GBASE-S transmitter shall meet the specifications defined in Table 52–7 per measurement techniques defined in 52.9. It shall also meet the center wavelength, maximum spectral width and minimum optical modulation amplitude as defined in Table 52–8.

Table 52–7—10GBASE-S transmit characteristics

Description	10GBASE-SW	10GBASE-SR	Unit
Signaling speed (nominal)	9.95328	10.3125	GBd
Signaling speed variation from nominal (max)	± 20	± 100	ppm
Center wavelength (range)	840 to 860		nm
RMS spectral width[a] (max)	See footnote[b]		
Average launch power (max)	See footnote[c]		
Average launch power[d] (min)	–7.3		dBm
Launch power (min) in OMA	See footnote[b]		
Average launch power of OFF transmitter[e] (max)	–30		dBm
Extinction ratio (min)	3		dB
$RIN_{12}OMA$ (max)	–128		dB/Hz
Optical Return Loss Tolerance (max)	12		dB
Encircled flux	See footnote[f]		
Transmitter eye mask definition[g] A {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}		
Transmitter eye mask definition[g] B {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5×10^{-5} per sample	{0.235, 0.395, 0.45, 0.235, 0.265, 0.4}		
Transmitter and dispersion penalty[h] (max)	3.9		dB

[a]RMS spectral width is the standard deviation of the spectrum.
[b]Trade-offs are available between spectral width, center wavelength and minimum optical modulation amplitude. See Figure 52–3 and Table 52–8.
[c]The 10GBASE-S launch power shall be the lesser of the Hazard Level 1 safety limit as defined by 52.10.2 or the average receive power (max) defined by Table 52–9.
[d]Average launch power (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[e]Examples of an OFF transmitter are: no power supplied to the PMD, laser shutdown for safety conditions, activation of a PMD_global_transmit_disable or other optional transmitter shut down conditions.
[f]The encircled flux at 19 μm shall be greater than or equal to 86% and the encircled flux at 4.5 μm shall be less than or equal to 30% when measured into Type A1a (50/125 μm multimode) fiber per IEC 61280-1-4:2009.
[g]Either transmitter eye mask definition A or B may be used. A transmitter is not required to comply with both definitions.
[h]TDP(max) and OMA(min) are at the respective wavelength and spectral width as specified in Table 52–8.

The tradeoffs between center wavelength, maximum RMS spectral width and minimum optical modulation amplitude are defined in Table 52–8 and are shown graphically in the illustrative Figure 52–3. In Table 52–8 the minimum optical modulation amplitude (dBm) allowed by this standard is given for the various ranges of center wavelength and spectral width.

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Table 52–8—Minimum 10GBASE-S optical modulation amplitude (dBm) as a function of center wavelength and spectral width

Center wavelength (nm)	RMS Spectral width (nm)								
	Up to 0.05	0.05 to 0.1	0.1 to 0.15	0.15 to 0.2	0.2 to 0.25	0.25 to 0.3	0.3 to 0.35	0.35 to 0.4	0.4 to 0.45
840 to 842	–4.2	–4.2	–4.1	–4.1	–3.9	–3.8	–3.5	–3.2	–2.8
842 to 844	–4.2	–4.2	–4.2	–4.1	–3.9	–3.8	–3.6	–3.3	–2.9
844 to 846	–4.2	–4.2	–4.2	–4.1	–4.0	–3.8	–3.6	–3.3	–2.9
846 to 848	–4.3	–4.2	–4.2	–4.1	–4.0	–3.8	–3.6	–3.3	–2.9
848 to 850	–4.3	–4.2	–4.2	–4.1	–4.0	–3.8	–3.6	–3.3	–3.0
850 to 852	–4.3	–4.2	–4.2	–4.1	–4.0	–3.8	–3.6	–3.4	–3.0
852 to 854	–4.3	–4.2	–4.2	–4.1	–4.0	–3.9	–3.7	–3.4	–3.1
854 to 856	–4.3	–4.3	–4.2	–4.1	–4.0	–3.9	–3.7	–3.4	–3.1
856 to 858	–4.3	–4.3	–4.2	–4.1	–4.0	–3.9	–3.7	–3.5	–3.1
858 to 860	–4.3	–4.3	–4.2	–4.2	–4.1	–3.9	–3.7	–3.5	–3.2

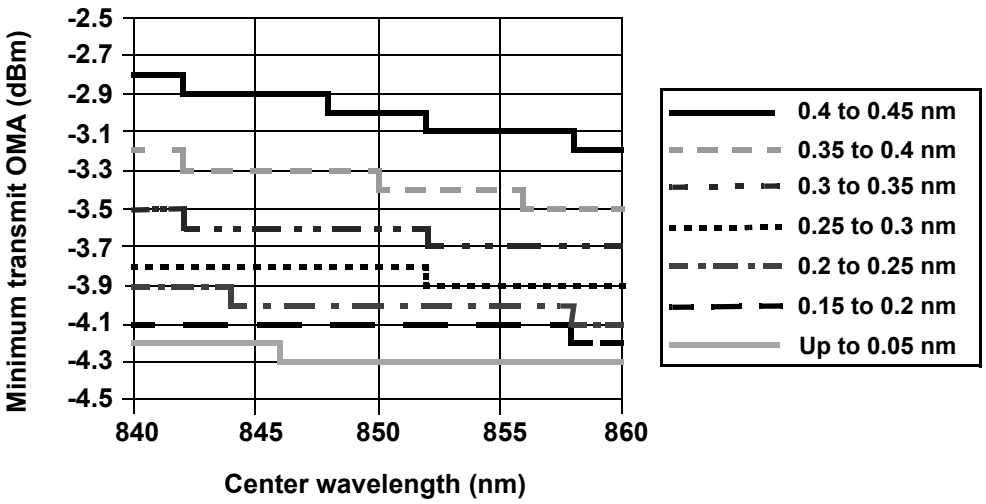

Figure 52–3—Illustration of triple tradeoff curve for 10GBASE-S

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52.5.2 10GBASE-S receive optical specifications

The 10GBASE-S receiver shall meet the specifications defined in Table 52–9 per measurement techniques defined in 52.9.

Table 52–9—10GBASE-S receive characteristics

Description	10GBASE-SW	10GBASE-SR	Unit
Signaling speed (nominal)	9.95328	10.3125	GBd
Signaling speed variation from nominal (max)	± 20	± 100	ppm
Center wavelength (range)	840 to 860		nm
Average receive power[a] (max)	–1.0		dBm
Average receive power[b] (min)	–9.9		dBm
Receiver sensitivity (max) in OMA[c]	0.077 (–11.1)		mW (dBm)
Receiver Reflectance (max)	–12		dB
Stressed receiver sensitivity in OMA[d] [e](max)	0.18 (–7.5)		mW (dBm)
Vertical eye closure penalty[f] (min)	3.5		dB
Stressed eye jitter[g] (min)	0.3		UI pk-pk
Receive electrical 3 dB upper cutoff frequency (max)	12.3		GHz

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having a power level equal to the average receive power (max) plus at least 1 dB.
[b]Average receive power (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity is optional.
[d]Measured with conformance test signal at TP3 (see 52.9.9.3) for BER = 10^{-12}.
[e]The stressed sensitivity values in the table are for system level BER measurements which include the effects of CDR circuits. It is recommended that at least 0.4 dB additional margin be allocated if component level measurements are made without the effect of CDR circuits
[f]Vertical eye closure penalty is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.
[g]Stressed eye jitter is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.

52.5.3 Illustrative 10GBASE-S link power budgets

Example power budgets and penalties for a 10GBASE-S channel are shown in Table 52–10.

52.6 PMD to MDI optical specifications for 10GBASE-L

The operating range for 10GBASE-L PMDs is defined in Table 52–11. A 10GBASE-L compliant PMD supports Types B1.1 and B1.3 single-mode fibers according to the specifications defined in 52.14. A PMD that exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., operating at 12.5 km meets the minimum range requirement of 2 m to 10 km).

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Table 52–10—10GBASE-S link power budgets[a,b]

Parameter	62.5 μm MMF		50 μm MMF				Unit
Modal bandwidth as measured at 850 nm	160	200	400	500	2000	4700	MHz•km
Power budget	7.3	7.3	7.3	7.3	7.3	7.3	dB
Operating distance	26	33	66	82	300	400	m
Channel insertion loss[c, d]	1.6	1.6	1.7	1.8	2.6	2.9	dB
Allocation for penalties	4.7	4.8	5.1	5.0	4.7	4.4	dB
Additional insertion loss allowed[e]	1.0	0.8	0.5	0.5	0.0	0.0	dB

[a]Budget numbers are rounded to nearest 0.1 dB.
[b]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[c]Operating distances used to calculate the channel insertion loss are the maximum values specified in Table 52–6.
[d]The specifications for a wavelength of 840 nm and a spectral width of 0.29 nm in Table 52–8 is used to calculate channel insertion loss, allocation for penalties, and additional insertion loss allowed.
[e]This portion of the link budget is permitted to be used to overcome insertion loss higher than the "Channel insertion loss" value and in some cases may be less than the value shown.

Table 52–11—10GBASE-L operating range

PMD Type	Nominal Wavelength (nm)	Minimum range
10GBASE-L	1310	2 m to 10 km

52.6.1 10GBASE-L transmitter optical specifications

The 10GBASE-L transmitter shall meet the specifications defined in Table 52–12 per measurement techniques defined in 52.9.

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Table 52–12—10GBASE-L transmit characteristics

Description	10GBASE-LW	10GBASE-LR	Unit
Signaling speed (nominal)	9.95328	10.3125	GBd
Signaling speed variation from nominal (max)	± 20	± 100	ppm
Center wavelength (range)	1260 to 1355		nm
Side Mode Suppression Ratio (min)	30		dB
Average launch power (max)	0.5		dBm
Average launch power[a] (min)	–8.2		dBm
Launch power (min) in OMA minus TDP[b]	–6.2		dBm
Optical Modulation Amplitude[c] (min)	–5.2		dBm
Transmitter and dispersion penalty (max)	3.2		dB
Average launch power of OFF transmitter[d] (max)	–30		dBm
Extinction ratio (min)	3.5		dB
$RIN_{12}OMA$ (max)	–128		dB/Hz
Optical Return Loss Tolerance (max)	12		dB
Transmitter Reflectance[e] (max)	–12		dB
Transmitter eye mask definition[f] A {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}		
Transmitter eye mask definition[f] B {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5×10^{-5} per sample	{0.235, 0.395, 0.45, 0.235, 0.265, 0.4}		

[a]Average launch power (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]TDP is transmitter and dispersion penalty.
[c]Even if the TDP < 1 dB, the OMA(min) has to exceed this value.
[d]Examples of an OFF transmitter are: no power supplied to the PMD, laser shutdown for safety conditions, activation of a PMD_global_transmit_disable or other optional transmitter shut down conditions.
[e]Transmitter reflectance is defined looking into the transmitter.
[f]Either transmitter eye mask definition A or B may be used. A transmitter is not required to comply with both definitions.

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52.6.2 10GBASE-L receive optical specifications

The 10GBASE-L receiver shall meet the specifications defined in Table 52–13 per measurement techniques defined in 52.9.

Table 52–13—10GBASE-L receive characteristics

Description	10GBASE-LW	10GBASE-LR	Unit
Signaling speed (nominal)	9.95328	10.3125	GBd
Signaling speed variation from nominal (max)	± 20	± 100	ppm
Center wavelength (range)	1260 to 1355		nm
Average receive power[a] (max)	0.5		dBm
Average receive power[b] (min)	–14.4		dBm
Receiver sensitivity (max) in OMA[c]	0.055 (–12.6)		mW (dBm)
Receiver Reflectance (max)	–12		dB
Stressed receiver sensitivity (max) in OMA[d, e]	0.093 (–10.3)		mW (dBm)
Vertical eye closure penalty[f] (min)	2.2		dB
Stressed eye jitter[g] (min)	0.3		UI pk-pk
Receive electrical 3 dB upper cutoff frequency (max)	12.3		GHz

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having a power level equal to the average receive power (max) plus at least 1 dB.
[b]Average receive power (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity is optional.
[d]Measured with conformance test signal at TP3 (see 52.9.9.3) for BER = 10^{-12}.
[e]The stressed sensitivity values in the table are for system level BER measurements, which include the effects of CDR circuits. It is recommended that at least 0.4 dB additional margin be allocated if component level measurements are made without the effect of CDR circuits.
[f]Vertical eye closure penalty is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.
[g]Stressed eye jitter is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.

52.6.3 Illustrative 10GBASE-L link power budgets

An example power budget and penalties for a 10GBASE-L channel are shown in Table 52–14.

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Table 52–14—10GBASE-L link power budget[a,b]

Parameter	10GBASE-L	Unit
Power budget	9.4	dB
Operating distance	10	km
Channel insertion loss[c, d]	6.2	dB
Allocation for penalties	3.2	dB
Additional insertion loss allowed	0.0	dB

[a]Budget numbers are rounded to nearest 0.1 dB.
[b]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[c]The channel insertion loss is calculated using the maximum distance specified in Table 52–11 and cabled optical fiber attenuation of 0.4 dB/km at 1310 nm plus an allocation for connection and splice loss given in 52.14.2.1.
[d]A transmitter wavelength of 1260 nm with a TDP of 3 dB is used to calculate channel insertion loss, and allocation for penalties in this table.

52.7 PMD to MDI optical specifications for 10GBASE-E

The operating range for 10GBASE-E PMDs is defined in Table 52–15. A 10GBASE-E compliant PMD supports Types B1.1 and B1.3 single-mode fibers according to the specifications defined in 52.14. A PMD which exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., operating at 42.5 km meets the minimum range requirement of 2 m to 30 km).

Table 52–15—10GBASE-E operating range

PMD Type	Nominal Wavelength (nm)	Minimum Range
10GBASE-E	1550	2 m to 30 km
		2 m to 40 km[a]

[a]Links longer than 30 km for the same link power budget are considered engineered links. Attenuation for such links needs to be less than the minimum specified for B1.1 or B1.3 single-mode fiber.

Link attenuation requirements are specified in 52.14.3.

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52.7.1 10GBASE-E transmitter optical specifications

The 10GBASE-E transmitter shall meet the specifications defined in Table 52–16 per measurement techniques defined in 52.9.

Table 52–16—10GBASE-E transmit characteristics

Description	10GBASE-EW	10GBASE-ER	Unit
Signaling speed (nominal)	9.95328	10.3125	GBd
Signaling speed variation from nominal (max)	± 20	± 100	ppm
Center wavelength (range)	1530 to 1565		nm
Side Mode Suppression Ratio (min)	30		dB
Average launch power (max)	4.0		dBm
Average launch power[a] (min)	–4.7		dBm
Launch power (min) in OMA minus TDP[b]	–2.1		dBm
Average launch power of OFF transmitter[c] (max)	–30		dBm
Optical Modulation Amplitude[d] (min)	–1.7		dBm
Transmitter and dispersion penalty (max)	3.0		dB
Extinction ratio (min)	3		dB
$RIN_{21}OMA$[e] (max)	–128		dB/Hz
Optical Return Loss Tolerance (max)	21		dB
Transmitter eye mask definition[f] A {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}		
Transmitter eye mask definition[f] B{X1, X2, X3, Y1, Y2, Y3} Hit ratio 5×10^{-5} per sample	{0.235, 0.395, 0.45, 0.235, 0.265, 0.4}		

[a]Average launch power (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]TDP is transmitter and dispersion penalty.
[c]Examples of an OFF transmitter are: no power supplied to the PMD, laser shutdown for safety conditions, activation of a PMD_global_transmit_disable or other optional transmitter shut-down conditions.
[d]Even if the TDP < 0.4 dB, the OMA(min) has to exceed this value.
[e]RIN measurement is made with a return loss at 21 dB.
[f]Either transmitter eye mask definition A or B may be used. A transmitter is not required to comply with both definitions.

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52.7.2 10GBASE-E receive optical specifications

The 10GBASE-E receiver shall meet the specifications defined in Table 52–17 per measurement techniques defined in 52.9.

Table 52–17—10GBASE-E receive characteristics

Description	10GBASE-EW	10GBASE-ER	Unit
Signaling speed (nominal)	9.95328	10.3125	GBd
Signaling speed variation from nominal (max)	± 20	± 100	ppm
Center wavelength (range)	1530 to 1565		nm
Average receive power (max)	–1.0		dBm
Average receive power[a] (min)	–15.8		dBm
Maximum receive power (for damage)	4.0		dBm
Receiver sensitivity (max) in OMA[b]	0.039 (–14.1)		mW (dBm)
Receiver Reflectance (max)	–26		dB
Stressed receiver sensitivity (max) in OMA[c,d]	0.074 (-11.3)		mW (dBm)
Vertical eye closure penalty[e] (min)	2.7		dB
Stressed eye jitter (min)[f]	0.3		UI pk-pk
Receive electrical 3 dB upper cutoff frequency (max)	12.3		GHz

[a]Average receive power (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]Receiver sensitivity is optional.
[c]Measured with conformance test signal at TP3 (see 52.9.9.3) for BER = 10^{-12}.
[d]The stressed sensitivity values in the table are for system level BER measurements which include the effects of CDR circuits. It is recommended that at least 0.4 dB additional margin be allocated if component level measurements are made without the effects of CDR circuits.
[e]Vertical eye closure penalty is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.
[f]Stressed eye jitter is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.

52.7.3 Illustrative 10GBASE-E link power budgets

Example power budgets and penalties for a 10GBASE-E channel are shown in Table 52–18.

52.8 Jitter specifications for 10GBASE-R and 10GBASE-W

Acceptable transmitted jitter is achieved by compliance with 52.9.7, transmitter optical waveform, and 52.9.10, transmitter and dispersion penalty. Tolerance to received jitter is achieved by compliance to 52.9.9, stressed receiver conformance, which includes sinusoidal jitter as in the following subclause. There is no jitter transfer specification.

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Table 52–18—10GBASE-E link power budgets[a,b]

Parameter	10GBASE-E		Unit
Power budget	15.0		dB
Operating distance	30	40[c]	km
Channel insertion loss[d, e]	10.9	10.9	dB
Maximum Discrete Reflectance (max)	–26		dB
Allocation for penalties	3.6	4.1	dB
Additional insertion loss allowed	0.5	0.0	dB

[a]Budget numbers are rounded to nearest 0.1 dB.
[b]Link penalties are built into the transmitter specifications by testing the PMD with a maximum dispersion fiber.
[c]Links longer than 30 km are considered engineered links. Attenuation for such links needs to be less than that guaranteed by B1.1 or B1.3 single-mode fiber.
[d]Operating distances used to calculate the channel insertion loss are the maximum values specified in Table 52–15
[e]A wavelength of 1565 nm and 3dB transmitter and dispersion penalty (TDP) is used to calculate channel insertion loss, and allocation for penalties.

52.8.1 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. Sinusoidal jitter may vary over a magnitude range as required to accurately calibrate a stressed eye per 52.9.9. The range is limited by the constraints of Table 52–19.

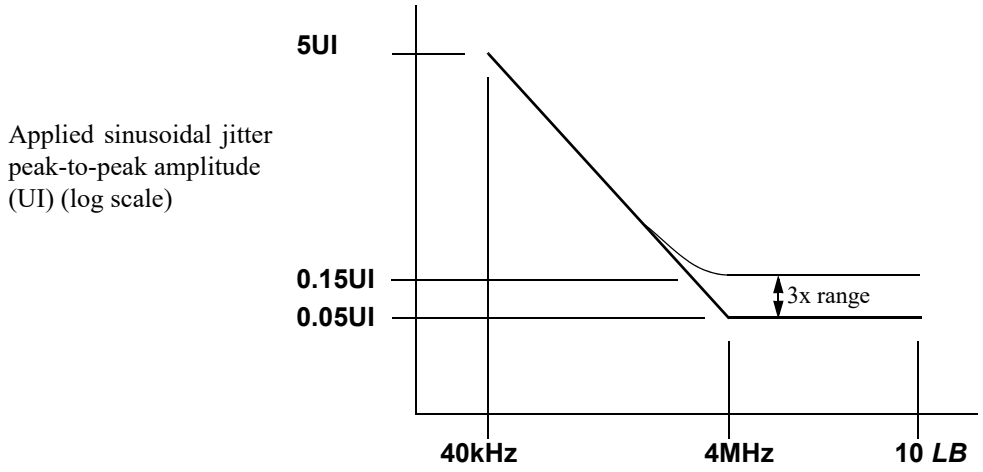

Figure 52–4—Illustration of the mask of the sinusoidal component of jitter tolerance

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Table 52–19—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter ($UI_{pk\ to\ pk}$)
$f < 40$kHz	NA
40 kHz $< f \leq$ 4MHz	2×10^5 Hz $/ f + S - 0.05$[a]
4 MHz $< f <$ 10 LB[b]	$0.05 \leq S \leq 0.15$ [a]

[a]S is the magnitude of sine jitter actually used in the calibration of the stressed eye per the methods of 52.9.9.3.
[b]LB = Loop Bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

52.9 Optical measurement requirements

All optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

52.9.1 Test patterns

Compliance is to be achieved in normal operation. Two types of test pattern are used, square wave (52.9.1.2) and other (52.9.1.1). Test patterns are as in Table 52–22 for 10GBASE-R and in 50.3.8 for 10GBASE-W unless specified otherwise.

NOTE—Test patterns for specific optical tests are designed to emulate system operation, which would entail passing valid 10GBASE-R or 10GBASE-W data.

52.9.1.1 Test-pattern definition

Patterns 1, 2, and 3 are defined in Table 52–21. Pattern 3 is optional.

For 10GBASE-R, two test pattern segments are specified, in two variants, “normal” (n) and “inverted” (i). Both are 8448 bits long. They may be generated dynamically by the 58 bit scrambler and “control block” sync header generation defined in 49.2.6, and using the scrambler starting seeds specified in Table 52–20 and the method of generation in 49.2.8. The segments are assembled into patterns, each containing four segments, as described in Table 52–21. Each may be held as a static pattern in test equipment, or generated or detected dynamically using the methods of 49.2.8 and 49.2.12 respectively, or otherwise.

Each segment contains a sync header transition every 66 bits.

Table 52–20—Pattern segments

Segments	Seed[57:0][a]
A_n	0x3C8B44DCAB6804F
B_n	0x34906BB85A38884

[a]The “invert” segments A_i and B_i are generated using the inverted seeds for A_n and B_n, respectively.

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Table 52–21—Test patterns

Pattern	Pattern for 10GBASE-R	Pattern for 10GBASE-W
1	$B_n B_i B_n B_i$	Mixed[a]
2	$A_n A_i A_n A_i$	
3	PRBS31[b]	PRBS31[c]

[a]The patterns for 10GBASE-W are defined in 50.3.8.
[b]This is the test-pattern checker defined in 49.2.12.
[c]This is the test-pattern checker defined in 50.3.8.2.

The test pattern 1 is generated with the data input mode programmed to select LF data input. The test pattern 2 is generated with the data input mode programmed to select all zero data input.

Pattern 1 represents typical scrambled data while pattern 2 represents a less typical pattern that could happen by chance and is thought to be more demanding of the transmission process including the clock recovery subsystem. Both patterns are balanced over their length of 33 792 bits.

NOTE—While other test methods and patterns could be used it is the implementer's responsibility to ensure that measurements carried out with the specified patterns achieve the requirements specified.

Table 52–22—Test-pattern definitions and related subclauses

Test	Pattern	Related subclause
Average optical power	1 or 3	52.9.3
OMA (modulated optical power)	Square	52.9.5
Extinction ratio	1 or 3	52.9.4
Transmit eye	1 or 3	52.9.7
Receive upper cutoff frequency	1 or 3	52.9.11
$RIN_x OMA$	Square	52.9.6
Wavelength, spectral width	1 or 3	52.9.2
Side mode suppression ratio	1 or 3	52.9.2
Vertical eye closure penalty calibration	2 or 3	52.9.9
Receiver sensitivity	1 or 3	52.9.9
Receiver overload	1 or 3	—
Stressed receive conformance	2 or 3	52.9.9
Transmitter and dispersion penalty	2 or 3	52.9.10

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52.9.1.2 Square wave pattern definition

A pattern consisting of four to eleven consecutive ones followed by an equal run of zeros may be used as a square wave. These patterns have fundamental frequencies between approximately 452 MHz (10GBASE-W) and 1289 MHz (10GBASE-R).

52.9.2 Center wavelength, spectral width, and side mode suppression ratio (SMSR) measurements

The center wavelength, spectral width (RMS), and SMSR shall be measured using an optical spectrum analyzer per the centroidal wavelength, RMS spectral width, and SMSR definitions in IEC 61280-1-3 under modulated conditions using an appropriate PRBS or a valid 10GBASE-R or 10GBASE-W signal, OC-192 signal, STM-64 signal, or another representative test pattern.

52.9.3 Average optical power measurements

Average optical power shall be measured using the methods specified in IEC 61280-1-1 or ANSI/TIA/EIA-455-95. This measurement may be made with the node transmitting test pattern 1 or 3 or a valid 10GBASE-R or 10GBASE-W signal, OC-192 signal, STM-64 signal, or another representative test pattern.

52.9.4 Extinction ratio measurements

Extinction ratio shall be measured using the methods specified in IEC 61280-2-2. This parameter is to be assured during system operation. However, measurements with an appropriate PRBS ($2^{23} – 1$ or $2^{31} – 1$) or a valid 10GBASE-R or 10GBASE-W or OC-192c or STM-64 signal will give equivalent results.

52.9.5 Optical modulation amplitude (OMA) test procedure

OMA is the difference in optical power for the nominal “1” and “0” levels of the optical signal, OMA in Figure 52–6, using waveform averaging or histogram means. OMA should be measured for a node transmitting the square wave pattern defined in 52.9.1.

The recommended technique for measuring optical modulation amplitude is illustrated in Figure 52–5. Optionally, a fourth-order Bessel-Thomson filter as specified in 52.9.7 can be used after the O/E converter. The measurement system consisting of the O/E converter, the optional filter and the oscilloscope has the following requirements:

a) The bandwidth of the measurement system shall be at least 3/T where T is the time at high or low (00001111 giving approximately T = 400 ps and 7.5 GHz as an example); and
b) The measurement system is calibrated at the appropriate wavelength for the transmitter under test.

With the device under test transmitting the square wave described above, use the following procedure to measure optical modulation amplitude:

c) Configure the test equipment as illustrated in Figure 52–5.
d) Measure the mean optical power P_1 of the logic “1” as defined over the center 20% of the time interval where the signal is in the high state. (See Figure 52–6.)
e) Measure the mean optical power P_0 of the logic “0” as defined over the center 20% of the time interval where the signal is in the low state. (See Figure 52–6.)
f) $OMA = P_1 – P_0$.

A method of approximating OMA is shown in Figure 52–11.

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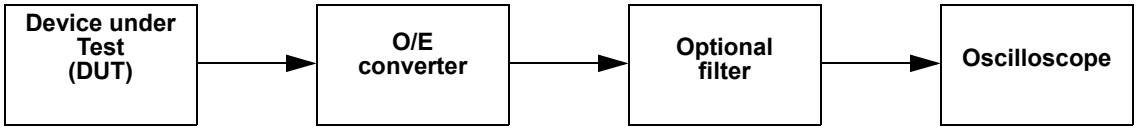

Figure 52–5—Recommended test equipment for measurement of optical modulation amplitude

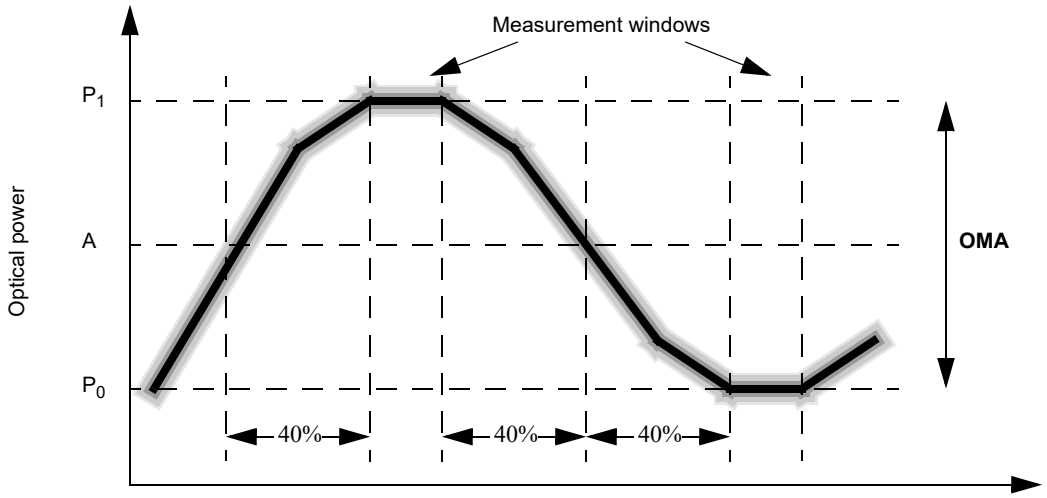

Figure 52–6—Optical modulation amplitude waveform measurement

52.9.6 Relative intensity noise optical modulation amplitude (RIN_xOMA) measuring procedure

This procedure describes a component test that may not be appropriate for a system level test depending on the implementation. If used, the procedure shall be performed as described in 52.9.6.1, 52.9.6.2, and 52.9.6.3.

52.9.6.1 General test description

The test arrangement is shown in Figure 52–7. The optical path between the device under test (DUT) and the detector has a single discrete reflection with the specified optical return loss as seen by the DUT.

Both the OMA power and noise power are measured by AC-coupling the O/E converter into the high-frequency electrical power meter. If needed, an amplifier may be used to boost the signal to the power meter. A low-pass filter is used between the photodetector and the power meter to limit the noise measured to the passband appropriate to the data rate of interest. In order to measure the noise, the modulation to the DUT is turned off.

52.9.6.2 Component descriptions

Optical path: The optical path and detector combination is configured for a single dominant reflection with an optical return loss specified in Table 52–7 for 10GBASE-S, Table 52–12 for 10GBASE-L, and Table 52–16 for 10GBASE-E. (The optical return loss may be determined by the method of FOTP-107.) The length of the test cable is not critical but should be in excess of 2 m.

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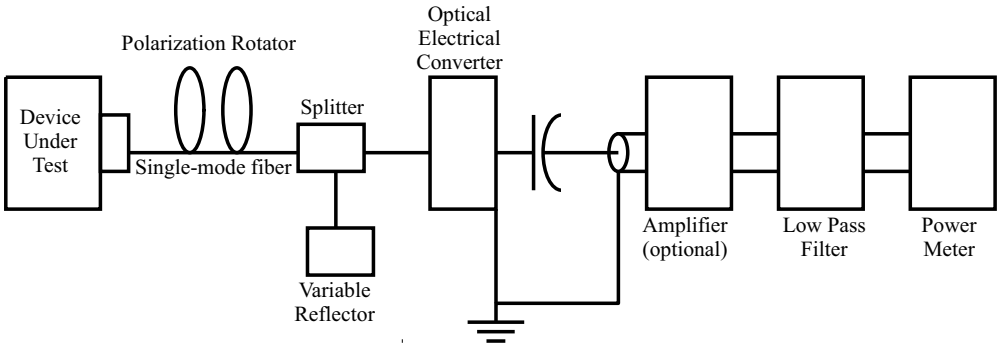

Figure 52–7—RIN$_x$OMA measurement setup

Polarization rotator: The polarization rotator is required to be capable of transforming an arbitrary orientation elliptically polarized wave into a fixed orientation linearly polarized wave.

O/E converter (and amplifier): If necessary, the noise may be amplified to a level consistent with accurate measurement by the power meter.

Filter: The upper –3 dB limit of the measurement apparatus is to be approximately equal to the bit rate (i.e., 10 GHz). The total filter bandwidth used in the RIN calculation is required to take the low-frequency cutoff of the DC-blocking capacitor into consideration. The low-frequency cutoff is recommended to be less than 1 MHz.

The filter should be placed in the circuit as the last component before the power meter so that any high-frequency noise components generated by the detector/amplifier are eliminated. If the power meter used has a very wide bandwidth, care should be taken to ensure that the filter does not lose its rejection at extremely high frequencies.

Power meter: The RMS electrical power meter should be capable of being zeroed in the absence of input optical power to remove any residual noise.

52.9.6.3 Test Procedure

Use the following procedure to test relative intensity noise optical modulation amplitude:

a) With the DUT disconnected, zero the power meter;
b) Connect the DUT, turn on the laser, and ensure that the laser is not modulated;
c) Operate the polarization rotator while observing the power meter output to maximize the noise read by the power meter. Note the maximum power, P_N;
d) Turn on the modulation to the laser using the square wave pattern of 52.9.1 and note the power measurement, P_M. It may be necessary to change or remove the effective reflection to obtain an accurate reading;
e) Calculate RIN from the observed electrical signal power and noise power by use of Equation (52–1).

$$RIN_xOMA = 10\log\frac{P_N}{BW \times P_M} \text{ (dB/Hz)} \quad (52–1)$$

where:

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RIN_xOMA= Relative Intensity Noise referred to optical modulation amplitude measured with x dB reflection,

P_N = Electrical noise power in watts with modulation off,

P_M = Electrical power in watts with modulation on,

BW = Low-pass bandwidth of filter – high-pass bandwidth of DC-blocking capacitor [noise bandwidth of the measuring system (Hz)].

For testing multimode components or systems, the polarization rotator is removed from the setup and the single-mode fiber replaced with a multimode fiber. Step c) of the test procedure is eliminated.

52.9.7 Transmitter optical waveform

The required transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 52–8. Compliance is to be assured during system operation. However, measurements with pattern 3 or 1 defined in 52.9.1, or other patterns such as a 2^{23}– 1 PRBS or a valid 10GBASE-R, or 10GBASE-W, or OC-192c, or STM-64 signal are likely to give very similar results. Measurements should be made as defined by IEC 61280-2-2 with the eye mask definition A coordinates, or as defined by 86.8.3.2 with the eye mask definition B coordinates. The two sets of coordinates (A and B) are given in Table 52–7, Table 52–12 or Table 52–16 as appropriate. A transmitter is not required to comply with both definitions. Measurement at 10.3125 GBd shall qualify for 10GBASE-W and 10GBASE-R use, measurement at 9.95328 GBd shall qualify for 10GBASE-W use only.

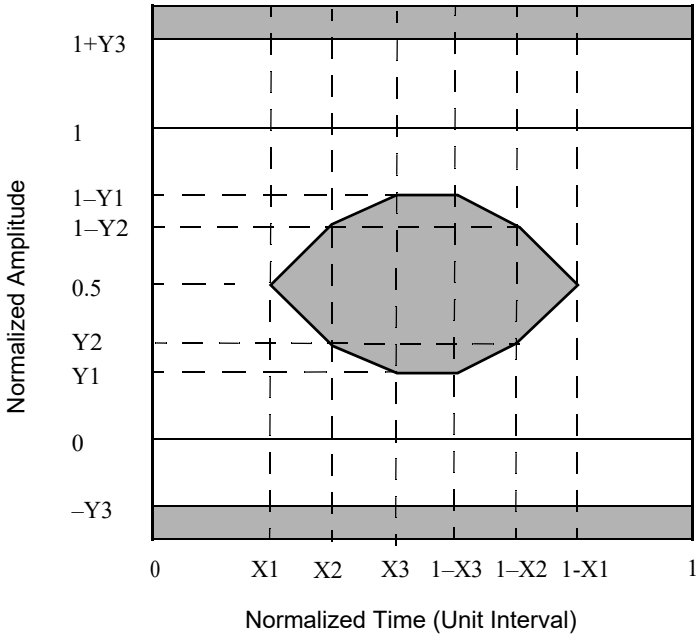

Figure 52–8—Transmitter eye mask definition

Normalized amplitudes of 0.0 and 1.0 represent the amplitudes of logic ZERO and ONE respectively. Normalized times of 0 and 1 on the unit interval scale are to be determined by the eye crossing means measured at the average value of the optical eye pattern.

A clock recovery unit (CRU) should be used to trigger the scope for mask measurements as shown in Figure 52–9. It should have a high-frequency corner bandwidth of less than or equal to 4 MHz and a slope of –20 dB/decade.

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The eye shall be measured with respect to the mask of the eye using a receiver with a fourth-order Bessel-Thomson response having a transfer function given by Equation (52–2) and Equation (52–3):

$$H(y) = \frac{105}{105 + 105y + 45y^2 + 10y^3 + y^4} \tag{52–2}$$

where:

$$y = 2.114p\ ; \quad p = \frac{j\omega}{\omega_r}\ ; \quad \omega_r = 2\pi f_r\ ; \quad f_r = 7.5\text{GHz} \tag{52–3}$$

and where the filter response vs. frequency range for this fourth-order Bessel-Thomson receiver is defined in ITU-T G.691, along with the allowed tolerances (STM-64 values) for its physical implementation.

This Bessel-Thomson receiver is not intended to represent the noise filter used within a compliant optical receiver, but is intended to provide uniform measurement conditions at the transmitter.

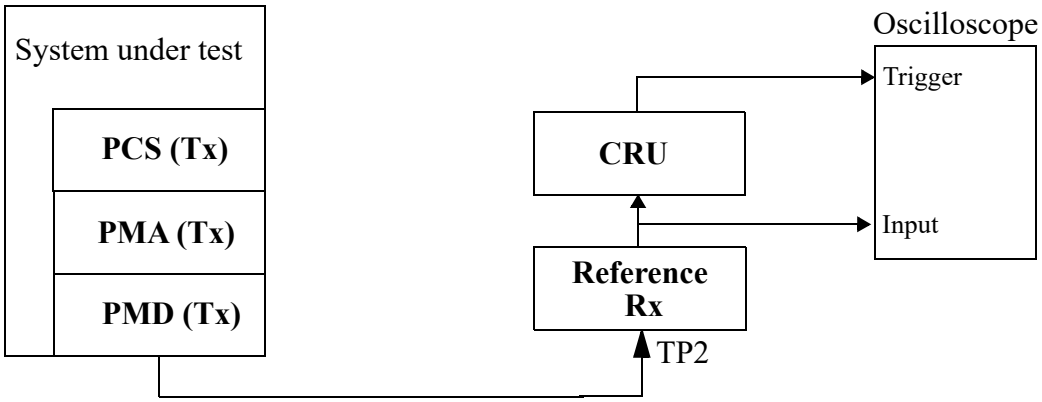

Figure 52–9—Transmitter optical waveform test block diagram

The fourth-order Bessel-Thomson filter is reactive. In order to suppress reflections, a 6 dB attenuator may be required at the filter input and/or output.

52.9.8 Receiver sensitivity measurements

Receiver sensitivity, which is defined for an ideal input signal, is optional and testing is not required. If measured, the test signal should have negligible impairments such as intersymbol interference (ISI), rise/fall times, jitter and RIN. Instead, the normative requirement for receivers is stressed receiver sensitivity. Stressed sensitivity is measured with a conditioned input signal where both vertical eye closure and jitter have been added according to 52.9.9.

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52.9.9 Stressed receiver conformance test

Stressed receiver tolerance testing shall be performed in accordance with the requirements of 52.9.9.1, 52.9.9.2, 52.9.9.3, and 52.9.9.4.

Receivers have to operate with BER less than 10^{-12} when tested with a conditioned input signal that combines vertical eye closure and jitter according to this clause.

The measurements in this subclause are performed with asynchronous data flowing out of the optical transmitter of the system under test. The output data pattern from the transmitter of the system under test is to be the same pattern defined for this measurement in 52.9.1.

52.9.9.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 52–10. A suitable pattern generator is used to continuously generate a signal or test pattern according to 52.9.1. The optical test signal is conditioned (stressed) using the methodology, as defined in 52.9.9.3, while applying sinusoidal jitter, as defined in 52.8.1. The receiver of the system under test is tested for conformance by enabling the error counter on the receiving side. As defined in section 49.2.12 and 50.3.8, the PCS or WIS is capable of detecting the data pattern and reporting any errors received. The optical power penalty for the stressed eye is intended to be similar to its vertical eye closure penalty. This is not necessarily the same as the highest TDP anticipated in service, but represents a standardized test condition for the receiver.

A suitable test set is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics. The test fiber called out for LW/LR and EW/ER and the transversal filter called out for SW/SR are not needed to characterize the receiver input signal; nor are they used during testing.

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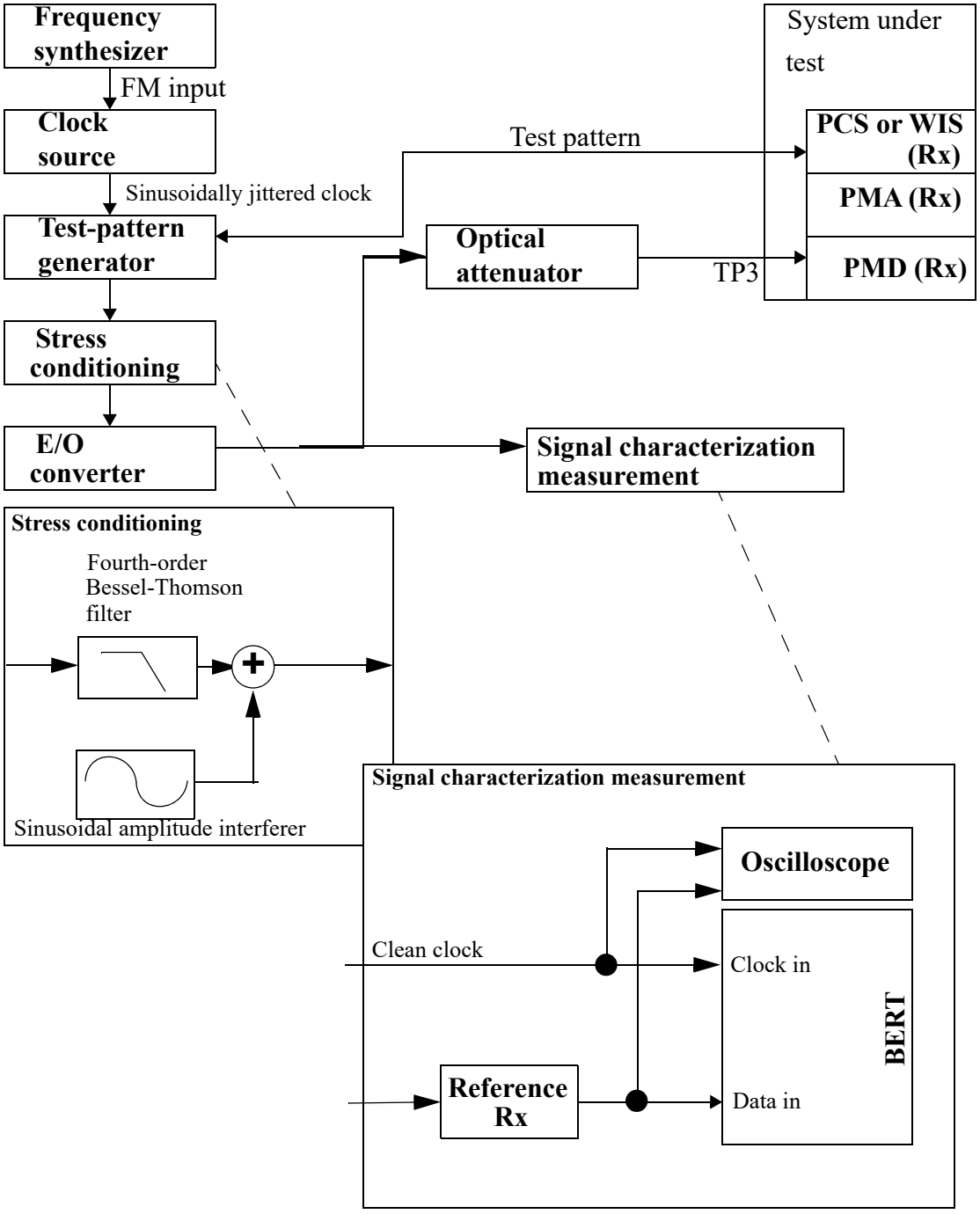

Figure 52–10—Stressed receiver conformance test block diagram

The fourth-order Bessel-Thomson filter is used to create ISI-induced vertical eye closure penalty (VECP). The sinusoidal amplitude interferer causes additional eye closure, but in conjunction with the slowed edge rates from the filter, also causes jitter. The nature of the jitter is intended to emulate instantaneous bit shrinkage that can occur with DDJ. This type of jitter cannot be created by simple phase modulation. The sinusoidal phase modulation represents other forms of jitter and also verifies that the receiver under test can

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track low-frequency jitter. The frequency of the sinusoidal interference may be set at any frequency between 100 MHz and 2 GHz, although be careful to avoid a harmonic relationship between the sinusoidal interference, the sinusoidal jitter, the data rate and the pattern repetition rate.

For improved visibility for calibration, it is imperative that the Bessel-Thomson filter and all other elements in the signal path (cables, DC blocks, E/O converter, etc.) have wide and smooth frequency response and linear phase response throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be minimized. If this is achieved, then data dependent effects should be minimal, and short data patterns can be used for calibration with the benefit of providing much improved trace visibility on sampling oscilloscopes. Actual patterns for testing the receiver shall be as specified in Table 52–22.

To further improve visibility for calibration, random noise effects, such as RIN and random clock jitter, should also be minimized. A small amount of residual noise and jitter from all sources is unavoidable, but should be less than 0.25 UI peak-peak of jitter at the 10^{-12} points.

The Bessel-Thomson filter and the E/O converter should have the appropriate frequency response to result in the appropriate level of initial ISI eye closure before the sinusoidal terms are added. The E/O converter should be fast and linear such that the waveshape and edge rates are predominantly controlled or limited by the electrical circuitry. Electrical summing requires high linearity of all elements including the E/O converter. Summing with an optical coupler after the E/O converter is an option that eases linearity requirements, but requires a second source for the interfering signal, will complicate settings of extinction ratio, and will add more RIN.

The vertical and horizontal eye closures to be used for receiver conformance testing are verified using an optical reference receiver with a 7.5 GHz fourth order ideal Bessel-Thomson response. Use of G.691 tolerance filters may significantly degrade this calibration. Care should be taken to ensure that all the light from the fiber is collected by the fast photodetector and that there is negligible mode selective loss, especially in the optical attenuator and the optical coupler, if used.

The clock output from the clock source in Figure 52–10 will be modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye jitter that includes the sinusoidal jitter component, a separate clock source (clean clock of Figure 52–10) is required that is synchronized to the source clock, but not modulated with the jitter source.

52.9.9.2 Parameter definitions

The primary parameters of the conformance test signal are vertical eye closure penalty (VECP) and stressed eye jitter, J. Vertical eye closure penalty is measured at the time center of the eye (halfway between 0 and 1 on the unit interval scale as defined in 52.9.7) and is calculated relative to the measured OMA value. J is defined from the 0.5th to the 99.5th percentile of the jitter histogram. J is measured at the average optical power, which can be obtained with AC-coupling. The values of these components are defined by their histogram results.

The vertical eye closure penalty is given by Equation (52–4).

$$\text{Vertical eye closure penalty [dB, optical]} = 10 \times \log\frac{OMA}{A_O} \tag{52–4}$$

where:

A_O is the amplitude of the eye opening from the 99.95th percentile of the lower histogram to the 0.05th percentile of the upper histogram, and

OMA is the normal amplitude without ISI, as shown in Figure 52–11.

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52.9.9.3 Stressed receiver conformance test signal characteristics and calibration

The conformance test signal is used to validate that the PMD receiver meets BER requirements with near worst case waveforms including pulse width shrinkage, power, simulated channel penalties, and a swept frequency sinusoidal jitter contribution applied at TP3.

Signal characteristics are described below along with a suggested approach for calibration.

The test signal includes vertical eye closure and high-probability jitter components. For this test, these two components are defined by peak values that include all but 0.1% for VECP and all but 1% for jitter of their histograms. Histograms should include at least 10 000 hits, and should be about 1%-width in the direction not being measured. Residual low-probability noise and jitter should be minimized—that is, the outer slopes of the final histograms should be as steep as possible down to very low probabilities.

The following steps describe a suggested method for calibrating a stressed eye generator:

1) Set the signaling speed of the test-pattern generator to satisfy the requirements of 52.5.2, 52.6.2, or 52.7.2.
2) Turn on the calibration pattern. A short pattern may be used for calibration if the conditions described in 52.9.9.1 are met, but this increases the risk that the longer test pattern used during testing will overstress the device under test. In any case, a pattern shorter than PRBS10 is not recommended.
3) Set the extinction ratio to approximately the Extinction Ratio (min) value given in 52.5.1, 52.6.1, or 52.7.1. Sinusoidal interference and jitter signals should be turned off at this point. If optical summing is used, the extinction ratio may need to be adjusted after the sinusoidal interference signal is added below.
4) Measure the OMA of the test signal (without attenuation). OMA is measured per the method in 52.9.5 using the square wave pattern.
5) The requirements for vertical eye closure and jitter of the stressed eye test signal are given by the Vertical eye closure penalty (VECP) and Stressed eye jitter (J) values given in Table 52–9 for 10GBASE-S, Table 52–13 for 10GBASE-L, or Table 52–17 for 10GBASE-E.

   There are three components involved in calibration for vertical closure and J. These are a linear phase filter, sinusoidal interference, and sinusoidal jitter.

   Without sinusoidal jitter or sinusoidal interference, greater than two thirds of the vertical eye closure penalty value should be created by use of a linear phase, low jitter filter (such as Bessel-Thomson). The filter should be tested with the prescribed test patterns to verify that residual jitter and baseline wander are small, not to exceed 0.25 UI peak-peak. If not, the stress may be more than desired, leading to conservative results. However, compensation is not allowed. Once done, revert to the calibration pattern, if different than the final test pattern specified in Table 52–22.

   Any remaining vertical eye closure required has to be created with sinusoidal interference or sinusoidal jitter.

   Sinusoidal jitter (phase modulation) has to be added per the template of Table 52–19. For calibration purposes, sinusoidal jitter frequencies should be well within the flat portion of the template greater than 4 MHz.

   Iterate the settings for sinusoidal interference and/or jitter until all constraints are met, including jitter (J), vertical closure (VECP), and that sinusoidal jitter above 4 MHz is as specified in Table 52–19.

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Verify that the optical power penalty for the stressed eye (relative to the reference transmitter per 52.9.10) is greater than or equal to VECP.

To emulate the effects of DCD or data-dependent jitter, at least 5 ps peak-peak of pulse shrinkage jitter should have been achieved.

6) Decrease the amplitude with the optical attenuator until the OMA complies with the OMA values given in Table 52–9 for 10GBASE-S, Table 52–13 for 10GBASE-L, Table 52–17 for 10GBASE-E. If high linearity exists, then the sinusoidal interference should not change the OMA value. OMA can be approximated with histograms as suggested in Figure 52–11. However, the normative definition for OMA is as given in 52.9.5.

7) For testing, turn on the actual required test pattern(s) per 52.9.1.

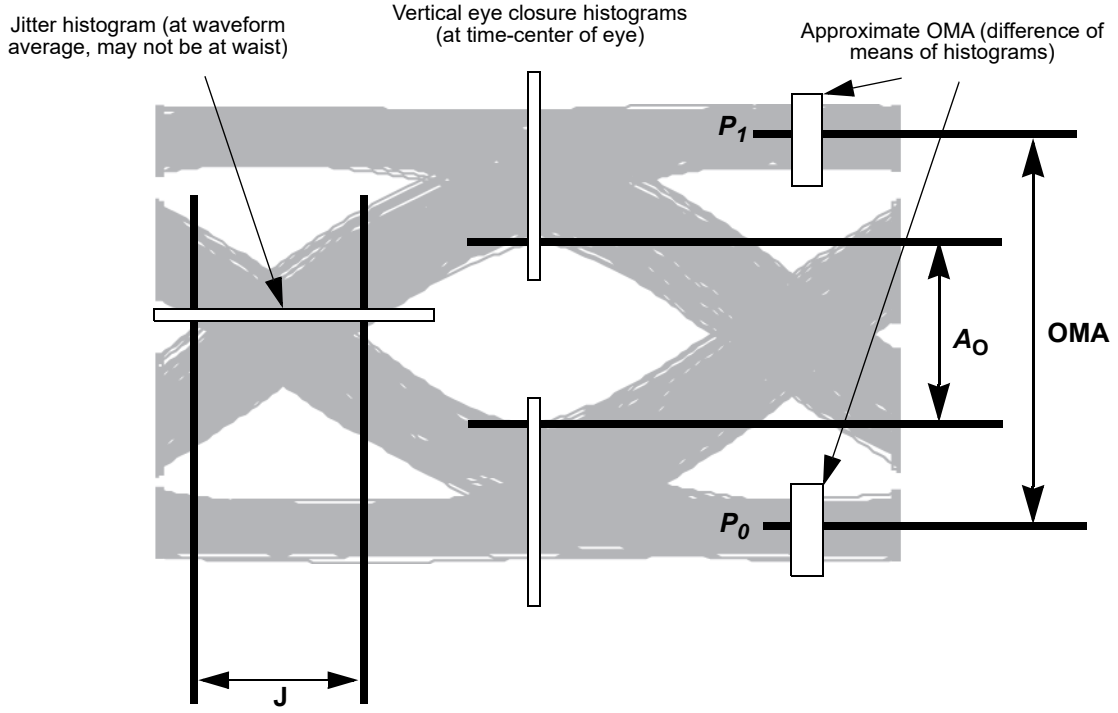

Figure 52–11—Required characteristics of the conformance test signal at TP3

Care should be taken when characterizing the signal used to make receiver tolerance measurements. In the case of a transmit jitter measurement, excessive and/or uncalibrated noise/jitter in the test system makes it more difficult to meet the specification and may have a negative impact on yield but will not effect interoperability. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. Care should be taken to minimize and/or correct for the noise/jitter introduced by the reference receiver, filters, oscilloscope, and BERT. While the details of measurement and test equipment are beyond the scope of this standard it is recommended that the implementer fully characterize the test equipment and apply appropriate guard bands to ensure that the receive input signal meets the specified requirements.

52.9.9.4 Stressed receiver conformance test procedure

The test apparatus is set up as described in 52.9.9.1, 52.9.9.2 and 52.9.9.3. The sinusoidal jitter is then stepped across the frequency and amplitude range specified in 52.8.1 while monitoring BER at the receiver. The BER is to be compliant for all jitter frequencies. This method does not result in values for jitter

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contributed by the receiver. It does, however, guarantee that a receiver meeting the requirements of this test will operate with the worst-case optical input.

52.9.10 Transmitter and dispersion penalty measurement

The transmitter and dispersion penalty (TDP) measurement tests for transmitter impairments with chromatic effects for a transmitter to be used with single-mode fiber, and for transmitter impairments with modal (not chromatic) dispersion effects for a transmitter to be used with multimode fiber.

The setup for measurement of transmitter and dispersion penalty is shown in Figure 52–12 and consists of a reference transmitter, the transmitter under test, a controlled optical reflection, an optical attenuator, a test fiber, a reference receiver, a transversal filter for 10GBASE-S, and a bit-error ratio tester. For 10GBASE-S, the polarization rotator shown in Figure 52–12 is removed from the setup and the single-mode fiber replaced with a multimode fiber. All BER and sensitivity measurements are made with the test patterns in 52.9.1.

52.9.10.1 Reference transmitter requirements

The reference transmitter is a high-quality instrument-grade device, which can be implemented by a CW laser modulated by a high-performance modulator. It should meet the following basic requirements:

a) The rise/fall times should be less than 30 ps at 20% to 80%.
b) The output optical eye is symmetric and passes the eye mask test of 52.9.7.
c) In the center 20% region of the eye, the worst case vertical eye closure penalty as defined in 52.9.9.3 is less than 0.5 dB.
d) Jitter less than 0.20 UI peak-peak.
e) RIN should be minimized to less than –136 dB/Hz

52.9.10.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 52–23.

Table 52–23—Transmitter compliance channel specifications

PMD Type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c] (max)
	Minimum	Maximum		
10GBASE-S	N/A	N/A	Minimum	See ORLT in Table 52–7
10GBASE-L	$0.2325 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.2325 \cdot \lambda \cdot [1 – (1300 / \lambda)^4]$	Minimum	21 dB
10GBASE-E	0 (maximum)	$0.93 \cdot \lambda \cdot [1 – (1300 / \lambda)^4]$	Minimum	See ORLT in Table 52–16

[a]The dispersion is measured for the wavelength of the device under test. The coefficient assumes 10 km for 10GBASE-L and 40 km for 10GBASE-E.
[b]There is no intent to stress the sensitivity of the BERT's optical receiver.
[c]The optical return loss is applied at TP2.

A 10GBASE-L/E transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 52–23 for the

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wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel for 10GBASE-S is a 2 m to 5 m patch cord meeting the requirements in Table 52–25.

The channel provides a maximum optical return loss specified in Table 52–23. The state of polarization of the back reflection is adjusted to create the greatest RIN. The methods of 52.9.6.2 and 52.9.6.3 may be used.

52.9.10.3 Reference receiver requirements

The reference receiver should have the bandwidth given in 52.9.7. The sensitivity of the reference receiver should be limited by Gaussian noise. The receiver should have minimal threshold offset, deadband, hysteresis, baseline wander, deterministic jitter or other distortions. Decision sampling should be instantaneous with minimal uncertainty and setup/hold properties.

The nominal sensitivity of the reference receiver, S, is measured in OMA using the set up of Figure 52–12 without the test fiber and with the transversal filter removed. The sensitivity S has to be corrected for any significant reference transmitter impairments including any vertical eye closure. It should be measured while sampling at the eye center or corrected for off-center sampling. It is calibrated at the wavelength of the transmitter under test.

For all transmitter and dispersion penalty measurements, determination of the center of the eye is required. Center of the eye is defined as the time halfway between the left and right sampling points within the eye where the measured BER is greater than or equal to 1×10^{-3}.

For 10GBASE-S the reference receiver is followed by a transversal filter with two equal amplitude paths with a differential delay of 55 ps. For 10GBASE-L/E the transversal filter is not used.

The clock recovery unit (CRU) used in the TDP measurement has a corner frequency of less than or equal to 4 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low-frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.

52.9.10.4 Test procedure

To measure the transmitter and dispersion penalty (TDP) the following procedure shall be used. The decision threshold amplitude is defined to occur at the average signal level. The sampling instant is displaced from the eye center by $\pm$ 0.05 UI. The following procedure is repeated for early and late decision and the larger TDP value is used:

a) Configure the test equipment as described above and illustrated in Figure 52–12.
b) Adjust the attenuation of the optical attenuator to obtain a BER of 1×10^{-12}.
c) Record the optical power in OMA at the input to the reference receiver, P_DUT, in dBm.
d) If P_DUT is larger than S, the transmitter and dispersion penalty (TDP) for the transmitter under test is the difference between P_DUT and S, TDP = P_DUT – S. Otherwise the transmitter and dispersion penalty is zero, TDP = 0.

It is to be ensured that the measurements are made in the linear power regime of the fiber.

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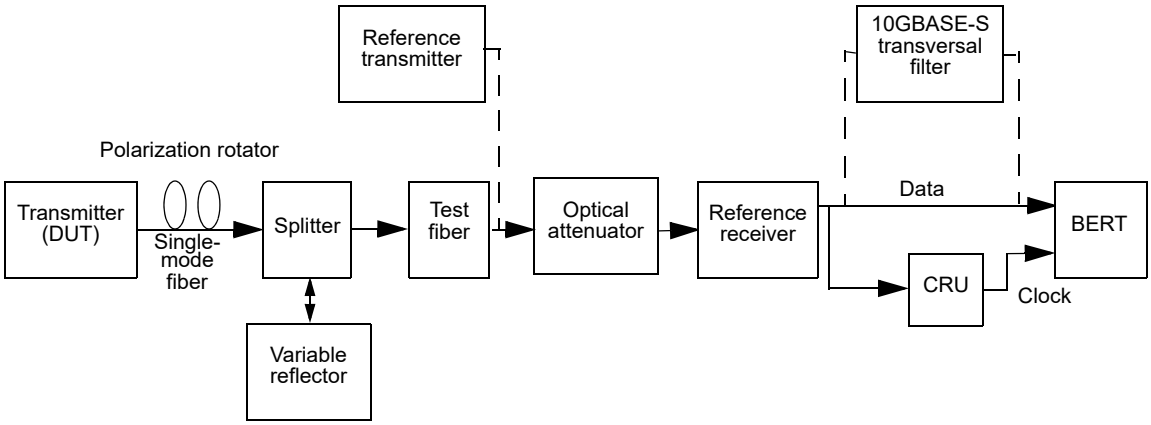

Figure 52–12—Test setup for measurement of transmitter and dispersion penalty

52.9.11 Measurement of the receiver 3 dB electrical upper cutoff frequency

The receiver 3 dB electrical upper cutoff frequency may be measured as described in Figure 52–13 and the list below. The test setup is shown in Figure 52–13. The test uses two optical sources and an optical combiner. One source is modulated by a digital data signal. The other, approximately linear, source is modulated with an analog signal. The analog and digital signals should be asynchronous. The recommended patterns are test patterns 1 or 3 of 52.9.1. An appropriate PRBS or a valid 10GBASE-R or 10GBASE-W signal, OC-192 signal, STM-64 signal, or another representative test pattern may be used.

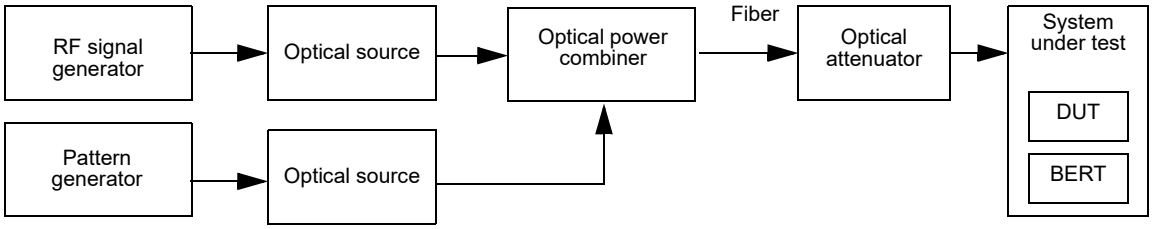

Figure 52–13—Test setup for receiver bandwidth measurement

The 3 dB upper cutoff frequency may be measured using the following steps:

a) Calibrate the frequency response characteristics of the test equipment including the analog radio frequency (RF) signal generator and laser sources. The digital optical source meets the requirements of this clause.

b) Configure the test equipment as shown in Figure 52–13. Take care to minimize changes to the signal path which could affect the system frequency response after the calibration in step a. With the RF modulation turned off, and both optical sources turned on, set the Optical Modulation Amplitude to a level that approximates the stressed receiver sensitivity level in Table 52–9 for 10GBASE-S, Table 52–13 for 10GBASE-L, and Table 52–17 for 10GBASE-E.

c) Turn on the RF modulation while maintaining the same average optical power and OMA established in step b).

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d) Measure the necessary RF modulation amplitude (in electrical dBm) required to achieve a constant BER (e.g., 10^{-8}) for a number of frequencies.

e) The receiver 3 dB electrical upper cutoff frequency is that frequency where the corrected RF modulation amplitude (the measured amplitude in "d" corrected with the calibration data in "a") increases by 3 dB (electrical).

52.10 Environmental specifications

52.10.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

52.10.2 Laser safety

10GBASE-R and 10GBASE-W optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation is required to explicitly define requirements and usage restrictions on the host system necessary to meet these safety certifications.[99]

52.10.3 Installation

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

52.11 Environment

Normative specifications in this clause shall be met by a system integrating a 10GBASE-R or 10GBASE-W over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

52.11.1 Electromagnetic emission

A system integrating a 10GBASE-R or 10GBASE-W PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

[99]A host system that fails to meet the manufacturers requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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52.11.2 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

52.12 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 10GBASE-ER).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 52.10.2.

52.13 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 52–14.

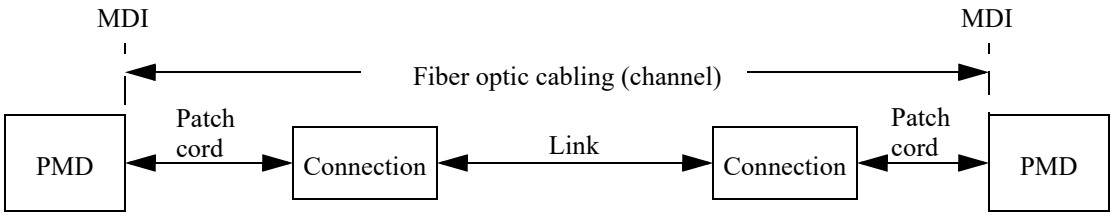

Figure 52–14—Fiber optic cabling model

The channel insertion loss is given in Table 52–24. A channel may contain additional connectors or other optical elements as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, polarization mode dispersion and modal bandwidth meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1 one-cord method, and IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

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Table 52–24—Fiber optic cabling (channel)

Description	62.5 μm MMF		50 μm MMF				Type B1.1, B1.3 SMF			Unit
Nominal wavelength	**850[a]**						**1310[b]**	**1550**		**nm**
Modal bandwidth (min)	**160**	**200**	**400**	**500**	**2000**	**4700**	**N/A**	**N/A**		**MHz•km**
Operating distance (max)	26 m	33 m	66 m	82 m	300 m	400 m	10 km	30 km	40 km	
Channel insertion loss (max) [c,d,e]	2.6	2.5	2.2	2.3	2.6	2.9	6.0	11.0[f]		dB
Channel insertion loss (min)	0	0	0	0	0	0	0	5		dB
Dispersion (max)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	546	728	ps/nm
DGD_max[g]	N/A	N/A	N/A	N/A	N/A	N/A	10	19		ps
Optical return loss	N/A	N/A	N/A	N/A	N/A	N/A	N/A	21		dB

[a]Channel insertion loss at 850 nm includes cable, connectors, and splices.
[b]Channel insertion loss at 1310 nm includes cable, connectors, and splices.
[c]These channel insertion loss numbers are based on the nominal wavelength.
[d]Operating distances used to calculate channel insertion loss are those listed in this table.
[e]Maximum attenuation given in Table 52–25.
[f]Channel insertion loss at 1550 nm includes cable, connectors and splices.
[g]Differential Group Delay (DGD) is the time difference between the fractions of a pulse that are transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

52.14 Characteristics of the fiber optic cabling (channel)

The 10GBASE-R and 10GBASE-W fiber optic cabling shall meet the specifications defined in Table 52–24. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

52.14.1 Optical fiber and cable

The fiber optic cable shall meet the requirements of IEC 60793-2 or the requirements of Table 52–25 where they differ for fiber types A1a (50/125 μm multimode), A1b (62.5/125 μm multimode), B1.1 (dispersion un-shifted single mode), or B1.3 (low water peak single mode).

NOTE—It is believed that for 10GBASE-E, type B4 fiber with positive dispersion may be substituted for B1.1 or B1.3. A link using B4 fiber with negative dispersion should be validated for compliance at TP3.

52.14.2 Optical fiber connection

An optical fiber connection, as shown in Figure 52–14, consists of a mated pair of optical connectors.

52.14.2.1 Connection insertion loss

The insertion loss is specified for a connection, which consists of a mated pair of optical connectors.

The maximum link distances for multimode fiber are calculated based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an insertion loss

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Table 52–25—Optical fiber and cable characteristics

Description	62.5 μm MMF	50 μm MMF		Type B1.1, B1.3 SMF		Unit
Nominal fiber specification wavelength	**850**	**850**		**1310**	**1550**	**nm**
Cabled optical fiber attenuation (max)	3.5	3.5		0.4[a] or 0.5[b]	see footnote[c]	dB/km
Modal Bandwidth (min)	160[d] or 200[d]	400[d] or 500[d] or 2000[e]	4700[f]	N/A		MHz km
Zero dispersion wavelength (λ_0)	$1320 \le \lambda_0 \le 1365$	$1295 \le \lambda_0 \le 1320$[g]	$1295 \le \lambda_0 \le 1340$[f]	$1300 \le \lambda_0 \le 1324$		nm
Dispersion slope (max) (S_0)	0.11 for $1320 \le \lambda_0 \le 1348$ and $0.001(1458-\lambda_0)$ for $1348 \le \lambda_0 \le 1365$	0.11 for $1300 \le \lambda_0 \le 1320$ and $0.001(\lambda_0-1190)$ for $1295 \le \lambda_0 \le 1300$[g]	0.105 for $1295 \le \lambda_0 \le 1310$ and $0.000375(1590-\lambda_0)$ for $1310 \le \lambda_0 \le 1340$	0.093		ps / nm^2 km

[a]For the single-mode case, the 0.4 dB/km attenuation for optical fiber cables is defined in ITU-T G.652.
[b]For the single-mode case, the 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3. Using 0.5 dB/km may not support operation at 10 km.
[c]Attenuation for 1550 nm links is based on the fiber channel and is specified in 52.14.3.
[d]Overfilled launch bandwidth per IEC 60793-1-41:2001 or ANSI/TIA/EIA 455-204.
[e]Effective modal bandwidth for fiber meeting IEC 60793-2-10 Type A1a.2 when used with sources meeting the wavelength (range) and encircled flux specifications of Table 52–7.
[f]Effective modal bandwidth, zero dispersion wavelength and dispersion slope for OM4 fibers are specified in IEC 60793-2-10 Type A1a.3.
[g]Cabled optical fiber with 400 or 500 or 2000 MHz km minimum Modal Bandwidth may alternatively comply with the zero dispersion wavelength and dispersion slope specifications for 4700 MHz km minimum Modal Bandwidth fiber.

equal to 0.5 dB (or less) per connection, or two connections (as shown in Figure 52–14) with an insertion loss of 0.75 dB per connection. Connections with different loss characteristics may be used provided the requirements of Table 52–24 are met.

The maximum link distances for single-mode fiber are calculated based on an allocation of 2 dB total connection and splice loss at 1310 nm for 10GBASE-L, and 2 dB for 30 km total connection and splice loss at 1550 nm for 10GBASE-E.

52.14.2.2 Maximum discrete reflectance

The maximum discrete reflectance for 10GBASE-S shall be less than –20 dB.

The maximum discrete reflectance for 10GBASE-L and 10GBASE-E shall be less than –26 dB.

52.14.3 10GBASE-E attenuator management

The 10GBASE-E channel shall have an attenuation between 5 dB and 11 dB. If required, an attenuator can be added to comply with this specification. The ideal channel attenuation is 8 dB. Figure 52–15 graphically shows the compliant region.

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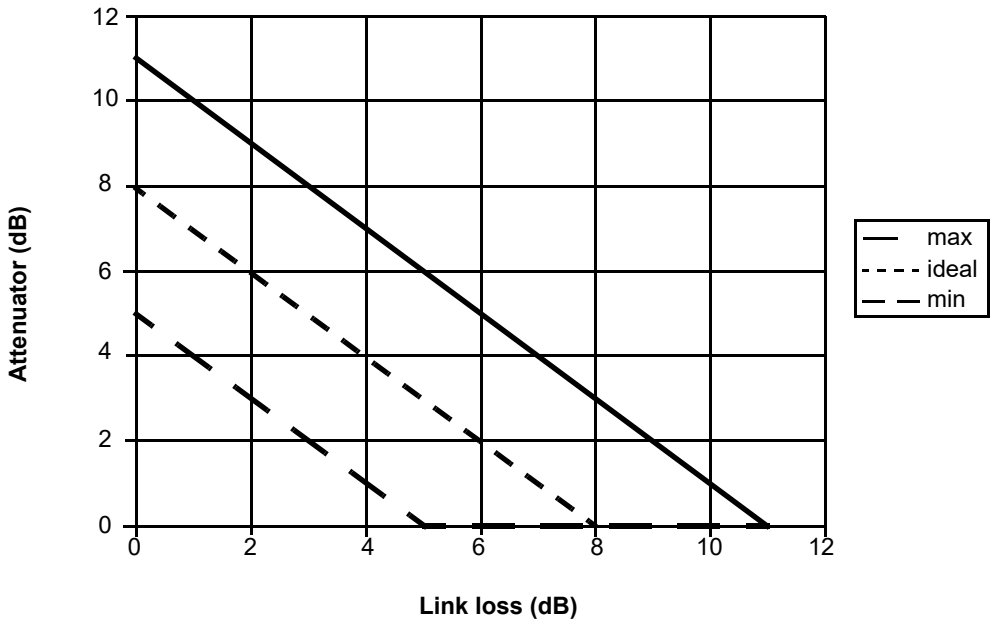

Figure 52–15—10GBASE-E attenuator management (illustrative)

52.14.4 Medium Dependent Interface (MDI) requirements

The 10GBASE-R and 10GBASE-W PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 52–14). Examples of an MDI include the following:

a) Connectorized fiber pigtail.
b) PMD receptacle.

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of the following:

c) IEC 61753-1-1—Fibre optic interconnecting devices and passive component performance standard—Part 1-1: General and guidance—Interconnecting devices (connectors).
d) IEC 61753-021-2—Fibre optic passive components performance standard—Part 021-2: Fibre optic connectors terminated on single-mode fibre for Category C—Controlled environment, performance Class S.
e) IEC 61753-022-2—Fibre optic passive components performance standard—Part 022-2: Fibre optic connectors terminated on multimode fibre for Category C—Controlled environment, performance Class M.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 52.4.1, not at the MDI.

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52.15 Protocol implementation conformance statement (PICS) proforma for Clause 52, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-S (short wavelength serial), 10GBASE-L (long wavelength serial), and 10GBASE-E (extra long wavelength serial)[100]

52.15.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 52, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-R and 10GBASE-W, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

52.15.2 Identification

52.15.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

52.15.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 52, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-R and 10GBASE-W
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[100] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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52.15.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*MD	MDIO capability	52.3	Registers and interface supported	O	Yes [ ] No [ ]
*SR	10GBASE-SR PMD	52.5	Device supports shortwave (850 nm) operation LAN PHY	O	Yes [ ] No [ ]
*LR	10GBASE-LR PMD	52.6	Device supports longwave (1310 nm) operation LAN PHY	O	Yes [ ] No [ ]
*ER	10GBASE-ER PMD	52.7	Device supports extra long wave (1550 nm) operation LAN PHY	O	Yes [ ] No [ ]
*SW	10GBASE-SW PMD	52.5	Device supports shortwave (850 nm) operation WAN PHY	O	Yes [ ] No [ ]
*LW	10GBASE-LW PMD	52.6	Device supports longwave (1310 nm) operation WAN PHY	O	Yes [ ] No [ ]
*EW	10GBASE-EW PMD	52.7	Device supports extra long wave (1550 nm) operation WAN PHY	O	Yes [ ] No [ ]
*INS	Installation / Cable	52.4.1	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
DLY	Delay constraints	52.2	Device conforms to delay constraints	M	Yes [ ]

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52.15.3 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, types 10GBASE-R and 10GBASE-W

52.15.3.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Transmit function	52.4.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FS2	Transmitter optical signal	52.4.2	Higher optical power transmitted is a logic 1	M	Yes [ ]
FS3	Receive function	52.4.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FS4	Receiver optical signal	52.4.3	Higher optical power received is a logic 1	M	Yes [ ]
FS5	Signal detect function	52.4.4	Mapping to PMD service interface	M	Yes [ ]
FS6	Signal detect parameter	52.4.4	Generated according to Table 52–5	M	Yes [ ]

52.15.3.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MD1	Management register set	52.3	As defined in Table 52–3 and Table 52–4	MD:M	Yes [ ] N/A [ ]
MD2	PMD_reset bit	52.4.5	As defined in 45.2.1.1.1	MD:M	Yes [ ] N/A[ ]
MD3	PMD_global_transmit_disable bit	52.4.7	As defined in 45.2.1.8.7	MD:O	Yes [ ] No [ ] N/A [ ]
MD4	PMD_transmit_fault bit	52.4.8	As defined in 45.2.1.7.4	MD:O	Yes [ ] No [ ] N/A [ ]
MD5	PMA/PMD receive fault bit	52.4.9	Contributes to receive fault bit as defined in 45.2.1.7.5	MD:O	Yes [ ] No [ ] N/A [ ]
MD6	PMD_signal_detect bit	52.4.4	As defined in 45.2.1.9.7	MD:M	Yes [ ] N/A [ ]

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52.15.3.3 PMD to MDI optical specifications for 10GBASE-SR

Item	Feature	Subclause	Value/Comment	Status	Support
SR1	10GBASE-SR transmitter	52.5.1	Meets specifications in Table 52–8 and Table 52–7	SR:M	Yes [ ] N/A [ ]
SR2	10GBASE-SR receiver	52.5.2	Meets specifications in Table 52–9	SR:M	Yes [ ] N/A [ ]

52.15.3.4 PMD to MDI optical specifications for 10GBASE-SW

Item	Feature	Subclause	Value/Comment	Status	Support
SW1	10GBASE-SW transmitter	52.5.1	Meets specifications in Table 52–8 and Table 52–7	SW:M	Yes [ ] N/A [ ]
SW2	10GBASE-SW receiver	52.5.2	Meets specifications in Table 52–9	SW:M	Yes [ ] N/A [ ]

52.15.3.5 PMD to MDI optical specifications for 10GBASE-LR

Item	Feature	Subclause	Value/Comment	Status	Support
LR1	10GBASE-LR transmitter	52.6.1	Meets specifications in Table 52–12	LR:M	Yes [ ] N/A [ ]
LR2	10GBASE-LR receiver	52.6.2	Meets specifications in Table 52–13	LR:M	Yes [ ] N/A [ ]

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52.15.3.6 PMD to MDI optical specifications for 10GBASE-LW

Item	Feature	Subclause	Value/Comment	Status	Support
LW1	10GBASE-LW transmitter	52.6.1	Meets specifications in Table 52–12	LW:M	Yes [ ] N/A [ ]
LW2	10GBASE-LW receiver	52.6.2	Meets specifications in Table 52–13	LW:M	Yes [ ] N/A [ ]

52.15.3.7 PMD to MDI optical specifications for 10GBASE-ER

Item	Feature	Subclause	Value/Comment	Status	Support
ER1	10GBASE-ER transmitter	52.7.1	Meets specifications in Table 52–16	ER:M	Yes [ ] N/A [ ]
ER2	10GBASE-ER receiver	52.7.2	Meets specifications in Table 52–17	ER:M	Yes [ ] N/A [ ]

NOTE— Link attenuation requirements are specified in 52.14.3.

52.15.3.8 PMD to MDI optical specifications for 10GBASE-EW

Item	Feature	Subclause	Value/Comment	Status	Support
EW2	10GBASE-EW transmitter	52.7.1	Meets specifications in Table 52–16	EW:M	Yes [ ] N/A [ ]
EW2	10GBASE-EW receiver	52.7.2	Meets specifications in Table 52–17	EW:M	Yes [ ] N/A [ ]

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52.15.3.9 Optical measurement requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	52.9	2–5 m in length	M	Yes [ ]
OM2	Center wavelength, spectral width, and SMSR measurement	52.9.2	Measured using an optical spectrum analyzer per the centroidal wavelength, RMS spectral width, and SMSR definitions in IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	52.9.3	Measured using the methods specified in IEC 61280-1-1 or ANSI/TIA/EIA-455-95	M	Yes [ ]
OM4	Extinction ratio	52.9.4	Measured using the methods specified in IEC 61280-2-2	M	Yes [ ]
OM5	OMA measurement bandwidth	52.9.5	At least 3/T	M	Yes [ ]
OM6	RIN_XOMA measurement procedure	52.9.6	As described in 52.9.6.1, 52.9.6.2, and 52.9.6.3	M	Yes [ ]
OM7	Transmit eye	52.9.7	10.3125 GBd shall qualify for 10GBASE-W and 10GBASE-R use, measurement at 9.95328 GBd shall qualify for 10GBASE-W use only	M	Yes [ ]
OM8	Stressed receiver conformance test	52.9.9	Performed in accordance with the requirements of 52.9.9.1, 52.9.9.2, 52.9.9.3, and 52.9.9.4	M	Yes [ ]
OM9	Transmitter and dispersion penalty measurement	52.9.10.4		M	Yes [ ]

52.15.3.10 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
FO1	Fiber optic cabling	52.14	Specified in Table 52–24	INS:M	Yes [ ] N/A [ ]
FO2	Optical fiber characteristics	52.14.1	Meet the requirements of IEC 60793-2 and the requirements of Table 52–25	INS:M	Yes [ ] N/A [ ]
FO3	Maximum discrete reflectance-multimode fiber	52.14.2.2	Less than –20 dB	INS:M	Yes [ ] N/A [ ]
FO4	Maximum discrete reflectance -single-mode fiber	52.14.2.2	Less than –26 dB	INS:M	Yes [ ] N/A [ ]
FO5	10GBASE-E attenuation management	52.14.3	An attenuation between 5 dB and 11 dB	INS:M	Yes [ ] N/A [ ]
FO6	MDI requirements	52.14.4	Meet the interface performance specifications listed	INS:M	Yes [ ] N/A [ ]

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52.15.3.11 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	52.10.1	Conforms to J.2	M	Yes [ ]
ES2	Laser safety —IEC Hazard Level 1	52.10.2	Conform to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Installation	52.10.3	Follow applicable local codes and regulations	M	Yes [ ]

52.15.3.12 Environment

Item	Feature	Subclause	Value/Comment	Status	Support
EC1	Electromagnetic interference	52.11.1	Comply with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

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53. Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-LX4

53.1 Overview

This clause specifies the 10GBASE-LX4 PMD (including MDI) and the baseband medium for both multimode and single-mode optical fiber. When forming a complete PHY, a PMD shall be connected to the appropriate sublayers (see Table 53–1) and with the management functions that are accessible through the Management Interface defined in Clause 45, all of which are hereby incorporated by reference.

Table 53–1—LX4 PMD type and associated Physical Layer clauses

Associated clause	10GBASE-LX4
46—RS and	Required
XGMII[a]	Optional
47—XGXS and XAUI	Optional
48—10GBASE-X PCS/PMA	Required
49—10GBASE-R PCS	n/a
50—10GBASE-W WIS	n/a

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation behaves functionally as though the RS and XGMII were present.

Figure 53–1 shows the relationship of the PMD and MDI sublayers to the ISO/IEC (IEEE) OSI reference model.

53.1.1 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 10GBASE-LX4 PMD. The service interface for this PMD is described in an abstract manner and do not imply any particular implementation. The PMD Service Interface supports the exchange of encoded data between peer PMA entities. The PMD translates the encoded data to and from signals suitable for the specified medium.

The following PMD service primitives are defined:

PMD_UNITDATA.request

PMD_UNITDATA.indication

PMD_SIGNAL.indication

53.1.2 PMD_UNITDATA.request

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMA to the PMD.

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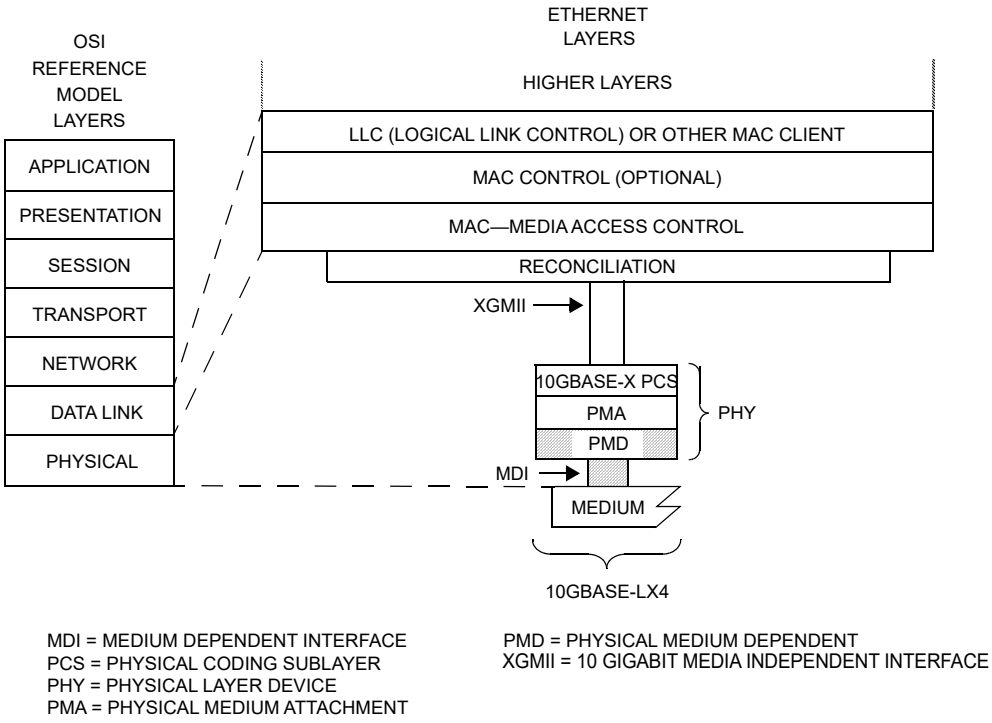

Figure 53–1—10GBASE-LX4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

53.1.2.1 Semantics of the service primitive

PMD_UNITDATA.request (tx_bit <0:3>)

The data conveyed by PMD_UNITDATA.request is a continuous sequence of four parallel code-group streams, one stream for each lane. The tx_bit <0:3> correspond to the bits in the tx_lane<0:3> bit streams. Each bit in the tx_bit parameter can take one of two values: ONE or ZERO.

53.1.2.2 When generated

The PMA continuously sends four parallel code-group streams to the PMD at a nominal signaling speed of 3.125 GBd.

53.1.2.3 Effect of Receipt

Upon receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals on the MDI.

53.1.3 PMD_UNITDATA.indication

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMD to the PMA.

53.1.3.1 Semantics of the service primitive

PMD_UNITDATA.indication (rx_bit <0:3>)

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The data conveyed by PMD_UNITDATA.indication is a continuous sequence of four parallel encoded bit streams. The rx_bit<0:3> correspond to the bits in the rx_lane<0:3> bit streams. Each bit in the rx_bit parameter can take one of two values: ONE or ZERO.

53.1.3.2 When generated

The PMD continuously sends stream of bits to the PMA corresponding to the signals received from the MDI.

53.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

53.1.4 PMD_SIGNAL.indication

This primitive is generated by the PMD to indicate the status of the signals being received from the MDI.

53.1.4.1 Semantics of the service primitive

PMD_SIGNAL.indication (SIGNAL_DETECT)

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, rx_bit is undefined, but consequent actions based on PMD_UNITDATA.indication, where necessary, interpret rx_bit as a logic ZERO.

NOTE—SIGNAL_DETECT = OK does not guarantee that rx_bit is known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the 10^{-12} BER objective.

53.1.4.2 When generated

The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT.

53.1.4.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

53.2 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. The sum of transmit and receive delay contributed by the 10GBASE-LX4 PMD shall be no more than 512 BT (including 2 m of fiber).

53.3 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. Mapping of MDIO control variables to PMD control variables is shown in Table 53–2. Mapping of MDIO status variables to PMD status variables is shown in Table 53–3.

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Table 53–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
Global PMD transmit disable	Transmit disable register	1.9.0	Global_PMD_transmit_disable
Transmit disable 3	Transmit disable register	1.9.4	PMD_transmit_disable_3
Transmit disable 2	Transmit disable register	1.9.3	PMD_transmit_disable_2
Transmit disable 1	Transmit disable register	1.9.2	PMD_transmit_disable_1
Transmit disable 0	Transmit disable register	1.9.1	PMD_transmit_disable_0

Table 53–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Local fault	Status register 1	1.1.7	PMD_fault
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD signal detect	Receive signal detect register	1.10.0	Global_PMD_signal_detect
PMD signal detect 3	Receive signal detect register	1.10.4	PMD_signal_detect_3
PMD signal detect 2	Receive signal detect register	1.10.3	PMD_signal_detect_2
PMD signal detect 1	Receive signal detect register	1.10.2	PMD_signal_detect_1
PMD signal detect 0	Receive signal detect register	1.10.1	PMD_signal_detect_0

53.4 PMD functional specifications

The 10GBASE-LX4 PMD performs the Transmit and Receive functions which convey data between the PMD service interface and the MDI plus various management functions if the optional MDIO is implemented.

53.4.1 PMD block diagram

The PMD block diagram is shown in Figure 53–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output

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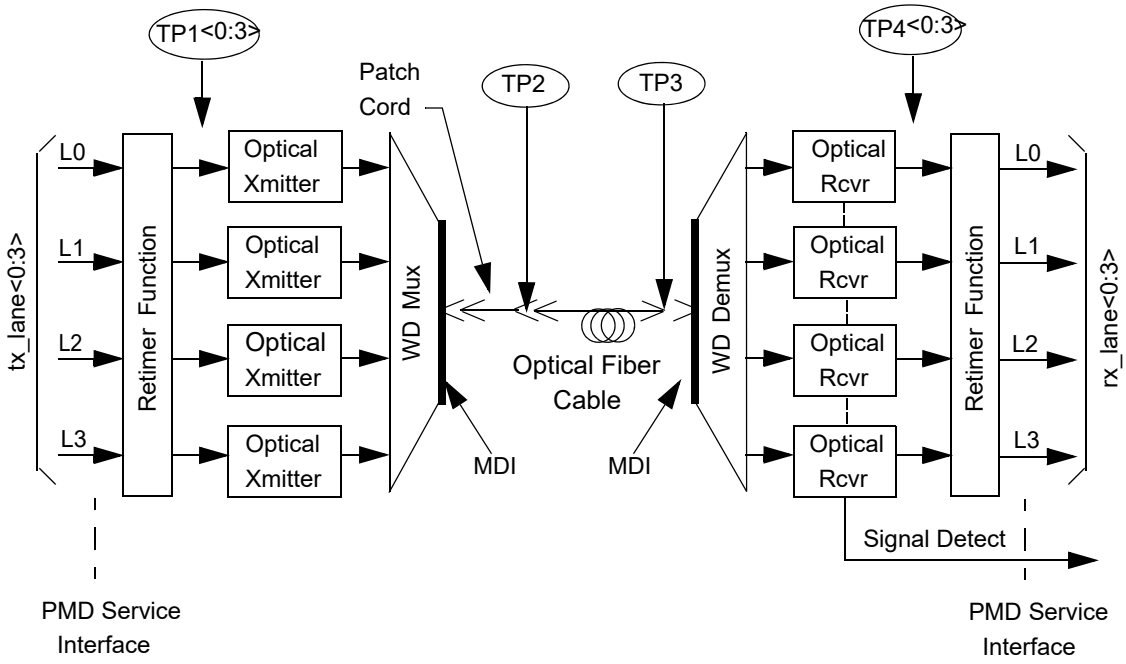
end of a patch cord (TP2), between 2 m and 5 m in length, of a type consistent with the link type connected to the transmitter receptacle defined in 53.14.2. If a single-mode fiber offset-launch mode-conditioning patch cord is used, the optical transmit signal is defined at the end of this single-mode fiber offset-launch mode-conditioning patch cord at TP2. Unless specified otherwise, all transmitter measurements and tests defined in 53.9.1 through 53.9.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 53.14.3). Unless specified otherwise, all receiver measurements and tests defined in 53.9.9 through 53.9.15 are made at TP3.



WD = Wavelength Division

NOTE—Specification of the retimer function is beyond the scope of this standard; however, a retimer may be required to ensure compliance at test points TP2 and TP3.

Figure 53–2—Block diagram for LX4 PMD transmit/receive paths

TP1 <0:3> and TP4 <0:3> are optional reference points that may be useful to implementers for testing components (these test points will not typically be testable in an implemented system).

53.4.2 PMD transmit function

The PMD Transmit function shall convert the four electronic bit streams requested by the PMD service interface message PMD_UNITDATA.request (tx_bit<0:3>) into four separate optical signals. The four optical signals shall then be wavelength division multiplexed and delivered to the MDI, all according to the transmit optical specifications in this clause. The higher optical power level in each signal shall correspond to a tx_bit = ONE.

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53.4.3 PMD receive function

The PMD Receive function shall demultiplex the composite optical signal received from the MDI into four separate optical signals. The four optical signals shall then be converted into four electronic bit streams for delivery to the PMD service interface using the message PMD_UNITDATA.indication (rx_bit<0:3>), all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to a rx_bit = ONE.

The PMD shall convey the bits received from the PMD_UNITDATA.request(tx_bit<0:3>) service primitive to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit<0:3>), where rx_bit<0:3> = tx_bit<0:3>.

53.4.4 Global PMD signal detect function

The Global PMD Receive Signal OK function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all four lanes. The PMD receiver is not required to verify whether a compliant 10GBASE-LX4 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 53–4—SIGNAL_DETECT value definition

Receive conditions	Receive Signal OK value
For any lane; Input_optical_power ≤ –30 dBm	FAIL
For all lanes; [(Input_optical_power ≥ Receiver sensitivity (max) in OMA in Table 53–8) AND (compliant 10GBASE-LX4 signal input)]	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD due to crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

53.4.5 PMD lane by lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_n, where n represents the lane number in the range 0:3, value shall be continuously set in response to the amplitude of the average optical power of the modulated optical signal on its associated lane, according to the requirements of Table 53–4.

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53.4.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

53.4.7 Global PMD transmit disable function

The Global_PMD_transmit_disable function is optional and allows all of the optical transmitters to be disabled.

a) When a Global_PMD_transmit_disable variable is set to ONE, this function shall turn off all of the optical transmitters so that the each transmitter meets the requirements of the Average Launch Power of the OFF Transmitter in Table 53–7.
b) If a PMD_fault is detected, then the PMD may set the Global_PMD_transmit_disable variable to ONE, turning off the optical transmitter in each lane.

53.4.8 PMD lane by lane transmit disable function

The PMD_transmit_disable function is optional and allows the optical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_n variable is set to ONE, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the Average Launch Power of the OFF Transmitter in Table 53–7.
b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_n to ONE, turning off the optical transmitter in each lane.

If the optional PMD_lane_by_lane_transmit_disable function is not implemented in MDIO, an alternative method shall be provided to independently disable each transmit lane.

53.4.9 PMD fault function

If the MDIO is implemented, and the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to ONE.

53.4.10 PMD transmit fault function (optional)

If the MDIO is implemented, and the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to ONE.

53.4.11 PMD receive fault function (optional)

If the MDIO is implemented, and the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to ONE.

53.5 Wavelength-division multiplexed-lane assignments

The wavelengths for each multiplexed lane of the 10GBASE-LX4 PMD shall be as defined in Table 53–5.

53.6 Operating ranges for 10GBASE-LX4 PMD

The operating ranges for 10GBASE-LX4 PMD are defined in Table 53–6. A 10GBASE-LX4 compliant transceiver supports all media types listed in Table 53–6 (i.e., 50 μm and 62.5 μm multimode fiber, and

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Table 53–5—Wavelength-division-multiplexed lane assignments

Lane	Wavelength ranges	PMD Service Interface transmit bit stream	PMD Service Interface receive bit stream
L_0	1269.0 – 1282.4 nm	tx_lane<0>	rx_lane<0>
L_1	1293.5 – 1306.9 nm	tx_lane<1>	rx_lane<1>
L_2	1318.0 – 1331.4 nm	tx_lane<2>	rx_lane<2>
L_3	1342.5 – 1355.9 nm	tx_lane<3>	rx_lane<3>

10 µm single-mode fiber) according to the specifications defined in 53.14. A transceiver that exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a single-mode solution operating at 10 500 m meets the minimum range requirement of 2 m to 10 000 m).

Table 53–6—Operating range for 10GBASE-LX4 PMD over each optical fiber type

Fiber type	Modal bandwidth at 1300 nm (min. overfilled launch) (MHz•km)	Minimum range (meters)
62.5 µm MMF	500	2 to 300
50 µm MMF	400	2 to 240
50 µm MMF	500	2 to 300
10 µm SMF	n/a	2 to 10 000

For MMF links, to ensure that the specifications of Table 53–6 are met with MMF links, the wavelength-division-multiplexed 10GBASE-LX4 transmitter outputs shall be coupled through a single-mode fiber offset-launch mode-conditioning patch cord, as defined in 38.11.4.

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53.7 PMD to MDI optical specifications for 10GBASE-LX4

53.7.1 Transmitter optical specifications

The 10GBASE-LX4 transmitters shall meet the specifications defined in Table 53–7 per measurement techniques defined in 53.9.

Table 53–7—Transmit characteristics for the 10GBASE-LX4 over each optical fiber type

Description	62.5 µm and 50 µm MMF	10 µm SMF	Units
Transmitter type	Longwave Laser		
Signaling speed per lane (nominal)	3.125 ± 100 ppm		GBd
Lane wavelengths (range)	1269.0 – 1282.4 1293.5 – 1306.9 1318.0 – 1331.4 1342.5 – 1355.9		nm
Trise/Tfall (max. 20–80 % response time)	120		ps
Side-mode suppression ratio (SMSR), (min)	0.0		dB
RMS spectral width (max)[a]	0.62		nm
Average launch power, four lanes (max)	5.5		dBm
Average launch power, per lane (max)	–0.5		dBm
Optical Modulation Amplitude (OMA), per lane (max)	750 (–1.25)		µW (dBm)
Optical Modulation Amplitude (OMA), per lane (min)[b]	211 (–6.75)	237 (–6.25)	µW (dBm)
Extinction Ratio (min)	3.5		dB
Average launch power of OFF transmitter, per lane (max)	–30		dBm
RIN_{12} (OMA)	–120		dB/Hz

[a]For sources with a distribution of two discrete modes, the spectral window containing 90% of source spectral power (max) equals 1.0 nm and the spectral window containing 99% of source spectral power (max) equals 1.4 nm. For sources with a continuous spectral distribution, the spectral window containing 90% of source spectral power (max) equals 2.0 nm and the spectral window containing 99% of source spectral power (max) equals 3.2 nm. The spectral window specifications for the continuous case is consistent with a Gaussian spectral distribution having an RMS spectral width of 0.62 nm.

[b]Transmitter values are specified at TP2. For MMF, the values in the above table include a 0.5dB attenuation for the offset launch patch cord.

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53.7.2 Receive optical specifications

The 10GBASE-LX4 receiver shall meet the specifications defined in Table 53–8 per measurement techniques defined in 53.9. The receive sensitivity includes the extinction ratio penalty.

Table 53–8—10GBASE-LX4 receive characteristics

Description	62.5 μm MMF 50 μm MMF	10 μm SMF	Unit
Signaling speed per lane (nominal)	3.125 ± 100 ppm		GBd
Lane wavelengths (range)	1269.0 – 1282.4 1293.5 – 1306.9 1318.0 – 1331.4 1342.5 – 1355.9		nm
Average receive power, four lanes (max)	5.5		dBm
Average receive power, per lane (max)	–0.5		dBm
Return loss (min)	12		dB
Receive sensitivity (OMA), per lane	37.4 (–14.25)	35.9 (–14.45)	μW (dBm)
Stressed receive sensitivity (OMA),[a,b] per lane	89.0 (–10.5)	45.7 (–13.4)	μW (dBm)
Vertical eye closure penalty,[c] per lane	3.7	1.1	dB
Receive electrical 3 dB upper cutoff frequency, per lane (max)	3750		MHz

[a]Measured with conformance test signal at TP3 (see 53.9.14) for BER = 10^{-12}.
[b]The stressed sensitivity values in the table are for system level BER measurements which include the effects of CDR circuits. It is recommended that at least 0.4dB additional margin be allocated if component level measurements are made without the effect of CDR circuits.
[c]Vertical eye closure penalty is a test condition for measuring stressed receive sensitivity. It is not a required characteristic of the receiver.

53.7.3 Illustrative 10GBASE-LX4 link power budget and penalties

The worst case power budget and link penalties for a 10GBASE-LX4 channel are shown in Table 53–9.

53.8 Jitter specifications for each lane of the 10GBASE-LX4 PMD

53.8.1 Transmit jitter specification

The transmit jitter is tested using a bit error ratio tester[101] (BERT), where the tester horizontally scans the eye opening across the centerline at a virtual TP3 (hereafter referred to as simply TP3) and measures the bit error ratio at each point in time. The plot of BER as a function of sampling time is called the “bathtub curve.”

[101]In this document, BERT is intended to include any test measurement device that can generate a BER bathtub curve. Here, it is implied that the BERT includes the Reference Receiver, filters, PLLs, etc.

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Table 53–9—Worst case 10GBASE-LX4 link power budget and penalties[a]

Parameter	62.5 µm MMF	50 µm MMF		10 µm SMF	Unit
Modal bandwidth as measured at 1300 nm (minimum, overfilled launch)	500	400	500	n/a	MHz•km
Link power budget	7.5	7.5	7.5	8.2	dB
Operating distance[b]	300	240	300	10 000	m
Channel insertion loss[c, d]	2.0	1.9	2.0	6.2	dB
Allocation of penalties	5.0	5.5	5.5	1.9	dB
Additional insertion loss allowed[e]	0.5	0.1	0.0	0.1	dB

[a]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[b]An offset launch patch cord is required for MMF.
[c]The channel insertion loss is calculated using the maximum distance values specified in Table 53–6 plus an allocation of 1.5dB for MMF and 2.0dB for SMF for connection and splice loss. Channel insertion loss is specified from TP2 to TP3 in Figure 53–2. The total insertion loss for cabled multimode optical fiber, including the attenuation of the offset launch patch cord, is allowed to be 0.5 dB higher than shown in the table.
[d]A wavelength of 1269 nm, a minimum receiver bandwidth of 2550 MHz, and a DCD_DJ of 14 ps is used to calculate lane insertion loss, link power penalties, and unallocated margin.
[e]This portion of the link budget is permitted to be used to overcome insertion loss higher than the "Channel insertion loss" value.

All points on the BER "bathtub curve" shall have an eye opening greater than specified by the bit error ratio tester (BERT) mask at the respective BER when measured using the jitter compliance test methodology for the transmitter as defined in 53.9.10. The BERT mask (see example in Figure 53–3) is specified by the following polynomial:

$$\log_{10}(BER) \le A - B\left(\frac{t - 0.5W}{\sigma}\right)^2 \quad (53\text{–}1)$$

$$\log_{10}(BER) \le A - B\left(\frac{1 - t - 0.5W}{\sigma}\right)^2 \quad (53\text{–}2)$$

where:

$$A = -1.75, B = \frac{\log_{10}(e)}{2} \approx 0.217$$

and the variables "W" and "σ" for the polynomial are specified in Table 53–10. The variables "W" and "σ" are the effective DJ and RJ respectively although the DJ and RJ values are not normative in the standard. In the above equations the variable "t" is time specified in unit intervals (UI). The BER mask is defined for $10^{-12} <$ BER $< 10^{-6}$. The DJ and RJ values do not need to be individually met, the required mask is defined by the formulas above.

Table 53–10—BERT mask specifications

PMD	W (UI pk to pk)	σ (UI rms)
10GBASE-LX4	0.3	0.015

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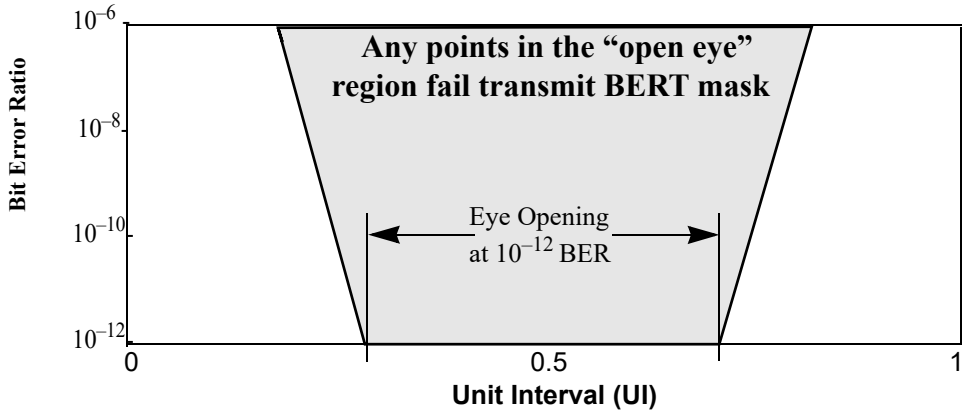

Figure 53–3—Example transmit BER mask at TP3

53.8.1.1 Channel requirements for transmit jitter testing

The optical channel for 10GBASE-LX4 shall

a) Have an ITU-T G.652 fiber or fibers with lengths chosen to have a total dispersion larger than specified in Table 53–12 for the wavelength of the device under test. To verify that the fiber has the correct amount of dispersion, use the measurement method defined in IEC 60793-1-42.
b) Meet these requirements in the linear regime of the single-mode fiber.
c) Meet the requirements in Table 53–14 for the case of a 2 to 5 meter offset launch patch cord.

The transmitter shall be tested for single-mode fiber use using the single-mode simulation channel defined in 53.9.10.2. The transmitter shall also be tested for multimode fiber use using the multimode simulation channel defined in 53.9.10.2.

53.8.1.2 Test pattern requirements for transmit jitter testing

Test patterns for 10GBASE-LX4 are specified in Annex 48A.

53.8.2 Receive jitter tolerance specification

The jitter compliance methodology for the receiver is defined in Annex 48B. The receiver shall operate at a BER less than 10^{-12} when tested with an input signal defined in 53.8.2.1 through 53.8.2.1.

The input signal used for jitter tolerance is composed of the appropriate test pattern, the stressed receiver conformance test signal, the minimum specified input jitter (TJ and DJ) and added sinusoidal jitter.

53.8.2.1 Input jitter for receiver jitter test

The input jitter used to test receiver jitter tolerance shall meet the requirements of the receiver input jitter mask defined by the following equations and Table 53–10.

$$\log_{10}(BER) \geq A - B\left(\frac{t - 0.5W}{\sigma}\right)^2 \quad (53\text{–}3)$$

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$$\log_{10}(BER) \geq A - B\left(\frac{1 - t - 0.5W}{\sigma}\right)^2 \quad (53–4)$$

where:

$$A = -1.75, B = \frac{\log_{10}(e)}{2} \approx 0.217$$

The mask is defined for a BER range of $10^{-12} < BER < 10^{-6}$. An explanation of the variables W, σ, and t can be found in 53.8.1.

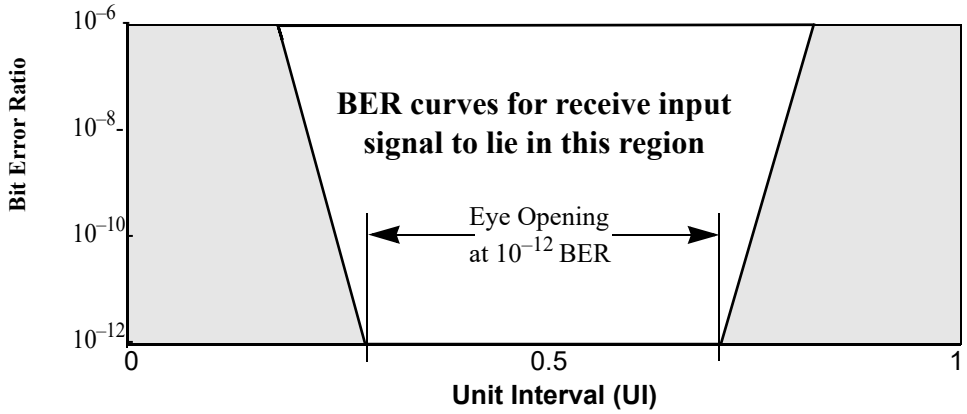

Figure 53–4—Illustration of input jitter mask for receiver test

The random jitter (RJ) component of the input signal shall have uniform spectral content over the measurement frequency range of 18.75kHz to 1.5GHz.

The test method for verification of the input jitter is defined in 53.8.1. A Clock Recovery Unit shall be used for verification of the input jitter. It shall have a high-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade. The low-frequency corner corresponds to the point at which the PLL has to begin to track low-frequency jitter. The filter used for RX input signal characterization shall be a fourth-order Bessel-Thomson filter as specified in section 53.9.7.

53.8.2.2 Added sinusoidal jitter for receiver jitter test

The sinusoidal jitter used to test receiver jitter tolerance shall meet the requirements of Table 53–11. Sinusoidal jitter shall be added to the test signal that complies with 53.8.2.1.

Table 53–11—Applied sinusoidal jitter

Frequency range	Sinusoidal amplitude jitter (UI pk-pk)
f <18.75 kHz	NA
18.75 kHz < f < 1.875 MHz	$\frac{93\ 750\ \text{Hz}}{f}$
1.875 MHz < f < 10 LB[a]	0.05

[a]LB = Loop Bandwidth; Recommended minimum value of upper bound of 0.05 UI added range is 10 times loop bandwidth.

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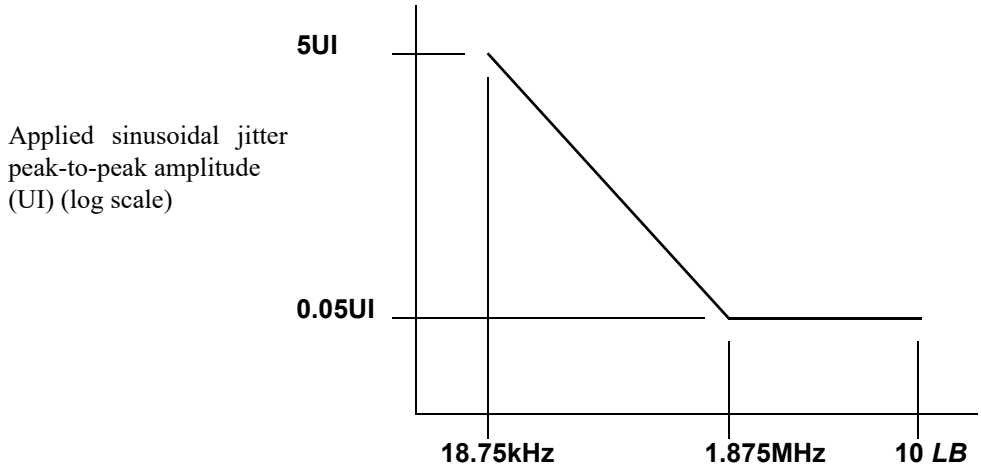

Figure 53–5—Illustration of the mask of the sinusoidal component of jitter tolerance

53.9 Optical measurement requirements

All optical measurements shall be made through a short patch cable, between 2 m and 5 m in length. If a single-mode fiber offset-launch mode-conditioning patch cord is used, the optical transmit signal is defined at the output end (TP2) of the single-mode fiber offset-launch mode-conditioning patch cord.

It is recommended that wavelength measurements, RIN measurements, optical power measurements, source spectral window measurements, extinction ratio measurements, optical modulation amplitude measurements, and transmit rise/fall characteristics be performed using a low-frequency square-wave pattern (K28.7).

It is recommended that the receiver 3dB electrical upper cutoff frequency characterization be performed using CRPAT or another reasonable mixed frequency pattern.

Furthermore, it is recommended that the transmitter optical waveform, receive sensitivity measurements, transmitter jitter conformance tests, stressed receiver conformance tests, and jitter tolerance measurements be characterized using CJPAT.

The recommendation of specific test patterns is provided in an effort to meet the overall objective of ensuring compliance of the standard under any and all valid data patterns.

53.9.1 Wavelength range measurements

The wavelength ranges of each wavelength lane shall be measured with an optical spectrum analyzer (OSA) or equivalent device over the wavelength range specified in Table 53–8; with the following conditions:

a) The resolution bandwidth equal to the spectral window values for the particular source type as specified in Table 53–8, and
b) The channel under test is modulated using valid 10GBASE-LX4 signals.

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53.9.2 Optical power measurements

The absolute optical power of each channel shall be measured using the methods in IEC 61280-1-1 or ANSI/TIA/EIA-455-95, with the sum of the optical power from all of the channels not under test below –30 dBm, per the test set-up in Figure 53–6.

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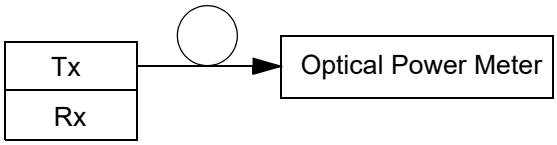

Figure 53–6—Optical power measurement test set-up

53.9.3 Source spectral window measurements

The source spectral window shall be measured for each channel individually with the sum of the optical power from all of the channels not under test below –30dBm, per the test set-up in Figure 53–7. The channel under test shall be modulated using valid 10GBASE-LX4 signals.

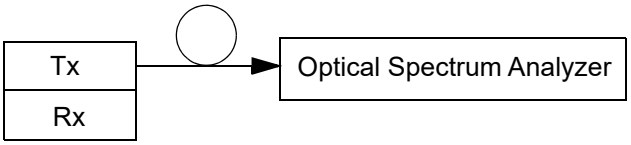

Figure 53–7—Source spectral window measurement test set-up

53.9.4 Extinction ratio measurements

Extinction ratio shall be measured using the methods specified in IEC 61280-2-2. The extinction ratio is measured under fully modulated conditions.

53.9.5 Optical Modulation Amplitude (OMA) measurements

The OMA measurement methodology is defined in 52.9.5 with the exception that each channel will be tested individually and the sum of the optical power from all of the channels not under test shall be below –30 dBm.

53.9.6 Relative Intensity Noise [RIN_{12}(OMA)]

The RIN measurement methodology is defined in 52.9.6 with the exception that each channel will be tested individually, the sum of the optical power from all of the channels not under test shall be below –30 dBm, and the upper –3 dB limit of the measurement apparatus is to be approximately equal to the bit rate (i.e., 3.125 GHz).

53.9.7 Transmitter optical waveform (transmit eye)

The required transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 53–8. Measurements shall be made as per IEC 61280-2-2. The transmit mask is not used for response time and jitter specification.

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Normalized amplitudes of 0.0 and 1.0 represent the amplitudes of logic ZERO and ONE respectively.

The eye shall be measured with respect to the mask of the eye using a fourth-order Bessel-Thomson filter having a transfer function given by Equation (53–5):

$$H(p) = \frac{105}{105 + 105\,y + 45\,y^2 + 10\,y^3 + y^4} \tag{53–5}$$

where:

$$y = 2.114\,p; \qquad p = \frac{j\omega}{\omega_r}; \qquad \omega_r = 2\pi f_r \; ; \qquad f_r = 2.344 \text{ GHz}$$

and where the filter response vs. frequency range for this fourth-order Bessel-Thomson filter is defined in ITU-T G.957, along with the allowed tolerances (STM-16 values) for its physical implementation.

This Bessel-Thomson filter is not intended to represent the noise filter used within an optical receiver, but is intended to provide uniform measurement conditions at the transmitter.

The fourth-order Bessel-Thomson filter is reactive. In order to suppress reflections, a 6 dB attenuator may be required at the filter input and/or output.

A Clock Recovery Unit shall be used to trigger the scope for mask measurements. It shall have a low-frequency corner of less than or equal to 1.875 MHz and a slope of 20 dB/decade.

For each lane, the transmit optical waveform is tested with the receive section in operation on all four lanes and with the transmit lanes not under test in operation. CJPAT, CRPAT, or valid 8B/10B encoded data, may be sent to the receive section of the transmitter under test. The data being received has to be asynchronous to the transmitted data.

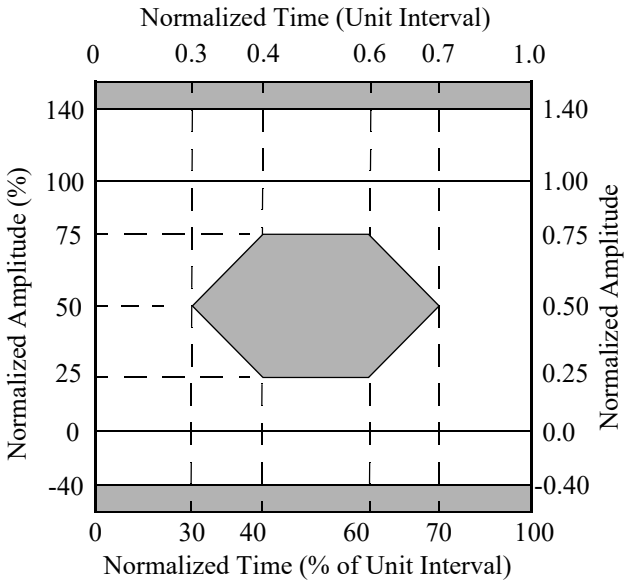

Figure 53–8—Transmitter eye mask definition

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53.9.8 Transmit rise/fall characteristics

Optical response time specifications are based on unfiltered waveforms. Some lasers have overshoot and ringing on the optical waveforms, which, if unfiltered, reduce the accuracy of the measured 20–80% response times. For the purpose of standardizing the measurement method, measured waveforms shall conform to the mask defined in Figure 53–8. If a filter is needed to conform to the mask, the filter response shall be removed using Equation (53–6):

$$T_{rise,\,fall} = \sqrt{(T_{rise,\,fall\_measured})^2 - (T_{rise,\,fall\_filter})^2} \quad (53–6)$$

where the filter may be different for rise and fall. Any filter shall have an impulse response equivalent to a fourth-order Bessel-Thomson filter. The fourth-order Bessel-Thomson filter defined in 53.9.7 may be a convenient filter for this measurement; however, its low bandwidth adversely impacts the accuracy of the $T_{rise,fall}$ measurements.

53.9.9 Receive sensitivity measurements

The stressed receive sensitivity shall be measured using the conformance test signal at TP3, as specified in 53.9.14 and meet the conditions specified in Table 53–8.

53.9.10 Transmitter jitter conformance (per lane)

53.9.10.1 Block diagram and general description of test set up

A block diagram for the transmitter jitter conformance test is shown in Figure 53–9. The transmitter (Tx) of the system under test is tested for conformance by continuously generating the test pattern specified in Annex 48A. Depending on the port type, a “Test Fiber” is added to the channel so that the jitter can be measured at a virtual TP3 (hereafter simply referred to simply as TP3) and thus include dispersion and other chromatic and channel induced penalties.

A “Reference Optical Filter” selects the wavelength channel under test in the presence of all channels operating.

A “Reference Receiver (Rx)” converts the optical signal to the electrical domain for input to the BERT.

For 10GBASE-LX4 (single-mode) the receiver shall have a fourth-order Bessel-Thomson response with the transfer function specified in 53.9.7.

Since there is no known way to create a channel using multimode fiber that would yield consistent results, the fiber is omitted from TP2 to TP3.

For 10GBASE-LX4 (multimode), the receiver shall have a fourth-order Bessel-Thomson response with the transfer function specified in 53.9.7 followed by a transversal filter with two equal amplitude paths with a differential delay of 157ps.

The PLL is used in the jitter measurement. It shall have a corner frequency of less than or equal to 1.875MHz and a slope of 20dB/decade. When using a Clock Recovery Unit as a clock for BER measurements, passing of low-frequency jitter from the data to the clock removes this low-frequency jitter from the measurement. The corner frequency corresponds to the point at which the PLL has to begin to track this low-frequency jitter.

Jitter shall be measured at the average value of the overall waveform. This can be accomplished with AC-coupling to ground and measuring at ground.

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The measurement in this section shall be satisfied with asynchronous data flowing into all four optical receiver channels of the system under test.

The method by which the test pattern is loaded into, or generated by, the BERT is outside the scope of this document.

For each lane, the transmit jitter is tested with the receive section in operation on all four lanes and with the transmit lanes not under test in operation. CJPAT, CRPAT, or valid 8B/10B encoded data, may be sent to the receive section of the transmitter under test. The data being received has to be asynchronous to the transmitted data.

Annex 48B contains both theoretical and practical information on jitter testing.

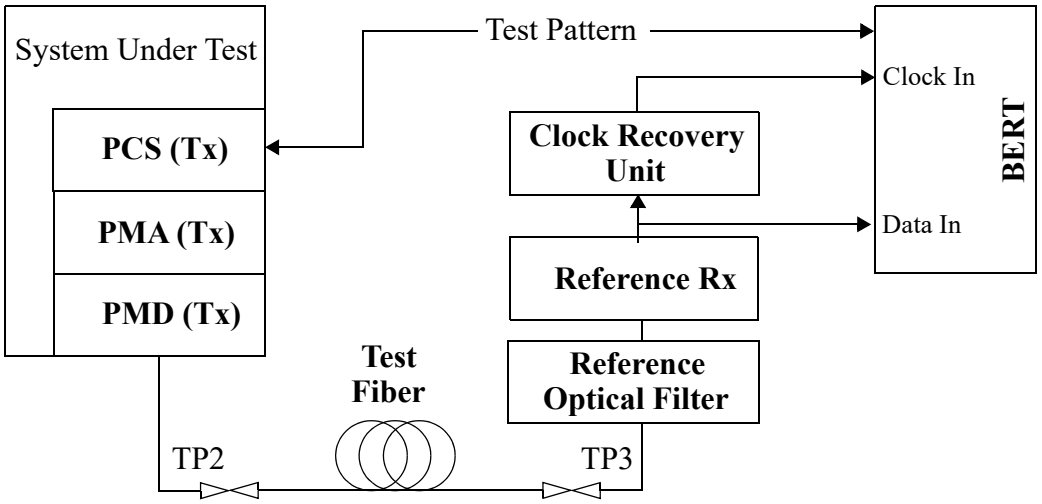

Figure 53–9—Transmit jitter test block diagram

53.9.10.2 Channel requirements for transmit jitter testing

The optical channel used to test the transmitter shall meet the requirements listed in Table 53–12.

Table 53–12—Transmit jitter compliance channel specifications

PMD Type	Minimum dispersion[a] (ps/nm)		Insertion loss[b]	Minimum Return loss[c]
	Minimum	Maximum		
10GBASE-LX4 (multimode)	N/A	N/A	Minimum	See Table 53–8
10GBASE-LX4 (single-mode)	$0.2325 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	$0.2325 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	Minimum	See Table 53–8

[a]The dispersion is measured for the wavelength of the device under test. The coefficient assumes 10 km for the case of single-mode fiber.
[b]There is no intent to stress the sensitivity of the BERT's optical receiver.
[c]The return loss is applied at TP2. Note that the referenced return losses are maximums. Here, the return loss is a minimum.

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For 10GBASE-LX4 (single-mode), the transmitter shall be compliant with dispersion at least as negative as the “minimum dispersion” and at least as positive as the “maximum dispersion” columns. This shall be achieved using ITU-T G.652 fiber or fibers with lengths chosen to have a total dispersion larger than specified in Table 53–12 for the wavelength of the device under test. To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The channel shall meet these requirements in the linear regime of the fiber. The channel shall provide an optical back reflection specified in Table 53–7 for 10GBASE-LX4. The state of polarization of the back reflection shall be adjusted to create the greatest RIN. The methods of 52.9.6.2 and 52.9.6.3 may be used.

The channel for 10GBASE-LX4 (multimode) is a 2 to 5 meter patch cord meeting the requirements in Table 53–12. The channel shall provide back reflection to the transmitter at –12 dB. The polarization adjustment does not apply, as noted in 52.9.6.3 item c).

53.9.10.3 Transmit jitter test procedure

After setting up the test as described above, the BERT is scanned horizontally across the center of the eye, from 0 unit intervals (UI) to 1 unit interval, while measuring the error ratio to develop a BER “bathtub curve” as described in 53.8.1.1. This clause also specifies the BER mask. It is not necessary to measure the error ratio in the center of the eye where the BER is less than 10^{-12} or at the edges where the BER is worse than 10^{-4}. The mask natively includes those components of jitter (random, deterministic, bounded) historically measured independently.

A Clock Recovery Unit having a low-frequency corner of less than or equal to 1.875 MHz and a slope of 20 dB/decade shall be used to generate the reference clock for transmit jitter measurements.

NOTE—The specifications for the Reference Optical Filter, Reference Rx, Clock Recovery Unit, and BERT, except as specified above, are outside the scope of this document. The Reference Rx and Clock Recovery Unit are intended to provide consistent and repeatable measurements, not to represent the worst case receiver. It should also be noted that a poorer grade of test equipment will force a greater burden onto the system-under-test to meet specifications. Similarly, a better grade of test equipment will ease the development and manufacture of the system and system components. It is expected that trade-offs needed to optimize the overall cost of development, manufacture and test will change over time and are best left to the implementer.

53.9.11 Receive sensitivity measurements

The receiver sensitivity, which is defined for an ideal input signal is optional. Receivers are tested with a conditioned input signal where both vertical eye closure and jitter have been added according to 53.9.12. When tested according to 53.9.12, the stressed sensitivity shall meet the specifications in Table 53–8 for 10GBASE-LX4.

53.9.12 Stressed receiver conformance test

The measurements in this subclause shall be satisfied with asynchronous data flowing out of the optical transmitter of the system under test. This data shall be consistent with normal signal properties and content.

53.9.12.1 Block diagram of stressed receiver tolerance test set up

A block diagram for the receiver jitter conformance test is shown in Figure 53–10. The receiver of the system under test is tested for conformance by putting the PCS in test mode as specified in Annex 48A. A suitable pattern generator is used to continuously generate a test pattern defined in Annex 48A. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 53.9.14 and applying sinusoidal jitter as defined in 53.8.2.2. As defined in section Annex 48A, the PCS is capable of detecting the data pattern and reporting any errors received.

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A BER test set or other suitable test set is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics. This measurement is made using the same method as the transmit jitter test method described in 52.8. The "Test Fiber" called out for LX4 is not needed to characterize the receiver input signal. A "Clock Recovery Unit" meeting the requirements of 53.8.2.1 shall be used.

Jitter shall be calibrated at the average value of the overall optical waveform. This can be accomplished by AC-coupling.

The method by which the test pattern is loaded into, or generated by, the BERT is outside the scope of this document.

Annex 48B contains both theoretical and practical information on jitter testing.

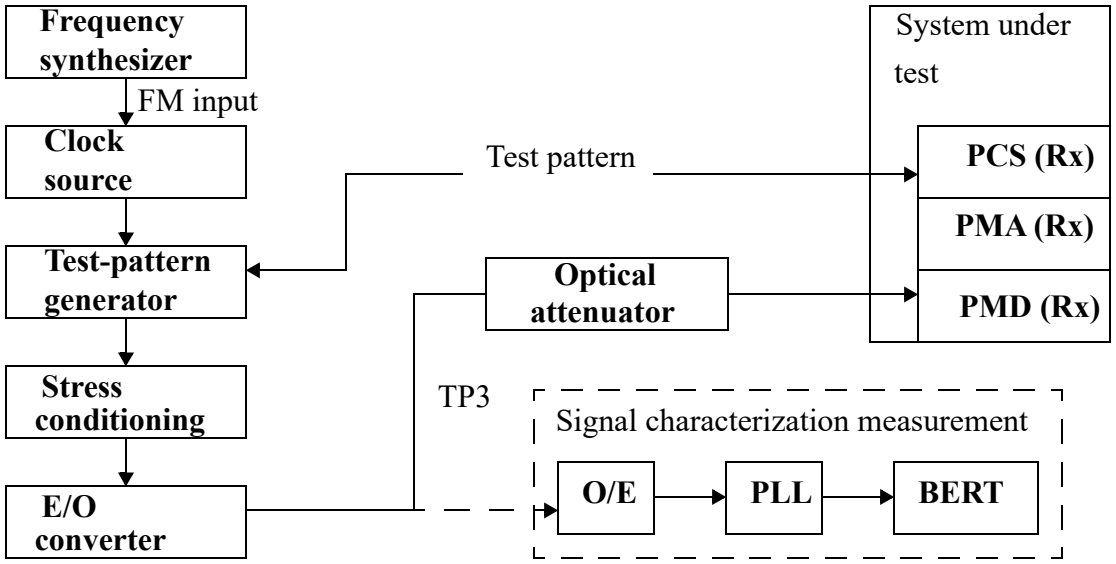

Figure 53–10—Receive jitter test block diagram

53.9.12.2 Stressed receiver conformance test procedure

A BER test set, or other suitable test set, is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics. This measurement is made using the same method as the transmit jitter test method described in 53.9.10. The "Test Fiber" called out for LX4 (single-mode) and the transversal filter called out for LX4 (multimode) are not needed to characterize the receiver input signal. A Clock Recovery Unit meeting the requirements of 53.8.2.1 shall be used.

53.9.12.3 Characterization of receiver input signal

Care should be taken when characterizing the signal used to make receiver tolerance measurements. In the case of a transmit jitter measurement, excessive and/or uncalibrated noise/jitter in the test system makes it more difficult to meet the specification and may have a negative impact on yield, but will not effect interoperability. In the case of the receiver input calibration measurement, however, excessive noise/jitter will result in an input signal that does not meet the mask requirements defined in 53.8.2.1. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant

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receivers. Care should be taken to minimize the noise/jitter introduced by the reference O-E, filters and BERT and/or to correct for this noise. While the details of a BER scan measurement and test equipment are beyond the scope of this document, it is recommended that the implementer fully characterize their test equipment and apply appropriate guard bands to ensure that the RX input signal meets the mask specified in 53.8.2.1.

53.9.12.4 Jitter tolerance test procedure

Set up the test apparatus as described in 53.9.12.1 and adjust the optical input power to the receiver under test to meet the requirements of 53.8.2.1. The sinusoidal jitter is then swept across the frequency and amplitude range specified in 53.8.2.1 while monitoring BER at the receiver. This method does not result in values for TJ, DJ, or RJ contributed by the receiver. It does, however, guarantee that a receiver meeting the requirements of this test will operate with the worst-case optical input

For each lane, the receive jitter tolerance is tested with the transmit section in operation on all four lanes and with the receive lanes not under test in operation. CJPAT, CRPAT, or valid 8B/10B encoded data, may be sent from the transmit section of the receiver under test. The data being transmitted has to be asynchronous to the received data.

53.9.13 Measurement of the receiver 3 dB electrical upper cutoff frequency

The receiver cutoff frequency measurement shall be performed on each wavelength channel independently using a laser source with its output wavelength within the specified wavelength range of the channel to be tested. The test setup is shown in Figure 53–11. The test is performed with a tunable laser that is suitable for analog signal transmission. The laser is modulated by a digital data signal. In addition to the digital modulation the laser is modulated with an analog signal. The analog and digital signals should be asynchronous. The data pattern to be used for this test is the short continuous random test pattern defined in Annex 48A. The frequency response of the laser needs to be sufficient to allow it to respond to both the digital modulation and the analog modulation. The laser should be biased so that it remains linear when driven by the combined signals. The test may use two optical sources and an optical combiner as defined in 52.9.11.

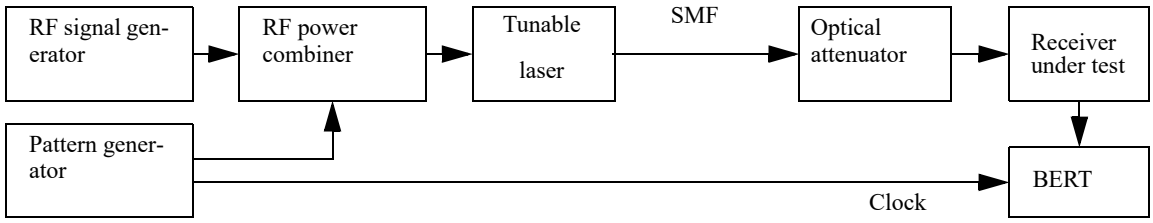

Figure 53–11—Test setup for receiver bandwidth measurement

The 3 dB upper cutoff frequency shall be measured using the following steps:

a) Calibrate the frequency response characteristics of the test equipment including the analog radio frequency (RF) signal generator, RF power combiner, and laser source, with the optical source meeting the requirements of this clause.
b) Configure the test equipment as shown in Figure 53–11. Take care to minimize changes to the signal path that could affect the system frequency response after the calibration in step a). Connect the laser output with no RF modulation applied to the receiver under test through an optical attenuator and

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taking into account the extinction ratio of the source, set the optical power to a level that approximates the stressed receive sensitivity level in Table 53–8.

c) Locate the center of the eye with the BERT. Turn on the RF modulation while maintaining the same average optical power established in step b).

d) Measure the necessary RF modulation amplitude (in dBm) required to achieve a constant BER (e.g., 10^{-8}) for a number of frequencies.

e) The receiver 3 dB electrical upper cutoff frequency is that frequency where the corrected RF modulation amplitude (the measured amplitude in "d" corrected with the calibration data in "a") increases by 3 dB (electrical). If necessary, interpolate between the measured response values.

53.9.14 Conformance test signal at TP3 for receiver testing

Receivers being tested for conformance to the stressed receive sensitivity requirements of 53.9.9 and the total jitter requirements of 53.9.10 shall be tested using a conformance test signal at TP3 conforming to the requirements described in Figure 53–12. It is recommended that the conformance test signal be generated using a short continuous random test pattern as defined in Annex 48A. The conformance test signal is conditioned by applying deterministic jitter (DJ) and intersymbol interference (ISI). The conditioned conformance test signal is shown schematically in Figure 53–12. The horizontal eye closure (reduction of pulse width) caused by the duty cycle distortion (DCD) component of DJ shall be no less than 14 ps.

The vertical eye closure penalty shall be greater than or equal to the value specified in Table 53–8. The DJ cannot be added with a simple phase modulation, which does not account for the DCD component of DJ.

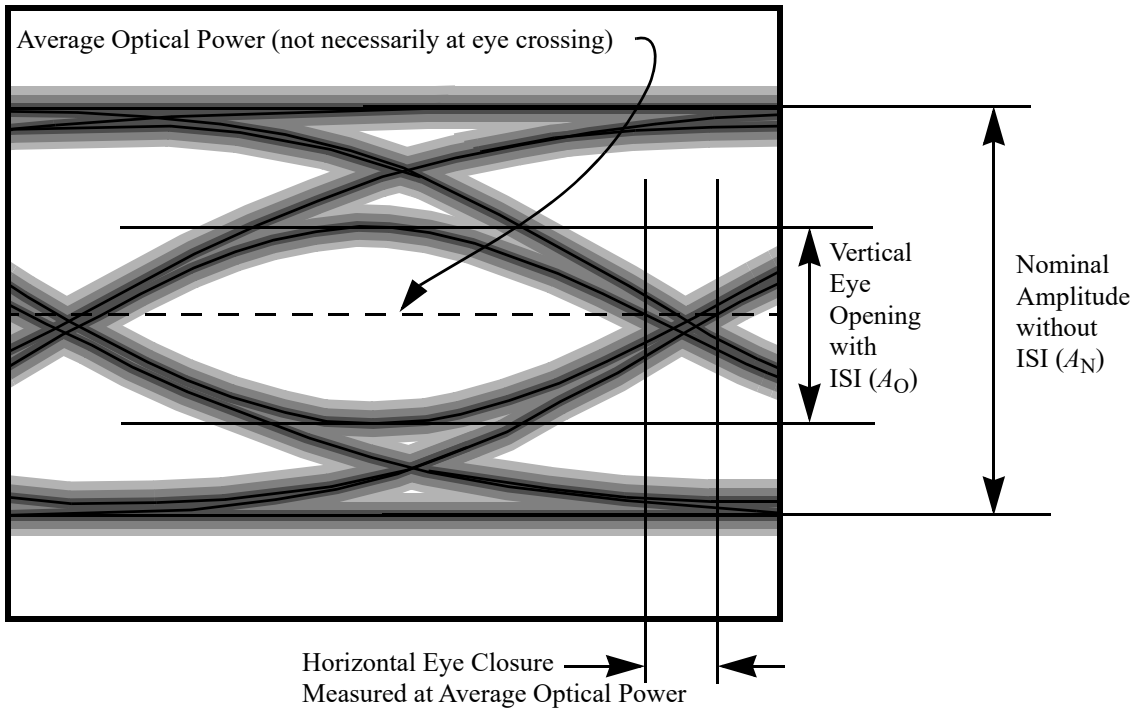

Figure 53–12—Required characteristics of the conformance test signal at TP3

The vertical eye closure penalty is given by:

$$\text{Vertical eye closure penalty [dB]} = 10 \times \log \frac{A_O}{A_N}$$

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where, A_O is the amplitude of the eye opening and A_N is the normal amplitude without ISI, as measured in Figure 53–12.

Figure 53–13 shows a possible test set up for producing the conformance test signal at TP3. The coaxial cable is adjusted in length to produce the correct DCD component of DJ. Since the coaxial cable can produce the incorrect ISI, a limiting amplifier is used to restore fast rise and fall times. A Bessel-Thomson filter is selected to produce the minimum ISI induced eye closure as specified per Figure 53–12. This conditioned signal is used to drive a high bandwidth, tunable, wavelength tunable source.

Figure 53–13 shows this function being performed by a tunable source in combination with an external optical modulator. However, any other method capable of this combined function will suffice. Similarly, the remaining sources supply to their respective channels modulated signals at specific wavelengths, as specified in 53.9.15. This could be accomplished with tunable or fixed sources at the wavelengths required. The vertical and horizontal eye closures to be used for receiver conformance testing are verified using a fast photodetector and amplifier coupled to the oscilloscope input through a filter. The combined filtering effect of the photodetector, amplifier, and filter shall be a fourth-order Bessel-Thomson filter of 2.34 GHz bandwidth. Special care should be taken to ensure that all the light from the fiber is collected by the fast photodetector and that there is negligible mode selective loss, especially in the optical attenuator.

The source for the channel under test shall be set to supply a signal at the output of the optical multiplexer at the minimum OMA with all other remaining channels set to the maximum OMA. Each channel is to be tested with its adjacent channels set at the near end of their wavelength range. This is to occur sequentially, as described in 53.9.15. The channel under test is to be tuned over its wavelength range during a given measurement to account for wavelength dependent losses within the channel.

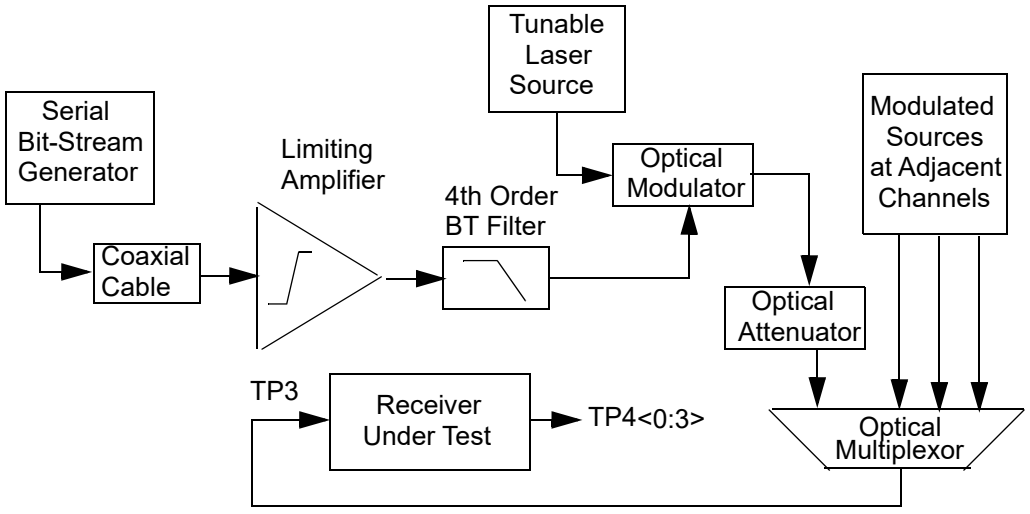

Figure 53–13—Setup for generating receiver conformance test signal at TP3

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53.9.15 Receiver test suite for WDM conformance testing

The receiver tests requiring the TP3 conformance test signal are performed on a per channel basis and shall meet the following test conditions:

a) All channels are modulated simultaneously, using valid 10GBASE-LX4 signals.
b) The center wavelengths of channels adjacent to the channel under test are tuned to the edge of their wavelength band nearest the channel under test.
c) When setting the wavelength of the channels adjacent to the channel under test, the center wavelength of the adjacent channels are set within 0.5 nm of the edge of that channel's wavelength band while remaining within that channel's wavelength band.
d) In the case of the interior channels, which have two adjacent channels, each adjacent channel is tuned individually and receiver testing is done twice, once for each adjacent channel.
e) The non-adjacent channels are to be tuned to the center of their respective wavelength ranges.
f) The transmitter of the transceiver under test is operating with valid test patterns as defined in Annex 48A.

These conditions are summarized graphically in Figure 53–14 for each channel under test.

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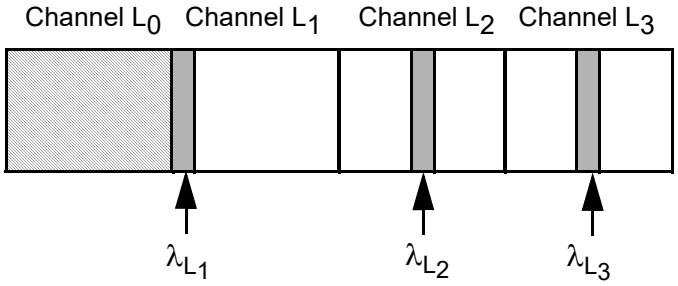
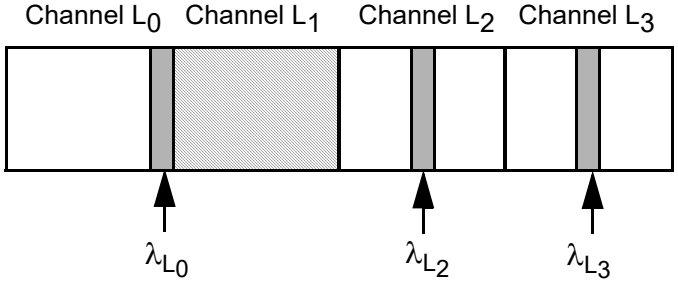
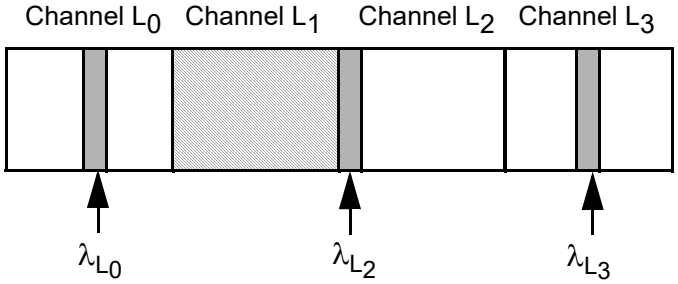
a) Channel L0 under test



Channel L1 under test (L0 in extreme position)



Channel L1 under test (L2 in extreme position)



Channel L2 under test (L1 in extreme position)

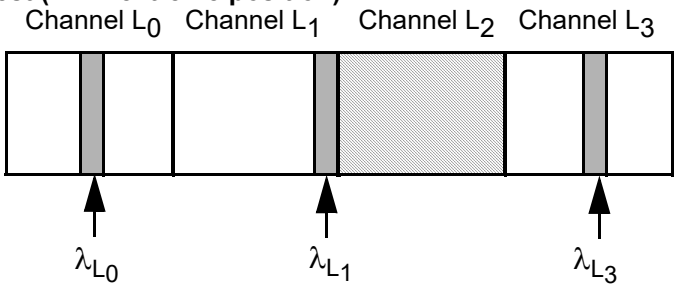


Figure 53–14—Channel test conditions for conformance test at TP3

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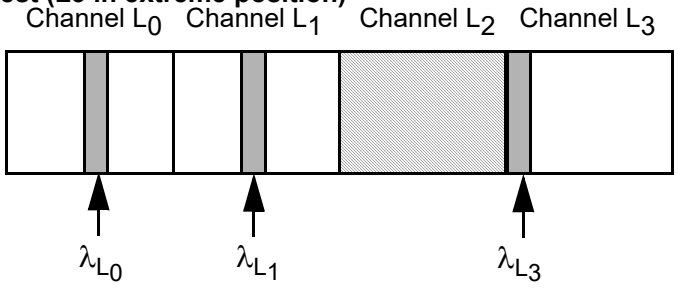
Channel L2 under test (L3 in extreme position)



Channel L3 under test (L2 in extreme position)

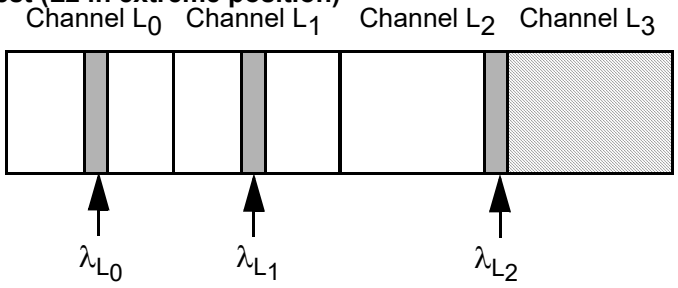


Figure 53–14—Channel test conditions for conformance test at TP3 *(continued)*

NOTE—The two interior channels (L_1, L_2) require two different wavelength configurations since they have two adjacent channels. Therefore, there will be twice as many tests to perform on these channels as on exterior channels L_0, L_3.

53.10 Environmental specifications

53.10.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

53.10.2 Laser safety

The 10GBASE-LX4 optical transceivers shall be Hazard Level 1 laser certified under any condition of operation in conformance to IEC 60825-1 and IEC 60825-2. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly define requirements and usage restrictions on the host system necessary to meet these safety certifications.[102]

[102]A host system that fails to meet the manufacturers requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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53.10.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

53.11 Environment

Normative specifications in this clause shall be met by a system integrating a 10GBASE-LX4 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

53.11.1 Electromagnetic emission

A system integrating a 10GBASE-LX4 PMD shall comply with applicable local, national, and international codes for the limitation of electromagnetic interference.

53.11.2 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

53.12 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters, according to the PMD-MDI type.

PMD MDI type 10GBASE-LX4:

a) 10GBASE-LX4;
b) Applicable safety warnings.

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 53.10.2.

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53.13 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 53–15.

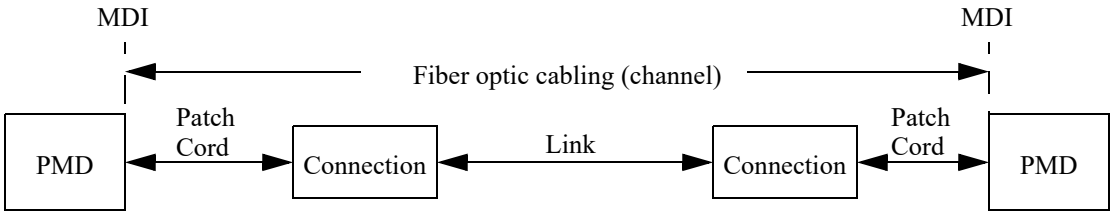

Figure 53–15—Fiber optic cabling model

The channel insertion loss is given in Table 53–13. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1 one-cord method, and IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 53–13—Fiber optics cabling (channel) characteristics

Description	62.5 μm MMF	50 μm MMF		SMF	Unit
Modal bandwidth at 1300nm (min; overfilled launch)	**500**	**400**	**500**	**n/a**	**MHz•km**
Operating distance (max)	300	240	300	10 000	m
Channel insertion loss (max)[a]	2.5	2.0	2.0	6.6	dB

[a]These channel insertion loss numbers are calculated using a wavelength of 1300nm for MMF and 1310nm for SMF. An offset launch patch cord is assumed. Channel insertion loss is specified from TP2 to TP3 in Figure 53–2. The total insertion loss, when including the attenuation of the offset launch patch cord, is allowed to be 0.5dB higher than shown in the table.

53.14 Characteristics of the fiber optic cabling (channel)

The 10GBASE-LX4 fiber optic cabling shall meet the specifications defined in Table 53–13. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. The fiber optic cabling spans from one MDI to another MDI, as shown in Figure 53–15.

53.14.1 Optical fiber and cable

The fiber optic cable requirements are satisfied by the fibers specified in IEC 60793-2:1992. Types A1a (50/125 μm multimode), A1b (62.5/125 μm multimode), and B1.1 (dispersion un-shifted single-mode) and B1.3 (low water peak single-mode) with the exceptions noted in Table 53–14.

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Table 53–14—Optical fiber and cable characteristics

Description	62.5 μm MMF	50 μm MMF	Type B1.1, B1.3 SMF	Unit
Nominal fiber specification wavelength	1300	1300	1310	nm
Cabled optical fiber attenuation (max)	1.5	1.5	0.4[a] or 0.5[b]	dB/km
Modal Bandwidth	500	400	N/A	MHz km
(min; overfilled launch)		500	N/A	MHz km
Zero dispersion wavelength (λ_0)	$1320 \le \lambda 0 \le 1365$	$1295 \le \lambda 0 \le 1320$	$1300 \le \lambda 0 \le 1324$	nm
Dispersion slope (max) (S_0)	0.11 for $1320 \le \lambda_0 \le 1348$ and $0.001(1458 - \lambda_0)$ for $1348 \le \lambda_0 \le 1365$	0.11 for $1300 \le \lambda_0 \le 1320$ and $0.001(\lambda_0 - 1190)$ for $1295 \le \lambda_0 \le 1300$	0.093	ps/nm^2 km

[a]For the single-mode case, the 0.4 dB/km attenuation for optical fiber cables is defined in ITU-T G.652.
[b]For the single-mode case, the 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3. Using 0.5 dB/km may not support operation at 10 km.

53.14.2 Optical fiber connection

An optical fiber connection as shown in Figure 53–15 consists of a mated pair of optical connectors. The 10GBASE-LX4 PMD is coupled to the fiber optic cabling through a connector plug into the MDI optical receptacle, as shown in 53.14.3.

53.14.2.1 Connection insertion loss

The insertion loss is specified for a connection that consists of a mated pair of optical connectors.

The maximum link distances for multimode fiber are calculated based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an average insertion loss equal to 0.5 dB (or less) per connection. Connections with different loss characteristics may be used provided the requirements of Table 53–13 and Table 53–14 are met.

The maximum link distances for single-mode fiber are calculated based on an allocation of 2.0 dB total connection and splice loss. For example, this allocation supports four connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 53–13 and Table 53–14 are met.

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53.14.2.2 Connection return loss

The return loss for multimode connections shall be greater than 20 dB.

The return loss for single-mode connections shall be greater than 26 dB.

53.14.3 Medium Dependent Interface (MDI)

The 10GBASE-LX4 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the fiber optic cabling. Examples of an MDI include the following:

a) Connectorized fiber pigtail.
b) PMD receptacle.

When connected to the fiber optic cabling, the MDI shall meet the interface performance specifications of:

c) IEC 61753-1-1—Fibre optic interconnecting devices and passive component performance standard—Part 1-1: General and guidance—Interconnecting devices (connectors).
d) IEC 61753-021-2—Fibre optic passive component performance standard—Part 021-2:Fibre optic connectors terminated on single-mode fibre for Category C—Controlled environment, performance Class S.
e) IEC 61753-022-2—Fibre optic passive component performance standard—Part 022-2:Fibre optic connectors terminated on multimode fibre for Category C—Controlled environment, performance Class M.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 53.4.1, not at the MDI.

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53.15 Protocol implementation conformance statement (PICS) proforma for Clause 53, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-LX4[103]

53.15.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 53, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-LX4 (Long Wavelength Laser), shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

53.15.2 Identification

53.15.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

53.15.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 53, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-LX4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[103] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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53.15.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
LX4	10GBASE-LX4 PMD	53.1	Device supports long wavelength operation (1269–1356 nm)	O/1	Yes [ ] No [ ]
*INS	Installation / cable	53.13	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
OFP	Single-mode offset-launch mode-conditioning patch cord	53.6	Items marked with OFP include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Standardized reference point TP1 exposed and available for testing	53.4.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Standardized reference point TP4 exposed and available for testing	53.4.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	53.2	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO capability	53.3	Registers and interface supported	O	Yes [ ] No [ ]

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53.15.4 PICS proforma tables for 10GBASE-LX4 and baseband medium

53.15.4.1 PMD Functional specifications

Item	Feature	Sub clause	Value/Comment	Status	Support
FN1	Integration with 10GBASE-X PCS and PMA and management functions	53.1		M	Yes [ ]
FN2	Transmit function	53.4.2	Convey bits requested by PMD_UNITDATA.request() to the MDI	M	Yes [ ]
FN3	Optical multiplexing and delivery to the MDI	53.4.2	Optically multiplexes the four optical signals for delivery to the MDI	M	Yes [ ]
FN4	Mapping between optical signal and logical signal for transmitter	53.4.2	Higher optical power is a one	M	Yes [ ]
FN5	Receive function	53.4.3	Convey bits received from the MDI to PMD_UNITDATA.indication(rx_bit<0:3>)	M	Yes [ ]
FN6	Conversion of four optical signals to four electrical signals	53.4.3	Converts the four optical signals into four electrical bit streams for delivery to the PMD service	M	Yes [ ]
FN7	Mapping between optical signal and logical signal for receiver	53.4.3	Higher optical power is a one	M	Yes [ ]
FN8	Receive function behavior	53.4.3	Conveys bits from PMD service primitive to the PMD service interface	M	Yes [ ]
FN9	Global Signal Detect function	53.4.4	Report to the PMD service interface the message PMD_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
FN10	Global Signal Detect behavior	53.4.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all four lanes	M	Yes [ ]
FN11	Lane-by-Lane Signal Detect function	53.4.5	Sets PMD_signal_detect_n values on a lane-by-lane basis per requirements of Table 53–4	MD:O	Yes [ ] No [ ] N/A [ ]
FN12	PMD_reset function	53.4.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

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53.15.4.2 PMD to MDI optical specifications for 10GBASE-LX4

Item	Feature	Subclause	Value/Comment	Status	Support
PMS1	Wavelength division multiplexed lane assignment	53.5	Device supports passbands defined in Table 53–5	M	Yes [ ] N/A [ ]
PMS2	Transmitter meets specifications in Table 53–7	53.7.1	Per measurement techniques in 53.9	M	Yes [ ] N/A [ ]
PMS3	Receiver meets specifications in Table 53–8	53.7.2	Per measurement techniques in 53.9	M	Yes [ ] N/A [ ]

53.15.4.3 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MR1	Management register set	53.3		MD:M	Yes [ ] N/A [ ]
MR2	Global transmit disable function	53.4.7	Disables all of the optical transmitters with the Global_PMD_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
MR3	PMD_lane_by_lane_transmit_disable function	53.4.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_n variable	MD:O.2	Yes [ ] No [ ] N/A [ ]
MR4	PMD_lane_by_lane_transmit_disable	53.4.8	Disables each optical transmitter independently if MR3 = NO	O.2	Yes [ ] No [ ]
MR5	PMD_fault function	53.4.9	Sets PMD_fault to a logical 1 if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
MR6	PMD_transmit_fault function	53.4.10	Sets PMD_transmit_fault to a logical 1 if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
MR7	PMD_receive_fault function	53.4.11	Sets PMD_receive_fault to a logical 1 if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

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53.15.4.4 Jitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
JS1	Transmit jitter	53.8.1	Meet BER “bathtub curve” specifications	M	Yes [ ]
JS2	Channel transmit jitter	53.8.1.1	As described in steps a) through c) in 53.8.1.1	M	Yes [ ]
JS3	Channel transmit jitter	53.8.1.1	Also tested on MMF as defined in 53.9.10.1	M	Yes [ ]
JS4	Receive jitter	53.8.2	BER less than 10^{-12}	M	Yes [ ]
JS5	Receive jitter	53.8.2.1	Meets requirements of the receiver input jitter mask	M	Yes [ ]
JS6	Receive jitter	53.8.2.1	Uniform spectral content over the measurement frequency range of 18.75kHz to 1.5GHz	M	Yes [ ]
JS7	Receive jitter	53.8.2.1	Using a Clock Recovery Unit	M	Yes [ ]
JS8	Receive jitter	53.8.2.1	Using a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade	M	Yes [ ]
JS9	Receive jitter	53.8.2.1	Using fourth-order Bessel-Thomson filter	M	Yes [ ]
JS10	Receive jitter	53.8.2.2	Meets the requirements of Table 53–11	M	Yes [ ]
JS11	Receive jitter	53.8.2.2	Sinusoidal jitter added to the test signal in compliance with 53.8.2.1	M	Yes [ ]

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53.15.4.5 Optical measurement requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Length of patch cord used for measurements	53.9	2 to 5 m	M	Yes [ ]
OM2	Wavelength ranges	53.9.1	Wavelengths fall within ranges specified inTable 53–5, and under modulated conditions using valid 10GBASE-X signals	M	Yes [ ]
OM3	Optical power measurements	53.9.2	Per IEC 61280-1-1 or ANSI/TIA/EIA-455-95	M	Yes [ ]
OM4	Source spectral window measurements	53.9.3	Individually measured per test setup in Figure 53–7, with all other channels below –30 dBm	M	Yes [ ]
OM5	Source spectral window measurements	53.9.3	Under modulated conditions using valid 10GBASE-X signals	M	Yes [ ]
OM6	Extinction ratio measurements	53.9.4	Per IEC 61280-2-2	M	Yes [ ]
OM7	OMA measurements	53.9.5	Each channel tested individually per methodology defined in 52.9.5	M	Yes [ ]
OM8	$RIN_{12}OMA$	53.9.6	Each channel tested individually per methodology defined in 52.9.6		Yes [ ]
OM9	Transmit eye	53.9.7	Per IEC 61280-2-2	M	Yes [ ]
OM10	Transmit eye mask measurement conditions	53.9.7	Using fourth-order Bessel-Thomson filter	M	Yes [ ]
OM11	Transmit eye mask measurement conditions	53.9.7	Using a Clock Recovery Unit to trigger the scope	M	Yes [ ]
OM12	Transmit eye mask measurement conditions	53.9.7	Using a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade	M	Yes [ ]
OM13	Transmit rise/fall characteristics conditions	53.9.8	Waveforms conform to mask in Figure 53–8, measured from 20% to 80%, using a patch cord	M	Yes [ ]
OM14	Transmit rise/fall characteristics conditions	53.9.8	Removed mask conforming filter mathematically	M	Yes [ ]
OM15	Transmit rise/fall characteristics conditions	53.9.8	Mask filters use a fourth-order Bessel-Thomson filter	M	Yes [ ]
OM16	Receive sensitivity measurement conditions	53.9.9	Using conformance test at TP3 and meeting conditions specified in Table 53–8	M	Yes [ ]
OM17	Transmit jitter conformance measurement conditions	53.9.10.1	Using a fourth-order Bessel-Thomson filter for single-mode fiber	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
OM18	Transmit jitter conformance measurement conditions	53.9.10.1	Using a fourth-order Bessel-Thomson filter followed by a transversal filter with 2 equal amplitude paths with a differential delay of 157 ps for multimode fiber	M	Yes [ ]
OM19	Transmit jitter conformance measurement conditions	53.9.10.1	Using a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade	M	Yes [ ]
OM20	Transmit jitter conformance measurement conditions	53.9.10.1	Measured at the average value of the overall waveform	M	Yes [ ]
OM21	Transmit jitter conformance measurement conditions	53.9.10.1	Asynchronous data flowing in all four optical receiver channels	M	Yes [ ]
OM22	Transmit jitter conformance measurement conditions	53.9.10.2	Meets requirements listed in Table 53–12	M	Yes [ ]
OM23	Transmit jitter conformance measurement conditions	53.9.10.2	For single-mode fiber; compliant with dispersion at least as negative as the “minimum dispersion” and at least as positive as the “maximum dispersion”	M	Yes [ ]
OM24	Transmit jitter conformance measurement conditions	53.9.10.2	Achieved using ITU-T G.652 fiber	M	Yes [ ]
OM25	Transmit jitter conformance measurement conditions	53.9.10.2	Using the linear regime of the single-mode fiber	M	Yes [ ]
OM26	Transmit jitter conformance measurement conditions	53.9.10.2	Provide an optical back reflection specified in Table 53–7	M	Yes [ ]
OM27	Transmit jitter conformance measurement conditions	53.9.10.2	Back reflection adjusted to create the greatest RIN	M	Yes [ ]
OM28	Transmit jitter conformance measurement conditions	53.9.10.2	For multimode fiber, back reflection set to –12 dB	M	Yes [ ]
OM29	Transmit jitter conformance measurement conditions	53.9.10.3	Using a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade	M	Yes [ ]
OM30	Receiver sensitivity	53.9.11	Meet the specifications in Table 53–8	M	Yes [ ]
OM31	Stressed receiver conformance conditions	53.9.12	Asynchronous data flowing out of the optical transmitter of the system under test	M	Yes [ ]
OM32	Stressed receiver conformance conditions	53.9.12	Data is consistent with normal signal properties and content	M	Yes [ ]
OM33	Stressed receiver conformance conditions	53.9.12.1	Using a Clock Recovery Unit meeting the requirements of 53.8.2.1	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
OM34	Stressed receiver conformance conditions	53.9.12.1	Calibrated at the average value of the overall optical waveform	M	Yes [ ]
OM35	Stressed receiver conformance conditions	53.9.12.3	Using a Clock Recovery Unit meeting the requirements of 53.8.2.1	M	Yes [ ]
OM36	Receiver 3dB electrical upper cutoff frequency	53.9.13	Performed on each channel independently using a laser source with its output wavelength within the specified wavelength range of the channel to be tested	M	Yes [ ]
OM37	Receiver 3dB electrical upper cutoff frequency	53.9.13	As described in steps a) through e) of 53.9.13	M	Yes [ ]
OM38	Compliance test signal at TP3	53.9.14	Meets the requirements of Figure 53–12	M	Yes [ ]
OM39	Compliance test signal at TP3	53.9.14	DJ eye closure no less than 14 ps	M	Yes [ ]
OM40	Compliance test signal at TP3	53.9.14	Vertical eye-closure penalty meets requirements of Table 53–8	M	Yes [ ] N/A [ ]
OM41	Compliance test signal at TP3	53.9.14	Bandwidth of photodetector > 2.34GHz, and couple through fourth-order Bessel-Thomson filter	M	Yes [ ]
OM42	Receiver WDM conformance conditions	53.9.15	As described in steps a) through f) of 53.9.15	M	Yes [ ]
OM43	General safety	53.10.1	Conform to J.2	M	Yes [ ]
OM44	Laser safety	53.10.2	Hazard Level 1	M	Yes [ ]
OM45	Compliance with all requirements over the life of the product	53.11		M	Yes [ ]
OM46	Compliance with applicable local and national codes for the limitation of electromagnetic interference	53.11.1		M	Yes [ ]

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53.15.4.6 Characteristics of the fiber optic cabling

Item	Feature	Subclause	Value/Comment	Status	Support
LI1	Fiber optic cabling	53.13	Meets specifications in Table 53–13	INS:M	Yes [ ] N/A [ ]
LI2	Return loss for multimode connections	53.14.2.2	> 20 dB	INS:M	Yes [ ] No [ ] N/A [ ]
LI3	Return loss for single-mode connections	53.14.2.2	> 26 dB	INS:M	Yes [ ] No [ ] N/A [ ]
LI4	MDI	53.14.3	IEC 61753-1-1 and IEC 61753-3-2	M	Yes [ ]

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54. Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4

54.1 Overview

This clause specifies the 10GBASE-CX4 PMD (including MDI) and the baseband medium. In order to form a complete PHY (Physical Layer device), a PMD is combined with the appropriate sublayers (see Table 54–1) and with the management functions, which are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 54–1—Physical Layer clauses associated with the 10GBASE-CX4 PMD

Associated clause	10GBASE-CX4
46—XGMII[a]	Optional
47—XGXS and XAUI	Optional
48—10GBASE-X PCS/PMA	Required

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation behaves functionally as though the RS and XGMII were present.

Figure 54–1 shows the relationship of the 10GBASE-CX4 PMD sublayers and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.

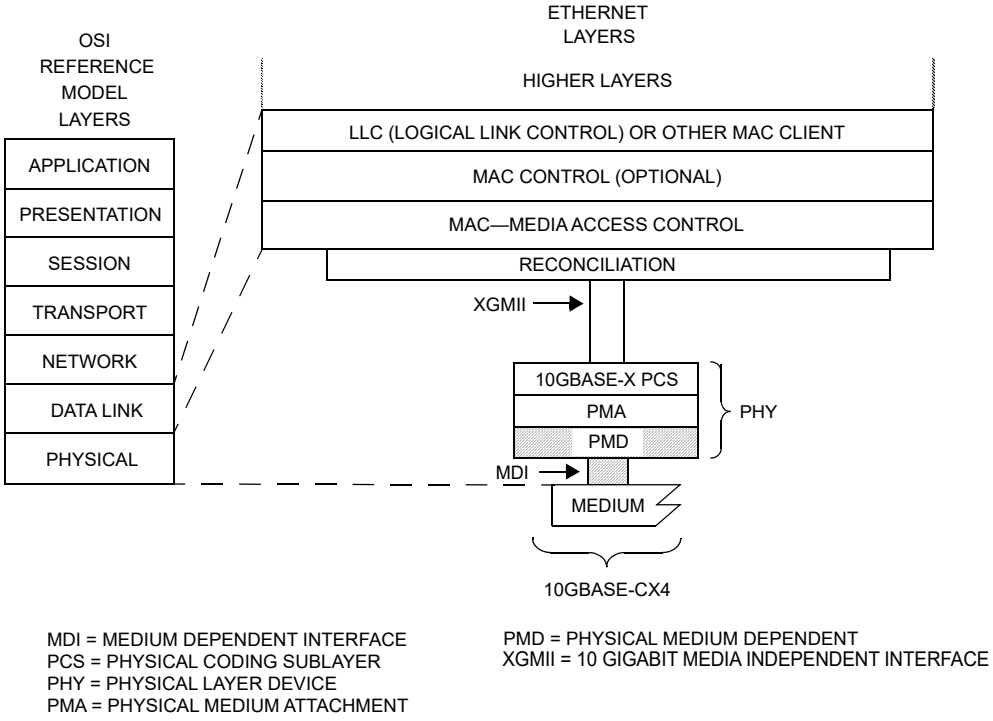

Figure 54–1—10GBASE-CX4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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54.2 Physical Medium Dependent (PMD) service interface

The 10GBASE-CX4 PMD utilizes the PMD service interface defined in 53.1.1. The PMD service interface is summarized as follows:

PMD_UNITDATA.request
PMD_UNITDATA.indication
PMD_SIGNAL.indication

54.3 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that implementers of MAC, MAC Control, and PHY consider the delay maxima, and that network planners and administrators consider the delay constraints regarding the cable topology and concatenation of devices. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 44.3.

The sum of the transmit and the receive delays contributed by the 10GBASE-CX4 PMD shall be no more than 512 BT or 1 pause_quantum.

54.4 PMD MDIO function mapping

The 10GBASE-CX4 PMD uses the same MDIO function mapping as 10GBASE-LX4, as defined in 53.3.

54.5 PMD functional specifications

The 10GBASE-CX4 PMD performs the transmit and receive functions (which convey data between the PMD service interface and the MDI), and provides various management functions if the optional MDIO is implemented.

54.5.1 Link block diagram

A 10GBASE-CX4 link is shown in Figure 54–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The electrical transmit signal is defined at the output end of the mated connector (TP2). Unless specified otherwise, all transmitter measurements and tests defined in 54.6.3 are made at TP2. Unless specified otherwise, all receiver measurements and tests defined in 54.6.4 are made at the input end of the mated connector (TP3). A mated connector pair has been included in both the transmitter and receiver specifications defined in 54.6.3 and 54.6.4. Two mated connector pairs have been included in the cable assembly specifications defined in 54.7.

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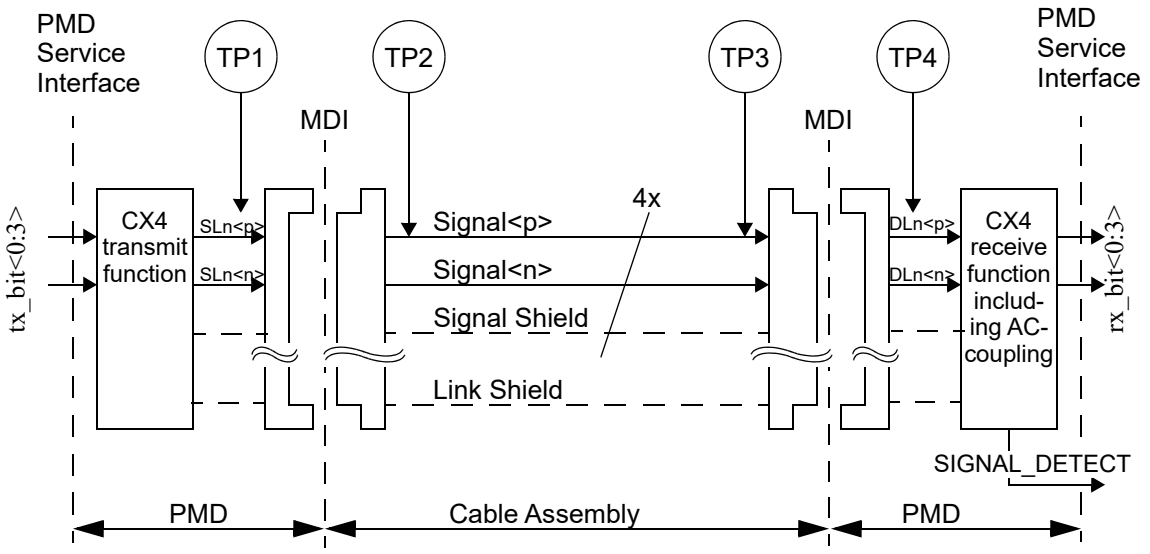

Figure 54–2—10GBASE-CX4 link (half link is shown)

NOTE—SLn<p> and SLn<n> are the positive and negative sides of the transmit differential signal pair and DLn<p> and DLn<n> are the positive and negative sides of the receive differential signal pair for lane n (n = 0, 1, 2, 3).

54.5.2 PMD Transmit function

The PMD Transmit function shall convert the four logical bit streams requested by the PMD service interface message PMD_UNITDATA.request (tx_bit<0:3>) into four separate electrical signals. The four electrical signals shall then be delivered to the MDI, all according to the transmit electrical specifications in 54.6.3. A positive output voltage of SLn<p> minus SLn<n> (differential voltage) shall correspond to tx_bit = ONE.

The PMD shall convey the bits received from the PMD service interface using the message PMD_UNITDATA.request(tx_bit<0:3>) to the MDI lanes, where (SL0<p>/<n>, SL1<p>/<n>, SL2<p>/<n>, SL3<p>/<n>) = tx_bit<0:3>.

54.5.3 PMD Receive function

The PMD Receive function shall convert the four electrical signals from the MDI into four logical bit streams for delivery to the PMD service interface using the message PMD_UNITDATA.indication (rx_bit<0:3>), all according to the receive electrical specifications in 54.6.4. A positive input voltage level in each signal of DLn<p> minus DLn<n> (differential voltage) shall correspond to a rx_bit = ONE.

The PMD shall convey the bits received from the MDI lanes to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit<0:3>), where rx_bit<0:3> = (DL0<p>/<n>, DL1<p>/<n>, DL2<p>/<n>, DL3<p>/<n>).

54.5.4 Global PMD signal detect function

The Global_PMD_signal_detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs.

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SIGNAL_DETECT is a global indicator of the presence of electrical signals on all four lanes. The PMD receiver is not required to verify whether a compliant 10GBASE-CX4 signal is being received; however, it shall assert SIGNAL_DETECT = OK within 100 μs after the absolute differential peak-to-peak input voltage on each of the four lanes at the MDI has exceeded 175 mV for at least 1 UI (unit interval).

After any such assertion of SIGNAL_DETECT = OK, SIGNAL_DETECT = FAIL shall not be asserted for at least 250 μs. The PMD shall have asserted SIGNAL_DETECT = FAIL when the absolute differential peak-to-peak input voltage on any of the four lanes at the MDI has dropped below 50 mV and has remained below 50 mV for longer than 500 μs.

Table 54–2—SIGNAL_DETECT summary

Parameter	Value	Units
SIGNAL_DETECT = OK level (maximum differential peak-to-peak amplitude)	175	mV
SIGNAL_DETECT = OK width (minimum)	1	UI
SIGNAL_DETECT = OK assertion time (maximum)	100	μs
SIGNAL_DETECT = FAIL level (minimum differential peak-to-peak amplitude)	50	mV
SIGNAL_DETECT = FAIL de-assertion time maximum minimum	 500 250	 μs μs

NOTE—SIGNAL_DETECT may not activate with a continuous 1010… pattern, such as the high-frequency pattern of 48A.1, but it will be activated by an interpacket gap (IPG).

54.5.5 PMD lane-by-lane signal detect function

When the MDIO is implemented, each PMD_signal_detect_n value, where n represents the lane number in the range 0:3, shall be continuously updated in response to the amplitude of the receive signal on its associated lane, according to the requirements of 54.5.4.

54.5.6 Global PMD transmit disable function

The Global_PMD_transmit_disable function is optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When a Global_PMD_transmit_disable variable is set to ONE, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage in Table 54–3.
b) If a PMD_fault (54.5.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 54.5.8, shall not be affected by Global_PMD_transmit_disable.

54.5.7 PMD lane-by-lane transmit disable function

The PMD_transmit_disable_n function is optional. It allows the electrical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_n variable is set to ONE, this function shall turn off the transmitter associated with that variable such that the corresponding transmitter drives a constant level (i.e., no

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transitions) and does not exceed the maximum differential peak-to-peak output voltage in Table 54–3.

b) If a PMD_fault (54.5.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 54.5.8, shall not be affected by PMD_transmit_disable_n.

NOTE—Turning off a transmitter can be disruptive to a network.

54.5.8 Loopback mode

Loopback mode shall be provided for the 10GBASE-CX4 PMD by the transmitter and receiver of a device as a test function to the device. When loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. The transmitters shall not be disabled when loopback mode is enabled. A device has to be explicitly placed in loopback mode because loopback mode is not the normal mode of operation of a device. Loopback applies to all lanes as a group (the lane 0 transmitter is directly connected to the lane 0 receiver, the lane 1 transmitter is directly connected to the lane 1 receiver, etc.). The method of implementing loopback mode is not defined by this standard.

Control of the loopback function is specified in 45.2.1.1.5.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

54.5.9 PMD fault function

If the MDIO is implemented, and the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to ONE; otherwise, the PMD shall set PMD_fault to ZERO.

54.5.10 PMD transmit fault function

If the MDIO is implemented, and the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to ONE; otherwise, the PMD shall set PMD_transmit_fault to ZERO.

54.5.11 PMD receive fault function

If the MDIO is implemented, and the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to ONE; otherwise, the PMD shall set PMD_receive_fault to ZERO.

54.6 MDI Electrical specifications for 10GBASE-CX4

54.6.1 Signal levels

The 10GBASE-CX4 MDI is a low-swing AC-coupled differential interface. Transmitter to receiver path AC-coupling, as defined in 54.6.4.3, allows for interoperability between components operating from different supply voltages. Low-swing differential signaling provides noise immunity and improved electromagnetic interference (EMI).

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54.6.2 Signal paths

The 10GBASE-CX4 MDI signal paths are point-to-point connections. Each path corresponds to a 10GBASE-CX4 MDI lane and comprises two complementary signals, which form a balanced differential pair. There are four differential paths in each direction for a total of eight pairs, or sixteen connections. The signal paths are intended to operate on twinaxial cable assemblies up to 15 m in length, as described in 54.7.

54.6.3 Transmitter characteristics

Transmitter characteristics shall meet specifications at TP2, unless otherwise noted. The specifications are summarized in Table 54–3 and detailed in 54.6.3.1 through 54.6.3.9.

Table 54–3—Transmitter characteristics' summary[a]

Parameter	Subclause reference	Value	Units
Signaling speed, per lane	54.6.3.3	3.125 ± 100 ppm	GBd
Unit interval nominal	54.6.3.3	320	ps
Differential peak-to-peak output voltage maximum minimum	54.6.3.4	 1200 800	 mV mV
Differential peak-to-peak output voltage difference (maximum)	54.6.3.4	 150	 mV
Common-mode voltage limits maximum minimum	54.6.3.4	 1.9 –0.4	 V V
Differential output return loss minimum	54.6.3.5	[See Equation (54–1) and Equation (54–2)]	dB
Differential output template	54.6.3.6	(See Figure 54–6 and Table 54–4)	V
Transition time maximum minimum	54.6.3.7	 130 60	 ps ps
Output jitter (peak-to-peak) Random jitter Deterministic jitter[b] Total jitter	54.6.3.8	 0.27 0.17 0.35	 UI UI UI

[a] Should there be a discrepancy between this table and the requirements of the referenced subclause, the subclause prevails.
[b] Deterministic jitter is already incorporated into the differential output template.

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54.6.3.1 Test fixtures

The test fixture of Figure 54–3, or its functional equivalent, is required for measuring the transmitter specifications described in 54.6.3.

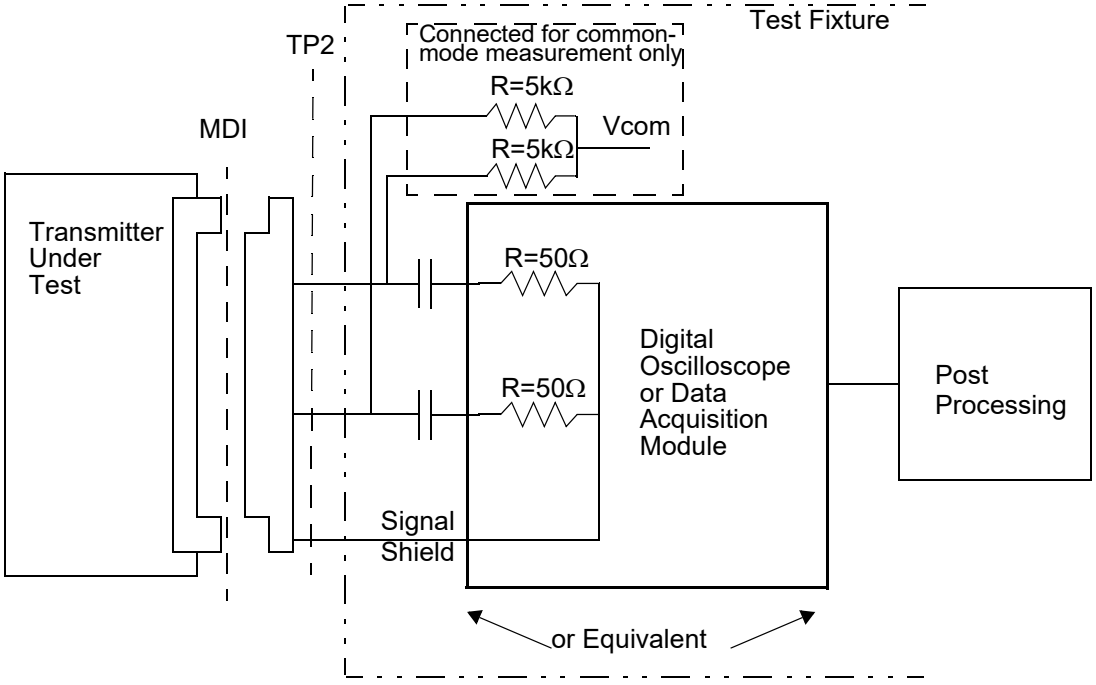

Figure 54–3—Transmit test fixture

54.6.3.2 Test-fixture impedance

The differential load impedance applied to the transmitter output by the test fixture depicted in Figure 54–3 shall have a return loss greater than 20 dB from 100 MHz to 2000 MHz. The reference impedance for differential return loss measurements shall be 100 Ω.

54.6.3.3 Signaling speed range

The 10GBASE-CX4 MDI signaling speed shall be 3.125 GBd ±100 ppm. The corresponding unit interval is nominally 320 ps.

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54.6.3.4 Output amplitude

While transmitting the test pattern specified in 48A.2:

a) The transmitter maximum differential peak-to-peak output voltage shall be less than 1200 mV.
b) The minimum differential peak-to-peak output voltage shall be greater than 800 mV.
c) The maximum difference between any two lanes' differential peak-to-peak output voltage shall be less than or equal to 150 mV.

See Figure 54–4 for an illustration of the definition of differential peak-to-peak output voltage.

DC-referenced logic levels are not defined since the receiver is AC-coupled. The common-mode voltage of SLn<p> and SLn<n> shall be between –0.4 V and 1.9 V with respect to Signal Shield as measured at Vcom in Figure 54–3.

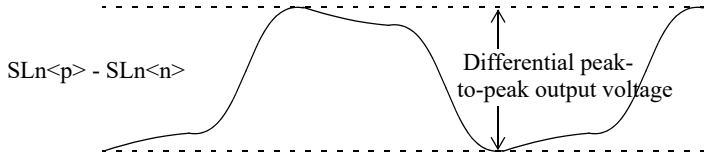

Figure 54–4—Transmitter differential peak-to-peak output voltage definition

NOTE—SLn<p> and SLn<n> are the positive and negative sides of the differential signal pair for Lane n (n = 0,1,2,3).

54.6.3.5 Output return loss

For frequencies from 100 MHz to 2000 MHz, the differential return loss, in dB with f in MHz, of the transmitter shall meet Equation (54–1) and Equation (54–2). This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$Return\ Loss\ (f) \geq 10 \tag{54–1}$$

for 100 MHz ≤ f < 625 MHz and

$$Return\ Loss\ (f) \geq 10 - 10 \times \log\left(\frac{f}{625}\right) \tag{54–2}$$

for 625 MHz ≤ f ≤ 2000 MHz.

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The minimum transmit differential output return loss is shown in Figure 54–5.

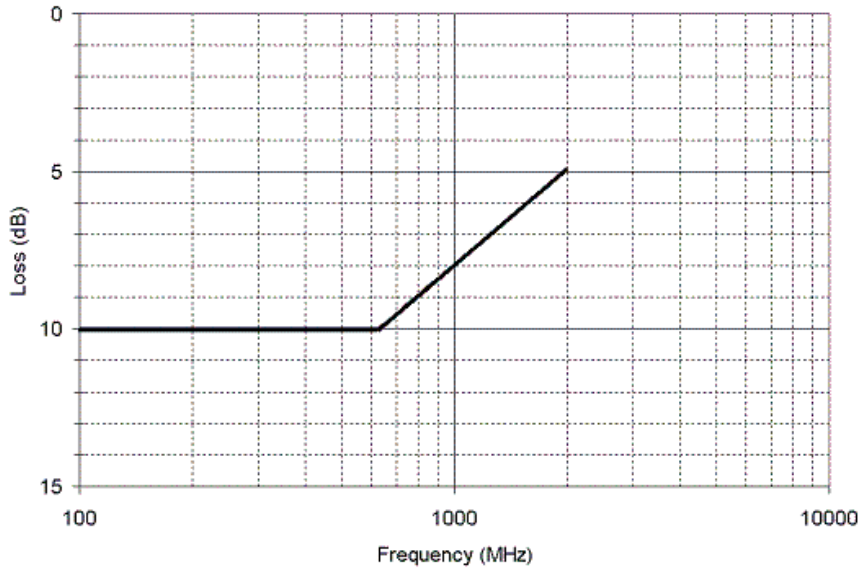

Figure 54–5—Illustration of minimum transmit differential output return loss

54.6.3.6 Differential output template

The transmitter differential output signal is defined at TP2, as shown in Figure 54–2. The transmitter shall provide equalization such that the output waveform falls within the template shown in Figure 54–6 for the test pattern specified in 48A.2, with all other transmitters active. Voltage and time coordinates for inflection points on Figure 54–6 are given in Table 54–4. The signals on each pair at TP2 shall meet the transmit template specifications when connected to the transmitter test fixture shown in Figure 54–3, with all other transmitters active. The waveform under test shall be normalized by using the following procedure:

1) Align the output waveform under test, to achieve the best fit along the horizontal time axis.
2) Calculate the +1 low frequency level as V_{lowp} = average of any 2 successive unit intervals (2UI) between 2.5 UI and 5.5 UI.
3) Calculate the 0 low frequency level as V_{lowm} = average of any 2 successive unit intervals (2UI) between 7.5 UI and 10.5 UI.
4) Calculate the vertical offset to be subtracted from the waveform as $V_{off} = (V_{lowp} + V_{lowm}) / 2$.
5) Calculate the vertical normalization factor for the waveform as $V_{norm} = (V_{lowp} - V_{lowm}) / 2$.
6) Calculate the normalized waveform as Normalized_Waveform=(Original_Waveform – V_{off}) × ($0.69/V_{norm}$).
7) Align the Normalized_Waveform under test, to achieve the best fit along the horizontal time axis.

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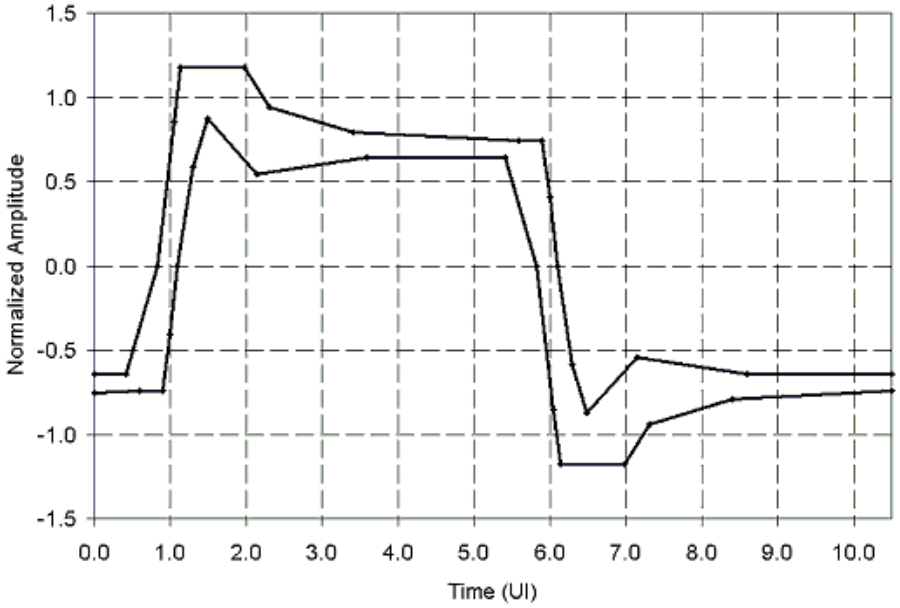

Figure 54–6—Normalized transmit template

Table 54–4—Normalized transmit time domain template

Upper limit				Lower limit			
Time (UI)	Amplitude	Time (UI)	Amplitude	Time (UI)	Amplitude	Time (UI)	Amplitude
0.000	–0.640	5.897	0.740	0.000	–0.754	5.409	0.640
0.409	–0.640	5.997	0.406	0.591	–0.740	5.828	0.000
0.828	0.000	6.094	0.000	0.897	–0.740	6.050	–0.856
1.050	0.856	6.294	–0.586	0.997	–0.406	6.134	–1.175
1.134	1.175	6.491	–0.870	1.094	0.000	6.975	–1.175
1.975	1.175	7.141	–0.546	1.294	0.586	7.309	–0.940
2.309	0.940	8.591	–0.640	1.491	0.870	8.500	–0.790
3.409	0.790	10.500	–0.640	2.141	0.546	10.500	–0.742
5.591	0.740	—	—	3.591	0.640	—	—

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54.6.3.7 Transition time

The rising-edge transition time shall be between 60 ps and 130 ps as measured at the 20% and 80% levels of the peak-to-peak differential value of the waveform using the high-frequency test pattern of 48A.1. The falling edge transition time shall be between 60 ps and 130 ps as measured at the 80% and 20% levels of the peak-to-peak differential value of the waveform using the high-frequency test pattern of 48A.1.

54.6.3.8 Transmit jitter

The transmitter shall satisfy the jitter requirements of 54.6.3.9 with a maximum total jitter of 0.350 UI peak-to-peak, a maximum deterministic component of 0.170 UI peak-to-peak and a maximum random component of 0.270 UI peak-to-peak. Jitter specifications include all but 10^{-12} of the jitter population. Transmit jitter test requirements are specified in 54.6.3.9.

54.6.3.9 Transmit jitter test requirements

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in Annex 48B. For the purpose of jitter measurement, the effect of a single-pole, high-pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements shall be the CJPAT pattern defined in 48A.5. All four lanes of the 10GBASE-CX4 transceiver are active in both directions, and opposite ends of the link use asynchronous clocks. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal.

54.6.4 Receiver characteristics

Receiver characteristics are summarized in Table 54–5 and detailed in 54.6.4.1 through 54.6.4.5.

Table 54–5—Receiver characteristics' summary[a]

Parameter	Subclause reference	Value	Units
Bit error ratio	54.6.4.1	10^{-12}	
Signaling speed, per lane	54.6.4.2	3.125 ± 100 ppm	GBd
Unit interval (UI) nominal	54.6.4.2	320	ps
Receiver coupling	54.6.4.3	AC	—
Differential input peak-to-peak amplitude (maximum)	54.6.4.4	1200	mV
Return loss[b] differential (minimum)	54.6.4.5	[See Equation (54–1) and Equation (54–2)]	dB

[a] Should there be a discrepancy between this table and the requirements of the referenced subclause, the subclause prevails.
[b] Relative to 100 Ω differential.

54.6.4.1 Bit error ratio

The receiver shall operate with a BER of better than 10^{-12} when receiving a compliant transmit signal, as defined in 54.6.3, through a compliant cable assembly as defined in 54.7.

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NOTE—The BER should be met with a worst-case insertion loss, long cable, as well as a low-loss, short cable. The low-loss cable may be a more stringent requirement on the system due to higher reflections and crosstalk than with long cables.

54.6.4.2 Signaling speed range

A 10GBASE-CX4 receiver shall comply with the requirements of 54.6.4.1 for any signaling speed in the range 3.125 GBd ± 100 ppm. The corresponding unit interval is nominally 320 ps.

54.6.4.3 AC-coupling

The 10GBASE-CX4 receiver shall be AC-coupled to the cable assembly to allow for maximum interoperability between various 10 Gb/s components. AC-coupling is considered to be part of the receiver for the purposes of this standard unless explicitly stated otherwise. It should be noted that there may be various methods for AC-coupling in actual implementations.

NOTE—It is recommended that the maximum value of the coupling capacitors be limited to 470 pF. This will limit the inrush currents to the receiver that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

54.6.4.4 Input signal amplitude

10GBASE-CX4 receivers shall accept differential input signal peak-to-peak amplitudes produced by compliant transmitters connected without attenuation to the receiver, and still meet the BER requirement specified in 54.6.4.1. Note that this may be larger than the 1200 mV differential maximum of 54.6.3.4 due to the actual transmitter output and receiver input impedances. The input impedance of a receiver can cause the minimum signal into a receiver to differ from that measured when the receiver is replaced with a 100 Ω test load. Since the 10GBASE-CX4 receiver is AC-coupled, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

54.6.4.5 Input return loss

For frequencies from 100 MHz to 2000 MHz, the differential return loss (in dB with f in MHz) of the receiver shall be greater than or equal to Equation (54–1) and Equation (54–2). The reference impedance for differential return loss measurements is 100 Ω.

54.7 Cable assembly characteristics

The 10GBASE-CX4 cable assembly contains insulated conductors terminated in a connector at each end for use as a link segment between MDIs. This cable assembly is primarily intended as a point-to-point interface of up to 15 m between network ports using controlled impedance cables. All cable assembly measurements

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are to be made between TP1 and TP4 as shown in Figure 54–2. These cable assembly specifications are based upon twinaxial cable characteristics, but other cable types are acceptable if the specifications are met.

Table 54–6—Cable assembly differential characteristics' summary[a]

Description	Reference	Value	Unit
Maximum Insertion loss at 1.5625 GHz	54.7.2 and 54.7.3	16	dB
Minimum Return loss at 1.5625 GHz	54.7.3	12.0	dB
Minimum NEXT loss at 1.5625 GHz	54.7.4.1	31.8	dB
Minimum MDNEXT loss at 1.5625 GHz	54.7.4.2	29.8	dB
Minimum ELFEXT loss at 1.5625 GHz	54.7.5.1	23.3	dB
Minimum MDELFEXT loss at 1.5625 GHz	54.7.5.2	21.1	dB

[a] Should there be a discrepancy between this table and the requirements of the referenced subclause, the subclause prevails.

54.7.1 Characteristic impedance and reference impedance

The nominal differential characteristic impedance of the cable assembly is 100 Ω. The differential reference impedance for cable assembly specifications shall be 100 Ω.

54.7.2 Cable assembly insertion loss

The insertion loss (in dB with f in MHz) of each pair of the 10GBASE-CX4 cable assembly shall be:

$$Insertion\ Loss\ (f) \leq (0.2629 \times \sqrt{f}) + (0.0034 \times f) + \left(\frac{12.76}{\sqrt{f}}\right) \quad (54\text{–}3)$$

for all frequencies from 100 MHz to 2000 MHz. This includes the attenuation of the differential cabling pairs and the assembly connectors.

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The maximum cable assembly insertion loss is shown in Figure 54–7.

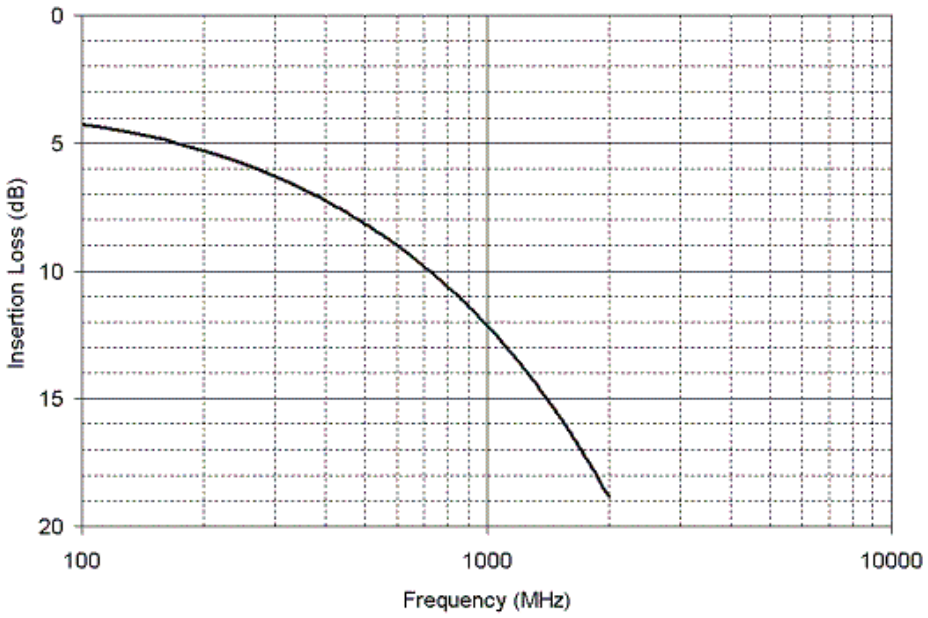

Figure 54–7—Illustration of maximum cable assembly insertion loss

54.7.3 Cable assembly return loss

The return loss (in dB with f in MHz) of each pair of the 10GBASE-CX4 cable assembly shall be:

$$Return\ Loss(f) \geq 22.35 - 17.19 \times \log\left(\frac{f}{100}\right) \quad (54\text{–}4)$$

for 100 MHz $\leq f <$ 400 MHz.

$$Return\ Loss(f) \geq 12 \quad (54\text{–}5)$$

for 400 MHz $\leq f \leq$ 2000 MHz.

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The minimum cable assembly return loss is shown in Figure 54–8.

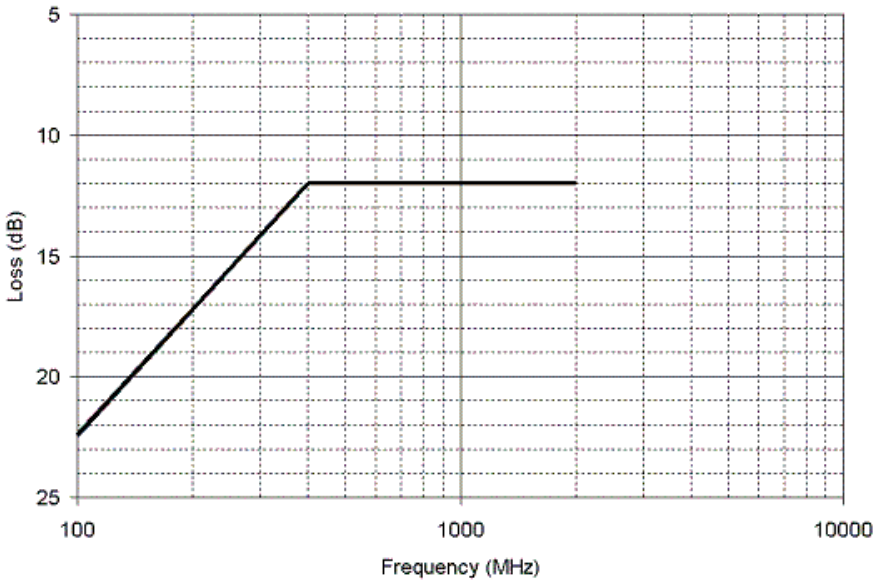

Figure 54–8—Illustration of minimum cable assembly return loss

54.7.4 Near-End Crosstalk (NEXT)

54.7.4.1 Differential Near-End Crosstalk

In order to limit the crosstalk at the near end of a link segment, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between any of the four transmit lanes and any of the four receive lanes is specified to meet the BER objective specified in 54.6.4.1. The NEXT loss between any transmit and receive lane of a link segment (in dB with f in MHz) shall be at least:

$$NEXT(f) \geq 30 - 17 \times \log\left(\frac{f}{2000}\right) \quad (54–6)$$

for all frequencies from 100 MHz to 2000 MHz.

54.7.4.2 Multiple Disturber Near-End Crosstalk (MDNEXT)

Since four transmit and four receive lanes are used to transfer data between PMDs, the NEXT that is coupled into a receive lane will be from the four transmit lanes. To ensure the total NEXT coupled into a receive lane is limited, multiple disturber NEXT loss is specified as the power sum of the individual NEXT losses.

The Power Sum loss between a receive lane and the four transmit lanes (in dB with f in MHz) shall be at least:

$$MDNEXT(f) \geq 28 - 17 \times \log\left(\frac{f}{2000}\right) \quad (54–7)$$

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for all frequencies from 100 MHz to 2000 MHz.

MDNEXT loss is determined by summing the power of the four individual pair-to-pair differential NEXT loss values over the frequency range 100 MHz to 2000 MHz as follows:

$$MDNEXT_{\text{loss}}(f) = -10 \times \log\left(\sum_{i=0}^{i=3} 10^{-NL(f)_i/10}\right) \quad (54\text{–}8)$$

where

$MDNEXT_{\text{loss}}(f)$ is the MDNEXT loss at frequency f,
$NL(f)_i$ is the power of the NEXT loss at frequency f of pair combination i, in dB,
f is frequency ranging from 100 MHz to 2000 MHz,
i is the 0, 1, 2, or 3 (pair-to-pair combination).

The minimum cable assembly NEXT / MDNEXT loss is shown in Figure 54–9.

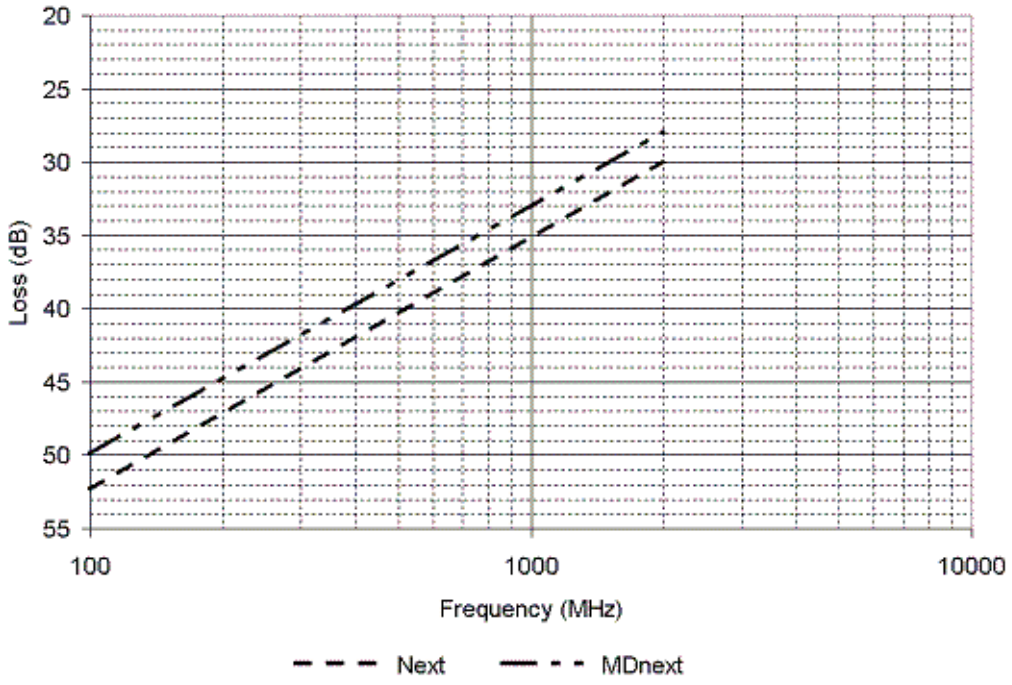

Figure 54–9—Illustration of minimum cable assembly NEXT / MDNEXT loss

54.7.5 Far-End Crosstalk (FEXT)

54.7.5.1 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk at the far end of each link segment and meet the BER objective specified in 54.6.4.1. Far-End Crosstalk (FEXT) is crosstalk that appears at the far end of a lane (disturbed lane), which is coupled from another lane (disturbing lane) with the noise source (transmitters) at the near end. FEXT loss is defined as

$$FEXT\_Loss(f) = 20 \times \log(V\text{pds}(f)/V\text{pcn}(f))$$

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and ELFEXT Loss is defined as

$$ELFEXT\_Loss(f) = 20 \times \log(V\text{pds}(f)/V\text{pcn}(f)) - SLS\_Loss(f)$$

where

FEXT_Loss(*f*)is the FEXT loss at frequency *f,*
ELFEXT_Loss(*f*)is the ELFEXT loss at frequency *f,*
*V*pds is the peak voltage of the disturbing signal (near-end transmitter),
*V*pcn is the peak crosstalk noise at the far end of the disturbed lane,
SLS_Loss(*f*)is the insertion loss of the disturbed lane in dB,
f is frequency ranging from 100 MHz to 2000 MHz.

The worst pair ELFEXT loss between any two lanes shall be at least:

$$ELFEXT(f) \geq 21 - 20 \times \log\left(\frac{f}{2000}\right) \quad (54\text{–}9)$$

for all frequencies from 100 MHz to 2000 MHz.

54.7.5.2 Multiple Disturber Equal Level Far-End Crosstalk (MDELFEXT) loss

Since four lanes are used to transfer data between PMDs, the FEXT that is coupled into a data carrying lane will be from the three other lanes in the same direction. To ensure the total FEXT coupled into a lane is limited, multiple disturber ELFEXT loss is specified as the power sum of the individual ELFEXT losses.

The Power Sum loss (labeled as MDELFEXT) between a lane and the three adjacent disturbers shall be at least:

$$MDELFEXT(f) \geq 19 - 20 \times \log\left(\frac{f}{2000}\right) \quad (54\text{–}10)$$

for all frequencies from 100 MHz to 2000 MHz.

MDELFEXT loss is determined by summing the power of the three individual pair-to-pair differential ELFEXT loss values over the frequency range 100 MHz to 2000 MHz as follows:

$$MDELFEXT_{\text{loss}}(f) = -10 \times \log\left(\sum_{i=0}^{i=3} 10^{-NL(f)_i/10}\right) \quad (54\text{–}11)$$

where

$MDELFEXT_{\text{loss}}(f)$is the MDELFEXT loss at frequency *f*,
$NL(f)_i$ is the power of ELFEXT loss at frequency *f* of pair combination *i*, in dB,
f is frequency ranging from 100 MHz to 2000 MHz,
i is the 1, 2, or 3 (pair-to-pair combination).

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The minimum cable assembly ELFEXT / MDELFEXT loss is shown in Figure 54–10.

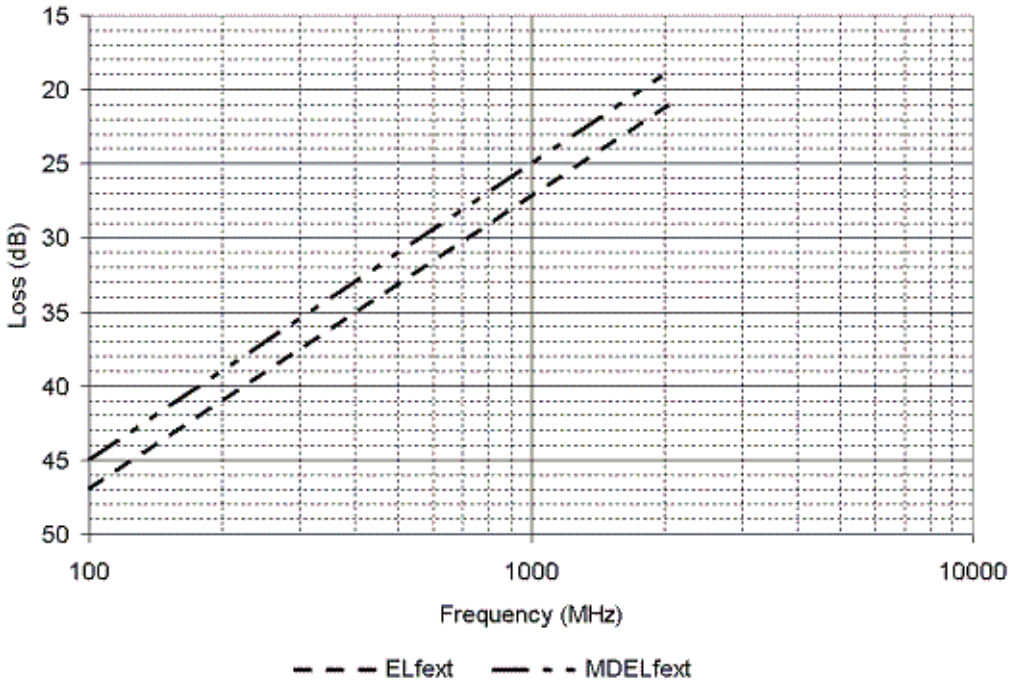

Figure 54–10—Illustration of minimum cable assembly ELFEXT / MDELFEXT loss

54.7.6 Shielding

The cable assembly shall provide Class 2 or better shielding in accordance with IEC 61196-1.

54.7.7 Crossover function

The cable assembly shall be wired in a crossover fashion as shown in Figure 54–11, with each of the four pairs being attached to the transmitter contacts at one end and the receiver contacts at the other end.

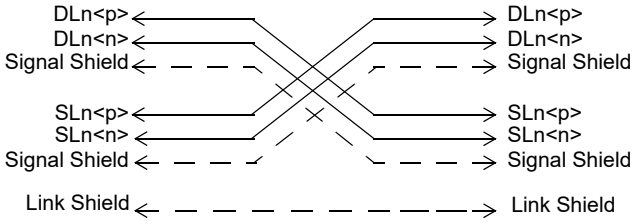

Figure 54–11—Cable wiring

NOTE—SLn<p> and SLn<n> are the positive and negative sides of the differential signal pair for Lane n (n = 0,1,2,3)

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54.8 MDI specification

This subclause defines the Media Dependent Interface (MDI). The 10GBASE-CX4 PMD, as per 54.6, is coupled to the cable assembly, as per 54.7, by the MDI.

54.8.1 MDI connectors

The connector for each end of the cable assembly shall be the latch-type plug with the mechanical mating interface defined by SFF-8470 and illustrated in Figure 54–12. The MDI connector shall be the latch-type receptacle with the mechanical mating interface defined by SFF-8470 and illustrated in Figure 54–13. These connectors have a pinout matching that in Table 54–7, and electrical performance consistent with the signal quality and electrical requirements of 54.6 and 54.7.

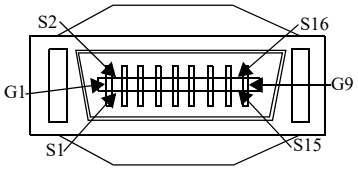

Figure 54–12—Example cable assembly plug

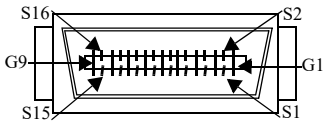

Figure 54–13—Example MDI board receptacle

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54.8.2 Connector pin assignments

The MDI connector of the PMD comprises 16 signal connections, eight signal shield connections, and one link shield connection. The 10GBASE-CX4 PMD MDI connector pin assignments shall be as defined in Table 54–7.

Table 54–7—CX4 lane to MDI connector pin mapping

Rx lane	MDI Connector pin	Tx lane	MDI Connector pin
DL0<p>	S1	SL0<p>	S16
DL0<n>	S2	SL0<n>	S15
DL1<p>	S3	SL1<p>	S14
DL1<n>	S4	SL1<n>	S13
DL2<p>	S5	SL2<p>	S12
DL2<n>	S6	SL2<n>	S11
DL3<p>	S7	SL3<p>	S10
DL3<n>	S8	SL3<n>	S9
Signal Shield	G1	Signal Shield	G5
Signal Shield	G2	Signal Shield	G6
Signal Shield	G3	Signal Shield	G7
Signal Shield	G4	Signal Shield	G8
—	—	Link Shield	G9

54.9 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 14.7.

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54.10 Protocol implementation conformance statement (PICS) proforma for Clause 54, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4[104]

54.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 54 Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

54.10.2 Identification

54.10.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

54.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 54., Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[104]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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54.10.3 PICS proforma tables for 10GBASE-CX4 and baseband medium

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Environmental specifications	54.9		M	Yes [ ]

54.10.4 Major capabilities/options

Item[a]	Feature	Subclause	Value/Comment	Status	Support
XGE	XGMII interface	46, 54.1	Interface is supported	O	Yes [ ] No [ ]
XGXS	XGXS and XAUI	47, 54.1		O	Yes [ ] No [ ]
PCS	Support of 10GBASE-X PCS / PMA	48, 54.1		O	Yes [ ] No [ ]
DC	Delay constraints	54.3	Delay no more than 512 BT or 1 pause_quantum	M	Yes [ ]
*MD	MDIO capability	54.4	Registers and interface supported	O	Yes [ ] No [ ]
*CBL	Cable assembly	54.7	Items marked with CBL include cable assembly specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

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54.10.4.1 PMD Functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PF1	Transmit function	54.5.2	Convert the four logical signals requested by PMD_UNIT-DATA.request (tx_bit<0:3>) to 4 electrical signals	M	Yes [ ]
PF2	Delivery to the MDI	54.5.2	Supplies four electrical signals for delivery to the MDI	M	Yes [ ]
PF3	Mapping between logical signal and electrical signal for transmitter	54.5.2	A positive differential voltage is a one	M	Yes [ ]
PF4	Transmit Signal order	54.5.2	PMD_UNITDATA.request (tx_bit<0:3>) = (SL0<p>/<n>, SL1<p>/<n>, SL2<p>/<n>, SL3<p>/<n>)	M	Yes [ ]
PF5	Receive function	54.5.3	Convert the four electrical signals received from the MDI to 4 logical signals PMD_UNITDATA.indication(rx_bit<0:3>) per 54.6.4	M	Yes [ ]
PF6	Mapping between electrical signal and logical signal for receiver	54.5.3	A positive differential voltage is a one	M	Yes [ ]
PF7	Receive Signal order	54.5.3	(DL0<p>/<n>, DL1<p>/<n>, DL2<p>/<n>, DL3<p>/<n>) = PMD_UNITDATA.indication (rx_bit<0:3>)	M	Yes [ ]
PF8	Global PMD Signal Detect function	54.5.4	Report state via PMD_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
PF9	Global PMD Signal Detect OK threshold	54.5.4	SIGNAL_DETECT = OK for signal value ≥ 175 mV for at least 1 UI on each of the four lanes	M	Yes [ ]
PF10	Global PMD Signal Detect FAIL threshold, minimum	54.5.4	SIGNAL_DETECT = FAIL not asserted for signal level < 50 mV for < 250 µs on all four lanes	M	Yes [ ]
PF11	Global PMD Signal Detect FAIL threshold, maximum	54.5.4	SIGNAL_DETECT = FAIL asserted for signal level < 50 mV for > 500 µs on any of the four lanes	M	Yes [ ]
PF12	Global_PMD_transmit_disable	54.5.6	Disables all transmitters by forcing a constant output state	O	Yes [ ] No [ ]
PF13	PMD_fault disables transmitter	54.5.6	Disables all transmitters by forcing a constant output state when a fault is detected	O	Yes [ ] No [ ]
PF14	Effect on loopback of Global_PMD_transmit_disable	54.5.6	Global_PMD_transmit_disable does not affect loopback function	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PF15	PMD_transmit_disable_n	54.5.7	Disables transmitter n (n=0:3) by forcing a constant output state	O	Yes [ ]
PF16	PMD_fault disables transmitter n	54.5.7	Disables transmitter n (n=0:3) by forcing a constant output state when a fault is detected	O	Yes [ ] No [ ]
PF17	Effect on loopback of PMD_transmit_disable_n	54.5.7	PMD_transmit_disable_n does not affect loopback function	M	Yes [ ]
PF18	Loop Back	54.5.8	Loopback function provided	M	Yes [ ]
PF19	Transmitters on during loopback	54.5.8	Loopback function does not disable the transmitters	M	Yes [ ]

54.10.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Lane-by-Lane Signal Detect function	54.5.5	Sets PMD_signal_detect_n values on a lane-by-lane basis per requirements of 54.5.4	MD:M	Yes [ ] N/A [ ]
MF2	PMD_fault function	54.5.9	Sets PMD_fault to a logical 1 if any local fault is detected otherwise set to 0	MD:M	Yes [ ] N/A [ ]
MF3	PMD_transmit_fault function	54.5.10	Sets PMD_transmit_fault to a logical 1 if a local fault is detected on the transmit path otherwise set to 0	MD:M	Yes [ ] N/A [ ]
MF4	PMD_receive_fault function	54.5.11	Sets PMD_receive_fault to a logical 1 if a local fault is detected on the receive path otherwise set to 0	MD:M	Yes [ ] N/A [ ]

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54.10.4.3 Transmitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
DS1	Meets specifications at TP2	54.6.3		M	Yes [ ]
DS2	Test load	54.6.3.2	100 Ω differential load with return loss > 20 dB	M	Yes [ ]
DS3	Signaling speed	54.6.3.3	3.125 GBd ± 100 ppm	M	Yes [ ]
DS4	Maximum transmitter differential peak-to-peak output amplitude	54.6.3.4	Less than 1200 mV	M	Yes [ ]
DS5	Minimum transmitter differential peak-to-peak output amplitude	54.6.3.4	Greater than 800 mV	M	Yes [ ]
DS6	Maximum transmitter differential peak-to-peak amplitude difference	54.6.3.4	Less than 150 mV	M	Yes [ ]
DS7	Common-mode output voltage	54.6.3.4	Between –0.4 V and +1.9 V	M	Yes [ ]
DS8	Transmitter output return loss	54.6.3.5	Per Equation (54–1) and Equation (54–2)	M	Yes [ ]
DS9	Transmitter output return loss reference impedance	54.6.3.5	100 Ω	M	Yes [ ]
DS10	Transmitter output template test pattern	54.6.3.6	Per 48A.2	M	Yes [ ]
DS11	Transmitter output template compliance	54.6.3.6	Met while connected to test fixture shown in Figure 54–3, with all outputs active	M	Yes [ ]
DS12	Transmitter output normalization	54.6.3.6	Per process defined in 54.6.3.6	M	Yes [ ]
DS13	Transmitter output template	54.6.3.6	Lies within template of Figure 54–6 and Table 54–4	M	Yes [ ]
DS14	Rising edge transition time	54.6.3.7	Between 60 ps and 130 ps as measured per 54.6.3.7	M	Yes [ ]
DS15	Falling edge transition time	54.6.3.7	Between 60 ps and 130 ps as measured per 54.6.3.7	M	Yes [ ]
DS16	Jitter requirements	54.6.3.8	Meet BER bathtub curve, See Annex 48B	M	Yes [ ]
DS17	Transmit jitter, peak-to-peak	54.6.3.8	Meet BER bathtub curve, See Annex 48B, with Total jitter < 0.35 UI Deterministic jitter < 0.17 UI Random jitter < 0.27 UI	M	Yes [ ]
DS18	Jitter test patterns	54.6.3.9	As per Annex 48A.5	M	Yes [ ]

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54.10.4.4 Receiver specifications

Item	Feature	Subclause	Value/Comment	Status	Support
RS1	Bit Error Ratio	54.6.4.1	BER of better than 10^{-12}	M	Yes [ ]
RS2	Signaling speed	54.6.4.2	3.125 GBd ± 100 ppm	M	Yes [ ]
RS3	AC-coupling	54.6.4.3	—	M	Yes [ ]
RS4	Input peak-to-peak amplitude tolerance	54.6.4.4	Accepts signals compliant with 54.6.3, may be larger than 1200 mV	M	Yes [ ]
RS5	Receiver input return loss	54.6.4.5	Per Equation (54–1) and Equation (54–2)	M	Yes [ ]

54.10.4.5 Cable assembly specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CA1	Differential reference impedance	54.7.1	100 Ω	CBL:M	Yes [ ] N/A [ ]
CA2	Insertion loss	54.7.2	Per Equation (54–3)	CBL:M	Yes [ ] N/A [ ]
CA3	Return loss	54.7.2	Per Equation (54–4), Equation (54–5), and Equation (54–6)	CBL:M	Yes [ ] N/A [ ]
CA4	NEXT	54.7.4.1	Per Equation (54–6)	CBL:M	Yes [ ] N/A [ ]
CA5	MDNEXT	54.7.4.2	Per Equation (54–7)	CBL:M	Yes [ ] N/A [ ]
CA6	ELFEXT	54.7.5.1	Per Equation (54–9)	CBL:M	Yes [ ] N/A [ ]
CA7	MDELFEXT	54.7.5.2	Per Equation (54–10)	CBL:M	Yes [ ] N/A [ ]
CA8	Shielding	54.7.6	Class 2 or better in accordance with IEC 61196-1	CBL:M	Yes [ ] N/A [ ]
CA9	Crossover function	54.7.7	Per Figure 54–11	CBL:M	Yes [ ] N/A [ ]
CA10	Cable assembly connector type	54.8.1	SFF-8470 latch-type plug	CBL:M	Yes [ ] N/A [ ]
CA11	Pin assignments	54.8.2	Per Table 54–7	CBL:M	Yes [ ] N/A [ ]

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54.10.4.6 MDI connector specifications

Item	Feature	Subclause	Value/Comment	Status	Support
MDC1	MDI connector type	54.8.1	SFF-8470 latch-type receptacle	M	Yes [ ]

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55. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10GBASE-T

55.1 Overview

The 10GBASE-T PHY is one of the 10 Gigabit Ethernet family of high-speed network specifications. The 10GBASE-T Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and baseband medium specifications are intended for users who want 10 Gb/s performance over balanced twisted-pair structured cabling systems. 10GBASE-T signaling requires four pairs of balanced cabling, as specified in ISO/IEC 11801:2002 with appropriate augmentation as specified in 55.7. It is recommended that the guidelines in TIA TSB-155-A, ISO/IEC TR 24750, ANSI/TIA-568-C.2, and ISO/IEC 11801:2002/ Amendment 1 be considered before the installation of 10GBASE-T equipment for any cabling system.

This clause defines the type 10GBASE-T PCS, type 10GBASE-T PMA sublayer, and type 10GBASE-T Medium Dependent Interface (MDI). Together, the PCS and the PMA sublayer define a 10GBASE-T Physical Layer device (PHY). Functional, electrical, and mechanical specifications for the type 10GBASE-T PCS, PMA, and MDI are provided in this document. This clause also specifies the baseband medium used with 10GBASE-T. Management is specified in Clause 30.

This clause also specifies 10GBASE-T Low Power Idle (LPI) as part of Energy-Efficient Ethernet (EEE). This allows the PHY to enter a low power mode of operation during periods of low link utilization as described in Clause 78. 10GBASE-T PHYs may optionally support a fast retrain mechanism.

55.1.1 Objectives

The objectives of 10GBASE-T are as follows:

a) Support full duplex operation only
b) Support star-wired local area networks using point-to-point links and structured cabling topologies
c) Support a speed of 10 Gb/s at the MAC/PLS service interface
d) Support copper medium from ISO/IEC 11801:2002, with appropriate augmentation as specified in 55.7
e) Support operation over 4-connector structured 4-pair, twisted copper cabling for all supported distances and Classes
f) Define a single 10 Gb/s PHY that would support links of up to 100 m on 4-pair balanced copper cabling as specified in 55.7
g) Preserve the IEEE 802.3/Ethernet frame format at the MAC client service interface
h) Preserve minimum and maximum frame size of the current IEEE 802.3 standard
i) Support Auto-Negotiation (Clause 28)
j) Meet CISPR/FCC Class A EMC requirements
k) Support a BER of less than or equal to 10^{-12} on all supported distances and Classes
l) Support a EEE capability as part of Energy-Efficient Ethernet (Clause 78)

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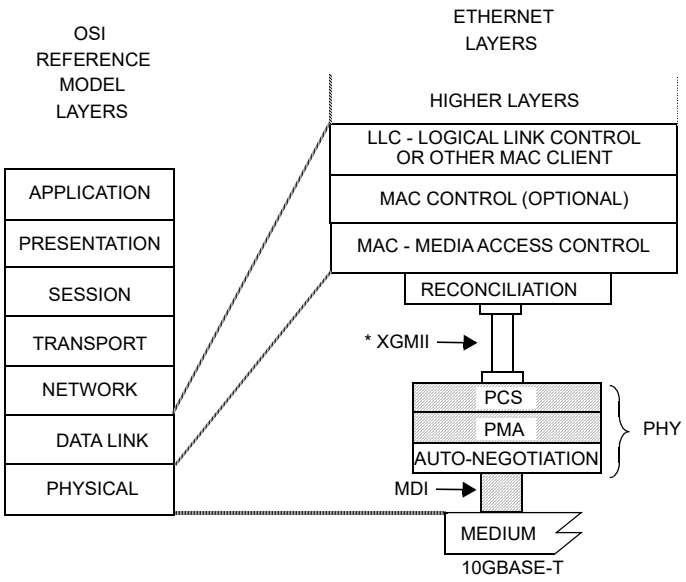
55.1.2 Relationship of 10GBASE-T to other standards

Relations between the 10GBASE-T PHY, the ISO Open Systems Interconnection (OSI) reference model, and the IEEE 802.3 Ethernet model are shown in Figure 55–1. The PHY sublayers (shown shaded) in Figure 55–1 connect the IEEE 802.3 MAC to the medium.



MDI = MEDIUM DEPENDENT INTERFACE
XGMII = TEN GIGABIT MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE

*XGMII is optional.

Figure 55–1—Type 10GBASE-T PHY relationship to the ISO Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

55.1.3 Operation of 10GBASE-T

The 10GBASE-T PHY employs full duplex baseband transmission over four pairs of balanced cabling. The aggregate data rate of 10 Gb/s is achieved by transmitting 2500 Mb/s in each direction simultaneously on each wire pair, as shown in Figure 55–2. Baseband 16-level PAM signaling with a modulation rate of 800 Megasymbol per second is used on each of the wire pairs. Ethernet data and control characters are encoded at a rate of 3.125 information bits per PAM16 symbol, along with auxiliary channel bits. Two consecutively transmitted PAM16 symbols are considered as one two-dimensional (2D) symbol. The 2D symbols are selected from a constrained constellation of 128 maximally spaced 2D symbols, called DSQ128[105] (double square 128). After link startup, PHY frames consisting of 512 DSQ128 symbols are continuously transmitted. The DSQ128 symbols are determined by 7-bit labels, each comprising 3 uncoded bits and 4 LDPC-encoded bits. The 512 DSQ128 symbols of one PHY frame are transmitted as 4 × 256 PAM16 symbols over the four wire pairs. Data and Control symbols are embedded in a framing scheme that runs continuously after startup of the link. The modulation symbol rate of 800 Msymbols/s results in a symbol period of 1.25 ns.

[105]The DSQ128 symbols are obtained by concatenating two time-adjacent 1D PAM16 symbols and retaining among the 256 possible Cartesian product combinations, 128 maximally spaced 2D symbols. The resulting checkerboard constellation is based on a lattice called RZ^2 in the literature (see Forney [B25]). DSQ constellations have previously been introduced under the name “AMPM” (see [B26] for examples of 8 point and 32 point AMPM/DSQ constellations).

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A 10GBASE-T PHY can be configured either as a MASTER PHY or as a SLAVE PHY. The MASTER-SLAVE relationship between two stations sharing a link segment is established during Auto-Negotiation (see Clause 28, 55.6, Annex 28B, Annex 28C, and Annex 28D). The MASTER PHY uses a local clock to determine the timing of transmitter operations. The MASTER-SLAVE relationship may include loop timing. If loop timing is implemented, the SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in Figure 55–3. If loop timing is not implemented, the SLAVE PHY transmit clocking is identical to the MASTER PHY transmit clocking.

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

10GBASE-T PHYs optionally provide support for LPI as part of EEE (see Clause 78). This extension allows PHYs to enter an LPI mode when either the local or link partner system requests low power operation. The transmit and receive functions may enter and leave the LPI mode independently so that both symmetric and asymmetric operation is supported. While the PHY is in the LPI mode, the PHY periodically transmits a refresh signal to allow the remote PHY to refresh its receiver state (e.g., timing recovery, adaptive filter coefficients) and thereby track long-term variation in the timing of the link or the underlying channel characteristics. An easily detectable alert signal is transmitted to signal an end to the LPI mode. The alert signal is followed by a wake signal to enable a rapid transition back to the normal operational mode.

10GBASE-T PHYs may optionally support a fast retrain mechanism. This function allows PHYs to quickly recover from link degradation without a normal two second retrain.

The PCS and PMA subclauses of this document are summarized in 55.1.3.1 and 55.1.3.2. The EEE capability is summarized in 55.1.3.3. Figure 55–3 shows the functional block diagram.

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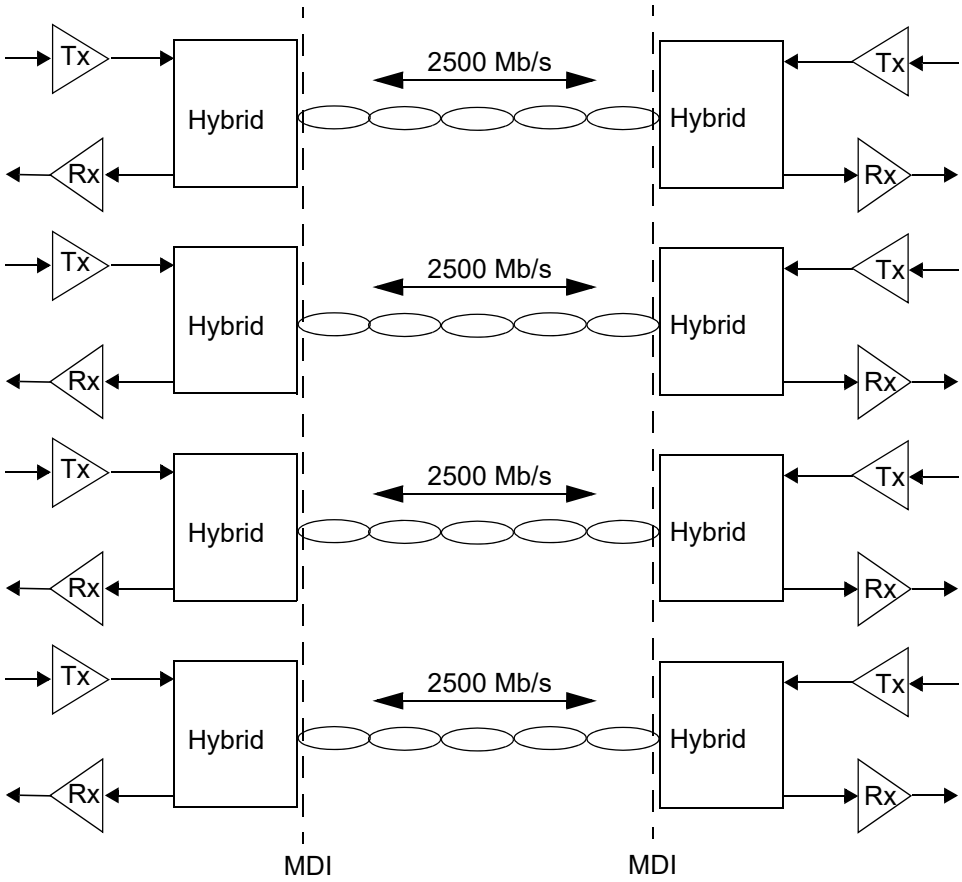

Figure 55–2—10GBASE-T topology

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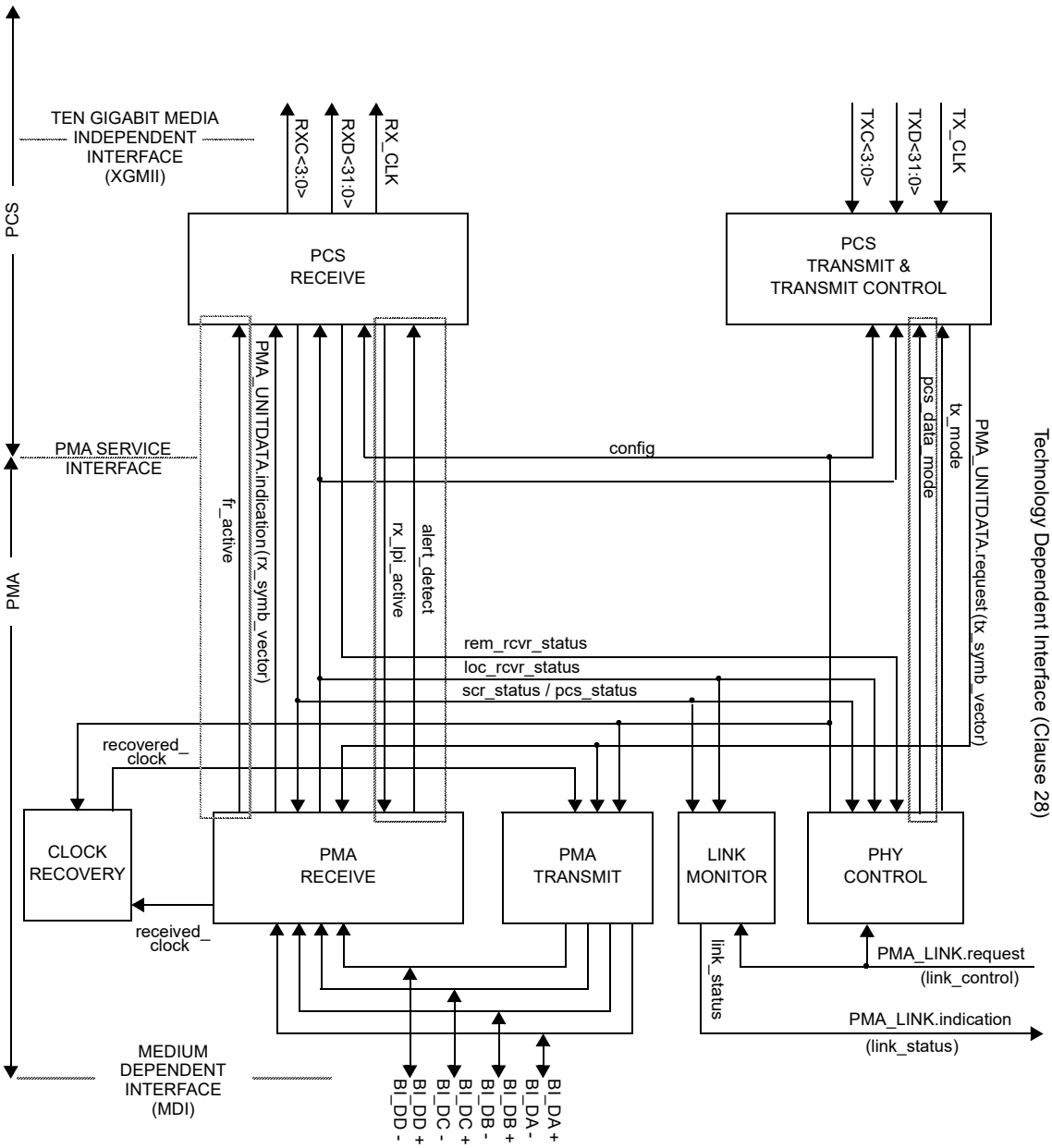

NOTE 1—The recovered_clock arc is shown to indicate delivery of the received clock signal back to PMA TRANSMIT for loop timing.

NOTE 2—pcs_data_mode is required only for the EEE or fast retrain capabilities; alert_detect and rx_lpi_active are only required for the EEE capability; fr_active is only required for the fast retrain capability.

Figure 55–3—Functional block diagram

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55.1.3.1 Physical Coding Sublayer (PCS)

The 10GBASE-T PCS couples a Ten Gigabit Media Independent Interface (XGMII), as described in Clause 46, to the 10GBASE-T Physical Medium Attachment (PMA) sublayer.

In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in normal mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. The resulting 65-bit blocks are scrambled and assembled in a group of 50 blocks. Adding CRC8 check bits yields a CRC-checked Ethernet payload of $50 \times 65 + 8 = 3258$ bits. An auxiliary channel bit is added to obtain a block of 3259 bits.

The 3259 bits are divided into 3×512 bits and 1723 bits. The 3×512 bits, among them the auxiliary channel bit, remain uncoded. The 1723 bits are encoded by a systematic LDPC(1723,2048) encoder, which adds 325 LDPC check bits to form an LDPC codeword of 2048 coded bits. The 3×512 uncoded bits and the $2048 = 4 \times 512$ coded bits are arranged in a frame of 512 7-bit labels. Each 7-bit label comprises 3 uncoded bits and 4 coded bits.

The 512 7-bit labels are mapped into 512 2D modulation symbols selected from a DSQ128 constellation. The DSQ128 symbols are obtained by concatenating two time-adjacent 1D PAM16 symbols and retaining among the 256 possible Cartesian product combinations, 128 maximally spaced 2D symbols. The resulting checkerboard constellation is based on a lattice called RZ^2 in the literature (see Forney [B25]).

The DSQ128 constellation is partitioned into eight subsets, each subset containing 16 maximally spaced 2D symbols. The three uncoded bits of each 7-bit label select one DSQ128 subset, and the four LDPC-coded bits of the label select one 2D symbol in this subset.

The obtained PHY frame of 512 DSQ128 symbols is passed on to the PMA as PMA_UNITDATA.request. The PMA transmits the DSQ128 symbols over the four wire pairs in the form of 256 constituent PAM16 symbols per pair. Details of the PCS function are covered in 55.3.

In the receive direction, in normal mode, the PCS processes code-groups received from the remote PHY via the PMA in 256 4D symbol blocks and maps them to the XGMII service interface in the receive path. In this receive processing scheme, symbol clock synchronization is done by the PMA Receive function.

The PCS functions and state diagrams are specified in 55.3. The signals provided by the PCS at the XGMII conform to the interface requirements of Clause 46. The interface to the PMA is an abstract message-passing interface specified in 55.2.

55.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto the balanced cabling physical medium via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions. The PMA provides full duplex communications at 800 Msymbols/s over four pairs of balanced cabling up to 100 m in length.

The PMA Transmit function comprises four transmitters to generate continuous time analog signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD, as described in 55.4.3.1. In normal mode, each four-dimensional (4D) symbol received from the PCS Transmit function undergoes multiple stages of processing. First the symbol goes through a Tomlinson-Harashima precoder (THP), which maps the PAM16 input (as described in 55.3.2.2.19) in each dimension of the four-dimensional symbol into a quasi-continuous discrete

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time value in the range $-16 \le x < 16$. This THP-processed four-dimensional symbol stream may be further processed by a digital transmit filter and is then passed on to four digital to analog converters (DACs). The DAC outputs may be further processed with continuous time filters to roll off the high-frequency spectral response to limit high-frequency emissions and are then applied to each of the four balanced pairs via the MDI port.

The PMA Receive function comprises four independent receivers for pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD, as described in 55.4.3.2. The receivers are responsible for acquiring symbol timing and, when operating in normal mode, for cancelling echo, near-end crosstalk, far-end crosstalk, and equalizing the signal. The 4D symbols are provided to the PCS Receive function via the PMA_UNITDATA.indication message. The PMA also contains functions for Link Monitor.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control begins following the completion of Auto-Negotiation and provides the startup functions required for successful 10GBASE-T operation. It determines whether the PHY operates in a normal mode, enabling data transmission over the link segment, or whether the PHY sends special PAM2 code-groups that are used in the training mode. The latter occurs when either one or both of the PHYs that share a link segment are not operating reliably.

PMA functions and state diagrams are specified in 55.4. PMA electrical specifications are given in 55.5.

The PMA sublayer may also support a fast retrain function. The fast retrain function is specified in 55.4.2.5.15.

55.1.3.3 EEE capability

A 10GBASE-T PHY may optionally support the EEE capability, as described in 78.3. The EEE capability is a mechanism by which 10GBASE-T PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter this mode of operation after reaching PCS data mode. Each direction of the full duplex link is able to enter and exit the LPI mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full duplex link is in a period of low utilization. No data frames are lost or corrupted during the transition to or from the LPI mode.

In the transmit direction the transition to the LPI transmit mode begins when the PCS transmit function detects an LPI control character in all four lanes of two consecutive transfers of TXD[31:0] that will be mapped into a single 64B/65B block. Following this event a sleep signal is transmitted by the PMA. The sleep signal is composed of LDPC frames that contain only LP_IDLE 64B/65B blocks. The sleep signal indicates to the link partner that the transmit function of the PHY is entering the LPI transmit mode. Immediately after the transmission of the sleep frames, the transmit function of the local PHY enters the LPI transmit mode. While the transmit function is in the LPI mode the PHY may disable data path and control logic to save additional power. Periodically the transmit function of the local PHY transmits refresh frames that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity. The LPI mode begins with quiet signaling or with a full refresh period. Partial refreshes (defined as a refresh signal shorter than 4 LDPC frames) that immediately follow the transition to the LPI mode are replaced with quiet signaling. The quiet-refresh cycle continues until the PCS function detects IDLE characters on the XGMII. These characters signal to the PHY that the LPI transmit mode should end. The PMA Transmit function in the PHY then sends an alert message to the link partner. The alert signal begins on a LDPC frame boundary, but has no fixed relationship to the quiet-refresh cycle. The alert signal wakes the link partner from sleep. The alert signal is followed by a wake signal, composed of LDPC frames containing only IDLE 64B/65B blocks. After a short recovery time the normal operational mode is resumed.

In the receive direction the transition to the LPI mode is triggered when the PCS Receive function detects LPI control characters within received LDPC frames. This indicates that the link partner is about to enter the LPI transmit mode. Following these frames the link partner ceases transmission and begins quiet-refresh

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signaling. During the quiet time it is highly recommended that the local receiver power off circuits to reduce power consumption. Periodically the link partner transmits refresh frames that are used by the receiver to update adaptive coefficients and timing circuits. This quiet-refresh cycle continues until the link partner transmits the alert signal, initiating a transition back to the normal operational mode. The alert signal is detected in the PMA and signals that normal data frames will follow. The alert signal is followed by a wake signal that allows the local receiver time to prepare for the normal operational mode. The wake signal is composed of repeated IDLE 64B/65B blocks. After a short recovery time the normal operational mode is resumed.

Support for the EEE capability is advertised during Auto-Negotiation. Transitions to and from the LPI transmit mode are controlled via XGMII signaling. Transitions to and from the LPI receive mode are controlled by the link partner using sleep, alert, and wake signaling.

The PCS 64B/65B Transmit state diagram in Figure 55–16 and Figure 55–17 includes additional states for EEE. The PCS 64B/65B Receive state diagram in Figure 55–18 and Figure 55–19 includes additional states for EEE. The EEE Transmit state diagram is contained in the PCS Transmit function and is specified in Figure 55–20.

55.1.4 Signaling

10GBASE-T signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over each wire pair. The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to four-dimensional symbols in the transmit path.
c) Algorithmic mapping from the received four-dimensional signals on the MDI port to RXD<31:0> and RXC<3:0> on the XGMII interface.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions on any pair combination.
f) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
g) Block framing and other control signals.
h) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
i) Ability to automatically detect and correct for pair swapping and crossover connections.
j) Ability to automatically detect and correct for incorrect polarity in the connections.
k) Ability to automatically correct for differential delay variations across the wire-pairs.
l) Ability to support refresh, quiet and alert signaling during LPI operation.

The PHY operates in two modes—normal mode or training mode. In normal mode, PCS generates a continuous stream of four-dimensional symbols that are transmitted via the PMA at one of eight power levels. In training mode, the PCS is directed to generate only PAM2 symbols for transmission by the PMA, which enable the receiver at the other end to train until it is ready to operate in normal mode. (See the PCS reference diagram in 55.2.)

PHYs may also support the EEE capability as described in 55.1.3.3. Transitions to the LPI mode are supported after reaching normal mode.

55.1.5 Interfaces

All 10GBASE-T PHY implementations are compatible at the MDI and at a physically exposed XGMII, if made available. Physical implementation of the XGMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII

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(if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not.

55.1.6 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

Default initializations, unless specifically specified, are left to the implementer.

55.2 10GBASE-T service primitives and interfaces

10GBASE-T transfers data and control information across the following four service interfaces:

a) Ten Gigabit Media Independent Interface (XGMII)
b) Technology Dependent Interface
c) PMA service interface
d) Medium dependent interface (MDI)

The XGMII is specified in Clause 46; the Technology Dependent Interface is specified in Clause 28. The PMA service interface is defined in 55.2.2 and the MDI is defined in 55.8.

55.2.1 Technology Dependent Interface

10GBASE-T uses the following service primitives to exchange status indications and control signals across the Technology Dependent Interface as specified in Clause 28:

PMA_LINK.request (link_control)

PMA_LINK.indication (link_status)

55.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation algorithm to enable and disable operation of the PMA as specified in 28.2.6.2.

55.2.1.1.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PMA reports link_status=FAIL. PHY processes are disabled.
DISABLE	Set by the Auto-Negotiation algorithm in the event fast link pulses are detected. PHY processes are disabled. This allows the Auto-Negotiation algorithm to determine how to configure the link.

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ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions.

55.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in Clause 28.

55.2.1.1.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as defined in 55.4.2.6.

55.2.1.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 28.2.6.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation algorithm about the status of the underlying link.

55.2.1.2.1 Semantics of the primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK.

FAIL	No valid link established.
READY	For 10GBASE-T link_status does not take the value READY.
OK	The Link Monitor function indicates that a valid 10GBASE-T link is established. Reliable reception of signals transmitted from the remote PHY is possible.

55.2.1.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 55–31.

55.2.1.2.3 Effect of receipt

Auto-Negotiation uses this primitive to detect a change in link_status as described in Clause 28.

55.2.2 PMA service interface

10GBASE-T uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication (tx_mode)

PMA_CONFIG.indication (config)

PMA_UNITDATA.request (tx_symb_vector)

PMA_UNITDATA.indication (rx_symb_vector)

PMA_SCRSTATUS.request (scr_status)

PMA_PCSSTATUS.request (pcs_status)

PMA_RXSTATUS.indication (loc_rcvr_status)

PMA_REMRXSTATUS.request (rem_rcvr_status)

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EEE-capable PHYs additionally support the following service primitives:

PMA_ALERTDETECT.indication (alert_detect)

PCS_RX_LPI_STATUS.request (rx_lpi_active)

PMA_PCSDATAMODE.indication (pcs_data_mode)

Fast retrain capable PHYs additionally support the following service primitive:

PMA_FR_ACTIVE.indication (fr_active)

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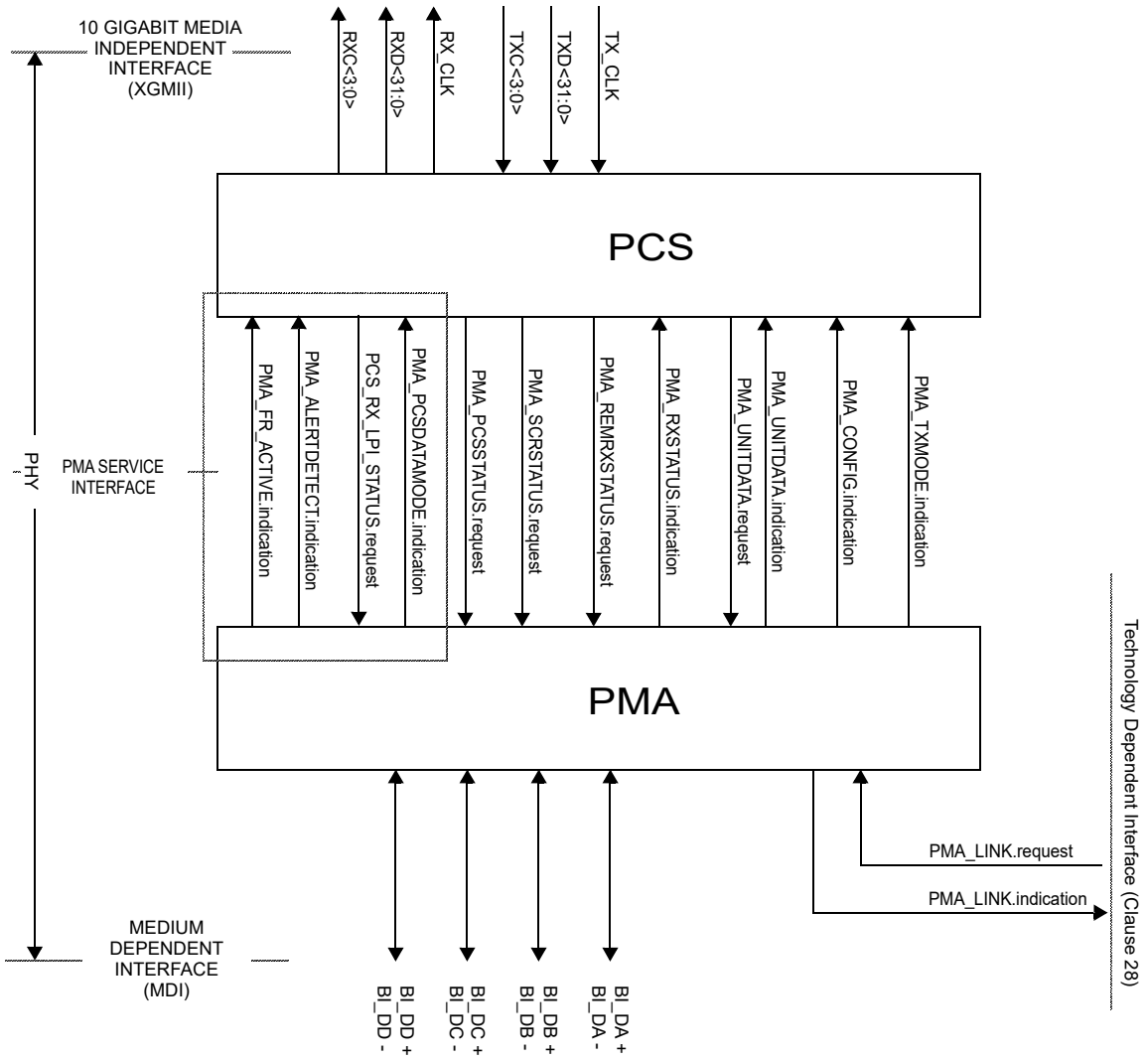
The use of these primitives is illustrated in Figure 55–4. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 55–4.



NOTE—
PMA_PCSDATAMODE.indication is required only for the EEE or fast retrain capabilities.
PMA_ALERTDETECT.indication and PCS_RX_LPI_STATUS.request are only required for the EEE capability.
PMA_FR_ACTIVE.indication is only required for the fast retrain capability.

Figure 55–4—10GBASE-T service interfaces

55.2.2.1 PMA_TXMODE.indication

The transmitter in a 10GBASE-T link normally sends over the four pairs, four-dimensional symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

55.2.2.1.1 Semantics of the primitive

PMA_TXMODE.indication (tx_mode)

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PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of code-groups the PCS should be transmitting. The parameter tx_mode can take on one of the following three values of the form:

SEND_N	This value is continuously asserted when transmission of sequences of four-dimensional symbols representing an XGMII data stream in normal mode.
SEND_T	This value is continuously asserted in case transmission of sequences of code-groups representing the training mode is to take place.
SEND_Z	This value is continuously asserted in case transmission of zeros is required.

55.2.2.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

55.2.2.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 55.3.2.2.

55.2.2.2 PMA_CONFIG.indication

Each PHY in a 10GBASE-T link is capable of operating as a MASTER PHY and as a SLAVE PHY. MASTER-SLAVE configuration is determined during Auto-Negotiation (55.6.1). The result of this negotiation is provided to the PMA.

55.2.2.2.1 Semantics of the primitive

PMA_CONFIG.indication (config)

PMA_CONFIG.indication specifies to PCS and PMA Transmit via the parameter config whether the PHY operates as a MASTER PHY or as a SLAVE PHY. The parameter config can take on one of the following two values of the form:

MASTER	This value is continuously asserted when the PHY operates as a MASTER PHY.
SLAVE	This value is continuously asserted when the PHY operates as a SLAVE PHY.

55.2.2.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in config.

55.2.2.2.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter config.

55.2.2.3 PMA_UNITDATA.request

This primitive defines the transfer of code-groups in the form of the tx_symb_vector parameter from the PCS to the PMA. The code-groups are obtained in the PCS Transmit function using the encoding rules defined in 55.3.2.2 to represent XGMII data and control streams or other sequences.

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55.2.2.3.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. For EEE-capable PHYs, the vector also requests the PMA to send the ALERT signal during LPI. The tx_symb_vector parameter takes on the form:

SYMB_4D	A vector of four multi-level symbols, one for each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. In normal operation, each symbol may take on one of the values in the set {–15, –13, –11, –9, –7, –5, –3, –1, 1, 3, 5, 7, 9, 11, 13, 15}. The symbols may additionally take the value 0 when zeros are to be transmitted in the following two cases: 1) when PMA_TXMODE.indication is SEND_Z during PMA training, and 2) after data mode is reached, the transmit function is in the LPI transmit mode and lpi_tx_mode is QUIET
ALERT	A vector used to indicate that the PMA should transmit the alert sequence. ALERT will be asserted for a time equal to 4 LDPC frames.

The symbols that are elements of tx_symb_vector are called, according to the pair on which each is transmitted, tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD].

55.2.2.3.2 When generated

The PCS generates PMA_UNITDATA.request synchronously with every transmit clock cycle.

55.2.2.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols after processing with the THP, the transmit filter and other specified PMA Transmit processing. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD for cancelling the echo and near-end crosstalk (NEXT).

55.2.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of code-groups in the form of the rx_symb_vector parameter from the PMA to the PCS.

55.2.2.4.1 Semantics of the primitive

PMA_UNITDATA.indication (rx_symb_vector)

During reception the PMA_UNITDATA.indication simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on each of the four receive pairs BI_DA, BI_DB, BI_DC, and BI_DD. The rx_symb_vector parameter takes on the form:

SYMB_4D	A vector of the four 1D symbols that is the receiver's best estimate of the symbols that were sent by the remote transmitter across the four pairs with reliability measures.

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55.2.2.4.2 When generated

The PMA generates PMA_UNITDATA.indication (SYMB_4D) messages synchronously every four symbols received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is 800 MHz, as governed by the recovered clock.

55.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

55.2.2.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the training mode descrambler has achieved synchronization.

55.2.2.5.1 Semantics of the primitive

PMA_SCRSTATUS.request (scr_status)

The scr_status parameter can take on one of two values of the form:

OK	The training mode descrambler has achieved synchronization.
NOT_OK	The training mode descrambler is not synchronized.

55.2.2.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

55.2.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 55.4.2.4, 55.4.2.5, and 55.4.6.1.

55.2.2.6 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in data mode.

55.2.2.6.1 Semantics of the primitive

PMA_PCSSTATUS.request (pcs_status)

The pcs_status parameter can take on one of two values of the form:

OK	The PCS is operating reliably in data mode.
NOT_OK	The PCS is not operating reliably in data mode.

55.2.2.6.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

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55.2.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 55.4.6.

55.2.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol streams.

55.2.2.7.1 Semantics of the primitive

PMA_RXSTATUS.indication (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

55.2.2.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

55.2.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 55–28 and in subclauses 55.2 and 55.4.6.3.

55.2.2.8 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The criterion for setting the parameter rem_rcvr_status is left to the implementer. It can be based, for example, on asserting rem_rcvr_status is NOT_OK until loc_rcvr_status is OK and then asserting the detected value of rem_rcvr_status after proper PCS Receive decoding is achieved.

55.2.2.8.1 Semantics of the primitive

PMA_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

55.2.2.8.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages to indicate a change in rem_rcvr_status on the basis of signals received at the MDI.

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55.2.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 55–28.

55.2.2.9 PMA_ALERTDETECT.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY when rx_lpi_active is TRUE. The parameter alert_detect conveys to the PCS receive function information regarding the detection of the LPI alert signal by the PMA receive function. The criterion for setting the parameter alert_detect is left to the implementer.

55.2.2.9.1 Semantics of the primitive

PMA_ALERTDETECT.indication (alert_detect)

The alert_detect parameter can take on one of two values of the form:

TRUE	The alert signal has been reliably detected at the local receiver.
FALSE	The alert signal at the local receiver has not been detected.

55.2.2.9.2 When generated

The PMA generates PMA_ALERTDETECT.indication messages to indicate a change in the alert_detect status.

55.2.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in 55.3.2.3, Figure 55–18, and Figure 55–19.

55.2.2.10 PCS_RX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS receive function to indicate the status of the receive link at the local PHY. The parameter PCS_RX_LPI_STATUS.request conveys to the PCS transmit and PMA receive functions information regarding whether the receive function is in the LPI receive mode. The parameter is generated by the Receive 64B/65B state diagram in Figure 55–18.

55.2.2.10.1 Semantics of the primitive

PCS_RX_LPI_STATUS.request (rx_lpi_active)

The rx_lpi_active parameter can take on one of two values of the form:

TRUE	The receive function is in the LPI receive mode.
FALSE	The receive function is not in the LPI receive mode.

55.2.2.10.2 When generated

The PCS generates PCS_RX_LPI_STATUS.request messages to indicate a change in the rx_lpi_active variable as determined by the receive state diagram in Figure 55–18.

55.2.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in 55.3.2.3 and Figure 55–32.

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55.2.2.11 PMA_PCSDATAMODE.indication

This primitive indicates whether or not the PCS state diagrams are able to transition from their initialization states. The pcs_data_mode variable is generated by the PMA PHY Control function. It is passed to the PCS Control function via the PMA_PCSDATAMODE.indication primitive.

55.2.2.11.1 Semantics of the primitive

PMA_PCSDATAMODE.indication (pcs_data_mode)

55.2.2.11.2 When generated

The PMA PHY Control function generates PMA_PCSDATAMODE.indication messages continuously.

55.2.2.11.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 55.3.2.2.

55.2.2.12 PMA_FR_ACTIVE.indication

This primitive indicates whether or not the PMA is currently performing a fast retrain. The fr_active variable is generated by the PMA PHY Control function. It is passed to the PCS Receive Control function via the PMA_FR_ACTIVE.indication primitive. This primitive is only supported by PHYs with the fast retrain capability.

55.2.2.12.1 Semantics of the primitive

PMA_FR_ACTIVE.indication (fr_active)

55.2.2.12.2 When generated

The PMA PHY Control function generates PMA_FR_ACTIVE.indication messages continuously.

55.2.2.12.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 55–18.

55.3 Physical Coding Sublayer (PCS)

55.3.1 PCS service interface (XGMII)

The PCS service interface allows the 10GBASE-T PCS to transfer information to and from a PCS client. The PCS Interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

55.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

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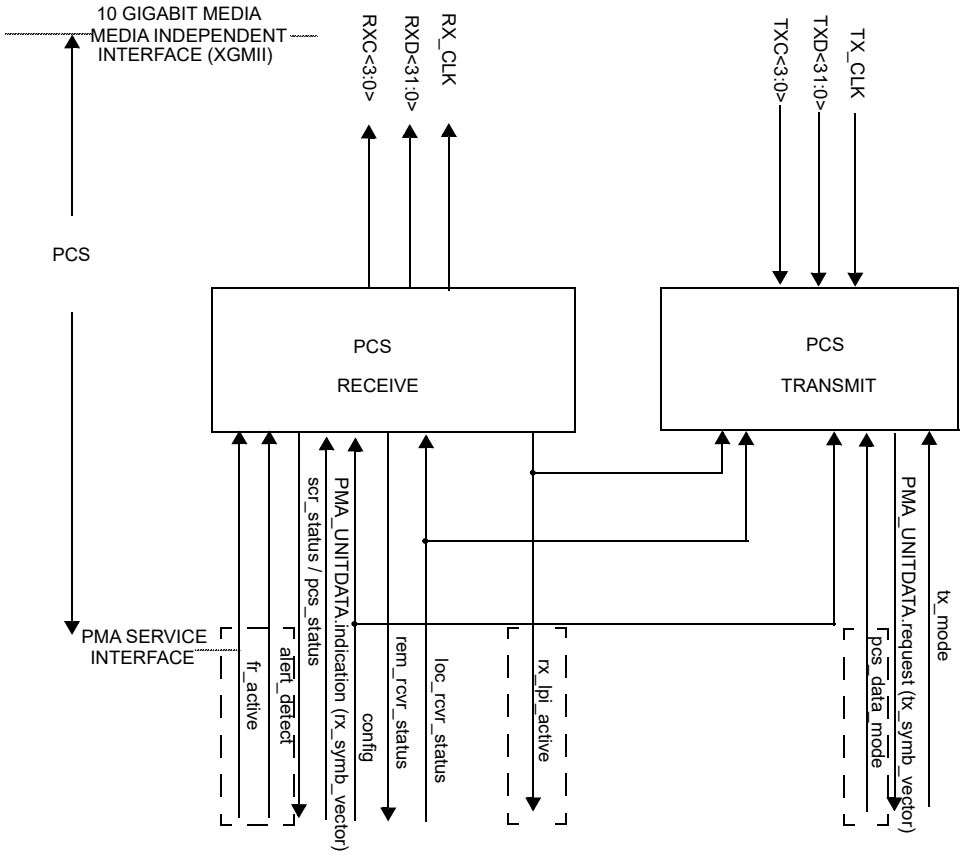
The PCS reference diagram, Figure 55–5, shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 55–5.



NOTE—
pcs_data_mode is required only for the EEE or fast retrain capabilities.
alert_detect and rx_lpi_active are only required for the EEE capability.
fr_active is only required for the fast retrain capability.

Figure 55–5—PCS reference diagram

55.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 55.3.6.2.2).
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset = true while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

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55.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 55–16 and the PCS Transmit bit ordering in Figure 55–6 and Figure 55–8.

Dashed rectangles in Figure 55–16 and Figure 55–17 are used to indicate states and state transitions in the transmit process state diagram that shall be supported by PHYs with the EEE capability. PHYs without the EEE capability do not support these transitions.

When communicating with the XGMII, the PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment to 64B/65B is performed in the PCS. The PMA sublayer operates independently of block and packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

When the transmit channel is in normal mode, the PCS Transmit process continuously generates 65B blocks based upon the TXD <31:0> and TXC <3:0> signals on the XGMII. The subsequent functions of the PCS Transmit process then pack the resulting blocks, and split the bits into the uncoded set and the coded set, which is processed by a low density parity check (LDPC) encoder and then joint mapped into a transmit LDPC frame of DSQ128 symbols. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a code-group (A_n, B_n, C_n, D_n) that is transferred to the PMA via the PMA_UNITDATA.request primitive. The PMA transmits symbols A_n, B_n, C_n, D_n over wire-pairs BI_DA, BI_DB, BI_DC, and BI_DD respectively. The integer, n, is a time index that is introduced to establish a temporal relationship between different symbol periods. A symbol period, T, is 1.25 ns.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate sequences of code-groups (TA_n, TB_n, TC_n, TD_n) defined in 55.3.4.2 to the PMA via the PMA_UNITDATA.request primitive. These code-groups are used for training mode and only transmit the values {–9, 9} to keep the transmit power in the training mode the same as the transmit power in normal mode.

During training mode an InfoField is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes requests for remote transmitter settings. (See 55.4.2.5.)

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the normal mode of operation, and the PCS Transmit function shall use a 65B-LDPC coding technique to generate at each symbol period code-groups that represent data or control. During transmission, the 65B bits are scrambled by the PCS using a PCS scrambler, 8 CRC check bits and an auxiliary channel bit are added, then frames are encoded into a code-group of four-dimensional symbols and transferred to the PMA. During data encoding, PCS Transmit utilizes a LDPC frame encoder.

After reaching the normal mode of operation, EEE-capable PHYs may enter the LPI transmit mode under the control of the MAC via the XGMII. The EEE Transmit state diagram is contained within the PCS Transmit function. The EEE capability is described in 55.3.2.2.22.

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55.3.2.2.1 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an LDPC frame, and vice versa, using a 65B-LDPC coding scheme. The PAM2 PMA training frame synchronization allow establishment of LDPC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. During the LPI mode, LDPC frame boundaries delimit sleep, wake, refresh, quiet, and alert cycles. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 55.3.2.2.2.

55.3.2.2.2 65B-LDPC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters. The encoding defined by the transmission code ensure that sufficient information is present in the PHY bit stream to make clock recovery possible at the receiver. The encoding also preserves the likelihood of detecting any LDPC frame errors that may occur during transmission and reception of information. In addition, the code enables the receiver to achieve PCS synchronization alignment on the incoming PHY bit stream.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 55–6 for transmit and Figure 55–7 for receive. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 55.3.2.2.5 for information on how blocks containing control characters are mapped.

55.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. Control characters other than /O/, /S/ and /T/ are labeled C_0 to C_7. The control character for ordered set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7.

Two consecutive XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfers.

Contents of block type fields, data octets and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled TxB<64:0> and RxB<64:0> respectively where TxB<0> and RxB<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

55.3.2.2.4 Transmission order

The PCS Transmit bit ordering shall conform to Figure 55–6 and Figure 55–8. Note that these figures show the mapping from XGMII to 64B/65B block for a block containing eight data characters.

55.3.2.2.5 Block structure

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

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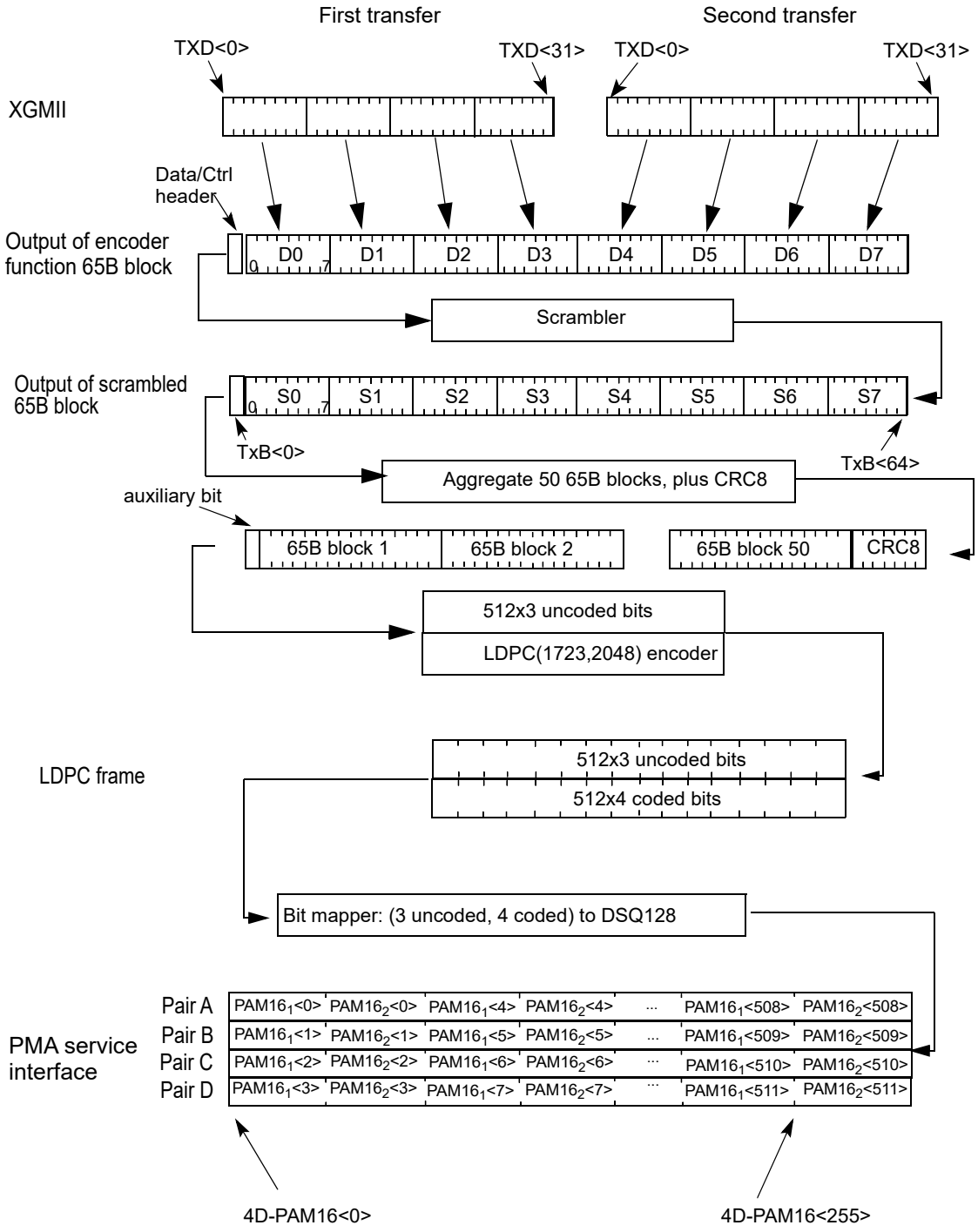

Figure 55–6—PCS Transmit bit ordering

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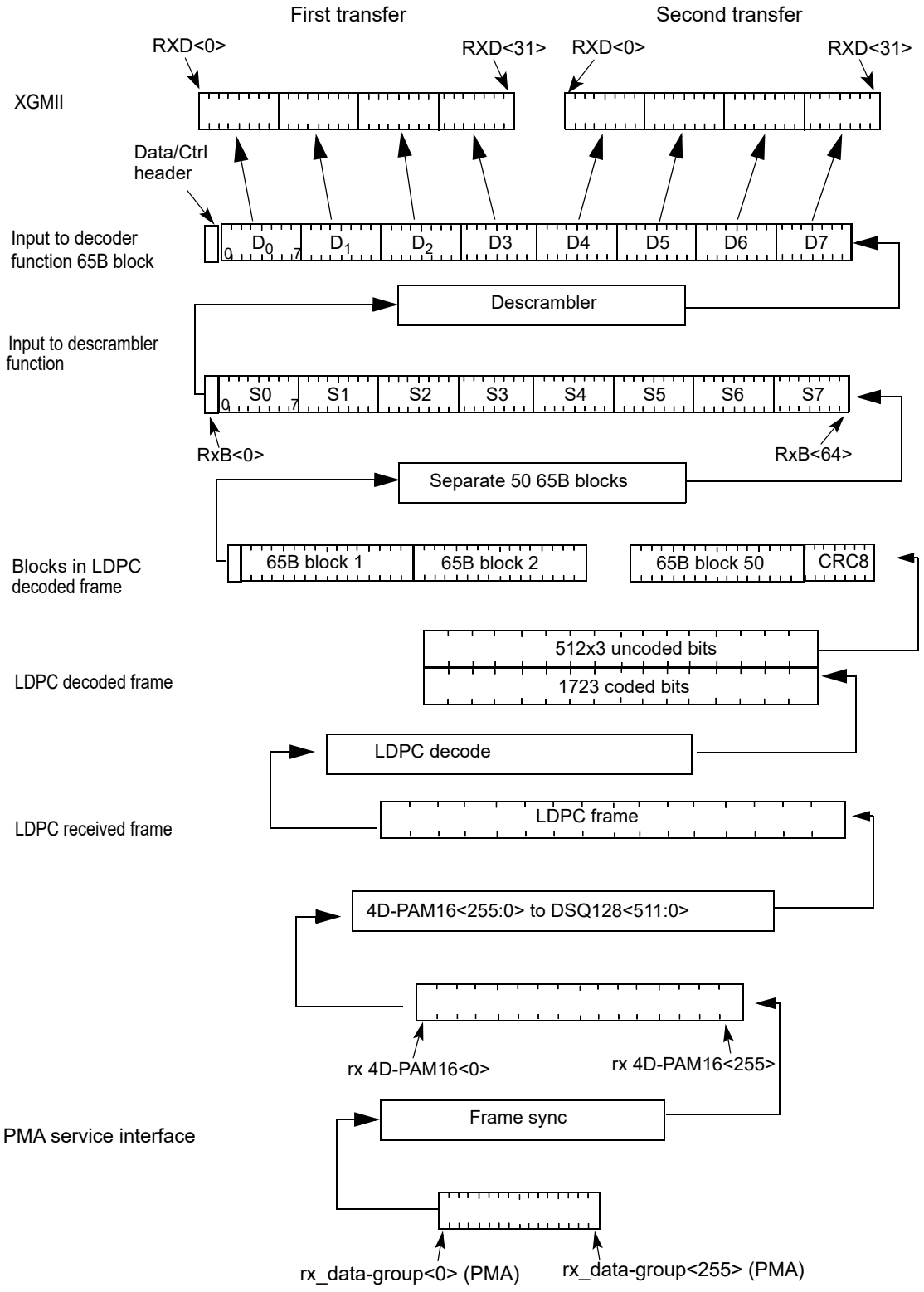

Figure 55–7—PCS Receive bit ordering

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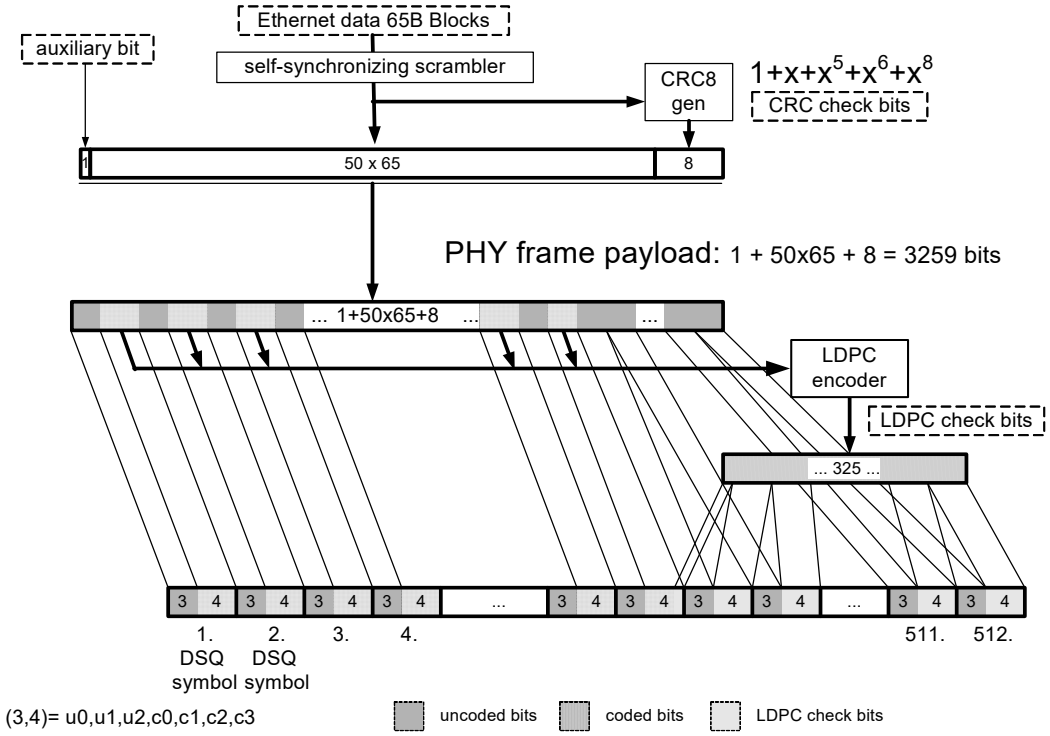

Figure 55–8—PCS detailed transmit bit ordering

Data blocks contain eight data characters. Control blocks begin with an 8-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that character is implied by the block type field. Other control characters are encoded in a 7-bit control code or a 4-bit O Code. Each control block contains eight characters.

The format of the blocks is as shown in Figure 55–9. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the Input Data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt.

Bits and field positions are shown with the least significant bit on the left. Hexadecimal numbers are shown prepended with '0x', and with the least significant digit on the right. For example the block type field 0x1E is sent as 01111000 representing bits 1 through 8 of the 65-bit block. The least significant bit for each field is placed in the lowest numbered position of the field.

All unused values of block type field[106] are reserved.

[106]The block type field values have been chosen to have a 4-bit Hamming distance between them. The only unused value that maintains the Hamming distance is 0x00.

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55.3.2.2.6 Control codes

The same set of control characters are supported by the XGMII and the 10GBASE-T PCS. The representations of the control characters are the control codes. XGMII encodes a control character into an octet (an 8-bit value). The 10GBASE-T PCS encodes the start and terminate control characters implicitly by the block type field. The 10GBASE-T PCS encodes the ordered set control codes using a combination of the block type field and a 4-bit O code for each ordered set. The 10GBASE-T PCS encodes each of the other control characters into a 7-bit C code).

The control characters and their mappings to 10GBASE-T control codes and XGMII control codes are specified in Table 55–1. All XGMII and 10GBASE-T control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

Input Data	data ctrl header	**Block Payload**							
Bit Position: / **Data Block Format:**	0	1							64
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 55–9—64B/65B block formats

55.3.2.2.7 Ordered sets

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and local fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the XGMII. 10 Gigabit Ethernet uses one kind of ordered set: the sequence ordered set (see 46.3.4). The sequence ordered set control character is denoted /Q/. An additional ordered set, the signal ordered set, has been reserved and it begins with another control code. The 4-bit O field encodes the control code. See Table 55–1 for the mappings.

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55.3.2.2.8 Valid and invalid blocks

A block is invalid if any of the following conditions exists:

a) The block type field contains a reserved value.
b) Any control character contains a value not in Table 55–1.
c) Any O code contains a value not in Table 55–1.
d) The set of eight XGMII characters does not have a corresponding block format in Figure 55–9.
e) The block contains the payload of an invalid received PHY frame or the first 64B/65B block following an invalid received PHY frame to account for self-synchronizing scrambler error propagation.

55.3.2.2.9 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

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Table 55–1—Control codes

Control character	Notation	XGMII control code	10GBASE-T control code	10GBASE-T O code	8B/10B code[a]
idle	/I/	0x07	0x00		K28.0 or K28.3 or K28.5 without D20.5[b]
LPI	/LI/	0x06	0x06		K28.0 or K28.3 or K28.5 with D20.5[b]
start	/S/	0xFB	Encoded by block type field		K27.7
terminate	/T/	0xFD	Encoded by block type field		K29.7
error	/E/	0xFE	0x1E		K30.7
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0	K28.4
reserved0	/R/[c]	0x1C	0x2D		K28.0
reserved1		0x3C	0x33		K28.1
reserved2	/A/	0x7C	0x4B		K28.3
reserved3	/K/	0xBC	0x55		K28.5
reserved4		0xDC	0x66		K28.6
reserved5		0xF7	0x78		K23.7
Signal ordered set[d]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF	K28.2

[a]For information only. The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48.
[b]Use of idle and LPI ordered sets per 48.2.4.2.
[c]The codes for /A/, /K/, and /R/ are used on the XAUI interface to signal idle. They are not present on the XGMII when no errors have occurred, but certain bit errors cause the XGXS to send them on the XGMII.
[d]Reserved for INCITS T11 Fibre Channel use.

55.3.2.2.10 LPI (/LI/)

Low power idle (LPI) control characters (/LI/) on the XGMII indicate that the LPI client is requesting operation in the LPI transmit mode. A continuous stream of LPI control characters (/LI/) is used to maintain a link in the LPI transmit mode. Idle control characters (/I/) are used to transition from the LPI transmit mode to the normal mode. EEE compliant PHYs respond to the LPI XGMII control characters using the

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procedure outlined in 55.1.3.3. LPI characters may be added or deleted by the PCS to adapt between clock rates. /LI/ insertion and deletion shall occur in groups of four. /LI/s may be added following low power idle characters. They shall not be added while data is being received.

If EEE is not supported, then /LI/ is not a valid control character.

55.3.2.2.11 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<0:7> and RXD<0:7>). Receipt of an /S/ on any other octet of TxD indicates an error. Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

55.3.2.2.12 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and on any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

55.3.2.2.13 ordered set (/O/)

The ordered set control characters (/O/) indicate the start of an ordered set. There are two kinds of ordered sets: the sequence ordered set and the signal ordered set (which is reserved). When it is necessary to designate the control character for the sequence ordered set specifically, /Q/ is used. /O/ is only valid on the first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered set.

Sequence ordered sets may be deleted by the PCS to adapt between clock rates. Such deletion shall only occur when two consecutive sequence ordered sets have been received and shall delete only one of the two. Only Idles may be inserted for clock compensation. Signal ordered sets are not deleted for clock compensation.

55.3.2.2.14 Error (/E/)

The /E/ is sent whenever an /E/ is received. It is also sent when invalid blocks are received. The /E/ allows physical sublayers such as the XGXS and PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 55.3.6.2.4 for further information.

55.3.2.2.15 Transmit process

The transmit process generates blocks based upon the TXD<31:0> and TXC<3:0> signals received from the XGMII. Two XGMII data transfers are encoded into each block. It takes 256 PMA_UNITDATA transfers to send an LDPC frame of data. Therefore, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 25:64, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the transmit process state diagram. The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

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55.3.2.2.16 PCS scrambler

The payload of the PCS PHY frame is scrambled with a self-synchronizing scrambler. The scrambler for the MASTER shall produce the same result as the implementation shown in Figure 55–10. This implements the scrambler polynomial:[107]

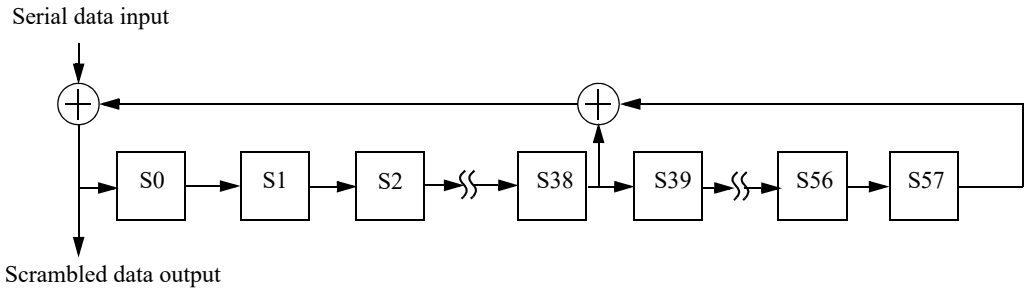
$$G(x) = 1 + x^{39} + x^{58} \tag{55–1}$$

The scrambler for the SLAVE shall produce the same result as the implementation shown in Figure 55–10. This implements the scrambler polynomial:

$$G(x) = 1 + x^{19} + x^{58} \tag{55–2}$$

The initial seed values for the MASTER and SLAVE are left to the implementer. The scrambler is run continuously on all payload bits.

PCS scrambler employed by the MASTER



PCS scrambler employed by the SLAVE

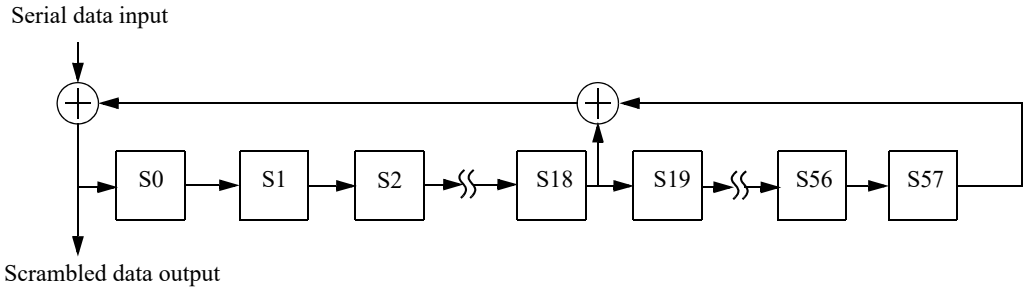


Figure 55–10—MASTER and SLAVE PCS scramblers

[107]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (55–1). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.

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55.3.2.2.17 CRC8

The aggregated 50 65B blocks shall be used to calculate the cyclic redundancy check parity bits for each PHY frame. The parity bits are generated by the following CRC8 cyclic generator polynomial:

$$C(x) = 1 + x + x^5 + x^6 + x^8 \quad (55–3)$$

The CRC8 shall produce the same result as the implementation shown in Figure 55–11. In Figure 55–11 the 8 delay elements S0,..., S7, shall be initialized to zero. Afterwards the 50 65B blocks of serial data input are used to compute the CRC8 with the switch connected, which is setting CRCgen in Figure 55–11. After all the 50 65B blocks have been processed, the switch is disconnected (setting CRCout) and the 8 values stored in the delay elements are transmitted in the order illustrated, first S7, followed by S6, and so on until the final value S0.

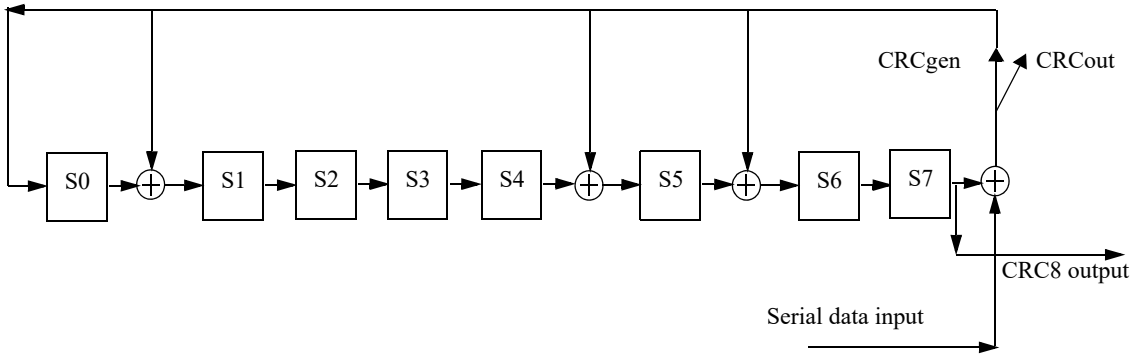

Figure 55–11—CRC8

55.3.2.2.18 LDPC encoder

The resulting payload of scrambled 50 65B blocks, followed by the corresponding 8 bits from the CRC8 and preceded by 1 auxiliary bit results in a total payload of 50 × 65 + 8 +1 = 3259 bits. The use of this bit for vendor-specific communication is outside the scope of this document. For the purposes of this standard it is ignored by the link partner. From the total payload of 3259 bits, 1536 (3 bits for each of the 512 DSQ128 symbols) are uncoded bits and the remaining 1723 shall be encoded by the LDPC(1723, 2048) generator matrix G. G is described in Annex 55A.

The LPDC encoding takes the 1723 bit input code vector $x = [x_0\ x_1\ x_2\ ...\ x_{1722}]$, and shall generate the 2048 bit codeword c represented by the matrix multiplication $c = x \times G$. For both x and c the encoder shall follow the notation described in 55.3.2.2.3 where the LSB (leftmost element of the vectors x and c) is the first bit into the LDPC encoder and the first transmitted bit.

55.3.2.2.19 DSQ128 bit mapping

DSQ128 refers to a two dimensional constellation with 128 possible 2D values, such that the combined 2D symbol carries $\log_2(128)$ or 7 bits. The PHY frame of 1536 uncoded bits and 2048 (LDPC output) coded bits described in Figure 55–6 shall be partitioned into 7-bit groups of (3 uncoded, 4 coded) as described in Figure 55–8. The bit partition is as follows, the first 1290 (3 × 430) uncoded bits are paired with the first 1720 (4 × 430) LDPC input bits. The following 3 uncoded bits are paired with the last 3 LDPC input bits and the first LDPC parity bit. Finally the remaining 243 (3 × 81) uncoded bits are paired with the remaining 324 (4 × 81) LDPC parity bits.

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Each 2D-DSQ128 value has two PAM16 components denoted $PAM16_1$ and $PAM16_2$ respectively. The DSQ128 can be constructed by pruning the 256 values of a 2D-PAM16 where every other point in 2D is discarded (like the black or white squares in a checkerboard). The PAM16 components $PAM16_1$ and $PAM16_2$ can each take any of the values from the set {–15, –13, –11, –9, –7, –5, –3, –1, 1, 3, 5, 7, 9, 11, 13, 15}. The mapping from 7 bits where u_0 u_1 u_2 denote the 3 uncoded bits and c_0 c_1 c_2 c_3 denote the 4 coded bits to the DSQ128 is described by the following four steps (the bits from the scrambler output shall be read LSB first):

Step 1:

$x_{13} = (!u_0)\ \&\ u_2$

$x_{12} = u_0$ XOR u_2

$x_{11} = c_0$

$x_{10} = c_0$ XOR c_1

$x_{23} = (u_1\ \&\ u_2)$ OR $(u_0\ \&\ !u_1)$

$x_{22} = u_1$ XOR u_2

$x_{21} = c_2$

$x_{20} = c_2$ XOR c_3

Step 2:

$x_1 = 8x_{13} + 4x_{12} + 2x_{11} + x_{10}$

$x_2 = 8x_{23} + 4x_{22} + 2x_{21} + x_{20}$

Step 3:

$y_1 = (x_1 + x_2)$ mod16

$y_2 = (–x_1 + x_2)$ mod16

Step 4:

$PAM16_1 = 2y_1 – 15$

$PAM16_2 = 2y_2 – 15$

where '*n* mod16' for an integer *n*, is defined as the integer value *p* in the range 0 to 15 (both inclusive) such that '$p = n + 16m$', for some integer *m*.

55.3.2.2.20 DSQ128 to 4D-PAM16

The DSQ mapper generates 512 2D-DSQ128 symbols per LDPC frame that are mapped onto 256 4D-PAM16 symbols prior to sending to the PMA via PMA_UNITDATA.request. The mapping of DSQ128 to 4D-PAM16 is illustrated in Figure 55–6. As shown in Figure 55–6, the two PAM16 components of each DSQ128 symbol are mapped onto two consecutive time periods on the same wire pair.

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55.3.2.2.21 65B-LDPC framer

The 65B-LDPC framer adapts between the 65-bit width of the 65B blocks and the 4D-PAM16 width of the PMA. When the transmit channel is operating in normal mode, the 65B-LDPC sends four PAM16 of transmit data at a time via PMA_UNITDATA.request primitives. The PMA_UNITDATA.request primitives are fully packed with bits.

55.3.2.2.22 EEE capability

The optional 10GBASE-T EEE capability allows compliant PHYs to transition to an LPI mode of operation when link utilization is low.

EEE compliant PHYs shall implement the EEE transmit state diagram, shown in Figure 55–20, within the PCS.

When PCS_Reset is asserted or pcs_data_mode is not asserted, the state diagram enters the TX_NORMAL state.

When a complete 64B/65B block of LPI characters is generated by the PCS transmit function, the PHY transmits the sleep signal to indicate to the link partner that it is transitioning to the LPI transmit mode. If the sleep signal begins on an LDPC frame boundary, then it contains 9 full LDPC frames each composed entirely of 64B/65B LDPC-encoded LP_IDLE blocks. If the sleep signal does not begin on an LDPC frame boundary, then it contains one LDPC frame partially composed of LP_IDLE blocks followed by 9 LDPC frames fully composed of LP_IDLE blocks.

Following the transmission of the sleep signal, quiet-refresh signaling begins, as described in 55.3.5.

After the sleep signal is transmitted LPI control characters shall be input to the PCS scrambler continuously until the PCS Transmit Function exits the LPI transmit mode.

While the PMA asserts SEND_N, the lpi_tx_mode variable shall control the transmit signal through the PMA_UNITDATA.request primitive described as follows:

When the PHY is not in the PCS_Data state, the lpi_tx_mode variable is ignored.

When the lpi_tx_mode variable takes the value NORMAL and the PMA asserts SEND_N, the PCS passes coded data to the PMA via the PMA_UNITDATA.request primitive as described in 55.3.2.2.

When the lpi_tx_mode variable takes the value QUIET and the PMA asserts SEND_N, the PCS passes zeros to the PMA through the PMA_UNITDATA.request primitive.

When the lpi_tx_mode variable takes the value REFRESH_A and the PMA asserts SEND_N, the PCS passes the PMA training signal to the PMA on pair A, to allow both the local and remote PHY to refresh adaptive filters and timing loops. The PCS passes zeros to all other pairs in this condition. REFRESH_B, REFRESH_C and REFRESH_D operate in a analogous manner for the other pairs.

When the lpi_tx_mode variable takes the value ALERT and the PMA asserts SEND_N, the PCS passes the ALERT vector to the PMA.

The quiet-refresh cycle is repeated until codewords other than LP_IDLE are detected at the XGMII. These codewords indicate that the local system is requesting a transition back to the normal operational mode. Following this event, the PMA_UNITDATA.request parameter tx_symb_vector is set to the value ALERT. The alert signal is not synchronized with respect to the quiet-refresh cycle but shall be synchronized so that the alert signal from the PMA begins on a LDPC frame boundary.

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The PHY will also transition back to the normal operation mode if an error condition occurs. This error condition is defined as the detection of any characters other than LPI or IDLE at the XGMII.

After the alert signal the PCS completes the transition from LPI mode to normal mode by sending a wake signal containing lpi_wake_time LDPC frames composed of IDLE 64B/65B blocks.

lpi_wake_time is a fixed parameter that is defined as 9 LDPC frames as shown in Table 55–2. The maximum PHY wake time when wake is requested before sleep has been completely transmitted is 7.36 μs (lpi_wake_timer=T_{w_phy} as defined by Clause 78). The maximum PHY wake time when wake is requested after sleep has been completely transmitted is 4.48 μs.

Table 55–2—LPI wake time

lpi_wake_time	lpi_wake_timer when wake starts before sleep signal is complete		lpi_wake_timer when wake starts after sleep signal is complete	
(frames)	(frames)	(μs)	(frames)	(μs)
9	23	7.36	14	4.48

55.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B receive state diagram in Figure 55–18 and the PCS Receive bit ordering in Figure 55–7 including compliance with the associated state variables as specified in 55.3.6.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb_vector. The PCS receiver uses knowledge of the encoding rules to correctly align the 65B-LDPC frames. The received 65B-LDPC frames are decoded with error correction; the CRC8 and framing is checked; and the 64B/65B ordered sets are converted to 64-bit data blocks to obtain the signals RXD<31:0> and RXC<3:0> for transmission to the XGMII. Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized to a 25:64 ratio, the receive process inserts idles, delete idles, or delete sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the descrambler state by setting the parameter scr_status to OK.

When the PCS Synchronization process has obtained synchronization, the LDPC frame error ratio (LFER) monitor process monitors the signal quality asserting hi_lfer if excessive LDPC frame errors are detected (LDPC parity error or CRC8 error). If 40 consecutive LDPC frame errors are detected, the block_lock flag is de-asserted. When block_lock is asserted and hi_lfer is de-asserted, the PCS_status parameter of the PMA_PCSSTATUS.request primitive is set to OK, and the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication (loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.request primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training sequence includes 1 bit pattern on pair A every 256 PAM2 symbols,

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which is aligned with the PCS PHY frame boundary. When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.

PHYs with the EEE capability support transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. Transitions to and from the LPI mode are allowed to occur independently in the transmit and receive functions. The PCS receive function is responsible for detecting transitions to and from the LPI receive mode and indicating these transitions using signals defined in 55.2.2.

The link partner signals a transition to the LPI mode of operation by transmitting 9 LDPC frames composed entirely of 64B/65B blocks of /LI/. When blocks of /LI/ are detected at the output of the 64B/65B decoder, rx_lpi_active is asserted by the PCS receive function and the /LI/ character is continuously asserted at the receive XGMII. These frames may be preceded by a frame composed partially of /LI/ characters. After these frames the link partner begins transmitting zeros, and it is recommended that the receiver power down receive circuits to reduce power consumption. The receive function uses LDPC frame counters to maintain synchronization with the remote PHY and receives periodic refresh signals that are used to update coefficients, so that the integrity of adaptive filters and timing loops in the PMA is maintained. LPI signaling is defined in 55.3.5. The quiet-refresh cycle continues until the PMA asserts alert_detect to indicate that the alert signal has been reliably detected. After the alert signal the link partner transmits repeated /I/ characters, representing a wake signal. The PHY receive function sends /I/ to the XGMII for 9 LDPC frame periods and then resumes normal operation.

55.3.2.3.1 Frame and block synchronization

When the receive channel is operating in normal mode, the frame and block synchronization function receives data via 4D-PAM16 PMA_UNITDATA.request primitives. It shall form a 4D-PAM16 stream from the primitives by concatenating requests with the PAM16s of each primitive in order from rx_data-group<0> to rx_data-group<255> (see Figure 55–7). It obtains block_lock to the LDPC frames during the PAM2 training pattern using synchronization bits provided on pair A. The 65-bit blocks are extracted based on their location in the LDPC frame.

55.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. It shall produce the same result as the implementations shown in Figure 55–12 for the MASTER and the SLAVE.

55.3.2.3.3 CRC8 receive function

The PCS Receive function shall check the integrity of the CRC8 parity bits defined in 55.3.2.2.17. If the CRC check fails the PHY frame is invalid.

The PCS Receive function may decode and check the CRC8 parity bits simultaneous to resolving the LDPC error correction function. It is recommended that the PCS receiver not use the CRC8 parity check code to assist the LDPC convergence.

55.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel and remote receiver. When the transmit PCS is operating in test-pattern mode it shall transmit continuously as illustrated in Figure 55–6, with the input to the scrambler set to zero and the initial condition of the scrambler set to any non-zero value. When the receiver PCS is operating in test-pattern mode it shall receive continuously as illustrated in Figure 55–7. After acquiring the self-synchronizing scrambler state, the output of the received scrambled values should ideally be zero. Any nonzero values correspond to receiver bit errors. This mode is further described as test mode 7 in 55.5.2

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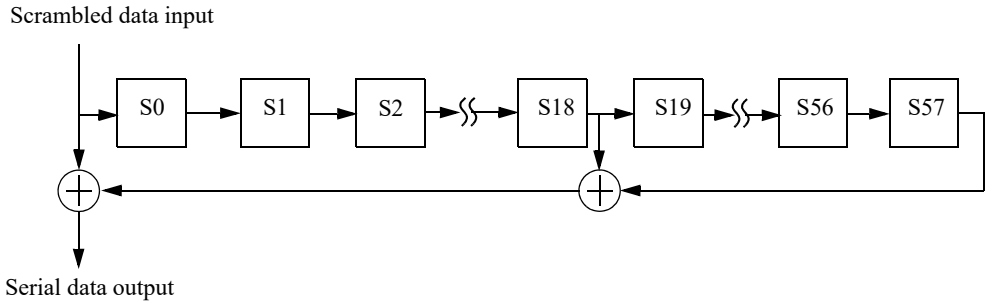
PCS descrambler employed by the MASTER



PCS descrambler employed by the SLAVE

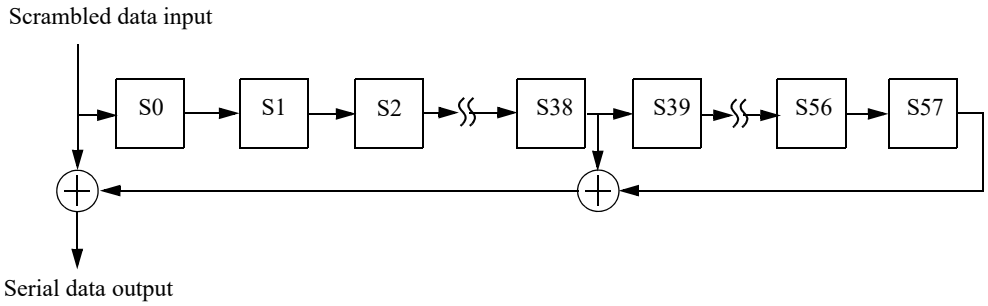


Figure 55–12—MASTER and SLAVE PCS descramblers

55.3.4 PMA training side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling for generating 2-level PAM PMA training sequences as shown in Figure 55–13. An implementation of MASTER and SLAVE PHY side-stream scramblers is shown in the “Main PN sequence” box. The bits stored in the shift register delay line at time *n* are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

NOTE—During Auto-Negotiation a device may request its link partner to use periodic training sequence initialization. This function is deprecated; devices may ignore this request if it is received, and it is recommended not to send it. A device that receives this request and does not ignore it generates a periodically repeating pattern by reinitializing its scrambler state after every 16 384 symbol periods to the 33-bit value generated by combining 0x39A422 for the 22 MSBs and random value SB10-SB0 from Table 55–15 generated by the local device for the 11 LSBs as shown in Figure 55–13.

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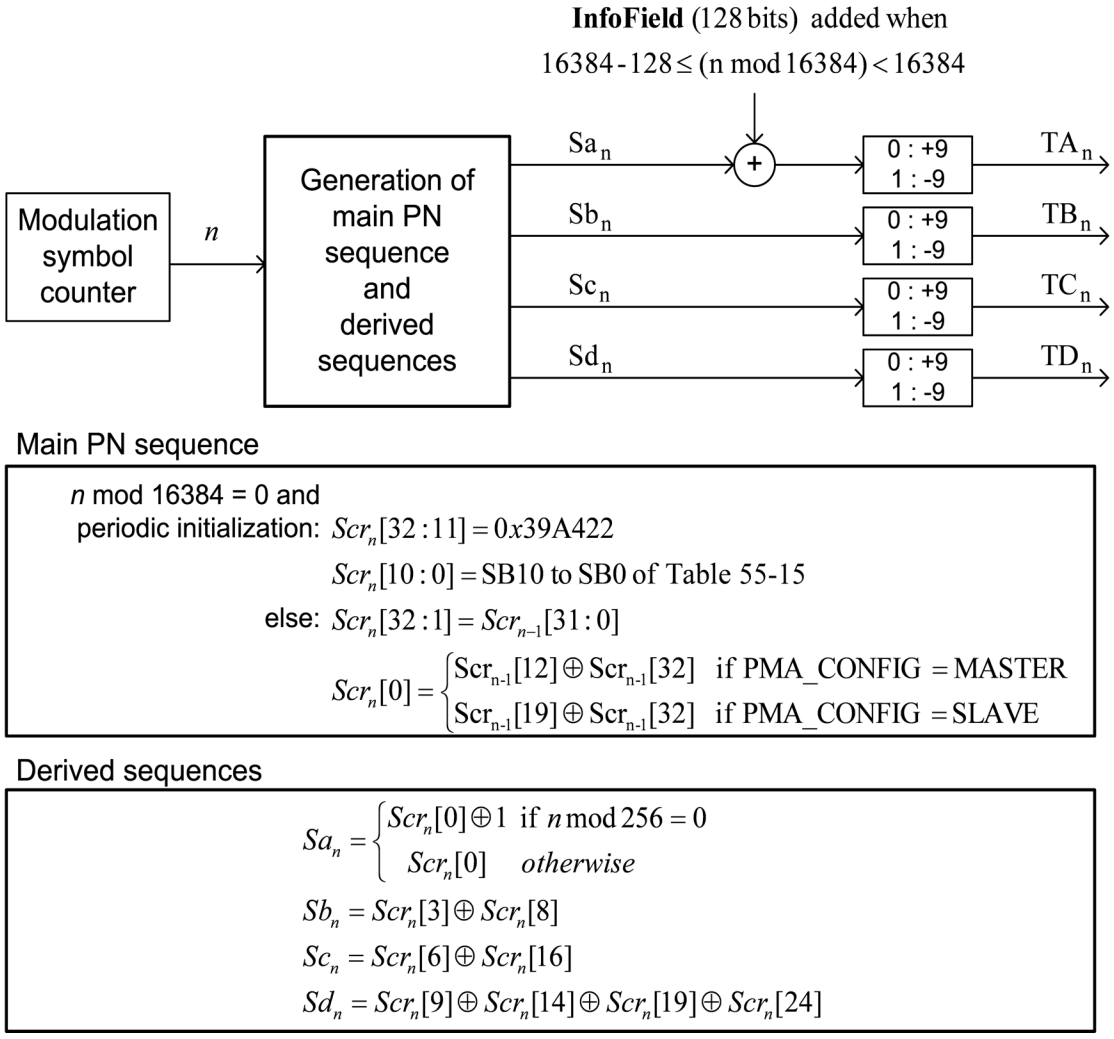

Figure 55–13—A realization of PMA training PAM2 sequences

55.3.4.1 Generation of bits Sa_n, Sb_n, Sc_n, Sd_n

PMA training signal encoding rules are based on the generation, at time n, of the four bits Sa_n, Sb_n, Sc_n, Sd_n. These four bits are generated in a systematic fashion using the bits in $Scr_n[32:0]$, and an auxiliary generating polynomial. For both MASTER and SLAVE PHYs, they are obtained by the same linear combinations of bits stored in the transmit scrambler shift register delay line. These four bits are derived from elements of the same maximum-length shift register sequence of length $2^{33}–1$ as $Scr_n[0]$, but shifted in time. The associated delays are all large and different so that there is no short-term correlation among the bits Sa_n, Sb_n, Sc_n, Sd_n. The four bits are generated using the bit $Scr_n[0]$ and the equations in Figure 55–13 in the "Derived sequences" box.

55.3.4.2 Generation of 4D symbols TA_n, TB_n, TC_n, TD_n

The four bits Sa_n, Sb_n, Sc_n, Sd_n are mapped to a 4D symbol (TA_n, TB_n, TC_n, TD_n) as shown in Figure 55–13.

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The inversion on pair A at 256 intervals ($n = k \times 256, k = 0, 1, 2, \ldots$) defines the LDPC boundary during data mode. If requested by the link partner, the PCS shall reset the training mode scrambler every 16384 periods aligned with the 256 symbol period inversion on pair A, which corresponds to the time instants $n = m \times 16384, m = 0, 1, 2, \ldots$

Notice that over the repeating time intervals of 16384 and of length 128, $m \times 16384 - 128 \le n < m \times 16384, m = 1, 2, 3, \ldots,$ the PMA training pattern in pair A is XOR'ed with the InfoField. Thus, pair A transmits the InfoField, which communicates to the remote transceiver settings of THP and power backoff and other control information.

55.3.4.3 PMA training mode descrambler polynomials

The PHY shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial $g'_M(x) = 1 + x^{20} + x^{33}$ and the SLAVE PHY shall employ the receiver descrambler generator polynomial $g'_S(x) = 1 + x^{13} + x^{33}$.

55.3.5 LPI signaling

PHYs with EEE capability have transmit and receive functions that can enter and leave the LPI mode independently. The PHY can transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. The transmit function of the PHY initiates a transition to the LPI transmit mode when it generates 64B/65B blocks composed entirely of LPI control characters, as described in 55.3.2.2.22. The transmit function of the link partner signals the transition using the sleep signal. When the transmitter begins to send the sleep signal, it asserts tx_lpi_active and the transmit function enters the LPI transmit mode.

Within the LPI mode PHYs use a repeating quiet-refresh cycle (see Figure 55–14). The first part of this cycle is known as the quiet period and lasts for a time lpi_quiet_time equal to 124 LDPC frame periods. The quiet period is defined in 55.3.5.2. The second part of this cycle is known as the refresh period and lasts for a time lpi_refresh_time equal to 4 LDPC frame periods. The refresh period is defined in 55.3.5.3. A cycle composed of one quiet period and one refresh period is known as a single pair LPI cycle and lasts for a time lpi_qr_time equal to 128 LDPC frame periods. The time taken to complete a quiet-refresh cycle for all four pairs is known as a complete LPI cycle.

lpi_offset, lpi_quiet_time, lpi_refresh_time, lpi_qr_time, and lpi_allpairs_qr_time are timing parameters that are integer multiples of the LDPC frame period. lpi_offset is a fixed value equal to lpi_qr_time/2 that is used to ensure refresh signals are appropriately offset by the link partners.

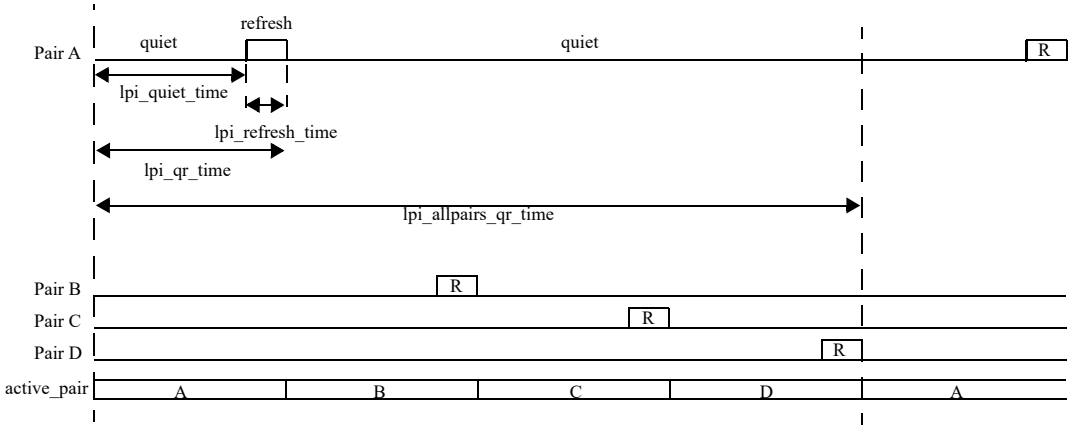

Figure 55–14—Timing periods for LPI signals

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PHYs begin the transition from the LPI receive mode when the alert signal is detected by the PMA as defined in 55.4.2.4.

55.3.5.1 LPI Synchronization

To maximize power savings, maintain link integrity, and ensure interoperability, EEE-capable PHYs synchronize refresh intervals during the LPI mode. The transition to PCS_Test is used as a fixed timing reference for the link partners. Refresh signaling is derived by counting LDPC frames from the transition to PCS_Test. An EEE-capable PHY shall support loop timing and loop timing shall be enabled on the slave PHY.

In initial training, normal retraining, and fast retraining, with or without the EEE capability being supported, the master and slave signal when they will transition to PCS_Test using the transition counter following the procedure described in 55.4.2.5.14.

A EEE-capable PHY in slave mode is responsible for synchronizing its PMA training frame to the master's PMA training frame during the transition to PMA_Training_Init_S. The slave shall ensure that its PMA training frames are synchronized to the master's PMA training frames within 1 LDPC frame, measured at the slave MDI on pair A. In addition, the slave shall initialize its transition counter so that it transitions to PCS_Test within 1 LDPC frame of the master PHY's transition to PCS_Test, measured at the slave PHY's MDI on pair A. This mechanism ensures that the refresh offset is bounded to a small value at both MDI interfaces, thus ensuring there is no overlap of master and slave signals when both transmit and receive are in the LPI mode.

Following the transition to PCS_Test, the PCS counts transmitted and received LDPC frames, and uses these counters to generate refresh and pair control signals for the transmit and receive functions. The transmitted LDPC frame count is named tx_ldpc_frame_cnt. The received LDPC frame count is named rx_ldpc_frame_cnt.

The master and slave shall derive the active pair and refresh_active signals from the LDPC frame counters as shown in Table 55–3 and Table 55–4.

Table 55–3—Synchronization logic derived from slave signal LDPC frame count

Slave-side variable	Master-side variable	for master u=rx_ldpc_frame_cnt for slave u=tx_ldpc_frame_cnt
tx_refresh_active=true	rx_refresh_active=true	lpi_offset – lpi_refresh_time ≤ mod(u,lpi_qr_time) < lpi_offset
tx_lpi_full_refresh=true	N/A	lpi_offset – lpi_refresh_time = mod(u,lpi_qr_time)
tx_active_pair=PAIR_A	rx_active_pair=PAIR_A	lpi_offset + lpi_qr_time ≤ u < lpi_offset + 2 x lpi_qr_time
tx_active_pair=PAIR_B	rx_active_pair=PAIR_B	lpi_offset + 2 x lpi_qr_time ≤ u < lpi_offset + 3 x lpi_qr_time
tx_active_pair=PAIR_C	rx_active_pair=PAIR_C	lpi_offset + 3 x lpi_qr_time ≤ u < 4 x lpi_qr_time OR 0 ≤ u < lpi_offset
tx_active_pair=PAIR_D	rx_active_pair=PAIR_D	lpi_offset ≤ u < lpi_offset + lpi_qr_time

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Table 55–4—Synchronization logic derived from master signal LDPC frame count

Slave-side variable	Master-side variable	for master v=tx_ldpc_frame_cnt for slave v=rx_ldpc_frame_cnt
rx_refresh_active=true	tx_refresh_active=true	lpi_quiet_time ≤ mod(v,lpi_qr_-time)
N/A	tx_lpi_full_refresh=true	lpi_quiet_time = mod(v,lpi_qr_-time)
rx_active_pair=PAIR_A	tx_active_pair=PAIR_A	0 ≤ v < lpi_qr_time
rx_active_pair=PAIR_B	tx_active_pair=PAIR_B	lpi_qr_time ≤ v < 2 x lpi_qr_time
rx_active_pair=PAIR_C	tx_active_pair=PAIR_C	2 x lpi_qr_time ≤ v < 3 x lpi_qr_-time
rx_active_pair=PAIR_D	tx_active_pair=PAIR_D	3 x lpi_qr_time ≤ v < 4 x lpi_qr_-time

55.3.5.2 Quiet period signaling

During the quiet period the transmitters on all four pairs should be turned off. Average launch power (as measured from 28 LDPC frames after a refresh period to 28 LDPC frames before the next refresh period on the same lane) for each Transmitter shall be less than –41dBm. This requirement does not apply to the periods when the alert signal is transmitted as defined in 55.4.2.2.1.

55.3.5.3 Refresh period signaling

During the LPI mode 10GBASE-T PHYs use staggered, out-of-phase refresh signaling to maximize power savings. Two-level PAM refresh symbols are generated using the PMA side-stream scrambler polynomials described in 55.3.4 and exactly as is shown in Figure 55–13 with the exception that the InfoField consists of a sequence of 128 zeros. The training sequence without periodic reinitialization described in 55.3.4 shall be used during the LPI mode, with the scramblers free-running from PCS Reset. If scrambler reinitialization is used for normal training, it shall be disabled and the scramblers shall begin free-running when the PHY Control state diagram enters the PCS_Test state.

Refresh signals shall be sent using the THP filter as described in 55.4.3.1. At the start of each refresh signal the THP feedback delay line shall be initialized with zeros.

While a transmit function is in the LPI transmit mode only one of the transmit pairs will be active during a refresh period. tx_symb_vector for all transmit pairs that are not active shall be set to zero.

When tx_symb_vector has the value ALERT and the PHY is master, the transmitter on pair A shall be active and all other pairs shall be quiet. When tx_symb_vector has the value ALERT and the PHY is slave, the transmitter on pair C shall be active and all other pairs shall be quiet. If lpi_tx_mode=REFRESH_A on a MASTER PHY or lpi_tx_mode=REFRESH_C on a SLAVE PHY, and tx_symb_vector has the value ALERT, then the alert signaling shall be transmitted in place of the refresh signaling where the signals overlap.

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55.3.6 Detailed functions and state diagrams

55.3.6.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

55.3.6.2 State diagram parameters

55.3.6.2.1 Constants

EBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in 46.3.4.

LBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing two Local Fault ordered sets.

LPBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII containing /LI/ in all the eight character locations.

LPBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing /LI/ in all the eight character locations.

IBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII containing /I/ in all the eight character locations.

IBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing /I/ in all the eight character locations.

UBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII containing two Link Interruption ordered sets. The Link Interruption ordered set is defined in 46.3.4.

55.3.6.2.2 Variables

lfer_test_lf
: Boolean variable that is set true when a new LDPC frame is available for testing and false when LFER_TEST_LF state is entered. A new LDPC frame is available for testing when the Block Sync process has accumulated enough symbols from the PMA to evaluate the next LDPC frame.

block_lock
: Boolean variable that is set true when receiver acquires block delineation.

hi_lfer
: Boolean variable which is asserted true when the lfer_cnt reaches 16 indicating a bit error ratio $> 4 \times 10^{-4}$.

pcs_reset
: Boolean variable that controls the resetting of the PCS. It is true whenever a reset is necessary

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including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rx_coded<64:0>

Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 55–9. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_raw<71:0>

Vector containing two successive XGMII output transfers. RXC<0> through RXC<3> for the first transfer are taken from rx_raw<0> through rx_raw<3>, respectively. RXC<0> through RXC<3> for the second transfer are taken from rx_raw<4> through rx_raw<7>, respectively. RXD<0> through RXD<31> for the first transfer are taken from rx_raw<8> through rx_raw<39>, respectively. RXD<0> through RXD<31> for the second transfer are taken from rx_raw<40> through rx_raw<71>, respectively.

lf_valid

Boolean indication that is set true if received LDPC frame is valid. LDPC frame is valid if:

a. All parity checks of the coded bits are satisfied
b. CRC8 check is satisfied

tx_coded<64:0>

Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 55–9. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_raw<71:0>

Vector containing two successive XGMII transfers. TXC<0> through TXC<3> for the first transfer are placed in tx_raw<0> through tx_raw<3>, respectively. TXC<0> through TXC<3> for the second transfer are placed in tx_raw<4> through tx_raw<7>, respectively. TXD<0> through TXD<31> for the first transfer are placed in tx_raw<8> through tx_raw<39>, respectively. TXD<0> through TXD<31> for the second transfer are placed in tx_raw<40> through tx_raw<71>, respectively.

The following variables are required for PHYs that support the EEE capability:

tx_lpi_active

A Boolean variable that is set true when the PHY transmit function is operating in the LPI transmit mode and during transitions to and from the LPI transmit mode (i.e., at any time when the PHY is transmitting sleep, alert, wake, or quiet-refresh signaling). It is set false otherwise.

tx_lpi_qr_active

A Boolean variable that is set true during the LPI transmit mode, when the PHY is transmitting quiet-refresh signaling. Set false otherwise.

rx_lpi_active

A Boolean variable that is set true when the PHY receive function is operating in the LPI receive mode and set false otherwise. The LPI receive mode begins when the sleep signal is detected and lasts until the alert signal is detected. When the EEE capability is not supported, rx_lpi_active is set false.

tx_lpi_req

A Boolean variable that is set true when the LPI client indicates that it is requesting operation in the LPI transmit mode via the XGMII and set false otherwise.

alert_detect

Indicates that an alert signal from the link partner has been received at the MDI as indicated by PMA_ALERTDETECT.indication(alert_detect).

tx_lpi_alert_active

A Boolean variable that is set true when the PHY is transmitting ALERT signaling. Set false otherwise.

rx_lpi_wake

A Boolean variable that is set true when the PHY receiver is in the WAKE state and sending IDLE to the XGMII. Set false otherwise. When the EEE capability is not supported, rx_lpi_wake is set false.

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tx_active_pair
: A variable indicating the transmit active pair during the LPI transmit mode. The variable may take the values PAIR_A, PAIR_B, PAIR_C, PAIR_D. This variable is defined in 55.3.5.1.

lpi_tx_mode
: A variable indicating the signaling to be used from the PCS to the PMA across the PMA_UNITDATA.request (tx_symb_vector) interface.
lpi_tx_mode controls tx_symb_vector only when tx_mode is set to SEND_N.
The variable is set to NORMAL when (!tx_lpi_qr_active * !tx_lpi_alert_active), indicating that the PCS is in the normal mode of operation and will encode code-groups as described in Figure 55–16 and Figure 55–17.
The variable is set to REFRESH_A when (tx_lpi_qr_active * (tx_active_pair==PAIR_A) * tx_refresh active).
The variable is set to REFRESH_B when (tx_lpi_qr_active * (tx_active_pair==PAIR_B) * tx_refresh active).
The variable is set to REFRESH_C when (tx_lpi_qr_active * (tx_active_pair==PAIR_C) * tx_refresh active).
The variable is set to REFRESH_D when (tx_lpi_qr_active * (tx_active_pair==PAIR_D) * tx_refresh active).
The variable is set to QUIET when (tx_lpi_qr_active * (!tx _refresh_active + tx_lpi_initial_quiet))
The variable is set to ALERT when (tx_lpi_alert_active)

tx_refresh_active
: A Boolean value. This variable is set true following the logic described in 55.3.5.1.

tx_lpi_full_refresh
: A Boolean value. This variable is set true following the logic described in 55.3.5.1.

tx_lpi_initial_quiet
: A Boolean value. This variable is set true when the transmit function enters the LPI transmit mode and a partial refresh will be replaced by quiet signaling.

ldpc_frame_done
: A Boolean value. This variable is set true when the final symbol of each LDPC frame is transmitted and is set false otherwise.

The following variable is only required for PHYs that support the fast retrain capability:

fr_sigtype
: If fast retrain is supported, this variable is set based on the value in 1.147.2:1 as follows:
00 IBLOCK_R
01 LBLOCK_R
10 UBLOCK_R
11 Reserved

55.3.6.2.3 Timers

State diagram timers follow the conventions described in 14.2.3.2.

125_ustimer:
: Timer that is triggered every 125 μs +1%, –25%.

The following timers are required for PHYs that support the EEE capability:

lpi_tx_sleep_timer
: This timer defines the time the local transmitter sends the sleep signal to the link partner.

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Values: The condition lpi_tx_sleep_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 9 LDPC frame periods.

lpi_tx_alert_timer
This timer defines the time the local transmitter transmits the alert signal.
Values: The condition lpi_tx_alert_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 4 LDPC frame periods.

lpi_tx_wake_timer:
This timer defines the time the local transmitter transmits the wake signal.
Values: The condition lpi_tx_wake_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time LDPC frame periods.

lpi_rx_wake_timer:
This timer defines the time the receiver sends IDLE blocks to the XGMII after the alert signal is detected.
Values: The condition lpi_rx_wake_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time LDPC frame periods.

55.3.6.2.4 Functions

DECODE(rx_symb_vector<64:0>)
In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the LDPC decoder and decodes the 65B-LDPC bit vector returning a vector rx_raw<71:0>, which is sent to the XGMII. The DECODE function shall decode the block based on code specified in 55.3.2.2.2.

ENCODE(tx_raw<71:0>)
Encodes the 72-bit vector received from the XGMII, returning 65 bit vector tx_coded. The ENCODE function shall encode the block as specified in 55.3.2.2.2.

R_BLOCK_TYPE = {C, S, T, D, E, I, LI, LII}
When the EEE capability is not supported, this function classifies each 65 bit rx_coded vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.
When the EEE capability is supported, this function classifies each 65 bit rx_coded vector as belonging to the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /I/, but in every other case the vector belongs to only one type.
Values: C; The vector contains a data/ctrl header of 1 and one of the following:
a) A block type field of 0x1E and eight valid control characters other than /E/ and /LI/;
b) A block type field of 0x2D or 0x4B, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.

S; The vector contains a data/ctrl header of 1 and one of the following:
a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.

T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.

D; The vector contains a data/ctrl header of 0.

I; If the optional EEE capability is supported, then the I type is a special case of the C type where the vector contains a data/ctrl header of 1, a block type field of 0x1E, and eight control characters of /I/.

LI: If the optional EEE capability is supported, then the LI type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and eight control characters of /LI/.

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LII: If the optional EEE capability is supported, then the LII type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and one of the following:
a) four control characters of /LI/ followed by four control characters of /I/;
b) four control characters of /I/ followed by four control characters of /LI/
E; The vector does not meet the criteria for any other value.

A valid control character is one containing a 10GBASE-T control code specified in Table 55–1. A valid O code is one containing an O code specified in Table 55–1.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E, I, LI, LII}

When the EEE capability is not supported, this function classifies each 72-bit tx_raw vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.

When the EEE capability is supported, this function classifies each 72-bit tx_raw vector as belonging to the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /I/, but in every other case the vector belongs to only one type.

Values: C; The vector contains one of the following:
a) eight valid control characters other than /O/, /S/, /T/, /E/, and /LI/;
b) one valid ordered set and four valid control characters other than /O/, /S/ and /T/;
c) two valid ordered sets.
S; The vector contains an /S/ in its first or fifth character, any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.
T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.
D; The vector contains eight data characters.
I; If the optional EEE capability is supported, then the I type is a special case of the C type where the vector contains eight control characters of /I/.
LI: If the optional EEE capability is supported, then the LI type occurs when the vector contains eight control characters of /LI/.
LII: If the optional EEE capability is supported, then the LII type occurs when the vector contains one of the following:
a) four control characters of /LI/ followed by four control characters of /I/;
b) four control characters of /I/ followed by four control characters of /LI/.
E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 55–1. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 55–1.

T_TYPE(tx_raw<71:0>)

Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

T_TYPE_NEXT

Prescient end of packet check function. It returns the FRAME_TYPE of the tx_raw vector immediately following the current tx_raw vector.

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55.3.6.2.5 Counters

lfer_cnt
: Count up to a maximum of 16 of the number of invalid LDPC frames within the current 125 μs period.

The following counters are required for PHYs that support the EEE capability:

tx_ldpc_frame_cnt
: An integer value that counts transmit LDPC frame periods. The counter is reset when the first symbol of the first LDPC frame crosses the MDI on pair A in the transmit direction after normal training or fast retraining. It is incremented after the last symbol of each transmitted LDPC frame. tx_ldpc_frame_cnt is reset to 0 when tx_ldpc_frame_cnt = lpi_qr_time x 4.

rx_ldpc_frame_cnt
: An integer value that counts receive LDPC frame periods. The counter is reset when the first symbol of the first LDPC frame crosses the MDI on pair A in the receive direction after normal training or fast retraining. It is incremented after the last symbol of each received LDPC frame. rx_ldpc_frame_cnt is reset to 0 when rx_ldpc_frame_cnt = lpi_qr_time x 4.

lpi_rxw_err_cnt
: An integer value that counts the number of receive wake on error conditions. lpi_rxw_err_cnt is reset to zero during PCS_Test. The counter is reflected in register 3.22 (see 45.2.3.12).

55.3.6.3 State diagrams

The LFER Monitor state diagram shown in Figure 55–15 monitors the received signal for high LDPC frame error ratio.

The 64B/65B Transmit state diagram shown in Figure 55–16 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the Transmit state diagram sends Local Fault ordered sets when reset is asserted, the scrambler and 65B-LDPC may not be operational during reset. Thus, the Local Fault ordered sets may not appear on the PMA service interface.

The 64B/65B Receive state diagram shown in Figure 55–18 controls the decoding of 65B received blocks. It makes exactly one transition for each receive block processed except for the transition from RX_WE to RX_E, which occurs immediately after the RX_WE processes are complete.

The PCS shall perform the functions of LFER Monitor, Transmit, and Receive as specified in these state diagrams. The PCS shall not perform the LFER Monitor function during LPI receive operation from the time that the PCS 64B/65B Receiver enters the state RX_L, until the state RX_W is exited.

Transitions surrounded by dashed rectangles indicate requirements for 10GBASE-T EEE-capable implementations.

55.3.7 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

55.3.7.1 Status

PCS_status:
: Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_lfer is false. This status is reflected in MDIO register 3.32.12. A latch low view of this status is

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reflected in MDIO register 3.1.2 and a latch high of the inverse of this status, Receive fault, is reflected in MDIO register 3.8.10.

block_lock:

Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.32.0. A latch low view of this status is reflected in MDIO register 3.33.15.

hi_lfer:

Indicates the state of the hi_lfer variable. This status is reflected in MDIO register 3.32.1. A latch high view of this status is reflected in MDIO register 3.33.14.

Rx LPI indication:

For EEE capability, this variable indicates the current state of the receive LPI function. This flag is set to TRUE (register bit set to one) when the PCS 64B/65B Receive state diagram (Figure 55–19) is in the RX_L or RX_W states. This status is reflected in MDIO register 3.1.8. A latch high view of this status is reflected in MDIO register 3.1.10 (Rx LPI received).

Tx LPI indication

For EEE capability, this variable indicates the current state of the transmit LPI function. This flag is set to TRUE (register bit set to one) when the PCS 64B/65B Transmit state diagram (Figure 55–17) is in the TX_L or TX_W states. This status is reflected in MDIO register 3.1.9. A latch high view of this status is reflected in MDIO register 3.1.11 (Tx LPI received).

55.3.7.2 Counters

The following counters are reset to zero upon read and upon reset of the PCS. When they reach all ones, they stop counting. Their purpose is to help monitor the quality of the link.

lfer_count:

6-bit counter that counts each time LFER_BAD_LF state is entered. This counter is reflected in MDIO register bits 3.33.13:8. The counter is reset when register 3.33 is read by management. Note that this counter counts a maximum of 16 counts per 125 μs since the LFER_BAD_LF can be entered a maximum of 16 times per 125 μs window.

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errored_block_count:
8-bit counter. When the receiver is in normal mode, errored_block_count counts once for each time RX_E state is entered. This counter is reflected in MDIO register bits 3.33.7:0

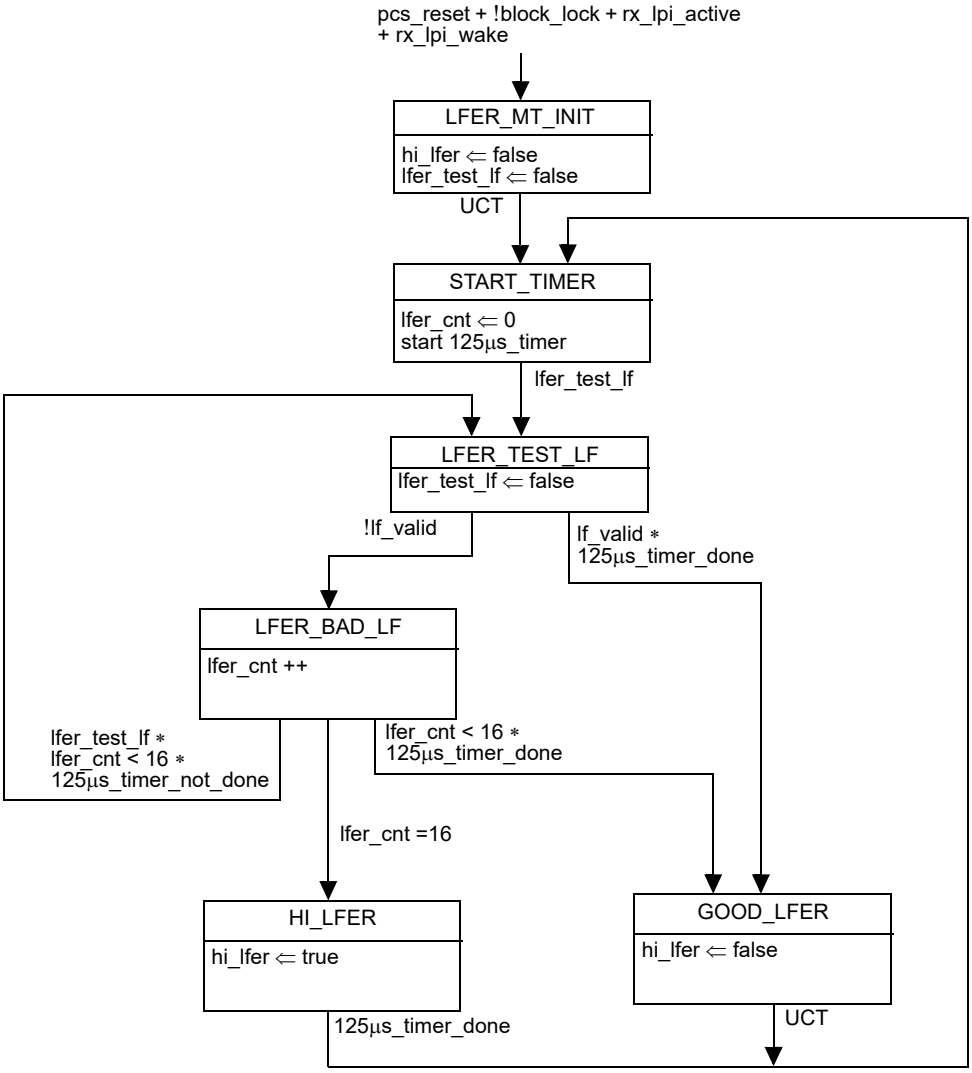

Figure 55–15—LFER monitor state diagram

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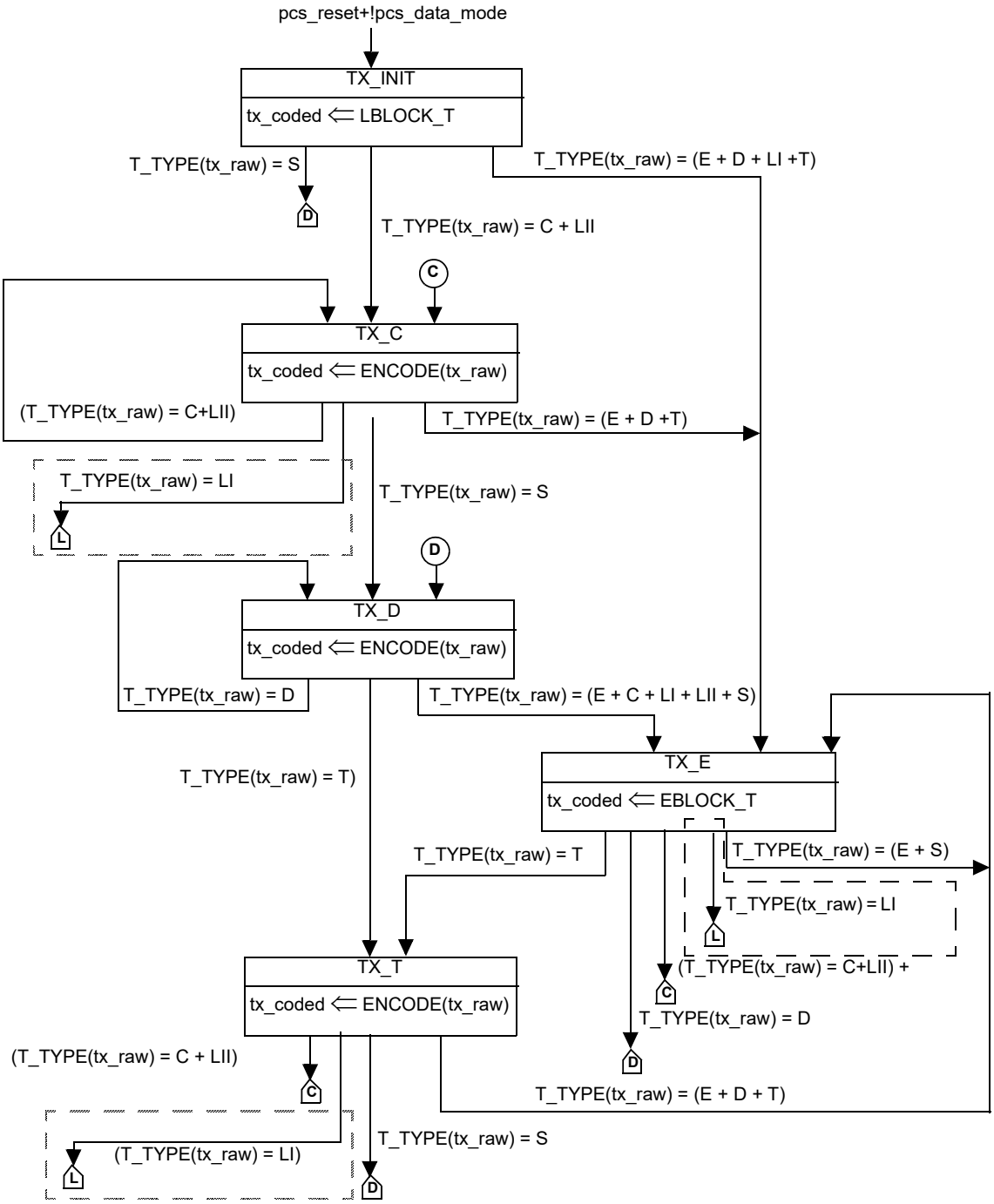

NOTE—Transitions inside dashed boxes are only required for the EEE capability.

Figure 55–16—PCS 64B/65B Transmit state diagram, part a

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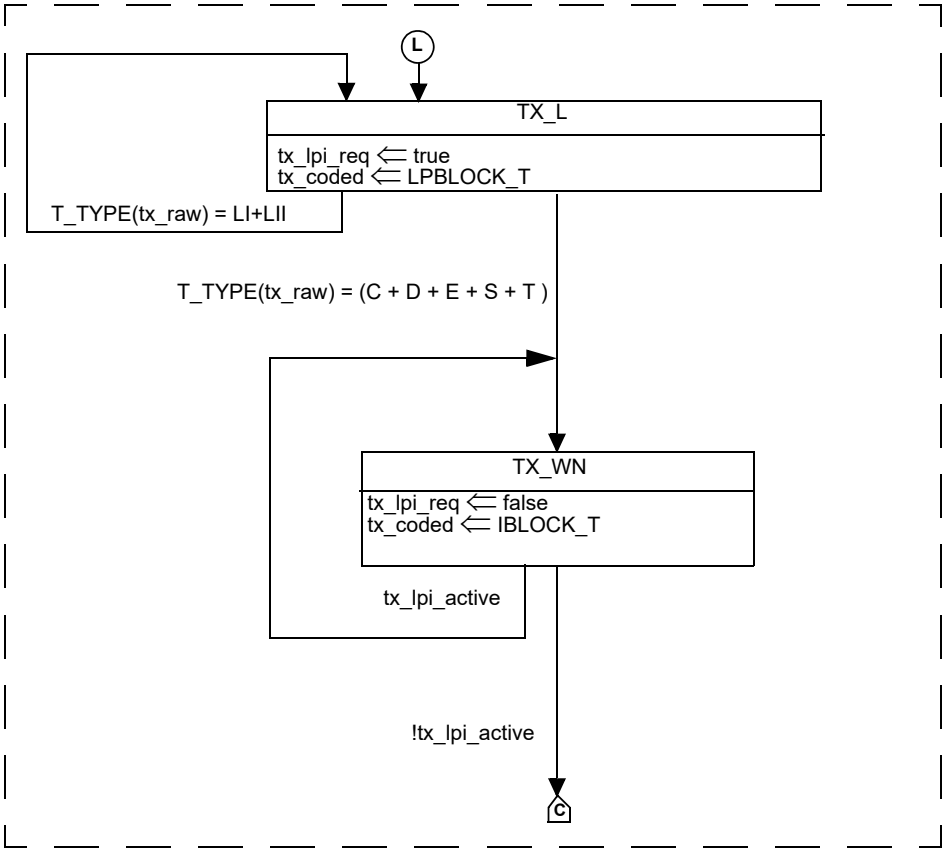

NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 55–17—PCS 64B/65B Transmit state diagram, part b

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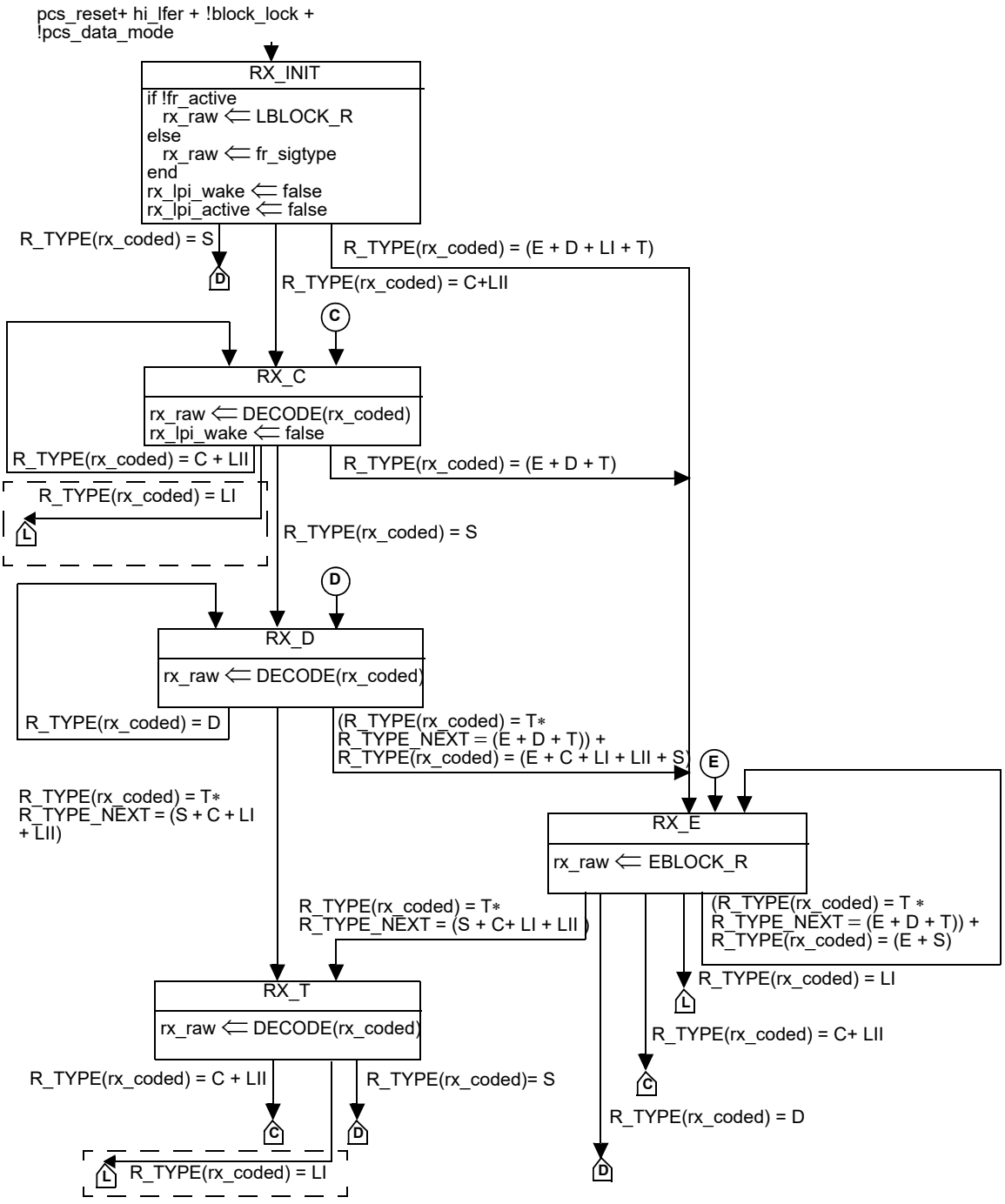

NOTE—Signals and functions shown with dashed lines are only required for the EEE capability.

Figure 55–18—PCS 64B/65B Receive state diagram, part a

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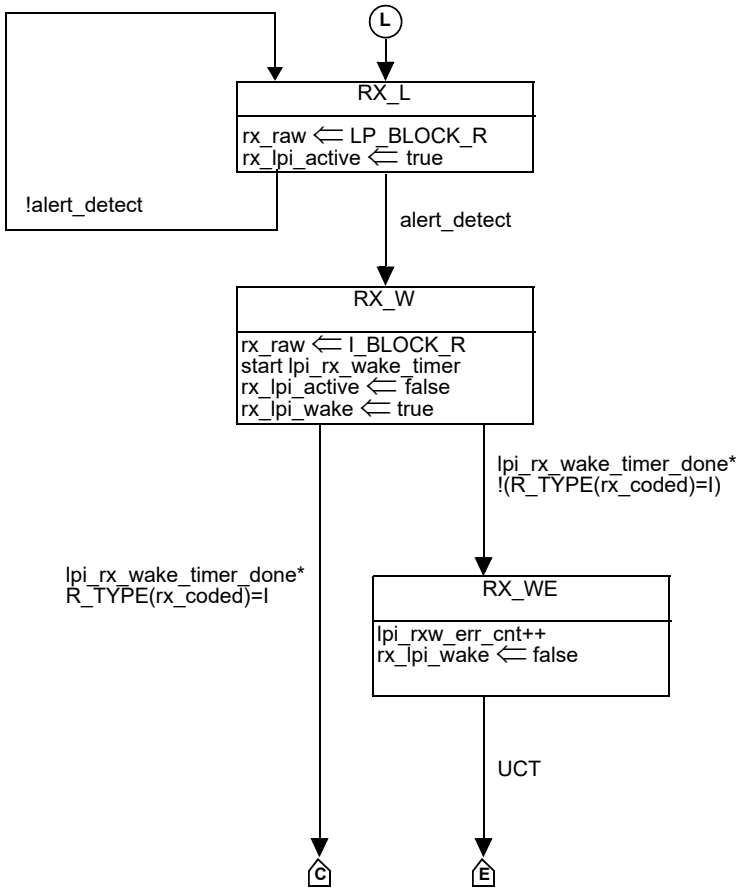

NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 55–19—PCS 64B/65B Receive state diagram, part b

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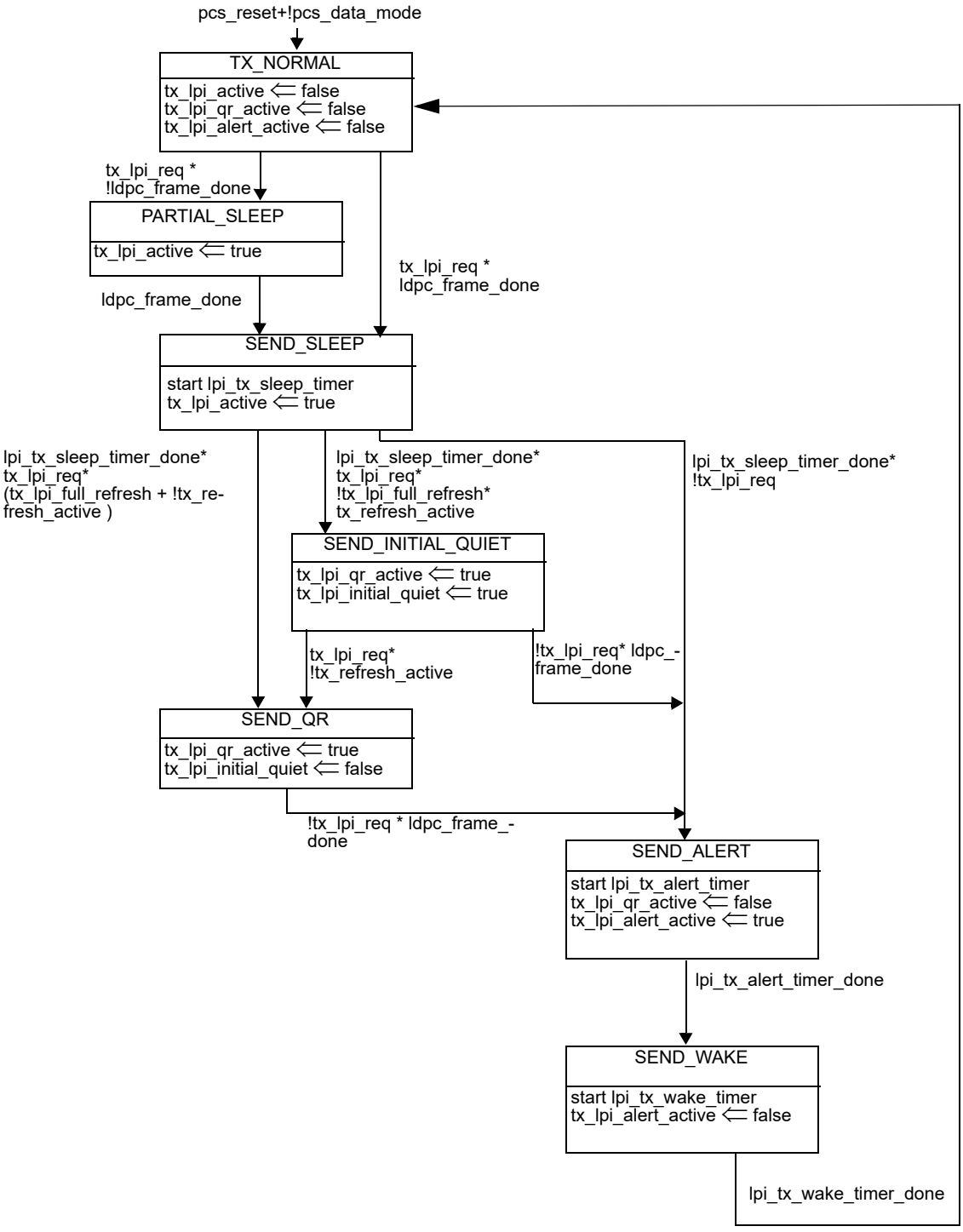

NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 55–20—EEE transmit state diagram

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55.3.7.3 Loopback

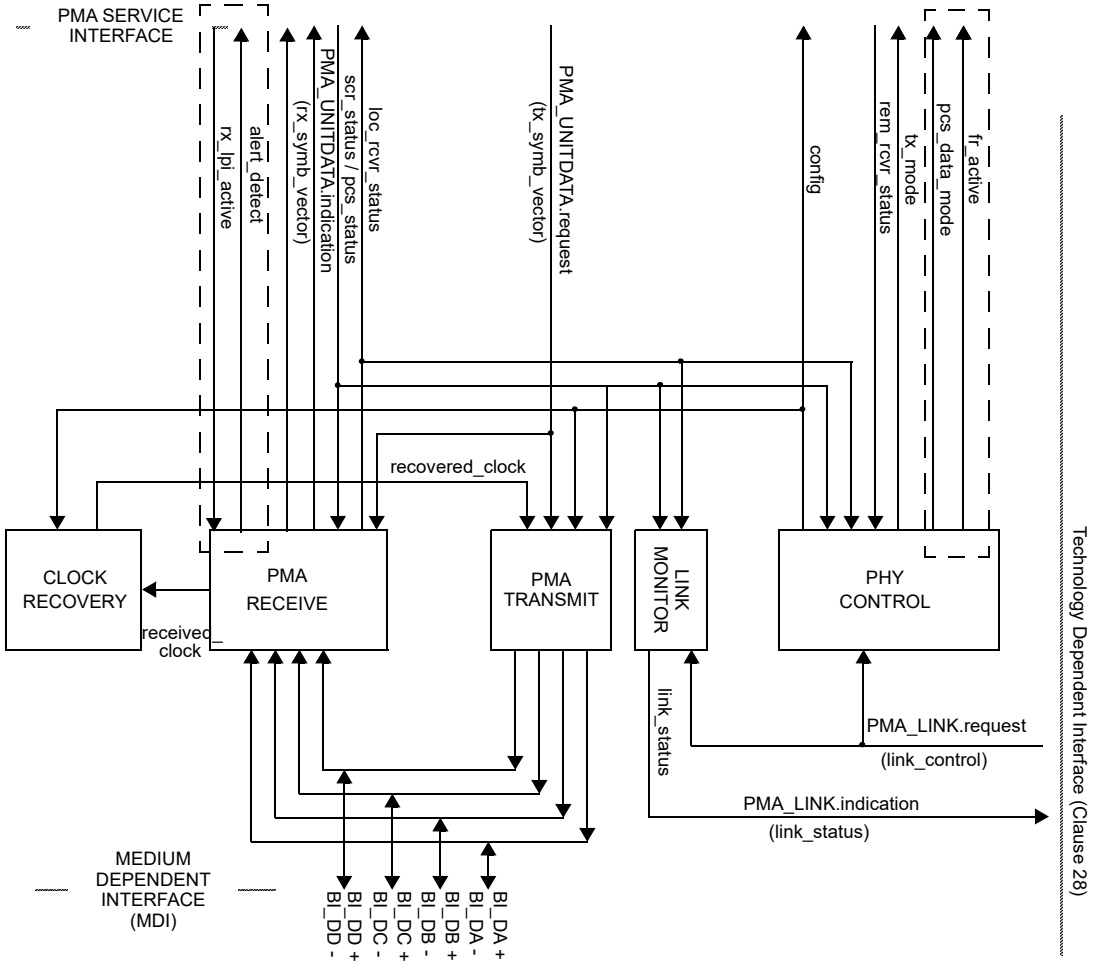
The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14 is set to a one. In this mode, the PCS shall accept data on the transmit path from the XGMII and return it on the receive path to the XGMII. In addition, the PCS shall transmit a continuous stream of 65B-LDPC encoded 4D-PAM16 symbols to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer.

55.4 Physical Medium Attachment (PMA) sublayer

55.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 55.2.2 to the 10GBASE-T baseband medium, specified in 55.7.

The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 55.8.



NOTE 1—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

NOTE 2—pcs_data_mode is required only for the EEE or fast retrain capabilities alert_detect and rx_lpi_active are only required for the EEE capability fr_active is only required for the fast retrain capability

Figure 55–21— PMA reference diagram

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55.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 55–21, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 55–21.

55.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power on (see 55.3.6.2.2)
b) The receipt of a request for reset from the management entity

All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

55.4.2.2 PMA Transmit function

The PMA Transmit function comprises four synchronous transmitters to generate four pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. While send_fail is FALSE and ALERT is not indicated by tx_symb_vector, PMA Transmit shall continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively after processing with the THP, optional transmit filtering, digital to analog conversion (DAC) and subsequent analog filtering. When ALERT is indicated by tx_symb_vector, the alert signal is transmitted as specified in 55.4.2.2.1. When send_fail is TRUE, the link failure signal is transmitted as specified in 55.4.2.2.2. The four transmitters shall be driven by the same transmit clock, TX_TCLK. The signals generated by PMA Transmit shall follow the mathematical description given in 55.4.3.1, and shall comply with the electrical specifications given in 55.5.

When the PMA_CONFIG.indication parameter config is MASTER, for both normal and LPI operation, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 55.5.3.3. The MASTER/SLAVE relationship may include loop timing. If loop timing is implemented and the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 55.4.2.8 while meeting the jitter requirements of 55.5.3.3. If loop timing is not implemented, the SLAVE PHY transmit clocking is identical to the MASTER PHY transmit clocking. An EEE-capable PHY shall operate with loop timing when configured as SLAVE.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

EEE-capable PHYs shall implement a PMA Transmit function that generates the alert signal as defined in 55.4.2.2.1. PHYs that support the fast retrain capability shall implement a PMA Transmit function that generates the link failure signal as defined in 55.4.2.2.2. If ALERT is indicated by tx_symb_vector at the same time as send_fail is TRUE, then link failure signaling is transmitted.

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55.4.2.2.1 Alert signal

PHYs that support the optional EEE capability will transmit the following PAM2 sequence when the PMA_UNITDATA.request parameter is set to ALERT. The alert signal is sent for a total of 4 LDPC frame periods and begins on a LDPC frame boundary. The alert signal is transmitted without THP filtering. The alert signal is transmitted on pair A when the PHY operates as a MASTER. The alert signal is transmitted on pair C when the PHY operates as a SLAVE. All other pairs transmit quiet as described in 55.3.5.

When the PMA_CONFIG.indication(config) is MASTER the alert signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xpr_master =

9 9 -9 -9 -9 -9 -9 -9 9 9 -9 -9 9 9 9 9

9 9 9 9 -9 -9 9 9 9 9 -9 -9 9 9 -9 -9

-9 -9 -9 -9 -9 -9 9 9 -9 -9 -9 -9 -9 -9 9 9

-9 -9 -9 -9 -9 -9 -9 -9 9 9 -9 -9 9 9 -9 -9

-9 -9 9 9 9 9 9 9 9 9 9 9 -9 -9 -9 -9

9 9 -9 -9 -9 -9 9 9 9 9 -9 -9 9 9 -9 -9

-9 -9 -9 -9 -9 -9 -9 -9 9 9 9 9 -9 -9 9 9

9 9 -9 -9 9 9 -9 -9 9 9 9 9 -9 -9 -9 -9

When the PMA_CONFIG.indication(config) is SLAVE the alert signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xpr_slave =

-9 -9 -9 -9 9 9 9 9 -9 -9 9 9 -9 -9 9 9

9 9 -9 -9 9 9 9 9 -9 -9 -9 -9 -9 -9 -9 -9

-9 -9 9 9 -9 -9 9 9 9 9 -9 -9 -9 -9 9 9

-9 -9 -9 -9 9 9 9 9 9 9 9 9 9 9 -9 -9

-9 -9 9 9 -9 -9 9 9 -9 -9 -9 -9 -9 -9 -9 -9

9 9 -9 -9 -9 -9 -9 -9 9 9 -9 -9 -9 -9 -9 -9

-9 -9 9 9 -9 -9 9 9 9 9 -9 -9 9 9 9 9

9 9 9 9 -9 -9 9 9 -9 -9 -9 -9 -9 -9 9 9

The alert signal is followed by a wake signal composed of repeated IDLE characters encoded using the 64B/65B encoding technique. At the start of the wake signal all THP feedback delay lines are initialized with zeros.

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55.4.2.2.2 Link failure signal

PHYs that support the fast retrain capability transmit the link failure signal under the control of the Fast Retrain state diagram. The link failure signal indicates to the link partner that a link failure has been detected and that the link partners should begin the fast retrain procedure.

The link failure signal is sent for 4 LDPC frames and begins on a LDPC frame boundary. The link failure signal is transmitted without THP filtering. The link failure signal is transmitted on pair A when the PHY operates as a MASTER. The link failure signal is transmitted on pair C when the PHY operates as a SLAVE. All other pairs transmit quiet as described in 55.3.5.

When the PMA_CONFIG.indication(config) is MASTER, the link failure signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xfr_master = xpr_master × (−1)

When the PMA_CONFIG.indication(config) is SLAVE the link failure signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xfr_slave = xpr_slave × (−1)

55.4.2.3 PMA transmit disable function

55.4.2.3.1 Global PMA transmit disable function

The Global_PMA_transmit_disable function allows all of the transmitters to be disabled, when either.

a) When a Global_PMA_transmit_disable variable is set to TRUE, this function shall turn off all of the transmitters so that the each transmitter Average Launch Power of the OFF Transmitter is less than –53 dBm.
b) If a PMA_transmit_fault is detected, then the PMA may set the Global_PMA_transmit_disable to TRUE, turning off the transmitter on each pair.

55.4.2.3.2 PMA pair by pair transmit disable function

The PMA_transmit_disable function allows the transmitters on each pair to be selectively disabled.

When a PMA_transmit_disable_N variable is set to TRUE, this function shall turn off the transmitter associated with that variable so that the transmitter Average Launch Power of the OFF Transmitter is less than –53 dBm.

55.4.2.3.3 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 55–5. Mapping of MDIO status variables to PMA status variables is shown in Table 55–6.

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Table 55–5—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	Control register 1	1.0.15	PMA_reset
Global transmit disable	Transmit disable register	1.9.0	Global_PMA_transmit_disable
Transmit disable pair D	Transmit disable register	1.9.4	PMA_transmit_disable_D
Transmit disable pair C	Transmit disable register	1.9.3	PMA_transmit_disable_C
Transmit disable pair B	Transmit disable register	1.9.2	PMA_transmit_disable_B
Transmit disable pair A	Transmit disable register	1.9.1	PMA_transmit_disable_A

Table 55–6—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Fault	Status register 1	1.1.7	PMA_fault
Transmit fault	Status register 2	1.8.11	PMA_transmit_fault
Receive fault	Status register 2	1.8.10	PMA_receive_fault

55.4.2.4 PMA Receive function

The PMA Receive function comprises four independent receivers for pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over receive pairs BI_DA, BI_DB, BI_DC, and BI_DD and to present these sequences to the PCS Receive function. The signals received at the MDI are described mathematically in 55.4.3.2. The PMA translates the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DB into the PMA_UNITDATA.indication parameter rx_symb_vector. The quality of these symbols shall allow LFER of less than 3.2×10^{-9} after LDPC decoding, over a channel meeting the requirements of 55.7. The receiver shall correct for differential delay variations of up to 50 ns across the wire-pairs. The delay skew is removed by computing the relative received delay of the four known transmit patterns described in 55.3.4.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization, echo and crosstalk cancellation. The sequence of code-groups assigned to tx_symb_vector is needed to perform echo and self near-end crosstalk cancellation.

The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, estimation, and LPI functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

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The receiver uses the sequence of symbols during the training sequence to detect and correct for pair swaps and crossovers. The receiver pairs BI_DA, BI_DB, BI_DC, and BI_DD may be connected in any manner described in 55.4.4 to the corresponding transmit pairs. The receiver also detects and corrects for polarity mismatches on any pairs and corrects for differential delay variations across the wire-pairs.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5.

PMA receive functions that support the optional EEE capability shall generate alert_detect when the alert signal is detected at the receiver. The PMA receive function asserts alert_detect after the entire alert signal (3.5 LDPC frame periods of the xpr_master or xpr_slave sequence and 0.5 frames of silence) has been detected. The alert signal is specified in 55.4.2.2.1. The criterion used to generate alert_detect is left to the implementer.

PHYs that support the fast retrain capability shall set link_fail_detect to TRUE when the link failure signal is reliably detected at the receiver. The PMA receive function asserts link_fail_detect after the entire link failure signal (3.5 LDPC frame periods of the xfr_master or xfr_slave sequence and 0.5 frames of silence) has been detected. The link failure signal is specified in 55.4.2.2.2. The criterion used to generate link_fail_detect is left to the implementer. It is highly recommended that the generation of link_fail_detect is qualified with repeated errored frames at the LDPC decoder output.

55.4.2.5 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 55–28.

During PMA training (includes PMA_Training_Init_M, PMA_Training_Init_S, PMA_PBO_Exch, PMA_Coeff_Exch, and PMA_Fine_Adjust states in Figure 55–28), PHY Control information is exchanged between link partners with a 16 octet InfoField, which is XOR'ed with the last 128 bits of the PMA 16384 PAM2 frame on pair A (see Figure 55–13). The InfoField is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions to timer expiration times, transition counter values, etc. described in Figure 55–28, Figure 55–29, and Figure 55–30.

The 16 octet InfoField shall include the fields in 55.4.2.5.2 through 55.4.2.5.13, also shown in the overview Figure 55–22, and the more detailed Figure 55–23, Figure 55–24, and Figure 55–25.

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Message Field Dependent	Message Field Dependent	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	4 octets	2 octets

Figure 55–22—InfoField format

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Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Reser-ved	Transition Counter	Reser-ved	Vendor Specific	CRC16
4 octets	3 octets	1 octet	4 bits	2 bits	10 bits	2 octets	2 octets	2 octets

Figure 55–23—InfoField transition counter format

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Coefficient Exchange	Coefficient Field	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	4 octets	2 octets

Figure 55–24—InfoField coefficient exchange format

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Reserved	Reserved	Vendor Specific	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	2 octets	2 octets	2 octets

Figure 55–25—InfoField not transition counter and not coefficient exchange format

55.4.2.5.1 Infofield notation

For all the InfoField notation below, Reserved<bit location> represents any unused values and shall be set to zero and ignored by the link partner. For all PBO InfoField values below, the PBO<6:4> are unsigned 3-bit values 000, 001, 010, 011, 100, 101, 110, and 111 shall indicate power backoffs of 0 dB, 2 dB, 4 dB, 6 dB, 8 dB, 10 dB, 12 dB, and 14 dB respectively. The InfoField is transmitted following the notation described in 55.3.2.2.3 where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

55.4.2.5.2 Start of Frame Delimiter

The start of Frame Delimiter consist of 4 octets [Oct1<7:0>, Oct2<7:0>, Oct3<7:0>, Oct4<7:0>] and shall use the hexadecimal value 0xBBA70000. 0xBB corresponds to Oct1<7:0> and so forth.

55.4.2.5.3 Current transmitter settings

Current transmitter setting (1 octet). Represented by the octet Oct5{Valid<7>, PBO<6:4>, Reserved<3:0>} and shown in Figure 55–26. Used to announce the current fixed PBO setting during PMA_Training_Init_M, PMA_Training_Init_S and PMA_PBO_Exch, and the current programmable PBO setting during PMA_Coeff_Exch. For every other state this octet is set to zero and ignored by the link partner. The bit Valid shall be set to one if the corresponding octet information is valid and shall be set to zero if it the octet information is not valid. If Valid is set to zero, the octet is ignored by the link partner.

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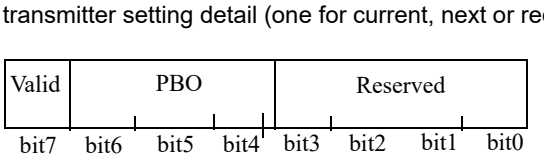

Figure 55–26—InfoField transmitter setting format

55.4.2.5.4 Next transmitter settings

Next transmitter setting (1 octet). Represented by the octet Oct6{Valid<7>, PBO<6:4>, Reserved<3:0>} and shown in Figure 55–26. Used to announce the next programmable PBO setting during PMA_PBO_Exch that takes effect upon entering PMA_Coeff_Exch state. For every other state, this octet is set to zero and ignored by the link partner. The bit Valid shall be set to one if the corresponding octet information is valid and shall be set to zero if it the octet information is not valid. If Valid is set to zero, the octet is ignored by the link partner.

55.4.2.5.5 Requested transmitter settings

Requested remote transmitter setting (1 octet). Represented by the octet Oct7{Valid<7>, PBO<6:4>, Reserved<3:0>} and shown in Figure 55–26. Used to request the remote transmitter programmable PBO setting during PMA_PBO_Exch that takes effect upon entering PMA_Coeff_Exch state. For every other state, this octet is set to zero and ignored by the link partner. The bit Valid shall be set to one if the corresponding octet information is valid and shall be set to zero if it the octet information is not valid. If Valid is set to zero, the octet is ignored by the link partner.

55.4.2.5.6 Message Field

Message Field (1 octet). For the MASTER, this field is represented by the octet Oct8{PMA_state<7:6>, loc_rcvr_status<5>, en_slave_tx<4>, trans_to_Coeff_Exch<3>, Coeff_exchange<2>, trans_to_Fine_Adjust<1>, trans_to_PCS_Test<0>}. For the SLAVE, this field is represented by the octet Oct8{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, trans_to_Coeff_Exch<3>, Coeff_exchange<2>, trans_to_Fine_Adjust <1>, trans_to_PCS_Test<0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6>=00 indicates PMA_Training_Init_M or PMA_Training_Init_S, PMA_state<7:6>=01 indicates PMA_PBO_Exch, PMA_state<7:6>=10 indicates PMA_Coeff_Exch, and PMA_state<7:6>=11 indicates PMA_Fine_Adjust.

All possible Message Field settings are listed in Table 55–7 for the MASTER and Table 55–8 for the SLAVE. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 55–7 for the MASTER and the first row of Table 55–8 for the SLAVE. Moreover, for a given Message Field setting, the following Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status=OK the InfoField variable is set to loc_rcvr_status<5>=1 and set to 0 otherwise.

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Table 55–7—InfoField message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_ status	en_slave_tx	trans_to_ Coeff_Exch	Coeff_ exchange	trans_to_ Fine_Adjust	trans_to_ PCS_test
00	0	0	0	0	0	0
00	0	1	0	0	0	0
01	0	1	0	0	0	0
01	0	1	1	0	0	0
10	0	1	0	0	0	0
10	0	1	0	1	0	0
10	0	1	0	0	0	0
10	0	1	0	0	1	0
11	0/1	1	0	0	0	0
11	1	1	0	0	0	1

Table 55–8—InfoField message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_ status	timing_lock _OK	trans_to_ Coeff_Exch	Coeff_ exchange	trans_to_ Fine_Adjust	trans_to_ PCS_test
00	0	0	0	0	0	0
00	0	0/1	0	0	0	0
01	0	1	0	0	0	0
01	0	1	1	0	0	0
10	0	0/1	0	0	0	0
10	0	1	0	1	0	0
10	0	1	0	0	0	0
10	0	1	0	0	1	0
11	0	0/1	0	0	0	0
11	0/1	1	0	0	0	0
11	1	1	0	0	0	1

55.4.2.5.7 SNR_margin

SNR_margin (4 bits). Represented by the half octet Oct9<7:4>, which reports received decision point SNR margin in 1/2 dB steps. SNR_margin is relative to the SNR required for reception of LDPC-coded DSQ128 at an LDPC frame error ratio of less than 3.2×10^{-9}. The SNR_margin<7:4> 4-bit values, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110 shall indicate the decision point SNR margin

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values of –1.5, –1, –0.5, 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5 dB respectively. The value 0001 shall indicate a margin of –2 dB or less, and the value 1111 shall indicate 5 dB or more. Finally the value 0000 shall indicate that the SNR margin value is unknown.

55.4.2.5.8 Transition counter

Transition counter (10 bits). Represented by the 1.25 octets [Oct9<1:0>, Oct10<7:0>]. When configured as Transition counter (Coeff_exchange<2>=0 and a transition is announced to PMA_Coeff_Exch, PMA_Fine_Adjust or PCS_Test) this field is used as a 10 bit counter that counts the number of remaining frames until the next transition (PMA_Coeff_Exch, PMA_Fine_Adjust, PCS_Test).

55.4.2.5.9 Coefficient exchange handshake

Coefficient exchange handshake (12 bits). Represented by the 1.5 octets [Oct9<3:0>, Oct10<7:0>]. If Coeff_exchange<2>=1, this field is configured as a Coefficient exchange handshake and is used as a handshake control channel during programmable THP coefficient exchange. The details of the coefficient exchange are described in 55.4.2.5.14.

55.4.2.5.10 Reserved Fields

All InfoField fields denoted Reserved in Figure 55–23, Figure 55–24, and Figure 55–25 are reserved for future use. This includes octets Oct11 and Oct12 when Coeff_exchange<2>=0, Oct9<3:2> when transition counter is announced and [Oct9<3:0>, Oct10<7:0>] when no transition is announced and no coefficients are exchanged.

55.4.2.5.11 Vendor-specific field

If Coeff_exchange<2>=0 octets, Oct13 and Oct14 are vendor-specific fields. If during Auto-Negotiation both transceivers agree on the use of the two vendor-specific octets, they may be used as a PHY communication channel; otherwise they are set to zero and ignored by the link partner. Represented by the 2 octets [Oct13<7:0>, Oct14<7:0>].

55.4.2.5.12 Coefficient Field

Coefficient Field (4 octets). Represented by the octets [Oct11<7:0>, Oct12<7:0>, Oct13<7:0>, Oct14<7:0>]. When Coeff_exchange<2>=1, this field is used to exchange programmable THP coefficients. It transmits four 8-bit THP coefficients out of the total of 64 (16 coefficients over each of the 4 pairs). The order is pair A, coefficients 0:3, followed by coefficients 4:7, followed by 8:11 and 12:15. For all cases the first coefficient (indices 0, 4, 8 and 12) is mapped to Oct11, the second coefficient (indices 1, 5, 9, 13) is mapped to Oct12 and so on. The same coefficient order is followed to transmit the coefficients for pair B, followed by pair C, and finally pair D. The details of the coefficient exchange are described in 55.4.2.5.14.

55.4.2.5.13 CRC16

CRC16 (2 octets). Shall implement the CRC16 polynomial $(x+1)(x^{15}+x+1)$ of the previous 10 octets, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, Oct10<7:0>, Oct11<7:0>, Oct12<7:0>, Oct13<7:0>, and Oct14<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 55–27. In Figure 55–27 the 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards Oct5 through Oct14 are used to compute the CRC16 with the switch connected, which is setting CRCgen in Figure 55–27. After all the 10 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

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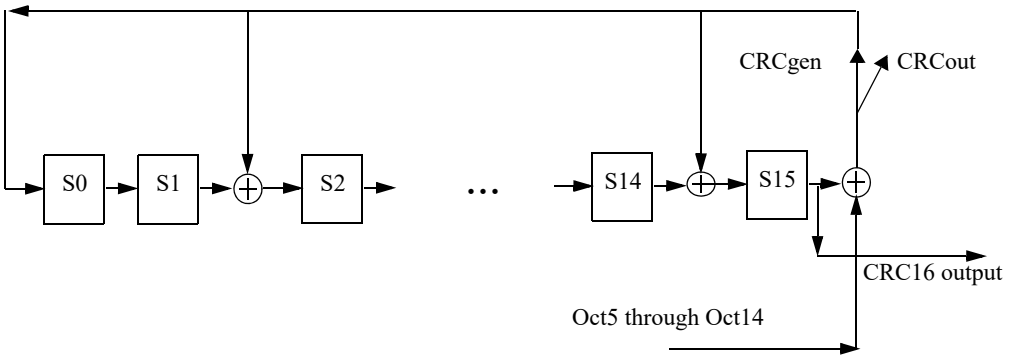

Figure 55–27—CRC16

55.4.2.5.14 Startup sequence

The startup sequence shall comply with the state diagram description given in Figure 55–28 and the transition counter state diagrams Figure 55–29 and Figure 55–30.

During Auto-Negotiation, PHY Control is in the DISABLE_10GBASE-T_TRANSMITTER state and the transmitters are disabled. During normal training, prior to enabling the transmitter, the THP coefficients are set to zero.

When the Auto-Negotiation process asserts link_control=ENABLE, PHY Control enters the INIT_MAXWAIT_TIMER state. Upon entering this state, the maxwait_timer is started and PHY Control enters the SILENT state, which starts the minwait_timer and forces transmission of zeros by setting tx_mode=SEND_Z.

In MASTER mode, after expiration of the minwait_timer, PHY Control transitions to the PMA_Training_Init_M state.

Upon entering the PMA_Training_Init_M and PMA_Training_Init_S states, the PHY Control forces transmission into the training mode by asserting tx_mode=SEND_T, which includes the transmission of InfoFields.

Upon entering state PMA_Training_Init_M, the MASTER starts transmission with a fixed transmit power level, PBO=4 (corresponding to a power backoff of 8 dB). The PBO variable is communicated to the link partner via the current transmitter octet of the InfoField.

Initially the MASTER is not ready for the SLAVE to respond and sets en_slave_tx=0, which is communicated to the link partner via the InfoField. After the MASTER has sufficiently converged the necessary circuitry, the MASTER sets en_slave_tx=1 to allow the SLAVE to transition to PMA_Training_Init_S.

In SLAVE mode, PHY Control transitions to the PMA_Training_Init_S state only after the SLAVE PHY acquires timing, converges its equalizers, acquires its descrambler state and sets loc_SNR_margin=OK. The SLAVE shall respond using the fixed PBO transmit power level, PBO=4 (corresponding to a power backoff of 8 dB). For PHYs with the EEE capability, further requirements for this transition are described in 55.3.5.1.

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While in states PMA_Training_Init_S, PMA_PBO_Exch, or PMA_Coeff_Exch, whenever a SLAVE operating in loop timing mode loses the MASTER timing reference (for example, after transmit power level transitions) it sets timing_lock_OK=0, which is communicated to the link partner via the InfoField. Otherwise, timing_lock_OK is set to one.

In MASTER mode, PHY Control enters the PMA_PBO_Exch state after loc_SNR_margin=OK and in SLAVE mode PHY Control enters the PMA_PBO_Exch state after the loc_SNR_margin=OK and minwait_timer expires. In the PMA_PBO_Exch state, after the MASTER has computed the final desired programmable PBO level, it shall request a PBO change using the requested transmitter setting in the InfoField (octet 7). In SLAVE mode, after the MASTER has requested the desired PBO level, the SLAVE shall request a desired PBO level that is within two levels (within 4 dB) of the requested MASTER PBO level.

Following PBO exchange for both transceivers, each PHY shall announce the next PBO setting using the next transmitter setting (octet 6). Afterwards, each PHY announces a transition to the PMA_Coeff_Exch state using the trans_to_Coeff_Exch=1 and transition_count as described in 55.4.5.1. MASTER initiates the transition to PMA_Coeff_Exch count with the trans_to_Coeff_Exch=1 flag and a transition counter value of 2^9 (10 ms). The SLAVE responds prior to the MASTER transition counter reaching 2^6 (1 ms) by setting trans_to_Coeff_Exch=1 flag and a transition counter value matching the MASTER. The PMA frame after each transceiver transition_count reaches zero, the PHYs shall enter the PMA_Coeff_Exch state and enable the requested PBO. Therefore, both PHYs will enter the PMA_Coeff_Exch state within one PMA frame.

While both MASTER and SLAVE are in state PMA_Coeff_Exch, when either end has computed the programmable THP settings, the programmable THP coefficient exchange process can begin, using the 1.5 octet Coefficient exchange handshake and the 4 octet Coefficient Field as follows:

a) During PMA_Coeff_Exch each PHY begins a coefficient exchange by setting the Coeff_Exchange flag to 1 in the Message Field.
b) During coefficient exchange, the transition counter bits are used as the Coefficient Exchange Handshake
    1) Oct9{Reserved<3:0>}: unused
    2) Coefficient Pair Received, Oct10<7:6>: 01 for local transmitter pair A, 10 for B, 11 for C and 00 for D (default). This is the handshake to tell the remote unit the last coefficients received.
    3) Coefficient Group Received, Oct10<5:4>: 01 for coefficients 0:3, 10 for 4:7, 11 for 8:11 and 00 for 12:15 (default). This is the handshake to tell the remote unit the last coefficients received.
    4) Coefficient Pair Sent, Oct10<3:2>: 01 for remote transmitter pair A, 10 for B, 11 for C and 00 for D (default). This is the handshake to tell the remote unit the current coefficients being sent.
    5) Coefficient Group Sent, Oct10<1:0>: 01 for 0:3, 10 for 4:7, 11 for 8:11 and 00 for 12:15 (default). This is the handshake to tell the remote unit the current coefficients being sent.
c) The Coefficient Field is used to send 4 8-bit coefficients in each frame designated by the Coefficient Pair Sent and Coefficient Group Sent bits. The coefficient format is:
    1) 8 bits per coefficient. Use one octet per coefficient in twos complement notation
    2) Coefficient range is –2.0 to 1.984375 in steps of 0.015625
    3) The sign of the coefficients shall be consistent with Equation (55–4)
d) Each PHY begins the exchange by sending pair A coefficients 0:3 with Coefficient Pair Sent=01 and Coefficient Group Sent=01.
e) The remote unit acknowledges by setting Coefficient Pair Received=01 and Coefficient Group Received=01.
f) Following each acknowledgement, the PHY increments through the Coefficient Group and then Coefficient Pair settings until Coefficient Pair Sent=00 and Coefficient Group Sent=00 and Coefficient Pair Received=00 and Coefficient Group Received=00. At this time, coefficient exchange is done and both PHYs set Coeff_Exchange=0.

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Following coefficient exchange for both transceivers, each PHY announces a transition to the PMA_Fine_Adjust state (trans_to_Fine_Adjust=1) and starts the transition_count as described in 55.4.5.1. During the first PMA frame after the transition_count reaches zero, the PHYs enter the PMA_Fine_Adjust state and enable the THP precoders with the requested coefficients. At the closure of the THP feedback loop, the initial state of the THP feedback filters shall be the last 16 symbols from the state PMA_Coeff_Exch.

The THP coefficients and PBO setting may not be changed during PMA_Fine_Adjust. The final convergence of the adaptive filter parameters is completed in the PMA_Fine_Adjust state.

After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter InfoField value loc_rcvr_status. The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr status. When the condition loc_rcvr_status=OK and rem_rcvr_status=OK is satisfied, each PHY announces a transition to the PCS_Test state (trans_to_PCS_Test=1) and start the transition counter as described in 55.4.5.1. For PHYs with the EEE capability, further requirements for this transition are described in 55.3.5.1.

The normal mode of operation corresponds to the PCS_Data state, where PHY Control asserts tx_mode=SEND_N and transmission of data over the link can take place.

PHY Control may force the transmit scrambler state to be initialized to an arbitrary value by requesting the execution of the PCS Reset function defined in 55.3.2.1.

The operation of the maxwait_timer requires that the PHY complete the startup sequence from state SILENT to PMA_Fine_Adjust in the PHY Control state diagram (Figure 55–28) in less than 2000 ms to avoid link_status being changed to FAIL by the Link Monitor state diagram (Figure 55–31). To ensure interoperability the timing in Table 55–9 should be observed.

After reaching the PCS_Data state PHYs with the EEE capability can transition to the LPI receive mode under the control of the link partner and to the LPI transmit mode under control of the local LPI client.

Table 55–9—Recommended startup sequence timing

Master	Recommended maximum time (ms)	Recommended average time (ms)	Slave
SILENT plus (PMA_Training_Init_M state AND en_slave_tx = 0)	350	315	SILENT
(PMA_Training_Init_M state AND en_slave_tx = 1) plus PMA_PBO_Exch state	480	432	PMA_Training_Init_S state plus PMA_PBO_Exch state
PMA_Coeff_Exch state	100	90	PMA_Coeff_Exch state with timing_lock_OK=0
	520	468	Total for PMA Coeff Exch state
PMA_Fine_Adjust state	650	585	PMA_Fine_Adjust state
Total	2000	1800	

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55.4.2.5.15 Fast retrain function

PHYs that support the fast retrain capability shall implement the fast retrain state diagram shown in Figure 55–33. PHYs may request a fast retrain by setting the variable loc_fr_req to TRUE. This causes the transmission of an easily-detected link failure signal specified in 55.4.2.2.2. After completing the link failure signal the PHY shall transition to the PMA_Coeff_Exch state, keep its THP turned on with its previously exchanged coefficients, and send PAM2 signaling within a time period equivalent to 9 LDPC frame periods.

After the detection of the link failure signal, a PHY shall transition to the PMA_Coeff_Exch state and respond with PAM2 signaling within a time period equivalent to 9 LDPC frame periods after receiving the link failure signal.

The PAM2 symbols are generated using the PMA sidestream scrambler polynomials shown in Figure 55–13. The training sequence without periodic re-initialization described in 55.3.4 shall be used during fast retraining, with the scramblers free-running from PCS Reset. If scrambler re-initialization is used for normal training, it shall be disabled and the scramblers shall begin free-running when the PHY Control state diagram enters the PCS_Test state and the variable fr_active is FALSE.

Note that reliable traffic on the transmitter may be interrupted when the local receiver requests a fast retrain.

Following the link failure signal, the two link partners transition back to the PMA_Coeff_Exch state and follow the training procedure described in 55.4.2.5.14, with the exception that the initial infofield countdown values are reduced as indicated in Figure 55–29 and Figure 55–30.

To ensure interoperability the training times in Table 55–10 should be observed during the fast retrain.

Table 55–10—Recommended fast retrain sequence timing

State	Recommended maximum time (ms)
PMA_Coeff_Exch state	20
PMA_Fine_Adjust state	10

55.4.2.6 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel typically causes the PMA's clients to suspend normal operation.

The Link Monitor function shall comply with the state diagram of Figure 55–31.

Upon power on, reset, or release from power down, the Auto-Negotiation algorithm sets link_control=SCAN_FOR_CARRIER and, during this period, sends fast link pulses to signal its presence to a remote station. If the presence of a remote station is sensed through reception of fast link pulses, the Auto-Negotiation algorithm sets link_control=DISABLE and exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. If the presence of a remote 10GBASE-T station is established, the Auto-Negotiation algorithm permits full operation by setting link_control=ENABLE. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

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55.4.2.7 Refresh Monitor function

The Refresh monitor is required for PHYs that support the EEE capability. The Refresh monitor operates when the PHY is in the LPI receive mode. The Refresh monitor shall comply with the state diagram of Figure 55–32. The function forces a link retrain if a refresh signal is not reliably detected within a moving time window equivalent to 50 complete LPI cycles (nominally equal to 8.192 ms), when the PHY is in the lower power receive mode.

55.4.2.8 Clock Recovery function

The Clock Recovery function couples to all four receive pairs. It may provide independent clock phases for sampling the signals on each of the four pairs.

The Clock Recovery function shall provide clocks suitable for signal sampling on each line so that the LDPC FER indicated in 55.4.2.4 is achieved. The received clock signal should be stable and ready for use when training has been completed (loc_rcvr_status=OK). The received clock signal is supplied to the PMA Transmit function by received_clock.

55.4.3 MDI

Communication through the MDI is summarized in 55.4.3.1 and 55.4.3.2.

55.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA on the four pairs BI_DA, BI_DB, BI_DC, and BI_DD are denoted by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively. The modulation scheme used over each pair is PAM16. PMA Transmit generates a pulse-amplitude modulated signal on each pair in the following form:

$$x_n = M(a_n - \sum_{k=1}^{16} x_{n-k}c_k) = a_n + 32m_n - \sum_{k=1}^{16} x_{n-k}c_k \quad (55\text{–}4)$$

$$s(t) = \sum_{n=0}^{\infty} x_n h_T(t - nT) \quad (55\text{–}5)$$

In Equation (55–4), a_n is the PAM16 modulation symbol from the set {–15, –13, –11, –9, –7, –5, –3, –1, 1, 3, 5, 7, 9, 11, 13, 15} to be transmitted at time nT. Each of the 16 THP coefficients c_1, c_2,..., c_{16} per wire pair is represented in two's complement form by 8 bits described in 55.4.2.5. The nonlinear THP operation given by $M(\alpha) = (\alpha + 16) mod 32 - 16$ corresponds to changing the modulation symbol a_n to an augmented modulation symbol $\tilde{a}_n = a_n + 32m_n$ with the integer m_n chosen such that the THP output lies in the interval $-16 \le x_n < 16$. Equation (55–5)describes the convolution of the THP output signals with the transmitter symbol response $h_T(t)$ to obtain the transmit signal $s(t)$ at the MDI. The values of the programmable THP coefficients are exchanged in the InfoField during PMA_Coeff_Exch. The THP filter coefficients shall be fixed after startup.

The nominal power (denoted Ptx) and the symbol response of the PMA transmitted signal $s(t)$, shall comply with the electrical specifications given in 55.5. When the link segment does not experience the maximum insertion loss (IL), each transceiver indicates to the link partner that the link partner PMA Transmit signal shall be reduced in increments of 2 dB. The minimum power backoff level requested shall comply with the power backoff schedule in Table 55–11. If a given receiver has sufficient decision point SNR margin, it may choose to request from the link partner larger power backoff (up to 14 dB) than shown in Table 55–11. Additionally, the Slave shall select a PBO level as described in the PMA_PBO_Exch state of 55.4.2.5.14. The PMA Transmit shall be capable of eight power backoff settings in approximately 2 dB

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steps. The difference between each consecutive power setting shall be 2 ± 0.25 dB, and each step shall be centered at 2 × n dB (n = 0 to 7) reduction from nominal, with a maximum error of ± 1 dB.

The received signal power at the MDI, P (dBm), in Table 55–11, should be the estimate of the average received power across all four pairs from the remote transmitter when the link partner PMA Transmit is at nominal power (after accounting for local transmitter power). If the remote transmitter is not at nominal power during the measurement, the estimate of the received power should be incremented by the amount of power backoff of the link partner transmitter during the measurement. Nominal power refers to the transmit power without any power backoff and is specified in 55.5.3.4. The estimate of the received signal power is stored in registers 1.141 to 1.144 as described in 45.2.1. The values in the length, L (m), column in Table 55–11 are for reference only (not required for power backoff evaluation) and have been computed using the scaled insertion loss equation in 55.7.

Table 55–11—Power backoff schedule

Received signal power at MDI, P (dBm)	Length L(m) (reference)	Minimum power backoff (dB)
$-1.1 < P$	$0 \le L < 35$	10
$-2.3 < P \le -1.1$	$35 \le L < 45$	8
$-3.3 < P \le -2.3$	$45 \le L < 55$	6
$-4.2 < P \le -3.3$	$55 \le L < 65$	4
$-5.0 < P \le -4.2$	$65 \le L < 75$	2
$P \le -5.0$	$75 \le L$	0

55.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise as follows:

$$r(t) = \sum_{n=0}^{\infty} \tilde{a}_n h_R(t - nT) + w(t) \quad (55–6)$$

In Equation (55–6), $\tilde{a}_n$ are the augmented PAM16 modulation symbols described in 55.4.3.1, $h_R(t)$ denotes the symbol response of the overall channel from the THP precoder to the MDI at the receiver and $w(t)$ represents the contribution of various noise sources including uncancelled crosstalk. The four signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD are processed within the PMA Receive function to yield the received symbols rx_symb_vector.

55.4.4 Automatic MDI/MDI-X configuration

Automatic MDI/MDI-X configuration is intended to eliminate the need for crossover cables between similar devices. Automatic MDI/MDI-X configuration is required for 10GBASE-T devices and shall comply with 40.4.4.1 and 40.4.4.2.

Having established MDI/MDI-X configuration, the receiver shall detect and correct for several configurations of pair swaps and crossovers and arbitrary polarity swaps. The receiver pairs BI_DA, BI_DB, BI_DC, and BI_DD might be connected to the corresponding transmit pairs in any of the following ways with arbitrary polarity:

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a) No crossover
b) A/B crossover only
c) C/D crossover only
d) A/B crossover and C/D crossover

For EEE-capable PHYs, the MDI/MDIX function configuration shall apply to refresh and alert signaling. For PHYs with the fast retrain capability, the MDI/MDIX function configuration shall apply to link failure signaling.

55.4.5 State variables

55.4.5.1 State diagram variables

coeff_exchange_done
: This variable reports that both transceivers have received the corresponding coefficients from the link partner.
Values: TRUE: The coefficient exchange has completed.
FALSE: The coefficient exchange has not completed.

config
: The PMA shall generate this variable continuously and pass it to the PCS via the PMA_CONFIG.indication primitive.
Values: MASTER or SLAVE

link_control
: The link_control parameter generated by Auto-Negotiation and passed to the PMA via the PMA_LINK.request primitive (see 55.2.1.1).

link_status
: The link_status parameter set by PMA Link Monitor state diagram and communicated through the PMA_LINK.indication primitive.
Values: OK or FAIL

loc_rcvr_status
: Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY.
Values: OK: The receive link for the local PHY is operating reliably.
NOT_OK: Operation of the receive link for the local PHY is unreliable.

loc_SNR_margin
: This variable reports whether the local device has sufficient SNR margin to continue to the next state. The criterion for setting the parameter loc_SNR_margin is left to the implementer.
Values: OK: The local device has sufficient SNR margin.
NOT_OK: The local device does not have sufficient SNR margin.

master_transition_counter
: This variable reports the current value of the MASTER's transition counter reported in the InfoField defined in 55.4.2.5.
Values: 0 to 2^9

MessageField_IF
: This variable reports that a receiver has successfully received and decoded the InfoField from the remote device. This variable takes on the value contained in the Message Field. If the Message Field cannot be decoded or no explicit action is outstanding the value

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Null is returned.
Values: trans_to_Coeff_Exch, trans_to_Fine_Adjust, trans_to_PCS_Test or Null

PBO

PBO is a variable that can take any integer value from 0 to 7 and indicates the power backoff level. Denoting Ptx as the maximum nominal power, the PBO values are:
Values: 0, 1, 2, 3, 4, 5, 6, 7, which correspond to transmit power levels of *Ptx*, *Ptx*–2 dB, *Ptx*–4 dB, *Ptx*–6 dB, *Ptx*–8 dB, *Ptx*–10 dB, *Ptx*–12 dB, *Ptx*–14 dB respectively

PBO_next

PBO_next is a variable that can take any integer value from 0 to 7 and indicates the next power backoff level to be used at the local transmitter. The value is taken from the fixed set of values during PMA_Training_Init_M and PMA_Training_Init_S as described in 55.4.2.5. The value is taken from the decoded value of the link partner InfoField during PMA_PBO_Exch
Values: 0, 1, 2, 3, 4, 5, 6, 7, which correspond to transmit power levels of *Ptx*, *Ptx*–2 dB, *Ptx*–4 dB, *Ptx*–6 dB, *Ptx*–8 dB, *Ptx*–10 dB, *Ptx*–12 dB, *Ptx*–14 dB respectively

PBO_tx

PBO_tx is a variable that can take any integer value from 0 to 7 and indicates the power backoff level currently used at the local transmitter.
Values: 0, 1, 2, 3, 4, 5, 6, 7, which correspond to transmit power levels of *Ptx*, *Ptx*–2 dB, *Ptx*–4 dB, *Ptx*–6 dB, *Ptx*–8 dB, *Ptx*–10 dB, *Ptx*–12 dB, *Ptx*–14 dB respectively

PBO_exchange_done

This variable reports that both transceivers have received the corresponding PBO levels from the link partner.
Values: TRUE: The PBO exchange has completed.
FALSE: The PBO exchange has not completed.

pma_reset

Allows reset of the PHY Control and Link Monitor state diagrams.
Values: ON or OFF

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not.
Values: OK: The receive link for the remote PHY is operating reliably.
NOT_OK: Reliable operation of the receive link for the remote PHY is not detected.

THP_next

THP is a variable that contains sixteen 8-bit values and describes the next transmitter setting of the THP coefficients. It refers to the programmable THP coefficients selected during coefficient exchange described in 55.4.2.5.
Values: 16 coefficients of 8-bit values each. Range is –2.0 to 1.984375 in steps of 0.015625

THP_tx

THP is a variable that contains sixteen 8-bit values and describes the current transmitter setting of the THP coefficients. It refers to the programmable THP coefficients selected during coefficient exchange described in 55.4.2.5.
Values: 16 coefficients of 8-bit values each. Range is –2.0 to 1.984375 in steps of 0.015625

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trans_to_Coeff_Exch

Message field variable defined in 55.4.2.5 that flags a transition by the local device to the PMA_Coeff_Exch state.

Values: 1: The local device transitions to the PMA_Coeff_Exch state on expiration of the transition counter.
0: The local device does not transition to the PMA_Coeff_Exch state.

trans_to_Fine_Adjust

Message field variable defined in 55.4.2.5 that flags a transition by the local device to the PMA_Fine_Adjust state.

Values: 1: The local device transitions to the PMA_Fine_Adjust state on expiration of the transition counter.
0: The local device does not transition to the PMA_Fine_Adjust state.

trans_to_PCS_Test

Message field variable defined in 55.4.2.5 that flags a transition by the local device to the PCS_test state.

Values: 1: The local device transitions to the PCS_test state on expiration of the transition counter.
0: The local device does not transition to the PCS_test state.

transition_count

This variable reports the value of the transition counter contained in the InfoField sent to the remote device. Transition_count has to comply with the state diagram description given in 55.4.6.2. When the message field contains a flag for a state transition, the transition counter denotes the remaining number of InfoField until the next state transition. MASTER initiates the transition to PMA_Coeff_Exch count with the trans_to_Coeff_Exch=1 flag and a counter value of 2^9 (10 ms). The SLAVE responds prior to the counter reaching 2^6 (1 ms) with the same flag and a count value matching the MASTER. Then both PHY's transition to PMA_Coeff_Exch within one PMA frame. The same sequence is performed in the transition to PMA_Fine_Adjust state and PCS_Test state using the trans_to_Fine_Adjust=1 and trans_to_PCS_Test=1 flags respectively. In EEE-capable PHYs, synchronization of the PMA frames is tightly controlled as described in 55.3.5.1. When the message field does not contain a flag for a state transition, the transition counter is set to zero and ignored by the receiver.

Values: 0 to 2^9

tx_mode

PCS Transmit sends code-groups according to the value assumed by this variable.

Values: SEND_N: This value is continuously asserted when transmission of sequences of code-groups representing a XGMII data stream take place.

SEND_T: This value is continuously asserted when transmission of sequences of code-groups representing the sequences of code-groups (TA_n, TB_n, TC_n, TD_n) defined in 55.3.4.2 is to take place.

SEND_Z: This value is asserted when transmission of zero code-groups is to take place.

The following variables are required only for PHYs that support the EEE capability:

lpi_refresh_detect

Set TRUE when the receiver has reliably detected refresh signaling and FALSE otherwise. The exact criteria left to the implementer.

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pcs_data_mode
: Generated by the PMA PHY Control function and indicates whether or not the local PHY may transition its PCS state diagrams out of their initialization states. The current value of the pcs_data_mode is passed to the PCS via the PMA_PCSDATAMODE.indicate primitive. In the absence of the optional EEE and fast retrain capabilities, the PHY operates as if the value of this variable is TRUE.

mtc
: mtc is the transition count for a MASTER PHY during normal training and fast retraining. mtc shall be equal to 2^9 for normal training and 2^5 for fast retrain.

stc
: stc is the transition count for a SLAVE PHY during normal training and fast retraining. stc shall be equal to 2^6 for normal training and 2^4 for fast retrain.

The following six variables are required only for PHYs that support the fast retrain capability:

fr_enable
: This variable is set to TRUE if 1.147.0 is set to 1 and fast retrain is supported. The variable is set to FALSE otherwise.

loc_fr_req
: Set TRUE when the receiver has detected a link failure condition and is requesting a fast retrain; set FALSE otherwise.

loc_fr_detect
: Set TRUE when the receiver has reliably detected the link failure signal. It is highly recommended that loc_fr_detect is qualified with the reception of errored blocks at the LDPC decoder output. Set FALSE when the link failure signal is not detected.

send_link_fail
: When TRUE indicates that the PMA should send the link failure signal. When FALSE the variable has no effect.

fr_active
: Set TRUE when the PHY is performing a fast retrain and set FALSE otherwise.

fast_retrain_flag
: Set TRUE after the PHY generates or detects a link failure signal and set FALSE otherwise.

55.4.5.2 Timers

All timers operate in the manner described in 14.2.3.2.

maxwait_timer
: A timer used to limit the amount of time during which a receiver dwells in the SILENT and TRAINING states. The timer shall expire 2000 ms ± 10 ms after being started. This timer is used jointly in the PHY Control and Link Monitor state diagrams. The maxwait_timer is tested by the Link Monitor to force link_status to be set to FAIL if the timer expires and loc_rcvr_status is NOT_OK. See Figure 55–28 and Figure 55–31.

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minwait_timer
: A timer used to determine the minimum amount of time the PHY Control stays in the SILENT, PMA_Training_Init_S, PCS_Test and PCS_Data states. The timer shall expire 1 ms ± 0.1 ms after being started.

The following timer is required only for PHYs that support the EEE capability:

lpi_refresh_rx_timer
: This timer is used to monitor link quality during the LPI receive mode. If the PHY does not reliably detect reliable refresh signaling before this timer expires then a full retrain is performed.
Values: The condition lpi_refresh_rx_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 50 complete quiet-refresh signal periods, equivalent to 8.192 ms.

The following two timers are required only for PHYs that support the fast retrain capability:

link_fail_sig_timer
: Determines the period of time the PHY sends the link failure signal.
Values: The condition link_fail_sig_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 4 LDPC frame periods.

fr_maxwait_timer
: Determines the period of time the PHY has to transition its PCS Control State to PCS_Test following a fast retrain before the fast retrain is aborted and a full retrain performed.
Values: The condition fr_maxwait_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 30 ms.

55.4.5.3 Functions

Exchange_Final_PBO
: This function transmits and receives the final PBO settings using the InfoField as described in 55.4.2.5.

Exchange_THP_Coefficients
: This function compiles and sends to the link partner and receives from the link partner the desired programmable THP coefficients using the InfoField as described in 55.4.2.5.

55.4.5.4 Counters

The following two counters are required only for PHYs that support the fast retrain capability:

fr_tx_counter
: Counts the number of times the PHY initiates a fast link retrain by transmitting the link failure signal. This counter is reflected in MDIO register 1.147.10:6 specified in 45.2.1.94.2.

fr_rx_counter
: Counts the number of times the PHY begins a fast link retrain in response to the detection of link failure signaling from the link partner. This counter is reflected in MDIO register 1.147.15:11 specified in 45.2.1.94.1.

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55.4.6 State diagrams

55.4.6.1 PHY Control state diagram

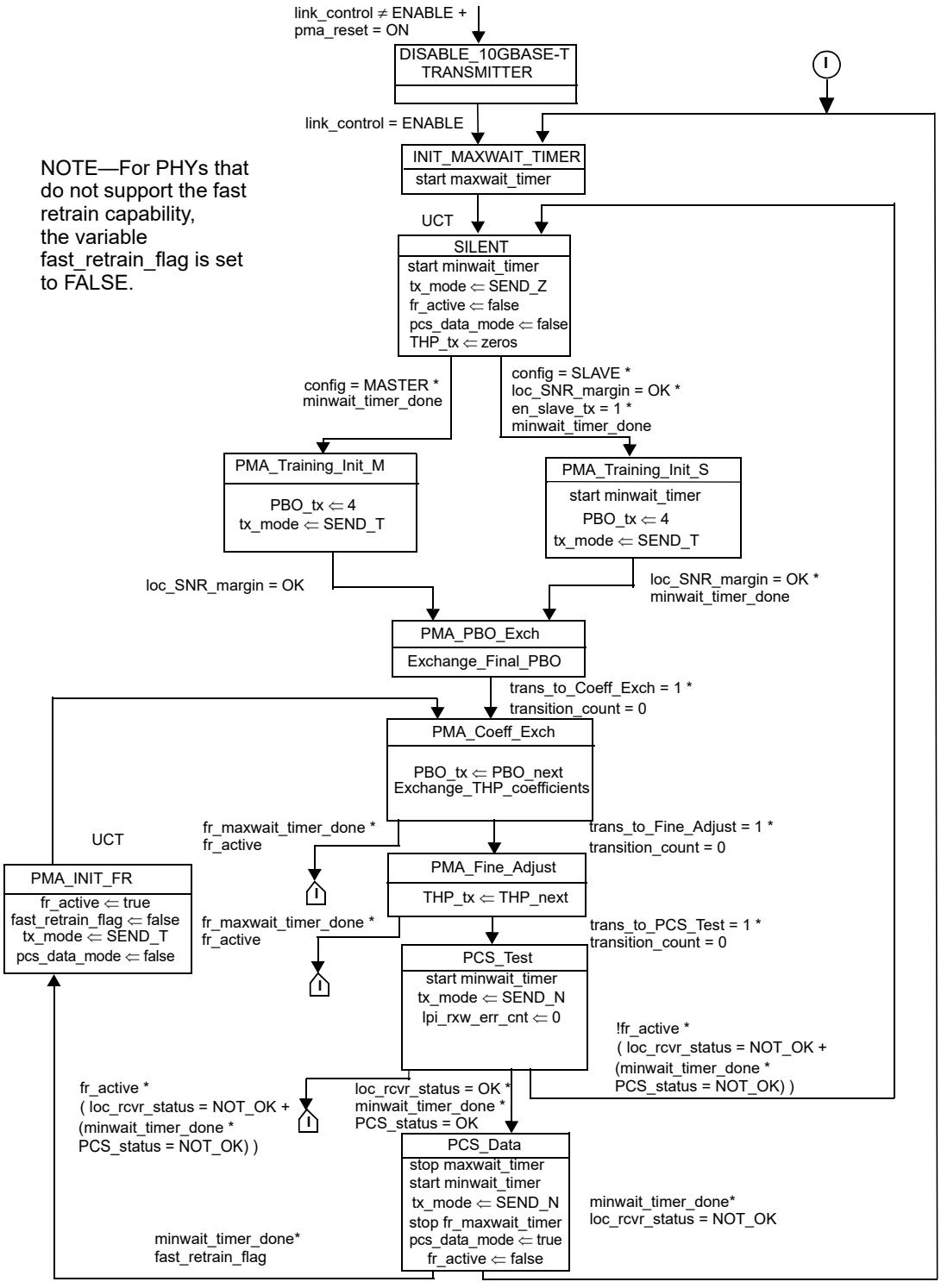

Figure 55–28—PHY Control state diagram

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55.4.6.2 Transition counter state diagrams

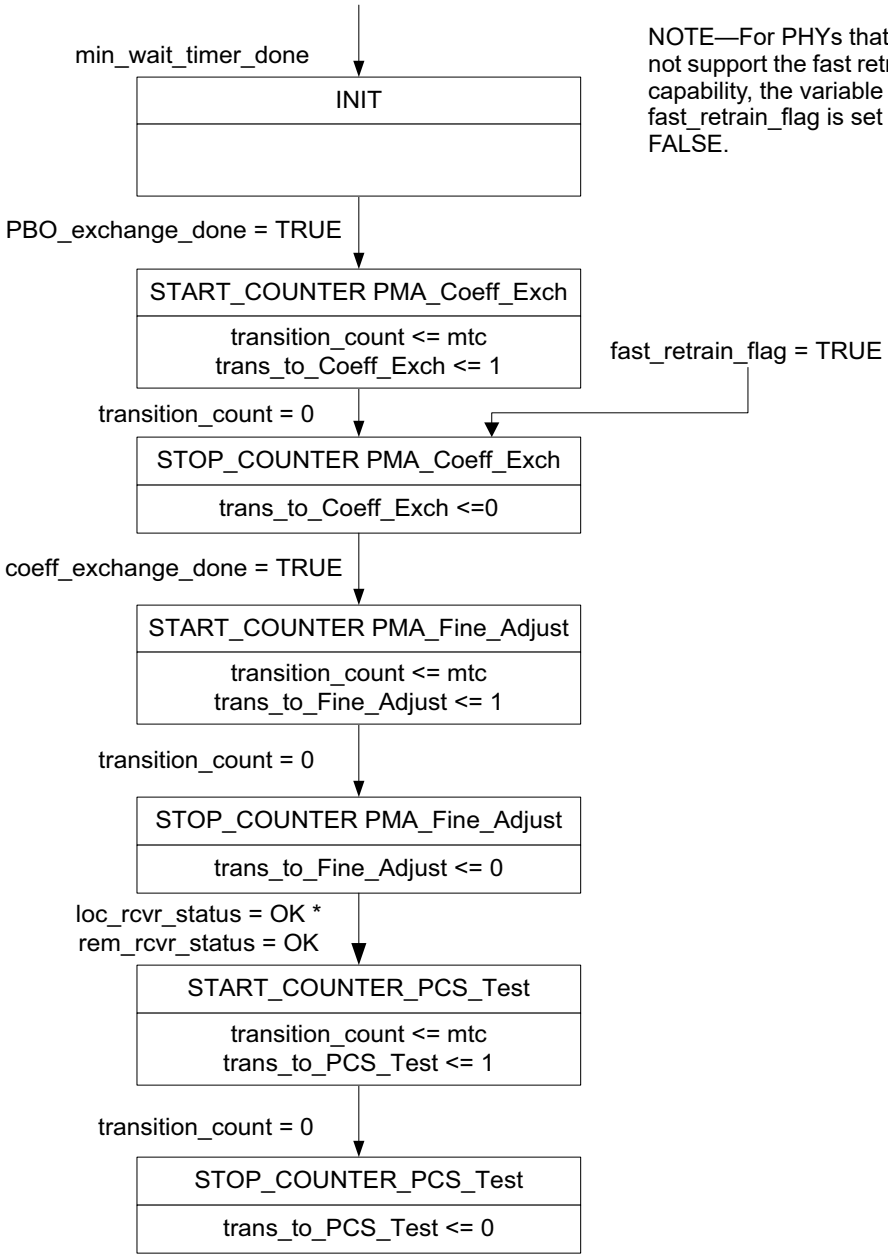

Figure 55–29—MASTER transition counter state diagram

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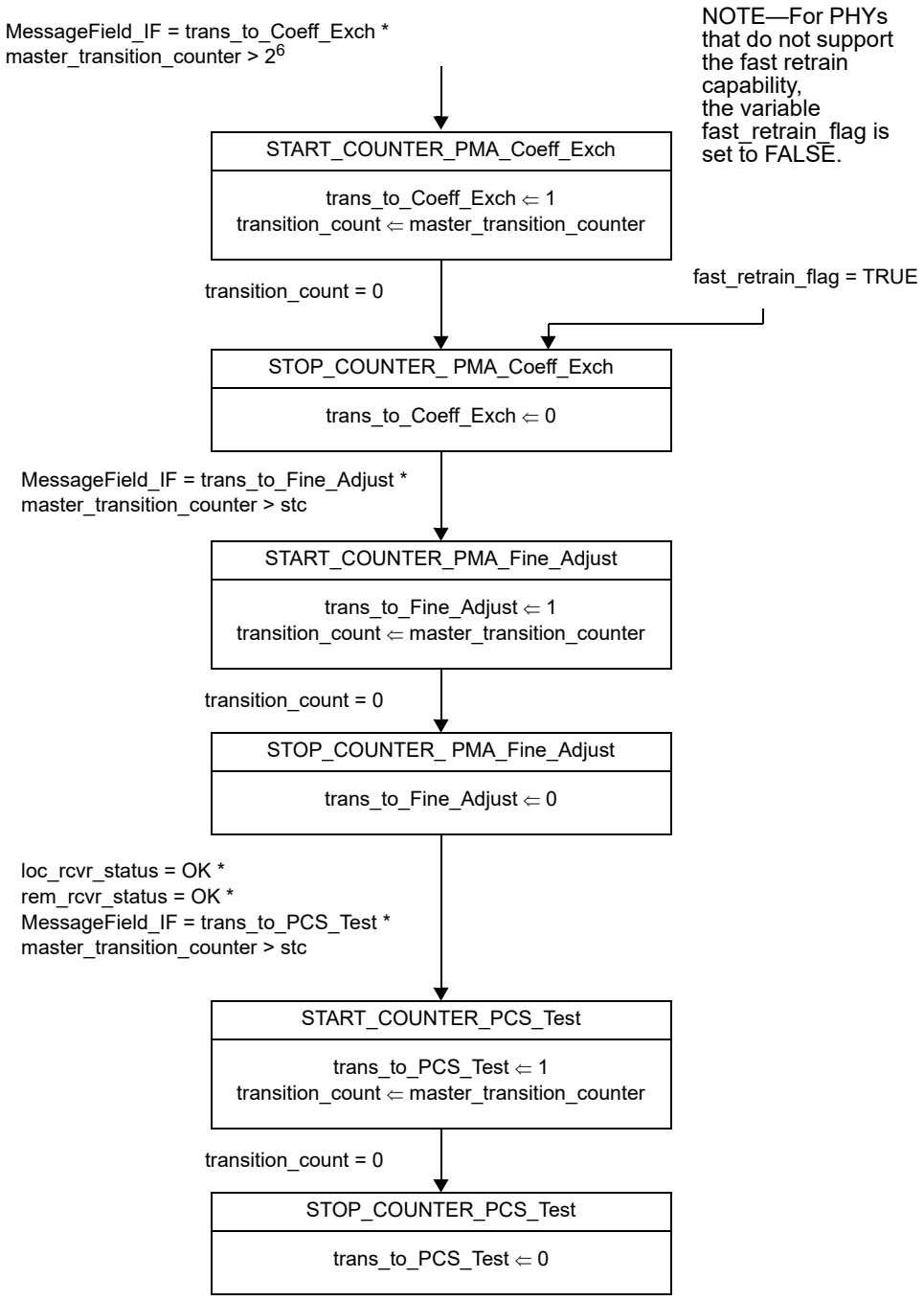

Figure 55–30—SLAVE transition counter state diagram

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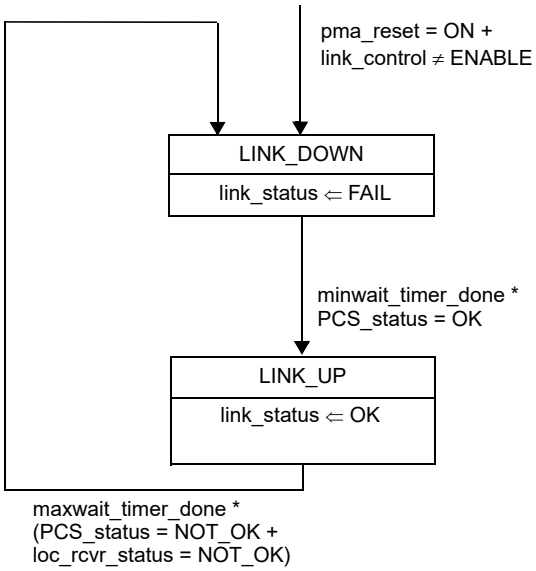
55.4.6.3 Link Monitor state diagram



NOTE 1—maxwait_timer is started in PHY Control state diagram (see Figure 55–28).
NOTE 2—The variables link_control and link_status are designated as link_control_10GigT and link_status_10GigT, respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

Figure 55–31—Link Monitor state diagram

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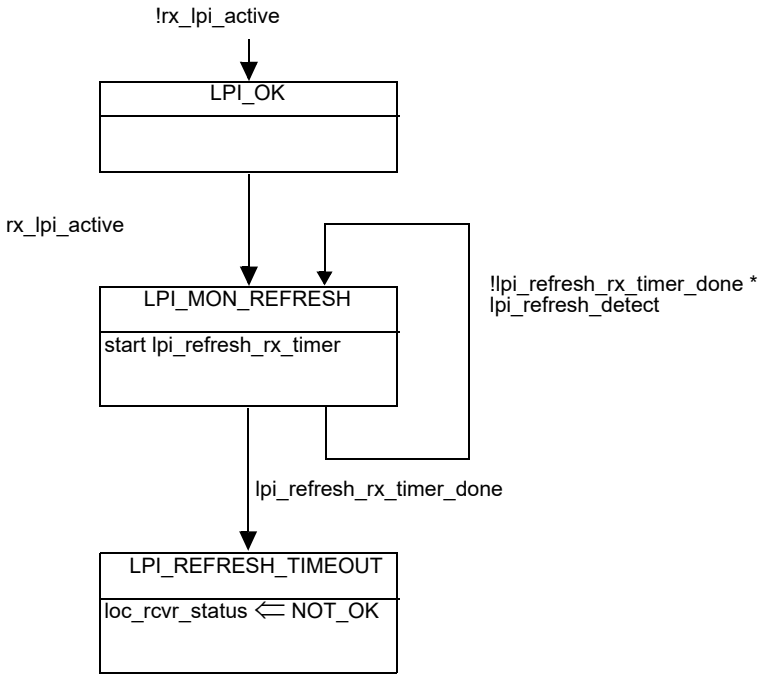
55.4.6.4 EEE Refresh monitor state diagram



NOTE—This state diagram is only required when the PHY supports the EEE capability.

Figure 55–32—EEE Refresh monitor state diagram

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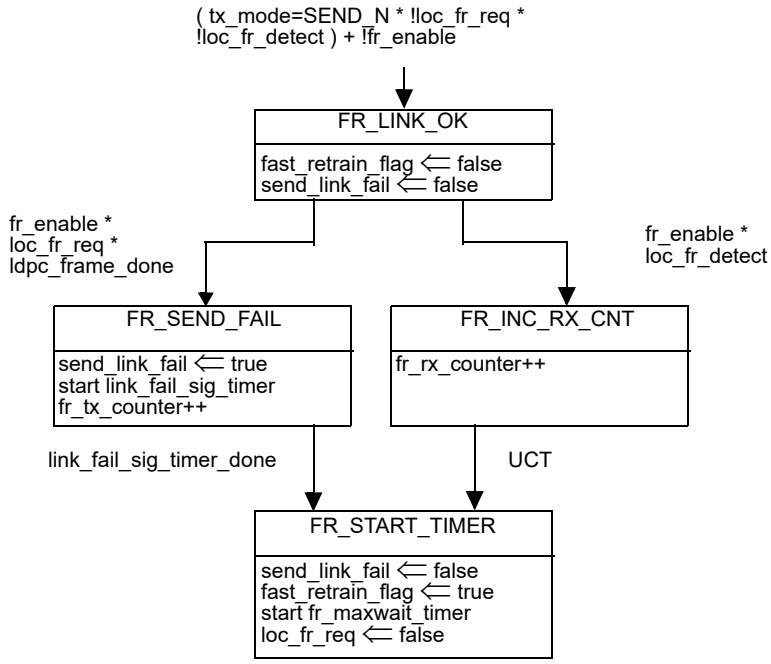
55.4.6.5 Fast retrain state diagram



NOTE—This state diagram is only required when the PHY supports the fast retrain capability.

Figure 55–33—Fast retrain control state diagram

55.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

Common-mode tests use the common-mode return point as a reference.

55.5.1 Electrical isolation

The PHY with a MDI that is not a PI shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical isolation shall meet the isolation requirements as specified in J.1.

55.5.2 Test modes

The test modes described below shall be provided to allow for testing of the transmitter waveform, transmitter distortion, transmitted jitter, transmitter droop and BER testing.

For a PHY with an MDIO management interface, these modes shall be enabled by setting bits 1.132.15:13 (10GBASE-T test mode register) of the MDIO Management register set as shown in Table 55–12. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the

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electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation. PHYs without a MDIO shall provide a means to enable these modes for conformance testing.

Table 55–12—MDIO management register settings for test modes

1.132.15	1.132.14	1.132.13	Mode
0	0	0	Normal operation.
0	0	1	Test mode 1—Setting of MASTER transmitter required by SLAVE for transmit jitter test in SLAVE mode.
0	1	0	Test mode 2—Transmit jitter test in MASTER mode.
0	1	1	Test mode 3—Transmit jitter test in SLAVE mode (if loop timing is supported).
1	0	0	Test mode 4—Transmit distortion test.
1	0	1	Test mode 5—Normal operation with no power backoff. This is for the PSD mask and power level test.
1	1	0	Test mode 6—Transmitter droop test mode.
1	1	1	Test mode 7—Pseudo random test mode for BER Monitor.

Test mode 1 is a mode provided for enabling testing of timing jitter on a SLAVE transmitter. When test mode 1 is enabled, the PHY shall transmit the PMA training pattern (PRBS 33) continually from all four transmitters with the THP turned off, with no power backoff and with the transmitted symbols timed from its local clock source.

Test mode 2 is for transmitter jitter testing when transmitter is in MASTER timing mode. When test mode 2 is enabled, the PHY shall transmit {Two +16 symbols followed by two –16 symbols} continually from all four transmitters with the THP turned off, with no power backoff and with the transmitted symbols timed from its local clock source. The transmitter output is a 200 MHz signal.

Test mode 3 is optional for a PHY that does not support loop timing. When test mode 3 is enabled on a PHY that supports loop timing, the PHY shall transmit, with THP turned off, the data symbol sequence {two +16 symbols followed by two –16 symbols} repeatedly on pair D with the symbols timed from its recovered receive data clock in SLAVE timing mode. A PHY that supports loop timing operates in test mode 3 when there is no input signal on pair D. The transmitter output is a 200 MHz signal on pair D and shall be silence on pairs A, B, and C.

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Test mode 4 is for transmitter linearity testing. When test mode 4 is enabled, the PHY shall transmit, with the THP turned off, transmitted symbols, timed from a transmit clock (as specified in 55.5.3.5) in the MASTER timing mode, defined by the bits1.132.12:10 and Table 55–13.

Table 55–13—MDIO management register settings for transmit frequencies in Test mode 4

1.132.12	1.132.11	1.132.10	Output waveform frequencies in MHz
			Two tone frequency pairs
0	0	0	Reserved
0	1	1	Reserved
1	1	1	Reserved
0	0	1	(800/1024) × 47, (800/1024) × 53
0	1	0	(800/1024) × 101, (800/1024) × 103
1	0	0	(800/1024) × 179, (800/1024) × 181
1	0	1	(800/1024) × 277, (800/1024) × 281
1	1	0	(800/1024) × 397, (800/1024) × 401

The peak-to-peak levels used in this test shall correspond to the ± 16 symbol levels and the relative amplitudes of the tones in a two-tone pair shall be within 0.5 dB of each other.

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit as in normal operation but with the power backoff disabled.

Test mode 6 is for testing transmitter droop. When test mode 6 is enabled, the PHY shall transmit the following sequence of data symbols A_n, B_n, C_n, D_n, of 55.4.3.1 continually from all four transmitters, with the THP turned off:

{One hundred twenty eight +16 followed by one hundred twenty eight –16 symbols}.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the LDPC encoder/decoder, the transmit and receive analog front ends of the PHY and a cable connecting two PHYs. This mode shall reuse the 10GBASE-T scrambler defined in detail in 55.3.3.

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55.5.2.1 Test fixtures

The following fixtures (illustrated by Figure 55–34, Figure 55–35, and Figure 55–36), or their functional equivalents, can be used for measuring the transmitter specifications described in 55.5.3.

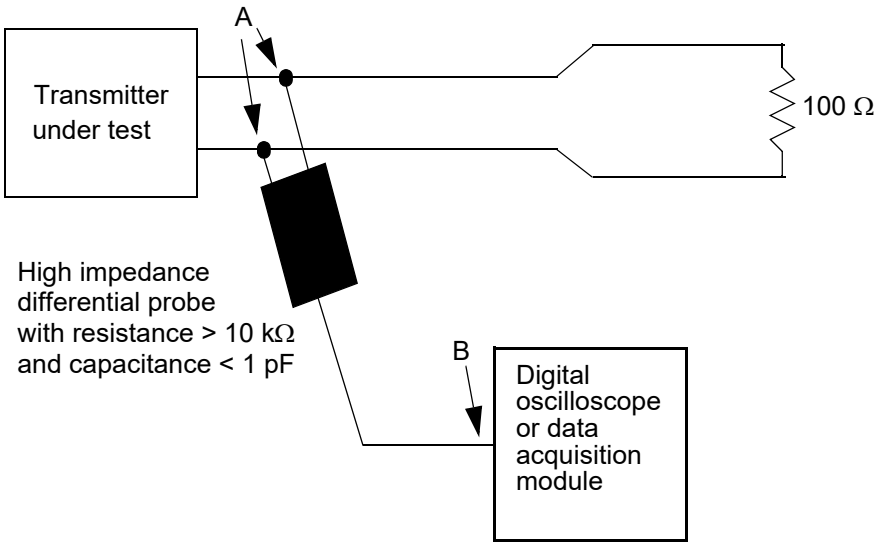

Figure 55–34—Transmitter test fixture 1 for transmitter droop measurement

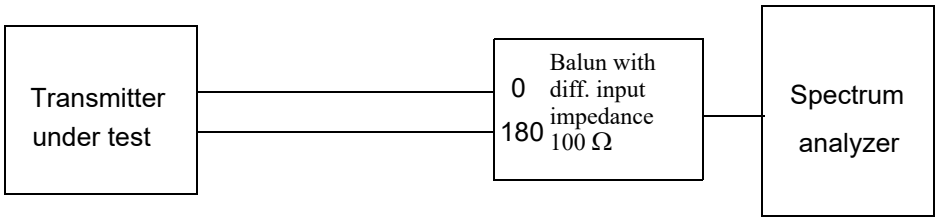

Figure 55–35—Transmitter test fixture 2 for linearity measurement, power spectral density measurement and transmit power level measurement

The high impedance probe shown in Figure 55–34 in transmitter test fixture 1 has resistance > 10 kΩ and capacitance < 1 pF over the frequency range of 1 MHz to 400 MHz. Figure 55–35 includes a power summer or balun device to couple the 100 Ω differential output of the transmitter to the 50 Ω single-ended input typically found in a spectrum analyzer input. The center frequency (f_c) of the band pass filter show in Figure 55–36 is 200 MHz ± 200 kHz and the band pass filter noise bandwidth (B_n) is 2 MHz ± 200 kHz.

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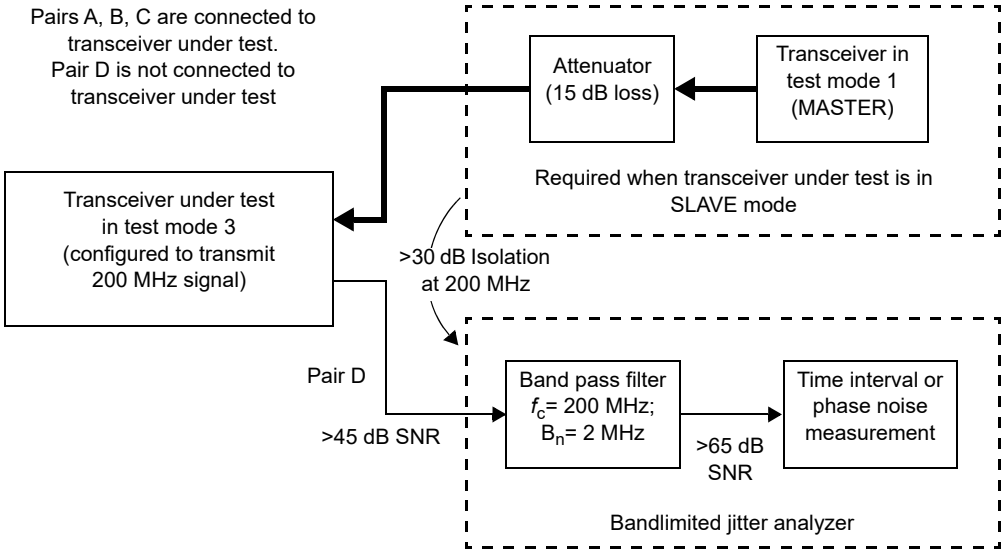

Figure 55–36—Transmitter test fixture 3 for transmitter jitter measurement

55.5.3 Transmitter electrical specifications

The PMA provides the Transmit function specified in 55.4.2.2 in accordance with the electrical specifications of this clause. The PMA shall operate with AC-coupling to the MDI.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.

55.5.3.1 Maximum output droop

With the transmitter in test mode 6 and using the transmitter test fixture 1, the magnitude of both the positive and negative droop shall be less than 10%, measured with respect to an initial value at 10 ns after the zero crossing and a final value at 90 ns after the zero crossing.

55.5.3.2 Transmitter linearity.

When in test mode 4 and observing the spectrum of the differential signal output at the MDI using transmitter test fixture 2, for each pair, with no intervening cable, the transmitter linearity mask is defined as follows:

The SFDR of the transmitter, with dual tone inputs as specified in test mode 4, shall meet the requirement that:

$$\mathrm{SFDR} \geq \quad 2.5 + \ \min\{52,\ 58 - 20 \times \log_{10}(f/25)\} \tag{55–7}$$

where f is the maximum frequency of the two test tones in MHz and SFDR is the ratio in dB of the minimum RMS value of either input tone to the RMS value of the worst intermodulation product in the frequency range of 1 MHz to 400 MHz.

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This specification on transmit linearity is derived from the requirement for interoperability with the far-end device.

55.5.3.3 Transmitter timing jitter

When in test mode 2, the PHY transmits {two +16 symbols followed by two –16 symbols} continually with the THP turned off and with no power backoff. In this mode, the transmitter output should be a 200 MHz signal and the RMS period jitter measured at the PHY MDI output shall be less than 5.5 ps. The RMS period jitter is measured as per the test configuration shown in Figure 55–36 over an integration time interval of 1 ms ± 10%.

For a PHY that can operate in loop timing mode, the SLAVE mode RMS period jitter test shall be run using the test configuration shown in Figure 55–36. For this test, the MASTER PHY is in test mode 1 and the SLAVE PHY is in test mode 3. The MASTER is transmitting the PMA training pattern (PRBS 33) to the SLAVE PHY on pairs A, B, and C. The SLAVE PHY is in loop timing mode, synchronizing its transmit clock to the signals received from the MASTER PHY on pairs A, B, and C. In this configuration, the transmitter output on pair D should be a 200 MHz signal and the RMS period jitter measured at the SLAVE PHY MDI output shall be less than 5.5 ps. The RMS period jitter is measured over an integration time interval of 1 ms ± 10%.

RMS period jitter over an integration time interval of 1 ms ± 10% is defined as the root mean square period difference from the average period ($T - T_{avg}$), accumulated over a sample size of 200 000 ± 20 000:

$$\text{RMS period jitter} = \sqrt{\frac{\sum[(T - T_{avg})^2]}{\text{Sample size}}} \tag{55–8}$$

55.5.3.4 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation with no power backoff), the transmit power shall be in the range 3.2 dBm to 5.2 dBm and the power spectral density of the transmitter, measured into a 100 Ω, load using the test fixture shown in Figure 55–35 shall be between the upper and lower masks specified in Equation (55–9) and Equation (55–10). The masks are shown graphically in Figure 55–37.

$$\text{Upper PSD}\,(f) \le \begin{cases} -78.5\ \text{dBm/Hz} & 0 < f \le 70 \\ -78.5 - \left(\dfrac{f-70}{80}\right)\text{dBm/Hz} & 70 < f \le 150 \\ -79.5 - \left(\dfrac{f-150}{58}\right)\text{dBm/Hz} & 150 < f \le 730 \\ -79.5 - \left(\dfrac{f-330}{40}\right)\text{dBm/Hz} & 730 < f \le 1790 \\ -116\ \text{dBm/Hz} & 1790 < f \le 3000 \end{cases} \tag{55–9}$$

and

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$$\text{Lower PSD}\,(f) \geq \begin{cases} -83 \text{ dBm/Hz} & 5 \leq f \leq 50 \\ -83 - \left(\dfrac{f-50}{50}\right) \text{dBm/Hz} & 50 < f \leq 200 \\ -86 - \left(\dfrac{f-200}{25}\right) \text{dBm/Hz} & 200 < f \leq 400 \end{cases} \quad (55\text{–}10)$$

where f is in MHz.

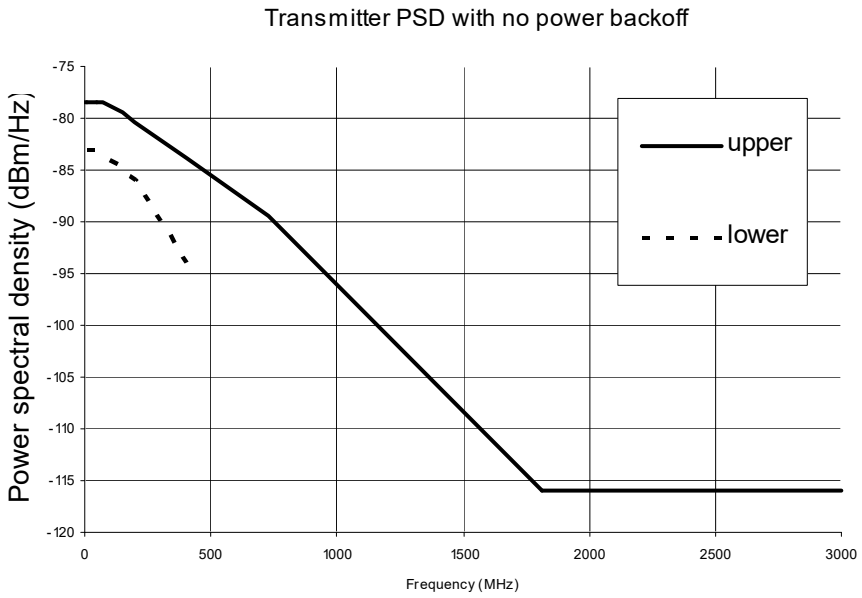

Figure 55–37—Transmitter power spectral density mask

55.5.3.5 Transmit clock frequency

The symbol transmission rate on each pair of the MASTER PHY shall be within the range 800 MHz ± 50 ppm.

When the transmitter is in the LPI transmit mode or when the receiver is in the LPI receive mode the transmitter clock short-term rate of frequency variation shall be less than 0.1 ppm/second. The short-term frequency variation limit shall also apply when switching to and from the LPI mode.

55.5.4 Receiver electrical specifications

The PMA provides the Receive function specified in 55.4.2.4 in accordance with the electrical specifications of this clause using patch cabling and interconnecting hardware that is within the limits specified in 55.7.

55.5.4.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 55.5.3 and have passed through a link specified in 55.7 shall be received with a BER less

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than 10^{-12} after LDPC decoding, and are sent to the XGMII after link reset completion. This specification can be verified by a frame error ratio less than 9.6×10^{-9} for 800 octet frames with minimum IPG or greater than 799 octet IPG.

55.5.4.2 Receiver frequency tolerance

The receive feature shall properly receive incoming data, per the requirements of 55.5.4.1, with a symbol rate within the range 800 MHz ± 50 ppm.

55.5.4.3 Common-mode noise rejection

This specification is provided to limit the sensitivity of the PMA receiver to common-mode noise from the cabling system. Common-mode noise generally results when the cabling system is subjected to electromagnetic fields.

The common-mode noise can be simulated using the cable clamp test defined in 40.6.1.3.3. A 6 dBm sine wave signal from 80 MHz to 1000 MHz can be used to simulate an external electromagnetic field. Operational requirements of the transceiver during the test are determined by the manufacturer. A system integrating a 10GBASE-T PHY may perform this test.

55.5.4.4 Alien crosstalk noise rejection

While receiving data from a transmitter compliant with specifications in 55.5.3, through a 100 m link segment compliant with the specifications in 55.7, a receiver shall operate with an Ethernet frame error ratio less than 9.6×10^{-9} for 800 octet frames with either a minimum IPG or greater than 799 octet IPG with four noise sources at the specified levels representing alien crosstalk, one connected to each of the four pairs. Independent noise sources should be injected into each MDI inputs using couplers that do not significantly alter the link segment characteristics. Each noise source shall have a flat noise spectrum, with 3 dB bandwidth at least 10 MHz to 400 MHz and a power spectral density such that at the MDI port of the device under test the power spectral density of the injected noise is –141.9 dBm/Hz. A flat noise source is chosen to model the sum of all alien noise sources. See Figure 55–38.

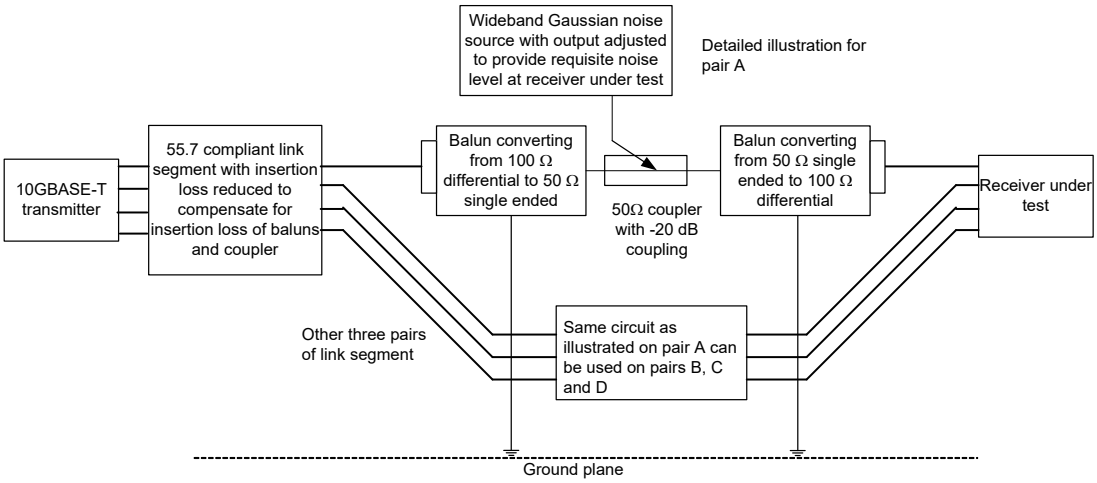

Figure 55–38—Alien crosstalk noise rejection test

The structure shown for injecting the noise in Figure 55–38 is illustrative and alternative approaches are possible. The loss of the coupling structure shown in Figure 55–38, which consists of two baluns and a coupler, is approximately 2.5 dB. The overall insertion loss of the link segment together with the insertion loss of the coupling structure should be adjusted to match the insertion loss specified in 55.7.2.1 to within ±

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0.5 dB. This can be achieved by shortening the cable by approximately 5 m. The balun-coupler-balun structure shown in Figure 55–38 can be replaced by resistively coupling a balanced noise source to the twisted pair using 500 Ω resistors. In either case, calibration of the test setup is required to confirm the overall insertion loss and the injected noise power at the MDI of the receiver under test.

55.5.4.5 Short reach mode link test

In short reach mode (indicating operation over a short reach channel) while receiving data from a transmitter compliant with specifications in 55.5.3 (whether or not in short reach mode), through both short reach test channels, a receiver shall operate with a frame error ratio less than 9.6×10^{-9} for 800 octet frames with minimum IPG or greater than 799 octet IPG (e.g., operate with a BER less than 10^{-12}).

The PHY short reach register setting 1.131.0 indicates whether the PHY is operating in the short reach mode.

55.5.4.5.1 Short reach test channels

One short reach test channel specification is consistent with the transmission characteristics of a cabling link of 30 m consisting of two connectors, 10 m of cable cord, and a horizontal cable distance of 20 m, that meets the ISO/IEC 11801 Category 7 component specifications.

One short reach test channel specification is consistent with the transmission characteristics of a cabling link of 30 m consisting of two connectors, 10 m of cable cord, and a horizontal cable distance of 20 m that meets the Category 6A component specifications.

55.6 Management interfaces

10GBASE-T makes extensive use of the management functions that may be provided by the MDIO (Clause 45), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28). Additional Auto-Negotiation requirements are set forth within this subclause.

55.6.1 Support for Auto-Negotiation

All 10GBASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE. All 10GBASE-T PHYs shall provide support for Extended Next Pages as defined in 28.2.3.4.2 and shall support and use optimized FLP Burst to FLP burst timing as defined in 28.2.1.1.1, and nlp_link_test_min_timer and link_fail_inhibit_timer as defined in 28.3.2.

Auto-Negotiation is performed as part of the initial set-up of the link, and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-Negotiation signaling is used for the following primary purposes for 10GBASE-T:

a) To negotiate that the PHY is capable of supporting 10GBASE-T transmission.
b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.
c) To determine whether the local PHY performs PMA training pattern reset.
d) To determine whether the local PHY supports the EEE capability.
e) To determine whether the local PHY supports the fast retrain capability.

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55.6.1.1 10GBASE-T use of registers during Auto-Negotiation

A 10GBASE-T PHY shall use the management register definitions and values specified in Table 55–14.

Table 55–14—10GBASE-T registers

Register	Bit	Name	Description	Type [a]
7.0	7.0.15:0	AN control register	Defined in 45.2.7.1	R/W
7.1	7.1.15:0	AN status register	Defined in 45.2.7.2	RO
7.2, 7.3	7.2.15:0, 7.3.15:0	AN device identifier registers	Defined in 45.2.7.3	R/W
7.5, 7.6	7.5.15:0, 7.6.15:0	AN devices in package registers	Defined in 45.2.7.4	R/W
7.14, 7.15	7.14.15:0, 7.15.15:0	AN package identifier registers	Defined in 45.2.7.5	R/W
7.16	7.16.15:0	AN advertisement register	Defined in 45.2.7.6	R/W
7.19	7.19.15:0	AN LP Base Page ability register	Defined in 45.2.7.7	RO
7.22, 7.23, 7.24	7.22.15:0, 7.23.15:0, 7.24.15:0	AN XNP transmit register	Defined in 45.2.7.8	R/W
7.25, 7.26, 7.27	7.25.15:0, 7.26.15:0, 7.27.15:0	AN LP XNP ability register	Defined in 45.2.7.9	RO
7.32	7.32.15:0	10GBASE-T AN control register	Defined in 45.2.7.10	R/W
7.33	7.33.15:0	10GBASE-T AN status register	Defined in 45.2.7.11	RO

[a] R/W = Read/Write, RO = Read only

55.6.1.2 10GBASE-T Auto-Negotiation page use

10GBASE-T PHYs shall exchange a 10GBASE-T and 1000BASE-T formatted Extended Next Page, as specified in Table 55–15, immediately following the exchange of the Base Page.

Note that the Acknowledge 2 bit is not utilized and has no meaning when used for the 10GBASE-T message page exchange.

Table 55–15—10GBASE-T Base and Next Pages bit assignments

Bit	Name	Description
Base Page		
D15	Next Page	Defined in 28.2.1.2.6
D14	Acknowledge	Defined in 28.2.1.2.5
D13	Remote Fault	Defined in 28.2.1.2.4
D12	Extended Next Page	Defined in 28.2.1.2.3
D11:D5	Technology Ability Field	Defined in 28.2.1.2.2
D4:D0	Selector Field	Defined in 28.2.1.2.1
Extended Next Page (Message Code Field and Flags Field)		
M10:M0	Next Page message code	Defined in Annex 28C
T	Toggle	Defined in 28.2.3.4.7

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Table 55–15—10GBASE-T Base and Next Pages bit assignments *(continued)*

Bit	Name	Description
Ack2	Acknowledge 2	Defined in 28.2.3.4.6
MP	Message Page	Defined in 28.2.3.4.5
Ack	Acknowledge	Defined in 28.2.3.4.4
NP	Next Page	Defined in 28.2.3.4
Extended Next Page (Unformatted Message Code Field)		
U31:U25	Reserved, transmit as 0	
U24	10GBASE-T EEE (1 = Advertise EEE capability for 10GBASE-T 0 = Do not advertise EEE capability for 10GBASE-T)	Defined in 45.2.7.14.12
U23	1000BASE-T EEE (1 = Advertise EEE capability for 1000BASE-T 0 = Do not advertise EEE capability for 1000BASE-T)	Defined in 45.2.7.14.13
U22	100BASE-TX EEE (1 = Advertise EEE capability for100BASE-TX 0 = Do not advertise EEE capability for 100BASE-TX)	Defined in 45.2.7.14.14
U21	Reserved	
U20	10GBASE-T LD PMA training reset request (1 = Local Device requests that Link Partner reset PMA training PRBS every frame 0 = Local Device requests that Link Partner run PMA training PRBS continuously)	Defined in 45.2.7.10.13
U19	10GBASE-T Fast retrain ability (1 = Advertise PHY as supporting fast retrain, 0 = Advertise PHY as not supporting fast retrain)	Defined in 45.2.7.10.14
U18	PHY short reach mode (1 = PHY of Local Device is operating in short reach mode 0 = PHY of Local Device is operating in normal mode)	Defined in 45.2.1.79.2
U17	10GBASE-T LD loop timing ability (1 = Advertise PHY as capable of loop timing and 0 = do not advertise PHY as capable of loop timing)	Defined in 45.2.7.10.15
U16	10GBASE-T ability (1 = support of 10GBASE-T and 0 = no support)	Defined in 45.2.7.10.4
U15	1000BASE-T half duplex (1 = half duplex and 0 = no half duplex)	
U14	1000BASE-T full duplex (1 = full duplex and 0 = no full duplex)	
U13	Port type bit (1 = multiport device and 0 = single-port device)	Defined in 45.2.7.10.3
U12	10GBASE-T MASTER-SLAVE config value (1 = MASTER and 0 = SLAVE) This bit is ignored if 7.32.15 =0.	Defined in 45.2.7.10.1
U11	10GBASE-T MASTER-SLAVE manual config enable (1 = manual configuration enable) This bit is intended to be used for manual selection in a particular MASTER-SLAVE mode and is to be used in conjunction with bit 7.32.14.	Defined in 45.2.7.10.2
U10	MASTER-SLAVE seed Bit 10 (SB10) (MSB)	
U9	MASTER-SLAVE seed Bit 9 (SB9)	

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Table 55–15—10GBASE-T Base and Next Pages bit assignments *(continued)*

Bit	Name	Description
U8	MASTER-SLAVE seed Bit 8 (SB8)	
U7	MASTER-SLAVE seed Bit 7 (SB7)	
U6	MASTER-SLAVE seed Bit 6 (SB6)	
U5	MASTER-SLAVE seed Bit 5 (SB5)	
U4	MASTER-SLAVE seed Bit 4 (SB4)	
U3	MASTER-SLAVE seed Bit 3 (SB3)	
U2	MASTER-SLAVE seed Bit 2 (SB2)	
U1	MASTER-SLAVE seed Bit 1 (SB1)	
U0	MASTER-SLAVE seed Bit 0 (SB0)	

55.6.1.3 Sending Next Pages

Implementers who do not wish to send additional Next Pages (i.e., Next Pages in addition to those required to perform PHY configuration as defined in this clause) can use Auto-Negotiation as defined in Clause 28.

55.6.2 MASTER-SLAVE configuration resolution

Since both PHYs that share a link segment are capable of being MASTER or SLAVE, a prioritization scheme exists to ensure that the correct mode is chosen. The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using Table 55–16 with the 10GBASE-T Technology Ability Next Page bit values specified in Table 55–15 and information received from the link partner. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown in the Arbitration state diagram (Figure 28–18.)

The following four equations are used to determine these relationships:

manual_MASTER = U11 * U12
manual_SLAVE = U11 * !U12
single-port device = !U11 * !U13
multiport device = !U11 * U13

where

U11 is bit 11 of MultiGBASE-T and 1000BASE-T Technology message code,
U12 is bit 12 of MultiGBASE-T and 1000BASE-T Technology message code,
U13 is bit 13 of MultiGBASE-T and 1000BASE-T Technology message code (see Table 55–15).

A 10GBASE-T PHY is capable of operating either as the MASTER or SLAVE. In the scenario of a link between a single-port device and a multiport device, the preferred relationship is for the multiport device to be the MASTER PHY and the single-port device to be the SLAVE. However, other topologies may result in contention. The resolution function of Table 55–16 is defined to handle any relationship conflicts.

In the instance when both link partners support the optional loop timing mode, or both link partners do not support the loop timing mode, as designated by bit U17, the resolution shown in Table 55–16 shall be used.

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When only one link partner supports loop timing, the device that supports loop timing shall be forced to SLAVE and the other device shall be forced to MASTER.

Table 55–16—10GBASE-T MASTER-SLAVE configuration resolution table

Local device type	Remote device type	Local device resolution	Remote device resolution
single-port device	multiport device	SLAVE	MASTER
single-port device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	manual_MASTER	SLAVE	MASTER
manual_SLAVE	multiport device	SLAVE	MASTER
multiport device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	single-port device	SLAVE	MASTER
multiport device	single-port device	MASTER	SLAVE
multiport device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	manual_SLAVE	MASTER	SLAVE
manual_MASTER	single-port device	MASTER	SLAVE
single-port device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	multiport device	MASTER	SLAVE
multiport device	multiport device	The device with the higher seed value is configured as MASTER, otherwise SLAVE.	The device with the higher seed value is configured as MASTER, otherwise SLAVE.
single-port device	single-port device	The device with the higher seed value is configured as MASTER, otherwise SLAVE	The device with the higher seed value is configured as MASTER, otherwise SLAVE.
manual_SLAVE	manual_SLAVE	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault
manual_MASTER	manual_MASTER	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault

A 10GBASE-T multiport device has higher priority than a single-port device to become the MASTER. In the case where both devices are of the same type, e.g., both devices are multiport devices and both devices have the same loop timing support, the device with the higher MASTER-SLAVE seed bits (SB0...SB10), where SB10 is the MSB, shall become the MASTER and the device with the lower seed value shall become the SLAVE. In case both devices have the same seed value, both should assert link_status_10GigT=FAIL (as defined in 28.3.1) to force a new cycle through Auto-Negotiation. Successful completion of the MASTER-SLAVE resolution shall be treated as MASTER-SLAVE configuration resolution complete.

The method of generating a random or pseudorandom seed is left to the implementer. The generated random seeds should belong to a sequence of independent, identically distributed integer numbers with a uniform distribution in the range of 0 to 2^{11}– 2. The algorithm used to generate the integer should be designed to minimize the correlation between the number generated by any two devices at any given time. A seed counter shall be provided to track the number of seed attempts. The seed counter shall be set to zero at startup and shall be incremented each time a seed is generated. When MASTER-SLAVE resolution is

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complete, the seed counter shall be reset to 0 and bit 7.33.15 shall be set to zero. A MASTER-SLAVE resolution fault shall be declared if resolution is not reached after the generation of seven seeds.

The MASTER-SLAVE manual configuration enable bit (control register bit 7.32.15) and the MASTER-SLAVE config value bit (control register bit 7.32.14) are used to manually set a device to become the MASTER or the SLAVE. In case both devices are manually set to become the MASTER or the SLAVE, this condition shall be flagged as a MASTER-SLAVE configuration fault condition; thus the MASTER-SLAVE configuration fault bit (status register bit 7.33.15) shall be set to logical one. In the situation where one link partner supports loop timing and the other does not, a MASTER-SLAVE configuration fault bit (status register bit 7.33.15) shall be set to one if the link partner with loop timing support is manually set to MASTER or the link partner with no loop timing support is manually set to SLAVE. The MASTER-SLAVE configuration fault condition shall be treated as MASTER-SLAVE configuration resolution complete and link_status_10GigT shall be set to FAIL, because the MASTER-SLAVE relationship was not resolved. This forces a new cycle through Auto-Negotiation after the link_fail_inhibit_timer has expired. Determination of MASTER-SLAVE values occur on the entrance to the FLP LINK GOOD CHECK state (Figure 28–18) when the highest common denominator (HCD) technology is 10GBASE-T. The resulting MASTER-SLAVE value is used by the 10GBASE-T PHY Control (55.4.2.5).

If MASTER-SLAVE manual configuration is disabled (bit 7.32.15 is set to 0) and the local device detects that both the local device and the remote device are of the same type (either multiport device or single-port device and identical loop timing support) and that both have generated the same random seed, it generates and transmits a new random seed for MASTER-SLAVE negotiation by setting link_status to FAIL and cycling through the Auto-Negotiation process again.

The MASTER-SLAVE configuration process returns one of the three following outcomes:

a) *Successful:* Bit 7.33.15 of the 10GBASE-T status register is set to logical zero and bit 7.33.14 is set to logical one for MASTER resolution or for logical zero for SLAVE resolution. 10GBASE-T returns control to Auto-Negotiation (at the entrance to the FLP LINK GOOD CHECK state in Figure 28–18) and passes the value MASTER or SLAVE to PMA_CONFIG.indication (see 55.2.2.2).
b) *Unsuccessful:* link_status_10GigT is set to FAIL and Auto-Negotiation restarts (see Figure 28–18).
c) *Fault detected:* Bit 7.33.15 of the 10GBASE-T status register is set to logical one to indicate that a configuration fault has been detected. This bit also is set when seven attempts to configure the MASTER-SLAVE relationship via the seed method have failed. When a fault is detected, link_status_10GigT is set to FAIL, causing Auto-Negotiation to cycle through again.

NOTE—MASTER-SLAVE arbitration only occurs if 10GBASE-T or 1000BASE-T is selected as the highest common denominator.

55.7 Link segment characteristics

10GBASE-T is designed to operate over ISO/IEC 11801 Class E or Class F 4-pair balanced cabling that meets the additional requirements specified in this subclause. Each of the four pairs supports an effective data rate of 2500 Mb/s in each direction simultaneously. The term “link segment” used in this clause refers to four twisted-pairs operating in full duplex. Specifications for a link segment apply equally to each of the four twisted-pairs. All implementations of the balanced cabling link segment specification shall be compatible at the MDI. It is recommended that the guidelines in TIA TSB-155-A, ISO/IEC TR 24750, ANSI/TIA-568-C.2, and ISO/IEC 11801:2002/Amendment 1 be considered before the installation of 10GBASE-T equipment for any cabling system.

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55.7.1 Cabling system characteristics

The cabling system used to support 10GBASE-T requires 4 pairs of ISO/IEC 11801 Class E or Class F balanced cabling with a nominal impedance of 100 Ω. Operation on other classes of cabling may be supported if the link segment meets the requirements of 55.7.

Additionally:

a) 10GBASE-T uses a star topology with Class E or Class F balanced cabling used to connect PHY entities.
b) 10GBASE-T is an ISO/IEC 11801 Class E and Class F application with the additional transmission requirements specified in this subclause. The ISO/IEC 11801 cabling limit calculation minimums apply to the link segment specifications. Mitigation practices may be required—see Annex 55B.

55.7.2 Link segment transmission parameters

A link segment consisting of up to 100 m of Class E or up to 100 m of Class F that meets the transmission parameters of this subclause provides a reliable medium. The transmission parameters of the link segment include insertion loss, delay parameters, nominal impedance, NEXT loss, ELFEXT, and return loss. In addition, the requirements for the alien crosstalk coupled "between" link segments is specified.

Table 55–17 lists the supported cabling types and distances.

Table 55–17— Cabling types and distances

Cabling	Supported link segment distances	Cabling references
Class E / Category 6	55 m to 100 m[a]	ISO/IEC TR 24750 / TIA TSB-155-A
Class E / Category 6: unscreened	55 m	ISO/IEC TR 24750 / TIA TSB-155-A
Class E / Category 6: screened	100 m	ISO/IEC TR 24750 / TIA TSB-155-A
Class F	100 m	ISO/IEC TR 24750
Class E_A / Category 6A	100 m	ISO/IEC 11801:2002/Amendment 1 / ANSI/TIA-568-C.2
Class F_A	100 m	ISO/IEC 11801:2002 Amendment 1

[a]Supported link segments up to 100 m shall meet the alien crosstalk to insertion loss requirements specified in 55.7.3.1.2 and 55.7.3.2.2.

The link segment transmission parameters of insertion loss and ELFEXT specified are ISO/IEC 11801 Class E specifications extended by extrapolating the formulas to a frequency up to 500 MHz with appropriate adjustments for length when applicable as specified in ISO/IEC TR 24750 and TIA TSB-155-A. The link segment transmission parameters of NEXT loss, MDNEXT loss, and return loss specified are ISO/IEC 11801 Class E specifications extended beyond 250 MHz by utilizing the equations referenced in TIA TSB-155.

55.7.2.1 Insertion loss

The insertion loss of each duplex channel shall meet the values determined using Equation (55–11).

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$$\text{Insertion loss}(f) \leq 1.05\left(1.82 \times \sqrt{f} + 0.0169 \times f + \frac{0.25}{\sqrt{f}}\right) + 4 \times 0.02 \times \sqrt{f} \quad \text{(dB)} \tag{55–11}$$

where

f is the frequency in MHz; $1 \leq f \leq 500$

This includes the insertion loss of the balanced cabling pairs, including work area and equipment cables plus connector losses within each duplex channel.

For the purpose of calculating the link segment insertion loss for cabling less than 100 m the cable insertion loss is assumed to scale linearly with length as defined in Equation (55–27).

55.7.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each link segment duplex channel, which includes cable cords and connecting hardware, is 100 Ω for all frequencies between 1 MHz and 500 MHz.

55.7.2.3 Return loss

In order to limit the noise at the receiver due to impedance mismatches in the cabling system, each link segment duplex channel shall meet the values determined using Equation (55–12) at all frequencies from 1 MHz to 500 MHz. The reference impedance for the return loss specification is 100 Ω.

$$\text{Return loss} \geq \left\{ \begin{array}{ll} 19 & 1 \leq f < 10 \\ 24 - 5\log_{10}(f) & 10 \leq f < 40 \\ 32 - 10\log_{10}(f) & 40 \leq f < 400 \\ 6 & 400 \leq f \leq 500 \end{array} \right\} \quad \text{(dB)} \tag{55–12}$$

where

f is the frequency in MHz.

55.7.2.4 Coupling parameters between duplex channels comprising one link segment

In order to limit the noise coupled into a duplex channel from adjacent duplex channels, near-end crosstalk (NEXT) loss and equal level far-end crosstalk (ELFEXT) are specified for each link segment. In addition, each duplex channel can be disturbed by more than one duplex channel. To ensure the total NEXT loss and FEXT loss coupled into a duplex channel is limited, multiple disturber near-end crosstalk (MDNEXT) and multiple disturber ELFEXT (MDELFEXT) is specified.

55.7.2.4.1 Differential near-end crosstalk

In order to limit the crosstalk at the near end of a link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between a duplex channel and the other three duplex channels is specified to meet the bit error ratio objective specified in 55.1.1. The NEXT loss between any two duplex channels of a link segment shall meet the values determined using Equation (55–13)

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$$\text{NEXT loss}(f) \geq \begin{cases} -20\log_{10}\left(10^{\frac{74.3 - 15\log_{10}(f)}{-20}} + 2 \times 10^{\frac{94 - 20\log_{10}(f)}{-20}}\right) \text{ (dB)} & 1 \leq f < 330 \\ 31 - 50\log_{10}\left(\frac{f}{330}\right) \text{ (dB)} & 330 \leq f \leq 500 \end{cases} \quad (55\text{–}13)$$

where

f is the frequency in MHz.

Calculations that result in NEXT loss values greater than 65 dB shall revert to a requirement of 65 dB minimum.

55.7.2.4.2 Multiple disturber near-end crosstalk (MDNEXT) loss

Since four duplex channels are used to transfer data between PMDs, the NEXT that is coupled into a data carrying channel is from the three adjacent disturbing duplex channels.

To ensure the total NEXT coupled into a duplex channel is limited, multiple disturber NEXT loss is specified as the power sum of the individual NEXT losses. The power sum loss between a duplex channel and the three adjacent disturbers shall meet the values determined using Equation (55–14).

$$\text{MDNEXT loss}(f) \geq \begin{cases} -20\log_{10}\left(10^{\frac{72.3 - 15\log_{10}(f)}{-20}} + 2 \times 10^{\frac{90 - 20\log_{10}(f)}{-20}}\right) \text{ (dB)} & 1 \leq f < 330 \\ 28 - 50\log_{10}\left(\frac{f}{330}\right) \text{ (dB)} & 330 \leq f \leq 500 \end{cases} \quad (55\text{–}14)$$

where

f is the frequency in MHz.

Calculations that result in PS NEXT loss values greater than 62 dB shall revert to a requirement of 62 dB minimum.

55.7.2.4.3 Multiple disturber power sum near-end crosstalk (PSNEXT) loss

PS NEXT loss is determined by summing the power of the three individual pair-to-pair differential NEXT loss values over the frequency range 1 MHz to 500 MHz as follows in Equation (55–15).

$$\text{PSNEXT loss}(f) = \left(-10\log_{10}\sum_{i=1}^{n} 10^{\frac{-NL(f)i}{10}}\right) \text{ (dB)} \quad (55\text{–}15)$$

where

$NL(f)i$ is the magnitude in dB of NEXT loss at frequency f (in MHz) of pair combination i

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i is the pair-to-pair combination (1 to *n*)

n is the number of pair-to-pair combinations (*n*=3)

55.7.2.4.4 Equal level far-end crosstalk (ELFEXT)

Equal level far-end crosstalk (ELFEXT) is specified in order to limit the crosstalk at the far end of each link segment duplex channel and meet the bit error ratio objective specified in 55.1.1. Far-end crosstalk (FEXT) is crosstalk that appears at the far end of a duplex channel (disturbed channel), which is coupled from another duplex channel (disturbing channel) with the noise source (transmitters) at the near end.

FEXT loss is defined in Equation (55–16) as

$$\text{FEXT loss}(f) = 20\log_{10}\left(\frac{V_{pds}(f)}{V_{pcn}(f)}\right) \quad \text{(dB)} \tag{55–16}$$

and ELFEXT is defined in Equation (55–17) as

$$\text{ELFEXT}\ (f) = 20\log_{10}\left(\frac{V_{pds}(f)}{V_{pcn}(f)}\right) - \text{SLS\_Loss(f)}\ \text{(dB)} \tag{55–17}$$

where

Vpds is the peak voltage of disturbing signal (near-end transmitter),
Vpcn is the peak crosstalk noise at far end of disturbed channel,
SLS_Loss is the insertion loss of disturbed channel in dB.

The worst pair ELFEXT between any two duplex channels shall meet the values determined using Equation (55–18).

$$\text{ELFEXT} \geq -20\log_{10}\left(10^{\frac{67.8 - 20\log_{10}(f)}{-20}} + 4 \times 10^{\frac{83.1 - 20\log_{10}(f)}{-20}}\right) \quad \text{(dB)} \tag{55–18}$$

where

f is the frequency in MHz and $1 \leq f \leq 500$.

The numerator of the first term “raised to the power of 10” in Equation (55–18) is the cable portion of the duplex channel of 100 m. The ELFEXT of the cable improves as the cable is reduced in length as defined in Equation (55–19). The equation assumes coupling over 100 m of cable including horizontal cable and cable cords.

$$\text{ELFEXT}(f, L) = (67.8 - 20\log_{10}(f)) - 10\log_{10}\left(\frac{L}{100}\right) \quad \text{(dB)} \tag{55–19}$$

where

L is the length in meters of the link segment,
f is the frequency in MHz.

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55.7.2.4.5 Multiple disturber equal level far-end crosstalk (MDELFEXT)

Since four duplex channels are used to transfer data between PMDs, the FEXT that is coupled into a data carrying channel is from the three adjacent disturbing duplex channels. To ensure the total FEXT coupled into a duplex channel is limited, multiple disturber ELFEXT is specified as the power sum of the individual ELFEXT disturbers. The power sum loss between a duplex channel and the three adjacent disturbers shall meet the values determined using Equation (55–20).

$$\text{MDELFEXT}(f) \geq -20\log_{10}\left(10^{\frac{64.8 - 20\log_{10}(f)}{-20}} + 4 \times 10^{\frac{80.1 - 20\log_{10}(f)}{-20}}\right) \quad \text{(dB)} \qquad \text{(dB)} \qquad (55\text{–}20)$$

where

f is the frequency $1 \leq f \leq 500$.

55.7.2.4.6 Multiple disturber power sum equal level far-end crosstalk (PS ELFEXT)

PS ELFEXT is determined by summing the power of the three individual pair-to-pair differential ELFEXT values over the frequency range 1 MHz to 500 MHz as follows in Equation (55–21):

$$\text{PSELFEXT}\ (f)\ =\ -10\log_{10}\sum_{i\,=\,1}^{i\,=\,n} 10^{\frac{-EL(f)i}{10}} \qquad \text{(dB)} \qquad (55\text{–}21)$$

where

EL(f)i is the magnitude of ELFEXT at frequency *f* of pair combination *i*,
i is the pair-to-pair combination (1 to *n*),
f is the frequency in MHz,
n is the number of pair-to-pair combinations (*n*=3).

55.7.2.5 Maximum link delay

The propagation delay of a link segment shall not exceed 570 ns at all frequencies between 2 MHz and 500 MHz.

55.7.2.6 Link delay skew

The difference in propagation delay, or skew, between all duplex channel pair combinations of a link segment, under all conditions, shall not exceed 50 ns at all frequencies from 2 MHz to 500 MHz. It is a further functional requirement that, once installed, the skew between any two of the four duplex channels due to environmental conditions shall not vary more than 10 ns within the above requirement.

55.7.3 Coupling parameters between link segments

Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. To ensure the total alien NEXT loss and alien FEXT loss coupled between link segments is limited, multiple disturber alien near-end crosstalk (MD ANEXT) loss and multiple disturber alien FEXT (MDAFEXT) loss is specified. In addition, to ensure the reliable operation of the link segment, a minimum alien crosstalk to insertion loss ratio are specified.

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55.7.3.1 Multiple disturber alien near-end crosstalk (MDANEXT) loss

In order to limit the alien crosstalk at the near end of a link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is specified to meet the bit error ratio objective specified in 55.1.1. To ensure the total alien NEXT coupled into a duplex channel is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT disturbers.

55.7.3.1.1 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

PS ANEXT loss is determined by summing the power of the individual pair-to-pair differential alien NEXT loss values over the frequency range 1 MHz to 500 MHz as follows in Equation (55–22):

$$\mathrm{PSANEXT}_N(f) = -10\log_{10}\sum_{j=1}^{m}\sum_{i=1}^{4} 10^{\frac{-AN(f)_{i,j,N}}{10}} \quad (\mathrm{dB}) \tag{55–22}$$

where

$AN(f)_{i,j,N}$ is the magnitude in dB of the alien NEXT loss at frequency f of the individual pair combination i (1 to 4) of the disturbing link j (1 to m) for each disturbed pair N.

Annex 55B provides additional information on identifying the number of adjacent link segments to consider in the PSANEXT calculation.

The power sum ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall meet the values determined using Equation (55–23) independent of length.

$$\mathrm{PSANEXT}(f) \geq \begin{cases} X1 - 10\log_{10}\left(\frac{f}{100}\right) \ (\mathrm{dB}) & 1 \leq f \leq 100 \\ X1 - 15\log_{10}\left(\frac{f}{100}\right) \ (\mathrm{dB}) & 100 < f \leq 500 \end{cases} \tag{55–23}$$

where

f is the frequency in MHz,
$X1$ is the value at f=100 MHz. $X1$ is referred to as the PSANEXT constant.

When the computed PSANEXT value at a certain frequency exceeds 67 dB, the PSANEXT result at that frequency is for information only.

The PSANEXT constant is determined in 55.7.3.1.2 constrained by the ratio of the PSANEXT to the insertion loss.

The average PSANEXT between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is the average of the individual-pair PSANEXT “across the 4-pairs” determined using Equation (55–24):

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$$\text{PSANEXT}avg(f) = \frac{\left(\sum_{i=1}^{n} \text{PSANEXT}(f)\_\text{pair\_i (dB)} \right)}{4} \qquad (55\text{–}24)$$

where

PSANEXT*(f)*_pair_i is the magnitude in dB of PSANEXT loss at frequency *f* of pair_i,
n is the number of individual-pairs (*n* = 4).

The average PSANEXT loss of the 4-pairs shall meet the values determined using Equation (55–25) independent of length.

$$\text{PSANEXT}avg(f) \geq \begin{cases} (X1 + 2.25) - 10 \log_{10}\left(\frac{f}{100}\right) \text{ (dB)} & 1 \leq f \leq 100 \\ (X1 + 2.25) - 15 \log_{10}\left(\frac{f}{100}\right) \text{ (dB)} & 100 < f \leq 500 \end{cases} \qquad (55\text{–}25)$$

where

f is the frequency in MHz,
X1 is the value at *f* =100 MHz. *X1* is referred to as the PSANEXT constant.

55.7.3.1.2 PSANEXT loss to insertion loss ratio requirements

To ensure reliable operation, a minimum insertion loss to alien crosstalk ratio shall be maintained. The PSANEXT loss requirement of 55.7.3.1.1 can be relaxed based on a reduction in the maximum insertion loss specified in 55.7.2.1. The insertion loss reduction can be achieved by utilizing link segments less than 100 m defined by (55–27) or the insertion loss at 250 MHz of the supported cabling types in Table 55–17.

The adjusted PSANEXT loss requirement is determined by first calculating the PSANEXT constant and utilizing the constant in the PSANEXT limit line Equation (55–23) and Equation (55–25).

The PSANEXT_constant shall be specified by the following Equation (55–26):

$$\text{PSANEXT\_constant} = 62 - \frac{10GBTIL(250\text{ MHz}) - \text{IL}(250\text{ MHz})}{1.04} \text{ (dB)} \qquad (55\text{–}26)$$

where

10*GBTIL(*250*MHz)* is the link segment insertion loss at 250 MHz [Equation (55–11)],
IL(250*MHz*) is the insertion loss of a link segment less than 100 m [Equation (55–27)] or the insertion loss at 250 MHz of the supported cabling types in Table 55–17. For measurement-based calculations, IL(250 MHz) shall be the average of the insertion loss of the 4-pairs at 250 MHz.

The calculated PSANEXT_constant values less than 33.5 dB shall revert to a value of 33.5 dB.

For the purpose of calculating the link segment insertion loss for cabling less than 100 m the cable insertion loss is assumed to scale linearly with length.

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The scaled link segment is defined by the following Equation (55–27):

$$\text{Scaled\_10GBTIL} = \frac{\text{Length\_m}}{100} \times 1.05\left(1.82 \times \sqrt{f} + 0.0169 \times f + \frac{0.25}{\sqrt{f}}\right) + 4 \times 0.02 \times \sqrt{f} \quad \text{(dB)} \qquad (55\text{–}27)$$

where

Length_m is in meters,
f is the frequency in MHz.

Table 55–18 provides the calculated PSANEXT_constants for link segments of 100 m and 55 m.

Table 55–18— Calculated PS ANEXT constants

Link segment distance	PSANEXT_constant (dB)	PSANEXT_constant_avg average of the 4-pairs (dB)	Insertion loss at 250 MHz (dB)
100 m	62	64.25	35.9
55 m	47	49.25	20.3

Table 55–19 provides the calculated PSANEXT_constants for the supported cabling types.

Table 55–19— Calculated PSANEXT constants for supported cabling types

Cabling	Insertion loss at 250 MHz (dB)	PSANEXT_constant (dB)	PSANEXT_constant_avg average of the 4-pairs (dB)
Category 6/ Class E	35.9[a], 20.3[b]	62[a], 47[b]	64.25[a], 49.25[b]
Class E_A / Category 6A	33.8	60	62.25
Class F	33.8	60	62.25

[a]Link segment length of 100 m.
[b]Link segment length of 55 m.

Table 55–20 provides the calculated PSANEXT to insertion loss ratio for the supported cabling types.

Table 55–20— Calculated PSANEXT to insertion loss ratio at 250 MHz

Cabling	Insertion loss at 250 MHz (dB)	PSANEXT at 250 MHz (dB)	PSANEXT to insertion loss ratio at 250 MHz (dB)
Category 6/ Class E	35.9[a], 20.3[b]	56.0[a], 41.0[b]	20.1[a], 20.7[b]
Class E_A / Category 6A	33.8	54.0	20.2
Class F	33.8	54.0	20.2

[a]Link segment length of 100 m.
[b]Link segment length of 55 m.

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For simulating PHY performance to estimate system margin, the PSANEXT_constant is increased by 3.5 dB to account for an averaging of the PSANEXT over frequency and averaging the PSANEXT *across the 4-pairs*.

55.7.3.2 Multiple disturber alien far-end crosstalk (MDAFEXT) loss

In order to limit the alien crosstalk at the far-end of a link segment, the differential pair-to-pair alien far-end crosstalk loss between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is specified to meet the bit error ratio objective specified in 55.1.1. To ensure the total alien FEXT coupled into a duplex channel is limited, multiple disturber ELFEXT is specified as the power sum of the individual alien ELFEXT disturbers.

55.7.3.2.1 Multiple disturber power sum alien equal level far-end crosstalk (PSAELFEXT)

Power sum alien ELFEXT is determined by summing the power of the individual pair-to-pair differential alien ELFEXT values over the frequency range 1 MHz to 500 MHz as follows in Equation (55–28):

$$\mathrm{PSAELFEXT}_N(f) = -10\log_{10}\sum_{j=1}^{m}\sum_{i=1}^{4} 10^{\frac{-EL(f)_{i,j,N}}{10}} \quad \text{(dB)} \tag{55–28}$$

where

$EL(f)_{i,j,N}$ is determined using Equation (55–29) as the magnitude in dB of the alien ELFEXT of the coupled length at frequency f of the individual pair combination i (1 to 4) of the disturbing link j (1 to m) for each disturbed pair N corrected by subtracting the $10\log_{10}$ ratio of the disturbed length insertion loss to the coupled length insertion loss. The coupled length is the length of cabling over which the crosstalk coupling can occur.

$$EL(f)_{i,j,N} = AlienELFEXT(f)_{i,j,N} - 10\log_{10}\left(\frac{DisturbedIL_N}{CoupledlengthIL_{i,j,N}}\right) \tag{55–29}$$

where

$AlienELFEXT(f)_{i,j,N}$ is determined using Equation (55–30) as the difference of the magnitude in dB of the Alien FEXT of the coupled length at frequency f of the individual pair combination i (1 to 4) of the disturbing link j (1 to m) for each disturbed pair N and the insertion loss of the coupled length.

$$AlienELFEXT(f)_{i,j,N} = AFEXT(f)_{i,j,N} - CoupledlengthIL(f)_{i,j,N} \tag{55–30}$$

where

$CoupledlengthIL(f)_{i,j,N}$ is determined using Equation (55–31) as the minimum of the insertion loss of the disturbed pair N and the disturbing individual pair i (1 to 4) of the disturbing link j (1 to m).

$$CoupledlengthIL(f)_{i,j,N} = min(DisturbedIL_N, DisturbingIL_{i,j}) \tag{55–31}$$

NOTE—The computation of PSAELFEXT in Equation (55–28) is consistent with the computation of power sum alien attenuation to crosstalk ratio far end (PS AACR-F). The term PS AACR-F is used in ISO/IEC TR 24750 and in the 1st amendment to the second edition of ISO/IEC 11801.

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The PSAELFEXT between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall meet the values determined using Equation (55–32).

$$\text{PSAELFEXT}(f) \geq X2 - 20\log_{10}\left(\frac{f}{100}\right) \quad (dB) \qquad 1 \leq f \leq 500 \tag{55–32}$$

where

f is the frequency in MHz,
X2 is the value at *f* =100 MHz. *X2* is referred to as the PSAELFEXT constant.

When the measured PSAFEXT limit value at a certain frequency exceeds 72-15log$_{10}$(*f*/100) dB, 67 dB max, the PSAELFEXT result at that frequency is for information only.

The average PSAELFEXT between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is the average of the individual-pair PS AELFEXT *across the 4-pairs* determined using Equation (55–33).

$$\text{PSAELFEXT}avg(f) = \frac{\left(\sum_{i=1}^{n} \text{PSAELFEXT}(f)\_\text{pair\_i (dB)}\right)}{4} \tag{55–33}$$

where

PSAELFEXT*(f)*_pair_i is the magnitude in dB of PSAELFEXT loss at frequency *f* of pair *i*,
n is the number of individual-pairs (*n* = 4).

The average PSAELFEXT of the 4-pairs shall meet the values determined using Equation (55–34).

$$\text{PSAELFEXT}avg(f) \geq (X2 + 4) - 20\log_{10}\left(\frac{f}{100}\right) \quad (\text{dB}) \qquad 1 \leq f \leq 500 \tag{55–34}$$

where

f is the frequency in MHz,
X2 is the value at *f* =100 MHz. The value at *f* =100 MHz is referred to as the PSAELFEXT constant.

The PSAELFEXT constant is determined in 55.7.3.2.2 by the ratio of the PS AELFEXT to the insertion loss and a length correction term. The insertion loss dependent term maintains the required SNR ratio and the IL independent term enables a relaxation of the PS AELFEXT due the reduction in crosstalk coupling for lengths less than 100 m.

55.7.3.2.2 PSAELFEXT to insertion loss ratio requirements

To ensure reliable operation, a minimum insertion loss to alien crosstalk ratio shall be maintained. The PS AELFEXT requirement of 55.7.3.2.1 can be relaxed based on a reduction in the maximum insertion loss specified in 55.7.2.1 and a reduction in the AELFEXT coupling for cabling lengths less than 100 m.

The adjusted PSAELFEXT requirement is determined by first calculating the PSAELFEXT constant and utilizing the constant in the PSAELFEXT limit line model of Equation (55–35).

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The PSAELFEXT_constant shall be specified by the following equation:

$$\text{PSAELFEXT\_constant} = 37.9 - \left(\frac{10GBTIL(250\ \text{MHz}) - \overline{IL(250\ \text{MHz})}}{2.29} \right) - 10\log_{10}\left(\frac{L}{100}\right) \quad (dB) \quad (55\text{–}35)$$

where

$10GBTIL($250 MHz) is the link segment insertion loss at 250 MHz [Equation (55–11)],
IL(250 MHz) is the insertion loss of a link segment less than 100 m [Equation (55–27)] or the insertion loss of the supported cabling types in Table 55–17 at 250 MHz. For measurement based calculations, IL(250 MHz) shall be the average of the insertion loss of the 4-pairs at 250 MHz.
L is the length in meters of the link segment. The equation assumes coupling over 100 m of horizontal cable and cable cords. For measurement based calculations (e.g., field testing), L can derived from the measured insertion loss and substituted in Equation (55–35) as defined in Equation (55–36).

$$L = 2.77 \times (\text{measured insertion loss at 250 MHz}) \quad (55\text{–}36)$$

For insertion loss values less than 10 dB at 250 MHz the calculated PSAELFEXT_constant values that exceed 32.5 dB shall revert to a value of 32.5 dB.

The field testing of length and insertion loss are addressed in TIA TSB-155-A and ISO/IEC TR 24750.

Table 55–21 provides the calculated PSAELFEXT_constants for link segments of 100 m and 55 m.

Table 55–21—Calculated PS AELFEXT constants

Link segment distance	PS AELFEXT_constant (dB)	PS AELFEXT_constant_avg average of the 4-pairs (dB)	Insertion loss at 250 MHz (dB)
100 m	37.9	41.9	35.9
55 m	33.7	37.7	20.3

Table 55–22 provides the calculated PSAELFEXT_constants for the supported cabling types.

Table 55–22—Calculated PSAELFEXT constants for supported cabling types

Cabling	Insertion loss at 250 MHz (dB)	PSAELFEXT_constant (dB)	PSAELFEXT_constant_avg average of the 4-pairs (dB)
Category 6/ Class E	35.9[a], 20.3[b]	37.9[a], 33.7[b]	41.9[a], 37.7[a]
Class E_A / Category 6A	33.8	37	41
Class F	33.8	37	41

[a]Link segment length of 100 m.
[b]Link segment length of 55 m.

Table 55–23 provides the calculated PS AELFEXT at 250 MHz for the supported cabling types.

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Table 55–23—Calculated PS AELFEXT at 250 MHz for supported cabling types

Cabling	Insertion loss at 250 MHz (dB)	PS AELFEXT at 250 MHz (dB)
Category 6/ Class E	35.9[a], 20.3[b]	29.9[a], 25.7[b]
Class E_A / Category 6A	33.8	29.0
Class F	33.8	29.0

[a]Link segment length of 100 m.
[b]Link segment length of 55 m.

55.7.3.3 Alien crosstalk margin computation

The objective of alien crosstalk margin computation is to further characterize the alien crosstalk coupling "between" link segments. The alien crosstalk margin computation ensures the total combined PSAFEXT and PSANEXT coupled into a duplex channel is limited in order to maintain the minimum signal-to-noise ratio. The alien crosstalk margin computation can be applied in the event that the PSANEXT limits specified in 55.7.3.1.1 [Equation (55–23) and Equation (55–25)] or the PSAELFEXT limits specified in 55.7.3.2. [Equation (55–32) and Equation (55–34)] are not met. The alien crosstalk margin is specified for each of the individual 4-pairs as well as the average "across the 4-pairs".

The alien crosstalk margin is determined by the following algorithm:

Step 1. Determine the length of the disturbed link segment and the disturbing link segments using Equation (55–37).

$$L = 277 \times \mathrm{IL\_avg} \tag{55–37}$$

where

IL_*avg*is the average measured insertion loss at 250 MHz "across the 4-pairs" of each disturbed and disturbing link segment.
L is the length in meters for each disturbed and disturbing link segment derived from the measured insertion loss.

Step 2. Determine the minimum power backoff (dB) for each disturbed and disturbing link segment from Table 55–11. Power backoff schedule utilizing the calculated link segment length from Step 1 (e.g., from Table 55–11; a length of 30 m has a minimum power backoff of 10 dB).

Step 3. Determine the insertion loss backoff factor using Equation (55–38).

$$\mathrm{IL\_bof}_j = \mathrm{min\_PBO\_disturbing\ link}_j - \mathrm{min\_PBO\_disturbed\ link} \tag{55–38}$$

where

IL_*bof*$_j$is calculated as the difference between the minimum power backoff (dB) of the disturbing link j and the disturbed link segments determined in Step 2.

Step 4. Determine the PSANEXT and the PSAFEXT from the measured ANEXT and AFEXT and the insertion loss backoff factor for each disturbed pair N = 1, 2, 3, 4 of a link segment using Equation (55–39) and Equation (55–40) respectively.

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$$\text{PSANEXT}_N(f) = -10\log_{10}\sum_{j=1}^{m}\sum_{i=1}^{4} 10^{\frac{-(AN\_\text{pr(f)}_{i,j,N} + IL\_\text{bof}_j)}{10}} \quad \text{(dB)} \qquad (55\text{–}39)$$

$$\text{PSAFEXT}_N(f) = -10\log_{10}\sum_{j=1}^{m}\sum_{i=1}^{4} 10^{\frac{-(AF\_\text{pr(f)}_{i,j,N} + IL\_\text{bof}_j)}{10}} \quad \text{(dB)} \qquad (55\text{–}40)$$

where

$AN\_pr(f)_{i,j,N}$ is the measured ANEXT of the individual pair combination i (1 to 4) of the disturbing link j (1 to m) for each disturbed pair N.
$AF\_pr(f)_{i,j,N}$ is the measured AFEXT of the individual pair combination i (1 to 4) of the disturbing link j (1 to m) for each disturbed pair N.
IL_bof_j is the insertion loss backoff factor determined in Equation (55–38).

Step 5. Determine the individual-pair margin for each of the 4-pairs using Equation (55–41).

$$XWn(f) = -10\log_{10}\left(10^{\frac{\text{PSANEXT}_N(f)}{-10}} + 10^{\frac{\text{PSAFEXT}_N(f)}{-10}}\right) + 10\log_{10}\left(10^{\frac{AN\_ipl(f)+2.5}{-10}} + 10^{\frac{AF\_ipl(f)}{-10}}\right) \quad \text{(dB)} \qquad (55\text{–}41)$$

where: f is the frequency in MHz,

$XWn(f)$ is the individual-pair margin for each of the 4-pairs,

$\text{PSANEXT}_N(f)$ is the measured PSANEXT loss in dB in the frequency range $10 \le f \le 400$ determined in Equation (55–39) adjusted for the insertion loss power backoff,

$\text{PSAFEXT}_N(f)$ is the measured PSAFEXT loss in dB in the frequency range $10 \le f \le 400$ determined in Equation (55–40) adjusted for the insertion loss power backoff,

$AN\_ipl(f)$ is the individual-pair limit line for PSANEXT calculated using Equation (55–42). $AN\_ipl(f)$ is derived utilizing the average of the insertion loss of the 4-pairs at 250 MHz determined in Step 1 to calculate the PSANEXT constant using Equation (55–26).

$$AN\_\text{ipl}(f) = \begin{cases} \text{PSANEXT constant} - 10\log_{10}\left(\frac{f}{100}\right) & \text{(dB)} \quad 1 \le f \le 100 \\ \text{PSANEXT constant} - 15\log_{10}\left(\frac{f}{100}\right) & \text{(dB)} \quad 100 < f \le 500 \end{cases} \qquad (55\text{–}42)$$

$AF\_ipl(f)$ is the individual-pair line for PSAFEXT calculated using Equation (55–43) $AF\_ipl(f)$ is derived by adding the average of the measured insertion loss of the 4-pairs at 250 MHz determined in Step 1 to the PSAELFEXT limit line. The PSAELFEXT constant is derived using Equation (55–32) utilizing the average of the insertion loss of the 4-pairs at 250 MHz determined in Step 1.

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$$AF\_\text{ipl(f)} = (\text{ PSAEFEXT constant }) - 20\log_{10}(\frac{f}{100}) + IL\_\text{avg}(f)\ \ (dB)\ \ \ 1 \le f \le 500 \qquad (55\text{–}43)$$

NOTE—The 2.5 dB is the PSANEXT allowance for the peak-to-average difference across frequency.

Step 6. Determine the average value "across frequency" of XWn(f) from 10 MHz to 400 MHz, for each individual-pair of the 4-pair cabling using Equation (55–44).

$$XAWn = \frac{\int_{f=10}^{400} XWn(f)df}{390}(\text{dB}) \qquad (55\text{–}44)$$

where

f is the frequency in MHz,

XAWn is the average value "across frequency" for the individual-pair number n (n = 1,2,3,4).

Step 7. Determine the individual-pair margin as the minimum of the average value "across frequency" of each of the individual pairs of the 4-pair cabling determined from Step 2 using Equation (55–45).

$$Y_{\text{inp}} = \min(XAW1, XAW2, XAW3, XAW4)(\text{dB}) \qquad (55\text{–}45)$$

where

Y_{inp} is the individual-pair margin.

Step 8. Determine the power sum of the PSANEXT and PSAFEXT for each of the 4-pairs using Equation (55–46).

$$XXn(f) = 10\log_{10}\left(10^{\frac{AN(f)}{-10}} + 10^{\frac{AF(f)}{-10}}\right)(\text{dB}) \qquad (55\text{–}46)$$

where

f is the frequency in MHz,

XXn(f) is the power sum of the PSANEXT and PSAFEXT for each of the 4-pairs,

AN(f) is the measured PSANEXT loss in dB in the frequency range $10 \le f \le 400$ determined in Equation (55–39) adjusted for the insertion loss power backoff,

AF(f) is the measured PSAFEXT loss in dB in the frequency range $10 \le f \le 400$ determined in Equation (55–40) adjusted for the insertion loss power backoff.

Step 9. Determine the average of the power sum of the PSANEXT and PSAFEXT of the 4-pairs using Equation (55–47).

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$$XXavg(f) = \frac{\left(\sum_{i=1}^{n} XXi(f)\right)}{4} (\text{dB}) \quad (55–47)$$

where

XXavg(f) is the average of the power sum of the PSANEXT and PSAFEXT of the 4-pairs,

n is the number of individual pairs; *n* = 4.

Step 10. Determine the average margin using Equation (55–48).

$$XA(f) = -XXavg + 10\log_{10}\left(10^{\frac{AN\_avgl(f)}{-10}} + 10^{\frac{AF\_avgl(f)}{-10}}\right) \quad (\text{dB}) \quad (55–48)$$

where

XA(f) is the average margin,

AN_avgl(f) is the average limit line for PSANEXT calculated using Equation (55–49). AN_avgl(f) is derived using the PSANEXT constant determined in Step 5.

$$AN\_\text{avgl(f)} = \begin{cases} PSANEXT_{\text{constant}} + 3.5 - 10\log_{10}\left(\frac{f}{100}\right) & (\text{dB}) \quad 1 \le f \le 100 \\ PSANEXT_{\text{constant}} + 3.5 - 15\log_{10}\left(\frac{f}{100}\right) & (\text{dB}) \quad 100 < f \le 500 \end{cases} \quad (55–49)$$

where

f is the frequency in MHz,

AF_avgl(f) is the average limit line for PSAFEXT calculated using Equation (55–50). *AF_avgl(f)* is derived by adding the average of the measured insertion loss of the 4-pairs at 250 MHz determined in Step 1 to the PSAELFEXT limit line using the PSAELFEXT constant determined in Step 5.

$$AF\_avg1(f) = (\text{PSAELFEXT constant} + 4) - 20\log_{10}\left(\frac{f}{100}\right) + IL\_\text{avg}(f) \quad (\text{dB}) \quad 1 \le f \le 500 \quad (55–50)$$

Step 11. Determine the average margin as the average value across frequency of *XA(f)* using Equation (55–51).

$$Y_{\text{avg}} = \frac{\int_{f=10}^{400} XAfdf}{390} (\text{dB}) \quad (55–51)$$

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where

f is the frequency in MHz,
Y_{avg} is the average value "across frequency" of *XA(f)* from 10 to 400 MHz.

Step 12. Determine the alien crosstalk margin as the minimum value of the individual pair margin [Equation (55–45)] and the average margin [Equation (55–51)] using Equation (55–52).

$$YL = min(Y_{inp}, Y_{avg}) \text{ (dB)} \quad (55–52)$$

The alien crosstalk margin *YL* shall be greater than zero.

55.7.4 Noise environment

The 10GBASE-T noise environment consists of noise from many sources. The primary noise sources that impact the objective BER are the crosstalk and echo interference of a link segment, which are reduced to a small residual noise, and the noise coupled between the link segments referred to as alien crosstalk noise. The remaining noise sources, which are secondary sources, are discussed in the following. The 10GBASE-T noise environment consists of the following:

a) Echo from the local transmitter on the same duplex channel (cable pair). Echo is caused by the hybrid function used to achieve simultaneous bi-directional transmission of data and by impedance mismatches in the link segment. It is impractical to achieve the objective BER without using echo cancellation. Since the symbols transmitted by the local disturbing transmitter are available to the cancellation processor, echo interference can be reduced to a small residual noise using echo cancellation methods.
b) Near-end crosstalk (NEXT) interference from the local transmitters on the duplex channels (cable pairs) of the link segment. Each receiver experiences NEXT interference from three adjacent transmitters. NEXT cancellers are used to reduce the interference from each of the three disturbing transmitters to a small residual noise. NEXT cancellation is possible since the symbols transmitted by the three disturbing local transmitters are available to the cancellation processor.
c) Far-end crosstalk (FEXT) noise at a receiver is from three disturbing transmitters at the far end of the duplex channel (cable pairs) of the link segment. FEXT noise can be reduced through cross coupled equalizers although the symbols from the remote transmitters are not immediately available.
d) Intersymbol interference (ISI). ISI is the extraneous energy from one signaling symbol that interferes with the reception of another symbol on the same channel. 10GBASE-T supports the use of Tomlinson-Harashima Precoding as a mechanism to reduce the effects of ISI.
e) Noise from non-idealities in the duplex channel, transmitters, and receivers; for example, DAC/ADC non-linearity, electrical noise (shot and thermal), and non-linear channel characteristics. 10GBASE-T limits the effects of some of these non-idealities by a variety of PMA electrical specifications.
f) Noise coupled between link segments. Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. Since the transmitted symbols from the alien crosstalk noise sources are not available to the cancellation processor (they are in another cable), it is very difficult to cancel the alien crosstalk noise. To ensure robust operation the alien crosstalk is specified in 55.7.3.
g) The background noise for 10GBASE-T is expected not to exceed –150 dBm/Hz. A background noise limit of –150 dBm/Hz was assumed for determining the minimum signal-to-noise ratio.

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55.8 MDI specification

This subclause defines the MDI. The link topology requires a crossover function in a DTE-to-DTE connection. See 55.4.4 for a description of the automatic MDI/MDI-X configuration.

55.8.1 MDI connectors

Eight-pin connectors meeting the requirements of IEC 60603-7-4 (unscreened) or IEC 60603-7-5 (screened) shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figure 55–39 and Figure 55–40. The assignment of PMA signals to connector contacts for PHYs is shown in Table 55–24.

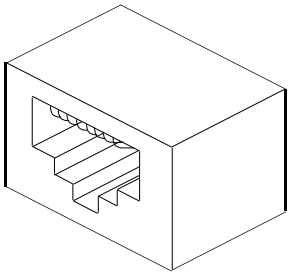

Figure 55–39—MDI connector

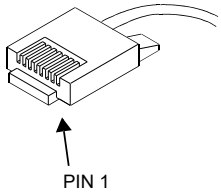

Figure 55–40—Balanced cabling connector

Table 55–24—Assignment of PMA signal to MDI and MDI-X pin-outs

Contact	MDI	MDI-X
1	BI_DA+	BI_DB+
2	BI_DA–	BI_DB–
3	BI_DB+	BI_DA+
4	BI_DC+	BI_DD+
5	BI_DC–	BI_DD–
6	BI_DB–	BI_DA–
7	BI_DD+	BI_DC+
8	BI_DD–	BI_DC–

55.8.2 MDI electrical specifications

The MDI connector (jack) when mated with a specified balanced cabling connector (plug) shall meet the FEXT requirements as specified in Equation (55–53):

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$$\text{FEXT loss} \geq 43.1 - 20\log_{10}(f/100) \quad \text{(dB)} \tag{55–53}$$

where f is the frequency over the range 1 MHz to 500 MHz between all contact pair combinations shown in Table 55–24.

No spurious signals shall be emitted onto the MDI when the PHY is held in power-down mode (as defined in 22.2.4.1.5), when released from power-down mode, or when external power is first applied to the PHY.

55.8.2.1 MDI return loss

The differential impedance at the MDI for each transmit/receive channel shall be such that any reflection due to differential signals incident upon the MDI from a balanced cabling having a nominal differential characteristic impedance of 100 Ω is attenuated, relative to the incident signal as per the relationship:

$$\text{Return loss} \geq \begin{cases} 16 & 1 \leq f \leq 40 \quad \text{(dB)} \\ 16 - 10\log_{10}(f/40) & 40 < f \leq 400 \quad \text{(dB)} \\ 6 - 30\log_{10}(f/400) & 400 < f \leq 500 \quad \text{(dB)} \end{cases} \tag{55–54}$$

where f is in MHz.

55.8.2.2 MDI impedance balance

Impedance balance is a measure of the impedance-to-ground difference between the two MDI contacts used by a duplex link channel and is referred to as common-mode-to-differential-mode impedance balance. The common-mode-to-differential-mode impedance balance, $Bal(f)$, of each channel of the MDI shall meet the relationship:

$$Bal(f) \geq \begin{cases} 48 & 1 \leq f < 30 \quad \text{(dB)} \\ 44 - 19.2\log_{10}\left(\frac{f}{50}\right) & 30 \leq f \leq 500 \quad \text{(dB)} \end{cases} \tag{55–55}$$

where f is the frequency in MHz when the transmitter is transmitting random or pseudo random data. Test-mode 4 may be used to generate an appropriate transmitter output. The impedance balance (in dB) is defined as:

$$Bal(f) = 20\log_{10}\left(\frac{E_{cm}(f)}{E_{dif}(f)}\right) - IL_{cal}(f) \quad \text{(dB)} \tag{55–56}$$

where E_{cm} is an externally applied common-mode sinusoidal voltage as shown in Figure 55–41, E_{dif} is the resulting differential waveform due only to the applied sine wave E_{cm} and not the transmitted data, and $IL_{cal}(f)$ is the coupling circuit common-mode insertion loss (in dB). The coupling circuit common-mode insertion loss is defined as:

$$IL_{\text{cal}}(f) = 20\log_{10}\left(\frac{E_{cin}(f)}{E_{cout}(f)}\right) \quad \text{(dB)} \tag{55–57}$$

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where E_{cin} and E_{cout} are test signals used to measure the coupling circuit common-mode insertion loss as shown in Figure 55–42.

The impedance balance is measured with a common-mode coupling circuit presenting a differential termination of 100 Ω and a common-mode termination of 50 Ω to the MDI pair under test as shown in Figure 55–41. The return loss for both differential and common terminations in the common-mode coupling circuit should be greater than 20 dB from 10 MHz to 500 MHz. The insertion loss IL_{cal} (in dB) of the common-mode coupling circuit can be measured with the test circuit shown in Figure 55–42.

NOTE 1—Triggered averaging can be used to separate the component due to the applied common-mode sine wave from the transmitted data component.
NOTE 2—The imbalance of the test equipment should be insignificant relative to the balance requirements.

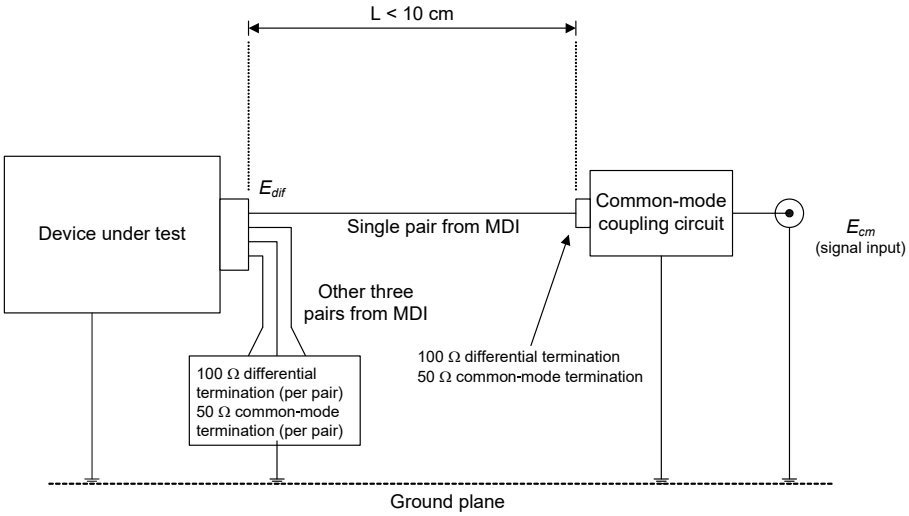

Figure 55–41—MDI impedance balance test circuit

The impedance balance may also be measured with a mixed mode four port network analyzer capable of measuring the common-mode voltage and differential mode voltage of a balanced port. Impedance balance is the S parameter measurement of Scd11 in dB at the MDI where two ports of the four port network analyzer are connected between two MDI contacts used by a duplex link channel and these two ports are configured as a single balanced port. For this test the PHY ground is connected to the network analyzer ground. The other two ports of the network analyzer are unconnected. The network analyzer should be capable of measuring Scd11 to at least –60 dB and should use a differential input impedance of 100 Ω and a common-mode impedance of 75 Ω.

During the test the PHY is connected to the MDI as in normal operation, but with the transmitter output disabled.

55.8.2.3 MDI fault tolerance

Each wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to any other wire within the 4-pair cable for an indefinite period of time and shall resume normal operation after the short circuit(s) are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

A 10GBASE-T PHY shall be able to sustain, without damage, connection to a PSE and shall not cause damage to the PSE as defined in 33.2.

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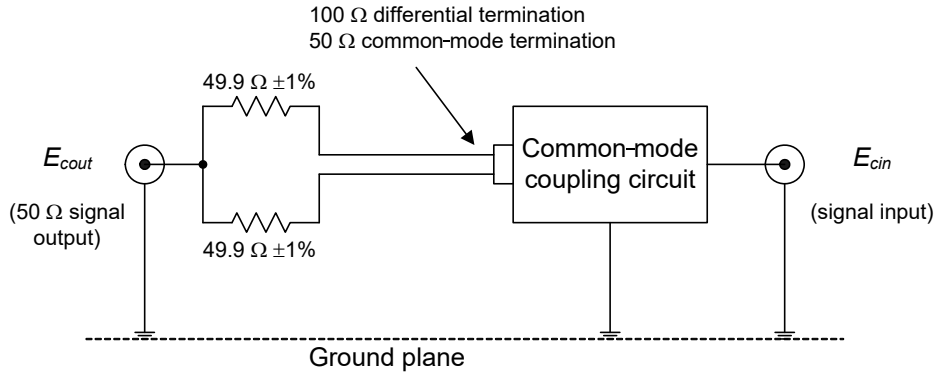

Figure 55–42— Impedance balance calibration circuit

Each wire pair shall withstand without damage a 1000 V common-mode impulse of either polarity. The shape of the impulse is 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060. See Figure 40–33 in 40.8.3.4.

55.9 Environmental specifications

55.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

55.9.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cabling systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards should be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures should be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

55.9.3 Installation and maintenance guidelines

It is recommended that sound installation practice, including screen management, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable. In addition, Annex 55B provides additional cabling guidelines for 10GBASE-T deployment on balanced copper cabling systems.

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It is a mandatory requirement that, during installation of the cabling plant, care be taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

55.9.4 Telephone voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 10GBASE-T. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the “battery” and ringing voltages. Although there is no universal standard, the following maximums generally apply.

a) Battery voltage to a telephone line is generally 56 V dc applied to the line through a balanced 400 Ω source impedance.
b) Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 V dc with a 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 10GBASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

55.9.5 Electromagnetic compatibility

A system integrating the 10GBASE-T shall comply with applicable local and national codes for the limitation of electromagnetic interference.

55.9.6 Temperature and humidity

A system integrating the 10GBASE-T is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

55.10 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability and units thereof
b) Power level in terms of maximum current drain (for external PHYs)
c) Port type (i.e., 10GBASE-T)
d) Any applicable safety warnings
e) EEE support
f) Fast retrain support

55.11 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of a 10GBASE-T PHY shall not exceed 25 600 BT. Transmit data delay is measured from the input of a given unit of data at the XGMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the

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input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the XGMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link. Equation (44–1) specifies the calculation of bit time per meter of electrical cable and Table 44–3 can also be used to convert electrical cable delay values specified relative to the speed of light or in nanoseconds per meter.

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55.12 Protocol implementation conformance statement (PICS) proforma for Clause 55—Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10GBASE-T[108]

The supplier of a protocol implementation that is claimed to conform to this clause shall complete the protocol implementation conformance statement (PICS) proforma listed in the following subclauses.

Instructions for interpreting and filling out the PICS proforma may be found in Clause 21.

55.12.1 Identification

55.12.1.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

55.12.1.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 55, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 10GBASE-T
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exceptions items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[108] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so it can be used for its intended purpose and may further publish the completed PICS.

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55.12.2 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
XGE	XGMII compatibility interface	46, 55.1.5	O	Yes [ ] No [ ]	Compatibility interface is supported
*LT	Support of loop timing		O	Yes [ ] No [ ]	
*EEE	Support of EEE capability		O	Yes [ ] No [ ]	55.1.3.3
*FR	Support of Fast Retrain capability		O	Yes [ ] No [ ]	55.4.2.5.15
*INS	Installation / cabling	55.7	O	Yes [ ] No [ ]	Items marked with INS include installation practices and cabling specifications not applicable to a PHY manufacturer

55.12.3 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Status	Support	Value/Comment
PCT1	PCS Transmit function state diagram	55.3.2.2	M	Yes [ ]	See Figure 55–16
PCT2	PCS Transmit function state diagram with EEE states	55.3.2.2	EEE:M	Yes [ ]	See Figure 55–16 and Figure 55–17
PCT3	SEND_Z Operation	55.3.2.2	M	Yes [ ]	PMA_TXMODE.indication message
PCT4	SEND_N Operation	55.3.2.2	M	Yes [ ]	PMA_TXMODE.indication message
PCT5	SEND_T Operation	55.3.2.2	M	Yes [ ]	PMA_TXMODE.indication message
PCT6	PCS Transmit bit ordering	55.3.2.2.4	M	Yes [ ]	See Figure 55–6 and Figure 55–8
PCT7	Invalid control code handling	55.3.2.2.6	M	Yes [ ]	
PCT8	/I/ insertion and deletion	55.3.2.2.9	M	Yes [ ]	
PCT9	/LI/ insertion and deletion	55.3.2.2.10	EEE:M	Yes [ ]	
PCT10	/O/ deletion	55.3.2.2.13	M	Yes [ ]	
PCT11	Scrambler as MASTER	55.3.2.2.16	M	Yes [ ]	
PCT12	Scrambler as SLAVE	55.3.2.2.16	M	Yes [ ]	
PCT13	CRC8	55.3.2.2.17	M	Yes [ ]	See Figure 55–11
PCT14	LDPC encoding	55.3.2.2.18	M	Yes [ ]	Generator matrix is described in Annex 55A
PCT15	DSQ128 mapping	55.3.2.2.19	M	Yes [ ]	
PCT16	EEE Transmit function state diagram	55.3.2.2.22	EEE:M	Yes [ ]	See Figure 55–20

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Item	Feature	Subclause	Status	Support	Value/Comment
PCT17	LP_IDLE input to scrambler during LPI mode	55.3.2.2.22	EEE:M	Yes [ ]	
PCT18	lpi_tx_mode control	55.3.2.2.22	EEE:M	Yes [ ]	
PCT19	PCS test pattern mode	55.3.3	M	Yes [ ]	See Figure 55–6
PCT20	PMA training - MASTER scrambler	55.3.4	M	Yes [ ]	
PCT21	PMA training - SLAVE scrambler	55.3.4	M	Yes [ ]	
PCT22	PMA training scrambler initial state	55.3.4	M	Yes [ ]	In no case shall the scrambler state be initialized to all zeros
PCT23	LPI active pair and refresh_active signals	55.3.5.1	EEE:M	Yes [ ]	
PCT24	Alert signaling in place of refresh signaling	55.3.5.3	EEE:M	Yes [ ]	
PCT25	Slave synchronization	55.3.5.1	EEE:M	Yes [ ]	
PCT26	Quiet launch power	55.3.5.2	EEE:M	Yes [ ]	
PCT27	LPI sleep timer	55.3.6.2.3	EEE:M	Yes [ ]	
PCT28	LPI alert timer	55.3.6.2.3	EEE:M	Yes [ ]	
PCT29	LPI wake timer	55.3.6.2.3	EEE:M	Yes [ ]	
PCT30	LPI rx wake timer	55.3.6.2.3	EEE:M	Yes [ ]	
PCT31	LPI tx wake timer	55.3.6.2.3	EEE:M	Yes [ ]	
PCT32	LPI scrambler	55.3.5.3	EEE:M	Yes [ ]	The training sequence without periodic re-initialization described in 55.3.5 shall be used
PCT33	Disable scrambler reinitialization	55.3.5.3	EEE:M	Yes [ ]	
PCT34	Refresh using THP	55.3.5.3	EEE:M	Yes [ ]	
PCT35	Reset THP at the start of refresh	55.3.5.3	EEE:M	Yes [ ]	
PCT36	Master alert on pair A, other pairs silent	55.3.5.3	EEE:M	Yes [ ]	
PCT37	Slave alert on pair C, other pairs silent	55.3.5.3	EEE:M	Yes [ ]	
PCT38	Inactive pairs transmit zeros	55.3.5.3	EEE:M	Yes [ ]	
PCT39	ENCODE function	55.3.6.2.4	M	Yes [ ]	Encode the block as specified in 55.3.2.2.2
PCT40	PCS loopback setup	55.3.7.3	M	Yes [ ]	

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55.12.3.1 PCS Receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR1	PCS Receive function state diagram	55.3.2.3	M	Yes [ ]	See Figure 55–18 and state variables as specified in 55.3.6.2.
PCR2	PCS Receive bit ordering	55.3.2.3.1	M	Yes [ ]	See Figure 55–7
PCR3	Descrambling as MASTER	55.3.2.3.2	M	Yes [ ]	
PCR4	Descrambling as SLAVE	55.3.2.3.2	M	Yes [ ]	
PCR5	PMA training descrambler - MASTER	55.3.4.3	M	Yes [ ]	
PCR6	PMA training descrambler - SLAVE	55.3.4.3	M	Yes [ ]	
PCR7	DECODE operation	55.3.6.2.4	M	Yes [ ]	Decode the block as specified in 55.3.4
PCR8	LFER monitor	55.3.6.3	M	Yes [ ]	See state diagrams in Figure 55–15, Figure 55–16 and Figure 55–18.

55.12.3.2 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	PCS Reset function	55.3.2.1	M	Yes [ ]	

55.12.4 Physical Medium Attachment (PMA)

Item	Feature	Subclause	Status	Support	Value/Comment
PMF1	PMA Reset function	55.4.2.1	M	Yes [ ]	
PMF2	PMA transmission	55.4.2.2	M	Yes [ ]	
PMF3	Transmitter clocking	55.4.2.2	M	Yes [ ]	All driven by TX_TCLK
PMF4	PMA Transmit mapping	55.4.2.2	M	Yes [ ]	Per mathematical description given in 55.4.3.1
PMF5	PMA Transmit electrical compliance	55.4.2.2	M	Yes [ ]	See PMA electrical specifications given in 55.5
PMF6	Clocking as MASTER	55.4.2.2	M	Yes [ ]	Source the transmit clock TX_TCLK from a local clock
PMF7	Clocking as SLAVE in loop timed mode	55.4.2.2	M	Yes [ ]	Source the transmit clock TX_TCLK from the recovered clock

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Item	Feature	Subclause	Status	Support	Value/Comment
PMF8	Transmit fault mapping	55.4.2.2	O	Yes [ ]	Contribute to the transmit fault bit as specified in 45.2.1.7.4
PMF9	Generates alert signal	55.4.2.2	EEE:M	Yes [ ]	Generates the alert signal defined in 55.4.2.2.1
PMF10	Generates link failure signaling	55.4.2.2	FR:M	Yes [ ] No [ ]	Generates the link failure signal defined in 55.4.2.2.2
PMF11	PMA Receive function performance	55.4.2.4	M	Yes [ ]	LDPC frame error ratio of less than 3.2×10^{-9}
PMF12	Receive fault mapping	55.4.2.4	O	Yes [ ]	Contribute to the receive fault bit as specified in 45.2.1.7.5
PMF13	Implement alert_detect	55.4.2.4	EEE:M	Yes [ ]	Generates alert_detect when the alert signal is detected at the receiver
PMF14	Detect link failure signaling	55.4.2.4	FR:M	Yes [ ] No [ ]	Sets link_fail_detect to true when the link failure signal is detected
PMF15	PHY Control function	55.4.2.5	M	Yes [ ]	See state diagram in Figure 55–28 and state diagrams in Figure 55–29 and Figure 55–30
PMF16	InfoField	55.4.2.5	M	Yes [ ]	All subclauses from 55.4.2.5.1 to 55.4.2.5.13
PMF17	THP initialization	55.4.2.5.14	M	Yes [ ]	Last 16 symbols of PMA_Coeff_Exch
PMF18	PBO exchange	55.4.2.5.14	M	Yes [ ]	
PMF19	Slave PBO setting	55.4.2.5.14	M	Yes [ ]	Slave's PBO final setting within two levels (4 dB) of the MASTER's PBO level
PMF20	THP coefficient exchange	55.4.2.5.14	M	Yes [ ]	
PMF21	Recommended startup sequence timing	55.4.2.5.14	O	Yes [ ] No [ ]	See Table 55–9
PMF22	Implements fast retrain state diagram	55.4.2.5.15	FR:M	Yes [ ] No [ ]	
PMF23	Behavior after fast retrain request	55.4.2.5.15	FR:M	Yes [ ] No [ ]	Transmit PAM2 within 9 LDPC frame periods following link failure request
PMF24	Behavior after fast retrain signal detection	55.4.2.5.15	FR:M	Yes [ ] No [ ]	Transmit PAM2 within 9 LDPC frame periods following link failure signal detection
PMF25	Link Monitor	55.4.2.6	M	Yes [ ]	See state diagram in Figure 55–31
PMF26	Refresh monitor state diagram	55.4.2.7	EEE:M	Yes [ ] No [ ]	Implements state diagram of Figure 55–32
PMF27	Recommended fast retrain sequence timing	55.4.2.5.15	FR:O	Yes [ ] No [ ]	See Table 55–10

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Item	Feature	Subclause	Status	Support	Value/Comment
PMF28	Clock Recovery function	55.4.2.8	M	Yes [ ]	
PMF29	MDIX for EEE refreshes and alert	55.4.4	EEE:M	Yes [ ]	
PMF30	Symbol response	55.4.3.1	M	Yes [ ]	Per electrical specifications given in 55.5
PMF31	THP filter coefficient setting	55.4.3.1	M	Yes [ ]	Fixed after startup
PMF32	PMA Transmit power backoff settings	55.4.3.1	M	Yes [ ]	
PMF33	Minimum power backoff requested	55.4.3.1	M	Yes [ ]	Per Table 55–11
PMF34	Automatic configuration	55.4.4	M	Yes [ ]	Comply with the specifications of 40.4.4.1 and 40.4.4.2
PMF35	Pair/Polarity swap detection and correction	55.4.4	M	Yes [ ]	
PMF36	PMA_CONFIG.indication generation	55.4.5.1	M	Yes [ ]	
PMF37	Maxwait_timer expiration	55.4.5.2	M	Yes [ ]	
PMF38	Minwait_timer expiration	55.4.5.2	M	Yes [ ]	

55.12.5 Management interface

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	Support for Auto-Negotiation	55.6.1	M	Yes [ ]	See Clause 28
MF2	MASTER and SLAVE operation	55.6.1	M	Yes [ ]	Capable of operating either as MASTER or SLAVE
MF3	Extended Next Page support	55.6.1	M	Yes [ ]	
MF4	Optimized FLP timing	55.6.1	M	Yes [ ]	
MF5	Management registers	55.6.1.1	M	Yes [ ]	As defined in Table 55–14
MF6	10GBASE-T Extended Next Page bit assignments	55.6.1.2	M	Yes [ ]	As defined in Table 55–15
MF7	EEE advertisement	55.6.1.2	EEE:M	Yes [ ]	As defined in Table 55–15
MF8	Fast retrain ability advertisement	55.6.1.2	FR:M	Yes [ ]	As defined in Table 55–15
MF9	MASTER-SLAVE resolution with both or neither devices supporting loop timing	55.6.2	M	Yes [ ]	As defined in Table 55–16
MF10	MASTER-SLAVE resolution with one device supporting loop timing	55.6.2	M	Yes [ ]	Device supporting loop timing forced to SLAVE

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Item	Feature	Subclause	Status	Support	Value/Comment
MF11	Resolution completion	55.6.2	M	Yes [ ]	Successful completion of resolution treated as MASTER-SLAVE configuration resolution complete.
MF12	Seed counter	55.6.2	M	Yes [ ]	Counter provided to track number of seed attempts
MF13	Counter set to zero at startup	55.6.2	M	Yes [ ]	
MF14	Counter increment	55.6.2	M	Yes [ ]	
MF15	Counter reset	55.6.2	M	Yes [ ]	After resolution is complete
MF16	Bit 7.33.15 set to zero after resolution is complete	55.6.2	M	Yes [ ]	After resolution is complete
MF17	Resolution fault declared	55.6.2	M	Yes [ ]	After generation of seven seeds
MF18	MASTER-SLAVE fault condition	55.6.2	M	Yes [ ]	Condition occurs when both devices manually select MASTER or SLAVE
MF19	MASTER-SLAVE fault condition bit	55.6.2	M	Yes [ ]	Set to one upon fault condition
MF20	MASTER-SLAVE fault resolution	55.6.2	M	Yes [ ]	Fault condition treated as MASTER-SLAVE resolution complete
MF21	MASTER-SLAVE fault condition indication	55.6.2	M	Yes [ ]	link_status_10GigT set to FAIL

55.12.6 PMA electrical specifications

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	Electrical isolation	55.5.1	M	Yes [ ]	Conforms to J.1
PME2	Test modes supported	55.5.2	M	Yes [ ]	
PME3	Test mode enablement	55.5.2	M	Yes [ ]	Per management register settings shown in Table 55–12
PME4	The test modes only change the data symbols	55.5.2	M	Yes [ ]	
PME5	Provide a means to enable the test modes	55.5.2	O	Yes [ ]	Mandatory for PHYs without MDIO
PME6	Test mode 1 operation	55.5.2	M	Yes [ ]	
PME7	Test mode 2 operation	55.5.2	M	Yes [ ]	
PME8	Test mode 3 operation, pair D	55.5.2	LT:M	Yes [ ] N/A [ ]	Mandatory for PHY that supports loop timing
PME9	Test mode 3 operation, pairs A, B and C	55.5.2	M	Yes [ ]	Transmit silence

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Item	Feature	Subclause	Status	Support	Value/Comment
PME10	Test mode 4 waveform	55.5.2	M	Yes [ ]	Tones per Table 55–13
PME11	Test mode 4 levels	55.5.2	M	Yes [ ]	
PME12	Test mode 5 operation	55.5.2	M	Yes [ ]	
PME13	Test mode 6 operation	55.5.2	M	Yes [ ]	
PME14	Test mode 7 operation	55.5.2	M	Yes [ ]	
PME15	Text fixture 3 isolation	55.5.2	M	Yes [ ]	>30 dB between signals on any of {pairs A, B, C} and pair D
PME16	Transmitter nominal load	55.5.3	M	Yes [ ]	
PME17	AC-coupling to the MDI	55.5.3	M	Yes [ ]	
PME18	Droop test	55.5.3.1	M	Yes [ ]	
PME19	SFDR of transmitter	55.5.3.2	M	Yes [ ]	
PME20	Transmitter jitter as MASTER	55.5.3.3	M	Yes [ ]	
PME21	Transmitter jitter as loop-timed SLAVE	55.5.3.3	LT: M	N/A [ ] Yes [ ]	Applicable only if loop timing is supported
PME22	Transmit power level	55.5.3.4	M	Yes [ ]	
PME23	Transmitter PSD	55.5.3.4	M	Yes [ ]	
PME24	MASTER symbol rate	55.5.3.5	M	Yes [ ]	
PME25	Maximum short term rate of frequency variation during LPI	55.5.3.5	EEE:M	Yes [ ]	Less than 0.1 ppm/s
PME26	Maximum short term rate of frequency variation when switching to and from LPI	55.5.3.5	EEE:M	Yes [ ]	Less than 0.1 ppm/s
PME27	BER over a 55.7 compliant link	55.5.4.1	M	Yes [ ]	
PME28	Receiver frequency tolerance	55.5.4.2	M	Yes [ ]	
PME29	Alien noise tolerance	55.5.4.4	M	Yes [ ]	

55.12.7 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	MDI compatibility	55.7	M	Yes [ ]	
LKS2	Insertion loss of each duplex channel	55.7.2.1	M	Yes [ ]	See Equation (55–11)
LKS3	Return loss	55.7.2.3	M	Yes [ ]	See (55–12)
LKS4	NEXT loss within pairs in a link segment	55.7.2.4.1	M	Yes [ ]	See (55–13)
LKS5	Power sum NEXT loss	55.7.2.4.2	M	Yes [ ]	See (55–14)
LKS6	Worst pair ELFEXT loss	55.7.2.4.4	M	Yes [ ]	See (55–18)

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Item	Feature	Subclause	Status	Support	Value/Comment
LKS7	Power sum ELFEXT loss	55.7.2.4.5	M	Yes [ ]	See (55–20)
LKS8	Propagation delay	55.7.2.5	M	Yes [ ]	
LKS9	Delay skew	55.7.2.6	M	Yes [ ]	
LKS10	Delay skew change	55.7.2.6	M	Yes [ ]	
LKS11	Power sum ANEXT loss	55.7.3.1.1	M	Yes [ ]	See (55–23)
LKS12	Average PS ANEXT loss	55.7.3.1.1	M	Yes [ ]	See (55–25)
LKS13	PSANEXT_constant	55.7.3.1.2	M	Yes [ ]	See (55–26)
LKS14	IL(250) used in PSANEXT_ constant equation	55.7.3.1.2	M	Yes [ ]	Actual measured insertion loss at 250 MHz
LKS15	PS AELFEXT loss	55.7.3.2.1	M	Yes [ ]	See (55–32)
LKS16	Average PS AELFEXT loss	55.7.3.2.1	M	Yes [ ]	See (55–34)
LKS17	PSAELFEXT_constant	55.7.3.2.2	M	Yes [ ]	See (55–35)
LKS18	IL(250) used in PSAELFEXT_ constant equation	55.7.3.2.2	M	Yes [ ]	Actual measured insertion loss at 250 MHz
LKS19	Alien crosstalk margin *YL*	55.7.3.3	M	Yes [ ]	Greater than zero

55.12.8 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	55.8.1	M	Yes [ ]	Eight-pin connectors meeting the requirements of IEC 60603-7-4 (unscreened) or IEC 60603-7-5 (screened)
MDI2	Cabling connector	55.8.1	M	Yes [ ]	Plug
MDI3	PHY connector	55.8.1	M	Yes [ ]	Jack (as opposed to plug)
MDI4	MDI connector jack plus plug performance	55.8.2	M	Yes [ ]	
MDI5	Mated MDI connector FEXT loss	55.8.2	M	Yes [ ]	Per (55–53)
MDI6	MDI power down	55.8.2	M	Yes [ ]	
MDI7	MDI return loss	55.8.2.1	M	Yes [ ]	
MDI8	MDI impedance balance	55.8.2.2	M	Yes [ ]	
MDI9	MDI fault tolerance to short circuits	55.8.2.3	M	Yes [ ]	No damage with an indefinite short
MDI10	Recovery from short	55.8.2.3	M	Yes [ ]	
MDI11	Short circuit current	55.8.2.3	M	Yes [ ]	Less than 300 mA

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Item	Feature	Subclause	Status	Support	Value/Comment
MDI12	Connection to PSE	55.8.2.3	M	Yes [ ]	No damage to PHY
MDI13	Connection to PSE	55.8.2.3	M	Yes [ ]	No damage to PSE
MDI14	Common-mode impulse tolerance	55.8.2.3	M	Yes [ ]	1000 V common-mode impulse of either polarity

55.12.9 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ENV1	Conformance to safety specifications	55.9.1	M	Yes [ ]	Conforms to J.2
ENV2	Installation isolation integrity	55.9.3	INS:M	N/A [ ] Yes [ ]	No electrical contact with unintended conductors or ground
ENV3	Phone voltage immunity	55.9.4	M	Yes [ ]	
ENV4	Electromagnetic compatibility	55.9.5	INS:M	N/A [ ] Yes [ ]	With local and national codes

55.12.10 Timing requirements

Item	Feature	Subclause	Status	Support	Value/Comment
TR1	Delay	55.11	M	Yes [ ]	

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56. Introduction to Ethernet for subscriber access networks

56.1 Overview

Ethernet for subscriber access networks, also referred to as "Ethernet in the First Mile," or EFM, combines a minimal set of extensions to the IEEE 802.3 Media Access Control (MAC) and MAC Control sublayers with a family of Physical Layers. These Physical Layers include optical fiber and voice grade copper cable Physical Medium Dependent sublayers (PMDs) for point-to-point (P2P) connections in subscriber access networks. EFM also introduces the concept of Ethernet Passive Optical Networks (EPONs), in which a point-to-multipoint (P2MP) network is implemented over an optical distribution network (ODN), along with extensions to the MAC Control sublayer and Reconciliation sublayer as well as optical fiber PMDs to support this topology. Furthermore, EFM introduces the concept of EPON Protocol over Coax (EPoC) networks, in which a P2MP network is implemented over a coax cable distribution network (CCDN), along with extensions to the MAC Control sublayer and Reconciliation sublayer as well as EPoC PMDs to support this topology.

In addition, a mechanism for network Operations, Administration, and Maintenance (OAM) is included to facilitate network operation and troubleshooting.

The relationships between these EFM elements and the ISO/IEC Open System Interconnection (OSI) reference model are shown in Figure 56–1 and Figure 56–2 for point-to-point topologies, Figure 56–3 for 1G-EPON topologies, Figure 56–4 for 10/10G-EPON topologies, Figure 56–5 for 10/1G-EPON topologies, Figure 56–6 for EPoC topologies, and Figure 56–7 for Nx25G-EPON topologies.

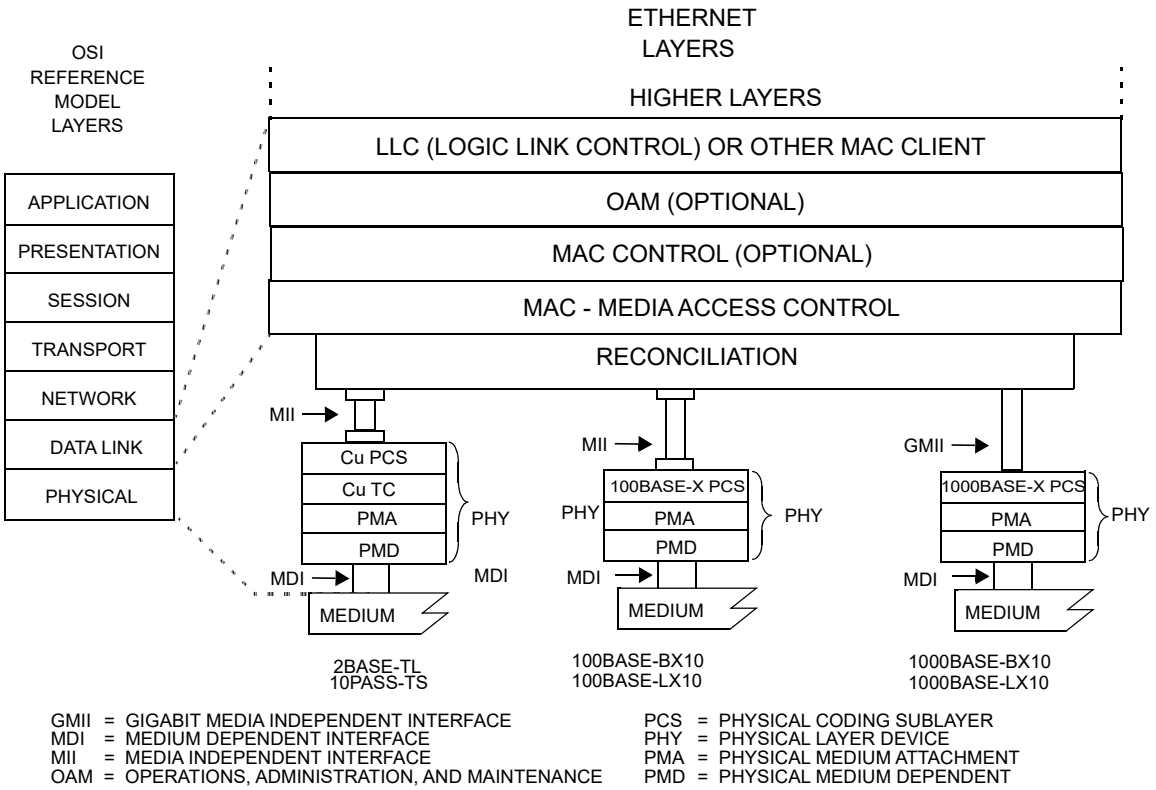

Figure 56–1—Architectural positioning of EFM: P2P Topologies

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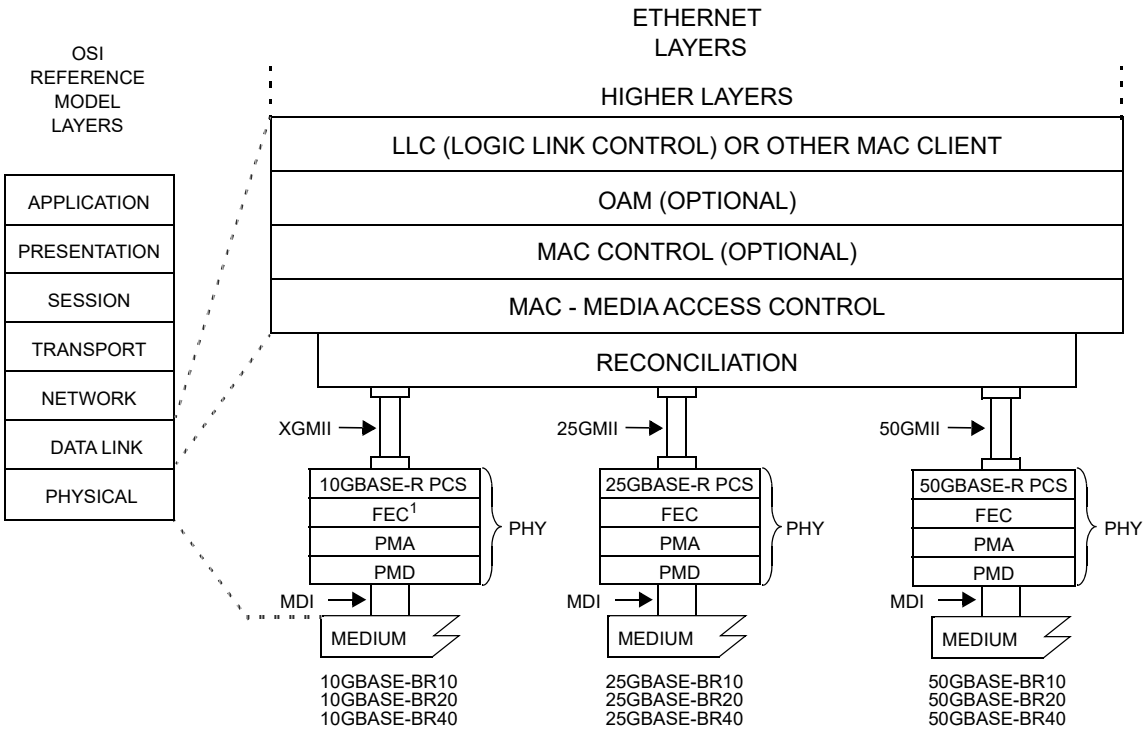

FEC = FORWARD ERROR CORRECTION
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
50GMII = 50 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION, AND MAINTENANCE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 56–2—Architectural positioning of EFM: higher rate P2P topologies

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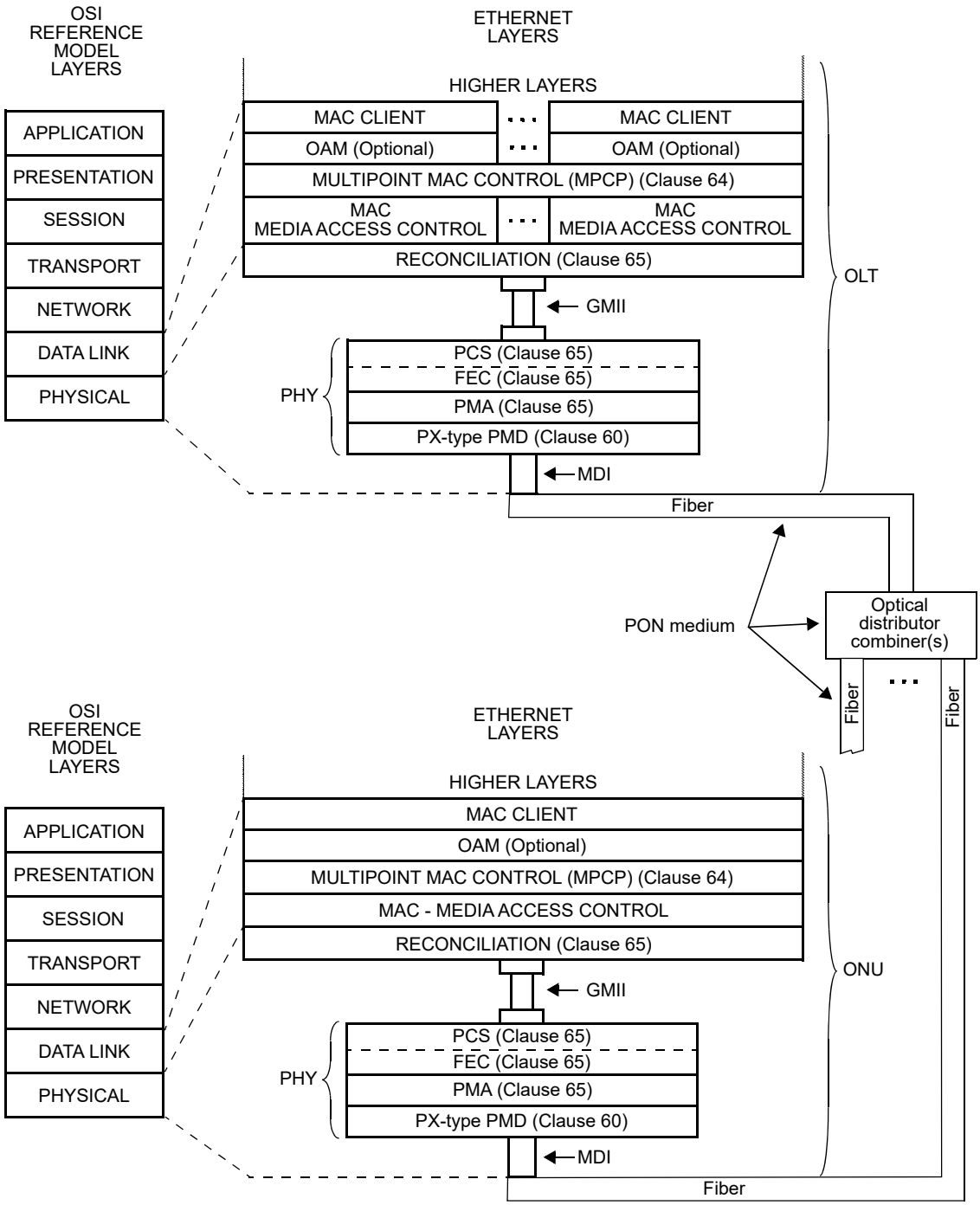

GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 56–3—Architectural positioning of EFM:
P2MP 1G-EPON architecture (1 Gb/s downstream, 1 Gb/s upstream)

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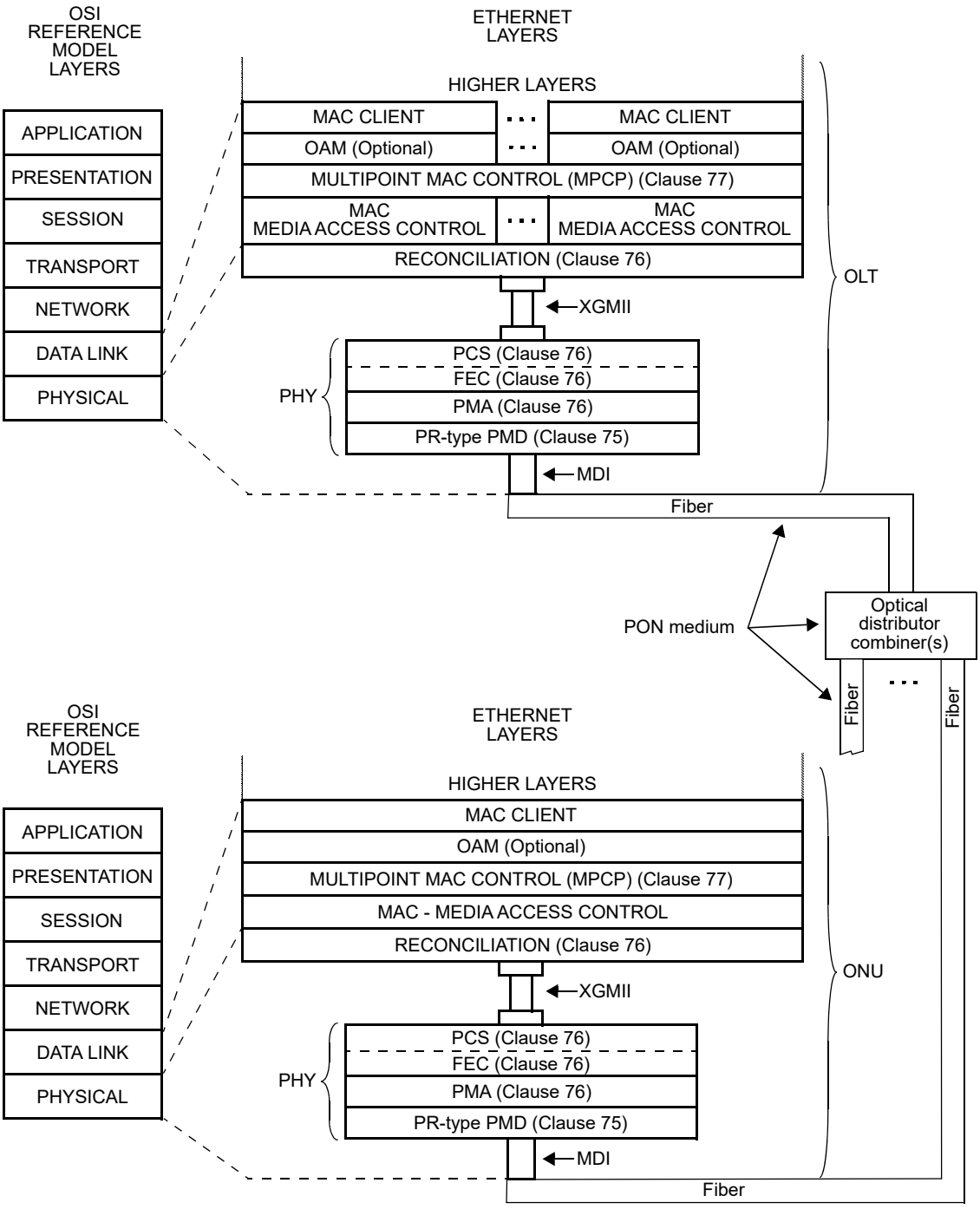

XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL

ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 56–4—Architectural positioning of EFM: P2MP 10/10G–EPON architecture (10 Gb/s downstream, 10 Gb/s upstream)

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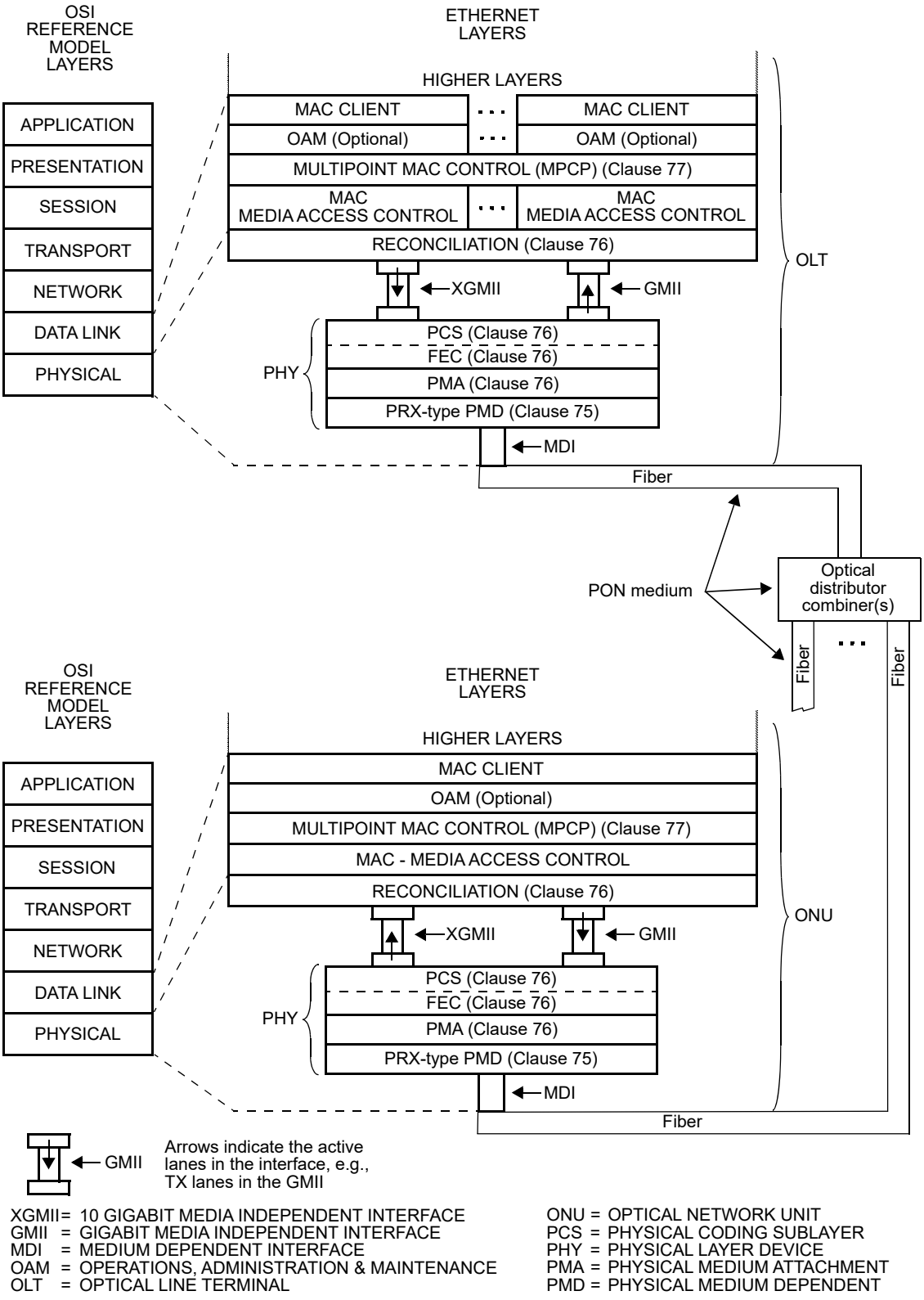

Figure 56–5—Architectural positioning of EFM: P2MP 10/1G–EPON architecture (10 Gb/s downstream, 1 Gb/s upstream)

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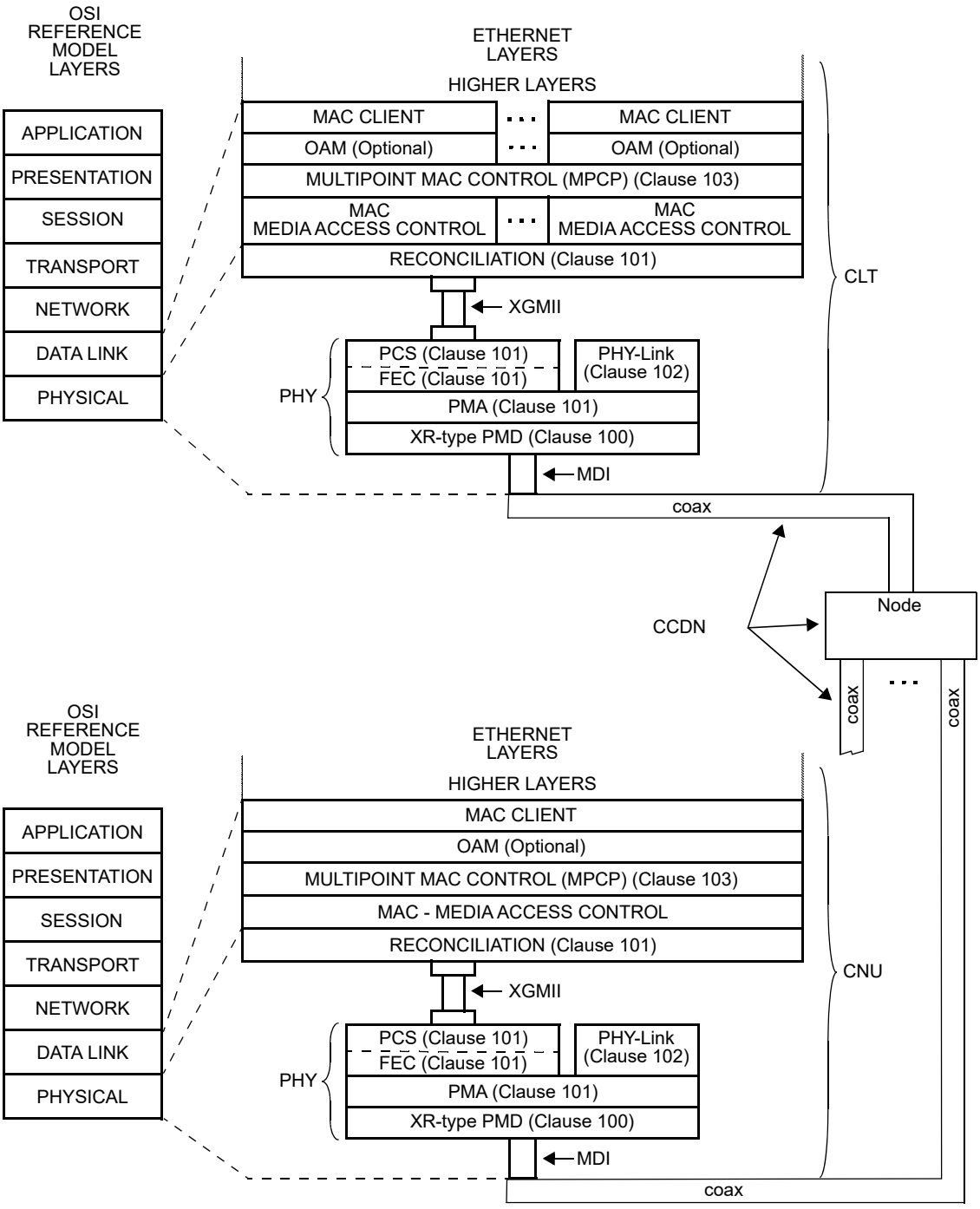

XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
CCDN= COAX CABLE DISTRIBUTION NETWORK
CLT = COAXIAL LINE TERMINAL
CNU = COAXIAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 56–6—Architectural positioning of EFM:
P2MP EPoC architecture (up to 10 Gb/s downstream, up to 1.6 Gb/s upstream)

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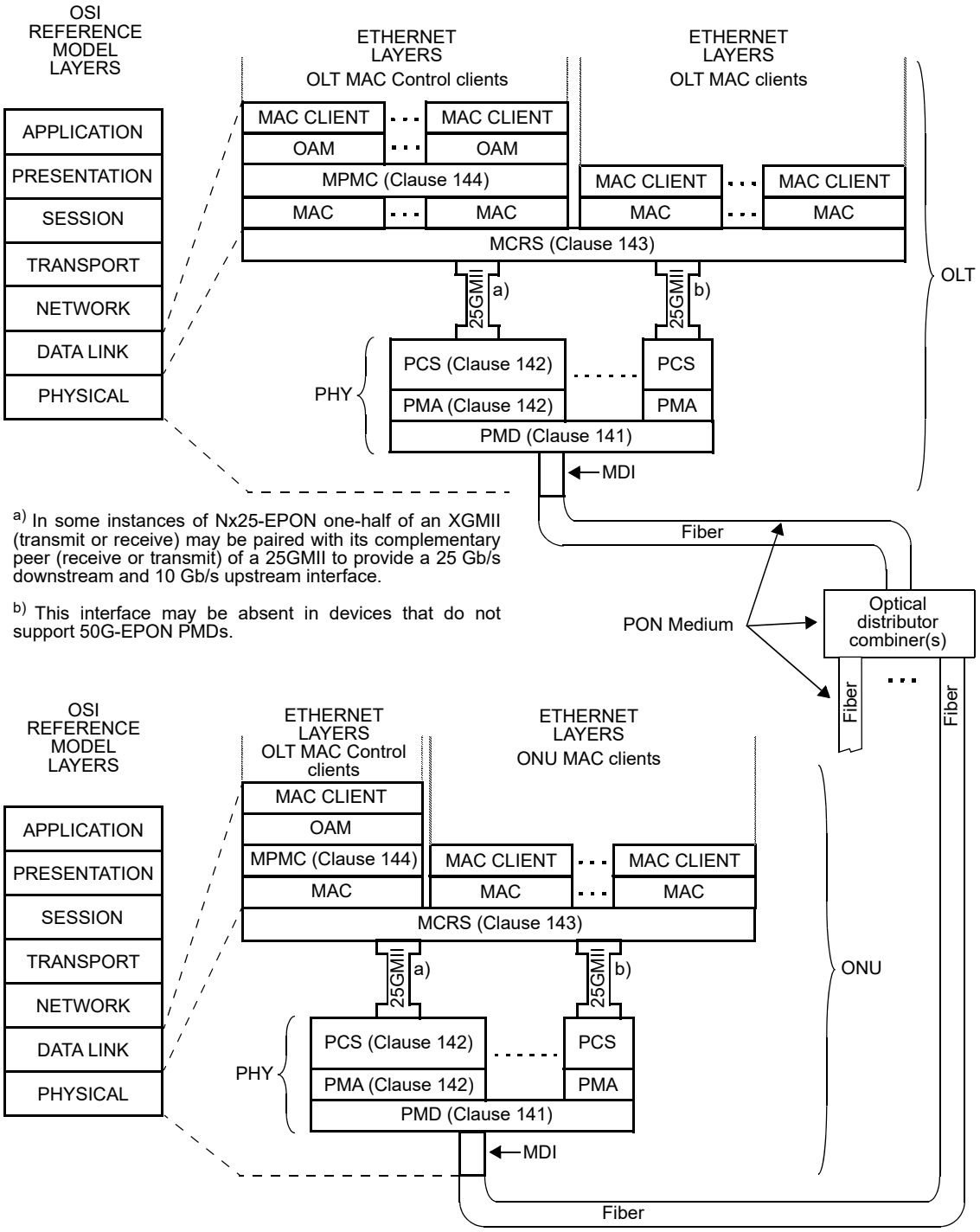

[a] In some instances of Nx25-EPON one-half of an XGMII (transmit or receive) may be paired with its complementary peer (receive or transmit) of a 25GMII to provide a 25 Gb/s downstream and 10 Gb/s upstream interface.

[b] This interface may be absent in devices that do not support 50G-EPON PMDs.

25GMII=25 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
MCRS= MULTI-CHANNEL RECONCILIATION SUBLAYER
MPMC= MULTI-POINT MAC CONTROL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 56–7—Architectural positioning of EFM: P2MP Nx25G-EPON architecture

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An important characteristic of EFM is that only full duplex links are supported. A simplified full duplex MAC is defined in Annex 4A for use in EFM networks. P2MP applications use this simplified full duplex MAC. EFM Copper applications may use either this simplified full duplex MAC or the Clause 4 MAC operating in half duplex mode as described in 61.1.4.1.2. All other EFM P2P applications may use either this simplified full duplex MAC or the Clause 4 MAC operating in full duplex mode.

The EFM architecture is further extended in:

— Clause 75 and Clause 76 by the addition of 10G–EPON.
— Clause 100, Clause 101, and Clause 102 by the addition of EPoC.
— Clause 141, Clause 142, and Clause 143 by the addition of Nx25G-EPON.

56.1.1 Summary of P2P sublayers

EFM P2P supports operation at several different bit rates, depending on the characteristics of the underlying medium.

56.1.1.1 P2P fiber media

The 100BASE-X Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayers are used to support a bit rate of 100 Mb/s as defined in 66.1. 100BASE-LX10 extends the reach of 100BASE-X to achieve 10 km over conventional single-mode two-fiber cabling.

The 1000BASE-X PCS and PMA sublayers are used to support a bit rate of 1000 Mb/s as defined in 66.2.

The 10GBASE-R PCS, RS-FEC, and PMA sublayers are used to support a bit rate of 10 Gb/s as defined in Clause 158.

The 25GBASE-R PCS, RS-FEC, and PMA sublayers are used to support a bit rate of 25 Gb/s as defined in Clause 159.

The 50GBASE-R PCS, RS-FEC, and PMA sublayers are used to support a bit rate of 50 Gb/s as defined in Clause 160.

56.1.1.2 P2P copper media

The P2P copper links support a variety of bit rates, depending on the span and the signal-to-noise ratio (SNR) characteristics of the medium as described in Clause 61 and Clause 63.

The 2BASE-TL P2P link supports a nominal bit rate of 2 Mb/s at a nominal reach of 2700 meters (see Annex 63B for a more detailed discussion of bit rates and reach).

The 10PASS-TS P2P link supports a nominal bit rate of 10 Mb/s at a nominal reach of 750 meters (see Annex 62B for a more detailed discussion of bit rates and reach).

56.1.2 Summary of P2MP sublayers

For P2MP optical fiber topologies, EFM supports the following systems:

a) PON with a nominal MAC data rate of 1 Gb/s in both downstream and upstream directions (1G-EPON), shared amongst the population of Optical Network Units (ONUs) attached to the P2MP topology. The P2MP PHYs use the 1000BASE-PX Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA) sublayer defined in Clause 65 and an optional forward error correction (FEC) function defined in Clause 65.
b) PON with a nominal MAC data rate of 10 Gb/s in both the downstream and upstream directions (10/10G-EPON) as well as PON with the nominal MAC data rate of 10 Gb/s in the downstream direction and 1 Gb/s in the upstream direction (10/1G-EPON), shared amongst the population of

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ONUs attached to the P2MP topology, and collectively referred to as 10G-EPON. The P2MP PHYs for the 10/10G-EPON use the 10GBASE-PR PCS and PMA (see Clause 76). The P2MP PHYs for 10/1G-EPON use the 10GBASE-PRX PCS and PMA (see Clause 76). EPONs using a nominal 10 Gb/s bit rate use a mandatory FEC function defined in Clause 76 in any direction running at the 10 Gb/s bit rate.

c) PON with a nominal MAC data rate of 25 Gb/s in the downstream direction and 10 Gb/s in the upstream direction (25/10G-EPON), 25 Gb/s in both the downstream and upstream directions (25/25G-EPON), 50 Gb/s in the downstream direction and 10 Gb/s in the upstream direction (50/10G-EPON), 50 Gb/s in the downstream direction and 25 Gb/s in the upstream direction (50/25G-EPON), and 50 Gb/s in both the downstream and upstream directions (50/50G-EPON), shared amongst the population of ONUs attached to the P2MP topology, and collectively referred to as Nx25G-EPON. The P2MP PHYs for the 25/10G-EPON and 25/25G-EPON use a single channel in each direction. The P2MP PHYs for the 50/10G-EPON and 50/25G-EPON use two channels in the downstream direction and a single channel in the upstream direction. The P2MP PHYs for the 50/50G-EPON use two channels in each direction. Each PMA channel in the downstream direction operates at a 25.78125 GBd line rate. Each PMA channel in the upstream direction operates at either a 25.78125 GBd or a 10.3125 GBd line rate. Each channel implements a mandatory FEC function in each direction (see Clause 142).

For P2MP coaxial topologies, EFM supports EPoC operating with a nominal bit rate of up to 10 Gb/s in the downstream direction and up to 1.6 Gb/s in the upstream direction. The P2MP EPoC PHYs use the 10GPASS-XR Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA) sublayer, and the mandatory forward error correction (FEC) function defined in Clause 101.

56.1.2.1 Multipoint MAC Control Protocol (MPCP)

The Multipoint MAC Control Protocol (MPCP) for 1G-EPON uses messages, state diagrams, and timers, as defined in Clause 64, to control access to a P2MP topology: Clause 77 defines the messages, state diagrams, and timers required to control access to a P2MP ODN topology in 10G-EPON; and Clause 144 defines the messages, state diagrams, and timers required to control access to a P2MP ODN topology in Nx25G-EPON. The issues related to coexistence of 1G-EPON and 10G-EPON on the same fiber plant are described in 77.4.

Every P2MP ODN topology consists of one Optical Line Terminal (OLT) and one or more ONUs, as shown in Figure 56–3, Figure 56–4, Figure 56–5, and Figure 56–7 for 1G-EPON, 10/10G-EPON, 10/1G-EPON, and Nx25G-EPON, respectively. One of several instances of the MPCP in the OLT communicates with the instance of the MPCP in the ONU. A pair of MPCPs that communicate between the OLT and ONU are a distinct and associated pair.

The MPCP for EPoC uses messages, state diagrams, and timers, as defined in Clause 103 to control access to a P2MP CCDN topology.

Every P2MP CCDN topology consists of one CLT plus one or more CNUs, as shown in Figure 56–6. One of several instances of the MPCP in the CLT communicates with the instance of the MPCP in the CNU. A pair of MPCPs that communicate between the CLT and CNU are a distinct and associated pair.

56.1.2.2 Reconciliation Sublayer (RS) and media independent interfaces

The Clause 22 RS and MII, Clause 35 RS and GMII, Clause 46 RS and XGMII, Clause 106 RS and 25GMII, and Clause 132 RS and 50GMII are all employed for the same purpose in EFM, that being the interconnection between the MAC sublayer and the PHY sublayers. Extensions to the Clause 35 RS for P2MP topologies are described in Clause 65, the RS for 10G-EPON P2MP topologies is described in Clause 76, the RS for Nx25G-EPON P2MP topologies is described in Clause 143, and the RS for EPoC P2MP topologies is described in Clause 101.

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The combination of MPCP and the extension of the Reconciliation Sublayer (RS) for P2P Emulation allows an underlying P2MP network to appear as a collection of point-to-point links to the higher protocol layers (at and above the MAC Client).

The MPCP achieves this by providing a Logical Link Identification (LLID) in each packet by replacing two octets of the preamble.

This is described in Clause 65 for EPON, in Clause 76 for 10G-EPON, in Clause 143 for Nx25G-EPON, and in Clause 101 for EPoC. EFM Copper links use the MII of Clause 22 operating at 100 Mb/s. This is described in 61.1.4.1.2.

56.1.3 Physical Layer signaling systems

EFM extends the family of 100BASE-X Physical Layer signaling systems to include 100BASE-LX10 (long wavelength), plus the combination of the 100BASE-BX10-D (Bi-directional long wavelength Downstream) and the 100BASE-BX10-U (Bi-directional long wavelength Upstream), as defined in Clause 58. All of these systems employ the 100BASE-X PCS and PMA as defined in Clause 66.

EFM also extends the family of 1000BASE-X Physical Layer signaling systems to include 1000BASE-LX10 (long wavelength), plus the combination of the 1000BASE-BX10-D (Bi-directional long wavelength Downstream) and the 1000BASE-BX10-U (Bi-directional long wavelength Upstream), as defined in Clause 59. All of these systems employ the 1000BASE-X PCS and PMA as defined in Clause 66. 1000BASE-LX10 is interoperable with 1000BASE-LX on single-mode and multimode fiber, and offers greater reach than 1000BASE-LX on single-mode fiber.

EFM extends the family of 10GBASE-R Physical Layer signaling systems to include the following combinations of bidirectional PMDs defined in Clause 158:

— 10GBASE-BR10-D and 10GBASE-BR10-U
— 10GBASE-BR20-D and 10GBASE-BR20-U
— 10GBASE-BR40-D and 10GBASE-BR40-U

EFM extends the family of 25GBASE-R Physical Layer signaling systems to include the following combinations of bidirectional PMDs defined in Clause 159:

— 25GBASE-BR10-D and 25GBASE-BR10-U
— 25GBASE-BR20-D and 25GBASE-BR20-U
— 25GBASE-BR40-D and 25GBASE-BR40-U

EFM extends the family of 50GBASE-R Physical Layer signaling systems to include the following combinations of bidirectional PMDs defined in Clause 160:

— 50GBASE-BR10-D and 50GBASE-BR10-U
— 50GBASE-BR20-D and 50GBASE-BR20-U
— 50GBASE-BR40-D and 50GBASE-BR40-U

For P2MP topologies, EFM introduces a family of Physical Layer signaling systems that are derived from 1000BASE-X, but which include extensions to the RS, PCS and PMA, along with an optional forward error correction (FEC) capability, as defined in Clause 65. The family of P2MP Physical Layer signaling systems includes the combination of 1000BASE-PX10-D (Passive Optical Network Downstream 10 km), plus 1000BASE-PX10-U (PON Upstream 10 km), the combination of 1000BASE-PX20-D (PON Downstream 20 km) plus 1000BASE-PX20-U (PON Upstream 20 km), the combination of 1000BASE-PX30-D (PON Downstream 20 km) plus 1000BASE-PX30-U (PON Upstream 20 km), and the combination of 1000BASE-PX40-D (PON Downstream 20 km) plus 1000BASE-PX40-U (PON Upstream 20 km), as defined in Clause 60.

Additionally, EFM introduces a family of Physical Layer signaling systems which are derived from 10GBASE–R, but which include RS, PCS and PMA sublayers adapted for 10G-EPON, along with a

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mandatory FEC capability, as defined in Clause 76. All of these systems employ the PMD defined in Clause 75. The family of P2MP Physical Layer signaling systems utilizes 10GBASE-R signaling for the downstream direction while supporting both 10GBASE-R and 1000BASE-X upstream signaling in the following series of PMD combinations:

a) 10GBASE–PR–D1 and 10GBASE–PR–U1, creating a PR10 power budget, with 10 Gb/s downstream and 10 Gb/s upstream data rates, supporting a reach of at least 10 km and a split ratio of at least 1:16.
b) 10GBASE–PR–D2 and 10GBASE–PR–U1, creating a PR20 power budget, with 10 Gb/s downstream and 10 Gb/s upstream data rates, supporting a reach of at least 20 km and a split ratio of at least 1:16 or the reach of at least 10 km and the split ratio of at least 1:32.
c) 10GBASE–PR–D3 and 10GBASE–PR–U3, creating a PR30 power budget, with 10 Gb/s downstream and 10 Gb/s upstream data rates, supporting a reach of at least 20 km and a split ratio of at least 1:32.
d) 10GBASE–PR–D4 and 10GBASE–PR–U4, creating a PR40 power budget, with 10 Gb/s downstream and 10 Gb/s upstream data rates, supporting a reach of at least 20 km and a split ratio of at least 1:64.
e) 10/1GBASE–PRX–D1 and 10/1GBASE–PRX–U1, creating a PRX10 power budget, with 10 Gb/s downstream and 1 Gb/s upstream data rates, supporting a reach of at least 10 km and a split ratio of at least 1:16.
f) 10/1GBASE–PRX–D2 and 10/1GBASE–PRX–U2, creating a PRX20 power budget, with 10 Gb/s downstream and 1 Gb/s upstream data rates, supporting a reach of at least 20 km and a split ratio of at least 1:16.
g) 10/1GBASE–PRX–D3 and 10/1GBASE–PRX–U3, creating a PRX30 power budget, with 10 Gb/s downstream and 1 Gb/s upstream data rates, supporting a reach of at least 20 km and a split ratio of at least 1:32.
h) 10/1GBASE–PRX–D4 and 10/1GBASE–PRX–U4, creating a PRX40 power budget, with 10 Gb/s downstream and 1 Gb/s upstream data rates, supporting a reach of at least 20 km and a split ratio of at least 1:64.

All 10G-EPON PMDs are defined in Clause 75.

Additionally, EFM introduces a family of Physical Layer signaling systems that are derived from 25GBASE–R, but which include RS, PCS and PMA sublayers adapted for Nx25G-EPON, along with a mandatory FEC function, as defined in Clause 142. All these systems employ PMDs defined in Clause 141.

Moreover, EFM introduces a Physical Layer signaling system derived from 10GBASE-R, but which includes RS, PCS, and PMA sublayers adapted for EPoC, along with a mandatory FEC capability, as defined in Clause 101. This system employs the PMD defined in Clause 100. EPoC uses a PHY Link for Physical Layer signaling as defined in Clause 102.

For copper cabling, EFM introduces a family of Physical Layer signaling systems. There are two distinct signaling systems specified for copper cabling. Both of them share a set of common functions and interfaces as described in Clause 61. Clause 61 also includes an optional specification that supports combined operation on multiple copper pairs, affording greater data rate capability for a given link span. Underlying these functions, two Physical Layer signaling system specific PMAs and PMDs are described in Clause 62 and Clause 63. Non-loaded cable is a requirement of the signaling methods employed.

For high-speed applications, the 10PASS-TS signaling system is defined in Clause 62. 10PASS-TS relies on a technique referred to as Frequency Division Duplexing (FDD) to accomplish full duplex communication on a single wire pair. 10PASS-TS is a passband signaling system derived from the Very high-speed Digital Subscriber Line (VDSL) standard defined in ATIS-0600424, using Multiple Carrier Modulation (MCM, also referred to as Discrete Multi-Tone or DMT). This PHY supports a nominal full duplex data rate of 10 Mb/s, hence the identifier 10PASS-TS. For the 10PASS-TS PHY, two subtypes are defined: 10PASS-TS-O and 10PASS-TS-R. A connection can be established only between a 10PASS-TS-O PHY on one end

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of the voice-grade copper line, and a 10PASS-TS-R PHY on the other end. In public networks, a 10PASS-TS-O PHY is used at a central office (CO), a cabinet, or other centralized distribution point; a 10PASS-TS-R PHY is used at the subscriber premises. In private networks, the network administrator will designate one end of each link as the network end. A PHY implementation may be equipped to support both subtypes and provide means to be configured as a 10PASS-TS-O or a 10PASS-TS-R.

For long distance applications, the 2BASE-TL signaling system is defined in Clause 63. 2BASE-TL is a baseband signaling system derived from the Single-Pair High-Speed Digital Subscriber Line (SHDSL) standards defined by ITU-T. The 2BASE-TL PMD supports a nominal full duplex data rate of approximately 2 Mb/s. As is the case with the 10PASS-TS PHY, the 2BASE-TL PHY consists of two subtypes: 2BASE-TL-O (network end) and 2BASE-TL-R (subscriber end).

System considerations for Ethernet subscriber access networks are described in Clause 67.

Specifications unique to the operation of each Physical Layer device are shown in Table 56–1.

Table 56–1—Summary of EFM Physical Layer signaling systems

Name	Location	Rate[a]	Nominal reach (km)	Medium	Clause
100BASE-LX10	ONU/OLT[b]	100 Mb/s	10	Two single-mode fibers	58
100BASE-BX10-D	OLT	100 Mb/s	10	One single-mode fiber	58
100BASE-BX10-U	ONU				
1000BASE-LX10	ONU/OLT[b]	1000 Mb/s	10 0.55	Two single-mode fibers Two multimode fibers	59
1000BASE-BX10-D	OLT	1000 Mb/s	10	One single-mode fiber	59
1000BASE-BX10-U	ONU				
10GBASE-BR10-D	OLT	10 Gb/s	10	One single-mode fiber	158
10GBASE-BR10-U	ONU				
10GBASE-BR20-D	OLT		20		
10GBASE-BR20-U	ONU				
10GBASE-BR40-D	OLT		40		
10GBASE-BR40-U	ONU				
25GBASE-BR10-D	OLT	25 Gb/s	10	One single-mode fiber	159
25GBASE-BR10-U	ONU				
25GBASE-BR20-D	OLT		20		
25GBASE-BR20-U	ONU				
25GBASE-BR40-D	OLT		40		
25GBASE-BR40-U	ONU				

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Table 56–1—Summary of EFM Physical Layer signaling systems *(continued)*

Name	Location	Rate[a]	Nominal reach (km)	Medium	Clause
50GBASE-BR10-D	OLT	50 Gb/s	10	One single-mode fiber	160
50GBASE-BR10-U	ONU				
50GBASE-BR20-D	OLT		20		
50GBASE-BR20-U	ONU				
50GBASE-BR40-D	OLT		40		
50GBASE-BR40-U	ONU				
1000BASE-PX10-D	OLT	1000 Mb/s	10	One single-mode fiber PON	60
1000BASE-PX10-U	ONU				
1000BASE-PX20-D	OLT	1000 Mb/s	20	One single-mode fiber PON	60
1000BASE-PX20-U	ONU				
1000BASE-PX30-D	OLT	1000 Mb/s	20	One single-mode fiber PON	60
1000BASE-PX30-U	ONU				
1000BASE-PX40-D	OLT	1000 Mb/s	20	One single-mode fiber PON	60
1000BASE-PX40-U	ONU				
10/1GBASE-PRX-D1	OLT	10 Gb/s (tx) 1000 Mb/s (rx)	10	One single-mode fiber PON	75
10/1GBASE-PRX-U1	ONU	1000 Mb/s (tx) 10 Gb/s (rx)			
10/1GBASE-PRX-D2	OLT	10 Gb/s (tx) 1000 Mb/s (rx)	20	One single-mode fiber PON	75
10/1GBASE-PRX-U2	ONU	1000 Mb/s (tx) 10 Gb/s (rx)			
10/1GBASE-PRX-D3	OLT	10 Gb/s (tx) 1000 Mb/s (rx)	20	One single-mode fiber PON	75
10/1GBASE-PRX-U3	ONU	1000 Mb/s (tx) 10 Gb/s (rx)			
10/1GBASE-PRX-D4	OLT	10 Gb/s (tx) 1000 Mb/s (rx)	20	One single-mode fiber PON	75
10/1GBASE-PRX-U4	ONU	1000 Mb/s (tx) 10 Gb/s (rx)			
10GBASE-PR-D1	OLT	10 Gb/s	10	One single-mode fiber PON	75
10GBASE-PR-U1	ONU				
10GBASE-PR-D2	OLT	10 Gb/s	20	One single-mode fiber PON	75
10GBASE-PR-U1	ONU				
10GBASE-PR-D3	OLT	10 Gb/s	20	One single-mode fiber PON	75
10GBASE-PR-U3	ONU				

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Table 56–1—Summary of EFM Physical Layer signaling systems *(continued)*

Name	Location	Rate[a]	Nominal reach (km)	Medium	Clause
10GBASE-PR-D4	OLT	10 Gb/s	20	One single-mode fiber PON	75
10GBASE-PR-U4	ONU				
10PASS-TS-O	CO[c]	10 Mb/s[d]	0.75[e]	One or more pairs of voice grade copper cable	62
10PASS-TS-R	Subscriber[c]				
2BASE-TL-O	CO[c]	2 Mb/s[f]	2.7[g]	One or more pairs of voice grade copper cable	63
2BASE-TL-R	Subscriber[c]				
10GPASS-XR-D	CLT	Up to 10 Gb/s (tx)[h] Up to 1.6 Gb/s (rx)[h]	2.9[i]	One CCDN	100
10GPASS-XR-U	CNU[c]	Up to 1.6 Gb/s (tx)[h] Up to 10 Gb/s (rx)[h]	2.9[i]	One CCDN	100
25/10GBASE-PQG-D2	OLT	25 Gb/s (tx) 10 Gb/s (rx)	20	One single-mode fiber PON	141
25/10GBASE-PQG-D3					
25/10GBASE-PQX-D2					
25/10GBASE-PQX-D3					
25/10GBASE-PQG-U2	ONU	10 Gb/s (tx) 25 Gb/s (rx)			
25/10GBASE-PQG-U3					
25/10GBASE-PQX-U2					
25/10GBASE-PQX-U3					
25GBASE-PQG-D2	OLT	25 Gb/s	20	One single-mode fiber PON	141
25GBASE-PQG-D3					
25GBASE-PQX-D2					
25GBASE-PQX-D3					
25GBASE-PQG-U2	ONU				
25GBASE-PQG-U3					
25GBASE-PQX-U2					
25GBASE-PQX-U3					

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Table 56–1—Summary of EFM Physical Layer signaling systems *(continued)*

Name	Location	Rate[a]	Nominal reach (km)	Medium	Clause
50/10GBASE-PQG-D2	OLT	50 Gb/s (tx) 10 Gb/s (rx)	20	One single-mode fiber PON	141
50/10GBASE-PQG-D3					
50/10GBASE-PQX-D2					
50/10GBASE-PQX-D2					
50/10GBASE-PQG-U2	ONU	10 Gb/s (tx) 50 Gb/s (rx)			
50/10GBASE-PQG-U3					
50/10GBASE-PQX-U2					
50/10GBASE-PQX-U2					
50/25GBASE-PQG-D2	OLT	50 Gb/s (tx) 25 Gb/s (rx)	20	One single-mode fiber PON	141
50/25GBASE-PQG-D3					
50/25GBASE-PQX-D2					
50/25GBASE-PQX-D3					
50/25GBASE-PQG-U2	ONU	25 Gb/s (tx) 50 Gb/s (rx)			
50/25GBASE-PQG-U3					
50/25GBASE-PQX-U2					
50/25GBASE-PQX-U3					
50GBASE-PQG-D2	OLT	50 Gb/s	20	One single-mode fiber PON	141
50GBASE-PQG-D3					
50GBASE-PQX-D2					
50GBASE-PQX-D3					
50GBASE-PQG-U2	ONU				
50GBASE-PQG-U3					
50GBASE-PQX-U2					
50GBASE-PQX-U3					

[a]For Physical Layer signaling systems the transmit rate is denoted with the abbreviation “(tx)” to the location: whereas, the receive rate is denoted with the abbreviation “(rx)”.
[b]Symmetric
[c]In private networks, the network administrator designates one end of each link as the network end.
[d]Nominal rate stated at the nominal reach. Rate may vary depending on plant. Refer to Annex 62B for more information.
[e]Reach may vary depending on plant. Refer to Annex 62B for further information.
[f]Nominal rate stated at the nominal reach. Rate may vary depending on plant. Refer to Annex 63B for more information.
[g]Reach may vary depending on plant. Refer to Annex 63B for further information.
[h]These rates are based on maximum mandatory modulation format in Table 100–3.
[i]Maximal differential distance between CNUs. Reach may vary depending on the CCDN.

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Table 56–2 specifies the correlation between nomenclature and clauses for P2P systems, while Table 56–3 specifies the correlation between nomenclature and clauses for optical P2MP systems, and Table 56–4 specifies the correlation between nomenclature and clauses for coaxial P2MP systems. A complete implementation conforming to one or more nomenclatures meets the requirements of the corresponding clauses.

Table 56–2—Nomenclature and clause correlation for P2P systems

Nomenclature	Clause																							
	57	78	58		59		61	62	63	66		49	51	158	107	108	109	159	133	134	135	160
	OAM	EEE	100BASE-LX10 PMD	100BASE-BX10 PMD	1000BASE-LX10 PMD	1000BASE-BX10 PMD	Cu PCS	10PASS-TS PMA & PMD	2BASE-TL PMA & PMD	100BASE-X PCS, PMA	1000BASE-X PCS, PMA	10GBASE-R PCS	10GBASE-R PMA	10GBASE-BRx PMD	25GBASE-R PCS	Reed-Solomon FEC	25GBASE-R PMA	25GBASE-BRx PMD	50GBASE-R PCS	50GBASE-R RS-FEC	50GBASE-R PMA	50GBASE-BRx PMD
2BASE-TL	O[a]						M		M													
10PASS-TS	O						M	M														
100BASE-LX10	O		M							M												
100BASE-BX10	O			M						M												
1000BASE-LX10	O				M						M											
1000BASE-BX10	O					M					M											
10GBASE-BR10	O											M	M	M								
10GBASE-BR20	O											M	M	M		M						
10GBASE-BR40	O											M	M	M								
25GBASE-BR10	O	O													M	M	M	M				
25GBASE-BR20	O	O													M	M	M	M				
25GBASE-BR40	O	O													M	M	M	M				
50GBASE-BR10	O	O																	M	M	M	M
50GBASE-BR20	O	O																	M	M	M	M
50GBASE-BR40	O	O																	M	M	M	M

[a]O = Optional, M = Mandatory

56.1.4 Management

Managed objects, attributes, and actions are defined for all EFM components in Clause 30.

In addition to the management objects, attributes, and actions defined in Clause 30, EFM introduces Operations, Administration, and Maintenance (OAM) for subscriber access networks to Ethernet. OAM, as defined in Clause 57, includes a mechanism for communicating management information using OAM frames, as well as functions for performing low-level diagnostics on a per link basis in an Ethernet subscriber access network.

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Table 56–3—Nomenclature and clause correlation for optical P2MP systems[a]

Nomenclature	Clause															
	57	60				64	65		66	75	76	77	141	142	143	144
	OAM	1000BASE-PX10 PMD	1000BASE-PX20 PMD	1000BASE-PX30 PMD	1000BASE-PX40 PMD	P2MP MPMC	P2MP RS, PCS, PMA	FEC	1000BASE-X PCS, PMA	10/1GBASE–PRX or 10GBASE-PR PMDs	P2MP RS, PCS, PMA, FEC	10G-EPON P2MP MPMC	Nx25GBASE-PQ PMD	Nx25GBASE-PQ P2MP PCS, PMA, FEC	Nx25GBASE-PQ M2MP MCRS	Nx25GBASE-PQ P2MP MPMC
1000BASE-PX10-D	O	M				M	M	O	M							
1000BASE-PX10-U	O	M				M	M	O								
1000BASE-PX20-D	O		M			M	M	O	M							
1000BASE-PX20-U	O		M			M	M	O								
1000BASE-PX30-D	O			M		M	M	O	M							
1000BASE-PX30-U	O			M		M	M	O								
1000BASE-PX40-D	O				M	M	M	O	M							
1000BASE-PX40-U	O				M	M	M	O								
10/1GBASE-PRX-D1	O			M		M				M	M	M				
10/1GBASE-PRX-U1	O			M		M				M	M	M				
10/1GBASE-PRX-D2	O				M	M				M	M	M				
10/1GBASE-PRX-U2	O				M	M				M	M	M				
10/1GBASE-PRX-D3	O					M				M	M	M				
10/1GBASE-PRX-U3	O					M				M	M	M				
10/1GBASE-PRX-D4	O					M				M	M	M				
10/1GBASE-PRX-U4	O					M				M	M	M				
10GBASE-PR-D1	O									M	M	M				
10GBASE-PR-U1	O									M	M	M				
10GBASE-PR-D2	O									M	M	M				
10GBASE-PR-D3	O									M	M	M				
10GBASE-PR-U3	O									M	M	M				
10GBASE-PR-D4	O									M	M	M				
10GBASE-PR-U4	O									M	M	M				
25/10GBASE-PQG-U2	O												M	M	M	M
25/10GBASE-PQG-U3	O												M	M	M	M
25/10GBASE-PQG-D2	O												M	M	M	M
25/10GBASE-PQG-D3	O												M	M	M	M
25/10GBASE-PQX-U2	O												M	M	M	M

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Table 56–3—Nomenclature and clause correlation for optical P2MP systems[a] *(continued)*

Nomenclature	Clause															
	57	60				64	65		66	75	76	77	141	142	143	144
	OAM	1000BASE-PX10 PMD	1000BASE-PX20 PMD	1000BASE-PX30 PMD	1000BASE-PX40 PMD	P2MP MPMC	P2MP RS, PCS, PMA	FEC	1000BASE-X PCS, PMA	10/1GBASE–PRX or 10GBASE-PR PMDs	P2MP RS, PCS, PMA, FEC	10G-EPON P2MP MPMC	Nx25GBASE-PQ PMD	Nx25GBASE-PQ P2MP PCS, PMA, FEC	Nx25GBASE-PQ M2MP MCRS	Nx25GBASE-PQ P2MP MPMC
25/10GBASE-PQX-U3	O												M	M	M	M
25/10GBASE-PQX-D2	O												M	M	M	M
25/10GBASE-PQX-D3	O												M	M	M	M
25GBASE-PQG-U2	O												M	M	M	M
25GBASE-PQG-U3	O												M	M	M	M
25GBASE-PQG-D2	O												M	M	M	M
25GBASE-PQG-D3	O												M	M	M	M
25GBASE-PQX-U2	O												M	M	M	M
25GBASE-PQX-U3	O												M	M	M	M
25GBASE-PQX-D2	O												M	M	M	M
25GBASE-PQX-D3	O												M	M	M	M
50/10GBASE-PQG-U2	O												M	M	M	M
50/10GBASE-PQG-U3	O												M	M	M	M
50/10GBASE-PQG-D2	O												M	M	M	M
50/10GBASE-PQG-D3	O												M	M	M	M
50/10GBASE-PQX-U2	O												M	M	M	M
50/10GBASE-PQX-U3	O												M	M	M	M
50/10GBASE-PQX-D2	O												M	M	M	M
50/10GBASE-PQX-D3	O												M	M	M	M
50/25GBASE-PQG-U2	O												M	M	M	M
50/25GBASE-PQG-U3	O												M	M	M	M
50/25GBASE-PQG-D2	O												M	M	M	M
50/25GBASE-PQG-D3	O												M	M	M	M
50/25GBASE-PQX-U2	O												M	M	M	M
50/25GBASE-PQX-U3	O												M	M	M	M
50/25GBASE-PQX-D2	O												M	M	M	M
50/25GBASE-PQX-D3	O												M	M	M	M
50GBASE-PQX-U2	O												M	M	M	M

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Table 56–3—Nomenclature and clause correlation for optical P2MP systems[a] *(continued)*

Nomenclature	Clause															
	57	60				64	65		66	75	76	77	141	142	143	144
	OAM	1000BASE-PX10 PMD	1000BASE-PX20 PMD	1000BASE-PX30 PMD	1000BASE-PX40 PMD	P2MP MPMC	P2MP RS, PCS, PMA	FEC	1000BASE-X PCS, PMA	10/1GBASE–PRX or 10GBASE-PR PMDs	P2MP RS, PCS, PMA, FEC	10G-EPON P2MP MPMC	Nx25GBASE-PQ PMD	Nx25GBASE-PQ P2MP PCS, PMA, FEC	Nx25GBASE-PQ M2MP MCRS	Nx25GBASE-PQ P2MP MPMC
50GBASE-PQX-U3	O												M	M	M	M
50GBASE-PQX-D2	O												M	M	M	M
50GBASE-PQX-D3	O												M	M	M	M
50GBASE-PQG-U2	O												M	M	M	M
50GBASE-PQG-U3	O												M	M	M	M
50GBASE-PQG-D2	O												M	M	M	M
50GBASE-PQG-D3	O												M	M	M	M

[a]O = Optional, M = Mandatory

Table 56–4—Nomenclature and clause correlation for coaxial P2MP systems[a]

Nomenclature	Clause				
	57	100	101	102	103
	OAM	10GPASS-XR	EPoC P2MP RS, PCS, PMA, FEC	EPoC PHY-Link	EPoC P2MP MPMC
10GPASS-XR-D	O	M	M	M	M
10GPASS-XR-U	O	M	M	M	M

[a]O = Optional, M = Mandatory

56.1.5 Unidirectional transmission

In contrast to previous editions of IEEE Std 802.3, in certain circumstances a DTE is allowed to transmit frames while not receiving a satisfactory signal. It is necessary for an EPON OLT or EPoC CLT to do this to

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bring an ODN or CCDN into operation (although it is highly inadvisable for an EPON ONU or EPoC CNU to transmit without receiving). Clause 66 describes optional modifications to the 100BASE-X PHY, 1000BASE-X PHY and 10GBASE RS so that a DTE may signal remote fault using OAMPDUs. When unidirectional operation is not enabled, the sublayers in Clause 66 are precisely the same as their equivalents in Clause 24, Clause 36, and Clause 46.

56.2 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

56.3 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE 802.3, Clause 57 through Clause 66, demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the EFM PICS conforms to the same notation and conventions used in 100BASE-T (see 21.6).

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57. Operations, Administration, and Maintenance (OAM)

57.1 Overview

57.1.1 Scope

This clause defines the Operations, Administration, and Maintenance (OAM) sublayer, which provides mechanisms useful for monitoring link operation such as remote fault indication and remote loopback control. In general, OAM provides network operators the ability to monitor the health of the network and quickly determine the location of failing links or fault conditions. The OAM described in this clause provides data link layer mechanisms that complement applications that may reside in higher layers.

OAM information is conveyed in Slow Protocol frames (see Annex 57A) called OAM Protocol Data Units (OAMPDUs). OAMPDUs contain the appropriate control and status information used to monitor, test and troubleshoot OAM-enabled links. OAMPDUs traverse a single link, being passed between peer OAM entities, and as such, are not forwarded by MAC clients (e.g., bridges or switches).

OAM does not include functions such as station management, bandwidth allocation, or provisioning functions, which are considered outside the scope of this standard.

For the remainder of this clause, the term OAM is specific to the link level OAM described here.

57.1.2 Summary of objectives and major concepts

This subclause provides details and functional requirements for the OAM objectives:

a) Remote Failure Indication
   1) A mechanism is provided to indicate to a peer that the receive path of the local DTE is non-operational.
   2) Physical Layer devices using Clause 66 may support unidirectional operation that allows OAM remote failure indication during fault conditions.
   3) Subscriber access Physical Layer devices using Clause 65 support unidirectional operation in the direction from OLT to ONU that allows OAM remote failure indication from OLT during fault conditions.
   4) Physical Layer devices other than those listed above do not support unidirectional operation allowing OAM remote failure indication during fault conditions. Some Physical Layer devices have specific remote failure signaling mechanisms in the Physical Layer.

b) Remote Loopback—A mechanism is provided to support a data link layer frame-level loopback mode.

c) Link Monitoring
   1) A mechanism is provided to support event notification that permits the inclusion of diagnostic information.
   2) A mechanism is provided to support polling of any variable in the Clause 30 MIB.

d) Miscellaneous
   1) Implementation and activation of OAM is optional.
   2) A mechanism is provided that performs OAM capability discovery.
   3) An extension mechanism is provided and made available for higher layer management applications.

These objectives support a subset of the user-plane OAM requirements found in ITU-T Y.1730 [B50].

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57.1.3 Summary of non-objectives

This subclause explicitly lists certain functions that are not addressed by OAM. These functions, while valuable, do not fall within the scope of this standard.

a) Management functions not pertaining to a single link such as protection switching and station management are not covered by this clause. Such functions could be addressed using the extension mechanism.
b) Provisioning and negotiation functions such as bandwidth allocation, rate adaptation and speed/ duplex negotiation are not supported by OAM.
c) Issues related to privacy of OAM data and authentication of OAM entities are beyond the scope of this standard.
d) The ability to set/write remote MIB variables is not supported.

57.1.4 Positioning of OAM within the IEEE 802.3 architecture

OAM comprises an optional sublayer between a superior sublayer (e.g., MAC client or optional Link Aggregation) and a subordinate sublayer (e.g., MAC or optional MAC Control sublayer). Figure 57–1 shows the relationship of the OAM sublayer to the ISO/IEC (IEEE) OSI reference model.

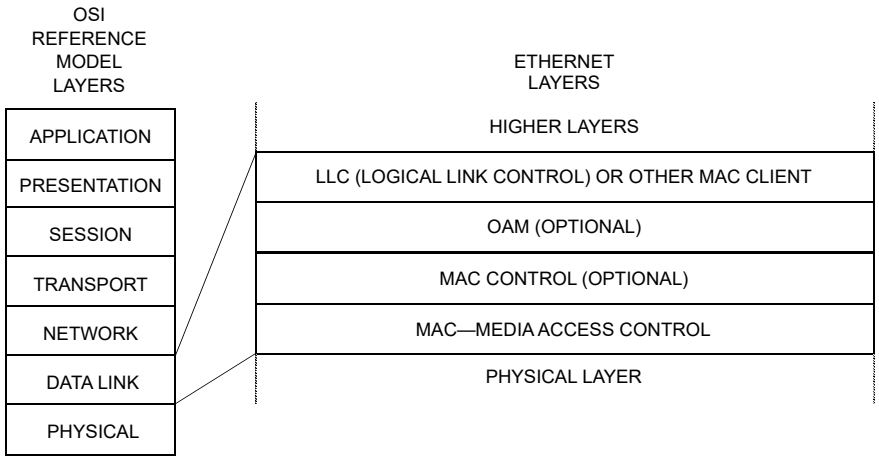

Figure 57–1—OAM sublayer relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

57.1.5 Compatibility considerations

57.1.5.1 Application

OAM is intended for point-to-point and emulated point-to-point IEEE 802.3 links. Implementation of OAM functionality is optional. A conformant implementation may implement the optional OAM sublayer for some ports within a system while not implementing it for other ports.

57.1.5.2 Interoperability between OAM capable DTEs

A DTE is able to determine whether or not a remote DTE has OAM functionality enabled. The OAM Discovery mechanism ascertains the configured parameters, such as maximum allowable OAMPDU size, and supported functions, such as OAM remote loopback, on a given link.

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57.1.5.3 MAC Control PAUSE

MAC Control PAUSE, commonly referred to as Flow Control as defined in Annex 31B, inhibits the transmission of all MA_DATA.request service primitives, including OAMPDUs. This may delay or prevent the signaling of critical events such as unrecoverable failure conditions and link faults.

57.1.5.4 Interface to MAC Control client

MAC Control clients that generate MA_CONTROL.request service primitives (and which expect MA_CONTROL.indication service primitives in response) are not acted upon by the OAM sublayer. They communicate directly with the MAC Control entity as though no OAM sublayer exists.

57.1.5.5 Frame loss during OAM remote loopback

Invocations of OAM remote loopback may result in frame loss. OAM remote loopback is an intrusive operation that prevents a link from passing frames between the MAC client of the local DTE and the MAC client of the remote DTE. Refer to 57.2.11 for a complete description of OAM remote loopback operation.

57.1.6 State diagram conventions

Many of the functions specified in this clause are presented in state diagram notation. All state diagrams contained in this clause use the notation and conventions defined in 21.5. In the event of a discrepancy between the text description and the state diagram formalization of a function, the state diagrams take precedence.

57.2 Functional specifications

57.2.1 Interlayer service interfaces

Figure 57–2 depicts the usage of interlayer interfaces by the OAM sublayer.

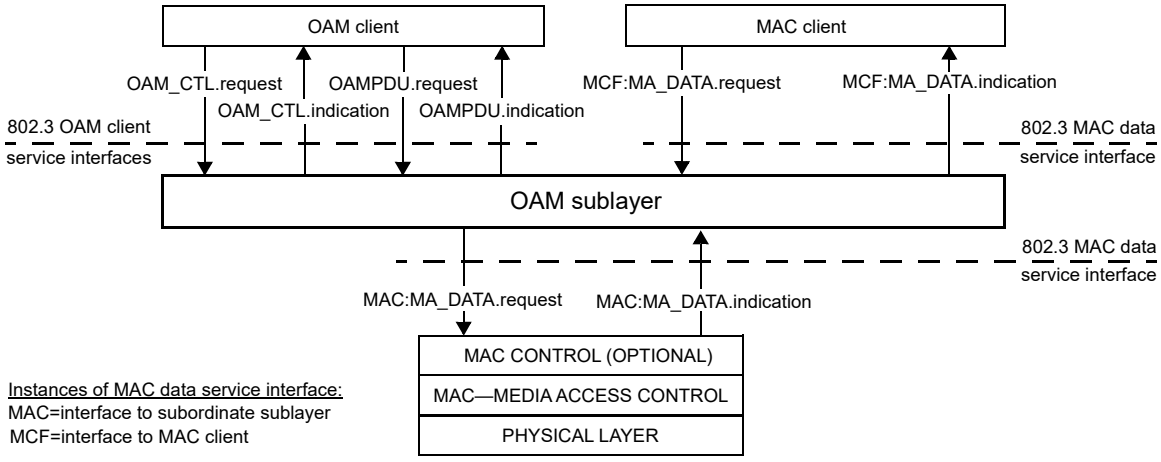

Figure 57–2—OAM sublayer support of interlayer service interfaces

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57.2.2 Principles of operation

OAM employs the following principles and concepts:

a) The OAM sublayer presents a standard IEEE 802.3 MAC service interface to the superior sublayer. Superior sublayers include MAC client and Link Aggregation.
b) The OAM sublayer employs a standard IEEE 802.3 MAC service interface to the subordinate sublayer. Subordinate sublayers include MAC and MAC Control.
c) Frames from superior sublayers are multiplexed within the OAM sublayer with OAMPDUs.
d) The OAM sublayer parses received frames and passes OAMPDUs to the OAM client. In general, non-OAMPDUs are passed to the superior sublayer. When in OAM remote loopback mode, non-OAMPDUs are looped back to the subordinate sublayer. When the peer OAM entity is in OAM remote loopback mode, non-OAMPDUs are discarded by the OAM sublayer so that higher layer functions (e.g., bridging) do not process the looped back frames.
e) Knowledge of the underlying Physical Layer device is not required by the OAM sublayer.
f) OAMPDUs traverse a single link and are passed between OAM client entities or OAM sublayer entities. OAMPDUs are not forwarded by OAM clients.
g) OAM is extensible through the use of an Organization Specific OAMPDU, Organization Specific Information TLV, and Organization Specific Event TLV. These can be used for functions outside the scope of this standard.

57.2.3 Instances of the MAC data service interface

A superior sublayer such as the MAC client communicates with the OAM sublayer using the standard MAC data service interface specified in Clause 2. Similarly, the OAM sublayer communicates with a subordinate sublayer such as the MAC Control or MAC using the same standard service interfaces.

Since this clause uses two instances of the MAC data service interface, it is necessary to introduce a notation convention so that the reader can be clear as to which interface is being referred to at any given time. A prefix is therefore assigned to each service primitive, indicating which of the two interfaces is being invoked, as depicted in Figure 57–2. The prefixes are as follows:

a) MCF:, for primitives issued on the interface between the superior sublayer and the OAM sublayer (MCF is an abbreviation for MAC client frame)
b) MAC:, for primitives issued on the interface between the underlying subordinate sublayer (e.g., MAC) and the OAM sublayer

57.2.4 Responsibilities of OAM client

The OAM client plays an integral role in establishing and managing OAM on a link. The OAM client enables and configures the OAM sublayer entity. During the OAM Discovery process (see 57.3.2.1), the OAM client monitors received OAMPDUs from the remote DTE and based upon local and remote state and configuration settings allows OAM functionality to be enabled on the link.

After OAM has been established, the OAM client is responsible for adhering to the OAMPDU response rules. For example, the OAM client does not respond to illegal requests such as Variable Request and Loopback Control OAMPDUs from Passive DTEs. The OAM client is also expected to manage the OAM remote loopback mode (see 57.2.11). It does so by reacting to particular OAMPDUs and altering local configuration parameters.

Link events are signalled between peer OAM client entities. The OAM client transfers events by sending and receiving particular OAMPDUs. To increase the likelihood that a specific event is received by the remote DTE, the OAM client may send the event multiple times.

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57.2.5 OAM client interactions

The OAM sublayer entity communicates with the OAM client using the following new interlayer service interfaces:

OAMPDU.request
OAMPDU.indication
OAM_CTL.request
OAM_CTL.indication

The OAMPDU.request, OAMPDU.indication, OAM_CTL.request and OAM_CTL.indication service primitives described in this subclause are mandatory.

57.2.5.1 OAMPDU.request

57.2.5.1.1 Function

This primitive defines the transfer of data from an OAM client entity to a peer OAM client entity.

57.2.5.1.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
OAMPDU.request      (
                    source_address,
                        flags,
                        code,
                        data
                        )
```

The source_address parameter specifies an individual MAC address. The flags parameter is used to create the Flags field within the OAMPDU to be transmitted. Only the indications corresponding to the Flags field bits 15:3 are contained in the flags parameter since the indications corresponding to Flags field bits 2:0 are contained in the OAM_CTL.request service primitive. The code parameter is used to create the Code field within the OAMPDU to be transmitted. The data parameter is used to create the Data field within the OAMPDU to be transmitted.

57.2.5.1.3 When generated

This primitive is generated by the OAM client entity whenever an OAMPDU is to be transferred to a peer entity. This can be in response to a request from the peer entity or from data generated internally to the OAM client.

57.2.5.1.4 Effect of receipt

The receipt of this primitive will cause the OAM sublayer entity to insert all OAMPDU specific fields, including DA, SA, Length/Type and Subtype, and pass the properly formed OAMPDU to the lower protocol layers for transfer to the peer OAM client entity according to the transmit rules as described in 57.3.2.2.6.

57.2.5.2 OAMPDU.indication

57.2.5.2.1 Function

This primitive defines the transfer of data from an OAM sublayer entity to an OAM client entity.

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57.2.5.2.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
OAMPDU.indication    (
                         source_address,
                         flags,
                         code,
                         data
                         )
```

The source_address parameter is the MAC source address of the incoming OAMPDU. The flags parameter is the entire Flags field of the incoming OAMPDU. The code parameter is the Code field of the incoming OAMPDU. The data parameter is the Data field of the incoming OAMPDU.

57.2.5.2.3 When generated

This primitive is passed from the OAM sublayer entity to the OAM client entity to indicate the arrival of an OAMPDU to the local OAM sublayer entity that is destined for the OAM client. Such OAMPDUs are reported only if they are validly formed and received without error.

57.2.5.2.4 Effect of receipt

The effect of receipt of this primitive by the OAM client is unspecified.

57.2.5.3 OAM_CTL.request

57.2.5.3.1 Function

This primitive defines the transfer of control information from an OAM client entity to an OAM sublayer entity.

57.2.5.3.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
OAM_CTL.request      (
                         local_unidirectional,
                         local_link_status,
                         local_dying_gasp,
                         local_critical_event,
                         local_satisfied,
                         remote_state_valid,
                         remote_stable,
                         local_mux_action,
                         local_par_action,
                         information_data
                              )
```

When set, the local_unidirectional parameter is used to indicate the sending station supports transmission of OAMPDUs on unidirectional links as supported by some physical coding layers (see 57.2.12).

The local_link_status, local_dying_gasp, and local_critical_event parameters are used to indicate immediate event situations that should be transmitted to the peer OAM entity. The local_link_status parameter is used

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to convey the status of the link as determined by the underlying Physical Layer. When set to FAIL, the local_link_status parameter will cause the OAM sublayer entity to transmit an Information OAMPDU with the Link Fault bit of the Flags field set and no Information TLVs. The local_dying_gasp parameter is used to signal a local unrecoverable failure condition. When set, the local_dying_gasp parameter will cause the OAM sublayer to transmit an Information OAMPDU with the Dying Gasp bit of the Flags field set. The local_critical_event parameter is used to signal an unspecified critical link event condition. When set, the local_critical_event parameter will cause the OAM sublayer to transmit an Information OAMPDU with the Critical Event bit of the Flags field set.

The local_satisfied, remote_state_valid, and remote_stable parameters are used in the Discovery process. The local_satisfied parameter is set by the OAM client as a result of comparing its local configuration and the remote configuration found in the received Local Information TLV (see 57.3.2.1).

The local_mux_action and local_par_action parameters are used to control the state of the Multiplexer and Parser functions of the OAM sublayer (see 57.3.3 and 57.3.4).

The information_data parameter contains the Local Information TLV fields, and, if available, the Remote Information and Organization Specific Information TLV fields, to be included in Information OAMPDUs generated by the Transmit process (see 57.3.2.2).

57.2.5.3.3 When generated

This primitive is passed from the OAM client entity to the OAM sublayer to update control information.

57.2.5.3.4 Effect of receipt

The receipt of this primitive will cause the OAM sublayer to generate Information OAMPDUs or update specific fields of future Information OAMPDUs. Also, OAM functions will be re-evaluated based upon any changing control information.

57.2.5.4 OAM_CTL.indication

57.2.5.4.1 Function

This primitive defines the transfer of control information from an OAM sublayer entity to an OAM client entity.

57.2.5.4.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
OAM_CTL.indication      (
                        local_pdu,
                        local_stable,
                        local_lost_link_timer_done
                            )
```

The local_pdu and local_stable parameters are used by the OAM sublayer to indicate to the OAM client state information in the Discovery process (see 57.3.2.1). The local_lost_link_timer_done parameter is used to convey the expiration of the local_lost_link_timer.

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57.2.5.4.3 When generated

This primitive is passed from the OAM sublayer entity to the OAM client entity to indicate local state information has changed.

57.2.5.4.4 Effect of receipt

The effect of receipt of this primitive by the OAM client is unspecified.

57.2.6 Instances of the OAM internal service interface

The OAM sublayer communicates internally using the OAM internal service interface. Since two instances of the OAM internal service interface are used, it is necessary to introduce a notation convention so that the reader can be clear as to which interface is being referred to at any given time. A prefix is therefore assigned to each service primitive, indicating which of the two interfaces is being invoked (see Figure 57–3). The prefixes are as follows:

a) LBF:, for primitives issued on the interface between the Parser and the Multiplexer (LBF is an abbreviation for loopback frame).
b) CTL:, for primitives issued on the interface between the Control and other OAM functions (CTL is an abbreviation for Control function).

57.2.7 Internal block diagram

Figure 57–3 depicts the major blocks within the OAM sublayer and their interrelationships.

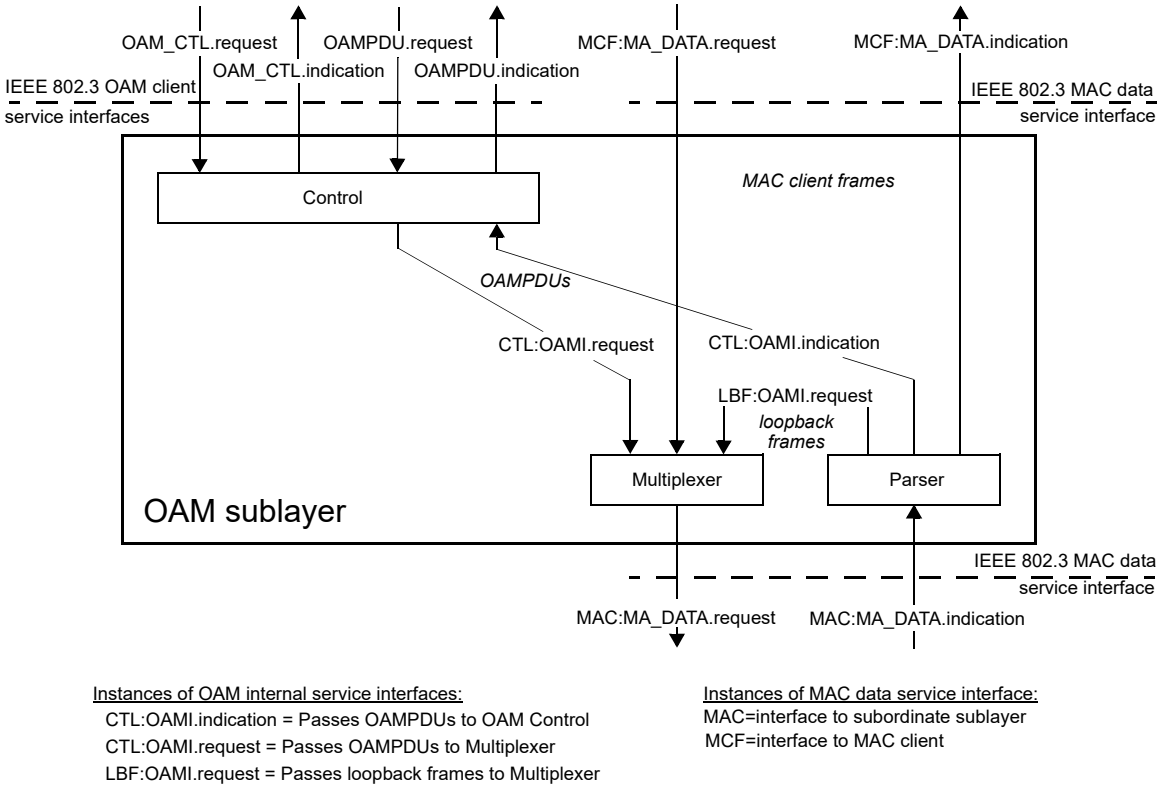

Figure 57–3—OAM sublayer block diagram

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57.2.8 OAM internal interactions

The OAM sublayer entity employs the following new internal service interfaces:
OAMI.request
OAMI.indication

The OAMI.request and OAMI.indication service primitives described in this subclause are mandatory.

57.2.8.1 OAMI.request

57.2.8.1.1 Function

This primitive defines the transfer of frames to the Multiplexer function internal to the OAM sublayer.

57.2.8.1.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
OAMI.request        (
                    destination_address,
                    source_address,
                    oam_service_data_unit,
                        frame_check_sequence
                        )
```

The destination_address parameter specifies the Slow Protocols Multicast Address. The source_address parameter has to specify an individual MAC address. The oam_service_data_unit parameter specifies the OAM service data unit to be transmitted within the OAM sublayer entity. This parameter includes the Length/Type, Subtype, Flags, Code and Data/Pad fields. There is sufficient information associated with the oam_service_data_unit for the OAM sublayer entity to determine the length of the data unit. The frame_check_sequence parameter, if present, has to specify the frame check sequence field for the frame (see 3.2.9).

57.2.8.1.3 When generated

This primitive is generated by the Parser function whenever a frame is intended to be looped back to the remote DTE via the Multiplexer function. This primitive is also generated by the Control function whenever an OAMPDU is to be conveyed to the peer OAM entity via the Multiplexer function, internal to the OAM sublayer.

57.2.8.1.4 Effect of receipt

The receipt of this primitive will cause the Multiplexer function to pass the properly formed frame, subject to Figure 57–7, to the subordinate sublayer via the MAC data service interface (see 57.2.3).

57.2.8.2 OAMI.indication

57.2.8.2.1 Function

This primitive defines the transfer of frames to the Control function internal to the OAM sublayer.

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57.2.8.2.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
OAMI.indication     (
                        destination_address,
                        source_address,
                        oam_service_data_unit,
                        frame_check_sequence,
                        reception_status
                        )
```

The destination_address parameter is the Slow Protocols Multicast Address as specified by the DA field of the incoming frame. The source_address parameter is an individual address as specified by the SA field of the incoming frame. The oam_service_data_unit parameter specifies the OAM service data unit as received by the internal OAM function. The frame_check_sequence parameter, if present, is the cyclic redundancy check value (see 3.2.9) as specified by the FCS field of the incoming frame. The reception_status parameter is used to pass status information to the internal OAM function. Values for the reception_status parameter can be found in 4.3.2.

57.2.8.2.3 When generated

This primitive is generated whenever the Parser function intends to pass a received OAMPDU to the Control function, internal to the OAM sublayer. Frames are reported only if they are validly formed and received without error.

57.2.8.2.4 Effect of receipt

The receipt of this primitive will cause the Control function to update internal state variables and pass the OAMPDU to the OAM client via the OAMPDU.indication service primitive (see 57.2.5.2).

57.2.9 Modes

DTEs incorporating the OAM sublayer support Active and/or Passive mode. When OAM is enabled, a DTE capable of both Active and Passive modes shall select either Active or Passive. Table 57–1 contains the behavior of Active and Passive mode DTEs.

Table 57–1—Active and passive mode behavior

Capability	Active DTE	Passive DTE
Initiates OAM Discovery process	Yes	No
Reacts to OAM Discovery process initiation	Yes	Yes
Required to send Information OAMPDUs	Yes	Yes
Permitted to send Event Notification OAMPDUs	Yes	Yes
Permitted to send Variable Request OAMPDUs	Yes	No
Permitted to send Variable Response OAMPDUs	Yes[a]	Yes
Permitted to send Loopback Control OAMPDUs	Yes	No
Reacts to Loopback Control OAMPDUs	Yes[a]	Yes
Permitted to send Organization Specific OAMPDUs	Yes	Yes

[a]Requires the peer DTE to be in Active mode.

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57.2.9.1 Active mode

DTEs configured in Active mode initiate the exchange of Information OAMPDUs as defined by the Discovery state diagram (see Figure 57–5). Once the Discovery process completes, Active DTEs are permitted to send any OAMPDU while connected to a remote OAM peer entity in Active mode. Active DTEs operate in a limited respect if the remote OAM entity is operating in Passive mode (see Table 57–1). Active devices should not respond to OAM remote loopback commands and variable requests from a Passive peer.

57.2.9.2 Passive mode

DTEs configured in Passive mode do not initiate the Discovery process. Passive DTEs react to the initiation of the Discovery process by the remote DTE. This eliminates the possibility of passive to passive links. Passive DTEs shall not send Variable Request or Loopback Control OAMPDUs.

57.2.10 OAM events

OAM defines a set of events that may impact link operation. OAM contains mechanisms to communicate such events to the remote DTE. The following sections provide an overview of these events and mechanisms.

57.2.10.1 Critical link events

Table 57–2 lists the defined critical link events. Critical link events are carried within the Flags field of each OAMPDU. Refer to 57.4.2.1 for the definition and encoding of the Flags field.

Table 57–2—Critical link event

Critical link event	Description
Link fault	The PHY has determined a fault has occurred in the receive direction of the local DTE.
Dying gasp	An unrecoverable local failure condition has occurred.
Critical event	An unspecified critical event has occurred.

NOTE—The definition of the specific faults comprising the Critical Event, Dying Gasp, and Link Fault flags is implementation specific and beyond the scope of this standard.

57.2.10.2 Link events

Link events are signaled via Link Event TLVs that are defined in 57.5.3. Examples of link events include Errored Symbol Period Event and Errored Frame Event.

57.2.10.3 Local event procedure

Local events are communicated to the remote DTE via one of two mechanisms described as follows:

a) Critical link events, defined in 57.2.10.1, are communicated to the OAM sublayer via the OAM_CTL.request service primitive. The OAM sublayer shall respond to critical link events by setting or clearing the appropriate bits within the Flags field on any subsequently generated OAMPDUs of any type.
b) The OAM client sends an Event Notification OAMPDU (see 57.4.3.2) containing a Link Event TLV (see Table 57–12) for every event not yet signaled to the remote DTE. The OAM client uses the OAMPDU.request service primitive to send Event Notification OAMPDUs. The OAM client may send duplicate Event Notification OAMPDUs to increase the probability of reception at the remote DTE on deteriorating links.

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57.2.10.4 Remote event procedure

Remote events are detected by the local OAM client via one of two mechanisms described as follows:

a) Critical link events, defined in 57.2.10.1, shall be detected by the local OAM sublayer via the Flags field of any received OAMPDU. The OAM sublayer signals the Flags field to the OAM client using the OAMPDU.indication service primitive. When receiving Information OAMPDUs indicating Link Fault from the remote DTE, it is recommended that the local OAM client set the local_link_status parameter in the OAM_CTL.request service primitive to OK. This avoids the situation where both ends of a link are in a deadlock condition where neither DTE will be capable of receiving frames.
b) All other link events shall be detected by the local OAM sublayer via the reception of an Event Notification OAMPDU and the subsequent passing of the OAMPDU to the OAM client via the OAMPDU.indication service primitive. The OAM client discards any duplicate received Event Notification OAMPDU.

57.2.11 OAM remote loopback

OAM provides an optional data link layer frame-level loopback mode, which is controlled remotely. OAM remote loopback can be used for fault localization and link performance testing. Statistics from both the local and remote DTE can be queried and compared at any time while the remote DTE is in OAM remote loopback mode. These queries can take place before, during or after loopback frames have been sent to the remote DTE. In addition, an implementation may analyze loopback frames within the OAM sublayer to determine additional information about the health of the link (i.e., determine which frames are being dropped due to link errors). Figure 57–4 shows the path of frames traversing the layer stack of both the local and remote DTEs.

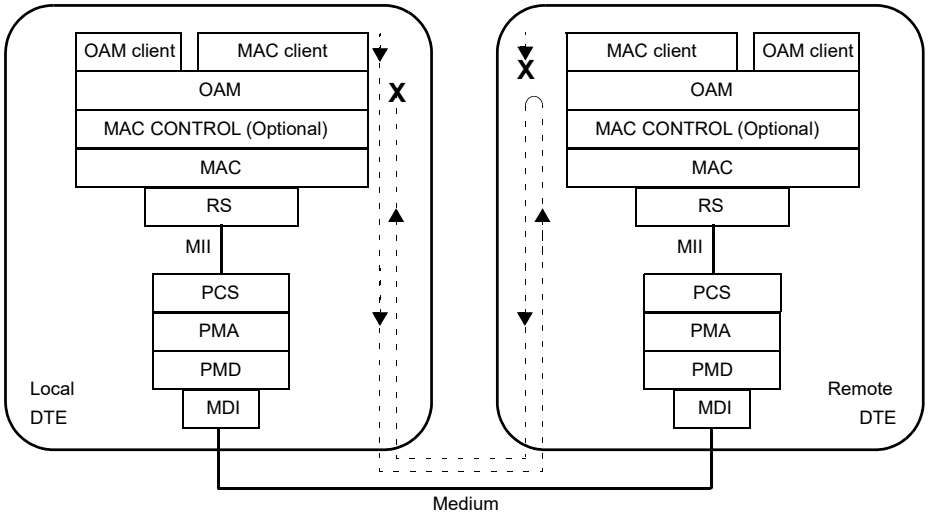

Figure 57–4—OAM remote loopback

57.2.11.1 Initiating OAM remote loopback

To initiate OAM remote loopback, the local OAM client sets its local_mux_action parameter to DISCARD and the local_par_action parameter to DISCARD via the OAM_CTL.request service primitive. The local OAM client sends a Loopback Control OAMPDU (see 57.4.3.5) with the Enable OAM Remote Loopback command. After receiving the Loopback Control OAMPDU, the remote OAM client first sets its local_par_action parameter to LB and its local_mux_action parameter to DISCARD via the OAM_CTL.request service primitive, and then sends an Information OAMPDU with updated state

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information reflecting its local_par_action set to LB and its local_mux_action parameter set to DISCARD. On the reception of an Information OAMPDU from the remote OAM client with updated state information, the local OAM client sets the local_mux_action to FWD.

If an OAM client has sent a Loopback Control OAMPDU and is waiting for the peer DTE to respond with an Information OAMPDU that indicates it is in OAM remote loopback mode, and that OAM client receives an OAM remote loopback command from the peer device, the following procedures are recommended:

a) If the local DTE has a higher source_address than the peer, it should enter OAM remote loopback mode at the command of its peer.
b) If the local DTE has a lower source_address than the peer, it should ignore the OAM remote loopback command from its peer and continue as if it were never received.

If OAM clients do not follow these guidelines, it may be possible for two OAM clients to issue simultaneous OAM remote loopback commands with indeterminate results.

57.2.11.2 During OAM remote loopback

This subclause elaborates on Figure 57–4 and describes the flow of frames within the local and remote DTEs and across the link during OAM remote loopback mode. While in OAM remote loopback mode:

a) The local DTE transmits frames from the MAC client and OAMPDUs from the local OAM client or OAM sublayer.
b) Within the remote OAM sublayer entity, every non-OAMPDU, including other Slow Protocol frames, is looped back without altering any field of the frame.
c) OAMPDUs received by the remote DTE are passed to the remote OAM client.
d) Both DTEs are required to send OAMPDUs to the peer DTE in order to keep the Discovery process from re-starting. Both are also permitted to send other OAMPDUs to the peer DTE.
e) Frames received by the local DTE are parsed by the OAM sublayer. OAMPDUs are passed to the OAM client and all other frames are discarded.

57.2.11.3 Exiting OAM remote loopback

When the local DTE wishes to end the OAM remote loopback test, the local OAM client sets its local_mux_action parameter to DISCARD. The local OAM client then sends a Loopback Control OAMPDU with the Disable OAM Remote Loopback command. After receiving a Loopback Control OAMPDU with the Disable OAM Remote Loopback command, the remote OAM client first sets the local_par_action and local_mux_action parameters to FWD via the OAM_CTL.request service primitive and then sends an Information OAMPDU with updated state information reflecting the local_par_action and local_mux_action parameters set to FWD. After receiving an Information OAMPDU with local_par_action and local_mux_action set to FWD, the local OAM client sets its local_par_action and local_mux_action parameters to FWD via the OAM_CTL.request service primitive. The remote Parser resumes passing received non-OAMPDUs up to the MAC client and the local Multiplexer resumes forwarding any frames sourced by the local MAC client.

57.2.11.4 Loss of OAMPDUs during OAM remote loopback

There is the possibility of OAMPDU loss before, during and after OAM remote loopback tests. Of particular interest to the operation of OAM remote loopback is the loss of Loopback Control OAMPDUs and Information OAMPDUs. The local OAM client is able to determine whether or not the remote OAM client received Loopback Control OAMPDUs by examining all received Information OAMPDUs. Since Information OAMPDUs are continually sent to keep the OAM Discovery process from restarting, the occasional loss of an Information OAMPDU should not adversely impact the operation of OAM remote loopback mode.

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57.2.11.5 Loss of frames during OAM remote loopback

While the link is operating in OAM remote loopback mode, MAC client frames originating from the remote DTE are not transmitted by the remote OAM sublayer entity. Depending upon the remote DTE's implementation of OAM remote loopback, not every frame received is guaranteed to be looped back to the local DTE. Clock differences between the local and remote DTEs may also be a source of lost frames, as the delta in the rate of frames transmitted and received may overrun buffers within either DTE. As always, frames that incur errors during transit will be dropped by the MAC sublayer receiving the frame. Also, OAMPDUs inserted by the remote DTE impacts the bandwidth available to loopback frames. Implementations should take into account the topology (e.g., emulated point-to-point, asymmetrical links) when determining the rate at which to send frames during OAM remote loopback. When a bi-directional link has asymmetric data rates, frame loss may occur if the receive bandwidth is less than the transmit bandwidth.

Loopback frames that are discarded by the OAM sublayer within the remote DTE are counted and, if Clause 30 is present, are reflected in 30.3.6.1.46. This helps determine the health of the link by distinguishing between frames discarded due to link errors and those discarded within the OAM sublayer.

57.2.11.6 Timing considerations for OAM remote loopback

For effective OAM remote loopback operation, it is necessary to place an upper bound on the response time of the remote OAM client after receiving Loopback Control OAMPDUs.

To ensure correct operation, the OAM client needs to, within one second of receiving a Loopback Control OAMPDU with the Enable OAM Remote Loopback command

a) Set its local_par_action parameter to LB and the local_mux_action to DISCARD via the OAM_CTL.request service primitive.
b) Send an Information OAMPDU.

To ensure correct operation, the OAM client needs to, within one second of receiving a Loopback Control OAMPDU with the Disable OAM Remote Loopback command

c) Set its local_par_action and local_mux_action parameters to FWD via the OAM_CTL.request service primitive.
d) Send an Information OAMPDU.

It is possible for the remote MAC client to send frames before the remote OAM client can send the Information OAMPDU instructing the local DTE to change its local_par_action variable. As a result these remote MAC client frames will be discarded by the local DTE.

57.2.12 Unidirectional OAM operation

OAM provides an OAMPDU-based mechanism to notify the remote DTE when one direction of a link is non-operational and therefore data transmission is disabled. The ability to operate a link in a unidirectional mode for diagnostic purposes supports the maintenance objective of failure detection and notification.

Some Physical Layer devices support Unidirectional OAM operation (see 22.2.4.1.12, 22.2.4.2.8, and Clause 66). When a link is operating in Unidirectional OAM mode, the OAM sublayer ensures that only Information OAMPDUs with the Link Fault critical link event indication set and no Information TLVs are sent once per second across the link.

57.3 Detailed functions and state diagrams

As depicted in Figure 57–3, the OAM sublayer comprises the following functions:

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a) ***Multiplexer.*** This function is responsible for passing frames received from the superior sublayer (e.g., MAC client sublayer), OAMPDUs from the Control function and loopback frames from the Parser, to the subordinate sublayer (e.g., MAC sublayer).
b) ***Parser.*** This function distinguishes among OAMPDUs, MAC client frames and loopback frames and passes each to the appropriate entity (Control, superior sublayer and Multiplexer, respectively).
c) ***Control.*** This function is responsible for providing the interface between the OAM client entity and the functions internal to the OAM sublayer. It incorporates the Discovery process which detects the existence and capabilities of OAM at the remote DTE. Also, it includes the Transmit process, which governs the transmission of OAMPDUs to the Multiplexer function and a set of Receive rules, which govern the reception of OAMPDUs.

57.3.1 State diagram variables

57.3.1.1 Constants

OAM_subtype
: The value of the Subtype field for OAMPDUs (see Table 57A–3).

Slow_Protocols_Multicast
: The value of the Slow Protocols Multicast Address. (see Table 57A–1.)

Slow_Protocols_Type
: The value of the Slow Protocols Length/Type field. (see Table 57A–2.)

57.3.1.2 Variables

BEGIN
: A variable that resets the functions within OAM.
Values: TRUE; when the OAM sublayer is reset, or when local_oam_enable is set to DISABLE.
FALSE; When (re-)initialization has completed and local_oam_enable is set to ENABLE.

ind_DA
ind_SA
ind_mac_service_data_unit
ind_reception_status
: The parameters of the MA_DATA.indication service primitive, as defined in Clause 2.

ind_subtype
: The value of the octet following the Length/Type field in a Slow Protocol frame (see Annex 57A).
Value: Integer

local_critical_event
: A parameter of the OAM_CTL.request service primitive, as defined in 57.2.5.3. This indicates the DTE has experienced an unspecified critical event condition.
Values: FALSE; A critical event condition has not occurred.
TRUE; A critical event condition has occurred.

local_dying_gasp
: A parameter of the OAM_CTL.request service primitive, as defined in 57.2.5.3. This indicates the DTE has experienced an unrecoverable failure condition.
Values: FALSE; An unrecoverable local failure condition has not occurred.
TRUE; An unrecoverable local failure condition has occurred.

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local_link_status

A parameter of the OAM_CTL.request service primitive, as defined in 57.2.5.3. This indicates the status of the established link (see 67.6.3).

Values: FAIL; A link fault condition does exist.
OK; A link fault condition does not exist.

local_lost_link_timer_done

A parameter of the OAM_CTL.indication service primitive, as defined in 57.2.5.4. This is used to indicate the local_lost_link_timer has expired.

Values: TRUE; local_lost_link_timer has expired.
FALSE; local_lost_link_timer has not expired.

local_mux_action

A parameter of the OAM_CTL.request service primitive, as defined in 57.2.5.3. This governs the flow of frames from the MAC client through the Multiplexer function (see 57.3.3).

Values: FWD; Multiplexer passes MAC client frames to subordinate sublayer.
DISCARD; Multiplexer discards MAC client frames.

local_oam_enable

Used to enable and disable the OAM sublayer entity. If Clause 30 is present, this maps to 30.3.6.1.2 aOAMAdminState.

Values: DISABLE; The interface acts as it would if it had no OAM sublayer.
ENABLE; The interface employs the OAM sublayer and its functions.

local_oam_mode

Used to configure the OAM sublayer entity in either Active or Passive mode. If Clause 30 is present, this maps to 30.3.3.2 aOAMMode.

Values: PASSIVE; The OAM sublayer entity is configured in Passive mode.
ACTIVE; The OAM sublayer entity is configured in Active mode.

local_par_action

A parameter of the OAM_CTL.request service primitive, as defined in 57.2.5.3. This governs the flow of non-OAMPDUs through the Parser function (see 57.3.4).

Values: FWD; Parser passes received non-OAMPDUs to superior sublayer.
LB; Parser passes received non-OAMPDUs to Multiplexer during remote loopback test.
DISCARD; Parser discards received non-OAMPDUs.

local_pdu

This is used to govern the transmission and reception of OAMPDUs as part of the Discovery process (see 57.3.2.1).

Values: LF_INFO; Only Information OAMPDUs with the Link Fault critical link event set and without Information TLVs are allowed to be transmitted; only Information OAMPDUs are allowed to be received.
RX_INFO; No OAMPDUs are allowed to be transmitted; only Information OAMPDUs are allowed to be received.
INFO; Only Information OAMPDUs are allowed to be transmitted and received.
ANY; Any permissible OAMPDU is allowed to be transmitted and received (see Table 57–1).

local_satisfied

A parameter of the OAM_CTL.request service primitive, as defined in 57.2.5.3. This indicates the OAM client finds the local and remote OAM configuration settings are agreeable.

Values: FALSE; OAM client either has not seen or is not satisfied with local and remote settings.
TRUE; OAM client is satisfied with local and remote settings.

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local_stable
: A variable set by the Discovery state diagram (see Figure 57–5). This is used to indicate local OAM client acknowledgment of and satisfaction with remote OAM state information.
Values: FALSE; Indicates that local DTE either has not seen or is unsatisfied with remote state information.
TRUE; Indicates that local DTE has seen and is satisfied with remote state information.

local_unidirectional
: A parameter of the OAM_CTL.request service primitive, as defined in 57.2.5.3. This indicates the DTE is capable of sending OAMPDUs when the link in the receive direction is not operational.
Values: FALSE; DTE is unable to send OAMPDUs when receive path is not operational.
TRUE; DTE is capable of sending OAMPDUs when receive path is not operational.

pdu_limit
: This variable represents the maximum number of OAMPDUs that are allowed to be transmitted in one second. The value of the pdu_limit variable is equal to the value of the aSlowProtocolFrameLimit attribute (see 30.3.1.1.38).

pdu_req
: This represents a request to send an OAMPDU and is used within the Transmit state diagram (see Figure 57–6).
Values: NONE: No OAMPDU.request
CRITICAL: OAMPDU.request with one or more critical link event OAM_CTL.request parameters set (local_dying_gasp, local_link_status, local_critical_event).
NORMAL: OAMPDU.request with no critical link event(s) set.

remote_stable
: A parameter of the OAM_CTL.request service primitive, as defined in 57.2.5.3. OAM client extracts remote state information from received OAMPDUs. This is used to indicate remote OAM client acknowledgment of and satisfaction with local OAM state information.
Values: FALSE; Indicates that remote DTE either has not seen or is unsatisfied with local state information.
TRUE; Indicates that remote DTE has seen and is satisfied with local state information.

remote_state_valid
: A parameter of the OAM_CTL.request service primitive, as defined in 57.2.5.3. This is used to indicate OAM client has received remote state information found within Local Information TLVs of received Information OAMPDUs.
Values: FALSE; Indicates that OAM client has not seen remote state information.
TRUE; Indicates that OAM client has seen remote state information.

req_DA
req_SA
req_mac_service_data_unit
req_frame_check_sequence
: The parameters of the MA_DATA.request service primitive, as defined in Clause 2.

57.3.1.3 Messages

CTL:OAMI.indication
: The service primitive used to pass a received frame to an internal OAM function with the specified parameters.

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CTL:OAMI.request
LBF:OAMI.request
The service primitives used to transmit a frame with the specified parameters.

MAC:MA_DATA.indication
MCF:MA_DATA.indication
The service primitives used to pass a received frame to a client with the specified parameters.

MAC:MA_DATA.request
MCF:MA_DATA.request
The service primitives used to transmit a frame with the specified parameters.

MADI
Alias for
MA_DATA.indication(ind_DA, ind_SA, ind_mac_service_data_unit, ind_reception_status)

MADR
Alias for
MA_DATA.request(req_DA, req_SA, req_mac_service_data_unit, req_frame_check_sequence)

OAMII
Alias for
OAMI.indication(DA, SA, oam_service_data_unit, frame_check_sequence, reception_status)

OAMIR
Alias for
OAMI.request(DA, SA, oam_service_data_unit, frame_check_sequence)

RxOAMPDU
Alias for ind_DA = Slow_Protocols_Multicast * ind_Length/Type = Slow_Protocols_Type * ind_subtype = OAM_subtype

rxOK
Alias for ind_reception_status = receiveOK

valid_pdu_req
Alias for the following term:
(local_pdu≠RX_INFO * pdu_req=NORMAL * pdu_cnt≠0)
+ (local_pdu=ANY * pdu_req=CRITICAL)

57.3.1.4 Counters

pdu_cnt
This counter is used to limit the number of OAMPDUs transmitted per second and ensure at least one OAMPDU is sent each second within the Transmit state diagram (see Figure 57–6).

57.3.1.5 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where 'stop x_timer' is asserted.

local_lost_link_timer
Timer used to reset the Discovery state diagram (see Figure 57–5).
Duration: 5 s ± 10%.

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pdu_timer
: Timer used to ensure OAM sublayer adheres to maximum number of OAMPDUs per second and emits at least one OAMPDU per second.
Duration: 1 s ± 10%.

57.3.2 Control

The Control function provides the interfaces with the OAM client necessary to transmit and receive OAMPDUs and convey control and status parameters. The Control function also contains the Discovery process, which enables OAM to be established on a link, and the Transmit process, which governs the transmission of OAMPDUs to the Multiplexer block. Rules governing the reception of OAMPDUs are also contained within the Control function.

57.3.2.1 OAM Discovery

OAM provides a mechanism to detect the presence of an OAM sublayer at the remote DTE. This mechanism is called Discovery. OAM sublayer entities shall implement the OAM Discovery state diagram shown in Figure 57–5.

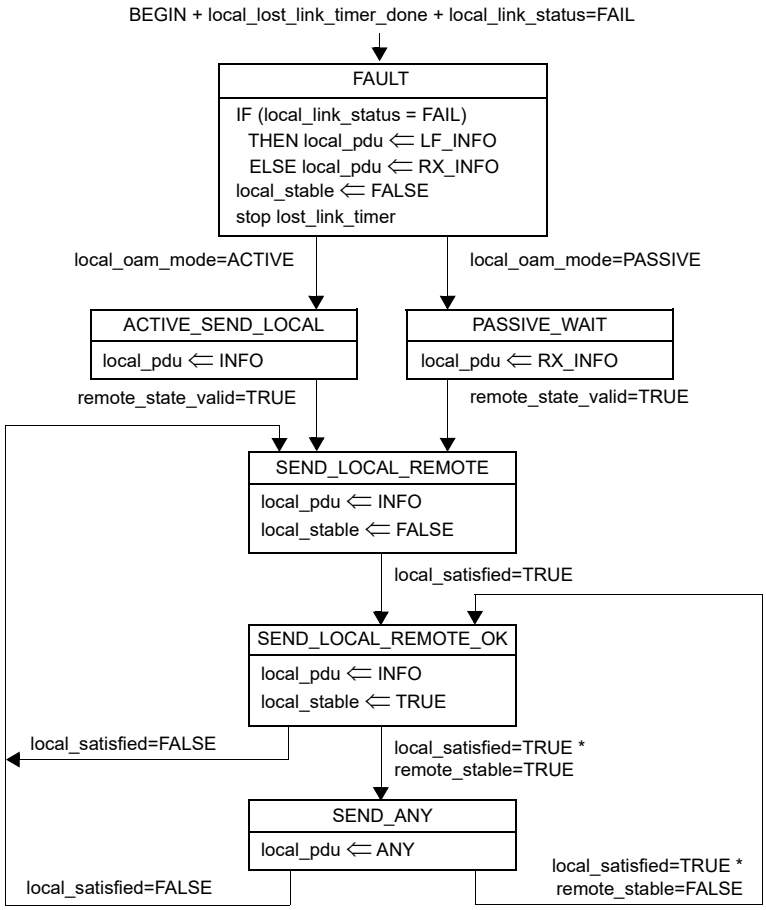

Figure 57–5—OAM Discovery state diagram

In each state, the OAM sublayer sends specified OAMPDUs in a periodic fashion, normally once a second. When local_pdu is set to LF_INFO, the OAM sublayer sends Information OAMPDUs with the Link Fault bit of the Flags field set and without any Information TLVs. When local_pdu is set to RX_INFO, the OAM

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sublayer does not send any OAMPDUs. When local_pdu is set to INFO, only Information OAMPDUs are sent. When local_pdu is set to ANY, all permissible OAMPDUs may be sent, subject to the restrictions found in Table 57–1.

57.3.2.1.1 FAULT state

Upon entering the FAULT state, local_pdu is set based on the value of local_link_status. If it is set to FAIL, local_pdu is set to LF_INFO, otherwise is it set to RX_INFO. Then, local_stable is set to FALSE and local_lost_link_timer is stopped. While local_link_status is set to FAIL, the DTE will remain in this state indicating to the remote DTE there is link fault. This is accomplished by sending Information OAMPDUs once per second with the Link Fault bit of the Flags field set and no Information TLVs in the Data field. The unidirectional transmission of Information OAMPDUs is supported by some physical coding sublayers (see 57.2.12).

If OAM is reset, disabled, the local_lost_link_timer expires or the local_link_status equals FAIL, the Discovery process returns to the FAULT state.

57.3.2.1.2 ACTIVE_SEND_LOCAL state

Once local_link_status is set to OK, the DTE evaluates local_oam_mode. A DTE configured in Active mode (see 57.2.9.1) sends Information OAMPDUs that only contain the Local Information TLV (see 57.5.2.1). This state is called ACTIVE_SEND_LOCAL. While in this state, the local DTE waits for Information OAMPDUs received from the remote DTE.

57.3.2.1.3 PASSIVE_WAIT state

A DTE configured in Passive mode (see 57.2.9.2) waits until receiving Information OAMPDUs with Local Information TLVs before sending any Information OAMPDUs with Local Information TLVs. This state is called PASSIVE_WAIT. By waiting until first receiving an Information OAMPDU with the Local Information TLV, a Passive DTE cannot complete the OAM Discovery process when connected to another Passive DTE.

57.3.2.1.4 SEND_LOCAL_REMOTE state

Once the local DTE has received an Information OAMPDU with the Local Information TLV from the remote DTE, the local DTE begins sending Information OAMPDUs that contain both the Local and Remote Information TLVs. This state is called SEND_LOCAL_REMOTE. If at any time the settings on either the local or remote DTE change resulting in the local OAM client becoming unsatisfied with the settings, the Discovery process returns to the SEND_LOCAL_REMOTE state.

57.3.2.1.5 SEND_LOCAL_REMOTE_OK state

If the local OAM client deems the settings on both the local and remote DTEs are acceptable, it enters the SEND_LOCAL_REMOTE_OK state. If at any time the settings on the local OAM client change resulting in the remote OAM client becoming unsatisfied with the settings, the OAM Discovery process returns to the SEND_LOCAL_REMOTE_OK state.

57.3.2.1.6 SEND_ANY state

Finally, once an OAMPDU has been received indicating the remote device is satisfied with the respective settings, the local device enters the SEND_ANY state. This is the expected normal operating state for OAM on fully operational links.

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57.3.2.1.7 Sending Discovery status to peer

The Local Stable and Local Evaluating bits of the Flags field communicate the status of the local Discovery process to the peer. When the OAM Discovery process is started, the local DTE sets the Local Stable to 0 and Local Evaluating bits to 1 indicating OAM Discovery has not completed.

If, after learning of the remote OAM settings, the local OAM client determines it is unsatisfied it sets the Local Stable and Local Evaluating bits to 0 indicating Discovery cannot successfully complete. If the local OAM client is satisfied, the local DTE sets the Local Stable bit to 1 and Local Evaluating bit to 0 indicating the local OAM client is satisfied.

When Local Stable is set to 1 and Local Evaluating is set to 0 and Remote Stable is set to 1 and Remote Evaluating is set to 0 indicating that both OAM clients are satisfied, the OAM Discovery process has successfully completed and local_pdu is set to ANY. See Table 57–3 for more information.

57.3.2.2 Transmit

OAM sublayer entities shall implement the Transmit state diagram shown in Figure 57–6.

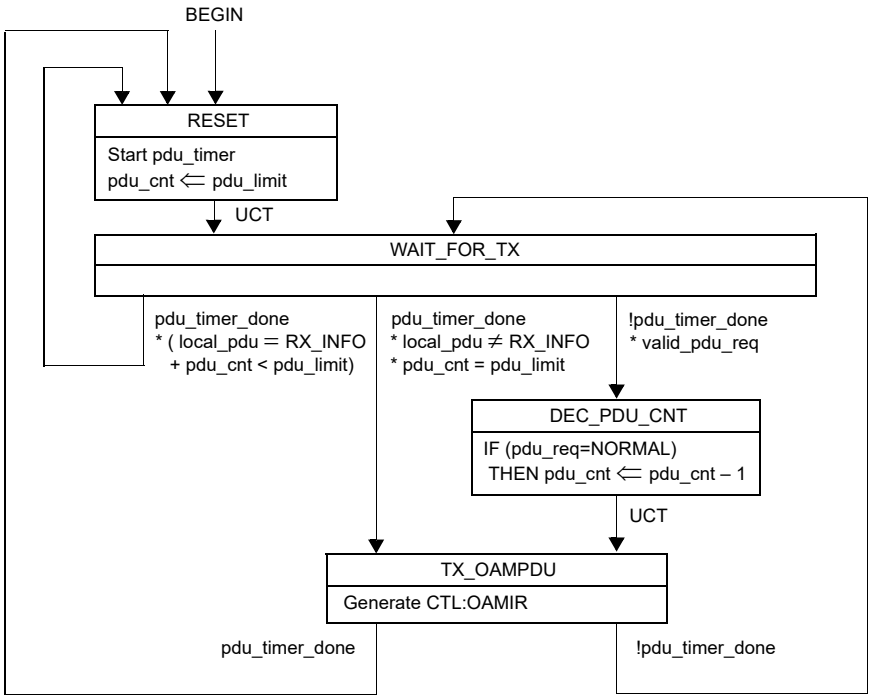

Figure 57–6—Transmit state diagram

57.3.2.2.1 RESET state

Upon initialization, the RESET state is entered. A one second timer is started called pdu_timer. The pdu_cnt variable is reset with a value of ten, the maximum number of OAMPDUs that may be sent in one second. Following RESET, the WAIT_FOR_TX state is entered.

57.3.2.2.2 WAIT_FOR_TX state

While in the WAIT_FOR_TX state, the Transmit process waits for the occurrence of one of three conditions. These three conditions are summarized as follows:

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a) Expiration of pdu_timer:
   1) With one or more OAMPDUs sent within the last second
   2) Without any OAMPDUs being sent within the last second and without a valid pending request to send an OAMPDU
b) Valid request to send an OAMPDU present

57.3.2.2.3 Expiration of pdu_timer

While in the WAIT_FOR_TX state, if the pdu_timer expires and one or more OAMPDUs have been sent within the last second, the Transmit process transitions to the RESET state. If, however, the pdu_timer expires and no OAMPDUs have been sent within the last second and there is no valid request to send an OAMPDU present, the Transmit process transitions to the TX_OAMPDU state sending an Information OAMPDU. This prevents the Discovery process from restarting. If local_pdu is set to LF_INFO, the Transmit process ensures the Information OAMPDU has the Link Fault bit of the Flags field set and has no Information TLVs in the Data field.

If, however, the OAM sublayer entity is configured to not send any OAMPDUs, as indicated by the local_pdu variable set to RX_INFO, the Transmit function will simply restart the pdu_timer by returning to the RESET state.

57.3.2.2.4 Valid request to send an OAMPDU

While in the WAIT_FOR_TX state, if a valid request to send an OAMPDU is present, the Transmit process transmits the requested OAMPDU in the TX_OAMPDU state. If the Flags field of the OAMPDU to be sent does not contain any critical link events, the pdu_cnt variable is decremented in the DEC_PDU_CNT state. A valid request is either one of the following:

a) An OAMPDU.request service primitive from the OAM client with the local_pdu variable set to INFO or ANY and pdu_cnt not equal to zero.
b) An OAM_CTL.request service primitive from the OAM client with one or more critical event parameters set and the local_pdu variable set to ANY. When the local_pdu variable is set to ANY, the Discovery process has completed and is in the SEND_ANY state. The Discovery process needs to complete before critical events, other than Link Fault, may be sent to the peer OAM entity.

57.3.2.2.5 TX_OAMPDU state

The TX_OAMDPU state generates the CTL:OAMI.request service primitive, which requests the transmission of an OAMPDU to the Multiplexer process. After generating the request, the Transmit process returns to the RESET state if the pdu_timer is expired or the WAIT_FOR_TX state if the pdu_timer has not expired.

57.3.2.2.6 Transmit rules

The following rules govern the generation of the CTL:OAMIR service primitive:

a) While local_pdu is set to LF_INFO, only Information OAMPDUs with the Link Fault bit of the Flags field set and without any Information TLVs shall be generated.
b) While local_pdu is set to RX_INFO, CTL:OAMIR service primitives shall not be generated.
c) While local_pdu is set to INFO, only Information OAMPDUs shall be generated.
d) While local_pdu is set to ANY:
   1) An OAM_CTL.request service primitive with one or more of the critical link event parameters set shall generate a CTL:OAMIR service primitive, requesting the transmission of an Information OAMPDU with the appropriate bit(s) of the Flags field set.
   2) An OAMPDU.request service primitive shall generate a CTL:OAMIR service primitive, requesting the transmission of the particular OAMPDU.

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57.3.2.3 Receive rules

CTL:OAMII service primitives indicate a received OAMPDU and in turn generate an OAMPDU.indication service primitive to the OAM client entity subject to the following rules:

a) When local_pdu is not set to ANY, Information OAMPDUs shall be passed to the OAM client and non-Information OAMPDUs are discarded.
b) When local_pdu is set to ANY, all OAMPDUs, including those with unknown Code fields shall be passed to the OAM client.[109] It is anticipated that the OAM client will ignore unknown or unsupported OAMPDUs.

57.3.3 Multiplexer

OAM sublayer entities shall implement the Multiplexer state diagram shown in Figure 57–7.

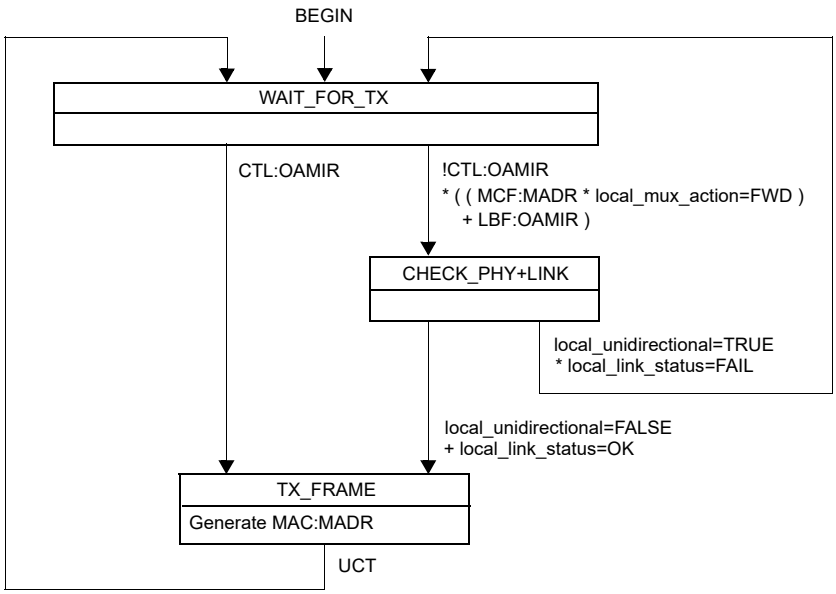

Figure 57–7—Multiplexer state diagram

57.3.3.1 WAIT_FOR_TX state

Upon initialization, the WAIT_FOR_TX state is entered. While in the WAIT_FOR_TX state, the Multiplexer waits for the occurrence of one of two conditions. These two conditions are summarized as follows:

a) Valid request to send an OAMPDU present
b) Valid request to forward a MAC client frame or loopback frame from Parser

57.3.3.1.1 Valid request to send an OAMPDU

While in the WAIT_FOR_TX state, if a request to send an OAMPDU is present, the Multiplexer function transmits the requested OAMPDU in the TX_FRAME state.

[109]The behavior of the OAM sublayer is different in this regard from the behavior of the MAC Control sublayer (see Clause 31 and Clause 64).

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57.3.3.1.2 Valid request to forward or loopback frame

While in the WAIT_FOR_TX state, if a valid request to forward or loop back a frame is present and no request to send an OAMPDU is present, the Multiplexer will then check the status of the underlying Physical Layer and unidirectional configuration (in the CHECK_PHY+LINK state) and either transmit the frame in the TX_FRAME state or simply return to the WAIT_FOR_TX state.

A valid request to forward a frame from the superior sublayer is indicated by the variable MCF:MADR with the Multiplexer configured to forward frames as indicated by the local_mux_action variable set to FWD. A request to loop back a frame from the Parser function is indicated by the variable LBF:OAMIR. When either request occurs, the local_unidirectional variable needs to be FALSE or the local_link_status variable needs to be OK in order for the frame to be sent to the subordinate sublayer via the TX_FRAME state. Since only Information OAMPDUs with the Link Fault critical link event indication set and no Information TLVs are sent on a unidirectional link, the status of the link is evaluated to ensure the same behavior as devices that do not support the optional Unidirectional OAM capability. When the local_link_status variable is OK, the MAC client frame will be transmitted regardless of the Unidirectional OAM capability or setting (see 57.2.12).

57.3.3.2 TX_FRAME state

Once the Multiplexer process reaches the TX_FRAME state, it shall provide transparent pass-through of frames submitted by the superior sublayer, the Transmit process and the Parser process. The transmission of an OAMPDU shall not affect the transmission of a frame that has been submitted to the subordinate sublayer (i.e., the MAC's TransmitFrame function is synchronous, and is never interrupted). After the frame has been sent to the subordinate sublayer, the Multiplexer process returns to the WAIT_FOR_TX state.

57.3.4 Parser

OAM sublayer entities shall implement the Parser state diagram shown in Figure 57–8.

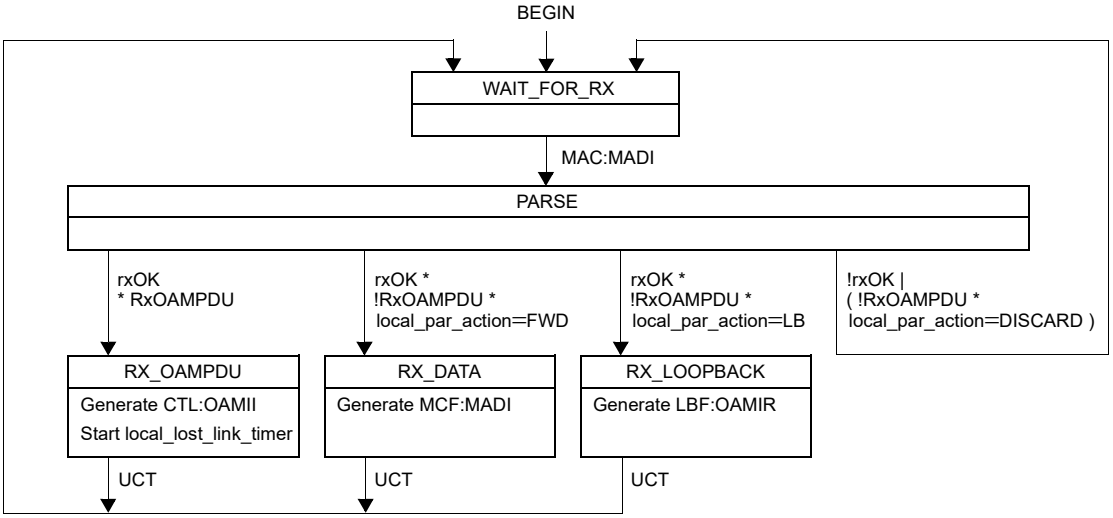

Figure 57–8—Parser state diagram

The Parser decodes frames received from the subordinate sublayer, passes OAMPDUs to the Control function, MAC client frames to the superior sublayer and loopback frames to the Multiplexer function. After reset, the Parser function enters the WAIT_FOR_RX state. The reception of a frame is detected when the MAC:MADI service primitive occurs. When a frame is received, the Parser function enters the PARSE state.

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57.3.4.1 Reception of OAMPDU

The RX_OAMPDU state is entered when the receive frame is identified as an OAMPDU. Received OAMPDUs are sent to the OAM Control function via the CTL:OAMII service primitive. Following the receive rules in 57.3.2.3, the OAM Control function then passes the received OAMPDU to the OAM client. In addition, the local_lost_link_timer is reset. The Parser function then returns to the WAIT_FOR_RX state.

57.3.4.2 Reception of non-OAMPDUs

Received non-OAMPDUs are handled according to the setting of the local_par_action parameter. Refer to 57.2.11 for a complete description of OAM remote loopback operation and the local_par_action variable.

57.3.4.2.1 Reception of non-OAMPDU in FWD mode

The RX_DATA state is entered if the frame is determined to not be an OAMPDU and the local_par_action variable is set to FWD. The received frame is passed up to the superior sublayer via the MCF:MADI service primitive. The Parser then returns to the WAIT_FOR_RX state.

57.3.4.2.2 Reception of non-OAMPDU in LB mode

The RX_LOOPBACK state is entered if the frame is determined to not be an OAMPDU and the local_par_action parameter is set to LB. The received loopback frame is passed to the Multiplexer function via the LBF:OAMIR service primitive to be looped back to the remote DTE. After the frame is passed to the Multiplexer function, the Parser function returns to the WAIT_FOR_RX state.

57.3.4.2.3 Reception of non-OAMPDU in DISCARD mode

If the local_par_action parameter is set to DISCARD, the Parser function simply returns to the WAIT_FOR_RX state.

57.4 OAMPDUs

57.4.1 Ordering and representation of octets

All OAMPDUs comprise an integral number of octets. When the encoding of (an element of) an OAMPDU is depicted in a diagram:

a) Octets are transmitted from top to bottom.
b) Within an octet, bits are shown with bit 0 to the left and bit 7 to the right.
c) When consecutive octets are used to represent a binary number, the octet transmitted first has the more significant value.
d) When consecutive octets are used to represent a MAC address, the least significant bit of the first octet is assigned the value of the first bit of the MAC address, the next most significant bit the value of the second bit of the MAC address, and so on for all the octets of the MAC address.

When the encoding of an element of an OAMPDU is depicted in a table, the least significant bit is bit 0.

The bit/octet ordering of any Organizationally Unique Identifier (OUI) or Company ID (CID) field within an OAMPDU is identical to the bit/octet ordering of the OUI portion of the DA/SA. Additional detail defining the format of OUIs and CIDs can be found in IEEE Std 802 Overview and Architecture.

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57.4.2 Structure

The OAMPDU structure shall be as shown in Figure 57–9.

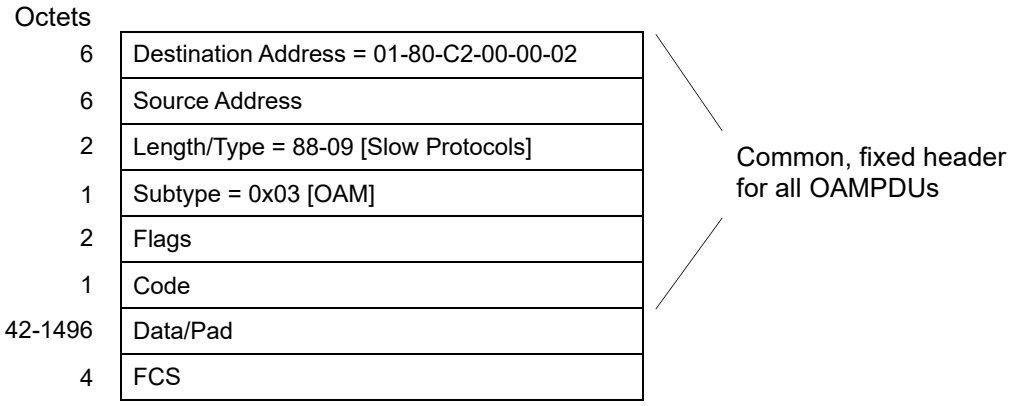

Figure 57–9—OAMPDU frame structure

OAMPDUs shall have the following fields:

a) ***Destination Address*** (DA). The DA in OAMPDUs is the Slow_Protocols_Multicast address. Its use and encoding are specified in Annex 57A.
b) ***Source Address*** (SA). The SA in OAMPDUs carries the individual MAC address associated with the port through which the OAMPDU is transmitted.
c) ***Length/Type***. The Length/Type in OAMPDUs carries the Slow_Protocols_Type field value as specified in 57A.4.
d) ***Subtype***. The Subtype field identifies the specific Slow Protocol being encapsulated. OAMPDUs carry the Subtype value 0x03.
e) ***Flags***. The Flags field contains status bits as defined in 57.4.2.1.
f) ***Code***. The Code field identifies the specific OAMPDU. The use and encoding of this field is specified in Table 57–4.
g) ***Data/Pad***. This field contains the OAMPDU data and any necessary pad. Implementations shall support OAMPDUs at least minFrameSize in length.
h) ***FCS***. This field is the Frame Check Sequence, as defined in Clause 4.

57.4.2.1 Flags field

The Flags field is encoded as individual bits within two octets as shown in Table 57–3. Additional diagnostic information may be sent using the Event Notification OAMPDU.

Table 57–3—Flags field

Bit(s)	Name	Description
15:7	Reserved	Reserved bits shall be set to zero when sending an OAMPDU, and should be ignored on reception for compatibility with future use of reserved bits.
6	Remote Stable	When remote_state_valid is set to TRUE, the Remote Stable and Remote Evaluating values shall be a copy of the last valid received Local Stable and Local Evaluating values from the remote OAM peer. Otherwise, the Remote Stable and Remote Evaluating bits shall be set to 0.
5	Remote Evaluating	

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Table 57–3—Flags field *(continued)*

Bit(s)	Name	Description
4	Local Stable	Local Stable and Local Evaluating form a two-bit encoding shown below: 4:3 0x0 = Local DTE Unsatisfied, Discovery can not complete 0x1 = Local DTE Discovery process has not completed 0x2 = Local DTE Discovery process has completed 0x3 = Reserved. This value shall not be sent. If the value 0x3 is received, it should be ignored and not change the last received value.
3	Local Evaluating	
2	Critical Event	1 = A critical event has occurred. 0 = A critical event has not occurred.
1	Dying Gasp	1 = An unrecoverable local failure condition has occurred. 0 = An unrecoverable local failure condition has not occurred.
0	Link Fault	The PHY has detected a fault has occurred in the receive direction of the local DTE (e.g., link, Physical Layer). 1 = Local device's receive path has detected a fault. 0 = Local device's receive path has not detected a fault.

NOTE—The definition of the specific faults comprising the Critical Event, Dying Gasp, and Link Fault flags is implementation specific and beyond the scope of this standard.

57.4.2.2 Code field

The value of the Code field is set by the Transmit process in the Control function for Information OAMPDUs it generates. The OAM client sets the Code field for all OAMPDUs it generates. Table 57–4 contains the defined OAMPDU codes.

Table 57–4—OAMPDU codes

Code	OAMPDU	Comment	Source
00	Information	Communicates local and remote OAM information.	OAM client / OAM sublayer
01	Event Notification	Alerts remote DTE of link event(s).	OAM client
02	Variable Request	Requests one or more specific MIB variables.	OAM client
03	Variable Response	Returns one or more specific MIB variables.	OAM client
04	Loopback Control	Enables/disables OAM remote loopback.	OAM client
05-FD	Reserved	Reserved	OAM client
FE	Organization Specific	Organization Specific Extensions, distinguished by Organizationally Unique Identifier.	OAM client
FF	Reserved	Reserved	OAM client

57.4.3 OAMPDU descriptions

The local OAM sublayer communicates with the remote OAM sublayer via OAMPDUs. OAMPDUs are identified with a specific code. OAMPDUs are formatted as compliant IEEE 802.3 frames, where the IEEE 802.3 frame header format is described in Clause 3. OAMPDUs are further defined, as shown in Figure 57–9, to include a Subtype field, a Flags field, and a Code field following the IEEE 802.3 defined Length/Type field. The Data field begins in a fixed location within the OAMPDU. The Data field contents are unique to the particular OAMPDU. The following sections provide a detailed description of each OAMPDU and its corresponding Data field. All received OAMPDUs, including those with reserved Code fields, are passed to the OAM client. OAMPDUs with reserved Code field values shall not be transmitted.

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57.4.3.1 Information OAMPDU

The Information OAMPDU, identified by the Code field 0x00, is used to send OAM state information to the remote DTE. The Information OAMPDU frame structure shall be as depicted in Figure 57–10.

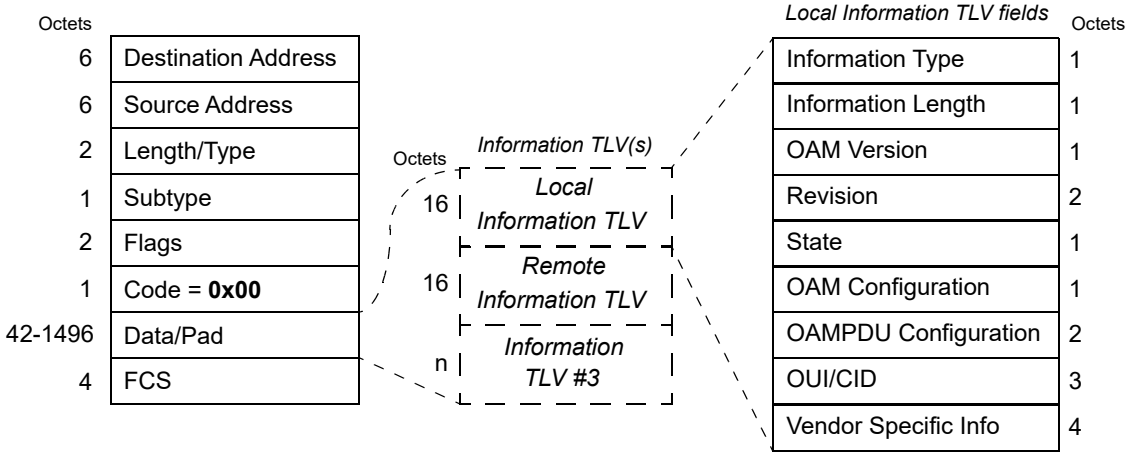

Figure 57–10—Information OAMPDU frame structure

When local_pdu is set to LF_INFO, the Information OAMPDU Data field shall not have any Information TLVs. When local_pdu is not set to LF_INFO, the Information OAMPDU Data field shall consist of the Local Information TLV (see 57.5.2.1) immediately following the Code field. In addition, if the Discovery state diagram variable remote_state_valid is TRUE, the Data field shall also contain the Remote Information TLV (see 57.5.2.2), immediately following the Local Information TLV and may also contain other Information TLVs found in Table 57–6.

57.4.3.2 Event Notification OAMPDU

The optional Event Notification OAMPDU, identified with the Code field set to 0x01, is used to alert the remote DTE of link events introduced in 57.2.10.2. The Event Notification OAMPDU frame structure shall be as depicted in Figure 57–11.

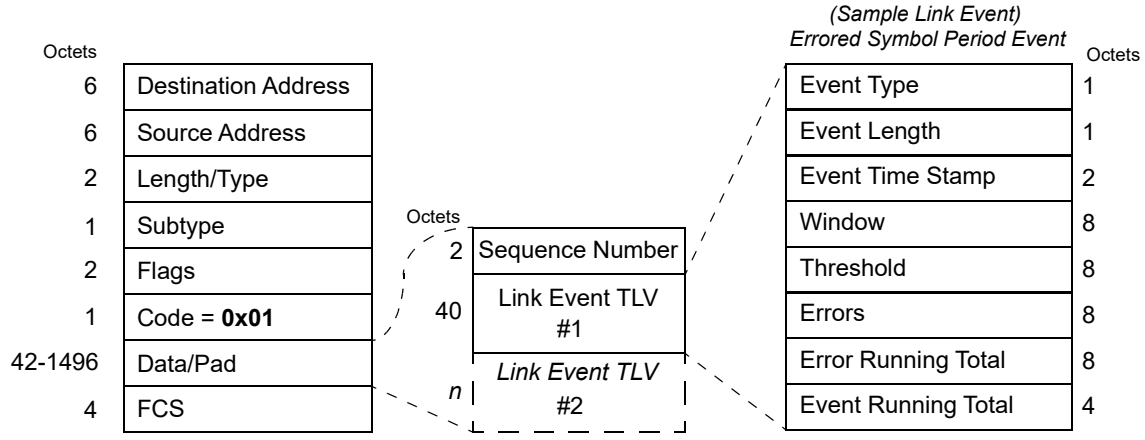

Figure 57–11—Event Notification OAMPDU frame structure

The first two octets of the Data field shall contain a Sequence Number, encoded as a 16-bit unsigned integer. As described in 57.2.3, the OAM client may send duplicate Event Notification OAMPDUs to increase the likelihood the remote DTE receives a particular event. The OAM client increments the Sequence Number

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for each unique Event Notification OAMPDU formed by the OAM client. A particular Event Notification OAMPDU may be sent multiple times with the same sequence number. It is recommended that any duplicate Event Notification OAMPDUs follow its original without a different, intervening Event Notification OAMPDU. A duplicate Event Notification OAMPDU should not be transmitted if a new Event Notification OAMPDU has already followed the original OAMPDU. Any particular event can be signaled in only one unique Event Notification OAMPDU (though that OAMPDU may be transmitted multiple times). Upon receiving an Event Notification OAMPDU, the OAM client compares the Sequence Number with the last received Sequence Number. If equal, the current event is a duplicate and is ignored by the OAM client.

Following the Sequence Number field, the Data field shall contain one or more optional Link Event TLVs which may provide useful information for troubleshooting events and faults. Link Event TLVs are defined in 57.5.3.

57.4.3.3 Variable Request OAMPDU

The optional Variable Request OAMPDU, identified with a Code field of 0x02, is used to request one or more MIB variables from the remote DTE. The Variable Request OAMPDU frame structure shall be as depicted in Figure 57–12.

The Variable Request OAMPDU Data field shall contain one or more Variable Descriptors. Variable Descriptors are defined in 57.6.1.

The Variable Request OAMPDU Data field may contain one or more Variable Containers, to determine the scope of subsequent Variable Descriptors, as described in 57.6.2.

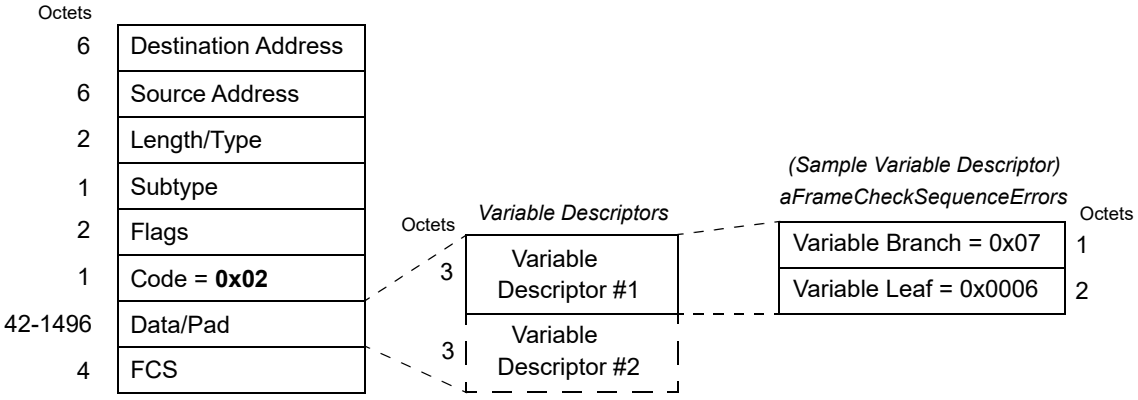

Figure 57–12—Variable Request OAMPDU frame structure

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57.4.3.4 Variable Response OAMPDU

The optional Variable Response OAMPDU, identified with the Code field of 0x03, is used to return one or more MIB variables. The Variable Response OAMPDU frame structure shall be as depicted in Figure 57–13.

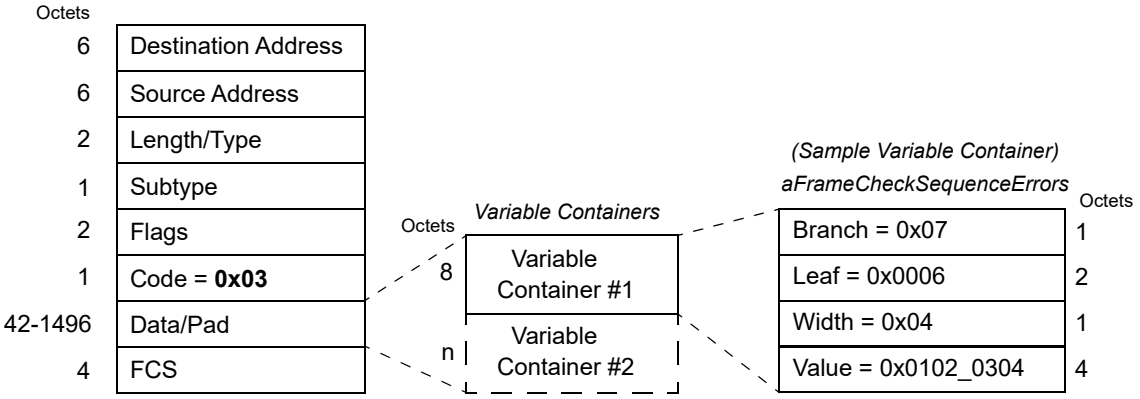

Figure 57–13—Variable Response OAMPDU frame structure

The Variable Response OAMPDU Data field shall contain one or more Variable Containers. Variable Containers are defined in 57.6.2. A Variable Response OAMPDU needs to be sent by the OAM client within one second of receipt of a Variable Request OAMPDU. If a DTE is unable to retrieve one or more variables, it needs to respond within one second and indicate the appropriate error(s) as found in Table 57–17. If a DTE is unable to retrieve one or more attributes within a package or object, it needs to either a) return the appropriate Variable Indication for the particular attribute(s) and return all other requested variables or b) return a Variable Indication for the entire package or object.

57.4.3.5 Loopback Control OAMPDU

The optional Loopback Control OAMPDU, identified with the Code field set to 0x04, is used to control the remote DTE's OAM remote loopback state. The Loopback Control OAMPDU frame structure shall be as depicted in Figure 57–14.

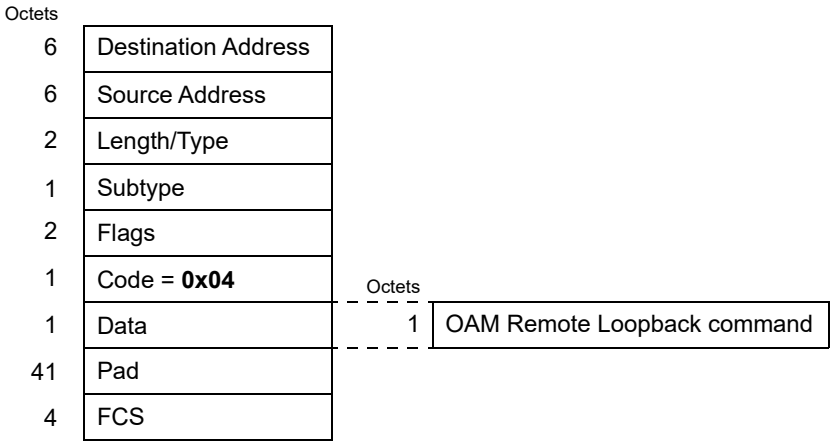

Figure 57–14—Loopback Control OAMPDU frame structure

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The Loopback Control OAMPDU Data field shall consist of an OAM remote loopback command. Table 57–5 lists the defined OAM remote loopback commands.

Table 57–5—OAM remote loopback commands

Command	Description
0x00	Reserved — shall not be transmitted, should be ignored on reception by OAM client
0x01	Enable OAM Remote Loopback
0x02	Disable OAM Remote Loopback
0x03–0xFF	Reserved — shall not be transmitted, should be ignored on reception by OAM client

For a complete description of OAM remote loopback refer to 57.2.11.

57.4.3.6 Organization Specific OAMPDU

The optional Organization Specific OAMPDU, identified with the Code field set to 0xFE, is used for organization specific extensions. The Organization Specific OAMPDU frame structure shall be as depicted in Figure 57–15.

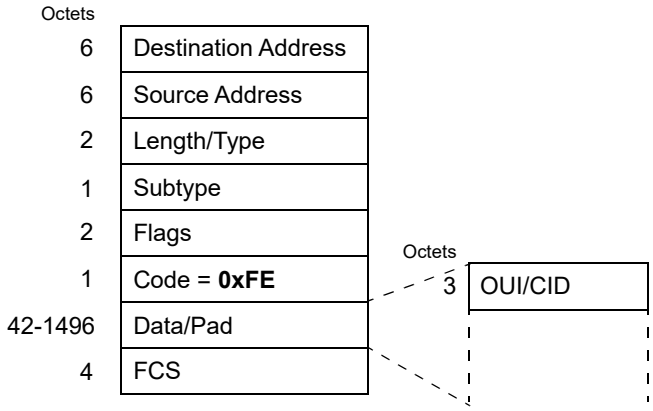

Figure 57–15—Organization Specific OAMPDU frame structure

The first three octets of the Organization Specific OAMPDU Data field shall contain the Organizationally Unique Identifier (OUI) or Company ID (CID).[110] The format and function of the rest of the Organization Specific OAMPDU Data field is dependent on OUI or CID value and is beyond the scope of this standard.

57.5 OAM TLVs

57.5.1 Parsing

The OAM client parses OAM TLVs. All OAM TLVs contain a single octet Type field and a single octet Length field. The Length field encompasses the entire TLV including the Type and Length fields. TLV processing should follow these recommendations:

a) Detection of a TLV type 0x00 should indicate there are no more TLVs to process (the length and value of the Type 0x00 TLV can be ignored).
b) TLVs with lengths 0x00 or 0x01 should be considered invalid, and the OAMPDU should be considered to have no more TLVs.
c) TLVs with unknown or unexpected types should be ignored.

[110]Interested applicants should contact the IEEE Standards Department, Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854, USA, https://standards.ieee.org/regauth/index.html.

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d) If the length of a TLV is less than that defined for the Type, that TLV should be ignored and the rest of the frame may be ignored. If the length of a TLV is greater than that defined for the Type, the expected fields of the TLV should be processed, and the remainder of the frame after the TLV should also be processed.
e) If a TLV length indicates that the TLV extends beyond the frame (e.g., the length cannot fit into the frame given its length and starting point), then the TLV should be ignored.

57.5.2 Information TLVs

This subclause contains the definitions for Information TLVs. Information TLVs are found in Information OAMPDUs. Table 57–6 contains the defined Information TLVs.

Table 57–6—Information TLV types

Type	Description
0x00	*End of TLV marker*
0x01	Local Information
0x02	Remote Information
0x03–0xFD	Reserved—shall not be transmitted, should be ignored on reception by OAM client
0xFE	Organization Specific Information
0xFF	Reserved—shall not be transmitted, should be ignored on reception by OAM client

The following subclauses describe the defined Information TLVs.

57.5.2.1 Local Information TLV

The Local Information TLV shall have the following fields:

a) ***Information Type*** = *Local Information*. This one-octet field indicates the nature of the data carried in this TLV-tuple. The encoding of this field is found in Table 57–6.
b) ***Information Length***. The one-octet field indicates the length (in octets) of this TLV-tuple. Local Information TLV uses a length value of 16 (0x10).
c) ***OAM Version***. This one-octet field indicates the version supported by the DTE. This field shall contain the value 0x01 to claim compliance with Version 1 of this protocol.
d) ***Revision.*** This two-octet field indicates the current revision of the Information TLV. The value of this field shall start at zero and be incremented each time something in the Information TLV changes. Upon reception of an Information TLV from a peer, an OAM client may use this field to decide if it needs to be processed (an Information TLV that is identical to the previous Information TLV does not need to be parsed as nothing in it has changed).
e) ***State***. This one-octet field contains OAM state information and shall be as shown in Table 57–7.
f) ***OAM Configuration***. This one-octet field contains OAM configuration variables and shall be as shown in Table 57–8.
g) ***OAMPDU Configuration***. This two-octet field contains OAMPDU configuration variables and shall be as shown in Table 57–9 and encoded as specified in 57.4.1 c).
h) ***OUI/CID***. This three-octet field contains the 24-bit Organizationally Unique Identifier or Company ID and shall be as shown in Table 57–10.
i) ***Vendor Specific Information***. This four-octet field contains the Vendor Specific Information field and shall be as shown in Table 57–11.

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Table 57–7—State field

Bit(s)	Name	Description
7:3	Reserved	In Local Information TLVs, reserved bits shall be set to zero when sending an OAMPDU, and should be ignored on reception for compatibility with future use of reserved bits.
2	Multiplexer Action	0 = Device is forwarding non-OAMPDUs to the lower sublayer (local_mux_action = FWD). 1 = Device is discarding non-OAMPDUs (local_mux_action = DISCARD).
1:0	Parser Action	00 = Device is forwarding non-OAMPDUs to higher sublayer (local_par_action = FWD). 01 = Device is looping back non-OAMPDUs to the lower sublayer (local_par_action = LB). 10 = Device is discarding non-OAMPDUs (local_par_action = DISCARD). 11 = Reserved. In Local Information TLVs, this value shall not be sent. If the value 11 is received, it should be ignored and not change the last received value.

Table 57–8—OAM Configuration field

Bit(s)	Name	Description
7:5	Reserved	In Local Information TLVs, reserved bits shall be set to zero when sending an OAMPDU, and should be ignored on reception for compatibility with future use of reserved bits.
4	Variable Retrieval	1 = DTE supports sending Variable Response OAMPDUs. 0 = DTE does not support sending Variable Response OAMPDUs.
3	Link Events	1 = DTE supports interpreting Link Events. 0 = DTE does not support interpreting Link Events.
2	OAM Remote Loopback Support	1 = DTE is capable of OAM remote loopback mode. 0 = DTE is not capable of OAM remote loopback mode.
1	Unidirectional Support	1 = DTE is capable of sending OAMPDUs when the receive path is non-operational. 0 = DTE is not capable of sending OAMPDUs when the receive path is non-operational.
0	OAM Mode	1 = DTE configured in Active mode. 0 = DTE configured in Passive mode.

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Table 57–9—OAMPDU Configuration field

Bit(s)	Name	Description
15:11	Reserved	In Local Information TLVs, reserved bits shall be set to zero when sending an OAMPDU, and should be ignored on reception for compatibility with future use of reserved bits.
10:0	Maximum OAMPDU Size	11-bit field which represents the largest OAMPDU, in octets, supported by the DTE. This value is compared to the remote's Maximum OAMPDU Size and the smaller of the two is used. The minimum value of this field is minFrameSize / 8. The maximum value of this field is equal to maxBasicFrameSize, which is defined in 4.4.2. Prior to exchanging Maximum OAMPDU Size and agreeing upon a maximum OAMPDU size, a DTE sends OAMPDUs of length minFrameSize / 8. The OAMPDUs transmitted by a DTE are limited by both the local DTE's Maximum OAMPDU Size and the remote DTE's Maximum OAMPDU Size as indicated in received Information OAMPDUs. A DTE is not required to change the value transmitted in this field after negotiation to an agreed size as each end will dynamically determine the correct maximum OAMPDU size to use.

Table 57–10—OUI/CID field

Bit(s)	Name	Description
23:0	OUI/CID[a]	24-bit Organizationally Unique Identifier or Company ID of the vendor.

[a]Organizations that have previously received OUIs or CIDs from the IEEE Registration Authority should use one of their allocated OUIs or CIDs consistently in this field.

Table 57–11—Vendor Specific Information field

Bit(s)	Name	Description
31:0	Vendor Specific Information	32-bit identifier that may be used to differentiate a vendor's product models/versions.

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57.5.2.2 Remote Information TLV

The Remote Information TLV shall be a copy of the last received Local Information TLV from the remote OAM peer, with the exception of the Information Type field. The encoding of this field is found in Table 57–6.

57.5.2.3 Organization Specific Information TLV

The Organization Specific Information TLV shall have the following fields:

a) ***Information Type*** = *Organization Specific Information*. This one-octet field indicates the nature of the data carried in this TLV-tuple. The encoding of this field is found in Table 57–6.
b) ***Information Length*****.** This one-octet field indicates the length (in octets) of this TLV-tuple. The length of an Organization Specific Information TLV is unspecified.
c) ***Organizationally Unique Identifier or Company ID.*** This three-octet field shall contain the 24-bit Organizationally Unique Identifier (OUI) or Company ID (CID).
d) ***Organization Specific Value*****.** This field indicates the value of the Organization Specific Information TLV. This field's length and contents are unspecified.

57.5.3 Link Event TLVs

This subclause contains the definitions for Link Event TLVs. Link Event TLVs are found in Event Notification OAMPDUs. Table 57–12 contains the defined Link Event TLVs.

Table 57–12—Link Event TLV type value

Type	Description
0x00	*End of TLV marker*
0x01	Errored Symbol Period Event
0x02	Errored Frame Event
0x03	Errored Frame Period Event
0x04	Errored Frame Seconds Summary Event
0x05–0xFD	Reserved—shall not be transmitted, should be ignored on reception by OAM client
0xFE	Organization Specific Event
0xFF	Reserved—shall not be transmitted, should be ignored on reception by OAM client

The following subclauses describe the defined Link Event TLVs.

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57.5.3.1 Errored Symbol Period Event TLV

The Errored Symbol Period Event TLV counts the number of symbol errors that occurred during the specified period. The period is specified by the number of symbols that can be received in a time interval on the underlying Physical Layer. This event is generated if the symbol error count is equal to or greater than the specified threshold for that period.

The Errored Symbol Period Event TLV shall have the following fields:

a) ***Event Type*** = *Errored Symbol Period Event*. This one-octet field indicates the nature of the information carried in this TLV-tuple. The encoding of this field is found in Table 57–12.

b) ***Event Length*****.** This one-octet field indicates the length (in octets) of this TLV-tuple. Errored Symbol Period Event uses a length value of 40 (0x28).

c) ***Event Time Stamp.*** This two-octet field indicates the time reference when the event was generated, in terms of 100 ms intervals, encoded as a 16-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.35. When received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.42.

d) ***Errored Symbol Window*****.** This eight-octet field indicates the number of symbols in the period, encoded as a 64-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.35. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.42.
   1) The default value is the number of symbols in one second for the underlying Physical Layer.
   2) The lower bound is the number of symbols in one second for the underlying Physical Layer.
   3) The upper bound is the number of symbols in one minute for the underlying Physical Layer.

e) ***Errored Symbol Threshold*****.** This eight-octet field indicates the number of errored symbols in the period is required to be equal to or greater than in order for the event to be generated, encoded as a 64-bit unsigned integer. When generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.35. When received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.42.
   1) The default value is one symbol error.
   2) The lower bound is zero symbol errors.
   3) The upper bound is unspecified.

f) ***Errored Symbols*****.** This eight-octet field indicates the number of symbol errors in the period, encoded as a 64-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.35. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.42.

g) ***Error Running Total*****.** This eight-octet field indicates the sum of symbol errors since the OAM sublayer was reset. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.35. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.42.

h) ***Event Running Total*****.** This four-octet field indicates the number of Errored Symbol Period Event TLVs that have been generated since the OAM sublayer was reset, encoded as a 32-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.35. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.42.

This event is generated at the end of the event window rather than when the threshold is crossed.

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57.5.3.2 Errored Frame Event TLV

The Errored Frame Event TLV counts the number of errored frames detected during the specified period. The period is specified by a time interval. This event is generated if the errored frame count is equal to or greater than the specified threshold for that period. Errored frames are frames that had transmission errors as detected at the Media Access Control sublayer as communicated via the reception_status parameter of the MA_DATA.indication service primitive. Refer to 4.2.9 for the definition of detectable transmission errors during reception.

The Errored Frame Event TLV shall have the following fields:

a) ***Event Type*** = *Errored Frame Event*. This one-octet field indicates the nature of the information carried in this TLV-tuple. The encoding of this field is found in Table 57–12.
b) ***Event Length*****.** This one-octet field indicates the length (in octets) of this TLV-tuple. Errored Frame Event uses a length value of 26 (0x1A).
c) ***Event Time Stamp.*** This two-octet field indicates the time reference when the event was generated, in terms of 100 ms intervals, encoded as a 16-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.37. When received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.43.
d) ***Errored Frame Window*****.** This two-octet field indicates the duration of the period in terms of 100 ms intervals, encoded as a 16-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.37. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.43.
    1) The default value is one second.
    2) The lower bound is one second.
    3) The upper bound is one minute.
e) ***Errored Frame Threshold*****.** This four-octet field indicates the number of detected errored frames in the period is required to be equal to or greater than in order for the event to be generated, encoded as a 32-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.37. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.43.
    1) The default value is one frame error.
    2) The lower bound is zero frame errors.
    3) The upper bound is unspecified.
f) ***Errored Frames*****.** This four-octet field indicates the number of detected errored frames in the period, encoded as a 32-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.37. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.43.
g) ***Error Running Total*****.** This eight-octet field indicates the sum of errored frames that have been detected since the OAM sublayer was reset. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.37. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.43.
h) ***Event Running Total*****.** This four-octet field indicates the number of Errored Frame Event TLVs that have been generated since the OAM sublayer was reset, encoded as a 32-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.37. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.43.

This event is generated at the end of the event window rather than when the threshold is crossed.

57.5.3.3 Errored Frame Period Event TLV

The Errored Frame Period Event TLV counts the number of errored frames detected during the specified period. The period is specified by a number of received frames. This event is generated if the errored frame count is greater than or equal to the specified threshold for that period (for example, if the errored frame count is greater than or equal to 10 for the last 1 000 000 frames received). Errored frames are frames that had transmission errors as detected at the Media Access Control sublayer as communicated via the reception_status parameter of the MA_DATA.indication service primitive. Refer to 4.2.9 for the definition of detectable transmission errors during reception.

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The Errored Frame Period Event TLV shall have the following fields:

a) ***Event Type*** = *Errored Frame Period Event*. This one-octet field indicates the nature of the information carried in this TLV-tuple. The encoding of this field is found in Table 57–12.
b) ***Event Length*****.** This one-octet field indicates the length (in octets) of this TLV-tuple. Errored Frame Period Event uses a length value of 28 (0x1C).
c) ***Event Time Stamp.*** This two-octet field indicates the time reference when the event was generated, in terms of 100 ms intervals, encoded as a 16-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.39. When received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.44.
d) ***Errored Frame Window*****.** This four-octet field indicates the duration of period in terms of frames, encoded as a 32-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.39. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.44.
    1) The default value is the number of minFrameSize frames that can be received in one second on the underlying Physical Layer.
    2) The lower bound is the number of minFrameSize frames that can be received in 100 ms on the underlying Physical Layer.
    3) The upper bound is the number of minFrameSize frames that can be received in one minute on the underlying Physical Layer.
e) ***Errored Frame Threshold*****.** This four-octet field indicates the number of errored frames in the period is required to be equal to or greater than in order for the event to be generated, encoded as a 32-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.39. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.44.
    1) The default value is one frame error.
    2) The lower bound is zero frame errors.
    3) The upper bound is unspecified.
f) ***Errored Frames*****.** This four-octet field indicates the number of frame errors in the period, encoded as a 32-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.39. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.44.
g) ***Error Running Total*****.** This eight-octet field indicates the sum of frame errors that have been detected since the OAM sublayer was reset. When this event is generated by the local DTE and if Clause 30 is present, this maps to 330.3.6.1.39. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.44.
h) ***Event Running Total*****.** This four-octet field indicates the number of Errored Frame Period Event TLVs that have been generated since the OAM sublayer was reset, encoded as a 32-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.39. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.44.

This event is generated at the end of the event window rather than when the threshold is crossed.

57.5.3.4 Errored Frame Seconds Summary Event TLV

The Errored Frame Seconds Summary Event TLV counts the number of errored frame seconds that occurred during the specified period. The period is specified by a time interval. This event is generated if the number of errored frame seconds is equal to or greater than the specified threshold for that period. An errored frame second is a one second interval wherein at least one frame error was detected. Errored frames are frames that had transmission errors as detected at the Media Access Control sublayer and communicated via the reception_status parameter of the MA_DATA.indication service primitive. Refer to 4.2.9 for the definition of detectable transmission errors during reception.

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The Errored Frame Seconds Summary Event TLV shall have the following fields:

a) ***Event Type*** = *Errored Frame Seconds Summary Event*. This one-octet field indicates the nature of the information carried in this TLV-tuple. The encoding of this field is found in Table 57–12.
b) ***Event Length*****.** This one-octet field indicates the length (in octets) of this TLV-tuple. Errored Frame Seconds Summary Event uses a length value of 18 (0x12).
c) ***Event Time Stamp.*** This two-octet field indicates the time reference when the event was generated, in terms of 100 ms intervals, encoded as a 16-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.41. When received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.45.
d) ***Errored Frame Seconds Summary Window*****.** This two-octet field indicates the duration of the period in terms of 100 ms intervals, encoded as a 16-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.41. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.45.
    1) The default value is 60 seconds.
    2) The lower bound is 10 seconds.
    3) The upper bound is 900 seconds.
e) ***Errored Frame Seconds Summary Threshold*****.** This two-octet field indicates the number of errored frame seconds in the period is required to be equal to or greater than in order for the event to be generated, encoded as a 16-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.41. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.45.
    1) The default value is one errored second.
    2) The lower bound is zero errored seconds.
    3) The upper bound is unspecified.
f) ***Errored Frame Seconds Summary*****.** This two-octet field indicates the number of errored frame seconds in the period, encoded as a 16-bit unsigned integer. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.41. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.45.
g) ***Error Running Total*****.** This four-octet field indicates the sum of errored frame seconds that have been detected since the OAM sublayer was reset. When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.41. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.45.
h) ***Event Running Total*****.** This four-octet field indicates the number of Errored Frame Seconds Summary Event TLVs that have been generated since the OAM sublayer was reset, encoded as a 32-bit unsigned integer.When this event is generated by the local DTE and if Clause 30 is present, this maps to 30.3.6.1.41. When this event is received from the remote DTE and if Clause 30 is present, this maps to 30.3.6.1.45.

This event is generated at the end of the event window rather than when the threshold is crossed.

57.5.3.5 Organization Specific Event TLVs

The optional Organization Specific Event TLV may be used by organizations to define extensions to the Event mechanisms in this clause. Organization Specific Event TLVs shall have the following fields:

a) ***Event Type*** = *Organization Specific Event*. This one-octet field indicates the nature of the information carried in this TLV-tuple. The encoding of this field is found in Table 57–12.
b) ***Event Length*****.** This one-octet field indicates the length (in octets) of this TLV-tuple. The length of the Organization Specific Event is unspecified.
c) ***Organizationally Unique Identifier.*** This three-octet field shall contain a 24-bit Organizationally Unique Identifier.
d) ***Organization Specific Value*****.** This field indicates the value of the Organization Specific Event. This field's length and contents are unspecified.

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57.6 Variables

MIB variables are queried through the use of Variable Request OAMPDUs and returned through the use of Variable Response OAMPDUs. Variable Request OAMPDUs, defined in 57.4.3.3, use data structures called Variable Descriptors (see 57.6.1). An OAM client may request one or more variables in each Variable Request OAMPDU.

Variable Response OAMPDUs, defined in 57.4.3.4, use data structures called Variable Containers (see 57.6.2). Each returned Variable Container resides within a single Variable Response OAMPDU. If a Variable Container does not fit within a Variable Response OAMPDU, an error code is returned. In returning requested variables, an OAM client generates at least one and perhaps additional Variable Response OAMPDUs per received Variable Request OAMPDU. The following subclauses describe the format of Variable Descriptors and Variable Containers.

See 57.6.3 for a description of the parsing rules for Variable Descriptors and Variable Containers.

57.6.1 Variable Descriptors

A Variable Descriptor is used to request MIB attributes, objects and packages and uses the encodings found in Annex B of IEEE Std 802.3.1. The Variable Descriptor structure shall be as shown in Table 57–13.

Table 57–13—Variable Descriptor format

Octet(s)	Name	Description
1	Variable Branch	As defined in Annex B of IEEE Std 802.3.1, Variable Branches may reference attributes, objects or packages. If an object or package is referenced, only the attributes within the object or package shall be found within the Variable Container. Actions shall not be found within Variable Containers.
2	Variable Leaf	The Variable Leaf field is derived from the encodings found in Annex B of IEEE Std 802.3.1.

57.6.2 Variable Containers

Variable Containers are used to return MIB attributes, objects and packages. One or more Variable Containers may exist in the Data field of a Variable Response OAMPDU (see 57.4.3.4).

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57.6.2.1 Format of Variable Containers when returning attributes

The Variable Container structure for an attribute shall be as shown in Table 57–14.

Table 57–14—Variable Container format when returning an attribute

Octet(s)	Name	Description
1	Variable Branch	Derived from the encodings found in Annex B of IEEE Std 802.3.1, Variable Branches may reference attributes, objects or packages. If an object or package is referenced, only the attributes within the object or package shall be found within the Variable Container. Actions shall not be found within Variable Containers.
2	Variable Leaf	The Variable Leaf field is derived from the encodings found in Annex B of IEEE Std 802.3.1.
1	Variable Width	When bit 7 = 1, bits 6:0 represent a Variable Indication. Refer to Table 57–17 for the encoding of bits 6:0. There is no Variable Value field when bit 7 = 1. When bit 7 = 0, bits 6:0 represent the length of the Variable Value field in octets. An encoding of 0x00 equals 128 octets. All other encodings represent actual lengths.
varies	Variable Value	The Variable Value field may be 1 to 128 octets in length. Its width is determined by the Variable Width field.

The first field is the one-octet Variable Branch field. The second field is the two-octet Variable Leaf field. See Table 57–16 for examples of Variable Branch and Variable Leaves. The third field is the dual purpose one-octet Variable Width field. This field either contains the actual width of the attribute or a Variable Indication providing information as to the reason this particular attribute could not be returned. See Table 57–17 for the defined Variable Indications. If the Variable Width field contains a width value, the fourth field is the Variable Value field, which contains the attribute. This field may be up to 128 octets in length. Octets of the attribute are ordered most significant first, followed by each successive octet. If the Variable Width field contains a Variable Indication, the Variable Value field does not exist.

Additionally, a special Variable Container with Variable Branch and Leaf values corresponding to an object identification number (such as 7/330 for a PME ID, or 7/282 for an EPON LLID), Variable Width equal to 2, and Variable Value equal to a 2-octet identification number, may be used in a Variable Request OAMPDU to select a particular instance of a managed object of which multiple instances exist in the remote MIB.

The Variable Value identifies which instance is being addressed. Subsequent Variable Descriptors shall be understood to target the attributes of the selected instance until an other instance selector is received or the Variable Request OAMPDU ends. Each instance selector shall be acknowledged with a Variable Container indicating the same Branch/Leaf and the identifier that was selected, preceding the concerned variables. If no explicit instance selection has taken place, all instances of the concerned object are addressed. In this case, each subsequent Variable Descriptor shall be understood to consecutively target the attributes of all existing instances until an instance selector is received or the Variable Request OAMPDU ends.

The Variable Containers returned by the far-end OAM client may be transmitted in one or more OAMPDUs, respecting the OAMPDU size limitations.

NOTE—In the case of PME Aggregation, each PME is identified by a bit position in a 32-bit string during the Handshake process. This position should be transformed into a number between 0 and 31 before transmission in the Variable Value field.

57.6.2.2 Format of Variable Containers when returning packages and objects

The Variable Container structure for packages and objects shall be as shown in Table 57–15.

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Table 57–15—Variable Container format when returning packages and objects

Octet(s)	Name	Description
1	Variable Branch	Derived from the encodings found in Annex B of IEEE Std 802.3.1, Variable Branches may reference attributes, objects or packages. If an object or package is referenced, only the attributes within the object or package shall be found within the Variable Container. Actions shall not be found within Variable Containers.
2	Variable Leaf	The Variable Leaf field is derived from the encodings found in Annex B of IEEE Std 802.3.1.
1	Variable Width	When bit 7 = 1, bits 6:0 represent a Variable Indication. Refer to Table 57–17 for the encoding of bits 6:0. There is no Variable Value field when bit 7 = 1. When bit 7 = 0, bits 6:0 represent the length of the Variable Value field in octets. An encoding of 0x00 equals 128 octets. All other encodings represent actual lengths.
varies	Variable Value	The Variable Value field may be 1 to 128 octets in length. Its width is determined by the Variable Width field.

A package is defined as a set of MIB attributes and/or actions. An object is a set of packages, which in turn are made up of MIB attributes and/or actions. Variable Containers provide an efficient method for returning packages and objects. Objects are returned in the order they are listed in Annex B of IEEE Std 802.3.1.

The Variable Container structure for packages and objects is similar to the structure for attributes. The first field is the one-octet Variable Branch field for the specific package or object being returned. The second field is the two-octet Variable Leaf field for the specific package or object being returned. See Table 57–16 for examples of Variable Branch and Variable Leaves. The third field is the dual purpose one-octet Variable Width field of the first attribute within the package or object being returned. This field either contains the actual width of the attribute or a Variable Indication providing information as to the reason this particular attribute could not be returned. See Table 57–17 for the defined Variable Indications. If the Variable Width field contains a width value, the fourth field is the Variable Value field, which contains the first attribute of the package or object being returned. This field may be up to 128 octets in length. Octets of the attribute are ordered most significant first, followed by each successive octet. If the Variable Width field contains a Variable Indication, the Variable Value field does not exist.

For each successive attribute within the package, the third field (Variable Width) and fourth field (Variable Value), if applicable, are repeated.

For each successive attribute within each successive package of the object, the third field (Variable Width) and fourth field (Variable Value), if applicable, are repeated.

57.6.3 Parsing

The OAM client parses Variable Descriptors and Variable Containers. All Variable Descriptors/Containers contain a one-octet Variable Branch field and a two-octet Variable Leaf field. Variable Descriptor/Container processing should follow these recommendations:

a) Detection of a Variable Branch field equal to 0x00 should indicate there are no more Variable Descriptors/Containers to process (subsequent fields can be ignored).
b) Variable Branch or Variable Leaf fields with unknown or unexpected values should be ignored.
c) If a Variable Width field indicates Variable Container extends beyond the frame (e.g., the length cannot fit into the frame given its length and starting point), then the Variable Container should be ignored.

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d) Detection of a Variable Indication value equal to 0x40 should indicate there are no more attributes within the object to process.
e) Detection of a Variable Indication value equal to 0x60 should indicate there are no more objects within the package to process.
f) Detection of a Variable Container in a Variable Request OAMPDU indicates that subsequent Variable Descriptors shall be applied to the instance of the managed object corresponding to the identification number expressed in the Variable Value field of the Variable Container. In the corresponding Variable Response OAMPDU, a Variable Container indicating the selected instance shall immediately precede the Variable Containers pertaining to objects of which a particular instance was selected.

57.6.4 Variable Branch/Leaf examples

Table 57–16 contains a set of example branch and leaf values for attributes, packages and objects.

Table 57–16—Variable Branch/Leaf examples

Variable Type	Variable Name	Variable	
		Branch	Leaf
attribute	aFramesTransmittedOK	0x07	0x0002
attribute	aFramesReceivedOK	0x07	0x0005
package	pMandatory	0x04	0x0001
package	pRecommended	0x04	0x0002
object	oMACEntity	0x03	0x0001
object	oPHYEntity	0x03	0x0002

57.6.5 Variable Indications

If a DTE is unable to retrieve one or more variables, the Variable Container is used to return the appropriate Variable Indication for the particular variable(s). The Variable Indications are defined in Table 57–17.

Table 57–17—Variable indications

Coding	Indication
0x00	Reserved - shall not be transmitted, should be ignored on reception by OAM client.
0x01	Length of requested Variable Container(s) exceeded OAMPDU data field.
0x02 to 0x1F	Reserved—shall not be transmitted, should be ignored on reception by OAM client.
Attribute Indications	
0x20	Requested attribute was unable to be returned due to an undetermined error.
0x21	Requested attribute was unable to be returned because it is not supported by the local DTE.
0x22	Requested attribute may have been corrupted due to reset.
0x23	Requested attribute unable to be returned due to a hardware failure.
0x24	Requested attribute experienced an overflow error.
0x25 to 0x3F	Reserved—shall not be transmitted, should be ignored on reception by OAM client.
Object Indications	
0x40	End of object indication.

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Table 57–17—Variable indications *(continued)*

Coding	Indication
0x41	Requested object was unable to be returned due to an undetermined error.
0x42	Requested object was unable to be returned because it is not supported by the local DTE.
0x43	Requested object may have been corrupted due to reset.
0x44	Requested object unable to be returned due to a hardware failure.
0x45 to 0x5F	Reserved—shall not be transmitted, should be ignored on reception by OAM client.
Package Indications	
0x60	End of package indication.
0x61	Requested package was unable to be returned due to an undetermined error.
0x62	Requested package was unable to be returned because it is not supported by the local DTE.
0x63	Requested package may have been corrupted due to reset.
0x64	Requested package unable to be returned due to a hardware failure.
0x65 to 0x7F	Reserved—shall not be transmitted, should be ignored on reception by OAM client.

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57.7 Protocol implementation conformance statement (PICS) proforma for Clause 57, Operations, Administration, and Maintenance (OAM)[111]

57.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 57, Operations, Administration, and Maintenance (OAM), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

57.7.2 Identification

57.7.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

57.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 57, Operations, Administration, and Maintenance (OAM)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[111] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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57.7.2.3 Major capabilities/options

Item	Feature	Subclause/ Table	Value/Comment	Status	Support
OM	OAM object class	30.3.6		O	Yes [ ] No [ ]
CSI	OAM client service interfaces	57.2.5		M	Yes [ ]
ISI	Internal service interfaces	57.2.8		M	Yes [ ]
*ACTV	Active mode	57.2.9		O.1	Yes [ ] No [ ]
*PASS	Passive mode	57.2.9		O.1	Yes [ ] No [ ]
*LB	OAM remote loopback	57.2.11, Table 57–8		O	Yes [ ] No [ ]
UNI	Unidirectional operation	57.2.12, Table 57–8	Requires support for unidirectional operation as defined in Clause 66.	O	Yes [ ] No [ ]
*EVNT	Link Events	57.4.3.2, 57.5.3		O	Yes [ ] No [ ]
*VAR	Variable Retrieval	57.4.3.3, 57.4.3.4		O	Yes [ ] No [ ]
*OSP	Organization Specific OAMPDU	57.4.3.6		O	Yes [ ] No [ ]
*OSE	Organization Specific Events	57.5.3.5		O	Yes [ ] No [ ]
OSI	Organization Specific Information TLV	57.5.2.3		O	Yes [ ] No [ ]

57.7.3 PICS proforma tables for Operation, Administration, and Maintenance (OAM)

57.7.3.1 Functional specifications

Item	Feature	Subclause/ Table	Value/Comment	Status	Support
OFS1	Passive mode limited transmission	57.2.9.2	Cannot send Variable Request or Loopback Control OAMPDUs	PASS:M	Yes [ ] No [ ] N/A [ ]
OFS2	Discovery state diagram	57.3.2.1	Implemented as defined in Figure 57–5	M	Yes [ ]
OFS3	Transmit state diagram	57.3.2.2	Implemented as defined in Figure 57–6	M	Yes [ ]
OFS4	OAMPDU transmission when local_pdu is set to LF_INFO	57.3.2.2.6	Only Information OAMPDUs with Link Fault bit of Flags field and without Information TLVs can be transmitted	M	Yes [ ]
OFS5	OAMPDU transmission when local_pdu is set to RX_INFO	57.3.2.2.6	No OAMPDU transmission allowed	M	Yes [ ]
OFS6	OAMPDU transmission when local_pdu is set to INFO	57.3.2.2.6	Only Information OAMPDUs can be transmitted	M	Yes [ ]

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Item	Feature	Subclause/ Table	Value/Comment	Status	Support
OFS7	OAMPDU transmission when local_pdu is set to ANY: OAM_CTL.request service primitive with one or more critical link event parameters	57.3.2.2.6	Requests transmission of Information OAMPDU with appropriate bits of Flags field set	M	Yes [ ]
OFS8	OAMPDU.request service primitive	57.3.2.2.6	Requests transmission of OAMPDU	M	Yes [ ]
OFS9	OAMPDU Flags field reserved encodings Remote Stable and Remote Evaluating bits	Table 57–3	Encoding of 0x3 is not transmitted	M	Yes [ ]
OFS10	Local Stable and Local Evaluating bits	Table 57–3	Encoding of 0x3 is not transmitted	M	Yes [ ]
OFS11	Reserved bits	Table 57–3	Reserved bits are zero on transmission	M	Yes [ ]
OFS12	OAMPDU Code field	57.4.2.2	Only defined Code field values are permitted in transmitted OAMPDUs	M	Yes [ ]
OFS13	OAMPDU reception when local_pdu is not set to ANY	57.3.2.3	Only Information OAMPDUs are sent to OAM client entity	M	Yes [ ]
OFS14	OAMPDU reception when local_pdu is set to ANY	57.3.2.3	All OAMPDUs are sent to OAM client entity	M	Yes [ ]
OFS15	Multiplexer state diagram	57.3.3	Implemented as defined in Figure 57–7	M	Yes [ ]
OFS16	Multiplexer transparent pass-through	57.3.3.2	Provide transparent pass-through of frames from superior sublayer to subordinate sublayer	M	Yes [ ]
OFS17	Effect of OAMPDU on a frame already submitted to subordinate sublayer	57.3.3.2	Has no effect	M	Yes [ ]
OFS18	Parser state diagram	57.3.4	Implemented as defined in Figure 57–8	M	Yes [ ]

57.7.3.2 Event Notification Generation and Reception

Item	Feature	Subclause/ Table	Value/Comment	Status	Support
EV1	Response to Critical Events	57.2.10.3	Set/clear Flag bits based on OAM_CTL.request service primitive	M	Yes [ ]
EV2	Critical Event reception	57.2.10.4	Indicated via Flags field of OAMPDU.indication service primitive	M	Yes [ ]
EV3	Link Event reception	57.2.10.4	Indicated via OAMPDU.indication service primitive with all received Event Notification OAMPDUs	EVNT:M	Yes [ ] N/A [ ]

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57.7.3.3 OAMPDUs

Item	Feature	Subclause/ Table	Value/Comment	Status	Support
PDU2	OAMPDU structure	57.4.2	As defined in Figure 57–9 and field definitions	M	Yes [ ]
PDU3	Minimum OAMPDU size	57.4.2	Support OAMPDUs minFrame-Size in length	M	Yes [ ]
PDU4	Information OAMPDU frame structure	57.4.3.1	Shown in Figure 57–10	M	Yes [ ]
PDU5	Information OAMPDU when local_pdu set to LF_INFO	57.4.3.1	Data field contains zero Information TLVs	M	Yes [ ]
	Information OAMPDU when local _pdu not set to LF_INFO				
PDU6	remote_state_valid=FALSE	57.4.3.1	Data field contains Local Information TLV	M	Yes [ ]
PDU7	remote_state_valid=TRUE	57.4.3.1	Data field contains Local and Remote Information TLVs	M	Yes [ ]
PDU8	Type values 0x03-0xFD	Table 57–6	Not to be sent	M	Yes [ ]
PDU9	Type value 0xFF	Table 57–6	Not to be sent	M	Yes [ ]
PDU10	Event Notification OAMPDU frame structure	57.4.3.2	Shown in Figure 57–11	EVNT:M	Yes [ ] N/A [ ]
PDU11	Event Notification OAMPDU Sequence Number	57.4.3.2	The first two bytes of the Data field contain a Sequence Number encoded as an unsigned 16-bit integer	EVNT:M	Yes [ ] N/A [ ]
PDU12	Event Notification OAMPDU Event(s)	57.4.3.2	Data field containing one or more Link Event TLVs following the Sequence Number	EVNT:M	Yes [ ] N/A [ ]
PDU13	Variable Request OAMPDU frame structure	57.4.3.3	Shown in Figure 57–12	VAR * ACTV:M	Yes [ ] No [ ] N/A [ ]
PDU14	Variable Request OAMPDU Data field	57.4.3.3	Data field contains one or more Variable Descriptors	VAR * ACTV:M	Yes [ ] N/A [ ]
PDU15	Variable Response OAMPDU frame structure	57.4.3.4	Shown in Figure 57–13	VAR:M	Yes [ ] N/A [ ]
PDU16	Variable Response OAMPDU Data field	57.4.3.4	Data field contains one or more Variable Containers	VAR:M	Yes [ ] N/A [ ]
PDU17	Loopback Control OAMPDU frame structure	57.4.3.5	Shown in Figure 57–14	!PASS * LB:M	Yes [ ] N/A [ ]
PDU18	Loopback Control OAMPDU Data field	57.4.3.5	Data field contains a single OAM Remote Loopback command from Table 57–5	!PASS * LB:M	Yes [ ] N/A [ ]
PDU19	Command value 0x00	Table 57–5	Not to be sent	!PASS * LB:M	Yes [ ] N/A [ ]
PDU20	Command values 0x03–0xFF	Table 57–5	Not to be sent	!PASS * LB:M	Yes [ ] N/A [ ]
PDU21	Organization Specific OAMPDU frame structure	57.4.3.6	Shown in Figure 57–15	OSP:M	Yes [ ] N/A [ ]
PDU22	Organization Specific OAMPDU Organizationally Unique Identifier field	57.4.3.6	Contains 24-bit Organizationally Unique Identifier	OSP:M	Yes [ ] N/A [ ]

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57.7.3.4 Local Information TLVs

Item	Feature	Subclause/ Table	Value/Comment	Status	Support
LIT1	Local Information TLV	57.5.2.1	Contains the following fields: Information Type, Information Length, OAM Version, Revision, State, OAM Configuration, OAMPDU Configuration, OUI/CID, Vendor Specific Information	M	Yes [ ]
LIT2	Local Information TLV OAM Version field	57.5.2.1	Contains 0x01 to claim compliance to this specification	M	Yes [ ]
LIT3	Local Information TLV Revision Field	57.5.2.1	Starts at zero and incremented each time a Local Information TLV field changes	M	Yes [ ]
LIT4	Local Information TLV State field	57.5.2.1	As defined in Table 57–7	M	Yes [ ]
LIT5	Local Information TLV State field Parser Action 0x3 value	57.5.2.1	Is not transmitted	M	Yes [ ]
LIT6	Reserved bits	Table 57–7	Reserved bits are zero on transmission	M	Yes [ ]
LIT7	Local Information TLV OAM Configuration field	57.5.2.1	As defined in Table 57–8	M	Yes [ ]
LIT8	Reserved bits	Table 57–8	Reserved bits are zero on transmission	M	Yes [ ]
LIT9	Local Information TLV OAMPDU Configuration field	57.5.2.1	As defined in Table 57–9	M	Yes [ ]
LIT10	Local Information TLV OUI/ CID field	57.5.2.1	As defined in Table 57–10	M	Yes [ ]
LIT11	Reserved bits	Table 57–9	Reserved bits are zero on transmission	M	Yes [ ]
LIT12	Local Information TLV Vendor Specific Information field	57.5.2.1	As defined in Table 57–11	M	Yes [ ]

57.7.3.5 Remote Information TLVs

Item	Feature	Subclause	Value/Comment	Status	Support
RIT1	Remote Information TLV	57.5.2.2	Contains the Information Type field specifying the Remote Information TLV Type value and all remaining fields are copied from the last received Local Information TLV from remote OAM peer	M	Yes [ ]

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57.7.3.6 Organization Specific Information TLVs

Item	Feature	Subclause	Value/Comment	Status	Support
OIT1	Organization Specific Information TLV	57.5.2.3	Contains the following fields: Information Type, Information Length, OUI/CID, Organization Specific Value	M	Yes [ ]
OIT2	Organization Specific Information TLV OUI field	57.5.2.3	Contains 24-bit OUI/CID	M	Yes [ ]

57.7.4 Link Event TLVs

Item	Feature	Subclause/ Table	Value/Comment	Status	Support
ET1	Errored Symbol Period Event TLV structure	57.5.3.1	Contains the following fields: Event Type, Event Length, Event Time Stamp, Errored Symbol Window, Errored Symbol Threshold, Errored Symbols, Error Running Total, Event Running Total	EVNT:M	Yes [ ] N/A [ ]
ET2	Errored Frame Event TLV structure	57.5.3.2	Contains the following fields: Event Type, Event Length, Event Time Stamp, Errored Frame Window, Errored Frame Threshold, Errored Frames, Error Running Total, Event Running Total	EVNT:M	Yes [ ] N/A [ ]
ET3	Errored Frame Period Event TLV structure	57.5.3.3	Contains the following fields: Event Type, Event Length, Event Time Stamp, Errored Frame Window, Errored Frame Threshold, Errored Frames, Error Running Total, Event Running Total	EVNT:M	Yes [ ] N/A [ ]
ET4	Errored Frame Seconds Summary Event TLV structure	57.5.3.4	Contains the following fields: Event Type, Event Length, Event Time Stamp, Errored Frame Seconds Summary Window, Errored Frame Seconds Summary Threshold, Errored Frame Seconds Summary, Error Running Total, Event Running Total	EVNT:M	Yes [ ] N/A [ ]
ET5	Organization Specific Event TLV structure	57.5.3.5	Contains the following fields: Event Type, Event Length, Organizationally Unique Identifier, Organization Specific Value	EVNT * OSE:M	Yes [ ] N/A [ ]
ET6	Organization Specific Event Organizationally Unique Identifier field	57.5.3.5	Contains 24-bit Organizationally Unique Identifier	EVNT * OSE:M	Yes [ ] N/A [ ]
ET7	Type values 0x05 to 0xFD	Table 57–12	Not to be sent	EVNT:M	Yes [ ] N/A [ ]
ET8	Type value 0xFF	Table 57–12	Not to be sent	EVNT:M	Yes [ ] N/A [ ]

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57.7.5 Variables Descriptors and Containers

Item	Feature	Subclause/ Table	Value/Comment	Status	Support
VAR1	Variable Descriptor structure	57.6.1	As defined in Table 57–13	VAR * ACTV:M	Yes [ ] N/A [ ]
	Variable Descriptor / Variable Branch				
VAR2	references attributes	57.6.1	If an object or package is referenced, only attributes can be found within Variable Container	VAR * ACTV:M	Yes [ ] N/A [ ]
VAR3	does not reference actions	57.6.1	Actions are not found in Variable Containers	VAR * ACTV:M	Yes [ ] N/A [ ]
VAR4	Variable Container structure for an attribute	57.6.2	As defined in Table 57–14	VAR:M	Yes [ ] N/A [ ]
	Variable Container / Variable Branch				
VAR5	references attributes	57.6.2	If an object or package is referenced, only attributes can be found within Variable Container	VAR:M	Yes [ ] N/A [ ]
VAR6	does not reference actions	57.6.2	Actions are not found in Variable Containers	VAR:M	Yes [ ] N/A [ ]
VAR7	Type value 0x00	Table 57–16	Not to be sent	VAR:M	Yes [ ] N/A [ ]
VAR8	Type values 0x02 to 0x1F	Table 57–16	Not to be sent	VAR:M	Yes [ ] N/A [ ]
VAR9	Type values 0x25 to 0x2F	Table 57–16	Not to be sent	VAR:M	Yes [ ] N/A [ ]
VAR10	Type values 0x45 to 0x5F	Table 57–16	Not to be sent	VAR:M	Yes [ ] N/A [ ]
VAR11	Type values 0x65 to 0x7F	Table 57–16	Not to be sent	VAR:M	Yes [ ] N/A [ ]

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58. Physical Medium Dependent (PMD) sublayer and medium, type 100BASE-LX10 (Long Wavelength) and 100BASE-BX10 (Bi-Directional Long Wavelength)

58.1 Overview

The 100BASE-LX10 and 100BASE-BX10 PMD sublayers provide point-to-point 100 Mb/s Ethernet links over a pair of single-mode fibers or an individual single-mode fiber, respectively, up to at least 10 km. They complement 100BASE-TX (twisted-pair cable, see Clause 25) and 100BASE-FX (multimode fiber, see Clause 26).

This clause specifies the 100BASE-LX10 PMD and the 100BASE-BX10 PMDs for operation over single-mode fiber. A PMD is connected to the 100BASE-X PMA of 66.1, and to the medium through the MDI. A PMD is optionally combined with the management functions that may be accessible through the management interface defined in Clause 22 or by other means.

Table 58–1 shows the primary attributes of each PMD type.

Table 58–1—Classification of 100BASE-LX10 and 100BASE-BX10

Description	100BASE-LX10	100BASE-BX10-D	100BASE-BX10-U	Unit
Fiber type	B1.1, B1.3 SMF[a]			
Number of fibers	2	1		
Typical transmit direction	Any	Downstream	Upstream	
Nominal transmit wavelength	1310	1550	1310	nm
Minimum range	0.5 m to 10 km			
Maximum channel insertion loss[b]	6.0	5.5	6.0	dB

[a]Specified in IEC 60793-2.
[b]At the nominal wavelength.

A 100BASE-LX10 link uses 100BASE-LX10 PMDs at each end while a 100BASE-BX10 link uses a 100BASE-BX10-D PMD at one end and a 100BASE-BX10-U PMD at the other. Typically, the 1550 nm band is used to transmit away from the center of the network (“downstream”) and the 1310 nm band towards the center (“upstream”), although this arrangement, or the notion of hierarchy, is not required. The suffixes “D” and “U” indicate the PMDs at each end of a link which transmit in these directions and receive in the opposite directions.

Two optional temperature ranges are defined; see 58.8.4 for further details. Implementations may be declared as compliant over one or both complete ranges, or not so declared (compliant over parts of these ranges or another temperature range).

58.1.1 Goals and objectives

The following are the objectives of 100BASE-LX10 and 100BASE-BX10:

a) Point-to-point on optical fiber
b) 100BASE-X up to at least 10 km over single-mode fiber (SMF)
c) BER better than or equal to 10^{-12} at the PHY service interface

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58.1.2 Positioning of this PMD set within the IEEE 802.3 architecture

Figure 58–1 depicts the relationships of the PMD (shown shaded) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

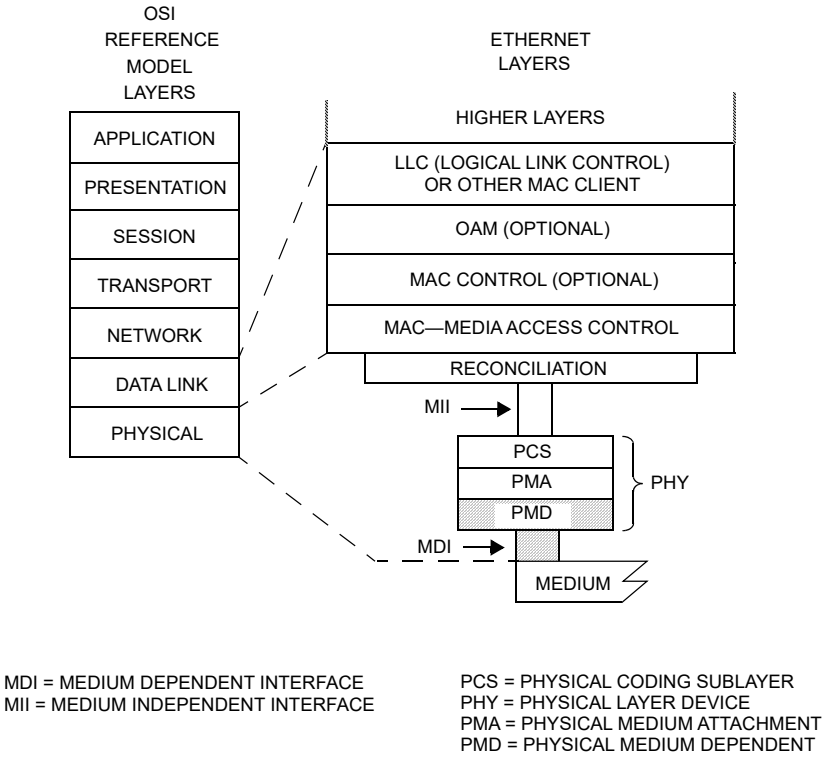

Figure 58–1—100BASE-LX10 and 100BASE-BX10 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

58.1.3 Terminology and conventions

The following list contains references to terminology and conventions used in this clause:

Basic terminology and conventions, see 1.1 and 1.2.

Normative references, see 1.3.

Definitions, see 1.4.

Abbreviations, see 1.5.

Informative references shown referenced in the format [Bn], see Annex A.

Introduction to 100 Mb/s baseband networks, see Clause 21.

Introduction to Ethernet for subscriber access networks, see Clause 56

58.1.4 Physical Medium Dependent (PMD) sublayer service interface

The following specifies the services provided by the 100BASE-LX10 and 100BASE-BX10 PMDs. These PMD sublayer service interfaces are described in an abstract manner and do not imply any particular implementation.

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The PMD service interface supports the exchange of NRZI encoded 4B/5B bit streams between the PMA and PMD entities. The PMD translates the serialized data of the PMA to and from signals suitable for the specified medium.

The following primitives are defined:

PMD_UNITDATA.request

PMD_UNITDATA.indication

PMD_SIGNAL.indication

58.1.4.1 Delay constraints

Delay requirements which affect the PMD layer are specified in 24.6. Of the budget, up to 12 ns is allocated for each of the transmit and receive functions of the PMD to account for those cases where the PMD includes a pigtail.

58.1.4.2 PMD_UNITDATA.request

This primitive defines the transfer of a serial data stream from the PMA to the PMD.

The semantics of the service primitive are PMD_UNITDATA.request(tx_bit). The data conveyed by PMD_UNITDATA.request is a continuous stream of bits where the tx_bit parameter can take one of two values: ONE or ZERO. The PMA continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal 125 MBd signaling speed. Upon receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals at the MDI.

58.1.4.3 PMD_UNITDATA.indication

This primitive defines the transfer of data from the PMD to the PMA.

The semantics of the service primitive are PMD_UNITDATA.indication(rx_bit). The data conveyed by PMD_UNITDATA.indication is a continuous stream of bits where the rx_bit parameter can take one of two values: ONE or ZERO. The PMD continuously sends a stream of bits to the PMA corresponding to the signals received from the MDI.

58.1.4.4 PMD_SIGNAL.indication

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

The semantics of the service primitive are PMD_SIGNAL.indication(SIGNAL_DETECT). The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting light at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication(rx_bit) is undefined. The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT.

NOTE—SIGNAL_DETECT = OK does not guarantee that PMD_UNITDATA.indication(rx_bit) is known good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the specified bit error ratio.

58.2 PMD functional specifications

The 100BASE-X PMDs perform the transmit and receive functions that convey data between the PMD service interface and the MDI.

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58.2.1 PMD block diagram

The PMD sublayer is defined at the four reference points shown in Figure 58–2. Two points, TP2 and TP3, are compliance points. TP1 and TP4 are reference points for use by implementers. The optical transmit signal is defined at the output end of a patch cord (TP2), between 2 and 5 m in length, of single-mode fiber. Unless specified otherwise, all transmitter measurements and tests defined in 58.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) connected to the receiver. Unless specified otherwise, all receiver measurements and tests defined in 58.7 are made at TP3.

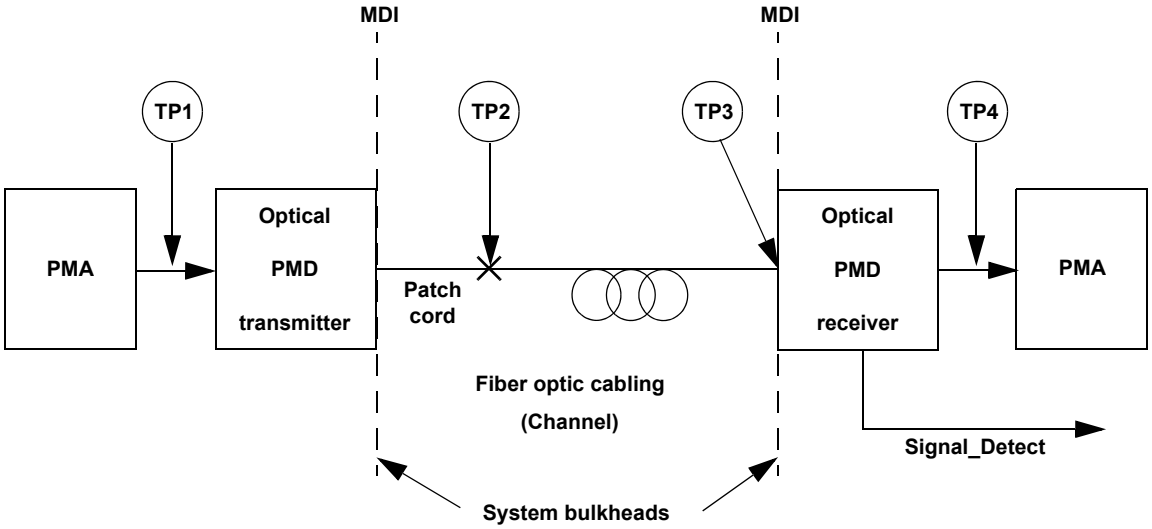

Figure 58–2—100BASE-X block diagram

The electrical specifications of the PMD service interface (TP1 and TP4) are not system compliance points (these are not readily testable in a system implementation). It is expected that in many implementations, TP1 and TP4 will be common between 100BASE-LX10, 100BASE-BX10-D, 100BASE-BX10-U, and 100BASE-FX (multimode fiber, see Clause 26).

58.2.2 PMD transmit function

The PMD transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the optical specifications in this clause. The higher optical power level should correspond to tx_bit = ONE.

NOTE—Because the NRZI coding distinguishes between a transition and no transition on the line, as opposed to 0 and 1, an inverted signal is usable.

58.2.3 PMD receive function

The PMD receive function shall convey the bits received from the MDI according to the optical specifications in this clause to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). The higher optical power level should correspond to rx_bit = ONE.

NOTE—Because the NRZI coding distinguishes between a transition and no transition on the line, as opposed to 0 and 1, an inverted signal is usable.

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58.2.4 100BASE-LX10 and 100BASE-BX10 signal detect function

The PMD signal detect function shall report to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indication is intended to be an indicator of optical signal presence.

The value of the SIGNAL_DETECT parameter for 100BASE-LX10 and 100BASE-BX10 shall be generated according to the conditions defined in Table 58–2. The PMD receiver is not required to verify whether a compliant 100BASE-LX10 signal or 100BASE-BX10 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 58–2—100BASE-LX10 and 100BASE-BX10 SIGNAL_DETECT value definition

Receive conditions		SIGNAL_DETECT value
100BASE-LX10	**100BASE-BX10**	
Average input optical power ≤ Signal detect threshold (min) in Table 58–4	Average input optical power ≤ Signal detect threshold (min) in Table 58–6	FAIL
Average input optical power ≥ Receiver sensitivity (max) in Table 58–4 with a compliant 100BASE-LX10 signal input	Average input optical power ≥ Receiver sensitivity (max) in Table 58–6 with a compliant 100BASE-BX10 signal input at the specified receiver wavelength	OK
All other conditions		Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD due to cross talk, power supply noise, etc.

Various implementations of the signal detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

58.3 PMD to MDI optical specifications for 100BASE-LX10

The operating range for 100BASE-LX10 is defined in Table 58–1. A 100BASE-LX10 compliant transceiver operates over the media types listed in Table 58–1 according to the specifications described in 58.9. A transceiver which exceeds the operational range requirement while meeting all other optical specifications is considered compliant.

NOTE—In this subclause and 58.4, the specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is explained in 58.7.6.

58.3.1 Transmitter optical specifications

The 100BASE-LX10 transmitter's signaling speed, operating wavelength, spectral width, average launch power, extinction ratio, return loss tolerance, OMA, eye and TDP shall meet the specifications defined in Table 58–3 per measurement techniques described in 58.7. Its $RIN_{12}OMA$ should meet the value listed in Table 58–3 per measurement techniques described in 58.7.7.

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Table 58–3—100BASE-LX10 transmit characteristics

Description	Type B1.1, B1.3 SMF	Unit
Transmitter type[a]	Longwave laser	
Signaling speed (range)	125 ± 50 ppm	MBd
Operating wavelength range[b]	1260 to 1360	nm
RMS spectral width (max)	7.7	nm
Average launch power (max)	–8	dBm
Average launch power (min)	–15	dBm
Average launch power of OFF transmitter (max)	–45	dBm
Extinction ratio (min)	5	dB
$RIN_{12}OMA$[c] (max)	–110	dB/Hz
Optical return loss tolerance (max)	12	dB
Launch OMA (min)	–14.8 (33.1)	dBm (μW)
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3, Y4}	{0.18, 0.29, 0.35, 0.35, 0.38, 0.4, 0.55}	UI
Transmitter and dispersion penalty (max)	4.5	dB
Decision timing offsets for transmitter and dispersion penalty (min)	±1.6	ns

[a]The nominal transmitter type is not intended to be a requirement on the source type, and any transmitter meeting the transmitter characteristics specified may be substituted for the nominal transmitter type.
[b]The great majority of the transmitted spectrum has to fall within the operating wavelength range, see 58.7.2.
[c]The $RIN_{12}OMA$ recommendation is not mandatory.

58.3.2 Receiver optical specifications

The 100BASE-LX10 receiver's signaling speed, operating wavelength, damage, overload, sensitivity, reflectance and signal detect shall meet the specifications defined in Table 58–4 per measurement techniques defined in 58.7. Its stressed receive characteristics should meet the values listed in Table 58–4 per measurement techniques described in 58.7.11. The receiver sensitivity includes the extinction ratio penalty.

A compliant receiver may be shown to deliver an error ratio lower than that in the table at the received power shown in the table, or shown to deliver an error ratio lower than 10^{-10} at a received power 1 dB lower than the value in the table. Sensitivity measurement is described in 58.7.10. Similarly, stressed receiver conformance may be shown for the error ratio and power shown in the table, or for 10^{-10} and 1 dB lower power. The 10^{-10} limits are more demanding but can be verified more accurately with reasonable test times.

Table 58–4—100BASE-LX10 receive characteristics

Description	Type B1.1, B1.3 SMF	Unit
Signaling speed (range)	125 ± 50 ppm	MBd
Operating wavelength range	1260 to 1360	nm
Bit error ratio (max)	10^{-12}	

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Table 58–4—100BASE-LX10 receive characteristics *(continued)*

Description	Type B1.1, B1.3 SMF	Unit
Average received power[a] (max)	–8	dBm
Receiver sensitivity (max)	–25	dBm
Receiver sensitivity as OMA (max)	–24.8 (3.3)	dBm (μW)
Receiver reflectance[b] (max)	–12	dB
Stressed receiver sensitivity[c]	–20.1	dBm
Stressed receiver sensitivity as OMA (max)	–19.9 (10.2)	dBm (μW)
Vertical eye-closure penalty[d] (min)	3.7	dB
Stressed eye jitter (min)	0.25	UI pk-pk
Jitter corner frequency	20	kHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)	0.05, 0.15	UI
Signal detect threshold (min)	–45	dBm

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having a power level equal to the average received power (max) plus at least 1 dB.
[b]See 1.4 for definition of reflectance.
[c]The stressed receiver sensitivity is optional.
[d]Vertical eye closure penalty and the jitter specifications are test conditions for measuring stressed receiver sensitivity. They are not required characteristics of the receiver.

58.4 PMD to MDI optical specifications for 100BASE-BX10

The operating range for 100BASE-BX10 is defined in Table 58–1. A 100BASE-BX10-D or 100BASE-BX10-U compliant transceiver operates over the media types listed in Table 58–1 according to the specifications described in 58.9. A transceiver which exceeds the operational range requirement while meeting all other optical specifications is considered compliant.

NOTE—In this subclause and 58.3, the specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is explained in 58.7.6.

58.4.1 Transmit optical specifications

The 100BASE-BX10 transmitters' signaling speed, operating wavelength, spectral width, average launch power, extinction ratio, return loss tolerance, OMA, eye and TDP shall meet the specifications defined in Table 58–5 per measurement techniques described in 58.7. Its RIN_{12}OMA should meet the value listed in Table 58–5 per measurement techniques described in 58.7.7.

Table 58–5—100BASE-BX10 transmit characteristics

Description	100BASE-BX10-D	100BASE-BX10-U	Unit
Nominal transmitter type[a]	Longwave laser		
Signaling speed (range)	125 ± 50 ppm		MBd
Operating wavelength range[b]	1480 to 1580	1260 to 1360	nm
RMS spectral width (max)	4.6	7.7	nm

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Table 58–5—100BASE-BX10 transmit characteristics *(continued)*

Description	100BASE-BX10-D	100BASE-BX10-U	Unit
Average launch power (max)	–8		dBm
Average launch power (min)	–14		dBm
Average launch power of OFF transmitter (max)	–45		dBm
Extinction ratio (min)	6.6		dB
$RIN_{12}OMA$[c] (max)	–110		dB/Hz
Optical return loss tolerance (max)	12		dB
Launch OMA (min)	–12.9 (51.0)		dBm (μW)
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3, Y4}	{0.18, 0.29, 0.35, 0.35, 0.38, 0.4, 0.55}		UI
Transmitter and dispersion penalty (max)	4.5		dB
Decision timing offsets for transmitter and dispersion penalty (min)	±1.6		ns

[a]The nominal transmitter type is not intended to be a requirement on the source type, and any transmitter meeting the transmitter characteristics specified may be substituted for the nominal transmitter type.
[b]The great majority of the transmitted spectrum has to fall within the operating wavelength range, see 58.7.2.
[c]The $RIN_{12}OMA$ recommendation is not mandatory.

58.4.2 Receiver optical specifications

The 100BASE-BX10 receivers' signaling speed, operating wavelength, damage, overload, sensitivity, reflectance and signal detect shall meet the specifications defined in Table 58–6 per measurement techniques defined in 58.7. Its stressed receive characteristics should meet the values listed in Table 58–6 per measurement techniques described in 58.7.11. The receiver sensitivity includes the extinction ratio penalty.

Table 58–6—100BASE-BX10 receive characteristics

Description	100BASE-BX10-D	100BASE-BX10-U	Unit
Signaling speed (range)	125 ± 50 ppm		MBd
Operating wavelength range[a]	1260 to 1360	1480 to 1600	nm
Bit error ratio (max)	10^{-12}		
Average received power[b] (max)	–8		dBm
Receiver sensitivity (max)	–28.2		dBm
Receiver sensitivity as OMA (max)	–27.1 (1.94)		dBm (μW)
Receiver reflectance[c] (max)	–12		dB
Stressed receiver sensitivity[d]	–23.3		dBm
Stressed receiver sensitivity as OMA (max)	–22.3 (6.0)		dBm (μW)
Vertical eye-closure penalty[e] (min)	3.8		dB

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Table 58–6—100BASE-BX10 receive characteristics *(continued)*

Description	100BASE-BX10-D	100BASE-BX10-U	Unit
Stressed eye jitter (min)	0.25		UI pk-pk
Jitter corner frequency	20		kHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)	0.05, 0.15		UI
Signal detect threshold (min)	–45		dBm

[a]The receiver wavelength range of 100BASE-BX10-U is wider than the associated transmitter to allow interoperation with existing implementations of 100 Mb/s bi-directional transceivers.
[b]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having a power level equal to the average received power (max) plus at least 1 dB.
[c]See 1.4 for definition of reflectance.
[d]The stressed receiver sensitivity is optional.
[e]Vertical eye closure penalty and jitter specifications are test conditions for measuring stressed receiver sensitivity. They are not required characteristics of the receiver.

A compliant receiver may be shown to deliver an error ratio lower than that in the table at the received power shown in the table, or shown to deliver an error ratio lower than 10^{-10} at a received power 1 dB lower than the value in the table. Sensitivity measurement is described in 58.7.10. Similarly, stressed receiver conformance may be shown for the error ratio and power shown in the table, or for 10^{-10} and 1 dB lower power. The 10^{-10} limits are more demanding but can be verified more accurately with reasonable test times.

58.5 Illustrative 100BASE-LX10 and 100BASE-BX10 channels and penalties

Illustrative channels and penalties for 100BASE-LX10 and 100BASE-BX10 are shown in Table 58–7.

NOTE—The budgets include an allowance for –12 dB reflection at the receiver.

Table 58–7—Illustrative 100BASE-LX10 and 100BASE-BX10 channels and penalties

Description	100BASE-LX10	100BASE-BX10-D	100BASE-BX10-U	Unit
Fiber type	B1.1, B1.3 SMF			
Measurement wavelength for fiber	1310	1550	1310	nm
Nominal distance	10			km
Available power budget	10	14.2		dB
Maximum channel insertion loss[a]	6.0	5.5	6.0	dB
Allocation for penalties[b]	4.0	8.7	8.2	dB

[a]The maximum channel insertion loss is based on the cable attenuation at the target distance and nominal measurement wavelength. The channel insertion loss also includes the loss for connectors, splices and other passive components.
[b]The allocation for penalties is the difference between the available power budget and the channel insertion loss; insertion loss difference between nominal and worst-case operating wavelength is considered a penalty. For 100BASE-X, it is possible for the allocation for penalties to be less than the TDP limit, as some penalties measured by TDP may arise in the receiver and need not be counted twice.

58.6 Jitter at TP1 and TP4 for 100BASE-LX10 and 100BASE-BX10

Jitter at TP1 and TP4 for 100BASE-LX10 and 100BASE-BX10 is informatively described in 58B.1.

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58.7 Optical measurement requirements

The following subclauses describe definitive patterns and test procedures for certain PMDs of this standard. implementers using alternative verification methods need to ensure adequate correlation and allow adequate margin such that specifications are met by reference to the definitive methods.

All optical measurements, except TDP and RIN, shall be made through a short patch cable, between 2 m and 5 m in length.

NOTE—58.7.5, 58.7.6, 58.7.7, 58.7.9, 58.7.10, 58.7.11, and 58.7.12 apply to Clause 58, Clause 59, and Clause 60. Clause 59 (1000BASE-LX10) uses multimode fiber, although Clause 58 (100BASE-LX10 and 100BASE-BX10) and Clause 60 (1000BASE-PX10 and 1000BASE-PX20) do not.

58.7.1 Test patterns

Compliance is to be achieved in normal operation. The definitive patterns for testing are shown in Table 58–8.

Table 58–8—List of test patterns and tests

Test pattern	Test	Related subclause
Valid 100BASE-X signal	Wavelength Spectral width	58.7.2
Valid balanced NRZI encoded 4B/5B bit stream	Optical power	58.7.3
Idle or far-end fault indication (see Clause 24)	Extinction ratio OMA RIN_xOMA	58.7.4 58.7.5 58.7.7
Optical frame-based test pattern of 58.7.1.1	Eye mask TDP Receiver sensitivity Stressed receiver sensitivity Jitter measurements	58.7.8 58.7.9 58.7.10 58.7.11 58.7.12

58.7.1.1 100BASE-X optical frame-based test pattern

Transmit eye mask, TDP and sensitivity are to be assured against the test pattern defined below. This represents an extremely untypical pattern. The BER in service can be expected to be lower than with the test pattern. In this clause, extinction ratio, OMA and RIN_xOMA are referred to the idle pattern (1010… for 4B/5B NRZI) or the nearly identical far-end fault indication.

The following test pattern is intended for frame-based testing of the 100BASE-LX10 and 100BASE-BX10 PMDs. It contains compliant Ethernet frames with adequate user defined fields to allow them to be passed through a system to the point of the test. Further information on frame-based testing is included in Annex 58A. The test suite and the recommended patterns are shown in Table 58–8.

NOTE—Users are advised to take care that the system under test is not connected to a network in service.

The test pattern shall be constructed as follows.

A test pattern for base line wander is composed of a sequence of three frames continuously repeated. Each frame has a 1500 octet length client data field and a zero length pad field. The contents of the destination address, source address, length/type fields and the first 32 octets of the client data field are at the discretion of the tester and may be implementation specific. The remaining 1468 octets of the client data field are filled with symbols with an even number of ones in the 4B/5B encoded data prior to NRZI transmission as shown in Table 58–9.

Frames are separated by a near minimum interpacket gap (IPG) of 14 octets.

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Within the limits of the three bit maximum run length of the 4B/5B code this sequence gives a near worst case ISI pattern and provides alternating periods of high and low transition density to test clock and data recovery (CDR) performance.

The first 32 octets of the client data field are configured such that, after the frame check sequence (FCS) is added, there are an even number of ones in the first two packets and an odd number of ones in the third packet. This results in a six frame sequence on the line (after NRZI) with three frames containing near 40% ones density and three frames with near 60% ones density. Table 58–10 shows a pattern, nearly identical to the pattern in Table 58–9, that ends in 0 rather than 1 and can be used to join a 40% section to a 60% section. The "flipping" content causes a different frame check sequence which in turn causes the following idle to be inverted.

When transmitted with a near minimum interpacket gap the resulting data stream has baseline wander at 1.35 kHz. In the example shown, IEEE Std 802.2 logical link control headers are used to form TEST command PDUs with null DSAP and SSAP addresses.

Table 58–9—Example unbalanced pattern

Item	Number of octets	Code-group name or hexa-decimal value	TXD<3:0>[a] (binary)		4B/5B encoded (binary)		NRZI encoded (binary)			
			1st nibble	2nd nibble	1st code-group[b]	2nd code-group	40% mark ratio		60% mark ratio	
Idle	13	I	Idle	Idle	11111	11111	10101	01010	01010	10101
Start-of-stream delimiter (SSD)	1	/J/K/			11000	10001	10000	11110	01111	00001
Remainder of preamble	6	55	0101	0101	01011	01011	01101	10010	10010	01101
Start of frame delimiter	1	D5	0101	1101	01011	11011	01101	01101	10010	10010
Destination address[c]	6	FF	1111	1111	11101	11101	01001	01001	10110	10110
Source address	6	00	0000	0000	11110	11110	01011	01011	10100	10100
Length/type	2	05	0101	0000	01011	11110	10010	10100	01101	01011
		DC	1100	1101	11010	11011	10011	01101	01100	10010
DSAP	1	00	0000	0000	11110	11110	01011	01011	10100	10100
SSAP	1	00	0000	0000	11110	11110	01011	01011	10100	10100
Control	1	F3	0011	1111	10101	11101	11001	01001	00110	10110
Implementation specific (example)	1	06	0110	0000	01110	11110	10100	10100	01011	01011
	28	00	0000	0000	11110	11110	10100	10100	01011	01011
Low transition density[d]	968	42	0010	0100	10100	01010	11000	01100	00111	10011
		24	0100	0010	01010	10100	01100	11000	10011	00111
Mixed	8	00	0000	0000	11110	11110	10100	10100	01011	01011
		D2	0010	1101	10100	11011	11000	10010	00111	01101
High transition density	484	07	0111	0000	01111	11110	01010	10100	10101	01011
		70	0000	0111	11110	01111	10100	01010	01011	10101
Mixed	8	00	0000	0000	11110	11110	10100	10100	01011	01011
		D2	0010	1101	10100	11011	11000	10010	00111	01101
Frame check sequence 1[e]	1	FF	1111	1111	11101	11101	10110	10110	01001	01001
Frame check sequence 2	1	13	0011	0001	10101	01001	00110	01110	11001	10001

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Table 58–9—Example unbalanced pattern *(continued)*

Item	Number of octets	Code-group name or hexa-decimal value	TXD<3:0>[a] (binary)		4B/5B encoded (binary)		NRZI encoded (binary)			
			1st nibble	2nd nibble	1st code-group[b]	2nd code-group	40% mark ratio		60% mark ratio	
Frame check sequence 3	1	9E	1110	1001	11100	10011	10111	00010	01000	11101
Frame check sequence 4	1	59	1001	0101	10011	01011	11101	10010	00010	01101
End-of-stream delimiter (ESD)	1	/T/R/			01101	00111	01001	11010	10110	00101

[a]See Table 24–2.
[b]The five bit code-groups are transmitted left most bit first.
[c]Use of the example broadcast address may cause problems in a system test; any unicast address is preferable. Other source and destination addresses may be chosen.
[d]The first row precedes the second row and the sub-sequence is repeated 16 times. This pattern can be varied to cause the disparity to remain the same or flip.
[e]The frame check sequence for another pattern may be calculated following 3.2.9 and Clause 24.

Table 58–10—Example unbalanced pattern to flip polarity

Item	Number of octets	Code-group name or hexa-decimal value	TXD<3:0> (binary)		4B/5B encoded (binary)		NRZI encoded (binary)			
			1st nibble	2nd nibble	1st code-group	2nd code-group	40% mark ratio		60% mark ratio	
Idle, SSD, preamble, SFD, DA, SA, Length/ type, DSAP, SSAP, Control	38	As in Table 58–9								
Flipping	1	05	0101	0000	01011	11110	10010	10100	01101	01011
Implementation specific, and pattern	1496	As in Table 58–9								
Frame check sequence 1	1	0B	1011	0000	10111	11110	11010	10100	00101	01011
Frame check sequence 2	1	E2	0010	1110	10100	11100	11000	10111	00111	01000
Frame check sequence 3	1	08	1000	0000	10010	11110	00011	01011	11100	10100
Frame check sequence 4	1	3B	1011	0011	10111	10101	00101	11001	11010	00110
End-of-stream delimiter (ESD)	1	/T/R/			01101	00111	10110	00101	01001	11010

NOTE—While it is expected that these frames will be counted by a DTE under test, the likelihood of additional behavior means that the DTE should not be connected to a network in service while being tested.

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58.7.2 Wavelength and spectral width measurements

The wavelength and spectral width (RMS) shall meet specifications according to the centroidal wavelength and RMS spectral width definitions in IEC 61280-1-3, under modulated conditions using a valid 100BASE-X signal.

NOTE—The great majority of the transmitted spectrum has to fall within the operating wavelength range. The allowable range of central wavelengths is narrower than the operating wavelength range by the actual RMS spectral width at each extreme.

58.7.3 Optical power measurements

Optical power shall meet specifications according to the methods specified in IEC 61280-1-1. A measurement may be made with the port transmitting any valid balanced NRZI encoded 4B/5B bit stream.

58.7.4 Extinction ratio measurements

Extinction ratio shall meet specifications according to IEC 61280-2-2 with the port transmitting the NRZI encoded 4B/5B idle pattern (1010…) or far-end fault indication, that may be interspersed with OAM packets per 57A.2 and with minimal back reflections into the transmitter, lower than –20 dB. The extinction ratio is expected to be similar for other valid balanced NRZI encoded 4B/5B bit streams. The test receiver has the frequency response as specified for the transmitter optical waveform measurement.

58.7.5 Optical modulation amplitude (OMA) measurements (optional)

The normative way of measuring transmitter characteristics is extinction ratio and mean power. The following clause is intended to inform on how the OMA measurement is performed.

In this clause, OMA is the difference in optical power for “1” and “0” levels of the optical signal in an idle (10101… for 100BASE-LX10 and 100BASE-BX10) sequence or far-end fault indication. It may be found using waveform averaging or histogram means. The measurement is recommended to be equivalent to that described below.

The recommended technique for measuring optical modulation amplitude is illustrated in Figure 58–3. A fourth-order Bessel-Thomson filter as specified for measuring the transmitter concerned is to be used with the O/E converter. The measurement system consisting of the O/E converter, the filter and the oscilloscope is calibrated at the appropriate wavelength for the transmitter under test.

With the device under test transmitting the idle pattern or far-end fault indication, use the following procedure to measure optical modulation amplitude:

a) Configure the test equipment as illustrated in Figure 58–3.
b) Measure the mean optical power P_1 of the logic “1” as defined over the center 20% of the time interval, here 1 UI long, where the signal is in the high state.
c) Measure the mean optical power P_0 of the logic “0” as defined over the center 20% of the time interval, here 1 UI long, where the signal is in the low state.
d) $OMA = P_1 - P_0$.

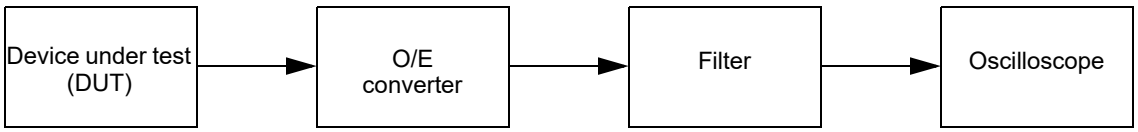

Figure 58–3—Recommended test equipment for measurement of optical modulation amplitude

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A method of approximating OMA is shown in Figure 58–9.

Similarly, the optical power measure A_N is to be measured with a square wave pattern consisting of four to eleven consecutive ones followed by an equal run of zeros. Five ones followed by five zeros is convenient (the /H/ code-group in Clause 24, or K28.7 in 1000BASE-X which is the "Low-frequency test pattern" of 36A.2). The OMA of Clause 52 is A_N, and OMA here may differ.

NOTE—This OMA measurement procedure applies to Clause 58, Clause 59, and Clause 60.

58.7.6 OMA relationship to extinction ratio and power measurements

Annex 58B provides information on how OMA, extinction ratio, and mean power, are related to each other (see 58B.2).

58.7.7 Relative intensity noise optical modulation amplitude (RIN_xOMA) measuring procedure

This procedure describes a component test that may not be appropriate for a system level test depending on the implementation. If used, the procedure is performed as described in 58.7.7.1, 58.7.7.2, and 58.7.7.3.

NOTE—This RIN_xOMA measurement procedure applies to Clause 58, Clause 59, and Clause 60.

58.7.7.1 General test description

The test arrangement is shown in Figure 58–4. The optical path between the Device Under Test (DUT) and the detector has a single discrete reflection with the specified optical return loss as seen by the DUT.

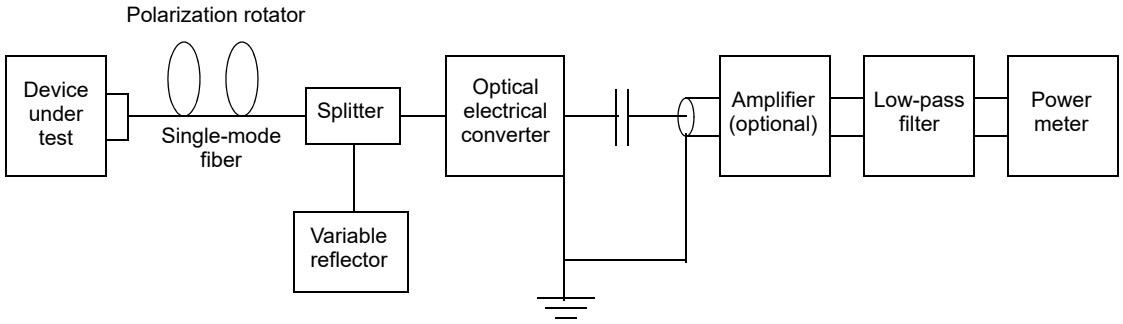

Figure 58–4—RIN_xOMA measurement setup

Both the OMA power and noise power are measured by AC-coupling the O/E converter into the electrical power meter. If needed, an amplifier may be used to boost the signal to the power meter. A low-pass filter is used between the photo detector and the power meter to limit the noise measured to the passband appropriate to the data rate of interest. In order to measure the noise, the modulation to the DUT is turned off.

58.7.7.2 Component descriptions

The optical path and detector combination is configured for a single dominant reflection with an optical return loss as specified in the appropriate transmitter table, e.g., Table 58–3. (The optical return loss may be determined by the method of FOTP-107.) The length of the fiber is not critical but should be in excess of 2 m.

The polarization rotator is capable of transforming an arbitrary orientation elliptically polarized wave into a fixed orientation linearly polarized wave.

If necessary, the noise may be amplified to a level consistent with accurate measurement by the power meter.

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The upper –3 dB limit of the measurement apparatus is as specified for the transmitter optical waveform test. The bandwidth used in the RIN calculation takes the low-frequency cutoff of the DC-blocking capacitor into consideration. The low-frequency cutoff is recommended to be less than 1 MHz. The filter should be placed in the circuit as the last component before the power meter so that any high-frequency noise components generated by the detector/amplifier are eliminated. If the power meter used has a very wide bandwidth, care should be taken to ensure that the filter does not lose its rejection at extremely high frequencies.

The RMS electrical power meter should be capable of being zeroed in the absence of input optical power to remove any residual noise.

58.7.7.3 Test procedure

Use the following procedure to test relative intensity noise optical modulation amplitude:

a) With the DUT disconnected, zero the power meter;
b) Connect the DUT, turn on the laser, and ensure that the laser is not modulated;
c) Operate the polarization rotator while observing the power meter output to maximize the noise read by the power meter. Note the maximum power, P_N;
d) Turn on the modulation to the laser using the pattern specified for the PMD type (e.g., in 58.7.1 and 59.7.1) and note the power measurement, P_M. It may be necessary to change or remove the effective reflection to obtain an accurate reading;
e) Calculate RIN from the observed electrical signal power and noise power by use of Equation (0–1).

$$RIN_xOMA = 10 \times \log_{10}\frac{P_N}{BW \times P_M} \text{ [dB/Hz]} \quad (0–1)$$

where:

RIN_xOMA = Relative Intensity Noise referred to optical modulation amplitude measured with x dB reflection,
P_N = Electrical noise power in Watts with modulation off,
P_M = Electrical power in Watts with modulation on,
BW = Low-pass bandwidth of apparatus – high-pass bandwidth of apparatus due to DC-blocking capacitor [noise bandwidth of the measuring system (Hz)].

For testing multimode components or systems, the polarization rotator is removed from the setup and the single-mode fiber replaced with a multimode fiber. Step c) of the test procedure is eliminated.

58.7.8 Transmitter optical waveform (transmit eye)

The required transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 58–5 for 100BASE-LX10 and 100BASE-BX10. Compliance is to be assured during system operation. The transmitter optical waveform of a port transmitting the test pattern specified for the PMD type, e.g., in 58.7.1, shall meet specifications according to the methods specified below.

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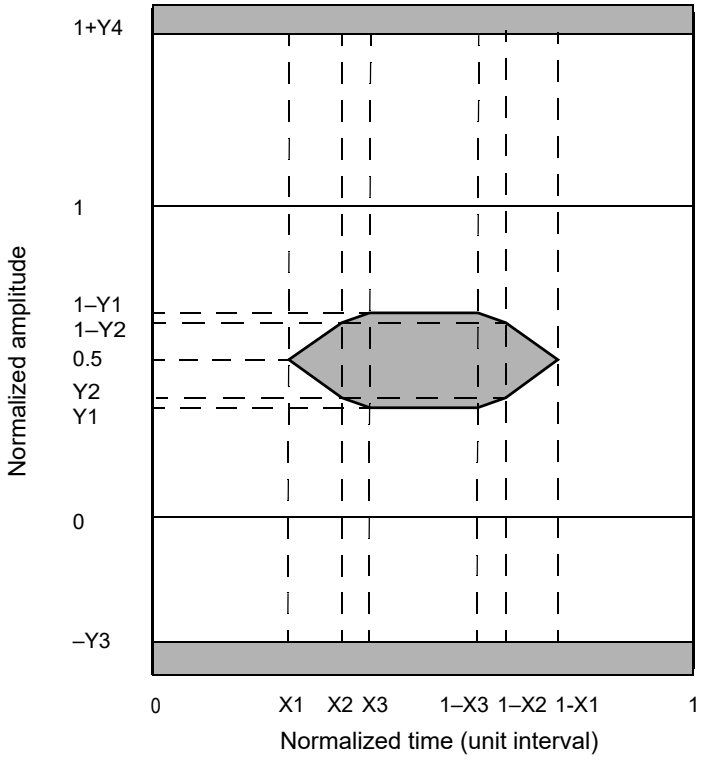

Figure 58–5—Transmitter eye mask definition

NOTE—This transmitter optical waveform measurement procedure applies to Clause 58, Clause 59, and Clause 60.

Normalized amplitudes of 0 and 1 represent the amplitudes of logic ZERO and ONE respectively. These are defined by the means of the lower and upper halves of the central 0.2 UI of the eye. 0 and 1 on the unit interval scale are to be determined by the eye crossing means. A clock recovery unit (CRU) may be used to trigger the scope for mask measurements as shown in Figure 58–6. It should have a high-frequency corner bandwidth of less than or equal to the jitter corner frequency in the appropriate table for the transmitter's peer receiver, e.g., Table 58–4 or Table 58–6, and a slope of –20 dB/decade. The CRU tracks acceptable levels of low frequency jitter and wander. The frequency response of the measurement instrument (e.g., oscilloscope) extends substantially lower than the test pattern repetition frequency. A DC-coupled instrument is convenient.

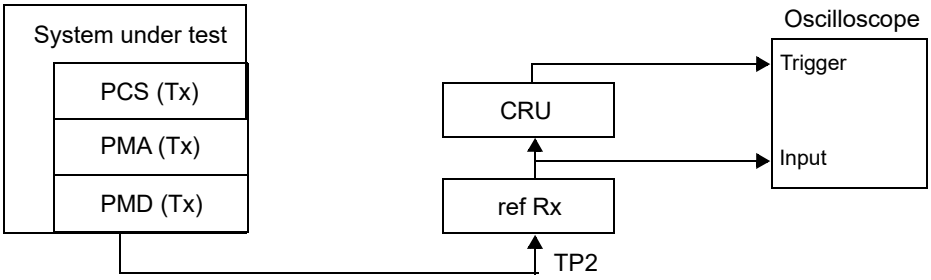

Figure 58–6—Transmitter optical waveform test block diagram

For 100BASE-LX10 and 100BASE-BX10, the eye is measured with respect to the mask of the eye using a receiver with a fourth-order Bessel-Thomson response with nominal f_r of 116.64 MHz as specified for STM-

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1 in ITU-T G.957, with the tolerances there specified. Receiver responses for other PMD types are specified in the appropriate clause. The Bessel-Thomson receiver is not intended to represent the noise filter used within a compliant optical receiver, but is intended to provide uniform measurement conditions at the transmitter.

The transmitter shall achieve a hit ratio lower than 5×10^{-5} hits per sample, where "hits" are the number of samples within the grey areas of Figure 58–5, and the sample count is the total number of samples from 0 UI to 1 UI.

NOTE—As an example, if an oscilloscope records 1350 samples/screen, and the timebase is set to 0.2 UI/div with 10 divisions across the screen, and the measurement is continued for 200 waveforms, then a transmitter with an expectation of less than 6.75 hits is compliant:

$$5 \times 10^{-5} \times 200 \times \frac{1350}{(0.2 \times 10)} = 6.75 \quad (0–2)$$

Likewise, if a measurement is continued for 1000 waveforms, then an expectation of less than 33.75 hits is compliant. An extended measurement is expected to give a more accurate result, and a single reading of 6 hits in 200 waveforms would not give a statistically significant pass or fail. Measurements to "zero hits," which involve finding the position of the worst single sample in the measurement, have degraded reproducibility because random processes cause the position of such a single low-probability event to vary.

The hit ratio limit has been chosen to avoid misleading results due to transmitter and oscilloscope noise, and to give the best correlation to transmitter penalty; see 58.7.9.5.

Further information on optical eye pattern measurement procedures may be found in IEC 61280-2-2.

58.7.9 Transmitter and dispersion penalty (TDP) measurement

The TDP of a port transmitting the appropriate test pattern test shall meet specifications according to the methods specified below. The transmitter and dispersion penalty (TDP) measurement tests for transmitter impairments with chromatic effects for a transmitter to be used with single-mode fiber, and for transmitter impairments with modal (not chromatic) dispersion effects for a transmitter to be used with multimode fiber. Possible causes of impairment include intersymbol interference, jitter, RIN and mode partition noise. Meeting the separate requirements (e.g., eye mask, spectral characteristics) does not in itself guarantee the TDP. The procedure tests for pattern dependent effects; for 100BASE-LX10 and 100BASE-BX10, a standardized element of pattern dependent baseline wander is included in the reference channel.

Transmitter and dispersion penalty may be measured with apparatus shown in Figure 58–7, consisting of a reference transmitter, the transmitter under test, a controlled optical reflection, an optical attenuator, a test fiber, and a reference receiver system containing a reference receiver front end (optical to electrical converter), a transversal filter to emulate multimode fiber, if appropriate, and a bit error ratio tester. All BER and sensitivity measurements are made with the test patterns specified for the PMD type, e.g., in 58.7.1

NOTE 1—This TDP measurement procedure applies to Clause 58, Clause 59, and Clause 60.

NOTE 2—Multimode fiber is not used with 100BASE-LX10 or 100BASE-BX10.

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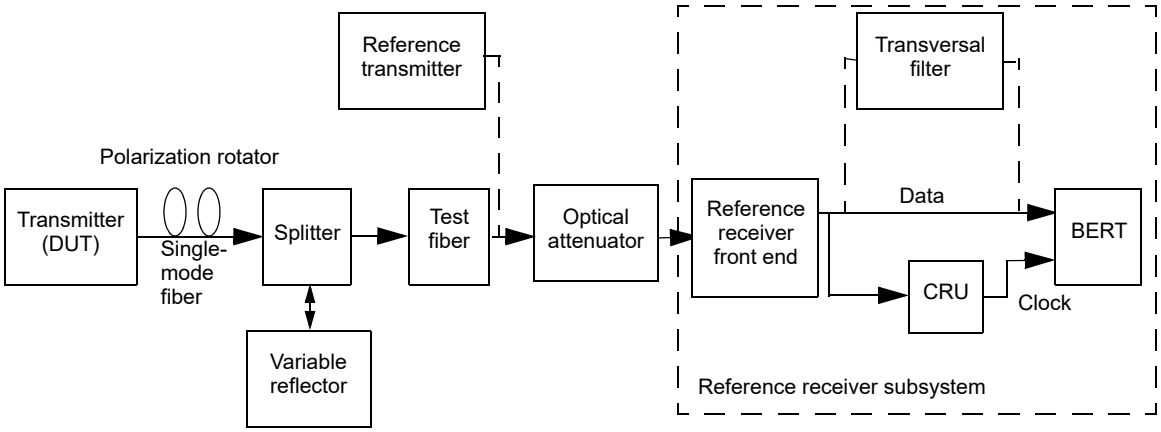

Figure 58–7—Test setup for measurement of transmitter and dispersion penalty

58.7.9.1 Reference transmitter requirements

The reference transmitter is a high-quality instrument-grade device, which can be implemented by a CW laser modulated by a high-performance modulator. It should meet the following basic requirements:

a) The rise/fall times should be less than 0.15 UI at 20% to 80%.
b) The output optical eye is symmetric and with good margin to the eye mask test for the transmitter (PMD) type under test.
c) In the center 20% region of the eye, the worst-case vertical eye closure penalty, as defined in 58.7.11.2, is less than 0.5 dB.
d) Jitter less than 0.20 UI peak-peak.
e) $RIN_{12}OMA$ should be minimized to less than –120 dB/Hz for 100BASE-X and –125 dB/Hz for 1000BASE-X.

58.7.9.2 Channel requirements

The transmitter is tested using an optical and electrical channel that meets the requirements specified for the PMD type listed in Table 58–11. A transmitter is to be compliant with a total dispersion at least as negative as the “minimum dispersion” and at least as positive as the “maximum dispersion” columns specified for the wavelength of the device under test. This may be achieved with a channel or channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

When emulating a multimode fiber link, the optical channel is a 2 m to 5 m patch cord meeting the appropriate specifications. In this case, the link bandwidth is emulated in the electrical domain.

The channel provides a maximum optical return loss specified as “Optical return loss tolerance (maximum)” in the specification of the transmitter under test. For a single-mode fiber channel, the state of polarization of the back reflection is adjusted to create the greatest RIN. The methods of 58.7.7.2 and 58.7.7.3 may be used.

The BERT’s receiver sensitivity needs to be adequate to meet the BER with the worst-case test signal and minimum attenuation.

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Table 58–11—Transmitter compliance channel specifications

PMD transmitter wavelength, fiber type	Optical channel			Electrical channel
	Dispersion[a] (ps/nm)		Optical return loss[b] (max)	Differential delay (ps)
	Minimum	Maximum		
1310 nm band for SMF	$0.02325 \cdot L^{c} \cdot \lambda \cdot [1-(1324/\lambda)^4]$	$0.02325 \cdot L \cdot \lambda \cdot [1-(1300/\lambda)^4]$	See ORLT in Transmitter spec	N/A
1550 nm band for SMF	0	$0.02325 \cdot L \cdot \lambda \cdot [1-(1300/\lambda)^4]$		N/A

[a]The dispersion is specified for the actual wavelength of the device under test.
[b]The optical return loss is applied with respect to TP2.
[c]L is the upper operating range limit (reach) as defined e.g. in Table 58–1.

58.7.9.3 Reference receiver requirements

The reference receiver system should have the bandwidth specified for the transmitter optical waveform measurement for the transmitter under test. The sensitivity of the reference receiver system should be limited by Gaussian noise. The receiver system should have minimal threshold offset, deadband, hysteresis, deterministic jitter or other distortions. Decision sampling should be instantaneous with minimal uncertainty and setup/hold properties. When testing 100BASE-X optical transmitters, the receiver should have a passband not extending below 10 kHz at the –3 dBe (electrical) point, so as to emulate the pattern-induced baseline wander expected in a compliant receiver.

For all transmitter and dispersion penalty measurements, determination of the center of the eye is required. The center of the eye is defined as the time halfway between the left and right sampling points within the eye where the measured BERs are equal to each other, and greater than or equal to 10^{-3} (the BER at the eye center is much lower). The decision threshold is to occur at the average signal level.

For a transmitter to be used with multimode fiber the reference receiver is followed by a transversal filter with two equal amplitude paths with a differential delay as specified for the transmitter. In this case, the receiver front end should be operating in its linear regime (not clipping). For a transmitter to be used with single-mode fiber, the transversal filter is not used.

The clock recovery unit (CRU) used in the TDP measurement has a corner frequency of less than or equal to the jitter tolerance frequency specified for the appropriate receiver (the peer PMD to the transmitter under test), and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low-frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.

The nominal sensitivity of the reference receiver system, S, is measured in OMA using the apparatus described above but with a short patchcord in place of the test fiber and without any transversal filter. The sensitivity S has to be corrected for any significant reference transmitter impairments including any vertical eye closure. It should be measured while sampling at the eye center or corrected for off-center sampling. It is calibrated at the wavelength of the transmitter under test. For 100BASE-LX10 and 100BASE-BX10, TDP includes a pattern dependent penalty. It may be inconvenient or impossible to obtain reference transmitters and receivers which are immune to this penalty. For these cases, S may be measured with a benign pattern e.g., PRBS7.

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58.7.9.4 Test procedure

To measure the transmitter and dispersion penalty (TDP) the following procedure is used. The sampling instant is displaced from the eye center by the amount specified for decision timing offsets in e.g., Table 58–3 or Table 58–5. The following procedure is repeated for early and late decision and the larger TDP value is used:

a) Configure the test equipment as described above and illustrated in Figure 58–7.
b) Adjust the attenuation of the optical attenuator to obtain a BER of 10^{-12}. Extrapolation techniques may be used with care.
c) Record the optical power in OMA at the input to the reference receiver, P_DUT, in dBm.
d) If P_DUT is larger than S, the transmitter and dispersion penalty (TDP) for the transmitter under test is the difference between P_DUT and S, TDP = P_DUT – S. Otherwise the transmitter and dispersion penalty is zero, TDP = 0.

It is to be ensured that the measurements are made in the linear power regime of the fiber.

58.7.9.5 Approximate measures of TDP

Approximate measures of TDP are informatively described in 58B.3.

58.7.10 Receiver sensitivity measurements

Receiver sensitivity is defined for an ideal input signal. The test signal should have negligible impairments such as intersymbol interference (ISI), jitter and RIN (but see the end of this subclause). The test pattern shall be as specified in 58.7.1, 59.7.1 or 60.9.1 as appropriate. Sensitivity is defined by the specified bit error ratio, which may be determined by counting bit or byte errors or errored frames. Extrapolation techniques may be used with care. Sensitivity is measured at a low but compliant extinction ratio, and correction made for any difference between the measurement extinction ratio and the specified minimum extinction ratio. This assurance should be met with asynchronous data flowing out of the optical transmitter of the system under test. The output data pattern from the transmitter of the system under test is the same pattern as defined for this measurement.

The sampling point is set by the system under test. While this standard applies to complete data terminal equipment (DTE), the test may be used as a diagnostic for testing components with appropriate margin, in which case the sampling point should be set at the average optical power level and at the specified timing offsets from the eye center, which may be found as the mid-point between the 10^{-3} BER points.

An implementer may use a combination of extrapolation and margin to assure compliance. This can entail a statistical analysis which could be implementation specific. As an example, with a small margin, it might not be advisable to extrapolate beyond a limited optical power difference; this represents an extrapolation in BER terms which varies according to circumstance.

In the case of 100BASE-X, systematic baseline wander of the input signal is to be expected. This may be generated with AC-coupling above 10 kHz within the transmitter, and/or with the interfering signal technique as described in 58.7.11.2. A standardized baseline wander of ± OMA/10 is defined for these PMD types. This causes some jitter in the test signal, which is acceptable.

For 100BASE-LX10 and 100BASE-BX10 only, sensitivities are defined for 10^{-12} and 10^{-10} bit error ratios. It is sufficient to show compliance to either of these. The 10^{-10} limit is the more demanding but can be verified more accurately with reasonable test times.

NOTE—This receiver sensitivity measurement applies to Clause 58, Clause 59, and Clause 60.

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58.7.11 Stressed receiver conformance test

The stressed receiver conformance test is intended to screen against receivers with poor frequency response or timing characteristics that could cause errors when combined with a distorted but compliant signal at TP3. Modal (MMF) or chromatic (SMF) dispersion can cause distortion. Stressed receiver tolerance testing may be performed in accordance with the requirements of 58.7.11.1, 58.7.11.2, and 58.7.11.3. If this test is applied the receiver shall be compliant to for example Table 58–4.

A receiver should receive a conditioned input signal that combines vertical eye closure and jitter according to this clause with BER specified in the receiver tables. This assurance should be met with asynchronous data flowing out of the optical transmitter of the system under test. The output data pattern from the transmitter of the system under test is to be the same pattern as defined for this measurement.

NOTE 1—The length of the test pattern, low signaling rate and narrow rate tolerance of 100BASE-X means that the input and output patterns beat very slowly. Long test times or a slight modification to the length of one pattern may be appropriate.

NOTE 2—This stressed receiver conformance test applies to Clause 58, Clause 59, and Clause 60.

58.7.11.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 58–8. A pattern generator continuously generates a signal or test pattern as specified for the receiver under test, e.g., in 58.7.1. The optical test signal is conditioned (stressed) using the methodology, as defined in 58.7.11.2, while applying sinusoidal jitter, as specified e.g., in 58.7.11.4. The receiver of the system under test is tested for conformance by counting bit or byte errors or errored frames. The optical power penalty for the stressed eye is intended to be similar to its vertical eye closure penalty. This is not necessarily the same as the highest TDP anticipated in service, but represents a standardized test condition for the receiver.

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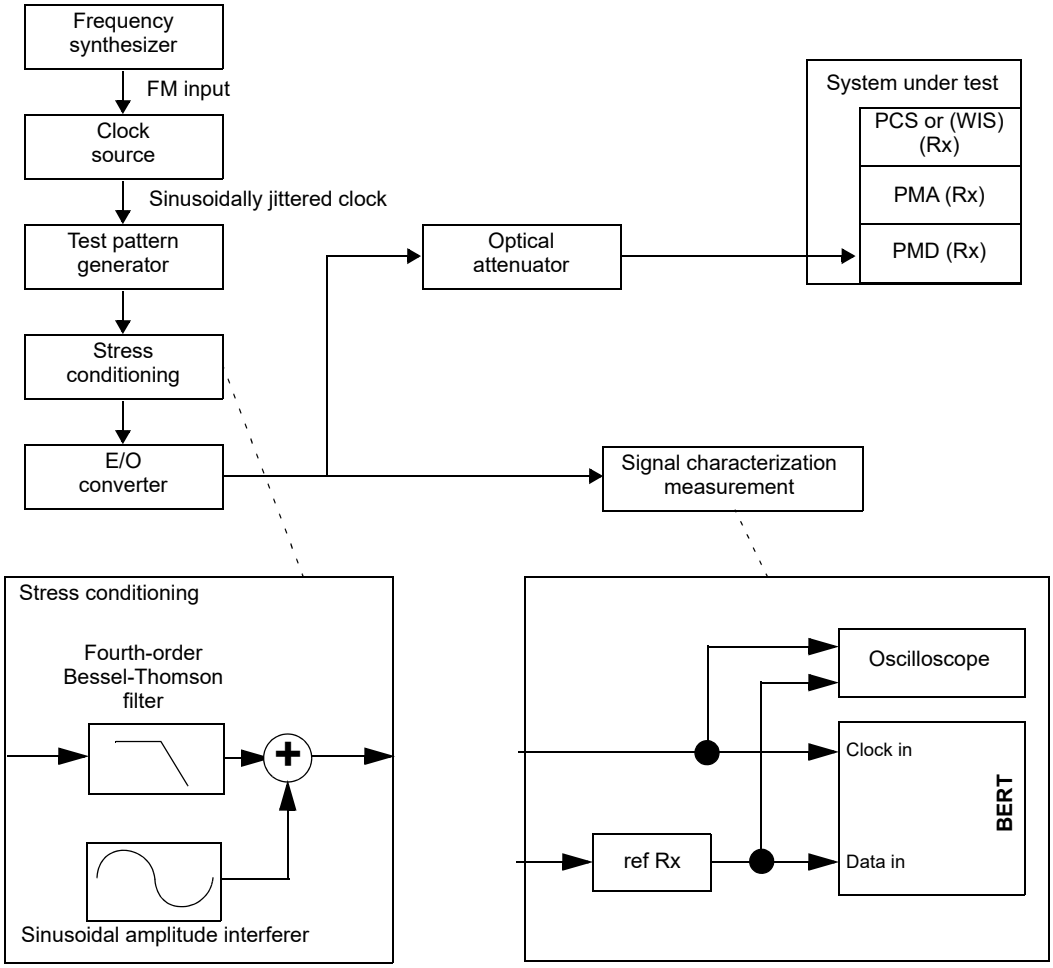

Figure 58–8—Stressed receiver conformance test block diagram

A suitable test set is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics. The test fiber called out for single-mode fiber based PMD layers and the transversal filter called out to emulate multimode fiber are not needed to characterize the receiver input signal; nor are they used during testing.

The fourth-order Bessel-Thomson filter is used to create ISI-induced vertical eye closure. The sinusoidal amplitude interferer causes additional eye closure, but in conjunction with the slowed edge rates from the filter, also causes jitter. The nature of the jitter is intended to emulate instantaneous bit shrinkage that can occur with DDJ. This type of jitter cannot be created by simple phase modulation. The sinusoidal phase modulation represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter.

For improved visibility for calibration, it is imperative that the Bessel-Thomson filter and all other elements in the signal path (cables, DC blocks, E/O converter, etc.) have wide and smooth frequency response and linear phase response throughout the spectrum of interest. Overshoot and undershoot should be minimized. If this is achieved, then data dependent effects should be minimal, and short data patterns can be used for calibration with the benefit of providing much improved trace visibility on sampling oscilloscopes. Actual patterns for testing the receiver are specified in the appropriate clause.

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To further improve visibility for calibration, random noise effects, such as RIN and random clock jitter, should also be minimized. A small amount of residual noise and jitter from all sources is unavoidable, but should be less than 0.25 UI peak-peak of jitter.

The test pattern generator, filter and E/O converter should together have a frequency response to result in the appropriate level of initial ISI eye closure before the sinusoidal terms are added. The E/O converter should have a linear response if electrical summing is used, linearity of all elements including the E/O modulator is critical. Summing with an optical coupler after the modulator is an option that eases linearity requirements, but requires a second source for the interfering signal, will complicate settings of extinction ratio, and will add more RIN. In either case, a typical optical transmitter with built-in driver is not linear and not suitable.

The vertical and horizontal eye closures to be used for receiver conformance testing are verified using an optical reference receiver with the response specified for the appropriate transmitter (the peer PMD to the receiver under test) e.g., in 58.7.8. Use of standard tolerance filters may significantly degrade this calibration. Care should be taken to ensure that all the light from the fiber is collected by the fast photo detector and (if using multimode fiber) that there is negligible mode selective loss, especially in the optical attenuator and the optical coupler, if used. The reference receiver and oscilloscope should achieve adequately low noise and jitter.

The clock output from the clock source in Figure 58–8 will be modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye jitter that includes the sinusoidal jitter component, a separate clock source (clean clock of Figure 58–8) is required that is synchronized to the source clock, but not modulated with the jitter source.

58.7.11.2 Stressed receiver conformance test signal characteristics and calibration

The conformance test signal is used to validate that the PMD receiver meets BER requirements with near worst case waveforms at TP3 including pulse width shrinkage, power, simulated channel penalties, and a swept frequency sinusoidal jitter contribution.

Signal characteristics are described below along with a suggested approach for calibration.

The test signal includes vertical eye closure and high-probability jitter components. Vertical eye closure is measured at the time center of the eye (halfway between 0 and 1 on the unit interval scale as determined by the eye crossing means) and is the vertical eye closure penalty (VECP) when calculated relative to the measured A_N value. J is measured at the average optical power, which can be obtained with AC-coupling. The values of these components are defined as below by their histogram results. The vertical eye closure penalty is given in Equation (0–3):

$$\text{Vertical eye closure penalty [dB, optical]} = 10 \times \log_{10}\frac{A_N}{A_O} \tag{0–3}$$

where, A_O is the amplitude of the eye opening and A_N is the normal amplitude without ISI, as shown in Figure 58–9. A_N can be approximated with histograms as suggested in Figure 58–9. However, the definition for A_N is given in 58.7.5.

For this test, VECP is defined by the 99.95th percentile of the histogram of the lower half of the signal and the 0.05th percentile of the histogram of the upper half of the signal, and jitter is defined by the 0.5th and 99.5th percentiles of the jitter histogram. Histograms should include at least 10 000 hits, and should be about 1%-width in the direction not being measured. Residual low-probability noise and jitter should be minimized—that is, the outer slopes of the final histograms should be as steep as possible down to very low probabilities.

The following steps describe a suggested method for calibrating a stressed eye generator:

a) Set the signaling speed of the test-pattern generator as specified for the appropriate transmitter. Sinusoidal interference and jitter signals should be turned off at this point.

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b) Turn on the calibration pattern. A repetitive pattern may be used for calibration if the conditions described in 58.7.11.1 are met, but this increases the risk that the longer test pattern used during testing will overstress the device under test.
c) Set the extinction ratio to approximately the extinction ratio (minimum) value as specified for the appropriate transmitter. If optical summing is used, the extinction ratio may need to be adjusted after the sinusoidal interference signal is added below.
d) Measure the settled signal amplitude A_N of the test signal (without attenuation). A_N may be measured according to 58.7.5 using a square wave pattern, although for the purposes of this clause, OMA is to be measured with a different pattern; A_N and OMA are not likely to be equal.
e) The requirements for vertical eye closure and jitter of the stressed eye test signal are given by the vertical eye closure penalty (VECP) and stressed eye jitter (J) values given in the appropriate receiver specification table.

   There are three components involved in calibration for vertical closure and J. These are a linear phase filter, sinusoidal interference, and sinusoidal jitter.

   In general, the majority of the vertical eye closure penalty value should be created by use of a linear phase, low jitter filter (such as Bessel-Thomson). In the case of 100BASE-X, the majority of the vertical eye closure penalty value should be created by baseline wander or sinusoidal interference. The filter should be tested with the prescribed test patterns to verify that residual jitter is small, less than 0.25 UI peak-peak. If not, the stress may be more than desired, leading to conservative results. However, compensation is not allowed. Once done, revert to the calibration pattern, if different than the specified test pattern.

   Any remaining vertical eye closure required has to be created with sinusoidal interference or sinusoidal jitter.

   To emulate the effects of DCD or data-dependent jitter, at least 0.05 but no more than 0.15 UI peak-peak of pulse shrinkage jitter should have been achieved. This imposes a limit of less than 1.2 dB of vertical closure from sinusoidal interference, applied after vertical closure created by filtering.

   The frequency of the sinusoidal interference may be set at any frequency between B / 100 and B / 5 where B is the signaling speed, although care should be taken to avoid a harmonic relationship between the sinusoidal interference, the sinusoidal jitter, the signaling speed and the pattern repetition rate.
   Sinusoidal jitter (phase modulation) has to be added according to the appropriate jitter specification. For calibration purposes, sinusoidal jitter frequencies should be well within the flat portion of the template above the corner frequency.

   Iterate the filter bandwidth and the settings for sinusoidal interference and/or jitter until all constraints are met, including jitter (J), vertical eye closure penalty (VECP), and that sinusoidal jitter above the corner frequency is as specified.

   Verify that the optical power penalty for the stressed eye (relative to the reference transmitter per 58.7.9.1) is greater than or equal to VECP.
f) Decrease the amplitude with the optical attenuator until the OMA complies with the OMA values specified for the receiver under test.
g) For testing, turn on the actual required test pattern(s).

Care should be taken when characterizing the signal used to make receiver tolerance measurements. In the case of a transmit jitter measurement, excessive and/or uncalibrated noise/jitter in the test system makes it more difficult to meet the specification and may have a negative effect on yield but will not impact interoperability. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. Care should be taken to minimize and/or correct for the noise/jitter

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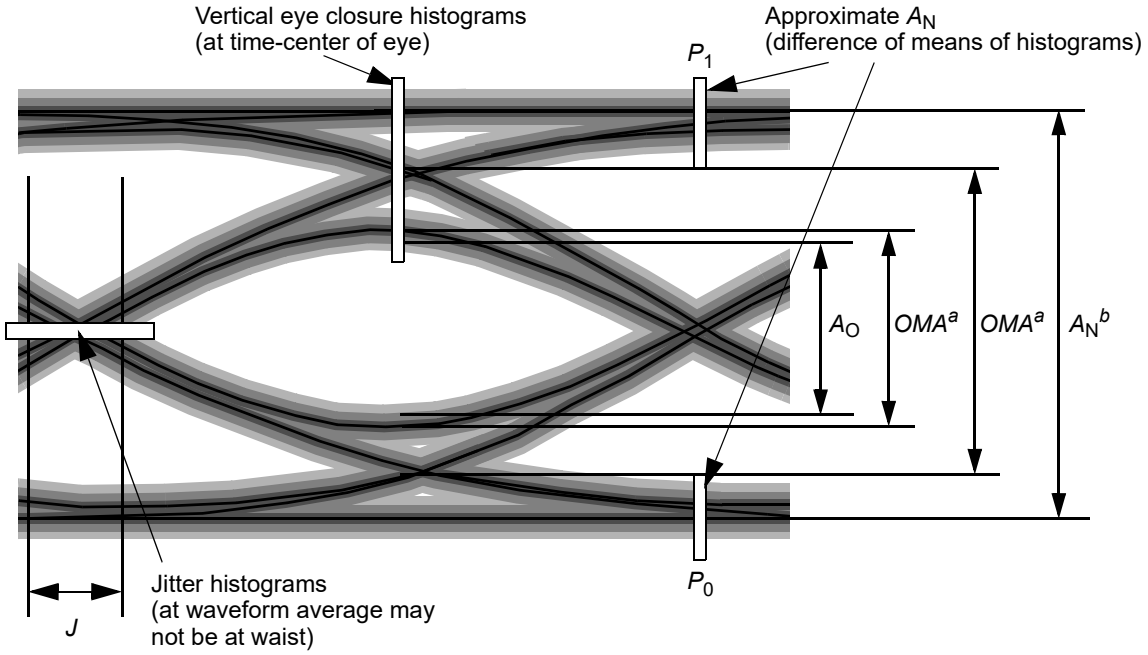

[a]This measure of OMA on the eye of the conformance test signal differs between 100BASE-X, 1000BASE-X and 10GBASE-R/W.
[b]This is also OMA for 10GBASE-R/W.

Figure 58–9—Required characteristics of the conformance test signal at TP3

introduced by the reference receiver, filters, oscilloscope, and BERT. While the details of measurement and test equipment are beyond the scope of this standard it is recommended that the implementers fully characterize their test equipment and apply appropriate guard bands to ensure that the receive input signal meets the specified requirements.

58.7.11.3 Stressed receiver conformance test procedure

The test apparatus is set up as described in 58.7.11.1 and 58.7.11.2. The sinusoidal jitter is then stepped across the specified frequency and amplitude range while monitoring errors at the receiver. The BER is to be compliant at all jitter frequencies in the specified frequency range. This method does not result in values for jitter contributed by the receiver. It does, however, ensure that a receiver meeting the requirements of this test will operate with the worst-case optical input.

58.7.11.4 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. Sinusoidal jitter may vary over a magnitude range as required to accurately calibrate a stressed eye per 58.7.11.2. The range is limited by the constraints of Table 58–12 as illustrated in Figure 58–10, where *f2*, *SJ1,* and *SJ2* are specified in the appropriate receiver table: Table 58–4, Table 58–6, Table 59–6, Table 59–8, Table 60–5, Table 60–6, or Table 60–14. The frequency *f2* is specified as “Jitter corner frequency” in the receiver tables. *SJ1* and *SJ2* are defined as “sinusoidal jitter limits for stressed receiver conformance test (min, max)” in e.g., Table 58–4.

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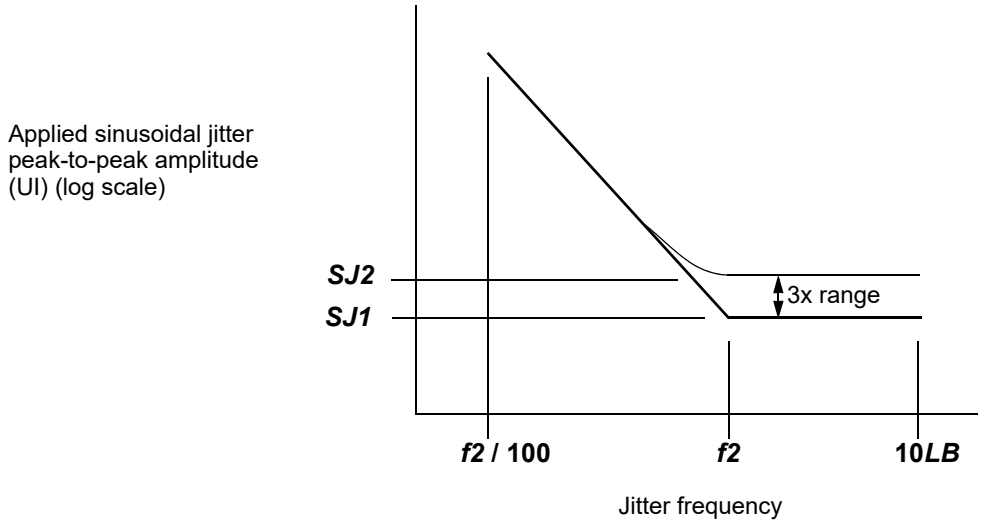

Figure 58–10—Illustration of the mask of the sinusoidal component of jitter tolerance

Table 58–12—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter (UI pk-pk)
$f < f2 / 100$	N/A
$f2 / 100 < f \leq f2$	$0.05 \times f2 / f + S - 0.05$[a]
$f2 < f < 10 \times LB$[b]	$SJ1 \leq S \leq SJ2$[a]

[a]S is the magnitude of sine jitter actually used in the calibration of the stressed eye per the methods of 58.7.11.2.
[b]LB = Loop Bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

58.7.12 Jitter measurements

Jitter measurements are informatively described in 58B.4.

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58.8 Environmental, safety, and labeling

58.8.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

58.8.2 Laser safety

100BASE-LX10 and 100BASE-BX10 optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore. Conformance to additional laser safety standards may be required for operation within specific geographical regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation shall explicitly define requirements and usage restrictions on the host system necessary to meet these safety certifications.

58.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

58.8.4 Environment

Two optional temperature ranges are defined in Table 58–13. Implementations shall be declared as compliant over one or both complete ranges, or not so declared (compliant over parts of these ranges or another temperature range).

Table 58–13—Component case temperature classes

Class	Low temperature (°C)	High temperature (°C)
Warm extended	–5	+85
Cool extended	–40	+60
Universal extended	–40	+85

Reference Annex 67A for additional environmental information.

58.8.5 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 100BASE-BX10-U).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 58.8.2.

Compliant systems and field pluggable components shall be clearly labeled with the operating temperature range over which their compliance is ensured.

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58.9 Characteristics of the fiber optic cabling

The 100BASE-LX10 and 100BASE-BX10 fiber optic cabling shall meet the dispersion specifications of IEC 60793-2 and ITU-T G.652, or the requirements of Table 58–14 where they differ. The fiber cable attenuation is for information only; the end-to-end channel loss shall meet the requirements of Table 58–1. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. The fiber optic cabling spans from one MDI to another MDI, as shown in Figure 58–11.

58.9.1 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 58–11.

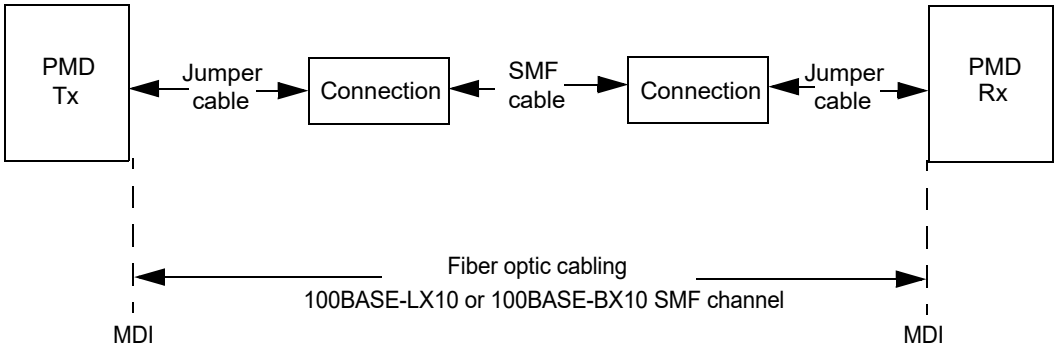

Figure 58–11—Fiber optic cabling model

The maximum channel insertion losses shall meet the requirements specified in Table 58–1. The minimum loss for 100BASE-LX10 and 100BASE-BX10 is zero. A channel may contain additional connectors or other optical elements as long as the optical characteristics of the channel, such as attenuation, dispersion and reflections, meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

NOTE—In extreme cases with minimum length links (less than 2 m), care may be taken to avoid excess optical power delivered through cladding modes to the receiver.

58.9.2 Optical fiber and cable

The fiber optic cable requirements are satisfied by the fibers specified in IEC 60793-2, Types B1.1 (dispersion un-shifted single-mode) and B1.3 (low water peak single-mode) and ITU-T G.652, or by the requirements of Table 58–14 where they differ.

Table 58–14—Optical fiber and cable characteristics

Description[a]	B1.1, B1.3 SMF		Unit
Nominal fiber specification wavelength[b]	1310	1550	nm
Cabled optical fiber attenuation (max)[c]	0.4	0.35	dB/km
Zero dispersion wavelength (λ_0)[d]	$1300 \le \lambda_0 \le 1324$		nm
Dispersion slope (max) (S_0)	0.093		ps/nm^2km

[a]The fiber dispersion values are normative, all other values in the table are optional.
[b]Wavelength specified is the nominal fiber specification wavelength which is the typical measurement wavelength. Power penalties at other wavelengths are accounted for.
[c]Attenuation values are not mandatory requirements. Attenuation for single-mode optical fiber cables is defined in ITU-T G.652.
[d]See IEC 60793 or G.652 for correct use of zero dispersion wavelength and dispersion slope.

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58.9.3 Optical fiber connection

The maximum link distances for single-mode fiber are calculated based on an allocation of 2 dB total connection and splice loss. Connections with different loss characteristics may be used provided the requirements of Table 58–1 are met.

The maximum discrete reflectance of e.g., a connection or splice shall be less than –26 dB.

58.9.4 Medium Dependent Interface (MDI)

The 100BASE-LX10, 100BASE-BX10-D or 100BASE-BX10-U PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 58–11). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

The MDI carries the signal in both directions. For 100BASE-BX10 it couples a single fiber and for 100BASE-LX10 it couples dual fibers.

When the MDI is a remateable connection it shall meet the interface performance specifications of IEC 61753-1.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 58.2.1, not at the MDI.

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58.10 Protocol implementation conformance statement (PICS) proforma for Clause 58, Physical Medium Dependent (PMD) sublayer and medium, type 100BASE-LX10 (Long Wavelength) and 100BASE-BX10 (Bi-Directional Long Wavelength)[112]

58.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 58, Physical Medium Dependent (PMD) sublayer and medium, type 100BASE-LX10 and 100BASE-BX10, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

58.10.2 Identification

58.10.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

58.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 58, Physical Medium Dependent (PMD) sublayer and medium, type 100BASE-LX10 and 100BASE-BX10
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[112]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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58.10.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
HT	High temperature operation	58.8.4	–5 °C to 85 °C	O	Yes [ ] No [ ]
LT	Low temperature operation	58.8.4	–40 °C to 60 °C	O	Yes [ ] No [ ]
*LX	100BASE-LX10 PMD	58.3	Device supports long wavelength (1310 nm) over dual single-mode fiber operation	O/1	Yes [ ] No [ ]
*BD	100BASE-BX10-D	58.4	Device operates with one single single-mode fiber and transmits at downstream wavelength (1550 nm)	O/1	Yes [ ] No [ ]
*BU	100BASE-BX10-U	58.4	Device operates with one single single-mode fiber and transmits at upstream wavelength (1310 nm)	O/1	Yes [ ] No [ ]
*INS	Installation / Cable	58.9	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]

58.10.3 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 100BASE-LX10 and 100BASE-BX10

58.10.3.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FN1	Transmit function	58.2.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FN2	Transmitter optical signal	58.2.2	Higher optical power transmitted is a logic 1	O	Yes [ ] No [ ]
FN3	Receive function	58.2.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FN4	Receiver optical signal	58.2.3	Higher optical power received is a logic 1	O	Yes [ ] No [ ]
FN5	Signal detect function	58.2.4	Mapping to PMD service interface	M	Yes [ ]
FN6	Signal detect behavior	58.2.4	Generated according to Table 58–2	M	Yes [ ]

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58.10.3.2 PMD to MDI optical specifications for 100BASE-LX10

Item	Feature	Subclause	Value/Comment	Status	Support
LX1	100BASE-LX10 transmitter	58.3.1	Meets specifications in Table 58–3	LX:M	Yes [ ] N/A [ ]
LX2	100BASE-LX10 receiver	58.3.2	Meets specifications in Table 58–4	LX:M	Yes [ ] N/A [ ]
LX3	100BASE-LX10 stressed receiver sensitivity	58.3.2	Meets specification in Table 58–4	LX:O	Yes [ ] No [ ] N/A [ ]

58.10.3.3 PMD to MDI optical specifications for 100BASE-BX10-D

Item	Feature	Subclause	Value/Comment	Status	Support
BD1	100BASE-BX10 transmitter	58.4.1	Meets specifications in Table 58–5	BD:M	Yes [ ] N/A [ ]
BD2	100BASE-BX10 receiver	58.4.2	Meets specifications in Table 58–6	BD:M	Yes [ ] N/A [ ]
BD3	100BASE-BX10 stressed receiver sensitivity	58.4.2	Meets specification in Table 58–6	BD:O	Yes [ ] No [ ] N/A [ ]

58.10.3.4 PMD to MDI optical specifications for 100BASE-BX10-U

Item	Feature	Subclause	Value/Comment	Status	Support
BU1	100BASE-BX10 transmitter	58.4.1	Meets specifications in Table 58–5	BU:M	Yes [ ] N/A [ ]
BU2	100BASE-BX10 receiver	58.4.2	Meets specifications in Table 58–6	BU:M	Yes [ ] N/A [ ]
BU3	100BASE-BX10 stressed receiver sensitivity	58.4.2	Meets specification in Table 58–6	BU:O	Yes [ ] No [ ] N/A [ ]

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58.10.3.5 Optical measurement requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	58.7	2 m to 5 m in length	M	Yes [ ]
OM2	Test pattern	58.7.1, 58.7.8, 58.7.10	For eye, sensitivity, TDP, stressed sensitivity, jitter	M	Yes [ ]
OM3	Wavelength and spectral width	58.7.2	Per the centroidal wavelength and RMS spectral width definitions in IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM4	Average optical power	58.7.3	Per IEC 61280-1-1	M	Yes [ ]
OM5	Extinction ratio	58.7.4	Per IEC 61280-2-2	M	Yes [ ]
OM6	Transmit eye	58.7.8	Per 58.7.8 with specified test pattern	M	Yes [ ]
OM7	Receiver sensitivity	58.7.10	With specified pattern	M	Yes [ ]
OM8	Transmitter and dispersion penalty	58.7.9	With dispersion, reflection and decision timing offsets	M	Yes [ ]
OM9	Stressed receiver conformance test	58.7.11	According to 58.7.11.1, 58.7.11.2, and 58.7.11.3	O	Yes [ ] No [ ]

58.10.3.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	58.8.1	Conforms to J.2	M	Yes [ ]
ES2	Laser safety —IEC Hazard Level 1	58.8.2	Conform to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Documentation	58.8.2	Explicitly defines requirements and usage restrictions to meet safety certifications	M	Yes [ ]
ES4	Operating temperature range labeling	58.8.5	If required	M	Yes [ ] N/A [ ]

58.10.3.7 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
FO1	Fiber optic cabling	58.9	Dispersion specifications of Table 58–14	INS:M	Yes [ ] N/A [ ]
FO2	End-to-end channel loss	58.1, 58.9	Meet the requirements of Table 58–1	INS:M	Yes [ ] N/A [ ]
FO3	Maximum discrete reflectance	58.9.3	Less than –26 dB	INS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
FO4	MDI requirements	58.9.4	IEC 61753-1 if remateable	INS:O	Yes [ ] No [ ] N/A [ ]

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59. Physical Medium Dependent (PMD) sublayer and medium, type 1000BASE-LX10 (Long Wavelength) and 1000BASE-BX10 (Bi-Directional Long Wavelength)

59.1 Overview

The 1000BASE-LX10 and 1000BASE-BX10 PMD sublayers provide point-to-point (P2P) 1000BASE-X links over a pair of fibers or a single fiber, respectively, up to 10 km.

This clause specifies the 1000BASE-LX10 PMD for both single-mode and multimode fiber, and the 1000BASE-BX10 PMD for single-mode fiber. A PMD is connected to the 1000BASE-X PMA of 66.2, and to the medium through the MDI. A PMD is optionally combined with the management functions that may be accessible through the management interface defined in Clause 22 or by other means.

Table 59–1 shows the primary attributes of each PMD type.

Table 59–1—Classification of 1000BASE-LX10 and 1000BASE-BX10 PMDs

Description	1000BASE-LX10		1000BASE-BX10-D	1000BASE-BX10-U	Unit
Fiber type[a]	B1.1, B1.3 SMF	50, 62.5 µm MMF	B1.1, B1.3 SMF		
Number of fibers	2	2	1		
Typical transmit direction	N/A		Downstream	Upstream	
Nominal transmit wavelength	1310	1310	1490	1310	nm
Minimum range	0.5 m to 10 km	0.5 m to 550 m[b]	0.5 m to 10 km		
Maximum channel insertion loss[c]	6.0	2.4	5.5	6.0	dB

[a]Per IEC 60793-2.
[b]See Table 59–14 for fiber and cable characteristics.
[c]At the nominal operating wavelength.

A 1000BASE-LX10 link uses 1000BASE-LX10 PMDs at each end while a 1000BASE-BX10 link uses a 1000BASE-BX10-D PMD at one end and a 1000BASE-BX10-U PMD at the other. Typically the 1490 nm band is used to transmit away from the center of the network (“downstream”) and the 1310 nm band towards the center (“upstream”), although this arrangement, or the notion of hierarchy, is not required. The suffixes “D” and “U” indicate the PMDs at each end of a link that transmit in these directions and receive in the opposite directions.

1000BASE-LX10 is interoperable with 1000BASE-LX (see Clause 38). If used on single-mode fiber, operation is not ensured by this standard beyond the reach given in Table 38–6.

Two optional temperature ranges are defined; see 59.8.4 for further details. Implementations may be declared as compliant over one or both complete ranges, or not so declared (compliant over parts of these ranges or another temperature range).

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59.1.1 Goals and objectives

The following are the objectives of 1000BASE-LX10 and 1000BASE-BX10:

a) Point-to-point on optical fiber
b) 1000BASE-LX extended temperature range optics
c) 1000BASE-X up to 10km over SM fiber
d) BER better than or equal to 10^{-12} at the PHY service interface

59.1.2 Positioning of 1000BASE-LX10 and 1000BASE-BX10 PMDs within the IEEE 802.3 architecture

Figure 59–1 depicts the relationships of the PMD (shown shaded) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

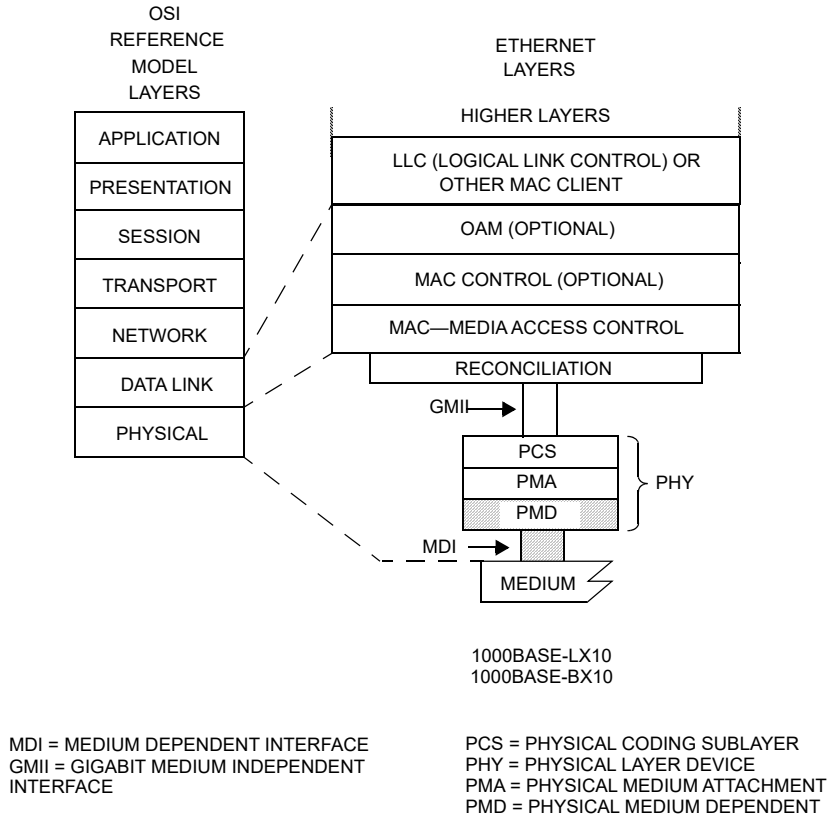

Figure 59–1—1000BASE-LX10 and 1000BASE-BX10 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

59.1.3 Terminology and conventions

The following list contains references to terminology and conventions used in this clause:

Basic terminology and conventions, see 1.1 and 1.2.

Normative references, see 1.3.

Definitions, see 1.4.

Abbreviations, see 1.5.

Informative references, see Annex A.

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Introduction to 1000 Mb/s baseband networks, see Clause 34.

Introduction to Ethernet for subscriber access networks, see Clause 56.

59.1.4 Physical Medium Dependent (PMD) sublayer service interface

The following specifies the services provided by the 1000BASE-LX10 and 1000BASE-BX10 PMDs. These PMD sublayers are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded 8B/10B code-groups between the PMA and PMD entities. The PMD translates the serialized data of the PMA to and from signals suitable for the specified medium.

The following primitives are defined:

PMD_UNITDATA.request

PMD_UNITDATA.indication

PMD_SIGNAL.indication

59.1.5 Delay constraints

Delay requirements from the MDI to the GMII which include the PMD layer are specified in Clause 36. Of the budget, up to 20 ns is allocated for each of the transmit and receive functions of the PMD to account for those cases where the PMD includes a pigtail.

59.1.5.1 PMD_UNITDATA.request

This primitive defines the transfer of a serial data stream from the PMA to the PMD.

The semantics of the service primitive are PMD_UNITDATA.request(tx_bit). The data conveyed by PMD_UNITDATA.request is a continuous stream of bits where the tx_bit parameter can take one of two values: ONE or ZERO. The PMA continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal 1.25 GBd signaling speed. Upon receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals at the MDI.

59.1.5.2 PMD_UNITDATA.indication

This primitive defines the transfer of data from the PMD to the PMA.

The semantics of the service primitive are PMD_UNITDATA.indication(rx_bit). The data conveyed by PMD_UNITDATA.indication is a continuous stream of bits where the rx_bit parameter can take one of two values: ONE or ZERO. The PMD continuously sends a stream of bits to the PMA corresponding to the signals received from the MDI.

59.1.5.3 PMD_SIGNAL.indication

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

The semantics of the service primitive are PMD_SIGNAL.indication(SIGNAL_DETECT). The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting light at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication(rx_bit) is undefined. The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT.

SIGNAL_DETECT = OK does not guarantee that PMD_UNITDATA.indication(rx_bit) is known good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the specified bit error ratio.

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59.2 PMD functional specifications

The 1000BASE-X PMDs perform the transmit and receive functions that convey data between the PMD service interface and the MDI.

59.2.1 PMD block diagram

The PMD sublayer is defined at the four reference points shown in Figure 59–2. Two points, TP2 and TP3, are compliance points. TP1 and TP4 are reference points for use by implementers. The optical transmit signal is defined at the output end of a patch cord (TP2), between 2 m and 5 m in length, of a fiber type consistent with the link type connected to the transmitter. If a single-mode fiber offset-launch mode-conditioning patch cord is used, the optical transmit signal is defined at the end of this single-mode fiber offset-launch mode-conditioning patch cord at TP2. Unless specified otherwise, all transmitter measurements and tests defined in 59.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) connected to the receiver. Unless specified otherwise, all receiver measurements and tests defined in 59.7 are made at TP3.

The electrical specifications of the PMD service interface (TP1 and TP4) are not system compliance points (these are not readily testable in a system implementation). It is expected that in many implementations, TP1 and TP4 will be common between 1000BASE-X PMD types.

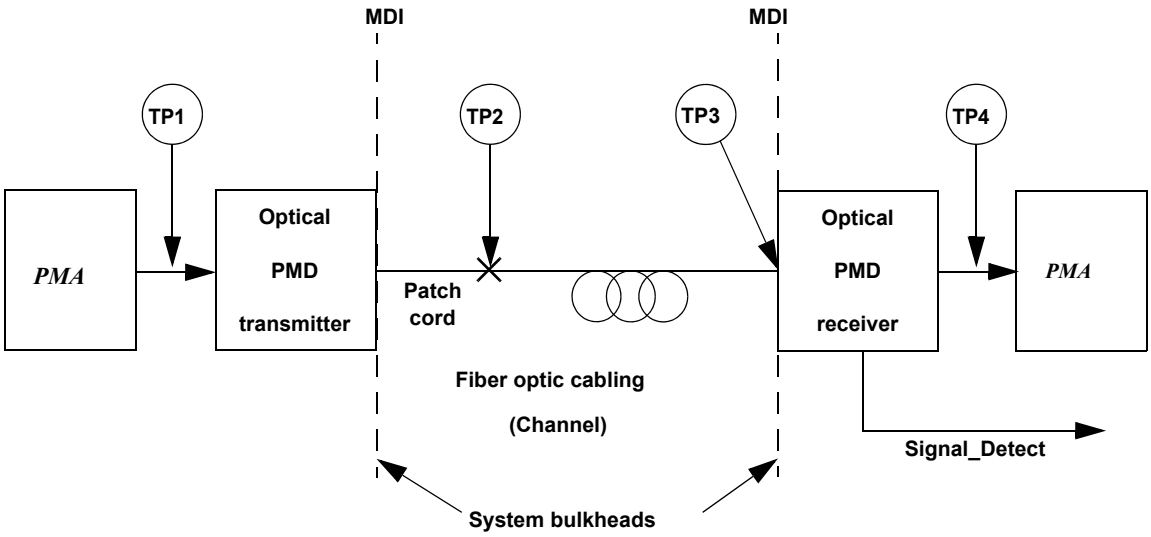

Figure 59–2—1000BASE-X block diagram

59.2.2 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the optical specifications in this clause. The higher optical power level shall correspond to tx_bit =ONE.

59.2.3 PMD receive function

The PMD receive function shall convey the bits received from the MDI according to the optical specifications in this clause to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). The higher optical power level shall correspond to rx_bit =ONE.

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59.2.4 PMD signal detect function

The PMD signal detect function shall report to the PMD service interface using the message PMD_SIGNAL.indication(SIGNAL DETECT) which is signaled continuously. PMD_SIGNAL.indication is intended to be an indicator of optical signal presence.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 59–2. The PMD receiver is not required to verify whether a compliant 1000BASE-X signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD due to cross talk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations which generate the SIGNAL_DETECT parameter values in response to the amplitude of the 8B/10B modulation of the optical signal and implementations which respond to the average optical power of the 8B/10B modulated optical signal.

Table 59–2—1000BASE-LX10 and 1000BASE-BX10 SIGNAL_DETECT value definition

Receive conditions		Signal_detect value
1000BASE-LX10	**1000BASE-BX10**	
Average input optical power ≤ signal detect threshold (min) in Table 59–5	Average input optical power ≤ signal detect threshold (min) in Table 59–7	FAIL
Average input optical power ≥ receiver sensitivity (max) in Table 59–5 with a compliant 1000BASE-LX or 1000BASE-LX10 signal input	Average input optical power ≥ receiver sensitivity (max) in Table 59–7 with a compliant 1000BASE-BX10 signal input at the specified receiver wavelength	OK
All other conditions		Unspecified

59.3 PMD to MDI optical specifications for 1000BASE-LX10

The operating range for 1000BASE-LX10 is defined in Table 59–1. A 1000BASE-LX10 compliant transceiver operates over the media types listed in Table 59–1 according to the specifications described in 59.9. A transceiver that exceeds the operational range requirement while meeting all other optical specifications is considered compliant.

NOTE—In this subclause and Table 59–5, the specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is explained in 58.7.6.

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59.3.1 Transmitter optical specifications

The 1000BASE-LX10 transmitter's signaling speed, operating wavelength, spectral width, average launch power, extinction ratio, return loss tolerance, OMA, eye and TDP shall meet the specifications defined in Table 59–3 per measurement techniques described in 59.7. Its $RIN_{12}OMA$ should meet the value listed in Table 59–3 per measurement techniques described in 58.7.7. To ensure that the specifications of Table 59–3 are met with MMF links, the 1000BASE-LX10 transmitter output shall be coupled through a single-mode fiber offset-launch mode-conditioning patch cord, as defined in 59.9.5.The maximum RMS spectral width vs. center wavelength for 1000BASE-LX10 is shown in Table 59–4 and Figure 59–3. The equation used to generate these values is included in 59.7.2. The values in bold are normative, the others optional.

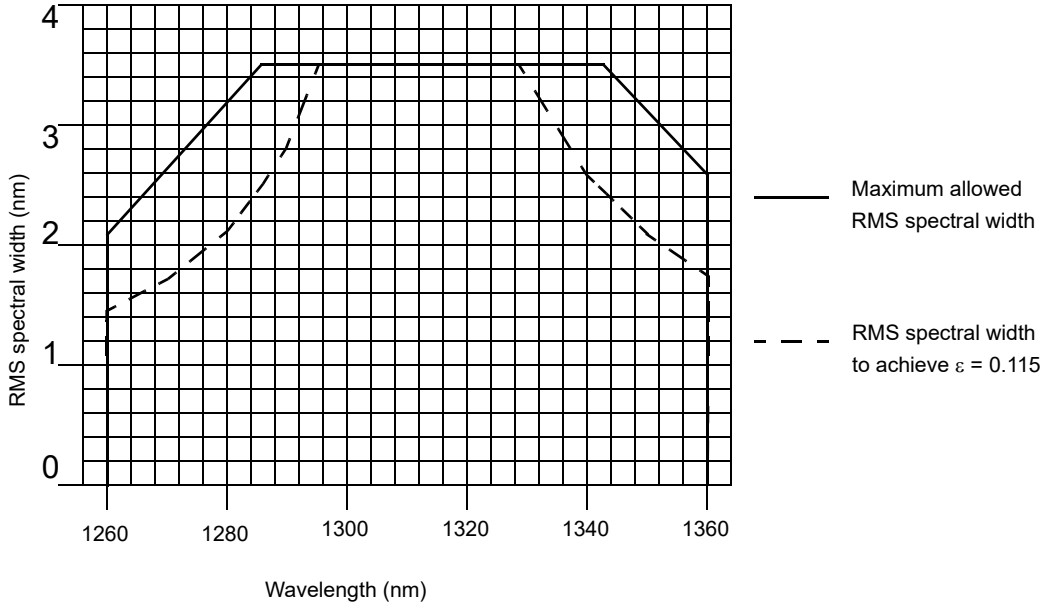

Figure 59–3—1000BASE-LX-10 Transmitter spectral limits

Table 59–3—1000BASE-LX10 transmit characteristics

Description	SMF	50 µm MMF	62.5 µm MMF	Unit
Nominal transmitter type[a]	Longwave Laser			
Signaling speed (range)	1.25 ± 100 ppm			GBd
Operating wavelength range[b]	1260 to 1360			nm
T rise /T fall (max, 20–80% response time)	0.30			ns
RMS spectral width (max)	See Table 59–4			nm
Average launch power (max)	–3			dBm
Average launch power (min)	–9	–11.0	–11.0	dBm
Average launch power of OFF transmitter (max)	–45			dBm
Extinction ratio (min)	6			dB
$RIN_{12}OMA$ (max)	–113			dB/Hz
Optical return loss tolerance (max)	12			dB
Launch OMA (min)	–8.7 (130)	–10.2 (100)	–10.2 (100)	dBm (µW)
Transmitter eye mask definition {X1, X2, Y1, Y2, Y3}	0.22, 0.375, 0.20, 0.20, 0.30			UI

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Table 59–3—1000BASE-LX10 transmit characteristics *(continued)*

Description	SMF	50 µm MMF	62.5 µm MMF	Unit
Decision timing offsets for transmitter and dispersion penalty (min)	±80			ps
Transmitter reflectance (max)	–6			dB
Transmitter and dispersion penalty, TDP (max)	3.3	3.5		dB
Differential delay, reference receiver for TDP (min)[c]	NA	367		ps

[a]The nominal device type is not intended to be a requirement on the source type, and any device meeting the transmitter characteristics specified may be substituted for the nominal device type.
[b]The great majority of the transmitted spectrum has to fall within the operating wavelength range. The allowable range of central wavelengths is narrower than the operating wavelength range by the actual RMS spectral width at each extreme.
[c]Delay is calculated as Td = L/(3.BWf) where BWf is defined to –3 dB (optical). 1000BASE-LX is rated for 550 m of 500 MHz.km fiber while 1000BASE-LX also covered 550 m of 400 MHz.km fiber, but this is now seen as a historical bandwidth requirement.

Table 59–4—1000BASE-LX10 and 1000BASE-BX10 transmitter spectral limits

Center wavelength	RMS spectral width (max)[a]	RMS spectral width to achieve ε ≤0.115 (optional)
nm	**nm**	**nm**
1260	**2.09**	1.43
1270	**2.52**	1.72
1280	**3.13**	2.14
1286	**3.50**	2.49
1290		2.80
1297		3.50
1329		
1340		2.59
1343		2.41
1350	**3.06**	2.09
1360	**2.58**	1.76
1480 to 1500	**0.88**	0.60

[a]These limits for the 1000BASE-LX10 transmitter are illustrated in Figure 59–3. Limits at intermediate wavelengths may be found by interpolation.

59.3.2 Receiver optical specifications

The 1000BASE-LX10 receiver's signaling speed, operating wavelength, damage, overload, sensitivity, stressed receive characteristics, reflectance, and signal detect shall meet the specifications defined in Table 59–5 per measurement techniques defined in 59.7.

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Table 59–5—1000BASE-LX10 receive characteristics

Description	Value	Unit
Signaling speed (range)	1.25 ± 100 ppm	GBd
Wavelength (range)	1260 to 1360	nm
Average receive power (max)	–3	dBm
Receive sensitivity (max)	–19.5	dBm
Receiver sensitivity as OMA (max)	–18.7 (13.4)	dBm (μW)
Bit error ratio (max)	10^{-12}	
Receiver reflectance (max)[a]	–12	dB
Stressed receive sensitivity (max)	–15.4	dBm
Stressed receiver sensitivity as OMA (max)	–14.6 (35)	dBm (μW)
Vertical eye-closure penalty (min)	3.6	dB
Receive electrical 3 dB upper cutoff frequency (max)	1500	MHz
Signal detect threshold (min)	–45	dBm
Stressed eye jitter (min)[b]	0.3	UI pk-pk
Jitter corner frequency	637	kHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)	0.05, 0.15	UI

[a]See 1.4 for definition of reflectance.
[b]Vertical eye closure penalty and jitter specifications are test conditions for measuring stressed receiver sensitivity. They are not required characteristics of the receiver.

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59.4 PMD to MDI optical specifications for 1000BASE-BX10-D and 1000BASE-BX10-U

The operating range for 1000BASE-BX10-D and 1000BASE-BX10-U is defined in Table 59–1. A 1000BASE-BX10 compliant transceiver operates over all single-mode fibers listed in Table 59–1. A transceiver that exceeds the operational range requirement while meeting all other optical specifications is considered compliant.

NOTE—In this subclause and 59.3, the specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is explained in 58.7.6.

59.4.1 Transmit optical specifications

The 1000BASE-BX10-D and 1000BASE-BX10-U transmitter's signaling speed, operating wavelength, spectral width, average launch power, extinction ratio, return loss tolerance, OMA, eye and TDP shall meet the specifications defined in Table 59–6 per measurement techniques described in 59.7. Its $RIN_{12}OMA$ should meet the value listed in Table 59–6 per measurement techniques described in 59.7.7.

Table 59–6—1000BASE-BX10-D and 1000BASE-BX10-U transmit characteristics

Description	1000BASE-BX10-D	1000BASE-BX10-U	Unit
Nominal transmitter type[a]	Longwave Laser		
Signaling speed (range)	1.25 ± 100 ppm		GBd
Operating wavelength range[b]	1480 to 1500	1260 to 1360	nm
RMS spectral width (max)	See Table 59–4		nm
Average launch power (max)	–3		dBm
Average launch power (min)	–9		dBm
Average launch power of OFF transmitter (max)	–45		dBm
Extinction ratio (min)	6		dB
$RIN_{12}OMA$ (max)	–113		dB/Hz
Optical return loss tolerance (max)	12		dB
Launch OMA	–8.2 (151)		dBm (μW)
Transmitter eye mask definition {X1, X2, Y1, Y2, Y3}	0.22, 0.375, 0.20, 0.20, 0.30		UI
Transmitter reflectance (max)	–10	–6	dB
Transmitter and dispersion penalty, TDP (max)	3.3		dB
Decision timing offsets for transmitter and dispersion penalty (min)	± 80		ps

[a]The nominal device type is not intended to be a requirement on the source type, and any device meeting the transmitter characteristics specified may be substituted for the nominal device type.

[b]The great majority of the transmitted spectrum has to fall within the operating wavelength range. The allowable range of central wavelengths is narrower than the operating wavelength range by the actual RMS spectral width at each extreme.

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59.4.2 Receiver optical specifications

The 1000BASE-BX10-D and 1000BASE-BX10-U receiver's signaling speed, operating wavelength, damage, overload, sensitivity, reflectance and signal detect shall meet the specifications defined in Table 59–7 per measurement techniques defined in 59.7. Its stressed receive characteristics should meet the values listed in Table 59–7 per measurement techniques described in 59.7.11.

Table 59–7—1000BASE-BX10-D and 1000BASE-BX10-U receive characteristics

Description	1000BASE-BX10-D	1000BASE-BX10-U	Unit
Signaling speed (range)	1.25 ± 100 ppm		GBd
Wavelength (range)	1260 to 1360	1480 to 1500	nm
Bit error ratio (max)	10^{-12}		
Average receive power (max)	–3		dBm
Receive sensitivity (max)	–19.5		dBm
Receiver sensitivity as OMA (max)	–18.7 (13.4)		dBm (μW)
Receiver reflectance (max)	–12		dB
Stressed receive sensitivity (max)[a]	–15.4		dBm
Stressed receiver sensitivity as OMA (max)	–14.6 (35)		dBm (μW)
Vertical eye-closure penalty (min)[b]	2.6		dB
Receive electrical 3 dB upper cutoff frequency (max)	1500		MHz
Signal detect threshold (min)	–45		dBm
Stressed eye jitter (min)	0.3		UI pk-pk
Jitter corner frequency	637		kHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)	0.05, 0.15		UI

[a]The stressed receiver sensitivity is optional.
[b]Vertical eye closure penalty and jitter specifications are test conditions for measuring stressed receiver sensitivity. They are not required characteristics of the receiver.

59.5 Illustrative 1000BASE-LX10 and 1000BASE-BX10 channels and penalties

The illustrative channel and penalties for 1000BASE-LX10 and 1000BASE-BX10 PMDs are shown in Table 59–8.

NOTE—The budgets include an allowance for –12 dB reflection at the receiver.

59.6 Jitter specifications

Informative jitter specifications are described in 59A.1.

59.7 Optical measurement requirements

All optical measurements, except TDP and RIN, shall be made through a short patch cable, between 2 m and 5 m in length.

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Table 59–8—Illustrative 1000BASE-LX10 and 1000BASE-BX10 channel and penalties

PMD type	1000BASE-LX10		1000BASE-BX10-D	1000BASE-BX10-U	Unit
Fiber type	B1.1, B1.3 SMF	50µm, 62.5µm MMF	B1.1, B1.3 SMF		
Measurement wavelength for fiber	1310	1300	1550	1310	nm
Nominal distance	10	0.55	10		km
Available power budget	10.5	8.5	10.5		dB
Maximum channel insertion loss[a]	6.0	2.4	5.5	6.0	dB
Allocation for penalties[b]	4.5	6.1	5.0	4.5	dB

[a]The maximum channel insertion loss is based on the cable attenuation at the target distance and nominal measurement wavelength. The channel insertion loss also includes the loss for connectors, splices and other passive components.

[b]The allocation for penalties is the difference between the available power budget and the channel insertion loss; insertion loss difference between nominal and worst-case operating wavelength is considered a penalty.

The following sections describe definitive patterns and test procedures for certain PMDs of this standard. implementers using alternative verification methods need to ensure adequate correlation and allow adequate margin such that specifications are met by reference to the definitive methods.

59.7.1 Test patterns

The frame-based test patterns defined here are suitable for testing all Clause 59 and Clause 60 PMDs. Further information on frame-based testing in included in Annex 58A. The test suite and the patterns are shown in Table 59–9.

Table 59–9—List of test patterns and tests

Test pattern	Tests	Related subclauses
Any valid 8B/10B encoded signal	Eye mask Optical power Central wavelength Spectral width	59.7.8 59.7.3 59.7.2 59.7.2
Idles	Extinction ratio $RIN_{12}OMA$ OMA	59.7.4 59.7.7
Random pattern test frame	Receiver sensitivity Stressed receiver sensitivity Receiver 3dB upper cutoff frequency TDP	59.7.11 59.7.14 59.7.15 59.7.10
Jitter pattern test frame	All jitter tests	59.7.12

The following test patterns are intended for frame-based testing of the 1000BASE-X PMDs of Clause 59 and Clause 60. They are compliant Ethernet packets with adequate user defined fields to allow them to be routed through a system to the point of the test. The common portions of the frames are given in Table 59–10.

NOTE—Users are advised to take care that the system under test is not connected to a network in service.

Two payloads are defined. The first, which emulates a random pattern with broad spectral content and minimal peaking, is shown in Table 59–11.

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Table 59–10—Common portion of frame-based test pattern

Field	Number of octets	Hexadecimal	8B/10B encoded binary[a]	
			Starting disparity +	Starting disparity–
SPD (/S/)	1	N/A[b]	N/A[c]	110110 1000
Remainder of preamble	6	55	N/A[c]	101010 0101
SFD	1	D5	N/A[c]	101010 0110
Destination address	6	User defined	User defined	User defined
Source address	6	User defined	User defined	User defined
Length/Type	2	User defined	User defined	User defined
First portion of MAC client data	32	User defined	User defined	User defined
Second portion of MAC client data	456	See Table 59–11 or Table 59–12	See Table 59–11 or Table 59–12	See Table 59–11 or Table 59–12
Frame check sequence[d]	4	As required by frame	As required by frame	As required by frame
EPD (/T/R/)[e]	2	N/A[b]	010001 0111 000101 0111	101110 1000 111010 1000
Idle (/I1/ or /I2/)[e]	2	N/A[b]	110000 0101 101001 0110	001111 1010 100100 0101
Idle (/I2/)[e]	10	N/A[b]	N/A[f]	001111 1010 100100 0101

[a]The binary bits are transmitted left most bit first.
[b]The SPD, EPD, and Idle code-groups are generated by the PCS and their hexadecimal octet values have no meaning without relation to the signals transmitted across the GMII.
[c]Except when operating in a half-duplex mode, it is not possible to transmit an SPD with a positive starting disparity. The first code-group that could begin with a positive running disparity would be the second octet of the destination address.
[d]The frame check sequence may be calculated using the method described in 3.2.9.
[e]The first row precedes the second row.
[f]The first idle code-group following the frame will be an /I1/ if the running disparity is positive and an /I2/ if the running disparity is negative. All subsequent idle code-groups will be /I2/.

Table 59–11—Payload for random pattern test frame

Number of octets	Hexadecimal	8B/10B encoded binary	
		Starting disparity +	Starting disparity –
Repeat 19 times for 228 bytes	BE	100001 1010	011110 1010
	D7	111010 0110	000101 0110
	23	110001 1001	110001 1001
	47	000111 0101	111000 0101
	6B	110100 0011	110100 1100
	8F	101000 1101	010111 0010
	B3	110010 1010	110010 1010
	14	001011 0100	001011 1011
	5E	011110 0101	100001 0101
	FB	001001 1110	110110 0001
	35	101010 1001	101010 1001
	59	100110 0101	100110 0101

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Table 59–11—Payload for random pattern test frame *(continued)*

Number of octets	Hexadecimal	8B/10B encoded binary	
		Starting disparity +	Starting disparity –
Transmit once for 12 bytes	BC	001110 1010	001110 1010
	D7	000101 0110	111010 0110
	23	110001 1001	110001 1001
	47	111000 0101	000111 0101
	6B	110100 1100	110100 0011
	8F	010111 0010	101000 1101
	B3	110010 1010	110010 1010
	14	001011 1011	001011 0100
	5E	100001 0101	011110 0101
	FB	110110 0001	001001 1110
	35	101010 1001	101010 1001
	59	100110 0101	100110 0101
Repeat 18 times for 216 bytes	BE	011110 1010	100001 1010
	D7	000101 0110	111010 0110
	23	110001 1001	110001 1001
	47	111000 0101	000111 0101
	6B	110100 1100	110100 0011
	8F	010111 0010	101000 1101
	B3	110010 1010	110010 1010
	14	001011 1011	001011 0100
	5E	100001 0101	011110 0101
	FB	110110 0001	001001 1110
	35	101010 1001	101010 1001
	59	100110 0101	100110 0101

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The payload for the second pattern is shown in Table 59–12.

Table 59–12—Payload for jitter test frame

Field	Hexadecimal	8B/10B encoded binary	
		Starting disparity +	Starting disparity –
Low Transition Density, Repeat 96 times for 192 bytes	7E	100001 1100	011110 0011
	7E	011110 0011	100001 1100
Phase Jump, Repeat one time for 8 bytes	F4	001011 0001	001011 0111
	EB	110100 1110	110100 1000
	F4	001011 0001	001011 0111
	EB	110100 1110	110100 1000
	F4	001011 0001	001011 0111
	EB	110100 1110	110100 1000
	F4	001011 0001	001011 0111
	AB	110100 1010	110100 1010
High Transition Density, Repeat 20 times for 20 bytes	B5	101010 1010	101010 1010
Phase Jump, Repeat 4 times for 8 bytes	EB	110100 1110	110100 1000
	F4	001011 0001	001011 0111
Low Transition Density, Repeat 96 times for 192 bytes	7E	011110 0011	100001 1100
	7E	100001 1100	011110 0011
Phase Jump, Repeat one time for 8 bytes	F4	001011 0111	001011 0001
	EB	110100 1000	110100 1110
	F4	001011 0111	001011 0001
	EB	110100 1000	110100 1110
	F4	001011 0111	001011 0001
	EB	110100 1000	110100 1110
	F4	001011 0111	001011 0001
	AB	110100 1010	110100 1010
High Transition Density, Repeat 20 times for 20 bytes	B5	101010 1010	101010 1010
Phase Jump, Repeat 4 times for 8 bytes	EB	110100 1000	110100 1110
	F4	001011 0111	001011 0001

This pattern has areas of high and low transition density to aggravate jitter susceptibility.

Frames are separated by a near minimum interpacket gap (IPG) of 14 octets.

59.7.2 Wavelength and spectral width measurements

The wavelength and spectral width (RMS) shall meet the specifications according to the centroidal wavelength and RMS spectral width definitions in IEC 61280-1-3, under modulated conditions using a valid 1000BASE-X signal.

NOTE 1—The great majority of the transmitted spectrum has to fall within the operating range. The allowable range of central wavelengths is narrower than the operating wavelength range by the actual RMS spectral width at each extreme.

NOTE 2—The 20 dB width for SLM lasers is taken as 6.07 times the RMS width.

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The interaction between the transmitter and the chromatic dispersion of the fiber is accounted for by a parameter ε (epsilon), which is defined as the product of 10^{-3} times the signaling speed (in GBd) times the path dispersion (in ps/nm) times the RMS spectral width (in nm).

$$\varepsilon = \text{dispersion} \times \text{length} \times \text{RMS spectral width} \times \text{signaling speed} \times 10^{-3} \quad (0–1)$$

A maximum ε close to 0.168 is imposed by column 2 of Table 59–5. If the spectral width is kept below the limits of column 3, ε will not exceed 0.115, and the chromatic dispersion penalty is expected to be below 2 dB. The chromatic dispersion penalty is a component of transmitter and dispersion penalty (TDP) which is specified in Table 59–3, Table 59–6 and described in 58.7.9.

59.7.3 Optical power measurements

Optical power shall meet specifications according to the methods specified in ANSI/TIA/EIA-455-95. A measurement may be made with the port transmitting any valid encoded 8B/10B data stream.

59.7.4 Extinction ratio measurements

Extinction ratio shall meet specifications according to IEC 61280-2-2 with the port transmitting a repeating idle pattern /I2/ ordered set (see 36.2.4.12) that may be interspersed with OAM packets per 57A.2, and with minimal back reflections into the transmitter, lower than –20 dB. The /I2/ ordered set is defined in Clause 36, and is coded as /K28.5/D16.2/, which is binary 001111 1010 100100 0101 within idles. The extinction ratio is expected to be similar for other valid 8B/10B bit streams. The test receiver has the frequency response as specified for the transmitter optical waveform measurement.

59.7.5 OMA measurements (optional)

58.7.5 provides a reference technique for performing OMA measurements.

59.7.6 OMA relationship to extinction ratio and power measurements

Annex 58B provides information on how OMA, extinction ratio, and mean power, are related to each other (see 58B.2).

59.7.7 Relative intensity noise optical modulation amplitude ($RIN_{12}OMA$)

$RIN_{12}OMA$ is the ratio of noise to modulated optical signal in the presence of a back reflection. The measurement procedure is described in 58.7.7.

59.7.8 Transmitter optical waveform (transmit eye)

The required transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 59–4.

The measurement procedure is described in 58.7.8 and references therein.

The eye shall comply to the mask of the eye using a fourth-order Bessel-Thomson receiver response with f_r= 0.9375 GHz, and where the relative response vs. relative frequency is defined in ITU-T G.957, Table B.2 (STM-16 values), along with the allowed tolerances for its physical implementation.

NOTE 1—This Bessel-Thomson filter is not intended to represent the noise filter used within an optical receiver, but is intended to provide uniform measurement conditions on the transmitter.

NOTE 2—The fourth-order Bessel-Thomson filter is reactive. In order to suppress reflections, a 6 dB attenuator may be required at the filter input and/or output.

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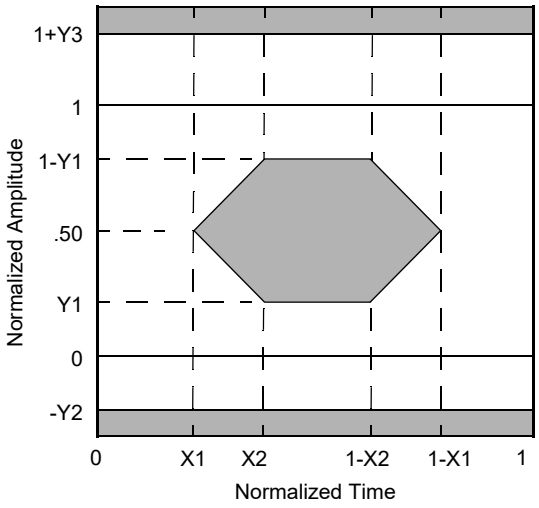

Figure 59–4—Transmitter eye mask definition

59.7.9 Transmit rise/fall characteristics

Optical response time specifications are based on unfiltered waveforms. Some lasers have overshoot and ringing on the optical waveforms, which, if unfiltered, reduce the accuracy of the 20–80% response times. For the purpose of standardizing the measurement method, measured waveforms shall conform to the mask defined in 59.7.8. If a filter is needed to conform to the mask, the filter response should be removed using Equation (0–2):

$$T_{\text{rise, fall}} = \sqrt{(T_{\text{rise, fall, measured}})^2 - (T_{\text{rise, fall, filter}})^2} \quad (0–2)$$

where the filter may be different for rise and fall. Any filter should have an impulse response equivalent to a fourth-order Bessel-Thomson filter. The fourth-order Bessel-Thomson filter describe in 59.7.8 may be a convenient filter for this measurement, however its low bandwidth adversely impacts the accuracy of the rise and fall time measurements.

59.7.10 Transmitter and dispersion penalty (TDP)

This measurement tests for transmitter impairments with modal (not chromatic) dispersion effects for a transmitter to be used with multimode fiber, and for transmitter impairments with chromatic effects for a transmitter to be used with single-mode fiber. Possible causes of impairment include intersymbol interference, jitter, RIN and mode partition noise. Meeting the separate requirements (e.g., eye mask, spectral characteristics) does not in itself guarantee the transmitter and dispersion penalty (TDP). The TDP limit shall be met. See 59.7.9 for details of the measurement.

59.7.11 Receive sensitivity measurements

Receiver sensitivity is defined for the random pattern test frame (see 59.7.1) and an ideal input signal quality with the specified extinction ratio. The measurement procedure is described in 58.7.10. The sensitivity shall be met for the bit error ratio defined in Table 59–5 or Table 59–7 as appropriate. Stressed sensitivity is described in 59.7.14 and 58.7.11.

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59.7.12 Total jitter measurements

Total jitter measurements are informatively described in 59A.2.

59.7.13 Deterministic or high probability jitter measurement

Deterministic or high probability jitter measurement is informatively described in 59A.3.

59.7.14 Stressed receiver conformance test

The stressed receiver conformance test is intended to screen against receivers with poor frequency response or timing characteristics which could cause errors when combined with a distorted but compliant signal at TP3. Modal (MMF) or chromatic (SMF) dispersion can cause distortion. The conformance test signal uses the random pattern test frame and is conditioned by applying deterministic jitter and intersymbol interference. If the option for stressed receiver compliance is chosen, the receiver shall meet the specified bit error ratio at the power level and signal quality defined in Table 59–5 and Table 59–7 as appropriate, according to the measurement procedures of 58.7.11.

59.7.15 Measurement of the receiver 3 dB electrical upper cutoff frequency

The receiver 3 dB electrical upper cutoff frequency shall meet specifications according to the methods specified below. The test setup is shown in Figure 59–5. The test is performed with a laser that is suitable for analog signal transmission. The laser is modulated by a digital data signal. In addition to the digital modulation, the laser is modulated with an analog signal. The analog and digital signals should be asynchronous. The data pattern to be used for this test is the random pattern test frame defined in 59.7.1. The frequency response of the laser needs to be sufficient to allow it to respond to both the digital modulation and the analog modulation. The laser should be biased so that it remains linear when driven by the combined signals. Alternatively the two signals may be combined in the optical domain.

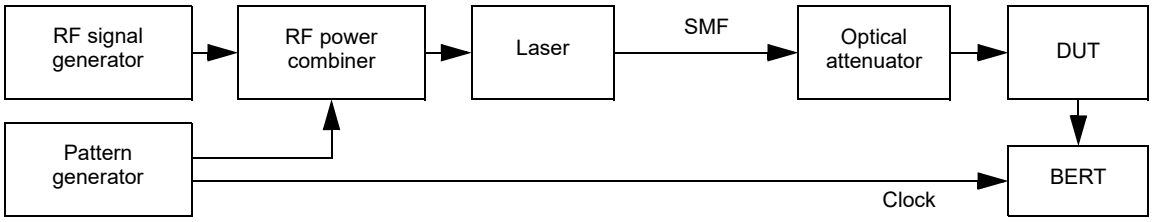

Figure 59–5—Test setup for receiver bandwidth measurement

The 3 dB upper cutoff frequency is measured using the following steps a) through e):

a) Calibrate the frequency response characteristics of the test equipment including the analog radio frequency (RF) signal generator, RF power combiner, and laser source. Measure the laser's extinction ratio according to 59.7.4. With the exception of extinction ratio, the optical source shall meet the requirements of Clause 59.
b) Configure the test equipment as shown in Figure 59–5. Take care to minimize changes to the signal path that could affect the system frequency response after the calibration in step a. Connect the laser output with no RF modulation applied to the receiver under test through an optical attenuator and taking into account the extinction ratio of the source, set the optical power to a level that approximates the stressed receive sensitivity level in Table 59–5 for 1000BASE-LX10 and in Table 59–7 for 1000BASE-BX10.
c) Locate the center of the eye with the BERT. Turn on the RF modulation while maintaining the same average optical power established in step b).

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d) Measure the necessary RF modulation amplitude (in dBm) required to achieve a constant BER (e.g., 10^{-8}) for a number of frequencies.
e) The receiver 3 dB electrical upper cutoff frequency is that frequency where the corrected RF modulation amplitude (the measured amplitude in step d) corrected with the calibration data in step a) increases by 3 dB (electrical). If necessary, interpolate between the measured response values.

59.8 Environmental, safety, and labeling specifications

59.8.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

59.8.2 Laser safety

1000BASE-BX10 and 1000BASE-LX10 optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore. Conformance to additional laser safety standards may be required for operation within specific geographical regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance and service. This documentation shall explicitly define requirements and usage restrictions on the host system necessary to meet these safety certifications.

59.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulations, be followed in every instance in which such practices are applicable.

59.8.4 Environment

Reference Annex 67A for additional environmental information.

Two optional temperature ranges are defined in Table 59–13. Implementations shall be declared as compliant over one or both complete ranges, or not so declared (compliant over parts of these ranges or another temperature range).

Table 59–13—Component case temperature classes

Class	Low temperature (°C)	High temperature (°C)
Warm extended	–5	+85
Cool extended	–40	+60
Universal extended	–40	+85

59.8.5 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 1000BASE-BX10-U).

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Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 59.8.2.

Compliant systems and field pluggable components shall be clearly labeled with the operating temperature range over which their compliance is ensured.

59.9 Characteristics of the fiber optic cabling

The 1000BASE-BX10 and 1000BASE-LX10 fiber optic cabling shall meet the dispersion and modal bandwidth specifications defined in IEC 60793-2 and ITU-T G.652, or the requirements of Table 59–14 where they differ. The fiber cable attenuation is shown for information only; the end-to-end channel loss shall meet the requirements of Table 59–1. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. The fiber optic cabling spans from one MDI to another MDI, as shown in Figure 59–6.

59.9.1 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 59–6.

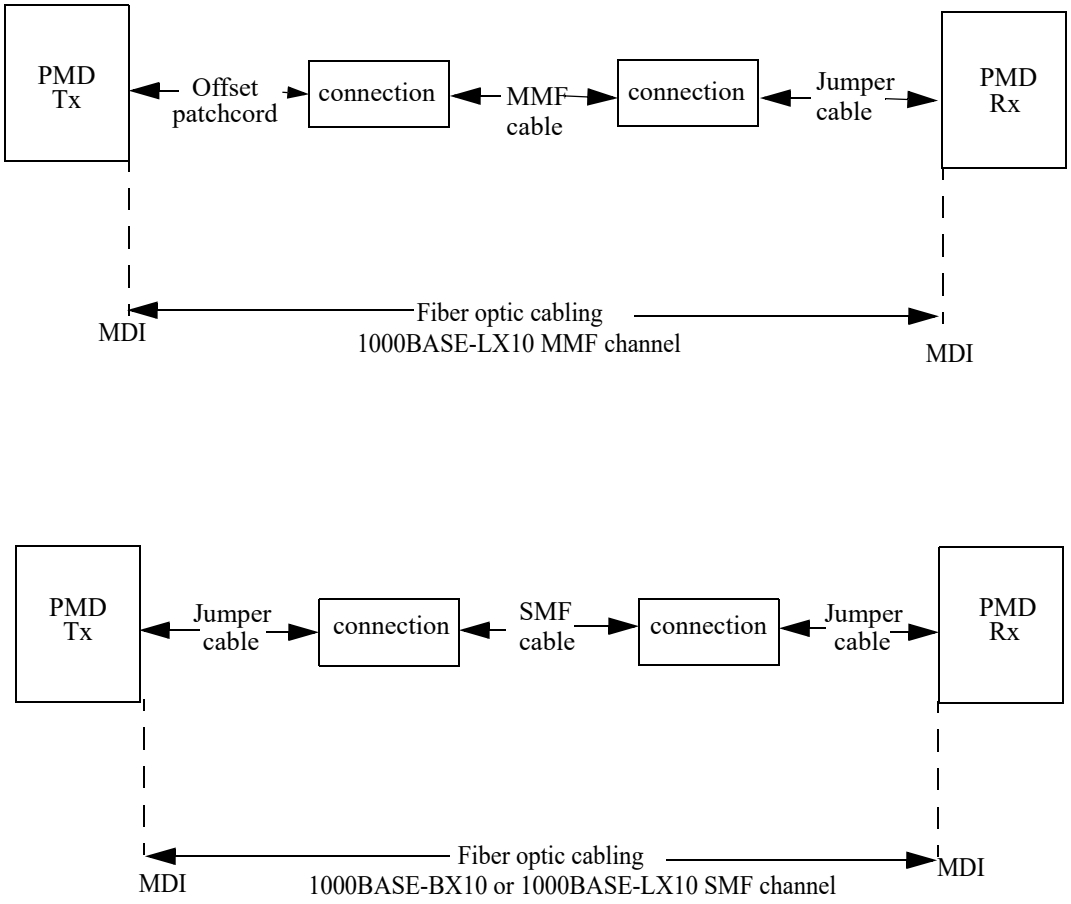

Figure 59–6—Fiber optic cable model

The maximum channel insertion loss shall meet the requirements specified in Table 59–1. The minimum loss for 1000BASE-BX10 and 100BASE-LX10 is zero. A channel may contain additional connectors or

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other optical elements as long as the optical characteristics of the channel, such as attenuation, dispersion and reflections, meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1 one-cord method for multimode cabling and IEC 61280-4-2 one-cord reference method for single-mode cabling. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

59.9.2 Optical fiber and cable

The fiber optic cable requirements are satisfied by the fibers specified in IEC 60793-2 Type B1.1 (dispersion un-shifted single-mode fiber) and Type B1.3 (low water peak single-mode fiber) and ITU-T G.652, or by the requirements of Table 59–14 where they differ.

Table 59–14—Optical fiber and cable characteristics

Description[a]	B1.1, B1.3 SMF		50 µm MMF	62.5 µm MMF	Unit
Nominal fiber specification wavelength[b]	1310	1550	1300		nm
Cabled optical fiber attenuation (max)[c]	0.4	0.35	1.5		dB/km
Modal Bandwidth (min; overfilled launch)	N/A		500[d]		MHz· km
Zero dispersion wavelength[e]	$1300 \le \lambda_0 \le 1324$		$1295 \le \lambda_0 \le 1320$	$1320 \le \lambda_0 \le 1365$	nm
Dispersion slope (max)	0.093		0.11 for $1300 \le \lambda_0 \le 1320$ and $0.001(\lambda_0\text{-}1190)$ for $1295 \le \lambda_0 \le 1300$	0.11 for $1320 \le \lambda_0 \le 1348$ and $0.001(1458\text{-}\lambda_0)$ for $1348 \le \lambda_0 \le 1365$	ps /nm^2 · km

[a]The fiber dispersion values are normative, all other values in the table are optional.
[b]The wavelength specified is the nominal fiber specification wavelength which is the typical measurement wavelength. Power penalties at other wavelengths are accounted for.
[c]Attenuation values are optional. Attenuation for single-mode optical fiber cables is defined in ITU-T G.652 and for multimode fiber cables is defined in ISO/IEC 11801.
[d]1000BASE-LX10 is rated for 550 m of 500 MHz·km fiber, while 1000BASE-LX also covered 550 m of 400 MHz·km, but this now seen as a historical bandwidth requirement.
[e]See IEC 60793 or G.652 for correct use of zero dispersion wavelength and dispersion slope.

59.9.3 Optical fiber connection

The maximum link distances for multimode fiber are calculated based on the allocation of 1.5 dB total connection and splice loss. Connections with different loss characteristics may be used provided the requirements of Table 59–1 are met.

The maximum link distances for single-mode fiber are calculated based on the allocation of 2 dB total connection and splice loss for 1000BASE-LX10 and 1000BASE-BX10. Connections with different loss characteristics may be used provided the requirements of Table 59–1 are met.

The maximum discrete reflectance for multimode connections shall be less than –20 dB.

The maximum discrete reflectance for single-mode connections shall be less than –26 dB.

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59.9.4 Medium Dependent Interface (MDI)

The 1000BASE-LX10 or 1000BASE-BX10 PMD is coupled to the fiber cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" as shown in Figure 59–6. Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a remateable connection, it shall meet the interface performance specifications of IEC 61753-1. The MDI carries the signal in both directions. For 1000BASE-BX10 it couples a single fiber and for 1000BASE-LX10 it couples dual fibers.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 59.2.1, not at the MDI.

59.9.5 Single-mode fiber offset-launch mode-conditioning patch cord for MMF operation of 1000BASE-LX10

This subclause specifies an example embodiment of a mode conditioner for 1000BASE-LX10 operation with MMF cabling. The mode conditioner consists of a single-mode fiber permanently coupled off-center to a graded index fiber. This example embodiment of a patch cord is not intended to exclude other physical implementations of offset-launch mode conditioners. However, any implementation of an offset-launch mode conditioner used for 1000BASE-LX10 shall meet the specifications of Table 59–15. The offset launch shall be contained within the patch cord assembly and is not adjustable by the user.

NOTE—The single-mode fiber offset-launch mode-conditioning patch cord described in Clause 38 may be used, although its labeling and coloring requirements are not mandatory here. See 38.11.4.

Table 59–15—Single-mode fiber offset-launch mode conditioner specifications

Description	62.5 μm MMF	50 μm MMF	Unit
Maximum insertion loss	0.5	0.5	dB
Coupled power ratio (CPR)	28 < CPR < 40	12 < CPR < 20	dB
Optical center offset between SMF and MMF	17 < Offset < 23	10 < Offset < 16	μm
Maximum angular offset	1	1	degree

Patch cord connectors and ferrules for the single-mode-to-multimode offset launch shall have single-mode tolerances, float, and other mechanical requirements according to IEC 61754-1.

The single-mode fiber used in the construction of the single-mode fiber offset-launch mode conditioner shall meet the requirements of 59.9.2. The multimode fiber used in the construction of the single-mode fiber offset-launch mode conditioner shall be of the same type as the cabling over which the 1000BASE-LX10 link is to be operated. If the cabling is 62.5 μm MMF then the MMF used in the construction of the mode conditioner is of type 62.5 μm MMF. If the cabling is 50 μm MMF, then the MMF used in the construction of the mode conditioner is of type 50 μm MMF.

Figure 59–7 shows an example of an embodiment of the single-mode fiber offset-launch mode-conditioning patch cord. This patch cord consists of duplex fibers including a single-mode-to-multimode offset launch fiber connected to the transmitter MDI and a second conventional graded index MMF connected to the receiver MDI. The preferred configuration is a plug-to-plug patch cord since it maximizes the power budget margin of the 1000BASE-LX10 link. The single-mode end of the patch cord is labeled "To Equipment". The multimode end of the patch cord is labeled "To Cable". The recommended color identifier of the single-mode fiber connector is blue. The recommended color identifier of all multimode fiber connector plugs is

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beige. The patch cord assembly is labeled “Offset-launch mode-conditioning patch cord assembly”. Labeling identifies which size multimode fiber is used in the construction of the patch cord. The keying of this duplex optical plug ensures that the single-mode fiber end is automatically aligned to the transmitter MDI.

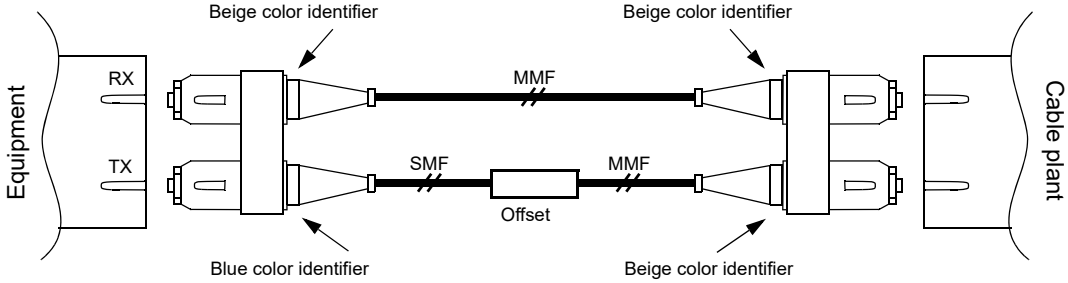

Figure 59–7—1000BASE-LX10 single-mode fiber offset-launch mode-conditioning patch cord assembly

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59.10 Protocol implementation conformance statement (PICS) proforma for Clause 59, Physical Medium Dependent (PMD) sublayer and medium, type 1000BASE-LX10 (Long Wavelength) and 1000BASE-BX10 (Bi-Directional Long Wavelength)[113]

59.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 59, Physical Medium Dependent (PMD) sublayer and medium, type 1000BASE-LX10 and type 1000BASE-LX10, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

59.10.2 Identification

59.10.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

59.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 59, Physical Medium Dependent (PMD) sublayer and medium, type 1000BASE-LX10 and 1000BASE-BX10
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[113] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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59.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
HT	High temperature operation	59.8.4	–5 to 85°C	O	Yes [ ] No [ ]
LT	Low temperature operation	59.8.4	–40 to 60°C	O	Yes [ ] No [ ]
*LX	1000BASE-LX10 PMD	59.3	Device supports long wavelength (1310 nm) over dual multimode and single-mode fibers.	O/1	Yes [ ] No [ ]
*BXD	1000BASE-BX10-D PMD	Table 59–6	Device operates with one single single-mode fiber and transmits at downstream wavelength (1490 nm).	O/1	Yes [ ] No [ ]
*BXU	1000BASE-BX10-U PMD	Table 59–6	Device operates with one single single-mode fiber and transmits upstream wavelength (1310 nm).	O/1	Yes [ ] No [ ]
*INS	Installation / cable	59.9	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]
*OFP	Single-mode offset-launch mode-conditioning patch cord	59.9.5	Items marked with OFP include installation practices and cable specifications not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]

59.10.3.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FN1	Transmit function	59.2.2	Convey bits requested by PMD_UNITDATA.request() to the MDI.	M	Yes [ ]
FN2	Transmitter optical signal	59.2.2	Higher optical power is a logical 1.	M	Yes [ ]
FN3	Receive function	59.2.3	Convey bits received from the MDI to PMD_UNITDATA.indication().	M	Yes [ ]
FN4	Receiver optical signal	59.2.3	Higher optical power is a logical 1.	M	Yes [ ]
FN5	Signal detect function	59.2.4	Mapping to PMD interface.	M	Yes [ ]
FN6	Signal detect behavior	59.2.4	Generated according to Table 59–2.	M	Yes [ ]

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59.10.3.2 PMD to MDI optical specifications for 1000BASE-LX10

Item	Feature	Subclause	Value/Comment	Status	Support
LX1	1000BASE-LX10 transmitter	59.3.1	Transmitter meets specifications in Table 59–3.	LX:M	Yes [ ] N/A [ ]
LX2	Offset-launch mode-conditioning patch cord	59.3.1	Required for LX10 multimode operation.	OFP:M	Yes [ ] N/A [ ]
LX3	1000BASE-LX10 receiver	59.3.2	Receiver meets mandatory specifications in Table 59–5.	LX:M	Yes [ ] N/A [ ]
LX4	1000BASE-LX10 stressed receiver sensitivity	59.3.2	Receiver meets mandatory specifications in Table 59–5.	LX:M	Yes [ ] N/A [ ]

59.10.3.3 PMD to MDI optical specifications for 1000BASE-BX10-D

Item	Feature	Subclause	Value/Comment	Status	Support
BXD1	1000BASE-BX10-D transmitter	59.4.1	Transmitter meets specifications in Table 59–6.	BXD:M	Yes [ ] N/A [ ]
BXD2	1000BASE-BX10-D receiver	59.4.2	Receiver meets mandatory specifications in Table 59–7.	BXD:M	Yes [ ] N/A [ ]
BXD3	1000BASE-BX10-D stressed receiver sensitivity	59.4.2	Receiver meets specifications in Table 59–7.	BXD:O	Yes [ ] No [ ] N/A [ ]

59.10.3.4 PMD to MDI optical specifications for 1000BASE-BX10-U

Item	Feature	Subclause	Value/Comment	Status	Support
BXU1	1000BASE-BX10-U transmitter	59.4.1	Transmitter meets specifications in Table 59–6.	BXU:M	Yes [ ] N/A [ ]
BXU2	1000BASE-BX10-U receiver	59.4.2	Receiver meets mandatory specifications in Table 59–7.	BXU:M	Yes [ ] N/A [ ]
BXU3	1000BASE-BX10-U stressed receiver sensitivity	59.4.2	Receiver meets specifications in Table 59–7.	BXU:O	Yes [ ] No [ ] N/A [ ]

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59.10.3.5 Optical Measurement requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable		2 m to 5 m in length.	M	Yes [ ]
OM2	Test patterns	59.7.1	See Table 59–9.	M	Yes [ ]
OM3	Wavelength and spectral width	59.7.2	Per the centroidal wavelength and RMS spectral width definitions in IEC 61280-1-3 under modulated conditions.	M	Yes [ ]
OM4	Average optical power	59.7.3	Per ANSI/TIA/EIA-455-95.	M	Yes [ ]
OM5	Extinction ratio	59.7.4	Per IEC 61280-2-2 with minimal back reflections and fourth-order Bessel-Thomson receiver.	M	Yes [ ]
OM6	$RIN_{12}OMA$	58.7.7	As described in 58.7.7.	M	Yes [ ]
OM7	Transmit optical waveform (transmit eye)	59.7.8	Per ANSI/TIA/EIA-526-4A with test pattern and fourth-order Bessel-Thomson receiver.	M	Yes [ ]
OM8	Transmit rise/fall characteristics	59.7.9	Waveforms conform to mask in Figure 59–4, measure from 20% to 80%, using patch cable per 59.7.	LX:M	Yes [ ]
OM9	Transmitter and dispersion penalty	59.7.10	As described in 58.7.9.	M	Yes [ ]
OM10	Receive sensitivity	59.7.11	With specified pattern.	M	Yes [ ]
*OM11	Stressed receiver conformance	59.7.14	As described in 59.7.14.	O	Yes [ ] N/A[ ]
OM12	Receiver 3dB electrical upper cutoff frequency	59.7.15	As described in 59.7.15.	M	Yes [ ]

59.10.3.6 Environmental, safety, and labeling specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	59.8.1	Conforms to J.2.	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	59.8.2	Conform to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2.	M	Yes [ ]
ES3	Documentation	59.8.2	Explicitly define requirements and usage restrictions to meet safety certifications.	M	Yes [ ]
ES4	Operating temperature range labeling	59.8.5	If required, label range over which compliance is ensured.	M	Yes [ ] N/A[ ]

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59.10.3.7 Characteristics of the fiber optic cabling

Item	Feature	Subclause	Value/Comment	Status	Support
FO1	Fiber optic cabling	59.9	Meets specifications in Table 59–14.	INS:M	Yes [ ] N/A [ ]
FO2	End-to-end channel loss	59.9.1	Meet the requirements specified in Table 59–1.	INS:M	Yes [ ] N/A [ ]
FO3	Maximum discrete reflectance for multimode connections	59.9.3	Less than –20 dB.	INS:M	Yes [ ] N/A [ ]
FO4	Maximum discrete reflectance for single-mode connections	59.9.3	Less than –26 dB.	INS:M	Yes [ ] N/A [ ]
FO5	MDI requirements	59.9.4	Meet the interface performance specifications of IEC 61753-1, if remateable.	INS:O	Yes [ ] No[ ] N/A [ ]

59.10.3.8 Offset-launch mode-conditioning patch cord

Item	Feature	Subclause	Value/Comment	Status	Support
LPC1	Offset-launch mode-conditioning patch cord	59.9.5	Meet conditions of 59.9.5.	OFP:M	Yes [ ] N/A [ ]
LPC2	Single-mode mechanics in offset-launch mode-conditioning patch cords	59.9.5	IEC 61754-1:1997 [B33] grade 1 ferrule.	OFP:M	Yes [ ] N/A [ ]
LPC3	Single-mode fiber in offset-launch mode-conditioning patch cords	59.9.5	Per 59.9.5.	OFP:M	Yes [ ] N/A [ ]
LPC4	Multimode fiber in offset-launch mode-conditioning patch cords	59.9.5	Same type as used in cable plant.	OFP:M	Yes [ ] N/A [ ]

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60. Physical Medium Dependent (PMD) sublayer and medium, type 1000BASE-PX (long wavelength passive optical networks)

60.1 Overview

The 1000BASE-PX10, 1000BASE-PX20, 1000BASE-PX30, and 1000BASE-PX40 PMD sublayers provide point-to-multipoint (P2MP) 1000BASE-X connections over passive optical networks (PONs). The 1000BASE-PX10 PMD sublayers support a reach of at least 10 km whereas the 1000BASE-PX20, 1000BASE-PX30, and 1000BASE-PX40 PMD sublayers support a reach of at least 20 km. The 1000BASE-PX10 and 1000BASE-PX20 PMD sublayers support a typical split ratio of 1:16. The 1000BASE-PX30 PMD sublayers support a typical split ratio of 1:32. The 1000BASE-PX40 PMD sublayers support a typical split ratio of 1:64. In an Ethernet PON, a single downstream (D) PMD broadcasts to multiple upstream (U) PMDs and receives bursts from each "U" PMD over a single branched topology, single-mode fiber network. The same fibers are used simultaneously in both directions. This clause specifies a single-mode fiber medium and the following PMDs (including MDI): 1000BASE-PX10-D, 1000BASE-PX10-U, 1000BASE-PX20-D, 1000BASE-PX20-U, 1000BASE-PX30-D, 1000BASE-PX30-U, 1000BASE-PX40-D, and 1000BASE-PX40-U. A 1000BASE-PX-U PMD or a 1000BASE-PX-D PMD is connected to the appropriate 1000BASE-X PMA of Clause 65, and to the medium through the MDI. A PMD is optionally combined with the management functions that may be accessible through the management interface defined in Clause 22 or by other means.

A 1000BASE-PX10 link uses a 1000BASE-PX10-U PMD at one end and a 1000BASE-PX10-D PMD at the other. A 1000BASE-PX20 link uses a 1000BASE-PX20-U PMD at one end and a 1000BASE-PX20-D PMD at the other. A 1000BASE-PX30 link uses a 1000BASE-PX30-U PMD at one end and a 1000BASE-PX30-D PMD at the other. A 1000BASE-PX40 link uses a 1000BASE-PX40-U PMD at one end and a 1000BASE-PX40-D PMD at the other. A 1000BASE-PX20-D PMD is interoperable with a 1000BASE-PX10-U PMD. This allows certain upgrade possibilities from 10 km to 20 km PONs.

Two optional temperature ranges are defined; see 60.10.4 for further details. Implementations may be declared as compliant over one or both complete ranges, or not so declared (compliant over parts of these ranges or another temperature range).

Table 60–1 shows the primary attributes of each PMD type.

60.1.1 Goals and objectives

All 1000BASE-PX PMDs share the objectives of:

a) Point-to-multipoint on optical fiber.
b) BER better than or equal to 10^{-12} at the PHY service interface.
c) 1000 Mb/s on one single-mode fiber.

1000BASE-PX10 has an objective of operating at the distance of at least of 10 km and at a split ratio of at least of 1:16. 1000BASE-PX20 has an objective of operating at the distance of at least of 20 km and at a split ratio of at least of 1:16. 1000BASE-PX30 has an objective of operating at the distance of at least of 20 km and at a split ratio of at least of 1:32. 1000BASE-PX40 has an objective of operating at the distance of at least of 20 km and at a split ratio of at least of 1:64.

60.1.2 Positioning of this PMD set within the IEEE 802.3 architecture

Figure 60–1 depicts the relationships of the PMD (shown shaded) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

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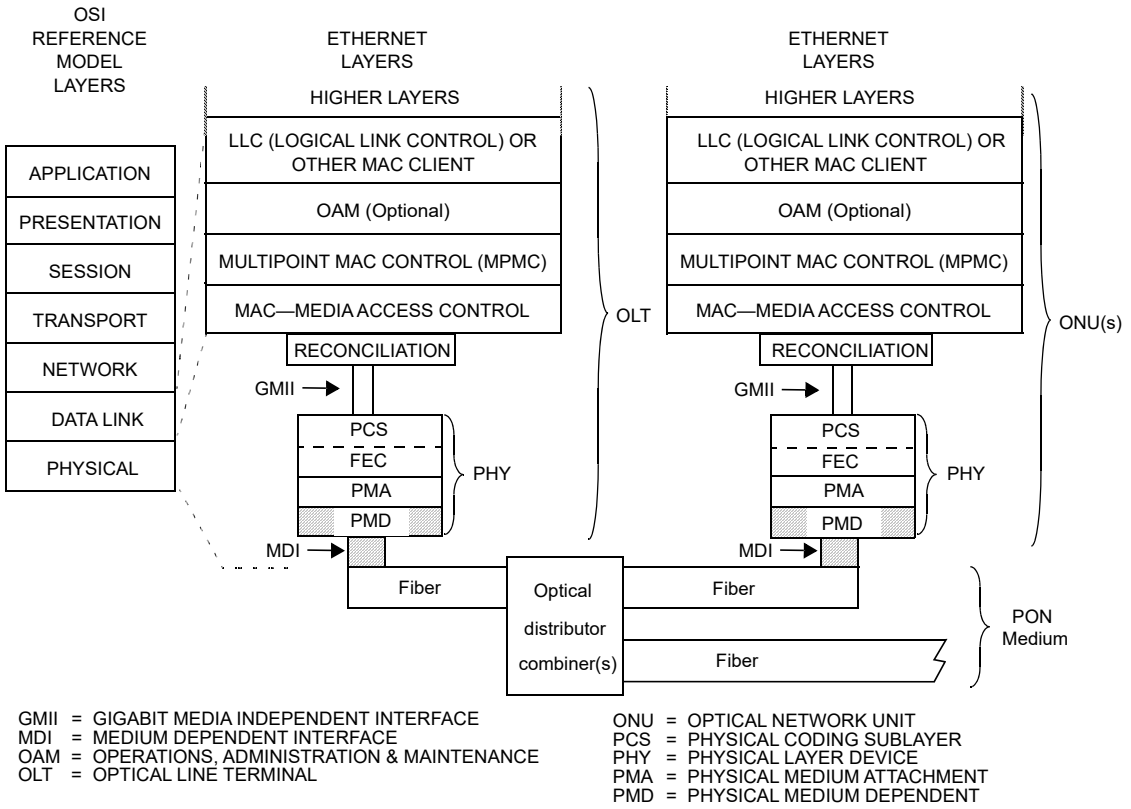

Figure 60–1—P2MP PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

60.1.3 Terminology and conventions

The following list contains references to terminology and conventions used in this clause:

Basic terminology and conventions, see 1.1 and 1.2.

Normative references, see 1.3.

Definitions, see 1.4.

Abbreviations, see 1.5.

Informative references, see Annex A.

Introduction to 1000 Mb/s baseband networks, see Clause 34.

Introduction to Ethernet for subscriber access networks, see Clause 56.

60.1.4 Physical Medium Dependent (PMD) sublayer service interface

The following specifies the services provided by the 1000BASE-PX10, 1000BASE-PX20, 1000BASE-PX30, and 1000BASE-PX40 PMDs.

These PMD sublayer service interfaces are described in an abstract manner and do not imply any particular implementation. The PMD Service Interface supports the exchange of 8B/10B code-groups between the PMA and PMD entities. The PMD translates the serialized data of the PMA to and from signals suitable for the specified medium. The following primitives are defined:

PMD_UNITDATA.request

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PMD_UNITDATA.indication

PMD_SIGNAL.request

PMD_SIGNAL.indication

Table 60–1—PMD types specified in this clause

Description	1000BASE-PX10-U	1000BASE-PX10-D	1000BASE-PX20-U	1000BASE-PX20-D	1000BASE-PX30-U	1000BASE-PX30-D	1000BASE-PX40-U	1000BASE-PX40-D	Unit
Fiber type	IEC 60793–2 B1.1, B1.3 SMF				IEC 60793–2 B1.1, B1.3 SMF ITU–T G.652, G.657 SMF				
Number of fibers	1				1				
Nominal transmit wavelength	1310	1490	1310	1490	1310	1490	1310	1490	nm
Transmit direction[a]	US	DS	US	DS	US	DS	US	DS	
Minimum range[b]	0.5 m to 10 km		0.5 m to 20 km						
Maximum channel insertion loss[c]	20	19.5	24	23.5	29		33		dB
Minimum channel insertion loss[d]	5		10		15		18		dB

[a]US stands for Upstream, DS stands for Downstream.
[b]In an FEC enabled link, the minimum range may be increased, or, links with a higher channel insertion loss may be used.
[c]At nominal transmit wavelength.
[d]The differential insertion loss for a link is the difference between the maximum and minimum channel insertion loss, and not applicable to 1000BASE-PX30 and 1000BASE-PX40.

60.1.5 Delay constraints

Delay requirements from the MDI to the GMII which include the PMD layer are specified in Clause 36. Of the budget, up to 20 ns is allocated for each of the transmit and receive functions of the PMD to account for those cases where the PMD includes a pigtail.

60.1.5.1 PMD_UNITDATA.request

This primitive defines the transfer of a serial data stream from the PMA to the PMD.

The semantics of the service primitive are PMD_UNITDATA.request(tx_bit). The data conveyed by PMD_UNITDATA.request is a continuous stream of bits. The tx_bit parameter can take one of two values: ONE or ZERO. The PMA continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal 1.25 GBd signaling speed. Upon receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals at the MDI.

60.1.5.2 PMD_UNITDATA.indication

This primitive defines the transfer of data from the PMD to the PMA.

The semantics of the service primitive are PMD_UNITDATA.indication(rx_bit). The data conveyed by PMD_UNITDATA.indication is a continuous stream of bits. The rx_bit parameter can take one of two values: ONE or ZERO. The PMD continuously sends a stream of bits to the PMA corresponding to the signals received from the MDI.

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60.1.5.3 PMD_SIGNAL.request

In the upstream direction, this primitive is generated by the PCS to turn on and off the transmitter according to the granted time. A signal for laser control is generated in 65.3.1.1.

The semantics of the service primitive are PMD_SIGNAL.request(tx_enable). The tx_enable parameter can take on one of two values: ENABLE or DISABLE, determining whether the PMD transmitter is on (enabled) or off (disabled). The PCS generates this primitive to indicate a change in the value of tx_enable. Upon receipt of this primitive, the PMD turns the transmitter on or off as appropriate.

60.1.5.4 PMD_SIGNAL.indication

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

The semantics of the service primitive are PMD_SIGNAL.indication(SIGNAL_DETECT). The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting light at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication(rx_bit) is undefined. The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT. If the MDIO interface is implemented, then PMD_global_signal_detect shall be continuously set to the value of SIGNAL_DETECT.

NOTE—SIGNAL_DETECT = OK does not guarantee that PMD_UNITDATA.indication(rx_bit) is known good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the specified bit error ratio. PMD_SIGNAL.indication(SIGNAL_DETECT) has different characteristics for upstream and downstream links, see 60.2.4.

60.2 PMD functional specifications

The 1000BASE-PX PMDs perform the transmit and receive functions that convey data between the PMD service interface and the MDI.

60.2.1 PMD block diagram

The PMD sublayer is defined at the four reference points shown in Figure 60–2 where the first digit represents the downstream direction and the second the upstream. Two points, TP2 and TP3, are compliance points. TP1 and TP4 are reference points for use by implementers. The optical transmit signal is defined at the output end of a patch cord (TP2), between 2 m and 5 m in length, of a fiber type consistent with the link type connected to the transmitter. Unless specified otherwise, all transmitter measurements and tests defined in 60.9 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) connected to the receiver. Unless specified otherwise, all receiver measurements and tests defined in 60.9 are made at TP3.

The electrical specifications of the PMD service interface (TP1 and TP4) are not system compliance points (these are not readily testable in a system implementation). It is expected that in many implementations, TP1 and TP4 will be common between 1000BASE-PX PMDs.

60.2.2 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the optical specifications in this clause. The higher optical power level shall correspond to tx_bit = ONE.

In the upstream direction, the flow of bits is interrupted according to PMD_SIGNAL.request(tx_enable). This implies three optical levels, 1, 0, and dark, the latter corresponding to the transmitter being in the OFF state.

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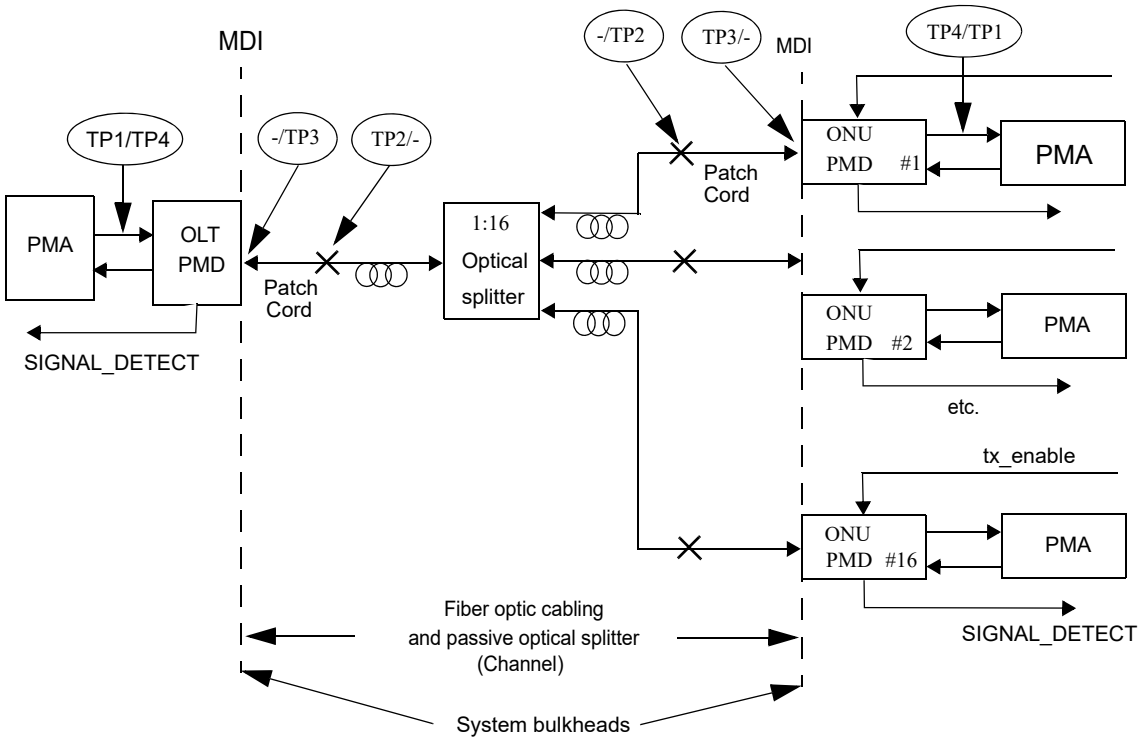

Figure 60–2—1000BASE-PX block diagram

60.2.3 PMD receive function

The PMD Receive function shall convey the bits received from the MDI according to the optical specifications in this clause to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). The higher optical power level shall correspond to rx_bit = ONE.

60.2.4 PMD signal detect function

60.2.4.1 ONU PMD signal detect (downstream)

The PMD Signal Detect function for the continuous mode downstream signal shall report to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indication is intended to be an indicator of optical signal presence.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 60–2 for 1000BASE-PX. The PMD receiver is not required to verify whether a compliant 1000BASE-PX signal is being received.

60.2.4.2 OLT PMD signal detect (upstream)

The response time for the PMD Signal Detect function for the burst mode upstream signal may be longer or shorter than a burst length, thus, it may not fulfill the traditional requirements placed on Signal Detect. PMD_SIGNAL.indication is intended to be an indicator of optical signal presence. The signal detect function in the OLT may be realized in the PMD or PMA layer.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 60–2 for 1000BASE-PX. The PMD receiver is not required to verify whether a compliant 1000BASE-PX signal is being received.

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60.2.4.3 1000BASE-PX Signal detect functions

The Signal Detect value definitions for the 1000BASE-PX PMDs are shown in Table 60–2.

Table 60–2—1000BASE-PX SIGNAL_DETECT value definition

PMD type	Receive conditions	SIGNAL_DETECT value
1000BASE-PX10	Average input optical power ≤ Signal Detect Threshold (min) in Table 60–5 at the specified receiver wavelength	FAIL
	Average input optical power ≥ Receive sensitivity (max) in Table 60–5 with a compliant 1000BASE-X signal input at the specified receiver wavelength	OK
	All other conditions	Unspecified
1000BASE-PX20	Average input optical power ≤ Signal Detect Threshold (min) in Table 60–8 at the specified receiver wavelength	FAIL
	Average input optical power ≥ Receive sensitivity (max) in Table 60–8 with a compliant 1000BASE-X signal input at the specified receiver wavelength	OK
	All other conditions	Unspecified
1000BASE-PX30	Average input optical power ≤ Signal Detect Threshold (min) in Table 60–9 at the specified receiver wavelength	FAIL
	Average input optical power ≥ Receive sensitivity (max) in Table 60–9 with a compliant 1000BASE-X signal input at the specified receiver wavelength	OK
	All other conditions	Unspecified
1000BASE-PX40	Average input optical power ≤ Signal Detect Threshold (min) in Table 60–12 at the specified receiver wavelength	FAIL
	Average input optical power ≥ Receive sensitivity (max) in Table 60–12 with a compliant 1000BASE-X signal input at the specified receiver wavelength	OK
	All other conditions	Unspecified

60.2.5 PMD transmit enable function for ONU

PMD_SIGNAL.request(tx_enable) is defined for the two ONU PMDs. PMD_SIGNAL.request(tx_enable) is asserted prior to data transmission by the ONU PMDs.

60.3 PMD to MDI optical specifications for 1000BASE-PX10-D and 1000BASE-PX10-U

The operating range for 1000BASE-PX10 is defined in Table 60–1. A 1000BASE-PX10 compliant transceiver supports all media types listed in Table 60–16 according to the specifications described in 60.11. A transceiver which exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a single-mode solution operating at 10.5 km meets the minimum range requirement of 0.5 m to 10 km for 1000BASE-PX10).

NOTE—The specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is defined in 58.7.6.

60.3.1 Transmitter optical specifications

The 1000BASE-PX10-D and 1000BASE-PX10-U transmitter's specifications described in Table 60–3 are normative requirements, per measurement techniques described in 60.9, with the exception of $RIN_{15}OMA$ which is an optional requirement per measurement techniques described in 60.9.7.

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Table 60–3—1000BASE-PX10-D and 1000BASE-PX10-U transmit characteristics

Description	1000BASE-PX10-D	1000BASE-PX10-U	Unit
Nominal transmitter type[a]	Longwave Laser	Longwave Laser	
Signaling speed (range)	1.25 ± 100 ppm	1.25 ± 100 ppm	GBd
Wavelength[b] (range)	1480 to 1500	1260 to 1360	nm
RMS spectral width (max)	see Table 60–4		nm
Average launch power (max)	+2	+4	dBm
Average launch power (min)	–3	–1	dBm
Average launch power of OFF transmitter (max)	–39	–45	dBm
Extinction ratio (min)	6	6	dB
$RIN_{15}OMA$ (max)	–118	–113	dB/Hz
Launch OMA (min)	–2.2 (0.6)	–0.22 (0.95)	dBm (mW)
Transmitter eye mask definition {X1, X2, Y1, Y2, Y3}	{0.22, 0.375, 0.2, 0.2, 0.3}	{0.22, 0.375, 0.2, 0.2, 0.3}	UI
T_{on} (max)	N/A	512	ns
T_{off} (max)	N/A	512	ns
Optical return loss tolerance (max)	15	15	dB
Optical return loss of ODN (min)	20	20	dB
Transmitter reflectance (max)	–10	–6	dB
Transmitter and dispersion penalty (max)	1.3	2.8	dB
Decision timing offset for transmitter and dispersion penalty (min)	± 0.1	± 0.125	UI

[a]The nominal transmitter type is not intended to be a requirement on the source type, and any device meeting the transmitter characteristics specified may be substituted for the nominal transmitter type.
[b]This represents the range of centre wavelength ±1σ of the rms spectral width.

The maximum RMS spectral width vs. wavelength for 1000BASE-PX10 is shown in Table 60–4 and for 1000BASE-PX10-U in Figure 60–3. The equation used to generate these values is included in 60.9.2. The central column values are normative, the right hand column is optional.

Table 60–4—1000BASE-PX10-D and 1000BASE-PX10-U transmitter spectral limits

Center Wavelength	RMS spectral width (max)[a]	RMS spectral width to achieve epsilon $\varepsilon \leq$ **0.115 (optional)**
nm	**nm**	**nm**
1260	**2.09**	1.43
1270	**2.52**	1.72
1280	**3.13**	2.14

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Table 60–4—1000BASE-PX10-D and 1000BASE-PX10-U transmitter spectral limits *(continued)*

Center Wavelength	RMS spectral width (max)[a]	RMS spectral width to achieve epsilon $\varepsilon \leq 0.115$ (optional)
nm	**nm**	**nm**
1286	**3.50**	2.49
1290		2.80
1297		3.50
1329		
1340		2.59
1343		2.41
1350	**3.06**	2.09
1360	**2.58**	1.76
1480 to 1500	**0.88**	0.60

[a]These limits for the 1000BASE-PX10-U transmitter are illustrated in Figure 60–3. The equation used to calculate these values is detailed in 60.9.2. Limits at intermediate wavelengths may be found by interpolation.

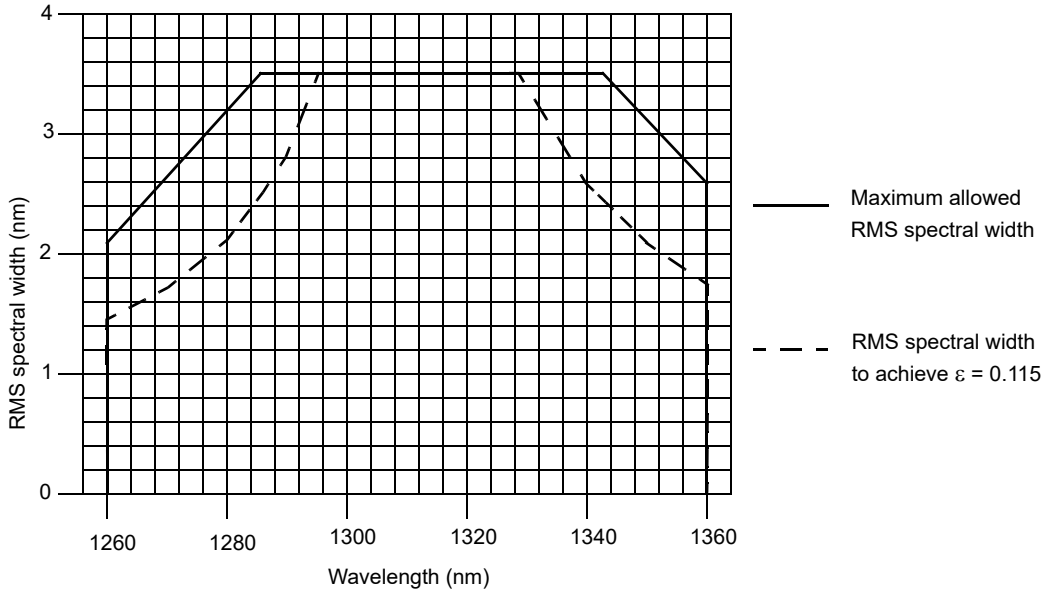

Figure 60–3—1000BASE-PX10-U transmitter spectral limits

60.3.2 Receiver optical specifications

The 1000BASE-PX10-D and 1000BASE-PX10-U receiver shall meet the specifications defined in Table 60–5 per measurement techniques defined in 60.9.10 with the following exceptions. The stressed receive sensitivity (OMA) should meet the values listed in Table 60–5 per measurement techniques described in 60.9.11. Either the damage threshold included in Table 60–5 shall be met, or, the receiver shall

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be labeled to indicate the maximum optical input power level to which it can be continuously exposed without damage. The vertical eye-closure penalty, the stressed eye jitter, the jitter corner frequency, and the sinusoidal jitter limits are test conditions for measuring stressed receiver sensitivity and are not required characteristics of the receiver.

Table 60–5—1000BASE-PX10-D and 1000BASE-PX10-U receive characteristics

Description	1000BASE-PX10-D	1000BASE-PX10-U	Unit
Signaling speed (range)	1.25 ± 100 ppm	1.25 ± 100 ppm	GBd
Wavelength (range)	1260 to 1360	1480 to 1500	nm
Bit error ratio (max)	10^{-12}		
Average receive power (max)	–1	–3	dBm
Damage threshold (max)	+4	+2	dBm
Receiver sensitivity (max)	–24	–24	dBm
Receiver sensitivity OMA (max)	–23.2 (5)	–23.2 (5)	dBm (μW)
Signal detect threshold (min)	–45	–44	dBm
Receiver reflectance (max)	–12	–12	dB
Stressed receive sensitivity (max)	–22.3	–21.4	dBm
Stressed receive sensitivity OMA (max)	–21.5 (7)	–20.7 (8.6)	dBm (μW)
Vertical eye-closure penalty (min)	1.2	2.2	dB
$T_{receiver\_settling}$ (max)	400	N/A	ns
Stressed eye jitter (min)	0.25	0.25	UI pk-pk
Jitter corner frequency	637	637	kHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)	(0.05, 0.15)	(0.05, 0.15)	UI

60.4 PMD to MDI optical specifications for 1000BASE-PX20-D and 1000BASE-PX20-U

The operating range for 1000BASE-PX20 is defined in Table 60–1. A 1000BASE-PX20 compliant transceiver supports all media types listed in Table 60–16 according to the specifications described in 60.11.2. A transceiver that exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a single-mode solution operating at 20.5 km meets the minimum range requirement of 0.5 m to 20 km for 1000BASE-PX20).

NOTE—The specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is explained in 58.7.6.

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60.4.1 Transmitter optical specifications

The 1000BASE-PX20-D and 1000BASE-PX20-U transmitter's specifications described in Table 60–6 are normative requirements, per measurement techniques described in 60.9, with the exception of $RIN_{15}OMA$ which is an optional requirement per measurement techniques described in 60.9.7.

Table 60–6—1000BASE-PX20-D and 1000BASE-PX20-U transmit characteristics

Description	1000BASE-PX20-D	1000BASE-PX20-U	Unit
Nominal transmitter type[a]	Longwave Laser	Longwave Laser	
Signaling speed (range)	1.25 ± 100 ppm	1.25 ± 100 ppm	GBd
Wavelength[b] (range)	1480 to 1500	1260 to 1360	nm
RMS spectral width (max)	see Table 60–7		nm
Average launch power (max)	+7	+4	dBm
Average launch power (min)	+2	–1	dBm
Average launch power of OFF transmitter (max)	–39	–45	dBm
Extinction ratio (min)	6	6	dB
$RIN_{15}OMA$ (max)	–115	–115	dB/Hz
Launch OMA (min)	2.8 (1.9)	–0.22 (0.95)	dBm (mW)
Transmitter eye mask definition {X1, X2, Y1, Y2, Y3}	{0.22, 0.375, 0.2, 0.2, 0.3}	{0.22, 0.375, 0.2, 0.2, 0.3}	UI
T_{on} (max)	N/A	512	ns
T_{off} (max)	N/A	512	ns
Optical return loss tolerance (max)	15	15	dB
Optical return loss of ODN (min)	20	20	dB
Transmitter reflectance (max)	–10	–10	dB
Transmitter and dispersion penalty (max)	2.3	1.8	dB
Decision timing offset for transmitter and dispersion penalty (min)	± 0.1	± 0.125	UI

[a]The nominal transmitter type is not intended to be a requirement on the source type, and any device meeting the transmitter characteristics specified may be substituted for the nominal transmitter type.
[b]This represents the range of centre wavelength ±1σ of the rms spectral width.

The maximum RMS spectral width vs. wavelength for 1000BASE-PX20 is shown in Table 60–7 and for 1000BASE-PX20-U in Figure 60–4. The equation used to generate these values is included in 60.9.2. The central column values are normative, the right hand column is optional.

60.4.2 Receiver optical specifications

The 1000BASE-PX20-D and 1000BASE-PX20-U receiver shall meet the specifications defined in Table 60–8 per measurement techniques defined in 60.9.10 with the following exceptions. The stressed receive sensitivity (OMA) should meet the values listed in Table 60–8 per measurement techniques

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Table 60–7—1000BASE-PX20-D and 1000BASE-PX20-U transmitter spectral limits

Center Wavelength	RMS spectral width (max) [a]	RMS spectral width to achieve epsilon $\varepsilon \leq 0.10$ (optional)
nm	nm	nm
1260	**0.72**	0.62
1270	**0.86**	0.75
1280	**1.07**	0.93
1290	**1.40**	1.22
1300	**2.00**	1.74
1304	**2.5**	2.42
1305	**2.55**	2.5
1308	**3.00**	
1317		
1320	**2.53**	2.2
1321	**2.41**	
1330	**1.71**	1.48
1340	**1.29**	1.12
1350	**1.05**	0.91
1360	**0.88**	0.77
1480 to 1500	**0.44**	0.30

[a]These limits for the 1000BASE-PX20-U are illustrated in Figure 60–4. The equation used to calculate these values is detailed in 60.9.2. Limits at intermediate wavelengths may be found by interpolation.

described in 60.9.11. Either the damage threshold included in Table 60–8 shall be met, or, the receiver shall be labeled to indicate the maximum optical input power level to which it can be continuously exposed without damage. The vertical eye-closure penalty, the stressed eye jitter, the jitter corner frequency, and the sinusoidal jitter limits are test conditions for measuring stressed receiver sensitivity and are not required characteristics of the receiver.

Table 60–8—1000BASE-PX20-D and 1000BASE-PX20-U receive characteristics

Description	1000BASE-PX20-D	1000BASE-PX20-U	Unit
Signaling speed (range)	1.25 ± 100 ppm	1.25 ± 100 ppm	GBd
Wavelength (range)	1260 to 1360	1480 to 1500	nm
Bit error ratio (max)	10^{-12}		
Average receive power (max)	–6	–3	dBm
Damage threshold (max)	+4	+7	dBm
Receive sensitivity (max)	–27	–24	dBm
Receiver sensitivity OMA (max)	–26.2 (2.4)	–23.2 (5)	dBm (μW)

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Table 60–8—1000BASE-PX20-D and 1000BASE-PX20-U receive characteristics *(continued)*

Description	1000BASE-PX20-D	1000BASE-PX20-U	Unit
Signal detect threshold (min)	–45	–44	dBm
Receiver reflectance (max)	–12	–12	dB
Stressed receive sensitivity (max)	–24.4	–22.1	dBm
Stressed receive sensitivity OMA (max)	–23.6 (4.3)	–21.3 (7.4)	dBm (μW)
Vertical eye-closure penalty (min)	2.2	1.5	dB
$T_{receiver\_settling}$ (max)	400	N/A	ns
Stressed eye jitter (min)	0.28	0.25	UI pk-pk
Jitter corner frequency	637	637	kHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)	(0.05, 0.15)	(0.05, 0.15)	UI

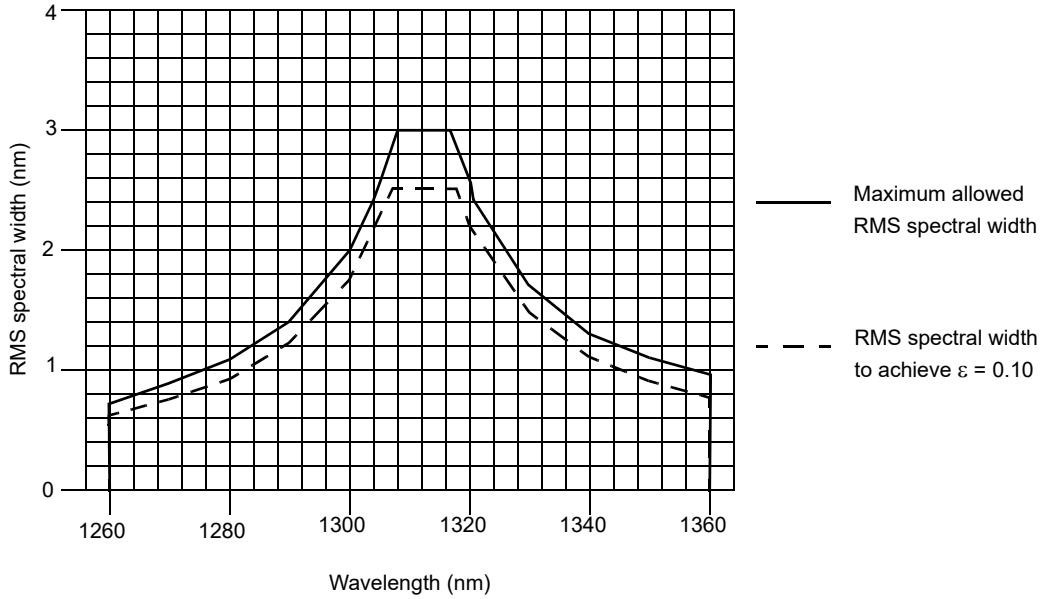

Figure 60–4—1000BASE-PX20-U transmitter spectral limits

60.5 PMD to MDI optical specifications for 1000BASE-PX30-D and 1000BASE-PX30-U

The operating range for 1000BASE-PX30 is defined in Table 60–1. A 1000BASE-PX30 compliant transceiver supports all media types listed in Table 75–14 according to the specifications described in 75.9. A transceiver which exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a single-mode solution operating at 20.5 km meets the minimum range requirement of 0.5 m to 20 km for 1000BASE-PX30).

NOTE—The specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is defined in 58.7.6.

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60.5.1 Transmitter optical specifications

The 1000BASE-PX30-D and 1000BASE-PX30-U transmitter's specifications described in Table 60–9 are normative requirements, per measurement techniques described in 60.8, with the exception of $RIN_{15}OMA$ which is an optional requirement, per measurement techniques described in 60.9.7.

The maximum RMS spectral width vs. wavelength for 1000BASE-PX30 is shown in Table 60–10 and for 1000BASE-PX30-U in Figure 60–5. 1000BASE-PX30-D transmitter uses a DFB laser, and 1000BASE-PX30-U transmitter can use either a DFB or Fabry-Perot laser. If 1000BASE-PX30-U PMD employs a DFB laser, Side Mode Suppression Ratio requirement shown in Table 60–9 is mandatory. If 1000BASE-PX30-U PMD employs a Fabry-Perot laser, RMS spectral width requirement shown in Table 60–10 and Figure 60–5 is mandatory. The equation used to generate these values is included in 60.9.2. The central column values are normative, the right hand column is optional.

Table 60–9—1000BASE-PX30-D and 1000BASE-PX30-U transmit characteristics

Description	1000BASE-PX30-D	1000BASE-PX30-U	Unit
Nominal transmitter type[a]	Longwave Laser	Longwave Laser	
Signaling speed (range)	1.25 ± 100 ppm	1.25 ± 100 ppm	GBd
Wavelength[b] (range)	1480 to 1500	1260 to 1360	nm
Side Mode Suppression Ratio	30	30[c]	dB
RMS spectral width (max)	N/A	see Table 60–10[c]	nm
Average launch power (max)	7	5.62	dBm
Average launch power (min)	3	0.62	dBm
Average launch power of OFF transmitter (max)	–39	–45	dBm
Extinction ratio (min)	6	6	dB
$RIN_{15}OMA$ (max)	–115	–115	dB/Hz
Launch OMA (min)	3.78 (2.39)	1.4 (1.38)	dBm (mW)
Transmitter eye mask definition {X1, X2, Y1, Y2, Y3}	{0.22, 0.375, 0.2, 0.2, 0.3}	{0.22, 0.375, 0.2, 0.2, 0.3}	UI
T_{on} (max)	N/A	512	ns
T_{off} (max)	N/A	512	ns
Optical return loss tolerance (max)	15	15	dB
Optical return loss of ODN (min)	20	20	dB
Transmitter reflectance (max)	–10	–10	dB
Transmitter and dispersion penalty (max)	1	1.4	dB
Decision timing offset for transmitter and dispersion penalty (min)	±0.1	±0.125	UI

[a]The nominal transmitter type is not intended to be a requirement on the source type, and any device meeting the transmitter characteristics specified may be substituted for the nominal transmitter type.
[b]This represents the range of centre wavelength ±1σ of the rms spectral width.
[c]If 1000BASE-PX30-U PMD employs a DFB laser, Side Mode Suppression Ratio is mandatory. If it employs a Fabry-Perot laser, RMS spectral width requirement is mandatory.

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Table 60–10—1000BASE-PX30-U transmitter spectral limits

Center wavelength	RMS spectral width (max)[a]	RMS spectral width to achieve epsilon $\varepsilon \leq 0.08$ (optional)
nm	nm	nm
1260	0.59	0.5
1270	0.7	0.59
1280	0.87	0.74
1290	1.14	0.97
1300	1.64	1.39
1304	1.98	1.67
1305	2.09	1.77
1308	2.4	2
1317	2.4	2
1320	2.07	1.75
1321	1.98	1.67
1330	1.4	1.18
1340	1.06	0.89
1350	0.86	0.72
1360	0.72	0.61
1480 to 1500	0.25	0.21

[a]These limits for the 1000BASE–PX30–U transmitter are illustrated in Figure 60–5. The equation used to calculate these values is detailed in 60.9.2. Limits at intermediate wavelengths may be found by interpolation.

60.5.2 Receiver optical specifications

The 1000BASE-PX30-D and 1000BASE-PX30-U receiver shall meet the specifications defined in Table 60–11 per measurement techniques defined in 60.9.10 with the following exceptions. The stressed receive sensitivity OMA (max) should meet the value listed in Table 60–11 per measurement techniques described in 60.9.11. Either the damage threshold included in Table 60–11 shall be met, or, the receiver shall be labeled to indicate the maximum optical input power level to which it can be continuously exposed without damage. The vertical eye-closure penalty, the stressed eye jitter, the jitter corner frequency, and the sinusoidal jitter limits are test conditions for measuring stressed receiver sensitivity and are not required characteristics of the receiver.

60.6 PMD to MDI optical specifications for 1000BASE-PX40-D and 1000BASE-PX40-U

The operating range for 1000BASE-PX40 is defined in Table 60–1. A 1000BASE-PX40 compliant transceiver supports all media types listed in Table 75–14 according to the specifications described in 75.9. A transceiver which exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a single-mode solution operating at 20.5 km meets the minimum range requirement of 0.5 m to 20 km for 1000BASE-PX40).

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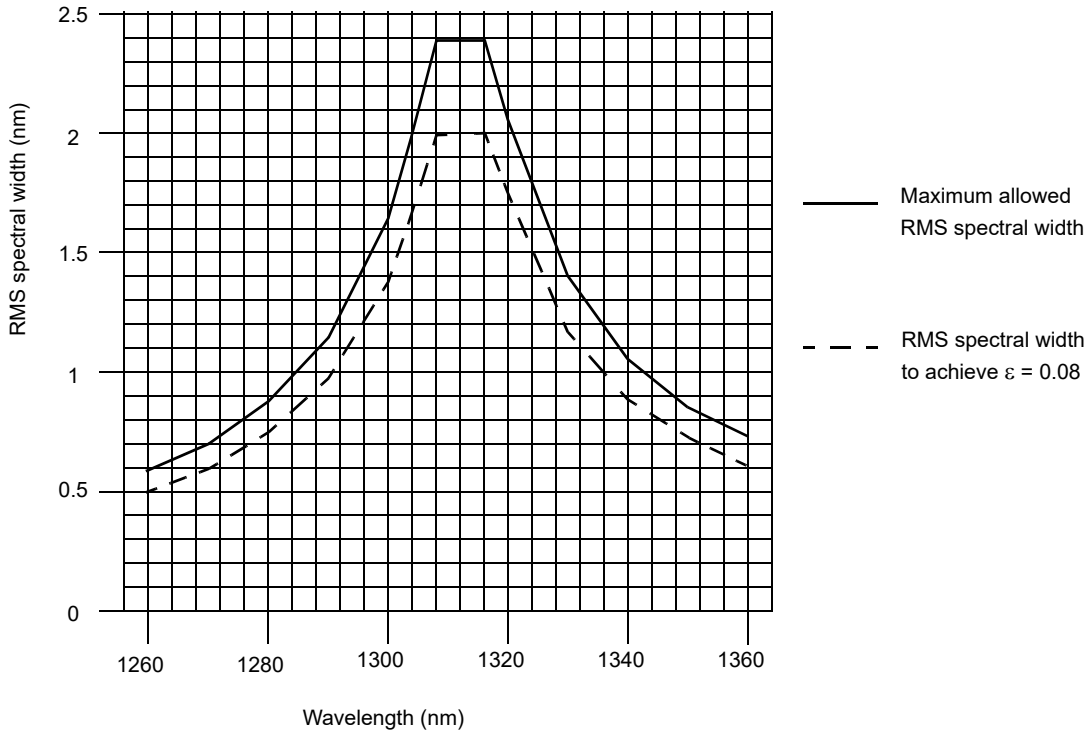

Figure 60–5—1000BASE-PX30-U transmitter spectral limits

Table 60–11—1000BASE-PX30-D and 1000BASE-PX30-U receive characteristics

Description	1000BASE-PX30-D	1000BASE-PX30-U	Unit
Signaling speed (range)	1.25 ± 100 ppm	1.25 ± 100 ppm	GBd
Wavelength (range)	1260 to 1360	1480 to 1500	nm
Bit error ratio (max)	10^{-12}		
Average receive power (max)	–9.38	–8	dBm
Damage threshold (max)[a]	–5	+4	dBm
Receiver sensitivity (max)	–29.78	–27	dBm
Receiver sensitivity OMA (max)	–29 (1.26)	–26.22 (2.39)	dBm (μW)
Signal detect threshold (min)	–45	–44	dBm
Receiver reflectance (max)	–12	–12	dB
Stressed receive sensitivity (max)	–28.38	–26	dBm
Stressed receive sensitivity OMA (max)	–27.6 (1.74)	–25.22 (3.01)	dBm (μW)
Vertical eye-closure penalty (min)	1.4	1.5	dB

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Table 60–11—1000BASE-PX30-D and 1000BASE-PX30-U receive characteristics *(continued)*

Description	1000BASE-PX30-D	1000BASE-PX30-U	Unit
$T_{receiver\_settling}$ (max)[b]	400	N/A	ns
Stressed eye jitter (min)	0.28	0.25	UI pk-pk
Jitter corner frequency	637	637	kHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)	(0.05, 0.15)	(0.05, 0.15)	UI

[a]Direct ONU–OLT connection may result in damage of the receiver.
[b]$T_{receiver\_settling}$ represents an upper bound. Optics with better performance may be used in compliant implementations, since the OLT notifies the ONUs of its requirements in terms of the $T_{receiver\_settling}$ time via the syncTime parameter.

NOTE—The specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is defined in 58.7.6.

60.6.1 Transmitter optical specifications

The 1000BASE-PX40-D and 1000BASE-PX40-U transmitter's specifications described in Table 60–12 are normative requirements, per measurement techniques described in 60.9, with the exception of $RIN_{15}OMA$ which is an optional requirement, per measurement techniques described in 60.9.7.

Table 60–12—1000BASE-PX40-D and 1000BASE-PX40-U transmit characteristics

Description	1000BASE-PX40-D	1000BASE-PX40-U	Unit
Nominal transmitter type[a]	Longwave Laser	Longwave Laser	
Signaling speed (range)	1.25 ± 100 ppm	1.25 ± 100 ppm	GBd
Wavelength (range)	1480 to 1500	1290 to 1330	nm
Side Mode Suppression Ratio (min)[b]	30		dB
Average launch power (max)	10	6	dBm
Average launch power (min)	4	2	dBm
Average launch power of OFF transmitter (max)	–39	–45	dBm
Extinction ratio (min)	6	6	dB
$RIN_{15}OMA$ (max)	–115	–115	dB/Hz
Launch OMA (min)	4.78 (3.01)	2.78 (1.9)	dBm (mW)
Transmitter eye mask definition {X1, X2, Y1, Y2, Y3}	{0.22, 0.375, 0.2, 0.2, 0.3}	{0.22, 0.375, 0.2, 0.2, 0.3}	UI
T_{on} (max)	N/A	512	ns
T_{off} (max)	N/A	512	ns
Optical return loss tolerance (max)	15	15	dB
Optical return loss of ODN (min)	20	20	dB
Transmitter reflectance (max)	–10	–10	dB
Transmitter and dispersion penalty (max)	1	1	dB
Decision timing offset for transmitter and dispersion penalty (min)	±0.1	±0.125	UI

[a]The nominal device type is not intended to be a requirement on the source type, and any device meeting the transmitter characteristics specified may be substituted for the nominal device type.

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[b]Transmitter is a single longitudinal mode device. Chirp is allowed such that the total penalty does not exceed that found in Table 60–14.

60.6.2 Receiver optical specifications

The 1000BASE-PX40-D and 1000BASE-PX40-U receiver shall meet the specifications defined in Table 60–13 per measurement techniques defined in 60.9.10 with the following exceptions. The stressed receive sensitivity OMA (max) should meet the value listed in Table 60–13 per measurement techniques described in 60.9.11. Either the damage threshold included in Table 60–13 shall be met, or, the receiver shall be labeled to indicate the maximum optical input power level to which it can be continuously exposed without damage. The vertical eye-closure penalty, the stressed eye jitter, the jitter corner frequency, and the sinusoidal jitter limits are test conditions for measuring stressed receiver sensitivity and are not required characteristics of the receiver.

Table 60–13—1000BASE-PX40-D and 1000BASE-PX40-U receive characteristics

Description	1000BASE-PX40-D	1000BASE-PX40-U	Unit
Signaling speed (range)	1.25 ± 100 ppm	1.25 ± 100 ppm	GBd
Wavelength (range)	1260 to 1360	1480 to 1500	nm
Bit error ratio (max)	10^{-12}		
Average receive power (max)	–12	–8	dBm
Damage threshold (max)[a]	–6	–3	dBm
Receiver sensitivity (max)	–32	–30	dBm
Receiver sensitivity OMA (max)	–31.22 (0.76)	–29.22 (1.2)	dBm (μW)
Signal detect threshold (min)	–45	–44	dBm
Receiver reflectance (max)	–12	–12	dB
Stressed receive sensitivity (max)	–31	–29	dBm
Stressed receive sensitivity OMA (max)	–30.22 (0.95)	–28.22 (1.51)	dBm (μW)
Vertical eye-closure penalty (min)	2.2	1.5	dB
$T_{receiver\_settling}$ (max)[b]	400	N/A	ns
Stressed eye jitter (min)	0.28	0.25	UI pk-pk
Jitter corner frequency	637	637	kHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)	(0.05, 0.15)	(0.05, 0.15)	UI

[a]Direct ONU–OLT connection may result in damage of the receiver.
[b]$T_{receiver\_settling}$ represents an upper bound. Optics with better performance may be used in compliant implementations, since the OLT notifies the ONUs of its requirements in terms of the $T_{receiver\_settling}$ time via the syncTime parameter.

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60.7 Illustrative 1000BASE-PX channels and penalties

Illustrative power budget for 1000BASE-PX10, 1000BASE-PX20, 1000BASE-PX30, and 1000BASE-PX40 channels are shown in Table 60–14.

Table 60–14—Illustrative 1000BASE-PX channel insertion loss and penalties

Description[a]	1000BASE -PX10		1000BASE -PX20		1000BASE -PX30		1000BASE -PX40		Unit
	US	DS	US	DS	US	DS	US	DS	
Fiber type	IEC 60793–2 B1.1, B1.3 SMF				IEC 60793–2 B1.1, B1.3 SMF ITU-T G.652, G.657 SMF				
Measurement wavelength for fiber	1310	1550[b]	1310	1550[b]	1310	1550[b]	1310	1550[b]	nm
Nominal distance	10		20						km
Available power budget[c]	23	21	26	26	30.4	30	34	34	dB
Channel insertion loss (max)[d]	20	19.5	24	23.5	29		33		dB
Channel insertion loss (min)[e]	5		10		15		18		dB
Allocation for penalties[f]	3	1.5	2	2.5	1.4	1	1	1	dB
Optical return loss of ODN (min)	20								dB

[a]US stands for Upstream, DS stands for Downstream.
[b]The nominal transmit wavelength is 1490 nm.
[c]In an FEC enabled link, when not operating at the dispersion limit, the available power budget is increased by 2.5 dB.
[d]The channel insertion loss is based on the cable attenuation at the target distance and nominal measurement wavelength. The channel insertion loss also includes the loss for connectors, splices and other passive components such as splitters.
[e]The power budgets for PX10, PX20, PX30, and PX40 links are such that a minimum insertion loss is assumed between transmitter and receiver. This minimum attenuation is required for PMD testing.
[f]The allocation for penalties is the difference between the available power budget and the channel insertion loss; insertion loss difference between nominal and worst case operating wavelength is considered a penalty. This allocation may be used to compensate for transmission related penalties. Further details are given in 60.9.2.

NOTE—The budgets include an allowance for –12 dB reflection at the receiver.

60.8 Jitter at TP1 to TP4 for 1000BASE-PX

Jitter at TP1 to TP4 for 1000BASE-PX is informatively described in Annex 60A.

60.9 Optical measurement requirements

The following sections describe definitive patterns and test procedures for certain PMDs of this standard. implementers using alternative verification methods need to ensure adequate correlation and allow adequate margin such that specifications are met by reference to the definitive methods. All optical measurements, except TDP and $RIN_{15}OMA$, shall be made through a short patch cable between 2 m and 5 m in length.

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60.9.1 Frame-based test patterns

Subclause 59.7.1 provides suitable patterns for frame-based testing.

NOTE—Users are advised to take care that the system under test is not connected to a network in service.

60.9.2 Wavelength, spectral width, and side mode suppression ratio (SMSR) measurements

The wavelength, spectral width (RMS), and SMSR shall meet specifications according to the centroidal wavelength, RMS spectral width, and SMSR definitions in IEC 61280-1-3, under modulated conditions using a valid 1000BASE-X signal.

NOTE 1—The allowable range of central wavelengths is narrower than the operating wavelength range by the actual RMS spectral width at each extreme.

NOTE 2—The 20 dB width for SLM lasers is taken as 6.07 times the RMS width.

The interaction between the transmitter and the chromatic dispersion of the fiber is accounted for by a parameter ε (epsilon), which is defined as the product of 10^{-3} times the signaling speed (in GBd) times the path dispersion (in ps/nm) times the RMS spectral width (in nm).

$$\varepsilon = \text{dispersion} \times \text{length} \times \text{RMS spectral width} \times 10^{-3} \quad (60–1)$$

For the 1000BASE-PX10-D and 1000BASE-PX10-U links, a maximum ε close to 0.168 is imposed by the middle column of Table 60–4. If the spectral width is kept below the limits of the right hand column, ε will not exceed 0.115, and the chromatic dispersion penalty is expected to be below 2 dB when all link parameters are simultaneously at worst case values. For the 1000BASE-PX20-D and 1000BASE-PX20-U links, a maximum ε close to 0.115 is imposed by the middle column of Table 60–7. If the spectral width is kept below the limits of the right hand column, ε will not exceed 0.10, and the chromatic dispersion penalty is expected to be below 1.5 dB when all link parameters are simultaneously at worst case values.

For the 1000BASE-PX30-D and 1000BASE-PX30-U links, a maximum ε close to 0.095 is imposed by the middle column of Table 60–10. If the spectral width is kept below the limits of the right hand column, ε will not exceed 0.08, and the chromatic dispersion penalty is expected to be below 0.9 dB when all link parameters are simultaneously at worst case values.

The chromatic dispersion penalty is a component of transmitter and dispersion penalty (TDP), which is specified in Table 60–3, Table 60–6, Table 60–9, and Table 60–12, and described in 58.7.9.

60.9.3 Optical power measurements

Optical power shall meet specifications according to the methods specified in IEC 61280-1-1. A measurement may be made with the port transmitting any valid encoded 8B/10B data stream.

60.9.4 Extinction ratio measurements

Extinction ratio shall meet specifications according to IEC 61280-2-2 with the port transmitting a repeating idle pattern /I2/ ordered set (see 36.2.4.12) that may be interspersed with OAM packets per 57A.2, and with minimal back reflections into the transmitter, lower than –20 dB. The /I2/ ordered set is defined in Clause 36, and is coded as /K28.5/D16.2/, which is binary 001111 1010 100100 0101 within idles. The extinction ratio is expected to be similar for other valid 8B/10B bit streams. The test receiver has the frequency response as specified for the transmitter optical waveform measurement.

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60.9.5 OMA measurements (optional)

Subclause 58.7.5 provides a reference technique for performing OMA measurements.

60.9.6 OMA relationship to extinction ratio and power measurements

Annex 58B provides information on how OMA, extinction ratio and mean power are related to each other (see 58B.2).

60.9.7 Relative intensity noise optical modulation amplitude ($RIN_{15}OMA$)

$RIN_{15}OMA$ is the ratio of noise to modulated optical signal in the presence of a back reflection. The measurement procedure is described in 58.7.7.

60.9.8 Transmitter optical waveform (transmit eye)

The required transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 60–6.

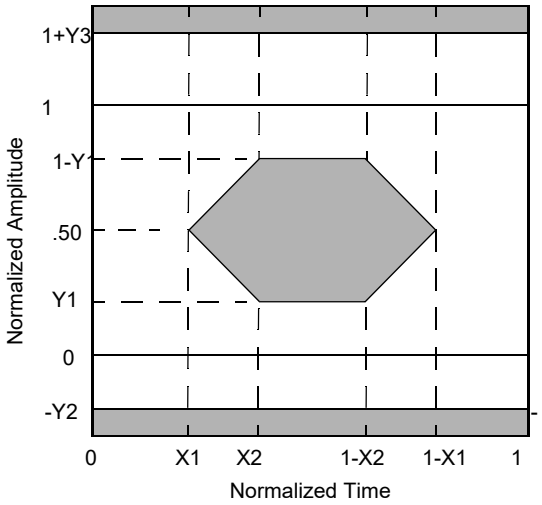

Figure 60–6—Transmitter eye mask definition

The measurement procedure is described in 58.7.8 and references therein.

The eye shall comply to the mask of the eye using a fourth-order Bessel-Thomson receiver response with f_r = 0.9375 GHz, and where the relative response vs. relative frequency is defined in ITU-T G.957, Table B.2 (STM-16 values), along with the allowed tolerances for its physical implementation.

NOTE 1—This Bessel-Thomson filter is not intended to represent the noise filter used within an optical receiver, but is intended to provide uniform measurement conditions on the transmitter.

NOTE 2—The fourth-order Bessel-Thomson filter is reactive. In order to suppress reflections, a 6 dB attenuator may be required at the filter input and/or output.

60.9.9 Transmitter and dispersion penalty (TDP)

TDP measurement tests for transmitter impairments with chromatic effects for a transmitter to be used with single-mode fiber. Possible causes of impairment include intersymbol interference, jitter, RIN and mode partition noise. Meeting the separate requirements (e.g., eye mask, spectral characteristics) does not in itself

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guarantee the transmitter and dispersion penalty (TDP). The TDP limit shall be met. See 58.7.9 for details of the measurement.

60.9.10 Receive sensitivity measurement

Receiver sensitivity is defined for the random pattern test frame and an ideal input signal quality with the specified extinction ratio. The measurement procedure is described in 58.7.10. The sensitivity shall be met for the bit error ratio defined in Table 60–5, Table 60–8, Table 60–11, or Table 60–13 as appropriate.

60.9.11 Stressed receive conformance test

The stressed receiver conformance test is intended to screen against receivers with poor frequency response or timing characteristics which could cause errors when combined with a distorted but compliant signal at TP3. Modal (MMF) or chromatic (SMF) dispersion can cause distortion. The conformance test signal uses the random pattern test frame and is conditioned by applying deterministic jitter and intersymbol interference. If the option for stressed receiver compliance is chosen, the receiver shall meet the specified bit error ratio at the power level and signal quality defined in Table 60–5, Table 60–8, Table 60–11, and Table 60–13 as appropriate, according to the measurement procedures of 58.7.11.

60.9.12 Jitter measurements

Jitter measurements are informatively described in 58B.4.

60.9.13 Other measurements

60.9.13.1 Laser On/Off timing measurement

T_{on} is defined in 60.9.13.1.1, value is less than 512 ns (defined in Table 60–3, Table 60–6, Table 60–9, and Table 60–12).

$T_{receiver\_settling}$ is defined in 60.9.13.2.1, value is less than 400 ns (defined in Table 60–5, Table 60–8, Table 60–11, and Table 60–13).

T_{CDR} is defined in 65.3.2.1, value is less than 400 ns (defined in 60.2.2).

$T_{code\_group\_align}$ is defined in 36.3.2.4, value is less than 4 ten-bit code-groups.

T_{off} is defined in 60.9.13.1.1, value is less than 512 ns (defined in Table 60–3, Table 60–6, Table 60–9, and Table 60–12).

60.9.13.1.1 Definitions

T_{on} is denoted as the time beginning from the falling edge of the tx_enable line to the ONU PMD and ending at the time that the optical signal at TP2 of the ONU PMD is within 15% of its steady state parameters (average launched power, wavelength, RMS spectral width, transmitter and dispersion penalty, optical return loss tolerance, jitter, $RIN_{15}OMA$, extinction ratio and eye mask opening) as defined in Table 60–3 for 1000BASE-PX10-U, Table 60–6 for 1000BASE-PX20-U, Table 60–9 for 1000BASE-PX30-U, and Table 60–12 for 1000BASE-PX40-U. T_{on} is presented in Figure 60–7. The data transmitted may be any valid 8B/10B symbols.

T_{off} is denoted as the time beginning from the rising edge of the tx_enable line to the ONU PMD and ending at the time that the optical signal at TP2 of the ONU PMD reaches the specified average launch power of off transmitter as defined in Table 60–3 for 1000BASE-PX10-U, Table 60–6 for 1000BASE-PX20-U,

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Table 60–9 for 1000BASE-PX30-U, and Table 60–12 for 1000BASE-PX40-U. T_{off} is presented in Figure 60–7. The data transmitted may be any valid 8B/10B symbols.

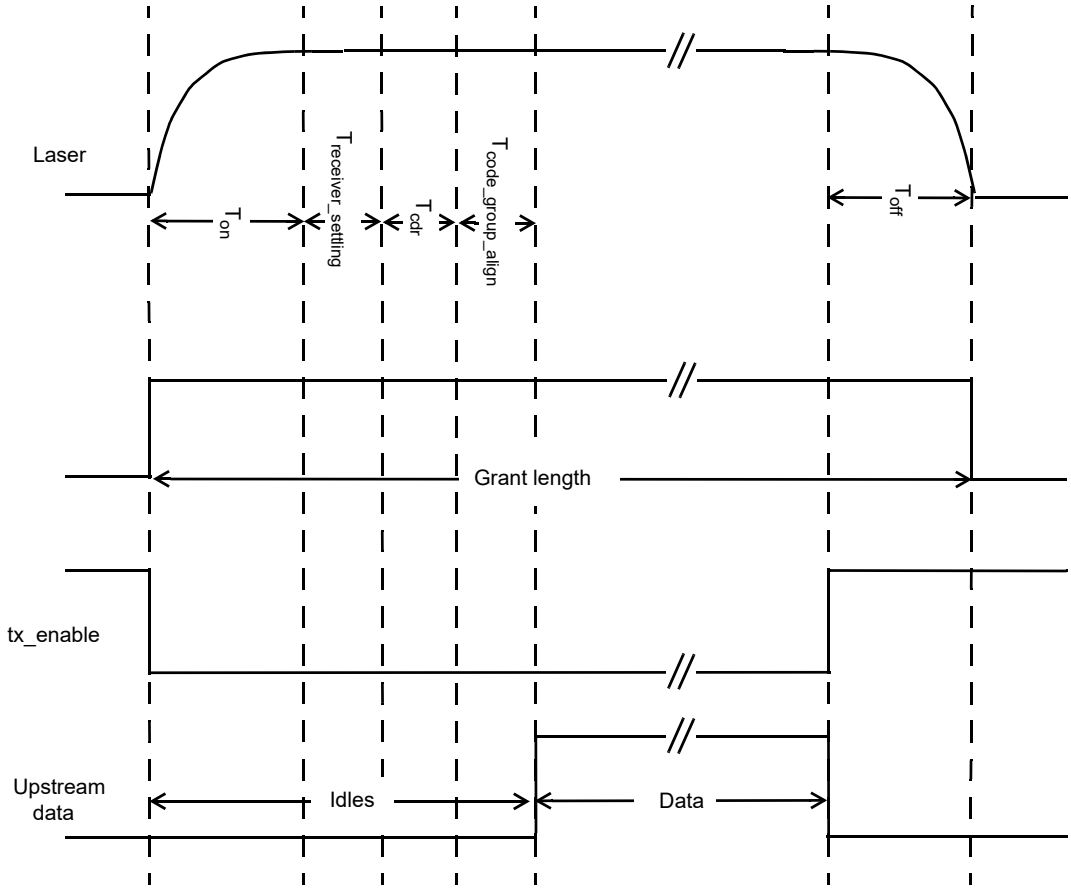

Figure 60–7—P2MP timing parameter definition

60.9.13.1.2 Test specification

The test setup for measuring T_{on} and T_{off} is described in Figure 60–8. An O/E converter is used to convert the optical signal at TP3 to an electrical signal at TP4 where it is assumed that the response time of the converter is considerably shorter that the T_{on} value under measurement. A scope, with a variable delay, can measure the time from the tx_enable trigger to the time the optical signal reaches all its specified conditions. The delay to the scope trigger is adjusted until the point that the received signal meets all its specified conditions. This is the T_{on} in question.

A non-rigorous way to describe this test setup would be: for a PMD with a declared T_{on} and T_{off}, measure all PMD optical parameter after T_{on} and T_{off} from the tx_enable trigger, ensuring conformance to within 15% of the steady state values. Notice that only the steady state optical OFF power has to be verified when measuring T_{off} time, since that is the only relevant parameter.

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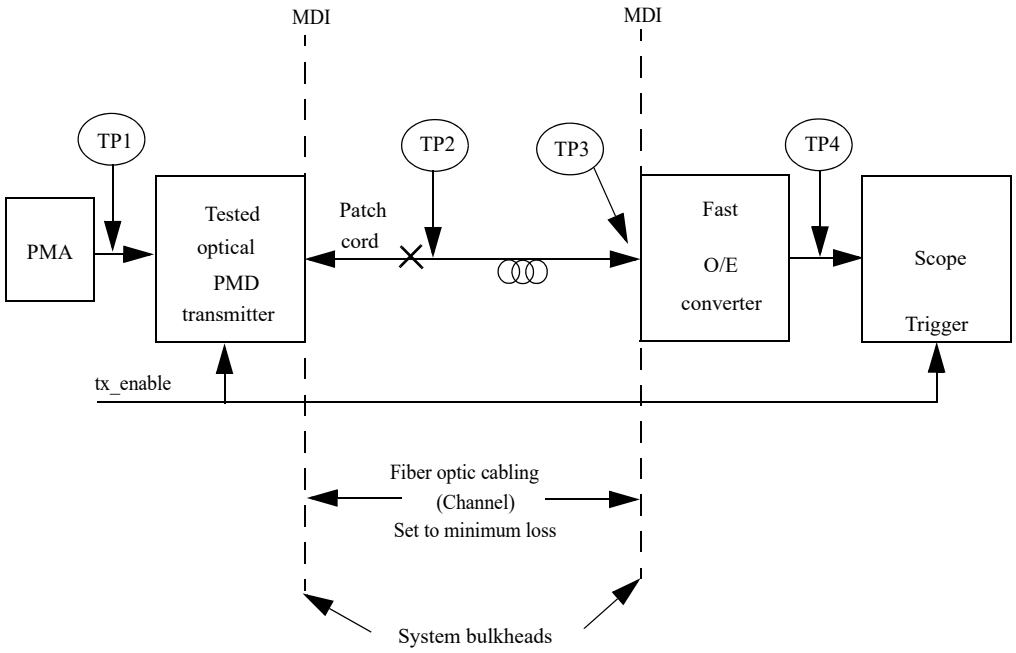

Figure 60–8—ONU PMD Laser on/off time measurement setup

60.9.13.2 Receiver settling timing measurement

60.9.13.2.1 Definitions

$T_{receiver\_settling}$ is denoted as the time beginning from the time that the optical power in the receiver at TP3 reaches the conditions specified in 38.6.11, 58.7.11.2 and ending at the time that the electrical signal after the PMD at TP4, reaches within 15% of its steady state parameter, (average power, jitter), see Table 60–5, Table 60–8, Table 60–11, and Table 60–13. $T_{receiver\_settling}$ is presented in Figure 60–7. The data transmitted may be any valid 8B/10B symbols (or a specific power synchronization sequence). The optical signal at TP3, at the beginning of the locking, may have any valid 8B/10B pattern, optical power level, jitter, or frequency shift matching the standard specifications.

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60.9.13.2.2 Test specification

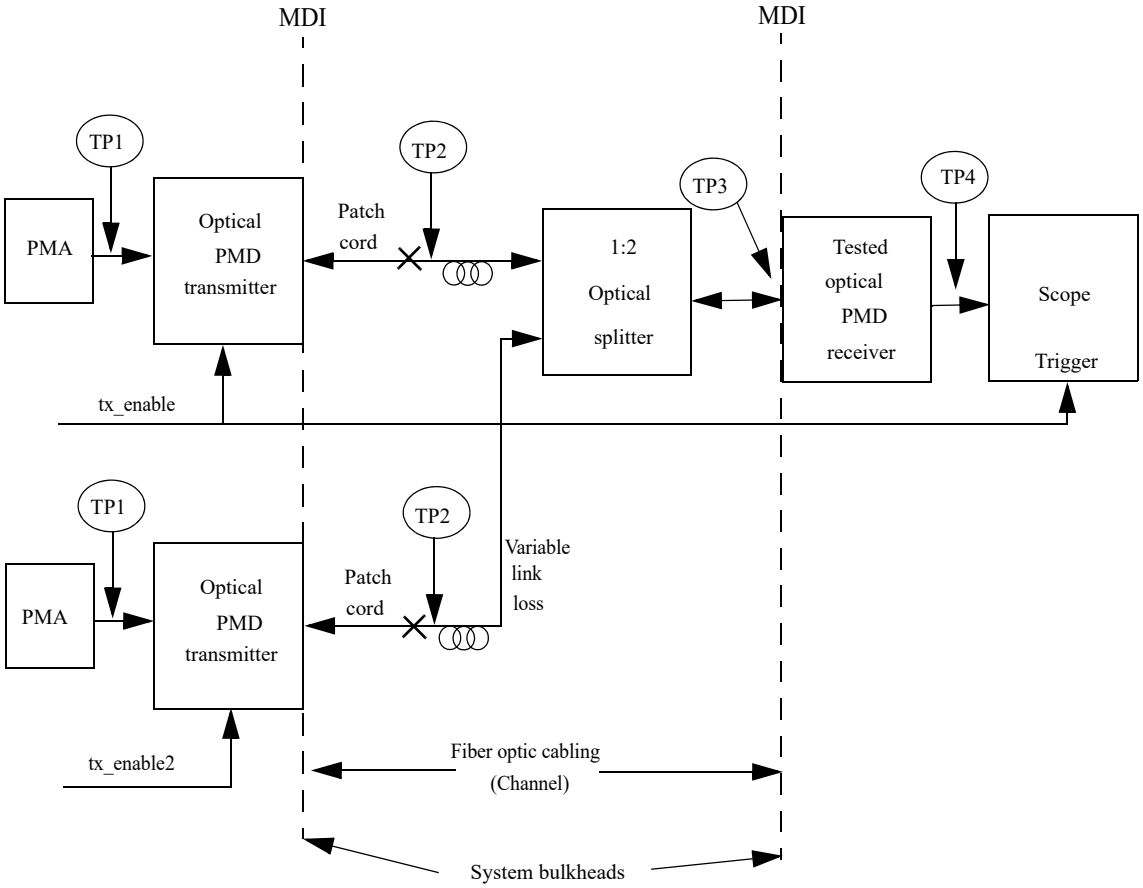

Figure 60–9—Receiver settling time measurement setup

Figure 60–9 illustrates the test setup for the OLT PMD receiver (upstream) $T_{receiver\_settling}$ time. The optical PMD transmitter has well-known parameters, with a fixed known T_{on} time. After T_{on} time the parameters of the reference transmitter, at TP2 and therefore at TP3, reach within 15% of its steady state values as specified in Table 60–3 for 1000BASE-PX10-U, Table 60–6 for 1000BASE-PX20-U, Table 60–9 for 1000BASE-PX30-U, and Table 60–12 for 1000BASE-PX40-U.

Define $T_{receiver\_settling}$ time as the time from the tx_enable assertion, minus the known T_{on} time, to the time the electrical signal at TP4 reaches within 15% of its steady state conditions.

Conformance should be assured for an optical signal at TP3 with any level of its specified parameters before the tx_enable assertion. Especially the $T_{receiver\_settling}$ time has to be met in the following scenarios:

— Switching from a ‘weak’ (minimal received power at TP3) ONU to a ‘strong’ (maximal received power at TP3) ONU, with minimal guard band between.
— Switching from a ‘strong’ ONU to a ‘weak’ ONU, with minimal guard band between.
— Switching from noise level, with maximal duration interval, to ‘strong’ ONU power level.

The following procedure is a non-rigorous way to verify the declared $T_{receiver\_settling}$ time.

a) Use a reference transmitter with a known T_{on}.
b) For the PMD receiver under test, measure all PMD receiver electrical parameters at TP8 after $T_{receiver\_settling}$ from the tx_enable trigger minus the reference transmitter T_{on}.

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c) Verify the conformance of the measured parameters to within 15% of their specified steady state values.

60.10 Environmental, safety, and labeling

60.10.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

60.10.2 Laser safety

1000BASE-PX10, 1000BASE-PX20, 1000BASE-PX30, and 1000BASE-PX40 optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore. Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation shall explicitly define requirements and usage restrictions on the host system necessary to meet these safety certifications.

60.10.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

60.10.4 Environment

Reference Annex 67A for additional environmental information.

Two optional temperature ranges are defined in Table 60–15. Implementations shall be declared as compliant over one or both complete ranges, or not so declared (compliant over parts of these ranges or another temperature range).

Table 60–15—Component case temperature classes

Class	Low temperature (°C)	High temperature (°C)
Warm extended	–5	+85
Cool extended	–40	+60
Universal extended	–40	+85

60.10.5 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 1000BASE-PX10-U).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 60.10.2.

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Each systems and field pluggable component shall be clearly labeled with its operating temperature range over which their compliance is ensured.

60.11 Characteristics of the fiber optic cabling

The 1000BASE-PX fiber optic cabling shall meet the dispersion specifications defined in IEC 60793-2 and ITU-T G.652, or the requirements of Table 60–16 where they differ. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. It also includes a connector plug at each end to connect to the MDI. The fiber optic cabling spans from one MDI to another MDI, as shown in Figure 60–10.

60.11.1 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 60–10.

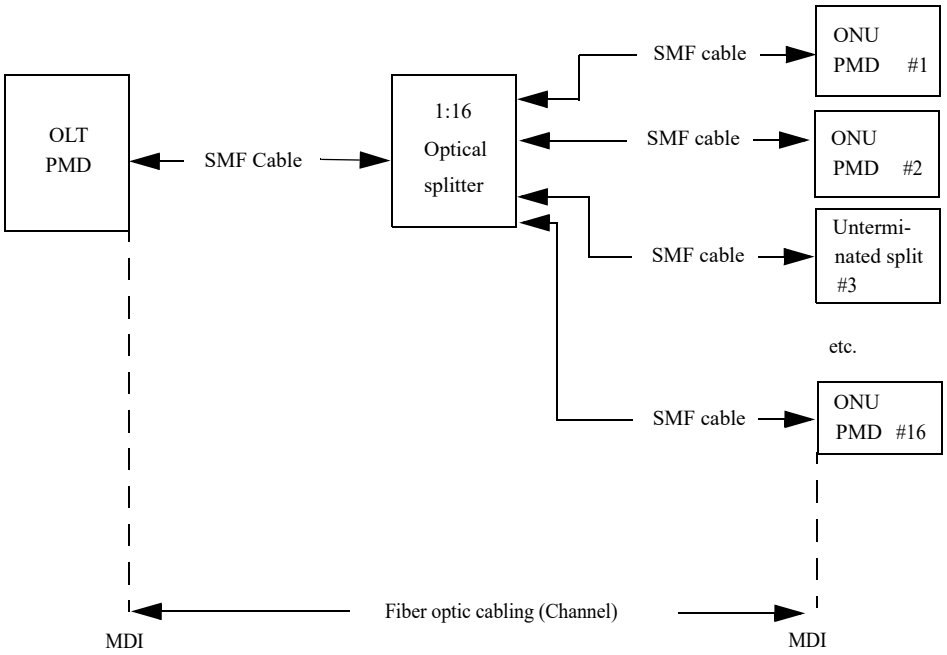

Figure 60–10—Fiber optic cable model

NOTE—The 1:16 optical splitter may be replaced by a number of smaller 1:n splitters such that a different topology may be implemented while preserving the link characteristics and power budget as defined in Table 60–14.

The maximum channel insertion losses shall meet the requirements specified in Table 60–1. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

60.11.2 Optical fiber and cable

The fiber optic cable requirements for 1000BASE-PX10 and 1000BASE-PX20 are satisfied by the fibers specified in IEC 60793-2 Type B1.1 (dispersion un-shifted single-mode fiber) and Type B1.3 (low water peak single-mode fiber) and ITU-T G.652, or by the requirements of Table 60–16 where they differ.

The fiber optic cable requirements for 1000BASE-PX30 and 1000BASE-PX40 are satisfied by the fibers specified in IEC 60793–2 Type B1.1 (dispersion un–shifted single-mode fiber), Type B1.3 (low water peak

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single-mode fiber), ITU-T G.652, and ITU-T G.657 (bend–insensitive single-mode fiber), or by the requirements of Table 75–14 where they differ.

60.11.3 Optical fiber connection

Table 60–16—Optical fiber and cable characteristics

Description[a]	Type B1.1, B1.3 SMF		Unit
Nominal wavelength[b]	1310	1550	nm
Cabled optical fiber attenuation (max)[c]	0.4	0.35	dB/km
Zero dispersion wavelength[d]	$1300 \le \lambda_0 \le 1324$		nm
Dispersion slope (max)	0.093		ps / nm^2 · km

[a]The fiber dispersion values are normative, all other values in the table are optional.
[b]Wavelength specified is the nominal wavelength and typical measurement wavelength. Power penalties at other wavelengths are accounted for.
[c]Attenuation for single-mode optical fiber cables is defined in ITU-T G.652.
[d]See IEC 60793 or ITU-T G.652.

An optical fiber connection as shown in Figure 60–10 consists of a mated pair of optical connectors. The 1000BASE-PX is coupled to the fiber optic cabling through an optical connection and any optical splitters into the MDI optical receiver, as shown in Figure 60–10. The channel insertion loss includes the loss for connectors, splices and other passive components such as splitters, see Table 60–14.

The link attenuations have been calculated on the assumption of 14.5 dB for a 16:1 splitter; 3.5 dB, 4 dB, 7.5 dB, or 8 dB (at the appropriate measurement wavelength where these attenuations are a combination of the minimum range given in Table 60–1 and the values in Table 60–16) for cabled optical fiber attenuation and 1.5 dB for connectors and splices. For example, this allocation supports three connections with an average insertion loss equal to 0.5 dB (or less) per connection, or two connections with a maximum insertion loss of 0.75 dB. Other arrangements, such as a shorter link length and a higher split ratio in the case of 1000BASE-PX20, may be used provided the requirements of Table 60–1 are met.

The maximum discrete reflectance for single-mode connections shall be less than –26 dB.

60.11.4 Medium Dependent Interface (MDI)

The 1000BASE-PX10, 1000BASE-PX20, 1000BASE-PX30, or 1000BASE-PX40 PMD is coupled to the fiber cabling at the MDI. The MDI is the interface between the PMD and the “fiber optic cabling” as shown in Figure 60–10. Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a remateable connection, it shall meet the interface performance specifications of IEC 61753-1. The MDI carries the signal in both directions for 1000BASE-PX10, 1000BASE-PX20, 1000BASE-PX30, and 1000BASE-PX40 and couples to a single fiber.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 60.2.1, not at the MDI.

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60.12 Protocol implementation conformance statement (PICS) proforma for Clause 60, Physical Medium Dependent (PMD) sublayer and medium, type 1000BASE-PX (long wavelength passive optical networks)[114]

60.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 60, Physical Medium Dependent (PMD) sublayer and medium, type 1000BASE-PX (long wavelength passive optical networks), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

60.12.2 Identification

60.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

60.12.2.2 Protocol Summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 60, Physical Medium Dependent (PMD) sublayer and medium, type 1000BASE-PX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[114]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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60.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
HT	High temperature operation	60.10.4	–5 °C to 85 °C	O	Yes [ ] No [ ]
LT	Low temperature operation	60.10.4	–40 °C to 60 °C	O	Yes [ ] No [ ]
*PX10U	1000BASE-PX10-U-PHY or 1000BASE-PX10-U PMD	60.3	Device supports 10 km	O/1	Yes [ ] No [ ]
*PX10D	1000BASE-PX10-D-PHY or 1000BASE-PX10-D PMD	60.3	Device supports 10 km	O/1	Yes [ ] No [ ]
*PX20U	1000BASE-PX20-U-PHY or 1000BASE-PX20-U PMD	60.4	Device supports 20 km	O/1	Yes [ ] No [ ]
*PX20D	1000BASE-PX20-D-PHY or 1000BASE-PX20-D PMD	60.4	Device supports 20 km	O/1	Yes [ ] No [ ]
*PX30U	1000BASE-PX30-U-PHY or 1000BASE-PX30-U PMD	60.5	Device supports 20 km	O/1	Yes [] No []
*PX30D	1000BASE-PX30-D-PHY or 1000BASE-PX30-D PMD	60.5	Device supports 20 km	O/1	Yes [] No []
*PX40U	1000BASE-PX40-U-PHY or 1000BASE-PX40-U PMD	60.6	Device supports 20 km	O/1	Yes [] No []
*PX40D	1000BASE-PX40-D-PHY or 1000BASE-PX40-D PMD	60.6	Device supports 20 km	O/1	Yes [] No []
*INS	Installation / Cable	60.11	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]

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60.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 1000BASE-PX (long wavelength passive optical networks)

60.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FN1	Transmit function	60.2.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FN2	Transmitter optical signal	60.2.2	Higher optical power transmitted is a logic 1	M	Yes [ ]
FN3	Receive function	60.2.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FN4	Receiver optical signal	60.2.3	Higher optical power received is a logic 1	M	Yes [ ]
FN5	Signal detect function (downstream)	60.2.4.1	Mapping to PMD service interface	M	Yes [ ]
FN6	Signal detect parameter (downstream)	60.2.4.1	Generated according to Table 60–2	M	Yes [ ]
FN7	Signal detect function (upstream)	60.2.4.2	Mapping to PMD service interface	O/2	Yes [ ]
FN7	Signal detect function (upstream)	60.2.4.2	Provided by higher layer	O/2	Yes [ ]
FN8	Signal detect parameter (upstream)	60.2.4.1	Generated according to Table 60–2	O	Yes [ ]

60.12.4.2 PMD to MDI optical specifications for 1000BASE-PX10-D

Item	Feature	Subclause	Value/Comment	Status	Support
PX10D1	1000BASE-PX10-D transmitter	60.3.1	Meets specifications in Table 60–3	PX10D:M	Yes [ ] N/A [ ]
PX10D2	1000BASE-PX10-D transmitter $RIN_{15}OMA$	60.3.1	Meets the $RIN_{15}OMA$ specification in Table 60–3	PX10D:O	Yes [ ] N/A [ ]
PX10D3	1000BASE-PX10-D receiver	60.3.2	Meets specifications in Table 60–5	PX10D:M	Yes [ ] N/A [ ]
PX10D4	1000BASE-PX10-D stressed receiver sensitivity	60.3.2	Meets specifications in Table 60–5	PX10D:O	Yes [ ] No [ ] N/A[ ]
PX10D5	1000BASE-PX10-D receiver damage threshold	60.3.2	If the receiver does not meet the damage requirements in Table 60–5 then label accordingly	PX10D:M	Yes [ ] N/A [ ]

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60.12.4.3 PMD to MDI optical specifications for 1000BASE-PX10-U

Item	Feature	Subclause	Value/Comment	Status	Support
PX10U1	1000BASE-PX10-U transmitter	60.3.1	Meets specifications in Table 60–3	PX10U:M	Yes [ ] N/A [ ]
PX10U2	1000BASE-PX10-U transmitter $RIN_{15}OMA$	60.3.1	Meets the $RIN_{15}OMA$ specification in Table 60–3	PX10U:O	Yes [ ] N/A [ ]
PX10U3	1000BASE-PX10-U receiver	60.3.2	Meets specifications in Table 60–5	PX10U:M	Yes [ ] N/A [ ]
PX10U4	1000BASE-PX10-U stressed receiver sensitivity	60.3.2	Meets specifications in Table 60–5	PX10U:O	Yes [ ] No [ ] N/A[ ]
PX10U5	1000BASE-PX10-U receiver damage threshold	60.3.2	If the receiver does not meet the damage requirements in Table 60–5 then label accordingly	PX10U:M	Yes [ ] N/A [ ]

60.12.4.4 PMD to MDI optical specifications for 1000BASE-PX20-D

Item	Feature	Subclause	Value/Comment	Status	Support
PX20D1	1000BASE-PX20-D transmitter	60.4.1	Meets specifications in Table 60–6	PX20D:M	Yes [ ] N/A [ ]
PX20D2	1000BASE-PX20-D transmitter $RIN_{15}OMA$	60.4.1	Meets the $RIN_{15}OMA$ specification in Table 60–6	PX20D:O	Yes [ ] N/A [ ]
PX20D3	1000BASE-PX20-D receiver	60.4.2	Meets specifications in Table 60–8	PX20D:M	Yes [ ] N/A [ ]
PX20D4	1000BASE-PX20-D stressed receiver sensitivity	60.4.2	Meets specifications in Table 60–8	PX20D:O	Yes [ ] No [ ] N/A[ ]
PX20D5	1000BASE-PX20-D receiver damage threshold	60.4.2	If the receiver does not meet the damage requirements in Table 60–8 then label accordingly	PX20D:M	Yes [ ] N/A [ ]

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60.12.4.5 PMD to MDI optical specifications for 1000BASE-PX20-U

Item	Feature	Subclause	Value/Comment	Status	Support
PX20U1	1000BASE-PX20-U transmitter	60.4.1	Meets specifications in Table 60–6	PX20U:M	Yes [ ] N/A [ ]
PX20U2	1000BASE-PX20-U transmitter $RIN_{15}OMA$	60.4.1	Meets the $RIN_{15}OMA$ specification in Table 60–6	PX20U:O	Yes [ ] N/A [ ]
PX20U3	1000BASE-PX20-U receiver	60.4.2	Meets specifications in Table 60–8	PX20U:M	Yes [ ] N/A [ ]
PX20U4	1000BASE-PX20-U stressed receiver sensitivity	60.4.2	Meets specifications in Table 60–8	PX20U:O	Yes[ ] No [ ] N/A[ ]
PX20U5	1000BASE-PX20-U receiver damage threshold	60.4.2	If the receiver does not meet the damage requirements in Table 60–8 then label accordingly	PX20U:M	Yes [ ] N/A [ ]

60.12.4.6 PMD to MDI optical specifications for 1000BASE-PX30-D

Item	Feature	Subclause	Value/Comment	Status	Support
PX30D1	1000BASE-PX30-D transmitter	60.5.1	Meets normative specifications in Table 60–9	PX30D:M	Yes [ ] N/A [ ]
PX30D2	1000BASE-PX30-D transmitter $RIN_{15}OMA$	60.5.1	Meets the $RIN_{15}OMA$ specification in Table 60–9	PX30D:O	Yes [ ] N/A [ ]
PX30D3	1000BASE-PX30-D receiver	60.5.2	Meets specifications in Table 60–11	PX30D:M	Yes [ ] N/A [ ]
PX30D4	1000BASE-PX30-D stressed receiver sensitivity	60.5.2	Meets specifications in Table 60–11	PX30D:O	Yes [ ] No [ ] N/A[ ]
PX30D5	1000BASE-PX30-D receiver damage threshold	60.5.2	If the receiver does not meet the damage requirements in Table 60–11 then label accordingly	PX30D:M	Yes [ ] N/A [ ]

60.12.4.7 PMD to MDI optical specifications for 1000BASE-PX30-U

Item	Feature	Subclause	Value/Comment	Status	Support
PX30U1	1000BASE-PX30-U transmitter	60.5.1	Meets specifications in Table 60–9	PX30U:M	Yes [ ] N/A [ ]
PX30U2	1000BASE-PX30-U transmitter $RIN_{15}OMA$	60.5.1	Meets the $RIN_{15}OMA$ specification in Table 60–9	PX30U:O	Yes [ ] N/A [ ]
PX30U3	1000BASE-PX30-U receiver	60.5.2	Meets specifications in Table 60–11	PX30U:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PX30U4	1000BASE-PX30-U stressed receiver sensitivity	60.5.2	Meets specifications in Table 60–11	PX30U:O	Yes [ ] No [ ] N/A[ ]
PX30U5	1000BASE-PX30-U receiver damage threshold	60.5.2	If the receiver does not meet the damage requirements in Table 60–11 then label accordingly	PX30U:M	Yes [ ] N/A [ ]

60.12.4.8 PMD to MDI optical specifications for 1000BASE-PX40-D

Item	Feature	Subclause	Value/Comment	Status	Support
PX40D1	1000BASE-PX40-D transmitter	60.6.1	Meets specifications in Table 60–12	PX40D:M	Yes [ ] N/A [ ]
PX40D2	1000BASE-PX40-D transmitter $RIN_{15}OMA$	60.6.1	Meets the $RIN_{15}OMA$ specification in Table 60–12	PX40D:O	Yes [ ] N/A [ ]
PX40D3	1000BASE-PX40-D receiver	60.6.2	Meets specifications in Table 60–13	PX40D:M	Yes [ ] N/A [ ]
PX40D4	1000BASE-PX40-D stressed receiver sensitivity	60.6.2	Meets specifications in Table 60–13	PX40D:O	Yes[ ] No [ ] N/A[ ]
PX40D5	1000BASE-PX40-D receiver damage threshold	60.6.2	If the receiver does not meet the damage requirements in Table 60–13 then label accordingly	PX40D:M	Yes [ ] N/A [ ]

60.12.4.9 PMD to MDI optical specifications for 1000BASE-PX40-U

Item	Feature	Subclause	Value/Comment	Status	Support
PX40U1	1000BASE-PX40-U transmitter	60.6.1	Meets specifications in Table 60–12	PX40U:M	Yes [ ] N/A [ ]
PX40U2	1000BASE-PX40-U transmitter $RIN_{15}OMA$	60.6.1	Meets the $RIN_{15}OMA$ specification in Table 60–12	PX40U:O	Yes [ ] N/A [ ]
PX40U2	1000BASE-PX40-U receiver	60.6.2	Meets specifications in Table 60–13	PX40U:M	Yes [ ] N/A [ ]
PX40U3	1000BASE-PX40-U stressed receiver sensitivity	60.6.2	Meets specifications in Table 60–13	PX40U:O	Yes[ ] No [ ] N/A[ ]
PX40U4	1000BASE-PX40-U receiver damage threshold	60.6.2	If the receiver does not meet the damage requirements in Table 60–13 then label accordingly	PX40U:M	Yes [ ] N/A [ ]

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60.12.4.10 Optical measurement requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	60.9	2 m to 5 m in length	M	Yes [ ]
OM2	Wavelength, spectral width, and SMSR	60.9.2	Per the centroidal wavelength, RMS spectral width, and SMSR definitions in IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	60.9.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	Extinction ratio	60.9.4	Per IEC 61280-2-2 with minimal back reflections and fourth-order Bessel-Thomson receiver	M	Yes [ ]
OM5	$RIN_{15}OMA$	60.9.7	As described in 58.7.7	M	Yes [ ]
OM6	Transmit optical waveform (transmit eye)	60.9.8	Per 58.7.8 and references therein	M	Yes [ ]
OM7	Transmitter and dispersion penalty measurements	60.9.9	As described in 58.7.9	M	Yes [ ]
OM8	Receive sensitivity	60.9.10	With specified pattern	M	Yes [ ]
*OM9	Stressed receiver conformance test	60.9.11	As described in 60.9.11	O	Yes[ ] N/A[ ]

60.12.4.11 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
FO1	Fiber optic cabling	60.11	Specified in Table 60–16	INS:M	Yes [ ] N/A[ ]
F02	End-to-end channel loss	60.11	Meeting the requirements of Table 60–1	INS:M	Yes [ ] N/A[ ]
FO3	Maximum discrete reflectance - single-mode fiber	60.11.2	Less than –26 dB	INS:M	Yes [ ] N/A [ ]
FO4	MDI requirements	60.11.4	Meet the interface performance specifications of IEC 61753-1, if remateable	INS:O	Yes [ ] No [ ] N/A [ ]

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60.12.4.12 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	60.10.1	Conforms to J.2	M	Yes [ ]
ES2	Laser safety —IEC Hazard Level 1	60.10.2	Conform to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Documentation	60.10.2	Explicitly defines requirements and usage restrictions to meet safety certifications	M	Yes [ ]
ES4	Operating temperature range labeling	60.10.5	If required	M	Yes [ ] N/A[ ]

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61. Physical Coding Sublayer (PCS), Transmission Convergence (TC) sublayer, and common specifications, type 10PASS-TS and type 2BASE-TL

61.1 Overview

This clause specifies the Physical Coding Sublayer (PCS), Transmission Convergence sublayer (TC), and handshaking mechanisms that are common to a family of Physical Layer implementations for Ethernet over voice-grade copper known as 10PASS-TS and 2BASE-TL. These PHYs deliver a minimum of 10 Mb/s over distances of up to 750 m, and a minimum of 2 Mb/s over distances of up to 2700 m, using a single copper pair. Optionally, transmission over multiple copper pairs is supported.

The copper category of EFM PHYs is based on Digital Subscriber Line (DSL) PMDs defined for use in the access network according to ATIS T1, ETSI, and ITU-T standards. These systems are intended to be used in public as well as private networks; therefore they shall be capable of compliance with appropriate regulatory, governmental and regional requirements.

Unlike the specified copper categories for 10BASE-T, 100BASE-T, and 1000BASE-T, existing common carrier voice-grade copper has channel characteristics that are very diverse. Therefore it is conventional to discuss the channel behavior only in terms of averages, standard deviations and percentage worst case.

The 10PASS-TS and 2BASE-TL EFM Copper PHYs, in conjunction with the MAC specified in Clause 4 and Annex 4A, are used for point-to-point communications on a subscriber access network, typically between centralized distribution equipment, such as a Central Office (CO), and equipment located at the subscriber premises [Customer Premises Equipment, (CPE)].

For the 10PASS-TS and 2BASE-TL EFM Copper PHYs, two subtypes are defined: 10PASS-TS-O and 10PASS-TS-R are the subtypes of 10PASS-TS; 2BASE-TL-O and 2BASE-TL-R are the subtypes of 2BASE-TL. A connection can only be established between a 10PASS-TS-O PHY on one end of the voice-grade copper line, and a 10PASS-TS-R PHY on the other end, or between a 2BASE-TL-O PHY on one end and a 2BASE-TL-R PHY on the other end. In public networks, a 10PASS-TS-O or 2BASE-TL-O PHY is used at a CO, a cabinet or other centralized distribution point; a 10PASS-TS-R or 2BASE-TL-R PHY is used as CPE. In private networks, the network administrator will designate one end of each link as the network end. In this clause, 10PASS-TS-O and 2BASE-TL-O are collectively referred to as “CO-subtypes”; 10PASS-TS-R and 2BASE-TL-R are collectively referred to as “CPE-subtypes”. The CO and CPE subtypes of a 10PASS-TS or 2BASE-TL PHY may be implemented in a single physical device.

10PASS-TS and 2BASE-TL PHYs do not provide support for unidirectional links as described in 57.2.12. If a particular anomaly or failure occurs in either downstream or upstream, sublayer-specific signaling will alert the remote end of this condition. In the case of a sustained anomaly or failure, the link will reinitialize.

61.1.1 Scope

This clause defines the Physical Coding Sublayer (PCS) and Transmission Convergence (TC) sublayer for 2BASE-TL and 10PASS-TS. The PCS has similarities to other IEEE 802.3 PCS types, but also differs since new sublayers are added within the PCS sublayer to accommodate the operation of Ethernet over access network copper channels. The TC contains additional functions specific to the EFM Copper PHYs. This clause also defines the common startup and handshaking mechanism used by both PHYs. Parts of register 3.0, parts of register 3.4, and registers 3.60 through 3.73 specified in Clause 45 may be used to control the PCS specified in this clause. The remaining PCS registers defined in Clause 45 do not have any effect on the PCS specified in this clause. Parts of register 6.0 and registers 6.16 through 6.23 specified in Clause 45 may be used to control the TC sublayer specified in this clause.

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61.1.2 Objectives

The following are the objectives for 2BASE-TL and 10PASS-TS:

a) To provide 100 Mb/s burst data rate at the MII using Rate Matching.
b) To provide support for simultaneous transmission and reception without interference.
c) To provide for operating over unshielded voice grade twisted pair cable.
d) To provide a communication channel with a mean BER at the PMA service interface of less than 10^{-7} with a noise margin of 6 dB (10PASS-TS) or 5 dB (2BASE-TL).
e) To provide optional support for operation on multiple pairs.
f) To provide functional layering in the PCS which ensures compatibility with the layering and frame interfaces for xDSL systems, including a γ-interface based on that used for the PTM-TC sublayer as defined in ITU-T Recommendation G.993.1.

61.1.3 Relation of 2BASE-TL and 10PASS-TS to other standards

The relation of 2BASE-TL and 10PASS-TS to other standards is shown schematically in Figure 61–1.

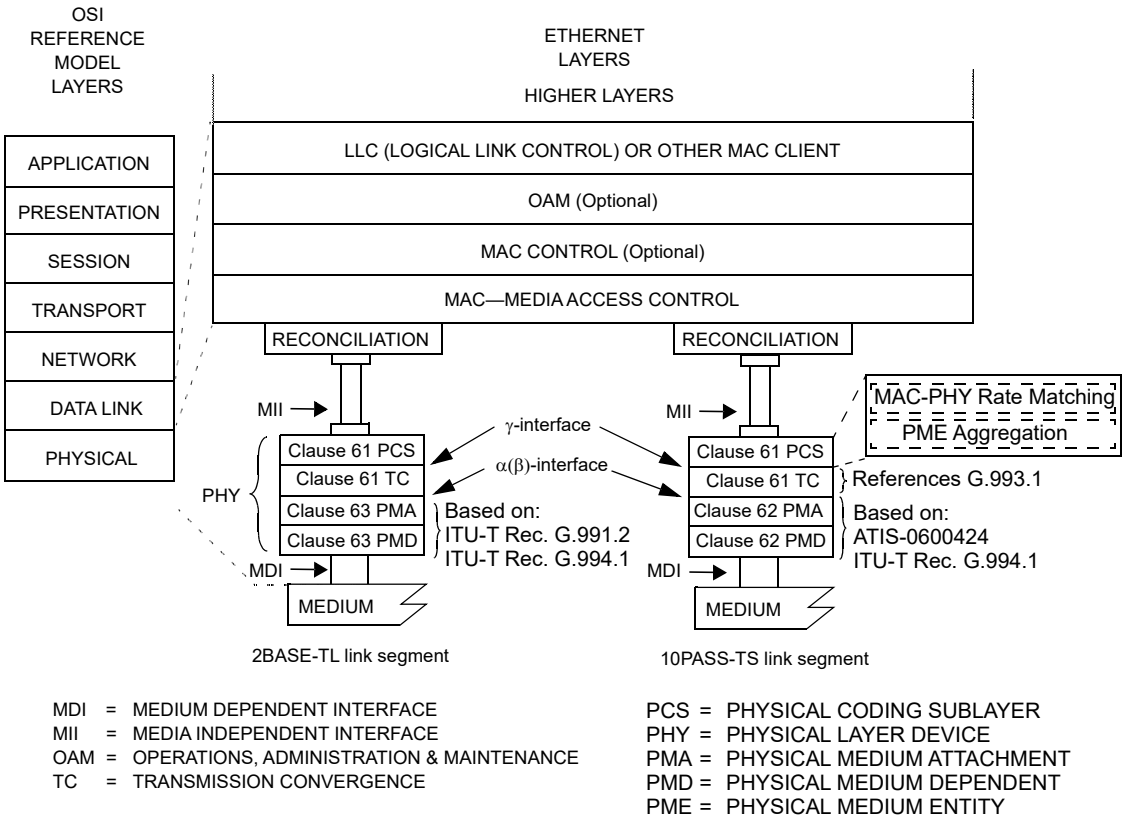

Figure 61–1—Relation of this clause to other standards

NOTE—The PCS shown in the 2BASE-TL PHY and the PCS shown in the 10PASS-TS PHY are two instances of one unique PCS, specified in this clause. The TC shown in the 2BASE-TL PHY and the TC shown in the 10PASS-TS PHY are two instances of one unique TC, specified in this clause.

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61.1.4 Summary

61.1.4.1 Summary of Physical Coding Sublayer (PCS) specification

The Physical Coding Sublayer (PCS) for 2BASE-TL and 10PASS-TS contains two functions: MAC-PHY rate matching and PME aggregation. The functional position of the PCS is shown in Figure 61–2.

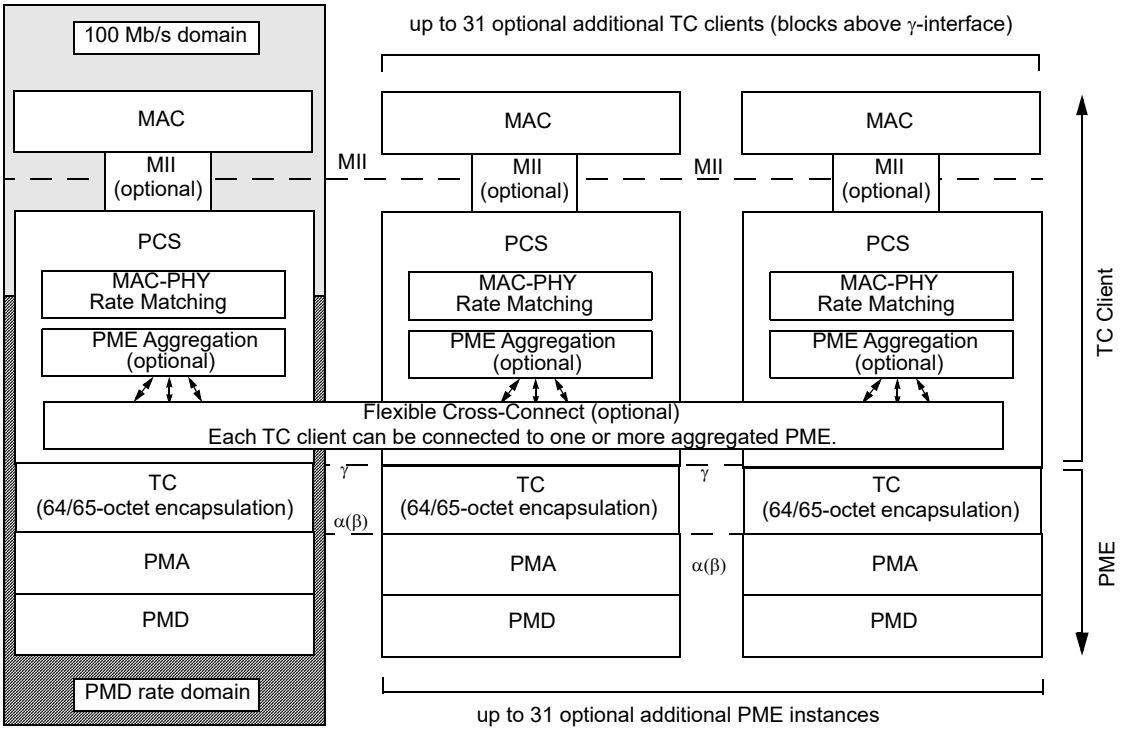

Figure 61–2—Overview of PCS functions

The γ-interface and α(β)-interface are specified in 61.3.1 and 61.3.2, respectively. They are generic interfaces used in various xDSL specifications, such as the ones referenced in Clause 62 and Clause 63. The α(β)-interface is a simple octet-synchronous data interface; the γ-interface adds protocol-awareness (in the case of the TC sublayer defined in this Clause, the γ-interface can signal packet boundaries).

The bit rates in the shaded area labeled "PMD rate domain" are derived from the DSL bit rates. Data is transferred across the γ-interface at the rate imposed by the lower layers. The bit rates in the shaded area labeled "100 Mb/s domain" are synchronous to the MII rate. Data is transferred across the MII at the rate of one nibble per MII clock cycle. The MAC-PHY rate matching function adjusts the inter packet gap so that the net data rate across these interface matches the sum of rates across the γ-interfaces.[115]

In the transmit direction, frames are transferred from the MAC to the PCS across the MII when the MAC-PHY rate matching function allows this. In the PCS, preamble and SFD octets are removed. If the optional PME aggregation function (PAF) is present, the MAC frame is fragmented by the PAF, and fragments are forwarded, optionally through a flexible cross-connect, towards each of the aggregated Physical Medium Entity (PME) instances via their γ-interfaces. If the PAF is not present, the data frame is forwarded to the TC sublayer via the γ-interface. The TC sublayer accepts data from the MAC-PHY rate matching function or the PAF, at the rate at which it can be processed by the TC sublayer, by asserting Tx_Enbl on the γ-interface.

[115]Bit rate domains and physical clock domains do not necessarily coincide. The TC sublayer receives a clock signal from the PMA via the α(β)-interface, and a clock signal from the optional PAF or the MAC-PHY Rate Matching function via the γ-interface. The TC provides matching between these two clock domains.

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In the receive direction the TC sublayer pushes data to the PAF (if present) or the MAC-PHY rate matching function by asserting Rx_Enbl on the γ-interface. If multiple links are aggregated, the PAF reassembles the received fragments into data frames. Preamble and SFD octets are generated and prepended to the data frame prior to passing it up to the MAC across the MII. The MAC-PHY Rate Matching function may delay the transfer of the frame to avoid simultaneous transfer of Transmit and Receive frames if required.

NOTE—The MAC_PHY rate matching function and PME Aggregation function both require some form of frame buffer for many implementations. It is recommended that these frame buffers should be sized to accommodate maximum length envelope frames (see 3.2.7).

61.1.4.1.1 Implementation of Media Independent Interface

10PASS-TS and 2BASE-TL specify the optional use of the MII electrical interface as defined in Clause 22 (see also 61.1.5.2). 10PASS-TS and 2BASE-TL do not utilize the MII management interface as described in 22.2.4. The use of the MDIO interface specified in Clause 45 or an equivalent management interface is recommended.

Notwithstanding the specifications in 22.2.2.9, CRS may be asserted by a full-duplex EFM Copper PHY to reduce the effective MAC rate to that of the PHY.

61.1.4.1.2 Summary of MAC-PHY Rate Matching specification

The 10PASS-TS and 2BASE-TL PCS is specified to work with a MAC operating at 100 Mb/s using the MII as defined in Clause 22. The PCS matches the MAC's rate of data transmission to the transmission data rate of the medium, if slower. This is achieved using deference as defined in Annex 4A.

The MAC transmits data at a rate of 100 Mb/s, which is buffered by the PCS before being transmitted onto the medium. Prior to transmission, the MAC checks the carrierSense variable (mapped from the MII signal CRS), and will not transmit another frame as long as carrierSense is asserted. In order to prevent the PCS's transmit buffer from overflowing, the PCS keeps CRS asserted until it has space to receive a maximum length frame. The PCS forces COL to logic zero to prevent the MAC from dropping the frame and performing a re-transmission.

The transmitter MAC-PHY Rate Matching function strips the Preamble and SFD fields from the MAC frame, and forwards the resulting data frame to the PME Aggregation Function or to the TC sublayer.

For reception the PHY buffers a complete frame, prepends the Preamble and SFD fields, and sends it to the MAC at 100 Mb/s.

It is recognized that some MAC implementations have to be configured for half duplex operation to support deference (according to 4.2.3.2.1), and that these may not allow the simultaneous transmission and reception of data while operating in half duplex mode. To permit operation with these MACs the PHY has an operating mode where MAC data transmission is deferred using CRS when received data is sent from the PHY to the MAC. This mode of operation is defined in Figure 61–8, which describes the MAC-PHY rate matching receive state diagram. This state diagram gives receive frames priority over transmitted frames to ensure the receive buffer does not overflow.

The definition of MAC-PHY rate matching is presented in 61.2.1.

61.1.4.1.3 Summary of PME Aggregation specification

An optional PME Aggregation Function (PAF) allows one or more PMEs to be combined together to form a single logical Ethernet link. The PAF is located in the PCS, between the MAC-PHY Rate Matching function and the TC sublayer. It interfaces with the PMEs across the γ-interface, and to the MAC-PHY Rate Matching function using an abstract interface. The definition of the PAF is presented in 61.2.2.

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61.1.4.1.4 Overview of management

Ethernet OAM (Clause 57) runs over a MAC service which uses a PHY consisting of either a single physical link, or more than one physical 2BASE-TL or 10PASS-TS links, aggregated as described in 61.2.2. The Ethernet OAM operates as long as there is at least one PME in the PHY that is operational. The physical xDSL PMEs in Clause 62 and Clause 63 each have their own management channel that operates per loop (eoc, VOC and IB for 10PASS-TS; EOC and IB for 2BASE-TL).

61.1.4.2 Summary of Transmission Convergence (TC) specification

The Transmission Convergence sublayer (TC) resides between the γ-interface of the PCS and α(β)-interface of the PMA. It is intended to convert the data frame to be sent into the format suitable to be mapped into PMA, and to recognize the received frame at the other end of the link. Since PMA and MII clocks may be unequal, the TC also provides clock rate matching. The definition of the TC sublayer is presented in 61.3.

61.1.4.3 Summary of handshaking and PHY control specification

Both 2BASE-TL and 10PASS-TS use handshake procedures defined in ITU-T G.994.1 at startup. Devices implementing both 2BASE-TL and 10PASS-TS port types may use ITU-T G.994.1 to determine a common mode of operation.

61.1.5 Application of 2BASE-TL, 10PASS-TS

61.1.5.1 Compatibility considerations

The PCS, TC, PMA, and the MDI are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the PCS, TC, and PMA in an application-dependent manner provided the MDI and MII specifications are met.

61.1.5.2 Incorporating the 2BASE-TL, 10PASS-TS PHY into a DTE

When the PHY is incorporated within the physical bounds of a DTE, conformance to the MII is optional, provided that the observable behavior of the resulting system is identical to that of a system with a full MII implementation. For example, an integrated PHY may incorporate an interface between PCS and MAC that is logically equivalent to the MII, but does not have the full output current drive capability called for in the MII specification.

61.1.5.3 Application and examples of PME Aggregation

The PME Aggregation Function defined in 61.2.2 allows multiple PME instances to be aggregated together to form one logical link underneath one MII (or MAC). Additionally, the control mechanism allows multi-MAC devices to be built with flexible connections between the MACs and the PMEs. Clause 45 defines a mechanism for addressing and controlling this flexible connectivity. The relationship between the flexible connectivity and the other functions within the PCS is shown in Figure 61–2.

The connection relationship between the PCS instances (including MIIs) and the PME instances is defined in two registers: PME_Available_register (see 45.2.3.29) and PME_Aggregate_register (see 45.2.3.30). The PME_Available_register controls which PMEs may be aggregated into a particular PCS (and MII). This register value is limited by the physical connectivity in the device, may be further constrained by management, and is additionally constrained as PMEs are aggregated into other PCSs (which causes their bit to be cleared to zero in the PCS instances that they are not aggregated into). The register represents the potential for connectivity into this PCS at the particular point in time. The PME_Aggregate_register indicates the actual connectivity, i.e., which PMEs are being aggregated into the particular PCS.

NOTE—The addressing of PCS instances is independent of the addressing of PME instances in order to support the flexible connectivity. Each PCS consumes one of the 32 available port addresses.

Bits corresponding to the same PME may appear in multiple PME_Available_registers but the PME_Aggregate_register for each MII shall be set such that each PME is only actively connected to at most

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one MII. A particular bit set in one PME_Aggregate_register shall exclude the same corresponding bit in all other PME_Aggregate_registers for the same MDIO connected system.

61.1.5.3.1 Addressing PCS and PME instances

The addressing of the MDIO management interface is defined in 45.1. It is assumed that the reader is familiar with the definition of this interface. The examples here assume that only three MMDs are used: PCS (MMD = 3), TC (MMD = 6), and PMA/PMD (MMD = 1). The combination of TC, PMA and PMD is shown as PME in Figure 61–3. The difference between these examples and the example shown in 45.1 is that the PCS instances are addressed independently of the PME instances. Up to 32 PCS instances and up to 32 PME instances may be addressed by one MDIO bus. These instances may make up one or more aggregateable subdomains. The connection of the MDIO bus to the MMDs is shown in Figure 61–3.

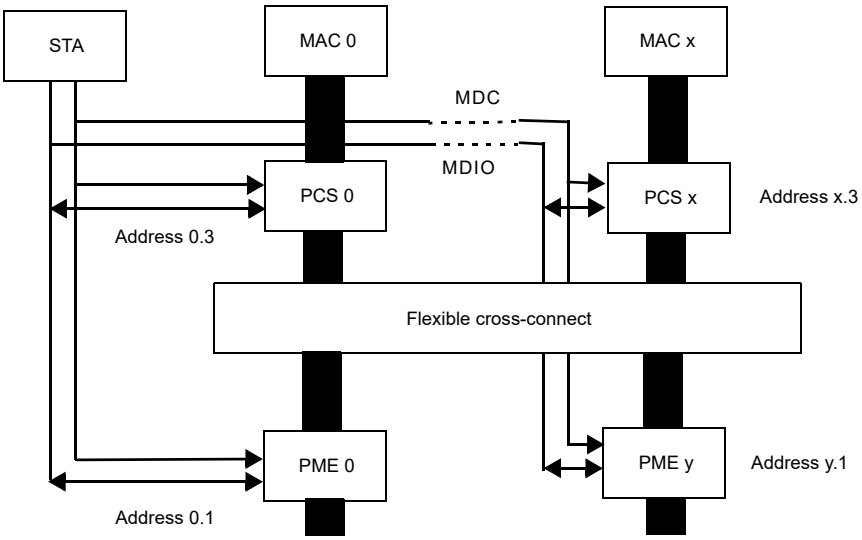

Figure 61–3—Connection of MDIO bus to MMD instances

In the example shown in Figure 61–3 there is no necessary connection between the PCS address and the PME address. The number of PCS instances may be different from the number of PME instances.

61.1.5.3.2 Indicating PME aggregation capability

The PME aggregation capability is indicated by the state of the PME_Available_register (see 45.2.3.29). An instance of this register is readable for each PAF instance *x* at register addresses *x*.3.62 and *x*.3.63. (Device address 3 of every port *x* is assigned to the PCS. The PAF specific registers reside under the *x*.3 register tree, because the PAF is part of the PCS as shown in Figure 61–2.) A bit is set in this register corresponding to the PME address for each PME which can be aggregated through the PAF in that PCS. Some examples are given that show register contents and connectivity for some popular configurations:

a) Simple two PME per MII connections, 32 PMEs are available for aggregation into 16 MIIs (PCS instances). PME_Available_register contents are shown in Table 61–1. A diagram of the connectivity is shown in Figure 61–4.
b) Pairs of 4-to-1 connections, 32 PMEs are available for aggregation into 16 MIIs (PCS instances) in a manner that allows each PME to connect to one of 2 MIIs and each MII to aggregate up to 4 PMEs. PME_Available_register contents are shown in Table 61–2. A diagram of the connectivity is shown in Figure 61–5.
c) 24-to-12 fully flexible connections, 24 PMEs are available for aggregation into 12 MIIs (PCS instances) in a manner that allows any PME to connect to any MII. PME_Available_register

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contents are shown in Table 61–3. No connectivity diagram is shown as any connection is possible between PMEs and MIIs.

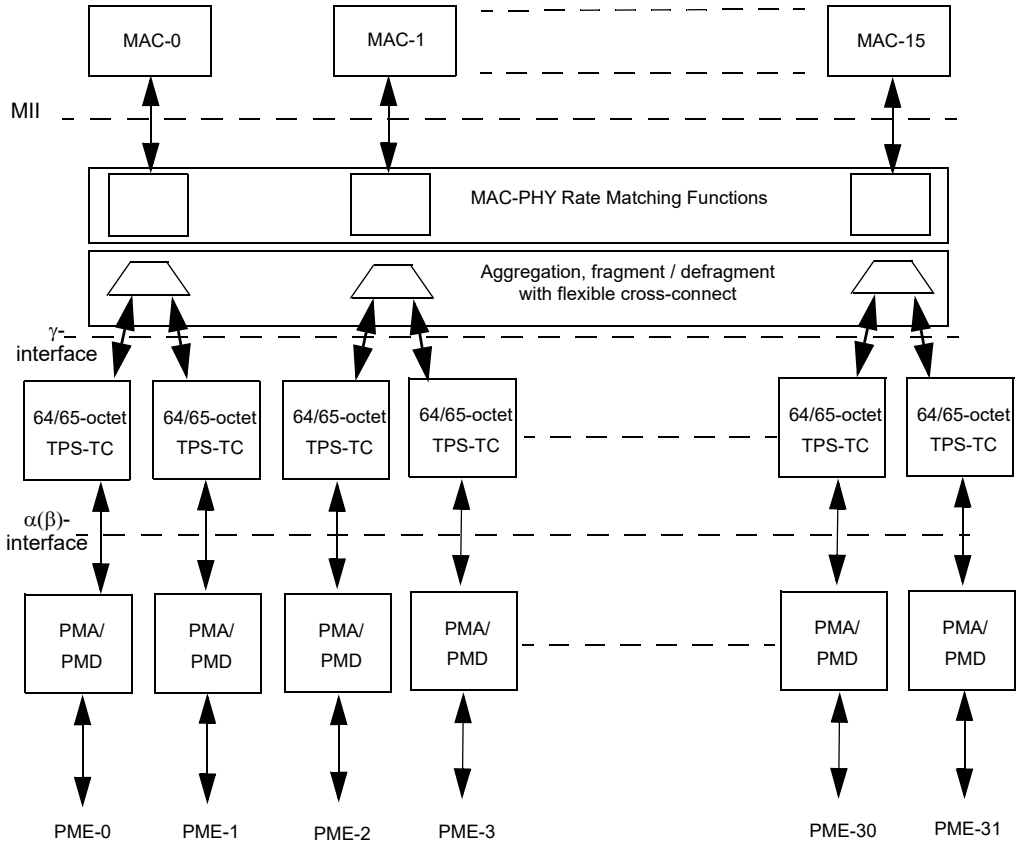

Figure 61–4—2 PME for each MII connectivity

Table 61–1—PME_Available_register contents (example a)

PME_Available_register	Contents
0.3.62 / 63	b11000000_00000000_00000000_00000000
1.3.62 / 63	b00110000_00000000_00000000_00000000
etc.	etc.
15.3.62 / 63	b00000000_00000000_00000000_00000011

Table 61–2—PME_Available_register contents (example b)[a]

PME_Available_register	Contents
0.3.62 / 63	b11110000_00000000_00000000_00000000
1.3.62 / 63	b11110000_00000000_00000000_00000000
etc.	etc.
15.3.62 / 63	b00000000_00000000_00000000_00001111

[a]A mapping in which the same PME is available for connection to several PCS instances (as shown) is only allowed at the CO-side.

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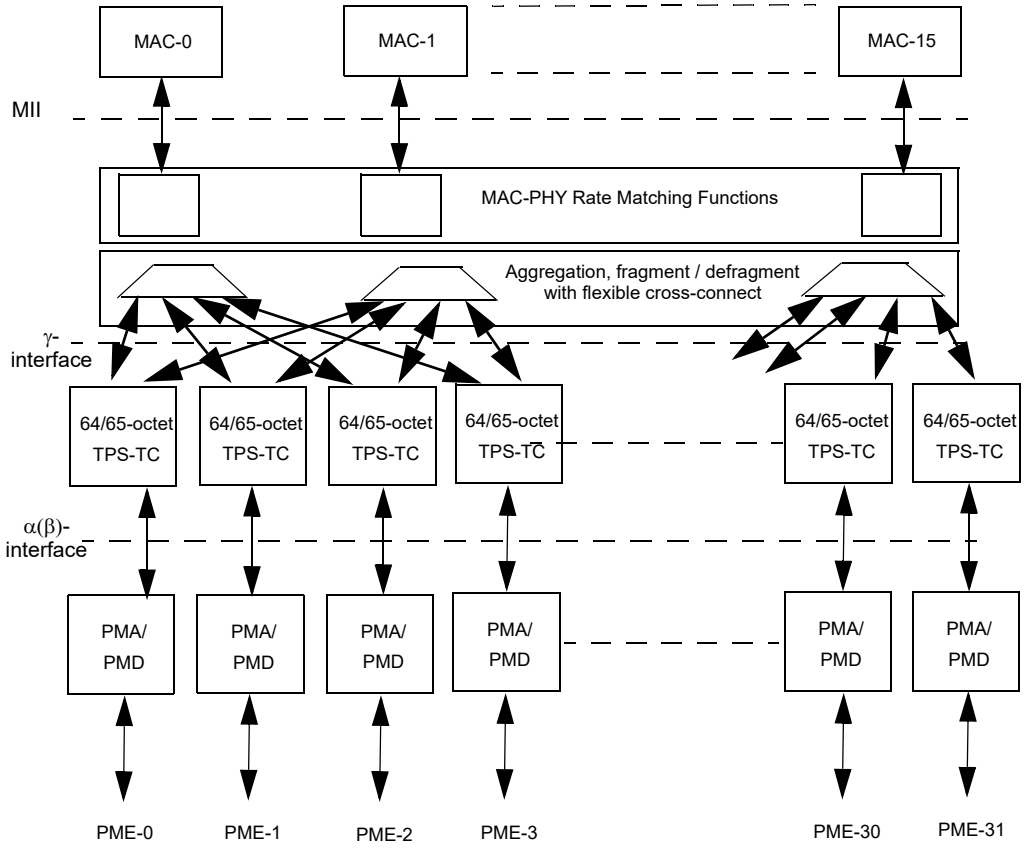

Figure 61–5—4 PME for each 2 MII connectivity

Table 61–3—PME_Available_register contents (example c)[a]

PME_Available_register	Contents
0.3.62 / 63	b11111111_11111111_11111111_00000000
1.3.62 / 63	b11111111_11111111_11111111_00000000
etc.	etc.
11.3.62/ 63	b11111111_11111111_11111111_00000000

[a]A mapping in which the same PME is available for connection to several PCS instances (as shown) is only allowed at the CO-side.

61.1.5.3.3 Setting PME aggregation connection

The PME aggregation connection is set using the PME_Aggregate_register (see 45.2.3.30). This register is writeable for each PCS instance (x) at register addresses x.3.64 and x.3.65. A bit is set in this register corresponding to the PME address for each PME that is to be aggregated through that PCS. Some examples are given that show register contents and connectivity for some popular configurations:

a) Simple two PME per MII connections (as shown in example a above), the first MII aggregates 2 PMEs, the second MII only connects through 1 PME, as does the sixteenth. PME_Aggregate_register contents are shown in Table 61–4.

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b) Pairs of 4-to-1 connections (as shown in example b above), the first MII aggregates 3 PMEs, the second MII only connects through 1 PME, the sixteenth MII aggregates 2 PMEs. PME_Aggregate_register contents are shown in Table 61–5.
c) 24-to-12 fully flexible connections (as shown in example c above), the first MII aggregates 5 PMEs, the second MII only connects through the 24th PME, the eleventh MII is not used, twelfth MII aggregates 2 PMEs. PME_Aggregate_register contents are shown in Table 61–6.

Table 61–4—PME_Aggregate_register contents (example a)

PME_Aggregate_register	Contents
0.3.64 / 65	b11000000_00000000_00000000_00000000
1.3.64 / 65[a]	b00010000_00000000_00000000_00000000
etc.	etc.
15.3.64 / 65	b00000000_00000000_00000000_00000010

[a]The PME Aggregation functions have to be performed when PAF_enable is set, even if only 1 bit is set in the PME_Aggregate_register.

Table 61–5—PME_Aggregate_register contents (example b)

PME_Aggregate_register	Contents
0.3.64 / 65	b11100000_00000000_00000000_00000000
1.3.64 / 65[a]	b00010000_00000000_00000000_00000000
etc.	etc.
15.3.64 / 65	b00000000_00000000_00000000_00000110

[a]The PME Aggregation functions have to be performed when PAF_enable is set, even if only 1 bit is set in the PME_Aggregate_register.

Table 61–6—PME_Aggregate_register contents (example c)

PME_Aggregate_register	Contents
0.3.64 / 65	b11111000_00000000_00000000_00000000
1.3.64 / 65[a]	b00000000_00000000_00000001_00000000
etc.	etc.
10.3.64 / 65	b00000000_00000000_00000000_00000000
11.3.64 / 65	b00000000_00000000_00000110_00000000

[a]The PME Aggregation functions have to be performed when PAF_enable is set, even if only 1 bit is set in the PME_Aggregate_register.

61.1.5.4 Support for handshaking

It is the goal of the ITU-T that all specifications for digital transceivers for use on public telephone network copper subscriber lines use ITU-T G.994.1 for startup. ITU-T G.994.1 procedures allow for a common startup mechanism for identification of available features, exchange of capabilities and configuration information, and selection of operating mode. As the two loop endpoints are usually separated by a large distance (e.g., in separate buildings) and often owned and installed by different entities, ITU-T G.994.1 also aids in diagnosing interoperability problems. ITU-T G.994.1 codespaces have been assigned by ITU-T to ATIS T1, ETSI, and IEEE 802.3 in support of this goal.

The description of how ITU-T G.994.1 procedures are used for Ethernet in the First Mile handshaking and PHY control are contained in 61.4.

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61.2 PCS functional specifications

61.2.1 MAC-PHY Rate Matching functional specifications

61.2.1.1 MAC-PHY Rate Matching functions

The PHY shall use CRS to match the MAC's faster rate of data transmission to the PHY's slower rate.

Upon receipt of a MAC frame on the MII, the PHY shall discard the Preamble and SFD fields, and transmit the resulting data frame across the physical link.

The PHY shall prepend the Preamble and the SFD fields to a received frame before sending it to the MAC.

The PHY shall support a mode of operation where it does not send data to the MAC while the MAC is transmitting (see MII receive during transmit register, defined in 45.2.3.28).

If the PAF is disabled or not present, transmit frames shall not be forwarded to the TC sublayer unless TC_link_state is true for the whole frame. If the PAF is enabled, transmit fragments shall not be forwarded from the PAF to a TC sublayer unless the TC_link_state value of that TC sublayer instance is true for the whole fragment.

NOTE—This implies that in the absence of an active PAF, frames being transmitted over the MII when TC_link_state becomes true are never forwarded to the TC sublayer. A frame being transmitted over the MII when TC_link_state becomes false is aborted.

61.2.1.2 MAC-PHY Rate Matching functional interfaces

61.2.1.2.1 MAC-PHY Rate Matching – MII signals

MII signals are defined in 22.2.2 and listed in Table 23–1 in 23.2.2.1.

COL shall be forced to logic zero by the PCS.

CRS behaves as defined in 61.2.1.3.2.

61.2.1.2.2 MAC-PHY Rate Matching–Management entity signals

See 61.2.3.

61.2.1.3 MAC-PHY Rate Matching state diagrams

61.2.1.3.1 MAC-PHY Rate Matching state diagram constants

No constants are defined for the MAC-PHY rate matching state diagrams.

61.2.1.3.2 MAC-PHY Rate Matching state diagram variables

CRS
: CRS signal of the MII as specified in Clause 22. It is asserted when either of crs_tx or crs_rx are true: CRS ⇐ crs_tx + crs_rx

crs_and_tx_en_infer_col
: True if a reduced-pin MAC-PHY interface is present that infers a collision when TX_EN and CRS are both true simultaneously.

crs_rx
: Asserted by the MAC-PHY rate matching receive state diagram to control CRS

crs_tx
: Asserted by the MAC-PHY rate matching transmit state diagram to control CRS

power_on
: 'power_on' is true while the device is powering up. It becomes false once the device has

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reached full power. Values:
FALSE; The device is completely powered (default).
TRUE; The device has not been completely powered.

Reset
: True when the PCS is reset via control register bit 3.0.15.

RX_DV
: RX_DV signal of the MII as specified in Clause 22

rx_frame_available
: Set when the PHY's receive FIFO contains one or more complete frames

transferFrameCompleted
: Variable of type Boolean
TRUE if the transmission of the received frame over the MII has been completed,
FALSE otherwise.
The variable returns to the default state (FALSE) upon entry into any state.

tx_buffer_available
: Set when the PHY's transmit FIFO has space to receive a maximum length packet from the MAC

TX_EN
: TX_EN signal of the MII as specified in Clause 22

tx_rx_simultaneously
: False if the MAC is configured in half duplex mode to support deference and it is not capable of transmitting and receiving simultaneously in this mode.

61.2.1.3.3 MAC-PHY Rate Matching state diagram timers

ipg_timer
: Timer used to generate a gap between receive packets across the MII.
Duration: 960 ns, tolerance ±100 ppm.

rate_matching_timer
: Timer used in rate matching state diagram
Duration: 1120 ns, tolerance ±100 ppm.

The rate_matching_timer operates in a manner consistent with 14.2.3.2. The timer is restarted on entry to the WAIT_FOR_TIMER_DONE state with the action: 'Start rate_matching_timer'. It is then tested in the exit condition with the expression "rate_matching_timer_done".

The duration is set to 1120 ns to allow 960 ns for the inter frame gap plus 160 ns for the MAC to recognize CRS. 160 ns is equivalent to 16 bit times and is consistent with the assumptions about MAC performance listed in Table 21–2 in 21.7.

61.2.1.3.4 MAC-PHY Rate Matching state diagram functions

transferFrame()
: This function transmits a packet to the MAC across the MII, according to the MII protocol as described in 22.2. This function generates RX_DV to delimit the frame in accordance with 22.2.2.6. Upon completion of frame transfer to the MAC, this function sets the variable transferFrameCompleted to TRUE.

61.2.1.3.5 MAC-PHY Rate Matching state diagrams

The state diagrams for the MAC-PHY Rate Matching functions are shown in Figure 61–6, Figure 61–7, and Figure 61–8.

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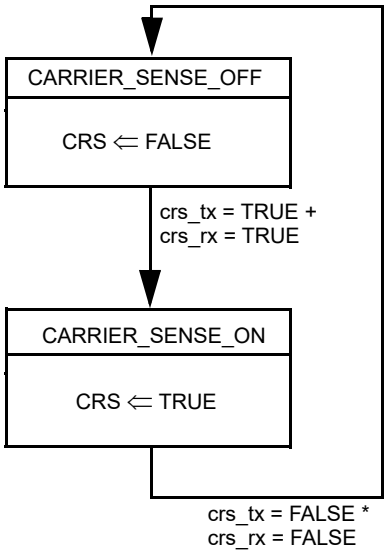

Figure 61–6—Carrier Sense state diagram

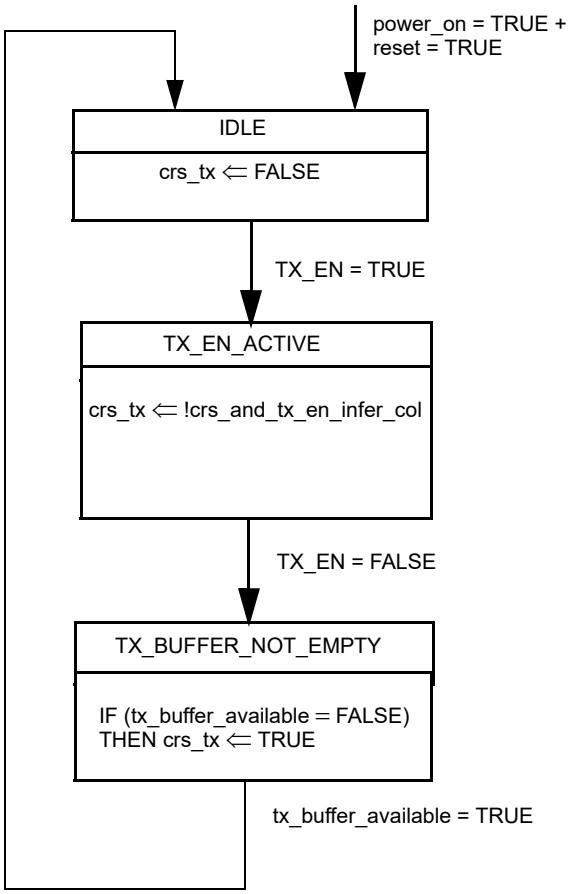

Figure 61–7—MAC-PHY rate matching transmit state diagram

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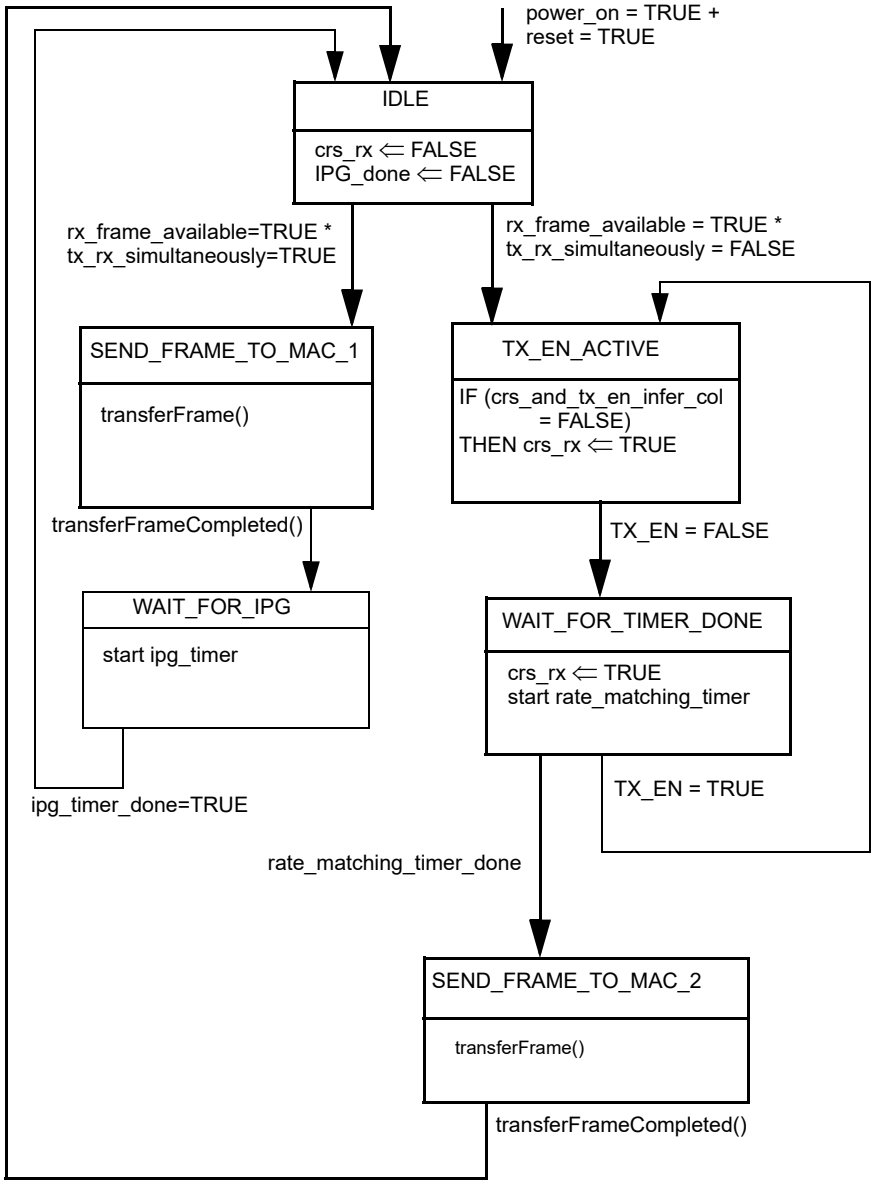

Figure 61–8—MAC-PHY rate matching receive state diagram

61.2.2 PME Aggregation functional specifications

This subclause defines an optional PME Aggregation Function (PAF) for use with Ethernet MACs in EFM copper PHYs. PME Aggregation allows one or more PMA/PMDs to be combined together to form a single logical Ethernet link.

The PAF is located between the MAC-PHY Rate Matching function and the TC sublayer as shown in Figure 61–2. The PAF interfaces with the TC sublayer instances across the γ-interface. The PAF interfaces to the MAC-PHY Rate Matching function using an abstract interface whose physical realization is left to the implementer, provided the requirements of this standard are met.

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The PME Aggregation function has the following characteristics:

a) Supports aggregation of up to 32 PMA/PMDs
b) Supports individual PMA/PMDs having different data rates
c) Ensures low packet latency and preserves packet sequence
d) Scalable and resilient to PME failure
e) Independent of type of EFM copper PHY
f) Allows vendor discretionary algorithms for fragmentation

61.2.2.1 PAF Enable and Bypass

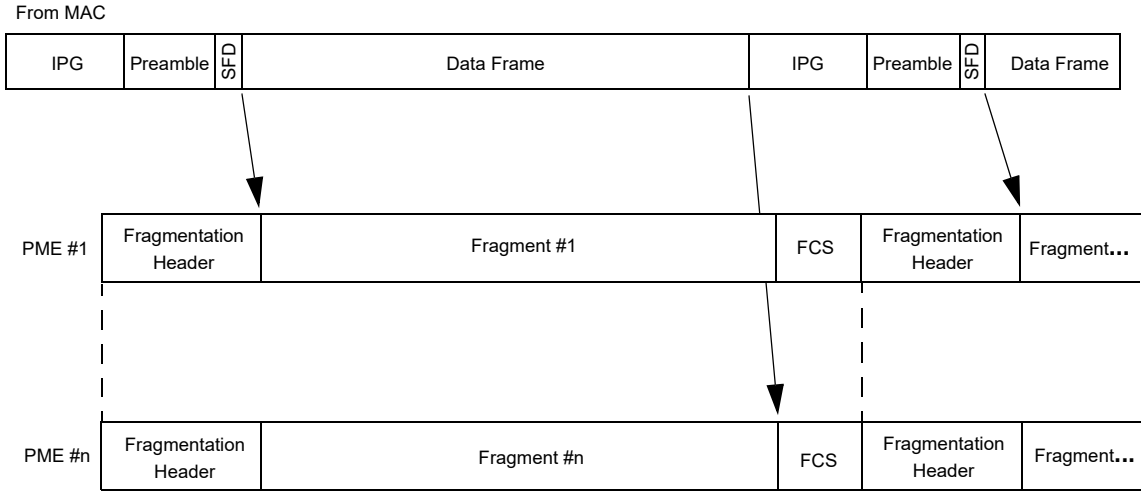
For systems that do not have the ability to aggregate loops PAF_available will not be asserted. Additionally, a system may have PAF_available asserted but PAF_enable will be deasserted to indicate that aggregation is not activated.

In both of these cases, the entire data frame is passed across the γ-interface to the TC sublayer without any fragmentation and without fragmentation header. On the receive end, entire data frames are transferred from the γ-interface to the MAC-PHY rate matching function without any reference to the PAF error detecting rules (see 61.2.2.7). If an error has been detected by the FCS in the TC then the MAC-PHY rate matching function shall assert RX_ER during at least one octet of the frame across the MII.

Systems that have the ability to aggregate but are not enabled for aggregation will have the connectivity between the PCS and one PME set either by default, by local management (for CO-subtype devices) or by remote management (for CPE-subtype devices). This will define which γ-interface is used for the transfer of non-fragmented frames. Refer to 61.2.2.8.3 for the function of PAF_available and PAF_enable and Clause 45 for access to these registers.

61.2.2.2 PME Aggregation functions

The PME Aggregation functions provide a fragmentation procedure at the transmitter and a reassembly procedure at the receiver. The fragmentation and reassembly procedures take a data frame and partition it into one or more fragments as shown in Figure 61–9. Each fragment is given a fragmentation header and transmitted over a specific TC sublayer instance. A Frame Check Sequence, known as the TC-CRC, is added to each fragment by the TC sublayer. The fragmentation header has the format shown in Figure 61–10. Short data frames can be transported over a single fragment, and consequently both StartOfPacket and EndOfPacket can be set to '1' simultaneously.



NOTE—This is one example of how a frame may be fragmented across multiple PMEs.

Figure 61–9—Data frame fragmentation

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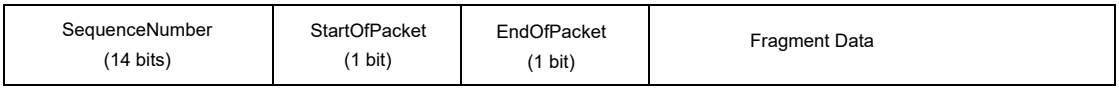

Figure 61–10—Fragment format

61.2.2.3 PME Aggregation Transmit function

The PME Aggregation transmit functions uses the following algorithm:

a) Select an active PME (i.e., one with TC_link_state asserted, see 61.3.1) for the next transmission.
b) Select the number of octets to transmit on that PME (shall not be less than minFragmentSize nor greater than maxFragmentSize, see 61.2.2.6).
c) Increment by one (modulo 2^{14}) and set fragment sequence number in the Fragmentation Header. There is a single sequence number stream for each aggregation, not one per PME. It is this sequence number stream that the receiver uses for fragment reassembly.
d) Set the start-of-packet and end-of-packet bits in the Fragmentation Header as appropriate.
e) Transmit fragment to the TC sublayer.

It is important to note that the selection of the next PME to use in transmission [step a)] and the number of octets to transmit [step b)] is implementation dependent. However, implementations shall follow the restrictions as outlined in 61.2.2.6.

61.2.2.4 PME Aggregation Receive function

The PME aggregation receive function requires per-PME queues as well as a per-MAC fragment buffer for fragment reassembly. The algorithm assumes only "good" fragments are placed on the per-PME receive queues ("bad" fragments are discarded according to the rules in 61.2.2.7).

The sequence number rolls over after it reaches the maximum value, thus all sequence number comparisons shall use "split horizon" calculations. Split horizon calculations are defined for comparisons that are valid for numbers that roll over after reaching the maximum value. Generically, "x is less than y" is defined as $x < y \le x +$ (maxSequenceNumber+1)/2.

61.2.2.4.1 Expected sequence number

During initial startup and in the event of certain errors, the receive algorithm has to determine which sequence number is expected next (expectedFragmentSequenceNumber). When the link state is changed to UP, the expected sequence number is unknown and no errors in fragment sequencing (see 61.2.2.7.2) shall be recorded.

61.2.2.4.2 PME Aggregation Receive function state diagram variables

The following variables are used in the PME Aggregation Receive function state diagram.

allQueuesNonEmpty
: variable of type Boolean that indicates whether any active queue is currently empty.
TRUE if none of the active queues is currently empty
FALSE if at least one active queue is currently empty

expectedFragmentSequenceNumber
: the sequence number expected in the receive process that would not result in a fragment error, initialized to the smallest sequence number of fragments at the head of per-PME queues when either all active queues are non-empty or at least one queue has been non-empty for maxDifferentialDelay bit times at the bit rate of the PMD associated with that queue

frameLengthOverflow
: variable of type Boolean, indicating that the reassembly buffer is overflowing due to a received frame that is too long, as described in 61.2.2.7.3.

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TRUE if the overflow condition exists
FALSE during normal operation

missingStartOfPacket
: variable of type Boolean, indicating that a fragment was received with the StartOfPacket bit deasserted while the packet assembly function was between frames (i.e., waiting for a Start of Packet).

nextFragmentSequenceNumber
: smallest sequence number of fragments at the head of per-PME queues

noFragmentProcessed_Timer
: variable of type Boolean that indicates whether at least one active queue has been non-empty for maxDifferentialDelay bit times at the bit rate of the PMD associated with that queue. Each fragment processed on any queue restarts all per-queue timers.
TRUE if a timeout of maxDifferentialDelay bit times has expired
FALSE if the timeout of maxDifferentialDelay bit times has not yet expired

oneQueueNonEmpty_Timer
: variable of type Boolean that indicates whether at least one active queue has been non-empty for at least maxDifferentialDelay bit times.
TRUE if at least one active queue has been non-empty for at least maxDifferentialDelay bit times
FALSE otherwise

smallestFragmentSequenceNumber
: smallest sequence number of fragments at the head of per-PME queues

unexpectedEndOfPacket
: variable of type Boolean, indicating that a fragment was received with the EndOfPacket bit asserted and the StartofPacket bit deasserted while the packet assembly function was between frames (i.e., waiting for a Start of Packet)

unexpectedStartOfPacket
: variable of type Boolean, indicating that a fragment is received with the StartOfPacket bit asserted while the packet assembly function was mid-frame (i.e., waiting for an End of Packet)

The following functions are used in the PME Aggregation Receive function state diagram.

errorDetection()
: function comprising the process described in 61.2.2.7.2

fragmentError()
: function comprising the process described in 61.2.2.7.3

61.2.2.4.3 PME Aggregation Receive function state diagram

The receive function executes the algorithm as shown in Figure 61–11. The initial state of the state diagram is INITIALIZING. This state is entered when at least one TC_link_state is asserted for the first time after system power-on, and each time when at least one TC_link_state is asserted after all having been deasserted for any reason.

61.2.2.4.4 PME Aggregation Receive function state diagram description

Aggregation receive algorithm is as follows:

a) Determine the nextFragmentSequenceNumber via the algorithm in 61.2.2.4.1.
b) If the nextFragmentSequenceNumber is equal to the expectedFragmentSequenceNumber, process that fragment and continue to step c). If (nextFragmentSequenceNumber is less than expectedFragmentSequenceNumber) or (all the active PME queues are non-empty and nextFragmentSequenceNumber ≠ expectedFragmentSequenceNumber) or (any PME queue has been non-empty for maxDifferentialDelay bit times without any fragment being processed) follow the fragment sequence error handling rules described in 61.2.2.7.2 before returning to normal fragment processing.

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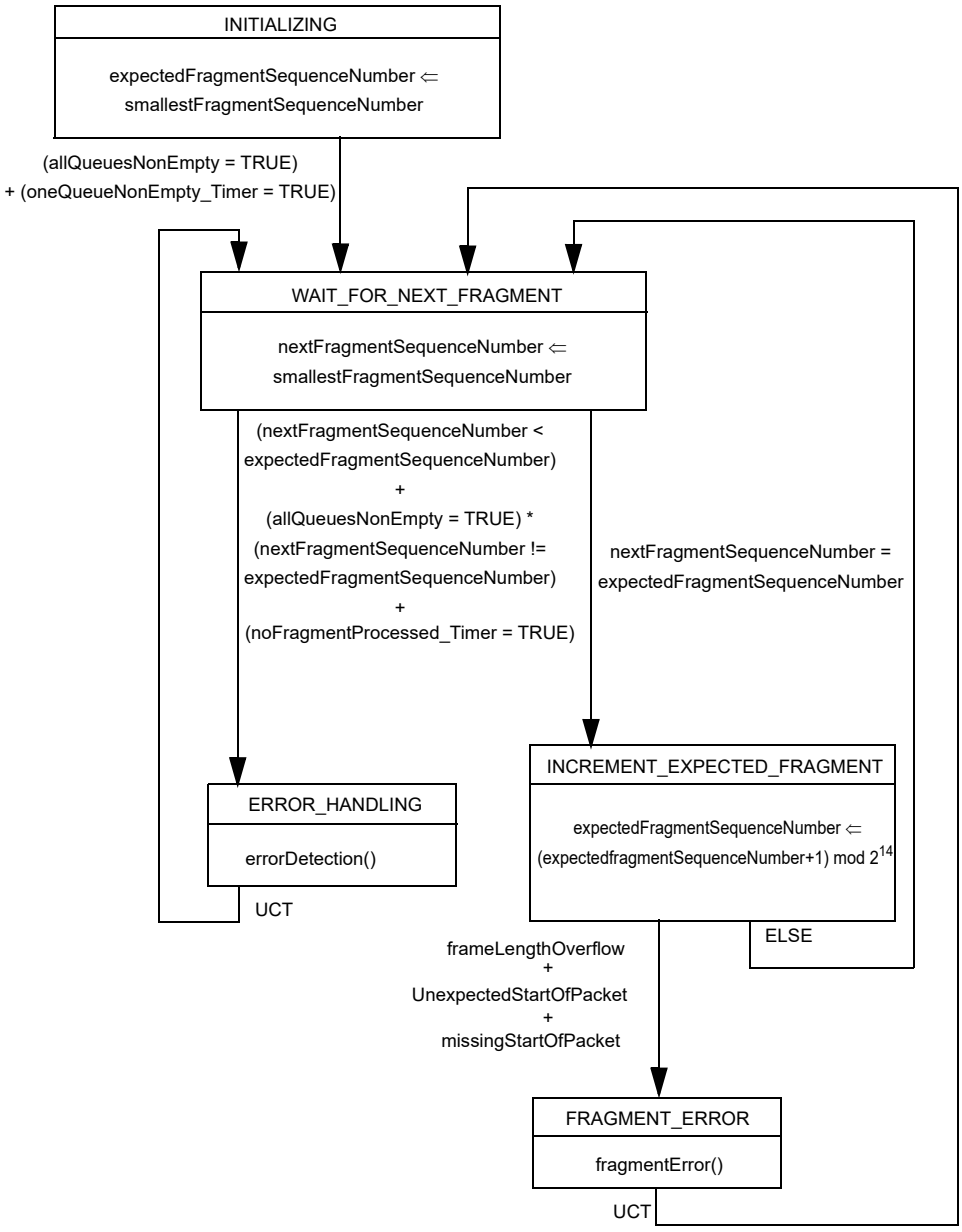

Figure 61–11—Aggregation receive function

c) Accept the fragment into the fragment buffer. If (accepting the fragment into the fragment buffer causes a frame length overflow) or (the fragment is an unexpected start of packet) or (the fragment is an unexpected end of packet) or (the fragment has the StartOfPacket bit deasserted when the start of a new packet is expected) then follow the error handling procedures described in 61.2.2.7.3. Else if that fragment is an end-of-packet, pass the packet to the MAC-PHY Rate Matching layer.
d) Increment (modulo 2^{14}) the expectedFragmentSequenceNumber.
e) Repeat processing.

61.2.2.5 PME Aggregation restrictions

In order to guarantee correct receiver operation, a transmitter has to ensure that pairs in an aggregate group obey certain restrictions.

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NOTE 1—These restrictions ensure that buffer sizes for receivers of 2^{14} bits per PME are sufficient.

One factor is the differential latency between multiple PMEs in an aggregated group. Differential latency measures the variation in the time required to transmit across different PMEs. To normalize the latency measurement for high and low speed links it is measured in bit times. A differential latency between two PMEs is defined as the number of bits, N, that can be sent across the fast link, in the time that it takes one maxFragmentSize fragment to be sent across the slow link. Large differential latencies generate greater variance in bit delivery times across aggregated PMEs, which in turn require large sequence number ranges. The PMD control of aggregated links controls the maximum latency difference between any two aggregated links. This is achieved by configuring the bit rate, error correction and interleaving functions in the PMA/PMD of each link. The burst noise protection offered by the error correction and interleaving[116] functions is directly proportional to the latency, therefore it is logical that multiple aggregated links in the same environment should be optimized to have similar latencies. Differences in electrical length will not contribute significantly to the differential latency; no additional per-PME buffer size is required for this variation.

NOTE 2—The value for differential latency for two identical links will be 4096 bit times because the definition includes the length of a maximum size fragment.

The speed ratio of the links also restricts what PMEs can be aggregated together. The speed ratio is defined as the ratio of the bit rate of the faster link divided by the bit rate of the slower link.

The restrictions that govern which PMEs can be aggregated are as follows:

a) The differential latency between any two PMEs in an aggregated group shall be no more than maxDifferentialDelay.
b) The highest ratio of speeds between any two aggregated links shall be maxSpeedRatio. A speed ratio of 4 may only be used if the latency is controlled to meet the restriction.

Table 61–7 specifies the values for constants maxDifferentialDelay and maxSpeedRatio.

Table 61–7—PME Aggregation constants

Constant name	Value
maxDifferentialDelay	15 000 bit times
maxSpeedRatio	4

61.2.2.6 PME Aggregation transmit function restrictions

There are factors that limit the freedom of the transmission algorithm specified in 61.2.2.3.

A first factor is the size of the fragments being transmitted across the PMEs. Very small fragments require larger sequence number ranges as there can be more fragments within the same number of bit times.

Another restriction on the size of the fragments, is that fragments shall be a multiple of 4 octets in size when possible.

The restrictions for the transmission algorithm in 61.2.2.3 are:

a) Fragments shall not be less than minFragmentSize not including PAF header.

[116]Interleaving is the relevant issue here, since it affects latency. While 2BASE-TL does not have block error correction, it does use trellis coding, which is sometimes considered forward error correction.

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b) Fragments shall not be more than maxFragmentSize not including PAF header.
c) The fragment size, not including PAF header, shall be a multiple of 4 octets except for the last fragment of a data frame.

NOTE—A fragment size of maxFragmentSize may only be used if the latency is controlled to meet the restriction a) in 61.2.2.5.

These restrictions allow the use of a 14-bit sequence number space. As a consequence, the maximum sequence number is $2^{14} - 1$ (maxSequenceNumber).

Table 61–8 specifies the values for constants maxFragmentSize and minFragmentSize.

Table 61–8—Fragment size constants

Constant name	Value
maxFragmentSize	512 octets
minFragmentSize	64 octets

61.2.2.7 Error-detecting rules

There are three classes of error detected by the PAF: Errors during fragment reception; Errors in fragment sequencing; and Errors during packet reassembly. In the case of an error detected by the PAF, it sends the frame or part of frame to the MAC with RX_ER asserted. When the PAF is unable to reconstruct or partially reconstruct a frame due to such errors, it sends a garbage frame up to the MAC, in order to allow higher-layer event counters to register the error. The garbage frame shall consist of 64 octets of 00 (including CRC). Preamble and SFD are prepended before the frame is sent to the MII according to 61.2.1.1.

The rules described in this subclause are applied by the functions errorDetection() and fragmentError() referenced in Figure 61–11.

61.2.2.7.1 Errors during fragment reception

The receive TC function passes all decapsulated fragments to the PAF across the γ-interface. If the TC detects an error in the encapsulation, it asserts Rx_Err on the γ-interface. If the TC detects an error in the TC-CRC, it asserts Rx_Err on the γ-interface. Asserting Rx_Err during fragment reception invalidates the entire fragment.

For each PMA α(β)-interface, the per-PMA buffering mechanism shall discard the fragment if any of the following conditions occur:

a) Rx_Err is asserted during the reception of the fragment across the γ-interface.
b) The fragment is too small — less than minFragmentSize as defined in 61.2.2.6.
c) The fragment is too large — more than maxFragmentSize as defined in 61.2.2.6.
d) The fragment would cause the per-PMA received buffer to overflow.

The PAF shall then assert one of the following per-PMA error flags as appropriate:

— TC_PAF_RxErrorReceived
— TC_PAF_FragmentTooSmall
— TC_PAF_FragmentTooLarge
— TC_PAF_Overflow

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61.2.2.7.2 Errors in fragment sequencing

If nextFragmentSequenceNumber is outside the range (expectedFragmentSequenceNumber through expectedFragmentSequenceNumber + (maxSequenceNumber+1)/2) then assert PAF_BadFragmentReceived. Discard the fragment, do not increment ExpectedFragmentSequenceNumber.

If all active PMA buffers are non empty and nextFragmentSequenceNumber is greater than expectedFragmentSequenceNumber then assert PAF_LostFragment, set expectedFragmentSequenceNumber equal to nextFragmentSequenceNumber.

If any PMA buffer is non empty for maxDifferentialDelay bit times (for that PMA/PMD) and no fragment is transferred then assert PAF_LostFragment, set expectedFragmentSequenceNumber equal to nextFragmentSequenceNumber.

Having detected one of the above fragment sequencing errors, the packet assembly function shall act as follows:

— If the packet assembly function was mid-frame (i.e., waiting for an End of Packet), the first part of the frame shall be transferred across the MII, then assert RX_ER signal on the MII, abort frame transfer and flush PMA buffers until the next Start of Packet is received.
— If the packet assembly function was between frames (i.e., waiting for a Start of Packet), assert RX_ER signal on the MII and send a garbage frame as defined in 61.2.2.7 to the MAC.

61.2.2.7.3 Errors in packet reassembly

If a fragment is received with the StartofPacket bit deasserted while the packet assembly function was between frames (i.e., waiting for a Start of Packet), discard the offending fragment, assert RX_ER signal on the MII and send a garbage frame as defined in 61.2.2.7 to the MAC. Assert PAF_LostStart.

If a fragment is received with the StartOfPacket bit asserted while the packet assembly function was mid-frame (i.e., waiting for an End of Packet), the first part of the frame shall be transferred across the MII, then assert RX_ER signal on the MII, abort frame transfer and flush the PMA buffers, starting the next frame with the Start of Packet fragment just received. Assert PAF_LostEnd.

If a fragment is received while the packet assembly function was mid-frame (i.e., waiting for an End of Packet) and would cause the frame size to exceed the maximum supported frame size (see 4.2.4.2.1) then the first part of the frame, excluding the error causing fragment, shall be transferred across the MII, then assert RX_ER signal on the MII, abort frame transfer and flush PMA buffers until the next Start of Packet is received. Assert PAF_LostEnd.

61.2.2.8 PME aggregation functional interfaces

The PAF interfaces with the TC sublayer instances across the γ-interface. The PAF interfaces to the MAC-PHY Rate Matching function using an abstract interface whose physical realization is left to the implementer, provided the requirements of this standard are met.

61.2.2.8.1 PME aggregation–γ-interface signals

The PAF interfaces with the PMA/PMDs across the γ-interface. The γ-interface specification is defined in 61.3.1. This subclause specifies the data, synchronization and control signals that are transmitted between the TC sublayer and the PAF.

61.2.2.8.2 PME aggregation–management entity signals

The management entity signals pertaining to PME aggregation are specified in 61.2.3.

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61.2.2.8.3 PME aggregation register functions

If an MDIO interface is provided (see Clause 22 and Clause 45), PME aggregation registers are accessed via that interface. If not, it is recommended that an equivalent access be provided.

Clause 45 defines one bit each in the EFM 10P/2B capability register and the 10P/2B PCS control register to control the PAF function (see 45.2.3.27 and 45.2.3.28 respectively). PAF_available is used to indicate that the system has the capability to aggregate PMEs, PAF_enable is used to control whether this ability is enabled or not. In all cases, the PAF_available bit is read-only; the PAF_enable bit is read-only when the PAF_available bit is not asserted.

For CO-subtype devices, both the PAF_available and the PAF_enable bits are only accessible locally, the PAF_enable bit is writeable.

For CPE-subtype devices, both the PAF_available and the PAF_enable bits are locally read only and remotely readable. Additionally, the PAF_enable bit is remotely writeable.

Clause 45 defines access to two registers which relate to the PME aggregation function: the PME_Available_register (see 45.2.3.29) and the PME_Aggregate_register (see 45.2.3.30). Additionally the remote_discovery_register and Aggregation_link_state_register shall be implemented.

NOTE—The remote_discovery_register is a variable which is defined for CPE-subtypes only. It is used during the PME aggregation discovery process. The Aggregation_link_state_register is a variable with significance for the PCS only. These variables have no associated management interface registers.

The PME_Available_register is read-only for CO-subtype and may be writeable for CPE-subtype (in order to restrict CPE-subtype connection capability according to 45.2.3.29). It indicates whether an aggregateable link is possible between this PCS and multiple PMDs. For a device that does not support aggregation of multiple PMEs, a single bit of this register shall be set and all other bits clear. The position of bits indicating aggregateable PME links correspond to the PMA/PMD sub-address defined in Clause 45.

For CPE-subtype devices, the PME_Available_register may optionally be writeable by the local management entity. The reset state of the register reflects the capabilities of the device. The management entity (through Clause 45 access) may clear bits which are set, in order to limit the mapping between MII and PME for PME aggregation. For CPE-subtype devices, PMD links shall not be enabled (such that it shall not respond to or initiate any G.994.1 handshaking sessions, on any of its PMEs) until the PME_Available register has been set to limit the connectivity such that each PME maps to at most one MII (see 45.2.3.29). This condition is necessary so that remote commands from the network-end which affect PCS registers have a defined target. PMDs that are not associated to any PCS shall not respond to or initiate any G.994.1 handshaking signals. Multiple PMEs per MII are allowed.

The PME_Aggregate_register is defined in Clause 45. For CO-subtype devices, access to this register is through Clause 45 register read and write mechanisms. For CPE-subtype devices the register may be read locally through Clause 45, and reads and writes shall be allowed from remote devices via the remote access signals passed across the γ-interface from the PMA (see 61.3.1). The operation of the PME_Aggregate_register for CPE-subtype devices is defined as follows:

a) If the remote_discovery_register is clear then the PME_Aggregate_register shall be cleared.
b) If write_remote_Aggregation_reg is asserted, the contents of remote_write_data bit zero is written to PME_Aggregate_register in the bit location corresponding to the PMA/PMD from which the request was received. Acknowledge_read_write is asserted for one octet clock cycle.
c) If read_remote_Aggregation_reg is asserted, the contents of PME_Aggregate_register are placed onto remote_read_data_bus, bits 31 through 0. Unsupported bits are written as zero if the full width of PME_Aggregate_register is not supported. Acknowledge_read_write is asserted for one octet clock cycle.

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61.2.2.8.4 PME aggregation discovery register functions

The remote_discovery_register shall be implemented for CPE-subtype devices. The remote_discovery_register shall support atomic write operations and reads from remote devices via the remote access signals passed across the γ-interface from the PMA (see 61.3.1). The operation of the remote_discovery_register for CPE-subtype devices is defined as follows:

a) If read_remote_discovery_reg is asserted, which corresponds to a "Get" command as described in 61.4.7.1, the contents of remote_discovery_register are placed onto remote_read_data_bus. Acknowledge_read_write is asserted for one octet clock cycle[117].
b) If write_remote_discovery_reg is asserted, which corresponds to a "Set if Clear" command as described in 61.4.7.1, the action depends on the contents of remote_discovery_register. If the remote_discovery_register is currently clear (no bits asserted), the contents of the remote_write_data bus are placed into the remote_discovery_register. The new contents of remote_discovery_register are placed on the remote_read_data_bus. Acknowledge_read_write is asserted for one octet clock cycle. Else if the remote_discovery_register is not currently clear (any bit asserted), no data is written. The old contents of remote_discovery_register are placed on the remote_read_data_bus. NAcknowledge_read_write is asserted for one octet clock cycle. If multiple write_remote_discovery_reg signals are asserted (from multiple γ-interfaces) they shall be acted upon serially.
c) If clear_remote_discovery_reg is asserted, which corresponds to a "Clear if Same" command as described in 61.4.7.1, the action depends on the contents of remote_discovery_register. If the contents of the remote_write_data bus match that of the remote_discovery_register, the remote_discovery_register is cleared, the PME_Aggregate_register is cleared, the new contents of remote_discovery_register are placed on the remote_read_data_bus, and Acknowledge_read_write is asserted for one octet clock cycle. If the contents of the remote_write_data bus do not match that of the remote_discovery_register, the remote_discovery_register is unchanged; its contents are placed on the remote_read_data_bus; and NAcknowledge_read_write is asserted for one octet clock cycle.
d) If the logical AND of the Aggregation_link_state_register and the PME_Aggregate_register is clear then a timeout counter shall be started. If this condition continues for 30 seconds (the timeout period) then the remote_discovery_register shall be cleared.

A single device may be implemented which has multiple MIIs and (therefore) multiple PCS instances. There shall be one remote_discovery_register per PCS instance. The PME_Available_register shall be set prior to the enabling of links so that each PMA/PMD is linked to only one PCS. Access to the remote_discovery_register (read or write) shall be restricted to PMA/PMD instances for which the corresponding PME_Available_register bit is asserted.

The Aggregation_link_state_register is a pseudo-register corresponding to the TC_link_state bits from each γ-interface in the appropriate bit positions according to the PMA/PMD from which the signal is received. Bits corresponding to unsupported aggregation connections are zero.

The remote access mechanisms for the PME aggregation registers are defined in 61.4.7.

61.2.3 PCS sublayer: Management entity signals

The management interface has pervasive connections to all functions. Operation of the management control lines MDC and MDIO is specified in Clause 22 and Clause 45, and requirements for managed objects inside the PCS and PMA are specified in Clause 30.

The following MAC-PHY Rate Matching function signals are mapped to Clause 45 registers:

[117]If the CPE device fails to respond, NAcknowledge_read_write is asserted with remote_read_data_bus set to 000000000000_{16}.

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tx_rx_simultaneously
: this signal is asserted by the management entity to indicate that the MAC which is connected to the PHY is capable of receiving and transmitting simultaneously while in half-duplex mode. The corresponding register ("MII receive during transmit") is defined in 45.2.3.28.

crs_and_tx_en_infer_col
: this signal is asserted by the management entity to indicate that the MAC uses simultaneous detection of TX_EN and CRS to infer a collision. This signal is used in the rate matching state diagrams (Figure 61–7 and Figure 61–8). The corresponding register ("TX_EN and CRS infer a collision") is defined in 45.2.3.28.

The following PAF signals are mapped to Clause 45 registers or cause Clause 45 counters to increment:

PAF_available
: this signal indicates to the management whether the PAF function is available for use. The corresponding register is defined in 45.2.3.27.1.

PAF_enable
: this signal is asserted by the management entity to indicate that the PAF function is enabled. The corresponding register is defined in 45.2.3.28.3.

TC_PAF_RxErrorReceived
: (for each PMA, γ-interface) this signal is asserted to indicate that a fragment has been received across the γ-interface with Rx_Err asserted. The errored fragment has been discarded. The corresponding register is defined in 45.2.3.31.

TC_PAF_FragmentTooSmall
: (for each PMA, γ-interface) this signal is asserted to indicate that a fragment has been received across the γ-interface that was smaller than the minFragmentSize defined. The errored fragment has been discarded. The corresponding register is defined in 45.2.3.32.

TC_PAF_FragmentTooLarge
: (for each PMA, γ-interface) this signal is asserted to indicate that a fragment has been received across the γ-interface that was larger than the maxFragmentSize defined. The errored fragment has been discarded. The corresponding register is defined in 45.2.3.33.

TC_PAF_Overflow
: (for each PMA, γ-interface) this signal is asserted to indicate that a fragment has been received across the γ-interface that would have caused the receive buffer to overflow. The errored fragment has been discarded. The corresponding register is defined in 45.2.3.34.

PAF_BadFragmentReceived
: this signal is asserted to indicate that a fragment has been received that does not fit into the sequence expected by the frame assembly function. The errored fragment has been discarded and the frame buffer flushed to the next valid frame start. The corresponding register is defined in 45.2.3.35.

PAF_LostFragment
: this signal is asserted to indicate that a fragment (or fragments) expected according to sequence has not been received by the frame assembly function. The missing fragment (or fragments) has been skipped and the frame buffer flushed to the next valid frame start. The corresponding register is defined in 45.2.3.36.

PAF_LostStart
: this signal is asserted to indicate that the packet reassembly function did not receive a StartOf Packet indicator in the appropriate sequence. The corresponding register is defined in 45.2.3.37.

PAF_LostEnd
: this signal is asserted to indicate that the packet reassembly function did not receive an EndOfPacket indicator in the appropriate sequence. The corresponding register is defined in 45.2.3.38.

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PCS_link_state
: this signal is asserted to indicate that at least one TC_link_state in the assigned aggregation group is up.

Additionally, the following PAF register is mapped to a Clause 45 register:

remote_discovery_register
: this register is implemented in CPE-subtype devices. It is written or read by the PME via the γ-interface. The PME relays this information to and from the associated CO-subtype device via the handshake messages described in 61.4.7. The CO-subtype device interprets the contents of the remote_discovery_register to determine which remote PMEs connect to the same PCS and may be aggregated. The corresponding Clause 45 register is defined in 45.2.6.6.1.

61.3 TC sublayer functional specifications

The functional model of the TC sublayer is presented in Figure 61–12. The term "TPS-TC" (Transport Protocol Specific - Transmission Convergence) is used in ITU-T Recommendation G.993.1. In this context the term "TC" (Transmission Convergence) is sufficient as no other types of TC are defined in this subclause (e.g., PMS-TC).

Because the PAF function is optional, either entire data frames or data frame fragments may be passed across the γ-interface. In this section, the term "fragment" will be used to describe either fragments or data frames depending on the existence of the PAF.

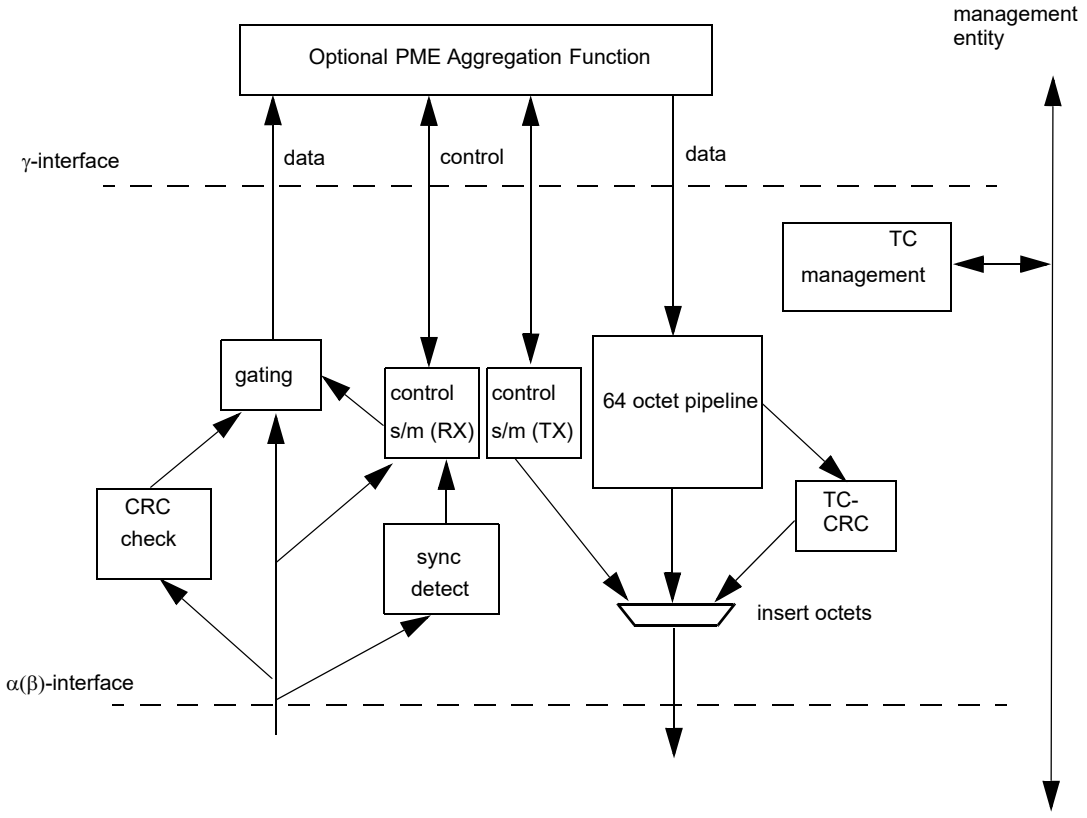

Figure 61–12—Functional diagram of TC sublayer

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61.3.1 The γ-interface

The γ-interface is specified by incorporating section H.3.1 and all subsections of ITU-T Recommendation G.993.1 (Annex H) by reference, with the following exceptions and additions:

The PCS shall assert Tx_Avbl when an entire data fragment is available for transmission, and de-assert Tx_Avbl when there are no data fragments to transmit. Tx_Avbl shall never be de-asserted during the transmission of a data fragment.

OAM Information flow across the γ-interface supports access to registers referenced in Clause 45. Refer to Clause 45 for a complete description of access to TC, PMA and PMD registers from the MDIO interface.

Additional signals, which would be represented in the referenced document section H.3.1.4, are described in Table 61–9. Some of these signals may be unused when Clause 45 is not implemented.

Table 61–9—Additional γ-interface signals for OAM[a]

Signal	Size	Description	Direction
TC_link_state	1 bit	Control signal asserted when link is active and framing has synchronized according to the definition in 61.3.3 (TC_synchronized = TRUE) and remote_TC_out_of_sync (see 61.3.3.7) is not asserted.	TC → PCS
write_remote_aggregation_reg[b]	1 bit	Control signal to write PME_Aggregate_register. Active (min) 1 octet clock cycle	to PCS
write_remote_discovery_reg[b]	1 bit	Control signal to write remote_discovery_register. Active (min) 1 octet clock cycle	to PCS
clear_remote_discovery_reg[b]	1 bit	Control signal to clear remote_discovery_register. Active (min) 1 octet clock cycle	to PCS
read_remote_aggregation_reg[b]	1 bit	Control signal to read PME_Aggregate_register. Active (min) 1 octet clock cycle	to PCS
read_remote_discovery_reg[b]	1 bit	Control signal to read remote_discovery_register. Active (min) 1 octet clock cycle	to PCS
remote_write_data_bus[b]	48 bit	Data bus for writing to PME aggregation registers. Valid during octet clock cycle when write control is asserted	to PCS
remote_read_data_bus[b]	48 bit	Data bus for the results of a read or atomic write function. Valid during octet clock cycle when Acknowledge_read_write or NAcknowledge read_write is asserted	from PCS
Acknowledge_read_write[b]	1 bit	Control signal responding (positively) to read or write. Active 1 octet clock cycle	from PCS
NAcknowledge read_write[b]	1 bit	Control signal responding (negatively) to read or write. Active 1 octet clock cycle	from PCS

[a]The term "OAM" as used here refers to the OAM facilities as defined in the referenced G.993.1 document.
[b]These signals are defined only if PAF is implemented, and then only in CPE subtypes. They are used only during G.994.1 handshake. For CO subtypes, pervasive access by management may be used to obtain the corresponding information. In case of read/write collision the PAF has to process the read/write-requests sequentially.

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61.3.2 The α(β)-interface

The α(β)-interface is specified by incorporating section 7.1 and all subsections of ITU-T Recommendation G.993.1 by reference.

NOTE—An identical α(β)-interface is defined in ITU-T G.991.2.

The α and β reference points define interfaces between the PCS and PMA in the 2BASE-TL-O/10PASS-TS-O and the 2BASE-TL-R/10PASS-TS-R, respectively. Both interfaces are functional, application independent and identical. Both interfaces are defined by the following signal flow:

a) Data flow
b) Synchronization flow
c) OAM flow[118]

61.3.2.1 α(β) data flow: reference G.993.1 section 7.1.1

Referenced as is, with the additions shown in Table 61–10.

Table 61–10— Additional α(β)-Interface signals

Signal(s)	Size	Description	Direction
PMA_receive_synchronized	1 bit	Receive PMA state diagram synchronized	PMA → TC
PMA_PMD_type	8 bit[a]	Signal indicating PMA/PMD mode of operation. Defined values: 00_{16} — 10PASS-TS CO subtype 01_{16} — 2BASE-TL CO subtype 02_{16}–$7B_{16}$ — reserved for allocation by IEEE 802.3 $7C_{16}$–$7F_{16}$ — assigned for allocation by ATIS T1E1.4 80_{16} – 10PASS-TS CPE subtype 81_{16} – 2BASE-TL CPE subtype 82_{16}–FB_{16} — reserved for allocation by IEEE 802.3 FC_{16}–FF_{16} — assigned for allocation by ATIS T1E1.4	PMA → TC

[a]NOTE—The MSB of this octet-wide signal is used to differentiate between CO-subtype and CPE-subtype.

61.3.2.2 α(β) synchronization flow

The synchronization flow comprises the following synchronization signals:

a) Transmission data flow octet synchronization (Osync_t)
b) Reception data flow octet synchronization (Osync_r)
c) Transmit and receive data flow bit-synchronization (Clk_t, Clk_r), optional
d) Transmit and receive data flow frame-synchronization (Fsync_t, Fsync_r), optional
e) Receive PMA state diagram synchronized (PMA_receive_synchronized)

The synchronization signals are asserted by the PMA and directed towards the PCS. The synchronization flow signals are described in Table 61–10.

[118]The term “OAM” as used here refers to the OAM facilities as defined in the referenced G.993.1 document.

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61.3.2.3 α(β) OAM flow[119]

The OAM Flow across the α(β)-interface exchanges OAM information between the PHY-OAM entity, the PMA and the PMD. The OAM flow is bi-directional and transports line related primitives, parameters, configuration setup and maintenance signals or commands.

Refer to Clause 62 and Clause 63 for definitions of the G.994.1 messaging, Operation Channel (OC) and Indicator Bits (IB) mechanisms for accessing remote parameters.

Refer to Annex 61A for an example of aggregation discovery.

61.3.3 TC functions

The TC shall provide full transparent transfer of data fragments between γ_O-interface and γ_R-interface (except non-correctable errors caused by the transmission medium). It shall also provide fragment integrity and fragment error monitoring capability.

In the transmit direction, the TC receives fragments from the PCS via the γ-interface. An additional 16- or 32-bit CRC is calculated on the data and appended. The TC then performs 64/65-octet encapsulation, and sends the resulting codewords to the PMA via the α(β)-interface. In the receive direction, the TC receives codewords from the PMA via α(β)-interface, recovers the transported TC fragment, checks the CRC, and submits the extracted fragment to the PCS via the γ-interface.

An implementation is shown in Figure 61–13 and some example timing diagrams are shown in Figure 61–14.

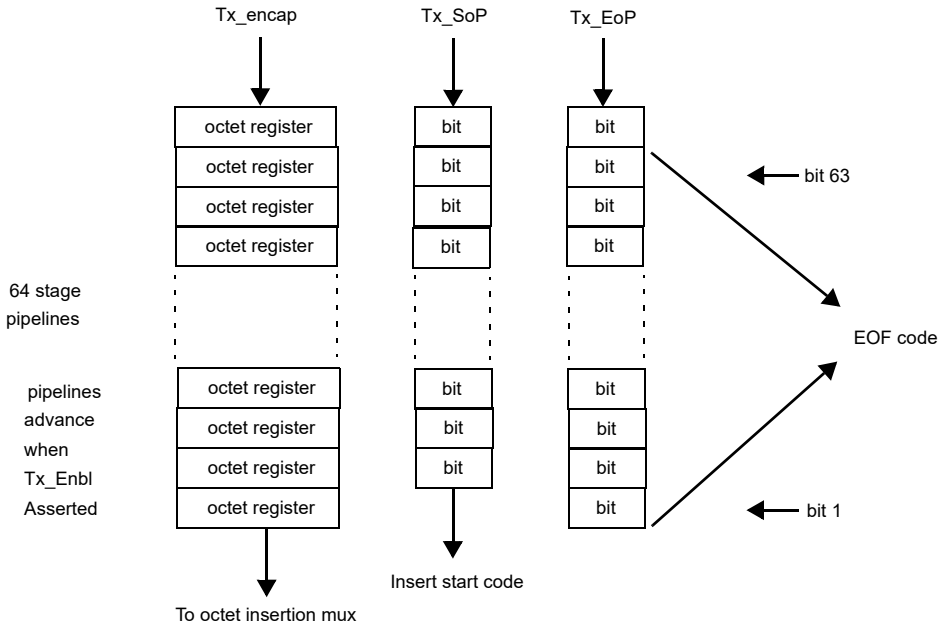

Figure 61–13—Example transmit pipeline

61.3.3.1 TC encapsulation and coding

A TC fragment consists of a fragment, followed by a 16- or 32-bit CRC (referred to as the TC-CRC) as defined in 61.3.3.3.

[119]The term "OAM" as used here refers to the OAM facilities as defined in the referenced G.993.1 document.

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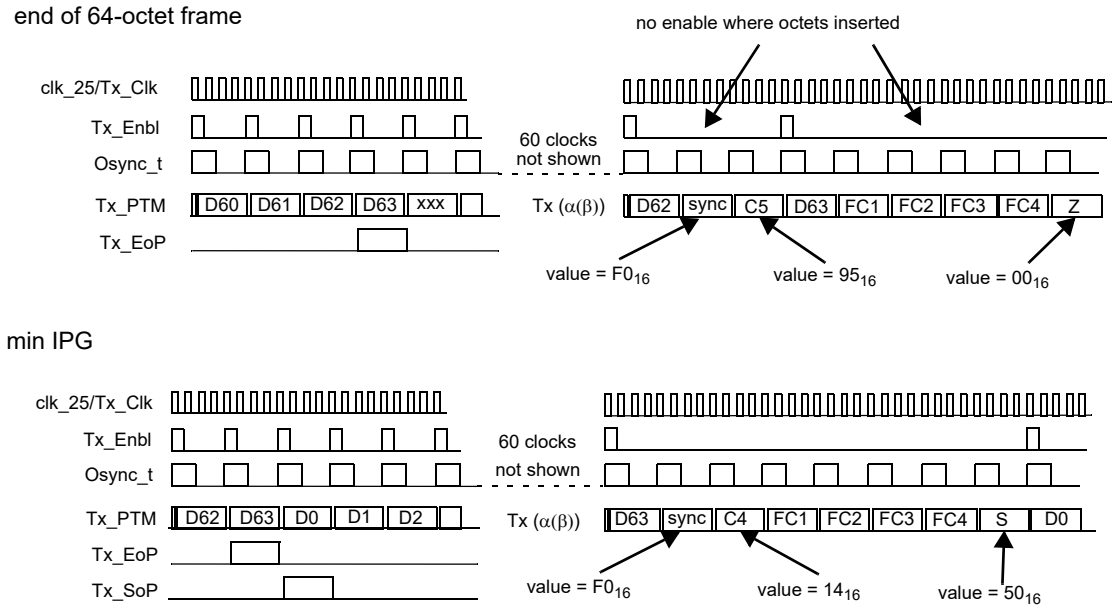

Figure 61–14—Example transmit timing

The TC coding function generates codewords with a fixed length of 65 octets (64/65-octet coding). A codeword consists of a Sync Octet and one of the following combinations:

a) all data: all of the octets in the codeword belong to the same TC fragment.
b) end of frame (go to idle): up to 63 octets in the codeword belong to the same TC fragment, the rest of the codeword consists of Idle octets.
c) end of frame (start new frame): up to 62 octets in the codeword belong to the same TC fragment, a number of Idle octets and a single Start of Frame octet precede the first data octets of the next TC fragment.
d) idle: all of the octets in the codeword are Idle octets.
e) idle (start new frame): a number of Idle octets and a single Start of Frame octet precede up to 63 data octets of the next TC fragment.
f) out-of-sync idle: all of the octets in the codeword are idle octets and the 64/65-octet receive state diagram is out-of-sync (TC_synchronized = FALSE).

Both transmit and receive data may be transferred across both the α(β) and the γ-interfaces at rates that are different from the rate across the MII; the frame buffering is managed in the sublayer above the γ-interface. The TC layer uses the γ-interface flow control signal, Tx_Enbl, to slow transmit data to the rate required for the encapsulated data across the α(β)-interface. The TC layer uses the γ-interface flow control signal, Rx_Enbl, to allow idle cycles in the flow of receive data across the γ-interface.

When a fragment arrives from the γ-interface while an End of Frame codeword is being transmitted, a Start of Frame octet shall be inserted prior to the transmission of data octets belonging to the next fragment. The Start of Frame octet *S* is distinct from the Idle octet *Z.* Valid locations for *S* are any valid location for *Z*, and the presence of an *S* rather than a *Z* octet indicates that what follows is the commencement of data for a new fragment.

No new fragment shall be transmitted when TC_link_state = FALSE (TC_link_state is defined in 61.3.3.7). If a fragment is being transmitted when TC_link_state becomes false, the End of Frame codeword completing the fragment shall not contain an *S* symbol after the end of the fragment. If an Idle codeword is being transmitted when TC_link_state becomes false, it shall be completed with *Z* symbols only. After the completed End of Frame or Idle codeword, only All Idle or All Idle Out-of-Sync codewords shall be

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transmitted until TC_link_state becomes TRUE again. After TC_link_state becomes true again, transmission of data can restart when a new fragment is available for transmission over the gamma-interface.

The data and sync format of the encapsulated data is shown in Table 61–11.

Table 61–11—Codeword formats

Type	Frame Data	Sync Octet	Octet fields 1–64									
all data	*DDDD—DDDD*	$0F_{16}$	D_0	D_1	D_2	D_3	D_4	D_5	...	D_{61}	D_{62}	D_{63}
end of frame	contains k *D*'s, where k = 0 to 63	$F0_{16}$	C_k	D_0	D_1	D_2	D_3	...	D_{k-1}	*Z*	...	*Z*
start of frame while transmitting	contains last k *D*'s of 1st frame, where k=0 to 62; & first j *D*'s of 2nd frame, where j=0 to 62-k	$F0_{16}$	C_k	D_0	...	D_{k-1}	*Z*	...	*S*	D_0	...	D_{j-1}
all idle	ZZZZ—ZZZZ	$F0_{16}$	*Z*	*Z*	*Z*	*Z*	*Z*	*Z*	...	*Z*	*Z*	*Z*
start of frame while idle	contains k *D*'s, where k=0 to 63, and contains j Z's, where j=63-k	$F0_{16}$	*Z*	*Z*	*S*	D_0	D_1	...	...	D_{k-3}	D_{k-2}	D_{k-1}
all idle out-of-sync	YZZZ—ZZZZ	$F0_{16}$	*Y*	*Z*	*Z*	*Z*	*Z*	*Z*	...	*Z*	*Z*	*Z*

The end of a TC fragment is always marked with an "end of frame" or "start of frame while transmitting" codeword; e.g., the received sequence [All Data codeword][All Idle codeword] is considered a sequencing error. When any of the following events occur, signal TC_coding_error shall be asserted:

a) An incorrect octet is received when a Sync Octet is expected.
b) Outside a fragment, the received octet following a valid $F0_{16}$ sync is not a *Z*, *Y*, *S*.
c) Inside a fragment, the received octet following a valid $F0_{16}$ sync is not a valid value of C_k.
d) *Z* or *S* is expected, and a value different from *Z* and *S* is received.

Signal remote_TC_out_of_sync shall be asserted when *Y* is received after an expected $F0_{16}$ sync symbol, and remain asserted until the beginning of a codeword other than All Idle Out-of-Sync is detected.

NOTE—When the local TC is not synchronized (TC_synchronized = FALSE), it may fail to detect incoming "All Idle Out-of-Sync" codewords. However, this does not affect the behavior of the local TC, which is sending "All Idle Out-of-Sync" codewords itself. Higher sublayers only use the combined signal TC_link_state, defined in 61.3.1.

Figure 61–15 illustrates two interesting examples. In the first example, the last 60 octets of a data frame, plus the 4 encapsulation CRC octets, are transmitted in an All Data codeword. In other words, the end of the (TC-CRC-augmented) frame coincides with the end of the codeword. In this case, the next codeword begins with Sync Octet equal to $F0_{16}$, C_k equal to C_0 (90_{16}). The second codeword indicates an End Of Frame, but with no additional data; in other words, the data in the previous codeword were the last of the frame. In the second example, the first octet of a frame is aligned with the first octet of an All Data codeword.

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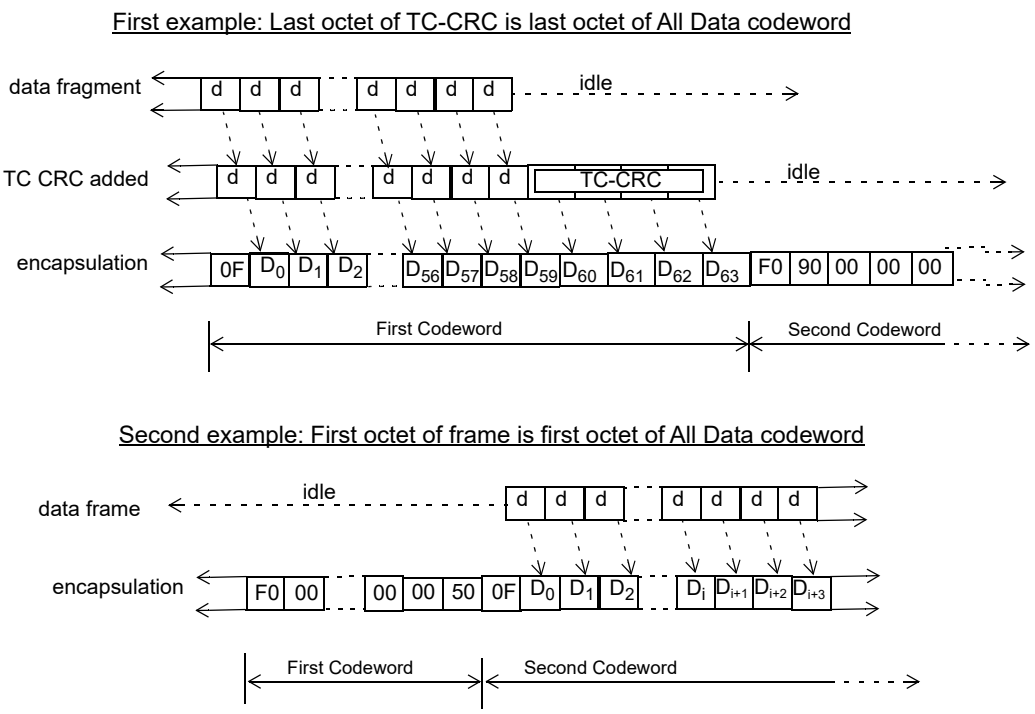

All octets other than D_x are written in hexadecimal notation.

Figure 61–15—TC Encapsulation examples

The values of the TC control characters are shown in Table 61–12.

Table 61–12—TC control character values

Character	Value
Z	00_{16}
C_k, k=0–63	$C_k = k+10_{16}$, with MSB set so that resulting value has even parity; $C_0=90_{16}$, $C_1=11_{16}$, $C_2=12_{16}$, $C_3=93_{16}$, ... $C_{62}=4E_{16}$, $C_{63}=CF_{16}$
Y	$D1_{16}$
S	50_{16}
R	All other values[a]

[a]See the state diagram for the 64/65-octet receive function (Figure 61–19) for required action when receiving reserved codewords.

61.3.3.2 Sync insertion and transmit control

The transmit data path needs a 64 stage pipeline in order to generate the appropriate sync octet along with an end-of-frame indicator when required. The flow control signal, Tx_Enbl, is used to slow the flow of data across the γ-interface to cater for the difference in clock speed between the α(β)-interface and the γ-interface and also to allow for the insertion of sync octets and CRC codes into the data stream.

A simple implementation may use a 64 bit pipeline for the Tx_EOP control signal. In that case, an end of frame sync code ($F0_{16}$, then C_k) would be inserted whenever a bit is set in stages 63 to 1 of the pipeline

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(stage 64 is the first stage). The value of C_k inserted would be such that k is equal to the stage number of the bit that is set.

Some implementations may optimize the insertions of idles between fragments. In particular an implementation may remove idle characters between fragments to increase the effective bandwidth of the channel.

If PMA/PMD link status is not Up (i.e. either Down or Initializing), the TC sublayer shall transmit only Out-of-Sync Idle codewords. The PMA/PMD link status is defined in 45.2.1.29.4.

61.3.3.3 TC-CRC functions

The TC-CRC is generated for the entire payload fragment including any attached header (from PAF), including the Ethernet CRC; i.e., the TC-CRC is computed over octets from the first octet of the PAF header (if present), or the first octet of the DestinationAddress (in the case where the PAF header not present), to the last octet of the Ethernet CRC (for a frame) or the last octet of the fragment (if PAF fragmentation is operating), inclusive. The TC-CRC is added to the data stream after the end of the fragment in the transmit direction. The TC-CRC is checked against the last 2 or 4 octets of the fragment in the receive direction. If the receive TC-CRC is incorrect then Rx_Err is asserted to signal that the fragment is errored.

The encoding for 2BASE-TL is defined by the following generating polynomial in Equation (61–1).

$$x^{32}+x^{28}+x^{27}+x^{26}+x^{25}+x^{23}+x^{22}+x^{20}+x^{19}+ \quad (61–1)$$
$$x^{18}+x^{14}+x^{13}+x^{11}+x^{10}+x^{9}+x^{8}+x^{6}+1 =$$
$$(x+1)(x^{31}+x^{30}+x^{29}+x^{28}+x^{26}+x^{24}+x^{23}+x^{21}+x^{20}+x^{18}+x^{13}+x^{10}+x^{8}+x^{5}+x^{4}+x^{3}+x^{2}+x+1)$$

The encoding for 10PASS-TS is defined by the following generating polynomial in Equation (61–2).[120]

$$x^{16}+x^{12}+x^{5}+1 \quad (61–2)$$

Mathematically, the TC-CRC value corresponding to a given payload fragment (including any attached header) is defined by the following procedure:

a) The first 32 bits (in the case of 2BASE-TL) or the first 16 bits (in the case of 10PASS-TS) of the payload are complemented.
b) The n bits of the payload are then considered to be the coefficients of a polynomial M(x) of degree n–1. (e.g., the first bit of the fragment corresponds to the x^{n-1} term and the last bit of the fragment corresponds to the x^0 term.)
c) $M(x)$ is multiplied by x^{32} (in the case of 2BASE-TL), or by x^{16} (in the case of 10PASS-TS), and divided by $G(x)$, the TC-CRC polynomial, producing a remainder $R(x)$ of degree 31 (in the case of 2BASE-TL), or degree 15 (in the case of 10PASS-TS).
d) The coefficients of $R(x)$ are considered to be a 32-bit sequence (in the case of 2BASE-TL), or a 16-bit sequence (in the case of 10PASS-TS).
e) The bit sequence is complemented and the result is the TC-CRC.

In the case of 2BASE-TL, the 32 bits of the TC-CRC value are placed so that the x^{31} term is the bit in position b_8 on the α(β)-interface (as shown in Figure 61–16) of the first octet, and the x^0 term is the bit in position b_1 on the α(β)-interface (as shown in Figure 61–16) of the last octet. (The bits of the CRC are thus transmitted in the order x^{31}, x^{30},.., x^1, x^0.) At the receiver, a payload received without error will result in the remainder $1C2D19ED_{16}$ when divided by $G(x)$.

[120]For 10PASS-TS, a 16-bit TC-CRC is sufficient for detecting payload errors, as the error-detecting capabilities of its Reed-Solomon decoder is also employed (see 62.2.2). In 2BASE-TL PHYs, a Reed-Solomon decoder is not present, hence a stronger TC-CRC is required.

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In the case of 10PASS-TS, the 16 bits of the TC-CRC value are placed so that the x^{15} term is the bit in position b_8 on the α(β)-interface (as shown in Figure 61–16) of the first octet, and the x^0 term is the bit in position b_1 on the α(β)-interface (as shown in Figure 61–16) of the last octet. (The bits of the CRC are thus transmitted in the order x^{15}, x^{14},.., x^1, x^0.) At the receiver, a payload received without error will result in the remainder $1D0F_{16}$ when divided by $G(x)$.

If, in the transmitter, the TX_Err signal is asserted during the transmission of the fragment across the γ-interface, the last octet of the TC-CRC shall be ones-complemented (i.e., intentionally corrupted by inverting all the bits of the last octet).

61.3.3.4 Bit ordering

In the transmitter, after encapsulation into 64/65-octet codewords, bits within each octet are labeled from b_1 to b_8, with the MSB labeled as b_1, the LSB labeled as b_8, and intervening bits labeled accordingly. In keeping with the labeling convention for the α(β)-interface in ITU-T Recommendations, bit b_8 is regarded as the MSB at the α(β)-interface, and is transmitted first if the α(β)-interface is serial by implementation.

Observe that the TC functionality defines a correspondence between the LSB at the γ-interface and b_8, between the next-order bit and b_7, etc., in order to conform to the Ethernet bit order convention of transmitting LSB first. See also H.4.1.1 in Annex H of ITU-T Recommendation G.993.1. In transmitting and calculating the TC-CRC, the octets at the γ-interface are processed LSB first.

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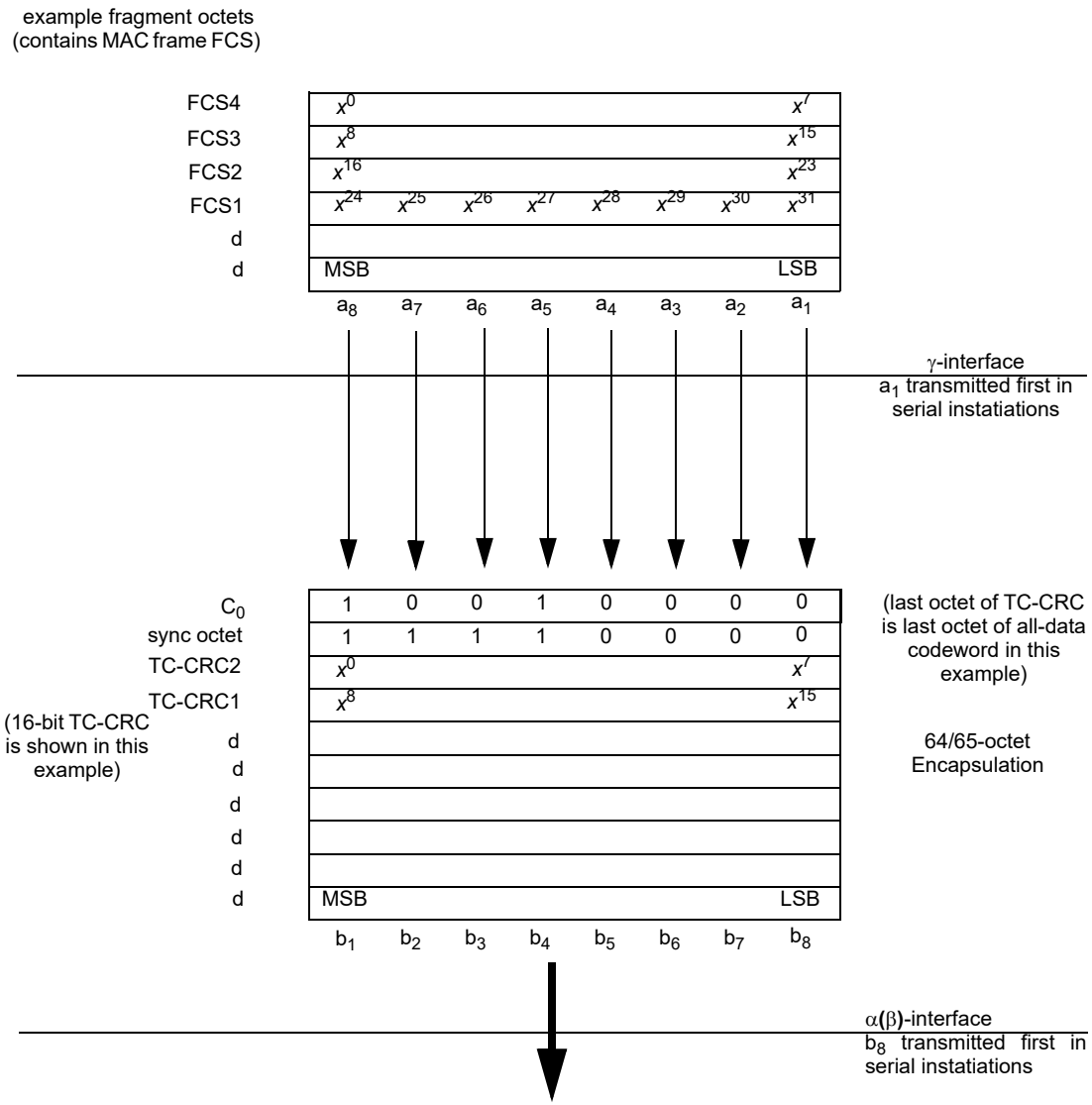

Figure 61–16—γ-interface to α(β)-interface bit ordering

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61.3.3.5 Sync detection

The sync detection function serves two purposes. Firstly, the synchronization is acquired from the incoming data stream, the sync detection function controls the initial acquisition and maintenance of the synchronization. Secondly, the sync detection is needed so that the receive control state diagram can extract framing information from the receive data stream and remove the sync characters and CRC codes. The sync detection state diagram is shown in Figure 61–17.

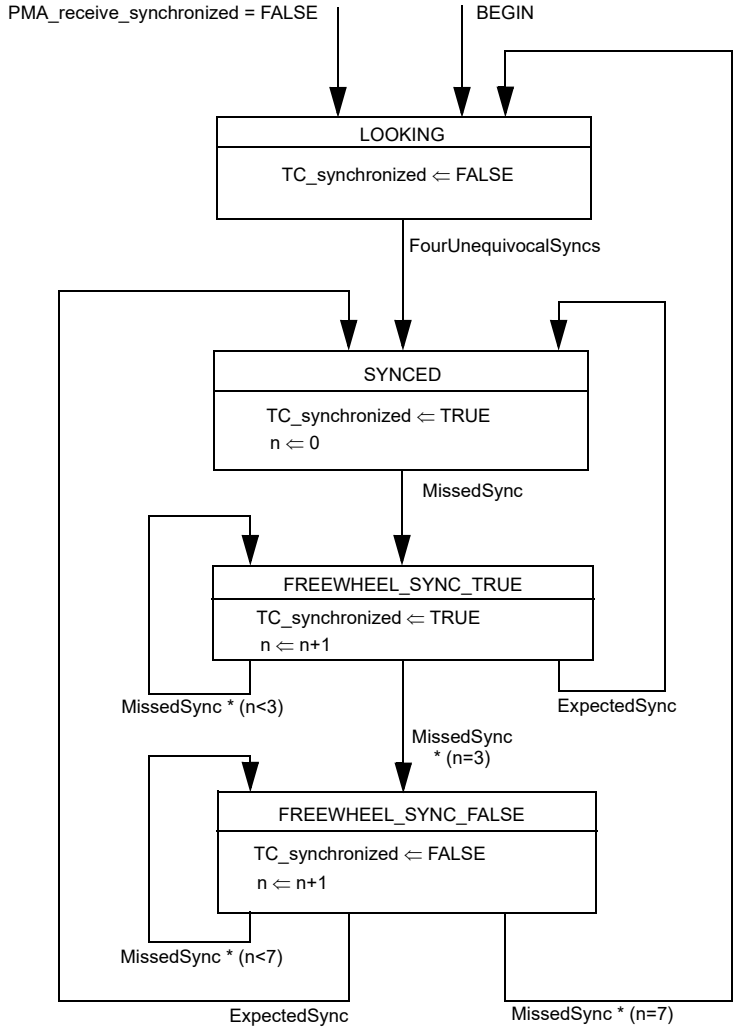

Figure 61–17—Sync detect state diagram

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61.3.3.5.1 State diagram variables

BEGIN

A variable that resets the functions within the sync detection function (see 45.2.1.1.1.)
TRUE when the TC sublayer is reset.
FALSE when (re-)initialization has completed.

ExpectedSync

variable of type Boolean, TRUE indicating the occurrence of a sync character in the correct position in the octet stream. The default value of this variable is FALSE; the value of the variable resets to FALSE on every state transition.

FourUnequivocalSyncs

variable of type Boolean, TRUE indicating the occurrence of a 196-octet sequence with the following two characteristics:

a)the sequence is of the form <sync><data><sync><data><sync><data><sync>, where each <sync> is $0F_{16}$ or $F0_{16}$ and each <data> is 64 octets of any value;
b)the pattern <sync><data><sync><data><sync> occurs nowhere in the sequence, where <sync> and <data> are as defined in (a, unless the <sync> values are coincident with those in (a;

The default value of this variable is FALSE; the value of the variable resets to FALSE on every state transition.

MissedSync

variable of type Boolean, TRUE indicating the occurrence of a non-sync character in the octet stream position where a sync character is expected. The default value of this variable is FALSE; the value of the variable resets to FALSE on every state transition.

n

variable of type integer, counting the occurrences of MissedSync = TRUE, used to determine when to leave state FREEWHEEL_SYNC_TRUE or FREEWHEEL_SYNC_FALSE.

PMA_receive_synchronized

signal of the α(β)-interface, see 61.3.2.

TC_synchronized

variable of type Boolean, TRUE indicating that the state diagram is in state SYNCED or FREEWHEEL_SYNC_TRUE. This variable is used to calculate the value of signal TC_link_state on the γ-interface (see 61.3.1), and to generate “All Idle Out Of Sync” codewords in the 64/65-octet transmit function (see Figure 61–18).

61.3.3.5.2 State diagram

The receiver shall implement the sync detect state diagram shown in Figure 61–17.

61.3.3.6 Receive control

The receive control function removes the sync characters and encapsulation CRC octets from the data stream and passes it upward across the γ-interface. If TC_synchronized = false then signal RX_Enbl shall be de-asserted. If a CRC error is detected the receive controller shall assert signal TC_CRC_error. The receive controller shall assert signal RX_Err at the γ-interface during at least one octet of a fragment as it is passed up across the γ-interface, if TC_CRC_error is asserted, or if the fragment contains data from a block of data in which the PMA detected errors, but did not correct them (the means by which the PHY passes this information from the PMA to the TC is unspecified).

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61.3.3.7 State diagrams for 64/65-octet encapsulation

This subclause contains the state diagrams for the 64/65-octet encapsulation function. Only the signals that affect the operation of the state diagrams are explicitly mentioned in the state diagrams. Other signals are to be set and read in accordance with the specifications of the γ-interface (see 61.3.1) and the α(β)-interface (see 61.3.2).

61.3.3.7.1 Transmit state diagram

The following variables are used in the state diagram.

BEGIN
: A variable that resets the functions within the sync detection function.
TRUE when the TC-sublayer is reset.
FALSE when (re-)initialization has completed.

k
: variable of type integer, used to keep track of the number of octets used in the current codeword, not including the sync symbols

loop
: variable of type Boolean, keeping track of the fact that an Out-of-Sync Idle codeword is being transmitted, thus preventing a Start-of-Frame to occur within this codeword (initial value is TRUE).

TC_link_state
: variable of type Boolean, indicating the current state of the TC_link_state signal on the γ-interface

TC_link_stateCHANGE
: This function monitors the TC_link_state variable for a state change. The function is set to TRUE on state change detection.
Values:
TRUE; A TC_link_state variable state change has been detected.
FALSE; A TC_link_state variable state change has not been detected (default).

NOTE—TC_link_stateCHANGE is set by this function definition; it is not set explicitly in the state diagrams. TC_link_stateCHANGE evaluates to its default value upon state entry.

TC_synchronized
: variable of type Boolean, indicating whether synchronization has been acquired (as used in Figure 61–17)

Tx_Avbl
: variable of type Boolean, indicating the current state of the Tx_Avbl (transmit data available) signal on γ-interface

Tx_EoP
: variable of type Boolean, indicating the current state of the Tx_EoP (end of packet) signal on γ-interface

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The following functions are used in the state diagram:

flushBuffer()
: function that removes any octets that have been pulled from the PCS by the function pullOctet() from the transmit fifo.

pullOctet()
: function that receives a single octet of data from the γ-interface. This function takes one cycle of the Tx_Enbl (transmit enable) signal (see 61.3.1) to complete. At the end of a fragment, this function returns the octets of the TC-CRC in the order specified in 61.3.3.3.

transmitAllDataSync()
: function that transmits the all-data sync symbol ($0F_{16}$) to the α(β)-interface. This function takes one cycle of the Osync_t signal (see 61.3.3.2) to complete.

transmitC(int k)
: function that transmits the C_k symbol as specified in Table 61–10 to the α(β)-interface. This function takes one cycle of the Osync_t signal (see 61.3.3.2) to complete.

transmitData()
: function that transmits all data currently in the transmit fifo to the α(β)-interface. This function takes one cycle of the Osync_t signal (see 61.3.3.2) per octet of data transmitted to complete.

transmitS()
: function that transmits the *S* symbol as specified in Table 61–12 to the α(β)-interface. This function takes one cycle of the Osync_t signal (see 61.3.3.2) to complete.

transmitSync()
: function that transmits the regular sync symbol ($F0_{16}$) to the α(β)-interface. This function takes one cycle of the Osync_t signal (see 61.3.3.2) to complete.

transmitZ(int k, Boolean loop)
: function that transmits the *Y* symbol ($D1_{16}$) to the α(β)-interface if (k=1) and (loop=TRUE), and transmits the *Z* symbol (00_{16}) to the α(β)-interface otherwise. This function takes one cycle of the Osync_t signal (see 61.3.3.2) to complete.

Figure 61–18 specifies the 64/65-octet encapsulation (transmit) function.

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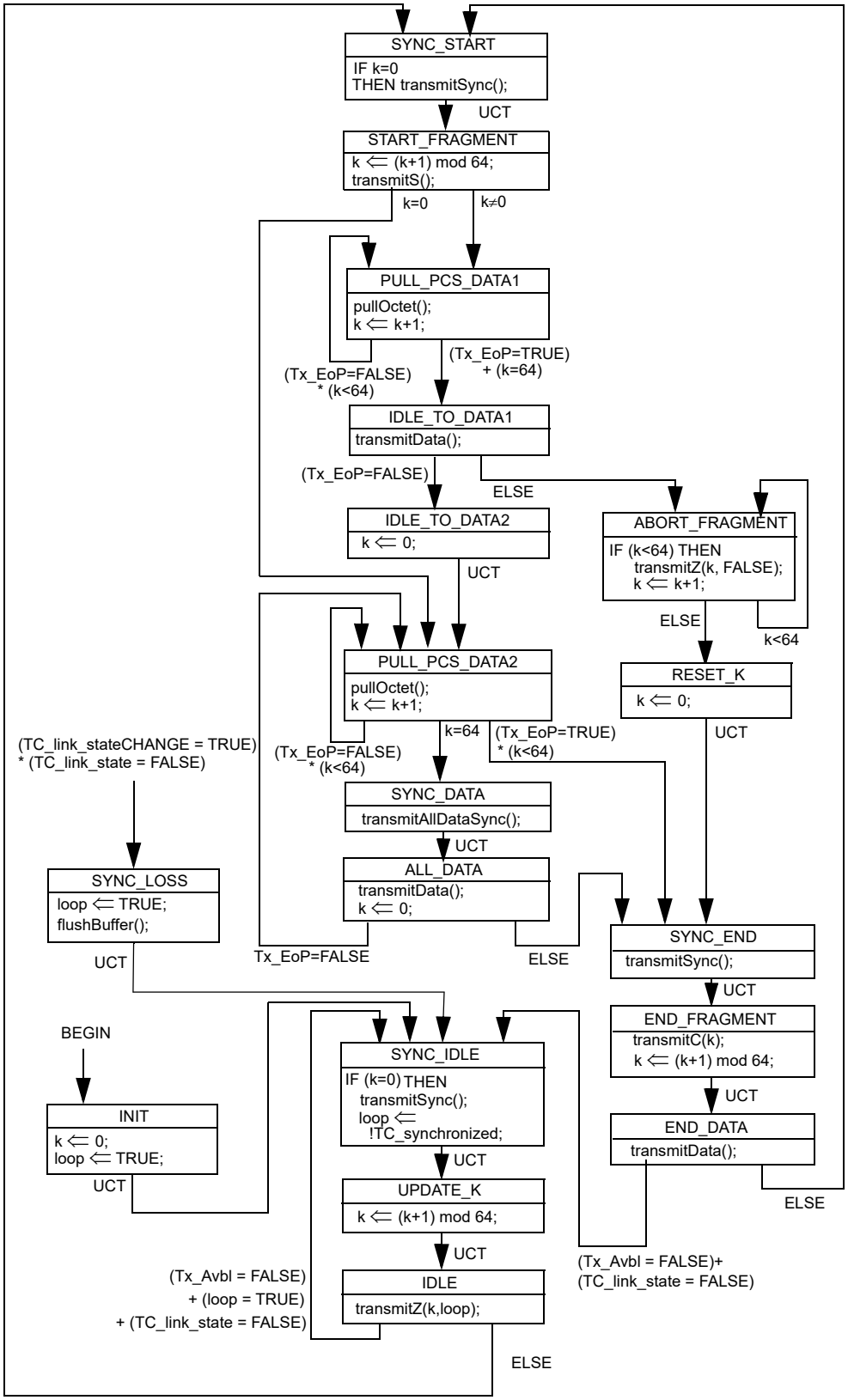

Figure 61–18—State diagram for 64/65-octet transmit function

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61.3.3.7.2 Receive state diagram

The following variables are used in the state diagram.

B
: variable of type octet, used to store a single received octet

C
: variable of type octet, used to store a received C_k symbol

codingViolation
: variable of type Boolean, used to mark detection of a coding violation when a sync octet was expected

expectedSync
: variable of type Boolean, used to mark successful sync octet detections, which are counted towards achieving synchronization as specified in Figure 61–17. The default value of this variable is FALSE; it returns to FALSE on every state transition.

k
: variable of type integer, used to keep track of the number of octets received in the current codeword, not including the sync symbols

kmax
: variable of type integer, used to store the decoded value of a C_k symbol

missedSync
: variable of type Boolean, used to mark unsuccessful sync octet detections, which are counted towards losing synchronization as specified in Figure 61–17. The default value of this variable is FALSE; it returns to FALSE on every state transition.

remote_TC_out_of_sync
: variable of type Boolean, representing the state of the remote TC synchronization state diagram (see 45.2.6.13).
TRUE if the remote TC has lost synchronization according to 61.3.3.5
FALSE if the remote TC has acquired synchronization according to 61.3.3.5

Rx_Err
: variable of type Boolean, representing the corresponding signal (receive error) on the γ-interface

TC_coding_error
: when this signal is asserted, the TPS-TC coding violations counter register is incremented (see 45.2.6.12). The default value of this variable is FALSE; it returns to FALSE on every state transition. If TC_coding_error becomes true during the reception of a fragment, Rx_Err is asserted on the γ-interface to signal this condition to the PCS, thus invalidating the entire fragment.

TC_synchronized
: variable of type Boolean, identical to the variable TC_synchronized defined in 61.3.3.7.1.

TC_synchronizedCHANGE
: This function monitors the TC_synchronized variable for a state change. The function is set to TRUE on state change detection.
Values:
TRUE; A TC_synchronized variable state change has been detected.
FALSE; A TC_synchronized variable state change has not been detected (default).

NOTE—TC_synchronizedCHANGE is set by this function definition; it is not set explicitly in the state diagrams. TC_synchronizedCHANGE evaluates to its default value upon state entry.

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The following functions are used in the state diagram.

decode(octet B)
: function that decodes the C_k symbol as specified in Table 61–12. A return value between 0 and 63 indicates a valid C_k symbol was read.

receiveOctet()
: function that receives a single octet of data over the α(β)-interface. This function takes one cycle of the Osync_r signal (see 61.3.2.2) to complete.

sendOctetToPCS()
: function that sends a single octet of data over an internal γ-interface to an intermediate fifo. The size of the intermediate fifo is more than 2 octets for 10PASS-TS and more than 4 octets for 2BASE-TL. Data is transmitted at the same rate from the intermediate fifo to the PCS (if present) over the γ-interface. This function takes one cycle of the Rx_clk (receive clock) signal (see 61.3.1) to complete. At the end of a fragment, the fifo contains the TC_CRC octets. The TC_CRC octets are never forwarded over the γ-interface. After verification of the TC_CRC octets, the result of the TC_CRC verification is signalled to the PCS (if present) over the γ-interface.

Figure 61–19 specifies the 64/65-octet decapsulation (receive) function.

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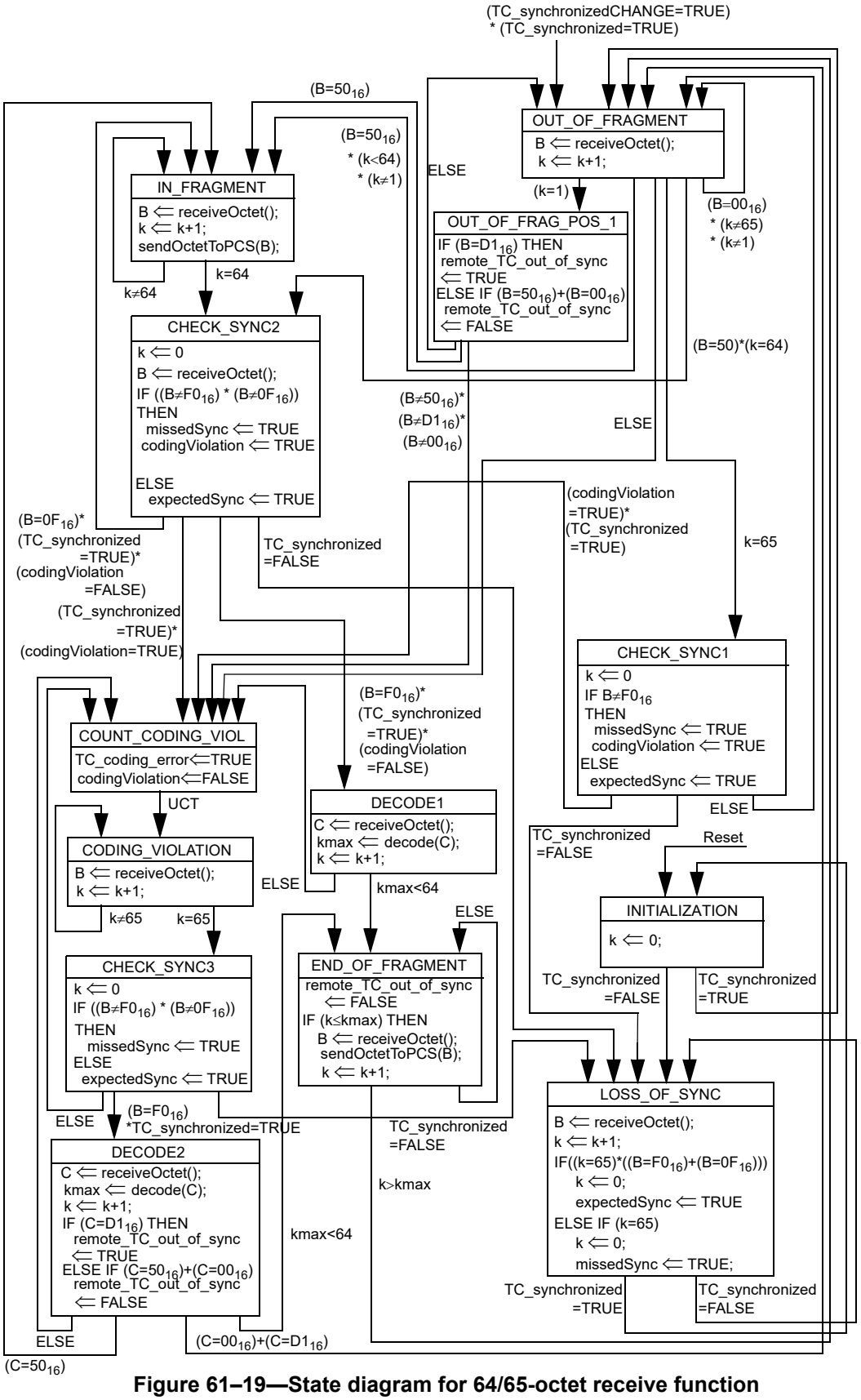

Figure 61–19—State diagram for 64/65-octet receive function

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61.3.3.8 TC sublayer management entity signals

The following TC sublayer signals are mapped to Clause 45 registers or cause Clause 45 counters to increment:

remote_TC_out_of_sync
: (for each PMA, γ-interface) this signal is asserted to indicate that the remote TC has signaled loss-of-sync. See Figure 61–19 and 45.2.6.13.

TC_synchronized
: (for each PMA, γ-interface) this signal is asserted to indicate that the state diagram has achieved codeword synchronization. See Figure 61–17 and 45.2.6.10.

TC_CRC_error
: (for each PMA, γ-interface) this signal is asserted to indicate that the synchronization state diagram has detected a false CRC code for a received frame (see 45.2.6.11).

TC_coding_error
: (for each PMA, γ-interface) this signal is asserted to indicate that a coding violation has been detected in the received octet stream (see 45.2.6.12).

61.4 Handshaking and PHY control specification for type 2BASE-TL and 10PASS-TS

61.4.1 Overview

This subclause defines the startup and handshaking procedures by incorporating ITU-T Recommendation G.994.1 by reference, with the exceptions listed below. Where there is conflict between specifications in G.994.1 and those in this standard, those of this standard will prevail. The G.994.1 parameter values and options to be used by 2BASE-TL and 10PASS-TS are specified here.

At the time of publication, G.994.1 Revision 3 (2004) is in force. Earlier Revisions of this Recommendation shall not be implemented in 2BASE-TL or 10PASS-TS.

61.4.2 Replacement of 1, “Scope”

61.4.2.1 Scope

This subclause defines signals, messages, and procedures for exchanging these between 2BASE-TL and 10PASS-TS port types, when the modes of operation of the equipment need to be automatically established and selected, but before signals are exchanged which are specific to a particular port type.

The startup procedures defined here are compatible with those used by other equipment on the public access network, such as DSL transceivers compliant with ITU-T Recommendations. For interrelationships of this subclause with ITU-T G.99x-series Recommendations, see ITU-T Series G Supplement 50 [B49].

The principal characteristics of this subclause are as follows:

a) Use over metallic local loops
b) Provisions to exchange capabilities information between DSL equipment and EFM PHYs to identify common modes of operation
c) Provisions for equipment at either end of the loop to select a common mode of operation or to request the other end to select the mode
d) Provisions for exchanging non-standard information between equipment
e) Provisions to exchange and request service and application related information
f) Support for both duplex and half-duplex transmission modes
g) Support for multi-pair operation
h) Provisions for equipment at the remote end of the loop (xTU-R) to propose a common mode of operation

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61.4.2.2 Purpose

It is the goal of the ITU-T that all specifications for digital transceivers for use on public telephone network copper subscriber lines use G.994.1 for startup. G.994.1 procedures allow for a common mechanism for identification of available features, exchange of capabilities and configuration information, and selection of operating mode. As the two loop endpoints are usually separated by a large distance (e.g., in separate buildings) and often owned and installed by different entities, G.994.1 also aids in diagnosing interoperability problems. G.994.1 codespaces have been assigned by ITU-T to ATIS, ETSI, and IEEE 802.3 in support of this goal.

In private networks, the management entity may additionally use G.994.1 tones or messages to autoconfigure the subtype (CO or CPE) in devices which implement both (see 61.1).

61.4.3 Changes to 6.1, “Description of signals”

NOTE 4 and NOTE 5 are not applicable.

Replace paragraph 3 of 6.1.1, “4.3125 kHz signaling family” with the following.

The carrier sets in this family are mandatory for the port types listed in Table 61–13. One or more carriers listed in Reference Table 1 or Reference Table 3 may be transmitted in addition to the mandatory carrier set listed in Table 61–13. Carriers not listed in Reference Table 1 or Reference Table 3 shall not be transmitted.

Table 61–13—Mandatory carrier sets

Port Types	Carrier set designation
10PASS-TS	V43

Replace paragraph 3 of section 6.1.2, “4 kHz signaling family” with the following.

The carrier sets in this family are mandatory for the port types listed in Table 61–14. One or more carriers listed in Reference Table 1 or Reference Table 3 may be transmitted in addition to the mandatory carrier set listed in Table 61–14. Carriers not listed in Reference Table 1 or Reference Table 3 shall not be transmitted.

Table 61–14—Mandatory carrier sets

Port Types	Carrier set designation
2BASE-TL	A4

61.4.4 Changes to 9.4, “Standard information field (S)”

Paragraphs 1–5: referenced as is.

Table 11.1 to Table 11.52 and Table 11.57 and beyond are not applicable.

The Standard information field (S) codepoints specified in Annex 61B shall be used in the transactions specified in this subclause.

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61.4.5 Changes to 9.5, “Non-standard information field (NS)”

Add this paragraph: The contents of the NS information field are outside the scope of this standard.

61.4.6 Applicability of Annex A–B and Appendix I–VI

Annex A / G.994.1—Support for legacy non-G.994.1 devices—Not applicable

Annex B / G.994.1—Operation over multiple wire pairs—Not applicable to the multipair operation for EFM

Appendix I / G.994.1—Not applicable

Appendix II / G.994.1—Provider Code contact Information —Referenced as is

Appendix III / G.994.1—Support for legacy DMT-based devices —Not applicable

Appendix IV / G.994.1—Procedure for the assignment of additional G.994.1 parameters—Not applicable

Appendix V / G.994.1—Rules for code point table numbering—Not applicable

Appendix VI / G.994.1—Bibliography

61.4.7 PME Aggregation – remote access of PME Aggregation registers

As the CO-subtype accesses PME Aggregation registers (i.e., remote_discovery_register and PME_Aggregate_register) in the CPE-subtype prior to training and establishment of the PMD-to-PMD link, it is performed using G.994.1 handshake messages.

The G.994.1 handshake messages described in this subclause shall assert the “Ethernet bonding” NPar(2) codepoint if and only if PAF_available is asserted. The “TDIM Bonding” NPar(2) bit shall be deasserted. In addition, the “Ethernet bonding” NPar(2) codepoint shall be asserted by the -O device in an MS message if and only if PAF_enable is asserted.

NOTE 1—A G.994.1 session including configuration of the PME Aggregation Function may violate the maximum activation time specified for SHDSL transceivers by ITU-T Recommendation G.991.2.

NOTE 2—In the transactions specified in this subclause, each CLR message may be preceded by MR/REQ-CLR messages. Each CL message is followed by an ACK(1). These messages are not shown in the diagrams.

61.4.7.1 Remote_discovery_register

2BASE-TL-R and 10PASS-TS-R PHYs shall assert the PME Aggregation Discovery SPar(2) bit in all G.994.1 CLR messages, if and only if its local PAF_available bit is set. CPE-subtypes shall place the contents of the remote_discovery_register in the corresponding NPar(3) bits in the outgoing CLR message, with the “Clear if Same” NPar(3) set to zero.

In response to a “Get” command, the CO-subtype shall perform a G.994.1 capabilities exchange with the CPE-subtype. The contents of the NPar(3) remote_discovery_register bits in the CLR message received from the CPE-subtype shall be reported as the result. The CL message sent by the CO-subtype in response to the CLR shall have the PME Aggregation Discovery SPar(2) bit set to zero.

In response to a “Set if Clear” command, the CO-subtype shall perform two back-to-back G.994.1 capabilities exchanges with the CPE-subtype. The contents of the NPar(3) remote_discovery_register bits in the first CLR message received from the CPE-subtype shall be ignored. The CL message sent by the CO-subtype in response to this first CLR shall have the PME Aggregation Discovery SPar(2) bit set to one, the Clear if Same NPar(3) bit set to zero, and the NPar(3) remote_discovery_register bits set to the CO-subtype

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PME Aggregation Discovery Code register. The CPE-subtype shall set the remote_discovery register to this value if it is currently clear. The contents of the NPar(3) remote_discovery_register bits in the CLR message received from the CPE-subtype during the second capabilities exchange shall be reported as the result. The CL message sent by the CO-subtype in response to this second CLR shall have the PME Aggregation Discovery SPar(2) bit set to zero.

In response to a “Clear if Same” command, the CO-subtype shall perform two back-to-back G.994.1 capabilities exchanges with the CPE-subtype. The contents of the NPar(3) remote_discovery_register bits in the first CLR message received from the CPE-subtype shall be ignored. The CL message sent by the CO-subtype in response to this first CLR shall have the PME Aggregation Discovery SPar(2) bit set to one, the Clear if Same NPar(3) bit set to one, and the NPar(3) remote_discovery_register bits set to the CO-subtype PME Aggregation Discovery Code register. The CPE-subtype shall clear the remote_discovery register if it is currently equal to this value. The contents of the NPar(3) remote_discovery_register bits in the CLR message received from the CPE-subtype during the second capabilities exchange shall be reported as the result. The CL message sent by the CO-subtype in response to this second CLR shall have the PME Aggregation Discovery SPar(2) bit set to zero.

Figure 61–20 illustrates the relevant sequences of G.994.1 transactions.

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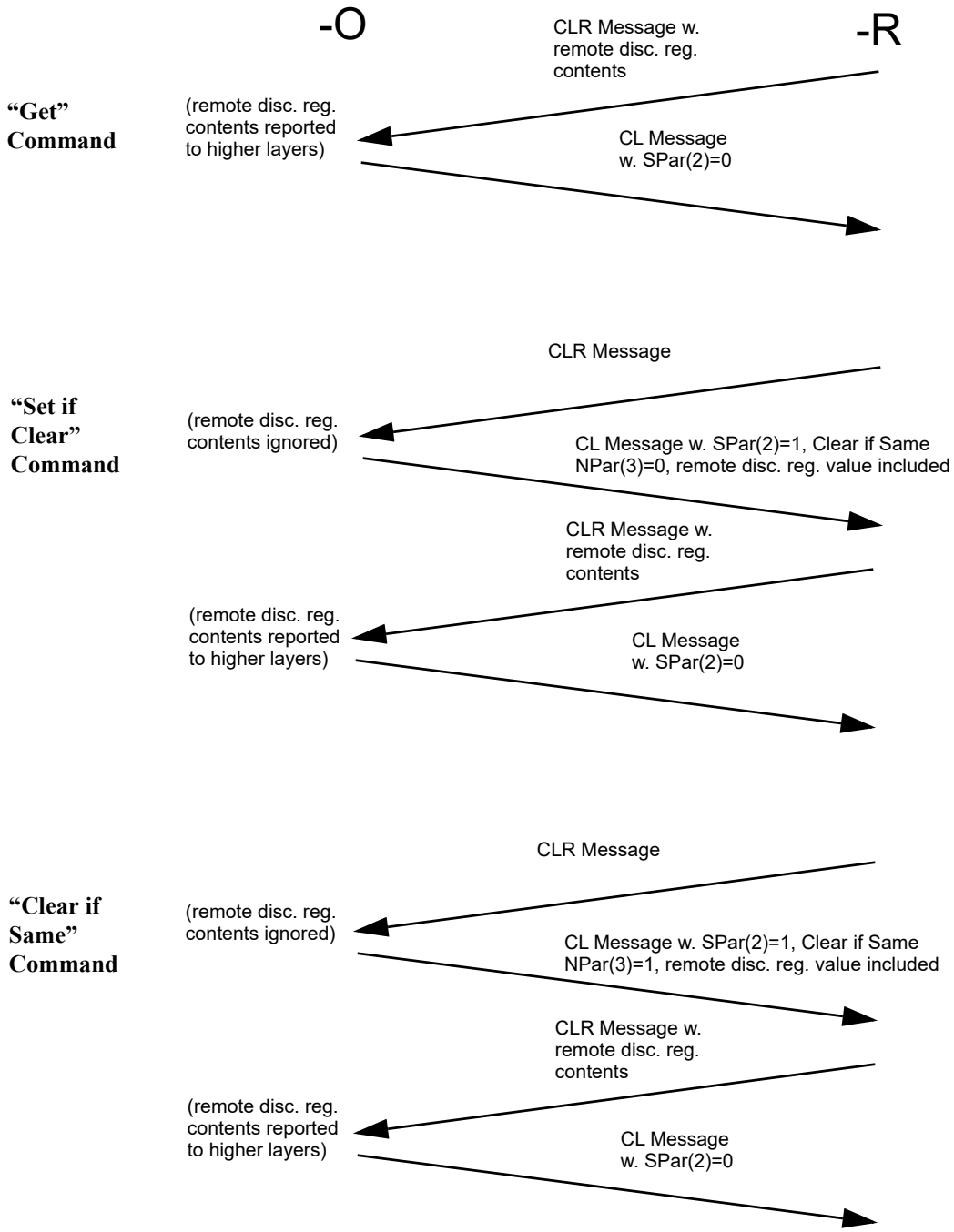

Figure 61–20—G.994.1 transactions for remote_discovery_register access

61.4.7.2 PME_Aggregate_register

2BASE-TL-R and 10PASS-TS-R PHYs shall assert the PME Aggregation SPar(2) bit in all G.994.1 CLR messages, if and only if its local PAF_available bit is set. CPE-subtypes shall place the contents of the PME_Aggregate_register in the corresponding NPar(3) bits in the outgoing CLR message.

In response to a "get" command, the CO-subtype shall perform a G.994.1 capabilities exchange with the CPE-subtype. The contents of the NPar(3) PME_Aggregate_register bits in the CLR message received from the CPE-subtype shall be reported as the result. The CL message sent by the CO-subtype in response to the CLR shall have the PME Aggregation SPar(2) bit set to zero.

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In response to a “set” command, the CO-subtype shall perform two back-to-back G.994.1 capabilities exchanges with the CPE-subtype. The contents of the NPar(3) PME_Aggregate_register bits in the first CLR message received from the CPE-subtype shall be ignored. The CL message sent by the CO-subtype in response to this first CLR shall have the PME Aggregation SPar(2) bit set to one and the NPar(3) PME_Aggregate_register bit zero. The -R device sets the bit position in the PME_Aggregate_register corresponding to the PME upon which the G.994.1 exchange takes place. The contents of the NPar(3) PME_Aggregate_register bits in the CLR message received from the CPE-subtype during the second capabilities exchange shall be reported as the result. The CL message sent by the CO-subtype in response to this second CLR shall have the PME Aggregation SPar(2) bit set to zero.

61.4.7.3 Timing and preferred transactions

This subclause is applicable to devices in which 10PASS-TS and/or 2BASE-TL are the only G.994.1-initiated PHYs implemented and enabled. Startup procedures for devices that include additional G.994.1-initiated modes of operation are outside the scope of this standard.

NOTE 1—Handshake operations specified in this subclause occur autonomously in the PHY, without intervention of the STA. They may however be triggered by an STA using the management interface.

If the PMA/PMD link control bit is set to 1 in the -O device (Table 45–31), or discovery register operations are initiated (Table 45–367), or link partner aggregation register operations are initiated (Table 45–370), the -O device initiates G.994.1 startup procedures by transmitting C-TONES.

If the PMA/PMD link control bit is set to 1 in the -R device (Table 45–31), the -R device initiates G.994.1 startup procedures by transmitting R-TONES-REQ.

At the conclusion of G.994.1 startup, the -R device shall begin G.994.1 transactions by transmitting an MR message. The -O device responds by sending C-TONES if the Ignore incoming handshake register bit (see 45.2.1.11) is set to 0_b.

If the G.994.1 session was initiated by the PMA/PMD link control bit (signifying that the link is to be brought up) in either the -O or -R device, then the -O device shall respond with an MS message specifying the configured mode of operation. However, if the PMA/PMD type selection bits in the -O device are set to the value 0011 or 0100, and a capabilities exchange has not previously taken place, the -O device shall instead respond with an REQ-CLR so that a capabilities exchange is performed. Following the final message of the capabilities exchange [i.e., an ACK(1)], the -R device once again sends an MR message. The -O device shall respond with an MS message specifying the configured mode of operation.

If the G.994.1 session was initiated in response to discovery register operations (Table 45–367), or link partner aggregation register operations (Table 45–370), then the -O device shall respond with an REQ-CLR message (MR received before) or with a CL message (CLR received before). This is then followed by one or two capability exchanges as described in the previous two subclauses. Following the final message of the final capabilities exchange [i.e., an ACK(1)], the CPE device once again sends an MR message. If neither the PMA/PMD control bit nor the discovery or link partner aggregation register operations are activated within the next 0.5 seconds, the -O shall transmit an MS message with the SPar(1) silent bit set.

NOTE 2—It is understood that the entire activation sequence consisting of PAF Discovery, PAF and line activation is time-consuming, therefore 2BASE-TL and 10PASS-TS devices are encouraged to exchange only relevant information in G.994.1 sessions during various stages of initialization.

61.5 Link segment characteristics

As stated in 61.1, the channel characteristics of voice grade copper are very diverse. Some typical channels are defined as part of the Performance Guidelines contained in Annex 62B (for 10PASS-TS) and Annex 63B (for 2BASE-TL). These annexes also define the reference performance levels for each PHY in these conditions. Behavior in other voicegrade installations may be interpolated or extrapolated from that set of references.

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61.6 MDI specification

The MDI interface for 10PASS-TS and the Service Splitter and Electrical Characteristics for 10PASS-TS are defined in 62.3.5.

The Electrical Characteristics of the MDI interface for 2BASE-TL are defined in 63.3.2.

The local regulations may dictate interface characteristics in addition to or in place of some or all of these requirements.

61.7 System considerations

Both EFM Copper port types are defined for full duplex operation only, although certain MACs may still require to be configured for half duplex operation in order to respond to the carrier Sense signal, as required by the specification of MAC-PHY Rate Matching. The requirements of 31B.1 restrict the transmission of PAUSE frames to DTEs configured to the full duplex mode of operation. If PAUSE frames are used on an EFM Copper link, consideration should be given to the link latency, and the fact that the MAC-PHY Rate Matching mechanism can interfere with the expected operation of the PAUSE frame mechanism.

NOTE—It is recognized that an EFM Copper system may have to comply with additional requirements and/or restrictions outside the scope of this standard (see 61.6 and 61.8 for examples) in order to be allowed to be connected to a public infrastructure in a certain geographic area or regulatory environment. These additional requirements and/or restrictions may prohibit operation under certain profiles, or degrade the performance of the system when working under certain profiles.This may limit the system's compliance with this standard, as compliant systems support all profiles (see Annex 62A for 10PASS-TS and Annex 63A for 2BASE-TL) and meet all performance guidelines (see Annex 62B for 10PASS-TS and Annex 63B for 2BASE-TL).

A compliant CPE-side system cannot distinguish a CO-side system designed to operate under a limited set of profiles from a fully compliant CO-side system, as the selection of profiles is under control of the CO-side. A CPE-side system designed to operate under a limited set of profiles cannot be guaranteed to correctly interoperate with compliant CO-side systems.

It is recommended that vendors of systems that support a limited set of profiles provide PICS forms to indicate which profiles are supported, in order to allow users to assess the impact on interoperability.

61.8 Environmental specifications

The requirements of 14.7 should be considered as baseline Environmental Specifications for types 10PASS-TS and type 2BASE-TL. Since equipment specified in this Clause will typically be deployed into public network environments, the specific requirements of the network operator or the local authority having jurisdiction shall prevail in all cases, and shall be considered in the development of such equipment. Such requirements may be statutory and may include product safety, electromagnetic compatibility and protection of the public network against harms from attached equipment.

61.9 PHY labeling

It is recommended that PHY equipment (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) PMA/PMD (sub-)type. A type (e.g., 10PASS-TS) can be specified if both -O and -R subtypes are supported. A subtype should be specified (e.g. 10PASS-TS-R) if only a single subtype is supported.
b) PAF capability if supported. The following information should be provided: number of MII/PCS ports provided; maximum number of PMEs per MII/PCS; total number of PMEs. For example:
    1) x8 or 1x8:8 for a single MII port with 8 PMEs
    2) 2x2:4 for a device with 2 MII ports and 4 PMEs, which can be aggregated up to 2 PMEs per port
    3) 4x4:4 for a device with 4 MII ports and 4 PMEs, which can be aggregated up to 4 PMEs per port
c) Homologation information
d) Applicable safety warnings

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61.10 Protocol implementation conformance statement (PICS) proforma for Clause 61, Physical Coding Sublayer (PCS), Transmission Convergence (TC) sublayer, and common specifications type 10PASS-TS, 2BASE-TL[121]

61.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 61, Physical Coding Sublayer (PCS), Transmission Convergence (TC) sublayer, and common specifications type 10PASS-TS, 2BASE-TL, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

61.10.2 Identification

61.10.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification--e.g., names and versions for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

61.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 61, Physical Coding Sublayer (PCS) and common specifications, type 10PASS-TS and 2BASE-TL.
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[121] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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61.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
RM	MAC-PHY Rate Matching	61.2.1	CRS deference mechanism supported.	M	Yes [ ]
TC	64/65-octet Encapsulation	61.3	The Ethernet-specific TPS-TC, between α(β)-interface and γ-interface is implemented.	M	Yes [ ]
*PAF	PME Aggregation	61.2.2	Up to 32 PMA/PMD instances can be aggregated into a single MAC.	O	Yes [ ] No [ ]
HS	Support for G.994.1 handshake	61.4	PHY uses G.994.1 handshake to identify remote transceiver and exchange capabilities.	M	Yes [ ]
*2BO	2BASE-TL-O subtype	61, 63	The 2BASE-TL CO subtype is implemented.	O.1	Yes [ ] No [ ]
*2BR	2BASE-TL-R subtype	61, 63	The 2BASE-TL CPE subtype is implemented.	O.1	Yes [ ] No [ ]
*10PO	10PASS-TS-O subtype	61, 62	The 10PASS-TS CO subtype is implemented.	O.1	Yes [ ] No [ ]
*10PR	10PASS-TS-R subtype	61, 62	The 10PASS-TS CPE subtype is implemented.	O.1	Yes [ ] No [ ]

61.10.4 PICS proforma tables for the Physical Coding Sublayer (PCS), Transmission Convergence (TC) sublayer, and common specifications type 10PASS-TS, 2BASE-TL

61.10.4.1 MAC-PHY Rate Matching

Item	Feature	Subclause	Value/Comment	Status	Support
RM-1	MAC-PHY Rate Matching functions	61.2.1.1	The PHY uses CRS to match the MAC's faster rate of data transmission to the PHY's slower rate.	M	Yes [ ]
RM-2	MAC-PHY Rate Matching functions	61.2.1.1	Upon receipt of a MAC frame from the MII, the PHY discards the Preamble and SFD fields, and transmits the resulting data frame across the physical link.	M	Yes [ ]
RM-3	MAC-PHY Rate Matching functions	61.2.1.1	The PHY prepends the Preamble and the SFD fields to a received frame before sending it to the MAC.	M	Yes [ ]
RM-4	MAC-PHY Rate Matching functions	61.2.1.1	The PHY supports a mode of operation where it does not send data to the MAC while the MAC is transmitting.	M	Yes [ ]

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61.10.4.2 64/65-octet Encapsulation

Item	Feature	Subclause	Value/Comment	Status	Support
TC-1	The γ-interface	61.3.1	The PAF asserts Tx_Avbl when it has a whole data fragment available for transmission, and de-assert Tx_Avbl when there are no data fragments to transmit.	M	Yes [ ]
TC-2	TC functions	61.3.3	The TC provides full transparent transfer of data frames between γ_O-interface and γ_R-interface.	M	Yes [ ]
TC-3	TC functions	61.3.3	The TC provides fragment integrity and fragment error monitoring capability.	M	Yes [ ]
TC-4	TC functions	61.3.3	The bit rate of data transport in the upstream and downstream directions are set independently of each other to any eligible value up to the maximum rate determined by the PMD.	M	Yes [ ]
TC-5	TC Encapsulation and Coding	61.3.3.1	When a frame arrives from the γ-interface while an End of Frame codeword is being transmitted, a Start of Frame octet is inserted prior to the transmission of data octets belonging to the next frame.	M	Yes [ ]
TC-6	Sync detection	61.3.3.5	The synchronization is acquired from the incoming data stream.	M	Yes [ ]
TC-7	Sync detection	61.3.3.5.2	The receiver implements the sync detect state diagram shown in Figure 61–17.	M	Yes [ ]
TC-8	Receive control	61.3.3.6	If TC_synchronized = false then signal RX_Enbl is de-asserted.	M	Yes [ ]
TC-9	Receive control	61.3.3.6	If a TC-CRC error is detected, the receive controller asserts signal RX_Err during at least one octet of the fragment as it is passed up across the γ-interface.	M	Yes [ ]
TC-10	Receive control	61.3.3.6	If the fragment contains data from a block in which the PMA detected errors but did not correct them, the receive controller asserts signal RX_Err during at least one octet of a fragment as it is passed up across the γ-interface.	M	Yes [ ]

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61.10.4.3 PME Aggregation[122]

Item	Feature	Subclause	Value/Comment	Status	Support
PAF-1	PME Aggregation Receive function	61.2.2.4	When the link state is changed to UP, the expected sequence number is unknown and no frame sequence errors are recorded.	*PAF:M	Yes [ ]
PAF-2	PME Aggregation Transmit Function Restrictions	61.2.2.6	The differential latency between any two PMEs in an aggregated group is no more than 15 000 bit times.	*PAF:M	Yes [ ]
PAF-3	PME Aggregation Transmit Function Restrictions	61.2.2.6	Fragments are not less than 64 octets.	*PAF:M	Yes [ ]
PAF-4	PME Aggregation Transmit Function Restrictions	61.2.2.6	Fragments are not more than 512 octets.	*PAF:M	Yes [ ]
PAF-5	PME Aggregation Transmit Function Restrictions	61.2.2.6	The highest ratio of speeds between any two aggregated links is 4.	*PAF:M	Yes [ ]
PAF-6	PME Aggregation Transmit Function Restrictions	61.2.2.6	The fragment size is a multiple of 4 octets except for the last fragment of a data frame.	*PAF:M	Yes [ ]
PAF-7	Error-detecting Rules	61.2.2.7	For each PMA, the per-PMA buffering mechanism discards the fragment if any of the listed conditions occur, and asserts the PAF error flags as appropriate. If the packet assembly function was mid-frame, the first part of the frame is transferred across the MII, then the RX_ER signal is asserted on the MII, the frame transfer is aborted and PMA buffers are flushed until the next Start of Packet is received.	*PAF:M	Yes [ ]
PAF-8	Error-detecting Rules	61.2.2.7	If a fragment is received with the StartOfPacket bit asserted while the packet assembly function was mid-frame, the first part of the frame is transferred across the MII, then the RX_ER signal is asserted on the MII, the frame transfer is aborted and PMA buffers are flushed until the next Start of Packet is received.	*PAF:M	Yes [ ]
PAF-9	PME aggregation register functions	61.2.2.8.3	The remote_discovery_register and Aggregation_link_state_register are implemented.	*PAF:M	Yes [ ]
PAF-10	PME aggregation register functions	61.2.2.8.3	The PME_Available_register is read-only.	*PAF: *2BO:M *10PO:M	Yes [ ]

[122]All items listed in this section are only applicable if the optional PME Aggregation Function is supported.

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PAF-11	PME aggregation register functions	61.2.2.8.3	The PME_Available_register is writeable.	*PAF: *2BR:O *10PR:O	Yes [ ] No [ ]
PAF-12	PME aggregation register functions	61.2.2.8.3	For a device that does not support aggregation of multiple PMEs, a single bit of the PME_Available_register is set and all other bits clear.	*PAF:M	Yes [ ]
PAF-13	PME aggregation register functions	61.2.2.8.3	The PME_Available_register is read-only.	*PAF: *2BO:M *10PO:M	Yes [ ]
PAF-14	PME aggregation register functions	61.2.2.8.3	The PME_Available_register is writeable.	*PAF: *2BR:O *10PR:O	Yes [ ] No [ ]
PAF-15	PME aggregation register functions	61.2.2.8.3	For CPE-subtype devices, PMD links are not enabled until the PME_Available_register has been set to limit the connectivity such that each PME maps to one, and only one MII.	*PAF:M	Yes [ ]
PAF-16	PME aggregation register functions	61.2.2.8.3	If the remote_discovery_register is clear then the PME_Aggregate_register is cleared.	*PAF:M	Yes [ ]
PAF-17	PME aggregation register functions	61.2.2.8.3	The remote_discovery_register is implemented for CPE-subtype devices.	*PAF: *2BR:M *10PR:M	Yes [ ]
PAF-18	PME aggregation register functions	61.2.2.8.3	The remote_discovery_register supports atomic write operations and reads from remote devices via the remote access signals passed across the γ-interface from the PMA.	*PAF:M	Yes [ ]
PAF-19	PME aggregation register functions	61.2.2.8.3	If multiple write_remote_discovery_reg signals are asserted they are acted upon serially.	*PAF:M	Yes [ ]
PAF-20	PME aggregation register functions	61.2.2.8.3	If the logical AND of the Aggregation_link_state_register and the PME_Aggregate_register is clear then a time-out counter is started. If this condition continues for 30 seconds then the remote_discovery_register is cleared.	*PAF:M	Yes [ ]
PAF-21	Remote access of PME Aggregation registers	61.4.7	The “TDIM Bonding” SPar(1) bit is deasserted.	*PAF:M	Yes [ ]
PAF-22	Remote_discovery_register	61.4.7.1	2BASE-TL-R and 10PASS-TS-R PHYs assert the PME Aggregation Discovery SPar bit in all G.994.1 CLR messages, if and only if its local PAF_available bit is set.	*PAF:M	Yes [ ]

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PAF-23	Remote_discovery_register	61.4.7.1	CPE-subtypes place the contents of the remote_discovery_register in the corresponding NPar bits in the outgoing CLR message, with the “Clear if Same” NPar set to zero.	*PAF:M	Yes [ ]
PAF-24	Remote_discovery_register	61.4.7.1	In response to a “Get” command, the CO-subtype performs a G.994.1 capabilities exchange with the CPE-subtype. The contents of the NPar remote_discovery_register bits in the CLR message received from the CPE-subtype are reported as the result.	*PAF:M	Yes [ ]
PAF-25	Remote_discovery_register	61.4.7.1	The CL message sent by the CO-subtype in response to the CLR has the PME Aggregation Discovery SPar bit set to zero.	*PAF:M	Yes [ ]
PAF-26	Remote_discovery_register	61.4.7.1	In response to a “Set if Clear” command, the CO-subtype performs two back-to-back G.994.1 capabilities exchanges with the CPE-subtype. The contents of the NPar remote_discovery_register bits in the first CLR message received from the CPE-subtype are ignored.	*PAF:M	Yes [ ]
PAF-27	Remote_discovery_register	61.4.7.1	The CL message sent by the CO-subtype in response to the first CLR has the PME Aggregation Discovery SPar bit set to one, the Clear if Same NPar bit set to zero, and the NPar remote_discovery_register bits set to the CO-subtype PME Aggregation Discovery Code register.	*PAF:M	Yes [ ]
PAF-28	Remote_discovery_register	61.4.7.1	In a set-if-clear exchange, the CPE-subtype sets the remote_discovery register to the value of the Remote Discovery register NPar(3) if it is currently clear.	*PAF:M	Yes [ ]
PAF-29	Remote_discovery_register	61.4.7.1	The contents of the NPar remote_discovery_register bits in the CLR message received from the CPE-subtype during the second capabilities exchange are reported as the result.	*PAF:M	Yes [ ]
PAF-30	Remote_discovery_register	61.4.7.1	The CL message sent by the CO-subtype in response to the second CLR has the PME Aggregation Discovery SPar bit set to zero.	*PAF:M	Yes [ ]

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PAF-31	Remote_discovery_register	61.4.7.1	In response to a “Clear if Same” command, the CO-subtype performs two back-to-back G.994.1 capabilities exchanges with the CPE-subtype. The contents of the NPar remote_discovery_register bits in the first CLR message received from the CPE-subtype are ignored.	*PAF:M	Yes [ ]
PAF-32	Remote_discovery_register	61.4.7.1	The CL message sent by the CO-subtype in response to the first CLR has the PME Aggregation Discovery SPar bit set to one, the Clear if Same NPar bit set to one, and the NPar remote_discovery_register bits set to the CO-subtype PME Aggregation Discovery Code register.	*PAF:M	Yes [ ]
PAF-33	Remote_discovery_register	61.4.7.1	In a clear-if-same exchange, the CPE-subtype clears the remote_discovery register if it is currently equal to the value of the Remote Discovery register NPar(3).	*PAF:M	Yes [ ]
PAF-34	Remote_discovery_register	61.4.7.1	The contents of the NPar remote_discovery_register bits in the CLR message received from the CPE-subtype during the second capabilities exchange are reported as the result.	*PAF:M	Yes [ ]
PAF-35	Remote_discovery_register	61.4.7.1	The CL message sent by the CO-subtype in response to the second CLR has the PME Aggregation Discovery SPar bit set to zero.	*PAF:M	Yes [ ]
PAF-36	PME_Aggregate_register	61.4.7.2	2BASE-TL-R and 10PASS-TS-R PHYs assert the PME Aggregation SPar bit in all G.994.1 CLR messages, if and only if their local PAF_available bit is set.	*PAF:M	Yes [ ]
PAF-37	PME_Aggregate_register	61.4.7.2	CPE-subtypes place the contents of the PME_Aggregate_register in the corresponding NPar bits in the outgoing CLR message.	*PAF:M	Yes [ ]
PAF-38	PME_Aggregate_register	61.4.7.2	In response to a “get” command, the CO-subtype performs a G.994.1 capabilities exchange with the CPE-subtype. The contents of the NPar PME_Aggregate_register bits in the CLR message received from the CPE-subtype are reported as the result.	*PAF:M	Yes [ ]

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PAF-39	PME_Aggregate_register	61.4.7.2	The CL message sent by the CO-subtype in response to the CLR has the PME Aggregation SPar bit set to zero.	*PAF:M	Yes [ ]
PAF-40	PME_Aggregate_register	61.4.7.2	In response to a “set” command, the CO-subtype performs two back-to-back G.994.1 capabilities exchanges with the CPE-subtype. The contents of the NPar PME_Aggregate_register bits in the first CLR message received from the CPE-subtype are ignored.	*PAF:M	Yes [ ]
PAF-41	PME_Aggregate_register	61.4.7.2	The CL message sent by the CO-subtype in response to the first CLR has the PME Aggregation SPar bit set to one and the NPar PME_Aggregate_register bit zero.	*PAF:M	Yes [ ]
PAF-42	PME_Aggregate_register	61.4.7.2	The contents of the NPar PME_Aggregate_register bits in the CLR message received from the CPE-subtype during the second capabilities exchange are reported as the result.	*PAF:M	Yes [ ]
PAF-43	PME_Aggregate_register	61.4.7.2	The CL message sent by the CO-subtype in response to the second CLR has the PME Aggregation SPar bit set to zero.	*PAF:M	Yes [ ]
PAF-44	Timing and preferred transactions	61.4.7.3	At the conclusion of G.994.1 startup, the -R device begins G.994.1 transactions by transmitting an MR message.	*PAF:M	Yes [ ]
PAF-45	Timing and preferred transactions	61.4.7.3	If the G.994.1 session was initiated by the PMA/PMD link control bit in either the -O or -R device, then the -O device responds with an MS message specifying the configured mode of operation.	*PAF:M	Yes [ ]
PAF-46	Timing and preferred transactions	61.4.7.3	If the PMA/PMD type selection bits in the -O device are set to the value 0011 or 0100, and a capabilities exchange has not previously taken place, the -O device instead responds with an REQ-CLR so that a capabilities is performed.	*PAF:M	Yes [ ]
PAF-47	Timing and preferred transactions	61.4.7.3	The -O device responds with an MS message specifying the configured mode of operation.	*PAF:M	Yes [ ]

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PAF-48	Timing and preferred transactions	61.4.7.3	If the G.994.1 session was initiated in response to discovery register operations, or link partner aggregation register operations, then the -O device responds with an REQ-CLR message or with a CL message.	*PAF:M	Yes [ ]
PAF-49	Timing and preferred transactions	61.4.7.3	If neither the PMA/PMD control bit nor the discovery or link partner aggregation register operations are activated within 0.5 seconds after an MR message, the -O transmits an MS message with the SPar silent bit set.	*PAF:M	Yes [ ]

61.10.4.4 Handshaking

Item	Feature	Subclause	Value/Comment	Status	Support
HS-1	Revision number: reference G.994.1 section 9.3.2	61.4.1	G.994.1 Revision Number 3 or higher is implemented.	M	Yes [ ]
HS-2	Summary of handshaking and PHY control specification	61.1.4.3	Devices implementing both 2BASE-TL and 10PASS-TS port types use G.994.1 to determine a common mode of operation.	O	Yes [ ] No [ ]
HS-3	4.3125 kHz signaling family: reference G.994.1 section 6.1.1	61.4.3	The mandatory carrier set listed in Table 61–13 is transmitted.	10PR:M 10PO:M	Yes [ ]
HS-4	4 kHz signaling family: reference G.994.1 section 6.1.2	61.4.3	The mandatory carrier set listed in Table 61–14 is transmitted.	2BR:M 2BO:M	Yes [ ]
HS-5	Prohibited carrier sets	61.4.3	Carriers not listed in Reference Table 1 or Reference Table 3 are not transmitted.	M	Yes [ ]
HS-6	Optional carrier sets	61.4.3	One or more carriers listed in Reference Table 1 or Reference Table 3 are transmitted in addition to a mandatory carrier set listed in Table 61–13 or Table 61–14.	O	Yes [ ] No [ ]
HS-7	Standard information field coding	61.4.4	The Standard information field (S) codepoints specified in Annex 61B are used in the transactions specified in 61.4.4.	M	Yes [ ]

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62. Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD), type 10PASS-TS

62.1 Overview

62.1.1 Scope

This clause specifies the 10PASS-TS Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD) for voice grade twisted-pair wiring. In order to form a complete 10PASS-TS PHY, the 10PASS-TS PMA and PMD are integrated with the TC and PCS of Clause 61. Parts of register 3.0, parts of register 3.4, and registers 3.60 through 3.73 specified in Clause 45 may be used to control the PCS of Clause 61. Parts of register 6.0 and registers 6.16 through 6.23 specified in Clause 45 may be used to control the TC sublayer of Clause 61. Registers 1.16 through 1.71 may be used to control the 10PASS-TS PMA and PMD.

62.1.2 Objectives

The following are the objectives for the 10PASS-TS PMA and PMD:

a) To provide 10Mb/s encapsulated packet data rate at the α(β)-interface.
b) To provide full duplex operation.
c) To provide for operating over non-loaded voice grade twisted pair cable at distances up to 750 m.
d) To provide a communication channel with a mean bit error ratio, at the α(β)-interface, of less than one part in 10^7 with 6 dB noise margin.

62.1.3 Relation of 10PASS-TS to other standards

The specifications of 10PASS-TS PMA and PMD are based on the VDSL transceiver specified in ATIS-0600424.

62.1.4 Summary of Physical Medium Attachment (PMA) specification

This layer is defined by the α(β)-interface and the I-interface.

62.1.4.1 α(β)-interface

A complete definition of the α(β)-interface is contained in 61.3.2.

62.1.4.2 I-interface

The I_O and I_R reference points define interfaces between the PMA and PMD in the 10PASS-TS-O and 10PASS-TS-R, respectively. Both interfaces are functional, application independent and identical. Both interfaces are defined by the following signal flows:

a) Data flow
b) Synchronization flow

62.1.4.2.1 I Data Flow

The data flow consists of the following two octet-oriented streams, both with the PMA frame format, with the bit rates defined by the PMD transmission profile:

a) Transmitted data (Tx)
b) Received data (Rx)

If data streams are implemented serially, the MSB of each octet is sent first.

Each stream bit rate value is set during PMD configuration.

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62.1.4.2.2 I Synchronization Flow

The synchronization flow consists of the transmitted and received octet synchronization signals (Clko_t, Clko_r). Optional transmit and receive bit-synchronization signals (Clkp_t, Clkp_r) are defined too.

Synchronization signals are asserted by the PMD and directed towards the PMA.

The synchronization flow signals are described in Table 62–1.

Table 62–1—I-interface signals

Signal(s)	Description	Direction	Notes
Data signals			
Tx	Transmitted data stream	PMA → PMD	Transmission frame format.
Rx	Received data stream	PMA ← PMD	
Synchronization signals			
Clko_t	Transmitted octet timing	PMA ← PMD	
Clko_r	Received octet timing	PMA ← PMD	
Clkp_t	Transmitted bit timing	PMA ← PMD	Optional
Clkp_r	Received bit timing	PMA ← PMD	Optional

62.2 PMA functional specifications

For the purpose of transmission over a serial implementation of the α(β)-interface or the I-interface, bit b_8 as defined in Figure 61–16 is considered MSB and shall therefore be transmitted first. However, for the purpose of all serial processing (e.g., scrambling, CRC calculation) bit b_8 is considered LSB and shall therefore be the first bit processed. Thus, the outside world MSB is considered as the 10PASS-TS LSB.

62.2.1 PMA functional diagram

Figure 62–1 shows a diagram of the PMA sublayer.

62.2.2 PMA functional specifications

The 10PASS-TS PMA is specified by incorporating the VDSL standard, ATIS-0600424, by reference, with the modifications noted below. This standard provides support for voice-grade twisted pair. For improved legibility in this clause, ATIS-0600424, will henceforth be referred to as MCM-VDSL.

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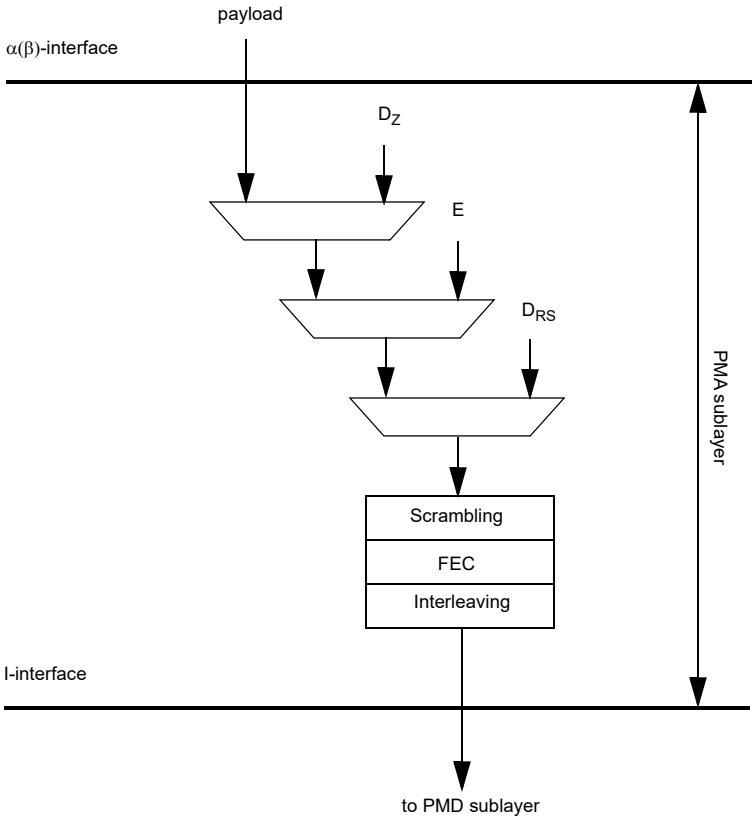

Figure 62–1—Diagram of PMA sublayer

62.2.3 General exceptions

The 10PASS-TS PMA is precisely the PMS-TC specified in MCM-VDSL, with the following general modifications:

a) There are minor terminology differences between this standard and MCM-VDSL that do not cause ambiguity. The terminology used in 10PASS-TS was chosen to be consistent with other IEEE 802 standards, rather than with MCM-VDSL. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 62–2.
b) The 10PASS-TS PMA does not support the “fast path”.

Table 62–2—Interpretation of general MCM-VDSL terms and concepts

MCM-VDSL term or concept	Interpretation for 10PASS-TS
PMS-TC	PMA
VTU-O, LT	10PASS-TS-O
VTU-R, NT	10PASS-TS-R
Transmission medium dependent interface	MDI
U1-interface (splitter present)	
U2-interface (splitter absent)	

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62.2.4 Specific requirements and exceptions

The 10PASS-TS PMA shall comply to the requirements of MCM-VDSL Section 9.3 with the exceptions listed below. Where there is conflict between specifications in MCM-VDSL and those in this standard, those of this standard shall prevail.

62.2.4.1 Replacement of 9.3.1, “PMS-TC functional diagram”

Replace 9.3.1 of MCM-VDSL by the PMA functional diagram in 62.2.1.

62.2.4.2 Changes to 9.3.3, “Forward error correction”

Referenced as is, with the exception of required Reed-Solomon encoder and interleaver settings.

The mandatory settings in MCM-VDSL (144,128) and (240,224) shall be supported. Other values are out of scope.

The following interleaver parameters shall be supported:

a) For (*N*,*K*)=(144,128) the following values for *M* and *I* shall be supported: *I*=36 and *M* between 2 and 52
b) For (*N*,*K*)=(240,224) the following values for *M* and *I* shall be supported: *I*=30 and *M* between 2 and 62

Other settings for *M* and *I* are out of scope.

62.2.4.3 Changes to 9.3.5, “Framing”

Referenced as is, with following exceptions:

a) The “fast” buffer is not supported
b) There shall be 1 VOC byte per packet; other values of V as defined in 9.3.5.5 are outside the scope of this standard
c) 9.3.5.5.4 (NTR) is not applicable
d) In Table 9-4 (9.3.5.5.3), following changes apply
    1) bits B2, B3 of Byte #2 are reserved
    2) bits B1, B2, B3, B4 of Byte #3 shall be set to 0

Additional text: the signal PMA_receive_synchronized, defined in 61.3.2.2, shall be asserted when 10PASS-TS is in the state “STEADY_STATE_TRANSMISSION” (see Figure 62–4), and deasserted when 10PASS-TS is in any other state.

62.3 PMD functional specifications

62.3.1 PMD Overview

The 10PASS-TS PMD functional model is presented in Figure 62–2. In the transmit direction, the PMD layer receives frames from the PMA layer. It sends a DMT modulated signal towards the physical medium over the MDI.

The bytes within the frame are encoded to a set of QAM constellation points that are used to modulate the carriers of the DMT symbol. The time-domain symbol is cyclically extended and then windowed to reduce sidelobe energy.

In the receive direction, a modulated signal is received from the transmission medium over the MDI. The PMD layer outputs a data frame to the PMA layer. The receiver is responsible for equalization and demodulation of the signal.

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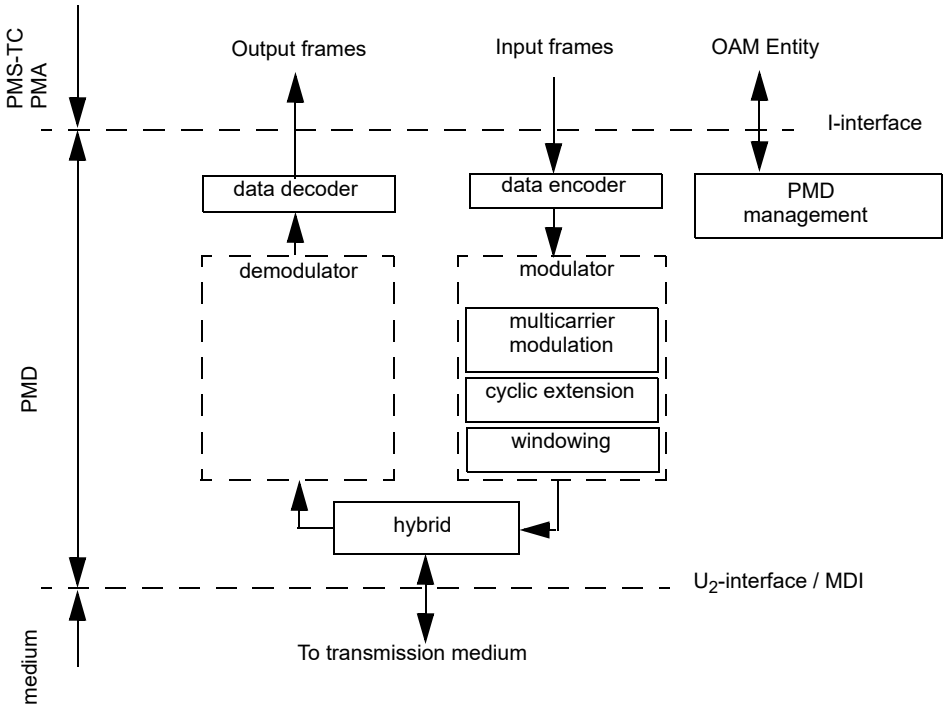

Figure 62–2—Functional diagram of PMD sublayer

62.3.2 PMD functional specifications

The 10PASS-TS PMD (and MDI) is specified by incorporating the MCM-VDSL standard, ATIS-0600424, by reference, with the modifications noted below. This standard provides support for voice-grade twisted pair.

62.3.3 General exceptions

The 10PASS-TS PMD is precisely the PMD specified as MCM-VDSL, with the following general modifications:

There are minor terminology differences between this standard and MCM-VDSL that do not cause ambiguity. The terminology used in 10PASS-TS was chosen to be consistent with other IEEE 802 standards, rather than with MCM-VDSL. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 62–3.

62.3.4 Specific requirements and exceptions

The 10PASS-TS PMD (including MDI) shall comply to the requirements of MCM-VDSL Section 8 [Physical medium dependent (PMD) sublayer], Section 10 (Operations and maintenance), Section 11 (Link activation and deactivation) and Section 18 (Normative Annex 4—Handshake procedure for VDSL) with the exceptions listed below. Section 12 (Test procedures and requirements), Section 13 (Physical conditions), Section 14 (Environmental conditions), Section 15 (Normative Annex 1: International amateur bands), Section 16 (Informative Annex 2: VDSL PSD templates figures), Section 17 (Informative Annex 3: Utopia implementation of the ATM-TC interface), Section 19 (Informative Annex 5: FMT implementation), Section 20 (Informative Annex 6: 8.625 kHz tone spacing), Section 21 (Normative Annex 7: Electrical characteristics of service splitter at remote subscriber end), Section 22 (Informative Annex 8: Electrical characteristics of service splitter at network end), and Section 23 (Informative Annex 9: Alien crosstalk descriptions), are outside the scope of this standard. Where there is conflict between specifications

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Table 62–3—Interpretation of general MCM-VDSL terms and concepts

MCM-VDSL term or concept	Interpretation for 10PASS-TS
PMS-TC	PMA
VTU-O, LT	10PASS-TS-O
VTU-R, NT	10PASS-TS-R
Transmission medium dependent interface	MDI
U1-interface (splitter present)	
U2-interface (splitter absent)	

in MCM-VDSL and those in this standard, those of this standard shall prevail. Optional specifications in MCM-VDSL are out of scope unless explicitly referenced in this document as mandatory. If out-of-scope optional features are implemented, the mode of operation of the PHY cannot be labeled "10PASS-TS" when these features are activated.

NOTE—If optional features are implemented, their use is negotiated during initialization.

62.3.4.1 Replacement of 8.2.1, "Multi-carrier Modulation"

10PASS-TS transceivers shall use Frequency Division Duplexing (FDD) to separate upstream and downstream transmission. 10PASS-TS transceivers shall support modulation of N_{SC} = 4096 subcarriers (n = 4). Disjoint subsets of the N_{SC} subcarriers shall be defined for use in the downstream and upstream directions. These subsets are determined by the choice of frequency plan. The exact subsets of subcarriers used to modulate data in each direction shall be determined during initialization and shall be based on management system settings and the signal-to-noise ratios (SNRs) of the subchannels. In many cases the number of subcarriers used in a direction will be less than the maximum number allowed by the partitioning.

Frequency plans are defined in Annex 62A. In standard frequency plans, frequency bands are allocated as shown in Figure 62–3. The values of the splitting frequencies are given in Annex 62A. Adherence to a particular frequency plan may be mandatory under local regulations when 10PASS-TS is deployed in public networks. Other frequency plans, for use in private networks, can be supported by means of Clause 45 register settings (see Annex 62C for examples).

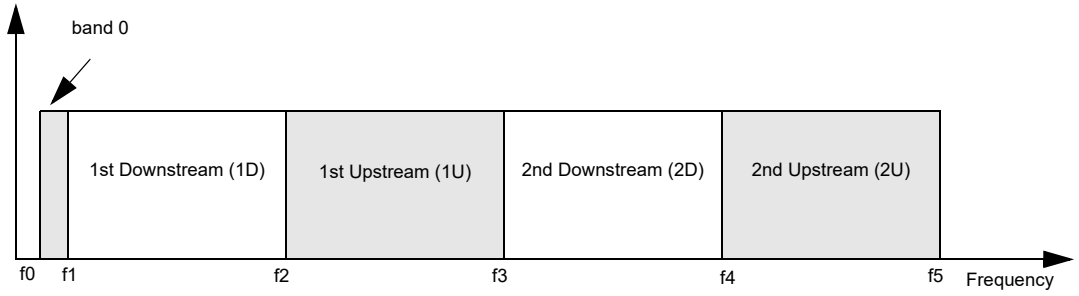

Figure 62–3—10PASS-TS band allocation

8.2.1.1 (Tone Spacing) is referenced as is.

8.2.1.2 (Data Sub Carriers) is referenced as is.

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8.2.1.3 (IDFT modulation) is referenced as is.

62.3.4.2 Changes to 8.2.2, “Cyclic extension”

8.2.2 of MCM-VDSL is further restricted by the following normative text:

The cyclic extension length is specified by the value of parameter *m*. In 10PASS-TS, support for the values $m = 10$, $m = 20$, and $m = 40$ is mandatory. The value $m=20$ is the default setting. Support for other values is out of scope.

62.3.4.3 Changes to 8.2.3, “Synchronization”

8.2.3.1 of MCM-VDSL is further clarified by the following text:

Support for pilot tones is mandatory. 10PASS-TS-O PHYs shall support the transmission of a pilot tone on any downstream tone.

8.2.3.2 (Loop Timing) is referenced as is.

8.2.3.3 (Timing Advance) is referenced as is.

8.2.3.4 of MCM-VDSL is replaced with the following:

The use of synchronous mode as defined in MCM-VDSL 8.2.3.4 may improve operation in certain binder environments and is a system implementation item that is outside the scope of this standard.

62.3.4.4 Replacement of 8.2.4, “Power back-off in the upstream direction”

To mitigate the effects of FEXT from short lines into long lines in distributed cable topologies, upstream power back-off shall be applied. Transceivers shall be capable of performing frequency-dependent power back-off.

It shall be possible to temporarily disable UPBO for performance testing purposes (as required by Annex 62B). In normal operation, only one UPBO mode shall be supported as described below:

a) It shall be possible for the network management system to set the limiting transmit PSD template PSD_0 for the 10PASS-TS-R to one of the standard transmit PSD templates as defined in the applicable section of 62A.3.3.
b) The 10PASS-TS-R shall perform UPBO autonomously, i.e., without sending any significant information to the 10PASS-TS-O until the UPBO is applied.
c) After UPBO has been applied as described in item b), the 10PASS-TS-O shall be capable of adjusting the transmit PSD selected by the 10PASS-TS-R; the adjusted transmit PSD shall be subject to the limitations given in the applicable section of 62A.3.3.

To enable the 10PASS-TS-R to initiate a connection with the 10PASS-TS-O, which will occur before UPBO has been applied, the 10PASS-TS-R shall be allowed to cause more degradation to other loops than expected when using the mode described below.

NOTE—Initiation refers to a request from the 10PASS-TS-R to start the initialization of the link. The particular method is in MCM-VDSL 11.2.

The 10PASS-TS-R shall explicitly estimate the electrical length of its line, kl_0, and use this value to calculate the transmit PSD template $TxPSD(kl_0,f)$. The 10PASS-TS-R shall then adapt its transmit signal PSD to conform to the template $TxPSD(kl_0,f)$ and the corresponding PSD mask, which is defined in the applicable section of 62A.3.3.

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The transmit PSD template shall be calculated as shown in Equation (62–1):

$$TxPSD(kl_0,f) = \min (PSD\_REF(f) + LOSS(kl_0,f), PSD_0), \text{ in dBm/Hz} \quad (62–1)$$

where PSD_0 as defined in item a) in the previous list, and:

$$LOSS = kl_0 \, \text{sqrt}(f), \text{ in dB} \quad (62–2)$$

where the *LOSS* function is an approximation of the loop attenuation (insertion loss).

NOTE—The estimation of the electrical length should be sufficiently accurate to avoid spectrum management problems and additional performance loss.

PSD_REF will depend on the limiting transmit PSD template PSD_0 and on the noise model that is relevant for a given deployment scenario. The values of *PSD_REF* depend on the selected UPBO Reference PSD profile, as shown in Table 62A-3. The same bandwidth as for all regular transmit PSD masks defined in the applicable section of 62A.3.3 shall be used to check the conformance of *TxPSD* with power back-off. The general methodology for testing PSD conformance is defined in 6.1 of ATIS-0600417.2003 (S2015). Conformance with the PSD template shall be verified using a 100 kHz sliding window in the in-band frequency range below 1 MHz and a 1 MHz sliding window in the in-band frequency range above 1 MHz.

PSD_REF shall be input via the management interface (by means of the UPBO Reference PSD field in the 10P tone control parameter register, see 45.2.1.54) and shall be transmitted from the 10PASS-TS-O to the 10PASS-TS-R.

The 10PASS-TS-R shall estimate the insertion losses of the upstream bands based on the received downstream signals. From this, the shape of the *LOSS* function (or, equivalently, the electrical length) as defined above shall be derived. The 10PASS-TS-R shall then compute the transmit PSD by dividing the reference PSD in the upstream bands by the estimated *LOSS* function. Next, the 10PASS-TS-R shall take a tone-by-tone minimum of this computed PSD and the maximum allowed transmit PSD in the upstream direction. The result shall be used as the initial upstream transmit PSD. The PSD received by the 10PASS-TS-O should approximate the reference PSD. Upon receiving signals from the 10PASS-TS-R, the 10PASS-TS-O shall compare the actual received PSD to the reference PSD. If necessary, it shall instruct the 10PASS-TS-R to fine-tune its PSD.

The 10PASS-TS-O shall also have the capability to directly impose a maximum allowed transmit PSD at the 10PASS-TS-R. This maximum transmit PSD shall also be input via the management interface and shall be transmitted from 10PASS-TS-O to 10PASS-TS-R in the early stages of the initialization. The 10PASS-TS-O shall allow the operator to select one of these two methods. If the PBO is defined as a maximum transmit PSD at the 10PASS-TS-R, the 10PASS-TS-R shall adjust its transmit PSD such that it does not exceed the maximum allowed transmit PSD. The restrictions specified in the previous paragraph shall also apply in this case (i.e., the 10PASS-TS-O shall not impose a transmit PSD mask that violates the mask specified there).

62.3.4.5 Changes to 8.2.5, “Constellation encoder”

In 8.2.5 of MCM-VDSL, the constraints on B_{max_d} and B_{max_u} are replaced by the following constraints:

$$B_{max\_d} = 12 \quad (62–3)$$

$$B_{max\_u} = 12 \quad (62–4)$$

62.3.4.6 Band notch profiles

The requirements specified in 62A.3.5 are to be met.

All other subclauses in MCM-VDSL Clause 8 are referenced as is.

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62.3.4.7 Changes to section 10, “Operations and maintenance”

Referenced as is, with the addition of the mapping between VTU-R data registers and Clause 45 register access shown in Table 62–4.

Table 62–4—Mapping of VTU-R data registers to Clause 45

VTU-R data register (eoc)		Clause 45 register access 10PASS-TS-O		Clause 45 register access 10PASS-TS-R	
Register number	**Description[a]**	**register**	**Subclause**	**Clause 45 register**	**Subclause**
0_{16}	VTU-R vendor ID	not applicable			
1_{16}	VTU-R revision number	not applicable			
2_{16}	VTU-R serial number	not applicable			
3_{16}	Self-test results	PMA/PMD link status[b]	45.2.1.29.4	PMA/PMD link status[c]	45.2.1.29.4
4_{16}	Performance[d]	bytes 00_{16}–03_{16}: attainable DS rate	45.2.1.60	bytes 00_{16}–03_{16}: attainable DS rate	45.2.1.60
		bytes 04_{16}–05_{16}: FEC correctable errors	45.2.1.43	bytes 04_{16}–05_{16}: FEC correctable errors	45.2.1.41
		bytes 08_{16}–09_{16}: FEC uncorrectable errors	45.2.1.44	bytes 08_{16}–09_{16}: FEC uncorrectable errors	45.2.1.42
5_{16}	Vendor-discretionary	not applicable			
6_{16}	Loop attenuation	10P/2B line attenuation	45.2.1.38	10P/2B line attenuation	45.2.1.37
7_{16}	SNR margin	10P/2B RX SNR margin	45.2.1.36	10P/2B RX SNR margin	45.2.1.35
8_{16}	VTU-R configuration	not applicable			
9-F_{16}	For future use	not applicable			

[a]This is the description of the VTU-R data registers as given in MCM-VDSL.
[b]A non-zero value of the Self-test results register shall cause PMA/PMD link status to be cleared to 0.
[c]A non-zero value of the Self-test results register shall cause PMA/PMD link status to be cleared to 0.
[d]This field contains 16 bytes in total. The bytes that are not mapped to a Clause 45 register in this table, are reserved.

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62.3.4.8 Changes to 11.1, “VDSL Link State and Timing Diagram”

See Figure 62–4.

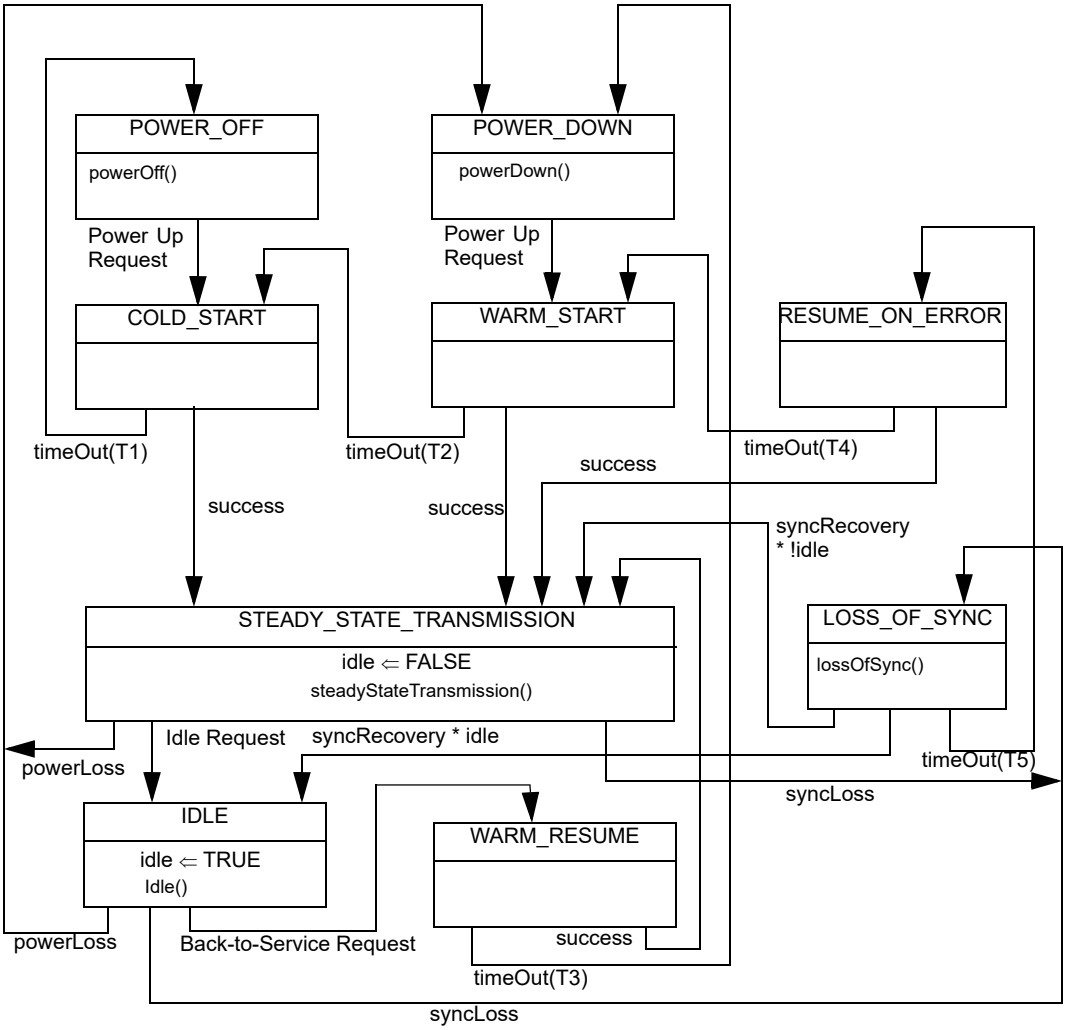

Figure 62–4—Link state and timing diagram

The function timeOut (time) returns FALSE upon entry of the associated state, and returns TRUE as soon as the interval specified by the argument “time” has expired. In addition, the state diagram uses following variables and constants:

T1
: Constant indicating the maximum cold-start activation time, equal to 10 000 ms

T2
: Constant indicating the maximum warm-start activation time, equal to 5000 ms

T3
: Constant indicating the maximum warm-resume activation time, equal to 100 ms

T4
: Constant indicating the maximum resume-on-error activation time, equal to 300 ms

T5
: Constant indicating the maximum sync-loss recovery time, equal to 200 ms

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idle Variable that indicates if the PMD has transitioned from STEADY_STATE_TRANSMISSION to IDLE. The idle variable becomes TRUE when the PMD enters the IDLE state, and becomes FALSE when the PMD enters the STEADY_STATE_TRANSMISSION mode.

success
Variable that is TRUE if and only if the procedures in the associated state were completed without error.

The following procedures are introduced to represent the actions associated with various states, as defined in MCM-VDSL.

powerOff()
See description of *Power-off* in MCM-VDSL section 11.1.1.1

steadyStateTransmission()
See description of *Steady-State Transmission* in MCM-VDSL section 11.1.1.1

lossOfSync()
See description of *Loss of Sync (Loss of Signal)* in MCM-VDSL section 11.1.1.1

powerDown()
See description of *Power Down* in MCM-VDSL section 11.1.1.1

idle()
See description of *Idle* in MCM-VDSL section 11.1.1.1

The remaining actions and transitions are documented in MCM-VDSL section 11.1, referenced as is.

62.3.4.9 Changes to section 18 (Annex 4), “Handshake procedure for VDSL”

62.3.4.9.1 Replacement of 18.1, “Introduction”

The 10PASS-TS handshake procedure is based on ITU-T Recommendation G.994.1 (G.hs). The carrier set used is specified in 61.3. During the handshake procedure, the following parameters shall be transmitted:

a) The size of IDFT/DFT;
b) the initial length of the cyclic extension;
c) flags indicating the use of the optional band, 25–138 kHz.

The parameters above shall be encoded using the information fields specified in 61.4.

62.3.4.9.2 Replacement of 18.2, “Description of signals”

The carrier set and signals used are specified in 61.4.

62.3.4.9.3 Replacement of 18.3, “Message coding format”

The message coding format and field definition tables are specified in 61.4.

62.3.4.9.4 Replacement of 18.4.1, “Handshake - 10PASS-TS-O”

The detailed procedures for handshake at the 10PASS-TS-O are defined in Recommendation G.994.1. A 10PASS-TS-O, after power-up, loss of signal, recovery from errors during the initialization procedure, shall enter the initial G.994.1 state C-SILENT1. The 10PASS-TS-O may transition to the Initialization Reset Procedure under instruction from the network. From either state, operation shall proceed according to the procedures defined in G.994.1.

If Recommendation G.994.1 procedures select 10PASS-TS as the mode of operation, the 10PASS-TS-O shall transition to state O-QUIET at the conclusion of G.994.1 operation.

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A 10PASS-TS-O wishing to indicate 10PASS-TS capabilities during in a G.994.1 CL message shall do so by setting to 1_b the Level 1 SPar(1)10PASS-TS bit as defined in G.994.1. The NPar(2) and SPar(2) fields corresponding to the "10PASS-TS" Level 1 bit are defined in 61.4. For each Level 2 SPar(2) bit set to 1_b, a corresponding NPar(3) field shall also be present. These NPar(3) fields are defined in 61.4. The Level 2 bits in a CL message are defined in Table 62–5 and Table 62–6.

Table 62–5—10PASS-TS-O CL message NPar(2) bit definitions

NPar(2) bit	Definition
Upstream use of 25 kHz–138 kHz band	If set to 1_b, signifies that the 10PASS-TS-O is capable of using the band between 25 kHz and 138 kHz and that the band can be used for the upstream transmission.
Downstream use of 25 kHz–138 kHz band	If set to 1_b, signifies that the 10PASS-TS-O is capable of using the band between 25 kHz and 138 kHz and that the band can be used for the downstream transmission.
EOC-Clear	If set to 1_b, signifies that the 10PASS-TS-O supports transmission and reception of G.997.1 OAM frames.

Table 62–6—10PASS-TS-O CL message SPar(2) bit definitions

NPar(2) bit	Definition
Used bands in upstream	The use of this bit is optional. If set to 1_b, indicates the used upstream bands. The optional band between 25 kHz and 138 kHz shall not be included.
Used bands in downstream	The use of this bit is optional. If set to 1_b, indicates the used downstream bands. The optional band between 25 kHz and 138 kHz shall not be included.
IDFT/DFT size	Always set to 1_b in a CL message. Indicates the maximum IDFT/DFT size that 10PASS-TS-O can support. The value shall be present in the corresponding NPar(3) field.
Initial length of *CE*	If set to 0_b, it signifies that the 10PASS-TS-O can support only the mandatory cyclic extension length of $40*2^n$ for a number of tones equal to $256*2^n$. If set to 1_b in a CL message, it indicates the initial sample length of the cyclic extension that 10PASS-TS-O can support. It also signifies that the 10PASS-TS-O can support CE lengths other than the mandatory length. The value shall be present in the corresponding NPar(3) field. If one of the modems supports only the mandatory value, then this value shall be used.
RFI bands	The use of this bit is optional. If set to 1_b, indicates the RFI bands.

A PHY selecting 10PASS-TS mode of operation in a G.994.1 MS message shall do so by setting to 1_b the Level 1 SPar(1) 10PASS-TS-O bit as defined in G.994.1. The NPar(2) and SPar(2) fields corresponding to this bit are defined in 61.3. For each Level 2 SPar(2) bit set to 1b, a corresponding NPar(3) field shall also be present, as defined in 61.3. The Level 2 bits in an MS message from the 10PASS-TS-O are defined in Table 62–7 and Table 62–8.

If both bits Upstream use of optional band and Downstream use of optional band are enabled in the CL and CLR message, one and only one of the bits shall be set to 1_b in an MS message sent from the 10PASS-TS-O, and the use of the band between 25 kHz and 138 kHz is at the 10PASS-TS-O's discretion. If the 10PASS-TS-O and 10PASS-TS-R have no common usage of the optional band, both bits shall be set to 0_b in an MS message sent from the 10PASS-TS-O.

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Table 62–7—10PASS-TS-O MS message NPar(2) bit definitions

NPar(2) bit	Definition
Upstream use of 25 kHz–138 kHz band	Set to 1_b if and only if this bit was set to 1_b in both the last previous CL message and the last previous CLR message. It signifies that the band between 25 kHz and 138 kHz shall be used for the upstream transmission.
Downstream use of 25 kHz–138 kHz band	Set to 1_b if and only if this bit was set to 1_b in both the last previous CL message and the last previous CLR message. It signifies that the band between 25 kHz and 138 kHz shall be used for the downstream transmission.
EOC-Clear	Set to 1_b if and only if this bit was set to 1_b in both the last previous CL message and the last previous CLR message. Signifies that both 10PASS-TS-O and 10PASS-TS-R may transmit and receive G.997.1 OAM frames.

Table 62–8—10PASS-TS-O MS message SPar(2) bit definitions

NPar(2) bit	Definition
Used bands in upstream	Always set to 0_b in an MS message.
Used bands in downstream	Always set to 0_b in an MS message.
IDFT/DFT size	Always set to 1_b in an MS message. Indicates the maximum IDFT/DFT size that both 10PASS-TS-O and 10PASS-TS-R can support. The value shall be present in the corresponding NPar(3) field.
Initial length of *CE*	Set to 0_b if and only if this bit was set to 0_b in the last previous CL message or the last previous CLR message, or both. It signifies that both 10PASS-TS-O and 10PASS-TS-R shall use only the mandatory cyclic extension length. Set to 1_b if and only if this bit was set to 1_b in both the last previous CL message and the last previous CLR message. It indicates the initial sample length of the cyclic extension. It also signifies that both 10PASS-TS-O and 10PASS-TS-R can support CE lengths other than the mandatory length. The value shall be given in the corresponding NPar(3) field.
RFI bands	Always set to 0_b in an MS message.

62.3.4.9.5 Replacement of 18.4.2, “Handshake - 10PASS-TS-R”

The detailed procedures for handshake at the 10PASS-TS-R are defined in Recommendation G.994.1. An 10PASS-TS-R, after power-up, loss of signal, recovery from errors during the initialization procedure, shall enter the initial G.994.1 state R-SILENT0. Upon command from the host controller, the 10PASS-TS-R shall initiate handshaking by invoking the Initialization Reset Procedure. Operation shall then proceed according to the procedures defined in G.994.1.

If Recommendation G.994.1 procedures select 10PASS-TS as the mode of operation, the 10PASS-TS-R shall transition to state R-QUIET at the conclusion of G.994.1 operation.

A 10PASS-TS-R wishing to indicate 10PASS-TS capabilities during in a G.994.1 CLR message shall do so by setting to 1_b the Level 1 SPar(1) 10PASS-TS bit as defined in G.994.1. The NPar(2) and SPar(2) fields corresponding to the “10PASS-TS” Level 1 bit are defined in 61.4. For each Level 2 SPar(2) bit set to 1_b, a corresponding NPar(3) field shall also be present. These NPar(3) fields are defined in 61.4. The Level 2 bits in a CLR message are defined in Table 62–9 and Table 62–10.

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Table 62–9—10PASS-TS-R CLR message NPar(2) bit definitions

NPar(2) bit	Definition
Upstream use of 25 kHz–138 kHz band	If set to 1_b, signifies that the 10PASS-TS-R is capable of using the band between 25 kHz and 138 kHz and that the band can be used for the upstream transmission.
Downstream use of 25 kHz–138 kHz band	If set to 1_b, signifies that the 10PASS-TS-R is capable of using the band between 25 kHz and 138 kHz and that the band can be used for the downstream transmission.
EOC-Clear	If set to 1_b, signifies that the 10PASS-TS-R supports transmission and reception of G.997.1 OAM frames.

Table 62–10—10PASS-TS-R CLR message SPar(2) bit definitions

NPar(2) bit	Definition
Used bands in upstream	Always set to 0_b in a CLR message.
Used bands in downstream	Always set to 0_b in a CLR message.
IDFT/DFT size	Always set to 1_b in a CLR message. Indicates the maximum IDFT/ DFT size that 10PASS-TS-R can support. The value shall be present in the corresponding NPar(3) field.
Initial length of *CE*	If set to 0_b, it signifies that the 10PASS-TS-R can support only the mandatory cyclic extension length of 40×2^n for a number of tones equal to 256×2^n. If set to 1_b in a CLR message, it indicates the initial sample length of the cyclic extension that 10PASS-TS-R can support. It also signifies that the 10PASS-TS-R can support CE lengths other than the mandatory length. The value shall be present in the corresponding NPar(3) field. If one of the modems supports only the mandatory value, then this value shall be used.
RFI bands	Always set to 0_b in a CLR message.

A 10PASS-TS-R selecting 10PASS-TS mode of operation in a G.994.1 MS message shall do so by setting to 1_b the Level 1 SPar(1) 10PASS-TS bit as defined in G.994.1. The NPar(2) and SPar(2) fields corresponding to this bit are defined in 61.4. For each Level 2 SPar(2) bit set to 1_b, a corresponding NPar(3) field shall also be present, as defined in 61.4. The Level 2 bits in an MS message from the 10PASS-TS-R are defined in Table 62–11 and Table 62–12.

If both bits Upstream use of optional band and Downstream use of optional band are enabled in the CL and CLR message, one and only one of the bits shall be set to 1_b in an MS message sent from the 10PASS-TS-R, and the use of the band between 25 kHz and 138 kHz shall be at the 10PASS-TS-R's discretion. If the 10PASS-TS-O and 10PASS-TS-R have no common usage of the optional band, both bits shall be set to 0_b in an MS message sent from the 10PASS-TS-R.

62.3.5 Transmission medium interface characteristics

This subclause specifies the interface between the transceiver and the transmission medium (U2 reference point). The interface at U1 reference point (see MCM-VDSL Section 5.1 for VDSL reference model) is specified by the corresponding characteristics of the service splitter. The definition of the service splitter is outside the scope of this standard. Relevant specifications may be found in MCM-VDSL Clause 21 and Clause 22.

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Table 62–11—10PASS-TS-R MS message NPar(2) bit definitions

NPar(2) bit	Definition
Upstream use of 25 kHz–138 kHz band	Set to 1_b if and only if this bit was set to 1_b in both the last previous CL message and the last previous CLR message. It signifies that the band between 25 kHz and 138 kHz shall be used for the upstream transmission.
Downstream use of 25 kHz–138 kHz band	Set to 1_b if and only if this bit was set to 1_b in both the last previous CL message and the last previous CLR message. It signifies that the band between 25 kHz and 138 kHz shall be used for the downstream transmission.
EOC-Clear	Set to 1_b if and only if this bit was set to 1_b in both the last previous CL message and the last previous CLR message. Signifies that both 10PASS-TS-O and 10PASS-TS-R may transmit and receive G.997.1 OAM frames.

Table 62–12—10PASS-TS-R MS message SPar(2) bit definitions

NPar(2) bit	Definition
Used bands in upstream	Always set to 0_b in an MS message.
Used bands in downstream	Always set to 0_b in an MS message.
IDFT/DFT size	Always set to 1_b in an MS message. Indicates the maximum IDFT/DFT size that both 10PASS-TS-O and 10PASS-TS-R can support. The value shall be present in the corresponding NPar(3) field.
Initial length of *CE*	Set to 0_b if and only if this bit was set to 0_b in the last previous CL message or the last previous CLR message, or both. It signifies that both 10PASS-TS-O and 10PASS-TS-R shall use only the mandatory cyclic extension length. Set to 1_b if and only if this bit was set to 1_b in both the last previous CL message and the last previous CLR message. It indicates the initial sample length of the cyclic extension. It also signifies that both 10PASS-TS-O and 10PASS-TS-R can support CE lengths other than the mandatory length. The value shall be given in the corresponding NPar(3) field.
RFI bands	Always set to 0_b in an MS message.

62.3.5.1 Transmit signal characteristics

62.3.5.1.1 Wide-band power

The average wide-band power of the transmitted 10PASS-TS signal measured over the frequency range between 25 kHz to 12 MHz shall be no greater than the values listed in Table 62–13 when terminated with resistive impedance of $R_V = 100\ \Omega$.

NOTE 1—For compliance with this requirement, the 10PASS-TS transceiver is terminated with the impedance R_V and configured to transmit pseudo-random data with any repetitive framing patterns enabled.

NOTE 2—Power is measured across the termination resistance of R_V. No energy is inserted into the POTS/ISDN port of the splitter (if applied) during this test.

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Table 62–13—10PASS-TS maximum transmit power

Central office deployment scenario		Cabinet deployment scenario	
Downstream [dBm]	**Upstream [dBm]**	**Downstream [dBm]**	**Upstream [dBm]**
14.5	14.5	11.5	14.5

62.3.5.1.2 Power spectral density (PSD)

Transmit PSD is characterized by the PSD template and PSD mask. PSD templates and masks are defined in Annex 62A.

62.3.5.1.3 Egress control

To avoid potential harm to amateur radio service due to radiated emission from 10PASS-TS, it shall be possible to reduce the PSD of the transmit signal within the amateur radio bands. Specifications for egress power control are described in Annex 62A.

62.3.5.2 Termination impedance

A termination impedance of $R_v = 100\ \Omega$ (purely resistive, either source or load) shall be used over the entire 10PASS-TS frequency band for both the 10PASS-TS-O and 10PASS-TS-R when matching to the metallic wire-pair.

This termination impedance approximates (and is based upon) the insertion-point impedance of the 10PASS-TS test loop. It enables a compromise high-frequency impedance match to the various types of unshielded cable in metallic access networks.

62.3.5.3 Return loss

The return loss requirement is defined to limit signal power uncertainties due to the tolerance of the line interface impedance. The return loss *RL* specifies the amount of reflected differential signal upon a reference impedance R_V

$$RL = 20 \times \log\left|\frac{Z + R_V}{Z - R_V}\right| \tag{62–5}$$

where Z is the internal impedance of the VTU. Note that in Equation (62–5), the log is taken to base 10, such that *RL* is expressed in dB.

The in-band return loss value of the 10PASS-TS transceiver shall be greater than or equal to 12 dB. The out-of-band return loss value shall be greater than or equal or 3 dB. In-band and out-of-band frequencies are defined by the frequency plan as shown in Figure 62–3 and by the transmit direction.

The value of 12 dB assumes a flat transmit PSD is applied over the entire in-band region. Requirements may be relaxed in the frequency ranges of reduced PSD values. The exact value requirements are outside the scope of this standard.

The return loss shall be measured on a resistive test load of $R_V = 100\ \Omega$ while the tested implementation of the 10PASS-TS transceiver is powered.

NOTE—If a splitter is used, the return-loss requirements should be met for the full range of possible values of the POTS/ISDN port termination.

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62.3.5.4 Output signal balance

Output signal balance (*OSB*) is a measure of unwanted longitudinal signals at the output of the transceiver, as defined by Equation (62–6). The longitudinal output voltage (V_{cm}) to the differential output voltage (V_{diff}) ratio shall be measured while the 10PASS-TS transmitter is active in accordance with ITU-T Recommendation G.117 and ITU-T Recommendation O.9.

$$OSB = 20\log\left|\frac{V_{diff}}{V_{cm}}\right| \tag{62–6}$$

The *OSB* of the 10PASS-TS transceiver shall be equal to or greater than 35 dB in the entire 10PASS-TS band.

NOTE—The equipment balance should be better than the anticipated cable balance in order to minimize the unwanted emissions and susceptibility to external RFI. The typical worst case balance for an aerial drop-wire has been observed to be in the range 30 dB – 35 dB, therefore the balance of the 10PASS-TS equipment should be equal or better.

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62.4 Protocol implementation conformance statement (PICS) proforma for Clause 62, Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD), type 10PASS-TS[123]

62.4.1 Introduction

The supplier of a protocol implementation that claimed to conform to Clause 62, Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD), type 10PASS-TS, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

62.4.2 Identification

62.4.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification--e.g., names and versions for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

62.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 62, Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD), type 10PASS-TS.
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[123] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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62.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
10PPMA	MCM-VDSL based PMA	62.2	The PMA based on the PMS-TC specified in ATIS-0600424 is implemented.	M	Yes [ ]
10PPMD	MCM-VDSL based PMD	62.3	The PMD based on the PMD specified in ATIS-0600424 is implemented.	M	Yes [ ]

62.4.4 PICS proforma tables for the Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD), type 10PASS-TS

62.4.4.1 MCM-VDSL based PMA

Item	Feature	Subclause	Value/Comment	Status	Support
10PPMA-1	DMT PMA functional specifications	62.2	All data bytes are transmitted MSB first.	M	Yes [ ]
10PPMA-2	DMT PMA functional specifications	62.2	All serial processing is performed LSB first, with the outside world MSB considered as the VDSL LSB.	M	Yes [ ]
10PPMA-3	Specific requirements and exceptions	62.2.4	The 10PASS-TS PMA complies to the requirements of MCM-VDSL Section 9.3, with the exception of support for the fast path, support for V>1, NTR, and TPS-TC specific bits as listed.	M	Yes [ ]
10PPMA-4	Specific requirements and exceptions: Reed-Solomon	62.2.4.2	The 10PASS-TS PMA supports Reed-Solomon settings (144,128) and (240, 224).	M	Yes [ ]
10PPMA-5	Specific requirements and exceptions: Interleaver	62.2.4.2	For (N,K) = (144,128) the following values for M and I are supported: I=36 and M between 2 and 52. For (N,K)=(240,224) the following values for M and I are supported: I=30 and M between 2 and 62.	M	Yes [ ]

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62.4.4.2 MCM-VDSL based PMD

Item	Feature	Subclause	Value/Comment	Status	Support
10PPMD-1	Specific requirements and exceptions	62.3.4	The PMD complies to the requirements of MCM-VDSL Section 8, Section 10, Section 11, and Section 12, with the exceptions listed.	M	Yes [ ]
10PPMD-2	Duplexing and Modulation	62.3.4.1	The PMD uses Frequency Division Duplexing to separate upstream and downstream transmission.	M	Yes [ ]
10PPMD-3	Duplexing and Modulation	62.3.4.1	The PMD supports modulation of N_{SC} = 4096 subcarriers.	M	Yes [ ]
10PPMD-4	Duplexing and Modulation	62.3.4.1	The PMD supports modulation of B_{max_d} = 12 bits per downstream subcarrier and B_{max_u} = 12 bits per upstream subcarrier.	M	Yes [ ]
10PPMD-5	Duplexing and Modulation	62.3.4.1	Disjoint subsets of the N_{SC} subcarriers are defined for use in the downstream and upstream directions.	M	Yes [ ]
10PPMD-6	Duplexing and Modulation	62.3.4.1	The exact subsets of subcarriers used to modulate data in each direction are determined during initialization, based on management system settings and the signal-to-noise ratios of the subchannels.	M	Yes [ ]
10PPMD-7	Duplexing and Modulation	62.3.4.1	The use of the band between 25 kHz and 138 kHz is negotiated during the initialization to indicate if the capability exists and select one of the following options: use for upstream transmission, use for downstream transmission, not used.	M	Yes [ ]
10PPMD-8	Duplexing and Modulation	62.3.4.1	10PASS-TS-O PMD supports the transmission of a pilot tone on any downstream tone.	M	Yes [ ]
10PPMD-9	Upstream Power Back-Off	62.3.4.1	Upstream power back-off is applied to mitigate the effects of FEXT from short lines into long lines in distributed cable topologies.	M	Yes [ ]
10PPMD-10	Upstream Power Back-Off	62.3.4.1	The PMD is capable of performing frequency-dependent power back-off.	M	Yes [ ]
10PPMD-11	Upstream Power Back-Off	62.3.4.1	It is possible for the network management system to set the limiting transmit PSD template PSD_0 for the 10PASS-TS-R to one of the standard transmit PSD templates as defined in the applicable section of 62A.3.4.	M	Yes [ ]
10PPMD-12	Upstream Power Back-Off	62.3.4.1	The 10PASS-TS-R PMD performs UPBO autonomously, i.e., without sending any significant information to the 10PASS-TS-O until the UPBO is applied.	M	Yes [ ]
10PPMD-13	Upstream Power Back-Off	62.3.4.1	The 10PASS-TS-O is capable of adjusting the transmit PSD selected by the 10PASS-TS-R, after UPBO has been applied. The adjusted transmit PSD is subject to the limitations given in the applicable section of 62A.3.3.	M	Yes [ ]

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10PPMD-14	Upstream Power Back-Off	62.3.4.1	The 10PASS-TS-R estimates the insertion losses of the upstream bands based on the received downstream signals. The 10PASS-TS-R explicitly estimates the electrical length of its line, kl_0, and uses this value to calculate the transmit PSD template TxPSD per Equation (62–1) and Equation (62–2).	M	Yes [ ]
10PPMD-15	Upstream Power Back-Off	62.3.4.1	The 10PASS-TS-R adapts its transmit signal PSD to conform to the template TxPSD and the corresponding PSD mask which is defined in the applicable section of 62A.3.3. The same bandwidth as for all regular transmit PSD masks defined in the applicable section of 62A.3.3 are used to check the conformance of TxPSD with power back-off. Conformance with the PSD template is verified using a 100 kHz sliding window in the in-band frequency range below 1 MHz and a 1 MHz sliding window in the in-band frequency range above 1 MHz.	M	Yes [ ]
10PPMD-16	Upstream Power Back-Off	62.3.4.1	PSD_REF is input via the management interface.	M	Yes [ ]
10PPMD-17	Upstream Power Back-Off	62.3.4.1	PSD_REF is transmitted from the 10PASS-TS-O to the 10PASS-TS-R.	M	Yes [ ]
10PPMD-18	Upstream Power Back-Off	62.3.4.1	The 10PASS-TS-R takes a tone-by-tone minimum of this computed PSD and the maximum allowed transmit PSD in the upstream direction. The result is used as the initial upstream transmit PSD.	M	Yes [ ]
10PPMD-19	Upstream Power Back-Off	62.3.4.1	Upon receiving signals from the 10PASS-TS-R, the 10PASS-TS-O compares the actual received PSD to the reference PSD. If necessary, it instructs the 10PASS-TS-R to fine-tune its PSD.	M	Yes [ ]
10PPMD-20	Upstream Power Back-Off	62.3.4.1	The 10PASS-TS-O has the capability to directly impose a maximum allowed transmit PSD at the 10PASS-TS-R.	M	Yes [ ]
10PPMD-21	Upstream Power Back-Off	62.3.4.1	The maximum transmit PSD is input via the management interface.	M	Yes [ ]
10PPMD-22	Upstream Power Back-Off	62.3.4.1	The maximum transmit PSD is transmitted from 10PASS-TS-O to 10PASS-TS-R during initialization.	M	Yes [ ]
10PPMD-23	Upstream Power Back-Off	62.3.4.1	The 10PASS-TS-O allows the operator to select between the UPBO method based on Reference PSD and the UPBO method based on maximum transmit PSD.	M	Yes [ ]
10PPMD-24	Handshake	62.3.4.9	The handshake uses the 4.3125 kHz signaling family and the duplex transmission mode.	M	Yes [ ]

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10PPMD-25	Handshake	62.3.4.9	The handshake proceeds as specified in 61.4.	M	Yes [ ]
10PPMD-26	Wide-band power	62.3.5.1.1	The average wide-band power of the transmitted 10PASS-TS signal measured over the frequency range between 25 kHz to 12 MHz is no greater than the values listed in Table 62–13 when terminated with resistive impedance of RV = 100 Ohm.	M	Yes [ ]
10PPMD-27	Egress control	62.3.5.1.3	To avoid potential harm to amateur radio service due to radiated emission from 10PASS-TS, it is possible to reduce the PSD of the transmit signal within the amateur radio bands.	M	Yes [ ]
10PPMD-28	Termination impedance	62.3.5.2	A termination impedance of Rv = 100 Ohm is used over the entire 10PASS-TS frequency band for both the 10PASS-TS-O and 10PASS-TS-R when matching to the metallic wire-pair.	M	Yes [ ]
10PPMD-29	Return loss	62.3.5.3	The in-band return loss value of the 10PASS-TS transceiver are greater than or equal to 12 dB.	M	Yes [ ]
10PPMD-30	Return loss	62.3.5.3	The out-of-band return loss value are greater than or equal or 3 dB.	M	Yes [ ]
10PPMD-31	Return loss	62.3.5.3	Requirements are relaxed in the frequency ranges of reduced PSD values.	O	Yes [ ] No [ ]
10PPMD-32	Return loss	62.3.5.3	The return loss are measured on a resistive test load of R_V = 100 Ohm while the tested implementation of the 10PASS-TS transceiver is powered.	M	Yes [ ]
10PPMD-33	Output signal balance	62.3.5.4	The longitudinal output voltage to the differential output voltage ratio is measured while the VTU transmitter is active in accordance with ITU-T Recommendation G.117 and ITU-T Recommendation O.9.	M	Yes [ ]
10PPMD-34	Output signal balance	62.3.5.4	The OSB of the 10PASS-TS transceiver is equal to or greater than 35 dB in the entire 10PASS-TS band.	M	Yes [ ]

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63. Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD), type 2BASE-TL

63.1 2BASE-TL Overview

63.1.1 Scope

This clause specifies the 2BASE-TL Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD) sublayer for voice grade twisted-pair wiring. In order to form a complete 2BASE-TL PHY, the 2BASE-TL PMA and PMD are integrated with the TC and PCS of Clause 61. Parts of register 3.0, parts of register 3.4 and registers 3.60 through 3.73 specified in Clause 45 may be used to control the PCS of Clause 61. Parts of register 6.0 and registers 6.16 through 6.23 specified in Clause 45 may be used to control the TC sublayer of Clause 61. Registers 1.16 through 1.42 and 1.80 through 1.109 specified in Clause 45 may be used to control the 2BASE-TL PMA and PMD.

63.1.2 Objectives

The following are the objectives for the 2BASE-TL PMA and PMD:

a) To provide 2 Mb/s encapsulated packet data rate at the α(β)-interface.

b) To provide full duplex operation.

c) To provide for operating over non-loaded voice grade twisted pair cable at distances up to 2700 m.

d) To provide a communication channel with a mean bit error ratio, at the α(β)-interface, of less than one part in 10^7 with 5 dB noise margin.

63.1.3 Relation of 2BASE-TL to other standards

The specifications of the 2BASE-TL PMA and PMD are based on the SHDSL transceiver (PMD and PMS-TC) specified in ITU-T Recommendation G.991.2.

Item	Feature	Subclause	Value/Comment	Status	Support

63.1.4 Summary of Physical Medium Attachment (PMA) specification

This layer is defined by the α(β)-interface and the I-interface. Figure 63–1 shows a functional diagram of the 2BASE-TL PMA layer functionality. The payload is formed into a 2BASE-TL PMA frame with overhead added (for example, the PME aggregation Header). The framed data is then scrambled and sent to the PMD sublayer. One distinguishes between the data mode PMA specification that is used during normal data operation and the activation PMA specification that is used when the PMD is training.

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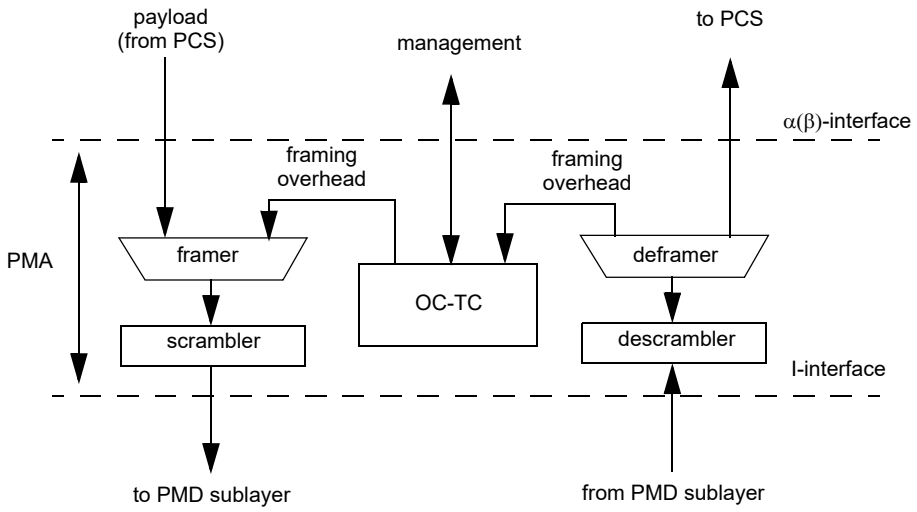

Figure 63–1—Diagram of PMA sublayer

63.1.4.1 α(β)-interface

A complete definition of the α(β)-interface is contained in 61.3.2. The signal PMA_receive_synchronized, defined in 61.3.2.2, shall be asserted when the LOSW bit is set to 0 (see 63.2.2.2), and deasserted when the LOSW is set to 1.

63.1.4.2 The I-interface

The I_O and I_R reference points define interfaces between the PMA and PMD in the 2BASE-TL-O and 2BASE-TL-R, respectively. Both interfaces are functional, application independent and identical. Both interfaces are defined by the following signal flows:

a) Data flow
b) Synchronization flow

The specification of the I-interface is implicit in ITU-T Recommendation G.991.2.

63.1.4.2.1 The I Data Flow

The data flow consists of two octet-oriented streams, both with the PMA frame format, with the bit rates defined by the PMD transmission profile:

a) Transmit data (Tx)
b) Receive data (Rx)

If data streams are implemented serially, the LSB of each octet (i.e., b_8 of Figure 61–16) shall be sent first. In section 7.1.1 of G.991.2, with i = 0, the payload blocks are made of a stream of octets. Each octet consists of 8 bits. The first bit of each octet (i.e., lowest frame bit number in an octet) maps to b_8 in Figure 61–16 and the last bit of each octet maps to b_1 of Figure 61–16.

Each stream bit rate value is set during PMD configuration.

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63.1.4.2.2 I Synchronization Flow

The synchronization flow consists of the transmitted and received octet synchronization signals (Clko_t, Clko_r). Optional transmit and receive bit-synchronization signals (Clkp_t, Clkp_r) are defined too.

Synchronization signals are asserted by the PMD and directed towards the PMA.

The synchronization signals are described in Table 63–1.

Table 63–1—I-interface signals

Signal(s)	Description	Direction	Notes
Data Signals			
Tx	Transmit data stream	PMA → PMD	Transmission frame format.
Rx	Receive data stream	PMA ← PMD	
Synchronization Signals			
Clko_t	Transmitted octet timing	PMA ← PMD	
Clko_r	Received octet timing	PMA ← PMD	
Clkp_t	Transmitted bit timing	PMA ← PMD	Optional
Clkp_r	Received bit timing	PMA ← PMD	Optional

63.1.4.3 Operation Channel (OC)

The OC-TC function of the PMA shall receive the EOC and overhead indicators over the OC-TC interface. For each 2BASE-TL PMA frame, the OC shall deliver a fixed number of embedded operations channel (EOC) and overhead indicators bits to the framer. These bits shall be included in the overhead sections of the 2BASE-TL PMA frames.

63.1.5 Summary of Physical Medium Dependent (PMD) specification

The PMD specification is based on Pulse Amplitude Modulation (PAM) and is divided into three consecutive phases, summarized as follows:

a) Preactivation: during this phase, the PMDs determine each other capabilities and the bit rate they will operate at in data mode. Reference section 6.3.1 (included in this standard per 63.3.2.2) describes the preactivation reference model. The preactivation uses G.994.1 as a handshake mechanism to exchange parameters in accordance with the specifications in 61.4. It also offers an optional line probing capability. The line probe uses 2-level PAM signals to determine a suitable bit rate to run at on the copper link.
b) Activation: during this phase, the PMDs train and exchange information necessary to adapt and operate the various filters and processes necessary during data mode operation. Reference section 6.2.1 describes the Activation reference model. The activation uses 2-level PAM to train the various filters.
c) Data Mode: once pre-activation and activation are complete, the PMD can start transmitting payload data. Reference section 6.1.1 describes the Data Mode reference model.

NOTE—Line activation takes place after entire discovery and PME aggregation operation.

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63.2 2BASE-TL PMA functional specifications

The 2BASE-TL PMA is specified by incorporating the SHDSL standard, ITU-T Recommendation G.991.2 (02/2001) with the changes specified in G.991.2 Amendment 1 (11/2001), by reference, with the modifications noted below. This standard provides support for voice-grade twisted pair. For improved legibility in this clause, ITU-T Recommendation G.991.2 and G.991.2 Amendment 1, will henceforth be referred to as G.991.2.

63.2.1 General exceptions

The 2BASE-TL PMA is precisely the PMS-TC specified in G.991.2, with the following general modifications:

a) There are minor terminology differences between this standard and G.991.2 that do not cause ambiguity. The terminology used in 2BASE-TL was chosen to be consistent with other IEEE 802 standards, rather than with G.991.2. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 63–2.

Table 63–2—Interpretation of general G.991.2 terms and concepts

G.991.2 term or concept	Interpretation for 2BASE-TL
PMS-TC	PMA
STU-C, LT	2BASE-TL-O
STU-R, NT	2BASE-TL-R
Transmission medium dependent interface, U-interface	MDI
byte	octet

b) The 2BASE-TL PMA supports only one channel of user data with an associated γ-interface.
c) The 2BASE-TL PMA does not support the optional “four-wire mode”. Operation over multiple pairs is optional; if implemented, multi-pair operation shall comply to the specifications in 61.2.2.
d) The 2BASE-TL PMA does not support “plesiochronous mode”.
e) The 2BASE-TL PMA shall be octet oriented; hence, the bit oriented parameter *i* defined for Equation (63–1) shall be equal to *0* in all cases.
f) The 2BASE-TL PMA does not support the notion of “sub-blocks” in the Payload Block. Each payload block consists of a contiguous sequence of 12*n* octets, with parameter *n* as defined for Equation (63–1).

63.2.2 Specific requirements and exceptions

The 2BASE-TL PMA shall comply to the requirements of G.991.2 Section 7 and Section 9 with the exceptions listed below. Where there is conflict between specifications in G.991.2 and those in this standard, those of this standard shall prevail.

Implementation of optional specifications in G.991.2 is not required for compliance with this standard. Reference Section 8 (TPS-TC Layer Functional Characteristics), Reference Annex D (Signal Regenerator Operation), Reference Annex E (Application-specific TPS-TC Framing) and Reference Appendices I, II, and III are out of scope for 2BASE-TL PMA. Deployment of compatible versions of G.991.2 Annex D is an implementation specific option for the purposes of 2BASE-TL.

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63.2.2.1 Changes to 7.1, “Data Mode Operation”

Reference 7.1.1 (Frame Structure) is replaced with the following:

Table 7-1 of the Reference summarizes the SHDSL frame structure. Complete bit definitions may be found in Reference 7.1.2. The size of each payload block is defined as k bits, where $k = 96n$. The payload rate r (in kb/s) is given by Equation (63–1) and Equation (63–3), with $i = 0$. The value of n is limited by Equation (63–2) and Equation (63–4).

Reference 7.1.2.6 (Stuff Indicator bits) is replaced with the following:

2BASE-TL operates in synchronous mode, therefore *sbid1* and *sbid2* are spare bits.

Reference 7.1.2.7 (Stuffing Bits) is replaced with the following:

2BASE-TL operates in synchronous mode, therefore *stb1* and *stb2* shall be present in every frame, and *stb3* and *stb4* shall not be present.

Reference 7.1.4 (Frame synchronization) is replaced with the following:

The precise manner in which frame synchronization is acquired or maintained is the choice of the receiver designer. Since different frame synchronization algorithms may require different values for the bits of the FSW, a provision has been made to allow the receiver to inform the far end transmitter of the particular values that are to be used for this field in the transmitted PMS-TC frame.

All other subsections of Reference 7.1 are referenced as is.

63.2.2.2 Changes to Section 9, “Management”

Referenced as is, with the exception of 9.5.5.6 where Message IDs 17 “ATM Cell Status Request”, 20 “ISDN Request”, 145 “ATM Cell Status Information” and 148 “ISDN Response” are out of scope.

63.2.2.3 Relation between the 2BASE-TL registers and the SHDSL management functions

The parameters of the various 2BASE-TL registers of the -R device, defined in Clause 45, are gathered via the SHDSL management. SNR margin, code violations, ES, SES, LOSW, UAS, SNR margin defect, Loop attenuation defect and loss of sync word failure shall be obtained in the following way:

The 2BASE-TL-O shall send a Status Request (Msg ID 11) EOC message. If there has been any change in performance status other than SNR margin since the last time a unit was polled, the peer 2BASE-TL-R shall respond with an SHDSL Network Side Performance Status (Msg ID 140) EOC message.

The following octets and bits are then mapped to the Clause 45 registers (see Table 63–3):

Otherwise, the peer 2BASE-TL-R shall respond with a Status/SNR (Msg ID 139) EOC message, in which the SNR margin is communicated in octet 2.

Loop attenuation and SNR margin threshold for both 2BASE-TL-O and 2BASE-TL-R devices shall be set in the Clause 45 register of the 2BASE-TL-O device; the 2BASE-TL-R thresholds will be passed to the 2BASE-TL-R using message ID 3.

The segment defect is defined in section 9.2.4 and uses a dedicated framing bit rather than the EOC messaging.

The retrieval of the remote vendor ID is defined in G.997.1. The use of this mechanism is outside the scope of this standard.

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Table 63–3—Mapping of registers to "Network Side Performance Status" EOC message octets

register	octets / bits
LOSW failure	octet 2 / bit 1
Loop attenuation defect	octet 2 / bit 2
SNR margin defect	octet 2 / bit 3
SNR margin	octet 3
Loop attenuation	octet 4
ES	octet 5
SES	octet 6
Code violations	octet 7 and 8
LOSW	octet 9
UAS	octet 10
See footnote[a]	octet 11

[a]Bit 6 and 7 of octet 11 indicate that either an overflow or reset condition has occurred on any of the code violations / ES/ SES / LOSW / UAS registers.

NOTE—The code violation, ES, SES, LOSW, and UAS in SHDSL are modulo counters. The absolute value of the counter is meaningless, however the difference in between two consecutive readings provides the change in code violation/ES/SES/LOSW/UAS. If there are no changes in the performance registers, message ID 139 rather than 140 will be sent by the 2BASE-TL-R. It only contains the SNR value and none of the other parameters.

63.3 2BASE-TL PMD functional specifications

The 2BASE-TL PMD (and MDI) is specified by incorporating the SHDSL standard, ITU-T Recommendation G.991.2 (02/2001) with the changes specified in G.991.2 Amendment 1 (11/2001), by reference, with the modifications noted below. This standard provides support for voice-grade twisted pair. For improved legibility in this clause, ITU-T Recommendation G.991.2 and G.991.2 Amendment 1, will henceforth be referred to as G.991.2.

63.3.1 General exceptions

The 2BASE-TL PMD is precisely the PMD specified in G.991.2, with the following general modifications:

a) There are minor terminology differences between this standard and G.991.2 that do not cause ambiguity. The terminology used in 2BASE-TL was chosen to be consistent with other IEEE 802 standards, rather than with G.991.2. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 63–4.
b) The 2BASE-TL PMD does not support the optional "four-wire mode". Operation over multiple pairs is optional; if implemented, multi-pair operation shall comply to the specifications in 61.2.2.
c) The 2BASE-TL PMD does not support "plesiochronous mode".
d) The 2BASE-TL PMD shall be octet oriented; hence, the bit oriented parameter *i* defined for Equation (63–1) shall be equal to *0* in all cases.
e) The 2BASE-TL PMD shall support the use of the 32-TCPAM constellation for specific rates (see 63.3.2.1).
f) The 2BASE-TL PMD shall support the use of the enhanced SHDSL[124] extended bandwidths.

[124]"Enhanced SHDSL" refers to 32TC-PAM modulation and higher values of n as defined in Equation (63–2) and Equation (63–4), which are not part of ITU-T Recommendation G.991.2.

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Table 63–4—Interpretation of general G.991.2 terms and concepts

G.991.2 term or concept	Interpretation for 2BASE-TL
PMS-TC	PMA
STU-C, LT	2BASE-TL-O
STU-R, NT	2BASE-TL-R
Transmission medium dependent interface, U-interface	MDI

63.3.2 Specific requirements and exceptions

The 2BASE-TL PMD (including MDI) shall comply to the requirements of G.991.2 Section 5 (Transport Capacity), Section 6 (PMD Layer Functional Characteristics), Section 10 (Clock Architecture), Section 11 (Electrical Characteristics), Section 12 (Conformance Testing) with the exceptions listed below. The 2BASE-TL PMD supports the requirements of G.991.2 Annex A (Regional Requirements - Region 1) and Annex B (Regional Requirements - Region 2) with the exception of performance requirements, which are replaced by Annex 63B. Where there is conflict between specifications in G.991.2 and those in this standard, those of this standard shall prevail.

Implementation of optional specifications in G.991.2 is not required for compliance with this standard. Reference Section 8 (TPS-TC Layer Functional Characteristics), Reference Annex D (Signal Regenerator Operation), Reference Annex E (Application-specific TPS-TC Framing), and Reference Appendices I, II, and III are out of scope for the 2BASE-TL PMD.

63.3.2.1 Replacement of section 5, “Transport Capacity”

This recommendation specifies a two-wire operational mode for 2BASE-TL transceivers that is capable of supporting user (payload) data rates from 192 kb/s to 3.840 Mb/s, using the 16-TCPAM constellation, and 768 kb/s to 5.696 Mb/s, using the 32-TCPAM constellation. The allowed rates r (in kb/s), using the 16-TCPAM constellation, are given by Equation (63–1):

$$r = n \times 64 + i \times 8 \tag{63–1}$$

where

$$3 \le n \le 60\,. \tag{63–2}$$

The allowed rates r (in kb/s), using the 32-TCPAM constellation, are given by Equation (63–3):

$$r = n \times 64 + i \times 8 \tag{63–3}$$

where

$$12 \le n \le 89 \tag{63–4}$$

In all cases, i is restricted to the value of 0. See 63.3.2.4, 63.3.2.5 and 63.3.2.6 for details of specific regional requirements.

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63.3.2.2 Changes to section 6, "PMD Layer Functional Characteristics"

Referenced as is, with the exception of subsection 6.4 (G.994.1 Preactivation Sequence), which is supplanted by 61.4.

Section 6.1.2.3 is superseded by the following text:

Mapper:

The $K + 1$ bits $Y_K(m)$, ..., $Y_1(m)$, and $Y_0(m)$ shall be mapped to a level $x(m)$. In section 6.1.2.3 of G.991.2, the mapper function is specified for 16-TCPAM. This text extends that mapping to include both 16- and 32-TCPAM encodings. Table 63–5 shows the bit to level mapping for 16 and 32 level mapping.

Table 63–5—Mapping of bits to PAM levels

$Y_4(m)$	$Y_3(m)$	$Y_2(m)$	$Y_1(m)$	$Y_0(m)$	32-PAM (5 Bits)	16-PAM (4 Bits)
0	0	0	0	0	–31/32	–15/16
0	0	0	0	1	–29/32	–13/16
0	0	0	1	0	–27/32	–11/16
0	0	0	1	1	–25/32	–9/16
0	0	1	0	0	–23/32	–7/16
0	0	1	0	1	–21/32	–5/16
0	0	1	1	0	–19/32	–3/16
0	0	1	1	1	–17/32	–1/16
0	1	1	0	0	–15/32	1/16
0	1	1	0	1	–13/32	3/16
0	1	1	1	0	–11/32	5/16
0	1	1	1	1	–9/32	7/16
0	1	0	0	0	–7/32	9/16
0	1	0	0	1	–5/32	11/16
0	1	0	1	0	–3/32	13/16
0	1	0	1	1	–1/32	15/16
1	1	0	0	0	1/32	—
1	1	0	0	1	3/32	—
1	1	0	1	0	5/32	—
1	1	0	1	1	7/32	—
1	1	1	0	0	9/32	—
1	1	1	0	1	11/32	—

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Table 63–5—Mapping of bits to PAM levels *(continued)*

Y_4(m)	Y_3(m)	Y_2(m)	Y_1(m)	Y_0(m)	32-PAM (5 Bits)	16-PAM (4 Bits)
1	1	1	1	0	13/32	—
1	1	1	1	1	15/32	—
1	0	1	0	0	17/32	—
1	0	1	0	1	19/32	—
1	0	1	1	0	21/32	—
1	0	1	1	1	23/32	—
1	0	0	0	0	25/32	—
1	0	0	0	1	27/32	—
1	0	0	1	0	29/32	—
1	0	0	1	1	31/32	—

63.3.2.3 Changes to section 10, “Clock Architecture”

Referenced as is, with the exception of Reference Table 10-1, which is replaced by Table 63–6.

Table 63–6—Clock synchronization configurations

Mode number	2BASE-TL-O symbol clock reference	2BASE-TL-R symbol clock reference	Example application	Mode
3a	Transmit data clock	Received symbol clock	Main application is synchronous transport in both directions.	Synchronous

63.3.2.4 Changes to Annex A, “Regional Requirements—Region 1”

63.3.2.4.1 General Changes

Referenced as is, with the exception of optional support for asymmetric PSD masks. Asymmetric PSD masks are not supported by 2BASE-TL.

Section A.5.3 “Span Powering” is out of scope.

63.3.2.4.2 Additional requirement: wetting current

The 2BASE-TL-R shall be capable of sustaining 20 mA of wetting (sealing) current. The maximum rate of change of the wetting current shall be no more than 20 mA per second.

NOTE—The -R device cannot be guaranteed to operate correctly if more than 20 mA (tip to ring) is sourced.

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63.3.2.5 Changes to Annex B, “Regional Requirements—Region 2”

63.3.2.5.1 General changes

Referenced as is, with the exception of optional support for asymmetric PSD masks. Asymmetric PSD masks are not supported by 2BASE-TL.

Section B.5.3. “Span Powering” is out of scope.

The RL_{min} value of section B.5.2 is modified from 14 to 12 dB for the purpose of 2BASE-TL.

63.3.2.5.2 Additional requirement: wetting current

The 2BASE-TL-R shall be capable of sustaining 20 mA of wetting (sealing) current. The maximum rate of change of the wetting current shall be no more than 20 mA per second.

NOTE—The -R device cannot be guaranteed to operate correctly if more than 20 mA (tip to ring) is sourced.

63.3.2.6 Changes to Annex C, “Regional Requirements – Region 3”

Referenced as is, with the exception of optional support for asymmetric PSD masks. Asymmetric PSD masks are not supported by 2BASE-TL.

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63.4 Protocol implementation conformance statement (PICS) proforma for Clause 63, Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD), type 2BASE-TL[125]

63.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 63, Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD), type 2BASE-TL, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

63.4.2 Identification

63.4.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., names and versions for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

63.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 63, Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD), type 2BASE-TL.
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[125] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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63.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
2BPMA	SHDSL based PMA	63.2	The PMA based on the PMS-TC specified in ITU-T Recommendation G.991.2 is implemented.	M	Yes [ ]
2BPMD	SHDSL based PMD	63.3	The PMD based on the PMD specified in ITU-T Recommendation G.991.2 is implemented.	M	Yes [ ]

63.4.4 PICS proforma tables for the Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD) sublayers, type 2BASE-TL

63.4.4.1 SHDSL based PMA

Item	Feature	Subclause	Value/Comment	Status	Support
2BPMA-1	α(β)-interface	63.1.4.1	The PMA_receive_synchronized is asserted when LOSW is “0” and deasserted when LOSW is “1”	M	Yes [ ]
2BPMA-2	The I-data flow	63.1.4.2.1	If data streams are implemented serially, the LSB of each octet (i.e., b_8 of Figure 61–16) is sent first.	M	Yes [ ]
2BPMA-3	Operation Channel	63.1.4.3	The OC-TC function of the PMA receives the EOC and overhead indicators over the OC-TC interface.	M	Yes [ ]
2BPMA-4	Operation Channel	63.1.4.3	The EOC and overhead indicators are included in the overhead sections of the 2BASE-TL PMA frames.	M	Yes [ ]
2BPMA-5	General exceptions	63.2.1	The 2BASE-TL PMA is octet oriented.	M	Yes [ ]
2BPMA-6	General exceptions	63.2.1	The bit oriented parameter i defined for Equation (63–1) and Equation (63–3) is equal to 0 in all cases.	M	Yes [ ]
2BPMA-7	Specific requirements and exceptions	63.2.2	The 2BASE-TL PMA complies to the requirements of G.991.2 Section 7.	M	Yes [ ]
2BPMA-8	Specific requirements and exceptions	63.2.2	The 2BASE-TL PMA complies to the requirements of G.991.2 Section 9.	M	Yes [ ]
2BPMA-9	Reference 7.1	63.2.2.1	2BASE-TL operates in synchronous mode. Bits stb1 and stb2 are present in every frame, and stb3 and stb4 are not present.	M	Yes [ ]
2BPMA-10	Reference 7.1	63.2.2.1	Since different frame synchronization algorithms require different values for the bits of the FSW, a provision has been made to allow the receiver to inform the far end transmitter of the particular values that are to be used for this field according to 61.4.	M	Yes [ ]

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63.4.4.2 SHDSL based PMD

Item	Feature	Subclause	Value/Comment	Status	Support
2BPMD-1	General exceptions	63.3.1	The 2BASE-TL PMD is octet oriented.	M	Yes [ ]
2BPMD-2	General exceptions	63.3.1	The 2BASE-TL PMD supports the use of the 32-TCPAM constellation for specific rates.	M	Yes [ ]
2BPMD-4	General exceptions	63.3.1	The 2BASE-TL PMD supports the use of the enhanced SHDSL extended bandwidths.	M	Yes [ ]
2BPMD-5	General exceptions	63.3.1	The bit oriented parameter *i* defined for Equation (63–1) and Equation (63–3) is equal to 0 in all cases.	M	Yes [ ]
2BPMD-6	Specific requirements and exceptions	63.3.2	The 2BASE-TL PMD complies to the requirements of G.991.2 Section 5, Section 6, Section 10, Section 11, Section 12.	M	Yes [ ]
2BPMD-7	Specific requirements and exceptions	63.3.2	The 2BASE-TL PMD complies to at least one of the three regional annexes: Annex A, Annex B, or Annex C with the exception of performance, which is defined in Annex 63B.	M	Yes [ ]
2BPMD-8	Reference section 6	63.3.2.2	The 16 and 32 TC-PAM mappings are per Table 63–5.	M	Yes [ ]
2BPMD-9	Changes to Annex A/B	63.3.2.4.2 63.3.2.5.2	The DC resistance of the 2BASE-TL-R is 1000 ohms plus or minus 10%.	M	Yes [ ]
2BPMD-10	Changes to Annex A/B	63.3.2.4.2 63.3.2.5.2	The 2BASE-TL-R is capable of sustaining 20 mA of wetting (sealing) current.	M	Yes [ ]

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64. Multipoint MAC Control

64.1 Overview

This clause deals with the mechanism and control protocols required in order to reconcile the P2MP topology into the Ethernet framework. The P2MP medium is a passive optical network (PON), an optical network with no active elements in the signal's paths from source to destination. The only interior elements used in a PON are passive optical components, such as optical fiber, splices, and splitters. When combined with the Ethernet protocol, such a network is referred to as Ethernet passive optical network (EPON).

P2MP is an asymmetrical medium based on a tree (or tree-and-branch) topology. The DTE connected to the trunk of the tree is called optical line terminal (OLT) and the DTEs connected at the branches of the tree are called optical network units (ONU). The OLT typically resides at the service provider's facility, while the ONUs are located at the subscriber premises.

In the downstream direction (from the OLT to an ONU), signals transmitted by the OLT pass through a 1:N passive splitter (or cascade of splitters) and reach each ONU. In the upstream direction (from the ONUs to the OLT), the signal transmitted by an ONU would only reach the OLT, but not other ONUs. To avoid data collisions and increase the efficiency of the subscriber access network, ONU's transmissions are arbitrated. This arbitration is achieved by allocating a transmission window (grant) to each ONU. An ONU defers transmission until its grant arrives. When the grant arrives, the ONU transmits frames at wire speed during its assigned time slot.

A simplified P2MP topology example is depicted in Figure 64–1. Clause 67 provides additional examples of P2MP topologies.

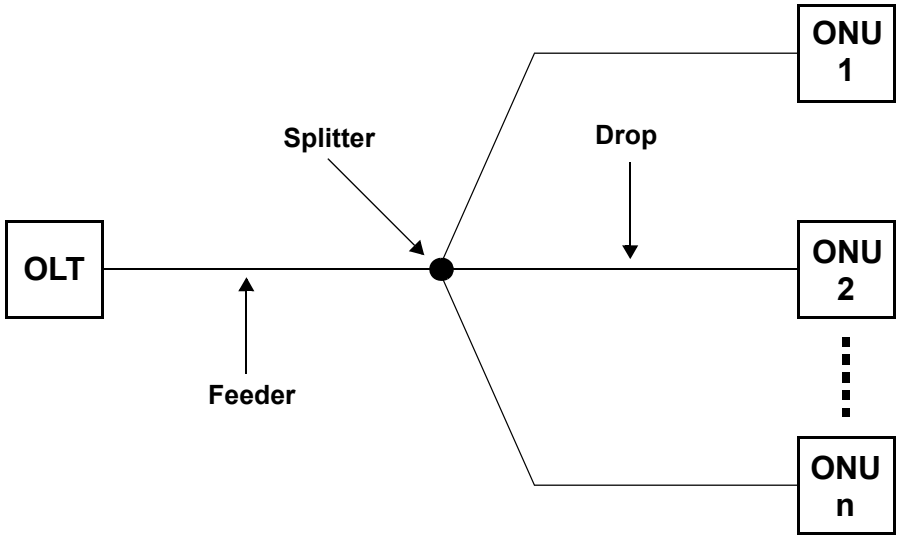

Figure 64–1—PON topology example

Topics dealt with in this clause include allocation of upstream transmission resources to different ONUs, discovery and registration of ONUs into the network, and reporting of congestion to higher layers to allow for dynamic bandwidth allocation schemes and statistical multiplexing across the PON.

This clause does not deal with topics including bandwidth allocation strategies, authentication of end-devices, quality-of-service definition, provisioning, or management.

This clause specifies the multipoint control protocol (MPCP) to operate an optical multipoint network by defining a Multipoint MAC Control sublayer as an extension of the MAC Control sublayer defined in Clause 31, and supporting current and future operations as defined in Clause 31 and annexes.

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Each PON consists of a node located at the root of the tree assuming the role of OLT, and multiple nodes located at the tree leaves assuming roles of ONUs. The network operates by allowing only a single ONU to transmit in the upstream direction at a time. The MPCP located at the OLT is responsible for timing the different transmissions. Reporting of congestion by the different ONUs may assist in optimally allocating the bandwidth across the PON.

Automatic discovery of end stations is performed, culminating in registration through binding of an ONU to an OLT port by allocation of a Logical Link ID (see LLID in 65.1.3.3.2), and dynamic binding to a MAC connected to the OLT.

The Multipoint MAC Control functionality shall be implemented for subscriber access devices containing point-to-multipoint Physical Layer devices defined in Clause 60.

64.1.1 Goals and objectives

The goals and objectives of this clause are the definition of a point-to-multipoint Ethernet network utilizing an optical medium.

Specific objectives met include the following:

a) Support of Point-to-Point Emulation (P2PE) as specified
b) Support multiple LLIDs and MAC Clients at the OLT
c) Support a single LLID per ONU
d) Support a mechanism for single copy broadcast
e) Flexible architecture allowing dynamic allocation of bandwidth
f) Use of 32 bit timestamp for timing distribution
g) MAC Control based architecture
h) Ranging of discovered devices for improved network performance
i) Continuous ranging for compensating round trip time variation

64.1.2 Position of Multipoint MAC Control within the IEEE 802.3 hierarchy

Multipoint MAC Control defines the MAC control operation for optical point-to-multipoint networks. Figure 64–2 depicts the architectural positioning of the Multipoint MAC Control sublayer with respect to the MAC and the MAC Control client. The Multipoint MAC Control sublayer takes the place of the MAC Control sublayer to extend it to support multiple clients and additional MAC control functionality.

Multipoint MAC Control is defined using the mechanisms and precedents of the MAC Control sublayer. The MAC Control sublayer has extensive functionality designed to manage the real-time control and manipulation of MAC sublayer operation. This clause specifies the extension of the MAC Control mechanism to manipulate multiple underlying MACs simultaneously. This clause also specifies a specific protocol implementation for MAC Control.

The Multipoint MAC Control sublayer is specified such that it can support new functions to be implemented and added to this standard in the future. MultiPoint Control Protocol (MPCP), the management protocol for P2MP is one of these protocols. Non-real-time, or quasi-static control (e.g., configuration of MAC operational parameters) is provided by Layer Management. Operation of the Multipoint MAC Control sublayer is transparent to the MAC.

As depicted in Figure 64–2, the layered system instantiates multiple MAC entities, using a single Physical Layer. The individual MAC instances offer a Point-to-point emulation service between the OLT and the ONU. An additional MAC is instantiated to communicate to all ONUs at once. This instance takes maximum advantage of the broadcast nature of the downstream channel by sending a single copy of a frame that is received by all ONUs. This MAC instance is referred to as single copy broadcast (SCB).

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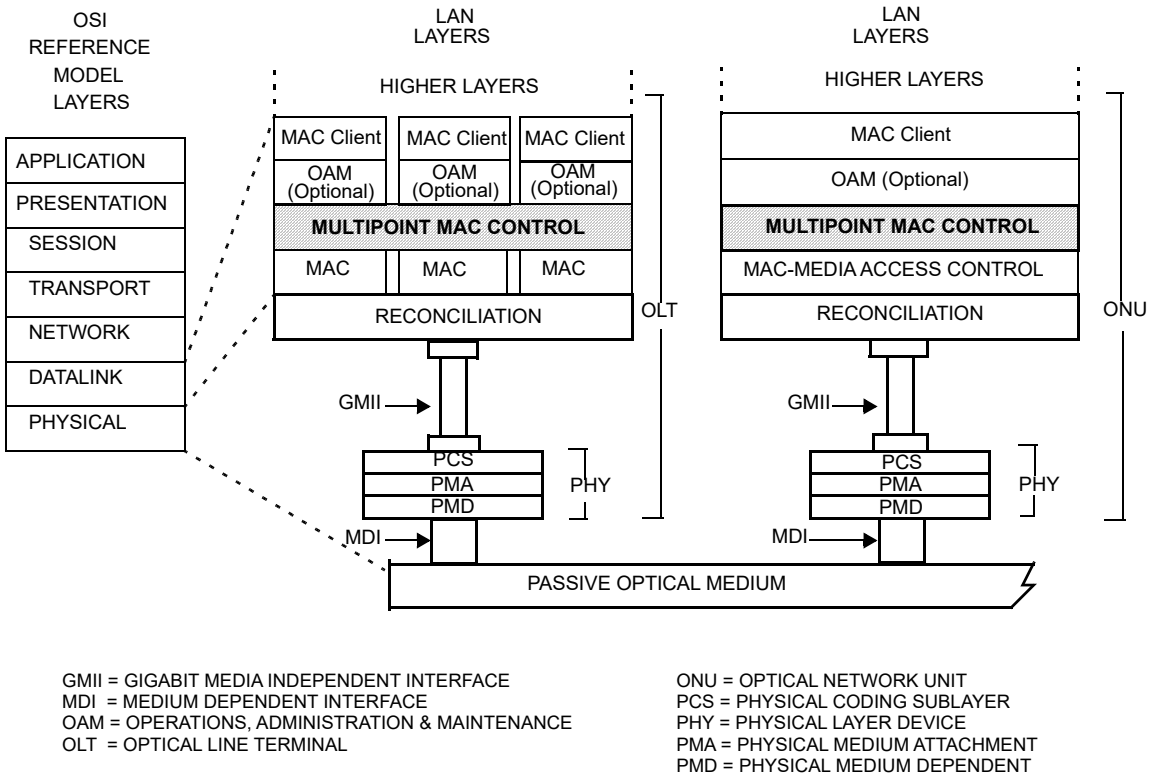
The ONU only requires one MAC instance since frame filtering operations are done at the RS layer before reaching the MAC. Therefore, MAC and layers above are emulation-agnostic at the ONU (see 65.1.3.3).

Although Figure 64–2 and supporting text describe multiple MACs within the OLT, a single unicast MAC address may be used by the OLT. Within the EPON Network, MACs are uniquely identified by their LLID which is dynamically assigned by the registration process.



GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 64–2—Relationship of Multipoint MAC Control and the OSI protocol stack

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64.1.3 Functional block diagram

Figure 64–3 provides a functional block diagram of the Multipoint MAC Control architecture.

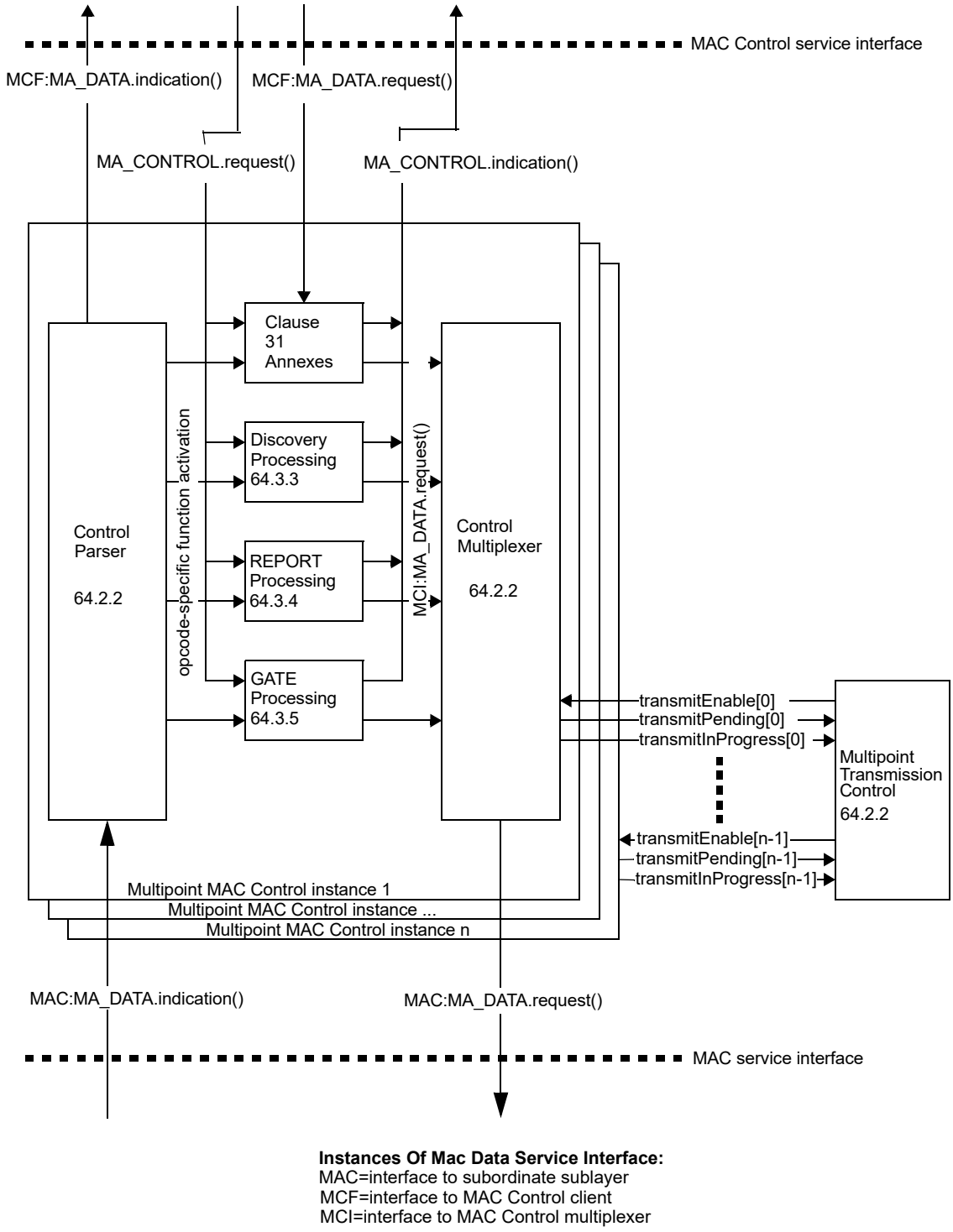

Figure 64–3—Multipoint MAC Control functional block diagram

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64.1.4 Service interfaces

The MAC Client communicates with the Control Multiplexer using the standard service interface specified in 2.3. Multipoint MAC Control communicates with the underlying MAC sublayer using the standard service interface specified in 4A.3.2. Similarly, Multipoint MAC Control communicates internally using primitives and interfaces consistent with definitions in Clause 31.

64.1.5 State diagram conventions

The body of this standard comprises state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2 augmented as follows:

a) [start x_timer, y] sets expiration of *y* to timer *x_timer*.
b) [stop x_timer] aborts the timer operation for *x_timer* asserting *x_timer_not_done* indefinitely.

The state diagrams use an abbreviation MACR as a shorthand form for MA_CONTROL.request and MACI as a shorthand form for MA_CONTROL.indication.

The vector notations used in the state diagrams for bit vector use 0 to mark the first received bit and so on (for example data[0:15]), following the conventions of 3.1 for bit ordering. When referring to an octet vector, 0 is used to mark the first received octet and so on (for example m_sdu[0..1]).

a < *b:* A function that is used to compare two (cyclic) time values. Returned value is true when *b* is larger than *a* allowing for wrap around of *a* and *b*. The comparison is made by subtracting *b* from *a* and testing the MSB. When MSB(*a*-*b*) = 1 the value true is returned, else false is returned. In addition, the following functions are defined in terms of *a* < *b*:
a > *b* is equivalent to !(*a* < *b* or *a* = *b*)
a ≥ *b* is equivalent to !(*a* < *b*)
a ≤ *b* is equivalent to !(*a* > *b*)

64.2 Multipoint MAC Control operation

As depicted in Figure 64–3, the Multipoint MAC Control functional block comprises the following functions:

a) *Multipoint Transmission Control*. This block is responsible for synchronizing Multipoint MAC Control instances associated with the Multipoint MAC Control. This block maintains the Multipoint MAC Control state and controls the multiplexing functions of the instantiated MACs.
b) *Multipoint MAC Control Instance n*. This block is instantiated for each MAC and respective MAC and MAC Control clients associated with the Multipoint MAC Control. It holds all the variables and state associated with operating all MAC Control protocols for the instance.
c) *Control Parser*. This block is responsible for parsing MAC Control frames, and interfacing with Clause 31 entities, the opcode specific blocks, and the MAC Client.
d) *Control Multiplexer*. This block is responsible for selecting the source of the forwarded frames.
e) *Clause 31 Annexes*. This block holds MAC Control actions as defined in Clause 31 annexes for support of legacy and future services.
f) *Discovery, Report and Gate Processing*. These blocks are responsible for handling the MPCP in the context of the MAC.

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64.2.1 Principles of Multipoint MAC Control

As depicted in Figure 64–3, Multipoint MAC Control sublayer may instantiate multiple Multipoint MAC Control instances in order to interface multiple MAC and MAC Control clients above with multiple MACs below. A unique unicast MAC instance is used at the OLT to communicate with each ONU. The individual MAC instances utilize the point-to-point emulation service between the OLT and the ONU as defined in 65.1.

At the ONU, a single MAC instance is used to communicate with a MAC instance at the OLT. In that case, the Multipoint MAC Control contains only a single instance of the Control Parser/Multiplexer function.

Multipoint MAC Control protocol supports several MAC and client interfaces. Only a single MAC interface and Client interface is enabled for transmission at a time. There is a tight mapping between a MAC service interface and a Client service interface. In particular, the assertion of the MAC:MA_DATA.indication primitive in MAC *j* leads to the assertion of the MCF:MA_DATA.indication primitive to Client *j*. Conversely, the assertion of the request service interface in Client *i* leads to the assertion of the MAC:MA_DATA.request primitive of MAC *i*. Note that the Multipoint MAC sublayer need not receive and transmit packets associated with the same interface at the same time. Thus the Multipoint MAC Control acts like multiple MAC Controls bound together with common elements.

The scheduling algorithm is implementation dependent, and is not specified for the case where multiple transmit requests happen at the same time.

The reception operation is as follows. The Multipoint MAC Control instances generate MAC:MA_DATA.indication service primitives continuously to the underlying MAC instances. Since these MACs are receiving frames from a single PHY only one frame is passed from the MAC instances to Multipoint MAC Control. The MAC instance responding to the MAC:MA_DATA.indication is referred to as the enabled MAC, and its service interface is referred to as the enabled MAC interface. The MAC passes to the Multipoint MAC Control sublayer all valid frames. Invalid frames, as specified in 3.4, are not passed to the Multipoint MAC Control sublayer in response to a MAC:MA_DATA.indication service primitive.

The enabling of a transmit service interface is performed by the Multipoint MAC Control instance in collaboration with the Multipoint Transmission Control. Frames generated in the MAC Control are given priority over MAC Client frames, in effect, prioritizing the MA_CONTROL primitive over the MCF:MA_DATA primitive, and for this purpose MCF:MA_DATA.request primitives may be delayed, discarded or modified in order to perform the requested MAC Control function. For the transmission of this frame, the Multipoint MAC Control instance enables forwarding by the MAC Control functions, but the MAC Client interface is not enabled. The reception of a frame in a MAC results in generation of the MAC:MA_DATA.indication primitive on that MAC's interface. Only one receive MAC interface will be enabled at any given time since there is only one PHY interface.

The information of the enabled interfaces is stored in the controller state variables, and accessed by the Multiplexing Control block.

The Multipoint MAC Control sublayer uses the services of the underlying MAC sublayer to exchange both data and control frames.

Receive operation (MAC:MA_DATA.indication) at each instance:

a) A frame is received from the underlying MAC.
b) The frame is parsed according to Length/Type field
c) MAC Control frames are demultiplexed according to opcode and forwarded to the relevant processing functions
d) Data frames (see 31.5.1) are forwarded to the MAC Client by asserting MCF:MA_DATA.indication primitives

Transmit operation (MAC:MA_DATA.request) at each instance:

e) The MAC Client signals a frame transmission by asserting MCF:MA_DATA.request, or

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f) A protocol processing block attempts to issue a frame, as a result of a previous MA_CONTROL.request or as a result of an MPCP event that generates a frame.
g) When allowed to transmit by the Multipoint Transmission Control block, the frame is forwarded.

64.2.1.1 Ranging and Timing Process

Both the OLT and the ONU have 32-bit counters that increment every 16 ns. These counters provide a local time stamp. When either device transmits an MPCPDU, it maps its counter value into the timestamp field. The time of transmission of the first octet of the MPCPDU frame from the MAC Control to the MAC is taken as the reference time used for setting the timestamp value.

When the ONU receives MPCPDUs, it sets its counter according to the value in the timestamp field in the received MPCPDU.

When the OLT receives MPCPDUs, it uses the received timestamp value to calculate or verify a round trip time between the OLT and the ONU. The RTT is equal to the difference between the timer value and the value in the timestamp field. The calculated RTT is notified to the client via the MA_CONTROL.indication primitive. The client can use this RTT for the ranging process.

A condition of *timestamp drift error* occurs when the difference between OLT's and ONU's clocks exceeds some predefined threshold. This condition can be independently detected by the OLT or an ONU. The OLT detects this condition when an absolute difference between new and old RTT values measured for a given ONU exceeds the value of guardThresholdOLT (see 64.2.2.1), as shown in Figure 64–10. An ONU detects the timestamp drift error condition when absolute difference between a timestamp received in an MPCPDU and the localTime counter exceeds guardThresholdONU (see 64.2.2.1), as is shown in Figure 64–11.

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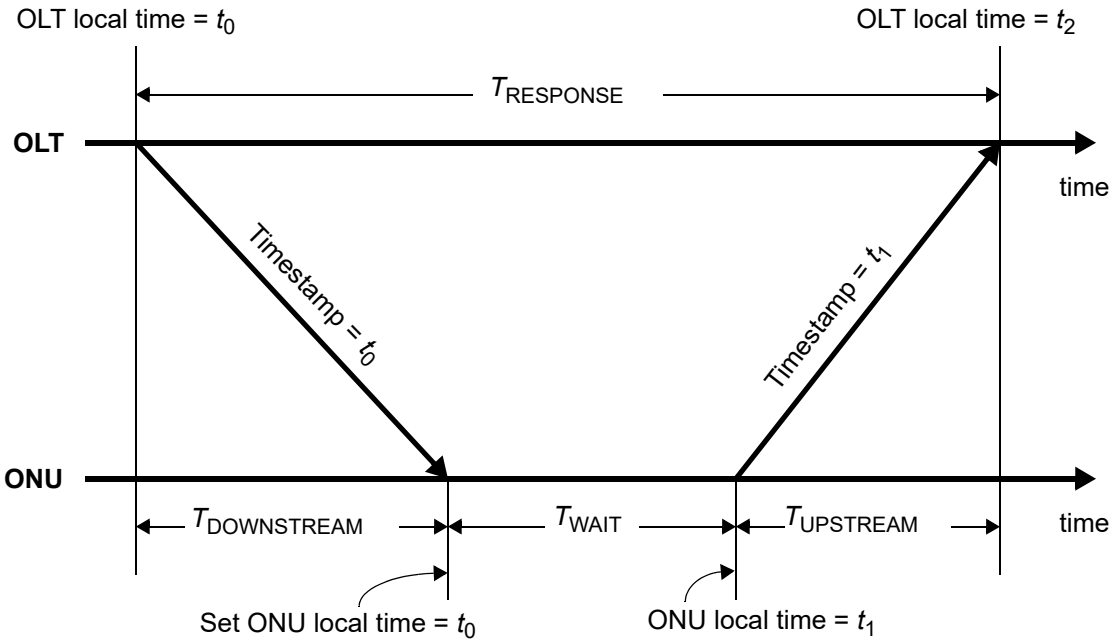

$T_{DOWNSTREAM}$ = downstream propagation delay

$T_{UPSTREAM}$ = upstream propagation delay

T_{WAIT} = wait time at ONU = t_1 - t_0

$T_{RESPONSE}$ = response time at OLT = t_2 - t_0

$$RTT = T_{DOWNSTREAM} + T_{UPSTREAM} = T_{RESPONSE} - T_{WAIT} = (t_2 - t_0) - (t_1 - t_0) = t_2 - t_1$$

Figure 64–4—Round trip time calculation

64.2.2 Multipoint transmission control, Control Parser, and Control Multiplexer

The purpose of the multipoint transmission control is to allow only one of the multiple MAC clients to transmit to its associated MAC and subsequently to the RS layer at one time by only asserting one transmitEnable signal at a time.

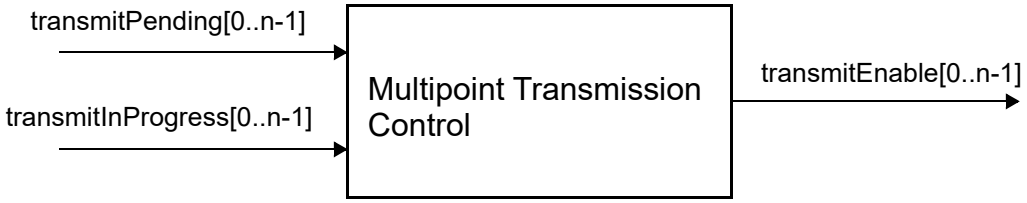

Figure 64–5—Multipoint Transmission Control Service Interfaces

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Multipoint MAC Control Instance n function block communicates with the Multipoint Transmission Control using transmitEnable[n], transmitPending[n], and transmitInProgress[n] state variables (see Figure 64–3).

The Control Parser is responsible for opcode independent parsing of MAC frames in the reception path. By identifying MAC Control frames, demultiplexing into multiple entities for event handling is possible. Interfaces are provided to existing Clause 31 entities, functional blocks associated with MPCP, and the MAC Client.

The Control Multiplexer is responsible for forwarding frames from the MAC Control opcode-specific functions and the MAC Client to the MAC. Multiplexing is performed in the transmission direction. Given multiple MCF:MA_DATA.request service primitives from the MAC Client, and MA_CONTROL.request primitives from the MAC Control Clients, a single MAC:MA_DATA.request service primitive is generated for transmission. At the OLT, multiple MAC instances share the same Multipoint MAC Control, as a result, the transmit block is enabled based on an external control signal housed in Multipoint Transmission Control for transmission overlap avoidance. At the ONU the Gate Processing functional block interfaces for upstream transmission administration.

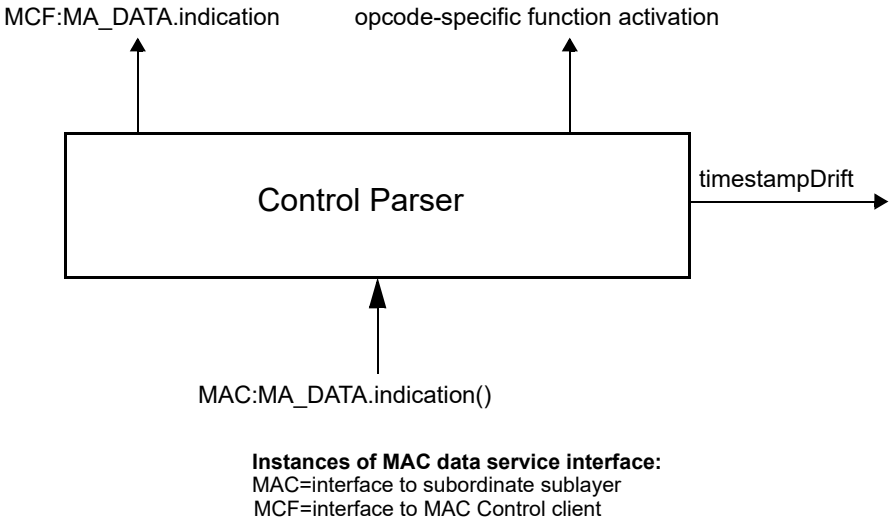

Figure 64–6—Control Parser service interfaces

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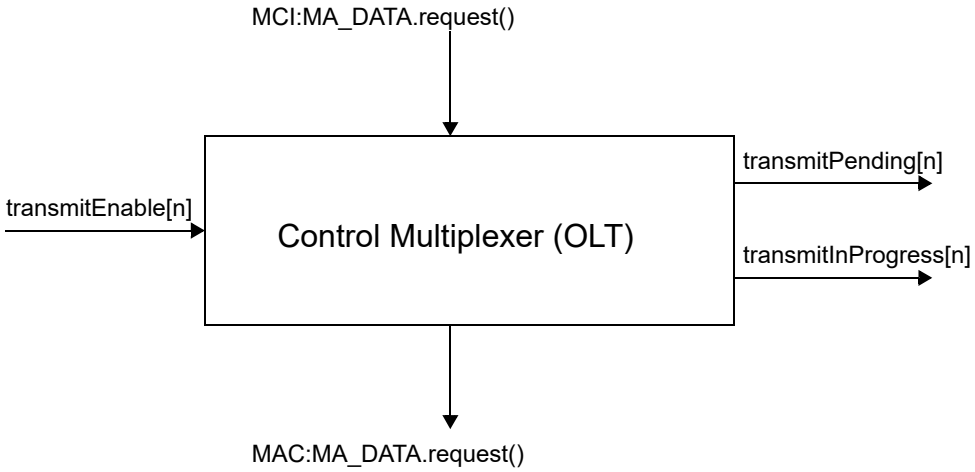
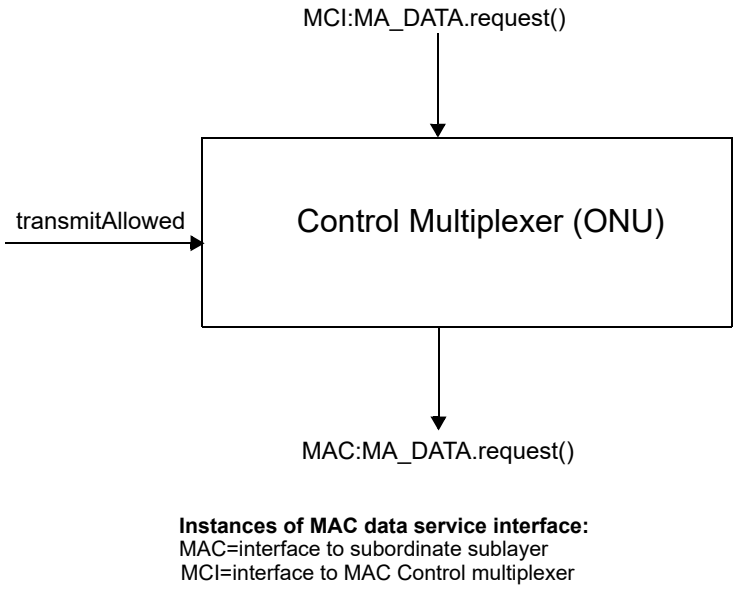


NOTE—MAC:MA_DATA.request primitive may be issued from multiple MAC Control processing blocks.

Figure 64–7—OLT Control Multiplexer service interfaces



NOTE—MAC:MA_DATA.request primitive may be issued from multiple MAC Control processing blocks.

Figure 64–8—ONU Control Multiplexer service interfaces

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64.2.2.1 Constants

defaultOverhead

This constant holds the size of packet transmission overhead. This overhead is measured in units of time quanta.

TYPE: integer
VALUE: 6

guardThresholdOLT

This constant holds the maximal amount of drift allowed for a timestamp received at the OLT. This value is measured in units of time_quantum (16 bit times).

TYPE: integer
VALUE: 12

guardThresholdONU

This constant holds the maximal amount of drift allowed for a timestamp received at the ONU. This value is measured in units of time_quantum (16 bit times)

TYPE: integer
VALUE: 8

MAC_Control_type

The value of the Length/Type field as defined in 31.4.1.3.

TYPE: integer
VALUE: 0x8808

tailGuard

This constant holds the value used to reserve space at the end of the upstream transmission at the ONU in addition to the size of last MAC service data unit (m_sdu) in units of octets. Space is allocated for the MAC overheads including: preamble, SFD, DA, SA, Length/Type, FCS, and the End of Packet Delimiter (EPD). The sizes of the above listed MAC overhead items are described in 3.1.1. The size of the EPD is described in 36.2.4.14.

TYPE: integer
VALUE: 29

time_quantum

The unit of time_quantum is used by all mechanisms synchronized to the advancement of the localTime variable. All variables that represent counters and time intervals are defined using time_quantum. Each time_quantum is 16 ns.

TYPE: integer
VALUE: 16

tqSize

This constant represents time_quantum in octet transmission times.

TYPE: integer
VALUE: 2

64.2.2.2 Counters

localTime

This variable holds the value of the local timer used to control MPCP operation. This variable is advanced by a timer at 62.5 MHz, and counts in time_quanta. At the OLT the counter shall track the transmit clock, while at the ONU the counter shall track the receive clock. For accuracy of receive clock, see 65.3.1.2. It is reloaded with the received timestamp value (from the OLT) by the Control Parser (see Figure 64–11). Changing the value of this variable while running using Layer Management is highly undesirable and is unspecified.

TYPE: 32 bit unsigned

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64.2.2.3 Variables

BEGIN

This variable is used when initiating operation of the functional block state diagram. It is set to true following initialization and every reset.

TYPE: Boolean

data_rx

This variable represents a 0-based bit array corresponding to the payload of a received MPCPDU. This variable is used to parse incoming MPCPDU frames.

TYPE: bit array

data_tx

This variable represents a 0-based bit array corresponding to the payload of an MPCPDU being transmitted. This variable is used to access payload of outgoing MPCPDU frames, for example to set the timestamp value.

TYPE: bit array

fecEnabled

This variable represents whether the FEC function is enabled. If FEC function is enabled, this variable equals true, otherwise it equals false.

TYPE: Boolean

flags_rx

This variable holds the value of the Flags field from the last received MPCPDU.

TYPE: 8-bit unsigned

newRTT

This variable temporary holds a newly-measured Round Trip Time to the ONU. The new RTT value is represented in units of time_quanta.

TYPE:16 bit unsigned

nextTxTime

This variable represents a total transmission time of next packet and is used to check whether the next packet fits in the remainder of ONU's transmission window. The value of nextTxTime includes packet transmission time, tailGuard defined in 64.2.2.1, and FEC parity data overhead, if FEC is enabled. This variable is measured in units of time quanta.

TYPE: 16 bit unsigned

opcode_rx

This variable holds an opcode of the last received MPCPDU.

TYPE: 16 bit unsigned

opcode_tx

This variable holds an opcode of an outgoing MPCPDU.

TYPE: 16 bit unsigned

RTT

This variable holds the measured Round Trip Time to the ONU. The RTT value is represented in units of time_quanta.

TYPE: 16 bit unsigned

stopTime

This variable holds the value of the localTime counter corresponding to the end of the nearest grant. This value is set by the Gate Processing function as described in 64.3.5.

TYPE: 32 bit unsigned

timestamp

This variable holds the value of timestamp of the last received MPCPDU frame.

TYPE: 32 bit unsigned

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timestampDrift

This variable is used to indicate whether an error is signaled as a result of uncorrectable timestamp drift.

TYPE: Boolean

transmitAllowed

This variable is used to control PDU transmission at the ONU. It is set to true when the transmit path is enabled, and is set to false when the transmit path is being shut down. transmitAllowed changes its value according to the state of the Gate Processing functional block.

TYPE: Boolean

transmitEnable[j]

These variables are used to control the transmit path in a Multipoint MAC Control instance at the OLT. Setting them to on indicates that the selected instance is permitted to transmit a frame. Setting it to off inhibits the transmission of frames in the selected instance. Only one of transmitEnable[j] should be set to on at a time.

TYPE: Boolean

transmitInProgress[j]

This variable indicates that the Multipoint MAC Control instance *j* is in a process of transmitting a frame.

TYPE: Boolean

transmitPending[j]

This variable indicates that the Multipoint MAC Control instance *j* is ready to transmit a frame.

TYPE: Boolean

64.2.2.4 Functions

abs(n)

This function returns the absolute value of the parameter n.

Opcode-specific function(opcode)

Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

FEC_Overhead(length)

This function calculates the size of additional overhead to be added by the FEC encoder while encoding a frame of size length. Parameter length represents the size of an entire frame including preamble, SFD, DA, SA, Length/Type, and FCS. As specified in 65.2.3, FEC encoder adds 16 parity octets for each block of 239 data octets. Additionally, 26 code-groups are required to accommodate IPG and longer start-of-frame and end-of-frame sequences, which are used to allow reliable packet boundary detection in presence of high bit error ratio. The function returns the value of FEC overhead in units of time quanta. The following formula is used to calculate the overhead:

$$FEC\_Overhead = 13 + \left\lceil \frac{length}{239} \right\rceil \times 8$$

NOTE—The notation $\lceil x \rceil$ represents a *ceiling* function, which returns the value of its argument *x* rounded up to the nearest integer.

select

This function selects the next Multipoint MAC Control instance allowed to initiate transmission of a frame. The function returns an index to the transmitPending array for which the value is not false. The selection criteria in the presence of multiple active elements in the list is implementation dependent.

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SelectFrame()

This function enables the interface, which has a pending frame. If multiple interfaces have frames waiting at the same time, only one interface will be enabled. The selection criteria is not specified, except for the case when some of the pending frames have Length/Type = MAC_Control. In this case, one of the interfaces with a pending MAC Control frame shall be enabled.

sizeof(sdu)

This function returns the size of the sdu in octets.

transmissionPending()

This function returns true if any of the Multipoint MAC Control instances has a frame waiting to be transmitted. The function can be represented as

transmissionPending() = transmitPending[0] +
transmitPending[1] +
... +
transmitPending[n-1]

where n is the total number of Multipoint MAC Control instances.

64.2.2.5 Timers

packet_initiate_timer

This timer is used to delay frame transmission from MAC Control to avoid variable MAC delay while MAC enforces IPG after a previous frame. In addition, when FEC is enabled, this timer increases interframe spacing just enough to accommodate the extra parity data to be added by the FEC encoder.

64.2.2.6 Messages

MAC:MA_DATA.indication(DA, SA, m_sdu, receiveStatus)

The service primitive is defined in 31.3.

MCF:MA_DATA.indication(DA, SA, m_sdu, receiveStatus)

The service primitive is defined in 31.3.

MAC:MA_DATA.request (DA, SA, m_sdu)

The service primitive is defined in 31.3. The action invoked by this service primitive is not considered to end until the transmission of the frame by the MAC has concluded. The ability of the MAC control layer to determine this is implementation dependent.

MCF:MA_DATA.request (DA, SA, m_sdu)

The service primitive is defined in 31.3.

64.2.2.7 State diagrams

The Multipoint transmission control function in the OLT shall implement state diagram shown in Figure 64–9. Control parser function in the OLT shall implement state diagram shown in Figure 64–10. Control parser function in the ONU shall implement state diagram shown in Figure 64–11. Control multiplexer function in the OLT shall implement state diagram shown in Figure 64–12. Control multiplexer function in the ONU shall implement state diagram shown in Figure 64–13.

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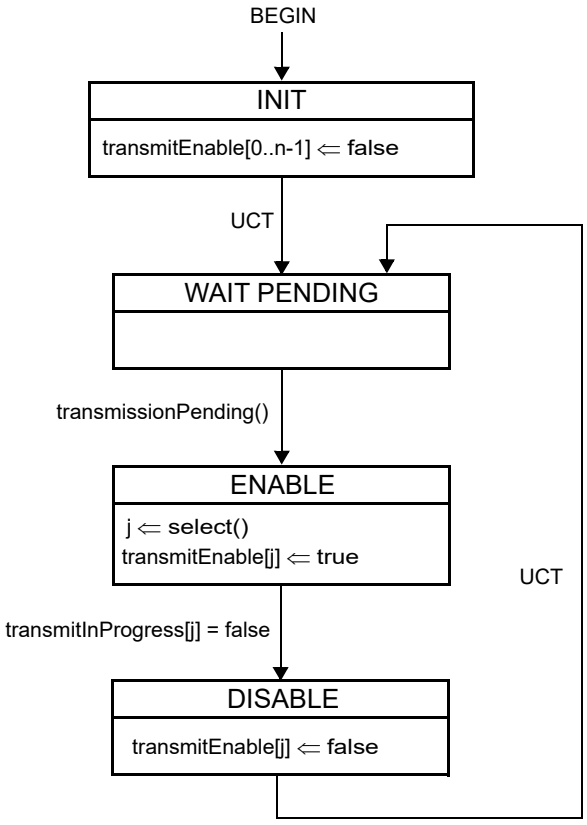

Figure 64–9—OLT Multipoint Transmission Control state diagram

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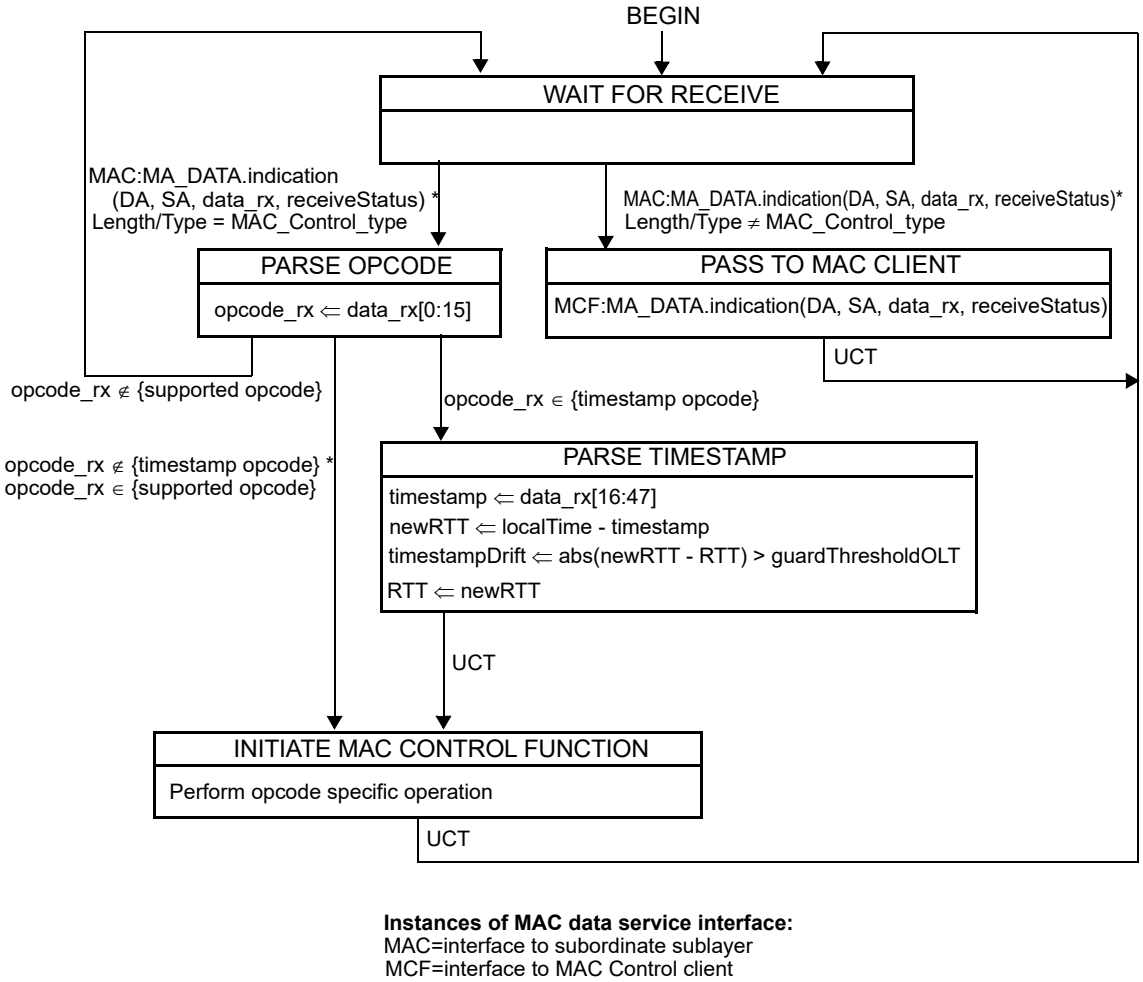

Instances of MAC data service interface:
MAC=interface to subordinate sublayer
MCF=interface to MAC Control client

NOTE—The opcode-specific operation is launched as a parallel process by the MAC Control sublayer, and not as a synchronous function. Progress of the generic MAC Control Receive state diagram (as shown in this figure) is not implicitly impeded by the launching of the opcode specific function.

Refer to Annex 31A for list of supported opcodes and timestamp opcodes.

Figure 64–10—OLT Control Parser state diagram

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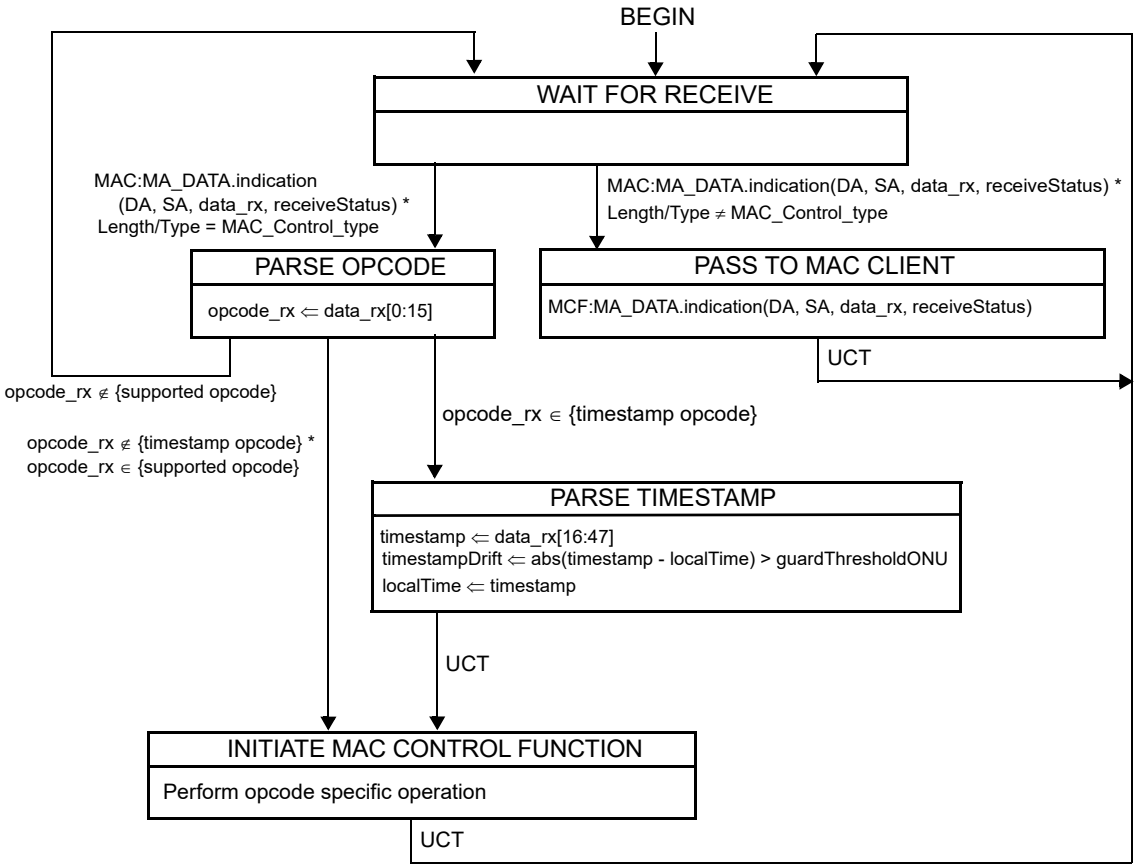

NOTE—The opcode-specific operation is launched as a parallel process by the MAC Control sublayer, and not as a synchronous function. Progress of the generic MAC Control Receive state diagram (as shown in this figure) is not implicitly impeded by the launching of the opcode specific function.

Refer to Annex 31A for list of supported opcodes and timestamp opcodes.

Figure 64–11—ONU Control Parser state diagram

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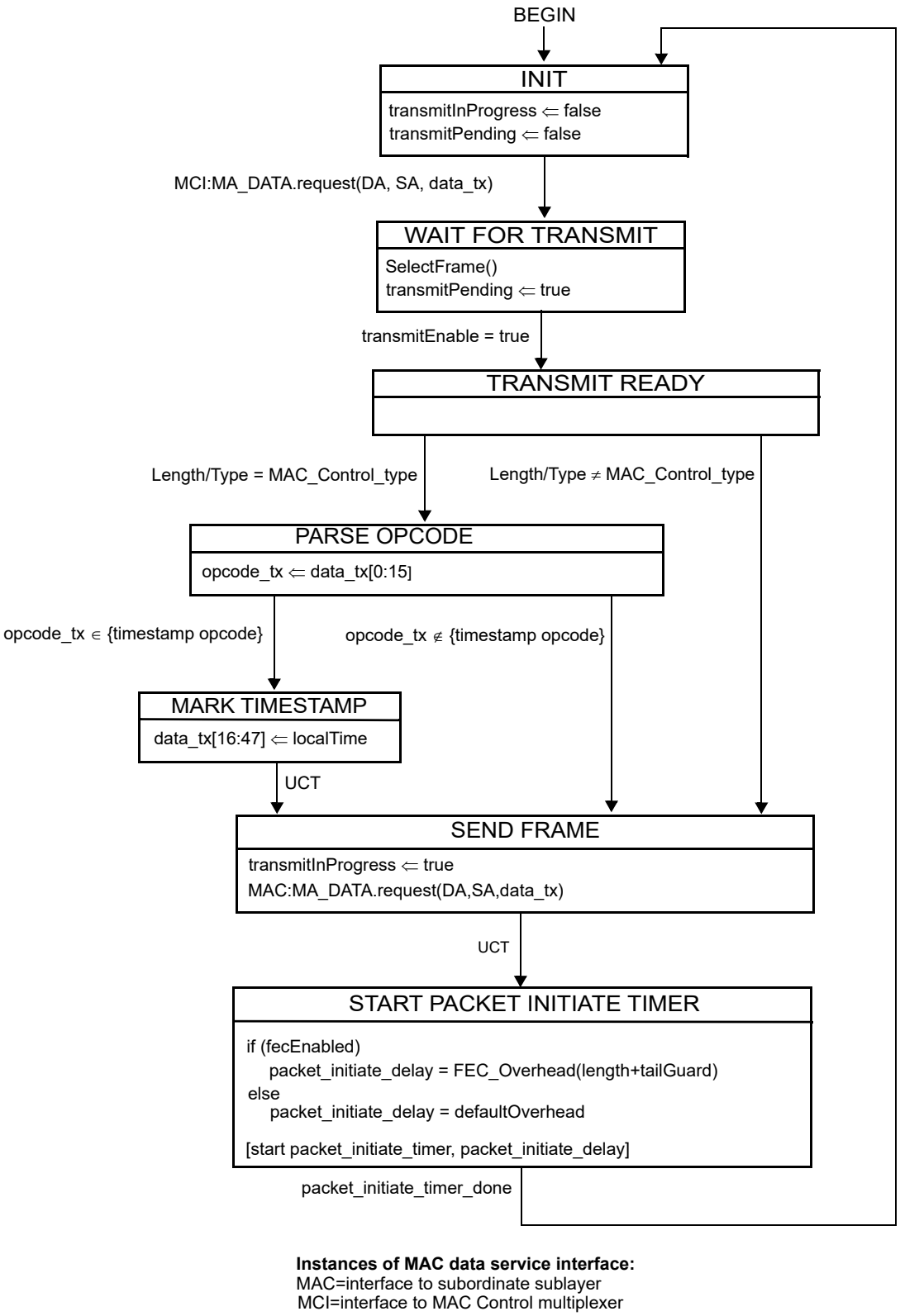

Figure 64–12—OLT Control Multiplexer state diagram

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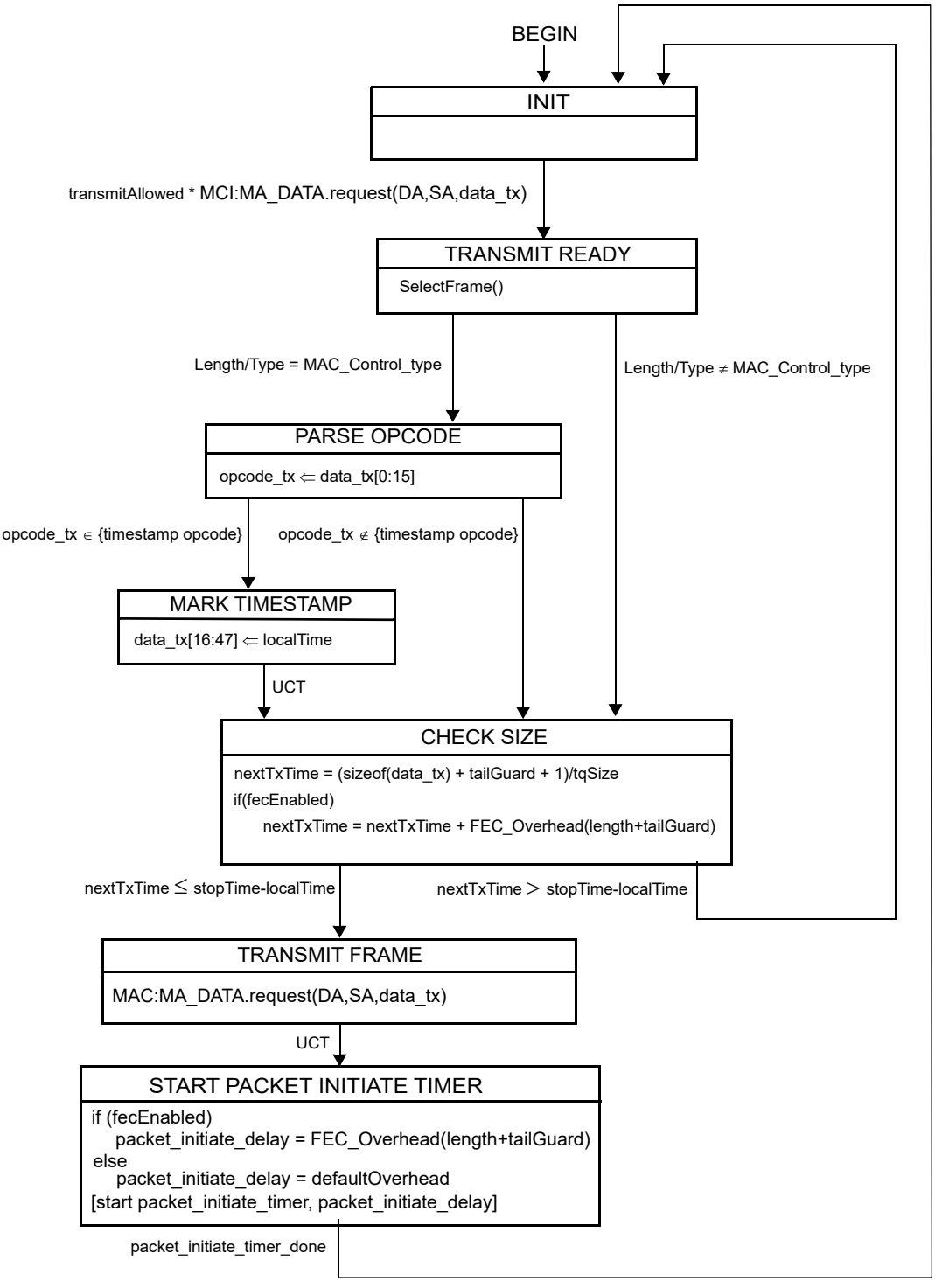

Figure 64–13—ONU Control Multiplexer state diagram

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64.3 Multipoint Control Protocol (MPCP)

As depicted in Figure 64–3, the Multipoint MAC Control functional block comprises the following functions:

a) *Discovery Processing*. This block manages the discovery process, through which an ONU is discovered and registered with the network while compensating for RTT.
b) *Report Processing*. This block manages the generation and collection of report messages, through which bandwidth requirements are sent upstream from the ONU to the OLT.
c) *Gate Processing*. This block manages the generation and collection of gate messages, through which multiplexing of multiple transmitters is achieved.

As depicted in Figure 64–3, the layered system may instantiate multiple MAC entities, using a single Physical Layer. Each instantiated MAC communicates with an instance of the opcode specific functional blocks through the Multipoint MAC Control. In addition some global variables are shared across the multiple instances. Common state control is used to synchronize the multiple MACs using MPCP procedures. Operation of the common state control is generally considered outside the scope of this document.

64.3.1 Principles of Multipoint Control Protocol

Multipoint MAC Control enables a MAC Client to participate in a point-to-multipoint optical network by allowing it to transmit and receive frames as if it was connected to a dedicated link. In doing so, it employs the following principles and concepts:

a) A MAC client transmits and receives frames through the Multipoint MAC Control sublayer.
b) The Multipoint MAC Control decides when to allow a frame to be transmitted using the client interface Control Multiplexer.
c) Given a transmission opportunity, the MAC Control may generate control frames that would be transmitted in advance of the MAC Client's frames, utilizing the inherent ability to provide higher priority transmission of MAC Control frames over MAC Client frames.
d) Multiple MACs operate on a shared medium by allowing only a single MAC to transmit upstream at any given time across the network using a time-division multiple access (TDMA) method.
e) Such gating of transmission is orchestrated through the Gate Processing function.
f) New devices are discovered in the network and allowed transmission through the Discovery Processing function.
g) Fine control of the network bandwidth distribution can be achieved using feedback mechanisms supported in the Report Processing function.
h) The operation of P2MP network is asymmetrical, with the OLT assuming the role of master, and the ONU assuming the role of slave.

64.3.2 Compatibility considerations

64.3.2.1 PAUSE operation

Even though MPCP is compatible with flow control, optional use of flow control may not be efficient in the case of large propagation delay. If flow control is implemented, then the timing constraints in Annex 31B supplement the constraints found at 64.3.2.4.

NOTE—MAC at an ONU can receive frames from unicast channel and SCB channel. If the SCB channel is used to broadcast data frames to multiple ONUs, the ONU's MAC may continue receiving data frames from SCB channel even after the ONU has issued a PAUSE request to its unicast remote-end.

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64.3.2.2 Optional Shared LAN Emulation

By combining P2PE, suitable filtering rules at the ONU, and suitable filtering and forwarding rules at the OLT, it is possible to emulate an efficient shared LAN. Support for shared LAN emulation is optional, and requires an additional layer above the MAC, which is out of scope for this document. Thus, shared LAN emulation is introduced here for informational purposes only.

Specific behavior of the filtering layer at the RS is specified in 65.1.3.3.2.

64.3.2.3 Multicast and single copy broadcast support

In the downstream direction, the PON is a broadcast medium. In order to make use of this capability for forwarding broadcast frames from the OLT to multiple recipients without multiple duplication for each ONU, the SCB and multicast LLID support is introduced.

The OLT has at least one MAC associated with every ONU. In addition one more MAC at the OLT is marked as the SCB MAC. Moreover, the OLT has a multicast MAC associated with each defined multicast LLID. The SCB MAC handles all downstream broadcast traffic, but is never used in the upstream direction for client traffic, except for client registration. Similarly, the multicast MACs handle downstream multicast traffic, but are never used in the upstream direction for client traffic. Optional higher layers may be implemented to perform selective broadcast and multicast of frames. Such layers may require additional MACs (multicast MACs) to be instantiated in the OLT for some or all ONUs increasing the total number of MACs beyond the number of ONUs + 1.

When connecting the SCB MAC or a multicast MAC to an IEEE 802.1Q bridge port it is possible that loops may be formed due to the broadcast or multicast nature of the associated LLIDs. Thus it is recommended that this MAC not be connected to an IEEE 802.1Q bridge port.

SCB channel configuration as well as filtering and marking of frames for support of SCB is defined in 65.1.3.3.2.

64.3.2.4 Delay requirements

The MPCP protocol relies on strict timing based on distribution of timestamps. A compliant implementation needs to guarantee a constant delay through the MAC and PHY in order to maintain the correctness of the timestamping mechanism. The actual delay is implementation dependent, however, a complying implementation shall maintain a delay variation of no more than 16 bit times through the implemented MAC stack.

The OLT shall not grant less than 1024 time_quanta into the future, in order to allow the ONU processing time when it receives a gate message. The ONU shall process all messages in less than this period. The OLT shall not issue more than one message every 1024 time_quanta to a single ONU. The unit of time_quantum is defined as 16 ns.

64.3.3 Discovery Processing

Discovery is the process whereby newly connected or off-line ONUs are provided access to the PON. The process is driven by the OLT, which periodically makes available Discovery Time Windows during which off-line ONUs are given the opportunity to make themselves known to the OLT. The periodicity of these windows is unspecified and left up to the implementer. The OLT signifies that a discovery period is occurring by broadcasting a discovery gate message, which includes the starting time and length of the discovery window. Off-line ONUs, upon receiving this message, wait for the period to begin and then transmit a REGISTER_REQ message to the OLT. Discovery windows are unique in that they are the only times where multiple ONUs can access the PON simultaneously, and transmission overlap can occur. In

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order to reduce transmission overlaps, a contention algorithm is used by all ONUs. Measures are taken to reduce the probability for overlaps by artificially simulating a random distribution of distances from the OLT. Each ONU shall wait a random amount of time before transmitting the REGISTER_REQ message that is shorter than the length of the discovery time window. It should be noted that multiple valid REGISTER_REQ messages can be received by the OLT during a single discovery time period. Included in the REGISTER_REQ message is the ONU's MAC address and number of maximum pending grants. Upon receipt of a valid REGISTER_REQ message, the OLT registers the ONU, allocating and assigning new port identities (LLIDs), and bonding corresponding MACs to the LLIDs.

The next step in the process is for the OLT to transmit a Register message to the newly discovered ONU, which contains the ONU's LLID, and the OLT's required synchronization time. Also, the OLT echoes the maximum number of pending grants. The OLT now has enough information to schedule the ONU for access to the PON and transmits a standard GATE message allowing the ONU to transmit a REGISTER_ACK. Upon receipt of the REGISTER_ACK, the discovery process for that ONU is complete, the ONU is registered and normal message traffic can begin. It is the responsibility of Layer Management to perform the MAC bonding, and start transmission from/to the newly registered ONU. The discovery message exchange is illustrated in Figure 64–14.

There may exist situations when the OLT requires that an ONU go through the discovery sequence again and reregister. Similarly, there may be situations where an ONU needs to inform the OLT of its desire to deregister. The ONU can then reregister by going through the discovery sequence. For the OLT, the REGISTER message may indicate a value, Reregister or Deregister, that if either is specified will force the receiving ONU into reregistering. For the ONU, the REGISTER_REQ message contains the Deregister bit that signifies to the OLT that this ONU should be deregistered.

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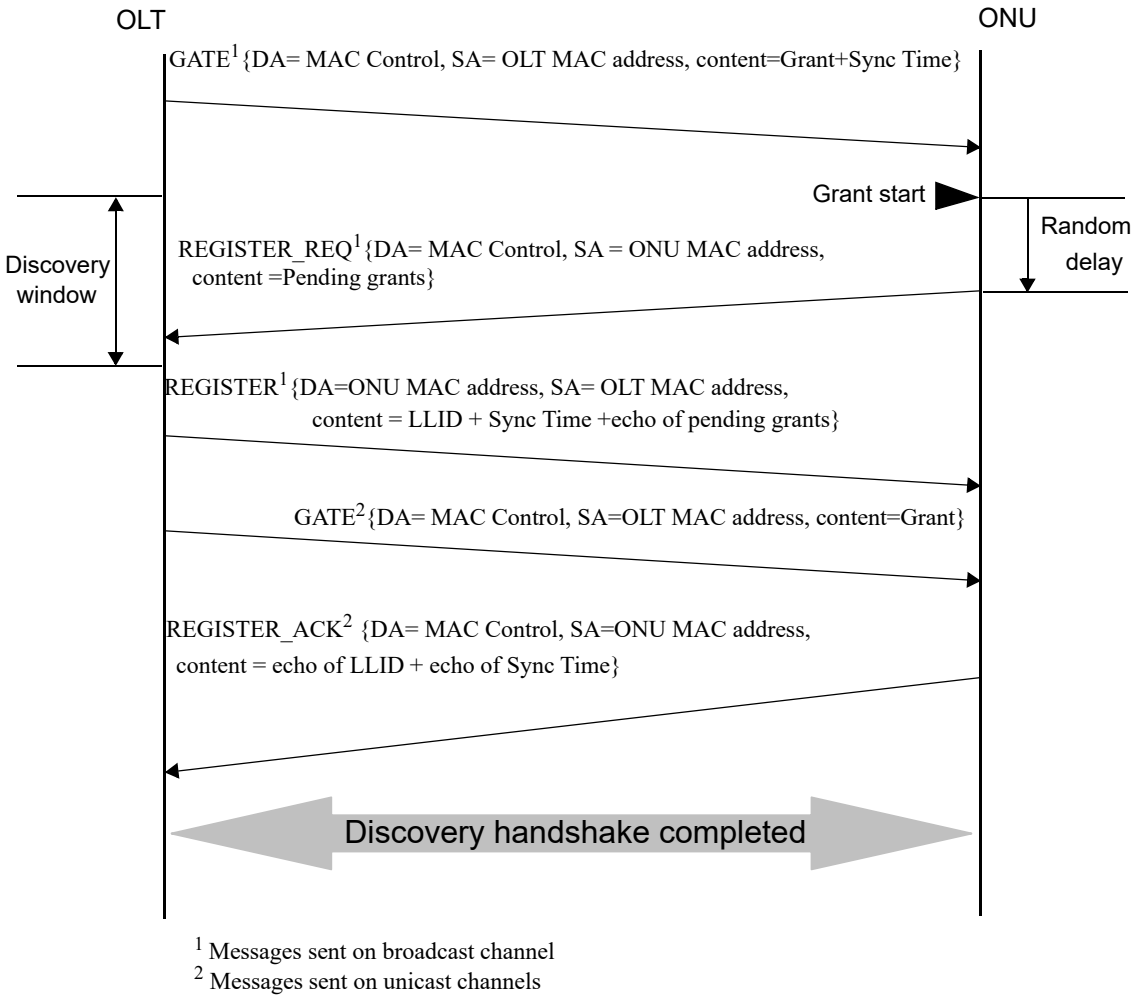

[1] Messages sent on broadcast channel
[2] Messages sent on unicast channels

Figure 64–14—Discovery Handshake Message Exchange

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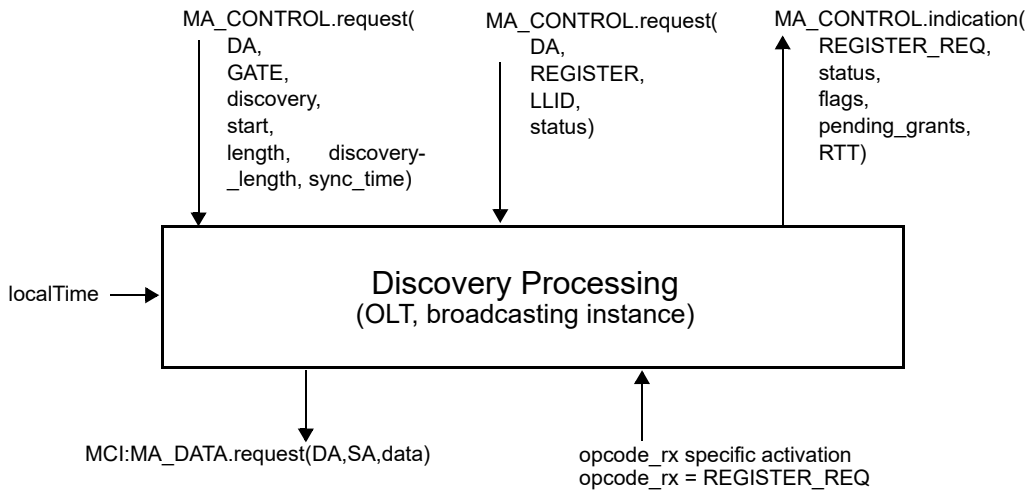

Figure 64–15—Discovery Processing service interfaces (OLT, broadcasting instance)

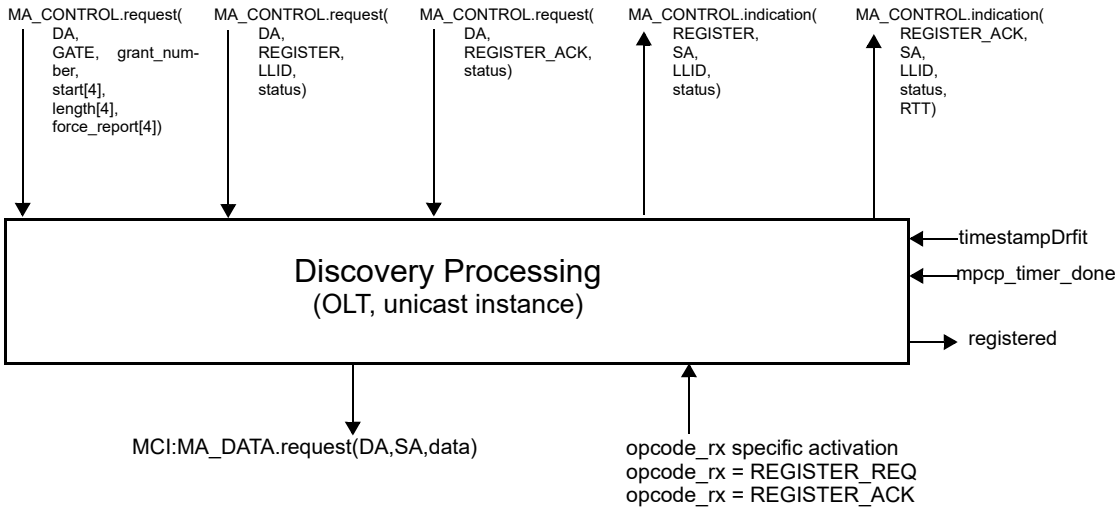

Figure 64–16—Discovery Processing service interfaces (OLT, unicasting instance)

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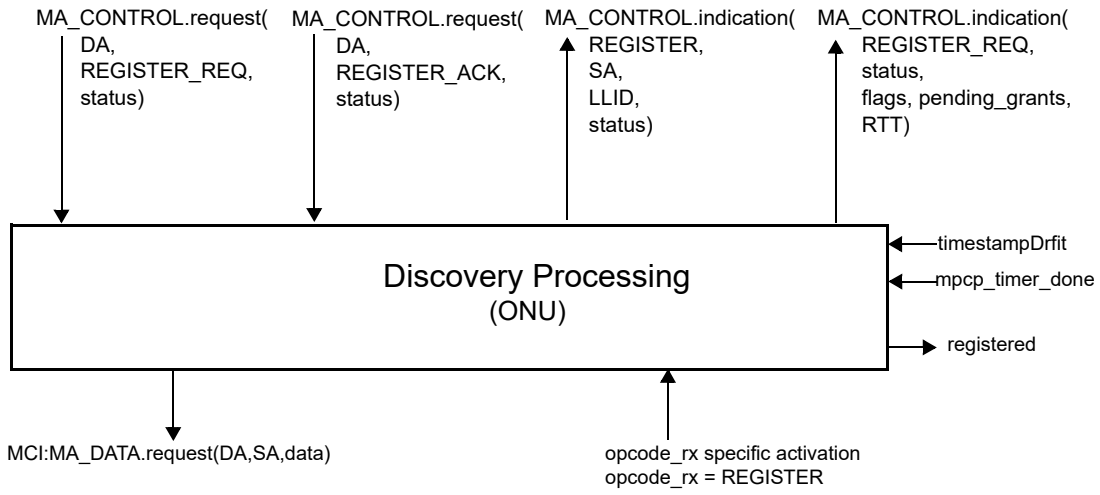

Figure 64–17—Discovery Processing service interfaces (ONU)

64.3.3.1 Constants

No constants defined.

64.3.3.2 Variables

BEGIN
: This variable is defined in 64.2.2.3.

data_rx
: This variable is defined in 64.2.2.3.

data_tx
: This variable is defined in 64.2.2.3.

grantEndTime
: This variable holds the time at which the OLT expects the ONU grant to complete. Failure of a REGISTER_ACK message from an ONU to arrive at the OLT before grantEndTime is a fatal error in the discovery process, and causes registration to fail for the specified ONU, who may then retry to register. The value of grantEndTime is measured in units of time_quantum.
: TYPE: 32-bit unsigned

insideDiscoveryWindow
: This variable holds the current status of the discovery window. It is set to true when the discovery window opens, and is set to false when the discovery window closes.
: TYPE: Boolean

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localTime
: This variable is defined in 64.2.2.2.

opcode_rx
: This variable is defined in 64.2.2.3.

opcode_tx
: This variable is defined in 64.2.2.3.

pendingGrants
: This variable holds the maximum number of pending grants that an ONU is able to queue.
TYPE: 16 bit unsigned

registered
: This variable holds the current result of the Discovery Process. It is set to true once the discovery process is complete and registration is acknowledged.
TYPE: Boolean

syncTime
: This variable holds the time required to stabilize the receiver at the OLT. It counts time_quanta units from the point where transmission output is stable to the point where synchronization has been achieved. The value of syncTime includes gain adjustment interval ($T_{receiver\_settling}$), clock synchronization interval (T_{CDR}), and code-group alignment interval ($T_{code\_group\_align}$), as specified in 60.9.13.2. The OLT conveys the value of syncTime to ONUs in Discovery GATE and REGISTER messages. During the synchronization time only IDLE patterns can be transmitted by an ONU.
TYPE: 16 bit unsigned

timestampDrift
: This variable is defined in 64.2.2.3.

64.3.3.3 Functions

None.

64.3.3.4 Timers

discovery_window_size_timer
: This timer is used to wait for the event signaling the end of the discovery window.
VALUE: The timer value is set dynamically based on the parameters received in a DISCOVERY GATE message.

mpcp_timer
: This timer is used to measure the arrival rate of MPCP frames in the link. Failure to receive frames is considered a fatal fault and leads to deregistration.

64.3.3.5 Messages

MA_DATA.indication(DA, SA, m_sdu, receiveStatus)
: The service primitive is defined in 2.3.2.

MA_DATA.request (DA, SA, m_sdu)
: The service primitive is defined in 2.3.2.

MA_CONTROL.request(DA, GATE, discovery, start, length, discovery_length, sync_time)
: The service primitive used by the MAC Control client at the OLT to initiate the Discovery Process. This primitive takes the following parameters:

DA:	multicast or unicast MAC address.
GATE:	opcode for GATE MPCPDU as defined in Table 31A–1.
discovery:	flag specifying that the given GATE message is to be used for discovery only.

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start: start time of the discovery window.
length: length of the grant given for discovery.
discovery_length: length of the discovery window process.
sync_time: the time interval required to stabilize the receiver at the OLT.

MA_CONTROL.request(DA, GATE, grant_number, start[4], length[4], force_report[4])

This service primitive is used by the MAC Control client at the OLT to issue the GATE message to an ONU. This primitive takes the following parameters:

DA: multicast MAC Control address as defined in Annex 31B.
GATE: opcode for GATE MPCPDU as defined in Table 31A–1.
grant_number: number of grants issued with this GATE message. The number of grants ranges from 0 to 4.
start[4]: start times of the individual grants. Only the first grant_number elements of the array are used.
length[4]: lengths of the individual grants. Only the first grant_number elements of the array are used.
force_report[4]: flags indicating whether a REPORT message should be generated in the corresponding grant. Only the first grant_number elements of the array are used.

MA_CONTROL.request(DA, REGISTER_REQ, status)

The service primitive used by a client at the ONU to request the Discovery Process to perform a registration. This primitive takes the following parameters:

DA: multicast MAC Control address as defined in Annex 31B.
REGISTER_REQ: opcode for REGISTER_REQ MPCPDU as defined in Table 31A–1.
status: This parameter takes on the indication supplied by the flags field in the REGISTER_REQ MPCPDU as defined in Table 64–3.

MA_CONTROL.indication(REGISTER_REQ, status, flags, pending_grants, RTT)

The service primitive issued by the Discovery Process to notify the client and Layer Management that the registration process is in progress. This primitive takes the following parameters:

REGISTER_REQ: opcode for REGISTER_REQ MPCPDU as defined in Table 31A–1.
status: This parameter holds the values incoming or retry. Value incoming is used at the OLT to signal that a REGISTER_REQ message was received successfully. The value retry is used at the ONU to signal to the client that a registration attempt failed and will be repeated.
flags: This parameter holds the contents of the flags field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process is in the OLT.
pending_grants: This parameters holds the contents of the pending_grants field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the OLT.

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RTT: The measured round trip time to/from the ONU is returned in this parameter. RTT is stated in time_quanta units. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the OLT.

MA_CONTROL.request(DA, REGISTER, LLID, status, pending_grants)

The service primitive used by the MAC Control client at the OLT to initiate acceptance of an ONU. This primitive takes the following parameters:

DA: Unicast MAC address or multicast MAC Control address as defined in Annex 31B.

REGISTER: opcode for REGISTER MPCPDU as defined in Table 31A–1.

LLID: This parameter holds the logical link identification number assigned by the MAC Control client.

status: This parameter takes on the indication supplied by the flags field in the REGISTER MPCPDU as defined in Table 64–4.

pending_grants: This parameters echoes back the pending_grants field that was previously received in the REGISTER_REQ message.

MA_CONTROL.indication(REGISTER, SA, LLID, status)

This service primitive is issued by the Discovery Process at the OLT or an ONU to notify the MAC Control client and Layer Management of the result of the change in registration status. This primitive takes the following parameters:

REGISTER: opcode for REGISTER MPCPDU as defined in Table 31A–1.

SA This parameter represents is the MAC address of the OLT.

LLID This parameter holds the logical link identification number assigned by the MAC Control client.

status This parameter holds the value of accepted/denied/deregistered/reregistered.

MA_CONTROL.request(DA, REGISTER_ACK, status)

This service primitive is issued by the MAC Control clients at the ONU and the OLT to acknowledge the registration. This primitive takes the following parameters:

DA: multicast MAC Control address as defined in Annex 31B.

REGISTER_ACK: opcode for REGISTER_ACK MPCPDU as defined in Table 31A–1.

status: This parameter takes on the indication supplied by the flags field in the REGISTER MPCPDU as defined in Table 64–5.

MA_CONTROL.indication(REGISTER_ACK, SA, LLID, status, RTT)

This service primitive is issued by the Discovery Process at the OLT to notify the client and Layer Management that the registration process has completed. This primitive takes the following parameters:

REGISTER_ACK: opcode for REGISTER_ACK MPCPDU as defined in Table 31A–1.

SA This parameter represents the MAC address of the reciprocating device (ONU address at the OLT, and OLT address at the ONU).

LLID This parameter holds the logical link identification number assigned by the MAC Control client.

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status	This parameter holds the value of accepted/denied/reset/ deregistered.
RTT	The measured round trip time to/from the ONU is returned in this parameter. RTT is stated in time_quanta units. This parameter holds a valid value only when the invoking Discovery Process is in the OLT

Opcode-specific function(opcode)

Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

64.3.3.6 State diagram

Discovery process in the OLT shall implement the discovery window setup state diagram shown in Figure 64–18, request processing state diagram as shown in Figure 64–19, register processing state diagram as shown in Figure 64–20, and final registration state diagram as shown in Figure 64–21. The discovery process in the ONU shall implement registration state diagram as shown in Figure 64–22.

Instantiation of state diagrams as described in Figure 64–18, Figure 64–19, and Figure 64–20 is performed only at the Multipoint MAC Control instance attached to the broadcast LLID. Instantiation of state diagrams as described in Figure 64–21 and Figure 64–22 is performed for every Multipoint MAC Control instance, except the instance attached to the broadcast channel.

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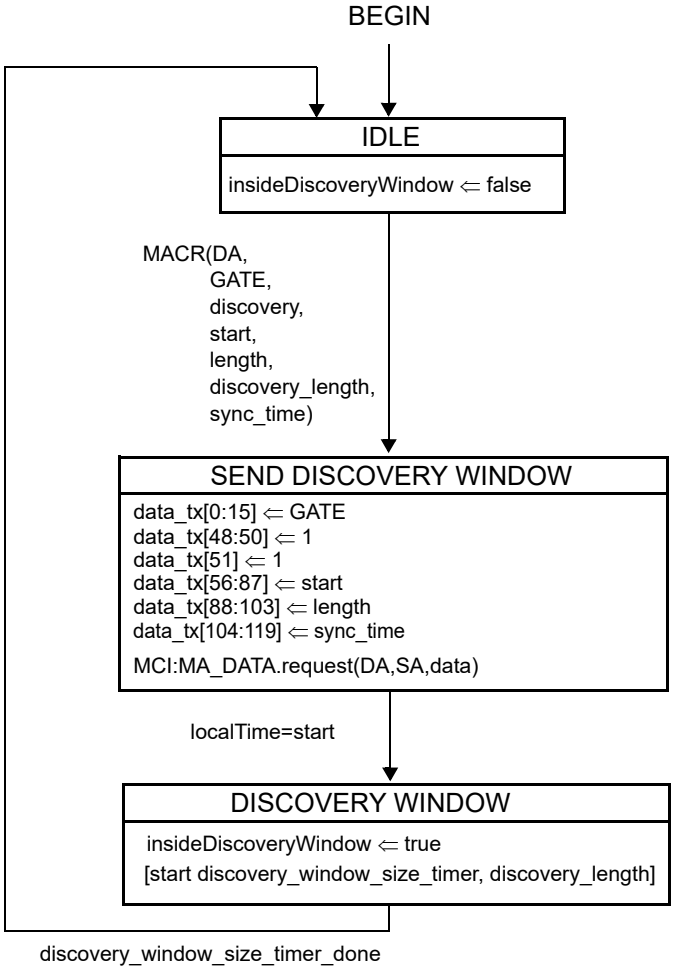

Figure 64–18—Discovery Processing OLT Window Setup state diagram

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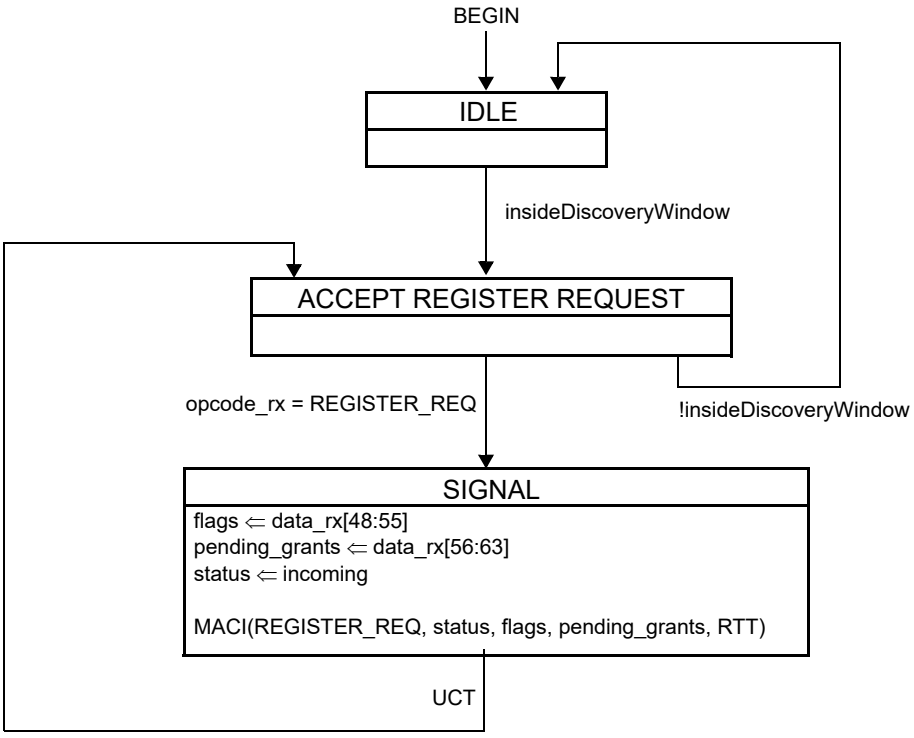

Figure 64–19—Discovery Processing OLT Process Requests state diagram

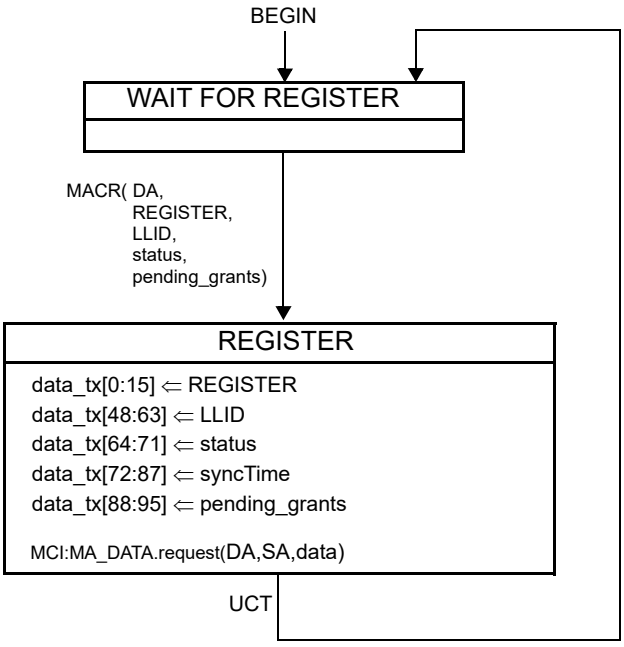

Figure 64–20—Discovery Processing OLT Register state diagram

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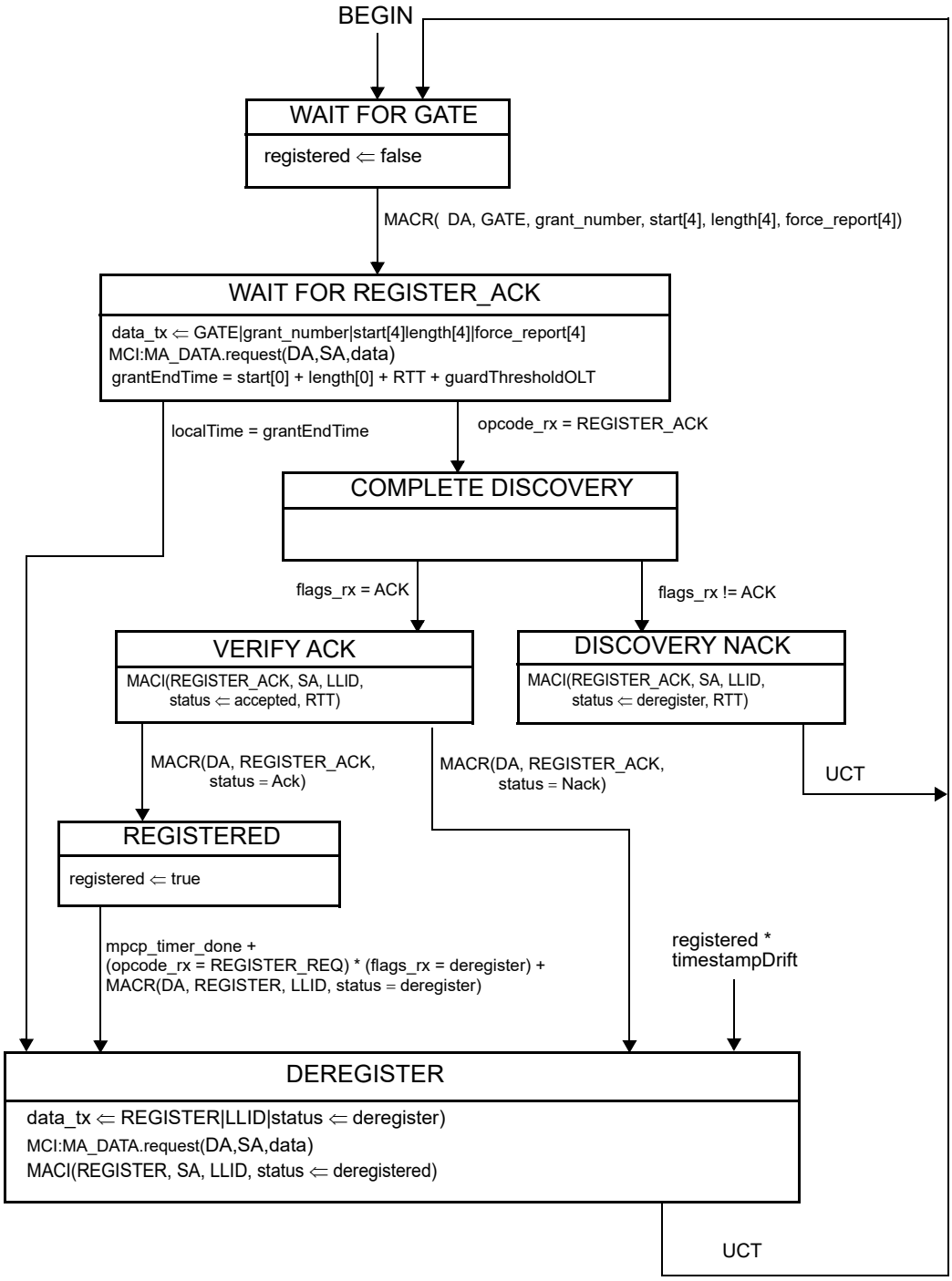

NOTE—The MAC Control Client issues the grant following the REGISTER message, taking the ONU processing delay of REGISTER message into consideration.

Figure 64–21—Discovery Processing OLT Final Registration state diagram

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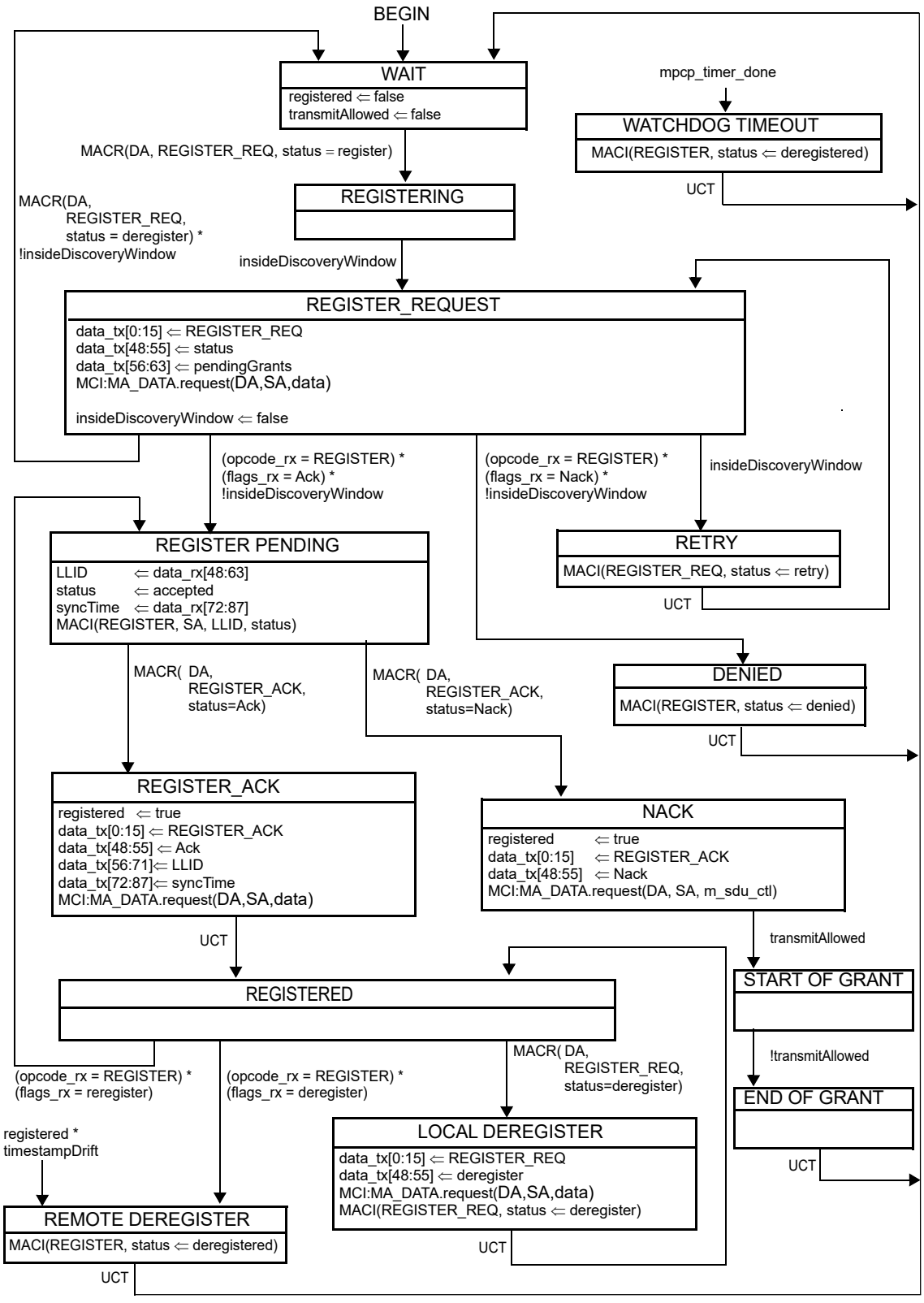

Figure 64–22—Discovery Processing ONU Registration state diagram

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64.3.4 Report Processing

The Report Processing functional block has the responsibility of dealing with queue report generation and termination in the network. Reports are generated by higher layers and passed to the MAC Control sublayer by the MAC Control clients. Status reports are used to signal bandwidth needs as well as for arming the OLT watchdog timer.

Reports shall be generated periodically, even when no request for bandwidth is being made. This keeps a watchdog timer in the OLT from expiring and deregistering the ONU. For proper operation of this mechanism the OLT shall grant the ONU periodically.

The Report Processing functional block, and its MPCP protocol elements are designed for use in conjunction with an IEEE 802.1P capable bridge.

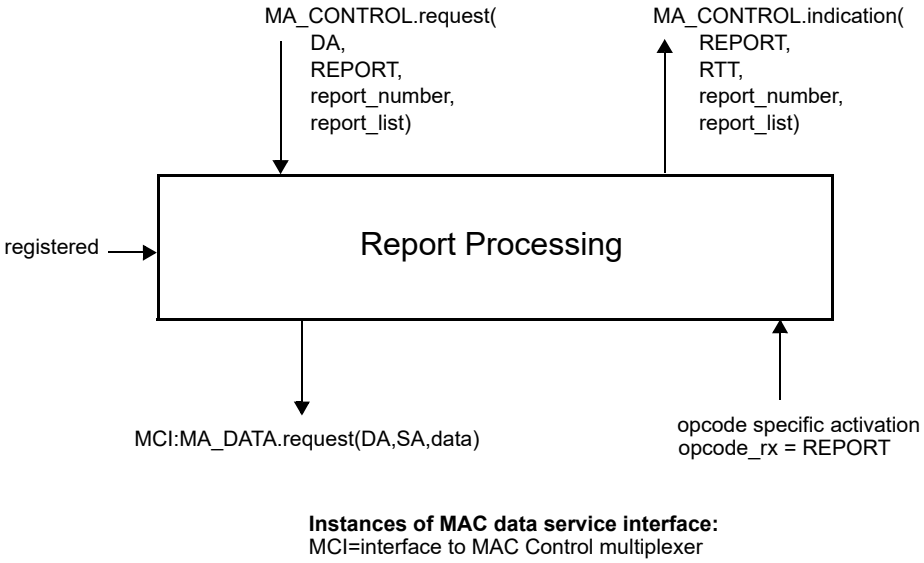

Figure 64–23—Report Processing service interfaces

64.3.4.1 Constants

None

64.3.4.2 Variables

BEGIN
: This variable is used when initiating operation of the functional block state diagram. It is set to true following initialization and every reset.
TYPE: Boolean

data_rx
: This variable is defined in 64.2.2.3.

data_tx
: This variable is defined in 64.2.2.3.

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mpcp_timeout
: This variable represents the maximum allowed interval of time between two MPCPDU messages. Failure to receive at least one frame within this interval is considered a fatal fault and leads to deregistration. This variable is expressed in units of time_quanta.
  TYPE 32-bit unsigned
  VALUE 03-B9-AC-A0 (1 s, default value)

opcode_rx
: This variable is defined in 64.2.2.3.

opcode_tx
: This variable is defined in 64.2.2.3.

registered
: This variable is defined in 64.3.3.2.

report_timeout
: This variable represents the maximum allowed interval of time between two REPORT messages generated by the ONU, expressed in units of time_quanta.
  TYPE 32-bit unsigned
  VALUE 00-2F-AF-08 (50 ms, default value)

64.3.4.3 Functions

None.

64.3.4.4 Timers

report_periodic_timer
: ONUs are required to generate REPORT MPCPDUs with a periodicity of less than report_timeout value. This timer counts down time remaining before a forced generation of a REPORT message in an ONU.

mpcp_timer
: This timer is defined in 64.3.3.4.

64.3.4.5 Messages

MA_DATA.request (DA, SA, m_sdu)
: The service primitive is defined in 2.3.2.

MA_CONTROL.request(DA, REPORT, report_number, report_list)
: This service primitive is used by a MAC Control client to request the Report Process at the ONU to transmit a queue status report. This primitive may be called at variable intervals, independently of the granting process, in order to reflect the time varying aspect of the network. This primitive uses the following parameters:

  DA: multicast MAC Control address as defined in Annex 31B.
  REPORT: opcode for REPORT MPCPDU as defined in Table 31A–1.
  report_number: the number of queue status report sets located in report list. The report_number value ranges from 0 to a maximum of 13.

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report_list: the list of queue status reports. A queue status report consists of two fields: valid and status. The parameter valid, is a Boolean array with length of 8, '0' or false indicates that the corresponding status field is not present (the length of status field is 0), while '1' or true indicates that the corresponding status field is present (the length of status field is 2 octets). The index of the array is meant to reflect the same numbered priority queue in the IEEE 802.1P nomenclature.
The parameter status is an array of 16-bit unsigned integer values. This array consists only of entries whose corresponding bit in field valid is set to true.

MA_CONTROL.indication(REPORT, RTT, report_number, report_list)

The service primitive issued by the Report Process at the OLT to notify the MAC Control client and higher layers the queue status of the MPCP link partner. This primitive may be called multiple times, in order to reflect the time-varying aspect of the network. This primitive uses the following parameters:

REPORT: opcode for REPORT MPCPDU as defined in Table 31A–1.

RTT: this parameter holds an updated round trip time value which is recalculated following each REPORT message reception.

report_number: the number of queue status report sets located in report list. The report_number value ranges from 0 to a maximum of 13.

report_list: the list of queue status reports. A queue status report consists of two fields: valid and status. The parameter valid, is a Boolean array with length of 8, '0' or false indicates that the corresponding status field is not present (the length of status field is 0), while '1' or true indicates that the corresponding status field is present (the length of status field is 2 octets). The index of the array is meant to reflect the same numbered priority queue in the 802.1P nomenclature.
The parameter status is an array of 16-bit unsigned integer values. This array consists only of entries whose corresponding bit in field valid is set to true.

Opcode-specific function(opcode)

Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

64.3.4.6 State diagram

The report process in the OLT shall implement the report processing state diagram as shown in Figure 64–24. The report process in the ONU shall implement the report processing state diagram as shown in Figure 64–25. Instantiation of state diagrams as described is performed for Multipoint MAC Control instances attached to unicast LLIDs only.

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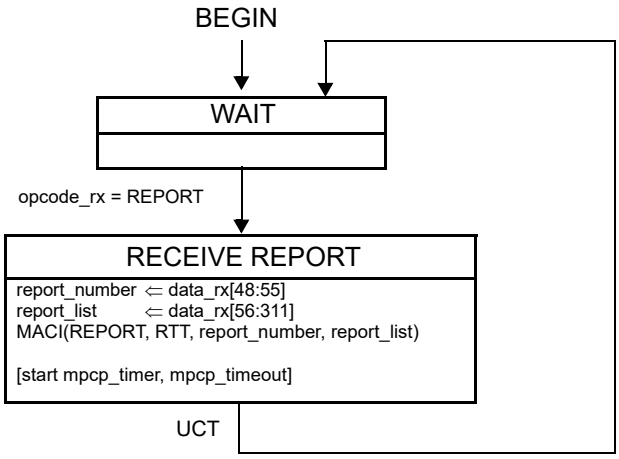
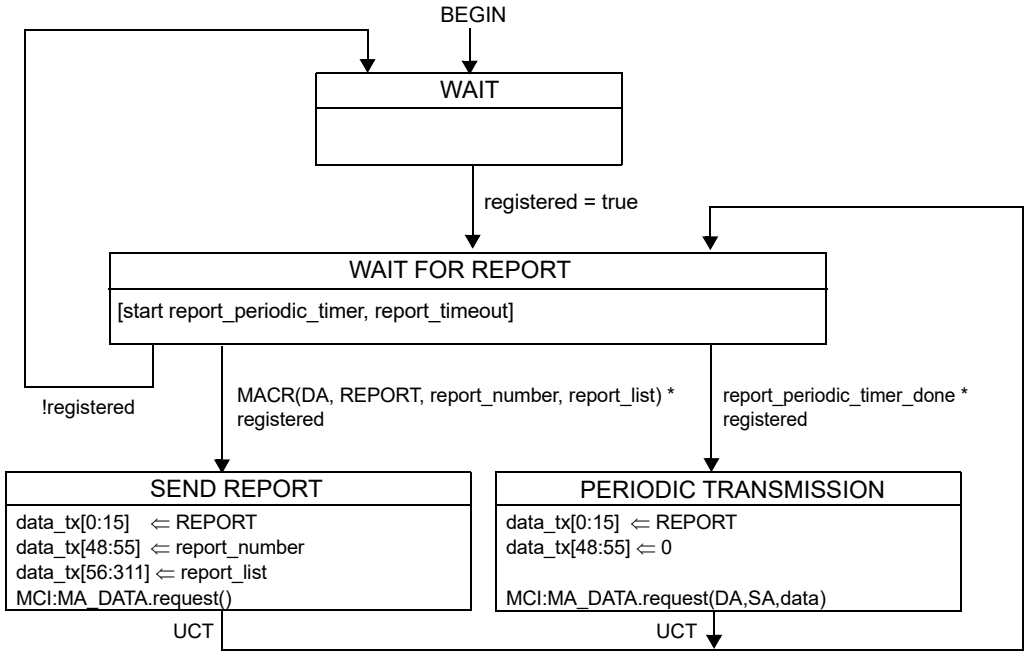


Figure 64–24—Report Processing state diagram at OLT



Instances of MAC data service interface:
MCI=interface to MAC Control multiplexer

Figure 64–25—Report Processing state diagram at ONU

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64.3.5 Gate Processing

A key concept pervasive in Multipoint MAC Control is the ability to arbitrate a single transmitter out of a plurality of ONUs. The OLT controls an ONU's transmission by the assigning of grants.

The transmitting window of an ONU is indicated in GATE message where start time and length are specified. An ONU will begin transmission when its localTime counter matches start_time value indicated in the GATE message. An ONU will conclude its transmission with sufficient margin to ensure that the laser is turned off before the grant length interval has elapsed.

Multiple outstanding grants may be issued to each ONU. The OLT shall not issue more than the maximal supported maximal outstanding grants as advertised by the ONU during registration (see pending grants in 64.3.6.3).

In order to maintain the watchdog timer at the ONU, grants are periodically generated. For this purpose empty GATE messages may be issued periodically.

When registered, the ONU ignores all gate messages where the discovery flag is set.

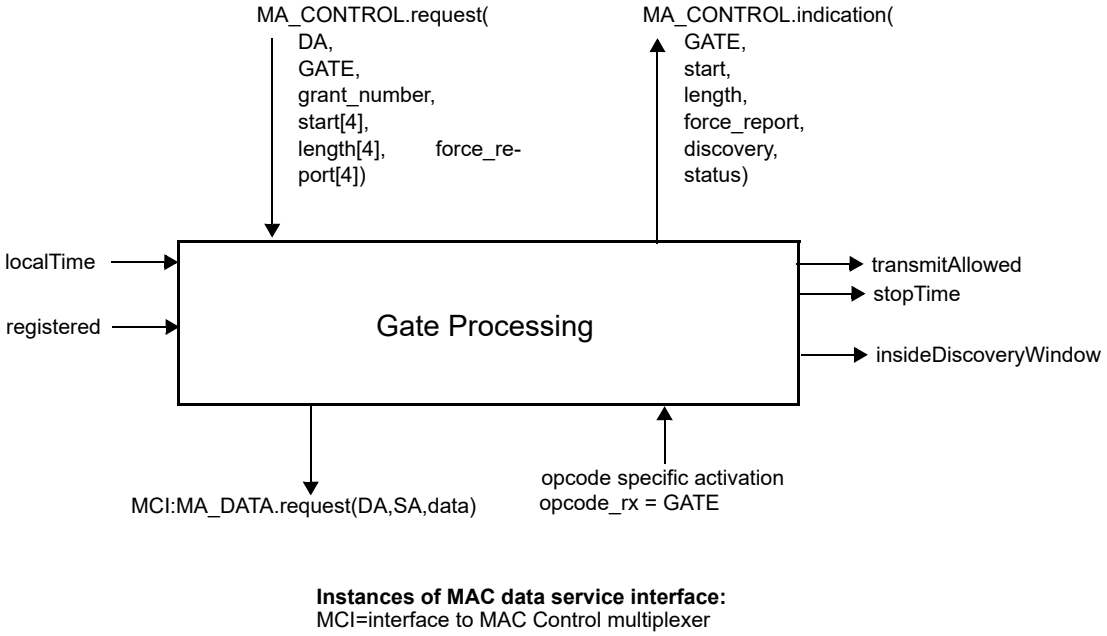

Figure 64–26—Gate Processing service interface

64.3.5.1 Constants

discoveryGrantLength

This constant represents the duration of ONU's transmission during discovery attempt. The value of discoveryGrantLength includes MPCPDU transmission time and tailGuard as defined in 64.2.2.1. discoveryGrantLength is represented in units of time_quanta.

TYPE: 32 bit unsigned
VALUE: 00-00-00-26 (608 ns)

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laserOffTime

This constant holds the time required to terminate the laser. It counts in time_quanta units the time period required for turning off the PMD, as specified in 60.9.13.1.

TYPE: 32 bit unsigned
VALUE: 00-00-00-20 (512 ns)

laserOnTime

This constant holds the time required to initiate the PMD. It counts in time_quanta units the time period required for turning on the PMD, as specified in 60.9.13.1.

TYPE: 32 bit unsigned
VALUE: 00-00-00-20 (512 ns)

max_future_grant_time

This constant holds the time limiting the future time horizon for a valid incoming grant.

TYPE: 32 bit unsigned
VALUE: 03-B9-AC-A0 (1 s)

min_processing_time

This constant is the time required for the ONU processing time.

TYPE: 32 bit unsigned
VALUE: 00-00-04-00 (16.384 us)

tqSize

This constant is defined in 64.2.2.1.

64.3.5.2 Variables

BEGIN

This variable is used when initiating operation of the functional block state diagram. It is set to true following initialization and every reset.

TYPE: Boolean

counter

This variable is used as a loop iterator counting the number of incoming grants in a GATE message.

TYPE: integer

currentGrant

This variable is used for local storage of a pending grant state during processing. It is dynamically set by the Gate Processing functional block and is not exposed.

The state is a structure field composed of multiple subfields.

TYPE: structure {

DA	48 bit unsigned, a.k.a MAC address type
start	32 bit unsigned
length	16 bit unsigned
force_report	Boolean
discovery	Boolean}

data_rx

This variable is defined in 64.2.2.3.

data_tx

This variable is defined in 64.2.2.3.

effectiveLength

This variable is used for temporary storage of a normalized net time value. It holds the net effective length of a grant normalized for elapsed time, and compensated for the periods required to turn the laser on and off, and waiting for receiver lock.

TYPE: 32 bit unsigned

fecEnabled

This variable is defined in 64.2.2.3.

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gate_timeout

This variable represents the maximum allowed interval of time between two GATE messages generated by the OLT to the same ONU, expressed in units of time_quanta.

TYPE 32-bit unsigned
VALUE 00-2F-AF-08 (50 ms, default value)

grantList

This variable is used for storage of the list of pending grants. It is dynamically set by the Gate Processing functional block and is not exposed. Each time a grant is received it is added to the list.

The list elements are structure fields composed of multiple subfields.

The list is indexed by the start subfield in each element for quick searches.

TYPE: list of elements having the structure define in currentGrant

insideDiscoveryWindow

This variable is defined in 64.3.3.2.

maxDelay

This variable holds the maximum delay that can be applied by an ONU before sending the REGISTER MPCPDU. This delay is calculated such that the ONU would have sufficient time to transmit the REGISTER message and its associated overhead (FEC parity date, end-of-frame sequence, etc.) and terminate the laser before the end of the discovery grant.

TYPE 16 bit unsigned

nextGrant

This variable is used for local storage of a pending grant state during processing. It is dynamically set by the Gate Processing functional block and is not exposed. The content of the variable is the next grant to become active.

TYPE: element having same structure as defined in currentGrant

nextStopTime

This variable holds the value of the localTime counter corresponding to the end of the next grant.

TYPE: 32 bit unsigned

registered

This variable is defined in 64.3.3.2.

stopTime

This variable is defined in 64.2.2.3.

syncTime

This variable is defined in 64.3.3.2.

transmitAllowed

This variable is defined in 64.2.2.3.

64.3.5.3 Functions

empty(list)

This function is use to check whether the list is empty. When there are no elements queued in the list, the function returns true. Otherwise, a value of false is returned.

InsertInOrder(sorted_list, inserted_element)

This function is used to queue an element inside a sorted list. The queueing order is sorted. In the condition that the list is full the element may be discarded. The length of the list is dynamic and its maximal size equals the value advertised during registration as maximum number of pending grants.

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IsBroadcast(grant)

This function is used to check whether its argument represents a broadcast grant, i.e., grant given to multiple ONUs. This is determined by the destination MAC address of the corresponding GATE message. The function returns the value true when MAC address is a global assigned MAC Control address as defined in Annex 31B, and false otherwise.

PeekHead(sorted_list)

This function is used to check the content of a sorted list. It returns the element at the head of the list without dequeuing the element.

Random(r)

This function is used to compute a random integer number uniformly distributed between 0 and r. The randomly generated number is then returned by the function.

RemoveHead(sorted_list)

This function is used to dequeue an element from the head of a sorted list. The return value of the function is the dequeued element.

64.3.5.4 Timers

gntStTmr

This timer is used to wait for the event signaling the start of a grant window.
VALUE: The timer value is dynamically set according to the signaled grant start time.

gntWinTmr

This timer is used to wait for the event signaling the end of a grant window.
VALUE: The timer value is dynamically set according to the signaled grant length.

gate_periodic_timer

The OLT is required to generate GATE MPCPDUs with a periodicity of less than gate_timeout value. This timer counts down time remaining before a forced generation of a GATE message in the OLT.

mpcp_timer

This timer is defined in 64.3.3.4.

rndDlyTmr

This timer is used to measure a random delay inside the discovery window. The purpose of the delay is to apriori reduce the probability of transmission overlap during the registration process, and thus lowering the expectancy of registration time in the PON.
VALUE: A random value less than the net discovery window size less the REGISTER_REQ MPCPDU frame size less the idle period and laser turn on and off delays less the preamble size less the IFG size. The timer value is set dynamically based on the parameters passed from the client.

64.3.5.5 Messages

MA_DATA.request (DA, SA, m_sdu)

The service primitive is defined in 2.3.2.

MA_CONTROL.request(DA, GATE, grant_number, start[4], length[4], force_report[4])

This service primitive is defined in 64.3.3.5.

MA_CONTROL.indication(GATE, start, length, force_report, discovery, status)

This service primitive issued by the Gate Process at the ONU to notify the MAC Control client and higher layers that a grant is pending. This primitive is invoked multiple times when a single GATE message arrives with multiple grants. It is also generated at the start and end of each grant as it becomes active. This primitive uses the following parameters:

GATE: opcode for GATE MPCPDU as defined in Table 31A–1.

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start:	start time of the grant. This parameter is not present when the status value is deactive.
length:	length of the grant. This parameter is not present when the status value is deactive.
force_report:	flags indicating whether a REPORT message should be transmitted in this grant. This parameter is not present when the status value is deactive.
discovery:	This parameter holds the value true when the grant is to be used for the discovery process, and false otherwise. This parameter is not present when the status value is deactive.
status:	This parameter takes the value *arrive* on grant reception, *active* when a grant becomes active, and *deactive* at the end of a grant.

Opcode-specific function(opcode)

Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

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64.3.5.6 State diagrams

The gating process in the OLT shall implement the gate processing state diagram as shown in Figure 64–26. The gating process in the ONU shall implement the gate processing state diagram as shown in Figure 64–27. Instantiation of state diagrams as described is performed for all Multipoint MAC Control instances.

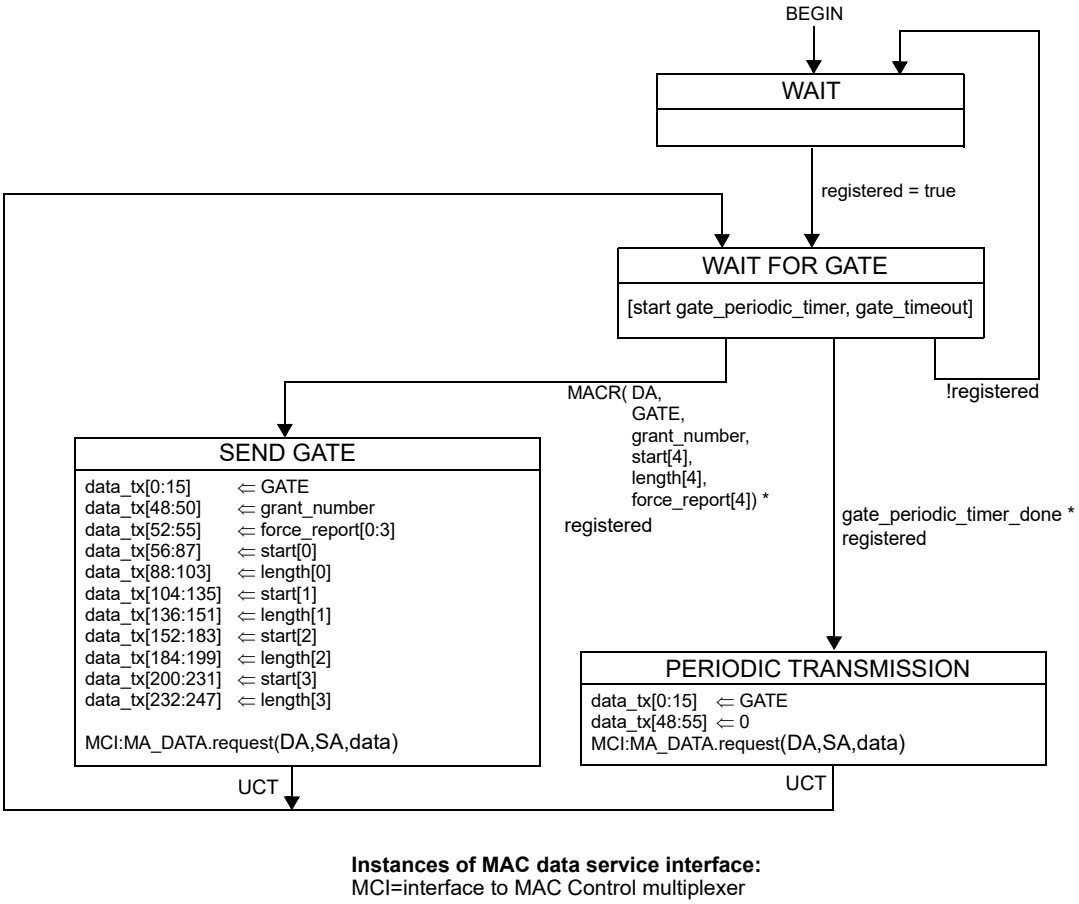

Figure 64–27—Gate Processing state diagram at OLT

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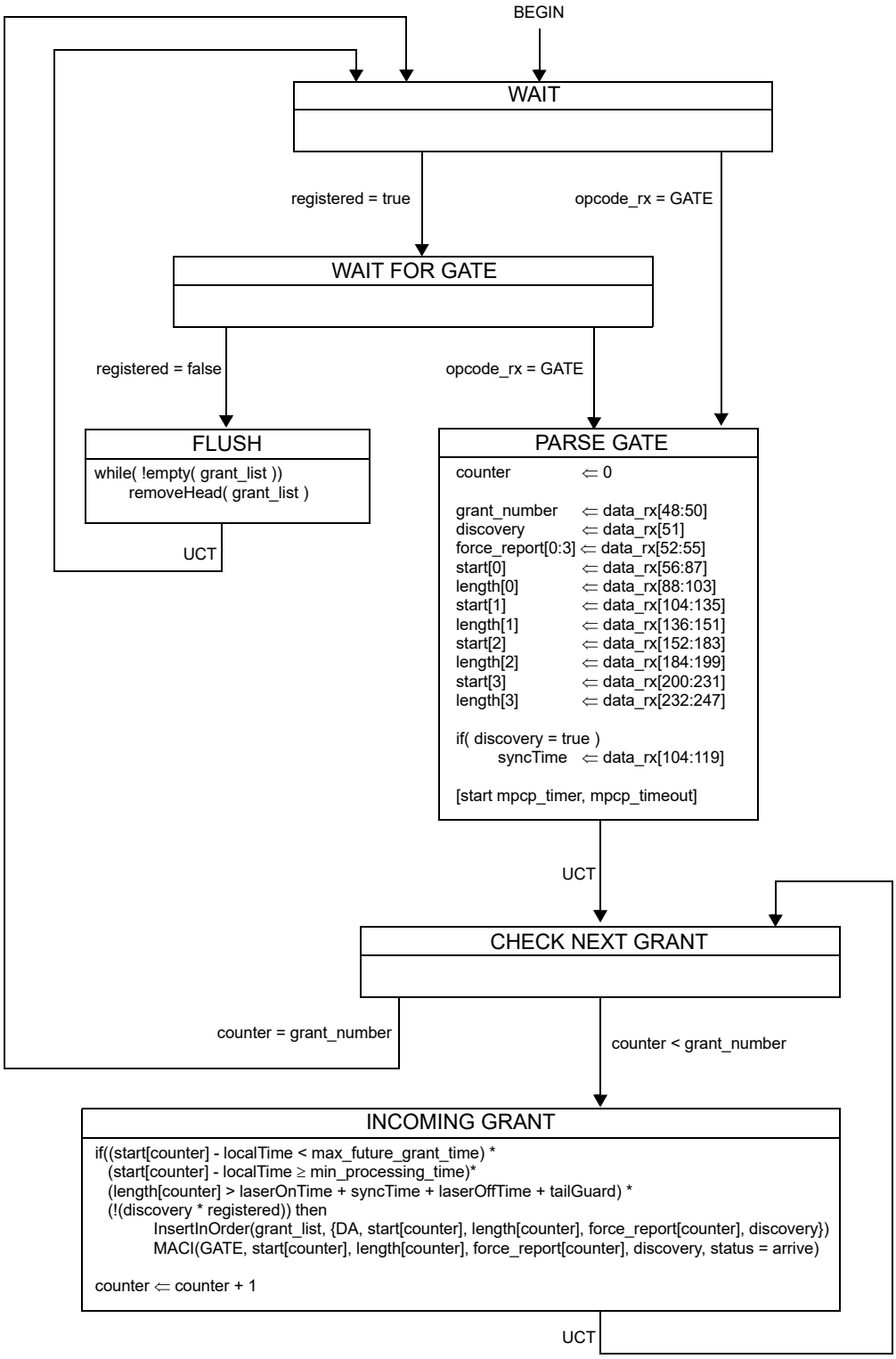

Figure 64–28—Gate Processing ONU Programing state diagram

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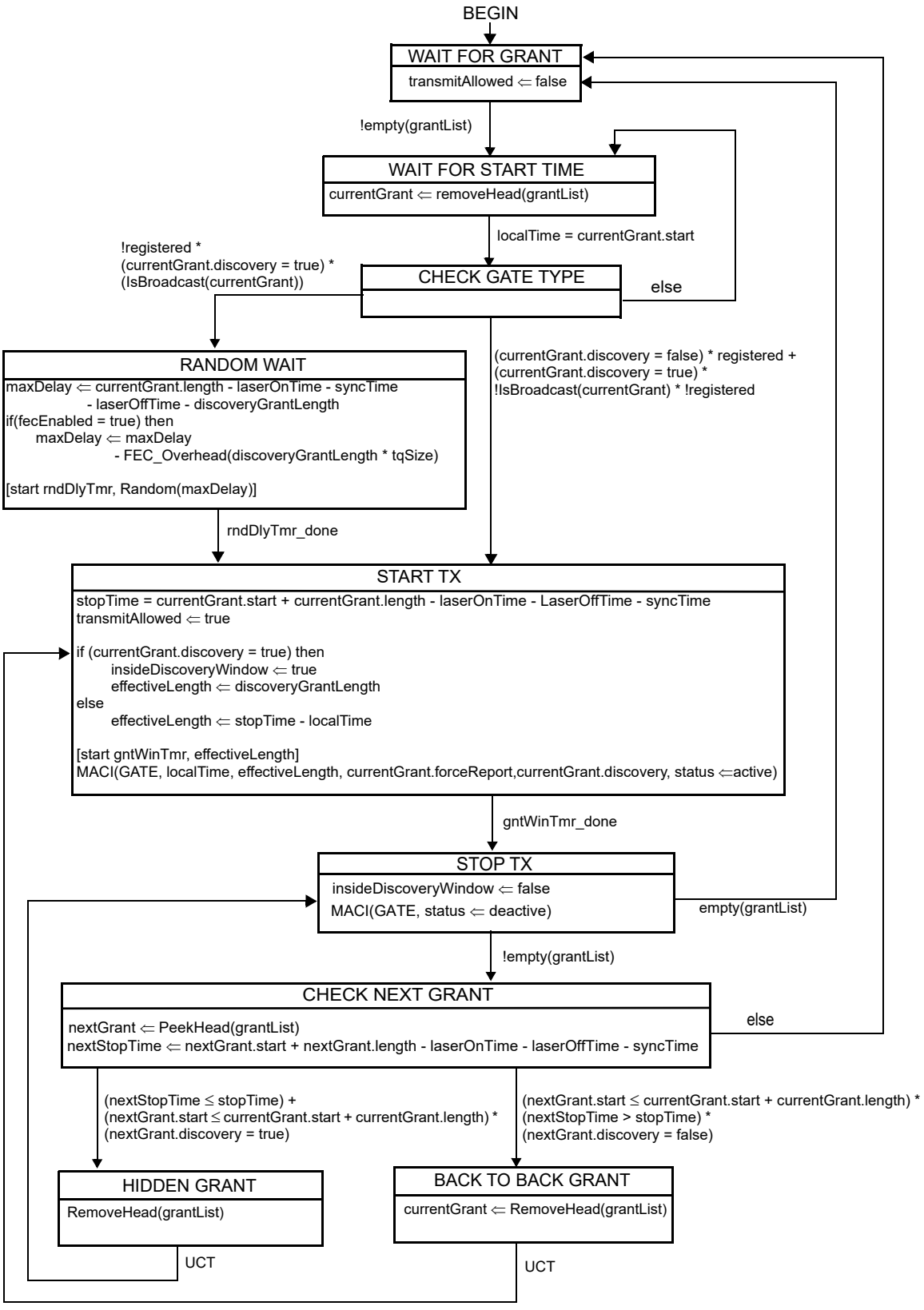

Figure 64–29—Gate Processing ONU Activation state diagram

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64.3.6 MPCPDU structure and encoding

The MPCPDU structure shall be as shown in Figure 64–30, and is further defined in the following definitions:

a) Destination Address (DA). The DA in MPCPDU is the MAC Control Multicast address as specified in the annexes to Clause 31, or the individual MAC address associated with the port to which the MPCPDU is destined.
b) Source Address (SA). The SA in MPCPDU is the individual MAC address associated with the port through which the MPCPDU is transmitted. For MPCPDUs originating at the OLT end, this can be the address any of the individual MACs. These MACs may all share a single unicast address, as explained in 64.1.2.
c) Length/Type. The Length/Type in MPCPDU carries the MAC_Control_Type field value as specified in 31.4.1.3.
d) Opcode. The opcode identifies the specific MPCPDU being encapsulated. Values are defined in Table 31A–1.
e) Timestamp. The timestamp field conveys the content of the localTime register at the time of transmission of the MPCPDUs. This field is 32 bits long, and counts 16 bit transmissions. The timestamp counts time in 16 bit time granularity.
f) Data/Reserved/PAD. These 40 octets are used for the payload of the MPCPDUs. When not used they would be filled with zeros on transmission, and be ignored on reception.
g) FCS. This field is the Frame Check Sequence, typically generated by the underlying MAC.

Based on the MAC instance used to generate the specific MPCPDU, the appropriate LLID shall be generated by the RS.

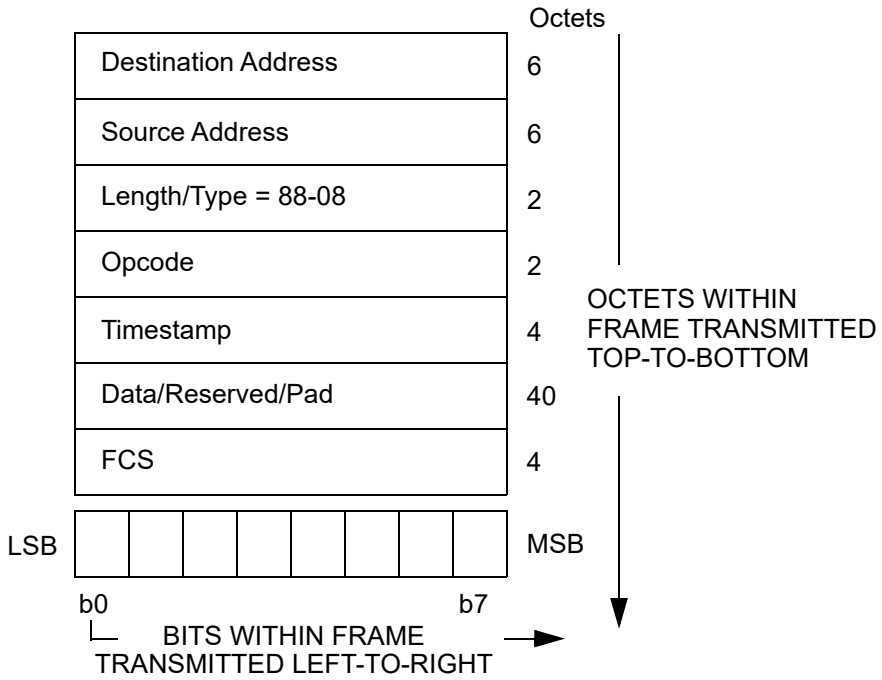

Figure 64–30—Generic MPCPDU

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64.3.6.1 GATE description

The purpose of GATE message is to grant transmission windows to ONUs for both discovery messages and normal transmission. Up to four grants can be included in a single GATE message. The number of grants can also be set to zero for using the GATE message as an MPCP keep alive from OLT to the ONU.

The GATE MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) Opcode. The opcode for the GATE MPCPDU is 0x0002.
b) Flags. This is an 8 bit flag register that holds the following flags: The Number of grants field contains the number of grants, composed of valid Length, Start Time pairs in this MPCPDU. This is a number between 0 and 4. Note: when Number of grants is set to 0, sole purpose of message is conveying of timestamp to ONU.
   The Discovery flag field indicates that the signaled grants would be used for the discovery process, in which case a single grant shall be issued in the gate message.
   The Force Report flag fields ask the ONU to issue a REPORT message related to the corresponding grant number at the corresponding transmission opportunity indicated in this GATE.
c) Grant #n Length. Length of the signaled grant, this is an 16 bit unsigned field. The length is counted in 16 bit time increments. There are 4 Grants that are possibly packed into the GATE MPCPDU. The laserOnTime, syncTime, and laserOffTime are included in and thus consume part of Grant #n Length.
d) Grant #n Start Time. Start time of the grant, this is an 32 bit unsigned field. The start time is compared to the local clock, to correlate the start of the grant. Transmitted values shall satisfy the condition Grant #n Start Time < Grant #n + 1 Start Time for consecutive grants within the same GATE MPCPDU.
e) Sync Time. This is an unsigned 16 bit value signifying the required synchronization time of the OLT receiver. During the synchronization time the ONU shall send IDLE code-pairs. The value is counted in 16 bit time increments. The advertised value includes synchronization requirement on all receiver elements including PMD, PMA and PCS. This field is present only when the gate is a discovery gate, as signaled by the Discovery flag and is not present otherwise.
f) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored on reception when constructing a complying MPCP protocol implementation. The size of this field depends on the used Grant #n Length/Start Time entry-pairs, and varies in length from 13–39 accordingly.

Table 64–1—GATE MPCPDU Number of grants/Flags Fields

Bit	Flag Field	Values
0–2	Number of grants	0–4
3	Discovery	0—Normal GATE 1—Discovery GATE
4	Force Report Grant 1	0—No action required 1—A REPORT frame should be issued at the corresponding transmission opportunity indicated in Grant 1
5	Force Report Grant 2	0—No action required 1—A REPORT frame should be issued at the corresponding transmission opportunity indicated in Grant 2
6	Force Report Grant3	0—No action required 1—A REPORT frame should be issued at the corresponding transmission opportunity indicated in Grant 3
7	Force Report Grant 4	0—No action required 1—A REPORT frame should be issued at the corresponding transmission opportunity indicated in Grant 4

The GATE MPCPDU shall be generated by a MAC Control instance mapped to an active ONU, and as such shall be marked with a unicast type of LLID, except when the discovery flag is set where the MAC Control instance is mapped to all ONUs and such frame is marked by the broadcast LLID.

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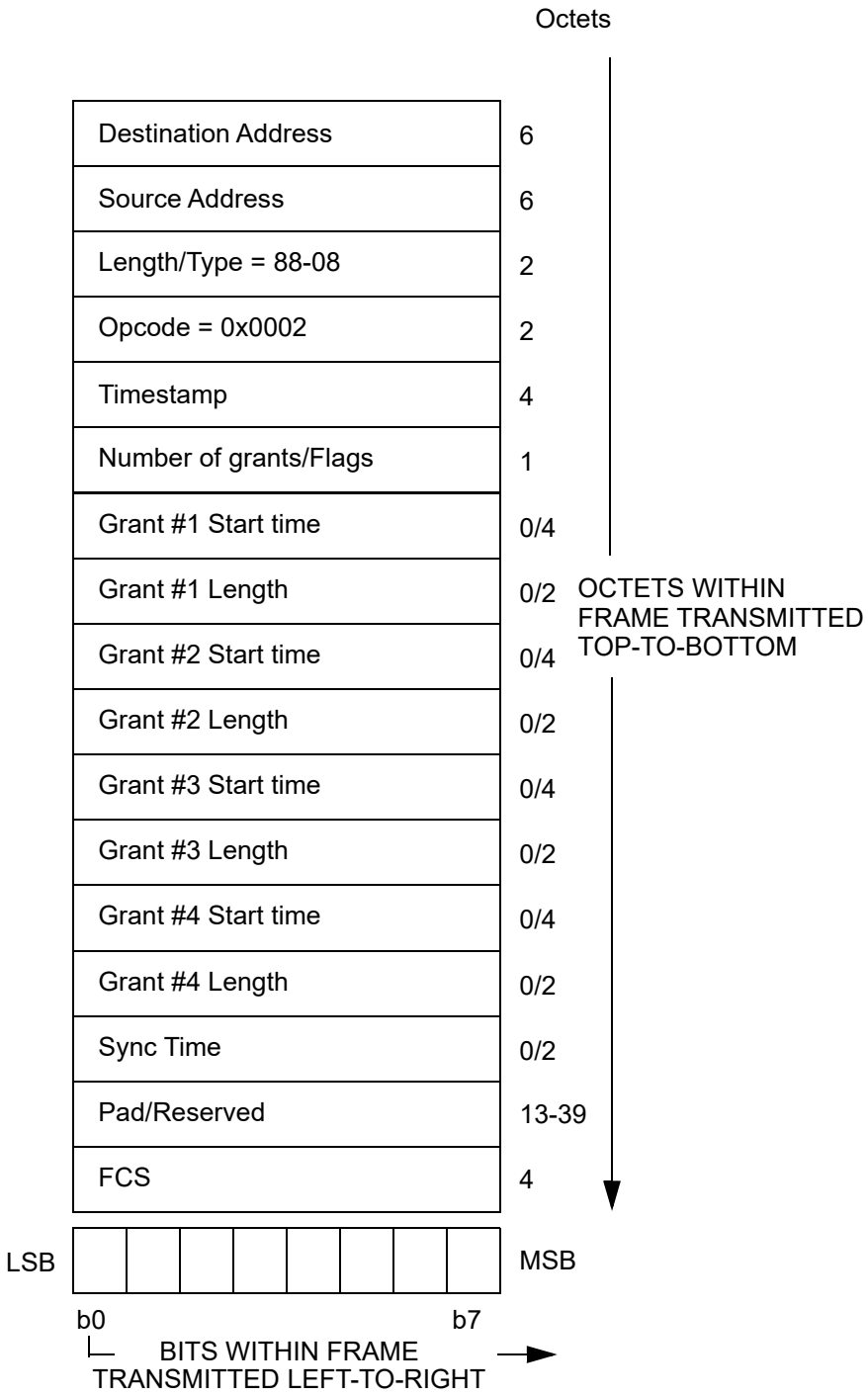

Figure 64–31—GATE MPCPDU

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64.3.6.2 REPORT description

REPORT messages have several functionalities. Time stamp in each REPORT message is used for round trip (RTT) calculation. In the REPORT messages ONUs indicate the upstream bandwidth needs they request per IEEE 802.1Q priority queue. REPORT messages are also used as keep-alives from ONU to OLT. ONUs issue REPORT messages periodically in order to maintain link health at the OLT as defined in 64.3.4. In addition, the OLT may specifically request a REPORT message.

The REPORT MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) Opcode. The opcode for the REPORT MPCPDU is 0x0003.
b) Number of Queue Sets. This field specifies the number of requests in the REPORT message. A REPORT frame may hold multiple sets of Report bitmap and Queue #n as specified in the Number of Queue Sets field
c) Report bitmap. This is an 8 bit flag register that indicates which queues are represented in this REPORT MPCPDU.

Table 64–2—REPORT MPCPDU Report bitmap fields

Bit	Flag Field	Values
0	Queue 0	0—queue 0 report is not present 1—queue 0 report is present
1	Queue 1	0—queue 1 report is not present 1—queue 1 report is present
2	Queue 2	0—queue 2 report is not present 1—queue 2 report is present
3	Queue 3	0—queue 3 report is not present 1—queue 3 report is present
4	Queue 4	0—queue 4 report is not present 1—queue 4 report is present
5	Queue 5	0—queue 5 report is not present 1—queue 5 report is present
6	Queue 6	0—queue 6 report is not present 1—queue 6 report is present
7	Queue 7	0—queue 7 report is not present 1—queue 7 report is present

d) Queue #n Report. This value represents the length of queue# n at time of REPORT message generation. The reported length shall be adjusted to account for the necessary inter-frame spacing and FEC parity data overhead, if FEC is enabled. The Queue #n Report field is an unsigned 16 bit integer representing transmission request in units of time quanta. This field is present only when the corresponding flag in the Report bitmap is set.
e) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored on reception when constructing a complying MPCP protocol implementation. The size of this field depends on the used Queue Report entries, and accordingly varies in length from 0 to 39.

The REPORT MPCPDU shall be generated by a MAC Control instance mapped to an active ONU, and as such shall be marked with a unicast type of LLID.

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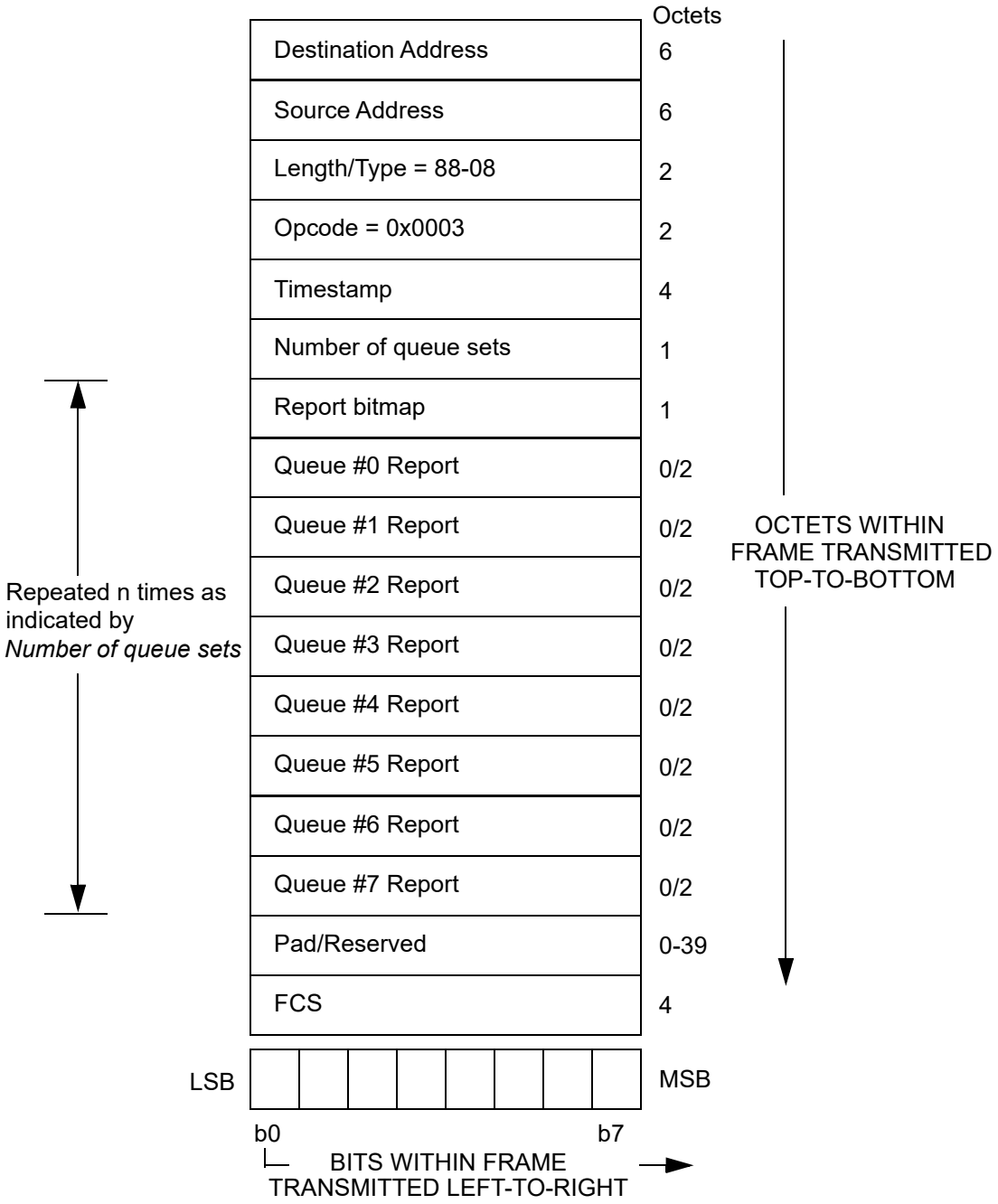

Figure 64–32—REPORT MPCPDU

64.3.6.3 REGISTER_REQ description

The REGISTER_REQ MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) Opcode. The opcode for the REGISTER_REQ MPCPDU is 0x0004.
b) Flags. This is an 8 bit flag register that indicates special requirements for the registration.

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Table 64–3—REGISTER_REQ MPCPDU Flags fields

Value	Indication	Comment
0	Reserved	Ignored on reception.
1	Register	Registration attempt for ONU.
2	Reserved	Ignored on reception.
3	Deregister	This is a request to deregister the ONU. Subsequently, the MAC is deallocated and the LLID may be reused.
4–255	Reserved	Ignored on reception.

c) Pending grants. This is an unsigned 8 bit value signifying the maximum number of future grants the ONU is configured to buffer. The OLT should not grant the ONU more than this maximum number of Pending grants vectors composed of {start, length, force_report, discovery} into the future.
d) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored on reception when constructing a complying MPCP protocol implementation.

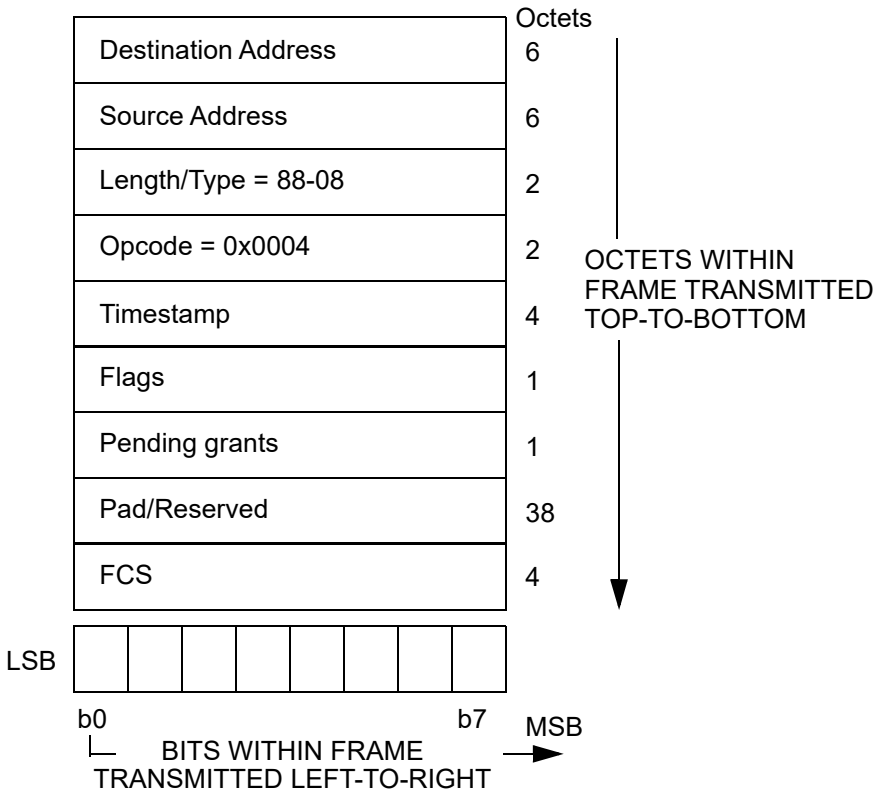

Figure 64–33—REGISTER_REQ MPCPDU

The REGISTER_REQ MPCPDU shall be generated by a MAC Control instance mapped to an undiscovered ONU, and as such shall be marked with a broadcast type of LLID.

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64.3.6.4 REGISTER description

The REGISTER MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) DA. The destination address used shall be an individual MAC address.
b) Opcode. The opcode for the REGISTER MPCPDU is 0x0005.
c) Assigned Port. This field holds a 16 bit unsigned value reflecting the LLID of the port assigned following registration.
d) Flags. this is an 8 bit flag register that indicates special requirements for the registration.

Table 64–4—REGISTER MPCPDU Flags field

Value	Indication	Comment
0	Reserved	Ignored on reception.
1	Reregister	The ONU is explicitly asked to re-register.
2	Deregister	This is a request to deallocate the port and free the LLID. Subsequently, the MAC is deallocated.
3	Ack	The requested registration is successful.
4	Nack	The requested registration attempt is denied by the higher-layer-entity.
5–255	Reserved	Ignored on reception.

e) Sync Time. This is an unsigned 16 bit value signifying the required synchronization time of the OLT receiver. During the synchronization time the ONU transmits only IDLE code-pairs. The value is counted in 16 bit time increments. The advertised value includes synchronization requirement on all receiver elements including PMD, PMA and PCS.
f) Echoed pending grants. This is an unsigned 8 bit value signifying the number of future grants the ONU may buffer before activating. The OLT should not grant the ONU more than this number of grants into the future.
g) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored on reception when constructing a complying MPCP protocol implementation.

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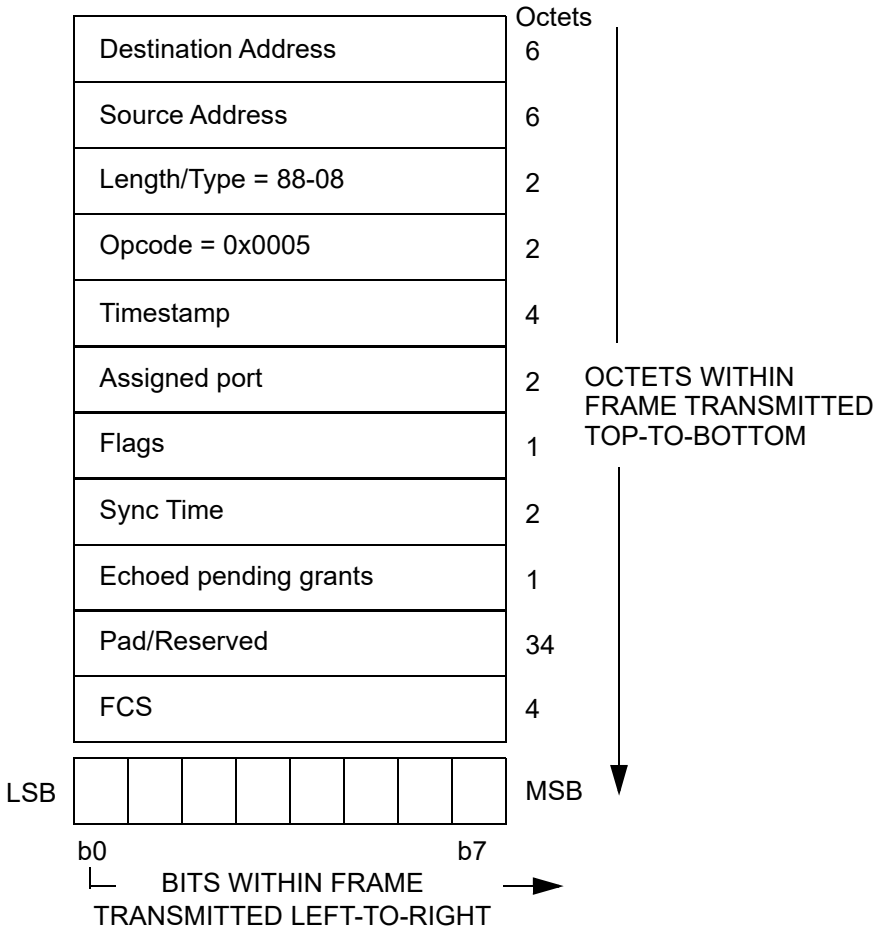

Figure 64–34—REGISTER MPCPDU

The REGISTER MPCPDU shall be generated by a MAC Control instance mapped to all ONUs and such frame is marked by the broadcast LLID.

64.3.6.5 REGISTER_ACK description

The REGISTER_ACK MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) Opcode. The opcode for the REGISTER_ACK MPCPDU is 0x0006.
b) Flags. This is an 8-bit flag register that indicates special requirements for the registration.Echoed assigned port. This field holds a 16 bit unsigned value reflecting the LLID of the port assigned following registration.
c) Echoed Sync Time. This is an unsigned 16 bit value echoing the required synchronization time of the OLT receiver as previously advertised (see 64.3.6.4).
d) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored at reception when constructing a complying MPCP protocol implementation.

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Table 64–5—REGISTER_ACK MPCPDU Flags fields

Value	Indication	Comment
0	Nack	The requested registration attempt is denied by the higher-layer-entity.
1	Ack	The registration process is successfully acknowledged.
2–255	Reserved	Ignored on reception.

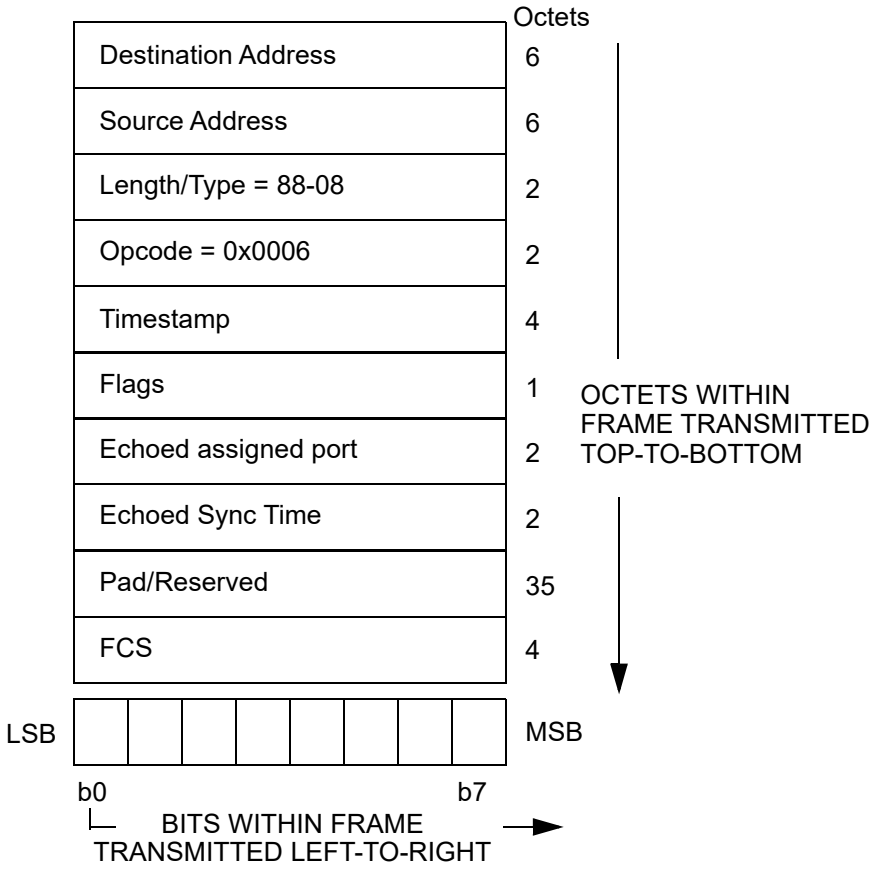

Figure 64–35—REGISTER_ACK MPCPDU

The REGISTER_ACK MPCPDU shall be generated by a MAC Control instance mapped to an active ONU, and as such shall be marked with a unicast type of LLID.

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64.4 Protocol implementation conformance statement (PICS) proforma for Clause 64, Multipoint MAC Control[126]

64.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 64 Multipoint MAC Control, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

64.4.2 Identification

64.4.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

64.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 64, Multipoint MAC Control
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[126]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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64.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*OLT	OLT functionality	64.1	Device supports functionality required for OLT	O/1	Yes [ ] No [ ]
*ONU	ONU functionality	64.1	Device supports functionality required for ONU	O/1	Yes [ ] No [ ]

64.4.4 PICS proforma tables for Multipoint MAC Control

64.4.4.1 Compatibility Considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Delay through MAC and PHY	64.3.2.4	Maximum delay variation of 16 ns (1 time_quantum)	M	Yes [ ]
CC2	OLT grant time delays	64.3.2.4	Not grant nearer than 1024 time_quanta into the future	OLT:M	Yes [ ]
CC3	ONU processing delays	64.3.2.4	Process all messages in less than 1024 time_quanta	ONU:M	Yes [ ]
CC4	OLT grant issuance	64.3.2.4	Not grant more than one message every 1024 time_quanta	OLT:M	Yes [ ]

64.4.4.2 Multipoint MAC Control

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	OLT localTime	64.2.2.2	Track transmit clock	OLT:M	Yes [ ]
OM2	ONU localTime	64.2.2.2	Track receive clock	ONU:M	Yes [ ]
OM3	Random wait for transmitting REGISTER_REQ messages	64.3.3	Shorter than length of discovery time window	ONU:M	Yes [ ]
OM4	Periodic report generation	64.3.4	Reports are generated periodically	ONU:M	Yes [ ]
OM5	Periodic granting	64.3.4	Grants are issued periodically	OLT:M	Yes [ ]
OM6	Issuing of grants	64.3.5	Not issue more than maximal supported grants	OLT:M	Yes [ ]

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64.4.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Multipoint Transmission Control	64.2.2.7	Meets the requirements of Figure 64–9	M	Yes [ ]
SM2	OLT Control Parser	64.2.2.7	Meets the requirements of Figure 64–10	M	Yes [ ]
SM3	ONU Control Parser	64.2.2.7	Meets the requirements of Figure 64–11	M	Yes [ ]
SM4	OLT Control Multiplexer	64.2.2.7	Meets the requirements of Figure 64–12	OLT:M	Yes [ ]
SM5	ONU Control Multiplexer	64.2.2.7	Meets the requirements of Figure 64–13	OLT:M	Yes [ ]
SM6	Discovery Processing OLT Window Setup	64.3.3.6	Meets the requirements of Figure 64–18	OLT:M	Yes [ ]
SM7	Discovery Processing OLT Process Requests	64.3.3.6	Meets the requirements of Figure 64–19	OLT:M	Yes [ ]
SM8	Discovery Processing OLT Register	64.3.3.6	Meets the requirements of Figure 64–20	ONU:M	Yes [ ]
SM9	Discovery Processing OLT Final Registration	64.3.3.6	Meets the requirements of Figure 64–21	OLT:M	Yes [ ]
SM10	Discovery Processing ONU Registration	64.3.3.6	Meets the requirements of Figure 64–22	ONU:M	Yes [ ]
SM11	Report Processing at OLT	64.3.4.6	Meets the requirements of Figure 64–24	OLT:M	Yes [ ]
SM12	Report Processing at ONU	64.3.4.6	Meets the requirements of Figure 64–25	ONU:M	Yes [ ]
SM13	Gate Processing at OLT	64.3.5.6	Meets the requirements of Figure 64–27	OLT:M	Yes [ ]
SM14	Gate Processing at ONU	64.3.5.6	Meets the requirements of Figure 64–28	ONU:M	Yes [ ]
SM15	Gate Processing ONU Activation	64.3.5.6	Meets the requirements of Figure 64–29	ONU:M	Yes [ ]

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64.4.4.4 MPCP

Item	Feature	Subclause	Value/Comment	Status	Support
MP1	MPCPDU structure	64.3.6	As in Figure 64–30	M	Yes [ ]
MP2	LLID for MPCPDU	64.3.6	RS generates LLID for MPCPDU	M	Yes [ ]
MP3	Grants during discovery	64.3.6.1	Single grant in GATE message during discovery	OLT:M	Yes [ ]
MP4	Grant start time	64.3.6.1	Grants within one GATE MPCPDU are sorted by their Start time values	OLT:M	Yes [ ]
MP5	TX during synchronization	64.3.6.1	Transmit IDLE code groups	ONU:M	Yes [ ]
MP6	GATE generation	64.3.6.1	GATE generated for active ONU except during discovery	OLT:M	Yes [ ]
MP7	GATE LLID	64.3.6.1	Unicast LLID except for discovery	OLT:M	Yes [ ]
MP8	REPORT issuing	64.3.6.2	Issues REPORT periodically	ONU:M	Yes [ ]
MP9	REPORT generation	64.3.6.2	Generated by active ONU	ONU:M	Yes [ ]
MP10	REPORT LLID	64.3.6.2	REPORT has unicast LLID	ONU:M	Yes [ ]
MP11	REGISTER_REQ generation	64.3.6.3	Generated by undiscovered ONU	ONU:M	Yes [ ]
MP12	REGISTER_REQ LLID	64.3.6.3	Use broadcast LLID	ONU:M	Yes [ ]
MP13	REGISTER DA address	64.3.6.4	Use individual MAC address	OLT:M	Yes [ ]
MP14	REGISTER generation	64.3.6.4	Generated for all ONUs	OLT:M	Yes [ ]
MP15	REGISTER_ACK generation	64.3.6.5	Generated by active ONU	ONU:M	Yes [ ]
MP16	REGISTER_ACK LLID	64.3.6.5	Use unicast LLID	ONU:M	Yes [ ]

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65. Extensions of the Reconciliation Sublayer (RS) and Physical Coding Sublayer (PCS)/Physical Media Attachment (PMA) for 1000BASE-X for multipoint links and forward error correction

This clause describes functions for use in a 1000BASE-PX point-to-multipoint (P2MP) networks. This is an optical multipoint network that connects multiple DTEs using a single shared fiber. The architecture is asymmetrical, based on a tree and branch topology utilizing passive optical splitters. This type of network requires that the Multipoint MAC Control sublayer exists above the MACs, as described in Clause 64.

65.1 Extensions of the Reconciliation Sublayer (RS) for point-to-point emulation

65.1.1 Overview

This subclause extends Clause 35 to enable multiple data link layers to interface with a single Physical Layer. The number of MACs supported is limited only by the implementation. It is acceptable for only one MAC to be connected to this Reconciliation Sublayer. Figure 65–1 shows the relationship of this RS to the ISO/IEC OSI reference model. The mapping of GMII signals to PLS service primitives is described in 35.2.1.

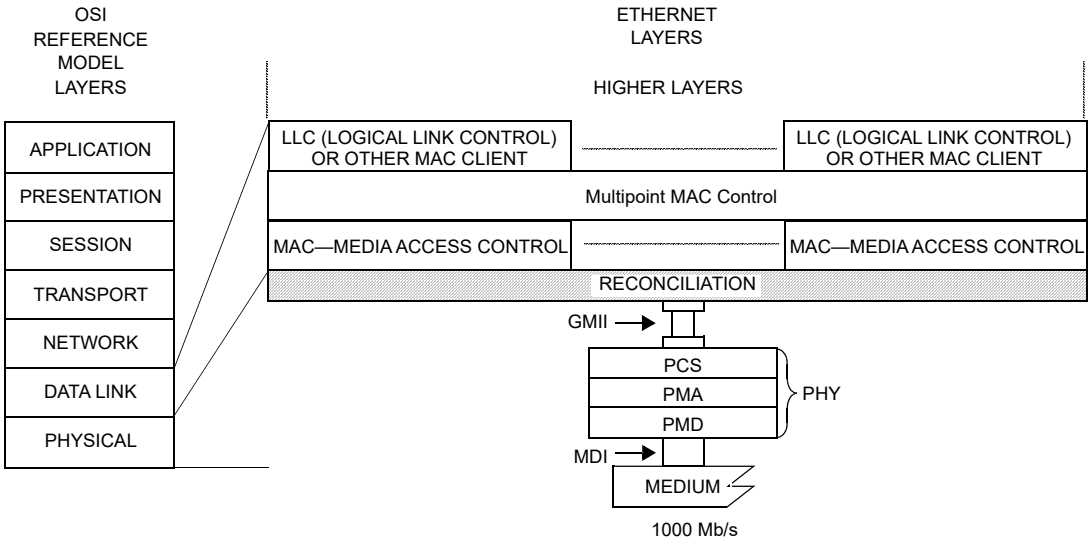

Figure 65–1—RS location in the OSI protocol stack

65.1.2 Principle of operation

A successful registration process, described in 64.3.3, results in the assignment of values to the MODE and LLID variables associated with a MAC. This may be one of many MACs in an Optical Line Terminal (OLT) or a single MAC in an Optical Network Unit (ONU). The MODE and LLID variables are used to identify a packet transmitted from that MAC and how received packets are directed to that MAC. The PCS of OLT shall operate in unidirectional mode as defined in 66.2.2.

As described in 64.1.2, multiple MACs within an OLT are bound to a single GMII, while at the ONU a single MAC is bound to the GMII. The multipoint control protocol (MPCP) ensures that only one MAC is transmitting at any one time. Correspondingly, only one PLS_DATA.request primitive is active at any time. The active PLS_DATA.request is mapped to the GMII signals, TXD<7:0>, TX_EN, TX_ER, and

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GTX_CLK. The RS replaces octets of preamble with the values of the transmitting MAC's MODE and LLID variables.

In the receive direction, these MODE and LLID values, embedded within the preamble, identify the MAC to which this frame should be directed. The RS establishes a temporal mapping of the GMII signals, RXD<7:0>, RX_ER, RX_CLK, and RX_DV, to the correct PLS_DATA.indication and PLS_DATA_VALID.indication primitives.

65.1.3 Functional specifications

The variables below provide a mapping between MODE and LLID variables and multiple MACs. While the usage of this mapping is less interesting in the ONU, it is critical in the OLT. This mapping is used to replace transmitted preambles with MODE and LLID fields as well as to steer received packets to the appropriate MAC.

65.1.3.1 Variables

enable
: Value: Boolean
: This variable shall be TRUE for an ONU MAC. For an OLT MAC, this variable is defined as below:
: TRUE when management has assigned a value to mode and logical_link_id. Indicates the MAC is enabled to receive frames.
: FALSE when the MAC is not in use.

mode
: Value: 1 bit
: This variable shall be 0 for an ONU MAC and may be 0 or 1 for an OLT MAC.
: When the LLID is used to emulate a single copy broadcast or multicast channel, this variable will be set to 1. When emulating a unicast channel, this variable will be set to 0.

logical_link_id
: Value: 15 bits
: This variable shall be set to the broadcast value of 0x7FFF for the unregistered ONU MAC.
: Enabled OLT MACs may use any value for this variable. If the optional multicast LLID feature is supported, the OLT may use a multicast_link_id along with the mode bit 0.
: Registered ONU MACs may use any value other than 0x7FFF or a multicast_link_id for this variable.

multicast_link_id
: Value: 15 bits
: Enabled OLT MACs that support the optional multicast LLID feature may use any value for this variable. This variable is used, along with a mode bit reset to 0, to derive the multicast LLID.

65.1.3.2 Transmit

The transmit function of this extended RS replaces some of the octets of the preamble as transmitted by the MAC with several fields: SLD (start of LLID delimiter), LLID and CRC8. The SLD field is used by the receiver function to locate the LLID and CRC8 fields. The LLID field identifies the source or destination MAC. The CRC8 field provides a level of integrity on the LLID field. Table 65–1 shows the replacement mapping.

Table 65–1—Preamble/SFD replacement mapping

Offset	Field	Preamble/SFD	Modified preamble/SFD
1	—	0x55	same
2	—	0x55	same
3	SLD	0x55	0xD5
4	—	0x55	same
5	—	0x55	same
6	LLID[15:8]	0x55	<mode, logical_link_id[14:8]>[a]

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Table 65–1—Preamble/SFD replacement mapping *(continued)*

Offset	Field	Preamble/SFD	Modified preamble/SFD
7	LLID[7:0]	0x55	<logical_link_id[7:0]>[b]
8	CRC8	0xD5	The 8-bit CRC calculated over offsets 3 through 7

[a]mode maps to TXD[7], logical_link_id[14] maps to TXD[6], logical_link_id[8] maps to TXD[0]
[b]logical_link_id[7] maps to TXD[7], logical_link_id[0] maps to TXD[0]

65.1.3.2.1 SLD

The SLD field is one octet in length and replaces the third octet of the preamble.

NOTE—The 1000BASE-X PCS transmit function replaces the first octet of preamble with the /S/ code-group or it discards the first octet and replaces the second octet of preamble with the /S/ code-group. This decision is based upon the even or odd alignment of the PCS's transmit state diagram (see Figure 36–5). The 1000BASE-X PCS receive function replaces the /S/ code-group with an octet of preamble. The third octet of preamble is the first octet passed through the 1000BASE-X PHY without modification.

65.1.3.2.2 LLID

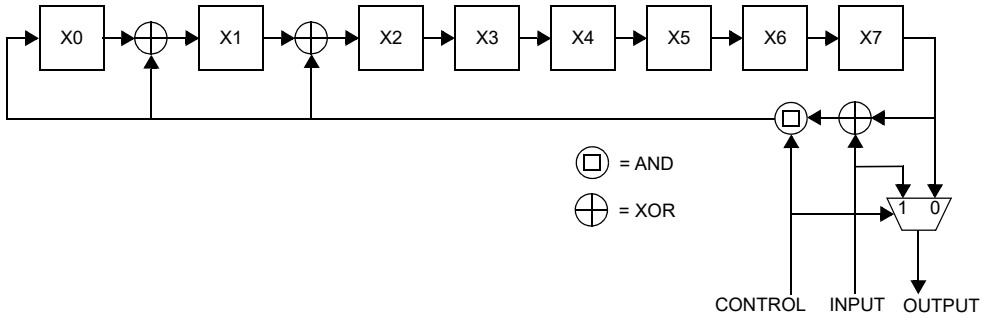
The LLID field is two octets in length and replaces the last two octets of preamble. The LLID field is a concatenation of the mode and logical_link_id variables for the associated MAC.

65.1.3.2.3 CRC-8

The CRC8 field contains an 8-bit cyclic redundancy check value. This value is computed as a function of the contents of the modified preamble beginning with the SLD field (offset 3) through the LLID field (offset 7). The encoding is defined by the generating polynomial shown in Equation (65–1):

$$G(x) = x^8 + x^2 + x + 1 \tag{65–1}$$

This CRC calculation shall produce the same result as the serial implementation shown in Figure 65–2. Before calculation begins, the shift register shall be initialized to the value 0x00. The content of the shift register is transmitted without inversion.



CONTROL = 1 when shifting the modified preamble and calculating the CRC
CONTROL = 0 when transmitting the CRC8 field

Figure 65–2—CRC8 field generation

65.1.3.3 Receive function

The receive function of this extended RS is responsible for the following functions:

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a) Locate the SLD field.
b) Use the location of the SLD field to locate the CRC8 field and verify that the received value matches the CRC calculated using the received data.
c) Use the location of the SLD field to locate the LLID field and parse it to determine the destination MAC.
d) If the packet is not discarded due to incorrect CRC or unknown LLID, then replace the SLD and LLID fields with normal preamble and the CRC8 field with the SFD and transfer the packet to the appropriate MAC.
e) Otherwise, discard the entire packet, replacing it with normal inter-frame.

Table 65–2 shows the mapping of the modified preamble/SFD to RXD.

Table 65–2—Preamble/SFD replacement mapping

Signal	Bit values of octets received through GMII[a]									
RXD0	X	1[b]	1	1[c]	1	1	logical_link_id[8][d]	logical_link_id[0][e]	X7[f]	D0[g]
RXD1	X	0	0	0	0	0	logical_link_id[9]	logical_link_id[1]	X6	D1
RXD2	X	1	1	1	1	1	logical_link_id[10]	logical_link_id[2]	X5	D2
RXD3	X	0	0	0	0	0	logical_link_id[11]	logical_link_id[3]	X4	D3
RXD4	X	1	1	1	1	1	logical_link_id[12]	logical_link_id[4]	X3	D4
RXD5	X	0	0	0	0	0	logical_link_id[13]	logical_link_id[5]	X2	D5
RXD6	X	1	1	1	1	1	logical_link_id[14]	logical_link_id[6]	X1	D6
RXD7	X	0	0	1	0	0	mode	logical_link_id[7]	X0	D7
RX_DV	0	1	1	1	1	1	1	1	1	1

[a]Leftmost octet is the first received
[b]This octet may be missing per 1000BASE-X PCS transmit state diagram (see Figure 36–5)
[c]SLD field
[d]First octet of LLID field
[e]Second octet of LLID field
[f]CRC8 field
[g]D0 through D7 is the first octet of the PDU (first octet of the Destination Address)

65.1.3.3.1 SLD

Recall that the 1000BASE-X transmit function has to maintain an even alignment for its Start_of_Packet delimiters. It may replace the first octet of preamble with the /S/ code-group and pass the second octet unchanged or it may discard the first octet of preamble and replace the second octet of preamble with the /S/ code-group. The SLD is transmitted in the third octet. These are the only two possibilities considered when parsing the incoming octet stream for the SLD. If the SLD field is not found then the packet shall be discarded. If the packet is transferred, the SLD shall be replaced with a normal preamble octet and the one or two octets preceding the SLD and the two octets following the SLD are passed without modification.

65.1.3.3.2 LLID

The third and fourth octets following the SLD contain the mode and logical_link_id values. These values are acted upon differently for OLTs and ONUs.

If the device is an OLT then the following comparison is made:

a) The received mode bit is ignored.
b) If the received logical_link_id value matches 0x7FFF and an enabled MAC exists with a logical_link_id variable with the same value then the comparison is considered a match to that MAC.

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c) If the received logical_link_id value is any value other than 0x7FFF and an enabled MAC exists with a mode variable with a value of 0 and a logical_link_id variable with a value matching the received logical_link_id value then the comparison is considered a match to that MAC.

If the device is an ONU then the following comparison is made:

d) If the received mode bit is 0 and the received logical_link_id value matches the logical_link_id variable then the comparison is considered a match.
e) If the received mode bit is 1 and the received logical_link_id value does not match the logical_link_id variable, or the received logical_link_id matches 0x7FFF, then the comparison is considered a match.
f) If the device supports the multicast LLID feature, the received mode bit is 0 and the received logical_link_id value matches an assigned multicast_link_id, then the comparison is considered a match.

If no match is found, then the packet shall be discarded within the RS. If a match is found, then the packet is intended to be transferred. If the packet is transferred, then both octets of the LLID field shall be replaced with normal preamble octets.

65.1.3.3.3 CRC-8

The octet following the LLID field contains the CRC8 field. The value of this field is compared against the calculated CRC of the received octets, beginning with the SLD field and ending with the last octet of the LLID field. If the received and calculated CRC values do not match, then the packet shall be discarded. If the values match then the packet is transferred. If the packet is transferred, then the CRC8 field shall be replaced with the SFD.

65.2 Extensions of the physical coding sublayer for data detection and forward error correction

65.2.1 Overview

This subclause extends the physical coding sublayer Clause 36 to support burst mode operation of the point-to-multipoint physical medium. This subclause also specifies an optional forward error correction (FEC) mechanism to increase the optical link budget or the fiber distance. Figure 65–3 shows the relationship between the extended PCS sublayer and the ISO/IEC OSI reference model. Auto-Negotiation, as defined in Clause 37, establishes a point-to-point handshaking mechanism for allowing 1000BASE-X devices to achieve a highest common denominator link. The P2MP aspect of a 1000BASE-PX network prohibits the use of the auto-negotiation protocol.

NOTE—Many implementations of the transmit and receive buffers might be dependent on the maximum length of frame supported. It is recommended that these frame buffers should be sized to accommodate maximum length envelope frames (see 3.2.7). It is also recommended that the FEC function should accommodate maximum length envelope frames, requiring up to 9 FEC code blocks per frame.

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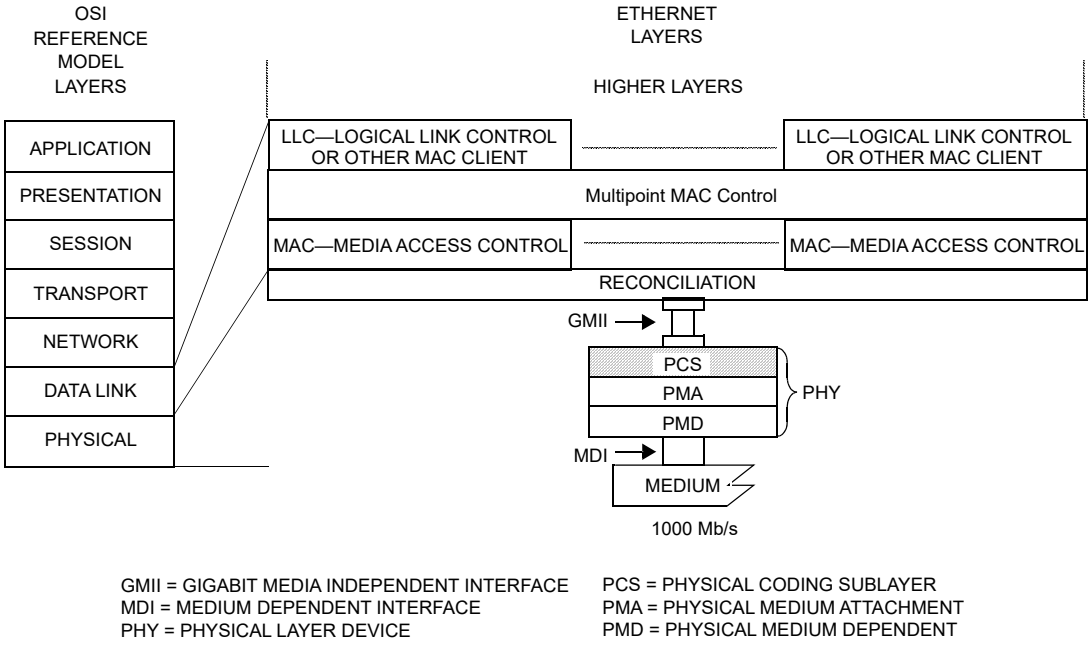

Figure 65–3—PCS location in the OSI protocol stack

65.2.2 Burst-mode operation

To avoid spontaneous emission noise from near ONUs obscuring signal from a distant ONU, the ONUs' lasers should be turned off between their transmissions. To control the laser, the PCS is extended to detect the presence of transmitted data and generate the PMD_SIGNAL.request(tx_enable) primitive to turn the laser on and off at the correct times. This function is performed by the Data Detector shown in the functional block diagram in Figure 65–4.

65.2.2.1 Principle of operation

The Data Detector contains a delay line (FIFO buffer) storing code-groups to be transmitted. The length of the FIFO buffer shall be chosen such that the delay introduced by the buffer together with any delay introduced by the PMA sublayer is long enough to turn the laser on and to allow a predefined number of idle characters to be transmitted. This number of idle characters is needed by the receiver to adjust its gain ($T_{receiver\_settling}$), synchronize its receiving clock (T_{CDR}), and complete the synchronization process (T_{sync}).

Upon initialization, the FIFO buffer is filled with /I/ ordered sets and the laser is turned off. When the first code-group that is not /I/ arrives at the buffer, the Data Detector sets the PMD_SIGNAL.request(tx_enable) primitive to the value ON, instructing the PMD sublayer to start the process of turning the laser on (see Figure 65–4).

When the buffer empties of data (i.e., contains only /I/ ordered sets), the Data Detector sets the PMD_SIGNAL.request(tx_enable) primitive to the value OFF, instructing the PMD sublayer to start the process of turning the laser off. Between packets, /I/ or /R/ ordered sets will arrive at the buffer. If the number of these /I/ or /R/ ordered sets is insufficient to fill the buffer then the laser is not turned off.

Figure 65–5 shows the relationship of filling the buffer and the generation of laser_control. In the OLT, the laser always remains turned on. Correspondingly, therefore the OLT's Data Detector does not need a delay line or buffer in the data path for this purpose.

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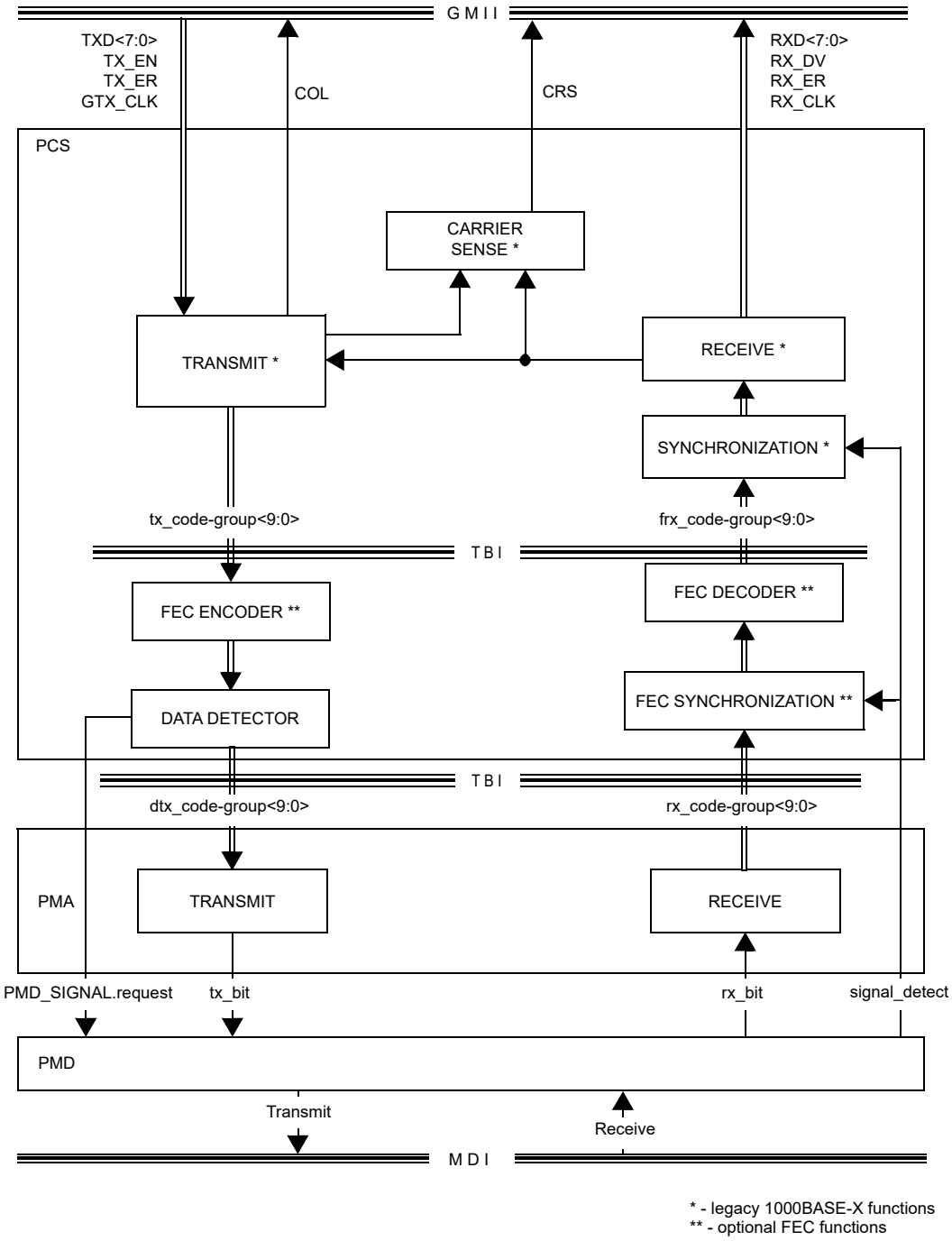

Figure 65–4—PCS Extension functional block diagram

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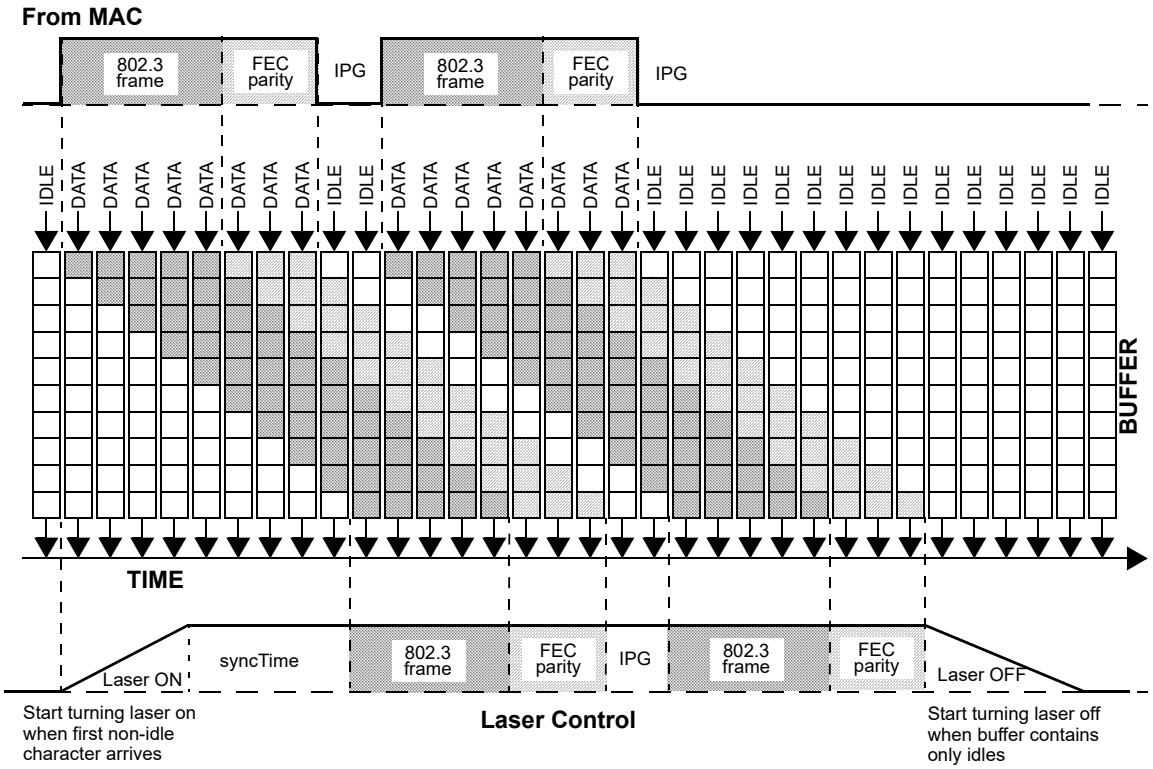

Figure 65–5—Laser control as a function of buffer fill

65.2.2.2 Detailed functions and state diagrams

The body of this clause comprises state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams in this clause follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

65.2.2.2.1 Variables

BEGIN

TYPE: Boolean

This variable is used when initiating operation of the state diagram. It is set to true following initialization and every reset.

DelayBound

TYPE: 16-bit unsigned

DEFAULT VALUE: 00-6A (106 code-groups = 848 ns)

This represents the delay sufficient to initiate the laser and to stabilize the receiver at the OLT. The default value of DelayBound is based on default values of laserOnTime (64.3.5.1) and SyncTime (64.3.3.2). This variable is only used by the ONU.

dtx_code-group

A 10-bit vector representing one code-group, as specified in Tables 36–1a through 36–2, which has been prepared for transmission by the Data Detector process. This vector is conveyed to

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the PMA as the parameter of a PMA_UNITDATA.request(dtx_code-group) service primitive. The element dtx_code-group<0> is the first bit transmitted and dtx_code-group<9> is the last bit transmitted.

laser_control

This variable represents the status of the laser. The value on corresponds to the laser being turned on, and the value off corresponds to laser being off.

TYPE: Boolean.

tx_code-group

A 10-bit vector of bits representing one code-group, as specified in Table 36–1a–e or Table 36–2, which has been prepared for transmission by the PCS Transmit process. The element tx_code-group<0> is the first tx_bit transmitted; tx_code-group<9> is the last tx_bit transmitted.

65.2.2.2.2 Functions

IsIdle(tx_code-group)

This function is used to determine whether tx_code-group is a code-group in /I/, the IDLE ordered set, or /C/, the Configuration ordered set. This function returns true if tx_code-group is /K28.5/ or any code-group that follows a /K28.5/ or any two consecutive /D/ code-groups that follow /K28.5/D21.5/ or /K28.5/D2.2/. Otherwise, the IsIdle function returns false.

FIFO.RemoveHead()

This function removes the first code-group from the FIFO buffer and advances all remaining code-groups one position ahead. This function returns the 10-bit vector representing the removed code-group.

FIFO.Append(tx_code-group)

This function appends a new 10-bit vector to the end of the FIFO buffer.

65.2.2.2.3 Messages

PMD_SIGNAL.request(tx_enable)

This primitive is used to turn the laser on and off at the PMD sublayer. In the OLT, this primitive shall always take the value ON. In the ONU, the value of this variable is controlled by the Data detector state diagram (see Figure 65–6).

PUDR

Alias for PMA_UNITDATA.request(tx_code-group<9:0>).

65.2.2.2.4 Counters

IdleLength

This counter represents the length of the consecutive interval of idles ending with the most recent tx_code-group. If the most recent tx_code-group represents a non-idle character, the IdleLength is reset to 0.

TYPE: 32-bit unsigned

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65.2.2.3 State diagrams

The Data Detector shall be implemented for an ONU as depicted in Figure 65–6, including compliance with the associated state variables as specified in 65.2.2.2.

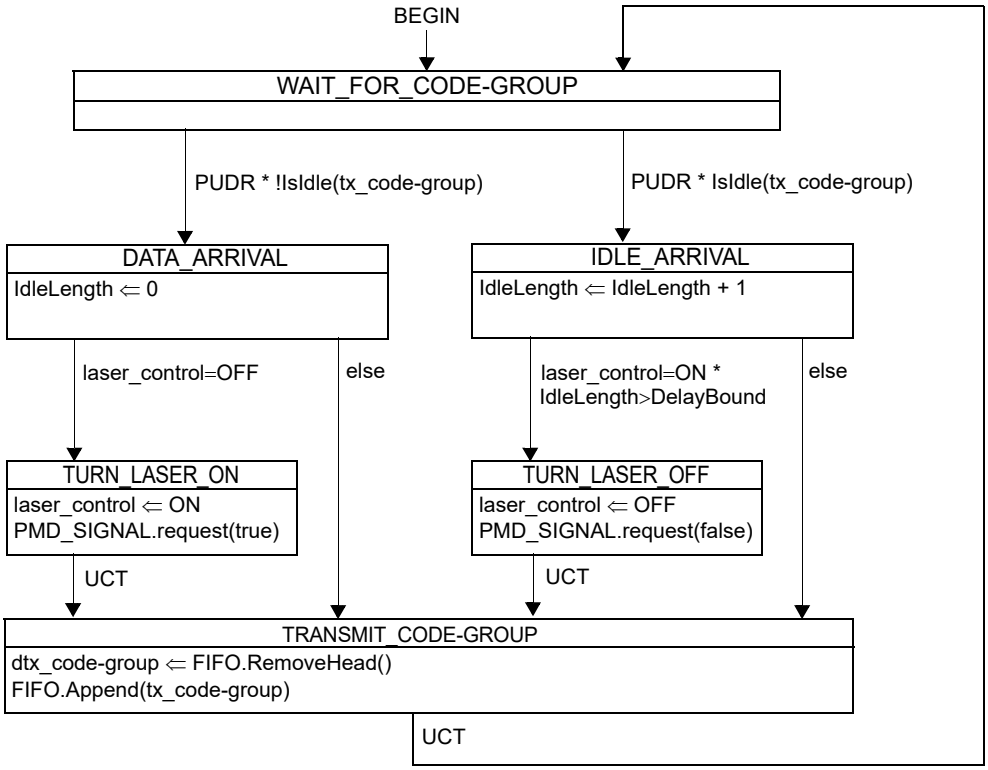

Figure 65–6—ONU data decoder state diagram

65.2.3 Forward error correction

This subclause specifies an optional forward error correction (FEC) mechanism to increase the optical link budget or the fiber distance. The FEC appends to the Ethernet frame additional data that is a result of a set of non-binary arithmetic functions (known as Galois arithmetic) performed on the data of the Ethernet frame. This additional data (known as the FEC parity octets) is used to correct errors at the receiving end of the link that may occur when the data is transferred through the link.

The FEC function comprises three functional blocks: FEC Encoder, FEC Decoder, and FEC Synchronization, as shown in Figure 65–4. These blocks have ten-bit interfaces (TBIs) to both sides and can be omitted for implementations not requiring FEC. Though the FEC functionality is optional, if implemented for operation over a multipoint optical link, it shall behave as specified in 65.2.3.

The following are the objectives of FEC:

a) Keep frame format compliant to 1000BASE-X PCS.
b) Support optional functionality.
c) Allow backwards compatibility with legacy 1000BASE-X devices.
d) Support BER objective of 10^{-12} at PCS.
e) Support BER objective of 10^{-4} at FEC sublayer.

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65.2.3.1 FEC code

The FEC code specification, properties and performance analysis are specified in ITU-T G.975.

The FEC code used is a linear cyclic block code - the Reed-Solomon code (255,239,8) over the Galois Field of GF(2^8) - a non-binary code operating on 8-bit symbols. The code encodes 239 information symbols and adds 16 parity symbols. The code is systematic—meaning that the information symbols are not disturbed in any way in the encoder and the parity symbols are added separately to each block.

The code is the systematic form of the RS code based on the generating polynomial $G(x) = \prod_{i=0}^{15}(x - \alpha^i)$

where α is equal to 0x02 and is a root of the binary primitive polynomial $x^8+x^4+x^3+x^2+1$.

A codeword of the systematic code is presented by $D(x) + P(x) = G(x) * L(x)$ where:

$D(x)$ is the data vector – $D(x)=D_{238}X^{254} + ... + D_0X^{16}$. D_{238} is the first data octet and D_0 is the last.

$P(x)$ is the parity vector – $P(x)=P_{15}X^{15} + ... + P_0$. P_{15} is the first parity octet and P_0 is the last.

A data octet (d_7, d_6, ..., d_1, d_0) is identified with the element: $d_7*\alpha^7 + d_6*\alpha^6 + ... d_1*\alpha^1 + d_0$ in GF(2^8), the finite field with 2^8 elements. The code has a correction capability of up to eight symbols.

NOTE—For the (255,239,8) Reed-Solomon code, the symbol size equals one octet. d_0 is identified as the LSB and d_7 is identified as the MSB bit in accordance with the conventions of 3.1.1.

The FEC decoder shall replace all octets in an uncorrectable block with /V/ to clearly propagate the error condition to the PCS.

65.2.3.2 FEC frame format

The frame format of an FEC coded Ethernet frame is herein described.

65.2.3.2.1 Placing parity octets

Ethernet packets are received from the PCS. The data is partitioned into 239-symbol frames (blocks), with the first block beginning with the first symbol after the /S/ code-group and the last block ending with the last symbol before the /T/ code-group. Each block is encoded using the (255,239,8) Reed-Solomon encoder, which results in an additional 16 parity symbols for each block. The block plus the associated 16 parity symbols form the 255 symbol Reed-Solomon codeword. The additional 16 parity symbols, which are generated from this encoding process for each block, are gathered and added at the end of the packet.

65.2.3.2.2 Shortened last block

When dividing the data into blocks there might be a case where the last block is shorter than 239 symbols. This block is noted as a shortened block. A shortened block of length r octets results in the data vector assignment of D_{238} to D_r as zeros and D_{r-1} to D_0 as valid data, where D_{r-1} is the first octet of the shortened block and D_0 is the last. This full size block is then encoded and the 16 parity symbols are generated. The data is then sent without the zero symbols. At the receiver, the decoder completes the block again into the full block (by adding back the zeros) for decoding.

65.2.3.2.3 Special frame markers

The Ethernet frame consists of a number of blocks plus special frame start and stop markers. In order to decode the FEC code, the receiver first has to synchronize on the Ethernet frame. The Ethernet frame

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markers are not protected by the FEC code and are exposed to higher BER. Therefore, special start and stop marker symbols are added at the beginning and the end of the FEC coded frame that are capable of being correctly detected in a high noise environment. The special symbol noise immunity is made possible by the implementation of a simple correlator. The marker framing sequences used are at least 5 octets long, long enough to be detected with very high probability. The start FEC framing sequence is denoted by /S_FEC/ and the end FEC framing sequence is denoted by /T_FEC/.

In order to determine that an FEC coded frame has started, the input symbol stream is scanned for a match with the /S_FEC/ ordered set with fewer than d/2 errors. In order to determine that an FEC coded frame has ended, the input symbol stream is scanned for a match with the /T_FEC_O/ or /T_FEC_E/ ordered sets with fewer than d/2 errors.

The value chosen for d is 10, the number of bits that are different between these ordered sets and any other regularly occurring five consecutive code-groups when considered in the 10-bit domain.

The sequence can flow through non-FEC PCS transparently (in a False_Carrier_Sense mode).

The start and end symbols are constructed from 8B/10B code-groups:

— /S_FEC/ - start of FEC coded packet - /K28.5/D6.4/K28.5/D6.4/S/
— /T_FEC_E/ - end of FEC coded packet with even alignment. If the starting running disparity is positive, the /T_FEC_E/ has the following pattern: /T/R/K28.5/D10.1/T/R/. If the starting running disparity is negative, the T_FEC_E has the following pattern: /T/R/K28.5/D29.5/T/R/.
— /T_FEC_O/ - end of FEC coded packet with odd alignment - /T/R/R/I/T/R/

/S/, /T/, /R/ and /I/ are described in Table 36–3. The /I/ in both the /T_FEC_E/ and the /T_FEC_O/ ordered sets can be either an /I1/ (a disparity correcting IDLE) or an /I2/ (a disparity preserving IDLE).

Figure 65–7 describes the FEC coded Ethernet frame. Between the FCS and PARITY fields, the T_FEC can be either the /T_FEC_E/ or the /T_FEC_O/ ordered set. After the PARITY field, the T_FEC can only be a /T_FEC_E/ ordered set.



Figure 65–7—FEC coded Ethernet frame

65.2.3.3 FEC sublayer operation

This section describes the functionality and operation of the FEC sublayer.

65.2.3.3.1 Principles of operation

At transmission, the FEC sublayer receives the packets from the PCS, performs the FEC coding, appends the parity octets in place of the stretched IPG and sends the data to the PMA. At reception, the FEC sublayer receives the data from the PMA, performs the octet alignment, detects the Start FEC Framing Sequence, decodes the FEC code, correcting data where necessary and possible, replaces the parity octets with IDLE and sends the data to the PCS.

NOTE—To ensure correct MPCP operation, the FEC function maintains constant and equal delay for all code-groups and all signals transmitted from PMA to PCS. Timing effects of adding FEC function should be indistinguishable from an increased propagation delay.

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65.2.3.3.2 Functional block diagram

As depicted in Figure 65–4, the FEC sublayer comprises a transmit side and a receive side. The following sections define the functionality of each block in the sublayer. See 36.3.3 for a complete description of the TBI.

65.2.3.3.3 Transmission

Figure 65–8 describes a block diagram of the FEC sublayer transmit data path. The packet delimiters of the packets from the PCS are detected. The /I/I/S/ is replaced with the /S_FEC/ ordered set. The data in the frame is then 8B/10B decoded so that the FEC coding can take place and the parity octets buffered. The /T/R/I/I/ or /T/R/R/I/I/ is detected and replaced with the /T_FEC_E/ or /T_FEC_O/, respectively. Then the parity octets and another /T_FEC_E/ is appended, replacing the stretched interframe spacing.

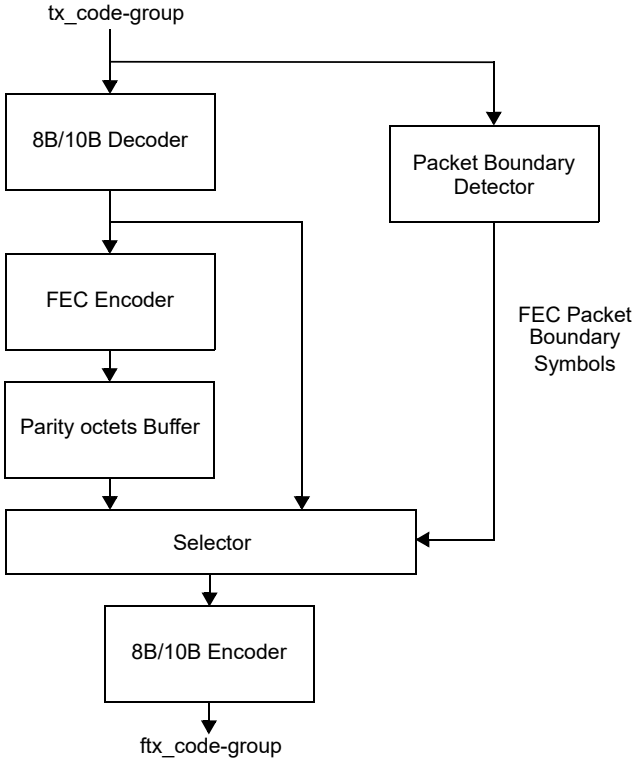

Figure 65–8—Transmit block diagram

The FEC Transmit process continually generates code-groups based upon information provided in the PMA_UNITDATA.request primitive with the tx_code-group<9:0> parameter, sending them immediately to the PMA Service Interface via the same primitive with the ftx_code-group<9:0> parameter.

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65.2.3.3.4 Reception

Figure 65–9 describes the receive synchronization block diagram of the FEC sublayer receive data path. The FEC Synchronization process continually accepts code-groups via the PMA_UNITDATA.indication service primitive and conveys received code-groups to the FEC Receive process via the SYNC_UNITDATA.indicate service primitive. The FEC Synchronization process sets the sync_status flag to indicate whether the PMA is functioning dependably (as well as can be determined without exhaustive error-ratio analysis).

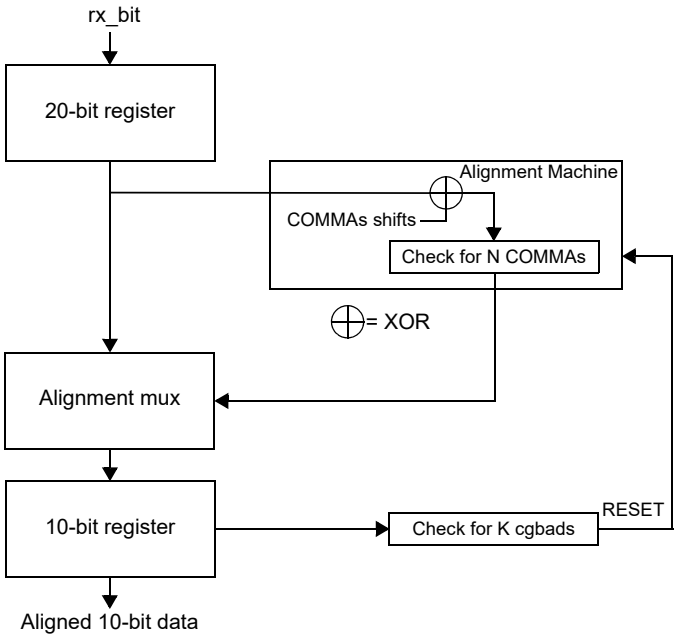

Figure 65–9—Receive synchronization block diagram

Figure 65–10 describes a block diagram of the FEC sublayer receive data path. The FEC Receive process continuously accepts code-groups via the SYNC_UNITDATA.indicate service primitive. It fills a buffer with these code-groups, converting an /S_FEC/ with fewer than d/2 errors to /I/I/S/ and converting all /T_FEC/ with fewer than d/2 errors to a clean /T_FEC/. This buffer exists in order to store all necessary data until the parity octets are available for performing data correction. Data correction is performed within the buffer. While emptying the buffer, the parity octets, along with the latter /T/R/ of the first /T_FEC/ and the entire second /T_FEC/ are converted to /I/.

NOTE—Under specific conditions, the PCS may generate a large number of FALSE_CARRIER events. FEC encryption only protects Ethernet frames. The IDLEs are not FEC-protected. During idle periods, excessive bit errors may results in FALSE_CARRIER events. Additionally, when FEC and non-FEC devices are combined in the same EPON, a non-FEC device will treat FEC parity data as FALSE_CARRIER events.

65.2.3.4 Detailed functions and state diagrams

The body of this clause comprises state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams in this clause follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

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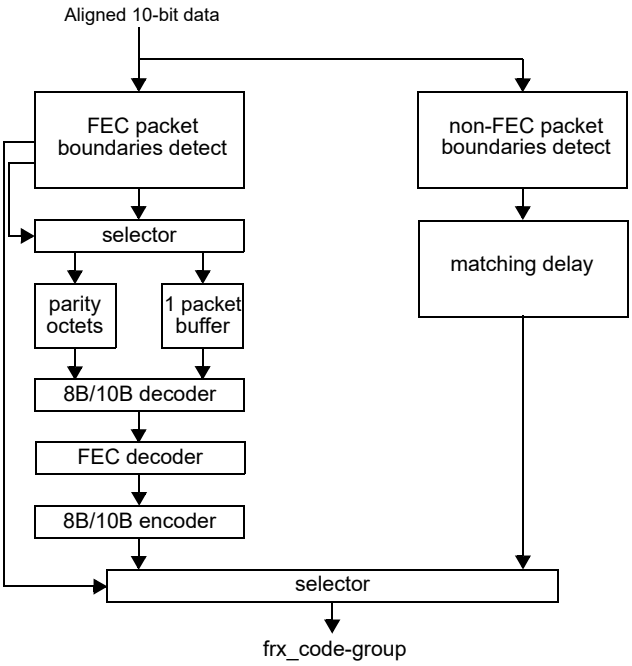

Figure 65–10—Receive data block diagram

65.2.3.4.1 State variables

65.2.3.4.2 Notation conventions

/x/

Denotes the constant code-group specified in 36.2.5.1.2 (valid code-groups have to follow the rules of running disparity as per 36.2.4.5 and 36.2.4.6).

[/x/]

Denotes the latched received value of the constant code-group (/x/) specified in 36.2.5.1.2 and conveyed by the SYNC_UNITDATA.indicate message described in 36.2.5.1.6.

65.2.3.4.3 Constants

/COMMA/

The set of special code-groups that include a comma as specified in 36.2.4.9 and listed in Table 36–2.

/D/

The set of 256 code-groups corresponding to valid data, as specified in 36.2.4.11.

/Dx.y/

One of the set of 256 code-groups corresponding to valid data, as specified in 36.2.4.11.

/I/

The IDLE ordered set group, comprising either the /I1/ or /I2/ ordered sets, as specified in 36.2.4.12.

/INVALID/

The set of invalid data or special code-groups, as specified in 36.2.4.6.

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/Kx.y/
: One of the set of 12 code-groups corresponding to valid special code-groups, as specified in Table 36–2.

/R/
: The code-group used as either: End_of_Packet delimiter part 2; End_of_Packet delimiter part 3; Carrier_Extend; and /I/ alignment.

/S/
: The code-group corresponding to the Start_of_Packet delimiter (SPD) as specified in 36.2.4.14.

/T/
: The code-group used for the End_of_Packet delimiter part 1.

/V/
: The Error_Propagation code-group, as specified in 36.2.4.17.

65.2.3.4.4 Variables

buffer
: The Receive process buffer of undefined length containing code-groups.

buffer_head
: The code-group at the head of the Receive process buffer.

cgbad
: Alias for the following terms: ((rx_code-group∈/INVALID/) + (rx_code-group=/COMMA/ *rx_even=TRUE)) * PMA_UNITDATA.indication

cggood
: Alias for the following terms: !((rx_code-group∈/INVALID/) + (rx_code-group=/COMMA/ *rx_even=TRUE)) * PMA_UNITDATA.indication

fec_encode
: A Boolean set by the FEC Transmit process to indicate the status of the RS_Encode(Data) function.

  Values: TRUE; data is acted upon by the RS_Encode(Data) function.
  FALSE; data is not being acted upon by the RS_Encode(Data) function.

ftx_bit
: A binary parameter used to convey data from the PMA to the PMD via the PMD_UNITDATA.request service primitive as specified in 60.1.5.1.

  Values: ZERO; Data bit is a logical zero.
  ONE; Data bit is a logical one.

ftx_code-group<9:0>
: A vector of bits representing one code-group, as specified in Table 36–1a through Table 36–2, which has been prepared for transmission by the FEC Transmit process. This vector is conveyed to the PMA as the parameter of a PMA_UNITDATA.request(ftx_code-group) service primitive. The element ftx_code-group<0> is the first ftx_bit transmitted; ftx_code-group<9> is the last ftx_bit transmitted.

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parity<D7:D0>

An 8-bit array that contains the current parity bits to be encoded in the FEC Transmit Process. The elements within the array are updated with the next 8-bits to be encoded upon each entry into the XMIT_PARITY state.

Values for each element in the array: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

parity_buffer_empty

A Boolean set by the FEC Transmit process to indicate if more parity octets need to be encoded.

Values: TRUE; No more parity octets need to be encoded.
FALSE; More parity octets need to be encoded.

rx_disparity

A Boolean set by the FEC Receive process to indicate the running disparity at the end of code-group reception as a binary value. Running disparity is described in 36.2.4.3.

Values: POSITIVE
NEGATIVE

rx_even

A Boolean set by the FEC Synchronization process to designate received code-groups as either even- or odd-numbered code-groups as specified in 36.2.4.2.

Values: TRUE; Even-numbered code-group being received.
FALSE; Odd-numbered code-group being received.

rx_code-group<9:0>

A 10-bit vector represented by the most recently received code-group from the PMA. The element rx_code-group<0> is the least recently received (oldest) rx_bit; rx_code-group<9> is the most recently received rx_bit (newest). When code-group alignment has been achieved, this vector contains precisely one code-group.

signal_detect

A Boolean set by the PMD continuously via the PMD_SIGNAL.indication(signal_detect) message to indicate the status of the incoming link signal.

Values: FAIL; A signal is not present on the link.
OK; A signal is present on the link.

sync_status

A parameter set by the FEC Synchronization process to reflect the status of the link as viewed by the receiver.

Values: FAIL; The receiver is not synchronized to code-group boundaries.
OK; The receiver is synchronized to code-group boundaries.

tx_bit

A binary parameter used to convey data from the PMA to the PMD via the PMD_UNITDATA.request service primitive as specified in 60.1.5.1.

Values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

tx_code-group<9:0>

A vector of bits representing one code-group, as specified in Table 36–1a–e or Table 36–2, which has been prepared for transmission by the PCS Transmit process. This vector is conveyed to the PMA as the parameter of a PMD_UNITDATA.request(tx_bit) service

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primitive. The element tx_code-group<0> is the first tx_bit transmitted; tx_code-group<9> is the last tx_bit transmitted.

tx_disparity
: A Boolean set by the FEC Transmit process to indicate the running disparity at the end of code-group transmission as a binary value. Running disparity is described in 36.2.4.3.

  Values: POSITIVE
  NEGATIVE

65.2.3.4.5 Functions

check_ahead_tx
: Prescient function used by the FEC Transmit process to find the Start_of_Packet in order to replace the Start_of_Packet and its two preceding IDLE ordered sets with /S_FEC/.

check_ahead_rx
: Prescient function used by the FEC Receive process to find the /S_FEC/ and /T_FEC/, with fewer than d/2 errors.

DECODE ([/x/])
: In the PCS Receive process, this function takes as its argument the latched value of rx_code-group<9:0> ([/x/]) and the current running disparity, and returns the corresponding GMII RXD<7:0>, rx_Config_Reg<D7:D0>, or rx_Config_Reg<D15:D8> octet, per Table 36–1a–e. DECODE also updates the current running disparity per the running disparity rules outlined in 36.2.4.4.

ENCODE(x)
: In the PCS Transmit process, this function takes as its argument (x), where x is a GMII TXD<7:0>, tx_Config_Reg<D7:D0>, or tx_Config_Reg<D15:D8> octet, and the current running disparity, and returns the corresponding ten-bit code-group per Table 36–1a–e. ENCODE also updates the current running disparity per Table 36–1a–e.

POP_BUFFER
: Removes the octet at the head of the Receive process buffer, making the next octet available.

RS_Encode(Data)
: This function is used to encode the Reed-Solomon (255,239,8) code. The encoder encodes the 239 octets data frame and generates 16 parity octets for each data frame. Before being passed to the Reed-Solomon encoder, this function passes the data through DECODE([/x/]).

RS_Decode(Data)
: This function is used to decode the Reed-Solomon (255,239,8) code. The decoder decodes the 255 symbols data frame and generates 239 corrected data octets for each frame and an error signal.

signal_detectCHANGE
: In the PCS Synchronization process, this function monitors the signal_detect variable for a state change. The function is set upon state change detection.

  Values: TRUE; A signal_detect variable state change has been detected.
  FALSE; A signal_detect variable state change has not been detected (default).

65.2.3.4.6 Counters

good_cgs
: Count of consecutive valid code-groups received.

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loop_count
: A 3-bit counter used to keep track of the number of loops in the receive synchronization process.

65.2.3.4.7 Messages

FEC_UNITDATA.indicate(frx_code-group<9:0>)
: A signal sent by the FEC Receive process conveying the next code-group received over the medium.

FUDI
: Alias for FEC_UNITDATA.indicate(frx_code-group<9:0>).

PMA_UNITDATA.indication(rx_code-group<9:0>)
: A signal sent by the PMA Receive process conveying the next code-group received over the medium (see 36.3.1.2).

PMA_UNITDATA.request(tx_code-group<9:0>)
: A signal sent to the PMA or FEC Transmit process conveying the next code-group ready for transmission over the medium (see 36.3.1.1).

PUDI
: Alias for PMA_UNITDATA.indication(rx_code-group<9:0>).

PUDR
: Alias for PMA_UNITDATA.request(tx_code-group<9:0>).

SUDI
: Alias for SYNC_UNITDATA.indicate(parameters).

SYNC_UNITDATA.indicate(parameters)
: A signal sent by the FEC Synchronization process to the FEC Receive process conveying the following parameters:

  Parameters: [/x/]; the latched value of the indicated code-group (/x/);
  EVEN/ODD; The latched state of the rx_even variable;

  Value: EVEN; Passed when the latched state of rx_even=TRUE.
  ODD; Passed when the latched state of rx_even=FALSE.

65.2.3.5 State diagrams

65.2.3.5.1 Transmit state diagram

The FEC shall implement its transmit process as depicted in Figure 65–11, including compliance with the associated state variables as specified in 65.2.3.4.1.

65.2.3.5.2 Receive synchronization state diagram

The FEC shall implement its synchronization process as depicted in Figure 65–12, including compliance with the associated state variables in 65.2.3.4.1.

65.2.3.5.3 Receive state diagram

The FEC shall implement its receive process as depicted in Figure 65–13 and Figure 65–14, including compliance with the associated state variables in 65.2.3.4.1.

It is expected that the FEC decoding is performed while the data is in the buffer.

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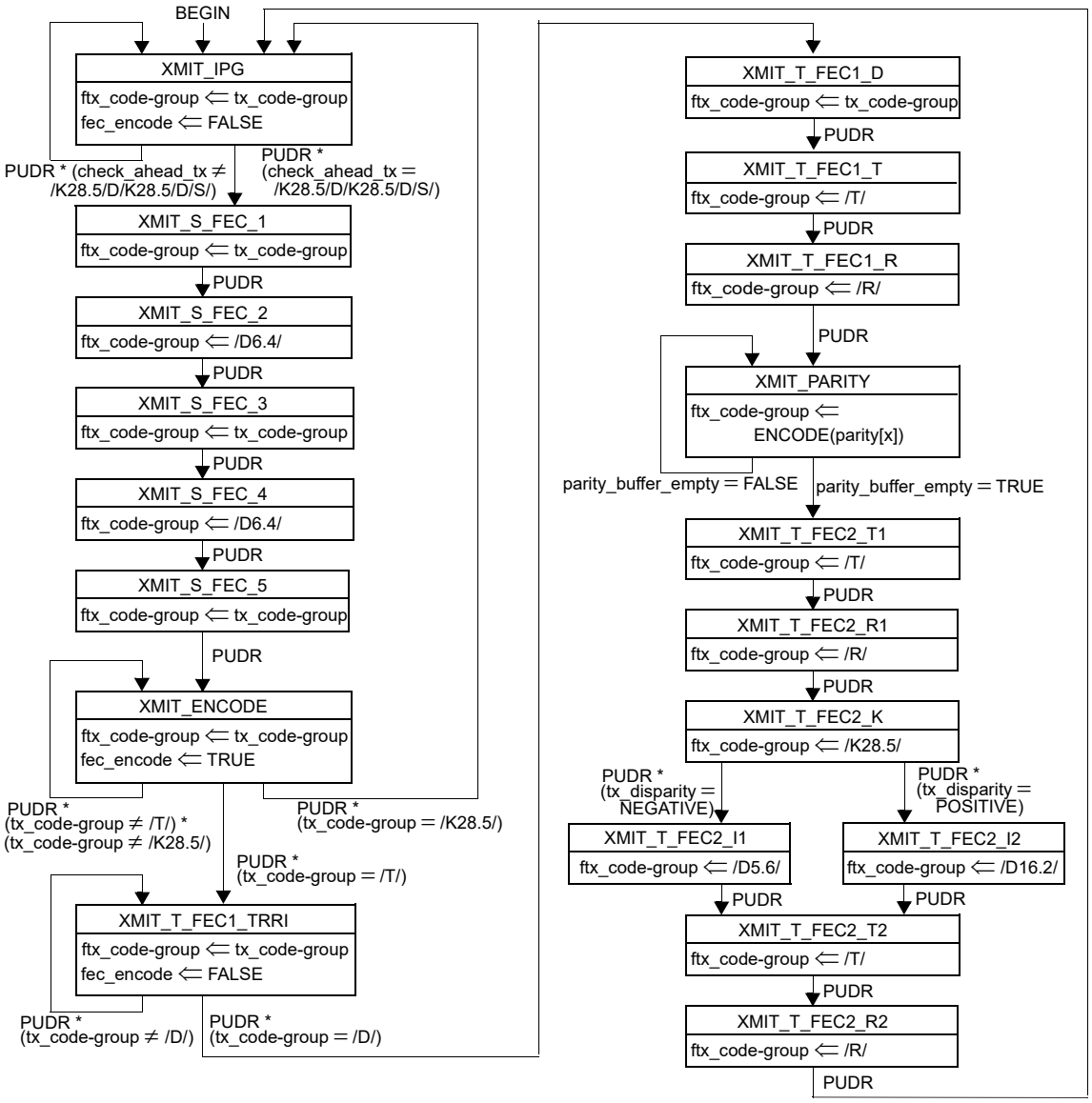

Figure 65–11—Transmit state diagram

65.2.3.6 Error monitoring capability

The following counters apply to FEC sublayer management and error monitoring. If an MDIO interface is provided (see Clause 22), it is accessed via that interface. If not, it is recommended that an equivalent access be provided. These counters are reset to zero upon read or upon reset of the FEC sublayer. When a counter reaches all ones, it stops counting. The counters' purpose is to help monitor the quality of the link.

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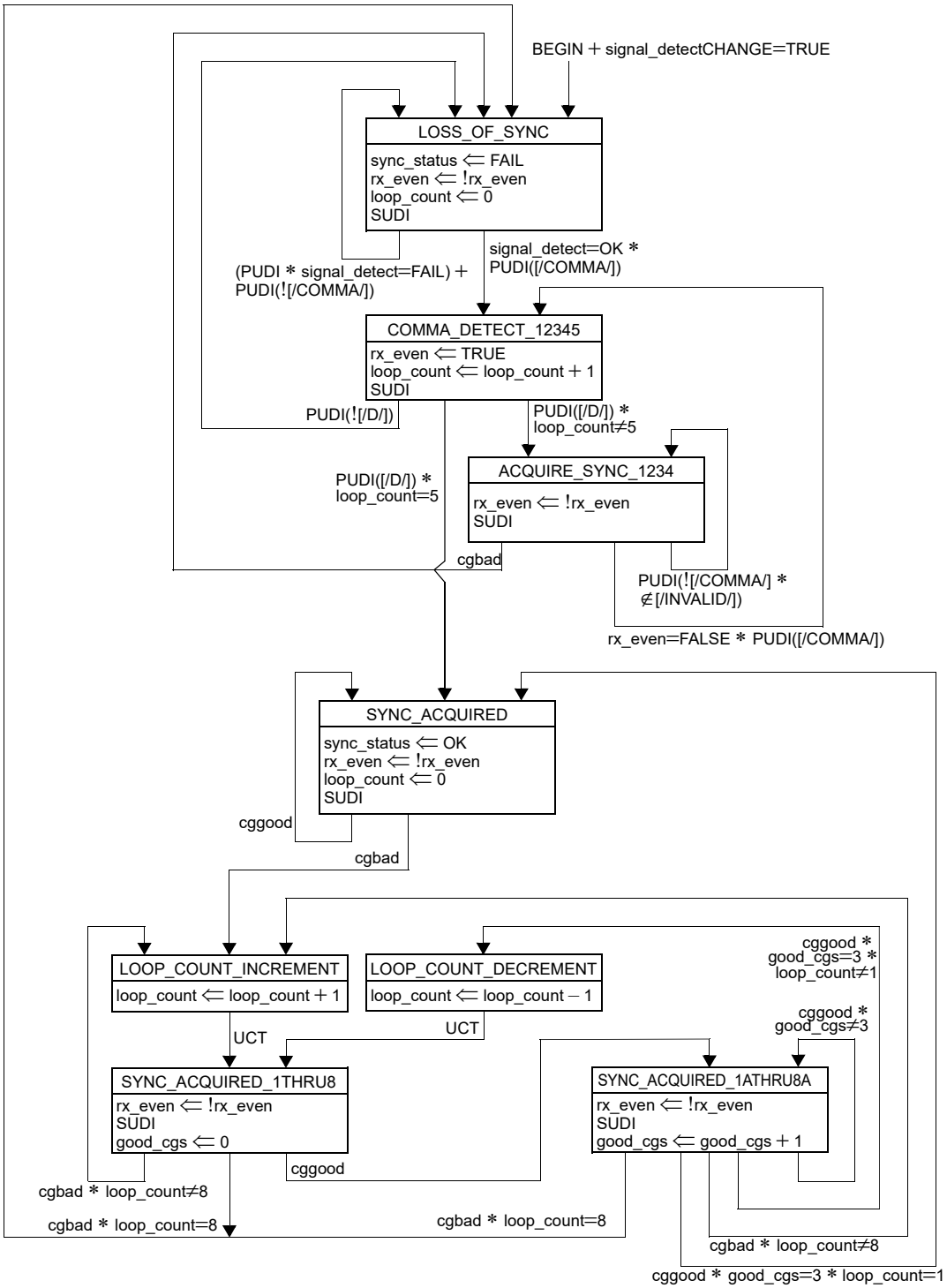

Figure 65–12—Receive synchronization state diagram

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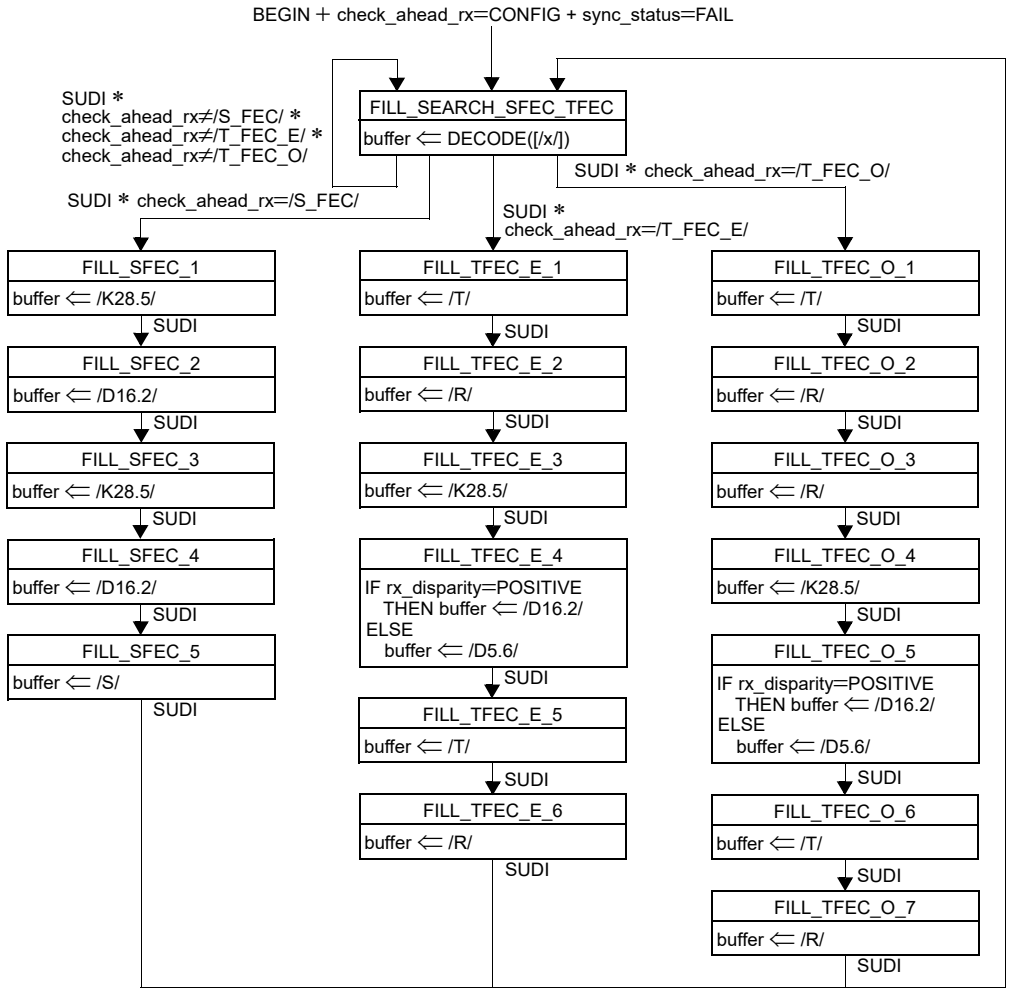

Figure 65–13—Receive buffer-fill state diagram

65.2.3.6.1 buffer_head_coding_violation_counter

32-bit counter. buffer_head_coding_violation_counter counts once for each invalid code-group received directly from the link. This variable is provided by a management interface that may be mapped to the 45.2.10.4 register (29.9.15:0).

65.2.3.6.2 FEC_corrected_blocks_counter

32-bit counter. FEC_corrected_blocks_counter counts once for each corrected FEC blocks in the decoding. This variable is provided by a management interface that may be mapped to the 45.2.10.5 register (29.10.15:0).

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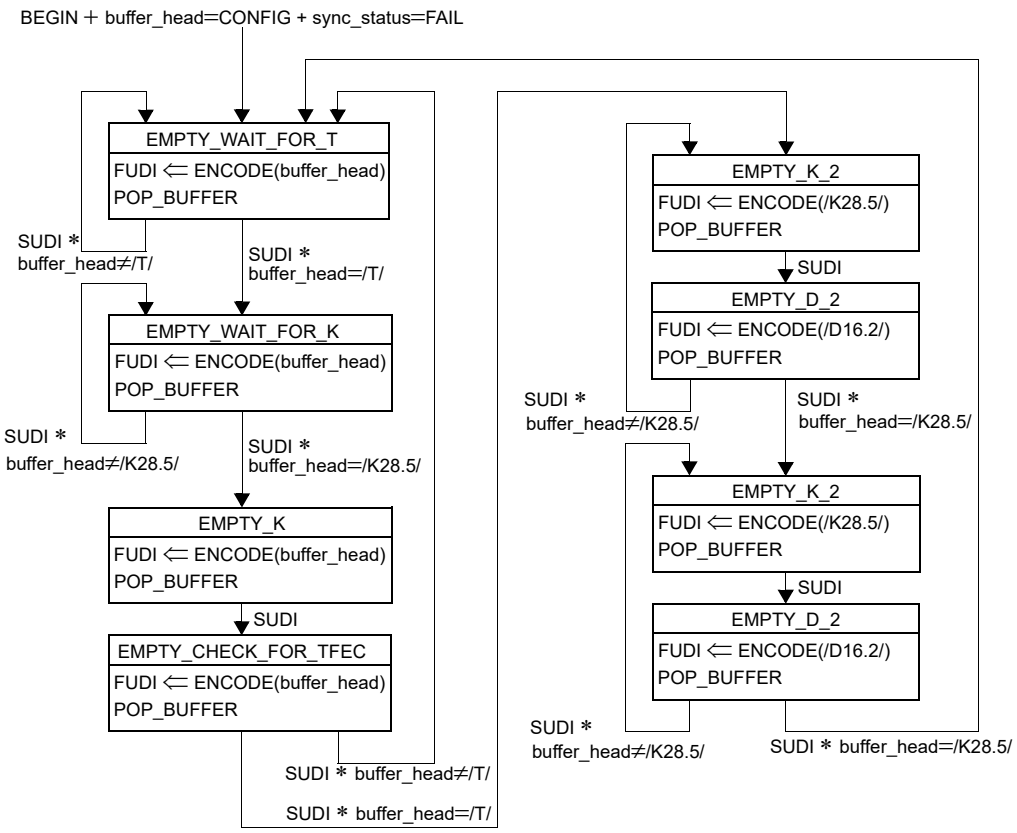

Figure 65–14—Receive buffer-empty state diagram

65.2.3.6.3 FEC_uncorrected_Blocks_counter

32-bit counter. FEC_uncorrected_blocks_counter counts once for each uncorrected FEC blocks in the decoding. This variable is provided by a management interface that may be mapped to the 45.2.10.6 register (29.11.15:0).

65.3 Extensions to PMA for 1000BASE-PX

In addition to the requirements defined in Clause 36, P2MP operation imposes the following requirement on the PMA sublayer of the OLT and ONU.

65.3.1 Extensions for 1000BASE-PX-U

65.3.1.1 Physical Medium Attachment (PMA) sublayer interfaces

In addition to the primitives of Clause 36, the following primitive is defined:

PMD_SIGNAL.request(tx_enable)

This primitive controls PMD emission of light. It is generated by the PCS's data detector (see 65.2.2.2.3) and the effect of its receipt is defined in 60.1.5.3. This primitive is received from the PCS and passed in timely fashion and without modification to the PMD. It takes the following parameter:

tx_enable The tx_enable parameter can take one of two values, ON or OFF.

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65.3.1.2 Loop-timing specifications for ONUs

ONUs shall operate at the same time basis as the OLT, i.e., the ONU TX clock tracks the ONU RX clock. Jitter transfer masks are defined in 60.8.

65.3.2 Extensions for 1000BASE-PX-D

65.3.2.1 CDR lock timing measurement

A PMA instantiated in an OLT becomes synchronized at the bit level within 400 ns (T_{CDR}) and code-group level within an additional 32 ns ($T_{code\_group\_alignment}$) of the appearance of a valid 1000BASE-X IDLE pattern at TP4 when the PMA_TX_CLK frequency is equal to twice the PMA_RX_CLK frequency.

65.3.2.1.1 Definitions

CDR Lock Time (denoted T_{CDR}) is defined as a time interval required by the receiver to acquire phase and frequency lock on the incoming data stream. T_{CDR} is measured as the time elapsed from the moment when electrical signal after the PMD at TP4 reaches the conditions specified in 60.9.13.2.1 for receiver settling time to the moment when the phase and frequency are recovered and jitter is maintained for a network with BER of no more than 10^{-12} for non-FEC systems, or no more than 10^{-4} for FEC enabled systems.

The combined value of measured T_{CDR} and $T_{code\_group\_alignment}$ shall not exceed 432 ns.

65.3.2.1.2 Test specification

Figure 60–2 illustrates the tests setup for the OLT PMA receiver (upstream) T_{CDR} time. The test assumes that there is an optical PMD transmitter at the ONU with well known parameters, having a fixed known T_{on} time as defined in 60.9.13.1, and an optical PMD receiver at the OLT with well-known parameters, having a fixed known $T_{receiver\_settling}$ time as defined in 60.9.13.2. After $T_{on} + T_{receiver\_settling}$ time the parameters at TP4 reach within 15% of their steady state values.

Measure T_{CDR} as the time from the tx_enable assertion, minus the known $T_{on} + T_{receiver\_settling}$ time, to the time the electrical signal at the output of the PMA reaches up to phase difference from the input signal of the transmitting PMA, assuring BER of 10^{-12} for non-FEC systems, or BER of 10^{-4} for FEC enabled systems, and maintaining its jitter specifications. The signal throughout this test, is the 1000BASE-X IDLE pattern.

A non-rigorous way to describe this test setup would be (using a transmitter PMD at the ONU, with a known T_{on} time and a receiver PMD at the OLT, with a known $T_{receiver\_settling}$ time):

For a tested PMA receiver with a declared T_{CDR} time, measure the phase and jitter of the recovered PMA receiver signal after T_{CDR} time from the tx_enable trigger minus the reference $T_{on} + T_{receiver\_settling}$ time, ensuring synchronization to the ONU PMA input signal and conformance to the specified steady state phase, frequency, and jitter values for BER of 10^{-12} for non-FEC systems, or BER of 10^{-4} for FEC enabled systems.

65.3.3 Delay variation requirements

The MPCP relies on strict timing based on the distribution of timestamps. The actual delay is implementation dependent but an implementation shall maintain a combined delay variation through RS, PCS, and PMA sublayers of no more than 16 bit times so as to comply with this mechanism.

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65.4 Protocol implementation conformance statement (PICS) proforma for Clause 65, Extensions of the Reconciliation Sublayer (RS) and Physical Coding Sublayer (PCS)/Physical Media Attachment (PMA) for 1000BASE-X for multipoint links and forward error correction[127]

65.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 65, Extensions of the Reconciliation Sublayer (RS) and Physical Coding Sublayer (PCS)/Physical Media Attachment (PMA) for 1000BASE-X for multipoint links and forward error correction, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

65.4.2 Identification

65.4.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

65.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 65, Extensions of the Reconciliation Sublayer (RS) and Physical Coding Sublayer (PCS)/Physical Media Attachment (PMA) for 1000BASE-X for multipoint links and forward error correction
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[127] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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65.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*OLT	OLT functionality	65.1.1	Device supports functionality required for OLT	O.1	Yes [ ] No [ ]
*ONU	ONU functionality	65.1.1	Device supports functionailty required for ONU	O.1	Yes [ ] No [ ]
*FEC	Forward error correction for multipoint optical links	65.2.3	Device supports FEC for multipoint optical links	O	Yes [ ] No [ ]

65.4.4 PICS proforma tables for Extensions of Reconciliation Sublayer (RS) and Physical Coding Sublayer (PCS)/Physical Media Attachment (PMA) for 1000BASE-X for multipoint links and forward error correction

65.4.4.1 Operating modes of OLT MACs

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Unidirectional mode	65.1.2	Device operates in unidirectional transmission mode	OLT:M	Yes [ ]

65.4.4.2 ONU and OLT variables

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	enable variable	65.1.3.1	True for ONU MAC, TRUE for OLT MAC if enabled, FALSE for OLT MAC if not enabled	M	Yes [ ]
FS2	mode variable	65.1.3.1	0 for ONU MAC, 0 or 1 for enabled OLT MAC	M	Yes [ ]
FS3	logical_link_id variable	65.1.3.1	Set to 0x7FFF until ONU MAC is registered Set to any value for enabled OLT MAC. Set to any value other then 0x7FFF for registered ONU MAC	M	Yes [ ]
FS4	multicast LLID support	65.1.3.1	Supports multicast LLID, multicast_link_id variable	O	Yes [ ] No [ ]

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65.4.4.3 Preamble mapping and replacement

Item	Feature	Subclause	Value/Comment	Status	Support
PM1	CRC-8 generation	65.1.3.2.3	CRC calculation produces same result as serial implementation	M	Yes [ ] No [ ]
PM2	CRC-8 initial value	65.1.3.2.3	CRC shift register initialized to 0x00 before each new calculations	M	Yes [ ] No [ ]
PM3	SLD parsing	65.1.3.3.1	If SLD is not found then discard packet	M	Yes [ ] No[ ]
PM4	SLD replacement	65.1.3.3.1	Replace SLD with preamble	M	Yes [ ] No [ ]
PM5	LLID matching	65.1.3.3.2	If LLID does not match then discard packet	M	Yes [ ] No [ ]
PM6	Multicast LLID matching	65.1.3.3.2	If multicast LLID matches accept the packet	*FS4:M	Yes [ ] No [ ]
PM7	LLID Replacement	65.1.3.3.2	Replace LLID with preamble	M	Yes [ ] No [ ]
PM8	CRC-8 checking	65.1.3.3.3	If CRC does not match then discard packet	M	Yes [ ] No [ ]
PM9	CRC-8 replacement	65.1.3.3.3	Replace CRC with preamble	M	Yes [ ] No [ ]

65.4.4.4 Data detection

Item	Feature	Subclause	Value/Comment	Status	Support
DD1	Buffer depth	65.2.2.1	Depth sufficient to turn on laser and settle receiver	ONU:M	Yes [ ] No [ ]
DD2	OLT laser control	65.2.2.2.3	Always takes the value ON	OLT:M	Yes [ ] No [ ]
DD3	State diagrams	65.2.2.3	Meets the requirements of Figure 65–6	ONU:M	Yes [ ] No[ ]

65.4.4.5 FEC requirements

Item	Feature	Subclause	Value/Comment	Status	Support
FE1	FEC Coding Choice	65.2.3	If FEC is used, it is this one	FEC:M	Yes [ ] No [ ]
FE2	Uncorrectable block replacement	65.2.3.1	Replace all code-groups in an uncorrectable block with /V/	FEC:M	Yes [ ] No [ ]

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65.4.4.6 FEC State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Transmit	65.2.3.5.1	Meets the requirements of Figure 65–11	FEC:M	Yes [ ]
SM2	Receive synchronization	65.2.3.5.2	Meets the requirements of Figure 65–12	FEC:M	Yes [ ]
SM3	Receive	65.2.3.5.3	Meets the requirements of Figure 65–13 for buffer fill and Figure 65–14 for buffer empty	FEC:M	Yes [ ]

65.4.4.7 PMA

Item	Feature	Subclause	Value/Comment	Status	Support
BMC1	Loop Timing	65.3.1.2	ONU RX clock tracks OLT TX clock	ONU:M	Yes [ ] No [ ]

65.4.4.8 OLT Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
OR1	Code-group synchronization delay	65.3.2.1.1	$T_{CDR} + T_{code\_group\_alignment} \leq$ 432 ns	M	Yes [ ] No [ ]

65.4.4.9 Delay variation

Item	Feature	Subclause	Value/Comment	Status	Support
DV1	Delay variation	65.3.3	Combined delay variation through RS, PCS, and PMA sublayers is limited to 16 bit times	M	Yes [ ] No [ ]

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66. Extensions of the 10 Gb/s Reconciliation Sublayer (RS), 100BASE-X PHY, and 1000BASE-X PHY for unidirectional transport

In the absence of unidirectional operation, the sublayers in this clause are precisely the same as their equivalents in Clause 24, Clause 36, and Clause 46. Otherwise, this clause describes additions and modifications to the 100BASE-X, 1000BASE-X, 10GBASE-R, 10GBASE-W, and 10GBASE-X Physical Layers, making them capable of unidirectional operation, which is required to initialize a 1000BASE-PX network, and allows the transmission of Operations, Administration and Management (OAM) frames regardless of whether the PHY has determined that a valid link has been established.

However, unidirectional operation may only be enabled under very limited circumstances. Before enabling this mode, the MAC shall be operating in full-duplex mode and Auto-Negotiation, if applicable, shall be disabled. In addition, the OAM sublayer above the MAC (see Clause 57) shall be present and enabled or (for 1000BASE-X), the PCS shall be part of a 1000BASE-PX-D PHY (see Clause 60 and Clause 64). Unidirectional operation shall not be invoked for a PCS that is part of a 1000BASE-PX-U PHY (except for out-of-service test purposes or where the PON contains just one ONU). Failure to follow these restrictions results in an incompatibility with the assumptions of IEEE 802.1 protocols, a PON that cannot initialize, or collisions, which are unacceptable in the P2MP protocol.

66.1 Modifications to the physical coding sublayer (PCS) and physical medium attachment (PMA) sublayer, type 100BASE-X

66.1.1 Overview

This subclause specifies the 100BASE-X PCS and PMA for support of subscriber access networks.

66.1.2 Functional specifications

The 100BASE-X PCS and PMA for subscriber access networks shall conform to the requirements of the 100BASE-X PCS specified in 24.2 and the 100BASE-X PMA specified in 24.3 with the following exception: The 100BASE-X PCS for subscriber access networks may have the ability to transmit data regardless of whether the PHY has determined that a valid link has been established. The following are the detailed changes to Clause 24 in order to support this additional ability.

66.1.2.1 Variables

Insert a new variable among those already described in 24.2.3.2:

mr_unidirectional_enable
: A control variable that enables the unidirectional mode of operation. This variable is provided by a management interface that may be mapped to the Clause 22 Control register Unidirectional enable bit (0.5).

  Values: FALSE; Unidirectional capability is not enabled
  TRUE; Unidirectional capability is enabled

66.1.2.2 Transmit state diagram

The description of the transmit state diagram is changed to include the contribution of the new mr_unidirectional_enable variable. The third paragraph of 24.2.4.2 is changed to read (~~strikethroughs~~ show deleted text and underscores show inserted text):

> The indication of link_status ≠ OK by the ~~PMA at any time~~ PMA, when mr_unidirectional_enable = FALSE, causes an immediate transition to the IDLE state and supersedes any other Transmit process operations. When mr_unidirectional_enable = TRUE, the Transmit process ignores the value of link_status. This enables the ability to transmit data from the MII when link_status ≠ OK.

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Additionally, the functionality of Figure 24–13 shall be changed as represented by Figure 66–1.

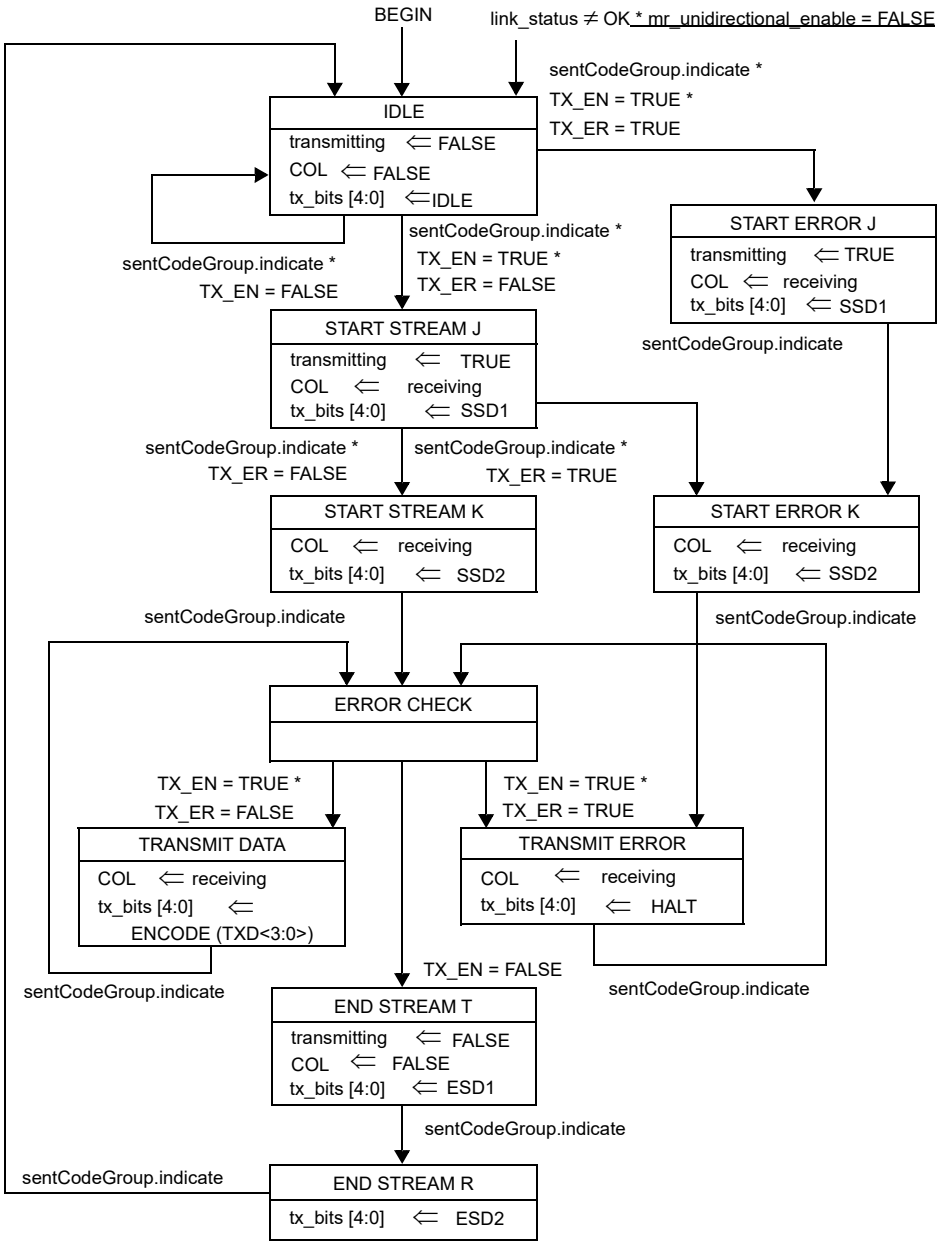

Figure 66–1—Transmit state diagram

66.1.2.3 Far-end fault generate

The description of the far-end fault generate state diagram is also changed to include the contribution of the new mr_unidirectional_enable variable. The first paragraph of 24.3.4.5 is changed to read (~~strikethroughs~~ show deleted text and underscores show inserted text):

> Far-End Fault Generate simply passes tx_code-bits to the TX process when signal_status=ON or when mr_unidirectional_enable=TRUE. When signal_status=OFF and mr_unidirectional_enable=FALSE, it repetitively generates each cycle of the Far-End Fault Indication until signal_status is reasserted or mr_unidirectional_enable is set to TRUE.

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Additionally, the functionality of Figure 24–16 shall be changed as represented by Figure 66–2.

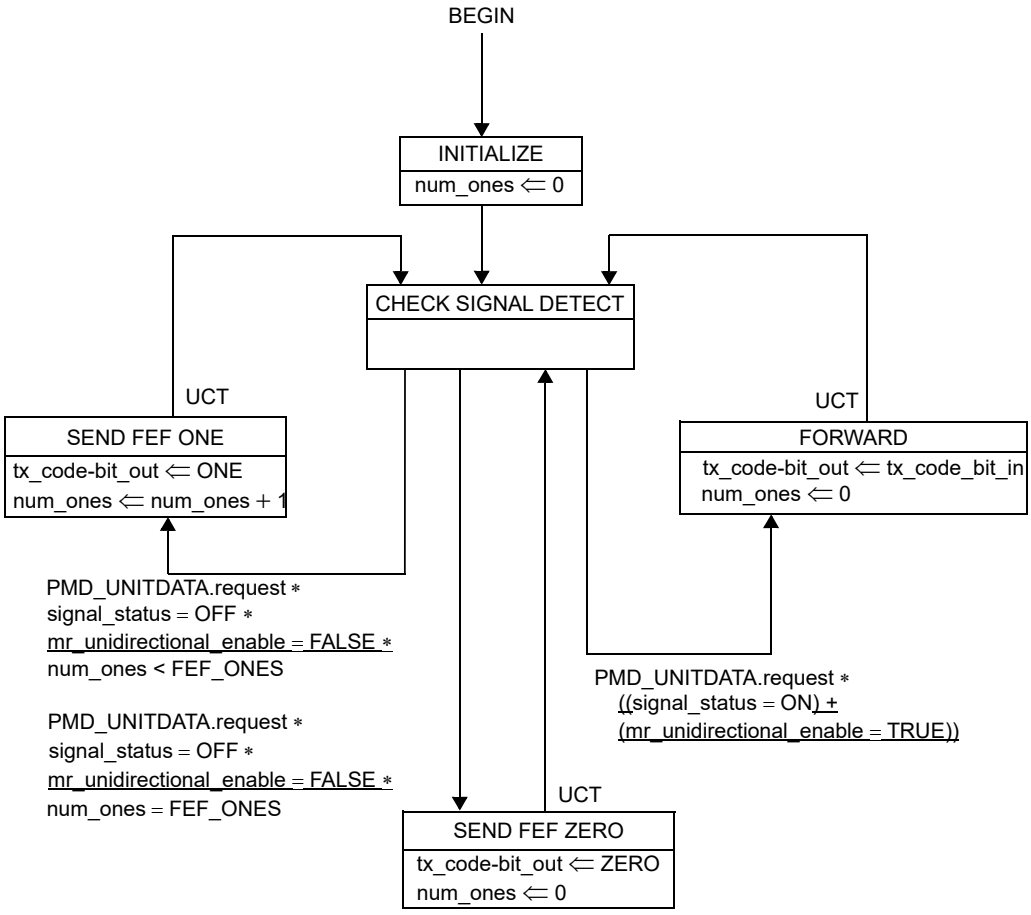

Figure 66–2—Far-End Fault Generate state diagram

66.2 Modifications to the physical coding sublayer (PCS) and physical medium attachment (PMA) sublayer, type 1000BASE-X

66.2.1 Overview

This subclause specifies the 1000BASE-X PCS and PMA for support of subscriber access networks.

66.2.2 Functional specifications

The 1000BASE-X PCS for subscriber access networks shall conform to the requirements of the 1000BASE-X PCS specified in 36.2 with the following exception: The 1000BASE-X PCS for subscriber access networks may have the ability to transmit data regardless of whether the PHY has determined that a valid link has been established. The 1000BASE-X PMA for subscriber access networks shall conform to the requirements of the 1000BASE-X PMA specified in 36.3 with no changes. The following are the detailed changes to Clause 36 in order to support this additional ability.

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66.2.2.1 Variables

Insert a new variable among those already described in 36.2.5.1.3:

mr_unidirectional_enable

A control variable that enables the unidirectional mode of operation. This variable is provided by a management interface that may be mapped to the Clause 22 Control register Unidirectional enable bit (0.5).

Values: FALSE; Unidirectional capability is not enabled
TRUE; Unidirectional capability is enabled

Additionally, modify the existing xmit variable from 36.2.5.1.3 as follows (~~strikethroughs~~ show deleted text and underscores show inserted text):

xmit

When mr_unidirectional_enable=FALSE, xmit is d~~D~~efined in 37.3.1.1. When mr_unidirectional_enable=TRUE, xmit always takes the value DATA.

66.2.2.2 Transmit

The description of the transmit state diagram is changed to include the contribution of the new mr_unidirectional_enable variable. The second paragraph of 36.2.5.2.1 is changed to read (~~strikethroughs~~ show deleted text and underscores show inserted text):

The Transmit ordered set process continuously sources ordered sets to the Transmit code-group process. When mr_unidirectional_enable = TRUE, the Auto-Negotiation process xmit flag always takes the value DATA and the Auto-Negotiation process is never invoked. Otherwise, when initially invoked, and when the Auto-Negotiation process xmit flag indicates CONFIGURATION, the Auto-Negotiation process is invoked. When the Auto-Negotiation process xmit flag indicates IDLE, and between packets (as delimited by the GMII), /I/ is sourced. Upon the assertion of TX_EN by the GMII when the Auto-Negotiation process xmit flag indicates DATA, the SPD ordered set is sourced. Following the SPD, /D/ code-groups are sourced until TX_EN is deasserted. Following the de-assertion of TX_EN, EPD ordered sets are sourced. If TX_ER is asserted when TX_EN is deasserted and carrier extend error is not indicated by TXD, /R/ ordered sets are sourced for as many GTX_CLK periods as TX_ER is asserted with a delay of two GTX_CLK periods to first source the /T/ and /R/ ordered sets. If carrier extend error is indicated by TXD during carrier extend, /V/ ordered sets are sourced. If TX_EN and TX_ER are both de-asserted, the /R/ ordered set may be sourced, after which the sourcing of /I/ is resumed. If, while TX_EN is asserted, the TX_ER signal is asserted, the /V/ ordered set is sourced except when the SPD ordered set is selected for sourcing.

66.2.2.3 Transmit state diagram

The 1000BASE-X PCS for subscriber access networks shall implement the transmit process as depicted in Figure 36–5 and Figure 36–6, including compliance with the associated state variables as specified in 36.2.5.1 and as modified in 66.2.2.1.

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66.3 Modifications to the reconciliation sublayer (RS) for P2P 10 Gb/s operation

66.3.1 Overview

This subclause specifies the 10 Gb/s RS for support of P2P subscriber access networks.

66.3.2 Functional specifications

The 10 Gb/s RS for subscriber access networks shall conform to the requirements of the 10 Gb/s RS specified in Clause 46 with the following exception: The 10 Gb/s RS for subscriber access networks may have the ability to transmit data regardless of whether the PHY has determined that a valid link has been established. The following are the detailed changes to Clause 46 in order to support this additional ability.

66.3.2.1 Link fault signaling

The description of the link fault signaling functional specification is changed to include the contribution of the new mr_unidirectional_enable variable. The second paragraph of 46.3.4 is changed to read (~~strikethroughs~~ show deleted text and underscores show inserted text):

> Sublayers within the PHY are capable of detecting faults that render a link unreliable for communication. Upon recognition of a fault condition a PHY sublayer indicates Local Fault status on the data path. When this Local Fault status reaches an RS, the RS tests the unidirectional_enable variable. If this variable is FALSE, the RS stops sending MAC data, and continuously generates a Remote Fault status on the transmit data path (possibly truncating a MAC frame being transmitted). If this variable is TRUE, the RS continues to allow the transmission of MAC data but replaces IPG with a Remote Fault status. When Remote Fault status is received by an RS, the RS tests the unidirectional_enable variable. If this variable is FALSE, the RS stops sending MAC data, and continuously generates Idle control characters. If this variable is TRUE, the RS continues to allow the transmission of MAC data. When the RS no longer receives fault status messages, it returns to normal operation, sending MAC data.

66.3.2.2 Variables

Insert a new variable among those already described in 46.3.4.2:

unidirectional_enable

A control variable that enables the unidirectional mode of operation.

Values: FALSE; Unidirectional capability is not enabled
TRUE; Unidirectional capability is enabled

66.3.2.3 State diagram

The description of what the RS outputs onto TXC<3:0> and TXD<31:0> is changed to include the contribution of the new mr_unidirectional_enable variable. The lettered list of 46.3.4.3 is changed to read (~~strikethroughs~~ show deleted text and underscores show inserted text):

a) link_fault = OK
The RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.

b) link_fault = Local Fault
If unidirectional_enable=FALSE, t~~T~~he RS shall continuously generate Remote Fault Sequence ordered sets.
If unidirectional_enable=TRUE, the RS shall send MAC frames as requested through the PLS service interface. After a MAC frame and before transition to generation of Remote Fault Sequence

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the RS shall ensure a column of idles has been sent. In the absence of MAC frames, the RS shall generate Remote Fault Sequence ordered sets.

c) link_fault = Remote Fault
If unidirectional_enable=FALSE, t~~T~~he RS shall continuously generate Idle control characters.
If unidirectional_enable=TRUE, the RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.

66.4 Modifications to the RS for P2MP 10 Gb/s operation

66.4.1 Overview

This subclause specifies the 10 Gb/s RS for support of P2MP subscriber access networks.

66.4.2 Functional specifications

The 10 Gb/s RS for P2MP subscriber access networks shall conform to the requirements of the 10 Gb/s RS specified in Clause 46 with the following exception: The 10 Gb/s RS for P2MP subscriber access networks may have the ability to transmit data regardless of whether the PHY has determined that a valid link has been established. The following are the detailed changes to Clause 46 in order to support this additional ability.

66.4.2.1 Link fault signaling

The description of the link fault signaling functional specification is changed to include the contribution of the new unidirectional_enable variable. The second paragraph of 46.3.4 is changed to read (~~strikethroughs~~ show deleted text and underscores show inserted text):

Sublayers within the PHY are capable of detecting faults that render a link unreliable for communication. The nature of the P2MP link allows for some of these fault conditions to be ignored. Upon recognition of a fault condition a PHY sublayer indicates Local Fault status on the data path. When this Local Fault status reaches an RS, the RS tests the unidirectional_enable variable. If this variable is FALSE, the RS stops sending MAC data, and continuously generates ~~a Remote Fault status~~ Idle control characters on the transmit data path (possibly truncating a MAC frame being transmitted). If this variable is TRUE, the RS continues to allow the transmissions of MAC data. When Remote Fault status is received by an RS, the RS tests the unidirectional_enable variable. If this variable is FALSE, the RS stops sending MAC data, and continuously generates Idle control characters. If this variable is TRUE, the RS continues to allow the transmission of MAC data. When the RS no longer receives fault status messages, it returns to normal operation, sending MAC data.

66.4.2.2 Variables

Insert a new variable among those already described in 46.3.4.2:

unidirectional_enable
A control variable that enables the unidirectional mode of operation.
Values:FALSE; Unidirectional capability is not enabled
TRUE; Unidirectional capability is enabled

66.4.2.3 State diagram

The description of what the RS outputs onto TXC<3:0> and TXD<31:0> is changed to include the contribution of the new unidirectional_enable variable. The lettered list of 46.3.4.3 is changed to read (~~strikethroughs~~ show deleted text and underscores show inserted text):

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a) link_fault = OK

The RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.

b) link_fault = Local Fault

If unidirectional_enable = FALSE, t~~T~~he RS shall continuously generate Idle control characters~~Remote Fault Sequence ordered sets~~.

If unidirectional_enable = TRUE, the RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.

c) link_fault = Remote Fault

If unidirectional_enable = FALSE, t~~T~~he RS shall continuously generate Idle control characters.

If unidirectional_enable = TRUE, the RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.

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66.5 Protocol implementation conformance statement (PICS) proforma for Clause 66, Extensions of the 10 Gb/s Reconciliation Sublayer (RS), 100BASE-X PHY, and 1000BASE-X PHY for unidirectional transport[128]

66.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 66, Extensions of the 10 Gb/s Reconciliation Sublayer (RS), 100BASE-X PHY, and 1000BASE-X PHY for unidirectional transport, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

66.5.2 Identification

66.5.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

66.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 66, Extensions of the 10 Gb/s Reconciliation Sublayer (RS), 100BASE-X PHY, and 1000BASE-X PHY for unidirectional transport
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[128] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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66.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PUNI	Unidirectional operation	66	Device supports unidirectional operation	O	Yes [ ] No [ ]
*HUN	100BASE-X functionality	66.1	Device supports functionality required for 100BASE-X PHY for subscriber access networks	O	Yes [ ] No [ ]
*GIG	1000BASE-X functionality	66.2	Device supports functionality required for 1000BASE-X PCS for subscriber access networks	O	Yes [ ] No [ ]
*XG	10 Gb/s functionality	66.3	Device supports functionality required for 10 Gb/s RS for subscriber access networks	O	Yes [ ] No [ ]
*XP2MP	10 Gb/s P2MP operation	66.4	Device supports 10 Gb/s P2MP operation	O	Yes [ ] No [ ]

66.5.4 PICS proforma tables for Extensions of the 10 Gb/s Reconciliation Sublayer (RS), 100BASE-X PHY, and 1000BASE-X PHY for unidirectional transport

66.5.4.1 Maintaining compatibility with IEEE 802.1 protocols

Item	Feature	Subclause	Value/Comment	Status	Support
MC1	Unidirectional mode enabled	66	Full duplex and disable AutoNeg and [(OAM present and enabled) or 1000BASE-PX-D] and not 1000BASE-PX-U	M	Yes [ ] No [ ]

66.5.4.2 Extensions of the 100BASE-X PHY

Item	Feature	Subclause	Value/Comment	Status	Support
H1	Integrates 100BASE-X PCS and PMA	66.1.2	See Clause 24	HUN:M	Yes [ ]
H2	Transmit state diagram	66.1.2.2	Replaces Figure 24–8	PUNI* HUN:M	Yes [ ]
H3	Far-End Fault Generate state diagram	66.1.2.3	Replaces Figure 24–16	PUNI* HUN:M	Yes [ ]

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66.5.4.3 Extensions of the 1000BASE-X PHY

Item	Feature	Subclause	Value/Comment	Status	Support
G1	Integrates 1000BASE-X PCS and PMA	66.2.2	See Clause 36	GIG:M	Yes [ ]
G2	Transmit state diagram	66.2.2.3	As modified by the new variables	PUNI* GIG:M	Yes [ ]

66.5.4.4 Extensions of the 10 Gb/s P2P RS

Item	Feature	Subclause	Value/Comment	Status	Support
LF1	Integrates 10 Gb/s RS	66.3.2	See Clause 46	XG:M	Yes [ ]
LF2	link_fault = OK and MAC frames	66.3.2.3	RS services MAC frame transmission requests	PUNI* XG:M	Yes [ ] No [ ]
LF3	link_fault = OK and no MAC frames	66.3.2.3	In absence of MAC frames, RS transmits Idle control characters	PUNI* XG:M	Yes [ ] No [ ]
LF4	link_fault = Local Fault and unidirectional_enable = FALSE	66.3.2.3	RS transmits continuous Remote Fault Sequence ordered sets	PUNI* XG:M	Yes [ ] No[ ]
LF5	link_fault = Local Fault and unidirectional_enable = TRUE and MAC frames	66.3.2.3	RS services MAC frame transmission requests	PUNI* XG:M	Yes [ ] No[ ]
LF6	link_fault = Local Fault and unidirectional_enable = TRUE and MAC frame ends	66.3.2.3	RS transmits one full column of IDLE after frame	PUNI* XG:M	Yes [ ] No[ ]
LF7	link_fault = Local Fault and unidirectional_enable = TRUE and no MAC frames	66.3.2.3	RS transmits continuous Remote Fault Sequence ordered sets	PUNI* XG:M	Yes [ ] No[ ]
LF8	link_fault = Remote Fault and unidirectional_enable = FALSE	66.3.2.3	RS transmits continuous Idle control characters	PUNI* XG:M	Yes [ ] No [ ]
LF9	link_fault = Remote Fault and unidirectional_enable = TRUE and MAC frames	66.3.2.3	RS services MAC frame transmission requests	PUNI* XG:M	Yes [ ] No [ ]
LF10	link_fault = Remote Fault and unidirectional_enable = TRUE and no MAC frames	66.3.2.3	RS transmits continuous Idle control characters	PUNI* XG:M	Yes [ ] No[ ]

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66.5.4.5 Extensions of the 10 Gb/s P2MP RS

Item	Feature	Subclause	Value/Comment	Status	Support
PF1	Integrates 10 Gb/s P2MP RS	66.4.2	See Clause 76	PUNI * XP2MP:M	Yes [ ]
PF2	link_fault = OK and MAC frames	66.4.2.3	RS services MAC frame transmission requests	PUNI * XP2MP:M	Yes [ ] No [ ]
PF3	link_fault = OK and no MAC frames	66.4.2.3	In absence of MAC frames, RS transmits Idle control characters	PUNI * XP2MP:M	Yes [ ] No [ ]
PF4	link_fault = Local Fault and unidirectional_enable = FALSE	66.4.2.3	RS transmits continuous Idle control characters	PUNI * XP2MP:M	Yes [ ] No [ ]
PF5	link_fault = Local Fault and unidirectional_enable = TRUE and MAC frames	66.4.2.3	RS services MAC frame transmission requests	PUNI * XP2MP:M	Yes [ ] No [ ]
PF6	link_fault = Local Fault and unidirectional_enable = TRUE and no MAC frames	66.4.2.3	In absence of MAC frames, RS transmits Idle control characters	PUNI * XP2MP:M	Yes [ ] No [ ]
PF7	link_fault = Remote Fault and unidirectional_enable = FALSE	66.4.2.3	RS transmits continuous Idle control characters	PUNI * XP2MP:M	Yes [ ] No [ ]
PF8	link_fault = Remote Fault and unidirectional_enable = TRUE and no MAC frames	66.4.2.3	RS services MAC frame transmission requests	PUNI * XP2MP:M	Yes [ ] No [ ]
PF9	link_fault = Remote Fault and unidirectional_enable = TRUE and no MAC frames	66.4.2.3	In absence of MAC frames, RS transmits Idle control characters	PUNI * XP2MP:M	Yes [ ] No [ ]

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67. System considerations for Ethernet subscriber access networks

67.1 Overview

This clause provides information on building Ethernet subscriber access networks, also referred to as "Ethernet in the First Mile" or EFM networks.

EFM encompasses a family of technologies that vary in media type and signaling speed. EFM is designed to be deployed in networks of one or multiple EFM media type(s) as well as interact with mixed 10/100/1000/10000 Mb/s Ethernet networks. Any network topology defined in IEEE Std 802.3 can be used within the subscriber premises and then connected to an Ethernet subscriber access network via an IEEE Std 802.1Q compliant bridge, or a router.

Further, within a given EFM domain, the specific EFM technologies allow for a variety of topologies affording the subscriber access network maximum flexibility. For example, a 1000BASE-PX10 P2MP system with 16 ONUs can be built with a 1:16 splitter or as a tree-and-branch network utilizing more than one splitter.

The design of multiple-domain networks is governed by the rules defining each of the transmission systems incorporated into the design. The physical size of a network is limited by the characteristics of individual network components. These characteristics include the media lengths and type.

Table 67–1 summarizes the various EFM media characteristics.

Table 67–1—Characteristics of the various EFM network media segments

Media type	Rate	Number of PHYs per segment	Nominal reach (km)
Optical 100 Mb/s fiber segment (100BASE-LX10, 100BASE-BX10)	100 Mb/s	2	10
Optical 1000 Mb/s fiber segment (1000BASE-LX10, 1000BASE-BX10)	1 Gb/s	2	10
Optical 1000 Mb/s P2MP segment (1000BASE-PX10)	1 Gb/s[a]	17[b,c]	10
Optical 1000 Mb/s P2MP segment (1000BASE-PX20)		17[b,c]	20
Optical 1000 Mb/s P2MP segment (1000BASE-PX30)		33[b,c]	20
Optical 1000 Mb/s P2MP segment (1000BASE-PX40)		65[b,c]	20
Optical 10/1 Gb/s P2MP segment (10/1GBASE-PRX10)	10 / 1 Gb/s[d]	17[b,c]	10
Optical 10/1 Gb/s P2MP segment (10/1GBASE-PRX20)		17[b,c]	20
Optical 10/1 Gb/s P2MP segment (10/1GBASE-PRX30)		33[b,c]	20
Optical 10/1 Gb/s P2MP segment (10/1GBASE-PRX40)		65[b,c]	20

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Table 67–1—Characteristics of the various EFM network media segments *(continued)*

Media type	Rate	Number of PHYs per segment	Nominal reach (km)
Optical 10 Gb/s P2MP segment (10GBASE-PR10)	10 Gb/s[e]	17[b,c]	10
Optical 10 Gb/s P2MP segment (10GBASE-PR20)		17[b,c]	20
Optical 10 Gb/s P2MP segment (10/1GBASE-PR30)		33[b,c]	20
Optical 10 Gb/s P2MP segment (10GBASE-PR40)		65[b,c]	20
Copper high-speed segment (10PASS-TS)	10 Mb/s[f]	2	0.75
Copper long reach segment (2BASE-TL)	2 Mb/s[c]	2	2.7
EPoC coaxial segment (10GPASS-XR)	Up to 10 Gb/s downstream	variable[g]	2.9[h]
	Up to 1.6 Gb/s upstream	variable[g]	2.9[h]
Optical Nx25-EPON P2MP segment (50/50-PQ20*, 50/25-PQ20*, 25/25-PQ20*) [i]	50 / 50 Gb/s [j] 50 / 25 Gb/s 25 / 25 Gb/s	17[b,c]	20
		33[b,c]	10
Optical Nx25-EPON P2MP segment (50/10-PQ20*, 25/25-PQ20*) [i]	50 / 10 Gb/s [j] 25 / 10 Gb/s	17[b,c]	20
		33[b,c]	10
Optical Nx25-EPON P2MP segment (50/50-PQ30*, 50/25-PQ30*, 25/25-PQ30*) [i]	50 / 50 Gb/s [j] 50 / 25 Gb/s 25 / 25 Gb/s	33[b,c]	20
Optical Nx25-EPON P2MP segment (50/10-PQ30*, 25/25-PQ30*) [i]	50 / 10 Gb/s [j] 25 / 10 Gb/s	33[b,c]	20

[a]1 Gb/s in downstream direction, 1 Gb/s in upstream direction.
[b]P2MP segments may be implemented with a trade off between link span and split ratio listed. Refer to 67.2.1.
[c]The number of PHYs in the P2MP segment includes the OLT PHY.
[d]10 Gb/s in downstream direction, 1 Gb/s in upstream direction (asymmetric data rate in 10/1G-EPON).
[e]10 Gb/s in downstream direction, 10 Gb/s in upstream direction (symmetric data rate in 10/10G-EPON).
[f]Nominal rate stated at the nominal reach in this table. Rate and reach can vary depending on the plant. For 2BASE-TL please refer to Annex 63B for more information. For 10PASS-TS, please refer to Annex 62A for more information.
[g] Based on the cable operator's CCDN configuration, the number of PHYs will be the CLT PHY plus each CNU PHY.
[h] Maximal differential distance between CNUs. Reach may vary depending on the CCDN.
[i]For brevity, the two Nx25G-EPON PMD coexistence class designators "X" and "G" have been abbreviated in this table with an asterisk ("*") as they are equivalent with respect to rate, number of PHYs per segment, and nominal reach (see 141.1.3 and 141.2.5).
[j]For Nx25G-EPON possible downstream rates are either 25 Gb/s or 50 Gb/s and possible upstream rates are 10 Gb/s, 25 Gb/s, or 50 Gb/s. The format shown in the table is the downstream rate followed by a forward slash ("/") followed by the upstream rate (see 141.2.2).

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67.2 Discussion and examples of EFM P2MP topologies

This subclause discusses EFM P2MP topologies. For P2MP PON architecture, this subclause details flexibility of trading off split ratio for link span. This subclause also shows some examples of different P2MP PON topologies.

67.2.1 Trade off between link span and split ratio for P2MP PON architecture

While the P2MP PON PMDs are nominally described in terms of a link span of either 10 km or 20 km with a 1:16 split ratio, other link spans and split ratios can be implemented provided that the requirements of Table 60–1 are met.

67.2.2 Single splitter topology for P2MP PON architecture

A P2MP PON topology implemented with a single optical splitter is shown in Figure 67–1.

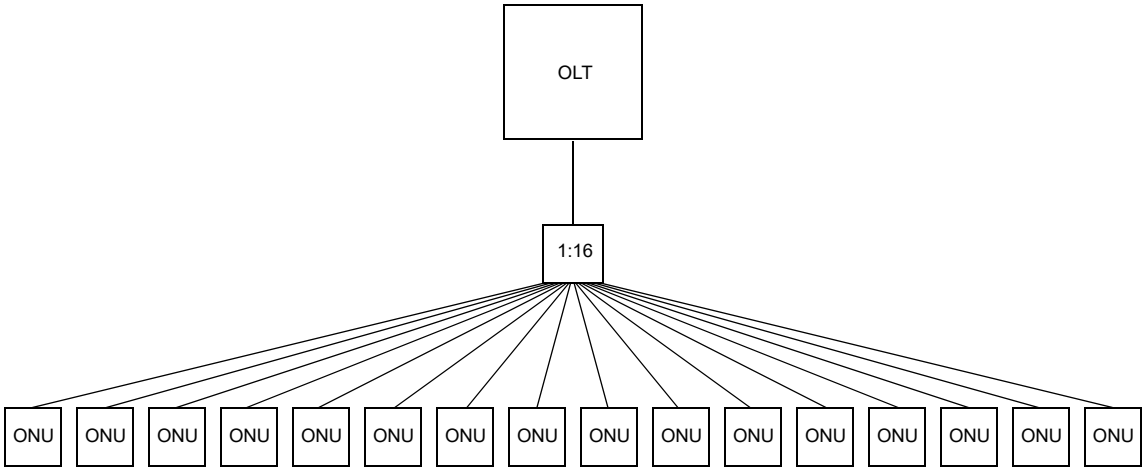

Figure 67–1—Single splitter topology

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67.2.3 Tree-and-branch topology for P2MP PON architecture

A P2MP PON topology implemented with a tree-and-branches of optical splitters is shown in Figure 67–2.

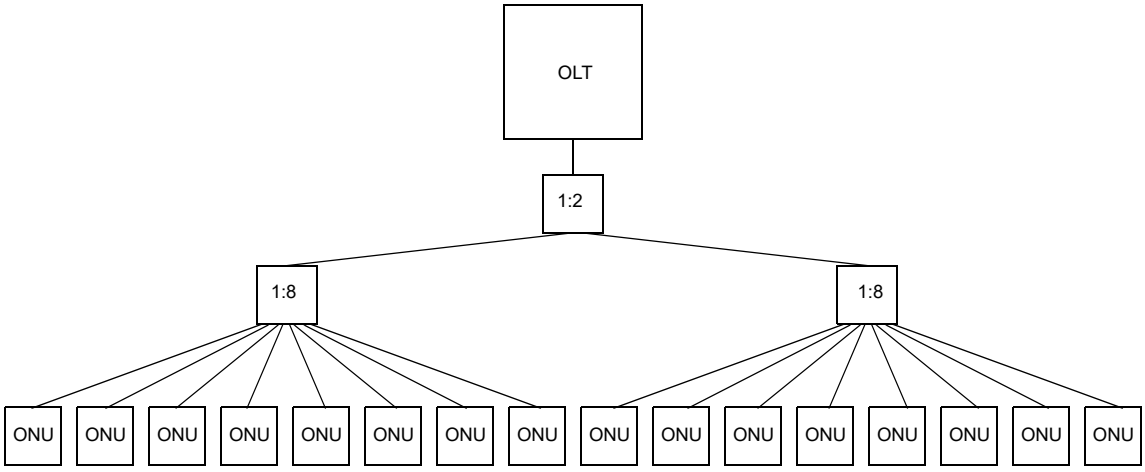

Figure 67–2—Tree-and-branch topology

67.2.4 Interoperability between certain 1000BASE-PX10 and 1000BASE-PX20

1000BASE-PX20-D PMD is interoperable with a 1000BASE-PX10-U PMD, this allows certain upgrade possibilities from 10 km to 20 km P2MP networks.

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67.3 Hybrid media topologies

Hybrid media topologies, such as those shown in Figure 67–3, can be implemented using a combination of P2P or P2MP optical links and copper links.

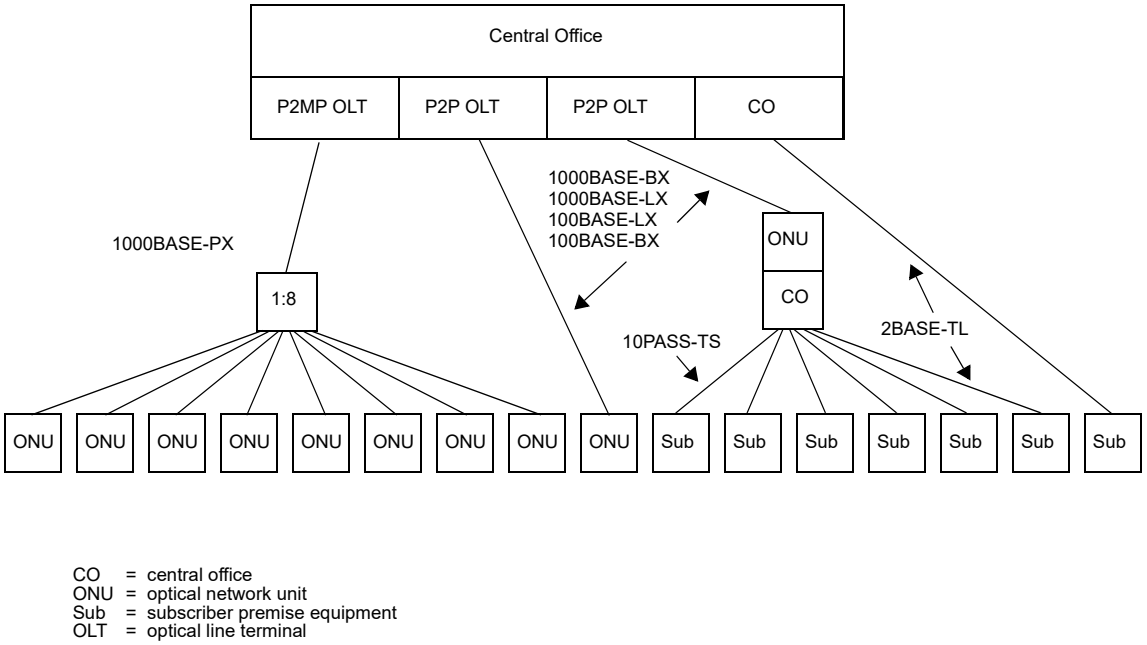

Figure 67–3—Hybrid media topologies

67.4 Topology limitations

The physical size of EFM networks is not limited by the round-trip collision propagation delay. Instead, the maximum link length between DTEs is limited by the signal transmission characteristics of the specific link.

67.5 Deployment restrictions for subscriber access copper

10PASS-TS and 2BASE-TL PHYs have been specified to allow deployment on public access networks. Non-loaded cable is a requirement of the signaling methods employed. The 10PASS-TS do not preclude coexistence with POTS. However, it is important that systems are designed and configured to comply with all appropriate regulatory, governmental and regional requirements. Refer to Annex 62A (10PASS-TS) and Annex 63A (2PASS-TL) for further information regarding configuration profiles.

67.6 Operations, Administration, and Maintenance

All P2P and emulated P2P links, including all of the EFM network media segments, support the optional OAM sublayer as defined in Clause 57. 2BASE-TL and 10PASS-TS PHYs do not support unidirectional links as defined in 57.2.6 (see 61.1).

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67.6.1 Unidirectional links

Some Physical Layer devices have the optional ability to encode and transmit data while one direction of the link is non-operational.

This ability should be used only when the OAM sublayer is present and enabled or for a 1000BASE-PX-D, 10/1GBASE-PRX, 10GBASE-PR PHY, or 10GPASS-XR-D PHY. Otherwise, MAC Client frames will be sent across a unidirectional link potentially causing havoc with bridge and other higher layer protocols. The feature should not be enabled for 1000BASE-PX-U, 10/1GBASE-PRX-U, 10GBASE-PR-U PHYs, or 10GPASS-XR-U PHYs in service, to avoid simultaneous transmission by more than one ONU or CNU.

67.6.2 Active and Passive modes

A device may be configured to be in either Active or Passive OAM mode. At least one end of a given link is required to be in Active mode.

In an access network, customer premises devices will commonly be configured as Passive devices. All other devices in an access network will commonly be configured as Active devices. For a detailed description of Active and Passive mode, refer to 57.2.6.

67.6.3 Link status signaling in P2MP networks

In P2MP networks the local_link_status parameter should reflect the status of a logical link associated with the underlying instance of Multipoint MAC Control. This is achieved by mapping the local_link_status parameter to variable 'registered' defined in 64.3.3.2 for 1G-EPON links, in 77.3.3.2 for 10G-EPON links, and in 103.3.3.2 for EPoC links as follows:

local_link_status = OK if registered = true

local_link_status = FAIL if registered = false

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68. Physical medium dependent (PMD) sublayer type 10GBASE-LRM

68.1 Overview

This clause specifies the 10GBASE-LRM PMD and the associated multimode fiber media. In order to form a complete Physical Layer, the PMD is combined with the sublayers appropriate for 10GBASE-R, as specified in Table 52–2, and optionally with the management functions that may be accessible through the management interface defined in Clause 45.

Figure 68–1 depicts the relationships of the PMD (shown hatched) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model. Clause 44 contains an introduction to 10 Gigabit Ethernet and the relationship of the 10GBASE-LRM PMD to other sublayers. Further relevant information may be found in Clause 1 (i.e., terminology and conventions, references, definitions and abbreviations) and Annex A (i.e., bibliography, entries referenced here in the format [B*n*]).

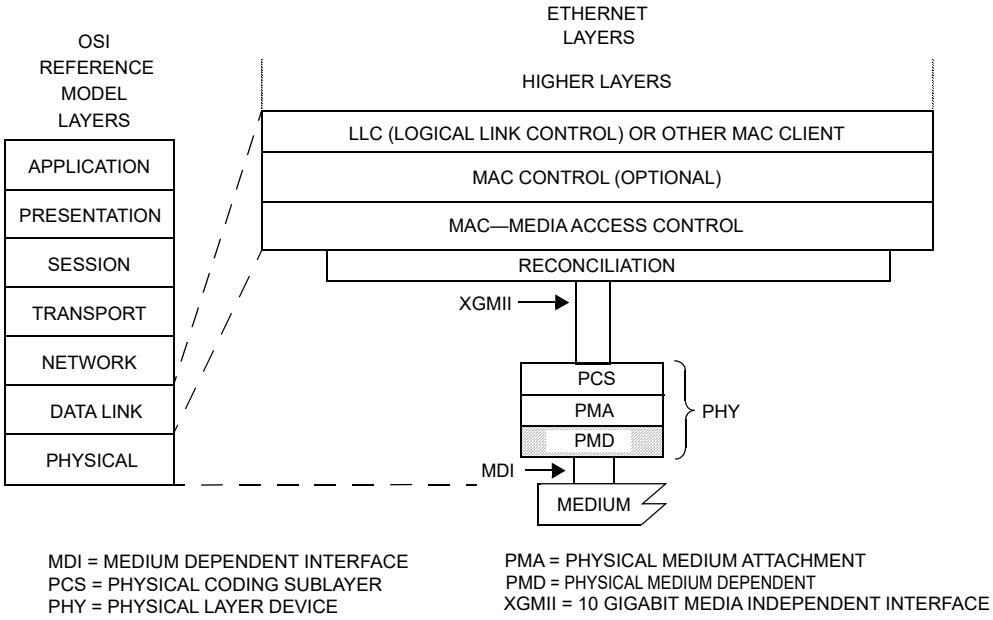

Figure 68–1—10GBASE-LRM PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

68.1.1 Physical Medium Dependent (PMD) sublayer service interface

The PMD service interface is the 10GBASE-R PMD service interface as described in 52.1.1.

68.2 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation. The PMA and PMD shall incur a round-trip delay (transmit and receive) of not more than 9216 bit times, or 18 pause_quanta, while including two meters of fiber. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 44.3.

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68.3 PMD MDIO function mapping

If present, the 10GBASE-LRM PMD MDIO function mapping shall be as specified in 52.3.

68.4 PMD functional specifications

The 10GBASE-LRM PMD performs the transmit and receive functions that convey data between the PMD service interface and the MDI.

68.4.1 PMD block diagram

For the purposes of system conformance, the PMD sublayer is standardized at test points TP2 and TP3, as shown in Figure 68–2. The optical transmit signal is defined at the output end of a patch cord (TP2), of between 2 m and 5 m in length. The optical launch condition at TP2 is either the preferred launch or the alternative launch (at the user's choice), as specified in 68.5.1. A compliant PMD shall support both options. The launch is selected by using either a single-mode fiber offset-launch mode-conditioning patch cord or a regular multimode fiber patch cord inserted between the MDI and TP2, consistent with the media type. Unless specified otherwise, all transmitter measurements and tests defined in 68.6 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) that is the input to the MDI of the optical receiver. Unless specified otherwise, for all receiver measurements and tests defined in 68.6, the test stimulus is applied at TP3.

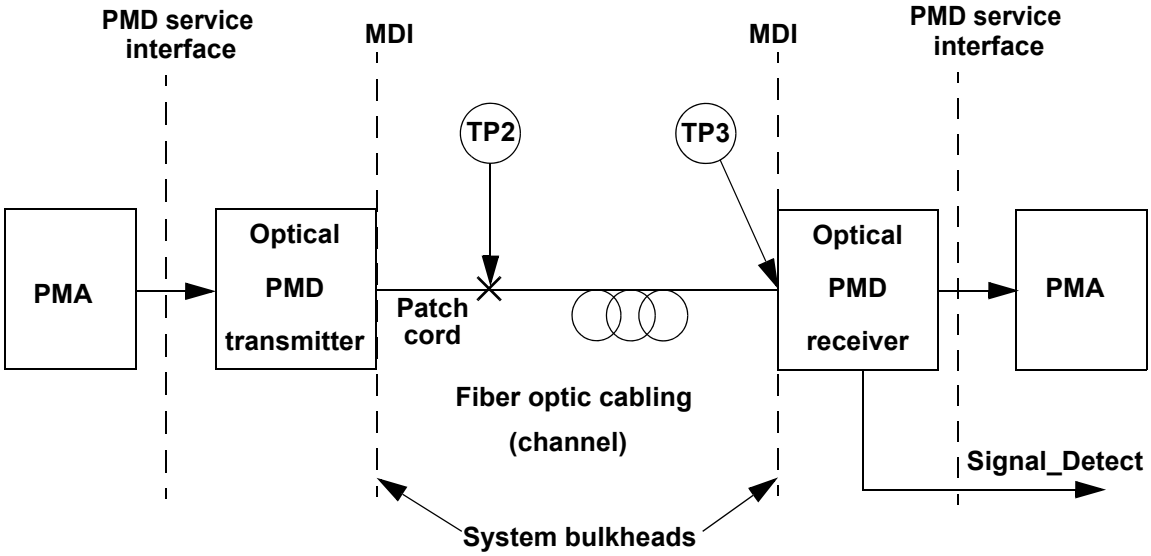

Figure 68–2—Block diagram

68.4.2 PMD transmit function

The PMD transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the optical specifications in this clause. The higher optical power level shall correspond to tx_bit = ONE.

68.4.3 PMD receive function

The PMD receive function shall convey the bits received from the MDI according to the optical specifications in this clause to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). The higher optical power level shall correspond to rx_bit = ONE.

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68.4.4 PMD signal detect function

The PMD signal detect function shall report to the PMD service interface using the message PMD_SIGNAL.indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indication is intended to be an indicator of optical signal presence. If the MDIO interface is implemented, then PMD_global_signal_detect (1.10.0) shall be continuously set to the value of SIGNAL_DETECT as described in 45.2.1.9.7.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 68–1. The PMD receiver is not required to verify whether a compliant 10GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 68–1—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
Input average power < –30 dBm	FAIL
Compliant 10GBASE-R input signal with optical power in OMA > stressed sensitivity in OMA in Table 68–5	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD due to crosstalk, power supply noise, etc.

Various implementations of the signal detect function are permitted, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the received optical signal and implementations that respond to the average power of the received optical signal.

68.4.5 PMD_reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as specified in 45.2.1.1.1.

68.4.6 PMD_fault function

If the MDIO is implemented, PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation-specific fault.

68.4.7 PMD_global_transmit_disable function

The PMD_global_transmit_disable function is optional. When asserted, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of OFF transmitter in Table 68–3.

If a PMD_transmit_fault (optional) is detected, then the PMD_global_transmit_disable function should also be asserted.

If the MDIO interface is implemented, then this function shall map to the PMD_global_transmit_disable bit as specified in 45.2.1.8.7.

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68.4.8 PMD_transmit_fault function

The PMD_transmit_fault function is optional. The faults detected by this function are implementation specific, but should not include the assertion of the PMD_global_transmit_disable function.

If a PMD_transmit_fault (optional) is detected, then the PMD_global_transmit_disable function should also be asserted.

If the MDIO interface is implemented, then this function shall be mapped to the PMD_transmit_fault bit as specified in 45.2.1.7.4.

68.4.9 PMD_receive_fault function

The PMD_receive_fault function is optional. PMD_receive_fault is the logical OR of NOT SIGNAL_DETECT and any implementation-specific fault.

If the MDIO interface is implemented, then this function shall contribute to the PMA/PMD receive fault bit as specified in 45.2.1.7.5.

68.5 PMD to MDI optical specifications

The operating ranges for 10GBASE-LRM are given in Table 68–2. A PMD that exceeds the operational range requirements given in this clause, while meeting all other specifications, is considered compliant.

Table 68–2—10GBASE-LRM fiber types and operating ranges

Multimode fiber type[a]	ISO/IEC 11801:2002 fiber type	Operating range (m)	Maximum channel insertion loss (dB)[b]
62.5 μm 160/500[c]		0.5 to 220	1.9
62.5 μm 200/500	OM1	0.5 to 220	1.9
50 μm 500/500	OM2	0.5 to 220	1.9
50 μm 400/400		0.5 to 100	1.7
50 μm 1500/500[d]	OM3	0.5 to 220	1.9

[a]Each fiber type is identified by its core diameter followed by a pair of OFL bandwidth values separated by "/". The OFL bandwidths are in MHz · km and are for 850 nm and 1300 nm respectively.
[b]Channel insertion loss includes cabled optical fiber attenuation and an allocation of 1.5 dB for connectors.
[c]160/500, 62.5 μm fiber is commonly referred to as "FDDI-grade" fiber.
[d]The OM3 fiber specification includes the 850 nm laser launch bandwidth in addition to the OFL bandwidths.

68.5.1 Transmitter optical specifications

The 10GBASE-LRM transmitter shall meet the specifications given in Table 68–3 and Figure 68–3, per definitions in 68.6.

68.5.2 Characteristics of signal within, and at the receiving end of, a compliant 10GBASE-LRM channel

Table 68–4 gives the characteristics of a signal within, and at the receiving end of, a compliant 10GBASE-LRM channel. A signal with power in OMA and average power not within the ranges given cannot be compliant. However, a signal with power values within the ranges is not necessarily compliant.

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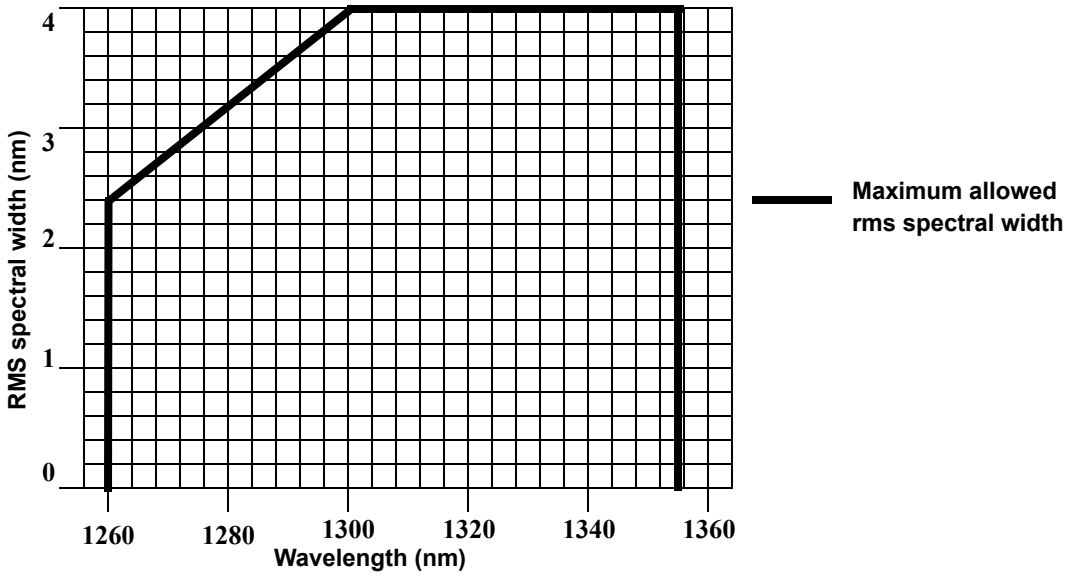

Figure 68–3—10GBASE-LRM Transmitter spectral limits

68.5.3 Receiver optical specifications

The 10GBASE-LRM receiver shall meet the specifications given in Table 68–5, per definitions in 68.6.

68.5.3.1 Dynamic response

Channel responses are expected to vary with time at rates of up to 10 Hz. It is highly recommended that receivers tolerate such time varying channel responses.

68.6 Definitions of optical parameters and measurement methods

The following definitions and measurement methods apply to the transmitter and receiver optical parameters given in Table 68–3 and Table 68–5.

68.6.1 Test patterns and related subclauses for optical parameters

Compliance is to be achieved in normal operation. Table 68–6 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. The test patterns include pattern 1, pattern 2, pattern 3, and square waves, defined in 52.9.1.1 and 52.9.1.2, as well as the PRBS9 pattern.

NOTE—The longer test patterns are designed to emulate system operation; however, they do not form valid 10GBASE-R frames.

68.6.2 Optical modulation amplitude (OMA)

For the purposes of Clause 68, OMA is defined by the measurement method given in 52.9.5, and as illustrated in Figure 68–4. The mean logic ONE and mean logic ZERO values are measured over the center 20% of the two time intervals of the square wave. The OMA is the difference between these two means.

NOTE—An estimate of the OMA value is provided by the variable Measured OMA in 68.6.6.2.

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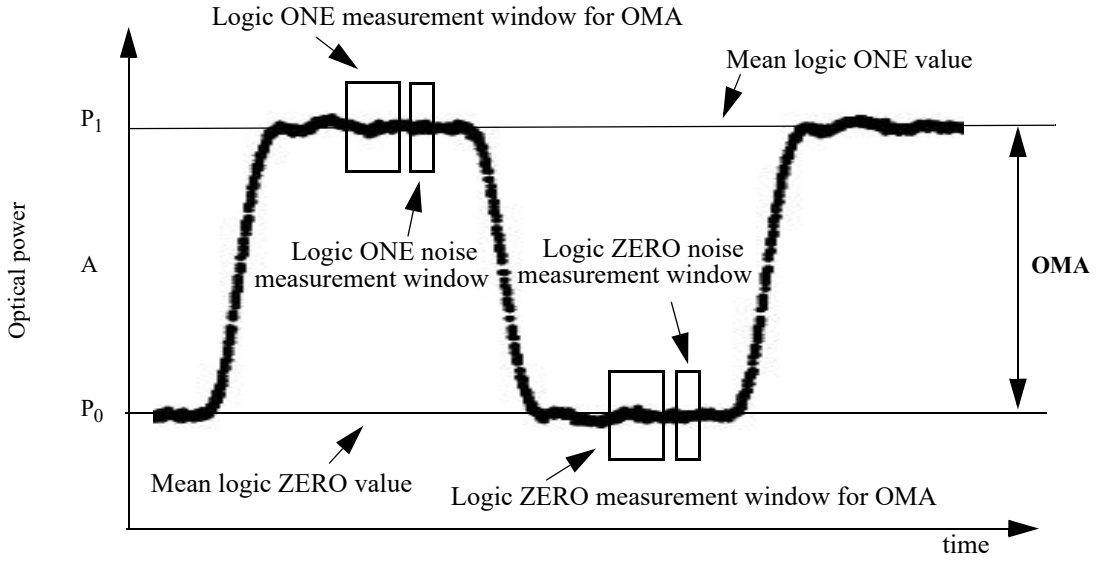

Figure 68–4—Positions of logic ZERO and logic ONE measurement windows for OMA and transmitter noise measurements

68.6.3 Extinction ratio measurement

The extinction ratio shall meet specifications according to 52.9.4.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 68–6).

68.6.4 Relationship between OMA, extinction ratio and average power

The relationship between OMA, extinction ratio and average power is described in 58B.2.

NOTE—The difference between Clause 68 and Clause 58 measurement methods for OMA causes the equations in 58B.2 to become approximations for transmitter signals with undershoot, overshoot, or intersymbol interference. It is recommended that these equations not be used for signals at TP3. Figure 68–5 illustrates the approximate region of transmitter compliance and also the approximate relationships between OMA, extinction ratio, and average power.

68.6.5 Transmitter optical waveform—transmitter eye mask

The required transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 68–6. Compliance is to be assured with pattern 1 or 3 defined in 52.9.1. Measurements during system operation or with other patterns, such as a 2^{23}– 1 PRBS or a valid 10GBASE-R signal, are likely to give very similar results. The transmitter optical waveform of a port transmitting the test pattern specified in Table 68–6 shall meet specifications according to the methods specified below.

Normalized amplitudes of 0 and 1 represent the amplitudes of logic ZERO and ONE respectively. These are defined by the means of the lower and upper halves of the central 0.2 UI of the eye. Normalized times of 0 and 1 on the unit interval scale are determined by the eye crossing means measured at the average value of the optical eye pattern. A clock recovery unit (CRU) should be used to trigger the oscilloscope for mask measurements, as shown in Figure 52–9. It should have a high-frequency corner bandwidth of 4 MHz and a slope of –20 dB/decade. The CRU tracks acceptable levels of low-frequency jitter and wander.

The eye is measured with respect to the mask using a receiver with the fourth-order Bessel-Thomson response with nominal f_r of 7.5 GHz as specified for STM-64 in ITU-T G.691, with the tolerances there specified. The Bessel-Thomson receiver is not intended to represent the noise filter used within a compliant

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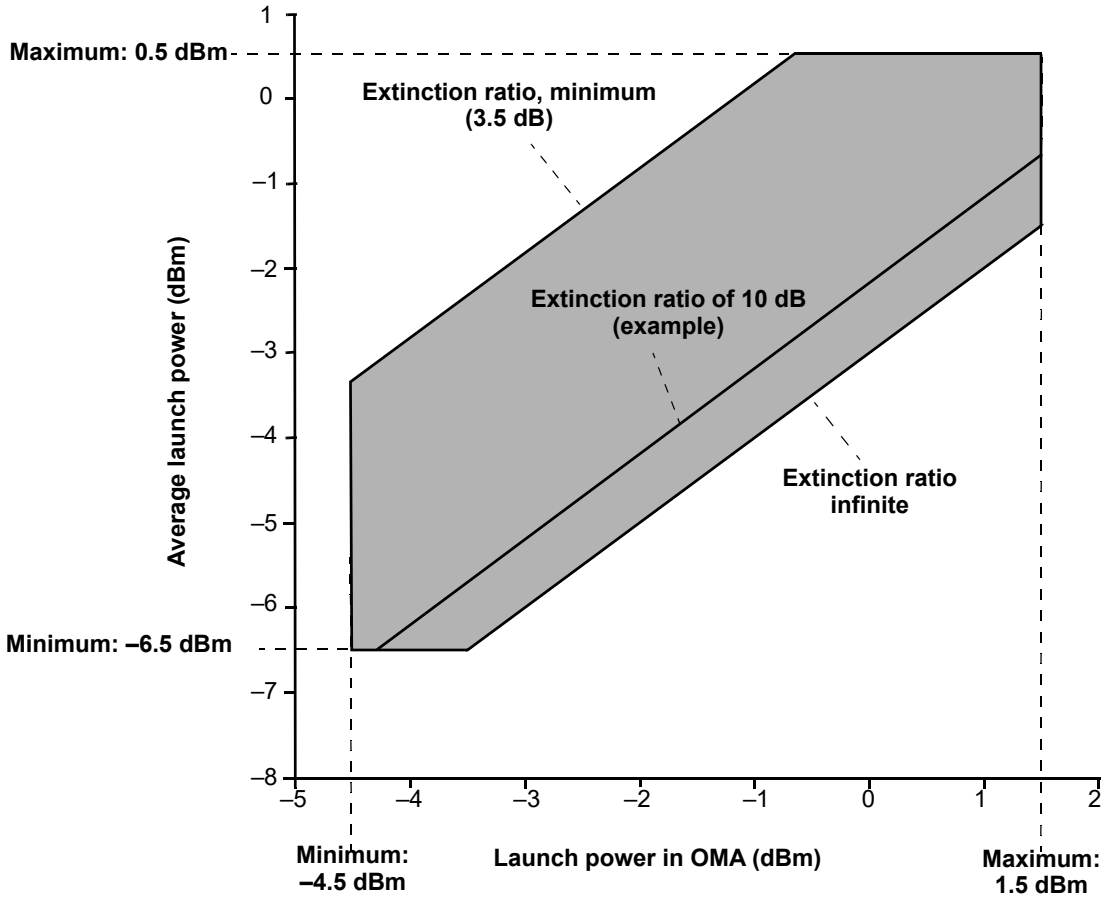

Figure 68–5—Illustration of approximate region of transmitter compliance (shown shaded)

optical receiver, but is intended to provide uniform measurement conditions at the transmitter. The nominal transfer function is given in Equation (52–2) and Equation (52–3).

The transmitter shall achieve a hit ratio lower than 5×10^{-5} hits per sample, where "hits" are the number of samples within the grey areas of Figure 68–6, and the sample count is the total number of samples from 0 UI to 1 UI. Some illustrative examples are provided in 68.6.5.1.

Further information on optical eye pattern measurement procedures may be found in IEC 61280-2-2.

68.6.5.1 Examples of transmitter eye mask acceptable hit count

If an oscilloscope records 1350 samples/screen, and the time-base is set to 0.2 UI per division with 10 divisions across the screen, and the measurement is continued for 200 waveforms, then a transmitter with an expectation of less than 6.75 hits is compliant. i.e.,

$$\frac{5 \times 10^{-5} \times 200 \times 1350}{0.2 \times 10} = 6.75 \tag{68–1}$$

Likewise, if a measurement is continued for 1000 waveforms, then an expectation of less than 33.75 hits is compliant. An extended measurement is expected to give a more accurate result, and a single reading of 6 hits in 200 waveforms would not give a statistically significant pass or fail. Measurements to "zero hits,"

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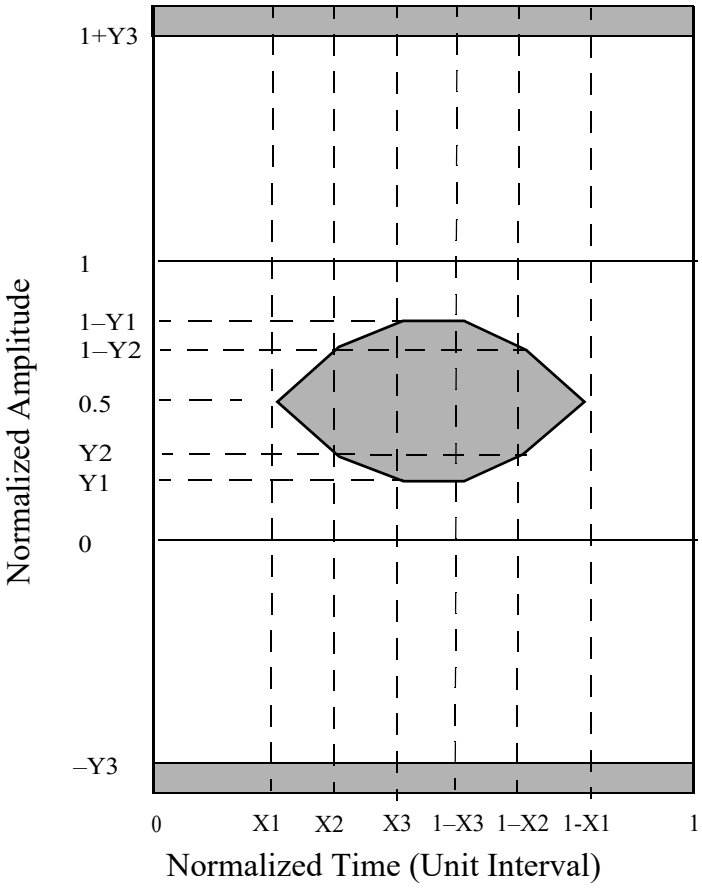

Figure 68–6—Transmitter eye mask definition

which involve finding the position of the worst single sample in the measurement, have degraded reproducibility because random processes cause the position of such a single low-probability event to vary.

The hit ratio limit has been chosen to avoid misleading results due to transmitter and oscilloscope noise.

68.6.6 Transmitter waveform and dispersion penalty (TWDP)

The transmitter waveform shall meet the transmitter waveform and dispersion penalty (TWDP) specification given in Table 68–3.

TWDP is a measure of the deterministic dispersion penalty due to a particular transmitter with reference emulated multimode fibers and receiver. Figure 68–7 shows the TWDP measurement configuration. A waveform from TP2 of the system under test is captured for analysis using an oscilloscope having a fourth-order, 7.5 GHz Bessel-Thomson response.

68.6.6.1 TWDP measurement procedure

The system under test repetitively transmits a test pattern, as specified in Table 68–6. The waveform is captured using averaging to avoid a pessimistic estimate of TWDP. An effective sample rate of at least seven samples per unit interval is required. If test pattern 1 is transmitted, then the specified sub-pattern is to be captured. If PRBS9 is used, then the entire pattern is to be captured.

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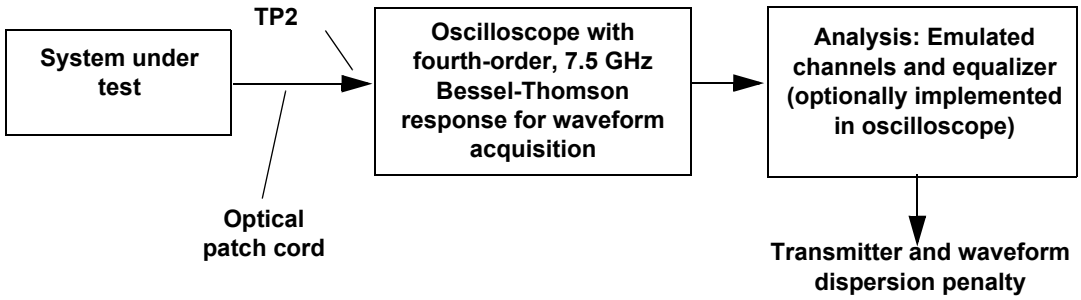

Figure 68–7—Transmitter waveform and dispersion penalty measurement configuration

NOTE—The algorithm assumes 16 samples per unit interval. Interpolation is required for a waveform not captured with 16 samples per unit interval. Use of the $\sin(x)/x$ method or the cubic spline method is recommended. Linear interpolation is not recommended.

The captured waveform is analyzed using the algorithm given below, or equivalent. This algorithm analyses the waveform in combination with each of three emulated channels, equivalent to those given in Table 68–5 for the comprehensive stressed receiver specifications, and with an emulated reference receiver equalizer. A penalty is computed for each of the three emulated channels and the TWDP value is the largest of the three penalty results.

The reference equalizer is a decision feedback equalizer with defined tap number and spacing, as specified in 68.6.6.2. This is not intended to represent the equalizer used within an optical receiver, but is intended to provide uniform measurement conditions at the transmitter.

See Swenson, et al. [B63] for a detailed explanation of the TWDP algorithm.

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Table 68–3—10GBASE-LRM transmit characteristics

Description	Type	Value	Unit
Signaling speed	nom	10.3125	GBd
Signaling speed variation from nominal	max	± 100	ppm
Center wavelength	range	1260 to 1355	nm
RMS spectral width[a] at 1260 nm RMS spectral width between 1260 nm and 1300 nm RMS spectral width between 1300 nm and 1355 nm	max max max	2.4 Figure 68–3 4	nm nm nm
Launch power in OMA[b]	max	1.5	dBm
Launch power in OMA[b]	min	–4.5	dBm
Average launch power[b]	max	0.5	dBm
Average launch power[b]	min	–6.5	dBm
Average launch power[b] of OFF transmitter	max	–30	dBm
Extinction ratio	min	3.5	dB
Peak launch power[bc]	max	3	dBm
$RIN_{20}OMA$	max	–128	dB/Hz
Eye mask parameters {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.40, 0.45, 0.25, 0.28, 0.80}	
Transmitter waveform and dispersion penalty (TWDP)	max	4.7	dB
Uncorrelated jitter (rms)	max	0.033	UI
Optical launch for OM1 and 160/500, 62.5 µm fiber Preferred[d] Encircled flux[e] for alternative launch	— min min	 62.5 µm mode-conditioning patch cord, as specified in 68.9.3 30% within 5 µm radius 81% within 11 µm radius	
Optical launch for OM2, and 400/400, 50 µm fiber Preferred[d] Encircled flux[e] for alternative launch	— min min	 50 µm mode-conditioning patch cord, as specified in 68.9.3 30% within 5 µm radius 81% within 11 µm radius	
Optical launch for OM3, 50 µm, fiber Encircled flux[e]	 min min	 30% within 5 µm radius 81% within 11 µm radius	
Optical return loss tolerance	min	20	dB

[a]RMS spectral width is the standard deviation of the spectrum.
[b]The OMA, average launch power and peak launch power specifications apply at TP2. This is after each type of patch cord. For information: Patch cord losses, between MDI and TP2, differ. The range of losses have to be accounted for to ensure compliance to TP2.
[c]Peak optical power can be determined as the maximum value from the waveform capture for the TWDP test, or equivalent method.
[d]The PMD has to support both the preferred and alternative launch types by the use of a single-mode fiber offset-launch mode-conditioning patch cord, or a regular multimode fiber patch cord, between the MDI and TP2.

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[e]This encircled flux specification, measured per IEC 61280-1-4:2003, defines the near field light distribution at TP2 when the MDI is coupled directly into a 50 μm patch cord and when the MDI is coupled directly into a 62.5 μm patch cord.

Table 68–4—Characteristics of signal within, and at the receiving end of, a compliant 10GBASE-LRM channel[a]

Description	Type	Value	Unit
Highest power in OMA	max	1.5	dBm
Lowest power in OMA	min	–6.4	dBm
Highest average power	max	0.5	dBm
Lowest average power	min	–8.4	dBm
Peak power	max	3	dBm

[a]A signal with power in OMA and average power not within the ranges given cannot be compliant. However, a signal with power values within the ranges is not necessarily compliant.

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Table 68–5—10GBASE-LRM receive characteristics

Description		Type	Value	Unit
Signaling speed		nom	10.3125	GBd
Signaling speed variation from nominal		max	±100	ppm
Center wavelength		range	1260 to 1355	nm
Stressed sensitivity in OMA		—	–6.5	dBm
Stressed sensitivity in OMA for symmetrical test		—	–6	dBm
Overload in OMA		—	1.5	dBm
Conditions of comprehensive stressed receiver tests:				
	Bandwidth of Gaussian white noise source[a]	min	10	GHz
	Test transmitter signal to noise ratio, Q_{sq} [b]	—	26.3	
	Tap spacing, Δt, of ISI generator	—	0.75	UI
	Pre-cursor tap weights {A1, A2, A3, A4}	—	{0.158, 0.176, 0.499, 0.167}	
	Symmetrical tap weights {A1, A2, A3, A4}	—	{0.00, 0.513, 0.00, 0.487}	
	Post-cursor tap weights {A1, A2, A3, A4}	—	{0.254, 0.453, 0.155, 0.138}	
Conditions of simple stressed receiver test:				
	Signal rise and fall times (20% to 80%)	—	115	ps
Conditions of receiver jitter tolerance test:				
	Jitter frequency and peak to peak amplitude	—	(75, 5)	(kHz, UI)
	Jitter frequency and peak to peak amplitude	—	(375, 1)	(kHz, UI)
Received average power for damage[c]		—	1.5	dBm
Receiver reflectance		max	–12	dB

[a]Bandwidth of Gaussian white noise source refers to the –3 dB (electrical) frequency of the noise spectrum before any subsequent filtering.
[b]Transmitter signal to noise ratio, Q_{sq}, is defined in 68.6.7 and its use here is qualified by 68.6.9.3.
[c]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average received power level.

Table 68–6—Test-pattern definitions and related subclauses

Test	Pattern	Related subclause
Transmitter OMA (modulated optical power)	Square	68.6.2
Calibration of OMA for receiver tests	Square, eight ONEs and eight ZEROs	68.6.9 and 68.6.10

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Table 68–6—Test-pattern definitions and related subclauses *(continued)*

Test	Pattern	Related subclause
Calibration of noise for receiver tests	Square, eight ONEs and eight ZEROs	68.6.9
Transmitter noise	Square	68.6.7
Transmitter uncorrelated jitter	1, 2, or PRBS9[a]	68.6.8
Extinction ratio	1 or 3	68.6.3
Average optical power	1 or 3	52.9.3
Transmitted waveform (eye mask)	1 or 3	68.6.5
Transmitter waveform and dispersion penalty (TWDP) Pattern 1 subsequence Pattern 1 subsequence key	1 or PRBS9[a] 348 bits, beginning at bit 3258 101010111011011, beginning immediately before the subsequence at bit 3243	68.6.6
Encircled flux	Not specified here	See IEC 61280-1-4:2003
Wavelength, spectral width	1 or 3	52.9.2
Receiver jitter tolerance	1 or 3	68.6.11
Comprehensive stressed receiver sensitivity	2 or 3	68.6.9
Comprehensive stressed receiver overload	1 or 3	68.6.9
Simple stressed receiver sensitivity	1 or 3	68.6.10
Simple stressed receiver overload	1 or 3	68.6.10

[a]The PRBS9 pattern is optional. If used, it is generated by the polynomial $x^9 + x^5 + 1$ as specified in ITU-T O.153. The binary (0,1) data sequence $d(n)$ is given by $d(n) = d(n – 9) + d(n – 5)$, modulo 2. The pattern has a run of nine ones in its length of 511 bits.

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68.6.6.2 TWDP signal processing algorithm [129, 130, 131]

```
%%%%%%% Script to compute TWDP %%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% TP2 test inputs
%% The values given below for TxDataFile and MeasuredWaveformFile are examples and should be
%% replaced by actual path\filenames for each waveform tested.
%% Transmit data file: The transmit data sequence is one of the TWDP test patterns defined in
%% Table 68–6. The file format is ASCII with a single column of chronological ones and zeros
%% with no headers or footers.
TxDataFile = 'prbs9_950.txt';
%% Measured waveform: The waveform consists of exactly N samples per unit interval T, where N is the
%% oversampling rate. The waveform is circularly shifted to align with the data sequence. The file
%% format for the measured waveform is ASCII with a single column of chronological numerical samples,
%% in optical power, with no headers or footers.
MeasuredWaveformFile = 'preproc-1207-01.txt';
OverSampleRate = 16; % Oversampling rate, has to be even
%% Simulated fiber responses, modeled as a set of ideal delta functions with specified amplitudes in optical
%% power and delays in nanoseconds, in rows. The three cases specified in Table 68–5 for the
%% comprehensive stressed receiver tests are used. The vector 'PCoefs' contains the amplitudes, and the
%% vector 'Delays' contains the delays.
FiberResp = [...
   0.000000 0.072727 0.145455 0.218182
   0.158 0.176 0.499 0.167
   0.000 0.513 0.000 0.487
   0.254 0.453 0.155 0.138];
Delays = FiberResp(1,:)';

%% Program constants %%
SymbolPeriod = 1/10.3125; % Symbol period (ns)
EqNf = 14; EqNb = 5; % 14 T/2-spaced feedforward equalizer taps; 5 T-spaced feedback equalizer taps
%% Set search range for equalizer delay, specified in symbol periods. Lower end of range is minimum
%% channel delay. Upper end of range is the sum of the lengths of the FFE and channel. Round up and add
%% 5 to account for the antialiasing filter.
EqDelMin = floor(min(Delays)/SymbolPeriod);
EqDelMax = ceil(EqNf/2 + max(Delays)/SymbolPeriod)+5;
EqDelVec = [EqDelMin:EqDelMax];
PAlloc = 6.5; % Total allocated dispersion penalty (dBo)
Q0 = 7.03; % BER = 10^(-12)
N0 = SymbolPeriod/2 / (Q0 * 10^(PAlloc/10))^2;

%% Load input waveform and data sequence, generate filter and other matrices
yout0 = load(MeasuredWaveformFile);
XmitData = load(TxDataFile);
PtrnLength = length(XmitData);
TotLen = PtrnLength*OverSampleRate;
Fgrid = [-TotLen/2:TotLen/2-1].'/(PtrnLength*SymbolPeriod);
%% Compute frequency response of 7.5 GHz 4th order Butterworth antialiasing filter
a = [1 123.1407 7581.811 273453.7 4931335]; % Denominator polynomial for frequency response
b = 4931335; % Numerator for frequency response
ExpArg = -j*2*pi*Fgrid;
H_r = b./polyval(a,-ExpArg); % Frequency response of Butterworth antialiasing filter
```

[129] This code is written in the MATLAB programming language (see 1.3); however, use of this language does not indicate an endorsement of MATLAB by IEEE and, as such, any tool can be used to perform this calculation.

[130] *Copyright release for MATLAB code:* Users of this standard may freely copy or reproduce the MATLAB code in this subclause so it can be used for its intended purpose. Users should be aware, however, that this copyright release does not cover any patent rights that a third party may have in the MATLAB code.

[131] The script and associated files are available at https://standards.ieee.org/downloads/802.3/.

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```
ONE=ones(PtrnLength,1);

%% Normalize the received OMA to 1. Estimate the OMA of the captured waveform by using a linear fit to
%% estimate a pulse response, synthesize a square wave, and calculate the OMA of the synthesized square
%% wave per 52.9.5
ant=4; mem=40; % Anticipation and memory parameters for linear fit
X=zeros(ant+mem+1,PtrnLength); % Size data matrix for linear fit
Y=zeros(OverSampleRate,PtrnLength); % Size observation matrix for linear fit
for ind=1:ant+mem+1
   X(ind,:)=circshift(XmitData,ind-ant-1)'; % Wrap appropriately for lin fit
end
X=[X;ones(1,PtrnLength)]; % The all-ones row is included to compute the bias
for ind=1:OverSampleRate
   Y(ind,:)=yout0([0:PtrnLength-1]*OverSampleRate+ind)'; % Each column is one bit period
end
Qmat=Y*X'*(X*X')^(-1); % Coefficient matrix resulting from linear fit. Each column (except
%% the last) is one bit period of the pulse response. The last column is the bias.
SqWvPer=16; % Even number; sets the period of the square wave used to compute the OMA
SqWv=[zeros(SqWvPer/2,1);ones(SqWvPer/2,1)]; % One period of square wave (column)
X=zeros(ant+mem+1,SqWvPer); % Size data matrix for synthesis
for ind=1:ant+mem+1
   X(ind,:)=circshift(SqWv,ind-ant-1)'; % Wrap appropriately for synthesis
end
X=[X;ones(1,SqWvPer)]; % Include the bias
Y=Qmat*X;Y=Y(:); % Synthesize the modulated square wave, put into one column
avgpos=[0.4*SqWvPer/2*OverSampleRate:0.6*SqWvPer/2*OverSampleRate]; % samples to average over
ZeroLevel=mean(Y(round(avgpos),:)); % Average over middle 20% of "zero" run
% Average over middle 20% of "one" run, compute OMA
MeasuredOMA=mean(Y(round(SqWvPer/2*OverSampleRate+avgpos),:))-ZeroLevel;
%% Subtract zero level and normalize OMA
yout0 = (yout0-ZeroLevel)/MeasuredOMA;

%% Compute the noise autocorrelation sequence at the output of the front-end antialiasing filter and
%% rate-2/T sampler.
Snn = N0/2 * fftshift(abs(H_r).^2) * 1/SymbolPeriod * OverSampleRate;
Rnn = real(ifft(Snn));
Corr = Rnn(1:OverSampleRate/2:end);
C = toeplitz(Corr(1:EqNf));

%% Compute the minimum slicer MSE and corresponding TWDP for the three stressor fibers
X = toeplitz(XmitData, [XmitData(1); XmitData(end:-1:2)]); % Used in MSE calculation
Rxx = X'*X; % Used in MSE calculation
TrialTWDP = [];
for ii=1:3 % index for stressor fiber
   %% Propagate the waveform through fiber ii.
   %% The DC response of each fiber is normalized to 1.
   PCoefs = FiberResp(ii+1,:)';
   Hsys = exp(ExpArg * Delays') * PCoefs; Hx = fftshift(Hsys/sum(PCoefs));
   yout = real(ifft(fft(yout0).*Hx));
   %% Process signal through front-end antialiasing filter %%%%%%%%%%%%%%%%%%%%
   yout = real(ifft(fft(yout) .* fftshift(H_r)));
   %% Compute MMSE-DFE %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
   %% The MMSE-DFE filter coefficients computed below minimize mean-squared error at the slicer input.
   %% The derivation follows from the fact that the slicer input over the period of the data sequence can be
   %% expressed as Z = (R+N)*W - X*[0 B]', where R and N are Toeplitz matrices constructed from the
   %% signal and noise components, respectively, at the sampled output of the antialiasing filter, W is the
   %% feedforward filter, X is a Toeplitz matrix constructed from the input data sequence, and B is the
   %% feedback filter. The computed W and B minimize the mean square error between the input to the
```


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```
   %% slicer and the transmitted sequence due to residual ISI and Gaussian noise. Minimize MSE over 2/T
   %% sampling phase and FFE delay and determine BER
   MseOpt = Inf;
   for jj= [0:OverSampleRate-1]-OverSampleRate/2 % sampling phase
      %% Sample at rate 2/T with new phase (wrap around as required)
      yout_2overT = yout(mod([1:OverSampleRate/2:TotLen]+jj-1,TotLen)+1);
      Rout = toeplitz(yout_2overT, [yout_2overT(1); yout_2overT(end:-1:end-EqNf+2)]);
      R = Rout(1:2:end, :);
      RINV = inv([R'*R+PtrnLength*C R'*ONE;ONE'*R PtrnLength]);
      R=[R ONE]; % Add all-ones column to compute optimal offset
      Rxr = X'*R; Px_r = Rxx - Rxr*RINV*Rxr';
      %% Minimize MSE over equalizer delay
      for kk = 1:length(EqDelVec)
         EqDel = EqDelVec(kk);
         SubRange = [EqDel+1:EqDel+EqNb+1];
         SubRange = mod(SubRange-1,PtrnLength)+1;
         P = Px_r(SubRange,SubRange);
         P00 = P(1,1); P01 = P(1,2:end); P11 = P(2:end,2:end);
         Mse = P00 - P01*inv(P11)*P01';
         if (Mse<MseOpt)
            MseOpt = Mse;
            B = -inv(P11)*P01'; % Feedback filter
            XSel = X(:,SubRange);
            W = RINV*R'*XSel*[1;B]; % Feedforward filter
            Z = R*W - XSel*[0;B]; % Input to slicer
            %% STEP 6 - Compute BER using semi-analytic method %%%%%%%%%%%%%%%%%%%
            MseGaussian = W(1:end-1)'*C*W(1:end-1);
            Ber = mean(0.5*erfc((abs(Z-0.5)/sqrt(MseGaussian))/sqrt(2)));
         end
      end
   end

   %% Compute equivalent SNR %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
   %% This function computes the inverse of the Gaussian error probability function. The
   %% built-in function erfcinv() is not sensitive enough for low probability of error cases.
   if Ber>10^(-12) Q = sqrt(2)*erfinv(1-2*Ber);
   elseif Ber>10^(-323) Q = 2.1143*(-1.0658-log10(Ber)).^0.5024;
   else Q = inf;
   end

   %% Compute penalty %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
   RefSNR = 10 * log10(Q0) + PAlloc;
   TrialTWDP(ii) = RefSNR-10*log10(Q);
end

%% Pick highest value due to the multiple fiber responses from TrialTWDP.
TWDP = max(TrialTWDP)
%% End of program
```

68.6.7 Transmitter signal to noise ratio

The system under test shall meet the RIN_xOMA specification, given in Table 68–3 as $RIN_{20}OMA$, when measured using the procedure given in 58.7.7. A different measurement procedure for the same quantity, giving approximately the same results, uses the setup shown in Figure 68–8 and proceeds as follows:

a) Measure OMA, using a square wave and following the method of 68.6.2

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b) Using the same square wave, measure the rms noise over flat regions of the logic ONE and logic ZERO portions of the square wave, as indicated in Figure 68–4, compensating for noise in the measurement system. The optical path and detector combination are configured for a single dominant reflection with the reflector adjusted to produce an optical return loss, as seen by the system under test, equal to the optical return loss tolerance (min) specified in Table 68–3. The length of the single-mode fiber is not critical, but should be in excess of 2 m. The polarization rotator is capable of transforming an arbitrary orientation elliptically polarized wave into a fixed orientation linearly polarized wave, and should be adjusted to maximize the noise. The receiver of the system under test should be receiving a signal that is asynchronous to that being transmitted. If possible, means should be used to prevent noise of frequency less than 1 MHz from affecting the result. Q_{sq} is given by Equation (68–2):

$$Q_{sq} = \frac{\text{OMA}}{\text{logic ONE noise (rms)} + \text{logic ZERO noise (rms)}} \tag{68–2}$$

where OMA and rms noise are measured in the same linear units of optical power, for example mW.

c) RIN_xOMA is then computed using the relationship shown in Equation (68–3):

$$RIN_xOMA = -20 \times \log_{10}(Q_{sq}) - 10 \times \log_{10}(BW) \quad \text{dB/Hz} \tag{68–3}$$

where BW is the low-pass bandwidth of oscilloscope minus high-pass bandwidth of the measurement system. For the specified measurement setup, BW is approximately 7.5×10^9 Hz.

Q_{sq} may be computed from the RIN_xOMA using the relationship shown in Equation (68–4):

$$Q_{sq} = 10^{-RINxOMA/20} / \sqrt{BW} \tag{68–4}$$

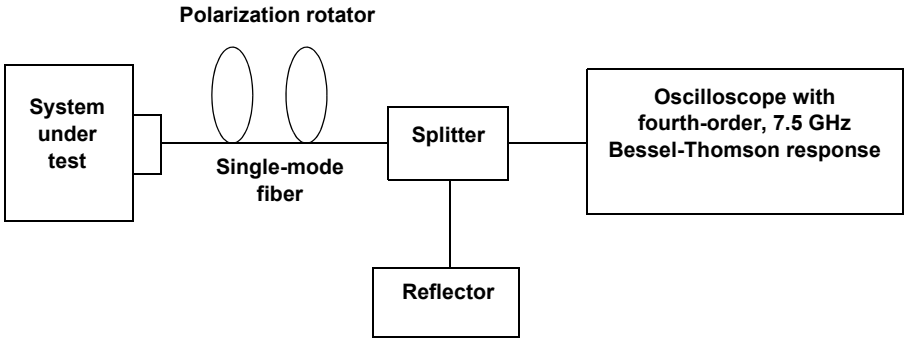

Figure 68–8—Transmitter signal to noise measurement setup

68.6.8 Transmitter uncorrelated jitter

Uncorrelated jitter refers to the component of jitter in the transmitted optical signal that is not correlated to the transmitter data.

The uncorrelated jitter specification of Table 68–3 shall be met when measured using an oscilloscope with a fourth-order, 7.5 GHz Bessel-Thomson response. The test pattern specified in Table 68–6 is used. A clock recovery unit (CRU) should be used to trigger the oscilloscope as shown in Figure 52–9. It should have a high frequency corner bandwidth of 4 MHz and a slope of –20 dB/decade. The CRU tracks acceptable levels

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of low-frequency jitter and wander. The oscilloscope is to be synchronized to the data pattern. The receiver of the system under test should be receiving a signal that is asynchronous to that being transmitted.

Figure 68–9 illustrates two measurement window positions, one on a rising edge, the other on a falling edge and both placed at the average power level of the pattern. The uncorrelated jitter (rms) is given by the RMS value of the standard deviations of the two distributions, as shown in Equation (68–5):

$$\text{Uncorrelated jitter (rms)} = \sqrt{(\sigma_r^2 + \sigma_f^2)/2} \tag{68–5}$$

where

σ_r is the standard deviation of the jitter on the rising edge

σ_f is the standard deviation of the jitter on the falling edge

Compensation for measurement system jitter is encouraged.

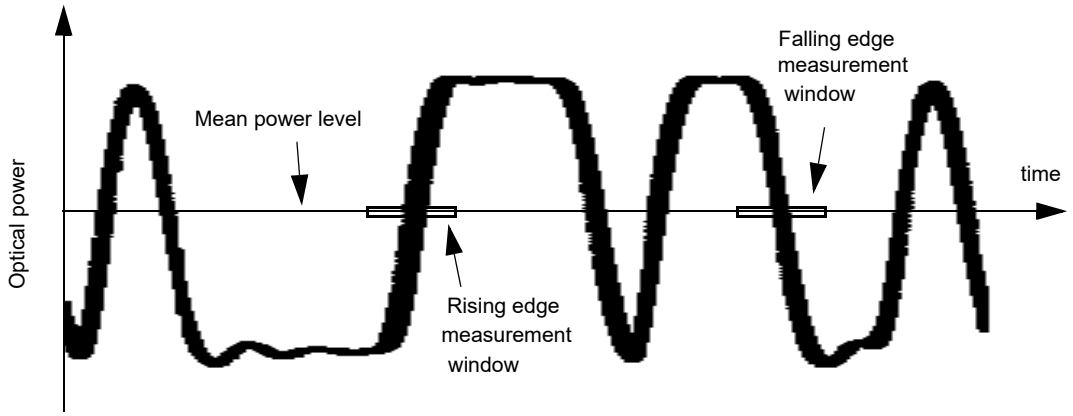

Figure 68–9—Measurement windows for transmitter uncorrelated jitter

68.6.9 Comprehensive stressed receiver sensitivity and overload

The PMD's receiver shall satisfy the comprehensive stressed receiver sensitivity and comprehensive stressed receiver overload specifications given in Table 68–5. These parameters are defined by reference to the procedures of 68.6.9.1 to 68.6.9.4. A BER of better than 10^{-12} shall be achieved with asynchronous transmission from the system under test. The received and transmitted patterns are the same, and as specified in Table 68–6 for the comprehensive stressed receiver sensitivity and the comprehensive stressed receiver overload.

68.6.9.1 Comprehensive stressed receiver sensitivity and overload test block diagram

Figure 68–10 shows the reference block diagram for the comprehensive stressed receiver test. As shown in the figure, an electrical signal is created using a pattern generator with pattern according to Table 68–6, and impaired by the following:

Gaussian low-pass filter

a) Gaussian white noise source
b) Intersymbol interference (ISI)

NOTE—Gaussian noise that extends, positively and negatively, to at least seven times its rms value is adequate.

The resulting electrical signal is converted to an optical signal using a linear electrical/optical converter, and the optical waveform is connected to an optical attenuator, and to the receiver under test via a mode-conditioning patch cord of the type defined in 38.11.4 or 59.9.5 for use with 62.5/125 μm fiber.

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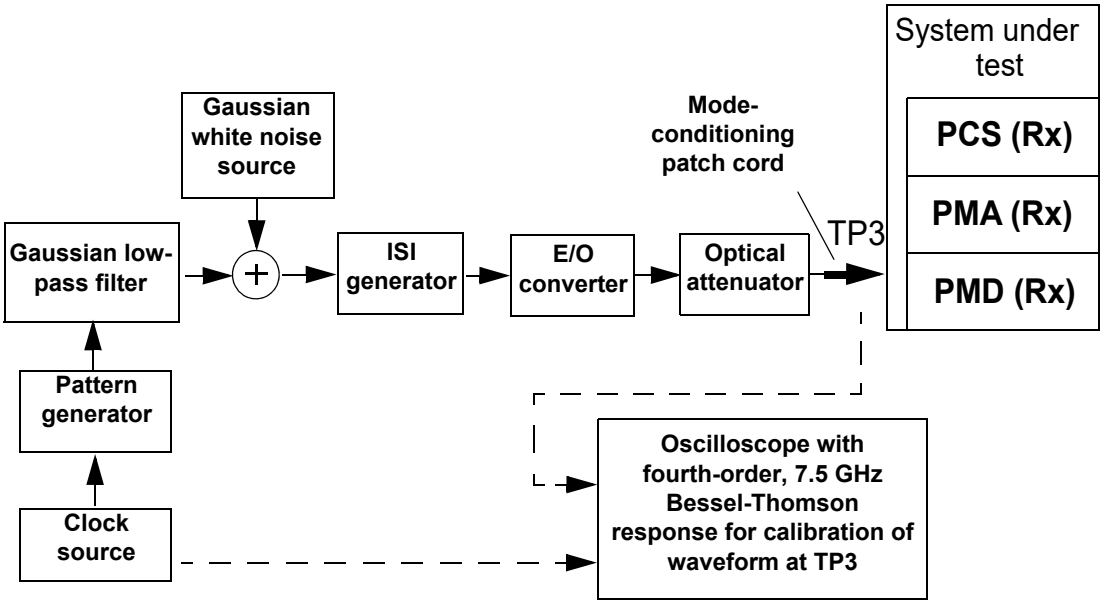

Figure 68–10—Reference measurement configuration for comprehensive stressed receiver sensitivity and overload test

The characteristics of the stressed test signal are defined in 68.6.9.2 and are based upon the parameters in Table 68–5. These parameters and the definition in 68.6.9.2 describe an ISI generator as a tapped delay line with four weighted taps, having equally spaced delays and with impulse response as illustrated in Figure 68–11.

Any implementation of the measurement configuration may be used, provided that the resulting signal and noise in the optical domain match those defined here. This consideration includes the shaping of the noise by the ISI generator.

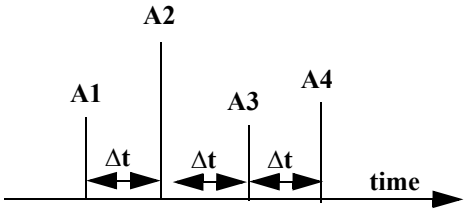

Figure 68–11—Illustration of parameters defining ISI generator impulse responses

68.6.9.2 Comprehensive stressed receiver test signal characteristics

The comprehensive stressed receiver test signal impairments are specified in Table 68–5 as the conditions of the comprehensive stressed receiver tests. These conditions include three sets of ISI parameters that are applied in turn. The ISI impaired test signal is defined by Equation (68–6):

$$S_{\mathrm{ISI}}(t) = S(t) * G_{47}(t) * \left[\sum_{i=1}^{4} A_i \times \delta(t - i \times \Delta t) \right] \tag{68–6}$$

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where

$S(t)$ is an ideal NRZ test pattern signal specified in Table 68–6
$G_{47}(t)$ is a Gaussian low-pass filter with a 20% to 80% step response of 47 ps
A_i are the amplitudes of the four impulses
Δt is their spacing
δ is the Dirac delta function
* denotes convolution

The impulse spacing, and the amplitudes of the impulses for the three different test cases, are specified in Table 68–5.

The test signal is also impaired by broadband white Gaussian noise with a minimum bandwidth specified in Table 68–5 and with the amplitude adjusted such that Q_{sq} of the test signal, without ISI impairment, is as specified in Table 68–5.

Two different optical signal powers, in OMA, are used for the comprehensive stressed receiver sensitivity test. For the test with pre-cursor ISI tap weights, and the test with the post-cursor ISI tap weights, the OMA is set to the stressed sensitivity in OMA, given in Table 68–5. For the test with the symmetrical ISI tap weights, the OMA is set to the stressed sensitivity in OMA for symmetrical test, given in Table 68–5. For all three tests, the minimum extinction ratio specified in Table 68–3 is used.

For the comprehensive stressed receiver overload test, the OMA is set to the overload in OMA, given in Table 68–5, and with the maximum average power specified in Table 68–3.

68.6.9.3 Comprehensive stressed receiver test signal calibration

The test signal is calibrated as follows, using an optical reference receiver with a multimode compatible input and a 7.5 GHz fourth-order ideal Bessel-Thomson response.

The extinction ratio of the optical output is calibrated with the Gaussian low-pass filter but without the ISI generator.

Without ISI impairment due to the ISI generator, the level of the Gaussian noise is adjusted such that Q_{sq} is as specified in Table 68–5. See 68.6.7 for the definition of signal to noise ratio Q_{sq}.

The ISI generator is configured and calibrated for each of the three ISI cases specified in Table 68–5. The calibration of the ISI may be done with any portion of a repeating test signal. One convenient example is an isolated ONE bit with at least ten ZERO bits before and after. The ISI generator is adjusted such that the signal, S_{meas}, recorded on the reference receiver is given by Equation (68–7):

$$S_{meas}(t) = S_{cal}(t) * G_{47}(t) * \left[\sum_{i=1}^{4} A_i \times \delta(t - i \times \Delta t) \right] * BT4_{7.5GHz}(t) \quad (68–7)$$

where

S_{cal} is an ideal NRZ calibration test signal
G_{47}, A_i , Δt, and * are defined as in 68.6.9.2
$BT4_{7.5GHz}(t)$ is the impulse response of an ideal 7.5 GHz fourth-order Bessel-Thomson filter representing the optical reference receiver response

In practice, the bandwidth of, or need for, the Gaussian low-pass filter shown in block diagram of Figure 68–10 is determined by the characteristics of the signal source, ISI generator and E/O converter such that the final measured signal has the overall pulse response given by Equation (68–7).

Figure 68–12 illustrates the required measured test signals for the three cases specified in Table 68–5, where the test signal, S_{cal}, is a single ONE bit (rectangular pulse with 1 UI width) surrounded by ZEROs. Table 68–7 gives the tabulated amplitude vs. time for these curves.

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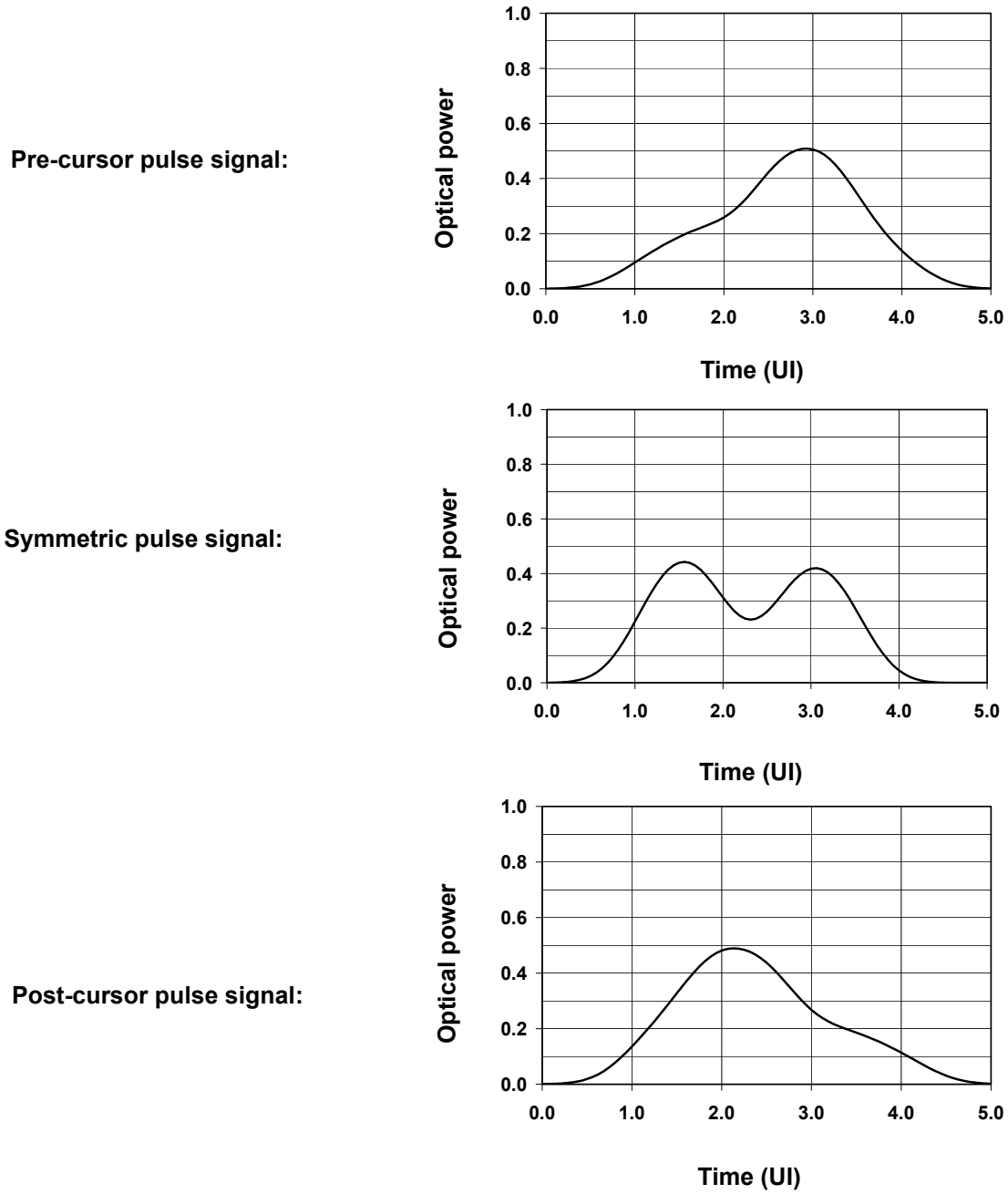

Figure 68–12—Comprehensive stressed receiver test pulse signals (i.e., signals corresponding to an isolated ONE bit)

NOTE—The optical powers have been normalized to correspond to waveforms with OMA of one.

NOTE—The TWDP values without simulated channels, which are measured using the same method as TWDP except that the simulated fiber stressors are set to (0,1,0,0), are 4.1 dB, 3.9 dB, and 4.2 dB for the pre-cursor, symmetrical and post-cursor tests, respectively. Significant differences from these values indicate problems with the test equipment (possibly nonlinearities) and that the test will not provide valid results. For small differences, the ISI generator should be adjusted to obtain the expected values. Also, one should ensure that the test system has adequate low-frequency response to avoid baseline wander problems with the longer test patterns used for the test.

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Table 68–7—Tabulated amplitude vs. time values for test signals of Figure 68–13

Time (UI)	Pre-cursor	Symmetrical	Post-cursor
0.000	0.000	0.000	0.000
0.125	0.001	0.001	0.001
0.250	0.003	0.004	0.003
0.375	0.008	0.011	0.009
0.500	0.016	0.026	0.019
0.625	0.029	0.053	0.036
0.750	0.048	0.095	0.061
0.875	0.071	0.154	0.095
1.000	0.096	0.224	0.136
1.125	0.121	0.298	0.180
1.250	0.146	0.364	0.227
1.375	0.168	0.413	0.276
1.500	0.189	0.439	0.327
1.625	0.207	0.439	0.378
1.750	0.223	0.413	0.423
1.875	0.239	0.367	0.459
2.000	0.259	0.312	0.481
2.125	0.288	0.264	0.489
2.250	0.327	0.235	0.484
2.375	0.374	0.234	0.467
2.500	0.422	0.261	0.437
2.625	0.464	0.305	0.398
2.750	0.494	0.355	0.352
2.875	0.508	0.395	0.307
3.000	0.506	0.417	0.268
3.125	0.487	0.415	0.238
3.250	0.451	0.388	0.216
3.375	0.402	0.338	0.200
3.500	0.344	0.273	0.186
3.625	0.284	0.203	0.171
3.750	0.228	0.137	0.154
3.875	0.180	0.084	0.135
4.000	0.138	0.046	0.114
4.125	0.103	0.022	0.091
4.250	0.072	0.009	0.069
4.375	0.048	0.003	0.048
4.500	0.029	0.001	0.031
4.625	0.016	0.000	0.018
4.750	0.007	0.000	0.009
4.875	0.003	0.000	0.004
5.000	0.001	0.000	0.001

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With the ISI generator present, the Q_{sq} values are as follows for the three different ISI impairments—precursor: 45.6; symmetrical: 37.2; post-cursor: 47.0. Significant differences from these values indicate problems with the test equipment (possibly noise sources within the ISI generator), and the test will not provide valid results. For small differences, the amplitude of the added Gaussian white noise should be adjusted to obtain the expected values.

The attenuator setting is determined by measuring the OMA of the impaired test signal according to 68.6.2.

68.6.9.4 Comprehensive stressed receiver test procedure

The three ISI impairments defined in Table 68–5 and 68.6.9.2, together with the appropriate OMA values, also as specified in Table 68–5, define six discrete signal conditions.

With the test system setup as described in 68.6.9.2 and 68.6.9.3, for each case, select the required ISI impairment and set the attenuator and Gaussian white noise source to obtain either the stressed sensitivity in OMA, stressed sensitivity in OMA for symmetrical test or overload in OMA, with the appropriate noise, as specified in Table 68–5. Set the pattern generator to one of the patterns specified in Table 68–6 for these measurements. Connect the test signal to the system receiver TP3 and a BER of better than 10^{-12} shall be achieved for each case.

68.6.10 Simple stressed receiver sensitivity and overload (optional)

The simple stressed receiver sensitivity and simple stressed receiver overload are optional and compliance is not required. If measured, the receiver under test will be expected to satisfy the simple stressed receiver sensitivity and simple stressed receiver overload specifications in Table 68–5.

Figure 68–13 gives the block diagram for the simple stressed receiver test. A pattern generator output is impaired by a low-pass filter and the resulting electrical signal is converted to an optical signal using a linear electrical/optical converter. Other signal impairments, such as jitter and RIN, should be negligible. The optical waveform is connected to an optical attenuator, and to the receiver under test via a mode-conditioning patch cord of the type defined in 38.11.4 or 59.9.5 for use with 62.5/125 μm fiber.

The filter should be chosen so as to produce an optical output with the rise and fall times given in Table 68–5, and dominated by a fourth-order Bessel-Thomson response. The rise and fall times of the test signal are defined as measured with a 7.5 GHz Bessel-Thomson reference receiver and with the square wave pattern used for calibrating OMA for the comprehensive stressed receiver test of 68.6.9.

Other implementations may be used provided that the resulting signal in the optical domain matches that created using the implementation described.

NOTE—The TWDP without simulated channels, which is measured using the same method as TWDP except that the simulated fiber stressors are set to (0, 1, 0, 0), for this test signal is 4 dB.

For the two OMA values (i.e., the stressed sensitivity in OMA, and the overload in OMA, both specified in Table 68–5), a BER of better than 10^{-12} should be achieved. For the simple stressed receiver sensitivity test, the minimum extinction ratio specified in Table 68–3 is used. For the simple stressed receiver overload test, the maximum average power specified in Table 68–3 is used.

68.6.11 Receiver jitter tolerance

The receiver jitter tolerance specification given in Table 68–5 shall be met when measured as described here. This specification addresses the need for the receiver to track low-frequency jitter without the occurrence of errors.

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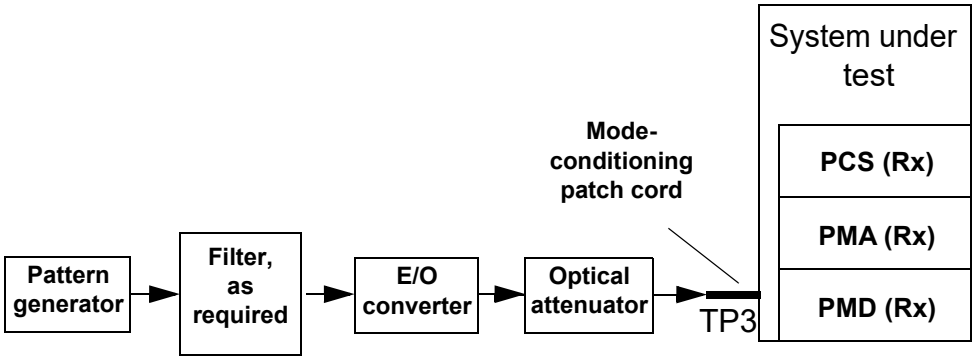

Figure 68–13—Measurement configuration for simple stressed receiver sensitivity test (optional)

Figure 68–14 gives the measurement configuration for the receiver jitter tolerance test. An optical pattern generator output is impaired by frequency modulation of the generating clock. The optical waveform is connected to the receiver under test via an optical attenuator and mode-conditioning patch cord suitable for 62.5/125 μm fiber.

Two jitter frequency and amplitude combinations are specified in Table 68–5. These are applied as the conditions of two separate receiver jitter tolerance tests. For each, the power in OMA at the receiver is adjusted, using the optical attenuator, to be equal to the stressed sensitivity in OMA, also given in Table 68–5, and a BER of better than 10^{-12} shall be achieved.

Various implementations may be used, provided that the resulting jitter in the optical domain matches that specified. Phase or frequency modulation may be applied to induce the sinusoidal jitter, and the modulation may be applied to the clock source or to the data stream itself.

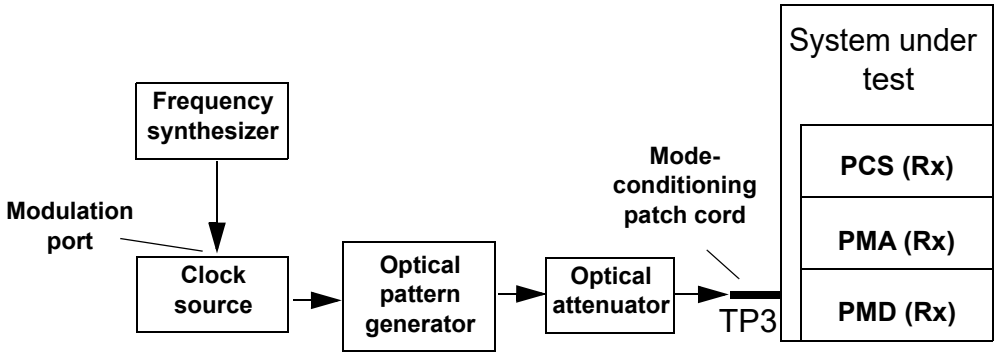

Figure 68–14—Measurement configuration for receiver jitter tolerance test

68.7 Safety, installation, environment, and labeling

68.7.1 Safety

The 10GBASE-LRM environmental specifications are as defined in 52.10.1 for general safety, and as defined in 52.10.2 for laser safety.

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68.7.2 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

NOTE—The preferred launch (as specified in Table 68–3) is expected to provide more stable operation. It is recommended that link stability be confirmed by physical manipulation of the transmitter patch cord.

68.7.3 Environment

The 10GBASE-LRM operating environment specifications are as defined in 52.11, as defined in 52.11.1 for electromagnetic emission, and as defined in 52.11.2 for temperature, humidity, and handling.

68.7.4 PMD labeling

The 10GBASE-LRM labeling recommendations and requirements are as defined in 52.12.

68.8 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 38–7.

A channel may contain additional connectors or other optical elements as long as the optical characteristics of the channel such as attenuation, dispersion, reflections, modal bandwidth and total connector loss meet the specifications. Insertion loss measurements of installed multimode fiber cables are made in accordance with IEC 61280-4-1 one-cord method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

68.9 Characteristics of the fiber optic cabling (channel)

The channel consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. The fiber optic cabling shall meet the requirements of Table 68–8.

Table 68–8—Fiber optic cabling (channel)

Description	Type	Value	Unit
Cabled optical fiber insertion loss at 1300 nm	max	0.4	dB
Losses of all connectors and splices	max	1.5	dB

68.9.1 Optical fiber and cable

The optical fiber shall meet the requirements of IEC 60793-2-10 and the requirements given in Table 68–9, where they differ. Multimode cables chosen from IEC 60794-2-11 or IEC 60794-3-12 may be suitable.

68.9.2 Optical fiber connections

An optical fiber connection, as shown in Figure 38–7, consists of a mated pair of optical connectors.

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Table 68–9—Optical fiber and cable

Description	Type	Value	Unit
Cabled optical fiber attenuation at 1300 nm	max	1.5	dB/km
Modal bandwidth at 1300 nm	min	Value used as 1300 nm modal bandwidth portion of fiber identifier in Table 68–2	MHz · km
Zero dispersion wavelength (λ_0) for 62.5 μm MMF	range	$1320 \le \lambda_0 \le 1365$	nm
Chromatic dispersion slope for 62.5 μm MMF	max	0.11 for $1320 \le \lambda_0 \le 1348$ and $0.001(1458 - \lambda_0)$ for $1348 \le \lambda_0 \le 1365$	ps/nm^2 · km
Zero dispersion wavelength (λ_0) for 50 μm MMF	range	$1295 \le \lambda_0 \le 1320$	nm
Chromatic dispersion slope for 50 μm MMF	max	0.11 for $1300 \le \lambda_0 \le 1320$ and $0.001(\lambda_0 - 1190)$ for $1295 \le \lambda_0 \le 1300$	ps/nm^2 · km

68.9.2.1 Connection insertion loss

The insertion loss is specified for a connection, which consists of a mated pair of optical connectors.

The maximum link distances for multimode fiber are calculated based on an allocation of 1.5 dB total connector and splice loss. For example, this allocation supports three connections with an insertion loss equal to 0.5 dB (or less) per connection, or two connections (as shown in Figure 38–7) with an insertion loss equal to 0.75 dB per connection. Connections with different loss characteristics may be used provided the requirements of Table 68–8 are met.

68.9.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –20 dB.

68.9.3 Single-mode fiber offset-launch mode-conditioning patch cord

Single-mode fiber offset-launch mode-conditioning patch cords shall satisfy the requirements of 38.11.4 or 59.9.5. Any discrete reflectance within the patch cord shall be less than –20 dB.

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68.10 Protocol implementation conformance statement (PICS) proforma for Clause 68, Physical medium dependent (PMD) sublayer type 10GBASE-LRM[132]

68.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3, Physical medium dependent (PMD) sublayer type 10GBASE-LRM, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

68.10.2 Identification

68.10.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

68.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 68, Physical medium dependent (PMD) sublayer type 10GBASE-LRM
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[132]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that if can be used for its intended purpose and may further publish the completed PICS.

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68.10.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*MD	MDIO capability	68.3	Registers and interface supported	O	Yes [ ] No [ ]
*INS	Installation / Cable	68.9	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
DLY	Delay constraints	68.2	Device conforms to delay constraints	M	Yes [ ]

68.10.3 PICS proforma tables for physical medium dependent (PMD) sublayer type 10GBASE-LRM

68.10.3.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Optical launch	68.4.1, 68.5.1	PMD supports both preferred and alternative launches	M	Yes [ ]
FS2	Transmit function	68.4.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FS3	Transmitter optical signal	68.4.2	Higher optical power transmitted is a logic 1	M	Yes [ ]
FS4	Receive function	68.4.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FS5	Receiver optical signal	68.4.3	Higher optical power received is a logic 1	M	Yes [ ]
FS6	Signal detect function	68.4.4	Mapping to PMD service interface	M	Yes [ ]
FS7	Signal detect parameter	68.4.4	Generated according to Table 68–1	M	Yes [ ]

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68.10.3.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MD1	Management register set	68.3	Mapped as per Table 52–3 and Table 52–4	MD:M	Yes [ ] N/A [ ]
MD2	PMD_reset bit	68.4.5, 45.2.1.1.1		MD:M	Yes [ ] N/A[ ]
MD3	PMD_global_transmit_disable bit	68.4.7, 45.2.1.8.7		MD:O	Yes [ ] No [ ] N/A [ ]
MD4	PMD_transmit_fault bit	68.4.8, 45.2.1.7.4		MD:O	Yes [ ] No [ ] N/A [ ]
MD5	PMD receive fault bit	68.4.9, 45.2.1.7.5		MD:O	Yes [ ] No [ ] N/A [ ]
MD6	PMD fault bit	68.4.6		MD:O	Yes [ ] No [ ] N/A [ ]
MD7	PMD_signal_detect bit	68.4.4, 45.2.1.9.7		MD:M	Yes [ ] N/A [ ]

68.10.3.3 PMD to MDI optical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
LRM1	10GBASE-LRM transmitter	68.5.1	Meets specifications in Table 68–3	M	Yes [ ]
LRM2	10GBASE-LRM receiver	68.5.3	Meets specifications in Table 68–5	M	Yes [ ]

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68.10.3.4 Definitions of optical parameters and measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Optical modulation amplitude	68.6.2		M	Yes [ ]
OM2	Extinction ratio	68.6.3		M	Yes [ ]
OM3	Transmitter optical wave-form— transmitter eye mask	68.6.5		M	Yes [ ]
OM4	Transmitter optical wave-form— transmitter waveform and dispersion penalty (TWDP)	68.6.6		M	Yes [ ]
OM5	Transmitter signal to noise ratio	68.6.7		M	Yes [ ]
OM6	Transmitter uncorrelated jitter	68.6.8		M	Yes [ ]
OM7	Comprehensive stressed receiver sensitivity	68.6.9		M	Yes [ ]
OM8	Comprehensive stressed receiver overload	68.6.9		M	Yes [ ]
OM9	Simple stressed receiver sensitivity	68.6.10		O	Yes [ ] No [ ]
OM10	Simple stressed receiver overload	68.6.10		O	Yes [ ] No [ ]
OM11	Receiver jitter tolerance	68.6.11		M	Yes [ ]

68.10.3.5 Safety, installation, environment, and labeling

Item	Feature	Subclause	Value/Comment	Status	Support
SE1	General safety	68.7.1	As 52.10.1. Conforms to IEC-60950-1	M	Yes [ ]
SE2	Laser safety — IEC Hazard Level 1	68.7.1	As 52.10.2. Conform to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
SE3	Electromagnetic interference	68.7.3	As 52.11.1. Comply with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]
SE4	PMD labeling	68.7.4	As 52.12.	M	Yes [ ]

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68.10.3.6 Characteristics of the fiber optic cabling (channel)

Item	Feature	Subclause	Value/Comment	Status	Support
FO1	Characteristics of fiber optic cabling (channel)	68.9	Meet the requirements of	INS:M	Yes [ ] N/A [ ]
FO2	Optical fiber characteristics	68.9.1	Meet the requirements given, including those of Table 68–9	INS:M	Yes [ ] N/A [ ]
FO3	Optical fiber connections	68.9.2	Insertion loss within specification of 68.9.2.1	INS:M	Yes [ ] N/A [ ]
FO4	Patch cords	68.9.3		INS:M	Yes [ ] N/A [ ]

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69. Introduction to Ethernet operation over electrical backplanes

69.1 Overview

69.1.1 Scope

Ethernet operation over electrical backplanes, also referred to as “Backplane Ethernet,” combines the IEEE 802.3 Media Access Control (MAC) and MAC Control sublayers with a family of Physical Layers defined to support operation over a modular chassis backplane.

Backplane Ethernet supports the IEEE 802.3 full duplex MAC operating at 1000 Mb/s, 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, or 200 Gb/s. The following Physical Layers are supported:

— 1000BASE-KX for 1 Gb/s operation over a single lane
— 2.5GBASE-KX for 2.5 Gb/s operation over a single lane
— 5GBASE-KR for 5 Gb/s operation over a single lane
— 10GBASE-KX4 for 10 Gb/s operation over four lanes
— 10GBASE-KR for 10 Gb/s operation over a single lane
— 25GBASE-KR and 25GBASE-KR-S for 25 Gb/s operation over a single lane
— 40GBASE-KR4 for 40 Gb/s operation over four lanes
— 50GBASE-KR for 50 Gb/s operation over a single lane
— 100GBASE-KR4 and 100GBASE-KP4 for 100 Gb/s operation over four lanes
— 100GBASE-KR2 for 100 Gb/s operation over two lanes
— 200GBASE-KR4 for 200 Gb/s operation over four lanes

Auto-Negotiation enables PHY selection amongst Backplane Ethernet Physical Layer signaling systems.

Energy Efficient Ethernet (EEE) is optionally supported for all Backplane Ethernet PHYs.

69.1.2 Relationship of Backplane Ethernet to the ISO OSI reference model

Backplane Ethernet couples the IEEE 802.3 MAC to a family of Physical Layers defined for operation over electrical backplanes. The relationships among Backplane Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 69–1, Figure 69–2, Figure 69–3, Figure 69–4, and Figure 69–5.

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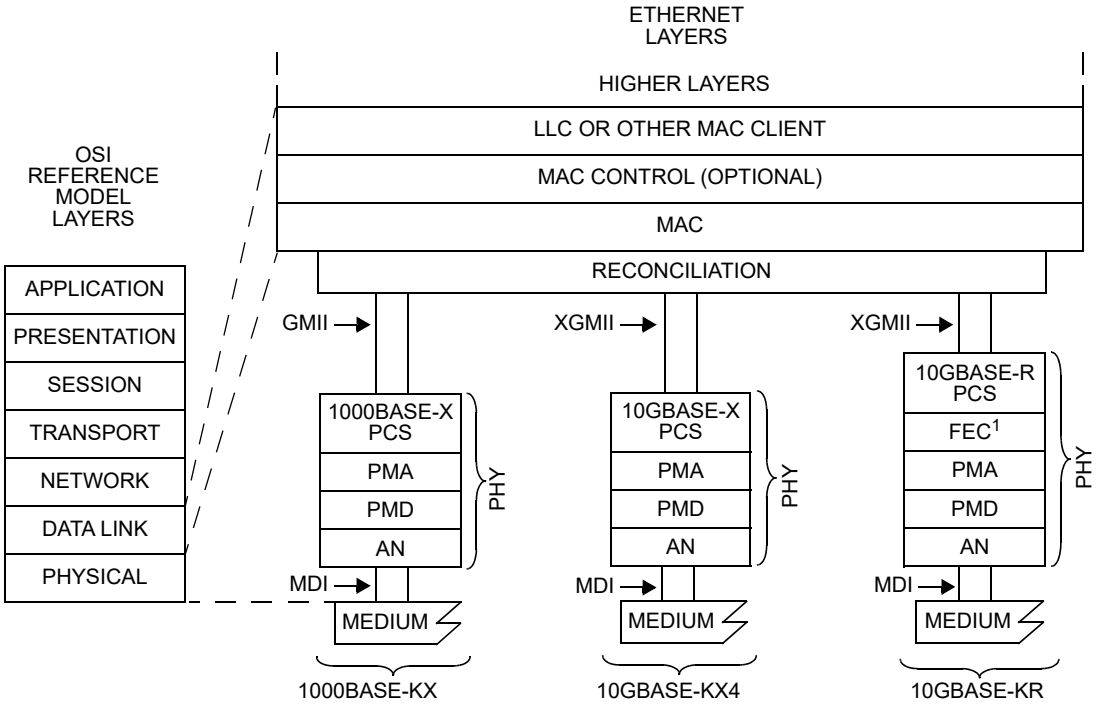

AN = AUTO-NEGOTIATION
FEC = FORWARD ERROR CORRECTION
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE

NOTE 1—OPTIONAL

Figure 69–1—Architectural positioning of 1 Gb/s and 10 Gb/s Backplane Ethernet

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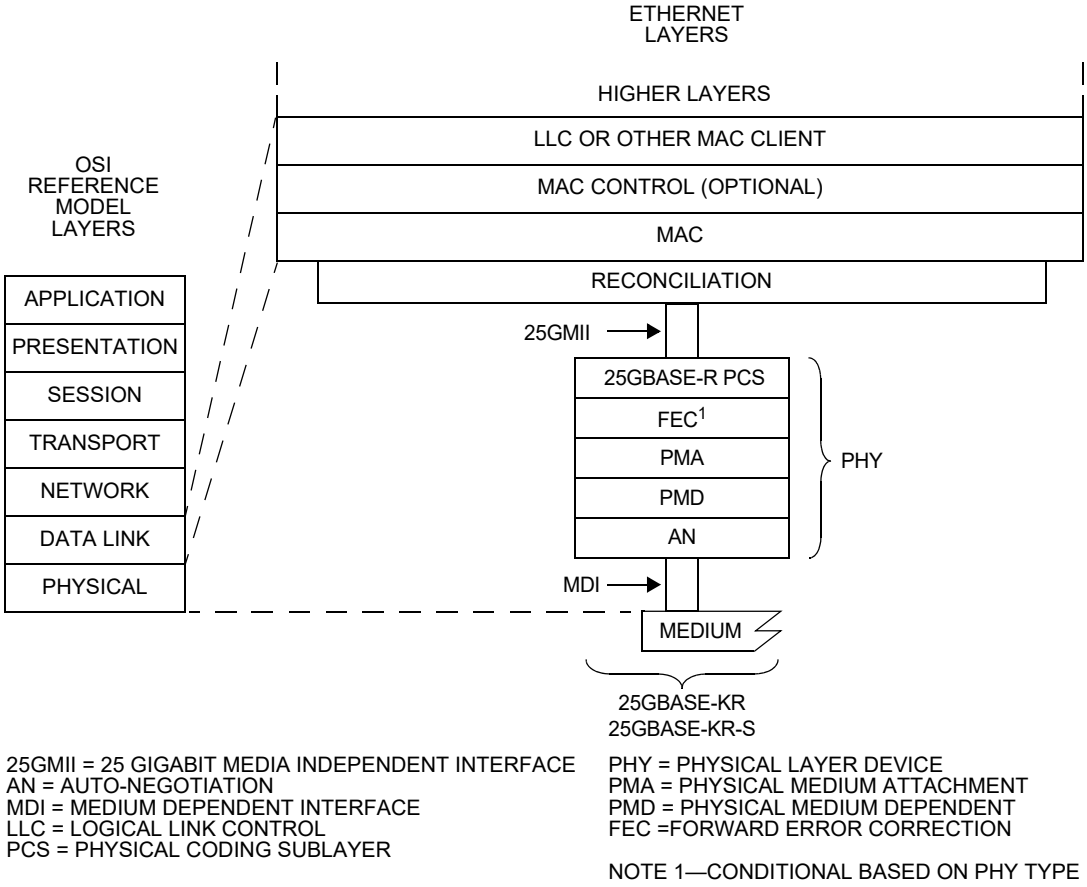

Figure 69–2—Architectural positioning of 25 Gb/s Backplane Ethernet

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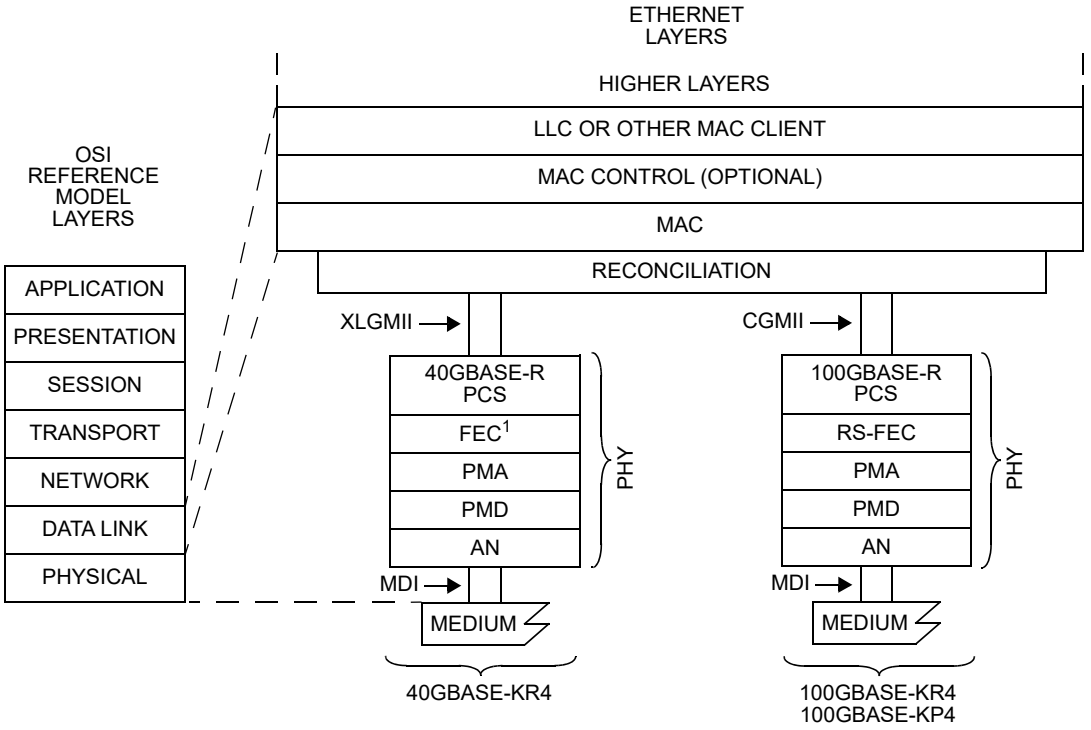

AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FEC
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—OPTIONAL

Figure 69–3—Architectural positioning of 40 Gb/s and 100 Gb/s Backplane Ethernet

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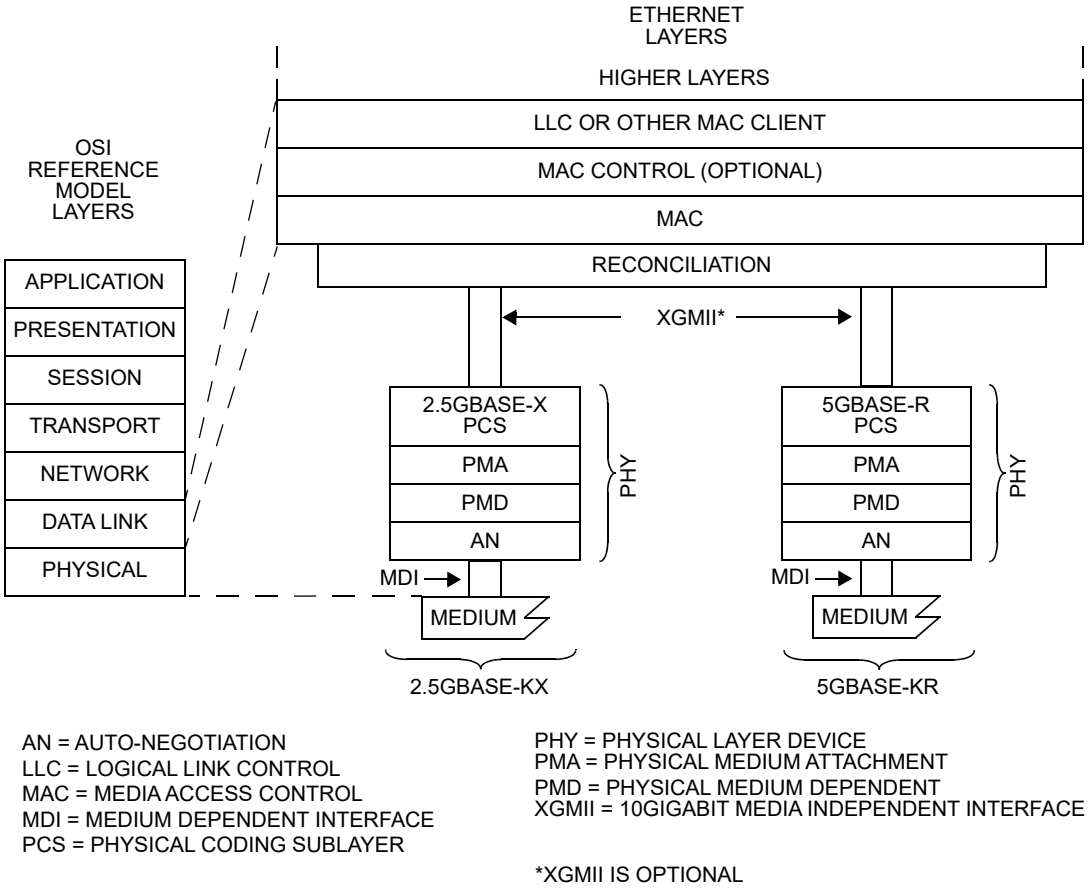

Figure 69–4—Architectural positioning of 2.5 Gb/s and 5 Gb/s Backplane Ethernet

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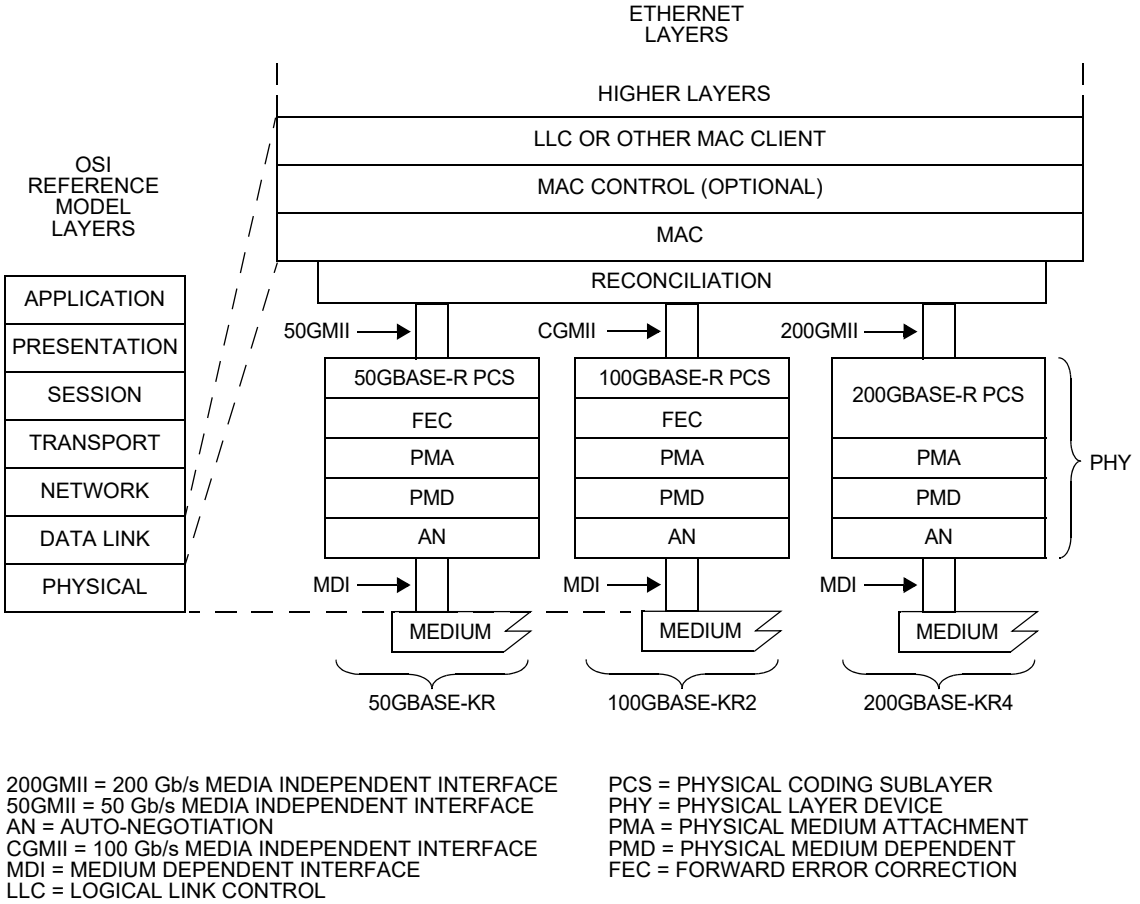

Figure 69–5—Architectural positioning of 50 Gb/s, 100 Gb/s, and 200 Gb/s PAM4 Backplane Ethernet

While this specification defines interfaces in terms of bits, octets, and frames, implementers may choose other data-path widths for implementation convenience. Exceptions are described in the clauses related to specific Backplane Ethernet PHY types.

69.2 Summary of Backplane Ethernet Sublayers

69.2.1 Reconciliation sublayer and media independent interfaces

The Clause 35 RS and GMII, the Clause 46 RS and XGMII, the Clause 106 RS and 25GMII, the Clause 81 RS, XLGMII, and CGMII, the Clause 132 RS and 50GMII, and the Clause 117 RS and 200GMII are employed for the same purpose in Backplane Ethernet, that being the interconnection between the MAC sublayer and the PHY.

69.2.2 Management interface

The MDIO/MDC management interface (Clause 45) is intended to provide an interconnection between MDIO Manageable Devices (MMD) and Station Management (STA) entities.

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69.2.3 Physical Layer signaling systems

Backplane Ethernet extends the family of 1000BASE-X Physical Layer signaling systems to include 1000BASE-KX. This embodiment specifies operation at 1 Gb/s over two differential, controlled impedance pairs of traces (one pair for transmit, one pair for receive). This system employs the 1000BASE-X PCS and PMA as defined in Clause 36. The 1000BASE-KX PMD is defined in Clause 70.

Backplane Ethernet also extends the family of 2.5GBASE-X Physical Layer signaling systems to include 2.5GBASE-KX. This embodiment specifies operation at 2.5 Gb/s over two differential, controlled impedance pairs of traces (one pair for transmit, one pair for receive). This system employs the 2.5GBASE-X PCS and PMA as defined in Clause 127. The 2.5GBASE-KX PMD is defined in Clause 128.

Backplane Ethernet also extends the family of 5GBASE-R Physical Layer signaling systems to include 5GBASE-KR. This embodiment specifies 5 Gb/s operation over two differential, controlled impedance pairs of traces (one pair for transmit, one pair for receive). This system employs the 5GBASE-R PCS and PMA as defined in Clause 129. The 5GBASE-KR PMD is defined in Clause 130.

Backplane Ethernet also extends the family of 10GBASE-X Physical Layer signaling systems to include 10GBASE-KX4. This embodiment is based on XAUI with 10GBASE-CX4 extensions and specifies 10 Gb/s operation over four differential paths in each direction for a total of eight pairs. This system employs the 10GBASE-X PCS and PMA as defined in Clause 48. The 10GBASE-KX4 PMD is defined in Clause 71.

Backplane Ethernet also extends the family of 10GBASE-R Physical Layer signaling systems to include the 10GBASE-KR. This embodiment specifies 10 Gb/s operation over two differential, controlled impedance pairs of traces (one pair for transmit, one pair for receive). This system employs the 10GBASE-R PCS as defined in Clause 49 and the serial PMA as defined in Clause 51. The 10GBASE-KR PMD is defined in Clause 72. The 10GBASE-KR PHY may optionally include 10GBASE-R forward error correction (FEC), as defined in Clause 74.

Backplane Ethernet also specifies 25GBASE-KR and 25GBASE-KR-S. The 25GBASE-KR embodiment employs the PCS defined in Clause 107, the BASE-R FEC defined in Clause 74, the RS-FEC defined in Clause 108, the PMA defined in Clause 109, and the PMD defined in Clause 111, and specifies 25 Gb/s operation over one differential path in each direction. The 25GBASE-KR-S embodiment employs the PCS defined in Clause 107, the BASE-R FEC defined in Clause 74, the PMA defined in Clause 109, and the PMD defined in Clause 111, and specifies 25 Gb/s operation over one differential path in each direction.

Backplane Ethernet also specifies 40GBASE-KR4. This embodiment employs the PCS defined in Clause 82, the PMA defined in Clause 83, and the PMD defined in Clause 84 and specifies 40 Gb/s operation over four differential paths in each direction for a total of eight pairs.

Backplane Ethernet also specifies 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4. The 50GBASE-KR embodiment employs the PCS defined in Clause 133, the RS-FEC defined in Clause 134, the PMA defined in Clause 135, and the PMD defined in Clause 137, and specifies 50 Gb/s operation using 4-level PAM over one differential path in each direction. The 100GBASE-KR2 embodiment employs the PCS defined in Clause 82, the RS-FEC defined in Clause 91, the PMA defined in Clause 135, and the PMD defined in Clause 137, and specifies 100 Gb/s operation using 4-level PAM over two differential paths in each direction. The 200GBASE-KR4 embodiment employs the PCS defined in Clause 119, the PMA defined in Clause 120, and the PMD defined in Clause 137, and specifies 200 Gb/s operation using 4-level PAM over four differential paths in each direction.

Backplane Ethernet also specifies 100GBASE-KR4 for 100 Gb/s operation using 2-level pulse amplitude modulation (PAM) over four differential signal pairs in each direction for a total of eight pairs where the insertion loss of each pair does not exceed 35 dB at 12.9 GHz. The embodiment of 100GBASE-KR4

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employs the PCS defined in Clause 82, the RS-FEC defined in Clause 91, the PMA defined in Clause 83, and the PMD defined in Clause 93.

Backplane Ethernet also specifies 100GBASE-KP4 for 100 Gb/s operation using 4-level PAM over four differential signal pairs in each direction for a total of eight pairs where the insertion loss of each pair does not exceed 33 dB at 7 GHz. The embodiment of 100GBASE-KP4 employs the PCS defined in Clause 82, the RS-FEC defined in Clause 91, and the PMA and PMD defined in Clause 94.

Table 69–1 specifies the correlation between nomenclature and clauses for 1 Gb/s and 10 Gb/s backplane Ethernet. For other backplane PHY types, refer to Table 125–2 (2.5 Gb/s and 5 Gb/s), Table 105–1 (25 Gb/s), Table 80–2 (40 Gb/s), Table 131–2 (50 Gb/s), Table 80–3 (100 Gb/s), and Table 116–3 (200 Gb/s).

Table 69–1—Nomenclature and clause correlation for 1 Gb/s and 10 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause													
	35		36	46		48	49	51	70	71	72	73	74	78
	RS	GMII	1000BASE-X PCS/PMA	RS	XGMII	10GBASE-X PCS/PMA	10GBASE-R PCS	Serial PMA	1000BASE-KX PMD	10GBASE-KX4 PMD	10GBASE-KR PMD	Auto-Negotiation	BASE-R FEC	Energy-Efficient Ethernet (EEE)
1000BASE-KX	M[a]	O[a]	M						M			M		O
10GBASE-KX4				M	O	M				M		M		O
10GBASE-KR				M	O		M	M			M	M	O	O

[a]O = Optional, M = Mandatory

69.2.4 Auto-Negotiation

Auto-Negotiation provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation.

Auto-Negotiation for Backplane Ethernet is based on the Clause 28 definition of Auto-Negotiation for twisted-pair link segments. Auto-Negotiation for Backplane Ethernet utilizes an extended Base Page and Next Page format and modifies the timers to allow rapid convergence. Furthermore, Auto-Negotiation does not utilize Fast Link Pulses (FLPs) for link codeword signaling and instead uses a signaling more suitable for electrical backplanes.

Auto-Negotiation for Backplane Ethernet is defined in Clause 73.

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69.2.5 Management

Managed objects, attributes, and actions are defined for all Backplane Ethernet components. These items are defined in Clause 30.

69.2.6 Low-Power Idle

With the optional EEE feature, described in Clause 78, Backplane Ethernet PHYs can achieve lower power consumption during periods of low link utilization. The EEE capabilities are advertised during Auto-Negotiation for Backplane Ethernet. The Backplane Ethernet LPI allows each link direction to enter sleep, refresh, or wake states asymmetric from the other direction.

69.3 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

Table 69–2 contains the values of maximum sublayer round-trip (sum of transmit and receive) delay for the 1000BASE-KX port types in bit time as specified in 1.4.

Table 69–2—Round-trip delay constraints for 1000BASE-KX

Sublayer	Maximum (bit time)	Notes
MAC Control, MAC, and RS	696	
1000BASE-X PCS, PMA, and PMD	328	See 36.5.1
Medium	16	See 70.4
Total delay	1040[a]	

[a]Per 31B.3.7, a station incorporating the 1000BASE-KX PHY will not begin to transmit a new frame more than two pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

Table 69–3 contains the values of maximum sublayer round-trip (sum of transmit and receive) delay for the 10GBASE-KX4 and 10GBASE-KR port types in bit time as specified in 1.4 and pause_quanta as specified in 31B.2.

For 2.5GBASE-KX, normative delay specifications may be found in 127.5 and 128.4. For 5GBASE-KR, normative delay specifications may be found in 129.5 and 130.4. They are also referenced in 125.3.

For 25GBASE-KR and 25GBASE-KR-S, normative delay specifications may be found in 106.1.4, 107.4, 109.5, and 111.4, and also referenced in 105.5.

For 40GBASE-KR4, normative delay specifications may be found in 81.1.4, 82.5, 83.5.4, and 84.4 and also referenced in 80.4.

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For 50GBASE-KR, normative delay specifications may be found in 132.1.4, 133.3, 135.5.4, and 137.5, and also referenced in 131.4.

For 100GBASE-KR4, normative delay specifications may be found in 81.1.4, 82.5, 83.5.4, 91.4, and 93.4 and also referenced in 80.4.

For 100GBASE-KP4, normative delay specifications may be found in 81.1.4, 82.5, 91.4, and 94.3.3 and also referenced in 80.4.

For 100GBASE-KR2, normative delay specifications may be found in 81.1.4, 82.5, 135.5.4, and 137.5, and also referenced in 80.4.

For 200GBASE-KR4, normative delay specifications may be found in 117.1.4, 119.5, 120.5.4, and 137.5, and also referenced in 116.4.

Table 69–3—Round-trip delay constraints for 10GBASE-KX4 and 10GBASE-KR

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Notes
MAC Control, MAC, and RS	8192	16	See 46.1.4
XGXS and XAUI	4096	8	Round-trip of 2 XGXS and trace for both directions, see 47.2.2
10GBASE-X PCS and PMA	2048	4	See 48.5
10GBASE-R PCS	3584	7	See 49.2.15
10GBASE-R FEC	6144	12	See 74.6
10GBASE-KX4 PMD[a]	512	1	See 71.3
10GBASE-KR PMA and PMD[a]	1024	2	See 72.4

[a]The 10GBASE-KX4 PMD and 10GBASE-KR PMA and PMD delays include the delay associated with the backplane medium.

69.4 State diagrams

In the case of any ambiguity between the text and the state diagrams, the state diagrams take precedence.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

69.5 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 70 through Clause 74, Clause 84, Clause 91, Clause 93, Clause 94, Clause 108, Clause 111, Clause 119, Clause 128, Clause 130, Clause 134, Clause 137, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each

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clause as appropriate. Each of the Backplane Ethernet PICS uses the notation and conventions specified in 21.6.

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70. Physical Medium Dependent sublayer and baseband medium, type 1000BASE-KX

70.1 Overview

This clause specifies the 1000BASE-KX PMD and baseband medium. When forming a complete PHY, a PMD shall be combined with the appropriate sublayers (see Table 70–1), and with the management functions that are optionally accessible through the management interface defined in Clause 45.

Table 70–1—Physical Layer clauses associated with the 1000BASE-KX PMD

Associated clause	1000BASE-KX
35—GMII[a]	Optional
36—1000BASE-X PCS/PMA	Required
73—Auto-Negotiation for Backplane Ethernet	Required
78—Energy-Efficient Ethernet	Optional

[a]The GMII is an optional interface. However, if the GMII is not implemented, a conforming implementation behaves functionally as though the RS and GMII were present.

The Clause 36 PCS/PMA when used with 1000BASE-KX PMD shall support full duplex operation only.

A 1000BASE-KX PHY with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization. The “Assert LPI” request at the GMII is encoded in the transmitted symbols. Detection of LPI signaling in the received symbols is indicated as “Assert LPI” at the GMII. Upon the detection of “Assert LPI” at the GMII, an energy-efficient 1000BASE-KX PHY continues transmitting for a predefined period, then ceases transmission and deactivates transmit functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g., timing recovery, adaptive filter coefficients) and thereby track long-term variations in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal interframes resume at the GMII, the PHY reactivates transmit functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the LPI mode.

70.2 Physical Medium Dependent (PMD) service interface

The 1000BASE-KX PMD performs the following three functions in support of the matching service interface primitives of 38.1.1: Transmit, Receive, and Signal Detect.

The PMD provides the following service interface signals if EEE is supported:

PMD_RXQUIET.request(rx_quiet)
PMD_TXQUIET.request(tx_quiet)

These messages signals are defined for the PCS in 36.2.5.1.6.

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70.2.1 PMD_RXQUIET.request

This primitive is generated by the PCS Receive Process when EEE is supported to indicate that the input signal is quiet and the PMA and PMD receiver may go into low power mode. See 36.2.4.13. When EEE is not supported, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

70.2.1.1 Semantics of the service primitive

PMD_RXQUIET.request (rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE.

70.2.1.2 When generated

The PCS generates this primitive to request the appropriate PMD receive LPI state.

70.2.1.3 Effect of receipt

This variable is from the receive process of the PCS to control the power-saving function of the local PMD receiver. The 1000BASE-KX PHY receiver should put unused functional blocks into a low power state to save energy.

70.2.2 PMD_TXQUIET.request

This primitive is generated by the PCS Transmit Process when EEE is supported to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. See 70.6.5. When EEE is not supported, the primitive is never invoked and the PMD behaves as if tx_quiet = FALSE.

70.2.2.1 Semantics of the service primitive

PMD_TXQUIET.request (tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE.

70.2.2.2 When generated

The PCS generates this primitive to request the appropriate PMD transmit LPI state.

70.2.2.3 Effect of receipt

This primitive affects operation of the PMD Transmit disable function as described in 70.6.5. The 1000BASE-KX PHY transmitter should put unused functional blocks into a lower power state to save energy.

70.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD shall support the AN service interface primitive AN_LINK.indication as defined in 73.9. (See 36.2.5.2.7.)

70.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control

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sublayer, and PHY implementers consider the delay maxima, and that network planners and administrators consider the delay constraints regarding the physical topology and concatenation of devices. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 69.3

The sum of transmit and receive delays contributed by the 1000BASE-KX PCS, PMA, and PMD shall be no more than 328 bit times. It is assumed that the round-trip delay through the medium is 16 bit times.

70.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. If the MDIO is implemented, it shall map MDIO control variables to PMD control variables as shown in Table 70–2, and MDIO status variables to PMD status variables as shown in Table 70–3.

Table 70–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
PMD Transmit Disable	1000BASE-KX/2.5GBASE-KX control register	1.160.0	PMD_transmit_disable

Table 70–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
Transmit fault ability	1000BASE-KX/2.5GBASE-KX status register	1.161.13	PMD_Transmit_fault_ability
Receive fault ability	1000BASE-KX/2.5GBASE-KX status register	1.161.12	PMD_Receive_fault_ability
Transmit fault	1000BASE-KX/2.5GBASE-KX status register	1.161.11	PMD_transmit_fault
Receive fault	1000BASE-KX/2.5GBASE-KX status register	1.161.10	PMD_receive_fault
PMD transmit disable ability	1000BASE-KX/2.5GBASE-KX status register	1.161.8	PMD_transmit_disable_ability
Signal detect from PMD	1000BASE-KX/2.5GBASE-KX status register	1.161.0	PMD_signal_detect

70.6 PMD functional specifications

The 1000BASE-KX PMD performs the following three functions in support of the matching service interface primitives of 38.1.1: Transmit, Receive, and Signal Detect (see service interface definition in 70.2).

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70.6.1 Link block diagram

For purposes of system conformance, the PMD sublayer is standardized at test points TP1 and TP4 as shown in Figure 70–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

The electrical path from the transmitter block to TP1, and from TP4 to the receiver block, will affect link performance and the measured values of electrical parameters used to verify conformance to this specification. It is therefore recommended that this path be carefully designed.

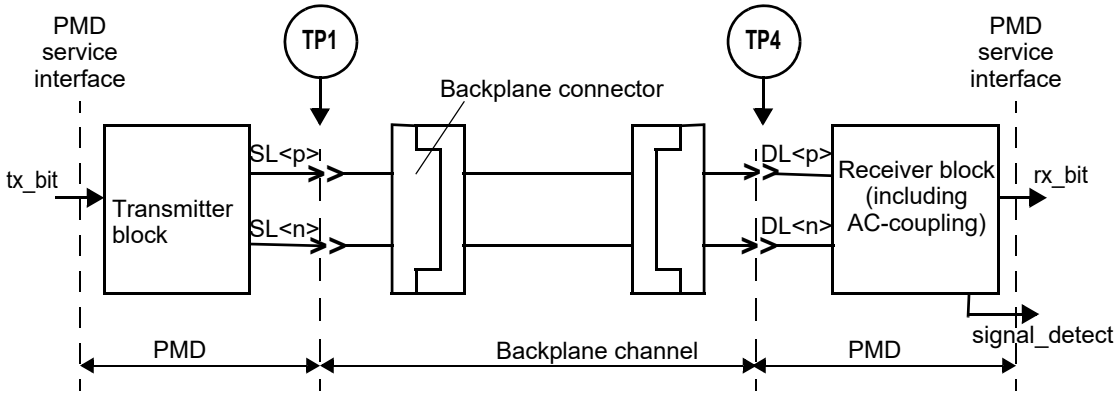

Figure 70–1—Link block diagram

70.6.2 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according electrical specifications in 70.7.1. A positive output voltage of SL<p> minus SL<n> (differential voltage) shall correspond to tx_bit = ONE.

70.6.3 PMD receive function

The PMD Receive function shall convey the bits received at the MDI in accordance with the electrical specifications of 70.7.2 to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). A positive input voltage of DL<p> minus DL<n> (differential voltage) shall correspond to rx_bit = ONE.

70.6.4 PMD signal detect function

For 1000BASE-KX operation PMD signal detect is mandatory if EEE is supported. When EEE is not supported, the PMD signal detect is optional for 1000BASE-KX and its definition is beyond the scope of this specification. When PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

If EEE is supported, a local PMD signal detect function shall report to the PMD service interface using the message PMD_SIGNAL.indication(SIGNAL_DETECT). This message is signaled continuously. For EEE, the SIGNAL_DETECT parameter can take on one of two values, OK or FAIL, indicating whether the PMD is detecting electrical energy at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication is undefined. The signal energy from a compliant transmitter shall set

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SIGNAL_DETECT to OK within 750 ns when transitioning from LPI quiet to active and set SIGNAL_DETECT to FAIL within 750 ns when transitioning from active to LPI quiet.

70.6.5 PMD transmit disable function

The PMD_transmit_disable function is mandatory if EEE is supported and is otherwise optional. When implemented, it allows the transmitter to be disabled with a single variable.

a) When the PMD_transmit_disable variable is set to ONE, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 70–4.
b) If a PMD_fault (70.6.7) is detected, then the PMD may turn off the electrical transmitter.
c) Loopback, as defined in 70.6.6, shall not be affected by PMD_transmit_disable.
d) For EEE capability, the PMD_transmit_disable function shall turn off the transmitter after tx_quiet is asserted within the time and voltage level specified in 70.7.1.5. The PMD_transmit_disable function shall turn on the transmitter after tx_quiet is de-asserted within a time and voltage level specified in 70.7.1.5.

70.6.6 Loopback mode

Loopback mode shall be provided for the 1000BASE-KX PMA/PMD by the transmitter and receiver of a device as a test function to the device. When loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. Transmitter operation shall be independent of loopback mode. A device has to be explicitly placed in loopback mode because loopback mode is not the normal mode of operation of a device. The method of implementing loopback mode is not defined by this standard.

Control of the loopback function is specified in 45.2.1.1.5.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

70.6.7 PMD fault function

If the MDIO is implemented, and the PMD has detected a local fault, the PMD shall set PMD_fault to ONE; otherwise, the PMD shall set PMD_fault to ZERO.

70.6.8 PMD transmit fault function

If the MDIO is implemented, and the PMD has detected a local fault on the transmitter, the PMD shall set the PMD_transmit_fault variable to ONE; otherwise, the PMD shall set PMD_transmit_fault to ZERO.

70.6.9 PMD receive fault function

If the MDIO is implemented, and the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to ONE; otherwise, the PMD shall set PMD_receive_fault to ZERO.

70.6.10 PMD LPI function

The PMD LPI function responds to the transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD_TXQUIET and PMD_RXQUIET requests. Implementation of the function is optional. EEE

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capabilities and parameters are advertised during the Backplane Auto-negotiation as described in 45.2.7.14. The transmitter on the local device informs the link partner's receiver when to sleep, refresh, and wake. The local receiver's transitions are controlled by the link partner's transmitter and change independently from the local transmitter's states and transitions.

The transmitter sends /LI/ ordered sets during the sleep and refresh states, disables the transmitter during quiet, and forwards /I/ during the wake phase.

If EEE is supported, the PMD transmit function enters into a low power mode when tx_quiet is set to TRUE and exits when tx_quiet is set to FALSE. While tx_quiet is TRUE the PMD transmitter functional blocks should be deactivated to conserve energy. The PMD receive function enters into a low power mode when rx_quiet is set to TRUE and exits when rx_quiet is set to FALSE. While rx_quiet is TRUE the PMD receiver functional blocks should be deactivated to conserve energy.

70.7 1000BASE-KX electrical characteristics

70.7.1 Transmitter characteristics

Transmitter characteristics at TP1 are summarized in Table 70–4 and detailed in 70.7.1.1 through 70.7.1.9.

Table 70–4—Transmitter characteristics for 1000BASE-KX

Parameter	Subclause reference	Value	Units
Signaling speed	70.7.1.3	1.25 ± 100 ppm	GBd
Differential peak-to-peak output voltage	70.7.1.5	800 to 1600	mV
Differential peak-to-peak output voltage (max.) with TX disabled	70.6.5	30	mV
DC common-mode voltage limits	70.7.1.5	–0.4 to 1.9	V
Common-mode voltage deviation (max) during LPI	70.7.1.5	150	mV
Differential output return loss (min.)	70.7.1.6	[See Equation (70–1) and Equation (70–2)]	dB
Transition time[a] (20%–80%)	70.7.1.7	60 to 320	ps
Output jitter (max. peak-to-peak) Deterministic jitter[b] Random jitter Total jitter[c]	70.7.1.8	 0.10 0.15 0.25	 UI UI UI

[a]Transition time parameters are recommended values, not compliance values.
[b]Deterministic jitter is already incorporated into the differential output template.
[c]At BER 10^{-12}.

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70.7.1.1 Test fixtures

The test fixture of Figure 70–2, or its functional equivalent, is required for measuring the transmitter specifications described in 70.7.1, with the exception of return loss.

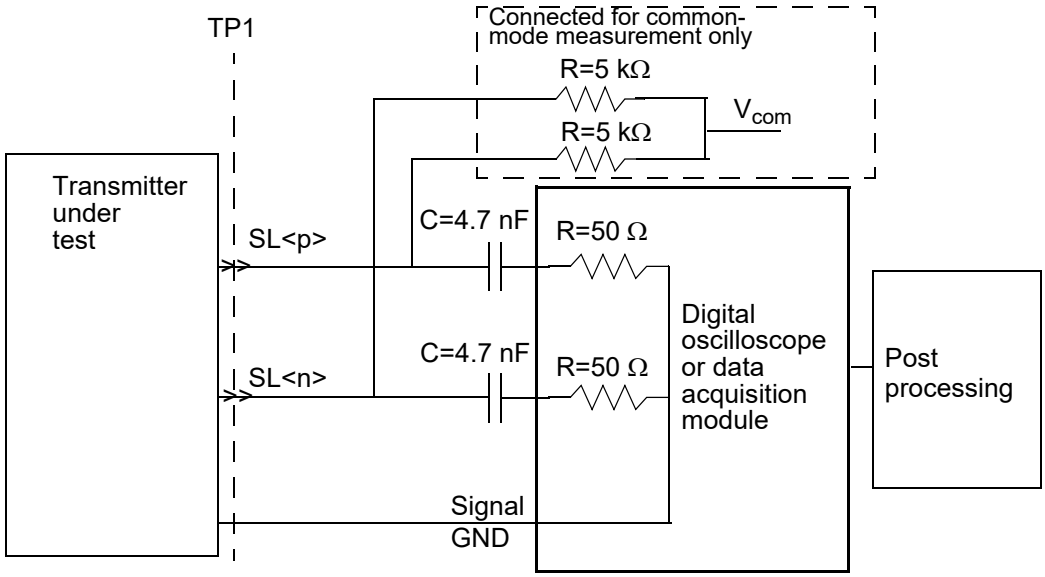

Figure 70–2—Transmit test fixture for 1000BASE-KX

70.7.1.2 Test fixture impedance

The differential load impedance applied to the transmitter output by the test fixture depicted in Figure 70–2 shall be 100 Ω with a return loss greater than 20 dB from 50 MHz to 625 MHz.

70.7.1.3 Signaling speed

The 1000BASE-KX signaling speed shall be 1.25 GBd ± 100 ppm.

70.7.1.4 Differential output eye mask

The transmitter differential output signal is defined at TP1, as shown in Figure 70–2. The transmitter output waveform shall fall within the eye mask shown in Figure 70–3 for the jitter test frame defined in 59.7.1. Voltage and time coordinates for mask points on Figure 70–3 are given in Table 70–5.

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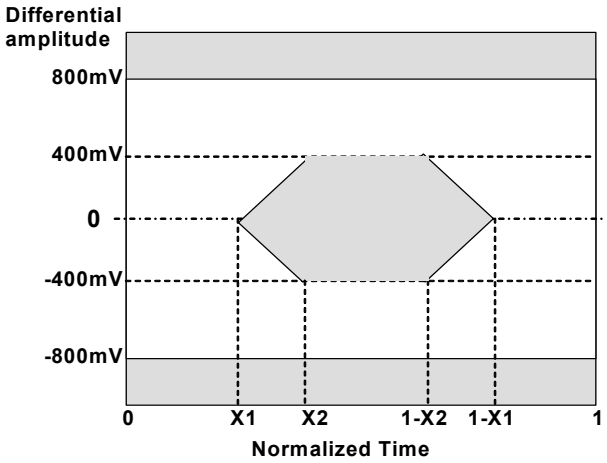

Figure 70–3—Absolute eye diagram mask at TP1 for 1000BASE-KX

Table 70–5—Transmitted eye mask at TP1 for 1000BASE-KX

Symbol	Value	Units
X1	0.125	Unit intervals (UI)
X2	0.325	Unit intervals (UI)

70.7.1.5 Output amplitude

While transmitting the test pattern specified in 36A.2, the transmitter differential peak-to-peak output voltage shall be between 800 mV and 1600 mV. See Figure 70–4 for an illustration of the definition of differential peak-to-peak output voltage. DC-referenced voltage levels are not defined since the receiver is AC-coupled. The common-mode voltage of SL<p> and SL<n> shall be between –0.4 V and 1.9 V with respect to signal ground as measured at V_{com} in Figure 70–2.

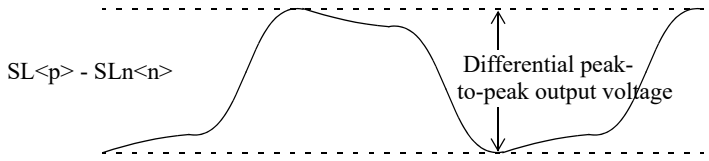

Figure 70–4—Transmitter differential peak-to-peak output voltage definition

NOTE—SL<p> and SL<n> are the positive and negative sides of the differential signal pair respectively.

For EEE capability, the transmitter's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of tx_quiet being asserted. Furthermore, the transmitters differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of tx_quiet being de-asserted. The transmitter output shall be fully compliant within 5 μs after tx_quiet is set to FALSE. During LPI, the common-mode shall be maintained to within ±150 mV of the pre-LPI value.

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70.7.1.6 Differential output return loss

For frequencies from 50 MHz to 1250 MHz, the differential return loss, in dB with f in MHz, of the transmitter shall meet the requirements of Equation (70–1) and Equation (70–2). This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$\text{ReturnLoss}(f) \geq 10 \tag{70–1}$$

for 50 MHz ≤ f < 625 MHz and

$$\text{ReturnLoss}(f) \geq 10 - 10 \times \log\left(\frac{f}{625}\right) \tag{70–2}$$

for 625 MHz ≤ f ≤ 1250 MHz.

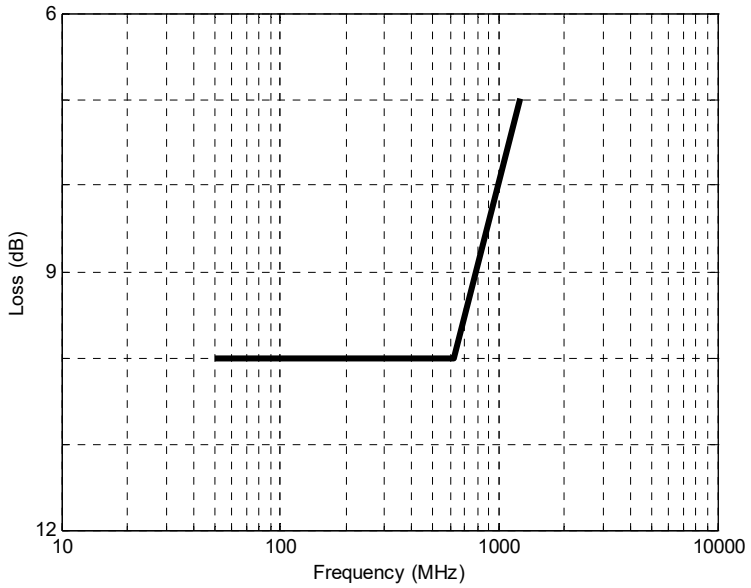

Figure 70–5—Differential return loss

70.7.1.7 Transition time

The rising edge transition time is recommended to be no less than 60 ps as measured at the 20% and 80% levels of the peak-to-peak differential value of the waveform using the high-frequency test pattern of 36A.1.

The falling edge transition time is recommended to be no less than 60 ps as measured at the 80% and 20% levels of the peak-to-peak differential value of the waveform using the high-frequency test pattern of 36A.1.

The maximum transition time is recommended to be no more than 320 ps.

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70.7.1.8 Transmit jitter

The transmitter shall have a maximum total jitter of 0.25 UI peak-to-peak and a maximum deterministic component of 0.10 UI peak-to-peak. Jitter specifications include all but 10^{-12} of the jitter population. Transmit jitter test requirements are specified in 70.7.1.9.

70.7.1.9 Transmit jitter test requirements

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in Annex 48B. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 750 kHz is applied to the jitter. The data pattern for jitter measurements shall be the jitter test frame described in 59.7.1. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal.

70.7.2 Receiver characteristics

Receiver characteristics at TP4 are summarized in Table 70–6 and detailed in 70.7.2.1 through 70.7.2.5.

Table 70–6—Receiver characteristics for 1000BASE-KX

Parameter	Subclause reference	Value	Units
Bit error ratio	70.7.2.1	10^{-12}	
Signaling speed	70.7.2.2	1.25 ± 100 ppm	GBd
Receiver coupling	70.7.2.3	AC	
Differential input peak-to-peak amplitude (max.)	70.7.2.4	1600	mV
Differential input return loss (min.)	70.7.2.5	[See Equation (70–1) and Equation (70–2)]	dB

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70.7.2.1 Receiver interference tolerance

The receiver interference tolerance shall be measured as described in Annex 69A with the parameters specified in Table 70–7. The data pattern for the interference tolerance test shall be the jitter pattern test frame as defined in 59.7.1. The receiver shall satisfy the requirements for interference tolerance specified in Annex 69A.

Table 70–7—1000BASE-KX interference tolerance parameters

Parameter	Value	Units
Target BER	10^{-12}	
m_{TC}[a] (min.)	1.0	
Amplitude of broadband noise (min. RMS)	8.6	mV
Applied transition time (20%–80%, min.)	320	ps
Applied sinusoidal jitter (min. peak-to-peak)	0.10	UI
Applied random jitter (min. peak-to-peak)[b]	0.15	UI
Applied duty cycle distortion (min. peak-to-peak)	0.0	UI

[a]m_{TC} is defined in Equation (69A–6) of Annex 69A.
[b]Applied random jitter is specified at a BER of 10^{-12}.

70.7.2.2 Signaling speed range

A 1000BASE-KX receiver shall comply with the requirements of Table 70–7 for any signaling speed in the range 1.25 GBd ± 100 ppm. The corresponding unit interval is nominally 800 ps.

70.7.2.3 AC-coupling

The receiver shall be AC-coupled to the backplane to allow for maximum interoperability between various PMD components. AC-coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC-coupling in actual implementations.

NOTE—It is recommended that the maximum value of the coupling capacitors be limited to 4.7 nF. This will limit the inrush currents to the receiver that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

70.7.2.4 Input signal amplitude

Receivers shall accept differential input signal peak-to-peak amplitudes produced by compliant transmitters connected without attenuation to the receiver, and still meet the BER requirement specified in 70.7.2.1. Note that this may be larger than the 1600 mV differential maximum of 70.7.1.5 due to the actual transmitter output and receiver input impedances. The input impedance of a receiver can cause the minimum signal into a receiver to differ from that measured when the receiver is replaced with a 100 Ω test load. Since the receiver is AC-coupled, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

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70.7.2.5 Differential input return loss

For frequencies from 50 MHz to 1250 MHz, the differential return loss, in dB with f in MHz, of the receiver shall meet the requirements of Equation (70–1) and Equation (70–2). The reference impedance for differential return loss measurements shall be 100 Ω.

70.8 Interconnect characteristics

Informative interconnect characteristics for 1000BASE-KX are provided in Annex 69B.

70.9 Environmental specifications

70.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

70.9.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

70.9.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

70.9.4 Electromagnetic compatibility

A system integrating the 1000BASE-KX PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

70.9.5 Temperature and humidity

A system integrating the 1000BASE-KX PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

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70.10 Protocol implementation conformance statement (PICS) proforma for Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-KX[132]

70.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3, Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium type 1000BASE-KX, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

70.10.2 Identification

70.10.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

70.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium type 1000BASE-KX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[132]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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70.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
GMII	GMII	70.1, 35	Interface is supported	O	Yes [ ] No [ ]
PCS	Support of 1000BASE-X PCS/PMA	70.1, 36		M	Yes [ ] No [ ]
AN	Auto-Negotiation for Backplane Ethernet	70.1, 73	Device implements Auto-Negotiation for Backplane Ethernet	M	Yes [ ]
FD	Full duplex operation	70.1	Clause 36 PCS/PMA when used with 1000GBASE-KX supports full-duplex operation only	M	Yes [ ]
DC	Delay Constraints	70.4	Device conforms to delay constraints	M	Yes [ ]
LPI	LPI	70.6.10	Capable of LPI	O	Yes [ ] No [ ]
*MD	MDIO interface	70.5	Device implements MDIO	O	Yes [ ] No [ ]
*SD	Signal Detect Generation	70.6.4	Signal detect implemented	O	Yes [ ] No [ ]
*TD	PMD_transmit_disable	70.6.5		O	Yes [ ] No [ ]

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70.10.4 PICS proforma tables for Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-KX

70.10.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Transmit function	70.6.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FS2	Transmitter signal	70.6.2	A positive differential voltage corresponds to tx_bit = ONE	M	Yes [ ]
FS3	Receive function	70.6.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FS4	Receiver signal	70.6.3	A positive differential voltage corresponds to rx_bit = ONE	M	Yes [ ]
FS5	PMD Signal Detect function	70.6.4	Continuously reported OK via PMD_SIGNAL.indication (SIGNAL_DETECT).	!SD:M	Yes [ ] No [ ]
FS6	PMD Signal Detect during LPI	70.6.4	Indicate signal energy during LPI	LPI:M	Yes [ ] N/A [ ]
FS7	Transmit Disable during LPI	70.6.5	Disable transmitter during tx_-quiet	LPI:M	Yes [ ] N/A [ ]
FS8	Signal Detect for EEE	70.6.4	Transition timing to set SIGNAL_DETECT	LPI:M	Yes[ ] N/A [ ]
FS9	Transmit Disable	70.6.5	Disables Transmitter when PMD_Transmit_disable set to ONE	TD:M	Yes [ ] N/A [ ]
FS10	PMD_fault	70.6.5	Transmit disabled if detected	TD:O	Yes [ ] No [ ] N/A [ ]
FS11	PMD_transmit_disable	70.6.5	Loopback function not affected	TD:M	Yes [ ] N/A [ ]
FS12	tx_quiet disabled transmitter	70.7.1	Disables Transmitter when tx_quiet is asserted as specified in 70.7.1.5	LPI:M	Yes [ ] N/A [ ]
FS13	Loopback Function	70.6.6	Loopback function provided	M	Yes [ ]
FS14	Loopback affect on Transmitter	70.6.6	Loopback function does not disable transmitter	M	Yes [ ]

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70.10.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	MDIO Variable Mapping	70.5	Per Table 70–2 and Table 70–3	MD:M	Yes [ ] N/A [ ]
MF2	PMD_fault function	70.6.7	Sets PMD_fault to a logical 1 if any local fault is detected; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]
MF3	PMD_transmit_fault function	70.6.8	Sets PMD_transmit_fault to a logical 1 if any local fault is detected on the transmit path; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]
MF4	PMD_receive_fault function	70.6.9	Sets PMD_receive_fault to a logical 1 if any local fault is detected on the receive path; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]

70.10.4.3 Transmitter electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	100 Ω differential test fixture	70.7.1.2	With return loss > 20 dB from 50 MHz to 625 MHz	M	Yes [ ]
TC2	Signaling speed	70.7.1.3	1.25 GBd ± 100ppm	M	Yes [ ]
TC3	Output waveform within template per Figure 70–3	70.7.1.4		M	Yes [ ]
TC4	Differential peak-to-peak output voltage	70.7.1.5	Between 800 mV and 1600 mV while transmitting test pattern specified in 36A.2	M	Yes [ ]
TC5	Common-mode output voltage	70.7.1.5	Between –0.4 V and 1.9 V	M	Yes [ ]
TC6	Output Return Loss	70.7.1.6	Per Equation (70–1) and Equation (70–2)	M	Yes [ ]
TC7	Reference Impedance	70.7.1.6	100 Ω for differential return loss measurements	M	Yes [ ]
TC8	Transmit jitter, peak-to-peak	70.7.1.8	Max TJ of 0.25 UI. Max DJ of 0.10 UI	M	Yes [ ]
TC9	Output Amplitude LPI voltage	70.7.1.5	Less than 30 mV within 500 ns of tx_quiet	LPI:M	Yes [ ] N/A [ ]
TC10	Output Amplitude ON voltage	70.7.1.5	Greater than 720 mV within 500 ns of tx_quiet de-asserted	LPI:M	Yes [ ] N/A [ ]
TC11	Jitter test patterns	70.7.1.9	Jitter test frame per 59.7.1	M	Yes [ ]

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70.10.4.4 Receiver electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Receiver interference tolerance measurement method	70.7.2.1	Per Annex 69A with parameters specified in Table 70–7	M	Yes [ ]
RC2	Receiver interference tolerance test pattern	70.7.2.1	Per 70.7.2.1	M	Yes [ ]
RC3	Receiver interference tolerance requirements	70.7.2.1	Satisfy requirements per Annex 69A	M	Yes [ ]
RC4	Input signaling speed in the range of 1.25 GBd ± 100ppm	70.7.2.2	Receiver meets requirements of Table 70–7	M	Yes [ ]
RC5	Receiver AC-coupled	70.7.2.3		M	Yes [ ]
RC6	Input signal amplitude	70.7.2.4	BER still met when compliant transmitter is connected with no attenuation	M	Yes [ ]
RC7	Differential input return loss	70.7.2.5	Per Equation (70–1) and Equation (70–2)	M	Yes [ ]
RC8	Reference Impedance	70.7.2.5	100 Ω for differential return loss measurements	M	Yes [ ]

70.10.4.5 Environmental and safety specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	70.9.1	Conforms to J.2	M	Yes [ ]
ES2	Electromagnetic compatibility	70.9.4	Comply with applicable local and national codes	M	Yes [ ]

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71. Physical Medium Dependent sublayer and baseband medium, type 10GBASE-KX4

71.1 Overview

This clause specifies the 10GBASE-KX4 PMD and the baseband medium. When forming a complete PHY, a PMD shall be connected to the appropriate sublayers (see Table 71–1), and with the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

The XAUI, defined by Clause 47, is intended for chip-to-chip applications for lengths up to approximately 0.5 m. 10GBASE-KX4 is intended for backplane applications up to 1 m in length.

Table 71–1—Physical Layer clauses associated with the 10GBASE-KX4 PMD

Associated clause	10GBASE-KX4
46—XGMII[a]	Optional
47—XGXS and XAUI	Optional
48—10GBASE-X PCS/PMA	Required
73—Auto-Negotiation for Backplane Ethernet	Required
78—EEE	Optional

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation behaves functionally as though the RS and XGMII were present.

A 10GBASE-KX4 PHY with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization. The “Assert LPI” request at the XGMII is encoded in the transmitted symbols. Detection of LPI signaling in the received symbols is indicated as “Assert LPI” at the XGMII. Upon the detection of “Assert LPI” at the XGMII, an energy-efficient 10GBASE-KX4 PHY continues transmitting for a predefined period, then ceases transmission and deactivates transmit functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g., timing recovery, adaptive filter coefficients) and thereby track long-term variations in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal interframes resume at the XGMII, the PHY reactivates transmit functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the LPI mode.

71.2 Physical Medium Dependent (PMD) service interface

The 10GBASE-KX4 PMD utilizes the PMD service interface defined in 53.1.1.

The following primitives are defined on the PMD Service Interface when EEE is supported:

PMD_RXQUIET.request(rx_quiet)
PMD_TXQUIET.request(tx_quiet)

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These messages are defined for the PCS in 48.2.6.1.7.

71.2.1 PMD_RXQUIET.request

This primitive is generated by the PCS Receive Process when EEE is supported to indicate that the input signal is quiet and the PMA and PMD receiver may go into a low power mode. When EEE is not supported, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

71.2.1.1 Semantics of the service primitive

PMD_RXQUIET.request (rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE.

71.2.1.2 When generated

The PCS generates this primitive to request the appropriate PMD receive LPI state.

71.2.1.3 Effect of receipt

This variable is from the Receive process of the PCS to control the power-saving function of the local receiver. The 10GBASE-KX4 PHY receiver should put unused functional blocks into a low power state to save energy.

71.2.2 PMD_TXQUIET.request

This primitive is generated by the PCS Transmit Process when EEE is supported to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. When EEE is not supported, the primitive is never invoked and the PMD behaves as if tx_quiet = FALSE.

71.2.2.1 Semantics of the service primitive

PMD_TXQUIET.request (tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE.

71.2.2.2 When generated

The PCS generates this primitive to request the appropriate PMD transmit LPI state.

71.2.2.3 Effect of receipt

This primitive affects operation of the PMD Transmit disable function as described in 71.6.6. The 10GBASE-KX4 PHY transmitter should put unused functional blocks into a lower power state to save energy.

71.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD shall support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 48.2.7.)

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71.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers consider the delay maxima, and that network planners and administrators consider the delay constraints regarding the physical topology and concatenation of devices. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 69.3.

The sum of transmit and receive delays contributed by the 10GBASE-KX4 PMD and medium shall be no more than 512 bit times or 1 pause_quanta. It is assumed that the round-trip delay through the medium is 160 bit times.

71.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. If the MDIO is implemented, it shall map MDIO control variables to PMD control variables as shown in Table 71–2 and MDIO status variables to PMD status variables as shown in Table 71–3.

Table 71–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
Global PMD transmit disable	Transmit disable register	1.9.0	Global_PMD_transmit_disable
Transmit disable 3	Transmit disable register	1.9.4	PMD_transmit_disable_3
Transmit disable 2	Transmit disable register	1.9.3	PMD_transmit_disable_2
Transmit disable 1	Transmit disable register	1.9.2	PMD_transmit_disable_1
Transmit disable 0	Transmit disable register	1.9.1	PMD_transmit_disable_0

71.6 PMD functional specifications

The 10GBASE-KX4 PMD performs the transmit and receive functions that convey data between the PMD service interface and the MDI, and provides various management functions if the optional MDIO is implemented.

71.6.1 Link block diagram

For purposes of system conformance, the PMD sublayer is standardized at test points TP1 and TP4 as shown in Figure 71–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

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Table 71–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD Receive signal detect	Receive signal detect register	1.10.0	Global_PMD_signal_detect
PMD signal detect 3	Receive signal detect register	1.10.4	PMD_signal_detect_3
PMD signal detect 2	Receive signal detect register	1.10.3	PMD_signal_detect_2
PMD signal detect 1	Receive signal detect register	1.10.2	PMD_signal_detect_1
PMD signal detect 0	Receive signal detect register	1.10.1	PMD_signal_detect_0

The electrical path from the transmitter block to TP1, and from TP4 to the receiver block, will affect link performance and the measured values of electrical parameters used to verify conformance to this specification. It is therefore recommended that this path be carefully designed.

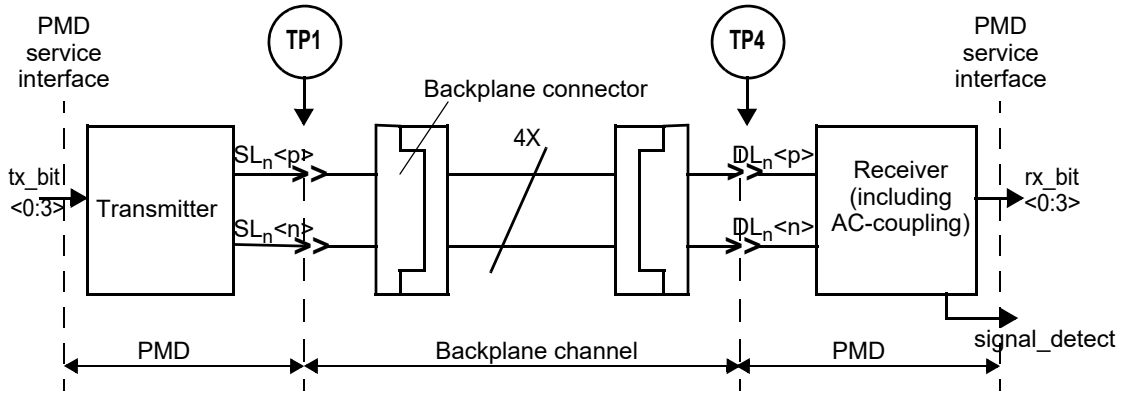

Figure 71–1—Link block diagram

71.6.2 PMD Transmit function

The PMD Transmit function shall convert the four logical bit streams requested by the PMD service interface message PMD_UNITDATA.request (tx_bit<0:3>) into four separate electrical signals. The four electrical signals shall then be delivered to the MDI, all according to the specifications in 71.7.1. A positive output voltage of SLn<p> minus SLn<n> (differential voltage) shall correspond to tx_bit = ONE.

The PMD shall convey the bits received from the PMD service interface using the message PMD_UNITDATA.request(tx_bit<0:3>) to the MDI lanes, where SL0<p>/<n> corresponds to tx_bit<0>, SL1<p>/<n> to tx_bit<1>, SL2<p>/<n> to tx_bit<2>, and SL3<p>/<n>) = tx_bit<3>.

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71.6.3 PMD Receive function

The PMD Receive function shall convert the four electrical signals from the MDI into four logical bit streams for delivery to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit<0:3>), all according to the receive electrical specifications in 71.7.2. A positive input voltage level in each signal of DLn<p> minus DLn<n> (differential voltage) shall correspond to a rx_bit = ONE.

The PMD shall convey the bits received from the MDI lanes to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit<0:3>), where rx_bit<0:3> = (DL0<p>/<n>, DL1<p>/<n>, DL2<p>/<n>, DL3<p>/<n>).

71.6.4 Global PMD signal detect function

For 10GBASE-KX4 operation Global PMD signal detect is mandatory if EEE is supported. When EEE is not implemented, the PMD signal detect is optional for 10GBASE-KX4 and its definition is beyond the scope of this standard. When Global PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

If EEE is supported, a local PMD signal detect function shall report to the PMD service interface using the message PMD_SIGNAL.indication(SIGNAL_DETECT). This message is signaled continuously. For EEE, the SIGNAL_DETECT parameter can take on one of two values, OK or FAIL, indicating whether the PMD is detecting electrical energy at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication(rx_lane<3:0>) is undefined. The signal energy from a compliant transmitter shall set SIGNAL_DETECT to OK within 750 ns when transitioning from LPI quiet to active and set SIGNAL_DETECT to FAIL within 750 ns when transitioning from active to LPI quiet.

71.6.5 PMD lane-by-lane signal detect function

When the MDIO is implemented, each PMD_signal_detect_n value, where n represents the lane number in the range 0:3, shall report the value of SIGNAL_DETECT for the corresponding lane when signal detect is implemented, or OK otherwise.

71.6.6 Global PMD transmit disable function

The Global_PMD_transmit_disable function is mandatory if EEE is supported and is otherwise optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When the Global_PMD_transmit_disable variable is set to ONE, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 71–4.
b) If a PMD_fault (71.6.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 71.6.8, shall not be affected by Global_PMD_transmit_disable.
d) For EEE capability, the PMD_transmit_disable function shall turn off all transmitter lanes after tx_quiet is asserted within a time and voltage level specified in 71.7.1.4. The PMD_transmit_disable function shall turn on all transmitter lanes after tx_quiet is de-asserted within a time and voltage level specified in 71.7.1.4.

71.6.7 PMD lane-by-lane transmit disable function

The PMD_transmit_disable_n function shall be implemented. It allows the electrical transmitters in each lane to be selectively disabled.

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a) When a PMD_transmit_disable_n variable is set to ONE, this function shall turn off the transmitter associated with that variable such that the corresponding transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 71–4.
b) If a PMD_fault (71.6.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 71.6.8, shall not be affected by PMD_transmit_disable_n.

NOTE—Turning off a transmitter can be disruptive to a network.

71.6.8 Loopback mode

Loopback mode shall be provided for the 1000BASE-KX4 PMA/PMD by the transmitter and receiver of a device as a test function to the device. When loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. Transmitter operation shall be independent of loopback mode. A device has to be explicitly placed in loopback mode because loopback mode is not the normal mode of operation of a device. The method of implementing loopback mode is not defined by this standard.

Control of the loopback function is specified in 45.2.1.1.5.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

71.6.9 PMD fault function

If the MDIO is implemented, and the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to ONE; otherwise, the PMD shall set PMD_fault to ZERO.

71.6.10 PMD transmit fault function

If the MDIO is implemented, and the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to ONE; otherwise, the PMD shall set PMD_transmit_fault to ZERO.

71.6.11 PMD receive fault function

If the MDIO is implemented, and the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to ONE; otherwise, the PMD shall set PMD_receive_fault to ZERO.

71.6.12 PMD LPI function

The PMD LPI function responds to transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD_TXQUIET and PMD_RXQUIET requests. Implementation of the function is optional. EEE capabilities and parameters, as described in 45.2.7, is advertised during the Backplane Auto-negotiation. The transmitter on the local device will inform the link partner’s receiver when to sleep, refresh, and wake. The local receiver transitions are controlled by the link partner’s transmitter and can change independent of the local transmitter states and transitions.

The transmitter sends /LI/ ordered sets during the sleep and refresh states, disables the transmitter during quiet, and forwards ||I|| during the wake phase.

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If EEE is supported, the PMD transmit function enters into a low power mode when tx_quiet is set to TRUE and exits when tx_quiet is set to FALSE. While tx_quiet is TRUE the PMD transmitter functional blocks should be deactivated to conserve energy. The PMD receive function enters into a low power mode when rx_quiet is set to TRUE and exits when rx_quiet is set to FALSE. While rx_quiet is TRUE, the PMD receiver functional blocks should be deactivated to conserve energy.

71.7 Electrical characteristics for 10GBASE-KX4

71.7.1 Transmitter characteristics

Transmitter characteristics at TP1 are summarized in Table 71–4.

Table 71–4—Transmitter characteristics for 10GBASE-KX4

Parameter	Subclause reference	Value	Units
Signaling speed, per lane	71.7.1.3	3.125 ± 100 ppm	GBd
Differential peak-to-peak output voltage	71.7.1.4	800 to 1200	mV
Differential peak-to-peak output voltage (max.) with TX disabled	71.6.6, 71.6.7	30	mV
Common-mode voltage limits	71.7.1.4	–0.4 to 1.9	V
Common-mode voltage deviation (max) during LPI	71.7.1.4	150	mV
Differential output return loss (min.)	71.7.1.5	[See Equation (71–1) and Equation (71–2)]	dB
Differential output template	71.7.1.6	[See Figure 71–5 and Table 71–5]	V
Transition time[a] (20%–80%)	71.7.1.7	60 to 130	ps
Output jitter (max. peak-to-peak) Random jitter Deterministic jitter Total jitter[b]	71.7.1.8	 0.27 0.17 0.35	 UI UI UI

[a]Transition time parameters are recommended values, not compliance values.
[b]At BER 10^{-12}.

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71.7.1.1 Test fixtures

The test fixture of Figure 71–2, or its functional equivalent, is required for measuring the transmitter specifications described in 71.7.1, with the exception of return loss.

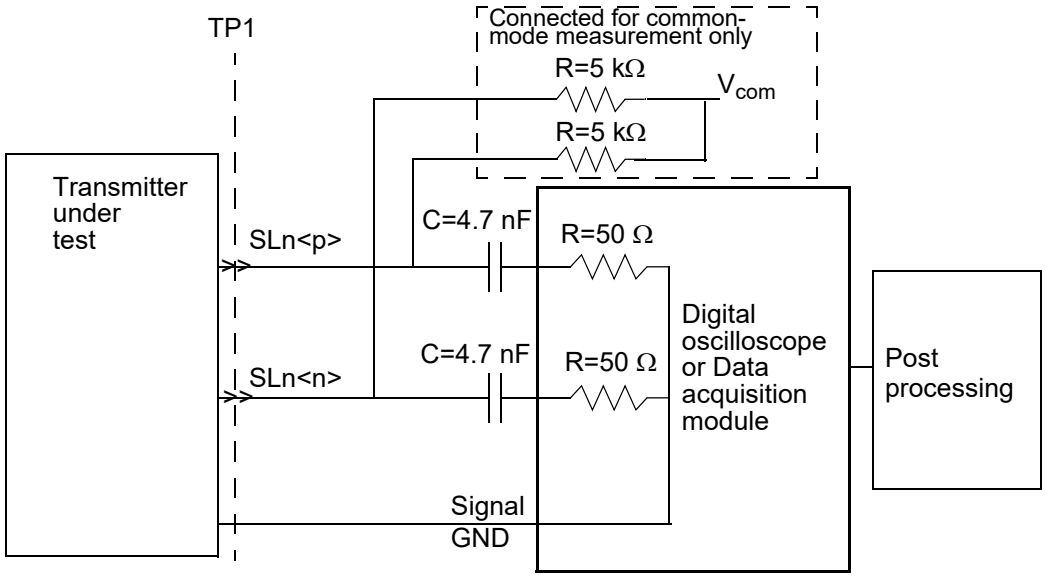

Figure 71–2—Transmit test fixture for 10GBASE-KX4

71.7.1.2 Test fixture impedance

The differential load impedance applied to the transmitter output by the test fixture depicted in Figure 71–2 shall be 100 Ω with a return loss greater than 20 dB from 100 MHz to 2000 MHz.

71.7.1.3 Signaling speed

The 10GBASE-KX4 signaling speed shall be 3.125 GBd ±100 ppm. The corresponding unit interval is nominally 320 ps.

71.7.1.4 Output amplitude

While transmitting the test pattern specified in 48A.2,

1) The transmitter maximum differential peak-to-peak output voltage shall be less than 1200 mV.
2) The minimum differential peak-to-peak output voltage shall be greater than 800 mV.
3) The maximum difference between any two lanes' differential peak-to-peak output voltage shall be less than or equal to 150 mV.

See Figure 71–3 for an illustration of the definition of differential peak-to-peak output voltage.

DC-referenced voltage levels are not defined since the receiver is AC-coupled. The common-mode voltage of SLn<p> and SLn<n> shall be between –0.4 V and 1.9 V with respect to signal ground as measured at V_{com} in Figure 71–2.

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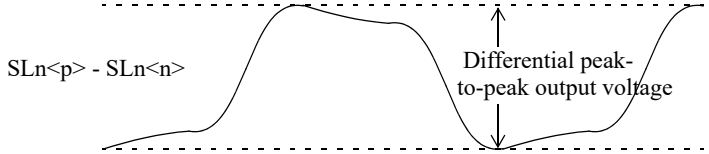

Figure 71–3—Transmitter differential peak-to-peak output voltage definition

NOTE—SLn<p> and SLn<n> are the positive and negative sides of the differential signal pair for Lane n (n = 0,1,2,3).

For EEE capability, the transmitter lane's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of tx_quiet being asserted. Furthermore, the transmitter lane's differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of tx_quiet being de-asserted. The transmitter output shall be fully compliant within 5 μs after tx_quiet is set to FALSE. During LPI, the common-mode shall be maintained to within ± 150 mV of the pre-LPI value.

71.7.1.5 Output return loss

For frequencies from 100 MHz to 2000 MHz, the differential return loss, in dB with f in MHz, of the transmitter shall meet the requirements of Equation (71–1) and Equation (71–2). This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$\text{ReturnLoss}(f) \geq 10 \tag{71–1}$$

for 100 MHz ≤ f < 625 MHz and

$$\text{ReturnLoss}(f) \geq 10 - 10 \times \log_{10}\left(\frac{f}{625}\right) \tag{71–2}$$

for 625 MHz ≤ f ≤ 2000 MHz

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The minimum differential output return loss is shown in Figure 71–4.

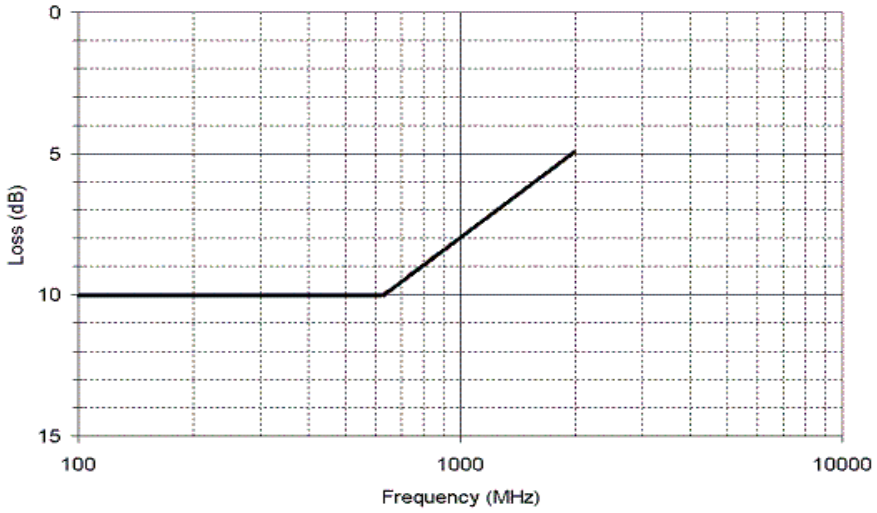

Figure 71–4—Minimum differential output return loss

71.7.1.6 Differential output template

The transmitter differential output signal is defined at TP1, as shown in Figure 71–2 and Figure 71–3. The transmitter shall provide equalization such that the output waveform falls within the template shown in Figure 71–5 for the test pattern specified in 48A.2, with all other transmitters active. All other transmitters shall be terminated with a load meeting the requirements described in 71.7.1.2. Voltage and time coordinates for inflection points on Figure 71–5 are given in Table 71–5. The waveform under test shall be normalized by using the following procedure:

a) Align the output waveform under test, to achieve the best fit along the horizontal time axis.
b) Calculate the +1 low frequency level as V_{lowp} = average of any two successive unit intervals (2UI) between 2.5 UI and 5.5 UI.
c) Calculate the 0 low frequency level as V_{lowm} = average of any two successive unit intervals (2UI) between 7.5 UI and 10.5 UI.
d) Calculate the vertical offset to be subtracted from the waveform as $V_{off} = (V_{lowp} + V_{lowm}) / 2$.
e) Calculate the vertical normalization factor for the waveform as $V_{norm} = (V_{lowp} – V_{lowm}) / 2$.
f) Calculate the normalized waveform as:
Normalized_Waveform = (Original_Waveform – V_{off}) × (0.69/V_{norm}).
g) Align the Normalized_Waveform under test, to achieve the best fit along the horizontal time axis.

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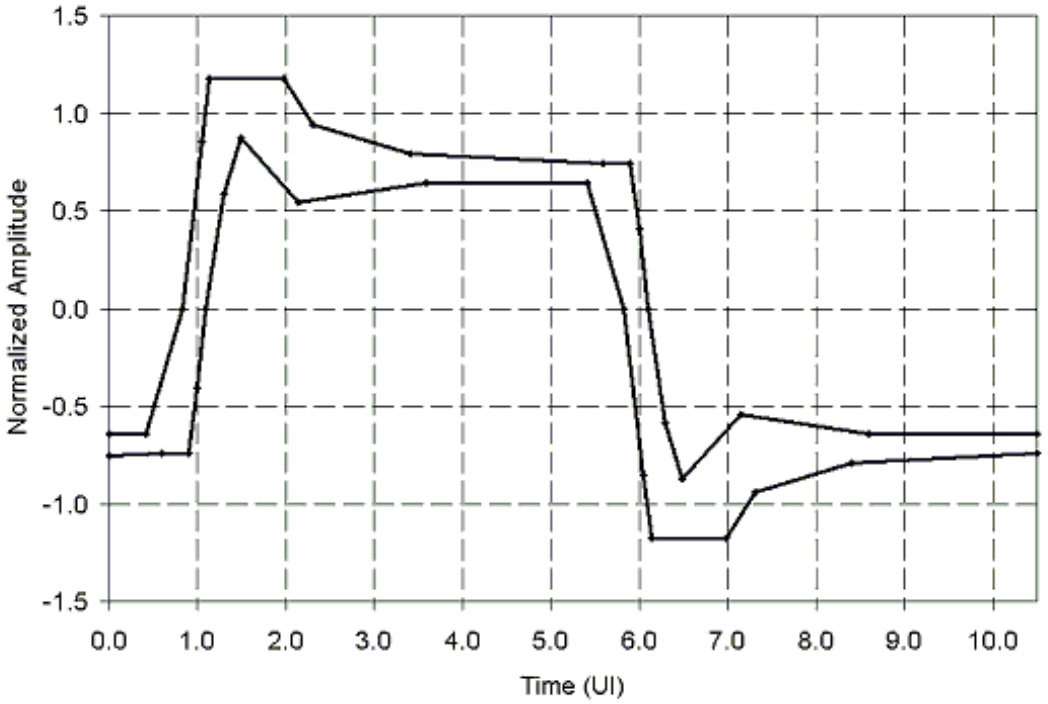

Figure 71–5—Normalized transmit template

Table 71–5—Normalized transmit time domain template

Upper limit				Lower limit			
Time (UI)	**Amplitude**	**Time (UI)**	**Amplitude**	**Time (UI)**	**Amplitude**	**Time (UI)**	**Amplitude**
0.000	–0.640	5.897	0.740	0.000	–0.754	5.409	0.640
0.409	–0.640	5.997	0.406	0.591	–0.740	5.828	0.000
0.828	0.000	6.094	0.000	0.897	–0.740	6.050	–0.856
1.050	0.856	6.294	–0.586	0.997	–0.406	6.134	–1.175
1.134	1.175	6.491	–0.870	1.094	0.000	6.975	–1.175
1.975	1.175	7.141	–0.546	1.294	0.586	7.309	–0.940
2.309	0.940	8.591	–0.640	1.491	0.870	8.500	–0.790
3.409	0.790	10.500	–0.640	2.141	0.546	10.500	–0.742
5.591	0.740			3.591	0.640		

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71.7.1.7 Transition time

The rising edge transition time is recommended to be between 60 ps and 130 ps as measured at the 20% and 80% levels of the peak-to-peak differential value of the waveform using the high-frequency test pattern of 48A.1. The falling edge transition time is recommended to be between 60 ps and 130 ps as measured at the 80% and 20% levels of the peak-to-peak differential value of the waveform using the high-frequency test pattern of 48A.1.

71.7.1.8 Transmit jitter

The transmitter shall have a maximum total jitter of 0.350 UI peak-to-peak, a maximum deterministic component of 0.170 UI peak-to-peak, and a maximum random component of 0.270 UI peak-to-peak. Jitter specifications include all but 10^{-12} of the jitter population. Transmit jitter test requirements are specified in 71.7.1.9.

71.7.1.9 Transmit jitter test requirements

Transmit jitter is defined with respect to the transmitter differential output signal at TP1, as shown in Figure 71–2 and Figure 71–5, and the test procedure resulting in a BER bathtub curve such as that described in Annex 48B. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements shall be the jitter tolerance test pattern defined in Annex 48A.5. For this test, all other transmitters shall be active and terminated with a load meeting the requirements described in 71.7.1.2. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal.

71.7.2 Receiver characteristics

Receiver characteristics at TP4 are summarized in Table 71–6 and detailed in 71.7.2.1 through 71.7.2.5.

Table 71–6—Receiver characteristics

Parameter	Subclause reference	Value	Units
Bit error ratio	71.7.2.1	10^{-12}	
Signaling speed, per lane	71.7.2.2	3.125 ± 100 ppm	GBd
Unit interval (UI) nominal	71.7.2.2	320	ps
Receiver coupling	71.7.2.3	AC	
Differential input peak-to-peak amplitude (maximum)	71.7.2.4	1600	mV
EEE Signal Detect deactivation time (T_{SD}) from active to LPI quiet	71.6.4	750	ns
EEE Signal Detect activation time (T_{SA}) from LPI quiet to active	71.6.4	750	ns
Differential input return loss[a] (minimum)	71.7.2.5	[See Equation (71–1) and Equation (71–2)]	dB

[a]Relative to 100 Ω differential.

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71.7.2.1 Receiver interference tolerance

The receiver interference tolerance shall be measured as described in Annex 69A with the parameters specified in Table 71–7. The data pattern for the interference tolerance test shall be the continuous jitter test pattern as defined in Annex 48A.5. The receiver shall satisfy the requirements for interference tolerance specified in Annex 69A.

Table 71–7—10GBASE-KX4 interference tolerance parameters

Parameter	Value	Units
Target BER	10^{-12}	
m_{TC}[a] (min.)	1.0	
Amplitude of broadband noise (min. RMS)	8.1	mV
Applied transition time (20%–80%, min.)	130	ps
Applied sinusoidal jitter (min. peak-to-peak)	0.17	UI
Applied random jitter (min. peak-to-peak)[b]	0.18	UI
Applied duty cycle distortion (min. peak-to-peak)	0.0	UI

[a]m_{TC} is defined in Equation (69A–6) of Annex 69A.
[b]Applied random jitter is specified at a BER of 10^{-12}.

71.7.2.2 Signaling speed

The 10GBASE-KX4 signaling speed shall be 3.125 GBd ± 100 ppm. The corresponding unit interval is nominally 320 ps.

71.7.2.3 AC-coupling

The 10GBASE-KX4 receiver shall be AC-coupled to the backplane to allow for maximum interoperability between various 10 Gb/s components. AC-coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC-coupling in actual implementations.

NOTE—It is recommended that the maximum value of the coupling capacitors be limited to 4.7 nF. This will limit the inrush currents to the receiver that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

71.7.2.4 Input signal amplitude

10GBASE-KX4 receivers shall accept differential input signal peak-to-peak amplitudes produced by compliant transmitters connected without attenuation to the receiver, and still meet the BER requirement specified in 71.7.2.1. Note that this may be larger than the 1200 mV differential maximum of 71.7.1.4 due to the actual transmitter output and receiver input impedances. The input impedance of a receiver can cause the minimum signal into a receiver to differ from that measured when the receiver is replaced with a 100 Ω test load. Since the channel is AC-coupled, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

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71.7.2.5 Differential input return loss

For frequencies from 100 MHz to 2000 MHz, the differential return loss, in dB with *f* in MHz, of the receiver shall be greater than or equal to Equation (71–1) and Equation (71–1). The reference impedance for differential return loss measurements is 100 Ω.

71.8 Interconnect characteristics

Informative interconnect characteristics for 10GBASE-KX4 are provided in Annex 69B.

71.9 Environmental specifications

71.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

71.9.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

71.9.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

71.9.4 Electromagnetic compatibility

A system integrating the 10GBASE-KX4 PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

71.9.5 Temperature and humidity

A system integrating the 10GBASE-KX4 PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

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71.10 Protocol implementation conformance statement (PICS) proforma for Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KX4[133]

71.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3, Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium type 10GBASE-KX4, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

71.10.2 Identification

71.10.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

71.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium type 10GBASE-KX4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[133] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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71.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XGE	XGMII	71.1, 46	Interface is supported	O	Yes [ ] No [ ]
XGXS	XGXS and XAUI	71.1, 47		O	Yes [ ] No [ ]
PCS	Support of 10GBASE-X PCS/PMA	71.1, 48		M	Yes [ ]
AN	Auto-Negotiation for Backplane Ethernet	71.1, 73	Device implements Auto-Negotiation for Backplane Ethernet	M	Yes [ ]
DC	Delay Constraints	71.4	Device conforms to delay constraints	M	Yes [ ]
LPI	LPI function	71.6.12	LPI supported	O	Yes [ ] No [ ]
*MD	MDIO interface	71.5	Device implements MDIO	O	Yes [ ] No [ ]
*SD	Signal Detect Generation	71.6.4	Signal detect implemented	O	Yes [ ] No [ ]
*TD	Global_PMD_transmit_disable	71.6.6		O	Yes [ ] No [ ]

71.10.4 PICS proforma tables for Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KX4

71.10.4.1 PCS requirements for AN service interface

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	AN service interface primitive	71.3	The PCS associated with this PMD supports the AN service interface primitive AN_LINK.indication defined in 73.9	M	Yes [ ]

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71.10.4.2 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Transmit function	71.6.2	Convert the 4 logical signals requested by PMD_UNITDA-TA.request (tx_bit<0:3>) to 4 electrical signals	M	Yes [ ]
FS2	Delivery to the MDI	71.6.2	Supplies 4 electrical signals for delivery to the MDI per 71.7.1	M	Yes [ ]
FS3	Transmitter signal	71.6.2	A positive differential voltage corresponds to tx_bit = ONE	M	Yes [ ]
FS4	Transmit Signal order	71.6.2	PMD_UNITDATA.request(tx_bit<0:3>) = (SL0<p>/<n>, SL1<p>/<n>, SL2<p>/<n>, SL3<p>/<n>)	M	Yes [ ]
FS5	Receive function	71.6.3	Convert the 4 electrical signals received from the MDI to 4 logical signals PMD_UNITDATA.indication (rx_bit<0:3>) per 71.7.2	M	Yes [ ]
FS6	Receiver signal	71.6.3	A positive differential voltage corresponds to rx_bit = ONE	M	Yes [ ]
FS7	Receive Signal order	71.6.3	PMD_UNITDATA.request(rx_bit<0:3>) = (DL0<p>/<n>, DL1<p>/<n>, DL2<p>/<n>, DL3<p>/<n>)	M	Yes [ ]
FS8	Behavior when Global_PMD_signal_detect is not implemented	71.6.4	SIGNAL_DETECT = OK continuously	!SD:M	Yes [ ] N/A [ ]
FS9	Global_PMD_signal_detect function	71.6.4	Reported via PMD_SIGNAL.indication (SIGNAL_DETECT)	SD:M	Yes [ ] N/A [ ]
FS10	Global_PMD_signal_detect during LPI	71.6.4	Detect signal energy during LPI	LPI:M	Yes [ ] N/A [ ]
FS11	Signal Detect for EEE	71.6.4	Transition timing to set SIGNAL_DETECT	LPI:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
FS12	Global_PMD_transmit_disable function	71.6.6	Disables all transmitters by forcing a constant level	TD:M	Yes [ ] N/A [ ]
FS13	PMD_fault global effect	71.6.6	All transmitters disabled if detected	TD:O	Yes [ ] No [ ] N/A [ ]
FS14	Global_PMD_transmit_disable affect on loopback	71.6.6	Loopback function not affected	TD:M	Yes [ ] N/A [ ]
FS15	Global_PMD_transmit_disable during LPI	71.6.6	Disable transmitters during tx_quiet	LPI:M	Yes [ ] N/A [ ]
FS16	PMD_transmit_disable_n function implemented	71.6.7		M	Yes [ ]
FS17	PMD_transmit_disable_n action when enabled	71.6.7	Disables transmitter by forcing a constant level	M	Yes [ ]
FS18	PMD_transmit_disable_n affect on loopback	71.6.7	Loopback function not affected	M	Yes [ ]
FS19	Loopback Function	71.6.8	Loopback function provided	M	Yes [ ]
FS20	Loopback affect on transmitters	71.6.8	Loopback function does not disable transmitters	M	Yes [ ]
FS21	LPI function	71.6.12	PMD_RXQUIET.request and PMD_TXQUIET.request supported	LPI:M	Yes [ ] No [ ] N/A [ ]

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71.10.4.3 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	MDIO Variable Mapping	71.5	Per Table 71–2 and Table 71–3	MD:M	Yes [ ] N/A [ ]
MF2	Lane-by-Lane Signal Detect function	71.6.5	Sets PMD_signal_detect_n values on a lane-by-lane basis per requirements of 71.6.5	MD*SD:M	Yes [ ] N/A [ ]
MF3	Lane-by-Lane Signal Detect function not implemented	71.6.5	PMD_signal_detect_n continuously indicated as OK	MD*!SD:M	Yes [ ] N/A [ ]
MF4	PMD_fault function	71.6.9	Sets PMD_fault to a logical 1 if any local fault is detected; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]
MF5	PMD_transmit_fault function	71.6.10	Sets PMD_transmit_fault to a logical 1 if any local fault is detected on the transmit path; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]
MF6	PMD_receive_fault function	71.6.11	Sets PMD_receive_fault to a logical 1 if any local fault is detected on the receive path; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]

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71.10.4.4 Transmitter electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	100 Ω differential test fixture	71.7.1.2	With return loss > 20 dB from 100 MHz to 2000 MHz	M	Yes [ ]
TC2	Signaling speed	71.7.1.3	3.125 GBd ± 100 ppm	M	Yes [ ]
TC3	Maximum transmitter differential peak-to-peak voltage	71.7.1.4	Less than 1200 mV	M	Yes [ ]
TC4	Minimum transmitter differential peak-to-peak voltage	71.7.1.4	Greater than 800 mV	M	Yes [ ]
TC5	Maximum transmitter differential peak-to-peak voltage difference	71.7.1.4	Less than or equal to 150 mV	M	Yes [ ]
TC6	Common-mode output voltage	71.7.1.4	Between –0.4 V and 1.9 V	M	Yes [ ]
TC7	Output Amplitude LPI voltage	71.7.1.4	Less than 30 mV within 500 ns of tx_quiet	LPI:M	Yes [ ] N/A [ ]
TC8	Output Amplitude ON voltage	71.7.1.4	Greater than 720 mV within 500 ns of tx_quiet de-asserted	LPI:M	Yes [ ] N/A [ ]
TC9	Output Return Loss	71.7.1.5	Per Equation (71–1) and Equation (71–2)	M	Yes [ ]
TC10	Reference Impedance	71.7.1.5	100 Ω for differential return loss measurements	M	Yes [ ]
TC11	Output within transmit template per Figure 71–5	71.7.1.6	While sending pattern specified in 48A.2, with all other transmitters active	M	Yes [ ]
TC12	Other transmitters terminated	71.7.1.6	Per 71.7.1.2	M	Yes [ ]
TC13	Transmitter output normalization	71.7.1.6	Per defined process	M	Yes [ ]
TC14	Transmit jitter, peak-to-peak	71.7.1.8	See 71.7.1.9. Max TJ of 0.35 UI. Max DJ of 0.17 UI. Max RJ of 0.27 UI	M	Yes [ ]
TC15	Jitter test patterns	71.7.1.9	Per 48A.5	M	Yes [ ]
TC16	Other transmitters during jitter test	71.7.1.9	Other transmitters active and terminated per 71.7.1.2	M	Yes [ ]

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71.10.4.5 Receiver electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Receiver interference tolerance	71.7.2.1	Per Annex 69A with parameters specified in Table 71–6	M	Yes [ ]
RC2	Receiver interference tolerance test pattern	71.7.2.1	Per 71.7.2.1	M	Yes [ ]
RC3	Receiver interference tolerance requirements	71.7.2.1	Satisfy requirements per Annex 69A	M	Yes [ ]
RC4	Signaling speed	71.7.2.2	3.125 GBd ±100 ppm	M	Yes [ ]
RC5	Receiver AC-coupled	71.7.2.3		M	Yes [ ]
RC6	Input signal amplitude	71.7.2.4	BER still met when compliant transmitter is connected with no attenuation	M	Yes [ ]
RC7	Differential return loss	71.7.2.5	Per Equation (71–1) and Equation (71–2)	M	Yes [ ]

71.10.4.6 Environmental and safety specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	71.9.1	Conforms to J.2	M	Yes [ ]
ES2	Electromagnetic compatibility	71.9.4	Comply with applicable local and national codes	M	Yes [ ]

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72. Physical Medium Dependent sublayer and baseband medium, type 10GBASE-KR

72.1 Overview

This clause specifies the 10GBASE-KR PMD and the baseband medium. When forming a complete PHY, a PMD shall be connected to the appropriate sublayers (see Table 72–1), and with the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 72–1—Physical Layer clauses associated with the 10GBASE-KR PMD

Associated clause	10GBASE-KR
46—XGMII[a]	Optional
47—XGXS and XAUI	Optional
49—10GBASE-R PCS	Required
51—10-Gigabit Serial PMA	Required
73—Auto-Negotiation for Backplane Ethernet	Required
74—BASE-R FEC	Optional
78—Energy-Efficient Ethernet	Optional

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation behaves functionally as though the RS and XGMII were present.

A 10GBASE-KR PHY with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization. The “Assert LPI” request at the XGMII is encoded in the transmitted symbols. Detection of LPI signaling in the received symbols is indicated as “Assert LPI” at the XGMII. Upon the detection of “Assert LPI” at the XGMII, an energy-efficient 10GBASE-KR PHY continues transmitting for a predefined period, then ceases transmission and deactivates transmit functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g., timing recovery, adaptive filter coefficients) and thereby track long-term variations in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal interframes resume at the XGMII, the PHY reactivates transmit functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the LPI mode.

72.2 Physical Medium Dependent (PMD) service interface

The 10GBASE-KR PMD utilizes the PMD service interface defined in 52.1.1. The PMD service interface is summarized as follows:

a) PMD_UNITDATA.request (as defined in 52.1.1)
b) PMD_UNITDATA.indication (as defined in 52.1.1)
c) PMD_SIGNAL.indication

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If EEE is supported, the following primitives are also defined on the PMD Service Interface:

PMD_RX_MODE.request(rx_mode)
PMD_TX_MODE.request(tx_mode)

These messages affect the PCS variables as described in 49.2.13.2.2.

72.2.1 PMD_RX_MODE.request

This primitive is generated by the PCS Receive Process when EEE is supported to indicate that the input signal is quiet and the PMA and PMD receiver may go into a low power mode. When EEE is not supported, the primitive is never invoked and the PMD behaves as if rx_mode = DATA.

72.2.1.1 Semantics of the service primitive

PMD_RX_MODE.request (rx_mode)

The rx_mode parameter takes on one of two values: QUIET or DATA.

72.2.1.2 When generated

The PCS generates this primitive to request the appropriate PMD receive LPI state.

72.2.1.3 Effect of receipt

When rx_mode is QUIET, the PMD receive function may deactivate functional blocks to conserve energy. When rx_mode is DATA, the PMD receive function operates normally.

72.2.2 PMD_TX_MODE.request

This primitive is generated by the PCS Transmit Process when EEE is supported to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. See subclause 72.6.5. When EEE is not supported, the primitive is never invoked and the PMD behaves as if tx_mode = DATA.

72.2.2.1 Semantics of the service primitive

PMD_TX_MODE.request (tx_mode)

The tx_mode parameter takes on one of three values: QUIET, ALERT, or DATA.

72.2.2.2 When generated

The PCS generates this primitive to request appropriate PMD transmit LPI state.

72.2.2.3 Effect of receipt

When tx_mode is QUIET, the PMD Transmit function may deactivate functional blocks to conserve energy. When tx_mode is ALERT, the PMD Transmit function transmits the alert pattern. And when it is DATA, the PMD Transmit function operates normally.

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72.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD shall support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 49.2.16.)

72.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers consider the delay maxima, and that network planners and administrators consider the delay constraints regarding concatenation of devices. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 69.3.

The sum of the transmit and the receive delays contributed by the 10GBASE-KR PMD and medium shall be no more than 1024 bit times. It is assumed that the round-trip delay through the medium is 160 bit times.

72.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control variables to PMD control variables as shown in Table 72–2, and MDIO status variables to PMD status variables as shown in Table 72–3.

Table 72–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
Global PMD Transmit Disable	Transmit disable register	1.9.0	Global_PMD_transmit_disable
Restart training	BASE-R PMD control register	1.150.0	mr_restart_training
Training enable	BASE-R PMD control register	1.150.1	mr_training_enable

72.6 PMD functional specifications

72.6.1 Link block diagram

For purposes of system conformance, the PMD sublayer is standardized at test points TP1 and TP4 as shown in Figure 72–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

The electrical path from the transmitter block to TP1, and from TP4 to the receiver block, will affect link performance and the measured values of electrical parameters used to verify conformance to this standard. Therefore, it is recommended that this path be carefully designed.

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Table 72–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD Receive signal detect	Receive signal detect register	1.10.0	Global_PMD_signal_detect
Receiver status	BASE-R PMD status register	1.151.0	rx_trained
Frame lock	BASE-R PMD status register	1.151.1	frame_lock
Startup protocol status	BASE-R PMD status register	1.151.2	training
Training failure	BASE-R PMD status register	1.151.3	training_failure

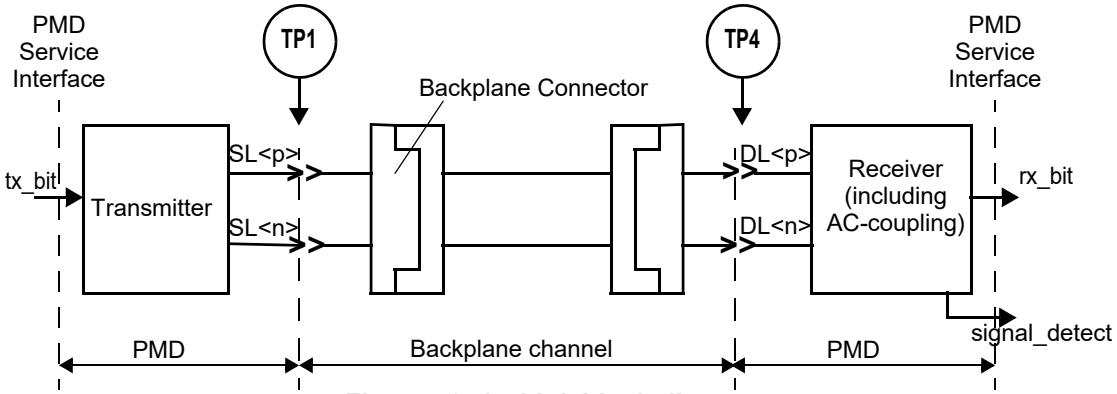

Figure 72–1—Link block diagram

72.6.2 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the specifications in this clause. A positive output voltage of SL<p> minus SL<n> (differential voltage) shall correspond to tx_bit = ONE.

If the optional Energy-Efficient Ethernet (EEE) capability is supported (see Clause 78) then when tx_mode is set to ALERT, the PMD will transmit a repeating 16-bit pattern, hexadecimal 0xFF00. When tx_mode is ALERT, the transmitter equalizer taps are set to the preset state specified in 72.6.10.2.3.1. When tx_mode is DATA, the driver coeffcients are restored to their states resolved during training.

72.6.3 PMD receive function

The PMD Receive function shall convey the bits received from the MDI according to the electrical specifications in this clause to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). A positive input voltage of DL<p> minus DL<n> (differential voltage) shall correspond to rx_bit = ONE.

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72.6.4 PMD signal detect function

The Global PMD signal detect function shall report to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indication is used by 10GBASE-KR to indicate the successful completion of the startup protocol. When the PHY supports the optional EEE capability, PMD_SIGNAL.indication is also used to indicate when the ALERT signal is detected, which corresponds to the beginning of a refresh or a wake. If the MDIO interface is implemented, then Global_PMD_signal_detect (1.10.0) shall be continuously set to the value of SIGNAL_DETECT as described in 45.2.1.9.7.

The value of the SIGNAL_DETECT is defined by the training state diagram shown in Figure 72–5 when the PHY does not support the EEE capability or if the PHY supports the EEE capability and rx_mode is set to DATA. When the PHY supports the EEE capability, SIGNAL_DETECT is set to FAIL following a transition from rx_mode = DATA to rx_mode = QUIET. When rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input that is the output of a channel that satisfies the requirements of all the parameters of both interference tolerance test channels defined in 72.7.2.1 when driven by a square wave pattern with a period of 16 unit intervals and peak-to-peak differential output amplitude of 720 mV. While rx_mode = QUIET, SIGNAL_DETECT changes from FAIL to OK only after a valid ALERT signal is applied to the channel.

SIGNAL_DETECT shall be set to FAIL following system reset or the manual reset of the training state diagram. Upon completion of training, SIGNAL_DETECT shall be set to OK.

If training is disabled by management and EEE is not implemented, SIGNAL_DETECT shall be set to OK.

72.6.5 PMD transmit disable function

The Global_PMD_transmit_disable function is mandatory if EEE is supported and is otherwise optional. When this function is supported, it shall meet the requirements of this subclause.

a) When the Global_PMD_transmit_disable variable is set to ONE, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 72–6.
b) If a PMD_fault (72.6.7) is detected, then the PMD may turn off the electrical transmitter.
c) Loopback, as defined in 72.6.6, shall not be affected by Global_PMD_transmit_disable.
d) For EEE capability, the PMD_transmit_disable function shall turn off the transmitter after tx_mode is set to QUIET within a time and voltage level specified in 72.7.1.4. The PMD_transmit_disable function shall turn on the transmitter after tx_mode is set to DATA or ALERT within the time and voltage level specified in 72.7.1.4.

If the MDIO interface is implemented, then this function shall map to the Global_PMD_transmit_disable bit as specified in 45.2.1.8.7.

72.6.6 Loopback mode

Loopback mode shall be provided for the 10GBASE-KR PMD by the transmitter and receiver of a device as a test function to the device. When loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. Note, this bit does not affect the state of the transmitter. The method of implementing loopback mode is not defined by this standard.

Control of the loopback function is specified in 45.2.1.1.5.

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NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

72.6.7 PMD_fault function

If the MDIO is implemented, PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault.

72.6.8 PMD transmit fault function

The PMD_transmit_fault function is optional. The faults detected by this function are implementation specific, but should not include the assertion of the Global_PMD_transmit_disable function.

If a PMD_transmit_fault (optional) is detected, then the Global_PMD_transmit_disable function should also be asserted.

If the MDIO interface is implemented, then this function shall be mapped to the PMD_transmit_fault bit as specified in 45.2.1.7.4.

72.6.9 PMD receive fault function

The PMD_receive_fault function is optional. The faults detected by this function are implementation specific.

If the MDIO interface is implemented, then this function shall contribute to PMA/PMD receive fault bit as specified in 45.2.1.7.5.

72.6.10 PMD control function

72.6.10.1 Overview

The PMD control function generates the control actions required to bring the PMD from initialization to a mode in which data may be exchanged with the link partner.

The PMD control function implements the 10GBASE-KR startup protocol. This protocol facilitates timing recovery and equalization while also providing a mechanism through which the receiver can tune the transmit equalizer to optimize performance over the backplane interconnect. The protocol supports these mechanisms through the continuous exchange of fixed-length training frames.

If EEE is supported, the PMD control function responds to PCS requests to transition in and out of quiet states.

72.6.10.2 Training frame structure

The training frame is a fixed length structure that is sent continuously during training. The training frame, shown in Figure 72–2, is 548 octets in length and contains a control channel and training pattern.

The control channel is signaled using differential Manchester encoding (DME) at a signaling rate equal to one quarter of the 10GBASE-KR signaling rate. Since each DME symbol contains two DME transition positions and each transition position is four 10GBASE-KR UI, one control channel bit is transmitted every eight 10GBASE-KR UI.

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Differential Manchester encoding guarantees transition density and DC balance while the reduced rate of transmission facilitates reception over non-optimally equalized channels.[134]

Training frames are delimited by a fixed 4 octet frame marker.

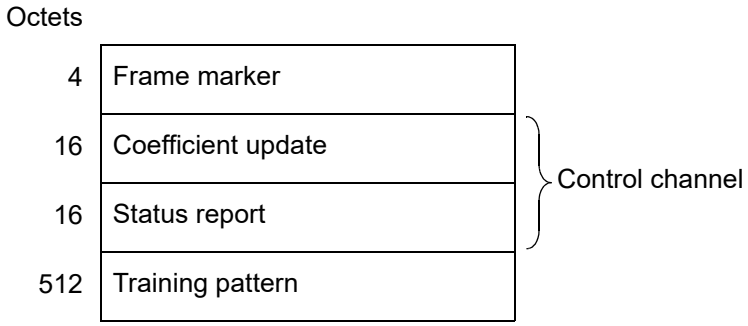

Figure 72–2—Training frame structure

72.6.10.2.1 Frame marker

Frames are delimited by the 32-bit pattern, hexadecimal 0xFFFF0000 (ones transmitted first), as expressed in 10.3125 Gbd symbols. This pattern does not appear in the control channel or the training pattern and therefore serves as a unique indicator of the start of a training frame.

72.6.10.2.2 Control channel encoding

The control channel shall be transmitted using differential Manchester encoding (DME). The rules of differential Manchester encoding are as follows:

a) A data transition shall occur at each cell boundary.
b) A mid-cell data transition shall be used to signal a logical one.
c) The absence of a mid-cell data transition shall be used to signal a logical zero.

If a coding violation is detected within the bounds of the control channel in a given training frame, the contents of the control channel for that frame shall be ignored.

The data cell length shall be 8 10GBASE-KR UI. Therefore, the total length of the control channel is 256 10GBASE-KR UI.

72.6.10.2.3 Coefficient update field

The coefficient update field carries correction information from the local receiver to the link partner transmit equalizer. The field consists of preset controls, initialization controls, and coefficient updates for three transmit equalizer taps. The format of the coefficient update field shall be as shown in Table 72–4. Cell 15 of the coefficient update field sent shall be transmitted first. The preset, initialize, and coefficient updates are set by the receiver adaptation process. The algorithm employed by the receiver adaptation process is beyond the scope of this standard.

[134]The differential Manchester encoding defined for Backplane Ethernet is different from that defined in IEEE Std 802.5™.

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Table 72–4—Coefficient update field

Cell(s)	Name	Description
15:14	Reserved	Transmitted as 0, ignored on reception.
13	Preset	1 = Preset coefficients 0 = Normal operation
12	Initialize	1 = Initialize coefficients 0 = Normal operation
11:6	Reserved	Transmitted as 0, ignored on reception.
5:4	Coefficient (+1) update	5 4 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold
3:2	Coefficient (0) update	3 2 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold
1:0	Coefficient (–1) update	1 0 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold

72.6.10.2.3.1 Preset

The preset control is sent to request that the coefficients be set to a state where equalization is turned off. When received, the pre-cursor ($k = -1$) and post-cursor ($k = +1$) coefficients shall be set to a zero value and the main ($k = 0$) coefficient shall be set to its maximum value. The preset control shall only be initially sent when all coefficient status fields indicate not_updated, and will then continue to be sent until the status for all coefficients indicates updated or maximum. At that point, the outgoing preset control shall be set to zero. Maximum status shall be returned when the main coefficient is updated. Maximum status shall be returned for the pre-cursor and/or post-cursor coefficients when the coefficient is updated and zero is its maximum supported value. Updated status shall be returned for the pre-cursor and/or post-cursor coefficients when the coefficient is updated and it supports additional settings above the value zero.

A new request to preset or initialize shall not be sent until the incoming status messages for all coefficients revert to not_updated. Preset shall not be sent in combination with initialize or coefficient increment/decrement requests.

72.6.10.2.3.2 Initialize

The initialize control is sent to request that the coefficients be set to configure the transmit equalizer to its INITIALIZE state. When received, the taps shall be set such that the transmit output meets the conditions defined in 72.6.10.4.2. The initialize control shall only be initially sent when all coefficient status fields indicate not_updated, and will then continue to be sent until no coefficient status field indicates not_updated.

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Updated status shall be returned for each coefficient when the coefficient update is completed. At that point, the outgoing initialize control shall be set to zero.

A new request to preset or initialize shall not be sent until the incoming status messages for all coefficients revert to not_updated. Initialize shall not be sent in combination with coefficient increment/decrement requests or preset.

72.6.10.2.3.3 Coefficient (*k*) update

Each coefficient, *k*, is assigned a 2-bit field describing a requested update. Three request encodings are defined: increment, decrement, and hold. The default state for a given tap is hold, which corresponds to no change in the coefficient. The increment or decrement encodings are transmitted to request that the corresponding coefficient be increased or decreased. The amount of change implemented by the transmitter in response to the coefficient update request shall meet the requirements of Table 72–7 and 72.7.1.10. An increment or decrement request shall continue to be transmitted until the update status for that tap (as defined in 72.6.10.2.4.5) indicates updated, maximum, or minimum. At that point, the outgoing requests for that tap shall be set to hold.

A new request to increment or decrement shall not be sent before the incoming status messages for that tap revert to not_updated. Coefficient increment/decrement shall not be sent in combination with initialize or preset.

The valid range for *k* is –1 to +1 where *k* = 0 denotes the main tap. The encoding of the coefficient update shall be as shown in Table 72–4.

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72.6.10.2.4 Status report field

The status report field is used to signal state information from the local PMD to the link partner. The format of the status report field shall be as shown in Table 72–5. Cell 15 of the status report field shall be transmitted first.

Table 72–5—Status report field

Cell(s)	Name	Description
15	Receiver ready	1 = The local receiver has determined that training is complete and is prepared to receive data. 0 = The local receiver is requesting that training continue.
14:6	Reserved	Transmitted as 0, ignored on reception.
5:4	Coefficient (+1) status	5 4 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated
3:2	Coefficient (0) status	3 2 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated
1:0	Coefficient (–1) status	1 0 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated

72.6.10.2.4.4 Receiver ready

The receiver ready bit is used to signal the local receiver state to the link partner. When asserted, the receiver ready bit indicates that the local receiver has concluded training and is prepared to receive data. When de-asserted, the receiver ready bit indicates that the local receiver is requesting that training continue. The format of the receiver ready bit shall be as shown in Table 72–5.

72.6.10.2.4.5 Coefficient (*k*) status

Each coefficient, *k*, is assigned a 2-bit field describing the status of pending updates to the coefficient. Four status encodings are defined: not updated, updated, maximum, and minimum.

These status encodings indicate the corresponding state of the coefficient update state diagram for coefficient *k*.

The valid range for *k* is –1 to +1 where *k* = 0 denotes the main tap. The encoding of the coefficient update shall be as shown in Table 72–5.

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72.6.10.2.5 Coefficient update process

Each coefficient, k, has an associated coefficient update state diagram that controls updates of the coefficient and generates the tap update status field.

The default state for a given tap is not_updated. An increment or decrement request will only be acted upon when the state of the tap is not_updated. Upon execution of a received increment or decrement request, the status is reported as updated, maximum, or minimum. Maximum is reported if a received increment request causes the tap value to reach its maximum limit, or if it is already at that limit. Minimum is reported if a received decrement request causes the tap value to reach its minimum limit, or if it is already at that limit.

Once the updated, maximum, or minimum state is reported it continues to be reported until a hold request is received, after which the status reverts to not_updated.

The coefficient update process responds to coefficient requests as specified in the state diagram shown in Figure 72–6.

72.6.10.2.6 Training pattern

The training pattern shall be a 512 octet pattern consisting of 4094 bits from the output of a pseudo-random bit sequence of order 11 (PRBS11) generator followed by two zeros. The PRBS11 pattern generator shall produce the same result as the implementation shown in Figure 72–3. This implements the generator polynomial shown in Equation (72–1).

$$G(x) = 1 + x^9 + x^{11} \tag{72–1}$$

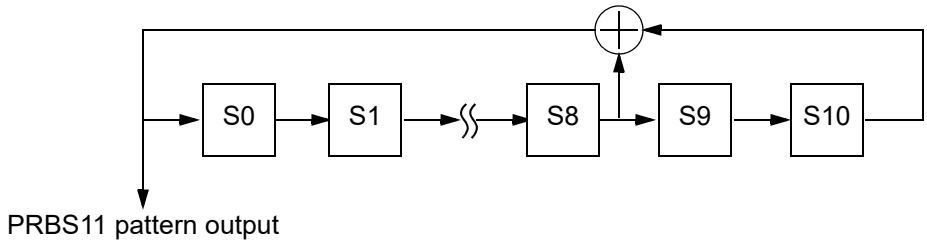

Figure 72–3—PRBS11 pattern generator

The pseudo-random generator shall have a random seed at the start of the training pattern. Each bit of the training pattern is transmitted as a single 10.3125 GBd symbol.

72.6.10.3 State variables

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

72.6.10.3.1 Variables

coefficient
: Integer variable containing a value that should be used as the tap coefficient.

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dec

Boolean variable that is set to TRUE when a training frame has been completely received and the coefficient update field of that frame for this coefficient is decrement, and is set to FALSE on reception of any other value.

frame_lock

Boolean variable that is set to TRUE when the receiver acquires training frame delineation and is set to FALSE otherwise.

frame_offset

Boolean variable that is set to TRUE after receiving one full training frame (548 octets) from the current frame start position. The Boolean variable is set to FALSE when the GET_NEW_MARKER state is entered. The current frame start position is indicated by a transition into the GET_NEW_MARKER state when the Boolean variable is set to FALSE.

hold

Boolean variable that is set to TRUE when a training frame has been completely received and the coefficient update field of that frame for this coefficient is hold, and neither preset or initialize are activated, and is set to FALSE on reception of any other value.

inc

Boolean variable that is set to TRUE when a training frame has been completely received and the coefficient update field of that frame for this coefficient is increment, and set to FALSE on reception of any other value.

initialize

Boolean variable that is set to TRUE when a training frame has been completely received and the initialize field of that frame is set to one and the preset field is set to zero, and is set to FALSE otherwise.

local_rx_ready

Boolean variable that is set to TRUE by the training state diagram when rx_trained is asserted and is set to FALSE otherwise. This value is transmitted as the receiver ready bit on all outgoing training frames.

marker_valid

Boolean variable that is set to TRUE when the candidate frame marker matches the specified frame marker pattern and is set to FALSE when the candidate frame marker does not match the specified frame marker pattern.

max_limit

Integer variable containing the maximum tap coefficient value, subject to the constraints detailed in 72.7.1.10.

min_limit

Integer variable containing the minimum tap coefficient value, subject to the constraints detailed in 72.7.1.10.

mr_restart_training

Boolean variable used by system management to restart the 10GBASE-KR startup protocol. When set to TRUE, it forces the training state diagram to the INITIALIZE state.

mr_training_enable

Boolean variable used by system management to enable or disable the 10GBASE-KR startup

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protocol. It is set to TRUE when the startup protocol is enabled and set to FALSE when the startup protocol is disabled.

new_coeff
: Integer variable containing the result of increment/decrement operations on the coefficient value

new_marker
: Boolean variable that is set to TRUE when a new candidate frame marker is available for testing and FALSE when the TEST_MARKER state is entered. A new marker is available for testing when the training frame lock process has accumulated one frame marker (4 octets) from a candidate frame start position.

preset
: Boolean variable that is set to TRUE when a training frame has been completely received and the preset field of that frame is set to one and is set to FALSE if set to zero.

remote_rx_ready
: Boolean variable that is set to FALSE upon entry into the SEND_TRAINING state. The value of remote_rx_ready shall not be set to TRUE until no fewer than three consecutive training frames have been received with the receiver ready bit asserted.

reset
: Boolean variable that controls the resetting of the PMA/PMD. It is set to TRUE whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PMA/PMD into low-power mode.

rx_trained
: Boolean variable that is set to TRUE when the remote transmit and local receive equalizers have been optimized and normal data transmission may commence and set to FALSE otherwise.

signal_detect
: Boolean variable that is set to TRUE when the training process is complete and is set to FALSE otherwise. The value of signal_detect is reported to the PMA sublayer via the PMD_SIGNAL.indication primitive.

slip_done
: Boolean variable that is set to TRUE when the SLIP requested by the Frame Lock State Diagram has been completed indicating that the next candidate frame sync position can be tested.

training
: Boolean variable that is set to TRUE to indicate that the 10GBASE-KR startup protocol is in progress and is set to FALSE when training has completed.

training_failure
: Boolean variable that is set to TRUE when the training state diagram has timed out due to expiration of the max_wait_timer while in the SEND_TRAINING, TRAIN_LOCAL, or TRAIN_REMOTE states and is set to FALSE otherwise.

update_status
: Value to be transmitted in the Coefficient Status field for this coefficient in the next transmitted training frame, as defined in Table 72–8.

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72.6.10.3.2 Timers

max_wait_timer
: This timer is started in the INITIALIZE state of the training state diagram. If the max_wait_timer expires the training state diagram will enter the TRAINING_FAILURE state. The value of max_wait_timer shall be 500 ms ± 1%.

wait_timer
: This timer is started when the local receiver is trained and detects that the remote receiver is ready to receive data. The local PMD will deliver wait_timer additional training frames to ensure that the link partner correctly detects the local receiver state. The value of wait_timer shall be between 100 and 300 training frames.

72.6.10.3.3 Counters

bad_markers
: Count of the number of consecutive frame marker mis-matches.

good_markers
: Count of the number of consecutive frame marker matches.

72.6.10.3.4 Functions

COEFF_UPDATE(coefficient, preset, initialize, inc, dec)
: Returns an updated coefficient based on the contents of the coefficient update field in the training frame. Sets a fixed coefficient value, or adds, or subtracts from the current coefficient value to create the updated coefficient. If multiple actions are requested in the coefficient update field, then the priority is:
  1) preset
  2) initialize
  3) inc/dec

  Values: preset; If preset is TRUE then the function returns the coefficient value equivalent to no equalization [$c(-1)$ and $c(1)$ coefficients are set to zero, $c(0)$ set to maximum].
  initialize; If initialize is TRUE, then the function returns the coefficient value such that the transmit output meets the conditions defined in 72.6.10.4.2.
  inc; If inc is TRUE then the function returns (coefficient + step).
  dec; If dec is TRUE then the function returns (coefficient – step).

  The requirements for the value of step are defined in 72.7.1.10 and Table 72–7.

SLIP
: Causes the next candidate frame sync position to be tested. The precise method for determining the next candidate frame sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

TRANSMIT(TRAINING, DATA)
: Controls the output of the TRANSMIT functional block.

  Values: TRAINING; the transmit block output is a continuous stream of training frames as defined in 72.6.10.2.
  DATA; the transmit block output is determined by the value of the input tx_bit.

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72.6.10.4 State diagrams

72.6.10.4.1 Frame lock

The 10GBASE-KR PMD shall implement the Frame Lock state diagram as depicted in Figure 72–4 including compliance with the associated state variables as specified in 72.6.10.3. The frame lock state diagram determines when the PMD control function has detected the frame boundaries in the received data stream.

72.6.10.4.2 Training

The 10GBASE-KR PMD shall implement the Training state diagram as depicted in Figure 72–5 including compliance with the associated state variables as specified in 72.6.10.3. The training state diagram defines the operation of the 10GBASE-KR startup protocol. When the training state diagram enters the INITIALIZE state, the transmitter equalizer shall be configured such that R_{pre} and R_{pst} are 1.29 ± 10% and 2.57 ± 10% respectively. R_{pre} and R_{pst} are defined in 72.7.1.11. At the start of training the initial value of c(0) shall be set such that the constraints of 72.7.1.11 are satisfied and the peak-to-peak differential output voltage shall be greater than or equal to 800 mV for a 1010 pattern.

72.6.10.4.3 Coefficient update

For each tap, the 10GBASE-KR PMD shall implement an instance of the coefficient update state diagram as depicted in Figure 72–6 including compliance with the associated state variables as specified in 72.6.10.3. The coefficient update state diagram defines the process for updating transmit equalizer coefficients in response to requests from the link partner, and also defines the coefficient update status to be reported in outgoing training frames.

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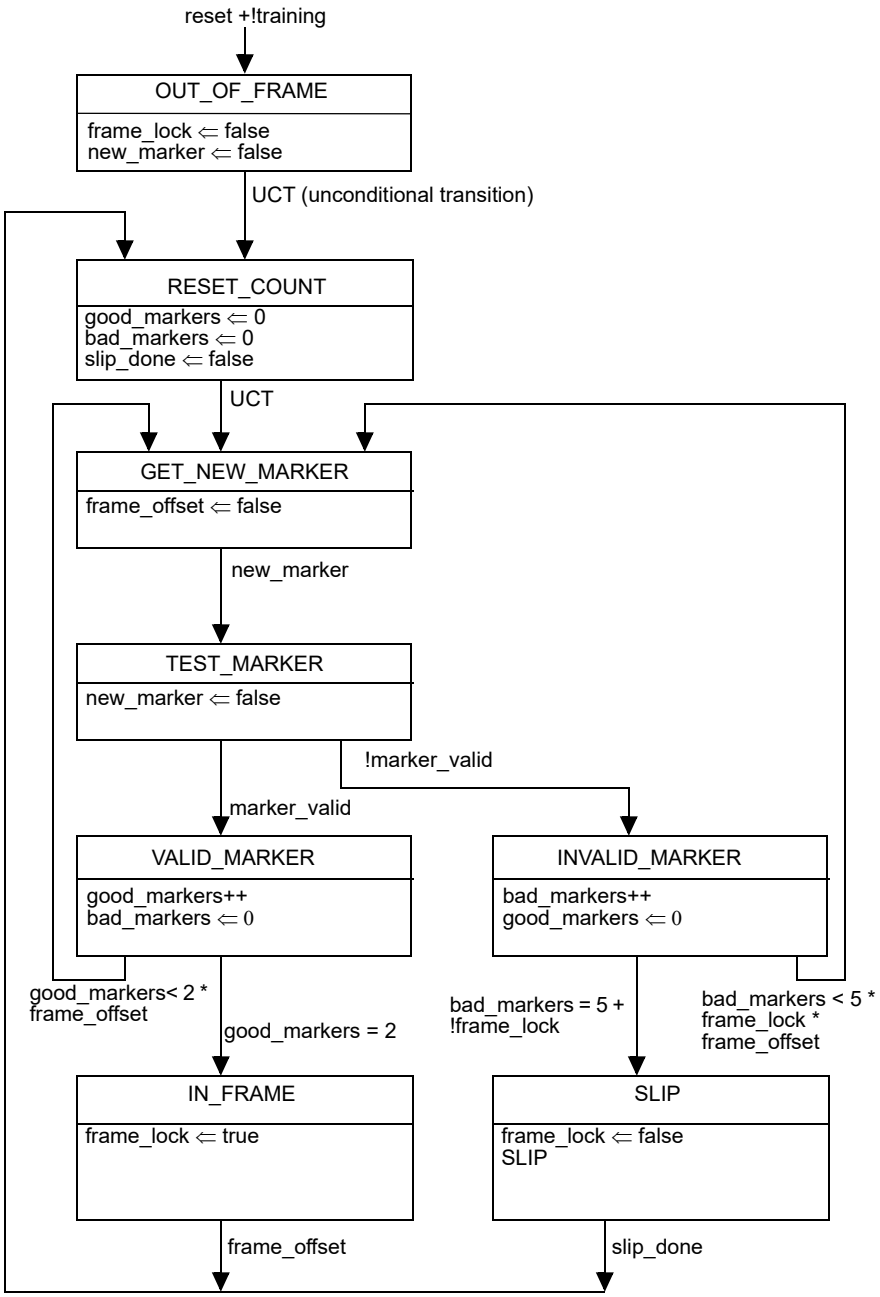

Figure 72–4—Frame lock state diagram

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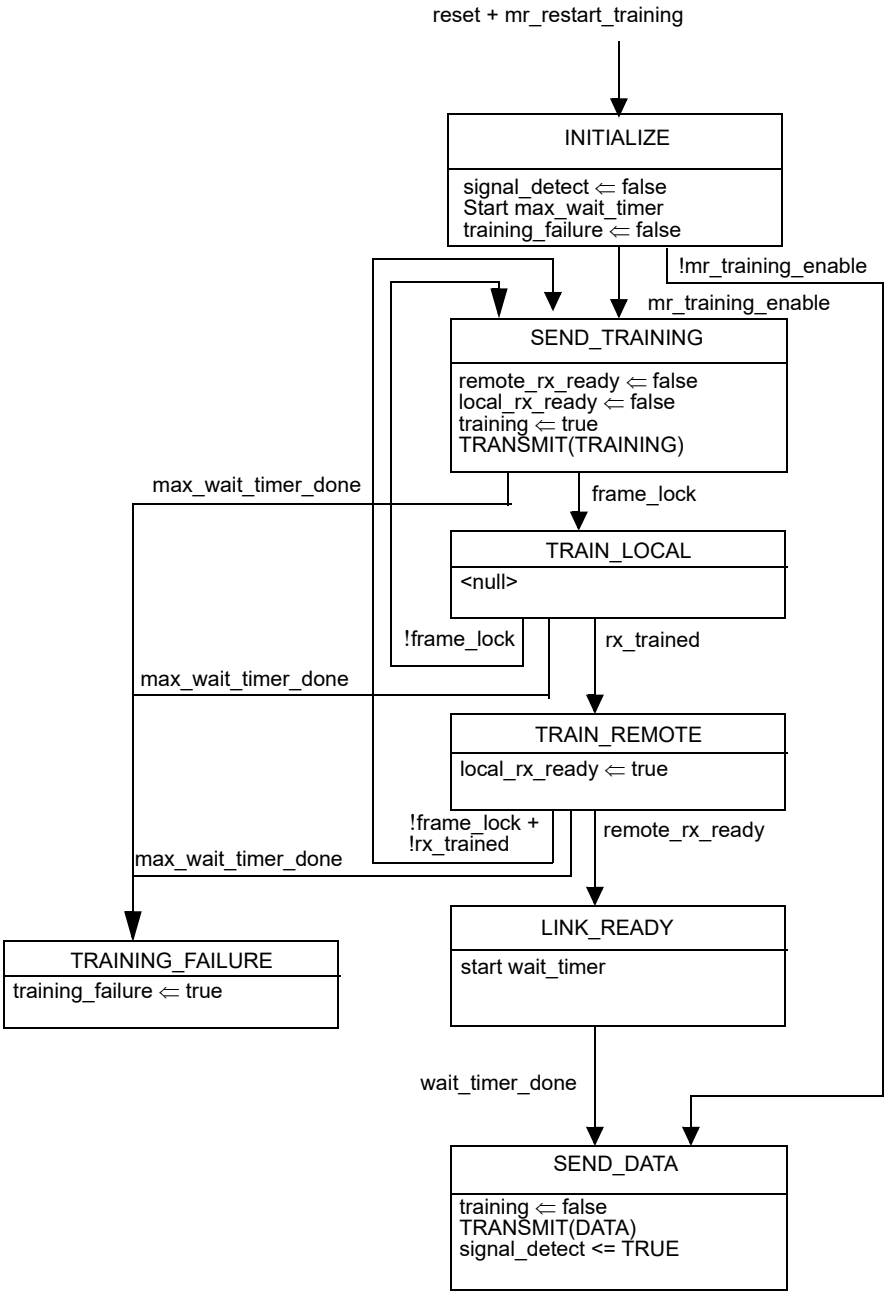

Figure 72–5—Training state diagram

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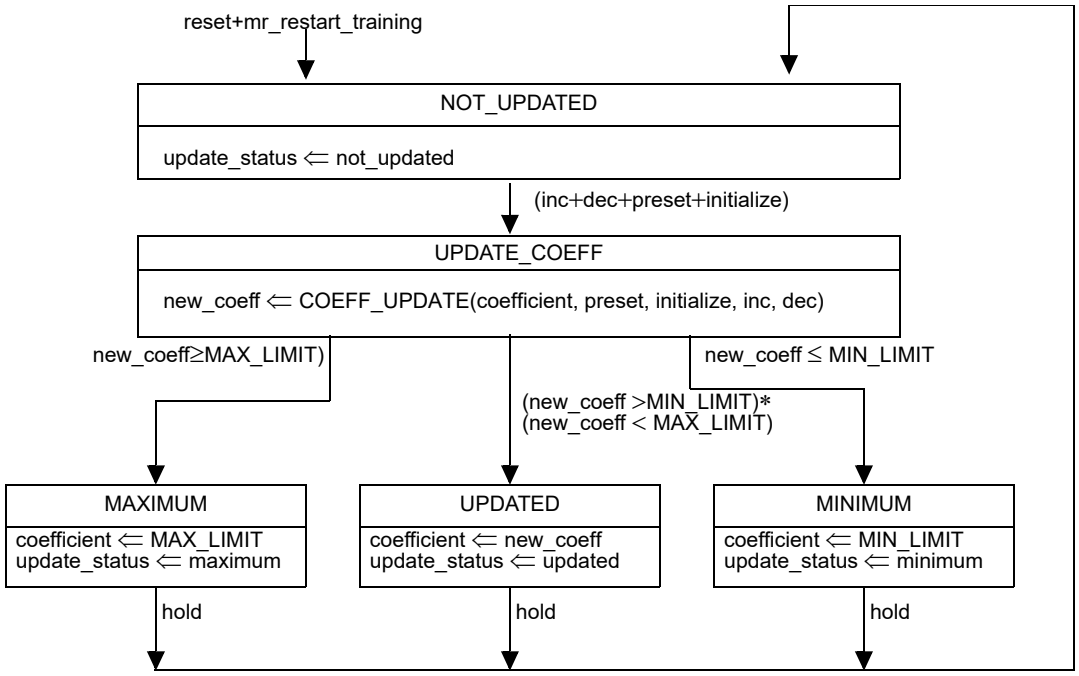

Figure 72–6—Coefficient update state diagram

72.6.11 PMD LPI function

The PMD LPI function responds to the transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD_TX_MODE and PMD_RX_MODE requests. Implementation of the function is optional. EEE capabilities and parameters will be advertised during the Backplane Auto-negotiation, as described in 45.2.7.14. The transmitter on the local device will inform the link partner's receiver when to sleep, refresh and wake. The local receiver transitions are controlled by the link partner's transmitter and can change independent of the local transmitter states and transitions.

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72.7 10GBASE-KR electrical characteristics

72.7.1 Transmitter characteristics

Transmitter characteristics at TP1 are summarized in Table 72–6 and detailed in 72.7.1.1 through 72.7.1.11.

Table 72–6—Transmitter characteristics for 10GBASE-KR

Parameter	Subclause reference	Value	Units
Signaling speed	72.7.1.3	10.3125 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max.)	72.7.1.4	1200	mV
Differential peak-to-peak output voltage (max.) with TX disabled	72.6.5	30	mV
Common-mode voltage limits	72.7.1.4	0 to 1.9	V
Common-mode voltage deviation (max) during LPI	72.7.1.4	150	mV
Differential output return loss (min.)	72.7.1.5	[See Equation (72–4) and Equation (72–5)]	dB
Common-mode output return loss (min.)	72.7.1.6	[See Equation (72–6) and Equation (72–7)]	dB
Transition time (20%–80%)	72.7.1.7	24 to 47	ps
Max output jitter (peak-to-peak) Random jitter[a] Deterministic jitter Duty Cycle Distortion[b] Total jitter	72.7.1.9	 0.15 0.15 0.035 0.28	 UI UI UI UI

[a]Jitter is specified at BER 10^{-12}.
[b]Duty Cycle Distortion is considered part of the deterministic jitter distribution.

72.7.1.1 Test fixture

The test fixture of Figure 72–7 or its functional equivalent, is required for measuring the transmitter specifications described in 72.7.1, with the exception of return loss.

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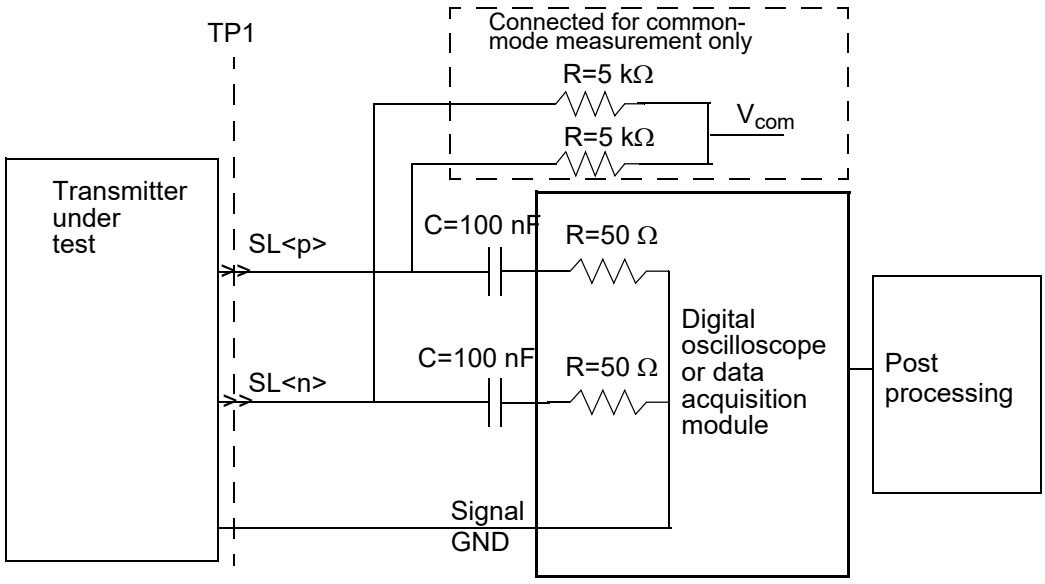

Figure 72–7—Transmit test fixture for 10GBASE-KR

72.7.1.2 Test fixture impedance

The differential load impedance applied to the transmitter output by the test fixture depicted in Figure 72–7 shall be 100 Ω. The differential return loss, in dB with f in MHz, of the test fixture shall meet the requirements of Equation (72–2) and Equation (72–3).

$$ReturnLoss(f) \geq 15 \tag{72–2}$$

for 100 MHz ≤ f < 5000 MHz

$$ReturnLoss(f) \geq 15 - 26.57\log_{10}\left(\frac{f}{5000\ \text{MHz}}\right) \tag{72–3}$$

for 5000 MHz ≤ f ≤ 10000 MHz

72.7.1.3 Signaling speed

The 10GBASE-KR signaling speed shall be 10.3125 GBd ± 100 ppm.

72.7.1.4 Output amplitude

The differential output voltage is constrained via the transmitter output waveform requirements specified in 72.7.1.10. For a 1010 pattern, the peak-to-peak differential output voltage shall be less than 1200 mV, regardless of equalization setting. The transmitter output voltage shall be less than 30 mV peak-to-peak when disabled. The differential output voltage test pattern shall consist of no fewer than eight symbols of alternating polarity.

NOTE 1—The required test patterns may be found in the training pattern field of the training frames or test patterns 2 or 3 as defined in 52.9.1.1.

NOTE 2—See Figure 72–8 for an illustration of the definition of differential peak-to-peak output voltage.

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DC-referenced voltage levels are not defined since the receiver is AC-coupled. The common-mode voltage of SL<p> and SL<n> shall be between 0 V and 1.9 V with respect to signal ground as measured at V_{com} in Figure 72–7.

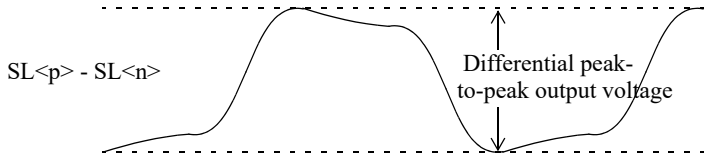

Figure 72–8—Transmitter differential peak-to-peak output voltage definition

NOTE—SL<p> and SL<n> are the positive and negative sides of the differential signal pair.

For EEE capability, the transmitter's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of tx_mode being set to QUIET and remain so while tx_mode is set to QUIET. Furthermore, the transmitter's differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of tx_mode being set to ALERT. The transmitter output shall be fully compliant within 5 μs after tx_mode is set to DATA. During LPI mode, the common-mode shall be maintained to within ± 150 mV of the pre-LPI value.

72.7.1.5 Differential output return loss

For frequencies from 50 MHz to 7500 MHz, the differential return loss, in dB with f in MHz, of the transmitter shall meet the requirements of Equation (72–4) and Equation (72–5). This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$ReturnLoss(f) \geq 9 \tag{72–4}$$

for 50 MHz ≤ f < 2500 MHz

$$ReturnLoss(f) \geq 9 - 12\log_{10}\left(\frac{f}{2500\ \text{MHz}}\right) \tag{72–5}$$

for 2500 MHz ≤ f ≤ 7500 MHz

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The minimum differential output return loss is shown in Figure 72–9.

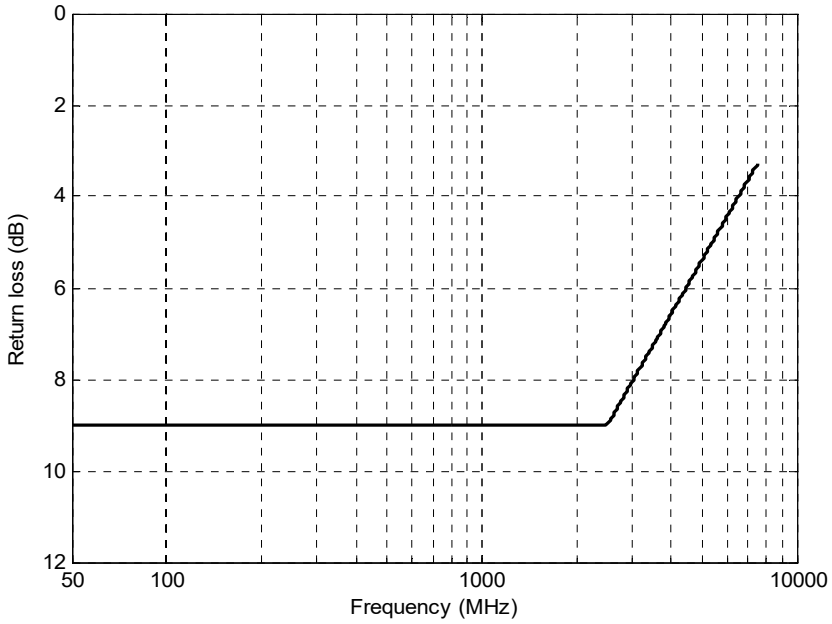

Figure 72–9—Minimum differential output return loss

72.7.1.6 Common-mode output return loss

The transmitter common-mode return loss shall meet the requirements of Equation (72–6) and Equation (72–7). The reference impedance for common-mode return loss measurements is 25 Ω.

$$ReturnLoss(f) \geq 6 \tag{72–6}$$

for 50 MHz ≤ f < 2500 MHz

$$ReturnLoss(f) \geq 6 - 12\log_{10}\left(\frac{f}{2500\ \text{MHz}}\right) \tag{72–7}$$

for 2500 MHz ≤ f ≤ 7500 MHz

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The minimum common-mode output return loss is shown in Figure 72–10.

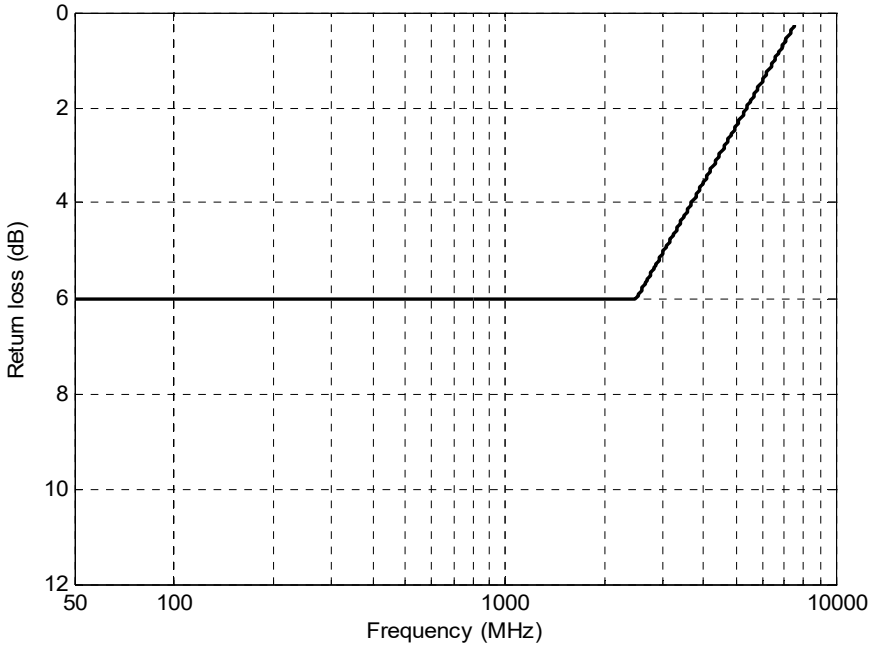

Figure 72–10—Minimum common-mode output return loss

72.7.1.7 Transition time

The rising and falling edge transition times shall be between 24 ps and 47 ps as measured at the 20% and 80% levels referenced to v_2 and v_5 as defined in 72.7.1.11. Measurement is done using the square wave test pattern defined in 52.9.1.2, with no equalization and a run of at least eight consecutive ones. Transmit equalization may be disabled by asserting the preset control defined in Table 45–77 and 45.2.1.97.3.

72.7.1.8 Transmit jitter test requirements

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in Annex 48B.3. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 4 MHz is applied to the jitter. The data pattern for jitter measurements shall be test patterns 2 or 3 as defined in 52.9.1.1. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal. Equalization shall be off during jitter testing. Transmit equalization may be disabled by asserting the preset control defined in Table 45–77 and 45.2.1.97.3.

The duty cycle distortion test pattern shall consist of no fewer than eight symbols of alternating polarity (e.g., a 10101010… bit sequence).

NOTE—The required test patterns may be found in the training pattern field of the training frames or test patterns 2 or 3 as defined in 52.9.1.1.

72.7.1.9 Transmit jitter

The transmitter shall have a maximum total jitter of 0.28 UI peak-to-peak, composed of a maximum deterministic component of 0.15 UI peak-to-peak and a maximum random component of 0.15 UI peak-to-peak. Duty cycle distortion (DCD) is considered a component of deterministic jitter and shall not exceed 0.035 UI peak-to-peak. The peak-to-peak duty cycle distortion is defined as the absolute value of the difference in the mean pulse width of a 1 pulse or the mean pulse width of a 0 pulse (as measured at the mean of the high and

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low voltage levels in a repeating 0101 bit sequence) and the nominal pulse width. Jitter specifications are specified for BER 10^{-12}. Transmit jitter test requirements are specified in 72.7.1.8.

72.7.1.10 Transmitter output waveform

The 10GBASE-KR transmitter includes programmable equalization to compensate for frequency-dependent loss in the backplane channel and facilitate data recovery at the receiver. This equalization may be accomplished with a three-tap finite impulse response (FIR) structure as shown in Figure 72–11. The actual implementation of the transmit equalizer, including the incorporation of additional taps, is beyond the scope of this standard.

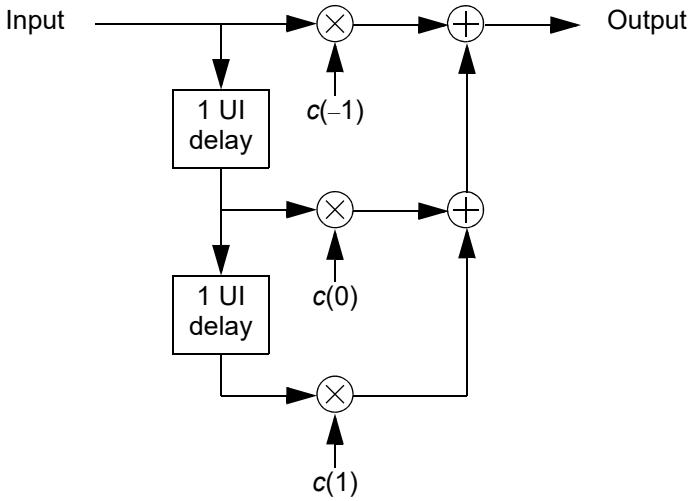

Figure 72–11—Transmit equalizer example

Transmit equalizer performance is specified in terms of the voltages defined in 72.7.1.11. It should be noted that the valid ranges of the $c(1)$ and $c(–1)$ coefficients may include positive and negative values. A value of zero is used to turn off equalization for the tap.

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72.7.1.11 Transmitter output waveform requirements

The test pattern for the transmitter output waveform is the square wave test pattern defined in 52.9.1.2, with a run of at least eight consecutive ones. The transmitter output waveform test is based on the voltages v_1 through v_6, Δv_2, and Δv_5, which shall be measured as shown in Figure 72–12 and described below.

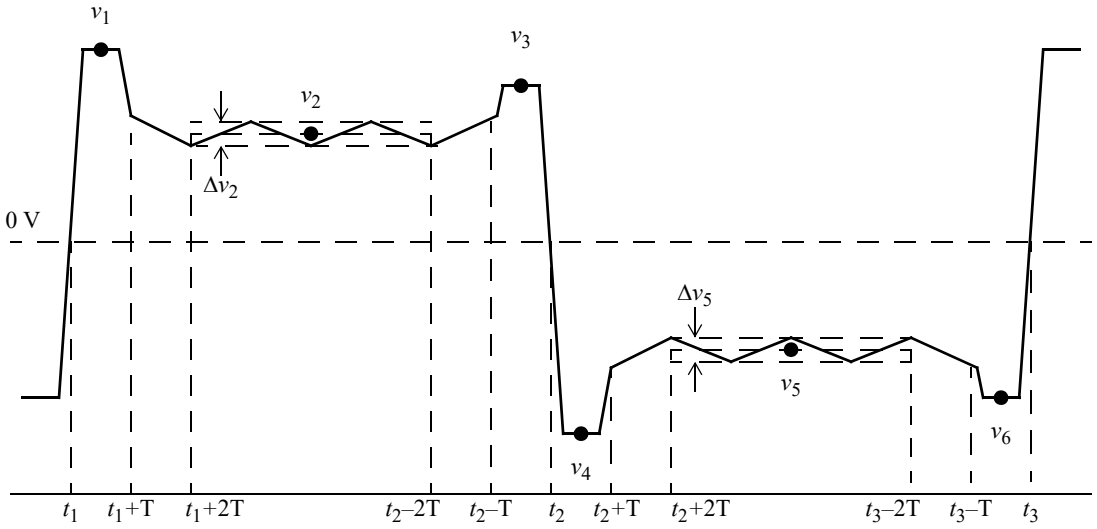

Figure 72–12—Transmitter output waveform

T	=	symbol period
t_1	=	zero-crossing point of the first rising edge of the AC-coupled signal
t_2	=	zero-crossing point of the falling edge of the AC-coupled signal
t_3	=	zero-crossing point of the second rising edge of the AC-coupled signal
v_1	=	maximum voltage measured in the interval t_1 to t_1 + T
v_2	=	positive steady-state voltage measured as the average voltage in the interval t_1 + 2T to t_2 – 2T
v_3	=	maximum voltage measured in the interval t_2 – T to t_2
v_4	=	minimum voltage measured in the interval t_2 to t_2 + T
v_5	=	negative steady-state voltage measured as the average voltage in the interval t_2 + 2T to t_3 – 2T
v_6	=	minimum voltage measured in the interval t_3 – T to t_3
Δv_2	=	positive voltage ripple measured as the peak-to-peak value of the difference between the voltage in the range t_1 + 2T to t_2 – 2T and v_2
Δv_5	=	negative voltage ripple measured as the peak-to-peak value of the difference between the voltage in the range t_2 + 2T to t_3 – 2T and v_5

From these voltages, the pre- and post-cursor equalization ratios R_{pre} and R_{pst} are derived from Equation (72–8) and Equation (72–9).

$$R_{pre} = \frac{v_3}{v_2} \tag{72–8}$$

$$R_{pst} = \frac{v_1}{v_2} \tag{72–9}$$

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The state of the transmitter equalizer and hence the transmitter output waveform is manipulated via the protocol defined in 72.6.10 or via management. The changes in the transmitter output waveform resulting from coefficient update requests shall meet the requirements stated in Table 72–7. The coefficient update requests in Table 72–7 are to be followed by a coefficient update equal to hold for all taps. The results shall be verified after the coefficient status for all taps is reported as not_updated.

Table 72–7—Transmitter output waveform requirements related to coefficient update

Coefficient update[a]			Requirements[b]		
$c(1)$	$c(0)$	$c(-1)$	$v_1(k) - v_1(k-1)$ (mV)	$v_2(k) - v_2(k-1)$ (mV)	$v_3(k) - v_3(k-1)$ (mV)
increment	hold	hold	–20 to –5	5 to 20	5 to 20
decrement	hold	hold	5 to 20	–20 to –5	–20 to –5
hold	increment	hold	5 to 20	5 to 20	5 to 20
hold	decrement	hold	–20 to –5	–20 to –5	–20 to –5
hold	hold	increment	5 to 20	5 to 20	–20 to –5
hold	hold	decrement	–20 to –5	–20 to –5	5 to 20

[a]Step size requirements for the tap under test apply regardless of the current value of the other taps.
[b]This difference is measured relative to the voltage prior to the assertion coefficient update k equal to hold.

For any coefficient update, the magnitudes of the changes in v_1, v_2, and v_3 shall be within 5 mV of each other. When sufficient increment or decrement updates have been applied to a given tap, it will reach a maximum or minimum limit governed by the coefficient range or by restrictions placed on minimum steady-state or maximum peak voltage, and the coefficient status is reported accordingly. The transmitter output waveform shall meet the requirements of Table 72–8 for all of the limiting cases represented in the table. Implementation of $c(-1)$ or $c(1)$ coefficient values greater than zero or less than the minimum defined by R_{pre} (min) and R_{pst} (min) is optional. A coefficient may be disabled by first asserting the preset control defined in Table 45–215 and 45.2.1.97, then manipulating the other coefficients as required by the test.

Table 72–8—Transmitter output waveform requirements related to coefficient status

Coefficient status			Requirements		
$c(1)$	$c(0)$	$c(-1)$	R_{pre}	R_{pst}	v_2 (mV)
disabled	minimum	disabled	0.90 to 1.10	0.90 to 1.10	220 to 330
disabled	maximum	disabled	0.95 to 1.05	0.95 to 1.05	400 to 600
minimum	minimum	disabled	—	4.00 (min)	—
disabled	minimum	minimum	1.54 (min)	—	—

In addition:

a) The quantities Δv_2 and Δv_5 shall not exceed 40 mV peak-to-peak.

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b) The positive and negative voltages shall match such that each of the quantities min($|v_1 + v_4|/v_1$, $|v_1 + v_4|/|v_4|$), min($|v_2 + v_5|/v_2$, $|v_2 + v_5|/|v_5|$), and min($|v_3 + v_6|/v_3$, $|v_3 + v_6|/|v_6|$) does not exceed 0.05.
c) The quantity v_2 shall be greater than or equal to 40 mV.
d) Any coefficient update equal to decrement applied to any tap that would result in v_2 less than 40 mV shall return a coefficient status value minimum.
e) Any coefficient update equal to decrement that would result in a violation of 72.7.1.4 shall return a coefficient status value minimum for that coefficient.
f) Any coefficient update equal to increment that would result in a violation of 72.7.1.4 shall return a coefficient status value maximum for that coefficient.

72.7.2 Receiver characteristics

Receiver characteristics at TP4 are summarized in Table 72–9 and detailed in 72.7.2.1 through 72.7.2.5.

Table 72–9—Receiver characteristics for 10GBASE-KR

Parameter	Subclause reference	Value	Units
Bit error ratio	72.7.2.1	10^{-12}	
Signaling speed	72.7.2.2	10.3125 ± 100 ppm	GBd
Receiver coupling	72.7.2.3	AC	
Differential input peak-to-peak amplitude (maximum)	72.7.2.4	1200[a]	mV
Differential input return loss (minimum)[b]	72.7.2.5	[See Equation (72–4) and Equation (72–5)]	dB

[a]The receiver shall tolerate amplitudes up to 1600 mV without permanent damage.
[b]Relative to 100 Ω differential.

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72.7.2.1 Receiver interference tolerance

The receiver interference tolerance shall consist of two separate tests as described in Annex 69A with the parameters specified in Table 72–10. The data pattern for the interference tolerance test shall be the test patterns 2 or 3 as defined in 52.9.1.1. The receiver shall satisfy the requirements for interference tolerance specified in Annex 69A for both tests.

Table 72–10—10GBASE-KR interference tolerance parameters

Parameter	Test 1 values	Test 2 values	Units
Target BER	10^{-12}	10^{-12}	
m_{TC} (min.)[a]	1.0	0.5	
Amplitude of broadband noise (min. RMS)	5.2	12	mV
Applied transition time (20%–80%, min.)	47	47	ps
Applied Sinusoidal jitter (min. peak-to-peak)	0.115	0.115	UI
Applied random jitter (min. peak-to-peak)[b]	0.130	0.130	UI
Applied Duty Cycle Distortion (min. peak-to-peak)	0.035	0.035	UI

[a]m_{TC} is defined in Equation (69A–6) of Annex 69A.
[b]Applied random jitter is specified at a BER of 10^{-12}.

72.7.2.2 Signaling speed range

A 10GBASE-KR receiver shall comply with the requirements of Table 72–9 for any signaling speed in the range 10.3125 GBd ± 100 ppm.

72.7.2.3 AC-coupling

The 10GBASE-KR receiver shall be AC-coupled to the backplane to allow for maximum interoperability between various 10 Gb/s components. AC-coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC-coupling in actual implementations.

NOTE—It is recommended that the maximum value of the coupling capacitors be limited to 100 nF. This will limit the inrush currents to the receiver that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

72.7.2.4 Input signal amplitude

10GBASE-KR receivers shall accept differential input signal peak-to-peak amplitudes produced by compliant transmitters connected without attenuation to the receiver, and still meet the BER requirement specified in 72.7.2.1. Note that this may be larger than the 1200 mV differential maximum of 72.7.1.4 due to the actual transmitter output and receiver input impedances. The input impedance of a receiver can cause the minimum signal into a receiver to differ from that measured when the receiver is replaced with a 100 Ω test load. Since the channel is AC-coupled, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

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72.7.2.5 Differential input return loss

For frequencies from 100 MHz to 7500 MHz, the differential return loss, in dB with *f* in MHz, of the receiver shall be greater than or equal to Equation (72–4) and Equation (72–5). The reference impedance for differential return loss measurements is 100 Ω.

72.8 Interconnect characteristics

Informative interconnect characteristics for 10GBASE-KR are provided in Annex 69B.

72.9 Environmental specifications

72.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

72.9.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

72.9.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

72.9.4 Electromagnetic compatibility

A system integrating the 10GBASE-KR PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

72.9.5 Temperature and humidity

A system integrating the 10GBASE-KR PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

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72.10 Protocol implementation conformance statement (PICS) proforma for Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KR[135]

72.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3, Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium type 10GBASE-KR, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

72.10.2 Identification

72.10.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

72.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium type 10GBASE-KR
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[135] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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72.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XGE	XGMII	72.1, 46	Interface is supported	O	Yes [ ] No [ ]
XGXS	XGXS and XAUI	72.1, 47		O	Yes [ ] No [ ]
PCS	Support of 10GBASE-R PCS	72.1, 49		M	Yes [ ]
PMA	Support of 10 Gigabit serial PMA	72.1, 51		M	Yes [ ]
AN	Auto-Negotiation for Backplane Ethernet	72.1, 73	Device implements Auto-Negotiation for Backplane Ethernet	M	Yes [ ]
FEC	Forward error correction	72.1, 74	Device implements 10GBASE-R forward error correction	O	Yes [ ] No [ ]
DC	Delay Constraints	72.4	Device conforms to delay constraints	M	Yes [ ]
LPI	LPI	72.6.11	LPI	O	Yes [ ] No [ ]
*MD	MDIO interface	72.5	Device implements MDIO	O	Yes [ ] No [ ]
*TD	Global_PMD_transmit_disable	72.6.5		O	Yes [ ] No [ ]

72.10.4 PICS proforma tables for Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KR

72.10.4.1 PCS requirements for AN service interface

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	AN service interface primitive	72.3	The PCS associated with this PMD supports the AN service interface primitive AN_LINK.indication defined in 73.9	M	Yes [ ]

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72.10.4.2 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Transmit function	72.6.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FS2	Transmitter signal	72.6.2	A positive differential voltage corresponds to tx_bit = ONE	M	Yes [ ]
FS3	Receive function	72.6.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FS4	Receiver signal	72.6.3	A positive differential voltage corresponds to rx_bit = ONE	M	Yes [ ]
FS5	Signal detect	72.6.4	Report to PMD service interface	M	Yes [ ]
FS6	Global signal detect	72.6.4	Value described in 45.2.1.9.7	M	Yes [ ]
FS7	SIGNAL_DETECT value	72.6.4	Set to FAIL	M	Yes [ ]
FS8	SIGNAL_DETECT value	72.6.4	Set to OK when traning is complete	M	Yes [ ]
FS9	SIGNAL_DETECT value	72.6.4	Set to OK when training disabled	M	Yes [ ]
FS10	Signal detect during LPI	72.6.4	Detect signal energy during LPI	LPI:M	Yes [ ] N/A[ ]
FS11	Signal detect for EEE	72.6.4	Transition timing to set SIGNAL_DETECT	LPI:M	Yes [ ] N/A [ ]
FS12	Transmit disable requirements	72.6.5	Requirements of 72.6.5 and Table 72–6	TD:M	Yes [ ] N/A[ ]
FS13	Transmit disable during LPI	72.6.5	Disable transmitter during tx_mode = QUIET	LPI:M	Yes [ ] N/A[ ]
FS14	Loopback support	72.6.6	Provided for 10GBASE-KR PMD by transmitter and receiver	M	Yes [ ]

72.10.4.3 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	MDIO Variable Mapping	72.5	Per Table 72–2 and Table 72–3	MD:M	Yes [ ] N/A [ ]
MF2	PMD_transmit_fault function	72.6.8	Sets PMD_transmit_fault as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
MF3	PMD_receive_fault function	72.6.9	Sets PMD_receive_fault as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]

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72.10.4.4 PMD Control functions

Item	Feature	Subclause	Value/Comment	Status	Support
CF1	Control Channel Encoding	72.6.10.2.2	Control channel transmitted using differential Manchester encoding (DME)	M	Yes [ ]
CF2	Differential Manchester Encoding rules	72.6.10.2.2	Transitions at cell boundary.	M	Yes [ ]
CF3	Differential Manchester Encoding rules	72.6.10.2.2	Presence of a mid-cell transition to signal logic 1	M	Yes [ ]
CF4	Differential Manchester Encoding rules	72.6.10.2.2	Absence of a mid-cell transition to signal logic 0	M	Yes [ ]
CF5	Coding violation	72.6.10.2.2	Ignore contents of control channel if coding violation found	M	Yes [ ]
CF6	Coefficient update field format	72.6.10.2.3	Format of the coefficient update field per Table 72–4	M	Yes [ ]
CF7	Cell 15 of the coefficient update field	72.6.10.2.3	Transmitted first	M	Yes [ ]
CF8	Preset control	72.6.10.2.3.1	When received, pre-cursor and post-cursor coefficients set to zero	M	Yes [ ]
CF9	Preset control	72.6.10.2.3.1	When received, main coefficient set to maximum value	M	Yes [ ]
CF10	Preset control initially sent	72.6.10.2.3.1	Only when all coefficient status fields indicate not_updated and continues until all coefficients indicate updated or maximum	M	Yes [ ]
CF11	Outgoing initialize control	72.6.10.2.3.1	Set to zero when all coefficients indicate updated or maximum following preset	M	Yes [ ]
CF12	Maximum status	72.6.10.2.3.1	Returned when the main coefficient is updated	M	Yes [ ]
CF13	Maximum status	72.6.10.2.3.1	Returned for pre-cursor and/or post-cursor coefficients when coefficient updated and zero is its maximum value	M	Yes [ ]
CF14	Updated status	72.6.10.2.3.1	Returned for pre-cursor and/or post-cursor coefficients when the coefficient is updated and it supports additional settings above the value zero	M	Yes [ ]
CF15	New Preset or Initialize requests	72.6.10.2.3.1	Not sent until the incoming status for all coefficients revert to not_updated	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
CF16	Preset	72.6.10.2.3.1	Not sent in combination with initialize or coefficient increment/decrement requests	M	Yes [ ]
CF17	Initalize control	72.6.10.2.3.2	When received, taps set to meet conditions of 72.6.10.4.2	M	Yes [ ]
CF18	Initalize control initially sent	72.6.10.2.3.2	Only when all coefficient status fields indicate not_updated and continues until all coefficients indicate updated	M	Yes [ ]
CF19	Updated status	72.6.10.2.3.2	Returned for each coefficient when the coefficient update is complete	M	Yes [ ]
CF20	Outgoing initalize field	72.6.10.2.3.2	Set to zero when all coefficients indicate update complete following initialize	M	Yes [ ]
CF21	New Preset or Initialize requests	72.6.10.2.3.2	Not sent until the incoming status for all coefficients revert to not_updated	M	Yes [ ]
CF22	Initialize	72.6.10.2.3.2	Not sent in combination with coefficient increment/decrement requests	M	Yes [ ]
CF23	Increment or decrement encodings transmitted	72.6.10.2.3.3	Transmitted until status indicates: updated, maximum, or minimum	M	Yes [ ]
CF24	Outgoing requests	72.6.10.2.3.3	Set to hold once update status for tap indicates updated, maximum or minimum	M	Yes [ ]
CF25	Increment or decrement request	72.6.10.2.3.3	Not sent before status reverts to not_updated	M	Yes [ ]
CF26	Encoding of coefficient update	72.6.10.2.3.3	Per Table 72–4	M	Yes [ ]
CF27	Format of status report field	72.6.10.2.4	Per Table 72–5	M	
CF28	Cell 15 of the status report field	72.6.10.2.4	Transmitted first	M	
CF29	Receiver ready indication	72.6.10.2.4.4	Per Table 72–5	M	Yes [ ]
CF30	Coefficient status	72.6.10.2.4.5	Per Table 72–5	M	Yes [ ]
CF31	Training pattern length	72.6.10.2.6	512 octets	M	Yes [ ]
CF32	Training pattern generator	72.6.10.2.6	Per Figure 72–3	M	Yes [ ]
CF33	Training pattern seed	72.6.10.2.6	The pseudo-random generator shall have a random seed at the start of the training pattern	M	Yes [ ]
CF34	Remote_rx_ready	72.6.10.3.1	TRUE after three or more consecutive training frames received with receiver ready indicated	M	Yes [ ]
CF35	Wait Timer	72.6.10.3.2	100 to 300 training frames	M	Yes [ ]
CF36	Max Wait Timer	72.6.10.3.2	500 ms ± 1%	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
CF37	Slip function to find framesync	72.6.10.3.2	Evaluates all possible positions	M	Yes [ ]
CF38	Frame Lock state diagram	72.6.10.4.1	Meets requirements of Figure 72–4	M	Yes [ ]
CF39	Training state diagram	72.6.10.4.2	Meets requirements of Figure 72–5	M	Yes [ ]
CF40	Entry to INITIALIZE state	72.6.10.4.2	Transmitter equalizer configured per 72.6.10.4.2	M	Yes [ ]
CF41	Initial value of c(0) at the start of training	72.6.10.4.2	Meets the requirements of 72.6.10.4.2	M	Yes [ ]
CF42	Coefficient Update state diagram	72.6.10.4.3	Meets requirements of Figure 72–6	M	Yes [ ]

72.10.4.5 Transmitter electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Test fixture impedance	72.7.1.2	100 Ω	M	Yes [ ]
TC2	Differential return loss of test fixture	72.7.1.2	Per Equation (72–2) and Equation (72–3)	M	Yes [ ]
TC3	Signaling speed	72.7.1.3	10.3125 GBd ± 100 ppm	M	Yes [ ]
TC4	Maximum transmitter differential peak-to-peak voltage	72.7.1.4	Less than 1200 mV for a 1010 pattern	M	Yes [ ]
TC5	Maximum transmitter differential peak-to-peak voltage when TX disabled	72.7.1.4	Less than 30 mV	M	Yes [ ]
TC6	Common-mode output voltage	72.7.1.4	Between 0 and 1.9 V	M	Yes [ ]
TC7	Output Amplitude LPI voltage	72.7.1.4	Less than 30 mV within 500 ns of tx_quiet	LPI:M	Yes [ ] N/A [ ]
TC8	Output Amplitude ON voltage	72.7.1.4	Greater than 90% of previous level within 500 ns of tx_quiet de-asserted	LPI:M	Yes [ ] N/A [ ]
TC9	Differential output return loss	72.7.1.5	Per Equation (72–4) and Equation (72–5)	M	Yes [ ]
TC10	Differential output reference impedance	72.7.1.5	100 Ω	M	Yes [ ]
TC11	Common-mode output return loss	72.7.1.6	Per Equation (72–6) and Equation (72–7)	M	Yes [ ]
TC12	Rising edge transition time	72.7.1.7	Between 24 ps and 47 ps as measured at the 20% and 80% levels referenced to v_2 and v_5 as defined in 72.7.1.11 with no equalization	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC13	Falling edge transition time	72.7.1.7	Between 24 ps and 47 ps as measured at the 20% and 80% levels referenced to v_2 and v_5 as defined in 72.7.1.11 with no equalization	M	Yes [ ]
TC14	Transmit jitter, peak-to-peak	72.7.1.9	See 72.7.1.8. Max TJ of 0.28 UI. Max DJ of 0.15 UI. Max RJ of 0.15 UI	M	Yes [ ]
TC15	Duty Cycle Distortion	72.7.1.9	Not to exceed 0.035 UI	M	Yes [ ]
TC16	Jitter test patterns	72.7.1.8	Test patterns 2 or 3 as defined in 52.9.1.1	M	Yes [ ]
TC17	During jitter testing	72.7.1.8	Equalization turned off	M	Yes [ ]
TC18	Changes in transmit output waveform resulting from coefficient updates	72.7.1.10	Meet requirements of Table 72–7	M	Yes [ ]
TC19	Verification of coefficient updates	72.7.1.10	After the coefficient status for all taps is reported as not_updated	M	Yes [ ]
TC20	Transmit output waveform	72.7.1.10	Meet requirements of Table 72–8	M	Yes [ ]
TC21	v_2	72.7.1.10	Greater than or equal to 40 mV for all transmit equalizer configurations	M	Yes [ ]
TC22	Coefficient status value minimum	72.7.1.10	Returned for any coefficient update equal to decrement applied to any tap that would result in Δv_2 or Δv_5 less than 40 mV	M	Yes [ ]
TC23	Coefficient status value maximum	72.7.1.10	Returned for any coefficient update equal to decrement applied to c(-1) or c(1) that would result in a violation of 72.7.1.4	M	Yes [ ]
TC24	Coefficient status value maximum	72.7.1.10	Returned for any coefficient update equal to increment applied to c(0) that would result in a violation of 72.7.1.4	M	Yes [ ]
TC25	Transmitter output waveform	72.7.1.11	Verified with test patterns 2 or 3 as defined in 52.9.1.1	M	Yes [ ]
TC26	v_1, v_2, Δv_2, v_3, v_4, v_5, Δv_5, v_6	72.7.1.11, 72.7.1.10	Measured per Figure 72–12. The absolute value of v_6 and v_3 are within 5%. The absolute value of v_1 and v_4 are within 5% and the absolute value of v_2 and v_5 are within 5%. The maximum peak-to-peak value of Δv_2 and Δv_5 shall not exceed 40 mV	M	Yes [ ]

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72.10.4.6 Receiver electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Receiver amplitude tolerance	72.7.2	Amplitudes up to 1600 mV without permanent damage	M	Yes [ ]
RC2	Receiver interference tolerance	72.7.2.1	Measured as described in Annex 69A with parameters in Table 72–10	M	Yes [ ]
RC3	Receiver interference tolerance	72.7.2.1	Receiver interference tolerance test pattern per 72.7.2.1	M	Yes [ ]
RC4	Receiver interference tolerance	72.7.2.1	Satisfy the requirements specified in Annex 69A	M	Yes [ ]
RC5	Signaling speed	72.7.2.2	10.3125 GBd ±100 ppm	M	Yes [ ]
RC6	Receiver coupling	72.7.2.3	AC-coupled	M	Yes [ ]
RC7	Input signal amplitude	72.7.2.4	BER still met when compliant transmitter is connected with no attenuation	M	Yes [ ]
RC8	Differential return loss	72.7.2.5	Per Equation (72–4) and Equation (72–5)	M	Yes [ ]

72.10.4.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	72.9.1	Conforms to J.2	M	Yes [ ]
ES2	Electromagnetic interference	72.9.4	Complies with applicable local and national codes	M	Yes [ ]

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73. Auto-Negotiation for backplane and copper cable assembly

Auto-Negotiation, as defined in this clause, is specified for use with Ethernet PHYs operating over a backplane and for use with certain Ethernet PHYs operating over a copper cable assembly.

73.1 Auto-Negotiation introduction

While implementation of Auto-Negotiation is mandatory for Backplane Ethernet PHYs, the use of Auto-Negotiation is optional. Parallel detection shall be provided for legacy devices that do not support Auto-Negotiation.

The Auto-Negotiation function allows an Ethernet device to advertise modes of operation it possesses to another device at the remote end of a Backplane Ethernet link and to detect corresponding operational modes the other device may be advertising.

The objective of this Auto-Negotiation function is to provide the means to exchange information between two devices that share a link across a backplane and to automatically configure both devices to take maximum advantage of their abilities. It has the additional objective of supporting a digital signal detect to ensure that the device is attached to a link partner rather than detecting signal due to crosstalk.

Auto-Negotiation is performed using differential Manchester encoding (DME) pages. DME provides a DC-balanced signal. DME does not add packet or upper layer overhead to the network devices.

Auto-Negotiation does not test the link segment characteristics.

This function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and discover the common modes of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The Auto-Negotiation function allows the devices to switch between the various operational modes in an orderly fashion, permits management to disable or enable the Auto-Negotiation function, and allows management to select a specific operational mode. The Auto-Negotiation function also provides a parallel detection function to allow Backplane Ethernet devices to connect to other Backplane Ethernet devices that have Auto-Negotiation disabled and interoperate with legacy devices that do not support Clause 73 Auto-Negotiation.

It is recommended that a device that has negotiated 1000BASE-KX operation through this clause not perform Clause 37 Auto-Negotiation. A device that performs Clause 37 Auto-Negotiation after having negotiated 1000BASE-KX operation through Clause 73 Auto-Negotiation will not interoperate with a device that does not perform Clause 37 Auto-Negotiation. Therefore, a device that intends to enable Clause 37 Auto-Negotiation after Clause 73 Auto-Negotiation has completed shall ensure through an implementation-specific mechanism that the link partner supports Clause 37 Auto-Negotiation and intends to enable it. If Clause 37 Auto-Negotiation is performed after Clause 73 Auto-Negotiation, then the advertised abilities used in the Clause 37 Auto-Negotiation shall match those advertised abilities used in the Clause 73 Auto-Negotiation.

The Auto-Negotiation functions are listed in 73.3.

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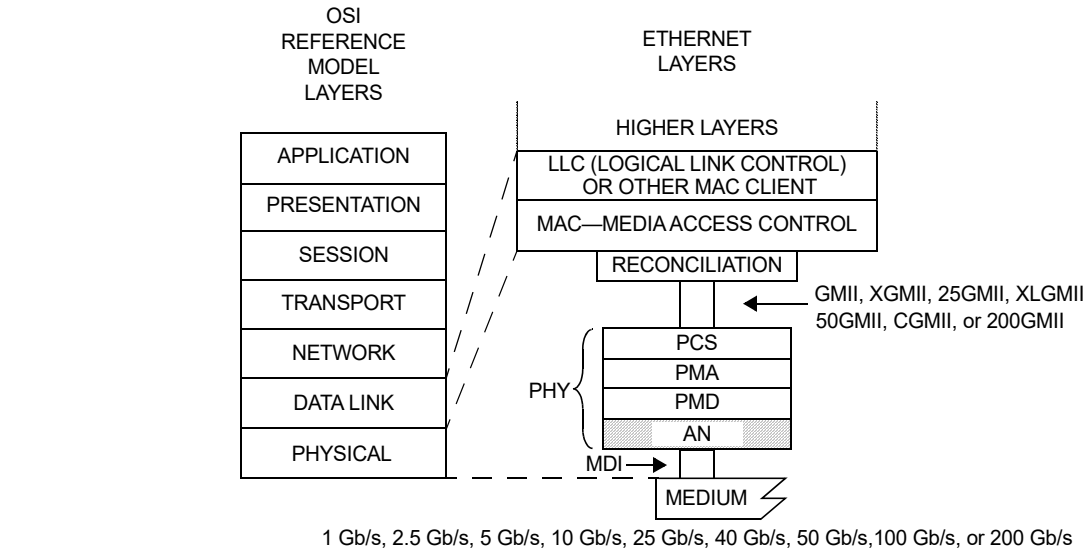
73.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

The Auto-Negotiation function is provided at the Physical Layer of the ISO/IEC OSI reference model as shown in Figure 73–1. A device that supports multiple modes of operation may advertise its capabilities using the Auto-Negotiation function. The actual transfer of information is observed only at the MDI or on the backplane medium.



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 73–1—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

73.3 Functional specifications

The Auto-Negotiation function provides a mechanism to control connection of a single MDI to a single PHY type, where more than one PHY type may exist. A management interface provides control and status of Auto-Negotiation, but the presence of a management agent is not required.

The Auto-Negotiation function shall provide the following:

a) Auto-Negotiation transmit
b) Auto-Negotiation receive
c) Auto-Negotiation arbitration

These functions shall comply with the state diagrams from Figure 73–9 through Figure 73–11. The Auto-Negotiation functions shall interact with the technology-dependent PHYs through the

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Technology-Dependent interface (see 73.9). Technology-Dependent PHYs are those supported by the Auto-Negotiation process (see Table 73–4).

When the MDI supports multiple lanes, then lane 0 of the MDI shall be used for Auto-Negotiation and for connection of any single-lane PHYs (e.g., 1000BASE-KX or 10GBASE-KR).

73.4 Transmit function requirements

The Transmit function provides the ability to transmit pages. The first pages exchanged by the local device and its link partner after Power-On, link restart, or renegotiation contain the base link codeword defined in Figure 73–6. The local device may modify the link codeword to disable an ability it possesses, but will not transmit an ability it does not possess. This makes possible the distinction between local abilities and advertised abilities so that multi-ability devices may Auto-Negotiate to a mode lower in priority than the highest common ability.

73.5 DME transmission

Auto-Negotiation's method of communication builds upon the encoding mechanism known as differential Manchester encoding (DME). The DME page encodes the data that is used to control the Auto-Negotiation function. DME pages shall not be transmitted when Auto-Negotiation is complete and the highest common denominator PHY has been enabled.

73.5.1 DME electrical specifications

Transmitter characteristics shall meet the specifications in Table 73–1 at TP1 while transmitting DME pages. Receiver characteristics shall meet the specifications in Table 73–1 at TP4 while receiving DME pages.

Table 73–1—DME electrical characteristics

Parameter	Value	Units
Transmit differential peak-to-peak output voltage	600 to 1200	mV
Receive differential peak-to-peak input voltage	200 to 1200	mV

For any multi-lane PHY, DME pages shall be transmitted only on lane 0. The transmitters on other lanes should be disabled as specified in 71.6.7, 84.7.7, 85.7.7, 92.7.7, 93.7.7, 94.3.6.7, 136.8.7, or 137.8.7.

73.5.2 DME page encoding

A DME page carries a 48-bit Auto-Negotiation page. It consists of 106 evenly spaced transition positions that contain a Manchester violation delimiter, the 48-bit page, and a single pseudo-random bit. The odd-numbered transition positions represent clock information. The even numbered transition positions represent data information. DME pages are transmitted continuously without any idle or gap.

The first eight transition positions contain the Manchester violation delimiter, which marks the beginning of the page. The Manchester violation contains a transition at position 1 and position 5 and no transitions at the remaining positions. The Manchester violation delimiter is the only place where four intervals occur between transitions. This allows the receiver to obtain page synchronization.

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Each of the remaining 49 odd-numbered transition positions shall contain a transition. The remaining 49 even-numbered transition positions shall represent data information as follows:

— A transition present in an even-numbered transition position represents a logical one
— A transition absent from an even-numbered transition position represents a logical zero

The first 48 of these positions shall carry the data of the Auto-Negotiation page. The final position carries the pseudo-random bit. The value of the pseudo-random bit shall be derived from a pseudo-random generator as shown in Figure 73–2.

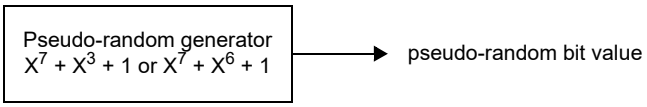

Figure 73–2—DME page bit 49 randomizer

The counter shall increment once per DME page.

The purpose of the 49th bit is to remove the spectral peaks that would otherwise occur when sending the same AN page repeatedly. Randomly choosing between 0 or 1 for one of the DME bits results in randomly inverting or not inverting the encoded page so that repetitions of the same page no longer produce a periodic signal.

Clock transition positions are differentiated from data transition positions by the spacing between them, as shown in Figure 73–3 and enumerated in Table 73–2.

The encoding of data using DME bits in an DME page is illustrated in Figure 73–3.

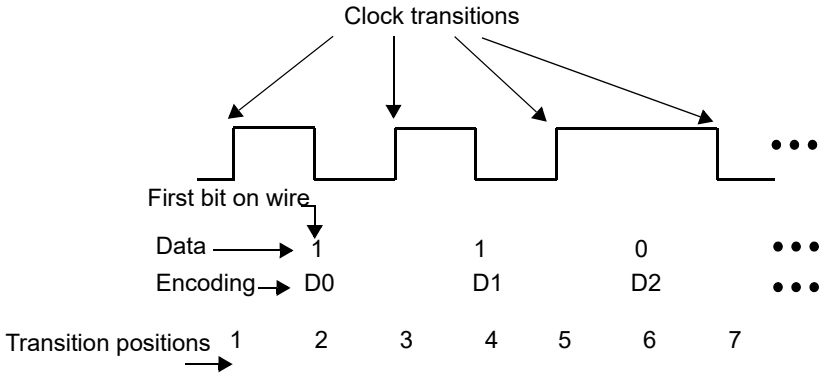

Figure 73–3—Data bit encoding within DME pages

73.5.3 DME page timing

The timing parameters for DME pages shall be followed as in Table 73–2. The transition positions within a DME page are spaced with a period of T1. T2 is the separation between clock transitions. T3 is the time from a clock transition to a data transition representing a one. The period, T1, shall be 3.2 ns ± 0.01%. Transitions shall occur within ± 0.2 ns of their ideal positions.

T5 specifies the duration of a DME page. Since DME pages are sent continuously during Auto-Negotiation, T5 is also the time from the start of one DME page to the start of the next DME page.

The minimum number of transitions and maximum number of transitions in a page is represented by T4.

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Table 73–2 summarizes the timing parameters. The transition timing parameters are illustrated in Figure 73–4.

Table 73–2— DME page timing summary

	Parameter	Min.	Typ.	Max.	Units
T1	Transition position spacing (period)	3.2 –0.01%	3.2	3.2 +0.01%	ns
T2	Clock transition to clock transition	6.2	6.4	6.6	ns
T3	Clock transition to data transition (data = 1)	3.0	3.2	3.4	ns
T4	Transitions in a DME page	51	—	100	—
T5	DME page width	338.8	339.2	339.6	ns
T6	DME Manchester violation delimiter width	12.6	12.8	13.0	ns

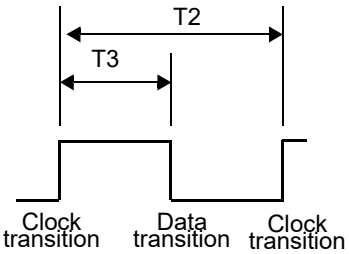

Figure 73–4—DME page transition timing

73.5.3.1 Manchester violation delimiter

A violation is signaled as shown in Figure 73–5.

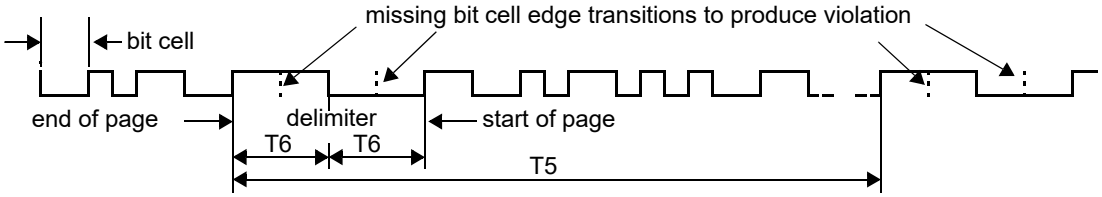

Figure 73–5—Manchester violation

73.6 Link codeword encoding

The base link codeword (Base Page) transmitted within a DME page shall convey the encoding shown in Figure 73–6. The Auto-Negotiation function supports additional pages using the Next Page function. Encoding for the link codeword(s) used in the Next Page exchange are defined in 73.7.7. In a DME page, D0 shall be the first bit transmitted.

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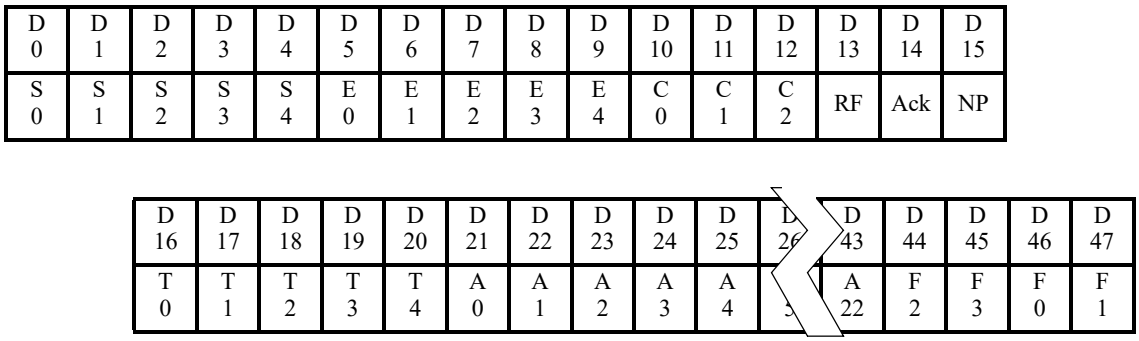

Figure 73–6—Link codeword Base Page

D[4:0] contains the Selector Field. D[9:5] contains the Echoed Nonce field. D[12:10] contains capability bits to advertise capabilities not related to the PHY. C[1:0] is used to advertise pause capability. The remaining capability bit C[2] is reserved. D[15:13] contains the RF, Ack, and NP bits. These bits shall function as specified in 28.2.1.2. D[20:16] contains the Transmitted Nonce field. D[43:21] contains the Technology Ability Field. D[47:44] contains FEC capability (see 73.6.5).

73.6.1 Selector Field

Selector Field (S[4:0]) is a five-bit wide field, encoding 32 possible messages. Selector Field encoding definitions are shown in Annex 28A. Combinations not specified are reserved for future use. Reserved combinations of the Selector Field shall not be transmitted.

The Selector Field for IEEE Std 802.3 is shown in Table 73–3.

Table 73–3—Selector Field Encoding

S4	S3	S2	S1	S0	Selector description
0	0	0	0	1	IEEE Std 802.3

73.6.2 Echoed Nonce Field

Echoed Nonce Field (E[4:0]) is a 5-bit wide field containing the nonce received from the link partner. When Acknowledge is set to logical zero, the bits in this field shall contain logical zeros. When Acknowledge is set to logical one, the bits in this field shall contain the value received in the Transmitted Nonce Field from the link partner.

73.6.3 Transmitted Nonce Field

Transmitted Nonce Field (T[4:0]) is a 5-bit wide field containing a random or pseudo-random number. A new value shall be generated for each entry to the Ability Detect state. The method of generating the nonce is left to the implementer. The transmitted nonce should have a uniform distribution in the range from 0 to $2^5 - 1$. The method used to generate the value should be designed to minimize correlation to the values generated by other devices.

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73.6.4 Technology Ability Field

Technology Ability Field (A[22:0]) is a 23-bit wide field containing information indicating supported technologies specific to the selector field value when used with the Auto-Negotiation for backplane and copper cable assembly. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. The Technology Ability Field encoding for the IEEE 802.3 selector with Auto-Negotiation for backplane and copper cable assembly is described in Table 73–4.

Table 73–4—Technology Ability Field encoding

Bit	Technology
A0	1000BASE-KX
A1	10GBASE-KX4
A2	10GBASE-KR
A3	40GBASE-KR4
A4	40GBASE-CR4
A5	100GBASE-CR10
A6	100GBASE-KP4
A7	100GBASE-KR4
A8	100GBASE-CR4
A9	25GBASE-KR-S or 25GBASE-CR-S
A10	25GBASE-KR or 25GBASE-CR
A11	2.5GBASE-KX
A12	5GBASE-KR
A13	50GBASE-KR or 50GBASE-CR
A14	100GBASE-KR2 or 100GBASE-CR2
A15	200GBASE-KR4 or 200GBASE-CR4
A16 through A22	Reserved

Multiple technologies may be advertised in the link codeword. A device shall support the data service ability for a technology it advertises. It is the responsibility of the Arbitration function to determine the common mode of operation shared by a link partner and to resolve multiple common modes.

NOTE—Previous editions of this standard prohibited simultaneous advertisement of PHYs that support operation over electrical backplanes with PHYs that support operation over copper cable assemblies.

25GBASE-KR-S abilities are a subset of 25GBASE-KR abilities, and likewise 25GBASE-CR-S abilities are a subset of 25GBASE-CR abilities. To allow interoperation between 25GBASE-KR-S and 25GBASE-KR PHY types, and between 25GBASE-CR-S and 25GBASE-CR PHY types, a device that supports 25GBASE-KR or 25GBASE-CR should advertise both A9 and A10 ability bits during auto-negotiation.

The fields A[22:16] are reserved for future use. Reserved fields shall be sent as zero and ignored on receive.

73.6.5 FEC capability

FEC (F2, F3, F0, F1) is encoded in bits D44:D47 of the base link codeword. The four FEC bits are used as follows:

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a) F0 is 10 Gb/s per lane FEC ability
b) F1 is 10 Gb/s per lane FEC requested
c) F2 is 25G RS-FEC requested
d) F3 is 25G BASE-R FEC requested

Bits F2 and F3 are used for resolving FEC operation for 25G PHYs, while bits F0 and F1 are used for 10 Gb/s per lane operation. Bits F0 and F1 are not used for 25G PHYs.

73.6.5.1 FEC resolution for 25G PHYs

For 25G PHYs if neither PHY requests FEC operation in bits F2 or F3 then FEC is not enabled.

For 25GBASE-KR and 25GBASE-CR PHYs if either PHY requests RS-FEC then RS-FEC operation is enabled, otherwise if either PHY requests BASE-R FEC then BASE-R operation is enabled.

For 25GBASE-KR-S and 25GBASE-CR-S PHYs, if either PHY requests RS-FEC or BASE-R FEC then BASE-R operation is enabled. This is because 25GBASE-KR-S and 25GBASE-CR-S PHYs do not support RS-FEC operation.

73.6.5.2 FEC resolution for 10 Gb/s per lane PHYs

For 10 Gb/s per lane operation, when the FEC ability bit F0 is set to logical one, it indicates that the PHY has FEC ability (see Clause 74). When the FEC requested F1 bit is set to logical one, it indicates a request to enable FEC on the link.

Since the local device and the link partner may have set the FEC capability bits differently, the priority resolution function is used to enable FEC in the respective PHYs. The FEC function shall be enabled on the link if 10GBASE-KR, 40GBASE-KR4, 40GBASE-CR4, or 100GBASE-CR10 is the HCD technology (see 73.7.6), both devices advertise FEC ability on the F0 bits, and at least one device requests FEC on the F1 bits; otherwise FEC shall not be enabled.

73.6.5.3 FEC control variables

The variable an_baser_fec_control indicates that BASE-R FEC operation has been negotiated. If the value is false, then BASE-R FEC has not been negotiated. If the value is true, then BASE-R FEC has been negotiated.

The variable an_rs_fec_control indicates that RS-FEC operation has been negotiated. If the value is false, then RS-FEC has not been negotiated. If the value is true, then RS-FEC has been negotiated.

The mapping of these variables to MDIO register bits is defined in Table 73–6.

If mr_autoneg_enable (see 73.10.1) is false, the FEC function is controlled by implementation-dependent means.

73.6.6 Pause Ability

Pause (C0:C1) is encoded in bits D11:D10 of the base link codeword. The two-bit Pause is encoded as follows:

a) C0 is the same as PAUSE as defined in Annex 28B
b) C1 is the same as ASM_DIR as defined in Annex 28B

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The Pause encoding is defined in Clause 28B.2, Table 28B–2. The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. The ASM_DIR bit indicates that asymmetric PAUSE is supported. The value of the PAUSE bit when the ASM_DIR bit is set indicates the direction the PAUSE frames are supported for flow across the link. Asymmetric PAUSE configuration results in independent enabling of the PAUSE receive and PAUSE transmit functions as defined by Annex 31B. See 28B.3 regarding PAUSE configuration resolution.

73.6.7 Remote Fault

Remote Fault (RF) is encoded in bit D13 of the base link codeword. The default value is logical zero. The Remote Fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the AN advertisement register (register 7.16.13) is set to logical one, the RF bit in the transmitted base link codeword is set to logical one. When the RF bit in the received base link codeword is set to logical one, the Remote Fault bit in the AN LP Base Page ability register (register 7.19.13) will be set to logical one, if the management function is present.

73.6.8 Acknowledge

Acknowledge (Ack) is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's link codeword. The Acknowledge Bit is encoded in bit D14 of link codeword. If no Next Page information is to be sent, this bit shall be set to logical one in the link codeword after the reception of at least three consecutive and consistent DME pages (ignoring the Acknowledge bit value). If Next Page information is to be sent, this bit shall be set to logical one after the device has successfully received at least three consecutive and matching DME pages (ignoring the Acknowledge bit value), and will remain set until the Next Page information has been loaded into the AN XNP transmit register (registers 7.22, 7.23, 7.24). In order to save the current received link codeword, it has to be read from the AN LP XNP ability register (register 7.25, 7.26, 7.27) before the Next Page of transmit information is loaded into the AN XNP transmit register. After the COMPLETE ACKNOWLEDGE state has been entered, the link codeword will be transmitted at least six times.

73.6.9 Next Page

Next Page (NP) is encoded in bit D15 of link codeword. Support of Next Pages is mandatory. If the device does not have any Next Pages to send, the NP bit shall be set to logical zero. If a device wishes to engage in Next Page exchange, it shall set the NP bit to logical one. If a device has no Next Pages to send and its link partner has set the NP bit to logical one, it shall transmit Next Pages with Null message codes and the NP bit set to logical zero while its link partner transmits valid Next Pages. Next page exchanges will occur if either the device or its link partner sets the Next Page bit to logical one. The Next Page function is defined in 73.7.7.

73.6.10 Transmit Switch function

During Auto-Negotiation and prior to entry into the AN_GOOD_CHECK state, the Transmit Switch function shall connect only the DME page generator controlled by the Transmit State Diagram to the MDI.

Upon entry into the AN_GOOD_CHECK state, the Transmit Switch function shall connect the transmit path from a single technology-dependent (highest common denominator) PHY to the MDI.

When a PHY is connected to the MDI through the Transmit Switch function, the signals at the MDI shall conform to all of the PHY's specifications within 20 ms.

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73.7 Receive function requirements

The receive function detects the DME page sequence, decodes the information contained within, and stores the data in rx_link_code_word[48:1]. The receive function incorporates a receive switch to control connection of the DME page receiver or a PHY to the MDI.

73.7.1 DME page reception

To be able to detect the DME bits, the receiver should have the capability to receive DME signals sent with the electrical specifications of the PHY. The DME transmit signal level and receive sensitivity are specified in 73.5.1.

73.7.2 Receive Switch function

During Auto-Negotiation and prior to entry into the AN_GOOD_CHECK state, the Receive Switch function shall connect the DME page receiver to the MDI. For the Parallel Detection function, the Receive Switch function shall also connect the receive path of the 1000BASE-KX and 10GBASE-KX4 PHY to the MDI when those PHYs are present.

Upon entry into the AN_GOOD_CHECK state, the Receive Switch function shall connect the receive path from a single technology-dependent (highest common denominator) PHY to the MDI.

73.7.3 Link codeword matching

The Receive function shall generate ability_match, acknowledge_match, and consistency_match variables as defined in Arbitration state diagram Figure 73–11.

73.7.4 Arbitration function requirements

The Arbitration function is described in Figure 73–11 and ensures proper sequencing of the Auto-Negotiation function using the Transmit function and Receive function. The Arbitration function enables the Transmit function to advertise and acknowledge abilities. Upon indication of acknowledgement, the Arbitration function determines the highest common denominator using the priority resolution function and enables the appropriate technology-dependent PHY via the link_control_[x] variables.

If mr_autoneg_enable (see 73.10.1) is false, enabling the desired technology-dependent PHY is controlled by implementation-dependent means.

73.7.4.1 Parallel Detection function

The local device detects a link partner that supports Auto-Negotiation by DME page detection. The Parallel Detection function allows detection of link partners that support 1000BASE-KX, 2.5GBASE-KX, and 10GBASE-KX4 but have disabled Auto-Negotiation, and detection of legacy devices that can interoperate with 1000BASE-KX, 2.5GBASE-KX, and 10GBASE-KX4 devices, but do not provide Clause 73 Auto-Negotiation.

A local device shall provide Parallel Detection for 1000BASE-KX, 2.5GBASE-KX, and 10GBASE-KX4 if it supports those PHYs. Additionally, parallel detection may be used for 10GBASE-CX4. Parallel detection of 10GBASE-CX4 will be indicated by the setting of the Negotiated Port Type to “10GBASE-KX4 or 10GBASE-CX4” in the management register bit 7.48.2. The means to distinguish between 10GBASE-KX4

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and 10GBASE-CX4 is implementation dependent. Parallel Detection shall be performed by directing the MDI receive activity to the PHY. This detection may be done in sequence between detection of DME pages and detection of each supported PHY. If at least one of the 1000BASE-KX, 2.5GBASE-KX, or 10GBASE-KX4 establishes link_status=OK, the LINK STATUS CHECK state is entered and the autoneg_wait_timer is started. If exactly one link_status=OK indication is present when the autoneg_wait_timer expires, then Auto-Negotiation shall set link_control=ENABLE for the PHY indicating link_status=OK. If a PHY is enabled, the Arbitration function shall set link_control=DISABLE to all other PHYs and indicate that Auto-Negotiation has completed. On transition to the AN GOOD CHECK state from the LINK STATUS CHECK state, the Parallel Detection function shall set the bit in the AN LP Base Page ability registers (see 45.2.7.7) corresponding to the technology detected by the Parallel Detection function.

If Auto-Negotiation detects link_status=OK from any of the technology-dependent PHYs prior to DME page detection, the autoneg_wait_timer shall start. If more than one technology-dependent PHYs indicate link_status=OK when the autoneg_wait_timer expires, Auto-Negotiation will not allow any data service to be enabled and may signal this as a remote fault to the link partner using the Base Page and will flag this in the local device by setting the Parallel Detection fault bit (45.2.7.2) in the AN Status register.

73.7.5 Renegotiation function

A renegotiation request from any entity, such as a management agent, shall cause the Arbitration function to disable all technology-dependent PHYs and halt any transmit data and link transition activity until the break_link_timer expires. Consequently, the link partner will go into link fail and normal Auto-Negotiation resumes. The local device shall resume Auto-Negotiation after the break_link_timer has expired by issuing DME pages with the Base Page valid in tx_link_code_word[48:1]. Once Auto-Negotiation has completed, renegotiation will take place if the Highest Common Denominator technology that receives link_control=ENABLE returns link_status=FAIL. To allow the PHY an opportunity to determine link integrity using its own link integrity test function, the link_fail_inhibit_timer qualifies the link_status=FAIL indication such that renegotiation takes place if the link_fail_inhibit_timer has expired and the PHY still indicates link_status=FAIL.

73.7.6 Priority Resolution function

Since a local device and a link partner may have multiple common abilities, a mechanism to resolve which mode to configure is required. The mechanism used by Auto-Negotiation is a Priority Resolution function that predefines the hierarchy of supported technologies. The single PHY enabled to connect to the MDI by Auto-Negotiation shall be the technology corresponding to the bit in the Technology Ability Field common

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to the local device and link partner that has the highest priority as defined in Table 73–5 (listed from highest priority to lowest priority).

Table 73–5—Priority Resolution

Priority	Technology	Capability
1	200GBASE-KR4 or 200GBASE-CR4	200 Gb/s 4 lane, highest priority
2	100GBASE-KR2 or 100GBASE-CR2	100 Gb/s 2 lane
3	100GBASE-CR4	100 Gb/s 4 lane
4	100GBASE-KR4	100 Gb/s 4 lane
5	100GBASE-KP4	100 Gb/s 4 lane
6	100GBASE-CR10	100 Gb/s 10 lane
7	50GBASE-KR or 50GBASE-CR	50 Gb/s 1 lane
8	40GBASE-CR4	40 Gb/s 4 lane
9	40GBASE-KR4	40 Gb/s 4 lane
10	25GBASE-KR or 25GBASE-CR	25 Gb/s 1 lane
11	25GBASE-KR-S or 25GBASE-CR-S	25 Gb/s 1 lane, short reach
12	10GBASE-KR	10 Gb/s 1 lane
13	10GBASE-KX4	10 Gb/s 4 lane
14	5GBASE-KR	5 Gb/s 1 lane
15	2.5GBASE-KX	2.5 Gb/s 1 lane
16	1000BASE-KX	1 Gb/s 1 lane, lowest priority

The common technology is referred to as the highest common denominator, or HCD, technology. If the local device receives a Technology Ability Field with a bit set that is reserved, the local device shall ignore that bit for priority resolution. Determination of the HCD technology occurs on entrance to the AN GOOD CHECK state. In the event that a technology is chosen through the parallel detection function, that technology shall be considered the highest common denominator (HCD) technology. In the event that there is no common technology, HCD shall have a value of “NULL”, indicating that no PHY receives link_control=ENABLE and link_status[HCD]=FAIL.

NOTE—If both local device and link partner are Backplane Ethernet compliant PHYs, then both ends use abilities exchanged through Clause 73 Auto-Negotiation function. If the Link partner is a legacy device (or has disabled Auto-Negotiation) as indicated by the parallel detect function, then the peer 1 Gb/s devices can opt to use abilities exchanged through Clause 37. This will ensure there are no interoperability issues when connected to a Backplane Ethernet PHY.

73.7.7 Next Page function

The Next Page function uses the Auto-Negotiation arbitration mechanisms to allow exchange of Next Pages of information, which may follow the transmission and acknowledgment procedures used for the base link codeword. The Next Page has both Message code field and Unformatted code fields.

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A dual acknowledgment system is used. Acknowledge (Ack) is used to acknowledge receipt of the information; Acknowledge 2 (Ack2) is used to indicate that the receiver is able to act on the information (or perform the task) defined in the message.

The Toggle bit is used to ensure proper synchronization between the local device and the link partner.

Next page exchange occurs after the base link codewords have been exchanged if either end of the link segment set the Next Page bit to logical one indicating that it had at least one Next Page to send. Next page exchange consists of using the normal Auto-Negotiation arbitration process to send Next Page messages.

The Next Page contains two message encodings. The message encodings are defined as follows: message code, which contain predefined 11-bit codes, and unformatted code contains 32 bit codes. Multiple Next Pages with appropriate message codes and unformatted codes can be transmitted to send extended messages. Each series of Next Pages shall have a Message code that defines how the Unformatted codes will be interpreted. Any number of Next Pages may be sent in any order; however, it is recommended that the total number of Next Pages sent be kept small to minimize the link startup time.

Next page transmission ends when both ends of a link segment set their Next Page bits to logical zero, indicating that neither has anything additional to transmit. It is possible for one device to have more pages to transmit than the other device. Once a device has completed transmission of its Next Page information, it shall transmit Next Pages with Null message codes and the NP bit set to logical zero while its link partner continues to transmit valid Next Pages. An Auto-Negotiation able device shall recognize reception of Message Pages with Null message codes as the end of its link partner's Next Page information.

73.7.7.1 Next page encodings

The Next Page shall use the encoding shown in Figure 73–7 and Figure 73–8 for the NP, Ack, MP, Ack2, and T bits. These bits shall function as specified in 28.2.3.4. There are two types of Next Page encodings—message and unformatted. For message Next Pages, the MP bit shall be set to logical one, the 11-bit field D[10:0] shall be encoded as a Message Code Field and D[47:16] shall be encoded as Unformatted Code Field. For Unformatted Next Pages, the MP bit shall be set to logical zero; D[10:0] and D[47:16] shall be encoded as the Unformatted Code Field.

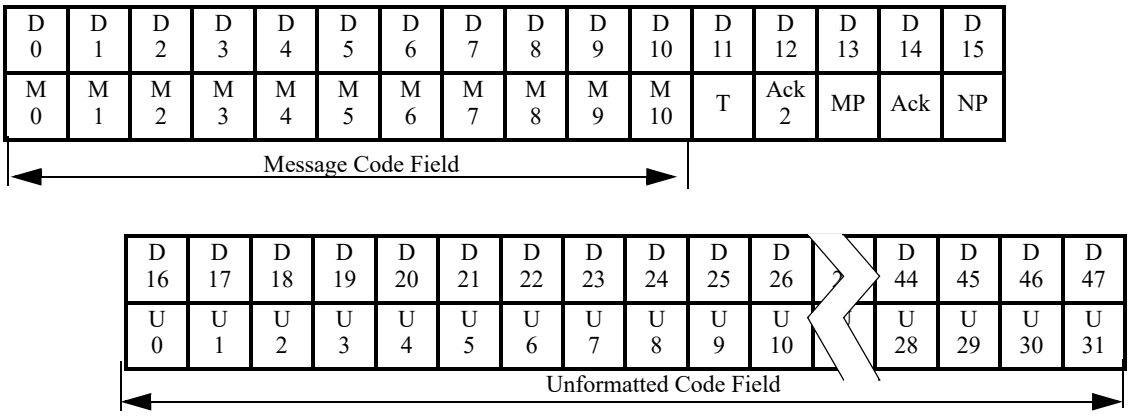

Figure 73–7—Message Next Page

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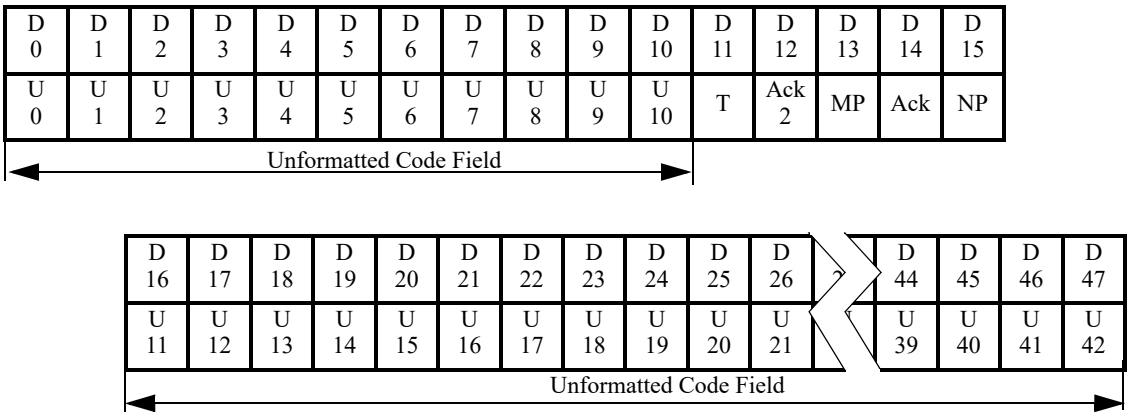

Figure 73–8—Unformatted Next Page

73.7.7.2 Use of Next Pages

Next page exchange will commence after the Base Page exchange if either device requests it by setting the NP bit to logical one.

Next page exchange shall continue until neither device on a link has more pages to transmit as indicated by the NP bit. A Next Page with a Null Message Code Field value shall be sent if the device has no other information to transmit.

A message code can carry either a specific message or information that defines how the corresponding unformatted codes should be interpreted.

73.8 Management register requirements

The management interface is used to communicate Auto-Negotiation information to the management entity. MMD7 of the Clause 45 Management Data Input/Output (MDIO) interface shall be provided as the logical interface to access the device registers for Auto-Negotiation and other management purposes. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended. Table 73–6 provides the mapping of Backplane Ethernet Auto-Negotiation variables to management registers.

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Table 73–6—Backplane Ethernet Auto-Negotiation variable to MDIO register mapping

Variable	Description
mr_adv_ability[48:1]	{7.18.15:0, 7.17.15:0, 7.16.15:0} AN advertisement registers
mr_autoneg_complete	7.1.5 Auto-Negotiation Complete
mr_autoneg_enable	7.0.12 Auto-Negotiation Enable
mr_lp_adv_ability[48:1]	For Base Page: {7.21.15:0, 7.20.15:0, 7.19.15:0} AN LP Base Page ability registers For Next Page(s): {7.27.15:0, 7.26.15:0, 7.25.15:0} AN LP XNP ability registers
mr_lp_autoneg_able	7.1.0 LP Auto-Negotiation Able
mr_main_reset	7.0.15 Reset
mr_next_page_loaded	Set on write to AN XNP Transmit registers; cleared by Arbitration state diagram
mr_np_tx[48:1]	{7.24.15:0, 7.23.15:0, 7.22.15:0} AN XNP Transmit registers
mr_page_rx	7.1.6 Page Received
mr_parallel_detection_fault	7.1.9 Parallel detection Fault
mr_restart_negotiation	7.0.9 Auto-Negotiation Restart
set to 1	7.1.3 Auto-Negotiation Ability
link_control_[x]	{7.48.15:8, 7.48.6:5, 7.48.3:1, 7.49.2:0} Negotiated Port Type
an_baser_fec_control	7.48.4 BASE-R FEC negotiated
an_rs_fec_control	7.48.7 RS-FEC negotiated

73.9 Technology-Dependent interface

The Technology-Dependent interface is the communication mechanism between each technology's PCS and the Auto-Negotiation function. Auto-Negotiation can support multiple technologies, all of which need not be implemented in a given device. Each of these technologies may utilize its own technology-dependent link integrity test function.

73.9.1 AN_LINK.indication

This primitive is generated by the PCS to indicate the status of the underlying medium. The purpose of this primitive is to give the Auto-Negotiation function a means of determining the validity of received code elements.

73.9.1.1 Semantics of the service primitive

AN_LINK.indication(link_status)

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The link_status parameter shall assume one of two values: OK or FAIL, indicating whether the underlying receive channel is intact and enabled (OK) or not intact (FAIL).

73.9.1.2 When generated

A technology-dependent PCS generates this primitive to indicate a change in the value of link_status.

73.9.1.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the state diagram of Figure 73–11.

73.10 State diagrams and variable definitions

The notation used in state diagrams follows the conventions in Clause 28. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

Auto-Negotiation shall implement the Transmit state diagram, Receive state diagram and Arbitration state diagram. Additional requirements to these state diagrams are made in the respective functional requirements sections. Options to these state diagrams clearly stated as such in the functional requirements sections or state diagrams shall be allowed. In the case of any ambiguity between stated requirements and the state diagrams, the state diagrams shall take precedence.

73.10.1 State diagram variables

A variable with "_[x]" appended to the end of the variable name indicates a variable or set of variables as defined by "x". "x" may be as follows:

all;	represents all specific technology-dependent PMDs supported in the local device.
1GKX;	represents the 1000BASE-KX PMD.
2.5GKX;	represents the 2.5GBASE-KX PMD.
5GKR;	represents the 5GBASE-KR PMD.
10GKR;	represents the 10GBASE-KR PMD.
10GKX4;	represents the 10GBASE-KX4 or 10GBASE-CX4 PMD.
25GR;	represents the 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, or 25GBASE-CR-S PMD.
40GKR4;	represents the 40GBASE-KR4 PMD.
40GCR4;	represents the 40GBASE-CR4 PMD.
50GR;	represents the 50GBASE-KR or 50GBASE-CR PMD.
100GCR10;	represents the 100GBASE-CR10 PMD.
100GKP4;	represents the 100GBASE-KP4 PMD.
100GKR4;	represents the 100GBASE-KR4 PMD.
100GCR4;	represents the 100GBASE-CR4 PMD.
100GR2;	represents the 100GBASE-KR2 or 100GBASE-CR2 PMD.
200GR4;	represents the 200GBASE-KR4 or 200GBASE-CR4 PMD.
HCD;	represents the single technology-dependent PMD chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or

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parallel detection function.

notHCD; represents all technology-dependent PMDs not chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or parallel detection function.

PD; represents all of the following that are present: 1000BASE-KX PMD, 2.5GBASE-KX PMD, and 10GBASE-KX4 (or 10GBASE-CX4) PMD.

Variables with [48:1] appended to the end of the variable name indicate arrays that can be directly mapped to 48-bit registers. For these variables, "[x]" indexes an element or set of elements in the array, where "[x]" may be as follows:

a) Any integer
b) Any range of integers
c) Any variable that takes on integer values
d) NP; represents the index of the Next Page bit
e) ACK; represents the index of the Acknowledge bit
f) RF; represents the index of the Remote Fault bit

Variables of the form "mr_x", where x is a label, comprise a management interface that is intended to be connected to the Management function. However, an implementation-specific management interface may provide the control and status function of these bits.

ability_match

Indicates that three consecutive link codewords match, ignoring the Acknowledge bit. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word-match comparison or not.

Values: false; three matching consecutive link codewords have not been received, ignoring the Acknowledge bit (default).
true; three matching consecutive link codewords have been received, ignoring the Acknowledge bit.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

ability_match_word [48:1]

A 48-bit array that is loaded upon transition to Acknowledge Detect state with the value of the link codeword that caused ability_match = true for that transition. For each element in the array transmitted.

Values: zero; data bit is logical zero.
one; data bit is logical one.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

ack_finished

Status indicating that the final remaining_ack_cnt link codewords with the Ack bit set have been transmitted.

Values: false; more link codewords with the Ack bit set to logical one have to be transmitted.
true; all remaining link codewords with the Ack bit set to logical one have been transmitted.

ack_nonce_match

Indicates whether the echoed nonce received from the link partner matches the transmitted nonce

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field sent by the local device. The echoed nonce value from the DME page that caused acknowledge_match to be set is used for this test.

Values false; link partner echoed nonce does not equal local device transmitted nonce.
true; link partner echoed nonce equals local device transmitted nonce.

acknowledge_match

Indicates that three consecutive link codewords match and have the Acknowledge bit set. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word match comparison or not.

Values: false; three matching and consecutive link codewords have not been received with the Acknowledge bit set (default).
true; three matching and consecutive link codewords have been received with the Acknowledge bit set.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

an_link_good

Indicates that Auto-Negotiation has completed.

Values: false; negotiation is in progress (default).
true; negotiation is complete, forcing the Transmit and Receive functions to IDLE.

an_receive_idle

Indicates that the Receive state diagram is in the IDLE or DELIMITER DETECT state.

Values: false; the Receive state diagram is not in the IDLE or DELIMITER DETECT state (default).
true; the Receive state diagram is in the IDLE or DELIMITER DETECT state.

base_page

Status indicating that the page currently being transmitted by Auto-Negotiation is the initial link codeword encoding used to communicate the device's abilities.

Values: false; a page other than base link codeword is being transmitted.
true; the base link codeword is being transmitted.

code_sel

A Boolean random or pseudo-random value uniformly distributed. A new value is generated each time the variable code_sel is used.

Values: zero; a zero has been assigned.
one; a one has been assigned.

complete_ack

Controls the counting of transmitted link codewords that have their Acknowledge bit set.

Values: false; transmitted link codewords with the Acknowledge bit set are not counted (default).
true; transmitted link codewords with the Acknowledge bit set are counted.

consistency_match

Indicates that the ability_match_word same as the link codeword that caused acknowledge_match to be set.

Values: false; the link codeword that caused ability_match to be set is not the same as the link codeword that caused acknowledge_match to be set, ignoring the Acknowledge bit value and the echoed nonce value.

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true; the link codeword that caused ability_match to be set is the same as the link codeword that caused acknowledge_match to be set, ignoring the Acknowledge bit value and the echoed nonce value.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

detect_mv_pair

Status indicating that the receiver has detected the pair of Manchester violations forming a Manchester Violation delimiter—a sequence of three consecutive transitions with 12.8 ns ± 200 ps between each pair of transitions.

Values: false; set to false after any Receive State Diagram state transition (default).
true; Manchester violation pair has been detected.

detect_transition

Status indicating that the receiver has detected a transtion.

Values: false; set to false after any Receive State Diagram state transition (default).
true; set to true when a transition is received.

incompatible_link

Parameter used following Priority Resolution to indicate the resolved link is incompatible with the local device settings. A device's ability to set this variable to true is optional.

Values: false; A compatible link exists between the local device and link partner (default).
true; Optional indication that Priority Resolution has determined no highest common denominator exists following the most recent negotiation.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

link_control_[x]

Controls the connection of each PMD to the MDI. When all PMD transmitters are isolated from the MDI, the AN transmitter is connected to the MDI.

Values: DISABLE; isolates the PMD from the MDI.
SCAN_FOR_CARRIER; connects the PMD receiver to the MDI and isolates the PMD transmitter from the link.
ENABLE; connects the PMD (both transmit and receive) to the MDI.

link_status_[x]

This variable is defined in 73.9.1.

mr_autoneg_complete

Status indicating whether Auto-Negotiation has completed or not.

Values: false; Auto-Negotiation has not completed.
true; Auto-Negotiation has completed.

mr_autoneg_enable

Controls the enabling and disabling of the Auto-Negotiation function.

Values: false; Auto-Negotiation is disabled.
true; Auto-Negotiation is enabled.

mr_adv_ability[48:1]

A 48-bit array that contains the Advertised Abilities link codeword.
For each element within the array:

Values: zero; data bit is logical zero.

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one; data bit is logical one.

mr_lp_adv_ability[48:1]

A 48-bit array that contains the link partner's Advertised Abilities link codeword.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_autoneg_able

Status indicating whether the link partner supports Auto-Negotiation.

Values: false; the link partner does not support Auto-Negotiation.
true; the link partner supports Auto-Negotiation.

mr_main_reset

Controls the resetting of the Auto-Negotiation state diagrams.

Values: false; do not reset the Auto-Negotiation state diagrams.
true; reset the Auto-Negotiation state diagrams.

mr_next_page_loaded

Status indicating whether a new page has been loaded into the AN XNP transmit register (45.2.7.8).

Values: false; a New Page has not been loaded.
true; a New Page has been loaded.

mr_np_tx[48:1]

A 48-bit array that contains the new Next Page to transmit.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_page_rx

Status indicating whether a New Page has been received. A New Page has been successfully received when acknowledge_match=true and consistency_match=true and the link codeword has been written to mr_lp_adv_ability[48:1].

Values: false; a New Page has not been received.
true; a New Page has been received.

mr_parallel_detection_fault

Error condition indicating that while performing parallel detection, either an_receive_idle = false, or zero or more than one of the following indications were present when the autoneg_wait_timer expired. This signal is cleared on read of the AN status register (register 7.1).

1) link_status_ [1GKX] = OK
2) link_status_[10GKX4] = OK

Values: false; Exactly one of the above two indications was true when the autoneg_wait_timer expired, and an_receive_idle = true.
true; either zero or more than one of the above two indications was true when the autoneg_wait_timer expired, or an_receive_idle = false.

mr_restart_negotiation

Controls the entrance to the TRANSMIT DISABLE state to break the link before Auto-Negotiation is allowed to renegotiate via management control.

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Values: false; renegotiation is not taking place.
true; renegotiation is started.

nonce_match

Indicates whether the transmitted nonce received from the link partner matches the transmitted nonce field sent by the local device.

Values false; link partner transmitted nonce does not equal local device transmitted nonce.
true; link partner transmitted nonce equals local device transmitted nonce.

np_rx

Flag to hold the value of rx_link_code_word[NP] upon entry to the COMPLETE ACKNOWLEDGE state. This value is associated with the value of rx_link_code_word[NP] when acknowledge_match was last set.

Values zero; local device np_rx bit equals a logical zero.
one; local device np_rx bit equals a logical one.

power_on

Condition that is true until such time as the power supply for the device that contains the Auto-Negotiation state diagrams has reached the operating region or the device has low-power mode set via MMD control register bit 1.120.12.

Values: false; the device is completely powered (default).
true; the device has not been completely powered.

pulse_too_long

Indicates that the receiver has detected successive transitions spaced too far apart for a valid DME page. Transitions separated by more than 20 ns shall cause this indication to be true. Valid Manchester violation delimiters shall not cause this indication to be true.

Values: false; excessively long pulses have not been detected.
true; excessively long pulses have been detected.

pulse_too_short

Indicates that the receiver has detected successive transitions spaced too closely for a valid DME page. Transitions separated by less than 1.6 ns shall cause this indication to be true. Valid Manchester transitions shall not cause this indication to be true.

Values: false; excessively short pulses have not been detected.
true; excessively short pulses have been detected.

rx_link_code_word[48:1]

A 48-bit array that contains the data bits to be received from a DME page.
For each element within the array:

Values: zero; data bit is a logical zero.
one; data bit is a logical one.

rx_nonce[4:0]

A 5-bit array that contains the transmitted nonce received from the DME page that caused ability_match=true.
For each element within the array:

Values: zero; data bit is a logical zero.
one; data bit is a logical one.

single_link_ready

Status indicating that an_receive_idle = true and only one the of the following indications is being

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received:

1) link_status_[1GKX] = OK
2) link_status_[2.5GKX] = OK
3) link_status_[5GKR] = OK
4) link_status_[10GKX4] = OK
5) link_status_[10GKR] = OK
6) link_status_[25GR] = OK
7) link_status_[40GKR4] = OK
8) link_status_[40GCR4] = OK
9) link_status_[50GR] = OK
10) link_status_[100GCR10] = OK
11) link_status_[100GKP4] = OK
12) link_status_[100GKR4] = OK
13) link_status_[100GCR4] = OK
14) link_status_[100GR2] = OK
15) link_status_[200GR4] = OK

Values: false; either zero or more than one of the above indications are true or an_receive_idle = false.
true; Exactly one of the above indications is true and an_receive_idle = true.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

TD_AUTONEG

Controls the signal sent by Auto-Negotiation on the TD_AUTONEG circuit.

Values: disable; transmission of Auto-Negotiation signals is disabled
idle; Auto-Negotiation maintains the current signal level on the MDI.
mv_delimiter; Auto-Negotiation causes the transmission of the Manchester violation delimiter on the MDI.
transition; Auto-Negotiation causes a transition in the level on the MDI.

toggle_rx

Flag to keep track of the state of the link partner's Toggle bit.

Values: zero; link partner's Toggle bit equals logical zero.
one; link partner's Toggle bit equals logical one.

toggle_tx

Flag to keep track of the state of the local device's Toggle bit.

Values: zero; local device's Toggle bit equals logical zero.
one; local device's Toggle bit equals logical one.

transmit_ability

Controls the transmission of the link codeword containing tx_link_code_word[48:1].

Values: false; any transmission of tx_link_code_word[48:1] is halted (default).
true; the transmit state diagram begins sending tx_link_code_word[48:1].

transmit_ack

Controls the setting of the Acknowledge bit in the tx_link_code_word[48:1] to be transmitted.

Values: false; sets the Acknowledge bit in the transmitted tx_link_code_word[48:1] to a logical zero (default).

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true; sets the Acknowledge bit in the transmitted tx_link_code_word[48:1] to a logical one.

transmit_disable

Controls the transmission of tx_link_code_word[48:1].

Values: false; tx_link_code_word[48:1] transmission is allowed (default).
true; tx_link_code_word[48:1] transmission is halted.

transmit_mv_done

Status indicating that the transmission of the Manchester violation delimiter has been completed.

Values: false; transmission of the Manchester violation is in progress.
true; transmission of the Manchester violation has been completed.

tx_link_code_word[49:1]

A 49-bit array that contains the data bits to be transmitted in an DME page.
tx_link_code_word[48:1] contains the Auto-Negotiation page to be transmitted.
tx_link_code_word[49] contains the pseudo-random bit. This array may be loaded from mr_adv_ability or mr_np_tx.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

73.10.2 State diagram timers

All timers operate in the manner described in 14.2.3.2.

autoneg_wait_timer

Timer for the amount of time to wait before evaluating the number of link integrity test functions with link_status=OK asserted. The autoneg_wait_timer shall expire 25 ms to 50 ms from the assertion of link_status=OK from the PCS.

break_link_timer

Timer for the amount of time to wait in order to assure that the link partner enters a Link Fail state. The timer shall expire 60 ms to 75 ms after being started.

clock_detect_min_timer

Timer for the minimum time between detection of differential Manchester clock transitions. The clock_detect_min_timer shall expire 4.8 ns to 6.2 ns after being started or restarted.

clock_detect_max_timer

Timer for the maximum time between detection of differential Manchester clock transitions. The clock_detect_max_timer shall expire 6.6 ns to 8.0 ns after being started or restarted.

data_detect_max_timer

Timer for the maximum time between a clock transition and the following data transition. This timer is used in conjunction with the data_detect_min_timer to detect whether the data bit between two clock transitions is a logical zero or a logical one. The data_detect_max_timer shall expire 3.4 ns to 4.8 ns from the last clock transition.

data_detect_min_timer

Timer for the minimum time between a clock transition and the following data transition. This timer is used in conjunction with the data_detect_max_timer to detect whether the data bit between two clock transitions is a logical zero or a logical one. The data_detect_min_timer shall expire 1.6 ns 3.0 ns from the last clock transition.

interval_timer

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Timer for the separation of a transmitted clock pulse from a data bit. The interval_timer shall expire 3.2 ns ± 0.01% from each clock pulse and data bit.

link_fail_inhibit_timer

Timer for qualifying a link_status=FAIL indication or a link_status=OK indication when a specific technology link is first being established. A link will only be considered "failed" if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The link_fail_inhibit_timer shall expire within the timer values given in Table 73–7 after entering the AN LINK GOOD CHECK state.

NOTE—The link_fail_inhibit_timer expiration value has to be greater than the time required for the link partner to complete Auto-Negotiation after the local device has completed Auto-Negotiation plus the time required for the specific technology to enter the link_status=OK state.

page_test_max_timer

Timer for the maximum time between detection of Manchester violation delimiters. This timer is used in conjunction with the page_test_min_timer to detect whether the link partner is transmitting DME pages. The page_test_max_timer shall expire 350 ns to 375 ns after being started or restarted.

page_test_min_timer

Timer for the minimum time between detection of Manchester violation delimiters. This timer is used in conjunction with the page_test_max_timer to detect whether the link partner is transmitting DME pages. The page_test_min_timer shall expire 305 ns 330 ns after being started or restarted.

Table 73–7—Timer min/max value summary

Parameter	Min	Value and tolerance	Max	Units
autoneg_wait_timer	25		50	ms
break_link_timer	60		75	ms
clock_detect_min_timer	4.8		6.2	ns
clock_detect_max_timer	6.6		8.0	ns
data_detect_min_timer	1.6		3.0	ns
data_detect_max_timer	3.4		4.8	ns
interval_timer		3.2 ± 0.01%		ns
link_fail_inhibit_timer (when the link is 50GBASE-KR, 50GBASE-CR, 100GBASE-KR2, 100GBASE-CR2, 200GBASE-KR4 or 200GBASE-CR4)	3.1		3.2	s
link_fail_inhibit_timer (when the link is 10GBASE-KR, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, 25GBASE-CR-S, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-KR4, 100GBASE-KP4, 100GBASE-CR4, or 100GBASE-CR10)	500		510	ms
link_fail_inhibit_timer (when the link is 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, or 10GBASE-KX4)	40		50	ms
page_test_min_timer	305		330	ns
page_test_max_timer	350		375	ns

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73.10.3 State diagram counters

remaining_ack_cnt

A counter that may take on integer values from 0 to 8. The number of additional link codewords with the Acknowledge Bit set to logical one to be sent to ensure that the link partner receives the acknowledgment.

Values: not_done; positive integers between 0 and 5 inclusive.
done; positive integers 6 to 8 inclusive (default).
init; counter is reset to zero.

rx_bit_cnt

A counter that may take on integer values from 0 to 49. This counter is used to keep a count of data bits received from a DME page and to ensure that when erroneous extra transitions are received, the first 48 bits are kept while the rest are ignored. When this variable reaches 49, enough data bits have been received. This counter does not increment beyond 49 and does not return to 0 until it is reinitialized.

Values: not_done; 0 to 48 inclusive.
done; 49
init; counter is reset to zero.

tx_bit_cnt

A counter that may take on integer values from 1 to 50. This counter is used to keep a count of data bits sent within a DME page. When this variable reaches 50, all data bits have been sent.

Values: not_done; 1 to 49 inclusive.
done; 50.
init; counter is initialized to 1.

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73.10.4 State diagrams

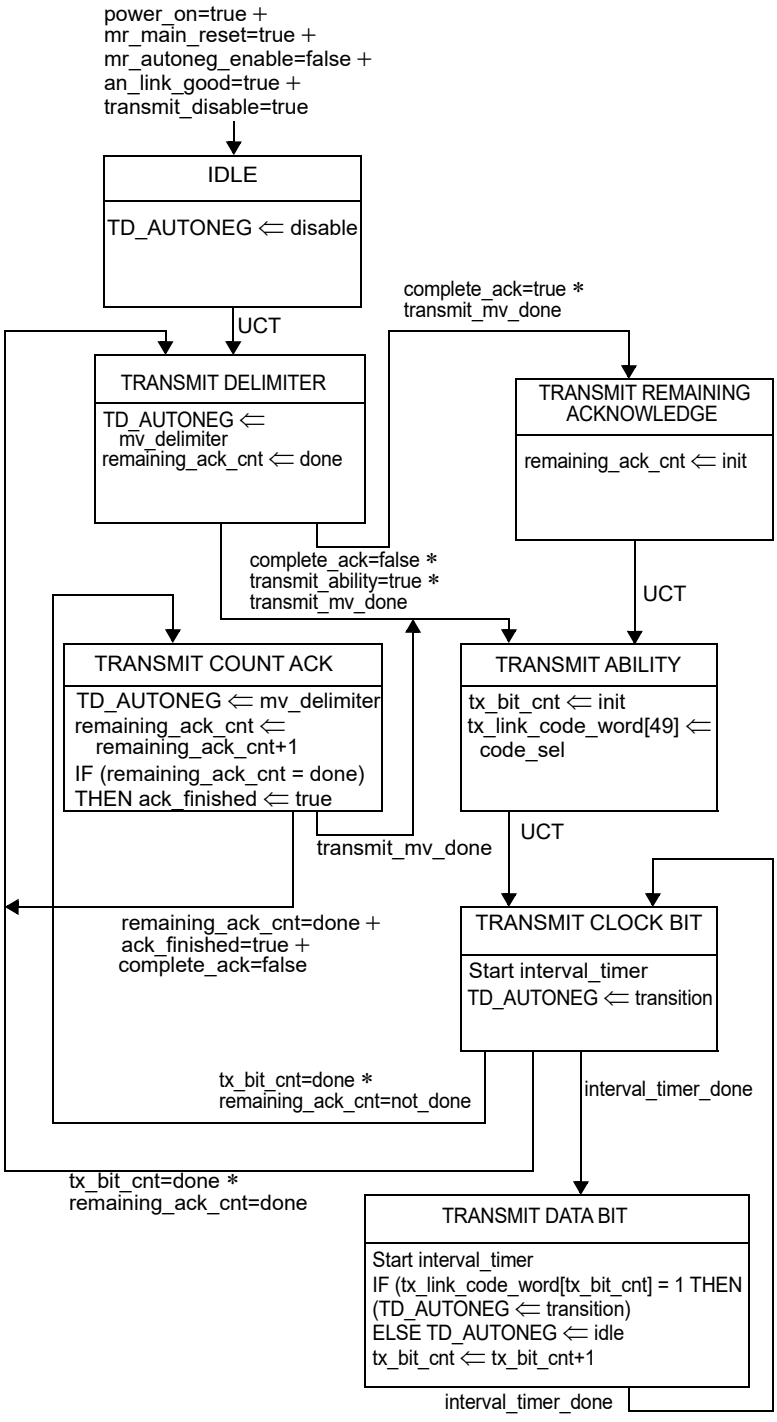

Figure 73–9—Transmit state diagram

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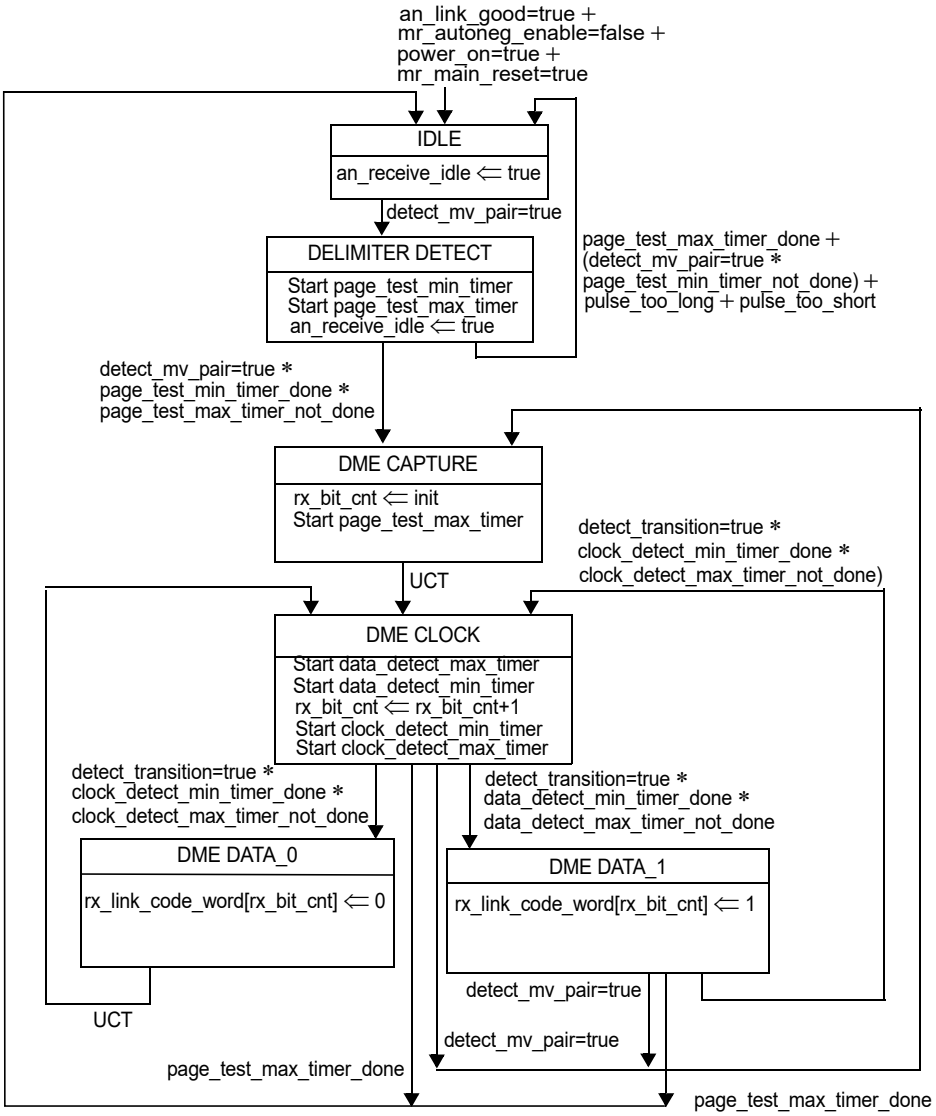

Figure 73–10—Receive state diagram

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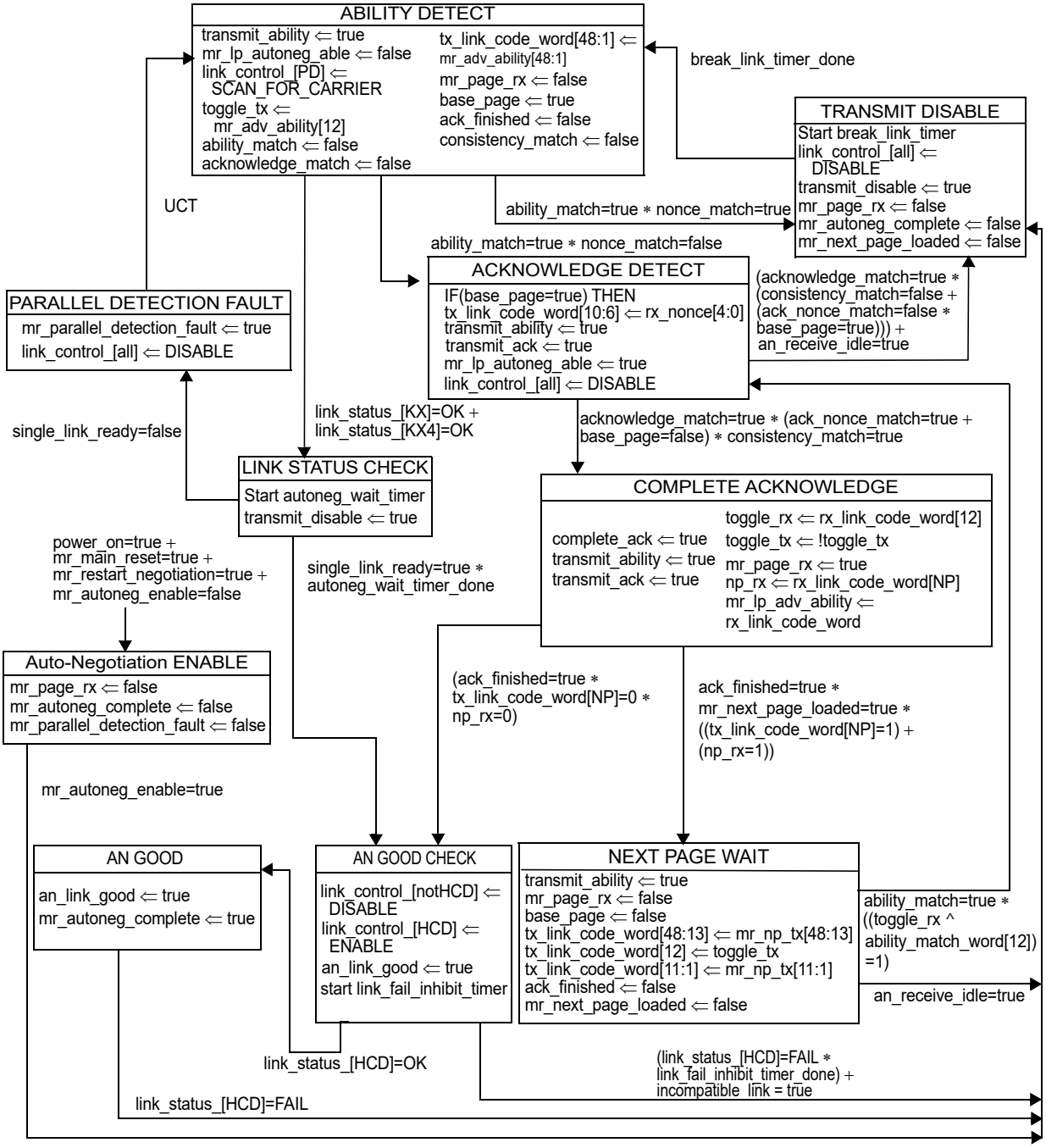

Figure 73–11—Arbitration state diagram

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73.11 Protocol implementation conformance statement (PICS) proforma for Clause 73, Auto-Negotiation for backplane and copper cable assembly[136]

73.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3, Clause 73, Auto-Negotiation for backplane and copper cable assembly, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

73.11.2 Identification

73.11.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

73.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 73, Auto-Negotiation for backplane and copper cable assembly
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[136]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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73.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
ANG	Auto-Negotiation	73.1		M	Yes [ ]
PLD	Parallel detection	73.1		M	Yes [ ]
NP	Next page support	73.6.9		M	Yes [ ]

73.11.4 PICS proforma tables for Auto-Negotiation for backplane and copper cable assembly

73.11.4.1 Functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Clause 37 Auto-Negotiation	73.1	Clause 37 Auto-Negotiation to be disabled	O	Yes [ ] No [ ]
FS2	Device intends to enable Clause 37 Auto-Negotiation after Clause 73 Auto-Negotiation	73.1	Ensure that link partner intends to enable Clause 37 Auto-Negotiation	FS1:M	Yes [ ]
FS3	Advertised abilities for Clause 37 Auto-Negotiation	73.1	Shall match those advertised in Clause 73 Auto-Negotiation	FS1:M	Yes [ ]
FS4	Auto-Negotiation functions	73.3	Auto-Negotiation function shall provide transmit, receive, and arbitration	M	Yes [ ]
FS5	Compliance with state diagrams	73.3	Figure 73–9 through Figure 73–11	M	Yes [ ]
FS6	Interaction with PHYs	73.3	Auto-Negotiation shall interact with technology-dependent PHYs through Technology -Dependent interface.	M	Yes [ ]

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73.11.4.2 DME transmission

Item	Feature	Subclause	Value/Comment	Status	Support
DT1	Transmission of DME pages	73.5	DME pages shall not be transmitted when Auto-Negotiation is complete and HCD PHY has been enabled	M	Yes [ ]
DT2	Multi-lane DME pages	73.5.1	Multi-lane DME pages shall be transmitted on Lane 0	M	Yes [ ]
DT3	DME electrical characteristics	73.5.1	Meet requirements of Table 73–1	M	Yes [ ]
DT4	Transitions in odd numbered positions	73.5.2	Remaining 49 odd-numbered positions shall contain a transition	M	Yes [ ]
DT5	Transitions in even numbered positions	73.5.2	Remaining 49 even-numbered positions shall represent data	M	Yes [ ]
DT6	First 48 even numbered positions	73.5.2	First 48 even numbered positions shall carry data of Auto-Negotiation page	M	Yes [ ]
DT7	Pseudo-random bit value	73.5.2	Value shall be derived from source as defined in 48.2.4.2	M	Yes [ ]
DT8	Pseudo-random counter	73.5.2	Counter shall increment once per DME page	M	Yes [ ]
DT9	DME page timing parameters	73.5.3	Meet requirements of Table 73–2	M	Yes [ ]

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73.11.4.3 Link codeword encoding

Item	Feature	Subclause	Value/Comment	Status	Support
LE1	Link codeword encoding	73.6	As shown in Figure 73–6	M	Yes [ ]
LE2	First bit transmitted	73.6	D0	M	Yes [ ]
LE3	RF, ACK, NP bits	73.6	As specified in 28.2.1.1	M	Yes [ ]
LE4	Reserved Selector Field	73.6.1	Shall not be transmitted	M	Yes [ ]
LE5	Echoed Nonce Field with Acknowledge set to zero	73.6.2	Contains logical zeros	M	Yes [ ]
LE6	Echoed Nonce Field with Acknowledge set to one	73.6.2	Values received in Transmitted Nonce Field from Link Partner	M	Yes [ ]
LE7	Transmitted Nonce Field	73.6.3	New value generated for each entry into Ability Detect	M	Yes [ ]
LE8	Support of multiple technologies	73.6.4	Shall support all technologies advertised	M	Yes [ ]
LE9	Technology ability reserved fields	73.6.4	Sent as zero and ignored by the receiver	M	Yes [ ]
LE10	FEC capability resolution	73.6.5	Resolve enabling of FEC capability based on F0 and F1 bits	M	Yes [ ]
LE11	Acknowledge with no Next Page	73.6.8	Set to 1 after three DME pages	M	Yes [ ]
LE12	Acknowledge with Next Page	73.6.8	Set to 1 after three DME pages	M	Yes [ ]
LE13	Device has no Next Pages to send	73.6.9	Next Page bit set to 0	M	Yes [ ]
LE14	Device has Next Pages to send	73.6.9	Next Page bit set to 1	M	Yes [ ]
LE15	Transmit switch function upon entry into the AN_GOOD_CHECK state	73.6.10	Connect the transmit path of HCD PHY to the MDI	M	Yes [ ]
LE16	Transmit switch function during Auto-Negotiation and prior to entry into the AN_GOOD_CHECK state	73.6.10	Connect only DME page generator to MDI	M	Yes [ ]
LE17	PHY connection to MDI	73.6.10	Signals at MDI conform to all PHY specifications within 20 ms	M	Yes [ ]

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73.11.4.4 Receive function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Receive switch function upon entry into the AN_GOOD_CHECK state	73.7.2	Connect the receive path of HCD PHY to the MDI	M	Yes [ ]
RF2	Receive switch function during Auto-Negotiation and prior to entry into the AN_GOOD_CHECK state	73.7.2	Connect DME page receiver to MDI	M	Yes [ ]
RF3	Receive switch function during Auto-Negotiation and prior to entry into the AN_GOOD_CHECK state	73.7.2	Connect receive path of the 1000BASE-KX and 10GBASE-KX4 PHY when present	M	Yes [ ]
RF4	Receive function variables	73.7.3	As defined in Figure 73–11	M	Yes [ ]
RF5	Parallel detection for 1000BASE-KX, 2.5GBASE-KX, and 10GBASE-KX4	73.7.4.1	Device provides parallel detection if it supports those PHYs	M	Yes [ ]
RF6	Parallel detection	73.7.4.1	Direct MDI receive activity to PHYs prior to DME detection	M	Yes [ ]
RF7	Enable one link after parallel detection	73.7.4.1	Enable link if signaling is present	M	Yes [ ]
RF8	Disable all other links after parallel detection	73.7.4.1	Disable all other PHYs	M	Yes [ ]
RF9	Parallel detection register settings	73.7.4.1	Set bit corresponding to technology detected	M	Yes [ ]
RF10	Detection of link_status=OK	73.7.4.1	autoneg_wait_timer starts	M	Yes [ ]
RF11	Renegotiation request	73.7.5	Disable PHYs and halt transmissions for break_link_timer	M	Yes [ ]
RF12	Resumption of Auto-Negotiation	73.7.5	Resume Auto-Negotiation after expiration of break_link_timer	M	Yes [ ]
RF13	Priority resolution	73.7.6	PHY with highest priority connected to MDI	M	Yes [ ]
RF14	Reception of reserved technology ability field bits	73.7.6	Ignore reserved technology ability field bits	M	Yes [ ]
RF15	Priority resolution through parallel detection	73.7.6	PHY chose through parallel detection is HCD	M	Yes [ ]
RF16	Priority resolution with no common technology	73.7.6	HCD takes on value of NULL and link_status=FAIL	M	Yes [ ]

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73.11.4.5 Next Page function

Item	Feature	Subclause	Value/Comment	Status	Support
NP1	Message codes	73.7.7	Each series of Next Pages has Message code	M	Yes [ ]
NP2	Next Page transmission while link partner not done	73.7.7	Device transmits Null Message code and sets NP bit to 0	M	Yes [ ]
NP3	Reception of Null message codes	73.7.7	Recognized as end of link partner's Next Pages	M	Yes [ ]
NP4	Next page encoding	73.7.7.1	As shown in Figure 73–7 and Figure 73–8	M	Yes [ ]
NP5	NP, Ack, MP, Ack2, T bits	73.7.7.1	As specified in 28.2.3.4	M	Yes [ ]
NP6	MP bit for message Next Pages	73.7.7.1	Set to logical one	M	Yes [ ]
NP7	Message Code Field in message Next Page	73.7.7.1	Encoded in D[10:0]	M	Yes [ ]
NP8	Unformatted Code Field in message Next Page	73.7.7.1	Encoded in D[47:16]	M	Yes [ ]
NP9	MP bit for Unformatted Next Pages	73.7.7.1	Set to logical zero	M	Yes [ ]
NP10	Unformatted Code Field in Unformatted Next Pages	73.7.7.1	Encoded in D[15:0] and D[47:16]	M	Yes [ ]
NP11	Continuation of Next Page exchange	73.7.7.2	Exchange continues until NP bit is zero on both devices	M	Yes [ ]
NP12	Transmission of Null Message Code field	73.7.7.2	Sent if device has no other information to transmit	M	Yes [ ]

73.11.4.6 Management register requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MR1	MMD 7 of Clause 45 MDIO	73.8	Logical interface for access to device registers	M	Yes [ ]
MR2	Clause 45 electrical interface	73.8	Electrical interface for access to device registers	O	Yes [ ] No [ ]

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73.11.4.7 State diagrams and variable definitions

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Support of state diagrams	73.10	Transmit, Receive, Arbitration	M	Yes [ ]
SD2	Support of options	73.10	Options are allowed	M	Yes [ ]
SD3	Ambiguity between state diagrams and text	73.10	State diagrams take precedence	M	Yes [ ]
SD4	Pulse too short	73.10.1	Transitions separated by less than 1.6 ns	M	Yes [ ]
SD5	Pulse too short with valid transitions	73.10.1	Valid transitions not to cause this to be true	M	Yes [ ]
SD6	Pulse too long	73.10.1	Transitions separated by more than 20 ns	M	Yes [ ]
SD7	Pulse too long with valid violation delimiters	73.10.1	Valid Manchester violation delimiters not to set this	M	Yes [ ]
SD8	autoneg_wait_timer	73.10.2	25 ms to 50 ms	M	Yes [ ]
SD9	break_link_timer	73.10.2	60 ms to 75 ms	M	Yes [ ]
SD10	clock_detect_min_timer	73.10.2	4.8 ns to 6.2 ns	M	Yes [ ]
SD11	clock_detect_max_timer	73.10.2	6.6 ns to 8.0 ns	M	Yes [ ]
SD12	data_detect_max_timer	73.10.2	4.0 ns to 4.8 ns	M	Yes [ ]
SD13	data_detect_min_timer	73.10.2	1.6 ns to 2.4 ns	M	Yes [ ]
SD14	interval_timer	73.10.2	3.2 ns ± 0.01%	M	Yes [ ]
SD15	link_fail_inhibit_timer	73.10.2	The values in Table 73–7	M	Yes [ ]
SD16	page_test_max_timer	73.10.2	350 ns to 375 ns	M	Yes [ ]
SD17	page_test_min_timer	73.10.2	305 ns to 330 ns	M	Yes [ ]

73.11.4.8 Service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
SP1	link_status parameter	73.9.1.1	OK, FAIL	M	Yes [ ]
SP2	Generation of link_status primitive	73.9.1.2	Generated by technology dependent PCS	M	Yes [ ]
SP3	Receipt of link_status primitive	73.9.1.3	Governed by Figure 73–10	M	Yes [ ]

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73.11.4.9 Auto-Negotiation annexes

Item	Feature	Subclause	Value/Comment	Status	Support
AN1	Null Message code	73A.1	Transmitted during Next Page exchange when local device has no information to transmit and link partner has additional pages to transmit	M	Yes [ ]
AN2	OUI message code	73A.2	0000 0000 0101	M	Yes [ ]
AN3	OUI first user code	73A.2	OUI or CID (bits 23:13)	M	Yes [ ]
AN4	OUI second user code	73A.2	OUI or CID (bits 12:2)	M	Yes [ ]
AN5	OUI third user code	73A.2	OUI or CID (bits 1:0)	M	Yes [ ]
AN6	OUI fourth user code	73A.2	User-defined code value	M	Yes [ ]
AN7	AN device identifier Message code	73A.3	0000 0000 0110	M	Yes [ ]
AN8	AN device identifier first user code	73A.3	AN device identifier (7.2.15:5)	M	Yes [ ]
AN9	AN device identifier second user code	73A.3	AN device identifier (7.2.4:0 to 7.3.15:10)	M	Yes [ ]
AN10	AN device identifier third user code	73A.3	AN device identifier (7.3.9:0)	M	Yes [ ]
AN11	AN device identifier third user code bit 0	73A.3	User-defined code value	M	Yes [ ]
AN12	AN device identifier fourth user code	73A.3	User-defined code value	M	Yes [ ]
AN13	AN message code 10	73A.4	EEE technology message code	M	Yes [ ]

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74. Forward error correction (FEC) sublayer for BASE-R PHYs

74.1 Overview

This clause specifies a forward error correction (FEC) sublayer for 10GBASE-R and other BASE-R PHYs. The FEC sublayer can be placed in between the PCS and PMA sublayers of the 10GBASE-R and other BASE-R Physical Layer implementations as shown in Figure 74–2, Figure 74–3, Figure 74–4, and Figure 74–5. For a PHY with a multi-lane BASE-R PCS, the FEC sublayer is instantiated for each PCS lane and operates autonomously on a per PCS lane basis. The FEC provides coding gain to increase the link budget and BER performance.

The 10GBASE-KR and 40GBASE-KR4 PHYs described in Clause 72 and Clause 84 optionally use the FEC sublayer to increase the performance on a broader set of backplane channels than are defined in Clause 69. The FEC sublayer provides additional margin to account for variations in manufacturing and environmental conditions.

The 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, and 25GBASE-KR-S PHYs described in Clause 110 and Clause 111 are required to implement the FEC sublayer and may use it with links with a BER of 10^{-8} or better.

The 40GBASE-CR4 and 100GBASE-CR10 PHYs described in Clause 85 optionally use the FEC sublayer to improve the BER performance beyond 10^{-12}.

74.2 Objectives

NOTE—The contents of this subclause have been deleted.

74.3 Relationship to other sublayers

Figure 74–1 depicts the relationships among the BASE-R FEC (shown shaded), the MAC and Reconciliation Sublayers, the BASE-R PCS, PMA and PMD, the ISO/IEC 8802-2 LLC, and the ISO/IEC Open System Interconnection (OSI) reference model.

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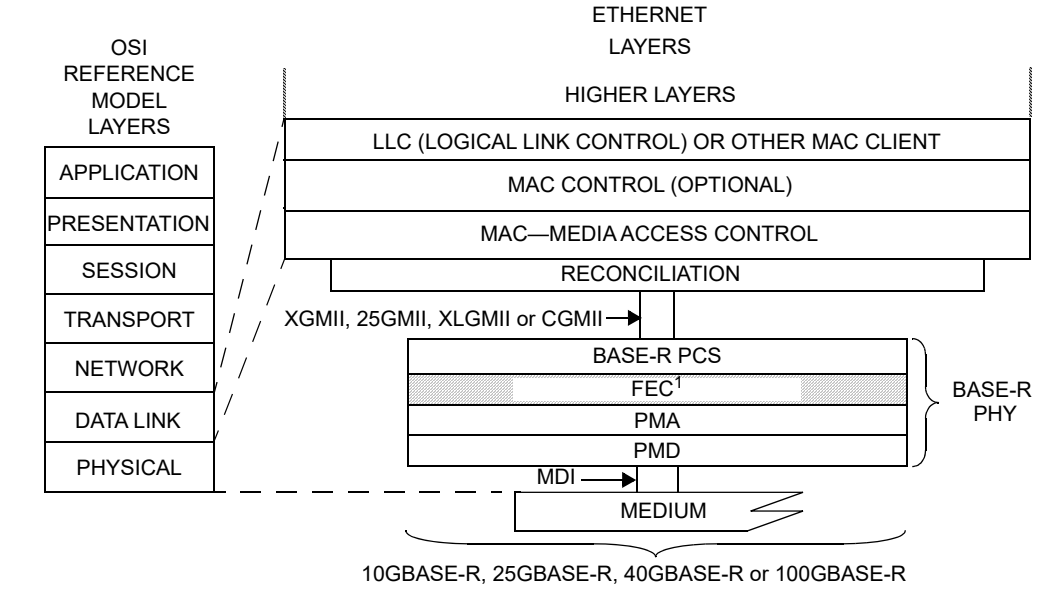

25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XGMII = 10 Gb/s MEDIA INDEPENDENT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—OPTIONAL OR CONDITIONAL BASED ON PHY TYPE

Figure 74–1—BASE-R FEC relationship to ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

74.4 Inter-sublayer interfaces

An FEC service interface is provided to allow the FEC sublayer to transfer information to and from the PCS. An abstract service model is used to define the operation of this interface. For 10GBASE-R, the FEC service interface directly maps to the PMA service interface of the PCS defined in Clause 49 and the lower FEC sublayer interface maps to the service interface provided by the serial PMA sublayer defined in Clause 51. For 25GBASE-R, the FEC service interface is an instance of the inter-sublayer service interface defined in 105.4, as is the PMA service interface defined in 109.2. For 40GBASE-R and 100GBASE-R, the FEC service interface is an instance of the inter-sublayer service interface defined in 80.3 as is the PMA service interface defined in 83.2.

For 25GBASE-R the FEC service interface can either connect to the PCS as illustrated in Figure 74–1 or the PMA as illustrated in Figure 109–3 where the FEC and PCS are in separate devices connected by 25GAUI.

For 40GBASE-R and 100GBASE-R the FEC service interface can either connect to the PCS as illustrated in Figure 74–1 or the PMA as illustrated in Figure 83–2 where the FEC and PCS are in separate devices connected by XLAUI/CAUI-n.

This standard defines these interfaces in terms of bits, octets, data-group, data units, and signals; however, implementers may choose other data-path widths and other control mechanisms for implementation convenience, provided that the implementation adheres to the logical model of the service interface.

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74.4.1 Functional Block Diagram for 10GBASE-R PHYs

Figure 74–2 shows the functional block diagram of FEC for 10GBASE-R PHY and the relationship between the PCS and PMA sublayers.

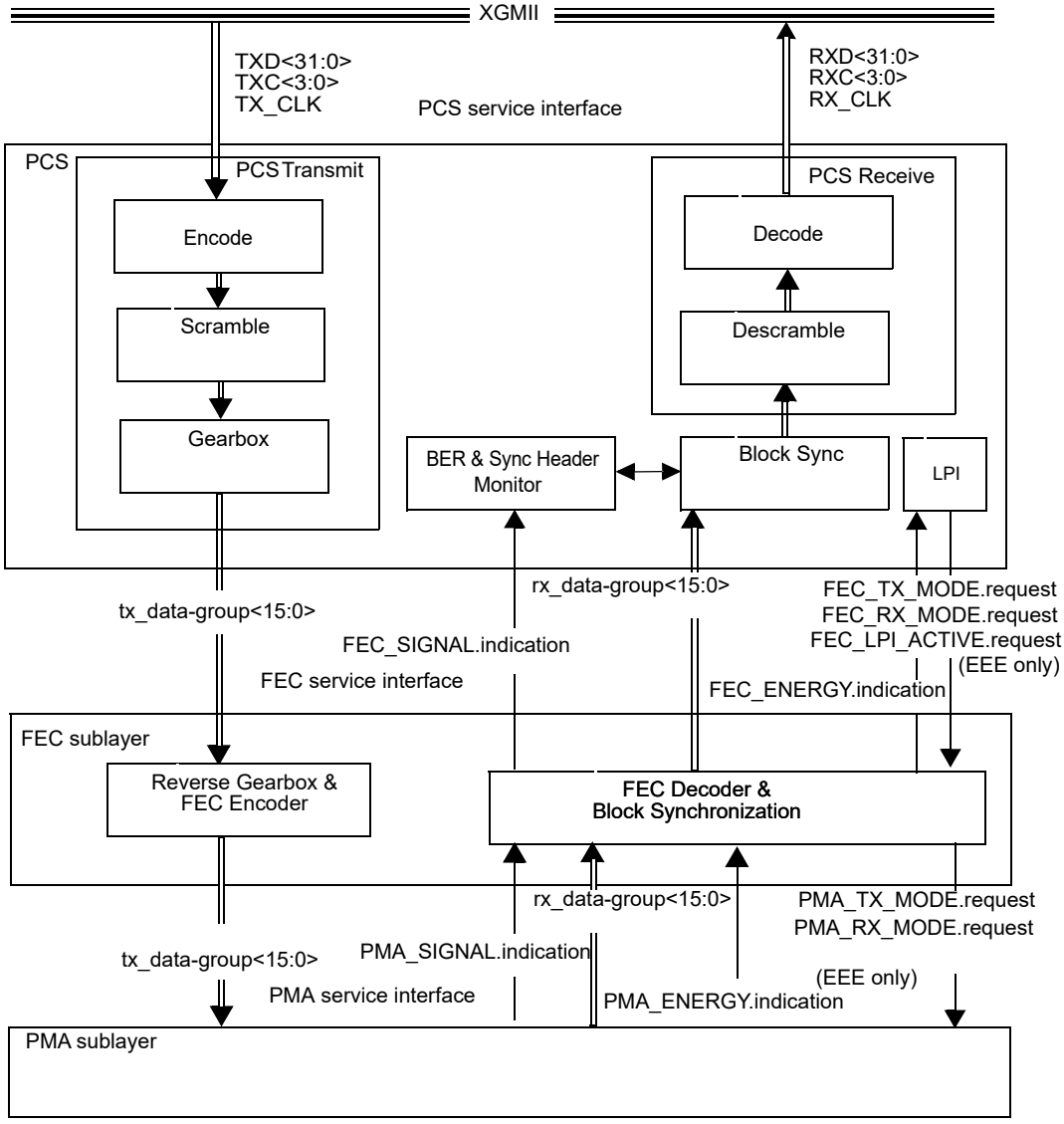

Figure 74–2—Functional block diagram for 10GBASE-R PHYs

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74.4.2 Functional block diagram for 25GBASE-R PHYs

Figure 74–3 shows the functional block diagram of FEC for 25GBASE-R PHYs and the relationship between the PCS and PMA sublayers.

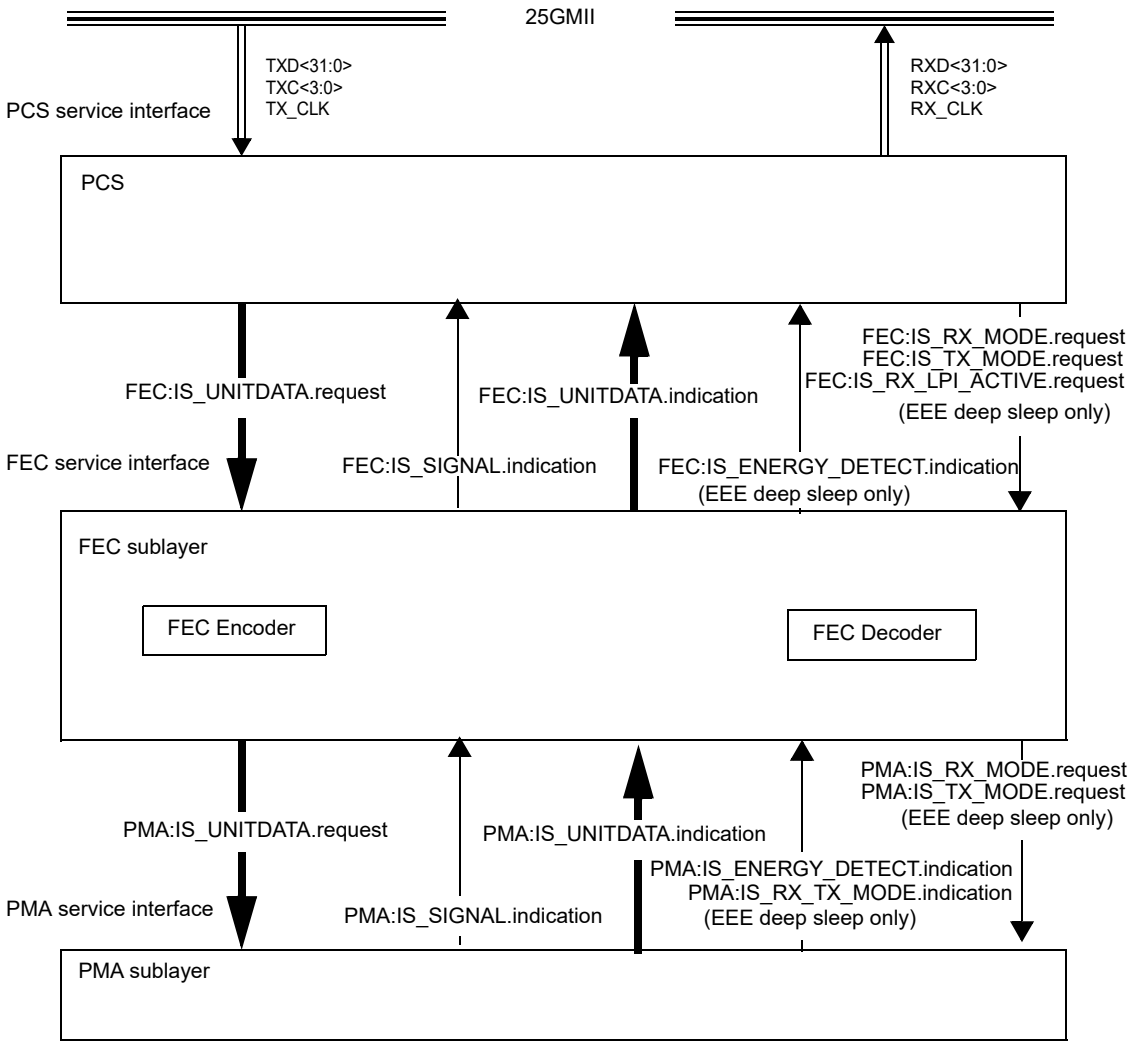

Figure 74–3— Functional block diagram for 25GBASE-R PHY

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74.4.3 Functional block diagram for 40GBASE-R PHYs

Figure 74–4 shows the functional block diagram of FEC for 40GBASE-R PHYs and the relationship between the PCS and PMA sublayers.

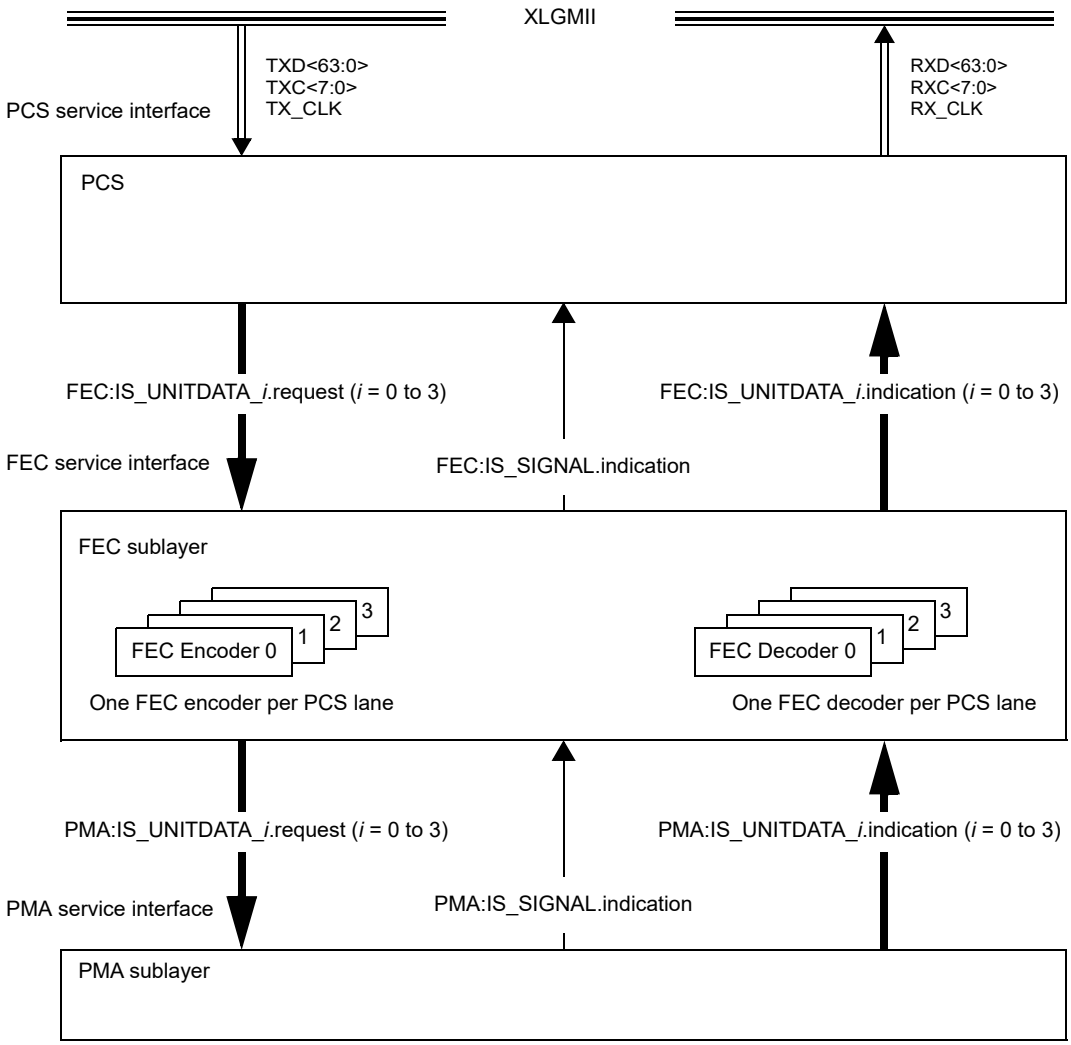

Figure 74–4—Functional block diagram for 40GBASE-R PHY

74.4.4 Functional block diagram for 100GBASE-R PHYs

Figure 74–5 shows the functional block diagram of FEC for 100GBASE-R PHYs and the relationship between the PCS and PMA sublayers.

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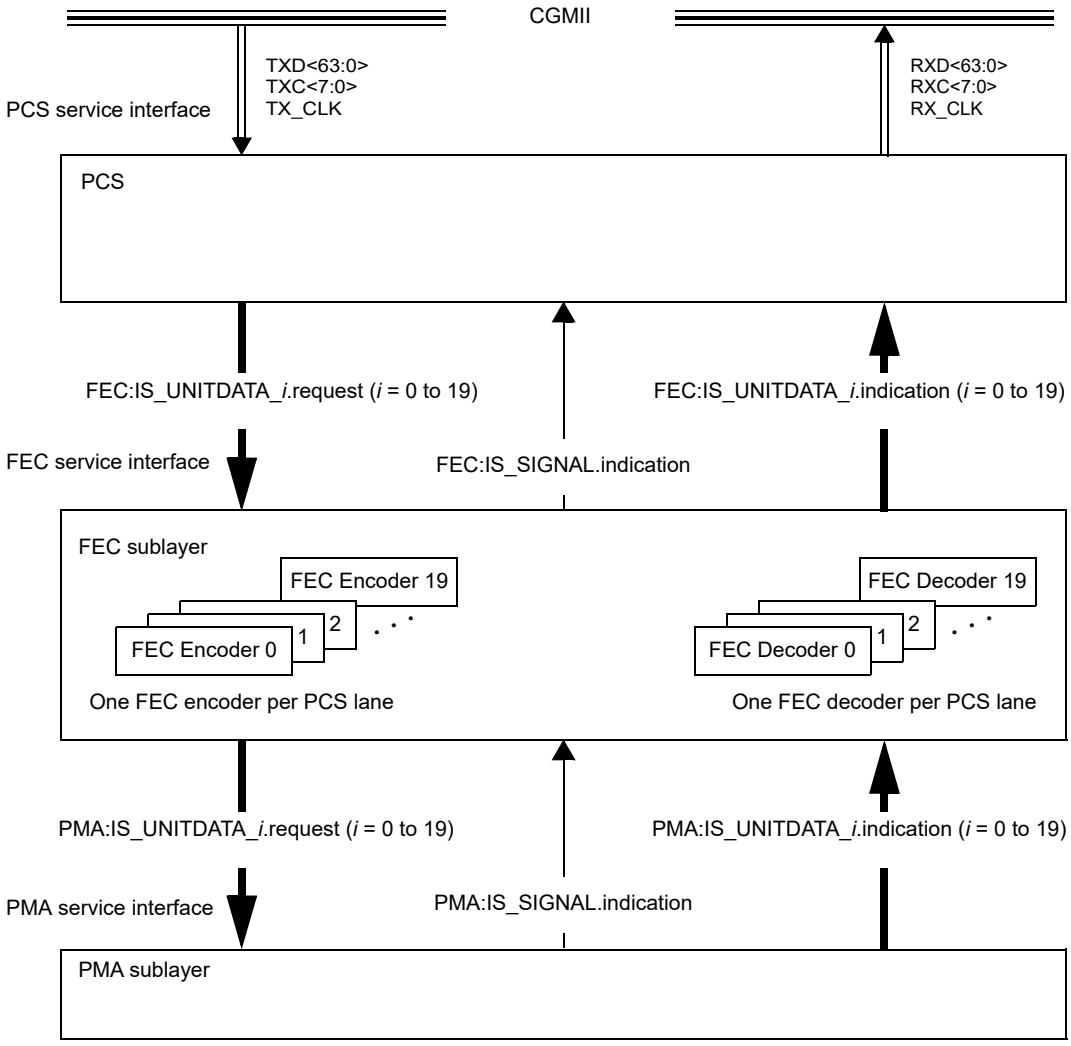

Figure 74–5—Functional block diagram for 100GBASE-R PHY

74.5 FEC service interface

The FEC service interface is provided to allow the PCS to transfer information to and from the FEC. The FEC service interface is equivalent to the PMA service interface for 10GBASE-R and an instance of the inter-sublayer service interface defined in 105.4 for 25GBASE-R, and 80.3 for 40GBASE-R and 100GBASE-R. These services are defined in an abstract manner and do not imply any particular implementation. The FEC service interface supports exchange of data units between PCS entities on either side of a link using request and indication primitives. Data units are mapped into FEC blocks by the FEC and passed to the PMA, and vice versa.

The service primitives are defined differently for 10GBASE-R, for 25GBASE-R, and for 40GBASE-R and 100GBASE-R.

Optional physical instantiations of the PMA service interface have been defined (see Clause 51, Annex 109A, Annex 109B, Annex 83A, Annex 83B, Annex 83D, and Annex 83E). There is XSBI

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(10 Gigabit Sixteen-Bit Interface) for 10GBASE-R, 25GAUI for 25GBASE-R, XLAUI for 40GBASE-R and CAUI-n for 100GBASE-R. These physical instantiations, with a PMA if required, may also be used for the FEC service interface.

74.5.1 10GBASE-R service primitives

The following primitives are defined within the FEC service interface:

a) FEC_UNITDATA.request(tx_data-group<15:0>)
b) FEC_UNITDATA.indication(rx_data-group<15:0>)
c) FEC_SIGNAL.indication(SIGNAL_OK)
d) FEC_TX_MODE.request(tx_mode)
e) FEC_RX_MODE.request(rx_mode)
f) FEC_ENERGY.indication(energy_detect)
g) FEC_LPI_ACTIVE.request(rx_lpi_active)

Items d), e), f), and g) are only required for the optional EEE capability.

The FEC service interface directly maps to the PMA service interface of the 10GBASE-R PCS defined in Clause 49. The FEC_UNITDATA.request maps to the PMA_UNITDATA.request primitive, the FEC_UNITDATA.indication maps to the PMA_UNITDATA.indication primitive, and the FEC_SIGNAL.indication maps to the PMA_SIGNAL.indication primitive of the 10GBASE-R PCS.

If the optional Energy-Efficient Ethernet (EEE) capability is supported (see Clause 78) then the interface with the PMA sublayer (or FEC sublayer) includes rx_mode and tx_mode to control power states in lower sublayers and energy_detect that indicates whether the PMD sublayer has detected a signal at the receiver.

74.5.1.1 FEC_UNITDATA.request

This primitive defines the transfer of data in the form of constant-width data units from the PCS to the FEC. The data supplied via FEC_UNITDATA.request is mapped by the FEC Transmit process into the payload capacity of the outgoing FEC block stream.

74.5.1.1.1 Semantics of the service primitive

FEC_UNITDATA.request(tx_data-group<15:0>)

The data conveyed by FEC_UNITDATA.request is a 16-bit vector representing a single data unit that has been prepared for transmission by the 10GBASE-R PCS Transmit process.

74.5.1.1.2 When generated

The 10GBASE-R PCS sends tx_data-group<15:0> to the FEC at a nominal rate of 644.53125 MHz, corresponding to the 10GBASE-R signaling rate of 10.3125 GBd.

74.5.1.1.3 Effect of receipt

Upon receipt of this primitive, the FEC Transmit process maps the data conveyed by the tx_data unit<15:0> parameter into the payload of the transmitted FEC block stream, adds FEC overhead as required, scrambles the data, and transfers the result to the PMA via the PMA_UNITDATA.request primitives.

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74.5.1.2 FEC_UNITDATA.indication

This primitive defines the transfer of received data in the form of constant-width data units from the FEC to the PCS. FEC_UNITDATA.indication is generated by the FEC Receive process in response to FEC block data received from the PMA.

74.5.1.2.1 Semantics of the service primitive

FEC_UNITDATA.indication(rx_data-group<15:0>)

The rx_data-group<15:0> parameter is a 16-bit vector that represents the data unit transferred by the FEC to the 10GBASE-R PCS.

74.5.1.2.2 When generated

The FEC sends one rx_data-group<15:0> to the 10GBASE-R PCS for each 16 bits received from the PMA sublayer. The nominal rate of generation of the FEC_UNITDATA.indication primitive is 644.53125 Mtransfers/s.

74.5.1.2.3 Effect of receipt

The effect of receipt of this primitive by the FEC client is unspecified by the FEC sublayer.

74.5.1.3 FEC_SIGNAL.indication

This primitive is sent by the FEC to the PCS to indicate the status of the Receive process. FEC_SIGNAL.indication is generated by the FEC Receive process in order to propagate the detection of severe error conditions (e.g., no valid signal being received from the PMA sublayer) to the PCS.

74.5.1.3.1 Semantics of the service primitive

FEC_SIGNAL.indication(SIGNAL_OK)

The SIGNAL_OK parameter can take one of two values: OK or FAIL. A value of OK denotes that the FEC Receive process is successfully delineating valid payload information from the incoming data stream received from the PMA sublayer indicated by the fec_signal_ok variable equal to true, and this payload information is being presented to the PCS via the FEC_UNITDATA.indication primitive. A value of FAIL denotes that errors have been detected by the Receive process indicated by the fec_signal_ok variable equal to false, that prevent valid data from being presented to the PCS, in this case the FEC_UNITDATA.indication primitive and its associated rx_data-group<15:0> parameter are meaningless.

74.5.1.3.2 When generated

The FEC generates the FEC_SIGNAL.indication primitive to the 10GBASE-R PCS whenever there is a change in the value of the SIGNAL_OK parameter and FEC block synchronization is achieved.

74.5.1.3.3 Effect of receipt

The effect of receipt of this primitive by the FEC client is unspecified by the FEC sublayer.

74.5.1.4 FEC_ENERGY.indication (optional)

FEC_ENERGY.indication(energy_detect)

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A Boolean variable that reflects the value of the energy detection primitive PMA_ENERGY.indication.

74.5.1.4.1 Effect of receipt

The effect of receipt of this primitive by the FEC client is unspecified by the FEC sublayer.

74.5.1.5 FEC_LPI_ACTIVE.request (optional)

FEC_LPI_ACTIVE.request(rx_lpi_active)

The rx_lpi_active parameter is a Boolean variable sent from the PCS that is set to TRUE when LPI mode is active at the receiver and set to FALSE otherwise.

74.5.1.5.1 When generated

The generation of this primitive by the FEC client is unspecified by the FEC sublayer.

74.5.1.5.2 Effect of receipt

When rx_lpi_active is TRUE, rapid block lock as specified in 74.7.4.8 will be used to quickly determine the start of the FEC block during EEE REFRESH or WAKE. When rx_lpi_active is FALSE, rapid block lock will not be used.

74.5.1.6 FEC_RX_MODE.request (optional)

FEC_RX_MODE.request(rx_mode)

The rx_mode parameter is a variable sent from the PCS. It is set to QUIET while the receiver is in the RX_QUIET state and is set to DATA otherwise.

74.5.1.6.1 When generated

The generation of this primitive by the FEC client is unspecified by the FEC sublayer.

74.5.1.6.2 Effect of receipt

When rx_mode is QUIET, the FEC decoder logic may deactivate functional blocks to conserve energy. When rx_mode is DATA, the FEC decoder logic operates normally. The value rx_mode is passed to the client layer through PMA_RX_MODE(rx_mode).request.

74.5.1.7 FEC_TX_MODE.request (optional)

FEC_TX_MODE.request(tx_mode)

The tx_mode parameter is a variable sent from the PCS. It is set to QUIET while the transmitter is in the TX_QUIET state, it is set to ALERT while the transmitter is in the TX_ALERT state and is set to DATA otherwise.

74.5.1.7.1 When generated

The generation of this primitive by the FEC client is unspecified by the FEC sublayer.

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74.5.1.7.2 Effect of receipt

When tx_mode is QUIET or ALERT, the FEC encoder logic may deactivate functional blocks to conserve energy. When tx_mode is DATA, the FEC encoder logic operates normally. The value tx_mode is passed to the client layer through PMA_TX_MODE(tx_mode).request.

74.5.2 25GBASE-R service primitives

The FEC service interface for 25GBASE-R is an instance of the inter-sublayer service interface defined in 105.4. The FEC service interface primitives are summarized as follows:

a) FEC:IS_UNITDATA.request
b) FEC:IS_UNITDATA.indication
c) FEC:IS_SIGNAL.indication
d) FEC:IS_TX_MODE.request(tx_mode)
e) FEC:IS_RX_MODE.request(rx_mode)
f) FEC:IS_RX_TX_MODE.indication(rx_tx_mode)
g) FEC:IS_LPI_ACTIVE.request(rx_lpi_active)
h) FEC:IS_ENERGY.indication(energy_detect)

Items d), e), f), g), and h) are only required for the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode.

The 25GBASE-R PCS (or PMA) continuously sends bit streams to the FEC via the tx_bit parameter of the FEC:IS_UNITDATA.request at a nominal signaling rate of 25.78125 GBd.

The FEC continuously sends bit streams to the 25GBASE-R PCS (or PMA) via the rx_bit parameter of the FEC:IS_UNITDATA.indication at a nominal signaling rate of 25.78125 GBd.

The SIGNAL_OK parameter of the FEC:IS_SIGNAL.indication primitive can take one of two values: OK or FAIL. A value of OK denotes that the FEC Receive process is successfully delineating valid payload information from the incoming data stream received from the PMA sublayer indicated by the fec_signal_ok variable equal to true, and this payload information is being presented to the PCS (or PMA) via the FEC:IS_UNITDATA.indication primitive. A value of FAIL denotes that errors have been detected by the Receive process indicated by the fec_signal_ok variable equal to false that prevent valid data from being presented to the PCS, in this case the rx_bit parameter of the FEC:IS_UNITDATA.indication primitive is undefined.

FEC:IS_TX_MODE.request is sourced from the PCS and passed through the FEC to the PMA sublayer. The tx_mode parameter can take the values QUIET, ALERT, or DATA. When tx_mode is QUIET or ALERT, the FEC encoder logic may deactivate functional blocks to conserve energy. When tx_mode is DATA, the FEC encoder logic operates normally.

FEC:IS_RX_MODE.request is sourced from the PCS and passed through the FEC to the PMA sublayer. The rx_mode parameter can take the values QUIET or DATA. When rx_mode is QUIET, the FEC decoder logic may deactivate functional blocks to conserve energy. When rx_mode is DATA, the FEC decoder logic operates normally.

FEC:IS_RX_TX_MODE.indication communicates the rx_tx_mode parameter to a PMA client layer if present. This parameter indicates the value of tx_mode that the PMA sublayer has inferred from the received signal. Without EEE deep sleep capability, the primitive is never generated and the sublayer behaves as if rx_tx_mode = DATA. The parameter rx_tx_mode is assigned one of the following values: DATA, QUIET, or ALERT.

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The rx_lpi_active parameter in FEC:IS_LPI_ACTIVE.request is a Boolean variable sent from the PCS that is set to TRUE when LPI mode is active at the receiver and set to FALSE otherwise. When TRUE, rx_lpi_active causes rapid FEC block lock as specified in 74.7.4.8 to be used to quickly determine the start of the FEC block during EEE REFRESH or WAKE.

The energy_detect parameter in FEC:IS_ENERGY.indication is a Boolean variable that indicates to the PCS that energy has been detected at the PMD. This signal is passed up through the FEC from the PMA sublayer to the PCS. It has no effect on FEC operation.

74.5.3 40GBASE-R and 100GBASE-R service primitives

The FEC service interface for 40GBASE-R and 100GBASE-R is an instance of the inter-sublayer service interface defined in 80.3. The FEC service interface primitives are summarized as follows:

a) FEC:IS_UNITDATA_*i*.request
b) FEC:IS_UNITDATA_*i*.indication
c) FEC:IS_SIGNAL.indication
d) FEC_TX_MODE.request(tx_mode)
e) FEC_RX_MODE.request(rx_mode)
f) FEC_RX_TX_MODE.indication(rx_tx_mode)
g) FEC_LPI_ACTIVE.request(rx_lpi_active)
h) FEC_ENERGY.indication(energy_detect)

Items d), e), f), g), and h) are only required for the optional EEE capability.

The 40GBASE-R FEC has four parallel bit streams, hence $i = 0$ to 3 for 40GBASE-R and the 100GBASE-R FEC has twenty parallel bit streams, hence $i = 0$ to 19 for 100GBASE-R.

The PCS (or PMA) continuously sends four or twenty parallel bit streams to the FEC, one per PCS lane, each at a nominal signaling rate of 10.3125 GBd for 40GBASE-R and 5.15625 GBd for 100GBASE-R.

This FEC:IS_SIGNAL.indication primitive is sent by the FEC to the PCS (or PMA) to indicate the status of the Receive process. FEC:IS_SIGNAL.indication is generated by the FEC Receive process in order to propagate the detection of severe error conditions (e.g., no valid signal being received from the PMA sublayer) to the PCS (or PMA).

The SIGNAL_OK parameter in FEC:IS_SIGNAL.indication can take one of two values: OK or FAIL. A value of OK denotes that the FEC Receive process is successfully delineating valid payload information from all of the incoming data streams received from the PMA sublayer indicated by the fec_signal_ok variable equal to true, for all data streams, and this payload information is being presented to the PCS (or PMA) via the FEC:IS_UNITDATA_*i*.indication primitive. A value of FAIL denotes that errors have been detected by the Receive process indicated by the fec_signal_ok variable equal to false, in any of the data streams, that prevent valid data from being presented to the PCS (or PMA), in this case the FEC:IS_UNITDATA_*i*.indication primitive is a direct pass through of the PMA:IS_UNITDATA_*i*.indication from the PMA.

If the optional Energy-Efficient Ethernet (EEE) capability is supported (see Clause 78) then the interface with the PMA sublayer (or FEC sublayer) includes rx_mode and tx_mode to control power states in lower sublayers and energy_detect that indicates whether the PMD sublayer has detected a signal at the receiver. If the optional EEE deep sleep capability is supported, rx_tx_mode is passed through the FEC but is not used by it.

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The tx_mode parameter in FEC_TX_MODE.request is sent from the PCS. It is set to QUIET while the transmitter is in the TX_QUIET state, it is set to ALERT while the transmitter is in the TX_ALERT state, and is set to DATA otherwise.

The rx_mode parameter in FEC_RX_MODE.request is sent from the PCS. It is set to QUIET while the receiver is in the RX_QUIET state and is set to DATA otherwise.

The FEC_RX_TX_MODE.indication primitive communicates the rx_tx_mode parameter. This parameter indicates the value of tx_mode that the PMA sublayer has inferred from the received signal. Without EEE deep sleep capability, the primitive is never generated and the sublayer behaves as if rx_tx_mode=DATA. The parameter rx_tx_mode is assigned one of the following values: DATA, QUIET, or ALERT.

The rx_lpi_active parameter in FEC_LPI_ACTIVE.request is a Boolean variable sent from the PCS that is set to TRUE when LPI mode is active at the receiver and set to FALSE otherwise.

The energy_detect parameter in FEC_ENERGY.indication is a Boolean variable that indicates to the PCS that energy has been detected at the PMD.

74.6 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The maximum delay contributed by the 10GBASE-R FEC (sum of transmit and receive delays at one end of the link) shall be no more than 6144 BT (or 12 pause_quanta or 614.4 ns).

The maximum delay contributed by the 25GBASE-R FEC (sum of transmit and receive delays at one end of the link) shall be no more than 6144 BT (or 12 pause quanta or 245.76 ns).

The maximum delay contributed by the 40GBASE-R FEC (sum of transmit and receive delays at one end of the link) shall be no more than 24576 BT (or 48 pause_quanta or 614.4 ns).

The maximum delay contributed by the 100GBASE-R FEC (sum of transmit and receive delays at one end of the link) shall be no more than 122880 BT (or 240 pause_quanta or 1228.8 ns).

A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 80.4 and its references.

74.7 FEC principle of operation

On transmission, the FEC sublayer receives data from the PCS, transcodes 64B/66B words, performs the FEC coding/framing, scrambles and sends the data to the PMA. On reception, the FEC sublayer receives data from the PMA, performs descrambling, achieves FEC framing synchronization, decodes the FEC code, correcting data where necessary and possible, re-codes 64B/66B words, and sends the data to the PCS.

74.7.1 FEC code

The FEC code used is a shortened cyclic code (2112, 2080) for error checking and forward error correction. The FEC block length is 2112 bits. The code encodes 2080 bits of payload (or information symbols) and adds 32 bits of overhead (or parity symbols). The code is systematic—meaning that the information symbols

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are not disturbed in anyway in the encoder and the parity symbols are added separately to the end of each block.

The (2112,2080) code is constructed by shortening the cyclic code (42987, 42955). The shortened cyclic code (2112,2080) is guaranteed to correct an error burst of up to 11 bits per block. It is a systematic code that is well suited for correction of the burst errors typical in a backplane channel (see 69.3) resulting from error propagation in the receive equalizer.

See Blahut [B16] and Lin and Costello [B52] for additional information on cyclic codes and shortened cyclic codes for correcting burst errors.

74.7.2 FEC block format

The format of the FEC block is shown in Table 74–1. The length of the FEC block is 2112 bits. Each FEC block contains 32 rows of 65 bits each; 64 bits of payload and 1 bit transcoding overhead (T bits). At the end of each block there is 32-bit overhead or parity check bits. Transmission is from left to right within each row and from top to bottom between rows. The payload bits carry the information symbols from the PCS layer.

Table 74–1—FEC block format

T_0	64 bit payload Word 0	T_1	64 bit payload Word 1	T_2	64 bit payload Word 2	T_3	64 bit payload Word 3
T_4	64 bit payload Word 4	T_5	64 bit payload Word 5	T_6	64 bit payload Word 6	T_7	64 bit payload Word 7
T_8	64 bit payload Word 8	T_9	64 bit payload Word 9	T_{10}	64 bit payload Word 10	T_{11}	64 bit payload Word 11
T_{12}	64 bit payload Word 12	T_{13}	64 bit payload Word 13	T_{14}	64 bit payload Word 14	T_{15}	64 bit payload Word 15
T_{16}	64 bit payload Word 16	T_{17}	64 bit payload Word 17	T_{18}	64 bit payload Word 18	T_{19}	64 bit payload Word 19
T_{20}	64 bit payload Word 20	T_{21}	64 bit payload Word 21	T_{22}	64 bit payload Word 22	T_{23}	64 bit payload Word 23
T_{24}	64 bit payload Word 24	T_{25}	64 bit payload Word 25	T_{26}	64 bit payload Word 26	T_{27}	64 bit payload Word 27
T_{28}	64 bit payload Word 28	T_{29}	64 bit payload Word 29	T_{30}	64 bit payload Word 30	T_{31}	64 bit payload Word 31
32 parity bits							

Total FEC block length = (32 × 65) + 32 = 2112 bits

74.7.3 Composition of the FEC block

The FEC sublayer does not decrease the symbol rate of the PCS, nor does it increase the signaling rate of the PMD sublayer. Instead, the FEC sublayer compresses the sync bits from the 64B/66B encoded data provided by the PCS to accommodate the addition of 32 parity check bits for every block of 2080 bits.

The BASE-R 64B/66B PCS maps 64 bits of scrambled payload and 2 bits of unscrambled sync header into 66-bit encoded blocks. The 2-bit sync header allows establishment of 64B/66B block boundaries by the PCS sync process. The sync header is 01 for data blocks and 10 for control blocks; the sync header is the only

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position in the PCS block that always contain a transition and this feature of the code is used to establish 64B/66B block boundaries.

The FEC sublayer compresses the 2 bits of the sync header to 1 transcode bit. The transcode bit carries the state of BASE-R sync bits for the associated payload. This is achieved by eliminating the first bit in 64B/66B block, which is also the first sync bit, and preserving the second bit. The value of the second bit defines the value of the removed first bit uniquely, since it is always an inversion of the first bit. The transcode bits are further scrambled (as explained in 74.7.4.2) to ensure DC balance.

The 32 sequential 64B/66B blocks are transcoded in this fashion, and then 32 bits of FEC parity are computed for them. The 32 transcoded words and the 32 FEC parity bits constitute an FEC block.

The error detection property of the FEC cyclic code is used to establish block synchronization at FEC block boundaries at the receiver. If decoding passes successfully, the FEC decoder produces 32 65-bit words, the first decoded bit of each word being the transcode bit. Then the first sync bit in 64B/66B code is constructed by the inversion of the transcode bit, and the value of the second sync bit is equal to the transcode bit.

74.7.4 Functions within FEC sublayer

The FEC sublayer comprises four functional blocks; FEC Encoder, Reverse Gearbox function, FEC decoder, and FEC block synchronization.

74.7.4.1 Reverse gearbox function

74.7.4.1.1 Reverse gearbox function for 10GBASE-R

The reverse gearbox function adapts between the 66-bit width of the 64B/66B blocks and the 16-bit width of the PCS interface. It receives the 16-bit stream from the PCS interface and converts them back to 66-bit encoded blocks for the FEC Encoder to process. The reverse gearbox function operates in the same manner as the block sync function defined in 49.2.9.

The reverse gearbox function receives data via 16-bit FEC_UNITDATA.request primitive. It will form a bit stream from the primitives by concatenating requests with the bits of each primitive in order to form tx_data-group<0> to tx_data-group<15> (see Figure 49–6). It obtains lock to the 66-bit blocks in the bit stream using the sync headers and outputs 66-bit blocks. Lock is obtained as specified in the block lock state diagram shown in Figure 49–14.

NOTE—Figure 49–6 shows rx_data-group<0> to rx_data-group<15> because the processing depicted in that figure is in the receive function. However, the reverse gearbox in this subclause is part of the transmit function, so it uses tx_-data-group<0> to tx_data-group<15>.

The reverse gearbox functionality is necessary only when the optional PMA compatibility interface named XSBI is implemented between the PCS and FEC functions, since that interface passes data via a 16-bit wide path. When the XSBI is not implemented, the internal data-path width between the PCS and FEC is an implementation choice. Depending on the path width, the reverse gearbox function may not be necessary.

74.7.4.1.2 Reverse gearbox function for 25GBASE-R, 40GBASE-R, and 100GBASE-R

The reverse gearbox function adapts between the 66-bit width of the 64B/66B blocks and the 1-bit wide lane of the 25GBASE-R, 40GBASE-R, or 100GBASE-R PCS to FEC interface (or PMA to FEC interface). It receives the 1-bit stream from the FEC service interface (or PMA service interface) and converts it back to 66-bit encoded blocks for the FEC Encoder to process. The reverse gearbox function, if implemented, shall operate in the same manner as the lane block sync function defined in 82.2.12.

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The reverse gearbox function receives data via the 25GBASE-R FEC:IS_UNITDATA.request primitive (or via the PMA:IS_UNITDATA.request primitive) or via the 40GBASE-R and 100GBASE-R FEC:IS_UNITDATA_*i*.request primitive see 74.5.3 (or via the PMA:IS_UNITDATA_*i*.request primitive). It obtains lock to the 66-bit blocks in each bit stream using the sync headers and outputs 66-bit blocks to the FEC encoder function (see 74.7.4.4). PCS lane lock is obtained as specified in the PCS lane lock state diagram shown in Figure 82–12.

The internal data-path width from the PCS or PMA is an implementation choice. Depending on the path width, the reverse gearbox function may not be necessary.

74.7.4.2 FEC Encoder

The FEC encoder connects to the reverse gearbox function using the 66-bit wide data path. The FEC encoder takes 32 × 64B/66B blocks from the reverse gearbox and encodes it into a single FEC block of 2112 bits. The FEC Encoder compresses the two sync bits to one transcode bit as explained in 74.7.3. The transcode bit is then XOR'ed with data bit 8 of the corresponding 64B/66B block. The resulting 32 × 65b = 2080 bits with the block format as shown in Table 74–1 are fed to the (2112,2080) encoder, which produces 32 parity-check bits. The parity check bits are appended to the end of the FEC block. The FEC block is scrambled using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1. and sent to the PMA interface.

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74.7.4.3 FEC transmission bit ordering

The format of the FEC block and the transmit bit ordering is shown in Figure 74–6.

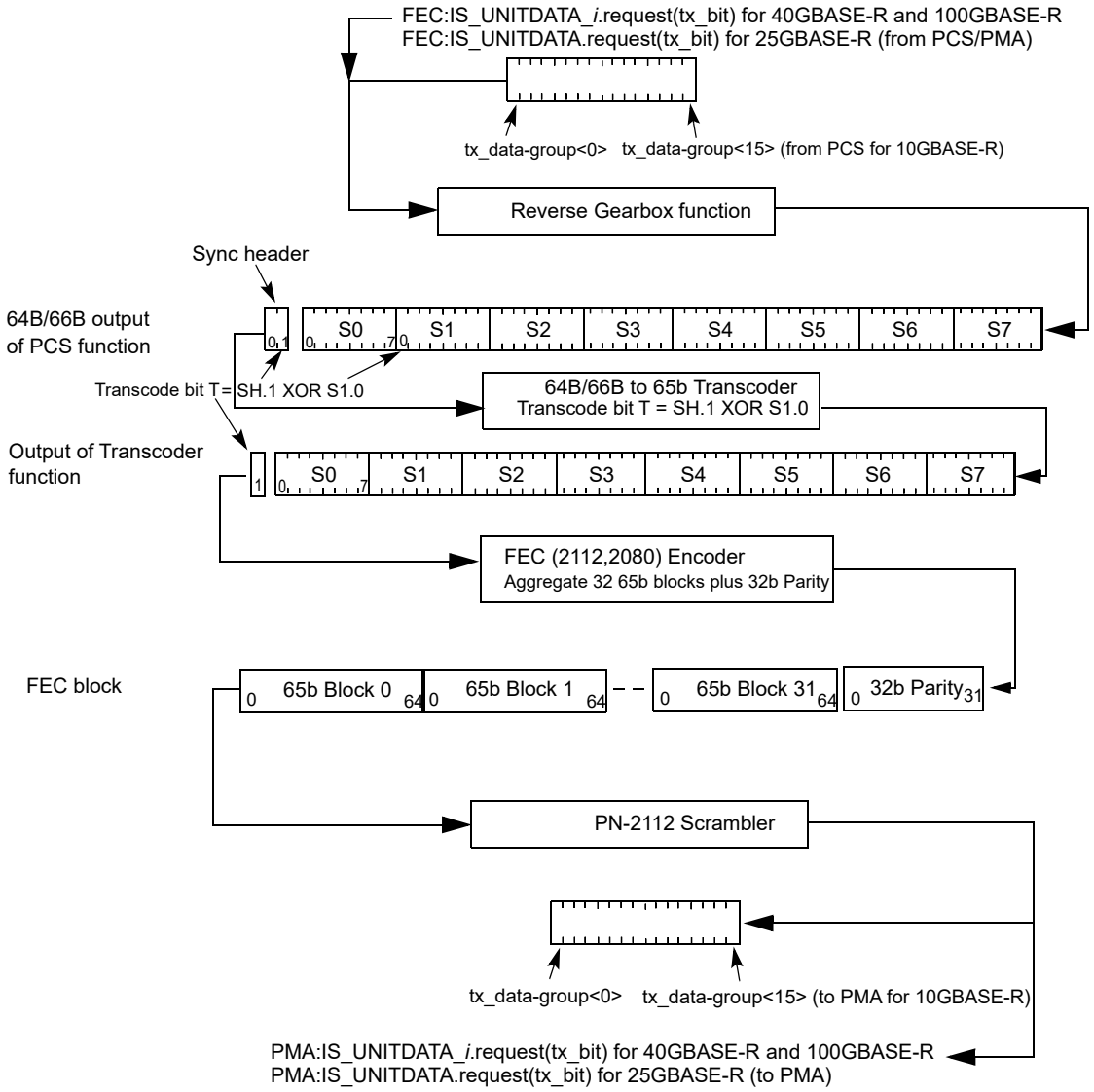

Figure 74–6—FEC Transmit bit ordering

74.7.4.4 FEC (2112,2080) encoder

The block diagram of the FEC Encoder is illustrated in Figure 74–7. The 32 × 65-bit payload blocks are encoded by the (2112, 2080) code. This code is a shortened cyclic code that can be encoded by generator polynomial $g(x)$. The FEC block is scrambled using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1.

The generator polynomial $g(x)$ for the (2112, 2080) parity-check bits is defined as given in Equation (74–1).

$$g(x) = x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1 \quad (74–1)$$

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If the polynomial representation of information bits is $m(x)$, the codeword $c(x)$ can be calculated in systematic form as given in Equation (74–2) and Equation (74–3).

$$p(x) = x^{32}m(x) \bmod g(x) \tag{74–2}$$

$$c(x) = p(x) + x^{32}m(x) \tag{74–3}$$

(Multiplication by x^{32} is performed using shifts).

Systematic form of the codeword means that first 2080 bits of the codeword are information bits that can be extracted directly.

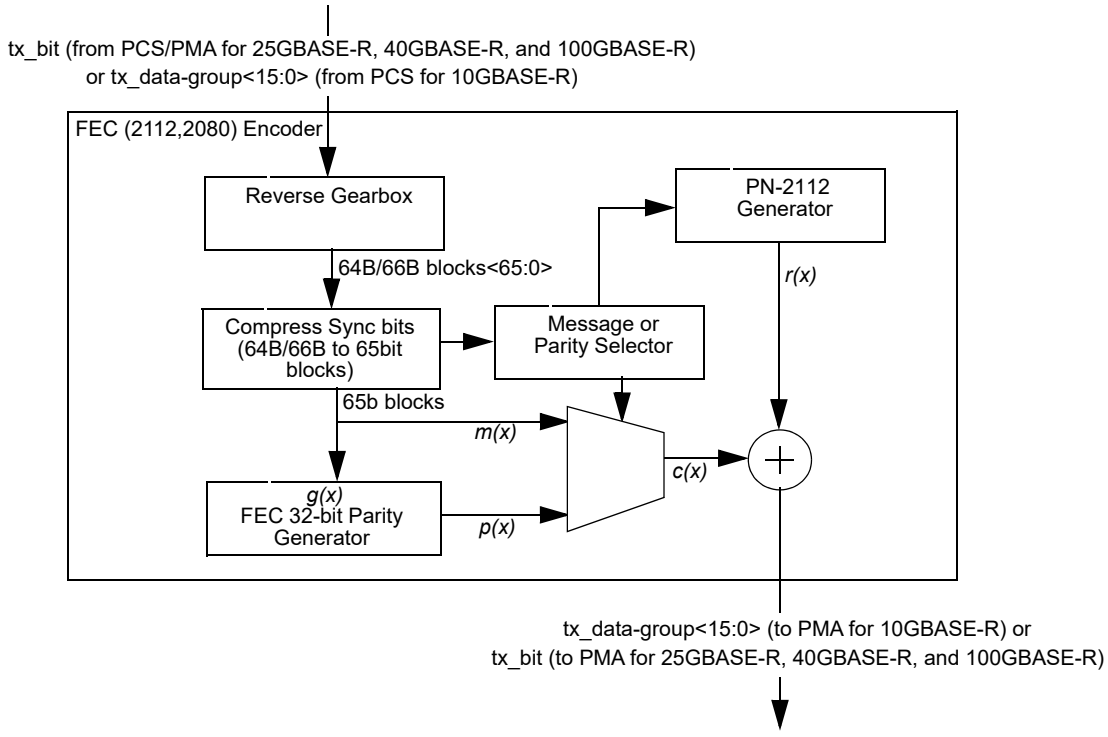

Figure 74–7—FEC (2112,2080) encoding

74.7.4.4.1 PN-2112 pseudo-noise sequence generator

PN-2112 is a pseudo-noise sequence of length 2112 generated by the polynomial *r(x)*, which is equal to the scrambler polynomial defined in 49.2.6 with initial state S57 = 1, Si–1 = Si XOR 1 or simply the binary sequence of 101010…. . Before each FEC block processing (encoding or decoding) the PN-2112 generator is initialized with this state. The PN-2112 generator shall produce the same result as the implementation shown in Figure 74–8. This implements the PN-2112 generator polynomial given in Equation (74–4).

$$r(x) = 1 + x^{39} + x^{58} \tag{74–4}$$

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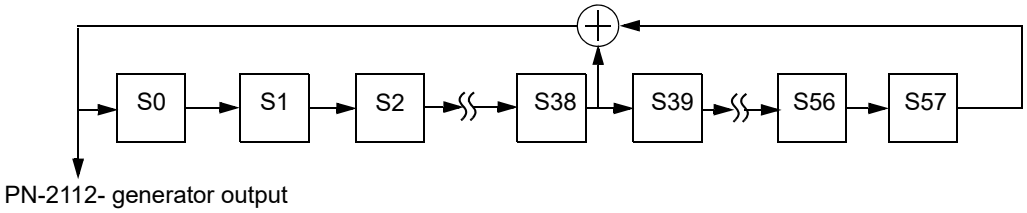

Figure 74–8—PN-2112 generator

Scrambling with the PN-2112 sequence at the FEC codeword boundary is necessary for establishing FEC block synchronization (to ensure that any shifted input bit sequence is not equal to another FEC codeword) and to ensure DC balance.

74.7.4.5 FEC decoder

The FEC decoder establishes FEC block synchronization based on repeated decoding of the received sequence. Decoding and error correction is performed after FEC synchronization is achieved. There is an option for the FEC decoder to indicate any decoding errors to the upper layer.

The FEC decoder recovers and extracts the information bits using the parity-check data. In case of successful decoding the decoder restores the sync bits in each of the 64B/66B blocks sent to the PCS function, by first performing an XOR operation of the received transcode bit with the associated data bit 8 and then generating the two sync bits.

When the decoder for 10GBASE-R or 25GBASE-R is configured to indicate decoding error, the decoder indicates error to the PCS by means of setting both sync bits to the value 11 in the 1st, 9th, 17th, 25th, and 32nd of the 32 decoded 64B/66B blocks from the corresponding errored FEC block, thus forcing the PCS sublayer to consider this block as invalid.

When the decoder for 40GBASE-R or 100GBASE-R is configured to indicate decoding error, the decoder needs to mark errors in more of the 64B/66B blocks to ensure that detected errors are signaled to the MAC for every frame containing an error. The FEC sublayers for 40GBASE-R and 100GBASE-R set both sync bits to the value 11 in all thirty-two 64B/66B blocks to indicate error to the PCS.

The FEC Synchronization process continuously monitors PMA_SIGNAL.indication(SIGNAL_OK) or PMA:IS_SIGNAL.indication(SIGNAL_OK). When SIGNAL_OK indicates OK, the FEC Synchronization process accepts data units via the PMA_UNITDATA.indication primitive or the PMA:IS_UNITDATA_*i*.indication primitives. It attains block synchronization based on the decoding of FEC blocks and conveys received 64B/66B blocks to the PCS Receive process. The FEC Synchronization process sets the sync_status flag to the PCS function to indicate whether the FEC has obtained synchronization.

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74.7.4.5.1 FEC (2112,2080) decoding

The FEC decoding function block diagram is shown in Figure 74–9. The decoder processes the 16-bit rx_data-group stream received from the PMA sublayer and descrambles the data using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1.

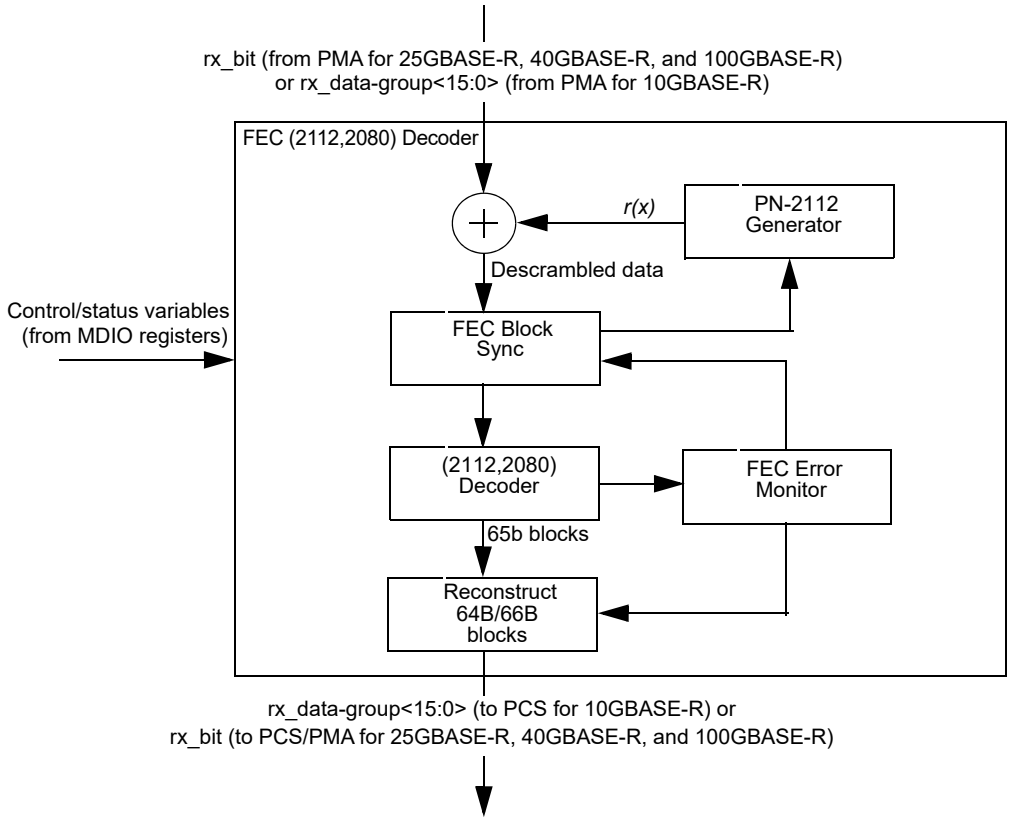

Figure 74–9—FEC (2112,2080) decoding

The synchronization of the 2112 bit FEC block is established using FEC decoding as described in 74.7.4.7. Each of the 32 65-bit data words is extracted from the recovered FEC block and the 2-bit sync is reconstructed for the 64B/66B codes from the transcode bit as shown in Figure 74–10. The FEC decoder provides an option to indicate decoding errors in the reconstructed sync bits. The sync bits {SH.0, SH.1} take the value as described in the following:

a) If decoding is successful (by either the parity match or the FEC block is correctable) and the descrambled received transcode bit (T) is 1 then the sync bits take a value of {SH.0,SH.1} = 01 or if the descrambled received transcode bit (T) is 0 then the sync bits take a value of {SH.0,SH.1} = 10.
b) If the variable FEC_Enable_Error_to_PCS is set to 1 to indicate error to PCS layer and the received FEC block has uncorrectable errors then the sync bits for the 1st, 9th, 17th, 25th, and 32nd of the 32 decoded 64B/66B blocks take a value of {SH.0,SH.1} = 11 for the 10GBASE-R and 25GBASE-R PHY. For the 40GBASE-R and 100GBASE-R PHYs, sync bits in all thirty-two 64B/66B decoded 64B/66B blocks take a value of {SH.0,SH.1} = 11. The sync bits for all other 64B/66B blocks take a value as described in item a) above.
c) If the variable FEC_Enable_Error_to_PCS is set to 0 and the received FEC block has uncorrectable errors then the sync bits take a value as described in item a) above.

This information corresponds to one complete (2112,2080) FEC block that is equal to 32 64B/66B code blocks.

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The FEC code (2112, 2080) and its performance is specified in 74.7.1. The FEC (2112,2080) decoder implementations shall be able to correct up to a minimum of 11-bit burst errors per FEC block.

74.7.4.6 FEC receive bit ordering

The format of the FEC block and the receive bit ordering is shown in Figure 74–10.

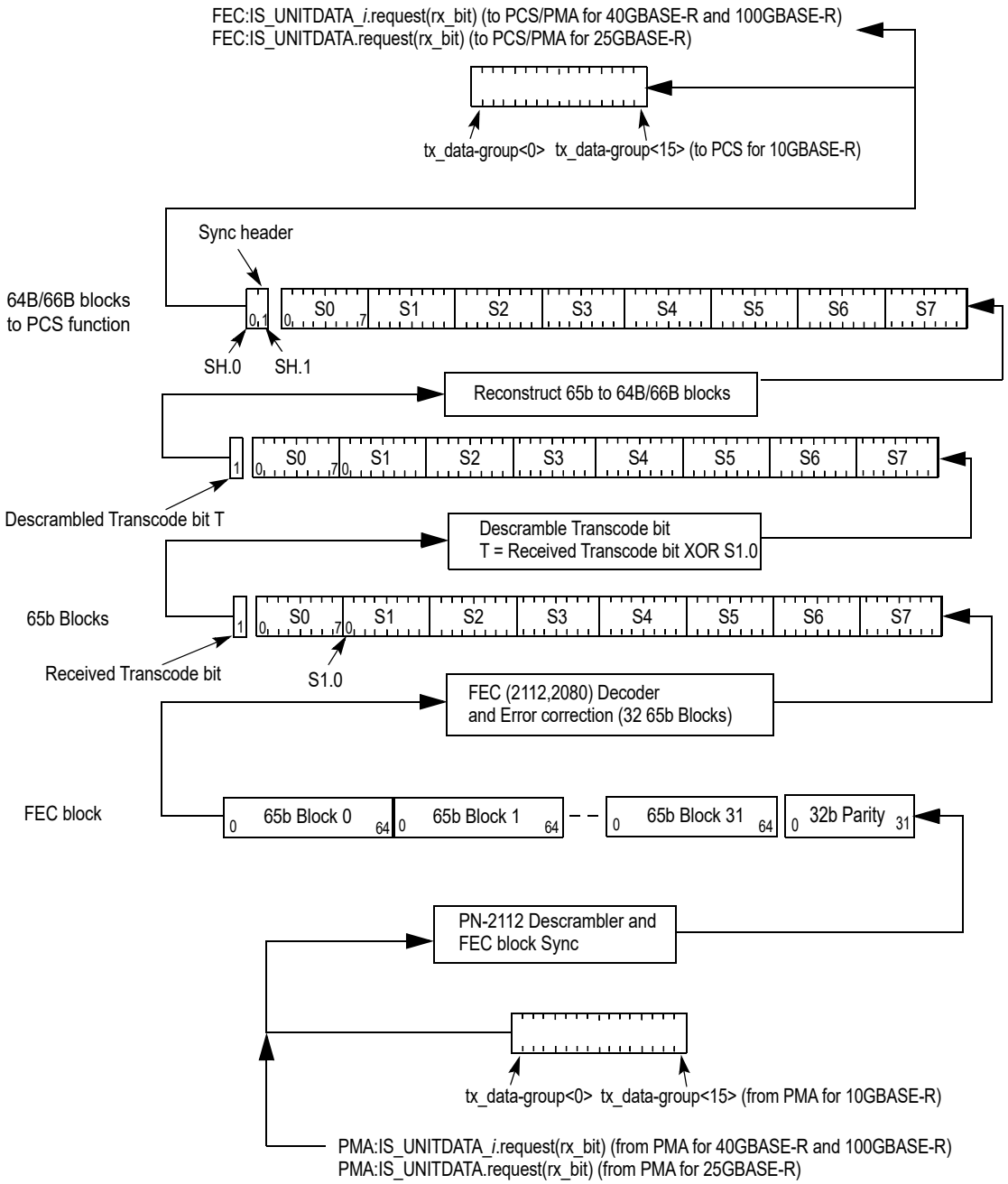

Figure 74–10—FEC Receive bit ordering

74.7.4.7 FEC block synchronization

The receive synchronization of FEC blocks is illustrated by FEC Lock state diagram in Figure 74–11.

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Receive FEC block synchronization is achieved using conventional n/m serial locking techniques as described as follows:

a) Test a potential candidate block start position
   1) Descramble block using PN-2112 Generator per 74.7.4.4.1
   2) Evaluate parity for the potential block
      i) If the parity does not match (i.e., the received parity does not match the computed parity), shift candidate start by one bit position and try again.
b) Validate potential block start position has good parity for "n" consecutive blocks
   1) If any of them fail shift candidate start one bit position and start again
   2) If "n" consecutive blocks are received with good parity, report Block Sync
c) Block Sync is established.
d) If "m" consecutive blocks are received with bad parity, drop Block Sync and restart again at item a).

The procedure is repeated at most 2111 times for all bits positions in the 2112 codeword. The values for m and n are as follows: m = 8 and n = 4.

74.7.4.8 FEC rapid block synchronization for EEE (optional)

If the optional EEE capability is supported then during the wake and refresh states the FEC decoder receives one of the two types of deterministic blocks to achieve rapid block synchronization. During these states the reverse gearbox of the remote FEC encoder is receiving unscrambled data from the PCS sublayer via 16-bit FEC_UNITDATA.request primitive.

The Clause 49 and Clause 107 PCS sublayers encode /I/ during the wake state and /LI/ during the refresh state, which produces the two types of deterministic FEC blocks.

If the optional EEE deep sleep capability is supported, then a Clause 82 PCS sublayer also encodes /I/ during the wake state and /LI/ during the refresh state, but in addition inserts Rapid Alignment Markers into each of the PCS Lanes (see 82.2.9). This causes the two types of deterministic FEC blocks to have a number of 65-bit words within the deterministic FEC block replaced with Rapid Alignment Markers, thus not matching the two deterministic patterns as shown in Table 74A–5 and Table 74A–6. The locations of the Rapid Alignment Markers within the Rapid FEC block are consistent for a given entry into the wake or refresh states, but the locations can vary for subsequent entries. This modification to the two deterministic patterns needs to be taken into account by the Rapid FEC Lock implementation.

When rx_lpi_active is TRUE and rx_mode (or rx_tx_mode if appropriate) transitions to DATA, start a hold-off timer whose duration is greater than or equal to 13.7 μs and enable the FEC Rapid block lock mechanism, which attempts to determine the FEC start of block location based on the deterministic pattern. When the rapid block lock is locked, the determined start of block location is used as the FEC lock state diagram candidate start of block location until the rapid block lock loses lock. Assuming the rapid block lock determined the correct start of block location, the FEC lock state diagram achieves lock without requiring subsequent slips. The rapid block lock mechanism is implementation dependent and outside the scope of this standard. The FEC sublayer shall hold off asserting SIGNAL_OK until one of the following two events occurs:

1) Two 65b payload blocks after the transition from deterministic FEC block to normal scrambled FEC block
2) Expiration of the hold-off timer

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74.8 FEC MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control, status, abilities/capabilities, error indication information for and about the PHY. If MDIO is implemented, it shall map MDIO variables to FEC variables as shown in Table 74–1.

Table 74–1—MDIO/FEC variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	FEC variable
BASE-R FEC ability	BASE-R FEC ability register	1.170.0	FEC_ability
BASE-R FEC Error Indication ability	BASE-R FEC ability register	1.170.1	FEC_Error_Indication_ability
FEC Enable	BASE-R FEC control register	1.171.0	FEC_Enable
FEC Enable Error Indication	BASE-R FEC control register	1.171.1	FEC_Enable_Error_to_PCS
FEC corrected blocks	Single-lane PHY BASE-R FEC corrected blocks counter register	1.172, 1.173	FEC_corrected_blocks_counter
FEC uncorrected blocks	Single-lane PHY BASE-R FEC uncorrected blocks counter register	1.174, 1.175	FEC_uncorrected_blocks_counter
FEC corrected blocks, lanes 0 through 19	BASE-R FEC corrected blocks counter register, lanes 0 through 19	1.300 through 1.339	FEC_corrected_blocks_counter_*i*
FEC uncorrected blocks, lanes 0 through 19	BASE-R FEC uncorrected blocks counter register, lanes 0 through 19	1.700 through 1.739	FEC_uncorrected_blocks_counter_*i*

74.8.1 FEC capability

Since the FEC is an optional sublayer, the FEC ability is indicated by the variable FEC_ability for each of the BASE-R PHY types. An MDIO interface or an equivalent management interface shall be provided to access the variable FEC_ability for the BASE-R PHY type. The FEC_ability variable bit is set to a one to indicate that the PHY supports FEC sublayer, it defaults to zero otherwise.

The FEC_ability variable for the BASE-R PHY is mapped to register bit 1.170.0 (refer to 45.2.1.107.1).

The FEC capability between the link partners can be negotiated using the Clause 73 Auto-Negotiation as defined in 73.6.5.

74.8.2 FEC Enable

The FEC sublayer shall have capability to enable or disable the FEC function. An MDIO interface or an equivalent management interface shall be provided to access the variable FEC_Enable for the BASE-R PHY (refer to 45.2.1.108 register bit 1.171.0). When FEC_Enable variable bit is set to a one, this enables the FEC for the BASE-R PHY. When the variable is set to zero, the FEC is disabled in the BASE-R PHY. This

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variable shall be set to zero upon execution of PHY reset. When the FEC function is disabled, the PHY shall have a mechanism to bypass the FEC Encode and Decode functions so as not to cause additional latency associated with encoding or decoding functions.

74.8.3 FEC Enable Error Indication

The FEC sublayer may have the option to enable the BASE-R FEC decoder to indicate decoding errors to the upper layers (PCS) through the sync bits for the BASE-R PHY as defined in 74.7.4.5, if this ability is supported. An MDIO interface or an equivalent management interface shall be provided to access the variable FEC_Enable_Error_to_PCS. When the variable is set to one, this enables indication of decoding errors through the sync bits to the PCS layer. When set to zero, the error indication function is disabled.

74.8.3.1 FEC Error Indication ability

The FEC error indication ability shall be indicated by the variable FEC_Error_Indication_ability. The variable is set to one to indicate that the BASE-R FEC has the ability to indicate decoding errors to the PCS layer. The variable is set to zero if this ability is not supported by the BASE-R FEC. An MDIO interface or an equivalent management interface shall be provided to access the variable FEC_Error_Indication_ability.

74.8.4 FEC Error monitoring capability

The following counters apply to FEC sublayer management and error monitoring. If an MDIO interface is provided (see Clause 45), it is accessed via that interface. If not, it is recommended that an equivalent access be provided. These counters are reset to zero upon read or upon reset of the FEC sublayer. When a counter reaches all ones, it stops counting. The counters' purpose is to help monitor the quality of the link.

These counters shall be disabled if FEC_LPI_ACTIVE.request(rx_lpi_active) is TRUE.

74.8.4.1 FEC_corrected_blocks_counter

A corrected block is an FEC block that has invalid parity, and has been corrected by the FEC decoder.

FEC_corrected_blocks_counter (for single-lane PHYs) or FEC_corrected_blocks_counter_*i* (for multi-PCS-lane PHYs, where $i = 0$ to 3 for 40 Gb/s and $i = 0$ to 19 for 100 Gb/s,) count once for each corrected FEC block processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK. These are 32-bit counters. These variables are accessed through a management interface that may be mapped to the registers defined in 45.2.1.109 (1.172, 1.173) for single-lane PHYs and 45.2.1.131 (1.300 to 1.339) for multi-lane PHYs.

74.8.4.2 FEC_uncorrected_blocks_counter

An uncorrected block is an FEC block that has invalid parity, and has not been corrected by the FEC decoder.

FEC_uncorrected_blocks_counter (for single-lane PHYs) or FEC_uncorrected_blocks_counter_*i* (for multi-PCS-lane PHYs, where $i = 0$ to 3 for 40 Gb/s and $i = 0$ to 19 for 100 Gb/s,) count once for each uncorrected FEC block processed when FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication is OK. These are 32-bit counters. These variables are accessed through a management interface that may be mapped to the registers defined in 45.2.1.110 (1.174, 1.175) for single-lane PHYs and 45.2.1.149 (1.700 to 1.739) for multi-lane PHYs.

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74.9 BASE-R PHY test-pattern mode

The 10GBASE-R PCS and the 25GBASE-R PCS provide test-pattern functionality and the PCS transmit channel and receive channel can each operate in normal mode or test-pattern mode (see 49.2.2). When the 10GBASE-R or 25GBASE-R PHY is configured for test-pattern mode, the FEC function may be disabled by setting the FEC Enable variable to zero, so the test-pattern from the PCS can be sent to the PMA service interface, bypassing the FEC Encode and Decode functions.

The Clause 82 and Clause 107 PCS can also operate in test pattern mode (see 82.2.11 and 107.2.3); however, the scrambled idle test pattern does not require bypassing FEC encode and decode.

74.10 Detailed functions and state diagrams

74.10.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

74.10.2 State variables

74.10.2.1 Constants

m
: Positive integer constant set to value 8.

n
: Positive integer constant set to value 4.

74.10.2.2 Variables

fec_block_lock
: Boolean variable that is set to true when receiver acquires FEC block delineation.

fec_block<2111:0>
: Vector containing 2112 bits of a new FEC block accumulated from the candidate start position received from the PMA and descrambled using PN-2112 as specified in 74.7.4.4.1. For each FEC block processing, the PN-2112 is returned to the initial state as described in 74.7.4.4.1.

fec_signal_ok
: Boolean variable that is set based on the most recently received value of PMA_UNITDATA.indication(SIGNAL_OK) or PMA:IS_SIGNAL.indication(SIGNAL_OK) and fec_block_lock. It is set to true if the fec_block_lock value is true and PMA_UNITDATA.indication(SIGNAL_OK) or PMA:IS_SIGNAL.indication(SIGNAL_OK) value was OK and set to false otherwise. The value is sent to the PCS layer through the primitive FEC_SIGNAL.indication or FEC:IS_SIGNAL.indication as specified in 74.5.1.3 or 74.5.3.

parity_good
: Boolean indication that is set to true if the FEC_PARITY_CHECK function returns “match” and false if the FEC_PARITY_CHECK function returns “no_match”.

parity_invalid
: Boolean indication that is set to true if the FEC_PARITY_CHECK function returns “no_match” and false if the FEC_PARITY_CHECK function returns “match”.

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reset
: Boolean variable that controls the resetting of the FEC sublayer. It is true whenever a reset is necessary, including when reset is initiated from the MDIO during power on.

signal_ok
: Boolean variable that is set based on the most recently received value of PMA_UNITDATA.indication(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done
: Boolean variable that is asserted true when the SLIP requested by the FEC Block Lock state diagram has been completed indicating that the next candidate block sync position can be tested.

test_fec_block
: Boolean variable that is set to true when a new FEC block is available for testing and false when TEST_FEC_BLOCK state is entered. A new FEC block is available for testing when the FEC Block Sync process has accumulated one FEC block from the candidate start position (fec_block<2111:0>) from the PMA to evaluate the parity of the next block.

74.10.2.3 Functions

FEC_PARITY_CHECK(fec_block<2111:0>)
: Computes parity based on the FEC generator polynomial *g(x)* on fec_block<2079:0> and compares it against the received 32-bit parity bits fec_block<2111:2080>. The FEC_PARIY_CHECK function returns “match” if the parity check matches, and returns “no_match” if the computed parity does not match the received parity.

SLIP
: Causes the next candidate FEC block sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

74.10.2.4 Counters

parity_good_cnt
: Count of the number of times the computed parity of received message bits matched the received parity.

parity_invalid_cnt
: Count of the number of times the computed parity of received message bits did not match the received parity.

74.10.3 State diagrams

The FEC sublayer shall implement the FEC Lock state diagram shown in Figure 74–11, including compliance with the associated state variables as specified in 74.10.2. The FEC Lock state diagram determines when the receiver has obtained FEC block lock on the received data stream.

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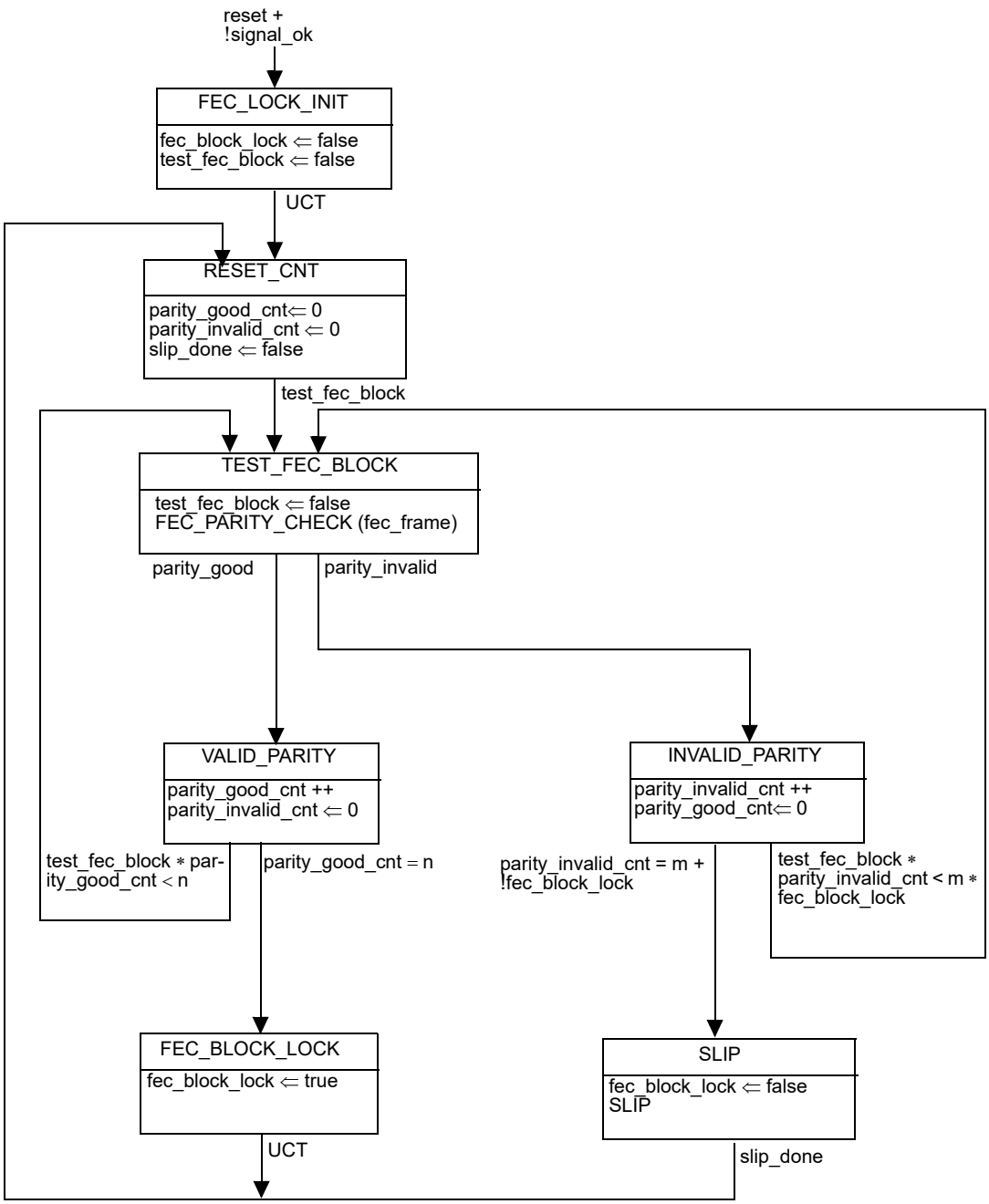

Figure 74–11—FEC Lock state diagram

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74.11 Protocol implementation conformance statement (PICS) proforma for Clause 74, forward error correction (FEC) sublayer for BASE-R PHYs[137]

74.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3, Clause 74 forward error correction (FEC) sublayer for BASE-R PHYs, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

74.11.2 Identification

74.11.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

74.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 74, forward error correction (FEC) sublayer for BASE-R PHYs
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022)	
Date of Statement	

[137] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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74.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
DC	FEC Delay Constraints	74.6	Sum of transmit and receive. No more than 12 pause_quanta for 10GBASE-R and 25GBASE-R, 48 pause_quanta for 40GBASE-R, and 240 pause_quanta for 100GBASE-R	M	Yes [ ]
*MD	MDIO Interface	45, 74.8.2, 74.8.4	Device implements MDIO registers and interface	O	Yes [ ] No [ ]
EF	FEC_Enable	74.8.2	The device has the capability to enable/disable the FEC function	M	Yes [ ]
*EIA	FEC Error Indication ability	74.8.3, 74.8.3.1	The device has ability to indicate FEC decoding errors to the PCS layer as specified in 74.8.3	O	Yes [ ] No [ ]
BF	Bypass FEC function	74.8.2	The device has mechanism to bypass FEC encode/decode functions to reduce latency	M	Yes [ ]
EEE	Rapid Block Lock	74.7.4.8	Device implements Rapid block lock mechanism to support EEE	O	Yes[]/No []
*XSBI	PMA compatibility interface XSBI	51, 74.7.4.1	Optional PMA compatibility interface named XSBI is implemented between the PCS and FEC functions	O	Yes [ ] No [ ]

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74.11.4 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Equivalent management interface is provided	74.8.2		!MD:M	N/A [ ] Yes [ ]
M2	Default value for FEC_Enable	74.8.2	FEC_Enable variable is set to zero upon execution of PHY reset	M	Yes [ ]
M3	MDIO register Mapping	74.8	If MDIO is implemented, the FEC variables and capabilities are mapped to the appropriate registers found in Table 74–1	MD:M	N/A [ ] Yes [ ]
M4	FEC_Error_Indication_ability variable access	74.8.3.1	An MDIO or equivalent managment interface is provided to access this variable	M	Yes [ ]
M5	FEC_Enable_Error_to_PCS variable access	74.8.3	An MDIO or equivalent managment interface is provided to access this variable	EIA:M	N/A [ ] Yes [ ]
M6	FEC_Enable variable access	74.8.2	An MDIO or equivalent managment interface is provided to access this variable	M	Yes [ ]
M7	FEC_ability variable access	74.8.1	An MDIO or equivalent managment interface is provided to access this variable	M	Yes [ ]

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74.11.5 FEC requirements

Item	Feature	Subclause	Value/Comment	Status	Support
FE1	FEC coding	74.7.1	The FEC code used is a shortened cyclic code (2112, 2080) for error checking and forward error correction	M	Yes [ ]
FE2	FEC block format	74.7.2	Meets the requirements of 74.7.2	M	Yes [ ]
FE3	Reverse gearbox function for 10GBASE-R	74.7.4.1.1	Reverse gearbox function implemented	XSBI:M	N/A[ ] Yes [ ]
FE4	Reverse gearbox function for 25GBASE-R, 40GBASE-R, and 100GBASE-R	74.7.4.1.2	Reverse gearbox function meets the requirements of 82.2.12	O	Yes [ ] No [ ]
FE5	FEC transmission bit ordering	74.7.4.3	Implements FEC transmission bit ordering as specified in 74.7.4.3	M	Yes [ ]
FE6	FEC encoder	74.7.4.4	Meets FEC encoder requirements of 74.7.4.4	M	Yes [ ]
FE7	PN-2112 generator	74.7.4.4.1	PN-2112 generator produces the same result as the implementation shown in Figure 74–8	M	Yes [ ]
FE8	PN-2112 Scrambler	74.7.4.4.1	Meets PN-2112 scrambler requirements of 74.7.4.4.1	M	Yes [ ]
FE9	PN-2112 descrambler	74.7.4.5.1	Meets PN-2112 descrambler requirements of 74.7.4.5.1	M	Yes [ ]
FE10	FEC decoding	74.7.4.5	Meets FEC decoder requirements of 74.7.4.5	M	Yes [ ]
FE11	FEC decoder error correction capability	74.7.4.5	The FEC decoder implementation is able to correct up to a minimum of 11 bit burst errors per FEC block as specified in 74.7.4.5.1	M	Yes [ ]
FE12	Indication of decoding errors	74.7.4.5, 74.7.4.5.1, 74.8.3	Device implements indication of decoding errors to PCS layer	EIA:M	N/A[ ] Yes [ ]
FE13	FEC block sync	74.7.4.7	Meets FEC block sync requirements as specified in 74.7.4.7	M	Yes [ ]
FE14	FEC Enable Error Indication	74.8.3	Enable FEC decoder to indicate decoding errors to PCS layer	EIA:M	N/A[ ] Yes [ ]
FE15	SLIP function	74.10.2.3	All possible bit positions can be evaluated	M	Yes [ ]
FE16	FEC Lock function	74.10.3	The FEC lock function meets the requirements of the state diagram in 74.10.3	M	Yes [ ]

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74.11.6 FEC Error Monitoring

Item	Feature	Subclause	Value/Comment	Status	Support
FEM1	FEC Error Monitoring	74.8.4	Meets FEC error monitoring capability requirements of 74.8.4	M	Yes [ ]
FEM2	FEC_corrected_blocks_counter	74.8.4.1	Meets 32-bit FEC corrected blocks counter requirements of 74.8.4.1	M	Yes [ ]
FEM3	FEC_uncorrected_blocks_counter	74.8.4.2	Meets 32-bit FEC uncorrected blocks counter requirements of 74.8.4.2	M	Yes [ ]
FEM4	FEC Error Monitoring during EEE	74.8.4	Disables FEC Error Monitoring during EEE as specified in 74.8.4	EEE:M	Yes[]

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75. Physical Medium Dependent (PMD) sublayer and medium for passive optical networks, type 10GBASE–PR and 10/1GBASE–PRX

75.1 Overview

Clause 75 describes Physical Medium dependent (PMD) sublayer for Ethernet Passive Optical Networks operating at the line rate of 10.3125 GBd in either downstream or in both downstream and upstream directions.

75.1.1 Terminology and conventions

The following list contains references to terminology and conventions used in Clause 75:

Basic terminology and conventions, see 1.1 and 1.2.

Normative references, see 1.3.

Definitions, see 1.4

Abbreviations, see 1.5.

Informative references, see Annex A.

Introduction to 1000 Mb/s baseband networks, see Clause 34.

Introduction to 10 Gb/s baseband network, see Clause 44.

Introduction to Ethernet for subscriber access networks, see Clause 56.

EPONs operate over a point-to-multipoint (P2MP) topology, also called a tree or trunk-and-branch topology. The device connected at the root of the tree is called an Optical Line Terminal (OLT) and the devices connected as the leaves are referred to as Optical network Units (ONUs). The direction of transmission from the OLT to the ONUs is referred to as the *downstream* direction, while the direction of transmission from the ONUs to the OLT is referred to as the *upstream* direction.

75.1.2 Goals and objectives

The following are the PMD objectives fulfilled by Clause 75:

a) Support subscriber access networks using point-to-multipoint topologies on optical fiber.
b) Provide Physical Layer specifications:
   1) PHY for PON, 10 Gb/s downstream / 1 Gb/s upstream, on a single SMF
   2) PHY for PON, 10 Gb/s downstream / 10 Gb/s upstream, on a single SMF
c) PHY(s) to have a BER better than or equal to 10^{-12} at the PHY service interface.
d) Define up to four optical power budgets that support split ratios of at least 1:16, 1:32, and 1:64, and distances of at least 10 km and 20 km.

75.1.3 Power budget classes

To support the above-stated objectives, Clause 75 defines the following four power budget classes:

— *Low power budget class* supports P2MP media channel insertion loss of ≤ 20 dB e.g., a PON with the split ratio of at least 1:16 and the distance of at least 10 km.
— *Medium power budget class* supports P2MP media channel insertion loss of ≤ 24 dB e.g., a PON with the split ratio of at least 1:16 and the distance of at least 20 km or a PON with the split ratio of at least 1:32 and the distance of at least 10 km.

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— *High power budget class* supports P2MP media channel insertion loss of ≤ 29 dB e.g., a PON with the split ratio of at least 1:32 and the distance of at least 20 km.
— *Extended power budget class* supports P2MP media channel insertion loss of ≤ 33 dB e.g., a PON with the split ratio of at least 1:64 and the distance of at least 20 km.

75.1.4 Power budgets

Each power budget class is represented by PRX-type power budget and PR-type power budget as follows:

— PRX–type power budget describes asymmetric-rate PHY for PON operating at 10 Gb/s downstream and 1 Gb/s upstream over a single SMF [see objective b 1) in 75.1.2].
— PR–type power budget describes symmetric-rate PHY for PON operating at 10 Gb/s downstream and 10 Gb/s upstream over a single SMF [see objective b 2) in 75.1.2].

Each power budget is further identified with a numeric representation of its class, where a value of 10 represents low power budget, a value of 20 represents medium power budget, a value of 30 represents high power budget, and a value of 40 represents extended power budget. Thus, the following power budgets are defined in Clause 75:

— PRX10: asymmetric-rate, low power budget, compatible with PX10 power budget defined in Clause 60.
— PRX20: asymmetric-rate, medium power budget, compatible with PX20 power budget defined in Clause 60.
— PRX30: asymmetric-rate, high power budget, compatible with PX30 power budget defined in Clause 60.
— PRX40: asymmetric-rate, extended power budget, compatible with PX40 power budget defined in Clause 60.
— PR10: symmetric-rate, low power budget, compatible with PX10 power budget defined in Clause 60
— PR20: symmetric-rate, medium power budget, compatible with PX20 power budget defined in Clause 60
— PR30: symmetric-rate, high power budget, compatible with PX30 power budget defined in Clause 60.
— PR40: symmetric-rate, extended power budget, compatible with PX40 power budget defined in Clause 60.

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Table 75–1 shows the primary attributes of all power budget types defined in Clause 75.

Table 75–1—Power budgets

Description	Low Power Budget		Medium Power Budget		High Power Budget		Extended Power Budget		Units
	PRX10	PR10	PRX20	PR20	PRX30	PR30	PRX40	PR40	
Number of fibers	1								–
Nominal downstream line rate	10.3125								GBd
Nominal upstream line rate	1.25	10.3125	1.25	10.3125	1.25	10.3125	1.25	10.3125	GBd
Nominal downstream wavelength	1577								nm
Downstream wavelength tolerance	–2, +3								nm
Nominal upstream wavelength	1310	1270	1310	1270	1310	1270	1310	1270	nm
Upstream wavelength tolerance	±50	±10	±50	±10	±50	±10	±20	±10	nm
Maximum reach[a]	≥10		≥20						km
Maximum channel insertion loss	20		24		29		33		dB
Minimum channel insertion loss	5		10		15		18		dB

[a]A compliant system may exceed the maximum reach designed for given power budget as long as optical power budget and other mandatory optical layer specifications are met.

75.1.5 Positioning of PMD sublayer within the IEEE 802.3 architecture

Figure 75–1 and Figure 75–2 depict the relationships of the symmetric-rate (10/10G–EPON) and asymmetric-rate (10/1G–EPON) PMD sublayer (shown hatched) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

75.2 PMD types

Similarly to power budget classes, asymmetric-rate and symmetric-rate PMDs are identified by PRX and PR designations, respectively.

The characteristics of the P2MP topology result in significantly different ONU and OLT PMDs. For example, the OLT PMD operates in a continuous mode in the transmit direction (downstream), but uses a burst mode in the receive direction (upstream). On the other hand, the ONU PMD receives data in a continuous mode, but transmits in a burst mode. To differentiate OLT PMDs from ONU PMDs, the OLT

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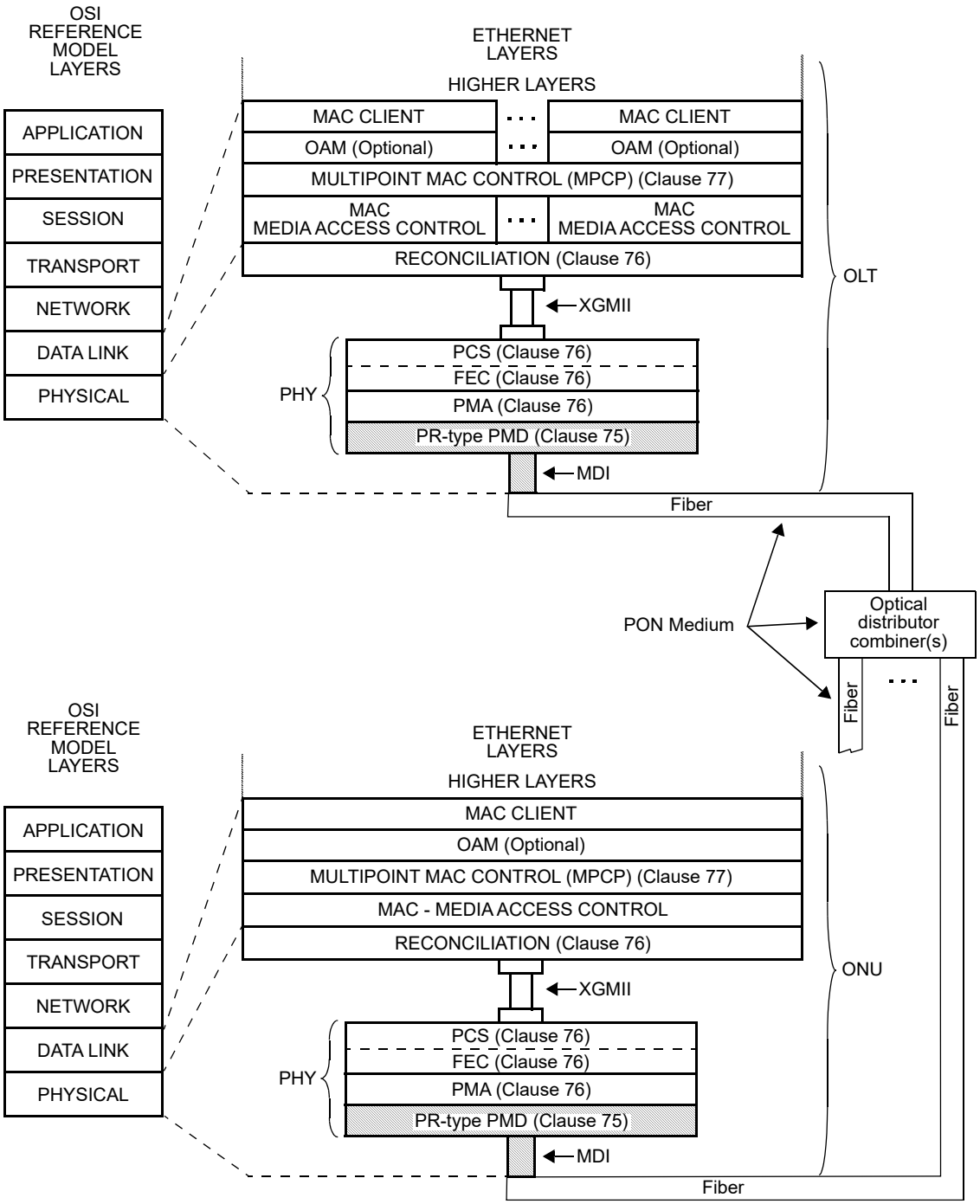

PMD and MDI described in this clause

XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 75–1—Relationship of 10/10G–EPON P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

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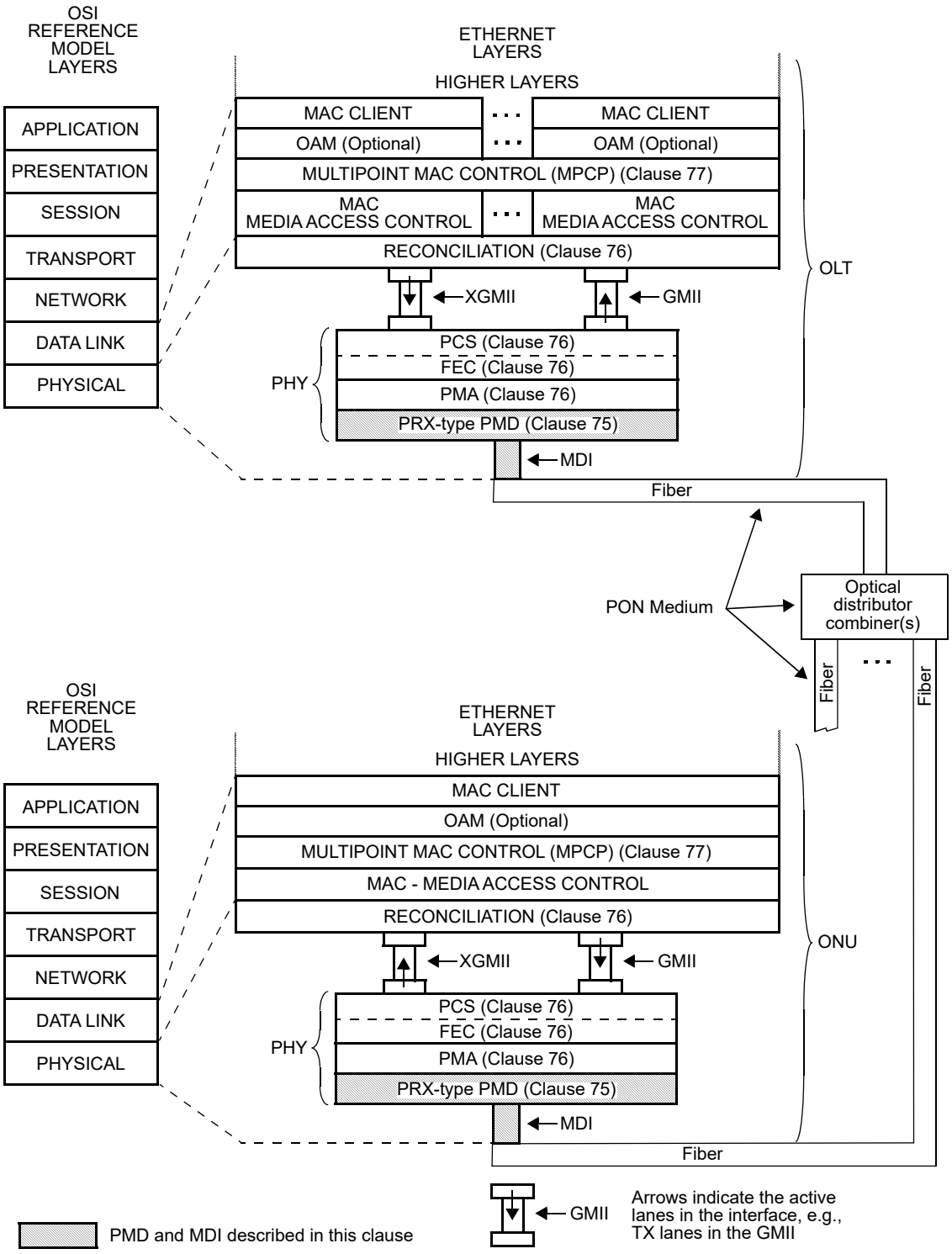

XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 75–2—Relationship of 10/1G–EPON P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

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PMD name has a suffix “D” appended to it, where D stands for downstream–facing PMD, e.g., 10GBASE–PR–D1. ONU PMDs have suffix “U” for upstream–facing PMD, e.g., 10GBASE–PR–U1.

In the downstream direction, the signal transmitted by the D-type PMD is received by all U-type PMDs. In the upstream direction, the D-type PMD receives data bursts from each of the U-type PMDs.

Clause 75 defines several D-type and several U-type PMDs, that differ in their receive and/or transmit characteristics. Such PMDs are further distinguished by appending a digit after the suffix D or U, e.g., 10GBASE–PR–D1 or 10GBASE–PR–D2.

The following OLT PMDs (D-type) are defined in this subclause:

a) Asymmetric-rate D-type PMDs (collectively referred to as 10/1GBASE–PRX–D), transmitting at 10.3125 GBd continuous mode and receiving at 1.25 GBd burst mode:
   1) 10/1GBASE–PRX–D1
   2) 10/1GBASE–PRX–D2
   3) 10/1GBASE–PRX–D3
   4) 10/1GBASE–PRX–D4
b) Symmetric-rate D-type PMDs (collectively referred to as 10GBASE–PR–D), transmitting at 10.3125 GBd continuous mode and receiving at 10.3125 GBd burst mode:
   1) 10GBASE–PR–D1
   2) 10GBASE–PR–D2
   3) 10GBASE–PR–D3
   4) 10GBASE–PR–D4

The following ONU PMDs (U-type) are defined in this subclause:

c) Asymmetric-rate U-type PMDs (collectively referred to as 10/1GBASE–PRX–U), transmitting at 1.25 GBd burst mode and receiving at 10.3125 GBd continuous mode:
   1) 10/1GBASE–PRX–U1
   2) 10/1GBASE–PRX–U2
   3) 10/1GBASE–PRX–U3
   4) 10/1GBASE–PRX–U4
d) Symmetric-rate U-type PMDs (collectively referred to as 10GBASE–PR–U), transmitting at 10.3125 GBd burst mode and receiving at 10.3125 GBd continuous mode:
   1) 10GBASE–PR–U1
   2) 10GBASE–PR–U3
   3) 10GBASE-PR–U4

A specific power budget is achieved by combining an OLT PMD (D-type) with an ONU PMD (U-type) as shown in 75.2.1. Detailed PMD receive and transmit characteristics for D-type PMDs are given in 75.4 and characteristics for U-type PMDs are presented in 75.5. Every PMD has non-overlapping transmit and receive wavelength bands and operates over a single SMF (see 75B.2).

75.2.1 Mapping of PMDs to power budgets

The power budget is determined by the PMDs located at the ends of the physical media. This subclause describes how PMDs may be combined to achieve the power budgets listed in Table 75–1.

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75.2.1.1 Asymmetric-rate, 10 Gb/s downstream and 1 Gb/s upstream power budgets (PRX type)

Table 75–2 illustrates recommended pairings of asymmetric-rate ONU PMDs with asymmetric-rate OLT PMDs to achieve the power budgets shown in Table 75–1.

Table 75–2—PMD – power budget mapping for asymmetric-rate PRX–type power budgets

		OLT PMDs			
		10/1GBASE–PRX–D1	**10/1GBASE–PRX–D2**	**10/1GBASE–PRX–D3**	**10/1GBASE–PRX–D4**
ONU PMDs	**10/1GBASE–PRX–U1**	PRX10	N/A	N/A	N/A
	10/1GBASE–PRX–U2	N/A	PRX20	N/A	N/A
	10/1GBASE–PRX–U3	N/A	N/A	PRX30	N/A
	10/1GBASE–PRX–U4	N/A	N/A	N/A	PRX40

75.2.1.2 Symmetric-rate, 10 Gb/s power budgets (PR type)

Table 75–3 illustrates recommended pairings of symmetric-rate ONU PMDs with symmetric-rate OLT PMDs to achieve the power budgets as shown in Table 75–1.

Table 75–3—PMD – power budget mapping for symmetric-rate PR–type power budgets

		OLT PMDs			
		10GBASE–PR–D1	**10GBASE–PR–D2**	**10GBASE–PR–D3**	**10GBASE–PR–D4**
ONU PMDs	**10GBASE–PR–U1**	PR10	PR20	N/A	N/A
	10GBASE–PR–U3	N/A	N/A	PR30	N/A
	10GBASE–PR–U4	N/A	N/A	N/A	PR40

75.3 PMD functional specifications

The 10GBASE–PR and 10/1GBASE–PRX type PMDs perform the transmit and receive functions that convey data between the PMD service interface and the MDI.

75.3.1 PMD service interface

The following specifies the services provided by Clause 75 PMDs. These PMD sublayer service interfaces are described in an abstract manner and do not imply any particular implementation.

The PMD Service Interface supports the exchange of a continuous stream of bits, representing either 64B/66B blocks (the transmit and receive paths in 10GBASE–PR PMDs, transmit path in 10/1GBASE–PRX–D PMDs) or 8B/10B blocks (transmit path in 10/1GBASE–PRX–U PMDs, receive path in 10/1GBASE–PRX–D PMDs), between the PMA and PMD entities. The PMD translates the serialized data

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received from the compatible PMA to and from signals suitable for the specified medium. The following primitives are defined:

— PMD_UNITDATA.request
— PMD_UNITDATA.indication
— PMD_SIGNAL.request
— PMD_SIGNAL.indication

75.3.1.1 Delay constraints

The PMD shall introduce a transmit delay of not more than 4 time_quanta with the variability of no more than 0.5 time_quanta, and a receive delay of not more than 4 time_quanta with the variability of no more than 0.5 time_quanta. A description of the overall system delay constraints can be found in 76.1.2 and the definition for the time_quantum can be found in 77.2.2.1.

75.3.1.2 PMD_UNITDATA.request

This primitive defines the transfer of a serial data stream from the Clause 65 or Clause 76 PMA to the PMD.

The semantics of the service primitive are PMD_UNITDATA.request(tx_bit). The data conveyed by PMD_UNITDATA.request is a continuous stream of bits. The tx_bit parameter can take one of two values: ONE or ZERO. The Clause 76 PMA continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal signaling speed of 10.3125 GBd in the case of 10/10G–EPON OLT, 10/10G–EPON ONU, and 10/1G–EPON OLT PMDs. The Clause 65 PMA continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal signaling speed of 1.25 GBd in the case of 10/1G–EPON ONU PMDs. Upon the receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals at the MDI.

75.3.1.3 PMD_UNITDATA.indication

This primitive defines the transfer of data from the PMD to the Clause 65 or Clause 76 PMA.

The semantics of the service primitive are PMD_UNITDATA.indication(rx_bit). The data conveyed by PMD_UNITDATA.indication is a continuous stream of bits. The rx_bit parameter can take one of two values: ONE or ZERO. The PMD continuously sends a stream of bits to the Clause 76 PMA corresponding to the signals received from the MDI, at the nominal signaling speed of 10.3125 GBd in the case of 10/10G–EPON OLT, 10/10G–EPON ONU, and 10/1G–EPON ONU PMDs or to the Clause 65 PMA at the nominal signaling speed of 1.25 GBd in the case of 10/1G–EPON OLT PMDs.

75.3.1.4 PMD_SIGNAL.request

In the upstream direction, this primitive is generated by the Clause 76 PMA to turn on and off the transmitter according to the granted time. A signal for laser control is generated as described in 76.4.1.1 for the Clause 76 PCS.

The semantics of the service primitive are PMD_SIGNAL.request(tx_enable). The tx_enable parameter can take on one of two values: ENABLE or DISABLE, determining whether the PMD transmitter is on (enabled) or off (disabled). The Clause 76 PMA generates this primitive to indicate a change in the value of tx_enable. Upon the receipt of this primitive, the PMD turns the transmitter on or off as appropriate.

75.3.1.5 PMD_SIGNAL.indication

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

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The semantics of the service primitive are PMD_SIGNAL.indication(SIGNAL_DETECT). The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting light at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication(rx_bit) is undefined. The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT. If the MDIO interface is implemented, then PMD_global_signal_detect shall be continuously set to the value of SIGNAL_DETECT.

NOTE—SIGNAL_DETECT = OK does not guarantee that PMD_UNITDATA.indication(rx_bit) is known good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the specified bit error ratio. PMD_SIGNAL.indication(SIGNAL_DETECT) has different characteristics for upstream and downstream links, see 75.3.5.

75.3.2 PMD block diagram

The PMD sublayer is defined at the eight reference points shown in Figure 75–3 for 10GBASE–PR and 10/1GBASE–PRX PMDs.

For 10GBASE–PR and 10/1GBASE–PRX PMDs, test points TP1 through TP4 refer to the downstream channel, while test points TP5 through TP8 refer to the upstream channel. In the downstream channel, TP2 and TP3 are compliance points, while in the upstream channel TP6 and TP7 are compliance points. TP1, TP4, TP5, and TP8 are reference points for use by implementers. The optical transmit signal is defined at the output end of a patch cord (TP2 for the downstream channel and TP6 for the upstream channel), between 2 m and 5 m in length, of a fiber type consistent with the link type connected to the transmitter. Unless specified otherwise, all transmitter measurements and tests defined in 75.7 are made at TP2 or TP6, while tests defined in 60.9 are made at TP6. The optical receive signal is defined at the output of the fiber optic cabling (TP3 for the downstream channel and TP7 for the upstream channel) connected to the receiver. Unless specified otherwise, all receiver measurements and tests defined in 75.7 are made at TP3 or TP7.

The electrical specifications of the PMD service interface (TP1 and TP4 for the downstream channel and TP5 and TP8 for the upstream channel) are not system compliance points (these are not readily testable in a system implementation).

75.3.3 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the optical specifications in Clause 75.

In the upstream direction, the flow of bits is interrupted according to PMD_SIGNAL.request(tx_enable). This implies three optical levels, 1, 0, and dark, the latter corresponding to the transmitter being in the OFF state. The higher optical power level shall correspond to tx_bit = ONE.

75.3.4 PMD receive function

The PMD Receive function shall convey the bits received from the MDI according to the optical specifications in Clause 75 to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). The higher optical power level shall correspond to rx_bit = ONE.

75.3.5 PMD signal detect function

75.3.5.1 ONU PMD signal detect

The PMD Signal Detect function for the continuous mode downstream signal shall report to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indication is intended to be an indicator of the presence of the optical signal.

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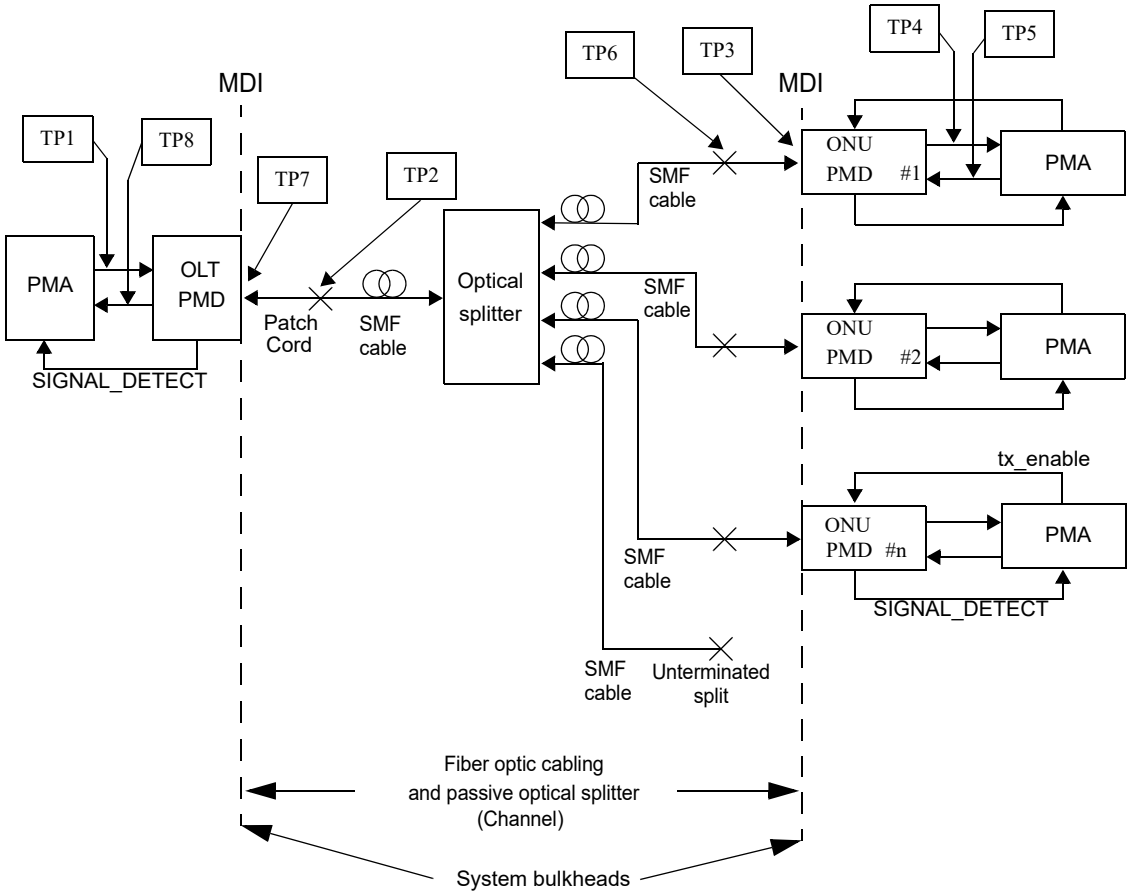

Figure 75–3—10GBASE–PR and 10/1GBASE–PRX block diagram

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 75–4 for 10GBASE–PR and 10/1GBASE–PRX type PMDs. The ONU PMD receiver is not required to verify whether a compliant 10GBASE–PR signal is being received.

75.3.5.2 OLT PMD signal detect

The response time for the PMD Signal Detect function for the burst mode upstream signal may be longer or shorter than a burst length; thus, it may not fulfill the traditional requirements placed on Signal Detect. PMD_SIGNAL.indication is intended to be an indicator of optical signal presence. The signal detect function in the OLT may be realized in the PMD or the Clause 76 PMA sublayer.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 75–4 for PMDs defined in Clause 75. The 10GBASE–PR–D PMD receiver is not required to verify whether a compliant 10GBASE–PR signal is being received. Similarly, the 10/1GBASE–PRX–D PMD receiver is not required to verify whether a compliant 1000BASE–PX signal is being received.

75.3.5.3 10GBASE–PR and 10/1GBASE–PRX Signal detect functions

The Signal Detect value definitions for Clause 75 PMDs are shown in Table 75–4.

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Table 75–4—SIGNAL_DETECT value definitions for Clause 75 PMDs

PMD type	Receive conditions	SIGNAL_DETECT value
10GBASE–PR–D1, 10GBASE–PR–D2, 10GBASE–PR–D3, 10GBASE–PR–D4	Average input optical power ≤ Signal Detect Threshold (min) in Table 75–6 at the specified receiver wavelength	FAIL
	Average input optical power ≥ Receive sensitivity (max) in Table 75–6 with a compliant 10GBASE–PR signal input at the specified receiver wavelength	OK
	All other conditions	Unspecified
10GBASE–PR–U1, 10GBASE–PR–U3, 10GBASE–PR–U4 10/1GBASE–PRX–U1, 10/1GBASE–PRX–U2, 10/1GBASE–PRX–U3, 10/1GBASE–PRX–U4	Average input optical power ≤ Signal Detect Threshold (min) in Table 75–10 at the specified receiver wavelength	FAIL
	Average input optical power ≥ Receive sensitivity (max) in Table 75–10 with a compliant 10GBASE–PR signal input at the specified receiver wavelength	OK
	All other conditions	Unspecified
10/1GBASE–PRX–D1, 10/1GBASE–PRX–D2, 10/1GBASE–PRX–D3, 10/1GBASE–PRX–D4	Average input optical power ≤ Signal Detect Threshold (min) in Table 75–7 at the specified receiver wavelength	FAIL
	Average input optical power ≥ Receive sensitivity (max) in Table 75–7 with a compliant 1000BASE–PX signal input at the specified receiver wavelength	OK
	All other conditions	Unspecified

75.3.6 PMD transmit enable function for ONU

PMD_SIGNAL.request(tx_enable) is defined for all ONU PMDs specified in Clause 75. PMD_SIGNAL.request(tx_enable) is asserted prior to data transmission by the ONU PMDs.

75.4 PMD to MDI optical specifications for 10/10G–EPON and 10/1G–EPON OLT PMDs

This subclause details the PMD to MDI optical specifications for 10/10G–EPON and 10/1G–EPON OLT PMDs, as specified in 75.2. Specifically, 75.4.1 defines the OLT transmit parameters, while 75.4.2 defines the OLT receive parameters.

The operating ranges for PR and PRX power budget classes are defined in Table 75–1. A PR or PRX compliant transceiver operates over the media types listed in Table 75–14 according to the specifications described in 75.9. A transceiver which exceeds the operational range requirement while meeting all other optical specifications is considered compliant.

NOTE—The specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is defined in 58.7.6.

75.4.1 Transmitter optical specifications

The signaling speed, operating wavelength, side mode suppression ratio, average launch power, extinction ratio, return loss tolerance, OMA, eye, and Transmitter and Dispersion Penalty (TDP) for transmitters making part of the 10/10G–EPON and 10/1G–EPON OLT PMDs (as specified in 75.2) shall meet the specifications defined in Table 75–5 per measurement techniques described in 75.7. Their $RIN_{15}OMA$ should meet the value listed in Table 75–5 per measurement techniques described in 75.7.8. Note that there are only two groups of transmit parameters. The first group is shared by 10GBASE–PR–D1, 10/1GBASE–PRX–D1, 10GBASE–PR–D3, and 10/1GBASE–PRX–D3. The second group is shared by 10GBASE–PR–D2, 10GBASE–PR–D4, 10/1GBASE–PRX–D2, and 10/1GBASE-PRX-D4.

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Table 75–5—PR and PRX type OLT PMD transmit characteristics

Description	10GBASE–PR–D1, 10GBASE–PR–D3, 10/1GBASE–PRX–D1, 10/1GBASE–PRX–D3	10GBASE–PR–D2, 10GBASE–PR–D4, 10/1GBASE–PRX–D2, 10/1GBASE-PRX-D4	Unit
Signaling speed (range)	10.3125 ± 100 ppm		GBd
Wavelength (range)	1575 to 1580		nm
Side Mode Suppression Ratio (min)[a]	30		dB
Average launch power (max)	5	9	dBm
Average launch power (min)[b]	2	5	dBm
Average launch power of OFF transmitter (max)	–39		dBm
Extinction ratio (min)	6		dB
$RIN_{15}OMA$ (max)	–128		dB/Hz
Launch OMA (min)[b]	3.91 (2.46)	6.91 (4.91)	dBm (mW)
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}[c]	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}		UI
Optical return loss tolerance (max)	15		dB
Transmitter reflectance (max)	–10		dB
Transmitter and dispersion penalty (max)	1.5		dB
Decision timing offset for transmitter and dispersion penalty	±0.05		UI

[a]Transmitter is a single longitudinal mode device. Chirp is allowed such that the total optical path penalty does not exceed that found in Table 75B–1 and Table 75B–2.
[b]Minimum average launch power and minimum launch OMA are valid for ER = 9 dB (see Figure 75–4 for details)
[c]As defined in Figure 75–6.

The relationship between OMA, extinction ratio, and average power is described in 58.7.6 and illustrated in Figure 75–4 for a compliant transmitter. Note that the OMA_{min} and AVP_{min} are calculated for ER = 9 dB, where AVP_{min} represents the Average launch power (min) as presented in Table 75–5. The transmitter specifications are further relaxed by allowing lower ER = 6 dB while maintaining the OMA_{min} and AVP_{min} constant. The shaded area indicates a compliant part.

75.4.2 Receiver optical specifications

The signaling speed, operating wavelength, overload, stressed sensitivity, reflectance, and signal detect for receivers forming part of the 10/10G–EPON and 10/1G–EPON OLT PMDs (as specified in 75.2) shall meet the specifications defined in Table 75–6 for 10/10G–EPON OLT PMDs and in Table 75–7 for 10/1G–EPON OLT PMDs, per measurement techniques defined in 75.7. Their unstressed receive characteristics should meet the values listed in Table 75–6 and Table 75–7 per measurement techniques described in 75.7.11. Either the damage threshold included in Table 75–6 or Table 75–7 shall be met, or the receiver shall be labeled to indicate the maximum optical input power level to which it can be continuously exposed without damage.

The damage threshold included in Table 75–6 and Table 75–7 does not guarantee direct ONU–OLT connection, which may result in damage of the receiver. If direct ONU–OLT connection is necessary, optical attenuators and/or equivalent loss components should be inserted to decrease receive power below the damage threshold.

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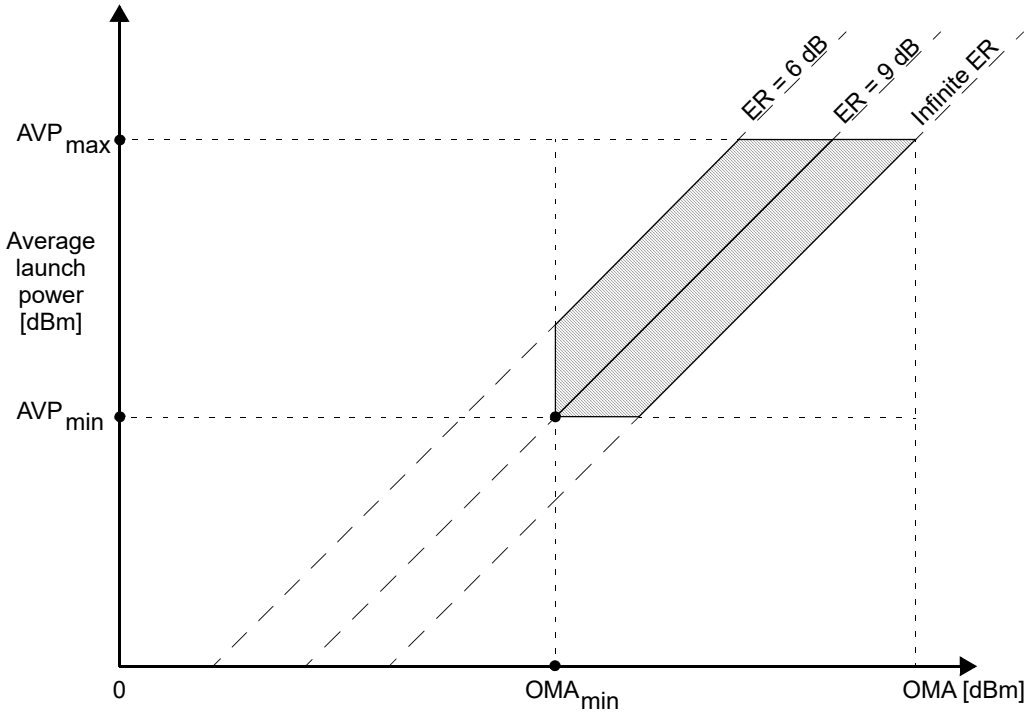

Figure 75–4—Graphical representation of region of PR–D type transmitter compliance

Table 75–6—PR type OLT PMD receive characteristics

Description	10GBASE–PR–D1	10GBASE–PR–D2, 10GBASE–PR–D3	10GBASE–PR–D4	Unit
Signaling speed (range)	10.3125 ± 100 ppm			GBd
Wavelength (range)	1260 to 1280			nm
Bit error ratio (max)[a]	10^{-3}			–
Average receive power (max)	–1	–6	–9	dBm
Damage threshold (max)[b]	0	–5	–8	dBm
Receiver sensitivity (max)	–24	–28	–29	dBm
Receiver sensitivity OMA (max)	–23.22 (4.77)	–27.22 (1.9)	–28.22 (1.51)	dBm (μW)
Signal detect threshold (min)	–45			dBm
Receiver reflectance (max)	–12			dB
Stressed receive sensitivity (max)[c]	–21	–25	–27	dBm

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Table 75–6—PR type OLT PMD receive characteristics *(continued)*

Description	10GBASE–PR–D1	10GBASE–PR–D2, 10GBASE–PR–D3	10GBASE–PR–D4	Unit
Stressed receive sensitivity OMA (max)	–20.22 (9.51)	–24.22 (3.79)	–26.22 (2.39)	dBm (μW)
Vertical eye–closure penalty[d]	2.99			dB
$T_{receiver\_settling}$ (max)[e]	800			ns
Stressed eye jitter	0.3			UI pk-pk
Jitter corner frequency for a sinusoidal jitter	4			MHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)	(0.05, 0.15)			UI

[a]The BER of 10^{-12} is achieved by the utilization of FEC as described in 76.3.
[b]Direct ONU–OLT connection may result in damage of the receiver.
[c]The stressed receiver sensitivity is mandatory.
[d]Vertical eye closure penalty and the jitter specifications are test conditions for measuring stressed receiver sensitivity. They are not required characteristics of the receiver.
[e]$T_{receiver\_settling}$ represents an upper bound. Optics with better performance may be used in compliant implementations, since the OLT notifies the ONUs of its requirements in terms of the $T_{receiver\_settling}$ time via the syncTime parameter (see 77.3.3.2).

Table 75–7—PRX type OLT PMD receive characteristics

PMD type	Receive parameters	Reference
10/1GBASE–PRX–D1	same as 1000BASE–PX10–D receive parameters	see Table 60–5
10/1GBASE–PRX–D2	same as 1000BASE–PX20–D receive parameters	see Table 60–8
10/1GBASE–PRX–D3	same as 1000BASE–PX30–D receive parameters[a]	see Table 60–11
10/1GBASE–PRX–D4	same as 1000BASE–PX40–D receive parameters[a]	see Table 60–13

[a]Stressed receive sensitivity (max) is mandatory for 10/1GBASE–PRX–D3 and 10/1GBASE–PRX–D4 PMDs.

75.5 PMD to MDI optical specifications for 10/10G–EPON and 10/1G–EPON ONU PMDs

This subclause details the PMD to MDI optical specifications for 10/10G–EPON and 10/1G–EPON ONU PMDs, as specified in 75.2. Specifically, 75.5.1 defines the ONU transmit parameters, while 75.5.2 defines the ONU receive parameters.

The operating ranges for PR and PRX power budget classes are defined in Table 75–1. A PR or PRX compliant transceiver operates over the media types listed in Table 75–14 according to the specifications described in 75.9. A transceiver which exceeds the operational range requirement while meeting all other optical specifications is considered compliant.

NOTE—The specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is defined in 58.7.6.

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75.5.1 Transmitter optical specifications

The signaling speed, operating wavelength, spectral width (for 10/1G–EPON ONU PMDs) or side mode suppression ratio (for 10/10G–EPON ONU PMDs), average launch power, extinction ratio, return loss tolerance, OMA, eye and TDP for transmitters forming part of the 10/10G–EPON and 10/1G–EPON ONU PMDs (as specified in 75.2) shall meet the specifications defined in Table 75–8 for 10/10G–EPON ONU PMDs and in Table 75–9 for 10/1G–EPON ONU PMDs, per measurement techniques described in 75.7. Their $RIN_{15}OMA$ should meet the value listed in Table 75–8 or Table 75–9, as appropriate, per measurement techniques described in 75.7.8.

Table 75–8—PR type ONU PMD transmit characteristics

Description	10GBASE –PR–U1	10GBASE –PR–U3	10GBASE –PR–U4	Unit
Signaling speed (range)	10.3125 ± 100 ppm			GBd
Wavelength (range)	1260 to 1280			nm
Side Mode Suppression Ratio (min)[a]	30			dB
Average launch power (max)	4	9	9	dBm
Average launch power (min)[b]	–1	4	6	dBm
Average launch power of OFF transmitter (max)	–45			dBm
Extinction ratio (min)	6			dB
$RIN_{15}OMA$ (max)	–128			dB/Hz
Launch OMA (min)[b]	–0.22 (0.95)	4.78 (3.01)	6.78 (4.77)	dBm (mW)
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}[c]	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			UI
T_{on} (max)	512			ns
T_{off} (max)	512			ns
Optical return loss tolerance (max)	15			dB
Transmitter reflectance (max)	–10			dB
Transmitter and dispersion penalty (max)[d]	3	3	2	dB
Decision timing offset for transmitter and dispersion penalty	±0.0625			UI

[a]Transmitter is a single longitudinal mode device. Chirp is allowed such that the total optical path penalty does not exceed that found in Table 75B–2.
[b]Minimum average launch power and minimum launch OMA are valid for ER = 6 dB (see Figure 75–5 for details).
[c]As defined in Figure 75–6.
[d]If a transmitter has a lower TDP, the minimum transmitter launch OMA (OMA_{min}) and average minimum launch power (AVP_{min}) may be relaxed by the amount 3 dB – TDP for 10GBASE-PR-U1 and 10GBASE-PR-U3 and 2 dB – TDP for 10G-BASE-PR-U4.

The relationship between OMA, extinction ratio and average power is described in 58.7.6 and illustrated in Figure 75–5 for a compliant transmitter. Note that the OMA_{min} and AVP_{min} are calculated for ER = 6 dB. The transmitter average launch power specifications are further relaxed by allowing ER higher than 6 dB while maintaining the OMA_{min} constant. The shaded area indicates a compliant part.

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Table 75–9—PRX type ONU PMD transmit characteristics

PMD type	Transmit parameters[a]	Reference
10/1GBASE–PRX–U1	same as 1000BASE–PX10–U transmit parameters	see Table 60–3
10/1GBASE–PRX–U2	same as 1000BASE–PX20–U transmit parameters	see Table 60–6
10/1GBASE–PRX–U3	same as 1000BASE–PX30–U transmit parameters	see Table 60–9
10/1GBASE–PRX–U4	same as 1000BASE–PX40–U transmit parameters	see Table 60–12

[a]Optical return loss of ODN (min) is optional for 10/1GBASE–PRX–U1, 10/1GBASE–PRX–U2, 10/1GBASE–PRX–U3, and 10/1GBASE–PRX–U4 PMDs.

The maximum RMS spectral width vs. wavelength for 10/1GBASE–PRX–U1, 10/1GBASE–PRX–U2 and 10/1GBASE–PRX–U3 PMDs are shown, respectively, in Table 60–4, Table 60–7, and Table 75–10. The equation used to generate these values is included in 60.9.2.

75.5.2 Receiver optical specifications

The signaling speed, operating wavelength, overload, stressed sensitivity, reflectance, and signal detect for receivers forming part of the 10/10G–EPON ONU and 10/1G–EPON ONU PMDs (as specified in 75.2) shall meet the specifications defined in Table 75–10 for Clause 75 ONU PMDs, per measurement techniques defined in 75.7. Their unstressed receive characteristics should meet the values listed in Table 75–10 per measurement techniques described in 75.7.11. Either the damage threshold included in Table 75–10 shall be met, or the receiver shall be labeled to indicate the maximum optical input power level to which it can be continuously exposed without damage.

The damage threshold included in Table 75–10 does not guarantee direct ONU–OLT connection, which may result in damage of the receiver. If direct ONU–OLT connection is necessary, optical attenuators and/or equivalent loss components should be inserted to decrease receive power below damage threshold.

Table 75–10—PR and PRX type ONU PMD receive characteristics

Description	10GBASE–PR–U1, 10/1GBASE–PRX–U1, 10/1GBASE–PRX–U2	10GBASE–PR–U3, 10/1GBASE–PRX–U3	10GBASE–PR–U4, 10/1GBASE–PRX–U4	Unit
Signaling speed (range)	10.3125 ± 100 ppm			GBd
Wavelength (range)	1575 to 1580			nm
Bit error ratio (max)[a]	10^{-3}			—
Average receive power (max)	0	–10	–9	dBm
Damage threshold (max)[b]	1	–9	–8	dBm
Receiver sensitivity (max)	–20.5	–28.5	–29.5	dBm
Receiver sensitivity OMA (max)	–18.59 (13.84)	–26.59 (2.19)	–27.59 (1.74)	dBm (μW)

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Table 75–10—PR and PRX type ONU PMD receive characteristics *(continued)*

Description	10GBASE–PR–U1, 10/1GBASE–PRX–U1, 10/1GBASE–PRX–U2	10GBASE–PR–U3, 10/1GBASE–PRX–U3	10GBASE–PR–U4, 10/1GBASE–PRX–U4	Unit
Signal detect threshold (min)	–44			dBm
Receiver reflectance (max)	–12			dB
Stressed receive sensitivity (max)[c]	–19	–27	–28	dBm
Stressed receive sensitivity OMA (max)	–17.09 (19.55)	–25.09 (3.1)	–26.09 (2.46)	dBm (μW)
Vertical eye–closure penalty[d]	1.5			dB
Stressed eye jitter (min)	0.3			UI pk-pk
Jitter corner frequency for a sinusoidal jitter	4			MHz
Sinusoidal jitter limits for stressed receiver conformance test (min, max)	(0.05, 0.15)			UI

[a]The BER of 10^{-12} is achieved by the utilization of FEC as described in 76.3.
[b]Direct ONU–OLT connection may result in damage of the receiver.
[c]The stressed receiver sensitivity is mandatory over the entire PR–D transmitter compliance region, as illustrated in Figure 75–4.
[d]Vertical eye closure penalty and the jitter specifications are test conditions for measuring stressed receiver sensitivity. They are not required characteristics of the receiver.

75.6 Dual-rate (coexistence) mode

To support coexistence of 10G–EPON and 1G–EPON ONUs on the same outside plant, the OLT may be configured to use a dual-rate mode. Dual-rate mode supports transmission and/or reception of both 10 Gb/s and 1 Gb/s data rates, and can be introduced as options for 10G–EPON OLTs, functionally combining PMDs supporting 10 Gb/s and 1 Gb/s data rates.

Table 75–11 depicts PMD coexistence mapping for dual-rate mode options.

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Table 75–11—PMD coexistence mapping for dual-rate mode option[a]

Direction of dual-rate operation	OLT PMD combination	ONU PMDs coexisting on the same ODN
Downstream	1000BASE–PX–D 10/1GBASE–PRX–D	(1) 1000BASE–PX–U (2) 10/1GBASE–PRX–U
Upstream	10GBASE–PR–D 10/1GBASE–PRX–D	(1) 10GBASE–PR–U (2) 10/1GBASE–PRX–U
Downstream and upstream	1000BASE–PX–D 10GBASE–PR–D	(1) 1000BASE–PX–U (2) 10/1GBASE–PRX–U (3) 10GBASE–PR–U

[a]Only PMDs with compatible power budgets can be connected to the same ODN.

75.6.1 Downstream dual-rate operation

When the downstream dual-rate operation is enabled, the OLT transmits both 10 Gb/s and 1 Gb/s downstream signals in a WDM manner. The OLT should meet both 10 Gb/s and 1 Gb/s specifications defined in Table 75–5 (10GBASE–PR–D transmit characteristics) and in Table 60–3, Table 60–6, Table 60–9, or Table 60–12 (1000BASE–PX–D transmit characteristics).

75.6.2 Upstream dual-rate operation

When the upstream dual-rate operation is enabled, the OLT receives both 10 Gb/s and 1 Gb/s upstream signals in a TDMA manner. Further implementation details are described in Annex 75A. The OLT should meet both 10 Gb/s and 1 Gb/s specifications defined in Table 75–6 (10GBASE–PR–D receive characteristics), and in Table 60–5, Table 60–8, Table 60–11, and Table 60–13 (1000BASE–PX–D receive characteristics).

NOTE—The damage threshold values in Table 60–5, Table 60–8, Table 60–11, and Table 60–13 are considerably higher than those in Table 75–6; the dual-rate PMD should be labeled appropriately.

75.7 Definitions of optical parameters and measurement methods

When measuring jitter at TP1 and TP5, it is recommended that jitter contributions at frequencies below receiver corner frequencies (i.e., 4 MHz for 10.3125 GBd receiver and 637 kHz for 1.25 GBd receiver) are filtered at the measurement unit. The following subclauses describe definitive patterns and test procedures for certain PMDs of this standard. Implementers using alternative verification methods should ensure adequate correlation and allow adequate margin such that specifications are met by reference to the definitive methods. All optical measurements, except TDP and $RIN_{15}OMA$ shall be made through a short patch cable between 2 m and 5 m in length.

75.7.1 Insertion loss

Insertion loss for SMF fiber optic cabling (channel) is defined at 1270 nm, 1310 nm, or 1577 nm, depending on the particular PMD. A suitable test method is described in ITU–T G.650.1.

75.7.2 Allocation for penalties in 10G–EPON PMDs

All the receiver types specified in Clause 75 are required to tolerate a path penalty not exceeding 1 dB to account for total degradations due to reflections, intersymbol interference, mode partition noise, laser chirp and detuning of the central wavelength, including chromatic dispersion penalty. All the transmitter types specified in Clause 75 introduce less than 1 dB of optical path penalty over the channel. The path penalty is

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a component of transmitter and dispersion penalty (TDP), which is specified in Table 75–5, Table 75–8, and Table 75–9 and described in 58.7.9.

75.7.3 Test patterns

Two types of test patterns are used for testing of 10 Gb/s optical PMDs: square wave (52.9.1.2) and patterns 1, 2, or 3 (52.9.1.1). These 10 Gb/s test patterns for 10GBASE–PR and 10/1GBASE–PRX are in Table 75–12. Two types of test frames [random and jitter (59.7.1)] are used for 1 Gb/s tests relevant to the 10/1GBASE–PRX PHY. All test patterns are listed in Table 75–12.

Table 75–12—Test patterns

Test	10 Gb/s pattern[a]	1 Gb/s pattern	Related subclause
Average optical power	1 or 3	Valid 8B/10B	75.7.5
OMA (modulated optical power)	Square	Idles	75.7.7
Extinction ratio	1 or 3	Idles	75.7.6
Transmit eye	1 or 3	Valid 8B/10B	75.7.7
$RIN_{15}OMA$	Square	Idles	75.7.8
Wavelength, spectral width	1 or 3	Valid 8B/10B	75.7.4
Side mode suppression ratio	1 or 3	Valid 8B/10B	75.7.4
VECP calibration	2 or 3	Jitter frame	75.7.12
Receiver sensitivity	1 or 3	Random frame	75.7.11
Receiver overload	1 or 3	Valid 8B/10B	—
Stressed receive sensitivity	2 or 3	Random frame	75.7.12
Transmitter and dispersion penalty	2 or 3	Random frame	75.7.10
Jitter	2 or 3	Jitter frame	75.7.13
Laser On/Off	1 or 3	Valid 8B/10B	75.7.14
Receiver settling	1 or 3	Valid 8B/10B	75.7.15

[a]Individual 10 Gb/s test patterns are described in 52.9.1.2 for a square wave and 52.9.1.1 for test patterns represented by numbers.

75.7.4 Wavelength, spectral width, and side mode suppression ratio (SMSR) measurement

The center wavelength, spectral width (RMS), and SMSR shall meet the specifications when measured according to the centroidal wavelength, RMS spectral width, and SMSR definitions in IEC 61280-1-3 under modulated conditions using an appropriate PRBS or a valid 10GBASE–PR signal, 1000BASE–X signal, or another representative test pattern.

NOTE—The allowable range of central wavelengths is narrower than the operating wavelength range by the actual RMS spectral width at each extreme.

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75.7.5 Optical power measurements

Optical power shall meet specifications according to the methods specified in IEC 61280-1-1. A measurement may be made with the port transmitting any valid encoded 8B/10B or 64B/66B data stream.

75.7.6 Extinction ratio measurements

The extinction ratio shall meet the specifications when measured according to IEC 61820-2-2 with the port transmitting a repeating idle pattern /I2/ ordered set (see 36.2.4.12) or valid 10GBASE–PR signal, and with minimal back reflections into the transmitter, lower than –20 dB. The test receiver has the frequency response as specified for the transmitter optical waveform measurement.

75.7.7 Optical modulation amplitude (OMA) test procedure

A description of OMA measurements for 1 Gb/s PHYs is found in 58.7.5. The OMA measurements for 10 Gb/s PHYs shall be compliant with the description found in 52.9.5.

75.7.8 Relative intensity noise optical modulation amplitude (RIN_xOMA) measuring procedure

This procedure describes a component test that may not be appropriate for a system level test depending on the implementation. If used, the procedure shall be performed as described in 52.9.6 for 10 Gb/s PHYs and in 58.7.7 for 1 Gb/s PHYs.

75.7.9 Transmit optical waveform (transmit eye)

The required transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 75–5 for upstream direction of 10/1GBASE–PRX PMD and Figure 75–6 for downstream direction of 10/1GBASE–PRX PMD and both directions of 10GBASE–PR PMD.

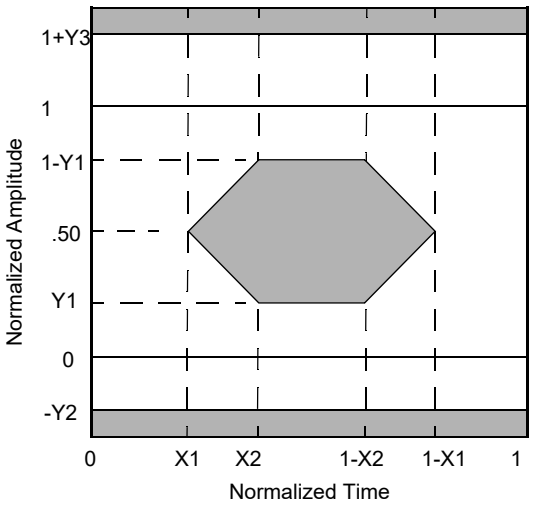

Figure 75–5—Transmitter eye mask definition for upstream direction of 10/1GBASE–PRX PMD

The measurement procedure is described in 58.7.8 for 1 Gb/s PHYs and 52.9.7 for 10 Gb/s PHYs and references therein. The eye shall comply to the mask of the eye using a fourth-order Bessel-Thomson

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receiver response as defined in 60.9.8 for 1 Gb/s PMD transmitters and 52.9.7 for 10 Gb/s PMD transmitters.

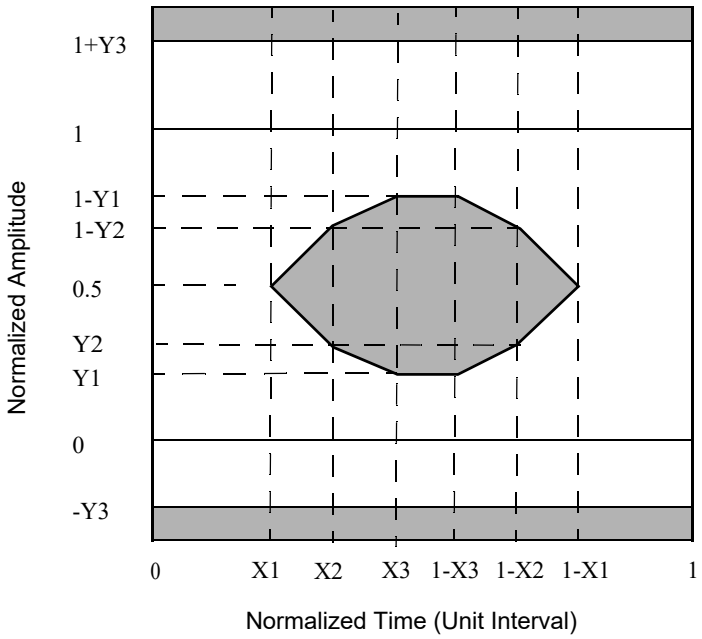

Figure 75–6—Transmitter eye mask definition for downstream direction of 10/1GBASE–PRX PMD and both directions of 10GBASE–PR PMD

75.7.10 Transmitter and dispersion penalty (TDP)

TDP measurement tests transmitter impairments, including chromatic dispersion effects, due to signal propagation in SMF used in PON. Possible causes of impairment include intersymbol interference, jitter, and RIN. Meeting the separate requirements (e.g., eye mask, spectral characteristics) does not in itself guarantee the TDP. The TDP limit shall be met. See 58.7.9 for details of the measurement for 1 Gb/s PHYs. For 10 Gb/s PHYs, TDP is measured as defined in 52.9.10 with an optical channel that meets the requirements listed in Table 75–13.

A 10 Gb/s transmitter is to be compliant with a total dispersion at least as negative as the “minimum dispersion” and at least as positive as the “maximum dispersion” columns specified in Table 75–13 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

75.7.11 Receive sensitivity

Receiver sensitivity is defined for the random pattern test frame, or test pattern 1, or test pattern 3, and an ideal input signal quality with the specified extinction ratio. The measurement procedure is described in 58.7.10 for 1 Gb/s PHYs and 52.9.8 for 10 Gb/s PHYs. The sensitivity shall be met for the bit error ratio defined in Table 75–6, Table 75–7, or Table 75–10 as appropriate.

75.7.12 Stressed receiver conformance test

Compliance with stressed receiver sensitivity is mandatory for the following PMDs: 10GBASE–PR–D1, 10GBASE–PR–D2, 10GBASE–PR–D3, 10GBASE–PR–D4, 10GBASE–PR–U1, 10GBASE–PR–U3, 10GBASE–PR–U4, 10/1GBASE–PRX–D3, 10/1GBASE–PRX–D4, 10/1GBASE–PRX–U1, 10/1GBASE–

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Table 75–13—10 Gb/s transmitter compliance channel specifications

PMD type	Max reach L (km)	Dispersion[a] (ps/nm)		Insertion loss	Optical return loss (dB)
		Minimum	Maximum		
10GBASE–PR–D1 10/1GBASE–PRX–D1	10	0	$0.2325 L\lambda[1–(1300/\lambda)^4]$	Minimum[b]	15
10GBASE–PR–D2 10GBASE–PR–D3 10GBASE–PR–D4 10/1GBASE–PRX–D2 10/1GBASE–PRX–D3 10/1GBASE–PRX–D4	20				
10GBASE–PR–U1	10	$0.2325 L\lambda[1–(1324/\lambda)^4]$	0		
10GBASE–PR–U3 10GBASE–PR–U4	20				

[a]The dispersion is measured for the wavelength of the device under test (λ in nm).
[b]There is no intent to stress the sensitivity of the BERT's optical receiver.

PRX–U2, 10/1GBASE–PRX–U3, and 10/1GBASE–PRX–U4. The stressed receiver conformance test is intended to screen against receivers with poor frequency response or timing characteristics that could cause errors when combined with a distorted but compliant signal. To be compliant with stressed receiver sensitivity, the receiver shall meet the specified bit error ratio at the power level and signal quality defined in Table 75–6, Table 75–7, or Table 75–10 as appropriate, according to the measurement procedures of 58.7.11 for 1 Gb/s PHYs and 52.9.9 for 10 Gb/s PHYs.

75.7.13 Jitter measurements

Jitter measurements for 1 Gb/s are described in 58.7.12. Jitter measurements for 10 Gb/s are described in 52.8.1.

75.7.14 Laser on/off timing measurement

The laser on/off timing measurement procedure is described in 60.9.13.1 with the following changes:

a) T_{on} is defined in 60.9.13.1.1, and its value is less than 512 ns (defined in Table 75–8 and Table 75–9).
b) $T_{receiver\_settling}$ is defined in 60.9.13.2.1, and its value is defined in Table 75–6 and Table 75–7.
c) T_{CDR} is defined in 76.4.2.1, and its value is less than 400 ns.
d) $T_{code\_group\_align}$ is defined in 36.3.2.4, and its value is less than 4 ten bit code–groups for 1 Gb/s PHYs, and is defined as 0 for 10 Gb/s PHYs.
e) T_{off} is defined in 60.9.13.1.1, and its value is less than 512 ns (defined in Table 75–8 and Table 75–9).

75.7.15 Receiver settling timing measurement

75.7.15.1 Definitions

$T_{receiver\_settling}$ is denoted as the time beginning from the time that the optical power in the receiver at TP7 reaches the conditions specified in 75.7.12 and ending at the time that the electrical signal after the PMD at

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TP8 reaches within 15 % of its steady state parameter (average power, jitter) (see Table 75–6 for 10GBASE–PR–D1, 10GBASE–PR–D2, 10GBASE–PR–D3, and 10GBASE–PR–D4, and Table 75–7 for 10/1GBASE–PRX–D1, 10/1GBASE–PRX–D2, 10/1GBASE–PRX–D3, and 10/1GBASE–PRX–D4). $T_{receiver\_settling}$ is presented in Figure 75–7. The data transmitted may be any valid 64B/66B symbols (or a specific power synchronization sequence). The optical signal at TP7, at the beginning of the locking, may have any valid 64B/66B pattern, optical power level, jitter, or frequency shift matching the standard specifications.

75.7.15.2 Test specification

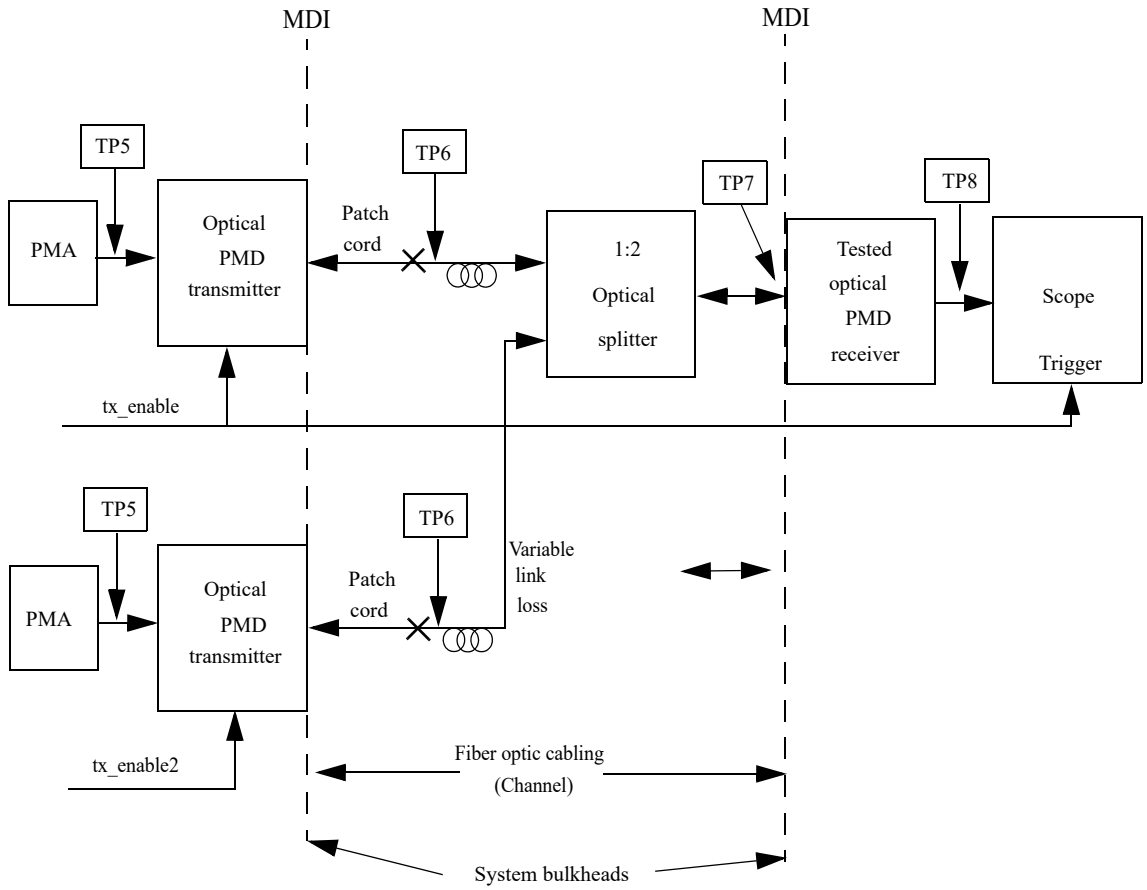

Figure 75–7—Receiver settling time measurement setup

Figure 75–7 illustrates the test setup for the OLT PMD receiver (upstream) $T_{receiver\_settling}$ time. The optical PMD transmitter has well–known parameters, with a fixed known T_{on} time. After T_{on} time the parameters of the reference transmitter, at TP6 and therefore at TP7, reach within 15% of its steady state values as specified in Table 75–8 for 10GBASE–PR–U1, 10GBASE–PR–U3, and 10GBASE–PR–U4 and Table 75–9 for 10/1GBASE–PRX–U1, 10/1GBASE–PRX–U2, 10/1GBASE–PRX–U3, and 10/1GBASE–PRX–U4.

Define $T_{receiver\_settling}$ time as the time from the tx_enable assertion, minus the known T_{on} time, to the time the electrical signal at TP8 reaches within 15% of its steady state conditions.

Conformance should be assured for an optical signal at TP7 with any level of its specified parameters before the tx_enable assertion. Especially the $T_{receiver\_settling}$ time has to be met in the following scenarios:

— Switching from a ‘weak’ (minimal received power at TP7) ONU to a ‘strong’ (maximal received power at TP7) ONU, with minimal guard band between.

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— Switching from a ‘strong’ ONU to a ‘weak’ ONU, with minimal guard band between.
— Switching from noise level, with maximal duration interval, to ‘strong’ ONU power level.

The following procedure is a non-rigorous way to verify the declared $T_{receiver\_settling}$ time.

a) Use a reference transmitter with a known T_{on}.
b) For the PMD receiver under test, measure all PMD receiver electrical parameters at TP8 after $T_{receiver\_settling}$ from the tx_enable trigger minus the reference transmitter T_{on}.
c) Verify the conformance of the measured parameters to within 15% of their specified steady state values.

75.8 Environmental, safety, and labeling

75.8.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

75.8.2 Laser safety

10GBASE–PR and 10/1GBASE–PRX optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825–1 and IEC 60825–2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product’s laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.

75.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

75.8.4 Environment

The 10GBASE–PR and 10/1GBASE–PRX operating environment specifications are as defined in 52.11, as defined in 52.11.1 for electromagnetic emission, and as defined in 52.11.2 for temperature, humidity, and handling.

See Annex 67A for additional environmental information. Two optional temperature ranges are defined in Table 60–15. Implementations shall be declared as compliant over one or both complete ranges, or not so declared (compliant over parts of these ranges or another temperature range).

75.8.5 PMD labeling

The 10GBASE–PR and 10/1GBASE–PRX labeling recommendations and requirements are as defined in 52.12.

Defined PMDs are as follows:

— 10/1GBASE–PRX–D1
— 10/1GBASE–PRX–D2

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— 10/1GBASE–PRX–D3
— 10/1GBASE–PRX–D4
— 10GBASE–PR–D1
— 10GBASE–PR–D2
— 10GBASE–PR–D3
— 10GBASE–PR–D4
— 10/1GBASE–PRX–U1
— 10/1GBASE–PRX–U2
— 10/1GBASE–PRX–U3
— 10/1GBASE–PRX–U4
— 10GBASE–PR–U1
— 10GBASE–PR–U3
— 10GBASE–PR–U4

Each field-pluggable component shall be clearly labeled with its operating temperature range over which compliance is ensured.

75.9 Characteristics of the fiber optic cabling

The 10GBASE–PR and 10/1GBASE–PRX fiber optic cabling shall meet the dispersion specifications defined in IEC 60793–2 and ITU–T G.652, or the requirements of Table 75–14 where they differ. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. It also includes a connector plug at each end to connect to the MDI. The fiber optic cabling spans from one MDI to another MDI, as shown in Figure 75–3.

75.9.1 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 75–3.

NOTE—The optical splitter presented in Figure 75–3 may be replaced by a number of smaller 1:n splitters such that a different topology may be implemented while preserving the link characteristics and power budget as defined in Table 75B–1 and Table 75B–2.

The maximum channel insertion losses shall meet the requirements specified in Table 75–1. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280–4–2:2000. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term *channel* is used here for consistency with generic cabling standards.

75.9.2 Optical fiber and cable

The fiber optic cable requirements are satisfied by the fibers specified in IEC 60793–2 Type B1.1 (dispersion un–shifted SMF) and Type B1.3 (low water peak SMF), ITU–T G.652 and ITU–T G.657 (bend–insensitive SMF), or by the requirements of Table 75–14 where they differ.

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Table 75–14—Optical fiber and cable characteristics

Description[a]	IEC 60793–2 B1.1, B1.3 SMF, ITU–T G.652, G.657 SMF[b]				Unit
Nominal wavelength[c]	1270	1310	1550	1577	nm
Cable attenuation (max)[d]	0.44	0.4	0.35	0.35	dB/km
Zero dispersion wavelength[e]	$1300 \leq \lambda_0 \leq 1324$				nm
Dispersion slope (max)	0.093				$ps/nm^2 \cdot km$

[a]The fiber dispersion values are normative, all other values in the table are optional
[b]Other fiber types are acceptable if the resulting ODN meets channel insertion loss and dispersion requirements.
[c]Wavelength specified is the nominal wavelength and typical measurement wavelength. Power penalties at other wavelengths are accounted for.
[d]Attenuation for single-mode optical fiber cables for 1310 nm and 1550 nm is defined in ITU–T G.652. The attenuation values in the 1270 nm and 1577 nm windows were calculated using spectral attenuation modelling method (5.4.4) included in G.650.1 and the matrix coefficients included in Appendix III therein. 1310 nm (0.4 dB/km), 1380 nm (0.5 dB/km) and 1550 nm (0.35 dB/km) attenuation values were used as the input for the predictor model.
[e]See IEC 60793 or ITU–T G.652.

75.9.3 Optical fiber connection

An optical fiber connection as shown in Figure 75–3 consists of a mated pair of optical connectors. The 10GBASE–PR or 10/1GBASE–PRX PMD is coupled to the fiber optic cabling through an optical connection and any optical splitters into the MDI optical receiver, as shown in Figure 75–3. The channel insertion loss includes the loss for connectors, splices and other passive components such as splitters, see Table 75B–1 and Table 75B–2.

The channel insertion loss was calculated under the assumption of 14.5 dB loss for a 1:16 splitter/18.1 dB loss for a 1:32 splitter (ITU–T G.671 am 1). Unitary fiber attenuation for particular transmission wavelength is provided in Table 75–14. The number of splices/connectors is not predefined; the number of individual fiber sections between the OLT MDI and the ONU MDI is not defined. The only requirements are that the resulting channel insertion loss is within the limits specified in Table 75–1 and the maximum reach in Table 75–1 is not exceeded. Other fiber arrangements (e.g., increasing the split ratio while decreasing the fiber length) are supported as long as the limits for the channel insertion loss specified in Table 75–1 are observed.

The maximum discrete reflectance for single-mode connections shall be less than –26 dB.

75.9.4 Medium Dependent Interface (MDI)

The 10GBASE–PR or 10/1GBASE–PRX PMD is coupled to the fiber cabling at the MDI. The MDI is the interface between the PMD and the “fiber optic cabling” as shown in Figure 75–3. Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a remateable connection, it shall meet the interface performance specifications of IEC 61753–1. The MDI carries the signal in both directions for 10GBASE–PR or 10/1GBASE–PRX PMD and couples to a single fiber.

NOTE—Transmitter compliance testing is performed at TP2 or TP6 as defined in 75.3.2, not at the MDI.

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75.10 Protocol implementation conformance statement (PICS) proforma for Clause 75, Physical Medium Dependent (PMD) sublayer and medium for passive optical networks, type 10GBASE–PR and 10/1GBASE–PRX[138]

75.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 75, Physical Medium Dependent (PMD) sublayer and medium for passive optical networks, type 10GBASE–PR and 10/1GBASE–PRX, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

75.10.2 Identification

75.10.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

75.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 75, Physical Medium Dependent (PMD) sublayer and medium for passive optical networks, type 10GBASE–PR and 10/1GBASE–PRX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required?	No [ ] Yes [ ]
(See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[138]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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75.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
DTX	Transmit delay	75.3.1.1	Delay of 4 TQ (max) with variability 0.5 TQ (max)	M	Yes [ ]
DRX	Receive delay	75.3.1.1	Delay of 4 TQ (max) with variability 0.5 TQ (max)	M	Yes [ ]
HT	High temperature operation	75.8.4	–5 ºC to 85 ºC	O	Yes [ ] No [ ]
LT	Low temperature operation	75.8.4	–40 ºC to 60 ºC	O	Yes [ ] No [ ]
*PR10U	10GBASE–PR–U1 PHY or 10GBASE–PR–U1 PMD	75.5	Maximum channel insertion loss of 20 dB	O/1	Yes [ ] No [ ]
*PR10D	10GBASE–PR–D1 PHY or 10GBASE–PR–D1 PMD	75.4	Maximum channel insertion loss of 20 dB	O/1	Yes [ ] No [ ]
*PR20D	10GBASE–PR–D2 PHY or 10GBASE–PR–D2 PMD	75.4	Maximum channel insertion loss of 24 dB	O/1	Yes [ ] No [ ]
*PR30U	10GBASE–PR–U3 PHY or 10GBASE–PR–U3 PMD	75.5	Maximum channel insertion loss of 29 dB	O/1	Yes [ ] No [ ]
*PR30D	10GBASE–PR–D3 PHY or 10GBASE–PR–D3 PMD	75.4	Maximum channel insertion loss of 29 dB	O/1	Yes [ ] No [ ]
*PR40U	10GBASE–PR–U4 PHY or 10GBASE–PR–U4 PMD	75.5	Maximum channel insertion loss of 33 dB	O/1	Yes [ ] No [ ]
*PR40D	10GBASE–PR–D4 PHY or 10GBASE–PR–D4 PMD	75.4	Maximum channel insertion loss of 33 dB	O/1	Yes [ ] No [ ]
*PRX10U	10/1GBASE–PRX–U1 PHY or 10/1GBASE–PRX–U1 PMD	75.5	Maximum channel insertion loss of 20 dB	O/1	Yes [ ] No [ ]
*PRX10D	10/1GBASE–PRX–D1 PHY or 10/1GBASE–PRX–D1 PMD	75.4	Maximum channel insertion loss of 20 dB	O/1	Yes [ ] No [ ]
*PRX20U	10/1GBASE–PRX–U2 PHY or 10/1GBASE–PRX–U2 PMD	75.5	Maximum channel insertion loss of 24 dB	O/1	Yes [ ] No [ ]
*PRX20D	10/1GBASE–PRX–D2 PHY or 10/1GBASE–PRX–D2 PMD	75.4	Maximum channel insertion loss of 24 dB	O/1	Yes [ ] No [ ]
*PRX30U	10/1GBASE–PRX–U3 PHY or 10/1GBASE–PRX–U3 PMD	75.5	Maximum channel insertion loss of 29 dB	O/1	Yes [ ] No [ ]
*PRX30D	10/1GBASE–PRX–D3 PHY or 10/1GBASE–PRX–D3 PMD	75.4	Maximum channel insertion loss of 29 dB	O/1	Yes [ ] No [ ]
*PRX40U	10/1GBASE–PRX–U4 PHY or 10/1GBASE–PRX–U4 PMD	75.5	Maximum channel insertion loss of 33 dB	O/1	Yes [ ] No [ ]
*PRX40D	10/1GBASE–PRX–D4 PHY or 10/1GBASE–PRX–D4 PMD	75.4	Maximum channel insertion loss of 33 dB	O/1	Yes [ ] No [ ]
*INS	Installation/Cable	75.9	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]

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75.10.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium for passive optical networks, type 10GBASE–PR and 10/1GBASE–PRX

75.10.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FN1	Transmit function	75.3.3	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FN2	Transmitter optical signal	75.3.3	Higher optical power transmitted is a logic 1	M	Yes [ ]
FN3	Receive function	75.3.4	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FN4	Receiver optical signal	75.3.4	Higher optical power received is a logic 1	M	Yes [ ]
FN5	ONU signal detect function	75.3.5.1	Mapping to PMD service interface	M	Yes [ ]
FN6	ONU signal detect parameter	75.3.5.1	Generated according to Table 75–4	M	Yes [ ]
FN7	OLT signal detect function	75.3.5.2	Mapping to PMD service interface	O/2	Yes [ ]
FN8	OLT signal detect function	75.3.5.2	Provided by higher layer	O/2	Yes [ ]
FN9	OLT signal detect parameter	75.3.5.1	Generated according to Table 75–4	O	Yes [ ]

75.10.4.2 PMD to MDI optical specifications for 10GBASE–PR–D1

Item	Feature	Subclause	Value/Comment	Status	Support
PRD1F1	10GBASE–PR–D1 transmitter	75.4.1	Meets specifications in Table 75–5	PR10D:M	Yes [ ] N/A [ ]
PRD1F2	10GBASE–PR–D1 receiver	75.4.2	Meets specifications in Table 75–6	PR10D:M	Yes [ ] N/A [ ]
PRD1F3	10GBASE–PR–D1 receiver damage threshold	75.4.2	If the receiver does not meet the damage requirements in Table 75–6 then label accordingly	PR10D:M	Yes [ ] N/A [ ]

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75.10.4.3 PMD to MDI optical specifications for 10GBASE–PR–D2

Item	Feature	Subclause	Value/Comment	Status	Support
PRD2F1	10GBASE–PR–D2 transmitter	75.4.1	Meets specifications in Table 75–5	PR20D:M	Yes [ ] N/A [ ]
PRD2F2	10GBASE–PR–D2 receiver	75.4.2	Meets specifications in Table 75–6	PR20D:M	Yes [ ] N/A [ ]
PRD2F3	10GBASE–PR–D2 receiver damage threshold	75.4.2	If the receiver does not meet the damage requirements in Table 75–6 then label accordingly	PR20D:M	Yes [ ] N/A [ ]

75.10.4.4 PMD to MDI optical specifications for 10GBASE–PR–D3

Item	Feature	Subclause	Value/Comment	Status	Support
PRD3F1	10GBASE–PR–D3 transmitter	75.4.1	Meets specifications in Table 75–5	PR30D:M	Yes [ ] N/A [ ]
PRD3F2	10GBASE–PR–D3 receiver	75.4.2	Meets specifications in Table 75–6	PR30D:M	Yes [ ] N/A [ ]
PRD3F3	10GBASE–PR–D3 receiver damage threshold	75.4.2	If the receiver does not meet the damage requirements in Table 75–6 then label accordingly	PR30D:M	Yes [ ] N/A [ ]

75.10.4.5 PMD to MDI optical specifications for 10GBASE–PR–D4

Item	Feature	Subclause	Value/Comment	Status	Support
PRD4F1	10GBASE–PR–D4 transmitter	75.4.1	Meets specifications in Table 75–5	PR40D:M	Yes [ ] N/A [ ]
PRD4F2	10GBASE–PR–D4 receiver	75.4.2	Meets specifications in Table 75–6	PR40D:M	Yes [ ] N/A [ ]
PRD4F3	10GBASE–PR–D4 receiver damage threshold	75.4.2	If the receiver does not meet the damage requirements in Table 75–6 then label accordingly	PR40D:M	Yes [ ] N/A [ ]

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75.10.4.6 PMD to MDI optical specifications for 10/1GBASE–PRX–D1

Item	Feature	Subclause	Value/Comment	Status	Support
PRXD1F1	10/1GBASE–PRX–D1 transmitter	75.4.1	Meets specifications in Table 75–5	PRX10D:M	Yes [ ] N/A [ ]
PRXD1F2	10/1GBASE–PRX–D1 receiver	75.4.2	Meets specifications in Table 75–7	PRX10D:M	Yes [ ] N/A [ ]
PRXD1F3	10/1GBASE–PRX–D1 receiver damage threshold	75.4.2	If the receiver does not meet the damage requirements in Table 75–7 then label accordingly	PRX10D:M	Yes [ ] N/A [ ]

75.10.4.7 PMD to MDI optical specifications for 10/1GBASE–PRX–D2

Item	Feature	Subclause	Value/Comment	Status	Support
PRXD2F1	10/1GBASE–PRX–D2 transmitter	75.4.1	Meets specifications in Table 75–5	PRX20D:M	Yes [ ] N/A [ ]
PRXD2F2	10/1GBASE–PRX–D2 receiver	75.4.2	Meets specifications in Table 75–7	PRX20D:M	Yes [ ] N/A [ ]
PRXD2F3	10/1GBASE–PRX–D2 receiver damage threshold	75.4.2	If the receiver does not meet the damage requirements in Table 75–7 then label accordingly	PRX20D:M	Yes [ ] N/A [ ]

75.10.4.8 PMD to MDI optical specifications for 10/1GBASE–PRX–D3

Item	Feature	Subclause	Value/Comment	Status	Support
PRXD3F1	10/1GBASE–PRX–D3 transmitter	75.4.1	Meets specifications in Table 75–5	PRX30D:M	Yes [ ] N/A [ ]
PRXD3F2	10/1GBASE–PRX–D3 receiver	75.4.2	Meets specifications in Table 75–7	PRX30D:M	Yes [ ] N/A [ ]
PRXD3F3	10/1GBASE–PRX–D3 receiver damage threshold	75.4.2	If the receiver does not meet the damage requirements in Table 75–7 then label accordingly	PRXD3F4:M	Yes [ ] N/A [ ]

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75.10.4.9 PMD to MDI optical specifications for 10/1GBASE–PRX–D4

Item	Feature	Subclause	Value/Comment	Status	Support
PRXD4F1	10/1GBASE–PRX–D4 transmitter	75.4.1	Meets specifications in Table 75–5	PRX40D:M	Yes [ ] N/A [ ]
PRXD4F2	10/1GBASE–PRX–D4 receiver	75.4.2	Meets specifications in Table 75–7	PRX40D:M	Yes [ ] N/A [ ]
PRXD4F3	10/1GBASE–PRX–D4 receiver damage threshold	75.4.2	If the receiver does not meet the damage requirements in Table 75–7 then label accordingly	PRX40D:M	Yes [ ] N/A [ ]

75.10.4.10 PMD to MDI optical specifications for 10GBASE–PR–U1

Item	Feature	Subclause	Value/Comment	Status	Support
PRU1F1	10GBASE–PR–U1 transmitter	75.5.1	Meets specifications in Table 75–8	PR10U:M	Yes [ ] N/A [ ]
PRU1F2	10GBASE–PR–U1 receiver	75.5.2	Meets specifications in Table 75–10	PR10U:M	Yes [ ] N/A [ ]
PRU1F3	10GBASE–PR–U1 receiver damage threshold	75.5.2	If the receiver does not meet the damage requirements in Table 75–10 then label accordingly	PR10U:M	Yes [ ] N/A [ ]

75.10.4.11 PMD to MDI optical specifications for 10GBASE–PR–U3

Item	Feature	Subclause	Value/Comment	Status	Support
PRU3F1	10GBASE–PR–U3 transmitter	75.5.1	Meets specifications in Table 75–8	PR30U:M	Yes [ ] N/A [ ]
PRU3F2	10GBASE–PR–U3 receiver	75.5.2	Meets specifications in Table 75–10	PR30U:M	Yes [ ] N/A [ ]
PRU3F3	10GBASE–PR–U3 receiver damage threshold	75.5.2	If the receiver does not meet the damage requirements in Table 75–10 then label accordingly	PR30U:M	Yes [ ] N/A [ ]

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75.10.4.12 PMD to MDI optical specifications for 10GBASE–PR–U4

Item	Feature	Subclause	Value/Comment	Status	Support
PRU4F1	10GBASE–PR–U4 transmitter	75.5.1	Meets specifications in Table 75–8	PR40U:M	Yes [ ] N/A [ ]
PRU4F2	10GBASE–PR–U4 receiver	75.5.2	Meets specifications in Table 75–10	PR40U:M	Yes [ ] N/A [ ]
PRU4F3	10GBASE–PR–U4 receiver damage threshold	75.5.2	If the receiver does not meet the damage requirements in Table 75–10 then label accordingly	PR40U:M	Yes [ ] N/A [ ]

75.10.4.13 PMD to MDI optical specifications for 10/1GBASE–PRX–U1

Item	Feature	Subclause	Value/Comment	Status	Support
PRXU1F1	10/1GBASE–PRX–U1 transmitter	75.5.1	Meets specifications in Table 75–9	PRX10U:M	Yes [ ] N/A [ ]
PRXU1F2	10/1GBASE–PRX–U1 receiver	75.5.2	Meets specifications in Table 75–10	PRX10U:M	Yes [ ] N/A [ ]
PRXU1F3	10/1GBASE–PRX–U1 receiver damage threshold	75.5.2	If the receiver does not meet the damage requirements in Table 75–10 then label accordingly	PRX10U:M	Yes [ ] N/A [ ]

75.10.4.14 PMD to MDI optical specifications for 10/1GBASE–PRX–U2

Item	Feature	Subclause	Value/Comment	Status	Support
PRXU2F1	10/1GBASE–PRX–U2 transmitter	75.5.1	Meets specifications in Table 75–9	PRX20U:M	Yes [ ] N/A [ ]
PRXU2F2	10/1GBASE–PRX–U2 receiver	75.5.2	Meets specifications in Table 75–10	PRX20U:M	Yes [ ] N/A [ ]
PRXU2F3	10/1GBASE–PRX–U2 receiver damage threshold	75.5.2	If the receiver does not meet the damage requirements in Table 75–10 then label accordingly	PRX20U:M	Yes [ ] N/A [ ]

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75.10.4.15 PMD to MDI optical specifications for 10/1GBASE–PRX–U3

Item	Feature	Subclause	Value/Comment	Status	Support
PRXU3F1	10/1GBASE–PRX–U3 transmitter	75.5.1	Meets specifications in Table 75–9	PRX30U:M	Yes [ ] N/A [ ]
PRXU3F2	10/1GBASE–PRX–U3 receiver	75.5.2	Meets specifications in Table 75–10	PRX30U:M	Yes [ ] N/A [ ]
PRXU3F3	10/1GBASE–PRX–U3 receiver damage threshold	75.5.2	If the receiver does not meet the damage requirements in Table 75–10 then label accordingly	PRX30U:M	Yes [ ] N/A [ ]

75.10.4.16 PMD to MDI optical specifications for 10/1GBASE–PRX–U4

Item	Feature	Subclause	Value/Comment	Status	Support
PRXU4F1	10/1GBASE–PRX–U4 transmitter	75.5.1	Meets specifications in Table 75–9	PRX40U:M	Yes [ ] N/A [ ]
PRXU4F2	10/1GBASE–PRX–U4 receiver	75.5.2	Meets specifications in Table 75–10	PRX40U:M	Yes [ ] N/A [ ]
PRXU4F3	10/1GBASE–PRX–U4 receiver damage threshold	75.5.2	If the receiver does not meet the damage requirements in Table 75–10 then label accordingly	PRX40U:M	Yes [ ] N/A [ ]

75.10.4.17 Definitions of optical parameters and measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	75.7.1	2 m to 5 m in length	M	Yes [ ]
OM2	Wavelength, spectral width, and SMSR	75.7.4	Per the centroidal wavelength, RMS spectral width, and SMSR definitions in IEC 61280-1-3 under modulated conditions.	M	Yes [ ]
OM3	Average optical power	75.7.5	Per IEC 61280-1-1.	M	Yes [ ]
OM4	Extinction ratio	75.7.6	Per ANSI/TIA/EIA–526–4A with minimal back reflections and fourth-order Bessel–Thomson receiver.	M	Yes [ ]
OM5	Optical modulation amplitude (OMA) test procedure	75.7.7	As described in 58.7.5 for 1 Gb/s PHY and in 52.9.5 for 10 Gb/s PHY.	M	Yes [ ]
OM6	$RIN_x OMA$	75.7.8	As described in 58.7.7for 1 Gb/s PHY and in 52.9.6 for 10 Gb/s PHY	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
OM7	Transmit optical waveform (transmit eye)	75.7.9	Per ANSI/TIA/EIA–526–4A with test pattern and fourth-order Bessel–Thomson receiver.	M	Yes [ ]
OM8	Transmitter and dispersion penalty	75.7.10	As described in 58.7.7 for 1 Gb/s PHY and in 52.9.6 for 10 Gb/s PHY.	M	Yes [ ]
OM9	Receive sensitivity	75.7.11	As described in 58.7.10 for 1 Gb/s PHY and in 52.9.8 for 10 Gb/s PHY. Values defined in Table 75–6, Table 75–7, or Table 75–10 as appropriate.	M	Yes [ ]
*OM10	Stressed receiver conformance test	75.7.12	As described in 58.7.11 for 1 Gb/s PHY and in 52.9.9 for 10 Gb/s PHY. Values defined in Table 75–6, Table 75–7, or Table 75–10 as appropriate.	O	Yes[ ] N/A[ ]
OM11	Jitter measurements	75.7.13	As described in 58.7.12 for 1 Gb/s PHY and in 52.8.1 for 10 Gb/s PHY.	M	Yes [ ]
OM12	Laser On/Off timing measurement	75.7.14	As described in 60.9.13.1 for 1 Gb/s PHY and in 60.9.13.1 with modifications defined in 75.7.14 for 10 Gb/s PHY.	M	Yes [ ]
OM13	Receiver settling timing measurement	75.7.15	As described in 60.9.13.2 for 1 Gb/s and 10 Gb/s PHY.	O	Yes [ ] No [ ]

75.10.4.18 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
FO1	Fiber optic cabling	75.9	Specified in Table 75–14	INS:M	Yes [ ] N/A[ ]
F02	End –to–end channel loss	75.9	Meeting the requirements of Table 75B–1 and Table 75B–2	INS:M	Yes [ ] N/A[ ]
FO3	Maximum discrete reflectance – single-mode fiber	75.9.3	Less than –26 dB	INS:M	Yes [ ] N/A [ ]
FO4	MDI requirements	75.9.4	Meet the interface performance specifications of IEC 61753–1, if remateable	INS:O	Yes [ ] No [ ] N/A [ ]

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75.10.4.19 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	75.8.1	Conforms to J.2	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	75.8.2	Conform to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Documentation	75.8.2	Explicitly defines requirements and usage restrictions to meet safety certifications	M	Yes [ ]
ES4	Operating temperature range labeling	75.8.5	If required	M	Yes [ ] N/A[ ]

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76. Reconciliation Sublayer, Physical Coding Sublayer, and Physical Media Attachment for 10G-EPON

76.1 Overview

This clause describes the Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS) with FEC, and Physical Medium Attachment (PMA) used with 10GBASE-PR and 10/1GBASE-PRX point-to-multipoint (P2MP) networks. These are passive optical multipoint networks (PONs) that connect multiple DTEs using a single shared fiber. The architecture is asymmetric, based on a tree and branch topology utilizing passive optical splitters. This type of network requires that the Multipoint MAC Control sublayer exists above the MACs, as described in Clause 77.

76.1.1 Conventions

The notation used in the state diagrams in this clause follows the conventions in 21.5. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation ++ after a counter indicates it is to be incremented by 1. The notation −− after a counter indicates it is to be decremented by 1. The notation −= after a counter indicates that the counter value is to be decremented by the following value. The notation += after a counter indicates that the counter value is to be incremented by the following value. Code examples given in this clause adhere to the style of the “C” programming language.

76.1.2 Delay constraints

The MPCP relies on strict timing based on the distribution of timestamps. The actual delay is implementation dependent but an implementation shall maintain a combined delay variation through RS, PCS, and PMA sublayers of no more than 1 time_quantum (see 77.2.2.1) so as not to interfere with the MPCP timing.

76.2 Reconciliation Sublayer (RS) for 10G-EPON

76.2.1 Overview

This subclause extends Clause 46 to enable multiple MACs to interface with a single Physical Layer, and to enable data links with one data rate (e.g., 10 Gb/s) in one direction but another (e.g., 1 Gb/s) in the opposite direction. The number of MACs supported is limited only by the implementation. It is acceptable for only one MAC to be connected to this Reconciliation Sublayer. Figure 76–1 and Figure 76–2 show the relationship between this RS and the ISO/IEC OSI reference model. The mapping of GMII/XGMII signals to PLS service primitives is described in 35.2.1 for GMII and 46.1.7 for XGMII with exceptions noted herein.

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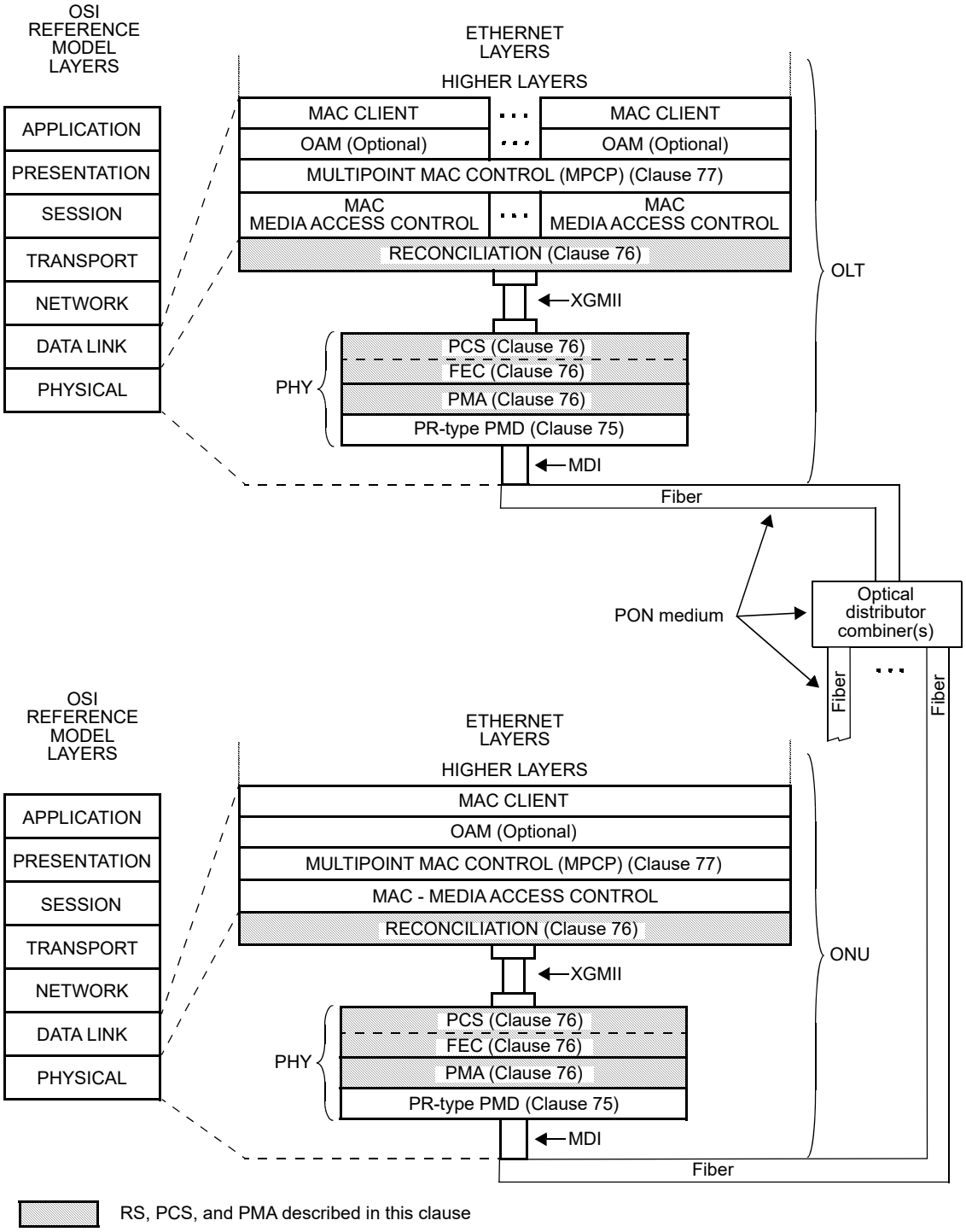

Figure 76–1—Relationship of 10/10G-EPON P2MP RS, PCS, and PMA to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

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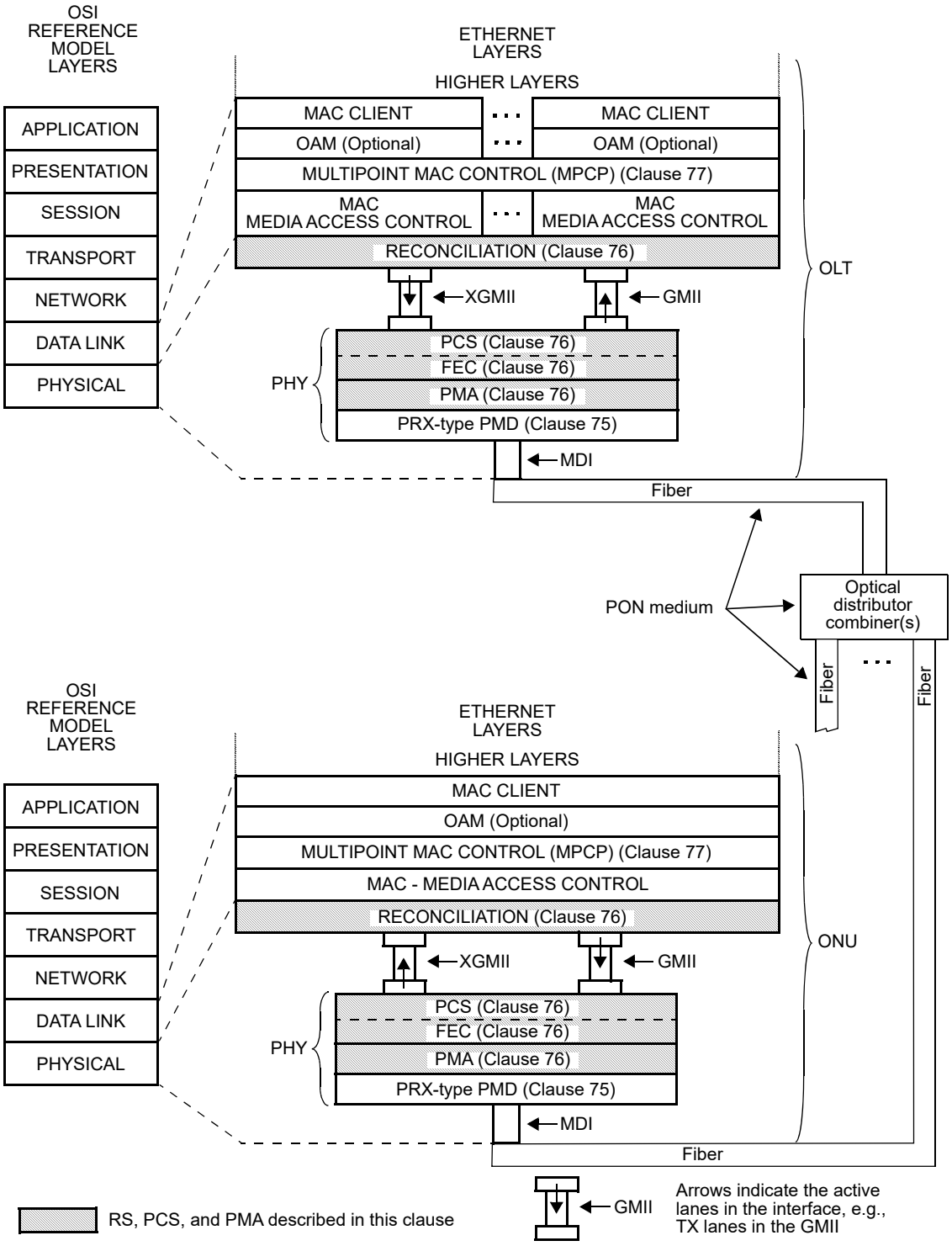

XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 76–2—Relationship of 10/1G-EPON P2MP RS, PCS, and PMA to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

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76.2.2 Dual-speed Media Independent Interface

In 1G-EPON architectures, the GMII is the interface used to transfer data between the RS and the PCS. For 10/10G-EPON architectures, the XGMII is the interface used to transfer data between the RS and the PCS. When using a 10/1G-EPON architecture, a combination of both GMII and XGMII is needed in order to support transmission and reception at different speeds. Through the parallel use of the GMII and XGMII, the following modes are supported:

— Symmetric-rate 10 Gb/s operation for transmit and receive data paths, utilizing all of the functionality of the XGMII defined in Clause 46.
— Symmetric-rate 1 Gb/s operation for transmit and receive data paths, utilizing all of the functionality of the GMII defined in Clause 35.
— Asymmetric-rate operation for transmit and receive data paths at the OLT, utilizing transmit path functionality of the XGMII defined in Clause 46 and receive path functionality of the GMII defined in Clause 35.
— Asymmetric-rate operation for transmit and receive data paths at the ONU, utilizing transmit path functionality of the GMII defined in Clause 35 and receive path functionality of the XGMII defined in Clause 46.
— Coexistence of various ONU types by utilizing different data paths within the OLT.

76.2.2.1 10/10G-EPON

Figure 76–3(a) depicts the data paths used in 10/10G-EPON.

76.2.2.2 10/1G-EPON

At the OLT, the transmit path uses XGMII signals TXD<31:0>, TXC<3:0> and TX_CLK, while the receive path uses GMII signals RXD<7:0>, RX_ER, RX_CLK, and RX_DV. At the ONU, the transmit path uses GMII signals TXD<7:0>, TX_EN, TX_ER, and GTX_CLK, while the receive path uses XGMII signals RXD<31:0>, RXC<3:0> and RX_CLK.

Figure 76–3(b) depicts the data paths used in 10/1G-EPON.

76.2.2.3 Dual-rate mode

To support coexistence of 10/10G-EPON, 10/1G-EPON, and 1G-EPON ONUs on the same outside plant, the OLT may optionally support dual-rate mode. Dual-rate mode supports transmission and reception at both 10 Gb/s and 1 Gb/s. When operating in a dual-rate mode, a combination of XGMII and GMII data paths are used for transmission and reception. Figure 76–4 depicts the data paths used in an OLT operating in a dual-rate mode.

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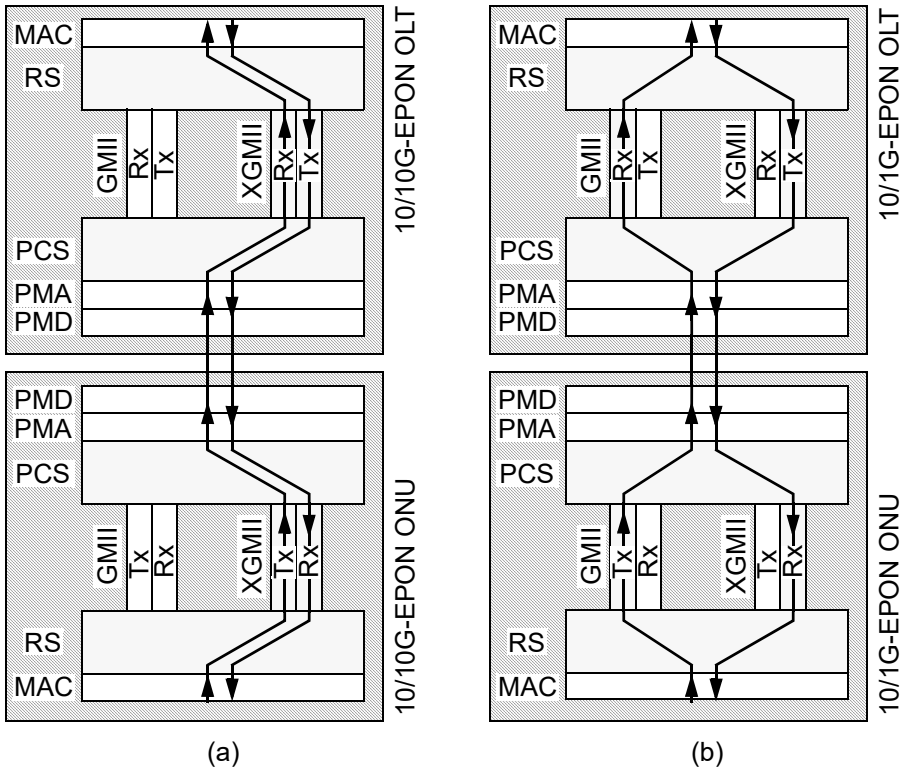

Figure 76–3—10/10G-EPON (a) and 10/1G-EPON (b) operation of OLT and ONU

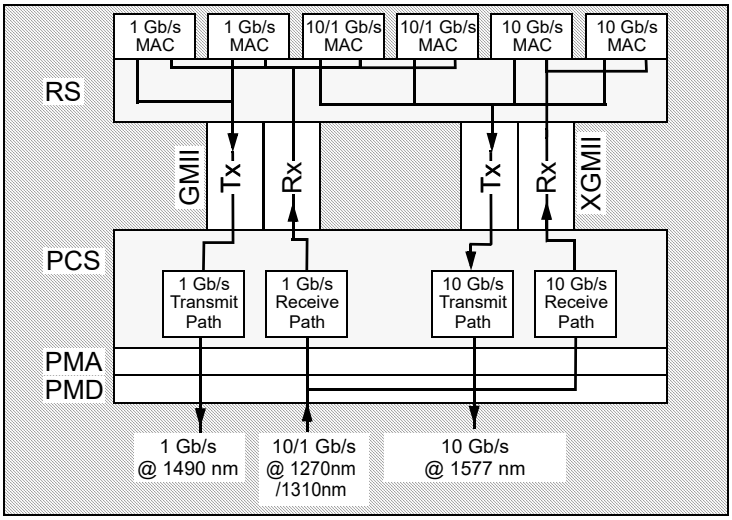

Figure 76–4—PCS and Reconciliation Sublayer for dual rate mode at OLT

76.2.2.4 Mapping of XGMII and GMII primitives

The mapping of XGMII/GMII signals to the PLS_DATA.request and PLS_DATA.indication primitives is described in 76.2.6. Additional details are provided in Table 76–1, which shows the mapping of PLS_-DATA.request primitives to transmit interface signals for different types of OLTs and ONUs. Table 76–2 shows the mapping of PLS_DATA.indication primitives to receive interface signals for different types of OLTs and ONUs.

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76.2.3 Summary of major concepts

A successful registration process, described in 77.3.3, results in the assignment of values to the MODE and LLID variables associated with a MAC. This may be one of many MACs in an OLT or a single MAC in an ONU. The MODE and LLID variables are used to identify a packet transmitted from that MAC and how received packets are directed to that MAC. The RS in the OLT shall operate in unidirectional mode as defined in 66.4.

As described in 77.1.2, multiple MACs within an OLT are bound to a single XGMII in the case of a 10/10G-EPON OLT, or to an XGMII transmit path and a GMII receive path in the case of a 10/1G-EPON OLT. Only one PLS_DATA.request primitive is active at any time.

At the ONU, the MAC is either bound to an XGMII in the case of a 10/10G-EPON ONU, or to an XGMII receive path and a GMII transmit path in case the of an 10/1G-EPON ONU.

In the transmit direction, the RS maps the active PLS_DATA.request to either the GMII signals (TXD<7:0>, TX_EN, TX_ER, and GTX_CLK) or the XGMII signals (TXD<31:0>, TXC<3:0>, and TX_CLK) according to the MAC instance generating the request. The RS replaces octets of preamble with the values of the transmitting MAC's MODE and LLID variables.

In the receive direction, the MODE and LLID values embedded within the preamble identify the MAC to which this packet should be directed. The RS establishes a temporal mapping of either the GMII signals (RXD<7:0>, RX_ER, RX_CLK, and RX_DV) or the XGMII signals (RXD<31:0>, RXC<3:0> and RX_CLK) to the correct PLS_DATA.indication and PLS_DATA_VALID.indication primitives.

76.2.3.1 Application

This subclause applies to the interface between the MAC and PHY in an OLT or an ONU. The physical implementation of the interface is primarily intended to be chip-to-chip, but may also be used as a logical interface between ASIC logic modules within an integrated circuit. These interfaces are used to provide media independence, so that an identical media access controller may be used with all 10GBASE-PR and 10/1GBASE-PRX PHY types.

76.2.4 GMII structure

See Clause 35.

76.2.5 XGMII structure

The XGMII structure is discussed in 46.1.6, and Figure 46–2 depicts a schematic view of the RS inputs and outputs.

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76.2.6 Mapping of XGMII and GMII signals to PLS service primitives

Except as noted in Table 76–1 and Table 76–2, the mapping of the signals provided at the XGMII to the PLS service primitives is defined in 46.1.7.

Table 76–1—Mapping of PLS_DATA.request primitive

MAC location	MAC operating speed	Transmit interface	Signals
OLT	1G-EPON (Tx: 1 Gb/s)	GMII	TXD<7:0>, TX_EN, TX_ER, GTX_CLK
OLT	10/10G-EPON (Tx: 10 Gb/s)	XGMII	TXD<31:0>, TXC<3:0>, TX_CLK
OLT	10/1G-EPON (Tx: 10 Gb/s)	XGMII	TXD<31:0>, TXC<3:0>, TX_CLK
ONU	1G-EPON (Tx: 1 Gb/s)	GMII	TXD<7:0>, TX_EN, TX_ER, GTX_CLK
ONU	10/10G-EPON (Tx: 10 Gb/s)	XGMII	TXD<31:0>, TXC<3:0>, TX_CLK
ONU	10/1G-EPON (Tx: 1 Gb/s)	GMII	TXD<7:0>, TX_EN, TX_ER, GTX_CLK

Table 76–2—Mapping of PLS_DATA.indication primitive

MAC location	MAC operating speed	Receive interface	Signals
OLT	1G-EPON (Rx: 1 Gb/s)	GMII	RXD<7:0>, RX_ER, RX_DV, RX_CLK
OLT	10/10G-EPON (Rx: 10 Gb/s)	XGMII	RXD<31:0>, RXC<3:0>, RX_CLK
OLT	10/1G-EPON (Rx: 1 Gb/s)	GMII	RXD<7:0>,RX_ER,RX_DV,RX_CLK
ONU	1G-EPON (Rx: 1 Gb/s)	GMII	RXD<7:0>, RX_ER, RX_DV, RX_CLK
ONU	10/10G-EPON (Rx: 10 Gb/s)	XGMII	RXD<31:0>, RXC<3:0>, RX_CLK
ONU	10/1G-EPON (Rx: 10 Gb/s)	XGMII	RXD<31:0>, RXC<3:0>, RX_CLK

76.2.6.1 Functional specifications for multiple MACs

76.2.6.1.1 Variables

The variables of 65.1.3.1 are inherited except as shown below.

logical_link_id
: Value: 15 bits
This variable shall be set to the broadcast value of 0x7FFE for the unregistered ONU MAC.
Enabled OLT MACs may use any value for this variable. If the optional multicast LLID feature is supported, the OLT may use a multicast_link_id along with the mode bit set to 0.
Registered ONU MACs may use any value other than the reserved values listed in Table 76–4 or a multicast_link_id for this variable.

76.2.6.1.2 RS Transmit function

The transmit function is described in 65.1.3.2 except as noted below in Table 76–3, which shows the replacement mapping for 10G-EPON. The XGMII transmit function is described in 46.3.1.

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Table 76–3—Preamble/SFD replacement mapping

Column	Lane	Field	Preamble/SFD	Modified preamble/SFD
0	0	—	0x55	Same
	1	—	0x55	Same
	2	SLD	0x55	0xD5
	3	—	0x55	Same
1	0	—	0x55	Same
	1	LLID[15:8]	0x55	<mode, logical_link_id[14:8]>[a]
	2	LLID[7:0]	0x55	<logical_link_id[7:0]>[b]
	3	CRC8	0xD5	The 8 bit CRC calculated over column 0 lane 2 through column 1 lane 2

[a]mode maps to TXD[15], logical_link_id[14] maps to TXD[14], logical_link_id[8] maps to TXD[8].
[b]logical_link_id[7] maps to TXD[23], logical_link_id[0] maps to TXD[16].

76.2.6.1.3 RS Receive function

The receive function is described in 65.1.3.3 except as noted below.

Table 65–2 is not applicable to 10G-EPON.

76.2.6.1.3.1 SLD

The 10 Gb/s RS transmit function maintains an alignment for its start control character to lane 0. The SLD is transmitted as the third octet and therefore is aligned to lane 2 in the same column containing the start control character. This is the only possibility considered when parsing the incoming octet stream for the SLD. If the SLD field is not found then the packet shall be discarded. If the packet is transferred, the SLD shall be replaced with a normal preamble octet and the two octets preceding the SLD and the one octet following the SLD are passed without modification. See Table 76–3.

76.2.6.1.3.2 LLID

This subclause supersedes the stipulations of 65.1.3.3.2.

The third and fourth octets following the SLD contain the mode and logical_link_id values. OLTs and ONUs act upon these values in a different manner.

If the device is an OLT, then the following comparison is made:

a) The received mode bit is ignored.
b) If the received logical_link_id value matches 0x7FFF or 0x7FFE and an enabled MAC exists with a logical_link_id variable with the same value, then the comparison is considered a match to that MAC.
c) If the received logical_link_id has a value other than 0x7FFF or 0x7FFE and an enabled MAC exists with a mode variable with a value of 0 and a logical_link_id variable matching the received logical_link_id value, then the comparison is considered a match to that MAC.

If the device is an ONU then the following comparison is made:

d) If the received mode bit is equal to 0 and the received logical_link_id value matches the logical_link_id variable, then the comparison is considered a match.

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e) If the received mode bit is equal to 1 and the received logical_link_id value does not match the logical_link_id variable, or the received logical_link_id matches 0x7FFE, then the comparison is considered a match.
f) If the received logical_link_id value matches one of the assigned multicast LLIDs, then the comparison is considered a match.

If no match is found, then the packet shall be discarded within the RS. If a match is found, then the packet is intended to be transferred. If the packet is transferred, then both octets of the LLID field shall be replaced with normal preamble octets.

If the packet is transferred, the one octet preceding the LLID is passed without modification. A number of LLIDs have been allocated (see Figure 76–4) for various purposes including downstream broadcast, discovery messages, and upstream registration request messages. An additional block of LLIDs has been set aside for future use and definition. A registered ONU shall not transmit frames with one of these reserved LLIDs.

Table 76–4—LLID values

LLID value	Used in RS	Purpose
0x7FFF	1000BASE-PX	Downstream: 1 Gb/s SCB Upstream: ONU registration at 1 Gb/s
0x7FFE	10/1GBASE-PRX	Downstream: 10 Gb/s SCB Upstream: ONU registration at 1 Gb/s
	10GBASE-PR	Downstream: 10 Gb/s SCB Upstream: ONU registration at 10 Gb/s
	10GPASS-XR	Downstream: EPoC SCB Upstream: CNU registration
0x7FFD–0x7F00	—	Reserved for future use

76.2.6.1.3.3 CRC-8

The CRC-8 field is as described in 65.1.3.3.3.

76.3 Physical Coding Sublayer (PCS) for 10G-EPON

76.3.1 Overview

This subclause defines the physical coding sublayers 10GBASE-PR and 10/1GBASE-PRX, supporting burst mode operation over the point-to-multipoint physical medium. The 10GBASE-PR PCS is specified to support 10/10G EPON, where both the receive and transmit paths operate at 10 Gb/s rate. The 10/1GBASE-PRX PCS supports 10/1G-EPON, in which OLT transmit path and ONU receive path operate at 10 Gb/s, while the ONU transmit path and the OLT receive path operate at 1 Gb/s rate.

This subclause also specifies a forward error correction (FEC) mechanism to increase the optical link budget or the fiber distance. Figure 76–1 and Figure 76–2 show the relationship between the PCS sublayer and the ISO/IEC OSI reference model.

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76.3.1.1 10/1GBASE-PRX PCS

Conceptually, the 10/1GBASE-PRX PCS represents a combination of transmit and receive functions defined in the 10GBASE-PR PCS (specified in this clause) and the 1000BASE-PX PCS (specified in Clause 65). At the OLT, the 10/1GBASE-PRX consists of the 10GBASE-PR transmit function and the 1000BASE-PX receive function (see Figure 76–5). Reciprocally, at the ONU, the 10/1GBASE-PRX PCS consists of the 10GBASE-PR receive function and the 1000BASE-PX transmit function (see Figure 76–6).

Deriving a specification for the 10/1GBASE-PRX PCS from the 10GBASE-PR PCS and the 1000BASE-PX PCS specifications as described previously is a straightforward process; therefore, no further explicit specification for the 10/1GBASE-PRX PCS is necessary.

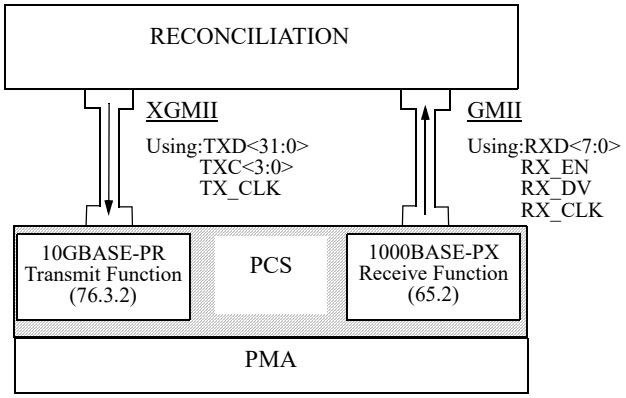

Figure 76–5—Conceptual diagram of 10/1GBASE-PRX PCS, OLT Side

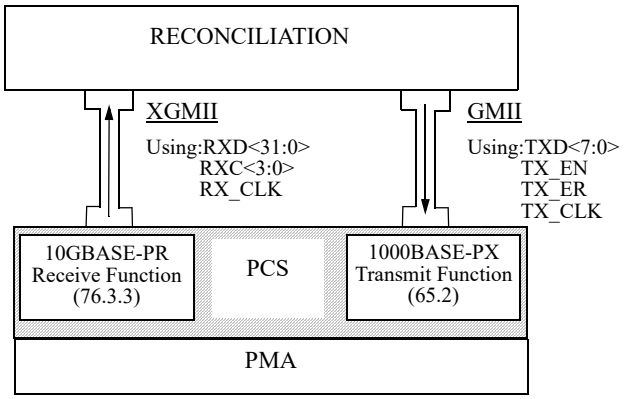

Figure 76–6—Conceptual diagram of 10/1GBASE-PRX PCS, ONU Side

76.3.1.2 10GBASE-PR PCS

The 10GBASE-PR PCS extends the physical coding sublayer described in Clause 49 to support burst mode operation over the point-to-multipoint physical medium. Figure 76–7 illustrates the functional block diagram of the downstream path and Figure 76–8 shows the functional block diagram of the upstream path.

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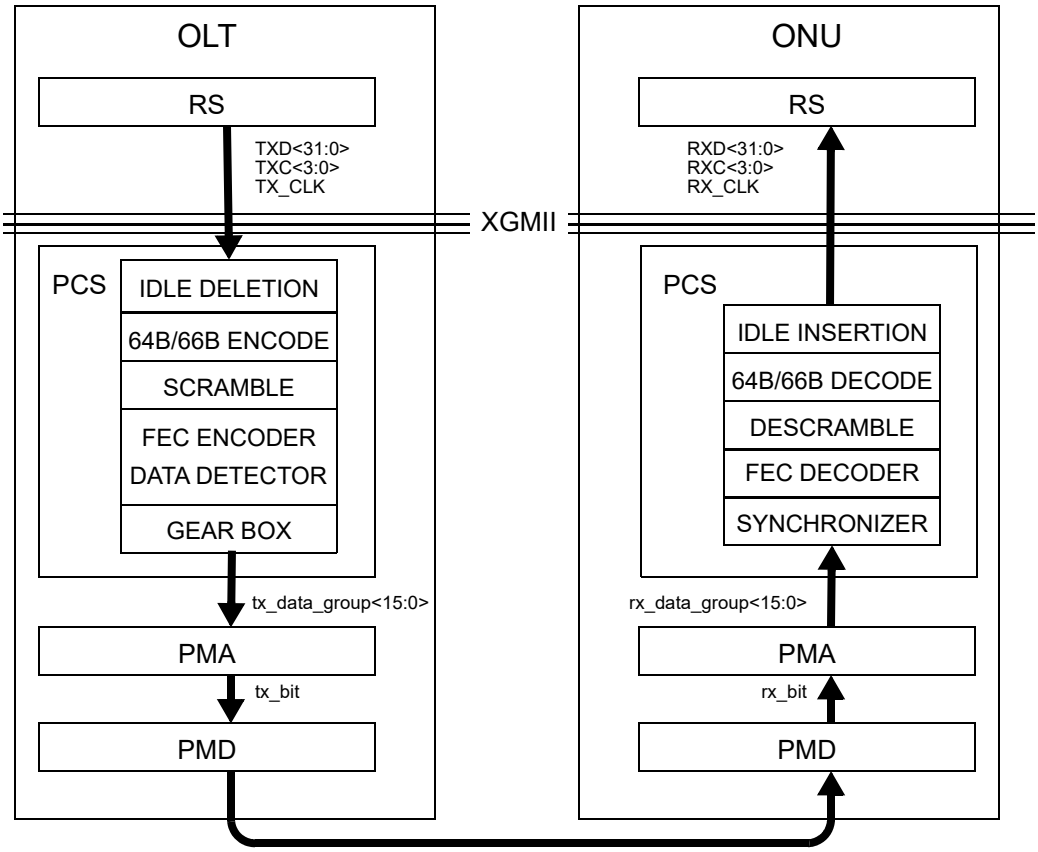

Figure 76–7—PCS functional block diagram, downstream path

76.3.2 PCS transmit function

This subclause defines the transmit direction of the physical coding sublayers for 10GBASE-PR and 10/1GBASE-PRX. In the OLT, the PCS transmit function operates at a 10 Gb/s rate in a continuous mode. In the ONU, the PCS transmit function may operate at a 10 Gb/s rate, as specified herein (10GBASE-PR), or at a 1 Gb/s rate, as specified in Clause 65 (10/1GBASE-PRX). For both 10GBASE-PR and 10/1GBASE-PRX, the ONU PCS always operates in a burst mode in the transmit direction. When operating at the 10 Gb/s rate, the PCS includes a mandatory FEC encoder. Figure 76–7 illustrates the transmit direction of OLT PCS. Figure 76–8 illustrates the transmit direction of the ONU PCS.

76.3.2.1 Idle control character deletion

The Idle Deletion process is responsible for deleting excess Idle characters to allow the parity data to be inserted without increasing the PMD line rate. This process deletes four 72 bit vectors containing Idle characters per every thirty-one 72 bit vectors received from the XGMII. The MPCP function ensures that sufficient Idle characters occur so that the minimum IPG is always preserved between two adjacent packets.

The Idle Deletion process is depicted in Figure 76–9 for OLTs and in Figure 76–10 for ONUs.

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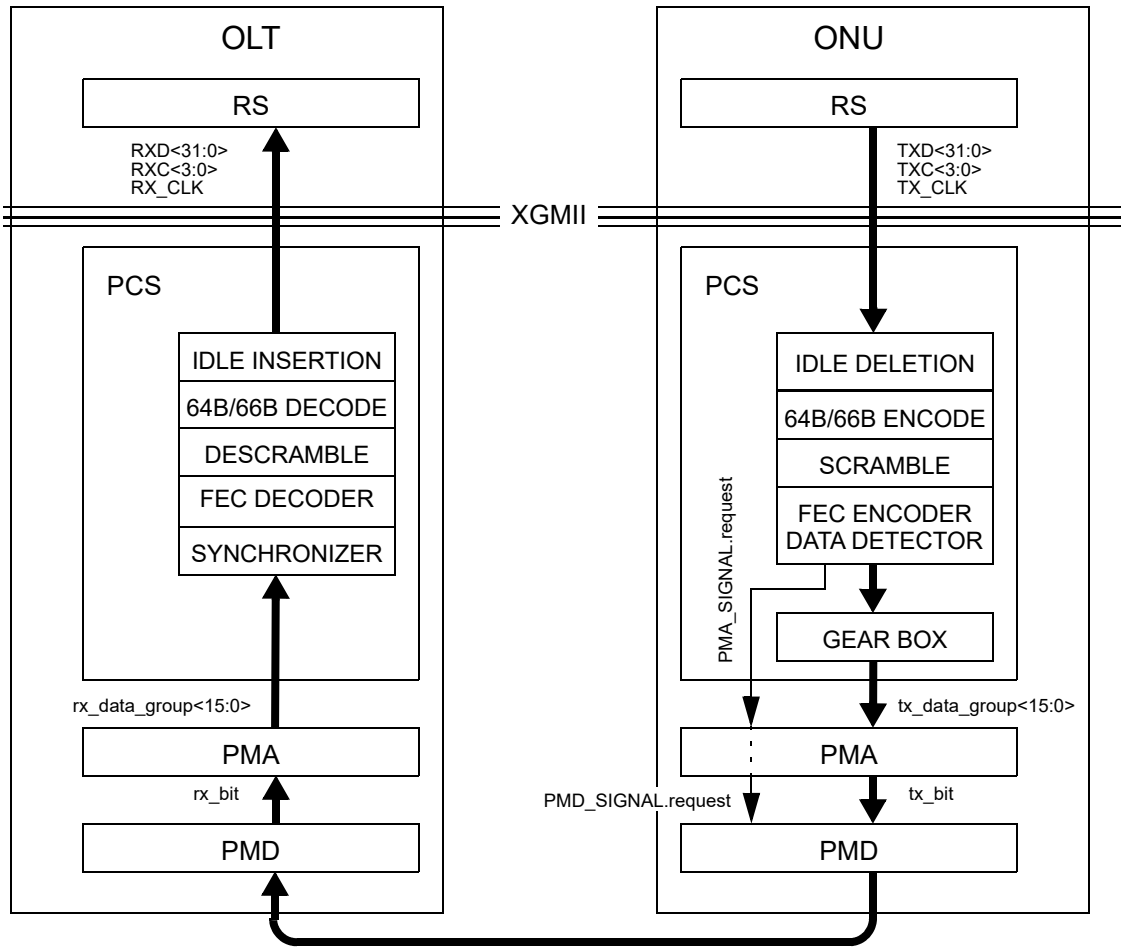

Figure 76–8—PCS functional block diagram, upstream path

76.3.2.1.1 Constants

FEC_DSize

TYPE: 16 bit unsigned

The number of 72 bit vectors constituting a payload of an FEC codeword. To normalize pre-FEC data rate, the Idle Deletion function removes FEC_PSize vectors per every FEC_DSize vectors transferred to the 64B/66B encoder.

Value: 27

FEC_PSize

TYPE: 16 bit unsigned

The number of 72 bit vectors constituting parity portion of an FEC codeword. To normalize pre-FEC data rate, the Idle Deletion function removes FEC_PSize vectors per every FEC_DSize vectors transferred to the 64B/66B encoder.

Value: 4

76.3.2.1.2 Variables

BEGIN

TYPE: Boolean

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This variable is used when initiating operation of the state diagram. It is set to true following initialization and every reset.

DelayBound
TYPE: 16 bit unsigned
This value represents the delay sufficient to initiate the laser and to stabilize the receiver at the OLT (i.e., the maximum FIFO size expressed in 66 bit blocks). The value includes LaserOnTime (77.3.3.2), $T_{receiver\_settling}$, T_{CDR}, Burst Delimiter, and the two 66 bit blocks containing Idles, that precede the first packet in the burst. This variable is used only by the ONU.

tx_raw<71:0>
This variable is defined in 49.2.13.2.2.

tx_raw_out<71:0>
72 bit vector sent from the output of the Idle Deletion function to the 64B/66B encoder. The vector contains two XGMII transfers mapped as shown for tx_raw<71:0>.

76.3.2.1.3 Functions

T_TYPE(tx_raw<71:0>)
This function is defined in 49.2.13.2.3.

76.3.2.1.4 Counters

DelCount
TYPE: 16 bit unsigned
Counts the number of 72 bit vectors that need to be deleted.

IdleCount
TYPE: 16 bit unsigned
Counts the number of 72 bit vectors containing Idle control characters or other control vectors.

VectorCount
TYPE: 16 bit unsigned
Counts the number of 72 bit vectors transmitted.

76.3.2.1.5 State diagrams

The OLT PCS shall perform the Idle Deletion process as shown in Figure 76–9. The ONU PCS shall perform the Idle Deletion process as shown in Figure 76–10. Should there be a discrepancy between a state diagrams and descriptive text, the state diagrams prevail.

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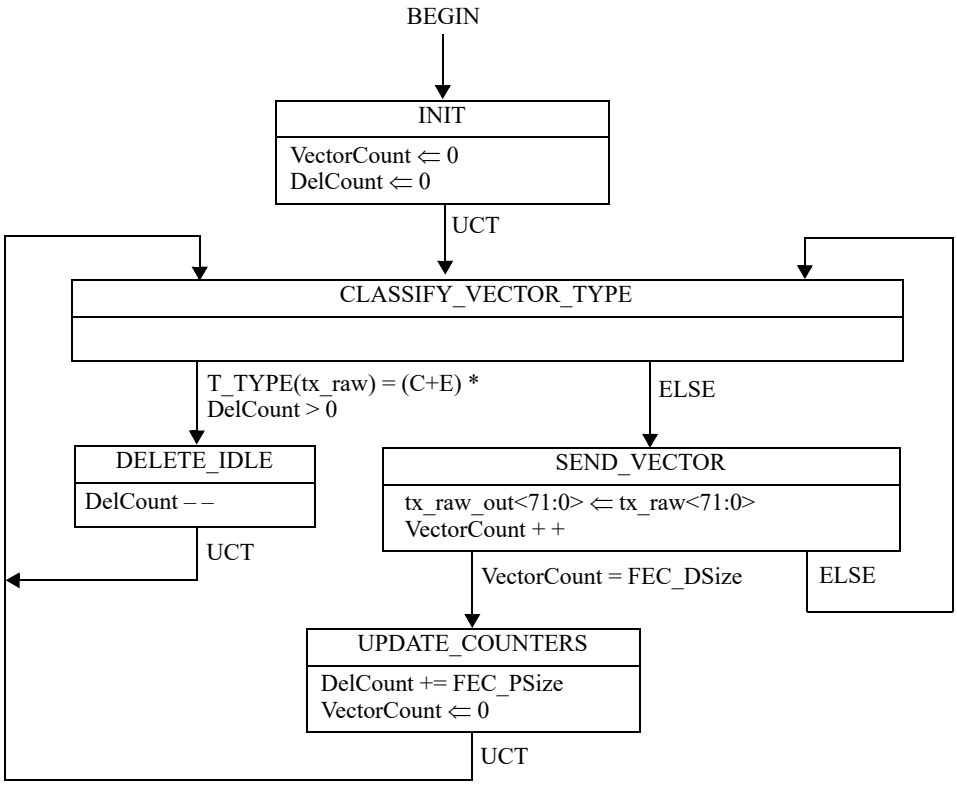

Figure 76–9—OLT Idle Deletion state diagram

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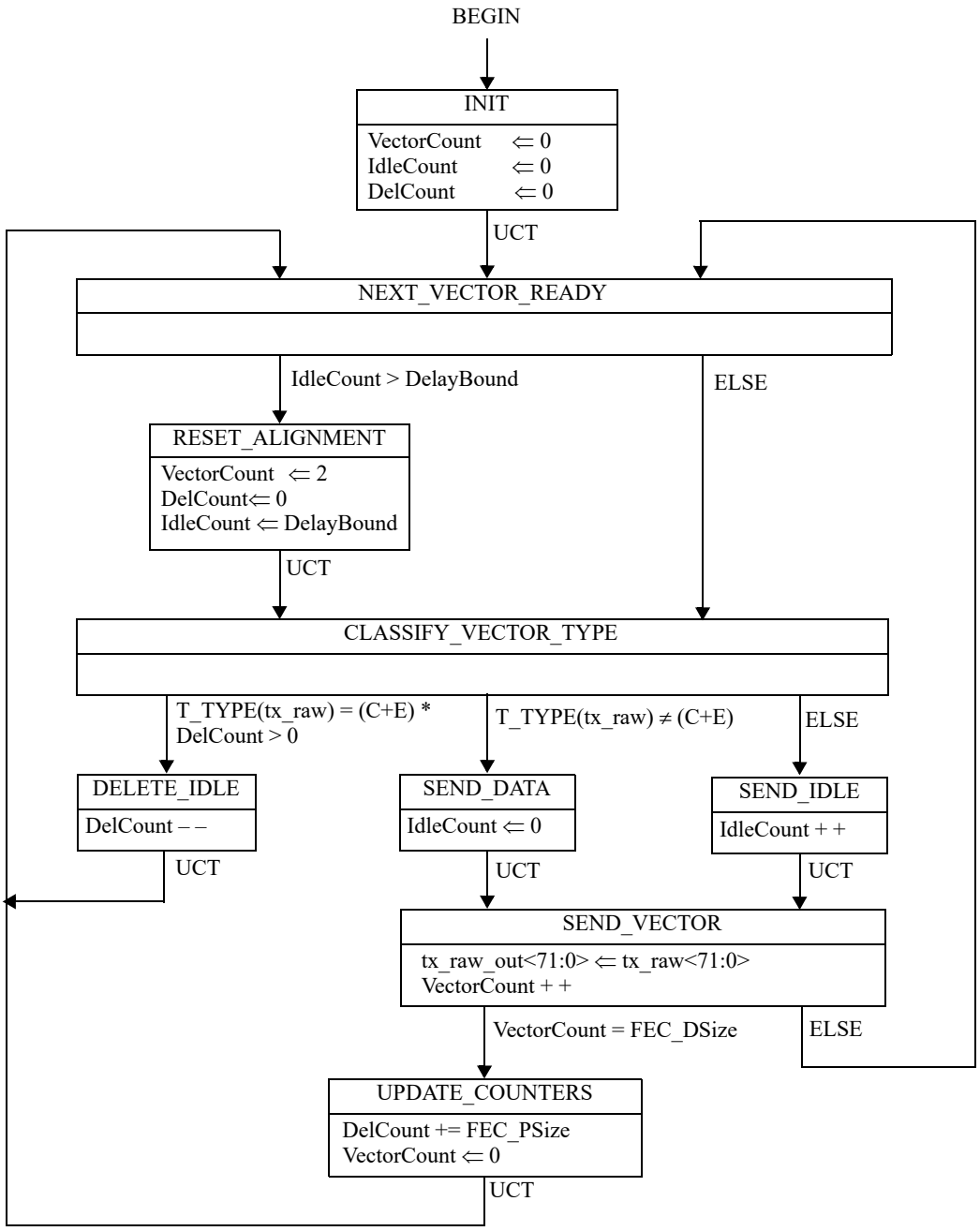

Figure 76–10—ONU Idle Deletion state diagram

76.3.2.2 64B/66B Encode

See 49.2.4 64B/66B transmission code. The encoder shall perform the functions specified in the state diagram shown in Figure 49–16.

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76.3.2.3 Scrambler

See 49.2.6 Scrambler.

76.3.2.4 FEC encoding

The 10GBASE-PR-D, 10GBASE-PR-U, and 10/1GBASE-PRX-D PCS shall encode the transmitted data stream using Reed-Solomon code (255,223). Annex 76A gives an example of RS(255,223) FEC Encoding.

76.3.2.4.1 FEC Algorithm [RS(255,223)]

The FEC code used for 10GBASE-PR links is a linear cyclic block code—the Reed-Solomon code (255, 223) over the Galois Field of GF(2^8)—a code operating on 8 bit symbols. The code encodes 223 information symbols and adds 32 parity symbols. The code is systematic, meaning that the information symbols are not disturbed in any way in the encoder and the parity symbols are added separately to each block.

The code is based on the generating polynomial shown in Equation (76-1).

$$G(Z) = \prod_{i=0}^{31}(Z - \alpha^i) = A_{32}Z^{32} + A_{31}Z^{31} + \ldots + A_0Z^0 \quad (76\text{–}1)$$

where

α is a root of the binary primitive polynomial $x^8 + x^4 + x^3 + x^2 + 1$ and is represented as 0x02
A is a series representing the resulting polynomial coefficients of $G(Z)$, (A_{32} is equal to 0x01)
Z corresponds to an 8 bit GF(2^8) symbol
x corresponds to a bit position in a GF(2^8) symbol

The parity calculation shall produce the same result as the shift register implementation shown in Figure 76–11. Before calculation begins, the shift register shall be initialized to zero. The contents of the shift register are transmitted without inversion.

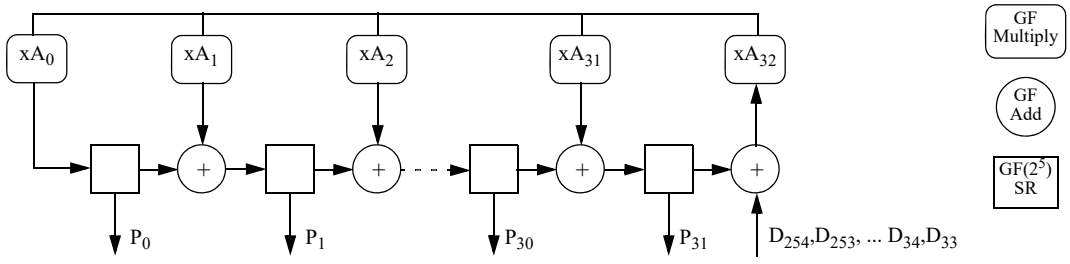

Figure 76–11—Circuit for generating FEC parity vector

An FEC parity vector is represented by Equation (76-2).

$$P(Z) = D(Z) \bmod G(Z) \quad (76\text{–}2)$$

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where

$D(Z)$ is the data vector $D(Z) = D_{222}Z^{254} + D_{221}Z^{253} + \ldots + D_0Z^{32}$. D_{222} is the first data octet and D_0 is the last.

$P(Z)$ is the parity vector $P(Z) = P_{31}Z^{31} + P_{30}Z^{30} \ldots + P_0Z^0$. P_{31} is the first parity octet and P_0 is the last.

A data octet $(d_7, d_6, \ldots, d_1, d_0)$ is identified with the element: $d_7\alpha^7 + d_6\alpha^6 + \ldots + d_1\alpha^1 + d_0$ in GF(2^8), the finite field with 2^8 elements. The code has a correction capability of up to sixteen symbols.

NOTE—For the (255,223) Reed-Solomon code, the symbol size equals one octet. The d_0 is identified as the LSB and d_7 is identified as the MSB for all octets in accordance with the conventions of 3.1.1.

Bit ordering shall be as illustrated in Figure 76–12.

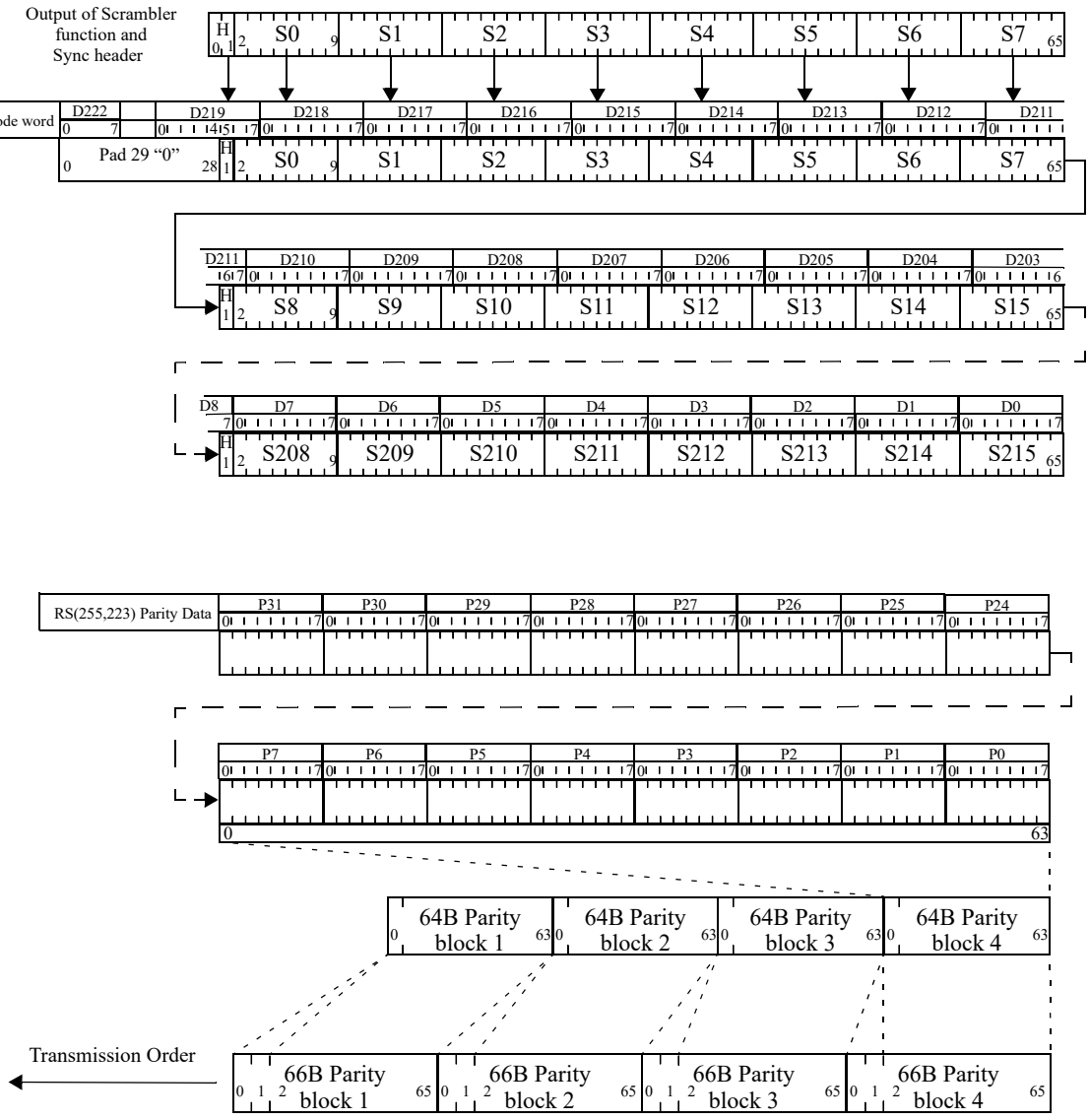

Figure 76–12—Bit ordering in FEC codeword generation

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76.3.2.4.2 Parity calculation

Padding of FEC codewords and appending FEC parity octets in the 10GBASE-PR and 10/1GBASE-PRX OLT PCS transmitter is illustrated in Figure 76–13. The 64B/66B encoder and scrambler produce 66 bit blocks. The FEC encoder accumulates 27 of these 66 bit blocks to form the basis of an FEC codeword, removing the redundant first bit (i.e., sync header bit <0>) of each block (the first bit is guaranteed to be the complement of the second bit).

The FEC encoder then prepends 29 padding bits (binary 0) to the 27 blocks (65 bits each) to form the 223-octet payload portion of an FEC codeword. This data is then FEC-encoded, resulting in the 32-octet parity portion of the FEC codeword. The 223-octet payload portion and 32-octet parity portion combine to form the 255-octet Reed-Solomon codeword. The padding is used to generate the FEC codeword but is not transmitted.

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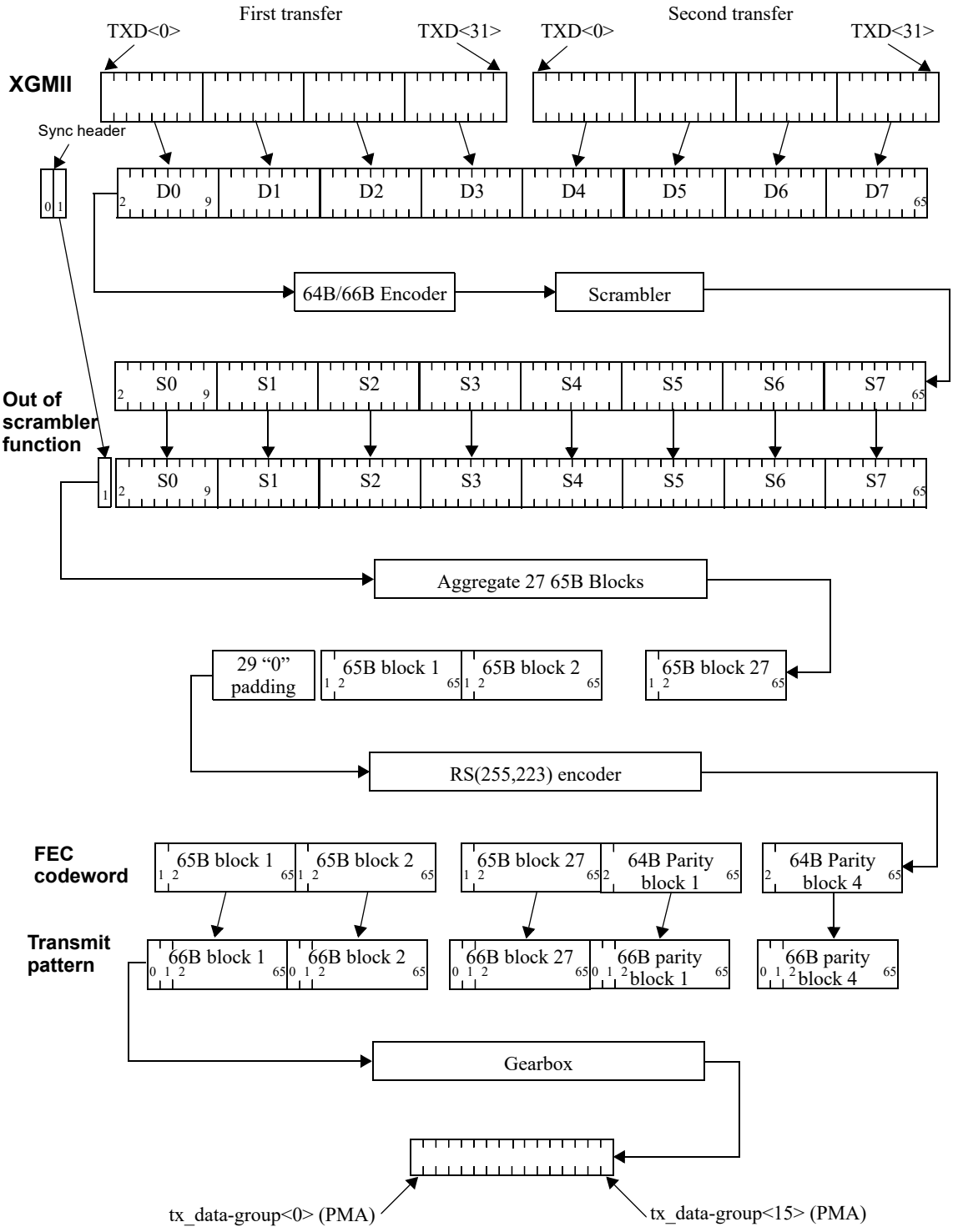

Figure 76–13—PCS Transmit bit ordering

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76.3.2.4.3 FEC Transmission Block Formatting

As shown in Figure 76–13, after the Reed-Solomon codeword has been computed, the FEC encoder constructs the transmittable FEC codeword with the original sequence of twenty-seven 66 bit blocks (including the redundant sync bit, but not including the 29 “0” padding bits). The FEC encoder prepends a 2 bit sync header to each group of 64 parity bits to construct a properly formed 66 bit codeword, according to the predefined sync header pattern for the four 64 bit parity blocks: 00 11 11 00. Finally the four 66 bit parity blocks are appended following the twenty-seven 66 bit data blocks and transmitted to the PMA.

76.3.2.5 Data Detector

The 10GBASE-PR-D, 10GBASE-PR-U, and 10/1GBASE-PRX-D PCS transmit path includes the Data Detector process. This process contains a delay line (FIFO_DD buffer) that stores the 66 bit blocks to allow insertion of the FEC parity data into the transmitted data stream. The length of the FIFO_DD buffer should be large enough to hold the amount of data equal to the maximum amount of parity data that may be inserted within the transmission time of one packet of a maximum length (i.e., at most forty 66 bit blocks of parity data).

76.3.2.5.1 Burst Mode operation (ONU only)

In addition to inserting the parity data into the data stream, the Data Detector process in the 10GBASE-PR-U PCS generates the PMA_SIGNAL.request(tx_enable) primitive to turn the laser on and off at the correct times.

Upon initialization, the laser is turned off. When the first 66 bit block containing data arrives at the buffer, the Data Detector sets the PMA_SIGNAL.request(tx_enable) primitive to the value ON, instructing the PMD sublayer to start the process of turning the laser on.

When the buffer becomes empty (i.e., contains only 66 bit blocks with Idle characters), the Data Detector sends the End of Burst Delimiter and after that sets the PMA_SIGNAL.request(tx_enable) primitive to the value OFF, instructing the PMD sublayer to start the process of turning the laser off. Between packets, Idle blocks arrive at the buffer. If the number of these Idle blocks is insufficient to fill the buffer then the laser is not turned off.

The length of the FIFO_DD buffer at the ONU shall be chosen such that the delay introduced by the buffer together with any delay introduced by the PMA sublayer is long enough to turn the laser on and to allow a laser synchronization pattern, Burst Delimiter pattern, and a predefined number of Idle blocks to be transmitted. The laser synchronization pattern allows the receiving optical detector to adjust its gain ($T_{receiver\_settling}$) and synchronize its receive clock (T_{CDR}). The Burst Delimiter allows the receiver to easily identify the beginning of FEC protected portion of the ONU transmission. The Idle control characters are used to synchronize the descrambler and establish start-of-packet delineation.

Figure 76–14 illustrates the details of the ONU burst transmission. In particular, this figure shows the details of the synchronization time and the FEC protected portions of the burst transmission.

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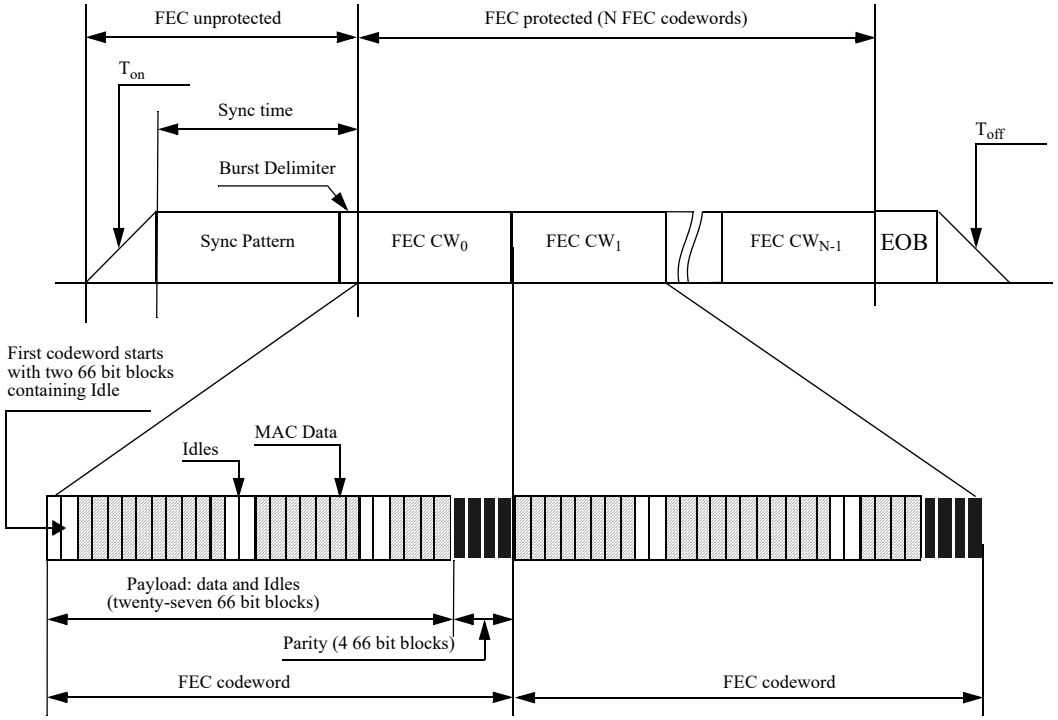

Figure 76–14—Details of burst composition

The ONU burst transmission begins with a Synchronization Pattern (see 76.3.2.5.2), which facilitates receiver clock recovery and gain control at the OLT. To facilitate FEC codeword synchronization, the ONU transmits a 66 bit BURST_DELIMITER (see Figure 76–15). When received at the OLT, the BURST_DELIMITER allows for FEC codeword alignment on the incoming data stream, even in the presence of bit errors. The BURST_DELIMITER is followed by two 66 bit blocks containing Idle codes. The first 66 bit block is used to synchronize the descrambler and a second 66 bit block is needed to provide packet delineation at the RS layer of the OLT. These two 66 bit Idle blocks are part of the first FEC codeword.

The ONU burst transmission ends with an END_BURST_DELIMITER (EOB) pattern of length TERMINATOR_LENGTH (see Figure 76–15). When received at the OLT, the burst terminator allows for the rapid reset of the OLT FEC synchronizer, so that it can search for the next burst. The burst terminator is not part of the last FEC codeword.

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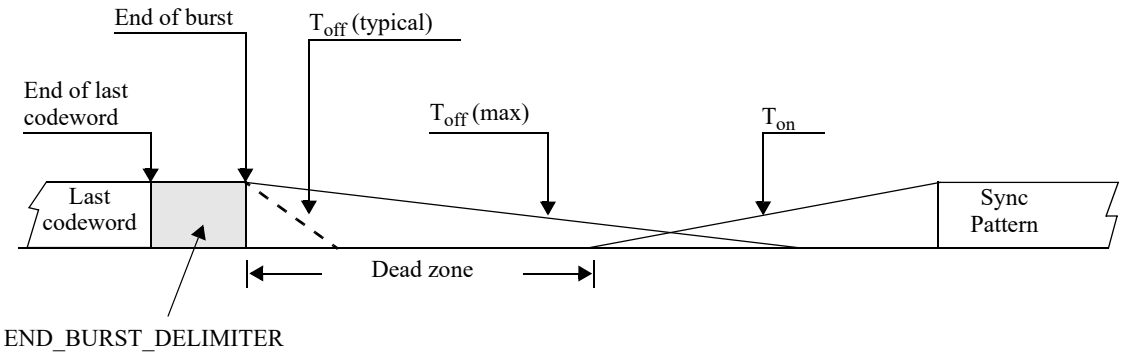

Figure 76–15—ONU burst transmission termination

The body of this subclause comprises state diagrams, including the associated definitions of variables, constants, and functions pertinent to the 10GBASE-PR and 10/1GBASE-PRX OLT PCS transmitters. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams in this clause follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value.

76.3.2.5.2 Constants

BURST_DELIMITER
: TYPE: 66 bit unsigned
A 66 bit value used to find the beginning of the first FEC codeword in the upstream burst.
Value: binary 01 followed by 0x 6B F8 D8 12 D8 58 E4 AB (transmission bit sequence: 01 1101 0110 0001 1111 0001 1011 0100 1000 0001 1011 0001 1010 0010 0111 1101 0101)

END_BURST_DELIMITER
: TYPE: 66 bit unsigned
A 66 bit value used to identify the end of the upstream burst transmission.
Value: binary 10 followed by 0x 55 55 55 55 55 55 55 55 (transmission bit sequence of 10 1010 1010 1010 1010 1010 1010 1010 1010 1010 1010 1010 1010 1010 1010 1010 1010)

FEC_DSize
: See 76.3.2.1.1.

FEC_PSize
: See 76.3.2.1.1.

SP
: Type: 66 bit unsigned
A 66 bit value used to for the burst mode synchronization pattern.
Value: binary 10 followed by 0x BF 40 18 E5 C5 49 BB 59 (transmission bit sequence 10 1111 1101 0000 0010 0001 1000 1010 0111 1010 0011 1001 0010 1101 1101 1001 1010)

TERMINATOR_LENGTH
: Type: 8 bit unsigned
Number of END_BURST_DELIMITER blocks that are transmitted at the end of each burst.
Value: 3

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SH_DATA
Type: 2-bit unsigned
The value of synchronization header indicating that the given 66-bit block is a data block, as defined in 49.2.4.3.
Value: 0x02 (binary representation 10)

SH_CTRL
Type: 2-bit unsigned
The value of synchronization header indicating that the given 66-bit block is a control block, as defined in 49.2.4.3.
Value: 0x01 (binary representation 01)

NOTE—The binary representation of the sync header in here is different than that in Clause 49. In Clause 49, binary values are shown with the first transmitted bit (the LSB) on the left.

76.3.2.5.3 Variables

CLK
TYPE: Boolean
This Boolean is true on every negative edge of TX_CLK (See 46.3.1) and represents instances of time at which a 66 bit block should be passed from Data Detector to the GearBox. This variable is reset to false upon read.

DelayBound
This variable is defined in 76.3.2.1.2.

FIFO_DD
TYPE: Array of 66 bit unsigned elements
A FIFO array used to store tx_coded<65:0> blocks while the parity is inserted and while burst preamble is generated (at the ONU only).

FifoSize
TYPE: 16 bit unsigned
Variable representing a number of elements stored in FIFO_DD.

SyncLength
TYPE: 16 bit unsigned
Required number of sync blocks per burst. The value of this variable is derived from the syncTime (excluding BURST_DELIMITER) and laserOnTime parameters defined in 77.3.3.

Transmitting
TYPE: Boolean
Boolean variable indicating whether the device is transmitting or not. At the ONU, the default value of Transmitting is false. At the OLT, this variable is always set to true.

tx_coded<65:0>
TYPE: 66 bit unsigned
66 bit block containing the output of the scrambler. The format for this vector is shown in Figure 49–7. The left-most bit in the figure is tx_coded<0> and the right-most bit is tx_coded<65>.

tx_coded_out<65:0>
TYPE: 66 bit unsigned

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66 bit block containing the output of Data Detector being passed to the Gearbox. The format for this vector is shown in Figure 49–7. The left-most bit in the figure is tx_coded<0> and the right-most bit is tx_coded<65>.

76.3.2.5.4 Functions

RemoveFifoHead()

This function removes the first block in FIFO_DD and decrements the variable FifoSize by 1.

```
RemoveFifoHead()
   {
      // shift FIFO_DD forward
      FIFO_DD[0] = FIFO_DD[1]
      FIFO_DD[1] = FIFO_DD[2]
          ...
      FIFO_DD[FifoSize-2] = FIFO_DD[FifoSize-1]
      FifoSize --
   }
```

76.3.2.5.5 Messages

PMA_SIGNAL.request(tx_enable)

This primitive is used to turn the laser on and off at the PMD sublayer. In the OLT, this primitive shall always take the value ON. In the ONU, the value of this variable is controlled by the Data detector state diagram (see Figure 76–17).

SCRAMBLER_UNITDATA.request(tx_coded<65:0>)

A primitive generated by the SCRAMBLER transmit process conveying the next 66 bit block to be transmitted.

SUDR

Alias for SCRAMBLER_UNITDATA.request(tx_coded<65:0>).

76.3.2.5.6 Counters

IdleBlockCount

TYPE: 32-bit signed integer

The number of consecutive non-data blocks ending with the most recently received block. The non-data blocks are represented by sync header 10 (binary).

ParityBlockCount

TYPE: 8 bit unsigned

The number of parity blocks transmitted in a current FEC codeword. After reaching the full parity size (FEC_PSize=4), this counter is reset to 0.

ProtectedBlockCount

TYPE: 8 bit unsigned

The number of blocks added to a payload of a current FEC codeword. After reaching the full payload size (FEC_DSize = 27), this counter is reset to 0.

SyncBlockCount

TYPE: 16 bit unsigned

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The number of synchronization blocks transmitted in current burst.

76.3.2.5.7 State diagrams

The OLT and the ONU shall implement the Data Detector input process as depicted in Figure 76–16. The OLT shall implement the Data Detector output process as depicted in Figure 76–17(a). The ONU shall implement the Data Detector output process as depicted in Figure 76–17(b).

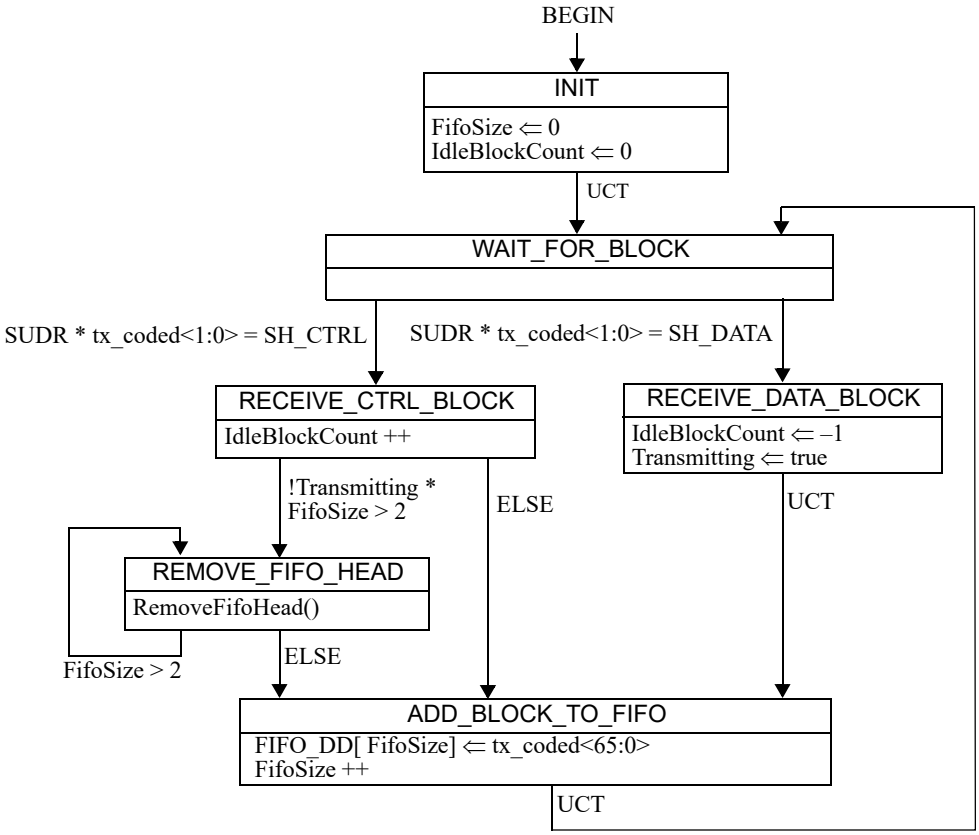

Figure 76–16—Data Detector, input process state diagram

76.3.2.6 Gearbox

See 49.2.7 Gearbox.

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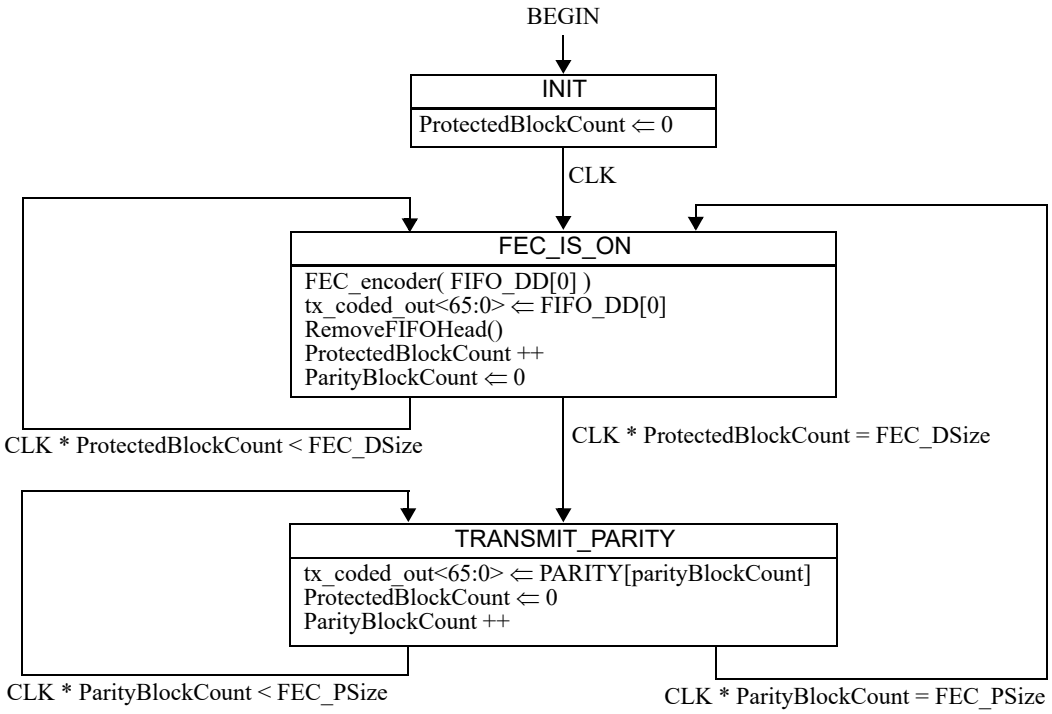

(a) OLT state diagram

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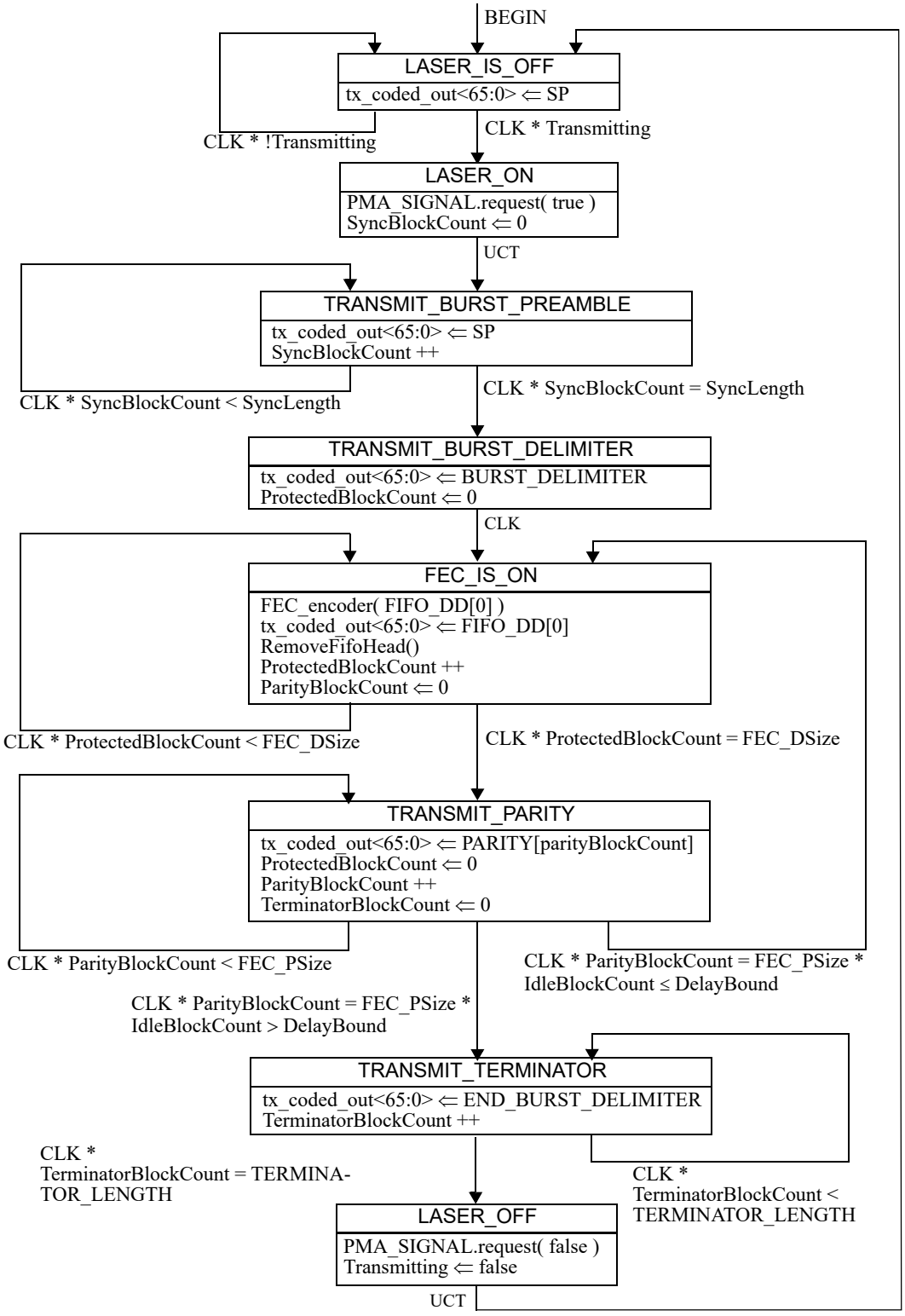

(b) ONU state diagram

Figure 76–17—Data Detector, output process state diagram

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76.3.3 PCS receive Function

This subclause defines the receive direction of physical coding sublayers for 10GBASE-PR and 10/1GBASE-PRX. In the ONU, the PCS operates at a 10 Gb/s rate in a continuous mode. In the OLT, the PCS may operate at a 10 Gb/s rate, as specified herein (10GBASE-PR), or at a 1 Gb/s rate, compliant with Clause 65 (10/1GBASE-PRX). For both 10GBASE-PR and 10/1GBASE-PRX, the OLT PCS always operates in burst mode. When operating at the 10 Gb/s rate, the PCS includes a mandatory FEC decoder. The receive direction of ONU PCS is illustrated in Figure 76–7 and receive direction for the OLT PCS is illustrated in Figure 76–8.

76.3.3.1 OLT synchronizer

The OLT codeword synchronization function receives data via the 16 bit PMA_UNITDATA.indication primitive.

The OLT synchronizer forms a bit stream from the primitives by concatenating requests with the bits of each primitive in order from rx_data-group<0> to rx_data-group<15> (see Figure 76–18). It obtains lock to the thirty-one 66 bit blocks in the bit stream by looking for the burst delimiter. Lock is obtained as specified in the codeword lock state diagram shown in Figure 76–18. While in codeword lock, the synchronizer copies the FEC-protected bits from each data block and the parity bits of the codeword into an input buffer. When the codeword is complete, the FEC decoder is triggered, and the input buffer is freed for the next codeword. When in codeword lock, the state diagram looks for the end of the burst. When this is observed, then the state diagram deasserts codeword lock. The state diagram then goes back to searching for the burst delimiter.

76.3.3.1.1 Variables

BD_valid
: TYPE:Boolean
Indication that is set true if received block rx_coded matches the BURST_DELIMITER with less than 12 bits difference, and de-asserted otherwise.

cword_lock
: TYPE: Boolean
Boolean variable that is set true when receiver acquires codeword delineation.

CurrentBlock<65:0>
: TYPE: 66 bit vector
The last 66 bit block received. This variable has an initial value of 0.

decode_success
: TYPE: Boolean
Indication that is set true if the codeword was successfully decoded by the FEC algorithm, and false otherwise.

EOB_valid
: TYPE: Boolean
Indication that is set true if:

$$\text{DistanceFromEob}(\text{CurrentBlock}) + \text{DistanceFromEob}(\text{PreviousBlock}) < 11$$

It is set to false otherwise.

inbuffer
: TYPE: bit array
An array of 2040 bits that holds the input to the FEC decoder.

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input_buffer_location
TYPE: integer
An integer that points to the next appending location in the input buffer.

persist_dec_fail
TYPE: Boolean
Indication that is set when three consecutive decoding failures have occurred.

PreviousBlock<65:0>
TYPE: 66 bit vector
The 66 bit block received previous to the current block. This variable has an initial value of 0.

reset
This variable is inherited from 49.2.13.2.2.

rx_coded<65:0>
This variable is inherited from 49.2.13.2.2.

signal_ok
This variable is inherited from 49.2.13.2.2.

76.3.3.1.2 Counters

decode_failures
TYPE:
Counter that holds the number of consecutive decoding failures.

sh_wndw_cnt
Count of the number of sync headers checked within the current 62-block window (composed of 2 codewords of 31 blocks each).

76.3.3.1.3 Functions

Append_inbuffer()
Appends the newly arrived 66 bit block into the input buffer of the FEC decoding algorithm, taking care to only insert the bits to be protected, and discarding the unwanted bits.

```
Append_inbuffer()
{
   BlockFromPMA()
   if (sh_wndw_cnt<27)
   {
      inbuffer[input_buffer_location]=rx_coded<1>
      input_buffer_location++
   }
   for(i=2, i<66, i++)
   {
      inbuffer[input_buffer_location]=rx_coded<i>
      input_buffer_location++
   }
}
```


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BlockFromPMA()

Function that accepts the next received data from the PMA. Conceptually, this function serializes the 16 bit rx_data_group<15:0> to a bit stream at 10.3125 Gb/s, and then deserializes the resulting bit stream into a 66 bit wide rx_coded<65:0> block of data. It does not return until 66 bits have been transferred. Note that the internal design by which this function is accomplished is an implementation choice; however, the design operates such that a new 66 bit block is made available at the regular interval of 6.4 ns, and the transfers are made synchronous to the XGMII clock.

Decode()

Triggers the FEC decoding algorithm to accept the contents of the input buffer, and do its decoding work. Note that this function is not blocking, and returns immediately. It is assumed that the FEC decoding algorithm copies the input buffer contents into its own internal memory, so that the input buffer is released to accept the next codeword.

DecodeWhenReady()

Determines if the inbuffer contains a full codeword, and if so, it triggers the Decode function, and then clears the inbuffer for the next codeword.

```
DecodeWhenReady()
{
   if (sh_wndw_cnt=0 or sh_wndw_cnt=31)
   {
      if (cword_lock)
      {
         Decode();
      }
      Flush_inbuffer();
   }
}
```

DistanceFromEob(block<65:0>)

Returns the Hamming distance between the supplied block and the END_BURST_DELIMITER

Flush_inbuffer()

Flushes the input buffer of the FEC decoding algorithm block.

```
Flush_inbuffer()
{
   for(i=0, i<2040, i++)
   {
      inbuffer[i]=0
   }
   input_buffer_location = 29
}
```

SLIP_One_Bit

Causes the next candidate block sync position to be tested. The next candidate is exactly one bit later than the previous candidate – no burst alignments may be skipped. Following the conceptual model mentioned in “BlockFromPMA,” this function transfers one more bit from the 16 bit serializer to the 66 bit deserializer.

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76.3.3.1.4 State diagram

The OLT Synchronizer shall implement the state diagram as depicted in Figure 76–18. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

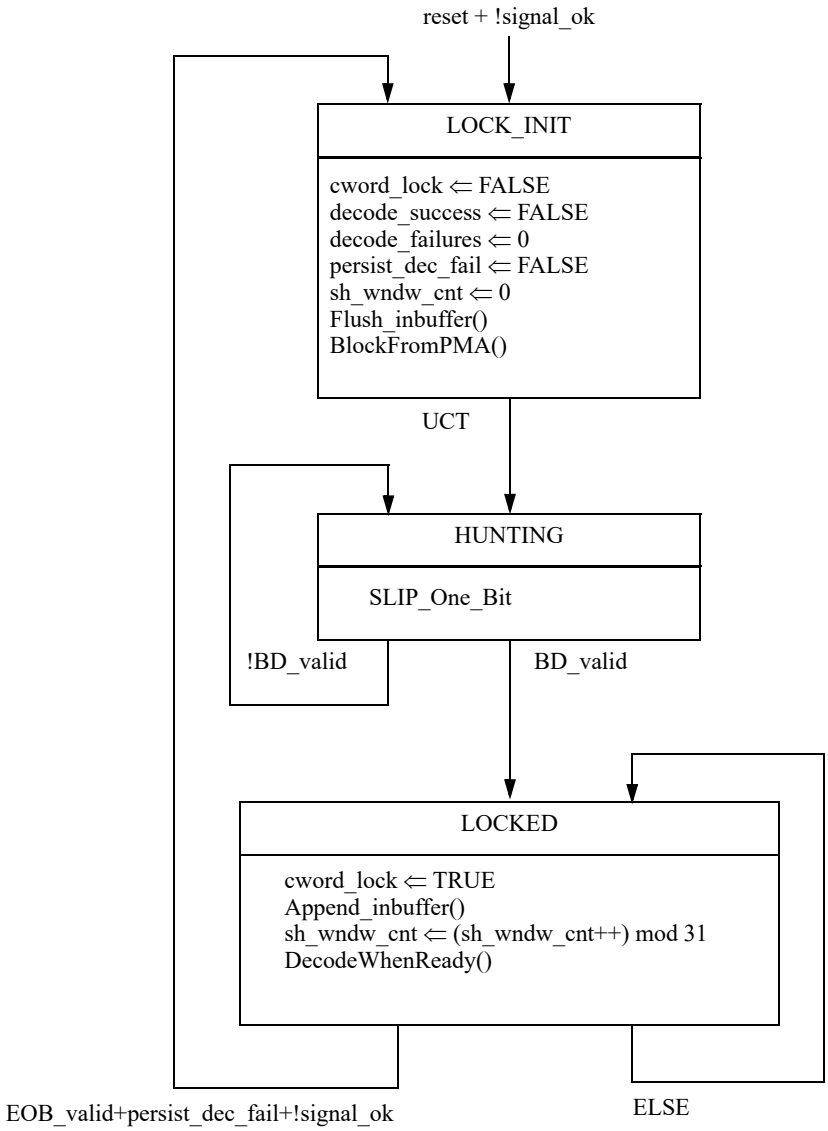

Figure 76–18—OLT Synchronizer state diagram

76.3.3.2 ONU Synchronizer

The codeword synchronization function receives data via the 16 bit PMA_UNITDATA.indication primitive.

The synchronizer forms a bit stream from the primitives by concatenating requests with the bits of each primitive in order from rx_data-group<0> to rx_data-group<15> (see Figure 76–19). It obtains lock to the thirty-one 66 bit blocks in the bit stream using the sync headers and outputs 2040 bit codewords to the FEC decoder function.

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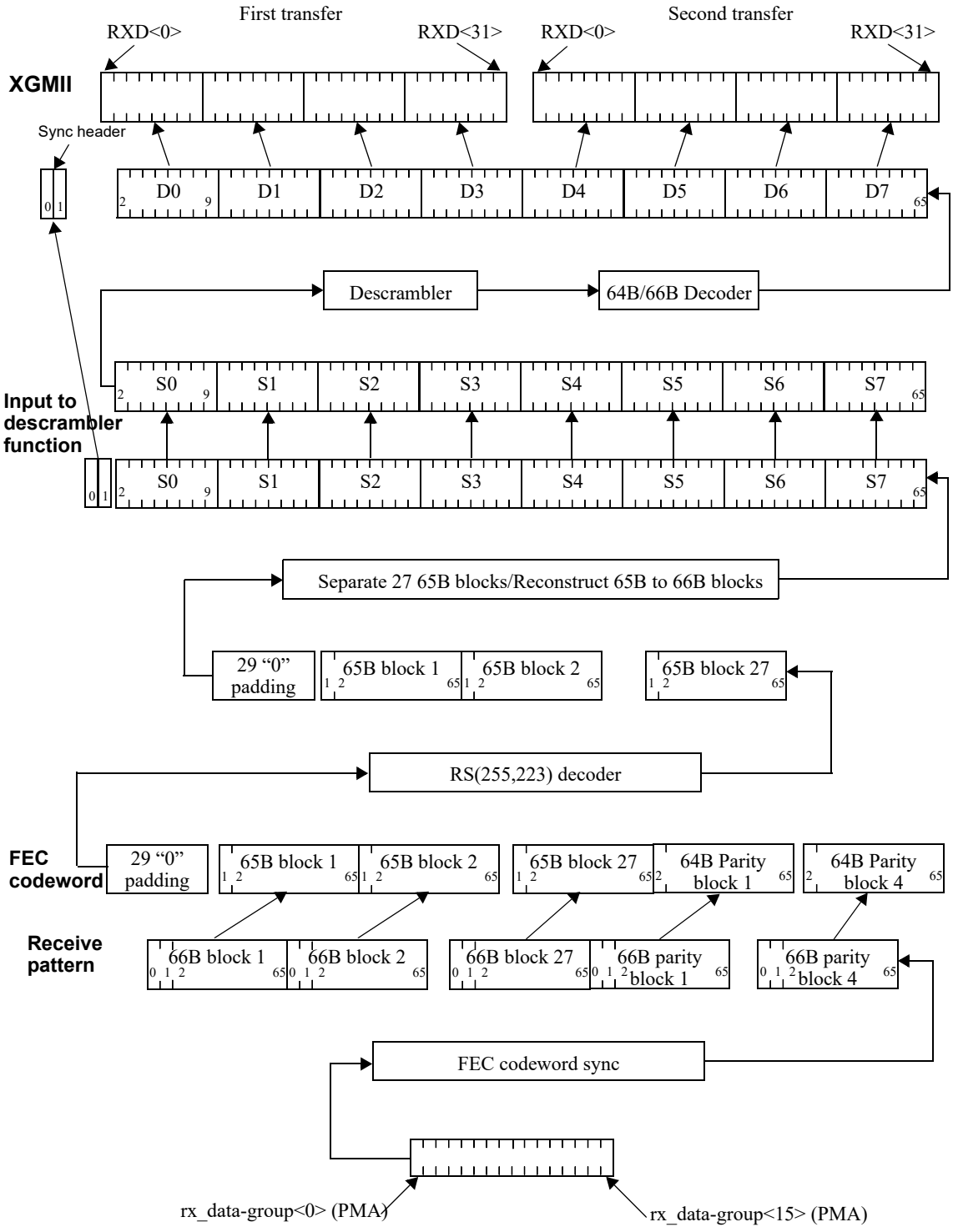

Figure 76–19—PCS Receive bit ordering

The incoming sync header pattern is 27 conventional (Clause 49) sync headers (binary 01 or 10), and then binary 00, 11, 11, and finally binary 00. The ONU synchronizer attempts to match this pattern to the

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received data stream, and when it finds a perfect match of two full codewords (62 blocks), it then asserts codeword lock.

While in codeword lock, the synchronizer copies the FEC-protected bits from each data block and the parity bits of the codeword into an input buffer. When the codeword is complete, the FEC decoder is triggered, and the input buffer is freed for the next codeword.

When in codeword lock, the state diagram continues to check for sync header validity. If 16 or more sync headers in a codeword pair (62 blocks) are invalid, then the state diagram deasserts codeword lock. In addition, if the persist_dec_fail signal becomes set, then codeword lock is deasserted (this check ensures that certain false-lock cases are not persistent.)

76.3.3.2.1 Constants

All the relevant constants defined in 49.2.13.2.1 are inherited. In addition, the following items are defined.

SH_CW_PATTERN
: TYPE: array of 8 bit unsigned
31 element array of codeword sync header bit counts, where each element is set to the value 1 except for:
Value:
SH_CW_PATTERN[27]=0
SH_CW_PATTERN[28]=2
SH_CW_PATTERN[29]=2
SH_CW_PATTERN[30]=0

76.3.3.2.2 Variables

cword_lock
: See 76.3.3.1.1.

decode_success
: See 76.3.3.1.1.

persist_dec_fail
: See 76.3.3.1.1.

reset
: This variable is inherited from 49.2.13.2.2.

sh_valid
: TYPE: Boolean array
Indication that is set true if received block rx_coded has valid sync header bits for the supposed current position in the FEC codeword. That is, sh_valid[i] is asserted if (rx_coded<0> + rx_coded<1>) = SH_CW_PATTERN[i mod 31] and de-asserted otherwise.

signal_ok
: This variable is inherited from 49.2.13.2.2.

slip_done
: This variable is inherited from 49.2.13.2.2.

test_sh
: This variable is inherited from 49.2.13.2.2.

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76.3.3.2.3 Counters

decode_failures
See 76.3.3.1.2.

FEC_cnt
TYPE: 8 bit unsigned
This counter keeps track of the parity sync header index that is currently being tested.

sh_wndw_cnt
See 76.3.3.1.2.

sh_valid_cnt
This counter is inherited from 49.2.13.2.4.

76.3.3.2.4 Functions

Append_inbuffer()
See 76.3.3.1.3.

DecodeWhenReady()
See 76.3.3.1.3.

SLIP
This function is inherited from 49.2.13.2.3.

76.3.3.2.5 State diagram

The ONU Synchronizer shall implement the state diagram as depicted in Figure 76–20. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

76.3.3.3 FEC decoding process

The 10GBASE-PR-D, 10GBASE-PR-U, and 10/1GBASE-PRX-U PCS shall correct errors in the received data stream using Reed-Solomon code (255,223). The FEC decoder corrects or confirms the correctness of the twenty-seven 66 bit blocks contained in the FEC codeword based on the four 66 bit blocks of parity information. The FEC decoding process then forwards the 66 bit data blocks to the descrambler and discards the parity blocks. The FEC decoding process is also responsible for setting bit 0 of the sync header to the inverse of bit 1 of the sync header. The handling of data leaving the FEC decoder and going to the descrambler is specified in the FEC decoding process state diagram shown in Figure 76–21. Implementations shall be capable of correcting up to 16 symbols in a codeword and detecting uncorrectable codewords.

The synchronizer state diagram accumulates a full codeword in a buffer. If the synchronizer is locked, then the FEC decoding process is triggered. The FEC algorithm then processes the buffer. The algorithm produces two outputs: the decode_success signal and (if successful) the corrected buffer. The data portion of the buffer is then read out to the descrambler logic in 66 bit blocks, as normal. Note that the rate of 66 bit transfers here is reduced due to the removal of the FEC parity blocks. This is corrected in the Idle Insertion step (see Figure 76–23).

If decode_success is false, then a counter is incremented (see 45.2.3.42). If there are three decoding failures in a row, then the Persist_dec_fail signal is asserted. This signal then resets the synchronizer.

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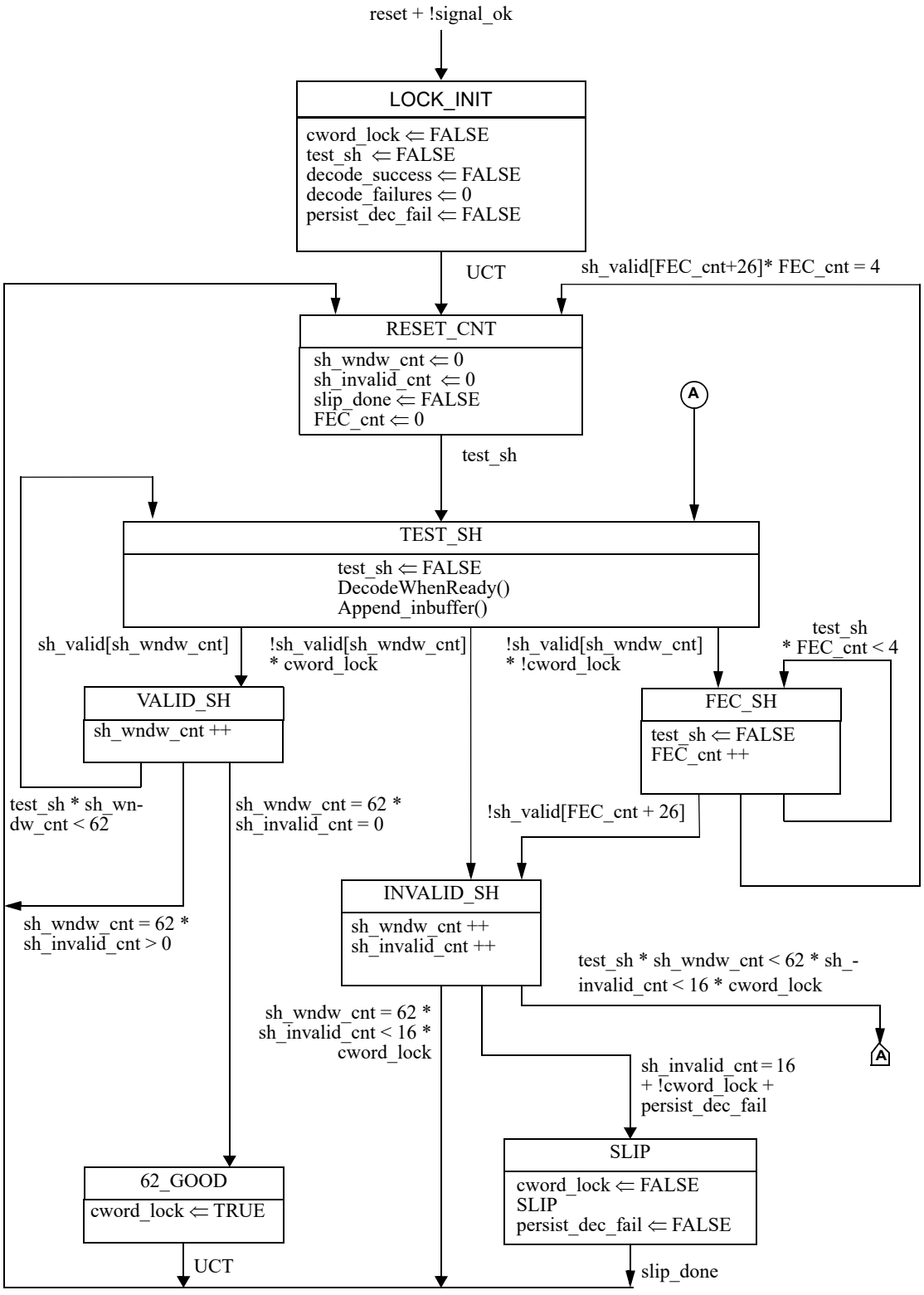

Figure 76–20—ONU Synchronizer state diagram

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The FEC decoding process shall provide a user option to indicate an uncorrectable FEC codeword (due to an excess of symbols containing errors) to higher layers. If this option is set to be true, the FEC decoding process checks for the value of decode_success. If the variable decode_success is set to false, then each sync header of the received payload blocks in the FEC codeword is set to a value of binary 00. However, the data blocks are nevertheless passed to the descrambler to maintain descrambling synchronization. When this option is set to FALSE and decode_success is FALSE then each received payload block is passed unchanged.

76.3.3.3.1 Variables

decode_done
: TYPE: Boolean
Indication that is transiently set when the FEC decoder algorithm has completed its processing and the corrected data is present in the output buffer.

decode_success
: See 76.3.3.1.1.

mark_uncorrectable
: TYPE: Boolean
Control variable that is set to true if the uncorrectable errors are to be marked.
Default: TRUE

outbuffer
: TYPE: bit array
An array of 2040 bits that holds the output of the FEC decoder.

persist_dec_fail
: See 76.3.3.1.1.

rx_code_corrected
: Type: 66 bit vector
The next block of data to be sent to the scrambler.

76.3.3.3.2 Counters

decode_failures
: See 76.3.3.1.2.

corrected_FEC_codewords_counter
: A corrected block is an FEC codeword that was received with one or more errored symbols, and that has been corrected by the FEC decoder.
corrected_FEC_codewords_counter counts once for each corrected FEC codeword processed. This is a 32 bit counter. This variable is provided by a management interface that may be mapped to the 45.2.3.41 register (3.76, 3.77).

FEC_uncorrected_blocks_counter
: An uncorrected block is an FEC codeword that was received with 17 or more errored symbols, and that has not been corrected by the FEC decoder.
FEC_uncorrected_blocks_counter counts once for each uncorrected FEC codeword processed. This is a 32 bit counter. This variable is provided by a management interface that may be mapped to the 45.2.3.42 register (3.78, 3.79).

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76.3.3.3.3 Functions

All the relevant functions defined in 49.2.13.2.3 are inherited. In addition, the following items are defined.

BlockFromPMA()
See 76.3.3.1.3.

BlockToDescrambler()
Function that sends the next rx_coded_corrected<65:0> block to the descrambler. It does not return until the transfer is completed, and each transfer takes 6.4 ns and is synchronized to the XGMII clock.

Flush_inbuffer()
See 76.3.3.1.3.

Read_outbuffer(i)
Passes output buffer contents to the descrambler, with the appropriate format.

```
Read_outbuffer[i]
{
   int offset = 29+i*65
   for(j=0, j<65, j++)
   {
      rx_coded_corrected<j+1> = outbuffer[j+offset]
   }
   if (!decode_success AND mark_uncorrectable)
   {
      rx_coded_corrected<0> = 0
      rx_coded_corrected<1> = 0
   }
   else
   {
      rx_coded_corrected<0> = !rx_coded_corrected<1>
   }
   BlockToDescrambler()
}
```

SLIP
This function is inherited from 49.2.13.2.3.

76.3.3.3.4 State diagrams

The body of this subclause comprises state diagrams, including the associated definitions of variables, constants, and functions pertinent to the 10GBASE-PR-D, 10GBASE-PR-U, and 10/1GBASE-PRX-U PCS receivers. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams in this clause follows the conventions in 21.5.

The FEC decoding process shall be implemented in the PCS as depicted in Figure 76–21. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

76.3.3.4 BER monitor

The BER monitor is described in Figure 76–22. This BER monitor function operates on the uncorrected incoming data stream.

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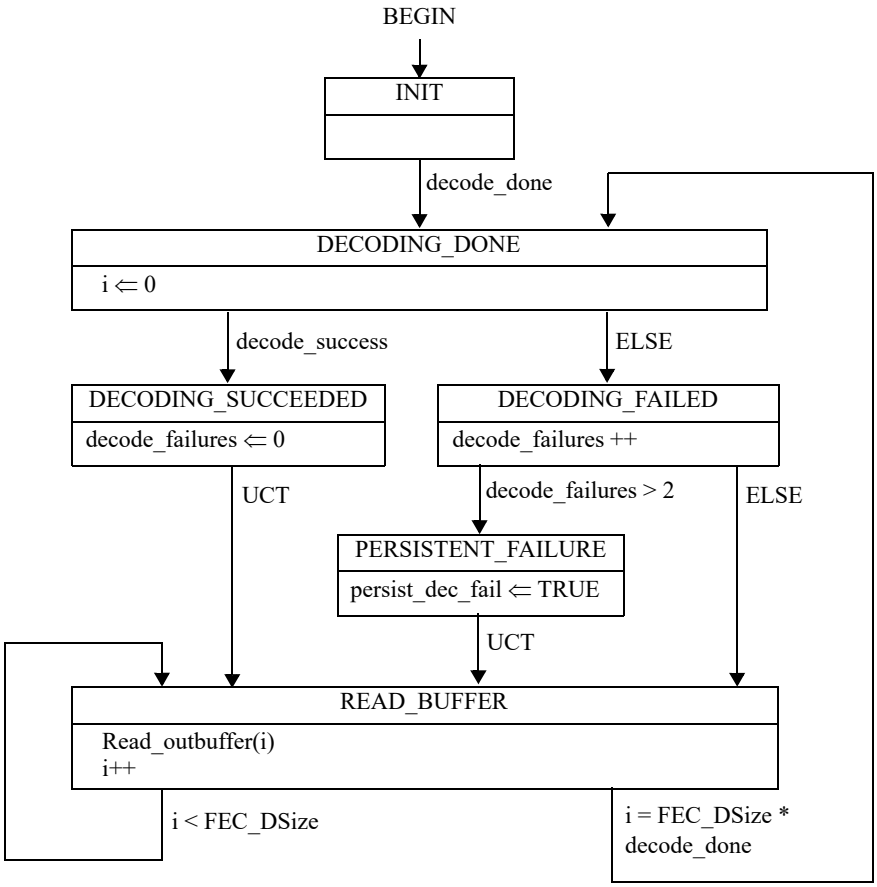

Figure 76–21—FEC decoding process state diagram

76.3.3.4.1 Variables

BER_Monitor_Interval
: Indicates the time window associated with the BER monitor function. The timers in the BER monitor state diagram depend on this configurable variable. This value is reflected in MDIO register 3.80.

ber_test_sh
: This variable is inherited from 49.2.13.2.2.

BER_Threshold
: Indicates the threshold value of invalid sync headers associated with the BER monitor function. When BER_Threshold bad sync headers are encountered within the BER Monitor_Interval period, the BER monitor raises the hi_ber flag. When the number of bad sync headers encountered within the BER_Monitor_interval period less than the BER_Threshold, the hi_ber flag is turned off. This value is reflected in MDIO register 3.82.

hi_ber
: This variable is inherited from 49.2.13.2.2.

reset
: This variable is inherited from 49.2.13.2.2.

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ber_test_sh
: This variable is inherited from 49.2.13.2.2.

76.3.3.4.2 Timers

State diagram timers follow the conventions of 14.2.3.2.

interval_timer
: Timer that is triggered every BER_monitor_interval μs +1%, –25%.

76.3.3.4.3 Counters

ber_cnt
: This counter is inherited from 49.2.13.2.4.

76.3.3.4.4 State diagrams

The BER monitor state diagram is present only in the ONU. It is shown in Figure 76–22.

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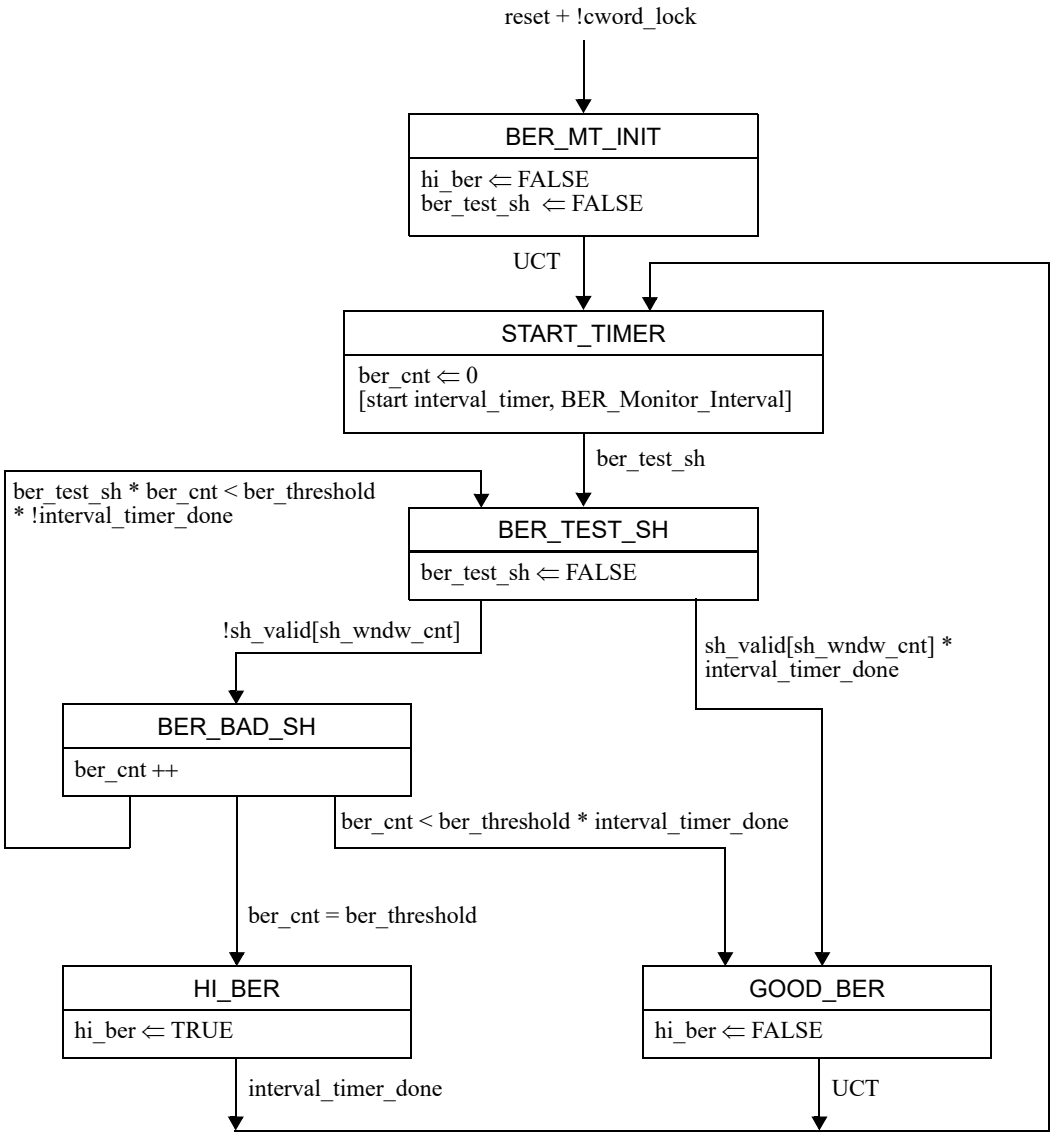

Figure 76–22—BER monitor state diagram (ONU only)

76.3.3.5 Descrambler

See 49.2.10 Descrambler.

76.3.3.6 64B/66B Decode

See 49.2.11 Receive process. The decoder shall perform functions specified in the state diagram shown in Figure 49–17.

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76.3.3.7 Idle Insertion

The receiving PCS inserts the Idle control characters to compensate for the removed FEC parity octets. The Idle Insertion function (see Figure 76–23) receives 72 bit vectors from the 64B/66B decoder and writes them into the Idle Insertion FIFO (called FIFO_II) and reads 72 bit vectors from the FIFO_II and transfers them to the XGMII.

The Idle Insertion process receives 72 bit vectors at a slower rate than the nominal XGMII rate due to the fact that the FEC parity blocks are removed by the FEC decoder and not put through the descrambler and 64B/66B decoder. The Idle Insertion process outputs 72 bit vectors at the nominal XGMII rate. To match the input and output rates, the Idle Insertion process inserts additional 72 bit vectors containing Idle codes. The additional blocks are inserted between packets and not necessarily at the same locations where parity blocks have been removed.

The body of this subclause comprises state diagrams, including the associated definitions of variables, constants, and functions pertinent to the 10GBASE-PR-D, 10GBASE-PR-U and 10/1GBASE-PRX-U PCS receivers. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams in this clause follows the conventions in 21.5.

76.3.3.7.1 Constants

FEC_DSize
: This constant is defined in 76.3.2.1.1.

FEC_PSize
: This constant is defined in 76.3.2.1.1.

FIFO_II_SIZE
: TYPE: 16 bit unsigned
This constant represents the size of Idle Insertion FIFO buffer. This buffer should be able to accommodate the number of 66 bit blocks sufficient to fill the gap introduced by removing the parity blocks from a maximum size MAC frame.
Value: 42

IDLE_VECTOR
: TYPE: 72 bit binary
This constant represents a 72 bit vector containing Idle characters.

LBLOCK_R
: This constant is defined in 49.2.13.2.1.

76.3.3.7.2 Variables

FIFO_II
: TYPE: Array of 72 bit vectors received from 64B/66B decoder.
This FIFO is internal to the Idle Insertion process. Upon initialization, all elements of this array are filled with IDLE_VECTORs. FIFO_II is a zero-based array of size FIFO_II_SIZE (see 76.3.3.7.1).

RX_CLK
: TYPE: Boolean
This variable represents the RX_CLK signal defined in 46.3.2.1.

rx_raw_in<71:0>
: TYPE: 72 bit binary

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Vector received from the output of the 64B/66B decoder. RXD<0> through RXD<31> for the second transfer are placed in rx_raw<40> through rx_raw<71>, respectively.

rx_raw_out<71:0>
TYPE: 72 bit binary
72 bit vector passed from the Idle Insertion process to XGMII. The vector is mapped to two XGMII transfers as follows:
Bits rx_raw<3:0> are mapped to RXC<3:0> for the first transfer;
Bits rx_raw<7:4> are mapped to RXC<3:0> for the second transfer;
Bits rx_raw<39:8> are mapped to RXD<31:0> for the first transfer;
Bits rx_raw<71:40> are mapped to RXD<31:0> for the second transfer.

VectorCount
TYPE: 16 bit unsigned
This variable tracks the number of 72 bit vectors stored in the FIFO_II.

76.3.3.7.3 Functions

T_TYPE(rx_raw)
This function is defined in 49.2.13.2.3.

76.3.3.7.4 Messages

DECODER_UNITDATA.indicate(rx_raw_in<71:0>)
A signal sent by the PCS Receive process conveying the next received 72 bit vector.

DUDI
Alias for DECODER_UNITDATA.indicate(rx_raw_in<71:0>).

76.3.3.7.5 State diagrams

The PCS Idle Insertion function shall implement the state diagram as shown in Figure 76–23. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

76.4 10GBASE-PR and 10/1GBASE-PRX PMA

The 10GBASE-PR PMA is derived from the 10GBASE-R PMA defined in Clause 51. This clause specifies 10GBASE-R extensions necessary to support P2MP operation. The 10/1GBASE-PRX PMA conceptually consists of a combination of transmit and receive functions specified for 10GBASE-PR and 1000BASE-PX defined in 65.3.2, as shown in Table 76–5.

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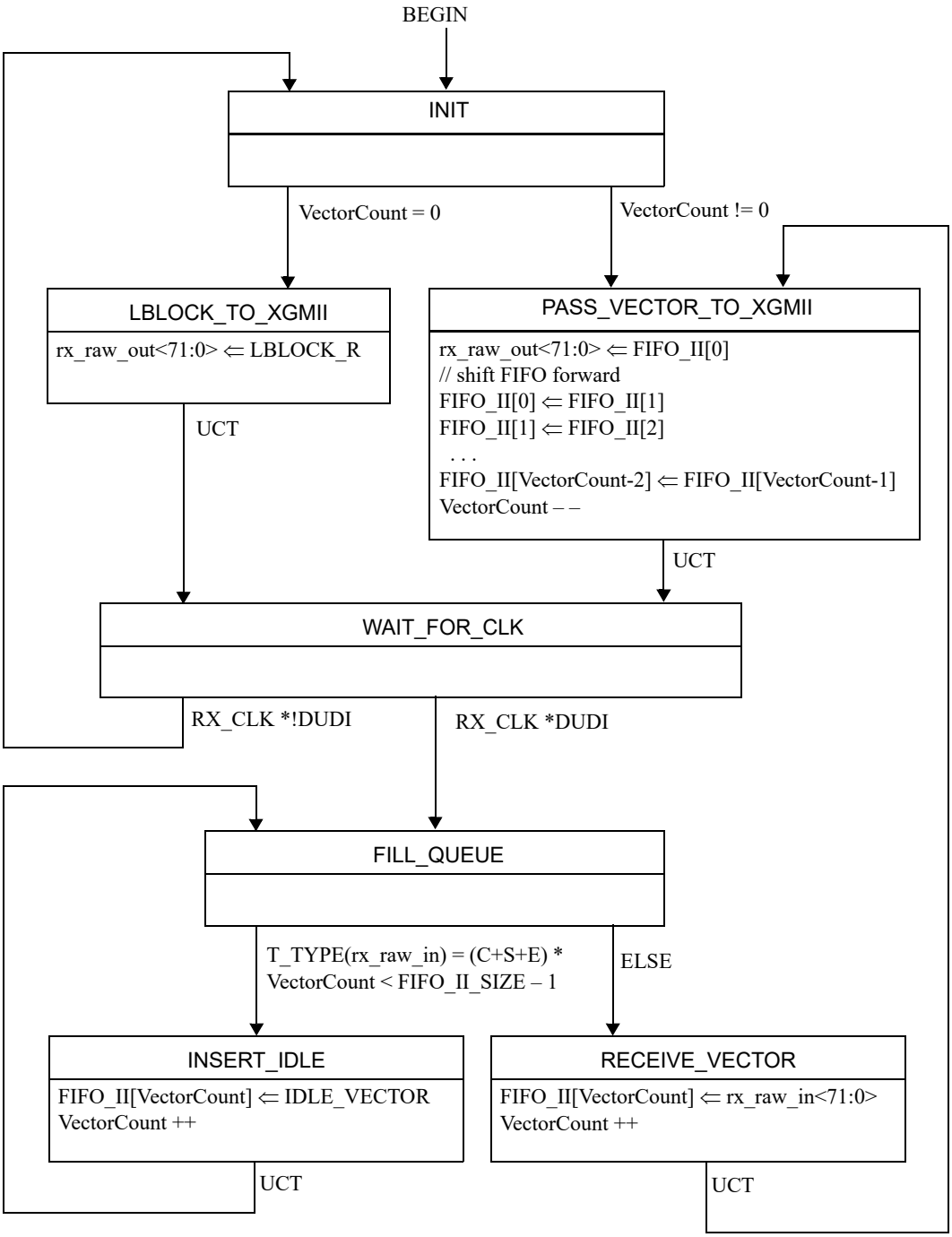

Figure 76–23—PCS Idle Insertion

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Table 76–5—Derivation of PMA transmit and receive functions for 10GBASE-PR and 10/1GBASE-PRX

PMA	Transmit function	Receive function
10GBASE-PR-U	As specified in Clause 51 with extensions defined in 76.4.1.	
10/1GBASE-PRX-U	Identical to 1000BASE-PX-U. See 65.3.1.	Identical to 10GBASE-PR-U. See 76.4.1.
10GBASE-PR-D	As specified in Clause 51 with extensions defined in 76.4.2.	
10/1GBASE-PRX-D	Identical to 10GBASE-PR-D.	Identical to 1000BASE-PX-D. See 65.3.2.

76.4.1 Extensions for 10GBASE-PR-U and 10/1GBASE-PRX-U

76.4.1.1 Physical Medium Attachment (PMA) sublayer interfaces

In addition to the primitives of Clause 51, the following primitive is defined:

PMA_SIGNAL.request(tx_enable)
: This primitive is mapped to PMD_SIGNAL.request(tx_enable). It is generated by the PCS's Data Detector. The effect of reception of PMD_SIGNAL.request(tx_enable) is defined in 75.3.1.4.

tx_enable
: The tx_enable parameter can take one of two values, ON or OFF.

76.4.1.2 Loop-timing specifications for ONUs

ONUs shall operate at the same time basis as the OLT, i.e., the ONU TX clock tracks the ONU RX clock, which in turn locks to OLT TX clock. Jitter transfer masks are defined in 75.7.

For the 10/1GBASE-PRX-U devices, the received clock PMA_RX_CLK is 644.53125 MHz (10.3125 GBd/16), however, the transmit clock PMA_TX_CLK is 125 MHz (1.25 GBd/10). The loop timing is achieved by multiplying the PMA_RX_CLK by 32 and dividing by 165.

76.4.2 Extensions for 10GBASE-PR-D and 10/1GBASE-PRX-D

76.4.2.1 CDR lock timing measurement for the upstream direction

CDR lock time (denoted T_{CDR}) is defined as a time interval required by the receiver to acquire phase lock on the incoming data stream. T_{CDR} is measured as the time elapsed from the moment when the electrical signal after the PMD at TP8, as illustrated in Figure 75–3, reaches the conditions specified in 75.7.15 for receiver settling time to the moment when the signal phase is recovered and jitter is maintained for a network with BER of no more than 10^{-3}.

A PMA instantiated in an OLT becomes synchronized at the bit level within 400 ns (T_{CDR}) after the appearance of a valid synchronization pattern (as defined in 76.3.2.5.2) at TP8.

76.4.2.1.1 Test specification

The test of the OLT PMA receiver T_{CDR} time assumes that there is an optical PMD transmitter at the ONU with well known T_{on} time as defined in 75.7.14, and an optical PMD receiver at the OLT with well-known $T_{receiver\_settling}$ time as defined in 75.7.15. After T_{on} + $T_{receiver\_settling}$ time, the parameters at TP8 reach within 15% of their steady state values, measure T_{CDR} as the time from the tx_enable assertion, minus the

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known $T_{on} + T_{receiver\_settling}$ time, to the time the electrical signal at the output of the receiving PMA reaches up to the phase difference from the input signal of the transmitting PMA assuring BER of 10^{-3}, and maintaining its jitter specifications. The signal throughout this test is the synchronization pattern, as illustrated in Figure 76–14.

76.5 Protocol implementation conformance statement (PICS) proforma for Clause 76, Reconciliation Sublayer, Physical Coding Sublayer, and Physical Media Attachment for 10G-EPON[139]

76.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 76, Reconciliation Sublayer, Physical Coding Sublayer and Physical Media Attachment for 10G-EPON, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

76.5.2 Identification

76.5.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

[139]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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76.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 76, Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), and Physical Media Attachment (PMA) for point-to-point media, types 10GBASE–PR and 10/1GBASE–PRX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

76.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*OLT	OLT functionality	76.2.1	Device supports functionality required for OLT	O.1	Yes [ ] No [ ]
*ONU	ONU functionality	76.2.1	Device supports functionality required for ONU	O.1	Yes [ ] No [ ]

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76.5.4 PICS proforma tables for Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), and Physical Media Attachment (PMA) for point-to-multipoint media, types 10GBASE–PR and 10/1GBASE–PRX

76.5.4.1 Operating modes of OLT MACs

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Unidirectional mode	76.2.3	Device operates in unidirectional transmission mode	OLT:M	Yes [ ]
OM2	Dual-rate mode	76.2.2.3	Device operates in dual-rate mode	OLT:O	Yes [ ] No [ ]

76.5.4.2 ONU and OLT variables

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	enable variable	65.1.3.1	True for ONU MAC, TRUE for OLT MAC if enabled, FALSE for OLT MAC if not enabled	M	Yes [ ]
FS2	mode variable	65.1.3.1	0 for ONU MAC, 0 or 1 for enabled OLT MAC	M	Yes [ ]
FS3	logical_link_id variable	76.2.6.1.1	Set to 0x7FFE until ONU MAC is registered Set to any value for enabled OLT MAC. Set to any value other then 0x7FFE for registered ONU MAC	M	Yes [ ]
FS4	multicast LLID support	76.2.6.1.1	Supports multicast LLID, multicast_link_id variable	O	Yes [ ] No [ ]

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76.5.4.3 Preamble mapping and replacement

Item	Feature	Subclause	Value/Comment	Status	Support
PM1	CRC-8 generation	65.1.3.2	CRC calculation produces same result as serial implementation	M	Yes [ ] No [ ]
PM2	CRC-8 initial value	65.1.3.2	CRC shift register initialized to 0x00 before each new calculations	M	Yes [ ] No [ ]
PM3	SLD parsing	76.2.6.1.3.1	If SLD is not found then discard packet	M	Yes [ ] No[ ]
PM4	SLD replacement	76.2.6.1.3.1	Replace SLD with preamble	M	Yes [ ] No [ ]
PM5	LLID matching	76.2.6.1.3.2	If LLID does not match then discard packet	M	Yes [ ] No [ ]
PM6	multicast LLID matching	76.2.6.1.3.2	If multicast LLID matches accept the packet	*FS4 :M	Yes [ ] No [ ]
PM7	LLID replacement	76.2.6.1.3.2	Replace LLID with preamble	M	Yes [ ] No [ ]
PM8	Reserved LLID	76.2.6.1.3.2	Registered ONU shall not transmit frames with a reserved LLID	M	Yes [ ] No [ ]
PM9	CRC-8 checking	65.1.3.3.3	If CRC does not match then discard packet	M	Yes [ ] No [ ]
PM10	CRC-8 replacement	65.1.3.3.3	Replace CRC with preamble	M	Yes [ ] No [ ]

76.5.4.4 Coding Rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder implements the code as specified	76.3.2.2		M	Yes [ ] No [ ]
C2	Decoder implements the code as specified	76.3.3.6		M	Yes [ ] No [ ]

76.5.4.5 Data detection

Item	Feature	Subclause	Value/Comment	Status	Support
DD1	Buffer depth	76.3.2.5.1	Depth sufficient to turn on laser and send laser synchronization pattern, Burst Delimiter pattern and a predefined number of Idle control character (receiver settle)	ONU:M	Yes [ ] No [ ]
DD2	OLT laser control	76.3.2.5.5	Always takes the value ON	OLT:M	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DD3	ONU State diagrams	76.3.2.5.7	Meets the requirements of Figure 76–16 and Figure 76–17	ONU:M	Yes [ ] No[ ]
DD4	OLT State diagrams	76.3.2.5.7	Meets the requirements of Figure 76–16 and Figure 76–17	OLT:M	Yes [ ] No[ ]

76.5.4.6 Idle control character deletion

Item	Feature	Subclause	Value/Comment	Status	Support
AIC1	Idle Deletion function implementation in ONU	76.3.2.1.5	Meets the requirements of Figure 76–10	ONU:M	Yes [ ] No [ ]
AIC2	Idle Deletion function implementation in OLT	76.3.2.1.5	Meets the requirements of Figure 76–9	OLT:M	Yes [ ] No [ ]

76.5.4.7 FEC requirements

Item	Feature	Subclause	Value/Comment	Status	Support
FE1	FEC Encoder	76.3.2.4	RS(255,223)	M	Yes [ ] No [ ]
FE2	FEC Decoder	76.3.3.3	RS(255,223)	M	Yes [ ] No [ ]
FE3	Uncorrectable block indication	76.3.3.3	When activated, mark all 66 bit blocks in an uncorrectable block by setting all sync headers for the received payload blocks of the FEC codeword to the value of 00	M	Yes [ ] No [ ]
FE4	Correctable codewords	76.3.3.3	Correct up to 16 symbols in a codeword and detect uncorrectable codewords	M	Yes [ ] No [ ]

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76.5.4.8 FEC state diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Transmit	76.3.2.4.1	Meets the requirements of Figure 76–12	M	Yes [ ]
SM2	ONU synchronization	76.3.3.2.5	Meets the requirements of Figure 76–20	ONU:M	Yes [ ] No [ ]
SM3	OLT synchronization	76.3.3.1.4	Meets the requirements of Figure 76–18	OLT:M	Yes [ ] No [ ]
SM4	FEC decoding process	76.3.3.3.4	Meets the requirements of Figure 76–21	M	Yes [ ] No [ ]

76.5.4.9 PCS Idle Insertion

Item	Feature	Subclause	Value/Comment	Status	Support
PI1	Idle Insertion	76.3.3.7.5	Meets the requirements of Figure 76–23	M	Yes [ ] No [ ]

76.5.4.10 PMA

Item	Feature	Subclause	Value/Comment	Status	Support
BMC1	Loop timing	76.4.1.2	ONU RX clock tracks OLT TX clock	ONU:M	Yes [ ] No [ ]

76.5.4.11 Delay variation

Item	Feature	Subclause	Value/Comment	Status	Support
DV1	Delay variation	76.1.2	Combined delay variation through RS, PCS, and PMA sublayers is limited to 1 time_quantum	M	Yes [ ] No [ ]

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77. Multipoint MAC Control for 10G–EPON

77.1 Overview

This clause deals with the mechanism and control protocols required in order to reconcile the 10 Gb/s P2MP topology into the Ethernet framework. The P2MP medium is a passive optical network (PON), an optical network with no active elements in the signal's path from source to destination. The only interior elements used in a PON are passive optical components, such as optical fiber, splices, and splitters. When combined with the Ethernet protocol, such a network is referred to as Ethernet passive optical network (EPON).

P2MP is an asymmetric medium based on a tree (or tree-and-branch) topology. The DTE connected to the trunk of the tree is called optical line terminal (OLT) and the DTEs connected at the branches of the tree are called optical network units (ONU). The OLT typically resides at the service provider's facility, while the ONUs are located at the subscriber premises.

In the downstream direction (from the OLT to an ONU), signals transmitted by the OLT pass through a 1:N passive splitter (or cascade of splitters) and reach each ONU. In the upstream direction (from the ONUs to the OLT), the signal transmitted by an ONU would only reach the OLT, but not other ONUs. To avoid data collisions and increase the efficiency of the subscriber access network, the ONU's transmissions are arbitrated. This arbitration is achieved by allocating a transmission window (grant) to each ONU. An ONU defers transmission until its grant arrives. When the grant arrives, the ONU transmits frames at wire speed during its assigned time slot.

A simplified P2MP topology example is depicted in Figure 77–1. Clause 67 provides additional examples of P2MP topologies.

Topics dealt with in this clause include allocation of upstream transmission resources to different ONUs, discovery and registration of ONUs into the network, and reporting of congestion to higher layers to allow for dynamic bandwidth allocation schemes and statistical multiplexing across the PON.

This clause does not deal with topics including bandwidth allocation strategies, authentication of end-devices, quality-of-service definition, provisioning, or management.

This clause specifies the multipoint control protocol (MPCP) to operate an optical multipoint network by defining a Multipoint MAC Control sublayer as an extension of the MAC Control sublayer defined in Clause 31, and supporting current and future operations as defined in Clause 31and annexes.

Each PON consists of a node located at the root of the tree assuming the role of OLT, and multiple nodes located at the tree leaves assuming roles of ONUs. The network operates by allowing only a single ONU to transmit in the upstream direction at a time. The MPCP located at the OLT is responsible for timing the different transmissions. Reporting of congestion by the different ONUs may assist in optimally allocating the bandwidth across the PON.

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Automatic discovery of end stations is performed, culminating in registration through binding of an ONU to an OLT port by allocation of a Logical Link ID (see LLID in 76.2.6.1.3.2), and dynamic binding to a MAC connected to the OLT.

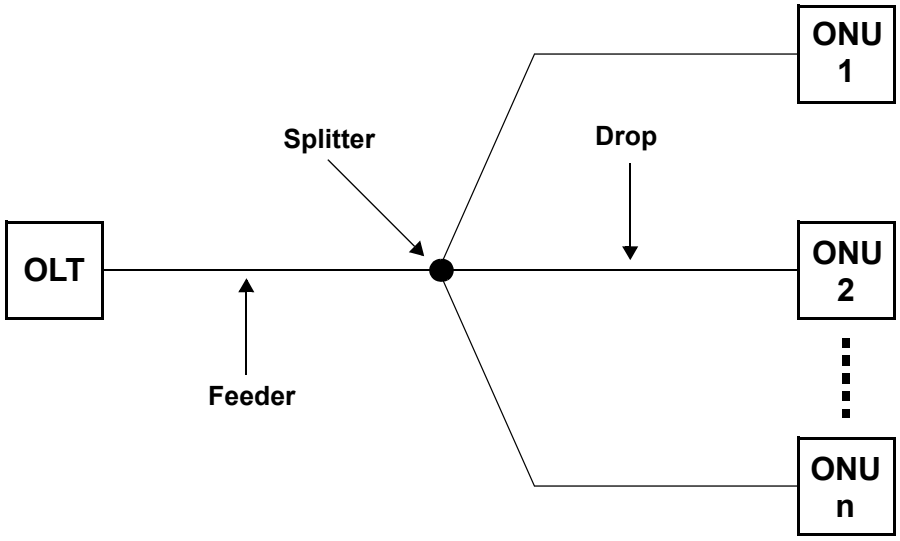

Figure 77–1—PON topology example

The Multipoint MAC Control functionality shall be implemented for subscriber access devices containing point-to-multipoint Physical Layer devices defined in Clause 75.

77.1.1 Goals and objectives

The goals and objectives of this clause are the definition of a point-to-multipoint Ethernet network utilizing an optical medium.

Specific objectives met include the following:

a) Support of point-to-point Emulation (P2PE) as specified
b) Support multiple LLIDs and MAC Clients at the OLT
c) Support a single LLID per ONU
d) Support a mechanism for single copy broadcast
e) Flexible architecture allowing dynamic allocation of bandwidth
f) Use of 32 bit timestamp for timing distribution
g) MAC Control based architecture
h) Ranging of discovered devices for improved network performance
i) Continuous ranging for compensating round trip time variation

77.1.2 Position of Multipoint MAC Control within the IEEE 802.3 hierarchy

Multipoint MAC Control defines the MAC control operation for optical point-to-multipoint networks. Figure 77–2 and Figure 77–3 depict the architectural positioning of the Multipoint MAC Control sublayer with respect to the MAC and the MAC Control client. The Multipoint MAC Control sublayer takes the place of the MAC Control sublayer to extend it to support multiple clients and additional MAC control functionality.

Multipoint MAC Control is defined using the mechanisms and precedents of the MAC Control sublayer. The MAC Control sublayer has extensive functionality designed to manage the real-time control and manipulation of MAC sublayer operation. This clause specifies the extension of the MAC Control

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mechanism to manipulate multiple underlying MACs simultaneously. This clause also specifies a specific protocol implementation for MAC Control.

The Multipoint MAC Control sublayer is specified such that it can support new functions to be implemented and added to this standard in the future. MultiPoint Control Protocol (MPCP), the management protocol for P2MP is one of these protocols. Non-real-time, or quasi-static control (e.g., configuration of MAC operational parameters) is provided by Layer Management. Operation of the Multipoint MAC Control sublayer is transparent to the MAC.

As depicted in Figure 77–2 and Figure 77–3, the layered system instantiates multiple MAC entities, using a single Physical Layer. The individual MAC instances offer a point-to-point emulation service between the OLT and the ONU. An additional MAC is instantiated to communicate to all 10G–EPON ONUs at once. This instance takes maximum advantage of the broadcast nature of the downstream channel by sending a single copy of a frame that is received by all 10G–EPON ONUs. This MAC instance is referred to as Single Copy Broadcast (SCB).

The ONU only requires one MAC instance since frame filtering operations are done at the RS layer before reaching the MAC. Therefore, MAC and layers above are emulation-agnostic at the ONU (see 76.2.6.1.3).

Although Figure 77–2 and Figure 77–3 and supporting text describe multiple MACs within the OLT, a single unicast MAC address may be used by the OLT. Within the EPON Network, MACs are uniquely identified by their LLIDs, which are dynamically assigned by the registration process.

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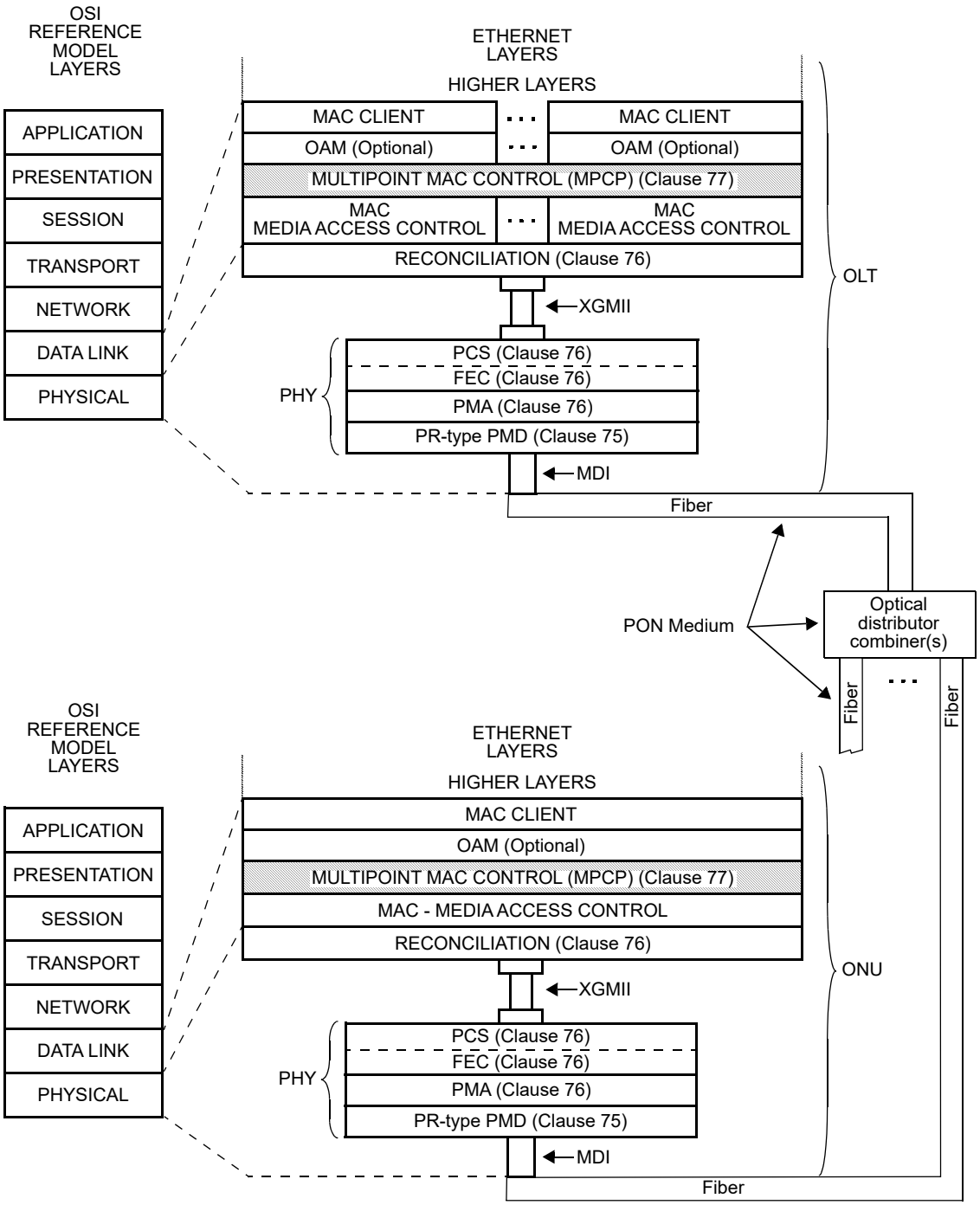

MPMC described in this clause

XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 77–2—Relationship of Multipoint MAC Control and the OSI protocol stack for 10/10G–EPON (10 Gb/s downstream and 10 Gb/s upstream)

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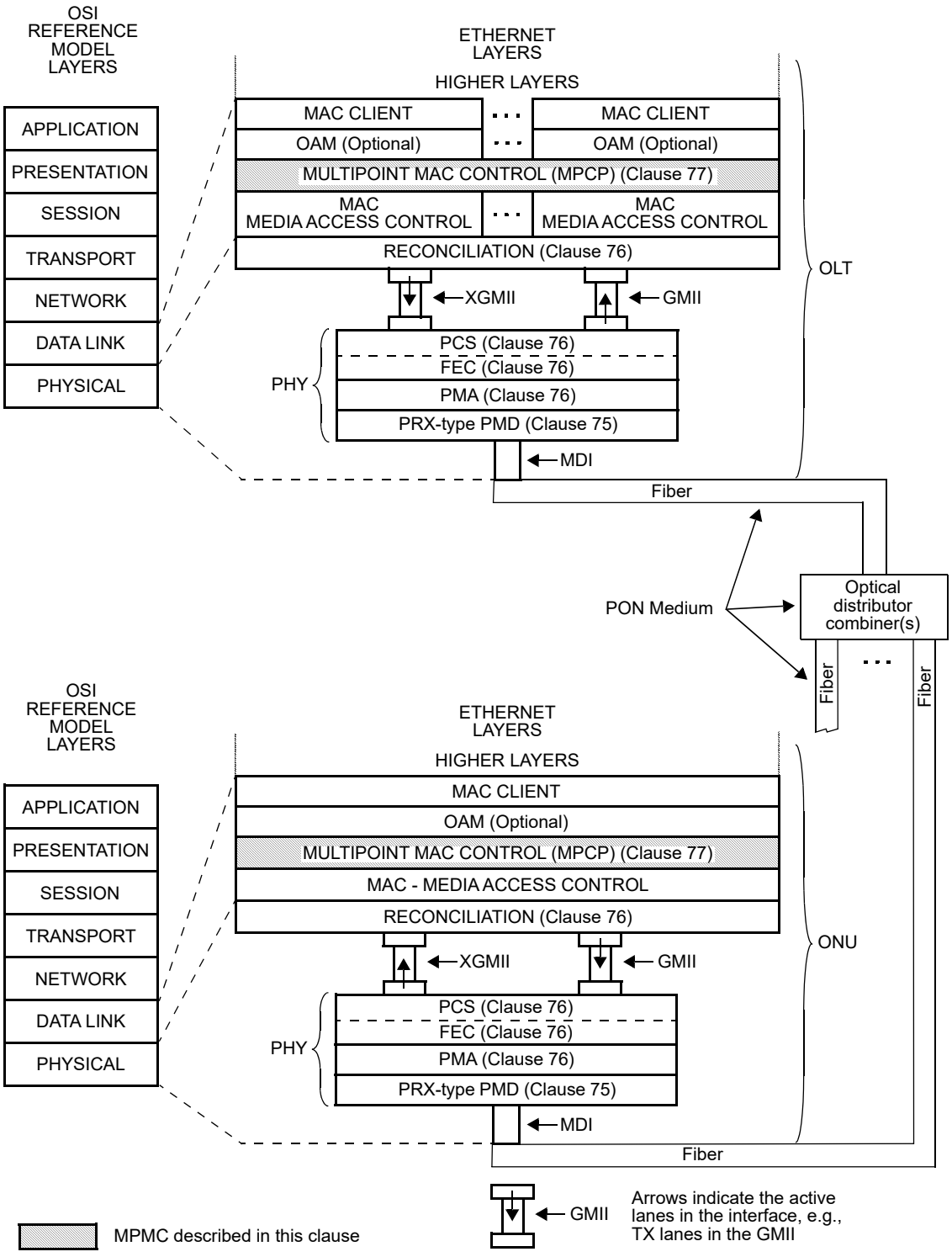

Figure 77–3—Relationship of Multipoint MAC Control and the OSI protocol stack for 10/1G–EPON (10 Gb/s downstream and 1 Gb/s upstream)

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77.1.3 Functional block diagram

Figure 77–4 provides a functional block diagram of the Multipoint MAC Control architecture.

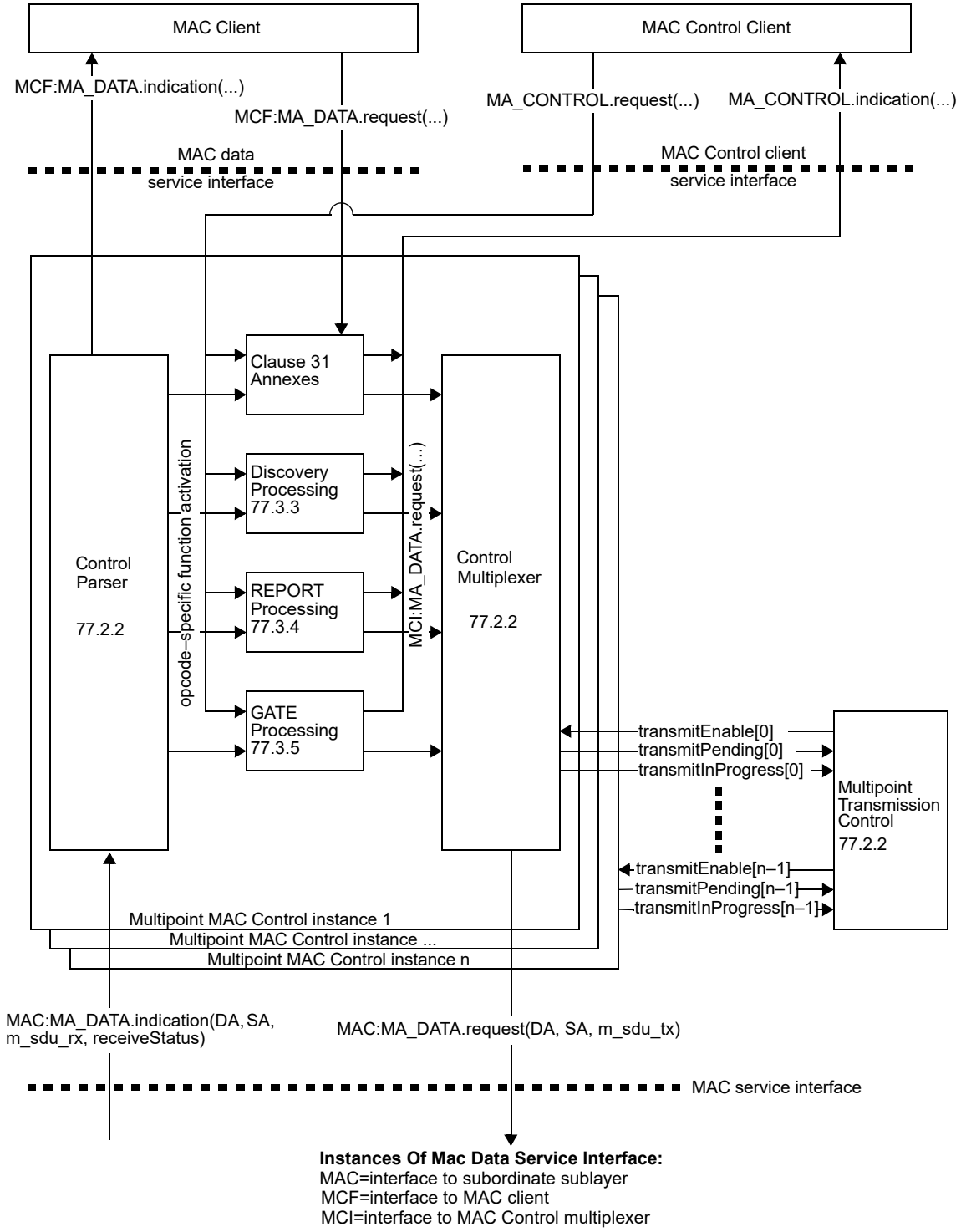

Figure 77–4—Multipoint MAC Control functional block diagram

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77.1.4 Service interfaces

The MAC Client communicates with the Control Multiplexer using the standard service interface specified in 2.3. Multipoint MAC Control communicates with the underlying MAC sublayer using the standard service interface specified in Annex 4A.3.2. Similarly, Multipoint MAC Control communicates internally using primitives and interfaces consistent with definitions in Clause 31.

77.1.5 State diagram conventions

The body of this standard comprises state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2 augmented as follows:

a) [start x_timer, y] sets expiration of *y* to timer *x_timer*.
b) [stop x_timer] aborts the timer operation for *x_timer* asserting *x_timer_not_done* indefinitely.

The state diagrams use an abbreviation MACR as a shorthand form for MA_CONTROL.request and MACI as a shorthand form for MA_CONTROL.indication.

The vector notations used in the state diagrams for bit vector use 0 to mark the first received bit and so on (for example data[0:15]), following the conventions of 3.1 for bit ordering. When referring to an octet vector, 0 is used to mark the first received octet and so on (for example m_sdu[0..1]).

a < *b:* A function that is used to compare two (cyclic) time values. Returned value is true when *b* is larger than *a* allowing for wrap around of *a* and *b*. The comparison is made by subtracting *b* from *a* and testing the MSB. When MSB(*a*–*b*) = 1 the value true is returned, else false is returned. In addition, the following functions are defined in terms of *a* < *b*:
a > *b* is equivalent to !(*a* < *b* or *a* = *b*)
a ≥ *b* is equivalent to !(*a* < *b*)
a ≤ *b* is equivalent to !(*a* > *b*)

77.2 Multipoint MAC Control operation

As depicted in Figure 77–4, the Multipoint MAC Control functional block comprises the following functions:

a) *Multipoint Transmission Control*. This block is responsible for synchronizing Multipoint MAC Control instances associated with the Multipoint MAC Control. This block maintains the Multipoint MAC Control state and controls the multiplexing functions of the instantiated MACs.
b) *Multipoint MAC Control Instance n*. This block is instantiated for each MAC and respective MAC and MAC Control clients associated with the Multipoint MAC Control. It holds all the variables and state associated with operating all MAC Control protocols for the instance.
c) *Control Parser*. This block is responsible for parsing MAC Control frames, and interfacing with Clause 31 entities, the opcode specific blocks, and the MAC Client.
d) *Control Multiplexer*. This block is responsible for selecting the source of the forwarded frames.
e) *Clause 31 annexes*. This block holds MAC Control actions as defined in Clause 31 annexes for support of legacy and future services.
f) *Discovery, Report, and Gate Processing*. These blocks are responsible for handling the MPCP in the context of the MAC.

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77.2.1 Principles of Multipoint MAC Control

As depicted in Figure 77–4, Multipoint MAC Control sublayer may instantiate multiple Multipoint MAC Control instances in order to interface multiple MAC and MAC Control clients above with multiple MACs below. A unique unicast MAC instance is used at the OLT to communicate with each ONU. The individual MAC instances utilize the point-to-point emulation service between the OLT and the ONU as defined in 76.2.

At the ONU, a single MAC instance is used to communicate with a MAC instance at the OLT. In that case, the Multipoint MAC Control contains only a single instance of the Control Parser/Multiplexer function.

Multipoint MAC Control protocol supports several MAC and client interfaces. Only a single MAC interface and Client interface is enabled for transmission at a time. There is a tight mapping between a MAC service interface and a Client service interface. In particular, the assertion of the MAC:MA_DATA.indication primitive in MAC *j* leads to the assertion of the MCF:MA_DATA.indication primitive to Client *j*. Conversely, the assertion of the request service interface in Client *i* leads to the assertion of the MAC:MA_DATA.request primitive of MAC *i*. Note that the Multipoint MAC sublayer need not receive and transmit packets associated with the same interface at the same time. Thus the Multipoint MAC Control acts like multiple MAC Controls bound together with common elements.

The scheduling algorithm is implementation dependent, and is not specified for the case where multiple transmit requests happen at the same time.

The reception operation is as follows. The Multipoint MAC Control instances generate MAC:MA_DATA.indication service primitives continuously to the underlying MAC instances. Since these MACs are receiving frames from a single PHY only one frame is passed from the MAC instances to Multipoint MAC Control. The MAC instance responding to the MAC:MA_DATA.indication is referred to as the enabled MAC, and its service interface is referred to as the enabled MAC interface. The MAC passes to the Multipoint MAC Control sublayer all valid frames. Invalid frames, as specified in 3.4, are not passed to the Multipoint MAC Control sublayer in response to a MAC:MA_DATA.indication service primitive.

The enabling of a transmit service interface is performed by the Multipoint MAC Control instance in collaboration with the Multipoint Transmission Control. Frames generated in the MAC Control are given priority over MAC Client frames, in effect, prioritizing the MA_CONTROL primitive over the MCF:MA_DATA primitive, and for this purpose MCF:MA_DATA.request primitives may be delayed, discarded or modified in order to perform the requested MAC Control function. For the transmission of this frame, the Multipoint MAC Control instance enables forwarding by the MAC Control functions, but the MAC Client interface is not enabled. The reception of a frame in a MAC results in generation of the MAC:MA_DATA.indication primitive on that MAC's interface. Only one receive MAC interface is enabled at any given time since there is only one PHY interface.

The information of the enabled interfaces is stored in the controller state variables, and accessed by the Multiplexing Control block.

The Multipoint MAC Control sublayer uses the services of the underlying MAC sublayer to exchange both data and control frames.

Receive operation (MAC:MA_DATA.indication) at each instance:

a) A frame is received from the underlying MAC
b) The frame is parsed according to Length/Type field
c) MAC Control frames are demultiplexed according to opcode and forwarded to the relevant processing functions
d) Data frames (see 31.5.1) are forwarded to the MAC Client by asserting MCF:MA_DATA.indication primitives

Transmit operation (MAC:MA_DATA.request) at each instance:

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e) The MAC Client signals a frame transmission by asserting MCF:MA_DATA.request, or

f) A protocol processing block attempts to issue a frame, as a result of a previous MA_CONTROL.request or as a result of an MPCP event that generates a frame.

g) When allowed to transmit by the Multipoint Transmission Control block, the frame is forwarded.

77.2.1.1 Ranging and timing process

Both the OLT and the ONU have 32 bit counters that increment every 16 ns. These counters provide a local time stamp. When either device transmits an MPCPDU, it maps its counter value into the timestamp field. The time of transmission of the first octet of the MPCPDU frame from the MAC Control to the MAC is taken as the reference time used for setting the timestamp value.

When the ONU receives MPCPDUs, it sets its counter according to the value in the timestamp field in the received MPCPDU.

When the OLT receives MPCPDUs, it uses the received timestamp value to calculate or verify a round trip time between the OLT and the ONU. The Round Trip Time (RTT) is equal to the difference between the timer value and the value in the timestamp field. The calculated RTT is notified to the client via the MA_CONTROL.indication primitive. The client can use this RTT for the ranging process.

A condition of *timestamp drift error* occurs when the difference between OLT's and ONU's clocks exceeds some predefined threshold. This condition can be independently detected by the OLT or an ONU. The OLT detects this condition when an absolute difference between new and old RTT values measured for a given ONU exceeds the value of guardThresholdOLT (see 77.2.2.1), as shown in Figure 77–11. An ONU detects the timestamp drift error condition when absolute difference between a timestamp received in an MPCPDU and the localTime counter exceeds guardThresholdONU (see 77.2.2.1), as is shown in Figure 77–12.

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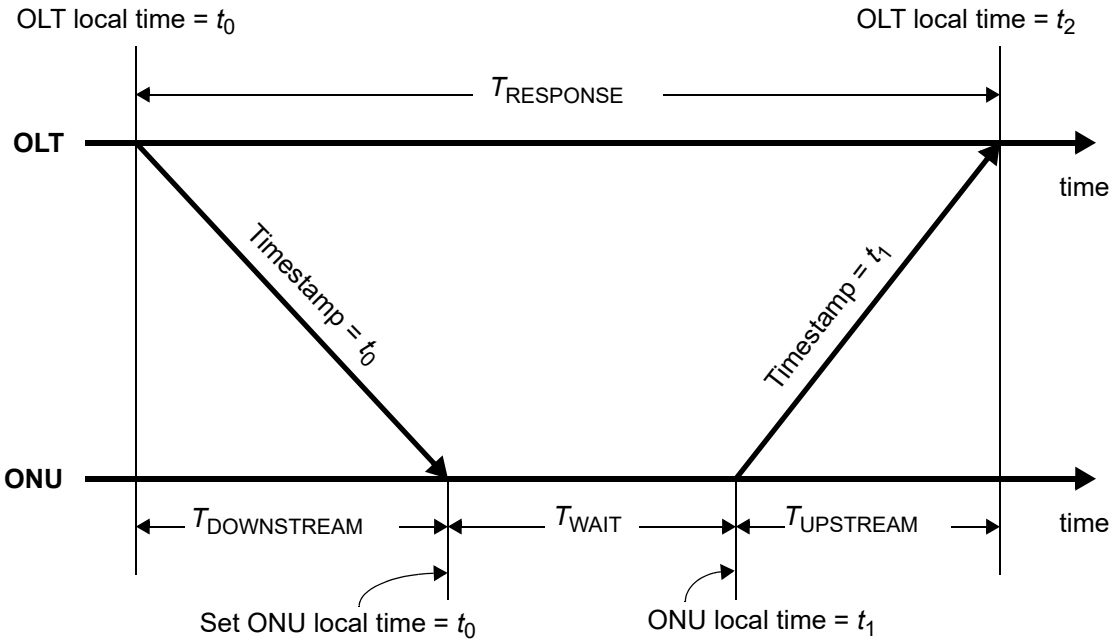

$T_{DOWNSTREAM}$ = downstream propagation delay

$T_{UPSTREAM}$ = upstream propagation delay

T_{WAIT} = wait time at ONU = $t_1 - t_0$

$T_{RESPONSE}$ = response time at OLT = $t_2 - t_0$

$$RTT = T_{DOWNSTREAM} + T_{UPSTREAM} = T_{RESPONSE} - T_{WAIT} = (t_2 - t_0) - (t_1 - t_0) = t_2 - t_1$$

Figure 77–5—Round trip time calculation

77.2.2 Multipoint transmission control, Control Parser, and Control Multiplexer

The purpose of the multipoint transmission control is to allow only one of the multiple MAC clients to transmit to its associated MAC and subsequently to the RS layer at one time by only asserting one transmitEnable signal at a time.

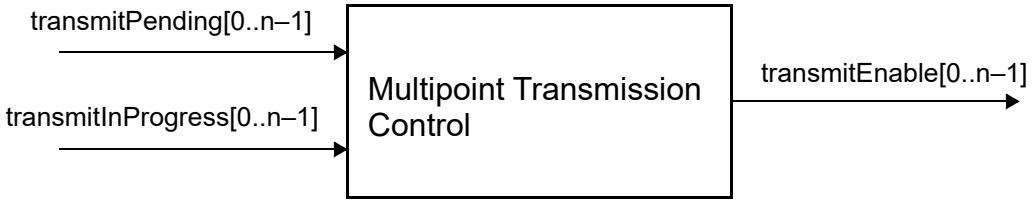

Figure 77–6—Multipoint Transmission Control service interfaces

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Multipoint MAC Control Instance n function block communicates with the Multipoint Transmission Control using transmitEnable[n], transmitPending[n], and transmitInProgress[n] state variables (see Figure 77–4).

The Control Parser is responsible for opcode independent parsing of MAC frames in the reception path. By identifying MAC Control frames, demultiplexing into multiple entities for event handling is possible. Interfaces are provided to existing Clause 31 entities, functional blocks associated with MPCP, and the MAC Client.

The Control Multiplexer is responsible for forwarding frames from the MAC Control opcode-specific functions and the MAC Client to the MAC. Multiplexing is performed in the transmission direction. Given multiple MCF:MA_DATA.request primitives from the MAC Client, and MA_CONTROL.request primitives from the MAC Control Clients, a single MAC:MA_DATA.request service primitive is generated for transmission. At the OLT, multiple MAC instances share the same Multipoint MAC Control, as a result, the transmit block is enabled based on an external control signal housed in Multipoint Transmission Control for transmission overlap avoidance. At the ONU, the Gate Processing functional block interfaces for upstream transmission administration.

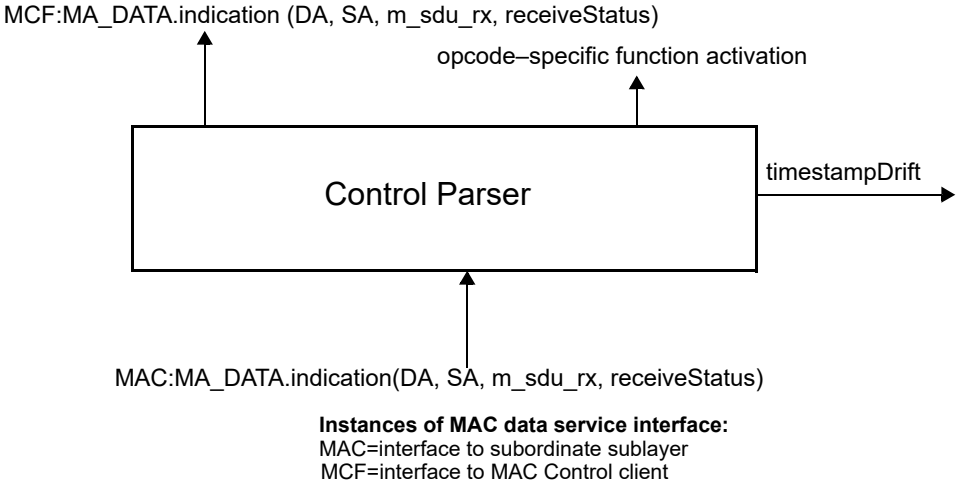
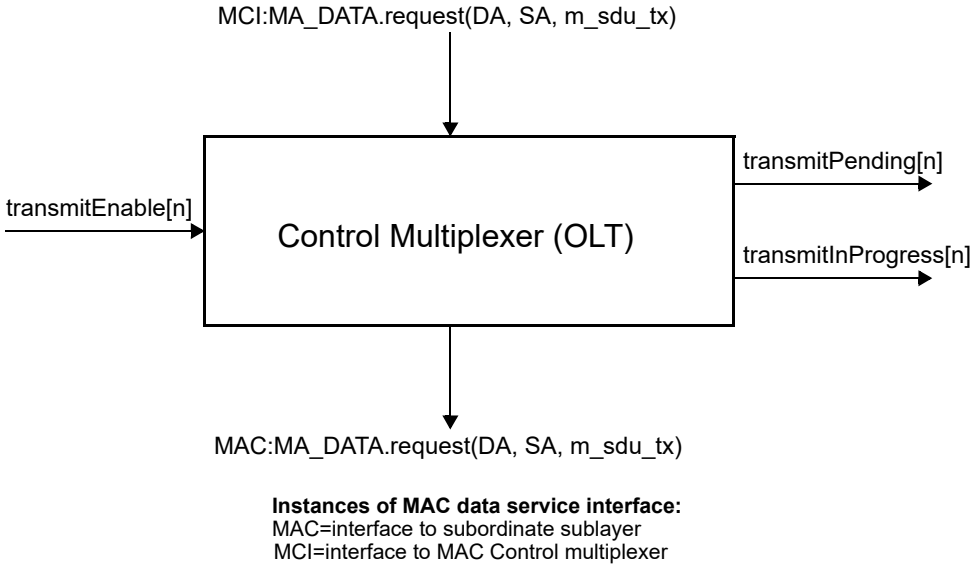


Figure 77–7—Control Parser service interfaces



NOTE—MAC:MA_DATA.request primitive may be issued from multiple MAC Control processing blocks.

Figure 77–8—OLT Control Multiplexer service interfaces

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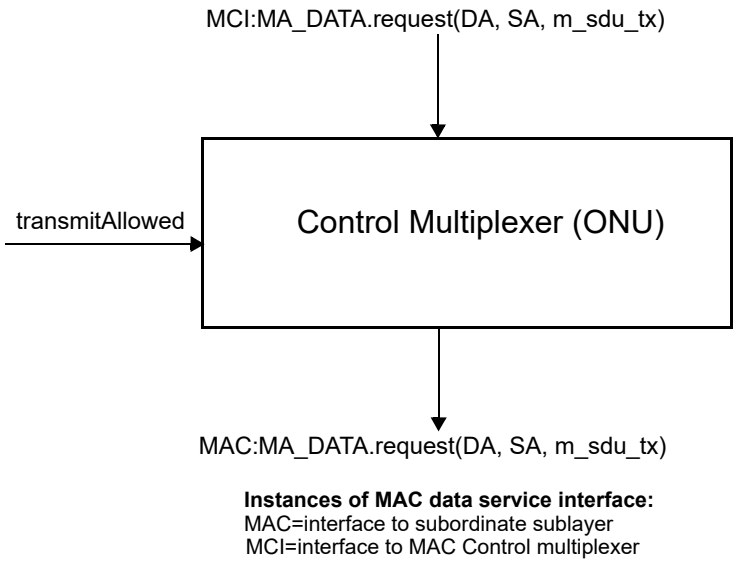

NOTE—MAC:MA_DATA.request primitive may be issued from multiple MAC Control processing blocks.

Figure 77–9—ONU Control Multiplexer service interfaces

77.2.2.1 Constants

FEC_CODEWORD_SIZE
TYPE: integer
This constant represents the size of FEC codeword in octets (FEC_PAYLOAD_SIZE + FEC_PARITY_SIZE).
Value: 248

FEC_PARITY_SIZE
TYPE: integer
This constant represents the size of FEC codeword parity field in octets.
Value: 32

FEC_PAYLOAD_SIZE
TYPE: integer
This constant represents the size of FEC codeword payload in octets.
VALUE: 216

guardThresholdOLT
TYPE: integer
This constant holds the maximum amount of drift allowed for a timestamp received at the OLT. This value is measured in units of time_quantum.
VALUE: 12

guardThresholdONU
TYPE: integer
This constant holds the maximum amount of drift allowed for a timestamp received at the ONU. This value is measured in units of time_quantum.
VALUE: 8

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MAC_Control_type
TYPE: integer
The value of the Length/Type field as defined in 31.4.1.3.
VALUE: 0x8808

tailGuard
TYPE: integer
This constant holds the value used to reserve space at the end of the upstream transmission at the ONU in addition to the size of last MAC service data unit (m_sdu) in units of octets. Space is allocated for the MAC overheads including: preamble, SFD, DA, SA, Length/Type, FCS, and minimum interpacket gap. The sizes of the above listed MAC overhead items are described in 3.1.1. The size of the minimum IPG is described in 4A.4.2.
VALUE: 38

time_quantum
This variable is defined in 64.2.2.1.

tqSize
TYPE: integer
This constant represents time_quantum in octet transmission times.
VALUE: 20

77.2.2.2 Counters

localTime
TYPE: 32 bit unsigned
This variable holds the value of the local timer used to control MPCP operation. This variable is advanced by a timer at 62.5 MHz, and counts in time_quanta. At the OLT the counter shall track the transmit clock, while at the ONU the counter shall track the receive clock. For accuracy of receive clock see 76.4.1.2. It is reloaded with the received timestamp value (from the OLT) by the Control Parser (see Figure 77–12). Changing the value of this variable while running using Layer Management is highly undesirable and is unspecified.

77.2.2.3 Variables

BEGIN
TYPE: Boolean
This variable is used when initiating operation of the functional block state diagram. It is set to true following initialization and every reset.

fecOffset
TYPE: 32 bit unsigned
A variable that advances by 1 after every 8 bit times. After reaching the value of FEC_CODEWORD_SIZE, this variable is reset to zero. In the OLT, this variable is initialized to 0 at system initialization. In the ONU, this variable is assigned in the ONU Control Multiplexer state diagram (see Figure 77–14).
NOTE—Notation fecOffset[1:0] refers to two least significant bits of this variable.

data_rx
TYPE: bit array
This variable represents a 0–based bit array corresponding to the payload of a received MPCPDU. This variable is used to parse incoming MPCPDU frames.

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data_tx

TYPE: bit array

This variable represents a 0-based bit array corresponding to the payload of an MPCPDU being transmitted. This variable is used to access payload of outgoing MPCPDU frames, for example to set the timestamp value.

flags_rx

TYPE: 8-bit unsigned

This variable holds the value of the Flags field from the last received MPCPDU.

grantStart

TYPE: Boolean

This variable indicates beginning of a grant transmission. It is set to true in the GATE Processing ONU Activation state diagram (see Figure 77–30) when a new grant activates. It is reset to false after the transmission of the first frame in the grant (see Figure 77–14). This variable is defined in ONU only.

IdleGapCount

TYPE: 32-bit unsigned

This variable represents length of gap between subsequent frames, expressed in the unit of octet time. This variable advances by 1 after every 8-bit times.

newRTT

TYPE: 16 bit unsigned

This variable temporary holds a newly–measured Round Trip Time to the ONU. The new RTT value is represented in units of time_quanta.

m_sdu_rx

TYPE: bit array

Equal to the concatenation of the Length/Type and data_rx variables.

m_sdu_tx

TYPE: bit array

Equal to the concatenation of the Length/Type and data_tx variables.

m_sdu_ctl

TYPE: bit array

Equal to the concatenation of the MAC_Control_type and data_tx variables.

OctetsRemaining

TYPE: 32 bit unsigned

This variable is an alias for the expression (((stopTime – localTime) × tqSize) – tqOffset). It denotes the number of octets that can be transmitted between the current time and the end of the grant.

OctetsRequired

TYPE: 16 bit unsigned

This variable represents a total transmission time of next packet and is used to check whether the next packet fits in the remainder of ONU's transmission window. The value of OctetsRequired includes packet transmission time, tailGuard defined in 77.2.2.1, and FEC parity data overhead. This variable is measured in units of octets.

opcode_rx

TYPE: 16 bit unsigned

This variable holds an opcode of the last received MPCPDU.

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opcode_tx
: TYPE: 16 bit unsigned
This variable holds an opcode of an outgoing MPCPDU.

packet_initiate_delay
: TYPE: 16 bit unsigned
This variable is used to set the time–out interval for packet_initiate_timer defined in 77.2.2.5. The packet_initiate_delay value is represented in units of octets.

ResetBound
: TYPE: 32-bit unsigned
This variable represents the value of DelayBound (see 76.3.1.2) expressed in units of octet time (i.e., ResetBound = 8 * DelayBound).

RTT
: TYPE: 16 bit unsigned
This variable holds the measured Round Trip Time to the ONU. The RTT value is represented in units of time_quanta.

stopTime
: TYPE: 32 bit unsigned
This variable holds the value of the localTime counter corresponding to the end of the nearest grant. This value is set by the Gate Processing function as described in 77.3.5.

timestamp
: TYPE: 32 bit unsigned
This variable holds the value of timestamp of the last received MPCPDU frame.

timestampDrift
: TYPE: Boolean
This variable is used to indicate whether an error is signaled as a result of uncorrectable timestamp drift.

tqOffset
: TYPE: 8 bit unsigned
This variable denotes the offset (in octet times) of the current actual time from the localTime variable (which maintains the current time in units of time_quanta).

transmitAllowed
: TYPE: Boolean
This variable is used to control PDU transmission at the ONU. It is set to true when the transmit path is enabled, and is set to false when the transmit path is being shut down. transmitAllowed changes its value according to the state of the Gate Processing functional block.

transmitEnable
: TYPE: Boolean array
This array contains one element per each Multipoint MAC Control instance. Elements of this array are used to control the transmit path in the Multipoint MAC Control instance at the OLT. Setting an element to TRUE indicates that the selected instance is permitted to transmit a frame. Setting it to FALSE inhibits the transmission of frames in the selected instance. Only one element of transmitEnable should be set to TRUE at a time.

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transmitInProgress
TYPE: Boolean array
This array contains one element per each Multipoint MAC Control instance. The element *j* of this array set to on indicates that the Multipoint MAC Control instance *j* is in the process of transmitting a frame.

transmitPending
TYPE: Boolean array
This array contains one element per each Multipoint MAC Control instance. The element *j* of this array set to on indicates that the Multipoint MAC Control instance *j* is ready to transmit a frame.

77.2.2.4 Functions

abs(n)
This function returns the absolute value of the parameter n.

Opcode–specific function(opcode)
Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

CheckGrantSize(length)
This function calculates the future time at which the transmission of the current frame (including the FEC parity overhead) is completed.

$$\text{CheckGrantSize(length)} = \left\lceil \frac{\text{fecOffset} + \text{length}}{\text{FEC\_PAYLOAD\_SIZE}} \right\rceil \times \text{FEC\_CODEWORD\_SIZE} - \text{fecOffset}$$

NOTE—The notation $\lceil x \rceil$ represents a *ceiling* function, which returns the value of its argument *x* rounded up to the nearest integer.

FEC_Overhead(length)
This function calculates the additional amount of time (in octet times) that the MPCP control multiplexer waits following transmission of a frame of size 'length' by the MAC. The additional time is added to allow the insertion of parity data into the frame by the PHY layer. As described in 76.3.2.4, FEC encoder adds 32 parity octets for each block of 216 data or control octets. FEC_Overhead() returns the number of octets that the PHY inserts during transmission of a particular packet and its subsequent IPG. Parameter 'length' represents the size of an entire frame including preamble, SFD, DA, SA, Length/Type, FCS, and IPG. The following formula is used to calculate the overhead:

$$\text{FEC\_Overhead(length)} = 12 + \text{FEC\_PARITY\_SIZE} \times \left\lfloor \frac{\text{fecOffset} + \text{length}}{\text{FEC\_PAYLOAD\_SIZE}} \right\rfloor$$

NOTE—The notation $\lfloor x \rfloor$ represents a *floor* function, which returns the value of its argument *x* rounded down to the nearest integer.

select()
This function selects the next Multipoint MAC Control instance allowed to initiate transmission of a frame. The function returns an index to the transmitPending array for which the value is not false. The selection criteria in the presence of multiple active elements in the list is implementation dependent.

SelectFrame()
This function enables the interface, which has a pending frame. If multiple interfaces have frames waiting at the same time, only one interface is enabled. The selection criteria is not specified,

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except for the case when some of the pending frames have Length/Type = MAC_Control. In this case, one of the interfaces with a pending MAC Control frame shall be enabled.

sizeof(sdu)
: This function returns the size of the sdu in octets.

transmissionPending()
: This function returns true if any of the Multipoint MAC Control instances has a frame waiting to be transmitted. The function can be represented as:

```
transmissionPending() =
   transmitPending[0] +
   transmitPending[1] +
   ... +
   transmitPending[n-1]
```

where n is the total number of Multipoint MAC Control instances.

77.2.2.5 Timers

packet_initiate_timer
: This timer is used to delay frame transmission from MAC Control to avoid variable MAC delay while MAC enforces IPG after a previous frame. In addition, this timer increases interframe spacing just enough to accommodate the extra parity data to be added by the FEC encoder.

77.2.2.6 Messages

MAC:MA_DATA.indication(DA, SA, m_sdu, receiveStatus)
: The service primitive is defined in 31.3.

MCF:MA_DATA.indication(DA, SA, m_sdu, receiveStatus)
: The service primitive is defined in 31.3.

MAC:MA_DATA.request (DA, SA, m_sdu)
: The service primitive is defined in 31.3. The action invoked by this service primitive is not considered to end until the transmission of the frame by the MAC has concluded. The ability of the MAC control layer to determine this is implementation dependent.

MCF:MA_DATA.request (DA, SA, m_sdu)
: The service primitive is defined in 31.3.

77.2.2.7 State diagrams

The Multipoint transmission control function in the OLT shall implement state diagram shown in Figure 77–10. Control parser function in the OLT shall implement state diagram shown in Figure 77–11. Control parser function in the ONU shall implement state diagram shown in Figure 77–12. Control multiplexer function in the OLT shall implement state diagram shown in Figure 77–13. Control multiplexer function in the ONU shall implement state diagram shown in Figure 77–14.

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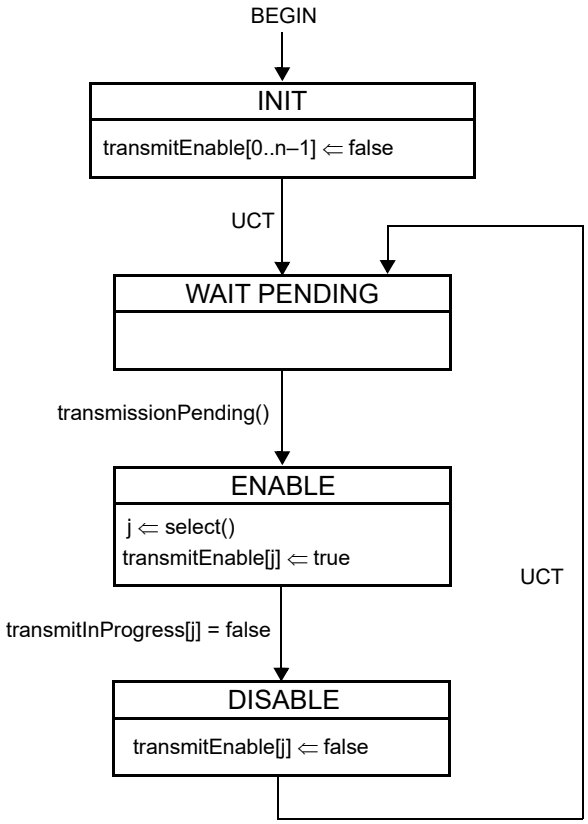

Figure 77–10—OLT Multipoint Transmission Control state diagram

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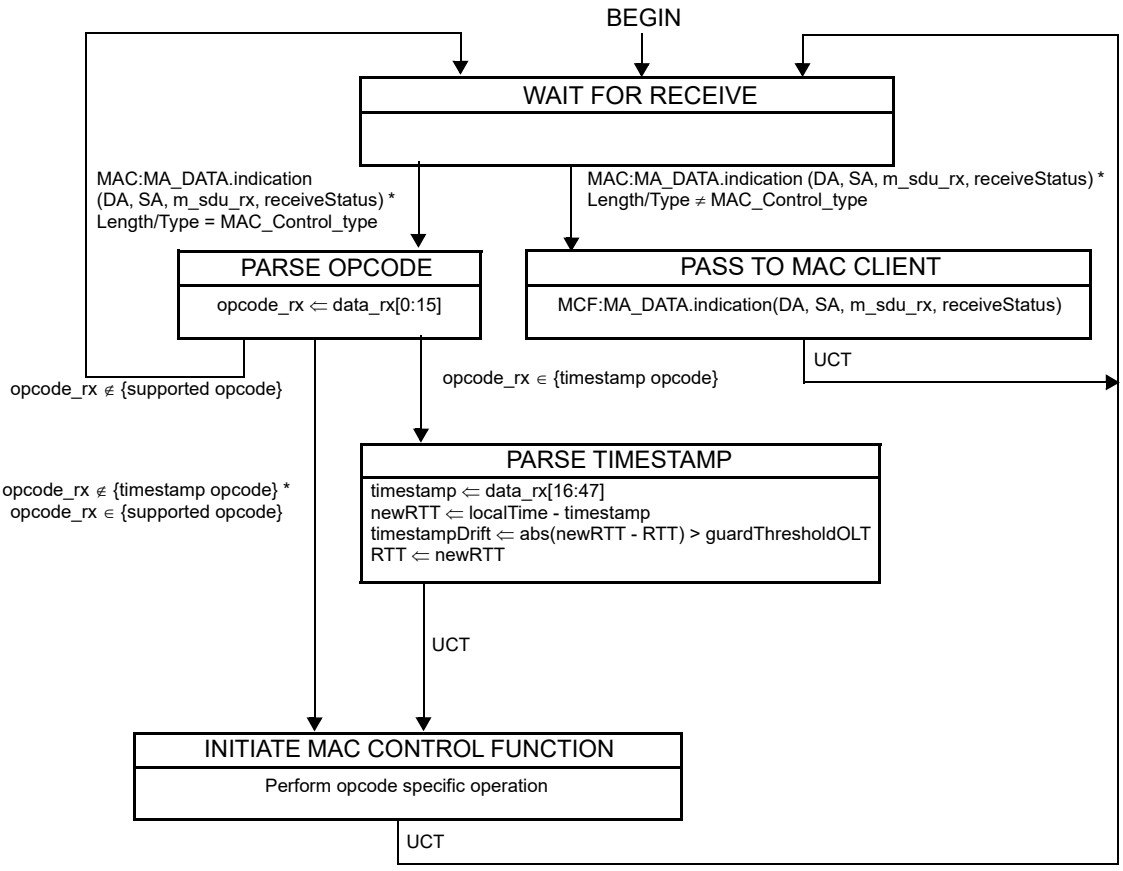

Instances of MAC data service interface:
MAC=interface to subordinate sublayer
MCF=interface to MAC Control client

NOTE—The opcode–specific operation is launched as a parallel process by the MAC Control sublayer, and not as a synchronous function. Progress of the generic MAC Control Receive state diagram (as shown in this figure) is not implicitly impeded by the launching of the opcode specific function.

Refer to Annex 31A for list of supported opcodes and timestamp opcodes.

Figure 77–11—OLT Control Parser state diagram

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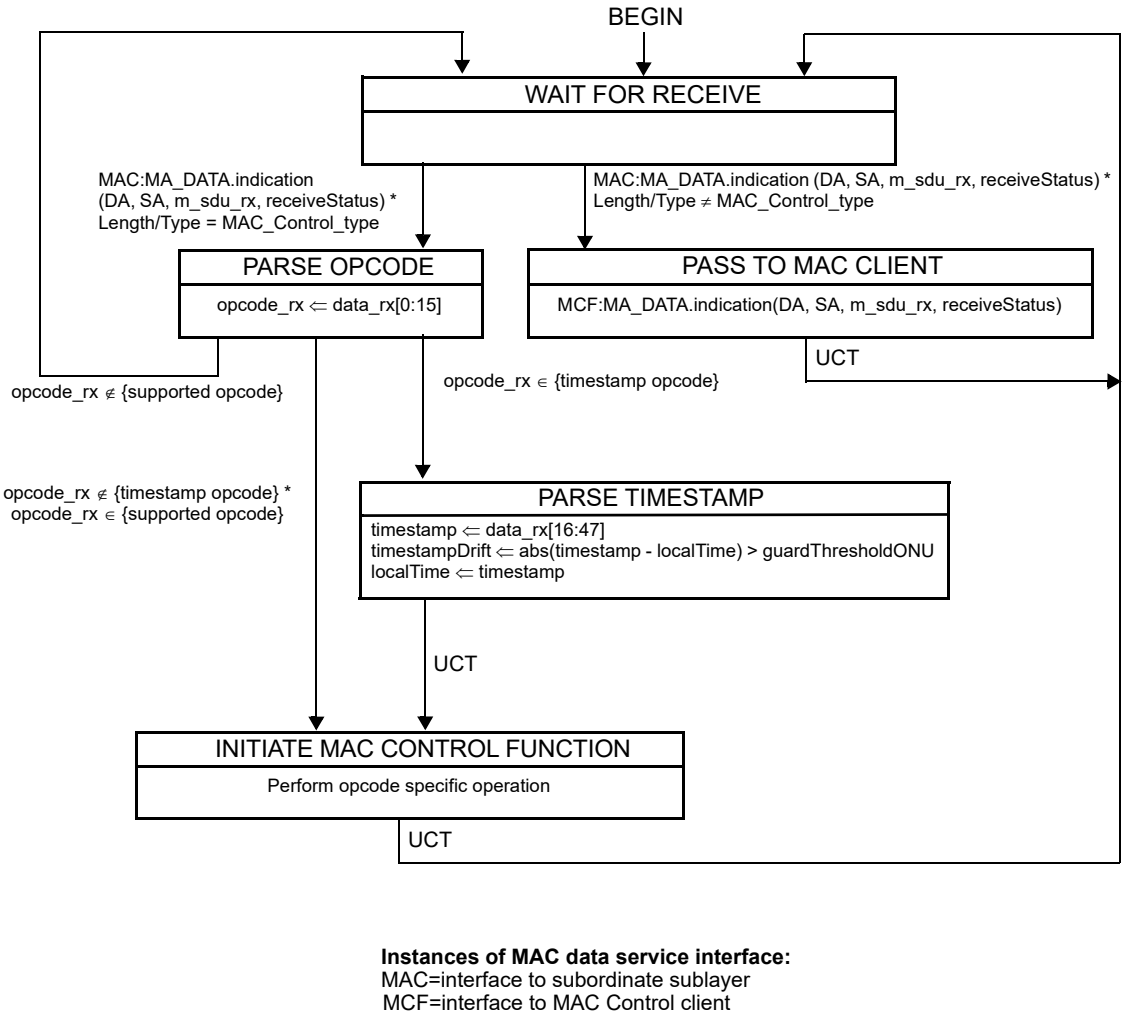

NOTE—The opcode–specific operation is launched as a parallel process by the MAC Control sublayer, and not as a synchronous function. Progress of the generic MAC Control Receive state diagram (as shown in this figure) is not implicitly impeded by the launching of the opcode specific function.

Refer to Annex 31A for list of supported opcodes and timestamp opcodes.

Figure 77–12—ONU Control Parser state diagram

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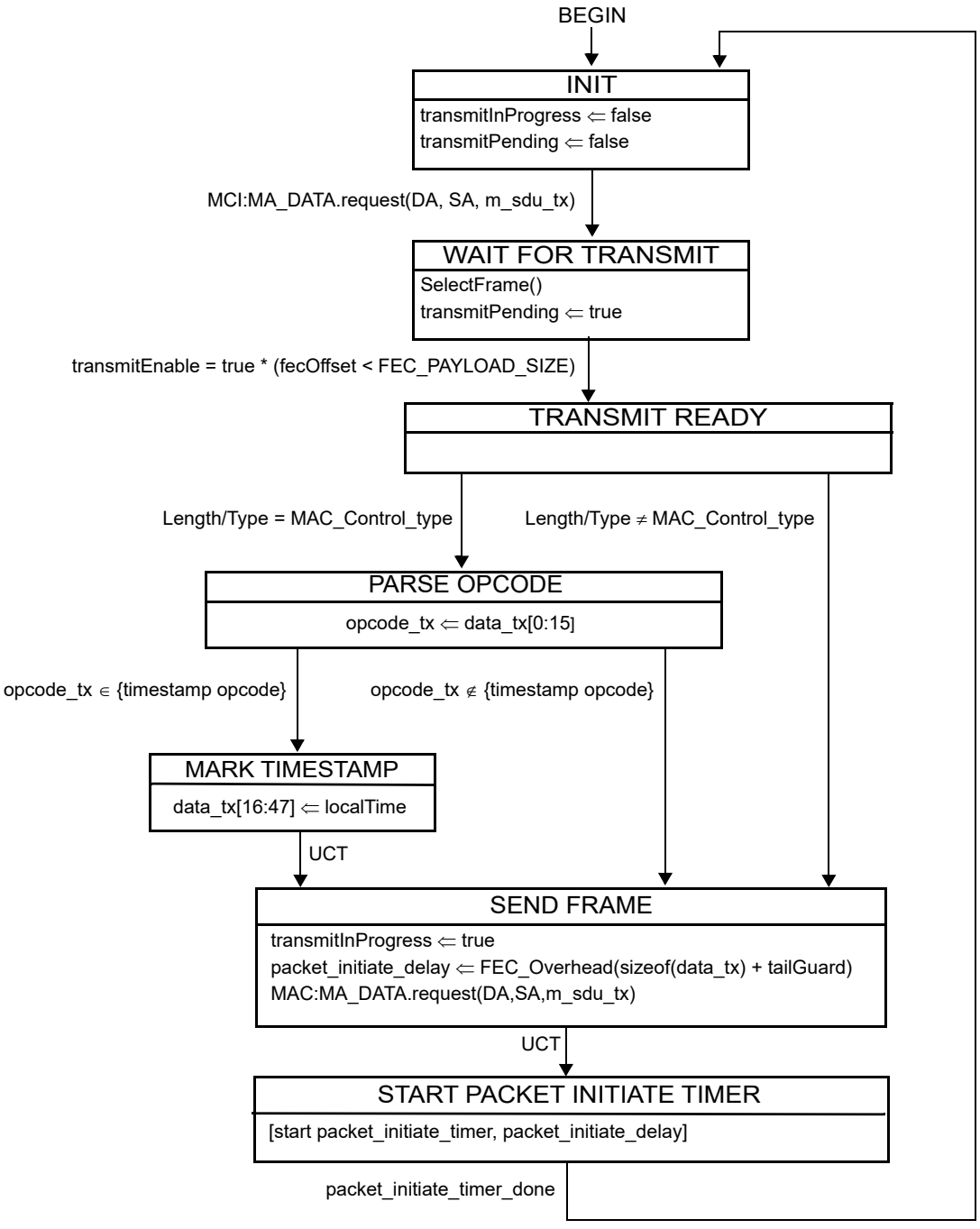

Instances of MAC data service interface:
MAC=interface to subordinate sublayer
MCI=interface to MAC Control multiplexer

Figure 77–13—OLT Control Multiplexer state diagram

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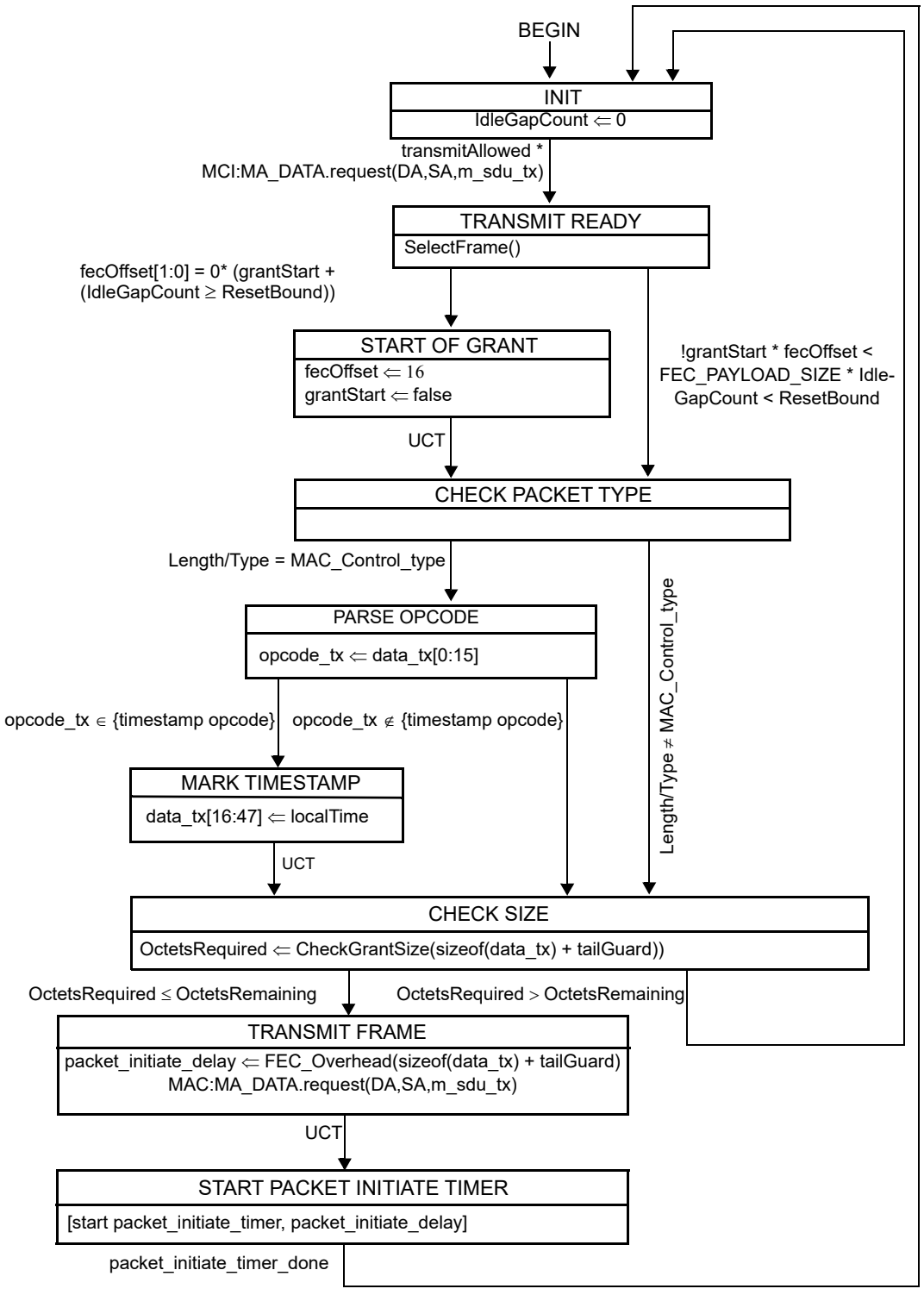

Instances of MAC data service interface:
MAC=interface to subordinate sublayer
MCI=interface to MAC Control multiplexer

Figure 77–14—ONU Control Multiplexer state diagram

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77.3 Multipoint Control Protocol (MPCP)

As depicted in Figure 77–4, the Multipoint MAC Control functional block comprises the following functions:

a) *Discovery Processing*. This block manages the discovery process, through which an ONU is discovered and registered with the network while compensating for RTT.
b) *Report Processing*. This block manages the generation and collection of report messages, through which bandwidth requirements are sent upstream from the ONU to the OLT.
c) *Gate Processing*. This block manages the generation and collection of gate messages, through which multiplexing of multiple transmitters is achieved.

As depicted in Figure 77–4, the layered system may instantiate multiple MAC entities, using a single Physical Layer. Each instantiated MAC communicates with an instance of the opcode specific functional blocks through the Multipoint MAC Control. In addition some global variables are shared across the multiple instances. Common state control is used to synchronize the multiple MACs using MPCP procedures. Operation of the common state control is generally considered outside the scope of this document.

77.3.1 Principles of Multipoint Control Protocol

Multipoint MAC Control enables a MAC Client to participate in a point-to-multipoint optical network by allowing it to transmit and receive frames as if it was connected to a dedicated link. In doing so, it employs the following principles and concepts:

a) A MAC client transmits and receives frames through the Multipoint MAC Control sublayer.
b) The Multipoint MAC Control decides when to allow a frame to be transmitted using the client interface Control Multiplexer.
c) Given a transmission opportunity, the MAC Control may generate control frames that would be transmitted in advance of the MAC Client's frames, utilizing the inherent ability to provide higher priority transmission of MAC Control frames over MAC Client frames.
d) Multiple MACs operate on a shared medium by allowing only a single MAC to transmit upstream at any given time across the network using a time-division multiple access (TDMA) method.
e) Such gating of transmission is orchestrated through the Gate Processing function.
f) New devices are discovered in the network and allowed transmission through the Discovery Processing function.
g) Fine control of the network bandwidth distribution can be achieved using feedback mechanisms supported in the Report Processing function.
h) The operation of P2MP network is asymmetric, with the OLT assuming the role of master, and the ONU assuming the role of slave.

77.3.2 Compatibility considerations

77.3.2.1 PAUSE operation

Even though MPCP is compatible with flow control, optional use of flow control may not be efficient in the case of large propagation delay. If flow control is implemented, then the timing constraints in Annex 31B supplement the constraints found at 77.3.2.4.

NOTE—MAC at an ONU can receive frames from unicast channel and SCB channel. If the SCB channel is used to broadcast data frames to multiple ONUs, the ONU's MAC may continue receiving data frames from SCB channel even after the ONU has issued a PAUSE request to its unicast remote-end.

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77.3.2.2 Optional Shared LAN emulation

By combining P2PE, suitable filtering rules at the ONU, and suitable filtering and forwarding rules at the OLT, it is possible to emulate an efficient shared LAN. Support for shared LAN emulation is optional, and requires an additional layer above the MAC, which is out of scope for this document. Thus, shared LAN emulation is introduced here for informational purposes only.

Specific behavior of the filtering layer at the RS is specified in 76.2.6.1.3.2.

77.3.2.3 Multicast and single copy broadcast support

In the downstream direction, the PON is a broadcast medium. In order to make use of this capability for forwarding broadcast frames from the OLT to multiple recipients without multiple duplication for each ONU, the SCB and multicast LLID support is introduced.

The OLT has at least one MAC associated with every ONU. In addition one more MAC at the OLT is marked as the SCB MAC. Moreover, the OLT has a multicast MAC associated with each defined multicast LLID. The SCB MAC handles all downstream broadcast traffic, but is never used in the upstream direction for client traffic, except for client registration. Similarly, the multicast MACs handle downstream multicast traffic, but are never used in the upstream direction for client traffic. Optional higher layers may be implemented to perform selective broadcast and multicast of frames. Such layers may require additional MACs (multicast MACs) to be instantiated in the OLT for some or all ONUs increasing the total number of MACs beyond the number of ONUs + 1.

When connecting the SCB MAC or a multicast MAC to an IEEE 802.1Q bridge port it is possible that loops may be formed due to the broadcast or multicast nature of the associated LLIDs. Thus it is recommended that this MAC not be connected to an IEEE 802.1Q bridge port.

Configuration of SCB channels as well as filtering and marking of frames for support of SCB is defined in 76.2.6.1.3.2 for 10G–EPON compliant Reconciliation Sublayers.

77.3.2.4 Delay requirements

The MPCP protocol relies on strict timing based on distribution of timestamps. A compliant implementation needs to guarantee a constant delay through the MAC and PHY in order to maintain the correctness of the timestamping mechanism. The actual delay is implementation dependent; however, a complying implementation shall maintain a delay variation of no more than 1 time_quantum through the MAC.

The OLT shall not grant less than 1024 time_quanta into the future, in order to allow the ONU processing time when it receives a gate message. The ONU shall process all messages in less than this period. The OLT shall not issue more than one message every 1024 time_quanta to a single ONU. The unit of time_quantum is defined in 77.2.2.1.

77.3.3 Discovery processing

Discovery is the process whereby newly connected or off-line ONUs are provided access to the PON. The process is driven by the OLT, which periodically makes available Discovery Windows during which off-line ONUs are given the opportunity to make themselves known to the OLT. The periodicity of these windows is unspecified and left up to the implementer. The OLT signifies that a discovery period is occurring by broadcasting a discovery GATE MPCPDU, which includes the starting time and length of the discovery window, along with the Discovery Information flag field, as defined in 77.3.6.1. With the appropriate settings of individual flags contained in this 16 bit wide field, the OLT notifies all the ONUs about its upstream and downstream channel transmission capabilities. Note that the OLT may simultaneously support more than one data rate in the given transmission direction.

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Off-line ONUs, upon receiving a Discovery GATE MPCPDU, wait for the period to begin and then transmit a REGISTER_REQ MPCPDU to the OLT. Discovery windows are unique in that they are the only times when multiple ONUs can access the PON simultaneously, and transmission overlap can occur. In order to reduce transmission overlaps, a contention algorithm is used by all ONUs. Measures are taken to reduce the probability for overlaps by artificially simulating a random distribution of distances from the OLT. Each ONU waits a random amount of time before transmitting the REGISTER_REQ MPCPDU that is shorter than the length of the discovery window. It should be noted that multiple valid REGISTER_REQ MPCPDUs can be received by the OLT during a single discovery window. Included in the REGISTER_REQ MPCPDU is the ONU's MAC address and number of maximum pending grants. Additionally, a registering ONU notifies the OLT of its transmission capabilities in the upstream and downstream channels by setting appropriately the flags in the Discovery Information field, as specified in 77.3.6.3.

Note that even though a compliant ONU is not prohibited from supporting more than one data rate in any transmission channel, it is expected that a single supported data rate for upstream and downstream channel is indicated in the Discovery Information field. Moreover, in order to assure maximum utilization of the upstream channel and to decrease the required size of the guard band between individual data bursts, the registering ONU notifies the OLT of the laser on/off times, by setting appropriate values in the Laser On Time and Laser Off Time fields, where both values are expressed in the units of time_quanta.

Upon receipt of a valid REGISTER_REQ MPCPDU, the OLT registers the ONU, allocating and assigning a new port identity (LLID), and bonding a corresponding MAC to the LLID.

The next step in the process is for the OLT to transmit a REGISTER MPCPDU to the newly discovered ONU, which contains the ONU's LLID, and the OLT's required synchronization time. Moreover, the OLT echoes the maximum number of pending grants. The OLT also sends the target value of laser on time and laser off time, which may be different than laser on time and laser off time delivered by the ONU in the REGISTER_REQ MPCPDU.

The OLT now has enough information to schedule the ONU for access to the PON and transmits a standard GATE message allowing the ONU to transmit a REGISTER_ACK. Upon receipt of the REGISTER_ACK, the discovery process for that ONU is complete, the ONU is registered and normal message traffic can begin. It is the responsibility of Layer Management to perform the MAC bonding, and start transmission from/to the newly registered ONU. The discovery message exchange is illustrated in Figure 77–15.

There may exist situations when the OLT requires that an ONU go through the discovery sequence again and reregister. Similarly, there may be situations where an ONU needs to inform the OLT of its desire to deregister. The ONU can then reregister by going through the discovery sequence. For the OLT, the REGISTER message may indicate a value, Reregister or Deregister, that if either is specified forces the receiving ONU into reregistering. For the ONU, the REGISTER_REQ message contains the Deregister bit that signifies to the OLT that this ONU should be deregistered.

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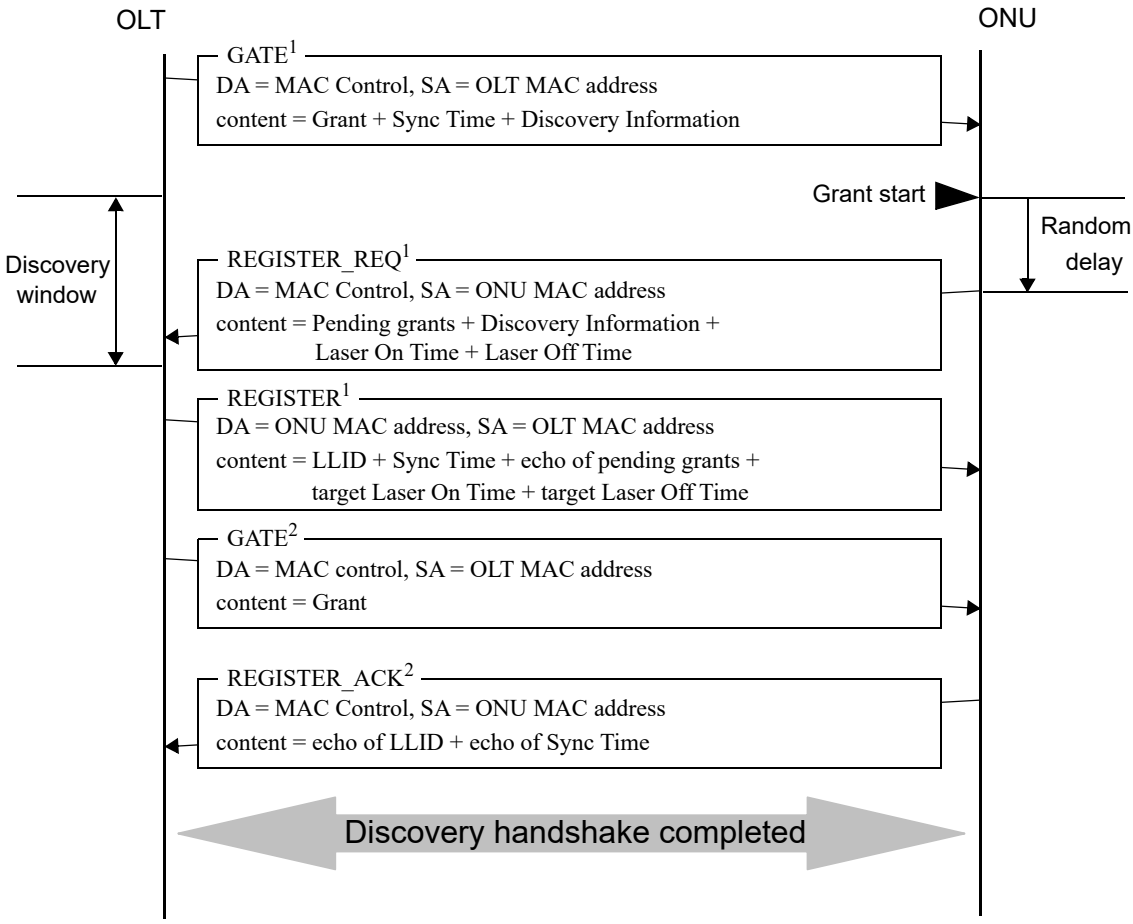

[1] Messages sent on a broadcast channel
[2] Messages sent on unicast channels

Figure 77–15—Discovery handshake message exchange

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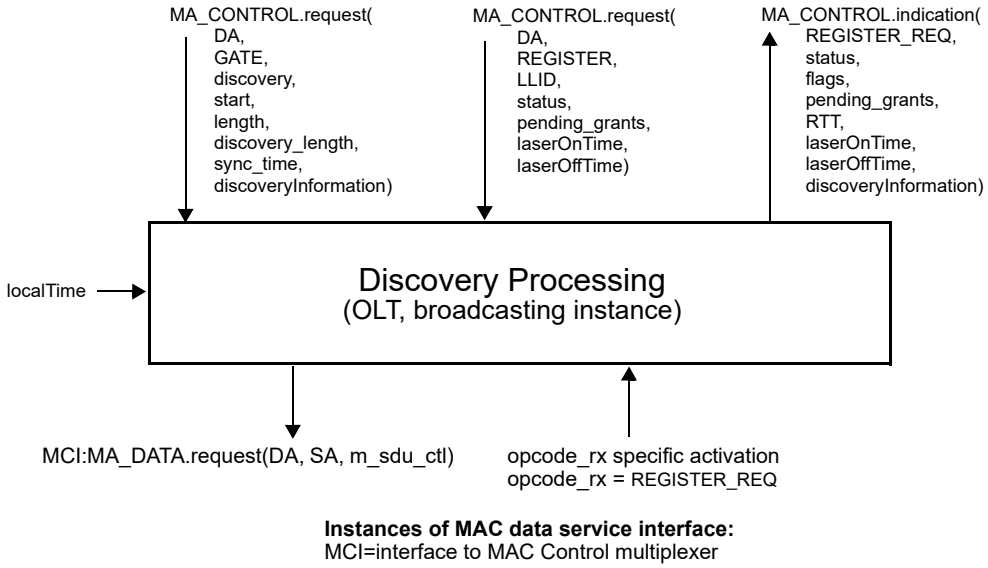

Figure 77–16—Discovery Processing service interfaces (OLT, broadcasting instance)

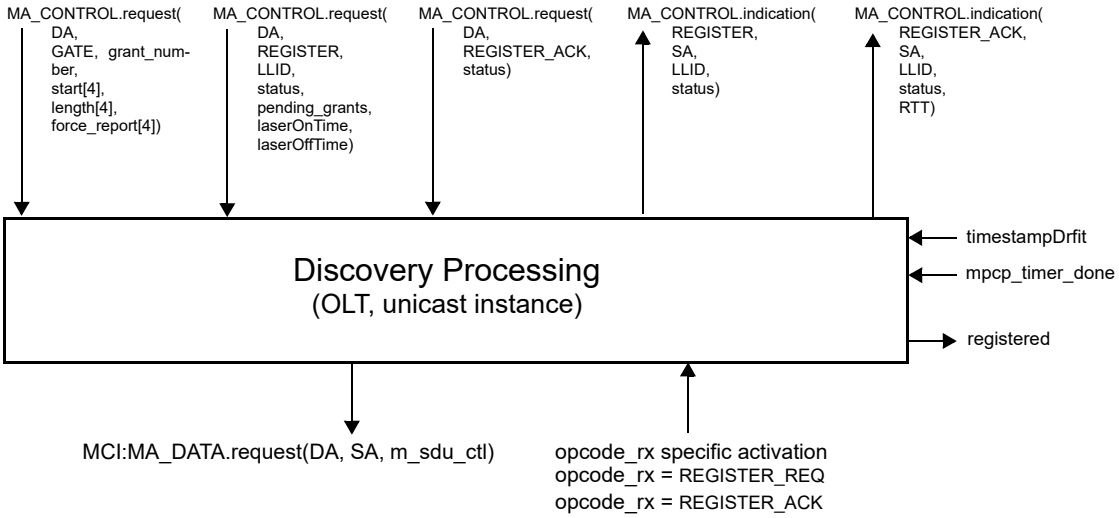

Figure 77–17—Discovery Processing service interfaces (OLT, unicasting instance)

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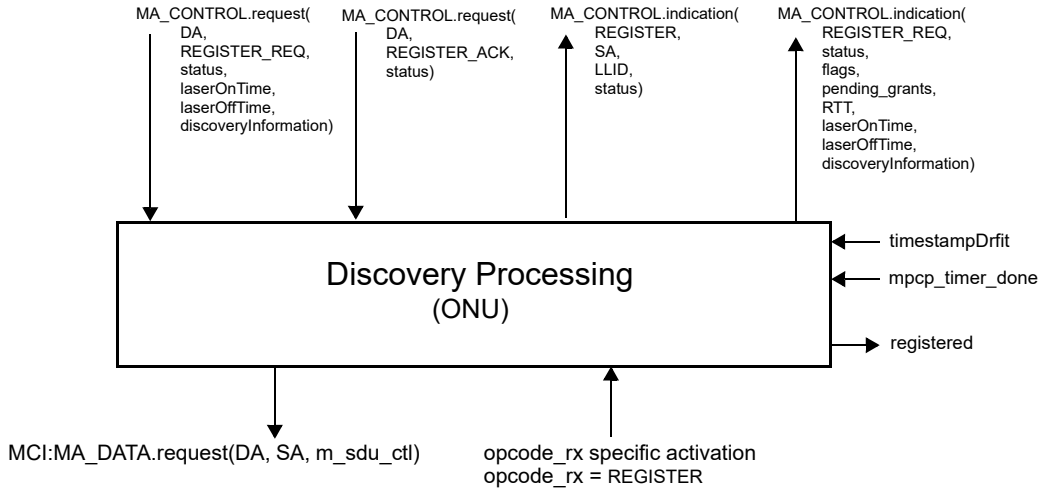

Figure 77–18—Discovery Processing service interfaces (ONU)

77.3.3.1 Constants

laserOffTimeCapability

TYPE: 8 bit unsigned

This constant represents the time required to terminate the laser, in units of time_quantum. While the default value corresponds to a maximum allowed T_{off} (as specified in Table 75–8 and Table 75–9), implementations may set it to the actual value time period required for turning off the PMD, as specified in 75.7.14.

VALUE: 0x20 (512 ns, default value)

laserOnTimeCapability

TYPE: 8 bit unsigned

This constant represents the time required to initialize the laser, in units of time_quantum. While the default value corresponds to a maximum allowed T_{on} (as specified in Table 75–8 and Table 75–9), implementations may set it to the actual value time period required for turning on the PMD, as specified in 75.7.14.

VALUE: 0x20 (512 ns, default value)

77.3.3.2 Variables

BEGIN

This variable is defined in 77.2.2.3.

data_rx

This variable is defined in 77.2.2.3.

data_tx

This variable is defined in 77.2.2.3.

grantEndTime

TYPE: 32 bit unsigned

This variable holds the time at which the OLT expects the ONU grant to complete. Failure of a

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REGISTER_ACK message from an ONU to arrive at the OLT before grantEndTime is a fatal error in the discovery process, and causes registration to fail for the specified ONU, who may then retry to register. The value of grantEndTime is measured in units of time_quantum.

insideDiscoveryWindow

TYPE: Boolean

This variable holds the current status of the discovery window. It is set to true when the discovery window opens, and is set to false when the discovery window closes.

laserOffTime

TYPE: 8 bit unsigned

This variable holds the time required to terminate the laser. It counts in time_quanta units the time period required for turning off the PMD, as specified by the value of T_{off} in 75.7.14.

VALUE: laserOffTimeCapability (default value)

laserOnTime

TYPE: 8 bit unsigned

This variable holds the time required to initiate the PMD. It counts in time_quanta units the time period required for turning on the PMD, as specified by the value of T_{on} in 75.7.14.

VALUE: laserOnTimeCapability (default value)

localTime

This variable is defined in 77.2.2.2.

m_sdu_ctl

This variable is defined in 77.2.2.3.

opcode_rx

This variable is defined in 77.2.2.3.

pendingGrants

TYPE: 16 bit unsigned

This variable holds the maximum number of pending grants that an ONU is able to queue.

registered

TYPE: Boolean

This variable holds the current result of the Discovery Process. It is set to true once the discovery process is complete and registration is acknowledged.

syncTime

TYPE: 16 bit unsigned

This variable holds the time required to stabilize the receiver at the OLT. It counts time_quanta units from the point where transmission output is stable to the point where synchronization has been achieved. The value of syncTime includes gain adjustment interval ($T_{receiver\_settling}$), clock synchronization interval (T_{CDR}), and code–group alignment interval ($T_{code\_group\_align}$), as specified in 75.7.14. The OLT conveys the value of syncTime to ONUs in Discovery GATE and REGISTER messages. During the synchronization time a 10/1G–EPON ONU transmits only IDLE patterns, and a 10/10G–EPON ONU sends synchronization pattern (SP, see 76.3.2.5.2) followed by burst delimiter pattern (BURST_DELIMITER, see 76.3.2.5.2).

timestampDrift

This variable is defined in 77.2.2.3.

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77.3.3.3 Functions

None.

77.3.3.4 Timers

discovery_window_size_timer
: This timer is used to wait for the event signaling the end of the discovery window.
VALUE: The timer value is set dynamically based on the parameters received in a DISCOVERY GATE message.

mpcp_timer
: This timer is used to measure the arrival rate of MPCP frames in the link. Failure to receive frames is considered a fatal fault and leads to deregistration.

77.3.3.5 Messages

MA_DATA.indication(DA, SA, m_sdu, receiveStatus)
: The service primitive is defined in 2.3.2.

MA_DATA.request (DA, SA, m_sdu)
: The service primitive is defined in 2.3.2.

MA_CONTROL.request(DA, GATE, discovery, start, length, discovery_length, sync_time, discoveryInformation)
: The service primitive is used by the MAC Control client at the OLT to initiate the Discovery Process. This primitive takes the following parameters:

DA:	Multicast or unicast MAC address.
GATE:	Opcode for GATE MPCPDU as defined in Table 31A–1.
discovery:	Flag specifying that the given GATE message is to be used for discovery only.
start:	Start time of the discovery window.
length:	Length of the grant given for discovery.
discovery_length:	Length of the discovery window process.
sync_time:	The time interval required to stabilize the receiver at the OLT.
discoveryInformation:	This parameter represents the Discovery Information field in GATE MPCPDU as specified in 77.3.6.1, defining the speed(s) the OLT is capable of receiving and speed(s) at which the discovery window is opened for.

MA_CONTROL.request(DA, GATE, grant_number, start[4], length[4], force_report[4])
: This service primitive is used by the MAC Control client at the OLT to issue the GATE message to an ONU. This primitive takes the following parameters:

DA:	Multicast MAC Control address as defined in Annex 31B.
GATE:	Opcode for GATE MPCPDU as defined in Table 31A–1.
grant_number:	Number of grants issued with this GATE message. The number of grants ranges from 0 to 4.
start[4]:	Start times of the individual grants. Only the first grant_number elements of the array are used.
length[4]:	Lengths of the individual grants. Only the first grant_number elements of the array are used.

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force_report[4]: Flags indicating whether a REPORT message should be generated in the corresponding grant. Only the first grant_number elements of the array are used.

MA_CONTROL.request(DA, REGISTER_REQ, status, laserOnTime, laserOffTime, discoveryInformation)

The service primitive is used by a client at the ONU to request the Discovery Process to perform a registration. This primitive takes the following parameters:

DA: Multicast MAC Control address as defined in Annex 31B.

REGISTER_REQ: opcode for REGISTER_REQ MPCPDU as defined in Table 31A–1.

status: This parameter takes on the indication supplied by the flags field in the REGISTER_REQ MPCPDU as defined in Table 77–5.

laserOnTime: This parameter holds the laserOnTime value, expressed in units of time_quanta, as reported by MAC client and specified in 77.3.6.3.

laserOffTime: This parameter holds the laserOffTime value, expressed in units of time_quanta, as reported by MAC client and specified in 77.3.6.3.

discoveryInformation: This parameter represents the Discovery Information field, as specified in 77.3.6.3, defining the speed(s) the ONU is capable of transmitting and speed(s) at which the registration attempt is made.

MA_CONTROL.indication(REGISTER_REQ, status, flags, pending_grants, RTT, laserOnTime, laserOffTime, discoveryInformation)

The service primitive is issued by the Discovery Process to notify the client and Layer Management that the registration process is in progress. This primitive takes the following parameters:

REGISTER_REQ: Opcode for REGISTER_REQ MPCPDU as defined in Table 31A–1.

status: This parameter holds the values incoming or retry. Value incoming is used at the OLT to signal that a REGISTER_REQ message was received successfully. The value retry is used at the ONU to signal to the client that a registration attempt failed and needs to be repeated.

flags: This parameter holds the contents of the flags field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the OLT.

pending_grants: This parameter holds the contents of the pending_grants field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the OLT.

RTT: The measured round trip time to/from the ONU is returned in this parameter. RTT is stated in time_quanta units. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the OLT.

laserOnTime: This parameter holds the contents of the laserOnTime field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the OLT.

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laserOffTime: This parameter holds the contents of the laserOffTime field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the OLT.

discoveryInformation: This parameter holds the contents of the Discovery Information field in the REGISTER_REQ MPCPDU. This parameter holds a valid value only when the primitive is generated by the Discovery process in the OLT.

MA_CONTROL.request(DA, REGISTER, LLID, status, pending_grants, laserOnTime, laserOffTime)

The service primitive is used by the MAC Control client at the OLT to initiate acceptance of an ONU. This primitive takes the following parameters:

DA: Unicast MAC address or multicast MAC Control address as defined in Annex 31B.

REGISTER: Opcode for REGISTER MPCPDU as defined in Table 31A–1.

LLID: This parameter holds the logical link identification number assigned by the MAC Control client.

status: This parameter takes on the indication supplied by the flags field in the REGISTER MPCPDU as defined in Table 77–7.

pending_grants: This parameters echoes back the pending_grants field that was previously received in the REGISTER_REQ message.

laserOnTime: This parameter carries the target value of Laser On Time for the given ONU transmitter. This value may be different than the laserOnTime value carried in the REGISTER_REQ MPCPDU received from the corresponding ONU MAC during Discovery stage.

laserOffTime: This parameter carries the target value of Laser Off Time for the given ONU transmitter. This value may be different than the laserOffTime value carried in the REGISTER_REQ MPCPDU received from the corresponding ONU MAC during Discovery stage.

MA_CONTROL.indication(REGISTER, SA, LLID, status)

This service primitive is issued by the Discovery Process at the OLT or an ONU to notify the MAC Control client and Layer Management of the result of the change in registration status. This primitive takes the following parameters:

REGISTER: Opcode for REGISTER MPCPDU as defined in Table 31A–1.

SA: This parameter represents the MAC address of the OLT.

LLID: This parameter holds the logical link identification number assigned by the MAC Control client.

status: This parameter holds the value of accepted / denied / deregistered / reregistered.

MA_CONTROL.request(DA, REGISTER_ACK, status)

This service primitive is issued by the MAC Control clients at the ONU and the OLT to acknowledge the registration. This primitive takes the following parameters:

DA: Multicast MAC Control address as defined in Annex 31B.

REGISTER_ACK: Opcode for REGISTER_ACK MPCPDU as defined in Table 31A–1.

status: This parameter takes on the indication supplied by the flags field in the REGISTER MPCPDU as defined in Table 77–8.

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MA_CONTROL.indication(REGISTER_ACK, SA, LLID, status, RTT)

This service primitive is issued by the Discovery Process at the OLT to notify the client and Layer Management that the registration process has completed. This primitive takes the following parameters:

REGISTER_ACK:	Opcode for REGISTER_ACK MPCPDU as defined in Table 31A–1.
SA:	This parameter represents the MAC address of the reciprocating device (ONU address at the OLT, and OLT address at the ONU).
LLID:	This parameter holds the logical link identification number assigned by the MAC Control client.
status:	This parameter holds the value of accepted/denied/reset/deregistered.
RTT:	The measured round trip time to/from the ONU is returned in this parameter. RTT is stated in time_quanta units. This parameter holds a valid value only when the invoking Discovery Process in the OLT.

Opcode-specific function(opcode)

Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

77.3.3.6 State Diagrams

The Discovery Process in the OLT shall implement the discovery window setup state diagram shown in Figure 77–19, request processing state diagram as shown in Figure 77–20, register processing state diagram as shown in Figure 77–21, and final registration state diagram as shown in Figure 77–22. The discovery process in the ONU shall implement the registration state diagram as shown in Figure 77–23.

Instantiation of state diagrams as described in Figure 77–19, Figure 77–20, and Figure 77–21 is performed only at the Multipoint MAC Control instances attached to the broadcast LLID (0x7FFE). Instantiation of state diagrams as described in Figure 77–22 and Figure 77–23 is performed for every Multipoint MAC Control instance, except the instance attached to the broadcast channel.

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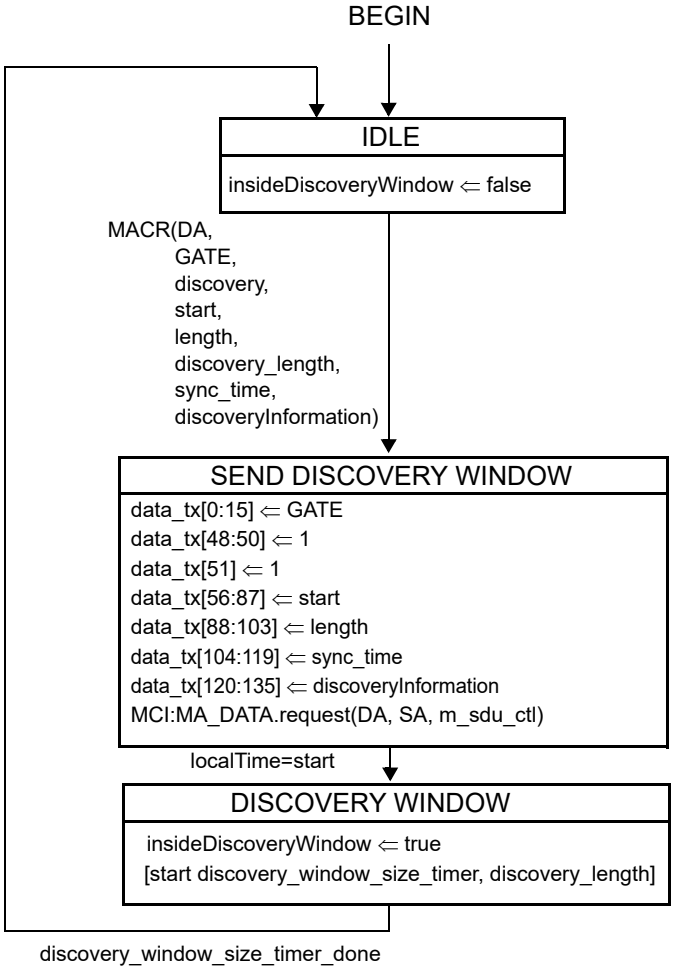

Figure 77–19—Discovery Processing OLT Window Setup state diagram

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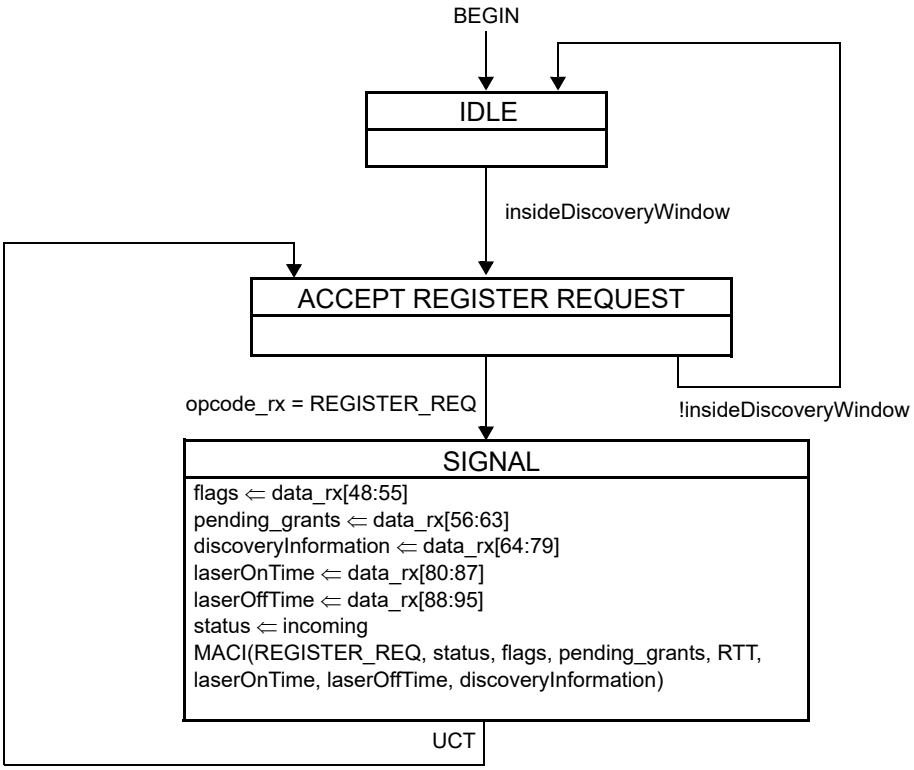
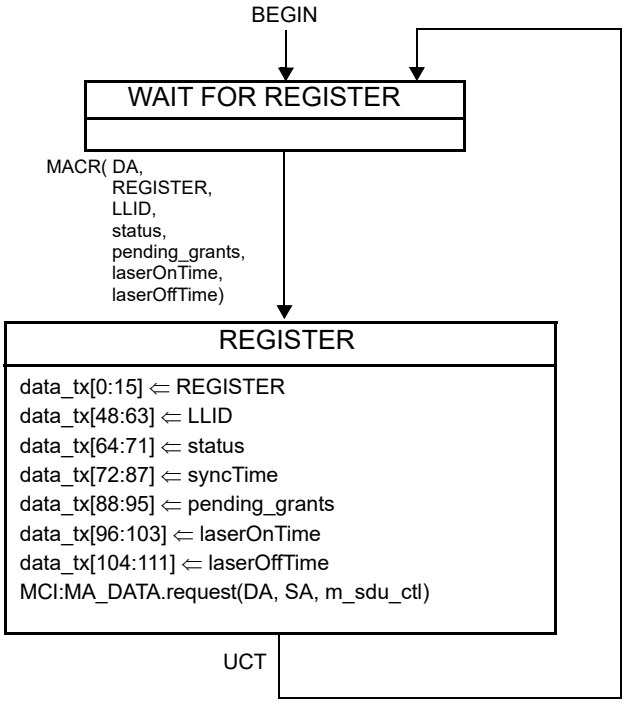


Figure 77–20—Discovery Processing OLT Process Requests state diagram



Instances of MAC data service interface:
MCI=interface to MAC Control multiplexer

Figure 77–21—Discovery Processing OLT Register state diagram

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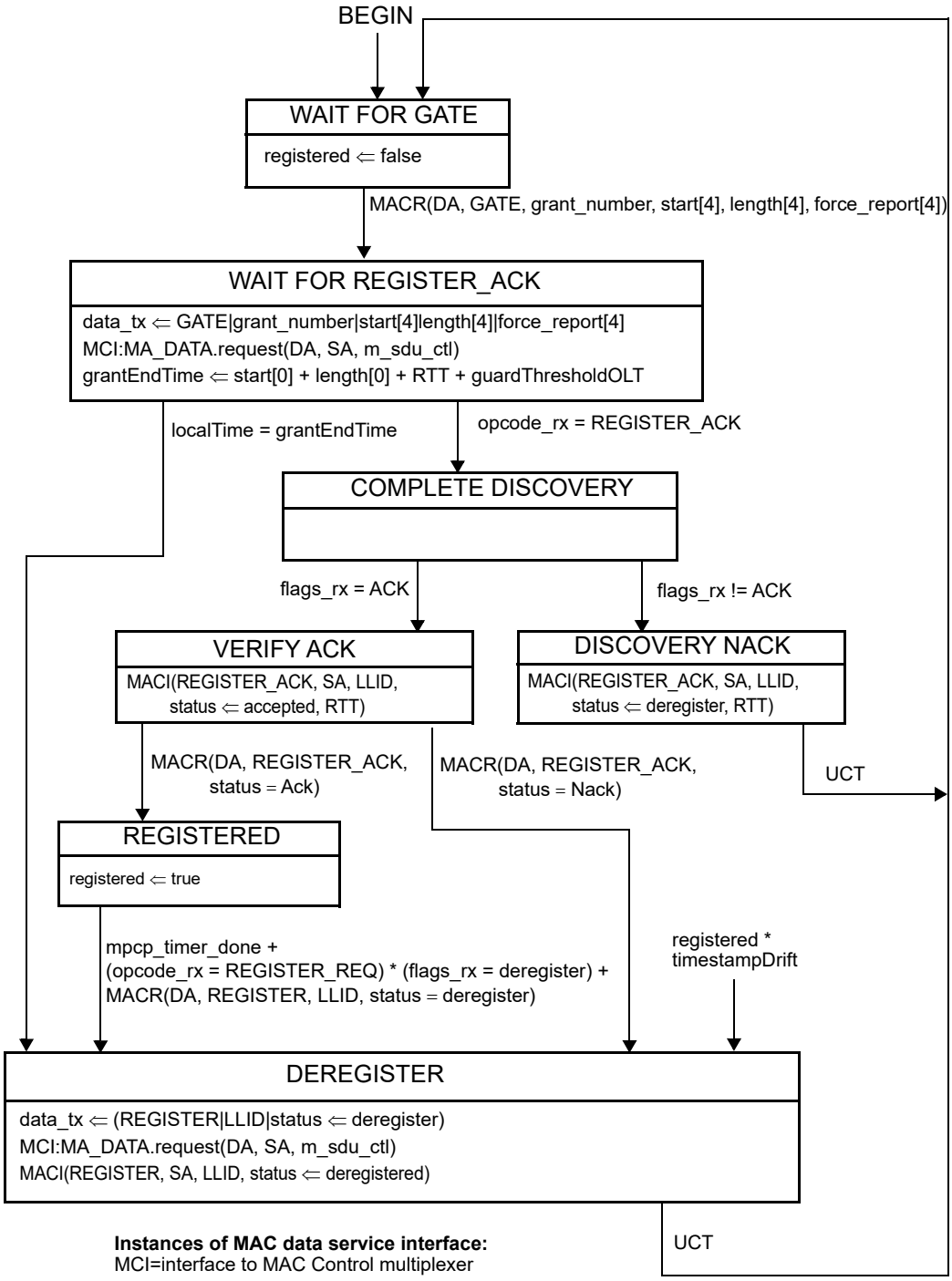

NOTE—The MAC Control Client issues the grant following the REGISTER message, taking the ONU processing delay of REGISTER message into consideration.

Figure 77–22—Discovery Processing OLT Final Registration state diagram

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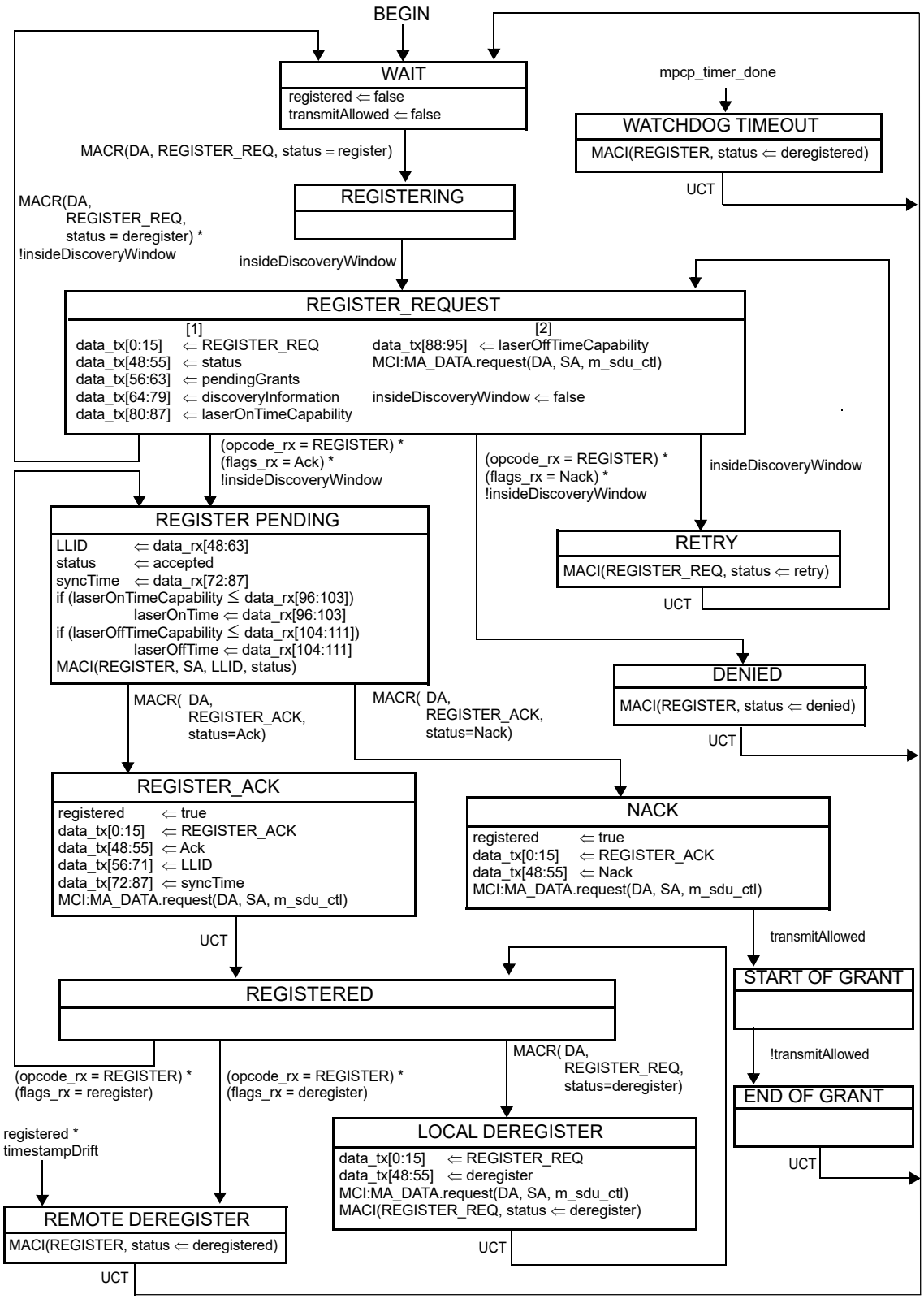

Figure 77–23—Discovery Processing ONU Registration state diagram

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77.3.4 Report Processing

The Report Processing functional block has the responsibility of dealing with queue report generation and termination in the network. Reports are generated by higher layers and passed to the MAC Control sublayer by the MAC Control clients. Status reports are used to signal bandwidth needs as well as for arming the OLT watchdog timer.

Reports shall be generated periodically, even when no request for bandwidth is being made. This keeps a watchdog timer in the OLT from expiring and deregistering the ONU. For proper operation of this mechanism the OLT shall grant the ONU periodically.

The Report Processing functional block, and its MPCP protocol elements are designed for use in conjunction with an IEEE 802.1P capable bridge.

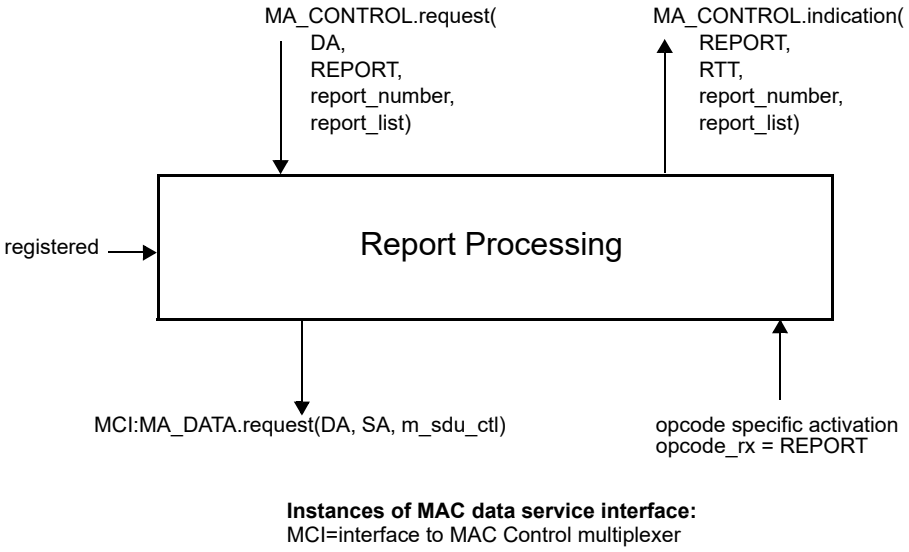

Figure 77–24—Report Processing service interfaces

77.3.4.1 Constants

None.

77.3.4.2 Variables

BEGIN
: TYPE: Boolean
This variable is used when initiating operation of the functional block state diagram. It is set to true following initialization and every reset.

data_rx
: This variable is defined in 77.2.2.3.

data_tx
: This variable is defined in 77.2.2.3.

m_sdu_ctl
: This variable is defined in 77.2.2.3.

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mpcp_timeout
TYPE: 32 bit unsigned
This variable represents the maximum allowed interval of time between two MPCPDU messages. Failure to receive at least one frame within this interval is considered a fatal fault and leads to deregistration. This variable is expressed in units of time_quanta.
VALUE: 0x03B9ACA0 (1 s, default value)

opcode_rx
This variable is defined in 77.2.2.3.

registered
This variable is defined in 77.3.3.2.

report_timeout
TYPE: 32 bit unsigned
This variable represents the maximum allowed interval of time between two REPORT messages generated by the ONU, expressed in units of time_quanta.
VALUE: 0x002FAF08 (50 ms, default value)

77.3.4.3 Functions

None.

77.3.4.4 Timers

report_periodic_timer
ONUs are required to generate REPORT MPCPDUs with a periodicity of less than report_timeout value. This timer counts down time remaining before a forced generation of a REPORT message in an ONU.

mpcp_timer
This timer is defined in 77.3.3.4.

77.3.4.5 Messages

MA_DATA.request (DA, SA, m_sdu)
The service primitive is defined in 2.3.2.

MA_CONTROL.request(DA, REPORT, report_number, report_list)
This service primitive is used by a MAC Control client to request the Report Process at the ONU to transmit a queue status report. This primitive may be called at variable intervals, independently of the granting process, in order to reflect the time varying aspect of the network. This primitive uses the following parameters:

DA:	Multicast MAC Control address as defined in Annex 31B.
REPORT:	Opcode for REPORT MPCPDU as defined in Table 31A–1.
report_number:	The number of queue status report sets located in report list. The report_number value ranges from 0 to a maximum of 13.
report_list:	The list of queue status reports. A queue status report consists of two fields: valid and status. The parameter valid is a Boolean array of length of 8. The index of an element of this array reflects the numbered priority queue in the IEEE 802.1P nomenclature. An element with the value of '0' or false indicates that the corresponding status field is not present (the

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length of status field is 0),while '1' or true indicates that the corresponding status field is present (the length of status field is 2 octets). The parameter status is an array of 16 bit unsigned integer values. This array consists only of entries whose corresponding bit in field valid is set to true.

MA_CONTROL.indication(REPORT, RTT, report_number, report_list)

The service primitive is issued by the Report Process at the OLT to notify the MAC Control client and higher layers the queue status of the MPCP link partner. This primitive may be called multiple times, in order to reflect the time–varying aspect of the network. This primitive uses the following parameters:

REPORT: Opcode for REPORT MPCPDU as defined in Table 31A–1.

RTT: This parameter holds an updated round trip time value that is recalculated following each REPORT message reception.

report_number: The number of queue status report sets located in report list. The report_number value ranges from 0 to a maximum of 13.

report_list: The list of queue status reports. A queue status report consists of two fields: valid and status. The parameter valid is a Boolean array of length of 8. The index of an element of this array reflects the numbered priority queue in the IEEE 802.1P nomenclature. An element with the value of '0' or false indicates that the corresponding status field is not present (the length of status field is 0),while '1' or true indicates that the corresponding status field is present (the length of status field is 2 octets). The parameter status is an array of 16 bit unsigned integer values. This array consists only of entries whose corresponding bit in field valid is set to true.

Opcode-specific function(opcode)

Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

77.3.4.6 State diagrams

The report process in the OLT shall implement the report processing state diagram as shown in Figure 77–25. The report process in the ONU shall implement the report processing state diagram as shown in Figure 77–26. Instantiation of state diagrams as described is performed for Multipoint MAC Control instances attached to unicast LLIDs only.

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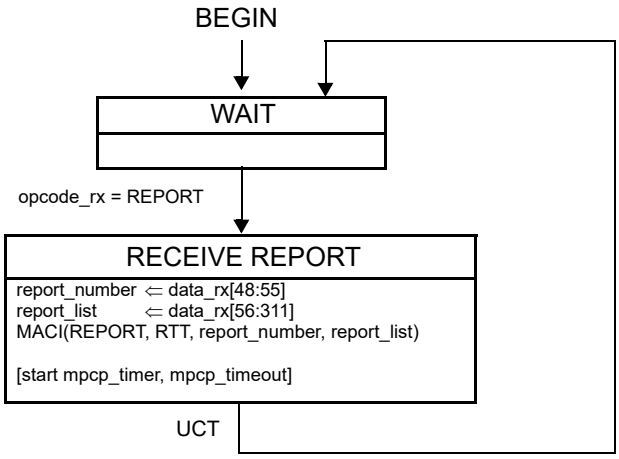
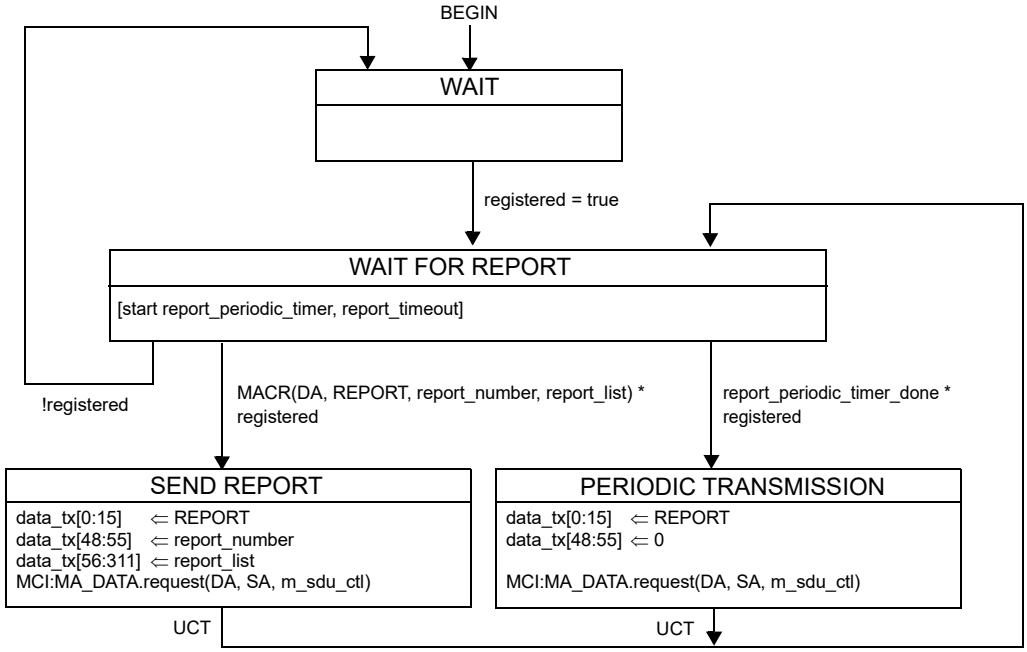


Figure 77–25—Report Processing state diagram at OLT



Instances of MAC data service interface:
MCI=interface to MAC Control multiplexer

Figure 77–26—Report Processing state diagram at ONU

77.3.5 Gate Processing

A key concept pervasive in Multipoint MAC Control is the ability to arbitrate a single transmitter out of a plurality of ONUs. The OLT controls an ONU's transmission by the assigning of grants.

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The transmitting window of an ONU is indicated in the GATE message where start time and length are specified. An ONU begins transmission when its localTime counter matches the start_time value indicated in the GATE message. An ONU concludes its transmission with sufficient margin to ensure that the laser is turned off before the grant length interval has elapsed.

Multiple outstanding grants may be issued to each ONU. The OLT shall not issue more than the maximum supported maximum outstanding grants as advertised by the ONU during registration (see pending grants in 77.3.6.3).

In order to maintain the watchdog timer at the ONU, grants are periodically generated. For this purpose empty GATE messages may be issued periodically.

When registered, the ONU ignores all gate messages where the Discovery flag is set.

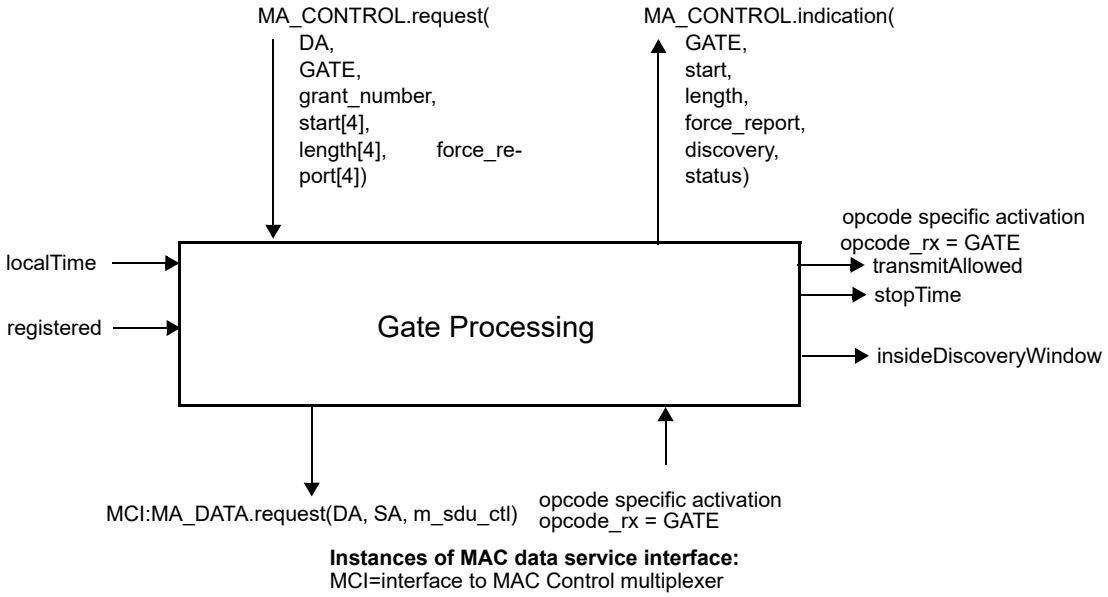

Figure 77–27—Gate Processing service interface

77.3.5.1 Constants

max_future_grant_time
: TYPE: 32 bit unsigned
This constant holds the time limiting the future time horizon for a valid incoming grant.
VALUE: 0x03B9ACA0 (1 s)

min_processing_time
: TYPE: 32 bit unsigned
This constant is the time required for the ONU processing time.
VALUE: 0x00000400 (16.384 μs)

minGrantLength
: TYPE: 32 bit unsigned
This constant represents the minimum data portion of a grant. The minGrantLength is equal to one FEC codeword (see FEC_CODEWORD_SIZE in 77.2.2.1), less the initial 16 idle octets, expressed

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in units of time_quanta. The minimum grant length accepted by an ONU is equal to minGrantLength + BurstOverhead (see 77.3.5.2).
VALUE: 12

tqSize
This constant is defined in 77.2.2.1.

77.3.5.2 Variables

BEGIN
TYPE: Boolean
This variable is used when initiating operation of the functional block state diagram. It is set to true following initialization and every reset.

BurstOverhead
TYPE: integer
This variable represents the burst overhead and equals the sum of laserOnTime, laserOffTime, syncTime and an additional two time_quanta to account for END_BURST_DELIMITER and two leading IDLE vectors of the payload. This variable is expressed in units of time_quanta.

counter
TYPE: integer
This variable is used as a loop iterator counting the number of incoming grants in a GATE message.

currentGrant
TYPE:

```
structure
{
    DA:           48 bit unsigned, a.k.a MAC address type
    start         32 bit unsigned
    length        16 bit unsigned
    force_report  Boolean
    discovery     Boolean
}
```

This variable is used for local storage of a pending grant state during processing. It is dynamically set by the Gate Processing functional block and is not exposed.
The state is a structure field composed of multiple subfields.

data_rx
This variable is defined in 77.2.2.3.

data_tx
This variable is defined in 77.2.2.3.

effectiveLength
TYPE: 32 bit unsigned
This variable is used for temporary storage of a normalized net time value. It holds the net effective length of a grant normalized for elapsed time, and compensated for the periods required to turn the laser on and off, and waiting for receiver lock.

gate_timeout
TYPE: 32 bit unsigned
This variable represents the maximum allowed interval of time between two GATE messages gen-

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erated by the OLT to the same ONU, expressed in units of time_quanta.
VALUE: 0x002FAF08 (50 ms, default value)

grantList
TYPE: list of elements having the structure define in currentGrant
This variable is used for storage of the list of pending grants. It is dynamically set by the Gate Processing functional block and is not exposed. Each time a grant is received it is added to the list. The list elements are structure fields composed of multiple subfields. The list is indexed by the start subfield in each element for quick searches.

grantStart
This variable is defined in 77.2.2.3.

insideDiscoveryWindow
This variable is defined in 77.3.3.2.

maxDelay
TYPE: 16 bit unsigned
This variable holds the maximum delay that can be applied by an ONU before sending the REGISTER_REQ MPCPDU. This delay is calculated such that the ONU would have sufficient time to transmit the REGISTER_REQ message and its associated overhead (FEC parity data, end-of-frame sequence, etc.) and terminate the laser before the end of the discovery grant.

m_sdu_ctl
This variable is defined in 77.2.2.3.

nextGrant
TYPE: element having same structure as defined in currentGrant
This variable is used for local storage of a pending grant state during processing. It is dynamically set by the Gate Processing functional block and is not exposed. The content of the variable is the next grant to become active.

nextStopTime
TYPE: 32 bit unsigned
This variable holds the value of the localTime counter corresponding to the end of the next grant.

opcode_rx
This variable is defined in 77.2.2.3.

registered
This variable is defined in 77.3.3.2.

stopTime
This variable is defined in 77.2.2.3.

syncTime
This variable is defined in 77.3.3.2.

transmitAllowed
This variable is defined in 77.2.2.3.

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77.3.5.3 Functions

empty(list)

This function is use to check whether the list is empty. When there are no elements queued in the list, the function returns true. Otherwise, a value of false is returned.

confirmDiscovery(data)

This function is used to check whether the current Discovery Window is open for the given ONU (TRUE) or not (FALSE). This function returns values as shown in Table 77–1.

Table 77–1—Operation of the confirmDiscovery(data) function

OLT Discovery Information: Discovery Window		ONU Tx capability		confirmDiscovery(data) returns
1G	10G	1G	10G	
X	1	0	1	TRUE
1	X	1	0	TRUE
0	1	1	0	FALSE
1	0	0	1	FALSE
0	0	X	X	FALSE[a]

[a]These particular values for the Discovery Window fields should not be normally generated by the OLT.

InsertInOrder(sorted_list, inserted_element)

This function is used to queue an element inside a sorted list. The queuing order is sorted. In the condition that the list is full the element may be discarded. The length of the list is dynamic and it's maximum size equals the value advertised during registration as maximum number of pending grants.

IsBroadcast(grant)

This function is used to check whether its argument represents a broadcast grant, i.e., grant given to multiple ONUs. This is determined by the destination MAC address of the corresponding GATE message. The function returns the value true when MAC address is a global assigned MAC Control address as defined in Annex 31B, and false otherwise.

PeekHead(sorted_list)

This function is used to check the content of a sorted list. It returns the element at the head of the list without dequeuing the element.

Random(r)

This function is used to compute a random integer number uniformly distributed between 0 and r. The randomly generated number is then returned by the function.

RemoveHead(sorted_list)

This function is used to dequeue an element from the head of a sorted list. The return value of the function is the dequeued element.

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77.3.5.4 Timers

gntWinTmr
: This timer is used to wait for the event signaling the end of a grant window.
VALUE: The timer value is dynamically set according to the signaled grant length.

gate_periodic_timer
: The OLT is required to generate GATE MPCPDUs with a periodicity of less than gate_timeout value. This timer counts down time remaining before a forced generation of a GATE message in the OLT.

mpcp_timer
: This timer is defined in 77.3.3.4.

rndDlyTmr
: This timer is used to measure a random delay inside the discovery window. The purpose of the delay is to a priori reduce the probability of transmission overlap during the registration process, and thus lowering the expectancy of registration time in the PON.
VALUE: A random value less than the net discovery window size less the REGISTER_REQ MPCPDU frame size less the idle period and laser turn on and off delays less the preamble size less the IFG size. The timer value is set dynamically based on the parameters passed from the client.

77.3.5.5 Messages

MA_DATA.request (DA, SA, m_sdu)
: The service primitive is defined in 2.3.2.

MA_CONTROL.request(DA, GATE, grant_number, start[4], length[4], force_report[4])
: This service primitive is defined in 77.3.3.5.

MA_CONTROL.indication(GATE, start, length, force_report, discovery, status)
: This service primitive issued by the Gate Process at the ONU to notify the MAC Control client and higher layers that a grant is pending. This primitive is invoked multiple times when a single GATE message arrives with multiple grants. It is also generated at the start and end of each grant as it becomes active. This primitive uses the following parameters:

GATE:	Opcode for GATE MPCPDU as defined in Table 31A–1.
start:	start time of the grant. This parameter is not present when the parameter *status* value is equal to *deactive*.
length:	Length of the grant. This parameter is not present when the parameter *status* value is equal to *deactive*.
force_report:	Flags indicating whether a REPORT message should be transmitted in this grant. This parameter is not present when the parameter *status* value is equal to *deactive*.
discovery:	This parameter holds the value true when the grant is to be used for the discovery process, and false otherwise. This parameter is not present when the parameter *status* value is equal to *deactive*.
status:	This parameter takes the value *arrive* on grant reception, *active* when a grant becomes active, and *deactive* at the end of a grant.

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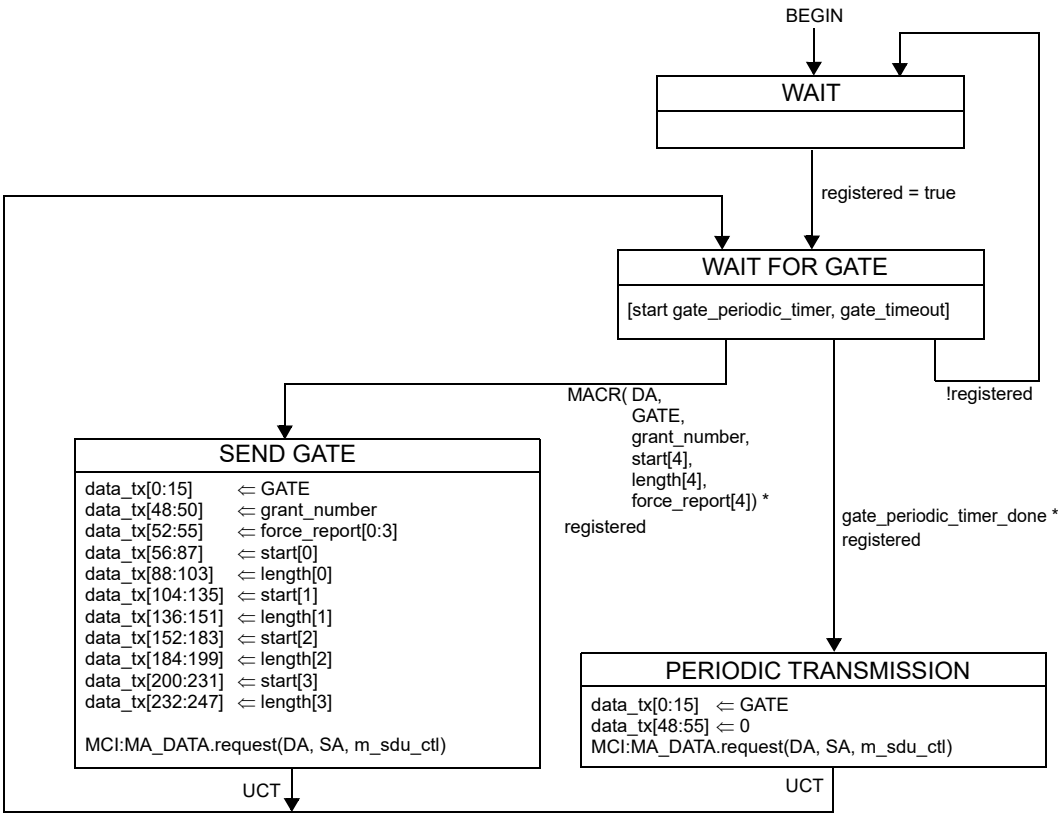
Opcode-specific function(opcode)

Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

77.3.5.6 State diagrams

The gating process in the OLT shall implement the Gate processing state diagram as shown in Figure 77–28. The gating process in the ONU shall implement the Gate processing state diagram as shown in Figure 77–29 and Figure 77–30. Instantiation of state diagrams as described is performed for all Multipoint MAC Control instances.



Instances of MAC data service interface:
MCI=interface to MAC Control multiplexer

Figure 77–28—Gate Processing state diagram at OLT

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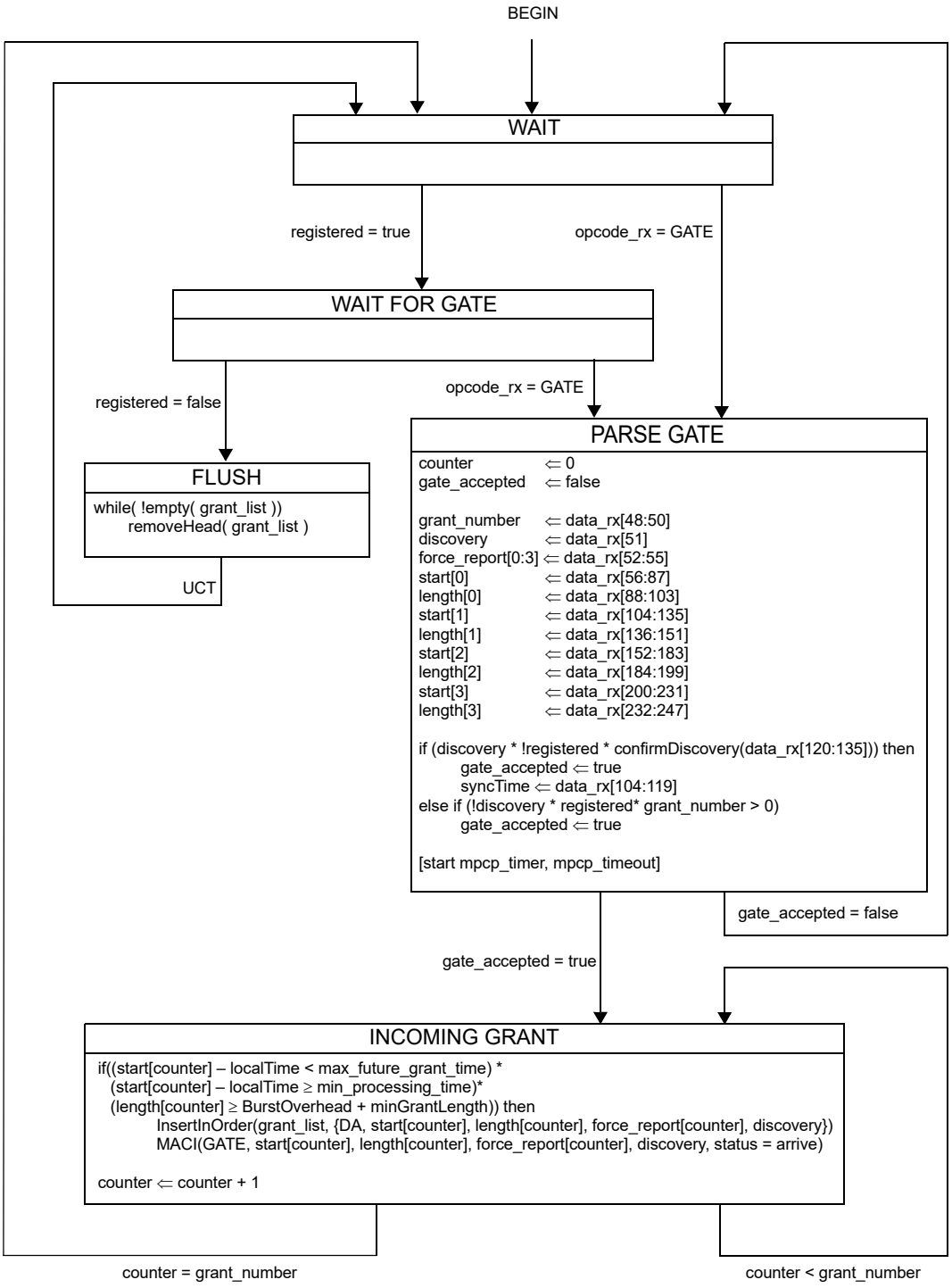

Figure 77–29—Gate Processing ONU Programing state diagram

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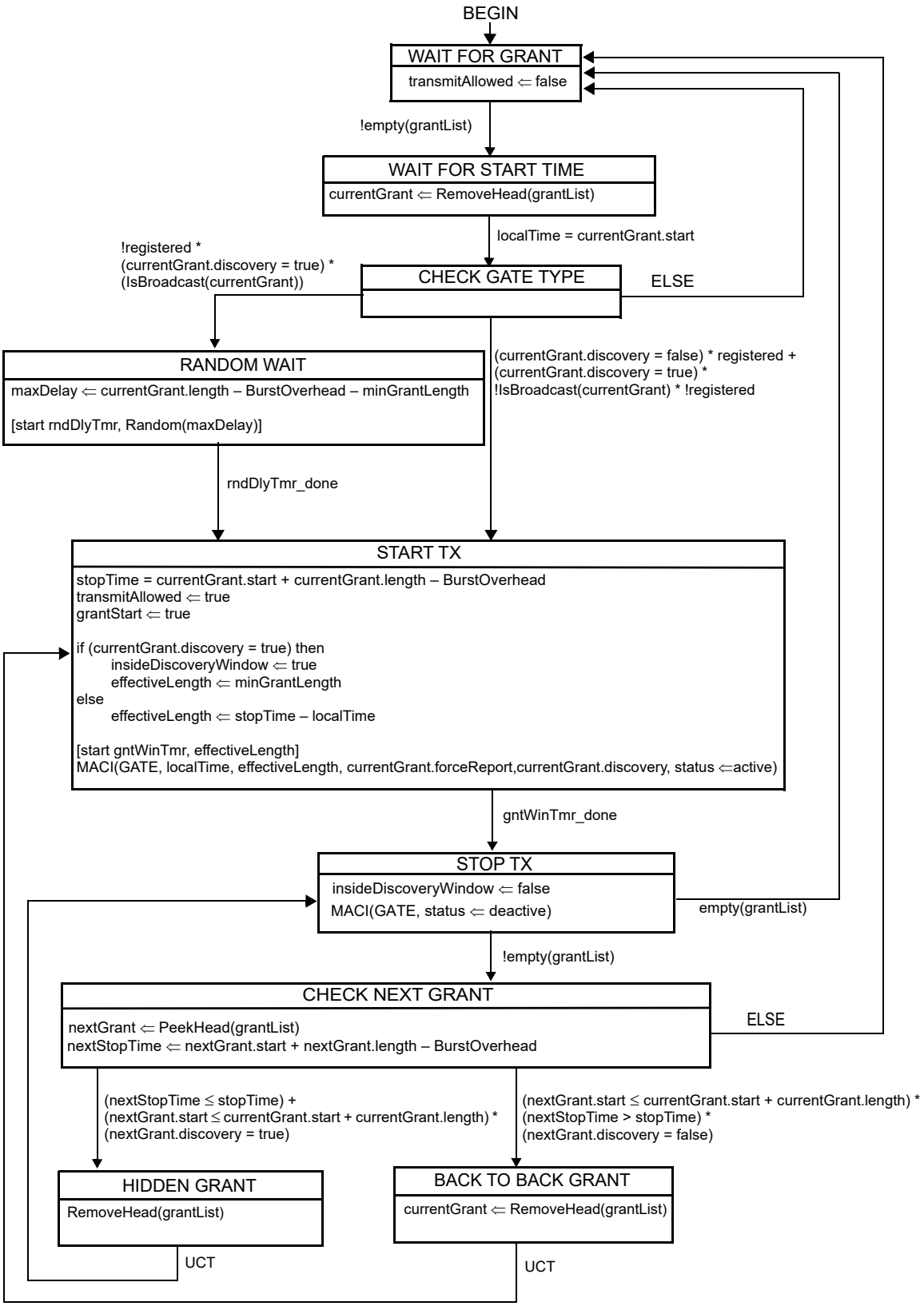

Figure 77–30—Gate Processing ONU Activation state diagram

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77.3.6 MPCPDU structure and encoding

The MPCPDU structure shall be as shown in Figure 77–31, and is further defined in the following definitions:

a) Destination Address (DA). The DA in MPCPDU is the MAC Control Multicast address as specified in the annexes to Clause 31, or the individual MAC address associated with the port to which the MPCPDU is destined.

b) Source Address (SA). The SA in MPCPDU is the individual MAC address associated with the port through which the MPCPDU is transmitted. For MPCPDUs originating at the OLT end, this can be the address any of the individual MACs. These MACs may all share a single unicast address, as explained in 77.1.2.

c) Length/Type. The Length/Type in MPCPDUs carries the MAC_Control_Type field value as specified in 31.4.1.3.

d) Opcode. The opcode identifies the specific MPCPDU being encapsulated. Values are defined in Table 31A–1.

e) Timestamp. The timestamp field conveys the content of the localTime register at the time of transmission of the MPCPDUs. This field is 32 bits long and counts time in units of time_quanta.

f) Data/Reserved/PAD. These 40 octets are used for the payload of the MPCPDUs. When not used they would be filled with zeros on transmission, and be ignored on reception.

g) FCS. This field is the Frame Check Sequence, typically generated by the underlying MAC.
Based on the MAC instance used to generate the specific MPCPDU, the appropriate LLID shall be generated by the RS.

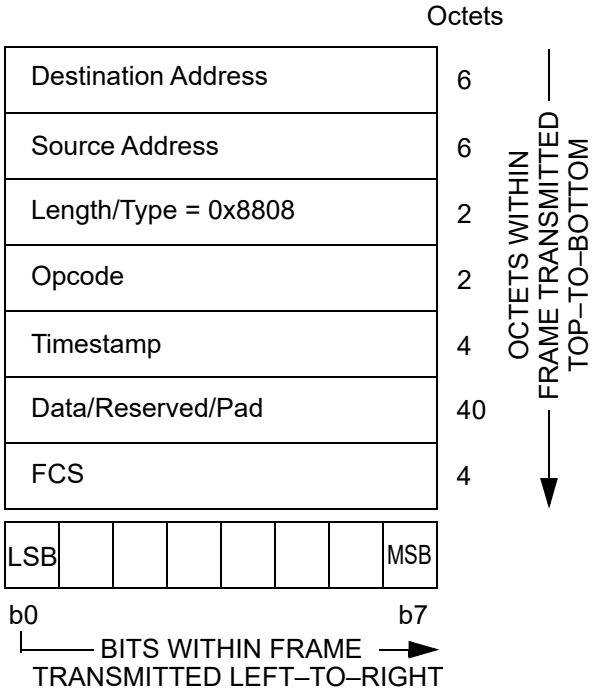

Figure 77–31—Generic MPCPDU

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77.3.6.1 GATE description

The purpose of GATE message is to grant transmission windows to ONUs for both discovery messages and normal transmission. Up to four grants can be included in a single GATE message. The number of grants can also be set to zero for using the GATE message as an MPCP keep alive from OLT to the ONU.

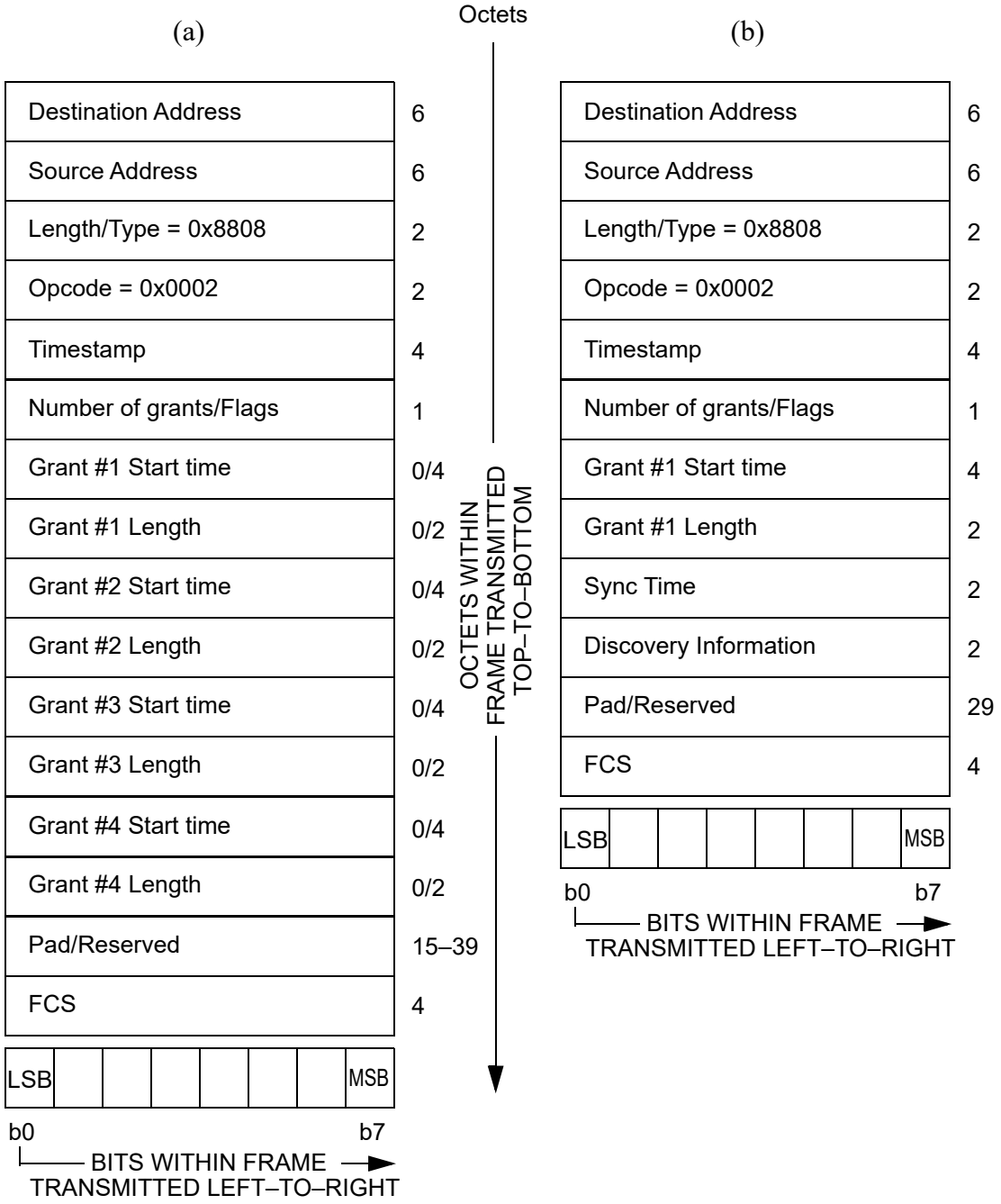

Figure 77–32—GATE MPCPDU: (a) normal GATE MPCPDU, (b) discovery GATE MPCPDU

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The GATE MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) Opcode. The opcode for the GATE MPCPDU is 0x0002.

b) Flags. This is an 8 bit flag register that holds the following flags: As presented in Table 77–2, the Number of grants field contains the number of grants, composed of valid Length, Start Time pairs in this MPCPDU. This is a number between 0 and 4.

NOTE—When Number of grants is set to 0, sole purpose of message is conveying of timestamp to ONU.

The Discovery flag field indicates that the signaled grants would be used for the discovery process, in which case a single grant shall be issued in the GATE message.
The Force Report flag fields ask the ONU to issue a REPORT message related to the corresponding grant number at the corresponding transmission opportunity indicated in this GATE.

Table 77–2—GATE MPCPDU Number of grants/flags fields

Bit	Flag field	Values
0–2	Number of grants	0 – 4
3	Discovery	0 – Normal GATE 1 – Discovery GATE
4	Force Report Grant 1	0 – No action required 1 – A REPORT frame should be issued at the corresponding transmission opportunity indicated in Grant 1
5	Force Report Grant 2	0 – No action required 1 – A REPORT frame should be issued at the corresponding transmission opportunity indicated in Grant 2
6	Force Report Grant3	0 – No action required 1 – A REPORT frame should be issued at the corresponding transmission opportunity indicated in Grant 3
7	Force Report Grant 4	0 – No action required 1 – A REPORT frame should be issued at the corresponding transmission opportunity indicated in Grant 4

c) Grant #n Start Time. This 32 bit unsigned field represents the start time of the grant. The start time is compared to the local clock, to correlate the start of the grant. Transmitted values shall satisfy the condition Grant #n Start Time < Grant #n+1 Start Time for consecutive grants within the same GATE MPCPDU.

d) Grant #n Length. This 16 bit unsigned field represents the length of the grant. The length is counted in 1 time_quantum increments. There are 4 Grants that are possibly packed into the GATE MPCPDU. The laserOnTime, syncTime, laserOffTime, two initial Idle blocks, FEC parity overhead, and burst terminator sequence (composed of three END_BURST_DELIMITER blocks) are included in and thus consume part of the Grant #n length.

e) Sync Time. This is an unsigned 16 bit value signifying the required synchronization time of the OLT receiver. The ONU calculates the effective grant length by subtracting the syncTime, laserOnTime, laserOffTime and END_BURST_DELIMITER from the grant length it received from the OLT. The value is counted in 1 time_quantum increments. The advertised value includes synchronization requirement on all receiver elements including PMD, PMA and PCS. This field is present only when the GATE is a discovery GATE, as signaled by the Discovery flag and is not present otherwise.

f) Discovery Information. This is a 16 bit flag register. This field is present only when the GATE is a discovery GATE, as signaled by the Discovery flag and is not present otherwise. Table 77–3 presents the internal structure of the Discovery Information flag field.

g) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored on reception. The size of this field depends on the used Grant #n Length/Start Time entry-pairs as well as the presence of the Sync Time and Discovery Information fields, and varies in length from 15–39 accordingly.

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The GATE MPCPDU shall be generated by a MAC Control instance mapped to an active ONU, and as such shall be marked with a unicast type of LLID, except when the MPCPDU is a discovery GATE, as indicated by the Discovery flag being set to true. For the discovery procedure, a MAC Control instance is mapped to all ONUs, and therefore, the discovery GATE MPCPDU is marked with the appropriate broadcast LLID (see 77.3.2.3).

Table 77–3—GATE MPCPDU discovery information fields

Bit	Flag field	Values
0	OLT is 1G upstream capable	0 – OLT does not support 1 Gb/s reception 1 – OLT supports 1 Gb/s reception
1	OLT is 10G upstream capable	0 – OLT does not support 10 Gb/s reception 1 – OLT supports 10 Gb/s reception
2–3	Reserved	Ignored on reception
4	OLT is opening 1G discovery window	0 – OLT cannot receive 1 Gb/s data in this window 1 – OLT can receive 1 Gb/s data in this window
5	OLT is opening 10G discovery window	0 – OLT cannot receive 10 Gb/s data in this window 1 – OLT can receive 10 Gb/s data in this window
6–15	Reserved	Ignored on reception

77.3.6.2 REPORT description

REPORT messages have several functionalities. Time stamp in each REPORT message is used for round trip (RTT) calculation. In the REPORT messages ONUs indicate the upstream bandwidth needs they request per IEEE 802.1Q priority queue. REPORT messages are also used as keep–alives from ONU to OLT. ONUs issue REPORT messages periodically in order to maintain link health at the OLT as defined in 77.3.4. In addition, the OLT may specifically request a REPORT message.

The REPORT MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) Opcode. The opcode for the REPORT MPCPDU is 0x0003.
b) Number of Queue Sets. This field specifies the number of requests in the REPORT message. A REPORT frame may hold multiple sets of Report bitmap and Queue #n as specified in the Number of Queue Sets field.
c) Report bitmap. This is an 8 bit flag register that indicates which queues are represented in this REPORT MPCPDU—see Table 77–4.

Table 77–4—REPORT MPCPDU Report bitmap fields

Bit	Flag field	Values
0	Queue 0	0 – queue 0 report is not present; 1 – queue 0 report is present
1	Queue 1	0 – queue 1 report is not present; 1 – queue 1 report is present
2	Queue 2	0 – queue 2 report is not present; 1 – queue 2 report is present
3	Queue 3	0 – queue 3 report is not present; 1 – queue 3 report is present
4	Queue 4	0 – queue 4 report is not present; 1 – queue 4 report is present
5	Queue 5	0 – queue 5 report is not present; 1 – queue 5 report is present

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Table 77–4—REPORT MPCPDU Report bitmap fields *(continued)*

Bit	Flag field	Values
6	Queue 6	0 – queue 6 report is not present; 1 – queue 6 report is present
7	Queue 7	0 – queue 7 report is not present; 1 – queue 7 report is present

d) Queue #n Report. This value represents the length of queue #n at time of REPORT message generation. The reported length shall be adjusted and rounded up to the nearest time_quantum to account for the necessary inter–frame spacing and preamble. FEC parity overhead is not included in the reported length. The Queue #n Report field is an unsigned 16 bit integer representing the transmission request in units of time_quanta. This field is present only when the corresponding flag in the Report bitmap is set.

e) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored on reception. The size of this field depends on the used Queue Report entries, and accordingly varies in length from 0 to 39.

The REPORT MPCPDU shall be generated by a MAC Control instance mapped to an active ONU, and as such shall be marked with a unicast type of LLID.

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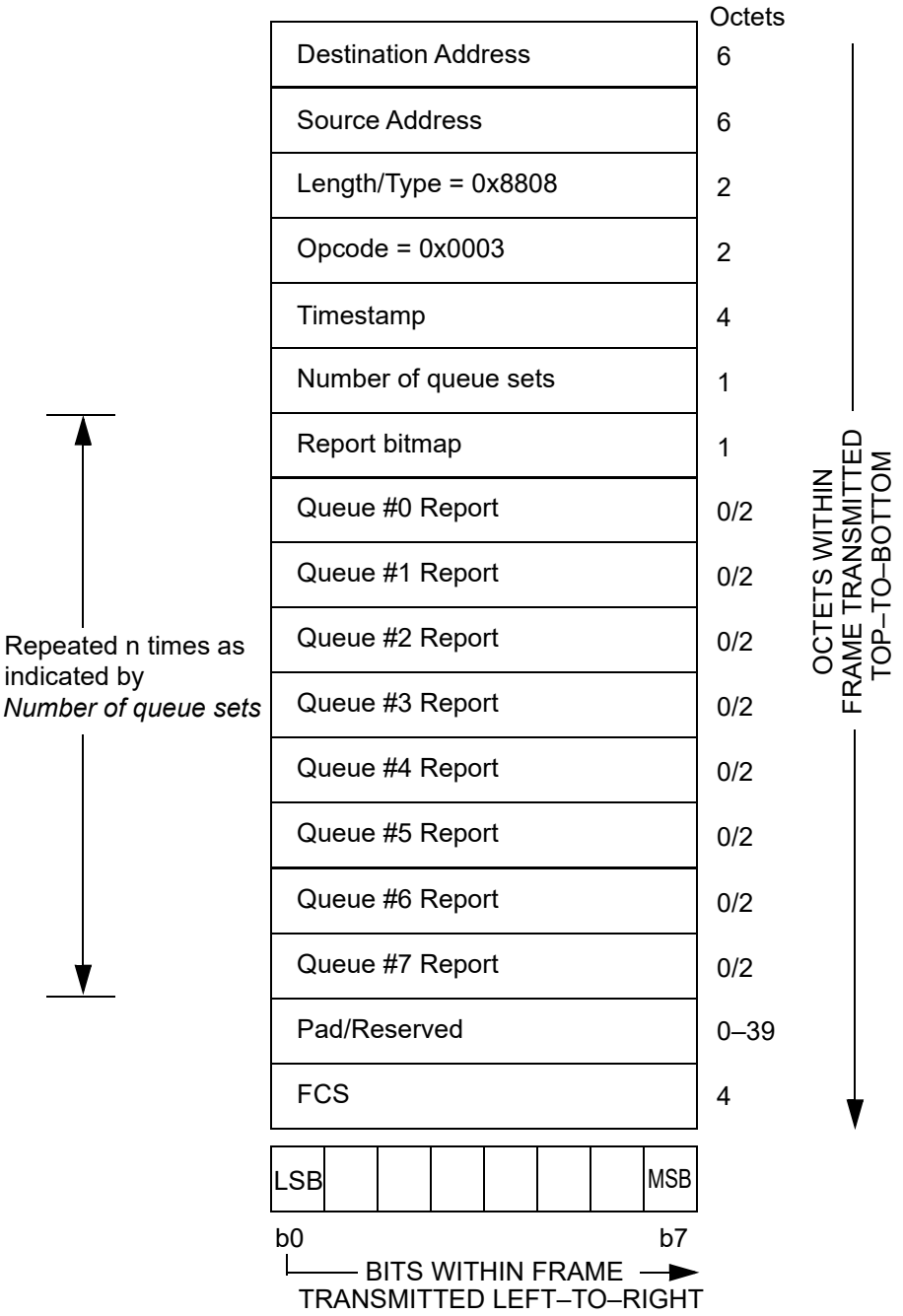

Figure 77–33—REPORT MPCPDU

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77.3.6.3 REGISTER_REQ description

The REGISTER_REQ MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) Opcode. The opcode for the REGISTER_REQ MPCPDU is 0x0004.
b) Flags. This is an 8 bit flag register that indicates special requirements for the registration, as presented in Table 77–5.

Table 77–5—REGISTER_REQ MPCPDU Flags fields

Value	Indication	Comment
0	Reserved	Ignored on reception.
1	Register	Registration attempt for ONU.
2	Reserved	Ignored on reception.
3	Deregister	This is a request to deregister the ONU. Subsequently, the MAC is deallocated and the LLID may be reused.
4–255	Reserved	Ignored on reception.

c) Pending grants. This is an unsigned 8 bit value signifying the maximum number of future grants the ONU is configured to buffer. The OLT should not grant the ONU more than this maximum number of Pending grants vectors composed of {start, length, force_report, discovery} into the future.
d) Discovery Information. This is a 16 bit flag register. Table 77–6 presents the structure of the Discovery Information flag.

Table 77–6—REGISTER_REQ MPCPDU Discovery Information Fields

Bit	Flag field	Values
0	ONU is 1G upstream capable	0 – ONU transmitter is not capable of 1 Gb/s 1 – ONU transmitter is capable of 1 Gb/s
1	ONU is 10G upstream capable	0 – ONU transmitter is not capable of 10 Gb/s 1 – ONU transmitter is capable of 10 Gb/s
2–3	Reserved	Ignored on reception
4	1G registration attempt	0 – 1 Gb/s registration is not attempted 1 – 1 Gb/s registration is attempted
5	10G registration attempt	0 – 10 Gb/s registration is not attempted 1 – 10 Gb/s registration is attempted
6–15	Reserved	Ignored on reception

e) Laser On Time. This field is 1 octet long and carries the Laser On Time characteristic for the given ONU transmitter. The value is expressed in the units of time_quanta.
f) Laser Off Time. This field is 1 octet long and carries the Laser Off Time characteristic for the given ONU transmitter. The value is expressed in the units of time_quanta.
g) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored on reception.

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The REGISTER_REQ MPCPDU shall be generated by a MAC Control instance mapped to an undiscovered ONU, and as such shall be marked with a broadcast type of LLID (77.3.2.3).

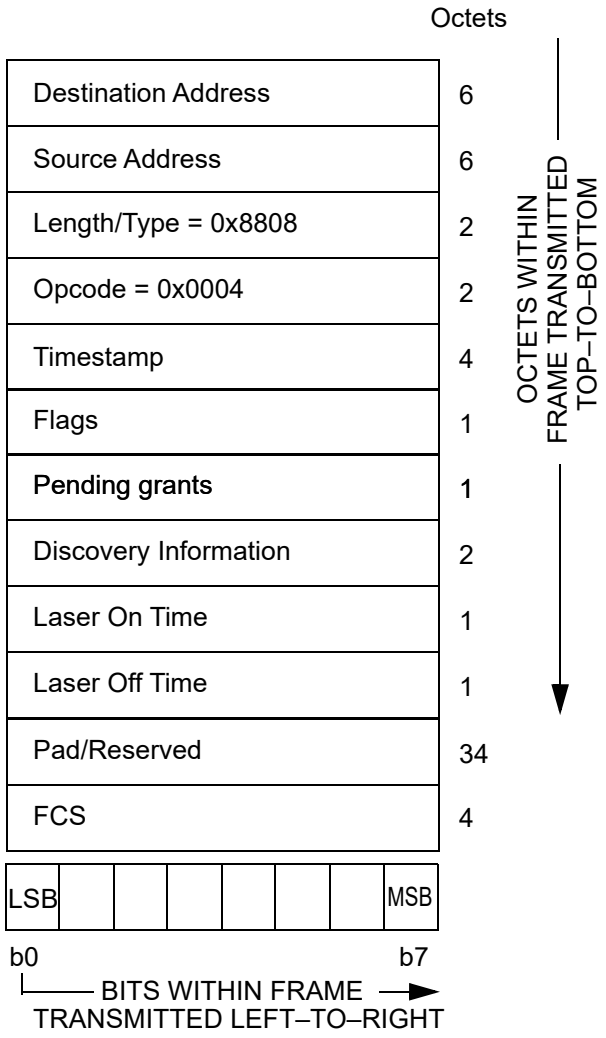

Figure 77–34—REGISTER_REQ MPCPDU

77.3.6.4 REGISTER description

The REGISTER MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) DA. The destination address used shall be an individual MAC address.
b) Opcode. The opcode for the REGISTER MPCPDU is 0x0005.
c) Assigned Port. This field holds a 16 bit unsigned value reflecting the LLID of the port assigned following registration.
d) Flags. this is an 8 bit flag register that indicates special requirements for the registration, as presented in Table 77–7.
e) Sync Time. This is an unsigned 16 bit value signifying the required synchronization time of the OLT receiver. The ONU calculates the effective grant length by subtracting the syncTime, laserOnTime, laserOffTime, and END_BURST_DELIMITER from the grant length it received from the OLT. The value is counted in 1 time_quantum increments. The advertised value includes synchronization requirement on all receiver elements including PMD, PMA, and PCS.

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Table 77–7—REGISTER MPCPDU Flags field

Value	Indication	Comment
0	Reserved	Ignored on reception.
1	Reregister	The ONU is explicitly asked to re-register.
2	Deregister	This is a request to deallocate the port and free the LLID. Subsequently, the MAC is deallocated.
3	Ack	The requested registration is successful.
4	Nack	The requested registration attempt is denied by the MAC Control Client.
5–255	Reserved	Ignored on reception.

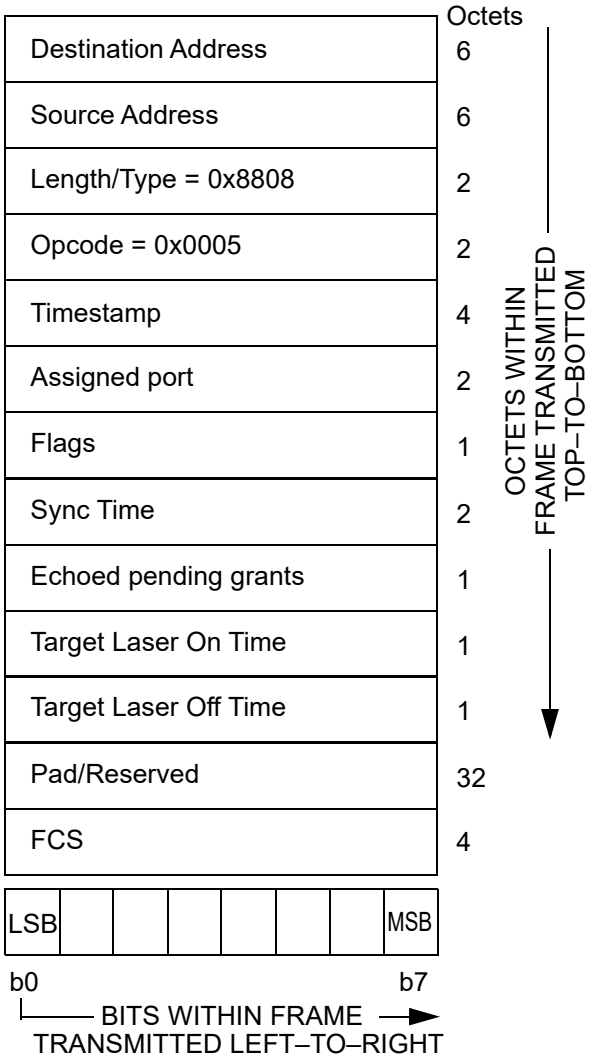

Figure 77–35—REGISTER MPCPDU

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f) Echoed pending grants. This is an unsigned 8 bit value signifying the number of future grants the ONU may buffer before activating. The OLT should not grant the ONU more than this number of grants into the future.
g) Target Laser On Time. This is an unsigned 8 bit value, expressed in the units of time_quanta, signifying the Laser On Time for the given ONU transmitter. This value may be different from Laser On Time delivered by the ONU in the REGISTER_REQ MPCPDU during the Discovery process. The ONU updates the local laserOnTime variable per state diagram in Figure 77–23.
h) Target Laser Off Time. This is an unsigned 8 bit value, expressed in the units of time_quanta, signifying the Laser Off Time for the given ONU transmitter. This value may be different from Laser Off Time delivered by the ONU in the REGISTER_REQ MPCPDU during the Discovery process. The ONU updates the local laserOffTime variable per state diagram in Figure 77–23.
i) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored on reception.

The REGISTER MPCPDU shall be generated by a MAC Control instance mapped to all ONUs and such frame is marked by the broadcast LLID (77.3.2.3).

77.3.6.5 REGISTER_ACK description

The REGISTER_ACK MPCPDU is an instantiation of the Generic MPCPDU, and is further defined using the following definitions:

a) Opcode. The opcode for the REGISTER_ACK MPCPDU is 0x0006.
b) Flags. This is an 8 bit flag register that indicates special requirements for the registration, as presented in Table 77–8.
c) Echoed assigned port. This field holds a 16 bit unsigned value reflecting the LLID for the port assigned following registration.
d) Echoed Sync Time. This is an unsigned 16 bit value echoing the required synchronization time of the OLT receiver as previously advertised (77.3.6.4).
e) Pad/Reserved. This is an empty field that is transmitted as zeros, and ignored at reception.

Table 77–8—REGISTER_ACK MPCPDU Flags fields

Value	Indication	Comment
0	Nack	The requested registration attempt is denied by the MAC Control Client.
1	Ack	The registration process is successfully acknowledged.
2–255	Reserved	Ignored on reception.

The REGISTER_ACK MPCPDU shall be generated by a MAC Control instance mapped to an active ONU, and as such shall be marked with a unicast type of LLID.

77.4 Discovery Process in dual-rate systems

The enhancements introduced to the Clause 77 discovery process for EPONs facilitate the coexistence of 10G–EPON with 1G–EPON.

77.4.1 OLT speed-specific discovery

The discovery GATE MPCPDU is defined in Clause 64 for 1 Gb/s operation and in Clause 77 for 10 Gb/s operation. An additional field (Discovery Information field) was added to the 10 Gb/s discovery GATE MPCPDU. This field allows the OLT to relay speed-specific information regarding the discovery window to the different ONUs that may coexist in the same PON. The OLT has the ability to transmit common discovery GATE MPCPDUs on both the 1 Gb/s transmit path and 10 Gb/s transmit path, or it can send

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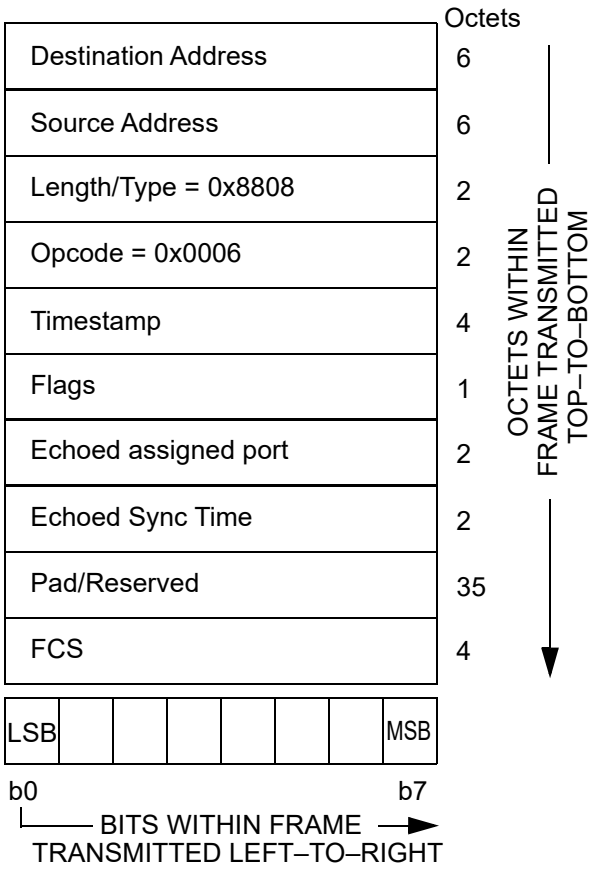

Figure 77–36—REGISTER_ACK MPCPDU

completely separate and independent GATE messages on these different paths. For each discovery window, the OLT is capable of opening windows for individual speeds or multiple speeds.

These different combinations allow the OLT MAC Control Client to open a number of discovery windows for all of the different ONU types. Table 77–9 shows the different types of windows that are possible, along with the necessary LLID and discovery information that also needs to be present in the discovery GATE MPCPDUs. For some combinations, it may be desirable for the OLT MAC Control Client to open overlapping discovery windows. It may do so by sending one discovery GATE MPCPDU on the 1 Gb/s downstream channel and a similar discovery GATE MPCPDU on the 10 Gb/s downstream channel; both discovery GATE MPCPDUs having the same Start Time value.

Figure 77–37 shows the three primary combinations of discovery windows and the different types of REGISTER_REQ MPCPDUs that may be received during the window. Figure 77–37(a) shows reception of messages from 1 Gb/s and 10/1 Gb/s ONUs. Figure 77–37(b) shows reception of messages from 10 Gb/s ONUs. Figure 77–37(c) shows reception of messages from all types of ONUs.

77.4.2 ONU speed-specific registration

A 1G–EPON ONU receives only discovery GATE messages transmitted by the OLT in the 1 Gb/s broadcast channel. Operation and registration of these ONUs is specified in Clause 64.

A 10/1G–EPON ONU is only capable of receiving discovery GATE MPCPDU transmitted by the OLT in the 10 Gb/s broadcast channel. These messages are parsed, and if a 1 Gb/s discovery window is opened, the ONU may attempt to register in the EPON.

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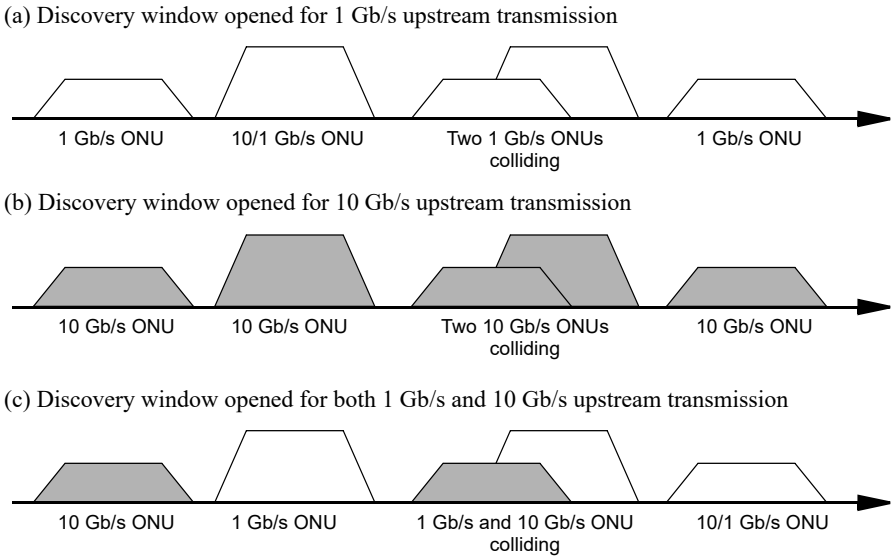

Figure 77–37—Combinations of REGISTER_REQ MPCPDUs during discovery window for 10G–EPON and 1G–EPON coexisting in the same PON

Table 77–9—Discovery GATE MPCPDUs for all ONU types

ONU types targeted by discovery GATE MPCPDU	LLID of discovery GATE(s)	Discovery information			
		Upstream capable		Discovery window	
		1G	10G	1G	10G
1G–EPON	0x7FFF	No Discovery Information field present			
10/1G–EPON	0x7FFE	1	0	1	0
1G–EPON and 10/1G–EPON	0x7FFF[a]	No Discovery Information field present			
	0x7FFE[a]	1	0	1	0
10/10G–EPON	0x7FFE	0	1	0	1
10/1G–EPON and 10/10G–EPON	0x7FFE	1	1	1	1
1G–EPON, 10/1G–EPON, and 10/10G–EPON	0x7FFF[a]	No Discovery Information field present			
	0x7FFE[a]	1	1	1	1

[a]Two discovery GATE MPCPDUs are transmitted in two separate downstream broadcast channels: one with the LLID of 0x7FFF transmitted in the 1 Gb/s downstream broadcast channel and another one the LLID of 0x7FFE transmitted in the 10 Gb/s downstream broadcast channel.

A 10/10G–EPON ONU is only capable of receiving discovery GATE MPCPDU transmitted by the OLT in the 10 Gb/s broadcast channel. These messages are parsed, and if a 10 Gb/s discovery window is opened, the ONU may attempt to register in the EPON.

A dual speed ONU capable of 10/1G–EPON operation or 10/10G–EPON operation is also only capable of receiving discovery GATE MPCPDU transmitted by the OLT in the 10 Gb/s broadcast channel. These messages need to be parsed, and the ONU makes the registration decision based on the available information. The ONU should attempt to register during the discovery window announced as supporting the

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highest speed common to both the OLT and ONU. Table 77–10 shows the action the ONU should take based on the ONU transmit capabilities and the received discovery information.

Table 77–10—ONU action during discovery window

OLT Discovery information				ONU Tx capability		ONU action
Upstream capable		Discovery window				
1G	10G	1G	10G	1G	10G	
1	0	1	0	1	X	Attempt 1G registration
1	X	1	X	1	0	Attempt 1G registration
X	1	X	1	X	1	Attempt 10G registration
1	1	0	1	1	0	Wait for 1G discovery window
1	1	1	0	X	1	Wait for 10G discovery window

The ONU generates the REGISTER_REQ MPCPDU with the same LLID as the discovery GATE MPCPDU it responds to, i.e., 1G–EPON ONU (per Clause 64) use LLID 0x7FFF, while the 10G–EPON ONUs use LLID 0x7FFE.

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77.5 Protocol implementation conformance statement (PICS) proforma for Clause 77, Multipoint MAC Control[140]

77.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 77 Multipoint MAC Control, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

77.5.2 Identification

77.5.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

77.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 77, Multipoint MAC Control
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[140]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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77.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*OLT	OLT functionality	77.1	Device supports functionality required for OLT	O/1	Yes [ ] No [ ]
*ONU	ONU functionality	77.1	Device supports functionality required for ONU	O/1	Yes [ ] No [ ]

77.5.4 PICS proforma tables for Multipoint MAC Control

77.5.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Delay through MAC	77.3.2.4	Maximum delay variation of 1 time_quantum	M	Yes [ ]
CC2	OLT grant time delays	77.3.2.4	Not grant nearer than 1024 time_quanta into the future	OLT:M	Yes [ ]
CC3	ONU processing delays	77.3.2.4	Process all messages in less than 1024 time_quanta	ONU:M	Yes [ ]
CC4	OLT grant issuance	77.3.2.4	Not grant more than one message every 1024 time_quanta to a single ONU	OLT:M	Yes [ ]

77.5.4.2 Multipoint MAC Control

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	OLT localTime	77.2.2.2	Track transmit clock	OLT:M	Yes [ ]
OM2	ONU localTime	77.2.2.2	Track receive clock	ONU:M	Yes [ ]
OM3	Random wait for transmitting REGISTER_REQ messages	77.3.3	Shorter than length of discovery window	ONU:M	Yes [ ]
OM4	Periodic report generation	77.3.4	Reports are generated periodically	ONU:M	Yes [ ]
OM5	Periodic granting	77.3.4	Grants are issued periodically	OLT:M	Yes [ ]
OM6	Issuing of grants	77.3.5	Not issue more than maximum supported grants	OLT:M	Yes [ ]

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77.5.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Multipoint Transmission Control	77.2.2.7	Meets the requirements of Figure 77–10	M	Yes [ ]
SM2	OLT Control Parser	77.2.2.7	Meets the requirements of Figure 77–11	M	Yes [ ]
SM3	ONU Control Parser	77.2.2.7	Meets the requirements of Figure 77–12	M	Yes [ ]
SM4	OLT Control Multiplexer	77.2.2.7	Meets the requirements of Figure 77–13	OLT:M	Yes [ ]
SM5	ONU Control Multiplexer	77.2.2.7	Meets the requirements of Figure 77–14	OLT:M	Yes [ ]
SM6	Discovery Processing OLT Window Setup	77.3.3.6	Meets the requirements of Figure 77–19	OLT:M	Yes [ ]
SM7	Discovery Processing OLT Process Requests	77.3.3.6	Meets the requirements of Figure 77–20	OLT:M	Yes [ ]
SM8	Discovery Processing OLT Register	77.3.3.6	Meets the requirements of Figure 77–21	ONU:M	Yes [ ]
SM9	Discovery Processing OLT Final Registration	77.3.3.6	Meets the requirements of Figure 77–22	OLT:M	Yes [ ]
SM10	Discovery Processing ONU Registration	77.3.3.6	Meets the requirements of Figure 77–23	ONU:M	Yes [ ]
SM11	Report Processing at OLT	77.3.4.6	Meets the requirements of Figure 77–25	OLT:M	Yes [ ]
SM12	Report Processing at ONU	77.3.4.6	Meets the requirements of Figure 77–26	ONU:M	Yes [ ]
SM13	Gate Processing at OLT	77.3.5.6	Meets the requirements of Figure 77–28	OLT:M	Yes [ ]
SM14	Gate Processing at ONU	77.3.5.6	Meets the requirements of Figure 77–29	ONU:M	Yes [ ]
SM15	Gate Processing ONU Activation	77.3.5.6	Meets the requirements of Figure 77–30	ONU:M	Yes [ ]

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77.5.4.4 MPCP

Item	Feature	Subclause	Value/Comment	Status	Support
MP1	MPCPDU structure	77.3.6	As in Figure 77–31	M	Yes [ ]
MP2	LLID for MPCPDU	77.3.6	RS generates LLID for MPCPDU	M	Yes [ ]
MP3	Grants during discovery	77.3.6.1	Single grant in GATE message during discovery	OLT:M	Yes [ ]
MP4	Grant start time	77.3.6.1	Grants within one GATE MPCPDU are sorted by their Start time values	OLT:M	Yes [ ]
MP5	GATE generation	77.3.6.1	GATE generated for active ONU except during discovery	OLT:M	Yes [ ]
MP6	GATE LLID	77.3.6.1	Unicast LLID except for discovery	OLT:M	Yes [ ]
MP7	REPORT issuing	77.3.6.2	Issues REPORT periodically	ONU:M	Yes [ ]
MP8	REPORT generation	77.3.6.2	Generated by active ONU	ONU:M	Yes [ ]
MP9	REPORT generation	77.3.6.2	REPORT Queue #n length rounding	ONU:M	Yes [ ]
MP10	REPORT LLID	77.3.6.2	REPORT has unicast LLID	ONU:M	Yes [ ]
MP11	REGISTER_REQ generation	77.3.6.3	Generated by undiscovered ONU	ONU:M	Yes [ ]
MP12	REGISTER_REQ LLID	77.3.6.3	Use broadcast LLID	ONU:M	Yes [ ]
MP13	REGISTER DA address	77.3.6.4	Use individual MAC address	OLT:M	Yes [ ]
MP14	REGISTER generation	77.3.6.4	Generated for all ONUs	OLT:M	Yes [ ]
MP15	REGISTER_ACK generation	77.3.6.5	Generated by active ONU	ONU:M	Yes [ ]
MP16	REGISTER_ACK LLID	77.3.6.5	Use unicast LLID	ONU:M	Yes [ ]

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78. Energy-Efficient Ethernet (EEE)

78.1 Overview

The optional EEE capability combines the IEEE 802.3 Media Access Control (MAC) Sublayer with a family of Physical Layers defined to support operation in the Low Power Idle (LPI) mode. When the LPI mode is enabled, systems on both sides of the link can save power during periods of low link utilization.

EEE also provides a protocol to coordinate transitions to or from a lower level of power consumption and does this without changing the link status and without dropping or corrupting frames. The transition time into and out of the lower level of power consumption is kept small enough to be transparent to upper layer protocols and applications.

EEE supports operation over twisted-pair cabling systems, twinaxial cable, electrical backplanes, optical fiber, the XGXS for 10 Gb/s PHYs, the 25GAUI for 25 Gb/s PHYs, the XLAUI for 40 Gb/s PHYs, the LAUI-2 or 50GAUI-n for 50 Gb/s PHYs, the CAUI-n or 100GAUI-n for 100 Gb/s PHYs, the 200GAUI-n and 200GXS for 200 Gb/s PHYs, and the 400GAUI-n and 400GXS for 400 Gb/s PHYs. Table 78–1 lists the supported PHYs and interfaces and their associated clauses.

In addition to the above, EEE defines a 10 Mb/s MAU (10BASE-Te) with reduced transmit amplitude requirements. The 10BASE-Te MAU is fully interoperable with 10BASE-T MAUs over 100 m of class D (Category 5) or better cabling as specified in ISO/IEC 11801:1995. These requirements can also be met by Category 5 cable and components as specified in ANSI/TIA/EIA-568-B-1995. The definition of 10BASE-Te allows a reduction in power consumption.

EEE also specifies means to exchange capabilities between link partners to determine whether EEE is supported and to select the best set of parameters common to both devices. Clause 78 provides an overview of EEE operation. PICS for the optional EEE capability for each specific PHY type are specified in the respective PHY clauses. Normative requirements for Data Link Layer capabilities are contained in 78.4.

78.1.1 LPI Signaling

LPI signaling allows the LPI Client to indicate to the PHY, and to the link partner, that a break in the data stream is expected, and the LPI Client can use this information to enter power-saving modes that require additional time to resume normal operation. LPI signaling also informs the LPI Client when the link partner has sent such an indication.

The definition of LPI signaling assumes the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in the LPI mode.

The LPI Client connects to the RS service interface. LPI signaling between the RS and PCS is performed by LPI encoding on the Media Independent Interface. The transmit PCS encodes LPI symbols, which are decoded by the link partner receive PCS. The receive and transmit PCS also generate service interface signals, which are passed down to the lower PHY sublayers and indicate when receive and transmit PHY functions may be powered down.

The EEE request signals from the PCS control transitions between quiescent and normal operation. The Clause 49 PCS, Clause 107 PCS, Clause 82 PCS, and Clause 129 PCS also request transmit alert operation to assist the partner device PMD to detect the end of the quiescent state. Additionally the Clause 49 PCS, Clause 107 PCS, and Clause 82 PCS generate the RX_LPI_ACTIVE signal, which indicates to the Clause 74 BASE-R FEC that it can use rapid block lock because the link partner PCS has bypassed scrambling.

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Coding defined in 83.5.11 also allows LPI transmit quiet and alert requests from the PCS to be signaled over the 25GAUI, XLAUI, and CAUI-n interfaces. The 25GAUI, XLAUI, and CAUI-n receive interfaces infer the quiet and alert requests from the data received over the interface and use that to recreate the transmit or receive direction signaling.

The receive PCS checks that the link cycles out of the quiescent state at the correct time and that the received signals return to their expected state within the required time. The ENERGY_DETECT indicate signal is passed up from the PMA to the PCS to allow the PCS to monitor the waking process.

78.1.1.1 Reconciliation sublayer service interfaces

Figure 78–1 depicts the LPI Client and the RS interlayer service interfaces.

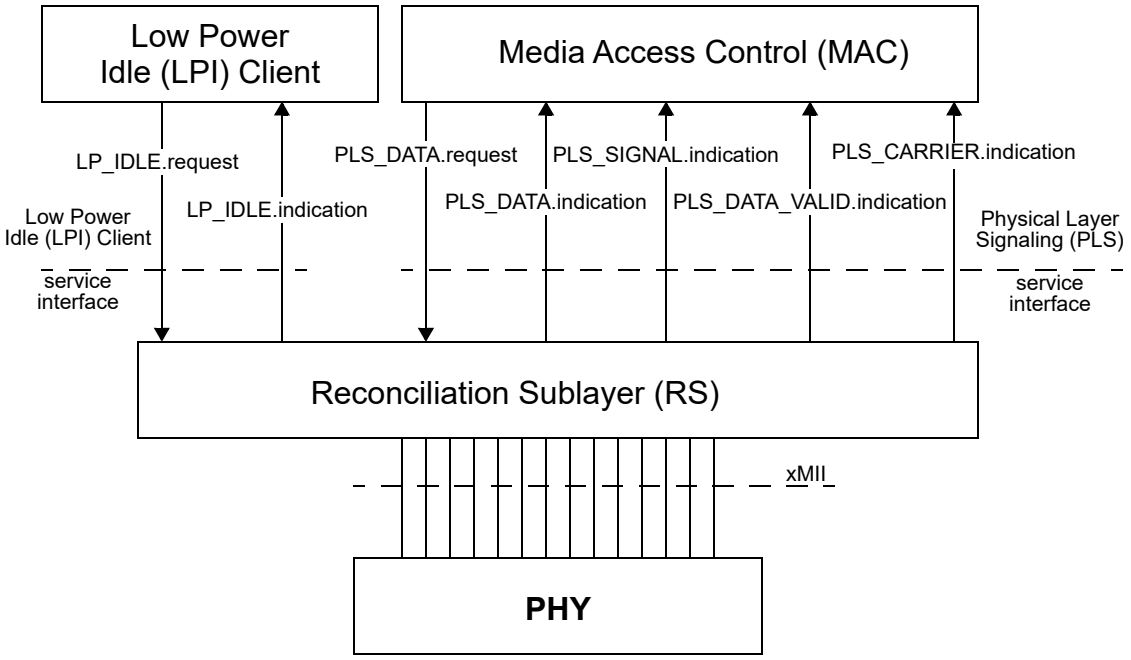

Figure 78–1—LPI Client and RS interlayer service interfaces

78.1.1.2 Responsibilities of LPI Client

The decision on when to signal LPI to the link partner is made by the LPI Client and communicated to the PHY through the RS. The LPI Client is also informed when the link partner is signaling LPI by the RS.

The conditions under which the LPI Client decides to send LPI, and what action are taken by the LPI Client when it receives LPI from the link partner, are implementation specific and beyond the scope of this standard.

78.1.2 LPI Client service interface

The following specifies the service interface provided by the RS to the LPI Client. These services are described in an abstract manner and do not imply any particular implementation.

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The following primitives are defined:

LP_IDLE.request
LP_IDLE.indication

78.1.2.1 LP_IDLE.request

78.1.2.1.1 Function

A primitive used by the LPI Client to start or stop the signaling of LPI to the link partner.

78.1.2.1.2 Semantics of the service primitive

The semantics of the service primitive are as follows:

LP_IDLE.request (LPI_REQUEST)

The LPI_REQUEST parameter can take one of two values: ASSERT or DEASSERT. ASSERT initiates the signaling of LPI to the link partner. DEASSERT stops the signaling of LPI to the link partner. The effect of receipt of this primitive is undefined in any of the following cases:

a) link_status is not OK (see 28.2.6.1.1)
b) LPI_REQUEST=ASSERT within 1 s of the change of link_status to OK
c) The PHY is indicating LOCAL FAULT
d) The PHY is indicating REMOTE FAULT

78.1.2.1.3 When generated

Specification of the time when this primitive is generated by the LPI client is out of the scope of this standard.

78.1.2.1.4 Effect of receipt

The receipt of this primitive will cause the RS to start or stop signaling LPI to the link partner.

78.1.2.2 LP_IDLE.indication

78.1.2.2.1 Function

A primitive that is used to indicate to the LPI Client that the link partner has started or stopped signaling LPI.

78.1.2.2.2 Semantics of the service primitive

The semantics of the service primitive are as follows:

LP_IDLE.indication (LPI_INDICATION)

The LPI_INDICATION parameter can take one of two values: ASSERT or DEASSERT. ASSERT indicates that the link partner has started signaling LPI. DEASSERT indicates that the link partner has stopped signaling LPI.

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78.1.2.2.3 When generated

This primitive is generated by the RS when it starts or stops receiving Assert LPI encoded on the receive xMII according to the rules defined in 78.1.3.2.

78.1.2.2.4 Effect of receipt

The effect of receipt of this primitive by the LPI client is unspecified.

78.1.3 Reconciliation sublayer operation

LPI assert and detect functions are contained in the Reconciliation Sublayer as shown in Figure 78–2. The xMII in this diagram represents any of the family of medium independent interfaces supported by EEE.

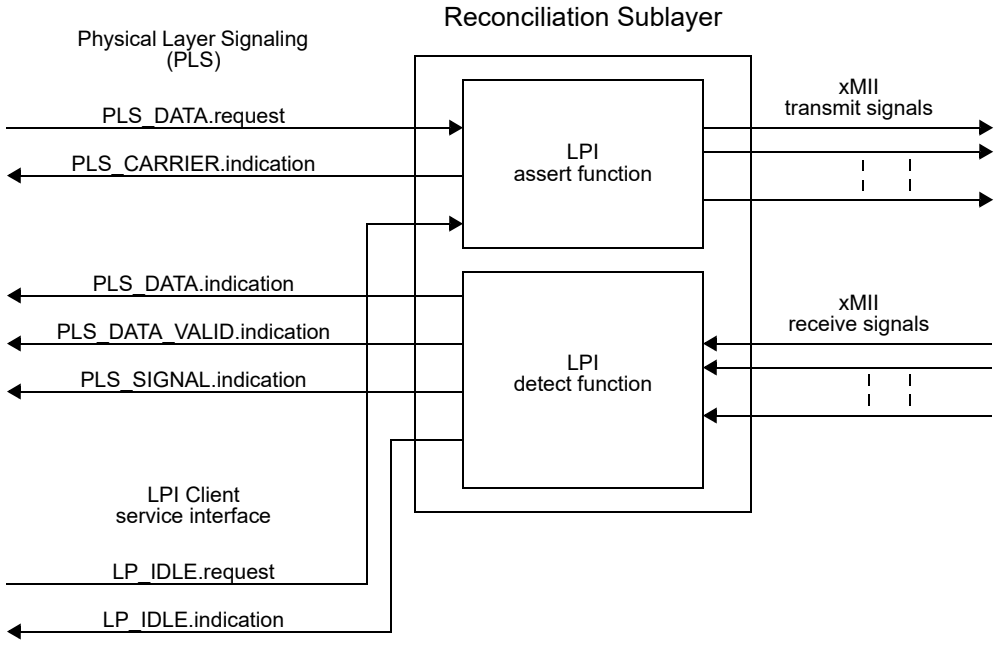

Figure 78–2—RS LPI assert and detect functions

The following provides an overview of RS LPI operation. The actual specification of RS LPI operation can be found in the respective RS clauses.

78.1.3.1 RS LPI assert function

In the absence of an LPI request, indicated by the LPI_REQUEST parameter set to DEASSERT in the LP_IDLE.request primitive of the LPI Client interface, the LPI assert function maps the PLS service interface to the transmit xMII signals as under normal conditions.

When an LPI request is asserted, indicated by the LPI_REQUEST parameter set to ASSERT in the LP_IDLE.request primitive of the LPI Client interface, the LPI assert function starts to transmit the "Assert LPI" encoding on the xMII. The LPI assert function also sets the CARRIER_STATUS parameter to CARRIER_ON in the PLS_CARRIER.indication primitive of the PLS service interface. This will prevent the MAC from transmitting.

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When the LPI request is deasserted, indicated by the LPI_REQUEST parameter set to DEASSERT in the LP_IDLE.request primitive of the LPI Client interface, the LPI assert function starts to transmit the normal interframe encoding on the xMII. After a delay, the LPI assert function sets the CARRIER_STATUS parameter to CARRIER_OFF in the PLS_CARRIER.indication primitive of the PLS service interface, allowing the MAC to start transmitting again. This delay is provided to allow the link partner to prepare for normal operation. This delay has a PHY dependent default value but this value can be adjusted using the Data Link Layer capabilities defined in 78.4.

78.1.3.2 LPI detect function

In the absence of LPI, indicated by an encoding other than “Assert LPI” on the receive xMII, the LPI detect function maps the receive xMII signals to the PLS service interface as under normal conditions.

At the start of LPI, indicated by the transition from normal interframe encoding to the “Assert LPI” encoding on the receive xMII, the LPI detect function continues to indicate idle on the PLS service interface, but sets LP_IDLE.indication(LPI_INDICATION) to ASSERT.

At the end of LPI, indicated by the transition from the “Assert LPI” encoding to any other encoding on the receive xMII, LP_IDLE.indication(LPI_INDICATION) is set to DEASSERT and the RS receive function resumes normal decode operation.

78.1.3.3 PHY LPI operation

The following provides an overview of PHY LPI operation. The specification of PHY LPI operation can be found in the respective PHY clauses (see Table 78–1).

78.1.3.3.1 PHY LPI transmit operation

When the start of “Assert LPI” encoding on the xMII is detected, the PHY signals sleep to its link partner to indicate that the local transmitter is entering LPI mode.

The EEE capability in most PHYs requires the local PHY transmitter to go quiet after sleep is signaled.

In the 1000BASE-T LPI mode, the local PHY transmitter goes quiet only after the local PHY signals sleep and receives a sleep signal from the remote PHY. If the remote PHY chooses not to signal LPI, then neither PHY can go into a low power mode; however, LPI requests are passed from one end of the link to the other regardless and system energy savings can be achieved even if the PHY link does not go into a low power mode.

The transmit function of the local PHY is enabled periodically to transmit refresh signals that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity.

This quiet-refresh cycle continues until the reception of the normal interframe encoding on the xMII. The transmit function in the PHY communicates this to the link partner by sending a wake signal for a predefined period of time. The PHY then enters the normal operating state.

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Figure 78–3 illustrates general principles of the EEE-capable transmitter operation.

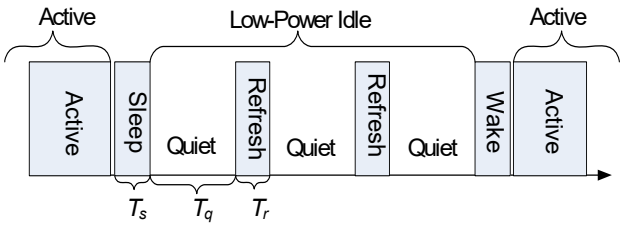
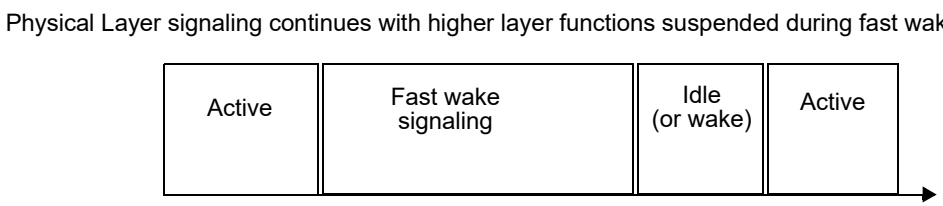


Figure 78–3—Overview of EEE LPI operation

No data frames are lost or corrupted during the transition to or from the LPI mode.

Except for BASE-T, for PHYs with an operating speed of 25 Gb/s or greater that implement the optional EEE capability, two modes of LPI operation may be supported: deep sleep and fast wake. *Deep sleep* refers to the mode for which the transmitter ceases transmission during Low Power Idle (as shown in Figure 78–3) and is equivalent to the only mechanism defined for PHYs with an operating speed of 10 Gb/s or below. Deep sleep support is optional for PHYs with an operating speed of 25 Gb/s or greater that implement EEE with the exception of the PHYs noted in Table 78–1 that do not support deep sleep. *Fast wake* refers to the mode for which the transmitter continues to transmit signals during Low Power Idle so that the receiver can resume operation with a shorter wake time (as shown in Figure 78–4). For transmit, other than the PCS encoding LPI, there is no difference between fast wake and normal operation. Except for BASE-T PHYs, fast wake support is mandatory for PHYs with an operating speed of 25 Gb/s or greater that implement EEE.



NOTE—Fast wake signaling continually indicates LPI in a normally constituted data stream.

Figure 78–4—Overview of fast wake operation

WARNING
The signaling in deep sleep operation precludes transparent mapping of the link over Optical Transport Networks. Only fast wake operation should be enabled for any link that is intended for transparent OTN mapping.

78.1.3.3.2 PHY LPI receive operation

In the receive direction, entering the LPI mode is triggered by the reception of a sleep signal from the link partner, which indicates that the link partner is about to enter the LPI mode. After sending the sleep signal, the link partner ceases transmission if not in fast wake mode. When the receiver detects the sleep signal, the local PHY indicates “Assert LPI” on the xMII and the local receiver can disable some functionality to reduce power consumption.

If not in fast wake mode the link partner periodically transmits refresh signals that are used by the local PHY to update adaptive coefficients and timing circuits. This quiet-refresh cycle continues until the link partner

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initiates transition back to normal mode by transmitting the wake signal for a predetermined period of time controlled by the LPI assert function in the RS. This allows the local receiver to prepare for normal operation and transition from the "Assert LPI" encoding to the normal interframe encoding on the xMII. After a system specified recovery time, the link supports the nominal operational data rate.

78.1.4 PHY types optionally supporting EEE

EEE defines a low power mode of operation for the IEEE 802.3 PHYs and interfaces listed in Table 78–1. The table also lists the clauses associated with each PHY or sublayer. Normative requirements for the EEE capability for each PHY type and interface are in the associated clauses.

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
10BASE-Te	14
10BASE-T1L	146
100BASE-TX	24, 25
1000BASE-KX	70, 36
1000BASE-T1	97
1000BASE-RHC	115
1000BASE-RHA	115
1000BASE-RHB	115
1000BASE-T	40
2.5GBASE-KX	127, 128
2.5GBASE-T1	149
2.5GBASE-T	126
5GBASE-KR	129, 130
5GBASE-T1	149
5GBASE-T	126
XGXS (XAUI)	47, 48
10GBASE-KX4	71, 48
10GBASE-KR	72, 51, 49, 74
10GBASE-T1	149
10GBASE-T	55
25GAUI[a]	109A
25GBASE-KR-S	74, 107, 109, 111
25GBASE-KR	74, 107, 108, 109, 111
25GBASE-CR-S	74, 107, 109, 110
25GBASE-CR	74, 107, 108, 109, 110
25GBASE-T	113
25GBASE-SR[b]	107, 108, 109, 112

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Table 78–1—Clauses associated with each PHY or interface type *(continued)*

PHY or interface type	Clause
25GBASE-BR10[b]	159
25GBASE-LR[b]	107, 108, 109, 114
25GBASE-BR20[b]	159
25GBASE-BR40[b]	159
25GBASE-ER[b]	107, 108, 109, 114
XLAUI[a]	83A
40GBASE-KR4	82, 83, 84, 74
40GBASE-CR4	82, 83, 85, 74
40GBASE-T	113
40GBASE-SR4[b]	82, 83, 86
40GBASE-FR[b]	82, 83, 89
40GBASE-LR4[b]	82, 83, 87
40GBASE-ER4[b]	82, 83, 87
50GBASE-KR[b]	133, 134, 137
50GBASE-CR[b]	133, 134, 136
50GBASE-SR[b]	133, 134, 138
50GBASE-FR[b]	133, 134, 139
50GBASE-BR10[b]	160
50GBASE-LR[b]	133, 134, 139
50GBASE-BR20[b]	160
50GBASE-BR40[b]	160
50GBASE-ER[b]	133, 134, 139
CAUI-10[a]	83A
CAUI-4[a]	83D
100GBASE-KR4	82, 83, 91, 93
100GBASE-KP4	82, 91, 94
100GBASE-KR2[b]	82, 135, 137
100GBASE-CR2[b]	82, 135, 136
100GBASE-CR4	82, 83, 91, 92
100GBASE-CR10	82, 83, 85, 74
100GBASE-SR4[b]	82, 83, 91, 95
100GBASE-SR2[b]	82, 135, 138
100GBASE-SR10[b]	82, 83, 86
100GBASE-DR[b]	82, 135, 140

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Table 78–1—Clauses associated with each PHY or interface type *(continued)*

PHY or interface type	Clause
100GBASE-FR1[b]	82, 135, 140
100GBASE-LR4[b]	82, 83, 88
100GBASE-LR1[b]	82, 135, 140
100GBASE-ER4[b]	82, 83, 88
100GBASE-ZR[b]	82, 83, 91, 135, 152, 153, 154
200GBASE-KR4[b]	119, 120, 137
200GBASE-CR4[b]	119, 120, 136
200GBASE-SR4[b]	119, 120, 138
200GBASE-DR4[b]	119, 120, 121
200GBASE-FR4[b]	119, 120, 122
200GBASE-LR4[b]	119, 120, 122
200GBASE-ER4[b]	119, 120, 122
400GBASE-SR16[b]	119, 120, 123
400GBASE-SR8[b]	119, 120, 138
400GBASE-SR4.2[b]	119, 120, 150
400GBASE-DR4[b]	119, 120, 124
400GBASE-FR8[b]	119, 120, 122
400GBASE-FR4[b]	119, 120, 151
400GBASE-LR4-6[b]	119, 120, 151
400GBASE-LR8[b]	119, 120, 122
400GBASE-ER8[b]	119, 120, 122

[a]25GAUI/XLAUI/CAUI-n shutdown is supported only when deep sleep is enabled for the associated PHY.
[b]The deep sleep mode of EEE is not supported for this PHY.

78.2 LPI mode timing parameters description

T_s	The period of time that the PHY transmits the sleep signal before turning all transmitters off
T_q	The period of time that the PHY remains quiet before sending the refresh signal
T_r	Duration of the refresh signal
$T_{phy\_prop\_tx}$	The propagation delay of a given unit of data from the xMII to the MDI
$T_{phy\_prop\_rx}$	The propagation delay of a given unit of data from the MDI to the xMII

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$T_{phy\_shrink\_tx}$ Transmitter shrinkage time, defined as the absolute time difference between the following two timing parameters:

—Delay between a transition from the "Assert LPI" to "Normal Idle" at the xMII and the corresponding start of the wake signal at the MDI

—$T_{phy\_prop\_tx}$

$T_{phy\_shrink\_rx}$ Receiver shrinkage time, defined as the absolute time difference between the following two timing parameters:

—Delay between start of the wake signal at the MDI and the corresponding transition from "Assert LPI" to "Normal Idle" at the xMII

—$T_{phy\_prop\_rx}$

T_{w_phy} Parameter employed by the system that corresponds to the behavior of the PHY. It is the period of time between reception of an IDLE signal on the xMII and when the first data codewords are permitted on the xMII. The wake time of a compliant PHY does not exceed T_{w_phy} (min).

$T_{w\_sys\_tx}$ Parameter employed by the system that corresponds to its requirements. It is the longest period of time the system has to wait between a request to transmit and its readiness to transmit.

$T_{w\_sys\_rx}$ Parameter employed by the system that corresponds to its requirements. It is the minimum time required by the system between a request to wake and its readiness to receive data.

Table 78–2 summarizes three key EEE parameters (T_s, T_q, and T_r) for supported PHYs.

Table 78–2—Summary of the key EEE parameters for supported PHYs or interfaces

PHY or interface type	T_s (μs)		T_q (μs)		T_r (μs)	
	Min	Max	Min	Max	Min	Max
10BASE-T1L	20	20	6 000	6 000	250	250
100BASE-TX	200	220	20 000	22 000	200	220
1000BASE-KX	19.9	20.1	2 500	2 600	19.9	20.1
1000BASE-T1	3.6	3.6	84.95	84.97	1.44	1.44
1000BASE-RHC 1000BASE-RHA 1000BASE-RHB	0	0	23.52	23.52	1.3	1.3
1000BASE-T	182	202	20 000	24 000	198	218.2
2.5GBASE-KX	19.9	20.1	2 500	2 600	19.9	20.1
2.5GBASE-T1	10.24	10.24	121.6	121.6	1.28	1.28
2.5GBASE-T	11.52	12.8	76.8	76.8	5.12	5.12
5GBASE-KR	4.9	5.1	1 700	1 800	16.9	17.5
5GBASE-T1	5.12	5.12	60.8	60.8	0.64	0.64
5GBASE-T	5.76	6.4	38.4	38.4	2.56	2.56

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Table 78–2—Summary of the key EEE parameters for supported PHYs or interfaces *(continued)*

PHY or interface type	T_s (μs)		T_q (μs)		T_r (μs)	
	Min	Max	Min	Max	Min	Max
XGXS (XAUI)	19.9	20.1	2 500	2 600	19.9	20.1
10GBASE-KX4	19.9	20.1	2 500	2 600	19.9	20.1
10GBASE-KR	4.9	5.1	1 700	1 800	16.9	17.5
10GBASE-T1	2.56	2.56	30.4	30.4	0.32	0.32
10GBASE-T	2.88	3.2	39.68	39.68	1.28	1.28
25GBASE-KR-S 25GBASE-KR 25GBASE-CR-S 25GBASE-CR	4.9	5.1	1 700	1 800	16.9	17.5
25GBASE-T	0.768	0.896	15.616	15.616	0.768	0.768
40GBASE-KR4 40GBASE-CR4	0.9	1.1	1 700	1 800	5.9	6.5
40GBASE-T	0.48	0.56	9.76	9.76	0.48	0.48
100GBASE-KR4 100GBASE-KP4 100GBASE-CR4 100GBASE-CR10	0.9	1.1	1 700	1 800	5.9	6.5

Figure 78–5 illustrates the relationship between the LPI mode timing parameters and the minimum system wake time.

78.3 Capabilities Negotiation

The EEE capability shall be advertised during the Auto-Negotiation stage, except for PHYs that only support fast wake operation or PHYs that exchange EEE capability during link training. Auto-Negotiation provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation. Auto-Negotiation is performed at power up, on command from management, due to link failure, or due to user intervention. Fast wake capability shall be advertised using L2 protocol frames as described in 78.4. The EEE capability for 2.5GBASE-T and 5GBASE-T shall be advertised during link training according to 126.4.2.5.10. The EEE capability for 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 shall be advertised during link training according to 149.4.2.4.10. The EEE capability for 25GBASE-T and 40GBASE-T shall be advertised during link training according to 113.4.2.5.10.

During Auto-Negotiation, both link partners indicate their EEE capabilities. EEE is supported only if during Auto-Negotiation both the local device and link partner advertise the EEE capability for the resolved PHY type. If EEE is not supported, all EEE functionality is disabled and the LPI client does not assert LPI. EEE deep sleep operation shall not be enabled unless both the local device and link partner advertise deep sleep capability during Auto-Negotiation for the resolved PHY type. If EEE is supported by both link partners for the negotiated PHY type, then the EEE function can be used independently in either direction. The same applies to 2.5GBASE-T, 2.5GBASE-T1, 5GBASE-T, 5GBASE-T1, 10GBASE-T1, 25GBASE-T, and

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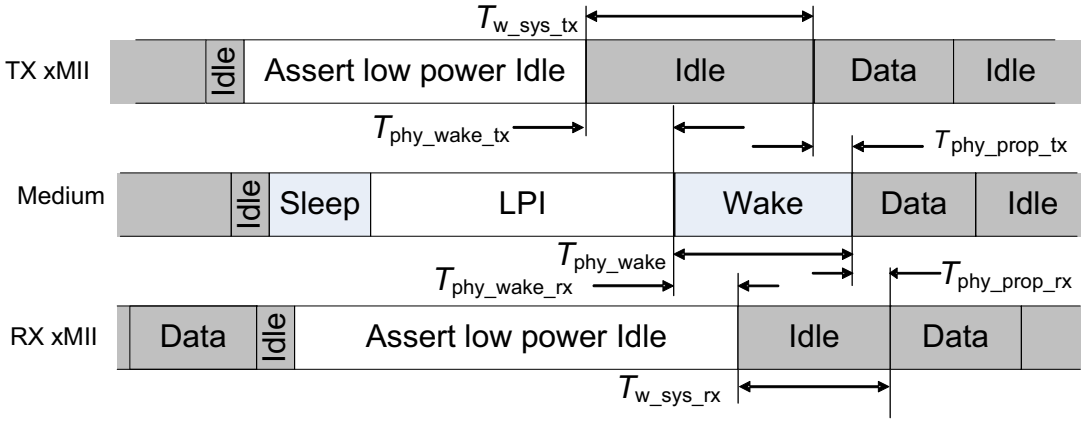

$T_{w\_sys\_tx}$ (min) = $T_{w\_sys\_rx}$ (min) + $T_{phy\_shrink\_tx}$ (max) + $T_{phy\_shrink\_rx}$ (max)
T_{w_phy} (min) = T_{phy_wake} (min) + $T_{phy\_shrink\_tx}$

$T_{w\_sys\_res}$ (min) is greater of $T_{w\_sys\_tx}$ (min) and T_{w_phy} (min)

$T_{phy\_shrink\_tx}$ (max) = ($T_{phy\_wake\_tx}$ (max) – $T_{phy\_prop\_tx}$ (min))
$T_{phy\_shrink\_rx}$ (max) = ($T_{phy\_wake\_rx}$(max) – $T_{phy\_prop\_rx}$ (min))

where

$T_{phy\_wake\_tx}$ = xMII start of wake to MDI start of wake delay
$T_{phy\_prop\_tx}$ = xMII to MDI data propagation delay
$T_{phy\_wake\_rx}$ = MDI start of wake to xMII start of wake delay
$T_{phy\_prop\_rx}$ = MDI to xMII data propagation delay
T_{phy_wake} = Minimum wake duration required by PHY

Figure 78–5—LPI mode timing parameters and their relationship to minimum system wake time

40GBASE-T except the EEE capabilities are exchanged and resolved during link training instead of during Auto-Negotiation.

Additional capabilities and settings using L2 protocol frames, including the adjustment of the $T_{w\_sys\_tx}$ parameter, are described in 78.4.

78.4 Data Link Layer capabilities

Additional capabilities and settings are supported using frames based on the IEEE 802.3 Organizationally Specific TLVs are defined in Annex F of IEEE Std 802.1AB™-2009. Devices that require longer wake-up times prior to being able to accept data on their receive paths may use the Data Link Layer capabilities defined in this subclause to negotiate for extended system wake-up times from the transmitting link partner. This mechanism may allow for more or less aggressive energy saving modes.

The Data Link Layer capabilities shall be implemented for devices with an operating speed equal to or greater than 10 Gb/s and may be implemented for all other devices. The use of the EEE Fast Wake TLV shall be interpreted as an indication that the device supports EEE fast wake operation, regardless of the capability advertised during the Auto-Negotiation stage. A device shall not indicate deep sleep capability using the EEE Fast Wake TLV unless both the local device and link partner advertise deep sleep capability during Auto-Negotiation for the resolved PHY type.

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Implementations that use the Data Link Layer capabilities shall comply with all mandatory parts of IEEE Std 802.1AB-2009; shall support the EEE Type, Length, Value (TLV) defined in 79.3.5; timing requirement in 78.4.1; and shall support the control state diagrams defined in 78.4.2. Devices with an operating speed equal to or greater than 40 Gb/s shall support EEE Fast Wake TLV as defined in 79.3.6.

The Data Link Layer capabilities are described from a unidirectional perspective on the link between transmitting and receiving link partners. For duplex EEE links that implement the Data Link Layer capabilities, each link partner shall implement the TLV, control and state diagrams for a transmitter as well as a receiver.

For purposes of Data Link Layer capabilities, all values that are negotiated and/or exchanged that have a fractional value shall be rounded up to the nearest integer number in microseconds.

78.4.1 Data Link Layer capabilities timing requirements

An EEE link partner shall send an LLDPDU containing an EEE TLV within 10 s of the Link Layer capability exchange being enabled when both the variables dll_enabled and dll_ready are asserted.

An LLDPDU containing an EEE TLV with an updated value for the "Echo Transmit $T_{w\_sys\_tx}$" field shall be sent within 10 s of receipt of an LLDPDU containing an EEE TLV where the value of "Transmit $T_{w\_sys\_tx}$" field is different from the previously communicated value.

An LLDPDU containing an EEE TLV with an updated value for the "Echo Receive $T_{w\_sys\_tx}$" field shall be sent within 10 s of receipt of an LLDPDU containing an EEE TLV where the value of "Receive $T_{w\_sys\_tx}$" field is different from the previously communicated value.

78.4.2 Control state diagrams

The control state diagrams for an EEE transmitting link partner and an EEE receiving link partner specify the externally observable behavior of an EEE transmitting link partner and an EEE receiving link partner implementing Data Link Layer capabilities respectively. EEE transmitting link partners implementing Data Link Layer capabilities shall provide the behavior of the state diagram as shown in Figure 78–6. EEE receiving link partners implementing Data Link Layer capabilities shall provide the behavior of the state diagram as shown in Figure 78–7.

78.4.2.1 Conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

78.4.2.2 Constants

PHY WAKE VALUE

Integer (2 octets wide) representing the $T_{w\_sys\_tx}$ (min) defined for the PHY that is in use for the link. This parameter should be rounded up to the nearest integer number when it is calculated and examined according to 78.2 and Table 78–4.

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78.4.2.3 Variables

Unless otherwise specified, all integers are assumed to be 2 octets wide.

LocTxSystemValue
: Integer that indicates the value of $T_{w\_sys\_tx}$ that the local system can support. This value is updated by the EEE DLL Transmitter state diagram. This variable maps into the aLldpXdot3LocTxTwSys attribute.

RemTxSystemValueEcho
: Integer that indicates the value Transmit $T_{w\_sys\_tx}$ echoed back by the remote system. This value maps from the aLldpXdot3RemTxTwSysEcho attribute.

LocRxSystemValue
: Integer that indicates the value of $T_{w\_sys\_tx}$ that the local system requests from the remote system. This value is updated by the EEE Receiver L2 state diagram. This variable maps into the aLldpXdot3LocRxTwSys attribute.

RemRxSystemValueEcho
: Integer that indicates the value of Receive $T_{w\_sys\_tx}$ echoed back by the remote system. This value maps from the aLldpXdot3RemRxTwSysEcho attribute.

LocFbSystemValue
: Integer that indicates the value of fallback $T_{w\_sys\_tx}$ that the local system requests from the remote system. This value is updated by the local system software.

RemTxSystemValue
: Integer that indicates the value of $T_{w\_sys\_tx}$ that the remote system can support. This value maps from the aLldpXdot3RemTxTwSys attribute.

LocTxSystemValueEcho
: Integer that indicates the remote system's Transmit $T_{w\_sys\_tx}$ that was used by the local system to compute the $T_{w\_sys\_tx}$ that it wants to request from the remote system. This value maps into the aLldpXdot3LocTxTwSysEcho attribute.

RemRxSystemValue
: Integer that indicates the value of $T_{w\_sys\_tx}$ that the remote system requests from the local system. This value maps from the aLldpXdot3RemRxTwSys attribute.

LocRxSystemValueEcho
: Integer that indicates the remote systems Receive $T_{w\_sys\_tx}$ that was used by the local system to compute the $T_{w\_sys\_tx}$ that it can support. This value maps into the aLldpXdot3LocRxTwSysEcho attribute.

LocResolvedTxSystemValue
: Integer that indicates the current $T_{w\_sys\_tx}$ supported by the local system.

LocResolvedRxSystemValue
: Integer that indicates the current $T_{w\_sys\_tx}$ supported by the remote system.

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LPI_FW
: Boolean variable controlling the wake mode for the LPI transmit and receive functions as defined in 82.2.19.2.2.

LocTxSystemFW
: Boolean variable that indicates the state of LPI_FW that the local transmit system can support. This value is updated by the EEE DLL Transmit fast wake state diagram. This variable maps into the aLldpXdot3LocTxFw attribute.

RemTxSystemFWEcho
: Boolean variable that indicates the state of transmit LPI_FW echoed back by the remote system. This value maps from the aLldpXdot3RemTxFwEcho attribute.

LocRxSystemFW
: Boolean variable that indicates the state of LPI_FW that the local receive system requests from the remote system. This value is updated by the EEE DLL Receive fast wake state diagram. This variable maps into the aLldpXdot3LocRxFw attribute.

RemRxSystemFWEcho
: Boolean variable that indicates the state of receive LPI_FW echoed back by the remote system. This value maps from the aLldpXdot3RemRxFwEcho attribute.

RemTxSystemFW
: Boolean variable that indicates the LPI_FW that the remote transmit system requests from the local system. This value maps from the aLldpXdot3RemTxFw attribute.

LocTxSystemFWEcho
: Boolean variable that indicates the remote system's transmit LPI_FW that was used by the local system to decide the LPI_FW that it wants to request from the remote system. This value maps into the aLldpXdot3LocTxFwEcho attribute.

RemRxSystemFW
: Boolean variable that indicates the LPI_FW that the remote receive system requests from the local system. This value maps from the aLldpXdot3RemRxFw attribute.

LocRxSystemFWEcho
: Boolean variable that indicates the remote system's receive LPI_FW that was used by the local system to decide the LPI_FW that it can support. This value maps into the aLldpXdot3LocRxFwEcho attribute.

LocResolvedTxSystemFW
: Boolean that indicates the current LPI_FW supported by the local system.

LocResolvedRxSystemFW
: Boolean variable that indicates the current LPI_FW supported by the remote system.

TempTxFW
: Boolean variable used to store the value of LPI_FW.

TempRxFW
: Boolean variable used to store the value of LPI_FW.

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local_system_FW_change
: An implementation-specific control variable that indicates that the local system wants to change either the Transmit LPI_FW or the Receive LPI_FW.

NEW_TX_FW
: Boolean variable that indicates the value of transmit LPI_FW that the local system can support.

NEW_RX_FW
: Boolean variable that indicates the value of receive LPI_FW that the local system wants the remote system to support.

TempTxVar
: Integer used to store the value of $T_{w\_sys\_tx}$.

TempRxVar
: Integer used to store the value of $T_{w\_sys\_tx}$.

local_system_change
: An implementation specific control variable that indicates that the local system wants to change either the Transmit $T_{w\_sys\_tx}$ or the Receive $T_{w\_sys\_tx}$.

tx_dll_ready
: Data Link Layer ready: This variable indicates that the tx system initialization is complete and is ready to update/receive LLDPDU containing EEE TLV. This variable is updated by the local system software.

rx_dll_ready
: Data Link Layer ready: This variable indicates that the rx system initialization is complete and is ready to update/receive LLDPDU containing EEE TLV. This variable is updated by the local system software.

NEW_TX_VALUE
: Integer that indicates the value of $T_{w\_sys\_tx}$ that the local system can support.

NEW_RX_VALUE
: Integer that indicates the value of $T_{w\_sys\_tx}$ that the local system wants the remote system to support.

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A summary of cross-references between the EEE object class attributes and the transmit and receive control state diagrams, including the direction of the mapping, is provided in Table 78–3.

Table 78–3—Attribute to state diagram variable cross-reference

Entity	Object class	Attribute	Mapping	State diagram variable
TX	oLldpXdot3Loc-SystemsGroup	aLldpXdot3LocTxTwSys	⇐	LocTxSystemValue
		aLldpXdot3LocRxTwSysEcho	⇐	LocRxSystemValueEcho
		aLldpXdot3LocDllEnabled	⇒	tx_dll_enabled
		aLldpXdot3LocTxDllReady	⇐	tx_dll_ready
		aLldpXdot3LocTxFw	⇐	LocTxSystemFW
		aLldpXdot3LocRxFwEcho	⇐	LocRxSystemFWEcho
	oLldpXdot3Rem-SystemsGroup	aLldpXdot3RemRxTwSys	⇒	RemRxSystemValue
		aLldpXdot3RemTxTwSysEcho	⇒	RemTxSystemValueEcho
		aLldpXdot3RemRxFw	⇒	RemRxSystemFW
		aLldpXdot3RemTxFwEcho	⇒	RemTxSystemFWEcho
RX	oLldpXdot3Loc-SystemsGroup	aLldpXdot3LocRxTwSys	⇐	LocRxSystemValue
		aLldpXdot3LocTxTwSysEcho	⇐	LocTxSystemValueEcho
		aLldpXdot3LocFbTwSys	⇐	LocFbSystemValue
		aLldpXdot3LocDllEnabled	⇒	rx_dll_enabled
		aLldpXdot3LocRxDllReady	⇐	rx_dll_ready
		aLldpXdot3LocRxFw	⇐	LocRxSystemFW
		aLldpXdot3LocTxFwEcho	⇐	LocTxSystemFWEcho
	oLldpXdot3Rem-SystemsGroup	aLldpXdot3RemTxTwSys	⇒	RemTxSystemValue
		aLldpXdot3RemRxTwSysEcho	⇐	RemRxSystemValueEcho
		aLldpXdot3RemTxFw	⇒	RemTxSystemFW
		aLldpXdot3RemRxFwEcho	⇐	RemRxSystemFWEcho

78.4.2.4 Functions

examine_Tx_change

This function computes the new value of $T_{w\_sys\_tx}$ that the local system can support when there is as updated request from the remote system or if local system conditions require a change in the value of the presently supported $T_{w\_sys\_tx}$.

examine_Rx_change

This function computes the new value of $T_{w\_sys\_tx}$ that the local system wants the remote system to support. This function is called when the remote system wants to change its presently allocated

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$T_{w\_sys\_tx}$ or if local system conditions require a change in the value of $T_{w\_sys\_tx}$ presently supported by the remote system.

examine_TxFW_change
: This function decides if the new value of LPI_FW is acceptable by the local transmit system when there is an updated request from the remote system or if local system conditions require a change in the value of the presently supported LPI_FW.

examine_RxFW_change
: This function decides if the new value of LPI_FW is acceptable by the local receive system when there is an updated request from the remote system or if local system conditions require a change in the value of the presently supported LPI_FW.

78.4.2.5 State diagrams

Control for placing data on the medium rests with the transmitting side, hence $T_{w\_sys\_tx}$ is enforced by the transmitter. For a given path between link partners (i.e., a transmitter and its associated receiver), the transmitting link partner shall wait for the time indicated by the Transmit $T_{w\_sys\_tx}$ after deasserting LPI (at the xMII) before sending data frames. The receiving link partner shall be ready to accept data based on its echoed value of Transmit link partner's $T_{w\_sys\_tx}$. This ensures that the link partners transition out of LPI mode and receive frames without loss or corruption.

The general state change procedure for transmitter is shown in Figure 78–6.

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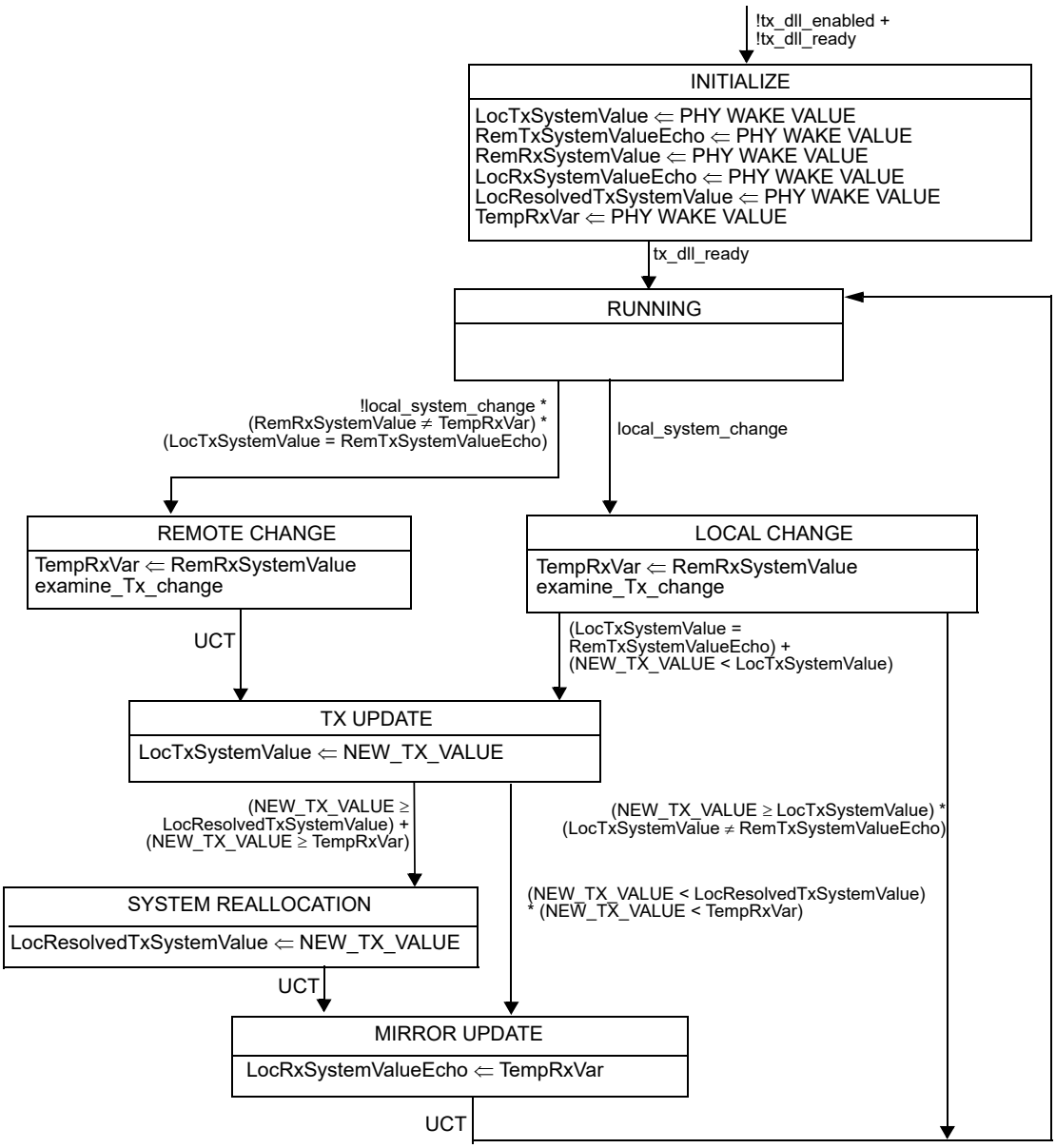

Figure 78–6—EEE DLL Transmitter state diagram

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The general state change procedure for receiver is shown in Figure 78–7.

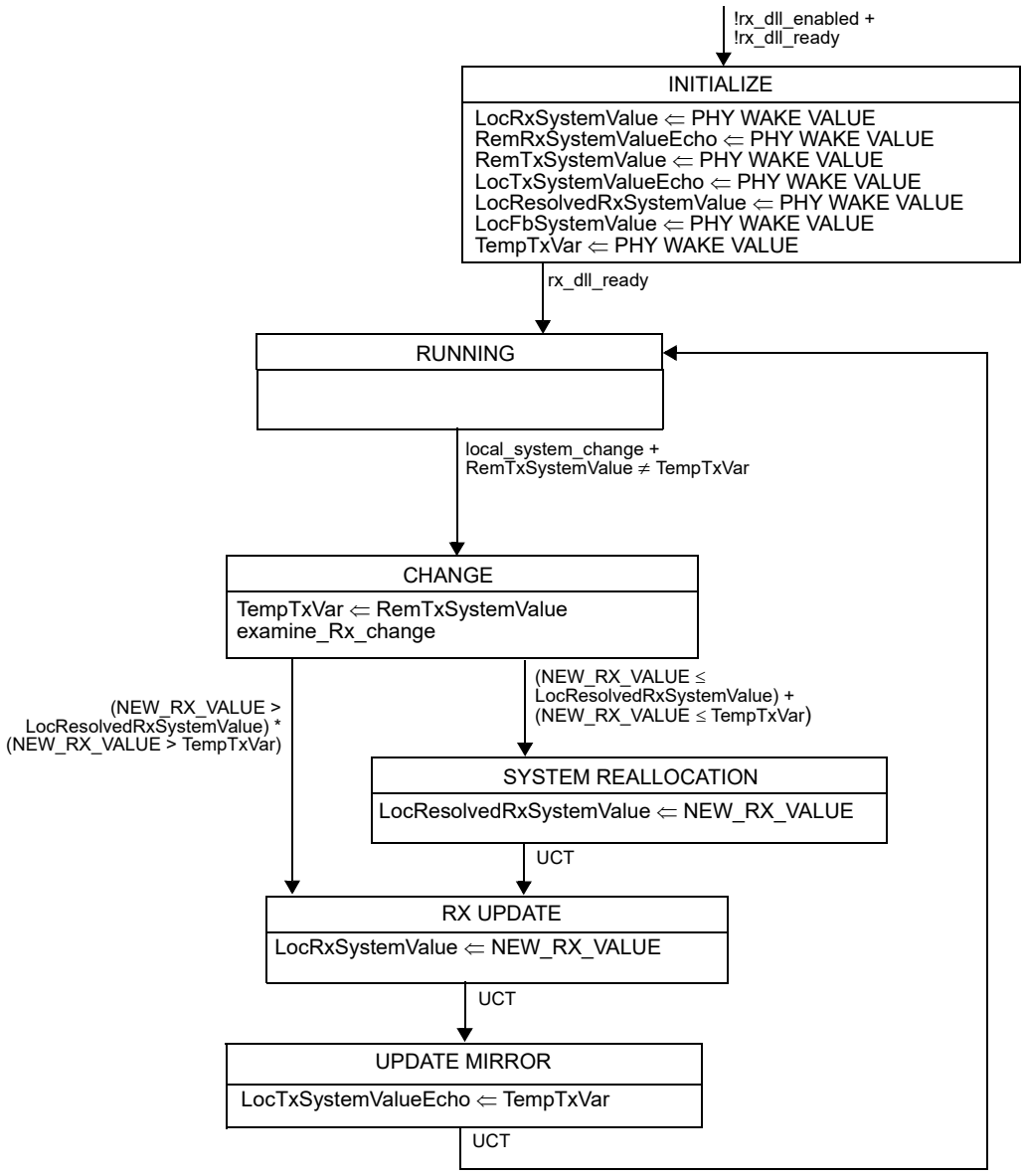

Figure 78–7—EEE DLL Receiver state diagram

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The general state change procedure for transmitter fast wake is shown in Figure 78–8.

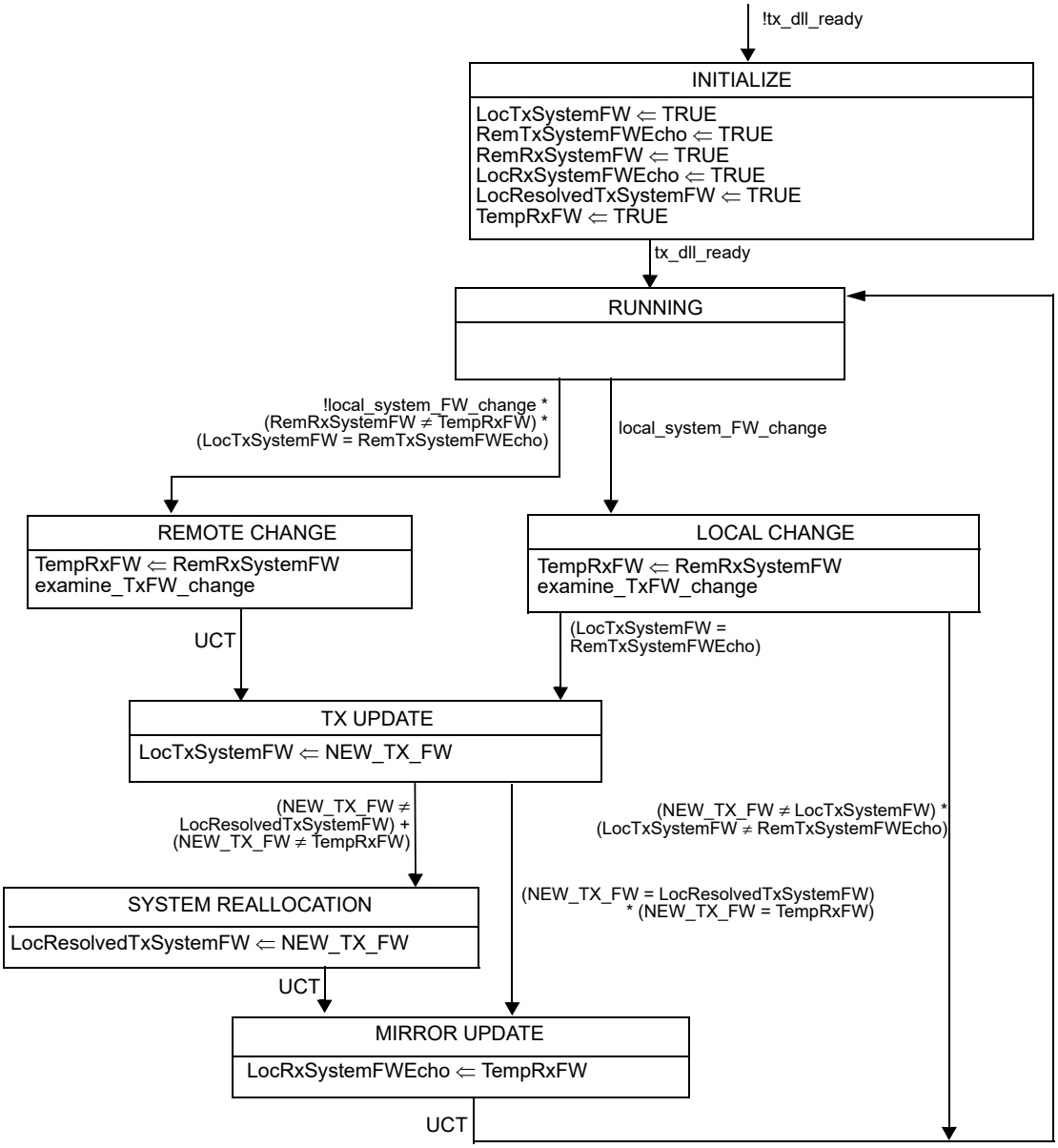

Figure 78–8—EEE DLL Transmitter fast wake state diagram

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The general state change procedure for receiver fast wake is shown in Figure 78–9.

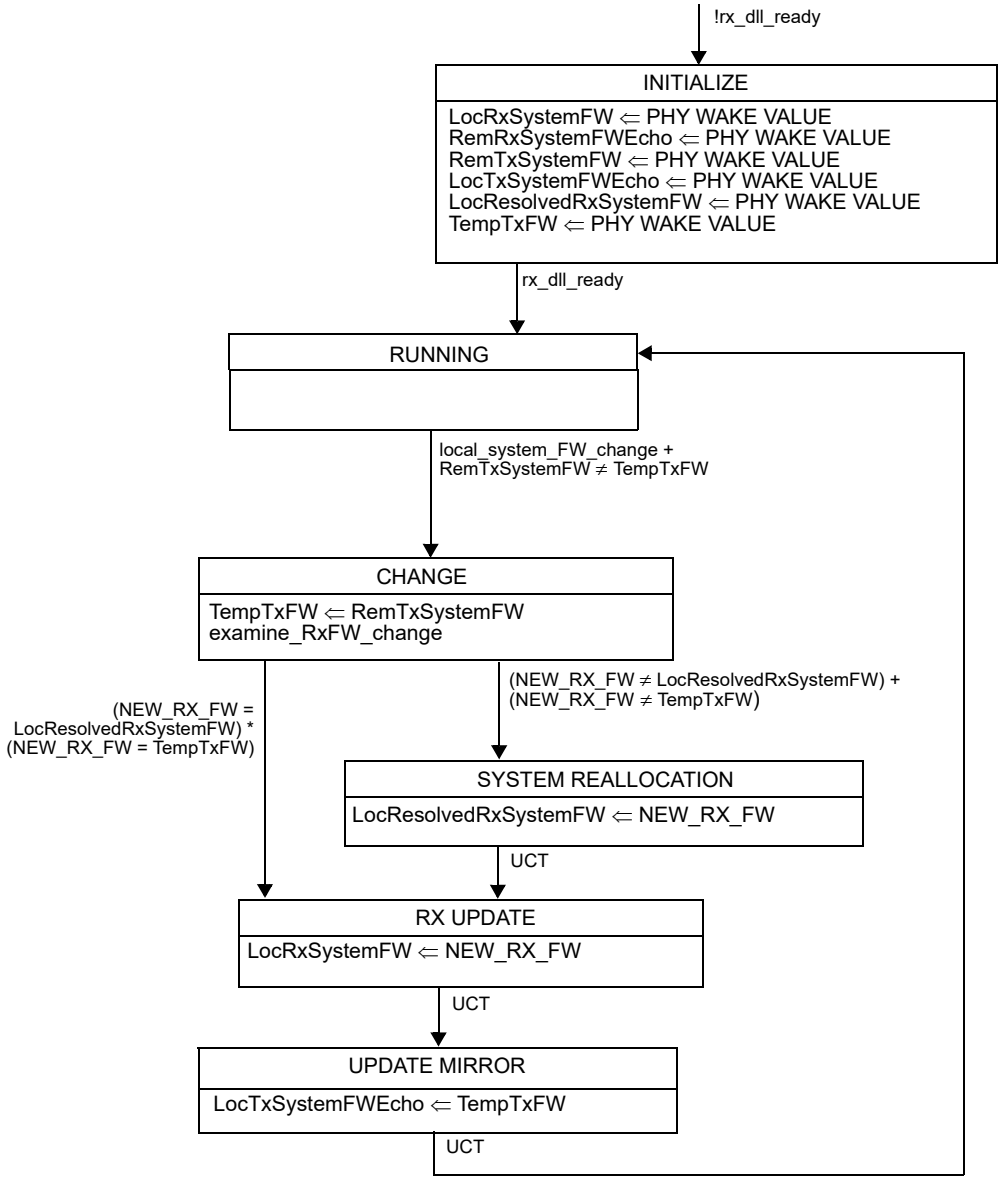

Figure 78–9—EEE DLL Receiver fast wake state diagram

78.4.3 State change procedure across a link

The transmitting and receiving link partners utilize the LLDP mechanism to advertise their various attributes to the other entity.

The initial $T_{w\_sys\_tx}$ defaults governing the EEE operation of the link default to the wake values required by the PHYs. This provides for EEE operation and functionality on initialization and prior to the exchange and processing of the TLVs.

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The receiving link partner may request a new $T_{w\_sys\_tx}$ value through the aLldpXdot3LocRxTwSys (30.12.2.1.64) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The request appears to the transmitting link partner as a change to the aLldpXdot3RemRxTwSys (30.12.3.1.62) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class. The transmitting link partner responds to its receiving partner's request through the aLldpXdot3LocTxTwSys (30.12.2.1.62) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The transmitting link partner also copies the value of the aLldpXdot3RemRxTwSys (30.12.3.1.62) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class to the aLldpXdot3LocRxTwSysEcho (30.12.2.1.65) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2).

The transmitting link partner may advertise new value of $T_{w\_sys\_tx}$ through the aLldpXdot3LocTxTwSys (30.12.2.1.62) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). This appears to the receiving link partner as a change to the aLldpXdot3RemTxTwSys (30.12.3.1.60) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class. The receiving link partner responds to a transmitter's request through the aLldpXdot3LocRxTwSys (30.12.2.1.64) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The receiving link partner also copies the value of the aLldpXdot3RemTxTwSys (30.12.3.1.60) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class to the aLldpXdot3LocTxTwSysEcho (30.12.2.1.63) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). This appears to the transmitting link partner as a change to the aLldpXdot3RemTxTwSysEcho (30.12.3.1.61) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3).

The state diagrams in Figure 78–6 and Figure 78–7 describe the preceding behavior.

The default state of Fast_Wake_Enable is TRUE for all PHYs that support the function. This provides for EEE operation and functionality on initialization and prior to the exchange and processing of the TLVs.

The receiving link partner may request a change of Fast_Wake_Enable through the aLldpXdot3LocRxFw (30.12.2.1.72) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The request appears to the transmitting link partner as a change to the aLldpXdot3RemRxFw (30.12.3.1.26) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class. The transmitting link partner responds to its receiving partner's request through the aLldpXdot3LocTxFw (30.12.2.1.70) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The transmitting link partner also copies the value of the aLldpXdot3RemRxFw (30.12.3.1.26) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class to the aLldpXdot3LocRxFwEcho (30.12.2.1.73) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2).

The transmitting link partner may advertise a change of Fast_Wake_Enable through the aLldpXdot3LocTxFw (30.12.2.1.70) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). This appears to the receiving link partner as a change to the aLldpXdot3RemTxFw (30.12.3.1.24) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class. The receiving link partner responds to a transmitter's request through the aLldpXdot3LocRxFw (30.12.2.1.72) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The receiving link partner also copies the value of the aLldpXdot3RemTxFw (30.12.3.1.24) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class to the aLldpXdot3LocTxFwEcho (30.12.2.1.71) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). This appears to the transmitting link partner as a change to the aLldpXdot3RemTxFwEcho (30.12.3.1.25) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3).

The state diagrams in Figure 78–8 and Figure 78–9 describe the preceding behavior.

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78.4.3.1 Transmitting link partner's state change procedure across a link

A transmitting link partner is said to be in sync with the receiving link partner if the presently advertised value of Transmit $T_{w\_sys\_tx}$ and the corresponding echoed value are equal.

During normal operation, the transmitting link partner is in the RUNNING state. If the transmitting link partner wants to initiate a change to the presently resolved value of $T_{w\_sys\_tx}$, the local_system_change is asserted and the transmitting link partner enters the LOCAL CHANGE state where NEW_TX_VALUE is computed. If the new value is smaller than the presently advertised value of $T_{w\_sys\_tx}$ or if the transmitting link partner is in sync with the receiving link partner, then it enters TX UPDATE state. Otherwise, it returns to the RUNNING state.

If the transmitting link partner sees a change in the $T_{w\_sys\_tx}$ requested by the receiving link partner, it recognizes the request only if it is in sync with the transmitting link partner. The transmitting link partner examines the request by entering the REMOTE CHANGE state where a NEW TX VALUE is computed and it then enters the TX UPDATE state.

Upon entering the TX UPDATE state, the transmitter updates the advertised value of Transmit $T_{w\_sys\_tx}$ with NEW_TX_VALUE. If the NEW_TX_VALUE is equal to or greater than either the resolved $T_{w\_sys\_tx}$ value or the value requested by the receiving link partner then it enters the SYSTEM REALLOCATION state where it updates the value of resolved $T_{w\_sys\_tx}$ with NEW_TX_VALUE. The transmitting link partner enters the MIRROR UPDATE state either from the SYSTEM REALLOCATION state or directly from the TX UPDATE state. The UPDATE MIRROR state then updates the echo for the Receive $T_{w\_sys\_tx}$ and returns to the RUNNING state.

A transmitting link partner is said to be in sync with the receiving link partner if the presently advertised value of Transmit Fast_Wake_Enable and the corresponding echoed value are equal.

During normal operation, the transmitting link partner is in the RUNNING state. If the transmitting link partner wants to initiate a change to the presently resolved value of Fast_Wake_Enable, the local_system_change is asserted and the transmitting link partner enters the LOCAL CHANGE state where NEW_TX_FW is computed. If the transmitting link partner is in sync with the receiving link partner, then it enters TX UPDATE state. Otherwise, it returns to the RUNNING state.

If the transmitting link partner sees a change in the Fast_Wake_Enable requested by the receiving link partner, it recognizes the request only if it is in sync with the transmitting link partner. The transmitting link partner examines the request by entering the REMOTE CHANGE state where a NEW_TX_FW is computed and it then enters the TX UPDATE state.

Upon entering the TX UPDATE state, the transmitter updates the advertised value of Transmit Fast_Wake_Enable with NEW_TX_FW. If the NEW_TX_FW is different to either the resolved Fast_Wake_Enable value or the value requested by the receiving link partner then it enters the SYSTEM REALLOCATION state where it updates the value of resolved Fast_Wake_Enable with NEW_TX_FW. The transmitting link partner enters the MIRROR UPDATE state either from the SYSTEM REALLOCATION state or directly from the TX UPDATE state. The UPDATE MIRROR state then updates the echo for the Receive Fast_Wake_Enable and returns to the RUNNING state.

78.4.3.2 Receiving link partner's state change procedure across a link

A receiving link partner is said to be in sync with the transmitting link partner if the presently requested value of Receive $T_{w\_sys\_tx}$ and the corresponding echoed value are equal.

During normal operation, the receiving link partner is in the RUNNING state. If the receiving link partner wants to request a change to the presently resolved value of $T_{w\_sys\_tx}$, the local_system_change is asserted.

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When local_system_change is asserted or when the receiving link partner sees a change in the $T_{w\_sys\_tx}$ advertised by the transmitting link partner, it enters the CHANGE state where NEW_RX_VALUE is computed. If NEW_RX_VALUE is less than either the presently resolved value of $T_{w\_sys\_tx}$ or the presently advertised value by the transmitting link partner, it enters the SYSTEM REALLOCATION state where it updates the resolved value of $T_{w\_sys\_tx}$ to NEW_RX_VALUE. The receiving link partner ultimately enters the RX UPDATE state, either from the SYSTEM REALLOCATION state or directly from the CHANGE state.

In the RX UPDATE state, it updates the presently requested value to NEW_RX_VALUE, then it updates the echo for the Transmit $T_{w\_sys\_tx}$ in the UPDATE MIRROR state and finally goes back to the RUNNING state.

A receiving link partner is said to be in sync with the transmitting link partner if the presently requested value of Receive Fast_Wake_Enable and the corresponding echoed value are equal.

During normal operation, the receiving link partner is in the RUNNING state. If the receiving link partner wants to request a change to the presently resolved value of Fast_Wake_Enable, the local_system_change is asserted. When local_system_change is asserted or when the receiving link partner sees a change in the Fast_Wake_Enable advertised by the transmitting link partner, it enters the CHANGE state where NEW_RX_FW is computed. If NEW_RX_FW is different from either the presently resolved value of Fast_Wake_Enable or the presently advertised value by the transmitting link partner, it enters the SYSTEM REALLOCATION state where it updates the resolved value of Fast_Wake_Enable to NEW_RX_FW. The receiving link partner ultimately enters the RX UPDATE state, either from the SYSTEM REALLOCATION state or directly from the CHANGE state.

In the RX UPDATE state, it updates the presently requested value to NEW_RX_FW, then it updates the echo for the Transmit Fast_Wake_Enable in the UPDATE MIRROR state and finally goes back to the RUNNING state.

78.5 Communication link access latency

In the full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delay through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and the concatenation of devices.

The EEE capability adds latency that has to be considered by the network designer. When in the LPI mode, the PHY link is not available immediately for transmission of data. The system has to wake it up by sending the normal IDLE code on the MAC interface. Following the reception of an IDLE code on the MAC interface, the PHY starts the wake-up process. The maximal PHY recovery time, T_{w_phy} is defined for each PHY.

Transmit and/or Receive wait time shrinkage can happen when $T_{phy\_shrink\_rx}$ or $T_{phy\_shrink\_tx}$ (as defined in 78.1.3) are not zero. This has to be taken into consideration in designing or configuring the network.

Table 78–4 summarizes critical timing parameters for supported PHYs. These are listed here to assist the system designer in assessing the impact of EEE on the operation of the link.

Case-1 of the 1000BASE-T PHY applies to PHYs in Master mode. Case-2 of the 1000BASE-T PHY applies to PHYs in Slave mode.

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

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Case-1 of the 10GBASE-KR PHY applies to PHYs without FEC. Case-2 of the 10GBASE-KR PHY applies to PHYs with FEC.

Case-1 of the PHY in the MultiGBASE-T set applies when the PHY is requested to transmit the Wake signal before transmission of the Sleep signal to the Link Partner is complete. Case-2 of the PHY in the MultiGBASE-T set applies when the PHY is requested to transmit the Wake signal after transmission of the Sleep signal to the Link Partner is complete and if the PHY has not indicated LOCAL FAULT at any time during the previous 10 ms.

Case-1 of the 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, and 25GBASE-KR-S PHYs applies to PHYs in deep sleep without FEC enabled. Case-2 applies to 25GBASE-R PHYs with the BASE-R FEC in deep sleep. Case-3 applies to 25GBASE-R PHYs with the RS-FEC in deep sleep.

Case-1 of the 40GBASE-CR4, 40GBASE-KR4, and 100GBASE-CR10 PHYs applies to PHYs without FEC in deep sleep. Case-2 of these PHYs applies to PHYs with FEC in deep sleep.

Case-1 of the PHY in the MultiGBASE-T1 set applies when the PHY is requested to transmit the alert signal before transmission of the sleep signal to the link partner is complete. Case-2 of the PHY in the MultiGBASE-T1 set applies when the PHY is requested to transmit the wake signal after transmission of the sleep signal to the link partner is complete and if the PHY has not indicated LOCAL FAULT at any time during the previous 10 ms. Case-3 of the PHY in the MultiGBASE-T1 set is the same as Case-1 when Slow Wake is active. Case-4 of the PHY in the MultiGBASE-T1 set is the same as Case-2 when Slow Wake is active.

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy\_shrink\_tx}$ (max) (μs)	$T_{phy\_shrink\_rx}$ (max) (μs)	$T_{w\_sys\_rx}$ (min) (μs)
10BASE-T1L		270	250.5	10	240	20
100BASE-TX		30	20.5	5	15	10
1000BASE-KX		13.26	11.25	5	6.5	1.76
1000BASE-T1		10.8	10.8	10.8	0[a]	0[a]
1000BASE-RHC 1000BASE-RHA 1000BASE-RHB		25	25	25	0	0
1000BASE-T	Case-1	16.5	16.5	5	2.5	1.76
	Case-2	16.5	16.5	12.24	9.74	1.76
2.5GBASE-KX		13.26	11.25	5.0	6.5	1.76
2.5GBASE-T1	Case-1	35.84	35.84	25.6	0	10.24
	Case-2	25.6	25.6	15.36	0	10.24
	Case-3	148.48	148.48	138.24	0	10.24
	Case-4	138.24	138.24	128	0	10.24

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Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces *(continued)*

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy\_shrink\_tx}$ (max) (μs)	$T_{phy\_shrink\_rx}$ (max) (μs)	$T_{w\_sys\_rx}$ (min) (μs)
2.5GBASE-T	Case-1	29.44	29.44	17.92	0	11.52
	Case-2	17.92	17.92	6.4	0	11.52
5GBASE-KR		15.38	12.25	5	7.5	2.88
5GBASE-T1	Case-1	17.92	17.92	12.8	0	5.12
	Case-2	12.8	12.8	7.68	0	5.12
	Case-3	74.24	74.24	69.12	0	5.12
	Case-4	69.12	69.12	64	0	5.12
5GBASE-T	Case-1	14.72	14.72	8.96	0	5.76
	Case-2	8.96	8.96	3.2	0	5.76
XGXS (XAUI)		12.38	9.25	5	4.5	2.88
10GBASE-KX4		12.38	9.25	5	4.5	2.88
10GBASE-KR	Case-1	15.38	12.25	5	7.5	2.88
	Case-2	17.38	14.25	5	9.5	2.88
10GBASE-T1	Case-1	8.96	8.96	6.4	0	2.56
	Case-2	6.4	6.4	3.84	0	2.56
	Case-3	37.12	37.12	34.56	0	2.56
	Case-4	34.56	34.56	32	0	2.56
10GBASE-T	Case-1	7.36	7.36	4.48	0	2.88
	Case-2	4.48	4.48	1.6	0	2.88
25GBASE-R fast wake		0.34	0.3	0	0	0.25
25GAUI[b]		1				
25GBASE-KR-S 25GBASE-KR 25GBASE-CR-S 25GBASE-CR	Case-1	15.38	12.25	5	7.5	2.88
	Case-2	17.38	14.25	5	9.5	2.88
	Case-3	15.38	12.25	5	7.5	2.88
25GBASE-T	Case-1	2.56	2.56	1.792	0	0.768
	Case-2	1.792	1.792	0.64	0	0.768
40GBASE-R fast wake		0.34	0.3	0	0	0.25
XLAUI[b]		1				
40GBASE-KR4 40GBASE-CR4	Case-1	5.5	5.5	2	3	1.2
	Case-2	6.5	6.5	2	3	1.2

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Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces *(continued)*

PHY or interface type	Case	$T_{w\_sys\_tx}$ (min) (μs)	T_{w_phy} (min) (μs)	$T_{phy\_shrink\_tx}$ (max) (μs)	$T_{phy\_shrink\_rx}$ (max) (μs)	$T_{w\_sys\_rx}$ (min) (μs)
40GBASE-T	Case-1	1.6	1.6	1.12	0	0.48
	Case-2	1.12	1.12	0.4	0	0.48
50GBASE-R fast wake		0.34	0.3	0	0	0.25
100GBASE-R fast wake		0.34	0.3	0	0	0.25
CAUI-n[b]		1				
100GBASE-KR4 100GBASE-KP4 100GBASE-CR4		5.5	5.5	2	3	1
100GBASE-CR10	Case-1	5.5	5.5	2	3	1
	Case-2	7.5	7.5	2	3	1
200GBASE-R fast wake		0.34	0.3	0	0	0.25
200GXS[c]		0.34				
400GBASE-R fast wake		0.34	0.3	0	0	0.25
400GXS[c]		0.34				

[a]All data transmission in 1000BASE-T1 PHY is synchronized to the PHY frame boundary. As such, the EEE function in the 1000BASE-T1 PHY is expected to assert the wake signal only at specific moments of time, aligned to PHY frame boundaries, and no shrinkage or delay at the RX side is expected.

[b] $T_{w\_sys\_tx}$ is increased by 1 μs for each instance of 25GAUI/XLAUI/CAUI with shutdown enabled on the transmit path.The receiver should negotiate an increase for remote T_{w_sys} for the link partner of 1 μs for each instance of 25GAUI/XLAUI/CAUI with shutdown enabled on the receive path.

[c]The minimum $T_{w\_sys\_tx}$ of a PHY is increased by the indicated period if there is a 200GXS/400GXS in the transmit path. A PHY that includes a 200GXS/400GXS in the receive path may require an increase of $T_{w\_sys\_tx}$ on the link partner; this may be negotiated using LLDP (see 79.3.5).

78.5.1 PHY extension using extender sublayers

The XGXS can be inserted between the RS and a 10 Gb/s PHY to transparently extend the physical reach of the XGMII. The LPI signaling can operate through the XGXS with the LPI timing parameters modified as described below.

If the DTE XS XAUI stop enable bit (5.0.9) is asserted, the DTE XS may stop signaling on the XAUI in the transmit direction to conserve energy. If the DTE XS XAUI stop enable bit is asserted, the RS defers sending data following deassertion of LPI by an additional time equal to $T_{w\_sys\_tx} - T_{w\_sys\_rx}$ for the XGXS as shown in Table 78–4 (see 46.4.2.1).

If the PHY XS XAUI stop enable bit (4.0.9) is asserted, the PHY XS may stop signaling on the XAUI in the receive direction to conserve energy. The receiver negotiates an additional time for the remote T_{w_sys} equal

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to $T_{w\_sys\_tx} - T_{w\_sys\_rx}$ for the XGXS as shown in Table 78–4 before setting the PHY XS XAUI stop enable bit.

The 200GXS or 400GXS (see Clause 118) can be inserted between the RS and a 200 Gb/s or 400 Gb/s PHY, respectively, to transparently extend the physical reach of the 200GMII or 400GMII. The LPI signaling can operate through the 200GXS or 400GXS with the PHY timing parameters modified as described in Table 78–4.

78.5.2 25 Gb/s 40 Gb/s, and 100 Gb/s PHY extension using 25GAUI, XLAUI, or CAUI-n

25GAUI, XLAUI, CAUI-10, and CAUI-4 may be used as physical instantiations of the inter-sublayer service interface to separate functions between devices. The LPI signaling can operate through these interfaces with the LPI timing parameters modified as described below.

If PMA Egress AUI Stop Enable (PEASE, see 83.3; MDIO register bit 1.7.8) is asserted for any of the PMA sublayers, the PMA may stop signaling on the AUI in the transmit direction to conserve energy. If PEASE is asserted, the RS defers sending data following deassertion of LPI by an additional time equal to $T_{w\_sys\_tx}$ for the AUI as shown in Table 78–4 for each PMA with PEASE asserted (see 81.4.2).

If PMA Ingress AUI Stop Enable (PIASE, see 83.3; MDIO register bit 1.7.9) is asserted for any of the PMA sublayers, the PMA may stop signaling on the AUI in the receive direction to conserve energy. The receiver should negotiate an additional time for the remote T_{w_sys} equal to $T_{w\_sys\_tx}$ for the AUI as shown in Table 78–4 for each PMA with PIASE to be asserted before setting the PIASE bits.

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78.6 Protocol implementation conformance statement (PICS) proforma for EEE Data Link Layer Capabilities[141]

78.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to 78.4 shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

78.6.2 Identification

78.6.2.1 Implementation identification

Supplier[a]	
Contact point for inquiries about the PICS[a]	
Implementation Name(s) and Version(s)[a, c]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[b]	
[a]Required for all implementations [b]May be completed as appropriate in meeting the requirements for the identification. [c]The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

78.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, 78.4, EEE Data Link Layer Capabilities
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.	
Date of Statement	

[141]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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78.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*10G	Support 10G or higher operation	78.4	Support for 10 Gb/s or higher operation	O	Yes [ ] No [ ]
*40G	Support 40G or higher operation	78.4	Support for 40 Gb/s or higher operation	O	Yes [ ] No [ ]
DLL1	DLL	78.4	DLL	10G:M	Yes [ ] N/A [ ]
DLL2	DLL	78.4	DLL	!10G:O	Yes [ ] No [ ]

In addition, the following predicate name is defined for use when different implementations from the preceding set have common parameters:

DLL = DLL1 OR DLL 2

78.6.4 DLL requirements

Item	Feature	Subclause	Value/Comment	Status	Support
DLR1	Fast Wake TLV	78.4	Support EEE Fast Wake TLV defined in 79.3.6	40G:M	Yes [ ] N/A [ ]
DLR2	DLL Timing	78.4.1	Timing requirements	DLL:M	Yes [ ] N/A [ ]
DLR3	DLL Control state diagrams	78.4.2	State machines for TX and RX	DLL:M	Yes [ ] N/A [ ]

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79. IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements

79.1 Overview

The Link Layer Discovery Protocol (LLDP) specified in IEEE Std 802.1AB-2009 is a MAC Client protocol that allows stations attached to an IEEE 802 LAN to advertise to all other stations attached to the same IEEE 802 LAN: the major capabilities provided by the system incorporating that station, the management address or addresses of the entity or entities that provide management of those capabilities, and the identification of the station's point of attachment to the IEEE 802 LAN.

The information fields in each LLDP frame are contained in a Link Layer Discovery Protocol Data Unit (LLDPDU) as a sequence of short, variable length, information elements known as TLVs that each include a type, length, and value field.

Organizationally Specific TLVs can be defined by either the professional organizations or the individual vendors that are involved with the particular functionality being implemented within a system. The basic format and procedures for defining Organizationally Specific TLVs are provided in subclause 9.6 of IEEE Std 802.1AB-2009.

79.1.1 IEEE 802.3 LLDP frame format

The IEEE 802.3 LLDP frame format is illustrated in Figure 79–1.

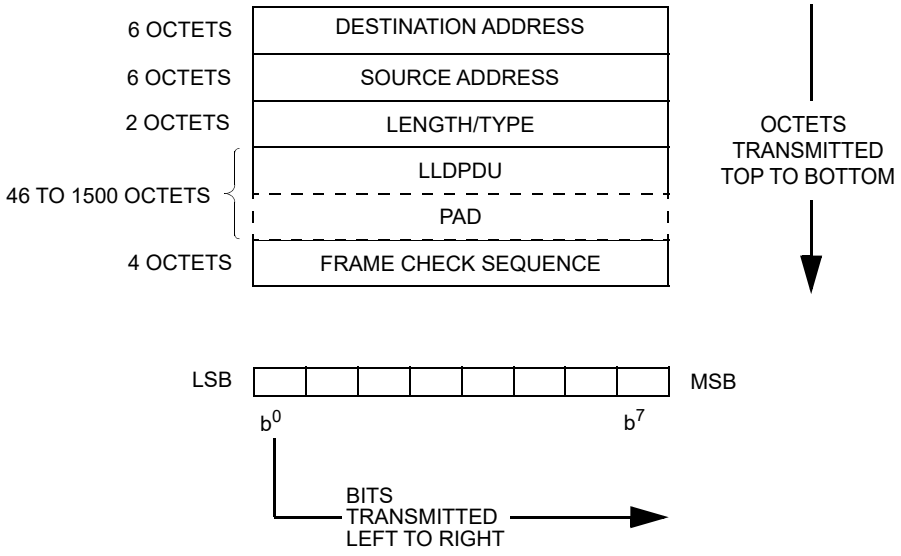

Figure 79–1—IEEE 802.3 LLDP frame format

NOTE—The illustration shows the simplest form of an IEEE 802.3 LLDP frame; i.e., where the frame has no IEEE Std 802.1Q™ tag header, or IEEE Std 802.1AE™ security tag, or any other form of encapsulation applied to it.

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79.1.1.1 Destination Address field

The Destination Address field of an IEEE 802.3 LLDP frame contains a MAC address specified by 7.1 of IEEE Std 802.1AB-2009 (see 79.2).

79.1.1.2 Source Address field

The Source Address field of an IEEE 802.3 LLDP frame contains the 48-bit individual address of the station sending the frame.

79.1.1.3 Length/Type field

The Length/Type field of an IEEE 802.3 LLDP frame is a 2-octet field that contains 0x88CC. This value carries the Type interpretation (see 3.2.6) and has been universally assigned for LLDP.

79.1.1.4 LLDPDU field

The LLDPDU field of an IEEE 802.3 LLDP frame contains the LLDPDU which is a sequence of short, variable length, information elements known as TLVs that each include type, length, and value fields.

79.1.1.5 Pad field

A minimum MAC frame size is required for correct operation and, if necessary, a Pad field is appended after the LLDPDU field as defined in 3.2.8.

79.1.1.6 Frame Check Sequence field

The Frame Check Sequence (FCS) field contains the Frame Check Sequence, as defined in 3.2.9.

79.2 Requirements of the IEEE 802.3 Organizationally Specific TLV set

All IEEE 802.3 Organizationally Specific TLVs shall conform to the LLDPDU bit and octet ordering conventions of 8.1 of IEEE Std 802.1AB-2009.

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79.3 IEEE 802.3 Organizationally Specific TLVs

The currently defined IEEE 802.3 Organizationally Specific TLVs are listed in Table 79–1. Any additions or changes to these TLVs will be included in this clause.

Table 79–1—IEEE 802.3 Organizationally Specific TLVs

IEEE 802.3 subtype	TLV name	Subclause reference
1	MAC/PHY Configuration/Status	79.3.1
2	Power Via Medium Dependent Interface (MDI)	79.3.2
3	Link Aggregation (deprecated)	79.3.3
4	Maximum Frame Size	79.3.4
5	Energy-Efficient Ethernet	79.3.5
6	EEE fast wake	79.3.6
7	Additional Ethernet Capabilities	79.3.7
8	Power Via MDI Measurements	79.3.8
9 to 255	Reserved	—

79.3.1 MAC/PHY Configuration/Status TLV

The MAC/PHY Configuration/Status TLV is an optional TLV that identifies the following:

a) The duplex and bit-rate capability of the sending IEEE 802.3 LAN node that is connected to the physical medium.
b) The current duplex and bit-rate settings of the sending IEEE 802.3 LAN node.
c) Whether the current duplex and bit-rate settings are the result of auto-negotiation during link initiation or of manual set override action.

Figure 79–2 shows the format of this TLV.

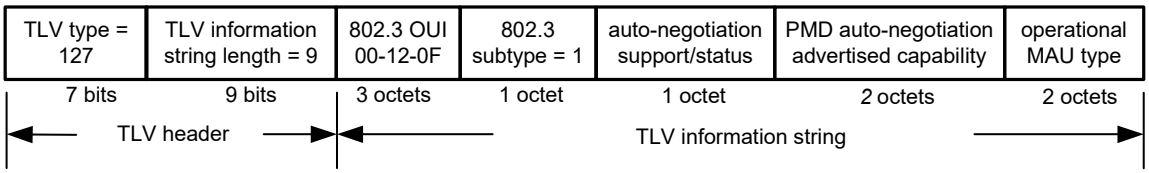

Figure 79–2—MAC/PHY configuration/status TLV format

79.3.1.1 Auto-negotiation support/status

The auto-negotiation support/status field shall contain a bitmap that identifies the auto-negotiation support and current status of the local IEEE 802.3 LAN station as defined in Table 79–2. If the auto-negotiation support bit (bit 0) is one and the auto-negotiation status bit (bit 1) is zero, the IEEE 802.3 physical media dependent sublayer (PMD) operating mode is determined by the operational Medium Attachment Unit (MAU) type field value rather than by auto-negotiation.

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Table 79–2—IEEE 802.3 auto-negotiation support/status

Bit	Function	Value/meaning	IETF RFC 4836 reference
0	Auto-negotiation support	1 = supported 0 = not supported	ifMauAutoNegSupported
1	Auto-negotiation status	1 = enabled 0 = not enabled	ifMauAutoNegAdminStatus
7:2	—	Reserved for future standardization	—

79.3.1.2 PMD auto-negotiation advertised capability field

The ‘PMD auto-negotiation capability’ field shall contain a 2-octet value that provides a bitmap of the ifMauAutoNegCapAdvertisedBits object, defined in IETF RFC 4836, of the sending device. Bit zero is the high order (left-most) bit in an octet string.

79.3.1.3 Operational MAU type

The operational MAU type field contains an integer value indicating the MAU type of the sending device. This value shall be derived from the list position of the corresponding dot3MauType as listed in IETF RFC 4836 (or subsequent revisions) and is equal to the last number in the respective dot3MauType Object Identifier (OID). For example, if the ifMauType object is dot3MauType1000BaseTHD which corresponds to {dot3MauType 29}, the numerical value of this field is 29. For MAU types not listed in IETF RFC 4836 (or subsequent revisions), the value of this field shall be set to zero.

79.3.1.4 MAC/PHY Configuration/Status TLV usage rules

An LLDPDU should contain no more than one MAC/PHY Configuration/Status TLV.

79.3.2 Power Via MDI TLV

Clause 33 and Clause 145 define two optional power entities: a Powered Device (PD) and Power Sourcing Equipment (PSE). These entities allow devices to draw/supply power over the sample generic cabling as used for data transmission. The Power Via MDI TLV allows network management to advertise and discover the Power over Ethernet capabilities of the sending IEEE 802.3 LAN station. This TLV is also required to perform Data Link Layer classification as defined in 33.6 and 145.5. Figure 79–3 shows the format of this TLV.

The Power via MDI TLV shown in Figure 79–3 was originally defined in IEEE Std 802.1AB-2005 Annex G.3. This original TLV supported only the first three fields of Figure 79–3, labeled basic fields, enabling discovery and advertisement of Power via MDI capabilities. The Power via MDI TLV was revised by IEEE Std 802.3at-2009 to add a further three fields, labeled DLL classification extension, to provide Data Link Layer (DLL) classification capabilities. The Power via MDI TLV was revised again by IEEE Std 802.3bt-2018 to add a further nine fields, labeled Type 3 and Type 4 extension, to support additional capabilities offered by Type 3 and Type 4 PSEs and PDs.

Power entities may continue to use the Power Via MDI TLV basic fields shown in Figure 79–3 prior to supplying/drawing power to/from the Power Interface (PI), as defined in 1.4.484. The DLL classification extension fields and Type 3 and Type 4 extension fields shown in Figure 79–3 shall not be sent by the PSE unless it is supplying power to a PI encompassed within an MDI and by the PD unless it is drawing power from the PI.

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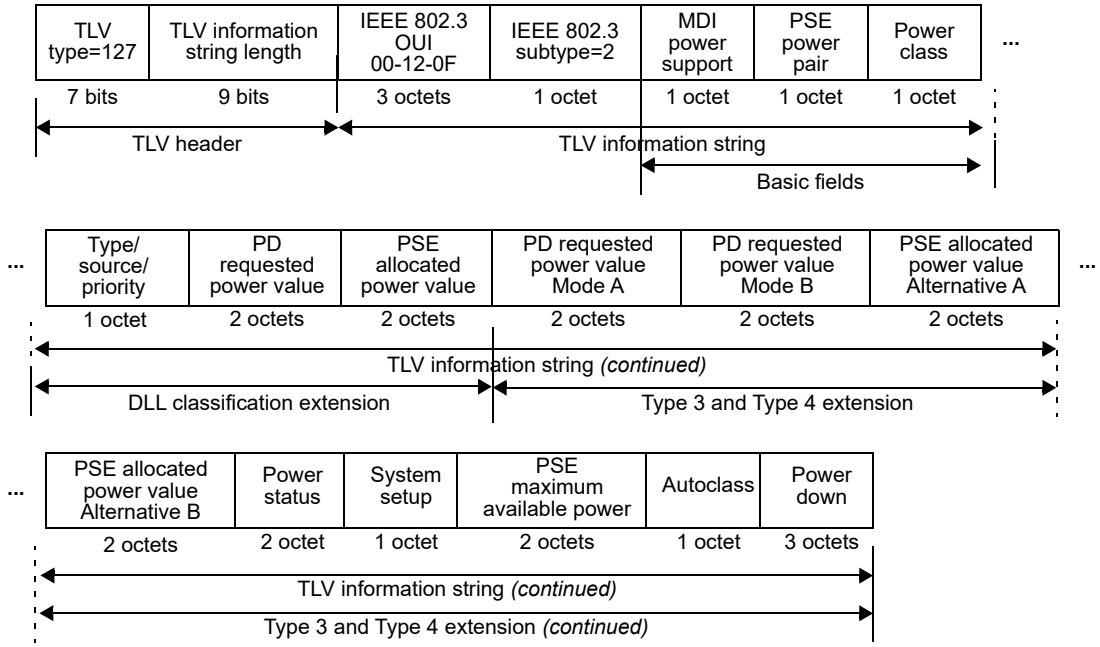

The TLV information string length is

- Basic fields: 7 octets
- Basic fields and DLL classification extension: 12 octets
- Basic fields, DLL classification extension, and Type 3 and Type 4 extension: 29 octets

Figure 79–3—Power Via MDI TLV format

Power entities that implement Data Link Layer classification shall support the Power via MDI TLV DLL classification extension fields shown in Figure 79–3 after the PI has been powered. Type 3 or Type 4 power entities that implement Data Link Layer classification and are connected to another Type 3 or Type 4 power entity shall support the Type 3 and Type 4 extension fields shown in Figure 79–3 after the PI has been powered. Such entities, when connected to a Type 1 or Type 2 power entity, may support the Type 3 and Type 4 extension fields shown in Figure 79–3 after the PI has been powered. Type 1 and Type 2 devices shall not include the Type 3 and Type 4 extension fields in the transmitted Power via MDI TLV.

NOTE—Some implementations of the Power via MDI TLV in Type 1 and Type 2 power entities ignore TLVs that are longer than 12 octets. In order to be interoperable with these implementations, Type 3 and Type 4 power entities are permitted to transmit 12-octet TLVs (without the Type 3 and Type 4 extension) after first transmitting at least one valid 29-octet TLV (including the Type 3 and Type 4 extension). Table 79–3 lists the recommended Power via MDI TLV formats for each combination of power entity Types.

Type 3 and Type 4 PD power entities can determine the PSE Type based on the duration of the first classification event (see 145.3.7) or based on the length of a received Power via MDI TLV (see Figure 79–3). Type 3 and Type 4 PSEs can determine the PD Type based on the PDs Physical Layer requested Class (see 145.2.8 and 145.3.6.1) or based on the length of a received Power via MDI TLV (see Figure 79–3).

79.3.2.1 MDI power support

The MDI power support field shall contain a bitmap of the MDI power capabilities and status as defined in Table 79–4.

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Table 79–3—Recommended TLV format

Power entity A	Power entity B	Power entity A sends	Power entity B sends	Recommended TLV format
Type 1, Type 2	Type 1, Type 2	12-octet TLV	12-octet TLV	12-octet TLV
Type 3, Type 4	Type 1, Type 2	29-octet TLV	12-octet TLV	12-octet TLV
Type 1, Type 2	Type 3, Type 4	12-octet TLV	29-octet TLV	12-octet TLV
Type 3, Type 4	Type 3, Type 4	29-octet TLV	29-octet TLV	29-octet TLV

Table 79–4—MDI power support field

Bit	Function	Value/meaning
7:4	Reserved for future standardization	—
3	PSE pairs control ability	1 = pair selection can be controlled 0 = pair selection can not be controlled
2	PSE MDI power state	1 = enabled 0 = disabled
1	PSE MDI power support	1 = supported 0 = not supported
0	Port class	1 = PSE 0 = PD

79.3.2.1.1 Port class

The ‘Port class’ field transmitted shall indicate if the port is a PSE or a PD.

79.3.2.1.2 PSE MDI power support

The ‘PSE MDI power support’ field transmitted by a PSE shall indicate if MDI power is supported. The value of the ‘PSE MDI power support’ field transmitted by a PD is undefined.

79.3.2.1.3 PSE MDI power state

The ‘PSE MDI power state’ field transmitted by a PSE shall indicate if the PSE function is enabled or disabled. When disabled all PSE functions are disabled and behavior is as if there was no PSE functionality. The value of the ‘PSE MDI power state’ field transmitted by a PD is undefined.

79.3.2.1.4 PSE pairs control ability

The ‘PSE pairs control ability’ field transmitted by a PSE shall indicate if the PSE has the capability to control which PSE Pinout Alternative (see 33.2.3 and 145.2.4) is used for PD detection and power. The value of the ‘PSE pairs control ability’ field transmitted by a PD is undefined.

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79.3.2.2 PSE power pair

The ‘PSE power pair’ field transmitted by a PSE shall contain an integer value as defined in Table 79–5 based on aPSEPowerPairs (see 30.9.1.1.4). A Type 3 or Type 4 PSE that is supplying power on a single pairset shall use the value that defines that pairset. Either pairset may be indicated when a PSE is detecting or supplying power on both pairsets. The ‘PSE power status value’ field defined in 79.3.2.9 indicates when a PSE is supplying power on both pairsets. The value of the ‘PSE power pair’ field transmitted by a PD is undefined.

Table 79–5—PSE power pair field

Value	Meaning	Alternative
1	signal	Alternative A
2	spare	Alternative B

79.3.2.3 Power class

The ‘Power class’ field transmitted by a PSE shall contain an integer value as defined in Table 79–6 based on aPSEPowerClassification (see 30.9.1.1.8). Class 4 and above is indicated with the same value in this field. Class 5 and above is communicated by the ‘Power Class ext’ field defined in 79.3.2.9.6. The ‘Power class’ field transmitted by a PD is undefined.

Table 79–6—Power class field

Value	Meaning
1	Class 0 PD
2	Class 1 PD
3	Class 2 PD
4	Class 3 PD
5	Class 4 and above PD

79.3.2.4 Power type/source/priority

The ‘Power type/source/priority’ field shall contain a bit-map of the power type, source, and priority defined in Table 79–7 and is reported for the device generating the TLV.

79.3.2.4.1 Power type

This field shall be set according to Table 79–7. Type 3 or Type 4 PSEs shall set this field to the value corresponding with Type 2 PSEs. Type 3 or Type 4 PDs shall set this field to the value corresponding with Type 2 PDs.

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Table 79–7—Power type/source/priority field

Bit	Function	Value/meaning
7:6	Power type	7 6 1 1 = Type 1 PD 1 0 = Type 1 PSE 0 1 = Type 2 PD 0 0 = Type 2 PSE
5:4	Power source	Where Power type = PD 5 4 1 1 = PSE and local 1 0 = Reserved 0 1 = PSE 0 0 = Unknown Where Power type = PSE 5 4 1 1 = Reserved 1 0 = Backup source 0 1 = Primary power source 0 0 = Unknown
3	Reserved	Transmit as zero, ignore on receive
2	PD 4PID	1 = PD supports powering of both Modes simultaneously 0 = PD does not support powering of both Modes simultaneously
1:0	Power priority	1 0 1 1 = low 1 0 = high 0 1 = critical 0 0 = unknown (default)

79.3.2.4.2 Power source

When the power type is PD, this field shall be set to 01 when the PD is being powered only through the PI; to 11 when the PD is being powered from both; and to 00 when this information is not available.

When the power type is PSE, this field shall be set to 01 when the PSE is sourcing its power through the PI from its primary supply; to 10 when the PSE is sourcing its power through the PI from a backup source; and to 00 when this information is not available.

79.3.2.4.3 PD 4PID

This field shall be set according to Table 79–7 when the Power type is PD to indicate whether the PD supports powering of both Modes simultaneously. This field shall be set to ‘0’ when the Power type is PSE.

79.3.2.4.4 Power priority

When the power type is PD, this field shall be set to the power priority configured for the device. If a PD is unable to determine its power priority or it has not been configured, then this field shall be set to 00.

When the power type is PSE, this field reflects the PD priority that the PSE advertises to assign to the PD.

79.3.2.5 PD requested power value

The ‘PD requested power value’ field shall contain the PD’s requested power value defined in Table 79–8. See 33.6.3.3 and Table 145–42 for permitted value ranges.

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Table 79–8—PD requested power value field

Bit	Function	Value/meaning
15:0	PD requested power value	Power expressed in units of 0.1 W Valid values for these bits are decimal 0 through 999.

"PD requested power value" is the maximum input average power (see 33.3.7.2 and 145.3.8.2) the PD is requesting. "PD requested power value" is the power value at the PD PI. A value higher than 713 requires the PSE to support a power level higher than P_{Class_PD} at the PD PI. See 145.2.8 and 145.3.8.2.

79.3.2.6 PSE allocated power value

The 'PSE allocated power value' field shall contain the PSE allocated power value defined in Table 79–9. See 33.6.3.3 and Table 145–41 for permitted value ranges.

Table 79–9—PSE allocated power value field

Bit	Function	Value/meaning
15:0	PSE allocated power value	Power expressed in units of 0.1 W Valid values for these bits are decimal 0 through 999.

"PSE allocated power value" is the maximum input average power (see 33.3.7.2 and 145.3.8.2) the PSE expects the PD to draw. "PSE allocated power value" is the power at the PD PI. The PSE uses this value to compute P_{Class} as defined in 33.2.6 and 145.2.8. A value higher than 713 indicates that the PSE is capable of supporting a power level beyond P_{Class_PD} at the PD PI. This may require an output power level higher than P_{Type} min. See 145.2.8.

79.3.2.7 Dual-signature PD requested power value for Mode A and Mode B

The 'PD requested power value Mode A' field and 'PD requested power value Mode B' field shall contain the PD requested power value defined in Table 79–10 for Mode A and in Table 79–11 for Mode B of a dual-signature PD.

Table 79–10—PD requested power value Mode A field

Bit	Function	Value/meaning
15:0	Dual-signature PD requested power value for Mode A	Power expressed in units of 0.1 W. Valid values for these bits are decimal 0 through 499.

Table 79–11—PD requested power value Mode B field

Bit	Function	Value/meaning
15:0	Dual-signature PD requested power value for Mode B	Power expressed in units of 0.1 W. Valid values for these bits are decimal 0 through 499.

The 'PD requested power value Mode A' field and 'PD requested power value Mode B' field are the maximum input average power levels (see 145.3.8.2) the PD is requesting for the respective Mode.

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79.3.2.8 PSE allocated power value Alternative A and Alternative B

The ‘PSE allocated power value Alternative A’ field and the ‘PSE allocated power value Alternative B’ field shall contain the values in Table 79–12 and Table 79–13 for Type 3 and Type 4 PSEs operating over both pairsets when connected to a dual-signature PD.

Table 79–12—PSE allocated power value Alternative A field

Bit	Function	Value/meaning
15:0	PSE allocated power value for Alternative A	Power expressed in units of 0.1 W. Valid values for these bits are decimal 0 through 499.

Table 79–13—PSE allocated power value Alternative B field

Bit	Function	Value/meaning
15:0	PSE allocated power value for Alternative B	Power expressed in units of 0.1 W. Valid values for these bits are decimal 0 through 499.

The ‘PSE allocated power value Alternative A’ and ‘PSE allocated power value Alternative B’ fields are the maximum input average power levels (see 145.3.8.2) the PSE expects the dual-signature PD to draw on the respective Alternatives when the PSE provides power over 4-pair. These fields are the power levels at the dual-signature PD PI. The PSE uses these values to compute $P_{Class\text{-}2P}$ as defined in 145.2.8.

79.3.2.9 Power status

The ‘Power status’ field contains the PSE's bit-map of the PSE power pair and PSE or PD power class, defined in Table 79–14, and is reported for the device generating the TLV.

Table 79–14—Power status field

Bit	Function	Value/meaning
15:14	PSE powering status	15 14 1 1 = 4-pair powering dual-signature PD 1 0 = 4-pair powering single-signature PD 0 1 = 2-pair powering 0 0 = Reserved/Ignore
13:12	PD powered status	13 12 1 1 = 4-pair powered dual-signature PD 1 0 = 2-pair powered dual-signature PD 0 1 = Powered single-signature PD 0 0 = Reserved/Ignore
11:10	PSE power pairs ext	11 10 1 1 = Both Alternatives 1 0 = Alternative B 0 1 = Alternative A 0 0 = Reserved/Ignore

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Table 79–14—Power status field *(continued)*

Bit	Function	Value/meaning
9:7	Dual-signature power Class ext Mode A	9 8 7 1 1 1 = Single-signature PD or 2-pair only PSE 1 1 0 = Reserved/Ignore 1 0 1 = Class 5 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Reserved/Ignore
6:4	Dual-signature power Class ext Mode B	6 5 4 1 1 1 = Single-signature PD or 2-pair only PSE 1 1 0 = Reserved/Ignore 1 0 1 = Class 5 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Reserved/Ignore
3:0	Power Class ext	3 2 1 0 1 1 1 1 = Dual-signature PD 1 1 1 0 = Reserved/Ignore 1 1 0 1 = Reserved/Ignore 1 1 0 0 = Reserved/Ignore 1 0 1 1 = Reserved/Ignore 1 0 1 0 = Reserved/Ignore 1 0 0 1 = Reserved/Ignore 1 0 0 0 = Class 8 0 1 1 1 = Class 7 0 1 1 0 = Class 6 0 1 0 1 = Class 5 0 1 0 0 = Class 4 0 0 1 1 = Class 3 0 0 1 0 = Class 2 0 0 0 1 = Class 1 0 0 0 0 = Reserved/Ignore

79.3.2.9.1 PSE powering status

The ‘PSE powering status’ field is used to indicate the existing powering configuration as shown in Table 145–41 and thus to indicate that the PSE is using the ‘PSE allocated power value’ field or is using the ‘PSE allocated power value Alternative A’ field and ‘PSE allocated power value Alternative B’ field as specified in Table 79–12 and Table 79–13. A PSE shall set this field according the current powering status as defined in Table 79–14. A PD shall set the field to 0.

79.3.2.9.2 PD powered status

The ‘PD powered status’ field is used to indicate the existing powered configuration of the PD as shown in Table 145–42 and thus to indicate that the PD is using the ‘PD requested power value’ field or is using the ‘PD requested power value Mode A’ field and the ‘PD requested power value Mode B’ field as specified in Table 79–10 and Table 79–11. A PD shall set this field according to its signature configuration and the current powering status as defined in Table 79–14. A PSE shall set the field to 0.

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79.3.2.9.3 PSE power pairs ext

The ‘PSE power pairs ext’ field shall contain the powering status of the PSE, as defined in Table 79–14. A PD shall set the field to 0.

79.3.2.9.4 Dual-signature power Class ext Mode A

A single-signature PD shall set this field to value 7. A dual-signature PD shall set this field per its requested Class on Mode A defined in 145.3.6. A 2-pair only PSE or a PSE connected to a single-signature PD shall set this field to value 7. A PSE connected to a dual-signature PD shall set this field to the PSEs assigned Class for Alternative A as defined in 145.2.8.

79.3.2.9.5 Dual-signature power Class ext Mode B

A single-signature PD shall set this field to value 7. A dual-signature PD shall set this field per its requested Class on Mode B defined in 145.3.6. A 2-pair only PSE or a PSE connected to a single-signature PD shall set this field to value 7. A PSE connected to a dual-signature PD shall set this field to the PSEs assigned Class for Alternative B as defined in 145.2.8.

79.3.2.9.6 Power Class ext

A single-signature PD shall set this field per its requested Class as defined in 145.3.6. A dual-signature PD shall set this field to value 15. A 2-pair only PSE or a PSE connected to a single-signature PD shall set this field to the PSEs assigned Class as defined in 145.2.8. A PSE connected to a dual-signature PD shall set this field to value 15.

79.3.2.10 System setup

The ‘System setup’ field shall contain the device bit-map of the Power Type ext and PD Load defined in Table 79–15 and is reported for the device generating the TLV.

Table 79–15—System setup field

Bit	Function	Value/meaning
7:4	Reserved	Transmit as zero. Ignore on receive.
3:1	Power Type ext	3 2 1 1 1 1 = Reserved / ignore 1 1 0 = Reserved / ignore 1 0 1 = Type 4 dual-signature PD 1 0 0 = Type 4 single-signature PD 0 1 1 = Type 3 dual-signature PD 0 1 0 = Type 3 single-signature PD 0 0 1 = Type 4 PSE 0 0 0 = Type 3 PSE
0	PD Load	1 = PD is dual-signature and power demand on Mode A and Mode B are electrically isolated. 0 = PD is single-signature or dual-signature and power demand on Mode A and Mode B are not electrically isolated.

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79.3.2.10.1 Power Type ext

This field shall be set according to Table 79–15.

79.3.2.10.2 PD Load

This field shall be set according to Table 79–15 when the Power type is PD. This field shall be set to 0 when the Power type is PSE. See 145.4.1 for details.

79.3.2.11 PSE maximum available power value

The ‘PSE maximum available power value’ field shall contain the highest power the PSE can grant as defined in Table 79–16. The PSE sets the value of this field taking available power budget and hardware capabilities into account. When connected to a dual-signature PD this value refers to the total amount of power available at the PI, even though power is allocated separately on a per pairset basis. A PD shall set this field to 0.

Table 79–16—PSE maximum available power value field

Bit	Function	Value/meaning
15:0	PSE maximum available power value	Power expressed in units of 0.1 W. Valid values for these bits are 1 through 999.

79.3.2.12 Autoclass

The ‘Autoclass’ field shall contain the bits defined in Table 79–17 to control Autoclass. See 145.2.8.2 and 145.3.6.2 for details on Autoclass. Using the ‘Autoclass’ field to trigger a new Autoclass measurement allows a PD to change maximum power consumption.

Table 79–17—Autoclass field

Bit	Function	Value/meaning
7:3	Reserved	Transmit as zero. Ignore on receive.
2	PSE Autoclass support	1 = PSE supports Autoclass 0 = PSE does not support Autoclass
1	Autoclass completed	1 = Autoclass measurement completed 0 = Autoclass idle
0	Autoclass request	1 = PD requests Autoclass measurement 0 = Autoclass idle

79.3.2.12.1 PSE Autoclass support

When the Power type is PSE, this field shall be set to indicate if the PSE supports Autoclass over DLL according to Table 79–17. When the Power type is PD, this field shall be set to 0.

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79.3.2.12.2 Autoclass completed

When the Power type is PSE, this field shall be set to indicate that the PSE has concluded the Autoclass measurement. This happens after a request for Autoclass is made by the PD using the 'Autoclass request' field defined in Table 79–17. When the Power type is PD, this field shall be set to 0.

79.3.2.12.3 Autoclass request

When the Power type is PD, this field may be set to 1 to request a Autoclass measurement by the PSE. The PD sets this field when it is in a state where it consumes its maximum amount of power. In all other cases, the PD sets this field to 0. When the Power type is PSE, this field shall be set to 0.

79.3.2.13 Power down

The 'Power down' field shall contain the bits defined in Table 79–18. The 'Power down' field allows the PD to request power delivery to be terminated, either indefinitely or for a certain period of time.

Table 79–18—Power down field

Bit	Function	Value/meaning
23:18	Power down request	Value = 0x1D requests a power down. Any other value is ignored.
17:0	Power down time	The amount of time in seconds the PD requests to be unpowered. A value of zero means to remain unpowered indefinitely. Valid values are 0 through 262 143.

79.3.2.13.1 Power down request

When the Power type is PD, this field may be set to 0x1D to indicate a request for power down. If power is to be maintained, the field shall be set to 0. When the Power type is PSE, this field shall be set to 0.

79.3.2.13.2 Power down time

This field controls the amount of time in seconds the PD is requesting to be unpowered. When the Power type is PD, this field shall be set per the description in Table 79–18. When the Power type is PSE, this field shall be set to 0.

79.3.2.14 Power Via MDI TLV usage rules

An LLDPDU should contain no more than one Power Via MDI TLV.

79.3.3 Link Aggregation TLV (deprecated)

The Link Aggregation TLV is an optional TLV that indicates whether the link is capable of being aggregated, whether the link is currently in an aggregation, and if in an aggregation, the port identification of the aggregation. Figure 79–4 shows the format for this TLV.

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NOTE—As the Link Aggregation specification has now been removed from IEEE Std 802.3 and is now standardized as IEEE Std 802.1AX, new implementations of this standard are encouraged to make use of the Link Aggregation TLV that is now part of the IEEE 802.1 extension MIB specified in Annex E of IEEE Std 802.1AB-2009.

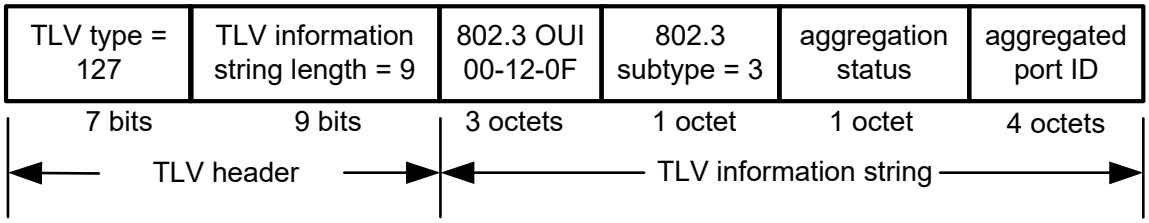

Figure 79–4—Link Aggregation TLV format

79.3.3.1 Aggregation status

The link aggregation status field shall contain a bitmap of the link aggregation capabilities and the current aggregation status of the link as defined in Table 79–19.

Table 79–19—Link aggregation capability/status

Bit	Function	Value/meaning
0	Aggregation capability	0 = not capable of being aggregated 1 = capable of being aggregated
1	Aggregation status	0 = not currently in aggregation 1 = currently in aggregation
7:2	reserved for future standardization	—

79.3.3.2 Aggregated port ID

The aggregated port ID field shall contain the IEEE 802.3 aggregated port identifier, aAggPortID, derived from the ifNumber in the ifIndex for the interface (see 30.7.2.1.1).

79.3.3.3 Link Aggregation TLV usage rules

An LLDPDU should contain no more than one Link Aggregation TLV.

79.3.4 Maximum Frame Size TLV

The Maximum Frame Size TLV is an optional TLV that indicates the maximum frame size capability of the implemented MAC and PHY. Figure 79–5 shows the format of this TLV.

NOTE—MAC and PHY support for a given frame size doesn't necessarily mean that the upper layers support that frame size.

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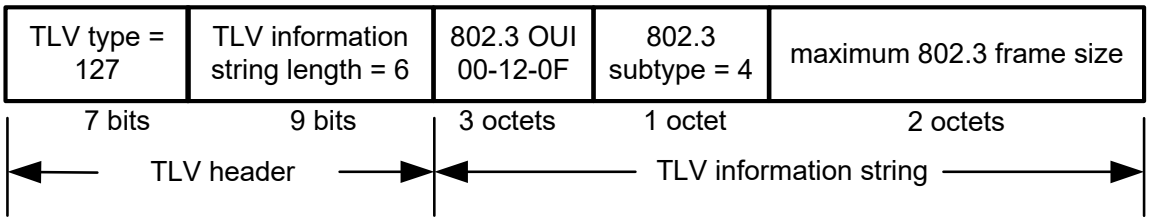

Figure 79–5—Maximum Frame Size TLV format

79.3.4.1 Maximum frame size

The maximum frame size field shall contain an integer value indicating the maximum supported frame size in octets as determined by the following:

a) If the MAC/PHY supports only basic frames (see 3.2.7) the maximum frame size field shall be set to 1518.
b) If the MAC/PHY supports Q-tagged frames (see 3.2.7) the maximum frame size field shall be set to 1522.
c) If the MAC/PHY supports envelope frames (see 3.2.7) the maximum frame size field shall be set to 2000.

79.3.4.2 Maximum Frame Size TLV usage rules

An LLDPDU should contain no more than one Maximum Frame Size TLV.

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79.3.5 EEE TLV

The EEE TLV is used to exchange information about the EEE Data Link Layer capabilities. Figure 79–6 shows the format of this TLV.

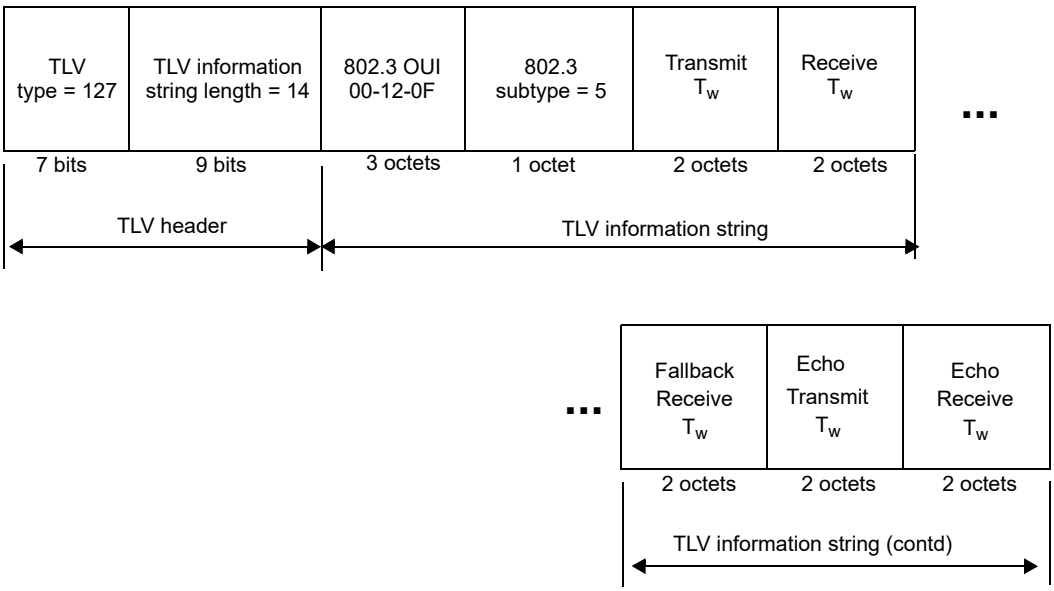

Figure 79–6—EEE TLV format

79.3.5.1 Transmit T_w

Transmit $T_{w\_sys\_tx}$ (2 octets wide) shall be defined as the time (expressed in microseconds) that the transmitting link partner will wait before it starts transmitting data after leaving the Low Power Idle (LPI) mode. This is a function of the transmit system design and may be constrained, for example, by the transmit path buffering. The default value for Transmit $T_{w\_sys\_tx}$ is the T_{w_phy} defined for the PHY that is in use for the link. The Transmitting link partner expects that the Receiving link partner will be able to accept data after the time delay Transmit $T_{w\_sys\_tx}$ (expressed in microseconds).

79.3.5.2 Receive T_w

Receive $T_{w\_sys\_tx}$ (2 octets wide) shall be defined as the time (expressed in microseconds) that the receiving link partner is requesting the transmitting link partner to wait before starting the transmission data following the LPI. The default value for Receive $T_{w\_sys\_tx}$ is the T_{w_phy} defined for the PHY that is in use for the link. The Receive $T_{w\_sys\_tx}$ value can be larger but not smaller than the default. The extra wait time may be used by the receive link partner for power-saving mechanisms that require a longer wake-up time than the PHY-layer definitions.

79.3.5.3 Fallback T_w

A receiving link partner may inform the transmitter of an alternate desired $T_{w\_sys\_tx}$. Since a receiving link partner is likely to have discrete levels for savings, this provides the transmitter with additional information that it may use for a more efficient allocation. As with the Receive $T_{w\_sys\_tx}$, this is 2 octets wide. Systems that do not implement this option default the value to be the same as that of the Receive $T_{w\_sys\_tx}$.

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79.3.5.4 Echo Transmit and Receive T_W

The respective echo values shall be defined as the local link partner's reflection (echo) of the remote link partner's respective values. When a local link partner receives its echoed values from the remote link partner it can determine whether or not the remote link partner has received, registered, and processed its most recent values. For example, if the local link partner receives echoed parameters that do not match the values in its local MIB, then the local link partner infers that the remote link partner's request was based on stale information.

79.3.5.5 EEE TLV usage rules

An LLDPDU should contain no more than one EEE TLV.

79.3.6 EEE Fast Wake TLV

The EEE Fast Wake TLV is used to exchange information about the EEE fast wake capabilities. This TLV is only used by systems with links operating at speeds greater than 10 Gb/s. Figure 79–7 shows the format of this TLV.

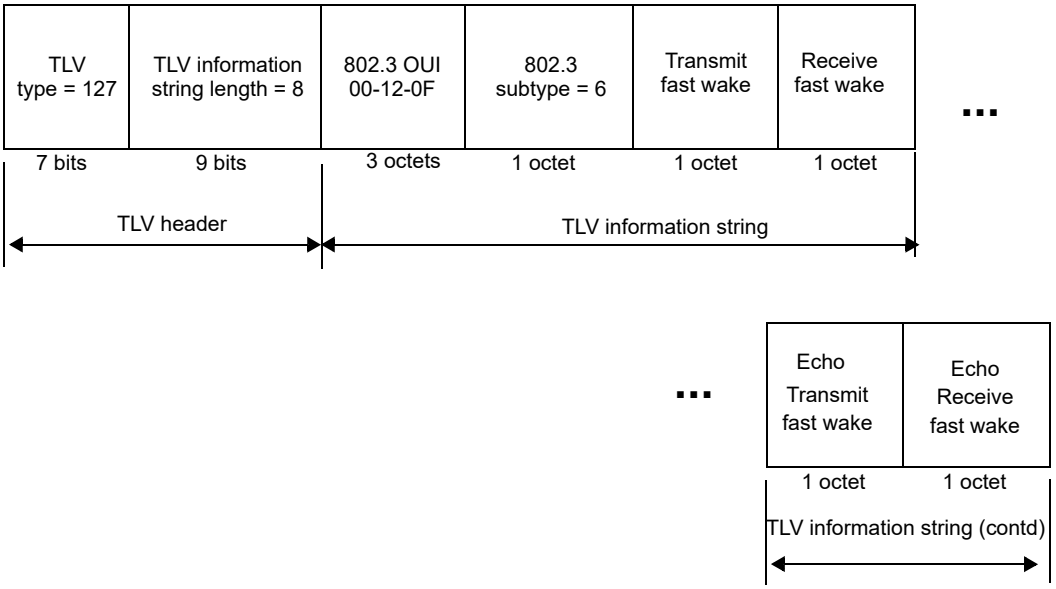

Figure 79–7—EEE Fast Wake TLV format

79.3.6.1 Transmit fast wake

Transmit fast wake (1 octet wide) is a logical indication that the transmit LPI state diagram intends to use the fast wake function (corresponding to the variable LPI_FW in 82.2.19.2.2). Transmit fast wake = 1 corresponds to LPI_FW being TRUE; Transmit fast wake = 0 corresponds to LPI_FW being FALSE. The default value for Transmit fast wake is 1 (TRUE). Transmit fast wake is set to TRUE unless the PHY is capable of deep sleep operation as determined by the PHY type and the results of auto-negotiation.

79.3.6.2 Receive fast wake

Receive fast wake (1 octet wide) is a logical indication that the receive LPI state diagram is expecting its link partner to use the fast wake function (corresponding to the variable LPI_FW in 82.2.19.2.2). Receive fast

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wake = 1 corresponds to LPI_FW being TRUE; Receive fast wake = 0 corresponds to LPI_FW being FALSE. The default value for Receive fast wake is 1 (TRUE). Receive fast wake is set to TRUE unless the PHY is capable of deep sleep operation as determined by the PHY type and the results of auto-negotiation.

79.3.6.3 Echo of Transmit fast wake and Receive fast wake

The respective echo values are the local link partner's reflection (echo) of the remote link partner's respective values. When a local link partner receives its echoed values from the remote link partner, it can determine whether or not the remote link partner has received, registered, and processed its most recent values. For example, if the local link partner receives echoed parameters that do not match the values in its local MIB, then the local link partner infers that the remote link partner's request was based on stale information.

79.3.6.4 EEE Fast Wake TLV usage rules

An LLDPDU should contain no more than one EEE Fast Wake TLV.

79.3.7 Additional Ethernet Capabilities TLV

The Additional Ethernet Capabilities TLV is an optional TLV that indicates which additional capabilities are supported. Figure 79–8 shows the format of this TLV.

NOTE—MAC and PHY support for a given frame size does not necessarily mean that the upper layers support that frame size.

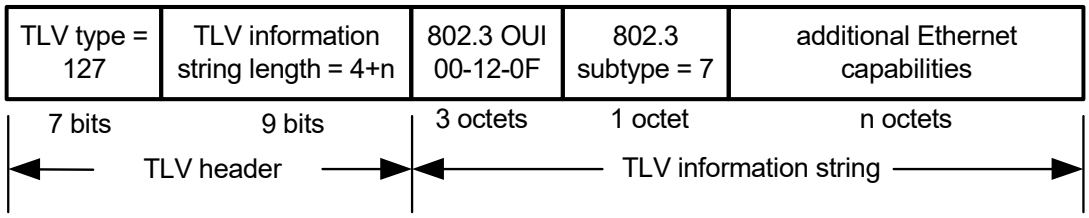

Figure 79–8—Additional Ethernet Capabilities TLV

79.3.7.1 Additional Ethernet capabilities

The additional Ethernet capabilities field shall contain a bitmap that identifies the support and current status of additional Ethernet capabilities on the local IEEE 802.3 LAN station. The first two octets of the field are defined in Table 79–20. Additional octets are reserved.

An implementation shall transmit all Reserved bits as zero and ignore received Reserved bits. Reserved octets shall not be transmitted and if more octets are received than were defined as other than Reserved, the additional octet(s) shall be ignored. If fewer octet(s) are received than defined, the implementation shall act as if the additional octet(s) were received as zero.

79.3.7.2 Additional Ethernet Capabilities TLV usage rules

An LLDPDU should contain no more than one Additional Ethernet Capabilities TLV. Since this TLV is intended to inform a link partner of capabilities, the Additional Ethernet Capabilities TLV should be sent in an LLDPDU addressed to the Nearest Bridge group address (see IEEE Std 802.1Q).

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Table 79–20—Additional Ethernet capabilities

Bit	Function	Value/meaning	Reference
0	preemption capability support	1 = supported 0 = not supported	99.4.2
1	preemption capability status	1 = enabled 0 = not enabled	99.4.2
2	preemption capability active	1 = active 0 = not active	99.4.3
4:3	additional fragment size	A 2-bit integer value indicating, in units of 64 octets, the minimum number of octets over 64 octets required in non-final fragments by the receiver	99.4.4
15:5	Reserved	—	—

79.3.8 Power via MDI Measurements TLV

Clause 33 and Clause 145 define two optional power entities: a Powered Device (PD) and Power Sourcing Equipment (PSE). These entities allow devices to draw/supply power over the same generic cabling as used for data transmission. The Power Via MDI Measurement TLV allows network management to read electrical measurement data from the sending IEEE 802.3 LAN station. Figure 79–9 shows the format of this TLV.

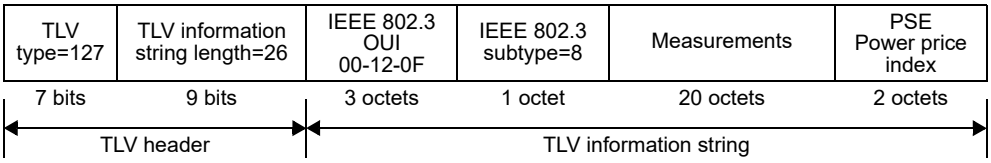

Figure 79–9—Power Via MDI Measurements TLV format for Type 3 and Type 4

79.3.8.1 Measurements

This field shall be set according to Table 79–21.

The ‘Voltage measurement’ field carries the measured voltage value at the PI, the ‘Current measurement’ field carries the measured current value at the PI, the ‘Power measurement’ field carries the measured power value at the PI, and the ‘Energy measurement’ field carries the measured energy consumption value at the PI, as defined in Table 79–21.

Measurement values (voltage, current, power, or energy) shall be set to 0 in case the corresponding request bit is 0. If a device does not support a particular measurement, the corresponding measurement value shall be set to 0.

79.3.8.2 PSE power price index

The ‘PSE power price index’ field shall contain an index of the current price of electricity compared to what the PSE considers the nominal electricity price. The determination of the nominal electricity price is implementation dependent. The field is encoded as defined in Equation (79–1). The PSE sets the value of

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Table 79–21—Measurements

Bit	Function	Value/meaning
159	Voltage support	1 = Device supports voltage measurement 0 = Device does not support voltage measurement
158	Current support	1 = Device supports current measurement 0 = Device does not support current measurement
157	Power support	1 = Device supports power measurement 0 = Device does not support power measurement
156	Energy support	1 = Device supports energy measurement 0 = Device does not support energy measurement
155:154	Reserved	
153:152	Measurement source	Determine where the measurement is to be taken. 153 152 0 0 No request 0 1 Pairset Alternative A / Mode A 1 0 Pairset Alternative B / Mode B 1 1 Port total
151	Voltage request	1 = Request for voltage measurement 0 = No request for voltage measurement
150	Current request	1 = Request for current measurement 0 = No request for current measurement
149	Power request	1 = Request for power measurement 0 = No request for power measurement
148	Energy request	1 = Request for energy measurement 0 = No request for energy measurement
147	Voltage measurement valid	1 = Voltage measurement field contains valid data 0 = Voltage measurement disabled
146	Current measurement valid	1 = Current measurement field contains valid data 0 = Current measurement disabled
145	Power measurement valid	1 = Power measurement field contains valid data 0 = Power measurement disabled
144	Energy measurement valid	1 = Energy measurement field contains valid data 0 = Energy measurement disabled
143:128	Voltage uncertainty	Expanded uncertainty (coverage factor k = 2) for the voltage measurement, expressed in units of 1 mV. Valid values are 1 through 65 000.
127:112	Current uncertainty	Expanded uncertainty (coverage factor k = 2) for the current measurement, expressed in units of 0.1 mA. Valid values are 1 through 65 000.
111:96	Power uncertainty	Expanded uncertainty (coverage factor k = 2) for the power measurement, expressed in units of 10 mW. Valid values are 1 through 65 000.

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Table 79–21—Measurements *(continued)*

Bit	Function	Value/meaning
95:80	Energy uncertainty	Expanded uncertainty (coverage factor k = 2) for the energy measurement, expressed in units of 0.1 kJ. Valid values are 1 through 65 000.
79:64	Voltage measurement	$V_{Port\_PD\text{-}2P}$ expressed in units of 1 mV. When the Measurement source is set to 'Port total' this field contains the measurement of the pairset with the highest voltage. Valid values are 0 through 65 000[a].
63:48	Current measurement	I_{Port} or $I_{Port\text{-}2P}$ expressed in units of 0.1 mA. Valid values are 0 through 20 000.
47:32	Power measurement	Power sourced or drawn expressed in units of 10 mW. Valid values are 0 through 10 000.
31:0	Energy measurement	Energy consumed at the port or pairset expressed in units of 0.1 kJ since power on. Valid values are 0 through 4 294 967 295.

[a] The valid range of this field extends beyond the allowed operating range of V_{Port_PD} or $V_{Port\_PD\text{-}2P}$; see 33.3.7.1 and 145.3.8.1.

this field taking the availability of power from any external and internal resources, and the relative supply and demand balance, into account. A value of 0xFFFF means that no power price index is available.

$$K_{PPI} = \left(\frac{(\text{Power price index} + 10046) \times 2.512}{75046}\right)^5 \quad (79\text{–}1)$$

where

K_{PPI} is the power price index expressed as a factor ranging from 0.0004 to 100 times the nominal price

Power price index is the value of the 'Power price index' field defined in Table 79–22

Table 79–22—Power price index

Bit	Function	Value/meaning
15:0	Power price index	Valid values for these bits are decimal 0 through 65 000, and hexadecimal value 0xFFFF.

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79.3.8.3 Power Via MDI Measurements TLV usage rules

An LLDPDU should contain no more than one Power Via MDI Measurements TLV.

79.4 IEEE 802.3 Organizationally Specific TLV selection management

TLV selection management consists of providing the network manager with the means to select which specific IEEE 802.3 Organizationally Specific TLVs are enabled for inclusion in an LLDPDU. The following LLDP variable cross references the LLDP local systems configuration MIB tables (see Clause 11 of IEEE Std 802.1AB-2009) to indicate which specific TLVs are enabled for the particular port(s) on the system. The specific port(s) through which each TLV is enabled for transmission may be set (or reset) by the network manager:

a) **mibXdot3TLVsTxEnable:** This variable lists the single-instance use IEEE 802.3 Organizationally Specific TLVs, each with a bitmap indicating the system ports through which the referenced TLV is enabled for transmission.

79.4.1 IEEE 802.3 Organizationally Specific TLV selection variable/LLDP Configuration managed object class cross reference

Table 79–23 lists the relationship both between IEEE 802.3 TLV selection variable and the corresponding LLDP Configuration managed object class (see 30.12.1) attribute.

Table 79–23—IEEE 802.3 Organizationally Specific TLV selection variable/LLDP MIB object cross reference

IEEE 802.3 TLV selection variable	LLDP Configuration managed object class attribute
mibXdot3TLVsTxEnable	aLldpXdot3PortConfigTLVsTxEnable

79.4.2 IEEE 802.3 Organizationally Specific TLV/LLDP Local and Remote System group managed object class cross references

The cross references between the IEEE 802.3 TLVs and the LLDP Local System Group managed object class (see 30.12.2) attributes are listed in Table 79–24. The cross references between the IEEE 802.3 TLVs and the LLDP Remote System Group managed object class (see 30.12.3) attributes are listed in Table 79–25.

The cross-references between the EEE TLV, the EEE Fast Wake TLV, and the EEE local (30.12.2) and remote (30.12.3) object class attributes are listed in Table 79–24 and Table 79–25.

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Table 79–24—IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references

TLV name	TLV variable	LLDP Local System Group managed object class attribute
MAC/PHY Configuration/Status	Auto-negotiation support	aLldpXdot3LocPortAutoNegSupported
	Auto-negotiation status	aLldpXdot3LocPortAutoNegEnabled
	PMD auto-negotiation advertised capability	aLldpXdot3LocPortAutoNegAdvertisedCap
	Operational MAU type	aLldpXdot3LocPortOperMauType
Power via MDI	Port class	aLldpXdot3LocPowerPortClass
	PSE MDI power support	aLldpXdot3LocPowerMDISupported
	PSE MDI power state	aLldpXdot3LocPowerMDIEnabled
	PSE pairs control ability	aLldpXdot3LocPowerPairControllable
	PSE power pair	aLldpXdot3LocPowerPairs
	Power class	aLldpXdot3LocPowerClass
	Power type	aLldpXdot3LocPowerType
	Power source	aLldpXdot3LocPowerSource
	Power priority	aLldpXdot3LocPowerPriority
	PD requested power value	aLldpXdot3LocPDRequestedPowerValue
	PSE allocated power value	aLldpXdot3LocPSEAllocatedPowerValue
	PD requested power value Mode A	aLldpXdot3LocPDRequestedPowerValueA
	PD requested power value Mode B	aLldpXdot3LocPDRequestedPowerValueB
	PSE allocated power value Alternative A	aLldpXdot3LocPSEAllocatedPowerValueA
	PSE allocated power value Alternative B	aLldpXdot3LocPSEAllocatedPowerValueB
	PSE powering status	aLldpXdot3LocPSEPoweringStatus
	PD powered status	aLldpXdot3LocPDPoweredStatus
	PSE power pairs ext	aLldpXdot3LocPowerPairsExt
	Dual-signature power Class ext Mode A	aLldpXdot3LocPowerClassExtA
	Dual-signature power Class ext Mode B	aLldpXdot3LocPowerClassExtB
	Power class ext	aLldpXdot3LocPowerClassExt
	Power Type ext	aLldpXdot3LocPowerTypeExt
	PD 4PID	aLldpXdot3LocPD4PID
	PD Load	aLldpXdot3LocPDLoad
	PSE maximum available power value	aLldpXdot3LocPSEMaxAvailPower
	PSE Autoclass support	aLldpXdot3LocPSEAutoclassSupport
	Autoclass completed	aLldpXdot3LocAutoclassCompleted

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Table 79–24—IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references *(continued)*

TLV name	TLV variable	LLDP Local System Group managed object class attribute
Power via MDI (*continued*)	Autoclass request	aLldpXdot3LocAutoclassRequest
	Power down request	aLldpXdot3LocPowerDownRequest
	Power down time	aLldpXdot3LocPowerDownTime
Power via MDI Measurements	Voltage support	aLldpXdot3LocMeasVoltageSupport
	Current support	aLldpXdot3LocMeasCurrentSupport
	Power support	aLldpXdot3LocMeasPowerSupport
	Energy support	aLldpXdot3LocMeasEnergySupport
	Measurement source	aLldpXdot3LocMeasurementSource
	Voltage request	aLldpXdot3LocMeasVoltageRequest
	Current request	aLldpXdot3LocMeasCurrentRequest
	Power request	aLldpXdot3LocMeasPowerRequest
	Energy request	aLldpXdot3LocMeasEnergyRequest
	Voltage measurement valid	aLldpXdot3LocMeasVoltageValid
	Current measurement valid	aLldpXdot3LocMeasCurrentValid
	Power measurement valid	aLldpXdot3LocMeasPowerValid
	Energy measurement valid	aLldpXdot3LocMeasEnergyValid
	Voltage uncertainty	aLldpXdot3LocMeasVoltageUncertainty
	Current uncertainty	aLldpXdot3LocMeasCurrentUncertainty
	Power uncertainty	aLldpXdot3LocMeasPowerUncertainty
	Energy uncertainty	aLldpXdot3LocMeasEnergyUncertainty
	Voltage measurement	aLldpXdot3LocVoltageMeasurement
	Current measurement	aLldpXdot3LocCurrentMeasurement
	Power measurement	aLldpXdot3LocPowerMeasurement
	Energy measurement	aLldpXdot3LocEnergyMeasurement
	PSE Power price index	aLldpXdot3LocPSEPowerPriceIndex
Link Aggregation (deprecated)	aggregation status	aLldpXdot3LocLinkAggStatus
	aggregated port ID	aLldpXdot3LocLinkAggPortId
Maximum Frame Size	maximum frame size	aLldpXdot3LocMaxFrameSize

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Table 79–24—IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references *(continued)*

TLV name	TLV variable	LLDP Local System Group managed object class attribute
EEE	Transmit $T_{w\_sys\_tx}$	aLldpXdot3LocTxTwSys
	Receive $T_{w\_sys\_tx}$	aLldpXdot3LocRxTwSys
	Echo Transmit $T_{w\_sys\_tx}$	aLldpXdot3LocTxTwSysEcho
	Echo Receive $T_{w\_sys\_tx}$	aLldpXdot3LocRxTwSysEcho
	Fallback $T_{w\_sys\_tx}$	aLldpXdot3LocFbTwSys
EEE Fast Wake	Transmit fast wake	aLldpXdot3LocTxFw
	Receive fast wake	aLldpXdot3LocRxFw
	Echo Transmit fast wake	aLldpXdot3LocTxFwEcho
	Echo Receive fast wake	aLldpXdot3LocRxFwEcho
Additional Ethernet Capabilities	preemption capability support	aLldpXdot3LocPreemptSupported
	preemption capability status	aLldpXdot3LocPreemptEnabled
	preemption capability active	aLldpXdot3LocPreemptActive
	additional fragment size	aLldpXdot3LocAddFragSize

Table 79–25—IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references

TLV name	TLV variable	LLDP Remote System Group managed object class attribute
MAC/PHY Configuration/Status	Auto-negotiation support	aLldpXdot3RemPortAutoNegSupported
	Auto-negotiation status	aLldpXdot3RemPortAutoNegEnabled
	PMD auto-negotiation advertised capability	aLldpXdot3RemPortAutoNegAdvertisedCap
	Operational MAU type	aLldpXdot3RemPortOperMauType
Power via MDI	Port class	aLldpXdot3RemPowerPortClass
	PSE MDI power support	aLldpXdot3RemPowerMDISupported
	PSE MDI power state	aLldpXdot3RemPowerMDIEnabled
	PSE pairs control ability	aLldpXdot3RemPowerPairControllable
	PSE power pair	aLldpXdot3RemPowerPairs
	Power class	aLldpXdot3RemPowerClass
	Power type	aLldpXdot3RemPowerType

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Table 79–25—IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references *(continued)*

TLV name	TLV variable	LLDP Remote System Group managed object class attribute
Power via MDI (*continued*)	Power source	aLldpXdot3RemPowerSource
	Power priority	aLldpXdot3RemPowerPriority
	PD requested power value	aLldpXdot3RemPDRequestedPowerValue
	PSE allocated power value	aLldpXdot3RemPSEAllocatedPowerValue
	PD requested power value Mode A	aLldpXdot3RemPDRequestedPowerValueA
	PD requested power value Mode B	aLldpXdot3RemPDRequestedPowerValueB
	PSE allocated power value Alternative A	aLldpXdot3RemPSEAllocatedPowerValueA
	PSE allocated power value Alternative B	aLldpXdot3RemPSEAllocatedPowerValueB
	PSE powering status	aLldpXdot3RemPSEPoweringStatus
	PD powered status	aLldpXdot3RemPDPoweredStatus
	PSE power pairs ext	aLldpXdot3RemPowerPairsExt
	Dual-signature power Class ext Mode A	aLldpXdot3RemPowerClassExtA
	Dual-signature power Class ext Mode B	aLldpXdot3RemPowerClassExtB
	Power class ext	aLldpXdot3RemPowerClassExt
	Power Type ext	aLldpXdot3RemPowerTypeExt
	PD 4PID	aLldpXdot3RemPD4PID
	PD Load	aLldpXdot3RemPDLoad
	PSE maximum available power value	aLldpXdot3RemPSEMaxAvailPower
	PSE Autoclass support	aLldpXdot3RemPSEAutoclassSupport
	Autoclass completed	aLldpXdot3RemAutoclassCompleted
	Autoclass request	aLldpXdot3RemAutoclassRequest
	Power down request	aLldpXdot3RemPowerDownRequest
	Power down time	aLldpXdot3RemPowerDownTime
Power via MDI Measurements	Voltage support	aLldpXdot3RemMeasVoltageSupport
	Current support	aLldpXdot3RemMeasCurrentSupport
	Power support	aLldpXdot3RemMeasPowerSupport
	Energy support	aLldpXdot3RemMeasEnergySupport
	Measurement source	aLldpXdot3RemMeasurementSource
	Voltage request	aLldpXdot3RemMeasVoltageRequest
	Current request	aLldpXdot3RemMeasCurrentRequest
	Power request	aLldpXdot3RemMeasPowerRequest
	Energy request	aLldpXdot3RemMeasEnergyRequest

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Table 79–25—IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references *(continued)*

TLV name	TLV variable	LLDP Remote System Group managed object class attribute
Power via MDI Measurements (*continued*)	Voltage measurement valid	aLldpXdot3RemMeasVoltageValid
	Current measurement valid	aLldpXdot3RemMeasCurrentValid
	Power measurement valid	aLldpXdot3RemMeasPowerValid
	Energy measurement valid	aLldpXdot3RemMeasEnergyValid
	Voltage uncertainty	aLldpXdot3RemMeasVoltageUncertainty
	Current uncertainty	aLldpXdot3RemMeasCurrentUncertainty
	Power uncertainty	aLldpXdot3RemMeasPowerUncertainty
	Energy uncertainty	aLldpXdot3RemMeasEnergyUncertainty
	Voltage measurement	aLldpXdot3RemVoltageMeasurement
	Current measurement	aLldpXdot3RemCurrentMeasurement
	Power measurement	aLldpXdot3RemPowerMeasurement
	Energy measurement	aLldpXdot3RemEnergyMeasurement
	PSE Power price index	aLldpXdot3RemPSEPowerPriceIndex
Link Aggregation (deprecated)	aggregation status	aLldpXdot3RemLinkAggStatus
	aggregated port ID	aLldpXdot3RemLinkAggPortId
Maximum Frame Size	maximum frame size	aLldpXdot3RemMaxFrameSize
EEE	Transmit $T_{w\_sys\_tx}$	aLldpXdot3RemTxTwSys
	Receive $T_{w\_sys\_tx}$	aLldpXdot3RemRxTwSys
	Echo Transmit $T_{w\_sys\_tx}$	aLldpXdot3RemTxTwSysEcho
	Echo Receive $T_{w\_sys\_tx}$	aLldpXdot3RemRxTwSysEcho
	Fallback $T_{w\_sys\_tx}$	aLldpXdot3RemFbTwSys
EEE Fast Wake	Transmit fast wake	aLldpXdot3RemTxFw
	Receive fast wake	aLldpXdot3RemRxFw
	Echo Transmit fast wake	aLldpXdot3RemTxFwEcho
	Echo Receive fast wake	aLldpXdot3RemRxFwEcho
Additional Ethernet Capabilities	preemption capability support	aLldpXdot3RemPreemptSupported
	preemption capability status	aLldpXdot3RemPreemptEnabled
	preemption capability active	aLldpXdot3RemPreemptActive
	additional fragment size	aLldpXdot3RemAddFragSize

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79.5 Protocol implementation conformance statement (PICS) proforma for IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements[142]

79.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 79, IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

79.5.2 Identification

79.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

79.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 79, IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[142]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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79.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*MP	MAC/PHY Configuration/Status TLV	79.3.1		O	Yes [ ] No [ ]
*PV	Power Via MDI TLV	79.3.2		O	Yes [ ] No [ ]
*PT12	Device is a Type 1 or Type 2 PSE or PD	79.3.2		O	Yes [ ] No [ ]
*PT34	Device is a Type 3 or Type 4 PSE or PD	79.3.2		O	Yes [ ] No [ ]
*LA	Link Aggregation TLV	79.3.3	TLV deprecated	O	Yes [ ] No [ ]
*FS	Maximum Frame Size TLV	79.3.4		O	Yes [ ] No [ ]
*EE	EEE TLV	79.3.5		O	Yes [ ] No [ ]
*EEFW	EEE Fast Wake TLV	79.3.6		O	Yes [ ] No [ ]
*AE	Additional Ethernet Capabilities TLV	79.3.7		O	Yes [ ] No [ ]
*PM	Power via MDI Measurements TLV	79.3.8		O	Yes [ ] No [ ]

79.5.4 IEEE 802.3 Organizationally Specific TLV

Item	Feature	Subclause	Value/Comment	Status	Support
TLV1	Group MAC addresses	79.2	*Nearest device* group MAC addresses listed in Table 7-1 of IEEE Std 802.1AB-2009	M	Yes [ ]
TLV2	LLDPDU bit and octet ordering	79.2	Defined in subclause 8.1 of IEEE Std 802.1AB-2009	M	Yes [ ]

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79.5.5 MAC/PHY Configuration/Status TLV

Item	Feature	Subclause	Value/Comment	Status	Support
MPT1	auto-negotiation support/status field	79.3.1.1	Identifies support and current status as defined in Table 79–2	MP:M	Yes [ ] N/A [ ]
MPT2	PMD auto-negotiation capability field	79.3.1.2	Bitmap of the ifMauAutoNeg-CapAdvertisedBits object defined in IETF RFC 4836	MP:M	Yes [ ] N/A [ ]
MPT3	operational MAU type field	79.3.1.3	Derived from the list position of the corresponding dot3Mau-Type as listed in IETF RFC 4836 (or subsequent revisions)	MP:M	Yes [ ] N/A [ ]
MPT4	operational MAU type field	79.3.1.3	Set to zero for MAU types not listed in IETF RFC 4836 (or subsequent revisions)	MP:M	Yes [ ] N/A [ ]
MPT5	Usage rules	79.3.1.4	LLDPDU contains no more than one MAC/PHY Configuration/Status TLV	MP:O	Yes [ ] No [ ] N/A [ ]

79.5.6 EEE TLV

Item	Feature	Subclause	Value/Comment	Status	Support
EET1	Transmit T_w field	79.3.5.1	2 octets representing time (expressed in microseconds) that the transmitting link partner will wait before it starts transmitting data after leaving the LPI mode	EE:M	Yes [ ] N/A [ ]
EET2	Receive T_w field	79.3.5.2	2 octets representing time (expressed in microseconds) that the receiving link partner is requesting the transmitting link partner to wait before it starts transmitting data following the LPI	EE:M	Yes [ ] N/A [ ]
EET3	Fallback field	79.3.5.3	2 octets representing time (expressed in microseconds)	EE:O	Yes [ ] No [ ] N/A [ ]
EET4	Echo Transmit and Receive T_w fields	79.3.5.4	2 octets representing time (expressed in microseconds)	EE:M	Yes [ ] N/A [ ]
EET5	Usage rules	79.3.5.5	LLDPDU contains no more than one EEE TLV	EE:O	Yes [ ] No [ ] N/A [ ]

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79.5.7 EEE Fast Wake TLV

Item	Feature	Subclause	Value/Comment	Status	Support
EFW1	Transmit fast wake field	79.3.6.1	1 octet representing fast wake option for transmit LPI function	EEFW: M	Yes [ ] N/A [ ]
EFW2	Receive fast wake field	79.3.6.2	1 octet representing fast wake option for receive LPI function	EEFW: M	Yes [ ] N/A [ ]
EFW3	Echo Transmit and Receive fast wake fields	79.3.6.3	2 octets representing received fast wake options	EEFW: M	Yes [ ] N/A [ ]

79.5.8 Power Via MDI TLV

Item	Feature	Subclause	Value/Comment	Status	Support
PVT1	Not send DLL classification or Type 3 and Type 4 extension fields	79.3.2	Unless supplying or drawing power from the PI	PV:M	Yes [ ] N/A [ ]
PVT2	Type 1 or Type 2 power entity DLL classification extension fields	79.3.2	Support the Power Via MDI TLV DLL classification extension fields shown in Figure 79–3 after the PI has been powered	PV*PT12:M	Yes [ ] N/A [ ]
PVT3	Type 3 or Type 4 power entity DLL classification extension fields	79.3.2	Support the Power Via MDI TLV DLL classification extension fields and Type 3 and Type 4 extension fields shown in Figure 79–3 after the PI has been powered	PV*PT34:M	Yes [ ] N/A [ ]
PVT4	Not support Type 3 and Type 4 power entity DLL Classification	79.3.2	Not include the Type 3 and Type 4 extension fields in Power via MDI TLVs	PV*PT12:M	Yes [ ] N/A [ ]
PVT5	‘Port class’ field	79.3.2.1.1	Indicates if the port is a PSE or a PD when transmitted	PV:M	Yes [ ] N/A [ ]
PVT6	‘PSE MDI power support’ field	79.3.2.1.2	Indicates if MDI power is supported	PV:M	Yes [ ] N/A [ ]
PVT7	‘PSE MDI power state’ field	79.3.2.1.3	Indicates if the PSE function is enabled or disabled	PV:M	Yes [ ] N/A [ ]
PVT8	‘PSE pairs control ability’ field	79.3.2.1.4	Indicates if the PSE has the capability to control which PSE Pinout Alternative is used for PD detection and power	PV:M	Yes [ ] N/A [ ]
PVT9	‘PSE power pair’ field	79.3.2.2	Integer value as defined in Table 79–5 based on aPSEPowerPairs (30.9.1.1.4)	PV:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PVT10	‘PSE power pair’ field for Type 3 or Type 4 PSEs furnishing power on a single pairset	79.3.2.2	To use value that defines that pairset	PV:M	Yes [ ] N/A [ ]
PVT11	‘Power class’ field	79.3.2.3	Integer value as defined in Table 79–6 by the aPsePortPowerClassification (30.9.1.1.8)	PV:M	Yes [ ] N/A [ ]
PVT12	‘Power type/source/priority’ field	79.3.2.4	Contains a bit-map of the Power type, source, and priority defined in Table 79–7	PV:M	Yes [ ] N/A [ ]
PVT13	‘Power type’ field	79.3.2.4.1	Set according to Table 79–7	PV:M	Yes [ ] N/A [ ]
PVT14	‘Power type’ field for Type 3 or Type 4 PSEs	79.3.2.4.1	Set to the value corresponding with Type 2 PSEs	PV*PT34:M	Yes [ ] N/A [ ]
PVT15	‘Power type’ field for Type 3 or Type 4 PDs	79.3.2.4.1	Set to the value corresponding with Type 2 PDs	PV*PT34:M	Yes [ ] N/A [ ]
PVT16	‘PD 4PID’ field when Power type is PD	79.3.2.4.3	Set according to Table 79–7 to indicate whether the PD supports powering of both Modes simultaneously	PV*PT34:M	Yes [ ] N/A [ ]
PVT17	‘PD 4PID’ field when Power type is PSE	79.3.2.4.3	Set to ‘0’	PV:M	Yes [ ] N/A [ ]
PVT18	‘PD requested power value’ field	79.3.2.5	Contains the PD’s requested power value defined in Table 79–8	PV:M	Yes [ ] N/A [ ]
PVT19	‘PSE allocated power value’ field	79.3.2.6	Contains the PSE’s allocated power value defined in Table 79–9	PV:M	Yes [ ] N/A [ ]
PVT20	‘PD requested power Mode A’ field and ‘PD requested power Mode B’ field	79.3.2.7	Contains the PD’s requested power value defined in Table 79–10 for Mode A and Table 79–11 for Mode B	PV*PT34:M	Yes [ ] N/A [ ]
PVT21	‘PSE allocated power Alternative A’ field and ‘PSE allocated power Alternative B’ field	79.3.2.8	Contains the values in Table 79–12 and Table 79–13	PV*PT34:M	Yes [ ] N/A [ ]
PVT22	‘PSE powering status’ field for PSEs	79.3.2.9.1	Set to the current powering status as defined in Table 79–14	PV*PT34:M	Yes [ ] N/A [ ]
PVT23	‘PSE powering status’ field for PDs	79.3.2.9.1	Set to ‘0’	PV*PT34:M	Yes [ ] N/A [ ]
PVT24	‘PD powered status’ field for PDs	79.3.2.9.2	Set to the current powered status as defined in Table 79–14	PV*PT34:M	Yes [ ] N/A [ ]
PVT25	‘PD powered status’ field for PSEs	79.3.2.9.2	Set to ‘0’	PV*PT34:M	Yes [ ] N/A [ ]
PVT26	‘PSE power pairs ext’ field for PSEs	79.3.2.9.3	Contain powering status of the PSE as defined in Table 79–14	PV*PT34:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PVT27	‘PSE power pairs ext’ field for PDs	79.3.2.9.3	Set to ‘0’	PV*PT34:M	Yes [ ] N/A [ ]
PVT28	‘Dual-signature power Class ext Mode A’ field for single-signature PDs	79.3.2.9.4	Set to ‘7’	PV*PT34:M	Yes [ ] N/A [ ]
PVT29	‘Dual-signature power Class ext Mode A’ field for dual-signature PDs	79.3.2.9.4	Set to the requested Class (see 145.3.6) for Mode A	PV*PT34:M	Yes [ ] N/A [ ]
PVT30	‘Dual-signature power Class ext Mode A’ field for 2-pair only PSEs or PSEs connected to a single-signature PD	79.3.2.9.4	Set to ‘7’	PV*PT34:M	Yes [ ] N/A [ ]
PVT31	‘Dual-signature power Class ext Mode A’ field for PSEs connected to a dual-signature PD	79.3.2.9.4	Set to the assigned Class (see 145.2.8) for Mode A	PV*PT34:M	Yes [ ] N/A [ ]
PVT32	‘Dual-signature power Class ext Mode B’ field for single-signature PDs	79.3.2.9.5	Set to ‘7’	PV*PT34:M	Yes [ ] N/A [ ]
PVT33	‘Dual-signature power Class ext Mode B’ field for dual-signature PDs	79.3.2.9.5	Set to the requested Class (see 145.3.6) for Mode B	PV*PT34:M	Yes [ ] N/A [ ]
PVT34	‘Dual-signature power Class ext Mode B’ field for 2-pair only PSEs or PSEs connected to a single-signature PD	79.3.2.9.5	Set to ‘7’	PV*PT34:M	Yes [ ] N/A [ ]
PVT35	‘Dual-signature power Class ext Mode B’ field for PSEs connected to a dual-signature PD	79.3.2.9.5	Set to the assigned Class (see 145.2.8) for Mode B	PV*PT34:M	Yes [ ] N/A [ ]
PVT36	‘Power Class ext’ field for single-signature PDs	79.3.2.9.6	Set to the requested Class (see 145.3.6)	PV*PT34:M	Yes [ ] N/A [ ]
PVT37	‘Power Class ext’ field for dual-signature PDs	79.3.2.9.6	Set to ‘7’	PV*PT34:M	Yes [ ] N/A [ ]
PVT38	‘Dual-signature power Class ext Mode B’ field for 2-pair only PSEs or PSEs connected to a single-signature PD	79.3.2.9.6	Set to the assigned Class (see 145.2.8)	PV*PT34:M	Yes [ ] N/A [ ]
PVT39	‘Dual-signature power Class ext Mode B’ field for PSEs connected to a dual-signature PD	79.3.2.9.6	Set to ‘7’	PV*PT34:M	Yes [ ] N/A [ ]
PVT40	‘System setup’ field	79.3.2.10	Contains the device bit-map of the Power Type ext and PD Load defined in Table 79–15	PV*PT34:M	Yes [ ] N/A [ ]
PVT41	‘Power type ext’ field	79.3.2.10.1	Set according to Table 79–15	PV*PT34:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PVT42	‘PD Load’ field when ‘Power type’ is PD	79.3.2.10.2	Set according to Table 79–15	PV*PT34:M	Yes [ ] N/A [ ]
PVT43	‘PD Load’ field when ‘Power type’ is PSE	79.3.2.10.2	Set to ‘0’	PV*PT34:M	Yes [ ] N/A [ ]
PVT44	‘PSE maximum available power value’ field	79.3.2.11	Contains the highest power the PSE can grant as defined in Table 79–16	PV*PT34:M	Yes [ ] N/A [ ]
PVT45	‘PSE maximum available power value’ field for PDs	79.3.2.11	Set to ‘0’	PV*PT34:M	Yes [ ] N/A [ ]
PVT46	‘Autoclass’ field	79.3.2.12	Contains the bits defined in Table 79–17	PV*PT34:M	Yes [ ] N/A [ ]
PVT47	‘PSE Autoclass support’ field when ‘Power type’ is PSE	79.3.2.12.1	Set to indicate if the PSE supports Autoclass over DLL according to Table 79–17	PV*PT34:M	Yes [ ] N/A [ ]
PVT48	‘PSE Autoclass support’ field when ‘Power type’ is PD	79.3.2.12.1	Set to ‘0’	PV*PT34:M	Yes [ ] N/A [ ]
PVT49	‘Autoclass completed’ field when ‘Power type’ is PSE	79.3.2.12.2	Set to indicate that the PSE has concluded the Autoclass measurement	PV*PT34:M	Yes [ ] N/A [ ]
PVT50	‘Autoclass completed’ field when ‘Power type’ is PD	79.3.2.12.2	Set to ‘0’	PV*PT34:M	Yes [ ] N/A [ ]
PVT51	‘Autoclass request’ field when ‘Power type’ is PSE	79.3.2.12.3	Set to 0’0	PV*PT34:M	Yes [ ] N/A [ ]
PVT52	‘Power down’ field	79.3.2.13	Contains the bits defined in Table 79–18	PV*PT34:M	Yes [ ] N/A [ ]
PVT53	‘Power down request’ field when ‘Power type’ is PD and power is to be maintained	79.3.2.13.1	Set to ‘0’	PV*PT34:M	Yes [ ] N/A [ ]
PVT54	‘Power down request’ field when ‘Power type’ is PSE	79.3.2.13.1	Set to ‘0’	PV*PT34:M	Yes [ ] N/A [ ]
PVT55	‘Power down time’ field when ‘Power type’ is PD	79.3.2.13.2	Set per the description in Table 79–18	PV*PT34:M	Yes [ ] N/A [ ]
PVT56	‘Power down time’ field when ‘Power type’ is PSE	79.3.2.13.2	Set to ‘0’	PV*PT34:M	Yes [ ] N/A [ ]

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79.5.9 Link Aggregation TLV

Item	Feature	Subclause	Value/Comment	Status	Support
LAT1	link aggregation status field	79.3.3.1	Bitmap of the link aggregation capabilities and the current aggregation status as defined in Table 79–19	LA:M	Yes [ ] N/A [ ]
LAT2	aggregated port ID	79.3.3.2	IEEE 802.3 aggregated port identifier, aAggPortID	LA:M	Yes [ ] N/A [ ]
LAT3	Usage rules	79.3.3.3	LLDPDU contains no more than one Link Aggregation TLV	LA:O	Yes [ ] No [ ] N/A [ ]

79.5.10 Maximum Frame Size TLV

Item	Feature	Subclause	Value/Comment	Status	Support
FST1	maximum frame size field	79.3.4.1	Integer value indicating the maximum supported frame size	FS:M	Yes [ ] N/A [ ]
FST2	maximum frame size field	79.3.4.1	1518 for basic frames	FS:O/1	Yes [ ] No [ ] N/A [ ]
FST3	maximum frame size field	79.3.4.1	1522 for Q-tagged frames	FS:O/1	Yes [ ] No [ ] N/A [ ]
FST4	maximum frame size field	79.3.4.1	2000 for envelope frames	FS:O/1	Yes [ ] No [ ] N/A [ ]
FST5	Usage rules	79.3.4.2	LLDPDU contains no more than one Maximum Frame Size TLV	FS:O	Yes [ ] No [ ] N/A [ ]

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79.5.11 Additional Ethernet Capabilities TLV

Item	Feature	Subclause	Value/Comment	Status	Support
AET1	Ethernet capabilities field	79.3.7.1	Contains a bitmap that identifies the support and current status of additional Ethernet capabilities	AE:M	Yes [ ] N/A [ ]
AET2	Reserved bits	79.3.7.1	Set to zero and ignored on receipt	AE:M	Yes [ ] N/A [ ]
AET3	Reserved octets	79.3.7.1	Not transmitted and ignored on receipt	AE:M	Yes [ ] N/A [ ]
AET4	octets not received	79.3.7.1	Treated as all zero	AE:M	Yes [ ] N/A [ ]
AET5	usage rule—at most one	79.3.7.2	LLDPDU should contain no more than one Additional Ethernet Capabilities TLV	AE:O	Yes [ ] No [ ] N/A [ ]
AET6	usage rule—address	79.3.7.2	Additional Ethernet Capabilities TLV should be sent in an LLDPDU addressed to Nearest Bridge group address	AE:O	Yes [ ] No [ ] N/A [ ]

79.5.12 Power via MDI Measurements TLV

Item	Feature	Subclause	Value/Comment	Status	Support
PMT1	‘Measurements’ field	79.3.8.1	Set according to Table 79–21	PV*PT34:M	Yes [ ] N/A [ ]
PMT2	Measurement values (voltage, current, power, or energy)	79.3.8.1	Set to ‘0’ in case the corresponding request bit is ‘0’	PV*PT34:M	Yes [ ] N/A [ ]
PMT3	No support for Measurement values (voltage, current, power, or energy)	79.3.8.1	Value that is not supported set to ‘0’	PV*PT34:M	Yes [ ] N/A [ ]
PMT4	‘PSE power price index’ field	79.3.8.2	Contains an index of the current price of electricity compared to what the PSE considers the nominal electricity price	PV*PT34:M	Yes [ ] N/A [ ]

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80. Introduction to 40 Gb/s and 100 Gb/s networks

80.1 Overview

80.1.1 Scope

This clause describes the general requirements for 40 Gigabit and 100 Gigabit Ethernet. 40 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 40 Gb/s, coupled with any IEEE 802.3 40GBASE Physical Layer implementation. 100 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 100 Gb/s, coupled with any IEEE 802.3 100GBASE Physical Layer implementation. 40 Gb/s and 100 Gb/s Physical Layer devices, such as those specified in Table 80–1, provide a bit error ratio (BER) better than or equal to 10^{-12} at the MAC/PLS service interface.

40 Gigabit and 100 Gigabit Ethernet is defined for full duplex operation only.

80.1.2 Objectives

NOTE—The contents of this subclause have been deleted.

80.1.3 Relationship of 40 Gigabit and 100 Gigabit Ethernet to the ISO OSI reference model

40 Gigabit and 100 Gigabit Ethernet couples the IEEE 802.3 MAC to a family of 40 Gb/s and 100 Gb/s Physical Layers. The relationships among 40 Gigabit and 100 Gigabit Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 80–1.

While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The XLGMII and CGMII, which, when implemented as a logical interconnection port between the MAC sublayer and the Physical Layer device (PHY), uses a 64-bit wide data path as specified in Clause 81. Physical instantiations of this interface may use other data-path widths.
b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.
c) The PMA service interface, which, when physically implemented as XLAUI (40 Gb/s Attachment Unit Interface) or CAUI-4 and 100GAUI-4 (100 Gb/s four-lane Attachment Unit Interface) at an observable interconnection port, uses a 4 lane data path as specified in Annex 83A, Annex 83B, Annex 83D, Annex 83E, Annex 135D, or Annex 135E.
d) The PMA service interface, which, when physically implemented as CAUI-10 (100 Gb/s ten-lane Attachment Unit Interface) at an observable interconnection port, uses a 10 lane data path as specified in Annex 83A or Annex 83B.
e) The PMA service interface, which, when physically implemented as 100GAUI-2 (100 Gb/s 2 lane Attachment Unit Interface) at an observable interconnection port, uses a 2 lane data path as specified in Annex 135F or Annex 135G.
f) The PMD service interface, which, when physically implemented as XLPPI (40 Gb/s Parallel Physical Interface) at an observable interconnection port, uses a 4 lane data path as specified in Annex 86A.
g) The PMD service interface, which, when physically implemented as CPPI (100 Gb/s Parallel Physical Interface) at an observable interconnection port, uses a 10 lane data path as specified in Annex 86A.

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h) The MDIs as specified in:
   — Clause 89 for 40GBASE-FR
   — Clause 140 for 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1
   — Clause 154 for 100GBASE-ZR
   use a single lane data path.
i) The MDIs as specified in:
   — Clause 85 for 40GBASE-CR4
   — Clause 86 for 40GBASE-SR4
   — Clause 87 for 40GBASE-LR4 and 40GBASE-ER4
   — Clause 88 for 100GBASE-LR4 and 100GBASE-ER4
   — Clause 92 for 100GBASE-CR4
   — Clause 95 for 100GBASE-SR4
   all use a 4 lane data path.
j) The MDIs as specified in Clause 85 for 100GBASE-CR10, and in Clause 86 for 100GBASE-SR10 use a 10 lane data path.
k) Although there is no electrical or mechanical specification of the MDI for backplane Physical Layers, the PMDs as specified in:
   — Clause 84 for 40GBASE-KR4
   — Clause 93 for 100GBASE-KR4
   — Clause 94 for 100GBASE-KP4
   all use a 4 lane data path.
l) The MDI as specified in Clause 113 for 40GBASE-T uses a 4 lane data path.
m) The MDIs as specified in:
   — Clause 136 for 100GBASE-CR2
   — Clause 137 for 100GBASE-KR2
   — Clause 138 for 100GBASE-SR2
   all use a 2 lane data path.

80.1.4 Nomenclature

The nomenclature employed by the 40 Gb/s and 100 Gb/s Physical Layers is explained as follows.

The alpha-numeric prefix 40GBASE in the port type (e.g., 40GBASE-R) represents a family of Physical Layer devices operating at a speed of 40 Gb/s. The alpha-numeric prefix 100GBASE in the port type (e.g., 100GBASE-R) represents a family of Physical Layer devices operating at a speed of 100 Gb/s.

40GBASE-R represents a family of Physical Layer devices using the Clause 82 Physical Coding Sublayer for 40 Gb/s operation over multiple PCS lanes (see Clause 82). Some 40GBASE-R Physical Layer devices may also use the FEC of Clause 74.

40GBASE-T represents Physical Layer devices using Clause 113 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, for data communication at 40 Gb/s over a point-to-point 4-pair balanced twisted-pair medium. 40GBASE-T uses a combination of Reed-Solomon FEC (RS-FEC) and low density parity check (LDPC) FECs in its physical coding sublayer that is mapped to a 128 double-square (DSQ128) constellation for transmission on 4-pair, twisted-pair copper cabling.

100GBASE-R represents a family of Physical Layer devices using the Clause 82 Physical Coding Sublayer for 100 Gb/s operation over multiple PCS lanes (see Clause 82) and a PMD implementing 2-level pulse amplitude modulation (PAM). Some 100GBASE-R Physical Layer devices also use the transcoding and FEC of Clause 91 and some may also use the FEC of Clause 74.

100GBASE-P represents Physical Layer devices using the Clause 82 Physical Coding Sublayer for 100 Gb/s operation over multiple PCS lanes (see Clause 82) and a PMD implementing more than 2-level pulse

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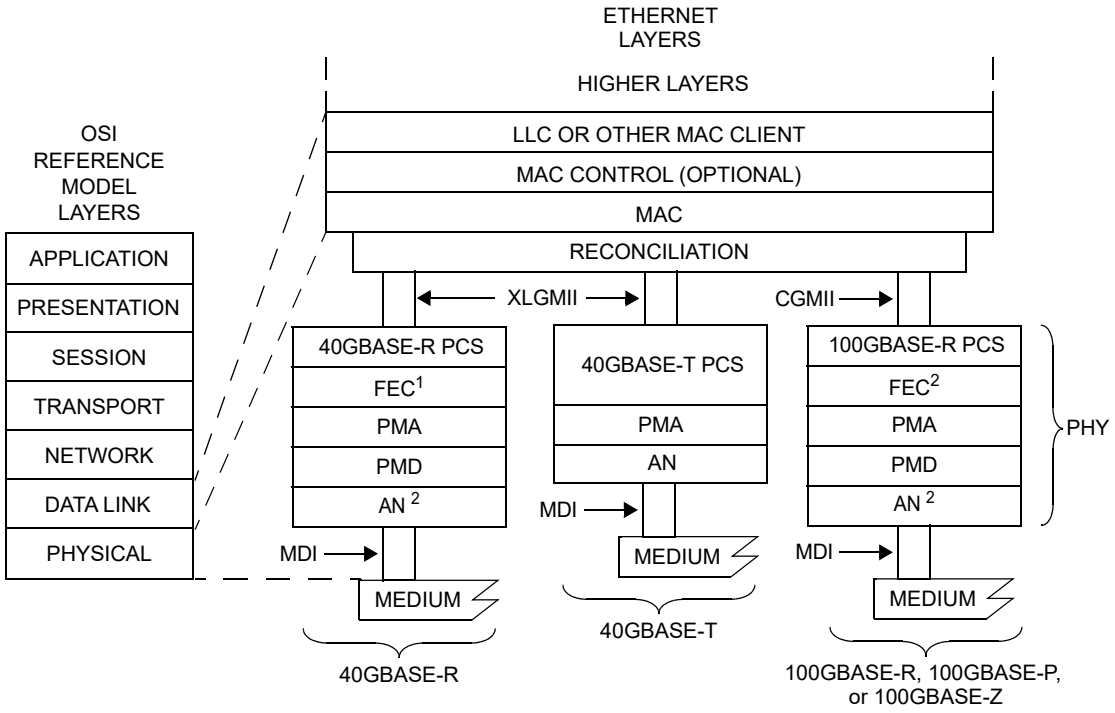

AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—OPTIONAL OR OMITTED DEPENDING ON PHY TYPE
NOTE 2—CONDITIONAL BASED ON PHY TYPE

Figure 80–1—Architectural positioning of 40 Gigabit and 100 Gigabit Ethernet

amplitude modulation (PAM). 100GBASE-P Physical Layer devices also use the transcoding and FEC of Clause 91.

100GBASE-Z represents a family of Physical Layer devices using the Clause 82 Physical Coding Sublayer for 100 Gb/s operation over multiple PCS lanes (see Clause 82), the FEC of Clause 153, and a PMD implementing dual polarization differential quadrature phase shift keying (DP-DQPSK) modulation. Some 100GBASE-Z Physical Layer devices also use the FEC of Clause 91 and the Inverse RS-FEC of Clause 152.

Physical Layer devices listed in Table 80–1 are defined for operation at 40 Gb/s and 100 Gb/s.

Table 80–1—40 Gb/s and 100 Gb/s PHYs

Name	Description
40GBASE-KR4	40 Gb/s PHY using 40GBASE-R encoding over four lanes of an electrical backplane, with reach up to at least 1 m (see Clause 84)
40GBASE-CR4	40 Gb/s PHY using 40GBASE-R encoding over four lanes of shielded balanced copper cabling, with reach up to at least 7 m (see Clause 85)
40GBASE-T	40 Gb/s PHY using RS-FEC and LDPC encoding over balanced twisted-pair structured cabling systems (see Clause 113)

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Table 80–1—40 Gb/s and 100 Gb/s PHYs *(continued)*

Name	Description
40GBASE-SR4	40 Gb/s PHY using 40GBASE-R encoding over four lanes of multimode fiber, with reach up to at least 100 m (see Clause 86)
40GBASE-FR	40 Gb/s PHY using 40GBASE-R encoding over one lane on single-mode fiber, with reach up to at least 2 km (see Clause 89)
40GBASE-LR4	40 Gb/s PHY using 40GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 10 km (see Clause 87)
40GBASE-ER4	40 Gb/s PHY using 40GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 40 km (see Clause 87)
100GBASE-KR4	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 2-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 35 dB at 12.9 GHz (see Clause 93)
100GBASE-KP4	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 4-level pulse amplitude modulation over four lanes of an electrical backplane, with a total insertion loss up to 33 dB at 7 GHz (see Clause 94)
100GBASE-KR2	100 Gb/s PHY using 100GBASE-R encoding, Clause 91 RS-FEC and 4-level pulse amplitude modulation over two lanes of an electrical backplane, with a total insertion loss up to 30 dB at 13.28 GHz (see Clause 137)
100GBASE-CR2	100 Gb/s PHY using 100GBASE-R encoding and Clause 91 RS-FEC and 4-level pulse amplitude modulation over two lanes of shielded balanced copper cabling, with reach up to at least 3 m (see Clause 136)
100GBASE-CR4	100 Gb/s PHY using 100GBASE-R encoding and Clause 91 RS-FEC over four lanes of shielded balanced copper cabling, with reach up to at least 5 m (see Clause 92)
100GBASE-CR10	100 Gb/s PHY using 100GBASE-R encoding over ten lanes of shielded balanced copper cabling, with reach up to at least 7 m (see Clause 85)
100GBASE-SR4	100 Gb/s PHY using 100GBASE-R encoding over four lanes of multimode fiber, with reach up to at least 100 m (see Clause 95)
100GBASE-SR2	100 Gb/s PHY using 100GBASE-R encoding over two lanes of multimode fiber, with reach up to at least 100 m (see Clause 138)
100GBASE-SR10	100 Gb/s PHY using 100GBASE-R encoding over ten lanes of multimode fiber, with reach up to at least 100 m (see Clause 86)
100GBASE-DR	100 Gb/s PHY using 100GBASE-R encoding over single-mode fiber, with reach up to at least 500 m (see Clause 140)
100GBASE-FR1	100 Gb/s PHY using 100GBASE-R encoding over single-mode fiber, with reach up to at least 2 km (see Clause 140)
100GBASE-LR4	100 Gb/s PHY using 100GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 10 km (see Clause 88)
100GBASE-LR1	100 Gb/s PHY using 100GBASE-R encoding over single-mode fiber, with reach up to at least 10 km (see Clause 140)
100GBASE-ER4	100 Gb/s PHY using 100GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 40 km (see Clause 88)
100GBASE-ZR	100 Gb/s PHY using 100GBASE-R encoding capable of transmission over a specified channel on a defined DWDM grid in each direction of transmission with reach up to at least 80 km (see Clause 154)

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80.1.5 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. Table 80–2, Table 80–3, Table 80–4, Table 80–5, and Table 80–6 specify the correlation between nomenclature and clauses. Implementations conforming to one or more nomenclatures meet the requirements of the corresponding clauses.

Table 80–2—Nomenclature and clause correlation (40GBASE)

Nomenclature	Clause[a]																	
	28	73	74	78	81		82	83	83A	83B	84	85	86	86A	87		89	113
	Auto-Negotiation	Auto-Negotiation	BASE-R FEC	EEE	RS	XLGMII	40GBASE-R PCS	40GBASE-R PMA	XLAUI C2C	XLAUI C2M	40GBASE-KR4 PMD	40GBASE-CR4 PMD	40GBASE-SR4 PMD	XLPPI	40GBASE-LR4 PMD	40GBASE-ER4 PMD	40GBASE-FR PMD	40GBASE-T PCS/PMA
40GBASE-KR4		M	O	O	M	O	M	M	O		M							
40GBASE-CR4		M	O	O	M	O	M	M	O			M						
40GBASE-T	M			O	M	O												M
40GBASE-SR4				O	M	O	M	M	O	O			M	O				
40GBASE-FR				O	M	O	M	M	O	O							M	
40GBASE-LR4				O	M	O	M	M	O	O				O	M			
40GBASE-ER4				O	M	O	M	M	O	O						M		

[a]O = Optional, M = Mandatory.

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Table 80–3—Nomenclature and clause correlation (100GBASE copper)

Nomenclature	Clause[a]																		
	73	74	78	81		82	83	83A	83D	85	91	92	93	94	135	135D	135F	136	137
	Auto-Negotiation	BASE-R FEC	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10 C2C	CAUI-4 C2C	100GBASE-CR10 PMD	RS-FEC	100GBASE-CR4 PMD	100GBASE-KR4 PMD	100GBASE-KP4 PMD	100GBASE-P PMA	100GAUI-4 C2C	100GAUI-2 C2C	100GBASE-CR2	100GBASE-KR2
100GBASE-KR4	M		O	M	O	M	M	O	O		M		M						
100GBASE-KP4	M		O	M	O	M	O	O	O		M			M					
100GBASE-KR2	M		O	M	O	M		O	O		M				M	O	O		M
100GBASE-CR2	M		O	M	O	M		O	O		M				M	O	O	M	
100GBASE-CR4	M		O	M	O	M	M	O	O		M	M							
100GBASE-CR10	M	O	O	M	O	M	M	O	O	M									

[a]O = Optional, M = Mandatory.

Table 80–4—Nomenclature and clause correlation (100GBASE-R optical)

Nomenclature	Clause[a]														
	78	81		82	83	83A	83B	83D	83E	86	86A	88		91	95
	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10 C2C	CAUI-10 C2M	CAUI-4 C2C	CAUI-4 C2M	100GBASE-SR10 PMD	CPPI	100GBASE-LR4 PMD	100GBASE-ER4 PMD	RS-FEC	100GBASE-SR4 PMD
100GBASE-SR4	O	M	O	M	M	O	O	O	O					M	M
100GBASE-SR10	O	M	O	M	M	O	O	O	O	M	O				
100GBASE-LR4	O	M	O	M	M	O	O	O	O			M			
100GBASE-ER4	O	M	O	M	M	O	O	O	O				M		

[a]O = Optional, M = Mandatory.

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Table 80–5—Nomenclature and clause correlation (100GBASE-P optical)

Nomenclature	Clause[a]																		
	78	81		82	83	83A	83B	83D	83E	91	135	135D	135E	135F	135G	138	140		
	EEE	RS	CGMII	PCS	100GBASE-R PMA	CAUI-10 C2C	CAUI-10 C2M	CAUI-4 C2C	CAUI-4 C2M	RS-FEC	100GBASE-P PMA	100GAUI-4 C2C	100GAUI-4 C2M	100GAUI-2 C2C	100GAUI-2 C2M	100GBASE-SR2	100GBASE-DR	100GBASE-FR1	100GBASE-LR1
100GBASE-SR2	O	M	O	M	O	O	O	O	O	M	M	O	O	O	O	M			
100GBASE-DR	O	M	O	M	O	O	O	O	O	M	M	O	O	O	O		M		
100GBASE-FR1	O	M	O	M	O	O	O	O	O	M	M	O	O	O	O			M	
100GBASE-LR1	O	M	O	M	O	O	O	O	O	M	M	O	O	O	O				M

[a]O = Optional, M = Mandatory.

Table 80–6—Nomenclature and clause correlation (100GBASE-Z optical)

Nomenclature	Clause[a]																		
	78	81		82	83	83A	83B	83D	83E	91	135	135D	135E	135F	135G	152	153	154	
	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMA	CAUI-10	CAUI-10	CAUI-4	CAUI-4	RS-FEC	100GBASE-P PMA	100GAUI-4 C2C	100GAUI-4 C2M	100GAUI-2 C2C	100GAUI-2 C2M	Inverse RS-FEC	SC-FEC and 100GBASE-ZR PMA	100GBASE-ZR PMD	
100GBASE-ZR	O	M	O	M	O	O	O	O	O	O	O	O	O	O	O	C[b]	M	M	

[a] O = Optional, M = Mandatory, C = Conditional.
[b] Clause 152 inverse RS-FEC mandatory when Clause 91 RS-FEC is present.

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80.2 Summary of 40 Gigabit and 100 Gigabit Ethernet sublayers

80.2.1 Reconciliation Sublayer (RS) and Media Independent Interface

The Media Independent Interface (Clause 81) provides a logical interconnection between the MAC sublayer and the Physical Layer device (PHY). The Media Independent Interface is not intended to be physically instantiated, rather it can logically connect layers within a device.

The XLGMII supports 40 Gb/s and CGMII supports 100 Gb/s operation through its 64-bit-wide transmit and receive data paths. The Reconciliation Sublayer (RS) provides a mapping between the signals provided at the Media Independent Interface (XLGMII and CGMII) and the MAC/PLS service definition.

While XLGMII and CGMII are optional interfaces, they are used extensively in this standard as a basis for functional specification and provides a common service interface for the physical coding sublayers defined in Clause 82.

80.2.2 Physical Coding Sublayer (PCS)

The terms 40GBASE-R, 100GBASE-R, 100GBASE-P, and 100GBASE-Z refer to a specific family of Physical Layer implementations based upon the 64B/66B data coding method specified in Clause 82 and the PMA specifications defined in Clause 83, Clause 94, Clause 135, or Clause 153. Clause 82 PCSs perform encoding (decoding) of data from (to) the XLGMII/CGMII to 64B/66B code blocks, distribute the data to multiple lanes, and transfer the encoded data to the PMA or FEC.

80.2.3 Forward error correction (FEC) sublayers

A forward error correction sublayer is optional for 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10 PHYs and mandatory for 100GBASE-CR2, 100GBASE-CR4, 100GBASE-KR2, 100GBASE-KR4, 100GBASE-KP4, 100GBASE-SR2, 100GBASE-SR4, 100GBASE-DR, 100GBASE-FR1, 100GBASE-LR1, and 100GBASE-ZR PHYs. The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers.

The BASE-R FEC (see Clause 74) is instantiated for each PCS lane and operates autonomously on a per PCS lane basis. The Reed-Solomon FEC (see Clause 91) is instantiated once and requires 20 PCS lanes and 4 PMA lanes for operation. The SC-FEC (see Clause 153) is instantiated once and requires 20 PCS lanes and 20 PMA lanes for operation.

80.2.4 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS to support the use of a range of physical media. The 40GBASE-R and 100GBASE-R PMAs perform the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface, and the mapping and multiplexing of transmit and receive data streams between the PMA and PMD via the PMD service interface. In addition, the PMAs perform retiming of the received data stream when appropriate, optionally provide data loopback at the PMA or PMD service interface, and optionally provide test pattern generation and checking.

Clause 83 specifies 40GBASE-R and 100GBASE-R PMAs that may be used with any PHY type of the corresponding rate. Additional PMAs are only applicable to specific PHY types:

a) Clause 94 specifies a PMA that may be used only in a 100GBASE-KP4 PHY.
b) Clause 135 specifies a PMA that may be used in other 100GBASE-P or 100GBASE-ZR PHY types.
c) Clause 153 specifies a PMA that is used in the 100GBASE-ZR PHY.

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80.2.5 Physical Medium Dependent (PMD) sublayer

The Physical Medium Dependent sublayer is responsible for interfacing to the transmission medium. The PMD is located just above the Medium Dependent Interface (MDI). The MDI, logically subsumed within each PMD subclause, is the actual medium attachment for the various supported media.

The 40GBASE-R, 100GBASE-R, 100GBASE-P, and 100GBASE-Z PMDs and their corresponding media are specified in Clause 84 through Clause 89, Clause 92 through Clause 95, Clause 136 through Clause 138, Clause 140, and Clause 154.

80.2.6 Auto-Negotiation

Auto-Negotiation provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation.

Clause 73 Auto-Negotiation is used by the 40 Gb/s and 100 Gb/s backplane PHYs (40GBASE-KR4, 100GBASE-KR2, 100GBASE-KP4, and 100GBASE-KR4) and the 40 Gb/s and 100 Gb/s copper PHYs (40GBASE-CR4, 100GBASE-CR2, 100GBASE-CR10, and 100GBASE-CR4).

80.2.7 Management interface (MDIO/MDC)

The optional MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMDs) and Station Management (STA) entities.

80.2.8 Management

Managed objects, attributes, and actions are defined for all 40 Gigabit and 100 Gigabit Ethernet components. These items are defined in Clause 30.

80.3 Service interface specification method and notation

The service interface specification for 40GBASE-R, 100GBASE-R, and 100GBASE-P Physical Layers is as per the definition in 1.2.2. Note that the 40GBASE-R, 100GBASE-R, and 100GBASE-P inter-sublayer service interfaces use multiple scalar REQUEST and INDICATION primitives, to indicate the transfer of multiple independent streams of data units, as explained in 80.3.1 through 80.3.3.

80.3.1 Inter-sublayer service interface

The inter-sublayer service interface is described in an abstract manner and does not imply any particular implementation. The inter-sublayer service interface primitives are defined as follows:

IS_UNITDATA_*i*.request
IS_UNITDATA_*i*.indication
IS_SIGNAL.indication

The IS_UNITDATA_*i*.request (where $i = 0$ to n – 1, and n is the number of streams of data units) primitive is used to define the transfer of multiple streams of data units from a sublayer N to the next lower sublayer N – 1. The IS_UNITDATA_*i*.indication (where $i = 0$ to n – 1, and n is the number of streams of data units) primitive is used to define the transfer of multiple streams of data units from a sublayer N – 1 to the next higher sublayer N. The IS_SIGNAL.indication primitive is used to define the transfer of signal status from a sublayer N – 1 to the next higher sublayer N.

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If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78, 78.1.3.3.1), then the inter-sublayer service interface includes five additional primitives defined as follows:

IS_TX_MODE.request
IS_RX_MODE.request
IS_ENERGY_DETECT.indication
IS_RX_LPI_ACTIVE.request
IS_RX_TX_MODE.indication

The IS_TX_MODE.request primitive is used to communicate the state of the PCS LPI transmit function to other sublayers in the PHY. The IS_RX_MODE.request primitive is used to communicate the state of the PCS LPI receive function to other sublayers. The IS_RX_TX_MODE.indication primitive is used to communicate the state of the rx_tx_mode parameter that reflects the inferred state of the link partner's tx_mode parameter from the PMA to other sublayers. The IS_RX_LPI_ACTIVE.request primitive is used to communicate to the BASE-R FEC (see Clause 74) that the PCS has detected LPI signaling. This allows the BASE-R FEC to use rapid block lock; the RS-FEC (see Clause 91) does not use this signal. The IS_ENERGY_DETECT.indication primitive is used to communicate that the PMD has detected the return of energy on the interface following a period of quiescence.

80.3.2 Instances of the Inter-sublayer service interface

The inter-sublayer interface can be instantiated between different sublayers, hence a prefix notation is defined to identify a specific instance of an inter-sublayer service interface. The following prefixes are defined:

a) PMD:—for primitives issued on the interface between the PMD sublayer and the PMA sublayer called the PMD service interface.
b) PMA:—for primitives issued on the interface between the PMA sublayer and the PCS (or the FEC) sublayer called the PMA service interface.
c) FEC:—for primitives issued on the interface between the FEC sublayer and the PCS (or the PMA) sublayer called the FEC service interface.
d) IFEC:—for primitives issued on the interface between the Inverse FEC sublayer and the PMA sublayer called the Inverse FEC service interface.

Examples of inter-sublayer service interfaces for 40GBASE-R, 100GBASE-R, 100GBASE-P, and 100GBASE-Z with their corresponding instance names are illustrated in Figure 80–2, Figure 80–3, Figure 80–4, Figure 80–5, and Figure 80–6. For example, the primitives for one instance of the inter-sublayer service interface, named the PMD service interface, are identified as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication.

Primitives for other instances, of inter-sublayer interfaces, are represented in a similar manner as described above.

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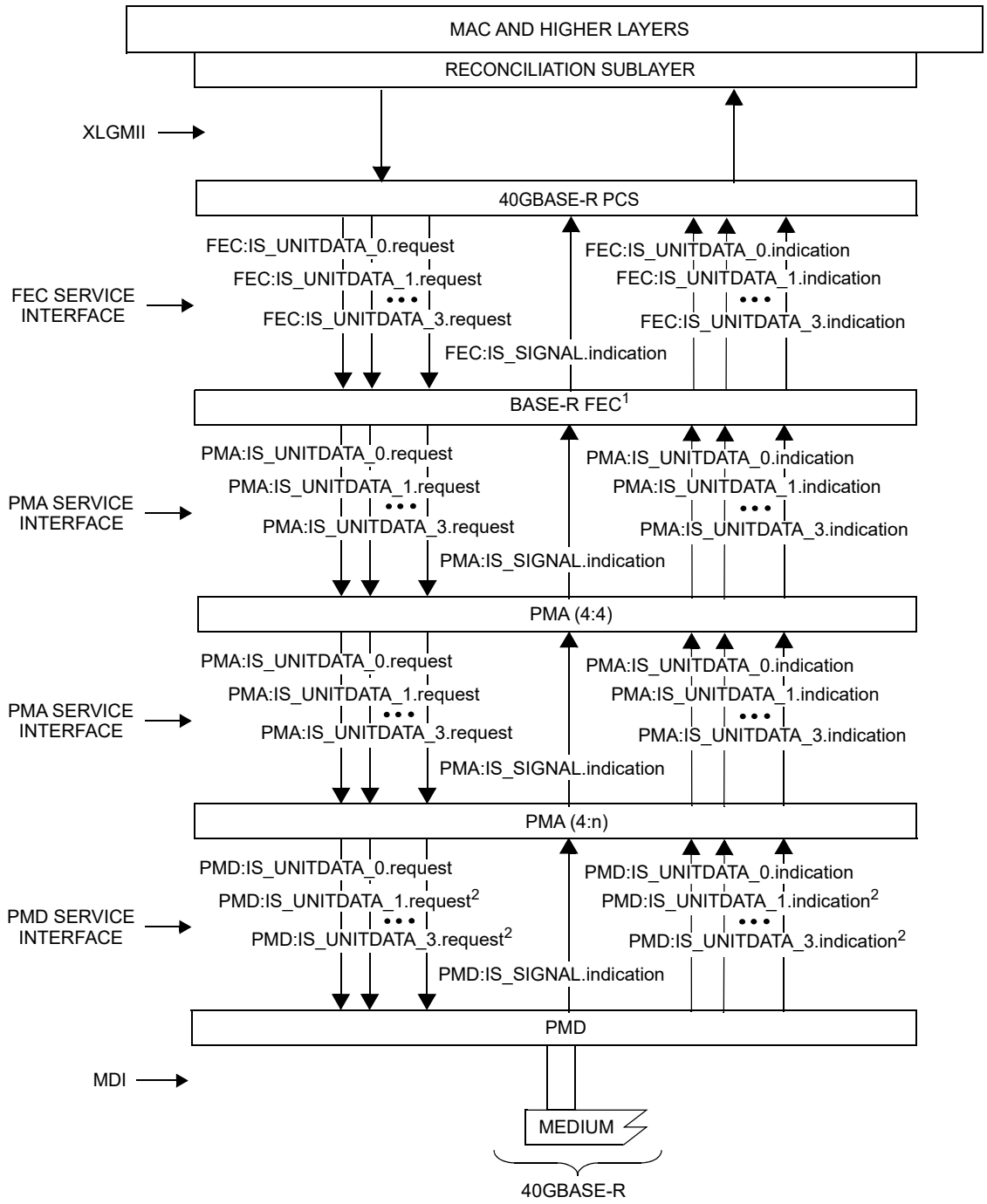

FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE
n = NUMBER OF PARALLEL STREAMS OF DATA UNITS

NOTE 1—OPTIONAL OR OMITTED DEPENDING ON PHY TYPE
NOTE 2—DOES NOT EXIST FOR 40GBASE-FR PMD

Figure 80–2—40GBASE-R inter-sublayer service interfaces

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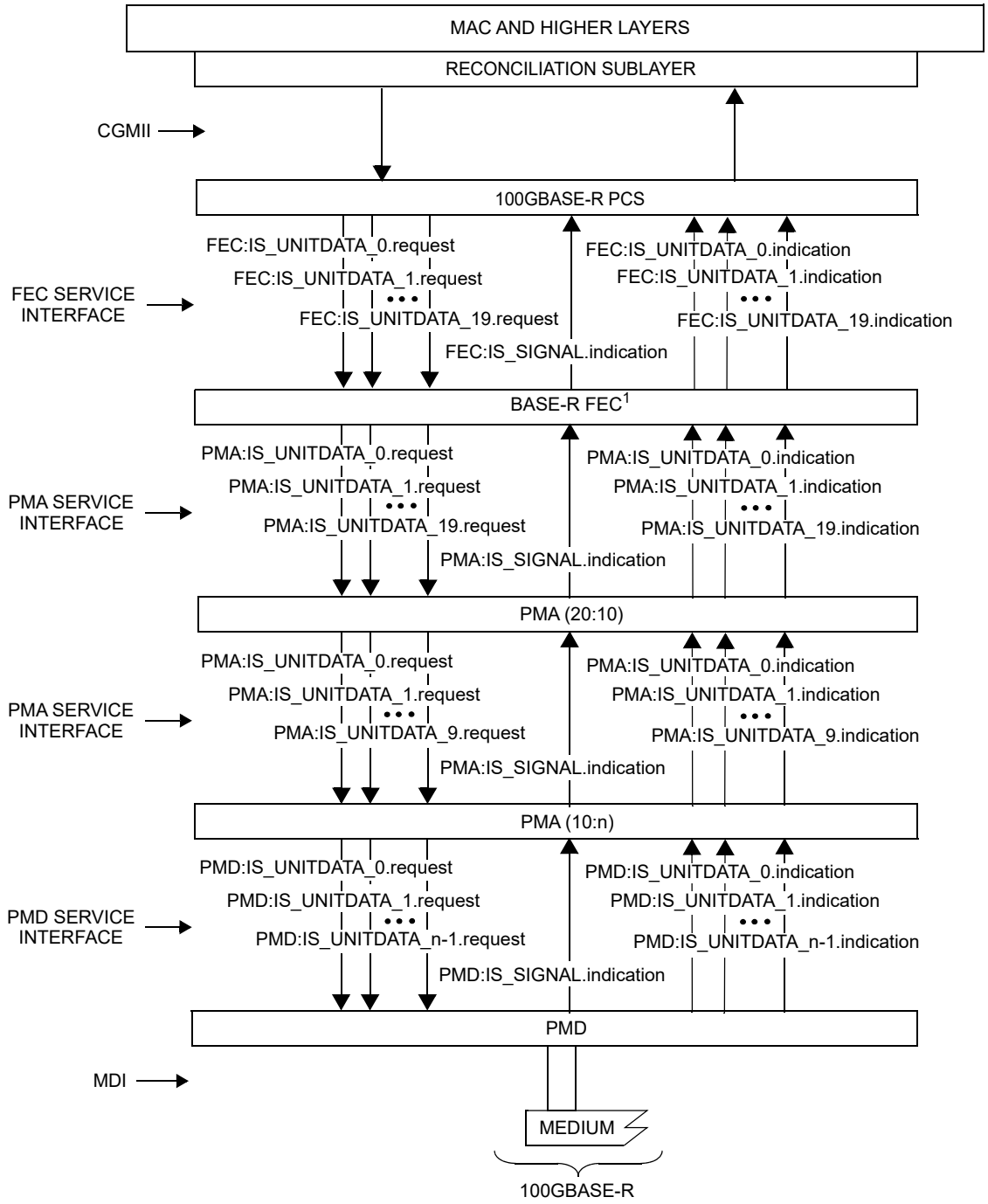

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = NUMBER OF PARALLEL STREAMS OF DATA UNITS

NOTE 1—OPTIONAL OR OMITTED DEPENDING ON PHY TYPE

Figure 80–3—100GBASE-R inter-sublayer service interfaces

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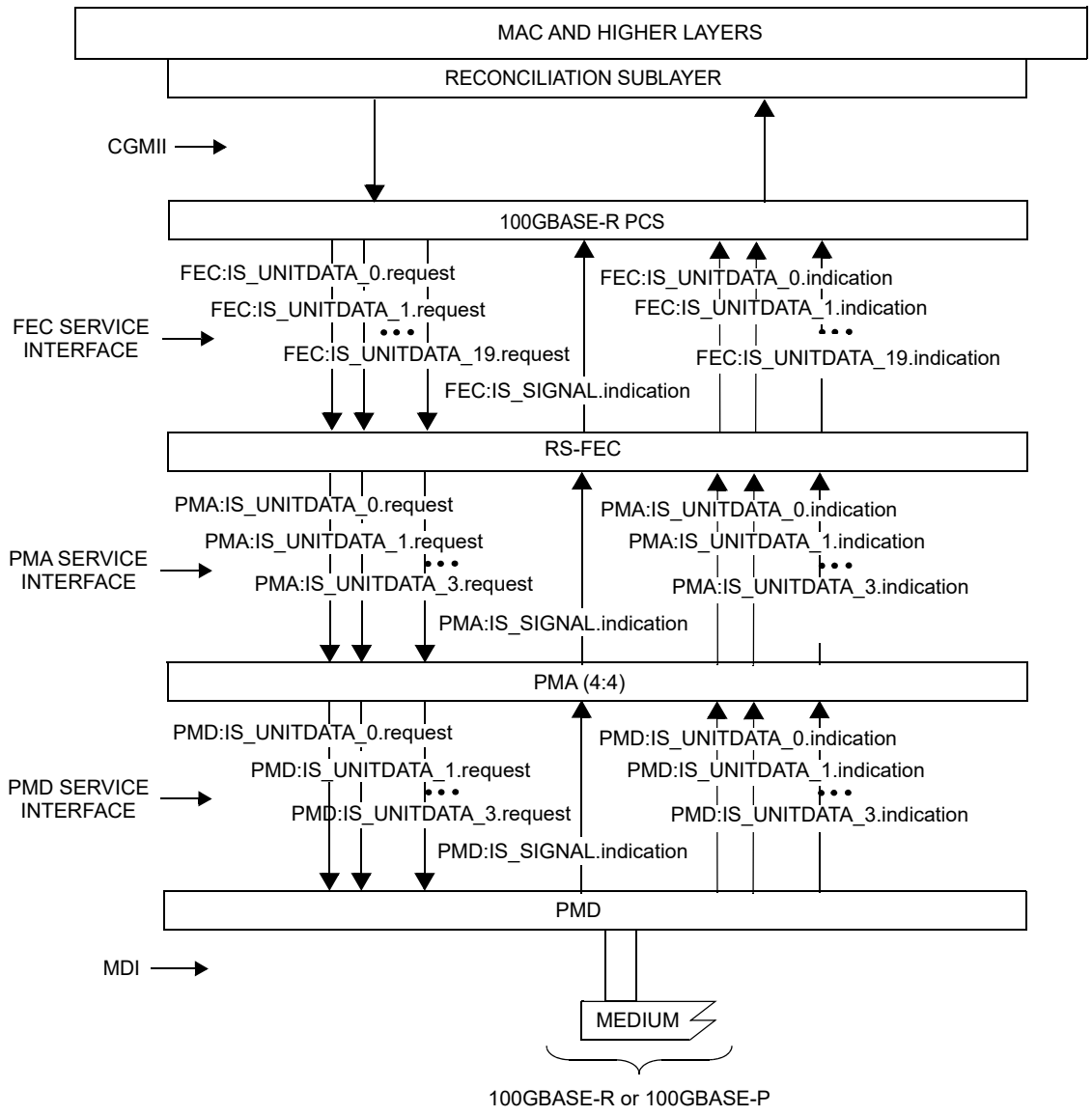

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 80–4—100GBASE-R and 100GBASE-P inter-sublayer service interfaces with RS-FEC

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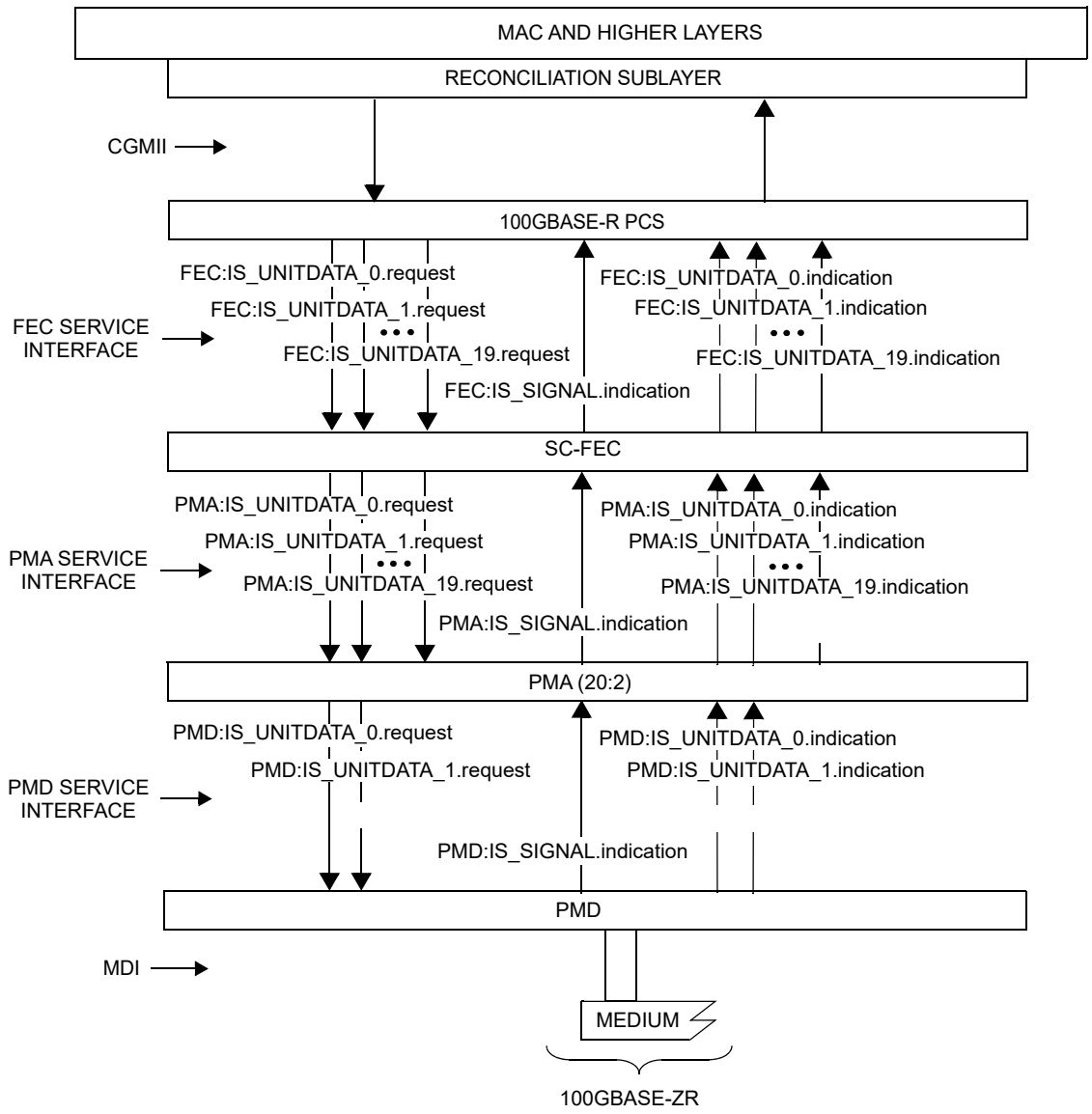

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
SC-FEC = STAIRCASE FORWARD ERROR CORRECTION

Figure 80–5—100GBASE-Z inter-sublayer service interfaces with SC-FEC

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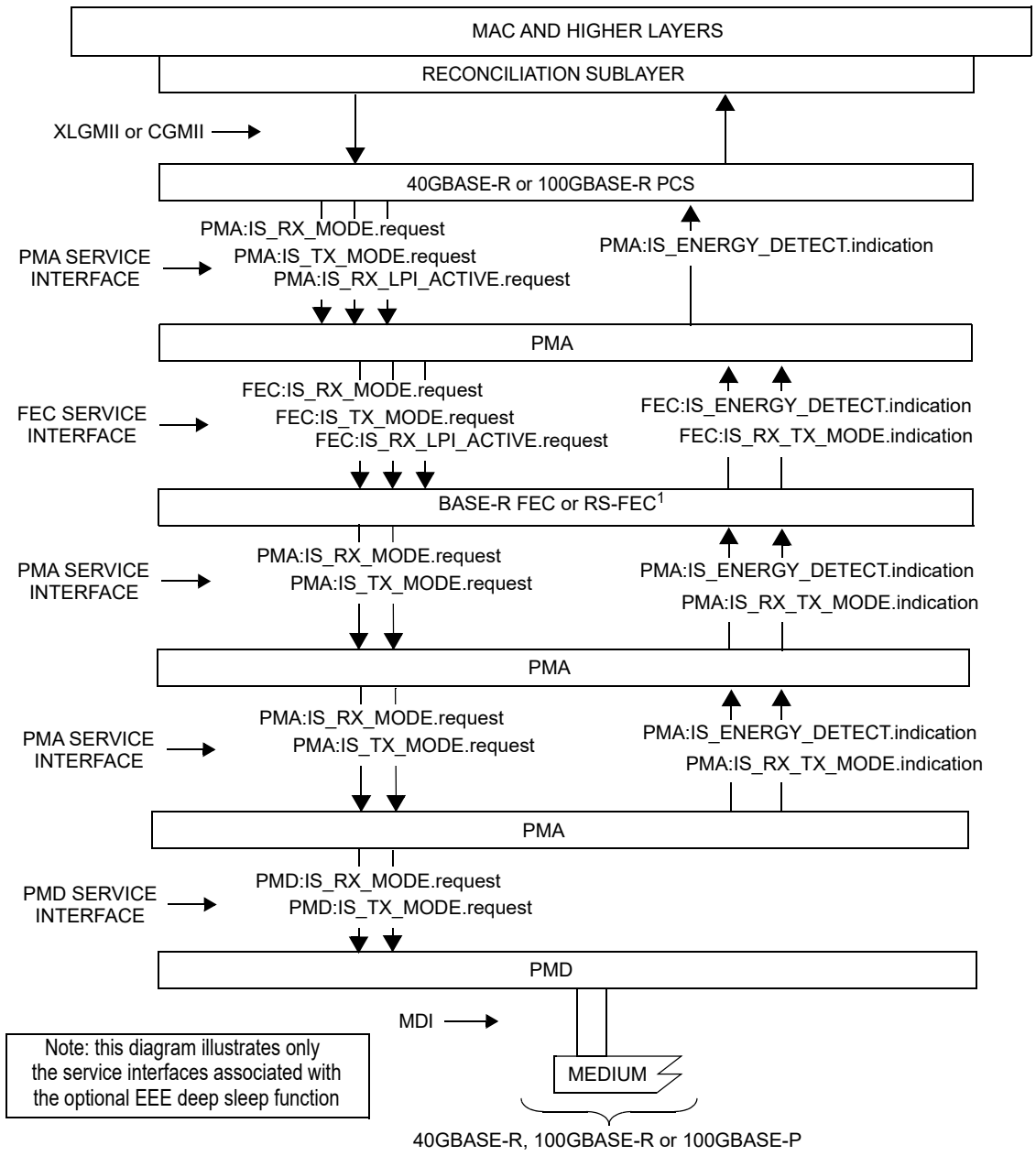

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 80–6—Optional inter-sublayer service interfaces for EEE deep sleep support

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80.3.3 Semantics of inter-sublayer service interface primitives

The semantics of the inter-sublayer service interface primitives for the 40GBASE-R and 100GBASE-R sublayers are described in 80.3.3.1 through 80.3.3.3.

80.3.3.1 IS_UNITDATA_*i*.request

The IS_UNITDATA_*i*.request (where i = 0 to n – 1) primitive is used to define the transfer of multiple streams of data units from a sublayer N to the next lower sublayer N – 1, where n is the number of parallel streams of data units.

80.3.3.1.1 Semantics of the service primitive

```
IS_UNITDATA_0.request(tx_bit)
IS_UNITDATA_1.request(tx_bit)
...
IS_UNITDATA_n–1.request(tx_bit)
```

The data conveyed by IS_UNITDATA_0.request to IS_UNITDATA_n–1.request consists of n parallel continuous streams of encoded bits, one stream for each lane. Each of the tx_bit parameters can take one of two values: one or zero.

80.3.3.1.2 When generated

The sublayer N continuously sends n parallel bit streams IS_UNITDATA_*i*.request(tx_bit) to the next lower sublayer N – 1, each at a nominal signaling rate defined by a specific instance of the inter-sublayer service interface.

80.3.3.1.3 Effect of receipt

The effect of receipt of this primitive is defined by the sublayer that receives this primitive.

80.3.3.2 IS_UNITDATA_*i*.indication

The IS_UNITDATA_*i*.indication (where i = 0 to n – 1) primitive is used to define the transfer of multiple streams of data units from the sublayer N – 1 to the next higher sublayer N, where n is the number of parallel streams of data units.

80.3.3.2.1 Semantics of the service primitive

```
IS_UNITDATA_0.indication(rx_bit)
IS_UNITDATA_1.indication(rx_bit)
...
IS_UNITDATA_n–1.indication(rx_bit)
```

The data conveyed by IS_UNITDATA_0.indication to IS_UNITDATA_n–1.indication consists of n parallel continuous streams of encoded bits, one stream for each lane. Each of the rx_bit parameters can take one of two values: one or zero.

80.3.3.2.2 When generated

The sublayer N–1 continuously sends n parallel bit streams IS_UNITDATA_*i*.indication(rx_bit) to the next higher sublayer N, each at a nominal signaling rate defined by a specific instance of the inter-sublayer service interface.

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80.3.3.2.3 Effect of receipt

The effect of receipt of this primitive is defined by the sublayer that receives this primitive.

80.3.3.3 IS_SIGNAL.indication

The IS_SIGNAL.indication primitive is generated by the sublayer N – 1 to the next higher sublayer N to indicate the status of the receive process. This primitive is generated by the receive process to propagate the detection of severe error conditions (e.g., no valid signal being received by the sublayer that generates this primitive) to the next higher sublayer N.

80.3.3.3.1 Semantics of the service primitive

IS_SIGNAL.indication(SIGNAL_OK)

The SIGNAL_OK parameter can take on one of two values: OK or FAIL. A value of FAIL denotes that invalid data is being presented (rx_bit parameters undefined) by the sublayer N – 1 to the next higher sublayer N. A value of OK does not guarantee valid data is being presented by the sublayer N – 1 to the next higher sublayer N.

80.3.3.3.2 When generated

The sublayer N – 1 generates the IS_SIGNAL.indication primitive to the next higher sublayer N whenever there is change in the value of the SIGNAL_OK parameter.

80.3.3.3.3 Effect of receipt

The effect of receipt of this primitive is defined by the sublayer that receives this primitive.

80.3.3.4 IS_TX_MODE.request

The IS_TX_MODE.request primitive communicates the tx_mode parameter generated by the PCS Transmit Process for EEE capability to invoke the appropriate PMA, FEC, and PMD transmit EEE states. Without EEE deep sleep mode capability, the primitive is never invoked and the sublayers behave as if tx_mode = DATA.

80.3.3.4.1 Semantics of the service primitive

IS_TX_MODE.request(tx_mode)

The tx_mode parameter takes on one of up to three values: DATA, QUIET, or ALERT.

80.3.3.4.2 When generated

This primitive is generated to indicate the low power mode of the transmit path.

80.3.3.4.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the sublayer that receives this primitive. In general, when tx_mode is DATA the sublayer operates normally and when tx_mode is QUIET, the sublayer may go into a low power mode.

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80.3.3.5 IS_RX_MODE.request

The IS_RX_MODE.request primitive communicates the rx_mode parameter generated by the PCS LPI receive function to other sublayers. Without EEE deep sleep mode capability, the primitive is never invoked and the sublayers behave as if rx_mode = DATA.

80.3.3.5.1 Semantics of the service primitive

IS_RX_MODE.request(rx_mode)

The rx_mode parameter takes on one of two values: DATA or QUIET.

80.3.3.5.2 When generated

This primitive is generated to indicate the state of the PCS LPI receive function.

80.3.3.5.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the sublayer that receives this primitive. In general, when rx_mode is DATA the sublayer operates normally and when rx_mode is QUIET, the sublayer may go into a low power mode.

80.3.3.6 IS_RX_LPI_ACTIVE.request

The IS_RX_LPI_ACTIVE.request primitive communicates to the FEC that the PCS LPI receive function is active. This primitive may be passed through a PMA sublayer but has no effect on that sublayer. This primitive is only used for a PMA sublayer that is between the PCS and a Clause 74 FEC sublayer; in all other cases the primitive is never invoked and has no effect. Without EEE deep sleep mode capability, the primitive is never invoked and has no effect.

80.3.3.6.1 Semantics of the service primitive

IS_RX_LPI_ACTIVE.request(rx_lpi_active)

The parameter rx_lpi_active is Boolean.

80.3.3.6.2 When generated

This primitive is generated to indicate the state of the PCS LPI receive function. It is FALSE when in the RX_ACTIVE state and TRUE in all other states.

80.3.3.6.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the FEC sublayer that receives this primitive. When rx_lpi_active is true the FEC sublayer uses rapid block lock to reestablish FEC operation following a period of quiescence.

80.3.3.7 IS_ENERGY_DETECT.indication

The IS_ENERGY_DETECT.indication primitive is used to communicate that the PMD has detected the return of energy on the interface following a period of quiescence. Without EEE deep sleep mode capability, the primitive is never invoked and has no effect.

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80.3.3.7.1 Semantics of the service primitive

IS_ENERGY_DETECT.indication(energy_detect)

The parameter energy_detect is Boolean.

80.3.3.7.2 When generated

This primitive is generated by the PMA, reflecting the state of the signal_detect parameter received from the PMD.

80.3.3.7.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the PCS sublayer that receives this primitive. This parameter is used to indicate that activity has returned on the interface following a period of quiescence.

80.3.3.8 IS_RX_TX_MODE.indication

The IS_RX_TX_MODE.indication primitive communicates the rx_tx_mode parameter. This parameter indicates the value of tx_mode that the PMA sublayer has inferred from the received signal. Without EEE deep sleep capability, the primitive is never generated and the sublayers behave as if rx_tx_mode=DATA.

80.3.3.8.1 Semantics of the service primitive

IS_RX_TX_MODE.indication(rx_tx_mode)

The parameter rx_tx_mode is assigned one of the following values: DATA, QUIET, or ALERT.

80.3.3.8.2 When generated

This primitive is generated whenever there is change in the value of the rx_tx_mode parameter.

80.3.3.8.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the sublayer that receives it.

80.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. Table 80–7 contains the values of maximum sublayer delay (sum of transmit and receive delays at one end of the link) in bit times as specified in 1.4 and pause_quanta as specified in 31B.2. If a PHY contains an Auto-Negotiation sublayer, the delay of the Auto-Negotiation sublayer is included within the delay of the PMD and medium.

Equation (80–1) specifies the calculation of cable delay in nanoseconds per meter of fiber or electrical cable, based upon the parameter *n*, which represents the ratio of the speed of electromagnetic propagation in the fiber or electrical cable to the speed of light in a vacuum, $c = 3 \times 10^8$ m/s.

$$\text{cable delay} = \frac{10^9}{nc} \text{ ns/m} \quad (80–1)$$

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The value of *n* should be available from the fiber or electrical cable manufacturer; but if no value is known, then a conservative delay estimate can be calculated using a default value of $n = 0.66$, which yields a default cable delay of 5 ns/m.

See 31B.3.7 for PAUSE reaction timing constraints for stations at operating speeds of 40 Gb/s and 100 Gb/s.

Table 80–7—Sublayer delay constraints

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
40G MAC, RS, and MAC Control	16 384	32	409.6	See 81.1.4.
40GBASE-R PCS	11 264	22	281.6	See 82.5.
40GBASE-R FEC	24 576	48	614.4	See 74.6.
40GBASE-R PMA	4 096	8	102.4	See 83.5.4.
40GBASE-T PHY	25 600	50	640	See 113.11
40GBASE-KR4 PMD	2 048	4	51.2	Includes delay of one direction through backplane medium. See 84.4.
40GBASE-CR4 PMD	4 096	8	102.4	Does not include delay of cable medium. See 85.4.
40GBASE-SR4 PMD	1 024	2	25.6	Includes 2 m of fiber. See 86.3.1.
40GBASE-FR PMD	1 024	2	25.6	Includes 2 m of fiber. See 89.3.1.
40GBASE-LR4 PMD	1 024	2	25.6	Includes 2 m of fiber. See 87.3.1.
40GBASE-ER4 PMD	1 024	2	25.6	Includes 2 m of fiber. See 87.3.1.
100G MAC, RS, and MAC Control	24 576	48	245.76	See 81.1.4.
100GBASE-R PCS	35 328	69	353.28	See 82.5.
100GBASE-R FEC	122 880	240	1 228.8	See 74.6.
100GBASE-R RS-FEC	40 960	80	409.60	See 91.4.
Inverse RS-FEC	40 960	80	409.60	See 152.4.
SC-FEC	1 827 840	3570	18 278.40	See 153.2.2.
100GBASE-R PMA	9 216	18	92.16	See 83.5.4.
100GBASE-P PMA	9 216	18	92.16	See 135.5.4.
100GBASE-KR2 PMD	4 096	8	40.96	Includes allocation of 20 ns for one direction through backplane medium. See 137.5.
100GBASE-KR4 PMD	2 048	4	20.48	Includes delay of one direction through backplane medium. See 93.4.
100GBASE-KP4 PMA/PMD	8 192	16	81.92	Includes delay of one direction through backplane medium. See 94.2.5.

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Table 80–7—Sublayer delay constraints *(continued)*

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
100GBASE-CR2 PMD	4 096	8	40.96	Includes allocation for 20 ns for one direction through cable medium. See 136.5.
100GBASE-CR4 PMD	2 048	4	20.48	Does not include delay of cable medium. See 92.4.
100GBASE-CR10 PMD	9 728	19	97.28	Does not include delay of cable medium. See 85.4.
100GBASE-SR4 PMD	2 048	4	20.48	Includes 2 m of fiber. See 95.3.1.
100GBASE-SR2 PMD	2 048	4	20.48	Includes 2 m of fiber. See 138.3.
100GBASE-SR10 PMD	2 048	4	20.48	Includes 2 m of fiber. See 86.3.1.
100GBASE-DR PMD	2 048	4	20.48	Includes 2 m of fiber. See 140.3.
100GBASE-FR1 PMD	2 048	4	20.48	Includes 2 m of fiber. See 140.3.
100GBASE-LR4 PMD	2 048	4	20.48	Includes 2 m of fiber. See 88.3.1.
100GBASE-LR1 PMD	2 048	4	20.48	Includes 2 m of fiber. See 140.3.
100GBASE-ER4 PMD	2 048	4	20.48	Includes 2 m of fiber. See 88.3.1.
100GBASE-ZR PMD	2 048	4	20.48	Includes 2 m of fiber. See 154.3.1.

[a] For 40GBASE-R, 1 bit time (BT) is equal to 25 ps and for 100GBASE-R, 1 bit time (BT) is equal to 10 ps. (See 1.4.215 for the definition of bit time.)
[b] For 40GBASE-R, 1 pause_quantum is equal to 12.8 ns and for 100GBASE-R, 1 pause_quantum is equal to 5.12 ns. (See 31B.2 for the definition of pause_quanta.)
[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

80.5 Skew constraints

Skew (or relative delay) can be introduced between lanes by both active and passive elements of a 40GBASE-R or 100GBASE-R link. Skew is defined as the difference between the times of the earliest PCS lane and latest PCS lane for the one to zero transition of the alignment marker sync bits. The PCS deskew function (see 82.2.13) compensates for all lane-to-lane Skew observed at the receiver. The Skew between the lanes is kept within limits as shown in Table 80–8 so that the transmitted information on the lanes can be reassembled by the receive PCS.

Skew Variation may be introduced due to variations in electrical, thermal or environmental characteristics. Skew Variation is defined as the change in Skew between any PCS lane and any other PCS lane over the entire time that the link is in operation. From the time the link is brought up, Skew Variation is limited to ensure that each PCS lane always traverses the same lane between any pair of adjacent sublayers while the link remains in operation.

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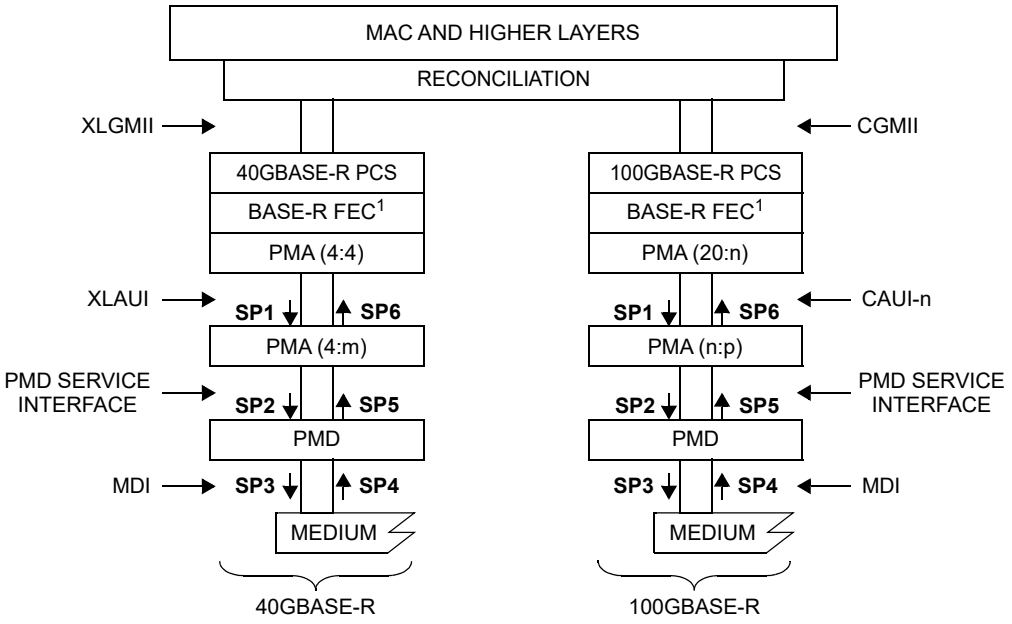

CAUI-n = 100 Gb/s ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

m = 1 or 4
n = 4 or 10
p = 4 or 10
NOTE1—CONDITIONAL BASED ON PHY TYPE

Figure 80–7—40GBASE-R and 100GBASE-R Skew points for single XLAUI or CAUI-n

The maximum Skew and Skew Variation at physically instantiated interfaces is specified at Skew points SP1, SP2, and SP3 for the transmit direction and SP4, SP5, and SP6 for the receive direction as illustrated in Figure 80–7 (single XLAUI or CAUI-n interface) and Figure 80–8 (multiple XLAUI or CAUI-n interfaces).

In the transmit direction, the Skew points are defined in the following locations:

— SP1 on the XLAUI/CAUI-n interface, at the input of the PMA closest to the PMD;
— SP2 on the PMD service interface, at the input of the PMD;
— SP3 at the output of the PMD, at the MDI.

In the receive direction, the Skew points are defined in the following locations:

— SP4 at the MDI, at the input of the PMD;
— SP5 on the PMD service interface, at the output of the PMD;
— SP6 on the XLAUI/CAUI-n interface, at the output of the PMA closest to the PCS.

The allowable limits for Skew are shown in Table 80–8 and the allowable limits for Skew Variation are shown in Table 80–9.

The skew points are similarly illustrated for a PHY incorporating RS-FEC (see Clause 91) in Figure 80–9.

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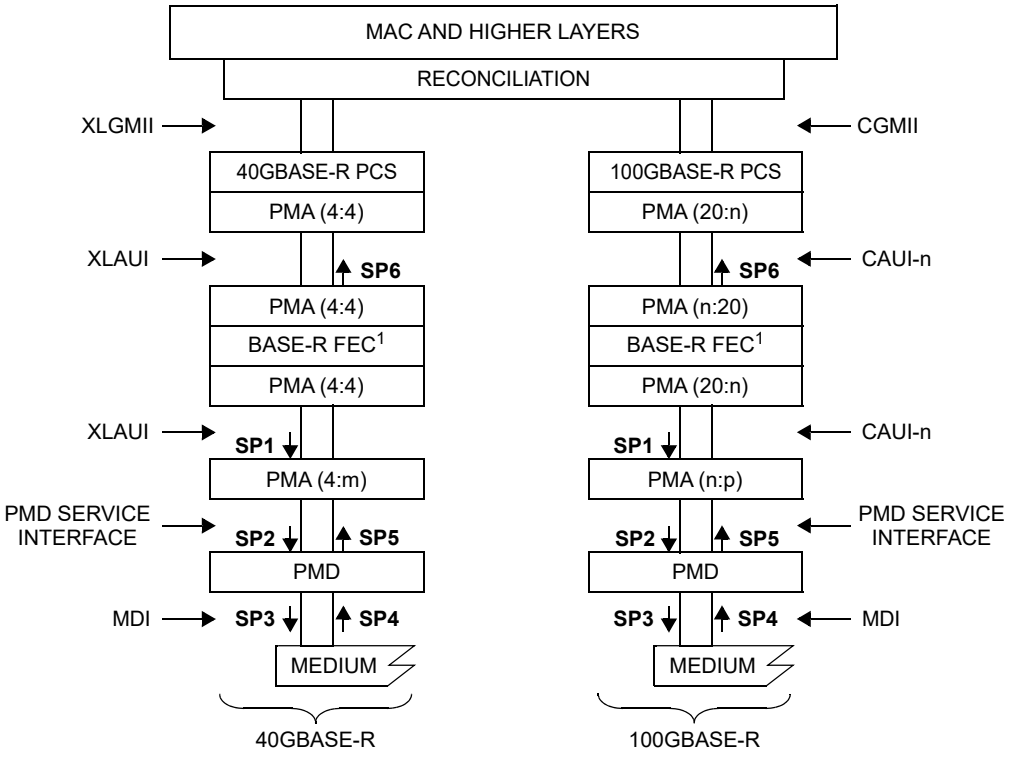

CAUI-n = 100 Gb/s ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

m = 1 or 4
n = 4 or 10
p = 4 or 10
NOTE1—CONDITIONAL BASED ON PHY TYPE

Figure 80–8—40GBASE-R and 100GBASE-R Skew points for multiple XLAUI or CAUI-n

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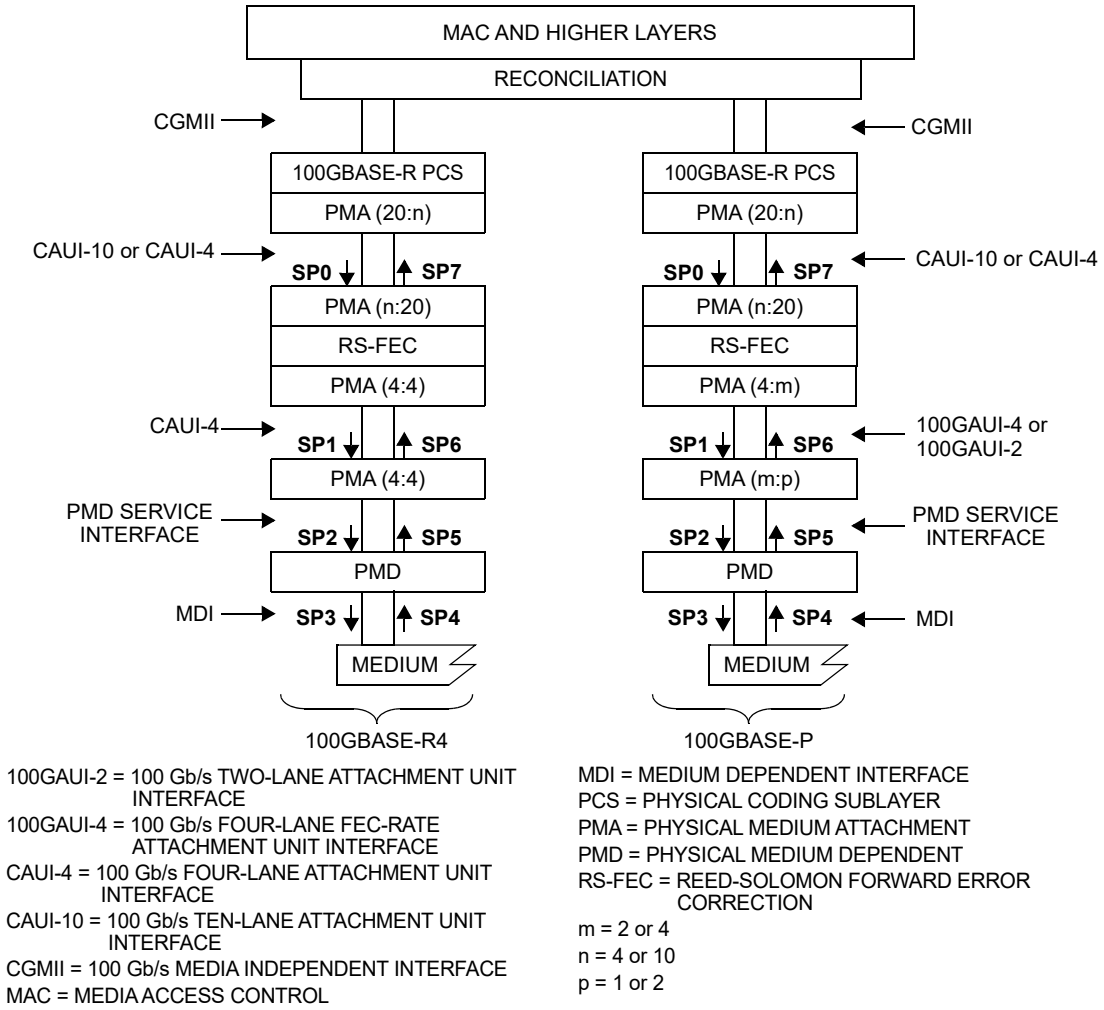

Figure 80–9—100GBASE-R Skew points with RS-FEC, CAUI-n, and 100GAUI-n

The Skew requirements for the PCS, PMA and PMD sublayers are specified in the respective clauses as noted in Table 80–8 and Table 80–9.

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Table 80–8—Summary of Skew constraints

Skew points	Maximum Skew (ns)[a]	Maximum Skew for 40GBASE-R PCS lane (UI)[b]	Maximum Skew for 100GBASE-R PCS lane (UI)[c]	Notes[d]
SP0	29	N/A	≈ 150	See 83.5.3.1 or 135.5.3
SP1	29	≈ 299	≈ 150	See 83.5.3.2 or 135.5.3
SP2	43	≈ 443	≈ 222	See 83.5.3.4, 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, 95.3.2, 135.5.3, 136.6, 137.6, 138.3, 140.3, or 154.3.2
SP3	54	≈ 557	≈ 278	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, 95.3.2, 135.5.3, 136.6, 137.6, 138.3, 140.3, or 154.3.2
SP4	134	≈ 1382	≈ 691	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, 95.3.2 135.5.3, 136.6, 137.6, 138.3, 140.3, or 154.3.2
SP5	145	≈ 1495	≈ 748	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, 95.3.2, 135.5.3, 136.6, 137.6, 138.3, 140.3, or 154.3.2
SP6	160	≈ 1649	≈ 824	See 83.5.3.6 or 135.5.3
SP7	29	N/A	≈ 150	See 83.5.3.8 or 135.5.3
At PCS receive	180	≈ 1856	≈ 928	See 82.2.13
At RS-FEC transmit	49	N/A	≈ 253	See 91.5.2.2
At RS-FEC receive[e]	180	N/A	≈ 4641	See 91.5.3.1
At PCS receive (with RS-FEC)	49	N/A	≈ 253	See 82.2.13

[a]The Skew limit includes 1 ns allowance for PCB traces that are associated with the Skew points.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew in UI for 40GBASE-R, based on 1 UI equals 96.969697 ps at PCS lane signaling rate of 10.3125 GBd.
[c]The symbol ≈ indicates approximate equivalent of maximum Skew in UI for 100GBASE-R, based on 1 UI equals 193.939394 ps at PCS lane signaling rate of 5.15625 GBd.
[d]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.
[e]The skew at the RS-FEC receive is the skew between RS-FEC lanes. The symbol ≈ indicates approximate equivalent of maximum Skew in UI for RS-FEC lanes with a signaling rate of 25.78125 GBd.

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Table 80–9—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation				Notes[a]
	ns	UI for 10.3125 GBd lane[b]	UI for 25.78125 GBd lane[c]	UI for 26.5625 GBd lane[d]	
SP0	0.2	≈ 2	≈ 5	N/A	See 83.5.3.1 or 135.5.3
SP1	0.2	≈ 2	≈ 5	≈ 5	See 83.5.3.2 or 135.5.3
SP2	0.4	≈ 4	≈ 10	≈ 11	See 83.5.3.4, 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, 95.3.2, 135.5.3, 136.6, 137.6, or 138.3
SP3	0.6	≈ 6	≈ 15	≈ 16	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, 95.3.2, 136.6, 137.6, or 138.3
SP4	3.4	≈ 35	≈ 88	≈ 90	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, or 95.3.2, 136.6, 137.6, or 138.3
SP5	3.6	≈ 37	≈ 93	≈ 96	See 84.5, 85.5, 86.3.2, 87.3.2, 88.3.2, 89.3.2, 92.5, 93.5, 94.3.4, 95.3.2, 135.5.3, 136.6, 137.6, 138.3
SP6	3.8	≈ 39	≈ 98	≈ 101	See 83.5.3.6 or 135.5.3
SP7	0.2	≈ 2	N/A	N/A	See 83.5.3.8 or 135.5.3
At PCS receive	4	≈ 41	N/A	N/A	See 82.2.13
At RS-FEC transmit	0.4	N/A	≈ 10	≈ 11	See 91.5.2.2
At RS-FEC receive[e]	4	N/A	≈ 103	≈ 106	See 91.5.3.1
At PCS receive (with RS-FEC)	0.4	N/A	≈ 10	N/A	See 82.2.13

[a]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI for 40GBASE-R, based on 1 UI equals 96.969697 ps at PMD lane signaling rate of 10.3125 GBd.
[c]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI for 100GBASE-R, based on 1 UI equals 38.787879 ps at PMD lane signaling rate of 25.78125 GBd.
[d]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI for 100GBASE-R, based on 1 UI equals 37.64706 ps at PMD lane signaling rate of 26.5625 GBd.
[e]The skew at the RS-FEC receive is the skew between RS-FEC lanes.

80.6 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

Multiple states of a function that have a transition to a common state utilizing different qualifiers (for example, multiple exit conditions to an IDLE or WAIT state) may be indicated by a shared arrow. An exit

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transition arrow connects to the shared arrow, and the qualifier is met prior to termination of the transition arrow on the shared arrow. The shared arrow has no qualifier.

80.7 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 45, Clause 73, Clause 74, Clause 81 through Clause 89, Clause 91 through Clause 95, Clause 135 through Clause 138, Clause 140, Clause 152 through Clause 154, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the 40 Gigabit and 100 Gigabit Ethernet PICS conforms to the same notation and conventions used in 21.6.

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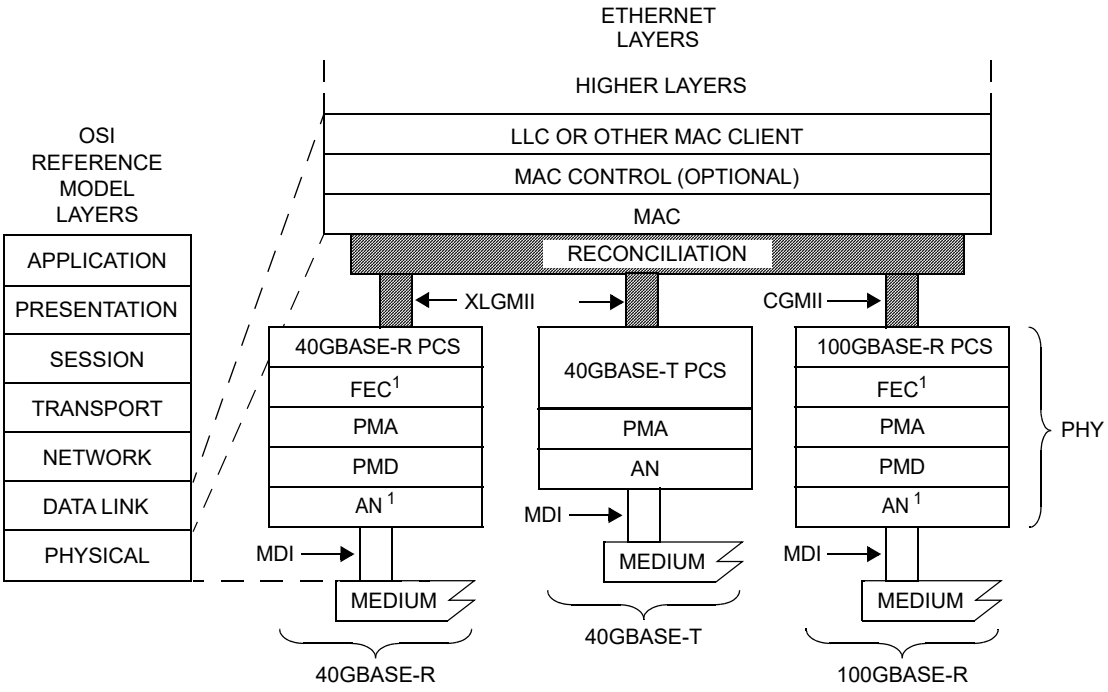
81. Reconciliation Sublayer (RS) and Media Independent Interface for 40 Gb/s and 100 Gb/s operation (XLGMII and CGMII)

81.1 Overview

This clause defines the characteristics of the Reconciliation Sublayer (RS) and the Media Independent Interface between Ethernet media access controllers and various PHYs. Figure 81–1 shows the relationship of the RS and Media Independent Interface to the ISO/IEC OSI reference model. Note that there are two variants of the Media Independent Interface in this clause, the 40 Gb/s Media Independent Interface (XLGMII) and the 100 Gb/s Media Independent Interface (CGMII).



AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 81–1—RS and MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The XLGMII and the CGMII are optional logical interfaces between the MAC sublayer and the Physical Layer device (PHY).

The RS adapts the bit serial protocols of the MAC to the parallel format of the PCS service interface. Though the XLGMII/CGMII is an optional interface, it is used in this standard as a basis for specification. The Physical Coding Sublayer (PCS) is specified to the XLGMII/CGMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and XLGMII/CGMII were implemented.

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The XLGMII/CGMII has the following characteristics:

a) The XLGMII supports a speed of 40 Gb/s.
b) The CGMII supports a speed of 100 Gb/s.
c) Data and delimiters are synchronous to a clock reference.
d) It provides independent 64-bit wide transmit and receive data paths.
e) It supports full duplex operation only.

81.1.1 Summary of major concepts

The following are the major concepts of the XLGMII/CGMII:

a) The XLGMII/CGMII is functionally similar to other media independent interfaces that have been defined for lower speeds, as they all define an interface allowing independent development of MAC and PHY logic.
b) The RS converts between the MAC serial data stream and the parallel data paths of the XLGMII/CGMII.
c) The RS maps the signal set provided at the XLGMII/CGMII to the PLS service primitives provided at the MAC.
d) Each direction of data transfer is independent and serviced by data, control, and clock signals.
e) The RS generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.
f) The RS participates in link fault detection and reporting by monitoring the receive path for status reports that indicate an unreliable link, and generating status reports on the transmit path to report detected link faults to the DTE on the remote end of the connecting link.
g) The XLGMII and CGMII may also support Low Power Idle (LPI) signaling for PHY types supporting Energy Efficient Ethernet (EEE) (see Clause 78).

81.1.2 Application

This clause applies to the interface between the MAC and PHY. This logical interface is used to provide media independence so that an identical media access controller may be used with supported PHY types.

81.1.3 Rate of operation

The XLGMII is specified to support 40 Gb/s operation and the CGMII is specified to support 100 Gb/s operation.

81.1.4 Delay constraints

The maximum cumulative MAC Control, MAC, and RS delay (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 81–1. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

81.1.5 Allocation of functions

The allocation of functions at the XLGMII/CGMII balances the need for media independence with interface simplicity. The XLGMII and CGMII maximize media independence by separating the Data Link and Physical Layers of the OSI seven-layer reference model.

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Table 81–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
40 Gb/s MAC, RS, and MAC Control	16384	32	409.6
100 Gb/s MAC, RS, and MAC Control	24576	48	245.76

81.1.6 XLGMII/CGMII structure

The XLGMII/CGMII is composed of independent transmit and receive paths. Each direction uses 64 data signals (TXD<63:0> and RXD<63:0>), 8 control signals (TXC<7:0> and RXC<7:0>), and a clock (TX_CLK and RX_CLK). Figure 81–2 depicts a schematic view of the RS inputs and outputs.

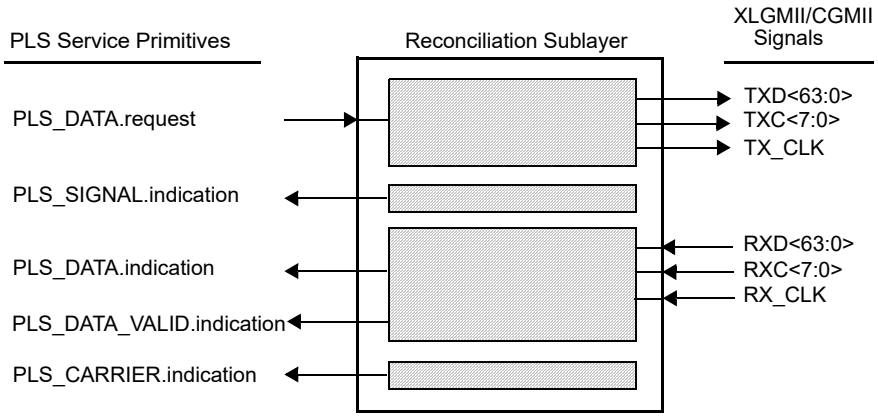

Figure 81–2—Reconciliation Sublayer (RS) inputs and outputs

The 64 TXD and 8 TXC signals shall be organized into eight data lanes, as shall the 64 RXD and 8 RXC signals (see Table 81–2). The eight lanes in each direction share a common clock, TX_CLK for transmit and RX_CLK for receive. The eight lanes are used in round-robin sequence to carry an octet stream. On transmit, each eight PLS_DATA.request transactions represent an octet transmitted by the MAC. The first octet is aligned to lane 0, the second to lane 1, the third to lane 2, the fourth to lane 3, the fifth to lane 4, the sixth to lane 5, the seventh to lane 6 and the eighth to lane 7, then repeating with the ninth to lane 0, etc. Delimiters and interframe idle characters are encoded on the TXD and RXD signals with the control code indicated by assertion of TXC and RXC, respectively.

81.1.7 Mapping of XLGMII/CGMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the XLGMII/CGMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 40 Gb/s and 100 Gb/s; therefore, PLS service primitives supporting CSMA/CD operation are not mapped through the RS to the XLGMII/CGMII. This behavior and restrictions are the same as described in 22.7, with the details of the signaling described in 81.3. LPI_REQUEST shall not be set to ASSERT unless the attached link has been operational for at least one second (i.e., link_status = OK, according to the underlying PCS/PMA).

EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

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Table 81–2—Transmit and receive lane associations

TXD, RXD	TXC, RXC	Lane
<7:0>	<0>	0
<15:8>	<1>	1
<23:16>	<2>	2
<31:24>	<3>	3
<39:32>	<4>	4
<47:40>	<5>	5
<55:48>	<6>	6
<63:56>	<7>	7

Mappings for the following primitives are defined for 40 Gb/s and 100 Gb/s operation:

PLS_DATA.request
PLS_DATA.indication
PLS_CARRIER.indication
PLS_SIGNAL.indication
PLS_DATA_VALID.indication

81.1.7.1 Mapping of PLS_DATA.request

81.1.7.1.1 Function

The RS maps the primitive PLS_DATA.request to the XLGMII/CGMII signals TXD<63:0>, TXC<7:0>, and TX_CLK.

81.1.7.1.2 Semantics of the service primitive

PLS_DATA.request(OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take one of three values: ONE, ZERO, or DATA_COMPLETE. ONE or ZERO represents a single data bit. The DATA_COMPLETE value signifies that the MAC sublayer has no more data to output.

81.1.7.1.3 When generated

This primitive is generated by the MAC sublayer to request the transmission of a single data bit on the physical medium or to stop transmission.

81.1.7.1.4 Effect of receipt

The OUTPUT_UNIT values are conveyed to the PHY by the signals TXD<63:0> and TXC<7:0> on each TX_CLK rising edge. Each PLS_DATA.request transaction shall be mapped to a TXD signal in sequence (TXD<0>, TXD<1>,... TXD<63>, TXD<0>) as described in 81.2, and for every eight transactions, a TXC signal in sequence (TXC<0>, TXC<1>,... TXC<7>, TXC<0>) is generated, as described in 81.3.1.2. After 64 PLS_DATA.request transactions from the MAC sublayer (eight octets of eight PLS_DATA.request transactions each), the RS requests transmission of 64 data bits by the PHY. The first octet of preamble shall

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be converted to a Start control character and aligned to lane 0. The TXD<63:0> and TXC<7:0> shall be generated by the RS every 64 bit-times of the MAC sublayer.

The DATA_COMPLETE value shall be mapped to a Terminate control character encoded on the next eight TXD signals in sequence after the last data octet; and is transferred to the PHY at the next TX_CLK rising edge. This may be on the same TX_CLK rising edge as the last data octet or the subsequent TX_CLK rising edge. When the Terminate control character is in lane 0, 1, 2, 3, 4, 5, or 6, the lanes following in sequence are encoded with an Idle control character.

81.1.7.2 Mapping of PLS_DATA.indication

81.1.7.2.1 Function

The RS maps the XLGMII/CGMII signals RXD<63:0>, RXC<7:0>, and RX_CLK to the primitive PLS_DATA.indication.

81.1.7.2.2 Semantics of the service primitive

PLS_DATA.indication (INPUT_UNIT)

The INPUT_UNIT parameter can take one of two values: one or zero. It represents a single data bit.

81.1.7.2.3 When generated

The INPUT_UNIT values are derived from the signals RXC<7:0> and RXD<63:0> received from the PHY on each rising edge of RX_CLK. Each primitive generated to the MAC sublayer entity corresponds to a PLS_DATA.request issued by the MAC at the remote end of the link connecting two DTEs. For each RXD<63:0> during frame reception, the RS shall generate 64 PLS_DATA.indication transactions until the end of frame (Terminate control character), where 0, 8, 16, 24, 32, 40, 48, or 56 PLS_DATA.indication transactions will be generated from the RXD<63:0> containing the Terminate. During frame reception, each RXD signal shall be mapped in sequence into a PLS_DATA.indication transaction (RXD<0>, RXD<1>,... RXD<63>, RXD<0>) as described in 81.2.

The RS shall convert a valid Start control character to a preamble octet prior to generation of the associated PLS_DATA.indication transactions. The RS shall not generate any PLS_DATA.indication primitives for a Terminate control character. To assure robust operation, the value of the data transferred to the MAC may be changed by the RS as required by XLGMII/CGMII error indications (see 81.3.3). Sequence ordered sets are not indicated to the MAC (see 81.3.4).

81.1.7.2.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is unspecified.

81.1.7.3 Mapping of PLS_CARRIER.indication

40 Gb/s and 100 Gb/s operation supports full duplex operation only. The RS only generates this primitive when optional EEE capability or the optional detection of Link Interruption is supported.

CARRIER_STATUS is set to CARRIER_ON if the optional EEE capability is supported and LPI_CARRIER_STATUS is TRUE, or if optional detection of Link Interruption is supported and link_fault is Link Interruption (see 81.3.4.1). CARRIER_STATUS is otherwise set to CARRIER_OFF. The deferral mechanism based upon the Link Interruption signal may be enabled or disabled by management.

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81.1.7.4 Mapping of PLS_SIGNAL.indication

40 Gb/s and 100 Gb/s operation supports full duplex operation only. The RS never generates this primitive.

81.1.7.5 Mapping of PLS_DATA_VALID.indication

81.1.7.5.1 Function

The RS maps the XLGMII/CGMII signals RXC<7:0> and RXD<63:0> to the primitive PLS_DATA_VALID.indication.

81.1.7.5.2 Semantics of the service primitive

PLS_DATA_VALID.indication (DATA_VALID_STATUS)

The DATA_VALID_STATUS parameter can take one of two values: DATA_VALID or DATA_NOT_VALID. The DATA_VALID value indicates that the INPUT_UNIT parameter of the PLS_DATA.indication primitive contains valid data of an incoming frame. The DATA_NOT_VALID value indicates that the INPUT_UNIT parameter of the PLS_DATA.indication primitive does not contain valid data of an incoming frame.

81.1.7.5.3 When generated

The PLS_DATA_VALID.indication service primitive shall be generated by the RS whenever the DATA_VALID_STATUS parameter changes from DATA_VALID to DATA_NOT_VALID or vice versa.

DATA_VALID_STATUS shall assume the value DATA_VALID when a PLS_DATA.indication transaction is generated in response to reception of a Start control character on lane 0 if the prior RXC<7:0> and RXD<63:0> contained eight Idle characters, a Sequence ordered set, or a Terminate character. DATA_VALID_STATUS shall assume the value DATA_NOT_VALID when RXC of the current lane in sequence is asserted for anything except an Error control character. In the absence of errors, DATA_NOT_VALID is caused by a Terminate control character. When DATA_VALID_STATUS changes from DATA_VALID to DATA_NOT_VALID because of a control character other than Terminate, the RS shall ensure that the MAC will detect a FrameCheckError prior to indicating DATA_NOT_VALID to the MAC (see 81.3.3.1).

81.1.7.5.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is unspecified.

81.2 XLGMII/CGMII data stream

Packets transmitted through the XLGMII/CGMII shall be transferred within the XLGMII/CGMII data stream. A data stream is a sequence of bytes, where each byte conveys either a data octet or control character. The parts of the data stream are shown in Figure 81–3.

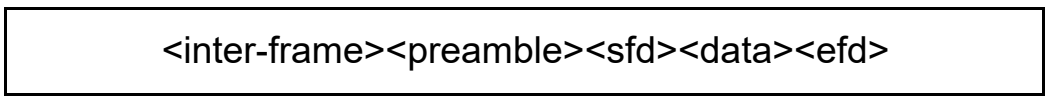

Figure 81–3—XLGMII/CGMII data stream

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For the XLGMII/CGMII, transmission and reception of each bit and mapping of data octets to lanes shall be as shown in Figure 81–4.

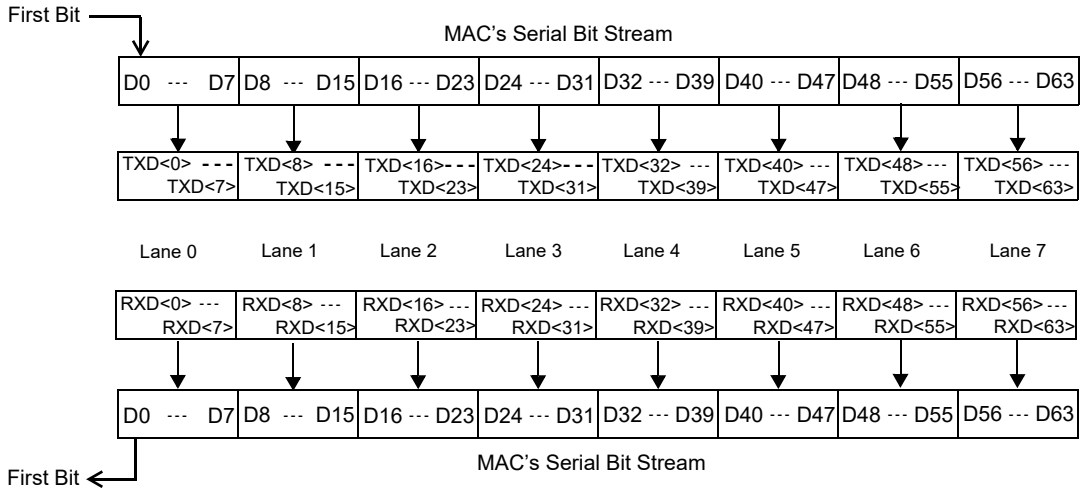

Figure 81–4—Relationship of data lanes to MAC serial bit stream

81.2.1 Inter-frame <inter-frame>

The inter-frame <inter-frame> period on an XLGMII/CGMII transmit or receive path is an interval during which no frame data activity occurs. The <inter-frame> corresponding to the MAC interpacket gap begins with the Terminate control character, continues with Idle control characters and ends with the Idle control character prior to a Start control character. The length of the interpacket gap may be changed between the transmitting MAC and receiving MAC by one or more functions (e.g., RS lane alignment or PHY clock rate compensation). The minimum IPG at the XLGMII/CGMII of the receiving RS is one octet.

The signaling of link status information logically occurs in the <inter-frame> period (see 81.3.4). Frame processing when signaling of link status information is initiated or terminated is described in 81.3.3.

81.2.2 Preamble <preamble> and start of frame delimiter <sfd>

The preamble <preamble> begins a frame transmission by a MAC as specified in 4.2.5 and when generated by a MAC consists of 7 octets with the following bit values:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

The Start control character indicates the beginning of MAC data on the XLGMII/CGMII. On transmit, the RS converts the first data octet of preamble transferred from the MAC into a Start control character. On receive, the RS converts the Start control character into a preamble data octet. The Start control character is aligned to lane 0 of the XLGMII/CGMII by the RS on transmit and by the PHY on receive.

The start of frame delimiter <sfd> indicates the start of a frame and immediately follows the preamble. The bit value of <sfd> at the XLGMII/CGMII is the same as the Start Frame Delimiter (SFD) specified in 4.2.6 and is equal to the following:

10101011

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The preamble and SFD are shown previously with their bits ordered for serial transmission from left to right. As shown, the left-most bit of each octet is the LSB of the octet and the right-most bit of each octet is the MSB of the octet.

The preamble and SFD are transmitted through the XLGMII/CGMII as octets sequentially ordered on the lanes of the XLGMII/CGMII. The first preamble octet is replaced with a Start control character and it is aligned to lane 0, the second octet on lane 1, the third on lane 2, the fourth on lane 3, the fifth on lane 4, the sixth on lane 5, the seventh on lane 6, and the SFD on lane 7, and the eight octets are transferred on the next rising edge of TX_CLK. The ninth octet is assigned to lane 0 with subsequent octets sequentially assigned to the lanes. The XLGMII/CGMII <preamble> and <sfd> are as follows:

Lane 0	**Lane 1**	**Lane 2**	**Lane 3**	**Lane 4**	**Lane 5**	**Lane 6**	**Lane 7**
Start	10101010	10101010	10101010	10101010	10101010	10101010	10101011

81.2.3 Data <data>

The data <data> in a frame shall consist of a set of data octets.

81.2.4 End of frame delimiter <efd>

Assertion of TXC with the appropriate Terminate control character encoding of TXD on a lane constitutes an end of frame delimiter <efd> for the transmit data stream. Similarly, assertion of RXC with the appropriate Terminate control character encoding of RXD constitutes an end of frame delimiter for the receive data stream. The XLGMII/CGMII shall recognize the end of frame delimiter on any of the eight lanes of the XLGMII/CGMII.

81.2.5 Definition of Start of Packet and End of Packet Delimiters

For the purposes of Clause 30, the Start of Packet Delimiter is defined as the Start control character, and the End of Packet delimiter is defined as the end of the last sequential data octet preceding the Terminate control character or other control character causing a change from DATA_VALID to DATA_NOT_VALID (see 81.1.7.5.2 and 30.3.2.1.5).

81.3 XLGMII/CGMII functional specifications

The XLGMII/CGMII is designed to make the differences among the various media and transceiver combinations transparent to the MAC sublayer. The selection of logical control signals and the functional procedures are all designed to this end.

NOTE—No XLGMII/CGMII loopback is defined, but XLGMII/CGMII signals are specified such that transmit signals may be connected to receive signals to create a loopback path. To do this, TXD<0> is connected to RXD<0> ... TXD<63> to RXD<63>, TXC<0> to RXC<0> ... TXC<7> to RXC<7>, and TXCLK to RXCLK. Such a loopback does not test the Link Fault Signaling state diagram, nor any of the error handling functions of the receive RS.

81.3.1 Transmit

81.3.1.1 TX_CLK

TX_CLK is a continuous clock used for operation at the appropriate frequency. TX_CLK provides the timing reference for the transfer of the TXC<7:0> and TXD<63:0> signals from the RS to the PHY. The values of TXC<7:0> and TXD<63:0> shall be sampled by the PHY on the rising edge of TX_CLK. TX_CLK is sourced by the RS.

The TX_CLK frequency shall be one-sixty-fourth of the MAC transmit data rate.

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81.3.1.2 TXC<7:0> (transmit control)

TXC<7:0> indicate that the RS is presenting either data or control characters on the XLGMII/CGMII for transmission. The TXC signal for a lane shall be deasserted when a data octet is being sent on the corresponding lane and asserted when a control character is being sent. In the absence of errors, the TXC signals are deasserted by the RS for each octet of the preamble (except the first octet that is replaced with a Start control character) and remain deasserted while all octets to be transmitted are presented on the lanes of the XLGMII/CGMII. TXC<7:0> are driven by the RS and shall transition synchronously with respect to the rising edge of TX_CLK. Table 81–3 specifies the permissible encodings of TXD and TXC for an XLGMII/CGMII transmit lane. Additional requirements apply for proper code sequences and in which lanes particular codes are valid (e.g., Start control character is to be aligned to lane 0).

Table 81–3—Permissible encodings of TXC and TXD

TXC	TXD	Description	PLS_DATA.request parameter
0	0x00 through 0xFF	Normal data transmission	Zero, one (eight bits)
1	0x00 through 0x05	Reserved	—
1	0x06	Only valid on all 8 lanes simultaneously to request LPI	No applicable parameter (normal inter-frame)
1	0x07	Idle	No applicable parameter (normal inter-frame)
1	0x08 through 0x9B	Reserved	—
1	0x9C	Sequence (only valid in lane 0)	No applicable parameter (inter-frame status signal)
1	0x9D through 0xFA	Reserved	—
1	0xFB	Start (only valid in lane 0)	No applicable parameter, replaces first eight zero, one of a frame (preamble octet)
1	0xFC	Reserved	—
1	0xFD	Terminate	DATA_COMPLETE
1	0xFE	Error	No applicable parameter
1	0xFF	Reserved	—

A PHY with EEE capability shall interpret the combination of TXC and TXD as shown in Table 81–3 as an assertion of LPI. Transition into and out of the LPI state is shown in Figure 81–7.

81.3.1.3 TXD<63:0> (transmit data)

TXD is a bundle of 64 data signals organized into eight lanes of eight signals each (TXD<7:0>, TXD<15:8>, TXD<23:16>, TXD<31:24>, TXD<39:32>, TXD<47:40>, TXD<55:48>, and TXD<63:56>) that are driven by the RS. Each lane is associated with a TXC signal as shown in Table 81–2 and shall be encoded as shown in Table 81–3. TXD<63:0> shall transition synchronously with respect to the rising edge of TX_CLK. For each high TX_CLK transition, data and/or control are presented on TXD<63:0> to the PHY for transmission. TXD<0> is the least significant bit of lane 0, TXD<8> the least significant bit of lane 1, TXD<16> the least significant bit of lane 2, TXD<24> the least significant bit of lane 3, TXD<32> the least significant bit of lane 4, TXD<40> the least significant bit of lane 5, TXD<48> the least significant bit of lane 6, and TXD<56> the least significant bit of lane 7.

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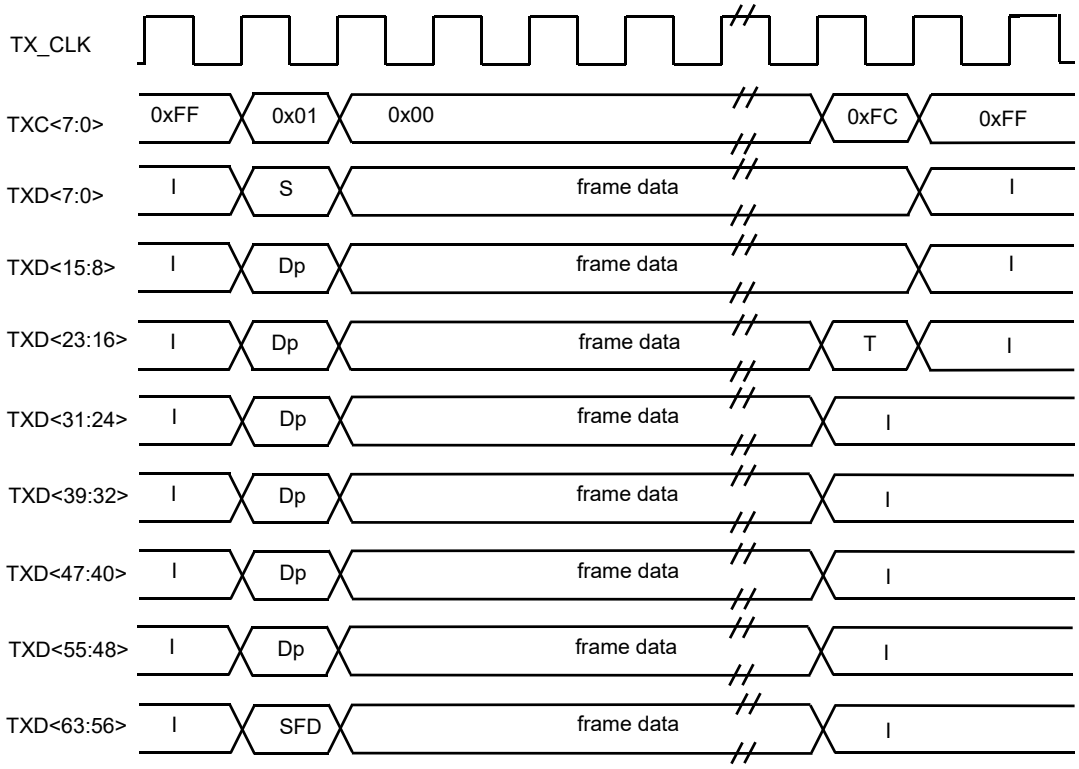
Assertion on a lane of appropriate TXD values when TXC is asserted will cause the PHY to generate code-groups associated with either Idle, Start, Terminate, Sequence, or Error control characters. While the TXC of a lane is deasserted, TXD of the lane is used to request the PHY to generate code-groups corresponding to the data octet value of TXD. An example of normal frame transmission is illustrated in Figure 81–5.



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character, SFD: Start of Frame Delimiter

Figure 81–5—Normal frame transmission

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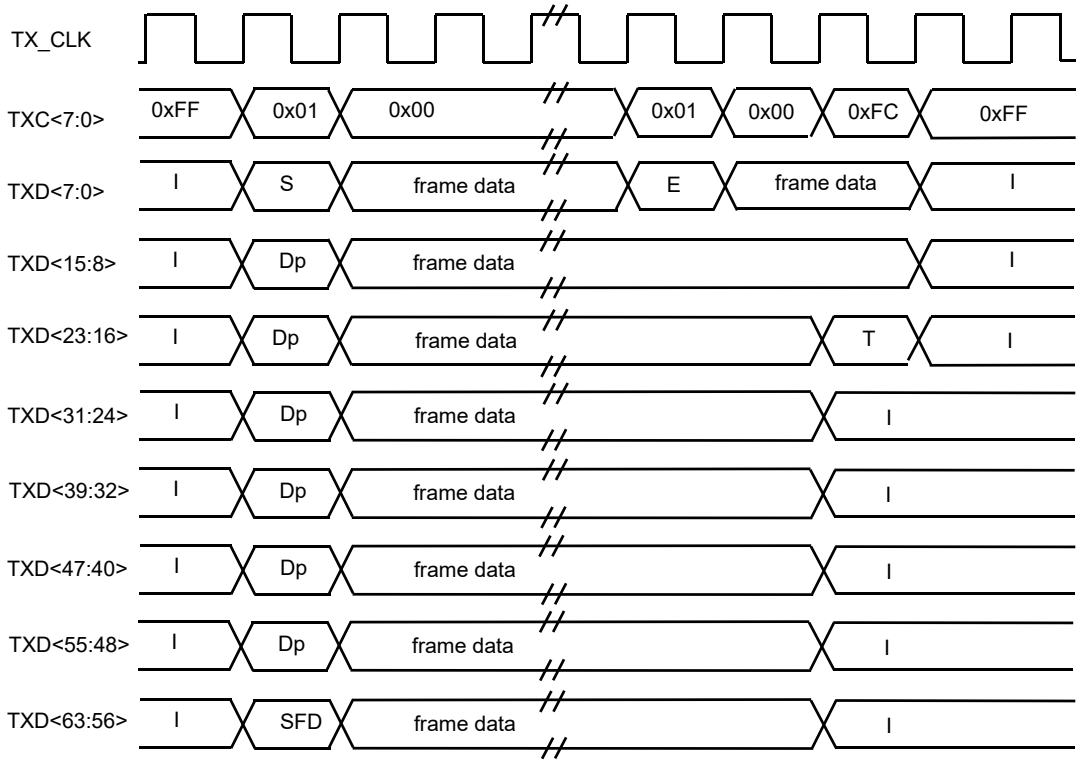
Figure 81–6 shows the behavior of TXD and TXC during an example transmission of a frame propagating an error.



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character, E: Error control character, SFD: Start of Frame Delimiter

Figure 81–6—Transmit Error Propagation

81.3.1.4 Start control character alignment

On transmit, it may be necessary for the RS to modify the length of the <inter-frame> in order to align the Start control character (first octet of preamble) on lane 0. This shall be accomplished in one of the following two ways:

a) A MAC implementation may incorporate this RS function into its design and always insert additional idle characters to align the start of preamble on an eight byte boundary. Note that this will reduce the effective data rate for certain packet sizes separated with minimum inter-frame spacing.

b) Alternatively, the RS may maintain the effective data rate by sometimes inserting and sometimes deleting idle characters to align the Start control character. When using this method the RS maintains a Deficit Idle Count (DIC) that represents the cumulative count of idle characters deleted or inserted. The DIC is incremented for each idle character deleted, decremented for each idle character inserted, and the decision of whether to insert or delete idle characters is constrained by bounding the DIC to a minimum value of zero and maximum value of seven. Note that this may result in inter-frame spacing observed on the transmit XLGMII/CGMII that is up to seven octets shorter than the minimum transmitted inter-frame spacing specified in Clause 4; however, the frequency of shortened inter-frame spacing is constrained by the DIC rules. The DIC is only reset at initialization and is applied regardless of the size of the IPG transmitted by the MAC sublayer. An equivalent technique may be employed to control RS alignment of the Start control character provided that the result is the same as if the RS implemented the DIC as described.

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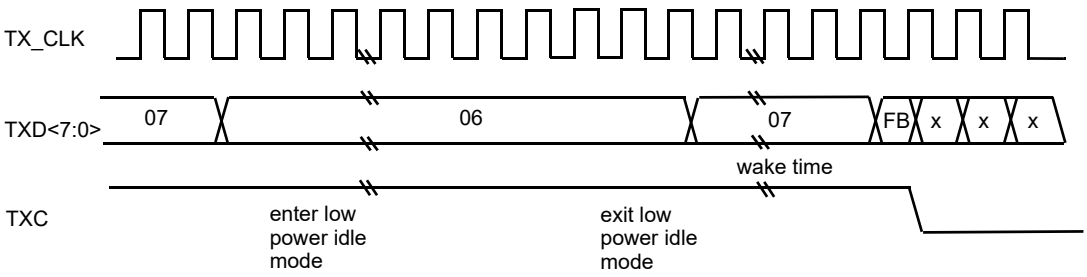
81.3.1.5 Transmit direction LPI transition

LPI operation and the LPI client are described in 78.1. The RS requests the PHY to transition to the LPI state by asserting TXC and setting TXD to 0x06 (in all lanes). The RS maintains the same state for these signals for the entire time that the PHY is to remain in the LPI state.

The RS asserts TXC and asserts IDLE on lanes 0 to 7 in order to make the PHY transition out of the LPI state. The RS should not present a start code for valid transmit data until after the wake-up time specified for the PHY ($T_{w\_sys\_tx}$). The wake times are shown in Table 78–4

Figure 81–7 shows the behavior of TXC and TXD<7:0> during the transition into and out of the LPI state.



NOTE—TXC and TXD are shown for one lane, all 8 lanes behave identically during LPI.

Figure 81–7—LPI transition

Table 81–3 summarizes the permissible encodings of TXD<63:0>, TXC<7:0>.

81.3.2 Receive

81.3.2.1 RX_CLK (receive clock)

RX_CLK is a continuous clock that provides the timing reference for the transfer of the RXC<7:0> and RXD<63:0> signals from the PHY to the RS. RXC<7:0> and RXD<63:0> shall be sampled by the RS on the rising edge of RX_CLK. RX_CLK is sourced by the PHY.

The frequency of RX_CLK may be derived from the received data or it may be that of a nominal clock (e.g., TX_CLK). When the received data rate at the PHY is within tolerance, the RX_CLK frequency shall be one-sixty-fourth of the MAC receive data rate.

There is no need to transition between the recovered clock reference and a nominal clock reference on a frame-by-frame basis. If loss of received signal from the medium causes a PHY to lose the recovered RX_CLK reference, the PHY shall source the RX_CLK from a nominal clock reference.

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals.

81.3.2.2 RXC<7:0> (receive control)

RXC<7:0> indicate that the PHY is presenting either recovered and decoded data or control characters on the XLGMII/CGMII. The RXC signal for a lane shall be deasserted when a data octet is being received on the corresponding lane and asserted when a control character is being received. In the absence of errors, the RXC signals are deasserted by the PHY for each octet of the preamble (except the first octet that is replaced with a Start control character) and remain deasserted while all octets to be received are presented on the

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lanes of the XLGMII/CGMII. RXC<7:0> are driven by the PHY and shall transition synchronously with respect to the rising edge of RX_CLK. Table 81–4 specifies the permissible encodings of RXD and RXC for an XLGMII/CGMII receive lane. Additional requirements apply for proper code sequences and in which lanes particular codes are valid (e.g., Start control character is to be aligned to lane 0).

Table 81–4—Permissible lane encodings of RXD and RXC

RXC	RXD	Description	PLS_DATA.indication parameter
0	0x00 through 0xFF	Normal data reception	Zero, one (eight bits)
1	0x00 through 0x05	Reserved	—
1	0x06	Only valid on all 8 lanes simultaneously to indicate LP_IDLE is asserted	No applicable parameter (normal inter-frame)
1	0x07	Idle	No applicable parameter (Normal inter-frame)
1	0x08 through 0x9B	Reserved	—
1	0x9C	Sequence (only valid in lane 0)	No applicable parameter (Inter-frame status signal)
1	0x9D through 0xFA	Reserved	—
1	0xFB	Start (only valid in lane 0)	No applicable parameter, first eight zero, one of a frame (a preamble octet)
1	0xFC	Reserved	—
1	0xFD	Terminate	No applicable parameter (start of inter-frame)
1	0xFE	Error	No applicable parameter
1	0xFF	Reserved	—

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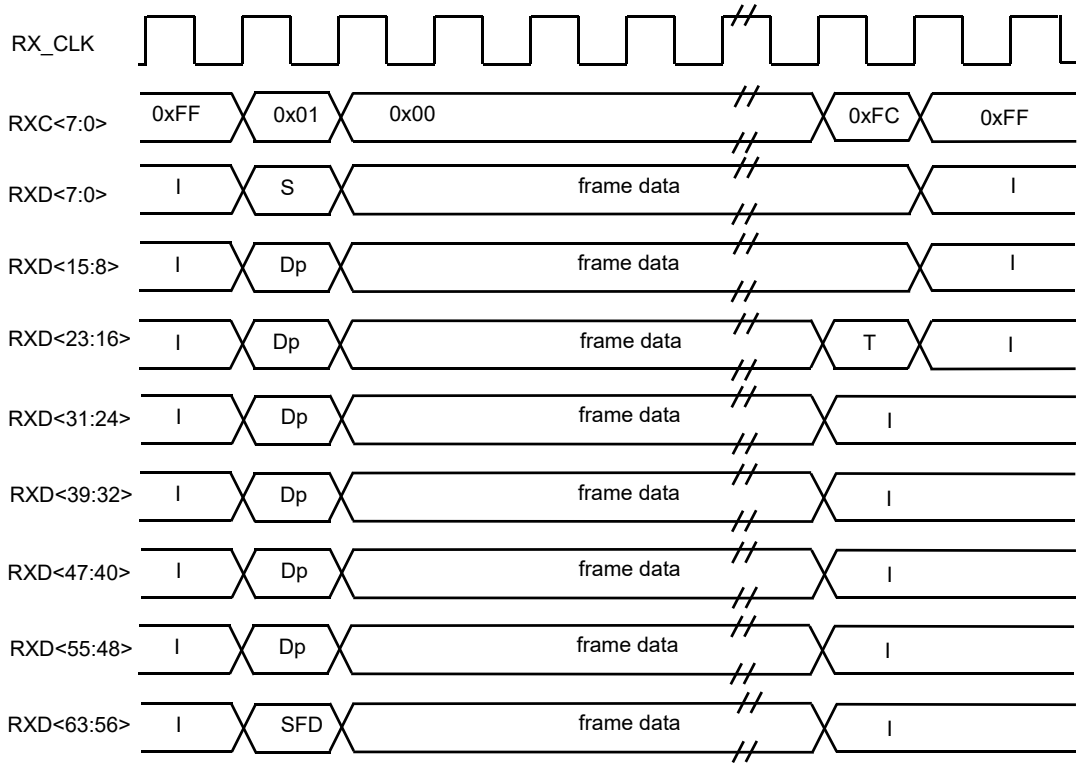
Figure 81–8 shows the behavior of RXC<7:0> during an example frame reception with no errors.



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character, SFD: Start of Frame Delimiter

Figure 81–8—Frame reception without error

81.3.2.3 RXD (receive data)

RXD is a bundle of 64 data signals (RXD<63:0>) organized into eight lanes of eight signals each (RXD<7:0>, RXD<15:8>, RXD<23:16>, RXD<31:24>, RXD<39:32>, RXD<47:40>, RXD<55:48>, and RXD<63:56>) that are driven by the PHY. Each lane is associated with an RXC signal as shown in Table 81–2 and shall be decoded by the RS as shown in Table 81–4. RXD<63:0> shall transition synchronously with respect to the rising edge of RX_CLK. For each rising RX_CLK transition, received data and/or control are presented on RXD<63:0> for mapping by the RS. RXD<0> is the least significant bit of lane 0, RXD<8> the least significant bit of lane 1, RXD<16> the least significant bit of lane 2, RXD<24> the least significant bit of lane 3, RXD<24> the least significant bit of lane 3, RXD<32> the least significant bit of lane 4, RXD<40> the least significant bit of lane 5, RXD<48> the least significant bit of lane 6, and RXD<56> the least significant bit of lane 7. Figure 81–8 shows the behavior of RXD<63:0> during frame reception.

While the RXC of a lane is deasserted, RXD of the lane is used by the RS to generate PLS_DATA.indications. Assertion on a lane of appropriate RXD values when RXC is asserted indicates to the RS the Start control character, Terminate control character, Sequence control character, or Error control character that drive its mapping functions.

RXC of a lane is asserted with the appropriate Error control character encoding on RXD of the lane to indicate that an error was detected somewhere in the frame presently being transferred from the PHY to the

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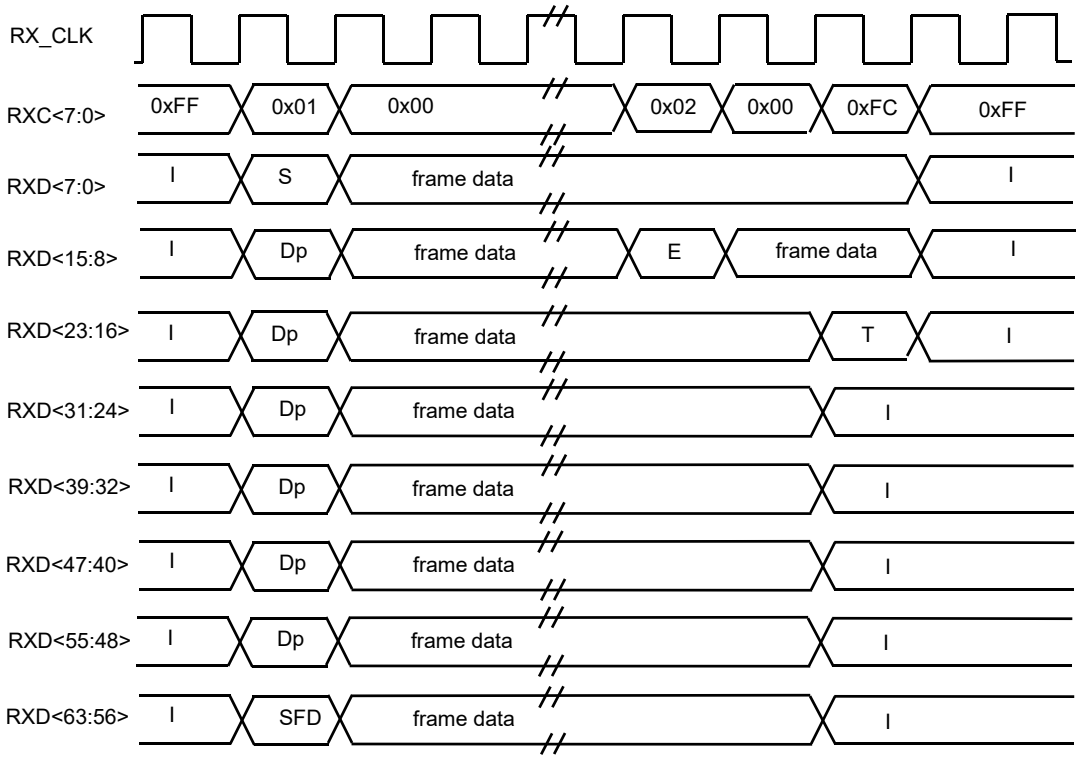
RS (e.g., a coding error, or any error that the PHY is capable of detecting, and that may otherwise be undetectable at the MAC sublayer).

The effect of an Error control character on the RS is defined in 81.3.3.1. Figure 81–9 shows the behavior of RXC and RXD during the reception of an example frame with an error.



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character, E: Error control character, SFD: Start of Frame Delimiter

Figure 81–9—Reception with error

81.3.2.4 Receive direction LPI transition

LPI operation and the LPI client are described in 78.1. When the PHY receives signals from the link partner to indicate transition into the low power state, it indicates this to the RS by asserting RXC and setting RXD to 0x06 (in all lanes). The PHY maintains these signals in this state while it remains in the LPI state. When the PHY receives signals from the link partner to indicate transition out of the LPI state, it indicates this to the RS by asserting RXC and asserting idle on all lanes 0 to 7 to return to a normal interframe state. The RS shall interpret the LPI coding as shown in Table 81–4.

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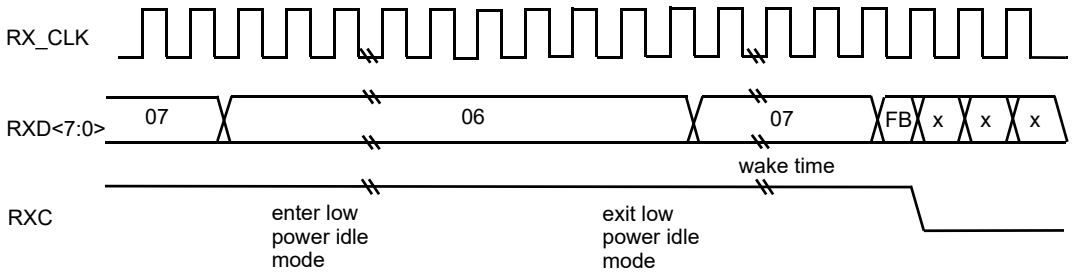
Figure 81–10 shows the behavior of RXC and RXD<7:0> during LPI transitions.



NOTE 1—RXC and RXD are shown for one lane, all 8 lanes behave identically during LPI.
NOTE 2—In some instances, LPI may be followed by characters other than IDLE during wake time.

Figure 81–10—LPI transition

81.3.3 Error and fault handling

81.3.3.1 Response to error indications by the XLGMII/CGMII

If, during frame reception (i.e., when DATA_VALID_STATUS = DATA_VALID), a control character other than a Terminate control character is signaled on a received lane, the RS shall ensure that the MAC will detect a FrameCheckError in that frame. This requirement may be met by incorporating a function in the RS that produces a received frame data sequence delivered to the MAC sublayer that is guaranteed to not yield a valid CRC result, as specified by the frame check sequence algorithm (see 3.2.8). This data sequence may be produced by substituting data delivered to the MAC. The RS generates eight PLS_DATA.indication primitives for each Error control character received within a frame, and may generate eight PLS_DATA.indication primitives to ensure FrameCheckError when a control character other than Terminate causes the end of the frame.

Other techniques may be employed to respond to a received Error control character provided that the result is that the MAC sublayer behaves as though a FrameCheckError occurred in the received frame.

81.3.3.2 Conditions for generation of transmit Error control characters

If, during the process of transmitting a frame, it is necessary to request that the PHY deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability, then an Error control character may be asserted on a transmit lane by the appropriate encoding of the lane's TXD and TXC signals.

81.3.3.3 Response to received invalid frame sequences

The RS shall not indicate DATA_VALID to the MAC for a Start control character received on any lane other than lane 0. Error free operation will not change the SFD alignment in lane 7. A MAC/RS implementation is not required to process a packet that has an SFD in a position other than lane 7 in the XLGMII/CGMII transfer containing the Start control character.

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81.3.4 Link fault signaling

Link fault signaling operates between the remote RS and the local RS. Faults detected between the remote RS and the local RS are received by the local RS as Local Fault. Only an RS originates Remote Fault signals. The behavior of the fault signaling is the same as it is for Clause 46 with the exception that the ordered sets are aligned to eight byte boundaries, padding lanes 4 to 7 with 0x00.

Clause 46 uses the term column when describing data transfers on the XGMII. The eight lanes of data and control transferred per clock cycle on XLGMII/CGMII are equivalent to a column in the following description of link fault signaling.

Sublayers within the PHY are capable of detecting faults that render a link unreliable for communication. Upon recognition of a fault condition, a PHY sublayer indicates Local Fault status on the data path. When this Local Fault status reaches an RS, the RS stops sending MAC data or LPI, and continuously generates a Remote Fault status on the transmit data path (possibly truncating a MAC frame being transmitted). When Remote Fault status is received by an RS, the RS stops sending MAC data or LPI, and continuously generates Idle control characters. When the RS no longer receives fault status messages, it returns to normal operation, sending MAC data or LPI. Note that this behavior only supports bidirectional operation.

Status is signaled in an eight byte Sequence ordered set as shown in Table 81–5. The PHY indicates Local Fault with a Sequence control character in lane 0 and data characters of 0x00 in lanes 1, 2, 4, 5, 6, and 7 plus a data character of 0x01 in lane 3. The RS indicates a Remote Fault with a Sequence control character in lane 0 and data characters of 0x00 in lanes 1, 2, 4, 5, 6, and 7 plus a data character of 0x02 in lane 3. Though most fault detection is on the receive data path of a PHY, in some specific sublayers, faults can be detected on the transmit side of the PHY. This is also indicated by the PHY with a Local Fault status. All other values in lanes 1 to 3 not shown in Table 81–5 are reserved. The link fault signaling state diagram allows future standardization of reserved Sequence ordered sets for functions other than link fault indications.

For operation with links that may be temporarily interrupted, optional detection of a third fault condition, Link Interruption, is provided. Link Interruption is indicated by the PHY receive function by continuously sending the Link Interruption ordered set as defined in Table 81–5.

Table 81–5—Sequence ordered sets

Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Description
Sequence	0x00	0x00	0x00	0x00	0x00	0x00	0x00	Reserved
Sequence	0x00	0x00	0x01	0x00	0x00	0x00	0x00	Local Fault
Sequence	0x00	0x00	0x02	0x00	0x00	0x00	0x00	Remote Fault
Sequence	0x00	0x00	0x03	0x00	0x00	0x00	0x00	Link Interruption

The RS reports the fault status of the link. Local Fault indicates a fault detected on the receive data path between the remote RS and the local RS. Remote Fault indicates a fault on the transmit path between the local RS and the remote RS. The RS shall implement the link fault signaling state diagram (see Figure 81–11).

81.3.4.1 Variables and counters

The Link Fault Signaling state diagram uses the following variables and counters:

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col_cnt
: A count of the number of columns received not containing a fault_sequence. This counter increments at RX_CLK rate (on the rising clock transitions) unless reset.

fault_sequence
: A new column received on RXC<7:0> and RXD<63:0> comprising a Sequence ordered set of eight bytes and consisting of a Sequence control character in lane 0 and a seq_type in lanes 1, 2, 3, 4, 5, 6, and 7 indicating either Local Fault, Remote Fault, or Link Interruption.

last_seq_type
: The seq_type of the previous Sequence ordered set received
  Values: Local Fault; 0x00 in lane 1, 0x00 in lane 2, 0x01 in lane 3, 0x00 in lane 4, 0x00 in lane 5, 0x00 in lane 6, 0x00 in lane 7.
  Remote Fault; 0x00 in lane 1, 0x00 in lane 2, 0x02 in lane 3, 0x00 in lane 4, 0x00 in lane 5, 0x00 in lane 6, 0x00 in lane 7.
  Link Interruption; 0x00 in lane 1, 0x00 in lane 2, 0x03 in lane 3, 0x00 in lane 4, 0x00 in lane 5, 0x00 in lane 6, 0x00 in lane 7.

link_fault
: An indicator of the fault status.
  Values: OK; No fault.
  Local Fault; fault detected by the PHY.
  Remote Fault; fault detection signaled by the remote RS.
  Link Interruption; link temporarily unavailable, signaled by the PHY.

reset
: Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.
  Values: FALSE: The device is completely powered and has not been reset (default).
  TRUE: The device has not been completely powered or has been reset.

seq_cnt
: A count of the number of received Sequence ordered sets of the same type.

seq_type
: The value received in the current Sequence ordered set
  Values: Local Fault; 0x00 in lane 1, 0x00 in lane 2, 0x01 in lane 3, 0x00 in lane 4, 0x00 in lane 5, 0x00 in lane 6, 0x00 in lane 7.
  Remote Fault; 0x00 in lane 1, 0x00 in lane 2, 0x02 in lane 3, 0x00 in lane 4, 0x00 in lane 5, 0x00 in lane 6, 0x00 in lane 7.
  Link Interruption; 0x00 in lane 1, 0x00 in lane 2, 0x03 in lane 3, 0x00 in lane 4, 0x00 in lane 5, 0x00 in lane 6, 0x00 in lane 7.

81.3.4.2 State diagram

The Link Fault Signaling state diagram specifies the RS monitoring of RXC<7:0> and RXD<63:0> for Sequence ordered sets. The variable link_fault is set to indicate the value of a received Sequence ordered set when four fault_sequences containing the same fault value have been received with fault sequence separated by less than 128 columns and no intervening fault_sequences of a different fault value. The state diagram is shown in Figure 81–11.

The variable link_fault is set to OK following any interval of 128 columns not containing a Remote Fault, Local Fault, or Link Interruption Sequence ordered set.

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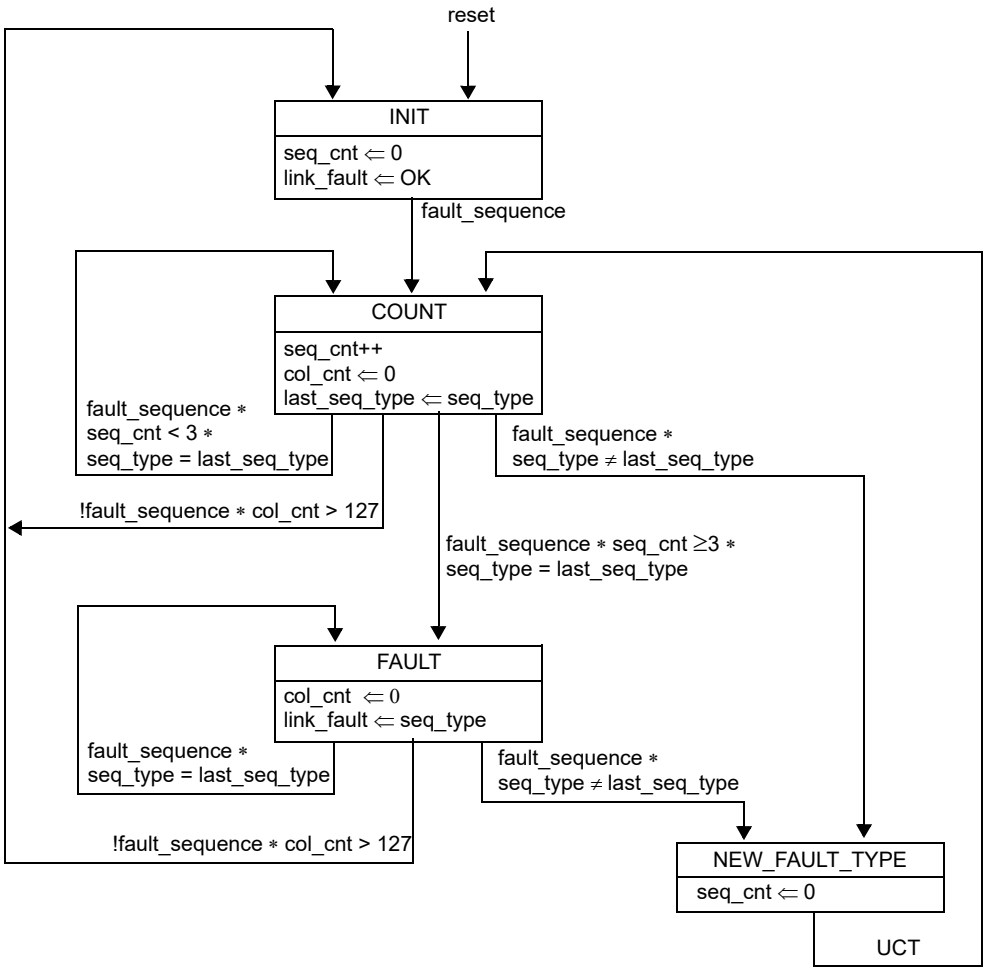

Figure 81–11—Link Fault Signaling state diagram

The RS output onto TXC<7:0> and TXD<63:0> is controlled by the variable link_fault.

a) link_fault = OK
The RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.

b) link_fault = Local Fault
The RS shall continuously generate Remote Fault Sequence ordered sets.

c) link_fault = Remote Fault or link_fault = Link Interruption
The RS shall continuously generate Idle control characters.

81.4 LPI assertion and detection

Certain PHYs support Energy Efficient Ethernet (see Clause 78). PHYs with EEE capability support LPI assertion and detection. LPI operation and the LPI client are described in 78.1. LPI signaling allows the RS to signal to the PHY and to the link partner that a break in the data stream is expected and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it allows the LPI client to understand that the link partner has sent such an indication.

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The LPI assertion and detection mechanism fits conceptually between the PLS Service Primitives and the XLGMII and CGMII signals as shown in Figure 81–12.

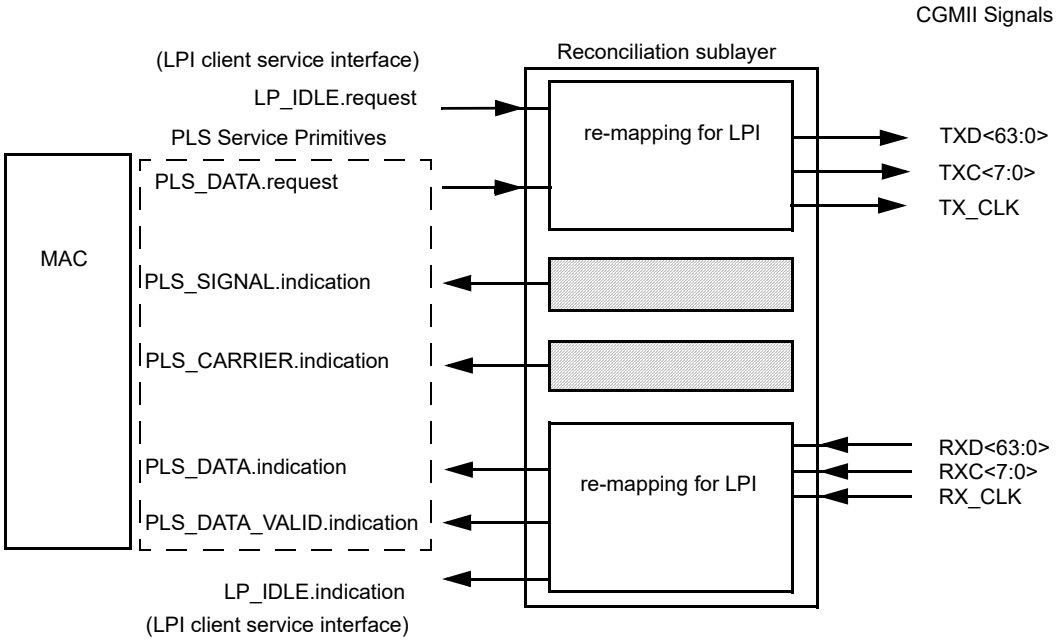

Figure 81–12—LPI assertion and detection mechanism

The definition of TXC<7:0> and TXD<63:0> is derived from the state of PLS_DATA.request (81.1.7), except when it is overridden by an assertion of Remote Fault or LP_IDLE.request.

Similarly, RXC<7:0> and RXD<63:0> are mapped to PLS_DATA.indication except when LP_IDLE is detected.

PLS_CARRIER.indication(CARRIER_STATUS) is set to CARRIER_ON when the link is in LPI mode. See 81.1.7.3.

The timing of PLS_CARRIER.indication when used for the LPI function is controlled by the LPI transmit state diagram.

81.4.1 LPI messages

LP_IDLE.indication(LPI_INDICATION)

A primitive that indicates to the LPI client that the PHY has detected the assertion or deassertion of LPI from the link partner.

Values: DEASSERT: The link partner is operating with normal inter-frame behavior (default).
ASSERT: The link partner has asserted LPI.

LP_IDLE.request(LPI_REQUEST)

The LPI_REQUEST parameter can take one of two values: ASSERT or DEASSERT. ASSERT initiates the signaling of LPI to the link partner. DEASSERT stops the signaling of LPI to the link partner. The effect of receipt of this primitive is undefined if link_status is not OK (see 73.9.1.1) or within 1 s of the change of link_status to OK.

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81.4.2 Transmit LPI state diagram

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been deasserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake-up time is enforced by the transmit LPI state diagram using PLS_CARRIER.indication(CARRIER_STATUS). The implementation shall conform to the behavior described by the transmit LPI state diagram shown in Figure 81–13.

81.4.2.1 Variables and counters

The transmit LPI state diagram uses the following variables and counters:

LPI_CARRIER_STATUS
: The LPI_CARRIER_STATUS variable indicates how the CARRIER_STATUS parameter is controlled by the LPI_REQUEST parameter. The LPI_CARRIER_STATUS is either TRUE or FALSE as determined by the Transmit LPI state diagram in Figure 81–13.

power_on
: Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.
  Values: FALSE: The device is completely powered (default).
  TRUE: The device has not been completely powered.

reset
: Used by management to control the resetting of the RS.
  Values: FALSE: Do not reset the RS (default).
  TRUE: Reset the RS.

tw_timer
: A timer that counts the time since the deassertion of LPI. The terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2. If PMA Ingress AUI Stop Enable (PIASE) bit (1.7.9) is asserted for any of the PMA sublayers, the terminal count of the timer is the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2 plus additional time equal to $T_{w\_sys\_tx}$–$T_{w\_sys\_rx}$ for the XLAUI and CAUI-n as shown in Table 78–4 for each PMA with PIASE to be asserted. The signal tw_timer_done is asserted when tw_timer reaches its terminal count.

81.4.2.2 State diagram

81.4.3 Considerations for transmit system behavior

The transmit system should expect that egress data flow is halted for at least resolved $T_{w\_sys\_tx}$ (see 78.2) time after it requests the deassertion of LPI. Buffering and queue management should be designed to accommodate this behavior.

81.4.4 Considerations for receive system behavior

The mapping function of the Reconciliation Sublayer shall continue to signal DATA_NOT_VALID on PLS_DATA_VALID.indication while it is detecting LP_IDLE on the XLGMII and CGMII. The receive system should be aware that data frames may arrive at the XLGMII and CGMII following the deassertion of LPI_INDICATION with a delay corresponding to the link partner's resolved $T_{w\_sys\_rx}$ (as specified in 78.5) time.

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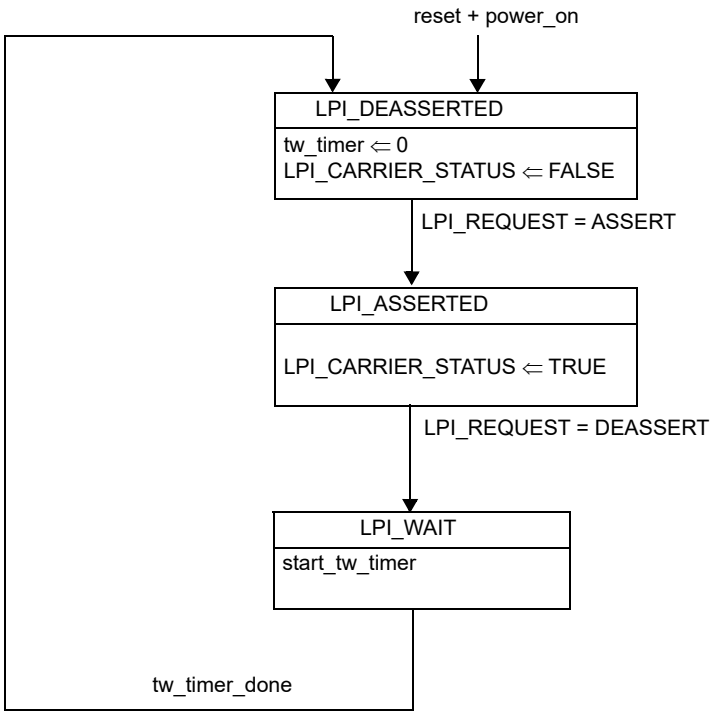

Figure 81–13—Transmit LPI State Diagram

If the PMA Ingress AUI Stop Enable (PIASE) bit (1.7.9) is asserted for any of the PMA sublayers, the PMA may stop signaling on the XLAUI and CAUI-n in the receive direction to conserve energy. The receiver should negotiate an additional time for the remote T_{w_sys} (equal to $T_{w\_sys\_tx}$–$T_{w\_sys\_rx}$ for the XLAUI and CAUI-n as shown in Table 78–4) for each PMA with PIASE to be asserted before setting the PIASE bits.

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81.5 Protocol implementation conformance statement (PICS) proforma for Clause 81, Reconciliation Sublayer (RS) and Media Independent Interface for 40 Gb/s and 100 Gb/s operation[144]

81.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 81, Reconciliation Sublayer (RS) and Media Independent Interface for 40 Gb/s and 100 Gb/s operation, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

81.5.2 Identification

81.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

81.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 81, Reconciliation Sublayer (RS) and Media Independent Interface for 40 Gb/s and 100 Gb/s operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[144]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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81.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PHY40	PHY support of XLGMII	81.2, 81.3		O	Yes [ ] No [ ]
*PHY100	PHY support of CGMII	81.2, 81.3		O	Yes [ ] No [ ]
*MII	Reconciliation Sublayer support of either XLGMII or CGMII	81.2, 81.3		O	Yes [ ] No [ ]
*LPI	Implementation of LPI	81.1.7		O	Yes [ ] No [ ]

81.5.3 PICS proforma tables for Reconciliation Sublayer and Media Independent Interface for 40 Gb/s and 100 Gb/s operation

81.5.3.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	PHY support of MAC data rate	81.1.3	Support MAC data rate of 40 Gb/s	PHY40:M	Yes [ ] N/A [ ]
G2	PHY support of MAC data rate	81.1.3	Support MAC data rate of 100 Gb/s	PHY100:M	Yes [ ] N/A [ ]
G3	Cumulative MAC Control, MAC and RS delay	81.1.4	Per Table 81–1	MII:M	Yes [ ] N/A [ ]
G4	Lane structure	81.1.6	Per Table 81–2	M	Yes [ ]

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81.5.3.2 Mapping of PLS service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
PL1	Mapping to Clause 6	81.1.7	RS implements mapping to Clause 6 PLS service primitives	MII:M	Yes [ ] N/A [ ]
PL2	Mapping of PLS_DATA.requests	81.1.7.1.4	In sequence TXD<0> to TXD<63>	MII:M	Yes [ ] N/A [ ]
PL3	Start control character creation	81.1.7.1.4	First octet of preamble converted to Start control character	MII:M	Yes [ ] N/A [ ]
PL4	TXD and TXC generation	81.1.7.1.4	For each 64 PLS_DATA.requests	MII:M	Yes [ ] N/A [ ]
PL5	Terminate control character creation	81.1.7.1.4	DATA_COMPLETE causes creation of Terminate control character in next lane in sequence	MII:M	Yes [ ] N/A [ ]
PL6	Mapping RXD to PLS_DATA.indications	81.1.7.2.3	Create PLS_DATA.indications in sequence from RXD<0> to RXD<63>	MII:M	Yes [ ] N/A [ ]
PL7	PLS_DATA.indication generation	81.1.7.2.3	Generate 64 PLS_DATA.indications for each RXD<63:0> until Terminate then generating 0, 8, 16, 24, 32, 40, 48, or 56	MII:M	Yes [ ] N/A [ ]
PL8	Start control character conversion	81.1.7.2.3	Convert valid Start control character to preamble before generating PLS_DATA.indications	MII:M	Yes [ ] N/A [ ]
PL9	Terminate control character	81.1.7.2.3	No PLS_DATA.indications generated	MII:M	Yes [ ] N/A [ ]
PL10	PLS_DATA_VALID.indication generation	81.1.7.5.3	On change of value of DATA_VALID_STATUS	MII:M	Yes [ ] N/A [ ]
PL11	DATA_VALID_STATUS	81.1.7.5.3	Value of DATA_VALID on a lane 0 Start control character preceded by eight idles, a Sequence ordered set, or a Terminate character	MII:M	Yes [ ] N/A [ ]
PL12	DATA_VALID_STATUS	81.1.7.5.3	Value of DATA_NOT_VALID on any control character but Error	MII:M	Yes [ ] N/A [ ]
PL13	Frame not ending with Terminate control character	81.1.7.5.3	Ensure MAC detects CRC error	MII:M	Yes [ ] N/A [ ]

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81.5.3.3 Data stream structure

Item	Feature	Subclause	Value/Comment	Status	Support
DS1	Frame transfer	81.2	Within XLGMII/CGMII data stream	MII:M	Yes [ ] N/A [ ]
DS2	Bit mapping	81.2	Per Figure 81–4	MII:M	Yes [ ] N/A [ ]
DS3	Content of <data>	81.2.3	Consist of data octets	MII:M	Yes [ ] N/A [ ]
DS4	Recognition of <efd>	81.2.4	Terminate recognized in any lane	MII:M	Yes [ ] N/A [ ]

81.5.3.4 XLGMII/CGMII signal functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	TX_CLK active edge	81.3.1.1	TXD and TXC sampled on the rising edge of TX_CLK	MII:M	Yes [ ] N/A [ ]
FS2	TX_CLK frequency	81.3.1.1	One-sixty-fourth of the MAC transmit data rate	MII:M	Yes [ ] N/A [ ]
FS3	TXC assertion and deassertion	81.3.1.2	Deasserted for data, asserted for control character	MII:M	Yes [ ] N/A [ ]
FS4	TXC clock	81.3.1.2	Synchronous to TX_CLK	MII:M	Yes [ ] N/A [ ]
FS5	TXD encoding	81.3.1.3	Per Table 81–3	MII:M	Yes [ ] N/A [ ]
FS6	TXD clock	81.3.1.3	Synchronous to TX_CLK	MII:M	Yes [ ] N/A [ ]
FS7	Start alignment	81.3.1.4	Start control character aligned to lane 0	MII:M	Yes [ ] N/A [ ]
FS8	RX_CLK active edge	81.3.2.1	RXD and RXC sampled on the rising edge of RX_CLK	MII:M	Yes [ ] N/A [ ]
FS9	RX_CLK frequency	81.3.2.1	One-sixty-fourth of the MAC receive data rate	MII:M	Yes [ ] N/A [ ]
FS10	Loss of receive signal	81.3.2.1	Source RX_CLK from nominal clock	PHY:M	Yes [ ] N/A [ ]
FS11	RXC assertion and deassertion	81.3.2.2	Deasserted for data, asserted for control character	PHY:M	Yes [ ] N/A [ ]
FS12	RXC clock	81.3.2.2	Synchronous to RX_CLK	MII:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
FS13	RXD decoding	81.3.2.3	Per Table 81–4	MII:M	Yes [ ] N/A [ ]
FS14	RXD clock	81.3.2.3	Synchronous to RX_CLK	MII:M	Yes [ ] N/A [ ]
FS15	Received Error control character	81.3.3.1	RS cause MAC FrameCheck-Error	MII:M	Yes [ ] N/A [ ]
FS16	DATA_VALID assertion	81.3.3.3	RS not assert DATA_VALID unless Start control character in lane 0	MII:M	Yes [ ] N/A [ ]

81.5.3.5 Link fault signaling state diagram

Item	Feature	Subclause	Value/Comment	Status	Support
LF1	Link fault signaling state diagram	81.3.4	Implement per Figure 81–11	MII:M	Yes [ ] N/A [ ]
LF2	link_fault = OK and MAC frames	81.3.4.2	RS services MAC frame transmission requests	MII:M	Yes [ ] N/A [ ]
LF3	link_fault = OK and no MAC frames	81.3.4.2	In absence of MAC frames, RS transmits Idle control characters	MII:M	Yes [ ] N/A [ ]
LF4	link_fault = Local Fault	81.3.4.2	RS transmits continuous Remote Fault Sequence ordered sets	MII:M	Yes [ ] N/A [ ]
LF5	link_fault = Remote Fault	81.3.4.2	RS transmits continuous Idle control characters	MII:M	Yes [ ] N/A [ ]

81.5.3.6 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Assertion of LPI in Tx direction	81.3.1.2	As defined in Table 81–3	LPI:M	Yes [ ] N/A [ ]
L2	Assertion of LPI wake time	81.4.2	As described by Figure 81–13	LPI:M	Yes [ ] N/A [ ]
L3	Assertion of LPI in Rx direction	81.3.2.2	As defined in Table 81–4	LPI:M	Yes [ ] N/A [ ]
L4	Signal DATA_NOT_VALID on PLS_DATA_VALID.indication	81.4.4	While detecting LP_IDLE on XLGMII or CGMII	LPI:M	Yes [ ] N/A [ ]

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81.5.3.7 Link Interruption

Item	Feature	Subclause	Value/Comment	Status	Support
*LINT1	Detection of Link Interruption	81.3.4	As defined in Table 81–5	O	Yes [ ] No [ ]
LINT2	CARRIER_STATUS response to Link Interruption	81.1.7.3	Set to CARRIER_ON if link_fault is Link Interruption	LINT1: M	Yes [ ] N/A [ ]

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82. Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R

82.1 Overview

82.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) that is common to two families of (40 Gb/s and 100 Gb/s) Physical Layer implementations, known as 40GBASE-R and 100GBASE-R. The 40GBASE-R PCS is a sublayer of the 40 Gb/s PHYs listed in Table 80–1. The 100GBASE-R PCS is a sublayer of the 100 Gb/s PHYs listed in Table 80–1. The terms 40GBASE-R and 100GBASE-R are used when referring generally to Physical Layers using the PCS defined in this clause.

Both 40GBASE-R and 100GBASE-R are based on a 64B/66B code. The 64B/66B code supports transmission of data and control characters, while maintaining robust error detection. Data distribution is introduced to support multiple lanes in the Physical Layer. Part of the distribution includes the periodic insertion of an alignment marker, which allows the receive PCS to align data from multiple lanes.

82.1.2 Relationship of 40GBASE-R and 100GBASE-R to other standards

Figure 82–1 depicts the relationships among the 40GBASE-R and 100GBASE-R sublayers (shown shaded), the Ethernet MAC and Reconciliation Sublayers, and the higher layers.

This clause borrows heavily from Clause 49. 64B/66B encoding is reused with appropriate changes made to support 8 byte alignment versus 4 byte alignment in Clause 49. In addition to 64B/66B encoding, there is a methodology to add alignment markers and distribute data to multiple lanes.

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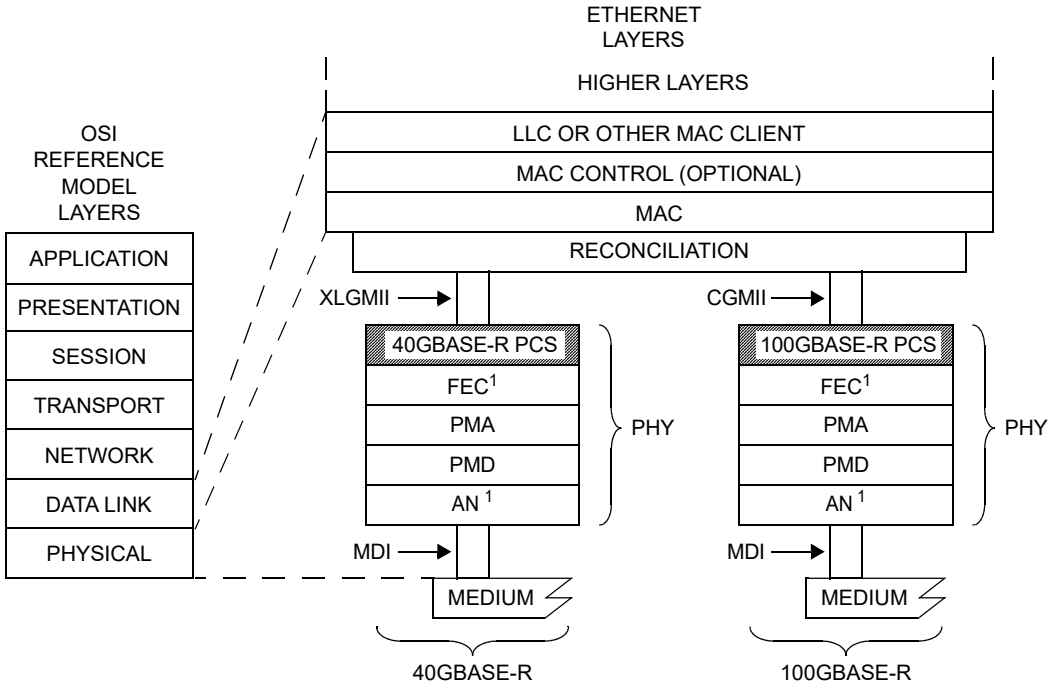
82.1.3 Summary of 40GBASE-R and 100GBASE-R sublayers

Figure 82–1 shows the relationship of the 40GBASE-R PCS and 100GBASE-R PCS sublayers (shown shaded) with other sublayers to the ISO Open System Interconnection (OSI) reference model.



AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 82–1—40GBASE-R and 100GBASE-R PCS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

82.1.3.1 Physical Coding Sublayer (PCS)

The PCS service interface is the Media Independent Interface (XLGMII/CGMII), which is defined in Clause 81. The 40 Gb/s variant of this is called the 40 Gb/s Media Independent Interface (XLGMII) and the 100 Gb/s variant of this interface is called the 100 Gb/s Media Independent Interface (CGMII). The XLGMII/CGMII provides a uniform interface to the Reconciliation Sublayer for all 40 Gb/s and 100 Gb/s PHY implementations.

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The 40GBASE-R and 100GBASE-R PCSs provide all services required by the XLGMII/CGMII, including the following:

a) Encoding (decoding) of eight XLGMII/CGMII data octets to (from) 66-bit blocks (64B/66B).
b) Transferring encoded data to (from) the PMA.
c) Compensation for any rate differences caused by the insertion or deletion of alignment markers or due to any rate difference between the XLMII/CGMII and PMA through the insertion or deletion of idle control characters.
d) Determining when a functional link has been established and informing the management entity via the MDIO when the PHY is ready for use.

82.1.4 Inter-sublayer interfaces

The upper interface of the PCS may connect to the Reconciliation Sublayer through the XLGMII/CGMII. The lower interface of the PCS connects to the PMA sublayer to support a PMD. If the optional BASE-R FEC sublayer is implemented (see Clause 74) and an optional physical instantiation, i.e., XLAUI or CAUI-n, is not implemented directly below the PCS sublayer, then the lower interface connects to the BASE-R FEC sublayer. For Physical Layers that use Clause 91 RS-FEC, if an optional physical instantiation (i.e., CAUI-n) is not implemented directly below the PCS sublayer, then the lower interface connects to the RS-FEC sublayer. The 40GBASE-R PCS has a nominal rate at the PMA/FEC service interface of 10.3125 Gtransfers/s per PCS lane, which provides capacity for the MAC data rate of 40 Gb/s. The 100GBASE-R PCS has a nominal rate at the PMA/FEC service interface of 5.15625 Gtransfers/s per PCS lane, which provides capacity for the MAC data rate of 100 Gb/s.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

82.1.4.1 PCS service interface (XLGMII/CGMII)

The PCS service interface allows the 40GBASE-R or 100GBASE-R PCS to transfer information to and from a PCS client. The PCS client is the Reconciliation Sublayer. The PCS Service Interface is precisely defined as the Media Independent Interface (XLGMII/CGMII) in Clause 81.

82.1.4.2 Physical Medium Attachment (PMA) or forward error correction (FEC) service interface

The PMA or FEC service interface for the PCS is described in an abstract manner and does not imply any particular implementation. The PMA/FEC Service Interface supports the exchange of encoded data between the PCS and PMA or FEC sublayer. The PMA or FEC service interface is defined in 83.3 or 94.2.1 and is an instance of the inter-sublayer service interface definition in 80.3 or 91.2.

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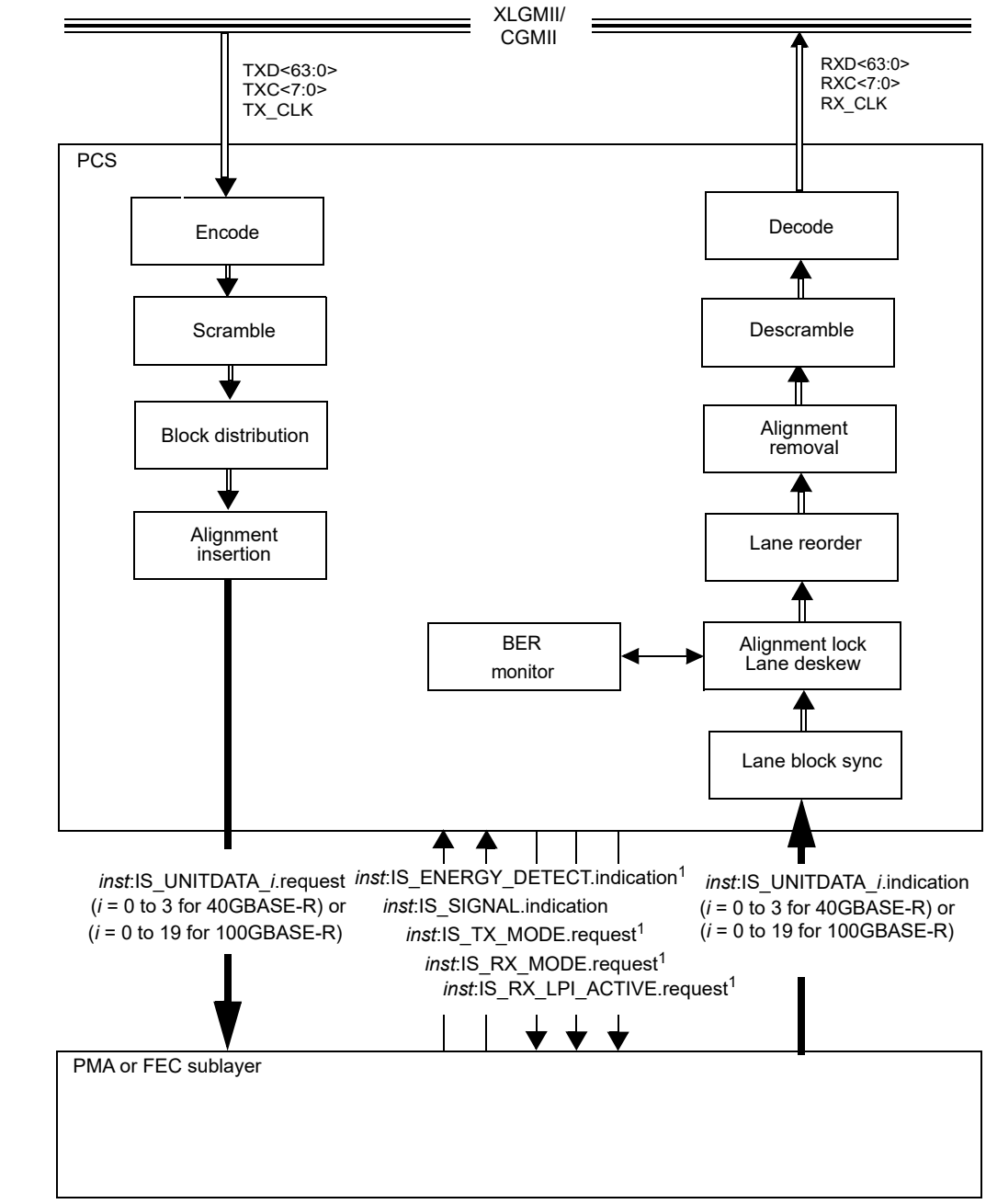
82.1.5 Functional block diagram

Figure 82–2 provides a functional block diagram of the 40GBASE-R PCS and 100GBASE-R PCS.



NOTE 1—FOR OPTIONAL EEE DEEP SLEEP CAPABILITY

Figure 82–2—Functional block diagram

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82.2 Physical Coding Sublayer (PCS)

82.2.1 Functions within the PCS

The 40GBASE-R and 100GBASE-R PCSs comprise the PCS Transmit and PCS Receive processes for each rate of operation. The PCS shields the Reconciliation Sublayer (and MAC) from the specific nature of the underlying channel. The PCS transmit channel and receive channel can each operate in normal mode or test-pattern mode.

When communicating with the XLGMII/CGMII, the PCS uses an eight octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals (TXC<n> = 1) and receive control signals (RXC<n> = 1). When communicating with the PMA, the PCS uses multiple serial streams, 4 encoded bit streams for a 40GBASE-R PCS, or 20 encoded bit streams for a 100GBASE-R PCS. Alignment to 64B/66B blocks is performed in the PCS. The PMA sublayer operates independently of block and packet boundaries. The PCS provides the functions necessary to map packets between the XLGMII/CGMII format and the PMA/FEC service interface format.

Note that these serial streams originate from a common clock in each direction, but may vary in phase and Skew dynamically.

When the transmit channel is in normal mode, the PCS Transmit process continuously generates blocks based upon the TXD <63:0> and TXC <7:0> signals on the XLGMII/CGMII. The blocks are scrambled and then distributed to individual PCS lanes. After distribution, alignment marker blocks are periodically added to each PCS lane. Transmit data-units are sent to the service interface via the *inst*:IS_UNITDATA_*i*.request primitive. In these primitives, the *inst* can be either FEC or PMA depending on which sublayer is adjacent to the PCS sublayer.

When the transmit channel is in test-pattern mode, a test pattern is packed into the transmit data-units that are sent to the PMA/FEC service interface via the *inst*:IS_UNITDATA_*i*.request primitive.

When the receive channel is in normal or test-pattern mode, the PCS Synchronization process continuously monitors *inst*:IS_SIGNAL.indication(SIGNAL_OK). When SIGNAL_OK indicates OK, then the PCS Synchronization process accepts data-units via the *inst*:IS_UNITDATA_*i*.indication primitive. It attains block synchronization based on the 2-bit synchronization headers on each one of the PCS lanes. Once block synchronization is found on a PCS lane, then alignment marker lock can be attained by searching for valid alignment markers. After alignment markers are found on all PCS lanes, the PCS lanes can be reordered and deskewed. Note that a particular transmit PCS lane can be received on any receive lane of the service interface due to the Skew and multiplexing that occurs in the path.

The PCS deskew process conveys received blocks to the PCS Receive process. The PCS deskew process deskews and aligns the individual PCS lanes, removes the alignment markers, forms a single stream, and sets the align_status flag to indicate whether the PCS has obtained alignment.

When the PCS deskew process has obtained alignment, the BER monitor process monitors the signal quality asserting hi_ber if excessive errors are detected. When align_status is asserted and hi_ber is deasserted, the PCS Receive process continuously accepts blocks and generates RXD <63:0> and RXC <7:0> on the MII.

When the receive channel is in test-pattern mode, the BER monitor process may be disabled. The Receive process will be held in the RX_INIT state. The received bits will be compared to the test pattern and errors counted.

The PCS shall provide transmit test-pattern mode for the scrambled idle pattern (see 82.2.11), and shall provide receive test-pattern mode for the scrambled idle pattern (see 82.2.11). Test-pattern mode is activated

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separately for transmit and receive. The PCS shall support transmit test-pattern mode and receive test-pattern mode operating simultaneously so as to support loopback testing.

82.2.2 Use of blocks

The PCS maps XLGMII/CGMII signals into 66-bit blocks, and vice versa, using a 64B/66B coding scheme. The synchronization headers of the blocks allow establishment of block boundaries by the PCS Synchronization process. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks as defined in 82.2.3.

82.2.3 64B/66B transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters. The encodings defined by the transmission code ensure that sufficient transitions are present in the PHY bit stream to make clock recovery possible at the receiver. The encoding also preserves the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, the synchronization headers of the code enable the receiver to achieve block alignment on the incoming PHY bit stream. The 64B/66B transmission code specified for use in this standard is a run-length-limited code.[145]

The relationship of block bit positions relative to XLGMII/CGMII, PMA, and other PCS functions is illustrated in Figure 82–3 for transmit and Figure 82–4 for receive. These figures illustrate the processing of a block containing 8 data octets. See 82.2.3.3 for information on how blocks containing control characters are mapped into 66-bit blocks. Note that the sync header is generated by the encoder and bypasses the scrambler.

82.2.3.1 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/66B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. The control characters /I/ and /E/ are labeled C_0 to C_7. The control character /Q/ for a sequence ordered set is labeled as O_0 since it is only valid on the first octet of the XLGMII/CGMII. The control character for start is labeled as S_0 for the same reason. The control character for terminate is labeled as T_0 to T_7. The four trailing zero data octets in ordered sets are labeled as Z_4 to Z_7.

One XLGMII/CGMII transfer provides eight characters that are encoded into one 66-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XLGMII/CGMII transfer.

Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled TxB<65:0> and RxB<65:0>, respectively, where TxB<0> and RxB<0> represent the first transmitted bit. The value of the sync header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

[145]In 10GBASE-R the run length is limited to 66 bits, but in 40GBASE-R and 100GBASE-R, when multiplexing occurs in the PMA, this guaranteed run length limit increases. For example, if two PCS lanes are multiplexed in the PMA, then the possible run length would double.

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82.2.3.2 Transmission order

Block bit transmission order shall be as illustrated in Figure 82–3 and Figure 82–4. Note that these figures show the mapping from XLGMII/CGMII to 64B/66B block for a block containing eight data characters.

82.2.3.3 Block structure

Blocks consist of 66 bits. The first two bits of a block are the synchronization header (sync header). Blocks are either data blocks or control blocks. The sync header is 01 for data blocks and 10 for control blocks. Thus, there is always a transition between the first two bits of a block. The remainder of the block contains the payload. The payload is scrambled and the sync header bypasses the scrambler. Therefore, the sync header is the only position in the block that is always guaranteed to contain a transition. This feature of the code is used to obtain block synchronization.

Data blocks contain eight data characters. Control blocks begin with an 8-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start, Terminate character, or ordered set, that character is implied by the block type field. Other control characters are encoded in a 7-bit control code. Each control block encodes eight characters.

The format of the blocks is as shown in Figure 82–5. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 66-bit block. These characters are either data characters or control characters and, when transferred across the XLGMII/CGMII, the corresponding TXC or RXC bit is set accordingly. Within the Input Data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control characters and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt.

All unused values of block type field[146] are invalid; they shall not be transmitted and shall be considered an error if received.

[146]The block type field values have been chosen to have a 4-bit Hamming distance between them. There are five unused values that maintain this Hamming distance: 0x00, 0x2D, 0x33, 0x55, and 0x66.

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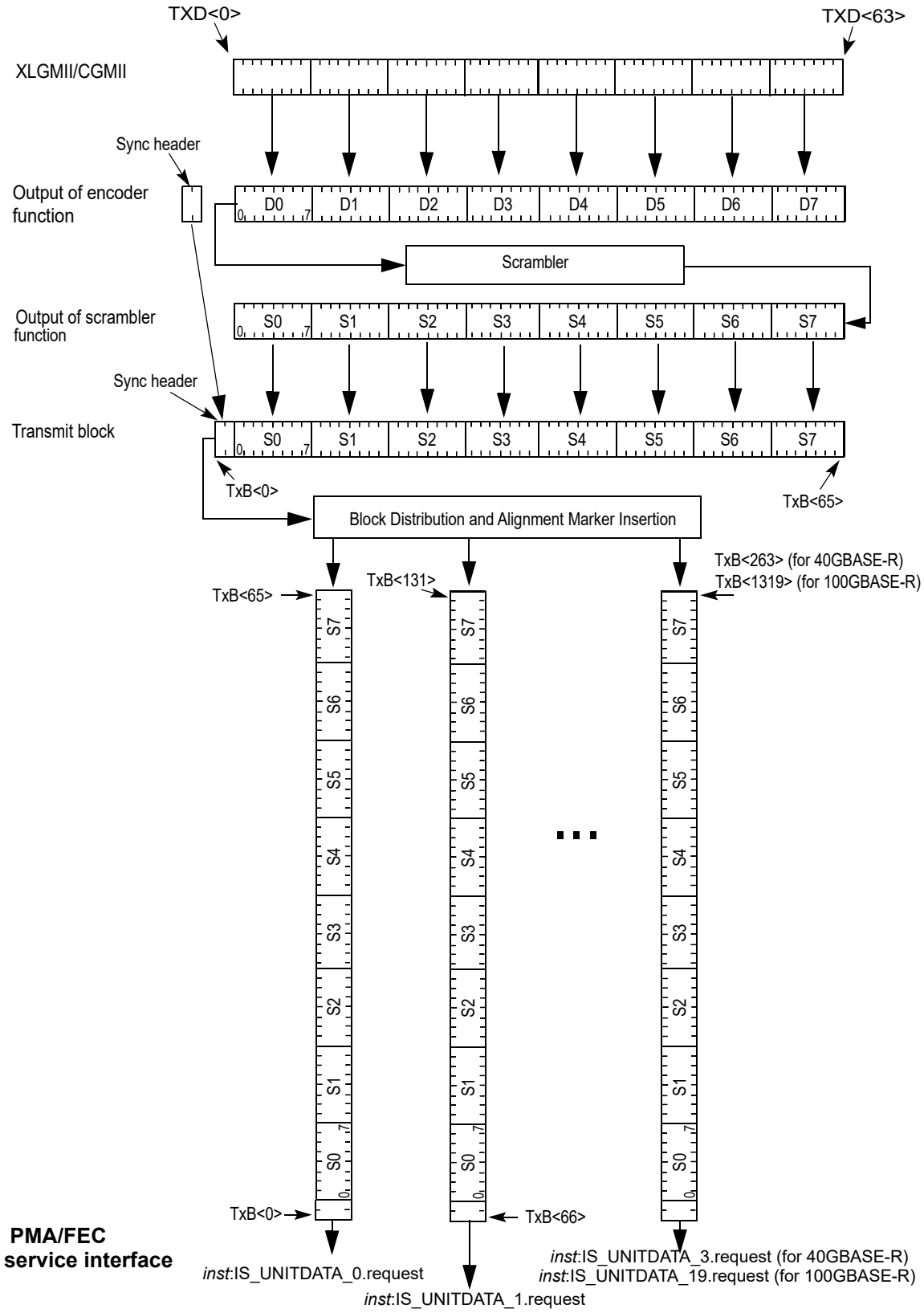

Figure 82–3—PCS Transmit bit ordering

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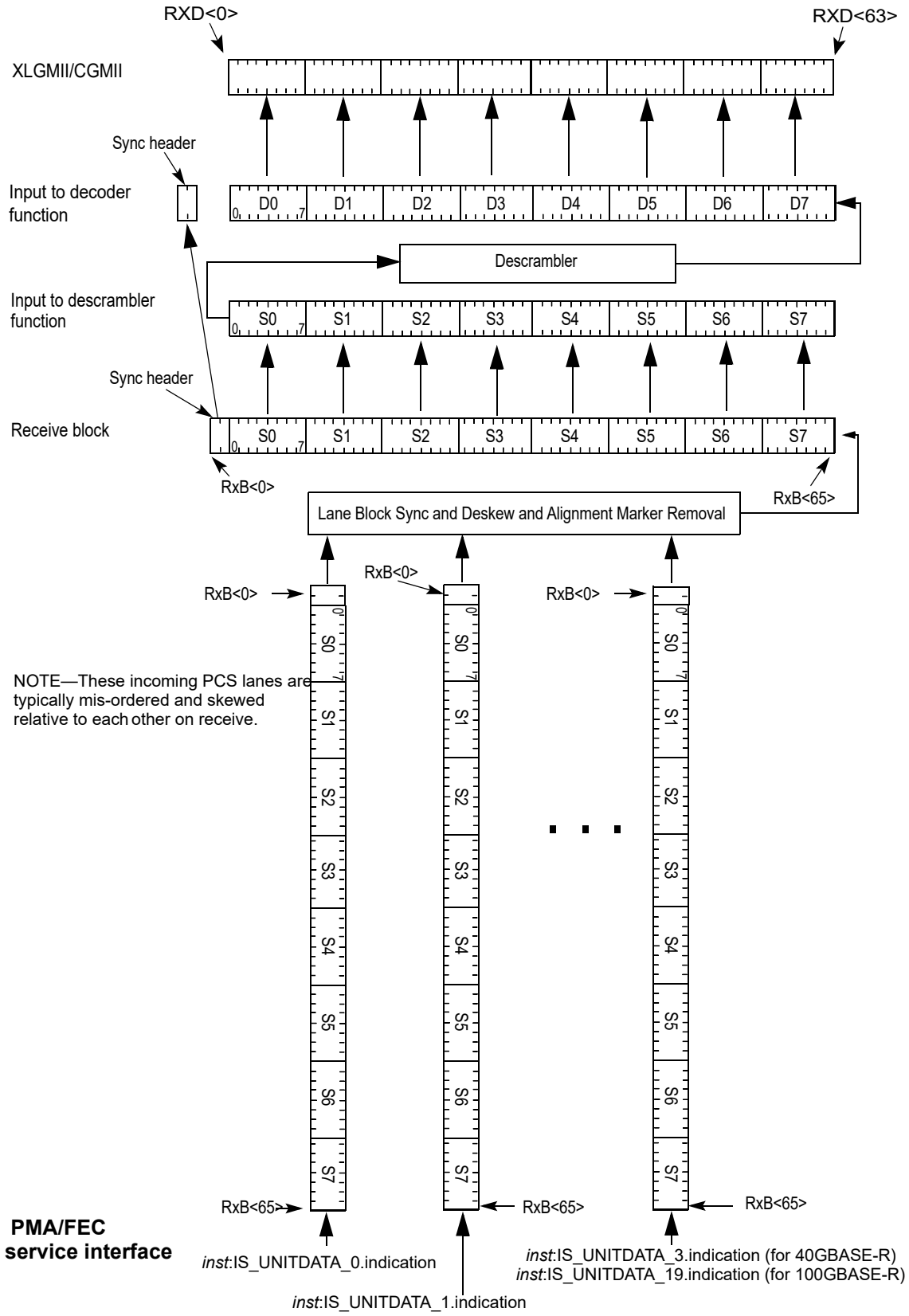

Figure 82–4—PCS Receive bit ordering

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Input Data	Sync	Block Payload							
Bit Position: / Data Block Format:	0 1	2							65
$D_0\,D_1\,D_2\,D_3\,D_4\,D_5\,D_6\,D_7$	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		**Block Type Field**							
$C_0\,C_1\,C_2\,C_3\,C_4\,C_5\,C_6\,C_7$	10	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$S_0\,D_1\,D_2\,D_3\,D_4\,D_5\,D_6\,D_7$	10	0x78	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3\,Z_4\,Z_5\,Z_6\,Z_7$	10	0x4B	D_1	D_2	D_3	O_0	0x000_0000		
$T_0\,C_1\,C_2\,C_3\,C_4\,C_5\,C_6\,C_7$	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,T_1\,C_2\,C_3\,C_4\,C_5\,C_6\,C_7$	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,T_2\,C_3\,C_4\,C_5\,C_6\,C_7$	10	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,T_3\,C_4\,C_5\,C_6\,C_7$	10	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3\,T_4\,C_5\,C_6\,C_7$	10	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3\,D_4\,T_5\,C_6\,C_7$	10	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\,D_1\,D_2\,D_3\,D_4\,D_5\,T_6\,C_7$	10	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\,D_1\,D_2\,D_3\,D_4\,D_5\,D_6\,T_7$	10	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 82–5—64B/66B block formats

WARNING

The mapping of 40GBASE-R PCS blocks into OPU3 specified in ITU-T G.709 depends on the set of control block types shown in Figure 82–5. Any deviation from the coding specified in Figure 82–5 will break the mapping and may prevent 40GBASE-R PCS blocks from being mapped into OPU3 (see ITU-T G.709 for more details).

82.2.3.4 Control codes

The same set of control characters are supported by the XLGMII/CGMII and the PCS. The representations of the control characters are the control codes. XLGMII/CGMII encodes a control character into an octet (an eight bit value). The 40GBASE-R and 100GBASE-R PCS encode the start and terminate control characters implicitly by the block type field. The 40GBASE-R and 100GBASE-R PCS encode the ordered set control codes using the block type field. The 40GBASE-R and 100GBASE-R PCS encode each of the other control characters into a 7-bit control code.

The control characters and their mappings to 40GBASE-R and 100GBASE-R control codes and XLGMII/CGMII control codes are specified in Table 82–1. All XLGMII/CGMII, 40GBASE-R, and 100GBASE-R control code values that do not appear in the table shall not be transmitted and shall be considered an error if received. The ability to transmit or receive Low Power Idle (LPI) is required for PHYs that support EEE (see Clause 78). If EEE has not been negotiated, LPI shall not be transmitted and shall be treated as an error if received.

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82.2.3.5 Valid and invalid blocks

A block is invalid if any of the following conditions exists:

a) The sync header has a value of 00 or 11.
b) The block type field contains an invalid value (one not included in Figure 82–5).
c) Any control character contains a value not included in Table 82–1.
d) The set of eight XLGMII/CGMII characters does not have a corresponding block format in Figure 82–5.

82.2.3.6 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XLGMII/CGMII. Idle control characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 8. /I/s may be added following idle control characters or ordered sets. They shall not be added while data is being received.

Table 82–1—Control codes

Control character	Notation	XLGMII/ CGMII control code	40/100GBASE-R O code[a]	40GBASE-R and 100GBASE-R control code
idle	/I/	0x07		0x00
LPI	/LI/	0x06		0x06
start	/S/	0xFB		Encoded by block type field
terminate	/T/	0xFD		Encoded by block type field
error	/E/	0xFE		0x1E
Sequence ordered set	/Q/	0x9C	0x0	Encoded by block type 0x4B plus O code, control codes are set to 0x00

[a] INCITS T11 Fibre Channel uses O code 0xF for the signal ordered set. OIF uses O code 0x5 for the FlexE [B59] ordered set. ITU-T uses O code 0xC for the G.8312 [B47] MTN path ordered set.

To communicate LPI, the LPI control character /LI/ is sent continuously in place of /I/. LPI control characters are transmitted when LPI control characters are received from the XLGMII or CGMII. LPI characters may be added or deleted by the PCS to adapt between clock rates in a similar manner to idle control characters. /LI/ insertion and deletion shall occur in groups of 8. /LI/s inserted for clock compensation may only be inserted following other LPI characters.

82.2.3.7 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XLGMII/CGMII (TXD<7:0> and RXD<7:0>). Receipt of an /S/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /S/ as the first character of the block.

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82.2.3.8 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets vary in length, the /T/ can occur on any octet of the XLGMII/CGMII and on any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/ or an /E/.

82.2.3.9 ordered set (/O/)

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and local fault status. Ordered sets consist of a control character followed by three data characters followed by four zero data characters on the XLGMII/CGMII. Ordered sets always begin on the first octet of the XLGMII/CGMII. 40 Gigabit and 100 Gigabit Ethernet use one kind of ordered set: the sequence ordered set (see 81.3.4). The ordered set control character /Q/ indicates the start of an ordered set. The block type field plus the O code encode the specific control character for the ordered set. See Table 82–1 for the mapping.

Sequence ordered sets may be deleted by the PCS to adapt between clock rates. Such deletion shall only occur when two consecutive sequence ordered sets have been received and only one of the two ordered sets may be deleted. Only idle control characters may be inserted for clock compensation.

82.2.3.10 Error (/E/)

In both the 64B/66B encoder and decoder, the /E/ is generated whenever an /E/ is detected. The /E/ is also generated when invalid blocks are detected. The /E/ allows the PCS to propagate detected errors. See R_TYPE and T_TYPE function definitions in 82.2.19.2.3 for further information.

82.2.4 Transmit process

The transmit process generates blocks based upon the TXD<63:0> and TXC<7:0> signals received from the XLGMII/CGMII. One XLGMII/CGMII data transfer is encoded into one 66-bit block. It takes 66 *inst*:IS_UNITDATA_*i* transfers to send a 66-bit block of data on each of the PCS lanes. The transmit process may delete idle control characters or sequence ordered sets to accommodate the transmission of alignment markers. If the PCS transmit process spans multiple clock domains, it may also perform clock rate compensation via the deletion of idle control characters or sequence ordered sets or the insertion of idle control characters.

There are sufficient idle control characters to delete in order to make room for alignment markers, in addition to handling clock compensation. Idle control characters or sequence ordered sets are removed, if necessary, to accommodate the insertion of the 66-bit alignment markers. See 82.2.3.6 for more details.

The transmit process generates blocks as specified in the transmit process state diagram. The contents of each block are contained in a vector tx_coded<65:0>, which is passed to the scrambler. tx_coded<1:0> contains the sync header and the remainder of the bits contain the block payload.

82.2.5 Scrambler

The payload, tx_coded<65:2>, is scrambled with a self-synchronizing scrambler. The scrambler is identical to the scrambler used in Clause 49, see 49.2.6 for the definition of the scrambler. The sync bits, tx_coded<1:0>, are not scrambled.

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82.2.6 Block distribution

Once the data is encoded and scrambled, it is distributed to multiple PCS lanes, 66-bit blocks at a time in a round robin distribution from the lowest to the highest numbered PCS lanes. This allows the PCS to support multiple physical lanes in the PMD and XLAUI or CAUI-n interfaces (see Annex 83A, Annex 83B, Annex 83D, and Annex 83E). The 40GBASE-R PCS distributes the 66-bit blocks to 4 PCS lanes, and the 100GBASE-R PCS distributes the blocks to 20 PCS lanes. The distribution process is shown in Figure 82–6.

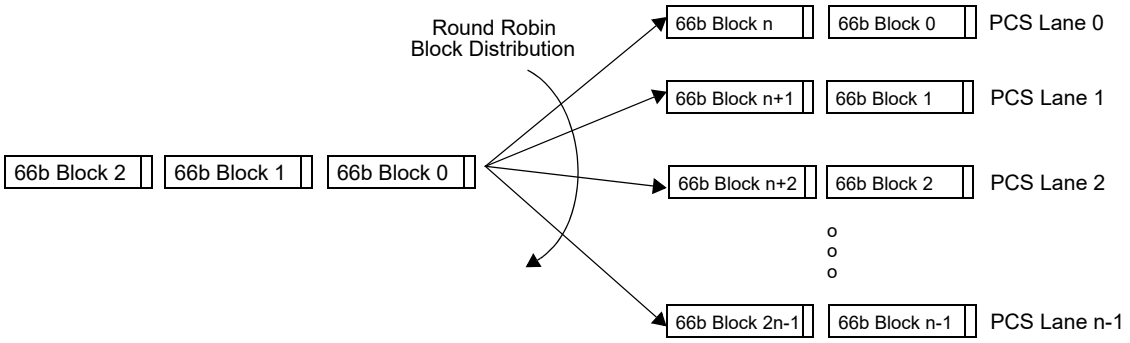

Figure 82–6—PCS Block distribution

82.2.7 Alignment marker insertion

In order to support deskew and reordering of individual PCS lanes at the receive PCS, alignment markers are added periodically to each PCS lane. The alignment marker has the form of a specially defined 66-bit block with a control block sync header. These markers interrupt any data transfer that is already in progress. This allows alignment markers to be inserted into all PCS lanes at the same time. If necessary, room for the alignment markers is created by periodically deleting IPG from the XLGMII/CGMII data stream. Other special properties of the alignment markers are that they are not scrambled and do not conform to the encoding rules as outlined in Figure 82–5. This is possible because the alignment markers are added after encoding is performed in the transmit PCS and the alignment markers are removed before 64B/66B decoding is performed in the receive PCS. The alignment markers are not scrambled in order to allow the receiver to find the alignment markers, deskew the PCS lanes, and reassemble the aggregate stream before descrambling is performed. The alignment markers themselves are formed from a known pattern that is defined to be balanced and with many transitions and therefore scrambling is not necessary for the alignment markers. The alignment markers shall be inserted after every 16383 66-bit blocks on each PCS lane. Alignment marker insertion is shown in Figure 82–7 and Figure 82–8.

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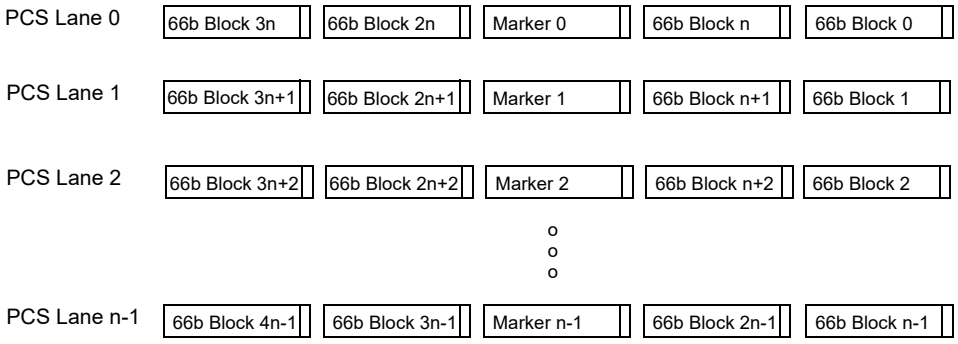

Figure 82–7—Alignment marker insertion

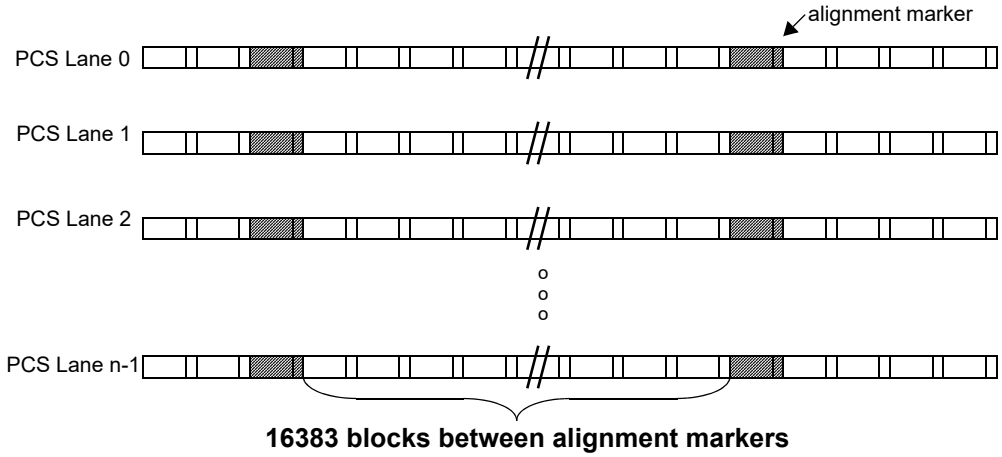

Figure 82–8—Alignment marker insertion period

The format of the alignment markers is shown in Figure 82–9.

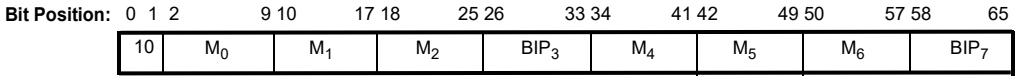

Figure 82–9—Alignment marker format

The content of the alignment markers shall be as shown in Table 82–2 for 100GBASE-R and in Table 82–3 for 40GBASE-R. The contents depend on the PCS lane number and the octet number. Note that M_4 through M_6 are the bit-wise inversion of M_0 through M_2, respectively. Also BIP_7 is the bit-wise inversion of BIP_3. This property allows the alignment markers to be DC-balanced. Lane markers 0 to 19 from Table 82–2 are used for the 100GBASE-R PCS and lane markers 0 to 3 from Table 82–3 are used for the 40GBASE-R PCS. As an example, the lane marker for 100GBASE-R lane number 0 is sent as (left most bit sent first):

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10 10000011 00010110 10000100 BIP_3 01111100 11101001 01111011 BIP_7

After the alignment markers are inserted, data is sent to the PMA or FEC sublayer adjacent to the PCS.

Table 82–2—100GBASE-R Alignment marker encodings

PCS lane number	Encoding[a] {M_0, M_1, M_2, BIP_3, M_4, M_5, M_6, BIP_7}	PCS lane number	Encoding[a] {M_0, M_1, M_2, BIP_3, M_4, M_5, M_6, BIP_7}
0	0xC1, 0x68, 0x21, BIP_3, 0x3E, 0x97, 0xDE, BIP_7	10	0xFD, 0x6C, 0x99, BIP_3, 0x02, 0x93, 0x66, BIP_7
1	0x9D, 0x71, 0x8E, BIP_3, 0x62, 0x8E, 0x71, BIP_7	11	0xB9, 0x91, 0x55, BIP_3, 0x46, 0x6E, 0xAA, BIP_7
2	0x59, 0x4B, 0xE8, BIP_3, 0xA6, 0xB4, 0x17, BIP_7	12	0x5C, 0x B9, 0xB2, BIP_3, 0xA3, 0x46, 0x4D, BIP_7
3	0x4D, 0x95, 0x7B, BIP_3, 0xB2, 0x6A, 0x84, BIP_7	13	0x1A, 0xF8, 0xBD, BIP_3, 0xE5, 0x07, 0x42, BIP_7
4	0xF5, 0x07, 0x09, BIP_3, 0x0A, 0xF8, 0xF6, BIP_7	14	0x83, 0xC7, 0xCA, BIP_3, 0x7C, 0x38, 0x35, BIP_7
5	0xDD, 0x14, 0xC2, BIP_3, 0x22, 0xEB, 0x3D, BIP_7	15	0x35, 0x36, 0xCD, BIP_3, 0xCA, 0xC9, 0x32, BIP_7
6	0x9A, 0x4A, 0x26, BIP_3, 0x65, 0xB5, 0xD9, BIP_7	16	0xC4, 0x31, 0x4C, BIP_3, 0x3B, 0xCE, 0xB3, BIP_7
7	0x7B, 0x45, 0x66, BIP_3, 0x84, 0xBA, 0x99, BIP_7	17	0xAD, 0xD6, 0xB7, BIP_3, 0x52, 0x29, 0x48, BIP_7
8	0xA0, 0x24, 0x76, BIP_3, 0x5F, 0xDB, 0x89, BIP_7	18	0x5F, 0x66, 0x2A, BIP_3, 0xA0, 0x99, 0xD5, BIP_7
9	0x68, 0xC9, 0xFB, BIP_3, 0x97, 0x36, 0x04, BIP_7	19	0xC0, 0xF0, 0xE5, BIP_3, 0x3F, 0x0F, 0x1A, BIP_7

[a]Each octet is transmitted LSB to MSB.

Table 82–3—40GBASE-R Alignment marker encodings

PCS lane number	Encoding[a] {M_0, M_1, M_2, BIP_3, M_4, M_5, M_6, BIP_7}
0	0x90, 0x76, 0x47, BIP_3, 0x6F, 0x89, 0xB8, BIP_7
1	0xF0, 0xC4, 0xE6, BIP_3, 0x0F, 0x3B, 0x19, BIP_7
2	0xC5, 0x65, 0x9B, BIP_3, 0x3A, 0x9A, 0x64, BIP_7
3	0xA2, 0x79, 0x3D, BIP_3, 0x5D, 0x86, 0xC2, BIP_7

[a]Each octet is transmitted LSB to MSB.

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82.2.8 BIP calculations

A PCS lane BIP field is carried in each PCS Lane alignment marker. This allows an accurate and fast measure of the bit error ratio of a given PCS Lane. This information is used to update error counters; no state machines use this information.

Each alignment marker has two Bit Interleaved Parity fields, BIP_3 and BIP_7. BIP_7 is a bit-wise inversion of BIP_3 in order to keep the alignment marker DC-balanced. The BIP_3 field contains the result of a bit interleaved parity calculation. Each bit in the BIP field is an even parity calculation over all of the previous specified bits of a given PCS Lane, from and including the previous alignment marker, but not including the current alignment marker. Using the bit definitions as shown in Figure 82–9, Table 82–4 has the bit assignments for each BIP_3 bit. As an example, BIP_3 bit 0 contains the result of XORing 131072 bits from 16384 66-bit words. BIP_3 bit 3 and bit 4 also include one sync header bit from each 66-bit word. Bit 3 and bit 4 each contain the result of XORing 147456 bits.

Table 82–4—BIP_3 bit assignments

BIP_3 bit number	Assigned 66-bit word bits
0	2, 10, 18, 26, 34, 42, 50, 58
1	3, 11, 19, 27, 35, 43, 51, 59
2	4, 12, 20, 28, 36, 44, 52, 60
3	0, 5, 13, 21, 29, 37, 45, 53, 61
4	1, 6, 14, 22, 30, 38, 46, 54, 62
5	7, 15, 23, 31, 39, 47, 55, 63
6	8, 16, 24, 32, 40, 48, 56, 64
7	9, 17, 25, 33, 41, 49, 57, 65

BIP_3 and BIP_7 are transmitted LSB to MSB. As an example, with BIP_3 = 0x0F, the PCS lane marker for 100GBASE-R lane number 0 is sent as (left most bit sent first):

10 10000011 00010110 10000100 11110000 01111100 11101001 01111011 00001111

If the EEE capability is supported, BIP statistics are only updated when the receiver is in the RX_ACTIVE state (see Figure 82–19). In all other states, the running parity is not calculated. The BIP statistics shall be first updated after transitioning from RAMs to normal AMs on the first received normal AM when LPI_FW is FALSE and on the second received AM after entering the RX_ACTIVE state when LPI_FW is TRUE.

82.2.9 Rapid alignment marker insertion

For the optional EEE capability, an alternate method of alignment is used when operating in the deep sleep low power state. Rapid Alignment Markers (RAMs) function in a similar manner to the alignment markers described in 82.2.7. Normal alignment markers are sent when the transmitter has an LPI transmit state of TX_ACTIVE; RAMs are sent in the TX_WAKE2 state until down_count_done is TRUE and in all the other LPI transmit states. Additionally, the BIP component defined for alignment markers is replaced by a count

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down field (CD) so that the transition from RAMs to normal alignment markers can be indicated. The RAMs shall be inserted after every 7 66-bit blocks on each 100G PCS lane and every 15 66-bit blocks on each 40G PCS lane. RAM insertion is performed in the same manner as shown in Figure 82–7 and Figure 82–10. The transition from RAMs to normal alignment markers is shown in Figure 82–10. The count down field is also used to communicate some of the states of the tx_mode when it is not being used to coordinate the transition. After the LPI Transmit state diagram transitions from TX_ACTIVE to TX_SLEEP, the first RAM shall be inserted after at least one block of /LI/ has been transmitted on PCS lane 0. In order to force the RAMs to coincide with the start of an FEC block, the distance between the first RAM and preceding normal alignment marker shall be a multiple of 4 66-bit blocks.

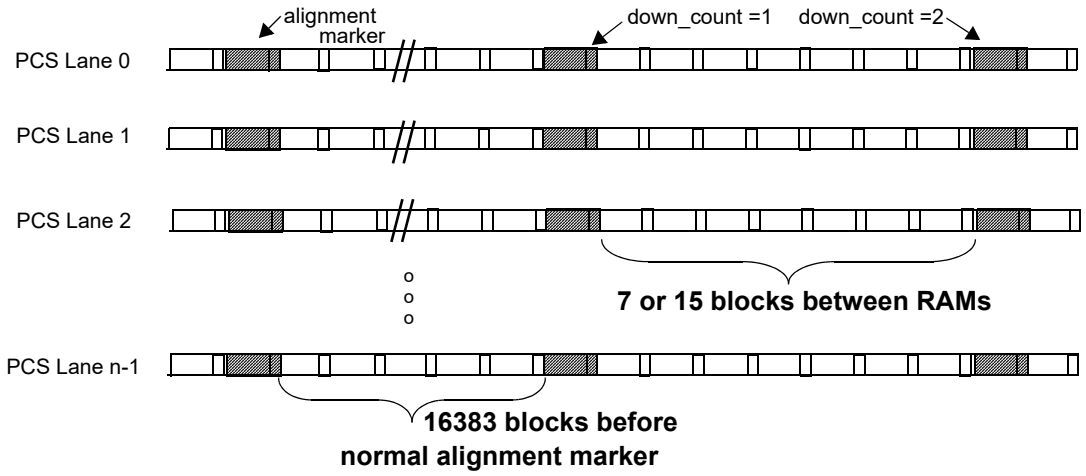

Figure 82–10—RAM transition

The format of the RAMs is shown in Figure 82–11.

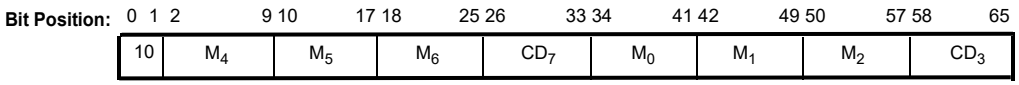

Figure 82–11—RAM format

The content of the RAMs shall be as shown in Table 82–5 for 100GBASE-R or Table 82–6 for 40GBASE-R. Note that these are similar to normal alignment markers, with CD_3 replacing BIP_3 and CD_7 replacing BIP_7, and also M_0 through M_2 and CD_3 swapped with M_4 through M_6 and CD_7, respectively. As an example, the lane marker for 100GBASE-R lane number 0 is sent as (left most bit sent first):

10 01111100 11101001 01111011 CD_7 10000011 00010110 10000100 CD_3

After the RAMs are inserted, data is sent to the PMA or FEC sublayer adjacent to the PCS.

The value of the CD_3 field is derived by the bit-wise XOR of the down_count variable with the M_0 value for the lane (therefore the last 5 RAMs sent by a 100GBASE-R PCS on PCS lane 0 would have CD_3 values: 0xC4, 0xC5, 0xC2, 0xC3, 0xC0; for PCS lane 1 these would be: 0x98, 0x99, 0x9E, 0x9F, 0x9C). The CD_7 field is the bit-wise inversion of CD_3. The CD field is used by the link partner to understand the expected

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transition from RAMs to normal AMs. It may also be used by a device with a detached PMA or FEC sublayer to infer the state of the PCS.

Table 82–5—100GBASE-R RAM encodings

PCS lane number	Encoding[a] {M_4, M_5, M_6, CD_7, M_0, M_1, M_2, CD_3}	PCS lane number	Encoding[a] {M_4, M_5, M_6, CD_7, M_0, M_1, M_2, CD_3}
0	0x3E, 0x97, 0xDE, CD_7, 0xC1, 0x68, 0x21, CD_3	10	0x02, 0x93, 0x66, CD_7, 0xFD, 0x6C, 0x99, CD_3
1	0x62, 0x8E, 0x71, CD_7, 0x9D, 0x71, 0x8E, CD_3	11	0x46, 0x6E, 0xAA, CD_7, 0xB9, 0x91, 0x55, CD_3
2	0xA6, 0xB4, 0x17, CD_7, 0x59, 0x4B, 0xE8, CD_3	12	0xA3, 0x46, 0x4D, CD_7, 0x5C, 0xB9, 0xB2, CD_3
3	0xB2, 0x6A, 0x84, CD_7, 0x4D, 0x95, 0x7B, CD_3	13	0xE5, 0x07, 0x42, CD_7, 0x1A, 0xF8, 0xBD, CD_3
4	0x0A, 0xF8, 0xF6, CD_7, 0xF5, 0x07, 0x09, CD_3	14	0x7C, 0x38, 0x35, CD_7, 0x83, 0xC7, 0xCA, CD_3
5	0x22, 0xEB, 0x3D, CD_7, 0xDD, 0x14, 0xC2, CD_3	15	0xCA, 0xC9, 0x32, CD_7, 0x35, 0x36, 0xCD, CD_3
6	0x65, 0xB5, 0xD9, CD_7, 0x9A, 0x4A, 0x26, CD_3	16	0x3B, 0xCE, 0xB3, CD_7, 0xC4, 0x31, 0x4C, CD_3
7	0x84, 0xBA, 0x99, CD_7, 0x7B, 0x45, 0x66, CD_3	17	0x52, 0x29, 0x48, CD_7, 0xAD, 0xD6, 0xB7, CD_3
8	0x5F, 0xDB, 0x89, CD_7, 0xA0, 0x24, 0x76, CD_3	18	0xA0, 0x99, 0xD5, CD_7, 0x5F, 0x66, 0x2A, CD_3
9	0x97, 0x36, 0x04, CD_7, 0x68, 0xC9, 0xFB, CD_3	19	0x3F, 0x0F, 0x1A, CD_7, 0xC0, 0xF0, 0xE5, CD_3

[a]Each octet is transmitted LSB to MSB.

Table 82–6—40GBASE-R RAM encodings

PCS lane number	Encoding[a] {M_4, M_5, M_6, CD_7, M_0, M_1, M_2, CD_3}
0	0x6F, 0x89, 0xB8, CD_7, 0x90, 0x76, 0x47, CD_3
1	0x0F, 0x3B, 0x19, CD_7, 0xF0, 0xC4, 0xE6, CD_3
2	0x3A, 0x9A, 0x64, CD_7, 0xC5, 0x65, 0x9B, CD_3
3	0x5D, 0x86, 0xC2, CD_7, 0xA2, 0x79, 0x3D, CD_3

[a]Each octet is transmitted LSB to MSB.

82.2.10 PMA or FEC Interface

When the transmit channel is operating in normal mode, the 40GBASE-R PCS sends four data streams via *inst*:IS_UNITDATA_*i*.request primitives and the 100GBASE-R PCS sends twenty data streams via *inst*:IS_UNITDATA_*i*.request primitives.

The *inst*:IS_UNITDATA_*i*.request primitives are separate serial streams of bits. Since 66-bit blocks were distributed to each lane, that means for the 40GBASE-R PCS: bits 0 to 65 are sent on PCSL 0, bits 66 to 131

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are sent on PCSL 1; bits 132 to 197 are sent on PCSL 2, bits 198 to 263 are sent on PCSL 3, then bits 264 to 329 are sent on PCSL 0 etc.

For 100GBASE-R it is: bits 0 to 65 on PCSL 0, bits 66 to 131 on PCSL 1, bits 132 to 197 on PCSL 2, bits 198 to 263 on PCSL 3, bits 264 to 329 on PCSL 4, bits 330 to 395 on PCSL 5, bits 396 to 461 on PCSL 6, bits 462 to 527 on PCSL 7, bits 528 to 593 on PCSL 8, bits 594 to 659 on PCSL 9, bits 660 to 725 on PCSL 10, bits 726 to 791 on PCSL 11, bits 792 to 857 on PCSL 12, bits 858 to 923 on PCSL 13, bits 924 to 989 on PCSL 14, bits 990 to 1055 on PCSL 15, bits 1056 to 1121 on PCSL 16, bits 1122 to 1187 on PCSL 17, bits 1188 to 1253 on PCSL 18, bits 1254 to 1319 on PCSL 19, then bits 1320 to 1385 on PCSL 0, etc.

82.2.11 Test-pattern generators

The PCS shall have the ability to generate and detect a scrambled idle test pattern. This test-pattern mode is suitable for receiver tests and for certain transmitter tests.

When a scrambled idle pattern is enabled, the test pattern is generated by the scrambler. No seeding of the scrambler is required during test-pattern operation. The input to the scrambler is a control block (block type=0x1E) with all idles as defined in Figure 82–5. Note that the sync headers and alignment markers are added to the stream so that the receive PCS can align and deskew the PCS lanes.

If a Clause 45 MDIO is implemented, then control of the test-pattern generation is from the BASE-R PCS test-pattern control register (bit 3.42.3).

When the transmit channel is operating in test-pattern mode, the encoded bit stream is distributed to the PCS Lanes as in normal operation (see 82.2.4).

82.2.12 Block synchronization

When the receive channel is operating in normal mode, the block synchronization function receives data via 4 (for 40GBASE-R) or 20 (for 100GBASE-R) IS_UNITDATA_*i*.indication primitives. The PCS forms 4 or 20 bit streams from the primitives by concatenating the bits from the indications of each primitive in order from each *inst*:IS_UNITDATA_0.indication to *inst*:IS_UNITDATA_3.indication or *inst*:IS_UNITDATA_0.indication to *inst*:IS_UNITDATA_19.indication. It obtains lock to the 66-bit blocks in each bit stream using the sync headers and outputs 66-bit blocks. Block lock is obtained as specified in the block lock state diagram shown in Figure 82–12.

If EEE is not supported then block_lock is identical to rx_block_lock. Otherwise the relationship between block_lock and rx_block_lock is given by Figure 82–19.

82.2.13 PCS lane deskew

Once the receiver achieves block lock on a lane, then it begins obtaining alignment marker lock as specified in the alignment marker lock state diagram shown in Figure 82–13. This process identifies the PCS lane number received on a particular lane of the service interface. After alignment marker lock is achieved on all lanes (4 or 20 lanes), then all inter-lane Skew is removed as shown in the PCS deskew state diagram in Figure 82–14. The Skew budget that the PCS receiver shall support is shown in Table 82–7.

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Note that Skew is defined in 80.5.

Table 82–7—Skew tolerance requirements

PCS	Maximum Skew	Maximum Skew Variation
40GBASE-R	180 ns (~1856 bits)	4ns (~41 bits)
100GBASE-R	180 ns (~928 bits)	4ns (~21 bits)
100GBASE-R with RS-FEC	49 ns (~253 bits)	0.4 ns (~2 bits)

If EEE is not supported then align_status is identical to rx_align_status. Otherwise the relationship between align_status and rx_align_status is given by Figure 82–19.

82.2.14 PCS lane reorder

Transmit PCS lanes can be received on different lanes of the service interface from which they were originally transmitted due to Skew between lanes and multiplexing by the PMA. The receive PCS shall order the received PCS lanes according to the PCS lane number.

82.2.15 Alignment marker removal

After all PCS lanes are aligned and deskewed, the PCS lanes are multiplexed together in the proper order to reconstruct the original stream of blocks and the alignment markers are deleted from the data stream. If necessary, the difference in rate due to deleted alignment markers is compensated for by inserting idle control characters. Note that an alignment marker is always deleted when a given PCS Lane is in am_lock=true even if it does not match the expected alignment marker value (due to a bit error for example). Repeated alignment marker errors will result in am_lock being set to false for a given PCS Lane, but until that happens it is sufficient to delete the block in the alignment marker position.

As part of the alignment marker removal process, the BIP_3 field is compared to the calculated BIP value for each PCS lane. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 3.200 through 3.219) is incremented by one each time the calculated BIP value does not equal the value received in the BIP_3 field. The incoming bit error ratio can be estimated by dividing the BIP block error ratio by a factor of 1081344.

82.2.16 Descrambler

The descrambler is identical to that used in Clause 49, see 49.2.10 for the definition.

82.2.17 Receive process

The receive process decodes blocks to produce RXD<63:0> and RXC<7:0> for transmission to the XLGMII/CGMII. One XLGMII/CGMII data transfer is decoded from each block. The receive process may insert idle control characters to compensate for the removal of alignment markers. If the PCS receive process spans multiple clock domains, it may also perform clock rate compensation via the deletion of idle control characters or sequence ordered sets or the insertion of idle control characters.

The receive process decodes blocks as specified in the receive state diagram shown in Figure 82–17.

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82.2.18 Test-pattern checker

When the receive channel is operating in scrambled idle test-pattern mode, the scrambled idle test-pattern checker checks the bits received via *inst*:IS_UNITDATA_*i*.indication primitives.

The scrambled idle test-pattern checker utilizes the block lock state diagram, the alignment marker state diagram, the PCS deskew state diagram, and the descrambler operating as they do during normal data reception. The BER monitor state diagram is disabled during receive test-pattern mode. When align_status is true and the scrambled idle receive test-pattern mode is active, the scrambled idle test-pattern checker observes the sync header and the output from the descrambler. When the sync header and the output of the descrambler is the all idle pattern, a match is detected. When operating in scrambled idle test pattern, the test-pattern error counter counts blocks with a mismatch. Any mismatch indicates an error and shall increment the test-pattern error counter. Because of the error multiplication characteristics of the descrambler, the incoming bit error ratio can be estimated by dividing the 66-bit block error ratio by a factor of 124.

If a Clause 45 MDIO is implemented, then control of the test-pattern reception is from the BASE-R PCS test-pattern control register (bit 3.42.2). In addition errors are counted in the BASE-R PCS test-pattern error counter register (3.43.15:0).

82.2.19 Detailed functions and state diagrams

82.2.19.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

82.2.19.2 State variables

82.2.19.2.1 Constants

EBLOCK_R<71:0>
: 72 bit vector to be sent to the XLGMII/CGMII containing /E/ in all the eight character locations.

EBLOCK_T<65:0>
: 66 bit vector to be sent to the PMA containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
: 72 bit vector to be sent to the XLGMII/CGMII containing one Local Fault ordered set. The Local Fault ordered set is defined in 81.3.4.

LBLOCK_T<65:0>
: 66 bit vector to be sent to the PMA containing one Local Fault ordered set.

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82.2.19.2.2 Variables

align_status
: A variable set by the PCS deskew process to reflect the status of the PCS lane-to-lane alignment. Set true when all lanes are synchronized and aligned, set false when the deskew process is not complete.

NOTE—If the EEE capability is supported, then this variable is affected by the LPI receive state diagram. If the EEE capability is not supported then this variable is identical to rx_align_status controlled according to Figure 82–13.

alignment_valid
: Boolean variable that is set true if all PCS lanes are aligned. It is valid when each lane is in am_lock, with each PCS lane locked to a unique alignment marker from Table 82–2 or Table 82–3, and when all PCS lanes are deskewed. Otherwise, alignment_valid is false.

am_lock<*x*>
: Boolean variable that is set true when receiver acquires alignment marker delineation for a given lane of the service interface, where $x = 0{:}3$ for 40GBASE-R and $x = 0{:}19$ for 100GBASE-R.

am_slip_done
: Boolean variable that is asserted true when the AM_SLIP requested by the alignment marker lock state diagram has been completed indicating that the next candidate 66-bit block position can be tested.

am_status
: A Boolean variable that is true when all lanes are in am_lock and false when at least one lane is not in am_lock.

am_counter_done
: Boolean variable that indicates that the alignment marker counter is done.

am_valid
: Boolean variable that is set true if received block rx_coded is a valid alignment marker. A valid alignment marker matches one of the encodings in Table 82–2, Table 82–3, Table 82–5, or Table 82–6, excluding the BIP_3 and BIP_7 fields.

ber_test_sh
: Boolean variable that is set true when a new sync header is available for testing and false when BER_TEST_SH state is entered. A new sync header is available for testing when the Block Sync process has accumulated enough bits from the PMA to evaluate the header of the next block.

block_lock<*x*>
: Boolean variable that is set true when receiver acquires block delineation for a given lane of the service interface, where $x = 0{:}3$ for 40GBASE-R and $x = 0{:}19$ for 100GBASE-R.

NOTE—If the EEE capability is supported, then this variable is affected by the LPI receive state diagram. If the EEE capability is not supported, then this variable is identical to rx_block_lock controlled according to Figure 82–12.

current_am
: This variable holds the lane number of the current alignment marker. This is compared to the variable first_am to determine if we have alignment marker lock and is always n × 16384 66-bit blocks away from the first_am.

enable_deskew
: A Boolean variable that indicates the enabling and disabling of the deskew process. Blocks may be discarded whenever deskew is enabled. True when deskew is enabled, false when deskew is disabled.

first_am
: A variable that holds the lane number of the first alignment marker that is recognized on a given lane. This is used later to compare to future alignment markers.

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hi_ber
: Boolean variable which is asserted true when the ber_cnt equals 97 indicating a bit error ratio $>10^{-4}$

lane_mapping<*x*>
: This variable indicates which PCS lane is received on lane *x* of the service interface when am_lock<*x*> = true, where *x* = 0:3 for 40GBASE-R and *x* = 0:19 for 100GBASE-R.

PCS_status
: A Boolean variable that is true when align_status is true and hi_ber is false.

r_block_type
: This variable contains the rx_coded<65:0> vector classification results, returned by the R_TYPE function. It can assume one of the following five values {C,S,T,D,E}, as defined by the R_TYPE function.

r_block_type_next
: This variable contains the rx_coded<65:0> vector classification results, returned by the R_TYPE_NEXT function. It can assume one of the following five values {C,S,T,D,E}, as defined by the R_TYPE_NEXT function.

r_test_mode
: Boolean variable that is asserted true when the receiver is in test-pattern mode.

reset
: Boolean variable that controls the resetting of the PCS. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rx_align_status
: Variable used by the PCS lane deskew process to reflect the status of the PCS lane-to-lane alignment. This variable is set true when all lanes are synchronized and aligned, set false when the deskew process is not complete.

rx_block_lock<x>
: Variable used in Figure 82–12 to reflect the status of the code-group delineation for each lane. This variable is set true when the receiver acquires block delineation.

rx_coded<65:0>
: Vector containing the input to the 64B/66B decoder. The format for this vector is shown in Figure 82–5. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<65>.

rx_down_count
: The value that results from the bit-wise exclusive-OR of the Count Down (CD3) byte and the M0 byte of the current received Rapid Alignment Marker (see 82.2.9).

rx_raw<71:0>
: Vector containing one XLGMII/CGMII transfer. RXC<0> through RXC<7> are from rx_raw<0> through rx_raw<7>, respectively. RXD<0> through RXD<63> are from rx_raw<8> through rx_raw<71>, respectively.

sh_valid
: Boolean variable that is set true if received block rx_coded has valid sync header bits. That is, sh_valid is asserted if rx_coded<0> ≠ rx_coded<1> and deasserted otherwise.

signal_ok
: Boolean variable that is set based on the most recently received value of *inst*:IS_SIGNAL.indication(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done
: Boolean variable that is asserted true when the SLIP requested by the Block Lock state diagram has been completed indicating that the next candidate block sync position can be tested.

t_block_type
: This variable contains the tx_raw<71:0> vector classification results, returned by the T_TYPE function. It can assume one of the following five values {C,S,T,D,E}, as defined by the T_TYPE function.

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test_am
: Boolean variable that is set true when a new block is available for testing and false when FIND_1ST state is entered. A new block is available for testing when the Block Sync process has accumulated enough bits from the PMA to evaluate the next block

test_sh
: Boolean variable that is set true when a new sync header is available for testing and false when TEST_SH and TEST_SH2 state are entered. A new sync header is available for testing when the Block Sync process has accumulated enough bits from the PMA to evaluate the header of the next block

tx_coded<65:0>
: Vector containing the output from the 64B/66B encoder. The format for this vector is shown in Figure 82–5. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<65>.

tx_raw<71:0>
: Vector containing one XLGMII/CGMII transfer. TXC<0> through TXC<7> are placed in tx_raw<0> through tx_raw<7>, respectively. TXD<0> through TXD<63> are placed in tx_raw<8> through tx_raw<71>, respectively.

The following variables are used only for the EEE capability.

down_count_done
: Boolean variable that indicates that the down_count counter has reached zero.

down_count_enable
: Boolean variable controlling decrement of the counter down_count. This variable is set by the LPI transmit state diagram.

energy_detect
: A parameter generated by the PMA/PMD sublayer to reflect the state of the received signal. In the PMD this has the same definition as parameter signal_detect and is passed through without modification by the PMA (and FEC).

first_rx_lpi_active
: Boolean variable first_rx_lpi_active is set true when the receiver is in state RX_ACTIVE in the LPI receive state diagram (see Figure 82–19) and R_TYPE(rx_coded) = LI and LPI_FW = FALSE and is otherwise false.

LPI_FW
: Boolean variable controlling the wake mode for the LPI transmit and receive functions. This variable is set true when the link is to use the fast wake mechanism, and false when the link is to use the optional deep sleep mechanism for each direction. This variable defaults true and may only be set to false if the optional deep sleep mode is supported.

rx_lpi_active
: A Boolean variable that is set to true when the receiver is in a low power state and set to false when it is in an active state and capable of receiving data.

Rx LPI indication:
: A Boolean variable indicating the current state of the receive LPI function. This flag is set to true (register bit set to one) when the LPI receive state diagram is in any state other than RX_ACTIVE. This status is reflected in MDIO register 3.1.8. A latch high view of this status is reflected in MDIO register 3.1.10 (Rx LPI received).

rx_mode
: A variable reflecting state of the LPI receive function as defined in Figure 82–19.The parameter has one of two values: DATA and QUIET.

scrambler_bypass
: This Boolean variable indicates whether the Tx PCS scrambler is to be bypassed in order to assist rapid synchronization following low power idle. When set to TRUE, the PCS passes the unscrambled data from the scrambler input rather than the scrambled data from the scrambler output. The scrambler continues to operate normally, shifting input data into the delay line. When scrambler_bypass is set to FALSE the PCS passes scrambled data from the scrambler output.

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scr_bypass_enable

A Boolean variable used to indicate to the transmit LPI state diagram that the scrambler bypass option is required. The PHY shall set scr_bypass_enable = TRUE if Clause 74 FEC is in use. The PHY shall set scr_bypass_enable = FALSE if this FEC is not in use.

tx_mode

A variable reflecting state of the LPI transmit function as defined in Figure 82–18. When tx_mode is set to QUIET the sublayer may go into a low power state.

82.2.19.2.3 Functions

AM_SLIP

Causes the next candidate block position to be tested. The precise method for determining the next candidate block position is not specified and is implementation dependent. However, an implementation shall ensure that all possible blocks are evaluated.

DECODE(rx_coded<65:0>)

Decodes the 66-bit vector returning rx_raw<71:0>, which is sent to the XLGMII/CGMII. The DECODE function shall decode the block as specified in 82.2.3.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector returning tx_coded<65:0> of which tx_coded<65:2> is sent to the scrambler. The two bits of the sync header bypass the scrambler. The ENCODE function shall encode the block as specified in 82.2.3.

R_TYPE(rx_coded<65:0>)

This function classifies the current rx_coded<65:0> vector as belonging to one of the following types, depending on its contents. The classification results are returned via the r_block_type variable.

Values: C; The vector contains a sync header of 10 and one of the following:

a) A block type field of 0x1E and eight valid control characters other than /E/ or /LI/;

b) A block type field of 0x4B.

LI; For EEE capability, the LI type is supported where the vector contains a sync header of 10, a block type field of 0x1E and eight control characters of 0x06 (/LI/).

S; The vector contains a sync header of 10 and the following:

a) A block type field of 0x78.

T; The vector contains a sync header of 10, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.

D; The vector contains a sync header of 01.

E; The vector does not meet the criteria for any other value.

Valid control characters are specified in Table 82–1.

NOTE—A PCS that does not support EEE classifies vectors containing one or more /LI/ control characters as type E.

R_TYPE_NEXT

This function classifies the 66-bit rx_coded vector that immediately follows the current rx_coded<65:0> vector as belonging to one of the five types defined in R_TYPE, depending on its contents. It is intended to perform a prescient end of packet check. The classification results are returned via the r_block_type_next variable.

SLIP

Causes the next candidate block sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

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T_TYPE = (tx_raw<71:0>)

This function classifies each 72-bit tx_raw vector as belonging to one of the following types depending on its contents. The classification results are returned via the t_block_type variable.

Values: C; The vector contains one of the following:
a) Eight valid control characters other than /O/, /S/, /T/, /LI/, and /E/;
b) One valid ordered set.
LI; For EEE capability, this vector contains eight /LI/ characters.
S; The vector contains an /S/ in its first character, and all characters following the /S/ are data characters.
T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.
D; The vector contains eight data characters.
E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XLGMII/CGMII control code specified in Table 82–1. A valid ordered set consists of a valid /O/ character in the first character and data characters in the seven characters following the /O/. A valid /O/ is any character with a value for O code in Table 82–1.

NOTE—A PCS that does not support EEE classifies vectors containing one or more /LI/ control characters as type E.

82.2.19.2.4 Counters

am_counter

This counter counts 66-bit blocks that separate two consecutive alignment markers. If the optional EEE deep sleep capability is supported, when rx_lpi_active is TRUE and LPI_FW is FALSE, the terminal count is 7 for 100GBASE-R PCS and 15 for 40GBASE-R PCS. If the optional EEE deep sleep capability is not supported, or rx_lpi_active is FALSE, the terminal count is 16383.

am_invld_cnt

Count of the number of invalid alignment markers seen in a row. This counter is always reset to all zeros when a valid marker is detected.

ber_count

A 22-bit counter that counts each time BER_BAD_SH state is entered. This counter is reflected in MDIO register bits 3.33.13:8 and 3.44.15:0.

ber_cnt

Count up to a maximum of 97 of the number of invalid sync headers within the current 1.25 ms (40GBASE-R) or 500 μs (100GBASE-R) period.

errored_block_count:

When the receiver is in normal mode, this 22-bit counter counts once for each time RX_E state is entered. This counter is reflected in MDIO register bits 3.33.7:0 and 3.45.13:0.

sh_cnt

Count of the number of sync headers checked within the current 64 or 1024 block window.

sh_invld_cnt

Count of the number of invalid sync headers within the current 64 or 1024 block window.

test_pattern_error_count:

When the receiver is in test-pattern mode, this 16-bit counter counts errors as described in 82.2.18. This counter is reflected in MDIO register bits 3.43.15:0.

The following counters are used only for the EEE capability:

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down_count
: A counter that is used in rapid alignment markers and is decremented each time a RAM is sent while variable down_count_enable = true. The counter initial value is set by the LPI transmit state diagram. When the down_count counter reaches zero, it sets the variable down_count_done = true.

wake_error_counter
: A counter that is incremented each time that the LPI receive state diagram enters the RX_WTF state indicating that a wake time fault has been detected. The counter is reflected in register 3.22 (see 45.2.3.12).

82.2.19.2.5 Timers

State diagram timers follow the conventions of 14.2.3.2.

*x*us_timer
: Timer that is triggered every 1.25 ms +1%, –25% for 40GBASE-R or 500 µs +1%, –25% for 100GBASE-R.

The following timers are used only for the EEE capability.

one_us_timer
: A timer used to count approximately 1 µs intervals. The timer terminal count is set to T_{1U}. When the timer reaches terminal count, it sets one_us_timer_done = true.

rx_tq_timer
: This timer is started when the PCS receiver enters the RX_SLEEP state. The timer terminal count is set to T_{QR}. When the timer reaches terminal count, it sets rx_tq_timer_done = true.

rx_tw_timer
: This timer is started when the PCS receiver enters the RX_WAKE state. The timer terminal count is set to a value no larger than the maximum value given for T_{WR} in Table 82–9. When the timer reaches terminal count, it sets rx_tw_timer_done = true.

rx_wf_timer
: This timer is started when the PCS receiver enters the RX_WTF state, indicating that the receiver has encountered a wake time fault. The rx_wf_timer allows the receiver an additional period in which to synchronize or return to the QUIET state before a link failure is indicated. The timer terminal count is set to T_{WTF}. When the timer reaches terminal count, it sets the rx_wf_timer_done = true.

scr_byp_timer
: This timer is started when the PCS transmitter enters the TX_SCR_BYPASS state. The timer terminal count is set to T_{BYP}. When the timer reaches terminal count, it sets the scr_byp_timer_done = true.

tx_ts_timer
: This timer is started when the PCS transmitter enters the TX_SLEEP state. The timer terminal count is set to T_{SL}. When the timer reaches terminal count, it sets the tx_ts_timer_done = true.

tx_tq_timer
: This timer is started when the PCS transmitter enters the TX_QUIET state. The timer terminal count is set to T_{QL}. When the timer reaches terminal count, it sets the tx_tq_timer_done = true.

tx_tw_timer
: This timer is started when the PCS transmitter enters the TX_WAKE state. The timer terminal count is set to T_{WL}. When the timer reaches terminal count, it sets the tx_tw_timer_done = true.

tx_tw2_timer
: This timer is started when the PCS transmitter enters the TX_WAKE2 state. The timer terminal count is set to T_{WL2}. When the timer reaches terminal count, it sets the tx_tw2_timer_done = true.

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82.2.19.3 State diagrams

The 40GBASE-R PCS shall implement four block lock processes as depicted in Figure 82–12. The 100GBASE-R PCS shall implement twenty block lock processes as depicted in Figure 82–12. A block lock process operates independently on each lane. Each block lock process looks for 64 valid sync headers in a row to declare lock. A valid sync header is either a 01 or a 10. Once in lock, the lock process looks for 65 invalid sync headers within a 1024 sync window to declare out of lock. An invalid sync header is a 11 or 00. Once block lock is achieved on a lane, then the alignment marker process starts.

The 40GBASE-R PCS shall implement four alignment marker lock processes as depicted in Figure 82–13. The 100GBASE-R PCS shall implement twenty alignment marker lock processes as depicted in Figure 82–13. An alignment marker lock process operates independently on each lane. The alignment marker lock state diagram shown in Figure 82–13 determines when the PCS has obtained alignment marker lock to the received bit stream for a given lane of the service interface. Each alignment marker lock process looks for two valid alignment markers 16384 66-bit blocks apart to gain alignment marker lock. On a given lane of the service interface, lane markers have to match each other and an entry from Table 82–2 for 100GBASE-R or Table 82–3 for 40GBASE-R. Note that the BIP_3 and BIP_7 fields are excluded from the markers when making a match to each other or the tables. Once in lock, a lane will go out of alignment marker lock if four markers are received in a row that do not match the alignment marker that the lane is currently locked to. When the alignment marker lock process achieves lock for a lane, and if a Clause 45 MDIO is implemented, the PCS shall record the number of the PCS lane received on that lane of the service interface in the appropriate lane mapping register (3.400 to 3.419).

The PCS shall run the deskew process as depicted in Figure 82–14. The PCS deskew process is responsible for determining if the PCS is capable of presenting coherent data to the XLGMII/CGMII. The deskew process ensures that all PCS lanes have alignment marker lock, are locked to different alignment markers, and that the Skew is within the boundaries of what the PCS can deskew.

The BER Monitor state diagram shown in Figure 82–15 monitors the received aggregate signal for high bit error ratio. The high BER state shall be entered if 97 invalid 66-bit sync headers are detected within a 500 μs window for 100GBASE-R, or a 1.25 ms window for 40GBASE-R. The high BER state is exited once there are less than 97 invalid sync headers in the same window.

The Transmit state diagram shown in Figure 82–16 controls the encoding of transmitted blocks. It makes exactly one transition for each transmit block processed. Though the Transmit state diagram sends Local Fault ordered sets when reset is asserted, the scrambler may not be operational during reset. Thus, the Local Fault ordered sets may not appear on the PMA/FEC service interface.

The Receive state diagram shown in Figure 82–17 controls the decoding of received blocks. It makes exactly one transition for each receive block processed.

The PCS shall perform the functions of block lock, alignment marker lock, PCS deskew, BER Monitor, Transmit, and Receive as specified in the respective state diagrams.

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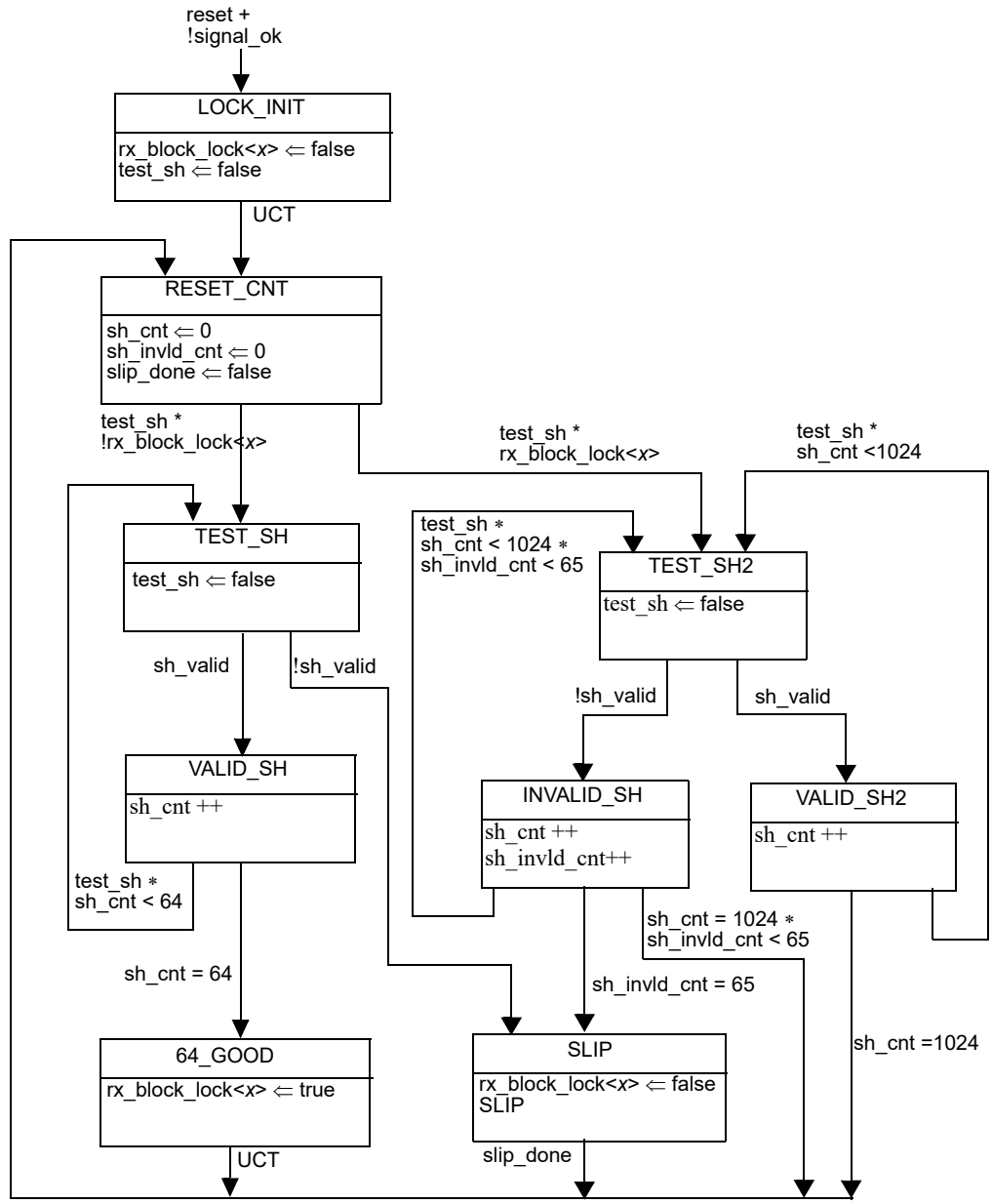

NOTE— rx_block_lock<*x*> refers to the received lane *x* of the service interface, where *x* = 0:3 (for 40GBASE-R) or 0:19 (for 100GBASE-R)

Figure 82–12—Block lock state diagram

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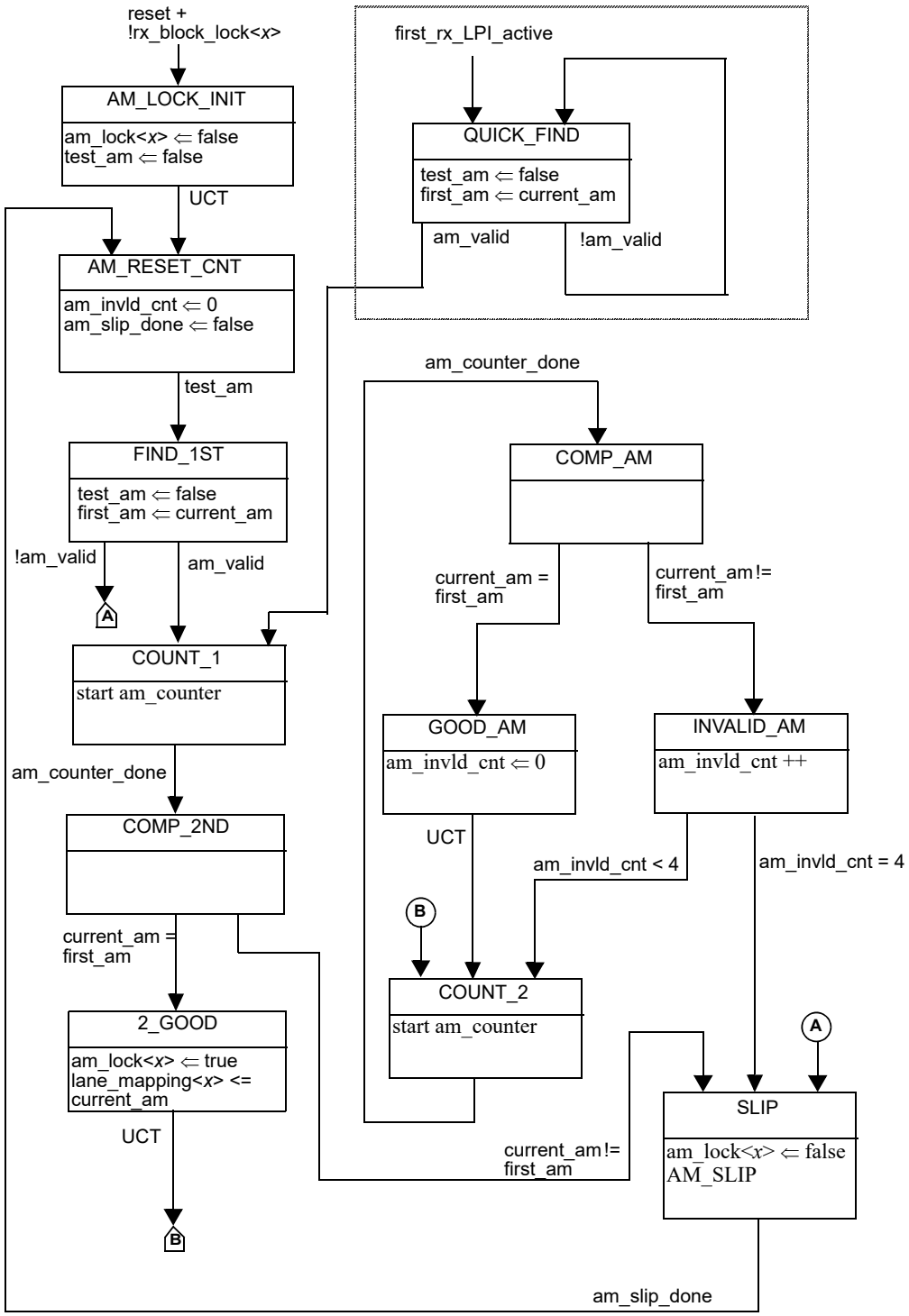

NOTE 1— am_lock<*x*> refers to the received lane *x* of the service interface, where *x* = 0:3 (for 40GBASE-R) or 0:19 (for 100GBASE-R)

NOTE 2—Optional state (inside the dotted box) is only required to support EEE capability.

Figure 82–13—Alignment marker lock state diagram

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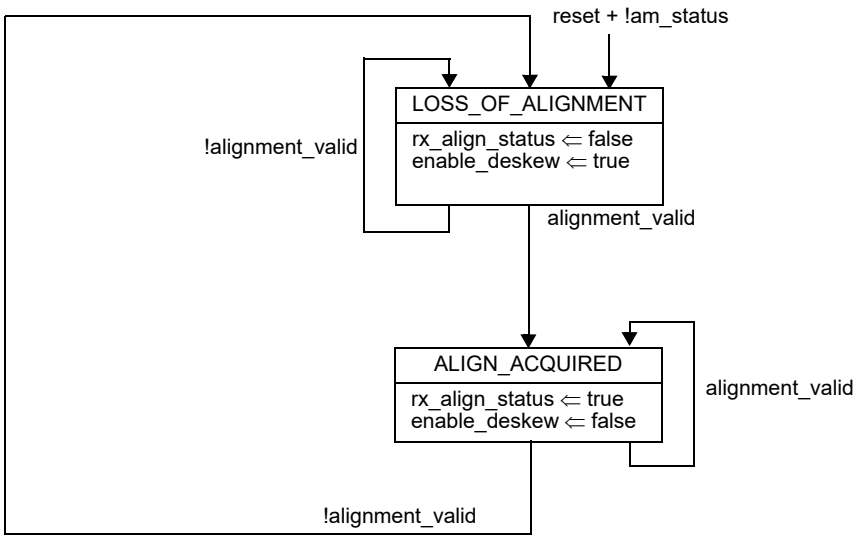

Figure 82–14—PCS deskew state diagram

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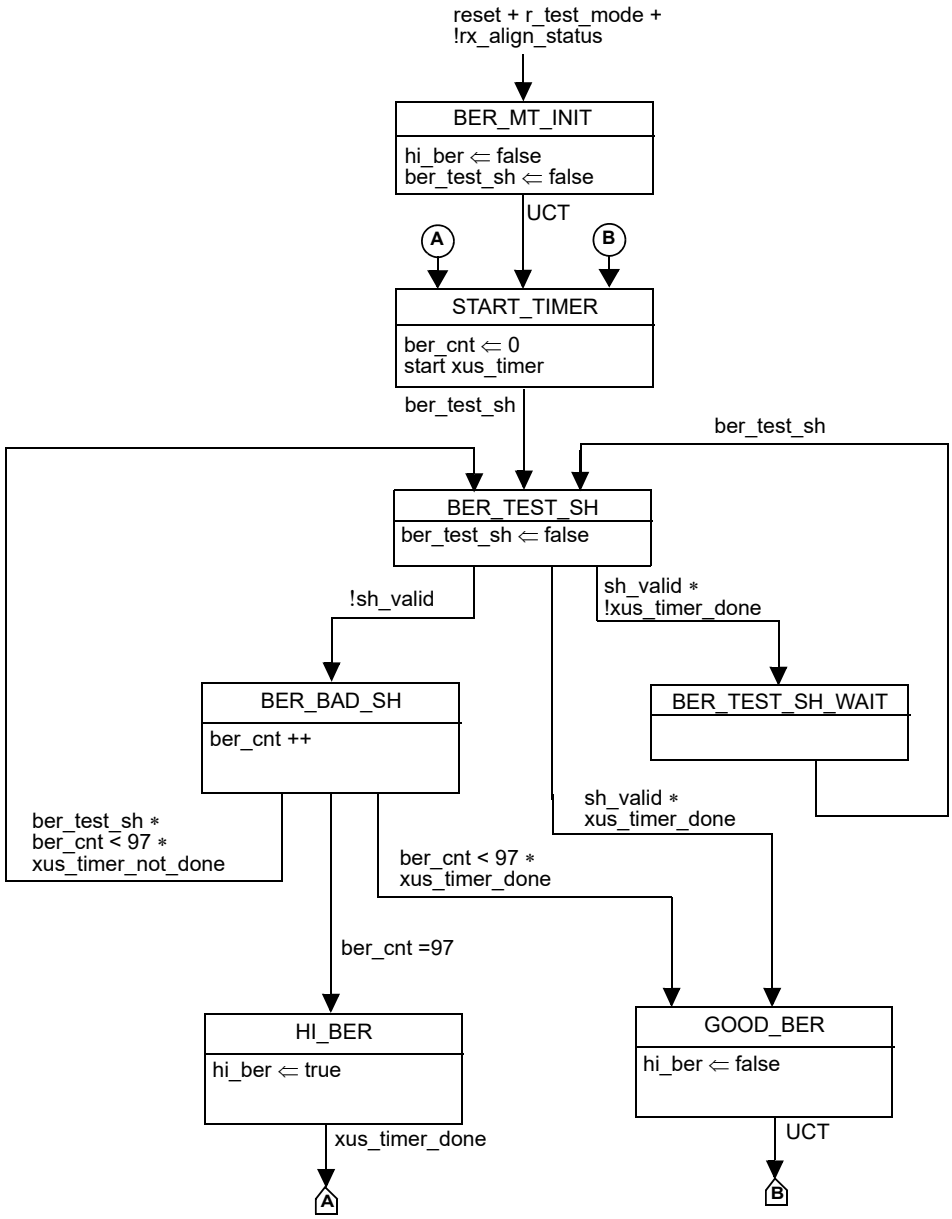

Figure 82–15—BER monitor state diagram

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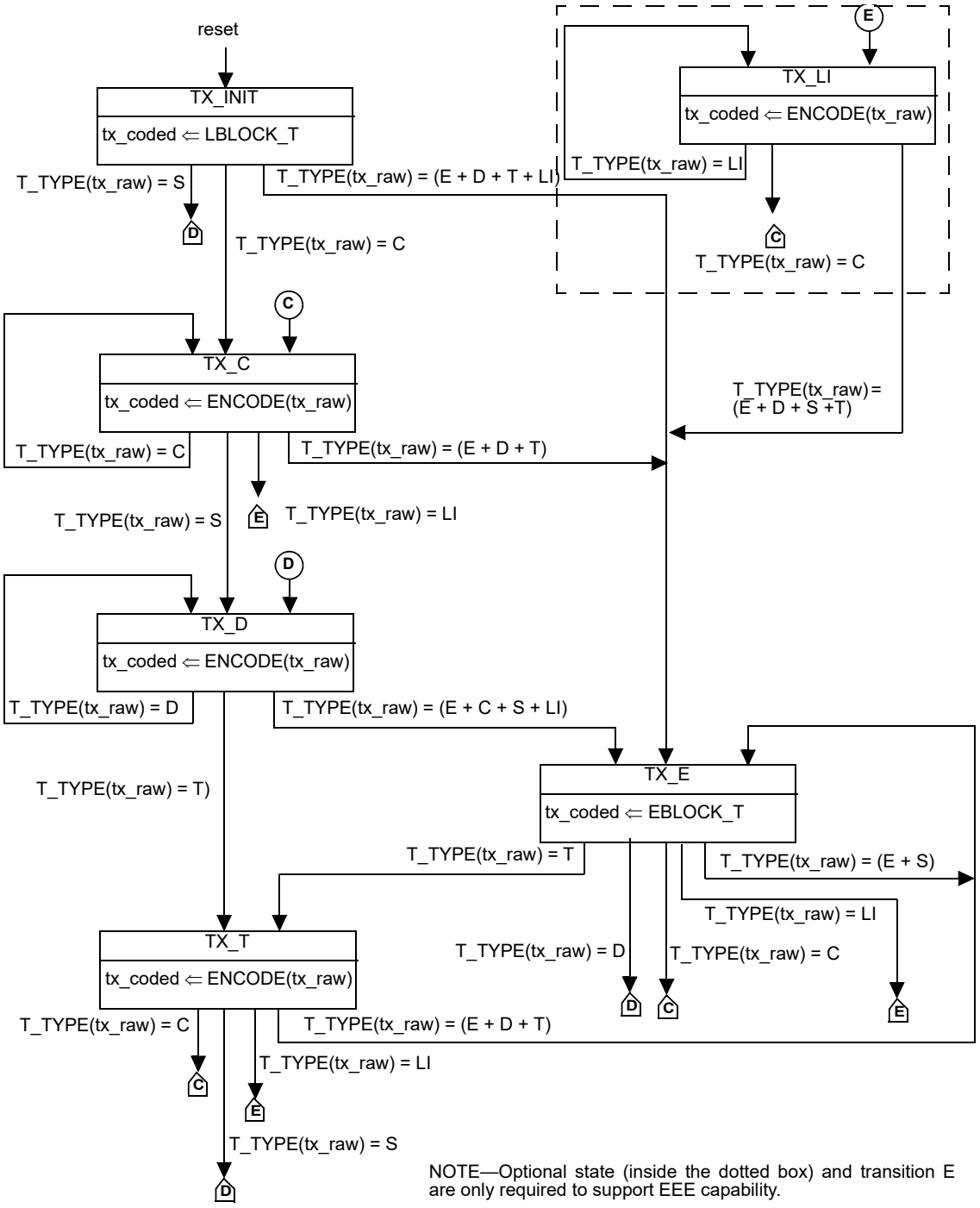

Figure 82–16—Transmit state diagram

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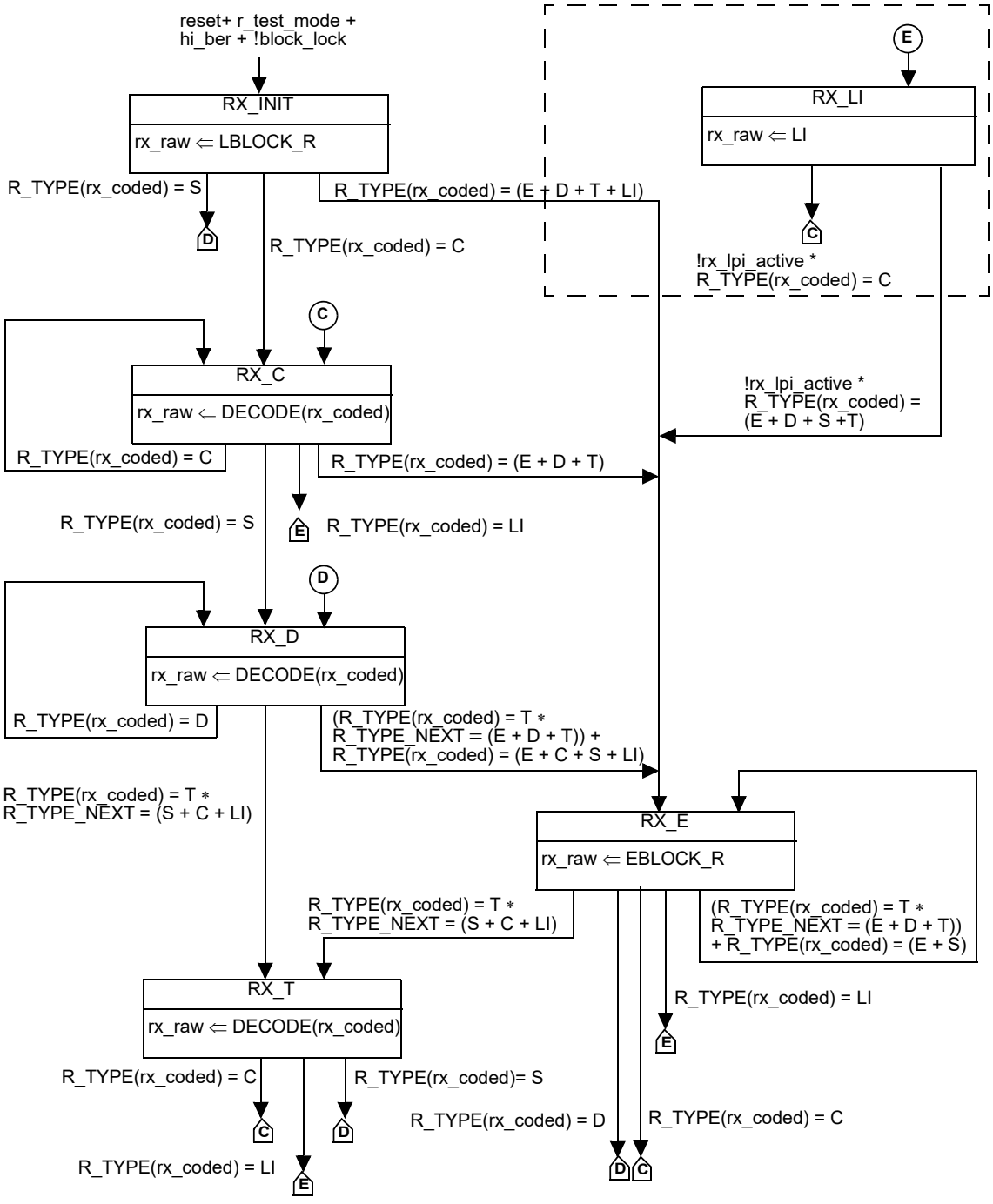

Figure 82–17—Receive state diagram

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82.2.19.3.1 LPI state diagrams

A PCS that supports the EEE capability shall implement the LPI transmit and receive processes as shown in Figure 82–18 and Figure 82–19. The transmit LPI state diagram controls tx_mode, which disables the transmitter when it is set to QUIET. The receive LPI state diagram controls block_lock during LPI and signals the end of LPI to the receive state diagram.

Following a period of LPI, the receiver is required to achieve block synchronization within the wake-up time specified (see Figure 82–19). The implementation of the block synchronization state diagram should use techniques to ensure that block lock is achieved with minimal numbers of slip attempts. If fast wake is selected then the receiver is expected to maintain sufficient state to allow much faster wake up.

The LPI functions shall use timer values for these state diagrams as shown in Table 82–8 for transmit and Table 82–9 for receive.

Table 82–8—Transmitter LPI timing parameters

Parameter	Description	Min	Max	Units
T_{SL}	Local Sleep Time from entering the TX_SLEEP state to when tx_mode is set to QUIET.	0.9	1.1	μs
T_{QL}	Local Quiet Time from when tx_mode is set to QUIET to entry into the TX_WAKE state.	1.7	1.8	ms
T_{WL}	Time spent in the TX_WAKE state.	1.5	1.6	μs
T_{WL2}	Time spent in the TX_WAKE2 state.	2.4	2.5	μs
T_{BYP}	Time spent in the TX_SCR_BYPASS state, 40 Gb/s operation.	0.9	1.1	μs
T_{BYP}	Time spent in the TX_SCR_BYPASS state, 100 Gb/s operation.	1.9	2.1	μs
T_{1U}	Time spent in the TX_ALERT state.	1.15	1.3	μs

Table 82–9—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	Time the receiver waits for energy_detect to be set to true while in the RX_QUIET state before asserting receive fault.	2	3	ms
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault, scr_bypass_enable = FALSE.	—	4.5	μs
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault, scr_bypass_enable = TRUE, 40 Gb/s.	—	5.5	μs
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault, scr_bypass_enable = TRUE, 100 Gb/s.	—	6.5	μs
T_{WTF}	Wake time fault recovery time.	—	10	ms

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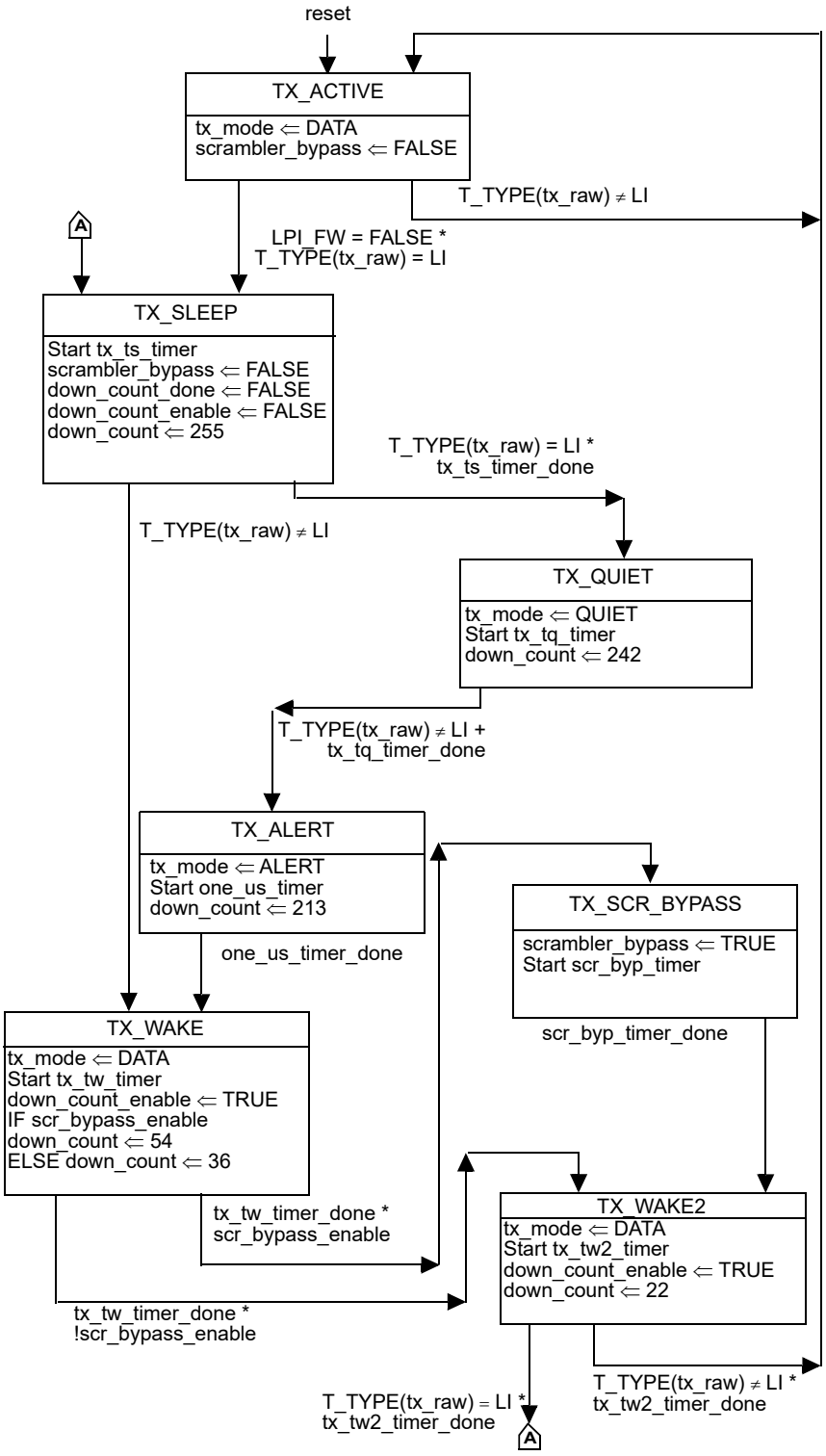

Figure 82–18—LPI Transmit state diagram

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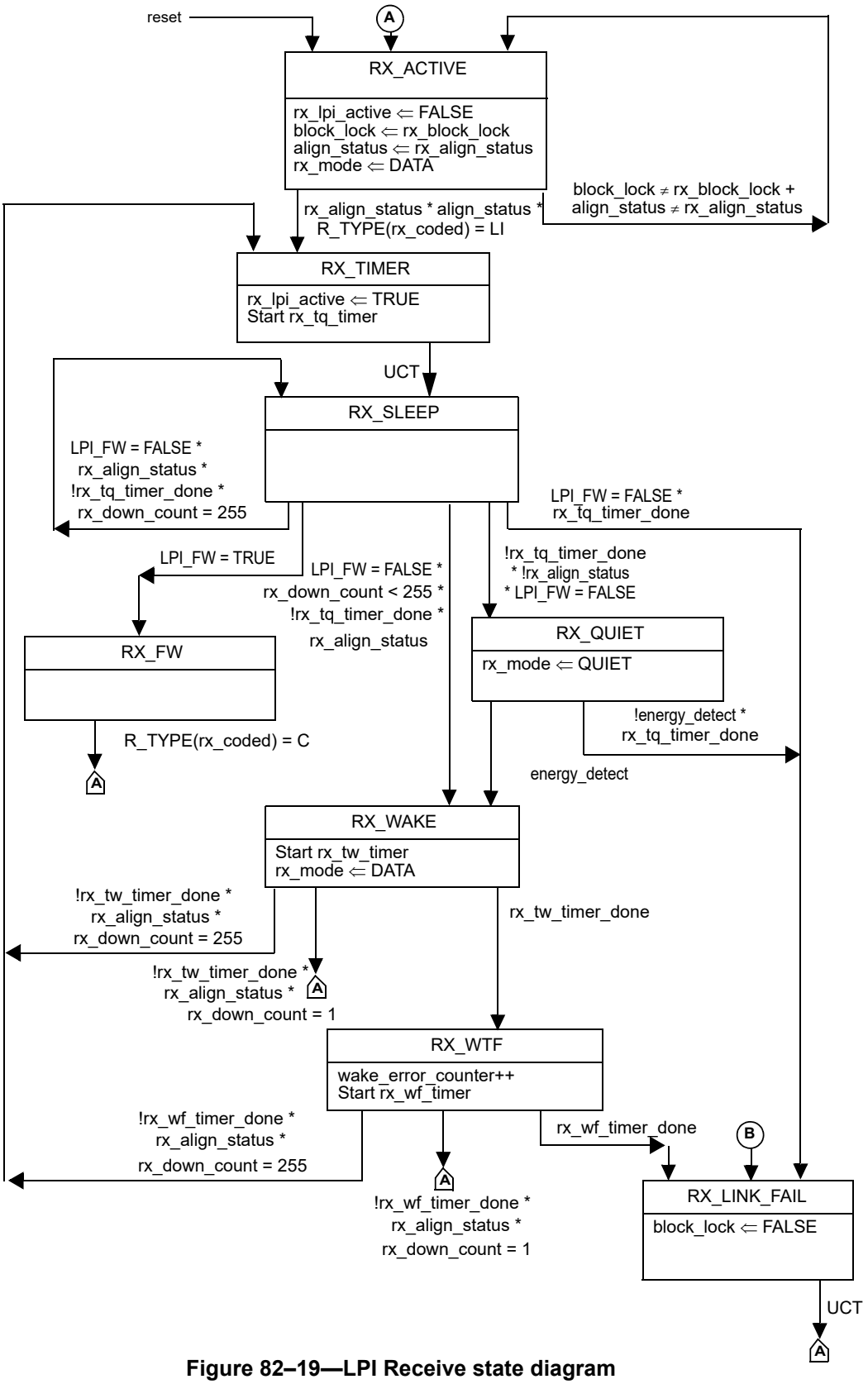

Figure 82–19—LPI Receive state diagram

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82.3 PCS Management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

82.3.1 PCS MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PCS. Mapping of MDIO control variables to PCS control variables is shown in Table 82–10. Mapping of MDIO status variables to PCS status variables is shown in Table 82–11.

Table 82–10—MDIO/PCS control variable mapping

MDIO control variable	PCS register name	Register/ bit number	PCS control variable
Reset	PCS control 1 register	3.0.15	reset
Loopback	PCS control 1 register	3.0.14	Loopback
Transmit test-pattern enable	BASE-R PCS test-pattern control register	3.42.3	tx_test_mode
Receive test-pattern enable	BASE-R PCS test-pattern control register	3.42.2	rx_test_mode
LPI_FW	LPI fast wake enable	3.20.0	LPI_FW

Table 82–11—MDIO/PCS status variable mapping

MDIO status variable	PCS register name	Register/ bit number	PCS status variable
BASE-R and 10GBASE-T receive link status	BASE-R and 10GBASE-T PCS status 1 register	3.32.12	PCS_status
BASE-R and 10GBASE-T PCS high BER	BASE-R and 10GBASE-T PCS status 1 register	3.32.1	hi_ber
Block lock *x*	Multi-lane BASE-R PCS alignment status 1 and 2 registers	3.50.7:0 3.51.11:0	block_lock<*x*>
Lane *x* aligned	Multi-lane BASE-R PCS alignment status 3 and 4 registers	3.52.7:0 3.53.11:0	am_lock<*x*>
PCS lane alignment status	Multi-lane BASE-R PCS alignment status 1 register	3.50.12	align_status
BER	BASE-R and 10GBASE-T PCS status 2 register BER high order counter register	3.33.13:8 3.44.15:0	ber_count
Errored blocks	BASE-R and 10GBASE-T PCS status 2 register Errored blocks high order counter register	3.33.7:0 3.45.13:0	errored_block_count

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Table 82–11—MDIO/PCS status variable mapping *(continued)*

MDIO status variable	PCS register name	Register/ bit number	PCS status variable
Test-pattern error counter	BASE-R PCS test-pattern error counter register	3.43.15:0	test_pattern_error_count
BIP error counter, lane *x*	BIP error counter, lane *x* register	3.200 through 3.219	bip_counter
Lane *x* mapping	Lane *x* mapping register	3.400 through 3.419	lane_mapping
Tx LPI indication	Tx LPI indication	3.1.9	Tx LPI indication
Tx LPI received	Tx LPI received	3.1.11	Tx LPI received
Rx LPI indication	Rx LPI indication	3.1.8	Rx LPI indication
Rx LPI received	Rx LPI received	3.1.10	Rx LPI received
Wake_error_counter	Wake_error_counter	3.22	Wake_error_counter

82.4 Loopback

If a Clause 45 MDIO is implemented, then the PCS shall be placed in the loopback mode when the loopback bit from the PCS control 1 register (bit 3.0.14) is set to a one. In this mode, the PCS shall accept data on the transmit path from the XLGMII/CGMII and return it on the receive path to the XLGMII/CGMII. In addition, the PCS shall transmit what it receives from the XLGMII/CGMII to the PMA/FEC sublayer, and shall ignore all data presented to it by the PMA/FEC sublayer.

82.5 Delay constraints

The maximum delay contributed by the 40GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 11264 BT (22 pause_quanta or 281.6 ns). The maximum delay contributed by the 100GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 35328 BT (69 pause_quanta or 353.28 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

82.6 Auto-Negotiation

The following requirements apply to a PCS used with a 40GBASE-KR4 PMD, 40GBASE-CR4 PMD, 100GBASE-CR10, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-KR4, 100GBASE-KP4, or 100GBASE-KR2 PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

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82.7 Protocol implementation conformance statement (PICS) proforma for Clause 82, Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R[147]

82.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 82, Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

82.7.2 Identification

82.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

82.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 82, Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[147] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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82.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PCS40	PCS for 40GBASE-R	82.1.1		O	Yes [ ] No [ ]
*PCS100	PCS for 100GBASE-R	82.1.1		O	Yes [ ] No [ ]
XGE40	XLGMII logical interface	81, 82.1.4	Logical interface is supported	O	Yes [ ] No [ ]
XGE100	CGMII logical interface	81, 82.1.4	Logical interface is supported	O	Yes [ ] No [ ]
*MD	MDIO	45, 82.3	Registers and interface supported	O	Yes [ ] No [ ]
PMA	Supports operation directly connected to a PMA	82.1.4.2		O.1	Yes [ ] No [ ]
FEC	Supports operation directly connected to an FEC sublayer	82.1.4.2		O.1	Yes [ ] No [ ]
*JTM	Supports test-pattern mode	82.2.1		PMA:M	Yes [ ] No [ ] N/A[ ]
*LPI	Implementation of LPI	82.2.3.4		O	Yes [ ] No [ ]

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82.7.4 PICS proforma tables for PCS, type 40GBASE-R and 100GBASE-R

82.7.4.1 Coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder (and ENCODE function) implements the code as specified	82.2.3 and 82.2.19.2.3		M	Yes [ ]
C2	Decoder (and DECODE function) implements the code as specified	82.2.3 and 82.2.19.2.3		M	Yes [ ]
C3	Only valid block types are transmitted	82.2.3.3		M	Yes [ ]
C4	Invalid block types are treated as an error	82.2.3.3		M	Yes [ ]
C5	Only valid control characters are transmitted	82.2.3.4		M	Yes [ ]
C6	Invalid control characters are treated as an error	82.2.3.4		M	Yes [ ]
C7	Idles do not interrupt data	82.2.3.6		M	Yes [ ]
C8	IDLE control code insertion and deletion	82.2.3.6	Insertion or Deletion in groups of 8 /I/s	M	Yes [ ]
C9	Sequence ordered set deletion	82.2.3.9	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ]

82.7.4.2 Scrambler and Descrambler

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Scrambler	82.2.5	Performs as shown in Figure 49–8	M	Yes [ ]
S2	Descrambler	82.2.16	Performs as shown in Figure 49–10	M	Yes [ ]

82.7.4.3 Deskew and Reordering

Item	Feature	Subclause	Value/Comment	Status	Support
DR1	Deskew	82.2.13	Able to deskew up to the value in Table 82–7	M	Yes [ ]
DR2	Reordering	82.2.14	Performs reordering	M	Yes [ ]

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82.7.4.4 Alignment Markers

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	Alignment marker insertion	82.2.7	Alignment markers are inserted periodically as described in 82.2.7	M	Yes [ ]
AM2	Alignment marker form	82.2.7	Alignment markers are formed as described in 82.2.7	M	Yes [ ]
AM3	Alignment marker removal	82.2.15	Alignment markers are removed as described in 82.2.15	M	Yes [ ]
AM4	Lane mapping	82.2.19.3	PCS lane number is captured	MD:M	Yes [ ] N/A [ ]

82.7.4.5 Test-pattern modes

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Scrambled idle transmit test-pattern generator is implemented	82.2.11	Performs as in 82.2.11	JTM:M	Yes [ ] N/A[ ]
JT2	Scrambled idle receive test-pattern checker is implemented	82.2.18	Performs as in 82.2.18	JTM:M	Yes [ ] N/A[ ]
JT3	Transmit and receive test-pattern modes can operate simultaneously	82.2.1		JTM:M	Yes [ ] N/A[ ]

82.7.4.6 Bit order

Item	Feature	Subclause	Value/Comment	Status	Support
B1	Transmit bit order	82.2.3.2	Placement of bits into the PCS lanes as shown in Figure 82–3	M	Yes [ ]
B2	Receive bit order	82.2.3.2	Placement of bits into the XLGMII/CGMII as shown in Figure 82–4	M	Yes [ ]

82.7.4.7 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Equivalent access to PCS Management objects is provided	82.3		!MD:O	Yes [ ] No [ ] N/A [ ]

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82.7.4.8 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	40GBASE-R Block Lock	82.2.19.3	Implements 4 block lock processes as depicted in Figure 82–12	PCS40:M	Yes [ ] N/A [ ]
SM2	100GBASE-R Block Lock	82.2.19.3	Implements 20 block lock processes as depicted in Figure 82–12	PCS100:M	Yes [ ] N/A [ ]
SM3	The SLIP function evaluates all possible bit positions	82.2.19.2.3		M	Yes [ ]
SM4	40GBASE-R Alignment Marker Lock	82.2.19.3	Implements 4 alignment marker lock processes as depicted in Figure 82–13	PCS40:M	Yes [ ] N/A [ ]
SM5	100GBASE-R Alignment Marker Lock	82.2.19.3	Implements 20 alignment marker lock processes as depicted in Figure 82–13	PCS100:M	Yes [ ] N/A [ ]
SM6	The AM_SLIP functions evaluates all possible blocks	82.2.19.2.3		M	Yes [ ]
SM7	40GBASE-R PCS deskew state diagram	82.2.19.3	Meets the requirements of Figure 82–14	PCS40:M	Yes [ ] N/A [ ]
SM8	100GBASE-R PCS deskew state diagram	82.2.19.3	Meets the requirements of Figure 82–14	PCS100:M	Yes [ ] N/A [ ]
SM9	40GBASE-R BER Monitor	82.2.19.3	Meets the requirements of Figure 82–15 with xus_timer_done set to 1.25 ms	PCS40:M	Yes [ ] N/A [ ]
SM10	100GBASE-R BER Monitor	82.2.19.3	Meets the requirements of Figure 82–15 with xus_timer_done set to 500 μs	PCS100:M	Yes [ ] N/A [ ]
SM11	40GBASE-R Transmit process	82.2.19.3	Meets the requirements of Figure 82–16	PCS40:M	Yes [ ] N/A [ ]
SM12	100GBASE-R Transmit process	82.2.19.3	Meets the requirements of Figure 82–16	PCS100:M	Yes [ ] N/A [ ]
SM13	40GBASE-R and 100GBASE-R Receive process	82.2.19.3	Meets the requirements of Figure 82–17	PCS40:M	Yes [ ] N/A [ ]
SM14	100GBASE-R Receive process	82.2.19.3	Meets the requirements of Figure 82–17	PCS100:M	Yes [ ] N/A [ ]

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82.7.4.9 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports loopback	82.4	Performs as in 82.4	M	Yes [ ]
L2	When in loopback, transmits what it receives from the XLGMII/CGMII	82.4	Performs as in 82.4	M	Yes [ ]

82.7.4.10 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS Delay Constraint	82.5	No more than 11264 BT for sum of transmit and receive path delays for 40GBASE-R and 35328 BT for 100GBASE-R	M	Yes [ ]

82.7.4.11 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
*AN1	Support for use with a 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-KR4, 100GBASE-KP4, or 100GBASE-KR2 PMD	82.6	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN2	AN_LINK.indication primitive	82.6	Support of the primitive AN_LINK.indication(link_status)	AN1:M	Yes [ ] N/A [ ]
AN3	link_status parameter	82.6	Takes the value OK or FAIL, as described in 82.6	AN1:M	Yes [ ] N/A [ ]
AN4	Generation of AN_LINK.indication primitive	82.6	Generated when the value of link_status changes	AN1:M	Yes [ ] N/A [ ]

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82.7.4.12 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
LP-01	Support for both wake modes	82.2.19.2.2	Variable LPI_FW may be true or false	LPI:O	Yes [ ] No [ ] N/A [ ]
LP-02	Insertion and deletion of LPIs in groups of 8	82.2.3.6		LPI:M	Yes [ ] N/A [ ]
LP-03	BIP statistics during LPI	82.2.8	BIP statistics not updated during LPI	LPI:M	Yes [ ] N/A [ ]
LP-04	RAM insertion	82.2.9	Insertion of Rapid Alignment Markers meets the requirements of 82.2.9	LPI:M	Yes [ ] N/A [ ]
LP-05	Transmit state diagrams	82.2.19.3	Support LPI operation in Figure 82–16	LPI:M	Yes [ ] N/A [ ]
LP-06	Receive state diagrams	82.2.19.3	Support LPI operation in Figure 82–17	LPI:M	Yes [ ] N/A [ ]
LP-07	LPI transmit state diagrams	82.2.19.3.1	Meets the requirements of Figure 82–18	LPI:M	Yes [ ] N/A [ ]
LP-08	LPI receive state diagrams	82.2.19.3.1	Meets the requirements of Figure 82–19	LPI:M	Yes [ ] N/A [ ]
LP-09	LPI transmit timing	82.2.19.3.1	Meets the requirements of Table 82–8	LPI:M	Yes [ ] N/A [ ]
LP-10	LPI receive timing	82.2.19.3.1	Meets the requirements of Table 82–9	LPI:M	Yes [ ] N/A [ ]

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83. Physical Medium Attachment (PMA) sublayer, type 40GBASE-R and 100GBASE-R

83.1 Overview

83.1.1 Scope

This clause specifies the Physical Medium Attachment sublayer (PMA) that is common to two families of (40 Gb/s and 100 Gb/s) Physical Layer implementations, known as 40GBASE-R and 100GBASE-R. The PMA allows the PCS (specified in Clause 82) to connect in a media-independent way with a range of physical media. The 40GBASE-R PMA(s) can support any of the 40 Gb/s PMDs in Table 80–2. The 100GBASE-R PMA(s) can support any of the 100 Gb/s PMDs in Table 80–3 or Table 80–4, but does not provide the PMD service interface for 100GBASE-KP4 (Clause 94). The terms 40GBASE-R and 100GBASE-R are used when referring generally to Physical Layers using the PMA defined in this clause.

40GBASE-R and 100GBASE-R can be extended to support any full duplex medium requiring only that the PMD be compliant with the appropriate PMA interface.

The interfaces for the inputs of the 40GBASE-R and 100GBASE-R PMAs are defined in an abstract manner and do not imply any particular implementation. The optional physical instantiation of the PMD service interfaces for 40GBASE-SR4, 40GBASE-LR4, and 100GBASE-SR10 PMDs, known as XLPPI and CPPI, are defined in Annex 86A. The PMD service interfaces for other PMDs are defined in an abstract manner according to 80.3.1. For 40GBASE-R PMAs, electrical interfaces connecting PMA sublayers, known as XLAUI, are defined in Annex 83A and Annex 83B. For 100GBASE-R PMAs, electrical interfaces connecting PMA sublayers, known as CAUI-n, are defined in Annex 83A, Annex 83B, Annex 83D, and Annex 83E.

83.1.2 Position of the PMA in the 40GBASE-R or 100GBASE-R sublayers

Figure 83–1 shows the relationship of the PMA sublayer (shown shaded) with other sublayers to the ISO Open System Interconnection (OSI) reference model.

83.1.3 Summary of functions

The following is a summary of the principal functions implemented (when required) by the PMA in both the transmit and receive directions:

a) Adapt the PCSL formatted signal to the appropriate number of abstract or physical lanes.
b) Provide per input-lane clock and data recovery.
c) Provide bit-level multiplexing.
d) Provide clock generation.
e) Provide signal drivers.
f) Optionally provide local loopback to/from the PMA service interface.
g) Optionally provide remote loopback to/from the PMD service interface.
h) Optionally provide test-pattern generation and detection.
i) Tolerate Skew Variation.

In addition, the PMA provides receive link status information in the receive direction.

83.1.4 PMA sublayer positioning

An implementation may use one or more PMA sublayers to adapt the number and rate of the PCS lanes to the number and rate of the PMD lanes. The number of PMA sublayers required depends on the partitioning

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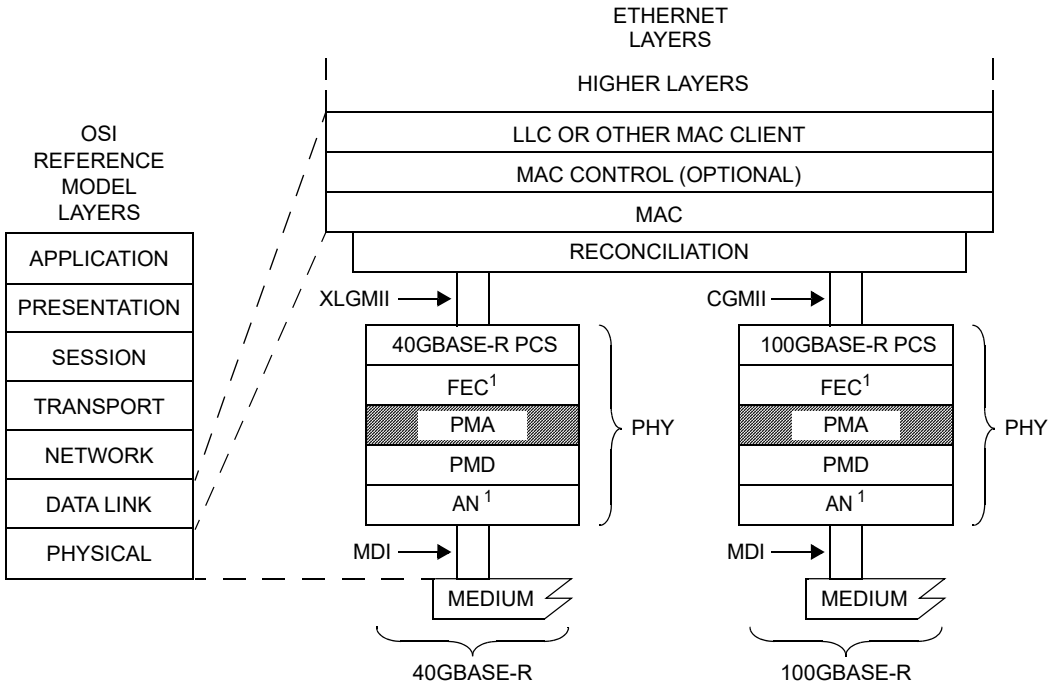

AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 83–1—40GBASE-R and 100GBASE-R PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

of functionality for a particular implementation. An example is illustrated in Figure 83–2. This example illustrates the partitioning that might arise from use of an FEC device that is separate from the PCS. Additional examples are illustrated in Annex 83C. Each PMA maps the PCSLs from p PMA input lanes to q PMA output lanes in the Tx direction, and from q PMA input lanes to p PMA output lanes in the Rx direction.

Management Data Input/Output (MDIO) Manageable Device (MMD) addresses 1, 8, 9, 10, and 11 are available for addressing multiple instances of PMA sublayers (see Table 45–1 for MMD device addresses). If the PMA sublayer that is closest to the PMD is packaged with the PMD, it shares MMD 1 with the PMD. If the PMD service interface is physically instantiated as nPPI (see Annex 86A), the PMA sublayer that is closest to the PMD will be addressed as MMD 8. More addressable instances of PMA sublayers, each one separated from lower addressable instances by chip-to-chip interfaces, may be implemented and addressed allocating MMD addresses to PMAs in increasing numerical order going from the PMD toward the PCS. The example shown in Figure 83–2 could be implemented with four addressable instances: MMD 8 addressing the lowest PMA sublayer (note that this cannot share MMD 1 with the PMD as they are not packaged together in this example), MMD 9 addressing the PMA sublayer above the XLAUI/CAUI-4 below the FEC, MMD 10 addressing the PMA sublayer below the XLAUI/CAUI-10 above the FEC, and MMD 11 addressing the PMA sublayer closest to the PCS.

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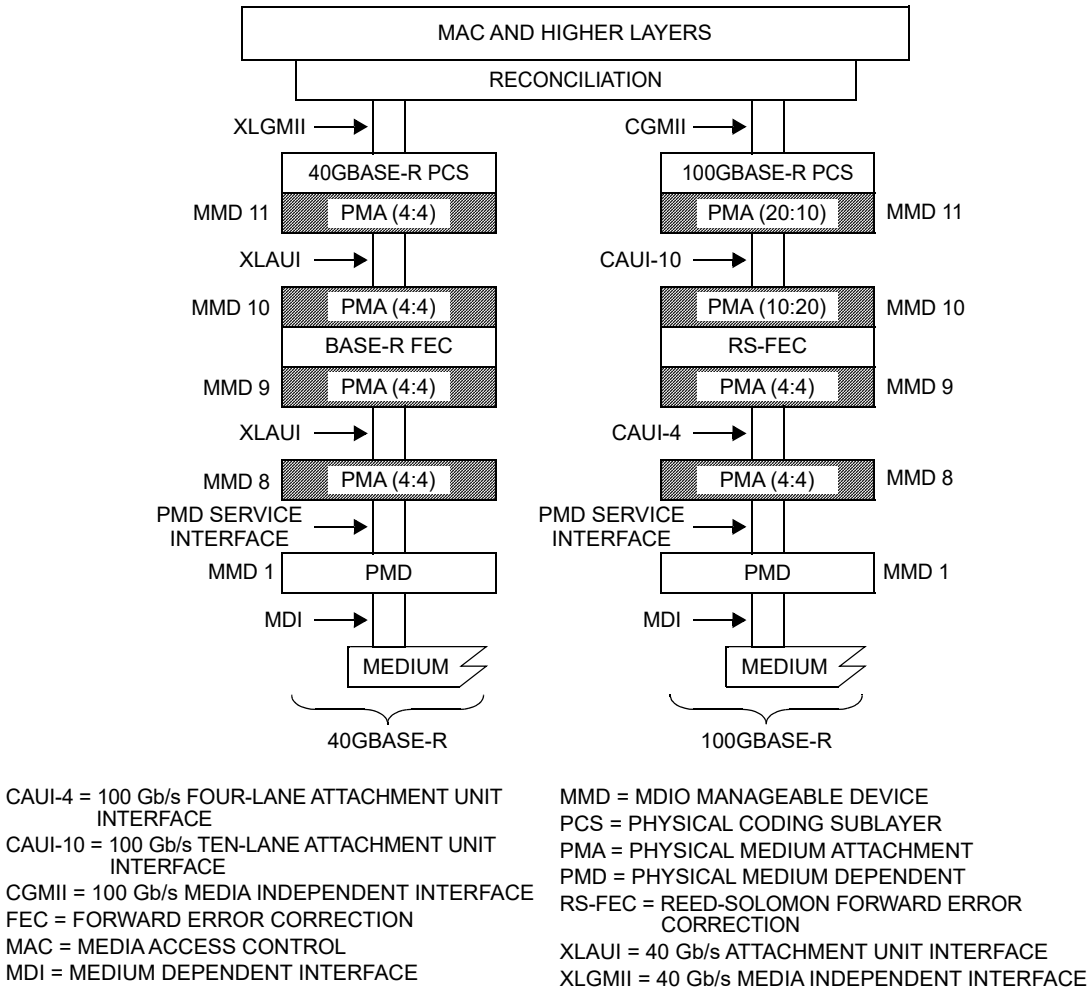

CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 83–2—Example 40GBASE-R and 100GBASE-R PMA layering

The number of input lanes and the number of output lanes for a PMA are always divisors of the number of PCSLs. For PMA sublayers supporting 40GBASE-R PMDs, the number of PCSLs is 4, and for PMA sublayers supporting 100GBASE-R PMDs, the number of PCSLs is 20.

The following guidelines apply to the partitioning of PMAs:

a) The inter-sublayer service interface, defined in 80.3, is used for the PMA, FEC, and PMD service interfaces supporting a flexible architecture with optional FEC and multiple PMA sublayers.
   1) An instance of this interface can only connect service interfaces with the same number of lanes, where the lanes operate at the same rate.
b) XLAUI and CAUI-n are physical instantiations of the connection between two adjacent PMA sublayers.
   1) As a physical instantiation, it defines electrical and timing specification as well as requiring a receive re-timing function
   2) XLAUI is a 10.3125 GBd by 4 lane physical instantiation of the respective 40 Gb/s connection
   3) CAUI-10 is a 10.3125 GBd by 10 lane physical instantiation of the respective 100 Gb/s connection
   4) CAUI-4 is a 25.78125 GBd by 4 lane physical instantiation of the respective 100 Gb/s connection

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c) The abstract inter-sublayer service interface can be physically instantiated as a XLAUI or CAUI-n, using associated PMAs to map to the appropriate number of lanes.
d) Opportunities for optional test-pattern generation, optional test-pattern detection, optional local loopback and optional remote loopback are dependent upon the location of the PMA sublayer in the implementation. See Figure 83–5.
e) A minimum of one PMA sublayer is required in a PHY.
f) A maximum of four PMA sublayers are addressable as MDIO MMDs.

83.2 PMA interfaces

All PMA variants for 40GBASE-R and 100GBASE-R signals are based on a generic specification of a bit mux function that applies to all input/output lane counts and each direction of transmission. Each direction of transmission employs one or more such bit muxes to adapt from the appropriate number of input lanes to the appropriate number of output lanes as illustrated in Figure 83–3.

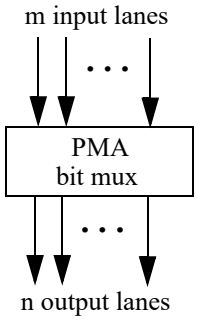

Figure 83–3—PMA bit mux used in both Tx and Rx directions

Conceptually, the PMA bit mux operates in one direction of transmission by demultiplexing PCSLs from m PMA input lanes and remultiplexing them into n PMA output lanes. The mapping of PCSLs from input to output lanes is not specified. See 83.5.2 and Figure 83–4 for details.

Figure 83–5 provides the functional block diagram of a PMA. The parameters of a PMA include the following:

— The aggregate rate supported (40GBASE-R or 100GBASE-R).
— The numbers of input and output lanes in each direction.
— Whether the PMA is adjacent to a physically instantiated interface (XLAUI/CAUI-n above or below, or PMD service interface below).
— Whether the PMA is adjacent to the PCS (or adjacent to FEC when FEC is adjacent to the PCS).
— Whether the PMA is adjacent to the PMD.

83.3 PMA service interface

The PMA service interface for 40GBASE-R and 100GBASE-R is an instance of the inter-sublayer service interface defined in 80.3. The PMA service interface primitives are summarized as follows:

PMA:IS_UNITDATA_*i*.request(tx_bit)
PMA:IS_UNITDATA_*i*.indication(rx_bit)
PMA:IS_SIGNAL.indication(SIGNAL_OK)

For a PMA with p lanes at the PMA service interface, the primitives are defined for $i = 0$ to $p - 1$.

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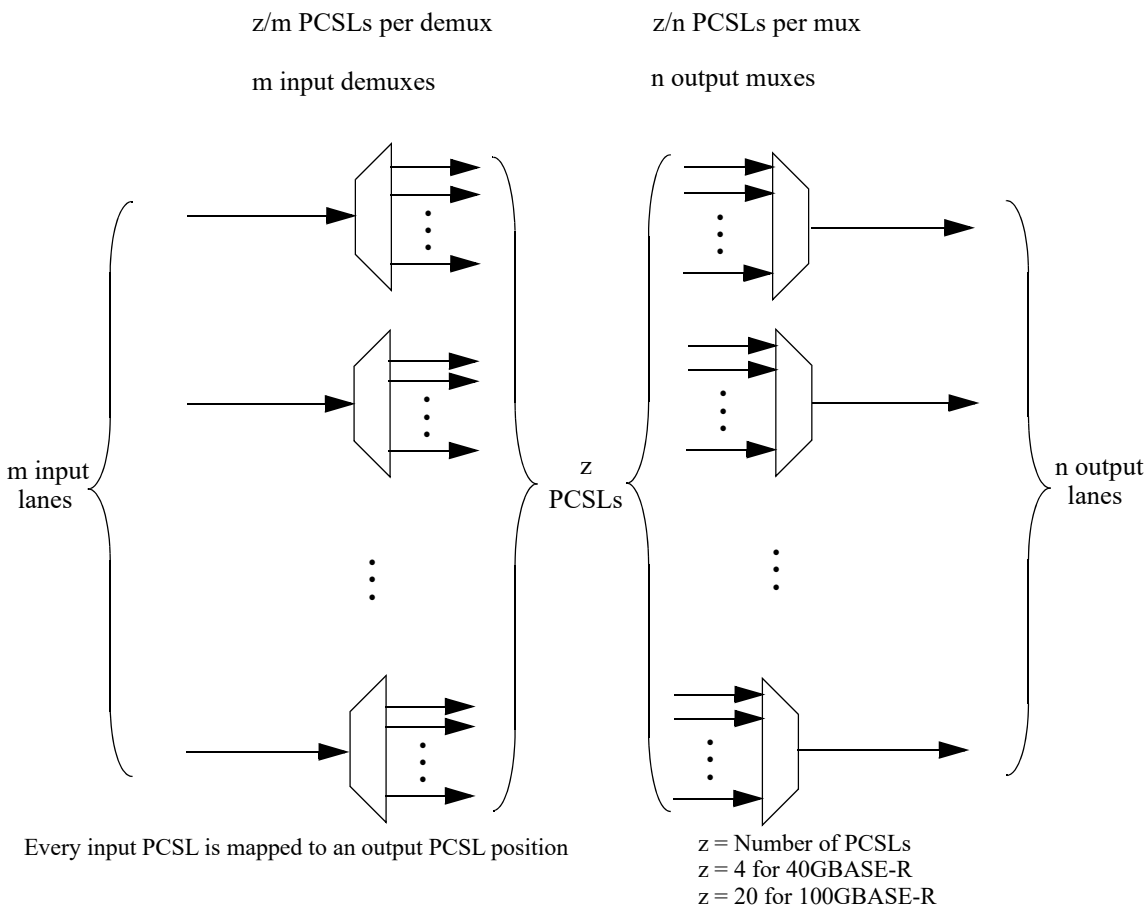

Figure 83–4—PMA bit mux operation used in both Tx and Rx directions

If the PMA client is the PCS or a BASE-R FEC sublayer (see Clause 74), the PMA (or PMA client) continuously sends four (for 40GBASE-R) or twenty (for 100GBASE-R) parallel bit streams to the PMA client (or PMA), each at the nominal signaling rate of the PCSL. If the PMA client is the 100GBASE-R RS-FEC sublayer (see Clause 91), the PMA continuously sends four parallel bit streams to the PMA client (or PMA), each at 25.78125 GBd.

If the PMA client is another PMA, for a PMA supporting a 40GBASE-R PMD, the number of PCSLs z = 4 and for a PMA supporting a 100GBASE-R PMD, the number of PCSLs z = 20. A PMA with p input lanes receives bits on each of its input lanes at z/p times the PCSL rate. Skew may exist between the bits received on each lane even though all lanes originate from the same synchronous source, so there is independence of arrival of bits on each lane.

In the Tx direction, if the bit from a PMA:IS_UNITDATA_*i*.request primitive is received over a physically instantiated interface (XLAUI/CAUI-n), clock and data are recovered on the lane receiving the bit. The bit is routed through the PMA to an output lane through a process that may demultiplex PCSLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs to output lanes. The bit is sent on an output lane to the sublayer below using the *inst*:IS_UNITDATA_*k*.request (*k* not necessarily equal to *i*) primitive (see 83.4).

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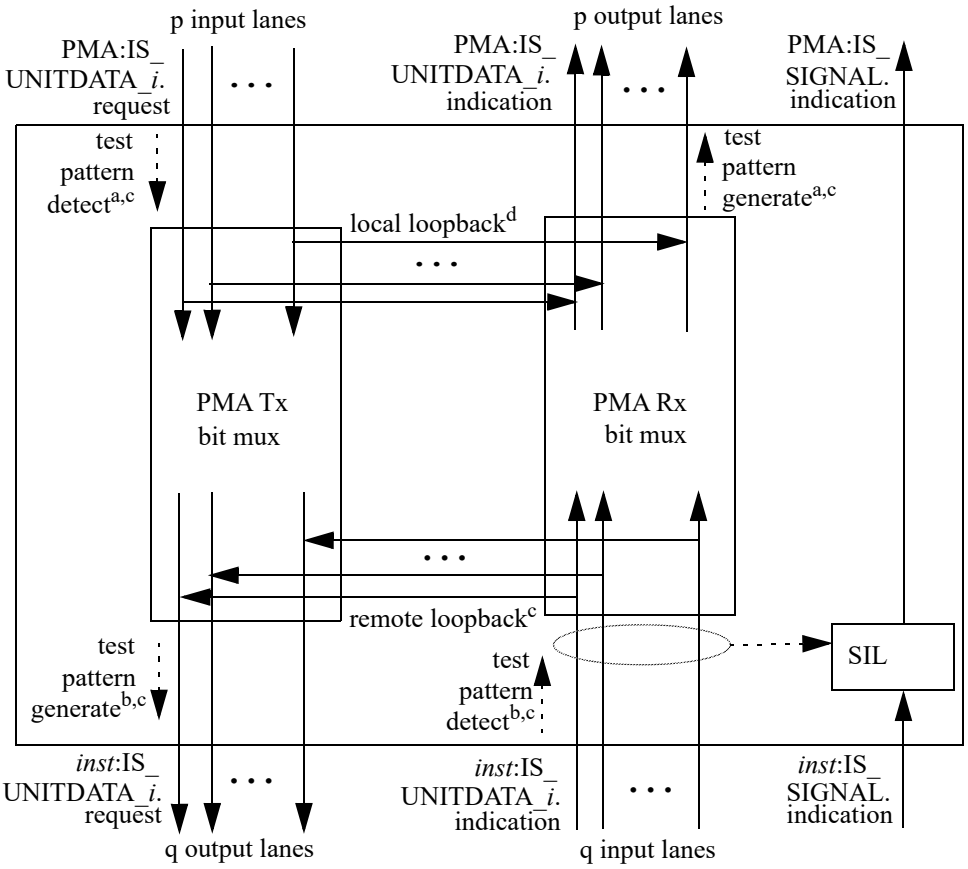

inst PMD, PMA, or FEC, depending on which sublayer is below this PMA
SIL Signal Indication Logic

[a] If physically instantiated interface (XLAUI/CAUI-n) immediately above this PMA.
[b] If physically instantiated interface (XLAUI/CAUI-n or PMD service interface) immediately below this PMA, or if this is the closest PMA to the PMD.
[c] Optional.
[d] Local loopback is required for PMAs adjacent to some PMDs, and optional for other PMAs. See 83.5.8.

Figure 83–5—PMA Functional Block Diagram

In the Rx direction, when data is being received from every input lane from the sublayer below the PMA that has a PCSL that is routed to a particular output lane at the PMA service interface, and (if necessary), buffers are filled to allow tolerating the Skew Variation that may appear between the input lanes, PCSLs are demultiplexed from the input lanes, remultiplexed to the output lanes, and bits are transferred over each output lane to the PMA client via the PMA:IS_UNITDATA_*i*.indication primitive.

The PMA:IS_SIGNAL.indication primitive is generated through a set of Signal Indication Logic (SIL) that reports signal health based on receipt of the *inst*:IS_SIGNAL.indication from the sublayer below, data being received on all of the input lanes from the sublayer below, buffers filled (if necessary) to accommodate Skew Variation, and bits being sent to the PMA client on all of the output lanes. When these conditions are met, the SIGNAL_OK parameter sent to the PMA client via the PMA:IS_SIGNAL.indication primitive will have the value OK. Otherwise, the SIGNAL_OK primitive will have the value FAIL.

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78, 78.1.3.3.1) then the inter-sublayer service interface includes four additional primitives defined as follows:

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IS_TX_MODE.request
IS_RX_MODE.request
IS_ENERGY_DETECT.indication
IS_RX_TX_MODE.indication

The IS_TX_MODE.request primitive is used to communicate the state of the PCS LPI transmit function to other sublayers in the PHY. The IS_RX_MODE.request primitive is used to communicate the state of the PCS LPI receive function to other sublayers. The IS_RX_TX_MODE.indication primitive is used to communicate the state of the rx_tx_mode parameter, that reflects the inferred state of the link partner's tx_mode parameter, from the PMA to other sublayers. The IS_ENERGY_DETECT.indication primitive is used to communicate that the PMD has detected the return of energy on the interface following a period of quiescence.

A physically instantiated service interface with the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option (see 78.1.3.3.1) may enter a low power state to conserve energy during periods of low link utilization. The ability to support transition to a low power state in the ingress direction is indicated by register 1.1.9 (PMA Ingress AUI Stop Ability, PIASA) and in the egress direction by register 1.1.8 (PMA Egress AUI Stop Ability, PEASA). Transition to the low power state is enabled in the ingress direction by register 1.7.9 (PMA Ingress AUI Stop Enable, PIASE) and in the egress direction by register 1.7.8 (PMA Egress AUI Stop Enable, PEASE). The system shall not assert the enable bit for an interface unless the corresponding ability bit at the other side of the interface is also asserted. If the PIASE bit is TRUE, then the PMA may disable transmitters on the physical instantiation of the ingress AUI when aui_tx_mode is QUIET. If the PEASE bit is TRUE, then the PMA may disable transmitters on the physical instantiation of the egress AUI when tx_mode is QUIET.

83.4 Service interface below PMA

Since the architecture supports multiple PMA sublayers for various PMD lane counts and device partitioning, there are several different sublayers that may appear below a PMA, including FEC, the PMD, or another PMA. The variable *inst* represents whichever sublayer appears below the PMA (e.g., another PMA, FEC, or PMD).

The sublayer below the PMA utilizes the inter-sublayer service interface defined in 80.3. The service interface primitives provided to the PMA are summarized as follows:

inst:IS_UNITDATA_*i*.request(tx_bit)
inst:IS_UNITDATA_*i*.indication(rx_bit)
inst:IS_SIGNAL.indication(SIGNAL_OK)

The number of lanes q for the service interface matches the number of lanes expected by the PMA. The *inst*:IS_UNITDATA_*i* primitives are defined for each lane $i = 0$ to $q - 1$ of the service interface below the PMA. Note that electrical and timing specifications of the service interface are defined if the interface is physically instantiated (e.g., XLAUI/CAUI-n or nPPI), otherwise the service interface is specified only abstractly. The interface between the PMA and the sublayer below consists of q lanes for data transfer and a status indicating a good signal sent by the sublayer below the PMA (see Figure 83–5).

In the Tx direction, when data is being received via the PMA:IS_UNITDATA_*i*.request primitive from every input lane from the PMA client at the PMA service interface (see 83.3) that has a PCSL that is routed to this output lane, and (if necessary), buffers are filled to allow tolerating the Skew Variation that may appear between the input lanes from the PMA client, PCSLs are demultiplexed from the input lanes, remultiplexed to the output lanes, and bits are transferred over each output lane to the sublayer below the PMA.

In the Rx direction, if the bit is received over a physically instantiated interface (XLAUI/CAUI-n or nPPI), clock and data are recovered on the lane receiving the bit. The bit is routed through the PMA to an output

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lane toward the PMA client through a process that may demultiplex PCSLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs to output lanes, and finally sending the bit on an output lane to the PMA client using the PMA:IS_UNITDATA_*k*.indication (*k* not necessarily equal to *i*) primitive at the PMA service interface.

83.5 Functions within the PMA

The purpose of the PMA is to adapt the PCSL formatted signal to an appropriate number of abstract or physical lanes, to recover clock from the received signal (if appropriate), and optionally to provide test signals and loopback. Each input (Tx direction) or output (Rx direction) lane between the PMA and the PMA client carries one or more PCSLs that are bit-multiplexed. All input and output lanes between the PMA and the PMA client carry the same number of PCSLs and operate at the same nominal signaling rate. Likewise, each input (Rx direction) or output (Tx direction) lane between the PMA and the sublayer below the PMA carries one or more PCSLs that are bit-multiplexed. All input and output lanes between the PMA and the sublayer below the PMA carry the same number of PCSLs and operate at the same nominal signaling rate. As described in 83.1.4, the number of input lanes and the number of output lanes for a given PMA are divisors of the number of PCSLs for the interface type supported.

83.5.1 Per input-lane clock and data recovery

If the interface between the PMA client and the PMA is physically instantiated as XLAUI/CAUI-n, the PMA shall meet the electrical and timing specifications in Annex 83A, Annex 83B, Annex 83D, or Annex 83E as appropriate. If the interface between the sublayer below the PMA and the PMA is physically instantiated as XLAUI/CAUI-n or nPPI, the PMA shall meet the electrical and timing specifications at the service interface as specified in Annex 83A, Annex 83B, Annex 83D, Annex 83E, or Annex 86A as appropriate.

83.5.2 Bit-level multiplexing

The PMA provides bit-level multiplexing in both the Tx and Rx directions. In the Tx direction, the function is performed among the bits received from the PMA client via the PMA:IS_UNITDATA_*i*.request primitives (for PMA client lanes $i = 0$ to $p - 1$) with the result sent to the service interface below the PMA using the *inst*:IS_UNITDATA_*i*.request primitives (for service interface lanes $i = 0$ to $q - 1$), referencing the functional block diagram shown in Figure 83–5. The bit multiplexing behavior is illustrated in Figure 83–4.

The aggregate signal carried by the group of input lanes or the group of output lanes is arranged as a set of PCSLs. For PMA sublayers supporting 40GBASE-R interfaces, the number of PCSLs z is 4, and the nominal signaling rate R of each PCSL is 10.3125 GBd. For PMA sublayers supporting 100GBASE-R interfaces, the number of PCSLs z is 20, and the nominal signaling rate R of each PCSL is 5.15625 GBd.

For a PMA with m input lanes (Tx or Rx direction), each input lane carries, bit multiplexed, z/m PCSLs. Each input lane has a nominal signaling rate of $R \times z/m$. If bit x received on an input lane belongs to a particular PCSL, the next bit of that same PCSL is received on the same input lane at bit position $x+(z/m)$. The z/m PCSLs may arrive in any sequence on a given input lane.

For a PMA with n output lanes (Tx or Rx direction), each output lane carries, bit multiplexed, z/n PCSLs. Each output lane has a nominal signaling rate of $R \times z/n$. Each PCSL is mapped from a position in the sequence on one of the z/m input lanes to a position in the sequence on one of the z/n output lanes. If bit x sent on an output lane belongs to a particular PCSL, the next bit of that same PCSL is sent on the same output lane at bit position $x + (z/n)$. The PMA shall maintain the chosen sequence of PCSLs on all output lanes while it is receiving a valid stream of bits on all input lanes.

Each PCSL received in any temporal position on an input lane is transferred into a temporal position on an output lane. As the PCS (see Clause 82) has fully flexible receive logic, an implementation is free to perform the mapping of PCSLs from input lanes to output lanes without constraint. Figure 83–6 illustrates one possible bit ordering for a 10:4 PMA bit mux. Other bit orderings are also valid.

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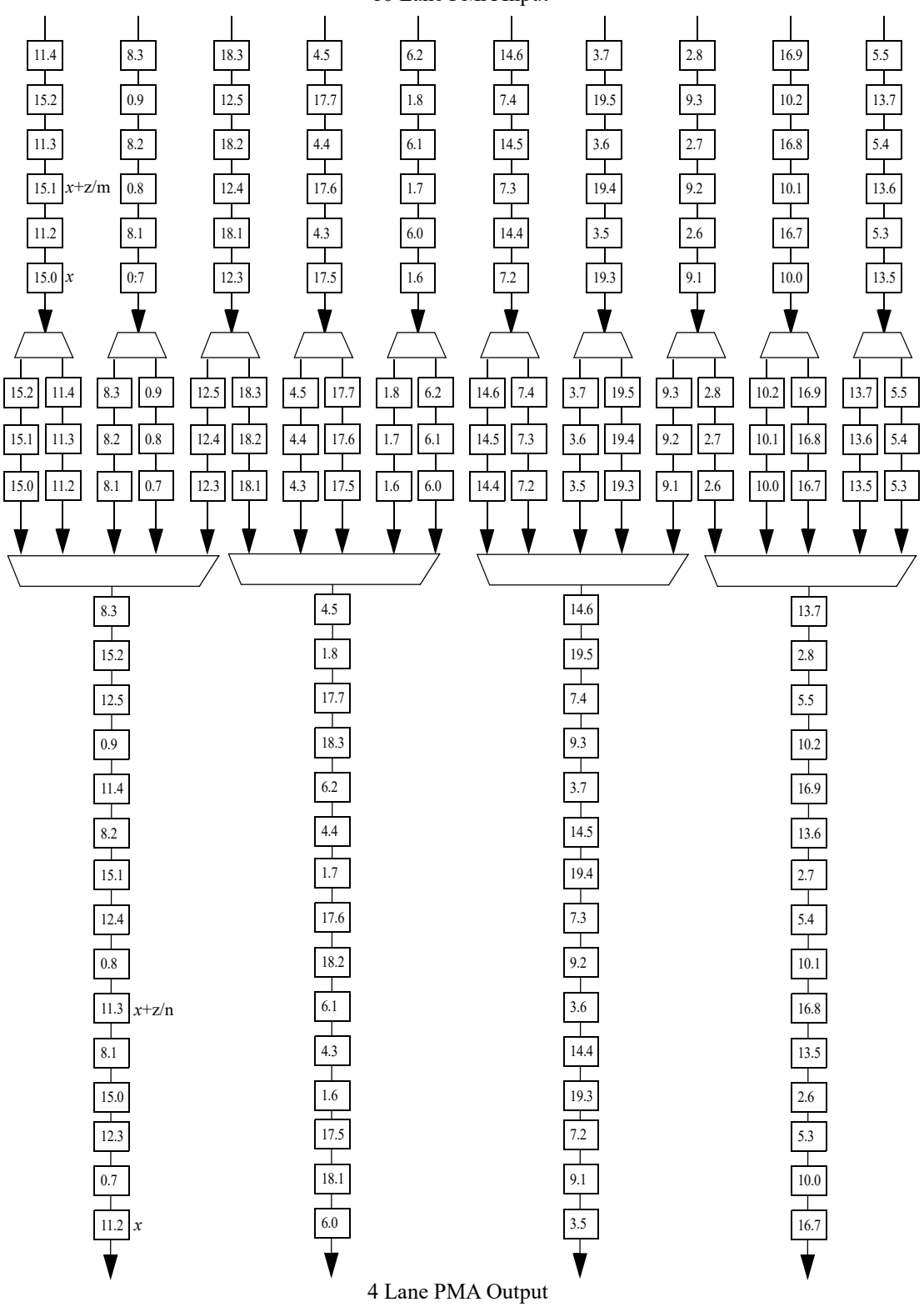

NOTE—i.k indicates bit k on PCSL i. Skew may exist between PCSLs.

Figure 83–6—Example 10: 4 PMA bit mux

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83.5.3 Skew and Skew Variation

The Skew (relative delay) between the PCSLs is kept within limits so that the information on the lanes can be reassembled by the PCS.

Any PMA that combines PCSLs from different input lanes onto the same output lane is required to tolerate Skew Variation between the input lanes without changing the PCSL positions on the output. Skew and Skew Variation are defined in 80.5. The limits for Skew and Skew Variation at physically instantiated interfaces are specified at Skew points SP0, SP1, and SP2 in the transmit direction and SP5, SP6, and SP7 in the receive direction as defined in 80.5 and illustrated in Figure 80–7, Figure 80–8, and Figure 80–9.

83.5.3.1 Skew generation toward SP0

In an implementation with one or more physically instantiated CAUI-n interfaces, the PMA that sends data in the transmit direction toward the CAUI-n that is closest to the RS-FEC (SP0 in Figure 80–9) shall produce no more than 29 ns of Skew between PCSLs toward the CAUI-n, and no more than 200 ps of Skew Variation.

83.5.3.2 Skew generation toward SP1

In an implementation with one or more physically instantiated XLAUI/CAUI-n interfaces, the PMA that sends data in the transmit direction toward the XLAUI/CAUI-n that is closest to the PMD (SP1 in Figure 80–7 and Figure 80–8) shall produce no more than 29 ns of Skew between PCSLs toward the XLAUI/CAUI-n, and no more than 200 ps of Skew Variation.

83.5.3.3 Skew tolerance at SP1

In an implementation with one or more physically instantiated XLAUI/CAUI-n interfaces, the PMA service interface that receives data in the transmit direction from the XLAUI/CAUI-n (SP1 in Figure 80–7 and Figure 80–8) shall tolerate the maximum amount of Skew Variation allowed at SP1 (200 ps) between input lanes while maintaining the bit ordering and position of each PCSL on each PMA lane in the transmit direction (toward the PMD).

83.5.3.4 Skew generation toward SP2

In an implementation with a physically instantiated PMD service interface, the PMA adjacent to the PMD service interface shall generate no more than 43 ns of Skew, and no more than 400 ps of Skew Variation between output lanes toward the PMD service interface (SP2 in Figure 80–7 and Figure 80–8). If there is a physically instantiated XLAUI/CAUI-n as well, then the Skew measured at SP1 is limited to no more than 29 ns of Skew and no more than 200 ps of Skew Variation.

83.5.3.5 Skew tolerance at SP5

In an implementation with a physically instantiated PMD service interface, the PMA adjacent to the PMD service interface (SP5) shall tolerate the maximum amount of Skew Variation allowed at SP5 (3.6 ns) between output lanes from the PMD service interface while maintaining the bit ordering and position of each PCSL on each PMA lane in the receive direction (toward the PCS).

83.5.3.6 Skew generation at SP6

In an implementation with one or more physically instantiated XLAUI/CAUI-n interfaces, at SP6 (the receive direction of the XLAUI/CAUI-n closest to the PCS), the PMA or group of PMAs between the PMD and the XLAUI/CAUI-n closest to the PCS shall deliver no more than 160 ns of Skew, and no more than 3.8 ns of Skew Variation between output lanes toward the XLAUI/CAUI-n in the Rx direction.

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If there is a physically instantiated PMD service interface as well, the Skew measured at SP5 is limited to no more than 145 ns of Skew and no more than 3.6 ns of Skew Variation. If there is no physically instantiated PMD service interface, the Skew measured at SP4 is limited to no more than 134 ns of Skew, and no more than 3.4 ns of Skew Variation.

83.5.3.7 Skew tolerance at SP6

In an implementation with one or more physically instantiated XLAUI/CAUI-n interfaces, the PMA between the XLAUI/CAUI-n closest to the PCS and the PCS shall tolerate the maximum amount of Skew Variation allowed at SP6 (3.8 ns) between input lanes while maintaining the bit order and position of PCSLs on lanes sent in the receive direction towards the PCS.

83.5.3.8 Skew generation toward SP7

In an implementation with one or more physically instantiated CAUI-n interfaces and RS-FEC, at SP7 (the receive direction of the CAUI-n closest to the PCS), the PMA or group of PMAs between the RS-FEC and the CAUI-n closest to the PCS shall deliver no more than 160 ns of Skew, and no more than 3.8 ns of Skew Variation between output lanes toward the CAUI-n in the Rx direction.

83.5.4 Delay constraints

The maximum cumulative delay contributed by up to four PMA stages in a PHY (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 83–1. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 80.4 and its references.

Table 83–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
40GBASE-R PMA	4096	8	102.4
100GBASE-R PMA	9216	18	92.16

83.5.5 Clocking architecture

A PMA with m input lanes and n output lanes shall clock the output lanes at m/n times the rate of the input lanes. This applies in both the Tx and Rx directions of transmission. In the case where the interfaces between the PMA client and the PMA and/or the PMA and the sublayer below the PMA are physically instantiated, the PMA may derive its input clock(s) from the electrical interface on one or more of the input lanes, and generate the output clock(s) with an appropriate PLL multiplier/divider circuit.

There is no requirement that the PMA clock all output lanes in unison. Examples of independent clocking of output lanes include the following:

— The case where the number of input and output lanes are equal (the PMA is provided for retiming and regeneration of the signal). This may be implemented without any rearrangement of PCSLs between input lanes and output lanes (although rearrangements are allowed), and such a PMA may be implemented by driving each output lane using the clock recovered from the corresponding input lane.

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— If the number of input and output lanes have a common factor, the PMA may be partitioned such that PCSLs from a subset of the input lanes are mapped only to a subset of the output lanes (for example, a 10:4 PMA could be implemented as two 5:2 PMAs). The output clock for one subset may be independent of the output clock for other subset(s).

83.5.6 Signal drivers

For cases where the interface between the PMA client and the PMA, or between the PMA and the sublayer below the PMA represent a physically instantiated interface, the PMA provides electrical signal drivers for that interface. The electrical and jitter/timing specifications for these interfaces appear in

— Annex 83A, which specifies the XLAUI/CAUI-10 interface for chip-to-chip applications.
— Annex 83B, which specifies the XLAUI/CAUI-10 interface for chip-to-module applications.
— Annex 83D, which specifies the CAUI-4 interface for chip-to-chip applications.
— Annex 83E, which specifies the CAUI-4 interface for chip-to-module applications.
— 86.2, which specifies the PMD service interface for 40GBASE-SR4 and 100GBASE-SR10 PMDs.
— 87.2, which specifies the PMD service interface for 40GBASE-LR4 and 40GBASE-ER4 PMDs.
— Annex 86A, which specifies the Parallel Physical Interface (XLPPI and CPPI), an optional physical instantiation of the PMD service interface for 40GBASE-SR4, 40GBASE-LR4, and 100GBASE-SR10 PMDs.

83.5.7 Link status

The PMA shall provide link status information to the PMA client using the PMA:IS_SIGNAL.indication primitive. The PMA continuously monitors the link status reported by the service interface below from the *inst*:IS_SIGNAL.indication primitive, and uses this as input to Signal Indication Logic (SIL) to determine the link status to report to the layer above. Other inputs to the SIL may include the status of clock and data recovery on the lanes from the service interface below the PMA and whether buffers/FIFOs have reached the required fill level to accommodate Skew Variation so that data is being sent on the output lanes.

83.5.8 PMA local loopback mode

PMA local loopback shall be provided by the PMA adjacent to the PMD for 40GBASE-KR4, 40GBASE-CR4, 100BASE-CR10, 100GBASE-KR4, and 100GBASE-CR4 PMDs. PMA local loopback mode is optional for other PMDs or for PMAs not adjacent to the PMD. If it is implemented, it shall be as described in this subclause (83.5.8).

The PMA sublayer may provide a local loopback function. The function involves looping back each input lane to the corresponding output lane. Each bit received from the PMA:IS_UNITDATA_*i*.request(tx_bit) primitive is looped back in the direction of the PCS using the PMA:IS_UNITDATA_*i*.indication(rx_bit) primitive.

During local loopback, the PMA performs normal bit muxing of PCSLs per 83.5.2 onto the lanes in the Tx direction toward the service interface below the PMA.

Ability to perform this function is indicated by the Local_loopback_ability status variable. If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.8.0 (45.2.1.7.15). A device is placed in local loopback mode when the Local_loopback_enable control variable is set to one, and removed from local loopback mode when this variable is set to zero. If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD control 1 register (bit 1.0.0, see 45.2.1.1.5).

83.5.9 PMA remote loopback mode (optional)

PMA remote loopback mode is optional. If implemented, it shall be as described in this subclause (83.5.9).

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Remote loopback, if provided, should be implemented in a PMA sublayer close enough to the PMD to maintain the bit sequence on each individual PMD lane. When remote loopback is enabled, each bit received over a lane of the service interface below the PMA via *inst*:IS_UNITDATA_*i*.indication is looped back to the corresponding output lane toward the PMD via *inst*:IS_UNITDATA_*i*.request. Note that the service interface below the PMA can be provided by the FEC, PMD, or another PMA sublayer.

During remote loopback, the PMA performs normal bit muxing of PCSLs per 83.5.2 onto the lanes in the Rx direction towards the PMA client.

The ability to perform this function is indicated by the Remote_loopback_ability status variable. If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.13.15 (45.2.1.12.1). A device is placed in remote loopback mode when the Remote_loopback_enable control variable is set to one, and removed from remote loopback mode when this variable is set to zero. If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD Control register 1 (bit 1.0.1, see 45.2.1.1.4).

83.5.10 PMA test patterns (optional)

Where the output lanes of the PMA appear on a physically instantiated interface XLAUI/CAUI-n or the PMD service interface (whether or not it is physically instantiated), the PMA may optionally generate and detect test patterns. These test patterns are used to test adjacent layer interfaces for an individual PMA sublayer or to perform testing between a physically instantiated interface of a PMA sublayer and external testing equipment.

The ability to generate each of the respective test patterns in each direction of transmission are indicated by the PRBS9_Tx_generator_ability, PRBS9_Rx_generator_ability, PRBS31_Tx_generator_ability, and PRBS31_Rx_generator_ability status variables, which if a Clause 45 MDIO is implemented are accessible through bits 1.1500.5, 1.1500.4, 1.1500.3, and 1.1500.1, respectively (see 45.2.1.169).

The ability to check PRBS31 test patterns in each direction of transmission are indicated by the PRBS31_Tx_checker_ability and PRBS31_Rx_checker_ability status variables, which, if a Clause 45 MDIO is implemented, are accessible through bits 1.1500.2 and 1.1500.0, respectively (see 45.2.1.169).

If supported, when send Tx PRBS31 test pattern is enabled by the PRBS31_enable and PRBS_Tx_gen_enable control variables, the PMA shall generate a PRBS31 pattern (as defined in 49.2.8) on each of the lanes toward the service interface below the PMA via the *inst*:IS_UNITDATA_*i*.request primitive. To avoid correlated crosstalk, it is highly recommended that the PRBS31 patterns generated on each lane be generated from independent, random seeds or at a minimum offset of 20 000 UI between the PRBS31 sequence on any lane and any other lane. When send Tx PRBS31 test pattern is disabled, the PMA returns to normal operation performing bit multiplexing as described in 83.5.2. If a Clause 45 MDIO is implemented, the PRBS31_enable and PRBS_Tx_gen_enable control variables are accessible through bits 1.1501.7 and 1.1501.3 (see 45.2.1.170).

If supported, when send Rx PRBS31 test pattern is enabled by the PRBS31_enable and PRBS_Rx_gen_enable control variables, the PMA shall generate a PRBS31 pattern on each of the lanes toward the PMA client via the PMA:IS_UNITDATA_*i*.indication primitive. While this test pattern is enabled, the PMA also generates PMA:IS_SIGNAL.indication(SIGNAL_OK) toward the PMA client independent of the link status at the service interface below the PMA. When send Rx PRBS31 test pattern is disabled, the PMA returns to normal operation performing bit multiplexing as described in 83.5.2. If a Clause 45 MDIO is implemented, the PRBS31_enable and PRBS_Rx_gen_enable control variables are accessible through bits 1.1501.7 and 1.1501.1 (see 45.2.1.170).

If supported, when check Tx PRBS31 test pattern mode is enabled by the PRBS31_enable and PRBS_Tx_check_enable control variables, the PMA shall check for the PRBS31 pattern on each of the lanes received from the PMA client via the PMA:IS_UNITDATA_*i*.request primitive. The checker shall

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increment the test-pattern error counter by one for each incoming bit error in the PRBS31 pattern for isolated single bit errors. Implementations should be capable of counting at least one error whenever one or more errors occur in a sliding 1000-bit window. If a Clause 45 MDIO is implemented, the PRBS31_enable and PRBS_Tx_check_enable control variables are accessible through bits 1.1501.7 and 1.1501.2 (see 45.2.1.170). The Tx test-pattern error counters Ln0_PRBS_Tx_test_err_counter through Ln9_PRBS_Tx_test_err_counter count, per lane, errors in detecting the PRBS31 pattern on the lanes from the PMA client. If a Clause 45 MDIO is implemented, these counters are accessible through registers 1.1600 through 1.1609 (see 45.2.1.173). When check Tx PRBS31 test pattern is disabled, the PMA expects normal traffic and test-pattern error counting does not continue. While in check Tx PRBS31 test-pattern mode, bit multiplexing continues as described in 83.5.2. Note that bit multiplexing of per-lane PRBS31 may produce a signal which is not meaningful for downstream sublayers.

If supported, when check Rx PRBS31 test-pattern mode is enabled by the PRBS31_enable and PRBS_Rx_check_enable control variables, the PMA shall check for the PRBS31 pattern on each of the lanes received from the service interface below the PMA via the *inst*:IS_UNITDATA_*i*.indication primitive. If a Clause 45 MDIO is implemented, the PRBS31_enable and PRBS_Rx_check_enable control variables are accessible through bits 1.1501.7 and 1.1501.0 (see 45.2.1.170). The Rx test-pattern error counters Ln0_PRBS_Rx_test_err_counter through Ln9_PRBS_Rx_test_err_counter count, per lane, errors in detecting the PRBS31 pattern on the lanes from the service interface below the PMA. If a Clause 45 MDIO is implemented, these counters are accessible through registers 1.1700 through 1.1709 (see 45.2.1.174). While in check Rx PRBS31 test-pattern mode, the PMA:IS_SIGNAL.indication primitive does not indicate a valid signal. When check Rx PRBS31 test pattern is disabled, the PMA returns to normal operation performing bit multiplexing as described in 83.5.2.

If supported, when send Tx PRBS9 test-pattern mode is enabled by the PRBS9_enable and PRBS_Tx_gen_enable control variables, the PMA shall generate a PRBS9 pattern (as defined in Table 68–6) on each lane toward the service interface below the PMA via the *inst*:IS_UNITDATA_*i*.request primitive. If a Clause 45 MDIO is implemented, the PRBS9_enable and PRBS_Tx_gen_enable control variables are accessible through bits 1.1501.6 and 1.1501.3 (see 45.2.1.170). When send Tx PRBS9 test-pattern mode is disabled, the PMA returns to normal operation performing bit multiplexing as described in 83.5.2.

If supported, when send Rx PRBS9 test-pattern mode is enabled by the PRBS9_enable and PRBS_Rx_gen_enable control variables, the PMA shall generate a PRBS9 pattern on each lane toward the PMA client via the PMA:IS_UNITDATA_*i*.indication primitive. The PMA will also generate PMA:IS_SIGNAL.indication(SIGNAL_OK) toward the PMA client independent of the link status at the service interface below the PMA. If a Clause 45 MDIO is implemented, the PRBS9_enable and PRBS_Rx_gen_enable control variables are accessible through bits 1.1501.6 and 1.1501.1 (see 45.2.1.170). When send Rx PRBS9 test-pattern mode is disabled, the PMA returns to normal operation performing bit multiplexing as described in 83.5.2.

Note that PRBS9 is intended to be checked by external test gear, and no PRBS9 checking function is provided within the PMA.

Transmit square wave test-pattern mode optionally applies to each lane of the Tx direction PMA towards a physically instantiated XLAUI/CAUI-n or towards the PMD service interface whether or not it is physically instantiated. The ability to perform this function is indicated by the Square_wave_ability status variable. If a Clause 45 MDIO is implemented, the Square_wave_ability status variable is accessible through the Square wave test ability bit 1.1500.12 (see 45.2.1.169). If implemented, the transmit square wave test-pattern mode is enabled by control variables Square_wave_enable_0 through Square_wave_enable_9. If a Clause 45 MDIO is implemented, these control variables are accessible through the square wave testing control and status register bits 1.1510.0 through 1.1510.9 (limited to the number of lanes of the service interface below the PMA, see 45.2.1.171). When enabled, the PMA shall generate a square wave test pattern (8 ones followed by 8 zeros) on the square wave enabled lanes toward the service interface below the PMA via the *inst*:IS_UNITDATA_*i*.request primitive. Lanes for which square wave is not enabled will transmit normal

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data resulting from the bit multiplexing operations described in 83.5.2 or test patterns as determined by other registers. When transmit square wave test pattern is disabled for all lanes, the PMA will perform normal operation performing bit multiplexing as described in 83.5.2 or transmit test patterns as determined by other registers.

83.5.11 Energy Efficient Ethernet

When the optional Energy Efficient Ethernet (EEE) deep sleep capability is supported and the PMA service interface is physically instantiated as XLAUI or CAUI-n, the additional functions listed in this subclause are required. These functions enable the communication of service interface parameters that are essential to the operation of the EEE deep sleep capability. The timing parameters for EEE operation are shown in Table 83–2.

Table 83–2—EEE timing parameters

Timer	Symbol	Min.	Max.	Units
PMA quiet signal duration	T_{pq}	200	225	ns
Energy detect hold-off time	T_{ho}	750	800	ns
Time to assert PMA quiet detect	T_{dq}	25	50	ns
Time to assert PMA alert detect	T_{da}	—	25	ns
Time to hold rx_lpi_active = true	T_{ht}	4000	5500	ns

83.5.11.1 PMA quiet and alert signals

The PMA quiet and alert signals are generated on each lane with a self-synchronizing scrambler. The scrambler shall produce the same result as the implementation shown in Figure 83–7. This implements the scrambler polynomial defined by Equation (83–1).

$$G(x) = 1 + x^{28} + x^{31} \tag{83–1}$$

To generate the PMA quiet signal the input to the scrambler shall be 0. To generate the PMA alert signal the input to the scrambler shall be 1.

The initial state the scrambler of a given lane of PMA service interface is chosen to minimize the correlation between lanes.

83.5.11.2 Detection of PMA quiet and alert signals

Each lane detects the PMA quiet and alert signals at the output of a self-synchronizing descrambler that implements the polynomial defined in Equation (83–1). The descrambler shall produce the same result as the implementation shown in Figure 83–8.

The output of the descrambler is considered in consecutive, non-overlapping blocks of 256 bits. If the number of zeros detected in a given 256-bit block is greater than or equal 224, then the lane shall indicate that the PMA quiet signal is detected. If the number of ones detected in a given block is greater than or equal to 224, then the lane shall indicate that the PMA alert signal has been detected. Otherwise, the lane infers

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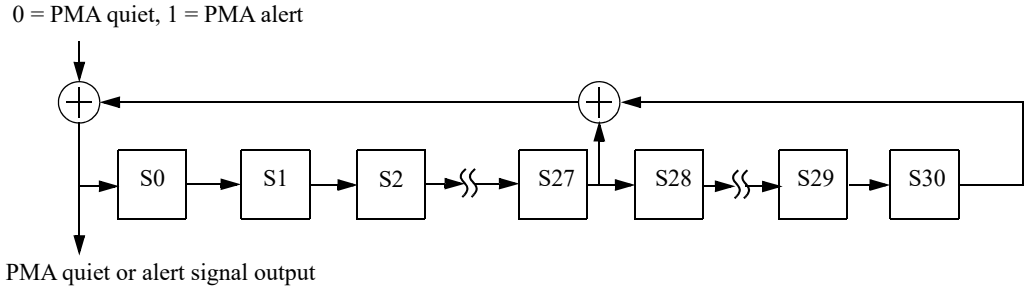

Figure 83–7—Scrambler for PMA quiet and alert signals

that normal data is being received and shall not indicate that either the PMA quiet or PMA alert signal has been detected.

The PMA shall indicate that the quiet signal is detected when all lanes of the PMA service interface have detected the quiet signal. The PMA shall indicate that the alert signal is detected when all lanes of the PMA service interface have detected the alert signal. Otherwise, the PMA infers that normal data is being received and shall not indicate that either the PMA quiet or PMA alert signal has been detected.

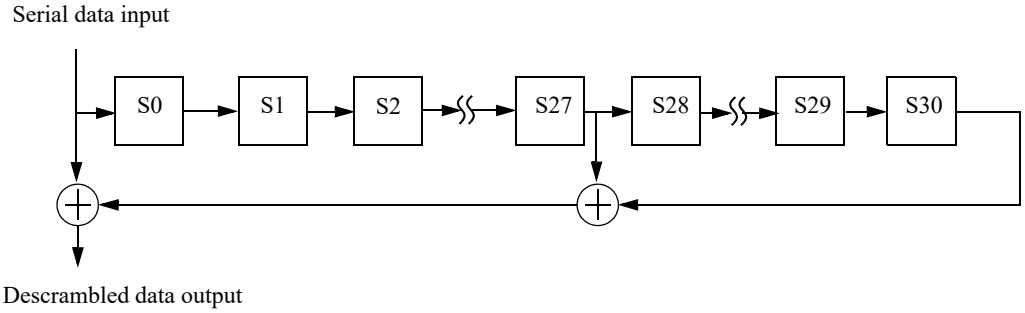

Figure 83–8—Descrambler for PMA quiet and alert signals

83.5.11.3 Additional transmit functions in the Tx direction

If the PMA client is the PCS, BASE-R FEC, or RS-FEC sublayer or is a PMA sublayer where the number of input lanes is not equal to the number of output lanes, then the PMA sublayer shall insert the PMA quiet and alert signals as follows: When the value of tx_mode is QUIET, the PMA inserts the PMA quiet signal defined in 83.5.11.1. When the value of tx_mode is ALERT, the PMA inserts the PMA alert signal defined in 83.5.11.1. For all other values of tx_mode, the PMA output is defined by the bit multiplexing function.

If XLAUI or CAUI-n is permitted to shut down (see 83.3), the variable aui_tx_mode shall be assigned the current value of tx_mode with the following exception. When tx_mode transitions from DATA to QUIET, the value of aui_tx_mode is held at DATA and the timer pma_quiet_timer (T_{pq}) is started. If tx_mode is QUIET when the timer expires, then aui_tx_mode is set to QUIET. If tx_mode is set to a value other than QUIET before the timer expires, then aui_tx_mode is set to DATA.

If XLAUI or CAUI-n is not permitted to shut down, aui_tx_mode shall be assigned the value DATA.

PMA functions in the Tx direction may be disabled in order to conserve energy while aui_tx_mode is QUIET.

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83.5.11.4 Additional receive functions in the Tx direction

For a PMA that is separated from the PCS by XLAUI or CAUI-n, the value of tx_mode shall be assigned as follows: If the PMA quiet signal is detected, the value of tx_mode is set to QUIET. If the PMA alert signal is detected, the value of tx_mode is set to ALERT. Otherwise, the value of tx_mode is DATA.

If XLAUI or CAUI-n is permitted to shut down (see 83.3), then the variable aui_rx_mode shall be assigned as follows: The variable aui_rx_mode is initialized to DATA upon PMA power on or reset. When the PMA quiet signal is detected, the timer hold_off_timer (T_{ho}) is started. If the PMA alert signal is not detected before the timer expires, then aui_rx_mode is set to QUIET and SIGNAL_DETECT is set to FAIL. While aui_rx_mode is QUIET, it shall be set to DATA when SIGNAL_DETECT transitions from FAIL to OK. The value of tx_mode is inferred to be ALERT and the timer alert_timer (T_a) started upon a transition of aui_rx_mode from QUIET to DATA. The value of ALERT shall be held until alert_timer expires after which the value of tx_mode shall be set to DATA.

If XLAUI or CAUI-n is not permitted to shut down, aui_rx_mode shall be assigned the value DATA.

PMA functions in the Tx direction may be disabled in order to conserve energy while aui_rx_mode is QUIET.

83.5.11.5 Additional transmit functions in the Rx direction

For a PMA that is separated from the PCS by XLAUI or CAUI-n, the value of rx_mode shall be assigned as follows. The value of rx_mode is initialized to DATA upon PMA power on or reset. When the PMA quiet signal is detected, the timer hold_off_timer (T_{ho}) is started. If the PMA alert signal is not detected before the timer expires, then rx_mode is set to QUIET. While rx_mode is QUIET, it shall be set to DATA when the PMA alert signal is detected or energy_detect (or SIGNAL_OK) transitions from false to true.

The value of rx_tx_mode may be passed via the PMA:IS_RX_TX_MODE.indication primitive, otherwise it shall be assigned as follows. If the PMA quiet signal is detected, the value of rx_tx_mode is set to QUIET. The value of rx_tx_mode is set to be ALERT and the timer alert_timer (T_a) started upon a transition of the value of rx_mode from QUIET to DATA. The value of ALERT shall be held until alert_timer expires after which the value of rx_tx_mode shall be set to DATA.

If XLAUI or CAUI-n is permitted to shut down (see 83.3), the variable aui_tx_mode shall be assigned the current value of rx_tx_mode with the following exception. When rx_tx_mode transitions from DATA to QUIET, the value of aui_tx_mode is held at DATA and the timer pma_quiet_timer (T_{pq}) is started. If rx_tx_mode is QUIET when the timer expires, then aui_tx_mode is set to QUIET. If rx_tx_mode is set to a value other than QUIET before the timer expires, then aui_tx_mode is set to DATA.

If XLAUI or CAUI-n is not permitted to shut down, aui_tx_mode shall be assigned the value DATA.

PMA functions in the Rx direction may be disabled in order to conserve energy while aui_tx_mode is QUIET.

If the PMA is the client of the BASE-R FEC or RS-FEC sublayer or a PMA sublayer where the number of input lanes is not equal to the number of output lanes, then the PMA sublayer shall insert the PMA quiet and alert signals as follows. When the value of rx_tx_mode is QUIET, the PMA inserts the PMA quiet signal defined in 83.5.11.1. When the value of rx_tx_mode is ALERT, the PMA inserts the PMA alert signal defined in 83.5.11.1. For all other values of rx_tx_mode, the PMA output is defined by the bit multiplexing function.

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83.5.11.6 Additional receive functions in the Rx direction

For a PMA that is separated from the PMD by XLAUI or CAUI, the value of energy_detect shall be assigned as follows. The value of energy_detect is initialized to true upon PMA power on or reset. When the value of rx_mode is set to QUIET, the value of energy_detect is set to false. The value of energy_detect is set to true when the PMA alert signal is detected or SIGNAL_DETECT transitions from FAIL to OK.

The value of rx_tx_mode shall be inferred as follows. If the PMA quiet signal is detected, the value of rx_tx_mode is set to QUIET. The value of rx_tx_mode is set to be ALERT and the timer alert_timer (T_a) started upon a transition of the value of rx_mode from QUIET to DATA. The value of ALERT shall be held until alert_timer expires after which the value of rx_tx_mode shall be set to DATA.

If XLAUI or CAUI is permitted to shut down (see 83.3), then the variable aui_rx_mode shall be assigned as follows. The variable aui_rx_mode is initialized to DATA upon PMA power on or reset. When the PMA quiet signal is detected, the timer hold_off_timer (T_{ho}) is started. If the PMA alert signal is not detected before the timer expires, then aui_rx_mode is set to QUIET. While aui_rx_mode is QUIET, it shall be set to DATA when SIGNAL_DETECT transitions from FAIL to OK. The value of tx_mode is assigned to be ALERT and the timer alert_timer (T_a) started upon a transition of aui_rx_mode from QUIET to DATA. The value of ALERT shall be held until alert_timer expires after which the value of tx_mode shall be set to DATA.

If XLAUI or CAUI is not permitted to shut down, aui_rx_mode shall be assigned the value DATA.

PMA functions in the Rx direction may be disabled in order to conserve energy while aui_rx_mode is QUIET.

83.5.11.7 Support for BASE-R FEC

When the PMA is a client of the BASE-R FEC sublayer, the rx_lpi_active parameter of the IS_RX_LPI_ACTIVE.request primitive shall be defined as follows. The value of rx_lpi_active is initialized to false upon PMA power on or reset. The value of rx_lpi_active is set to true and the timer rx_lpi_active_timer (T_{ht}) started upon a transition of the value of rx_mode from QUIET to DATA. When the timer expires, the value of rx_lpi_active is set to false.

83.6 PMA MDIO function mapping

The optional MDIO capability described in Clause 45 describes several variables that provide control and status information for and about the PMA. Since a given implementation may employ more than one PMA sublayer, the PMA control and status information is organized into multiple addressable instances, one for each possible PMA sublayer. See 45.2.1 and 83.1.4 for the allocation of MMD addresses to PMA sublayers. Control and status registers for MMD 8, 9, 10, and 11 will use the Extended PMA control and status registers at identical locations to those for MMD 1.

Mapping of MDIO control variables to PMA control variables is shown in Table 83–3. Mapping of MDIO status variables to PMA status variables is shown in Table 83–4. Mapping of MDIO counter to PMA counters is shown in Table 83–5. These tables provide the register and bit numbers for the PMA addressed as MMD 1. For implementations with multiple PMA sublayers, additional PMA sublayers use the corresponding register and bit numbers in MMDs 8, 9, 10, and 11 as necessary.

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Table 83–3—MDIO/PMA control variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
PMA remote loopback	PMA/PMD control 1	1.0.1	Remote_loopback_enable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
PRBS31 pattern enable	PRBS pattern testing control	1.1501.7	PRBS31_enable
PRBS9 pattern enable	PRBS pattern testing control	1.1501.6	PRBS9_enable
Tx generator enable	PRBS pattern testing control	1.1501.3	PRBS_Tx_gen_enable
Tx checker enable	PRBS pattern testing control	1.1501.2	PRBS_Tx_check_enable
Rx generator enable	PRBS pattern testing control	1.1501.1	PRBS_Rx_gen_enable
Rx checker enable	PRBS pattern testing control	1.1501.0	PRBS_Rx_check_enable
Lane 0 SW enable	Square wave testing control	1.1510.0	Square_wave_enable_0
Lane 1 SW enable	Square wave testing control	1.1510.1	Square_wave_enable_1
Lane 2 SW enable	Square wave testing control	1.1510.2	Square_wave_enable_2
Lane 3 SW enable	Square wave testing control	1.1510.3	Square_wave_enable_3
Lane 4 SW enable	Square wave testing control	1.1510.4	Square_wave_enable_4
Lane 5 SW enable	Square wave testing control	1.1510.5	Square_wave_enable_5
Lane 6 SW enable	Square wave testing control	1.1510.6	Square_wave_enable_6
Lane 7 SW enable	Square wave testing control	1.1510.7	Square_wave_enable_7
Lane 8 SW enable	Square wave testing control	1.1510.8	Square_wave_enable_8
Lane 9 SW enable	Square wave testing control	1.1510.9	Square_wave_enable_9
PIASE	PMA/PMD control 2	1.7.9	PIASE
PEASE	PMA/PMD control 2	1.7.8	PEASE

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Table 83–4—MDIO/PMA status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMA status variable
PMA remote loopback ability	40G/100G PMA/PMD extended ability register	1.13.15	Remote_loopback_ability
PMA local loopback ability	PMA/PMD status 2 register	1.8.0	Local_loopback_ability
PRBS9 Tx generator ability	Test-pattern ability register	1.1500.5	PRBS9_Tx_generator_ability
PRBS9 Rx generator ability	Test-pattern ability register	1.1500.4	PRBS9_Rx_generator_ability
PRBS31Tx generator ability	Test-pattern ability register	1.1500.3	PRBS31_Tx_generator_ability
PRBS31Tx checker ability	Test-pattern ability register	1.1500.2	PRBS31_Tx_checker_ability
PRBS31 Rx generator ability	Test-pattern ability register	1.1500.1	PRBS31_Rx_generator_ability
PRBS31 Rx checker ability	Test-pattern ability register	1.1500.0	PRBS31_Rx_checker_ability
Square wave test ability	Test-pattern ability register	1.1500.12	Square_wave_ability
PIASA	PMA/PMD status 1	1.1.9	PIASA
PEASA	PMA/PMD status 1	1.1.8	PEASA

Table 83–5—MDIO/PMA counters mapping

MDIO variable	PMA/PMD register name	Register/bit number	PMA status variable
Error counter Tx, lane 0	PRBS Tx pattern testing error counter, lane 0	1.1600	Ln0_PRBS_Tx_test_err_counter
Error counter Tx, lane 1	PRBS Tx pattern testing error counter, lane 1	1.1601	Ln1_PRBS_Tx_test_err_counter
Error counter Tx, lane 2	PRBS Tx pattern testing error counter, lane 2	1.1602	Ln2_PRBS_Tx_test_err_counter
Error counter Tx, lane 3	PRBS Tx pattern testing error counter, lane 3	1.1603	Ln3_PRBS_Tx_test_err_counter
Error counter Tx, lane 4	PRBS Tx pattern testing error counter, lane 4	1.1604	Ln4_PRBS_Tx_test_err_counter
Error counter Tx, lane 5	PRBS Tx pattern testing error counter, lane 5	1.1605	Ln5_PRBS_Tx_test_err_counter
Error counter Tx, lane 6	PRBS Tx pattern testing error counter, lane 6	1.1606	Ln6_PRBS_Tx_test_err_counter
Error counter Tx, lane 7	PRBS Tx pattern testing error counter, lane 7	1.1607	Ln7_PRBS_Tx_test_err_counter

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Table 83–5—MDIO/PMA counters mapping *(continued)*

MDIO variable	PMA/PMD register name	Register/bit number	PMA status variable
Error counter Tx, lane 8	PRBS Tx pattern testing error counter, lane 8	1.1608	Ln8_PRBS_Tx_test_err_counter
Error counter Tx, lane 9	PRBS Tx pattern testing error counter, lane 9	1.1609	Ln9_PRBS_Tx_test_err_counter
Error counter Rx, lane 0	PRBS Rx pattern testing error counter, lane 0	1.1700	Ln0_PRBS_Rx_test_err_counter
Error counter Rx, lane 1	PRBS Rx pattern testing error counter, lane 1	1.1701	Ln1_PRBS_Rx_test_err_counter
Error counter Rx, lane 2	PRBS Rx pattern testing error counter, lane 2	1.1702	Ln2_PRBS_Rx_test_err_counter
Error counter Rx, lane 3	PRBS Rx pattern testing error counter, lane 3	1.1703	Ln3_PRBS_Rx_test_err_counter
Error counter Rx, lane 4	PRBS Rx pattern testing error counter, lane 4	1.1704	Ln4_PRBS_Rx_test_err_counter
Error counter Rx, lane 5	PRBS Rx pattern testing error counter, lane 5	1.1705	Ln5_PRBS_Rx_test_err_counter
Error counter Rx, lane 6	PRBS Rx pattern testing error counter, lane 6	1.1706	Ln6_PRBS_Rx_test_err_counter
Error counter Rx, lane 7	PRBS Rx pattern testing error counter, lane 7	1.1707	Ln7_PRBS_Rx_test_err_counter
Error counter Rx, lane 8	PRBS Rx pattern testing error counter, lane 8	1.1708	Ln8_PRBS_Rx_test_err_counter
Error counter Rx, lane 9	PRBS Rx pattern testing error counter, lane 9	1.1709	Ln9_PRBS_Rx_test_err_counter

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83.7 Protocol implementation conformance statement (PICS) proforma for Clause 83, Physical Medium Attachment (PMA) sublayer, type 40GBASE-R and 100GBASE-R[148]

83.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 83, Physical Medium Attachment (PMA) sublayer, type 40GBASE-R and 100GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the same, can be found in Clause 21.

83.7.2 Identification

83.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

83.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 83, Physical Medium Attachment (PMA) sublayer, type 40GBASE-R and 100GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[148]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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83.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PMA40	PMA for 40GBASE-R	83.1.1		O.1	Yes [ ] No [ ]
*PMA100	PMA for 100GBASE-R	83.1.1		O.1	Yes [ ] No [ ]
LANES_ UPSTREAM	Number of lanes in direction of PCS	83.1.4	Divisor of number of PCS lanes	PMA40:M	4 [ ]
				PMA100: M	4 [ ] 10 [ ] 20 [ ]
LANES_ DOWNSTREAM	Number of lanes in direction of PMD	83.1.4	Divisor of number of PCS lanes	PMA40:M	1 [ ] 4 [ ]
				PMA100: M	4 [ ] 10 [ ] 20 [ ]
RX_CLOCK	Signaling rate of output lanes in Rx direction	83.5.5	LANES_DOWNSTREAM / LANES_UPSTREAM times signaling rate of input lanes in Rx direction	M	Yes [ ]
TX_CLOCK	Signaling rate of output lanes in Tx direction	83.5.5	LANES_UPSTREAM / LANES _DOWNSTREAM times signaling rate of input lanes in Tx direction	M	Yes [ ]
LANE_ MAPPING	Maintain lane mapping while link is in operation	83.5.2	Maintain sequence of PCSLs on all output lanes	M	Yes [ ]
LNKS	PMA link status	83.5.7	Meets the requirements of 83.5.7	M	Yes [ ]
JTP	Supports test-pattern mode	83.5.10		O	Yes [ ] No [ ]
*KRCR	PMA adjacent to the PMD for 40GBASE-KR4, 40GBASE-CR4, 100GBASE-KR4, 100GBASE-CR4, or 100GBASE-CR10	83.5.8		O	Yes [ ] No [ ]
*LBL	PMA local loopback	83.5.8	Supports local loopback	KRCR:M !KRCR:O	Yes [ ] No [ ] N/A[ ]
*LBR	PMA remote loopback	83.5.9	Supports remote loopback	O	Yes [ ] No [ ]
MD	MDIO	83.6	Registers and interface supported	O	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
*USP1SP6	Physically instantiated XLAUI or CAUI-n above (toward PCS)	83.5.3		O	Yes [ ] No [ ]
*DSP1SP6	Physically instantiated XLAUI or CAUI-n below (toward PMD)	83.5.3		O	Yes [ ] No [ ]
*SP2SP5	Physically instantiated PMD service interface	83.5.3		O	Yes [ ] No [ ]
*PPI	PMD service interface instantiated as nPPI	83.5.1, 83.5.5		O	Yes [ ] No [ ]
UNAUI	Electrical and timing requirements of Annex 83A or Annex 83B or Annex 83D or Annex 83E as appropriate met by upstream XLAUI/CAUI-n	83.5.1, 83.5.5		USP1SP6: M	Yes [ ] N/A [ ]
DNAUI	Electrical and timing requirements of Annex 83A or Annex 83B or Annex 83D or Annex 83E as appropriate met by downstream XLAUI/CAUI-n	83.5.1, 83.5.5		DSP1SP6: M	Yes [ ] N/A [ ]
PPIET	Electrical and timing requirements of Annex 86A met by PMD service interface	83.5.1, 83.5.5		PPI:M	Yes [ ] N/A [ ]
DELAY40	Roundtrip delay limit for 40GBASE-R	83.5.4	No more than 4096 BT or 8 pause_quanta	PMA40:M	Yes [ ] N/A [ ]
DELAY100	Roundtrip delay limit for 100GBASE-R	83.5.4	No more than 9216 BT or 18 pause_quanta	PMA100: M	Yes [ ] N/A [ ]
*LPI	Implementation of LPI with the deep sleep mode option	83.3		O	Yes [ ] No [ ]

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83.7.4 Skew generation and tolerance

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Skew generation toward SP1 in Tx direction	83.5.3.2	≤ 29 ns	DSP1SP6:M	Yes [ ] N/A [ ]
S2	Skew variation generation toward SP1 in Tx direction	83.5.3.2	≤ 200 ps	DSP1SP6:M	Yes [ ] N/A [ ]
S3	Skew variation tolerance at SP1	83.5.3.3	Minimum 200 ps	USP1SP6:M	Yes [ ] N/A [ ]
S4	Skew generation toward SP2 in Tx direction	83.5.3.4	≤ 43 ns	SP2SP5:M	Yes [ ] N/A [ ]
S5	Skew variation generation toward SP2 in Tx direction	83.5.3.4	≤ 400 ps	SP2SP5:M	Yes [ ] N/A [ ]
S6	Skew variation tolerance at SP5	83.5.3.5	Minimum 3.6 ns	SP2SP5:M	Yes [ ] N/A [ ]
S7	Skew generation toward SP6 in Rx direction	83.5.3.6	≤ 160 ns	USP1SP6:M	Yes [ ] N/A [ ]
S8	Skew variation generation toward SP6 in Rx direction	83.5.3.6	≤ 3.8 ns	USP1SP6:M	Yes [ ] N/A [ ]
S9	Skew variation tolerance at SP6	83.5.3.7	Minimum 3.8 ns	DSP1SP6:M	Yes [ ] N/A [ ]

83.7.5 Test patterns

Item	Feature	Subclause	Value/Comment	Status	Support
*JTP1	Physically Instantiated XLAUI/CAUI-n between PMA and PMA client	83.5.10		O	Yes [ ] No [ ]
*JTP2	Physically Instantiated XLAUI/CAUI-n between PMA and sublayer below the PMA, or adjacent to PMD whether or not PMD service interface is physically instantiated as nPPI	83.5.10		O	Yes [ ] No [ ]
J1	Send PRBS31 Tx	83.5.10		JTP2:O	Yes [ ] No [ ] N/A [ ]
J2	Send PRBS31 Rx	83.5.10		JTP1:O	Yes [ ] No [ ] N/A [ ]
J3	Check PRBS31 Tx	83.5.10		JTP1:O	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
J4	Check PRBS31 Rx	83.5.10		JTP2:O	Yes [ ] No [ ] N/A [ ]
J5	Send PRBS9 Tx	83.5.10		JTP2:O	Yes [ ] No [ ] N/A [ ]
J6	Send PRBS9 Rx	83.5.10		JTP1:O	Yes [ ] No [ ] N/A [ ]
J7	Send square wave Tx	83.5.10		JTP2:O	Yes [ ] No [ ] N/A [ ]

83.7.6 Loopback modes

Item	Feature	Subclause	Value/Comment	Status	Support
LB1	PMA local loopback implemented	83.5.8	Meets the requirements of 83.5.8	LBL:M	Yes [ ] N/A [ ]
LB2	PMA remote loopback implemented	83.5.9	Meets the requirements of 83.5.9	LBR:M	Yes [ ] N/A [ ]

83.7.7 EEE deep sleep with XLAUI/CAUI

Item	Feature	Subclause	Value/Comment	Status	Support
RXDS	XLAUI/CAUI-n deep sleep Rx direction	83.5.11		LPI*USP1SP6:M or LPI*DSP1SP6:M	Yes [ ] N/A [ ]
TXDS	XLAUI/CAUI-n deep sleep Tx direction	83.5.11		LPI*USP1SP6:M or LPI*DSP1SP6:M	Yes [ ] N/A [ ]

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84. Physical Medium Dependent sublayer and baseband medium, type 40GBASE-KR4

84.1 Overview

This clause specifies the 40GBASE-KR4 PMD. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 84–1, to the medium through the MDI and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 84–1—Physical Layer clauses associated with the 40GBASE-KR4 PMD

Associated clause	40GBASE-KR4
81—RS	Required
81—XLGMII[a]	Optional
82—PCS for 40GBASE-R	Required
74—BASE-R FEC	Optional
83—PMA for 40GBASE-R	Required
83A—XLAUI	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

[a]The XLGMII is an optional interface. However, if the XLGMII is not implemented, a conforming implementation behaves functionally as though the RS and XLGMII were present.

Figure 84–1 shows the relationship of the 40GBASE-KR4 PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model.

40GBASE-KR4 PHYs with the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78).

84.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 40GBASE-KR4 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data. The PMD translates the encoded data to and from signals suitable for the medium.

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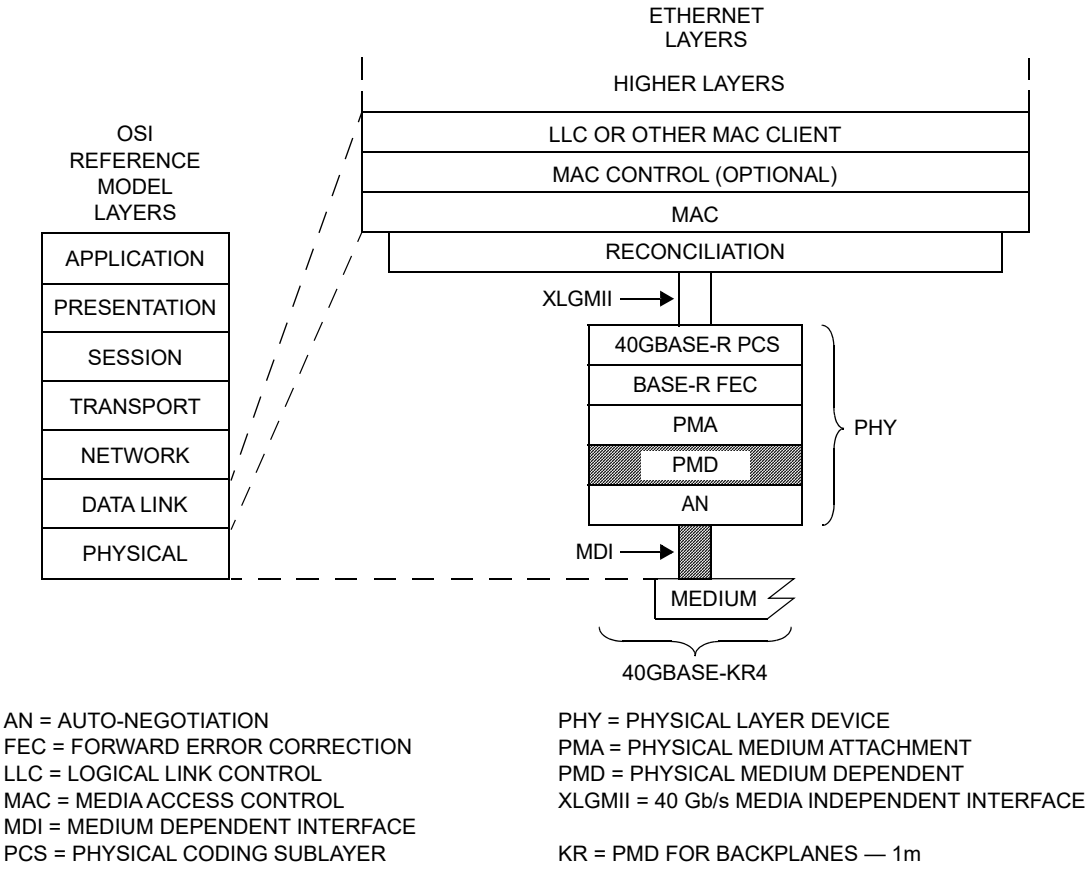

Figure 84–1—40GBASE-KR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The PMD service interface is an instance of the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 40GBASE-KR4 PMD has four parallel bit streams, hence $i = 0$ to 3.

The PMA (or the PMD) continuously sends four parallel bit streams to the PMD (or the PMA), one per lane, each at a nominal signaling rate of 10.3125 GBd.

SIGNAL_DETECT in 40GBASE-KR4 indicates the successful completion of the startup protocol on all four lanes.

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the PMD:IS_UNITDATA_*i*.indication parameters are undefined.

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The SIGNAL_DETECT parameter maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication primitive.

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78, 78.1.3.3.1), then the inter-sublayer service interface includes two additional primitives defined as follows:

PMD:IS_TX_MODE.request(tx_mode)
PMD:IS_RX_MODE.request(rx_mode)

The tx_mode parameter takes on one of up to three values: DATA, QUIET, or ALERT. When tx_mode = QUIET, transmission is disabled; when tx_mode = ALERT, the alert signal is transmitted (see 84.7.2).

The rx_mode parameter is used to communicate the state of the PCS LPI receive function and takes the value QUIET or DATA.

84.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 82.6.)

The 40GBASE-KR4 PHY may be extended using XLAUI as a physical instantiation of the inter-sublayer service interface between devices. If XLAUI is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementer. As examples, the implementer may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

84.4 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the 40GBASE-KR4 PMD, AN, and the medium in one direction shall be no more than 2048 bit times (4 pause_quanta or 51.2 ns). It is assumed that the one way delay through the medium is no more than 320 bit times (8 ns).

A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

84.5 Skew constraints

The Skew (relative delay) between the lanes is kept within limits so that the information on the lanes can be reassembled by the PCS. The Skew Variation is also limited to ensure that a given PCS lane always traverses the same physical lane. Skew and Skew Variation are defined in 80.5 and specified at the points SP1 to SP6 shown in Figure 80–7 and Figure 80–8.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

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If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5.

84.6 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control variables to PMD control variables as shown in Table 84–2, and MDIO status variables to PMD status variables as shown in Table 84–3.

Table 84–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 3	PMD transmit disable register	1.9.4	PMD_transmit_disable_3
PMD transmit disable 2	PMD transmit disable register	1.9.3	PMD_transmit_disable_2
PMD transmit disable 1	PMD transmit disable register	1.9.2	PMD_transmit_disable_1
PMD transmit disable 0	PMD transmit disable register	1.9.1	PMD_transmit_disable_0
Restart training	BASE-R PMD control register	1.150.0	mr_restart_training
Training enable	BASE-R PMD control register	1.150.1	mr_training_enable

Table 84–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 3	PMD receive signal detect register	1.10.4	PMD_signal_detect_3
PMD receive signal detect 2	PMD receive signal detect register	1.10.3	PMD_signal_detect_2
PMD receive signal detect 1	PMD receive signal detect register	1.10.2	PMD_signal_detect_1
PMD receive signal detect 0	PMD receive signal detect register	1.10.1	PMD_signal_detect_0
40GBASE-KR4 deep sleep	EEE capability	1.16.0	—
Receiver status 3	BASE-R PMD status register	1.151.12	rx_trained_3
Frame lock 3	BASE-R PMD status register	1.151.13	frame_lock_3

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Table 84–3—MDIO/PMD status variable mapping *(continued)*

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Startup protocol status 3	BASE-R PMD status register	1.151.14	training_3
Training failure 3	BASE-R PMD status register	1.151.15	training_failure_3
Receiver status 2	BASE-R PMD status register	1.151.8	rx_trained_2
Frame lock 2	BASE-R PMD status register	1.151.9	frame_lock_2
Startup protocol status 2	BASE-R PMD status register	1.151.10	training_2
Training failure 2	BASE-R PMD status register	1.151.11	training_failure_2
Receiver status 1	BASE-R PMD status register	1.151.4	rx_trained_1
Frame lock 1	BASE-R PMD status register	1.151.5	frame_lock_1
Startup protocol status 1	BASE-R PMD status register	1.151.6	training_1
Training failure 1	BASE-R PMD status register	1.151.7	training_failure_1
Receiver status 0	BASE-R PMD status register	1.151.0	rx_trained_0
Frame lock 0	BASE-R PMD status register	1.151.1	frame_lock_0
Startup protocol status 0	BASE-R PMD status register	1.151.2	training_0
Training failure 0	BASE-R PMD status register	1.151.3	training_failure_0

84.7 PMD functional specifications

84.7.1 Link block diagram

The 40GBASE-KR4 PMD uses the same Link block diagram as 10GBASE-KX4, as defined in 71.6.1.

84.7.2 PMD transmit function

The PMD Transmit function shall convert the four bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request into four separate electrical signals. A positive output voltage of SL<p> minus SL<n> (differential voltage) shall correspond to tx_bit = one.

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78), then when tx_mode is set to ALERT, the PMD transmit function shall transmit a repeating 16-bit pattern, hexadecimal 0xFF00, on each lane. This sequence is transmitted regardless of the value of tx_bit presented by the PMD:IS_UNITDATA_i.request primitive. When tx_mode is ALERT, the transmitter equalizer taps shall be set to the preset state specified in 72.6.10.2.3.1. When tx_mode is QUIET, the transmitter shall be disabled as specified in 84.7.6. For all other states of tx_mode, the driver coefficients are restored to their states resolved during training.

84.7.3 PMD receive function

The PMD Receive function shall convert the four electrical signals from the MDI into four bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to

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PMD:IS_UNITDATA_3.indication. A positive input voltage of DL<p> minus DL<n> (differential voltage) shall correspond to rx_bit = one.

84.7.4 Global PMD signal detect function

The Global PMD signal detect function shall continuously report the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT) to the PMD service interface. SIGNAL_DETECT, while normally intended to be an indicator of signal presence, is used by 40GBASE-KR4 to indicate the successful completion of the startup protocol on all lanes. When the PHY supports the optional EEE capability with the deep sleep mode, PMD_SIGNAL.indication is also used to indicate when the ALERT signal is detected, which corresponds to the beginning of a refresh or a wake.

When the PHY does not support the EEE capability or if the PHY supports the EEE capability and rx_mode is set to DATA, SIGNAL_DETECT shall be set to FAIL following system reset or the manual reset of the training state diagram. Upon successful completion of training on all lanes, SIGNAL_DETECT shall be set to OK.

When the PHY does not support the EEE capability or if the PHY supports the EEE capability and rx_mode is set to DATA, if training is disabled by management, SIGNAL_DETECT shall be set to OK. When the PHY supports the EEE capability with the deep sleep mode, SIGNAL_DETECT is set to FAIL following a transition from rx_mode = DATA to rx_mode = QUIET. When rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input that corresponds to an ALERT transmission (see 84.7.2) from the link partner. While rx_mode = QUIET, SIGNAL_DETECT shall be held at FAIL as long as the signal at the receiver input corresponds to a QUIET tx_mode (see 84.7.6) of the link partner.

If the MDIO interface is implemented, then Global_PMD_signal_detect (1.10.0) shall be continuously set to the value of SIGNAL_DETECT as described in 45.2.1.9.7.

84.7.5 PMD lane-by-lane signal detect function

If the MDIO interface is implemented, then PMD_signal_detect_0 (1.10.1), PMD_signal_detect_1 (1.10.2), PMD_signal_detect_2 (1.10.3), and PMD_signal_detect_3 (1.10.4) shall be set to one or zero depending on whether a particular lane's signal_detect, as defined by the training state diagram in Figure 72–5, returns true or false (see 45.2.1.9).

84.7.6 Global PMD transmit disable function

The Global_PMD_transmit_disable function is mandatory if EEE with the deep sleep mode option is supported and is otherwise optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When the Global_PMD_transmit_disable variable is set to one, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage with TX disabled as specified in Table 72–7.
b) If a PMD_fault (84.7.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 84.7.8, shall not be affected by Global_PMD_transmit_disable.
d) For EEE capability, the PMD_transmit_disable function shall turn off the transmitter after tx_mode is set to QUIET within a time and voltage level specified in 72.7.1.4. The PMD_transmit_disable function shall turn on the transmitter after tx_mode is set to DATA or ALERT within the time and voltage level specified in 72.7.1.4.

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If the MDIO interface is implemented, then this function shall map to the Global_PMD_transmit_disable bit as specified in 45.2.1.8.7.

84.7.7 PMD lane-by-lane transmit disable function

The PMD lane-by-lane transmit disable function is optional and allows the electrical transmitter in each lane to be selectively disabled. When this function is supported, it shall meet the following requirements:

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:3) is set to one, this function shall turn off the transmitter associated with that variable such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage with TX disabled as specified in Table 72–7.
b) If a PMD_fault (84.7.9) is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the electrical transmitter in each lane.
c) Loopback, as defined in 84.7.8, shall not be affected by PMD_transmit_disable_*i*.

84.7.8 Loopback mode

Local loopback shall be provided by the adjacent PMA (see 83.5.8) for the 40GBASE-KR4 PMD as a test function to the device. When loopback mode is enabled, transmission requests passed to each transmitter are sent directly to the corresponding receiver, overriding any signal detected by each receiver on its attached link. Note that loopback mode does not affect the state of the transmitter that continues to send data (unless disabled). The method of implementing loopback mode is not defined by this standard.

Control of the loopback function is specified in 45.2.1.1.5.

NOTE 1—The signal paths that are exercised in the loopback mode are implementation specific, but it is recommended that these signal paths encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

84.7.9 PMD_fault function

If the MDIO is implemented, PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault.

84.7.10 PMD transmit fault function

The PMD_transmit_fault function is optional. The faults detected by this function are implementation specific, but should not include the assertion of the Global_PMD_transmit_disable function.

If a PMD_transmit_fault (optional) is detected, then the Global_PMD_transmit_disable function should also be asserted.

If the MDIO interface is implemented, then this function shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

84.7.11 PMD receive fault function

The PMD_receive_fault function is optional. The faults detected by this function are implementation specific.

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If the MDIO interface is implemented, then this function shall contribute to PMA/PMD Receive fault bit as specified in 45.2.1.7.5.

84.7.12 PMD control function

Each lane of the 40GBASE-KR4 PMD shall use the same control function as 10GBASE-KR, as defined in 72.6.10.

The random seed for the training pattern described in 72.6.10.2.6 shall be different for each of the lanes.

The variables rx_trained_*i*, frame_lock_*i*, training_*i,* and training_failure_*i* (where *i* goes from 0 to 3) report status for each lane and are equivalent to rx_trained, frame_lock, training, and training_failure as defined in 72.6.10.3.1.

If the MDIO interface is implemented, then this function shall map these variables to the appropriate bits in the BASE-R PMD status register (register 1.151) as specified in 45.2.1.96.

84.8 40GBASE-KR4 electrical characteristics

84.8.1 Transmitter characteristics

Transmitter electrical characteristics at TP1 for 40GBASE-KR4 shall be the same as 10GBASE-KR, as detailed in 72.7.1.1 through 72.7.1.11.

84.8.1.1 Test fixture

The test fixture defined for 10GBASE-KR in 72.7.1.1 shall be used on all lanes.

84.8.2 Receiver characteristics

Receiver electrical characteristics at TP4 for 40GBASE-KR4 shall be the same as 10GBASE-KR, as detailed in 72.7.2.1 through 72.7.2.5.

84.8.2.1 Receiver interference tolerance

The receiver interference tolerance tests shall be the same as those described for 10GBASE-KR in 72.7.2.1 and Annex 69A.

For 40GBASE-KR4, each lane shall be tested individually using the methodology defined in Annex 69A with the transmitters of the unused lanes active and terminated by the reference impedance.

84.9 Interconnect characteristics

Informative interconnect characteristics for 40GBASE-KR4 are provided in Annex 69B.

84.10 Environmental specifications

84.10.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

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84.10.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

84.10.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

84.10.4 Electromagnetic compatibility

A system integrating the 40GBASE-KR4 PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

84.10.5 Temperature and humidity

A system integrating the 40GBASE-KR4 PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

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84.11 Protocol implementation conformance statement (PICS) proforma for Clause 84, Physical Medium Dependent sublayer and baseband medium, type 40GBASE-KR4[149]

84.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 84, Physical Medium Dependent sublayer and baseband medium, type 40GBASE-KR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

84.11.2 Identification

84.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

84.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 84, Physical Medium Dependent sublayer and baseband medium, type 40GBASE-KR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[149]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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84.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XGE	XLGMII	84.1	Interface is supported	O	Yes [ ] No [ ]
PCS	Support of 40GBASE-R PCS	84.1		M	Yes [ ]
PMA	Support of 40GBASE-R PMA	84.1		M	Yes [ ]
XLAUI	XLAUI	84.1	Interface is supported	O	Yes [ ] No [ ]
AN	Auto-Negotiation	84.1	Device implements Auto-Negotiation	M	Yes [ ]
FEC	Forward error correction	84.1	Device implements BASE-R forward error correction	O	Yes [ ] No [ ]
DC	Delay constraints	84.4	Device conforms to delay constraints	M	Yes [ ]
DSC	Skew constraints	84.5	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO interface	84.6	Device implements MDIO	O	Yes [ ] No [ ]
*TD	Global_PMD_transmit_disable	84.7.6		O	Yes [ ] No [ ]
*LPI	Implementation of LPI with the deep sleep mode option	84.1		O	Yes [ ] No [ ]

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84.11.4 PICS proforma tables for Clause 84, Physical Medium Dependent (PMD) sublayer and baseband medium, type 40GBASE-KR4

84.11.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Transmit function	84.7.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FS2	Transmitter signal	84.7.2	A positive differential voltage corresponds to tx_bit = one	M	Yes [ ]
FS3	Receive function	84.7.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FS4	Receiver signal	84.7.3	A positive differential voltage corresponds to rx_bit = one	M	Yes [ ]
FS5	Signal detect	84.7.4	Report to PMD service interface	M	Yes [ ]
FS6	SIGNAL_DETECT value	84.7.4	Set to FAIL on reset	M	Yes [ ]
FS7	SIGNAL_DETECT value	84.7.4	Set to OK when training completes successfully	M	Yes [ ]
FS8	SIGNAL_DETECT value	84.7.4	Set to OK when training disabled	M	Yes [ ]
FS9	Transmit disable requirements	84.7.6	Requirements of 84.7.6 and 84.7.7	TD:M	Yes [ ] N/A[ ]
FS10	Loopback support	84.7.8	Provided for 40GBASE-KR4 PMD by transmitter and receiver	M	Yes [ ]
FS11	Control function	84.7.12	The same control function as 10GBASE-KR is used	M	Yes [ ]
FS12	Random seed	84.7.12	The random seed shall be different for each lane	M	Yes [ ]
FS13	Transmit function for EEE	84.7.2	Transmitter behavior during ALERT and QUIET	LPI:M	Yes [ ] N/A[ ]
FS14	Signal detect function for EEE	84.7.4		LPI:M	Yes [ ] N/A[ ]
FS15	Transmit disable during LPI	84.7.6	Disable transmitter during tx_mode = QUIET	LPI:M	Yes [ ] N/A[ ]

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84.11.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	MDIO Variable Mapping	84.6	Per Table 84–2, and Table 84–3	MD:M	Yes [ ] N/A [ ]
MF2	Global signal detect	84.7.4	Value described in 45.2.1.9.7	MD:M	Yes [ ] N/A [ ]
MF3	Lane-by-lane signal detect	84.7.5	Value as described in 84.7.5	MD:M	Yes [ ] N/A [ ]
MF4	PMD_transmit_fault function	84.7.10	Sets PMD_transmit_fault as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
MF5	PMD_receive_fault function	84.7.11	Sets PMD_receive_fault as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]
MF6	PMD training status	84.7.12	Sets training status as specified in 45.2.1.96	MD:M	Yes [ ] N/A [ ]

84.11.4.3 Transmitter electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Transmitter characteristics	84.8.1	The same transmitter characteristics as 10GBASE-KR are used	M	Yes [ ]
TC2	Test fixture	84.8.1.1	The same test fixture as 10GBASE-KR is used	M	Yes [ ]
TC3	Output Amplitude LPI voltage	84.7.6	Less than 30 mV within 500 ns of tx_quiet	LPI:M	Yes [ ] N/A[ ]
TC4	Output Amplitude ON voltage	84.7.6	Greater than 90% of previous level within 500 ns of tx_quiet deasserted	LPI:M	Yes [ ] N/A[ ]

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84.11.4.4 Receiver electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Receiver characteristics	84.8.2	The same receiver characteristics as 10GBASE-KR are used	M	Yes [ ]
RC2	Receiver interference tolerance	84.8.2.1	The same receiver interference tolerance test as 10GBASE-KR is used	M	Yes [ ]
RC3	Receiver interference tolerance testing	84.8.2.1	Each lane shall be tested individually using the methodology defined in Annex 69A with the transmitters of the unused lanes active and terminated by the reference impedance	M	Yes [ ]

84.11.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	84.10.1	Conforms to J.2	M	Yes [ ]
ES2	Electromagnetic interference	84.10.4	Complies with applicable local and national codes	M	Yes [ ]

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85. Physical Medium Dependent sublayer and baseband medium, type 40GBASE-CR4 and 100GBASE-CR10

85.1 Overview

This clause specifies the 40GBASE-CR4 PMD and the 100GBASE-CR10 PMD (including MDI) and the baseband medium. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 85–1, to the medium through the MDI and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 85–1—Physical Layer clauses associated with the 40GBASE-CR4 and 100GBASE-CR10 PMDs

Associated clause	40GBASE-CR4	100GBASE-CR10
81—RS	Required	Required
81—XLGMII[a]	Optional	Not applicable
81—CGMII[b]	Not applicable	Optional
82—PCS for 40GBASE-R	Required	Not applicable
82—PCS for 100GBASE-R	Not applicable	Required
74—BASE-R FEC	Optional	Optional
83—PMA for 40GBASE-R	Required	Not applicable
83—PMA for 100GBASE-R	Not applicable	Required
83A—XLAUI	Optional	Not applicable
83A—CAUI-10	Not applicable	Optional
83D—CAUI-4	Not applicable	Optional
73—Auto-Negotiation	Required	Required
78—Energy Efficient Ethernet	Optional	Optional

[a]The XLGMII is an optional interface. However, if the XLGMII is not implemented, a conforming implementation behaves functionally as though the RS and XLGMII were present.
[b]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation behaves functionally as though the RS and CGMII were present.

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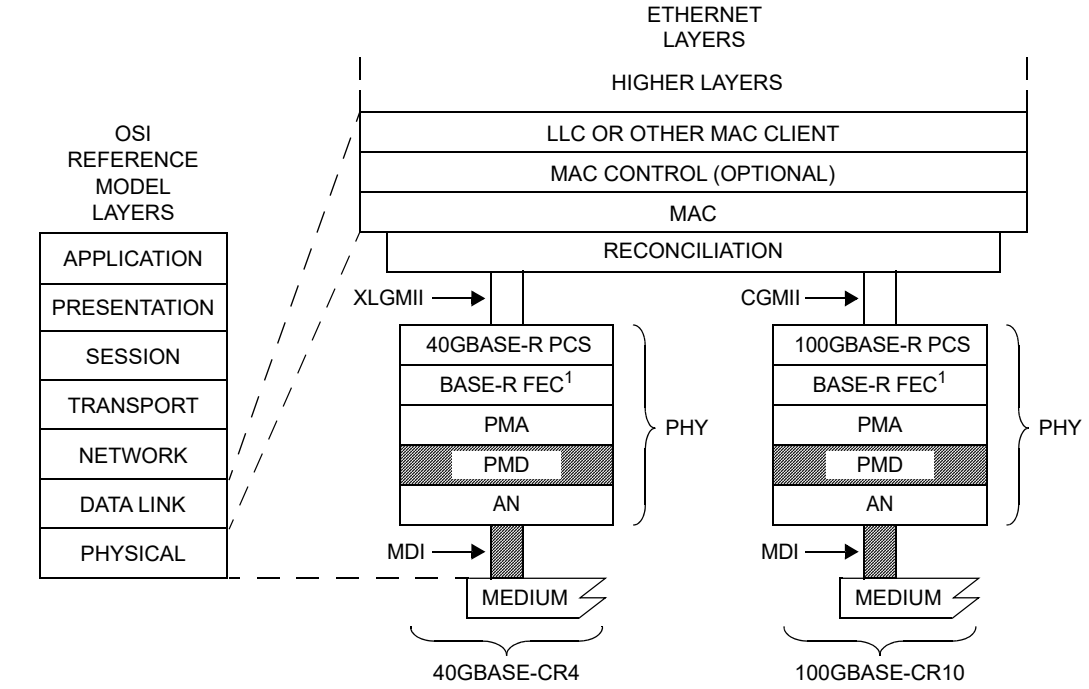
Figure 85–1 shows the relationship of the 40GBASE-CR4 and 100GBASE-CR10 PMD sublayers and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.



AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

CR = PMD FOR COPPER — 7 m
NOTE 1—OPTIONAL

Figure 85–1—40GBASE-CR4 and 100GBASE-CR10 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

100GBASE-CR10 and 40GBASE-CR4 PHYs with the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78).

85.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 40GBASE-CR4 and 100GBASE-CR10 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA and PMD entities. The PMD translates the encoded data to and from signals suitable for the specified medium.The PMD service interface is an instance of the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

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The 40GBASE-CR4 PMD has four parallel bit streams, hence *i* = 0 to 3 for 40GBASE-CR4, and the 100GBASE-CR10 PMD has ten parallel bit streams, hence *i* = 0 to 9 for 100GBASE-CR10. The PMA (or the PMD) continuously sends four or ten parallel bit streams to the PMD (or the PMA), one per lane, each at a nominal signaling rate of 10.3125 GBd.

For 40GBASE-CR4, SIGNAL_DETECT indicates the successful completion of the startup protocol on all four lanes. For 100GBASE-CR10, SIGNAL_DETECT indicates the successful completion of the startup protocol on all ten lanes.

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the PMD:IS_UNITDATA_*i*.indication parameters are undefined.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication primitive.

If the optional EEE capability with the deep sleep mode option is supported (see 78.1.3.3.1) then the inter-sublayer service interface includes two additional primitives defined as follows:

PMD:IS_TX_MODE.request(tx_mode)
PMD:IS_RX_MODE.request(rx_mode)

The tx_mode parameter takes on one of up to three values: DATA, QUIET, or ALERT. When tx_mode = QUIET, transmission is disabled; when tx_mode = ALERT, the alert signal is transmitted (see 85.7.2).

The rx_mode parameter is used to communicate the state of the PCS LPI receive function and takes the value QUIET or DATA.

85.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 82.6.)

The 40GBASE-CR4 PHY may be extended using XLAUI, a physical instantiation of the inter-sublayer service interface between devices. Similarly, the 100GBASE-CR10 PHY may be extended using CAUI-n. If XLAUI or CAUI-n is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementer. As examples, the implementer may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

85.4 Delay constraints

A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

The sum of the transmit and the receive delays at one end of the link contributed by the 40GBASE-CR4 PMD and AN shall be no more than 4096 bit times (8 pause_quanta or 102.4 ns). The delay through the medium is not included.

The sum of the transmit and the receive delays at one end of the link contributed by the 100GBASE-CR10 PMD and AN shall be no more than 9728 bit times (19 pause_quanta or 97.28 ns). The delay through the medium is not included.

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85.5 Skew constraints

The Skew (relative delay) between the lanes is kept within limits so that the information on the lanes can be reassembled by the PCS. The Skew Variation is also limited to ensure that a given PCS lane always traverses the same physical lane. Skew and Skew Variation are defined in 80.5 and are specified at the points SP1 to SP6 shown in Figure 80–7 and Figure 80–8.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns. For more information on Skew and Skew Variation, see 80.5.

85.6 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. Mapping of MDIO control variables to PMD control variables is illustrated in Table 85–2 for 40GBASE-CR4 and 100GBASE-CR10. Mapping of MDIO status variables to PMD status variables is illustrated in Table 85–3 for 40GBASE-CR4 and 100GBASE-CR10.

Table 85–2—40GBASE-CR4 and 100GBASE-CR10 MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 9 to PMD transmit disable 0	PMD transmit disable register	1.9.10 to 1.9.1	PMD_transmit_disable_9 to PMD_transmit_disable_0
Restart training	BASE-R PMD control register	1.150.0	mr_restart_training
Training enable	BASE-R PMD control register	1.150.1	mr_training_enable

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Table 85–3—40GBASE-CR4 and 100GBASE-CR10 MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 9 to PMD receive signal detect 0	PMD receive signal detect register	1.10.10 to 1.10.1	PMD_signal_detect_9 to PMD_signal_detect_0
40GBASE-CR4 deep sleep	EEE capability	1.16.1	—
100GBASE-CR10 deep sleep	EEE capability	1.16.8	—
Receiver status 9	BASE-R PMD status 3 register	1.157.4	rx_trained_9
Frame lock 9	BASE-R PMD status 3 register	1.157.5	frame_lock_9
Startup protocol status 9	BASE-R PMD status 3 register	1.157.6	training_9
Training failure 9	BASE-R PMD status 3 register	1.157.7	training_failure_9
Receiver status 8	BASE-R PMD status 3 register	1.157.0	rx_trained_8
Frame lock 8	BASE-R PMD status 3 register	1.157.1	frame_lock_8
Startup protocol status 8	BASE-R PMD status 3 register	1.157.2	training_8
Training failure 8	BASE-R PMD status 3 register	1.157.3	training_failure_8
Receiver status 7	BASE-R PMD status 2 register	1.156.12	rx_trained_7
Frame lock 7	BASE-R PMD status 2 register	1.156.13	frame_lock_7
Startup protocol status 7	BASE-R PMD status 2 register	1.156.14	training_7
Training failure 7	BASE-R PMD status 2 register	1.156.15	training_failure_7
Receiver status 6	BASE-R PMD status 2 register	1.156.8	rx_trained_6
Frame lock 6	BASE-R PMD status 2 register	1.156.9	frame_lock_6
Startup protocol status 6	BASE-R PMD status 2 register	1.156.10	training_6
Training failure 6	BASE-R PMD status 2 register	1.156.11	training_failure_6
Receiver status 5	BASE-R PMD status 2 register	1.156.4	rx_trained_5
Frame lock 5	BASE-R PMD status 2 register	1.156.5	frame_lock_5
Startup protocol status 5	BASE-R PMD status 2 register	1.156.6	training_5
Training failure 5	BASE-R PMD status 2 register	1.156.7	training_failure_5
Receiver status 4	BASE-R PMD status 2 register	1.156.0	rx_trained_4
Frame lock 4	BASE-R PMD status 2 register	1.156.1	frame_lock_4
Startup protocol status 4	BASE-R PMD status 2 register	1.156.2	training_4
Training failure 4	BASE-R PMD status 2 register	1.156.3	training_failure_4

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Table 85–3—40GBASE-CR4 and 100GBASE-CR10 MDIO/PMD status variable mapping *(continued)*

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Receiver status 3	BASE-R PMD status register	1.151.12	rx_trained_3
Frame lock 3	BASE-R PMD status register	1.151.13	frame_lock_3
Startup protocol status 3	BASE-R PMD status register	1.151.14	training_3
Training failure 3	BASE-R PMD status register	1.151.15	training_failure_3
Receiver status 2	BASE-R PMD status register	1.151.8	rx_trained_2
Frame lock 2	BASE-R PMD status register	1.151.9	frame_lock_2
Startup protocol status 2	BASE-R PMD status register	1.151.10	training_2
Training failure 2	BASE-R PMD status register	1.151.11	training_failure_2
Receiver status 1	BASE-R PMD status register	1.151.4	rx_trained_1
Frame lock 1	BASE-R PMD status register	1.151.5	frame_lock_1
Startup protocol status 1	BASE-R PMD status register	1.151.6	training_1
Training failure 1	BASE-R PMD status register	1.151.7	training_failure_1
Receiver status 0	BASE-R PMD status register	1.151.0	rx_trained_0
Frame lock 0	BASE-R PMD status register	1.151.1	frame_lock_0
Startup protocol status 0	BASE-R PMD status register	1.151.2	training_0
Training failure 0	BASE-R PMD status register	1.151.3	training_failure_0

85.7 PMD functional specifications

85.7.1 Link block diagram

A 40GBASE-CR4 or 100GBASE-CR10 link in one direction is illustrated in Figure 85–2. For purposes of system conformance, the PMD sublayer is standardized at the test points described in this subclause. The electrical transmit signal is defined at TP2. Unless specified otherwise, all transmitter measurements and tests defined in Table 85–5 are made at TP2 utilizing the test fixture specified in 85.8.3.5. Unless specified otherwise, all receiver measurements and tests defined in 85.8.4 are made at TP3 utilizing the test fixture specified in 85.8.3.5. A mated connector pair has been included in both the transmitter and receiver specifications defined in 85.8.3 and 85.8.4. The maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 85.8.3.4.

The 40GBASE-CR4 and 100GBASE-CR10 channels are defined between the transmitter (TP0) and receiver blocks (TP5) to include the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss as illustrated in Figure 85–2. Annex 85A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system. All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 85–2. The cable assembly test fixture of Figure 85–14 or its functional equivalent, is required for measuring the cable assembly specifications in 85.10 at TP1 and TP4. Two mated connector pairs and the cable assembly test fixture have been included in the cable assembly specifications defined in 85.10.

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Transmitter and receiver differential controlled impedance printed circuit board insertion losses defined between TP0–TP1 and TP4–TP5 respectively are provided informatively in Annex 85A.

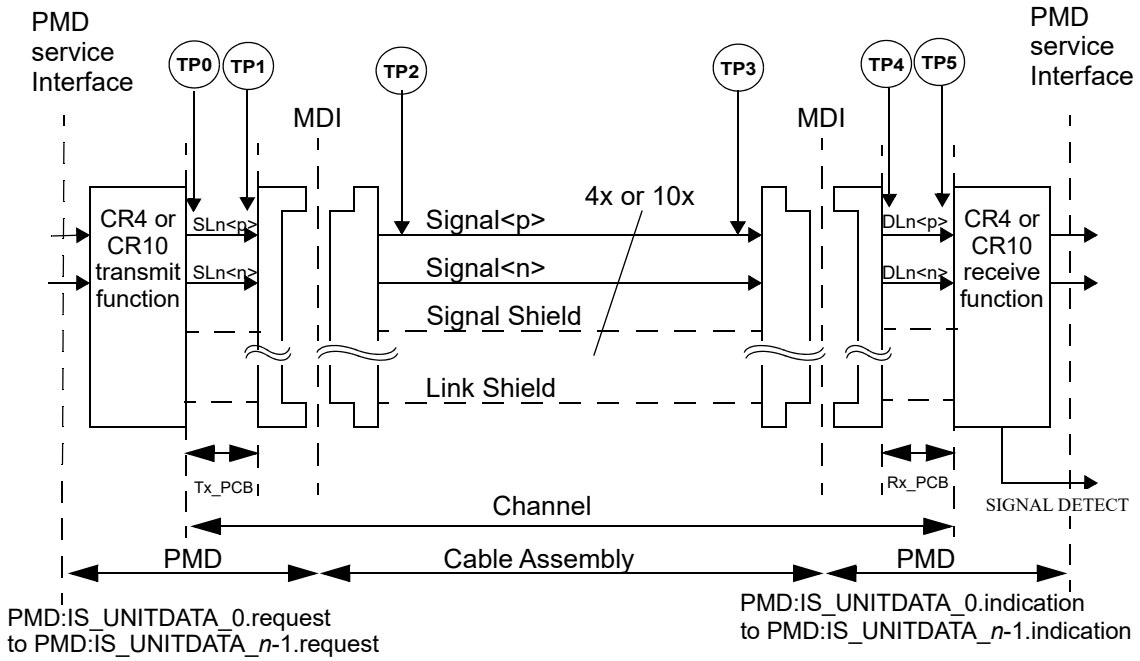

Figure 85–2—40GBASE-CR4 or 100GBASE-CR10 link (half link is illustrated)

Note that the source lanes (SL), signals SLn<p>, and SLn<n> are the positive and negative sides of the transmitters differential signal pairs and the destination lanes (DL) signals, DLn<p>, and DLn<n> are the positive and negative sides of the receivers differential signal pairs for lane n (n = 0, 1, 2, 3 or n = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9).

Table 85–4 describes the defined test points illustrated in Figure 85–2.

Table 85–4—40GBASE-CR4 and 100GBASE-CR10 test points

Test points	Description
TP0 to TP5	The 40GBASE-CR4 and 100GBASE-CR10 channels including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 85–2. The cable assembly test fixture of Figure 85–14 or its functional equivalent, is required for measuring the cable assembly specifications in 85.10 at TP1 and TP4.
TP0 to TP1 TP4 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 85.8.3 and 85.8.4. The maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 85.8.3.4.
TP2	Unless specified otherwise, all transmitter measurements and tests defined in Table 85–5 are made at TP2 utilizing the test fixture specified in 85.8.3.5.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 85.8.4 are made at TP3 utilizing the test fixture specified in 85.8.3.5.

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85.7.2 PMD Transmit function

The 40GBASE-CR4 PMD Transmit function shall convert the four bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request into four separate electrical signals. The four electrical signals shall then be delivered to the MDI, all according to the transmit electrical specifications in 85.8.3. A positive output voltage of SL<p> minus SL<n> (differential voltage) shall correspond to tx_bit = one. The 100GBASE-CR10 PMD Transmit function shall convert the ten bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_9.request into ten separate electrical signals. The ten electrical signals shall then be delivered to the MDI, all according to the transmit electrical specifications in 85.8.3. A positive output voltage of SL<p> minus SL<n> (differential voltage) shall correspond to tx_bit = one.

If the EEE capability with the deep sleep mode option is supported (see Clause 78) then when tx_mode is set to ALERT, the PMD transmit function shall transmit a repeating 16-bit pattern, hexadecimal 0xFF00, on each lane. This sequence is transmitted regardless of the value of tx_bit presented by the PMD:IS_UNITDATA_i.request primitive. When tx_mode is ALERT, the transmitter equalizer taps are set to the preset state specified in 72.6.10.2.3.1. When tx_mode is QUIET, the transmitter is disabled as specified in 85.7.6. For all other states of tx_mode, the driver coefficients are restored to their states resolved during training.

85.7.3 PMD Receive function

The 40GBASE-CR4 PMD Receive function shall convert the four electrical signals from the MDI into four bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication. A positive input voltage of DL<p> minus DL<n> (differential voltage) shall correspond to rx_bit = one. The 100GBASE-CR10 PMD Receive function shall convert the ten electrical signals from the MDI into ten bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_9.indication. A positive input voltage of DL<p> minus DL<n> (differential voltage) shall correspond to rx_bit = one.

85.7.4 Global PMD signal detect function

The Global PMD signal detect function shall continuously report the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT) to the PMD service interface. SIGNAL_DETECT, while normally intended to be an indicator of signal presence, is used by 40GBASE-CR4 and 100GBASE-CR10 to indicate the successful completion of the startup protocol on all lanes. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication primitive. When the PHY supports the optional EEE capability with deep sleep mode, PMD_SIGNAL.indication is also used to indicate when the ALERT signal is detected, which corresponds to the beginning of a refresh or a wake.

When the PHY does not support the EEE capability or if the PHY supports the EEE capability and rx_mode is set to DATA, SIGNAL_DETECT shall be set to FAIL following system reset or the manual reset of the training state diagram. Upon successful completion of training on all lanes, SIGNAL_DETECT shall be set to OK.

When the PHY does not support the EEE capability or if the PHY supports the EEE capability and rx_mode is set to DATA, if training is disabled by management, SIGNAL_DETECT shall be set to OK. When the PHY supports the EEE capability with deep sleep mode, SIGNAL_DETECT is set to FAIL following a transition from rx_mode = DATA to rx_mode = QUIET. When rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input that corresponds to an ALERT transmission (see 85.7.2) from the link partner. While rx_mode = QUIET, SIGNAL_DETECT shall be held at FAIL as long as the signal at the receiver input corresponds to a QUIET tx_mode (see 85.7.6) of the link partner.

If the MDIO interface is implemented, then Global_PMD_signal_detect (1.10.0) shall be continuously set to the value of SIGNAL_DETECT as described in 45.2.1.9.7.

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85.7.5 PMD lane-by-lane signal detect function

When the MDIO is implemented, each PMD_signal_detect_*i* value, where *i* represents the lane number in the range 0:3 for 40GBASE-CR4 and 0:9 for 100GBASE-CR10, shall be continuously updated as described in the following two paragraphs.

For 40GBASE-CR4 PMD_signal_detect_0 (1.10.1), PMD_signal_detect_1 (1.10.2), PMD_signal_detect_2 (1.10.3) and PMD_signal_detect_3 (1.10.4) shall be set to one or zero depending on whether a particular lane's signal_detect, as defined by the training state diagram in Figure 72–5, returns true or false.

For 100GBASE-CR10 PMD_signal_detect_0 (1.10.1), PMD_signal_detect_1 (1.10.2), PMD_signal_detect_2 (1.10.3), PMD_signal_detect_3 (1.10.4), PMD_signal_detect_4 (1.10.5), PMD_signal_detect_5 (1.10.6), PMD_signal_detect_6 (1.10.7), PMD_signal_detect_7 (1.10.8), PMD_signal_detect_8 (1.10.9), and PMD_signal_detect_9 (1.10.10) shall be set to one or zero depending on whether a particular lane's signal_detect, as defined by the training state diagram in Figure 72–5, returns true or false.

85.7.6 Global PMD transmit disable function

The Global_PMD_transmit_disable function is mandatory if EEE with the deep sleep mode option is supported and is otherwise optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When Global_PMD_transmit_disable variable is set to one, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage in Table 85–5.
b) If a PMD_fault (85.7.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 85.7.8, shall not be affected by Global_PMD_transmit_disable.
d) For EEE capability, the PMD_transmit_disable function shall turn off the transmitter after tx_mode is set to QUIET within a time and voltage level specified in 72.7.1.4. The PMD_transmit_disable function shall turn on the transmitter after tx_mode is set to DATA or ALERT within the time and voltage level specified in 72.7.1.4.

85.7.7 PMD lane-by-lane transmit disable function

The PMD lane-by-lane transmit disable function is optional and allows the electrical transmitter in each lane to be selectively disabled. When this function is supported, it shall meet the following requirements:

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:3 or 0:9) is set to one, this function shall turn off the transmitter associated with that variable such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 85–5.
b) If a PMD_fault (85.7.9) is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the electrical transmitter in each lane.
c) Loopback, as defined in 85.7.8, shall not be affected by PMD_transmit_disable_*i*.

85.7.8 Loopback mode

Local loopback mode shall be provided by the adjacent PMA (see 83.5.8) for the 40GBASE-CR4 and 100GBASE-CR10 PMDs as a test function to the device. When loopback mode is enabled, transmission requests passed to each transmitter are sent directly to the corresponding receiver, overriding any signal detected by each receiver on its attached link. Note that loopback mode does not affect the state of the transmitter, which continues to send data (unless disabled).

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Control of the loopback function is specified in 45.2.1.1.5.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

85.7.9 PMD_fault function

If the MDIO is implemented, PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault. The PMD fault function shall be mapped to bit 1.1.7 as listed in Table 85–3.

85.7.10 PMD transmit fault function

The PMD_transmit_fault function is optional. The faults detected by this function are implementation specific, but should not include the assertion of the Global_PMD_transmit_disable function.

If a PMD_transmit_fault (optional) is detected, then the Global_PMD_transmit_disable function should also be asserted.

If the MDIO interface is implemented, then this function shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

85.7.11 PMD receive fault function

The PMD_receive_fault function is optional. The faults detected by this function are implementation specific.

If the MDIO interface is implemented, then this function shall contribute to the Receive fault bit as specified in 45.2.1.7.5.

85.7.12 PMD control function

Each lane of the 40GBASE-CR4 or 100GBASE-CR10 PMD shall use the same control function as 10GBASE-KR, as defined in 72.6.10.

The random seed for the training pattern described in 72.6.10.2.6 shall be different for each of the lanes.

85.8 MDI Electrical specifications for 40GBASE-CR4 and 100GBASE-CR10

85.8.1 Signal levels

The 40GBASE-CR4 and 100GBASE-CR10 MDI is a low-swing AC-coupled differential interface. AC-coupling at the receiver, as defined in 85.8.4.5, allows for interoperability between components operating from different supply voltages. Low-swing differential signaling provides noise immunity and improved electromagnetic interference (EMI).

85.8.2 Signal paths

The 40GBASE-CR4 and 100GBASE-CR10 MDI signal paths are point-to-point connections. Each path corresponds to a 40GBASE-CR4 or 100GBASE-CR10 MDI lane and comprises two complementary

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signals, which form a balanced differential pair. For 40GBASE-CR4, there are four differential paths in each direction for a total of eight pairs, or sixteen connections. For 100GBASE-CR10, there are ten differential paths in each direction for a total of 20 pairs, or forty connections. The signal paths are intended to operate on twinaxial cable assemblies ranging from 0.5 m to 7 m in length, as described in 85.10.

85.8.3 Transmitter characteristics

Transmitter characteristics shall meet specifications summarized in Table 85–5 at TP2 unless otherwise noted. The transmitter specifications at TP0 are provided informatively in Annex 85A, Table 85A–1.

Table 85–5—Transmitter characteristics at TP2 summary

Parameter	Subclause reference	Value	Units
Signaling rate, per lane	85.8.3.9	10.3125 ± 100 ppm	GBd
Unit interval nominal	85.8.3.9	96.969697	ps
Differential peak-to-peak output voltage (max) with Tx disabled		30	mV
Common-mode voltage limits	72.7.1.4	0 to 1.9	V
Differential output return loss (min)	85.8.3.1	See Equation (85–1)	dB
AC common-mode output voltage (max., RMS)		30	mV
Common-mode voltage deviation (max) during LPI	72.7.1.4	150	mV
Amplitude peak-to-peak (max)	72.7.1.4	1200[a]	mV
Transmitter DC amplitude[b]	85.8.3.3	0.34 min, 0.6 max	V
Linear fit pulse (min)[c]	85.8.3.3	0.63 × Transmitter DC amplitude	V
Transmitted waveform max RMS normalized error (linear fit), "*e*" abs coefficient step size minimum precursor fullscale range minimum post cursor fullscale range	 85.8.3.3 85.8.3.3.2 85.8.3.3.3 85.8.3.3.3	 0.037 0.0083 min, 0.05 max 1.54 4	
Far-end transmit output noise (max) Low insertion loss channel High insertion loss channel	85.8.3.2	 2 See Equation (85–2) 1 See Equation (85–3)	mV
Max output jitter (peak-to-peak) Random jitter[d] Duty Cycle Distortion[e] Total jitter excluding data dependent jitter[f]		 0.15 0.035 0.25	 UI UI UI

[a]The 40GBASE-CR4 Style-1 connector may support 40GBASE-CR4 or XLPPI interfaces. For implementations that support both interfaces, the transmitter should not exceed the XLPPI voltage maximum until a 40GBASE-CR4 cable assembly has been identified. The 100GBASE-CR10 connector may support 100GBASE-CR10 or CPPI interfaces. For implementations that support both interfaces, the transmitter should not exceed the CPPI voltage maximum until a 100GBASE-CR10 cable assembly has been identified.
[b]The transmitter DC amplitude is the sum of linear fit pulse response $p(k)$ from step 3) divided by M from step 3).
[c]The peak of the linear fit pulse response $p(k)$ from step 3).
[d]Random jitter is specified at a BER of 10^{-12}
[e] See 72.7.1.9 for duty cycle distortion definition.
[f]Total jitter at a BER of 10^{-12} measured per 83A.5.1 excluding data dependent jitter (DDJ). DDJ is a jitter component where jitter that is not correlated to the data pattern has been removed. DDJ is measured with PRBS9 as specified in 83.5.10.

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85.8.3.1 Transmitter differential output return loss

The differential output return loss, in dB, of the transmitter shall meet Equation (85–1). This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 12 - 2\sqrt{f} & 0.05 \leq f < 4.11 \\ 6.3 - 13\log_{10}(f/5.5) & 4.11 \leq f \leq 10 \end{array} \right\} \quad \text{(dB)} \qquad (85\text{–}1)$$

where

f is the frequency in GHz
$Return\_loss(f)$ is the return loss at frequency f

The transmitter differential output return loss is illustrated in Figure 85–3.

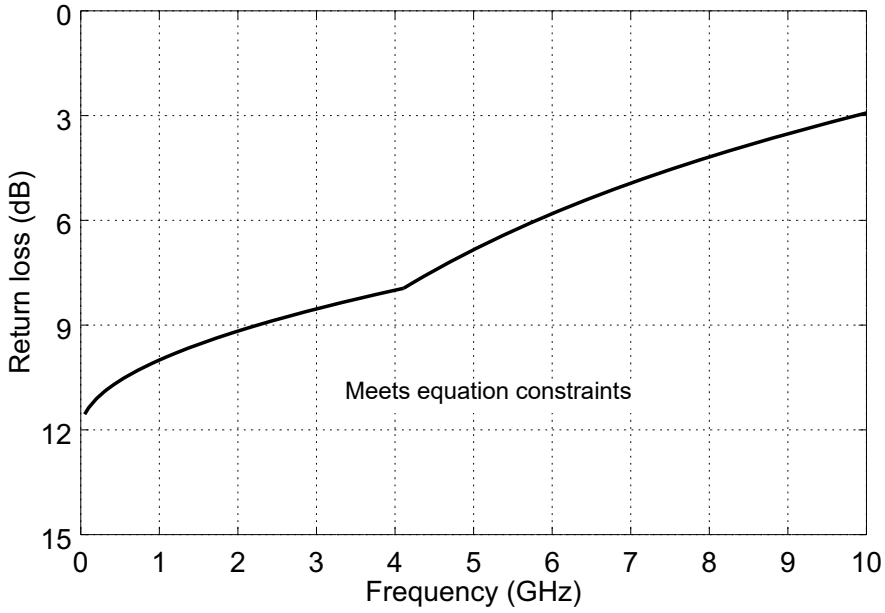

Figure 85–3—Transmitter differential output return loss

85.8.3.2 Transmitter noise parameter measurements

The far-end transmitter output noise is an additional source of noise to the cable assembly's integrated crosstalk noise (ICN) specified in 85.10.7. The far-end transmitter output noise parameter is characterized using two reference channels; a "low-loss" cable assembly with insertion loss on the reference pair of 6 dB ± 1.5 dB at 5.15625 GHz and cable assembly integrated crosstalk noise (ICN) meeting the requirements of 85.10.7 and a "high-loss" cable assembly with insertion loss on the reference pair of 15.7 dB ± 1.5 dB at 5.15625 GHz and cable assembly ICN meeting the requirements of 85.10.7. The far-end transmitter output noise is characterized as a deviation from the cable assembly ICN using the following procedure:

1) Compute the far-end integrated crosstalk noise σ_{fx} into the reference lane of the cable assembly using the methodology of 85.10.7 and the parameters in Table 85–11.
2) Denote σ_l as the far-end ICN for the low-loss cable assembly.

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3) Denote σ_h as the far-end ICN for the high-loss cable assembly.
4) The transmitter under test is connected to one end of the reference cable assembly and the other end is connected to the cable assembly test fixture specified in 85.10.8.
5) All lanes of the cable assembly test fixture are terminated in the reference impedance with the reference lane connected to the measuring instrument.
6) The reference lane of the transmitter under test sends a square wave test pattern as specified in 83.5.10 while all other adjacent transmitter lanes send either scrambled idle or PRBS31.
7) A fixed point on the square wave test pattern is chosen and the RMS deviation from the mean voltage at this observation point is measured. The histogram for RMS noise measurement is 1 UI wide.
8) The measurement should not include the measurement system noise.

For the low-loss cable assembly, the measured RMS deviation from the cable assembly ICN due to the far-end transmitter output noise shall meet the values determined using Equation (85–2).

$$RMSl_{dev} \leq \sqrt{\sigma_l^{\,2} + 2^2} \text{ (mV)} \tag{85–2}$$

For the high-loss cable assembly, the measured RMS deviation from the cable assembly ICN due to the far-end transmitter output noise shall meet the values determined using Equation (85–3).

$$RMSh_{dev} \leq \sqrt{\sigma_h^{\,2} + 1^2} \text{ (mV)} \tag{85–3}$$

85.8.3.3 Transmitter output waveform

The 40GBASE-CR4 and 100GBASE-CR10 transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in Figure 85–4.

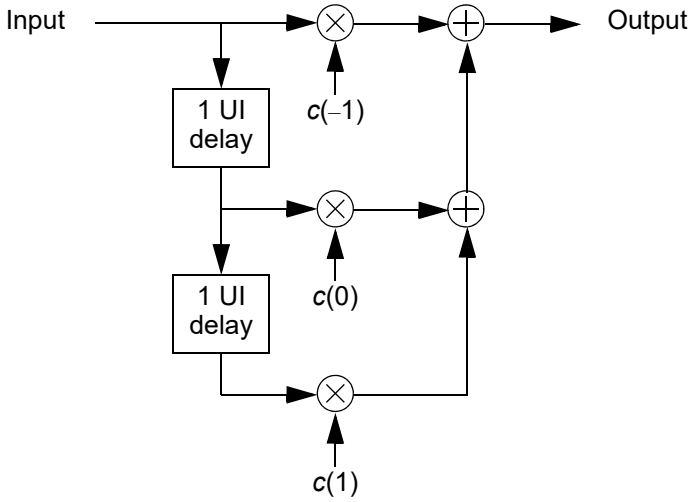

Figure 85–4—Transmit equalizer functional model

The state of the transmit equalizer and hence the transmitted output waveform may be manipulated via the PMD control function defined in 85.7.12 or via the management interface. The transmit function responds to a set of commands issued by the link partner's receive function and conveyed by a back-channel communications path.

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This command set includes instructions to

a) Increment coefficient $c(i)$.
b) Decrement coefficient $c(i)$.
c) Hold coefficient $c(i)$ at its current value.
d) Set the coefficients to a pre-defined value (preset or initialize).

In response, the transmit function relays status information to the link partner's receive function. The status messages indicate that

a1) The requested update to coefficient $c(i)$ has completed (updated).
b1) Coefficient $c(i)$ is at its minimum value.
c1) Coefficient $c(i)$ is at its maximum value.
d1) Coefficient $c(i)$ is ready for the next update request (not_updated).

The requirements for the 40GBASE-CR4 and 100GBASE-CR10 transmit equalizer are intended to be similar to the requirements for 10GBASE-KR specified in 72.7.1.10. However, the signal path from the transmit function to TP2 introduces frequency-dependent loss and phase shift that distorts the signal and makes it difficult to accurately characterize equalizer performance at TP2 using the methodology specified for 10GBASE-KR. The following process enables accurate characterization of the equalizer performance at TP2 by determining and correcting for the frequency-dependent loss and phase shift of the signal path from the transmit function to TP2.

1) The transmitter under test is preset as specified in 72.6.10.2.3.1 such that $c(-1)$ and $c(1)$ are zero and $c(0)$ is its maximum value.
2) Capture at least one complete cycle of the test pattern PRBS9 as specified in 83.5.10 at TP2 per 85.8.3.3.4.
3) Compute the linear fit to the captured waveform and the linear fit pulse response $p(k)$ per 85.8.3.3.5.
4) Define t_x to be the time where the rising edge of the linear fit pulse, p, from step 3) crosses 50% of its peak amplitude.
5) Sample the linear fit pulse, p, at symbol-spaced intervals relative to the time $t_0 = t_x + 0.5$ UI, interpolating as necessary to yield the sampled pulse p_i.
6) Use p_i to compute the vector of coefficients, w, of a N_w-tap symbol-spaced transversal filter that equalizes for the transfer function from the transmit function to TP2 per 85.8.3.3.6.

The parameters of the pulse fit and the equalizing filter are given in Table 85–6. The DC amplitude, the sum of linear fit pulse response, $p(k)$, from step 3) divided by M from step 3), shall be greater than 0.34 V and less than or equal to 0.6 V. The peak of the linear fit pulse response from step 3) shall be greater than 0.63 × DC amplitude. The RMS value of the error between the linear fit from step 3) and the measured waveform, e, normalized to the peak value of the pulse, p, shall be no greater than 0.037.

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Table 85–6—Normalized transmit pulse template

Description	Symbol	Value	Units
Linear fit pulse length	N_p	8	UI
Linear fit pulse delay	D_p	2	UI
Equalizer length	N_w	7	UI
Equalizer delay	D_w	1	UI

For each configuration of the transmit equalizer

7) Configure the transmitter under test as required by the test.
8) Capture at least one complete cycle of the test pattern PRBS9 as specified in 83.5.10 at TP2 per 85.8.3.3.4.
9) Compute the linear fit to the captured waveform and the linear fit pulse response p(k) per 85.8.3.3.5.
10) Define t_x to be the time where the rising edge of the linear fit pulse response, p(k), from step 9) crosses 50% of its peak amplitude.
11) Sample the linear fit pulse response, p(k), at symbol-spaced intervals relative to the time $t_0 = t_x + 0.5$ UI, interpolating as necessary to yield the sampled pulse p_i.
12) Equalize the sampled pulse p_i using the coefficient vector, w, computed in step 6) per 85.8.3.3.6 to yield the equalized pulse q_i.

The RMS value of the error between the linear fit from step 9) and the measured waveform, e, normalized to the peak value of the pulse, p, shall be no greater than 0.037.

Coefficient $c(-1)$ is defined to be the value of q_i at time $t_0 + (D_p - 1)$ UI. Coefficient $c(0)$ is defined to be the value of q_i at time $t_0 + D_p$ UI. Coefficient $c(1)$ is defined to be the value of q_i at time $t_0 + (D_p + 1)$ UI.

85.8.3.3.1 Coefficient initialization

When the PMD enters the INITIALIZE state of the Training state diagram (Figure 72–5) or receives a valid request to "initialize" from the link partner, the coefficients of the transmit equalizer shall be configured such that the ratio $(c(0)+c(1)-c(-1))/(c(0)+c(1)+c(-1))$ is 1.29 ±10% and the ratio $(c(0)-c(1)+c(1))/(c(0)+c(1)+c(-1))$ is 2.57 ±10%. These requirements apply upon the assertion a coefficient status report of "updated" for all coefficients.

85.8.3.3.2 Coefficient step size

The change in $c(i)$ corresponding to a request to "increment" that coefficient shall be between 0.0083 and 0.05. The change in $c(i)$ corresponding to a request to "decrement" that coefficient shall be between –0.05 and –0.0083.

The change in the coefficient is defined to be the difference in the value measured prior to the assertion of the "increment" or "decrement" request (e.g., the coefficient update request for all coefficients is "hold") and the value upon the assertion of a coefficient status report of "updated" for that coefficient.

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85.8.3.3.3 Coefficient range

When sufficient "increment" or "decrement" requests have been received for a given coefficient, the coefficient will reach a lower or upper bound based on the range of that coefficient or the combination of coefficients.

With $c(-1)$ set to zero and both $c(0)$ and $c(1)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0) - c(1))/(c(0) + c(1))$ shall be greater then or equal to 4.

With $c(1)$ set to zero and both $c(-1)$ and $c(0)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0) - c(-1))/(c(0) + c(-1))$ shall be greater then or equal to 1.54.

Note that a coefficient may be set to zero by first asserting a coefficient preset request and then manipulating the other coefficients as required by the test.

85.8.3.3.4 Waveform acquisition

The transmitter under test repetitively transmits the specified test pattern. The waveform shall be captured with an effective sample rate that is M times the signaling rate of the transmitter under test. The value of M shall be an integer not less than 7. Averaging multiple waveform captures is recommended.

The captured waveform shall represent an integer number of repetitions of the test pattern totaling N bits. Hence the length of the captured waveform should be MN samples. The waveform should be aligned such that the first M samples of waveform correspond to the first bit of the test pattern, the second M samples to the second bit, and so on.

85.8.3.3.5 Linear fit to the waveform measurement at TP2

Given the captured waveform $y(k)$ and corresponding aligned symbols $x(\mathrm{n})$ derived from the procedure defined in 85.8.3.3.4, define the M-by-N waveform matrix Y as shown in Equation (85–4).

$$Y = \begin{bmatrix} y(1) & y(M+1) & \dots & y(M(N-1)+1) \\ y(2) & y(M+2) & \dots & y(M(N-1)+2) \\ \dots & \dots & \dots & \dots \\ y(M) & y(2M) & \dots & y(MN) \end{bmatrix} \tag{85–4}$$

Rotate the symbols vector x by the specified pulse delay D_p to yield x_r as shown in Equation (85–5).

$$x_r = \left[x(D_p+1) \;\; x(D_p+2) \dots x(N) \; x(1) \; \dots \; x(D_p)\right] \tag{85–5}$$

Define the matrix X to be an N-by-N matrix derived from x_r as shown in Equation (85–6).

$$X = \begin{bmatrix} x_r(1) & x_r(2) & \dots & x_r(N) \\ x_r(N) & x_r(1) & \dots & x_r(N-1) \\ \dots & \dots & \dots & \dots \\ x_r(2) & x_r(3) & \dots & x_r(1) \end{bmatrix} \tag{85–6}$$

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Define the matrix X_1 to be the first N_p rows of X concatenated with a row vector of ones of length N. The M-by-$(N_p + 1)$ coefficient matrix, P, corresponding to the linear fit is then defined by Equation (85–7). The superscript "T" denotes the matrix transpose operator.

$$P = YX_1^T(X_1X_1^T)^{-1} \tag{85–7}$$

The error waveform, $e(k)$, is then read column-wise from the elements of the error matrix E defined by Equation (85–8).

$$E = PX_1 - Y = \begin{bmatrix} e(1) & e(M+1) & \dots & e(M(N-1)+1) \\ e(2) & e(M+2) & \dots & e(M(N-1)+2) \\ \dots & \dots & \dots & \dots \\ e(M) & e(2M) & \dots & e(MN) \end{bmatrix} \tag{85–8}$$

Define P_1 to be a matrix consisting of the first N_p columns of the matrix P as shown in Equation (85–9). The linear fit pulse response, $p(k)$, is then read column-wise from the elements of P_1.

$$P_1 = \begin{bmatrix} p(1) & p(M+1) & \dots & p(M(N_p-1)+1) \\ p(2) & p(M+2) & \dots & p(M(N_p-1)+2) \\ \dots & \dots & \dots & \dots \\ p(M) & p(2M) & \dots & p(MN_p) \end{bmatrix} \tag{85–9}$$

85.8.3.3.6 Transfer function between the transmit function and TP2

Rotate the sampled pulse response p_i by the specified equalizer delay D_w to yield p_r as shown in Equation (85–10).

$$p_r = \left[p_i(D_w+1)\ \ p_i(D_p+2) \dots\ p_i(N_p)\ p_i(1)\ \dots\ p_i(D_w)\right] \tag{85–10}$$

Define the matrix P_2 to be an N_p-by-N_p matrix derived from p_r as shown in Equation (85–11).

$$P_2 = \begin{bmatrix} p_r(1) & p_r(N_p) & \dots & p_r(2) \\ p_r(2) & p_r(1) & \dots & p_r(3) \\ \dots & \dots & \dots & \dots \\ p_r(N_p) & p_r(N_p-1) & \dots & p_r(1) \end{bmatrix} \tag{85–11}$$

Define the matrix P_3 to be the first N_w columns of P_2. Define a unit pulse column vector x_p of length N_p. The value of element $x_p(D_p + 1)$ is 1 and all other elements have a value of 0. The vector of filter coefficients w that equalizes p_i is then defined by Equation (85–12).

$$w = (P_3^TP_3)^{-1}P_3^Tx_p \tag{85–12}$$

Given the column vector of equalizer coefficients, w, the equalized pulse response q_i is determined by Equation (85–13).

$$q_i = P_3w \tag{85–13}$$

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85.8.3.4 Insertion loss TP0 to TP2 or TP3 to TP5

Transmitter measurements and tests defined in Table 85–5 are made at TP2 or TP3 using the test fixture of Figure 85–6, or its functional equivalent. The maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is determined using Equation (85–14).

$$Insertion\_loss(f) \le \left\{ \begin{array}{ll} 0.114 + 0.8914\sqrt{f} + 0.846f & 0.01 \le f < 7 \\ -35.91 + 6.3291f & 7 \le f < 8 \\ 14.72 & 8 \le f \le 10 \end{array} \right\} \text{ (dB)} \quad (85\text{–}14)$$

where

f is the frequency in GHz
$Insertion\_loss(f)$ is the insertion loss at frequency f

The maximum insertion loss of TP0 to TP2 or TP3 to TP5 is illustrated in Figure 85–5.

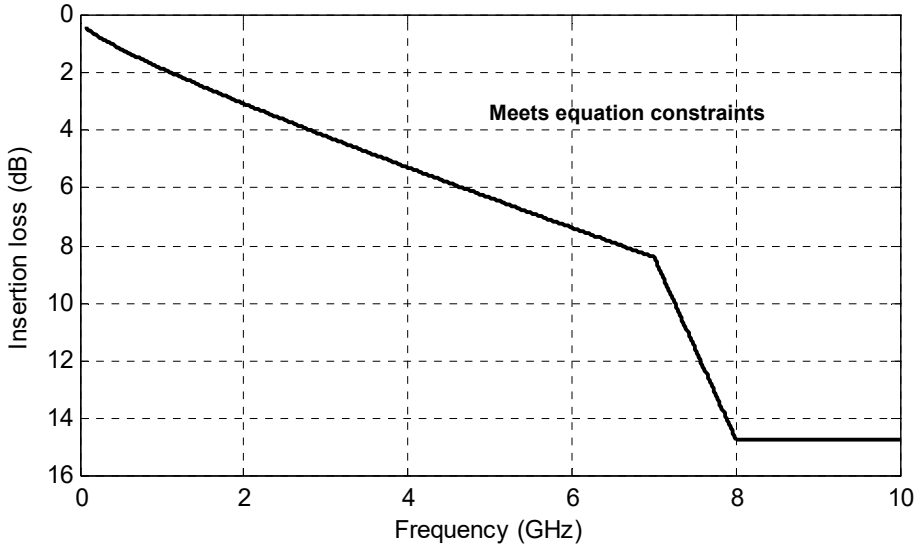

Figure 85–5—Maximum insertion loss TP0 to TP2 or TP3 to TP5

85.8.3.5 Test fixture

The test setup illustrated in Figure 85–6, or its functional equivalent, is required for measuring the transmitter specifications in 85.8.3 at TP2 and the receiver return loss at TP3. TP2 and TP3 are illustrated in Figure 85–2. Figure 85–6 illustrates the test fixture attached to TP2 or TP3.

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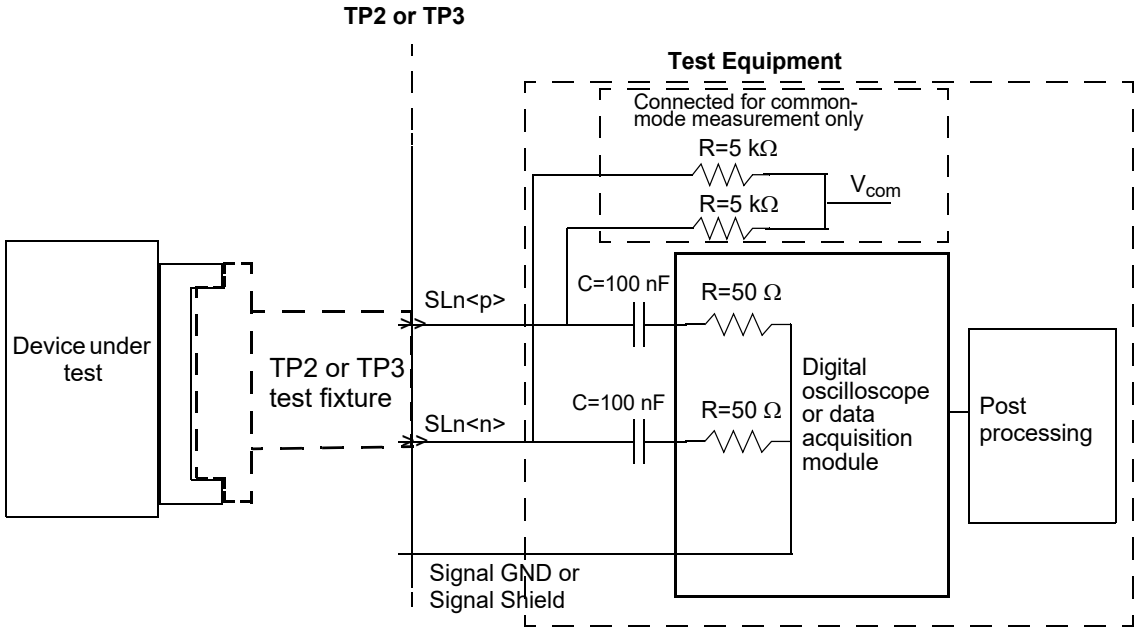

Figure 85–6—Transmitter and receiver test setup

85.8.3.6 Test fixture impedance

The differential return loss, in dB, of the test fixture is specified in a mated state and shall meet the requirements of 85.10.9.2.

85.8.3.7 Test fixture insertion loss

The reference test fixture printed circuit board insertion loss shall meet the values determined using Equation (85–15). The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the measurements.

$$IL_{tfref}(f) = 0.01 + 0.3\sqrt{f} + 0.11f \text{ (dB)} \quad (85–15)$$

for 0.01 GHz $\leq f \leq$ 10 GHz

where

f is the frequency in GHz
$IL_{tfref}(f)$ is the reference test fixture PCB insertion loss at frequency f

85.8.3.8 Data dependent jitter (DDJ)

An oscilloscope, time interval analyzer, or other instrument with equivalent capability may be used to measure DDJ. A repeating PRBS9 pseudo-random test pattern, 511 bits long, is used. For DDJ measurements, the measurement bandwidth should be at least 12 GHz. If the measurement bandwidth affects the result, it can be corrected for by post-processing.

Establish a crossing level equal to the average value of the entire waveform being measured. Synchronize the instrument to the pattern repetition frequency and average the waveforms or the crossing times

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sufficiently to remove the effects of random jitter and noise in the system. The PRBS9 pattern has 128 positive-going transitions and 128 negative-going transitions. The mean time of each crossing is then compared to the expected time of the crossing, and a set of 256 timing variations is determined. Crossings earlier than expected give a negative variation. Crossings later than expected give a positive variation. DDJ is the range (maximum minus minimum) of the timing variations. Note that it may be convenient to align the expected time of one of the crossings with the measured mean crossing.

Figure 85–7 illustrates the method. The vertical axis is in arbitrary units, and the horizontal axis is plotted in UI. The waveform is AC-coupled to an average value of 0, therefore 0 is the appropriate crossing level. The rectangular waveform shows the ideal crossing times, and the other is the waveform with jitter that is being measured. Only 16 UI are shown (out of 511). The waveforms have been arbitrarily aligned with ($\Delta t_2 = 0$) at 5 UI.

Data dependent jitter is defined as in Equation (85–16).

$$DDJ = max(\Delta t_1, \Delta t_2, \ldots \Delta t_{256}) - min(\Delta t_1, \Delta t_2, \ldots \Delta t_{256}) \quad (85\text{–}16)$$

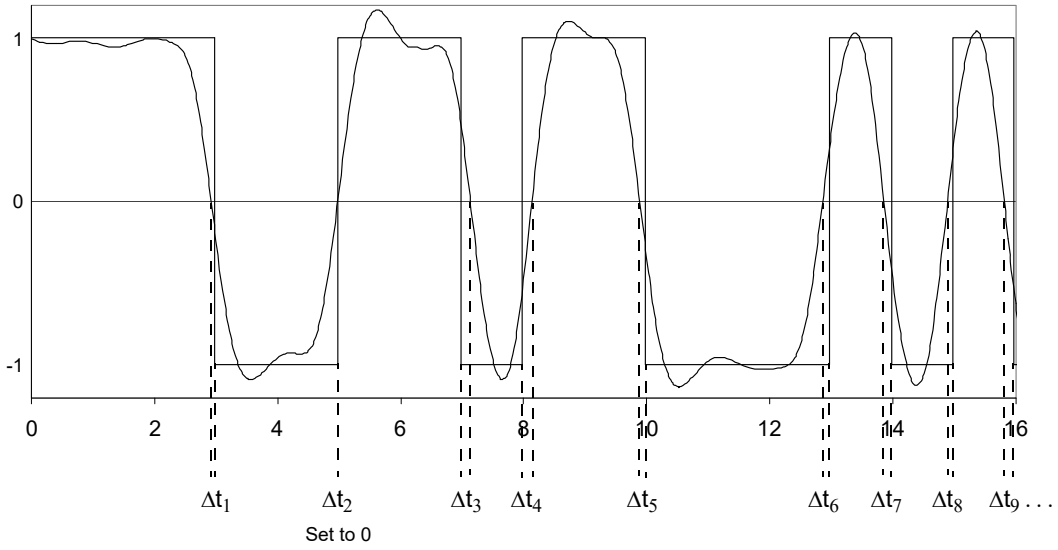

Figure 85–7—Data dependent jitter test method

85.8.3.9 Signaling rate range

The 40GBASE-CR4 and 100GBASE-CR10 MDI signaling rate shall be 10.3125 GBd ±100 ppm per lane. The corresponding unit interval is nominally 96.969697 ps.

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85.8.4 Receiver characteristics at TP3 summary

The receiver characteristics shall meet the specifications summarized in Table 85–7 at TP3 unless otherwise noted.

Table 85–7—Receiver characteristics at TP3 summary

Parameter	Subclause reference	Value	Units
Bit error ratio	85.8.4.3	10^{-12} or better	
Signaling rate, per lane	85.8.4.4	10.3125 ± 100 ppm	GBd
Unit interval (UI) nominal	85.8.4.4	96.969697	ps
Differential peak-to-peak input amplitude tolerance (max)	72.7.2.4	1200	mV
Differential input return loss (min)[a]	85.8.4.1	Equation (85–17)	dB
Differential to common-mode input return loss		10 min from 10 MHz to 10 GHz	dB

[a]Relative to 100 Ω differential.

85.8.4.1 Receiver differential input return loss

The differential input return loss, in dB, of the receiver shall meet Equation (85–17). The reference impedance for differential return loss measurements is 100 Ω.

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 12 - 2\sqrt{f} & 0.01 \leq f < 4.11 \\ 6.3 - 13\log_{10}(f/5.5) & 4.11 \leq f \leq 10 \end{array} \right\} \quad \text{(dB)} \qquad (85\text{–}17)$$

where

f is the frequency in GHz
$Return\_loss(f)$ is the return loss at frequency f

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85.8.4.2 Receiver interference tolerance test

The receiver interference tolerance of each lane shall comply with both test 1 and test 2 using the parameters of Table 85–8 when measured according to the requirements of 85.8.4.2.1 to 85.8.4.2.5.

Table 85–8—40GBASE-CR4 and 100GBASE-CR10 interference tolerance parameters

Parameter	Test 1 values	Test 2 values	Units
Maximum BER	10^{-12}	10^{-12}	
Fitted insertion loss coefficients	$a_1 = 2.15$ $a_2 = 0.78$ $a_4 = 0.03$	$a_1 = 6.04$ $a_2 = 0.94$ $a_4 = 0.08$	dB/√GHz dB/GHz dB/GHz^2
Applied SJ[a] (peak-to-peak)	0.115	0.115	UI
Applied RJ[b] (peak-to-peak)	0.13	0.13	UI
Applied DCD (peak-to-peak)	0.035	0.035	UI
Calibrated far-end crosstalk (RMS)	6.3	2.2	mV
Calibrated ICN (RMS) – σ_{nx}	3.7	3.7	mV

[a]Applied SJ frequency >15 MHz, specified at TP0.
[b]Applied random jitter at TP0 is specified at 10^{-12}.

85.8.4.2.1 Test setup

The interference tolerance test is performed with the setup shown in Figure 85–8. The requirements of this subclause are verified at the pattern generator connection (PGC) or test references in Figure 85–8 and Figure 85–9. The lanes under test (LUT) are illustrated in Figure 85–8 and Figure 85–9. The cable assembly receive lanes are terminated in 100 Ω differentially.

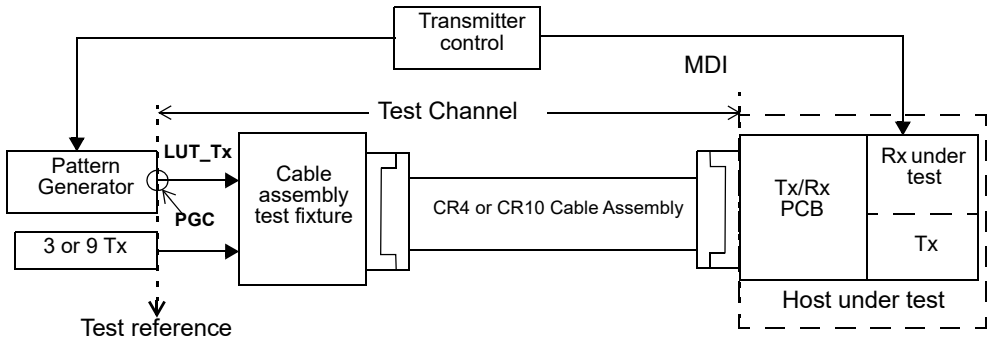

Figure 85–8—Interference tolerance test setup

85.8.4.2.2 Test channel

The test channel consists of the following:

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a) A cable assembly
b) A cable assembly test fixture
c) A connecting path from the pattern generator to the cable assembly test fixture

85.8.4.2.3 Test channel calibration

The insertion loss, near-end integrated crosstalk noise, and far-end crosstalk of the test channels are characterized at the test references as illustrated in Figure 85–9 using the cable assembly test fixtures specified in 85.10.8.

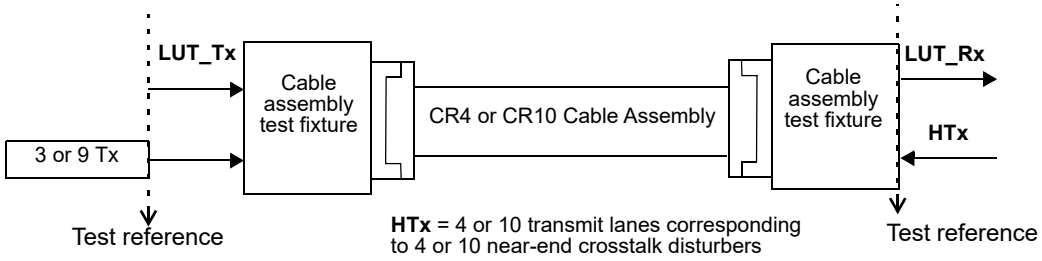

Figure 85–9—Test channel calibration

The fitted insertion loss coefficients of the lane under test (LUT), derived using the fitting procedure in 85.10.2, shall meet the test values in Table 85–8. It is recommended that the deviation between the insertion loss and the fitted insertion loss be as small as practical and that the fitting parameters be as close as practical to the values given in Table 85–8.

The MDNEXT is measured from points HTx to adjacent point LUT_Rx in Figure 85–9. HTx is the set of 4 or 10 transmit lanes of the device under test corresponding to the 4 or 10 near-end crosstalk disturbers with the parameters given in Table 85–11. The RMS value of the integrated MDNEXT crosstalk noise, determined using Equation (85–30) through Equation (85–34), shall meet the test values in Table 85–8.

The far-end crosstalk disturbers consist of 40GBASE-CR4 or 100GBASE-CR10 transmitters. It is recommended that the transition time, equalization setting, and path from the far-end crosstalk disturbers to the cable assembly test fixture emulate the pattern generator as much as practical. For 40GBASE-CR4 test channels, the crosstalk that is coupled into a receive lane is from three transmitters. For 100GBASE-CR10 test channels, the crosstalk that is coupled into a receiver lane is from nine transmitters. The disturber transmitters send either scrambled idle codes or PRBS31. The amplitudes of each of the disturbers should not deviate more than 3 dB from the mean of the disturber amplitudes. The amplitudes of the disturbers should be such that the calibrated far-end crosstalk in Table 85–8 is met in the calibration setup at the LUT point with no signal applied at the PGC, and HTx and PGC terminated in 100 Ω differentially.

85.8.4.2.4 Pattern generator

The pattern generator transmits data to the device under test. Its output amplitude shall be no more than 800 mV peak-to-peak differential when measured on an alternating one zero pattern. The rise and fall times of the pattern generator, as defined in 72.7.1.7, are 47 ps. If the rise and fall times of the pattern generator, T_r, are less than 47 ps the value of a_4 in Table 85–8 is increased by da_4 from Equation (85–18).

$$da_4 = 60.51 \times 10^{-6}(47^2 - T_r^2) \quad (85–18)$$

where T_r is the rise time in ps.

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The pattern generator shall meet the jitter specification in Table 85–8. The output waveform of the pattern generator shall comply to 72.7.1.11.

85.8.4.2.5 Test procedure

For 40GBASE-CR4 or 100GBASE-CR10 testing, the pattern generator is first configured to transmit the training pattern defined in 72.6.10.2. During this initialization period, the device under test (DUT) configures the pattern generator equalizer, via transmitter control, to the coefficient settings it would select using the protocol described in 72.6.10 and the receiver will be tuned using its optimization method.

After the pattern generator equalizer has been configured and the receiver tuned, the pattern generator is set to transmit test pattern 3 as defined in 86.8.2. The receiver under test shall meet the target BER listed in Table 85–8. During the tests, the disturbers transmit at their calibrated level and all of the transmitters in the device under test transmit either scrambled idle characters or PRBS31, with the maximum compliant amplitude and equalization turned off (preset condition).

85.8.4.3 Bit error ratio

The receiver shall operate with a BER 10^{-12} or better when receiving a compliant transmit signal, as defined in 85.8.3, through a compliant cable assembly as defined in 85.10.

85.8.4.4 Signaling rate range

A 40GBASE-CR4 and 100GBASE-CR10 receiver shall comply with the requirements of 85.8.4.3 for any signaling rate in the range 10.3125 GBd ± 100 ppm. The corresponding unit interval is nominally 96.969697 ps.

85.8.4.5 AC-coupling

The 40GBASE-CR4 and 100GBASE-CR10 receivers are AC-coupled. AC-coupling shall be part of the receive function for Style-2 40GBASE-CR4 connectors. For Style-1 40GBASE-CR4 and 100GBASE-CR10 plug connectors, the receive lanes are AC-coupled; the coupling capacitors shall be within the plug connectors. It should be noted that there may be various methods for AC-coupling in actual implementations. The low frequency 3 dB cutoff of the AC-coupling shall be less than 50 kHz.

It is recommended that the value of the coupling capacitors be 100 nF. This will limit the inrush currents and baseline wander.

85.9 Channel characteristics

The 40GBASE-CR4 and 100GBASE-CR10 channel is defined between TP0 and TP5 to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly as illustrated in Figure 85–2. The channel parameters insertion loss, insertion loss deviation (ILD), insertion loss to crosstalk ratio, and the transmitter and receiver differential controlled impedance printed circuit boards for each differential lane are provided informatively in 85A.4 through 85A.7.

85.10 Cable assembly characteristics

The 40GBASE-CR4 and 100GBASE-CR10 cable assembly contains insulated conductors terminated in a connector at each end for use as a link segment between MDIs. This cable assembly is primarily intended as a point-to-point interface of up to 7 m between network ports using controlled impedance cables. All cable assembly measurements are to be made between TP1 and TP4 with cable assembly test fixtures as specified

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in 85.10.8 and illustrated in Figure 85–14. These cable assembly specifications are based upon twinaxial cable characteristics, but other cable types are acceptable if the specifications of 85.10 are met.

Table 85–9 provides a summary of the cable assembly differential characteristics at 5.15625 GHz and references to the subclauses addressing each parameter.

Table 85–9—Cable assembly differential characteristics summary

Description	Reference	Value	Unit
Maximum insertion loss at 5.15625 GHz	85.10.2	17.04	dB
Minimum insertion loss at 5.15625 GHz		3	dB
Insertion loss deviation at 5.15625 GHz	85.10.3	max = 1.73 min = –1.73	dB
Minimum return loss at 5.15625 GHz	85.10.4	6.66	dB
MDNEXT loss	85.10.5	Equation (85–26)	dB
MDFEXT loss	85.10.6	Equation (85–27)	dB
Maximum integrated crosstalk noise	85.10.7	Equation (85–33)	mV

85.10.1 Characteristic impedance and reference impedance

The nominal differential characteristic impedance of the cable assembly is 100 Ω. The differential reference impedance for cable assembly specifications shall be 100 Ω.

85.10.2 Cable assembly insertion loss

The fitted cable assembly insertion loss $IL_{fitted}(f)$ as a function of frequency f is defined in Equation (85–19).

$$IL_{\text{fitted}}(f) = a_1\sqrt{f} + a_2 f + a_4 f^2 \quad \text{(dB)} \tag{85–19}$$

where

f is the frequency in GHz
$IL_{\text{fitted}}(f)$ is the fitted cable assembly insertion loss at frequency f

Given the cable assembly insertion loss measured between TP1 and TP4 is at N uniformly-spaced frequencies f_n spanning the frequency range 50 MHz to 7500 MHz with a maximum frequency spacing of 10 MHz, the coefficients of the fitted insertion loss are determined using Equation (85–20) and Equation (85–21).

Define the frequency matrix F as shown in Equation (85–20).

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$$F = \begin{bmatrix} \sqrt{f_1} & f_1 & f_1^2 \\ \sqrt{f_2} & f_2 & f_2^2 \\ \cdots & \cdots & \cdots \\ \sqrt{f_N} & f_N & f_N^2 \end{bmatrix} \quad (85–20)$$

The polynomial coefficients a_1, a_2, and a_4 are determined using Equation (85–21). In Equation (85–21), T denotes the matrix transpose operator and IL is a column vector of the measured insertion loss values, IL_n at each frequency f_n.

$$\begin{bmatrix} a_1 \\ a_2 \\ a_4 \end{bmatrix} = (F^T F)^{-1} F^T IL \quad (85–21)$$

The maximum allowed values of the polynomial coefficients a_1, a_2, and a_4 of the fitted cable assembly insertion loss of each pair of the 40GBASE-CR4 and 100GBASE-CR10 in Equation (85–19) and the maximum insertion loss at 5.15625 GHz shall meet the specifications summarized in Table 85–10 unless otherwise noted. The fitted insertion loss corresponding to one example of the maximum insertion loss at 5.15625 GHz and the maximum allowed values of a_1, a_2, and a_4 is illustrated in Figure 85–10.

Table 85–10—Maximum cable assembly insertion loss characteristics

Description	Value	Unit
Maximum insertion loss at 5.15625 GHz	17.04[a]	dB
Maximum fitted insertion loss coefficient a_1	6	dB/√GHz
Maximum fitted insertion loss coefficient a_2	1	dB/GHz
Maximum fitted insertion loss coefficient a_4	0.08	dB/GHz^2

[a]The limit on the maximum insertion loss at 5.15625 GHz precludes the coefficients a_1, a_2, and a_4 from simultaneous maximum values.

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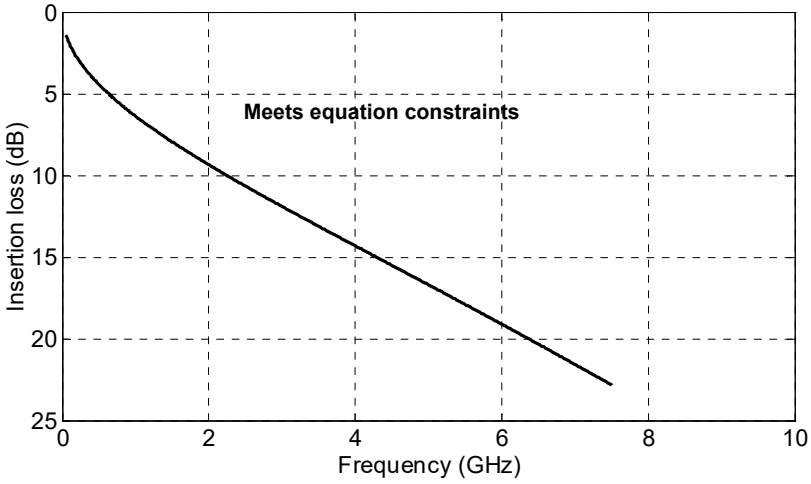

Figure 85–10—Example maximum cable assembly insertion

85.10.3 Cable assembly insertion loss deviation (ILD)

The cable assembly insertion loss deviation is the difference between the cable assembly insertion loss and the fitted cable assembly insertion loss determined using Equation (85–22).

$$ILD(f) = IL(f) - IL_{\text{fitted}}(f) \quad (85–22)$$

where

f	is the frequency in MHz
$ILD(f)$	is the cable assembly insertion loss deviation at frequency f

The *ILD* shall be within the region defined by Equation (85–23) and Equation (85–24). This includes the insertion loss of the differential cabling pairs and the cable assembly connectors.

$$ILD(f) \geq ILD_{\text{min}}(f) = -0.7 - 0.2\times10^{-3} f \text{ (dB)} \quad (85–23)$$

$$ILD(f) \leq ILD_{\text{max}}(f) = 0.7 + 0.2\times10^{-3} f \text{ (dB)} \quad (85–24)$$

for 50 MHz $\leq f \leq$ 7500 MHz

where

f	is the frequency in MHz

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The insertion loss deviation limits are illustrated in Figure 85–11.

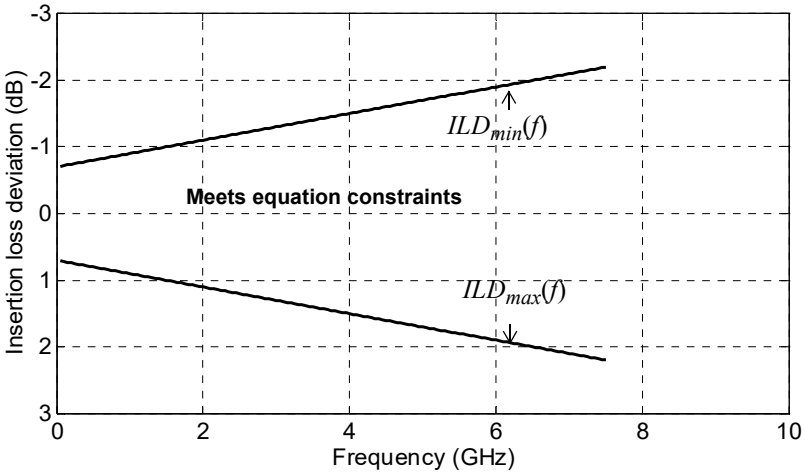

Figure 85–11—Maximum cable assembly insertion loss deviation

85.10.4 Cable assembly return loss

The return loss of each pair of the 40GBASE-CR4 and 100GBASE-CR10 cable assembly shall meet the values determined using Equation (85–25).

$$Return\_loss(f) \geq \begin{cases} 12 - 2\sqrt{f} & 0.05 \leq f < 4.1 \\ 6.3 - 13\log_{10}(f/5.5) & 4.1 \leq f \leq 10 \end{cases} \text{ (dB)} \quad (85–25)$$

where

f	is the frequency in GHz
$Return\_loss(f)$	is the return loss at frequency f

The minimum cable assembly return loss is illustrated in Figure 85–12.

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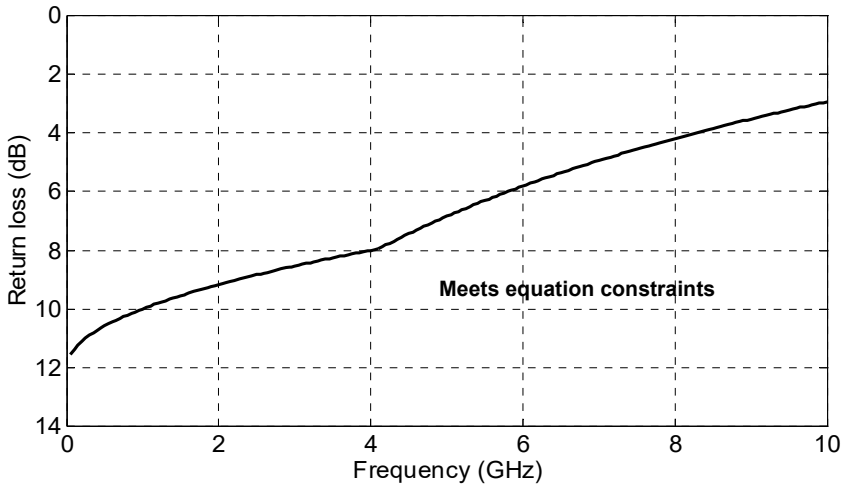

Figure 85–12—Minimum cable assembly return loss

85.10.5 Cable assembly multiple disturber near-end crosstalk (MDNEXT) loss

Since four lanes or ten lanes are used to transfer data between PMDs, the NEXT that is coupled into a receive lane will be from the four or ten transmit lanes. Multiple Disturber Near-End Crosstalk (MDNEXT) loss is determined using the individual NEXT losses.

MDNEXT loss is determined from the four or ten individual pair-to-pair differential NEXT loss values using Equation (85–26).

$$MDNEXT\_loss(f) = -10\log_{10}\left(\sum_{i=0}^{i=3\text{or }9} 10^{-NLi(f)/10}\right) \text{(dB)} \quad (85–26)$$

for 50 MHz ≤ f ≤ 10000 MHz

where

$MDNEXT\_loss(f)$	is the MDNEXT loss at frequency f
$NL_i(f)$	is the NEXT loss at frequency f of pair combination i, in dB
f	is the frequency in MHz
i	is the 0 to 3 (pair-to-pair combination) or 0 to 9 (pair-to-pair combination)

85.10.6 Cable assembly multiple disturber far-end crosstalk (MDFEXT) loss

Since four lanes or ten lanes are used to transfer data between PMDs, the FEXT that is coupled into a data carrying lane will be from the three other lanes or nine other lanes in the same direction. MDFEXT loss is specified using the individual FEXT losses. MDFEXT loss is determined from the three or nine individual pair-to-pair differential FEXT loss values using Equation (85–27).

$$MDFEXT\_loss(f) = -10\log_{10}\left(\sum_{i=0}^{i=2\text{ or }8} 10^{-NLi(f)/10}\right) \text{(dB)} \quad (85–27)$$

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for 50 MHz ≤ f ≤ 10000 MHz

where

$MDFEXT\_loss(f)$	is the MDFEXT loss at frequency f
$NL_i(f)$	is the FEXT loss at frequency f of pair combination i, in dB
f	is the frequency in MHz
i	is the 0 to 2 (pair-to-pair combination) or 0 to 8 (pair-to-pair combination)

85.10.7 Cable assembly integrated crosstalk noise (ICN)

In order to limit multiple disturber crosstalk noise at a receiver, the cable assembly integrated crosstalk noise (ICN) is specified in relationship to the measured insertion loss. ICN is calculated from the MDFEXT and MDNEXT. Given the multiple disturber near-end crosstalk loss $MDNEXT\_loss(f)$ and multiple disturber far-end crosstalk loss $MDFEXT\_loss(f)$ measured over N uniformly-spaced frequencies f_n spanning the frequency range 50 MHz to 10000 MHz with a maximum frequency spacing of 10 MHz, the RMS value of the integrated crosstalk noise shall be determined using Equation (85–28) through Equation (85–32). The RMS crosstalk noise is characterized at the output of a specified receive filter utilizing a specified transmitter waveform and the measured multiple disturber crosstalk transfer functions. The transmitter and receiver filters are defined in Equation (85–28) and Equation (85–29) as weighting functions to the multiple disturber crosstalk in Equation (85–30) and Equation (85–31). The sinc function is defined by $\mathrm{sinc}(x) = \sin(\pi x)/(\pi x)$.

Define the weight at each frequency f_n using Equation (85–28) and Equation (85–29).

$$W_{nt}(f_n) = (A_{nt}^2/f_b)\mathrm{sinc}^2(f_n/f_b)\left[\frac{1}{1+(f_n/f_{nt})^4}\right]\left[\frac{1}{1+(f_n/f_r)^8}\right] \quad (85–28)$$

$$W_{ft}(f_n) = (A_{ft}^2/f_b)\mathrm{sinc}^2(f_n/f_b)\left[\frac{1}{1+(f_n/f_{ft})^4}\right]\left[\frac{1}{1+(f_n/f_r)^8}\right] \quad (85–29)$$

where the equation parameters are given in Table 85–11.

Note that the 3 dB transmit filter bandwidths f_{nt} and f_{ft} are inversely proportional to the 20% to 80% rise and fall times T_{nt} and T_{ft} respectively. The constant of proportionality is 0.2365 (e.g., $T_{nt}f_{nt} = 0.2365$; with f_{nt} in hertz and T_{nt} in seconds). In addition, f_r is the 3 dB reference receiver bandwidth, which is set to 7.5 GHz.

The near-end integrated crosstalk noise σ_{nx} is calculated using Equation (85–30).

$$\sigma_{nx} = \left[2\Delta f\sum_n W_{nt}(f_n)10^{-MDNEXT_{loss}(f_n)/10}\right]^{1/2} \quad (85–30)$$

The far-end integrated crosstalk noise σ_{fx} is calculated using Equation (85–31).

$$\sigma_{fx} = \left[2\Delta f\sum_n W_{ft}(f_n)10^{-MDFEXT_{loss}(f_n)/10}\right]^{1/2} \quad (85–31)$$

where Δf is the uniform frequency step of f_n.

The total integrated crosstalk noise σ_x is calculated using Equation (85–32).

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$$\sigma_x = \sqrt{\sigma_{nx}^2 + \sigma_{fx}^2} \quad (85–32)$$

The total integrated crosstalk noise for the cable assembly shall be computed using the parameters shown in Table 85–11.

Table 85–11—Cable assembly integrated crosstalk parameters

Description	Symbol	Value	Units
Symbol rate	f_b	10.3125	GBd
Near-end disturber peak differential output amplitude	A_{nt}	600	mV
Far-end disturber peak differential output amplitude	A_{ft}	600	mV
Near-end disturber 20% to 80% rise and fall times	T_{nt}	24	ps
Far-end disturber 20% to 80% rise and fall times	T_{ft}	24	ps

The total integrated crosstalk RMS noise voltage shall meet the values determined by Equation (85–33) illustrated in Figure 85–13.

$$\sigma_{x,\,\mathrm{ca}} \leq \left\{ \begin{array}{ll} 10 & 3 \leq IL \leq 5.3 \\ 12.4 - 0.45IL & 5.3 < IL \leq 17.04 \end{array} \right\} \quad (\mathrm{mV}) \quad (85–33)$$

where IL is the value of the cable assembly insertion loss in dB at 5.15625 GHz.

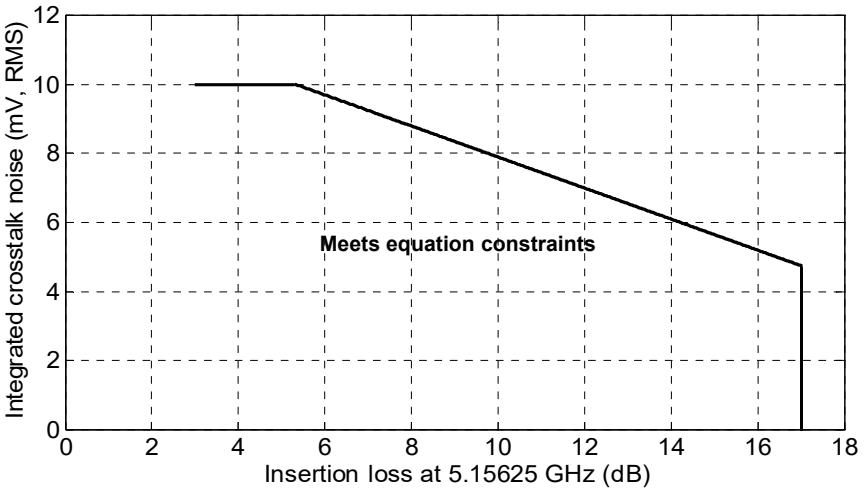

Figure 85–13—Integrated crosstalk noise limits

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85.10.8 Cable assembly test fixture

The test fixture of Figure 85–14 or its functional equivalent, is required for measuring the cable assembly specifications in 85.10 at TP1 and TP4. TP1 and TP4 are illustrated in Figure 85–2 and Figure 85–14. The test fixture return loss is equivalent to the test fixture return loss specified in 85.8.3.6. The reference test fixture printed circuit board insertion loss is given in Equation (85–34). The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the measurements.

$$IL_{\text{catf}}(f) = 0.0006 + 0.16\sqrt{f} + 0.0587f \text{ (dB)} \quad (85–34)$$

for 0.01 GHz $\leq f \leq$ 10 GHz

where

f is the frequency in GHz
$IL_{\text{catf}}(f)$ is the reference test fixture printed circuit board insertion loss at frequency f

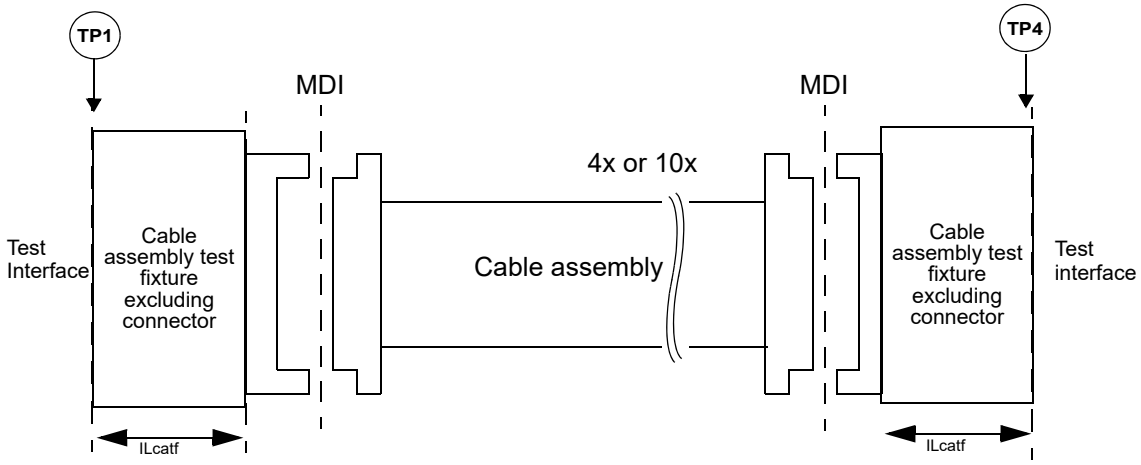

Figure 85–14—Cable assembly test fixtures

85.10.9 Mated test fixtures

The test fixtures of Figure 85–6 and Figure 85–14 are specified in a mated state illustrated in Figure 85–15.

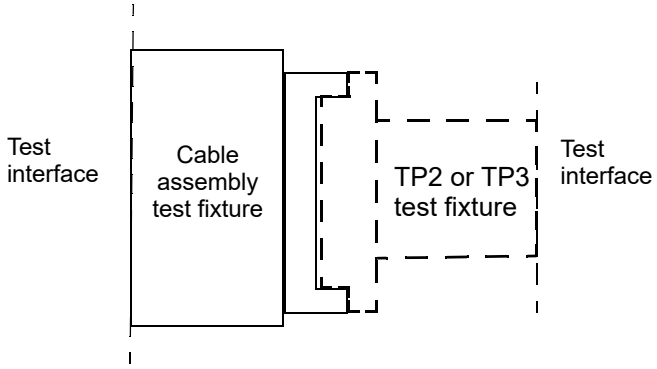

Figure 85–15—Mated test fixtures

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85.10.9.1 Mated test fixtures insertion loss

The insertion loss of the mated test fixtures shall meet the values determined using Equation (85–35) and Equation (85–36).

$$IL(f) \geq IL_{MTFmin}(f) = -0.11 + 0.46\sqrt{f} + 0.16f \qquad 0.01 \leq f \leq 10 \qquad \text{(dB)} \tag{85–35}$$

$$IL(f) \leq IL_{MTFmax}(f) = \left\{ \begin{array}{ll} 0.029 + 0.861\sqrt{f} + 0.158f & 0.01 \leq f < 5.5 \\ 0.2 + 0.65f & 5.5 \leq f \leq 10 \end{array} \right\} \text{(dB)} \tag{85–36}$$

where

f	is the frequency in GHz
$IL(f)$	is the mated test fixture insertion loss at frequency f

The mated test fixtures insertion loss limits are illustrated in Figure 85–16.

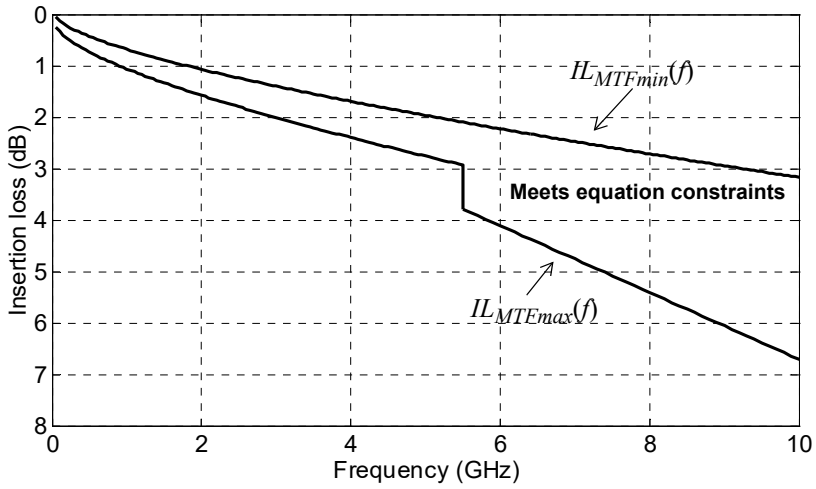

Figure 85–16—Mated test fixtures Insertion loss

85.10.9.2 Mated test fixtures return loss

The return loss of the mated test fixtures measured at either test fixture test interface shall meet the values determined using Equation (85–37).

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 20 - 2f & 0.01 \leq f < 2.5 \\ 15 & 2.5 \leq f < 5 \\ 13.8 - 28.85\log_{10}(f/5.5) & 5 \leq f \leq 10 \end{array} \right\} \text{(dB)} \tag{85–37}$$

where

f	is the frequency in GHz
$Return\_loss(f)$	is the return loss at frequency f

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The mated test fixtures return loss is illustrated in Figure 85–17.

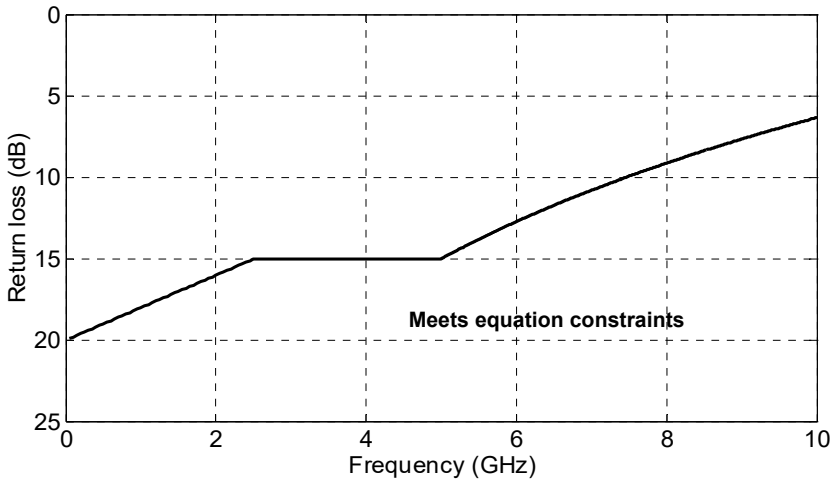

Figure 85–17—Mated test fixtures return loss

85.10.9.3 Mated test fixtures common-mode conversion loss

The common-mode conversion loss of the mated test fixtures measured at either test fixture test interface shall meet the values determined using Equation (85–38).

$$Conversion\_loss(f) \geq \left\{ \begin{array}{ll} 30 - 2.91f & 0.01 \leq f < 5.5 \\ 14 & 5.5 \leq f \leq 10 \end{array} \right\} \text{ (dB)} \quad (85–38)$$

where

f is the frequency in GHz
$Conversion\_loss(f)$ is the return loss at frequency f

The mated test fixtures common-mode conversion loss is illustrated in Figure 85–18.

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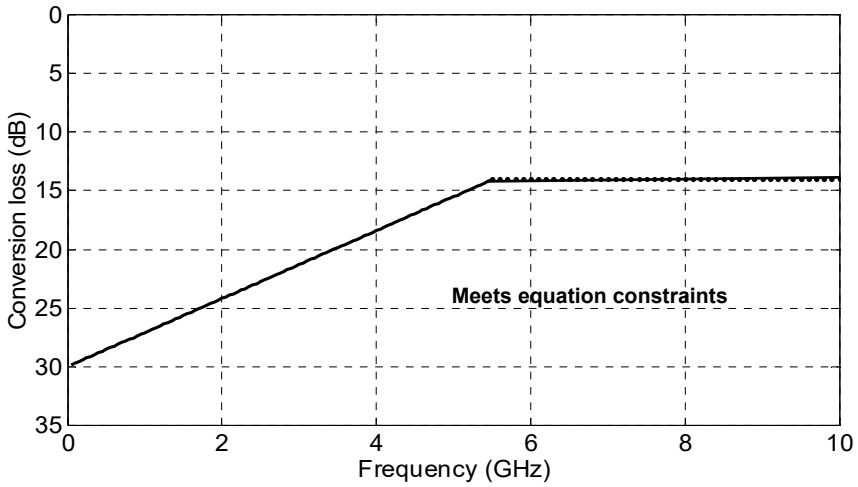

Figure 85–18—Common-mode conversion loss

85.10.9.4 Mated test fixtures integrated crosstalk noise

The mated test fixtures integrated crosstalk RMS noise voltages for the single-disturber near-end crosstalk loss and the single-disturber far-end crosstalk loss are determined using Equation (85–28) through Equation (85–32) by substituting the single disturber near-end for the multiple disturber near-end crosstalk loss and the single disturber far-end crosstalk loss for the multiple disturber far-end crosstalk loss. The values of the mated test fixtures integrated crosstalk RMS noise voltages determined using Equation (85–28) through Equation (85–32) for the single-disturber near-end crosstalk loss, the single-disturber far-end crosstalk loss, the multiple disturber near-end crosstalk loss, and the multiple disturber far-end crosstalk loss shall meet the specifications in Table 85–12.

Table 85–12—Mated test fixtures integrated crosstalk noise

Parameter	40GBASE-CR4	100GBASE-CR10	Units
Near-end integrated crosstalk noise voltage (max, RMS)	0.7	3	mV
Far-end integrated crosstalk noise voltage (max, RMS)	2.5	4	mV
MDNEXT integrated crosstalk noise voltage (max, RMS)	1	3	mV
MDFEXT integrated crosstalk noise voltage (max, RMS)	3.5	5	mV

85.10.10 Shielding

The cable assembly shall provide Class 2 or better shielding in accordance with IEC 61196-1.

85.10.11 Crossover function

The cable assembly shall be wired in a crossover fashion as illustrated in Figure 85–19, with each of the four or ten pairs being attached to the transmitter contacts at one end and the receiver contacts at the other end.

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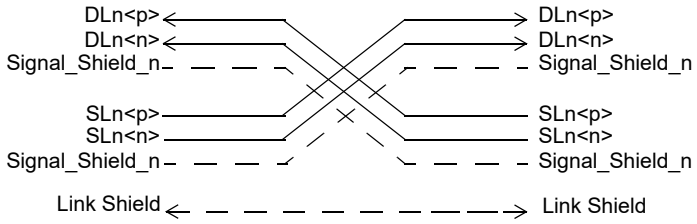

Figure 85–19—Cable assembly wiring

Note that the source lanes (SL) signals SLn<p> and SLn<n> are the positive and negative sides of the transmitters differential signal pairs and the destination lanes (DL) signals DLn<p> and DLn<n> are the positive and negative sides of the receivers differential signal pairs for lane n (n = 0, 1, 2, 3 or n = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9). Signal_Shield_n is the signal shield of the differential signal pair for Lane n.

85.11 MDI specification

This subclause defines the Media Dependent Interface (MDI). The 40GBASE-CR4 and 100GBASE-CR10 PMD, as per 85.7, is coupled to the cable assembly, as per 85.10, by the MDI.

85.11.1 40GBASE-CR4 MDI connectors

Connectors meeting the requirements of 85.11.1.1 (Style-1) or 85.11.1.2 (Style-2) shall be used as the mechanical interface between the PMD of 85.7 and the cable assembly of 85.10. The plug connector shall be used on the cable assembly and the receptacle on the PHY. Style-1 or Style-2 connectors may be used as the MDI interface.

85.11.1.1 Style-1 40GBASE-CR4 MDI connectors

The connector for each end of the cable assembly shall be the quad small form factor pluggable (QSFP+) with the mechanical mating interface defined by SFF-8436 and illustrated in Figure 85–20. The MDI connector shall be the quad small form factor pluggable (QSFP+) receptacle with the mechanical mating interface defined by SFF-8436 and illustrated in Figure 85–21. These connectors have contact assignments matching that in Table 85–13, and electrical performance consistent with the signal quality and electrical requirements of 85.8 and 85.9.

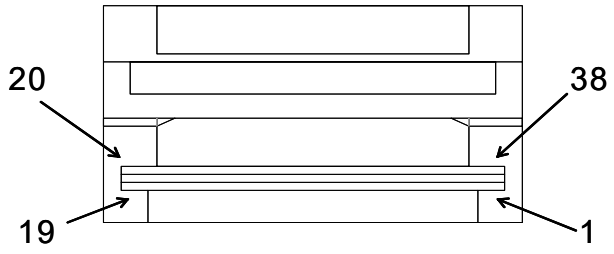

Figure 85–20—Example Style-1 cable assembly plug

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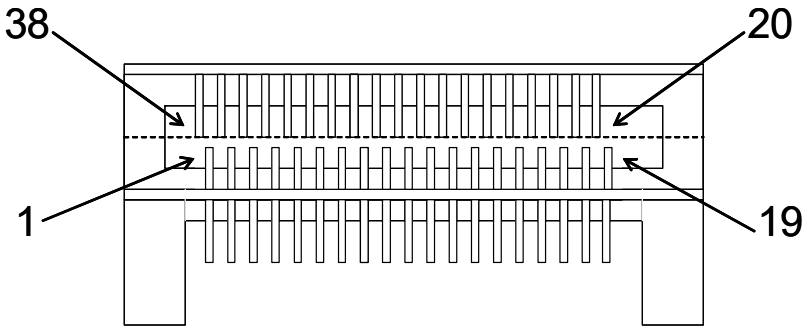

Figure 85–21—Example Style-1 MDI board receptacle

The Style-1 MDI connector of the 40GBASE-CR4 PMD comprises 38 signal connections. The Style-1 40GBASE-CR4 MDI connector contact assignments shall be as defined in Table 85–13.

Table 85–13—Style-1 40GBASE-CR4 lane to MDI connector contact mapping

Tx lane	MDI connector contact	Rx lane	MDI connector contact
signal gnd	S1	signal gnd	S13
SL1<n>	S2	DL2<p>	S14
SL1<p>	S3	DL2<n>	S15
signal gnd	S4	signal gnd	S16
SL3<n>	S5	DL0<p>	S17
SL3<p>	S6	DL0<n>	S18
signal gnd	S7	signal gnd	S19
SL2<p>	S33	DL1<n>	S21
SL2<n>	S34	DL1<p>	S22
signal gnd	S35	signal gnd	S23
SL0<p>	S36	DL3<n>	S24
SL0<n>	S37	DL3<p>	S25
signal gnd	S38	signal gnd	S26

NOTE—Although the 40GBASE-CR4 Style-1 MDI supports 38 connections only the transmitter and receiver contact assignments are specified.

85.11.1.1.1 Style-1 AC-coupling

For Style-1 40GBASE-CR4 plug connectors the receive lanes are AC-coupled; the coupling capacitors are contained within the plug connectors as specified in 85.8.4.5.

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85.11.1.2 Style-2 40GBASE-CR4 MDI connectors

The connector for each end of the cable assembly shall be the latch-type plug with the mechanical mating interface defined by SFF-8470 and illustrated in Figure 85–22. The MDI connector shall be the latch-type receptacle with the mechanical mating interface defined by SFF-8470 and illustrated in Figure 85–23. These connectors have a pinout matching that in Table 85–14, and electrical performance consistent with the signal quality and electrical requirements of 85.8 and 85.9. Note that support of compatibility with 10GBASE-CX4 is at the Style-2 40GBASE-CR4 MDI.

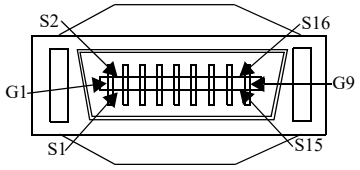

Figure 85–22—Example Style-2 cable assembly plug

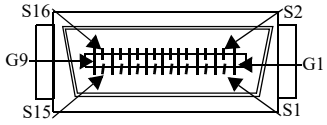

Figure 85–23—Example Style-2 MDI board receptacle

85.11.1.2.1 Style-2 40GBASE-CR4 Connector pin assignments

The MDI connector of the PMD comprises sixteen signal connections, eight signal shield connections, and one link shield connection. The 40GBASE-CR4 MDI connector pin assignments shall be as defined in Table 85–14.

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Table 85–14—Style-2 40GBASE-CR4 lane to MDI connector pin mapping

Rx lane	MDI connector pin	Tx lane	MDI connector pin
DL0<p>	S1	SL0<p>	S16
DL0<n>	S2	SL0<n>	S15
DL1<p>	S3	SL1<p>	S14
DL1<n>	S4	SL1<n>	S13
DL2<p>	S5	SL2<p>	S12
DL2<n>	S6	SL2<n>	S11
DL3<p>	S7	SL3<p>	S10
DL3<n>	S8	SL3<n>	S9
Signal Shield	G1	Signal Shield	G5
Signal Shield	G2	Signal Shield	G6
Signal Shield	G3	Signal Shield	G7
Signal Shield	G4	Signal Shield	G8
—	—	Link Shield	G9

85.11.2 100GBASE-CR10 MDI connectors

The connector for each end of the cable assembly shall be the plug with the mechanical mating interface defined in SFF-8642 and illustrated in Figure 85–24. The MDI connector shall be the receptacle with the mechanical mating interface defined by SFF-8642 and illustrated in Figure 85–25. These connectors have contact assignments matching that in Table 85–15, and electrical performance consistent with the signal quality and electrical requirements of 85.8 and 85.9.

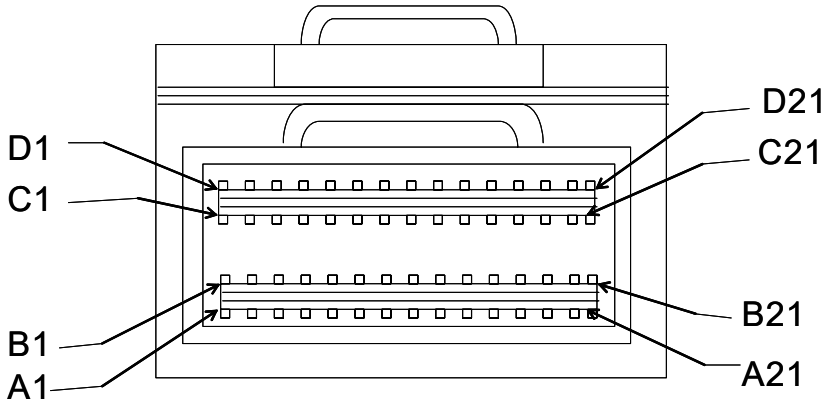

Figure 85–24—Example cable assembly plug

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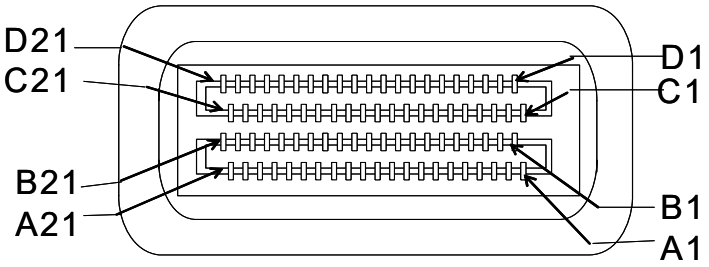

Figure 85–25—Example MDI board receptacle

The MDI connector of the PMD comprises 84 connections. The 100GBASE-CR10 PMD MDI connector contact assignments shall be as defined in Table 85–15.

Table 85–15—100GBASE-CR10 lane to MDI connector contact mapping

Tx lane	MDI connector contact	Tx lane	MDI connector contact	Rx lane	MDI connector contact	Rx lane	MDI connector contact
signal gnd	A1	signal gnd	B1	signal gnd	C1	signal gnd	D1
SL0<p>	A2	—	B2	DL0<p>	C2	—	D2
SL0<n>	A3	—	B3	DL0<n>	C3	—	D3
signal gnd	A4	signal gnd	B4	signal gnd	C4	signal gnd	D4
SL2<p>	A5	SL1<p>	B5	DL2<p>	C5	DL1<p>	D5
SL2<n>	A6	SL1<n>	B6	DL2<n>	C6	DL1<n>	D6
signal gnd	A7	signal gnd	B7	signal gnd	C7	signal gnd	D7
SL4<p>	A8	SL3<p>	B8	DL4<p>	C8	DL3<p>	D8
SL4<n>	A9	SL3<n>	B9	DL4<n>	C9	DL3<n>	D9
signal gnd	A10	signal gnd	B10	signal gnd	C10	signal gnd	D10
SL6<p>	A11	SL5<p>	B11	DL6<p>	C11	DL5<p>	D11
SL6<n>	A12	SL5<n>	B12	DL6<n>	C12	DL5<n>	D12
signal gnd	A13	signal gnd	B13	signal gnd	C13	signal gnd	D13
SL8<p>	A14	SL7<p>	B14	DL8<p>	C14	DL7<p>	D14
SL8<n>	A15	SL7<n>	B15	DL8<n>	C15	DL7<n>	D15
signal gnd	A16	signal gnd	B16	signal gnd	C16	signal gnd	D16
—	A17	SL9<p>	B17	—	C17	DL9<p>	D17
—	A18	SL9<n>	B18	—	C18	DL9<n>	D18
signal gnd	A19	signal gnd	B19	signal gnd	C19	signal gnd	D19

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NOTE—Although the 100GBASE-CR10 MDI supports 84 connections only the transmitter and receiver contact assignments are specified.

85.11.2.1 100GBASE-CR10 MDI AC-coupling

For 100GBASE-CR10 plug connectors, the receive lanes are AC-coupled; the coupling capacitors are contained within the plug connectors as specified in 85.8.4.5.

85.11.3 Electronic keying

Electronic keying can be used to enable the detection of Style-1 40GBASE-CR4 MDI connectors or 100GBASE-CR10 MDI cable assembly plugs versus fiber modules or no modules present. Specifications of electronic keying are beyond the scope of this standard.

85.12 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 14.7.

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85.13 Protocol implementation conformance statement (PICS) proforma for Clause 85, Physical Medium Dependent (PMD) sublayer and baseband medium, type 40GBASE-CR4 and 100GBASE-CR10[150]

85.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 85 Physical Medium Dependent (PMD) sublayer and baseband medium, type 40GBASE-CR4 and 100GBASE-CR10, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

85.13.2 Identification

85.13.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

85.13.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 85, Physical Medium Dependent (PMD) sublayer and baseband medium, type 40GBASE-CR4 and 100GBASE-CR10
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[150] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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85.13.3 Major capabilities/options

Item[a]	Feature	Subclause	Value/Comment	Status	Support
XLGMII	XLGMII	85.1	Interface is supported	O	Yes [ ] No [ ]
CGMII	CGMII	85.1	Interface is supported	O	Yes [ ] No [ ]
XLAUI	XLAUI	85.1		O	Yes [ ] No [ ]
CAUI-10	CAUI-10	85.1		O	Yes [ ] No [ ]
CAUI-4	CAUI-4	85.1		O	Yes [ ] No [ ]
CR4	40GBASE-CR4 PMD	85.1	Can operate as 40GBASE-CR4 PMD	O.1	Yes [ ] No [ ]
CR10	100GBASE-CR10 PMD	85.1	Can operate as 100GBASE-CR10 PMD	O.1	Yes [ ] No [ ]
PCS	Support of 40GBASE-R PCS	85.1		CR4:M	Yes [ ] N/A [ ]
PCS	Support of 100GBASE-R PCS	85.1		CR10:M	Yes [ ] N/A [ ]
PMA	Support of 40GBASE-R PMA	85.1		CR4:M	Yes [ ] N/A [ ]
PMA	Support of 100GBASE-R PMA	85.1		CR10:M	Yes [ ] N/A [ ]
FEC	Forward error correction	85.1	Device implements BASE-R forward error correction	O	Yes [ ] No [ ]
AN	Auto-negotiation	85.1	Device implements Auto-Negotiation	M	Yes [ ]
DC	Delay constraints	85.4	Device conforms to delay constraints specified in 85.4	M	Yes [ ]
DSC	Skew constraints	85.5	Device conforms to Skew and Skew Variation constraints specified in 85.5	M	Yes [ ]
*MD	MDIO capability	85.6	Registers and interface supported	O	Yes [ ] No [ ]
*CBL	Cable assembly	85.10	Items marked with CBL include cable assembly specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
CA401	40GBASE-CR4 Style-1 cable assembly	85.10	Cable assembly supports 40GBASE-CR4 Style-1	CBL:O.3	Yes [ ] No [ ] N/A [ ]
CA402	40GBASE-CR4 Style-2 cable assembly	85.10	Cable assembly supports 40GBASE-CR4 Style-2	CBL:O.3	Yes [ ] No [ ] N/A [ ]

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Item[a]	Feature	Subclause	Value/Comment	Status	Support
CA100	100GBASE-CR10 cable assembly	85.10	Cable assembly supports 100GBASE-CR10	CBL:O.3	Yes [ ] No [ ] N/A [ ]
MDIST1	Style-1 MDI connector	85.11.1.1	40GBASE-CR4 device uses Style-1 MDI	O:2	Yes [ ] No [ ]
MDIST2	Style-2 MDI connector	85.11.1.2	40GBASE-CR4 device uses Style-2 MDI	O:2	Yes [ ] No [ ]
*LPI	Implementation of LPI with the deep sleep mode option	85.2		O	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

85.13.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 40GBASE-CR4 and 100GBASE-CR10

85.13.4.1 PMD functional specifications

Item	Feature	Sub clause	Value/Comment	Status	Support
PF1	Transmit function	85.7.2	Converts four or ten logical bit streams into four or ten separate electrical signals	M	Yes [ ]
PF2	Transmit function	85.7.2	Conveys four or ten bits from PMD service interface to MDI lanes	M	Yes [ ]
PF3	Transmitter signal	85.7.2	A positive differential voltage corresponds to tx_bit = one	M	Yes [ ]
PF4	Receive function	85.7.3	Converts four or ten electrical signals from the MDI into four or ten logical bit streams	M	Yes [ ]
PF5	Receive function	85.7.3	Conveys four or ten logical bit streams from the MDI lanes to the PMD service interface	M	Yes [ ]
PF6	Receiver signal	85.7.3	A positive differential voltage corresponds to rx_bit = one	M	Yes [ ]
PF7	Global PMD Signal Detect function	85.7.4	Report state via PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
PF8	Signal_Detect value	85.7.4	Set to FAIL following reset	M	Yes [ ]
PF9	Signal_Detect value	85.7.4	Set to OK on completion of training	M	Yes [ ]
PF10	Signal_Detect value	85.7.4	Set to OK if training disabled by management	M	Yes [ ]
PF11	Global_PMD_transmit_disable	85.7.6	Disables all transmitters by forcing a constant output state	O	Yes [ ] No [ ]
PF12	Global_PMD_transmit_disable	85.7.6	Loopback not affected	O	Yes [ ] No [ ]

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Item	Feature	Sub clause	Value/Comment	Status	Support
PF13	Lane-by-lane_PMD_transmit_disable	85.7.7	Allows each lane transmitter to be selectively disabled	O	Yes [ ] No [ ]
PF14	Lane-by-lane_PMD_transmit_disable	85.7.7	Disables transmitters by forcing a constant output state	O	Yes [ ] No [ ]
PF15	Lane-by-lane_PMD_transmit_disable	85.7.7	Loopback not affected	O	Yes [ ] No [ ]
PF16	Loopback	85.7.8	Loopback function provided	M	Yes [ ]
PF17	PMD fault function	85.7.9	Mapped to bit 1.1.7 as listed in Table 85–3	M	Yes [ ]
PF18	PMD control function	85.7.12	Pattern described in 72.6.10 different for each of the lanes	M	Yes [ ]
PF19	Signal detect during LPI	85.7.4	Detect signal energy during LPI	LPI:M	Yes [ ] N/A [ ]
PF20	Signal detect for EEE	85.7.4	Transition timing to set SIGNAL_-DETECT	LPI:M	Yes [ ] N/A [ ]
PF21	Transmit disable during LPI	85.7.6	Disable transmitter during tx_mode = QUIET	LPI:M	Yes [ ] N/A [ ]

85.13.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Global_PMD_signal_detect	85.7.4	Set to the value described in 45.2.1.9.7	O	Yes [ ] No [ ]
MF2	Global_PMD_signal_detect	85.7.4	Set defined by the training state diagram in Figure 72–5	O	Yes [ ] No [ ]
MF3	Lane-by-Lane Signal Detect function	85.7.5	Sets PMD_signal_detect_n values on a lane-by-lane basis per requirements of 85.7.5	MD:M	Yes [ ] N/A [ ]
MF4	PMD_transmit_fault function	85.7.10	Mapped to the PMD_transmit_fault bit as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
MF5	PMD_receive_fault function	85.7.11	Contributes to the PMA/PMD receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]

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85.13.4.3 Transmitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
DS1	Meets specifications at TP2	85.8.3	Unless otherwise noted per Table 85–5	M	Yes [ ]
DS2	Test load	85.8.3.6	100 Ω differential load with return loss using Equation (85–1)	M	Yes [ ]
DS3	Test fixture return loss	85.8.3.6	Equation (85–37)	M	Yes [ ]
DS4	Test fixture insertion loss	85.8.3.7	Per Equation (85–15)	M	Yes [ ]
DS5	Signaling rate, per lane	85.8.3.9	10.3125 GBd ± 100 ppm	M	Yes [ ]
DS6	Output Amplitude LPI voltage	85.7.6	Less than 30 mV within 500 ns of tx_quiet	LPI:M	Yes [ ] N/A [ ]
DS7	Output Amplitude ON voltage	85.7.6	Greater than 90% of previous level within 500 ns of tx_quiet deasserted	LPI:M	Yes [ ] N/A [ ]

85.13.4.4 Receiver specifications

Item	Feature	Subclause	Value/Comment	Status	Support
RS1	Receiver tolerance	85.8.4.2	BER of better than 10^{-12}	M	Yes [ ]
RS2	Receiver tolerance	85.8.4.2	Maximum fitted insertion loss coefficients	M	Yes [ ]
RS3	Receiver tolerance	85.8.4.2	MDNEXT crosstalk noise	M	Yes [ ]
RS4	Receiver tolerance	85.8.4.2	Pattern generator output amplitude	M	Yes [ ]
RS5	Receiver tolerance	85.8.4.2	Pattern generator jitter specification	M	Yes [ ]
RS6	Bit Error Ratio	85.8.4.2.5	BER of better than 10^{-12}	M	Yes [ ]
RS7	Meets specifications at TP3	85.8.4	Unless otherwise noted per Table 85–7	M	Yes [ ]
RS8	Signaling rate, per lane	85.8.4.4	10.3125 GBd ± 100 ppm	M	Yes [ ]
RS9	AC-coupling	85.8.4.5	3 dB cutoff	M	Yes [ ]

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85.13.4.5 Cable assembly specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CA1	Differential reference impedance	85.10.1	100 Ω	CBL:M	Yes [ ] N/A [ ]
CA2	Insertion loss	85.10.2	Per Equation (85–19) and Table 85–10	CBL:M	Yes [ ] N/A [ ]
CA3	Insertion loss deviation	85.10.3	Per Equation (85–23) and Equation (85–24)	CBL:M	Yes [ ] N/A [ ]
CA4	Return loss	85.10.4	Per Equation (85–25)	CBL:M	Yes [ ] N/A [ ]
CA5	Integrated crosstalk noise	85.10.7	Integrated crosstalk noise voltage per Equation (85–28) through Equation (85–33) and Table 85–11	CBL:M	Yes [ ] N/A [ ]
CA6	Cable assembly test fixture insertion loss	85.10.8	Per Equation (85–34)	CBL:M	Yes [ ] N/A [ ]
CA7	Mated test fixture insertion loss	85.10.9.1	Per Equation (85–35) and Equation (85–36)	CBL:M	Yes [ ] N/A [ ]
CA8	Mated test fixture return loss	85.10.9.2	Per Equation (85–38)	CBL:M	Yes [ ] N/A [ ]
CA9	Mated test fixtures integrated crosstalk noise	85.10.9.4	Per Equation (85–28), through Equation (85–32) and Table 85–12	CBL:M	Yes [ ] N/A [ ]
CA10	Shielding	85.10.10	Class 2 or better in accordance with IEC 61196-1	CBL:M	Yes [ ] N/A [ ]
CA11	Crossover function	85.10.11	Per Figure 85–19	CBL:M	Yes [ ] N/A [ ]
CA12	Cable assembly connector type	85.11.1	40GBASE-CR4 Style-1 plug (SFF-8436 plug)	CA401:M	Yes [ ] N/A [ ]
CA13	Pin assignments	85.11.1.1	Per Table 85–13		Yes [ ] N/A [ ]
CA14	Cable assembly connector type	85.11.1	SFF-8470 latch-type plug	CA402:M	Yes [ ] N/A [ ]
CA15	Pin assignments	85.11.1.2.1	Per Table 85–14		Yes [ ] N/A [ ]
CA16	Cable assembly connector type	85.11.2	100GBASE-CR10 plug (SFF-8642 plug)	CA100:M	Yes [ ] N/A [ ]
CA17	Pin assignments	85.11.2	Per Table 85–15		Yes [ ] N/A [ ]
CA18	AC-coupling	85.8.4.5	3 dB cutoff	M	Yes [ ]

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85.13.4.6 MDI connector specifications

Item	Feature	Subclause	Value/Comment	Status	Support
MDC1	MDI connector type	85.11.1.1	40GBASE-CR4 Style-1 receptacle (SFF-8436 receptacle)	CR4*MDIST1:M	Yes [ ] N/A [ ]
MDC2	MDI connector type	85.11.1.2	SFF-8470 latch-type receptacle	CR4*MDIST2:M	Yes [ ] N/A [ ]
MDC3	MDI connector type	85.11.2.1	100GBASE-CR10 receptacle (SFF-8642 receptacle)	CR10:M	Yes [ ] N/A [ ]

85.13.4.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Environmental specifications	85.12		M	Yes [ ]

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86. Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-SR4 and 100GBASE-SR10

86.1 Overview

This clause specifies the 40GBASE-SR4 PMD and the 100GBASE-SR10 PMD together with the multimode fiber medium. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 86–1, to the medium through the MDI, and optionally to the management functions that are accessible through the management interface defined in Clause 45, or equivalent.

Table 86–1—Physical Layer clauses associated with the 40GBASE-SR4 and 100GBASE-SR10 PMDs

Associated clause	40GBASE-SR4	100GBASE-SR10
81—RS	Required	Required
81—XLGMII[a]	Optional	Not applicable
81—CGMII[a]	Not applicable	Optional
82—PCS for 40GBASE-R	Required	Not applicable
82—PCS for 100GBASE-R	Not applicable	Required
83—PMA for 40GBASE-R4	Required	Not applicable
83—PMA for 100GBASE-R10	Not applicable	Required
83A—XLAUI[b]	Optional	Not applicable
83A—CAUI-10[b]	Not applicable	Optional
83B—Chip to module XLAUI[b]	Optional	Not applicable
83B—Chip to module CAUI-10[b]	Not applicable	Optional
83D—CAUI-4	Not applicable	Optional
83E—Chip-to-module CAUI-4	Not applicable	Optional
86A—XLPPI	Optional	Not applicable
86A—CPPI	Not applicable	Optional
78—Energy Efficient Ethernet	Optional	Optional

[a] XLGMII and CGMII are optional interfaces. However, if the appropriate interface is not implemented, a conforming implementation behaves functionally as though the RS, and XLGMII or CGMII, were present.
[b] If XLAUI or CAUI-n is present, there is at least a PMA between the XLAUI or CAUI-n and the PMD.

Figure 86–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 40 Gb/s and 100 Gb/s Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2. Further relevant information may be found in Clause 1 (terminology and conventions, references, definitions and abbreviations) and Annex A (bibliography, referenced as [B1], [B2], etc.).

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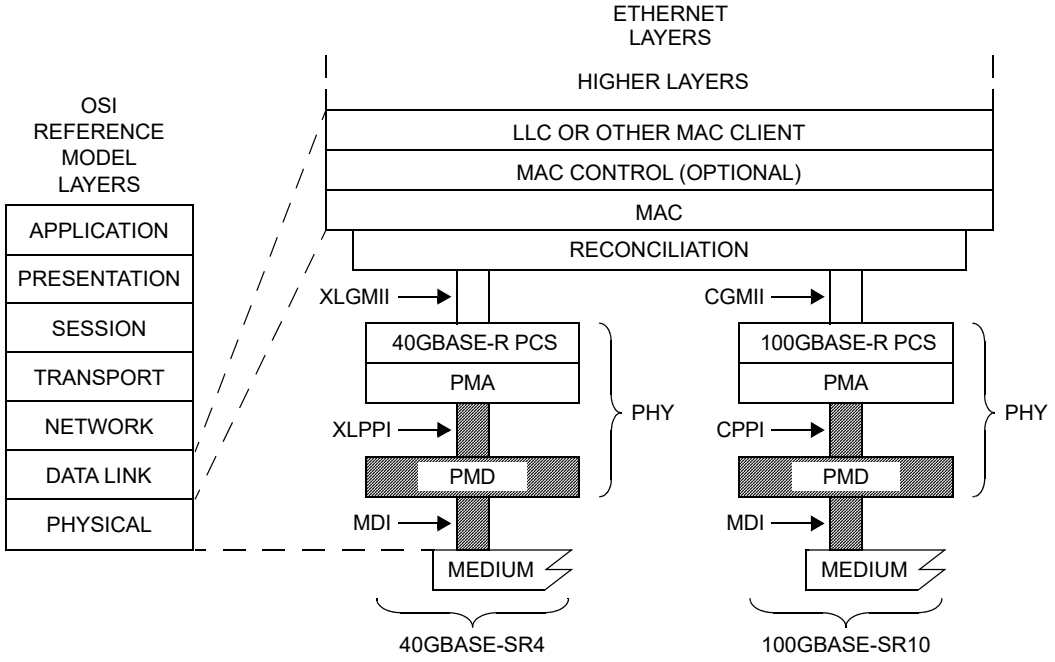

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
CPPI = 100 Gb/s PARALLEL PHYSICAL INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE
XLPPI = 40 Gb/s PARALLEL PHYSICAL INTERFACE
SR = PMD FOR MULTIMODE FIBER

Figure 86–1—40GBASE-SR4 and 100GBASE-SR10 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

The 40GBASE-SR4 and 100GBASE-SR10 PMD sublayers provide point-to-point 40 Gb/s and 100 Gb/s Ethernet links over four or ten pairs of multimode fiber, up to at least 100 m. Table 86–2 shows the primary attributes of each PMD type.

Table 86–2—Summary of 40GBASE–SR4 and 100GBASE–SR10

PMD Type	40GBASE–SR4	100GBASE–SR10	Unit
Fiber type	50/125 μm multimode, type A1a.2[a] (OM3) or A1a.3[b](OM4)		
Number of fiber pairs	4	10	
Nominal wavelength	850		nm
Required operating range	0.5 to 100 for OM3		m
	0.5 to 150 for OM4[c]		
Signaling rate, each lane	10.3125 ±100 ppm		GBd

[a] Type A1a.2 (OM3) specified in IEC 60793-2-10. See 86.10.2.1.
[b] Type A1a.3 (OM4) specified in IEC 60793-2-10. See 86.10.2.1.
[c] This is an engineered link with maximum 1 dB connection and splice loss.

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40GBASE–SR4 uses four identical lanes, while 100GBASE–SR10 uses ten of the same lanes. In this clause, where there are four or ten items (depending on PMD type) such as lanes, the items are numbered from 0 to $n - 1$, and an example item is numbered i. Thus n is 4 or 10.

The connection to the PMA may use the optional physical instantiation of the PMD service interface called XLPPI (four lanes, for 40GBASE-SR4) or CPPI (ten lanes, for 100GBASE-SR10). The term "nPPI" is used to denote either XLPPI or CPPI, or both.

This clause is arranged as follows: following the overview and an abstract description of the PMD service interface, delay and Skew specifications, control and status variables and registers, a block diagram and high-level specification of the PMD functions, and lane assignments, 86.7 (four parts) contains the optical specifications for 40GBASE-SR4 and 100GBASE-SR10. 86.8 defines test points and optical and dual-use parameters. 86.9 addresses safety, installation, environment and labeling, 86.10 defines the optical channel, and 86.11 contains the PICS. Annex 86A contains the electrical specifications for XLPPI and CPPI, electrical compliance boards, definitions of electrical parameters, and a recommended PCB response for the host (PMA).

40GBASE-SR4 and 100GBASE-SR10 PHYs with the optional Energy Efficient Ethernet (EEE) capability may enter the fast wake Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

86.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 40GBASE-SR4 and 100GBASE-SR10 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation, although an optional implementation of the PMD service interface, the Parallel Physical Interface (nPPI), is specified in 86A.4.1 and 86A.4.2. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 40GBASE-SR4 PMD has four parallel bit streams, hence $i = 0$ to 3 for 40GBASE-SR4 and the 100GBASE-SR10 PMD has ten parallel bit streams, hence $i = 0$ to 9 for 100GBASE-SR10.

The PMA (or the PMD) continuously sends four or ten parallel bit streams to the PMD (or the PMA), one per lane, each at a nominal signaling rate of 10.3125 GBd (see 83.4).

Upon receipt of the PMD:IS_UNITDATA_*i*.request primitive, the PMD converts the specified streams of bits into the appropriate signals on the MDI.

The PMD:IS_UNITDATA_*i*.indication primitive corresponds to one of the signals received from the MDI. This primitive is received by the client (the PMA), as described in 83.4.

The PMD:IS_SIGNAL.indication(SIGNAL_DETECT) primitive is generated by the PMD to report the parameter SIGNAL_DETECT, which indicates the status of the signals being received from the MDI (see 86.5.4). There is one parameter and primitive, reporting on all the lanes as a group. This primitive is received by the client (the PMA) as PMD:IS_SIGNAL.indication(SIGNAL_OK), as described in 83.4.

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NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_bit parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the 10^{-12} BER objective.

86.3 Delay and Skew

86.3.1 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the 40GBASE-SR4 PMD including 2 m of fiber in one direction shall be no more than 1024 bit times (2 pause_quanta or 25.6 ns). The sum of the transmit and receive delays at one end of the link contributed by the 100GBASE-SR10 PMD including 2 m of fiber in one direction shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

86.3.2 Skew and Skew Variation constraints

The Skew (relative delay) between the lanes is kept within limits so that the information on the lanes can be reassembled by the PCS. The Skew Variation is also limited to ensure that a given PCS lane always traverses the same physical lane. Skew and Skew Variation are defined in 80.5 and specified at the points SP1 to SP6 shown in Figure 80–7 and Figure 80–8. Skew points as they relate to the nPPI are shown in Figure 86–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5. The measurements of Skew and Skew Variation are defined in 86.8.3.1.

86.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If MDIO is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 86–3, and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 86–4.

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Table 86–3—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable 9[a]	PMD transmit disable register	1.9.10	PMD_transmit_disable_9
PMD transmit disable 8[a] to PMD transmit disable 0	PMD transmit disable register	1.9.9 to 1.9.1	PMD_transmit_disable_8 to PMD_transmit_disable_0

[a]For 40GBASE-SR4, the highest-numbered six of the ten lane-by-lane transmit disables do not apply.

Table 86–4—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect 9[a]	PMD receive signal detect register	1.10.10	PMD_signal_detect_9
PMD receive signal detect 8[a] to PMD receive signal detect 0	PMD receive signal detect register	1.10.9 to 1.10.1	PMD_signal_detect_8 to PMD_signal_detect_0

[a]For 40GBASE-SR4, the highest-numbered six of the ten lane-by-lane signal detects do not apply.

86.5 PMD functional specifications

The 40GBASE–SR4 and 100GBASE–SR10 PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

86.5.1 PMD block diagram

The PMD block diagram is shown in Figure 86–2. Figure 86–3 shows the test points. It is not required that the PMD service interface be exposed or measurable (nPPI as defined in Annex 86A with compliance points TP1, TP1a, TP4, TP4a). However, if it is not, a conforming implementation behaves as though the interface were compliant.

For purposes of system conformance, the PMD sublayer is standardized at the test points described in 86.8.1. The transmit side electrical signal (PMA output and PMD electrical input) is defined at TP1 and TP1a; see Annex 86A. The optical transmit signal is defined at the output end of a 50 μm multimode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all optical transmitter measurements and tests defined in 86.8 are made at TP2. The optical receive signal is defined at the output

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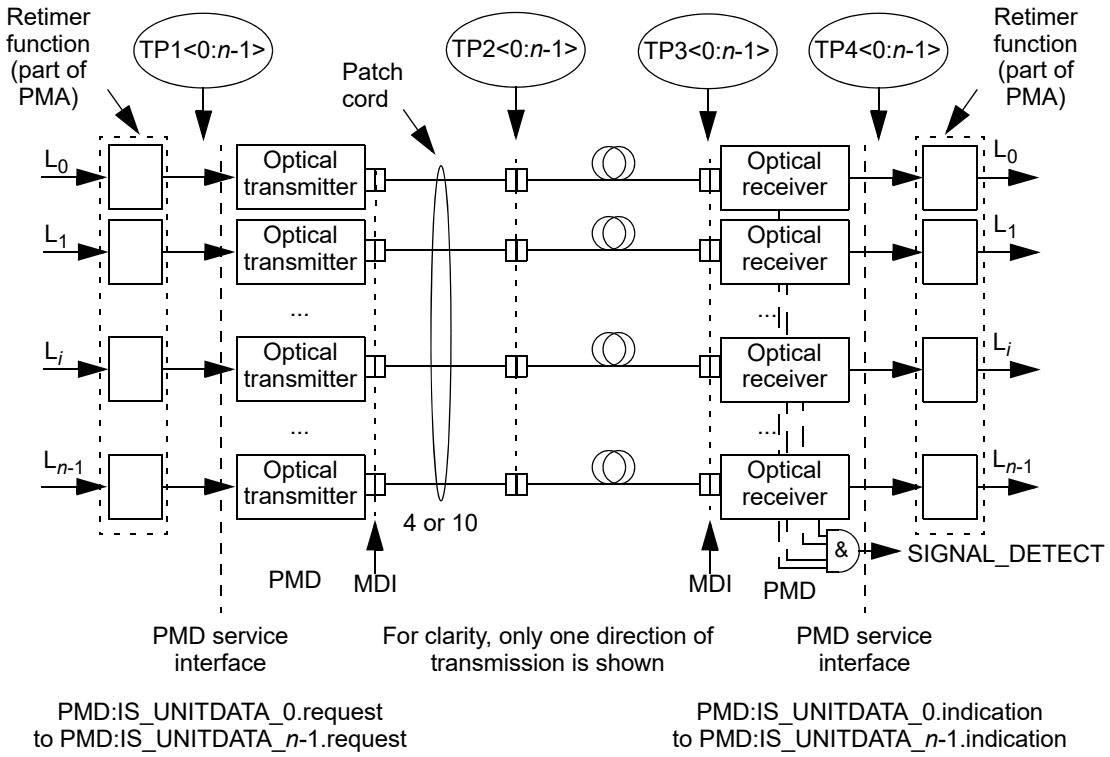

Figure 86–2—Block diagram for 40GBASE–SR4 and 100GBASE–SR10 transmit/receive paths

of the fiber optic cabling (TP3) at the MDI (see 86.10.3). Unless specified otherwise, all optical receiver measurements and tests defined in 86.8 are made at TP3. The receive side electrical signal (PMD electrical output and PMA input) is defined at TP4 and TP4a; see Annex 86A.

86.5.2 PMD transmit function

The PMD Transmit function shall convert the four or ten electronic bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_*n*-1.request into the same number of optical signals. The optical signals are delivered to the MDI, which contains four or ten parallel light paths for transmit, according to the transmit optical specifications in this clause. The higher optical power level in each signal shall correspond to tx_bit = one.

86.5.3 PMD receive function

The PMD Receive function shall convert the four or ten parallel optical signals received from the MDI into separate electronic bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_*n*-1.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to rx_bit = one.

86.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs.

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SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 86–5. The PMD receiver is not required to verify whether a compliant 40GBASE-SR4 or 100GBASE-SR10 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 86–5—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –30 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ Minimum OMA, each lane, in Table 86–7) and (compliant 40GBASE–SR4 or 100GBASE–SR10 signal input as appropriate)]	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

86.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:*n*-1, shall be continuously set in response to the optical signal on its associated lane, according to the requirements of Table 86–5.

86.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

86.5.7 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 86–6.
b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter in each lane.

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86.5.8 PMD lane-by-lane transmit disable function (optional)

The PMD lane-by-lane transmit disable function is optional and allows the optical transmitter in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:*n*-1) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 86–6.
b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the optical transmitter in each lane.

If the optional PMD lane-by-lane transmit disable function is not implemented in MDIO, an alternative method may be provided to independently disable each transmit lane.

86.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one. If the MDIO interface is implemented, PMD_fault shall be mapped to the PMA/PMD fault bit as specified in 45.2.1.2.3.

86.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to one. If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the PMA/PMD transmit fault bit as specified in 45.2.1.7.4.

86.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one. If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the PMA/PMD receive fault bit as specified in 45.2.1.7.5.

86.6 Lane assignments

There are no lane assignments (within a group of transmit or receive lanes) for 40GBASE-SR4 or 100GBASE-SR10. While it is expected that a PMD will map electrical lane *i* to optical lane *i* and vice versa, there is no need to define the physical ordering of the lanes, as the PCS is capable of receiving the lanes in any arrangement. The positioning of transmit and receive lanes at the MDI is specified in 86.10.3.

86.7 PMD to MDI specifications for 40GBASE-SR4 or 100GBASE-SR10

The required operating range for the 40GBASE–SR4 and 100GBASE–SR10 PMD is defined in Table 86–2. A compliant PMD operates on 50/125 μm multimode fibers according to the specifications of Table 86–14. A PMD which exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., operating at 125 m meets the operating range requirement of 0.5 m to 100 m). The signaling rate for a lane of a 40GBASE–SR4 or 100GBASE–SR10 PMD shall be as defined in Table 86–2. The optical signal at the transmit and receive side of the MDI is specified in 86.7.1 and 86.7.3. The range of optical signals within the optical medium is defined in 86.7.2, and an illustrative link power budget is provided in 86.7.4. Test points are defined in 86.8.1.

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86.7.1 Transmitter optical specifications

Each lane of a 40GBASE–SR4 or 100GBASE–SR10 optical transmitter shall meet the specifications of Table 86–6 per the definitions in 86.8.

Table 86–6—40GBASE–SR4 or 100GBASE–SR10 optical transmit characteristics

Description	Type	Value	Unit
Center wavelength	Range	840 to 860	nm
RMS spectral width[a]	Max	0.65	nm
Average launch power, each lane	Max	2.4	dBm
Average launch power, each lane	Min	–7.6	dBm
Optical Modulation Amplitude (OMA), each lane	Max	3	dBm
Optical Modulation Amplitude (OMA), each lane	Min	–5.6[b]	dBm
Difference in launch power between any two lanes (OMA)	Max	4	dB
Peak power, each lane	Max	4	dBm
Launch power in OMA minus TDP, each lane	Min	–6.5	dBm
Transmitter and dispersion penalty (TDP), each lane	Max	3.5	dB
Extinction ratio	Min	3	dB
Optical return loss tolerance	Max	12	dB
Encircled flux[c]		≥ 86% at 19 μm, ≤ 30% at 4.5 μm	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5×10^{-5} hits per sample	Spec values	0.23, 0.34, 0.43, 0.27, 0.35, 0.4	
Average launch power of OFF transmitter, each lane	Max	–30	dBm

[a] RMS spectral width is the standard deviation of the spectrum.
[b] Even if the TDP < 0.9 dB, the OMA (min) has to exceed this value.
[c] If measured into type A1a.2 or type A1a.3 50 μm fiber in accordance with IEC 61280-1-4:2009.

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86.7.2 Characteristics of signal within, and at the receiving end of, a compliant optical channel

Table 86–7 gives the characteristics of a signal within, and at the receiving end of, a lane of a compliant 40GBASE–SR4 or 100GBASE–SR10 optical channel, and the aggregate signal. A signal with power in OMA or average power not within the ranges given cannot be compliant. However, a signal with power values within the ranges is not necessarily compliant.

Table 86–7—Characteristics of signal within, and at the receiving end of, a compliant optical channel

Description	Minimum		Maximum	Unit
Fiber type	OM3	OM4		
Total average power for 40GBASE–SR4	–3.5	–3.1	+8.4	dBm
Total average power for 100GBASE–SR10	+0.5	+0.9	+12.4	dBm
Average power, each lane	–9.5	–9.1	+2.4	dBm
Optical Modulation Amplitude (OMA), each lane	–7.5	–7.1	+3	dBm

NOTE—Table 86–7 provides information for diagnostic purposes that is needed by network operators in maintenance. There is no need to assure compliance to it in normal circumstances.

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86.7.3 40GBASE-SR4 or 100GBASE-SR10 receiver optical specifications

Each lane of a 40GBASE–SR4 or 100GBASE–SR10 optical receiver shall meet the specifications defined in Table 86–8 per the definitions in 86.8.

Table 86–8—40GBASE-SR4 or 100GBASE-SR10 optical receiver characteristics

Description	Type	Value	Unit
Center wavelength, each lane	Range	840 to 860	nm
Damage threshold[a]	Min	+3.4	dBm
Average power at receiver input, each lane	Max	+2.4	dBm
	Min	–9.5	dBm
Receiver reflectance	Max	–12	dB
Optical Modulation Amplitude (OMA), each lane	Max	3	dBm
Stressed receiver sensitivity in OMA, each lane[b]	Max	–5.4	dBm
Peak power, each lane	Max	4	dBm
Conditions of stressed receiver sensitivity test:			
Vertical eye closure penalty (VECP)[c], each lane	—	1.9	dB
Stressed eye J2 Jitter[c], each lane	—	0.3	UI
Stressed eye J9 Jitter[c], each lane	—	0.47	UI
OMA of each aggressor lane	—	–0.4	dBm
Receiver jitter tolerance in OMA, each lane[d]	Max	–5.4	dBm
Conditions of receiver jitter tolerance test:			
Jitter frequency and peak-to-peak amplitude	—	(75, 5)	(kHz, UI)
Jitter frequency and peak-to-peak amplitude	—	(375, 1)	(kHz, UI)
OMA of each aggressor lane	—	–0.4	dBm

[a]The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
[b]Measured with conformance test signal at TP3 (see 86.8.4.7).
[c]Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver. The apparent discrepancy between VECP and TDP is because VECP is defined at eye center while TDP is defined with ±0.15 UI offsets of the sampling instant.
[d]This is a test of the optical receiver's ability to track low-frequency jitter and is inappropriate for any subsystem that does not include a CRU.

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86.7.4 40GBASE-SR4 or 100GBASE-SR10 illustrative link power budget

Illustrative power budgets and penalties for 40GBASE–SR4 or 100GBASE–SR10 optical channels are shown in Table 86–9.

Table 86–9—40GBASE–SR4 or 100GBASE–SR10 illustrative link power budgets

Parameter	OM3	OM4	Unit
Effective modal bandwidth at 850 nm[a]	2000	4700	MHz•km
Power budget (for maximum TDP)	8.3		dB
Operating distance	0.5 to 100	0.5 to 150	m
Channel insertion loss[b]	1.9	1.5	dB
Allocation for penalties (for maximum TDP)[c]	6.4	6.5	dB
Unallocated margin	0	0.3[d]	dB
Additional insertion loss allowed	0		dB

[a]Per IEC 60793-2-10.
[b] The channel insertion loss is calculated using the maximum distances specified in Table 86–2 and cabled optical fiber attenuation of 3.5 dB/km at 850 nm plus an allocation for connection and splice loss given in 86.10.2.2.1.
[c] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[d] This unallocated margin is not available for use.

86.8 Definitions of optical and dual-use parameters and measurement methods

In this section, the test points and the parameters applicable to optical signals and for dual use (both optical and electrical) are defined. Test points are defined in 86.8.1, test patterns in 86.8.2, and parameters in 86.8.3 and 86.8.4. Further parameters for electrical use, and the use of electrical compliance boards, are defined in 86A.5.

86.8.1 Test points and compliance boards

Figure 86–3 shows the six test points for 40GBASE-SR4 and 100GBASE-SR10. These are TP1, TP1a, TP2, TP3, TP4, and TP4a; four of these are Skew points SP2, SP3, SP4, and SP5 as shown. Figure 86–3 also shows the substitution of compliance boards for PMD or PMA. This is explained in Annex 86A. Table 86–10 shows the parameters or signals measured at each point, including the electrical compliance points.

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified. A patch cord that connects the MDI transmit side to 4 or 10 individual connectors may be suitable.

86.8.2 Test patterns and related subclauses

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 86–11 lists the defined test patterns, and Table 86–12 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. As Pattern 3 is more demanding than

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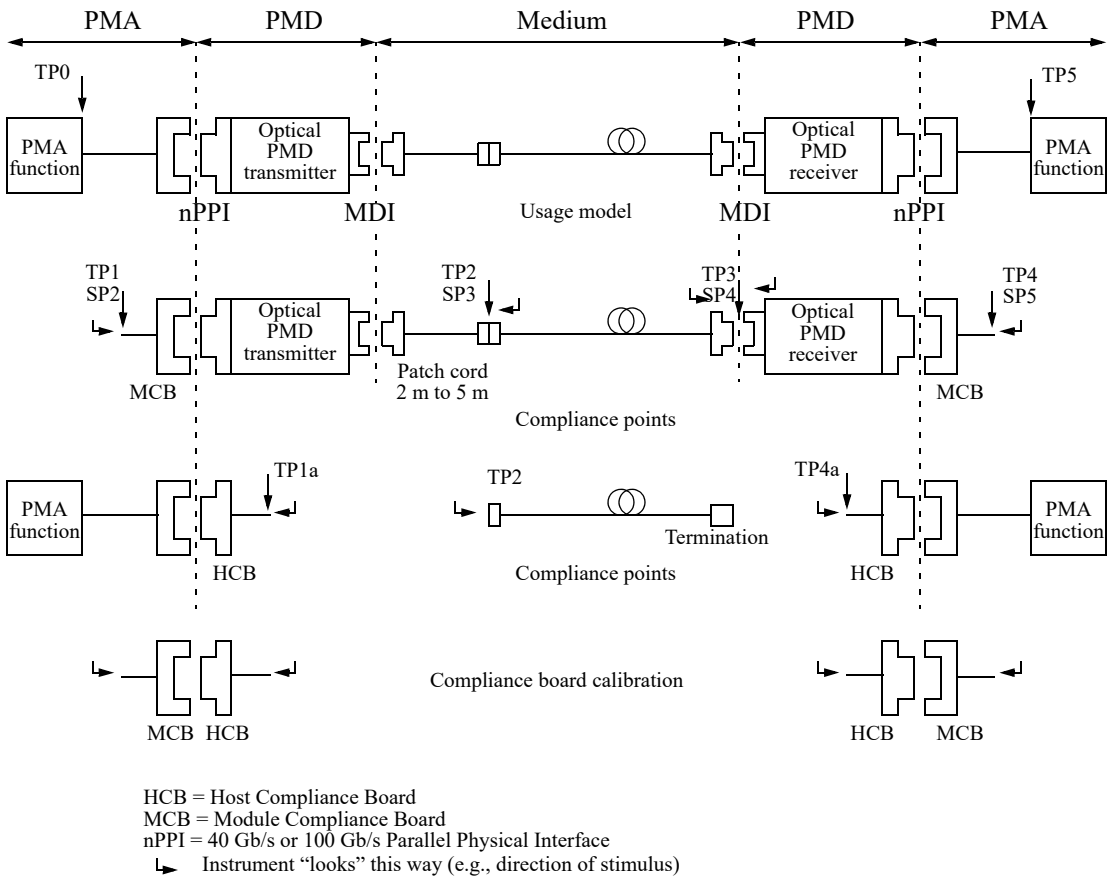

HCB = Host Compliance Board
MCB = Module Compliance Board
nPPI = 40 Gb/s or 100 Gb/s Parallel Physical Interface
↳ Instrument "looks" this way (e.g., direction of stimulus)

Figure 86–3—Test points for 40GBASE-SR4 and 100GBASE-SR10

Table 86–10—Parameters defined at each test point

Test point	Direction	Parameter
TP1	Looking downstream into PMD transmitter input	PMD transmitter input return loss
TP1a	Looking upstream into PMA transmitter output	PMA transmitter output signal and output return loss, PMD transmitter compliance signal calibration, PMA receiver compliance crosstalk signal calibration
TP2	Looking upstream into optical transmitter output	PMD transmitted signal, PMD transmitter reflectance
	Looking downstream into fiber	Optical return loss, connector reflections
TP3	Looking upstream into fiber	PMD receiver compliance signal
	Looking downstream into optical receiver input	PMD receiver reflectance
TP4	Looking upstream into PMD receiver output	PMD receiver output signal and output return loss, PMA receiver compliance signal calibration
TP4a	Looking downstream into PMA receiver input	PMA receiver input return loss

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Table 86–11—Test patterns

Pattern no.	Pattern	Pattern defined in
Square wave	Square wave (8 ones, 8 zeros)	83.5.10
3	PRBS31	83.5.10
4	PRBS9	83.5.10
5	Scrambled idle	82.2.11

Pattern 5 (which itself is the same or more demanding than other 40GBASE-R or 100GBASE-R bit streams) an item that is compliant using Pattern 5 is considered compliant even if it does not meet the required limit using Pattern 3. Test patterns for further electrical parameters are given in Table 86A–6.

Table 86–12—Test patterns and related subclauses

Parameter	Pattern	Related subclause
Wavelength, spectral width	3, 5, or valid 40GBASE-SR4 or 100GBASE-SR10 signal	86.8.4.1
Average optical power	3, 5, or valid 40GBASE-SR4 or 100GBASE-SR10 signal	86.8.4.2
Transmitter OMA (modulated optical power)	Square wave or 4	86.8.4.3
Extinction ratio	3, 5, or valid 40GBASE-SR4 or 100GBASE-SR10 signal	86.8.4.5
Transmitted optical waveform (eye mask)	3, 5, or valid 40GBASE-SR4 or 100GBASE-SR10 signal	86.8.3.2, 86.8.4.6
TDP (transmitter and dispersion penalty)	3 or 5	86.8.4.4
Stressed receiver sensitivity	3 or 5	86.8.4.7
Receiver jitter tolerance	3 or 5	86.8.4.8
Calibration of OMA for receiver tests	Square wave or 4	52.9.9
Vertical eye closure penalty calibration	3 or 5	52.9.9
J2 Jitter	3, 5, or valid 40GBASE-SR4 or 100GBASE-SR10 signal	86.8.3.3.1
J9 Jitter	3 or 5	86.8.3.3.2
Data Dependent Pulse Width Shrinkage (DDPWS)	4	86A.5.3.4

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Table 86–12—Test patterns and related subclauses *(continued)*

Parameter	Pattern	Related subclause
AC common-mode voltage	3, 5, or valid 40GBASE-SR4 or 100GBASE-SR10 signal	86A.5.3.1
Transition time	Square wave or 4	86A.5.3.3
Electrical waveform (eye mask)	3, 5, or valid 40GBASE-SR4 or 100GBASE-SR10 signal	86.8.3.2, 86A.5.3.6

86.8.2.1 Multi-lane testing considerations

TDP is defined for each lane, at a BER of 10^{-12} on that lane. Stressed receiver sensitivity, receiver jitter tolerance and host input signal tolerance (in Annex 86A) are defined for an interface BER of 10^{-12}. The interface BER is the average of the four or ten BERs of the receive lanes when they are stressed.

Measurements with Pattern 3 (PRBS31) allow lane-by-lane BER measurements. Measurements with Pattern 5 (scrambled idle) give the interface BER if all lanes are stressed at the same time. If each lane is stressed in turn, the BER is diluted by the three or nine unstressed lanes, and the BER for that stressed lane alone has to be found, e.g., by multiplying by 4 or 10 if the unstressed lanes have low BER. To allow TDP measurement with Pattern 5, unstressed lanes for the error detector may be created by setting the power at the reference receivers well above their sensitivities, or by copying the contents of the transmit lanes not under BER test to the error detector by other means. In stressed receiver sensitivity and receiver jitter tolerance measurements, unstressed lanes may be created by setting the power at the receiver under test well above its sensitivity and/or not stressing those lanes with ISI and jitter, or by other means. Each receive lane is stressed in turn while all are operated. All aggressor lanes are operated as specified. To find the interface BER, the BERs of all the lanes when stressed are averaged.

Where relevant, parameters are defined with all co-propagating and counter-propagating lanes operational so that crosstalk effects are included. Where not otherwise specified, the maximum amplitude (OMA or VMA) for a particular situation is used, and for counter-propagating lanes, the minimum transition time is used. Alternative test methods that generate equivalent results may be used. While the lanes in a particular direction may share a common clock, the Tx and Rx directions are not synchronous to each other. If Pattern 3 is used for the lanes not under test using a common clock, there is at least 31 UI delay between the PRBS31 patterns on one lane and any other lane.

86.8.3 Parameters applicable to both electrical and optical signals

86.8.3.1 Skew and Skew Variation

Skew and Skew Variation are defined in 80.5 and are required to remain within the limits given in 86.3.2 over the time that the link is in operation. Skew points as they relate to the nPPI are shown in Figure 86–3. The measurement of Skew and Skew Variation is made by acquiring the data on each lane using a clock and data recovery unit with a high-frequency corner bandwidth and slope as specified in 86.8.3.2. The arrival times of the one to zero transition of the alignment marker sync bits on each lane are then compared. This arrangement ensures that any high-frequency jitter that is present on the signals is not included in the Skew measurement.

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86.8.3.2 Eye diagrams

Eye diagrams can be used to assess both electrical and optical signals. The measurement of the electrical eye is defined in 86A.5.3.6 and the measurement of the optical transmitter waveform is defined in 86.8.4.6. Whether electrical or optical eye diagrams, all co-propagating and counter-propagating lanes are active as crosstalk sources, using one of patterns 3, 5, or a valid 40GBASE-R or 100GBASE-R signal. The input lanes of the item under test are receiving signals that are asynchronous to those being output.

Normalized times of 0 and 1 on the unit interval scale are determined by the eye crossing means measured at the average value of the eye pattern. A clock recovery unit (CRU) is used to trigger the oscilloscope for mask measurements, as shown in Figure 52–9. It has a high-frequency corner bandwidth of 4 MHz and a slope of –20 dB/decade. The CRU tracks acceptable levels of low-frequency jitter and wander.

Consideration should be given as to whether a correction is needed for actual instrument properties.

86.8.3.2.1 Eye mask acceptable hit count examples

An example calculation relating hit count to hit ratio for an eye mask measurement using an oscilloscope is detailed below.

If an oscilloscope records 1350 samples/screen, and the time-base is set to 0.2 UI per division with 10 divisions across the screen, and the measurement is continued for 200 waveforms, then a signal that averages less than 6.75 hits is compliant to a hit ratio specification of 5×10^{-5}, i.e.,

$$\frac{5 \times 10^{-5} \times 200 \times 1350}{0.2 \times 10} = 6.75 \tag{86–1}$$

Likewise, if a measurement is continued for 1000 waveforms, then an average of less than 33.75 hits is compliant. An extended measurement is expected to give a more accurate result, and a single reading of 6 hits in 200 waveforms would not give a statistically significant pass or fail.

The hit ratio limit has been chosen to avoid misleading results due to signal and oscilloscope noise.

86.8.3.3 Jitter

J2 Jitter and J9 Jitter are specified with all co-propagating and counter-propagating lanes active as crosstalk sources, using one of patterns 3, 5, or a valid 40GBASE-R or 100GBASE-R signal. The input lanes of the item under test are receiving signals that are asynchronous to those being output.

86.8.3.3.1 J2 Jitter

J2 Jitter is defined as the time interval that includes all but 10^{-2} of the jitter distribution, which is the time interval from the 0.5th to the 99.5th percentile of the jitter histogram. This may be measured using an oscilloscope, or if measured by plotting BER vs. decision time, J2 is the time interval between the two points with a BER of 2.5×10^{-3}. Oscilloscope histograms should include at least 10 000 hits, and should be taken over about 1% of the signal amplitude. Test patterns are given in Table 86–12.

86.8.3.3.2 J9 Jitter

J9 Jitter is defined as the time interval that includes all but 10^{-9} of the jitter distribution. If measured by plotting BER vs. decision time, it is the time interval between the two points with a BER of 2.5×10^{-10}. Test patterns are given in Table 86–12.

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86.8.4 Optical parameter definitions

86.8.4.1 Wavelength and spectral width

The wavelength and spectral width of each optical lane shall be within the range given in Table 86–6 if measured using the method given in the centroidal wavelength and RMS spectral width definitions in IEC 61280-1-3. The lane under test is modulated using the test pattern defined in Table 86–12.

86.8.4.2 Average optical power

Average optical power is defined by the methods given in IEC 61280-1-1.

86.8.4.3 Optical Modulation Amplitude (OMA)

OMA shall be as defined in 52.9.5 for measurement with a square wave (8 ones, 8 zeros) test pattern or 68.6.2 (from the variable MeasuredOMA in 68.6.6.2) for measurement with a PRBS9 test pattern, with the exception that each optical lane is tested individually. See 86.8.2 for test pattern information.

86.8.4.4 Transmitter and dispersion penalty (TDP)

Transmitter and dispersion penalty (TDP) shall be as defined for 10GBASE-S in 52.9.10 with the following exceptions:

a) Each optical lane is tested individually with all other lanes in operation.
b) The test pattern is as defined in Table 86–12.
c) The transmitter is tested using an optical channel with an optical return loss of 12 dB.
d) The reference receiver (including the effect of the decision circuit) has a fourth-order Bessel-Thomson filter response with a bandwidth of 6.1 GHz. The transversal filter of 52.9.10.3 is not used.
e) The reference sensitivity S and the measurement P_DUT are both measured with the sampling instant displaced from the eye center by ± 0.15 UI. For each of the two cases (early and late), if P_DUT(i) is larger than S(i), the TDP(i) for the transmitter under test is the difference between P_DUT(i) and S(i), TDP(i) = P_DUT(i) – S(i). Otherwise, TDP(i) = 0. The TDP is the larger of the two TDP(i).
f) The test setup illustrated in Figure 52–12 shows the reference method. Other measurement implementations may be used with suitable calibration.
g) The BER of 10^{-12} is for the lane under test on its own. See 86.8.2.1 for multi-lane pattern considerations.

NOTE—Because practical receivers and decision circuits have noise and timing impairments, the sampling instant offsets have to be calibrated. One method of doing this is via a jitter bathtub method using a known low-jitter signal.

86.8.4.5 Extinction ratio

Extinction ratio is defined by the methods of IEC 61280–2–2 using the test pattern defined in Table 86–12.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 86–12).

86.8.4.6 Transmitter optical waveform (transmit eye)

The required optical transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram specified in Table 86–6 and shown in Figure 86–4. The transmitter optical waveform of a port transmitting the test pattern specified in Table 86–12 shall meet specifications according

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to the methods specified in 86.8.4.6.1 with the filter nominal reference frequency f_r of 7.5 GHz and filter tolerances as specified for STM-64 in ITU-T G.691.

86.8.4.6.1 Optical transmitter eye mask

The eye is measured with respect to the mask specified in Table 86–6 and shown in Figure 86–4 using a receiver with the fourth-order Bessel-Thomson response having a transfer function given by Equation (86–2) and Equation (86–3):

$$H(y) = \frac{105}{105 + 105y + 45y^2 + 10y^3 + y^4} \tag{86–2}$$

where:

$$y = 2.114p\ ; \quad p = \frac{j\omega}{\omega_r}\ ; \quad \omega_r = 2\pi f_r\ ; \quad f_r = \text{Reference frequency in GHz} \tag{86–3}$$

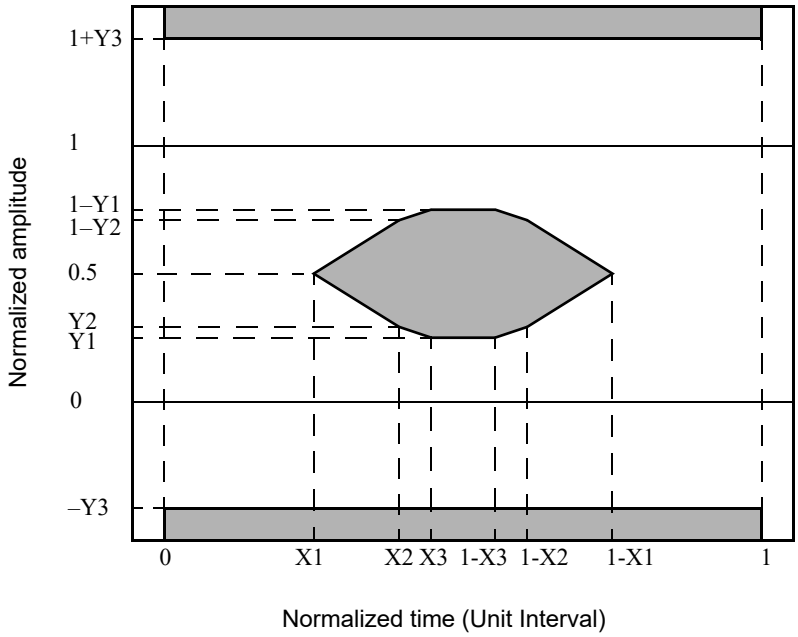

Figure 86–4—Transmitter eye mask definition

The Bessel-Thomson receiver is not intended to represent the noise filter used within a compliant optical receiver, but is intended to provide uniform measurement conditions at the transmitter. Compensation may be made for variation of the reference receiver filter response from an ideal fourth-order Bessel-Thomson response.

Normalized levels of 0 and 1 represent logic zero and one respectively. These are defined by the means of the lower and upper halves of the central 0.2 UI of the eye.

Further requirements are given in 86.8.3.2.

The transmitter shall achieve a hit ratio lower than the limit of hits per sample specified in the appropriate table or 5×10^{-5} hits per sample if not otherwise specified. “Hits” are the number of samples within the grey

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areas of Figure 86–4, and the sample count is the total number of samples from 0 UI to 1 UI. Some illustrative examples are provided in 86.8.3.2.1.

Further information on optical eye pattern measurement procedures may be found in IEC 61280-2-2.

86.8.4.7 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 86–8 if measured using the method defined by 52.9.9 with the conformance test signal at TP3 and with the following exceptions:

a) The reference test procedure for a single lane is defined in 52.9.9. See 86.8.2.1 and below for multi-lane considerations.
b) The sinusoidal amplitude interferer is replaced by a Gaussian noise generator.
c) The fourth-order Bessel-Thomson filter is replaced by a low-pass filter followed by a limiter and a fourth-order Bessel-Thomson filter.
d) The sinusoidal jitter is at a fixed 80 MHz frequency and between 0 and 0.05 UI peak-to-peak amplitude.
e) The Gaussian noise generator, the amplitude of the sinusoidal jitter, and the Bessel-Thomson filter are adjusted so that the VECP, J2 Jitter and J9 Jitter specifications given in Table 86–8 are simultaneously met (the random noise effects such as RIN, random clock jitter do not need to be minimized).
f) The pattern for the received compliance signal is specified in Table 86–12.
g) The interface BER of the PMD receiver is the average of the BER of all receive lanes while stressed and at the specified receive OMA.
h) Where nPPI or XLAUI/CAUI-n is exposed, a PMD receiver is considered compliant if it meets the module electrical output specifications at TP4 given in Table 86A–3 for nPPI, or the requirements in Table 83B–3 for XLAUI/CAUI-10, or the requirements in Table 83E–3 for CAUI-4.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Each receive lane is tested in turn while all aggressor receive lanes are operated as specified in Table 86–8. Pattern 3 or Pattern 5, or a valid 40GBASE–R4 or 100GBASE–R10 signal is sent from the transmit section of the receiver under test. The signal being transmitted is asynchronous to the received signal. If Pattern 3 is used for the transmit and receive lanes not under test, there is at least 31 UI delay between the PRBS31 patterns generated on one lane and any other lane.

For 40GBASE-SR4 and 100GBASE-SR10, the relevant BER is the interface BER. The interface BER is the average of the four or ten BERs of the receive lanes when stressed: see 86.8.2.1.

86.8.4.8 Receiver jitter tolerance

Receiver jitter tolerance shall be as defined as in 68.6.11, with the following differences:

a) The reference test procedure for a single lane is defined in 68.6.11. See 86.8.2.1 for multi-lane considerations.
b) The pattern to be received is specified in Table 86–12.
c) The parameters of the signal are specified in Table 86–8 and the power in OMA at the receiver is set to the maximum for receiver jitter tolerance in OMA given in Table 86–8.
d) Each receive lane is tested in turn while all are operated. All aggressor lanes are operated as specified in Table 86–8.
e) The receive lanes not being tested are receiving Pattern 3, Pattern 5, or a valid 40GBASE-R4 or 100GBASE-R10 signal.
f) The transmitter is transmitting one of these signals using all lanes.
g) The transmitter and the receiver are not synchronous.

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h) The interface BER of the PMD receiver is the average of the BER of all receive lanes when stressed.
i) The mode-conditioning patch cord suitable for 62.5/125 μm fiber is not used.

86.9 Safety, installation, environment, and labeling

86.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

86.9.2 Laser safety

40GBASE–SR4 and 100GBASE–SR10 optical transceivers shall conform to Hazard Level 1M laser requirements as defined in IEC 60825–1 and IEC 60825–2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[151]

86.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

86.9.4 Environment

The 40GBASE–SR4 and 100GBASE–SR10 operating environment specifications are as defined in 52.11, as defined in 52.11.1 for electromagnetic emission, and as defined in 52.11.2 for temperature, humidity, and handling.

86.9.5 PMD labeling

The 40GBASE–SR4 and 100GBASE–SR10 labeling recommendations and requirements are as defined in 52.12.

86.10 Optical channel

The fiber optic cabling (channel) contains 4 or 10 optical fibers for each direction to support 40GBASE-SR4 or 100GBASE-SR10, respectively. The fiber optic cabling interconnects the transmitters at the MDI on one end of the channel to the receivers at the MDI on the other end of the channel. As defined in 86.10.3, the optical lanes appear in defined locations at the MDI but the locations are not assigned specific lane numbers within this standard because any transmitter lane may be connected to any receiver lane. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term *channel* is used here for consistency with generic cabling standards.

[151] A host system that fails to meet the manufacturers requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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86.10.1 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 86–5.

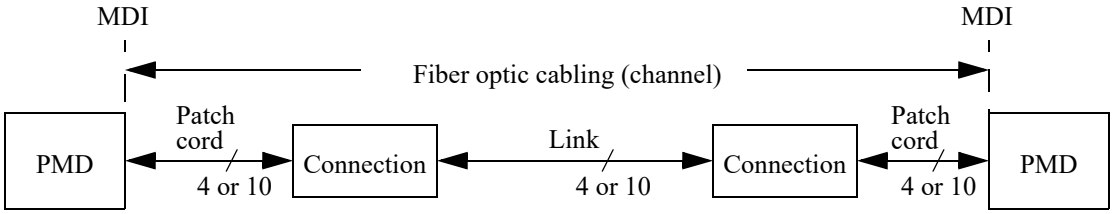

Figure 86–5—Fiber optic cabling model

The channel shall comply with the specifications in Table 86–13.

Table 86–13—Fiber optic cabling (channel) characteristics at 850 nm

Description	Type	OM3	OM4	Unit
Operating distance	Max	100	150	m
Cabling Skew	Max	79		ns
Cabling Skew Variation[a]	Max	2.2		ns
Channel insertion loss	Min	0		dB
Channel insertion loss[b]	Max	1.9[c]	1.5[d]	dB

[a] An additional 0.6 ns of Skew Variation could be caused by wavelength changes, which are attributable to the transmitter not the channel.
[b] These channel insertion loss values include cable, connectors, and splices.
[c] 1.5 dB allocated for connection and splice loss.
[d] 1 dB allocated for connection and splice loss.

A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, modal dispersion, reflections and losses of all connectors and splices meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1 one-cord method. As OM4 optical fiber meets the requirements for OM3, a channel compliant to the “OM3” column may use OM4 optical fiber, or a combination of OM3 and OM4.

86.10.2 Characteristics of the fiber optic cabling (channel)

86.10.2.1 Optical fiber cable

The fiber contained within the 40GBASE–SR4 or 100GBASE–SR10 fiber optic cabling shall comply with the specifications and parameters of Table 86–14. A variety of multimode cable types may satisfy these requirements, provided the resulting channel also meets the specifications of Table 86–13. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

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Table 86–14—Optical fiber and cable characteristics

Description	OM3[a]	OM4[b]	Unit
Nominal core diameter	50		μm
Nominal fiber specification wavelength	850		nm
Effective modal bandwidth (min)[c]	2000	4700	MHz•km
Cabled optical fiber attenuation (max)	3.5		dB/km
Zero dispersion wavelength (λ_0)	$1295 \le \lambda_0 \le 1340$		nm
Chromatic dispersion slope (max) (S_0)	0.105 for $1295 \le \lambda_0 \le 1310$ and $0.000375\times(1590 - \lambda_0)$ for $1310 \le \lambda_0 \le 1340$		$ps/nm^2\ km$

[a]IEC 60793-2-10 type A1a.2.
[b] IEC 60793-2-10 type A1a.3.
[c] When measured with the launch conditions specified in Table 86–6.

86.10.2.2 Optical fiber connection

An optical fiber connection, as shown in Figure 86–5, consists of a mated pair of optical connectors.

86.10.2.2.1 Connection insertion loss

The maximum operating distances are based on an allocation of 1.5 dB or 1 dB total connection and splice loss. For example, these allocations support two connections, each with an insertion loss of 0.75 dB or 0.5 dB respectively. Connections with lower loss characteristics may be used provided the requirements of Table 86–13 are met. However, the loss of a single connection shall not exceed 0.75 dB.

86.10.2.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –20 dB.

86.10.3 Medium Dependent Interface (MDI)

The 40GBASE–SR4 or 100GBASE–SR10 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 86–5). The 40GBASE–SR4 PMD is coupled to the fiber optic cabling through one connector plug into the MDI optical receptacle as shown in Figure 86–6. The 100GBASE–SR10 PMD is coupled to the fiber optic cabling through one or two connector plugs into the MDI optical receptacle(s), depending on choice of implementation, as shown in Figure 86–7. Example constructions of the MDI include the following:

a) PMD with a connectorized fiber pigtail plugged into an adapter;
b) PMD receptacle.

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86.10.3.1 Optical lane assignments for 40GBASE-SR4

The four transmit and four receive optical lanes of 40GBASE-SR4 shall occupy the positions depicted in Figure 86–6 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains eight active lanes within twelve total positions. The transmit optical lanes occupy the leftmost four positions. The receive optical lanes occupy the rightmost four positions. The four center positions are unused.

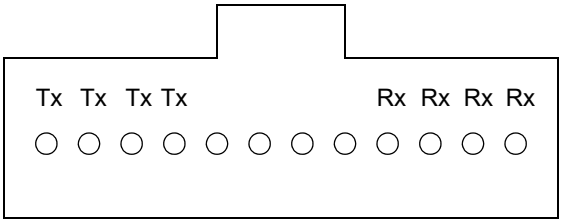

Figure 86–6—40GBASE-SR4 optical lane assignments

86.10.3.2 Optical lane assignments for 100GBASE-SR10

The ten transmit and ten receive optical lanes of 100GBASE-SR10 shall occupy the positions depicted in Figure 86–7 when looking into the MDI optical receptacle(s) with the connector keyway feature(s) on top. The single-receptacle Option A is recommended, the two-receptacle Option B and Option C are alternatives. The interface contains 20 active lanes within up to 24 total positions arranged in two rows of 10 or 12 positions. One row is dedicated to transmit optical lanes and the other row to receive optical lanes. For the depicted 12-position rows, the optical lanes occupy the center ten positions of each row with the outermost positions unused.

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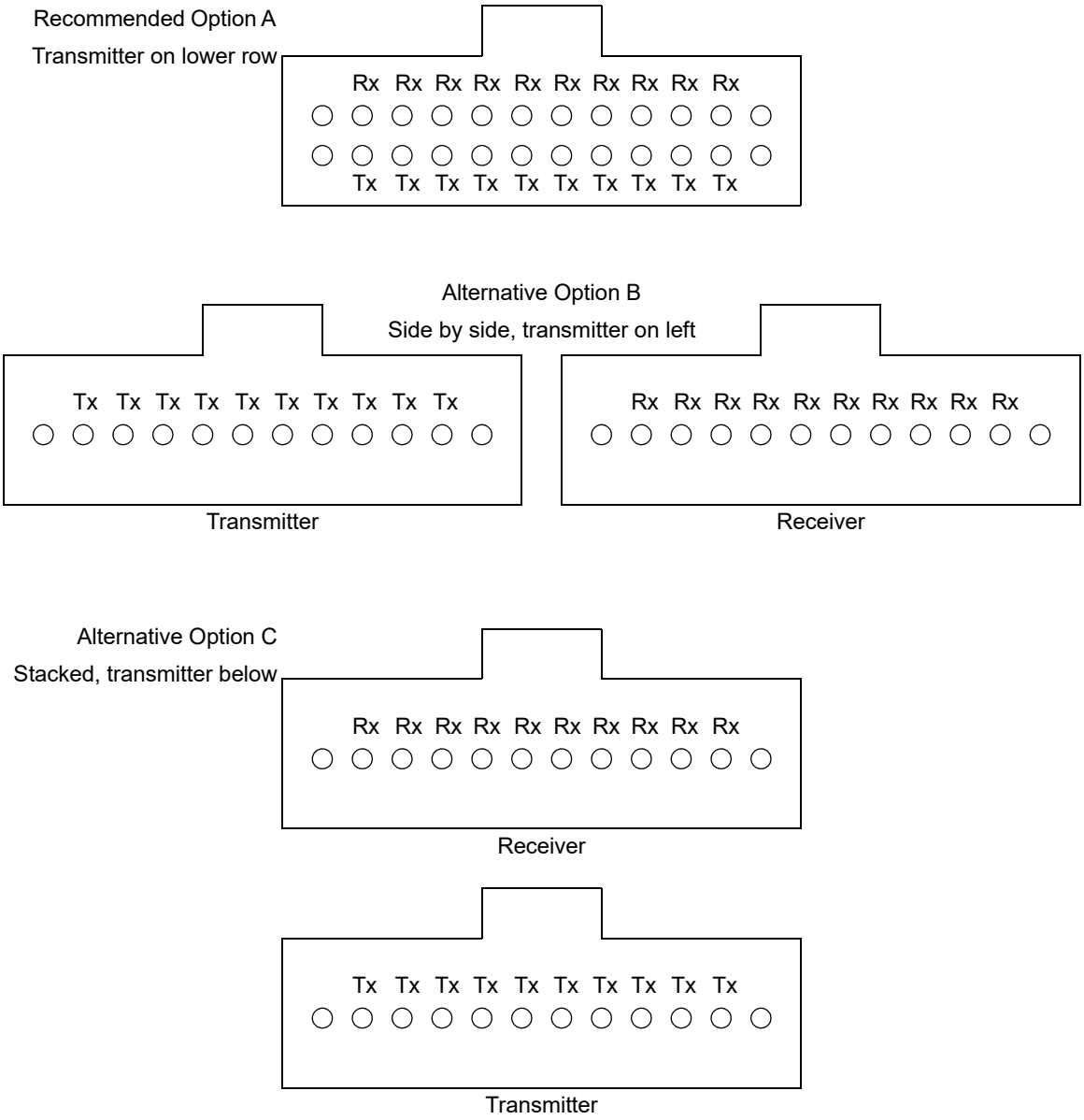

Figure 86–7—100GBASE-SR10 optical lane assignments

86.10.3.3 Medium Dependent Interface (MDI) requirements

The MDI adapter or receptacle shall meet the dimensional specifications of IEC 61754-7 interface 7-3, the MPO adapter interface. The plug terminating the optical fiber cabling shall meet the dimensional specifications of IEC 61754-7 interface 7-4, MPO female plug connector flat interface. The MDI shall optically mate with the plug on the optical fiber cabling. Figure 86–8 shows an MPO female plug connector with flat interface, and an MDI as a PMD receptacle using an MPO adapter interface.

The MDI shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-022-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 86.5.1, not at the MDI.

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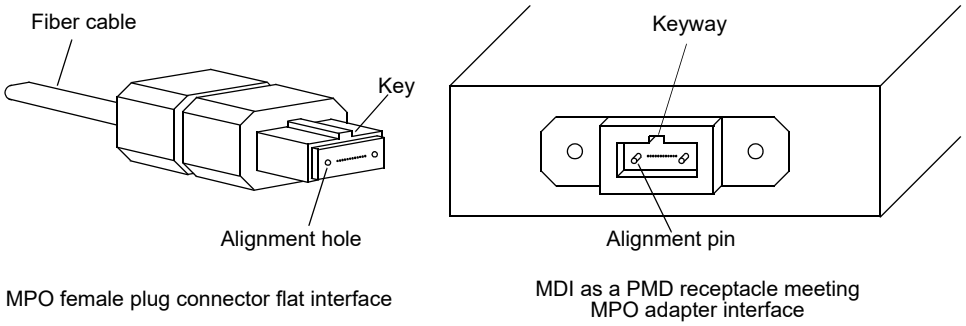

Figure 86–8—MPO female plug and MDI as a PMD receptacle using MPO adapter

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86.11 Protocol implementation conformance statement (PICS) proforma for Clause 86, Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-SR4 and 100GBASE-SR10[152]

86.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 86, Physical Medium Dependent sublayer and medium, type 40GBASE–SR4 and 100GBASE–SR10, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

86.11.2 Identification

86.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

86.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 86, Physical Medium Dependent sublayer and medium, type 40GBASE–SR4 and 100GBASE–SR10
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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86.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*SR4	40GBASE–SR4 PMD	86.7	Can operate as 40GBASE–SR4 PMD	O.1	Yes [ ] No [ ]
*SR10	100GBASE–SR10 PMD	86.7	Can operate as 100GBASE–SR10 PMD	O.1	Yes [ ] No [ ]
*INS	Installation / cable	86.10.1	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
*TP1	Compliance point TP1 exposed and available for testing	86.5.1	See text	O	Yes [ ] No [ ]
*TP4	Compliance point TP4 exposed and available for testing	86.5.1	See text	O	Yes [ ] No [ ]
*PIT	nPPI Tx interface	86.1	Uses XLPPI or CPPI host to module (see Annex 86A)	TP1:O	Yes [ ] No [ ] N/A [ ]
*PIR	nPPI Rx interface	86.1	Uses XLPPI or CPPI module to host (see Annex 86A)	TP4:O	Yes [ ] No [ ] N/A [ ]
*MD	MDIO capability	86.4	Registers and interface supported	O	Yes [ ] No [ ]

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86.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, types 40GBASE-SR4 and 100GBASE-SR10

86.11.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
SF1	Compatible with 40GBASE-R or 100GBASE-R PCS and PMA	86.1	See text	M	Yes [ ]
SF2	Integration with management functions	86.1	See text	O	Yes [ ] No [ ]
D	Delay constraints	86.3.1	For SR4, max 25.6 ns. For SR10, max 20.48 ns	M	Yes [ ]
SF3	Skew and Skew Variation at SP3 and SP4	86.3.2	At SP3, less than 54 ns, 600 ps. At SP4, less than 134 ns, 3.4 ns	M	Yes [ ]
SF4	Skew and Skew Variation at SP5 (TP4)	86.3.2	If measurable, less than 145 ns, 3.6 ns	TP4: M	Yes [ ] N/A [ ]
SF5	Transmit function	86.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
SF6	Delivery to the MDI	86.5.2	4 or 10 optical signals for delivery to the MDI	M	Yes [ ]
SF7	Mapping between optical signal and logical signal for transmitter	86.5.2	Higher optical power is a one	M	Yes [ ]
SF8	Receive function	86.5.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
SF9	Conversion of optical signals to electrical signals	86.5.3	For delivery to the PMD service interface	M	Yes [ ]
SF10	Mapping between optical signal and logical signal for receiver	86.5.3	Higher optical power is a one	M	Yes [ ]
SF11	Global Signal Detect function	86.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
SF12	Global Signal Detect behavior	86.5.4	Global indicator of the presence of optical signals on all lanes per Table 86–5	M	Yes [ ]
SF13	Lane-by-lane Signal Detect function	86.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per Table 86–5	MD:O	Yes [ ] No [ ] N/A [ ]
SF14	PMD_reset function	86.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

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86.11.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Management register set	86.4	See 86.4	MD:M	Yes [ ] N/A [ ]
SM2	Global transmit disable function	86.5.7	Disables all of the optical transmitters with Global_PMD_transmit_disable	MD:O	Yes [ ] No [ ] N/A [ ]
SM3	PMD lane-by-lane transmit disable function	86.5.8	Disables the optical transmitter on the lane associated with PMD_transmit_disable_*i*	MD:O	Yes [ ] No [ ] N/A [ ]
SM4	PMD lane-by-lane transmit disable	86.5.8	Disables each optical transmitter independently if MD = No	!MD:O	Yes [ ] No [ ] N/A [ ]
SM5	PMD_fault function	86.5.9	Sets PMD_fault to one if any local fault is detected	O	Yes [ ] No [ ]
SM6	PMD_fault mapping to MDIO	86.5.9	Mapped to PMA/PMD fault bit	SM5*MD:M	Yes [ ] N/A [ ]
SM7	PMD_transmit_fault function	86.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	O	Yes [ ] No [ ]
SM8	PMD_transmit_fault mapping to MDIO	86.5.10	Mapped to PMA/PMD transmit fault bit	SM7*MD:M	Yes [ ] N/A [ ]
SM9	PMD_receive_fault function	86.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	O	Yes [ ] No [ ]
SM10	PMD_receive_fault mapping to MDIO	86.5.11	Mapped to PMA/PMD receive fault bit	SM9*MD:M	Yes [ ] N/A [ ]

86.11.4.3 Optical specifications for 40GBASE-SR4 or 100GBASE-SR10

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Signaling rate per Table 86–2	86.7	10.3125 ±100 ppm	M	Yes [ ] N/A [ ]
S2	Optical transmitter meets specifications in Table 86–6	86.7.1	Per definitions in 86.8	M	Yes [ ] N/A [ ]
S3	Optical receiver meets specifications in Table 86–8	86.7.3	Per definitions in 86.8	M	Yes [ ] N/A [ ]

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86.11.4.4 Definitions of parameters and measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
SOM1	Measurement cable	86.8.1	2 m to 5 m in length	M	Yes [ ]
SOM2	Center wavelength and spectral width	86.8.4.1	Per the centroidal wavelength and RMS spectral width definitions in IEC 61280-1-3	M	Yes [ ]
SOM3	Average optical power	86.8.4.2	Per IEC 61280-1-1	M	Yes [ ]
SOM4	OMA measurements	86.8.4.3	Each lane, per methods of 52.9.5 or 68.6.2	M	Yes [ ]
SOM5	TDP	86.8.4.4	Each lane	M	Yes [ ]
SOM6	Extinction ratio	86.8.4.5	Per IEC 61280-2-2	M	Yes [ ]
SOM7	Transmit eye	86.8.4.6	Per 86.8.4.6.1 and 86.8.3.2, hit ratio lower than specified limit	M	Yes [ ]
SOM8	Stressed receiver conformance	86.8.4.7	See 86.8.4.7	M	Yes [ ]
SOM9	Receiver jitter tolerance	86.8.4.8	Per 68.6.11 as modified	M	Yes [ ]

86.11.4.5 Environmental and safety specifications

Item	Feature	Subclause	Value/Comment	Status	Support
SES1	General safety	86.9.1	Conforms to J.2	M	Yes [ ]
SES2	Laser safety	86.9.2	Conforms to Hazard Level 1M laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
SES3	Electromagnetic interference	86.9.4	As 52.11. Complies with codes for the limitation of electromagnetic interference	M	Yes [ ]

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86.11.4.6 Optical channel and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
SOC1	Fiber optic cabling	86.10.1	Specified in Table 86–13	INS:M	Yes [ ] N/A [ ]
SOC2	Optical fiber characteristics	86.10.2.1	Per Table 86–14	INS:M	Yes [ ] N/A [ ]
SOC3	Maximum loss per connection	86.10.2.2.1	0.75 dB	INS:M	Yes [ ] N/A [ ]
SOC4	Maximum discrete reflectance	86.10.2.2.2	Less than –20 dB	INS:M	Yes [ ] N/A [ ]
SOC5	40G MDI layout	86.10.3.1	Optical lane assignments per Figure 86–6	SR4:M	Yes [ ] N/A [ ]
SOC6	100G MDI layout	86.10.3.2	Optical lane assignments per Figure 86–7	SR10:M	Yes [ ] N/A [ ]
SOC7	MDI dimensions	86.10.3.3	Per IEC 61754-7 interface 7-3	M	Yes [ ]
SOC8	Cabling connector dimensions	86.10.3.3	Per IEC 61754-7 interface 7-4	INS:M	Yes [ ] N/A [ ]
SOC9	MDI mating	86.10.3.3	MDI optically mates with plug on the cabling	M	Yes [ ]
SOC10	MDI requirements	86.10.3.3	Meets IEC 61753-1-1 and IEC 61753-022-2	M INS:M	Yes [ ] N/A [ ]

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87. Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-LR4 and 40GBASE-ER4

87.1 Overview

This clause specifies the 40GBASE-LR4 PMD and the 40GBASE-ER4 PMD together with the single-mode fiber medium. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 87–1, to the medium through the MDI and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 87–1—Physical Layer clauses associated with the 40GBASE-LR4 and 40GBASE-ER4 PMDs

Associated clause	40GBASE-LR4	40GBASE-ER4
81—RS	Required	Required
81—XLGMII[a]	Optional	Optional
82—PCS for 40GBASE-R	Required	Required
83—PMA for 40GBASE-R	Required	Required
83A—XLAUI	Optional	Optional
83B—Chip-to-module XLAUI	Optional	Optional
86A—XLPPI	Optional	Not applicable
78—Energy Efficient Ethernet	Optional	Optional

[a]The XLGMII is an optional interface. However, if the XLGMII is not implemented, a conforming implementation behaves functionally as though the RS and XLGMII were present.

Figure 87–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 40 Gb/s and 100 Gb/s Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2.

40GBASE-LR4 and 40GBASE-ER4 PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

87.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 40GBASE-LR4 and 40GBASE-ER4 PMDs. The service interface for these PMDs are described in an abstract manner and do not imply any particular implementation, although an optional implementation of the PMD service interface, the 40 Gb/s Parallel Physical Interface (XLPPI), is specified in Annex 86A. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

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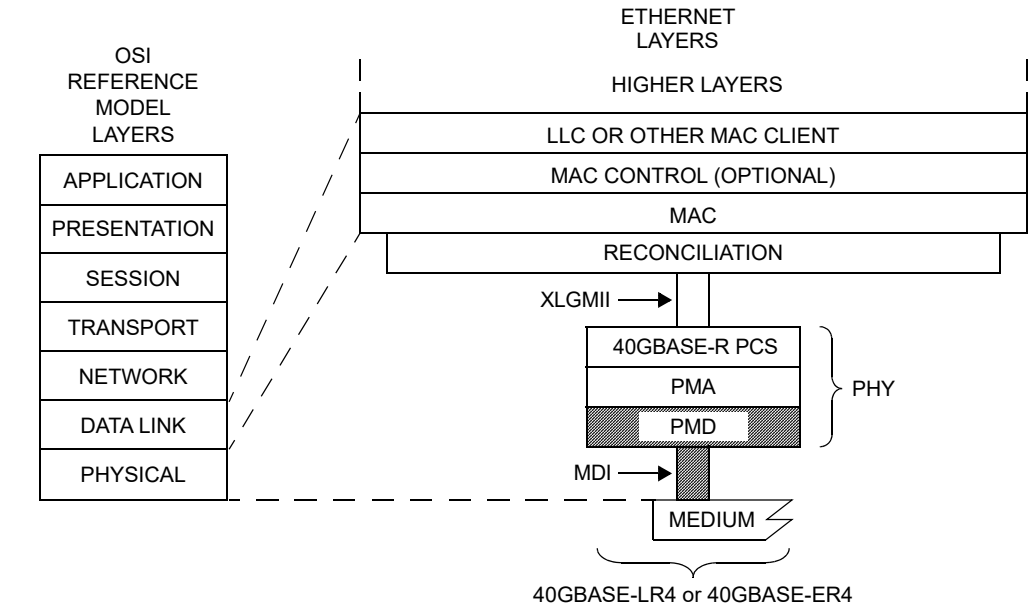

LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

LR = PMD FOR SINGLE-MODE FIBER — 10 km
ER = PMD FOR SINGLE-MODE FIBER — 40 km

Figure 87–1—40GBASE-LR4 and 40GBASE-ER4 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

The PMD service interface is an instance of the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 40GBASE-LR4 and 40GBASE-ER4 PMDs have four parallel bit streams, hence $i = 0$ to 3.

In the transmit direction, the PMA continuously sends four parallel bit streams to the PMD, one per lane, each at a nominal signaling rate of 10.3125 GBd. The PMD converts these streams of bits into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends four parallel bit streams to the PMA corresponding to the signals received from the MDI, one per lane, each at a nominal signaling rate of 10.3125 GBd.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication(SIGNAL_OK) inter-sublayer service primitive defined in 80.3.

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_bit parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_bit parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the 10^{-12} BER objective.

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87.3 Delay and Skew

87.3.1 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the 40GBASE-LR4 or 40GBASE-ER4 PMD including 2 m of fiber in one direction shall be no more than 1024 bit times (2 pause_quanta or 25.6 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

87.3.2 Skew constraints

The Skew (relative delay) between the lanes is kept within limits so that the information on the lanes can be reassembled by the PCS. The Skew Variation is also limited to ensure that a given PCS lane always traverses the same physical lane. Skew and Skew Variation are defined in 80.5 and specified at the points SP1 to SP6 shown in Figure 80–7 and Figure 80–8.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5. The measurements of Skew and Skew Variation are defined in 87.8.2.

87.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 87–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 87–3.

87.5 PMD functional specifications

The 40GBASE-LR4 and 40GBASE-ER4 PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

87.5.1 PMD block diagram

The PMD block diagram is shown in Figure 87–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 87.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 87.11.3). Unless specified otherwise, all receiver measurements and tests defined in 87.8 are made at TP3.

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Table 87–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable 3	PMD transmit disable register	1.9.4	PMD_transmit_disable_3
PMD transmit disable 2	PMD transmit disable register	1.9.3	PMD_transmit_disable_2
PMD transmit disable 1	PMD transmit disable register	1.9.2	PMD_transmit_disable_1
PMD transmit disable 0	PMD transmit disable register	1.9.1	PMD_transmit_disable_0

Table 87–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect 3	PMD receive signal detect register	1.10.4	PMD_signal_detect_3
PMD receive signal detect 2	PMD receive signal detect register	1.10.3	PMD_signal_detect_2
PMD receive signal detect 1	PMD receive signal detect register	1.10.2	PMD_signal_detect_1
PMD receive signal detect 0	PMD receive signal detect register	1.10.1	PMD_signal_detect_0

TP1<0:3> and TP4<0:3> are optional reference points that may be useful to implementers for testing components (these test points will not typically be accessible in an implemented system).

87.5.2 PMD transmit function

The PMD Transmit function shall convert the four bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request into four separate optical signals. The four optical signals shall then be wavelength division multiplexed and delivered to the MDI, all according to the transmit optical specifications in this clause. The higher optical power level in each signal shall correspond to tx_bit = one.

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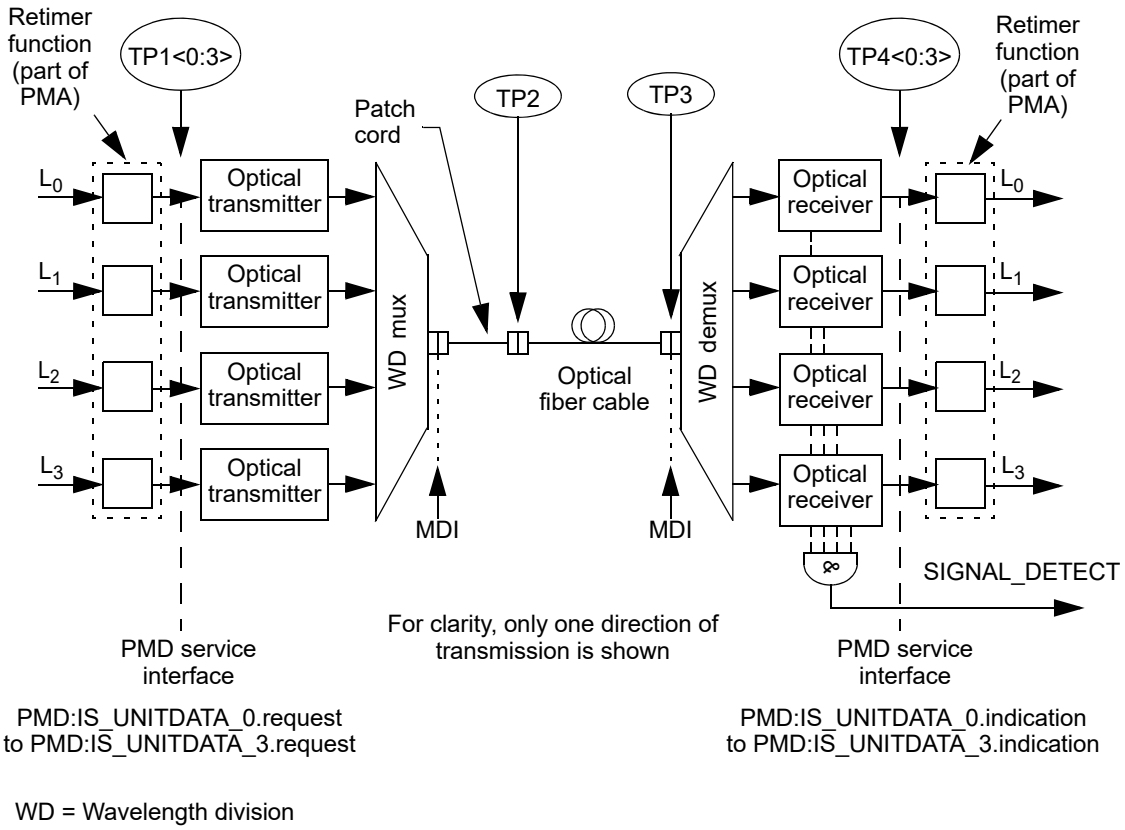

NOTE—Specification of the retimer function is beyond the scope of this standard.

Figure 87–2—Block diagram for 40GBASE-LR4 and 40GBASE-ER4 transmit/receive paths

87.5.3 PMD receive function

The PMD Receive function shall demultiplex the composite optical signal received from the MDI into four separate optical signals. The four optical signals shall then be converted into four bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to rx_bit = one.

87.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 80.3.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all four lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 87–4. The PMD receiver is not required to verify whether a compliant 40GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

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Table 87–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –30 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ receiver sensitivity (max) in OMA in Table 87–8) AND (compliant 40GBASE–R signal input)]	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

87.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:3, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 87–4.

87.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

87.5.7 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 87–7.
b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter in each lane.

87.5.8 PMD lane-by-lane transmit disable function

The PMD lane-by-lane transmit disable function is optional and allows the optical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:3) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 87–7.

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b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the optical transmitter in each lane.

If the optional PMD lane-by-lane transmit disable function is not implemented in MDIO, an alternative method shall be provided to independently disable each transmit lane for testing purposes.

87.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one. If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

87.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to one. If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

87.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one. If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

87.6 Wavelength-division-multiplexed lane assignments

The wavelength range for each lane of the 40GBASE-LR4 and 40GBASE-ER4 PMDs is defined in Table 87–5. The center wavelengths are members of the CWDM wavelength grid defined in ITU-T G.694.2 and are spaced at 20 nm.

Table 87–5—Wavelength-division-multiplexed lane assignments

Lane	Center wavelength	Wavelength range
L_0	1271 nm	1264.5 to 1277.5 nm
L_1	1291 nm	1284.5 to 1297.5 nm
L_2	1311 nm	1304.5 to 1317.5 nm
L_3	1331 nm	1324.5 to 1337.5 nm

NOTE—There is no requirement to associate a particular electrical lane with a particular optical lane, as the PCS is capable of receiving lanes in any arrangement.

87.7 PMD to MDI optical specifications for 40GBASE-LR4 and 40GBASE-ER4

The operating range for the 40GBASE-LR4 and 40GBASE-ER4 PMDs are defined in Table 87–6. A 40GBASE-LR4 or 40GBASE-ER4 compliant PMD operates on type B1.1, B1.3 or B6_a single-mode fibers according to the specifications defined in Table 87–14. A PMD that exceeds the required operating range

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while meeting all other optical specifications is considered compliant (e.g., a 40GBASE-LR4 PMD operating at 12.5 km meets the operating range requirement of 2 m to 10 km).

The 40GBASE-ER4 PMD interoperates with the 40GBASE-LR4 PMD provided that the channel requirements defined in 87.12 are met.

Table 87–6—40GBASE-LR4 and 40GBASE-ER4 operating ranges

PMD type	Required operating range
40GBASE-LR4	2 m to 10 km
40GBASE-ER4	2 m to 30 km
	2 m to 40 km[a]

[a]Links longer than 30 km for the same link power budget are considered engineered links. Attenuation for such links needs to be less than the worst case specified for B1.1, B1.3, or B6_a single-mode fiber.

87.7.1 40GBASE-LR4 and 40GBASE-ER4 transmitter optical specifications

The 40GBASE-LR4 transmitter shall meet the specifications defined in Table 87–7 per the definitions in 87.8. The 40GBASE-ER4 transmitter shall meet the specifications defined in Table 87–7 per the definitions in 87.8.

Table 87–7—40GBASE-LR4 and 40GBASE-ER4 transmit characteristics

Description	40GBASE-LR4	40GBASE-ER4	Unit
Signaling rate, each lane (range)	10.3125 ± 100 ppm		GBd
Lane wavelengths (range)	1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5		nm
Side-mode suppression ratio (SMSR), (min)	30		dB
Total average launch power (max)	8.3	10.5	dBm
Average launch power, each lane (max)	2.3	4.5	dBm
Average launch power, each lane[a] (min)	–7	–2.7	dBm
Optical Modulation Amplitude (OMA), each lane (max)	3.5	5	dBm
Optical Modulation Amplitude (OMA), each lane (min)[b]	–4	0.3	dBm
Difference in launch power between any two lanes (OMA) (max)	6.5	4.7	dB
Launch power in OMA minus TDP, each lane (min)	–4.8	–0.5	dBm
Transmitter and dispersion penalty (TDP), each lane (max)	2.6		dB

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Table 87–7—40GBASE-LR4 and 40GBASE-ER4 transmit characteristics *(continued)*

Description	40GBASE-LR4	40GBASE-ER4	Unit
Average launch power of OFF transmitter, each lane (max)	–30		dBm
Extinction ratio (min)	3.5	5.5	dB
$RIN_{20}OMA$ (max)	–128		dB/Hz
Optical return loss tolerance (max)	20		dB
Transmitter reflectance[c] (max)	–12		dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}		

[a]Average launch power, each lane (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]Even if the TDP < 0.8 dB, the OMA (min) has to exceed this value.
[c]Transmitter reflectance is defined looking into the transmitter.

87.7.2 40GBASE-LR4 and 40GBASE-ER4 receive optical specifications

The 40GBASE-LR4 receiver shall meet the specifications defined in Table 87–8 per the definitions in 87.8.
The 40GBASE-ER4 receiver shall meet the specifications defined in Table 87–8 per the definitions in 87.8.

Table 87–8—40GBASE-LR4 and 40GBASE-ER4 receive characteristics

Description	40GBASE-LR4	40GBASE-ER4	Unit
Signaling rate, each lane (range)	10.3125 ± 100 ppm		GBd
Lane wavelengths (range)	1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5		nm
Damage threshold[a] (min)	3.3	3.8	dBm
Average receive power, each lane (max)	2.3	–4.5	dBm
Average receive power, each lane[b] (min)	–13.7	–21.2	dBm
Receive power, each lane (OMA) (max)	3.5	–4	dBm
Difference in receive power between any two lanes (OMA) (max)	7.5	7	dB
Receiver reflectance (max)	–26		dB
Receiver sensitivity (OMA), each lane[c] (max)	–11.5	–19	dBm
Receiver 3 dB electrical upper cutoff frequency, each lane (max)	12.3		GHz
Stressed receiver sensitivity (OMA), each lane[d] (max)	–9.6	–16.8	dBm

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Table 87–8—40GBASE-LR4 and 40GBASE-ER4 receive characteristics *(continued)*

Description	40GBASE-LR4	40GBASE-ER4	Unit
Conditions of stressed receiver sensitivity test:			
Vertical eye closure penalty,[e] each lane	1.9	2.2	dB
Stressed eye J2 Jitter,[e] each lane	0.3		UI
Stressed eye J9 Jitter,[e] each lane	0.47		UI

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
[b]Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity (OMA), each lane (max) is optional.
[d]Measured with conformance test signal at TP3 (see 87.8.11) for BER = 10^{-12}.
[e]Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

87.7.3 40GBASE-LR4 and 40GBASE-ER4 illustrative link power budgets

Illustrative power budgets and penalties for 40GBASE-LR4 and 40GBASE-ER4 channels are shown in Table 87–9.

Table 87–9—40GBASE-LR4 and 40GBASE-ER4 illustrative link power budgets

Parameter	40GBASE-LR4	40GBASE-ER4		Unit
Power budget (for max TDP)	9.3	21.1		dB
Operating distance	10	30	40[a]	km
Channel insertion loss	6.7[b]	16.5[b]	18.5[a]	dB
Maximum discrete reflectance	–26	–26		dB
Allocation for penalties[c] (for max TDP)	2.6	2.6		dB
Additional insertion loss allowed	0	2	0	dB

[a]Links longer than 30 km are considered engineered links. Attenuation for such links needs to be less than the worst case for B1.1, B1.3, or B6_a single-mode cabled optical fiber.
[b]The channel insertion loss is calculated using the maximum distance specified in Table 87–6 and cabled optical fiber attenuation of 0.47 dB/km at 1264.5 nm plus an allocation for connection and splice loss given in 87.11.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

87.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

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87.8.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 87–11 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 87–11 may be used to perform that test. The test patterns used in this clause are shown in Table 87–10.

Table 87–10—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 ones, 8 zeros)	83.5.10
3	PRBS31	83.5.10
4	PRBS9	83.5.10
5	Scrambled idle	82.2.11

Table 87–11—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	3, 5 or valid 40GBASE-LR4 or 40GBASE-ER4 signal	87.8.3
Side mode suppression ratio	3, 5 or valid 40GBASE-LR4 or 40GBASE-ER4 signal	87.8.3
Average optical power	3, 5 or valid 40GBASE-LR4 or 40GBASE-ER4 signal	87.8.4
Optical modulation amplitude (OMA)	Square wave or 4	87.8.5
Transmitter and dispersion penalty (TDP)	3 or 5	87.8.6
Extinction ratio	3, 5 or valid 40GBASE-LR4 or 40GBASE-ER4 signal	87.8.7
$RIN_{20}OMA$	Square wave or 4	87.8.8
Transmitter optical waveform	3, 5 or valid 40GBASE-LR4 or 40GBASE-ER4 signal	87.8.9
Stressed receiver sensitivity	3 or 5	87.8.11
Calibration of OMA for receiver tests	Square wave or 4	87.8.11
Vertical eye closure penalty calibration	3 or 5	87.8.11
Receiver 3 dB electrical upper cutoff frequency	3, 5 or valid 40GBASE-LR4 or 40GBASE-ER4 signal	87.8.12

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87.8.2 Skew and Skew Variation

Skew and Skew Variation are defined in 80.5 and are required to remain within the limits given in 87.3.2 over the time that the link is in operation. The measurement of Skew and Skew Variation is made by separating optical lanes with an optical demultiplexer and then acquiring the data on each lane using clock and data recovery units with high-frequency corner bandwidths as specified in 86.8.3.2 and a slope of –20 dB/decade. The arrival times of the one to zero transition of the alignment marker sync bits on each lane are then compared. This arrangement ensures that any high frequency jitter that is present on the signals is not included in the Skew measurement.

87.8.3 Wavelength and side mode suppression ratio (SMSR)

The wavelength and SMSR of each optical lane shall be within the ranges given in Table 87–5 if measured per IEC 61280-1-3. The lane under test is modulated using the test pattern defined in Table 87–11.

87.8.4 Average optical power

The average optical power of each lane shall be within the limits given in Table 87–7 if measured using the methods given in IEC 61280-1-1, with the sum of the optical power from all of the lanes not under test below –30 dBm, per the test setup in Figure 53–6.

87.8.5 Optical Modulation Amplitude (OMA)

OMA shall be as defined in 52.9.5 for measurement with a square wave (8 ones, 8 zeros) test pattern or 68.6.2 (from the variable MeasuredOMA in 68.6.6.2) for measurement with a PRBS9 test pattern, with the exception that each lane may be tested individually with the sum of the optical power from all of the lanes not under test being below –30 dBm, or if other lanes are operating, a suitable optical filter may be used to separate the lane under test.

87.8.6 Transmitter and dispersion penalty

Transmitter and dispersion penalty (TDP) shall be as defined in 52.9.10 with the exception that each optical lane is tested individually using an optical filter to separate the lane under test from the others. The measurement procedure for 40GBASE-LR4 and 40GBASE-ER4 is detailed in 87.8.6.1 to 87.8.6.4.

The optical filter passband ripple shall be limited to 0.5 dB peak-to-peak and the isolation is chosen such that the ratio of the power in the lane being measured to the sum of the powers of all of the other lanes is greater than 20 dB (see ITU-T G.959.1 Annex B). The lanes not under test shall be operating with PRBS31 or valid 40GBASE-R bit streams.

87.8.6.1 Reference transmitter requirements

The reference transmitter is a high-quality instrument-grade device that can be implemented by a CW laser modulated by a high-performance modulator. The basic requirements are as follows:

a) Rise/fall times of less than 25 ps at 20% to 80%.
b) The output optical eye is symmetric and passes the transmitter optical waveform test of 87.8.9.
c) In the center 20% region of the eye, the worst-case vertical eye closure penalty as defined in 52.9.9.2 is less than 0.5 dB.
d) Total Jitter less than 0.2 UI peak-to-peak.
e) RIN of less than –136 dB/Hz.

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87.8.6.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 87–12.

Table 87–12—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]
	Minimum	Maximum		
40GBASE-LR4	$0.2325 \times \lambda \times [1 - (1324 / \lambda)^4]$	$0.2325 \times \lambda \times [1 - (1300 / \lambda)^4]$	Minimum	20 dB
40GBASE-ER4	$0.93 \times \lambda \times [1 - (1324 / \lambda)^4]$	$0.93 \times \lambda \times [1 - (1300 / \lambda)^4]$	Minimum	20 dB

[a]The dispersion is measured for the wavelength of the device under test (λ in nm). The coefficient assumes 10 km for 40GBASE-LR4 and 40 km for 40GBASE-ER4.
[b]There is no intent to stress the sensitivity of the BERT's optical receiver.
[c]The optical return loss is applied at TP2.

A 40GBASE-LR4 or 40GBASE-ER4 transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 87–12 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss specified in Table 87–12. The state of polarization of the back reflection is adjusted to create the greatest RIN.

87.8.6.3 Reference receiver requirements

The reference receiver is required to have the bandwidth given in 87.8.9. The sensitivity of the reference receiver is limited by Gaussian noise. The receiver has minimal threshold offset, deadband, hysteresis, baseline wander, deterministic jitter, or other distortions. Decision sampling has minimal uncertainty and setup/hold times.

The nominal sensitivity of the reference receiver, S, is measured in OMA using the setup of Figure 52–12 without the test fiber and with the transversal filter removed. The sensitivity S has to be corrected for any significant reference transmitter impairments including any vertical eye closure. It is measured while sampling at the eye center or corrected for off-center sampling. It is calibrated at the wavelength of the transmitter under test.

For all transmitter and dispersion penalty measurements, determination of the center of the eye is required. Center of the eye is defined as the time halfway between the left and right sampling points within the eye where the measured BER is greater than or equal to 1×10^{-3}.

The clock recovery unit (CRU) used in the TDP measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low-frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.

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87.8.6.4 Test procedure

The test procedure is as defined in 52.9.10.4 with the exception that all lanes are operational in both directions (transmit and receive), each lane is tested individually using an optical filter to separate the lane under test from the others, and the BER of 1×10^{-12} is for the lane under test on its own.

87.8.7 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 87–7 if measured using the methods specified in IEC 61280-2-2, with the sum of the optical power from all of the lanes not under test below –30 dBm. The extinction ratio is measured using the test pattern defined in Table 87–11.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 87–11).

87.8.8 Relative Intensity Noise ($RIN_{20}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 20 dB.
b) Each lane may be tested individually with the sum of the optical power from all of the lanes not under test being below –30 dBm, or if other lanes are operating, a suitable optical filter may be used to separate the lane under test.
c) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 10.3 GHz).

87.8.9 Transmitter optical waveform (transmit eye)

The required optical transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 86–4. The transmitter optical waveform of a port transmitting the test pattern specified in Table 87–11 shall meet specifications according to the methods specified in 86.8.4.6.1 with the filter nominal reference frequency f_r of 7.5 GHz and filter tolerances as specified for STM-64 in ITU-T G.691. Compensation may be made for variation of the reference receiver filter response from an ideal fourth-order Bessel-Thomson response.

87.8.10 Receiver sensitivity

Receiver sensitivity, which is defined for an ideal input signal, is optional and compliance is not required. If measured, the test signal should have negligible impairments such as intersymbol interference (ISI), rise/fall times, jitter, and RIN. Instead, the normative requirement for receivers is stressed receiver sensitivity.

87.8.11 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 87–8 if measured using the method described in 87.8.11.1 and 87.8.11.5 with the conformance test signal at TP3 as described in 87.8.11.2. The BER is required to be met for the lane under test on its own.

For each lane, the stressed receiver sensitivity is defined with the transmit section in operation on all four lanes and with the receive lanes not under test also in operation. Pattern 3 or Pattern 5, or a valid 40GBASE-R signal, is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal.

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87.8.11.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 87–3. The patterns used for testing the receiver are specified in Table 87–11. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 87.8.11.2, and has sinusoidal jitter applied as specified in 87.8.11.4. A suitable test set is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics.

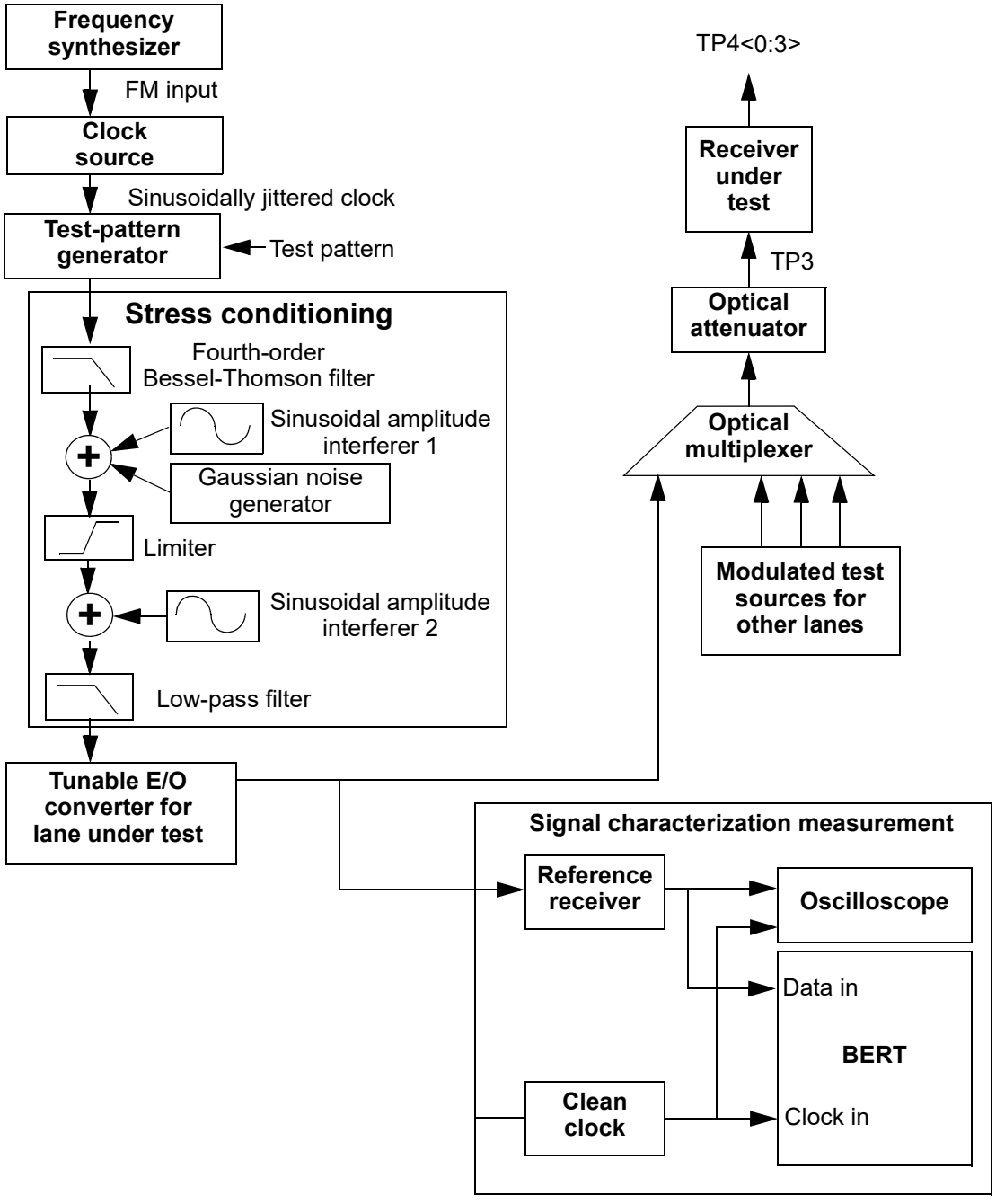

Figure 87–3—Stressed receiver conformance test block diagram

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The low-pass filter is used to create ISI-induced vertical eye closure penalty (VECP). The low-pass filter, when combined with the E/O converter, should have a frequency response that results in the appropriate level of initial vertical eye closure before the sinusoidal terms are added.

The sinusoidal amplitude interferer 1 causes jitter that is intended to emulate instantaneous bit shrinkage that can occur with DDJ. This type of jitter cannot be created by simple phase modulation. The sinusoidal amplitude interferer 2 causes additional eye closure, but in conjunction with the finite edge rates from the limiter, also causes some jitter. The sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferers may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferers, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The Gaussian noise generator, the amplitude of the sinusoidal interferers, and the low-pass filter are adjusted so that the VECP, stressed eye J2 Jitter, and stressed eye J9 Jitter specifications are met simultaneously.

For improved visibility for calibration, all elements in the signal path (cables, DC blocks, E/O converter, etc.) should have wide and smooth frequency response, and linear phase response, throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be minimized.

The stressed receiver conformance signal verification is described in 87.8.11.3.

87.8.11.2 Stressed receiver conformance test signal characteristics and calibration

The conformance test signal is used to validate that the PMD receiver of the lane under test meets BER requirements with near worst-case waveforms at TP3.

The primary parameters of the conformance test signal are vertical eye closure penalty (VECP), stressed eye J2 Jitter, and stressed eye J9 Jitter. VECP is measured at the time center of the eye (halfway between 0 and 1 on the unit interval scale as defined in 52.9.7). Stressed eye J2 Jitter is defined in 86.8.3.3.1 and stressed eye J9 Jitter is defined in 86.8.3.3.2. The values of these components are defined by their histogram results, as measured at the average optical power, which can be obtained with AC-coupling.

The vertical eye closure penalty is given by Equation (87–1).

$$\text{Vertical eye closure penalty} = 10\log_{10}\frac{OMA}{A_O} \quad \text{(dB)} \tag{87–1}$$

where

A_O is the amplitude of the eye opening from the 99.95th percentile of the lower histogram to the 0.05th percentile of the upper histogram

OMA is the optical modulation amplitude as defined in 87.8.5

An example stressed receiver conformance test setup is shown in Figure 87–3; however, any approach that modulates or creates the appropriate levels and frequencies of the VECP and jitter components is acceptable.

Residual low-probability noise and jitter should be minimized so that the outer slopes of the final amplitude histograms are as steep as possible.

The following steps describe a possible method for setting up and calibrating a stressed eye conformance signal when using a stressed receiver conformance test setup as shown in Figure 87–3:

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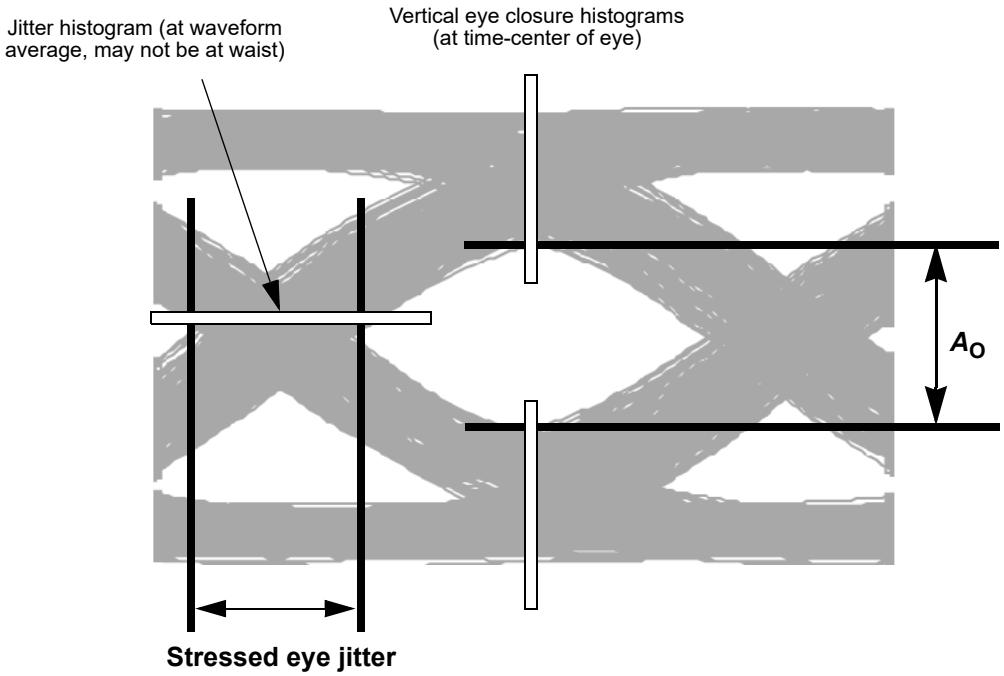

Figure 87–4—Required characteristics of the conformance test signal at TP3

1) Set the signaling rate of the test-pattern generator to meet the requirements in Table 87–8.
2) With sinusoidal interferers and sinusoidal jitter turned off, set the extinction ratio of the E/O to approximately the minimum specified in Table 87–7.
3) The required values of vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter of the stressed receiver conformance signal are given in Table 87–8.

   With the sinusoidal interferers and sinusoidal jitter turned off, greater than two thirds of the dB value of the VECP should be created by the selection of the appropriate bandwidth for the low-pass filter. Any remaining VECP has to be created with sinusoidal interferer 2 or sinusoidal jitter.

   The sinusoidal amplitude interferers may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferers, the sinusoidal jitter, the signaling rate and the pattern repetition rate.

   Sinusoidal jitter is added as specified in Table 87–13. When calibrating the conformance signal, the sinusoidal jitter frequency should be well within the 4 MHz to 10 times LB as defined in Table 87–13 and illustrated in Figure 87–5.

   Iterate the adjustments of sinusoidal interferers and Gaussian noise generator until the values of VECP, stressed eye J2 Jitter and stressed eye J9 Jitter meet the requirements in Table 87–8, and sinusoidal jitter above 4 MHz is as specified in Table 87–13. The resulting stressed eye conformance signal is required to have at least 0.05 UI of pulse width shrinkage.

Figure 87–3 shows the stress conditioned signal being applied to a tunable E/O converter. However, any optical source may be used that can meet the OMA and wavelength requirements for the lane under test as described in 87.8.11.5. Similarly, the other test sources that supply modulated signals to the other lanes may use any tunable or fixed sources that meet the OMA and wavelength requirements described in 87.8.11.5.

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Each receiver lane is conformance tested in turn. The source for the lane under test is adjusted to supply a signal at the input to the receiver under test at the stressed receiver sensitivity OMA specified in Table 87–8, and the test sources for the other lanes are set to the required OMA and wavelength as described in 87.8.11.5.

87.8.11.3 Stressed receiver conformance test signal verification

The stressed receiver conformance test signal can be verified using an optical reference receiver with an ideal fourth-order Bessel-Thomson response with a reference frequency f_r of 7.5 GHz. Use of G.691 tolerance filters may significantly degrade this calibration. The clock output from the clock source in Figure 87–3 will be modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye J2 Jitter and stressed eye J9 Jitter that includes the sinusoidal jitter component, a separate clock source (clean clock of Figure 87–3) is required that is synchronized to the source clock, but not modulated with the jitter source.

Care should be taken when characterizing the test signal because excessive noise/jitter in the measurement system will result in an input signal that does not fully stress the receiver under test. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. Care should be taken to minimize the noise/jitter introduced by the reference O/E, filters, and BERT and/or to correct for this noise. While the details of a BER scan measurement and test equipment are beyond the scope of this standard, it is recommended that the implementer fully characterize the test equipment and apply appropriate guard bands to ensure that the stressed receiver conformance input signal meets the stress and sinusoidal jitter specified in 87.8.11.2 and 87.8.11.4.

87.8.11.4 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table 87–13 and is illustrated in Figure 87–5.

Table 87–13—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter, peak-to-peak (UI)
$f < 40$ kHz	Not specified
40 kHz $< f \leq 4$ MHz	2×10^5 Hz / f
4 MHz $< f <$ 10 LB[a]	0.05

[a] LB = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

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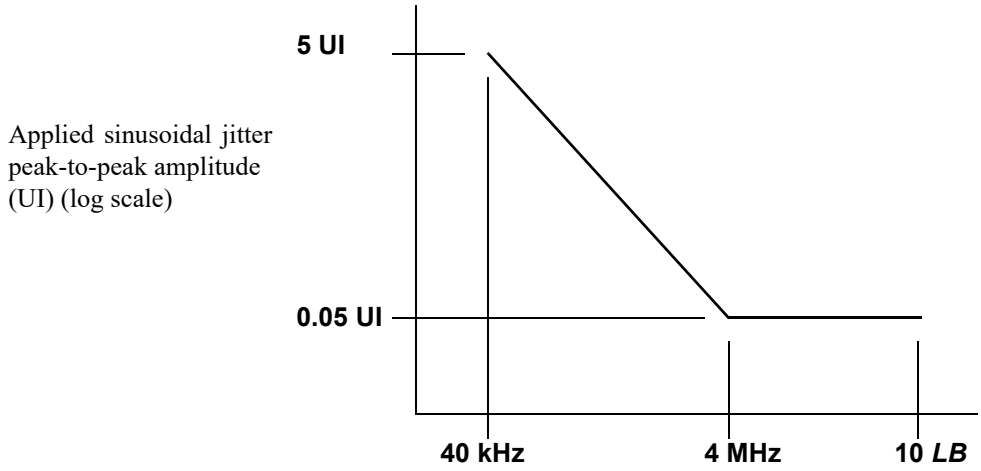

Figure 87–5—Illustration of the mask of the sinusoidal component of jitter tolerance

87.8.11.5 Stressed receiver conformance test procedure for WDM conformance testing

The receiver tests requiring the TP3 conformance test signal are performed on a per lane basis. For each lane, the stressed receiver sensitivity is defined with the transmit section in operation on all four lanes and with the receive lanes not under test also in operation. Pattern 3 or Pattern 5, or a valid 40GBASE-R signal is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal. All test sources are modulated simultaneously, using valid 40GBASE-R signals. The transmitter of the transceiver under test is operating with test patterns as defined in Table 87–11.

A rigorous method for testing WDM conformance using tunable test sources is described as follows:

a) The OMAs of the test sources in the lanes other than the lane under test are set to the highest OMA relative to the test source in the lane under test allowed by the “difference in receive power between any two lanes (OMA) (max)” parameter in Table 87–8.
b) The test sources in the lanes other than the lane under test are tuned to wavelengths within their wavelength range corresponding to the worst-case crosstalk to the lane under test.
c) The test source for the lane under test is tuned to the wavelength within its wavelength range corresponding to the worst-case sensitivity for the receiver under test.

It is recognized that a test setup that uses multiple tunable sources, while allowing rigorous worst-case measurements to be made, is likely to be onerous in practice.

A more practical, alternative method for testing WDM conformance is described below. The alternative WDM conformance test avoids the need for tunable sources but may result in some over-stressing of the receiver under test:

1) The test sources in each lane can be at any wavelength within each lane’s wavelength range.
2) The OMAs of the test sources in the lanes other than the lane under test are set to the highest OMA relative to the test source in the lane under test allowed by the “difference in receive power between any two lanes (OMA) (max)” parameter in Table 87–8, plus an increment corresponding to insertion loss variation within the lane under test (NOTE 1), plus an increment corresponding to the isolation variation of the lane in question (NOTE 2).

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NOTE 1—The increment corresponding to the variation of insertion loss with wavelength within the lane under test is equal to the dB variation of measured receiver sensitivity as the test source wavelength is swept across the wavelength range of the lane under test.

NOTE 2—For each of the test sources in the lanes not under test, an increment corresponding to the isolation variation is applied that is equal to the dB variation in optical crosstalk measured in the lane under test as the wavelength of each test source in the lanes not under test is swept across its respective wavelength range.

There are many ways to determine the size of the increments required, two example methods are given in the paragraphs that follow. Note that each lane will have one insertion loss variation value, and three values of optical crosstalk variation (one for each of the other lanes).

Example method 1: If a measure of the received signal strength is available for each lane, scan a tunable laser across the wavelength range of each lane while simultaneously recording the received signal in all lanes. As the laser sweeps across the wavelength range of a particular lane the dB variation in observed signal in that lane is equal to the insertion loss variation. The dB variation in signal observed in each of the other lanes is equal to the optical crosstalk variation.

Example method 2: If a discrete optical demultiplexer and discrete receivers are used, scan a tunable laser across the wavelength range of each channel while simultaneously recording the optical power of all four demultiplexer outputs. As the laser sweeps across the wavelength range of a particular channel, the dB variation in observed optical power in that lane's output is equal to the insertion loss variation. The dB variation in optical power observed in each of the other lanes outputs is equal to the optical crosstalk variation.

87.8.12 Receiver 3 dB electrical upper cutoff frequency

The receiver 3 dB electrical upper cutoff frequency shall be within the limits given in Table 87–8 if measured as described in 52.9.11. Each optical lane is measured using an optical signal or signals with its/their wavelength within the specified wavelength range of the lane to be tested. The test may use an electrical combiner and one optical source as in 53.9.13.

87.9 Safety, installation, environment, and labeling

87.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

87.9.2 Laser safety

40GBASE-LR4 and 40GBASE-ER4 optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[153]

[153]A host system that fails to meet the manufacturers requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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87.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

87.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 40GBASE-LR4 or 40GBASE-ER4 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

87.9.4.1 Electromagnetic emission

A system integrating a 40GBASE-LR4 or 40GBASE-ER4 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

87.9.4.2 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

87.9.5 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 40GBASE-LR4).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 87.9.2.

87.10 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 87–6.

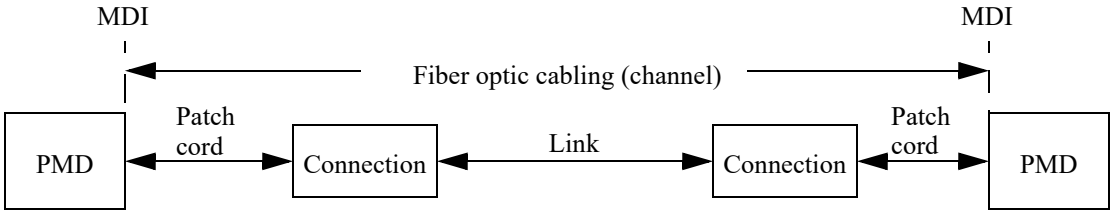

Figure 87–6—Fiber optic cabling model

The channel insertion loss is given in Table 87–14. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode

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dispersion meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 87–14—Fiber optic cabling (channel) characteristics

Description	40GBASE-LR4	40GBASE-ER4		Unit
Operating distance (max)	10	30	40	km
Channel insertion loss[a, b](max)	6.7	18.5		dB
Channel insertion loss (min)	0	9		dB
Positive dispersion[b] (max)	33.5	100.5	134	ps/nm
Negative dispersion[b] (min)	–59.5	–178.5	–238	ps/nm
DGD_max[c]	10	12		ps
Optical return loss (min)	21	21		dB

[a]These channel insertion loss values include cable, connectors, and splices.
[b]Over the wavelength range 1264.5 nm to 1337.5 nm.
[c]Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

87.11 Characteristics of the fiber optic cabling (channel)

The 40GBASE-LR4 and 40GBASE-ER4 fiber optic cabling shall meet the specifications defined in Table 87–14. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

87.11.1 Optical fiber cable

The fiber optic cable requirements are satisfied by cables containing IEC 60793-2-50 type B1.1 (dispersion un-shifted single-mode), type B1.3 (low water peak single-mode), or type B6_a (bend insensitive) fibers or the requirements in Table 87–15 where they differ.

Table 87–15—Optical fiber and cable characteristics

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.47[a] or 0.5[b]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \leq \lambda_0 \leq 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a]The 0.47 dB/km at 1264.5 nm attenuation for optical fiber cables is derived from Appendix I of ITU-T G.695.
[b]The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3. Using 0.5 dB/km may not support operation at 10 km for 40GBASE-LR4 or 40 km for 40GBASE-ER4.

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87.11.2 Optical fiber connection

An optical fiber connection, as shown in Figure 87–6, consists of a mated pair of optical connectors.

87.11.2.1 Connection insertion loss

The maximum link distances for single-mode fiber are calculated based on an allocation of 2 dB total connection and splice loss. For example, this allocation supports four connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 87–14 are met.

87.11.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –26 dB.

87.11.3 Medium Dependent Interface (MDI) requirements

The 40GBASE-LR4 or 40GBASE-ER4 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 87–6). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 87.5.1, not at the MDI.

87.12 Requirements for interoperation between 40GBASE-LR4 and 40GBASE-ER4

The 40GBASE-LR4 and 40GBASE-ER4 PMDs can interoperate with each other (over an engineered link) provided that the fiber optic cabling (channel) characteristics for 40GBASE-LR4 given in Table 87–14 are met, with the exception of the maximum and minimum channel insertion loss values, which are given in Table 87–16 for the two link directions separately.

Table 87–16—Channel insertion loss requirements for interoperation

Direction	Min loss	Max loss	Unit
40GBASE-LR4 Transmitter to 40GBASE-ER4 Receiver	7.5	14.2	dB
40GBASE-ER4 Transmitter to 40GBASE-LR4 Receiver	2.2	11	dB

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87.13 Protocol implementation conformance statement (PICS) proforma for Clause 87, Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-LR4 and 40GBASE-ER4[154]

87.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 87, Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-LR4 and 40GBASE-ER4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

87.13.2 Identification

87.13.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

87.13.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 87, Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-LR4 and 40GBASE-ER4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[154]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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87.13.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*LR4	40GBASE-LR4 PMD	87.7	Device supports requirements for 40GBASE-LR4 PHY	O.1	Yes [ ] No [ ]
*ER4	40GBASE-ER4 PMD	87.7	Device supports requirements for 40GBASE-ER4 PHY	O.1	Yes [ ] No [ ]
*INS	Installation/cable	87.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
XLTP1	Reference point TP1 exposed and available for testing	87.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
XLTP4	Reference point TP4 exposed and available for testing	87.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
XLDC	Delay constraints	87.3.1	Device conforms to delay constraints	M	Yes [ ]
XLSC	Skew constraints	87.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	87.4	Registers and interface supported	O	Yes [ ] No [ ]

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87.13.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-LR4 and 40GBASE-ER4

87.13.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
XLF1	Compatible with 40GBASE-R PCS and PMA	87.1		M	Yes [ ]
XLF2	Integration with management functions	87.1		O	Yes [ ] No [ ]
XLF3	Transmit function	87.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
XLF4	Optical multiplexing and delivery to the MDI	87.5.2	Optically multiplexes the four optical signals for delivery to the MDI	M	Yes [ ]
XLF5	Mapping between optical signal and logical signal for transmitter	87.5.2	Higher optical power is a one	M	Yes [ ]
XLF6	Receive function	87.5.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
XLF7	Conversion of four optical signals to four electrical signals	87.5.3	For delivery to the PMD service interface	M	Yes [ ]
XLF8	Mapping between optical signal and logical signal for receiver	87.5.3	Higher optical power is a one	M	Yes [ ]
XLF9	Global Signal Detect function	87.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
XLF10	Global Signal Detect behavior	87.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all four lanes	M	Yes [ ]
XLF11	Lane-by-Lane Signal Detect function	87.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 87–4	MD:O	Yes [ ] No [ ] N/A [ ]
XLF12	PMD_reset function	87.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

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87.13.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
XLM1	Management register set	87.4		MD:M	Yes [ ] N/A [ ]
XLM2	Global transmit disable function	87.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
XLM3	PMD_lane_by_lane_transmit_disable function	87.5.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_*i* variable	MD:O.2	Yes [ ] No [ ] N/A [ ]
XLM4	PMD_lane_by_lane_transmit_disable	87.5.8	Disables each optical transmitter independently if XLM3 = No	O.2	Yes [ ] No [ ]
XLM5	PMD_fault function	87.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
XLM6	PMD_transmit_fault function	87.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
XLM7	PMD_receive_fault function	87.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

87.13.4.3 PMD to MDI optical specifications for 40GBASE-LR4

Item	Feature	Subclause	Value/Comment	Status	Support
XLLR1	Transmitter meets specifications in Table 87–7	87.7.1	Per definitions in 87.8	LR4:M	Yes [ ] N/A [ ]
XLLR2	Receiver meets specifications in Table 87–8	87.7.2	Per definitions in 87.8	LR4:M	Yes [ ] N/A [ ]

87.13.4.4 PMD to MDI optical specifications for 40GBASE-ER4

Item	Feature	Subclause	Value/Comment	Status	Support
XLER1	Transmitter meets specifications in Table 87–7	87.7.1	Per definitions in 87.8	ER4:M	Yes [ ] N/A [ ]
XLER2	Receiver meets specifications in Table 87–8	87.7.2	Per definitions in 87.8	ER4:M	Yes [ ] N/A [ ]

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87.13.4.5 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
XLOM1	Measurement cable	87.8	2 m to 5 m in length	M	Yes [ ]
XLOM2	Center wavelength and SMSR	87.8.3	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
XLOM3	Average optical power	87.8.4	Per IEC 61280-1-1	M	Yes [ ]
XLOM4	Transmitter and dispersion penalty	87.8.6	Each lane	M	Yes [ ]
XLOM5	OMA	87.8.5	Each lane	M	Yes [ ]
XLOM6	Extinction ratio	87.8.7	Per IEC 61280-2-2	M	Yes [ ]
XLOM7	$RIN_{20}OMA$	87.8.8	Each lane	M	Yes [ ]
XLOM8	Transmit eye	87.8.9	Each lane	M	Yes [ ]
XLOM9	Stressed receiver sensitivity	87.8.11	Each lane	M	Yes [ ]
XLOM10	Receiver 3 dB electrical upper cutoff frequency	87.8.12	Each lane	M	Yes [ ]

87.13.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
XLES1	General safety	87.9.1	Conforms to J.2	M	Yes [ ]
XLES2	Laser safety—IEC Hazard Level 1	87.9.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
XLES3	Electromagnetic interference	87.9.4.1	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

87.13.4.7 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
XLOC1	Fiber optic cabling	87.11	Meets the requirements specified in Table 87–14	INS:M	Yes [ ] N/A [ ]
XLOC2	Maximum discrete reflectance	87.11.2.2	Less than –26 dB	INS:M	Yes [ ] N/A [ ]
XLOC3	MDI requirements	87.11.3	Meets the interface performance specifications listed	INS:M	Yes [ ] N/A [ ]

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88. Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-LR4 and 100GBASE-ER4

88.1 Overview

This clause specifies the 100GBASE-LR4 PMD and the 100GBASE-ER4 PMD together with the single-mode fiber medium. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 88–1, to the medium through the MDI and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 88–1—Physical Layer clauses associated with the 100GBASE-LR4 and 100GBASE-ER4 PMDs

Associated clause	100GBASE-LR4	100GBASE-ER4
81—RS	Required	Required
81—CGMII[a]	Optional	Optional
82—PCS for 100GBASE-R	Required	Required
83—PMA for 100GBASE-R	Required	Required
83A—CAUI-10	Optional	Optional
83B—Chip to module CAUI-10	Optional	Optional
83D—CAUI-4	Optional	Optional
83E—Chip-to-module CAUI-4	Optional	Optional
78—Energy Efficient Ethernet	Optional	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation behaves functionally as though the RS and CGMII were present.

Figure 88–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 40 Gb/s and 100 Gb/s Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2.

100GBASE-LR4 and 100GBASE-ER4 PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

88.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-LR4 and 100GBASE-ER4 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

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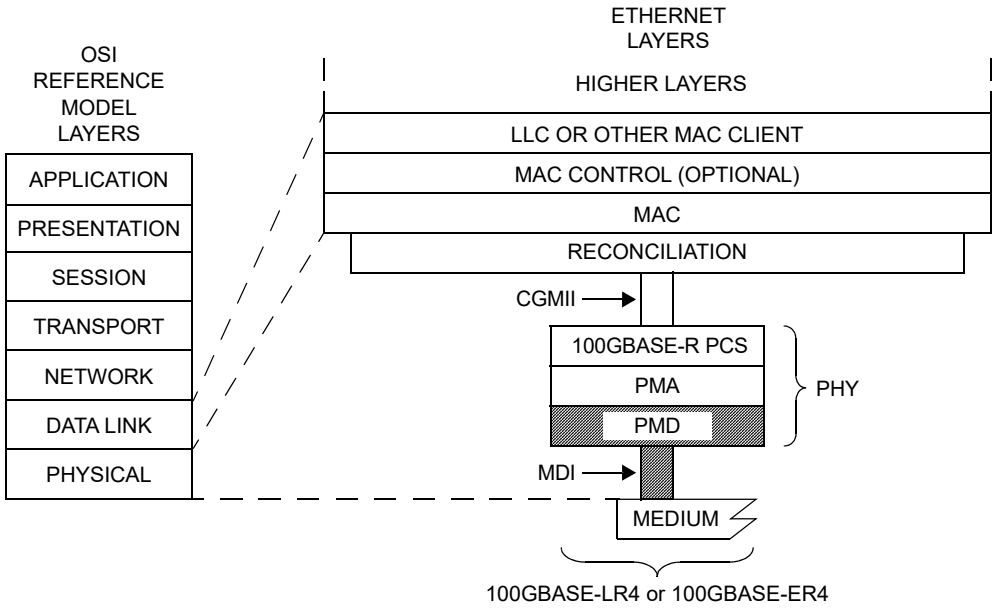

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

LR = PMD FOR SINGLE-MODE FIBER — 10 km
ER = PMD FOR SINGLE-MODE FIBER — 40 km

Figure 88–1—100GBASE-LR4 and 100GBASE-ER4 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

The PMD service interface is an instance of the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 100GBASE-LR4 and 100GBASE-ER4 PMDs have four parallel bit streams, hence $i = 0$ to 3.

In the transmit direction, the PMA continuously sends four parallel bit streams to the PMD, one per lane, each at a nominal signaling rate of 25.78125 GBd. The PMD then converts these streams of bits into the appropriate signals on the MDI.

In the receive direction, the PMD continuously sends four parallel bit streams to the PMA corresponding to the signals received from the MDI, one per lane, each at a nominal signaling rate of 25.78125 GBd.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication(SIGNAL_OK) inter-sublayer service interface primitive defined in 80.3.

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_bit parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_bit parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the 10^{-12} BER objective.

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88.3 Delay and Skew

88.3.1 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the 100GBASE-LR4 or 100GBASE-ER4 PMD including 2 m of fiber in one direction shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

88.3.2 Skew constraints

The Skew (relative delay) between the lanes is kept within limits so that the information on the lanes can be reassembled by the PCS. The Skew Variation is also limited to ensure that a given PCS lane always traverses the same physical lane. Skew and Skew Variation are defined in 80.5 and specified at the points SP1 to SP6 shown in Figure 80–7 and Figure 80–8.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5. The measurements of Skew and Skew Variation are defined in 87.8.2 with the exception that the clock and data recovery units' high-frequency corner bandwidths are 10 MHz.

88.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 88–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 88–3.

88.5 PMD functional specifications

The 100GBASE-LR4 and 100GBASE-ER4 PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

88.5.1 PMD block diagram

The PMD block diagram is shown in Figure 88–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 88.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 88.11.3). Unless specified otherwise, all receiver measurements and tests defined in 88.8 are made at TP3.

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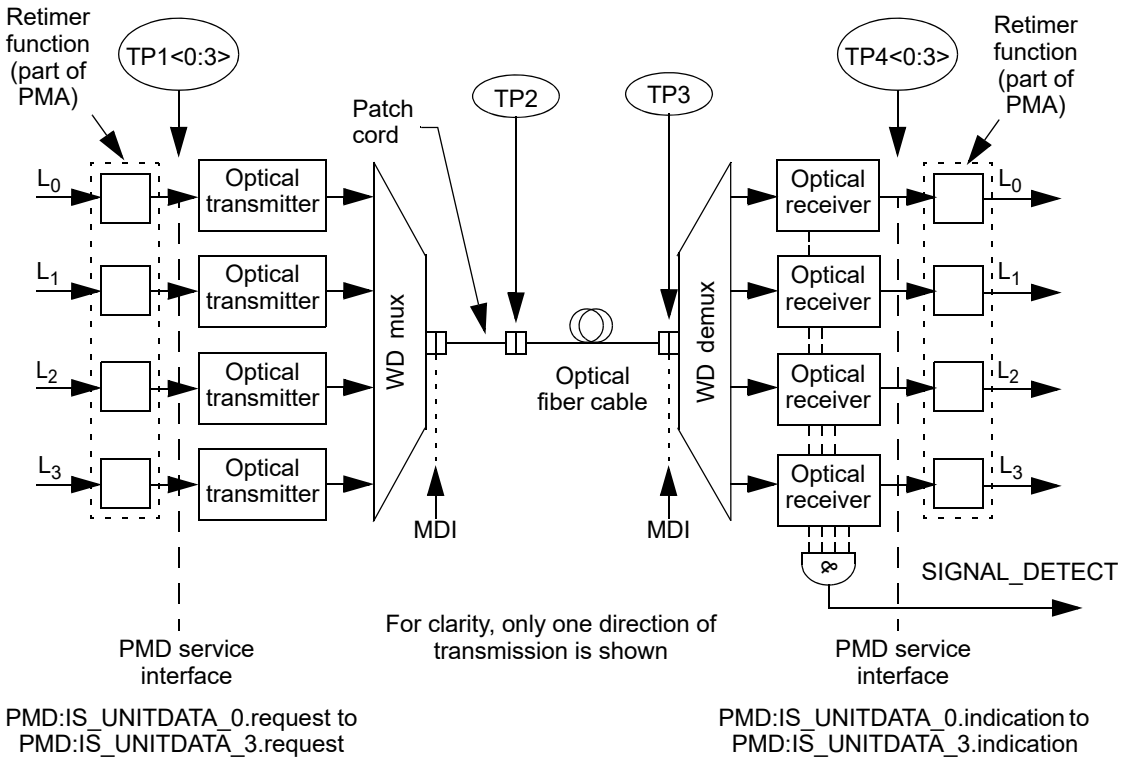

NOTE—Specification of the retimer function and the electrical implementation of the PMD service interface is beyond the scope of this standard.

Figure 88–2—Block diagram for 100GBASE-LR4 and 100GBASE-ER4 transmit/receive paths

Table 88–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable 3	PMD transmit disable register	1.9.4	PMD_transmit_disable_3
PMD transmit disable 2	PMD transmit disable register	1.9.3	PMD_transmit_disable_2
PMD transmit disable 1	PMD transmit disable register	1.9.2	PMD_transmit_disable_1
PMD transmit disable 0	PMD transmit disable register	1.9.1	PMD_transmit_disable_0

TP1<0:3> and TP4<0:3> are optional reference points that may be useful to implementers for testing components (these test points will not typically be accessible in an implemented system).

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Table 88–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect 3	PMD receive signal detect register	1.10.4	PMD_signal_detect_3
PMD receive signal detect 2	PMD receive signal detect register	1.10.3	PMD_signal_detect_2
PMD receive signal detect 1	PMD receive signal detect register	1.10.2	PMD_signal_detect_1
PMD receive signal detect 0	PMD receive signal detect register	1.10.1	PMD_signal_detect_0

88.5.2 PMD transmit function

The PMD Transmit function shall convert the four bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request into four separate optical signals. The four optical signals shall then be wavelength division multiplexed and delivered to the MDI, all according to the transmit optical specifications in this clause. The higher optical power level in each signal shall correspond to tx_bit = one.

88.5.3 PMD receive function

The PMD Receive function shall demultiplex the composite optical signal received from the MDI into four separate optical signals. The four optical signals shall then be converted into four bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to rx_bit = one.

88.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 80.3.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all four lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 88–4. The PMD receiver is not required to verify whether a compliant 100GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

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Table 88–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –30 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ receiver sensitivity (max) in OMA in Table 88–8) AND (compliant 100GBASE–R signal input)]	OK
All other conditions	Unspecified

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

88.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:3, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 88–4.

88.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

88.5.7 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 88–7.
b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter in each lane.

88.5.8 PMD lane-by-lane transmit disable function

The PMD lane-by-lane transmit disable function is optional and allows the optical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:3) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 88–7.
b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the optical transmitter in each lane.

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If the optional PMD lane-by-lane transmit disable function is not implemented in MDIO, an alternative method shall be provided to independently disable each transmit lane for testing purposes.

88.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

88.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

88.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

88.6 Wavelength-division-multiplexed lane assignments

The wavelength range for each lane of the 100GBASE-LR4 and 100GBASE-ER4 PMDs is defined in Table 88–5. The center frequencies are members of the frequency grid for 100 GHz spacing and above defined in ITU-T G.694.1 and are spaced at 800 GHz.

Table 88–5—Wavelength-division-multiplexed lane assignments

Lane	Center frequency	Center wavelength	Wavelength range
L_0	231.4 THz	1295.56 nm	1294.53 to 1296.59 nm
L_1	230.6 THz	1300.05 nm	1299.02 to 1301.09 nm
L_2	229.8 THz	1304.58 nm	1303.54 to 1305.63 nm
L_3	229 THz	1309.14 nm	1308.09 to 1310.19 nm

NOTE—There is no requirement to associate a particular electrical lane with a particular optical lane, as the PCS is capable of receiving lanes in any arrangement.

88.7 PMD to MDI optical specifications for 100GBASE-LR4 and 100GBASE-ER4

The operating ranges for the 100GBASE-LR4 and 100GBASE-ER4 PMDs are defined in Table 88–6. A 100GBASE-LR4 or 100GBASE-ER4 compliant PMD operates on type B1.1, B1.3, or B6_a single-mode fibers according to the specifications defined in Table 88–14. A PMD that exceeds the operating range

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requirement while meeting all other optical specifications is considered compliant (e.g., a 100GBASE-LR4 PMD operating at 12.5 km meets the operating range requirement of 2 m to 10 km). The 100GBASE-ER4 PMD interoperates with the 100GBASE-LR4 PMD provided that the channel requirements for 100GBASE-LR4 are met.

Table 88–6—100GBASE-LR4 and 100GBASE-ER4 operating ranges

PMD type	Required operating range
100GBASE-LR4	2 m to 10 km
100GBASE-ER4	2 m to 30 km
	2 m to 40 km[a]

[a]Links longer than 30 km for the same link power budget are considered engineered links. Attenuation for such links needs to be less than the worst case specified for B1.1, B1.3, or B6_a single-mode fiber.

88.7.1 100GBASE-LR4 and 100GBASE-ER4 transmitter optical specifications

The 100GBASE-LR4 transmitter shall meet the specifications defined in Table 88–7 per the definitions in 88.8. The 100GBASE-ER4 transmitter shall meet the specifications defined in Table 88–7 per the definitions in 88.8.

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Table 88–7—100GBASE-LR4 and 100GBASE-ER4 transmit characteristics

Description	100GBASE-LR4	100GBASE-ER4	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm		GBd
Lane wavelengths (range)	1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19		nm
Side-mode suppression ratio (SMSR), (min)	30		dB
Total average launch power (max)	10.5	8.9	dBm
Average launch power, each lane (max)	4.5	2.9	dBm
Average launch power, each lane[a] (min)	–4.3	–2.9	dBm
Optical Modulation Amplitude (OMA), each lane (max)	4.5		dBm
Optical Modulation Amplitude (OMA), each lane (min)	–1.3[b]	0.1	dBm
Difference in launch power between any two lanes (OMA) (max)	5	—	dB
Difference in launch power between any two lanes (Average and OMA) (max)	—	3.6	
Launch power in OMA minus TDP, each lane (min)	–2.3	—	dBm
Transmitter and dispersion penalty (TDP), each lane (max)	2.2	2.5	dB
Average launch power of OFF transmitter, each lane (max)	–30		dBm
Extinction ratio (min)	4	8	dB
$RIN_{20}OMA$ (max)	–130		dB/Hz
Optical return loss tolerance (max)	20		dB
Transmitter reflectance[c] (max)	–12		dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}		

[a]Average launch power, each lane (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]Even if the TDP < 1 dB, the OMA (min) has to exceed this value.
[c]Transmitter reflectance is defined looking into the transmitter.

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88.7.2 100GBASE-LR4 and 100GBASE-ER4 receive optical specifications

The 100GBASE-LR4 receiver shall meet the specifications defined in Table 88–8 per the definitions in 88.8.
The 100GBASE-ER4 receiver shall meet the specifications defined in Table 88–8 per the definitions in 88.8.

Table 88–8—100GBASE-LR4 and 100GBASE-ER4 receive characteristics

Description	100GBASE-LR4	100GBASE-ER4	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm		GBd
Lane wavelengths (range)	1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19		nm
Damage threshold[a]	5.5		dBm
Average receive power, each lane (max)	4.5[b]		dBm
Average receive power, each lane[c] (min)	–10.6	–20.9	dBm
Receive power, each lane (OMA) (max)	4.5		dBm
Difference in receive power between any two lanes (OMA) (max)	5.5	—	dB
Difference in receive power between any two lanes (Average and OMA) (max)	—	4.5	
Receiver reflectance (max)	–26		dB
Receiver sensitivity (OMA), each lane[d] (max)	–8.6	–21.4	dBm
Receiver 3 dB electrical upper cutoff frequency, each lane (max)	31		GHz
Stressed receiver sensitivity (OMA), each lane[e] (max)	–6.8	–17.9	dBm
Conditions of stressed receiver sensitivity test			
Vertical eye closure penalty,[f] each lane	1.8	3.5	dB
Stressed eye J2 Jitter,[f] each lane	0.3		UI
Stressed eye J9 Jitter,[f] each lane	0.47		UI

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
[b]The average receive power, each lane (max) for 100GBASE-ER4 is larger than the 100GBASE-ER4 transmitter value to allow compatibility with 100GBASE-LR4 units at short distances.
[c]Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[d]Receiver sensitivity (OMA), each lane (max) is optional.
[e]Measured with conformance test signal at TP3 (see 88.8.10) for BER = 10^{-12}.
[f]Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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88.7.3 100GBASE-LR4 and 100GBASE-ER4 illustrative link power budgets

Illustrative power budgets and penalties for 100GBASE-LR4 and 100GBASE-ER4 channels are shown in Table 88–9.

Table 88–9—100GBASE-LR4 and 100GBASE-ER4 illustrative link power budgets

Parameter	100GBASE-LR4	100GBASE-ER4		Unit
Power budget (for maximum TDP)	8.5	—		dB
Power budget	—	21.5		dB
Operating distance	10	30	40[a]	km
Channel insertion loss	6.3[b]	15	18	dB
Maximum discrete reflectance	–26	–26		dB
Allocation for penalties[c] (for maximum TDP)	2.2	—		dB
Allocation for penalties[c]	—	3.5		
Additional insertion loss allowed	0	3	0	dB

[a]Links longer than 30 km are considered engineered links. Attenuation for such links needs to be less than the worst case for B1.1, B1.3, or B6_a single-mode cabled optical fiber
[b]The channel insertion loss is calculated using the maximum distance specified in Table 88–6 for 100GBASE-LR4 and fiber attenuation of 0.43 dB/km at 1295 nm plus an allocation for connection and splice loss given in 88.11.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

88.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

88.8.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 88–11 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 88–11 may be used to perform that test. The test patterns used in this clause are shown in Table 88–10.

88.8.2 Wavelength and side mode suppression ratio (SMSR)

The wavelength and SMSR of each optical lane shall be within the ranges given in Table 88–5 if measured per IEC 61280-1-3. The lane under test is modulated using the test pattern defined in Table 88–11.

88.8.3 Average optical power

The average optical power of each lane shall be within the limits given in Table 88–7 if measured using the methods given in IEC 61280-1-1, with the sum of the optical power from all of the lanes not under test below –30 dBm, per the test setup in Figure 53–6.

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Table 88–10—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 ones, 8 zeros)	83.5.10
3	PRBS31	83.5.10
4	PRBS9	83.5.10
5	Scrambled idle	82.2.11

Table 88–11—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	3, 5 or valid 100GBASE-R signal	88.8.2
Side mode suppression ratio	3, 5 or valid 100GBASE-R signal	88.8.2
Average optical power	3, 5 or valid 100GBASE-R signal	88.8.3
Optical modulation amplitude (OMA)	Square wave or 4	88.8.4
Transmitter and dispersion penalty (TDP)	3 or 5	88.8.5
Extinction ratio	3, 5 or valid 100GBASE-R signal	88.8.6
$RIN_{20}OMA$	Square wave or 4	88.8.7
Transmitter optical waveform	3, 5 or valid 100GBASE-R signal	88.8.8
Stressed receiver sensitivity	3 or 5	88.8.10
Calibration of OMA for receiver tests	Square wave or 4	87.8.11
Vertical eye closure penalty calibration	3 or 5	87.8.11
Receiver 3 dB electrical upper cutoff frequency	3, 5 or valid 100GBASE-R signal	88.8.11

88.8.4 Optical Modulation Amplitude (OMA)

OMA shall be as defined in 52.9.5 for measurement with a square wave (8 ones, 8 zeros) test pattern or 68.6.2 (from the variable MeasuredOMA in 68.6.6.2) for measurement with a PRBS9 test pattern, with the exception that each lane may be tested individually with the sum of the optical power from all of the lanes not under test being below –30 dBm, or if other lanes are operating, a suitable optical filter may be used to separate the lane under test.

88.8.5 Transmitter and dispersion penalty (TDP)

Transmitter and dispersion penalty (TDP) shall be as defined in 52.9.10 with the exception that each optical lane is tested individually using an optical filter to separate the lane under test from the others. The measurement procedure for 100GBASE-LR4 and 100GBASE-ER4 is detailed in 88.8.5.1 to 88.8.5.4.

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The optical filter passband ripple shall be limited to 0.5 dB peak-to-peak and the isolation is chosen such that the ratio of the power in the lane being measured to the sum of the powers of all of the other lanes is greater than 20 dB (see ITU-T G.959.1 Annex B). The lanes not under test shall be operating with PRBS31 or valid 100GBASE-R bit streams.

88.8.5.1 Reference transmitter requirements

The reference transmitter is a high-quality instrument-grade device, which can be implemented by a CW laser modulated by a high-performance modulator. The basic requirements are as follows:

a) Rise/fall times of less than 12 ps at 20% to 80%.
b) The output optical eye is symmetric and passes the transmitter optical waveform test of 88.8.8.
c) In the center 20% region of the eye, the worst-case vertical eye closure penalty as defined in 87.8.11.2 is less than 0.5 dB.
d) Total Jitter less than 0.2 UI peak-to-peak.
e) RIN of less than –138 dB/Hz.

88.8.5.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 88–12.

Table 88–12—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]	Max mean DGD
	Minimum	Maximum			
100GBASE-LR4	$0.2325 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.2325 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	20 dB	0.8 ps
100GBASE-ER4	$0.93 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.93 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	20 dB	0.8 ps

[a]The dispersion is measured for the wavelength of the device under test (λ in nm). The coefficient assumes 10 km for 100GBASE-LR4 and 40 km for 100GBASE-ER4.
[b]There is no intent to stress the sensitivity of the BERT's optical receiver.
[c]The optical return loss is applied at TP2.

A 100GBASE-LR4 or 100GBASE-ER4 transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 88–12 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss specified in Table 88–12. The state of polarization of the back reflection is adjusted to create the greatest RIN.

The mean DGD of the channel is to be less than the value specified in Table 88–12.

88.8.5.3 Reference receiver requirements

The reference receiver is required to have the bandwidth given in 88.8.8. The sensitivity of the reference receiver is limited by Gaussian noise. The receiver has minimal threshold offset, deadband, hysteresis,

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baseline wander, deterministic jitter, or other distortions. Decision sampling has minimal uncertainty and setup/hold times.

The nominal sensitivity of the reference receiver, S, is measured in OMA using the setup of Figure 52–12 without the test fiber and with the transversal filter removed. The sensitivity S has to be corrected for any significant reference transmitter impairments including any vertical eye closure. It is measured while sampling at the eye center or corrected for off-center sampling. It is calibrated at the wavelength of the transmitter under test.

For all transmitter and dispersion penalty measurements, determination of the center of the eye is required. Center of the eye is defined as the time halfway between the left and right sampling points within the eye where the measured BER is greater than or equal to 1×10^{-3}.

The clock recovery unit (CRU) used in the TDP measurement has a corner frequency of 10 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low-frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.

88.8.5.4 Test procedure

The test procedure is as defined in 52.9.10.4 with the exception that all lanes are operational in both directions (transmit and receive), each lane is tested individually using an optical filter to separate the lane under test from the others and the BER of 1×10^{-12} is for the lane under test on its own.

88.8.6 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 88–7 if measured using the methods specified in IEC 61280-2-2, with the sum of the optical power from all of the lanes not under test below –30 dBm. The extinction ratio is measured using the test pattern defined in Table 88–11.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 88–11).

88.8.7 Relative Intensity Noise ($RIN_{20}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 20 dB.
b) Each lane may be tested individually with the sum of the optical power from all of the lanes not under test being below –30 dBm, or if other lanes are operating, a suitable optical filter may be used to separate the lane under test.
c) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 25.8 GHz).

88.8.8 Transmitter optical waveform (transmit eye)

The required optical transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 86–4. The transmitter optical waveform of a port transmitting the test pattern specified in Table 88–11 shall meet specifications according to the methods specified in 86.8.4.6.1 with the exception that the clock recovery unit's high-frequency corner bandwidth is 10 MHz. The filter nominal reference frequency f_r is 19.34 GHz and the filter tolerances are as specified for STM-64 in ITU-T G.691. Compensation may be made for variation of the reference receiver filter response from an ideal fourth-order Bessel-Thomson response.

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88.8.9 Receiver sensitivity

Receiver sensitivity, which is defined for an ideal input signal, is optional and compliance is not required. If measured, the test signal should have negligible impairments such as intersymbol interference (ISI), rise/fall times, jitter and RIN. Instead, the normative requirement for receivers is stressed receiver sensitivity.

88.8.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 88–8 if measured using the method defined in 87.8.11 with the following exceptions:

a) Added sinusoidal jitter is as specified in Table 88–13.
b) The stressed eye J2 Jitter, stressed eye J9 Jitter, and vertical eye closure penalty are as given in Table 88–8.
c) The test pattern is as given in Table 88–11.
d) The reference receiver used to verify the conformance test signal is required to have the bandwidth given in 88.8.8.

Table 88–13—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter, peak-to-peak (UI)
$f < 100$ kHz	Not specified
100 kHz $< f \leq$ 10 MHz	5×10^5 Hz / f
10 MHz $< f <$ 10 LB[a]	0.05

[a]LB = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

88.8.11 Receiver 3 dB electrical upper cutoff frequency

The receiver 3 dB electrical upper cutoff frequency shall be within the limits given in Table 88–8 if measured as described in 52.9.11. Each optical lane is measured using an optical signal or signals with its/their wavelength within the specified wavelength range of the lane to be tested. The test may use an electrical combiner and one optical source as in 53.9.13.

88.9 Safety, installation, environment, and labeling

88.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

88.9.2 Laser safety

100GBASE-LR4 and 100GBASE-ER4 optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

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Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[155]

88.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

88.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 100GBASE-LR4 or 100GBASE-ER4 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

88.9.5 Electromagnetic emission

A system integrating a 100GBASE-LR4 or 100GBASE-ER4 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

88.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

88.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 100GBASE-LR4).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 88.9.2.

[155]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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88.10 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 88–3.

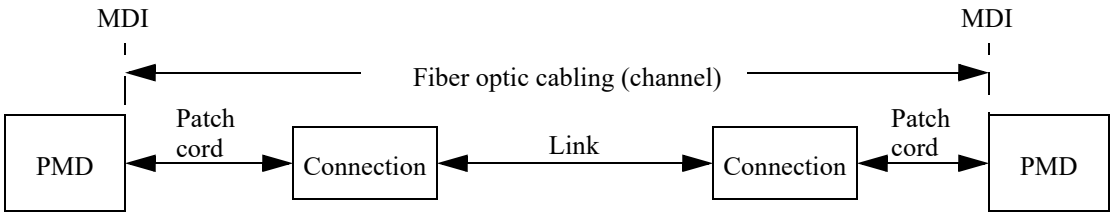

Figure 88–3—Fiber optic cabling model

The channel insertion loss is given in Table 88–14. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 88–14—Fiber optic cabling (channel) characteristics

Description	100GBASE-LR4	100GBASE-ER4		Unit
Operating distance (max)	10	30	40	km
Channel insertion loss[a, b] (max)	6.3	18	18	dB
Channel insertion loss (min)	0	0		dB
Positive dispersion[b] (max)	9.5	28	36	ps/nm
Negative dispersion[b] (min)	–28.5	–85	–114	ps/nm
DGD_max[c]	8	10.3	10.3	ps
Optical return loss (min)	21	21	21	dB

[a]These channel insertion loss values include cable, connectors, and splices.
[b]Over the wavelength range 1294.53 nm to 1310.19 nm.
[c]Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

88.11 Characteristics of the fiber optic cabling (channel)

The 100GBASE-LR4 and 100GBASE-ER4 fiber optic cabling shall meet the specifications defined in Table 88–14. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

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88.11.1 Optical fiber cable

The fiber optic cable requirements are satisfied by cables containing IEC 60793-2-50 type B1.1 (dispersion un-shifted single-mode), type B1.3 (low water peak single-mode), or type B6_a (bend insensitive) fibers or the requirements in Table 88–15 where they differ.

Table 88–15—Optical fiber and cable characteristics

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.43[a] or 0.5[b]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \leq \lambda_0 \leq 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a]The 0.43 dB/km at 1295 nm attenuation for optical fiber cables is derived from Appendix I of ITU-T G.695.
[b]The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3. Using 0.5 dB/km may not support operation at 10 km for 100GBASE-LR4 or 40 km for 100GBASE-ER4.

88.11.2 Optical fiber connection

An optical fiber connection, as shown in Figure 88–3, consists of a mated pair of optical connectors.

88.11.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 2 dB total connection and splice loss. For example, this allocation supports four connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 88–14 are met.

88.11.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –26 dB.

88.11.3 Medium Dependent Interface (MDI) requirements

The 100GBASE-LR4 or 100GBASE-ER4 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the “fiber optic cabling” (as shown in Figure 88–3). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 88.5.1, not at the MDI.

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88.12 Protocol implementation conformance statement (PICS) proforma for Clause 88, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-LR4 and 100GBASE-ER4[156]

88.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 88, Physical Medium Dependent sublayer and medium, type 100GBASE-LR4 and 100GBASE-ER4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

88.12.2 Identification

88.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

88.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 88, Physical Medium Dependent sublayer and medium, type 100GBASE-LR4 and 100GBASE-ER4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[156]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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88.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*LR4	100GBASE-LR4 PMD	88.7	Device supports requirements for 100GBASE-LR4 PHY	O.1	Yes [ ] No [ ]
*ER4	100GBASE-ER4 PMD	88.7	Device supports requirements for 100GBASE-ER4 PHY	O.1	Yes [ ] No [ ]
*INS	Installation / cable	88.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
CTP1	Reference point TP1 exposed and available for testing	88.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
CTP4	Reference point TP4 exposed and available for testing	88.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
CDC	Delay constraints	88.3.1	Device conforms to delay constraints	M	Yes [ ]
CSC	Skew constraints	88.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	88.4	Registers and interface supported	O	Yes [ ] No [ ]

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88.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, types 100GBASE-LR4 and 100GBASE-ER4

88.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CF1	Compatible with 100GBASE-R PCS and PMA	88.1		M	Yes [ ]
CF2	Integration with management functions	88.1		O	Yes [ ] No [ ]
CF3	Transmit function	88.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
CF4	Optical multiplexing and delivery to the MDI	88.5.2	Optically multiplexes the four optical signals for delivery to the MDI	M	Yes [ ]
CF5	Mapping between optical signal and logical signal for transmitter	88.5.2	Higher optical power is a one	M	Yes [ ]
CF6	Receive function	88.5.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
CF7	Conversion of four optical signals to four electrical signals	88.5.3	For delivery to the PMD service interface	M	Yes [ ]
CF8	Mapping between optical signal and logical signal for receiver	88.5.3	Higher optical power is a one	M	Yes [ ]
CF9	Global Signal Detect function	88.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
CF10	Global Signal Detect behavior	88.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all four lanes	M	Yes [ ]
CF11	Lane-by-lane Signal Detect function	88.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 88–4	MD:O	Yes [ ] No [ ] N/A [ ]
CF12	PMD reset function	88.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

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88.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
CM1	Management register set	88.4		MD:M	Yes [ ] N/A [ ]
CM2	Global transmit disable function	88.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
CM3	PMD_lane_by_lane_transmit_disable function	88.5.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_*i* variable	MD:O.2	Yes [ ] No [ ] N/A [ ]
CM4	PMD lane-by-lane transmit disable	88.5.8	Disables each optical transmitter independently if CM3 = No	O.2	Yes [ ] No [ ]
CM5	PMD_fault function	88.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
CM6	PMD_transmit_fault function	88.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
CM7	PMD_receive_fault function	88.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

88.12.4.3 PMD to MDI optical specifications for 100GBASE-LR4

Item	Feature	Subclause	Value/Comment	Status	Support
CLR1	Transmitter meets specifications in Table 88–7	88.7.1	Per definitions in 88.8	LR4:M	Yes [ ] N/A [ ]
CLR2	Receiver meets specifications in Table 88–8	88.7.2	Per definitions in 88.8	LR4:M	Yes [ ] N/A [ ]

88.12.4.4 PMD to MDI optical specifications for 100GBASE-ER4

Item	Feature	Subclause	Value/Comment	Status	Support
CER1	Transmitter meets specifications in Table 88–7	88.7.1	Per definitions in 88.8	ER4:M	Yes [ ] N/A [ ]
CER2	Receiver meets specifications in Table 88–8	88.7.2	Per definitions in 88.8	ER4:M	Yes [ ] N/A [ ]

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88.12.4.5 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Measurement cable	88.8	2 m to 5 m in length	M	Yes [ ]
COM2	Center wavelength and SMSR	88.8.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
COM3	Average optical power	88.8.3	Per IEC 61280-1-1	M	Yes [ ]
COM4	OMA measurements	88.8.4	Each lane	M	Yes [ ]
COM5	Transmitter and dispersion penalty	88.8.5	Each lane	M	Yes [ ]
COM6	Extinction ratio	88.8.6	Per IEC 61280-2-2	M	Yes [ ]
COM7	RIN_{20}OMA measurement procedure	88.8.7	Each lane	M	Yes [ ]
COM8	Transmit eye	88.8.8	Each lane	M	Yes [ ]
COM9	Stressed receiver sensitivity	88.8.10	Each lane	M	Yes [ ]
COM10	Receiver 3 dB electrical upper cutoff frequency	88.8.11	Each lane	M	Yes [ ]

88.12.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CES1	General safety	88.9.1	Conforms to J.2	M	Yes [ ]
CES2	Laser safety—IEC Hazard Level 1	88.9.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
CES3	Electromagnetic interference	88.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

88.12.4.7 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
COC1	Fiber optic cabling	88.11	Meets requirements specified in Table 88–14	INS:M	Yes [ ] N/A [ ]
COC2	Maximum discrete reflectance	88.11.2.2	Less than –26 dB	INS:M	Yes [ ] N/A [ ]
COC3	MDI requirements	88.11.3	Meets IEC 61753-1-1 and IEC 61753-021-2	INS:M	Yes [ ] N/A [ ]

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89. Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-FR

89.1 Overview

This clause specifies the 40GBASE-FR PMD together with the single-mode fiber medium. It is intended that devices compliant with this specification could be implemented to also be used for application VSR2000-3R2 as defined in ITU-T G.693 [B45] (but that is beyond the scope of this standard). The 40GBASE-FR PMD is defined using a specification and test methodology that is similar to that used in ITU-T G.693 [B45], which is different from the specification and test methodologies used for other optical PMDs at 1000 Mb/s and above in IEEE Std 802.3. For example, the transmitter specifications for 40GBASE-FR do not include OMA or TDP parameters but do include a dispersion penalty limit, and the receiver specifications for 40GBASE-FR do not include stressed receiver sensitivity parameters but do include a part-stressed sensitivity limit and a separate jitter tolerance limit. See 89.6.4.

When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 89–1, to the medium through the MDI and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 89–1—Physical Layer clauses associated with the 40GBASE-FR PMD

Associated clause	40GBASE-FR
81—RS	Required
81—XLGMII[a]	Optional
82—PCS for 40GBASE-R	Required
83—PMA for 40GBASE-R	Required
83A—XLAUI	Optional
83B—Chip to module XLAUI	Optional
78—Energy Efficient Ethernet	Optional

[a]The XLGMII is an optional interface. However, if the XLGMII is not implemented, a conforming implementation behaves functionally as though the RS and XLGMII were present.

Figure 89–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 40 Gb/s and 100 Gb/s Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2.

40GBASE-FR PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

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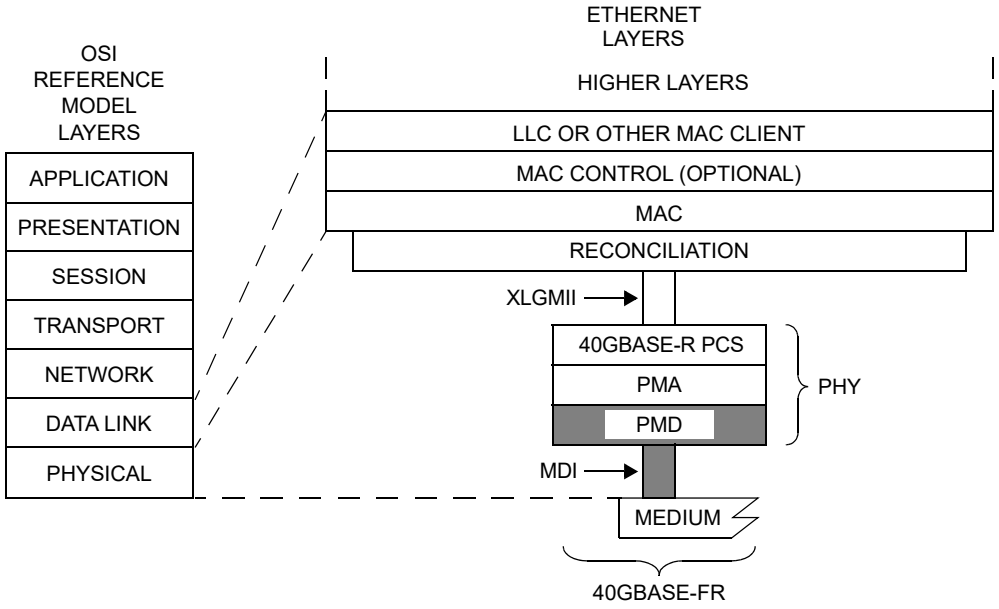

LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE
FR = PMD FOR SINGLE-MODE FIBER — 2 km

Figure 89–1—40GBASE-FR PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

89.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 40GBASE-FR PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_0.request
PMD:IS_UNITDATA_0.indication
PMD:IS_SIGNAL.indication

In the transmit direction, the PMA continuously sends a single serial stream of bits to the PMD at a nominal signaling rate of 41.25 GBd. The PMD converts this stream of bits into an appropriate signal on the MDI.

In the receive direction, the PMD continuously sends a single serial stream of bits to the PMA corresponding to the signal received from the MDI at a nominal signaling rate of 41.25 GBd.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication(SIGNAL_OK) inter-sublayer service primitive defined in 80.3.

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The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_bit parameter is undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_bit parameter is known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the 10^{-12} BER objective.

89.3 Delay and skew

89.3.1 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the 40GBASE-FR PMD including 2 m of fiber in one direction shall be no more than 1024 bit times (2 pause_quanta or 25.6 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

89.3.2 Skew constraints

The Skew (relative delay) between the PCS lanes is kept within limits so that the information on the lanes can be reassembled by the PCS. The Skew Variation is also limited to ensure that a given PCS lane always traverses the same physical lane. Skew and Skew Variation are defined in 80.5 and specified at the points SP1 to SP6 shown in Figure 80–7 and Figure 80–8.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 83.5.3.4. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 80.5. The measurements of Skew and Skew Variation are defined in 89.7.2.

89.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 89–2, and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 89–3.

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Table 89–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD Transmit disable register	1.9.0	PMD_global_transmit_disable

Table 89–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect

89.5 PMD functional specifications

The 40GBASE-FR PMD performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

89.5.1 PMD block diagram

The PMD block diagram is shown in Figure 89–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 89.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 89.10.3). Unless specified otherwise, all receiver measurements and tests defined in 89.7 are made at TP3.

89.5.2 PMD transmit function

The PMD Transmit function shall convert the bit stream requested by the PMD service interface message PMD:IS_UNITDATA_0.request into an optical signal and deliver it to the MDI, according to the transmit optical specifications in this clause. The higher optical power level in the signal shall correspond to tx_bit = one.

89.5.3 PMD receive function

The optical signal received from the MDI shall be converted into a bit stream for delivery to the PMD service interface using the message PMD:IS_UNITDATA_0.indication, according to the receive optical specifications in this clause. The higher optical power level in the signal shall correspond to rx_bit = one.

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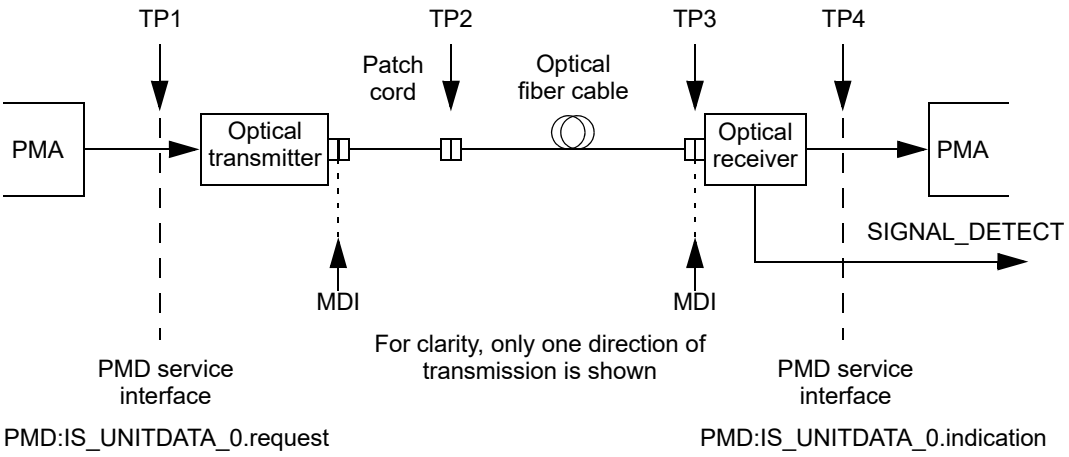

Figure 89–2—Block diagram for 40GBASE-FR transmit/receive paths

89.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 80.3.

SIGNAL_DETECT is an indicator of the presence of an optical signal. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 89–4. The PMD receiver is not required to verify whether a compliant 40GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 89–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
Average optical power at TP3 ≤ –30 dBm	FAIL
(Optical power at TP3 ≥ receiver sensitivity (average power) (max) in Table 89–7) AND (compliant 40GBASE–R signal input)	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

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89.5.5 PMD reset function

If the MDIO interface is implemented and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

89.5.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows the optical transmitter to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of the OFF transmitter in Table 89–6.
b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter.

If the MDIO interface is implemented, then this function shall map to the PMD_global_transmit_disable bit as specified in 45.2.1.8.7.

NOTE—The PMD lane-by-lane transmit disable function is not used for serial PMDs.

89.5.7 PMD fault function (optional)

If the PMD has detected a local fault on either the transmit or receive path, the PMD shall set PMD_fault to one. If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

89.5.8 PMD transmit fault function (optional)

If the PMD has detected a local fault on the transmitter, the PMD shall set the PMD_transmit_fault variable to one. If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

89.5.9 PMD receive fault function (optional)

If the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to one. If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

89.6 PMD to MDI optical specifications for 40GBASE-FR

The required operating range for the 40GBASE-FR PMD is defined in Table 89–5. A 40GBASE-FR compliant PMD operates on IEC 60793-2-50 type B1.1, B1.3 or B6_a single-mode fibers according to the specifications defined in Table 89–13. A PMD that exceeds the required operating range while meeting all other optical specifications is considered compliant (e.g., operating at 2.5 km meets the operating range requirement of 2 m to 2 km).

Table 89–5—40GBASE-FR required operating range

PMD type	Required operating range
40GBASE-FR	2 m to 2 km

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89.6.1 40GBASE-FR transmitter optical specifications

The 40GBASE-FR transmitter shall meet the specifications defined in Table 89–6 per the definitions in 89.7.

Table 89–6—40GBASE-FR transmit characteristics

Description	Value	Unit
Signaling rate (range)	41.25 ± 100 ppm	GBd
Center wavelength (range)	1530 to 1565	nm
Side-mode suppression ratio (SMSR), (min)	35	dB
Average launch power (max)	3	dBm
Average launch power (min)	0	dBm
Dispersion penalty (max)	2	dB
Average launch power of OFF transmitter (max)	–30	dBm
Extinction ratio (min)	8.2	dB
$RIN_{20}OMA$ (max)	–132	dB/Hz
Optical return loss tolerance (max)	20	dB
Transmitter reflectance[a] (max)	–12	dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.4, 0.45, 0.22, 0.25, 0.4}	

[a]Transmitter reflectance is defined looking into the transmitter.

89.6.2 40GBASE-FR receive optical specifications

The 40GBASE-FR receiver shall meet the specifications defined in Table 89–7 per the definitions in 89.7.

Table 89–7—40GBASE-FR receive characteristics

Description	Value	Unit
Signaling rate (range)	41.25 ± 100 ppm	GBd
Center wavelength (range)	1290 to 1330 and 1530 to 1565	nm
Damage threshold[a] (min)	4	dBm
Average receive power (max)	3	dBm
Receiver reflectance (max)	–26	dB
Receiver sensitivity (average power)[b] (max)	–6	dBm
Receiver jitter tolerance (max)	1	dB
Receiver 3 dB electrical upper cutoff frequency (max)	49	GHz

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.

[b]Receiver sensitivity (average power) is defined in 89.7.9 and is to be met with a transmitter with worst-case transmit eye, extinction ratio, transmitter reflectance, and $RIN_{20}OMA$. This is a different definition of receiver sensitivity from that used in other clauses (e.g., that in Clause 38). See 89.6.4 for a comparison.

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89.6.3 40GBASE-FR illustrative link power budget

An illustrative power budget and penalties for 40GBASE-FR channels are shown in Table 89–8.

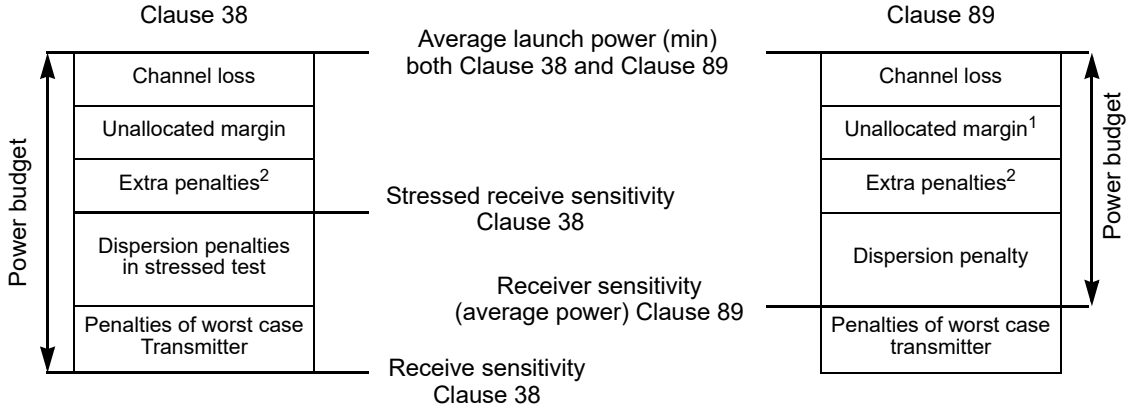
Table 89–8—40GBASE-FR illustrative power budget

Parameter	Value	Unit
Power budget[a]	6	dB
Operating distance	2	km
Channel insertion loss[b]	4	dB
Maximum discrete reflectance	–26	dB
Path penalty[a, c]	2	dB
Additional insertion loss allowed	0	dB

[a]This budget does not include the effect of a non-ideal transmitter waveform. See 89.6.4.
[b]The channel insertion loss is calculated using the maximum distance specified in Table 89–5 and cabled optical fiber attenuation of 0.5 dB/km at 1530 nm plus an allocation for connection and splice loss given in 89.10.2.1.
[c]Path penalty is the combined penalty caused by chromatic dispersion and polarization mode dispersion.

89.6.4 Comparison of power budget methodology

This clause uses the budgeting methodology that is used for application VSR2000-3R2 in ITU-T G.693 [B45], which is different from the methodology used in other clauses of this standard (e.g., Clause 38, Clause 52, Clause 86, Clause 87, Clause 88). Figure 89–3 compares the terminology used in this clause with Clause 38. Receiver sensitivity in this clause is specified with a worst-case transmitter input whereas in the other clauses it is specified with a perfect signal without penalties. Stressed receiver sensitivity is not specified in this clause but is specified as the key requirement in the other clauses with a signal that includes both transmitter and link penalties.



NOTE 1—For Clause 89 unallocated margin is zero and not mentioned in the rest of this clause.
NOTE 2—For Clause 38 extra penalties are any penalties that are not included in the stressed test while for Clause 89 extra penalties are any penalties that are not included in the dispersion penalty test.

Figure 89–3—Optical power budget methodology comparison with Clause 38

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89.7 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

89.7.1 Test patterns for optical parameters

Compliance is to be achieved in normal operation. Table 89–10 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 89–10 may be used to perform that test. The test patterns used in this clause are shown in Table 89–9.

Table 89–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 ones, 8 zeros)	83.5.10
3	PRBS31	83.5.10
4	PRBS9	83.5.10
5	Scrambled idle	82.2.11

Table 89–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	3, 5 or valid 40GBASE-R signal	89.7.3
Side mode suppression ratio	3, 5 or valid 40GBASE-R signal	89.7.3
Average optical power	3, 5 or valid 40GBASE-R signal	89.7.4
Dispersion penalty	3 or 5	89.7.5
Extinction ratio	3, 5 or valid 40GBASE-R signal	89.7.6
$RIN_{20}OMA$	Square wave or 4	89.7.7
Transmitter optical waveform	3, 5 or valid 40GBASE-R signal	89.7.8
Receiver sensitivity	3 or 5	89.7.9
Receiver jitter tolerance	3 or 5	89.7.10
Receiver 3 dB electrical upper cutoff frequency	3, 5 or valid 40GBASE-R signal	89.7.11

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89.7.2 Skew and Skew Variation

Skew and Skew Variation are defined in 80.5 and are required to remain within the limits given in 89.3.2 over the time that the link is in operation. Since the signal for this PMD is a serial bit stream at the PMD service interface and the MDI, there is no Skew Variation at skew points SP2, SP3, SP4, and SP5. The measurement of Skew is made by acquiring the data on the single lane using a clock and data recovery unit with high-frequency corner bandwidth of 16 MHz and a slope of –20 dB/decade. The arrival times of the one to zero transition of the alignment marker sync bits on each PCS lane are then compared. This arrangement ensures that any high-frequency jitter that is present on the signals is not included in the Skew measurement.

89.7.3 Wavelength and side mode suppression ratio (SMSR)

The center wavelength and SMSR shall be within the range given in Table 89–6 if measured per IEC 61280-1-3 using the test pattern referenced in Table 89–10.

89.7.4 Average optical power

The average optical power shall be within the limits given in Table 89–6 and Table 89–7 if measured using the methods given in IEC 61280-1-1 using the test pattern referenced in Table 89–10.

89.7.5 Dispersion penalty

The dispersion penalty of a transmitter is defined as the difference in sensitivity (at a BER of 10^{-12}) of a reference receiver as defined in 89.7.5.2 when receiving the signal from that transmitter via the channel defined in 89.7.5.1 compared to the sensitivity obtained when receiving the signal via an attenuator only.

89.7.5.1 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 89–11.

Table 89–11—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]	Max mean DGD
	Minimum	Maximum			
40GBASE-FR	$0.0465 \times \lambda \times [1 - (1324 / \lambda)^4]$	$0.0465 \times \lambda \times [1 - (1300 / \lambda)^4]$	Minimum	20 dB	0.5 ps

[a]The dispersion is measured for the wavelength of the device under test (λ in nm). The coefficient assumes a maximum operating distance of 2 km.
[b]There is no intent to stress the sensitivity of the BERT's optical receiver.
[c]The optical return loss is applied at TP2.

A 40GBASE-FR transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 89–11 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss specified in Table 89–11. The state of polarization of the back reflection is adjusted to create the greatest RIN.

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The mean DGD of the channel is to be less than the value specified in Table 89–11.

89.7.5.2 Reference receiver requirements

The reference receiver is required to have the bandwidth given in 89.7.8. The sensitivity of the reference receiver is limited by Gaussian noise. The receiver has minimal threshold offset, deadband, hysteresis, baseline wander, deterministic jitter, or other distortions. Decision sampling has minimal uncertainty and setup/hold times.

The clock recovery unit (CRU) used in the dispersion penalty measurement has a corner frequency of 16 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low-frequency jitter from the signal to the clock removes this low-frequency jitter from the measurement.

89.7.5.3 Test procedure

To measure the dispersion penalty, the following procedure shall be used:

a) Configure the test equipment as described above and illustrated in Figure 89–4.
b) With a short patch cable rather than the test fiber and with no reflection, adjust the attenuation of the optical attenuator to obtain a BER of 10^{-12}.
c) Record the optical power at the input to the reference receiver, P_ND, in dBm.
d) With the test fiber and reflection in place, adjust the attenuation of the optical attenuator to obtain a BER of 10^{-12}.
e) Record the optical power at the input to the reference receiver, P_D, in dBm.
f) If P_D is larger than P_ND, the dispersion penalty for the transmitter under test is P_D – P_ND. Otherwise, the dispersion penalty is zero.

It is to be ensured that the measurements are made in the linear power regime of the fiber.

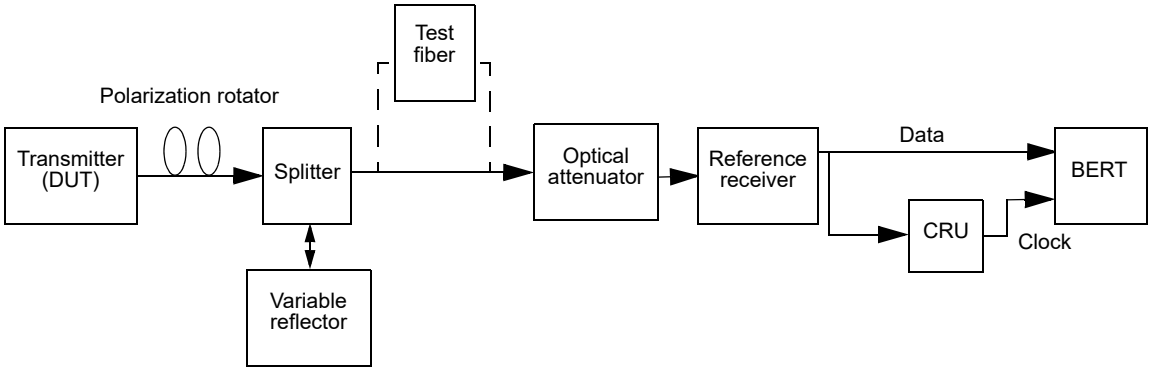

Figure 89–4—Test setup for measurement of dispersion penalty

89.7.6 Extinction ratio

The extinction ratio shall be within the limits given in Table 89–6 if measured using the methods specified in IEC 61280-2-2 using the test pattern referenced in Table 89–10.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 89–10).

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89.7.7 Relative Intensity Noise ($RIN_{20}OMA$)

The RIN measurement methodology shall be as defined in 52.9.6 with the following exceptions:

a) The optical return loss is 20 dB.
b) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 41.25 GHz).

89.7.8 Transmitter optical waveform (transmit eye)

The required optical transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 86–4. The transmitter optical waveform of a port transmitting the test pattern specified in Table 89–10 shall meet specifications according to the methods specified in 86.8.4.6.1 with the filter nominal reference frequency f_r of 30.94 GHz and filter tolerances as specified for STM–64 in ITU–T G.691. Compensation may be made for variation of the reference receiver filter response from an ideal fourth-order Bessel-Thomson response.

89.7.9 Receiver sensitivity

Receiver sensitivity is defined as the minimum value of mean received power at TP3 to achieve a BER of 10^{-12}. This shall be met with a transmitter with worst-case transmit eye, extinction ratio, transmitter reflectance, and $RIN_{20}OMA$. The receiver sensitivity does not have to be met in the presence of dispersion, as this effect is specified separately as the dispersion penalty.

Receiver sensitivity is defined with the transmit section in operation. Pattern 3, or Pattern 5, or a valid 40GBASE–R signal is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal.

89.7.10 Receiver jitter tolerance

Receiver jitter tolerance is defined as the largest increase in received optical power required to maintain a BER of 10^{-10} when the sinusoidal jitter defined in Table 89–12 is applied to the signal from a reference transmitter across the defined range of jitter frequencies.

The reference transmitter is a high-quality instrument-grade device, which can be implemented by a CW laser modulated by a high-performance modulator. The following basic requirements apply:

a) Rise/fall times are less than 10 ps at 20% to 80%.
b) The output optical eye is symmetric and passes the transmitter optical waveform test of 89.7.8.
c) In the center 20% region of the eye, the worst-case vertical eye closure penalty as defined in 52.9.9.2 is less than 0.5 dB.
d) Total Jitter is less than 0.2 UI peak-to-peak.

The receiver jitter tolerance shall be within the limits given in Table 89–7 if measured according to the above definition.

NOTE—Receiver jitter tolerance as defined here is made without additional amplitude stress.

89.7.11 Receiver 3 dB electrical upper cutoff frequency

The receiver 3dB electrical upper cutoff frequency shall be within the limits given in Table 89–7 if measured as described in 52.9.11 with the exception that the optical power level used in 52.9.11 b) is approximately equal to the receiver sensitivity level in Table 89–7.

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Table 89–12—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter, peak-to-peak (UI)
$f < 480$ kHz	Not specified
480 kHz $< f \leq$ 16 MHz	2.88×10^6 Hz / f
16 MHz $< f <$ 10 LB[a]	0.18

[a]LB = loop bandwidth; upper frequency bound for added sinusoidal jitter should be at least 10 times the loop bandwidth of the receiver being tested.

89.8 Safety, installation, environment, and labeling

89.8.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

89.8.2 Laser safety

40GBASE-FR optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single-fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[157]

89.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

89.8.4 Environment

Normative specifications in Clause 89 shall be met by a system integrating a 40GBASE-FR PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate, in the literature associated with the PHY, the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of Clause 89 will be met.

[157]A host system that fails to meet the manufacturers requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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89.8.4.1 Electromagnetic emission

A system integrating a 40GBASE-FR PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

89.8.4.2 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

89.8.5 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 40GBASE-FR).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 89.8.2.

89.9 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 89–5.

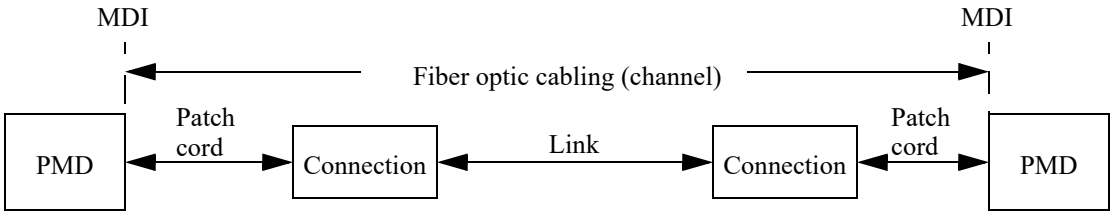

Figure 89–5—Fiber optic cabling model

The channel insertion loss is given in Table 89–13. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion, meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method, chromatic dispersion is measured in accordance with IEC 60793-1-42, and polarization mode dispersion is measured in accordance with IEC 60793-1-48. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term *channel* is used here for consistency with generic cabling standards.

89.10 Characteristics of the fiber optic cabling (channel)

The 40GBASE-FR fiber optic cabling shall meet the specifications defined in Table 89–13. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

89.10.1 Optical fiber cable

The fiber optic cable requirements are satisfied by cables containing IEC 60793-2-50 type B1.1 (dispersion un-shifted single-mode), type B1.3 (low water peak single-mode), or type B6_a (bend insensitive) fibers or the requirements in Table 89–14 where they differ.

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Table 89–13—Fiber optic cabling (channel) characteristics for 40GBASE-FR

Description	Value	Unit
Operating distance (max)	2	km
Channel insertion loss[a, b] (max)	4	dB
Channel insertion loss (min)	0	dB
Dispersion[b] (max)	38	ps/nm
DGD_max[c]	3	ps
Optical return loss (min)	21	dB

[a]These channel insertion loss values include cable, connectors, and splices.
[b]Over the wavelength range 1530 nm to 1565 nm.
[c]Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

Table 89–14—Optical fiber and cable characteristics for 40GBASE-FR

Description	Value	Unit
Nominal fiber specification wavelength	1550	nm
Cabled optical fiber attenuation (max)	0.5[a]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \leq \lambda_0 \leq 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a]The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA-568-C.3-2008.

89.10.2 Optical fiber connection

An optical fiber connection, as shown in Figure 89–5, consists of a mated pair of optical connectors.

89.10.2.1 Connection insertion loss

The maximum link distances for single-mode fiber are calculated based on an allocation of 3 dB total connection and splice loss. For example, this allocation supports six connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 89–13 are met.

89.10.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –26 dB.

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89.10.3 Medium Dependent Interface (MDI) requirements

The 40GBASE-FR PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 89–5). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 89.5.1, not at the MDI.

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89.11 Protocol implementation conformance statement (PICS) proforma for Clause 89, Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-FR[158]

89.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 89, Physical Medium Dependent sublayer and medium, type 40GBASE-FR, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

89.11.2 Identification

89.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

89.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 89, Physical Medium Dependent sublayer and medium, type 40GBASE-FR
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[158] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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89.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*INS	Installation / cable	89.9	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
XLDC	Delay constraints	89.3.1	Device conforms to delay constraints	M	Yes [ ]
XLSC	Skew constraints	89.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	89.4	Registers and interface supported	O	Yes [ ] No [ ]

89.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE-FR

89.11.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
XLF1	Compatible with 40GBASE-R PCS and PMA	89.1		M	Yes [ ]
XLF2	Integration with management functions	89.1		O	Yes [ ] No [ ]
XLF3	Transmit function	89.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
XLF4	Mapping between optical signal and logical signal for transmitter	89.5.2	Higher optical power is a one	M	Yes [ ]
XLF5	Receive function	89.5.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
XLF6	Mapping between optical signal and logical signal for receiver	89.5.3	Higher optical power is a one	M	Yes [ ]
XLF7	Global Signal Detect function	89.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
XLF8	Global Signal Detect behavior	89.5.4	SIGNAL_DETECT is an indicator of the presence of an optical signal	M	Yes [ ]
XLF9	PMD_reset function	89.5.5	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

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89.11.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
XLM1	Management register set	89.4		MD:M	Yes [ ] N/A [ ]
XLM2	Global transmit disable function	89.5.6	Disables the optical transmitter with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
XLM3	PMD_fault function	89.5.7	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
XLM4	PMD_transmit_fault function	89.5.8	Sets PMD_transmit_fault to one if a local transmitter fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
XLM5	PMD_receive_fault function	89.5.9	Sets PMD_receive_fault to one if a local receiver fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]

89.11.4.3 PMD to MDI optical specifications for 40GBASE-FR

Item	Feature	Subclause	Value/Comment	Status	Support
XLLR1	Transmitter meets specifications in Table 89–6	89.6.1	Per definitions in 89.7	M	Yes [ ]
XLLR2	Receiver meets specifications in Table 89–7	89.6.2	Per definitions in 89.7	M	Yes [ ]

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89.11.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
XLOM1	Measurement cable	89.7	2 m to 5 m in length	M	Yes [ ]
XLOM2	Center wavelength and SMSR	89.7.3	Per IEC 61280-1-3	M	Yes [ ]
XLOM3	Average optical power	89.7.4	Per IEC 61280-1-1	M	Yes [ ]
XLOM4	Dispersion penalty	89.7.5.3		M	Yes [ ]
XLOM5	Extinction ratio	89.7.6	Per IEC 61280-2-2	M	Yes [ ]
XLOM6	$RIN_{20}OMA$	89.7.7		M	Yes [ ]
XLOM7	Transmit eye	89.7.8		M	Yes [ ]
XLOM8	Receiver sensitivity	89.7.9		M	Yes [ ]
XLOM9	Receiver jitter tolerance	89.7.10		M	Yes [ ]
XLOM10	Receiver 3 dB electrical upper cutoff frequency	89.7.11		M	Yes [ ]

89.11.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
XLES1	General safety	89.8.1	Conforms to J.2	M	Yes [ ]
XLES2	Laser safety—IEC Hazard Level 1	89.8.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
XLES3	Electromagnetic interference	89.8.4.1	Complies with applicable codes for the limitation of electromagnetic interference	M	Yes [ ]

89.11.4.6 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
XLOC1	Fiber optic cabling	89.10	Meets the requirements specified in Table 89–13	INS:M	Yes [ ] N/A [ ]
XLOC2	Maximum discrete reflectance	89.10.2.2	Less than –26 dB	INS:M	Yes [ ] N/A [ ]
XLOC3	MDI requirements	89.10.3	Meets the interface performance specifications listed	INS:M	Yes [ ] N/A [ ]

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90. Ethernet support for time synchronization protocols

90.1 Introduction

This clause specifies the optional Time Synchronization Service Interface (TSSI). The TSSI can be used to support protocols that require knowledge of packet egress and ingress time.

The TSSI is defined for the full-duplex mode of operation only. It supports MAC operation at various data rates. The MII (Clause 22), GMII (Clause 35), XGMII (Clause 46), 25GMII (Clause 106), XLGMII (Clause 81), CGMII (Clause 81), 50GMII (Clause 132), 200GMII (Clause 117), and 400GMII (Clause 117) specifications are all compatible with the generic Reconciliation Sublayer (gRS) defined in 90.5.

90.2 Overview

The goal of this clause is to provide an accurate indication of the transmission and reception initiation times of all packets, as required to support various time synchronization protocols, e.g., IEEE Std 1588-2008 [B41], and IEEE Std 802.1AS [B39].

The specific goals are to:

a) Define the Time Synchronization Service Interface (TSSI), with associated service primitives;

b) Add management registers to indicate the maximum and minimum data delays for estimation of link latency at the Time Synchronization Protocol (TimeSync) Client.

90.3 Relationship with other IEEE standards

Per 90.2, the TimeSync capability provides support for various time synchronization protocols, including e.g., IEEE Std 1588-2008 or IEEE Std 802.1AS. The definition of TimeSync Client, its capabilities and functions is outside the scope of IEEE Std 802.3.

90.4 Time Synchronization Service Interface (TSSI)

90.4.1 Introduction

This subclause specifies services provided by an extension to the Reconciliation Sublayers specified elsewhere in this standard.

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90.4.1.1 Interlayer service interfaces

Figure 90–1 depicts the TimeSync Client and the RS interlayer service interfaces.

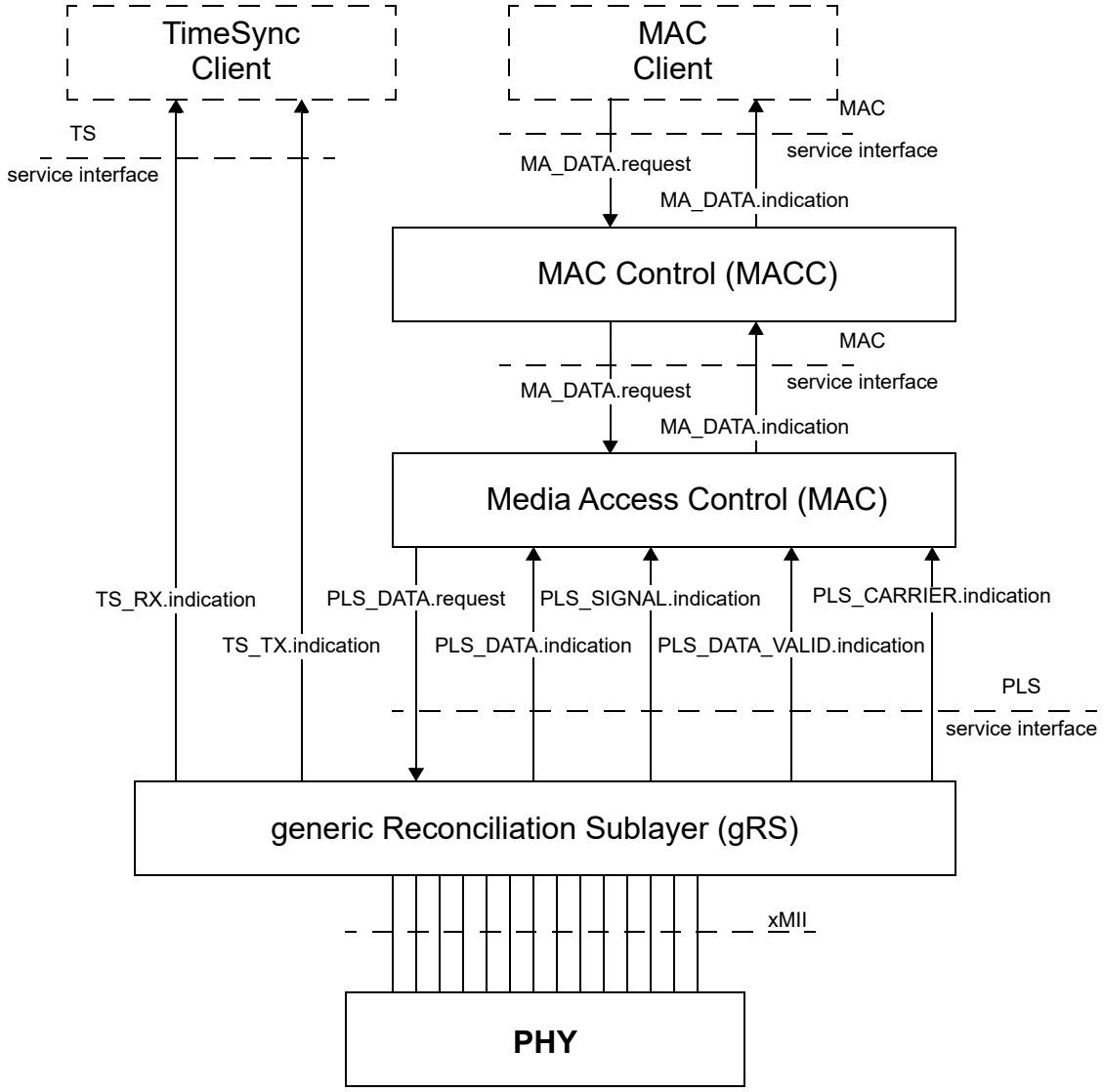

Figure 90–1—Relationship of the TimeSync Client, TSSI and gRS sublayer relative to MAC and MAC Client and associated interfaces

NOTE 1—In this figure, the xMII is used as a generic term for the Media Independent Interfaces for implementations of 10BASE-T1L, 10BASE-T1S, and 100 Mb/s and above. For example: for 100 Mb/s implementations this interface is called MII; for 1 Gb/s implementations, it is called GMII; for 10 Gb/s implementations, it is called XGMII; etc.

NOTE 2—Optional Low Power Idle (LPI) Client service interface not shown.

90.4.1.2 Responsibilities of TimeSync Client

The TimeSync Client can use the indication of the event corresponding to the egress and ingress of packets provided by the TSSI, combined with knowledge of the protocol frames, to select the egress and ingress times relevant to the protocol. Which frames are of interest to any particular protocol is beyond the scope of this standard.

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The TimeSync Client can use the indication of the event corresponding to the egress and ingress of packets at the xMII provided by the TSSI, together with the information provided by the TimeSync PHY transmit data delay and TimeSync PHY receive data delay (see 30.13.1).

90.4.2 TSSI

The following specifies the service interface provided by the RS to the TimeSync Client. These services are described in an abstract manner and do not imply any particular implementation. The model used in this service specification is identical to that used in 1.2.2.

The following primitives are defined:

— TS_TX.indication
— TS_RX.indication

90.4.3 Detailed service specification

90.4.3.1 TS_TX.indication primitive

This primitive defines the transfer of the indication of an event between gRS and the TimeSync Client.

90.4.3.1.1 Semantics

The semantics of the primitive are as follows:

TS_TX.indication(SFD, MM)

The SFD parameter can take only one possible value, DETECTED. When asserted (SFD = DETECTED), the TimeSync Client is notified that a valid SFD was detected by the gRS sublayer TS_SFD_Detect_TX function (see 90.5.1) in the xMII transmit signals.

The MM parameter is mandatory when the MAC Merge sublayer (see Clause 99) is instantiated. The MM parameter, when present, can take one of two possible values, i.e., PMAC or EMAC. The value EMAC indicates the SMD-E (SFD) value has been detected at the xMII. The value PMAC indicates that an SMD-S value has been detected at the xMII (see Table 99–1). The MM parameter is not provided when MAC Merge sublayer is not instantiated.

90.4.3.1.2 Condition for generation

This primitive is generated by the gRS sublayer in response to detection of a valid SFD in the data stream transmitted across the xMII transmit signals. Specific conditions for generation of this primitive are described in 90.5.1.

90.4.3.1.3 Effect of receipt

The receipt of this primitive by the TimeSync Client is undefined.

90.4.3.2 TS_RX.indication primitive

This primitive defines the transfer of the indication of an event between gRS and the TimeSync Client.

90.4.3.2.1 Semantics

The semantics of the primitive are as follows:

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TS_RX.indication(SFD, MM)

The SFD parameter can take only one possible value, DETECTED. When asserted (SFD = DETECTED), the TimeSync Client is notified that a valid SFD was detected by the gRS sublayer TS_SFD_Detect_RX function (see 90.5.2) in the xMII receive signals.

The MM parameter is mandatory when the MAC Merge sublayer (see Clause 99) is instantiated. The MM parameter, when present, can take one of two possible values, i.e., PMAC or EMAC. The value EMAC indicates the SMD-E (SFD) value has been detected at the xMII. The value PMAC indicates that an SMD-S value has been detected at the xMII (see Table 99–1). The MM parameter is not provided when MAC Merge sublayer is not instantiated.

90.4.3.2.2 Condition for generation

This primitive is generated by the gRS sublayer in response to detection of a valid SFD in the data stream received across the xMII receive signals. Specific conditions for generation of this primitive are described in 90.5.2.

90.4.3.2.3 Effect of receipt

The receipt of this primitive by the TimeSync Client is undefined.

90.5 generic Reconciliation Sublayer (gRS)

Within the scope of this clause, the term generic Reconciliation Sublayer (gRS) is used to denote any IEEE 802.3 Reconciliation Sublayer (RS) used to interface a MAC with any PHY supporting the TimeSync capability through the xMII. The behavior of the gRS depends on whether a MAC Merge sublayer (see Clause 99) is instantiated above the gRS.

For the purpose of the TimeSync capabilities, two new functions are defined in this subclause, namely TS_SFD_Detect_TX (see 90.5.1) and TS_SFD_Detect_RX (see 90.5.2), which are responsible for generation of the TS_TX.indication and TS_RX.indication service primitives, as defined in 90.4. Figure 90–2 presents the TS_SFD_Detect_TX and TS_SFD_Detect_RX functions and their location within the RS sublayer.

90.5.1 TS_SFD_Detect_TX function

The TS_SFD_Detect_TX function observes the xMII transmit signals.

When the MAC Merge sublayer is not instantiated, the TS_SFD_Detect_TX function detects the occurrence of the Start Frame Delimiter (SFD, see 3.1.1 and 3.2.2) in compliance with the specifications of the given type of the instantiated xMII. The service primitive across the TSSI, i.e., TS_TX.indication shall be generated only when the SFD is detected on the transmit signals of the xMII (SFD=DETECTED).

When the MAC Merge sublayer is instantiated, the TS_SFD_Detect_TX function detects the occurrence of the Start mPacket Delimiter for an express packet or preemptable packet start (SMD-E or SMD-S, see 99.3.3) in compliance with the specifications of the given type of the instantiated xMII. The service primitive across the TSSI, i.e., TS_TX.indication, shall be generated only when the SMD-E or SMD-S is detected on the transmit signals of the xMII (SFD=DETECTED). The value of MM shall indicate whether an SMD-E (MM=EMAC) or an SMD-S (MM=PMAC) was detected.

90.5.2 TS_SFD_Detect_RX function

The TS_SFD_Detect_RX function observes the xMII receive signals.

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When the MAC Merge sublayer is not instantiated, the TS_SFD_Detect_RX function detects the occurrence of the Start Frame Delimiter (SFD, see 3.1.1 and 3.2.2) in compliance with the specifications of the given type of the instantiated xMII. The service primitive across the TSSI, i.e., TS_RX.indication, shall be generated only when the SFD is detected on the receive signals of the xMII (SFD=DETECTED).

When the MAC Merge sublayer is instantiated, the TS_SFD_Detect_RX function detects the occurrence of the Start mPacket Delimiter for an express packet or preemptable packet start (SMD-E or SMD-S, see 99.3.3) in compliance with the specifications of the given type of the instantiated xMII. The service primitive across the TSSI, i.e., TS_RX.indication, shall be generated only when the SMD-E or SMD-S is detected on the transmit signals of the xMII (SFD=DETECTED). The value of MM shall indicate whether an SMD-E (MM=EMAC) or an SMD-S (MM=PMAC) was detected.

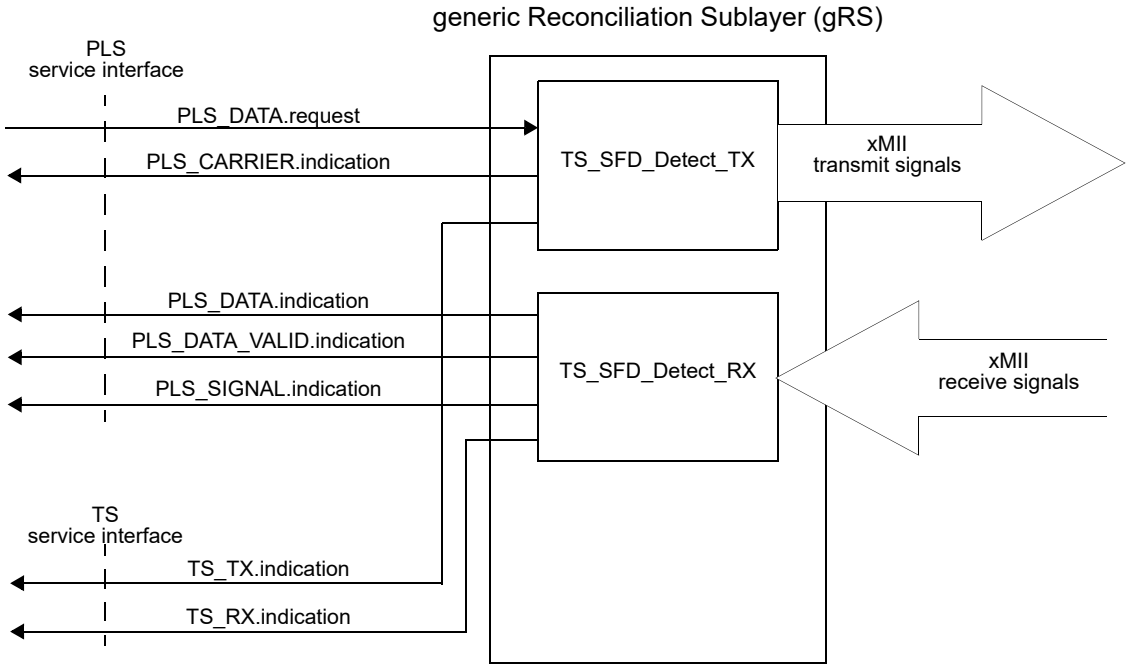

Figure 90–2—TS_SFD_Detect_TX and TS_SFD_Detect_RX functions within the generic Reconciliation Sublayer (gRS)

90.6 Overview of management features

Clause 30 describes the management functions for any of the IEEE Std 802.3 compliant PHYs. Objects defined in Clause 30 for the support of TimeSync capability are summarized below:

— oTimeSync managed object class, as defined in 30.13.1

— aTimeSyncCapabilityTX and aTimeSyncCapabilityRX managed objects, reflecting the status of a series of MDIO capability registers (1.1800, 2.1800, 3.1800, 4.1800, 5.1800, and 6.1800), as defined in 30.13.1.1 and 30.13.1.2, respectively

— aTimeSyncDelayTXmax and aTimeSyncDelayTXmin managed objects, representing the aggregate value of the series of transmit path data delay registers present in the instantiated MDIO registers (for each MMD, in case of multiple instances) 1.1801 through 1.1804, 2.1801 through 2.1804,

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3.1801 through 3.1804, 4.1801 through 4.1804, 5.1801 through 5.1804, and 6.1801 through 6.1804, as defined in 30.13.1.3 and 30.13.1.4, respectively

— aTimeSyncDelayRXmax and aTimeSyncDelayRXmin managed objects, representing the aggregate value of the series of receive path data delay registers present in the instantiated MDIO registers (for each MMD, in case of multiple instances) 1.1805 through 1.1808, 2.1805 through 2.1808, 3.1805 through 3.1808, 4.1805 through 4.1808, 5.1805 through 5.1808, and 6.1805 through 6.1808, as defined in 30.13.1.5 and 30.13.1.6, respectively

The Management Data Input/Output (MDIO) capability described in Clause 45 defines several variables that provide TimeSync status information for the PMD, as shown in Table 90–1:

Table 90–1—Summary of TimeSync features in Clause 45

Register	Name	Reference
1.1800	TimeSync PMA/PMD capability register	45.2.1.175
1.1801 through 1.1804	TimeSync PMA/PMD transmit path data delay	45.2.1.176
1.1805 through 1.1808	TimeSync PMA/PMD receive path data delay	45.2.1.177
2.1800	TimeSync WIS capability register	45.2.2.20
2.1801 through 2.1804	TimeSync WIS transmit path data delay	45.2.2.21
2.1805 through 2.1808	TimeSync WIS receive path data delay	45.2.2.22
3.1800	TimeSync PCS capability register	45.2.3.67
3.1801 through 3.1804	TimeSync PCS transmit path data delay	45.2.3.68
3.1805 through 3.1808	TimeSync PCS receive path data delay	45.2.3.69
4.1800	TimeSync PHY XS capability register	45.2.4.28
4.1801 through 4.1804	TimeSync PHY XS transmit path data delay	45.2.4.29
4.1805 through 4.1808	TimeSync PHY XS receive path data delay	45.2.4.30
5.1800	TimeSync DTE XS capability register	45.2.5.28
5.1801 through 5.1804	TimeSync DTE XS transmit path data delay	45.2.5.29
5.1805 through 5.1808	TimeSync DTE XS receive path data delay	45.2.5.30
6.1800	TimeSync TC capability register	45.2.6.14
6.1801 through 6.1804	TimeSync TC transmit path data delay	45.2.6.15
6.1805 through 6.1808	TimeSync TC receive path data delay	45.2.6.16

90.7 Data delay measurement

The TimeSync capability requires measurement of data delay in the transmit and receive paths, as shown in Figure 90–3. The transmit path data delay is measured from the beginning of the SFD at the xMII input to the beginning of the SFD at the MDI output. The receive path data delay is measured from the beginning of the SFD at the MDI input to the beginning of the SFD at the xMII output.

For a PHY that includes an FEC function, the transmit and receive path data delays may show significant variation depending upon the position of the SFD within the FEC block. However, since the variation due to

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this effect in the transmit path is expected to be compensated by the inverse variation in the receive path, it is recommended that the transmit and receive path data delays be reported as if the SFD is at the start of the FEC block.

The receiver of a multi-lane PHY is expected to include a buffer to compensate for skew between the lanes. This buffer selectively delays each lane such that the lanes are aligned at the buffer output. The earliest arriving lane experiences the most delay through the buffer and the latest arriving lane experiences the least delay through the buffer. The receive path data delay for a multi-lane PHY is reported as if the beginning of the SFD arrived at the MDI input on the lane with the smallest buffer delay.

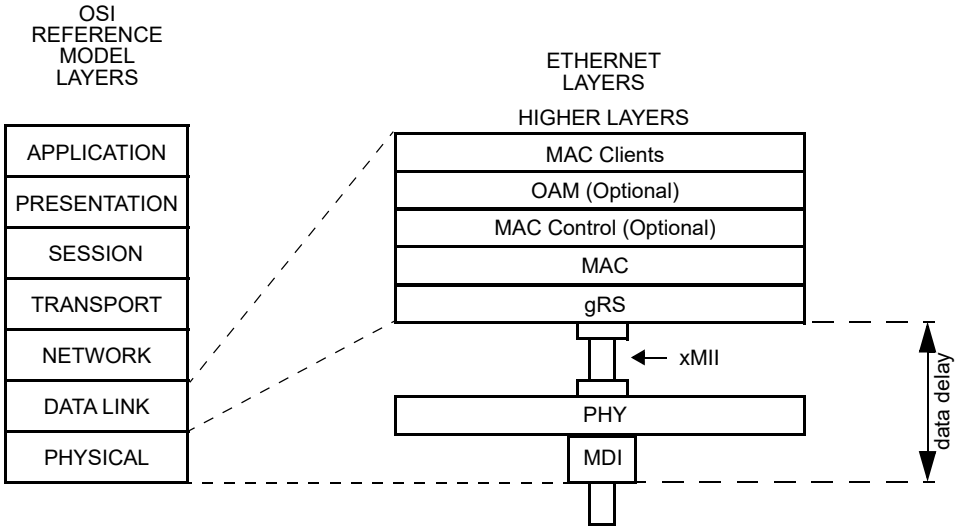

Figure 90–3—Data delay measurement

NOTE 1—The measured data delay in either the transmit or receive path should not include delay resulting from any length of the medium, regardless of the type of the medium used by the given PHY. It is observed that even if any medium-imposed delay is included in the measured data delay, it does not affect the operation of the TimeSync functions and only shifts the timing reference point farther from the MDI.

The obtained data delay measurement shall be reported in the form of a quartet of values; the maximum transmit data delay, the minimum transmit data delay, the maximum receive data delay, and the minimum receive data delay, as defined for the oTimeSync managed object class (30.13.1).

NOTE 2—The data delay values represent only the data delay in the PHY sublayers. The TimeSync Client may need to adjust for delays within the gRS. For example, the TimeSync Client may need to subtract the value of the delay associated with the TS_SFD_Detect_TX function from the sum of the minimum transmit data delay values reported by individual MMD(s). Likewise, the TimeSync Client may need to add the value of the delay associated with the TS_SFD_Detect_RX function to the sum of the maximum receive data delay values reported by individual MMD(s).

NOTE 3—For PHYs that are specified with an FEC sublayer separate from the PCS, the data delay for the FEC sublayer should be included in either the PCS delay registers or the PMA/PMD delay registers of the MMD in which the FEC sublayer is implemented, but not in both.

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90.8 Protocol implementation conformance statement (PICS) proforma for Clause 90, Ethernet support for time synchronization protocols[159]

90.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 90 Ethernet support for time synchronization protocols, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

90.8.2 Identification

90.8.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

90.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 90, Ethernet support for time synchronization protocols
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022)	
Date of Statement	

[159] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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90.8.3 TSSI indication

Item	Feature	Subclause	Value/Comment	Status	Support
*MM	MAC Merge	90.5	A MAC Merge sublayer is instantiated above gRS.	O	Yes [ ] No [ ]
TS_TX	TS_TX.indication generation	90.5.1	TS_TX.indication is generated only when the SFD is detected on the transmit signals of the xMII.	!MM:M	Yes [ ] N/A [ ]
TS_RX	TS_RX.indication generation	90.5.2	TS_RX.indication is generated only when the SFD is detected on the receive signals of the xMII.	!MM:M	Yes [ ] N/A [ ]
TS_T2	TS_TX.indication generation with MAC Merge	90.5.1	TS_TX.indication is generated only when SMD-E or SMD-S is detected on the transmit signals of the xMII.	MM:M	Yes [ ] N/A [ ]
TS_T3	MM parameter for TS_TX	90.5.1	Value of MM parameter indicates whether an SMD-E or SMD-S is detected.	MM:M	Yes [ ] N/A [ ]
TS_R2	TS_RX.indication generation with MAC Merge	90.5.2	TS_RX.indication is generated only when SMD-E or SMD-S is detected on the receive signals of the xMII.	MM:M	Yes [ ] N/A [ ]
TS_R3	MM parameter for TS_RX	90.5.2	Value of MM parameter indicates whether an SMD-E or SMD-S is detected.	MM:M	Yes [ ] N/A [ ]

90.8.4 Data delay reporting

Item	Feature	Subclause	Value/Comment	Status	Support
Report	Data delay reporting format	90.7	Data delay measurement is reported in the form of a quartet of values; the maximum transmit data delay, the minimum transmit data delay, the maximum receive data delay, and the minimum receive data delay, for each MMD instantiated in the device.	M	Yes [ ]

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91. Reed-Solomon forward error correction (RS-FEC) sublayer for 100GBASE-R PHYs

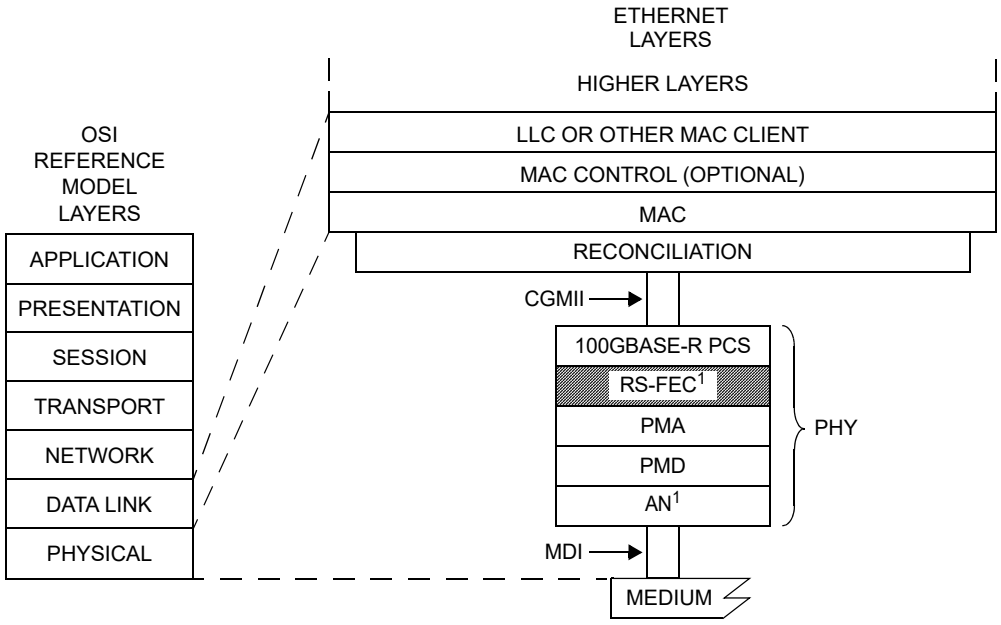
91.1 Overview

91.1.1 Scope

This clause specifies a Reed-Solomon forward error correction (RS-FEC) sublayer for 100GBASE-R PHYs. Annex 91A provides examples of RS-FEC codewords constructed with the method specified in this clause.

91.1.2 Position of RS-FEC in the 100GBASE-R sublayers

Figure 91–1 shows the relationship of the RS-FEC sublayer to the ISO/IEC Open System Interconnection (OSI) reference model.



AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 91–1—RS-FEC relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

91.2 FEC service interface

This subclause specifies the services provided by the RS-FEC sublayer. The service interface is described in an abstract manner and does not imply any particular implementation.

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The FEC service interface is provided to allow the PCS to transfer information to and from the RS-FEC. The PCS may be connected to the RS-FEC using an optional instantiation of the PMA service interface (refer to Annex 83A or Annex 83D) in which case a PMA is the client of the FEC service interface.

The FEC service interface is an instance of the inter-sublayer service interface defined in 80.3. The FEC service interface primitives are summarized as follows:

FEC:IS_UNITDATA_*i*.request
FEC:IS_UNITDATA_*i*.indication
FEC:IS_SIGNAL.indication

The RS-FEC operates on 20 parallel bit streams, hence $i = 0$ to 19. The PCS (or PMA) continuously sends 20 parallel bit streams to the RS-FEC, one per lane, each at a nominal signaling rate of 5.15625 GBd. The RS-FEC continuously sends 20 parallel bit streams to the PCS (or PMA), one per lane, each at a nominal signaling rate of 5.15625 GBd.

The SIGNAL_OK parameter of the FEC:IS_SIGNAL.indication primitive can take one of two values: OK or FAIL. The value is set to OK when the FEC receive function has identified codeword boundaries as indicated by fec_align_status equal to true. That value is set to FAIL when the FEC receive function is unable to reliably establish codeword boundaries as indicated by fec_align_status equal to false. When SIGNAL_OK is FAIL, the rx_bit parameters of the FEC:IS_UNITDATA_*i*.indication primitives are undefined.

If the optional EEE deep sleep capability is supported, then the FEC service interface includes four additional primitives as follows:

FEC:IS_TX_MODE.request
FEC:IS_RX_MODE.request
FEC:IS_RX_TX_MODE.indication
FEC:IS_ENERGY_DETECT.indication

When the tx_mode parameter of the FEC:IS_TX_MODE.request primitive is QUIET or ALERT, the RS-FEC sublayer may disable transmit functional blocks to conserve energy. Otherwise the RS-FEC transmit function operates normally. The value of tx_mode is passed to the client sublayer via the PMA:IS_TX_MODE.request primitive.

When the rx_mode parameter of the FEC:IS_RX_MODE.request primitive is QUIET, the RS-FEC sublayer may disable receive functional blocks to conserve energy. Otherwise the RS-FEC receive function operates normally. The value of rx_mode is passed to the client sublayer via the PMA:IS_RX_MODE.request primitive.

The rx_tx_mode parameter of the FEC:IS_RX_TX_MODE.indication primitive is used to communicate the link partner's value of tx_mode as inferred by the PMA. It is assigned the value that is received via the PMA:IS_RX_TX_MODE.indication primitive.

The energy_detect parameter of the FEC:IS_ENERGY_DETECT.indication primitive is used to communicate that the PMD has detected the return of energy on the interface following a period of quiescence. It is assigned the value that is received via the PMA:IS_ENERGY_DETECT.indication primitive.

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91.3 PMA compatibility

The RS-FEC sublayer requires that the PMA service interface consist of exactly four upstream lanes and exactly four downstream lanes. Therefore, the RS-FEC sublayer may be a client of the PMA sublayer defined in Clause 83 or Clause 135 when the PMA service interface width, *p*, is set to 4. The RS-FEC sublayer may also be a client of the PMA sublayer defined in Clause 94.

In addition, all PMA service interfaces between the RS-FEC sublayer and the PMD sublayer are required to consist of four or fewer upstream lanes and four or fewer downstream lanes. A consequence of this constraint is that a physical instantiation of the ten-lane PMA service interface (CAUI-10) may not be used below the RS-FEC sublayer.

91.4 Delay constraints

The maximum delay contributed by the RS-FEC sublayer (sum of transmit and receive delays at one end of the link) shall be no more than 40 960 bit times (80 pause_quanta or 409.6 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

91.5 Functions within the RS-FEC sublayer

91.5.1 Functional block diagram

A functional block diagram of the RS-FEC sublayer is shown in Figure 91–2.

91.5.2 Transmit function

91.5.2.1 Lane block synchronization

The RS-FEC transmit function forms 20 bit streams by concatenating the bits from each of the 20 FEC:IS_UNITDATA_*i*.request primitives in the order they are received. It obtains lock to the 66-bit blocks in each bit stream using the sync headers and outputs 66-bit blocks. Block lock is obtained as specified in the block lock state diagram shown in Figure 82–12.

91.5.2.2 Alignment lock and deskew

Once the RS-FEC transmit function achieves block lock on a PCS lane, it then begins obtaining alignment marker lock as specified by the alignment marker lock state diagram shown in Figure 82–13. This process identifies the PCS lane number received on a particular lane of the service interface. After alignment marker lock is achieved on all 20 lanes, all inter-lane Skew is removed as specified by the PCS deskew state diagram shown in Figure 82–14. The RS-FEC transmit function shall support a maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps. Skew and Skew Variation are defined in 80.5.

91.5.2.3 Lane reorder

PCS lanes can be received on different lanes of the service interface from which they were originally transmitted due to Skew between lanes and multiplexing by the PMA. The RS-FEC transmit function shall order the PCS lanes according to the PCS lane number.

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91.5.2.4 Alignment marker removal

After all PCS lanes are aligned and deskewed, the PCS lanes are multiplexed together in the proper order to reconstruct the original stream of blocks and the alignment markers are removed from the data stream. Note that an alignment marker is always removed when am_lock is true for a given PCS lane even if it does not match the expected alignment marker value (due to a bit error for example). Repeated alignment marker errors result in am_lock being set to false for a given PCS lane, but until that happens it is sufficient to remove the block in the alignment marker position.

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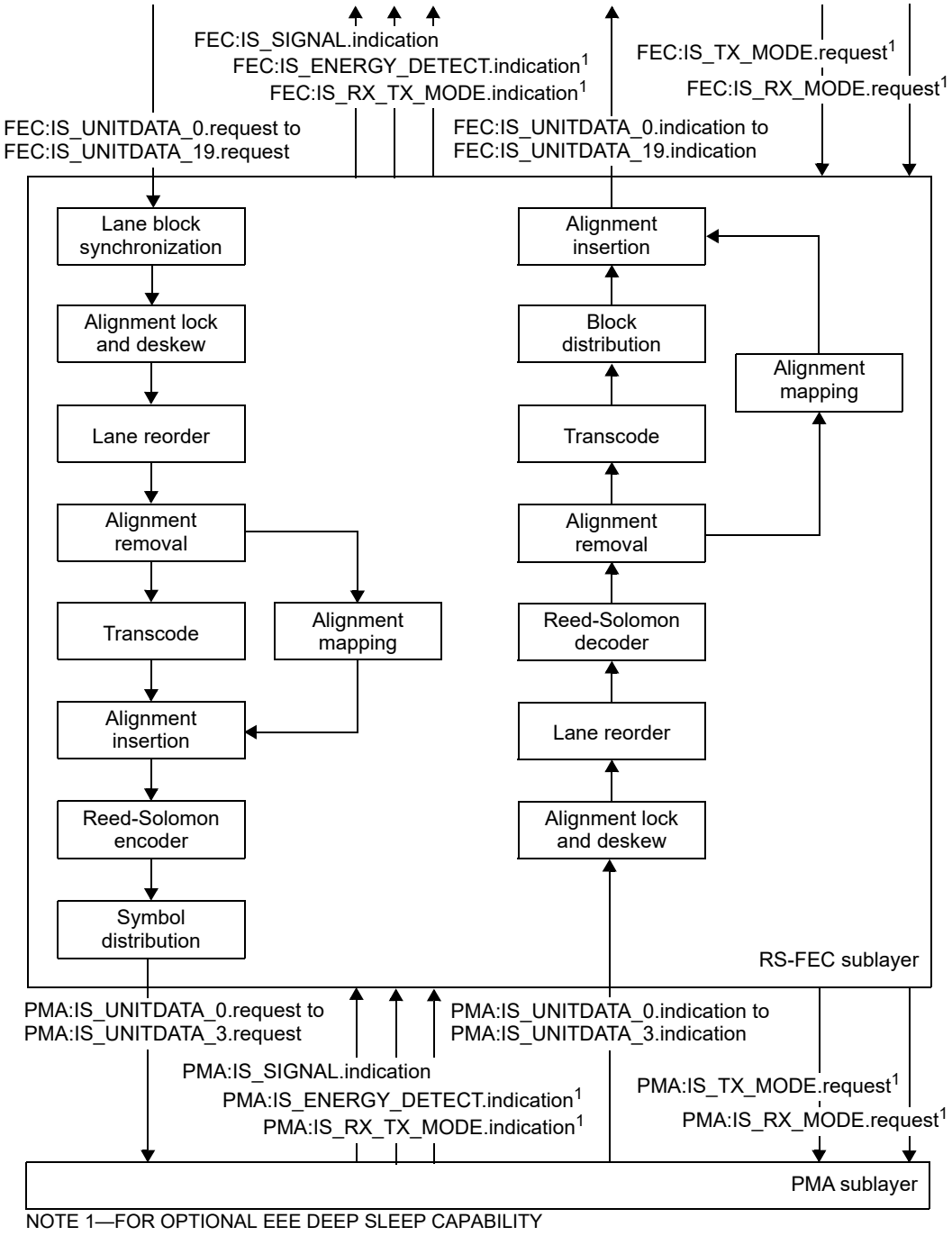

Figure 91–2—Functional block diagram

For the optional EEE deep sleep capability, transitions between normal alignment markers and Rapid Alignment Markers (RAMs) result in changes in relative position and frequency of alignment markers. These transitions are detected by the Transmit LPI state diagram (see Figure 91–10), and this information is used by the alignment marker removal function to determine which 66-bit blocks are to be removed.

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As part of the alignment marker removal process, the BIP_3 field is compared to the calculated Bit Interleaved Parity (BIP) value (see 82.2.8) for each PCS lane. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 1.230 to 1.249) is incremented by one each time the calculated BIP value does not equal the value received in the BIP_3 field. The bit error ratio in the data received from the local PCS can be estimated by dividing the BIP block error ratio by a factor of 1 081 344.

NOTE—The data received from the local PCS is processed by the RS-FEC transmit function without error correction.

91.5.2.5 64B/66B to 256B/257B transcoder

The transcoder constructs a 257-bit block, tx_scrambled<256:0>, from a group of four 66-bit blocks, tx_coded_*j*<65:0> where *j*=0 to 3. For each group of four 66-bit blocks, *j*=3 corresponds to the most recently received block. Bit 0 in each 66-bit block is the first bit received and corresponds to the first bit of the synchronization header.

If for all *j*=0 to 3, tx_coded_*j*<0>=0 and tx_coded_*j*<1>=1, tx_xcoded<256:0> shall be constructed as follows:

a) tx_xcoded<0> = 1
b) tx_xcoded<(64*j*+64):(64*j*+1)> = tx_coded_*j*<65:2> for *j*=0 to 3

If for all *j*=0 to 3, tx_coded_*j*<0> ≠ tx_coded_*j*<1> (valid synchronization header) and for any *j*=0 to 3, tx_coded_*j*<0>=1 and tx_coded_*j*<1>=0, tx_xcoded<256:0> shall be constructed as follows:

a1) tx_xcoded<0> = 0
b1) tx_xcoded<*j*+1> = tx_coded_*j*<1> for *j*=0 to 3
c1) Let *c* be the smallest value of *j* such that tx_coded_*c*<0>=1. In other words, tx_coded_*c* is the first 66-bit control block that was received in the current group of four blocks.
d1) Let tx_payloads<(64*j*+63):64*j*> = tx_coded_*j*<65:2> for *j*=0 to 3
e1) Omit tx_coded_*c*<9:6>, which is the second nibble (based on transmission order) of the block type field for tx_coded_*c,* from tx_xcoded per the following expressions.
tx_xcoded<(64*c*+8):5> = tx_payloads<(64*c*+3):0>
tx_xcoded<256:(64*c*+9)> = tx_payloads<255:(64*c*+8)>

If for any *j*=0 to 3, tx_coded_*j*<0> = tx_coded_*j*<1> (invalid synchronization header), tx_xcoded<256:0> shall be constructed as follows:

a2) tx_xcoded<0> = 0
b2) tx_xcoded<*j*+1> = 1 for *j*=0 to 3
c2) Let tx_payloads<(64*j*+63):64*j*> = tx_coded_*j*<65:2> for *j*=0 to 3
d2) Omit the second nibble (based on transmission order) of tx_coded_0 per the following expressions.
tx_xcoded<8:5> = tx_payloads<3:0>
tx_xcoded<256:9> = tx_payloads<255:8>

Several examples of the construction of tx_xcoded<256:0> are shown in Figure 91–3. In Figure 91–3, d_*j* indicates the *j*th 66-bit block contains only data octets, c_*j* indicates the *j*th 66-bit block contains one or more control characters, f_*j* denotes the first nibble of the block type field for 66-bit block *j*, and s_*j* denotes the second nibble of the block type field for 66-bit block *j*.

Finally, scramble the first 5 bits, based on transmission order, of tx_xcoded<256:0> to yield tx_scrambled<256:0> as follows:

a3) Set tx_scrambled<4:0> to the result of the bit-wise exclusive-OR of the tx_xcoded<4:0> and tx_xcoded<12:8>.

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b3) Set tx_scrambled<256:5> to tx_xcoded<256:5>

For each 257-bit block, bit 0 shall be the first bit transmitted.

91.5.2.6 Alignment marker mapping and insertion

The alignment markers that were removed per 91.5.2.4 are re-inserted after being processed by the alignment marker mapping function. The alignment marker mapping function compensates for the operation of the symbol distribution function defined in 91.5.2.8 and rearranges the alignment marker bits so that they appear on the FEC lanes intact and in the desired sequence. This preserves the properties of the alignment markers (e.g., DC balance, transition density) and provides a deterministic pattern for the purpose of synchronization. The RS-FEC receive function uses knowledge of this mapping to determine the FEC lane that is received on a given lane of the PMA service interface, to compensate for skew between FEC lanes, and to identify RS-FEC codeword boundaries.

The alignment marker mapping function operates on a group of 20 aligned and reordered alignment markers. Let am_tx_x<65:0> be the alignment marker for PCS lane x, x=0 to 19, where bit 0 is the first bit transmitted. The alignment markers shall be mapped to am_txmapped<1284:0> in a manner that yields the same result as the following process.

For x=0 to 19, amp_tx_x<63:0> is constructed as follows:

a) Set y = 0 when $x \le 3$, set y = 16 when $x \ge 16$ and four_lane_pmd, otherwise set $y = x$.
b) amp_tx_x<23:0> is set to M_0, M_1, and M_2 as shown in Figure 82–9 (bits 25 to 2) using the values in Table 82–2 for PCS lane number y. If am_tx_x corresponds to a Rapid Alignment marker, then the M_4, M_5, and M_6 values are used instead (see Figure 82–11).
c) amp_tx_x<31:24> = am_tx_x<33:26>
d) amp_tx_x<55:32> is set to M_4, M_5, and M_6 as shown in Figure 82–9 (bits 57 to 34) using the values in Table 82–2 for PCS lane number y. If am_tx_x corresponds to a Rapid Alignment marker, then the M_0, M_1, and M_2 values are used instead (see Figure 82–11).
e) amp_tx_x<63:56> = am_tx_x<65:58>

This process replaces the fixed bytes of the alignment markers received, possibly with errors, with the values from Table 82–2. In addition it substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 1, 2, and 3 with the fixed bytes for the alignment marker corresponding to PCS lane 0. Similarly when used with a four-lane PMD, it substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16. The variable bytes BIP or CD are unchanged. This process simplifies receiver synchronization since the receiver only needs to search for the fixed bytes corresponding to PCS lane 0 on each FEC lane. When the optional EEE deep sleep capability is supported, the receiver only needs to search for the fixed bytes corresponding to PCS lanes 0 and 16.

Construct a matrix of 4 rows and 320 columns, am_txpayloads, as shown in Figure 91–4. Given i=0 to 3, j=0 to 4, and x=i+4j, the matrix is derived per the following expression:

am_txpayloads<i, (64j+63):64j> = amp_tx_x<63:0>

Given i=0 to 3, k=0 to 31, and y=i+4k, am_txmapped may then be derived from am_txpayloads per the following expression:

am_txmapped<(10y+9):10y> = am_txpayloads<i, (10k+9):10k>

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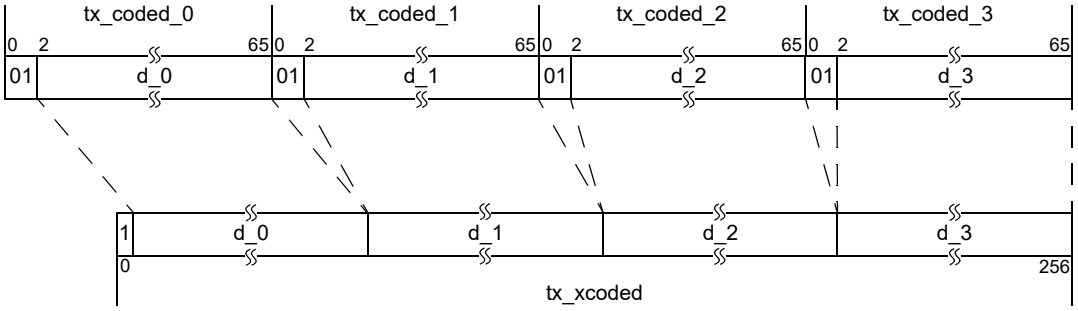
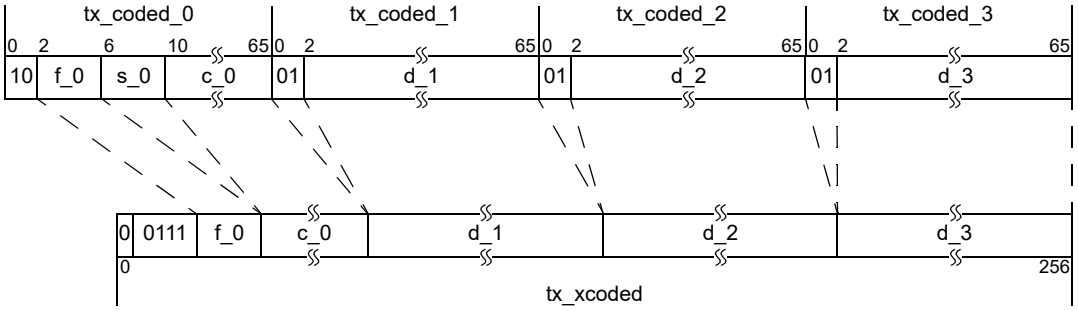
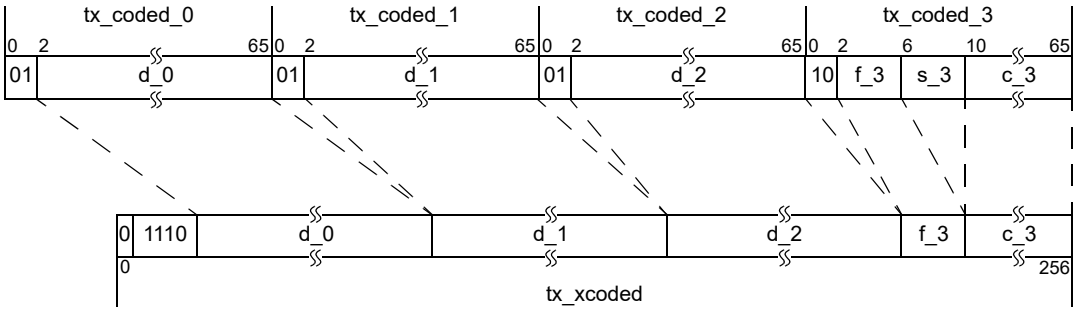


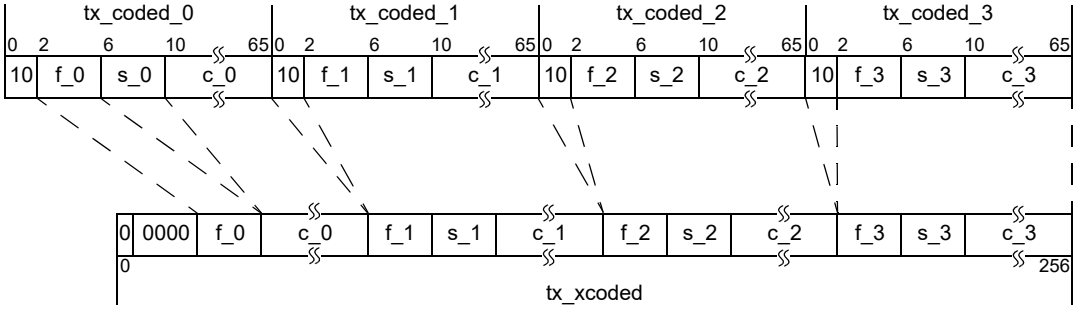
Example 1: All data blocks



Example 2: Control block followed by three data blocks



Example 3: Three data blocks followed by a control block



Example 4: All control blocks

Figure 91–3—Examples of the construction of tx_xcoded

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A 5-bit pad is appended to the mapped alignment markers to yield the equivalent of five 257-bit blocks. The pad bits, am_txmapped<1284:1280>, shall be set to the binary values 00101 and 11010 (the leftmost bit is assigned to the highest bit index) in an alternating pattern. In other words, if a pad value of 00101 is used for the current iteration of the mapping function, a value of 11010 is used in the next iteration and vice versa.

The result of the alignment marker mapping function is the deterministic mapping between alignment marker payloads and FEC lanes shown in Figure 91–4.

As a result of this process, the BIP_3 and BIP_7 fields from normal alignment markers are carried across the link protected by FEC. These fields cannot be used to monitor errors on the link protected by FEC as 64B/66B to 256B/257B transcoding and Reed-Solomon encoding alters the bit sequence. However, these fields may again be used to monitor errors after the original bit sequence is restored, i.e., following Reed-Solomon decoding and 256B/257B to 64B/66B transcoding.

One group of aligned and reordered alignment markers are mapped every 20 × 16384 66-bit blocks. This corresponds to 4096 Reed-Solomon codewords (refer to 91.5.2.7). The mapped alignment markers, am_txmapped<1284:0> shall be inserted as the first 1285 message bits to be transmitted from every 4096th codeword.

For the optional EEE deep sleep capability, when tx_lpi_active is true, one group of Rapid Alignment Markers (see 82.2.9) are mapped every 20 × 8 66-bit blocks. This corresponds to 2 Reed-Solomon codewords. The mapped Rapid Alignment Markers, am_txmapped<1284:0> shall be inserted as the first 1285 message bits to be transmitted from every other codeword.

The first 257-bit block inserted after am_txmapped shall correspond to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective lane.

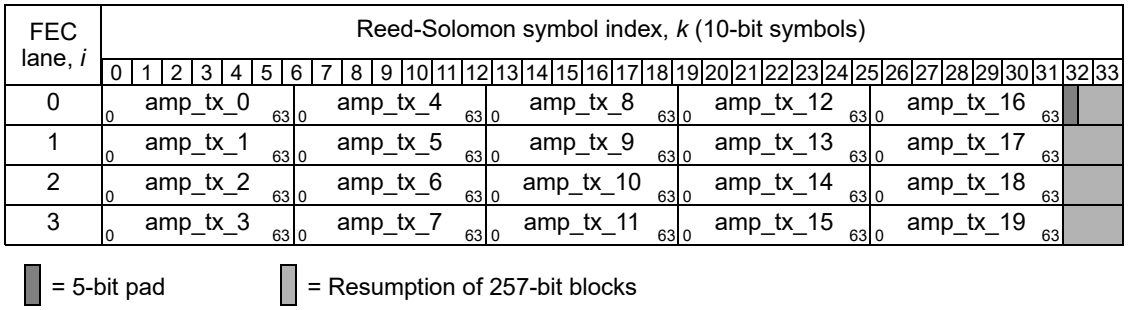

Figure 91–4—Alignment marker mapping to FEC lanes

91.5.2.7 Reed-Solomon encoder

The RS-FEC sublayer employs a Reed-Solomon code operating over the Galois Field GF(2^{10}) where the symbol size is 10 bits. The encoder processes k message symbols to generate $2t$ parity symbols, which are then appended to the message to produce a codeword of $n=k+2t$ symbols. For the purposes of this clause, a particular Reed-Solomon code is denoted RS(n,k).

When used to form a 100GBASE-CR4, 100GBASE-KR4, or 100GBASE-SR4 PHY, the RS-FEC sublayer shall implement RS(528,514). When used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PHY, the RS-FEC sublayer shall implement RS(544,514). Each k-symbol message corresponds to 20 257-bit blocks produced by the transcoder. Each code is based on the generating polynomial given by Equation (91–1).

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$$g(x) = \prod_{j=0}^{2t-1}(x-\alpha^j) = g_{2t}x^{2t} + g_{2t-1}x^{2t-1} + \ldots + g_1 x + g_0 \quad (91\text{–}1)$$

In Equation (91–1), α is a primitive element of the finite field defined by the polynomial $x^{10}+x^3+1$.

Equation (91–2) defines the message polynomial $m(x)$ whose coefficients are the message symbols m_{k-1} to m_0.

$$m(x) = m_{k-1}x^{n-1} + m_{k-2}x^{n-2} + \ldots + m_1 x^{2t+1} + m_0 x^{2t} \quad (91\text{–}2)$$

Each message symbol m_i is the bit vector $(m_{i,9}, m_{i,8}, \ldots, m_{i,1}, m_{i,0})$, which is identified with the element $m_{i,9}\alpha^9 + m_{i,8}\alpha^8 + \ldots + m_{i,1}\alpha + m_{i,0}$ of the finite field. The message symbols are composed of the bits of the transcoded blocks tx_scrambled (including a mapped group of alignment markers when appropriate) such that bit 0 of the first transcoded block in the message (or am_txmapped<0>) is bit 0 of m_{k-1} and bit 256 of the last transcoded block in the message is bit 9 of m_0. The first symbol input to the encoder is m_{k-1}.

Equation (91–3) defines the parity polynomial $p(x)$ whose coefficients are the parity symbols p_{2t-1} to p_0.

$$p(x) = p_{2t-1}x^{2t-1} + p_{2t-2}x^{2t-2} + \ldots + p_1 x + p_0 \quad (91\text{–}3)$$

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This may be computed using the shift register implementation illustrated in Figure 91–5. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0, is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x, $c_{n-1} = m_{k-1}$ is transmitted first and the coefficient of the lowest power of x, $c_0 = p_0$ is transmitted last. The first bit transmitted from each symbol is bit 0.

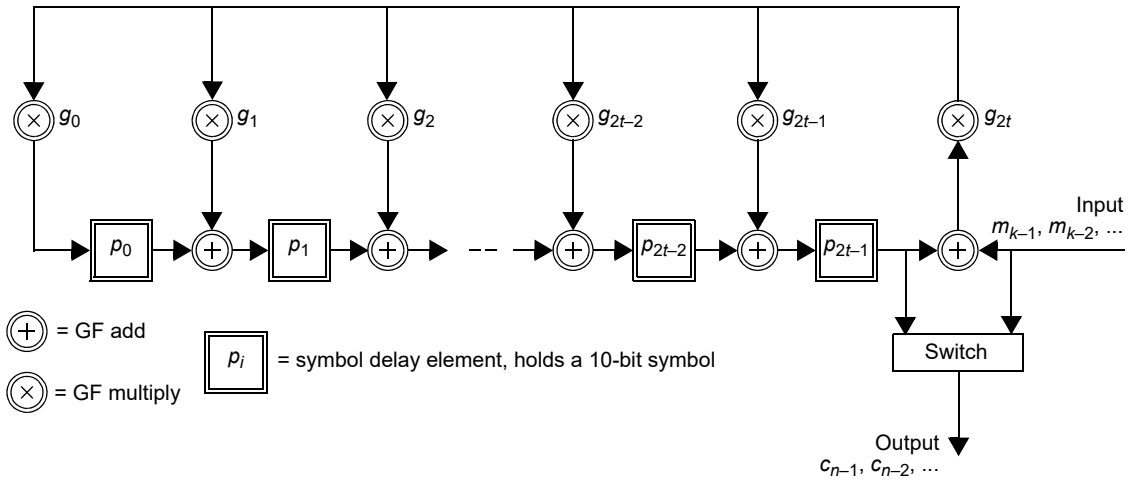

Figure 91–5—Reed-Solomon encoder functional model

The coefficients of the generator polynomial for each code are presented in Table 91–1. Example codewords for each code are provided in Annex 91A.

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Table 91–1—Coefficients of the generator polynomial g_i (decimal)

i	RS(528,514)	RS(544,514)	*i*	RS(528,514)	RS(544,514)	*i*	RS(528,514)	RS(544,514)
0	432	523	11	701	883	22		565
1	290	834	12	6	503	23		108
2	945	128	13	904	942	24		1
3	265	158	14	1	385	25		552
4	592	185	15		495	26		230
5	391	127	16		720	27		187
6	614	392	17		94	28		552
7	900	193	18		132	29		575
8	925	610	19		593	30		1
9	656	788	20		249			
10	32	361	21		282			

91.5.2.8 Symbol distribution

Once the data has been Reed-Solomon encoded, it shall be distributed to 4 FEC lanes, one 10-bit symbol at a time in a round robin distribution from the lowest to the highest numbered FEC lane. The distribution process is shown in Figure 91–6.

When used to form a 100GBASE-KP4 PHY, the PMA:IS_UNITDATA_*i*.request primitive is defined to include an additional parameter (refer to 94.2.1.1.1). At the beginning of an FEC codeword, the parameter start=TRUE is asserted for the first bit of the first four symbols of the codeword transferred across the four primitives. Otherwise the parameter start is set to FALSE.

91.5.2.9 Transmit bit ordering

The transmit bit ordering is illustrated in Figure 91–6.

91.5.3 Receive function

91.5.3.1 Alignment lock and deskew

The RS-FEC receive function forms 4 bit streams by concatenating the bits from each of the 4 PMA:IS_UNITDATA_*i*.indication primitives in the order they are received. It obtains lock to the alignment markers as specified by the FEC synchronization state diagram shown in Figure 91–8.

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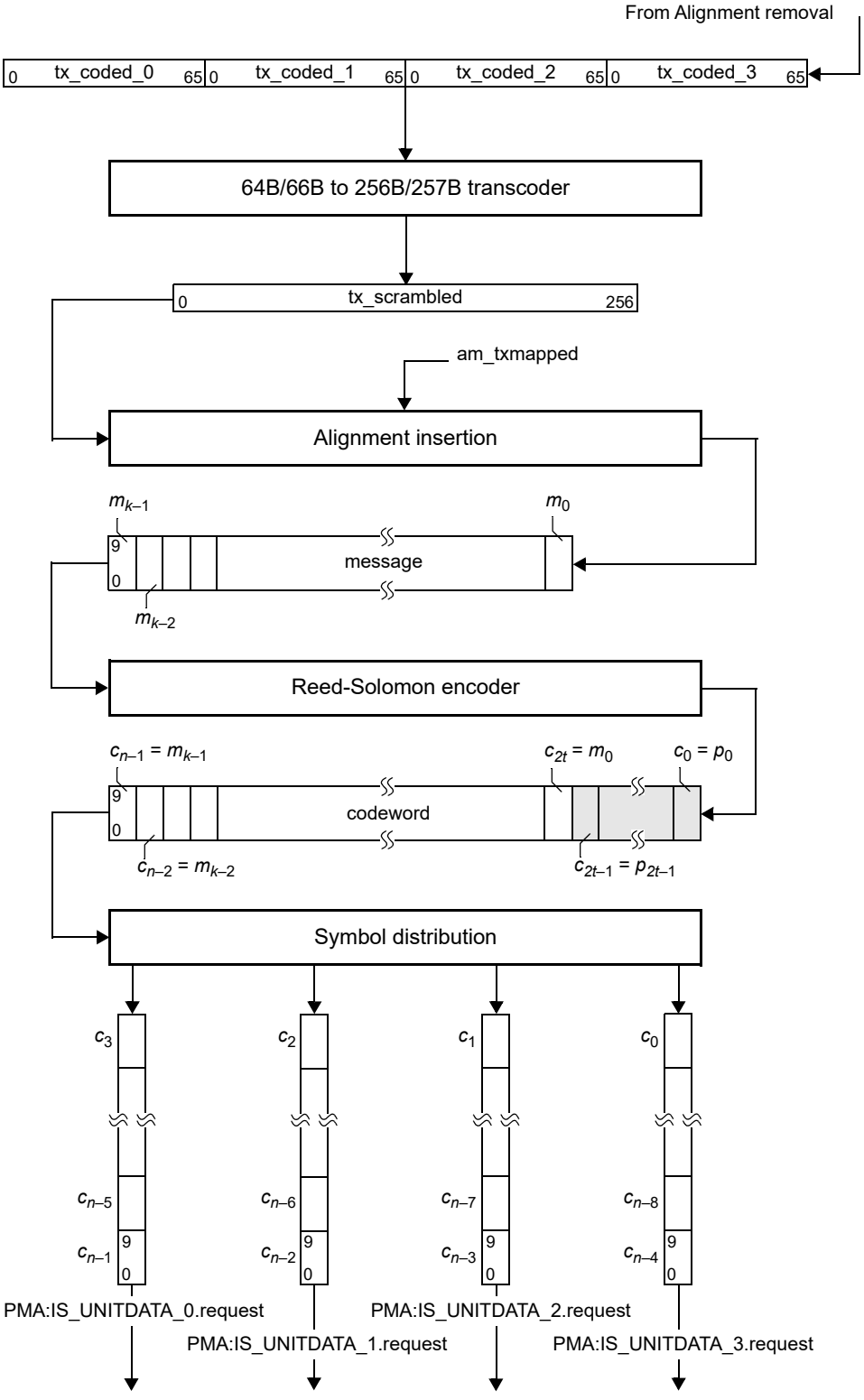

Figure 91–6—Transmit bit ordering

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After alignment marker lock is achieved on all 4 lanes, all inter-lane Skew is removed as specified by the FEC alignment state diagram shown in Figure 91–9. The FEC receive function shall support a maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns.

The 100GBASE-KP4 PMA transmit function (refer to 94.2.2) inserts PMA-specific overhead that is aligned with the start of a Reed-Solomon codeword. The 100GBASE-KP4 PMA receive function (refer to 94.2.3) synchronizes to this overhead and indicates the first bit of each of the first four symbols in a codeword by setting the PMA:IS_UNITDATA_*i*.indication parameter start=TRUE (see 94.2.1.2).

91.5.3.2 Lane reorder

FEC lanes can be received on different lanes of the service interface from which they were originally transmitted. The FEC receive function shall order the FEC lanes according to the FEC lane number (see 91.5.2.6). The FEC lane number is defined by the sequence of alignment markers that are mapped to each FEC lane.

After all FEC lanes are aligned, deskewed, and reordered, the FEC lanes are multiplexed together in the proper order to reconstruct the original stream of FEC codewords.

91.5.3.3 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the codeword, corrects them as necessary, and discards the parity symbols. The message symbols correspond to 20 transcoded blocks rx_scrambled.

When used to form a 100GBASE-CR4, 100GBASE-KR4, or 100GBASE-SR4 PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=7 symbol errors in a codeword. When used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword. The RS-FEC sublayer shall also be capable of indicating when an errored codeword was not corrected. The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10^{-6}. This limit is also expected to apply for t+2 errors, t+3 errors, and so on.

The Reed-Solomon decoder may provide the option to perform error detection without error correction to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_correction_ability variable (see 91.6.8). When the option is provided, it is enabled by the assertion of the FEC_bypass_correction_enable variable (see 91.6.1). This option shall not be used when the RS-FEC sublayer is used to form part of a 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-SR4, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PHY.

NOTE—The PHY may rely on the error correction capability of the RS-FEC sublayer to achieve its performance objectives. It is recommended that acceptable performance of the underlying link is verified before error correction is bypassed.

The Reed-Solomon decoder indicates errors to the PCS sublayer by intentionally corrupting 66-bit block synchronization headers. When the decoder determines that a codeword contains errors (when the bypass correction feature is enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled), it shall ensure that, for every other 257-bit block within the codeword starting with the first (1st, 3rd, 5th, etc.), the synchronization header for the first 66-bit block at the output of the 256B/257B to 64B/66B transcoder, rx_coded_0<1:0>, is set to 11. In addition, it shall ensure rx_coded_0<1:0> corresponding to the 6th 257-bit block and rx_coded_3<1:0> corresponding to the last (20th) 257-bit block in the codeword are set to 11. This causes the PCS to discard all frames 64 bytes and larger that are fully or partially within the codeword.

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The Reed-Solomon decoder may optionally provide the ability to bypass the error indication feature to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_indication_ability variable (see 91.6.9). When the option is provided it is enabled by the assertion of the FEC_bypass_indication_enable variable (see 91.6.2).

When FEC_bypass_correction_enable is asserted, the decoder shall not bypass error indication and the value of FEC_bypass_indication_enable has no effect.

When FEC_bypass_indication_enable is asserted, additional error monitoring is performed by the RS-FEC sublayer to reduce the likelihood that errors in a packet are not detected. The Reed-Solomon decoder counts the number of symbol errors detected on all four FEC lanes in consecutive non-overlapping blocks of 8192 codewords. When the number of symbol errors in a block of 8192 codewords exceeds *K*, the Reed-Solomon decoder shall cause synchronization header rx_coded<1:0> of each subsequent 66-bit block that is delivered to the PCS to be assigned a value of 00 or 11 for a period of 60 ms to 75 ms. As a result, the PCS sets hi_ber=true, which inhibits the processing of received packets. When Auto-Negotiation is supported and enabled, assertion of hi_ber causes Auto-Negotiation to restart.

For the optional EEE deep sleep capability, the error monitor employed when FEC_bypass_indication_enable is asserted shall be disabled when rx_lpi_active=true. The next block of 8192 codewords considered by the error monitor shall begin on the codeword boundary following the transition of rx_lpi_active from true to false.

When the RS-FEC sublayer is used to form a 100GBASE-CR4, 100GBASE-KR4, or 100GBASE-SR4 PHY, the symbol error threshold shall be *K*=417. When the RS-FEC sublayer is used to form a 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PHY, the symbol error threshold shall be *K*=6380.

91.5.3.3.1 FEC Degraded SER (optional)

For 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 PHYs an optional FEC degraded symbol error ratio function is available.

The Reed-Solomon decoder may optionally provide the ability to indicate a degradation of the received signal. The presence of this option is indicated by the assertion of the FEC_degraded_SER_ability variable (see 91.6.11). When the option is provided it is enabled by the assertion of the FEC_degraded_SER_enable variable (see 91.6.4).

When FEC_degraded_SER_enable is asserted, additional error monitoring is performed by the FEC. The Reed-Solomon decoder counts the total number of symbol errors detected in consecutive non-overlapping blocks of FEC_degraded_SER_interval codewords (see 91.6.7). If the decoder determines that a codeword is uncorrectable, the number of symbol errors detected is increased by 16. When the number of symbol errors exceeds the threshold set in FEC_degraded_SER_activate_threshold (see 91.6.5), the FEC_degraded_SER bit (see 91.6.12) is set. At the end of each interval, if the number of symbol errors is less than the threshold set in FEC_degraded_SER_deactivate_threshold (see 91.6.6), the FEC_degraded_SER bit is cleared. The value of the FEC_degraded_SER bit is unspecified if the value of FEC_degraded_SER_activate_threshold is less than the value of FEC_degraded_SER_deactivate_threshold.

If either FEC_degraded_SER_ability or FEC_degraded_SER_enable is deasserted then the FEC_degraded_SER bit is cleared.

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91.5.3.4 Alignment marker removal

The first 1285 message bits in every 4096th codeword is the vector am_rxmapped<1284:0> where bit 0 is the first bit received. The specific codewords that include this vector are indicated by the alignment lock and deskew function (refer to 91.5.3.1).

For the optional EEE deep sleep capability, transitions between normal alignment markers and Rapid Alignment Markers result in changes in the relative position and frequency of am_rxmapped<1284:0>. These transitions are detected by the Receive LPI state diagram (see Figure 91–11) and this information is used by the alignment marker removal function to determine which bits are to be removed. When rx_lpi_active is true, the first 1285 message bits in every other codeword is the vector am_rxmapped<1284:0>.

The vector am_rxmapped shall be removed prior to transcoding.

91.5.3.5 256B/257B to 64B/66B transcoder

The transcoder extracts a group of four 66-bit blocks, rx_coded_*j*<65:0> where *j*=0 to 3, from each 257-bit block rx_scrambled<256:0>. Bit 0 of the 257-bit block is the first bit received.

First, descramble the first 5 bits, based on reception order, of rx_scrambled<256:0> to yield rx_xcoded<256:0> as follows.

a) Set rx_xcoded<4:0> to the result of the bit-wise exclusive-OR of the rx_scrambled<4:0> and rx_scrambled<12:8>.
b) Set rx_xcoded<256:5> to rx_scrambled<256:5>.

If rx_xcoded<0> is 1, rx_coded_*j*<65:0> for *j*=0 to 3 shall be derived as follows.

a1) rx_coded_*j*<65:2> = rx_xcoded<(64*j*+64):(64*j*+1)> for *j*=0 to 3
b1) rx_coded_*j*<0>=0 and rx_coded_*j*<1>=1 for all *j*=0 to 3

If rx_xcoded<0> is 0 and any rx_xcoded<*j*+1>=0 for *j*=0 to 3, rx_coded_*j*<65:0> for *j*=0 to 3 shall be derived as follows.

a2) Let *c* be the smallest value of *j* such that rx_xcoded<*j*+1>=0. In other words, rx_coded_*c* is the first 66-bit control block in the resulting group of four blocks.
b2) Let rx_payloads be a vector representing the payloads of the four 66-bit blocks. It is derived using the following expressions:
rx_payloads<(64*c*+3):0> = rx_xcoded<(64*c*+8):5>
rx_payloads<(64*c*+7):(64*c*+4)> = 0000 (an arbitrary value that is later replaced by s_*c*)
rx_payloads<255:(64*c*+8)> = rx_xcoded<256:(64*c*+9)>
c2) rx_coded_*j*<65:2> = rx_payloads<(64*j*+63):64*j*> for *j*=0 to 3
d2) Let f_*c*<3:0> = rx_coded_*c*<5:2> be the scrambled first nibble (based on transmission order) of the block type field for rx_coded_*c*.
e2) Descramble f_*c*<3:0> to yield g<3:0> per the following expression where "^" denotes the exclusive-OR operation. When *c*=0, rx_coded_(*c*–1) corresponds to rx_coded_3 from the previous 257-bit block.
g<*i*> = f_*c*<*i*> ^ rx_coded_(*c*–1)<*i*+8> ^ rx_coded_(*c*–1)<*i*+27> for *i*=0 to 3
f2) The block type field may be uniquely identified by either its most or least significant nibble. Since g<3:0> is the least significant nibble of the block type field (per the transmission order), derive h<3:0> by cross-referencing to g<3:0> using Figure 82–5. For example, if g<3:0> is 0xE then h<3:0> is 0x1. If no match to g<3:0> is found, h<3:0> is set to 0000.
g2) If rx_xcoded<*j*+1>=0, rx_coded_*j*<0>=1 and rx_coded_*j*<1>=0 for *j*=0 to 3

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h2) If rx_xcoded<*j*+1>=1, rx_coded_*j*<0>=0 and rx_coded_*j*<1>=1 for *j*=0 to 3
i2) If h<3:0> = 0000, rx_coded_*c*<1>=1 (invalidate synchronization header)

If rx_xcoded<0> is 0 and all rx_xcoded<*j*+1>=1 for *j*=0 to 3, rx_coded_*j*<65:0> for *j*=0 to 3 shall be derived as follows.

a3) Set *c* = 0 and h<3:0> = 0000.
b3) Let rx_payloads be a vector representing the payloads of the four 66-bit blocks. It is derived using the following expressions.
rx_payloads<(64*c*+3):0> = rx_xcoded<(64*c*+8):5>
rx_payloads<(64*c*+7):(64*c*+4)> = 0000 (an arbitrary value that is later replaced by s_*c*)
rx_payloads<255:(64*c*+8)> = rx_xcoded<256:(64*c*+9)>
c3) rx_coded_*j*<65:2> = rx_payloads<(64*j*+63):(64*j*)> for *j*=0 to 3
d3) rx_coded_*j*<0>=0 and rx_coded_*j*<1>=0 for *j*=0 and 2
e3) rx_coded_*j*<0>=1 and rx_coded_*j*<1>=1 for *j*=1 and 3

If rx_xcoded<0> is 0, scramble h<3:0> to yield s_*c*<3:0> and assign it to rx_coded_*c* per the following expressions.

a4) s_*c*<*i*> = h<*i*> ^ rx_coded_(*c*–1)<*i*+12> ^ rx_coded_(*c*–1)<*i*+31> for *i*=0 to 3
b4) rx_coded_*c*<9:6> = s_*c*<3:0>

The 66-bit blocks are transmitted in order from *j*=0 to 3. Bit 0 of each block is the first bit transmitted.

91.5.3.6 Block distribution

After the data has been transcoded, it shall be distributed to multiple PCS lanes, one 66-bit block at a time in a round robin distribution from the lowest to the highest numbered PCS lanes. The distribution process is shown in Figure 82–6.

91.5.3.7 Alignment marker mapping and insertion

The alignment marker mapping function compensates for operation of lane reorder function (refer to 91.5.3.2) to derive the PCS lane alignment markers, am_rx_*x*<65:0> for *x*=0 to 19, from am_rxmapped<1284:0> (refer to 91.5.3.4).

The alignment markers shall be derived from am_rxmapped<1284:0> in a manner that yields the same result as the following process.

Given *i*=0 to 3, *k*=0 to 31, and *y*=*i*+4*k*, am_rxpayloads may be derived from am_rxmapped per the following expression:

am_rxpayloads<*i*, (10*k*+9):10*k*> = am_rxmapped<(10*y*+9):10*y*>

The 5-bit pad am_rxmapped<1284:1280> is ignored. Given *i*=0 to 3, *j*=0 to 4, and *x*=*i*+4*j*, amp_rx_*x* may be derived from am_rxpayloads by the following expression:

amp_rx_*x*<63:0> = am_rxpayloads<*i*, (64*j*+63):64*j*>

For *x*=0 to 19, am_rx_*x*<65:0> is constructed as follows:

a) am_rx_*x*<0>=1 and am_rx_*x*<1>=0.

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b) am_rx_*x*<25:2> is set to M_0, M_1, and M_2 as shown in Figure 82–9 using the values in Table 82–2 for PCS lane number *x*. If amp_rx_*x* corresponds to a Rapid Alignment marker, then the M_4, M_5, and M_6 values are used instead (see Figure 82–11).
c) am_rx_*x*<33:26> = amp_rx_*x*<31:24>.
d) am_rx_*x*<57:34> is set to M_4, M_5, and M_6 as shown in Figure 82–9 using the values in Table 82–2 for PCS lane number *x*. If amp_rx_*x* corresponds to a Rapid Alignment marker, then the M_0, M_1, and M_2 values are used instead (see Figure 82–11).
e) am_rx_*x*<65:58> = amp_rx_*x*<63:56>.

One vector is mapped to 20 alignment markers every 4096 Reed-Solomon codewords (see 91.5.3.4). The alignment markers are simultaneously transmitted on the 20 PCS lanes after every 16383rd column of 20 66-bit blocks.

For the optional EEE deep sleep capability, when rx_lpi_active is true, one vector is mapped to 20 Rapid Alignment Markers every 2 Reed-Solomon codewords. The Rapid Alignment Markers are simultaneously transmitted on the 20 PCS lanes after every 7th column of 20 66-bit blocks.

The alignment markers am_rx_0 to am_rx_3 shall be inserted so that they are immediately followed by rx_coded_0 to rx_coded_3, respectively, as derived from the first 257-bit block following am_rxmapped. Similarly am_rx_4 to am_rx_7 are followed by the 66-bit blocks corresponding to the second 257-bit block following am_rxmapped, and so on.

91.5.3.8 Receive bit ordering

The receive bit ordering is illustrated in Figure 91–7. This illustration shows the case where the FEC lanes appear across the PMA:IS_UNITDATA_*i*.indication primitives in the correct order.

91.5.4 Detailed functions and state diagrams

91.5.4.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, functions, and counters. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

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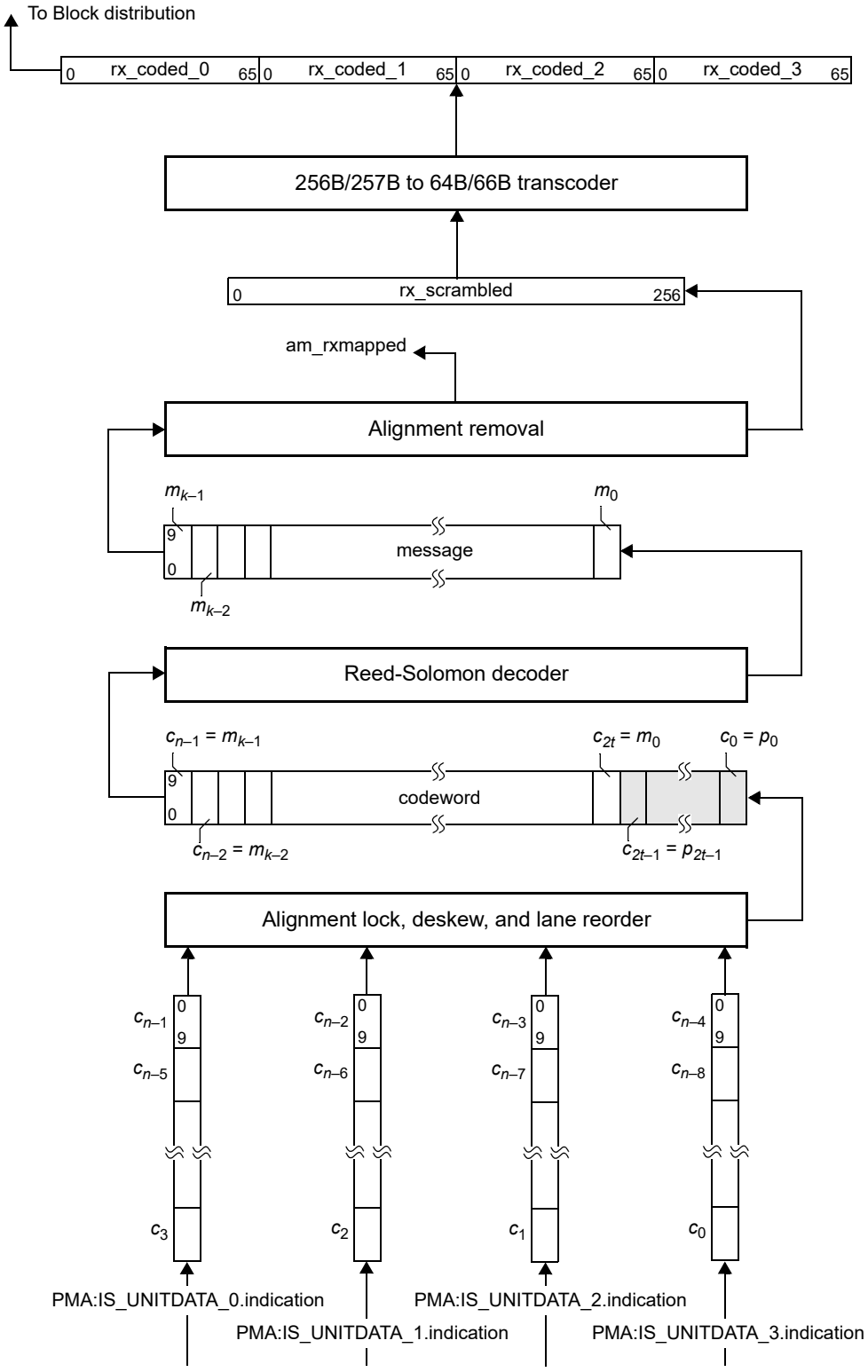

Figure 91–7—Receive bit ordering

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91.5.4.2 State variables

91.5.4.2.1 Variables

all_locked
: A Boolean variable that is set to true when amps_lock<*x*> is true for all *x* and is set to false when amps_lock<*x*> is false for any *x*.

amp_counter_done
: Boolean variable that indicates that amp_counter has reached its terminal count.

amp_match
: Boolean variable that holds the output of the function AMP_COMPARE.

amp_valid
: Boolean variable that is set to true if the received 64-bit block is a valid alignment marker payload. The alignment marker payload, mapped to an FEC lane according to the process described in 91.5.2.6, consists of 48 known bits and 16 variable bits (the BIP_3 or CD_3 field and its complement BIP_7 or CD_7, see 82.2.7). The bits of the candidate block that are in the positions of the known bits in the alignment marker payload are compared on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles in the alignment marker payload, the candidate block is considered a valid alignment marker payload. For the normal mode of operation, each FEC lane compares the candidate block to the alignment marker payload for PCS lane 0. For the optional EEE deep sleep capability, each FEC lane also compares the candidate block to the alignment marker payload for PCS lane 16 when rx_lpi_active is true.

amps_lock<*x*>
: Boolean variable that is set to true when the receiver has detected the location of the alignment marker payload sequence for a given lane on the PMA service interface, where *x* = 0:3.

current_pcsl
: A variable that holds the PCS lane number corresponding to the current alignment marker payload that is recognized on a given lane of the PMA service interface. It is compared to the variable first_pcsl to confirm that the location of the alignment marker payload sequence has been detected.

cw_bad
: A Boolean variable that is set to true if the Reed-Solomon decoder (see 91.5.3.3) fails to correct the current FEC codeword and is set to false otherwise.

deskew_done
: A Boolean variable that is set to true when fec_enable_deskew is set to true and the deskew process is completed. Otherwise, this variable is set to false.

fec_align_status
: A variable set by the FEC alignment process to reflect the status of FEC lane-to-lane alignment. Set to true when all lanes are synchronized and aligned and set to false when the deskew process is not complete.

fec_alignment_valid
: Boolean variable that is set to true if all FEC lanes are aligned. FEC lanes are considered to be aligned when amps_lock<*x*> is true for all *x*, each FEC lane is locked to a unique alignment marker payload sequence (see 91.5.2.6), and the FEC lanes are deskewed. Otherwise, this variable is set to false.

fec_enable_deskew
: A Boolean variable that enables and disables the deskew process. Received bits may be discarded whenever deskew is enabled. It is set to true when deskew is enabled and set to false when deskew is disabled.

fec_lane
: A variable that holds the FEC lane number (0 to 3) received on lane *x* of the PMA service interface when amps_lock<*x*>=true. The FEC lane number is determined by the alignment marker payloads in the 2nd, 3rd, or 4th positions of the sequence based on the mapping defined in 91.5.2.6. The 48 bits that are in the positions of the known bits in the received alignment marker payload are

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compared to the expected values for a given payload position and FEC lane on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles for any payload position on a given FEC lane, then the FEC lane number is assigned accordingly.

fec_lane_mapping<*x*>
: See 91.6.18.

fec_optional_states
: Boolean variable that is true if the optional states are implemented and false otherwise.

first_pcsl
: A variable that holds the PCS lane number that corresponds to the first alignment marker payload that is recognized on a given lane of the PMA service interface. It is compared to the PCS lane number corresponding to the second alignment marker payload that is tested.

reset
: Boolean variable that controls the resetting of the RS-FEC sublayer. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the RS-FEC sublayer into low-power mode.

restart_lock
: Boolean variable that is set by the FEC alignment process to reset the synchronization process on all FEC lanes. It is set to true after 3 consecutive uncorrected codewords are received (3_BAD state) and set to false upon entry into the LOSS_OF_ALIGNMENT state. It is also set to true when 5 Alignment Markers in a row fail to match (5_BAD state) if the optional states are supported in the FEC synchronization process.

rx_align_status
: Boolean variable that is set by the alignment lock and deskew function (see 91.5.2.2).

signal_ok
: Boolean variable that is set based on the most recently received value of PMA:IS_SIGNAL.indication(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done
: Boolean variable that is set to true when the SLIP requested by the synchronization state diagram has been completed indicating that the next candidate 64-bit block position can be tested.

test_amp
: Boolean variable that is set to true when a candidate block position is available for testing and false when the FIND_1ST state is entered.

test_cw
: Boolean variable that is set to true when a new FEC codeword is available for decoding and is set to false when the TEST_CW state is entered.

The following variables are only used for the optional EEE deep sleep capability. If this capability is not supported, the values of tx_lpi_active and rx_lpi_active are set to false.

1st_ram_counter_done
: Boolean variable that indicates that 1st_ram_counter has reached its terminal count.

1st_ramps_counter_done
: Boolean variable that indicates that 1st_ramps_counter has reached its terminal count.

fec_lpi_fw
: Boolean variable that controls the behavior of the Transmit LPI and Receive LPI state diagrams. This variable is set to true when the local PCS is configured to use the fast wake mechanism and set to false otherwise.

ram_counter_done
: Boolean variable that indicates that ram_counter has reached its terminal count.

ram_valid
: Boolean variable that is set to true when the 66-bit blocks concurrently received on at least 2 PCS lanes are valid Rapid Alignment Markers with identical values for rx_down_count and is set to false otherwise.

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ram_valid_prev
: Boolean variable that holds the value of ram_valid from the previous expected Rapid Alignment Marker position.

ramps_counter_done
: Boolean variable that indicates that ramps_counter has reached its terminal count.

ramps_valid
: Boolean variable that is set to true when the 64-bit block payloads concurrently received on at least 2 FEC lanes are valid Rapid Alignment Marker payloads with identical values for rx_down_count and is set to false otherwise.

ramps_valid_prev
: Boolean variable that holds that value of ramps_valid from the previous expected Rapid Alignment Marker payload position.

rx_down_count
: The value that results from the bit-wise exclusive-OR of the Count Down (CD_3) byte and the M_0 byte of the current Rapid Alignment Marker payload (see 82.2.9).

rx_lpi_active
: A Boolean variable that is set to true when the RS-FEC sublayer infers that the Low Power Idle is being received from the link partner and is set to false otherwise.

rx_quiet_timer_done
: A Boolean variable that indicates that rx_quiet_timer has reached its terminal count.

tx_down_count
: The value that results from the bit-wise exclusive-OR of the Count Down (CD_3) byte and the M_0 byte of the current Rapid Alignment Marker (see 82.2.9).

tx_lpi_active
: A Boolean variable that is set to true when the RS-FEC sublayer infers that the local PCS is transmitting Low Power Idle and is set to false otherwise.

tx_quiet_timer_done
: Boolean variable that indicates that tx_quiet_timer has reached its terminal count.

91.5.4.2.2 Functions

AMP_COMPARE
: This function compares the values of first_pcsl and current_pcsl to determine if a valid alignment marker payload sequence has been detected and returns the result of the comparison using the variable amp_match. When rx_lpi_active is false, if current_pcsl and first_pcsl are 0, amp_match is set to true. When rx_lpi_active is true, the comparison is performed as follows. If first_pcsl is 0 then amp_match is set to true if current_pcsl is 16. If first_pcsl is 16 then amp_match is set to true if current_pcsl is 0. Otherwise, amp_match is set to false.

SLIP
: Causes the next candidate block position to be tested. The precise method for determining the next candidate block position is not specified and is implementation dependent. However, an implementation shall ensure that all possible block positions are evaluated.

91.5.4.2.3 Counters

amp_bad_count
: Counts the number of consecutive alignment markers that don't match the expected values for a given FEC lane if the optional states are supported in the FEC synchronization process.

amp_counter
: When rx_lpi_active is false, this counter counts the 4096 FEC codewords that separate the ends of two consecutive normal alignment marker payload sequences. An FEC codeword is 1320 bits per FEC lane for 100GBASE-KR4 and 1360 bits per FEC lane for 100GBASE-KP4. When rx_lpi_active is true, then amp_counter is defined as follows. If first_pcsl corresponds to PCS

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lane 0, it counts the 256 bits to the end of the expected location of the Rapid Alignment Marker payload corresponding to PCS lane 16. If first_pcsl corresponds to PCS lane 16, this counter counts the 2 FEC codewords minus 256 bits to the end of the expected location of the next Rapid Alignment Marker payload corresponding to PCS lane 0.

cw_bad_count
: Counts the number of consecutive uncorrected FEC codewords. This counter is set to zero when an FEC codeword is received and cw_bad is false for that codeword.

The following counters are only used for the optional EEE deep sleep capability.

1st_ram_counter
: This counter counts 4 66-bit blocks from the end of one candidate RAM position to the end of the next candidate RAM position. The first instance of the counter counts from the end of the last normal alignment marker received.

1st_ramps_counter
: This counter counts one FEC codeword from the end of one candidate RAM payload to the end of the next RAM payload position. An FEC codeword is 1320 bits per FEC lane for 100GBASE-KR4 and 1360 bits per FEC lane for 100GBASE-KP4

ram_counter
: This counter counts 8 66-bit blocks from the end of the current RAM to the end of the next expected RAM position.

ramps_counter
: This counter counts 2 FEC codewords from the end of the current RAM payload to the end of the next expected RAM payload position.

rx_quiet_timer
: This timer limits the maximum time fec_align_status may be deasserted before the Transmit LPI state diagram concludes that the link has failed. The value of this timer is between 2 ms and 2.8 ms.

tx_quiet_timer
: This timer limits the maximum time rx_align_status may be deasserted before the Transmit LPI state diagram concludes that the link has failed. The value of this timer is between 1.8 ms and 2 ms.

91.5.4.3 State diagrams

The FEC shall implement four synchronization processes as shown in Figure 91–8. The synchronization process operates independently on each lane. The synchronization state diagram determines when the FEC has detected the location of the alignment marker payload sequence in the received bit stream for a given lane of the service interface.

The FEC shall implement the alignment process as shown in Figure 91–9.

When the optional EEE deep sleep capability is supported, the FEC shall also implement the Transmit LPI process as shown in Figure 91–10 and the Receive LPI process as shown in Figure 91–11. The Transmit LPI state diagram infers when Low Power Idle is being transmitted by the local PCS by checking for the presence of Rapid Alignment Markers. The Receive LPI state diagram infers when Low Power Idle is being received from the link partner using a similar mechanism. Monitoring the position and frequency of alignment markers is also critical to the operation of the alignment marker removal function (see 91.5.2.4 and 91.5.3.4).

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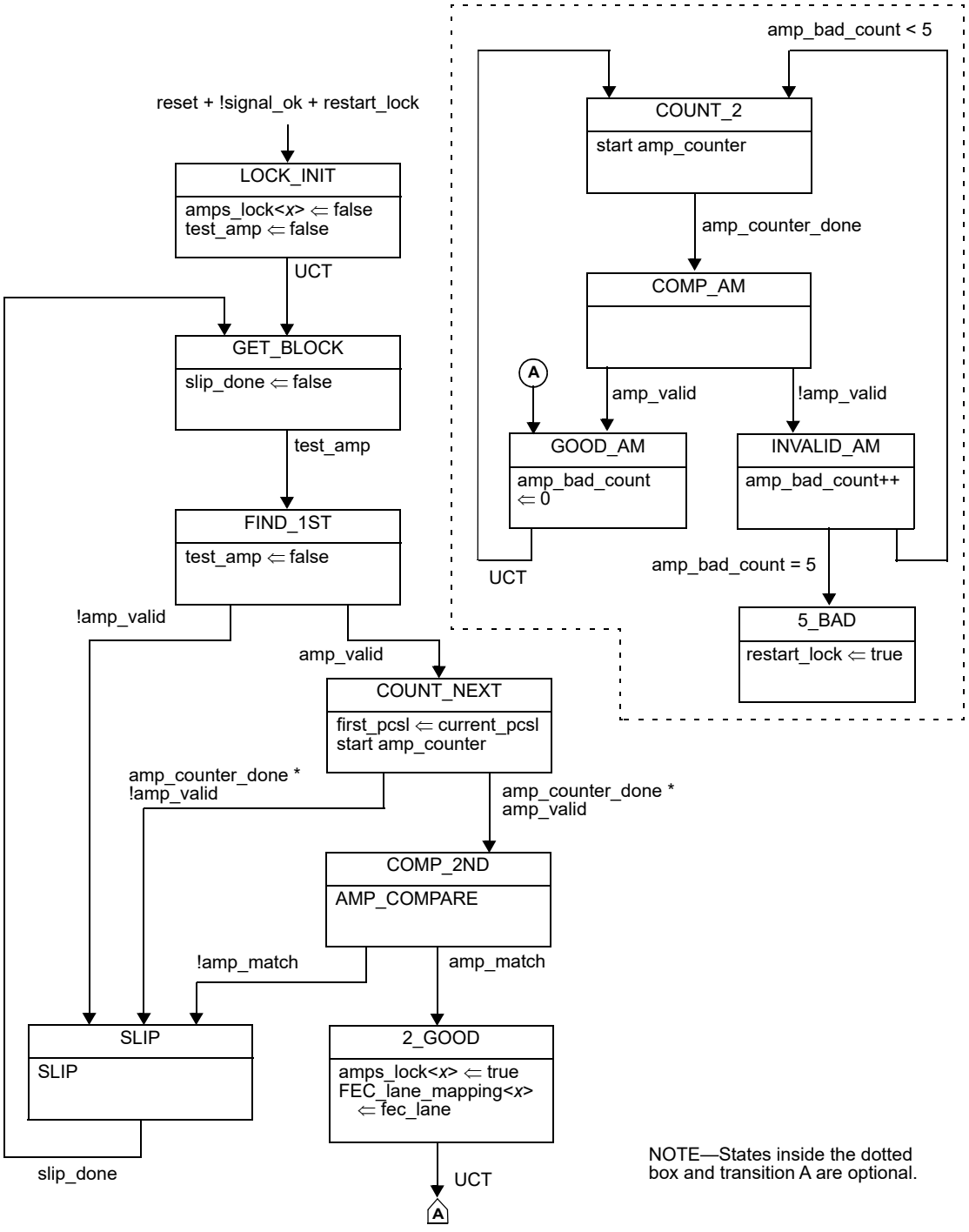

Figure 91–8—FEC synchronization state diagram

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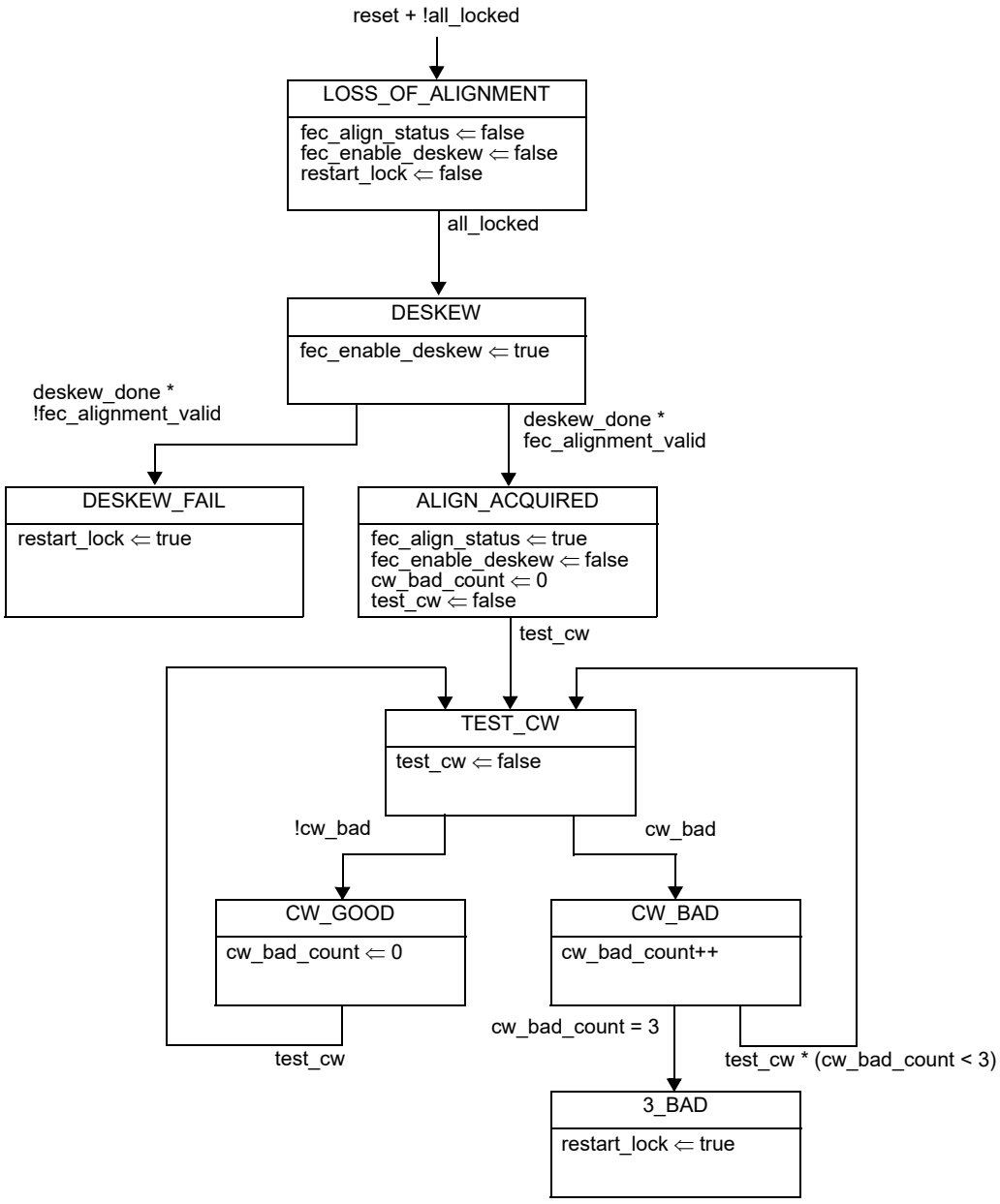

Figure 91–9—FEC alignment state diagram

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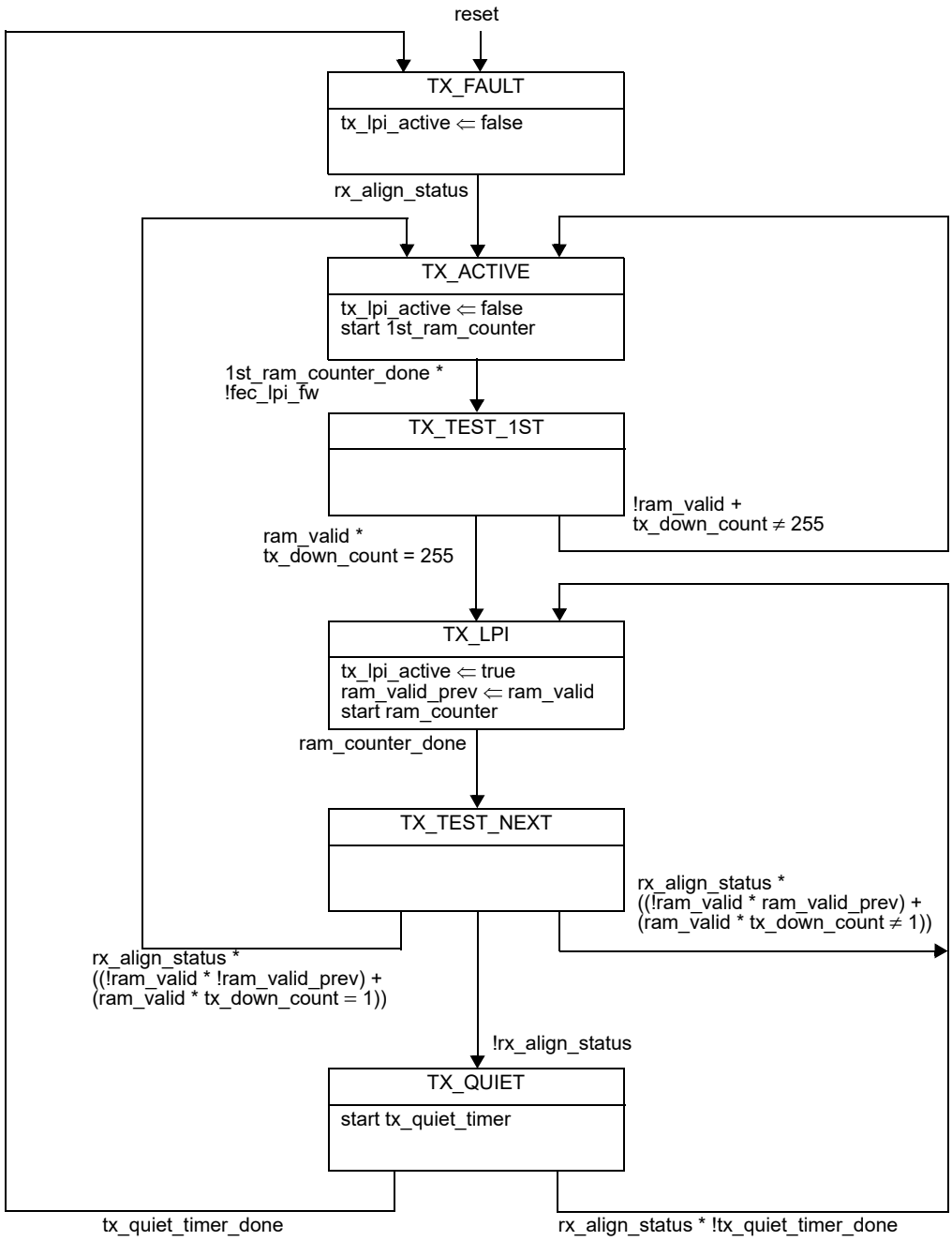

Figure 91–10—Transmit LPI state diagram

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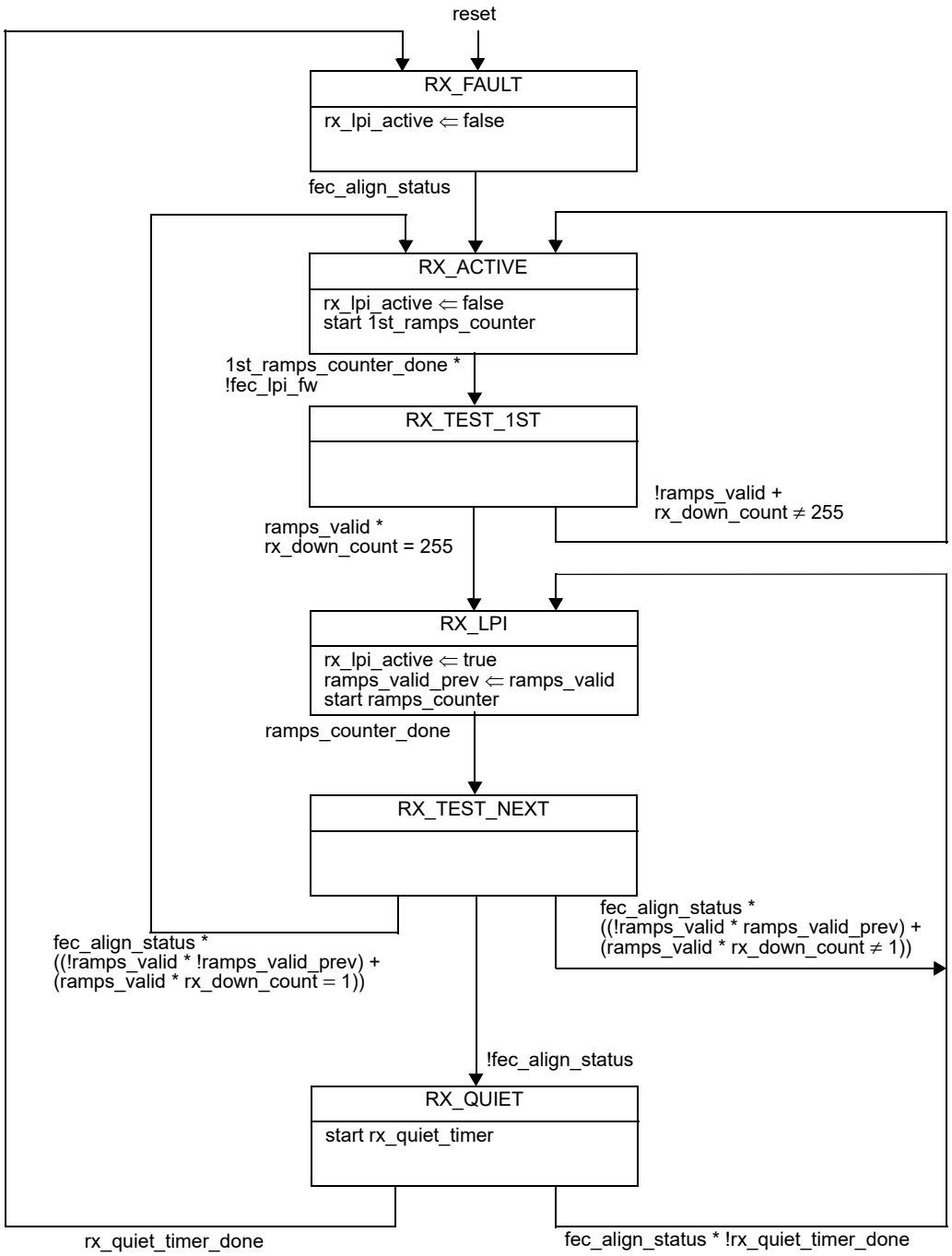

Figure 91–11—Receive LPI state diagram

91.6 RS-FEC MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the RS-FEC. If MDIO is implemented, it shall map MDIO control bits to RS-FEC control variables as shown in Table 91–2, and MDIO status bits to RS-FEC status variables as

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shown in Table 91–3, and if a separated PMA (see 45.2.1) is connected to the FEC service interface it shall map additional MDIO status bits to additional RS-FEC status variables as shown in Table 91–4.

Table 91–2—MDIO/RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass correction enable	RS-FEC control register	1.200.0	FEC_bypass_correction_enable
FEC bypass indication enable	RS-FEC control register	1.200.1	FEC_bypass_indication_enable
Four lane PMD	RS-FEC control register	1.200.3	four_lane_pmd
FEC degraded SER enable	RS-FEC control register	1.200.4	FEC_degraded_SER_enable
FEC degraded SER activate threshold	RS-FEC degraded SER activate threshold register	1.650, 1.651	FEC_degraded_SER_activate_threshold
FEC degraded SER deactivate threshold	RS-FEC degraded SER deactivate threshold register	1.652, 1.653	FEC_degraded_SER_deactivate_threshold
FEC degraded SER interval	RS-FEC degraded SER interval register	1.654, 1.655	FEC_degraded_SER_interval

Table 91–3—MDIO/RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass correction ability	RS-FEC status register	1.201.0	FEC_bypass_correction_ability
FEC bypass indication ability	RS-FEC status register	1.201.1	FEC_bypass_indication_ability
RS-FEC high SER	RS-FEC status register	1.201.2	hi_ser
FEC degraded SER ability	RS-FEC status register	1.201.3	FEC_degraded_SER_ability
FEC degraded SER	RS-FEC status register	1.201.4	FEC_degraded_SER
FEC optional states supported	RS-FEC status register	1.201.7	fec_optional_states
FEC AM lock *x*, *x*=0 to 3	RS-FEC status register	1.201.8:11	amps_lock<*x*>
RS-FEC align status	RS-FEC status register	1.201.14	fec_align_status
FEC corrected codewords	RS-FEC corrected codewords counter register	1.202, 1.203	FEC_corrected_cw_counter
FEC uncorrected codewords	RS-FEC uncorrected codewords counter register	1.204, 1.205	FEC_uncorrected_cw_counter
FEC lane *x* mapping	RS-FEC lane mapping register	1.206	FEC_lane_mapping<*x*>
FEC symbol errors, FEC lanes 0 to 3	RS-FEC symbol error counter register, FEC lanes 0 to 3	1.210 to 1.217	FEC_symbol_error_counter_*i*

The following subclauses define variables that are not otherwise defined, e.g., for use by state diagrams.

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Table 91–4—MDIO/RS-FEC status variable mapping for separated PMA

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
PCS align status	RS-FEC status register	1.201.15	align_status
BIP errors, PCS lanes 0 to 19	RS-FEC BIP error counter register, PCS lanes 0 to 19	1.230 to 1.249	BIP_error_counter_*i*
PCS lane *x* mapping	PCS lane *x* mapping register	1.250 to 1.269	lane_mapping<*x*>
Block lock *x*	RS-FEC PCS alignment status 1 and 2 registers	1.280 to 1.281	block_lock<*x*>
Lane *x* aligned	RS-FEC PCS alignment status 3 and 4 registers	1.282 to 1.283	am_lock<*x*>

91.6.1 FEC_bypass_correction_enable

When this variable is set to one, the Reed-Solomon decoder performs error detection without error correction (see 91.5.3.3). When this variable is set to zero, the decoder also performs error correction. The default value of the variable is zero. This variable is mapped to the bit defined in 45.2.1.116 (1.200.0).

91.6.2 FEC_bypass_indication_enable

This variable is set to one to bypass the error indication function (see 91.5.3.3) when this ability is supported. When this variable is set to zero, the decoder indicates errors to the PCS sublayer. This variable has no effect (the decoder does not bypass error indication) if FEC bypass correction enable (1.200.0) is set to one. The default value of this variable is zero. This variable is mapped to the bit defined in 45.2.1.116 (1.200.1).

91.6.3 four_lane_pmd

When this variable is set to one, the alignment marker mapping function substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16 (see 91.5.2.6). When this variable is set to zero, the alignment markers corresponding to PCS lanes 17, 18, and 19 are passed through unmodified. The default value of the variable is one which is the value required by the 100GBASE-CR4, 100GBASE-KR4, 100GBASE-KP4, and 100GBASE-SR4 PMDs. This variable is set to zero for the 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 PMDs. This variable is mapped to the bit defined in 45.2.1.116 (1.200.3).

91.6.4 FEC_degraded_SER_enable

This variable enables the FEC decoder to indicate the presence of a degraded SER when the ability is supported (see 91.5.3.3.1). When set to a one, this variable enables degraded SER detection. When set to a zero, degraded SER detection is disabled. Writes to this bit are ignored and reads return a zero if the FEC does not have the ability to signal the presence of a degraded SER. This variable is mapped to the bit defined in 45.2.1.116 (1.200.4).

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91.6.5 FEC_degraded_SER_activate_threshold

This variable controls the threshold used to set the FEC_degraded_SER bit as defined in 91.5.3.3.1. It is mapped to the registers defined in 45.2.1.146 (1.650, 1.651).

91.6.6 FEC_degraded_SER_deactivate_threshold

This variable controls the threshold used to clear the FEC_degraded_SER bit as defined in 91.5.3.3.1. It is mapped to the registers defined in 45.2.1.147 (1.652, 1.653).

91.6.7 FEC_degraded_SER_interval

This variable controls the interval used to set and clear the FEC_degraded_SER bit as defined in 91.5.3.3.1. It is mapped to the registers defined in 45.2.1.148 (1.654, 1.655).

91.6.8 FEC_bypass_correction_ability

The Reed-Solomon decoder may have the option to perform error detection without error correction (see 91.5.3.3) to reduce the delay contributed by the RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass error correction. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.117 (1.201.0).

91.6.9 FEC_bypass_indication_ability

The Reed-Solomon decoder may have the option to bypass the error indication function (see 91.5.3.3) to reduce the delay contributed by the RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass error indication. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.117 (1.201.1).

91.6.10 hi_ser

This variable is defined when the FEC_bypass_indication_ability variable is set to one. When FEC_bypass_indication_enable is set to one, this bit is set to one if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 91.5.3.3) and is set to zero otherwise. This variable is mapped to the bit defined in 45.2.1.117 (1.201.2).

91.6.11 FEC_degraded_SER_ability

The FEC decoder may have the option to indicate the presence of a degraded SER (see 91.5.3.3.1). This variable is set to one to indicate that the FEC decoder has the ability to indicate the presence of a degraded SER. This variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.117 (1.201.3).

91.6.12 FEC_degraded_SER

When FEC_degraded_SER_enable is asserted, this variable indicates the presence of a degraded SER as defined in 91.5.3.3.1. This variable is mapped to the bit defined in 45.2.1.117 (1.201.4).

91.6.13 FEC_optional_states

This variable is set to true when the optional states in the FEC synchronization state diagram are implemented. This variable is mapped to the bit defined in 45.2.1.117 (1.201.7).

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91.6.14 amps_lock<*x*>

These variables are assigned by the FEC alignment state diagram shown in Figure 91–9 (see 91.5.4.3). They are mapped to the bits defined in 45.2.1.117 (1.201.8 to 1.201.11 for FEC lanes 0 to 3, respectively).

91.6.15 fec_align_status

This variable assigned by the FEC alignment state diagram shown in Figure 91–9 (see 91.5.4.3). It is mapped to the bit defined in 45.2.1.117 (1.201.14).

91.6.16 FEC_corrected_cw_counter

A corrected FEC codeword is a codeword that contains errors and was corrected.

FEC_corrected_cw_counter is a 32-bit counter that counts once for each corrected FEC codeword processed when fec_align_status is true. This variable is mapped to the registers defined in 45.2.1.118 (1.202, 1.203).

91.6.17 FEC_uncorrected_cw_counter

An uncorrected FEC codeword is a codeword that contains errors (when the bypass correction feature is supported and enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled).

FEC_uncorrected_cw_counter is a 32-bit counter that counts once for each uncorrected FEC codeword processed when fec_align_status is true. This variable is mapped to the registers defined in 45.2.1.119 (1.204, 1.205).

91.6.18 FEC_lane_mapping<*x*>

When the RS-FEC receive function detects and locks to an alignment marker payload on PMA service interface lane *x*, the FEC lane number corresponding to the detected alignment marker payload is assigned to the variable FEC_lane_mapping<*x*>. These variables are mapped to the register defined in 45.2.1.120 (1.206).

91.6.19 FEC_symbol_error_counter_*i*

FEC_symbol_error_counter_*i*, where *i*=0 to 3, is a 32-bit counter that counts once for each 10-bit symbol corrected on FEC lane *i* when fec_align_status is true. These variables are mapped to the registers defined in 45.2.1.121 and 45.2.1.122 (1.210 to 1.217).

91.6.20 align_status

This variable is assigned the value of rx_align_status as defined by the PCS deskew state diagram shown in Figure 82–14 (see 91.5.2.2). It is mapped to the bit defined in 45.2.1.117 (1.201.15).

91.6.21 BIP_error_counter_*i*

BIP_error_counter_*i*, where *i*=0 to 19, is a 16-bit counter that holds the BIP error count for PCS lane *i* as calculated by the RS-FEC transmit function (see 91.5.2.4). These variables are mapped to the registers defined in 45.2.1.123 and 45.2.1.124 (1.230 to 1.249).

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91.6.22 lane_mapping<*x*>

When the RS-FEC transmit function detects and locks to an alignment marker on FEC service interface lane *x*, the PCS lane number corresponding to the detected alignment marker is assigned to the variable lane_mapping<*x*>. These variables are mapped to the registers defined in 45.2.1.125 and 45.2.1.126 (1.250 to 1.269).

91.6.23 block_lock<*x*>

These variables are assigned by the block lock state diagram shown in Figure 82–12 (see 91.5.2.1). They are mapped to the registers defined in 45.2.1.127 and 45.2.1.128 (1.280 to 1.281).

91.6.24 am_lock<*x*>

These variables are assigned by the alignment marker lock state diagram shown in Figure 82–13 (see 91.5.2.2). They are mapped to the registers defined in 45.2.1.129 and 45.2.1.130 (1.282 to 1.283).

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91.7 Protocol implementation conformance statement (PICS) proforma for Clause 91, Reed-Solomon forward error correction (RS-FEC) sublayer for 100GBASE-R PHYs[160]

91.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 91, Reed-Solomon forward error correction (RS-FEC) sublayer for 100GBASE-R PHYs, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

91.7.2 Identification

91.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

91.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 91, Reed-Solomon forward error correction (RS-FEC) sublayer for 100GBASE-R PHYs
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[160] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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91.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*KR4	100GBASE-CR4 or 100GBASE-KR4		Used to form complete 100GBASE-CR4 or 100GBASE-KR4 PHY	O	Yes [ ] No [ ]
*KP4	100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1		Used to form complete 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PHY	O	Yes [ ] No [ ]
*FDDP	100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1	91.5.3.3.1	Used to form complete 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PHY	O	Yes [ ] No [ ]
*FDD	Support for optional FEC degraded SER detection	91.5.3.3.1		FDDP:O	Yes [ ] No [ ] N/A [ ]
*SR4	100GBASE-SR4		Used to form complete 100GBASE-SR4 PHY	O	Yes [ ] No [ ]
DC	Delay constraints	91.4	Conforms to delay constraints specified in 91.4	M	Yes [ ]
*MD	MDIO capability	91.6	Registers and interface supported	O	Yes [ ] No [ ]
*BEC	Bypass error correction	91.5.3.3	Capability is supported	O	Yes [ ] No [ ]
*BEI	Bypass error indication	91.5.3.3	Capability is supported	O	Yes [ ] No [ ]
*EEE	EEE capability	91.5.4.3	Capability is supported	O	Yes [ ] No [ ]

91.7.4 PICS proforma tables for Reed-Solomon forward error correction (RS-FEC) sublayer for 100GBASE-R PHYs

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91.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Skew tolerance	91.5.2.2	Maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps	M	Yes [ ]
TF2	Lane reorder	91.5.2.3	Order the PCS lanes according to the PCS lane number	M	Yes [ ]
TF3	64B/66B to 256B/257B transcoder	91.5.2.5	tx_xcoded<256:0> constructed per 91.5.2.5	M	Yes [ ]
TF4	257-bit block transmission order	91.5.2.5	First bit transmitted is bit 0	M	Yes [ ]
TF5	Alignment maker mapping	91.5.2.6	Map to am_txmapped<1284:0> per 91.5.2.6	M	Yes [ ]
TF6	Pad value	91.5.2.6	Binary values 00101 and 11010 (the leftmost bit is assigned to the highest bit index) in an alternating pattern	M	Yes [ ]
TF7	Alignment marker insertion	91.5.2.6	First 1285 message bits to be transmitted from every 4096th codeword	M	Yes [ ]
TF8	Alignment marker insertion when tx_lpi_active is true	91.5.2.6	First 1285 message bits to be transmitted from every other codeword	EEE:M	Yes [ ] N/A [ ]
TF9	Alignment marker insertion point	91.5.2.6	First 257-bit block inserted after am_txmapped corresponds to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective lane	M	Yes [ ]
TF10	Reed-Solomon encoder for 100GBASE-CR4 or 100GBASE-KR4 or 100GBASE-SR4	91.5.2.7	RS(528,514)	KR4:M or SR4:M	Yes [ ] N/A [ ]
TF11	Reed-Solomon encoder for 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1	91.5.2.7	RS(544,514)	KP4:M	Yes [ ] N/A [ ]
TF12	Symbol distribution	91.5.2.8	Distributed to 4 FEC lanes, one 10-bit symbol at a time in a round robin distribution from the lowest to the highest numbered FEC lane	M	Yes [ ]

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91.7.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	91.5.3.1	Maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	Lane reorder	91.5.3.2	Order the FEC lanes according to the FEC lane number	M	Yes [ ]
RF3	Reed-Solomon decoder for 100GBASE-CR4 or 100GBASE-KR4	91.5.3.3	Corrects any combination of up to t=7 symbol errors in a codeword unless error correction bypassed	KR4:M	Yes [ ] N/A [ ]
RF4	Reed-Solomon decoder for 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1	91.5.3.3	Corrects any combination of up to t=15 symbol errors in a codeword unless error correction bypassed	KP4:M	Yes [ ] N/A [ ]
RF5	Reed-Solomon decoder for 100GBASE-SR4	91.5.3.3	Corrects any combination of up to t=7 symbol errors in a codeword	SR4:M	Yes [ ] N/A [ ]
RF6	Error correction bypass for 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-SR4, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1	91.5.3.3	Error correction is not bypassed	SR4:M or FDDP:M	Yes [ ] N/A [ ]
RF7	Reed-Solomon decoder	91.5.3.3	Capable of indicating when a codeword was not corrected.	M	Yes [ ]
RF8	Error indication function	91.5.3.3	Corrupts 66-bit block synchronization headers for uncorrected errored codewords (or errored codewords when correction is bypassed)	M	Yes [ ]
RF9	Error indication when error correction is bypassed	91.5.3.3	Error indication is not bypassed	BEI:M	Yes [ ] N/A [ ]
RF10	Error monitoring while error indication is bypassed	91.5.3.3	When the number of symbols errors in a block of 8192 codewords exceeds K, corrupt 66-bit block synchronization headers	BEI:M	Yes [ ] N/A [ ]
RF11	Symbol error threshold for 100GBASE-CR4, 100GBASE-KR4, and 100GBASE-SR4	91.5.3.3	K=417	BEI* KR4:M or BEI* SR4:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RF12	Symbol error threshold for 100GBASE-KP4, 100GBASE-CR2, 100GBASE-KR2, 100GBASE-SR2, 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1	91.5.3.3	*K*=6380	BEI* KP4:M	Yes [ ] N/A [ ]
RF13	Error monitoring during LPI	91.5.3.3	Error monitor disabled when rx_lpi_active=true	BEI* EEE:M	Yes [ ] N/A [ ]
RF14	Start of error monitoring window	91.5.3.3	Begins on the codeword boundary following the transition of rx_lpi_active from true to false	BEI* EEE:M	Yes [ ] N/A [ ]
RF15	Alignment marker removal	91.5.3.4	am_rxmapped removed prior to transcoding	M	Yes [ ]
RF16	256B/257B to 64B/66B transcoder	91.5.3.5	rx_coded_*j*<65:0>, *j*=0 to 3 constructed per 91.5.3.5	M	Yes [ ]
RF17	Block distribution	91.5.3.6	One 66-bit block at a time in a round robin fashion from the lowest to the highest numbered PCS lane	M	Yes [ ]
RF18	Alignment marker mapping	91.5.3.7	Map to am_rx_*x*, *x*=0 to 19 per 91.5.3.7	M	Yes [ ]
RF19	Alignment marker insertion point	91.5.3.7	Alignment markers immediately followed by the 66-bit blocks derived from the 257-blocks immediately following am_rxmapped	M	Yes [ ]
RF20	FEC decoder detects FEC degraded SER at a programmable threshold	91.5.3.3.1		FDD:M	Yes [ ] N/A [ ]

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91.7.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	SLIP function	91.5.4.2.2	Ensure that all possible block positions are evaluated	M	Yes [ ]
SD2	Synchronization process	91.5.4.3	One instance per FEC lane per Figure 91–8	M	Yes [ ]
SD3	Alignment process	91.5.4.3	Per Figure 91–9	M	Yes [ ]
SD4	Transmit LPI process	91.5.4.3	Per Figure 91–10	EEE:M	Yes [ ] N/A [ ]
SD5	Receive LPI process	91.5.4.3	Per Figure 91–11	EEE:M	Yes [ ] N/A [ ]
SD6	FEC synchronization enhancement	91.5.4.3	Check AMs after synchronization is achieved per Figure 91–8	O	Yes [ ] No [ ]

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92. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR4

92.1 Overview

This clause specifies the 100GBASE-CR4 PMD and baseband medium. Annex 92A, an associated annex, provides information on parameters with test points that may not be testable in an implemented system.

When forming a complete Physical Layer, a PMD shall be connected as illustrated in Figure 92–1, to the appropriate PMA as shown in Table 92–1, to the medium through the MDI and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 92–1—Physical Layer clauses associated with the 100GBASE-CR4 PMD

Associated clause	100GBASE-CR4
81—RS	Required
81—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R[b]	Required
83A—CAUI-10	Optional
83D—CAUI-4	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation behaves functionally as though the RS and CGMII were present.
[b]There are limitations on the number of PMA lanes that may be used between sublayers, see 83.

When forming a complete 100GBASE-CR4 Physical Layer, the following guidelines apply.

Differential signals received at the MDI from a transmitter that meets the requirements of 92.8.3 and have passed through the cable assembly specified in 92.10 are received with a BER less than 10^{-5}.

For a complete Physical Layer, this specification is considered to be satisfied by a frame loss ratio (see 1.4.344) less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap.

A 100GBASE-CR4 PHY with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization.

Figure 92–1 shows the relationship of the 100GBASE-CR4 PMD sublayer and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.

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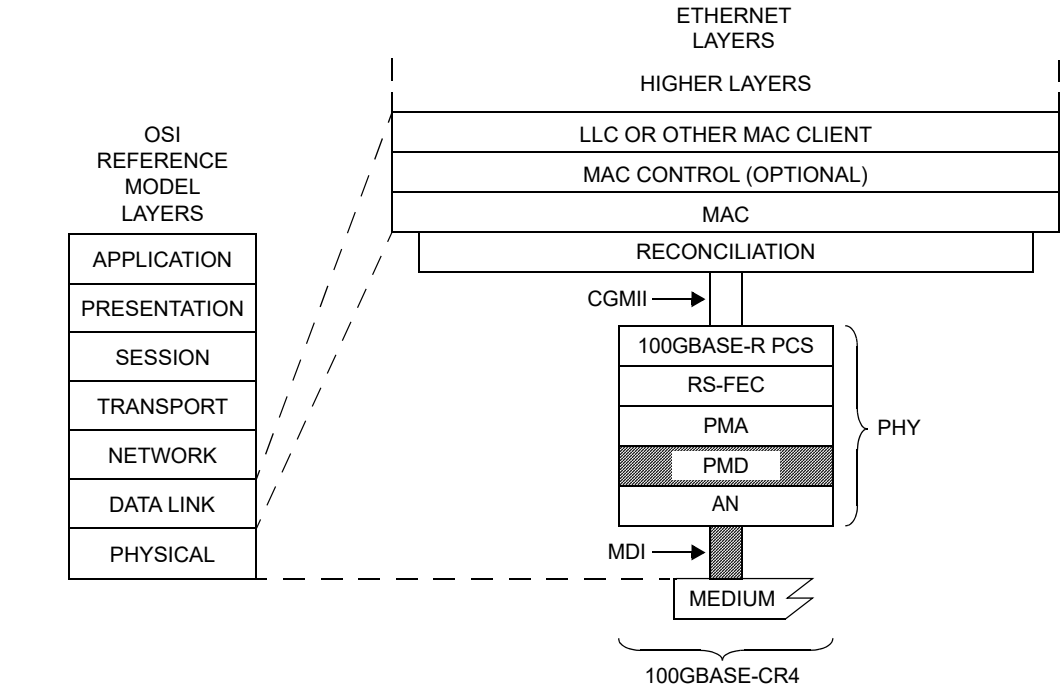

AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 92–1—100GBASE-CR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

92.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-CR4 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data. The PMD translates the encoded data to and from signals suitable for the medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 100GBASE-CR4 PMD has four parallel bit streams, hence i = 0 to 3. The PMA (or the PMD) continuously sends four parallel bit streams to the PMD (or the PMA), one per lane, each at a nominal signaling rate of 25.78125 GBd.

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The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable Global_PMD_signal_detect as defined in 92.7.4. When Global_PMD_signal_detect is one, SIGNAL_OK shall be assigned the value OK. When Global_PMD_signal_detect is zero, SIGNAL_OK shall be assigned the value FAIL. When SIGNAL_OK is FAIL, the PMD:IS_UNITDATA_i.indication parameters are undefined.

If the optional EEE deep sleep capability is supported, then the PMD service interface includes two additional primitives as follows:

PMD:IS_TX_MODE.request
PMD:IS_RX_MODE.request

92.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 82.6.)

The 100GBASE-CR4 PHY may be extended using CAUI-n as a physical instantiation of the inter-sublayer service interface between devices. If CAUI-n is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementer. As examples, the implementer may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

92.4 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the 100GBASE-CR4 PMD and AN shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns). It is assumed that the one way delay through the medium is no more than 6000 bit times (60 ns).

A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

92.5 Skew constraints

The Skew (relative delay) between the lanes is kept within limits so that the information on the lanes can be reassembled by the RS-FEC sublayer. Skew and Skew Variation are defined in 80.5 and specified at the points SP1 to SP6 shown in Figure 80–9.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5.

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92.6 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control bits to PMD control variables as shown in Table 92–2, and MDIO status bits to PMD status variables as shown in Table 92–3.

Table 92–2—100GBASE-CR4 MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 3 to PMD transmit disable 0	PMD transmit disable	1.9.4 to 1.9.1	PMD_transmit_disable_3 to PMD_transmit_disable_0
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable
Polynomial identifier 3	PMD training pattern 3	1.1453.12:11	identifier_3
Seed 3	PMD training pattern 3	1.1453.10:0	seed_3
Polynomial identifier 2	PMD training pattern 2	1.1452.12:11	identifier_2
Seed 2	PMD training pattern 2	1.1452.10:0	seed_2
Polynomial identifier 1	PMD training pattern 1	1.1451.12:11	identifier_1
Seed 1	PMD training pattern 1	1.1451.10:0	seed_1
Polynomial identifier 0	PMD training pattern 0	1.1450.12:11	identifier_0
Seed 0	PMD training pattern 0	1.1450.10:0	seed_0

Table 92–3—100GBASE-CR4 MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 0	PMD receive signal detect	1.10.4 to 1.10.1	PMD_signal_detect_3 to PMD_signal_detect_0
100GBASE-CR4 deep sleep	EEE capability	1.16.11	—
Receiver status 3	BASE-R PMD status	1.151.12	rx_trained_3
Frame lock 3	BASE-R PMD status	1.151.13	frame_lock_3

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Table 92–3—100GBASE-CR4 MDIO/PMD status variable mapping *(continued)*

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Startup protocol status 3	BASE-R PMD status	1.151.14	training_3
Training failure 3	BASE-R PMD status	1.151.15	training_failure_3
Receiver status 2	BASE-R PMD status	1.151.8	rx_trained_2
Frame lock 2	BASE-R PMD status	1.151.9	frame_lock_2
Startup protocol status 2	BASE-R PMD status	1.151.10	training_2
Training failure 2	BASE-R PMD status	1.151.11	training_failure_2
Receiver status 1	BASE-R PMD status	1.151.4	rx_trained_1
Frame lock 1	BASE-R PMD status	1.151.5	frame_lock_1
Startup protocol status 1	BASE-R PMD status	1.151.6	training_1
Training failure 1	BASE-R PMD status	1.151.7	training_failure_1
Receiver status 0	BASE-R PMD status	1.151.0	rx_trained_0
Frame lock 0	BASE-R PMD status	1.151.1	frame_lock_0
Startup protocol status 0	BASE-R PMD status	1.151.2	training_0
Training failure 0	BASE-R PMD status	1.151.3	training_failure_0

92.7 PMD functional specifications

92.7.1 Link block diagram

A 100GBASE-CR4 link in one direction is illustrated in Figure 92–2. For purposes of system conformance, the PMD sublayer is standardized at the test points described in this subclause. The electrical transmit signal is defined at TP2. Unless specified otherwise, all transmitter measurements and tests defined in 92.8.3 are made at TP2 utilizing the test fixture specified in 92.11.1. Unless specified otherwise, all receiver measurements and tests defined in 92.8.4 are performed at TP3 utilizing the test fixture specified in 92.11.1. A mated connector pair has been included in both the transmitter and receiver specifications defined in 92.8.3 and 92.8.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 92.8.3.6.

The 100GBASE-CR4 channel is defined between the transmitter (TP0) and receiver (TP5) blocks to include the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss, as illustrated in Figure 92–2. Annex 92A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system. All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92–2. The cable assembly test fixture of Figure 92–17, or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4. Two mated connector pairs and the cable assembly test fixture have been included in the cable assembly specifications defined in 92.10. Transmitter and receiver differential controlled impedance printed circuit board insertion losses defined between TP0–TP1 and TP4–TP5, respectively, are provided informatively in Annex 92A.

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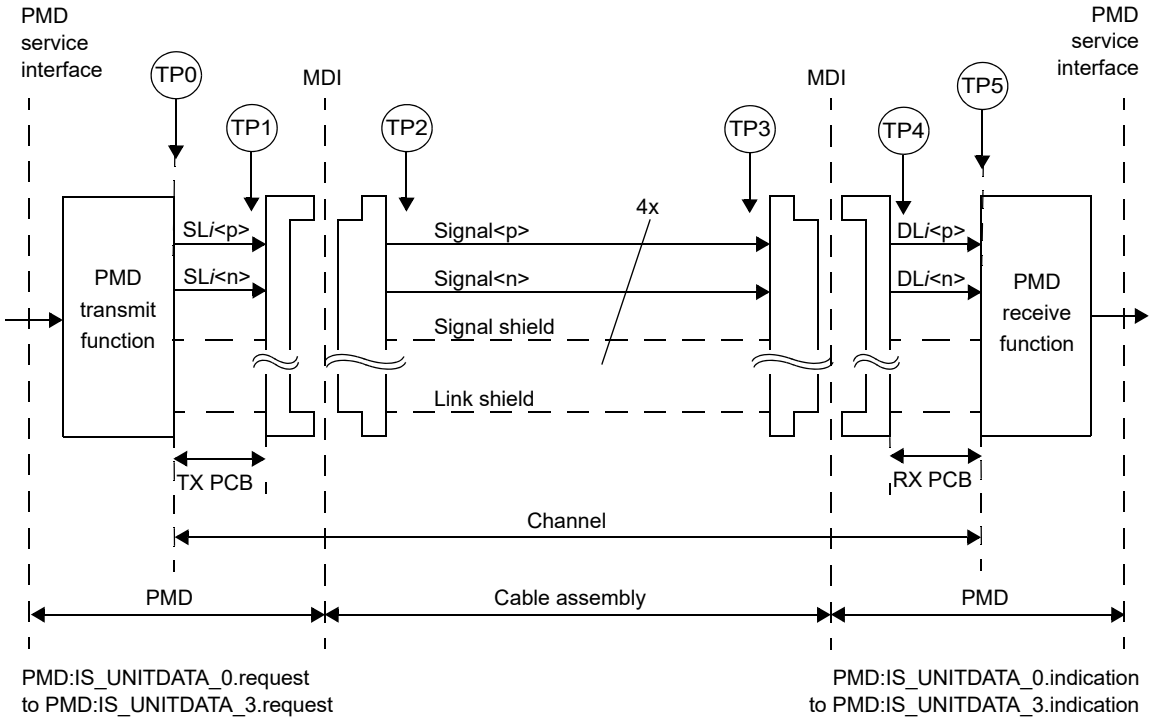

Figure 92–2—100GBASE-CR4 link (one direction is illustrated)

Note that the source lanes (SL), signals SL*i*<p>, and SL*i*<n> are the positive and negative sides of the transmitters differential signal pairs and the destination lanes (DL) signals, DL*i*<p>, and DL*i*<n> are the positive and negative sides of the receivers differential signal pairs for lane *i* (*i* = 0, 1, 2, 3).

Table 92–4 describes the defined test points illustrated in Figure 92–2.

Table 92–4—100GBASE-CR4 test points

Test points	Description
TP0 to TP5	The 100GBASE-CR4 channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92–2. The cable assembly test fixture of Figure 92–17 or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 92.8.3 and 92.8.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 92.8.3.6.
TP2	Unless specified otherwise, all transmitter measurements defined in Table 92–6 are made at TP2 utilizing the test fixture specified in 92.11.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 92.8.4 are made at TP3 utilizing the test fixture specified in 92.11.1.

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92.7.2 PMD Transmit function

The PMD transmit function shall convert the four bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_*i*.request (*i*=0 to 3) into four separate electrical signals. The four electrical signals shall then be delivered to the MDI, all according to the transmit electrical specifications in 92.8.3. A positive differential output voltage (SL*i*<p> minus SL*i*<n>) shall correspond to tx_bit = one.

If the optional EEE deep sleep capability is supported, the following requirements apply. When tx_mode is set to ALERT, the PMD transmit function shall transmit a periodic sequence, where each period of the sequence consists of 8 ones followed by 8 zeros, on each lane, with the transmit equalizer coefficients set to the preset values (see 72.6.10.2.3.1). This sequence is transmitted regardless of the value of tx_bit presented by the PMD:IS_UNITDATA_*i*.request primitive. When tx_mode is not set to ALERT, the transmit equalizer coefficients are set to the values determined via the startup protocol (see 92.7.12).

92.7.3 PMD Receive function

The PMD receive function shall convert the four electrical signals from the MDI into four bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_*i*.indication (*i*=0 to 3). A positive differential input voltage (DL*i*<p> minus DL*i*<n>) shall correspond to rx_bit = one.

92.7.4 Global PMD signal detect function

The variable Global_PMD_signal_detect is the logical AND of the values of PMD_signal_detect_*i* for *i*=0 to 3.

When the MDIO is implemented, this function maps the variable Global_PMD_signal_detect to the register and bit defined in 92.6.

92.7.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal detect function is used by the 100GBASE-CR4 PMD to indicate the successful completion of the startup protocol by the PMD control function (see 92.7.12). PMD_signal_detect_*i* (where *i* represents the lane number in the range 0 to 3) is set to zero when the value of the variable signal_detect is set to false by the Training state diagram for lane *i* (see Figure 72–5). PMD_signal_detect_*i* is set to one when the value of signal_detect for lane *i* is set to true.

If training is disabled by the management variable mr_training_enable (see 92.6), PMD_signal_detect_*i* shall be set to one for *i*=0 to 3.

If the optional EEE deep sleep capability is supported, the following requirements apply. The value of PMD_signal_detect_*i* (for *i*=0 to 3) is set to zero when rx_mode is first set to QUIET. While rx_mode is set to QUIET, PMD_signal_detect_*i* shall be set to one within 500 ns of the application of the ALERT pattern defined in 92.7.2, with peak-to-peak differential voltage of 720 mV measured at TP2, to the differential pair at the input of the cable assembly that connects the transmitter to the receiver of lane *i*. While rx_mode is set to QUIET, PMD_signal_detect_*i* shall not be set to one when the voltage input to the differential pair of the cable assembly that connects the transmitter to the receiver of lane *i* is less than or equal to 70 mV peak-to-peak differential.

When the MDIO is implemented, this function maps the variables to registers and bits as defined in 92.6.

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92.7.6 Global PMD transmit disable function

The Global PMD transmit disable function is mandatory if EEE deep sleep capability is supported and is otherwise optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When Global_PMD_transmit_disable variable is set to one, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage in Table 92–6.
b) If a PMD fault (92.7.9) is detected, then the PMD may set Global_PMD_transmit_disable to one.
c) Loopback, as defined in 92.7.8, shall not be affected by Global_PMD_transmit_disable.
d) The following additional requirements apply when the optional EEE deep sleep capability is supported. The Global PMD transmit disable function shall turn off all of the transmitters as specified in 92.8.3.1 when tx_mode transitions to QUIET from any other value. The Global PMD transmit disable function shall turn on all of the transmitters as specified in 92.8.3.1 when tx_mode transitions from QUIET to any other value.

92.7.7 PMD lane-by-lane transmit disable function

The PMD lane-by-lane transmit disable function is optional and allows the electrical transmitter in each lane to be selectively disabled. When this function is supported, it shall meet the following requirements:

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0 to 3) is set to one, this function shall turn off the transmitter associated with that variable such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 92–6.
b) If a PMD fault (92.7.9) is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the electrical transmitter in each lane.
c) Loopback, as defined in 92.7.8, shall not be affected by PMD_transmit_disable_*i*.

92.7.8 Loopback mode

Local loopback mode is provided by the adjacent PMA (see 83.5.8) as a test function. When loopback mode is enabled, transmission requests passed to each transmitter are sent directly to the corresponding receiver, overriding any signal detected by each receiver on its attached link. Note that loopback mode does not affect the state of the transmitter, which continues to send data (unless disabled).

Control of the loopback function is specified in 83.5.8.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

92.7.9 PMD fault function

If the MDIO is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3. PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault.

92.7.10 PMD transmit fault function

The PMD transmit fault function is optional. The faults detected by this function are implementation specific, but the assertion of Global_PMD_transmit_disable is not considered a transmit fault.

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If PMD_transmit_fault is set to one, then Global_PMD_transmit_disable should also be set to one.

If the MDIO interface is implemented, then this function shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

92.7.11 PMD receive fault function

The PMD receive fault function is optional. The faults detected by this function are implementation specific. A fault is indicated by setting the variable PMD_receive_fault to one.

If the MDIO interface is implemented, then PMD_receive_fault shall be mapped to the Receive fault bit as specified in 45.2.1.7.5.

92.7.12 PMD control function

Each lane of the 100GBASE-CR4 PMD shall use the same control function as 10GBASE-KR, as defined in 72.6.10, with the following differences:

a) The training frame structure used by the 100GBASE-CR4 PMD control function shall be as defined in 72.6.10 with the exception that 25.78125 GBd symbols replace 10.3125 GBd symbols and 100GBASE-CR4 UI replace 10GBASE-KR UI.
b) In addition to the coefficient update process specified in 72.6.10.2.5, the period from receiving a new request to responding to that request shall be less than 2 ms, except during the first 50 ms following the beginning of the startup protocol. The beginning of the startup protocol is defined to be entry into the AN_GOOD_CHECK state in Figure 73–10. The start of the period is the frame marker of the training frame with the new request and the end of the period is the frame marker of the training frame with the corresponding response. A new request occurs when the coefficient update field is different from the coefficient field in the preceding frame. The response occurs when the coefficient status report field is updated to indicate that the corresponding action is complete.
c) In addition, the training pattern defined in 72.6.10.2.6 is replaced with a set of training patterns designed to minimize the correlation between physical lanes. The training pattern for each lane shall consist of 4094 bits from the output of a pseudo-random bit sequence (PRBS) generator followed by two zeros. The PRBS generator for each lane shall implement each of the four generator polynomials (polynomial_*n* where *n* goes from 0 to 3) given in Table 92–5, selectable by identifier_*i* (where *i* is the lane number). By default identifier_*i* is set to lane number *i* (i.e., identifier_0 = 0; identifier_1 = 1, etc.). At the start of the training pattern, the state of the generator shall be set to the value in seed_*i* (where *i* is the lane number), with the default values given in Table 92–5. Note that a seed value of 0x000 is invalid. An example implementation of the PRBS generator for *n* = 0 with default settings is given in Figure 92–3. The first 32 bits of the training pattern for each polynomial is also provided in Table 92–5.

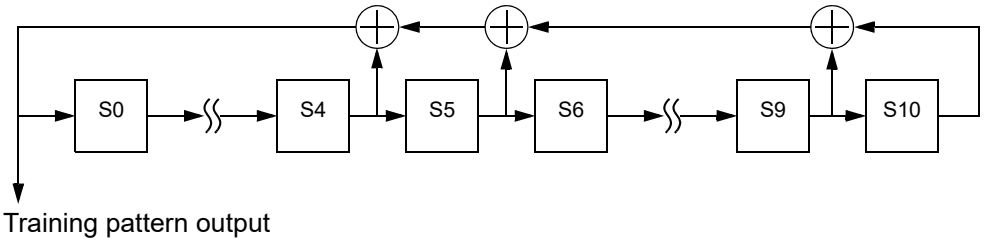

Figure 92–3—PRBS generator for polynomial_0

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Table 92–5—PRBS parameters for each physical lane

n	Polynomial_*n*, *G*(*x*)	Default seed bits, S0 is the left most bit	Initial output[a]
0	$1 + x^5 + x^6 + x^{10} + x^{11}$	10101111110	FBF1CB3E
1	$1 + x^5 + x^6 + x^9 + x^{11}$	11001000101	FBB1E665
2	$1 + x^4 + x^6 + x^8 + x^{11}$	11100101101	F3FDAE46
3	$1 + x^4 + x^6 + x^7 + x^{11}$	11110110110	F2FFA46B

[a]The first 32 bits of the training pattern are presented in a hexadecimal representation where the hex symbols are transmitted from left to right and the most significant bit of each hex symbol is transmitted first

The variables rx_trained_*i*, frame_lock_*i*, training_*i,* and training_failure_*i* (where *i* goes from 0 to 3) report status for each lane and are equivalent to rx_trained, frame_lock, training, and training_failure as defined in 72.6.10.3.1.

If the MDIO interface is implemented, then this function shall map the variables polynomial_*i*, seed_*i*, rx_trained_*i*, frame_lock_*i*, training_*i,* and training_failure_*i* to the registers and bits defined in 92.6.

92.8 100GBASE-CR4 electrical characteristics

92.8.1 Signal levels

The 100GBASE-CR4 MDI is a low-swing AC-coupled differential interface. AC-coupling within the plug connectors, as defined in 92.12.1, allows for interoperability between components operating from different supply voltages.

92.8.2 Signal paths

The 100GBASE-CR4 MDI signal paths are point-to-point connections. Each path corresponds to a 100GBASE-CR4 MDI lane and comprises two complementary signals, which form a balanced differential pair. For 100GBASE-CR4, there are four differential paths in each direction for a total of eight pairs, or sixteen connections. The signal paths are intended to operate on twinaxial cable assemblies ranging from 0.5 m to 5 m in length, as described in 92.10.

92.8.3 Transmitter characteristics

Transmitter characteristics are summarized in Table 92–6. Unless specified otherwise, all transmitter measurements defined in Table 92–6 are made at TP2 utilizing the test fixtures specified in 92.11.1. A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified. The transmitter specifications at TP0 are provided informatively in Annex 92A.

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Table 92–6—Transmitter characteristics at TP2 summary

Parameter	Subclause reference	Value	Units
Differential peak-to-peak output voltage (max.) with Tx disabled	92.8.3.1	35	mV
DC common-mode voltage (max.)	92.8.3.1	1.9	V
AC common-mode output voltage, v_{cmi} (max., RMS)	92.8.3.1	30	mV
Differential peak-to-peak voltage, v_{di} (max.)	92.8.3.1	1200	mV
Differential output return loss (min.)	92.8.3.2	See Equation (92–1)	dB
Common-mode to differential mode output return loss (min.)	92.8.3.3	See Equation (92–2)	dB
Common-mode to common-mode output return loss (min.)	92.8.3.4	See Equation (92–3)	dB
Transmitter steady-state voltage, v_f (min.) Transmitter steady-state voltage, v_f (max.)	92.8.3.5.2	0.34 0.6	V
Linear fit pulse peak (min.)	92.8.3.5.2	0.45 × v_f	V
Transmitted waveform abs coefficient step size (min.) abs coefficient step size (max.) minimum precursor full-scale ratio minimum post cursor full-scale ratio	 92.8.3.5.4 92.8.3.5.4 92.8.3.5.5 92.8.3.5.5	 0.0083 0.05 1.54 4	
Signal-to-noise-and-distortion ratio, SNDR (min.)	92.8.3.7	26	dB
Output jitter (max.) Even-odd jitter, peak-to-peak Effective bounded uncorrelated jitter, peak-to-peak Effective total uncorrelated jitter, peak-to-peak	 92.8.3.8.1 92.8.3.8.2 92.8.3.8.2	 0.035 0.1 0.18	 UI UI UI
Signaling rate, per lane	92.8.3.9	25.78125±100 ppm	GBd
Unit interval nominal	92.8.3.9	38.787879	ps

92.8.3.1 Signal levels

The differential output voltage v_{di} is defined to be SL*i*<p> minus SL*i*<n>. The common-mode output voltage v_{cmi} is defined to be one half of the sum of SL*i*<p> and SL*i*<n>. These definitions are illustrated by Figure 92–4.

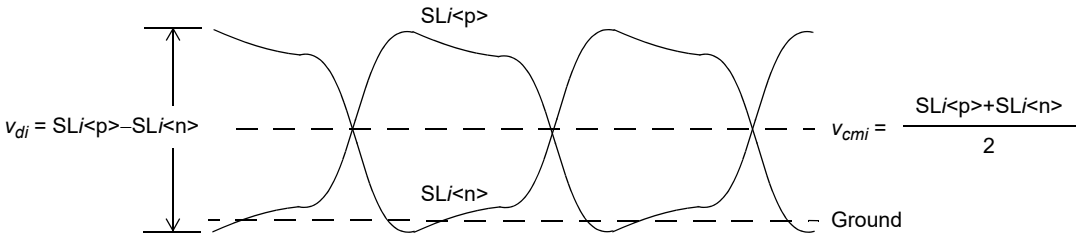

Figure 92–4—Transmitter output voltage definitions

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The peak-to-peak differential output voltage shall be less than or equal to 1200 mV regardless of the transmit equalizer setting. The peak-to-peak differential output voltage shall be less than or equal to 35 mV while the transmitter is disabled (refer to 92.7.6 and 92.7.7).

The 100GBASE-CR4 Style-1 connector may support 100GBASE-CR4 or XLPPI interfaces. For implementations that support both interfaces, the transmitter should not exceed the XLPPI voltage maximum until a 100GBASE-CR4 cable assembly has been identified.

The DC common-mode output voltage shall be between 0 V and 1.9 V with respect to signal ground. The AC common-mode output voltage shall be less than or equal to 30 mV RMS with respect to signal ground. Common-mode output voltage requirements shall be met regardless of the transmit equalizer setting.

If the optional EEE deep sleep capability is supported the following requirements also apply. The peak-to-peak differential output voltage shall be less than 35 mV within 500 ns of the transmitter being disabled. The peak-to-peak differential output voltage shall be greater than 720 mV within 500 ns of the transmitter being enabled. The transmitter is enabled by the assertion of tx_mode=ALERT, and the preceding requirement applies when the transmitted symbols are the periodic pattern defined in 92.8.1 and the transmitter equalizer coefficients are assigned their preset values. The transmitter shall meet the requirements of 92.8.3 within 1 μs of the transmitter being enabled. While the transmitter is disabled, the DC common-mode output voltage shall be maintained to within ±150 mV of the value for the enabled transmitter.

Differential and common-mode signal levels are measured with a PRBS9 test pattern.

92.8.3.2 Transmitter differential output return loss

The differential output return loss, in dB, of the transmitter shall meet Equation (92–1). This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$Return\_loss(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}(f/14) & 8 \leq f \leq 19 \end{cases} \quad \text{(dB)} \tag{92–1}$$

where

f is the frequency in GHz

$Return\_loss(f)$ is the differential output return loss at frequency f

The transmitter differential output return loss is illustrated in Figure 92–5.

92.8.3.3 Common-mode to differential mode output return loss

The common-mode to differential mode output return loss, in dB, of the transmitter shall meet Equation (92–2).

$$Return\_loss(f) \geq \begin{cases} 22 - (20/25.78)f & 0.01 \leq f < 12.89 \\ 15 - (6/25.78)f & 12.89 \leq f \leq 19 \end{cases} \quad \text{(dB)} \tag{92–2}$$

where

f is the frequency in GHz

$Return\_loss(f)$ is the common-mode to differential mode output return loss at frequency f

The common-mode to differential mode output return loss is illustrated in Figure 92–6.

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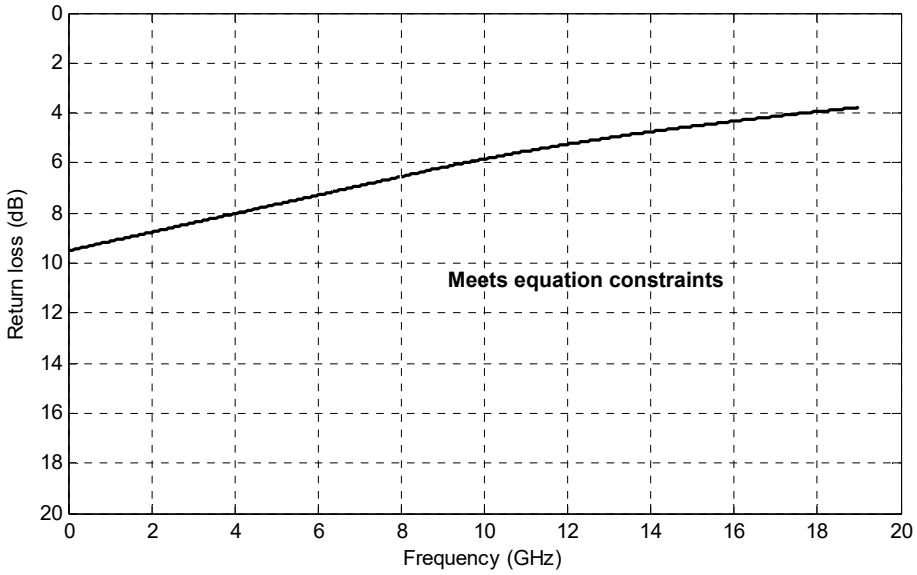

Figure 92–5—Transmitter differential output return loss

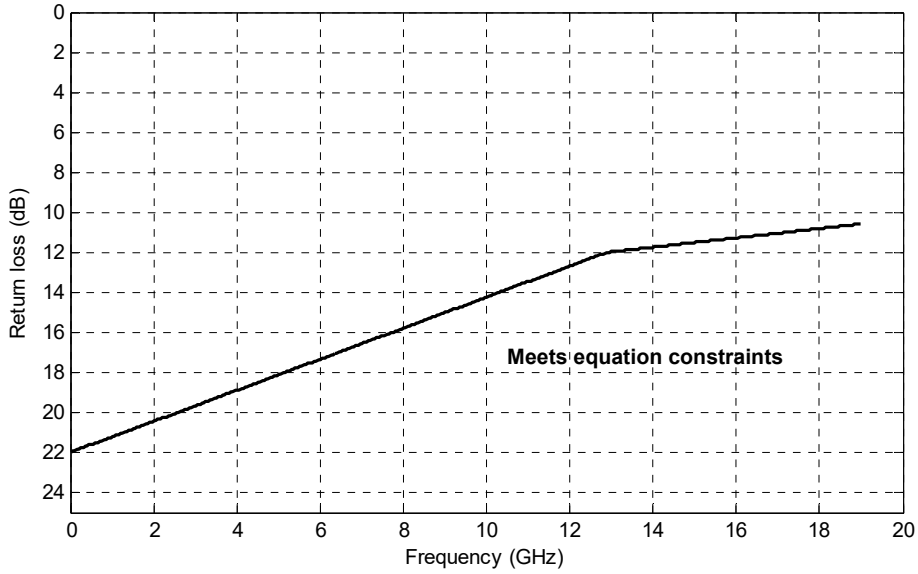

Figure 92–6—Common-mode to differential mode return loss

92.8.3.4 Common-mode to common-mode output return loss

The common-mode to common-mode output return loss, in dB, of the transmitter shall meet Equation (92–3).

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$$Return\_loss(f) \geq 2 \quad \text{(dB)} \tag{92–3}$$

for $0.2 \leq f \leq 19$ GHz

where

f is the frequency in GHz

$Return\_loss(f)$ is the common-mode to common-mode return loss at frequency f

92.8.3.5 Transmitter output waveform

The 100GBASE-CR4 transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in Figure 92–7.

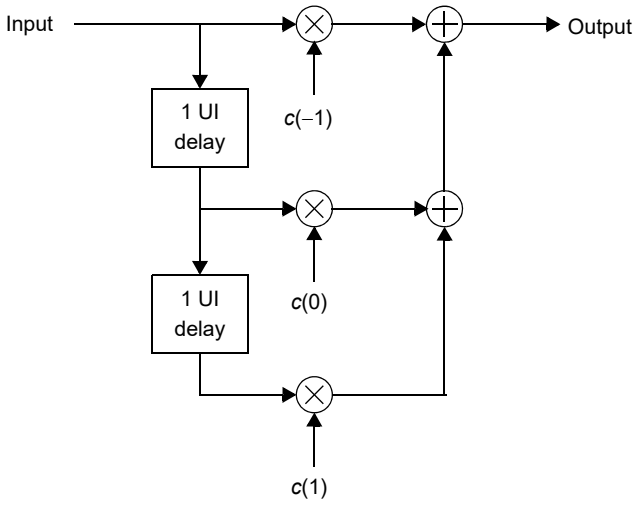

Figure 92–7—Transmit equalizer functional model

The state of the transmit equalizer and hence the transmitted output waveform may be manipulated via the PMD control function defined in 92.7.12 or via the management interface. The transmit function responds to a set of commands issued by the link partner's receive function and conveyed by a back-channel communications path.

This command set includes instructions to

a) Increment coefficient $c(i)$.
b) Decrement coefficient $c(i)$.
c) Hold coefficient $c(i)$ at its current value.
d) Set the coefficients to a predefined value (preset or initialize).

In response, the transmit function relays status information to the link partner's receive function. The status messages indicate that

a1) The requested update to coefficient $c(i)$ has completed (updated).
b1) Coefficient $c(i)$ is at its minimum value.
c1) Coefficient $c(i)$ is at its maximum value.
d1) Coefficient $c(i)$ is ready for the next update request (not_updated).

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92.8.3.5.1 Linear fit to the measured waveform

For each configuration of the transmit equalizer, capture at least one complete cycle of the test pattern PRBS9 as specified in 83.5.10 at TP2 per 85.8.3.3.4. In the following calculation, M should be an integer not less than 32. Interpolation of the captured waveform may be used to achieve this. Compute the linear fit pulse response $p(k)$ from the captured waveform per 85.8.3.3.5 using $N_p = 14$ and $D_p = 2$. Define $r(k)$ to be the linear fit pulse response when transmit equalizer coefficients have been set to the "preset" values. The coefficients for any configuration of the transmit equalizer are computed using the following method.

Define an MN_p-by-3 matrix R_m. The elements of R_m are assigned values per Equation (92–4) where $i = -1$ to 1, $j = 1$ to MN_p, and $m = -M/2$ to $M/2-1$ when M is even and $-(M-1)/2$ to $(M-1)/2$ when M is odd.

$$R_m(j, i+2) = \left\{ \begin{array}{cc} r(m+j-iM) & 1 \le m+j-iM \le MN_p \\ 0 & otherwise \end{array} \right\} \tag{92–4}$$

The coefficients of the transmit equalizer are computed using Equation (92–5).

$$\begin{bmatrix} c_m(-1) \\ c_m(0) \\ c_m(1) \end{bmatrix} = (R_m^T R_m)^{-1} R_m^T \begin{bmatrix} p(1) \\ \dots \\ p(MN_p) \end{bmatrix} \tag{92–5}$$

The linear fit pulse response is reconstructed from the matrix R_m and the coefficients using Equation (92–6).

$$\begin{bmatrix} p_m(1) \\ \dots \\ p_m(MN_p) \end{bmatrix} = R_m \begin{bmatrix} c_m(-1) \\ c_m(0) \\ c_m(1) \end{bmatrix} \tag{92–6}$$

The sum of the squared error between $p(k)$ and $p_m(k)$ is computed using Equation (92–7). The transmit equalizer coefficients $c(i)$ for a given linear fit pulse $p(k)$ are the values $c_m(i)$ for the value of m that minimizes $\varepsilon^2(m)$.

$$\varepsilon^2(m) = \sum_{k=1}^{MN_p} (p(k) - p_m(k))^2 \tag{92–7}$$

92.8.3.5.2 Steady-state voltage and linear fit pulse peak

The steady-state voltage v_f is defined to be the sum of the linear fit pulse $p(k)$ divided by M (refer to 85.8.3.3 step 3). The steady-state voltage shall be greater than or equal to 0.34 V and less than or equal to 0.6 V after the transmit equalizer coefficients have been set to the "preset" values.

The peak value of $p(k)$ shall be greater than $0.45 \times v_f$ after the transmit equalizer coefficients have been set to the "preset" values.

92.8.3.5.3 Coefficient initialization

When the PMD enters the INITIALIZE state of the Training state diagram (Figure 72–5) or receives a valid request to "initialize" from the link partner, the coefficients of the transmit equalizer shall be configured such that the ratio $(c(0)+c(1)-c(-1))/(c(0)+c(1)+c(-1))$ is $1.29 \pm 10\%$ and the ratio

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$(c(0)–c(1)+c(–1))/(c(0)+c(1)+c(–1))$ is $2.57 \pm 10\%$. These requirements apply upon the assertion of a coefficient status report of "updated" for all coefficients.

92.8.3.5.4 Coefficient step size

The change in $c(i)$ corresponding to a request to "increment" that coefficient shall be between 0.0083 and 0.05. The change in $c(i)$ corresponding to a request to "decrement" that coefficient shall be between –0.0083 and –0.05.

The change in the coefficient is defined to be the difference in the value measured prior to the assertion of the "increment" or "decrement" request (e.g., the coefficient update request for all coefficients is "hold") and the value upon the assertion of a coefficient status report of "updated" for that coefficient.

92.8.3.5.5 Coefficient range

When sufficient "increment" or "decrement" requests have been received for a given coefficient, the coefficient will reach a lower or upper bound based on the range of that coefficient or the combination of coefficients.

With $c(–1)$ set to zero and both $c(0)$ and $c(1)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0) – c(1))/(c(0) + c(1))$ shall be greater than or equal to 4.

With $c(1)$ set to zero and both $c(–1)$ and $c(0)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0) – c(–1))/(c(0) + c(–1))$ shall be greater than or equal to 1.54.

Note that a coefficient may be set to zero by first asserting a coefficient preset request and then manipulating the other coefficients as required by the test.

92.8.3.6 Insertion loss TP0 to TP2 or TP3 to TP5

The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is given by Equation (92–8). Note that the recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 is 9.85 dB at 12.8906 GHz.

$$Insertion\_loss(f) \le \left\{ \begin{array}{ll} 0.08 + 0.57\sqrt{f} + 0.599f & 0.01 \le f < 14 \\ -19.067 + 2.119f & 14 \le f \le 19 \end{array} \right\} \text{ (dB)} \qquad (92–8)$$

where

f is the frequency in GHz

$Insertion\_loss(f)$ is the insertion loss at frequency f

The maximum insertion loss of TP0 to TP2 or TP3 to TP5 is illustrated in Figure 92–8.

92.8.3.7 Transmitter signal-to-noise-and-distortion ratio (SNDR)

Signal-to-noise-and-distortion ratio (SNDR) is measured at the transmitter output using the following method, with transmitters on all PMD lanes enabled and transmitting the same pattern with identical transmit equalizer settings.

Given a configuration of the transmit equalizer, capture at least one complete cycle of the test pattern PRBS9 as specified in 83.5.10 at TP0a per 85.8.3.3.4. Compute the linear fit pulse response $p(k)$ and the linear fit

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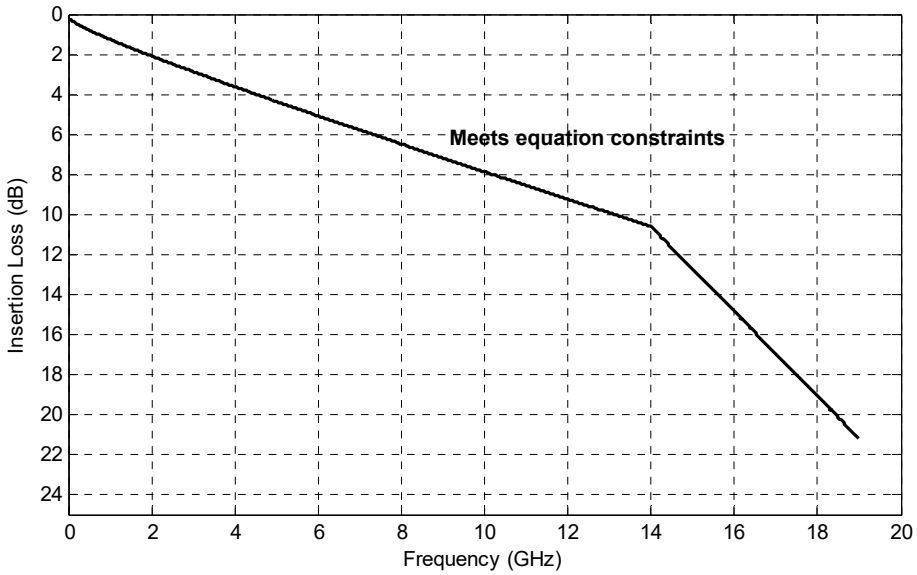

Figure 92–8—Maximum insertion loss TP0 to TP2 or TP3 to TP5

error waveform $e(k)$ from the captured waveform per 85.8.3.3.5 using $N_p = 14$ and $D_p = 2$. Denote the standard deviation of $e(k)$ as σ_e.

Given the same configuration of the transmit equalizer, measure the RMS deviation from the mean voltage at a fixed point in a run of at least 8 consecutive identical bits in a suitable pattern. PRBS9 is an example of a pattern that includes runs suitable to perform the measurement. It is recommended that the deviation is measured within the flattest portion of the waveform at a point where the slope is closest to zero. The RMS deviation is measured for a run of zeros and also a run of ones. The average of the two measurements is denoted as σ_n.

SNDR is defined by Equation (92–9) where $p_{\max}$ is the maximum value of $p(k)$.

$$SNDR = 10\log_{10}\left(\frac{p_{\max}^2}{\sigma_e^2 + \sigma_n^2}\right) \text{ dB} \tag{92–9}$$

SNDR shall be greater than 26 dB regardless of the transmit equalizer setting.

92.8.3.8 Transmitter output jitter

Three components of the transmitter output jitter are specified in this subclause: even-odd jitter, effective bounded uncorrelated jitter, and effective total uncorrelated jitter.

The effect of a single-pole high-pass filter with a 3 dB frequency of 10 MHz is applied to the jitter. The voltage threshold for the measurement of BER or crossing times is the mid-point (0 V) of the AC-coupled differential signal.

Jitter measurements are performed with transmitters on all PMD lanes enabled and transmitting the same pattern with identical transmit equalizer settings.

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92.8.3.8.1 Even-odd jitter

Even-odd jitter is measured using two repetitions of a PRBS9 pattern. The deviation of the time of each transition from an ideal clock at the signaling rate is measured. Even-odd jitter is defined as the magnitude of the difference between the average deviation of all even-numbered transitions and the average deviation of all odd-numbered transitions, where determining if a transition is even or odd is based on possible transitions but only actual transitions are measured and averaged.

Even-odd jitter shall be less than or equal to 0.035 UI regardless of the transmit equalization setting.

NOTE—Even-odd jitter has been referred to as *duty cycle distortion* by other Physical Layer specifications for operation over electrical backplane or twinaxial copper cable assemblies (see 72.7.1.9). The term *even-odd jitter* is used here to distinguish it from the duty cycle distortion referred to by Physical Layer specifications for operation over fiber optic cabling.

92.8.3.8.2 Effective bounded uncorrelated jitter and effective random jitter

Effective bounded uncorrelated jitter and effective random jitter are measured on each of two specific transitions in a PRBS9 pattern (see 83.5.10). The two transitions occur in the sequence of five zeros and four ones and nine ones and five zeros, respectively. The sequences are located at bits 10 to 18 and 1 to 14, respectively, where bits 1 to 9 are the run of nine ones.

a) The jitter components are determined according to the following method. Acquire a horizontal histogram of a transition around the zero-crossing point. The number of acquired samples should be sufficiently large to yield consistent measurement results. Designate the total number of samples as *NS*, the number of bins as *NB*, the number of samples in each bin as N_i where i is the bin number from 1 to *NB*, and the sample time corresponding with the center of each bin as t_i.
b) Create two cumulative distribution curves $CDFL_i$ and $CDFR_i$ according to Equation (92–10) and Equation (92–11) and two corresponding curves QR_i and QL_i according to Equation (92–12) and Equation (92–13), where $\text{erfc}^{-1}(x)$ is the inverse of the complementary error function $\text{erfc}(x)$ defined by Equation (92–14).
c) Determine the parameters m_{left} and b_{left} of Equation (92–15) that best fit QL_i as a function of t_i for bins with $CDFL_i$ in the range of 10^{-3} to 2.5×10^{-2}. Similarly determine the parameters of m_{right} and b_{right} that best fit QR_i as a function of t_i for bins with $CDFR_i$ in the range of 10^{-3} to 2.5×10^{-2}.
d) Calculate the values of effective bounded uncorrelated jitter and effective total uncorrelated jitter according to Equation (92–17) and Equation (92–19), respectively. The peak-to-peak contribution of the effective random jitter in the effective total uncorrelated jitter is related to a bit error ratio of 10^{-5}.

$$CDFL_i = \sum_{k=1}^{i} \frac{N_k}{NS} \tag{92–10}$$

$$CDFR_i = \sum_{k=i}^{NB} \frac{N_k}{NS} \tag{92–11}$$

$$QL_i = \sqrt{2} \times \text{erfc}^{-1}(2 \times CDFL_i) \tag{92–12}$$

$$QR_i = \sqrt{2} \times \text{erfc}^{-1}(2 \times CDFR_i) \tag{92–13}$$

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$$\text{erfc}(x) = \frac{2}{\sqrt{\pi}} \times \int_{x}^{\infty} e^{-t^2} dt \quad (92\text{–}14)$$

$$Q_{left} = m_{\text{left}} \times t + b_{\text{left}} \quad (92\text{–}15)$$

$$Q_{right} = m_{\text{right}} \times t + b_{\text{right}} \quad (92\text{–}16)$$

$$\text{effective bounded uncorrelated jitter} = EBUJ = b_{\text{left}} / m_{\text{left}} - b_{\text{right}} / m_{\text{right}} \quad (92\text{–}17)$$

$$\text{effective random jitter} = ERJ = \frac{m_{\text{left}} - m_{\text{right}}}{2 \times m_{\text{right}} \times m_{\text{left}}} \quad (92\text{–}18)$$

$$\text{effective total uncorrelated jitter} = 7.9 \times ERJ + EBUJ \quad (92\text{–}19)$$

Effective bounded uncorrelated jitter shall be less than or equal to 0.1 UI peak-to-peak regardless of the transmit equalization setting.

The effective total uncorrelated jitter shall be less than or equal to 0.18 UI peak-to-peak regardless of the transmit equalization setting.

92.8.3.9 Signaling rate range

The 100GBASE-CR4 MDI signaling rate shall be 25.78125 GBd ±100 ppm per lane. The corresponding unit interval is approximately 38.787879 ps.

92.8.4 Receiver characteristics

The receiver characteristics are summarized in Table 92–7. Unless specified otherwise, all receiver measurements defined in Table 92–7 are made at TP3 utilizing the test fixtures specified in 92.11.1. Unless otherwise specified, a test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all receiver input signal measurements. The receiver specifications at TP5 are provided informatively in Annex 92A.

Table 92–7—Receiver characteristics at TP3 summary

Parameter	Subclause reference	Value	Units
Receiver input amplitude tolerance	92.8.4.1	1200 mV as measured at TP2	mV
Differential input return loss (min)	92.8.4.2	Equation (92–20)	dB
Differential to common-mode input return loss	92.8.4.3	Equation (92–21)	dB
Interference Tolerance	92.8.4.4	Table 92–8	—
Signaling rate, per lane	92.8.4.6	25.78125 ± 100 ppm	GBd
Unit interval (UI) nominal	92.8.4.6	38.787879	ps

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92.8.4.1 Receiver input amplitude tolerance

100GBASE-CR4 receiver shall operate at a BER better than 10^{-5} when connected to a compliant transmitter whose peak-to-peak differential output voltage, as defined by 92.8.3.1 using preset equalizer coefficients, is 1200 mV using a compliant cable assembly with the minimum insertion loss defined in 92.10.2. The receiver is allowed to control the transmitter equalizer coefficients, using the protocol defined in 92.7.12 or an equivalent process, to meet this requirement.

92.8.4.2 Receiver differential input return loss

The differential input return loss, in dB, of the receiver shall meet Equation (92–20). The reference impedance for differential return loss measurements shall be 100 Ω.

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}(f/14) & 8 \leq f \leq 19 \end{array} \right\} \quad \text{(dB)} \tag{92–20}$$

where

f is the frequency in GHz

$Return\_loss(f)$ is the differential input return loss at frequency f

92.8.4.3 Differential to common-mode input return loss

The differential to common-mode input return loss, in dB, of the receiver shall meet Equation (92–21).

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 22 - (20/25.78)f & 0.01 \leq f < 12.89 \\ 15 - (6/25.78)f & 12.89 \leq f \leq 19 \end{array} \right\} \quad \text{(dB)} \tag{92–21}$$

where

f is the frequency in GHz

$Return\_loss(f)$ is the differential to common-mode input return loss at frequency f

92.8.4.4 Receiver interference tolerance test

The receiver interference tolerance of each lane shall comply with both test 1 and test 2 using the parameters of Table 92–8 when measured according to the requirements of 92.8.4.4.1 to 92.8.4.4.5. The cable assembly used in the test channel specified in 92.8.4.4.2 shall meet the cable assembly Channel Operating Margin (COM) specified in 92.10.7.

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Table 92–8—100GBASE-CR4 interference tolerance parameters

Parameter	Test 1 values	Test 2 values	Units
RS-FEC symbol error ratio[a] (max)	10^{-4}	10^{-4}	
Fitted insertion loss coefficients	$a_1 = 1.7$ $a_2 = 0.546$ $a_4 = 0.01$	$a_1 = 4.3$ $a_2 = 0.571$ $a_4 = 0.04$	dB/√GHz dB/GHz dB/GHz^2
Applied SJ[b] (peak-to-peak)	0.1	0.1	UI
Applied RJ (RMS)	0.01	0.01	UI
Even-odd jitter	0.035	0.035	UI
COM[c]	3	3	dB

[a]The FEC symbol error ratio is measured in step 10 of the receiver interference tolerance method defined in 93C.2.
[b]Applied SJ frequency >100 MHz, specified at TP0.
[c]The COM value is the target for the far-end aggressor amplitude calibration defined in 92.8.4.4.3 step d). The far-end aggressor amplitude should be as close as practical to the value needed to produce the target COM. If higher amplitude values are used, this would demonstrate margin to the specification but this is not required for compliance.

92.8.4.4.1 Test setup

The interference tolerance test is performed with the setup shown in Figure 92–9. The requirements of this subclause are verified at the pattern generator connection (PGC) or test references in Figure 92–9 and Figure 92–10. The lanes under test (LUT) are illustrated in Figure 92–9 and Figure 92–10. The cable assembly single-ended receive lanes are terminated in 50 Ω to provide 100 Ω differential termination.

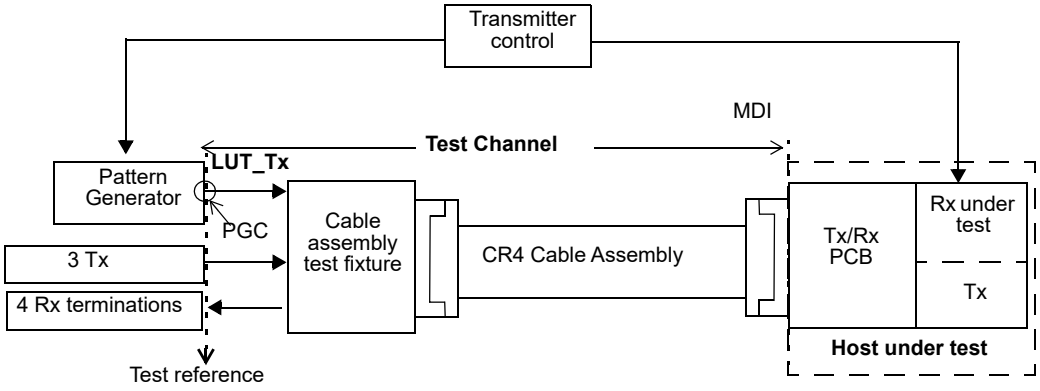

Figure 92–9—Interference tolerance test setup

92.8.4.4.2 Test channel

The test channel consists of the following:

a) A cable assembly that meets the cable assembly COM specified in 92.10.7.

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b) A cable assembly test fixture
c) A connecting path from the pattern generator to the cable assembly test fixture

92.8.4.4.3 Test channel calibration

The scattering parameters of the test channels are characterized at the test references as illustrated in Figure 92–10 using the cable assembly test fixtures specified in 92.11.2.

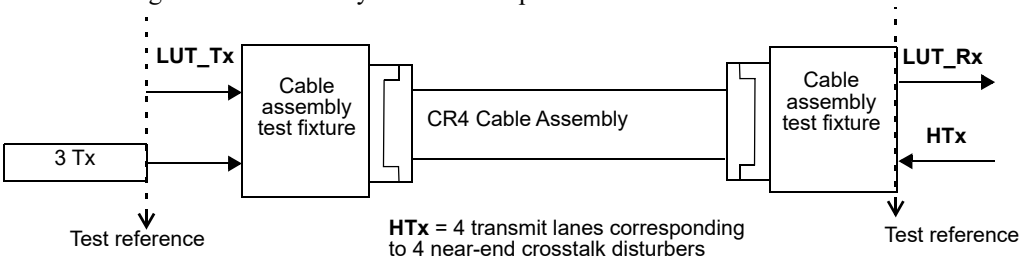

Figure 92–10—Test channel calibration

The fitted insertion loss coefficients of the lane under test (LUT), derived using the fitting procedure in 92.10.2, shall meet the test values in Table 92–8. It is recommended that the deviation between the insertion loss and the fitted insertion loss be as small as practical and that the fitting parameters be as close as practical to the values given in Table 92–8.

The far-end crosstalk disturbers consist of 100GBASE-CR4 transmitters. It is recommended that the transition time, equalization setting, and path from the far-end crosstalk disturbers to the cable assembly test fixture emulate the pattern generator as much as practical. For 100GBASE-CR4 test channels, the crosstalk that is coupled into a receive lane is from three transmitters. The disturber transmitters send scrambled idle encoded by RS-FEC. The amplitudes of each of the disturbers should be set to the value that results in the COM value given in Table 92–8 when calculated by the method given below.

The COM shall be calculated using the method and parameters of 92.10.7 with the following exceptions:

a) The channel signal path is $SCHS_p^{(k)} = \text{cascade}(\text{cascade}(S^{(CTSP)}, S^{(HOSP)}))$, where $S^{(CTSP)}$ is the measured channel between the test references for the LUT in Figure 92–10.
b) The channel far-end crosstalk path is $SCHNXT_p^{(k)} = \text{cascade}(\text{cascade}(S^{(CTFXTk)}, S^{(HOSP)}))$, where $S^{(CTFXTk)}$ is the measured FEXT channel between the test references [3 Tx] and LUT_Rx in Figure 92–10.
c) The value of the far-end aggressor amplitude A_{fe} is adjusted until the required COM is achieved. The far end aggressors ([3 Tx] in Figure 92–9) peak-to-peak amplitude is set to twice the resulting value for the test.
d) If the test transmitter presents a high-quality termination, e.g., it is a piece of test equipment, the transmitter device package model $S^{(tp)}$ is omitted from the calculation of $S_p^{(k)}$. Instead, the voltage transfer function is multiplied by the filter $H_t(f)$ defined by Equation (92–22) where T_r is the 20% to 80% transition time in ns (see 86A.5.3.3) of the signal as measured at TP0a and f is frequency in GHz.

$$H_t(f) = \exp(-2(\pi f T_r / 1.6832)^2) \quad (92–22)$$

92.8.4.4.4 Pattern generator

The pattern generator transmits data to the device under test. At the start of transmitter training, the pattern generator output amplitude shall be 800 mV peak-to-peak differential when measured on an alternating one-

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zero pattern. The output amplitude, measured on an alternating one zero pattern, is not permitted to exceed 800 mV peak-to-peak differential during transmitter training. The pattern generator shall be set to match the jitter specification in Table 92–8. The output waveform of the pattern generator shall comply to 93.8.1.

92.8.4.4.5 Test procedure

For 100GBASE-CR4 testing, the pattern generator is first configured to transmit the training pattern defined in 92.7.12. During this initialization period, the device under test (DUT) configures the pattern generator equalizer, via transmitter control, to the coefficient settings it would select using the protocol described in 72.6.10 and the receiver is tuned using its optimization method.

After the pattern generator equalizer has been configured and the receiver tuned, the pattern generator is set to generate scrambled idle encoded by RS-FEC. The receiver under test shall meet the target RS-FEC symbol error ratio listed in Table 92–8. During the tests, the disturbers transmit at their calibrated level and all of the transmitters in the device under test transmit scrambled idle encoded by RS-FEC, with the maximum compliant amplitude and equalization turned off (preset condition).

92.8.4.5 Receiver jitter tolerance

Receiver jitter tolerance is defined by the procedure in this subclause. When measured using the test setup shown in Figure 92–9, or its equivalent, the RS-FEC symbol error ratio for each lane of the receiver shall be less than or equal to 10^{-4} for each case listed in Table 92–9. The pattern generator meets the requirements of 92.8.4.4.4. The test channel meets the requirements of the interference tolerance test channel using Test 2 values listed in Table 92–8.

The test procedure is as described in 92.8.4.4.5 except that during the test the disturber transmitters are off and the pattern generator jitter is set to the frequency and peak-to-peak amplitude specified in Table 92–9.

Table 92–9—Receiver jitter tolerance parameters

Parameter	Case A values	Case B values	Units
Jitter frequency	190	940	kHz
Peak-to-peak jitter amplitude	5	1	UI

92.8.4.6 Signaling rate range

A 100GBASE-CR4 receiver shall comply with the requirements of 92.8.4.4 for any signaling rate in the range 25.78125 GBd ± 100 ppm. The corresponding unit interval is approximately 38.787879 ps.

92.9 Channel characteristics

The 100GBASE-CR4 channel is defined between TP0 and TP5 to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly as illustrated in Figure 92–2. The channel parameters insertion loss, return loss, COM and the transmitter and receiver differential controlled impedance printed circuit board parameters for each differential lane are provided informatively in 92A.4 through 92A.7.

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92.10 Cable assembly characteristics

The 100GBASE-CR4 cable assembly contains insulated conductors terminated in a connector at each end for use as a link segment between MDIs. This cable assembly is primarily intended as a point-to-point interface of up to 5 m between network ports using controlled impedance cables. All cable assembly measurements are to be made between TP1 and TP4 with cable assembly test fixtures as specified in 92.11.2 and illustrated in Figure 92–17. These cable assembly specifications are based upon twinaxial cable characteristics, but other cable types are acceptable if the specifications of 92.10 are met.

The cable assembly COM is specified in 92.10.7.

Table 92–10 provides a summary of the cable assembly characteristics and references to the subclauses addressing each parameter; reported values are at 12.8906 GHz.

Table 92–10—Cable assembly differential characteristics summary

Description	Reference	Value	Unit
Maximum insertion loss at 12.8906 GHz	92.10.2	22.48	dB
Minimum insertion loss at 12.8906 GHz	92.10.2	8	dB
Minimum return loss at 12.8906 GHz	92.10.3	6	dB
Differential to common-mode return loss	92.10.4	Equation (92–28)	dB
Differential to common-mode conversion loss	92.10.5	Equation (92–29)	dB
Common-mode to common-mode return loss	92.10.6	Equation (92–30)	dB

92.10.1 Characteristic impedance and reference impedance

The nominal differential characteristic impedance of the cable assembly is 100 Ω. The differential reference impedance for cable assembly specifications shall be 100 Ω.

92.10.2 Cable assembly insertion loss

The fitted cable assembly insertion loss $IL_{fitted}(f)$ as a function of frequency f is defined in Equation (92–23).

$$IL_{\text{fitted}}(f) = a_1\sqrt{f} + a_2 f + a_4 f^2 \quad \text{(dB)} \tag{92–23}$$

where

f is the frequency in GHz

$IL_{\text{fitted}}(f)$ is the fitted cable assembly insertion loss at frequency f

Given the cable assembly insertion loss measured between TP1 and TP4 is at N uniformly-spaced frequencies f_n spanning the frequency range 50 MHz to 19 000 MHz with a maximum frequency spacing of 10 MHz, the coefficients of the fitted insertion loss are determined using Equation (92–24) and Equation (92–25).

Define the frequency matrix F as shown in Equation (92–24).

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$$F = \begin{bmatrix} \sqrt{f_1} & f_1 & f_1^2 \\ \sqrt{f_2} & f_2 & f_2^2 \\ \cdots & \cdots & \cdots \\ \sqrt{f_N} & f_N & f_N^2 \end{bmatrix} \tag{92–24}$$

The polynomial coefficients a_1, a_2, and a_4 are determined using Equation (92–25). In Equation (92–25), T denotes the matrix transpose operator and IL is a column vector of the measured insertion loss values, IL_n at each frequency f_n.

$$\begin{bmatrix} a_1 \\ a_2 \\ a_4 \end{bmatrix} = (F^T F)^{-1} F^T IL \tag{92–25}$$

The fitted insertion loss corresponding to one example of the maximum insertion loss at 12.8906 GHz is illustrated in Figure 92–11.

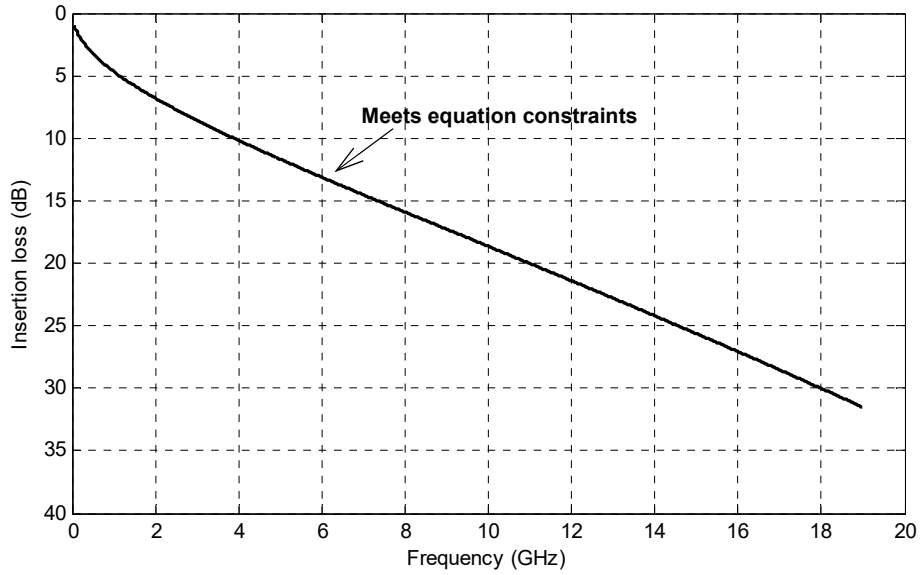

Figure 92–11—Example maximum cable assembly insertion loss

The measured insertion loss of the cable assembly shall be greater than or equal to the minimum cable assembly insertion loss given in Equation (92–26) and illustrated in Figure 92–12. The measured insertion loss of the cable assembly shall be less than or equal to the maximum cable insertion loss of 22.48 dB at 12.8906 GHz.

$$IL_{Cabmin}(f) = 0.7\sqrt{f} + 0.3f + 0.01f^2 \quad \text{(dB)} \tag{92–26}$$

where

f is the frequency in GHz

$IL_{\text{Cabmin}}(f)$ is the minimum cable assembly insertion loss at frequency f

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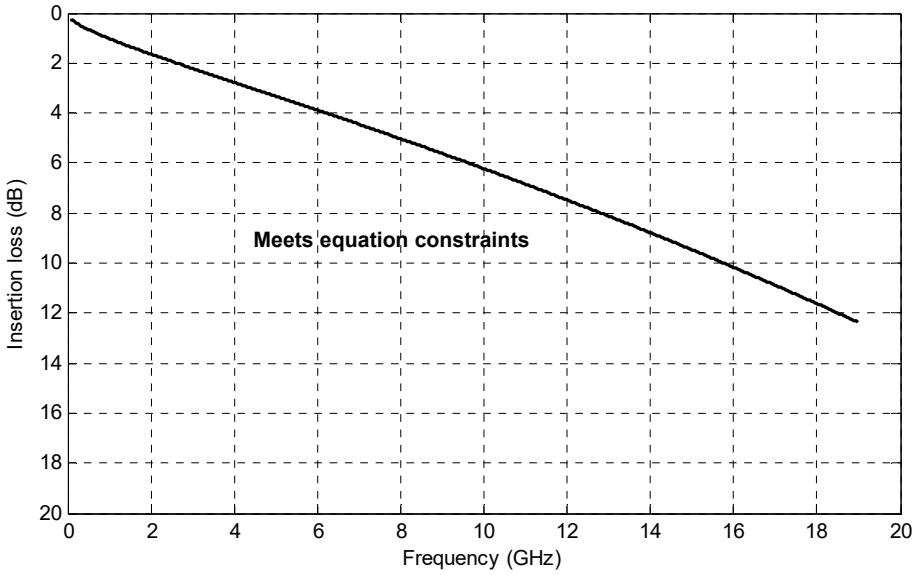

Figure 92–12—Minimum cable assembly insertion loss

Table 92–11—Maximum and minimum cable assembly insertion loss characteristics

Description	Value	Unit
Maximum insertion loss at 12.8906 GHz	22.48	dB
Minimum insertion loss at 12.8906 GHz	8	dB

92.10.3 Cable assembly differential return loss

The differential return loss of each pair of the 100GBASE-CR4 cable assembly shall meet the values determined using Equation (92–27).

$$Return\_loss(f) \geq \begin{cases} 16.5 - 2\sqrt{f} & 0.05 \leq f < 4.1 \\ 10.66 - 14\log_{10}(f/5.5) & 4.1 \leq f \leq 19 \end{cases} \text{ (dB)} \qquad (92\text{–}27)$$

where

f is the frequency in GHz

$Return\_loss(f)$ is the return loss at frequency f

The minimum cable assembly return loss is illustrated in Figure 92–13.

92.10.4 Differential to common-mode return loss

The differential to common-mode return loss, in dB, of the cable assembly shall meet Equation (92–28).

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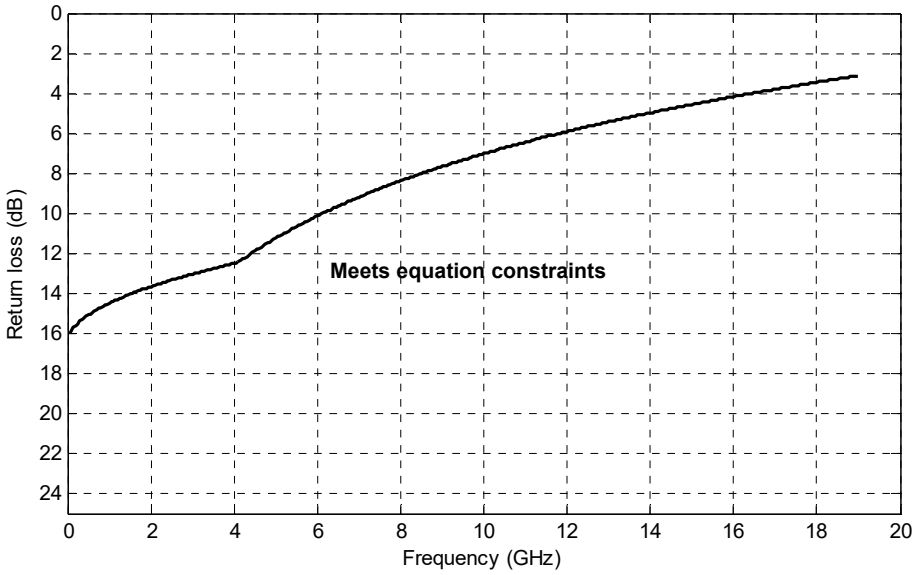

Figure 92–13—Minimum cable assembly return loss

$$Return\_loss(f) \geq \begin{cases} 22 - (20/25.78)f & 0.01 \leq f < 12.89 \\ 15 - (6/25.78)f & 12.89 \leq f \leq 19 \end{cases} \quad \text{(dB)} \qquad (92\text{–}28)$$

where

f is the frequency in GHz

$Return\_loss(f)$ is the return loss at frequency f

The differential to common-mode cable assembly return loss is illustrated in Figure 92–14.

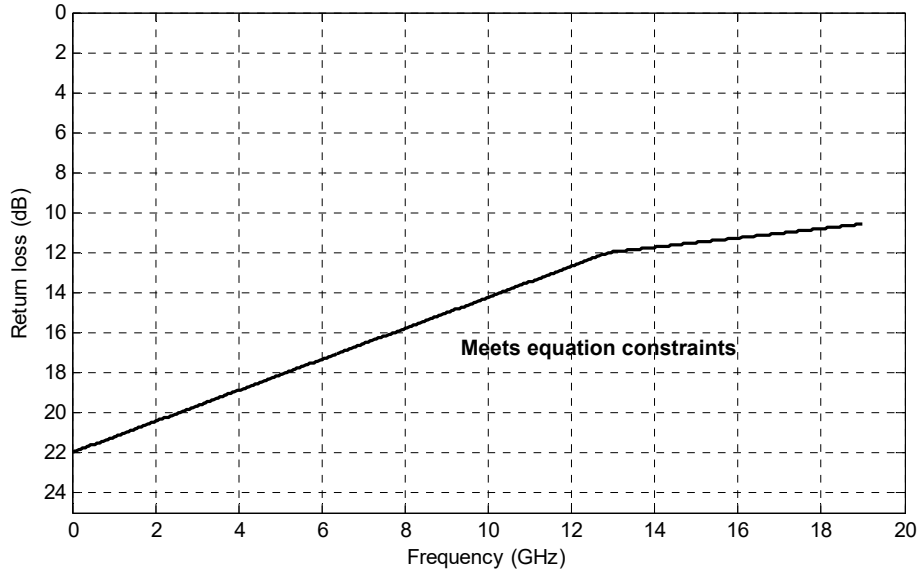

Figure 92–14—Differential to common-mode cable assembly return loss

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92.10.5 Differential to common-mode conversion loss

The difference between the cable assembly differential to common-mode conversion loss and the cable assembly insertion loss shall meet Equation (92–29).

$$Conversion\_loss\ (f) - IL(f) \geq \left\{ \begin{array}{ll} 10 & 0.01 \leq f < 12.89 \\ 27 - (29/22)f & 12.89 \leq f < 15.7 \\ 6.3 & 15.7 \leq f \leq 19 \end{array} \right\} \quad (92–29)$$

where

f	is the frequency in GHz
$Conversion\_loss(f)$	is the cable assembly differential to common-mode conversion loss
$IL(f)$	is the cable assembly insertion loss

92.10.6 Common-mode to common-mode return loss

The common-mode to common-mode return loss, in dB, of the cable assembly shall meet Equation (92–30).

$$Return\_loss(f) \geq 2 \quad (\text{dB}) \quad (92–30)$$

for $0.2 \leq f \leq 19$ GHz

where

f	is the frequency in GHz
$Return\_loss(f)$	is the common-mode to common-mode return loss at frequency f

92.10.7 Cable assembly Channel Operating Margin

The cable assembly Channel Operating Margin (COM) for each victim signal path (receive lane) is derived from measurements of the cable assembly victim signal path, the four individual near-end crosstalk paths, and the three far-end crosstalk paths that can couple into a victim signal path. COM is computed using the procedure in 93A.1 with the Test 1 and Test 2 values in Table 93–8 and the signal paths defined in 92.10.7.1 and 92.10.7.2. Test 1 and Test 2 differ in the value of the device package model transmission line length z_p.

NOTE—For cable lengths greater than 4 m a frequency step (Δf) no larger than 5 MHz is recommended.

The cable assembly COM shall be greater than or equal to 3 dB for each test. This minimum value allocates margin for practical limitations on the receiver implementation as well as the largest step size allowed for transmitter equalizer coefficients.

92.10.7.1 Channel signal path

The channel signal path between TP0 and TP5 for the cable assembly COM consists of the measured cable assembly signal path (TP1 and TP4), a representative transmitter PCB signal path (TP0 to TP1), and a representative receiver PCB signal path (TP4 to TP5). The signal path definitions include the function cascade() defined in 93A.1.2.1.

The channel signal path to be used in COM (93A.1.2) is the concatenation of the cable assembly signal path measurement, the transmitter PCB signal path, and the receiver PCB signal path using Equation (92–31) (see 93A.1.2.1). The transmitter and receiver PCB signal paths are calculated according to 92.10.7.1.1.

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$$SCHS_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOSP)}, S^{(CASP)}), S^{(HOSP)}) \quad (92–31)$$

where

$SCHS_p^{(k)}$ is the channel signal path

$S^{(HOSP)}$ is the signal path calculated according to 92.10.7.1.1

$S^{(CASP)}$ is the cable assembly signal path

k is equal to zero

92.10.7.1.1 TP0 to TP1 and TP4 to TP5 signal paths

The additional transmitter and receiver PCB signal paths are calculated using the method defined in 93A.1.2.3. The scattering parameters for a PCB of length z_p are defined by Equation (93A–13), Equation (93A–14), and the parameter values given in Table 92–12.

For the channel signal path defined in 92.10.7.1 and calculated using Equation (92–31), the transmitter and receiver PCB model are each z_p = 151 mm in length representing an insertion loss of 6.26 dB at 12.89 GHz and are each denoted as $S^{(HOSP)}$.

For the channel crosstalk paths defined in 92.10.7.2 and calculated using Equation (92–32) and Equation (92–33), the receiver PCB model is $S^{(HOSP)}$. The transmitter PCB model is z_p = 72 mm in length representing an insertion loss of 3 dB at 12.89 GHz and is denoted as $S^{(HOTxSP)}$. The transmitter PCB insertion loss for the crosstalk channel is less than that for the signal channel to allow for a reasonable worst-case crosstalk in the COM calculation.

Table 92–12—Transmission line model parameters

Parameter	Value	Units
γ_0	0	1/mm
a_1	4.114×10^{-4}	$ns^{1/2}$/mm
a_2	2.547×10^{-4}	ns/mm
τ	6.191×10^{-3}	ns/mm
Z_c	109.8	Ω

92.10.7.2 Channel crosstalk paths

The channel structure includes three far-end and four near-end crosstalk paths. The MDI is the significant contributor to the channel crosstalk and is included in and characterized by the cable assembly crosstalk measurements. The cable assembly crosstalk signal paths to be used in COM are the four individual near-end crosstalk paths and the three far-end crosstalk paths that can couple into a victim signal path using the cascaded function defined in 93A.1.2.1 given in Equation (92–32) and Equation (92–33).

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$$SCHNXT_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOTxSP)}, S^{(CANXTk)}), S^{(HOSP)}) \quad (92–32)$$

where

$SCHNXT_p^{(k)}$	is the channel near-end crosstalk path
$S^{(HOSP)}$	is the signal path calculated according to 92.10.7.1.1
$S^{(HOTxSP)}$	is the signal path calculated according to 92.10.7.1.1
$S^{(CANXTk)}$	is the cable assembly near-end crosstalk path k
k	is 1 to 4 near-end crosstalk paths

$$SCHFXT_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOTxSP)}, S^{(CASFXTk)}), S^{(HOSP)}) \quad (92–33)$$

where

$SCHFXT_p^{(k)}$	is the channel far-end crosstalk path
$S^{(HOSP)}$	is the signal path calculated according to 92.10.7.1.1
$S^{(HOTxSP)}$	is the signal path calculated according to 92.10.7.1.1
$S^{(CAFXTk)}$	is the cable assembly far-end crosstalk path k
k	is 1 to 3 far-end crosstalk paths

92.11 Test fixtures

Transmitter and receiver measurements are made at TP2 or TP3 utilizing the test fixture specified in 92.11.1. and illustrated in Figure 92–15. All cable assembly measurements are to be made between TP1 and TP4 with cable assembly test fixtures as specified in 92.11.2 and illustrated in Figure 92–17. The test fixtures of Figure 92–15 and Figure 92–17 are specified in a mated state, illustrated in Figure 92–18, to enable connections to measurement equipment. The requirements in this subclause are not MDI connector specifications for an implemented design.

92.11.1 TP2 or TP3 test fixture

The test fixture (also known as Host Compliance Board) of Figure 92–15, or its equivalent, is required for measuring the transmitter specifications in 92.8.3 at TP2 and the receiver return loss at TP3. The TP2 and TP3 test points are illustrated in Figure 92–2. Figure 92–15 illustrates the test fixture attached to TP2 or TP3.

92.11.1.1 Test fixture return loss

The differential return loss, in dB, of the test fixture is specified in a mated state and shall meet the requirements of 92.11.3.2.

92.11.1.2 Test fixture insertion loss

The test fixture printed circuit board insertion loss values determined using Equation (92–34) shall be used as the reference test fixture insertion loss. The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the measurements.

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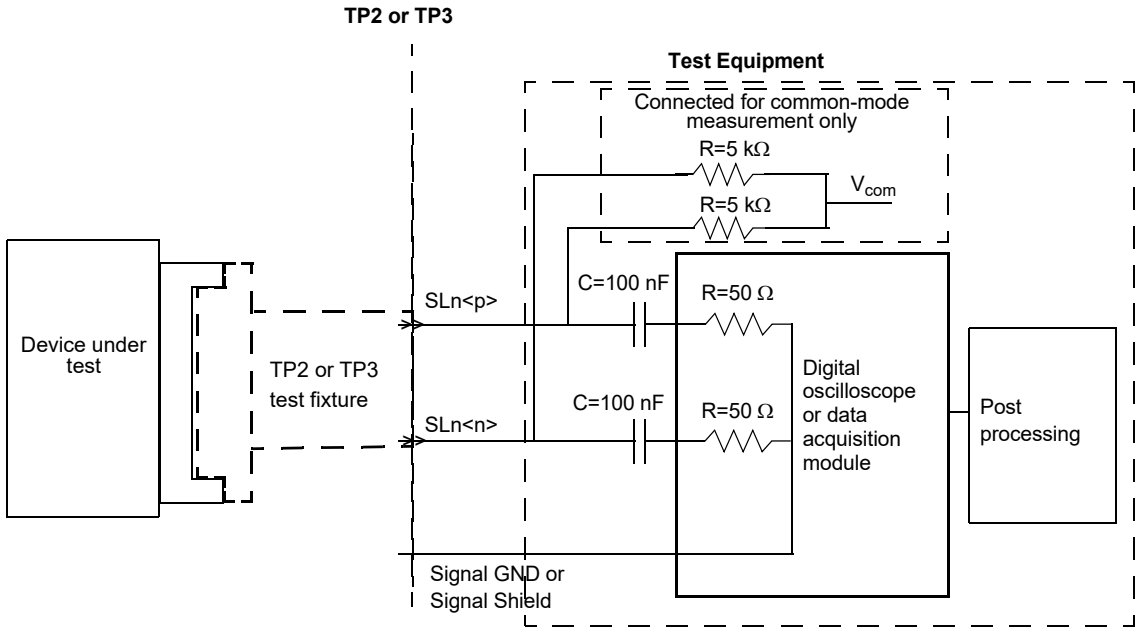

Figure 92–15—Transmitter and receiver test setup

$$IL_{tfref}(f) = -0.00144 + 0.13824\sqrt{f} + 0.06624\,f \quad \text{(dB)} \tag{92–34}$$

for $0.01 \le f \le 25$ GHz

where

f is the frequency in GHz

$IL_{tfref}(f)$ is the reference test fixture PCB insertion loss at frequency f

The reference test fixtures PCB insertion loss is illustrated in Figure 92–16.

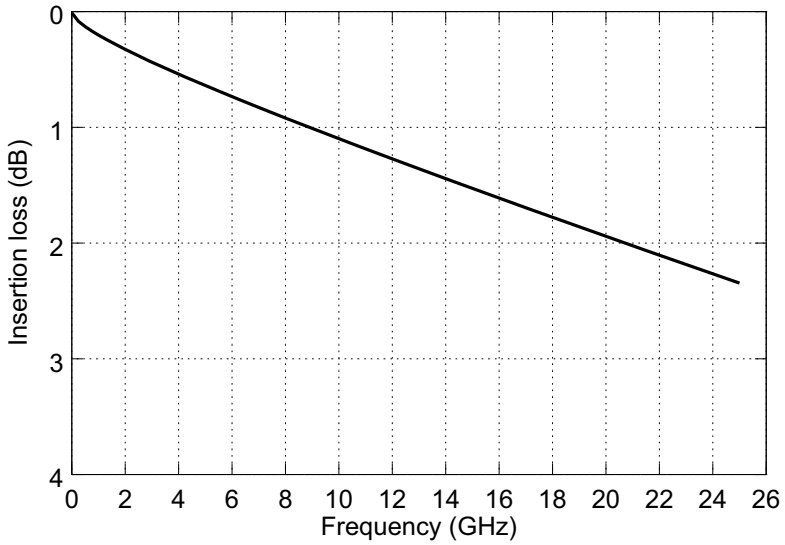

Figure 92–16—Reference test fixture insertion loss

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92.11.2 Cable assembly test fixture

The test fixture of Figure 92–17 (also known as Module Compliance Board) or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4. The TP1 and TP4 test points are illustrated in Figure 92–2 and Figure 92–17. The test fixture return loss is equivalent to the test fixture return loss specified in 92.11.3.2. The test fixture printed circuit board insertion loss values determined using Equation (92–35) shall be used as the reference test fixture insertion loss. The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the measurements.

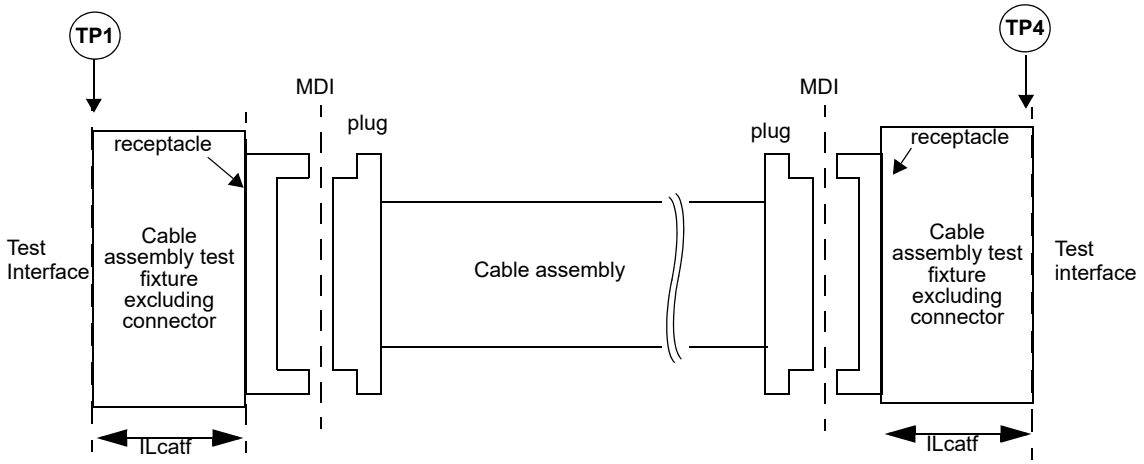

Figure 92–17—Cable assembly test fixtures

$$IL_{\mathrm{catf}}(f) = -0.00125 + 0.12\sqrt{f} + 0.0575f \quad \text{(dB)} \tag{92–35}$$

for $0.01\ \text{GHz} \le f \le 25\ \text{GHz}$

where

f is the frequency in GHz

$IL_{\mathrm{catf}}(f)$ is the reference test fixture printed circuit board insertion loss at frequency f

92.11.3 Mated test fixtures

The test fixtures of Figure 92–15 and Figure 92–17 are specified in a mated state illustrated in Figure 92–18. The mated test fixtures specifications shall be verified in both directions indicated by the arrows illustrated in Figure 92–18 except insertion loss, which shall be verified at either test interface illustrated in Figure 92–18.

92.11.3.1 Mated test fixtures insertion loss

The insertion loss of the mated test fixtures shall meet the values determined using Equation (92–36) and Equation (92–37).

$\mathrm{FOM_{ILD}}$ is calculated according to 93A.4 with f_b=25.78125 GHz, T_t=9.6 ps, and f_r=0.75 × f_b. The fitted insertion loss and insertion loss deviation are computed over the range $f_{\min}$=0.01 GHz to $f_{\max}$=25 GHz. $\mathrm{FOM_{ILD}}$ shall be less than 0.13 dB.

$$IL(f) \le IL_{\mathrm{MTFmax}}(f) = \left\{ \begin{array}{ll} 0.12 + 0.475\sqrt{f} + 0.221f & 0.01 \le f \le 14 \\ -4.25 + 0.66f & 14 < f \le 25 \end{array} \right\} \quad \text{(dB)} \tag{92–36}$$

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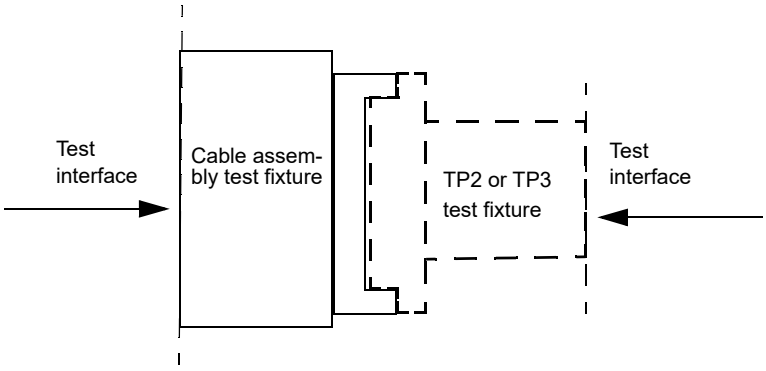

Figure 92–18—Mated test fixtures

$$IL(f) \geq IL_{\text{MTFmin}}(f) = 0.0656\sqrt{f} + 0.164f \quad 0.01 \leq f \leq 25 \quad \text{(dB)} \qquad (92\text{–}37)$$

where

f is the frequency in GHz

$IL(f)$ is the mated test fixture insertion loss at frequency f

The mated test fixtures insertion loss limits are illustrated in Figure 92–19.

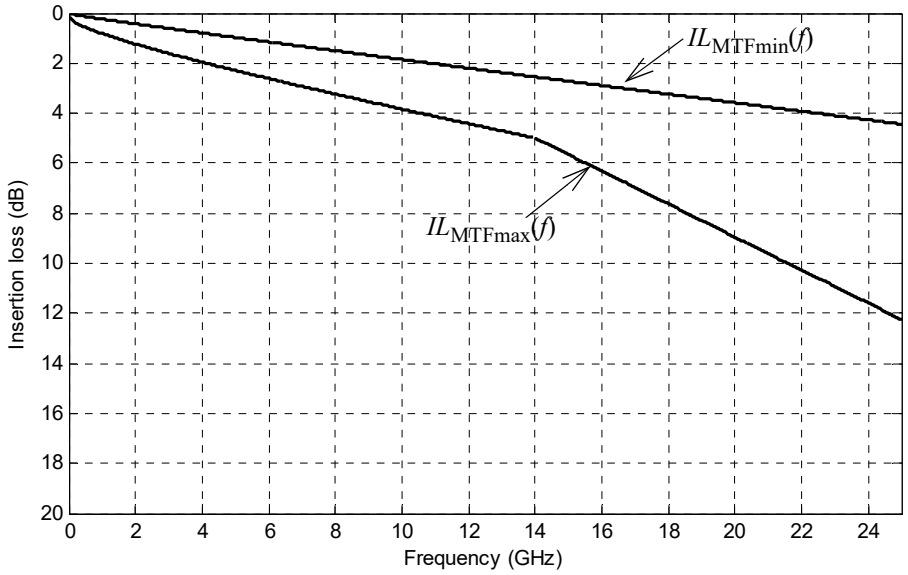

Figure 92–19—Mated test fixtures Insertion loss

92.11.3.2 Mated test fixtures return loss

The return loss of the mated test fixtures measured at each test fixture interface shall meet the values determined using Equation (92–38).

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$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 20 - f & 0.01 \leq f < 4 \\ 18 - 0.5f & 4 \leq f \leq 25 \end{array} \right\} \text{ (dB)} \quad (92\text{–}38)$$

where

f is the frequency in GHz

$Return\_loss(f)$ is the return loss at frequency f

The mated test fixtures return loss is illustrated in Figure 92–20.

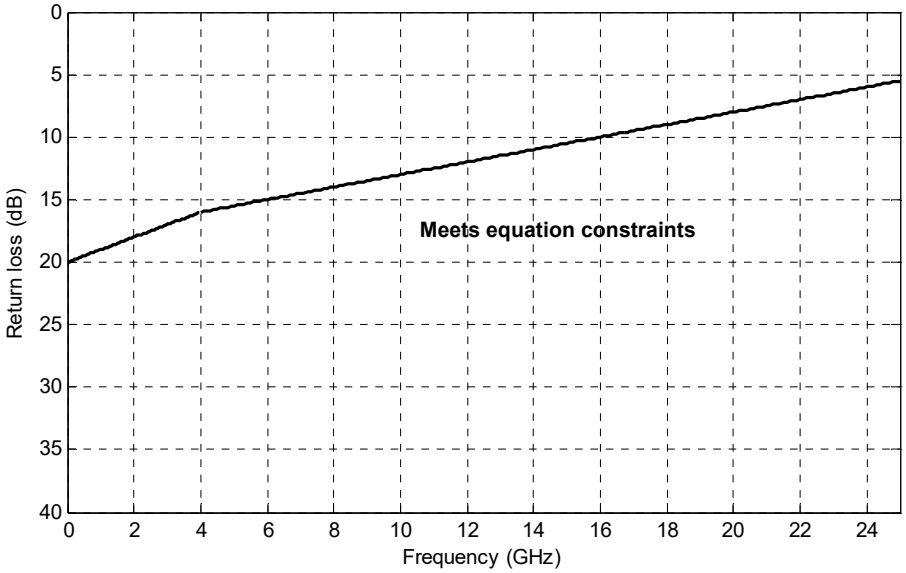

Figure 92–20—Mated test fixtures return loss

92.11.3.3 Mated test fixtures common-mode conversion insertion loss

The common-mode conversion insertion loss of the mated test fixtures measured at either test fixture test interface shall meet the values determined using Equation (92–39).

$$Conversion\_loss(f) \geq \left\{ \begin{array}{ll} 30 - (29/22)f & 0.01 \leq f < 16.5 \\ 8.25 & 16.5 \leq f \leq 25 \end{array} \right\} \text{ (dB)} \quad (92\text{–}39)$$

where

f is the frequency in GHz

$Conversion\_loss(f)$ is the conversion insertion loss at frequency f

The mated test fixtures common-mode conversion insertion loss is illustrated in Figure 92–21.

92.11.3.4 Mated test fixtures common-mode return loss

The common-mode return loss of the mated test fixtures measured at each test fixture test interface shall meet the values determined using Equation (92–40).

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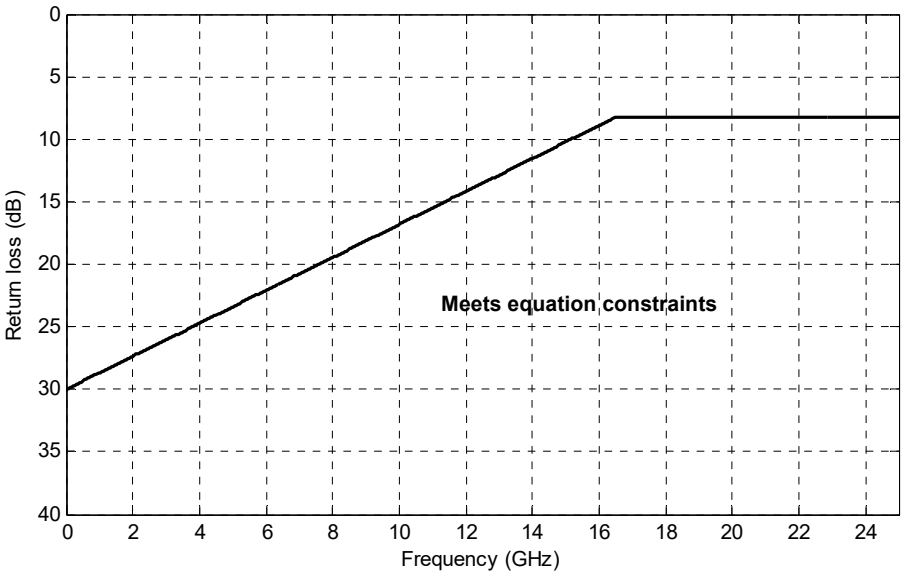

Figure 92–21—Common-mode conversion loss

$$Common\_mode\_return\_loss(f) \geq \begin{cases} 12 - 9f & 0.01 \leq f < 1 \\ 3 & 1 \leq f \leq 25 \end{cases} \quad \text{(dB)} \qquad (92\text{–}40)$$

where

f	is the frequency in GHz
$Common\_mode\_return\_loss(f)$	is the common-mode return loss at frequency f

The mated test fixtures common-mode return loss is illustrated in Figure 92–22.

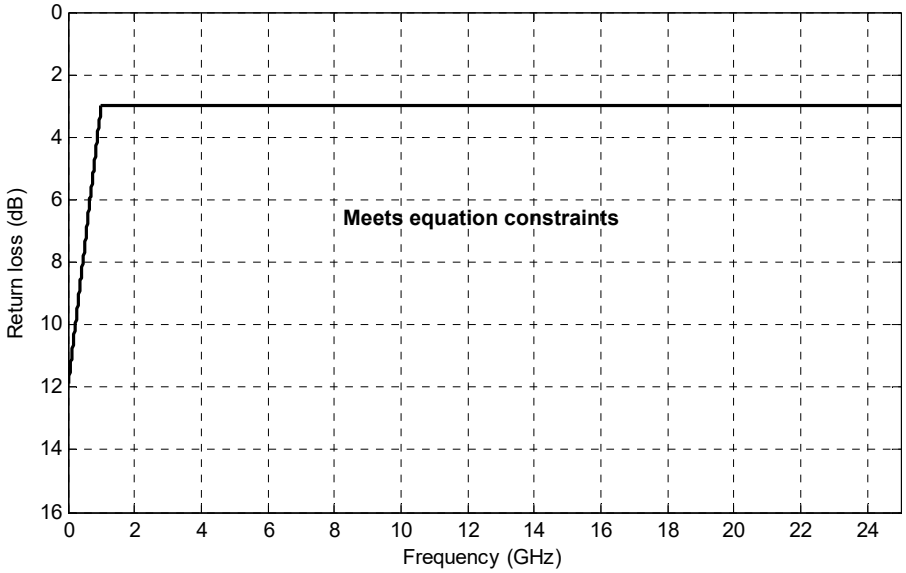

Figure 92–22—Common-mode return loss

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92.11.3.5 Mated test fixtures common-mode to differential mode return loss

The common-mode to differential mode return loss of the mated test fixtures measured at each test fixture test interface shall meet the values determined using Equation (92–41).

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 30 - (30/25.78)f & 0.01 \leq f < 12.89 \\ 18 - (6/25.78)f & 12.89 \leq f \leq 25 \end{array} \right\} \text{ (dB)} \quad (92–41)$$

where

f is the frequency in GHz

$Return\_loss(f)$ is the common-mode to differential mode return loss at frequency f

The mated test fixtures common-mode to differential mode return loss is illustrated in Figure 92–23.

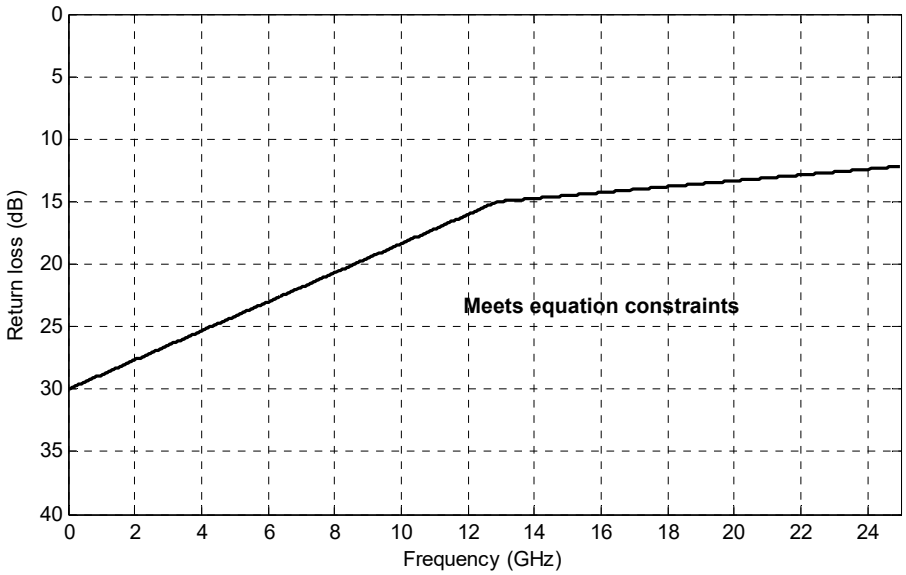

Figure 92–23—Common-mode to differential return loss

92.11.3.6 Mated test fixtures integrated crosstalk noise

The values of the mated test fixtures integrated crosstalk RMS noise voltages determined using Equation (92–44) through Equation (92–48) for the multiple disturber near-end crosstalk loss, and the multiple disturber far-end crosstalk loss shall meet the specifications in Table 92–13.

Table 92–13—Mated test fixtures integrated crosstalk noise

Parameter	100GBASE-CR4	Units
MDNEXT integrated crosstalk noise voltage	Less than 1.8	mV
MDFEXT integrated crosstalk noise voltage	Less than 4.8	mV

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92.11.3.6.1 Mated test fixture multiple disturber near-end crosstalk (MDNEXT) loss

Since four lanes are used to transfer data between PMDs, the NEXT that is coupled into a receive lane is from the four transmit lanes. Multiple Disturber Near-End Crosstalk (MDNEXT) loss is determined using the individual NEXT losses.

MDNEXT loss is determined from the four individual pair-to-pair differential NEXT loss values using Equation (92–42).

$$MDNEXT\_loss(f) = -10\log_{10}\left(\sum_{i=0}^{i=3} 10^{-NLi(f)/10}\right) \quad \text{(dB)} \tag{92–42}$$

for 0.05 GHz ≤ f ≤ 19 GHz

where

$MDNEXT\_loss(f)$	is the MDNEXT loss at frequency f
$NL_i(f)$	is the NEXT loss at frequency f of pair combination i, in dB
f	is the frequency in GHz
i	is the 0 to 3 (pair-to-pair combination)

92.11.3.6.2 Mated test fixture multiple disturber far-end crosstalk (MDFEXT) loss

Since four lanes are used to transfer data between PMDs, the FEXT that is coupled into a data carrying lane is from the three other lanes in the same direction. MDFEXT loss is specified using the individual FEXT losses. MDFEXT loss is determined from the three individual pair-to-pair differential FEXT loss values using Equation (92–43).

$$MDFEXT\_loss(f) = -10\log_{10}\left(\sum_{i=0}^{i=2} 10^{-NLi(f)/10}\right) \quad \text{(dB)} \tag{92–43}$$

for 0.05 GHz ≤ f ≤ 19 GHz

where

$MDFEXT\_loss(f)$	is the MDFEXT loss at frequency f
$NL_i(f)$	is the FEXT loss at frequency f of pair combination i, in dB
f	is the frequency in GHz
i	is the 0 to 2 (pair-to-pair combination)

92.11.3.6.3 Mated test fixture integrated crosstalk noise (ICN)

ICN is calculated from the MDFEXT and MDNEXT. Given the multiple disturber near-end crosstalk loss $MDNEXT\_loss(f)$ and multiple disturber far-end crosstalk loss $MDFEXT\_loss(f)$ measured over N uniformly-spaced frequencies f_n spanning the frequency range 50 MHz to 19 000 MHz with a maximum frequency spacing of 10 MHz, the RMS value of the integrated crosstalk noise is determined using Equation (92–44) through Equation (92–48). The RMS crosstalk noise is characterized at the output of a specified receive filter utilizing a specified transmitter waveform and the measured multiple disturber crosstalk transfer functions. The transmitter and receiver filters are defined in Equation (92–44) and Equation (92–45) as weighting functions to the multiple disturber crosstalk in Equation (92–46) and Equation (92–47). The sinc function is defined by $\text{sinc}(x) = \sin(\pi x)/(\pi x)$.

Define the weight at each frequency f_n using Equation (92–44) and Equation (92–45).

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$$W_{nt}(f_n) = (A_{nt}^2/f_b)\mathrm{sinc}^2(f_n/f_b)\left[\frac{1}{1+(f_n/f_{nt})^4}\right]\left[\frac{1}{1+(f_n/f_r)^8}\right] \quad (92–44)$$

$$W_{ft}(f_n) = (A_{ft}^2/f_b)\mathrm{sinc}^2(f_n/f_b)\left[\frac{1}{1+(f_n/f_{ft})^4}\right]\left[\frac{1}{1+(f_n/f_r)^8}\right] \quad (92–45)$$

where the equation parameters are given in Table 92–14.

Note that the 3 dB transmit filter bandwidths f_{nt} and f_{ft} are inversely proportional to the 20% to 80% rise and fall times T_{nt} and T_{ft} respectively. The constant of proportionality is 0.2365 (e.g., $T_{nt}f_{nt} = 0.2365$; with f_{nt} in hertz and T_{nt} in seconds). In addition, f_r is the 3 dB reference receiver bandwidth, which is set to 18.75 GHz.

The near-end integrated crosstalk noise σ_{nx} is calculated using Equation (92–46).

$$\sigma_{nx} = \left[2\Delta f\sum_n W_{nt}(f_n)10^{-MDNEXT_{loss}(f_n)/10}\right]^{1/2} \quad (92–46)$$

The far-end integrated crosstalk noise σ_{fx} is calculated using Equation (92–47).

$$\sigma_{fx} = \left[2\Delta f\sum_n W_{ft}(f_n)10^{-MDFEXT_{loss}(f_n)/10}\right]^{1/2} \quad (92–47)$$

where Δf is the uniform frequency step of f_n.

The total integrated crosstalk noise σ_x is calculated using Equation (92–48).

$$\sigma_x = \sqrt{\sigma_{nx}^2 + \sigma_{fx}^2} \quad (92–48)$$

The total integrated crosstalk noise for the mated test fixture is computed using the parameters shown in Table 92–14.

Table 92–14—Mated test fixture integrated crosstalk noise parameters

Description	Symbol	Value	Units
Symbol rate	f_b	25.78125	GBd
Near-end disturber peak differential output amplitude	A_{nt}	600	mV
Far-end disturber peak differential output amplitude	A_{ft}	600	mV
Near-end disturber 20% to 80% rise and fall times	T_{nt}	9.6	ps
Far-end disturber 20% to 80% rise and fall times	T_{ft}	9.6	ps

92.12 MDI specification

This subclause defines the Media Dependent Interface (MDI). The 100GBASE-CR4 PMD, as per 92.7, is coupled to the cable assembly, as per 92.10, by the MDI.

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92.12.1 100GBASE-CR4 MDI connectors

Connectors meeting the requirements of 92.12.1.1 (Style-1) or 92.12.1.2 (Style-2) are used as the mechanical interface between the PMD of 92.7 and the cable assembly of 92.10. The plug connector is used on the cable assembly and the receptacle on the PHY. Style-1 or Style-2 connectors may be used as the MDI.

For Style-1 and Style-2 100GBASE-CR4 plug connectors, the receive lanes are AC-coupled; the AC-coupling shall be within the plug connectors. It should be noted that there may be various methods for AC-coupling in actual implementations. The low-frequency 3 dB cutoff of the AC-coupling shall be less than 50 kHz. It is recommended that the value of the coupling capacitors be 100 nF. The capacitor limits the inrush charge and baseline wander.

92.12.1.1 Style-1 100GBASE-CR4 MDI connectors

The plug connector for each end of the cable assembly shall be the QSFP+ 28 Gb/s 4X Pluggable (QSFP28) plugs defined in SFF-8665 and illustrated in Figure 92–24. The MDI connector shall be the QSFP+ 28 Gb/s 4X Pluggable (QSFP28) receptacle with the mechanical mating interface defined in SFF-8665 and illustrated in Figure 92–25. These connectors have contact assignments that are listed in Table 92–15 and electrical performance consistent with the signal quality and electrical requirements of 92.8 and 92.9.

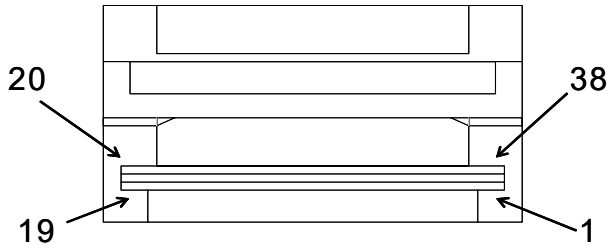

Figure 92–24—Style-1 example cable assembly

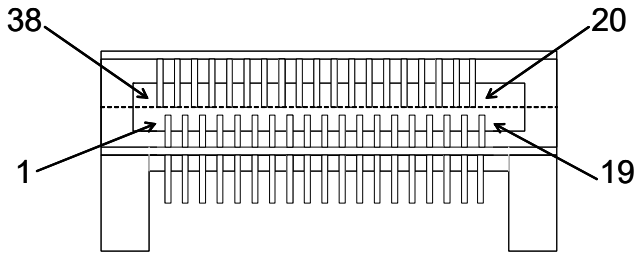

Figure 92–25—Style-1 example MDI board receptacle

The Style-1 MDI connector of the 100GBASE-CR4 PMD comprises 38 signal connections. The Style-1 100GBASE-CR4 MDI connector contact assignments shall be as defined in Table 92–15.

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Table 92–15—100GBASE-CR4 lane to MDI connector contact mapping

Tx lane	MDI connector contact	Rx lane	MDI connector contact
signal gnd	S1	signal gnd	S13
SL1<n>	S2	DL2<p>	S14
SL1<p>	S3	DL2<n>	S15
signal gnd	S4	signal gnd	S16
SL3<n>	S5	DL0<p>	S17
SL3<p>	S6	DL0<n>	S18
signal gnd	S7	signal gnd	S19
signal gnd	S32	signal gnd	S20
SL2<p>	S33	DL1<n>	S21
SL2<n>	S34	DL1<p>	S22
signal gnd	S35	signal gnd	S23
SL0<p>	S36	DL3<n>	S24
SL0<n>	S37	DL3<p>	S25
signal gnd	S38	signal gnd	S26

92.12.1.2 Style-2 100GBASE-CR4 MDI connectors

The connector for each end of the cable assembly shall be the 100G Form Factor Pluggable 4 (CFP4) with the mechanical mating interface defined in CFP4 MSA HW Specification and illustrated in Figure 92–26. The MDI connector shall be the 100G Form Factor Pluggable (CFP4) receptacle with the mechanical mating interface defined by CFP4 MSA HW Specification and illustrated in Figure 92–27. These connectors have contact assignments that are listed in Table 92–16, and electrical performance consistent with the signal quality and electrical requirements of 92.8 and 92.9.

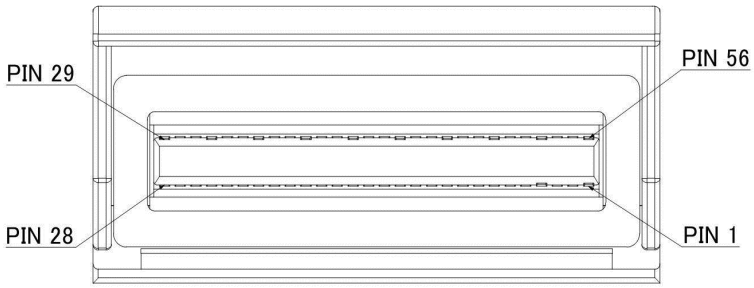

Figure 92–26—Style-2 example cable assembly

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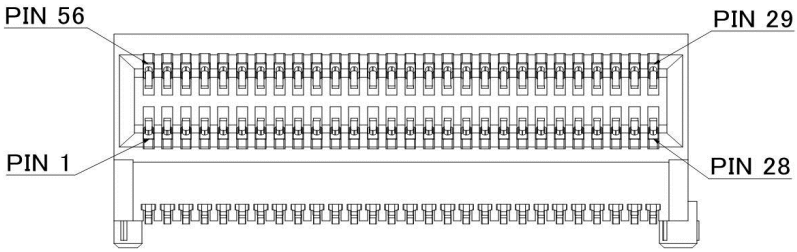

Figure 92–27—Style-2 example MDI board receptacle

The Style-2 MDI connector of the 100GBASE-CR4 PMD comprises 56 signal connections. The Style-2 100GBASE-CR4 MDI connector contact assignments shall be as defined in Table 92–16. Note that the source lanes (SL), signals SLi<p>, and SLi<n> are the positive and negative sides of the transmitters differential signal pairs and the destination lanes (DL) signals, DLi<p>, and DLi<n> are the positive and negative sides of the receivers differential signal pairs for lane i (i = 0, 1, 2, 3).

Table 92–16—100GBASE-CR4 lane to MDI connector contact mapping

Tx lanes	MDI connector contact	Rx lanes	MDI connector contact
signal gnd	44	signal gnd	29
SL0<p>	45	DL0<p>	30
SL0<n>	46	DL0<n>	31
signal gnd	47	signal gnd	32
SL1<p>	48	DL1<p>	33
SL1<n>	49	DL1<n>	34
signal gnd	50	signal gnd	35
SL2<p>	51	DL2<p>	36
SL2<n>	52	DL2<n>	37
signal gnd	53	signal gnd	38
SL3<p>	54	DL3<p>	39
SL3<n>	55	DL3<n>	40
signal gnd	56	signal gnd	41

92.13 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 14.7.

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92.14 Protocol implementation conformance statement (PICS) proforma for Clause 92, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR4[161]

92.14.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 92, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

92.14.2 Identification

92.14.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

92.14.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 92, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[161] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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92.14.3 Major capabilities/options

Item[a]	Feature	Subclause	Value/Comment	Status	Support
CGMII	CGMII	92.1	Interface is supported	O	Yes [ ] No [ ]
PCS	100GBASE-R PCS	92.1		M	Yes [ ]
RS-FEC	100GBASE-R RS-FEC	92.1		M	Yes [ ]
PMA	100GBASE-R PMA	92.1		M	Yes [ ]
CAUI-10	CAUI-10	92.1	Interface is supported	O	Yes [ ] No [ ]
CAUI-4	CAUI-4	92.1	Interface is supported	O	Yes [ ] No [ ]
CR4	100GBASE-CR4 PMD	92.1	Can operate as 100GBASE-CR4 PMD	M	Yes [ ]
AN	Auto-negotiation	92.1	Device implements Auto-Negotiation	M	Yes [ ]
DC	Delay constraints	92.4	Device conforms to delay constraints specified in 92.4	M	Yes [ ]
DSC	Skew constraints	92.5	Device conforms to Skew and Skew Variation constraints specified in 92.5	M	Yes [ ]
*MD	MDIO capability	92.6	Registers and interface supported	O	Yes [ ] No [ ]
*EEE	EEE deep sleep capability	92.1	Capability is supported	O	Yes [ ] No [ ]
*GTD	Global PMD transmit disable function	92.7.6	Function is supported	EEE:M	Yes [ ] N/A [ ]
*LTD	PMD lane-by-lane transmit disable function	92.7.7	Function is supported	O	Yes [ ] No [ ]
*CBL	Cable assembly	92.10	Items marked with CBL include cable assembly specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
CAST1	100GBASE-CR4 Style-1 cable assembly	92.10	Cable assembly supports 100GBASE-CR4 Style-1	CBL:O.1	Yes [ ] No [ ] N/A [ ]
CAST2	100GBASE-CR4 Style-2 cable assembly	92.10	Cable assembly supports 100GBASE-CR4 Style-2	CBL:O.1	Yes [ ] No [ ] N/A [ ]
MDIST1	Style-1 MDI connector	92.12.1.1	100GBASE-CR4 device uses Style-1 MDI	O:2	Yes [ ] No [ ]
MDIST2	Style-2 MDI connector	92.12.1.2	100GBASE-CR4 device uses Style-2 MDI	O:2	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

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92.14.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR4

92.14.4.1 PMD functional specifications

Item	Feature	Sub-clause	Value/Comment	Status	Support
PF1	Transmit function	92.7.2	Converts four logical bit streams from the PMD service interface into four electrical signals and delivers them to the MDI	M	Yes [ ]
PF2	Transmitter signal	92.7.2	A positive differential voltage corresponds to tx_bit = one	M	Yes [ ]
PF3	ALERT signal	92.7.2	Transmit a periodic sequence, where each period of the sequence consists of 8 ones followed by 8 zeros, on each lane when tx_mode is set to ALERT	EEE:M	Yes [ ] N/A [ ]
PF4	Receive function	92.7.3	Converts four electrical signals from the MDI into four logical bit streams delivers them to the PMD service interface	M	Yes [ ]
PF5	Receiver signal	92.7.3	A positive differential voltage corresponds to rx_bit = one	M	Yes [ ]
PF6	Training disabled by management	92.7.5	PMD_signal_detect_*i* set to one for *i*=0 to 3	M	Yes [ ]
PF7	PMD_signal_detect_*i* asserted, rx_mode=QUIET	92.7.5	Set to one within 500 ns following the application of the signal defined in 92.7.5 to the input of the channel corresponding to the receiver of lane *i*	EEE:M	Yes [ ] N/A [ ]
PF8	PMD_signal_detect_*i* not asserted, rx_mode=QUIET	92.7.5	Not set to one when the signal applied to the input of the channel corresponding to the receiver of lane *i* is less than or equal to 70 mV peak-to-peak differential	EEE:M	Yes [ ] N/A [ ]
PF9	Global_PMD_transmit_disable	92.7.6	Disables all transmitters by forcing a constant output level	GTD:M	Yes [ ] N/A [ ]
PF10	Global_PMD_transmit_disable affect on loopback	92.7.6	No effect	GTD:M	Yes [ ] N/A [ ]
PF11	Global PMD transmit disable function, tx_mode transition to QUIET	92.7.6	Turn off all transmitters when tx_mode transitions to QUIET from any other value	EEE:M	Yes [ ] N/A [ ]
PF12	Global PMD transmit disable function, tx_mode transition from QUIET	92.7.6	Turn on all transmitters when tx_mode transitions from QUIET to any other value	EEE:M	Yes [ ] N/A [ ]
PF13	PMD_transmit_disable_*i* variable	92.7.7	When set to one, the transmitter for lane *i* satisfies the requirements of Table 92–6	LTD:M	Yes [ ] N/A [ ]

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Item	Feature	Sub-clause	Value/Comment	Status	Support
PF14	PMD lane-by-lane transmit disable function affect on loopback	92.7.7	No effect	LTD:M	Yes [ ] N/A [ ]
PF15	PMD_fault variable mapping to MDIO	92.7.9	Mapped to the fault bit as specified in 45.2.1.2.3	MD:M	Yes [ ] N/A [ ]
PF16	PMD_transmit_fault variable mapping to MDIO	92.7.10	Mapped to Transmit fault bit as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
PF17	PMD_receive_fault variable mapping to MDIO	92.7.11	Mapped to Receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]
PF18	PMD control function	92.7.12	Each lane uses the same control function as 10GBASE-KR, as defined in 72.6.10	M	Yes [ ]
PF19	PMD control response time	92.7.12	Response time less than 2 ms.	M	Yes [ ]
PF20	Training frame structure	92.7.12	Defined in 72.6.10 but adjusted for 100GBASE-CR4 signaling rate and use of uncorrelated training patterns	M	Yes [ ]
PF21	Training pattern	92.7.12	4094 bits from the output of a pseudo-random bit sequence (PRBS) generator defined in Table 92–5 followed by two zeros	M	Yes [ ]
PF22	Training pattern seed	92.7.12	Set to the value in Table 92–5 at the start of the training pattern	M	Yes [ ]
PF23	PMD control function variable mapping	92.7.12	Map variables to the appropriate bits as specified in 45.2.1.96	MD:M	Yes [ ] N/A [ ]

92.14.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Global_PMD_signal_detect	92.7.4	Set to the value described in 45.2.1.9.7	O	Yes [ ] No [ ]
MF2	Global_PMD_signal_detect	92.7.4	Set defined by the training state diagram in Figure 72–5	O	Yes [ ] No [ ]
MF3	Lane-by-Lane Signal Detect function	92.7.5	Sets PMD_signal_detect_n values on a lane-by-lane basis per requirements of 92.7.5	MD:M	Yes [ ] N/A [ ]
MF4	Lane-by-Lane Signal Detect function	92.7.5	If training is disabled by management, PMD_signal_-detect_*i* is set to one for i=0 to 3.	MD:M	Yes [ ] N/A [ ]
MF5	Lane-by-Lane Signal Detect function	92.7.5	Apply EEE requirements as specified in 92.7.5	EEE:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MF6	Global_PMD_transmit_disable	92.7.6	Apply EEE requirements as specified in 92.7.6.	EEE:M	Yes [ ] N/A [ ]
MF7	PMD_fault function	92.7.9	Mapped to the fault bit as specified in 45.2.1.2.3	MD:M	Yes [ ] N/A [ ]
MF8	PMD_transmit_fault function	92.7.10	Mapped to the PMD_transmit_fault bit as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
MF9	PMD_receive_fault function	92.7.11	Contributes to the PMA/PMD receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]

92.14.4.3 Transmitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Test fixture return loss	92.11.1.1	Meets equation constraints	M	Yes [ ]
TC2	Test fixture insertion loss	92.11.1.2	Meets equation constraints	M	Yes [ ]
TC3	Signaling rate per lane	92.8.3.9	25.78125 GBd ± 100 ppm	M	Yes [ ]
TC4	Peak-to-peak differential output voltage	92.8.3.1	Less than or equal to 1200 mV regardless of transmit equalizer setting	M	Yes [ ]
TC5	Peak-to-peak differential output voltage, transmitter disabled	92.8.3.1	Less than or equal to 35 mV	M	Yes [ ]
TC6	DC common-mode output voltage	92.8.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC7	AC common-mode output voltage	92.8.3.1	Less than or equal to 30 mV RMS with respect to signal ground	M	Yes [ ]
TC8	The peak-to-peak differential output voltage	92.8.3.1	Less than 30 mV within 500 ns of the transmitter being disabled.	EEE:M	Yes [ ] N/A [ ]
TC9	The peak-to-peak differential output voltage	92.8.3.1	Greater than 720 mV within 500 ns of the transmitter being enabled	EEE:M	Yes [ ] N/A [ ]
TC10	The peak-to-peak differential output voltage	92.8.3.1	Meets the requirements of 92.8.3 within 1 μs of the transmitter being enabled.	EEE:M	Yes [ ] N/A [ ]
TC11	DC common-mode output voltage while the transmitter is disabled.	92.8.3.1	Maintained to within ±150 mV of the value for the enabled transmitter.	EEE:M	Yes [ ] N/A [ ]
TC12	Common-mode output voltage requirements	92.8.3.1	Met regardless of the transmit equalizer setting	M	Yes [ ]
TC13	Differential output return loss (min)	92.8.3.2	Meets equation constraints	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC14	Reference impedance for differential return loss measurements	92.8.3.2	100 Ω	M	Yes [ ]
TC15	Common-mode to differential mode output return loss	92.8.3.3	Meets equation constraints	M	Yes [ ]
TC16	Steady-state voltage, v_f	92.8.3.5.2	0.34 min, 0.6 max	M	Yes [ ]
TC17	Linear fit pulse peak (min)	92.8.3.5.2	$0.45 \times v_f$	M	Yes [ ]
TC18	Coefficient initialization	92.8.3.5.3	Satisfies the requirements of 92.8.3.5.3.	M	Yes [ ]
TC19	Normalized coefficient step size for “increment”	92.8.3.5.4	Between 0.0083 and 0.05	M	Yes [ ]
TC20	Normalized coefficient step size for “decrement”	92.8.3.5.4	Between –0.05 and –0.0083	M	Yes [ ]
TC21	Maximum post-cursor equalization ratio	92.8.3.5.5	Greater than or equal to 4	M	Yes [ ]
TC22	Maximum pre-cursor equalization ratio	92.8.3.5.5	Greater than or equal to 1.54	M	Yes [ ]
TC23	Transmitter output SNDR	92.8.3.7	Greater than or equal to 26 dB regardless of the transmit equalization setting	M	Yes [ ]
TC24	Even-odd jitter	92.8.3.8.1	Less than or equal to 0.035 UI regardless of the transmit equalization setting	M	Yes [ ]
TC25	Effective bounded uncorrelated jitter	92.8.3.8.2	Less than or equal to 0.1 UI peak-to-peak regardless of the transmit equalization setting	M	Yes [ ]
TC26	Effective total uncorrelated jitter	92.8.3.8.2	Less than or equal to 0.18 UI RMS regardless of the transmit equalization setting	M	Yes [ ]

92.14.4.4 Receiver specifications

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Test fixture return loss	92.11.1.1	Meets the requirements of 92.11.3.2	M	Yes [ ]
RC2	Test fixture insertion loss	92.11.1.2	Meets equation constraints	M	Yes [ ]
RC3	Receiver input amplitude tolerance	92.8.4.1	1200 mV measured at TP2	M	Yes [ ]
RC4	Differential input return loss	92.8.4.2	Meets equation constraints	M	Yes [ ]
RC5	Reference impedance for differential return loss measurements	92.8.4.2	100 Ω	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RC6	Common-mode input return loss	92.8.4.3	Meets equation constraints	M	Yes [ ]
RC7	Interference tolerance	92.8.4.4	Satisfy requirements summarized in Table 92–8	M	Yes [ ]
RC8	Interference tolerance	92.8.4.4.4	Pattern generator output amplitude	M	Yes [ ]
RC9	Interference tolerance	92.8.4.4.4	Pattern generator jitter specification	M	Yes [ ]
RC10	Receiver jitter tolerance for each lane	92.8.4.5	The RS-FEC symbol error ratio less than or equal to 10^{-4} for each test case	M	Yes [ ]
RC11	Signaling rate, per lane	92.8.4.6	25.78125 GBd ± 100 ppm	M	Yes [ ]

92.14.4.5 Cable assembly specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CA1	Differential reference impedance	92.10.1	100 Ω	CBL:M	Yes [ ] N/A [ ]
CA2	Minimum insertion loss	92.10.2	Per Equation (92–26)	CBL:M	Yes [ ] N/A [ ]
CA3	Maximum insertion loss	92.10.2	Less than or equal to 22.48 dB at 12.8906 GHz.	CBL:M	Yes [ ] N/A [ ]
CA4	Return loss	92.10.3	Per Equation (92–27)	CBL:M	Yes [ ] N/A [ ]
CA5	Differential to common-mode input and output return loss	92.10.4	Per Equation (92–28)	CBL:M	Yes [ ] N/A [ ]
CA6	Differential to common-mode conversion loss	92.10.5	Per Equation (92–29)	CBL:M	Yes [ ] N/A [ ]
CA7	Common-mode to common-mode return loss	92.10.6	Per Equation (92–30)	CBL:M	Yes [ ] N/A [ ]
CA8	Cable assembly Channel Operating Margin (COM)	92.10.7	Greater than 3 dB	CBL:M	Yes [ ] N/A [ ]
CA9	Test fixture reference printed circuit board insertion loss	92.11.2	Per Equation (92–35)	CBL:M	Yes [ ] N/A [ ]
CA10	Mated test fixture specifications	92.11.3	Verified in both directions illustrated in Figure 92–18 except insertion loss verified at either test interface in directions illustrated in Figure 92–18.	CBL:M	Yes [ ] N/A [ ]
CA11	Mated test fixture insertion loss	92.11.3.1	Per Equation (92–36) and Equation (92–37)	CBL:M	Yes [ ] N/A [ ]
CA12	Mated test fixture RMS insertion loss deviation	92.11.3.1	Less than 0.13 dB	CBL:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
CA13	Mated test fixture return loss	92.11.3.2	Per Equation (92–38)	CBL:M	Yes [ ] N/A [ ]
CA14	Mated test fixture common-mode conversion loss	92.11.3.3	Per Equation (92–39)	CBL:M	Yes [ ] N/A [ ]
CA15	Mated test fixture common-mode return loss	92.11.3.4	Per Equation (92–40)	CBL:M	Yes [ ] N/A [ ]
CA16	Mated test fixture common-mode to differential mode return loss	92.11.3.5	Per Equation (92–41)	CBL:M	Yes [ ] N/A [ ]
CA17	Mated test fixtures integrated crosstalk noise	92.11.3.6	Per Equation (92–44), through Equation (92–48) and Table 92–13	CBL:M	Yes [ ] N/A [ ]
CA18	Cable assembly connector type	92.12.1.1	100GBASE-CR4 Style-1 plug (SFF-8665 plug)	CAST1:M	Yes [ ] N/A [ ]
CA19	Pin assignments	92.12.1.1	Per Table 92–15	CAST1:M	Yes [ ] N/A [ ]
CA20	Cable assembly connector type	92.12.1.2	100GBASE-CR4 Style-2 plug (CFP4)	CAST2:M	Yes [ ] N/A [ ]
CA21	Pin assignments	92.12.1.2	Per Table 92–16	CAST2:M	Yes [ ] N/A [ ]
CA22	AC-coupling	92.12.1	3 dB cutoff	CBL:M	Yes [ ] N/A [ ]

92.14.4.6 MDI connector specifications

Item	Feature	Subclause	Value/Comment	Status	Support
MDC1	MDI connector type	92.12.1.1	100GBASE-CR4 Style-1 receptacle (SFF-8665 receptacle)	MDIST1:M	Yes [ ] N/A [ ]
MDC2	MDI connector type	92.12.1.2	100GBASE-CR4 Style-2 receptacle (CFP4 receptacle)	MDIST2:M	Yes [ ] N/A [ ]

92.14.4.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Environmental specifications	92.13		M	Yes [ ]

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93. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR4

93.1 Overview

This clause specifies the 100GBASE-KR4 PMD and baseband medium. There are three associated annexes. Annex 93A defines characteristics of electrical backplanes, Annex 93B extends the electrical backplane reference model with additional informative test points, and Annex 93C defines the test method for receiver interference tolerance.

When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 93–1, to the medium through the MDI and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 93–1—Physical Layer clauses associated with the 100GBASE-KR4 PMD

Associated clause	100GBASE-KR4
81—RS	Required
81—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R[b]	Required
83A—CAUI-10	Optional
83D—CAUI-4	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation behaves functionally as though the RS and CGMII were present.
[b]There are limitations on the number of PMA lanes that may be used between sublayers, see 83.3.

A 100GBASE-KR4 PHY with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization.

Figure 93–1 shows the relationship of the 100GBASE-KR4 PMD sublayer and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.

The receive path of the RS-FEC sublayer may have the option to perform error detection without correction to reduce the data delay (see 91.5.3.3). When the receive path of the RS-FEC sublayer performs error correction, the link is required to operate with a BER of 10^{-5} or better. When the RS-FEC sublayer is configured to bypass error correction, the link is required to operate with a BER of 10^{-12} or better. In this context, a link consists of a compliant PMD transmitter, a compliant PMD receiver, and a channel meeting the requirements of 93.9.1.

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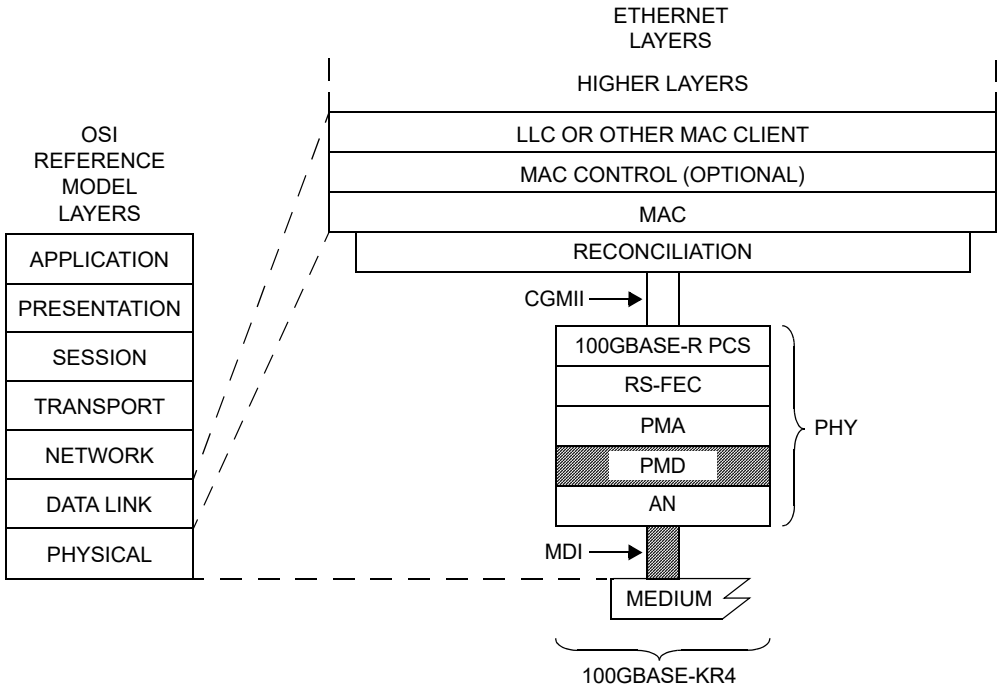

Figure 93–1—100GBASE-KR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

For a complete Physical Layer, this specification is considered to be satisfied by a frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap.

93.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-KR4 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data. The PMD translates the encoded data to and from signals suitable for the medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

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The 100GBASE-KR4 PMD has four parallel bit streams, hence *i* = 0 to 3. The PMA (or the PMD) continuously sends four parallel bit streams to the PMD (or the PMA), one per lane, each at a nominal signaling rate of 25.78125 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable Global_PMD_signal_detect as defined in 93.7.4. When Global_PMD_signal_detect is one, SIGNAL_OK shall be assigned the value OK. When Global_PMD_signal_detect is zero, SIGNAL_OK shall be assigned the value FAIL. When SIGNAL_OK is FAIL, the PMD:IS_UNITDATA_*i*.indication parameters are undefined.

If the optional EEE deep sleep capability is supported, then the PMD service interface includes two additional primitives as follows:

PMD:IS_TX_MODE.request
PMD:IS_RX_MODE.request

93.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 82.6.)

The 100GBASE-KR4 PHY may be extended using CAUI-n as a physical instantiation of the inter-sublayer service interface between devices. If CAUI-n is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementer. As examples, the implementer may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

93.4 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the 100GBASE-KR4 PMD, AN, and the medium in one direction shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns). It is assumed that the one way delay through the medium is no more than 800 bit times (8 ns).

A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

93.5 Skew constraints

The Skew (relative delay) between the lanes is kept within limits so that the information on the lanes can be reassembled by the RS-FEC sublayer. Skew and Skew Variation are defined in 80.5 and specified at the points SP1 to SP6 shown in Figure 80–9.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

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If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5.

93.6 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control bits to PMD control variables as shown in Table 93–2, and MDIO status bits to PMD status variables as shown in Table 93–3.

Table 93–2—100GBASE-KR4 MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 3 to PMD transmit disable 0	PMD transmit disable	1.9.4 to 1.9.1	PMD_transmit_disable_3 to PMD_transmit_disable_0
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable
Polynomial identifier 3	PMD training pattern 3	1.1453.12:11	identifier_3
Seed 3	PMD training pattern 3	1.1453.10:0	seed_3
Polynomial identifier 2	PMD training pattern 2	1.1452.12:11	identifier_2
Seed 2	PMD training pattern 2	1.1452.10:0	seed_2
Polynomial identifier 1	PMD training pattern 1	1.1451.12:11	identifier_1
Seed 1	PMD training pattern 1	1.1451.10:0	seed_1
Polynomial identifier 0	PMD training pattern 0	1.1450.12:11	identifier_0
Seed 0	PMD training pattern 0	1.1450.10:0	seed_0

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Table 93–3—100GBASE-KR4 MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 0	PMD receive signal detect	1.10.4 to 1.10.1	PMD_signal_detect_3 to PMD_signal_detect_0
100GBASE-KR4 deep sleep	EEE capability	1.16.10	—
Receiver status 3	BASE-R PMD status	1.151.12	rx_trained_3
Frame lock 3	BASE-R PMD status	1.151.13	frame_lock_3
Startup protocol status 3	BASE-R PMD status	1.151.14	training_3
Training failure 3	BASE-R PMD status	1.151.15	training_failure_3
Receiver status 2	BASE-R PMD status	1.151.8	rx_trained_2
Frame lock 2	BASE-R PMD status	1.151.9	frame_lock_2
Startup protocol status 2	BASE-R PMD status	1.151.10	training_2
Training failure 2	BASE-R PMD status	1.151.11	training_failure_2
Receiver status 1	BASE-R PMD status	1.151.4	rx_trained_1
Frame lock 1	BASE-R PMD status	1.151.5	frame_lock_1
Startup protocol status 1	BASE-R PMD status	1.151.6	training_1
Training failure 1	BASE-R PMD status	1.151.7	training_failure_1
Receiver status 0	BASE-R PMD status	1.151.0	rx_trained_0
Frame lock 0	BASE-R PMD status	1.151.1	frame_lock_0
Startup protocol status 0	BASE-R PMD status	1.151.2	training_0
Training failure 0	BASE-R PMD status	1.151.3	training_failure_0

93.7 PMD functional specifications

93.7.1 Link block diagram

One direction for one lane of a 100GBASE-KR4 link is shown in Figure 93–2.

93.7.2 PMD Transmit function

The PMD transmit function shall convert the four bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_*i*.request (*i*=0 to 3) into four separate electrical signals. The four electrical signals shall then be delivered to the MDI, all according to the transmit electrical specifications in 93.8.1. A positive differential output voltage (SL*i*<p> minus SL*i*<n>) shall correspond to tx_bit = one.

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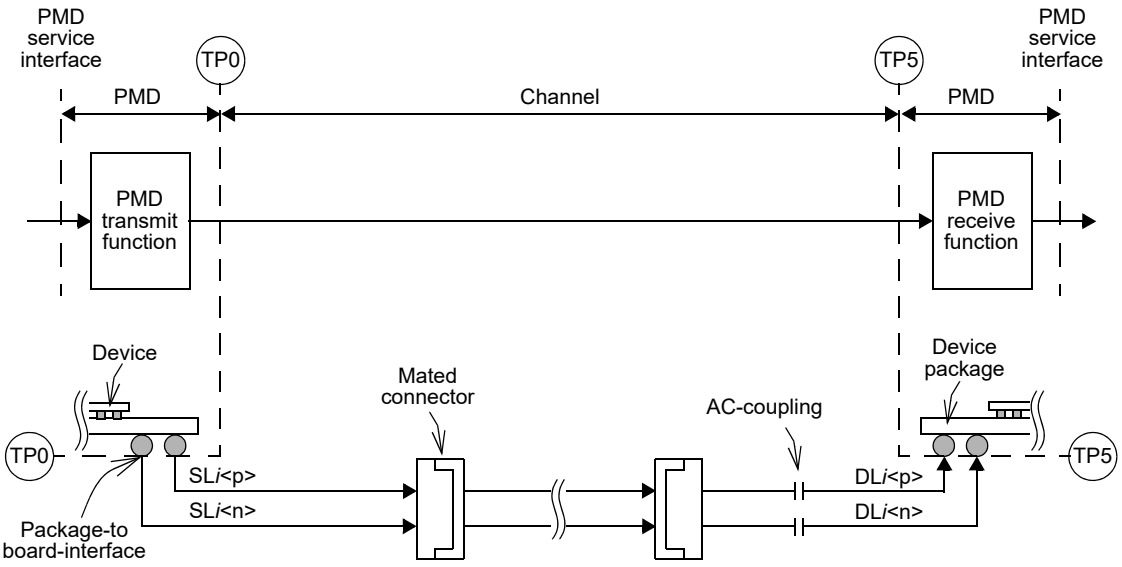

Figure 93–2—100GBASE-KR4 link (one direction for one lane is illustrated)

If the optional EEE deep sleep capability is supported, the following requirements apply. When tx_mode is set to ALERT, the PMD transmit function shall transmit a periodic sequence, where each period of the sequence consists of 8 ones followed by 8 zeros, on each lane, with the transmit equalizer coefficients set to the preset values (see 72.6.10.2.3.1). This sequence is transmitted regardless of the value of tx_bit presented by the PMD:IS_UNITDATA_*i*.request primitive.When tx_mode is not set to ALERT, the transmit equalizer coefficients are set to the values determined via the startup protocol (see 93.7.12).

93.7.3 PMD Receive function

The PMD receive function shall convert the four electrical signals from the MDI into four bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_*i*.indication (*i*=0 to 3). A positive differential input voltage (DL*i*<p> minus DL*i*<n>) shall correspond to rx_bit = one.

93.7.4 Global PMD signal detect function

The variable Global_PMD_signal_detect is the logical AND of the values of PMD_signal_detect_*i* for *i*=0 to 3.

When the MDIO is implemented, this function maps the variable Global_PMD_signal_detect to the register and bit defined in 93.6.

93.7.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal detect function is used by the 100GBASE-KR4 PMD to indicate the successful completion of the startup protocol by the PMD control function (see 93.7.12). PMD_signal_detect_*i* (where *i* represents the lane number in the range 0 to 3) is set to zero when the value of the variable signal_detect is set to false by the Training state diagram for lane *i* (see Figure 72–5). PMD_signal_detect_*i* is set to one when the value of signal_detect for lane *i* is set to true.

If training is disabled by the management variable mr_training_enable (see 93.6), PMD_signal_detect_*i* shall be set to one for *i*=0 to 3.

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If the optional EEE deep sleep capability is supported, the following requirements apply. The value of PMD_signal_detect_*i* (for *i*=0 to 3) is set to zero when rx_mode is first set to QUIET. While rx_mode is set to QUIET, PMD_signal_detect_*i* shall be set to one within 500 ns of the application of the ALERT pattern defined in 93.7.2, with peak-to-peak differential voltage of 720 mV as measured at TP0a, to the differential pair at the input of the channel that connects the transmitter to the receiver of lane *i*. While rx_mode is set to QUIET, PMD_signal_detect_*i* shall not be set to one when the voltage applied to the input of the differential pair of the channel that connects the transmitter to the receiver of lane *i* is less than or equal to 60 mV peak-to-peak differential.

When the MDIO is implemented, this function maps the variables to registers and bits as defined in 93.6.

93.7.6 Global PMD transmit disable function

The Global PMD transmit disable function is mandatory if the EEE deep sleep capability is supported and is otherwise optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When Global_PMD_transmit_disable variable is set to one, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage in Table 93–4.
b) If a PMD fault (93.7.9) is detected, then the PMD may set Global_PMD_transmit_disable to one.
c) Loopback, as defined in 93.7.8, shall not be affected by Global_PMD_transmit_disable.
d) The following additional requirements apply when the optional EEE deep sleep capability is supported. The Global PMD transmit disable function shall turn off all of the transmitters as specified in 93.8.1.3 when tx_mode transitions to QUIET from any other value. The Global PMD transmit disable function shall turn on all of the transmitters as specified in 93.8.1.3 when tx_mode transitions from QUIET to any other value.

93.7.7 PMD lane-by-lane transmit disable function

The PMD transmit disable function is optional and allows the electrical transmitter in each lane to be selectively disabled. When this function is supported, it shall meet the following requirements:

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0 to 3) is set to one, this function shall turn off the transmitter associated with that variable such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 93–4.
b) If a PMD fault (93.7.9) is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the electrical transmitter in each lane.
c) Loopback, as defined in 93.7.8, shall not be affected by PMD_transmit_disable_*i.*

93.7.8 Loopback mode

Local loopback mode is provided by the adjacent PMA (see 83.5.8) as a test function to the device. When loopback mode is enabled, transmission requests passed to each transmitter are sent directly to the corresponding receiver, overriding any signal detected by each receiver on its attached link. Note that loopback mode does not affect the state of the transmitter, which continues to send data (unless disabled).

Control of the loopback function is specified in 83.5.8.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

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NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

93.7.9 PMD fault function

PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault. If the MDIO is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

93.7.10 PMD transmit fault function

The PMD transmit fault function is optional. The faults detected by this function are implementation specific, but the assertion of Global_PMD_transmit_disable is not considered a transmit fault.

If PMD_transmit_fault is set to one, then Global_PMD_transmit_disable should also be set to one.

If the MDIO interface is implemented, then PMD_transmit_fault shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

93.7.11 PMD receive fault function

The PMD receive fault function is optional. The faults detected by this function are implementation specific. A fault is indicated by setting the variable PMD_receive_fault to one.

If the MDIO interface is implemented, then PMD_receive_fault shall be mapped to the Receive fault bit specified in 45.2.1.7.5.

93.7.12 PMD control function

Each lane of the 100GBASE-KR4 PMD shall use the same control function as 10GBASE-KR, as defined in 72.6.10, with the following differences:

a) The training frame structure used by the 100GBASE-KR4 PMD control function shall be as defined in 72.6.10 with the exception that 25.78125 GBd symbols replace 10.3125 GBd symbols and 100GBASE-KR4 UI replace 10GBASE-KR UI.
b) In addition to the coefficient update process specified in 72.6.10.2.5, the period from receiving a new request to responding to that request shall be less than 2 ms, except during the first 50 ms following the beginning of the startup protocol. The beginning of the startup protocol is defined to be entry into the AN_GOOD_CHECK state in Figure 73–10. The start of the period is the frame marker of the training frame with the new request and the end of the period is the frame marker of the training frame with the corresponding response. A new request occurs when the coefficient update field is different from the coefficient field in the preceding frame. The response occurs when the coefficient status report field is updated to indicate that the corresponding action is complete.
c) The training pattern defined in 72.6.10.2.6 shall be replaced with the set of training patterns defined in 92.7.12, which are designed to minimize the correlation between physical lanes.

The variables rx_trained_*i*, frame_lock_*i*, training_*i,* and training_failure_*i* (where *i* goes from 0 to 3) report status for each lane and are equivalent to rx_trained, frame_lock, training, and training_failure as defined in 72.6.10.3.1.

If the MDIO interface is implemented, then this function shall map these variables to the appropriate bits in the BASE-R PMD status register (register 1.151) as specified in 45.2.1.96.

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93.8 100GBASE-KR4 electrical characteristics

93.8.1 Transmitter characteristics

Transmitter characteristics measured at TP0a are summarized in Table 93–4.

Table 93–4—Summary of transmitter characteristics at TP0a

Parameter	Subclause reference	Value	Units
Signaling rate	93.8.1.2	25.78125±100 ppm	GBd
Differential peak-to-peak output voltage (max.) Transmitter disabled Transmitter enabled	93.8.1.3	 30 1200	 mV mV
DC common-mode output voltage (max.)	93.8.1.3	1.9	V
DC common-mode output voltage (min.)	93.8.1.3	0	V
AC common-mode output voltage (RMS, max.)	93.8.1.3	12	mV
Differential output return loss (min.)	93.8.1.4	Equation (93–3)	dB
Common-mode output return loss (min.)	93.8.1.4	Equation (93–4)	dB
Output waveform Steady-state voltage v_f (max.) Steady-state voltage v_f (min.) Linear fit pulse peak (min.) Normalized coefficient step size (min.) Normalized coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)	 93.8.1.5.2 93.8.1.5.2 93.8.1.5.2 93.8.1.5.4 93.8.1.5.4 93.8.1.5.5 93.8.1.5.5	 0.6 0.4 0.71 × v_f 0.0083 0.05 1.54 4	 V V V — — — —
Signal-to-noise-and-distortion ratio, SNDR (min.)	93.8.1.6	27	dB
Output jitter (max.) Even-odd jitter Effective bounded uncorrelated jitter, peak-to-peak Effective total uncorrelated jitter, peak-to-peak	93.8.1.7	 0.035 0.1 0.18	 UI UI UI

93.8.1.1 Transmitter test fixture

Unless otherwise noted, measurements of the transmitter are made at the output of a test fixture (TP0a) as shown in Figure 93–5. The connection from TP0a to the test equipment is AC-coupled.

The insertion loss of the test fixture shall be between 1.2 dB and 1.6 dB at 12.89 GHz. The magnitude of the insertion loss deviation of the test fixture shall be less than or equal to 0.1 dB from 0.05 to 13 GHz.

The reference insertion loss of the test fixture is defined by Equation (93–1) where f is the frequency in GHz.

$$IL_{ref}(f) = -0.0015 + 0.144\sqrt{f} + 0.069f \text{ dB} \qquad 0.05 \le f \le 25 \tag{93–1}$$

The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the measurements. The reference insertion loss is illustrated in Figure 93–3.

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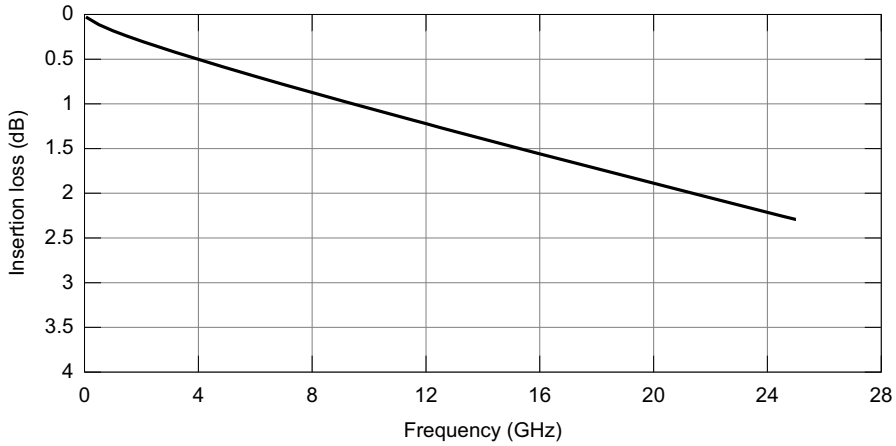

Figure 93–3—Test fixture reference insertion loss

The differential return loss of the test fixture, in dB, shall meet Equation (93–2) where f is the frequency in GHz.

$$RL_d(f) \geq \left\{ \begin{array}{ll} 20 - f & 0.05 \leq f \leq 5 \\ 15 & 5 < f \leq 13 \\ 20.57 - 0.4286f & 13 < f \leq 25 \end{array} \right\} \quad \text{dB} \tag{93–2}$$

The return loss limit is illustrated by Figure 93–4.

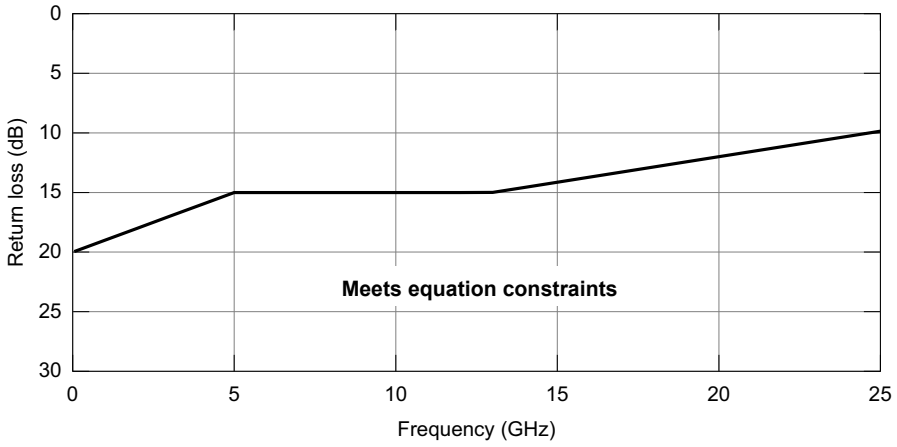

Figure 93–4—Test fixture differential return loss limit

The common-mode return loss of the test fixture shall be greater than or equal to 10 dB from 0.05 to 13 GHz.

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified.

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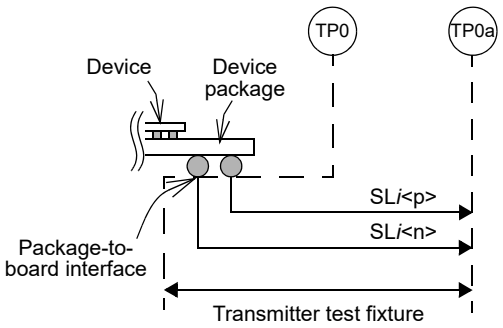

Figure 93–5—Transmitter test fixture and test points

93.8.1.2 Signaling rate and range

The 100GBASE-KR4 signaling rate shall be 25.78125 GBd ± 100 ppm per lane.

93.8.1.3 Signal levels

The differential output voltage v_{di} is defined to be SL*i*<p> minus SL*i*<n>. The common-mode output voltage v_{cmi} is defined to be one half of the sum of SL*i*<p> and SL*i*<n>. These definitions are illustrated by Figure 93–6.

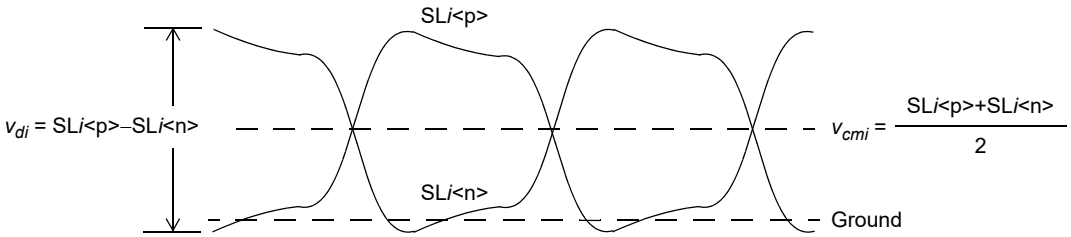

Figure 93–6—Transmitter output voltage definitions

Measurement of the DC common-mode voltage is made with a high-impedance connection to TP0a where each conductor of the differential pair is AC-coupled to a 50 Ω termination.

The peak-to-peak differential output voltage shall be less than or equal to 1200 mV regardless of the transmit equalizer setting. The peak-to-peak differential output voltage shall be less than or equal to 30 mV while the transmitter is disabled (refer to 93.7.6 and 93.7.7).

The DC common-mode output voltage shall be between 0 V and 1.9 V with respect to signal ground. The AC common-mode output voltage shall be less than or equal to 12 mV RMS with respect to signal ground. Common-mode output voltage requirements shall be met regardless of the transmit equalizer setting.

If the optional EEE deep sleep capability is supported the following requirements also apply. The peak-to-peak differential output voltage shall be less than 30 mV within 500 ns of the transmitter being disabled. The peak-to-peak differential output voltage shall be greater than 720 mV within 500 ns of the transmitter being enabled. The transmitter is enabled by the assertion of tx_mode=ALERT and the preceding requirement applies when the transmitted symbols are the periodic pattern defined in 93.7.2 and the transmitter equalizer coefficients are assigned their preset values. The transmitter shall meet the requirements of 93.8.1 within

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1 μs of the transmitter being enabled. While the transmitter is disabled, the DC common-mode output voltage shall be maintained to within ±150 mV of the value for the enabled transmitter.

Unless otherwise noted, differential and common-mode signal levels are measured with a PRBS9 test pattern.

93.8.1.4 Transmitter output return loss

The differential output return loss, in dB, of the transmitter shall meet Equation (93–3) where *f* is the frequency in GHz. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$RL_d(f) \geq \left\{ \begin{array}{ll} 12.05 - f & 0.05 \leq f \leq 6 \\ 6.5 - 0.075f & 6 < f \leq 19 \end{array} \right\} \quad \text{dB} \tag{93–3}$$

The differential return loss limit is illustrated by Figure 93–7.

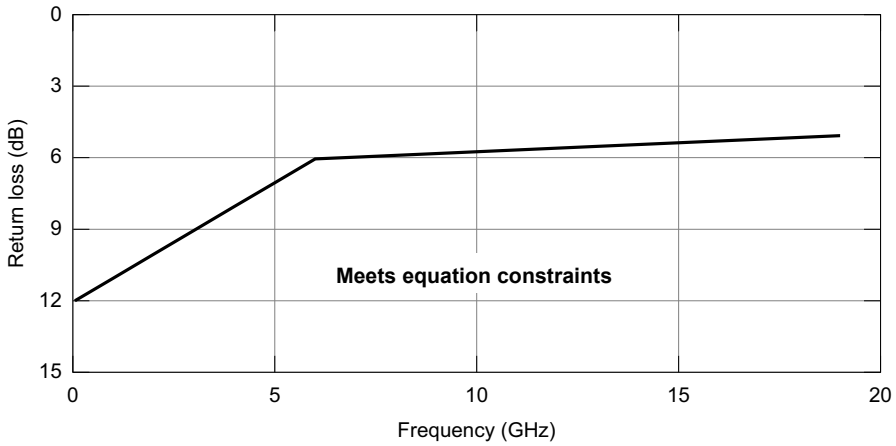

Figure 93–7—Differential return loss limit

The common-mode output return loss, in dB, of the transmitter shall meet Equation (93–4) where *f* is the frequency in GHz. This output impedance requirement applies to all valid output levels. The reference impedance for common-mode return loss measurements shall be 25 Ω.

$$RL_{cm}(f) \geq \left\{ \begin{array}{ll} 9.05 - f & 0.05 \leq f \leq 6 \\ 3.5 - 0.075f & 6 < f \leq 19 \end{array} \right\} \quad \text{dB} \tag{93–4}$$

The common-mode return loss limit is illustrated by Figure 93–8.

93.8.1.5 Transmitter output waveform

The 100GBASE-KR4 transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in Figure 93–9.

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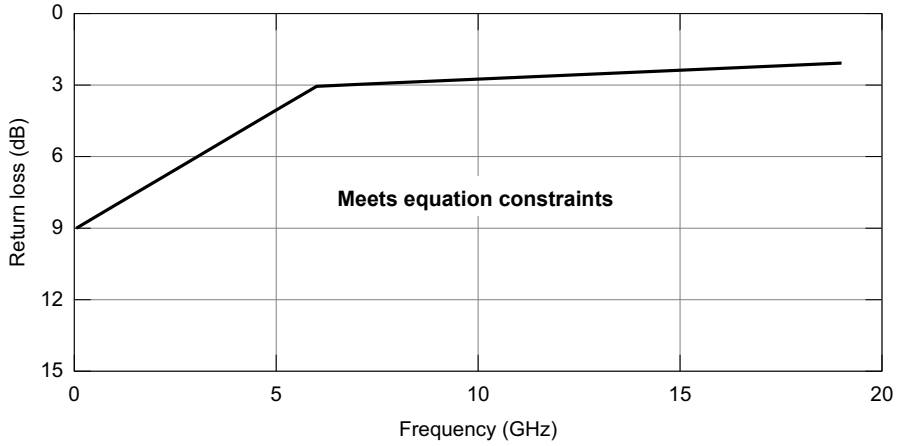

Figure 93–8—Common-mode return loss limit

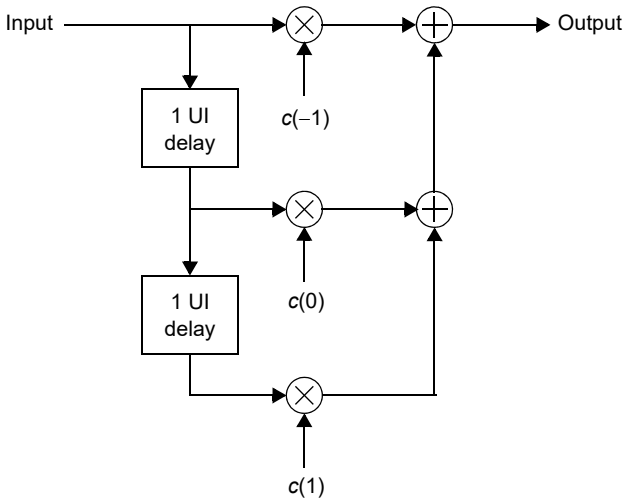

Figure 93–9—Transmit equalizer functional model

The state of the transmit equalizer and hence the transmitted output waveform may be manipulated via the PMD control function defined in 93.7.12 or via the management interface. The transmit function responds to a set of commands issued by the link partner's receive function and conveyed by a back-channel communications path.

This command set includes instructions to:

Increment coefficient $c(i)$.
Decrement coefficient $c(i)$.
Hold coefficient $c(i)$ at its current value.
Set the coefficients to a predefined value (preset or initialize).

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In response, the transmit function relays status information to the link partner's receive function. The status messages indicate that:

The requested update to coefficient $c(i)$ has completed (updated).
Coefficient $c(i)$ is at its minimum value.
Coefficient $c(i)$ is at its maximum value.
Coefficient $c(i)$ is ready for the next update request (not_updated).

93.8.1.5.1 Linear fit to the measured waveform

The transmitter output waveform is characterized using the procedure described in 92.8.3.5.1 with the exception that the measurement is performed at TP0a rather than TP2.

93.8.1.5.2 Steady-state voltage and linear fit pulse peak

The steady-state voltage v_f is defined to be the sum of the linear fit pulse $p(k)$ divided by M (refer to 85.8.3.3 step 3). The steady-state voltage shall be greater than or equal to 0.4 V and less than or equal to 0.6 V after the transmit equalizer coefficients have been set to the "preset" values.

The peak value of $p(k)$ shall be greater than $0.71 \times v_f$ after the transmit equalizer coefficients have been set to the "preset" values.

93.8.1.5.3 Coefficient initialization

When the PMD enters the INITIALIZE state of the Training state diagram (Figure 72–5) or receives a valid request to "initialize" from the link partner, the coefficients of the transmit equalizer shall be configured such that the ratio $(c(0)+c(1)-c(-1))/(c(0)+c(1)+c(-1))$ is 1.29±10% and the ratio $(c(0)-c(1)+c(-1))/(c(0)+c(1)+c(-1))$ is 2.57±10%. These requirements apply upon the assertion a coefficient status report of "updated" for all coefficients.

93.8.1.5.4 Coefficient step size

The change in the normalized amplitude of coefficient $c(i)$ corresponding to a request to "increment" that coefficient shall be between 0.0083 and 0.05. The change in the normalized amplitude of coefficient $c(i)$ corresponding to a request to "decrement" that coefficient shall be between −0.05 and −0.0083.

The change in the normalized amplitude of the coefficient is defined to be the difference in the value measured prior to the assertion of the "increment" or "decrement" request (e.g., the coefficient update request for all coefficients is "hold") and the value upon the assertion of a coefficient status report of "updated" for that coefficient.

93.8.1.5.5 Coefficient range

When sufficient "increment" or "decrement" requests have been received for a given coefficient, the coefficient will reach a lower or upper bound based on the range of that coefficient or the combination of coefficients.

With $c(-1)$ set to zero and both $c(0)$ and $c(1)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0)-c(1))/(c(0)+c(1))$ shall be greater than or equal to 4.

With $c(1)$ set to zero and both $c(-1)$ and $c(0)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0)-c(-1))/(c(0)+c(-1))$ shall be greater than or equal to 1.54.

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Note that a coefficient may be set to zero by first asserting the preset control and then manipulating the other coefficients as required by the test.

93.8.1.6 Transmitter signal-to-noise-and-distortion ratio (SNDR)

Signal-to-noise-and-distortion ratio (SNDR) measured at the transmitter output using the method described in 92.8.3.7 shall be greater than 27 dB regardless of the transmit equalizer setting.

93.8.1.7 Transmitter output jitter

The conditions for the measurement of transmitter output jitter (jitter filter, test pattern, etc.) are defined in 92.8.3.8.

Even-odd jitter is defined in 92.8.3.8.1. Even-odd jitter shall be less than or equal to 0.035 UI regardless of the transmit equalization setting.

Effective bounded uncorrelated jitter and effective total uncorrelated jitter are defined in 92.8.3.8.2. The effective bounded uncorrelated jitter shall be less than or equal to 0.1 UI peak-to-peak regardless of the transmit equalization setting. The effective total uncorrelated jitter shall be less than or equal to 0.18 UI peak-to-peak regardless of the transmit equalization setting.

93.8.2 Receiver characteristics

Receiver characteristics measured at TP5a are summarized in Table 93–5.

Table 93–5—Summary of receiver characteristics at TP5a

Parameter	Subclause reference	Value	Units
Differential input return loss (min.)	93.8.2.2	Equation (93–3)	dB
Differential to common-mode return loss (min.)	93.8.2.2	Equation (93–5)	dB
Interference tolerance	93.8.2.3	Table 93–6	—
Jitter tolerance	93.8.2.4	Table 93–7	—

93.8.2.1 Receiver test fixture

Unless otherwise noted, measurements of the receiver are made at the input to a test fixture (TP5a) as shown in Figure 93–10. The connection from the test equipment to TP5a is AC-coupled.

Unless otherwise noted, measurements of the receiver are made at the input to a test fixture as shown in Figure 93–10.

The insertion loss of the test fixture shall be between 1.2 dB and 1.6 dB at 12.89 GHz. The magnitude of the insertion loss deviation of the test fixture shall be less than or equal to 0.1 dB from 0.05 GHz to 13 GHz.

The reference insertion loss of the test fixture is defined by Equation (93–1) where f is the frequency in GHz. The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the measurements. The reference insertion loss is illustrated in Figure 93–3.

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The differential return loss of the test fixture, in dB, shall meet Equation (93–2) where *f* is the frequency in GHz. The return loss limit is illustrated by Figure 93–4.

The common-mode return loss of the test fixture shall be greater than or equal to 10 dB from 0.05 GHz to 13 GHz.

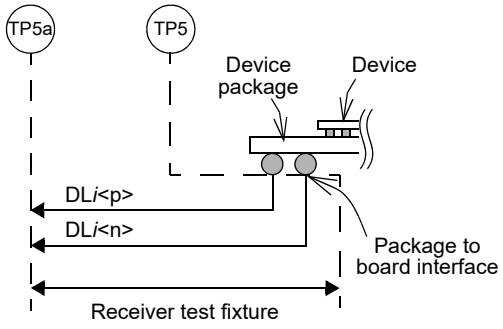

Figure 93–10—Receiver test fixture and test points

93.8.2.2 Receiver input return loss

The differential input return loss, in dB, of the receiver shall meet Equation (93–3) where *f* is the frequency in GHz. The reference impedance for differential return loss measurements shall be 100 Ω. The differential input return loss limit is illustrated by Figure 93–7.

The differential to common-mode return loss, in dB, of the receiver shall meet Equation (93–5).

$$RL_{cd}(f) = \left\{ \begin{array}{ll} 25 - 1.44f & 0.05 \le f \le 6.95 \\ 15 & 6.95 < f \le 19 \end{array} \right\} \quad \text{dB} \tag{93–5}$$

The differential to common-mode return loss limit is illustrated by Figure 93–11.

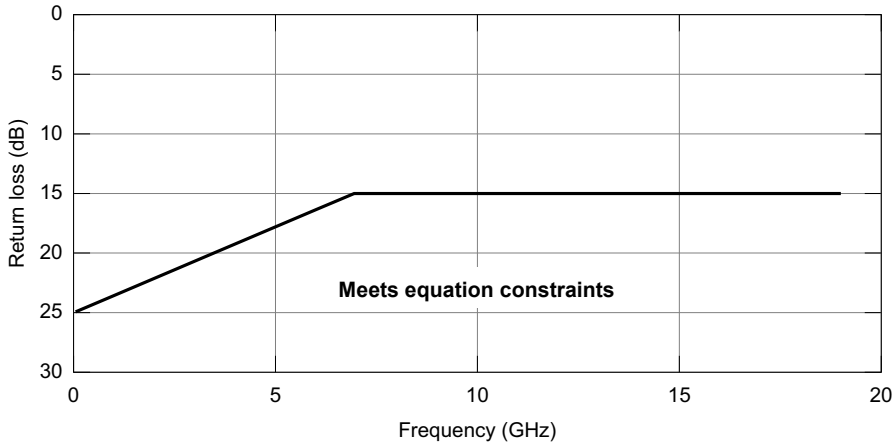

Figure 93–11—Receiver differential to common-mode return loss limit

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93.8.2.3 Receiver interference tolerance

The receiver interference tolerance test setup and method are defined in Annex 93C. The receiver on each lane shall meet the RS-FEC symbol error ratio requirement with the channel defined for each test listed in Table 93–6. The parameter RSS_DFE4 is a figure of merit for the test channel that is defined in 93A.2.

The following considerations apply to the interference tolerance test. The test transmitter meets the specifications in 93.8.1 as measured at TP0a (see Figure 93C–3). The test transmitter is constrained such that for any transmit equalizer setting the differential peak-to-peak voltage (see 93.8.1.3) is less than or equal to 800 mV and the pre- and post-cursor equalization ratios (see 93.8.1.5.5) are less than or equal to 1.54 and 4, respectively. The lowest frequency f_{NSD1} for constraints on the noise spectral density is 1 GHz. The return loss of the test setup in Figure 93C–4 measured at TP5 replica meets the requirements of Equation (93–2).

The values of the parameters required for the calculation of Channel Operating Margin (COM) are given in Table 93–8 with the following exceptions. The COM parameter σ_{RJ} is set to the measured value of effective random jitter (see 92.8.3.8.2), the COM parameter A_{DD} is set to half the measured value of effective bounded uncorrelated jitter (see 93.8.1.7), and the COM parameter SNR_{TX} is set to the value of SNDR measured at TP0a (see 93.8.1.6). Tests 1 and 2 are for the case when error correction is bypassed in the RS-FEC sublayer (see 91.5.3.3) and for these cases COM is computed with a DER_0 value of 10^{-12}. The test pattern to be used is any valid PCS output (such as scrambled idle), which is subsequently encoded by the RS-FEC sublayer.

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.

Table 93–6—Receiver interference tolerance parameters

Parameter	Test 1 values		Test 2 values		Test 3 values		Test 4 values		Units
	Min	Max	Min	Max	Min	Max	Min	Max	
RS-FEC symbol error ratio[a]	—	10^{-11}	—	10^{-11}	—	10^{-4}	—	10^{-4}	—
Insertion loss at 12.89 GHz[b]	—	16	30	—	—	30	35	—	dB
Coefficients of fitted insertion loss[c]									
a_0	–0.9	0.9	–0.9	0.9	–0.9	0.9	–0.9	0.9	dB
a_1	0	3.3	0	3.3	0	3.3	0	3.3	dB/GHz$^{1/2}$
a_2	0	—	0	—	0	—	0	—	dB/GHz
a_4	0	0.022	0	0.03	0	0.03	0	0.043	dB/GHz^2
RSS_DFE4	0.05	—	0.05	—	0.05	—	0.05	—	—
COM, including effects of broadband noise[d]	3		3		3		3		dB

[a]The FEC symbol error ratio is measured in step 10 of the receiver interference tolerance method defined in 93C.2.
[b]Measured between TPt and TP5 (see Figure 93C–4).
[c]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C–4) using the method in 93A.3 with f_{min} = 0.05 GHz, f_{max} = 25.78125 GHz, and maximum Δf = 0.01 GHz.
[d]The COM value is the target for the receiver noise level calibration defined in 93C.2 step 7. The channel noise voltage applied in 93C.2 step 8 should be as close as practical to the value needed to produce the target COM. If higher channel noise voltage values are used, this would demonstrate margin to the specification but this is not required for compliance.

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93.8.2.4 Receiver jitter tolerance

Receiver jitter tolerance is measured using the test setup shown in Figure 93–12, or its equivalent, for the receiver of each lane.

The test transmitter meets the specifications of 93.8.1. It is constrained so that its differential peak-to-peak output voltage does not exceed 800 mV at TP0a regardless of the transmitter equalizer setting (see 93.8.1.3). It is further constrained so that its maximum pre-cursor equalization ratio is 1.54 and its maximum post-cursor equalization ratio is 4 (see 93.8.1.5.5).

The test channel meets the requirements of the interference tolerance test channel using Test 4 values (see 93.8.2.3). No broadband noise is added for this test.

Receiver jitter tolerance is verified for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 93–7. The synthesizer frequency is set to the specified jitter frequency and the synthesizer output amplitude is adjusted until the specified peak-to-peak jitter amplitude for that frequency is measured at TP0a. The output of the ISI channel is connected to the input of the receiver under test at TP5a. The link is initialized and the PMD startup protocol is allowed to complete, thereby optimizing the test transmitter equalizer. The test transmitter then transmits any valid PCS output (such as scrambled idle), which is subsequently encoded by the RS-FEC sublayer. The RS-FEC symbol error ratio is measured using the errored symbol counter FEC_symbol_error_counter_*i* where *i* is the lane number of the receiver under test.

The RS-FEC symbol error ratio shall be less than or equal to 10^{-4} for each case listed in Table 93–7.

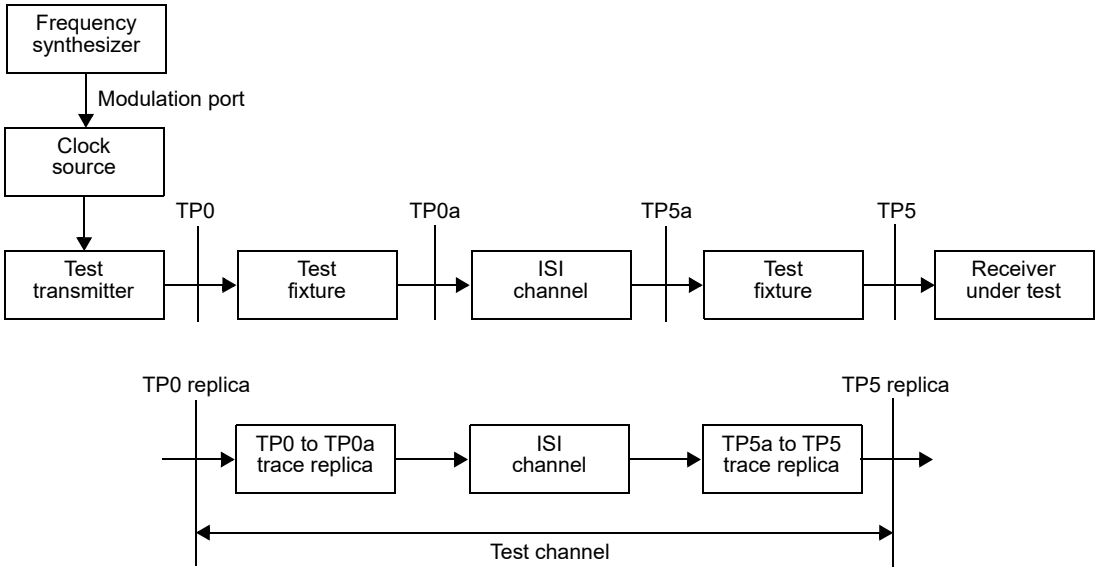

Figure 93–12—Jitter tolerance test setup

Table 93–7—Receiver jitter tolerance parameters

Parameter	Case A values	Case B values	Units
Jitter frequency	190	940	kHz
Peak-to-peak jitter amplitude	5	1	UI

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93.9 Channel characteristics

93.9.1 Channel Operating Margin

The Channel Operating Margin (COM) is computed using the procedure in 93A.1 with the Test 1 and Test 2 values in Table 93–8. Test 1 and Test 2 differ in the value of the device package model transmission line length z_p.

COM shall be greater than or equal to 3 dB for each test. This minimum value allocates margin for practical limitations on the receiver implementation as well as the largest step size allowed for transmitter equalizer coefficients.

The receive path of the RS-FEC sublayer may have the option to perform error detection without correction to reduce the data delay (see 91.5.3.3). Channels that are compatible with this mode of operation shall meet this COM requirement with the value of DER_0 set to 10^{-12}.

93.9.2 Insertion loss

The insertion loss, in dB, of the channel is recommended to meet Equation (93–6).

$$IL(f) \le \left\{ \begin{array}{ll} 1.5 + 4.6\sqrt{f} + 1.318f & 0.05 \le f \le f_b/2 \\ -12.71 + 3.7f & f_b/2 < f \le f_b \end{array} \right\} \text{ (dB)} \qquad (93\text{–}6)$$

where

f is the frequency in GHz
f_b is the signaling rate (25.78125) in GHz
$IL(f)$ is the insertion loss at frequency f

The insertion loss limit is illustrated by Figure 93–13.

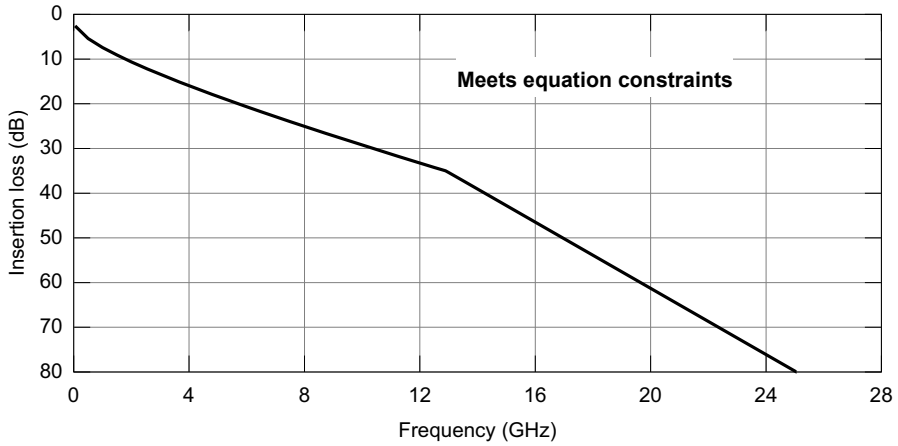

Figure 93–13—Insertion loss limit

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Table 93–8—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	$f_{\min}$	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface	 C_d z_p z_p C_p	 2.5×10^{-4} 12 30 1.8×10^{-4}	 nF mm mm nF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.62	—
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.18 0 0.02	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.38 0 0.02	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –12 0 1	 dB dB dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	$f_b / 4$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b / 4$ f_b	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.4 0.4 0.6	 V V V
Number of signal levels	L	2	—
Level separation mismatch ratio	R_{LM}	1	—
Transmitter signal-to-noise ratio	SNR_{TX}	27	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	14	UI
Normalized DFE coefficient magnitude limit, for $n = 1$ to N_b	$b_{\max}(n)$	1	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.05	UI
One-sided noise spectral density	η_0	5.2×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-5}	—

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93.9.3 Return loss

The return loss, in dB, of the channel is recommended to meet Equation (93–7).

$$RL_d(f) \geq \left\{ \begin{array}{ll} 12 & 0.05 \leq f \leq f_b/4 \\ 12 - 15\log_{10}(4f/f_b) & f_b/4 < f \leq f_b \end{array} \right\} \quad \text{dB} \qquad (93\text{–}7)$$

where

f is the frequency in GHz
f_b is the signaling rate (25.78125) in GHz
$RL(f)$ is the return loss at frequency f

The differential return loss limit is illustrated by Figure 93–14.

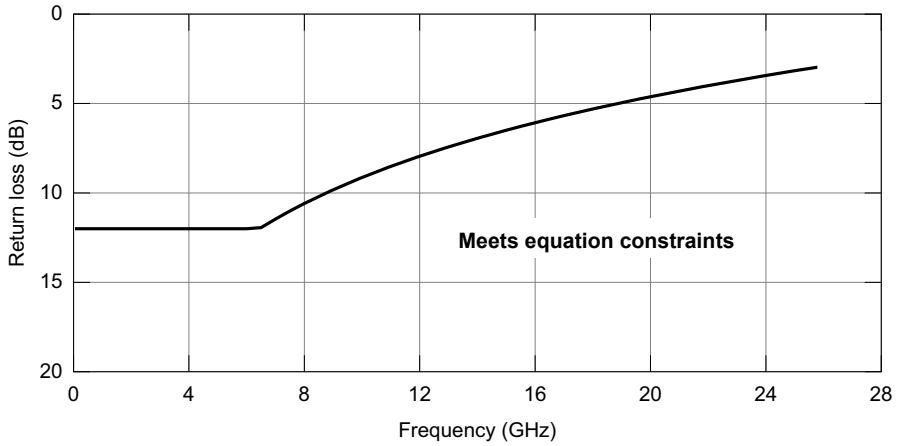

Figure 93–14—Differential return loss limit

93.9.4 AC-coupling

The 100GBASE-KR4 transmitter shall be AC-coupled to the receiver. Common-mode specifications are defined as if the DC-blocking capacitor is implemented between TP0 and TP5. Should the capacitor be implemented outside TP0 and TP5, the common-mode specifications in Table 93–4 may not be appropriate.

The impact of a DC-blocking capacitor implemented between TP0 and TP5 is accounted for within the channel specifications. Should the capacitor be implemented outside TP0 and TP5, it is the responsibility of implementers to consider any necessary modifications to common-mode and channel specifications required for interoperability as well as any impact on the verification of transmitter and receiver compliance.

The low-frequency 3 dB cutoff of the AC-coupling shall be less than 50 kHz.

93.10 Environmental specifications

93.10.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

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93.10.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

93.10.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

93.10.4 Electromagnetic compatibility

A system integrating the 100GBASE-KR4 PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

93.10.5 Temperature and humidity

A system integrating the 100GBASE-KR4 PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

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93.11 Protocol implementation conformance statement (PICS) proforma for Clause 93, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR4[162]

93.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 93, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

93.11.2 Identification

93.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

93.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 93, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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93.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
CGMII	CGMII	93.1	Interface is supported	O	Yes [ ] No [ ]
PCS	100GBASE-R PCS	93.1		M	Yes [ ]
RS-FEC	100GBASE-R RS-FEC	93.1		M	Yes [ ]
PMA	100GBASE-R PMA	93.1		M	Yes [ ]
CAUI-10	CAUI-10	93.1	Interface is supported	O	Yes [ ] No [ ]
CAUI-4	CAUI-4	93.1	Interface is supported	O	Yes [ ] No [ ]
AN	Auto-negotiation	93.1		M	Yes [ ]
DC	Delay constraints	93.4	Conforms to delay constraints specified in 93.4	M	Yes [ ]
DSC	Skew constraints	93.5	Conforms to the Skew and Skew Variation constraints specified in 93.5	M	Yes [ ]
*MD	MDIO capability	93.6	Registers and interface supported	O	Yes [ ] No [ ]
*EEE	EEE capability	93.1	Capability is supported	O	Yes [ ] No [ ]
*GTD	Global PMD transmit disable function	93.7.6	Function is supported	EEE:M	Yes [ ] N/A [ ]
*LTD	PMD lane-by-lane transmit disable function	93.7.7	Function is supported	O	Yes [ ] No [ ]
*CHNL	Channel	93.9	Channel specifications not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]

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93.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR4

93.11.4.1 Functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	PMD transmit function	93.7.2	Converts four logical bit streams from the PMD service interface into four electrical signals and delivers them to the MDI	M	Yes [ ]
FS2	Mapping of logical signals to electrical signals	93.7.2	Positive differential output voltage corresponds to tx_bit=one	M	Yes [ ]
FS3	ALERT signal	93.7.2	Transmit a periodic sequence, where each period of the sequence consists of 8 ones followed by 8 zeros, on each lane when tx_mode is set to ALERT	EEE:M	Yes [ ] N/A [ ]
FS4	PMD receive function	93.7.3	Converts four electrical signals from the MDI into four logical bit streams delivers them to the PMD service interface	M	Yes [ ]
FS5	Mapping of electrical signals to logical signals	93.7.3	Positive differential input voltage corresponds to rx-_bit=one	M	Yes [ ]
FS6	SIGNAL_OK mapping	93.2	Set to OK when Global_PM-D_signal_detect is one and set to FAIL when Global_P-MD_signal_detect is zero	M	Yes [ ]
FS7	Training disabled by variable mr_training_enable	93.7.5	PMD_signal_detect_*i* set to one for *i*=0 to 3	M	Yes [ ]
FS8	PMD_signal_detect_*i* asserted, rx_mode=QUIET	93.7.5	Set to one within 500 ns following the application of the signal defined in 93.7.5 to the input of the channel corresponding to the receiver of lane *i*	EEE:M	Yes [ ] N/A [ ]
FS9	PMD_signal_detect_*i* not asserted, rx_mode=QUIET	93.7.5	Not set to one when the signal applied to the input of the channel corresponding to the receiver of lane *i* is less than or equal to 60 mV peak-to-peak differential	EEE:M	Yes [ ] N/A [ ]
FS10	Global_PMD_transmit_disable variable	93.7.6	When set to one, all transmitters satisfy the requirements of 93.7.6	GTD:M	Yes [ ] N/A [ ]
FS11	Global PMD transmit disable function affect on loopback	93.7.6	No effect	GTD:M	Yes [ ] N/A [ ]
FS12	Global PMD transmit disable function, tx_mode transition to QUIET	93.7.6	Turn off all transmitters when tx_mode transitions to QUIET from any other value	EEE:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
FS13	Global PMD transmit disable function, tx_mode transition from QUIET	93.7.6	Turn on all transmitters when tx_mode transitions from QUIET to any other value	EEE:M	Yes [ ] N/A [ ]
FS14	PMD_transmit_disable_*i* variable	93.7.7	When set to one, the transmitter for lane *i* satisfies the requirements of 93.8.1.3	LTD:M	Yes [ ] N/A [ ]
FS15	PMD lane-by-lane transmit disable function affect on loopback	93.7.7	No effect	LTD:M	Yes [ ] N/A [ ]
FS16	PMD_fault variable mapping to MDIO	93.7.9	Mapped to the fault bit as specified in 45.2.1.2.3	MD:M	Yes [ ] N/A [ ]
FS17	PMD_transmit_fault variable mapping to MDIO	93.7.10	Mapped to Transmit fault bit as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
FS18	PMD_receive_fault variable mapping to MDIO	93.7.11	Mapped to Receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]
FS19	PMD control function	93.7.12	Defined in 72.6.10	M	Yes [ ]
FS20	Training frame structure	93.7.12	Defined in 72.6.10 but adjusted for 100GBASE-KR4 signaling rate	M	Yes [ ]
FS21	Training patterns	93.7.12	Training patterns defined in 92.7.12.	M	Yes [ ]
FS22	PMD control function variable mapping to MDIO	93.7.12	Map variables as specified in 93.7.12	MD:M	Yes [ ] N/A [ ]
FS23	PMD control response time	93.7.12	Response time less than 2 ms	M	Yes [ ]

93.11.4.2 Transmitter characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Test fixture insertion loss	93.8.1.1	Between 1.2 dB and 1.6 dB at 12.89 GHz	M	Yes [ ]
TC2	Test fixture insertion loss deviation	93.8.1.1	Magnitude less than 0.1 dB	M	Yes [ ]
TC3	Test fixture differential return loss	93.8.1.1	Meets equation constraints	M	Yes [ ]
TC4	Test fixture common-mode return loss	93.8.1.1	Greater than or equal to 10 dB from 0.05 to 13 GHz	M	Yes [ ]
TC5	Signaling rate per lane	93.8.1.2	25.78125 GBd ± 100 ppm	M	Yes [ ]
TC6	Peak-to-peak differential output voltage	93.8.1.3	Less than or equal to 1200 mV regardless of transmit equalizer setting	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC7	Peak-to-peak differential output voltage, transmitter disabled	93.8.1.3	Less than or equal to 30 mV	M	Yes [ ]
TC8	DC common-mode output voltage	93.8.1.3	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC9	AC common-mode output voltage	93.8.1.3	Less than or equal to 12 mV RMS with respect to signal ground	M	Yes [ ]
TC10	Common-mode output voltage requirements	93.8.1.3	Met regardless of the transmit equalizer setting	M	Yes [ ]
TC11	Transmitter disable timing	93.8.1.3	Peak-to-peak differential output voltage less than 30 mV within 500 ns of the transmitter being disabled	EEE:M	Yes [ ] N/A [ ]
TC12	Transmitter enable timing	93.8.1.3	Peak-to-peak differential output voltage greater than 720 mV within 500 ns of the transmitter being enabled and meet all requirements of 93.8.1 within 1 μs	EEE:M	Yes [ ] N/A [ ]
TC13	Common-mode output voltage, transmitter disabled	93.8.1.3	Maintained to within ±150 mV of the value for the enabled transmitter	EEE:M	Yes [ ] N/A [ ]
TC14	Differential input return loss	93.8.1.4	Meets equation constraints	M	Yes [ ]
TC15	Reference impedance for differential return loss measurements	93.8.1.4	100 Ω	M	Yes [ ]
TC16	Common-mode output return loss	93.8.1.4	Meets equation constraints	M	Yes [ ]
TC17	Reference impedance for common-mode return loss measurements	93.8.1.4	25 Ω	M	Yes [ ]
TC18	Steady-state voltage, v_f	93.8.1.5.2	Greater than or equal to 0.4 V and less than or equal to 0.6 V after the transmit equalizer coefficients have been set to the “preset” values	M	Yes [ ]
TC19	Linear fit pulse peak	93.8.1.5.2	Greater than $0.71 \times v_f$ after the transmit equalizer coefficients have been set to the “preset” values	M	Yes [ ]
TC20	Coefficient initialization	93.8.1.5.3	Satisfies the requirements of 93.8.1.5.3.	M	Yes [ ]
TC21	Normalized coefficient step size for “increment”	93.8.1.5.4	Between 0.0083 and 0.05	M	Yes [ ]
TC22	Normalized coefficient step size for “decrement”	93.8.1.5.4	Between –0.05 and –0.0083	M	Yes [ ]
TC23	Maximum post-cursor equalization ratio	93.8.1.5.5	Greater than or equal to 4	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC24	Maximum pre-cursor equalization ratio	93.8.1.5.5	Greater than or equal to 1.54	M	Yes [ ]
TC25	Transmitter output noise and distortion	93.8.1.6	SNDR greater than or equal to 27 dB	M	Yes [ ]
TC26	Even-odd jitter	93.8.1.7	Less than or equal to 0.035 UI regardless of the transmit equalization setting	M	Yes [ ]
TC27	Effective bounded uncorrelated jitter	93.8.1.7	Less than or equal to 0.1 UI peak-to-peak regardless of the transmit equalization setting	M	Yes [ ]
TC28	Effective total uncorrelated jitter	93.8.1.7	Less than or equal to 0.18 UI peak-to-peak regardless of the transmit equalization setting	M	Yes [ ]

93.11.4.3 Receiver characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Test fixture insertion loss	93.8.2.1	Between 1.2 dB and 1.6 dB at 12.89 GHz	M	Yes [ ]
RC2	Test fixture insertion loss deviation	93.8.2.1	Magnitude less than 0.1 dB	M	Yes [ ]
RC3	Test fixture differential return loss	93.8.2.1	Meets equation constraints	M	Yes [ ]
RC4	Test fixture common-mode return loss	93.8.2.1	Greater than or equal to 10 dB from 0.05 GHz to 13 GHz	M	Yes [ ]
RC5	Differential input return loss	93.8.2.2	Meets equation constraints	M	Yes [ ]
RC6	Reference impedance for differential return loss measurements	93.8.2.2	100 Ω	M	Yes [ ]
RC7	Differential to common-mode return loss	93.8.2.2	Meets equation constraints	M	Yes [ ]
RC8	Receiver interference tolerance	93.8.2.3	Satisfy requirements summarized in Table 93–6	M	Yes [ ]
RC9	Receiver jitter tolerance	93.8.2.4	RS-FEC symbol error ratio less than or equal to 10^{-4} for each case listed in Table 93–7	M	Yes [ ]

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93.11.4.4 Channel characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	93.9.1	Greater than or equal to 3 dB for each test listed in Table 93–8	CHNL:M	Yes [ ] N/A [ ]
CC2	COM when error correction is bypassed by the RS-FEC sublayer	93.9.1	Greater than or equal to 3 dB for each test listed in Table 93–8 but with $DER_0 = 10^{-12}$	CHNL:M	Yes [ ] N/A [ ]
CC3	AC-coupling	93.9.4	Channel AC-couples the transmitter to the receiver	CHNL:M	Yes [ ] N/A [ ]
CC4	AC-coupling 3 dB cut-off frequency	93.9.4	Less than 50 kHz	CHNL:M	Yes [ ] N/A [ ]

93.11.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	93.10.1	Conforms to J.2	M	Yes [ ]
ES2	Electromagnetic compatibility	93.10.4	Comply with applicable local and national codes	M	Yes [ ]

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94. Physical Medium Attachment (PMA) sublayer, Physical Medium Dependent (PMD) sublayer, and baseband medium, type 100GBASE-KP4

94.1 Overview

This clause specifies the Physical Medium Attachment (PMA) sublayers, Physical Medium Dependent (PMD) sublayer, and medium for the 100GBASE-KP4 PHY.

When forming a complete Physical Layer, the PMA shall be connected to the RS-FEC, the PMD shall be connected to the medium through the MDI as shown in Figure 94–1, and the PMA and PMD shall be connected to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 94–1—Physical Layer clauses associated with the 100GBASE-KP4 PMD

Associated clause	100GBASE-KP4
81—RS	Required
81—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
83—PMA for 100GBASE-R	Optional
83A—CAUI-10	Optional
83D—CAUI-4	Optional
91—RS-FEC	Required
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation behaves functionally as though the RS and CGMII were present.

Figure 94–1 shows the relationship of the 100GBASE-KP4 PMA and PMD sublayers and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.

Differential signals received at the MDI from a transmitter that meets the requirements of 94.2.2 and 94.3.12 and have passed through the channel specified in 94.4 are received with a BER less than 10^{-5} as measured at the PMA service interface.

For a complete Physical Layer, this specification is considered to be satisfied by a frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap.

A 100GBASE-KP4 PHY with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization.

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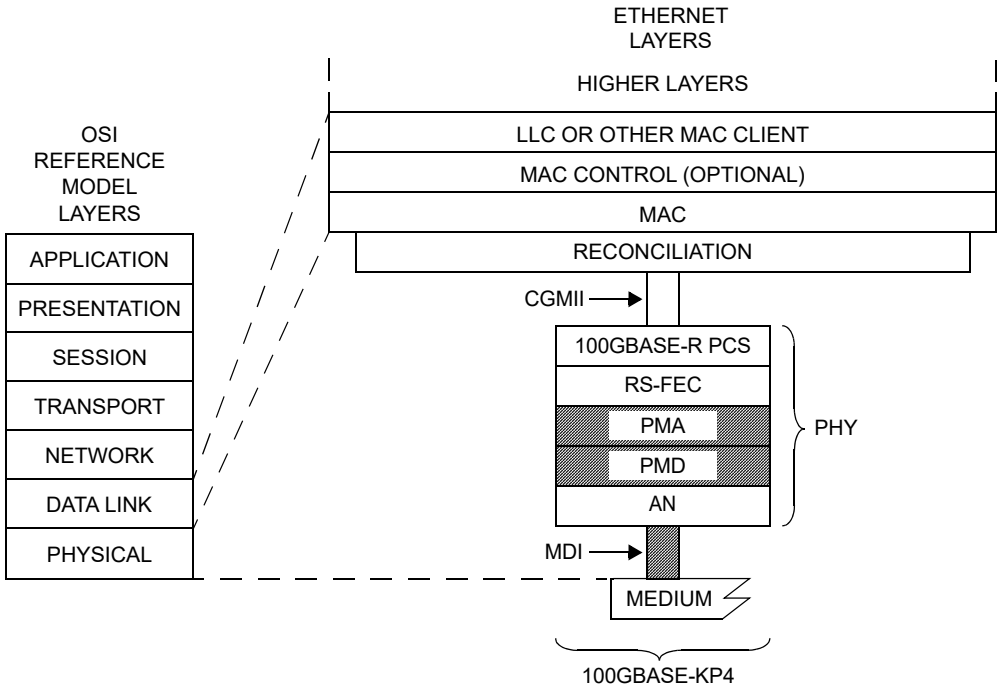

AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 94–1—100GBASE-KP4 PMA and PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

94.2 Physical Medium Attachment (PMA) Sublayer

94.2.1 PMA Service Interface

The PMA service interface for 100GBASE-KP4 PMA is based on the inter-sublayer service interface defined in 80.3. This interface is defined in an abstract manner and does not imply any particular implementation.

The PMA service interface primitives are summarized as follows:

PMA:IS_UNITDATA_*i*.request
PMA:IS_UNITDATA_*i*.indication
PMA:IS_SIGNAL.indication

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If the optional EEE deep sleep capability is supported (see Clause 78, 78.1.3.3.1), then the PMA service interface includes four additional primitives as follows:

PMA:IS_TX_MODE.request
PMA:IS_RX_MODE.request
PMA:IS_ENERGY_DETECT.indication
PMA:IS_RX_TX_MODE.indication

94.2.1.1 PMA:IS_UNITDATA_i.request

The PMA:IS_UNITDATA_*i*.request (where *i*=0 to 3) primitive is used to define the transfer of four streams of data units from the PMA client to the PMA.

94.2.1.1.1 Semantics of the service primitive

PMA:IS_UNITDATA_0.request(tx_bit,start)
PMA:IS_UNITDATA_1.request(tx_bit,start)
PMA:IS_UNITDATA_2.request(tx_bit,start)
PMA:IS_UNITDATA_3.request(tx_bit,start)

The data conveyed by PMA:IS_UNITDATA_0.request to IS_UNITDATA_3.request consists of four parallel continuous streams of encoded bits, one stream for each lane. Each of the tx_bit parameters can take one of two values: one or zero. The start parameter is TRUE to indicate that the concurrent tx_bit is the first bit of the first, second, third, or fourth FEC symbol in an FEC codeword and is otherwise FALSE.

94.2.1.1.2 When generated

The PMA client continuously sends four parallel bit streams PMA:IS_UNITDATA_*i*.request(tx_bit,start) to the PMA, each at a nominal signaling rate of 26.5625 Gb/s.

94.2.1.1.3 Effect of receipt

Upon receiving each instance of PMA:IS_UNITDATA_*i*.request, the tx_bit and start parameters are passed to the PMA framing process corresponding to each stream.

94.2.1.2 PMA:IS_UNITDATA_i.indication

The PMA:IS_UNITDATA_*i*.indication (where *i* = 0 to 3) primitive is used to define the transfer of four streams of data units from the PMA to the PMA client.

94.2.1.2.1 Semantics of the service primitive

PMA:IS_UNITDATA_0.indication(rx_bit, start)
PMA:IS_UNITDATA_1.indication(rx_bit, start)
PMA:IS_UNITDATA_2.indication(rx_bit, start)
PMA:IS_UNITDATA_3.indication(rx_bit, start)

The data conveyed by PMA:IS_UNITDATA_0.indication to PMA:IS_UNITDATA_3.indication consists of four parallel continuous streams of encoded bits, one stream for each lane. Each of the rx_bit parameters can take one of two values: one or zero. The start parameter is TRUE to indicate that the concurrent rx_bit is the first bit of the first, second, third, or fourth FEC symbol in the FEC codeword and is otherwise FALSE.

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94.2.1.2.2 When generated

The PMA continuously sends four parallel bit streams PMA:IS_UNITDATA_*i*.indication(rx_bit,start) to the PMA client, each at a nominal signaling rate of 26.5625 Gb/s.

94.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is defined by the PMA client.

94.2.1.3 PMA:IS_SIGNAL.indication

The PMA:IS_SIGNAL.indication primitive is generated by the PMA to the PMA client to indicate the status of the receive process. This primitive is generated by the receive process to propagate the detection of severe error conditions (e.g., loss of synchronization) to the PMA client.

94.2.1.3.1 Semantics of the service primitive

PMA:IS_SIGNAL.indication(SIGNAL_OK)

The SIGNAL_OK parameter can take on one of two values: OK or FAIL. A value of FAIL denotes that invalid data is being presented (rx_bit parameters undefined) by the PMA to the PMA client. A value of OK does not guarantee valid data is being presented by the PMA to the PMA client.

94.2.1.3.2 When generated

The PMA generates the PMA:IS_SIGNAL.indication primitive to the PMA client whenever there is a change in the value of the SIGNAL_OK parameter.

94.2.1.3.3 Effect of receipt

The effect of receipt of this primitive is defined by the PMA client.

94.2.1.4 PMA:IS_TX_MODE.request

The PMA:IS_TX_MODE.request primitive communicates the tx_mode parameter generated by the PCS LPI transmit process to invoke the appropriate PMA, FEC, and PMD transmit EEE states. Without EEE deep sleep capability, this primitive is never invoked and the sublayers behave as if tx_mode = DATA.

94.2.1.4.1 Semantics of the service primitive

PMA:IS_TX_MODE.request(tx_mode)

The tx_mode parameter takes on one of up to three values: DATA, QUIET, or ALERT.

94.2.1.4.2 When generated

This primitive is generated to indicate the state of the PCS LPI transmit function.

94.2.1.4.3 Effect of receipt

When this primitive is received, PMD:IS_TX_MODE.request(tx_mode) is generated with the value received in PMA:IS_TX_MODE.request(tx_mode).

If the value is DATA or ALERT, the PMA operates normally.

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If the value is QUIET, the PMA may go into a low power mode.

94.2.1.5 PMA:IS_RX_MODE.request

The PMA:IS_RX_MODE.request primitive communicates the rx_mode parameter generated by the PCS LPI receive process. Without EEE deep sleep capability, this primitive is never invoked and the sublayers behave as if rx_mode = DATA.

94.2.1.5.1 Semantics of the service primitive

PMA:IS_RX_MODE.request(rx_mode)

The rx_mode parameter takes on one of two values: DATA or QUIET.

94.2.1.5.2 When generated

This primitive is generated to indicate the state of the PCS LPI receive function.

94.2.1.5.3 Effect of receipt

When this primitive is received, PMD:IS_RX_MODE.request(rx_mode) is generated with the value received in PMA:IS_RX_MODE.request(rx_mode).

If the value is DATA, the PMA operates normally.

If the value is QUIET, the PMA may be go into a low power mode.

94.2.1.6 PMA:IS_ENERGY_DETECT.indication

The PMA:IS_ENERGY_DETECT.indication primitive is used to communicate that the PMD has detected the presence of energy on the interface following a period of quiescence. Without EEE deep sleep capability, this primitive is never invoked and has no effect.

94.2.1.6.1 Semantics of the service primitive

PMA:IS_ENERGY_DETECT.indication(energy_detect)

The parameter energy_detect is Boolean.

94.2.1.6.2 When generated

This primitive is generated by the PMA, reflecting the state of PMD:IS_SIGNAL.indication(SIGNAL_OK) received from the PMD (see 94.3.1.3). When SIGNAL_OK indicates OK, energy detect indicates TRUE. When SIGNAL_OK indicates FAIL, energy_detect indicates FALSE.

94.2.1.6.3 Effect of receipt

The effect of receipt of this primitive is defined by the PMA client sublayers that receive it.

94.2.1.7 PMA:IS_RX_TX_MODE.indication

The PMA:IS_RX_TX_MODE.indication primitive communicates the value of the rx_tx_mode parameter. This parameter indicates the value of tx_mode that the PMA sublayer has inferred from the received signal.

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Without EEE deep sleep capability, the primitive is never generated and the sublayers behave as if rx_tx_mode=DATA.

94.2.1.7.1 Semantics of the service primitive

PMA:IS_RX_TX_MODE.indication(rx_tx_mode)

The parameter rx_tx_mode is assigned one of the following values: DATA, QUIET, or ALERT. DATA is assigned when the PMA is reset or when PMA frames are being received. QUIET is assigned if PMA frame reception ceases. ALERT is assigned if rx_tx_mode = QUIET and PMD:IS_SIGNAL.indication(SIGNAL_OK) transitions from FAIL to OK.

94.2.1.7.2 When generated

This primitive is generated whenever there is change in the value of the rx_tx_mode parameter.

94.2.1.7.3 Effect of receipt

The RS-FEC sublayer passes this primitive through to the PMA sublayer that may exist above.

94.2.2 PMA Transmit Functional Specifications

In the transmit direction, the role of the 100GBASE-KP4 PMA is to adapt the signal from the FEC (the PMA client) to a PAM4 encoded signal to be passed to the PMD for transfer over the attached medium. The adaptation processes shown in Figure 94–2 include insert overhead, insert termination bits, apply Gray coding, apply 1/(1+D) mod 4 precoding, and apply PAM4 encoding.

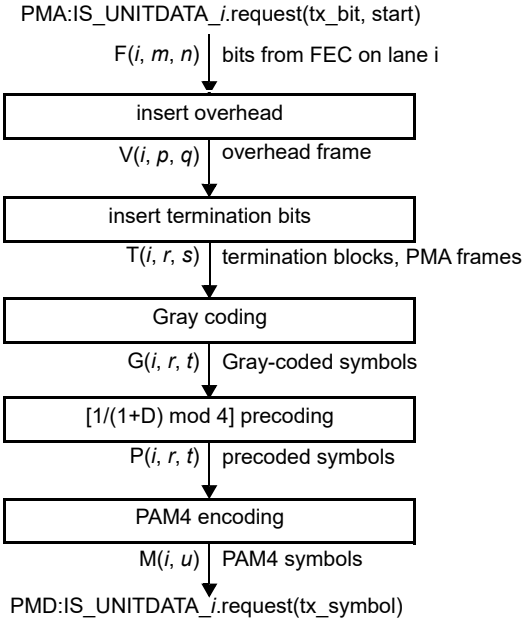

Figure 94–2—Transmit adaptation process diagram

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94.2.2.1 FEC Interface

The PMA transmit process receives FEC bits via the PMA:IS_UNITDATA_*i*(tx_bit, start) primitive (see 94.2.1.1). The index *i* indicates the PMA lane number: 0, 1, 2, or 3.

On each transaction, tx_bit is assigned to F(*i*, *m*, *n*), where

i is the lane number
m is an index indicating the FEC codeword number and increments at the start of each codeword
n is an index indicating the bit number within a codeword with a range 1 to 1360

The start of a codeword is determined by the start parameter associated with the tx_bit parameter being equal to TRUE.

94.2.2.2 Overhead Frame

The PMA transmit process shall create a sequence of overhead frames by inserting 40 overhead bits for every 31280 FEC bits as specified in this subclause.

The FEC bits, F(*i*, *m*, *n*), are mapped into a continuous sequence of overhead frames. The overhead frame is 31320 bits in length.

Each bit in the overhead frame is denoted V(*i*, *p*, *q*), where:

i is the lane number
p is an index that indicates the frame number and increments at the start of each frame
q is an index that indicates the bit number within a frame with a range 1 to 31320

The first 40 bits of the frame, V(*i*, *p*, 1) to V(*i*, *p*, 40), are the overhead bits (see 94.2.2.3). The next 31280 bits, V(*i*, *p*, 41) to V(*i*, *p*, 31320), are composed of the bits from 23 consecutive FEC codewords.

The overhead bits are inserted in the frame as follows:

V(*i*, *p*, 1) = H(*i*, *p*, 1)
V(*i*, *p*, 2) = H(*i*, *p*, 2)
V(*i*, *p*, ...) = H(*i*, *p*, ...)
V(*i*, *p*, 40) = H(*i*, *p*, 40)

The FEC codeword bits are aligned such that V(*i*, *p*, 41) is the first bit of a codeword, e.g., V(*i*, *p*, 41) = F(*i*, *m*, 1). The FEC bits are inserted into the frame in the order in which they were received from the FEC, e.g., V(*i*, *p*, 42) = F(*i*, *m*, 2), V(*i*, *p*, 43) = F(*i*, *m*, 3), and so on. The method for aligning the FEC codeword with the start of the overhead frame is outside the scope of this standard.

94.2.2.3 Overhead

The PMA transmit process shall form the overhead bits in each overhead frame as specified in this subclause.

The overhead bits are denoted H(*i*, *p*, *k*), where

i is the lane number
p is an index that indicates the frame number and increments at the start of each frame
k is an index that indicates the header bit number with a range 1 to 40

Bits are mapped to the overhead in a sequence of five groups of 8 bits each. Each 8-bit group takes on the value A or An. The values of the 8 bits in A are such that A(7:0) = TX_OH_pattern(7:0). The values of the 8 bits in An are such that each bit is the inverse of the corresponding bit in A. For each lane i, the sequence

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of 8-bit groups is according to the bits in TX_OH_sequence_i(4:0) such that H(*i*,*p*,((*a*+1)*8):(*a**8+1)) is equal to A(7:0) or An(7:0) if TX_OH_sequence_i(*a*) is equal to 0 or 1, respectively, where a ∈ {0,1,2,3,4}.

If the optional Clause 45 MDIO is implemented, the overhead function maps the TX_OH_pattern and TX_OH_sequence_i status variables to the registers and bits defined in 94.2.10. The default values for each of the variables are summarized in Table 94–2.

Table 94–2—Default overhead configuration values

Parameter	Values (binary)
TX_OH_pattern(7:0)	01100110
TX_OH_sequence_0(4:0)	00110
TX_OH_sequence_1(4:0)	01010
TX_OH_sequence_2(4:0)	10101
TX_OH_sequence_3(4:0)	11001

94.2.2.4 Termination Blocks

The PMA transmit process shall create a sequence of termination blocks by inserting two termination bits for every 90 overhead frame bits as specified in this subclause. The termination block is 92 bits in length. The overhead frame mapped into 348 consecutive termination blocks forms a PMA frame.

Each bit in a termination block is denoted T(*i*, *r*, *s*), where:

i is the lane number
r is an index indicating block number and increments at the start of each block
s is an index indicating the bit number within a termination block with a range 1 to 92

The first two bits in each termination block, T(*i*, *r*, 1) and T(*i*, *r*, 2), are populated with the output of a PRBS13 generator of the form specified in 94.3.10.8. For each termination block, the PRBS13 generator generates a block of 92 pseudo-random bits, R(*i*,1:92). The first two bits are used for the termination bits such that T(*i, r,* 1)=R(*i*, 1) and T(*i, r*, 2)=R(*i*, 2). The PRBS13 generator is initialized during training (94.3.10.8). Upon the transition from the last training frame to the first PMA frame the PRBS13 generator used during training advances without reseeding (see 94.3.10.7.2) and without inversion, and the output is used to generate the termination bits. The PRBS13 generator continues to advance without reseeding and without inversion.

The remaining 90 bits of each termination block, T(*i*, *r*, 3) to T(*i*, *r*, 92), are overhead frame bits (see 94.2.2.2). The overhead frame bits are aligned with the termination blocks such that the first overhead bit, V(*i*, *p*, 1), corresponds to the third bit of a termination block, T(*i*, *r*, 3).

Overhead frame bits are mapped to the termination blocks in order of location within the overhead frame, e.g., T(*i*, *r*, 4) = V(*i*, *p*, 2), T(*i*, *r*, 5) = V(*i*, *p*, 3), and so on.

The termination bit PRBS13 generator is initialized during the training process. When training is complete the state of the termination bit PRBS13 generator is retained and the resulting output is used for the termination bits in the PMA frame.

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94.2.2.5 Gray Mapping

The PMA transmit process shall map consecutive pairs of bits to one of four Gray-coded symbols as specified in this subclause.

Each pair of bits, {A, B}, of each termination block are converted to a Gray-coded symbol with one of the four Gray-coded levels as follows:

{0, 0} maps to 0,
{0, 1} maps to 1,
{1, 1} maps to 2, and
{1, 0} maps to 3.

Gray-coded symbols corresponding to each termination block are denoted G(i, r, t), where:

i is the lane number
r is an index indicating the termination block number
t is an index indicating the symbol number within a termination block with a range 1 to 46

Pairing of bits is such that the first two bits of each termination block, T(i, r, 1) and T(i, r, 2), form a pair. Each bit pair {T(i, r, 2t–1), T(i, r, 2t)} maps to {A, B} and the Gray-coded result is assigned to G(i, r, t). The Gray-coded symbol G(i, r, 1) is formed from the first two bits of a termination block, the termination bits, thus forming a termination symbol.

94.2.2.6 Precoding

The PMA transmit process shall precode the Gray-coded symbols as specified in this subclause.

The precoder output symbols are denoted, P(i, r, t), where:

i is the lane number
r is an index indicating the termination block number
t is an index indicating the symbol number within a termination block with a range 1 to 46.

For each Gray-coded symbol G(i, r, t), a precoded symbol, P(i, r, t) is determined by the following algorithm:

If t = 1 then
    P(i, r, t) = G(i, r, t)
Else
    P(i, r, t) = (G(i, r, t) – P(i, r, t–1)) mod 4
End If

The bits contributing to the Gray-coded termination symbol, G(i, r, 1), are the termination bits. The precoding algorithm applies this symbol directly to the output rather than combining it with the previous non-deterministic symbols and thus this termination symbol is always deterministic.

94.2.2.7 PAM4 encoding

The PMA transmit process shall encode each precoder output symbol to one of four PAM4 levels as specified in this subclause.

The PAM4 encoded symbols are denoted M(i, u), where

i is the lane number
u is an index indicating the symbol number

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Each consecutive precoder output symbol, P(*i*, *r*, *t*), is mapped to one of four PAM4 levels and assigned to the PAM4 encoder output M(*i*, u).

Mapping from the precoder output symbol P(*i*, *r*, *t*) to a PAM4 encoded symbol M(*i*, *u*) is as follows:

0 maps to –1,
1 maps to –1/3,
2 maps to +1/3, and
3 maps to +1.

94.2.2.8 PMD Interface

The PMA transmit process shall transmit each PAM4 encoded symbol, M(*i*, *u*) to the PMD via the PMD:IS_UNITDATA_*i*(tx_symbol) primitive at a symbol transfer rate of 13.59375 GBd.

94.2.3 PMA Receive Functional Specifications

The receive process shall recover the data encoded by the transmit process meeting the performance requirements specified in 94.1 after the overhead and termination bits have been removed.

The process by which the receiver recovers the data to meet this requirement is outside the scope of this standard. The signal structure encoded by the transmitter process including the overhead bits, Gray coding, and termination symbols may be leveraged by the receiver implementation at the discretion of the implementer. The remainder of this subclause specifies the receiver processes to reverse the transmitter encoding and report status.

In the received direction, the role of the 100GBASE-KP4 PMA is to adapt the PAM4 encoded signal from the PMD to an FEC encoded signal to be passed to the FEC for further processing. The adaptation processes shown in Figure 94–3 include PAM4 decoding, (1+D) mod 4 decoding, inverse Gray coding, remove termination bits, and remove overhead.

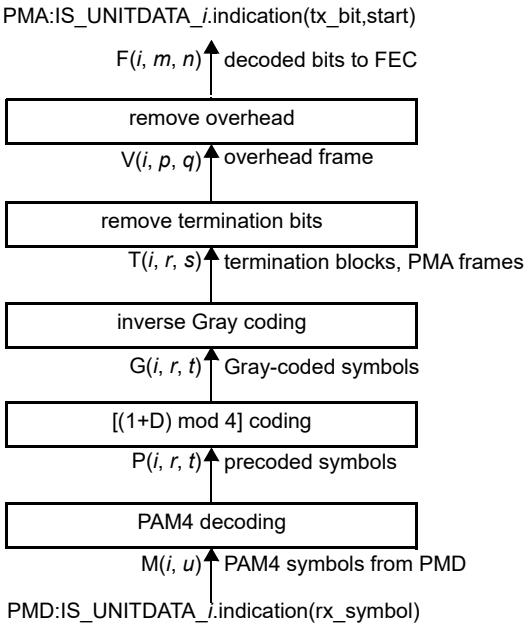

Figure 94–3—Receive adaptation process diagram

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94.2.3.1 Overhead

The PMA receive process shall decode the overhead bits in each overhead frame as specified in this subclause. The format of the overhead bits is specified in 94.2.2.3.

The receive process decodes the received overhead bits in a sequence of five groups of 8 bits each into a sequence of 5 bits. Each group of 8 bits is compared with A and An, where A(7:0) = RX_OH_pattern(7:0) and the values of the 8 bits in An are such that each bit is the inverse of the corresponding bit in A. A match of each 8-bit group with A or An results in a decoded value of 0 or 1, respectively. The decoded value when the 8-bit group matches neither A or An is not specified. The decoded values from H(*i*,*p*,((*a*+1)*8):(*a**8+1)) are assigned to RX_OH_sequence_i(*a*), where $a \in \{0,1,2,3,4\}$. If all of the 8-bit groups match either A or An, the RX_OH_sequence_i(5) is set to 1 and is otherwise set to 0.

If the optional Clause 45 MDIO is implemented, the PMA receive process maps the RX_OH_pattern and RX_OH_sequence_i variables to the registers and bits defined in 94.2.10. The default values for each of the control variables are summarized in Table 94–3.

Table 94–3—Default overhead control values

Parameter	Values (binary)
RX_OH_pattern(7:0)	01100110

94.2.4 Skew constraints

Skew considerations for the 100GBASE-KP4 PMA, PMD, and AN are specified in 94.3.4.

94.2.5 Delay constraints

Delay considerations for the 100GBASE-KP4 PMA, PMD, AN, and medium are specified in 94.3.3.

94.2.6 Link status

The PMA shall provide link status information to the PMA client using the PMA:IS_SIGNAL.indication primitive (see 94.2.1.3). The PMA continuously monitors the link status reported by the PMD from the PMD:IS_SIGNAL.indication primitive, and uses this as input to Signal Indication Logic (SIL) to determine the link status to report to the PMA client. Other inputs to the SIL may include status of clock and data recovery on the lanes from the PMD and frame synchronization.

94.2.7 PMA local loopback mode

PMA local loopback shall be provided. This function involves looping back each input lane from the PMA service interface to the corresponding output lane on the PMA service interface. Each received instance of the PMA:IS_UNITDATA_*i*.request(tx_bit,start) primitive is looped back in the direction of the PMA client using the PMA:IS_UNITDATA_*i*.indication(rx_bit,start) primitive.

During local loopback, the PMA performs normal framing and precoding onto the lanes in the Tx direction toward the PMD service interface.

Ability to perform this function is indicated by the Local_loopback_ability status variable. The Local_loopback_ability status variable is always set to 1. If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.8.0 (45.2.1.7.15). A device is placed in local loopback mode when the

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Local_loopback_enable control variable is set to one, and removed from local loopback mode when this variable is set to zero. If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD control 1 register (bit 1.0.0, see 45.2.1.1.5).

94.2.8 PMA remote loopback mode (optional)

PMA remote loopback mode is optional. If implemented, it shall be as described in this subclause.

Remote loopback, if provided, should be implemented close enough to the PMD to maintain the bit sequence on each individual PMD lane. When remote loopback is enabled, each bit received over a lane of the service interface below the PMA via PMD:IS_UNITDATA_*i*.indication is looped back to the corresponding output lane toward the PMD via PMD:IS_UNITDATA_*i*.request.

During remote loopback, the PMA performs normal bit processing operation in the Rx direction towards the PMA client.

The ability to perform this function is indicated by the Remote_loopback_ability status variable. If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.13.15 (Clause 45.2.1.2.3). A device is placed in remote loopback mode when the Remote_loopback_enable control variable is set to one, and removed from remote loopback mode when this variable is set to zero. If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD Control register 1 (bit 1.0.1, see Clause 45.2.1.1.4).

94.2.9 PMA test patterns

94.2.9.1 JP03A test pattern

A 100GBASE-KP4 PMA shall include a JP03A test pattern generator as specified in this subclause.

The JP03A test pattern is generated prior to PAM4 encoding. When the JP03A test pattern is enabled, it replaces the signal from the precoder. The JP03A test pattern is a repeating {0,3} sequence.

The JP03A test pattern is enabled by the test_pattern_enable and JP03A_enable control variables. If the optional Clause 45 MDIO is implemented, the control variables map to the registers and bits defined in 94.2.10.

94.2.9.2 JP03B test pattern

A 100GBASE-KP4 PMA shall include a JP03B test pattern generator as specified in this subclause.

The JP03B test pattern is generated prior to PAM4 encoding. When the JP03B test pattern is enabled, it replaces the signal from the precoder. The JP03B test pattern is a repeating sequence of {0,3} repeated 15 times followed by {3,0} repeated 16 times. The entire 62-symbol pattern is shown in Equation (94–1).

$$03030303030303030303030303033030303030303030303030303030303030 \quad (94–1)$$

The JP03B test pattern is enabled by the test_pattern_enable and JP03B_enable control variables. If the optional Clause 45 MDIO is implemented, the control variables map to the registers and bits defined in 94.2.10.

94.2.9.3 Quaternary PRBS13 test pattern

A 100GBASE-KP4 PMA shall include a quaternary PRBS13 (QPRBS13) pattern generator as specified in this subclause.

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The QPRBS13 test pattern is a repeating 15548-symbol (338 training frame words) sequence equivalent to the training pattern specified in 94.3.10.8.

The PRBS13 pattern generator is re-initialized for each repetition of QPRBS13 with the same seeds specified in Table 94–11.

The QPRBS13 test pattern is enabled by the test_pattern_enable and QPRBS13_enable control variables. If the optional Clause 45 MDIO is implemented, the control variables map to the registers and bits defined in 94.2.10.

94.2.9.4 Transmitter linearity test pattern

A 100GBASE-KP4 PMA shall include a transmitter linearity test pattern generator as specified in this subclause.

The transmitter linearity test pattern is a repeating 160-symbol pattern with a sequence of 10 symbol values each 16 UI in duration. The 10 values correspond to the set of PAM4 symbols shown in Equation (94–2).

$$\{-1,-1/3,+1/3,+1,-1,+1,-1,+1,+1/3,-1/3\} \quad (94–2)$$

The transmitter linearity test pattern is enabled by the test_pattern_enable and TX_linearity_enable control variables. If the optional Clause 45 MDIO is implemented, the control variables map to the registers and bits defined in 94.2.10.

94.2.10 PMA MDIO function mapping

Clause 45 specifies the optional MDIO capability that describes several registers that provide control and status information for and about the PMA. 45.2.1 describes the Management Data Input/Output (MDIO) Manageable Device (MMD) addresses. If MDIO is implemented, it shall map MDIO control bits to PMA control variables as shown in Table 94–4, and MDIO status bits to PMA status variables as shown in Table 94–5.

Table 94–4—100GBASE-KP4 MDIO/PMA control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMA control variable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
PMA remote loopback	PMA/PMD status 2	1.0.1	Remote_loopback_enable
PMA Tx generator enable	PRBS pattern testing control	1.1501.3	test_pattern_enable
JP03A pattern enable	PRBS pattern testing control	1.1501.8	JP03A_enable
JP03B pattern enable	PRBS pattern testing control	1.1501.9	JP03B_enable
QPRBS13 pattern enable	PRBS pattern testing control	1.1501.10	QPRBS13_enable
TX linearity pattern enable	PRBS pattern testing control	1.1501.11	TX_linearity_enable
PMA transmit overhead pattern	PMA overhead control 1	1.162.7:0	TX_OH_pattern
PMA transmit overhead sequence 0	PMA overhead control 1	1.162.12:8	TX_OH_sequence_0
PMA transmit overhead sequence 1	PMA overhead control 2	1.163.4:0	TX_OH_sequence_1

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Table 94–4—100GBASE-KP4 MDIO/PMA control variable mapping *(continued)*

MDIO control variable	PMA/PMD register name	Register/bit number	PMA control variable
PMA transmit overhead sequence 2	PMA overhead control 2	1.163.9:5	TX_OH_sequence_2
PMA transmit overhead sequence 3	PMA overhead control 2	1.163.14:10	TX_OH_sequence_3
PMA receive overhead pattern	PMA overhead control 3	1.164.7:0	RX_OH_pattern

Table 94–5—100GBASE-KP4 MDIO/PMA status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMA status variable
PMA local loopback ability	PMA/PMD status 2	1.8.0	Local_loopback_ability
PMA remote loopback ability	40G/100G PMA/PMD extended ability	1.13.15	Remote_loopback_ability
PMA receive overhead sequence 0	PMA overhead status 1	1.165.5:0	RX_OH_sequence_0
PMA receive overhead sequence 1	PMA overhead status 1	1.165.11:6	RX_OH_sequence_1
PMA receive overhead sequence 2	PMA overhead status 2	1.166.5:0	RX_OH_sequence_2
PMA receive overhead sequence 3	PMA overhead status 2	1.166.11:6	RX_OH_sequence_3

94.3 Physical Medium Dependent (PMD) Sublayer

94.3.1 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-KP4 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data. The PMD translates the encoded data to and from signals suitable for the medium.

The PMD service interface is based on the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

If the optional EEE deep sleep capability is supported, then the PMD service interface includes two additional primitives as follows:

PMD:IS_TX_MODE.request
PMD:IS_RX_MODE.request

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94.3.1.1 PMD:IS_UNITDATA_i.request

The PMD:IS_UNITDATA_*i*.request (where *i*=0 to 3) primitive is used to define the transfer of four streams of data units from the PMA to the PMD.

94.3.1.1.1 Semantics of the service primitive

PMD:IS_UNITDATA_0.request(tx_symbol)
PMD:IS_UNITDATA_1.request(tx_symbol)
PMD:IS_UNITDATA_2.request(tx_symbol)
PMD:IS_UNITDATA_3.request(tx_symbol)

The data conveyed by PMD:IS_UNITDATA_i.request consists of four parallel continuous streams of encoded symbols, tx_symbol, one stream for each lane. Each of the tx_symbol parameters can take one of four values: –1, –1/3, +1/3, or +1.

94.3.1.1.2 When generated

The PMA continuously sends four parallel symbol streams PMD:IS_UNITDATA_*i*.request(tx_symbol) to the PMD, each at a nominal signaling rate of 13.59375 GBd.

94.3.1.1.3 Effect of receipt

Upon receiving each instance of PMD:IS_UNITDATA_*i*.request, the tx_symbol parameter is passed to the PMD transmit process corresponding to each stream.

94.3.1.2 PMD:IS_UNITDATA_i.indication

The PMD:IS_UNITDATA_*i*.indication (where *i*=0 to 3) primitive is used to define the transfer of four streams of data units from the PMD to the PMA.

94.3.1.2.1 Semantics of the service primitive

PMD:IS_UNITDATA_0.indication(rx_symbol)
PMD:IS_UNITDATA_1.indication(rx_symbol)
PMD:IS_UNITDATA_2.indication(rx_symbol)
PMD:IS_UNITDATA_3.indication(rx_symbol)

The data conveyed by PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication consists of four parallel continuous streams of encoded symbols, one stream for each lane. Each of the rx_symbol parameters can take one of four values: –1, –1/3, +1/3, or +1.

94.3.1.2.2 When generated

The PMD continuously sends four parallel encoded symbol streams PMD:IS_UNITDATA_*i*.indication(rx_symbol) to the PMD client, each at a nominal signaling rate of 13.59375 GBd.

94.3.1.2.3 Effect of receipt

The effect of receipt of this primitive is undefined by the PMD.

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94.3.1.3 PMD:IS_SIGNAL.indication

The PMD:IS_SIGNAL.indication primitive is generated by the PMD to the PMA to indicate the status of the PMD receive process. This primitive is generated by the PMD receive process to propagate the detection of severe error conditions (e.g., loss of synchronization) to the PMA.

94.3.1.3.1 Semantics of the service primitive

PMD:IS_SIGNAL.indication(SIGNAL_OK).

The SIGNAL_OK parameter corresponds to the variable Global_PMD_signal_detect as defined in 94.3.6.4. When Global_PMD_signal_detect is one, SIGNAL_OK shall be assigned the value OK. When Global_PMD_signal_detect is zero, SIGNAL_OK shall be assigned the value FAIL. When SIGNAL_DETECT = FAIL, the PMD:IS_UNITDATA_*i*.indication parameters are undefined.

94.3.1.3.2 When generated

The PMD generates the PMD:IS_SIGNAL.indication primitive to the PMD client whenever there is change in the value of the Global_PMD_signal_detect parameter.

94.3.1.3.3 Effect of receipt

The effect of receipt of this primitive is undefined by the PMD.

94.3.2 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 82.6.)

The 100GBASE-KP4 PHY may be extended using CAUI-n as a physical instantiation of the inter-sublayer service interface between devices. If CAUI-n is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementer. As examples, the implementer may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

94.3.3 Delay constraints

The sum of the transmit and the receive delays contributed by the 100GBASE-KP4 PMA, PMD, AN, and the medium in one direction shall be no more than 8192 bit times (16 pause_quanta or 81.92 ns). It is assumed that the one way delay through the medium is no more than 800 bit times (8 ns).

A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

94.3.4 Skew constraints

The Skew (relative delay) between the lanes is kept within limits so that the information on the lanes can be reassembled by the RS-FEC sublayer. Skew and Skew Variation are defined in 80.5 and specified at the points SP1 to SP6 shown in Figure 80–9.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 0.4 ns.

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The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 0.6 ns.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5.

94.3.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control bits to PMD control variables as shown in Table 94–6, and MDIO status bits to PMD status variables as shown in Table 94–7.

Table 94–6—100GBASE-KP4 MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 3 to PMD transmit disable 0	PMD transmit disable	1.9.4 to 1.9.1	PMD_transmit_disable_3 to PMD_transmit_disable_0
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable

Table 94–7—100GBASE-KP4 MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 0	PMD receive signal detect	1.10.4 to 1.10.1	PMD_signal_detect_3 to PMD_signal_detect_0
100GBASE-KP4 deep sleep	EEE capability	1.16.9	—
Receiver status 3	BASE-R PMD status	1.151.12	rx_trained_3
Frame lock 3	BASE-R PMD status	1.151.13	frame_lock_3

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Table 94–7—100GBASE-KP4 MDIO/PMD status variable mapping *(continued)*

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Startup protocol status 3	BASE-R PMD status	1.151.14	training_3
Training failure 3	BASE-R PMD status	1.151.15	training_failure_3
Receiver status 2	BASE-R PMD status	1.151.8	rx_trained_2
Frame lock 2	BASE-R PMD status	1.151.9	frame_lock_2
Startup protocol status 2	BASE-R PMD status	1.151.10	training_2
Training failure 2	BASE-R PMD status	1.151.11	training_failure_2
Receiver status 1	BASE-R PMD status	1.151.4	rx_trained_1
Frame lock 1	BASE-R PMD status	1.151.5	frame_lock_1
Startup protocol status 1	BASE-R PMD status	1.151.6	training_1
Training failure 1	BASE-R PMD status	1.151.7	training_failure_1
Receiver status 0	BASE-R PMD status	1.151.0	rx_trained_0
Frame lock 0	BASE-R PMD status	1.151.1	frame_lock_0
Startup protocol status 0	BASE-R PMD status	1.151.2	training_0
Training failure 0	BASE-R PMD status	1.151.3	training_failure_0

94.3.6 PMD functional specifications

94.3.6.1 Link block diagram

One direction for one lane of a 100GBASE-KP4 link is shown in Figure 94–4.

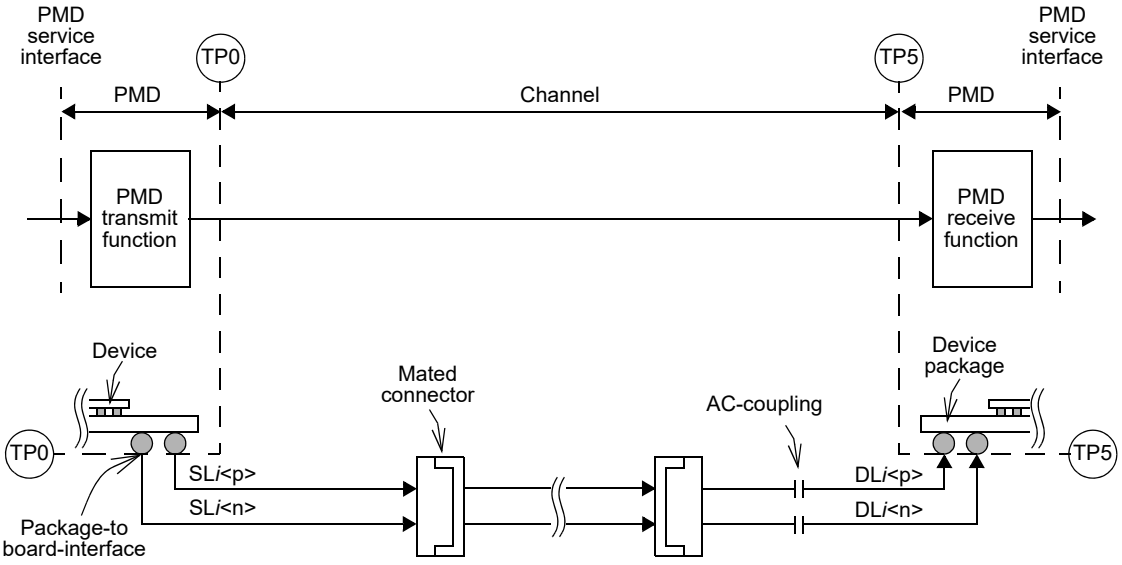

Figure 94–4—100GBASE-KP4 link (one direction for one lane is illustrated)

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94.3.6.2 PMD Transmit function

The PMD transmit function shall convert the four encoded symbol streams requested by the PMD service interface messages PMD:IS_UNITDATA_i.request (i=0 to 3) into four separate electrical signals. The four electrical signals shall then be delivered to the MDI, all according to the transmit electrical specifications in 94.3.12. A positive differential output voltage (SL*i*<p> minus SL*i*<n>) shall correspond to a positive tx_symbol value.

If the optional EEE deep sleep capability is supported, the PMD transmit function shall transmit a periodic sequence, where each period of the sequence is an ALERT frame (see 94.3.11.1) when tx_mode is set to ALERT. Regardless of tx_mode, the transmit equalizer coefficients shall be set to the values determined via the startup protocol (see 94.3.10).

94.3.6.3 PMD Receive function

The PMD receive function shall convert the four electrical signals from the MDI into four encoded symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_i.indication (i=0 to 3). A positive differential input voltage of (DL*i*<p> minus DL*i*<n>) shall correspond to a positive rx_symbol value.

94.3.6.4 Global PMD signal detect function

The variable Global_PMD_signal_detect is the logical AND of the values of PMD_signal_detect_i for i=0 to 3.

When the MDIO is implemented, this function maps the variable Global_PMD_signal_detect to the register and bit specified in 94.3.5.

94.3.6.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal detect function is used by the 100GBASE-KP4 PMD to indicate the successful completion of the startup protocol by the PMD control function (see 94.3.10). PMD_signal_detect_i (where i represents the lane number in the range 0 to 3) is set to zero when the value of the variable signal_detect is set to false by the Training state diagram for lane i (see Figure 72–5). PMD_signal_detect_i is set to one when the value of signal_detect for lane i is set to true.

If training is disabled by the management variable mr_training_enable (see 94.3.5), PMD_signal_detect_i shall be set to one for i=0 to 3.

If the optional EEE deep sleep capability is supported, the following requirements apply. The value of PMD_signal_detect_i (for i=0 to 3) is set to zero when rx_mode is first set to QUIET. While rx_mode is set to QUIET, PMD_signal_detect_*i* shall be set to one within 500 ns of the application of the ALERT pattern defined in 94.3.6.2 and meeting the EEE transmit-enabled amplitude requirement of 94.3.12.3. While rx_mode is set to QUIET, PMD_signal_detect_*i* shall not be set to one when the output of the transmitter on the same lane meets the EEE transmit-disabled amplitude requirement of 94.3.12.3.

When the MDIO is implemented, this function maps the variables to registers and bits as defined in 94.3.5.

94.3.6.6 Global PMD transmit disable function

The Global PMD transmit disable function is mandatory if EEE deep sleep capability is supported and is otherwise optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

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a) When Global_PMD_transmit_disable variable is set to one, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage in Table 94–13.

b) If a PMD fault (94.3.7) is detected, then the PMD may set Global_PMD_transmit_disable to one.

c) Loopback, as defined in 94.3.6.8, shall not be affected by Global_PMD_transmit_disable.

d) The following additional requirements apply when the optional EEE deep sleep capability is supported. The Global PMD transmit disable function shall turn off all of the transmitters as specified in 94.3.12.3 when tx_mode transitions to QUIET from any other value. The Global PMD transmit disable function shall turn on all of the transmitters as specified in 94.3.12.3 when tx_mode transitions from QUIET to any other value.

94.3.6.7 PMD lane-by-lane transmit disable function

The PMD lane-by-lane transmit disable function is optional and allows the electrical transmitter in each lane to be selectively disabled. When this function is supported, it shall meet the following requirements:

a) When a PMD_transmit_disable_*i* variable (where i represents the lane number in the range 0 to 3) is set to one, this function shall turn off the transmitter associated with that variable such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 94–13.

b) If a PMD_fault (94.3.7) is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the electrical transmitter in each lane.

c) Loopback, as defined in 94.3.6.8, shall not be affected by PMD_transmit_disable_*i.*

94.3.6.8 Loopback mode

Local loopback mode is provided by the PMA (94.2.7). Loopback shall not affect the state of the transmitter, which continues to send data unless disabled (94.3.6.7).

NOTE—Placing a network port into loopback mode can be disruptive to a network.

94.3.7 PMD fault function

PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault.

If the MDIO is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

94.3.8 PMD transmit fault function

The PMD transmit fault function is optional. The faults detected by this function are implementation specific, but the assertion of Global_PMD_transmit_disable is not considered a transmit fault. A fault is indicated by setting the variable PMD_transmit_fault to one.

If PMD_transmit_fault is asserted, then Global_PMD_transmit_disable should also be asserted.

If the MDIO interface is implemented, then this function shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

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94.3.9 PMD receive fault function

The PMD receive fault function is optional. The faults detected by this function are implementation specific. A fault is indicated by setting the variable PMD_receive_fault to one.

If the MDIO interface is implemented, then PMD_receive_fault shall contribute to the Receive fault bit as specified in 45.2.1.7.5.

94.3.10 PMD control function

94.3.10.1 Overview

The PMD control function generates the control actions required to bring the PMD from initialization to a mode in which data may be exchanged with the link partner.

The PMD control function is based upon the 10GBASE-KR startup protocol. This protocol facilitates timing recovery and equalization while also providing a mechanism through which the receiver can tune the transmit equalizer to optimize performance over the backplane interconnect. The protocol supports these mechanisms through the continuous exchange of fixed-length training frames.

Each lane of the 100GBASE-KP4 PMD shall have an independent control function as defined in this subclause.

The variables rx_trained_*i*, frame_lock_*i*, training_*i,* and training_failure_*i* (where *i* goes from 0 to 3) report status for each lane and are equivalent to rx_trained, frame_lock, training, and training_failure as defined in 72.6.10.3.1. If the MDIO interface is implemented, then this function shall map these variables to the appropriate bits in the BASE-R PMD status register (register 1.151) as specified in 45.2.1.96.

94.3.10.2 Training frame structure

The training frame is a fixed length structure that is sent continuously during training. The training frame, shown in Figure 94–5, is 348 training frame words (94.3.10.3) in length and contains a frame marker, a control channel, and training pattern. The frame marker delimits the beginning of a training frame. The control channel provides a means for the each receiver to control the taps on the link partner transmitter and communicate status. The training pattern provides content rich pattern for receiver convergence.

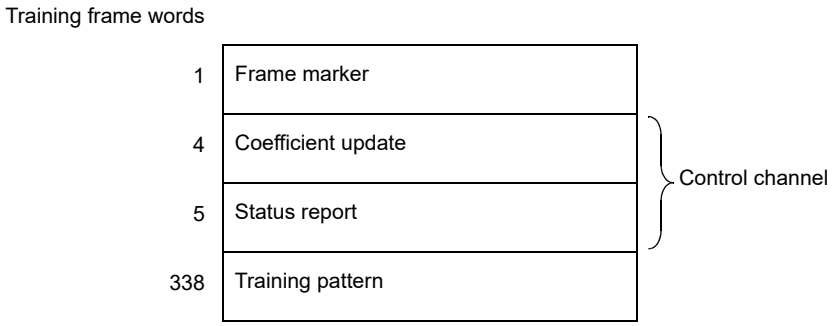

Figure 94–5—Training frame structure

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94.3.10.3 Training frame words

Each training frame is composed of a series of 348 training frame words. Each training frame word is 46 symbols in length, equivalent in size to a termination block described in 94.2.2.4.

94.3.10.4 Frame marker

Each training frame shall be delimited by a frame marker as described in this subclause. The frame marker is a training frame word composed of a 46-symbol pattern of 23 +1 symbols followed by 23 –1 symbols. This pattern does not appear in the control channel or the training pattern and therefore serves as a unique indicator of the start of a training frame.

94.3.10.5 Control channel encoding

94.3.10.5.1 Differential Manchester encoding

The control channel shall be transmitted using differential Manchester encoding (DME). DME guarantees transition density and DC balance while the reduced rate of transmission facilitates reception over non-optimally equalized channels.

DME cells shall be encoded using the following rules:

a) Each DME cell represents one bit of information.
b) The upper value is represented by a series of PAM4 +1 symbols.
c) The lower value is represented by a series of PAM4 –1 symbols.
d) A data transition occurs at each cell boundary.
e) A mid-cell data transition is used to signal a logical one.
f) The absence of a mid-cell data transition is used to signal a logical zero.

If a coding violation is detected within the bounds of the control channel in a given training frame, the contents of the control channel for that frame shall be ignored.

94.3.10.5.2 Control channel structure

The control channel shall be constructed of a series of DME cells as described in this subclause.

The control channel is composed of a series of 9 training frame words. Each training frame word is composed of four 10-symbol control channel DME cells and a 6-symbol control overhead DME cell.

The control overhead cell is always transmitted as a one following the DME rules. In other words, the control overhead cell is transmitted as either three +1 symbols followed by three –1 symbols or vice versa depending on the previously transmitted control channel cell.

The coefficient update field is transmitted in the first 16 control channel DME cells. The status report field is transmitted in the next 24 control channel DME cells. The structure of the frame marker and control channel are shown in Table 94–8.

94.3.10.6 Coefficient update field

The coefficient update field carries correction information from the local receiver to the link partner transmit equalizer. The field consists of preset controls, initialization controls, coefficient updates for three transmit equalizer taps, and parity. The coefficient update field is mapped into the first 16 control channel DME

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Table 94–8—Frame marker and control channel structure

Training frame word	Symbols 1:10	Symbols 11:20	Symbols 21:30	Symbols 31:40	Symbols 41:46	Training frame fields
1	cell 15	cell 14	cell 13	cell 12	overhead	coefficient update
2	cell 11	cell 10	cell 9	cell 8	overhead	
3	cell 7	cell 6	cell 5	cell 4	overhead	
4	cell 3	cell 2	cell 1	cell 0	overhead	
5	cell 19	cell 18	cell 17	cell 16	overhead	status report
6	cell 15	cell 14	cell 13	cell 12	overhead	
7	cell 11	cell 10	cell 9	cell 8	overhead	
8	cell 7	cell 6	cell 5	cell 4	overhead	
9	cell 3	cell 2	cell 1	cell 0	overhead	

The format of the coefficient update field shall be as shown in Table 94–9. Cell 15 of the coefficient update field shall be transmitted first. The preset, initialize, and coefficient update fields are set by the receiver adaptation process. The algorithm employed by the receiver adaptation process is beyond the scope of this standard.

Table 94–9—Coefficient update field

Cell(s)	Name	Description
15:14	Reserved	Transmitted as 0, ignored on reception.
13	Preset	1 = Preset coefficients 0 = Normal operation
12	Initialize	1 = Initialize coefficients 0 = Normal operation
11:7	Reserved	Transmitted as 0, ignored on reception.
6	Parity	Even parity of all other coefficient update cells.
5:4	Coefficient (+1) update	5 4 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold
3:2	Coefficient (0) update	3 2 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold
1:0	Coefficient (–1) update	1 0 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold

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94.3.10.6.1 Preset

The behavior in response to the preset field shall be as specified in 72.6.10.2.3.1.

94.3.10.6.2 Initialize

The behavior in response to the initialize field shall be as specified in 72.6.10.2.3.2, except that the conditions for the INITIALIZE state are specified in 94.3.12.5.4 instead of 72.6.10.4.2.

94.3.10.6.3 Parity

The parity bit shall be set so that all bits in the coefficient update field including the parity bit exhibit even parity. The parity bit protects against acceptance of errored control messages and preserves DC balance. If a parity violation is detected within a received coefficient update field, that field shall not be used to update the transmitter coefficients.

94.3.10.6.4 Coefficient (*k*) update

The coefficient update fields shall be encoded as described in this subclause.

Each coefficient, identified by the index k, is assigned a 2-bit field describing a requested update, where $k \in \{-1, 0, 1\}$ denoting the pre-cursor, main, and post-cursor taps, respectively. The encoding of the coefficient update fields are as shown in Table 94–9.

Three request encodings are defined: increment, decrement, and hold. The default state of each tap is hold, which corresponds to no change in the coefficient. The increment or decrement encodings are transmitted to request that the corresponding coefficient be increased or decreased. The amount of change implemented by the transmitter in response to the coefficient update request meets the requirements of 94.3.12.5.5. An increment or decrement request is transmitted continuously until the update status (94.3.10.7.4) for that tap indicates updated, maximum, or minimum. At that point, the outgoing requests for that tap may be set to hold. The hold setting has to be maintained until the incoming status message for that tap reverts to not_updated. A new request to increment or decrement a tap may be sent only when the incoming status message for that tap is not_updated.

Coefficient increment and decrement update requests are not sent in combination with initialize or preset.

94.3.10.7 Status report field

The status report field is used to signal state information from the local PMD to the link partner. The format of the status report field of training frames shall be as shown in Table 94–10. Cell 19 of the status report field shall be transmitted first.

Table 94–10—Status report field for training and alert frames

Cell(s)	Name	Description
19	Parity	Set to achieve even parity for status report field.
18	Mode	0: Training 1: EEE
17:16	Frame countdown	Number of frames remaining before transition to data mode.

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Table 94–10—Status report field for training and alert frames *(continued)*

Cell(s)	Name	Description
15:13	PMA alignment offset	Relative location of the next alert frame within the PMA frame (set to zero for training frames).
12:7	Reserved	Transmitted as zeros.
6	Receiver ready	1 = The local receiver has determined that training is complete and is prepared to receive data. 0 = The local receiver is requesting that training continue.
5:4	Coefficient (+1) status	5 4 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated (and for EEE alert frames)
3:2	Coefficient (0) status	3 2 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated (and for EEE alert frames)
1:0	Coefficient (–1) status	1 0 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated (and for EEE alert frames)

94.3.10.7.1 Parity

The parity cell shall be set so that all bits in the status report field including the parity bit exhibit even parity. The parity bit protects against acceptance of errored status messages and preserves DC balance. If a parity violation is detected within a received status field, that field shall not be used to determine the link partner status.

94.3.10.7.2 Training frame countdown

The training frame countdown cell shall signal the transition from training to data mode as described in this subclause. When training begins, countdown is set to the value 3 and remains so until all receivers have completed training. When the received status report receiver ready is 1 in all four received lanes and the transmitted status report receiver ready is 1 in all four transmitted lanes, the transmitter on each transmitted lane decrements the countdown in three successive frames. The countdown values are equal in all four lanes. In other words, in the last three training frames countdown contains 2, 1, and 0, respectively. Immediately after the last training frame word of the last training frame is sent, transmission of the PMA frame begins starting with the termination block containing the PMA overhead (see 94.3.10.9).

94.3.10.7.3 Receiver ready

The receiver ready bit shall signal the local receiver state to the link partner as described in this subclause. When training begins the receiver ready bit is deasserted and remains so until the receiver has concluded training. The receiver ready bit is asserted to indicate that the local receiver has concluded training and is prepared to receive data. The encoding of the receiver ready bit is as shown in Table 94–10.

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94.3.10.7.4 Coefficient (*k*) status

The behavior of the coefficient (*k*) status fields shall be as specified in 72.6.10.2.4.5.

94.3.10.7.5 Coefficient update process

The coefficient update process shall behave as specified in 72.6.10.2.5.

In addition, the period from receiving a new request to responding to that request shall be less than 2 ms, except during the first 50 ms following the beginning of the startup protocol. The beginning of the startup protocol is defined to be entry into the AN_GOOD_CHECK state in Figure 73–10. The start of the period is the frame marker of the training frame with the new request and the end of the period is the frame marker of the training frame with the corresponding response. A new request occurs when the coefficient update field is different from the coefficient field in the preceding frame. The response occurs when the coefficient status report field is updated to indicate that the corresponding action is complete.

94.3.10.8 Training pattern

The training pattern shall be encoded as specified in this subclause.

The training pattern is mapped into a series of 338 training frame words. Each training frame words is encoded as a PMA signal as specified in 94.2.2 with the exception that the input is from a PRBS13 generator rather than from the PMA service interface and no PMA overhead (94.2.2.2) is inserted.

For each training frame, the PRBS13 generator is used to produce 31096 bits. Three full cycles of 8191 bits and one truncated cycle of 6523 bits are concatenated to form the 31096 bit sequence, R(1:31096). Bits in the first and third cycle, R(1:8191) and R(16383:24573), are not inverted and bits in the second and fourth cycles, R(8192:16382) and R(24574:31096), are inverted.

The PRBS13 pattern generator produces the same result as the implementation shown in Figure 94–6, which implements the generator polynomial shown in Equation (94–3). The PRBS13 pattern generator is initialized for each frame using a unique seed for each lane. The 13-bit seed and the initial 16 bits for each lane are annotated in Table 94–11.

$$G(x) = 1 + x + x^2 + x^{12} + x^{13} \tag{94–3}$$

The PRBS13 pattern is mapped into the 92 bits of each training frame word. The first 2 bits of each training frame word form the termination bits (94.2.2.4) and each training frame word in the training pattern is equivalent to a termination block (94.2.2.4). The resulting termination blocks are Gray-mapped (94.2.2.5), precoded (94.2.2.6), and mapped to PAM4 levels (94.2.2.7).

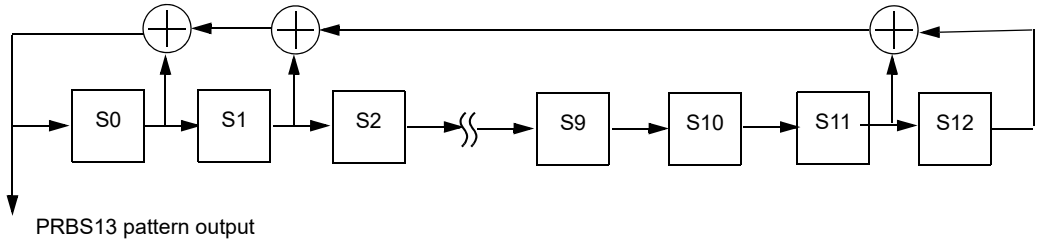

Figure 94–6—PRBS13 pattern generator

The outputs of PRBS13 generator, Gray mapper, and precoder for the first two training frame words are provided in Table 94–12.

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Table 94–11—PRBS13 seeds and initial output

PMD Lane	Seed bits (leftmost bit in S0, rightmost in S12)	Initial 16 bits (in order of transmission)
0	0000010101011	0100100110110011
1	0011101000001	1101111101010100
2	1001000101100	1100101111000011
3	0100010000010	0110111101000111

Table 94–12—Training pattern initial sequences

PMD Lane	Output of	Contents of first (top) and second (bottom) training frame words transmitted left to right
0	PRBS13	0100100110110011110001010101100001001001110111100111010000011 1010011011101001110011001010111 0001111111010111011011111101000101101111101001111011001010110 0111001001110000111100001101011
	Gray code	1031320220111130103121231210012102121023131112 0122211213222101132233123203320231023012301332
	Precoder	1301200200101031003201123322233220110021032320 0111101103333223111210211303311231122330012 11
1	PRBS13	1101111101010100000010010011011001111000101010110000100100111 0111100111010000011101001101110 1001110011001010111000111111101011101101111110100010110111110 1001111011001010110011100100111
	Gray code	2122111000310213123033320031023220233002331323 3120203323022233232122330321221022131113120312
	Precoder	2333232222100230112212113123112022030002123021 3200221203111121120111213023332202301012331233
2	PRBS13	1100101111000011111011101110110011001100111000111000110000110 0001110111000001100110000001110 0011011000011000101011000110010011101010100011001001000011100 1111011101010110011001001010101
	Gray code	2032200223232320202023023020020023230020200023 0213013033201310233330203100231232333202031111
	Precoder	2211131112033022002203112200022203300022000021 0230012212001231121213312313301120303311301010
3	PRBS13	0110111101000111101111101011001101111110001111011010111011110 0100001011000101100101011111000 1001011010111100101001011000100111110000101011010110010011111 1000101011011101001000101111100
	Gray code	1322101232233202122302213323220301130320332230 3113322033113031220033211310222011132331011220
	Precoder	1202310211121133202133321203331223213022120213 3230333121012210200030232100202232302123101113

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94.3.10.9 Transition from training to data

The transmitted signal shall transition from the training signal to normal data as described in this subclause.

The transition from the training signal to normal data occurs when the training countdown is complete, as indicated by the training frame countdown being equal to 0 (94.3.10.7.2). Immediately after the last bit of the last training frame, transmission of the first PMA frame (94.2.2.4) begins with the termination block containing the overhead, T(i,1,1:92). The PRBS13 generator used during training to generate the training pattern is used to generate the termination bits in data mode. The state of the training PRBS13 generator is retained and 92 new bits are generated without reseeding or inverting. Termination bits are assigned and the PRBS13 generator continues to operate as specified in 94.2.2.4. The transition from training to data mode and mapping of the PRBS13 to training frame and termination bits is depicted in Figure 94–7.

94.3.10.10 Frame lock state diagram

The 10GBASE-KP4 PMD shall implement the frame lock state diagram as depicted in Figure 72–4 including compliance with the associated state variables, timers, counters, and functions specified in 72.6.10.3. The frame lock state diagram determines when the PMD control function has detected the frame boundaries in the received data stream.

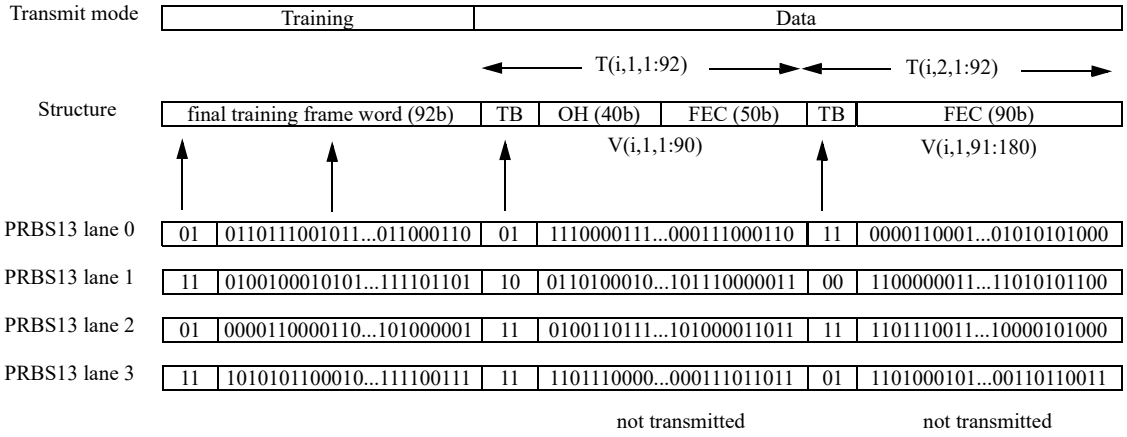

Figure 94–7—Transition from training to data mode

94.3.10.11 Training state diagram

The 10GBASE-KP4 PMD shall implement the training state diagram as depicted in Figure 72–5 including compliance with the associated state variables specified in 72.6.10.3. The training state diagram defines the operation of the 100GBASE-KP4 startup protocol.

When the training state diagram enters the INITIALIZE state, the transmitter equalizer shall be configured such that the output meets the requirements of 94.3.12.5.4.

94.3.10.12 Coefficient update state diagram

For each tap, the 100GBASE-KP4 PMD shall implement an instance of the coefficient update state diagram in Figure 72–6 including compliance with the associated state variables as specified in 72.6.10.3. The coefficient update state diagram defines the process for updating transmit equalizer coefficients in response to requests from the link partner and also defines the coefficient update status to be reported in outgoing training frames.

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94.3.11 PMD LPI function

The PMD LPI function responds to the transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD:IS_TX_MODE.request and PMD:IS_RX_MODE.request. Implementation of the function is optional. EEE capabilities and parameters are advertised during the Backplane Auto-negotiation, as described in 45.2.7.14. The transmitter on the local device informs the link partner's receiver when to sleep, refresh, and wake. The local receiver transitions are controlled by the link partner's transmitter and can change independent of the local transmitter states and transitions.

94.3.11.1 Alert Signal

During refresh and wake, to enable effective detection and quick receiver synchronization, an alert frame is sent prior to sending normal PMA frames. The alert signal is a series of repeating alert frames.

The alert frame shall be composed of a frame marker, control channel, and training pattern as depicted in Figure 94–8. The alert frame is based on the training frame specified in 94.3.10.2. The distinguishing differences are that the training pattern is truncated to 48 training frame words (4416 bits) and the coefficient update and status report fields are encoded differently. The alert frame is a total of 58 training frame words in length.

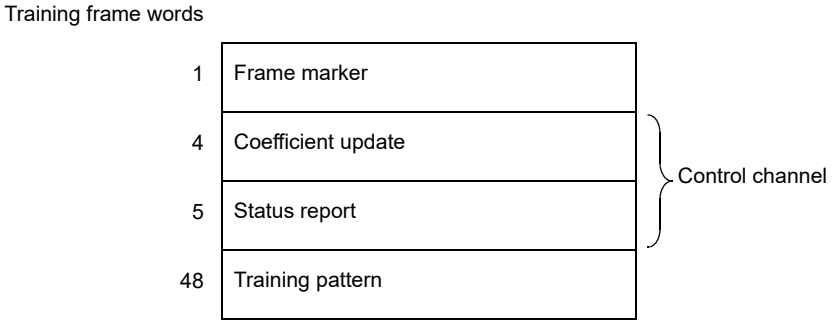

Figure 94–8—Alert frame structure

94.3.11.1.1 Frame marker

The frame marker shall be implemented as specified in 94.3.10.4.

94.3.11.1.2 Coefficient update field

The coefficient update field is unused in the alert frame. All bits in the coefficient update field are reserved and shall be transmitted as zeros.

94.3.11.1.3 Status report field

The status report field is used to signal state information from the local PMD to the link partner. The format of the status report field of alert frames shall be as shown in Table 94–10. Cell 19 of the status report field shall be transmitted first.

94.3.11.1.4 Parity

The parity field shall have the same behavior and purpose as specified for the training frame in 94.3.10.7.1.

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94.3.11.1.5 Mode

The mode field indicates whether the frame is a training frame (mode = 0) or an alert frame (mode = 1). This field differentiates the alert frame from a training frame. The mode field in the alert frame shall always indicate 1.

94.3.11.1.6 Alert frame countdown

The alert frame countdown field shall be updated as specified for the training frame in 94.3.10.7.2. The alert frame countdown may be used by the receiver to determine when the signal transitions from the alert frame to the PMA frame (see 94.3.11.1.9).

94.3.11.1.7 PMA alignment offset

The PMA alignment offset (PAO) shall indicate the relative position in the PMA frame in relation to the beginning of the next alert frame as described in this subclause. The PMA alignment offset may be used by the receiver to synchronize to the PMA frame without an additional frame synchronization process (see 94.3.11.1.9). The beginning of the PMA frame is defined as the termination block containing the PMA overhead (94.2.2.2).

The PMA frame length is exactly 6 times the alert frame length. The PMA alignment offset field indicates one of six offsets for the next alert frame within the PMA frame. The offset in number of training frame words of the next alert frame is determined by multiplying PMA alignment offset by 32. As a reference point, a PMA alignment offset of zero indicates that the start of the next alert frame is aligned with the start of a PMA frame. Valid values for the PMA alignment offset are {0,1,2,3,4,5}. The values {6,7} are not valid.

94.3.11.1.8 Receiver ready

The receiver ready cell shall always be set to 1 to indicate training is complete and the link is up.

94.3.11.1.9 Transition from alert to data

The transmitted signal shall transition from the alert signal to normal data as described in this subclause.

The transition from the alert signal to normal data occurs when the alert countdown is complete, as indicated by the alert frame countdown being equal to 0 (94.3.11.1.6). Immediately after the last bit of the last alert frame, transmission of the first PMA frame (94.2.2.4) begins with the termination block indicated by the PMA alignment offset, T(i,32*PAO,1:92). The PRBS13 generator used during alert to generate the training pattern is used to generate the termination bits in data mode. The state of the training PRBS13 generator is retained and 92 new bits are generated without reseeding or inverting. Termination bits are assigned and the PRBS13 generator continues to operate as specified in 94.2.2.4. The transition from alert to data mode and mapping of the PRBS13 to alert frame and termination bits is depicted in Figure 94–9. The values for the PRBS13 in Figure 94–9 are specific to a transition with a PAO of zero. The values are different for other PAO values.

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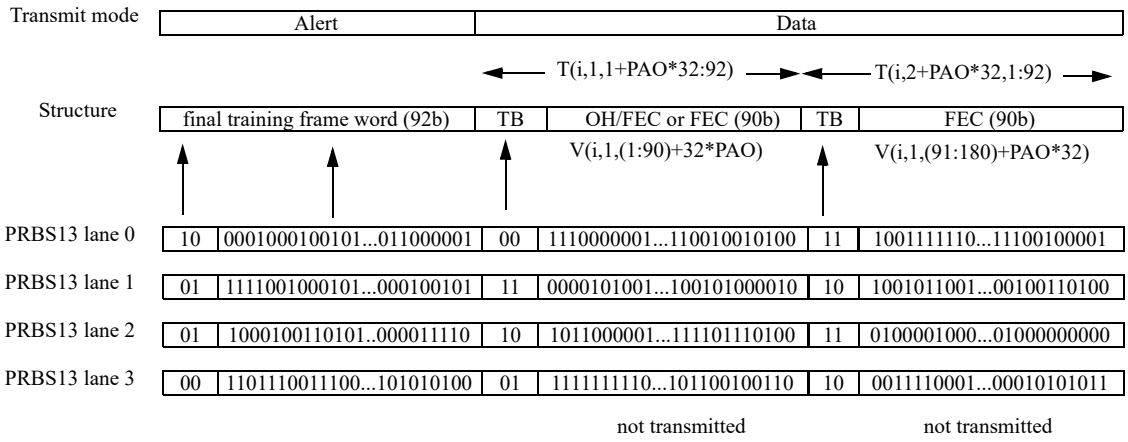

Figure 94–9—Transition from alert to data mode

94.3.12 PMD Transmitter electrical characteristics

Transmitter characteristics measured at TP0a are summarized in Table 94–13.

94.3.12.1 Test fixture

The test fixture of Figure 94–10 or its equivalent is required for measuring the transmitter specifications described in 94.3.12.

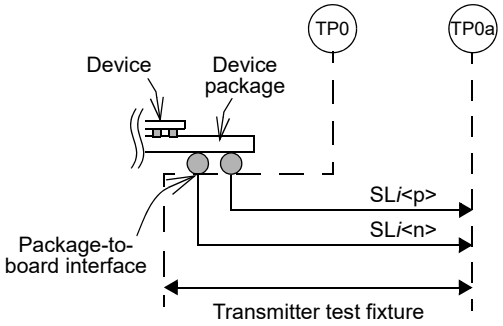

Figure 94–10—Transmitter test fixture and test points

94.3.12.1.1 Test fixture impedance

The differential load impedance applied to the transmitter output by the test fixture depicted in Figure 94–10 shall be 100 Ω.

The differential return loss, in dB with f in GHz, of the test fixture shall meet the requirement of Equation (94–4). The return loss limit $RL_{\min}(f)$ is shown Figure 94–11.

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Table 94–13—Summary of transmitter characteristics at TP0a

Parameter	Subclause reference	Value	Units
Signaling rate	94.3.12.2	13.59375 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max.) Transmitter disabled Transmitter enabled	94.3.12.3	 30 1200	 mV mV
DC common-mode output voltage (max.)	94.3.12.3	1.9	V
DC common-mode output voltage (min.)	94.3.12.3	0	V
AC common-mode output voltage (RMS, max.)	94.3.12.3	30	mV
Differential output return loss (min.)	94.3.12.4	Equation (94–7)	dB
Common-mode output return loss (min.)	94.3.12.4	Equation (94–8)	dB
Output waveform Level separation mismatch ratio, R_{LM} (min) Steady-state voltage v_f (max.) Steady-state voltage v_f (min.) Linear fit pulse peak (min.) Normalized coefficient step size (min.) Normalized coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)	 94.3.12.5.1 94.3.12.5.3 94.3.12.5.3 94.3.12.5.3 94.3.12.5.5 94.3.12.5.5 94.3.12.5.6 94.3.12.5.6	 0.92 0.6 0.4 0.85 × v_f 0.0083 0.05 1.54 4	 — V V V — — — —
Output jitter and linearity Clock random jitter, RMS (max.) Clock deterministic jitter, peak-to-peak (max.) Even-odd jitter (max.) Signal-to-noise-and-distortion ratio, SNDR (min.)	 94.3.12.6.1 94.3.12.6.1 94.3.12.6.2 94.3.12.7	 0.005 0.05 0.019 31	 UI UI UI dB

$$RL(f) \geq RL_{\min}(f) = \left\{ \begin{array}{ll} 20 - f & 0.05 \leq f \leq 5 \\ 15 & 5 < f \leq 13 \\ 20.57 - 0.4286f & 13 < f \leq 14 \end{array} \right\} \text{ (dB)} \qquad (94\text{–}4)$$

The common-mode return loss, in dB, with f in GHz, of the test fixture shall meet the requirement of Equation (94–5). The return loss limit $RL_{\min}(f)$ is shown Figure 94–12.

$$RL(f) \geq RL_{\min}(f) = 10 \text{ (dB)} \qquad 0.05 \leq f \leq 14 \qquad (94\text{–}5)$$

94.3.12.1.2 Test fixture insertion loss

The insertion loss of the test fixture measured at 12.89 GHz shall be between 1.2 dB and 1.6 dB.

The insertion loss deviation of the test fixture from 0.05 GHz to 10 GHz shall be less than 0.1 dB.

The reference insertion loss of the test fixture is defined by Equation (94–6), where f is the frequency in GHz, and is shown in Figure 94–13.

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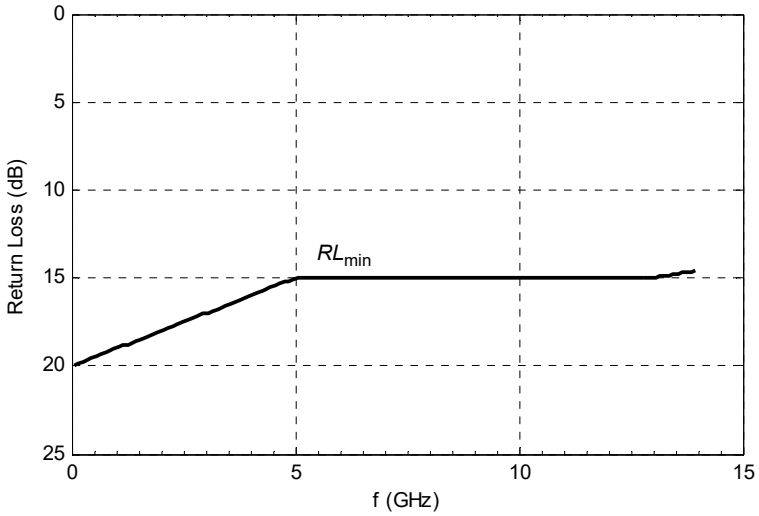

Figure 94–11—Test fixture differential return loss limit

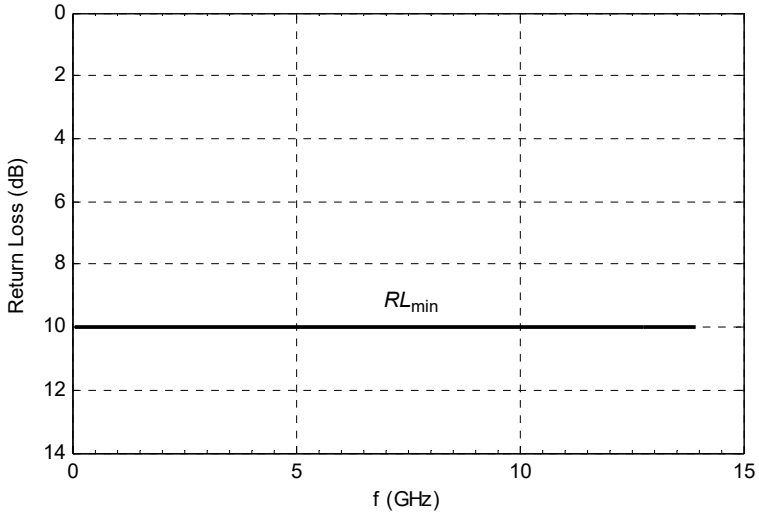

Figure 94–12—Test fixture common-mode return loss limit

$$IL_{ref}(f) = -0.0015 + 0.144\sqrt{f} + 0.069f \ \text{(dB)} \qquad 0.05 \le f \le 14 \tag{94–6}$$

The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the measurements.

A test system with a fourth-order Bessel-Thomson low-pass response with 17 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified.

94.3.12.2 Signaling rate and range

The 100GBASE-KP4 signaling rate shall be 13.59375 GBd ± 100 ppm per lane.

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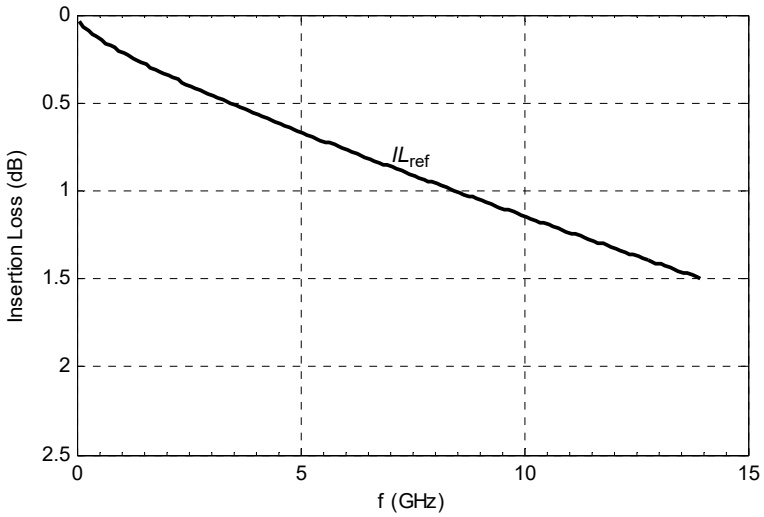

Figure 94–13—Test fixture reference insertion loss

94.3.12.3 Signal levels

The differential output voltage v_{di} is defined to be SL*i*<p> minus SL*i*<n>. The common-mode output voltage v_{cmi} is defined to be one half of the sum of SL*i*<p> and SL*i*<n>. These definitions are illustrated by Figure 94–14.

For a QPRBS13 test pattern (94.2.9.3), the peak-to-peak differential output voltage shall be less than or equal to 1200 mV regardless of the transmit equalizer setting. The peak-to-peak differential output voltage shall be less than or equal to 30 mV while the transmitter is disabled (refer to 94.3.6.6 and 94.3.6.7).

The DC common-mode output voltage shall be between 0 V and 1.9 V with respect to signal ground. The AC common-mode output voltage shall be less than or equal to 30 mV RMS with respect to signal ground. Common-mode output voltage requirements shall be met regardless of the transmit equalizer setting.

If the optional EEE deep sleep capability is supported, the following requirements also apply. The peak-to-peak differential output voltage shall be less than 30 mV within 500 ns of the transmitter being disabled.

When the transmitter transitions from disabled to enabled: (a) The amplitude of the frame marker of the third complete alert frame (see 94.3.11.1) after the transmitter is enabled shall be greater than 90% of the steady-state value (see 94.3.12.5.3), and (b) the transmitter output shall meet the requirements of 94.3.12 within 1 μs of the transmitter being enabled.

While the transmitter is disabled, the DC common-mode output voltage shall be maintained to within ±150 mV of the value for the enabled transmitter.

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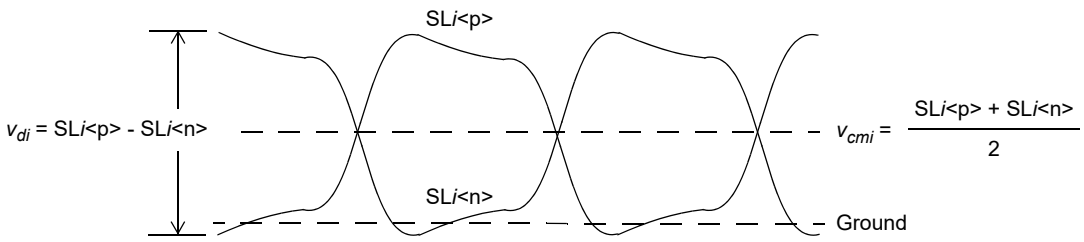

Figure 94–14—Transmitter output voltage definitions

94.3.12.4 Transmitter output return loss

The differential output return loss, in dB, of the transmitter shall meet Equation (94–7), where *f* is the frequency in GHz. The return loss limit $RL_{\min}(f)$ is shown Figure 94–15. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$RL(f) \geq RL_{\min}(f) = \left\{ \begin{array}{cc} 12.05 - f & 0.05 \leq f \leq 6 \\ 6.5 - 0.075f & 6 < f \leq 10 \end{array} \right\} \quad \text{(dB)} \tag{94–7}$$

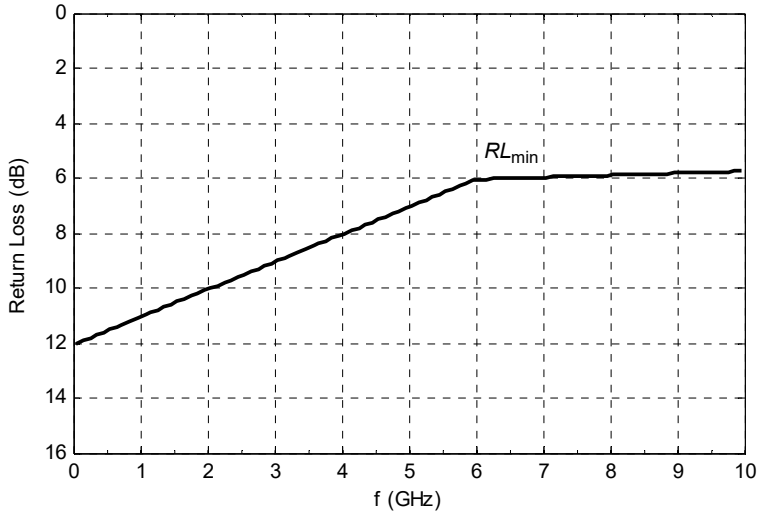

Figure 94–15—Transmitter differential return loss limit

The common-mode output return loss, in dB, of the transmitter shall meet Equation (94–8), where *f* is the frequency in GHz. The return loss limit $RL_{\min}(f)$ is shown Figure 94–16. This output impedance requirement applies to all valid output levels. The reference impedance for common-mode return loss measurements shall be 25 Ω.

$$RL(f) \geq RL_{\min}(f) = \left\{ \begin{array}{cc} 9.05 - f & 0.05 \leq f \leq 6 \\ 3.5 - 0.075f & 6 < f \leq 10 \end{array} \right\} \quad \text{(dB)} \tag{94–8}$$

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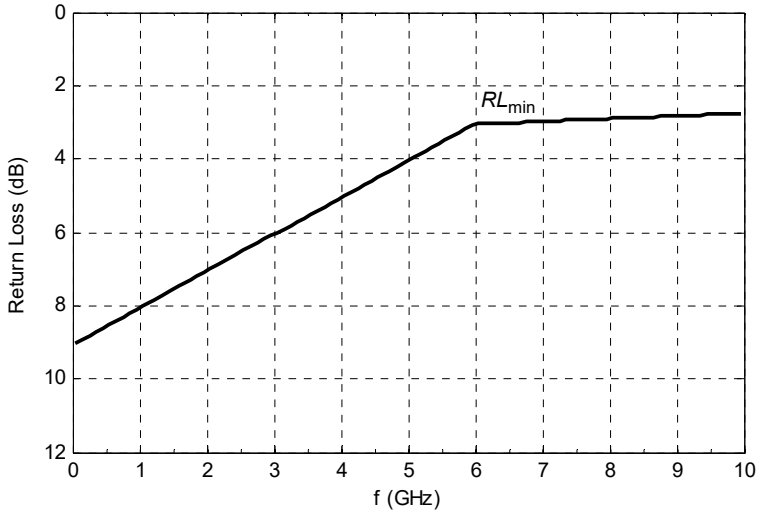

Figure 94–16—Transmitter common-mode return loss limit

94.3.12.5 Transmitter output waveform

The 100GBASE-KP4 transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in Figure 94–17.

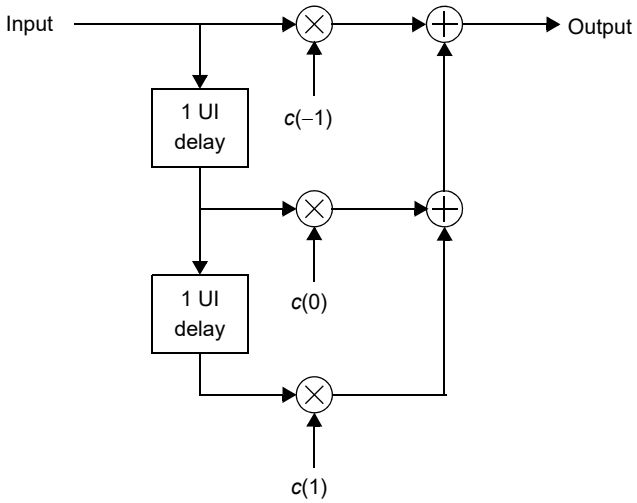

Figure 94–17—Transmit equalizer functional model

The state of the transmit equalizer and hence the transmitted output waveform may be manipulated via the PMD control function defined in 94.3.10 or via the management interface. The transmit function responds to a set of commands issued by the link partner's receive function and conveyed by a back-channel communications path.

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This command set includes instructions to:

Increment coefficient $c(i)$.
Decrement coefficient $c(i)$.
Hold coefficient $c(i)$ at its current value.
Set the coefficients to a predefined value (preset or initialize).

In response, the transmit function relays status information to the link partner's receive function. The status messages indicate that:

The requested update to coefficient $c(i)$ has completed (updated).
Coefficient $c(i)$ is at its minimum value.
Coefficient $c(i)$ is at its maximum value.
Coefficient $c(i)$ is ready for the next update request (not_updated).

94.3.12.5.1 Transmitter linearity

Transmitter linearity is measured using the transmitter linearity test pattern (see 94.2.9.4).

The resulting waveform is shown in Figure 94–18. Each measured level, V_A, V_B, V_C, and V_D, is measured within a 2 UI period starting 7 UI after the last level transition time. The minimum signal level, S_{min}, effective symbol levels ES_1 and ES_2, and level separation mismatch ratio, R_{LM}, are calculated based on Equation (94–9), Equation (94–10), Equation (94–11), Equation (94–12), and Equation (94–13), respectively.

The level separation mismatch ratio shall be greater than 0.92.

$$S_{\text{min}} = \frac{\min(V_D - V_C, V_C - V_B, V_B - V_A)}{2} \tag{94–9}$$

$$V_{\text{avg}} = \frac{V_A + V_B + V_C + V_D}{4} \tag{94–10}$$

$$ES_1 = \frac{V_B - V_{\text{avg}}}{V_A - V_{\text{avg}}} \tag{94–11}$$

$$ES_2 = \frac{V_C - V_{\text{avg}}}{V_D - V_{\text{avg}}} \tag{94–12}$$

$$R_{\text{LM}} = \frac{6 \cdot S_{\text{min}}}{V_D - V_A} \tag{94–13}$$

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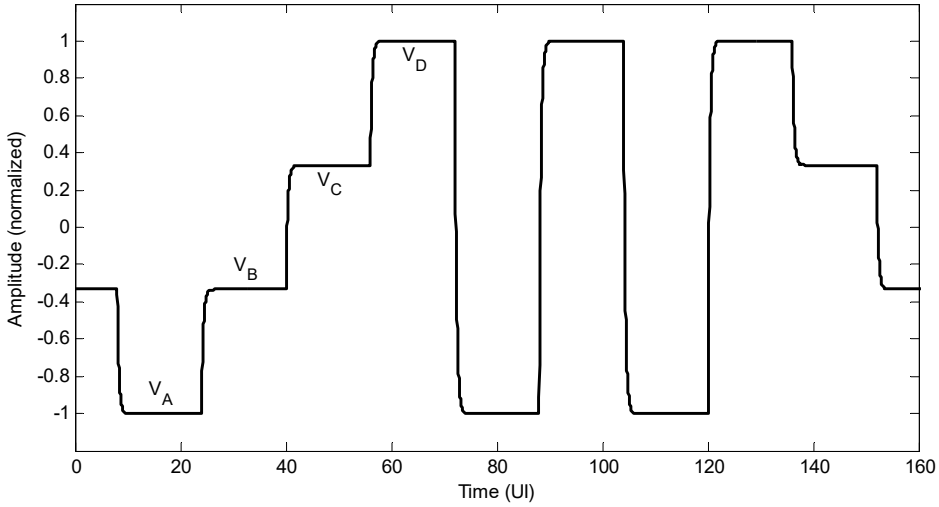

Figure 94–18—Transmitter linearity test pattern

94.3.12.5.2 Linear fit to the measured waveform

The following test procedure shall be followed to determine the linear fit pulse response, linear fit error, and normalized transmitter coefficient values.

For each configuration of the transmit equalizer, capture at least one complete cycle of the QPRBS13 test pattern (94.2.9.3) at TP0a per 85.8.3.3.4.

Compute the linear fit pulse response $p(k)$ from the captured waveform per 85.8.3.3.5 using $N_p = 16$ and $D_p = 2$. For aligned symbol values x(n) use –1, $-ES_1$, ES_2, and 1 to represent symbol values of 0, 1, 2, and 3, respectively, and where ES_1 and ES_2 are the effective symbol levels determined in 94.3.12.5.1.

Define $r(k)$ to be the linear fit pulse response when transmit equalizer coefficients have been set to the "preset" values (72.6.10.2.3.1).

For each configuration of the transmit equalizer, compute the normalized transmit equalizer coefficients, *c(i)*, according to 92.8.3.5.1.

94.3.12.5.3 Steady-state voltage and linear fit pulse peak

The linear fit pulse, $p(k)$, is determined according to the linear fit procedure in 94.3.12.5.2. The steady-state voltage v_f is defined to be the sum of the linear fit pulse $p(k)$ divided by M, determined in step 3 of the linear fit procedure.

The steady-state voltage shall be greater than or equal to 0.4 V and less than or equal to 0.6 V.

The peak value of $p(k)$ shall be greater than $0.85 \times v_f$.

94.3.12.5.4 Coefficient initialization

When the PMD enters the INITIALIZE state of the Training state diagram (Figure 72–5) or receives a valid request to "initialize" from the link partner, the coefficients of the transmit equalizer shall be configured such that the ratio (c(0)+c(1)–c(–1))/(c(0)+c(1)+c(–1)) is 1.29 ±10%, the ratio

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(c(0)–c(1)+c(–1))/(c(0)+c(1)+c(–1)) is 2.57 ±10%, and the steady-state voltage, v_f, (see 94.3.12.5) is greater than or equal to 140 mV. These requirements apply upon the assertion of a coefficient status report of "updated" for all coefficients.

94.3.12.5.5 Coefficient step size

The normalized amplitude of each coefficient $c(i)$ is determined according to the linear fit procedure in 94.3.12.5.2.

The change in the normalized amplitude of coefficient $c(i)$ corresponding to a request to "increment" that coefficient shall be between 0.0083 and 0.05. The change in the normalized amplitude of coefficient $c(i)$ corresponding to a request to "decrement" that coefficient shall be between –0.05 and –0.0083.

The change in the normalized amplitude of the coefficient is defined to be the difference in the value measured prior to the assertion of the "increment" or "decrement" request (e.g., the coefficient update request for all coefficients is "hold") and the value upon the assertion of a coefficient status report of "updated" for that coefficient.

94.3.12.5.6 Coefficient range

When sufficient "increment" or "decrement" requests have been received for a given coefficient, the coefficient reaches a lower or upper bound based on the coefficient range or restrictions placed on the minimum steady-state differential output voltage or the maximum peak-to-peak differential output voltage.

With $c(-1)$ set to zero and both $c(0)$ and $c(1)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0)–c(1))/(c(0)+c(1))$ shall be greater than or equal to 4.

With $c(1)$ set to zero and both $c(-1)$ and $c(0)$ having received sufficient "decrement" requests so that they are at their respective minimum values, the ratio $(c(0)–c(-1))/(c(0)+c(-1))$ shall be greater than or equal to 1.54.

Note that a coefficient may be set to zero by first asserting the preset control and then manipulating the other coefficients as required by the test.

94.3.12.6 Transmitter output jitter

Jitter measurements in this subclause are performed with transmitters on all PMD lanes enabled and transmitting the same pattern with identical transmit equalizer settings.

94.3.12.6.1 Clock random jitter and clock deterministic jitter

Clock random jitter (CRJrms) measured at the transmitter output using the methodology described in this subclause shall be less than 0.005 UI RMS regardless of transmit equalization setting.

Clock deterministic jitter (CDJ) measured at the transmitter output using the methodology described in this subclause shall be less than 0.05 UI peak-to-peak regardless of transmit equalization setting.

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CRJrms and CDJ are determined using the following procedure:

1) CRJrms and CDJ are measured using the JP03A test pattern (94.2.9.1).
2) Using appropriate test equipment and procedure, capture the zero-crossing times, $T_{ZC}(i)$, of a pattern of length, N, of 10^7 symbols or greater.
3) Determine the average pulse width ΔT_{Avg} using Equation (94–14).
4) Determine the jitter series, $\tau(k)$, using Equation (94–15).
5) Apply the effect of a high-pass filter with the response given by Equation (94–16) to the jitter samples to obtain $\tau_{HPF}(k)$, where f is the frequency in MHz, f_n is 2.12 MHz, T is 0.0286 μs, and $j = \sqrt{-1}$.
6) Create a CDF as a function of $\tau_{HPF}(k)$.
7) From the CDF, determine J_5 as the difference between τ_{HPF} at the $(1–0.5 \times 10^{-5})$ and 0.5×10^{-5} probabilities, respectively, and J_6 as the difference between τ_{HPF} at the $(1–0.5 \times 10^{-6})$ and 0.5×10^{-6} probabilities, respectively.
8) Calculate CRJrms and CDJ using the relationship in Equation (94–17).

$$\Delta T_{Avg} = \frac{T_{ZC}(N) - T_{ZC}(1)}{N-1} \tag{94–14}$$

$$\tau(k) = T_{ZC}(k) - (k-1)\cdot\Delta T_{Avg} - T_{ZC}(1) \qquad k = 2, 3, \ldots N \tag{94–15}$$

$$G(f) = \frac{f}{f - j \times f_n e^{(-j2\pi fT)}} \tag{94–16}$$

$$\begin{bmatrix} CRJrms \\ CDJ \end{bmatrix} = \begin{bmatrix} 1.0538 & -1.0538 \\ -9.3098 & 10.3098 \end{bmatrix} \begin{bmatrix} J_6 \\ J_5 \end{bmatrix} \tag{94–17}$$

94.3.12.6.2 Even-odd jitter

Even-odd jitter (EOJ) measured at the transmitter output using the methodology described in this subclause shall be less than 0.019 UI peak-to-peak regardless of transmit equalization setting.

EOJ is determined using the following procedure:

1) EOJ is measured using the JP03B test pattern (94.2.9.2).
2) Using appropriate test equipment and procedure, capture the time for each of the 60 transitions.
3) Averaging of the vertical waveform or of each zero-crossing time is recommended to mitigate the contribution of uncorrelated noise and jitter.
4) Denote the averaged zero-crossing times as $T_{ZC}(i)$, where i = {1,2,...60} and where i = 1 designates the transition from 3 to 0 after the consecutive pair of symbols {3,3}.
5) The set of 40 pulse widths, $\Delta T(j)$, isolated from the double-width pulses are determined using the relationship in Equation (94–18).
6) EOJ is calculated using the relationship in Equation (94–19).

$$\Delta T(j) = \left\{ \begin{array}{ll} T_{ZC}(j+10) - T_{ZC}(j+9) & 1 \le j \le 20 \\ T_{ZC}(j+19) - T_{ZC}(j+18) & 21 \le j \le 40 \end{array} \right\} \tag{94–18}$$

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$$EOJ = \frac{\left| \sum_{j=1}^{20} \Delta T(2 \cdot j) - \sum_{j=1}^{20} \Delta T(2 \cdot j - 1) \right|}{40} \quad (94\text{–}19)$$

94.3.12.7 Transmitter signal-to-noise-and-distortion ratio (SNDR)

Signal-to-noise-and-distortion ratio (SNDR) is measured at the transmitter output using the following method, with transmitters on all PMD lanes enabled and transmitting the same pattern with identical transmit equalizer settings.

Compute the linear fit to the captured waveform and the linear fit pulse response, $p(k)$, and error, $e(k)$, according to 94.3.12.5.2. Denote the standard deviation of $e(k)$ as σ_e.

Given the same configuration of the transmit equalizer, measure the RMS deviation from the mean voltage at a fixed point in a run of at least 8 consecutive identical levels. The transmitter linearity test pattern as specified in 94.3.12.5.1 is an example of a pattern that includes runs suitable to perform the measurement. The RMS deviation is measured for a run of each of the four levels. The average of the four measurements is denoted as σ_n.

SNDR is defined by Equation (94–20) where $p_{\max}$ is the maximum value of $p(k)$.

$$SNDR = 10\log_{10}\left(\frac{p_{\max}^2}{\sigma_e^2 + \sigma_n^2}\right) \text{ (dB)} \quad (94\text{–}20)$$

SNDR shall be greater than 31 dB for any allowable transmit equalizer setting.

94.3.13 PMD Receiver electrical characteristics

Receiver characteristics measured at TP5a are summarized in Table 94–14.

Table 94–14—Summary of receiver characteristics at TP5a

Parameter	Subclause reference	Value	Units
Differential input return loss (min.)	94.3.13.2	Equation (94–7)	dB
Differential to common-mode return loss (min.)	94.3.13.2	Equation (94–21)	dB
Interference tolerance	94.3.13.3	Table 94–15	—
Jitter tolerance	94.3.13.4	Table 94–16	—

94.3.13.1 Test fixture

The test fixture of Figure 94–19 or its equivalent is required for measuring the receiver specifications described in 94.3.13. The test fixture shall meet the requirements for insertion loss, insertion loss deviation, differential return loss, and common-mode return loss in 94.3.12.1.

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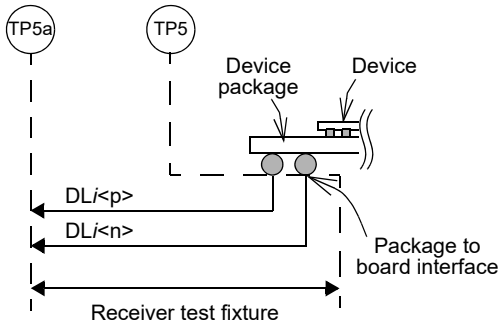

Figure 94–19—Receiver test fixture and test points

94.3.13.2 Receiver input return loss

The differential input return loss, in dB, of the receiver shall meet Equation (94–7). The reference impedance for differential return loss measurements shall be 100 Ω.

The differential to common-mode return loss, in dB, of the receiver shall meet Equation (94–21). The return loss limit $RL_{\min}(f)$ is shown Figure 94–20.

$$RL(f) \geq RL_{\min}(f) = \left\{ \begin{array}{cc} 25 - 1.44f & 0.05 \leq f \leq 6.95\text{GHz} \\ 15 & 6.95 \leq f \leq 10\text{GHz} \end{array} \right\} \text{ (dB)} \quad (94\text{–}21)$$

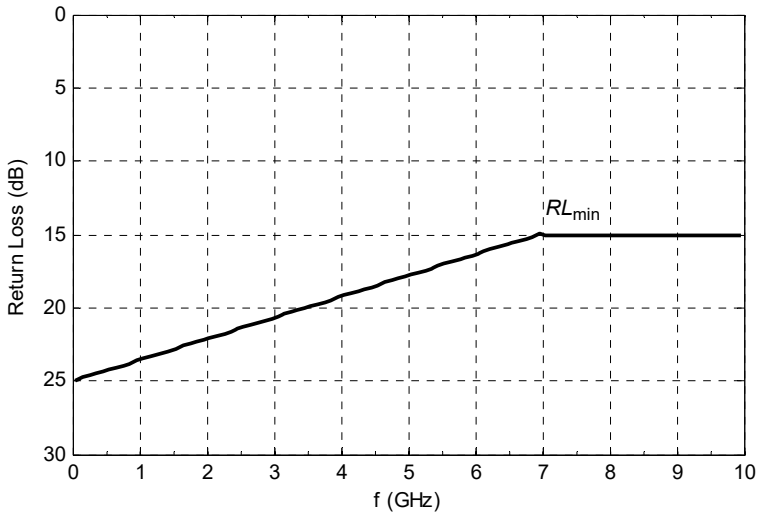

Figure 94–20—Receiver differential to common-mode return loss limit

94.3.13.3 Receiver interference tolerance

Receiver interference tolerance is defined by the procedure in Annex 93C. The receiver on each lane shall meet the FEC symbol error ratio requirement with channels matching the Channel Operating Margin (COM) and loss parameters for Test 1 and Test 2 in Table 94–15. Example fitted-insertion-loss curves for Test 1 and Test 2, as well as bounds resulting from the constraints on the fitted-insertion-loss coefficients with insertion loss at the limit specified for each test, are shown in Figure 94–21 and Figure 94–22, respectively. The

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parameter RSS_DFE4 in Table 94–15 is a figure of merit for the test channel that is defined by Equation (93A–50) (see 93A.2).

The following considerations apply to the interference tolerance test. The transmitter noise parameter is SNDR (see 94.3.12.7). The transmitter output levels are set such that R_{LM} is equal to 0.92. The test transmitter meets the specifications in 94.3.12. The test transmitter is constrained such that for any transmitter equalizer setting the differential peak-to-peak voltage (see 94.3.12.3) is less than 800 mV, the pre-cursor peaking ratio (see 94.3.12.5.6) is less than 1.54, and the post-cursor peaking ratio (see 94.3.12.5.6) is less than 4. The lower frequency bound for the noise spectral density constraints, f_{NSD1}, is 1 GHz. The jitter parameters to be measured are CRJrms and CDJ (see 94.3.12.6.1). The return loss of the test setup in Figure 93C–4 measured at TP5 replica meets the requirements of Equation (94–4). The COM parameter σ_{RJ} is set to the measured value of CRJrms and the COM parameter A_{DD} is set to half the measured value of CDJ. Other COM parameters are set according to the values in Table 94–17. The test pattern to be used is the scrambled idles test pattern. A test system with a fourth-order Bessel-Thomson low-pass response with 17 GHz 3 dB bandwidth is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.

Table 94–15—Receiver interference tolerance parameters

Parameter	Test 1 values		Test 2 values		Units
	Min	Max	Min	Max	
FEC symbol error ratio[a]	—	3.3×10^{-3}	—	3.3×10^{-3}	
COM, including effects of broadband noise[b]	3		3		dB
Insertion loss at 7 GHz[c]	—	14.4	33	—	dB
Fitted insertion loss coefficients[d]: a_0 a_1 a_2 a_4	 –1.5 0 0 0	 1 1.6 1.6 0.03	 –1.5 0 0 0	 2 3.8 4.2 0.065	 dB dB/√GHz dB/GHz dB/GHz^2
RSS_DFE4	0.05	—	0.05	—	—

[a]The FEC symbol error ratio is measured in step 10 of the interference tolerance test method in 93C.2.
[b]The COM value is the target for the receiver noise level calibration defined in 93C.2 step 7. The channel noise voltage applied in 93C.2 step 8 should be as close as practical to the value needed to produce the target COM. If higher channel noise voltage values are used, this would demonstrate margin to the specification but this is not required for compliance.
[c]Measured between TPt and TP5 (see Figure 93C–4).
[d]Coefficients are determined from insertion loss measured between TPt and TP5 (see Figure 93C–4) using the methodology in 93A.3 with f_{min} of 0.05 GHz, f_{max} of 13.59375 GHz, and maximum Δf of 0.01 GHz.

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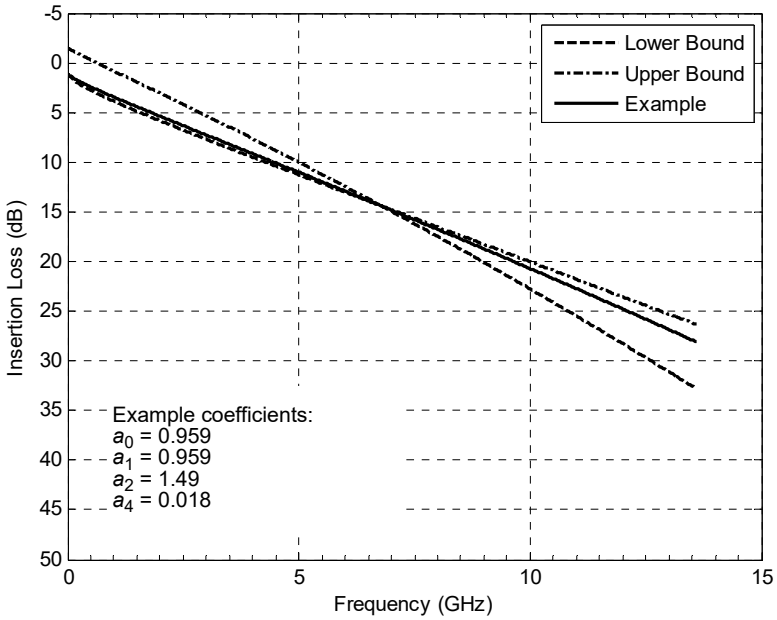

Figure 94–21—Insertion loss example and bounds for Test 1 channel

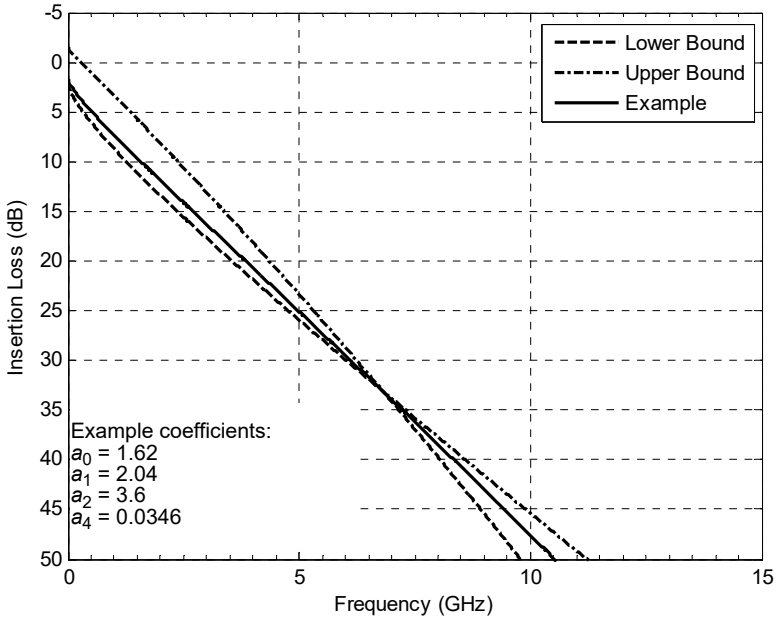

Figure 94–22—Insertion loss example and bounds for Test 2 channel

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94.3.13.4 Receiver jitter tolerance

Receiver jitter tolerance is defined by the procedure defined in 94.3.13.4.2. The receiver FEC symbol error ratio shall be less than the maximum value for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 94–16.

Table 94–16—Receiver jitter tolerance parameters

Parameter	Case A values	Case B values	Units
Maximum FEC symbol error ratio[a]	3.3×10^{-3}	3.3×10^{-3}	
Jitter frequency	16	160	kHz
Jitter amplitude	5	0.5	UI

[a]The FEC symbol error ratio is measured in step 3 of the jitter tolerance test method in 94.3.13.4.2.

94.3.13.4.1 Test setup

Jitter tolerance is measured using the test setup in Figure 93C–2 on each lane. The transmitter output is constrained as described in 93C.1. The Tx and channel noise sources are disabled. The test channel (TPt to TP5 replica) meets the requirements for the channel used for Test 2 in 94.3.13.3. The low-frequency jitter specified in Table 94–16 is applied to the output of the transmitter and is measured at TP0a.

94.3.13.4.2 Test method

The following jitter tolerance test method is repeated for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 94–16.

1) Configure the transmitter with the corresponding jitter frequency and amplitude from Table 94–16.
2) Initiate training on the receiver under test and allow training to complete.
3) Measure the FEC symbol error ratio on each lane using the errored symbol counter, FEC_symbol_error_counter_*i*, where *i* is the lane under test.

94.4 Channel characteristics

94.4.1 Channel Operating Margin

The Channel Operating Margin (COM) is computed using the procedure in 93A.1 with the Test 1 and Test 2 values in Table 94–17. Test 1 and Test 2 differ in the value of the device package model transmission line length z_p.

COM shall be greater than or equal to 3 dB for each test. This minimum value allocates margin for practical limitations on the receiver implementation as well as the largest step size allowed for transmitter equalizer coefficients.

94.4.2 Channel insertion loss

The insertion loss, in dB, of the channel is recommended to meet Equation (94–22). The insertion loss limit is shown Figure 94–23.

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Table 94–17—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	13.59375	GBd
Maximum start frequency	$f_{\min}$	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface	 C_d z_p z_p C_p	 2.5×10^{-4} 12 30 1.8×10^{-4}	 nF mm mm nF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.62	—
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.18 0 0.02	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.38 0 0.02	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –12 0 1	 dB dB dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	$f_b / 4$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b / 4$ f_b	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.4 0.4 0.6	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.92	—
Transmitter signal-to-noise ratio	SNR_{TX}	31	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	16	UI
Normalized DFE coefficient magnitude limit for n = 1 for n = 2 to N_b	$b_{max}(n)$	 1 0.2	—
Random jitter, RMS	σ_{RJ}	0.005	UI
Dual-Dirac jitter, peak	A_{DD}	0.025	UI
One-sided noise spectral density	η_0	5.2×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	3×10^{-4}	—

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$$IL(f) \le IL_{\max}(f) = \left\{ \begin{array}{cc} a_0 + a_1 \cdot \sqrt{f} + a_2 \cdot f + a_3 \cdot f^2 + a_4 \cdot f^3 & f_{\min} \le f \le f_2 \\ a_5 + a_6 \cdot (f - f_2) & f_2 \le f \le f_{\max} \end{array} \right\} \text{(dB)} \quad (94\text{–}22)$$

where

$IL(f)$ is the insertion loss in dB at frequency f
$IL_{\max}(f)$ is the maximum allowable insertion loss at frequency f
f is the measurement frequency in Hz
$f_{\min} = 0.05$ GHz
$f_2 = 7$ GHz
$f_{\max} = 15$ GHz
$a_0 = 0.8$
$a_1 = 1.7372 \times 10^{-4}$
$a_2 = 1.1554 \times 10^{-9}$
$a_3 = 2.7795 \times 10^{-19}$
$a_4 = -1.0423 \times 10^{-29}$
$a_5 = 33.467$
$a_6 = 1 \times 10^{-8}$

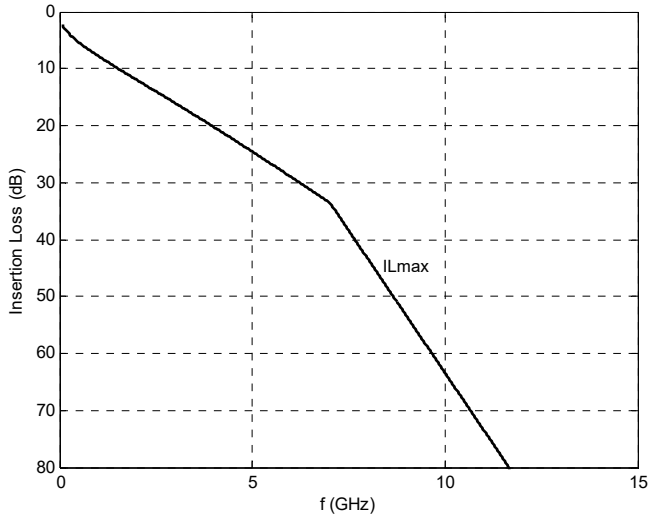

Figure 94–23—Channel insertion loss limit

94.4.3 Channel return loss

The return loss, in dB, of the channel is recommended to meet Equation (94–23). The return loss limit $RL_{\min}(f)$ is shown Figure 94–24.

$$RL(f) \ge RL_{\min}(f) = \left\{ \begin{array}{cc} 12 & 0.05 \le f \le f_b/4 \\ 12 - 15\log_{10}(4f/f_b) & f_b/4 < f \le f_b \end{array} \right\} \text{(dB)} \quad (94\text{–}23)$$

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where

$RL(f)$ is the return loss at frequency f in dB
$RL_{min}(f)$ is the minimum allowable return loss in dB
f is the measurement frequency in GHz
f_b is the signaling rate (13.59375) in GHz

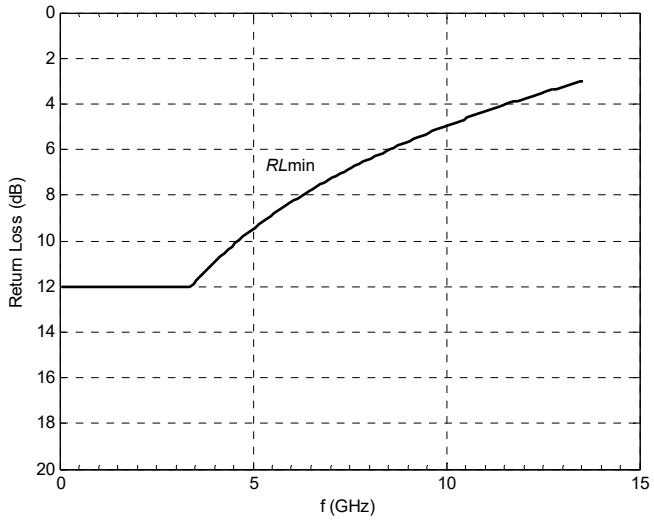

Figure 94–24—Channel return loss limit

94.4.4 Channel AC-coupling

The 100GBASE-KP4 transmitter shall be AC-coupled to the receiver. Common-mode specifications are defined as if the DC-blocking capacitor is implemented between TP0 and TP5. Should the capacitor be implemented outside TP0 and TP5, the common-mode specifications in Table 94–13 may not be appropriate.

The impact of a DC-blocking capacitor implemented between TP0 and TP5 is accounted for within the channel specifications. Should the capacitor be implemented outside TP0 and TP5, it is the responsibility of implementers to consider any necessary modifications to common-mode and channel specifications required for interoperability as well as any impact on the verification of transmitter and receiver compliance.

The low-frequency 3 dB cutoff of the AC-coupling shall be less than 50 kHz.

94.5 Environmental specifications

94.5.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

94.5.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

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94.5.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

94.5.4 Electromagnetic compatibility

A system integrating the 100GBASE-KP4 PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

94.5.5 Temperature and humidity

A system integrating the 100GBASE-KP4 PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

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94.6 Protocol implementation conformance statement (PICS) proforma for Clause 94, Physical Medium Attachment (PMA) sublayer, Physical Medium Dependent (PMD) sublayer, and baseband medium, type 100GBASE-KP4[163]

94.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 94, Physical Medium Attachment (PMA) sublayer, Physical Medium Dependent (PMD) sublayer, and baseband medium, type 100GBASE-KP4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

94.6.2 Identification

94.6.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

94.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 94, Physical Medium Attachment (PMA) sublayer, Physical Medium Dependent (PMD) sublayer, and baseband medium, type 100GBASE-KP4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[163] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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94.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
CGMII	CGMII	94.1	Interface is supported	O	Yes [ ] No [ ]
PCS	100GBASE-R PCS	94.1		M	Yes [ ]
RS-FEC	100GBASE-R RS-FEC	94.1		M	Yes [ ]
PMA	100GBASE-R PMA	94.1		O	Yes [ ] No [ ]
CAUI-10	CAUI-10	94.1	Interface is supported	O	Yes [ ] No [ ]
CAUI-4	CAUI-4	94.1	Interface is supported	O	Yes [ ] No [ ]
AN	Auto-negotiation	94.1		M	Yes [ ]
*MD	MDIO capability	94.3.5	Registers and interface supported	O	Yes [ ] No [ ]
*EEE	EEE capability	94.1	Capability is supported	O	Yes [ ] No [ ]
*GTD	Global PMD transmit disable function	94.3.6.6	Function is supported	O	Yes [ ] No [ ]
*LTD	PMD lane-by-lane transmit disable function	94.3.6.7	Function is supported	O	Yes [ ] No [ ]
*PDI	Physically instantiated PMD service interface	94.3.4	Interface is supported	O	Yes [ ] No [ ]
*CHNL	Channel	94.4	Channel specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]

94.6.4 PICS proforma tables for Physical Medium Attachment (PMA) sublayer, Physical Medium Dependent (PMD) sublayer, and baseband medium, type 100GBASE-KP4

94.6.4.1 PMA functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
AFS1	Overhead frame	94.2.2.2	Transmitter maps FEC bits to overhead frame	M	Yes [ ]
AFS2	Overhead	94.2.2.3	Transmitter maps sequence overhead bits	M	Yes []
AFS3	Termination blocks	94.2.2.4	Transmitter maps overhead frame bits to termination blocks	M	Yes [ ]
AFS4	Gray mapping	94.2.2.5	Transmitter maps each pair of termination block bits to Gray-mapped symbols	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
AFS5	Precoder	94.2.2.6	Transmitter precodes each Gray-mapped symbol	M	Yes [ ]
AFS6	PAM4 encoder	94.2.2.7	Transmitter maps each pre-coded symbol to PAM4 levels	M	Yes [ ]
AFS7	Transmit symbols	94.2.2.8	Transmitter sends each PAM4 symbol to the PMD	M	Yes [ ]
AFS8	Recover data	94.2.3	Receiver recovers data, meets performance requirements, and removes termination bits and overhead	M	Yes [ ]
AFS9	Overhead	94.2.3.1	Recover overhead sequence	M	Yes [ ]
AFS10	Link status	94.2.6	Provide link status to PMA client via PMA:IS_SIG-NAL.indication primitive	M	Yes [ ]
AFS11	PMA local loopback	94.2.7	Provide loopback from PMA SI input to PMA SI output	M	Yes [ ]
AFS12	PMA remote loopback	94.2.8	Provide loopback from PMA SI output to PMA SI input	O	Yes [ ] No [ ]
AFS13	JP03A pattern	94.2.9.1	Provide JP03A test pattern	M	Yes [ ]
AFS14	JP03B pattern	94.2.9.2	Provide JP03B test pattern	M	Yes [ ]
AFS15	QPRBS13 test pattern	94.2.9.3	Provide QPRBS13 test pattern	M	Yes [ ]
AFS16	Transmitter linearity test pattern	94.2.9.4	Provide transmitter linearity test pattern	M	Yes [ ]
AFS17	PMA control variables	94.2.10	Map PMA control variables to MDIO per Table 94–4	MD:M	Yes [ ] N/A [ ]
AFS18	PMA status variables	94.2.10	Map PMA status variables to MDIO per Table 94–5	MD:M	Yes [ ] N/A [ ]

94.6.4.2 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
DFS1	SIGNAL_OK assignment	94.3.1.3.1	Set SIGNAL_OK based on Global_PMD_signal_detect	M	Yes [ ]
DFS2	Sum of receive and transmit delays in one direction for PMA, PMD, and AN	94.3.3	Less than 8192 bit times	M	Yes [ ]
DFS3	Skew at SP3	94.3.4	Less than 54 ns	M	Yes [ ]
DFS4	Skew variation at SP3	94.3.4	Less than 0.6 ns	M	Yes [ ]
DFS5	Skew at SP4	94.3.4	Less than 134 ns	M	Yes [ ]
DFS6	Skew variation at SP4	94.3.4	Less than 3.4 ns	M	Yes [ ]
DFS7	Skew at SP5	94.3.4	Less than 145 ns	PDI:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DFS8	Skew variation at SP5	94.3.4	Less than 3.6 ns	PDI:M	Yes [ ] N/A [ ]
DFS9	PMD control variables	94.3.5	Map PMD control variables to MDIO per Table 94–6	MD:M	Yes [ ] N/A [ ]
DFS10	PMD status variables	94.3.5	Map PMD status variables to MDIO per Table 94–7	MD:M	Yes [ ] N/A [ ]
DFS11	Transmit function	94.3.6.2	Convert 4 encoded symbol streams from PMD SI to 4 electrical signals at the MDI	M	Yes [ ]
DFS12	Transmit symbol value	94.3.6.2	A positive value for SLi<p> minus SLi<n> corresponds to a positive symbol value	M	Yes [ ]
DFS13	Transmit EEE alert signal	94.3.6.2	Send ALERT frame	EEE:M	Yes [ ] N/A [ ]
DFS14	Transmit EEE alert transmitter setting	94.3.6.2	Using coefficients determined during startup	EEE:M	Yes [ ] N/A [ ]
DFS15	Receive function	94.3.6.3	Convert 4 electrical signals from MDI to 4 encoded symbol streams at the PMD SI	M	Yes [ ]
DFS16	Receive symbol value	94.3.6.3	A positive value for DLi<p> minus DLi<n> corresponds to a positive symbol value	M	Yes [ ]
DFS17	Signal detect parameter	94.3.6.4	Continuously send SIGNAL_DETECT to PMD SI.	M	Yes [ ]
DFS18	PMD_signal_detect_i when training is disabled by management	94.3.6.5	Set to one for all lanes.	M	Yes []
DFS19	PMD_signal_detect_i assertion time	94.3.6.5	Within 500 ns of compliant signal	EEE:M	Yes [ ] N/A [ ]
DFS20	PMD_signal_detect_i when transmitter is disabled	94.3.6.5	Not asserted when transmitter output meets requirements for disabled state	EEE:M	Yes [ ] N/A [ ]
DFS22	Global_PMD_transmit_ disable variable	94.3.6.6	When set to one, all transmitters satisfy the requirements of 94.3.12.3	GTD:M	Yes [ ] N/A [ ]
DFS21	Loopback when transmitter disabled	94.3.6.6	Loopback not affected	GTD:M	Yes [ ] N/A [ ]
DFS22	Transmitter output on transition to QUIET	94.3.6.6	Turn off and meet requirements in 94.3.12.3	EEE:M	Yes [ ] N/A [ ]
DFS23	Transmitter output on transition from QUIET	94.3.6.6	Turn on and meet requirements in 94.3.12.3	EEE:M	Yes [ ] N/A [ ]
DFS24	PMD_transmit_disable_*i* variable	94.3.6.7	When set to one, the transmitter for lane *i* satisfies the requirements of 94.3.12.3	LTD:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DFS25	PMD lane-by-lane transmit disable function affect on loopback	94.3.6.7	No effect	LTD:M	Yes [ ] N/A [ ]
DFS26	Loopback mode	94.3.6.8	Provided in adjacent PMA	M	Yes [ ]
DFS27	Loopback effect	94.3.6.8	Does not affect transmitter	M	Yes [ ]
DFS28	PMD_fault variable mapping to MDIO	94.3.7	Mapped to the fault bit as specified in45.2.1.2.3	MD:M	Yes [ ] N/A [ ]
DFS29	PMD_transmit_fault variable mapping to MDIO	94.3.8	Mapped to Transmit fault bit as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
DFS30	PMD_receive_fault variable mapping to MDIO	94.3.9	Mapped to Receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]
DFS31	Control function	94.3.10.1	Independent per lane	M	Yes [ ]
DFS32	Training variables	94.3.10.1	Map to MDIO bits per 45.2.1.91	MD:M	Yes [ ] N/A [ ]
DFS33	Training frame marker	94.3.10.4	Frame marker encoded per 94.3.10.4	M	Yes [ ]
DFS34	Training frame control channel encoding	94.3.10.5.1	Differential manchester encoding	M	Yes [ ]
DFS35	Training frame control channel DME	94.3.10.5.1	Encoded based on rules in 94.3.10.5.1	M	Yes [ ]
DFS36	Training frame coding violation	94.3.10.5.1	Discard control channel if there is any coding violation	M	Yes [ ]
DFS37	Training frame control channel structure	94.3.10.5.2	Series of DME cells specified in 94.3.10.5.2	M	Yes [ ]
DFS38	Training frame coefficient update field	94.3.10.6	Format per Table 94–9	M	Yes [ ]
DFS39	Training frame coefficient transmission order.	94.3.10.6	Cell 15 first	M	Yes [ ]
DFS40	Training frame preset	94.3.10.6.1	Response per 72.6.10.2.3.1	M	Yes [ ]
DFS41	Training frame initialize	94.3.10.6.2	Response per 72.6.10.2.3.2 and conditions per 94.3.12.5.4	M	Yes [ ]
DFS42	Training frame coefficient update parity	94.3.10.6.3	Set for even parity in coefficient update field.	M	Yes [ ]
DFS43	Training frame coefficient update parity violation	94.3.10.6.3	Discard control channel if parity violation	M	Yes [ ]
DFS44	Training frame coefficient (*k*) update	94.3.10.6.4	Encoded per 94.3.10.6.4	M	Yes [ ]
DFS45	Training and alert frame status report field	94.3.10.7	Format per Table 94–10	M	Yes [ ]
DFS46	Training frame status transmission order	94.3.10.7	Cell 19 first	M	Yes [ ]
DFS47	Training frame status report parity	94.3.10.7.1	Set for even parity in status report field	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DFS48	Training frame status report parity violation	94.3.10.7.1	Discard control channel if parity violation.	M	Yes [ ]
DFS49	Training frame countdown	94.3.10.7.2	Indicate transition per 94.3.10.7.2	M	Yes [ ]
DFS50	Training frame receiver ready	94.3.10.7.3	Signal local receiver state per 94.3.10.7.3	M	Yes [ ]
DFS51	Training frame coefficient status	94.3.10.7.4	Behavior per 72.6.10.2.4.5.	M	Yes [ ]
DFS52	Training frame coefficient update process	94.3.10.7.5	Update coefficients per 72.6.10.2.5	M	Yes [ ]
DFS53	PMD control response time	94.3.10.7.5	Response time less than 2 ms	M	Yes [ ]
DFS54	Training frame training pattern	94.3.10.8	Encode per 94.3.10.8	M	Yes [ ]
DFS55	Signal on transition from training mode to data mode	94.3.10.9	Signal according to 94.3.10.9	M	Yes [ ]
DFS56	Training frame lock state diagram	94.3.10.10	Implement per Figure 72–4 and 72.6.10.3.	M	Yes [ ]
DFS57	Training state diagram	94.3.10.11	Implement per Figure 72–5 and 72.6.10.3	M	Yes [ ]
DFS58	Transmitter setting in INITIALIZE state	94.3.10.11	Transmitter configured according to 94.3.12.5.4	M	Yes [ ]
DFS59	Coefficient update state diagram	94.3.10.12	Implement per Figure 72–6 and 72.6.10.3	M	Yes [ ]
DFS60	Alert frame	94.3.11.1	Structure per Figure 94–8	EEE:M	Yes [ ] N/A [ ]
DFS61	Alert frame marker	94.3.11.1.1	Implement per 94.3.10.4	EEE:M	Yes [ ] N/A [ ]
DFS62	Alert frame coefficient update field	94.3.11.1.2	Transmitted as all zeros	EEE:M	Yes [ ] N/A [ ]
DFS63	Alert frame status report field	94.3.11.1.3	Format per Table 94–10	EEE:M	Yes [ ] N/A [ ]
DFS64	Alert frame status report field order of transmission	94.3.11.1.3	Transmit cell 19 first	EEE:M	Yes [ ] N/A [ ]
DFS65	Alert frame status report parity	94.3.11.1.4	Behavior per 94.3.10.7.1	EEE:M	Yes [ ] N/A [ ]
DFS66	Alert frame mode	94.3.11.1.5	Always set to 1	EEE:M	Yes [ ] N/A [ ]
DFS67	Alert frame countdown	94.3.11.1.6	Indicate transition per 94.3.10.7.2	EEE:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DFS68	Alert frame PMA alignment offset	94.3.11.1.7	Indicate relative position of PMA frame and encoded per 94.3.11.1.7	EEE:M	Yes [ ] N/A [ ]
DFS69	Alert frame receiver ready	94.3.11.1.8	Always set to 1	EEE:M	Yes [ ] N/A [ ]
DFS70	Signal on transition from alert to data mode	94.3.11.1.9	Signal according to 94.3.11.1.9	M	Yes [ ]

94.6.4.3 PMD transmitter characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Test fixture impedance	94.3.12.1.1	100 Ω	M	Yes [ ]
TC2	Test fixture differential return loss	94.3.12.1.1	Equation (94–4)	M	Yes [ ]
TC3	Test fixture common-mode return loss	94.3.12.1.1	Equation (94–5)	M	Yes [ ]
TC4	Test fixture differential insertion loss	94.3.12.1.2	≥ 1.2 dB and ≤ 1.6 dB at 12.89 GHz.	M	Yes [ ]
TC5	Test fixture insertion loss deviation	94.3.12.1.2	Magnitude < 0.1 dB	M	Yes [ ]
TC6	Signaling rate per lane	94.3.12.2	13.59375 GBd ± 100 ppm	M	Yes [ ]
TC7	Peak-to-peak differential output voltage	94.3.12.3	≤ 1200 mV regardless of transmit equalizer setting	M	Yes [ ]
TC8	Peak-to-peak differential output voltage, transmitter disabled	94.3.12.3	≤ 30 mV	M	Yes [ ]
TC9	DC common-mode output voltage	94.3.12.3	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC10	AC common-mode output voltage	94.3.12.3	≤ 30 mV RMS regardless of transmit equalizer setting	M	Yes [ ]
TC11	EEE transmitter output level when disabled	94.3.12.3	< 35 mV peak-to-peak differential within 500 ns	EEE:M	Yes [ ] N/A [ ]
TC12	EEE transmitter output level when enabled	94.3.12.3	90% of steady-state voltage by third alert frame marker and meet requirements of 94.3.12 with 1 μs	EEE:M	Yes [ ] N/A [ ]
TC13	Transmitter output DC common-mode voltage when disabled	94.3.12.3	Within ±150 mV of value when transmitter is enabled	M	Yes [ ]
TC14	Differential output return loss	94.3.12.4	Equation (94–7) with 100 Ω reference impedance	M	Yes [ ]
TC15	Common-mode output return loss	94.3.12.4	Equation (94–8) with 25 Ω reference impedance	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC16	Level separation mismatch ratio, R_{LM}	94.3.12.5.1	> 0.92	M	Yes []
TC17	Steady-state voltage, v_f	94.3.12.5.3	≥ 0.4 V and ≤ 0.6 V after the transmit equalizer coefficients have been set to the "preset" values	M	Yes [ ]
TC18	Linear fit pulse peak	94.3.12.5.3	> 0.85 × v_f after the transmit equalizer coefficients have been set to the "preset" values	M	Yes [ ]
TC19	Coefficient initialization	94.3.12.5.4	Satisfies the requirements of 94.3.12.5.4	M	Yes [ ]
TC20	Normalized coefficient step size for "increment"	94.3.12.5.5	Between 0.0083 and 0.05	M	Yes [ ]
TC21	Normalized coefficient step size for "decrement"	94.3.12.5.5	Between –0.05 and –0.0083	M	Yes [ ]
TC22	Maximum post-cursor equalization ratio	94.3.12.5.6	≥ 4	M	Yes [ ]
TC23	Maximum pre-cursor equalization ratio	94.3.12.5.6	≥ 1.54	M	Yes [ ]
TC24	Clock random jitter RMS	94.3.12.6.1	≤ 0.005 UI RMS regardless of the transmit equalization setting	M	Yes [ ]
TC25	Clock deterministic jitter	94.3.12.6.1	≤ 0.05 UI regardless of the transmit equalization setting	M	Yes [ ]
TC26	Even-odd jitter	94.3.12.6.2	≤ 0.03 UI regardless of the transmit equalization setting	M	Yes [ ]
TC27	SNDR	94.3.12.7	≥ 31 dB	M	Yes [ ]

94.6.4.4 PMD receiver characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Test fixture insertion loss	94.3.13.1	Meet requirements in 94.3.12.1	M	Yes [ ]
RC2	Differential input return loss	94.3.13.2	Meets Equation (94–7) measured with a reference impedance of 100 Ω.	M	Yes [ ]
RC3	Differential to common-mode return loss	94.3.13.2	Meets Equation (94–21).	M	Yes [ ]
RC4	Interference tolerance	94.3.13.3	Satisfy requirements in Table 94–15	M	Yes [ ]
RC5	Jitter tolerance	94.3.13.4	Satisfy requirements in Table 94–16	M	Yes [ ]

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94.6.4.5 Channel characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	94.4.1	Greater than or equal to 3 dB	CHNL:M	Yes [ ] N/A [ ]
CC2	AC-coupling	94.4.4	Channel AC-couples the transmitter to the receiver	CHNL:M	Yes [ ] N/A [ ]
CC3	AC-coupling 3 dB cut-off frequency	94.4.4	Less than 50 kHz	CHNL:M	Yes [ ] N/A [ ]

94.6.4.6 Environment specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	94.5.1	Conforms to J.2	M	Yes [ ]
ES2	Electromagnetic interference	94.5.4	Complies with applicable local and national codes	M	Yes [ ]

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95. Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-SR4

95.1 Overview

This clause specifies the 100GBASE-SR4 PMD together with the multimode fiber medium. The PMD sublayer provides a point-to-point 100 Gb/s Ethernet link over four pairs of multimode fiber, up to at least 100 m. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 95–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 95–1—Physical Layer clauses associated with the 100GBASE-SR4 PMD

Associated clause	100GBASE-SR4
81—RS	Required
81—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
83—PMA for 100GBASE-R	Required
91—RS-FEC[b]	Required
83A—CAUI-10	Optional
83B—Chip-to-module CAUI-10[c]	Optional
83D—CAUI-4	Optional
83E—Chip-to-module CAUI-4	Optional
78—Energy Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation behaves functionally as though the RS and CGMII were present.
[b]The option to bypass the Clause 91 RS-FEC correction function is not supported.
[c]This option requires the RS-FEC sublayer to be within the module. See 91.3.

Figure 95–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 40 Gb/s and 100 Gb/s Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2.

100GBASE-SR4 PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Further relevant information may be found in Clause 1 (terminology and conventions, references, definitions and abbreviations) and Annex A (bibliography, referenced as [B1], [B2], etc.).

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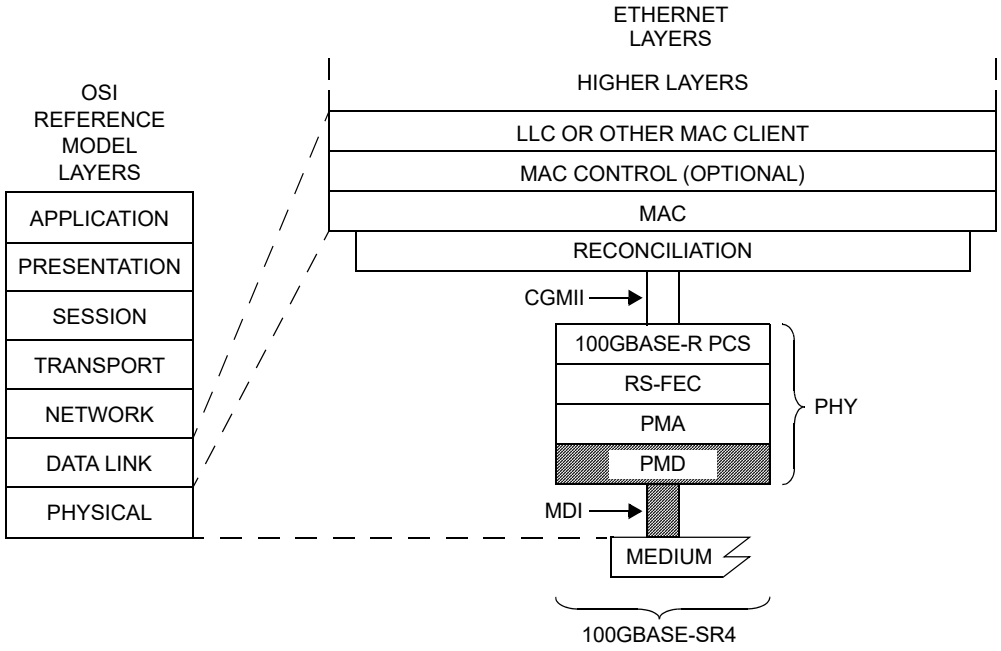

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
SR = PMD FOR MULTIMODE FIBER

Figure 95–1—100GBASE-SR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

95.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 5×10^{-5} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap when processed according to Clause 91.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap when processed according to Clause 91.

95.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-SR4 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 80.3. The PMD service interface primitives are summarized as follows:

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PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 100GBASE-SR4 PMD has four parallel bit streams, hence i = 0 to 3.

In the transmit direction, the PMA continuously sends four parallel bit streams to the PMD, one per lane, each at a nominal signaling rate of 25.78125 GBd. The PMD converts these streams of bits into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends four parallel bit streams to the PMA corresponding to the signals received from the MDI, one per lane, each at a nominal signaling rate of 25.78125 GBd.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication(SIGNAL_OK) inter-sublayer service primitive defined in 80.3.

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_bit parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_bit parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 95.1.1.

95.3 Delay and Skew

95.3.1 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the 100GBASE-SR4 PMD including 2 m of fiber in one direction shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

95.3.2 Skew constraints

The Skew (relative delay) between the lanes is kept within limits so that the information on the lanes can be reassembled by the RS-FEC sublayer. Skew and Skew Variation are defined in 80.5 and specified at the points SP0 to SP7 shown in Figure 80–9.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5. The measurements of Skew and Skew Variation are defined in 86.8.3.1 with the exception that the clock and data recovery units' high-frequency corner bandwidths are 10 MHz.

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95.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 95–2, and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 95–3.

Table 95–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable 3	PMD transmit disable register	1.9.4	PMD_transmit_disable_3
PMD transmit disable 2	PMD transmit disable register	1.9.3	PMD_transmit_disable_2
PMD transmit disable 1	PMD transmit disable register	1.9.2	PMD_transmit_disable_1
PMD transmit disable 0	PMD transmit disable register	1.9.1	PMD_transmit_disable_0

Table 95–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect 3	PMD receive signal detect register	1.10.4	PMD_signal_detect_3
PMD receive signal detect 2	PMD receive signal detect register	1.10.3	PMD_signal_detect_2
PMD receive signal detect 1	PMD receive signal detect register	1.10.2	PMD_signal_detect_1
PMD receive signal detect 0	PMD receive signal detect register	1.10.1	PMD_signal_detect_0

95.5 PMD functional specifications

The 100GBASE-SR4 PMD performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

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95.5.1 PMD block diagram

The PMD block diagram is shown in Figure 95–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a multimode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 95.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 95.11.3). Unless specified otherwise, all receiver measurements and tests defined in 95.8 are made at TP3.

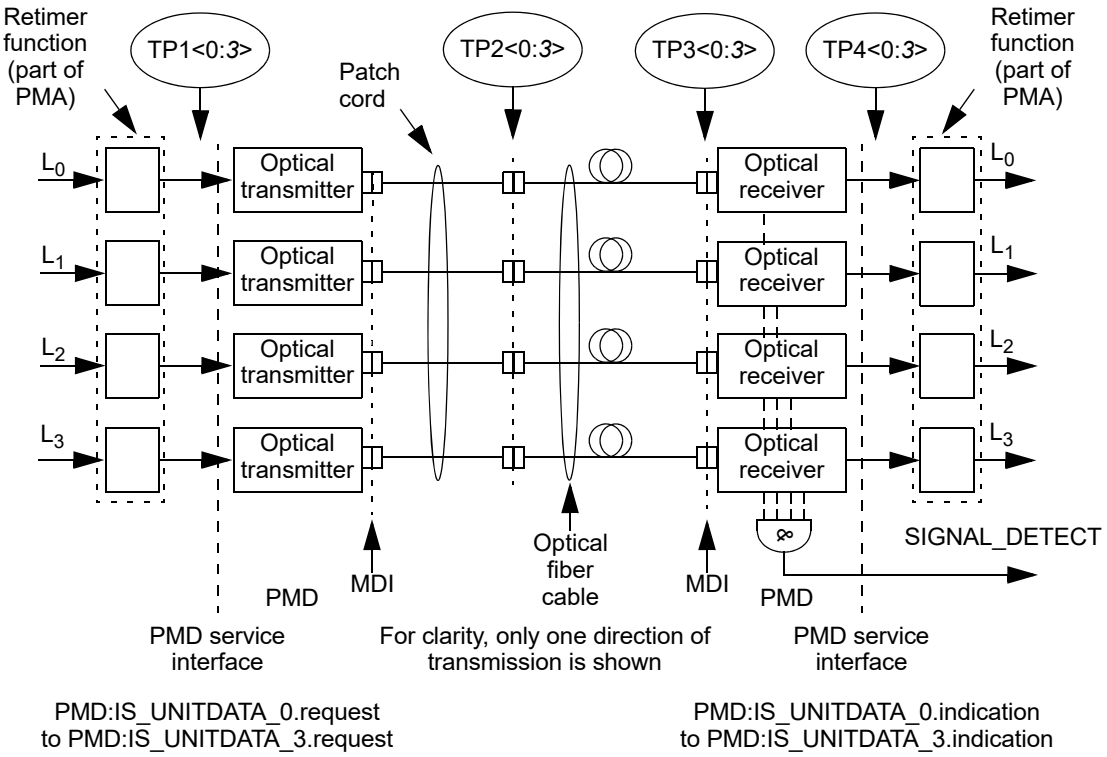

Figure 95–2—Block diagram for 100GBASE-SR4 transmit/receive paths

TP1<0:3> and TP4<0:3> are optional reference points that may be useful to implementers for testing components (these test points will not typically be accessible in an implemented system).

95.5.2 PMD transmit function

The PMD Transmit function shall convert the four bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request into four separate optical signals. The four optical signals shall then be delivered to the MDI, which contains four parallel light paths for transmit, according to the transmit optical specifications in this clause. The higher optical power level in each signal shall correspond to tx_bit = one.

95.5.3 PMD receive function

The PMD Receive function shall convert the four parallel optical signals received from the MDI into separate bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to rx_bit = one.

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95.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 80.3.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all four lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 95–4. The PMD receiver is not required to verify whether a compliant 100GBASE-SR4 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 95–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –30 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ average receive power, each lane (min) in Table 95–7) AND (compliant 100GBASE-SR4 signal input)]	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

95.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:3, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 95–4.

95.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

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95.5.7 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 95–6.
b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter in each lane.

95.5.8 PMD lane-by-lane transmit disable function (optional)

The PMD lane-by-lane transmit disable function is optional and allows the optical transmitter in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:3) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 95–6.
b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the optical transmitter in each lane.

If the optional PMD lane-by-lane transmit disable function is not implemented in MDIO, an alternative method may be provided to independently disable each transmit lane.

95.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

95.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set PMD_transmit_fault to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

95.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

95.6 Lane assignments

There are no lane assignments (within a group of transmit or receive lanes) for 100GBASE-SR4. While it is expected that a PMD will map electrical lane *i* to optical lane *i* and vice versa, there is no need to define the

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physical ordering of the lanes, as the RS-FEC sublayer is capable of receiving the lanes in any arrangement. The positioning of transmit and receive lanes at the MDI is specified in 95.11.3.1.

95.7 PMD to MDI optical specifications for 100GBASE-SR4

The operating range for the 100GBASE-SR4 PMD is defined in Table 95–5. A 100GBASE-SR4 compliant PMD operates on 50/125 μm multimode fibers, type A1a.2 (OM3) or type A1a.3 (OM4), according to the specifications defined in Table 95–12. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 100GBASE-SR4 PMD operating at 120 m meets the operating range requirement of 0.5 m to 100 m).

Table 95–5—100GBASE-SR4 operating range

PMD type	Required operating range[a]
100GBASE-SR4	0.5 m to 70 m for OM3
	0.5 m to 100 m for OM4

[a]The RS-FEC correction function may not be bypassed for any operating distance.

95.7.1 100GBASE-SR4 transmitter optical specifications

Each lane of a 100GBASE-SR4 transmitter shall meet the specifications in Table 95–6 per the definitions in 95.8.

Table 95–6—100GBASE-SR4 transmit characteristics

Description	Value	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm	GBd
Center wavelength (range)	840 to 860	nm
RMS spectral width[a] (max)	0.6	nm
Average launch power, each lane (max)	2.4	dBm
Average launch power, each lane (min)	–8.4	dBm
Optical Modulation Amplitude (OMA), each lane (max)	3	dBm
Optical Modulation Amplitude (OMA), each lane (min)[b]	–6.4	dBm
Launch power in OMA minus TDEC (min)	–7.3	dBm
Transmitter and dispersion eye closure (TDEC), each lane (max)	4.3	dB
Average launch power of OFF transmitter, each lane (max)	–30	dBm
Extinction ratio (min)	2	dB
Optical return loss tolerance (max)	12	dB

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Table 95–6—100GBASE-SR4 transmit characteristics *(continued)*

Description	Value	Unit
Encircled flux[c]	≥ 86% at 19 μm ≤ 30% at 4.5 μm	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 1.5×10^{-3} hits per sample	{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}	

[a]RMS spectral width is the standard deviation of the spectrum.
[b]Even if the TDEC < 0.9 dB, the OMA (min) has to exceed this value.
[c]If measured into type A1a.2 or type A1a.3 50 μm fiber in accordance with IEC 61280-1-4:2009.

95.7.2 100GBASE-SR4 receive optical specifications

Each lane of a 100GBASE-SR4 receiver shall meet the specifications in Table 95–7 per the definitions in 95.8.

Table 95–7—100GBASE-SR4 receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	25.78125 ± 100 ppm	GBd
Center wavelength (range)	840 to 860	nm
Damage threshold[a] (min)	3.4	dBm
Average receive power, each lane (max)	2.4	dBm
Average receive power, each lane[b] (min)	–10.3	dBm
Receive power, each lane (OMA) (max)	3	dBm
Receiver reflectance (max)	–12	dB
Stressed receiver sensitivity (OMA), each lane[c] (max)	–5.2	dBm
Conditions of stressed receiver sensitivity test:[d]		
Stressed eye closure (SEC), lane under test	4.3	dB
Stressed eye J2 Jitter, lane under test	0.39	UI
Stressed eye J4 Jitter, lane under test (max)	0.53	UI
OMA of each aggressor lane	3	dBm
Stressed receiver eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5×10^{-5} hits per sample	{0.28, 0.5, 0.5, 0.33, 0.33, 0.4}	

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
[b]Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Measured with conformance test signal at TP3 (see 95.8.8) for the BER specified in 95.1.1.
[d]These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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95.7.3 100GBASE-SR4 illustrative link power budget

An illustrative power budget and penalties for 100GBASE-SR4 channels are shown in Table 95–8.

Table 95–8—100GBASE-SR4 illustrative link power budget

Parameter	OM3	OM4	Unit
Effective modal bandwidth at 850 nm[a]	2000	4700	MHz.km
Power budget (for max TDEC)	8.2		dB
Operating distance	0.5 to 70	0.5 to 100	m
Channel insertion loss[b]	1.8	1.9	dB
Allocation for penalties[c] (for max TDEC)	6.3		dB
Additional insertion loss allowed	0.1	0	dB

[a]Per IEC 60793-2-10.
[b]The channel insertion loss is calculated using the maximum distance specified in Table 95–5 and cabled optical fiber attenuation of 3.5 dB/km at 850 nm plus an allocation for connection and splice loss given in 95.11.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

95.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

95.8.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 95–10 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 95–10 may be used to perform that test. As Pattern 3 is more demanding than Pattern 5 (which itself is the same or more demanding than other 100GBASE-R bit streams) an item that is compliant using Pattern 5 is considered compliant even if it does not meet the required limit using Pattern 3. The test patterns used in this clause are shown in Table 95–9.

Table 95–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 ones, 8 zeros)	83.5.10
3	PRBS31	83.5.10
4	PRBS9	83.5.10
5[a]	RS-FEC encoded scrambled idle	82.2.11[a]

[a]The pattern defined in 82.2.11 as encoded by Clause 91 RS-FEC for 100GBASE-SR4.

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Table 95–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength, spectral width	3, 5 or valid 100GBASE-SR4 signal	95.8.2
Average optical power	3, 5 or valid 100GBASE-SR4 signal	95.8.3
Optical modulation amplitude (OMA)	Square wave or 4	95.8.4
Transmitter and dispersion eye closure (TDEC)	3, 5 or valid 100GBASE-SR4 signal	95.8.5
Extinction ratio	3, 5 or valid 100GBASE-SR4 signal	95.8.6
Transmitter optical waveform	3, 5 or valid 100GBASE-SR4 signal	95.8.7
Stressed receiver sensitivity	3, 5 or valid 100GBASE-SR4 signal	95.8.8
Stressed eye closure (SEC), calibration	3, 5 or valid 100GBASE-SR4 signal	95.8.8

95.8.1.1 Multi-lane testing considerations

Stressed receiver sensitivity is defined for an interface at the BER specified in 95.1.1. The interface BER is the average of the four BERs of the receive lanes when they are stressed.

Measurements with Pattern 3 (PRBS31) allow lane-by-lane BER measurements. Measurements with Pattern 5 (RS-FEC encoded scrambled idle) give the interface BER if all lanes are stressed at the same time. If each lane is stressed in turn, the BER is diluted by the three unstressed lanes, and the BER for that stressed lane alone has to be found, e.g., by multiplying by four if the unstressed lanes have low BER. In stressed receiver sensitivity measurements, unstressed lanes may be created by setting the power at the receiver under test well above its sensitivity and/or not stressing those lanes with ISI and jitter, or by other means. Each receive lane is stressed in turn while all are operated. All aggressor lanes are operated as specified. To find the interface BER, the BERs of all the lanes when stressed are averaged.

Where relevant, parameters are defined with all co-propagating and counter-propagating lanes operational so that crosstalk effects are included. Where not otherwise specified, the maximum amplitude (OMA or VMA) for a particular situation is used, and for counter-propagating lanes, the minimum transition time is used. Alternative test methods that generate equivalent results may be used. While the lanes in a particular direction may share a common clock, the Tx and Rx directions are not synchronous to each other. If Pattern 3 is used for the lanes not under test using a common clock, there is at least 31 UI delay between the PRBS31 patterns on one lane and any other lane.

95.8.2 Center wavelength and spectral width

The center wavelength and RMS spectral width of each optical lane shall be within the range given in Table 95–6 if measured per IEC 61280-1-3. The lane under test is modulated using one of the test patterns specified in Table 95–10.

95.8.3 Average optical power

The average optical power of each lane shall be within the limits given in Table 95–6 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using the test pattern defined in Table 95–10.

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95.8.4 Optical Modulation Amplitude (OMA)

OMA shall be within the limits given in Table 95–6 if measured as defined in 52.9.5 for measurement with a square wave (8 ones, 8 zeros) test pattern or as defined in 68.6.2 (from the variable MeasuredOMA in 68.6.6.2) for measurement with a PRBS9 test pattern, with the exception that each optical lane is tested individually. See 95.8.1 for test pattern information.

95.8.5 Transmitter and dispersion eye closure (TDEC)

TDEC of each lane shall be within the limits given in Table 95–6 if measured using the methods specified in 95.8.5.1 and 95.8.5.2.

TDEC is a measure of each optical transmitter's vertical eye closure; it is based upon vertical histogram data from an eye diagram measured through an optical to electrical converter (O/E) with a bandwidth equivalent to a combined reference receiver and worst case optical channel. Table 95–10 specifies the test patterns to be used for measurement of TDEC.

95.8.5.1 TDEC conformance test setup

A block diagram for the TDEC conformance test is shown in Figure 95–3. Other measurement implementations may be used with suitable calibration.

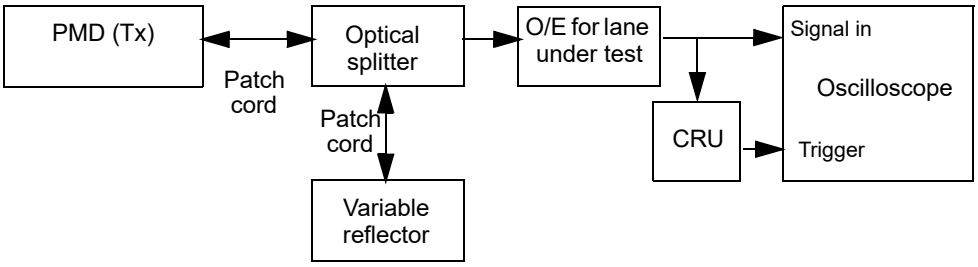

Figure 95–3—TDEC conformance test block diagram

Each optical lane is tested individually with all other lanes in operation. The optical splitter and variable reflector are adjusted so that each transmitter is tested with an optical return loss of 12 dB.

The combination of the O/E and the oscilloscope used to measure the optical waveform has a fourth-order Bessel-Thomson filter response with a bandwidth of 12.6 GHz. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The clock recovery unit (CRU) has a corner frequency of 10 MHz and a slope of 20 dB/decade.

95.8.5.2 TDEC measurement method

The oscilloscope is set up to accumulate samples of the optical eye diagram for the transmitter under test, as illustrated in Figure 95–4.

OMA is measured according to 95.8.4.

The standard deviation of the noise of the O/E and oscilloscope combination, *S*, is determined with no optical input signal and the same settings as used to capture the histograms described below.

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The average optical power (P_{ave}), the crossing points of the eye diagram, and the four vertical histograms used to calculate TDEC, are all measured using the same test pattern selected from those identified for TDEC in Table 95–10. The 0 UI and 1 UI crossing points are determined by the average of the eye diagram crossing times, as measured at P_{ave}, as illustrated in Figure 95–4.

Four vertical histograms are measured through the eye diagram, centered at 0.4 UI and 0.6 UI, and above and below P_{ave}, as illustrated in Figure 95–4.

Each histogram window has a width of 0.04 UI. Each histogram window has an inner height boundary, which is set close to P_{ave} (so that no further samples would be captured by moving it closer to P_{ave}), and an outer height boundary, which is set beyond the outer-most samples of the eye diagram (so that no further samples would be captured by increasing the outer boundary of the histogram window).

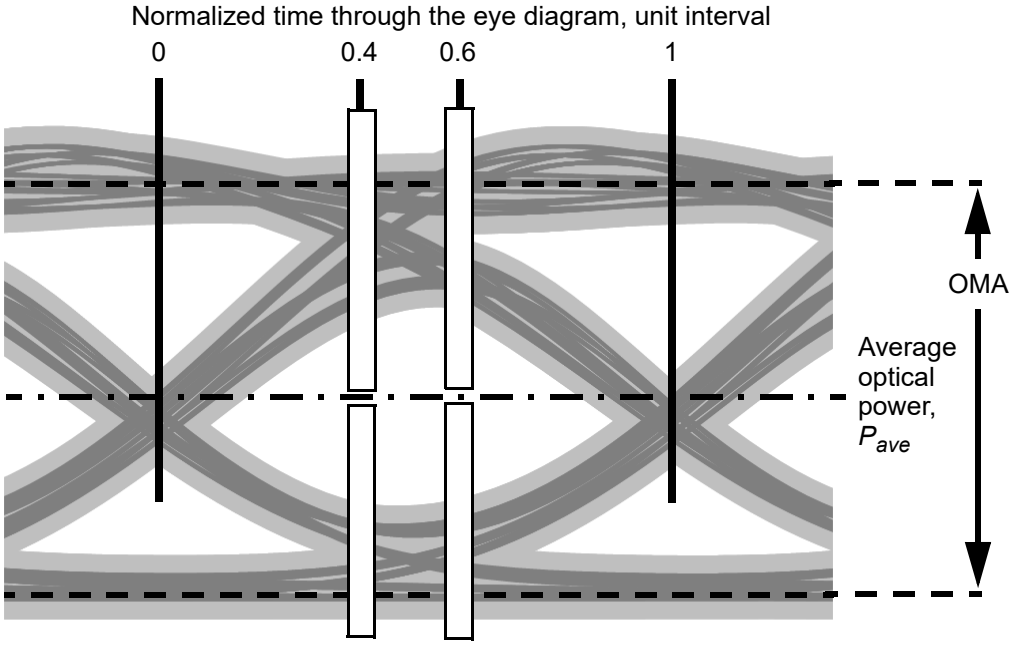

Figure 95–4—Illustration of the TDEC measurement

The distributions of the two histograms on the left are each multiplied by Q functions, which represent an estimate of the probability of errors caused by each part of the distribution for the greatest tolerable noise that could be added by an optical channel and a receiver. The resulting distributions are integrated and each integral is divided by the integral of the distribution it was derived from, giving two bit error probabilities. The Q function uses a standard deviation, σ_L, chosen so that the average of these two bit error probabilities is 5×10^{-5}. Similarly, for the two histograms on the right, a standard deviation, σ_R, is found.

Q(x) is the area under a Normal curve for values larger than *x* (the tail probability, related to the "complementary error function"), as shown in Equation (95–1):

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$$Q(x) = \int_{x}^{\infty} \frac{e^{(-z^2/2)}}{\sqrt{2\pi}} dz \tag{95–1}$$

where

x	is $(y–P_{ave})/\sigma_G$ or $(P_{ave}–y)/\sigma_G$, as in Equation (95–2)

This procedure finds a value of σ_G such that Equation (95–2) is satisfied:

$$\frac{1}{2}\left(\frac{\int fu(y)Q\left(\frac{y-P_{ave}}{\sigma_G}\right)dy}{\int fu(y)dy}\right) + \frac{1}{2}\left(\frac{\int fl(y)Q\left(\frac{P_{ave}-y}{\sigma_G}\right)dy}{\int fl(y)dy}\right) = 5\times10^{-5} \tag{95–2}$$

where

$fu(y), fl(y)$	are the upper and lower distributions
σ_G	is the left or right standard deviation, σ_L or σ_R

The lesser of σ_L and σ_R is N.

The noise, R, that could be added by a receiver is given by Equation (95–3).

$$R = (1 - M_1)\sqrt{N^2 + S^2 - M_2^2} \tag{95–3}$$

where

M_1, M_2	defined in Equation (95–4) and Equation (95–5), account for mode partition noise and modal noise that could be added by the optical channel
S	is the standard deviation of the noise of the O/E and oscilloscope combination

$$M_1 = 0.04 \tag{95–4}$$

$$M_2 = 0.0175P_{ave} \tag{95–5}$$

where

P_{ave}	is the average optical power of the eye diagram.

TDEC is given by Equation (95–6).

$$TDEC = 10\log_{10}\left(\frac{OMA}{2} \times \frac{1}{3.8906R}\right) \tag{95–6}$$

where

OMA	is the optical modulation amplitude as defined in 95.8.4

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The factor 3.8906 is chosen for consistency with the BER of 5×10^{-5} given in 95.1.1.

The method described in 95.8.5.1 and 95.8.5.2 is the reference measurement method. Other equivalent measurement methods may be used with suitable calibration.

95.8.6 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 95–6 if measured using the methods specified in IEC 61280-2-2. The extinction ratio is measured using one of the test patterns specified for extinction ratio in Table 95–10.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 95–10).

95.8.7 Transmitter optical waveform (transmit eye)

The required optical transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 86–4 with the transmitter eye mask coordinates and hit ratio in Table 95–6. The transmitter optical waveform of a port transmitting the test pattern specified in Table 95–10 shall meet specifications according to the methods specified in 86.8.4.6.1 with the following exceptions:

— The clock recovery unit's high-frequency corner bandwidth is 10 MHz.
— The filter nominal reference frequency f_r is 19.34 GHz and the filter tolerances are as specified for STM-64 in ITU-T G.691.

Compensation may be made for variation of the reference receiver filter response from an ideal fourth-order Bessel-Thomson response and for any excess reference receiver noise.

95.8.8 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 95–7 if measured using the method defined by 95.8.8.1 and 95.8.8.5, with the conformance test signal at TP3 as described in 95.8.8.2.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Pattern 3 or Pattern 5, or a valid 100GBASE-SR4 signal is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal. The interface BER of the PMD receiver is the average of the BER of all receive lanes while stressed and at the specified receive OMA.

95.8.8.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 95–5. The patterns used for the received conformance signal are specified in Table 95–10. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 95.8.8.2 and has sinusoidal jitter applied as specified in 95.8.8.5. A suitable test set is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics. The fourth-order Bessel-Thomson filter has a 3 dB bandwidth of approximately 19 GHz. The low-pass filter is used to create ISI. The combination of the low-pass filter and the E/O converter should have a frequency response that results in the level of stressed eye closure (SEC) before the sinusoidal and Gaussian noise terms are added, as described in 95.8.8.2.

The sinusoidal amplitude interferer 1 causes jitter that is intended to emulate instantaneous bit shrinkage that can occur with DDJ. This type of jitter cannot be created by simple phase modulation. The sinusoidal amplitude interferer 2 causes additional eye closure, but in conjunction with the finite edge rates from the limiter, also causes some jitter. The sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferers may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic

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relationships between the sinusoidal interferers, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The Gaussian noise generator, the amplitude of the sinusoidal interferers, and the low-pass filter are adjusted so that the SEC and stressed eye J2 Jitter specifications given in Table 95–7 are met simultaneously, while the maximum stressed eye J4 Jitter specified in Table 95–7 is not exceeded, and while also passing the stressed receiver eye mask in Table 95–7 according to the methods specified in 95.8.7 (the random noise effects such as RIN, or random clock jitter, do not need to be minimized).

For improved visibility for calibration, all elements in the signal path (cables, DC blocks, E/O converter, etc.) should have wide and smooth frequency response, and linear phase response, throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be minimized.

The stressed receiver conformance test signal verification is described in 95.8.8.4.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Each receive lane is tested in turn while all aggressor receive lanes are operated as specified in Table 95–7. Pattern 3, Pattern 5, or a valid 100GBASE–SR4 signal is sent from the transmit section of the receiver under test. The signal being transmitted is asynchronous to the received signal. If Pattern 3 is used with a common clock for the transmit or receive lanes not under test, there is at least 31 UI delay between the PRBS31 patterns generated on one lane and any other lane.

For 100GBASE-SR4 the relevant BER is the interface BER at the PMD service interface. The interface BER is the average of the four BER of the receive lanes when stressed: see 95.8.1.1. If present, the RS-FEC sublayer can measure the lane symbol error ratio at its input. The lane BER can be assumed to be one tenth of the lane symbol error ratio. If each lane is stressed in turn, the PMD interface BER is the average of the BERs of all the lanes when stressed: see 95.8.1.1.

95.8.8.2 Stressed receiver conformance test signal characteristics and calibration

The conformance test signal is used to validate that each lane of the PMD receiver meets BER requirements with near worst-case waveforms at TP3.

The primary parameters of the stressed receiver conformance test signal are its stressed eye closure (SEC), stressed eye J2 Jitter, and stressed eye J4 Jitter. The SEC of the stressed receiver conformance test signal is measured according to 95.8.5, except that the combination of the O/E and the oscilloscope used to measure the waveform has a fourth-order Bessel-Thomson filter response with a bandwidth of 19.34 GHz, and the values of M_1 and M_2 in Equation (95–3) are set to zero. Stressed eye J2 Jitter and stressed eye J4 Jitter are defined in 95.8.8.3.

An example stressed receiver conformance test setup is shown in Figure 95–5; however, alternative test setups that generate equivalent stress conditions may be used.

The following steps describe a possible method for setting up and calibrating a stressed receiver conformance test signal when using a stressed receiver conformance test setup as shown in Figure 95–5:

1) Set the signaling rate of the test pattern generator to meet the requirements in Table 95–7.
2) With the sinusoidal jitter, sinusoidal interferers, and the Gaussian noise generator turned off, set the extinction ratio of the E/O to approximately the minimum specified in Table 95–6.
3) The required values of SEC and J2 Jitter, and the maximum value of J4 Jitter of the stressed receiver conformance test signal are given in Table 95–7. A valid stressed receiver conformance test signal may have a lower value of J4 jitter than the maximum specified in Table 95–7, provided it meets the required values of SEC and J2 Jitter.

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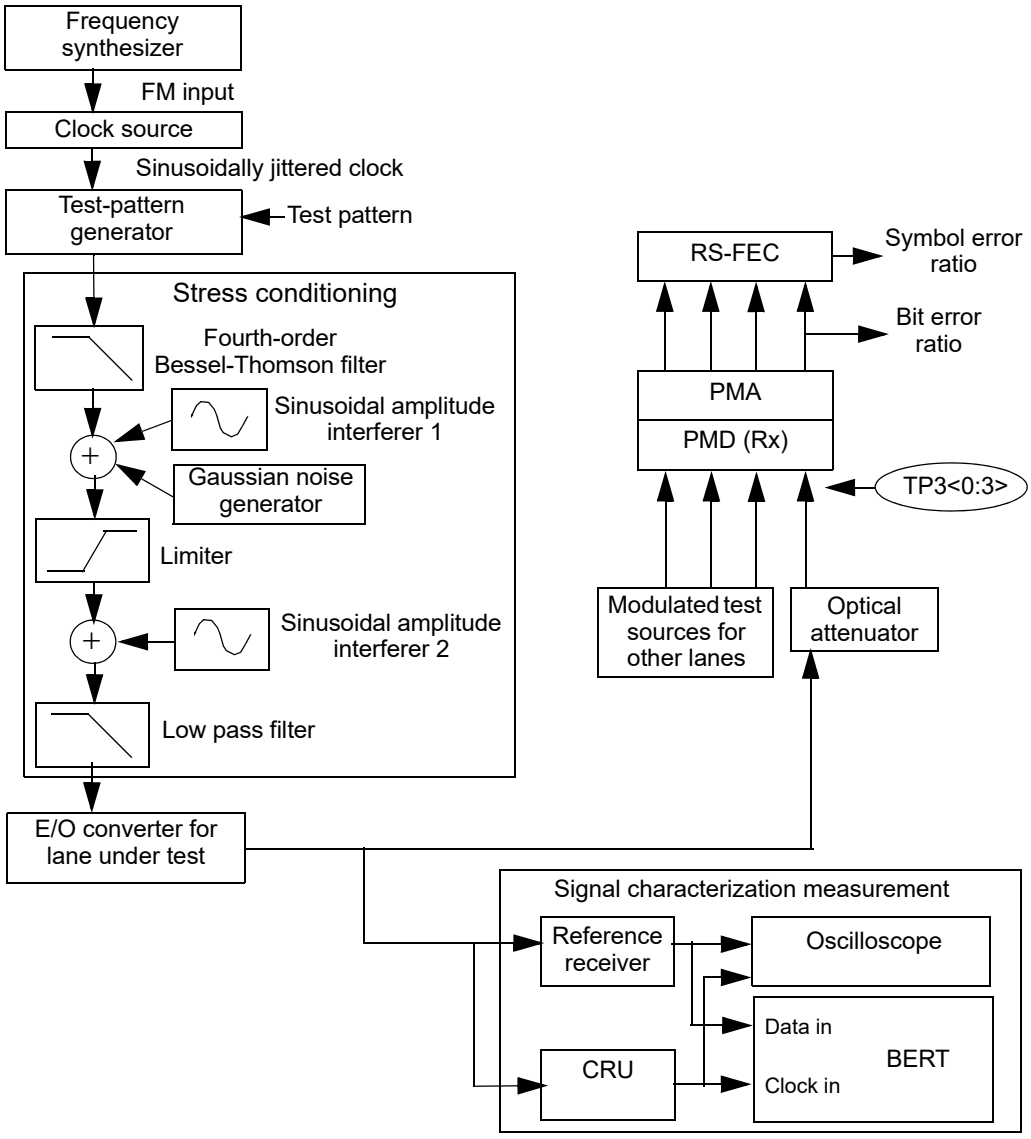

Figure 95–5—Stressed receiver conformance test block diagram

With the sinusoidal jitter, sinusoidal interferer 1, sinusoidal interferer 2, and the Gaussian noise generator turned off, at least 2.5 dB of SEC should be created by the selection of the appropriate bandwidth for the combination of the low-pass filter and the E/O converter. Any remaining SEC has to be created with a combination of sinusoidal jitter, sinusoidal interference, and Gaussian noise.

Sinusoidal jitter is added as specified in Table 95–11. When calibrating the conformance signal, the sinusoidal jitter frequency should be between 50 MHz and 10 times LB as defined in Table 95–11. Sinusoidal jitter amplitude may be calibrated by measuring the jitter on the oscilloscope, while transmitting the square wave pattern, and using a clean clock in place of the CRU to trigger the oscilloscope.

Iterate the adjustments of sinusoidal interferers and Gaussian noise generator and extinction ratio until the values of SEC and stressed eye J2 Jitter are met, while also meeting the following conditions: the maximum value of stressed eye J4 Jitter, as specified in Table 95–7, is not exceeded; the extinction ratio is approximately the minimum specified in Table 95–6; and sinusoidal jitter is as specified in Table 95–11.

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Each receiver lane is conformance tested in turn. The source for the lane under test is adjusted to supply a signal at the input to the receiver under test at the "Stressed receiver sensitivity (OMA), each lane (max)" specified in Table 95–7, and the test sources for the other lanes are set to the "OMA of each aggressor lane" specified in Table 95–7.

95.8.8.3 J2 and J4 Jitter

J2 Jitter is defined as the time interval at the average optical power level that includes all but 10^{-2} of the jitter distribution, which is the time interval from the 0.5th to the 99.5th percentile of the jitter histogram. J2 Jitter is defined using a clock recovery unit as in 95.8.7. If measured using an oscilloscope, the histogram should include at least 10 000 hits and should be taken over about 1% of the signal amplitude. If measured by plotting BER vs. decision time, J2 is the time interval between the two points with a BER of 2.5×10^{-3}.

J4 Jitter is defined as the time interval at the average optical power level that includes all but 10^{-4} of the jitter distribution. J4 Jitter is defined using a clock recovery unit as in 95.8.7. If measured using an oscilloscope, the histogram should include at least 1 000 000 hits and should be taken over about 1% of the signal amplitude. If measured by plotting BER vs. decision time, J4 is the time interval between the two points with a BER of 2.5×10^{-5}.

95.8.8.4 Stressed receiver conformance test signal verification

The stressed receiver conformance test signal can be verified using an optical reference receiver with an ideal fourth-order Bessel-Thomson response with a reference frequency f_r of 19.34 GHz. Use of G.691 tolerance filters may significantly degrade this calibration. The clock output from the clock source in Figure 95–5 is modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye J2 Jitter and stressed eye J4 Jitter that includes the sinusoidal jitter component, a clock recovery unit (CRU of Figure 95–5) is required.

Care should be taken when characterizing the test signal because excessive noise/jitter in the measurement system would result in an input signal that does not fully stress the receiver under test. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. Care should be taken to minimize the noise/jitter introduced by the reference O/E, filters, and BERT and/or to correct for this noise. While the details of a BER scan measurement and test equipment are beyond the scope of this standard, it is recommended that the implementer fully characterize the test equipment and apply appropriate guard bands to ensure that the stressed receiver conformance input signal meets the stress and sinusoidal jitter specified in 95.8.8.2 and 95.8.8.5.

95.8.8.5 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table 95–11.

Table 95–11—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter peak-to-peak (UI)
$f < 100$ kHz	Not specified
100 kHz $< f \leq$ 10 MHz	5×10^5 Hz / f
10 MHz $< f \leq 10\ LB$[a]	0.05

[a] LB = loop bandwidth; upper frequency bound for added sinusoidal jitter should be at least 10 times the loop bandwidth of the receiver being tested.

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95.9 Safety, installation, environment, and labeling

95.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

95.9.2 Laser safety

100GBASE-SR4 optical transceivers shall conform to Hazard Level 1M laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[164]

95.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

95.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 100GBASE-SR4 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate, in the literature associated with the PHY, the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

95.9.5 Electromagnetic emission

A system integrating a 100GBASE-SR4 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

95.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

[164]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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95.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 100GBASE-SR4).

Labeling requirements for Hazard Level 1M lasers are given in the laser safety standards referenced in 95.9.2.

95.10 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 95–6.

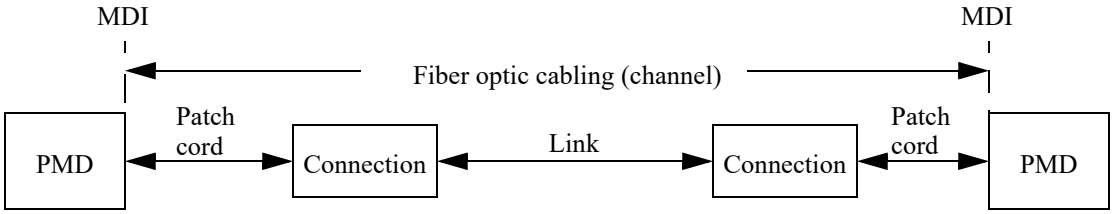

Figure 95–6—Fiber optic cabling model

The channel insertion loss is given in Table 95–12. A channel may contain additional connectors as long as the optical characteristics of the channel (such as attenuation, modal dispersion, reflections and losses of all connectors and splices) meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1 one-cord method. As OM4 optical fiber meets the requirements for OM3, a channel compliant to the "OM3" column may use OM4 optical fiber, or a combination of OM3 and OM4. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term *channel* is used here for consistency with generic cabling standards.

Table 95–12—Fiber optic cabling (channel) characteristics for 100GBASE-SR4

Description	OM3	OM4	Unit
Operating distance (max)	70	100	m
Cabling Skew (max)	79		ns
Cabling Skew Variation[a] (max)	2.4		ns
Channel insertion loss[b] (max)	1.8	1.9	dB
Channel insertion loss (min)	0		dB

[a]An additional 400 ps of Skew Variation could be caused by wavelength changes, which are attributable to the transmitter not the channel.
[b]These channel insertion loss values include cable loss plus 1.5 dB allocated for connection and splice loss, over the wavelength range 840 nm to 860 nm.

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95.11 Characteristics of the fiber optic cabling (channel)

The 100GBASE-SR4 fiber optic cabling shall meet the specifications defined in Table 95–12. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

95.11.1 Optical fiber cable

The fiber contained within the 100GBASE-SR4 fiber optic cabling shall comply with the specifications and parameters of Table 95–13. A variety of multimode cable types may satisfy these requirements, provided the resulting channel also meets the specifications of Table 95–12.

Table 95–13—Optical fiber and cable characteristics

Description	OM3[a]	OM4[b]	Unit
Nominal core diameter	50		μm
Nominal fiber specification wavelength	850		nm
Effective modal bandwidth (min)[c]	2000	4700	MHz.km
Cabled optical fiber attenuation (max)	3.5		dB/km
Zero dispersion wavelength (λ_0)	$1295 \le \lambda_0 \le 1340$		nm
Chromatic dispersion slope (max) (S_0)	0.105 for $1295 \le \lambda_0 \le 1310$ and $0.000375 \times (1590 - \lambda_0)$ for $1310 \le \lambda_0 \le 1340$		ps/nm^2 km

[a]IEC 60793-2-10 type A1a.2
[b]IEC 60793-2-10 type A1a.3
[c]When measured with the launch conditions specified in Table 95–6

95.11.2 Optical fiber connection

An optical fiber connection, as shown in Figure 95–6, consists of a mated pair of optical connectors.

95.11.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an average insertion loss per connection of 0.5 dB. Connections with lower loss characteristics may be used provided the requirements of Table 95–12 are met. However, the loss of a single connection shall not exceed 0.75 dB.

95.11.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –20 dB.

95.11.3 Medium Dependent Interface (MDI)

The 100GBASE-SR4 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the “fiber optic cabling” (as shown in Figure 95–6). The 100GBASE-SR4 PMD is

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coupled to the fiber optic cabling through one connector plug into the MDI optical receptacle as shown in Figure 95–7. Example constructions of the MDI include the following:

a) PMD with a connectorized fiber pigtail plugged into an adapter;
b) PMD receptacle.

95.11.3.1 Optical lane assignments

The four transmit and four receive optical lanes of 100GBASE-SR4 shall occupy the positions depicted in Figure 95–7 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains eight active lanes within twelve total positions. The transmit optical lanes occupy the left-most four positions. The receive optical lanes occupy the right-most four positions. The four center positions are unused.

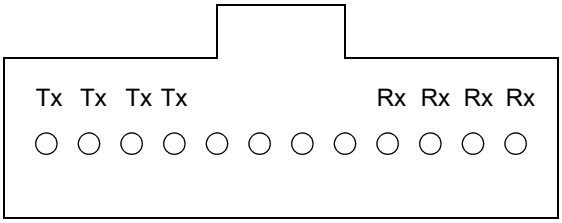

Figure 95–7—100GBASE-SR4 optical lane assignments

95.11.3.2 Medium Dependent Interface (MDI) requirements

The MDI adapter or receptacle shall meet the dimensional specifications for interface 7-1-3: *MPO adapter interface – opposed keyway configuration*, or interface 7-1-10: *MPO active device receptacle, flat interface*, as defined in IEC 61754-7-1. The plug terminating the optical fiber cabling shall meet the dimensional specifications of interface 7-1-4: *MPO female plug connector, flat interface for 2 to 12 fibres*, as defined in IEC 61754-7-1. The MDI shall optically mate with the plug on the optical fiber cabling. Figure 95–8 shows an MPO female plug connector with flat interface, and an MDI.

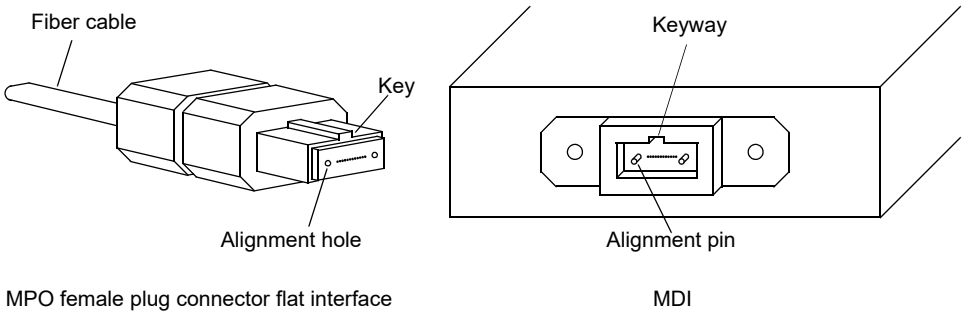

Figure 95–8—MPO female plug with flat interface and MDI

The MDI shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 95.5.1, not at the MDI.

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95.12 Protocol implementation conformance statement (PICS) proforma for Clause 95, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-SR4[165]

95.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 95, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-SR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

95.12.2 Identification

95.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

95.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 95, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-SR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[165]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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95.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
SR4	100GBASE-SR4 PMD	95.7	Device supports requirements for 100GBASE-SR4 PHY	O	Yes [ ] No [ ]
*INS	Installation / cable	95.11	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
CTP1	Reference point TP1 exposed and available for testing	95.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
CTP4	Reference point TP4 exposed and available for testing	95.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
CDC	Delay constraints	95.3.1	Device conforms to delay constraints	M	Yes [ ]
CSC	Skew constraints	95.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	95.4	Registers and interface supported	O	Yes [ ] No [ ]

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95.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-SR4

95.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CF1	Compatible with 100GBASE-R RS-FEC, PCS, and PMA	95.1		M	Yes [ ]
CF2	Integration with management functions	95.1		O	Yes [ ] No [ ]
CF3	Bit error ratio	95.1.1	Meets the BER specified in 95.1.1	M	Yes [ ]
CF4	Transmit function	95.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
CF5	Mapping between optical signal and logical signal for transmitter	95.5.2	Higher optical power is a one	M	Yes [ ]
CF6	Receive function	95.5.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
CF7	Conversion of four optical signals to four electrical signals	95.5.3	For delivery to the PMD service interface	M	Yes [ ]
CF8	Mapping between optical signal and logical signal for receiver	95.5.3	Higher optical power is a one	M	Yes [ ]
CF9	Global Signal Detect function	95.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
CF10	Global Signal Detect behavior	95.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all four lanes	M	Yes [ ]
CF11	Lane-by-lane Signal Detect function	95.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 95–4	MD:O	Yes [ ] No [ ] N/A [ ]
CF12	PMD reset function	95.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

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95.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
CM1	Management register set	95.4		MD:M	Yes [ ] N/A [ ]
CM2	Global transmit disable function	95.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
CM3	PMD_lane_by_lane_transmit_ disable function	95.5.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_*i* variable	MD:O	Yes [ ] No [ ] N/A [ ]
CM4	PMD lane-by-lane transmit disable	95.5.8	Disables each optical transmitter independently if CM3 = No	!MD:O	Yes [ ] No [ ]
CM5	PMD_fault function	95.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
CM6	PMD_transmit_fault function	95.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
CM7	PMD_receive_fault function	95.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

95.12.4.3 PMD to MDI optical specifications for 100GBASE-SR4

Item	Feature	Subclause	Value/Comment	Status	Support
CSR1	Transmitter meets specifications in Table 95–6	95.7.1	Per definitions in 95.8	M	Yes [ ] N/A [ ]
CSR2	Receiver meets specifications in Table 95–7	95.7.2	Per definitions in 95.8	M	Yes [ ] N/A [ ]

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95.12.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Measurement cable	95.8	2 m to 5 m in length	M	Yes [ ]
COM2	Center wavelength and spectral width	95.8.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
COM3	Average optical power	95.8.3	Per IEC 61280-1-1	M	Yes [ ]
COM4	OMA measurements	95.8.4	Each lane	M	Yes [ ]
COM5	Transmitter and dispersion eye closure (TDEC)	95.8.5	Each lane	M	Yes [ ]
COM6	Extinction ratio	95.8.6	Per IEC 61280-2-2	M	Yes [ ]
COM7	Transmit eye	95.8.7	Each lane	M	Yes [ ]
COM8	Stressed receiver sensitivity	95.8.8	See 95.8.8	M	Yes [ ]

95.12.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CES1	General safety	95.9.1	Conforms to J.2	M	Yes [ ]
CES2	Laser safety—IEC Hazard Level 1M	95.9.2	Conforms to Hazard Level 1M laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
CES3	Electromagnetic interference	95.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

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95.12.4.6 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
COC1	Fiber optic cabling	95.11	Meets requirements specified in Table 95–12	INS:M	Yes [ ] N/A [ ]
COC2	Optical fiber characteristics	95.11.1	Per Table 95–13	INS:M	Yes [ ] N/A [ ]
COC3	Maximum discrete reflectance	95.11.2.2	Less than –20 dB	INS:M	Yes [ ] N/A [ ]
COC4	MDI layout	95.11.3.1	Optical lane assignments per Figure 95–7	M	Yes [ ]
COC5	MDI dimensions	95.11.3.2	Per IEC 61754-7-1 interface 7-1-3 or interface 7-1-10	M	Yes [ ]
COC6	Cabling connector dimensions	95.11.3.2	Per IEC 61754-7-1 interface 7-1-4	INS:M	Yes [ ] N/A [ ]
COC7	MDI mating	95.11.3.2	MDI optically mates with plug on the cabling	M	Yes [ ]
COC8	MDI requirements	95.11.3.2	Meets IEC 61753-1 and IEC 61753-022-2	INS:M	Yes [ ] N/A [ ]

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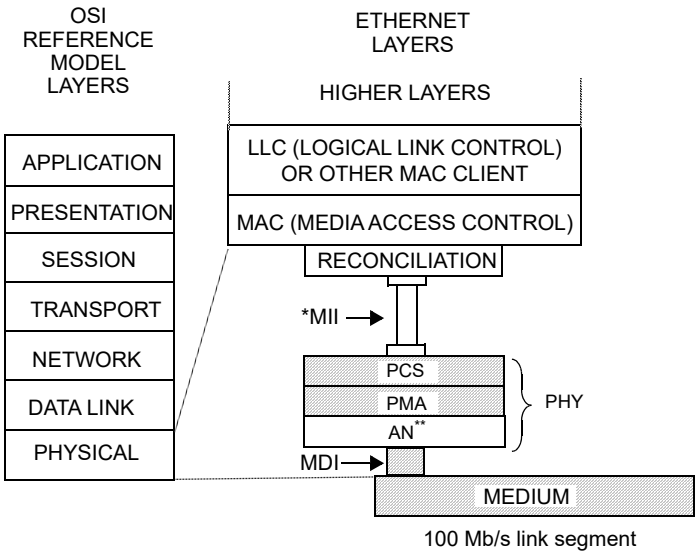
96. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T1

96.1 Overview

The 100BASE-T1 Physical Layer supports standard media access controller (MAC) interfaces via the MII defined in Clause 22 with the exception of the MII Management interface defined in 22.2.4. The 100BASE-T1 management functions are optionally accessible through the management interface defined in Clause 45. Each copper port supports a single balanced twisted-pair link segment connection up to 15 m in length. 100BASE-T1 provides data rate of 100 Mb/s at the MAC interface over a single balanced twisted-pair cable as defined in 96.7. The architectural positioning of the 100BASE-T1 Physical Layer is depicted in Figure 96–1.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* Physical instantiation of MII is optional.
** Auto-Negotiation is optional

Figure 96–1—Architectural positioning of 100BASE-T1

This clause defines the PCS and PMA sublayers of the 100BASE-T1 PHY. A functional block diagram of the 100BASE-T1 PHY is provided in Figure 96–3.

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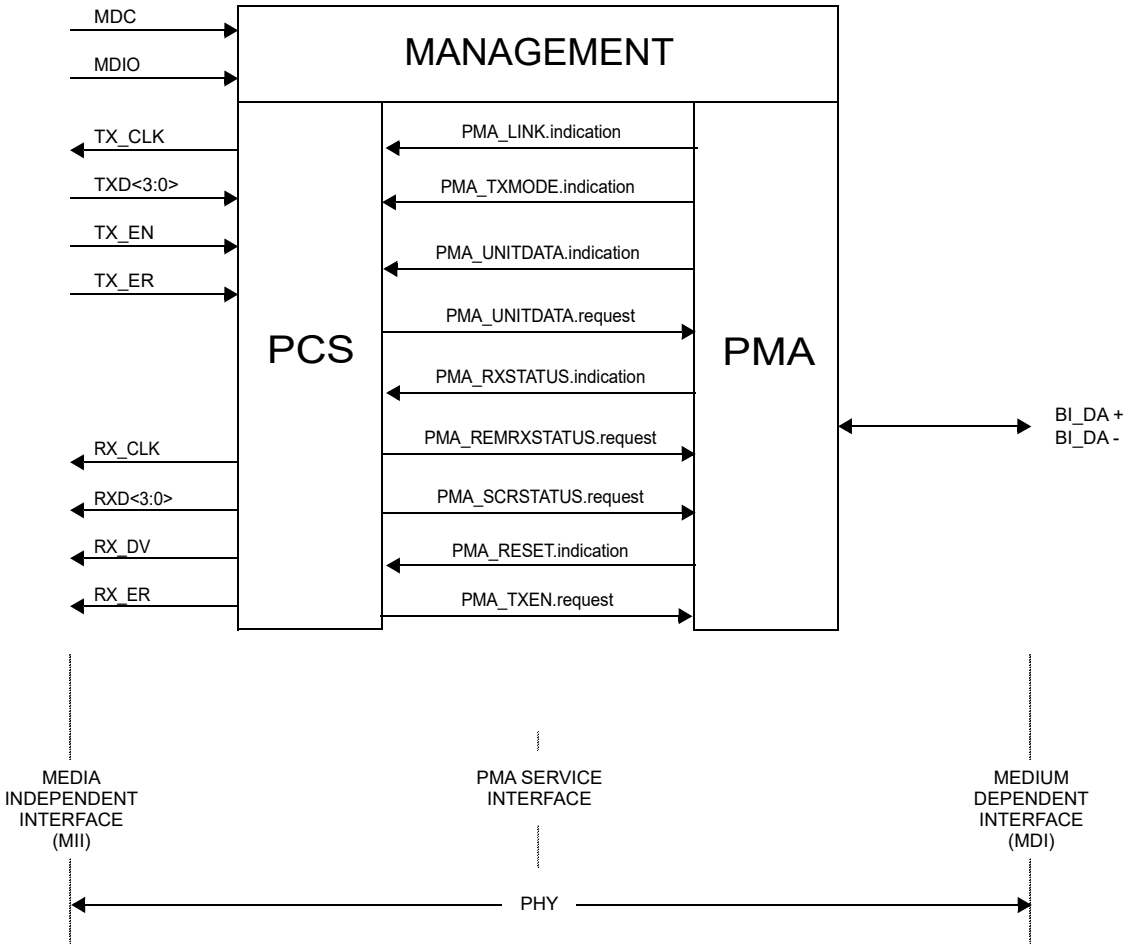

Figure 96–2—100BASE-T1 PHY interfaces

96.1.1 100BASE-T1 architecture

The 100BASE-T1 PHY operates using full-duplex communications (using echo cancellation) over a single balanced twisted-pair. This PHY uses ternary signaling and interfaces to the Clause 22 MII.

The 100BASE-T1 PHY interfaces to a Clause 22 MII. The PMA is similar to Clause 40. The PCS (specified in 96.3) is different from the PCS defined in Clause 40.

PMA functionality is defined in 96.4 with reference to Clause 40. The PMA functions are illustrated in Figure 96–3.

The 100BASE-T1 PHY leverages 1000BASE-T and 100BASE-TX PHY technologies in operation at 100 Mb/s, and introduces new PCS, PMA, and other modifications in support of the 100BASE-T1 PHY.

The specification features that enable operation over a single balanced twisted-pair are as follows:

a) Full-duplex communication with Ethernet MAC compatibility.

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b) Adopt Pulse Amplitude Modulation 3 (PAM3) to provide trade-off between bandwidth and EMI performance.

Auto-Negotiation (Clause 98) may optionally be used by 100BASE-T1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for normal operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding. The implementation of the Auto-Negotiation function is optional. If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.

96.1.1.1 Physical Coding Sublayer (PCS)

The 100BASE-T1 PCS transmits/receives signals to/from a Media Independent Interface (MII) as described in Clause 22, to/from signals on a 100BASE-T1 PMA, which supports a single balanced twisted-pair medium.

96.1.1.2 Physical Medium Attachment (PMA) sublayer

The 100BASE-T1 PMA transmits/receives signals to/from the PCS onto the single balanced twisted-pair cable medium and supports the link management and the 100BASE-T1 PHY Control function. The PMA provides full duplex communications at $66.66\overline{6}$ MBd over a single balanced twisted-pair cable up to 15 m in length.

96.1.1.3 Signaling

100BASE-T1 signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over the single balanced twisted-pair. The signaling scheme achieves a number of objectives including the following:

a) Algorithm mapping and inverse mapping from nibble data to ternary symbols and back.
b) Uncorrelated symbols in the transmitted symbol stream.
c) No correlation between symbol streams traveling both directions.
d) Ability to rapidly or immediately determine if a symbol stream represents data or idle.
e) Robust delimiters for Start-of-Stream delimiter (SSD), End-of-Stream delimiter (ESD), and other control signals.
f) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.

96.1.2 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and a descriptive text, the state diagram prevails.

96.1.2.1 State diagram notation

The notation used in the state diagrams follows the conventions of 21.5.

96.1.2.2 State diagram timer specifications

All timers operate in the manner described in 40.4.5.2.

96.1.2.3 Service specifications

The method and notation used in the service specification follows the conventions of 1.2.2.

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96.2 100BASE-T1 service primitives and interfaces

The 100BASE-T1 PHY shall use the service primitives and interfaces in 40.2, with exception of the following clarifications and differences noted in this section, in support of 100 Mb/s operations over a single balanced twisted-pair channel. Figure 96–2 shows the relationship of the service primitives and interfaces used by the 100BASE-T1 PHY.

Differences from the 40.2 service interface are as follows:

a) The 100BASE-T1 PHY uses the Media Independent Interface (MII) as specified in Clause 22.

b) The 100BASE-T1 PHY does not use 40.2 support of LPI (Low Power Idle) related functions.

c) The 100BASE-T1 PHY MASTER-SLAVE relationship is established by management (see 96.4.4).

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

96.2.1 PMA service interface

As shown in Figure 96–2, 100BASE-T1 uses the following service primitives to exchange symbol vectors, status indications, and control signals across the PMA service interface:

PMA_LINK.indications (link_status)
PMA_TXMODE.indication (tx_mode)
PMA_UNITDATA.request (tx_symb_vector)
PMA_UNITDATA.indication (rx_symb_vector)
PMA_SCRSTATUS.request (scr_status)
PMA_RXSTATUS.indication (loc_rcvr_status)
PMA_REMRXSTATUS.request (rem_rcvr_status)
PMA_TXEN.request (TX_EN)

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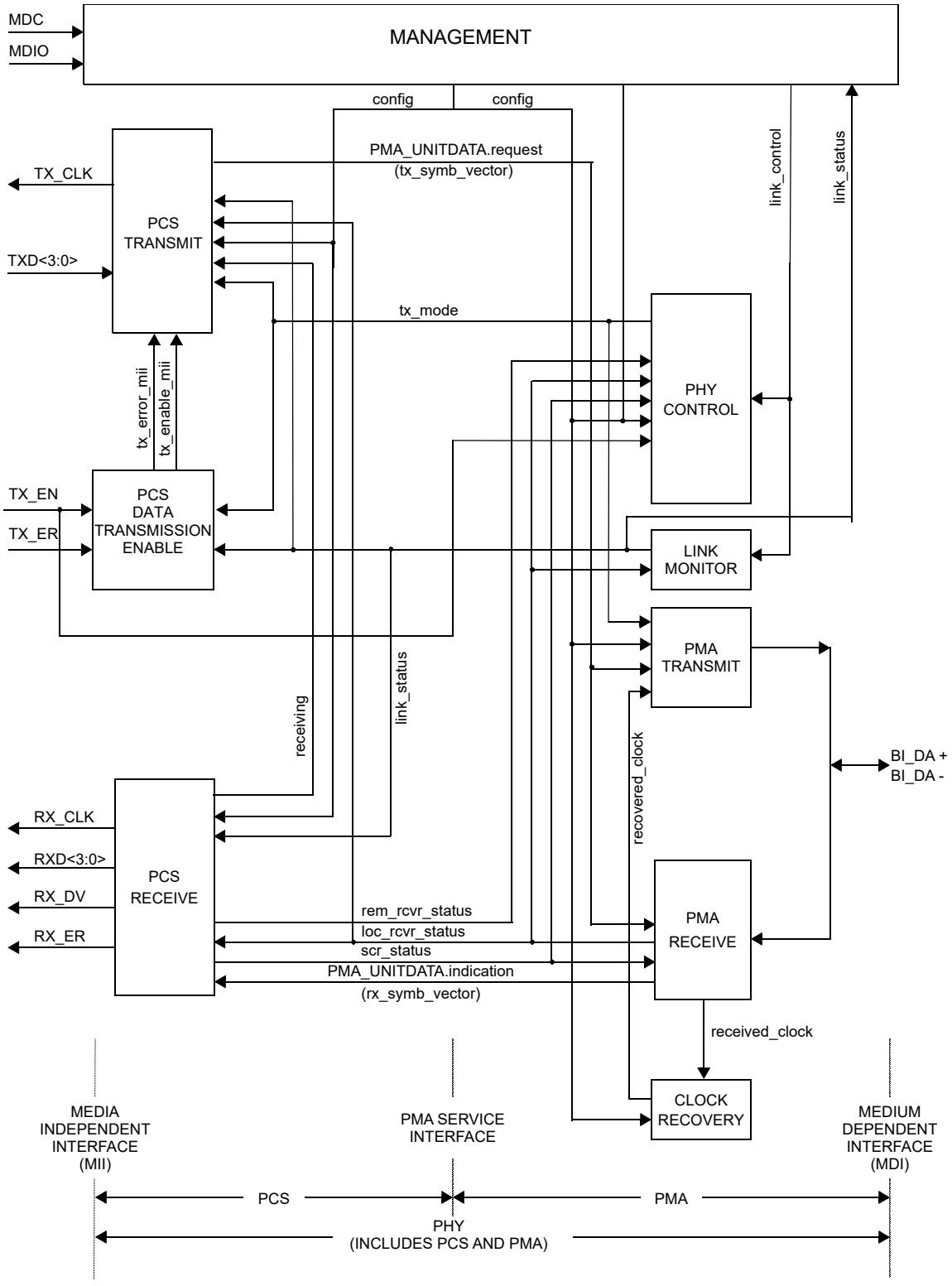

NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back to the PMA TRANSMIT for loop timing

Figure 96–3—Functional block diagram

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96.2.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 96.4.5. This primitive informs the PCS about the status of the underlying link.

96.2.2.1 Semantics of the primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on one of the following two values: FAIL or OK

FAIL	No valid link established
OK	The Link Monitor function indicates that a valid 100BASE-T1 link is established. Reliable reception of signals transmitted from the remote PHY is possible.

96.2.2.2 When generated

The PMA generates this primitive continuously to indicate the value of the link_status in compliance with the state diagram given in 96.4.5.

96.2.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 96.4.5.

96.2.3 PMA_TXMODE.indication

The 100BASE-T1 transmitter sends code-groups that represent an MII data stream, control information, idles, or zeros.

96.2.3.1 Semantics of the primitive

PMA_TXMODE.indication (tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of code-groups the PCS should be transmitting. The parameter tx_mode can take on one of the following three values:

SEND_N	This value is continuously asserted when transmission of sequences of code-groups representing a MII data stream (data mode), control mode or idle mode is to take place.
SEND_I	This value is continuously asserted in case transmission of sequences of code-groups representing the idle mode is to take place.
SEND_Z	This value is continuously asserted in case transmission of zeros is required.

96.2.3.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages continuously.

96.2.3.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Transmit function as described in 96.3.3.

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96.2.4 PMA_UNITDATA.request

This primitive defines the transfer of code-groups in the form of the tx_symb_vector parameter from the PCS to the PMA. The code-groups are obtained in the PCS Transmit function using the encoding rules defined in 96.3.3 to represent MII data streams, an idle mode, or other sequences.

96.2.4.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over the transmit pair BI_DA. The tx_symb_vector parameter takes on the following form:

SYMB_1D: A vector of one ternary symbol for a single transmit pair BI_DA. Each ternary symbol may take on one of the values {–1, 0, or +1}.

The ternary symbols that are elements of tx_symb_vector are called tx_symb_vector[BI_DA].

96.2.4.2 When generated

The PCS continuously generates PMA_UNITDATA.request (SYMB_1D) synchronously with every TX_TCLK cycle.

96.2.4.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated ternary symbols. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pair BI_DA.

96.2.5 PMA_UNITDATA.indication

This primitive defines the transfer of code-groups in the form of the rx_symb_vector parameter from the PMA to the PCS.

96.2.5.1 Semantics of the primitive

PMA_UNITDATA.indication (rx_symb_vector)

During reception, the PMA_UNITDATA.indication simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on the receive pair BI_DA. The rx_symb_vector parameter takes on the following form:

SYMB_1D A vector of ternary symbols for the receive pair BI_DA. Each ternary symbol may take on one of the values {–1, 0, or +1}.

The ternary symbols that are elements of rx_symb_vector are called rx_symb_vector[BI_DA].

96.2.5.2 When generated

The PMA generates PMA_UNITDATA.indication (SYMB_1D) messages synchronously with signals received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is $66.66\overline{6}$ MHz, as governed by the recovered clock.

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96.2.5.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

96.2.6 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the descrambler has achieved synchronization.

96.2.6.1 Semantics of the primitive

PMA_SCRSTATUS.request (scr_status)

The scr_status parameter can take on one of the following two values:

OK	The descrambler has achieved synchronization.
NOT_OK	The descrambler is not synchronized.

96.2.6.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages continuously.

96.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 96.4.3 and 96.4.4.

96.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementor. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol streams that represent the idle mode.

96.2.7.1 Semantics of the primitive

PMA_RXSTATUS.indication (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of the following two values:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

96.2.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages continuously on the basis of signals received at the MDI.

96.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 96–18, 96.4.4, and 96.4.5.

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96.2.8 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The criterion for setting the parameter rem_rcvr_status is left to the implementor. It can be based, for example, on asserting rem_rcvr_status is NOT_OK until loc_rcvr_status is OK and then asserting the detected value of rem_rcvr_status after proper PCS receive decoding is achieved.

96.2.8.1 Semantics of the primitive

PMA_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of the following two values:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

96.2.8.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages continuously on the basis of signals received at the MDI.

96.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 96–18.

96.2.9 PMA_RESET.indication

This primitive is used to pass the PMA Reset function to the PCS (pcs_reset=ON) when reset is enabled.

The PMA_RESET.indication primitive can take on one of the following two values:

TRUE	Reset is enabled.
FALSE	Reset is not enabled.

96.2.9.1 When generated

This primitive is generated under the conditions described in 40.4.2.1.

96.2.9.2 Effect of receipt

The effect of receipt of this primitive is specified in 40.4.2.1.

96.2.10 PMA_TXEN.request

This primitive indicates the presence of data on MII for transmission.

96.2.10.1 Semantic of the primitive

PMA_TXEN.request

The TX_EN parameter can take on one of the following two values:

TRUE	The data transmission on MII is enabled.
FALSE	The data transmission on MII is not enabled.

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96.2.10.2 When generated

PCS generates the PMA_TXEN.request messages continuously based on TX_EN signal received from MII.

96.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 96–18.

96.3 100BASE-T1 Physical Coding Sublayer (PCS) functions

The Physical Coding Sublayer (PCS) consists of PCS Reset, the PCS Data Transmission Enable, PCS Transmit, and PCS Receive functions as shown in Figure 96–4. The PCS Transmit function is explained in 96.3.3, and the PCS Receive function is explained in 96.3.4.

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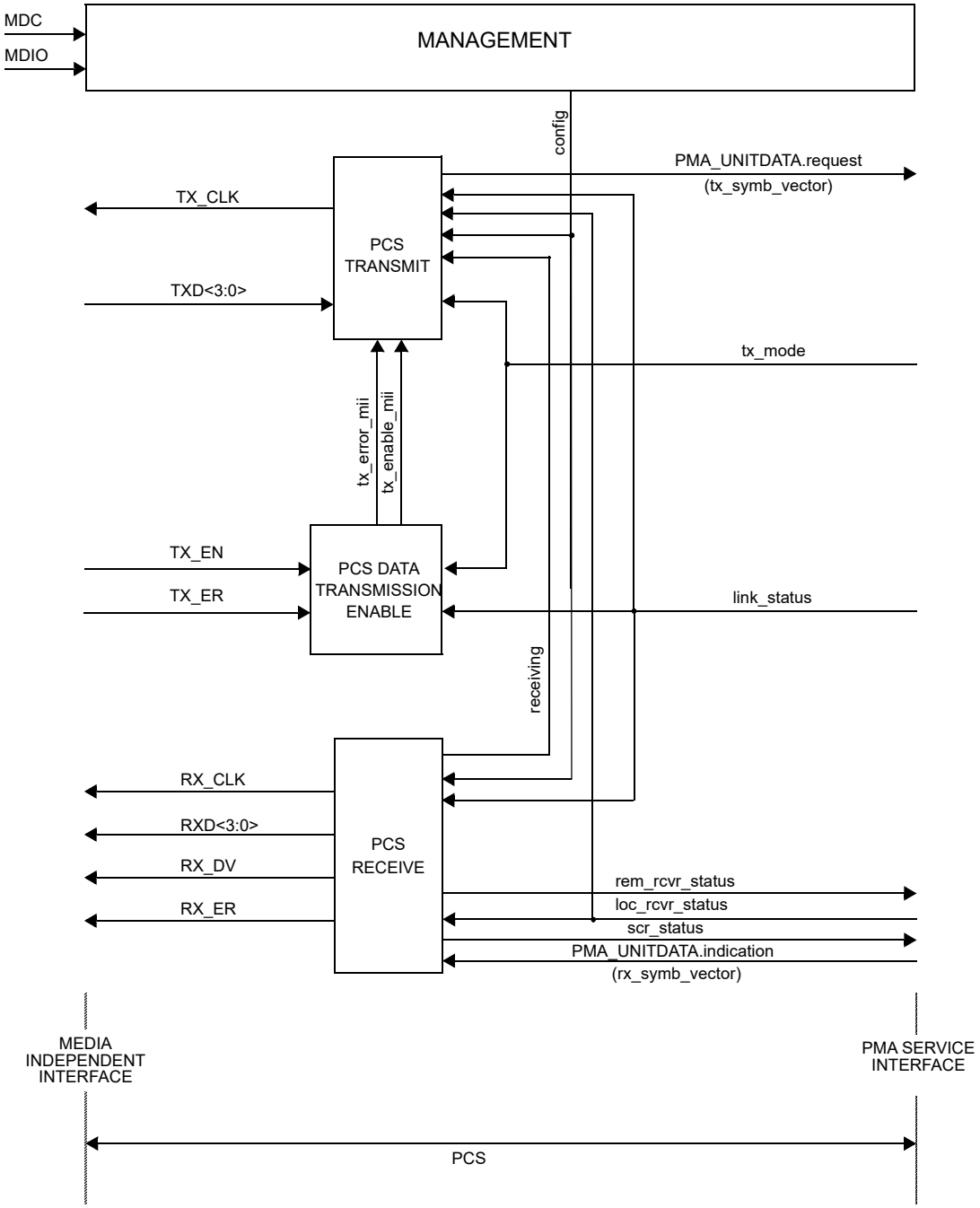

Figure 96–4—PCS reference diagram

96.3.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

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PCS Reset sets pcs_reset=ON while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

96.3.2 PCS data transmission enabling

The PCS data transmission enabling function shall conform to the PCS data transmission enabling state diagram in Figure 96–5. When tx_mode is equal to SEND_N, the signals tx_enable_mii and tx_error_mii are equal to the value of the MII signals TX_EN and TX_ER respectively, otherwise tx_enable_mii and tx_error_mii are set to the value FALSE.

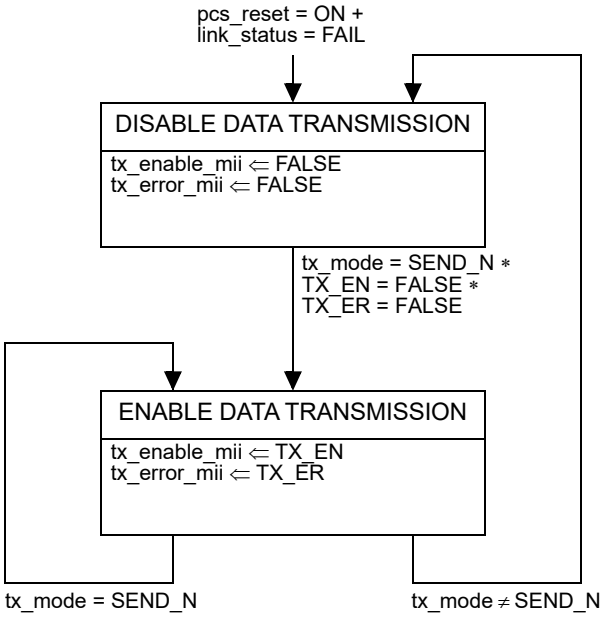

Figure 96–5—PCS data transmission enabling state diagram

96.3.2.1 Variables

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: ON or OFF

tx_enable_mii
: The tx_enable_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 96–5. When set to FALSE transmission is disabled, when set to TRUE transmission is enabled.
Values: TRUE or FALSE

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tx_error_mii
: The tx_error_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 96–5.When this variable is set to FALSE it indicates a non-errored transmission, when set to TRUE it indicates an errored transmission.
Values: TRUE or FALSE

TX_EN
: The TX_EN signal of the MII as specified in 22.2.2.3.

TX_ER
: The TX_ER signal of the MII as specified in 22.2.2.5.

tx_mode
: The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

96.3.3 PCS Transmit

96.3.3.1 4B/3B conversion

The PCS performs a 4B/3B conversion of the nibbles received at the MII, creates the ternary symbols, and then sends the symbols to the PMA for further processing. It receives 4 bits at the MII using TX_CLK, and converts the stream of 4-bit words at 25 MBd to a stream of 3-bit words at $33.33\overline{3}$ MBd. The bits are then scrambled and converted through PCS encoding to a stream of code-groups (pairs of ternary symbols). These ternary symbol pairs are then multiplexed to a serialized stream of ternary symbols at $66.66\overline{6}$ MBd

96.3.3.1.1 Control signals in 4B/3B conversion

Signals tx_enable_mii, tx_error_mii and TXD<3:0>, synchronized to MII TX_CLK are the input of 4B/3B conversion. After 4B/3B conversion, the transmit signals tx_data<2:0>, tx_enable and tx_error shall be synchronized with PCS transmit clock pcs_txclk. The frequencies of MII TX_CLK and pcs_txclk are 25 MHz and $33.33\overline{3}$ MHz respectively to keep the same bitwise throughput with 4B/3B conversion. TX_TCLK shall be derived from a local source in MASTER mode. TX_TCLK shall be derived from the recovered clock in SLAVE mode. The pcs_txclk is derived from the same clock source as TX_TCLK, with the proper clock division factor to get to the required frequency.

96.3.3.1.2 4B/3B conversion for MII data

The transmit data (TXD<3:0>) at the MII shall first be converted into 3 bits as a group (tx_data<2:0>). As shown in Figure 96–6b and Figure 96–6c, when the number of bits of a packet is not a multiple of three, the 4B/3B conversion shall append stuff bits to the end of a packet (1 or 2 bits), and correspondingly, the tx_enable signal remains TRUE until all the bits in a packet (appended with stuff bits if applicable) are rate converted. Note, a packet includes preamble, SFD, and a MAC Frame as specified in 1.4.447. Those stuff bits may be padded randomly, which is left to implementer, and will be discarded at the receiver upon the boundary of the last nibble at the MII RX domain. The minimum 12 byte IPG period between packets enables flushing the extra stuff bits to prevent FIFO overflow.

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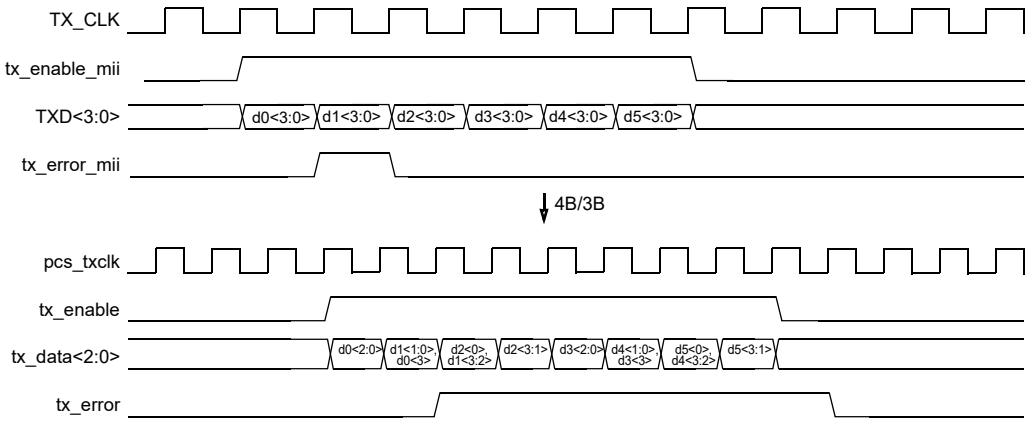

Figure 96–6a—4B/3B MII signal conversion (3*n*-bit data, no stuff bit appended)

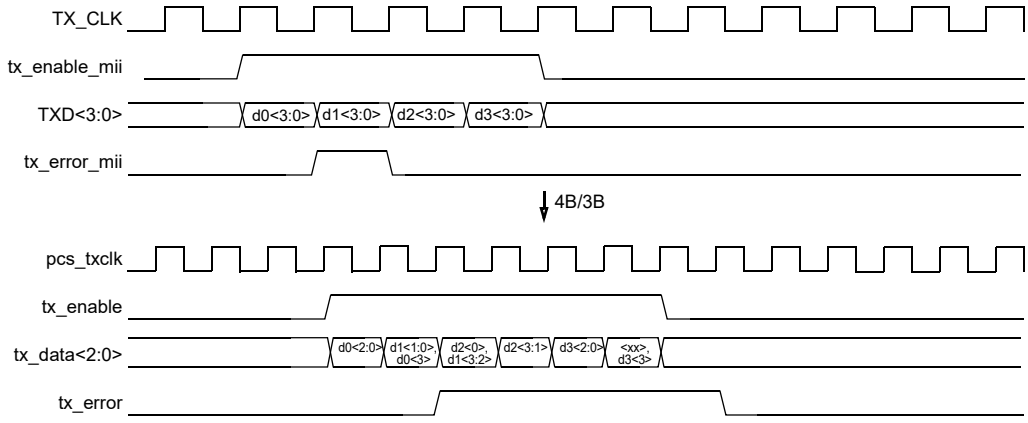

Figure 96–6b—4B/3B MII signal conversion ((3*n*+1)-bit data, 2 stuff bits appended)

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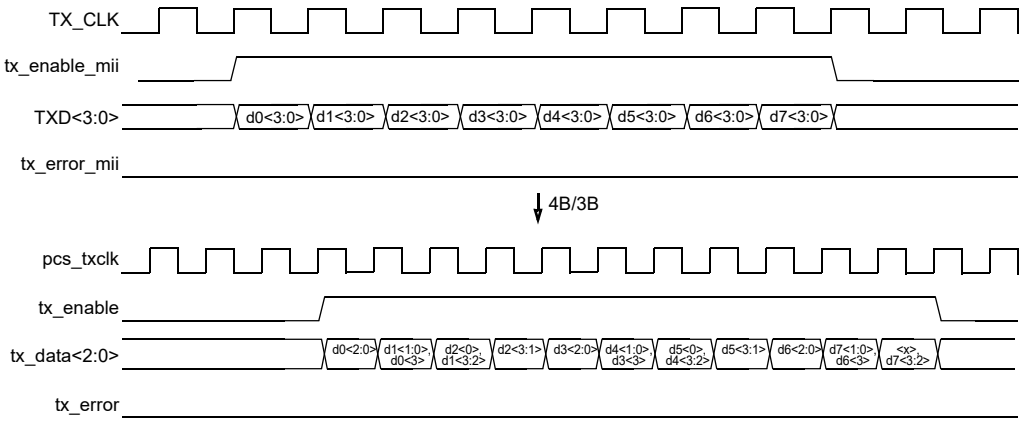

Figure 96–6c—4B/3B MII signal conversion ((3*n*+2)-bit data, 1 stuff bit appended)

96.3.3.2 PCS Transmit state diagram

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 96–7, and the associated state variables, functions, timers and messages.

In each symbol period, PCS Transmit generates a sequence of symbols A_n to the PMA, operating in one of three different modes (tx_mode), where symbol A_n is a ternary code that can take values of {–1, 0, or +1}. The PMA transmits symbol A_n over the wire pair BI_DA. The integer, n, is a time index, introduced to establish a temporal relationship between different symbol periods. A symbol period, T, is nominally equal to 15 ns. In the normal mode of operation, the PCS Transmit generates sequences of vectors using the encoding rules defined for SEND_N in 96.3.3.3.7 and 96.3.3.3.8, according to the value of tx_enable. Upon the assertion of tx_enable, the PCS Transmit function passes an SSD of 6 consecutive symbols to the PMA, which replaces the first 9 bits of preamble. Following SSD, tx_data<2:0> is encoded into ternary symbols as specified in 96.3.3.3, until tx_enable is de-asserted. Following the de-assertion of tx_enable, a special code ESD (or ERR_ESD when transmit error is encountered) of 6 consecutive symbols is generated, after which the transmission of idle mode is resumed. As shown in Figure 96–6a and Figure 96–6b, if tx_error_mii is ever asserted (due to MII TX_ER assertion) during the data frame period, tx_error is set as TRUE and stays TRUE till the end of frame to record such an occurrence. 100BASE-T1 only has one special symbol pair (0, 0) that is not used by Idle or Data symbols. Therefore, at the end of a frame, tx_error is examined to determine whether ESD3 or ERR_ESD3 are to be transmitted following ESD1 and ESD2, as shown in Figure 96–7.

The 100BASE-T1 PHY supports normal operation and link training operation. In training operation, the PCS ignores signals from MII and sends only the idle signals to the PMA until training process is complete (signaled by the link partner). The training process usually includes descrambler lock, timing acquisition, echo cancellation and equalizer convergence, etc.

If tx_mode has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA.

If tx_mode has the value SEND_I, PCS Transmit generates sequences of symbols according to the encoding rule in training mode as described in 96.3.3.3.6.

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If tx_mode has the value SEND_N, PCS Transmit generates symbols A_n at each symbol period representing data, special control symbols like SSD/ESD or IDLE symbols as defined in 96.3.3.3.5. The transition from idle to data is signaled by an SSD, and the end of transmission of data is signaled by an ESD.

During training operation (when tx_mode is SEND_I), knowledge of the transmitted symbols may be used at receiver side to perform any signal conditioning neccesary for meeting the required performance during normal operation. When the link is up, the PHY enters SEND_N mode and the transmitted PAM3 symbols are used at receiver PHY for continued clock frequency/phase tracking.

96.3.3.2.1 Variables

DATA
: A vector of two ternary symbols corresponding to the code-group indicating valid data, as specified in 96.3.

ERR_ESD3
: A vector of two ternary symbols in the third code-group of ESD in case of tx_error (–1, –1) as specified in 96.3.3.3.5.

ESD1
: A vector of two ternary symbols in the first code-group of ESD (0, 0) as specified in 96.3.3.3.5.

ESD2
: A vector of two ternary symbols in the second code-group of ESD (0, 0) as specified in 96.3.3.3.5.

ESD3
: A vector of two ternary symbols in the third code-group of ESD (1, 1) as specified in 96.3.3.3.5.

IDLE
: A sequence of vectors of ternary symbols representing the special code-group generated in Idle mode, as specified in 96.3.3.3.6 and 96.3.3.3.8.

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

loc_rcvr_status
: The loc_rcvr_status parameter set by the PMA Receive function and passed to the PCS via the PMA_RXSTATUS.indication primitive.
Values: OK or NOT_OK

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: ON or OFF

SSD1
: A vector of two ternary symbols in the first code-group of SSD (0, 0) as specified in 96.3.3.3.5.

SSD2
: A vector of two ternary symbols in the second code-group of SSD (0, 0) as specified in 96.3.3.3.5.

SSD3
: A vector of two ternary symbols in the third code-group of SSD (0, 0) as specified in 96.3.3.3.5.

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TXD<3:0>
The TXD<3:0> signal of the MII as specified in 22.2.2.4.

tx_enable
The tx_enable parameter generated by PCS Transmit as specified in Figure 96–7.
Values: TRUE or FALSE

tx_data<2:0>
Generated by PCS Transmit, transmit data is synchronous to pcs_txclk (33.33$\overline{3}$ MHz clock).

tx_error
The tx_error parameter generated by PCS Transmit as specified in Figure 96–7.
Values: TRUE or FALSE

TX_EN
The TX_EN signal of the MII as specified in 22.2.2.3.

TX_ER
The TX_ER signal of the MII as specified in 22.2.2.5.

tx_mode
The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

Tx_n
Alias for tx_symb_vector at time *n*.

tx_symb_pair
A pair of ternary symbols generated by the PCS Transmit function after ternary pair encoding.
Value: A pair of ternary transmit symbols. Each of the ternary symbols may take on one of the values {–1, 0, or +1}

96.3.3.2.2 Functions

ENCODE	In the PCS Transmit process, this function takes as its argument tx_data<2:0> and returns the corresponding tx_symb_pair. ENCODE follows the rules defined in 96.3.3.3.

96.3.3.2.3 Timers

symb_timer	The symb_timer shall be generated synchronously with TX_TCLK. In the PCS Transmit state diagram, the message PMA_UNITDATA.request is issued concurrently with symb_timer_done.	
	Continuous timer:	The condition symb_timer_done becomes true upon timer expiration.
	Restart time:	Immediately after expiration; timer restart resets the condition symb_timer_done.
	Duration:	15 ns nominal. (See clock tolerance in 96.5.4.5.)
symb_pair_timer	The symb_pair_timer shall be generated synchronously with PCS transmit clock pcs_txclk.	
	Continuous timer:	The condition symb_pair_timer_done becomes true upon timer expiration.

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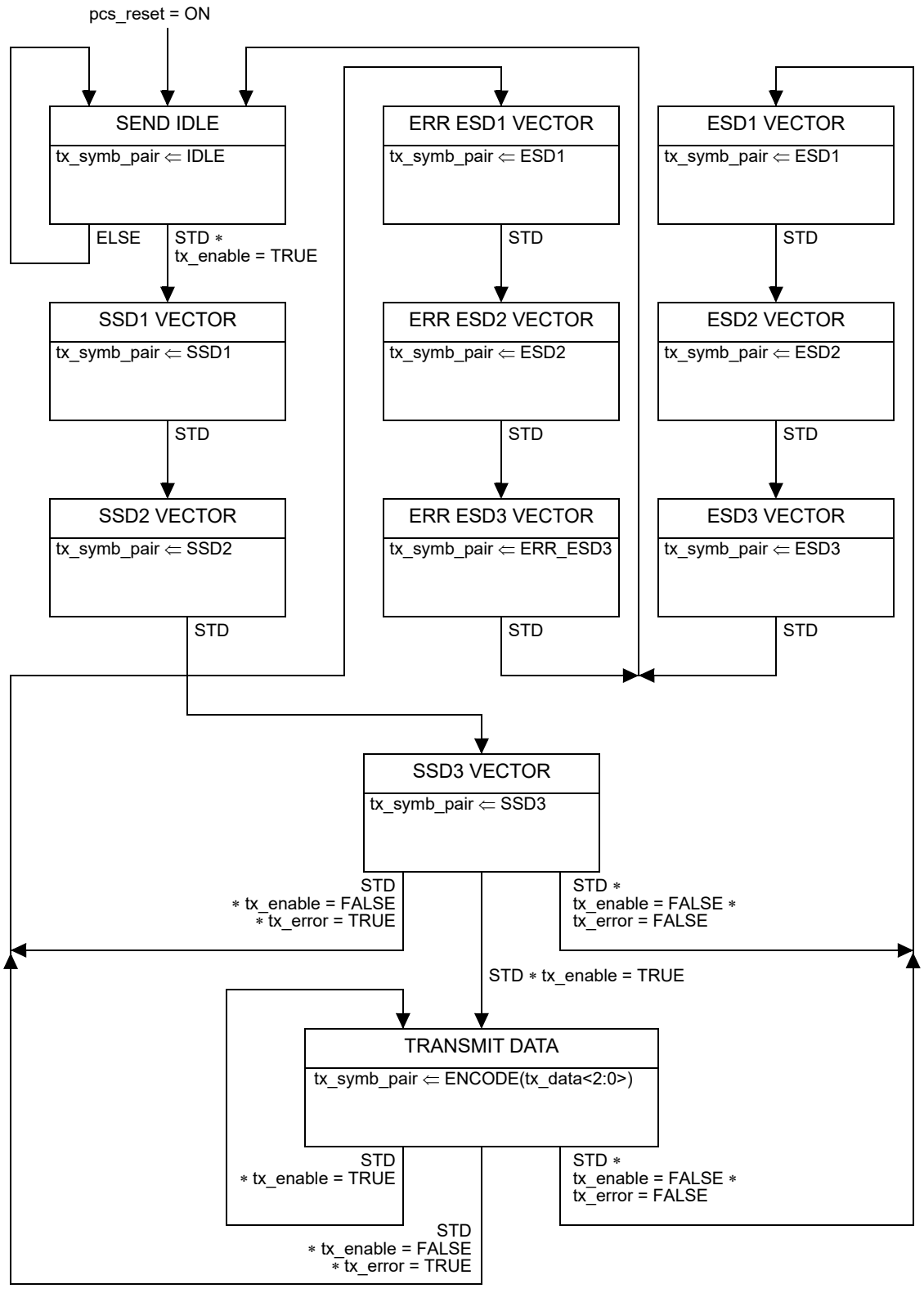

Figure 96–7—PCS Transmit state diagram

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Restart time:	Immediately after expiration; timer restart resets the condition symb_pair_timer_done.
Duration:	30 ns nominal.

96.3.3.2.4 Messages

STD	Alias for symb_pair_timer_done.

96.3.3.3 PCS transmit symbol generation

The reference diagram of PCS transmit symbol generation is indicated in Figure 96–8. The tx_symb_pair is the ternary pair (TA_n, TB_n).

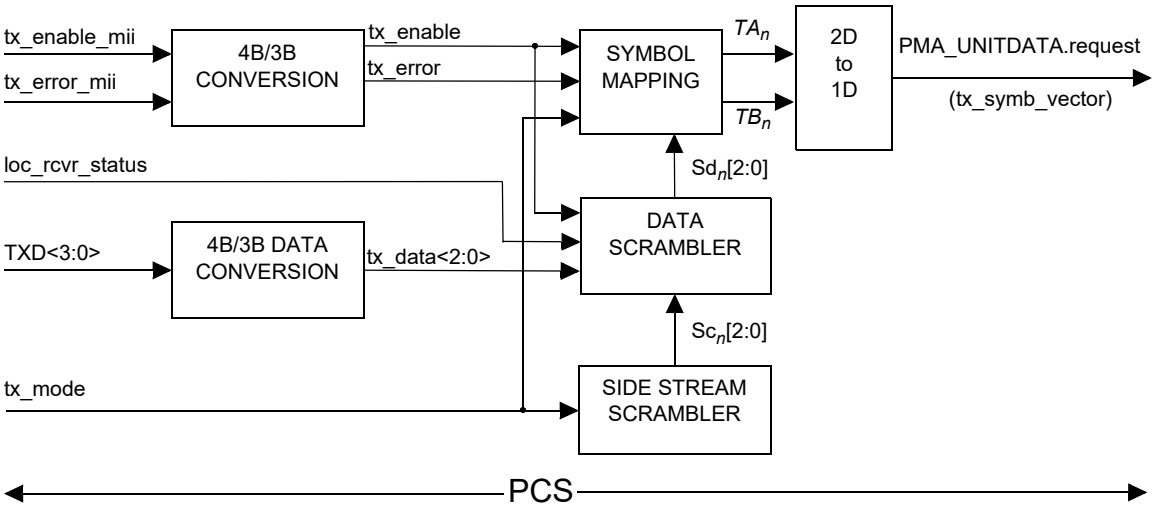

Figure 96–8—PCS transmit symbol generation

96.3.3.3.1 Side-stream scrambler polynomial

The scrambler function shall conform to 40.3.1.3.1 and associated Figure 40–6 without any exceptions.

96.3.3.3.2 Generation of Sy_n[2:0]

Generation of Sy_n[2:0] and Sc_n[2:0] shall conform to and be generated in accordance with the encoding rules in 40.3.1.3.2 and 40.3.1.3.3. Sy_n[2:0] vector in this specification is three bits, while the 40.3.1.3.2 vector is four bits.The PCS Transmit encoding of Sy_n[2:0] and then Sc_n[2:0] are performed, at time n, and used to eliminate the correlation of transmit data tx_data<2:0> and to generate idle and training symbols. Sy_n[3] is not used by definition.

96.3.3.3.3 Generation of Sc_n[2:0]

Bits Sc_n[2:0] shall be generated as follows:

$$Sc_n[2:0] = \begin{cases} [0\ 0\ 0] & \text{if (tx\_mode = SEND\_Z)} \\ Sy_n[2:0] & \text{else} \end{cases}$$

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96.3.3.3.4 Generation of scrambled bits $Sd_n[2:0]$

The $tx\_data_n<2:0>$ is a three bit vector after 4B/3B conversion.

From scrambler bits $Sc_n[2:0]$ and $tx\_data_n<2:0>$, bits $Sd_n[2:0]$ shall be generated as follows:

$$Sd_n[2] = \begin{cases} Sc_n[2] \wedge tx\_data_n<2> & \text{if } (tx\_enable_{n-3} = 1) \\ Sc_n[2] \wedge 1 & \text{else if } (loc\_rcvr\_status = OK) \\ Sc_n[2] & \text{else} \end{cases}$$

$$Sd_n[1:0] = \begin{cases} Sc_n[1:0] \wedge tx\_data_n<1:0> & \text{if } (tx\_enable_{n-3} = 1) \\ Sc_n[1:0] & \text{else} \end{cases}$$

where ^ denotes the XOR logic operator.

96.3.3.3.5 Generation of ternary pair (TA_n, TB_n)

The bits $Sd_n[2:0]$ are used to generate ternary pair (TA_n, TB_n). The ternary symbol pair (0, 0) is used in the special codes of SSD, ESD, and ESD with tx_error. Sequences of (0, 0), (0, 0), (0, 0) represent SSD, (0, 0), (0, 0), (1, 1) represent ESD and (0, 0), (0, 0), (–1, –1) represent ESD with tx_error.

96.3.3.3.6 Generation of (TA_n, TB_n) when tx_mode = SEND_I

Among the nine possible values for the ternary pair (TA_n, TB_n) only six values are used in the training sequence as indicated in Table 96–1. The ternary pairs used to encode SSD and ESD are not used during training.

Table 96–1—Idle symbol mapping in training

$Sd_n[2:0]$	TA_n	TB_n
000	–1	0
001	0	1
010	–1	1
011	0	1
100	1	0
101	0	–1
110	1	–1
111	0	–1

96.3.3.3.7 Generation of (TA_n, TB_n) when tx_mode = SEND_N, tx_enable = 1

The mapping from $Sd_n[2:0]$ to ternary pairs in data mode is indicated in Table 96–2.

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Table 96–2—Data symbols when tx_mode=SEND_N

$Sd_n[2:0]$	TA_n	TB_n
000	–1	–1
001	–1	0
010	–1	1
011	0	–1
Used for SSD/ESD	0	0
100	0	1
101	1	–1
110	1	0
111	1	1

96.3.3.3.8 Generation of (TA_n, TB_n) for idle sequence when tx_mode=SEND_N

The extra scrambling bit Sx_n is introduced to balance the power density for ternary pair (TA_n, TB_n). Sx_n shall be generated as follows:

$$Sx_n = Scr_n[7] \wedge Scr_n[9] \wedge Scr_n[12] \wedge Scr_n[14]$$

where ^ denotes the XOR logic operator. The ternary pair (TA_n, TB_n) is generated according to Table 96–3.

Table 96–3—Idle symbols when tx_mode=SEND_N

	tx_mode = SEND_N			
	$Sx_n = 0$		$Sx_n = 1$	
$Sd_n[2:0]$	TA_n	TB_n	TA_n	TB_n
000	–1	0	–1	0
001	0	1	1	1
010	–1	1	–1	1
011	0	1	1	1
100	1	0	1	0
101	0	–1	–1	–1
110	1	–1	1	–1
111	0	–1	–1	–1

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96.3.3.3.9 Generation of (TA_n, TB_n) when tx_mode=SEND_Z

The ternary pair (TA_n, TB_n) simply shows as zero vector (0, 0) when tx_mode=SEND_Z.

96.3.3.3.10 Generation of symbol sequence

The generation of one-dimensional symbol sequence from ternary pair (TA_n, TB_n) is illustrated in Figure 96–9.

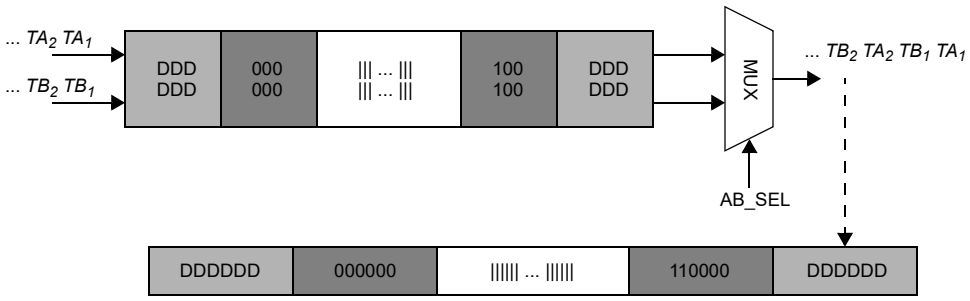

Figure 96–9—2-D symbol to 1-D symbol conversion

The symbol is sent to one sequence in the form of interleave in the order from right to left. AB_SEL signal defines the interleave selection for code-groups. The serial stream is created by interleaving either (TA_n, TB_n) with TA_n followed by TB_n or (TB_n, TA_n) with TB_n followed by TA_n. The ESD (after a packet) is followed by IDLE symbols, then SSD, and then by DATA. The symbol rate is twice as fast as pcs_txclk.

96.3.4 PCS Receive

96.3.4.1 PCS Receive overview

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 96–10a and Figure 96–10b, and associated state variables.

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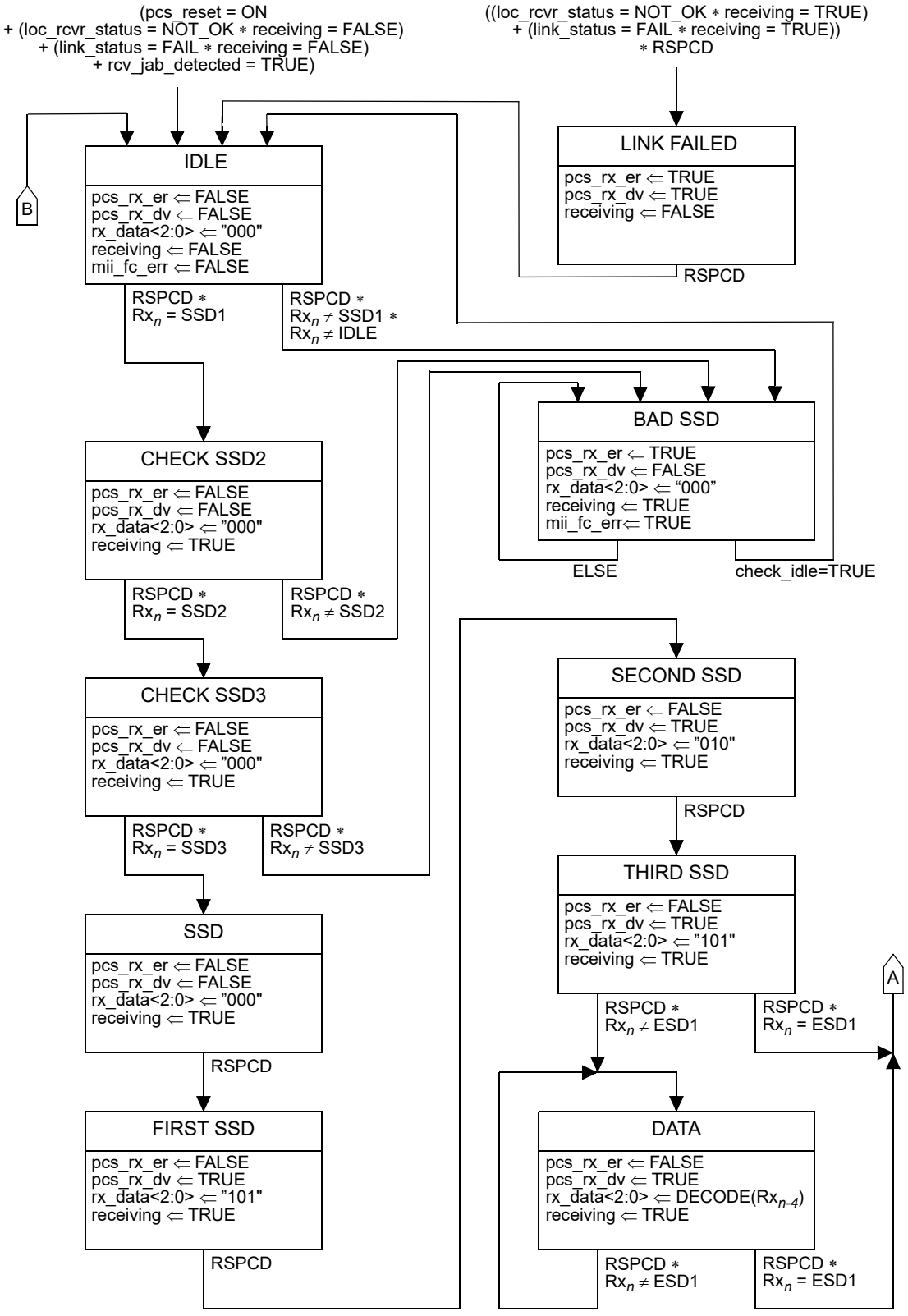

Figure 96–10a—PCS Receive state diagram

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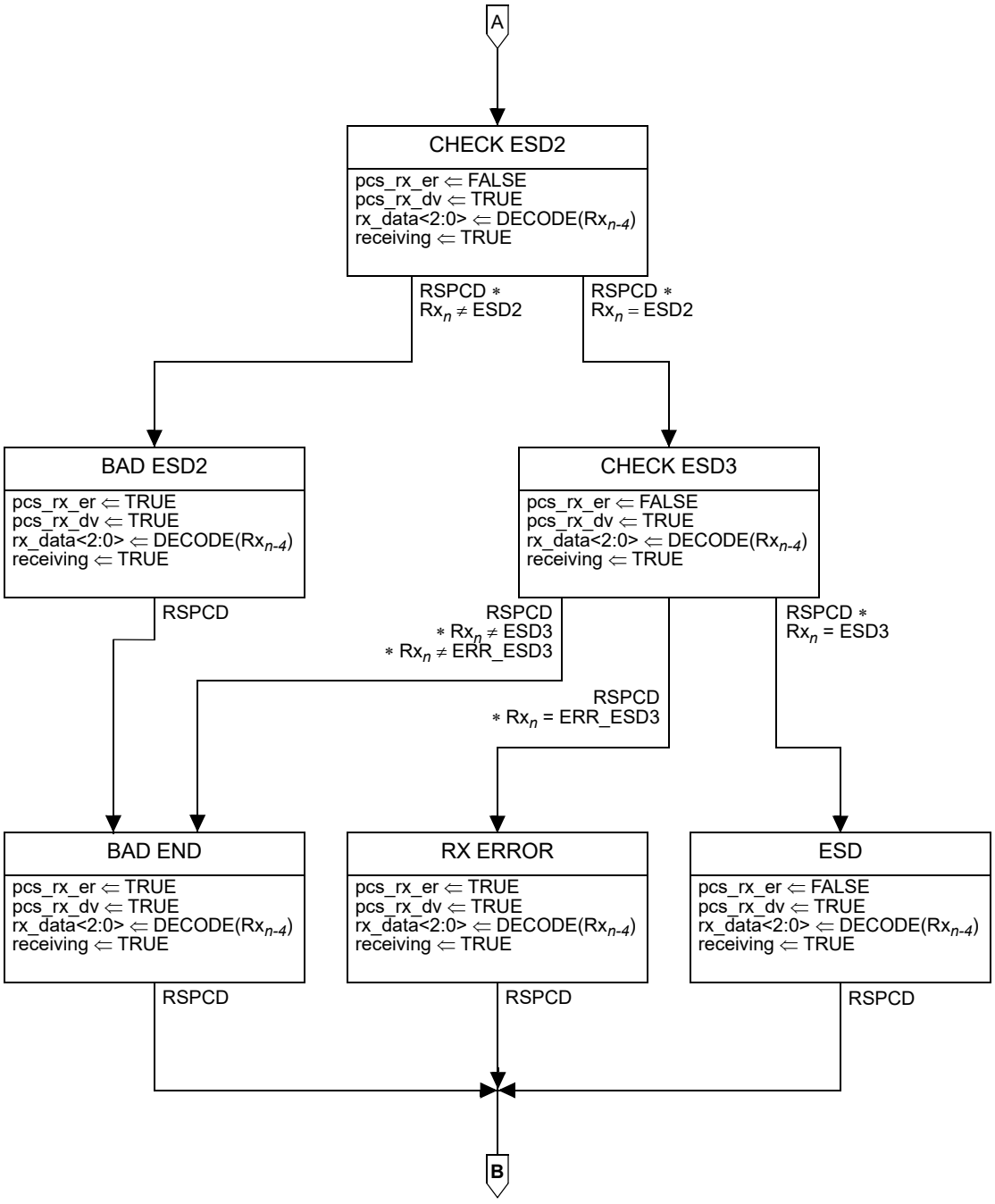

Figure 96–10b—PCS Receive state diagram (continued)

A JAB state machine as shown in Figure 96–11, is implemented to prevent any mis-detection of ESD1 and ESD2 that would make the PCS Receive state machine lock up in the DATA state. The maximum dwelling time in DATA state shall be less than the period specified for rcv_max_timer. When rcv_max_timer expires, the PCS Receive state machine is reset and transition to IDLE state is forced.

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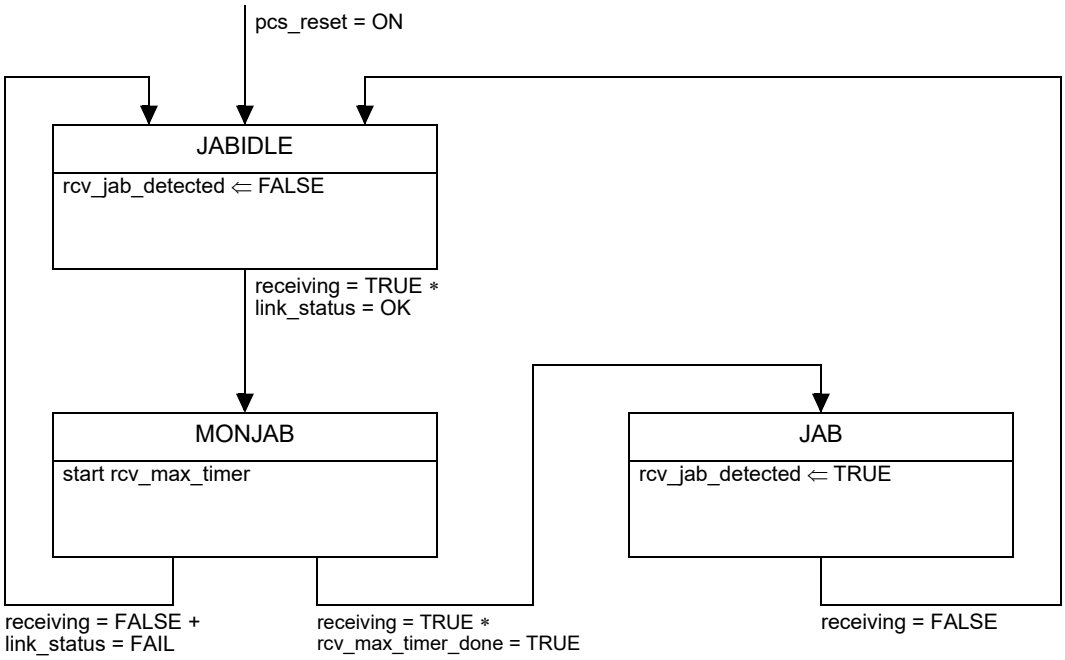

Figure 96–11—JAB state diagram

In Figure 96–10a, there are a total of four states after SSD3 detection before the DATA state; meanwhile, there are also four states before the IDLE state (including the DATA state) that perform DATA decoding. As a result, the depth of data flush-in delay line is the same as the flush-out delay line ensuring correct packet reception at the MII.

The variables, functions, and timers used in Figure 96–10a, Figure 96–10b, and Figure 96–11 are defined as below. For the definition of IDLE, SSD1, SSD2, SSD3, ESD1, ESD2, ESD3 and ERR_ESD3, see 96.3.3.2.1.

96.3.4.1.1 Variables

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

loc_rcvr_status
: The loc_rcvr_status parameter set by the PMA Receive function and passed to the PCS via the PMA_RXSTATUS.indication primitive.
Values: OK or NOT_OK

mii_fc_err
: Indicates that a false carrier error has occurred.
Values: TRUE or FALSE

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: ON or OFF

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pcs_rx_er
: PCS receive error indication signal synchronous to pcs_rxclk.
Values: TRUE or FALSE

pcs_rx_dv
: PCS receive data link indication signal synchronous to pcs_rxclk.
Values: TRUE or FALSE

receiving
: Generated by the PCS Receive function; if set as TRUE, it indicates that the PCS is in Data mode.
Values: TRUE or FALSE

rcv_jab_detected
: Variable set as TRUE when in JAB state as shown in JAB state diagram in Figure 96–11 else it is set FALSE.
Values: TRUE or FALSE

Rx_n
: Received symbol pair generated by PCS Receive at time *n*.

rx_data<2:0>
: PCS decoded data synchronous to pcs_rxclk.

rx_symb_pair
: A pair of ternary symbols generated by the PCS Receive function before ternary pair decoding.
Value: A pair of ternary receive symbols. Each of the ternary symbols may take on one of the values {–1, 0, or +1}.

rx_symb_vector
: A vector of ternary symbols received by the PMA and passed to the PCS via the PMA_UNITDATA.indication primitive.
Value: SYMB_1D

96.3.4.1.2 Functions

check_idle	A function used by the PCS Receive process to detect the reception of valid idle code-groups after an error condition during the process. The check_idle function operates on six consecutive code-groups after de-interleaving rx_symb_vectors. The check_idle function then returns a Boolean value indicating whether or not all six consecutive code-groups after de-interleaving rx_symb_vectors are valid in idle mode encoding, as specified in 96.3.3.3.5.
DECODE	In the PCS Receive process, this function takes as its argument the value of rx_symb_pair and returns the corresponding rx_data<2:0>. DECODE follows the rules outlined in 96.3.4.2.

96.3.4.1.3 Timer

RSPCD	Receive Symbol Pair Converted Done, synchronized with PCS receive clock pcs_rxclk of frequency 33.33$\overline{3}$ MHz.
rcv_max_timer	A timer used to determine the maximum amount of time the PHY Receive state machine stays in DATA state. The timer shall expire 1.08 ms ± 54 μs after being started. The condition rcv_max_timer_done becomes true upon timer expiration.

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96.3.4.2 PCS Receive symbol decoding

When PMA Receive indicates normal operation and sets loc_rcvr_status = OK, the PCS Receive function checks the symbol sequences and searches for SSD or receive error indicator. The receiver de-interleaves the sequences of rx_symb_vector to rx_symb_pair accordingly.

The received symbols, rx_symb_vector, are de-interleaved to generate rx_symb_pair (RA_n, RB_n). To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode. PCS Receive generates the sequence of symbols and indicates the reliable acquisition of the descrambler state by setting the parameter scr_status to OK. The received ternary pairs (RA_n, RB_n) are decoded to generate signals rx_data<2:0>, pcs_rx_dv, and pcs_rx_error. These signals are processed through 3B/4B conversion to generate signals RXD<3:0>, RX_DV and RX_ER at the MII.

PCS Receive sets pcs_rx_dv=TRUE when it receives SSD, and sets pcs_rx_dv=FALSE when it receives ESD or ESD with error. The number of bits received in a packet is always a multiple of 3 that shall go through the process of 3B/4B conversion, discarding the residual 1 bit or 2 bits of data.

PCS Receive shall set pcs_rx_er = TRUE when it receives bad ESDs, ERR_ESD, or bad SSDs. When the state machine reaches the IDLE state, pcs_rx_er gets reset to FALSE.

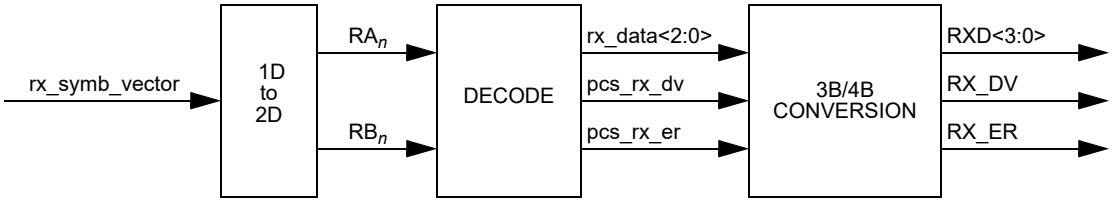

Figure 96–12—PCS Data receive symbol decoding

96.3.4.3 PCS Receive descrambler polynomial

This function shall conform to 40.3.1.4.2, with the exception that it applies to rx_data<2:0>.

96.3.4.4 PCS Receive automatic polarity detection (Optional)

During training, automatic polarity detection may be done in PCS Receive with proper decoding procedures. In the IDLE mode, $Sd_n[2:0]$ are generated by side-stream scrambler with $Sd_n[0]=Scr_n[0]$. According to Table 96–1, when $Sd_n[0]$ is 0, TA_n is either +1 or –1; otherwise, TA_n is 0. Based on this rule, $Scr_n[0]$ should be decoded solely depending on the value of RA_n, then fed back to the shift registers of side-stream descrambler to achieve reliable state acquisition. After that, in every symbol cycle, $Scr_n[0]$ should be compared with the processed RA_n value. Continuous consistency within a certain period means the scrambler has been successfully locked. Polarity can also be automatically detected with similar techniques in a recursive process: one assumption of polarity is made first and the descrambler synchronization is monitored within a certain period to determine whether such an assumption is correct; if not, the same procedure is repeated with a different polarity assumption.

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Polarity detection and correction can be done simultaneously at the earliest link up stages. Link up starts with the MASTER PHY sending symbols to the SLAVE PHY. During this initial stage, all hand-shaking signal status, such as rem_rcvr_status, are known as FALSE. With this a priori knowledge, polarity should be accurately detected by the SLAVE side. If a polarity flip is detected, the SLAVE changes the sign of its received signals (RA_n, RB_n) to correct the polarity. Furthermore, it shall invert its transmitted signals (TA_n, TB_n). Since polarity correction has been taken care of by the SLAVE PHY, the polarity would always be observed as correct by the MASTER PHY.

96.3.4.5 PCS Receive MII signal 3B/4B conversion

The MII receive signals RXD<3:0>, RX_DV and RX_ER are synchronized with clock RX_CLK ; while PCS Receive generated signals rx_data<2:0>, rx_dv, and rx_error shall be synchronized with pcs_rxclk to keep the same bitwise throughput after 3B/4B conversion. Generation of pcs_rxclk is implementation dependent. RX_CLK may be derived from the same clock source as TX_CLK if the PHY is in MASTER mode or from the recovered clock if the PHY is in SLAVE mode. The pcs_rxclk is derived from the same clock source as RX_CLK, with the proper clock division factor to get to the required frequency.

The conversion from pcs_rxclk domain signals to MII signals is shown in Figure 96–13. If the number of bits from the received data packet in pcs_rxclk domain is not a multiple of four, the residual bits are actually the stuff bits appended during 4B/3B conversion at the transmitter side. With 3B/4B conversion, those bits shall be discarded. RX_DV shall be deasserted right after the last nibble is converted.

If the BAD SSD state occurred in Figure 96–10a PCS Receive state diagram, the false carrier error shall be indicated on the MII after conversion.

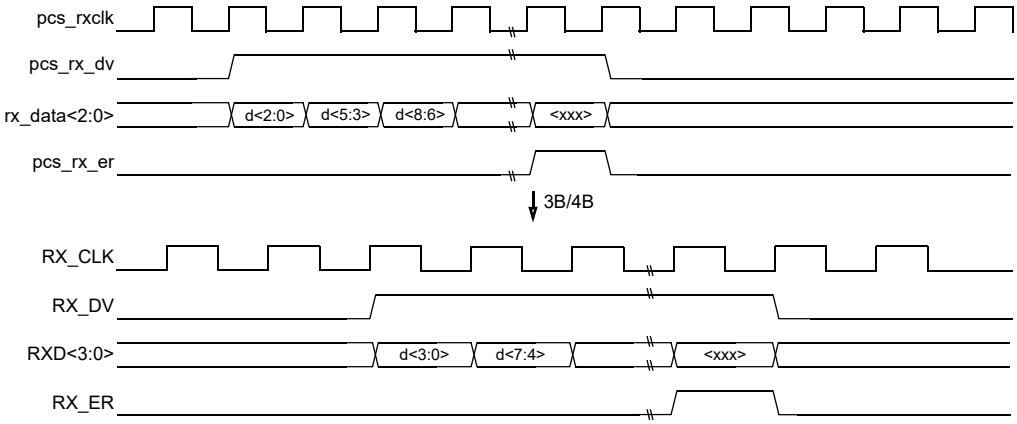

Figure 96–13—PCS Receive 3B/4B conversion reference diagram

96.3.5 PCS Loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to a one. In this mode, the PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium. The PCS loopback data flow is illustrated in Figure 96–14.

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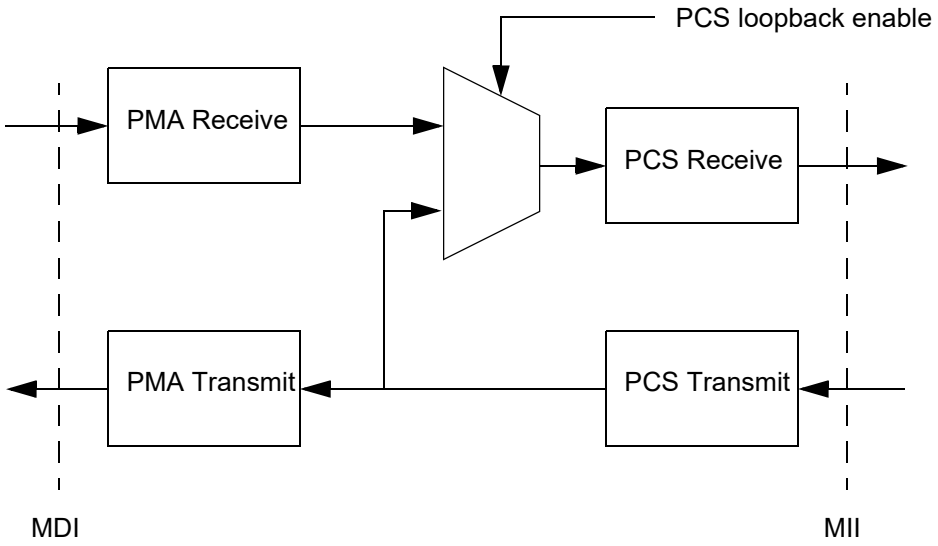

Figure 96–14—PCS loopback data flow

The MAC compares the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the functionality of 100BASE-T1 PCS functions.

96.4 Physical Medium Attachment (PMA) Sublayer

The PMA couples messages from the PMA service interface specified in 96.2.1 onto the 100BASE-T1 physical medium, and provides the link management and PHY Control functions. The PMA provides full duplex communications to and from medium employing 3-level Pulse Amplitude Modulation (PAM3). The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 96.8.

PMA functions are illustrated in Figure 96–15.

96.4.1 PMA Reset function

This function shall conform to 40.4.2.1 The optional low power mode referenced in 36.2.5.1.3 is not supported.

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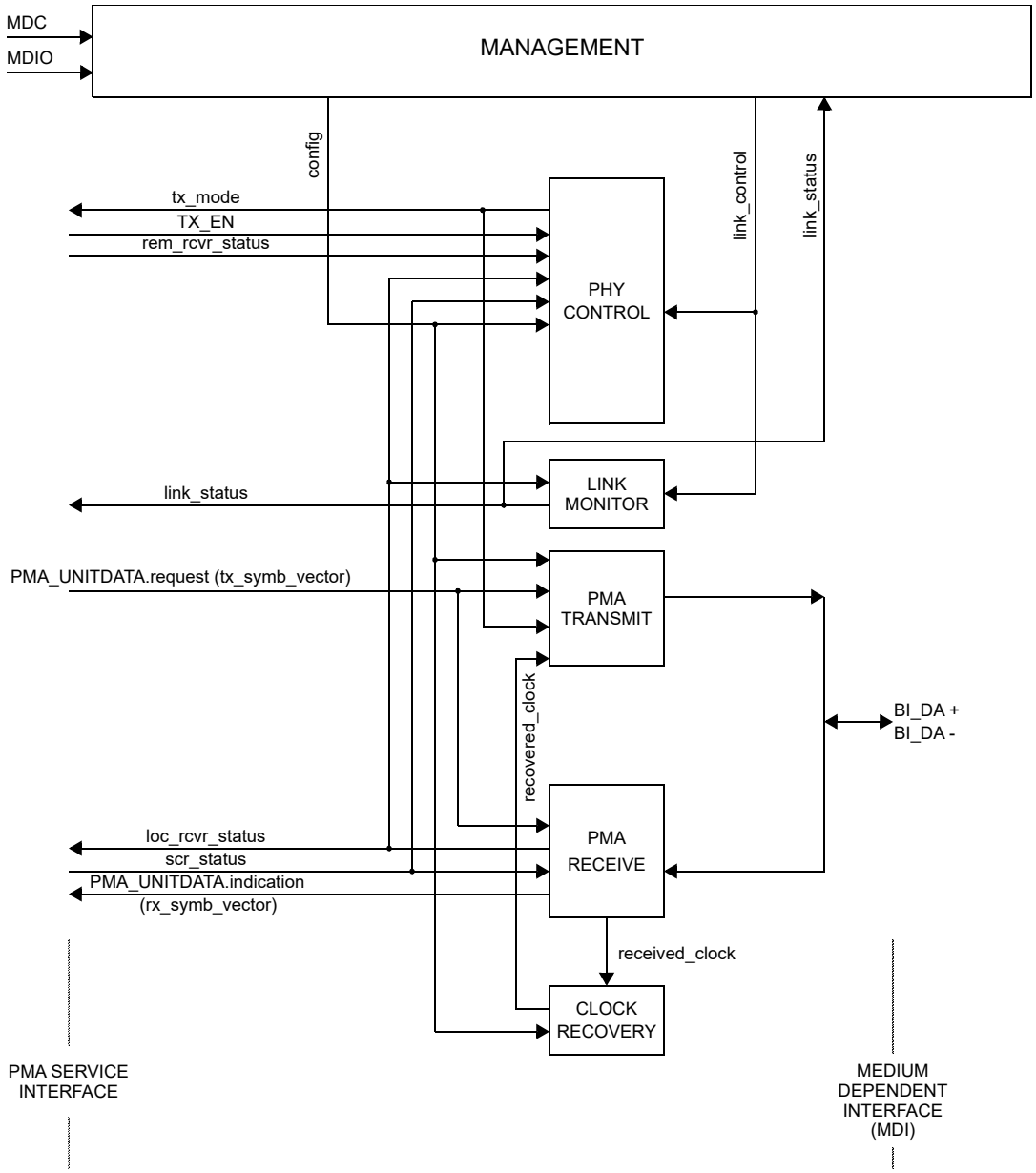

NOTE: The recovered_clock arc shown indicates delivery of the recovered clock back to PMA TRANSMIT for loop timing.

Figure 96–15—PMA functional block diagram

96.4.2 PMA Transmit function

Figure 96–16 illustrates the signal flow of the 100BASE-T1 PMA Transmit function. During transmission, PMA_UNITDATA.request conveys to the PMA using tx_symb_vector the value of the symbols to be sent over the single transmit pair.

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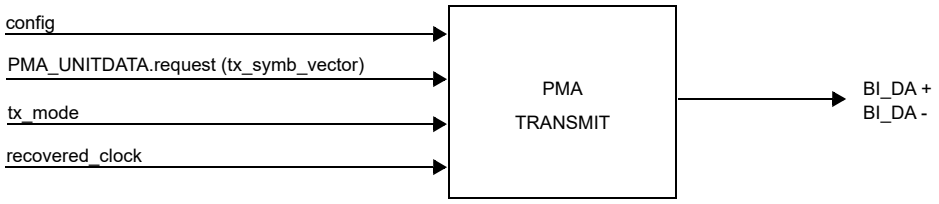

Figure 96–16—PMA Transmit

A single transmitter is used to generate the PAM3 signal BI_DA on the wire, using the transmit clock, TX_TCLK of 66.6$\overline{6}$ MHz, that is the reference clock for the MASTER. When the config parameter is set to MASTER, the PMA Transmit Function derives the TX_TCLK from a local clock source. When the config parameter is set to SLAVE, the PMA Transmit Function derives the TX_TCLK from the recovered clock.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

96.4.3 PMA Receive function

Figure 96–17 illustrates the signal flow of the 100BASE-T1 PMA Receive function. There are three primary PMA Receive characteristics: Receivers, Abilities, and Sub-Functions.

The 100BASE-T1 PMA Receive function comprises a single receiver (PMA Receive) for PAM3 modulated signals on a single balanced twisted-pair, BI_DA. PMA Receive has the ability to translate the received signals on the single pair into the PMA_UNITDATA.indication parameter rx_symb_vector. It detects ternary symbol sequences from the signals received at the MDI over one channel and presents these sequences to the PCS Receive function. PMA Receive has Signal Equalization and Echo Cancellation sub-functions. These sub-functions are used to determine the receiver performance and generate loc_rcvr_status. The parameter loc_rcvr_status is generated by PMA Receive to indicate the status of the receive link at the local PHY. This variable indicates to the PCS Transmitter, PCS Receiver, PMA PHY Control function and Link Monitor whether the status of the overall received link is ok or not. scr_status is generated by the PCS Receiver to indicate the status of the descrambler to the local PHY. It conveys the information on whether the scrambler has achieved synchronization or not to the PMA receive function.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = Fail and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5.

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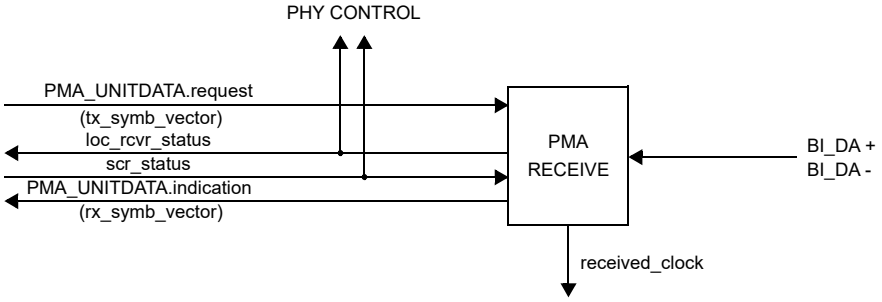

Figure 96–17—PMA Receive

96.4.4 PHY Control function

If the Auto-Negotiation process is not implemented or not enabled, PMA_CONFIG MASTER-SLAVE configuration is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup. It governs the control actions needed to bring the PHY into the 100BASE-T1 mode of operation so that frames can be exchanged with the link partner. PMA PHY Control also generates the signals that control PCS and PMA sublayer operations. It determines whether the PHY operates in the normal mode, enabling data transmission over the link segment, or whether the PHY sends special code-groups that represent the idle mode. PHY Control shall comply with the state diagram shown in Figure 96–18. PHY Control sets tx_mode to SEND_N (transmission of normal MII Data Stream, Control Information, or idle), SEND_I (transmission of IDLE code-groups), or SEND_Z (transmission of zero code-groups).

96.4.5 Link Monitor function

Link Monitor operation, as shown in state diagram of Figure 96–19, shall be provided to support PHY Control. The link_control variable is controlled by management during the PHY initialization. In all cases, the time from power_on = FALSE, transitioning to power_on = TRUE, to link_status=OK shall be less than 100 ms.

96.4.6 PMA clock recovery

This PMA function recovers the clock from the received stream. It is coupled to the receiver in order to provide the clock for optimum sampling of the channel. PMA clock recovery outputs are also used as input variables for other PMA functions.

96.4.7 State variables

96.4.7.1 State diagram variables

config
: The config parameter is set by management and passed to the PMA and PCS.
Values: MASTER or SLAVE.

link_control
: This variable is generated by management or set by default.
Values: ENABLE or DISABLE.

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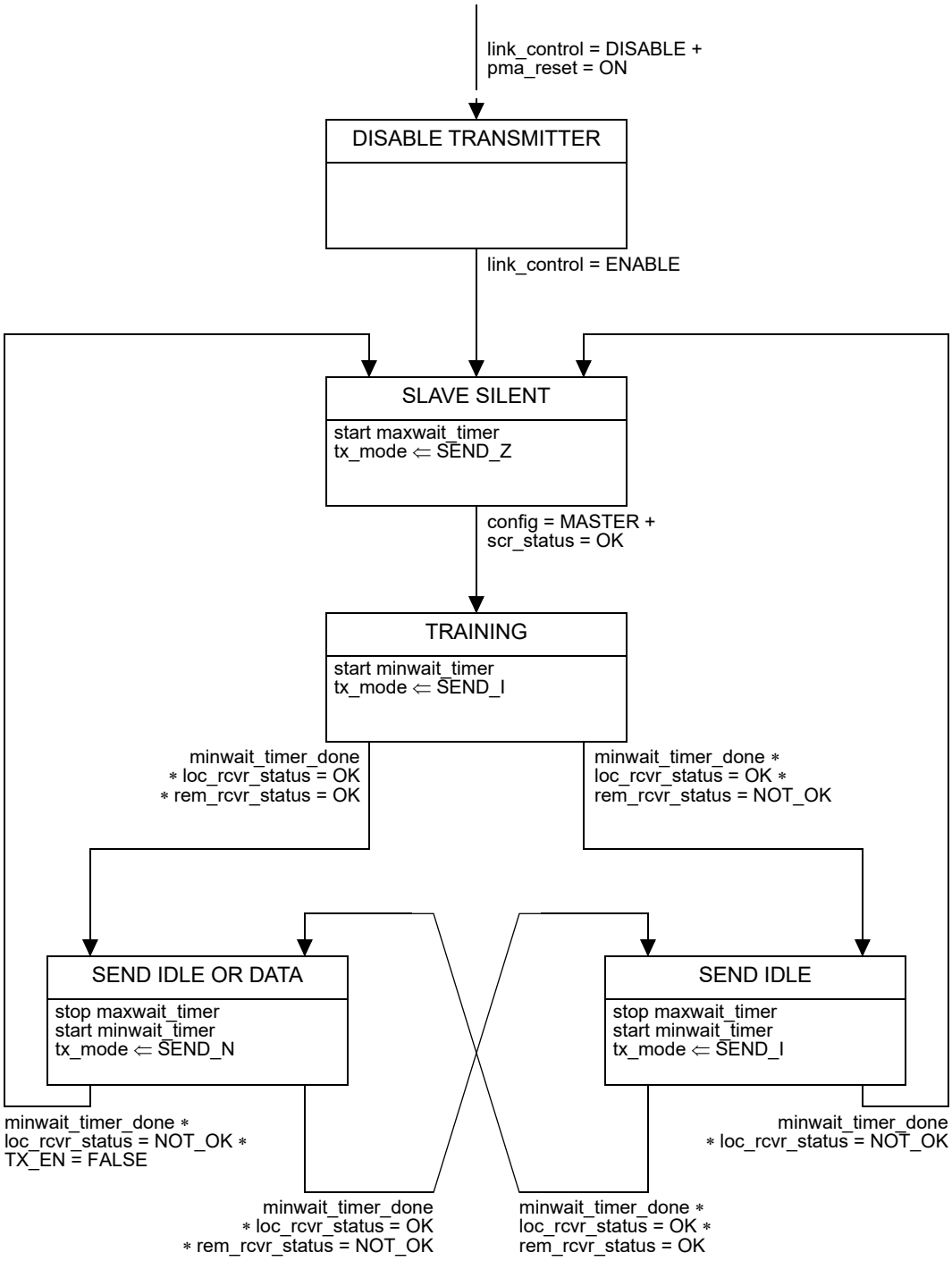

Figure 96–18—PHY Control state diagram

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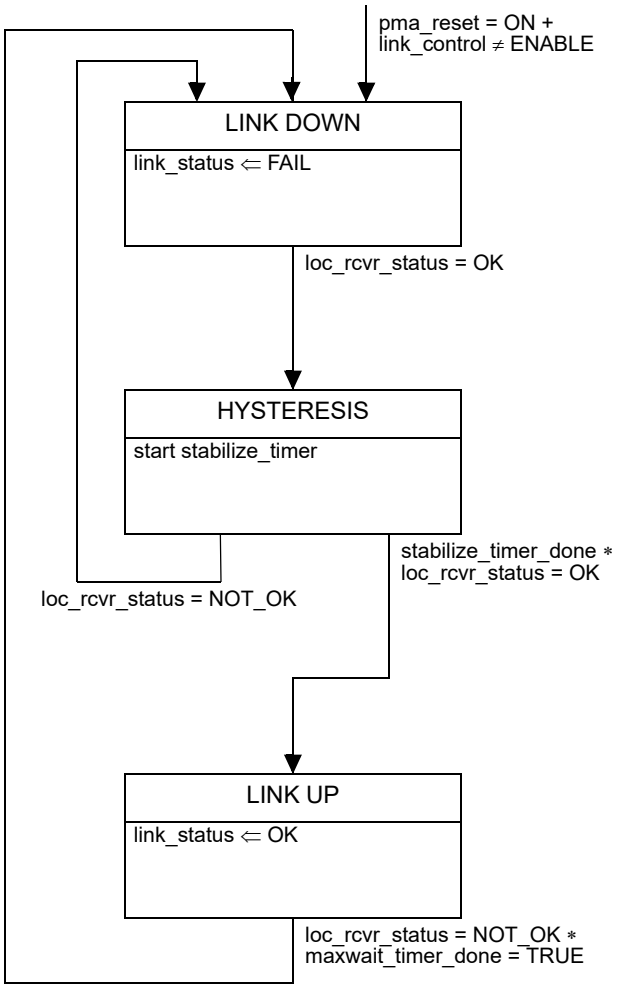

Figure 96–19—Link Monitor state diagram

link_status

This variable is generated by the PMA to indicate the status of the link.

Values: OK or FAIL.

loc_rcvr_status

Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive function for the local PHY.

Values: OK: The receive function for the local PHY is operating reliably.
NOT_OK: Operation of the receive function for the local PHY is unreliable.

pma_reset

Allows reset of all PMA functions.

Values: ON or OFF

Set by: PMA Reset

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive function for the remote PHY is detected or not.

Values: OK: The receive function for the remote PHY is operating reliably.
NOT_OK: Reliable operation of the receive function for the remote PHY is not detected.

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scr_status
: The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.
Values: OK: The descrambler has achieved synchronization.
NOT_OK: The descrambler is not synchronized.

tx_mode
: PCS Transmit sends code-groups according to the value assumed by this variable.
Values: SEND_N: This value is continuously asserted when code-group sequences representing a PCS code-group in PCS Transmit function, control information, or idle mode are transmitted.
SEND_I: This value is continuously asserted when transmission of sequences of code-groups representing the idle mode is to take place.
SEND_Z: This value is asserted when transmission of zero code-groups is to take place.

tx_enable
: The tx_enable parameter generated by PCS Transmit as specified in Figure 96–8.
Values: TRUE or FALSE.

96.4.7.2 Timers

maxwait_timer	A timer used to limit the amount of time during which a receiver dwells in the SLAVE SILENT and TRAINING states. The timer shall expire 200 ms ± 2 ms. This timer is used jointly in the PHY Control and Link Monitor state diagrams. The maxwait_timer is tested by the Link Monitor to force link_status to be set to FAIL if the timer expires and loc_rcvr_status is NOT_OK. See Figure 96–18.
minwait_timer	A timer used to determine the minimum amount of time the PHY Control stays in the TRAINING, SEND IDLE, or DATA states. The timer shall expire 1.8 µs ± 0.18 µs after being started.
stabilize_timer	A timer used to control the minimum time that loc_rcvr_status has to be OK before a transition to Link Up can occur. The timer shall expire 1.8 µs ± 0.18 µs after being started.

96.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA for a 100BASE-T1 Ethernet PHY.

96.5.1 EMC tests

Direct Power Injection (DPI) and 150 Ω emission tests for noise immunity and emission as per 96.5.1.1 and 96.5.1.2 may be used to establish a baseline for PHY EMC performance. These tests provide a high degree of repeatability and a good correlation to immunity and emission measurements. Additional tests may be needed to verify EMC performance in various configurations, applications, and conditions.

96.5.1.1 Immunity—DPI test

In a real application radio frequency (RF) common-mode (CM) noise at the PHY is the result of electromagnetic interference coupling to the cabling system. Additional differential-mode (DM) noise at the PHY is generated from the CM noise by mode conversion of all parts of the cabling system and the MDI. The sensitivity of the PMA's receiver to RF CM noise may be tested according to the DPI method of IEC 62132-4, and may need to comply with more stringent requirements as agreed upon between customer and supplier.

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96.5.1.2 Emission—Conducted emission test

The emission of the PMA transmitter to its electrical environment may be tested according to the 150 Ω direct coupling method of IEC 61967-4, and may need to comply with more stringent requirements as agreed upon between customer and supplier.

96.5.2 Test modes

The test modes described in this subclause shall be provided to allow testing of the transmitter waveform, transmitter distortion, transmitter jitter, and transmitter droop. The test modes can be enabled by setting bits 1.2102.15:13 (100BASE-T1 PMA/PMD test control register) of the PHY Management register set as described in 45.2.1.215. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

a) Test mode 1—Transmit droop test mode
b) Test mode 2—Transmit jitter test in MASTER mode
c) Test mode 4—Transmit distortion test
d) Test mode 5—Normal operation at full power (for the PSD mask)

When test mode 1 is enabled, the PHY shall transmit N "+1" symbols followed by N "–1" symbols. The value of N shall be a minimum of 34 symbol periods to achieve a symbol period greater than 500 ns. This sequence is repeated continually. For example, a PHY with test mode 1 enabled and N = 40 symbols (symbol period of 600 ns) would transmit a pattern sufficiently long enough for a 500 ns droop measurement.

When test mode 2 is enabled, the PHY shall transmit the data symbol sequence {+1, –1} repeatedly on its channel. The transmitter shall time the transmitted symbols from a 66.66$\overline{6}$ MHz ± 100 ppm clock in the MASTER timing mode.

When test mode 4 is enabled, the PHY shall transmit the sequence of symbols generated by the following scrambler generator polynomial, bit generation, and level mappings:

$$g(x) = 1 + x^{9} + x^{11} \tag{96–1}$$

The maximum-length shift register used to generate the sequences defined by this polynomial shall be updated once per symbol interval (15 ns). The bits stored in the shift register delay line at a particular time *n* are denoted by $Scr_n[10:0]$. At each symbol period the shift register is advanced by one bit and one new bit represented by $Scr_n[0]$ is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive OR'd together to generate the next $Scr_n[0]$ bit. The bit sequences, $x0_n$, and $x1_n$, generated from combinations of the scrambler bits as shown in the following equations, shall be used to generate the ternary symbols, s_n, as shown in Table 96–4. The transmitter shall time the transmitted symbols from a 66.66$\overline{6}$ MHz ± 100 ppm clock in the MASTER timing mode.

$$x0_n = Scr_n[0] \tag{96–2}$$

$$x1_n = Scr_n[1] \wedge Scr_n[4] \tag{96–3}$$

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Table 96–4—Transmitter test mode 4 symbol mapping

$x1_n$	$x0_n$	Transmit PAM3 symbol
0	0	0
0	1	1
1	0	0
1	1	–1

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask. When test mode 5 is enabled, the PHY shall transmit a pseudo-random sequence of PAM3 symbols, generated by the scrambling function described in 96.3.3.3.1.

96.5.3 Test fixtures

The fixtures shown in Figure 96–20, Figure 96–21, and Figure 96–22, or their equivalents, are used in the stated respective tests for measuring the transmitter specifications. The tolerance of resistors shall be ± 0.1%. All the transmitter tests are defined at the MDI.

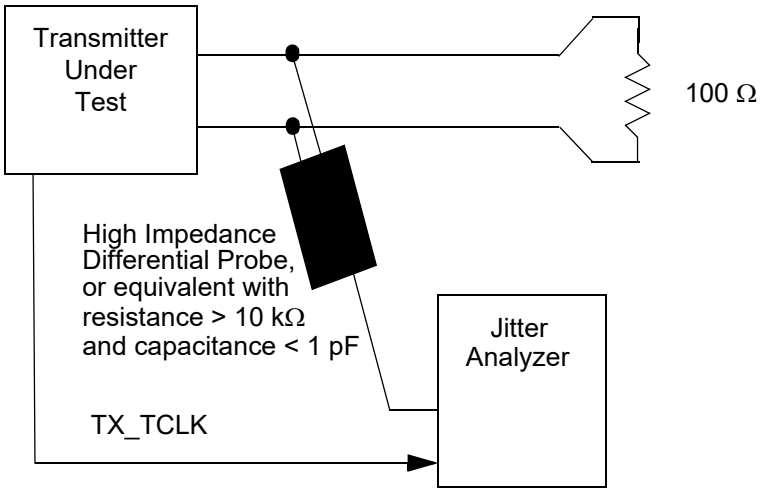

Figure 96–20—Transmitter test fixture 1: Droop, Jitter

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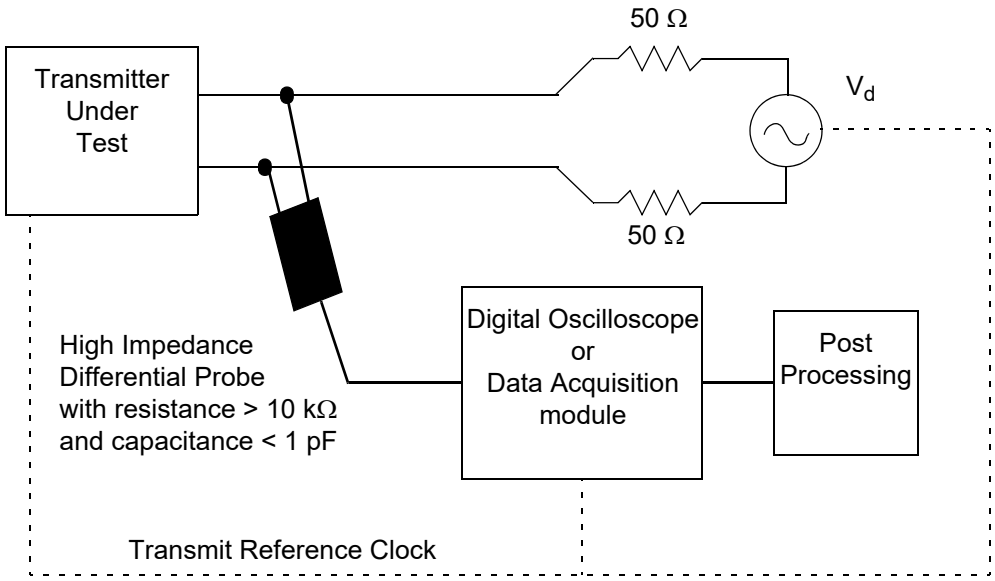

Figure 96–21—Transmitter test fixture 2: Distortion

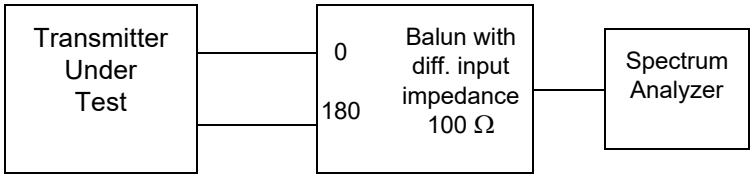

Figure 96–22—Transmitter test fixture 3: PSD mask

To allow for measurement of transmitted jitter in SLAVE modes, the PHY shall provide access to the symbol rate clock, TX_TCLK of 66.66$\overline{6}$ MHz, that times the transmitted symbols. The PHY shall provide a means to enable this clock output if it is not normally enabled.

In Figure 96–21, the disturbing signal, V_d, shall be a sine wave, synchronous with the transmit reference clock, with frequency given by one-sixth of the symbol rate and differential peak-to-peak voltage of 5.4 V.

The generator of the disturbing signal should have sufficient linearity and range that it does not introduce any appreciable distortion when connected to the transmitter output.

96.5.4 Transmitter electrical specifications

The PMA shall operate with AC coupling to the MDI. Where a load is not specified, the transmitter shall meet the requirements of this section with a 100 Ω (the value can vary within ±1% range) resistive differential load connected to the transmitter output.

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96.5.4.1 Transmitter output droop

The test mode 1 output droop is illustrated in Figure 96–23. With the transmitter in test mode 1 and using the transmitter test fixture 1, the magnitude of both the positive and negative droop measured with respect to an initial peak value after the zero crossing and the value 500 ns after the initial peak, shall be less than 45%.

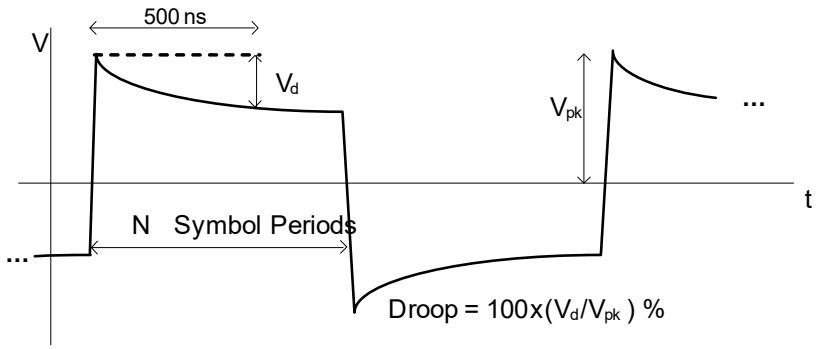

Figure 96–23—Test mode 1 output (not to scale)

When a Clause 104 Type A or Type C PI is encompassed within the MDI, the magnitude of both the positive and negative droop measured with respect to an initial peak value after the zero crossing and the value 500 ns after the initial peak, shall be less than 60%.

96.5.4.2 Transmitter distortion

The transmitter distortion is measured by capturing the test mode 4 waveform using transmitter test fixture 2. The peak distortion is determined by sampling the differential signal output with the symbol rate clock at an arbitrary phase and processing a block of consecutive samples with the code given below.[166, 167] The peak distortion values, measured at a minimum of 10 equally-spaced phases of a single symbol period, shall be less than 15 mV.

The code removes the disturbing signal from the measured data and computes the peak distortion. The code assumes the disturber signal and the data acquisition clock are frequency locked to the DUT transmit clock.

```
% 100BASE-T1 100 Mb/s single pair Ethernet PHY
% Test mode4: TX Distortion Post Processing
% Assumes frequency lock for PHY, data capturing clock and disturber

clear
Ns=2047; % Scrambler length
Nc=70;  % Canceller length

% Generate scrambler sequence
scr=ones(Ns,1);
for i=12:Ns
```

[166]This code is written in the MATLAB programming language (see 1.3); however, use of this language does not indicate an endorsement of MATLAB by IEEE and, as such, any tool can be used to perform this calculation.

[167]*Copyright release for MATLAB code:* Users of this standard may freely reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

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```
       scr(i)=mod(scr(i-11) + scr(i-9),2);
end

% PAM3 assignment
tm4=scr.*(1-2*mod(circshift(scr,1) + circshift(scr,4),2));

% Test mode4 matrix
for i=1:Nc
       X0(i,:)=circshift(tm4,1-i);
end

% Read captured data file
% 200us long, 2GSample/sec, 8bits or more accuracy
fid=fopen('RawData.bin','r');
tx = fread(fid,inf,'int16');
fclose(fid);

% LPF 33 1/3 MHz, not required if data capture accuracy is 10 bits or more
[A,B]=butter(3,1/30,'low');
tx=filter(A,B,tx);
tx=tx(1:3:end); % decimate to 10x oversampling

% HPF 1.07 MHz
tx = filter([1,-1],[1,-exp(-2*pi/625)],tx);

% Select six periods, 10x oversampling, a row vector
tx=tx((1:6*Ns*10)+2e3)'; % removes HPF transient

% Disturber removal and integration (average) of six periods
TX=fft(tx);
tx=ifft(TX(1:6:end)); % averaged and disturber frequency rejected

% Level normalization
tx=tx/(max(tx)-min(tx))*2;

% Compute distortion for 10 phases
for n=1:10
       tx1=tx(n:10:end);

       % Align data and test pattern
       temp=xcorr(tx1,tm4);
       index=find(abs(temp)==max(abs(temp)));
       X=circshift(X0, [0, mod(index(1)+Nc-10,Ns)]);

       % Compute coefficients that minimize squared error in cyclic block
       coef=tx1/X;

       % Linear canceller
       err=tx1-coef*X;

       % Peak distortion
       dist(n) = max(abs(err));
end

% Print results in mV for 10 sampling phases
format bank
peakDistortion_mV = 1000*dist'
```


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96.5.4.3 Transmitter timing jitter

When in test mode 2, the RMS (Root Mean Square) value of the MDI output jitter, J_{TXOUT}, relative to an unjittered reference shall be less than 50 ps. No high-pass filter is defined here for jitter measurement. The very low frequency components are expected to be filtered out in the setup via the memory size of the oscilloscope. For example, a digital sampling oscilloscope with 20 GSample/s with a 20 Mbytes sample memory size can only capture down to 1 kHz frequency.

When in the normal mode of operation as the SLAVE, jitter on the received signal reflects jitter on the TX_TCLK for SLAVE. Receiving valid signals from a compliant PHY operating as the MASTER with test port connected to the SLAVE, the RMS value of the SLAVE TX_TCLK jitter relative to an unjittered reference shall be less than 0.01 UI (Unit Interval) after the receiver is properly receiving the data. The test setup is shown in Figure 96–24.

For all jitter measurements, the RMS value is defined over an interval of not less than 1 ms and unjittered reference is a constant clock frequency extracted from each record of captured periodic wave. It is based on linear regression of frequency and phase that produces minimum Time Interval Error.

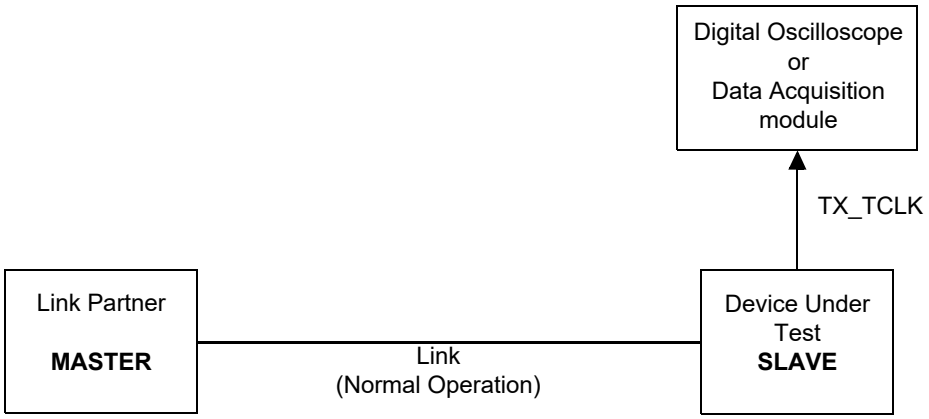

Figure 96–24—Setup for slave transmit timing jitter in normal mode

96.5.4.4 Transmitter power spectral density (PSD)

When test mode 5 is enabled, the PHY is forced to MASTER mode. In this mode, a pseudo-random sequence of ternary codes {–1, 0, +1}, which are mapped to 3 discrete differential signal levels, is transmitted.

In test mode 5, the power spectral density (PSD) of the transmitter, using the test fixture shown in Figure 96–22, shall be between the upper and lower bounds specified in the table below. The upper and lower limits are given in Equation (96–4) and Equation (96–5), and shown in Figure 96–25. The spectrum analyzer settings used for the PSD measurement should be: resolution bandwidth = 10 kHz, video bandwidth = 30 kHz, sweep time > 60 s, and RMS detector.

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$$\text{Upper PSD}\ (f)\ = \begin{cases} -63.3 - 1.5 \times \dfrac{f-1}{19}\ \text{dBm/Hz} & \text{for}\ \ 1\ \text{MHz}\ \ \le f < 20\ \text{MHz} \\ -64.8 - 3.7 \times \dfrac{f-20}{20}\ \text{dBm/Hz} & \text{for}\ \ 20\ \text{MHz}\ \le f < 40\ \text{MHz} \\ -68.5 - 8.0 \times \dfrac{f-40}{17}\ \text{dBm/Hz} & \text{for}\ \ 40\ \text{MHz}\ \le f < 57\ \text{MHz} \\ -76.5\ \text{dBm/Hz} & \text{for}\ \ 57\ \text{MHz}\ \le f \le 200\ \text{MHz} \end{cases} \tag{96–4}$$

$$\text{Lower PSD}\ (f)\ = \begin{cases} -70.9 - 4.9 \times \dfrac{f-1}{19}\ \text{dBm/Hz} & \text{for}\ \ 1\ \text{MHz}\ \ \le f < 20\ \text{MHz} \\ -75.8 - 13.4 \times \dfrac{f-20}{20}\ \text{dBm/Hz} & \text{for}\ \ 20\ \text{MHz}\ \le f < 40\ \text{MHz} \end{cases} \tag{96–5}$$

where

Upper PSD(f)	is the upper limit of the PSD of the transmitted signal frequency f
Lower PSD(f)	is the lower limit of the PSD of the transmitted signal frequency f
f	is the frequency in MHz

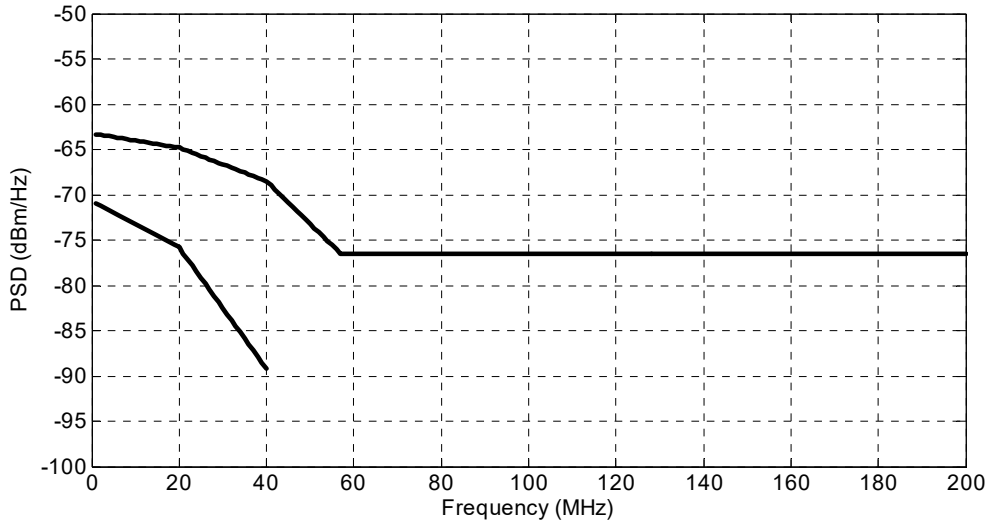

Figure 96–25—PSD upper and lower limits

96.5.4.5 Transmit clock frequency

The symbol transmission rate of the MASTER PHY shall be within the range 66.66$\overline{6}$ MBd ±100 ppm.

96.5.5 Receiver electrical specifications

The PMA shall meet the Receive function specified in PMA Receive function and the electrical specifications of this section. The single balanced twisted-pair cabling system used in test configurations shall be within the limits specified in 96.7.

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96.5.5.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of Transmitter Electrical Specifications and have passed through a link specified in 96.7, shall be received with a bit error ratio less than 10^{-10}.

96.5.5.2 Receiver frequency tolerance

The receiver feature shall properly receive incoming data with a symbol rate within the range 66.66$\overline{6}$ MBd ±100 ppm.

96.5.5.3 Alien crosstalk noise rejection

This specification is provided to verify the DUT's tolerance to alien crosstalk noise using two separate tests. The first test is performed with a noise source consisting of a 100BASE-T1 compliant transmitter sending idle symbols. The level of the noise at the MDI is nominally 100 mV peak-to-peak. The second test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwith of 50 MHz and magnitude of –85 dBm/Hz. The receive DUT is connected to these noise sources through a resistive network, as shown in Figure 96–26, with a link segment as defined in 96.7. The noise is added at the MDI of the DUT. The BER shall be less than 10^{-10}, and to satisfy this specification the frame error ratio is less than 10^{-7} for 125 octet packets measured at MAC/PLS service interface.

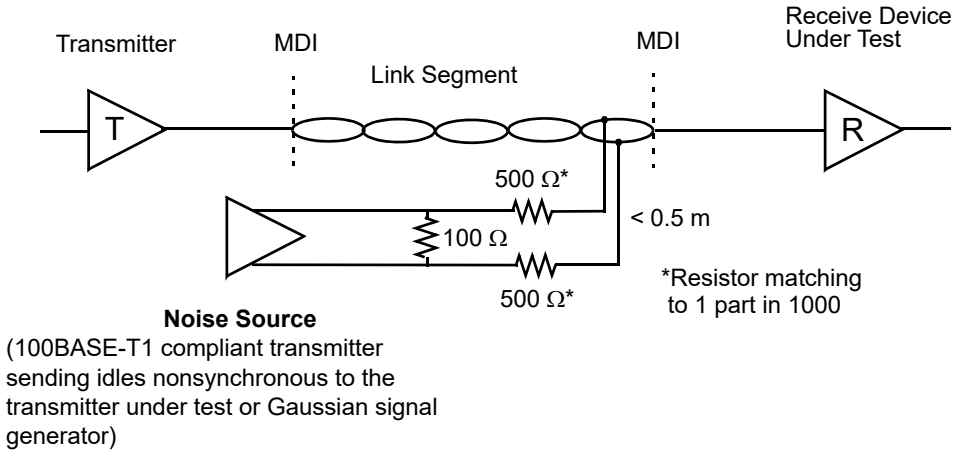

Figure 96–26—Alien crosstalk noise rejection test setup

96.5.6 Transmitter peak differential output

When measured with 100 Ω termination, transmit differential signal at MDI shall be less than 2.2 V peak-to-peak. This limit applies to all transmit modes including SEND_I and SEND_N modes.

96.5.7 PMA Local Loopback

The PMA local loopback function is optional. If supported, the PMA shall be placed in local loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, is set to a one. When the PHY is in the PMA local loopback mode the PMA Receive function utilizes the echo signals from the untermina-

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ted MDI and decodes these signals to pass the data back to the MII Receive interface. The data flow of the external loopback is shown in Figure 96–27.

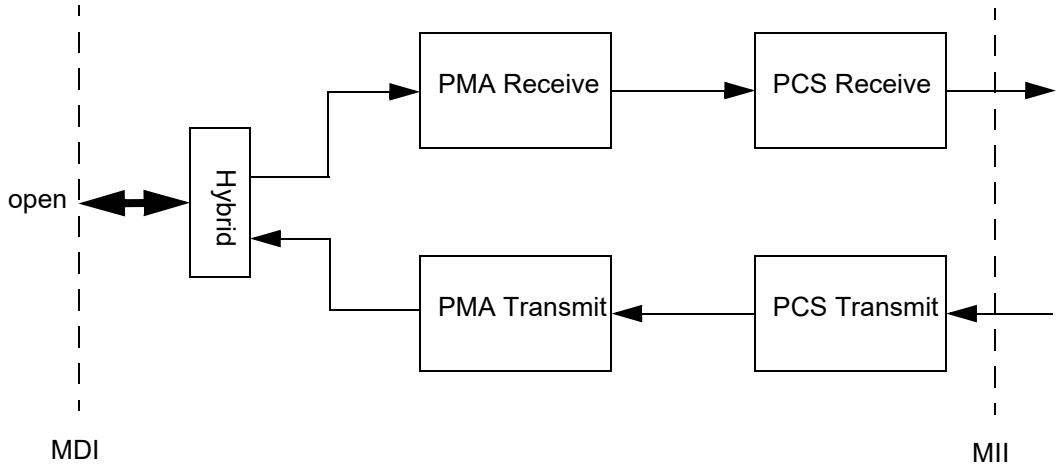

Figure 96–27—PMA loopback data flow

A MAC Client may compare the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the 100BASE-T1 PCS and PMA functions.

96.6 Management interface

100BASE-T1 uses the management interface as specified in Clause 45. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

96.6.1 MASTER-SLAVE configuration

MASTER-SLAVE assignment for each link configuration is necessary for establishing the timing control of each PHY. In 100BASE-T1, one PHY shall be configured as MASTER and one PHY shall be configured as SLAVE to operate. In the case where both PHYs are configured to be MASTER or both to be SLAVE, operation is undefined.

96.6.2 PHY-initialization

Both PHYs sharing a link segment are capable of being MASTER or SLAVE. A forced assignment scheme is employed depending on the physical deployment of the PHY within the application (e.g., at a multi-port bridge versus an end point). This process is conducted at the power-up or reset condition. The station management system manually configures the 100BASE-T1 PHY to be MASTER (before the link acquisition process starts) while the link partner defaults to SLAVE (un-managed).

96.6.3 PMA and PCS MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA and PCS. Mapping of MDIO register bits to PMA and PCS control/status variables is shown in Table 96–5.

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Table 96–5—MDIO register bit mapping reset and loopback control and link status variables

Register name	Register/bit number	Controls/status variable
PMA/PMD control 1	1.0.15	pma_reset
PMA/PMD control 1	1.0.0	PMA loopback
PCS control 1	3.0.15	pcs_reset
PCS control 1	3.0.14	PCS loopback
PMA/PMD status 1	1.1.2	link_status

96.7 Link segment characteristics

The 100BASE-T1 PHY is designed to operate over a single balanced twisted-pair cabling system. The single balanced twisted-pair cable supports an effective data rate of 100 Mb/s in each direction simultaneously. The link segment for a 100BASE-T1 PHY system is defined as in Figure 96–28, which consists of up to 15 m of single balanced twisted-pair cabling, with up to four in-line connectors and two mating connectors.

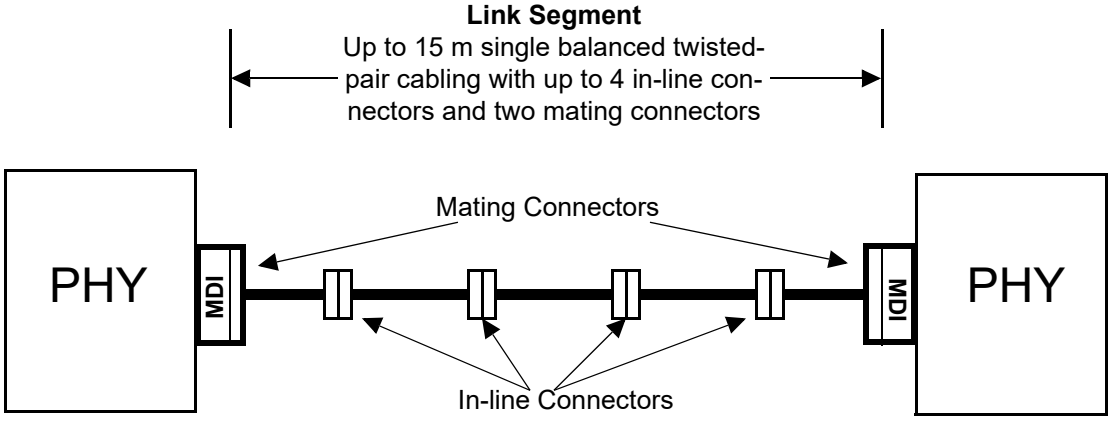

Figure 96–28—Link segment definition

96.7.1 Cabling system characteristics

The cabling system used in Figure 96–28 to support the 100BASE-T1 PHY is composed of a single balanced twisted-pair cable up to 15 m in length with associated connectors, and with impedance in the range of 90 Ω to 110 Ω (nominal 100 Ω) to support a data rate of 100 Mb/s in each direction simultaneously.

The transmission parameters contained in this specification are chosen to enable reliable operation over a single balanced twisted-pair cable link segment. The transmission parameters of the link segment include insertion loss, return loss, mode conversion loss, characteristic impedance, power sum alien near-end crosstalk, and power sum alien attenuation to crosstalk ratio far-end.

96.7.1.1 Characteristic impedance

The characteristic impedance of the cable and any mated MDI connector shall be 100 Ω ±10% measured with TDR and rise-time set not slower than 700 ps.

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96.7.1.2 Insertion loss

The insertion loss of the link segment shown in Figure 96–28 when measured with a 100 Ω termination shall be less than that contained in Equation (96–6).

$$\text{Insertion loss}\,(f) < \begin{cases} 1.0 + 1.6 \times \sqrt{\frac{f-1}{9}} \ \text{dB} & \text{for} \ \ 1\ \text{MHz} \le f < 10\ \text{MHz} \\ 2.6 + 2.3 \times \sqrt{\frac{f-10}{23}} \ \text{dB} & \text{for} \ \ 10\ \text{MHz} \le f < 33\ \text{MHz} \\ 4.9 + 2.3 \times \sqrt{\frac{f-33}{33}} \ \text{dB} & \text{for} \ \ 33\ \text{MHz} \le f \le 66\ \text{MHz} \end{cases} \tag{96–6}$$

where

Insertion loss(f)	is the Insertion loss of the link segment at frequency f
f	is the frequency in MHz

96.7.1.3 Return loss

The return loss of the link segment in Figure 96–28 shall meet or exceed Equation (96–7) for all frequencies from 1 MHz to 66 MHz (with 100 Ω reference impedance).

$$\text{Return loss}\,(f) \ge \begin{cases} 18 \ \text{dB} & \text{for} \ \ 1\ \text{MHz} \le f \le 20\ \text{MHz} \\ 18 - 10 \times \log_{10}\left(\frac{f}{20}\right) \ \text{dB} & \text{for} \ \ 20\ \text{MHz} \le f \le 66\ \text{MHz} \end{cases} \tag{96–7}$$

where

Return loss(f)	is the return loss of the link segment at frequency f
f	is the frequency in MHz

96.7.1.4 Mode conversion loss

Mode conversion LCL and LCTL (Sdc11, Sdc22 and Sdc21, Sdc12) of the link segment defined in 96.7 shall meet or exceed the limit defined in Equation (96–8) for all frequencies from 1 MHz to 200 MHz.

$$\text{Mode conversion loss}(f) \ge \begin{cases} 43 \ \text{dB} & \text{for} \ \ 1\ \text{MHz} \le f \le 33\ \text{MHz} \\ 43 - 20 \times \log_{10}\left(\frac{f}{33}\right) \ \text{dB} & \text{for} \ \ 33\ \text{MHz} \le f \le 200\ \text{MHz} \end{cases} \tag{96–8}$$

where

Mode conversion loss(f)	is the common-to-differential-mode conversion at frequency f
f	is the frequency in MHz

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Alternatively, TCL and TCTL (Scd11, Scd22 and Scd21, Scd12) may be measured to pass the limit line.

96.7.1.5 Power sum alien near-end crosstalk (PSANEXT)

There is no FEXT or NEXT as 100BASE-T1 is a single pair solution. When multiple cable pairs are bundled, the alien XTALK (ANEXT and AFEXT) become interference sources. Since the transmitted symbols from the alien noise source in one cable are not available to another cable, cancellation cannot be done. When there are multiple pairs of cables bundled together, where all pairs carry 100 Mb/s links, then each duplex link is disturbed by neighboring links, degrading the signal quality on the victim pair. In order to limit the near-end crosstalk noise for a 5-around-1 cable bundle (up to 15 m length and up to four in-line connectors, equally spaced), the Power sum alien near-end crosstalk (PSANEXT) loss shall meet Equation (96–9).

$$\text{PSANEXT}(f) \geq 31.5 - 10 \times \log_{10}\left(\frac{f}{100}\right) \quad \text{dB} \qquad \text{for} \quad 1\ \text{MHz} \leq f \leq 100\ \text{MHz} \qquad (96\text{–}9)$$

where

PSANEXT(f) is the power sum alien near-end crosstalk loss at frequency f
f is the frequency in MHz

96.7.1.6 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

The Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) for a 5-around-1 cable bundle (up to 15 m length and up to four in-line connectors, equally spaced) shall meet Equation (96–10).

$$\text{PSAACRF}(f) \geq 16.5 - 20 \times \log_{10}\left(\frac{f}{100}\right) \quad \text{dB} \qquad \text{for} \quad 1\ \text{MHz} \leq f \leq 100\ \text{MHz} \qquad (96\text{–}10)$$

where

PSAACRF(f) is the power sum alien attenuation to crosstalk ratio far-end at frequency f
f is the frequency in MHz

96.7.2 Noise environment

In the 100BASE-T1 automotive environment, there are several types of noise sources:

a) Echo from the local transmitter on the same cable pair is caused by the hybrid function for bidirectional data transmission in the 100BASE-T1 duplex channel and by the impedance discontinuities in the link segment. Echo cancellation techniques, up to each PHY implementer, are generally used to achieve the objective BER level.

b) The typical background noise is mainly due to thermal noise. Thermal noise, with level roughly at –140 dBm/Hz, is not a critical contributor that would impact performance. 100BASE-T1 signaling allows a robust margin over a 15 m single balanced twisted-pair cabling channel to combat thermal noise.

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c) PSANEXT as described in 96.7.1.5.

d) PSAACRF as described in 96.7.1.6.

96.8 MDI specification

This section defines the MDI for 100BASE-T1.

96.8.1 MDI connectors

The mechanical interface to the balanced cabling is a 2-pin connector or 2 pins of a multi-pin connector.

96.8.2 MDI electrical specification

The MDI connector mated with a specified single balanced twisted-pair cable connector shall meet the electrical requirements specified in 96.7.1, except for return loss, and 96.7.2.

96.8.2.1 MDI return loss

The MDI return loss (RL) shall meet or exceed Equation (96–11) for all frequencies from 1 MHz to 66 MHz (with 100 Ω reference impedance) at all times when the PHY is transmitting data or control symbols.

When a Clause 104 Type A or Type C PI is encompassed within the MDI, the MDI return loss (RL) shall meet or exceed Equation (96–12) for all frequencies from 1 MHz to 66 MHz (with 100 Ω reference impedance) at all times when the PHY is transmitting data or control symbols.

$$\text{MDI return loss}\ (f) \geq \begin{cases} 20\ \text{dB} & \text{for}\ \ 1\ \text{MHz} \leq f \leq 30\ \text{MHz} \\ 20 - 20 \times \log_{10}\left(\frac{f}{30}\right)\ \text{dB} & \text{for}\ \ 30\ \text{MHz} \leq f \leq 66\ \text{MHz} \end{cases} \tag{96–11}$$

$$\text{MDI return loss}(f) \geq \left\{ \begin{array}{ll} 20 - 20 \times \log_{10}\left(\frac{2}{f}\right) & 1 \leq f < 2 \\ 20 & 2 \leq f < 30 \\ 20 - 20 \times \log_{10}\left(\frac{f}{30}\right) & 30 \leq f < 66 \end{array} \right\} \text{dB} \tag{96–12}$$

where

MDI return loss(f) is the MDI return loss at frequency f
f is the frequency in MHz

96.8.2.2 MDI mode conversion loss

Mode conversion LCL (Sdc11) of the PHY measured at MDI shall meet or exceed the limit defined in Equation (96–13) for all frequencies from 1 MHz to 200 MHz.

$$\text{MDI mode conversion loss}(f) \geq \begin{cases} 50\ \text{dB} & \text{for}\ \ 1\ \text{MHz} \leq f \leq 33\ \text{MHz} \\ 50 - 20 \times \log_{10}\left(\frac{f}{33}\right)\ \text{dB} & \text{for}\ \ 33\ \text{MHz} \leq f \leq 200\ \text{MHz} \end{cases} \tag{96–13}$$

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where

MDI mode conversion loss(f) is the MDI mode conversion loss at frequency f

f is the frequency in MHz

Alternatively, TCL (Scd11) may be measured to pass the limit line.

96.8.3 MDI fault tolerance

The wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 96–6, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is (are) removed.

The wire pair of the MDI shall also withstand without damage high-voltage transient noises and ESD per application requirements.

Table 96–6—Connection fault

BI_DA+	BI_DA-
No fault	No fault
BI_DA–	BI_DA+
Ground	No fault
No fault	Ground
+50 V dc	No fault
No fault	+50 V dc
Ground	+50 V dc
+50 V dc	Ground

96.9 Environmental specifications

96.9.1 General safety

All equipment subject to this clause is expected to conform to all applicable local, state, national, and application-specific standards.

96.9.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner. In automotive applications, all 100BASE-T1 cabling shall be routed in way to provide maximum protection by the motor vehicle sheet metal and structural components, following SAE J1292, ISO 14229, and ISO 15764.

96.9.2.1 Environmental safety

In automotive applications, all equipment subject to this clause shall conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications:

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a) General loads: ISO 16750-1
b) Electrical loads: ISO 16750-2, ISO 7637-2:2008, and ISO 8820-1
c) Mechanical loads: ISO 16750-3, ASTM D4728, and ISO 12103-1
d) Climatic loads: ISO 16750-4 , IEC 60068-2-1, IEC 60068-2-27, IEC 60068-2-30, IEC 60068-2-38, IEC 60068-2-52, IEC 60068-2-64, and IEC 60068-2-78
e) Chemical loads: ISO 16750-5 and ISO 20653

Automotive environmental conditions are generally more severe than those found in many commercial environments. The targeted application environment(s) require careful analysis prior to implementation.

96.9.2.2 Electromagnetic compatibility

A system integrating the 100BASE-T1 PHY shall comply with all applicable local and national codes. In addition, the system may need to comply with more stringent requirements as agreed upon between customer and supplier, for the limitation of electromagnetic interference. In automotive applications, a 100BASE-T1 PHY shall be tested according to CISPR 25 test methods, and shall meet the following motor vehicle EMC requirements:

a) Radiated/Conducted Emissions: CISPR 25, IEC 61967-1/4, and IEC 61000-4-21
b) Radiated/Conducted Immunity: ISO 11452, IEC 62132-1/4, and IEC 61000-4-21
c) Electrostatic Discharge: ISO 10605 and IEC 61000-4-2/3
d) Electrical Disturbances: IEC 62215-3 and ISO 7637-2/3

Exact test setup and test limit values may be adapted to each specific application, subject to agreement between the customer and the supplier.

96.10 Delay constraints

Every 100BASE-T1 PHY associated with MII shall comply with the bit delay constraints for full duplex operation. The delay for the transmit path, from the MII input to the MDI, shall be less than 360 ns. The delay for the receive path, from the MDI to the MII output, shall be less than 960 ns.

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96.11 Protocol implementation conformance statement (PICS) proforma for Clause 96, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T1[168]

96.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 96, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) and baseband medium, type 100BASE-T1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

96.11.2 Identification

96.11.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

96.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 96, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T1
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[168] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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96.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
MII	PHY associated with MII	96.1	Interface is supported	O	Yes [ ] No [ ]
PCS	100BASE-T1 PCS	96.3		M	Yes [ ]
PMA	100BASE-T1 PMA	96.4		M	Yes [ ]
*CHNL	Channel	96.7	Channel specification not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
*MD	MDIO Capability	96.1	Register and Interface supported	O	Yes [ ] No [ ]
*AUTO	Automotive environment installation			O	Yes [ ] No [ ]
*POWER	PHY implemented with Clause 104 power	Clause 104		O	Yes [ ] No [ ]
AN	Auto-negotiation	96.1.1	If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.	O	Yes [ ] No [ ]

96.11.4 PICS proforma tables for Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T1

96.11.4.1 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Value/Comment	Status	Support
PCT1	PCS Transmit state diagram	96.3.3.2	See Figure 96–7	M	Yes [ ]
PCT2	PCS data transmission enabling state diagram	96.3.2	See Figure 96–5	M	Yes [ ]
PCT3	tx_data<2:0>, tx_enable and tx_error	96.3.3.1.1	Be synchronized with PCS transmit clock pcs_txclk	M	Yes [ ]
PCT4	TX_TCLK in MASTER mode	96.3.3.1.1	Derived from a local source in MASTER mode	M	Yes [ ]
PCT5	TX_TCLK in SLAVE mode	96.3.3.1.1	Derived from the recovered clock in SLAVE mode	M	Yes [ ]
PCT6	Transmit data	96.3.3.1.2	Be converted into 3 bits (tx_data<2:0>)	M	Yes [ ]
PCT7	Stuff bits	96.3.3.1.2	Append stuff bits to the end of a packet (1 or 2 bits) when the number of bits in a packet is not a multiple of 3	M	Yes [ ]
PCT8	symb_pair_timer	96.3.3.2.3	Generated synchronously with PCS transmit clock pcs_txclk	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PCT9	symb_timer	96.3.3.2.3	Generated synchronously with TX_TCLK	M	Yes [ ]
PCT10	scrambler function	96.3.3.3.1	Conform to 40.3.1.3.1 and associated Figure 40–6	M	Yes [ ]
PCT11	Sy_n[2:0]	96.3.3.3.2	Conform to and be generated in accordance with the encoding rules in 40.3.1.3.2 and 40.3.1.3.3	M	Yes [ ]
PCT12	Sc_n[2:0]	96.3.3.3.2	Conform to and be generated in accordance with the encoding rules in 40.3.1.3.2 and 40.3.1.3.3	M	Yes [ ]
PCT13	Sd_n[2:0]	96.3.3.3.4	Generated as defined in 96.3.3.3.4	M	Yes [ ]
PCT14	Sx_n	96.3.3.3.8	Generated as defined in 96.3.3.3.8	M	Yes [ ]

96.11.4.2 PCS Receive functions

Item	Feature	Subclause	Value/Comment	Status	Support
PCR1	PCS Receive state diagram	96.3.4.1	See Figure 96–10a and Figure 96–10b	M	Yes [ ]
PCR2	rcv_max_timer	96.3.4.1.3	Expire 1.08 ms ±54 μs after being started	M	Yes [ ]
PCR3	3B/4B conversion in PCS Receive	96.3.4.2	The number of bits recevied in a packet is always a multiple of 3 that shall go through the process of 3B/4B conversion, discarding the residual 1 bit or 2 bits of data	M	Yes [ ]
PCR4	PCS Receive	96.3.4.2	Set pcs_rx_er = TRUE when it receives bad ESDs, ERR_ESD, or bad SSDs	M	Yes [ ]
PCR5	PCS receive descrambler polynomial	96.3.4.3	Conform to 40.3.1.4.2, with the exception that it applies to rx_data<2:0>	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PCR6	PCS receive automatic polarity detection	96.3.4.4	Invert its transmitted signals (TAn, TBn)	O	Yes [ ] No [ ]
PCR7	rx_data<2:0>, rx_enable and rx_error	96.3.4.5	Be synchronized with pcs_rxclk	M	Yes [ ]
PCR8	Residual bits	96.3.4.5	When the number of bits from the received data packet is not a multiple of four, those extra bits are discarded	M	Yes [ ]
PCR9	RX_DV	96.3.4.5	Deasserted right after the last nibble is converted	M	Yes [ ]
PCR10	False carrier error	96.3.4.5	Indicated on the MII after conversion	M	Yes [ ]

96.11.4.3 PCS Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
PCL1	PCS Loopback	96.3.5	The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to a one.	M	Yes [ ]
PCL2	PCS Loopback function	96.3.5	The PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII.	M	Yes [ ]
PCL3	PHY receive circuitry isolation	96.3.5	The PHY receive circuitry shall be isolated from the network medium.	M	Yes [ ]
PCL4	PHY transmit circuity isolation	96.3.5	The assertion of TX_EN at the MII shall not result in the transmission of data on the network medium.	M	Yes [ ]

96.11.4.4 Physical Medium Attachment (PMA)

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Item	Feature	Subclause	Value/Comment	Status	Support
PMF1	PMA reset function	96.4.1	Conform to 40.4.2.1, optional low power mode referenced in 36.2.5.1.3 not supported.	M	Yes [ ]
PMF2	PMA transmit fault function	96.4.2	Be mapped to the transmit fault bit as specified in 45.2.1.7.4.	MDIO:M	Yes [ ] N/A [ ]
PMF3	PMA receive function	96.4.3	Contribute to the receive fault bit specified in 45.2.1.7.5.	MDIO:M	Yes [ ] N/A [ ]
PMF4	PHY Control function	96.4.4	See Figure 96–18.	M	Yes [ ]
PMF5	Link Monitor function	96.4.5	See Figure 96–19.	M	Yes [ ]
PMF6	Time from power_on = FALSE, transitioning to power_on = TRUE, to link_status=OK	96.4.5	Less than 100 ms.	M	Yes [ ]
PMF7	maxwait_timer	96.4.7.2	Expire 200 ms ± 2 ms.	M	Yes [ ]
PMF8	minwait_timer	96.4.7.2	Expire 1.8 µs ± 0.18 µs after being started.	M	Yes [ ]
PMF9	stabilize_timer	96.4.7.2	Expire 1.8 µs ± 0.18 µs after being started.	M	Yes [ ]

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96.11.4.5 PMA electrical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PME1	Test modes	96.5.2	Provided to allow testing of the transmitter waveform, transmitter distortion, transmitter jitter, and transmitter droop	M	Yes [ ]
PME2	These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.	96.5.2		M	Yes [ ]
PME3	When test mode 1 is enabled, the PHY shall	96.5.2	Transmit N "+1" symbols followed by N "–1" symbols. The value of N (minimum of 34) shall be chosen such that N symbol period is greater than 500 ns	M	Yes [ ]
PME4	When test mode 2 is enabled, the PHY shall	96.5.2	Transmit the data symbol sequence {+1, –1} repeatedly on its channel. The transmitter shall time the transmitted symbols from a $66.66\overline{6}$ MHz ± 100 ppm clock in the MASTER timing mode	M	Yes [ ]
PME5	When test mode 4 is enabled, the PHY shall	96.5.2	Transmit the sequence of symbols generated by the scrambler generator polynomial, bit generation, and level mappings as defined in 96.5.2	M	Yes [ ]
PME6	The maximum-length shift register used to generate the sequences defined by this polynomial shall	96.5.2	Be updated once per symbol interval (15 ns)	M	Yes [ ]
PME7	The transmitter shall	96.5.2	Time the transmitted symbols from a $66.66\overline{6}$ MHz ± 100 ppm clock in the MASTER timing mode	M	Yes [ ]
PME8	When test mode 5 is enabled, the PHY shall	96.5.2	Transmit a pseudo-random sequence of PAM3 symbols, generated by the scrambling function described in 96.3.3.3	M	Yes [ ]
PME9	The tolerance of resistors shall be ± 0.1%.	96.5.3		M	Yes [ ]
PME10	The PHY shall provide access to the symbol rate clock, TX_TCLK of $66.66\overline{6}$ MHz, that times the transmitted symbols.	96.5.3		M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PME11	The PHY shall provide a means to enable TX_TCLK output if it is not normally enabled.	96.5.3		M	Yes [ ]
PME12	The disturbing signal, V_d	96.5.3	Be a sine wave, synchronous with the transmit reference clock, with frequency given by one-sixth of the symbol rate and differential peak-to-peak voltage of 5.4 V	M	Yes [ ]
PME13	PMA	96.5.4	Operate with AC coupling to the MDI	M	Yes [ ]
PME14	The positive and negative droop without Clause 104 power	96.5.4.1	Be less than 45% with respect to an initial peak value after the zero crossing and the value 500 ns after the initial peak	!POWER:M	Yes [ ] N/A [ ]
PME15	The positive and negative droop without Clause 104 power	96.5.4.1	Be less than 60% with respect to an initial peak value after the zero crossing and the value 500 ns after the initial peak	POWER:M	Yes [ ] N/A [ ]
PME16	The peak distortion values, measured at a minimum of 10 equally-spaced phases of a single symbol period	96.5.4.2	Be less than 15 mV	M	Yes [ ]
PME17	When in test mode 2, the RMS value of the MDI output jitter, J_{TXOUT}, relative to an unjittered reference	96.5.4.3	Be less than 50 ps	M	Yes [ ]
PME18	When in the normal mode of operation as the SLAVE, the RMS value of the SLAVE TX_TCLK jitter relative to an unjittered reference	96.5.4.3	Be less than 0.01 UI	M	Yes [ ]
PME19	For all jitter measurements, the RMS value shall be measured over an interval of not less than 1 ms and unjittered reference is a constant clock frequency extracted from each record of captured periodic wave.	96.5.4.3		M	Yes [ ]
PME20	In test mode 5, PSD of the transmitter	96.5.4.4	Be between the upper and lower bounds given in Equation (96–4) and Equation (96–5), and shown in Figure 96–25	M	Yes [ ]
PME21	The symbol transmission rate of the MASTER PHY	96.5.4.5	Be within the range $66.66\overline{6}$ MBd ±100 ppm	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PME22	Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of Transmitter Electrical Specifications and have passed through a link specified in 96.7, shall be received with a bit error ratio less than 10^{-10}.	96.5.5.1		M	Yes [ ]
PME23	The receiver feature	96.5.5.2	Properly receive incoming data with a symbol rate within the range 66.66$\overline{6}$ MBd ±100 ppm	M	Yes [ ]
PME24	The alien crosstalk test specified in 96.5.5.3 shall be satisfied by	96.5.5.3	A bit error ratio of less than 10^{-10} that is derived from a measured packet error ratio less than 10^{-7} for 125 octet packets.	M	Yes [ ]
PME25	Transmit differential signal	96.5.6	Less than 2.2 V peak-to-peak when measured with a 100 Ω termination	M	Yes [ ]
PME26	PMA Local Loopback	96.5.7	The PMA is placed in local loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, is set to a one	O	Yes [ ] No [ ]

96.11.4.6 Management interface

Item	Feature	Subclause	Value/Comment	Status	Support
MI1	MASTER-SLAVE configuration	96.6.1	Each link configuration will have one PHY as MASTER one PHY configured as SLAVE	M	Yes [ ]

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96.11.4.7 Characteristics of the Link Segment

Item	Feature	Subclause	Value/Comment	Status	Support
LKS1	The characteristic impedance of the cable and any mated MDI connector	96.7.1.1	Be 100 Ω ±10% measured with TDR and rise-time set not slower than 700 ps	M	Yes [ ]
LKS2	The insertion loss when measured with a 100 Ω termination	96.7.1.2	Be less than that contained in Equation (96–6)	M	Yes [ ]
LKS3	The return loss (with 100 Ω reference impedance)	96.7.1.3	Meet or exceed Equation (96–7) for all frequencies from 1 MHz to 66 MHz	M	Yes [ ]
LKS4	Mode conversion LCL and LCTL	96.7.1.4	Meet or exceed the limit defined in Equation (96–8) for all frequencies from 1 MHz to 200 MHz	M	Yes [ ]
LKS5	The PSANEXT defined in 96.7.1.5	96.7.1.5	Meet Equation (96–9)	M	Yes [ ]
LKS6	The PSAACRF defined in 96.7.1.6	96.7.1.6	Meet Equation (96–10)	M	Yes [ ]

96.11.4.8 MDI Requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MDI1	The MDI connector mated with a specified single balanced twisted-pair cable connector	96.8.2	Meet the electrical requirements specified in 96.7.1, except for return loss, and 96.7.2	M	Yes [ ]
MDI2	The MDI return loss without Clause 104 power	96.8.2.1	Meet or exceed Equation (96–11) for all frequencies from 1 MHz to 66 MHz (with 100 Ω reference impedance) at all times when the PHY is transmitting data or control symbols	!POWER :M	Yes [ ] N/A [ ]
MDI3	The MDI return loss with Clause 104 power	96.8.2.1	Meet or exceed Equation (96–12) for all frequencies from 1 MHz to 66 MHz (with 100 Ω reference impedance) at all times when PHY is transmitting data or control symbols.	POWER: M	Yes [ ] N/A [ ]
MDI4	Mode conversion LCL	96.8.2.2	Meet or exceed the limit defined in Equation (96–13) for all frequencies from 1 MHz to 200 MHz	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MDI5	MDI wire pair short circuit	96.8.3	Under all operating conditions withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 96–6, for an indefinite period of time	M	Yes [ ]
MDI6	Operation after short circuit	96.8.3	Resume normal operation	M	Yes [ ]
MDI7	MDI wire pair transients and ESD	96.8.3	Under all operating conditions, withstand without damage high voltage transient noise and ESD per application requirements	M	Yes [ ]

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96.11.4.9 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	All 100BASE-T1 cabling	96.9	Be routed in way to provide maximum protection by the motor vehicle sheet metal and structural components, following SAE J1292, ISO 14229, and ISO 15764	AUTO: M	Yes [ ] N/A[ ]
ES2	Conform to the potential environmental stresses to their mounting locations, as defined in ISO 16750-1, ISO 16750-2, ISO 7637-2-2008, ISO 8820-1, ISO 16750-3, ASTM D4728, ISO 12103-1, ISO 16750-4, IEC 60068-2-1, IEC 60068-2-27, IEC 60068-2-30, IEC 60068-2-38, IEC 60068-2-52, IEC 60068-2-64, IEC 60068-2-78, ISO 16750-5, and ISO 20653	96.9		AUTO: M	Yes [ ] N/A[ ]
ES3	Compliance with applicable local and national codes for the limitation of electromagnetic interference, or as agreed to between the customer and the supplier	96.9		M	Yes [ ]
ES4	Tested according to CISPR 25 test methods defined to measure the PHY's EMC performance	96.9		AUTO: M	Yes [ ] N/A[ ]
ES5	Meet the following motor vehicle EMC requirements: CISPR 25, IEC 61967-1/4, IEC 61000-4-21, ISO 11452, IEC 62132-1/4, IEC 61000-4-21, ISO 10605, IEC 61000-4-2/3, IEC 62215-3, ISO 7637-2/3	96.9		AUTO: M	Yes [ ] N/A[ ]

96.11.4.10 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	100BASE-T1 PHY associated with MII	96.10	Comply with the bit delay constraints of full duplex operation	M	Yes [ ]
DC2	Delay for the transmit path	96.10	Less than 360 ns	M	Yes [ ]
DC3	Delay for the receive path	96.10	Less than 960 ns	M	Yes [ ]

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97. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 1000BASE-T1

97.1 Overview

This clause defines the type 1000BASE-T1 Physical Coding Sublayer (PCS) and type 1000BASE-T1 Physical Medium Attachment (PMA) sublayer. Together, the PCS and PMA sublayers comprise a 1000BASE-T1 Physical Layer device (PHY). Provided in this clause are fully functional and electrical specifications for the type 1000BASE-T1 PCS and PMA.

The 1000BASE-T1 PHY is one of the Gigabit Ethernet family of high-speed full-duplex PHY specifications, capable of operating at 1000 Mb/s. The 1000BASE-T1 PHY is intended to be operated over a single twisted-pair copper cable, referred to as an *automotive link segment* (Type A) or *optional link segment* (Type B), defined in 97.6. The automotive link segment specifications defined in 97.6 may also be used for other applications that have similar link segment requirements. The cabling supporting the operation of the 1000BASE-T1 PHY is defined in terms of performance requirements between the attachment points [Medium Dependent Interface (MDI)], allowing implementers to provide their own cabling to operate the 1000BASE-T1 PHY as long as the normative requirements included in this clause are met.

This clause also specifies an optional Energy-Efficient Ethernet (EEE) capability. A 1000BASE-T1 PHY that supports this capability may enter a Low Power Idle (LPI) mode of operation during periods of low link utilization as described in Clause 78.

97.1.1 Relationship of 1000BASE-T1 to other standards

The relationship between the 1000BASE-T1 PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model are shown in Figure 97–1. The PHY sublayers (shown shaded) in Figure 97–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto-Negotiation for 1000BASE-T1 is defined in Clause 98. GMII is defined in Clause 35.

97.1.2 Operation of 1000BASE-T1

The 1000BASE-T1 PHY operates using full-duplex communications over a single twisted-pair copper cable with an effective rate of 1 Gb/s in each direction simultaneously while meeting the requirements (EMC, temperature, etc.) of automotive and industrial environments. The PHY supports operation on two types of link segments:

a) An automotive link segment supporting up to four in-line connectors using a single twisted-pair copper cable for up to at least 15 m (referred to as *link segment type A*)

b) An optional link segment supporting up to four in-line connectors using a single twisted-pair copper cable for up to at least 40 m to support applications requiring extended physical reach, such as industrial and automation controls and transportation (aircraft, railway, bus and heavy trucks). This link segment is referred to as *link segment type B*.

The 1000BASE-T1 PHY utilizes 3 level Pulse Amplitude Modulation (PAM3) transmitted at a 750 MBd rate. A 15-bit scrambler is used to improve the EMC performance. GMII TX_D, TX_EN, and TX_ER are encoded together using 80B/81B encoding, where 10 cycles of GMII data and control are encoded together in 81 bits to reduce the overhead. To maintain a bit error ratio (BER) of less than or equal to 10^{-10}, the 1000BASE-T1 PHY adds 396 bits of Reed-Solomon forward error correction (RS-FEC) parity to each

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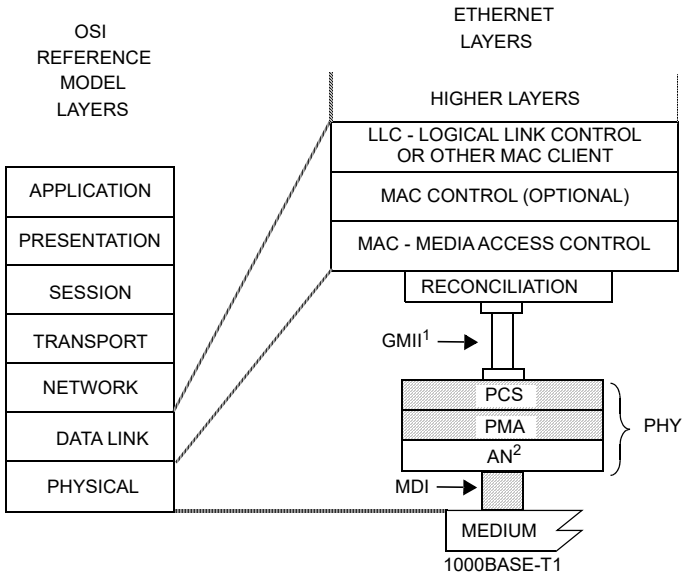
group of 45 80B/81B blocks (containing 450 octets of GMII data). The PAM3 mapping, scrambler, RS-FEC, and 80B/81B encoder/decoder are all contained in the PCS (see 97.3).



MDI = MEDIUM DEPENDENT INTERFACE
GMII = TEN GIGABIT MEDIA INDEPENDENT INTERFACE

NOTE 1—GMII is optional
NOTE 2—Auto-Negotiation is optional

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

Figure 97–1—Relationship of 1000BASE-T1 PHY to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model

Auto-Negotiation (Clause 98) may optionally be used by 1000BASE-T1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for normal operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding. The implementation of the Auto-Negotiation function is optional. If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.

A 1000BASE-T1 PHY shall be capable of operating as MASTER or SLAVE, per runtime configuration. A MASTER PHY uses a local clock to determine the timing of transmitter operations. A SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations. When Auto-Negotiation is used, the MASTER-SLAVE relationship between two devices sharing a link segment is established during Auto-Negotiation (see Clause 98). If Auto-Negotiation is not used, a MASTER-SLAVE relationship shall be established by management or hardware configuration of the PHYs. The MASTER and SLAVE are synchronized by a PHY Link Synchronization function in the PHY (see 97.4.2.6).

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

A 1000BASE-T1 PHY may optionally support Energy-Efficient Ethernet (see Clause 78) and advertise the EEE capability as described in 97.4.2.4.5. The EEE capability is a mechanism by which 1000BASE-T1 PHYs are able to reduce power consumption during periods of low link utilization.

The 1000BASE-T1 PHY may optionally support the 1000BASE-T1 PCS-based Operations, Administration, and Maintenance (OAM). The 1000BASE-T1 OAM is useful for monitoring link operation by exchanging PHY link health status and messages. The 1000BASE-T1 OAM information is exchanged between two

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1000BASE-T1 PHYs out of band. The 1000BASE-T1 OAM is specified in 97.3.8, and the 1000BASE-T1 PHY advertises its 1000BASE-T1 OAM capability as described in 97.4.2.4.5.

The 1000BASE-T1 PMA couples messages from the PCS to the MDI and provides clock recovery, link management, and PHY Control functions. The PMA provides full duplex communications at 750 MBd over the single twisted-pair copper cable. PMA functionality is described in 97.4. The MDI is specified in 97.7.

97.1.2.1 Physical Coding Sublayer (PCS)

The 1000BASE-T1 PCS couples a Gigabit Media Independent Interface (GMII), as described in Clause 35, to a Physical Medium Attachment (PMA) sublayer, described in 97.4, which supports communication over a single twisted-pair copper cable.

The PCS comprises the PCS Reset function, PCS Transmit, and PCS Receive. After completion of the Reset function, the Transmit and Receive functions start immediately and run simultaneously.

The PCS operates in two modes: the data mode and the training mode. In the data mode, the PCS Transmit function data path starts with the GMII interface, where TXD, TX_EN, and TX_ER input data to the PCS every 8 ns (as clocked by GTX_CLK). Data and control from ten GTX_CLK cycles are 80B/81B encoded into an 81-bit “81B block” that encodes every possible combination of data and control (control signals include transmit error propagation, receive error, assert low power idle, and inter-frame signaling, as defined in 35.2.1.6). Each set of 45 80B/81B blocks along with 9 bits of 1000BASE-T1 OAM data (see 97.3.8) is processed by an RS-FEC encoder. The RS-FEC encoder adds 396 RS-FEC parity bits and the resulting 4050 bits (45 80B/81B blocks = 3645 bits, 9 bits of 1000BASE-T1 OAM, and 396 bits of FEC parity bits) are scrambled using a 15-bit side-stream scrambler. The 4050 bits are referred to interchangeably as a *PHY frame* or as a *Reed-Solomon frame*. Each group of 3 bits of the scrambled data is converted to 2 PAM3 symbols by the 3B2T mapper (the 4050 bits in the PHY frame become 2700 PAM3 symbols) and passed to the PMA. PCS transmit functions are described in 97.3.2.2.

In the data mode, the PCS Receive function data path operates in the opposite order as the transmit path. The incoming PAM3 symbols are synchronized to PHY frame boundaries. Within each PHY frame, each two PAM3 symbols are demapped to 3 bits by the 3B2T demapper (the 2700 PAM3 symbols are converted to 4050 bits). The data is then descrambled and passed to the RS-FEC decoder for data validation and correction. Finally, each of the 45 80B/81B blocks is 80B/81B decoded into GMII data or control. The PCS data mode receive is described in 97.3.2.3.

In the training mode (see 97.4.2.4), the PCS transmits and receives PAM2 training sequences to synchronize to the PHY frame, learns the data mode scrambler seed, and exchanges EEE and 1000BASE-T1 OAM capabilities. The training mode uses PAM2 encoding.

97.1.2.2 Physical Medium Attachment (PMA) sublayer

The 1000BASE-T1 PMA transmits/receives symbol streams to/from the PCS onto the single balanced twisted-pair and provides the clock recovery, link monitor, and the 1000BASE-T1 PHY Control function. The PMA provides full duplex communications at 750 MBd.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled following the completion of Auto-Negotiation or PHY Link Synchronization and provides the startup functions required for successful 1000BASE-T1 operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

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The Link Monitor determines the status of the underlying link channel and communicates this status to other functional blocks. A failure of the receive channel causes the data mode operation to stop and Auto-Negotiation or Link Synchronization to restart.

The minimum link segment characteristics, EMC requirements, and test modes are specified in 97.5.

97.1.2.3 EEE capability

A 1000BASE-T1 PHY may optionally support the EEE capability, as described in 78.3. The EEE capability is a mechanism by which 1000BASE-T1 PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter the LPI mode of operation after completing training. Each direction of the full duplex link is able to enter and exit the LPI mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full duplex link is in a period of low utilization. The transition to or from LPI mode shall not cause any MAC frames to be lost or corrupted.

In the transmit direction the transition to the LPI transmit mode begins when the PCS transmit function detects an “Assert Low Power Idle” condition on the GMII in the last 80B/81B block of a PHY frame. At the next PHY frame aligned to the wake window the PCS transmits a sleep signal composed of an entire PHY frame containing only LP_IDLE. The sleep signal indicates to the link partner that the transmit function of the PHY is entering the LPI transmit mode. Immediately after the transmission of the sleep frame, the transmit function of the local PHY enters the LPI transmit mode. While the transmit function is in the LPI mode the PHY may disable data path and control logic to save additional power. Periodically the transmit function of the local PHY transmits refresh frames that may be used by the link partner to update adaptive filters and timing circuits. LPI mode may begin with quiet signaling, a full refresh period, or a wake frame. The quiet-refresh cycle continues until the PCS function detects a condition that is not Assert Low Power Idle on the GMII. This condition signals to the PHY that the LPI transmit mode should end. At the next PHY frame the PCS transmits a wake frame composed of an entire PHY frame containing only Idle. On the next PHY frame normal power mode shall resume.

Support for EEE capability is advertised during Training. See 97.4.2.4.5 for details. Transitions to and from the LPI transmit mode are controlled via GMII signaling. Transitions to and from the LPI receive mode are controlled by the link partner using sleep and wake signaling.

When the 1000BASE-T1 OAM SNR settings indicate that LPI is insufficient to maintain PHY SNR, the PHY may temporarily be forced to exit LPI mode and send idles.

The PCS 80B/81B Transmit state diagram in Figure 97–14 includes additional states for EEE. The PCS 80B/81B Receive state diagram in Figure 97–12 includes additional states for EEE.

97.1.2.4 Link Synchronization

The Link Synchronization function is used when Auto-Negotiation is disabled to synchronize between the MASTER PHY and SLAVE PHY before training starts. Link Synchronization provides a fast and reliable mechanism for the link partner to detect the presence of the other, validate link, and start the timers used by the link monitor. Link Synchronization operates in a half-duplex fashion. Based on timers, the MASTER PHY sends a synchronization sequence for 1 µs. If there is no response from the SLAVE, the MASTER repeats by sending a synchronization sequence every 5 µs. If the slave detects the sequence, it responds with a synchronization sequence for 1 µs (after the MASTER has stopped transmitting). If no other detection happens after the SLAVE response for 4 µs then Link Synchronization is successfully complete, link monitor timers are started, and the PHY Control state machine starts Training. Link synchronization is defined in 97.4.2.6.

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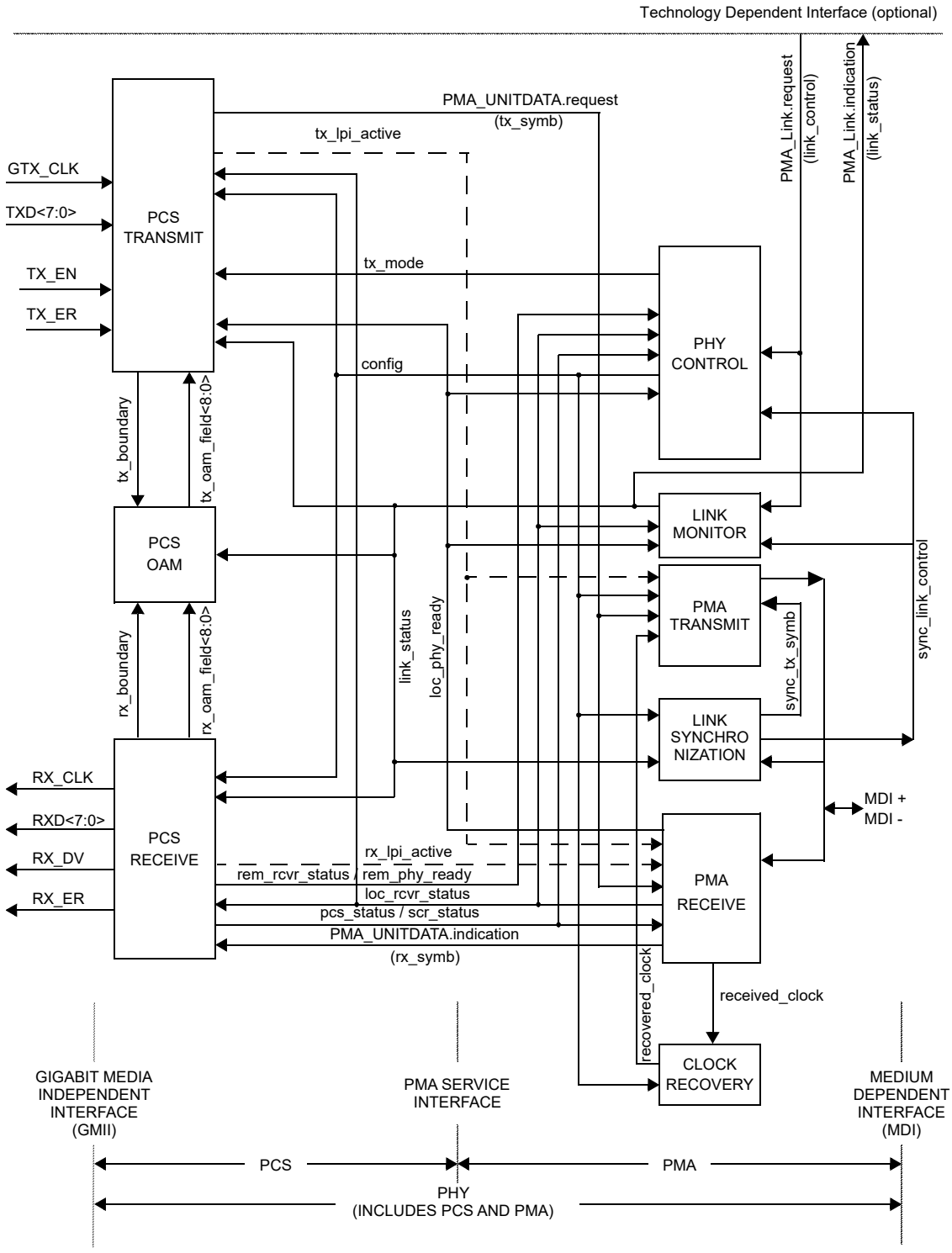

NOTE 1—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

NOTE 2—Signals and functions shown with dashed lines are optional.

Figure 97–2—Functional block diagram

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97.1.3 Signaling

1000BASE-T1 signaling is performed by the PCS generating continuous symbol sequences that the PMA transmits over the single twisted-pair copper cable. The signaling scheme achieves a number of objectives including the following:

a) Algorithmic mapping from TXD<7:0> to PAM3 symbols in the transmit path
b) Algorithmic mapping from PAM3 symbols to RXD<7:0> in the receive path
c) Adding FEC coded data to transmit and validating data using FEC on receive
d) Uncorrelated symbols in the transmitted symbol stream
e) No correlation between symbol streams traveling both directions
f) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining
g) Optionally, ability to signal to the remote PHY that the transmitting PHY is entering the LPI mode or exiting the LPI mode and returning to normal power operation

The PHY may operate in three basic modes: the normal data mode, the training mode, or an optional LPI mode.

In the normal data mode, PCS generates symbols that represent data, control, or idles for transmission by the PMA.

In the training mode, the PCS generates only a PAM2 pattern with periodic embedded data that enables the receiver at the other end to train and synchronize timing, scrambler seeds, and capabilities. The LPI mode is enabled separately in each direction (see LPI signaling in 97.3.5). When transmitting in LPI mode, the PCS generates zero symbols and periodically send a REFRESH pattern to keep the two PHYs synchronized (see 97.3.2.2.15).

97.1.4 Interfaces

All 1000BASE-T1 PHY implementations are compatible at the MDI and at a physically exposed GMII, if made available. Physical implementation of the GMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and GMII (if the GMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the GMII is implemented or not.

97.1.5 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

The values of all components in test circuits shall be accurate to within ± 1% unless otherwise stated.

Default initializations, unless specified, are left to the implementer.

97.2 1000BASE-T1 Service Primitives and Interfaces

1000BASE-T1 transfers data and control information across the following four service interfaces:

a) Gigabit Media Independent Interface (GMII)
b) Technology Dependent Interface

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c) PMA service interface

d) Medium dependent interface (MDI)

The GMII is specified in Clause 35; the Technology Dependent Interface is specified in 98.4. The PMA service interface is defined in 97.2.2, and the MDI is defined in 97.7.3.

97.2.1 Technology Dependent Interface

1000BASE-T1 uses the following service primitives to exchange status indications and control signals across the Technology Dependent Interface as specified in 98.4:

PMA_LINK.request(link_control)

PMA_LINK.indication(link_status)

97.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation or the PHY Link Synchronization algorithm to enable and disable operation of the PMA, as specified in 98.4.2, respectively.

97.2.1.1.1 Semantics of the primitive

PMA_LINK.request(link_control)

The link_control parameter can take on one of the following two values: DISABLE, or ENABLE.

DISABLE	Used by the Auto-Negotiation function to disable the PHY
ENABLE	Used by the Auto-Negotiation to enable the PHY

97.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in 98.4.

97.2.1.1.3 Effect of receipt

This primitive affects the operation of the PMA Link Monitor function as defined in 97.4.2.5, the PMA PHY Control function as defined in 97.4.2.4, and the PMA Receive function defined in 97.4.2.3.

97.2.1.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 98.4.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation functions about the status of the underlying link.

97.2.1.2.1 Semantics of the primitive

PMA_LINK.indication(link_status)

The link_status parameter can take on one of the following two values: FAIL or OK.

FAIL	No valid link established.
OK	The Link Monitor function indicates that a valid 1000BASE-T1 link is established. Reliable reception of signals transmitted from the remote PHY is possible.

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97.2.1.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 97–27.

97.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 98.4.1.

97.2.2 PMA service interface

1000BASE-T1 uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication(tx_mode)
PMA_CONFIG.indication(config)
PMA_UNITDATA.request(tx_symb)
PMA_UNITDATA.indication(rx_symb)
PMA_SCRSTATUS.request(scr_status)
PMA_PCSSTATUS.request(pcs_status)
PMA_RXSTATUS.indication(loc_rcvr_status)
PMA_PHYREADY.indication(loc_phy_ready)
PMA_REMRXSTATUS.request(rem_rcvr_status)
PMA_REMPHYREADY.request(rem_phy_ready)

The use of these primitives is illustrated in Figure 97–3. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 97–3.

EEE-capable PHYs additionally support the following service primitives:

PMA_PCS_RX_LPI_STATUS.request(rx_lpi_active)
PMA_PCS_TX_LPI_STATUS.request(tx_lpi_active)

97.2.2.1 PMA_TXMODE.indication

The transmitter in a 1000BASE-T1 link normally sends over the MDI symbols that represent a GMII data stream with framing, scrambling and encoding of data, control information, or idles.

97.2.2.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following four values of the form:

SEND_NThis value is continuously asserted during transmission of sequences of symbols representing a GMII data stream in the data mode
SEND_IThis value is continuously asserted when transmission of sequences of idle symbols is to take place
SEND_TThis value is continuously asserted in case transmission of sequences of symbols representing the training mode is to take place
SEND_ZThis value is continuously asserted in case transmission of zeros is required

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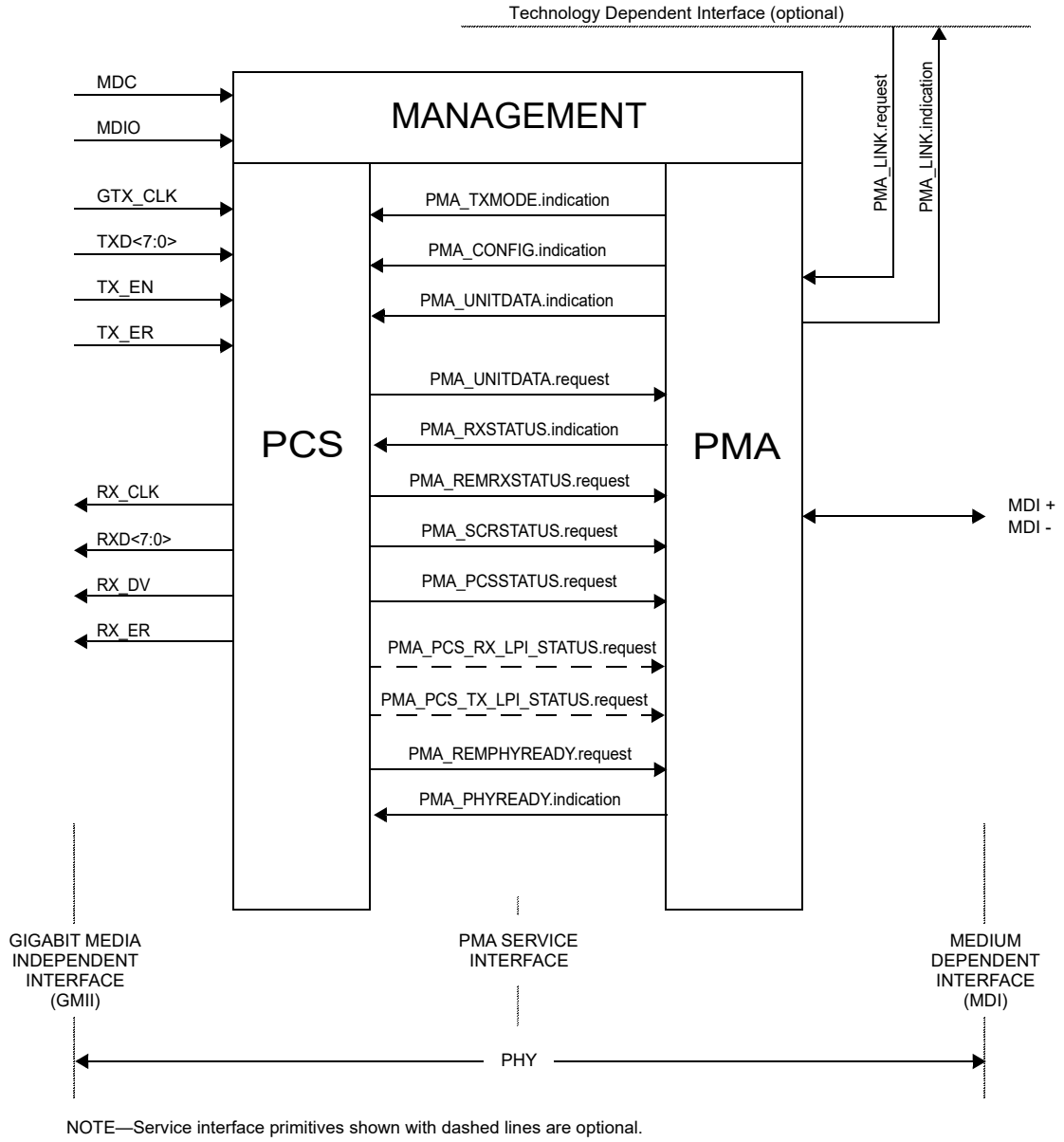

NOTE—Service interface primitives shown with dashed lines are optional.

Figure 97–3—1000BASE-T1 service interfaces

97.2.2.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

97.2.2.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 97.3.2.2.

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97.2.2.2 PMA_CONFIG.indication

Each PHY in a 1000BASE-T1 link is capable of operating as a MASTER PHY and as a SLAVE PHY. If the Auto-Negotiation process is enabled, PMA_CONFIG MASTER-SLAVE configuration is determined during Auto-Negotiation (Clause 98) and the result is provided to the PMA. If the Auto-Negotiation process is not implemented or not enabled, PMA_CONFIG MASTER-SLAVE configuration is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup.

97.2.2.2.1 Semantics of the primitive

PMA_CONFIG.indication(config)

PMA_CONFIG.indication specifies to PCS and PMA Transmit via the parameter config whether the PHY operates as a MASTER PHY or as a SLAVE PHY. The parameter config can take on one of the following two values of the form:

MASTER	This value is continuously asserted when the PHY operates as a MASTER PHY
SLAVE	This value is continuously asserted when the PHY operates as a SLAVE PHY

97.2.2.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in configuration.

97.2.2.2.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter configuration.

97.2.2.3 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 97.3.2.2 to represent GMII data and control streams or other sequences.

97.2.2.3.1 Semantics of the primitive

PMA_UNITDATA.request(tx_symb)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb the value of the symbols to be sent over the MDI. The tx_symb may take on one of the values in the set { –1, 0, 1 }

97.2.2.3.2 When generated

The PCS generates PMA_UNITDATA.request(tx_symb) synchronously with every transmit clock cycle.

97.2.2.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols after processing with optional transmit filtering and other specified PMA Transmit processing.

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97.2.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb parameter from the PMA to the PCS.

97.2.2.4.1 Semantics of the primitive

PMA_UNITDATA.indication(rx_symb)

During reception the PMA_UNITDATA.indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the recovered clock.

97.2.2.4.2 When generated

The PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is 750 MHz, as governed by the recovered clock.

97.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

97.2.2.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the training mode descrambler has achieved synchronization.

97.2.2.5.1 Semantics of the primitive

PMA_SCRSTATUS.request(scr_status)

The scr_status parameter can take on one of the following two values of the form:

OK	The training mode descrambler has achieved synchronization
NOT_OK	The training mode descrambler is not synchronized

97.2.2.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

97.2.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 97.4.2.3 and 97.4.2.4.

97.2.2.6 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in the data mode.

97.2.2.6.1 Semantics of the primitive

PMA_PCSSTATUS.request(pcs_status)

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The pcs_status parameter can take on one of the following two values of the form:

OK	The PCS is operating reliably in the data mode
NOT_OK	The PCS is not operating reliably in the data mode

97.2.2.6.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

97.2.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 97.4.4.1.

97.2.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol stream.

97.2.2.7.1 Semantics of the primitive

PMA_RXSTATUS.indication(loc_rcvr_status)

The loc_rcvr_status parameter can take on one of the following two values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable

97.2.2.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

97.2.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 97–26, 97.3.2.3, 97.4.2.4, and 97.4.5.

97.2.2.8 PMA_PHYREADY.indication

This primitive is generated by PMA Receive to indicate the local PHY is ready or not ready to receive data. The parameter loc_phy_ready is conveyed to the link partner by the PCS as defined in Table 97–1.

97.2.2.8.1 Semantics of the primitive

PMA_PHYREADY.indication(loc_phy_ready)

The loc_phy_ready parameter can take on one of the following two values of the form:

OK	The local PHY is ready to receive data
NOT_OK	The local PHY is not ready to receive data

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97.2.2.8.2 When generated

PMA Receive generates PMA_PHYREADY.indication messages to indicate a change in loc_phy_ready based on loc_rcvr_status and pcs_status values.

97.2.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 97–26 and Figure 97–27.

97.2.2.9 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received in the loc_rcvr_status bit in the InfoField from the remote PHY. The rem_rcvr_status is set to NOT_OK if the PCS has not decoded a valid InfoField from the remote PHY.

97.2.2.9.1 Semantics of the primitive

PMA_REMRXSTATUS.request(rem_rcvr_status)

The rem_rcvr_status parameter can take on one of the following two values of the form:

OK	The receive link for the remote PHY is operating reliably
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected

97.2.2.9.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages to indicate a change in rem_rcvr_status based on the PCS decoding the loc_rcvr_status bit in InfoField messages received from the remote PHY during training.

97.2.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 97–26.

97.2.2.10 PMA_REMPHYREADY.request

This primitive is generated by PCS Receive to indicate whether the remote PHY is ready or not ready to receive data. Its value is received from the link partner by the PCS as defined in Table 97–1.

97.2.2.10.1 Semantics of the primitive

PMA_REMPHYREADY.request(rem_phy_ready)

The rem_phy_ready parameter can take on one of the following two values of the form:

OK	The remote PHY is ready to receive data
NOT_OK	The remote PHY is not ready to receive data

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97.2.2.10.2 When generated

The PCS generates PMA_REMPHYREADY.request messages to indicate a change in rem_phy_ready based on the PCS decoding the control words in Table 97–1 received from the remote PHY.

97.2.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 97–26.

97.2.2.11 PMA_PCS_RX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS receive function to indicate the status of the receive link at the local PHY. The parameter PMA_PCS_RX_LPI_STATUS.request conveys to the PCS transmit and PMA receive functions information regarding whether the receive function is in the LPI receive mode.

97.2.2.11.1 Semantics of the primitive

PMA_PCS_RX_LPI_STATUS.request(rx_lpi_active)

The rx_lpi_active parameter can take on one of the following two values of the form:

true	The receive function is in the LPI receive mode
false	The receive function is not in the LPI receive mode

97.2.2.11.2 When generated

The PCS generates PMA_PCS_RX_LPI_STATUS.request messages to indicate a change in the rx_lpi_active variable as described in 97.3.2.3 and 97.3.6.2.2.

97.2.2.11.3 Effect of receipt

The effect of receipt of this primitive is specified in 97.3.6.4.

97.2.2.12 PMA_PCS_TX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS transmit function to indicate the status of the transmit link at the local PHY. The parameter PMA_PCS_TX_LPI_STATUS.request conveys to the PCS transmit and PMA receive functions information regarding whether the transmit function is in the LPI transmit mode.

97.2.2.12.1 Semantics of the primitive

PMA_PCS_TX_LPI_STATUS.request(tx_lpi_active)

The tx_lpi_active parameter can take on one of the following two values of the form:

true	The transmit function is in the LPI transmit mode
false	The transmit function is not in the LPI transmit mode

97.2.2.12.2 When generated

The PCS generates PMA_PCS_TX_LPI_STATUS.request messages to indicate a change in the tx_lpi_active variable as described in 97.3.5 and 97.3.6.2.2.

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97.2.2.12.3 Effect of receipt

The effect of receipt of this primitive is specified in 97.3.6.4.

97.3 Physical Coding Sublayer (PCS)

97.3.1 PCS service interface (GMII)

The PCS service interface allows the 1000BASE-T1 PCS to transfer information to and from a PCS client. The PCS Interface is defined as the Gigabit Media Independent Interface (GMII) in Clause 35.

97.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 97–4, shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 97–4.

97.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power for the device containing the PMA has not reached the operating state
b) The receipt of a request for reset from the management entity

PCS Reset sets pcs_reset = ON while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

The control and management interface shall be restored to operation within 10 ms from the setting of bit 3.2304.15.

97.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS 80B/81B Transmit state diagram in Figure 97–14 and the PCS Transmit bit ordering in Figure 97–5 and Figure 97–7.

When communicating with the GMII, the PCS uses an octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment to 80B/81B blocks is performed in the PCS. The PMA sublayer operates independently of block and packet boundaries. The PCS provides the functions necessary to map packets between the GMII format and the PMA service interface format.

When the transmit channel is in the data mode, the PCS Transmit process continuously generates 80B/81B blocks based upon the TXD <7:0>, TX_EN and TX_ER signals on the GMII. The subsequent functions of the PCS Transmit process then pack the resulting blocks plus one 1000BASE-T1 OAM symbol, both of which are then processed by a Reed-Solomon (RS-FEC) encoder and subsequently 3B2T mapped into a transmit PHY frame of PAM3 symbols. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive. A symbol period, T, is 4/3 ns.

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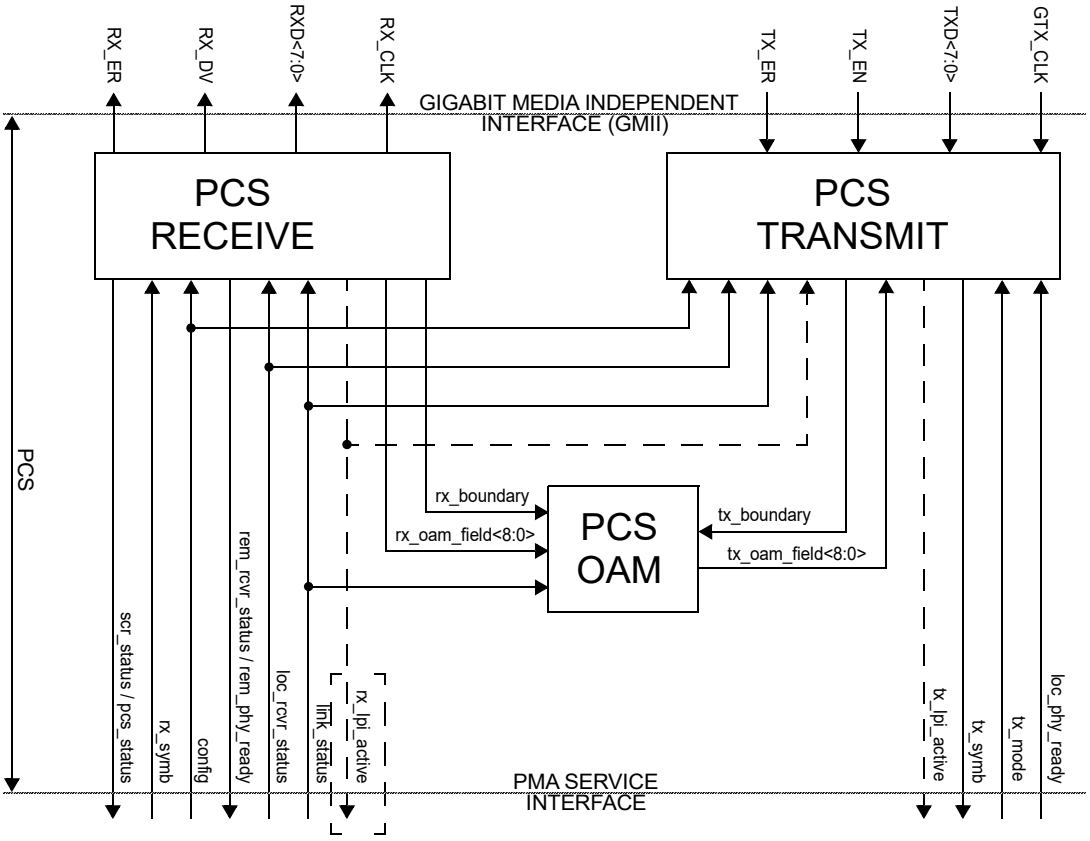

Figure 97–4—PCS reference diagram

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit generates sequences of codes defined in 97.3.4.2 to the PMA via the PMA_UNITDATA.request primitive. These codes are used for training mode and only transmit the values {–1, +1}.

During training mode an InfoField is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner. (See 97.4.2.4.)

In the data mode of operation, the PMA_TXMODE.indication message has the value SEND_N, and the PCS Transmit function uses an 81B-RS coding technique to generate at each symbol period symbols that represent data or control. During transmission, 45 80B/81B blocks shall be aggregated, encoded by a PHY frame encoder, and then scrambled by a PCS scrambler. During data encoding PCS Transmit frames shall be encoded into a sequence of PAM3 symbols and transferred to the PMA.

Dashed rectangles in Figure 97–14 indicate states and state transitions in the transmit process state diagram that are supported by PHYs with the EEE capability. PHYs without the EEE capability do not support these transitions.

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After reaching the data mode of operation, EEE-capable PHYs may enter the LPI transmit mode under the control of the MAC via the GMII. The EEE Transmit state diagram is contained within the PCS Transmit function. The EEE capability is described in 97.3.2.2.15.

97.3.2.2.1 Use of blocks

The PCS maps GMII signals into 81-bit blocks inserted into a PHY frame, and vice versa, using an 81B-RS coding scheme. The PAM2 PMA training frame synchronization allows establishment of PHY frame and 81B boundaries by the PCS Synchronization process. Blocks and PHY frames are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and PHY frames as provided by the rules in 97.3.2.2.2.

97.3.2.2.2 81B-RS transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters. The encoding defined by the transmission code ensures that sufficient information is present in the PHY bit stream to make clock recovery possible at the receiver. The encoding also preserves the likelihood of detecting any PHY frame errors that may occur during transmission and reception of information. In addition, the code enables the receiver to achieve PCS synchronization alignment on the incoming PHY bit stream.

The relationship of block bit positions to GMII, PMA, and other PCS constructs is illustrated in Figure 97–5 for transmit and Figure 97–6 for receive. These figures illustrate the processing of a multiplicity of blocks containing 10 data octets. See 97.3.2.2.5 for information on how blocks containing control characters are mapped.

97.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

97.3.2.2.4 Transmission order

The PCS Transmit bit ordering shall conform to Figure 97–5 and Figure 97–7. Note that these figures show the mapping from GMII to 80B/81B block for a block containing ten data characters. The LSB of the 1000BASE-T1 OAM symbol is transmitted first.

97.3.2.2.5 Block structure

Blocks consist of 81 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain 10 data octets. Control blocks begin with a 5-bit pointer field that indicates the location of the first control code within the block. Bits 0 to 3 of the pointer field points to the next octet that is a control symbol. Bit 4 of the pointer field indicates whether the next control symbol is the final control symbol of the block: 0 = final, 1 = more control symbols. If the first octet in the block is a control character, the pointer field is followed by a 3-bit control code. Otherwise the pointer field is followed by one or more data octets until the position of the first control code. Then the 3-bit control code indicates type of control character. The control code is followed by a 5-bit pointer field to the next control character if the prior pointer field value was greater than 15 (i.e., bit 4 = 1). The pointer field may be followed by a data octet or control code depending on the value of the pointer field. In this way any combination of ten data octets and control characters may be encapsulated within an 80B/81B block.

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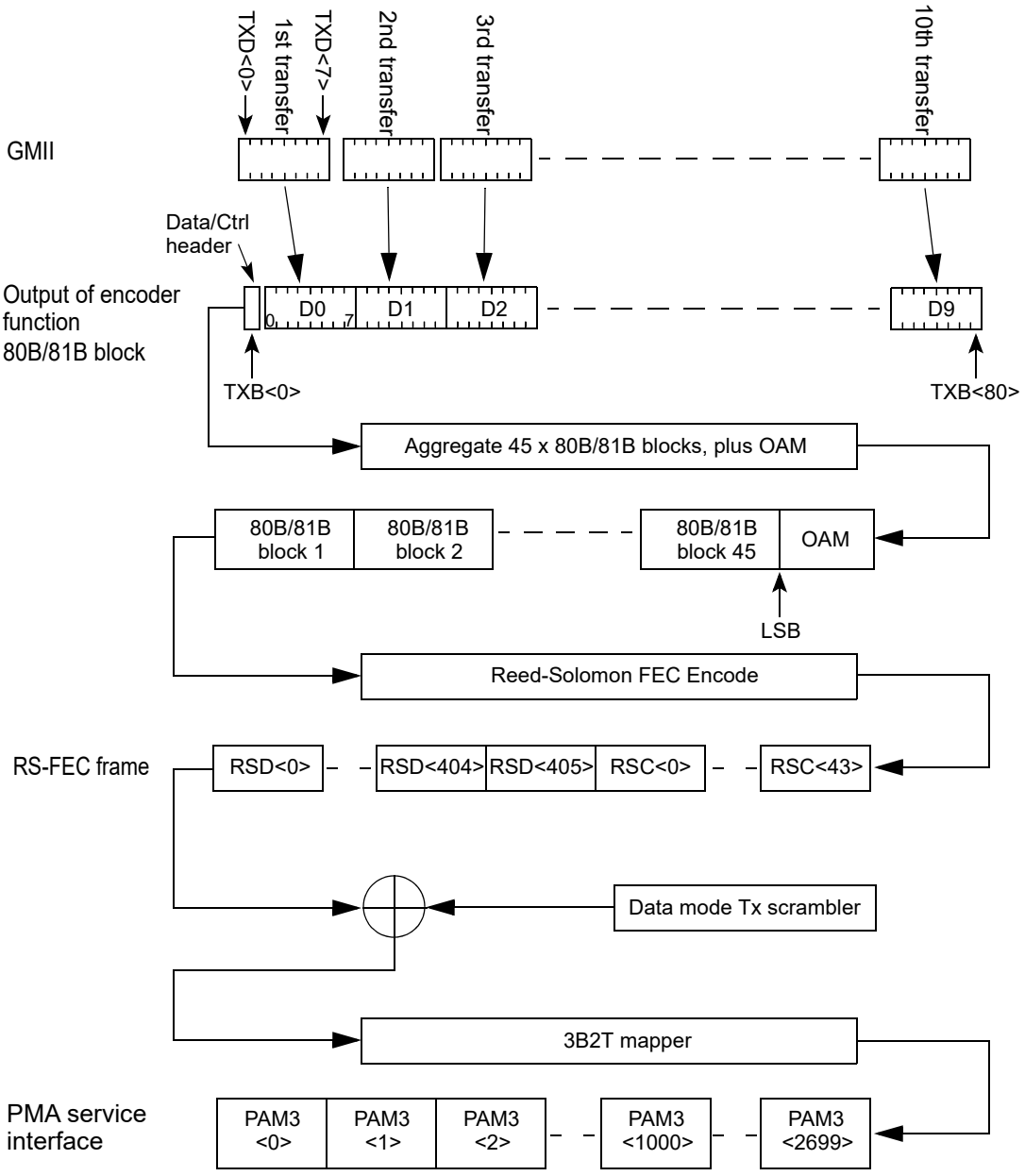

Figure 97–5—PCS Transmit bit ordering

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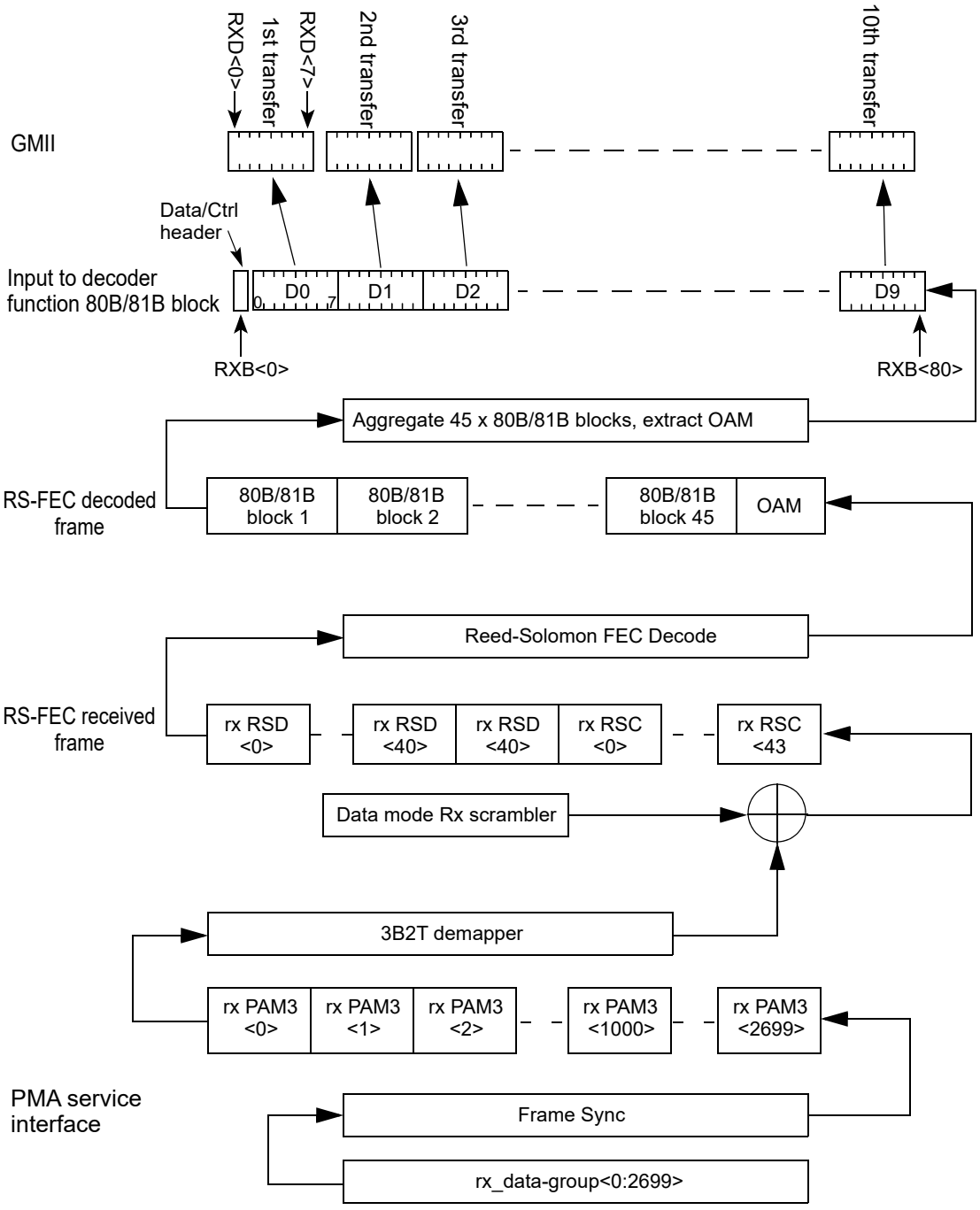

Figure 97–6—PCS Receive bit ordering

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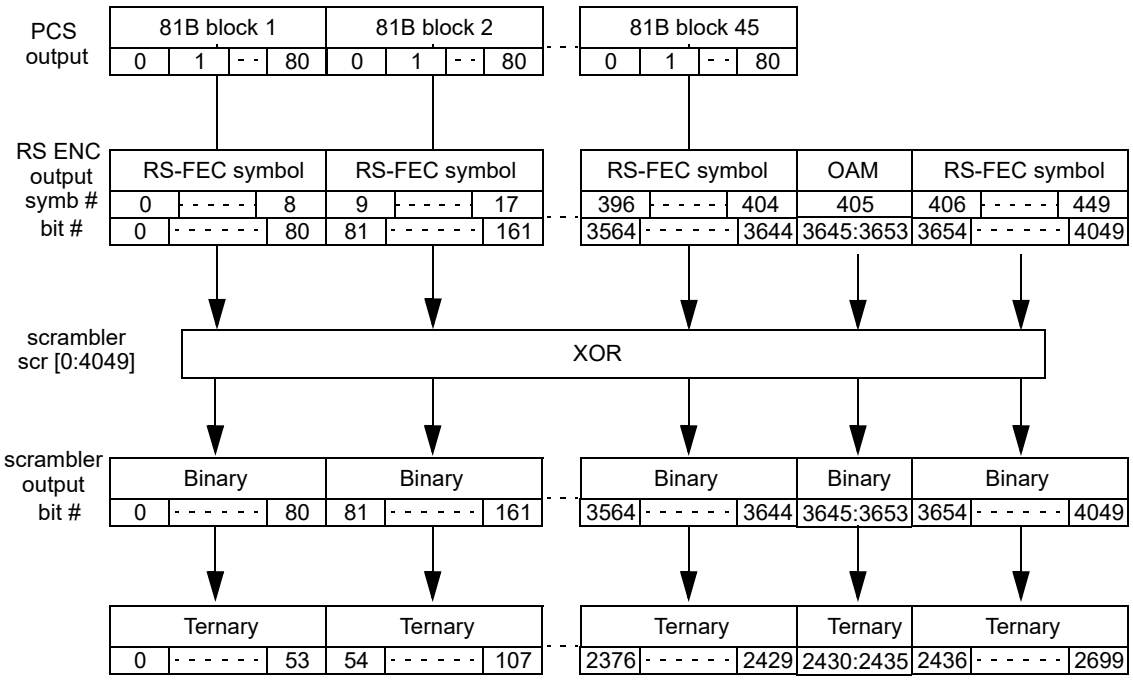

Figure 97–7—PCS detailed transmit bit ordering

The 80B/81B block encoding is defined by the following pseudo-code, where N = 10.

```
N = number of GMII octets encoded into block. Octets numbered n = 0,1,2,…,N-1.
octet 0 is the first one presented on GMII.
TC[n] = 0 if octet n is data octet on GMII, 1 if octet n is control octet on GMII
TC[-1] = 1 by definition
TD[n][0:7] = GMII octet n TXD[0:7] if TC[n] = 0
TD[n][5:7] = 010 – IPG (loc_phy_ready = OK), 101 – LPI, 001 – TX Error, 000 – IPG
(loc_phy_ready = NOT_OK) if TC[n] = 1. TD[n][0:4] is undefined.
B[0:8N] is the 8N+1 block. Bit 0 transmitted first.
OR(n) = Bitwise OR of TC[n:N-1]
NEXT(n)[0:3] = bit position of lowest bit in TC[n:N-1] that is a 1. Bit 3 is MSB.
NEXT(n)[4] = 0 if Bitwise SUM of TC[n:N-1] = 1, else 1

B[0] =              OR(0)
B[8n+1:8n+4] =      TD[n][0:3] – if OR(n) = 0
                    NEXT(n)[0:3] – if OR(n) = 1 AND TC[n-1] = 1
                    TD[n-1][3:6] – if OR(n) = 1 AND TC[n-1] = 0
B[8n+5] =           TD[n][4] – if OR(n) = 0
                    NEXT(n)[4] – if OR(n) = 1 AND TC[n-1] = 1
                    TD[n-1][7] – if OR(n) = 1 AND TC[n-1] = 0
B[8n+6:8n+8] =      TD[n][5:7] – if OR(n) = 0
                    TD[n][5:7] – if OR(n) = 1 AND TC[n] = 1
                    TD[n][0:2] – if OR(n) = 1 AND TC[n] = 0
```

97.3.2.2.6 Control codes

A subset of control characters defined at the GMII are supported by the 1000BASE-T1 PCS. When TX_ER and TX_EN are both asserted, the 1000BASE-T1 PCS conveys an Error symbol in the 80B/81B block code. When TX_EN is not asserted and no other supported control code is present at the GMII, the 1000BASE-T1 PCS conveys a Normal Inter-Frame control code in the 80B/81B block code.

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The control characters and their mappings to 1000BASE-T1 control code and GMII control code are specified in Table 97–1. All GMII and 1000BASE-T1 control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

Table 97–1—GMII control code mapping

Control Code[0:2]	GMII Transmit	GMII Receive
000	Normal Inter-Frame with loc_phy_ready = NOT_OK	Normal Inter-Frame with rem_phy_ready = NOT_OK
001	Transmit Error Propagation	Data Reception Error
010	Normal Inter-Frame with loc_phy_ready = OK	Normal Inter-Frame with rem_phy_ready = OK
101	Assert Low Power Idle	Assert Low Power Idle

The Carrier Extend and Carrier Extend Error, and Reserved transactions, if any occurred, are assigned to Normal inter-frame in the PCS 80B/81B Encoder.

97.3.2.2.7 Idle

Idle (Normal Inter-frame) control characters are transmitted when TX_EN is not asserted and no other supported control code is present at the GMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. Idle characters shall not be added within a MAC frame.

97.3.2.2.8 LP_IDLE

The low power idle control characters (LP_IDLEs) are transmitted when TX_EN is not asserted, TX_ER is asserted, and TXD<7:0> = 0x1. A continuous stream of LPI control characters is used to maintain a link in the LPI transmit mode. Idle control characters are used to transition from the LPI transmit mode to the normal power mode. EEE compliant PHYs respond to the Assert Low Power Idle condition on the GMII using the procedure outlined in 97.1.2.3. LP_IDLE characters may be added or deleted by the PCS to adapt between clock rates. LP_IDLE characters shall not be added within a MAC frame.

Where the GMII and PMA sublayer data rates are not synchronized, the transmit process needs to insert LPI_IDLEs, or delete LPI_IDLEs to adapt between the rates.

If EEE is not supported, then LP_IDLE shall be converted to IDLE.

97.3.2.2.9 Error

The Error control code is sent when TX_ER and TX_EN are both asserted. Error allows physical sublayers such as the PCS to propagate received errors.

97.3.2.2.10 Transmit process

The transmit process generates blocks based upon the TXD<7:0>, TX_EN, and TX_ER signals received from the GMII. Ten GMII data transfers are encoded into each block. It takes 2700 PMA_UNITDATA transfers to send a PHY frame of data. Where the GMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, or delete idles to adapt between the rates.

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The transmit process generates blocks as specified in the transmit process state diagram. The contents of each block are contained in a vector tx_coded<80:0>, which is aggregated with 45 80B/81B blocks and 1000BASE-T1 OAM, then passed to the RS-FEC Encoder and then finally passed to the scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

97.3.2.2.11 RS-FEC encoder

The 1000BASE-T1 PCS shall encode the transmitted data stream using Reed-Solomon code (450,406). The RS-FEC encoder shall follow the bit order described in 97.3.2.2.3 where the LSB is the first bit into the RS-FEC encoder and the first transmitted bit.

The FEC code used for 1000BASE-T1 links is a shortened Reed-Solomon (450,406) code over the Galois Field of GF(2^9)—a code operating on 9-bit symbols, as shown in Figure 97–8. The code encodes 406 information symbols and adds 44 parity symbols, enabling correction of up to 22 symbol errors. The code is systematic, meaning that the information symbols are not disturbed in any way in the encoder and the parity symbols are added separately to each block.

The code is based on the generating polynomial shown in Equation (97–1).

$$G(Z) = \prod_{i=0}^{43} (Z - \alpha^i) = A_{44}Z^{44} + A_{43}Z^{43} + \ldots + A_0Z^0 \quad (97–1)$$

where

α is a root of the binary primitive polynomial $x^9 + x^4 + 1$ and is represented as 0x002
A is a series representing the resulting polynomial coefficients of $G(Z)$, (A_{44} is equal to 0x001)
Z corresponds to an 9-bit GF(2^9) symbol
x corresponds to a bit position in a GF(2^9) symbol

The parity calculation shall produce the same result as the shift register implementation shown in Figure 97–8. Before calculation begins, the shift register shall be initialized to zero. The contents of the shift register are transmitted without inversion.

An FEC parity vector is represented by Equation (97–2).

$$P(Z) = D(Z) \bmod G(Z) \quad (97–2)$$

where

$D(Z)$ is the data vector $D(Z) = D_{405}Z^{449} + D_{404}Z^{448} + \ldots + D_0Z^{44}$. D_{405} is the first 9-bit data symbol and D_0 is the last

$P(Z)$ is the parity vector $P(Z) = P_{43}Z^{43} + P_{42}Z^{42} \ldots + P_0Z^0$. P_{43} is the first 9-bit parity symbol and P_0 is the last

A data symbol (d_8, d_7, ..., d_1, d_0) is identified with the element: $d_8\alpha^8 + d_7\alpha^7 + ... + d_1\alpha^1 + d_0$ in GF(2^9), the finite field with 2^9 elements.

The d_0 is identified as the LSB and d_8 is identified as the MSB for all symbols.

The resulting payload of scrambled 45 80B/81B blocks, followed by the 1000BASE-T1 OAM symbol results in a total payload of 3654 bits. The resulting PHY frame size is 450 9-bit symbols, a total of 4050 bits. Figure 97–7 shows the bit mapping between PCS and FEC.

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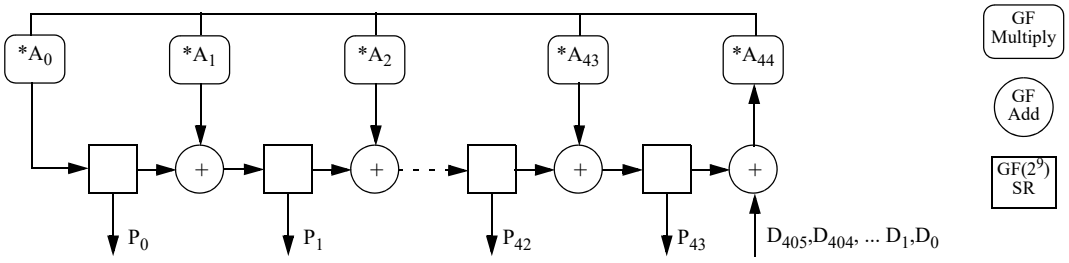


Figure 97–8—Circuit for generating FEC parity vector

97.3.2.2.12 PCS scrambler

The PCS Transmit function employs side-stream scrambling. The scrambler for the MASTER shall produce the same result as the implementation shown in Figure 97–9. This implements the scrambler polynomial as shown in Equation (97–3):[169]

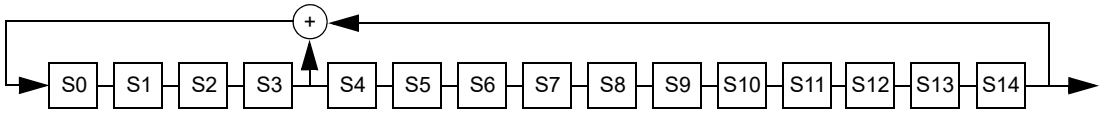
$$G(x) = 1 + x^4 + x^{15} \tag{97–3}$$

The scrambler for the SLAVE shall produce the same result as the implementation shown in Figure 97–9. This implements the scrambler polynomial as shown in Equation (97–4):

$$G(x) = 1 + x^{11} + x^{15} \tag{97–4}$$

The initial seed values for the MASTER and SLAVE scramblers are left to the implementer. The seed values shall be non-zero and transmitted during the InfoField exchange. (See 97.4.2.4.5). The scrambler is run continuously on all PHY frame output bits.

PCS scrambler employed by the MASTER



PCS scrambler employed by the SLAVE

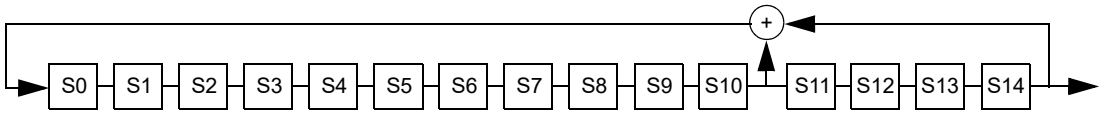


Figure 97–9—MASTER and SLAVE PCS scramblers

97.3.2.2.13 3B2T to PAM3

The 3B2T mapper generates 2700 PAM3 symbols per PHY frame that are sent to the PMA via PMA_UNITDATA.request. Every 9-bit symbol is divided into three 3-bit groups with the LSB bits as the first group. Each 3-bit group is then mapped by the 3B2T into 2 PAM3 symbols. The mapping of 3B2T to PAM3 is illustrated in Table 97–2. B[0] is the LSB and T[0] is the first PAM3 symbol transmitted..

[169]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (97–3). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.

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Table 97–2—3B2T Mapping to PAM3

B[2], B[1], B[0]	T[1], T[0]
000	–1,–1
001	0,–1
010	–1,0
011	–1,+1
100	+1,0
101	+1,–1
110	+1,+1
111	0,+1

97.3.2.2.14 81B-RS framer

The 81B-RS framer adapts between the 81-bit width of the 80B/81B blocks and the PAM3 input to the PMA. When the transmit channel is operating in the data mode, the 81B-RS sends one PAM3 symbol of transmit data at a time via PMA_UNITDATA.request primitives. The PMA_UNITDATA.request primitives are fully packed with bits.

97.3.2.2.15 EEE capability

The optional 1000BASE-T1 EEE capability allows compliant PHYs to transition to an LPI mode of operation when link utilization is low. EEE compliant PHYs shall implement the transmit state diagram including the EEE portion, noted by dotted lines in Figure 97–14, within the PCS.

When there is an Assert Low Power Idle while in the SEND_DATA state the PHY transmits the sleep signal to indicate to the link partner that it is transitioning to the SEND_LPI state. The sleep signal is one PHY frame composed entirely of LP_IDLE characters. If the LP_IDLE character fills the entire last 80B/81B block then the sleep signal is the next PHY frame. The PHY shall transmit no PHY frames partially filled with LP_IDLES.

Following the transmission of the sleep signal, quiet-refresh signaling begins, as described in 97.3.5.

While the PMA asserts SEND_N, the lpi_tx_mode variable shall control the transmit signal through the PMA_UNITDATA.request primitive described as follows:

- When the PMA_TXMODE.indication message does not have the value of SEND_N, the lpi_tx_mode variable is ignored
- When the lpi_tx_mode variable takes the value NORMAL the PCS passes coded data to the PMA via the PMA_UNITDATA.request primitive
- When the lpi_tx_mode variable takes the value QUIET the PCS passes zeros to the PMA through the PMA_UNITDATA.request primitive
- When the lpi_tx_mode variable takes the value REFRESH, the PCS passes zero data encoded through PCS data path to the PMA via the PMA_UNITDATA.request primitive

The quiet-refresh cycle is repeated until Assert Low Power Idle is not detected at the GMII (indicating that the local system is requesting a transition back to the normal power mode) or until an 1000BASE-T1 OAM

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message with SNR<1:0> set to 01 is transmitted to or received from the link partner (indicating that the LPI refresh is insufficient to maintain the SNR). At the next wake frame window the PCS transmits a wake frame composed of an entire PHY frame containing only Idle. The wake frame shall be sent only during alternating PHY frame counts.

The wake signal occurs at the beginning of every second PHY frame boundary, and the maximum duration of the PHY wake time is 10.8 μs (lpi_wake_timer = T_{w_phy} as defined by Clause 78).

97.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 80B/81B receive state diagram in Figure 97–12 and the PCS Receive bit ordering in Figure 97–6 including compliance with the associated state variables as specified in 97.3.6.

The PCS Receive function accepts received symbols provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the PMA training alignment to correctly align the 81B-RS frames. The received 81B-RS frames are decoded with error correction; the framing is checked; and the 80B/81B blocks are converted to 10 data octets to obtain the signals RXD<7:0>, RX_DV, and RX_ER for transmission to the GMII.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the descrambler state by setting the parameter scr_status to OK.

When the PCS Synchronization process has obtained synchronization, the PHY frame error rate (RFER) monitor process monitors the signal quality asserting hi_rfer if excessive PHY frame errors are detected (RS parity error). If 40 consecutive PHY frame errors are detected, the block_lock flag is de-asserted. When block_lock is asserted and hi_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD<7:0>, RX_DV and RX_ER for transmission to the GMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication(loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.request primitive. It attains PHY frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training sequence includes 1 bit pattern every 180 PAM2 symbols, which is aligned with the PCS partial PHY frame boundary, as well as an InfoField, which is inserted in the 15th PCS partial PHY frame. When the PCS Synchronization process is synchronized to the PHY frame boundary using this pattern, block_lock is asserted. One partial PHY frame codeword is defined to be 1/15 of a PHY frame. Fifteen partial PHY frames concatenated back to back form one PHY frame. The start of the first partial PHY frame coincides with the start of the PHY frame.

PHYs with the EEE capability support transition to the LPI mode when the PHY has successfully completed training. Transitions to and from the LPI mode are allowed to occur independently in the transmit and receive functions. The PCS receive function is responsible for detecting transitions to and from the LPI receive mode and indicating these transitions using signals defined in 97.3.6.

The link partner signals a transition to the LPI mode of operation by transmitting one PHY frame composed entirely of 80B/81B blocks of LP_IDLES. When blocks of LP_IDLES are detected at the output of the 80B/81B decoder, rx_lpi_active is asserted by the PCS receive function and the LPI character is continuously asserted at the receive GMII. After the sleep frame the link partner begins transmitting zeros, and it is recommended that the receiver power down receive circuits to reduce power consumption. The receive function uses PHY frame counters to maintain synchronization with the remote PHY and receives periodic refresh signals that are used to update coefficients, so that the integrity of adaptive filters and timing

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loops in the PMA is maintained. LPI signaling is defined in 97.3.5. The quiet-refresh cycle continues until the PHY detects the wake frame. The PHY receive function sends Idles to the GMII for the remainder of the wake frame and then resumes normal power mode operation.

97.3.2.3.1 Frame and block synchronization

When operating in the data mode, the receiving PCS shall form a PAM3 stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from rx_data<0> to rx_data<2699> (see Figure 97–6). It obtains block lock to the PHY frames during the PAM2 training pattern using synchronization bits provided in the training sequence.

97.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<7:0> to the GMII. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial per Equation (97–4) and the SLAVE PHY shall employ the receiver descrambler generator polynomial per Equation (97–3).

97.3.2.3.3 Valid and invalid blocks

An 80B/81B block is invalid if any of the following conditions exists:

a) The block contains an invalid pointer
b) Any control character contains a value not in Table 97–1
c) The PHY frame containing this 80B/81B block is uncorrectable

Invalid blocks are replaced with Error.

97.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel and remote receiver. When the transmit PCS is operating in test-pattern mode it shall transmit continuously as illustrated in Figure 97–5, with the input to the RS-FEC encoder set to zero and the initial condition of the scrambler set to any non-zero value. This has the same effect as setting the input to the scrambler to zero. When the receiver PCS is operating in test-pattern mode it shall receive continuously as illustrated in Figure 97–6. The output of the received descrambled values should be zero. Any nonzero values correspond to receiver bit errors. The output of the RS-FEC decoder should also be zero, however there is the possibility that the RS-FEC decoder may have corrected some errors. This mode is further described as test mode 7 in 97.5.2.

97.3.4 PMA training side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indication message assumes the value MASTER, PCS Transmit shall employ Equation (97–5)

$$g_M(x) = 1 + x^{13} + x^{33} \quad (97–5)$$

as transmitter side-stream scrambler generator polynomial. If the PMA_CONFIG.indication message assumes the value of SLAVE, PCS Transmit shall employ Equation (97–6)

$$g_S(x) = 1 + x^{20} + x^{33} \quad (97–6)$$

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as transmitter side-stream scrambler generator polynomial. An implementation of MASTER and SLAVE PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 97–9. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

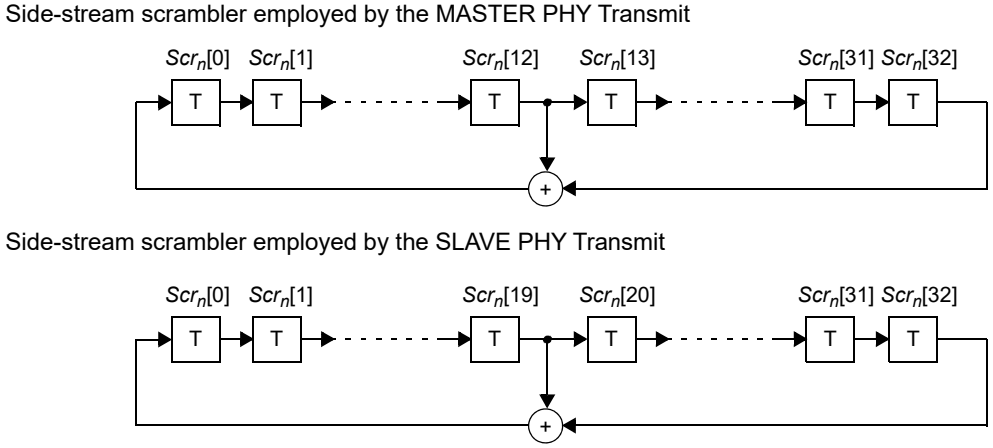

Figure 97–10—Realization of side-stream scramblers by linear feedback shift registers

97.3.4.1 Generation of S_n

During PMA training, the training pattern is embedded with indicators to establish alignment to the RS-FEC block and the 15 partial PHY frames that comprise the block. The last partial PHY frame is embedded with an information field used to exchange messages between link partners. PMA training signal encoding is based on the generation, at time n, of the bit S_n. The first bit is inverted in the first 14 partial PHY frames of each RS-FEC block. The first 96 bits of the 15th partial PHY frame is XORed with the contents of the InfoField. Each partial PHY frame is 180 bits long, beginning at S_n where (n mod 180) = 0. See Equation (97–7).

$$S_n = \begin{cases} Scr_n[0] \oplus InfoField_{(n \bmod 180)} & 2520 \le (n \bmod 2700) \le 2615 \\ Scr_n[0] \oplus 1 & \text{else if } (n \bmod 180) = 0 \\ Scr_n[0] & \text{otherwise} \end{cases} \quad (97\text{–}7)$$

97.3.4.2 Generation of symbol T_n

The bit S_n is mapped to the transmit symbol T_n as follows: if $S_n = 0$ then $T_n = +1$, if $S_n = 1$ then $T_n = -1$.

97.3.4.3 PMA training mode descrambler polynomials

The PHY shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. For side-stream descrambling, the MASTER PHY employs the receiver descrambler generator polynomial per Equation (97–6) and the SLAVE PHY employs the receiver descrambler generator polynomial per Equation (97–5).

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97.3.5 LPI signaling

PHYs with EEE capability have transmit and receive functions that can enter and leave the LPI mode independently. The PHY can transition to the LPI mode when the PHY has successfully completed training. The transmit function of the PHY initiates a transition to the LPI transmit mode when it generates a sleep signal composed of 80B/81B blocks containing only LPI control characters, as described in 97.3.2.2.15. When the transmitter begins to send the sleep signal, it asserts tx_lpi_active and the transmit function enters the LPI transmit mode.

Within the LPI mode PHYs use a repeating quiet-refresh cycle (see Figure 97–11). The first part of this cycle is known as the *quiet period* and lasts for a time lpi_quiet_time equal to 354 partial PHY frame periods. The quiet period is defined in 97.3.5.2. The second part of this cycle is known as the *refresh period* and lasts for a time lpi_refresh_time equal to 6 partial PHY frame periods. The refresh period is defined in 97.3.5.3. A cycle composed of one quiet period and one refresh period is known as an LPI cycle and lasts for an lpi_qr_time equal to 24 × 15 = 360 partial PHY frame periods.

lpi_offset, lpi_quiet_time, lpi_refresh_time, and lpi_qr_time are timing parameters that are integer multiples of the partial PHY frame period. lpi_offset is a fixed value equal to lpi_qr_time/2 + 15. It is used to ensure refresh signals and wake start times are appropriately offset by the link partners.

PHYs begin the transition from the LPI receive mode when they detect the wake frame.

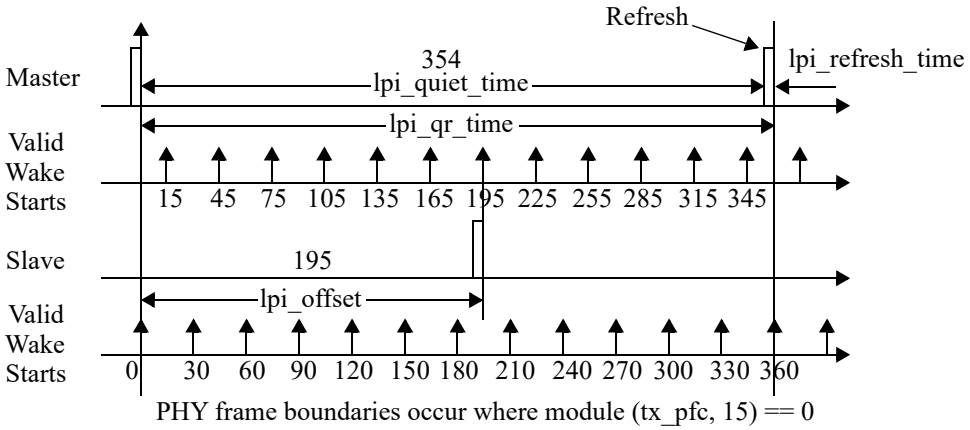

Figure 97–11—LPI signal timing

97.3.5.1 LPI Synchronization

To maximize power savings, maintain link integrity, and ensure interoperability, EEE-capable PHYs shall synchronize refresh intervals during the LPI mode. The quiet-refresh cycle is established from the Master partial PHY frame Count (PFC24) during PMA Training. At the MASTER, partial PHY frame zero and all multiples of 360 partial PHY frames thereafter denote the start of the cycle.

An EEE-capable PHY in SLAVE mode is responsible for synchronizing its partial PHY frame count to the MASTER's partial PHY frame count during link up. The SLAVE shall ensure that its partial PHY frame count is synchronized to the MASTER's partial PHY frames within 1 partial PHY frame. The start of the SLAVE quiet-refresh cycle is delayed from the MASTER by 13 PHY frames (195 partial PHY frames). This offset ensures that the MASTER and SLAVE wake/sense windows are offset from each other and that the refresh periods are nearly a half cycle offset.

Following the transition to PAM3, the PCS continues to count transmitted partial PHY frames (tx_pfc), and uses the counter to generate refresh and wake control signals for the transmit functions.

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Wake frames may be sent at the beginning of every second PHY frame boundary starting at the beginning of the refresh PHY frame. This sets wake_period to 30 partial PHY frames. The MASTER and SLAVE allowable wake positions do not overlap. The wake frame may start in the same PHY frame as a planned refresh and obviate this refresh.

The MASTER and SLAVE shall derive the tx_refresh_active and tx_wake_start signals from the transmitted partial PHY frames (tx_pfc) as shown in Table 97–3 and Table 97–4.

Table 97–3—Synchronization logic derived from SLAVE signal partial PHY frame count

Slave-side Variable	u = tx_pfc
tx_refresh_active=true	lpi_offset – lpi_refresh_time ≤ mod(u, lpi_qr_time) < lpi_offset
tx_wake_start=true	mod(u, wake_period) = 0

Table 97–4—Synchronization logic derived from MASTER signal partial PHY frame count

Master-side variable	v = tx_pfc
tx_refresh_active=true	mod(v, lpi_qr_time) ≥ lpi_quiet_time
tx_wake_start=true	mod(v, wake_period) = wake_period/2

97.3.5.2 Quiet period signaling

During the quiet period the transmitter shall put PAM3 symbol zero on to the MDI. During the quiet period the transmitter may be turned off to save power.

97.3.5.3 Refresh period signaling

During the LPI mode 1000BASE-T1 PHYs use staggered, out-of-phase refresh signaling to maximize power savings. PAM3 refresh symbols are generated from the output of the data mode PCS side-stream scrambler polynomials described in 97.3.2.2.12 with PCS transmit data masked to zero. The scramblers run continuously regardless of the transmit mode. The refresh occupies the last 6 partial PHY frames of where the PHY frame would occur if it were transmitted.

The 1000BASE-T1 OAM symbols and the RS parity symbols are XORed with the scrambler stream at the same relative position to the RS boundaries as they occupy during normal mode. The parity is generated using Equation (97–2) with D_{405} ... $D_1 = 0$ and D_0 = OAM.

97.3.6 Detailed functions and state diagrams

97.3.6.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of constants, variables, functions, counters, and messages. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

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97.3.6.2 State diagram parameters

97.3.6.2.1 Constants

EBLOCK_R<99:0>
TYPE: bit vector
100-bit vector to be sent to the GMII containing symbol errors in all 10 character locations.

IBLOCK_R<99:0>
TYPE: bit vector
100-bit vector to be sent to the GMII containing idles in all 10 character locations.

IBLOCK_T<99:0>
TYPE: bit vector
100-bit vector to be sent to the encoder containing idles in all 10 character locations.

LPBLOCK_R<99:0>
TYPE: bit vector
100-bit vector to be sent to the GMII containing LP_IDLEs in all 10 character locations.

LPBLOCK_T<99:0>
TYPE: bit vector
100-bit vector to be sent to the encoder containing LP_IDLEs in all 10 character locations.

RFER_CNT_LIMIT
TYPE: Integer
VALUE: 16
Number of Reed-Solomon frames with uncorrectable errors.

RFRX_CNT_LIMIT
TYPE: Integer
VALUE: 88
Number of Reed-Solomon frames received over bit error rate interval.

ZBLOCK_T<80:0>
TYPE: bit vector
81-bit vector containing all zero bits.

97.3.6.2.2 Variables

block_lock
Boolean variable that is set true when receiver acquires block delineation.

hi_rfer
Boolean variable that is asserted true when the rfer_cnt reaches RFER_CNT_LIMIT indicating a bit error ratio > 4×10^{-4}.

pcs_reset
When this variable is set to ON, all PCS functions are reset. Otherwise, this variable holds the value of OFF. This variable is set by the PCS Reset function.

rx_coded<81:0>
Vector containing the input to the 80B/81B decoder including a block valid flag. The format for

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rx_coded<80:0> is shown in Figure 97–6. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<80>. rx_coded<81> (not shown in the figure) is set to 1 if all parity checks of the Reed-Solomon frame are satisfied, otherwise it is set to 0.

rf_valid

Boolean indication that is set true if received Reed-Solomon frame is valid. The frame is valid if all parity checks of the coded bits are satisfied.

rx_lpi_active

This variable is set true upon detection of LP_IDLE. Set false upon detection of a wake frame.

rx_raw<99:0>

Vector containing 10 successive GMII output transfers. Each transfer is numbered from 0 to 9 with the first transfer numbered as the 0th transfer. The nth GMII transfer is labeled as RX_DV[n], RX_ER[n], RXD[n]<7:0>.
For n = 0 to 9, RX_DV[n] = rx_raw<10n>, RX_ER[n] = rx_raw<10n+1>,
RXD[n]<7:0> = rx_raw<10n+9:10n+2>

rx_wake_frame_complete

This variable is set true at end of WAKE PHY frame, otherwise false.

tx_coded<80:0>

Vector containing the output from the 80B/81B encoder. The format for this vector is shown in Figure 97–5. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<80>.

tx_data_mode

Set true when tx_mode = SEND_N, otherwise false.

tx_lpi_active

This variable is set false at the next wake frame window if any of the following conditions is true:

— a non-LP_IDLE is detected on GMII in any block

— the PHY receives SNR<1:0> set to 01 by its link partner

— the PHY transmits SNR<1:0> set to 01 to its link partner as defined in 97.3.8.2.14

This variable is set true on next PHY frame if all of the following conditions are true:

— an LP_IDLE detected on GMII during the entire last 80B/81B block

— the PHY does not receive SNR<1:0> set to 01 by its link partner

— the PHY does not transmit SNR<1:0> set to 01 to its link partner as defined in 97.3.8.2.14

tx_raw<99:0>

Vector containing 10 successive GMII transfers. Each transfer is numbered from 0 to 9 with the first transfer numbered as the 0th transfer. The nth GMII transfer is labeled as TX_EN[n], TX_ER[n], TXD[n]<7:0>.
For n = 0 to 9, tx_raw<10n> = TX_EN[n], tx_raw<10n+1> = TX_ER[n], tx_raw<10n+9:10n+2> = TXD[n]<7:0>

tx_sleep_frame_complete

This variable is set to true when PHY is transitioning to the LPI mode and the sleep signal transmission is completed. This variable is set to false when the PHY is transitioning out of the LPI mode.

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tx_wake_frame_complete
: This variable is set to true at the end of a complete wake frame. This variable is set to false otherwise.

lpi_tx_mode
: A variable indicating the signaling to be used from the PCS to the PMA across the PMA_UNITDATA.request(tx_symb) interface.
lpi_tx_mode controls tx_symb only when tx_mode is set to SEND_N.
The variable is set to NORMAL when !tx_lpi_active, indicating that the PCS is in the normal power mode of operation.
The variable is set to REFRESH when (tx_lpi_active * tx_refresh active).
The variable is set to QUIET when (tx_lpi_active * !tx_refresh active).

rx_aggregate
: This variable is set to true when nine aligned 9-bit Reed-Solomon symbols are aggregated in rx_coded. This variable is asserted even when the receiver is in low power idle mode at the time when the nine 9-bit RS-FEC symbols would be aggregated in rx_coded if the receiver was operating in non-lpi mode. This variable is set to false otherwise.

rx_frame
: This variable is set to true when a full Reed-Solomon frame has been decoded and the variable rf_valid is updated. This variable is set to false otherwise.

tx_aggregate
: This variable is set to true when 10 GMII transfers are aggregated in tx_raw<99:0>. This variable is set to false otherwise.

97.3.6.2.3 Functions

DECODE(rx_coded<81:0>)
: In the PCS Receive process, this function takes as its argument 82-bit rx_coded<81:0> from the Reed-Solomon decoder and descrambler. If rx_coded<81> = 1 then the decoder decodes the 81B-Reed-Solomon bit vector rx_coded<80:0> returning a vector rx_raw<99:0>, which is sent to the GMII. The DECODE function shall decode the block based on code specified in 97.3.2.2.2. If rx_coded<81> = 0 then the decoder returns EBLOCK_R.

ENCODE(tx_raw<99:0>)
: Encodes the 100-bit vector received from the GMII, returning 81-bit vector tx_coded. The ENCODE function shall encode the block as specified in 97.3.2.2.2. The ENCODE function shall only encode LPI_IDLE while in the SEND_LPI state. Otherwise LPI_IDLE is converted to Idle in the ENCODE function.

97.3.6.2.4 Counters

rfer_cnt
: Count up to a maximum of RFER_CNT_LIMIT of the number of invalid Reed-Solomon frames within the current RFRX_CNT_LIMIT Reed-Solomon frame period.

rfrx_cnt
: Count number Reed-Solomon frames received during current period.

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97.3.6.3 Messages

PCS_status
: Indicates whether the PCS is in a fully operational state. (See 97.3.7.1.)

PMA_UNITDATA.indication(rx_symb)
: A signal sent by PMA Receive indicating that a PAM3 symbol is available in rx_symb.

PMA_UNITDATA.request(tx_symb)
: A signal sent to PMA Transmit indicating that a PAM3 symbol is available in tx_symb.

97.3.6.4 State diagrams

The RFER Monitor state diagram shown in Figure 97–13 monitors the received signal for high PHY frame error ratio. The 80B/81B Transmit state diagram shown in Figure 97–14 controls the encoding of 81B transmitted blocks. It makes exactly one transition for each 81B transmit block processed. The 80B/81B Receive state diagram shown in Figure 97–12 controls the decoding of 81B received blocks. It makes exactly one transition for each receive block processed. The PCS shall perform the functions of PCS Receive, RFER monitor, and PCS Transmit, as specified in Figure 97–12, Figure 97–13, and Figure 97–14, respectively.

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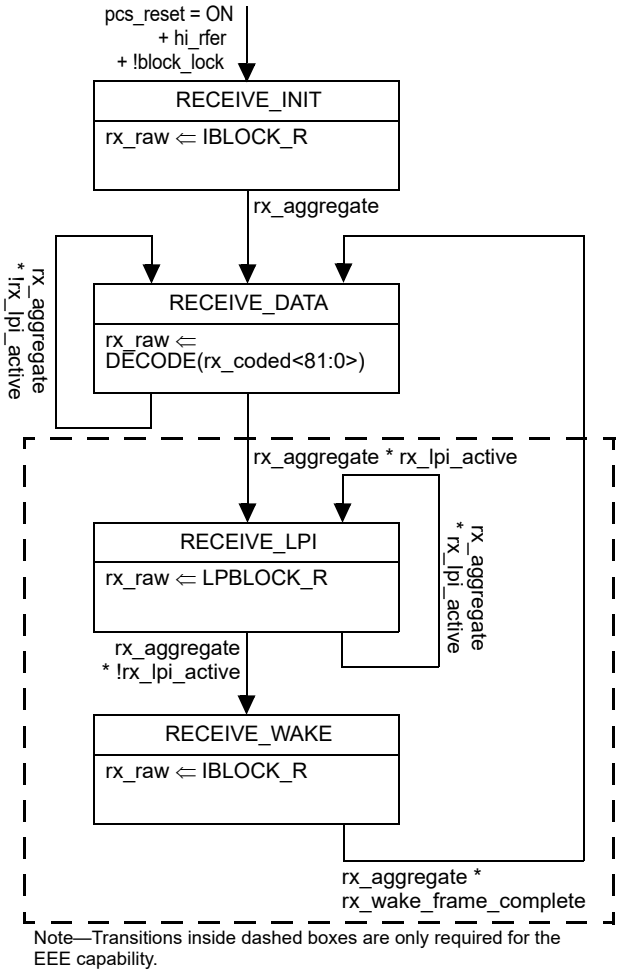

Note—Transitions inside dashed boxes are only required for the EEE capability.

Figure 97–12—PCS Receive state diagram

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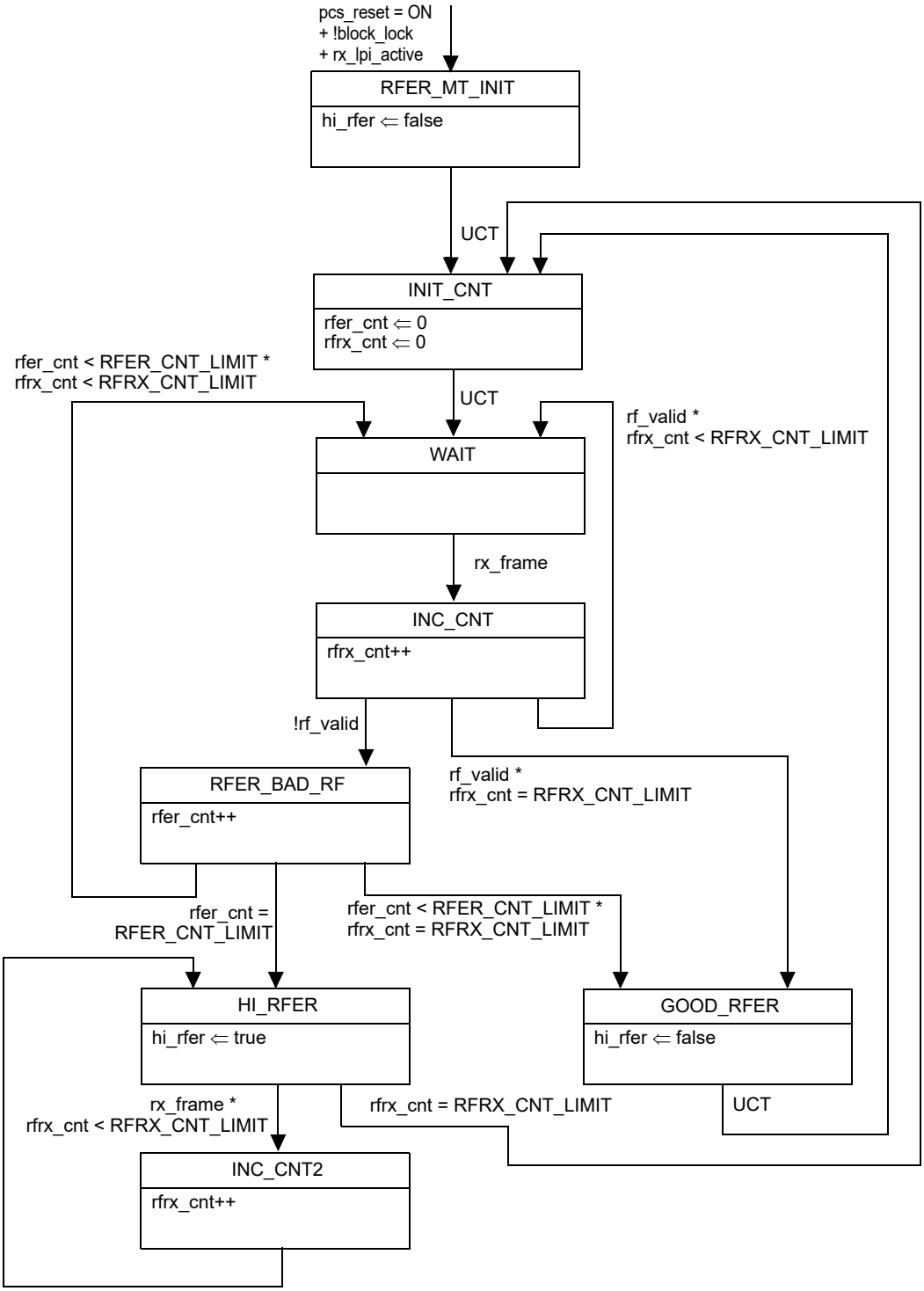

Figure 97–13—RFER monitor state diagram

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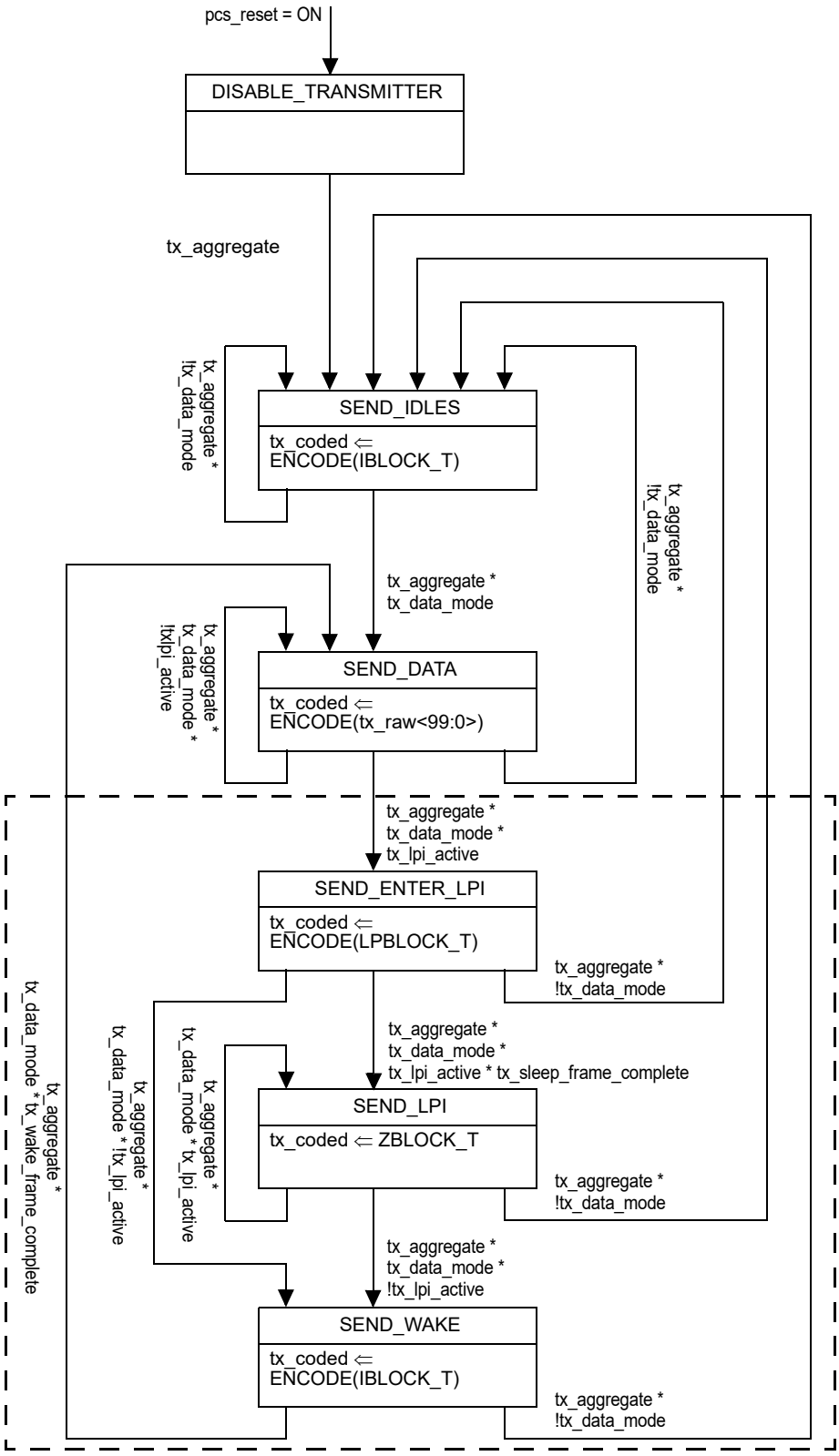

Note—Transitions inside dashed boxes are only required for the EEE capability.

Figure 97–14—PCS Transmit state diagram

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97.3.7 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

97.3.7.1 Status

PCS_status:
: Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_rfer is false. This status is reflected in MDIO register 3.2306.10. A latch low view of this status is reflected in MDIO register 3.2305.2 and the inverse of this status is reflected in MDIO register 3.2305.7.

block_lock:
: Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.2306.8. A latch low view of this status is reflected in MDIO register 3.2306.6.

hi_rfer:
: Indicates the state of the hi_rfer variable. This status is reflected in MDIO register 3.2306.9. A latch high view of this status is reflected in MDIO register 3.2306.7.

Rx LPI indication:
: For EEE capability, this variable indicates the current state of the receive LPI function. This flag is set to true (register bit set to one) when the PCS Receive state diagram (Figure 97–12) is in the RECEIVE_LPI or RECEIVE_WAKE states. This status is reflected in MDIO register 3.2305.8. A latch high view of this status is reflected in MDIO register 3.2305.10 (Rx LPI received).

Tx LPI indication:
: For EEE capability, this variable indicates the current state of the transmit LPI function. This flag is set to true (register bit set to one) when the PCS Transmit state diagram (Figure 97–14) is in the SEND_LPI or SEND_WAKE states. This status is reflected in MDIO register 3.2305.9. A latch high view of this status is reflected in MDIO register 3.2305.11 (Tx LPI received).

97.3.7.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

RFER_count:
: 6-bit counter that counts each time RFER_BAD_RF of the RFER monitor state diagram (see Figure 97–13) is entered. This counter is reflected in MDIO register bits 3.2306.5:0. The counter is reset when register 3.2306 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

97.3.7.3 Loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.2304.14 is set to a one. In this mode, the PCS shall accept data on the transmit path from the GMII and return it on the receive path to the GMII. In addition, the PCS shall transmit a continuous stream of GMII data to the 81B encoder and on further to the PMA sublayer and shall ignore all data presented to it by the PMA sublayer.

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97.3.8 BASE-T1 Operations, Administration, and Maintenance (OAM)

The 1000BASE-T1 PCS level Operations, Administration, and Maintenance (OAM) provides an optional mechanism useful for monitoring link operation such as exchanging PHY link health status and message exchange. When OAM is implemented, behavior shall conform to the state diagrams in Figure 97–17 and Figure 97–18. The 1000BASE-T1 OAM information is exchanged out of band between two PHYs using excess bandwidth available on the link. The 1000BASE-T1 OAM is strictly between two 1000BASE-T1 PHYs on the physical layer and their associated management entities if present. Passing 1000BASE-T1 OAM information to other layers is outside the scope of this standard.

1000BASE-T1 OAM is operational as long as both PHYs implement this mechanism and link is up. It continues to be operational during low power idle albeit the information is transferred at a slower rate during the refresh cycle.

The 1000BASE-T1 OAM frame data is carried in the OAM9 field described in 97.3.2.2.4 for the normal power data mode and 97.3.5.3 for low power mode. This 9-bit field is used to exchange 1000BASE-T1 OAM frames. The implementation of 1000BASE-T1 OAM frame exchange function is optional. However, if 1000BASE-T1 EEE is implemented, then the 1000BASE-T1 OAM frame exchange function is implemented to exchange, at a minimum, the link partner health status.

For the remainder of this subclause, the term 1000BASE-T1 OAM is specific to the 1000BASE-T1 PCS level OAM.

97.3.8.1 Definitions

1000BASE-T1 OAM frame: A frame consisting of 12 octets of data with 12 parity bits.

1000BASE-T1 OAM symbol: A 9-bit symbol consisting of one data octet plus a parity bit. Twelve 1000BASE-T1 OAM symbols make up an 1000BASE-T1 OAM frame.

1000BASE-T1 OAM field: The OAM9 field in each PHY frame as described in 97.3.2.2.11 or in each refresh cycle as described in 97.3.5.3.

1000BASE-T1 OAM message: A message contains a 4-bit message number plus 8 octets of message data embedded in an 1000BASE-T1 OAM frame. The same 1000BASE-T1 OAM message can be repeated on multiple 1000BASE-T1 OAM frames.

97.3.8.2 Functional specifications

97.3.8.2.1 1000BASE-T1 OAM Frame Structure

Each 1000BASE-T1 OAM frame is made up of 12 octets of data and 12 parity bits. Each symbol consists of 8 bits of data and one parity bit. The parity bit value for symbol 0 should be such that the sum of the number of 1s in the nine bits is even. The parity bit value for symbols 1 to 11 should be such that the sum of the number of 1s in the nine bits is odd.

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	D8	D7	D6	D5	D4	D3	D2	D1	D0
Symbol 0	Even Parity	Reserved	Reserved	Reserved	Reserved	PingRx	PingTx	SNR<1>	SNR<0>
Symbol 1	Odd Parity	Valid	Toggle	Ack	TogAck	Message_Number<3:0>			
Symbol 2	Odd Parity	Message<0><7:0>							
Symbol 3	Odd Parity	Message<1><7:0>							
Symbol 4	Odd Parity	Message<2><7:0>							
Symbol 5	Odd Parity	Message<3><7:0>							
Symbol 6	Odd Parity	Message<4><7:0>							
Symbol 7	Odd Parity	Message<5><7:0>							
Symbol 8	Odd Parity	Message<6><7:0>							
Symbol 9	Odd Parity	Message<7><7:0>							
Symbol 10	Odd Parity	CRC16							first bit
Symbol 11	Odd Parity	final bit	CRC16						

Figure 97–15—OAM Frame

One 1000BASE-T1 OAM symbol is placed in the 9-bit 1000BASE-T1 OAM field in each PHY frame during normal power operation in the data mode. One 1000BASE-T1 OAM symbol is placed in the 9-bit 1000BASE-T1 OAM field in each refresh cycle during low power idle. The 12 1000BASE-T1 OAM symbols are consecutively inserted into 12 consecutive PHY frames and/or refresh cycles. Once the 12 symbols of the current 1000BASE-T1 OAM frame are inserted, the 12 symbols of the next 1000BASE-T1 OAM frame are inserted. This process is continuous without any break in the insertion of 1000BASE-T1 OAM symbols.

Bit 0 of each 1000BASE-T1 OAM symbol is the first bit transmitted in the 9-bit 1000BASE-T1 OAM field. Symbol 0 is the first symbol transmitted in each 1000BASE-T1 OAM frame.

The 1000BASE-T1 OAM frame boundary can be found at the receiver by determining the symbol parity. Symbol 0 has even parity while all other symbols have odd parity.

If 1000BASE-T1 OAM is not implemented then the 9-bit 1000BASE-T1 OAM field shall be set to all 0s. If the link partner does not implement 1000BASE-T1 OAM, the 9-bit 1000BASE-T1 OAM field will remain static and the symbol parity will not change.

97.3.8.2.2 1000BASE-T1 OAM Frame Data

The 1000BASE-T1 OAM frame data is shown in Figure 97–15. OAM<x><y> refers to symbol x, bit y of the 1000BASE-T1 OAM frame. Reserved fields shall be set to 0.

97.3.8.2.3 Ping RX

The Ping RX is indicated in OAM<0><3>.

This bit is set by the PHY to the same value as the Ping TX bit received from the link partner.

97.3.8.2.4 Ping TX

The Ping TX is indicated in OAM<0><2>.

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This bit is set by the PHY to for the link partner to echo on Ping RX.

97.3.8.2.5 PHY Health

The PHY Health (SNR<1:0>) is indicated in OAM<0><1:0>.

This status is set by the PHY to indicate the status of the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

- 00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame
- 01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled)
- 10: PHY SNR is marginal
- 11: PHY SNR is good

97.3.8.2.6 1000BASE-T1 OAM Message Valid

The 1000BASE-T1 OAM message valid (Valid) is indicated in OAM<1><7>.

- 0: Current 1000BASE-T1 OAM frame does not contain a valid 1000BASE-T1 OAM message
- 1: Current 1000BASE-T1 OAM frame contains a valid 1000BASE-T1 OAM message

97.3.8.2.7 1000BASE-T1 OAM Message Toggle

The 1000BASE-T1 OAM message toggle (Toggle) is indicated in OAM<1><6>.

The toggle bit is used to ensure proper 1000BASE-T1 OAM message synchronization between the PHY and the link partner. The toggle bit in the current 1000BASE-T1 OAM message is set to the opposite value of the toggle bit in the previous 1000BASE-T1 OAM message only if link partner acknowledge the 1000BASE-T1 OAM message is received. This allows one 1000BASE-T1 OAM message to be delineated from a second 1000BASE-T1 OAM message since the same 1000BASE-T1 OAM message may be repeated over multiple 1000BASE-T1 OAM frames. This bit is valid only if Valid is set to 1.

97.3.8.2.8 1000BASE-T1 OAM Message Acknowledge

The 1000BASE-T1 OAM message Acknowledge (Ack) is indicated in OAM<1><5>.

Ack is set by the PHY to let the link partner know that the 1000BASE-T1 OAM message sent by the link partner was successfully received as defined in 97.3.8.2.13 and the PHY is ready to accept a new 1000BASE-T1 OAM message. An 1000BASE-T1 OAM message is defined to be Message_Number<3:0> and Message<7:0><7:0>.

- 0: No Acknowledge
- 1: Acknowledge

97.3.8.2.9 1000BASE-T1 OAM Message Toggle Acknowledge

The 1000BASE-T1 OAM message Toggle Acknowledge (TogAck) is indicated in OAM<1><4>.

TogAck is set by the PHY to let the link partner know which the 1000BASE-T1 OAM message is being acknowledged. TogAck takes the value of Toggle bit of the 1000BASE-T1 OAM message being acknowledged. This bit is valid only if Ack is set to 1.

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97.3.8.2.10 1000BASE-T1 OAM Message Number

The 1000BASE-T1 OAM message number is indicated in OAM<1><3:0>.

This field is user-defined but is recommended that it be used to indicate the meaning of the 8-octet message that follows. If used this way, up to 16 different 8-octet messages can be exchanged.

The message number is user-defined and its definition is outside the scope of this standard.

97.3.8.2.11 1000BASE-T1 OAM Message Data

The 1000BASE-T1 OAM message data is indicated in OAM<9:2><7:0>.

The 8-octet message data is user-defined and its definition is outside the scope of this standard.

Ack is set by the PHY to let the link partner know that the 1000BASE-T1 OAM frame sent by the link partner is successfully received as defined The 1000BASE-T1 OAM frame octet is the lower 8 bits of the 9-bit 1000BASE-T1 OAM symbol. Twelve octets form the 1000BASE-T1 OAM data.

97.3.8.2.12 CRC16

The CRC16 is indicated in OAM<11:10><7:0>.

The CRC16 implements the polynomial $(x+1)(x^{15}+x+1)$ of the previous 10 octets. The CRC16 shall produce the same result as the implementation shown in Figure 97–16. The 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards OEM<9:0><7:0> presented in their transmitted order as described in 97.3.8.2.1 are used to compute the CRC16 with the switch connected, which is setting CRC gen in Figure 97–16. Note that the parity bit is not used in the CRC16 calculation. After all the 10 octets have been processed, the switch is disconnected (setting CRC out) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0. S15 is indicated in OAM<10><0> and S0 is indicated in OAM<11><7>.

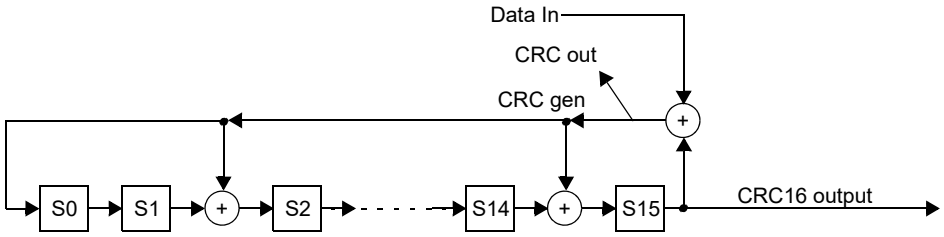

Figure 97–16—1000BASE-T1 OAM CRC16

97.3.8.2.13 1000BASE-T1 OAM Frame Acceptance Criteria

All fields of the 1000BASE-T1 OAM frame shall be accepted and updated, unless any of the following occurs:

a) Incorrect parity on any of the 12 symbols

b) Incorrect CRC16

c) Uncorrectable PHY frame on any of the 12 symbols

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97.3.8.2.14 PHY Health Indicator

The PHY current health is sent to the link partner on a per 1000BASE-T1 OAM frame basis using the SNR<1:0> bits as described in 97.3.8.2.5. It lets the link partner have an early indication of potential problems that may cause the PHY to drop link or have high error rates.

If EEE is implemented, there may be a case where a PHY's receiver can no longer maintain good SNR based on quiet/refresh cycles. Instead of dropping the link, the PHY can attempt to recover the link by forcing the link partner to exit LPI in its egress direction so that the PHY can use normal power mode to recover. This is done by transmitting SNR<1:0> with a value of 01.

If a PHY receives SNR<1:0> set to 01 by its link partner, then it cannot enter into LPI in the egress direction. If the PHY is already in LPI then the PHY shall immediately exit LPI.

97.3.8.2.15 Ping

The PingTx bit is set based on the value in mr_tx_ping. The PingRx bit is set based on the latest PingTx received from the link partner. The value in mr_rx_ping is set based on the received PingRx from the link partner. The user can determine that the link partner 1000BASE-T1 OAM is operating properly by togging mr_tx_ping and observing mr_rx_ping matches after a short delay.

The Ping bits are updated on a per 1000BASE-T1 OAM frame basis.

97.3.8.2.16 1000BASE-T1 OAM Message Exchange

Unlike the PHY health indicator and the ping function that operate on a per 1000BASE-T1 OAM frame basis, the 1000BASE-T1 OAM message exchange operates on a per 1000BASE-T1 OAM message basis that will occur over many 1000BASE-T1 OAM frames. The 1000BASE-T1 OAM message exchange mechanism allows a management entity attached to a PHY and its peer attached to the link partner to asynchronously pass 1000BASE-T1 OAM messages and verify their delivery.

The 1000BASE-T1 OAM message is first written into the 1000BASE-T1 OAM transmit registers in the PHY. The 1000BASE-T1 OAM message is then read out of the 1000BASE-T1 OAM transmit registers and transmitted to the link partner. After the link partner receives the 1000BASE-T1 OAM message it transfers it into the link partner's 1000BASE-T1 OAM receive registers and also sends an acknowledge back to the PHY indicating that the next 1000BASE-T1 OAM message can be transmitted. One 1000BASE-T1 OAM message can be loaded into the 1000BASE-T1 OAM transmit registers while another 1000BASE-T1 OAM message is being transmitted by the PHY to the link partner while yet another 1000BASE-T1 OAM message is being read out at the link partner's 1000BASE-T1 OAM receive registers. The exchange of 1000BASE-T1 OAM messages are occurring concurrently and bi-directionally.The transfers between the management entities can be done asynchronously. On the transmit side mr_tx_valid = 0 indicates that the next 1000BASE-T1 OAM message can be written into the 1000BASE-T1 OAM transmit registers. Once the registers are written the management entity sets mr_tx_valid to 1 to indicate that the 1000BASE-T1 OAM transmit registers contains a valid 1000BASE-T1 OAM message. Once the message is read out atomically, the state machine clears the mr_tx_valid to 0 to indicate that the registers are ready to accept the next 1000BASE-T1 OAM message.

On the receive side mr_rx_lp_valid indicates that valid 1000BASE-T1 OAM message can be read from the 1000BASE-T1 OAM receive registers. Once these registers are read, the mr_rx_lp_valid should be cleared to 0 to indicate that the registers are ready to receive the next 1000BASE-T1 OAM message. If mr_rx_lp_valid is not cleared then the 1000BASE-T1 OAM message transfer will eventually stall since the sender cannot send new 1000BASE-T1 OAM messages if the receiver does not acknowledge that an 1000BASE-T1 OAM message has been transferred into the 1000BASE-T1 OAM receive registers.

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The management entities can asynchronously read mr_tx_valid and mr_rx_lp_valid to know when 1000BASE-T1 OAM messages can be transferred in and out of the 1000BASE-T1 OAM registers.

The toggle bit alternates between 0 and 1, which lets the management entity determine which 1000BASE-T1 OAM message is being referred to. The toggle bit transitioning rules between one 1000BASE-T1 OAM frame to the next 1000BASE-T1 OAM frame are shown in Table 97–5.

Table 97–5—Toggle bit transition rules

Previous Valid	Previous Toggle	Current Valid	Current Toggle	Description
0	0	0	0	No valid 1000BASE-T1 OAM message
0	0	0	1	Illegal transition (Error)
0	0	1	0	New 1000BASE-T1 OAM message starting
0	0	1	1	Illegal transition (Error)
0	1	0	0	Illegal transition (Error)
0	1	0	1	No valid 1000BASE-T1 OAM message
0	1	1	0	Illegal transition (Error)
0	1	1	1	New 1000BASE-T1 OAM message starting
1	0	0	0	Illegal transition (Error)
1	0	0	1	Received acknowledge, no new 1000BASE-T1 OAM message to send
1	0	1	0	Repeating current 1000BASE-T1 OAM message, waiting for link partner's acknowledge
1	0	1	1	Previous 1000BASE-T1 OAM message ending, new 1000BASE-T1 OAM message starting
1	1	0	0	Received acknowledge, no new 1000BASE-T1 OAM message to send
1	1	0	1	Illegal transition (Error)
1	1	1	0	Previous 1000BASE-T1 OAM message ending, new 1000BASE-T1 OAM message starting
1	1	1	1	Repeating current 1000BASE-T1 OAM message, waiting for link partner's acknowledge

97.3.8.3 State diagram variable to BASE-T1 OAM register mapping

The state diagrams of Figure 97–18 and Figure 97–17 generate and accept variables of the form "mr_x," where x is an individual signal name. These variables comprise a management interface to communicate the 1000BASE-T1 OAM information to and from the management entity. Clause 45 MDIO registers are defined in MMD3 to support the 1000BASE-T1 OAM. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the information is recommended. Table 97–6 describes the MDIO register to the state diagrams variable mapping.

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Table 97–6—State Variables to BASE-T1 OAM Register Mapping

MDIO control/status variable	PCS register name	Register/bit number	PCS control/status variable
BASE-T1 OAM Message Valid	BASE-T1 OAM transmit register	3.2308.15	mr_tx_valid
Toggle Value	BASE-T1 OAM transmit register	3.2308.14	mr_tx_toggle
BASE-T1 OAM Message Received	BASE-T1 OAM transmit register	3.2308.13	mr_tx_received
Received Message Toggle Value	BASE-T1 OAM transmit register	3.2308.12	mr_tx_received_toggle
Message Number	BASE-T1 OAM transmit register	3.2308.11:8	mr_tx_message_num[3:0]
Ping Received	BASE-T1 OAM transmit register	3.2308.3	mr_rx_ping
Ping Transmit	BASE-T1 OAM transmit register	3.2308.2	mr_tx_ping
Local SNR	BASE-T1 OAM transmit register	3.2308.1:0	mr_tx_SNR[1:0]
BASE-T1 OAM Message 0	BASE-T1 OAM message register	3.2309.7:0	mr_tx_message[7:0]
BASE-T1 OAM Message 1	BASE-T1 OAM message register	3.2309.15:8	mr_tx_message[15:8]
BASE-T1 OAM Message 2	BASE-T1 OAM message register	3.2310.7:0	mr_tx_message[23:16]
BASE-T1 OAM Message 3	BASE-T1 OAM message register	3.2310.15:8	mr_tx_message[31:24]
BASE-T1 OAM Message 4	BASE-T1 OAM message register	3.2311.7:0	mr_tx_message[39:32]
BASE-T1 OAM Message 5	BASE-T1 OAM message register	3.2311.15:8	mr_tx_message[47:40]
BASE-T1 OAM Message 6	BASE-T1 OAM message register	3.2312.7:0	mr_tx_message[55:48]
BASE-T1 OAM Message 7	BASE-T1 OAM message register	3.2312.15:8	mr_tx_message[63:56]
Link Partner BASE-T1 OAM Message Valid	BASE-T1 OAM receive register	3.2313.15	mr_rx_lp_valid
Link Partner Toggle Value	BASE-T1 OAM receive register	3.2313.14	mr_rx_lp_toggle

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Table 97–6—State Variables to BASE-T1 OAM Register Mapping *(continued)*

MDIO control/status variable	PCS register name	Register/bit number	PCS control/status variable
Link Partner Message Number	BASE-T1 OAM receive register	3.2313.11:8	mr_rx_lp_message_num[3:0]
Link Partner SNR	BASE-T1 OAM receive register	3.2313.1:0	mr_rx_lp_SNR[1:0]
Link Partner BASE-T1 OAM Message 0	Link partner BASE-T1 OAM message register	3.2314.7:0	mr_rx_lp_message[7:0]
Link Partner BASE-T1 OAM Message 1	Link partner BASE-T1 OAM message register	3.2314.15:8	mr_rx_lp_message[15:8]
Link Partner BASE-T1 OAM Message 2	Link partner BASE-T1 OAM message register	3.2315.7:0	mr_rx_lp_message[23:16]
Link Partner BASE-T1 OAM Message 3	Link partner BASE-T1 OAM message register	3.2315.15:8	mr_rx_lp_message[31:24]
Link Partner BASE-T1 OAM Message 4	Link partner BASE-T1 OAM message register	3.2316.7:0	mr_rx_lp_message[39:32]
Link Partner BASE-T1 OAM Message 5	Link partner BASE-T1 OAM message register	3.2316.15:8	mr_rx_lp_message[47:40]
Link Partner BASE-T1 OAM Message 6	Link partner BASE-T1 OAM message register	3.2317.7:0	mr_rx_lp_message[55:48]
Link Partner BASE-T1 OAM Message 7	Link partner BASE-T1 OAM message register	3.2317.15:8	mr_rx_lp_message[63:56]

97.3.8.4 Detailed functions and state diagrams

97.3.8.4.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, counters, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

97.3.8.4.2 State diagram parameters

97.3.8.4.3 Variables

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_rx_lp_message[63:0]
: Eight octet 1000BASE-T1 OAM message from the link partner. The value in this variable is valid only when mr_rx_lp_valid is 1.

mr_rx_lp_message_num[3:0]
: Four bit message number from the link partner. The value in this variable is valid only when mr_rx_lp_valid is 1.

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mr_rx_lp_SNR[1:0]

Link partner health status.

Values:

00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame

01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled).

10: PHY SNR is marginal

11: PHY SNR is good

The threshold for the status is implementation dependent.

mr_rx_lp_toggle

The toggle bit value associated with the eight octet 1000BASE-T1 OAM message from the link partner.

Values:

The toggle bit alternates between 0 and 1.

mr_rx_lp_valid

Indicates whether 1000BASE-T1 OAM message in mr_rx_lp_message[63:0], mr_rx_lp_message_num[3:0] and the toggle bit in mr_rx_lp_toggle is valid or not. This variable should be cleared when mr_rx_lp_message[63:48] is read and is not explicitly shown in the state machine. The clearing of this variable indicates to the state machine that the 1000BASE-T1 OAM message is read by the user and the state machine can proceed to load in the next 1000BASE-T1 OAM message.

Values:

0: invalid

1: valid

mr_rx_ping

Echoed ping value from the link partner.

Values:

The value can be 0 or 1.

mr_tx_message[63:0]

Eight octet 1000BASE-T1 OAM message transmitted by the local PHY. The value in this variable is valid only when mr_tx_valid is 1.

mr_tx_message_num[3:0]

Four bit message number transmitted by the local PHY. The value in this variable is valid only when mr_tx_valid is 1.

mr_tx_ping

Ping value transmitted by the local PHY.

Values:

The value can be 0 or 1.

mr_tx_received

Indicates whether the most recently transmitted 1000BASE-T1 OAM message with a toggle bit value of mr_tx_received_toggle was received, read, and acknowledged by the link partner. This variable shall clear on read.

Values:

0: 1000BASE-T1 OAM message not received and read by the link partner

1: 1000BASE-T1 OAM message received by the link partner

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mr_tx_received_toggle

Toggle bit value of the 1000BASE-T1 OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if mr_tx_received is 1.

Values:

The value can be 0 or 1.

mr_tx_SNR[1:0]

Status register indicating PHY health status.

Values:

00: PHY link is failing and will drop link and relink within 2 to 4 ms after the end of the current 1000BASE-T1 OAM frame
01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled)
10: PHY SNR is marginal
11: PHY SNR is good

The threshold for the status is implementation dependent.

mr_tx_toggle

The toggle bit value associated with the eight octet 1000BASE-T1 OAM message transmitted by the PHY. The value is automatically set by the state machine and cannot be set by the user. This bit should be read and recorded prior to setting mr_tx_valid to 1.

Values:

The toggle bit alternates between 0 and 1.

mr_tx_valid

Indicates whether 1000BASE-T1 OAM message in mr_tx_message[63:0] and mr_rx_lp_message_num[3:0] is valid or not. This register will be cleared by the state machine to indicate whether the next 1000BASE-T1 OAM message can be written into the registers.

Values:

0: invalid
1: valid

reset

Reset

Values:

false: 1000BASE-T1 OAM circuit not in reset
true: 1000BASE-T1 OAM circuit is in reset

rx_ack

Acknowledge from link partner in response to PHY's 1000BASE-T1 OAM message.

Values:

0: no acknowledge
1: acknowledge

rx_ack_toggle

The toggle value corresponding to the PHY's 1000BASE-T1 OAM message that the link partner is acknowledging. This value is valid only if the rx_ack is set to 1.

Values:

The toggle bit can take on values of 0 or 1.

rx_boundary

This variable is set to true whenever the receive data stream reaches the end of a Reed-Solomon frames during normal power operation in the data mode, or at the end of a received refresh cycle

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during low power idle operation. This variable is set to false at other times.
Values:
false: receive stream not at a boundary end
true: receive stream at a boundary end

rx_exp_toggle
This variable holds the expected toggle value of the next 1000BASE-T1 OAM message. This is normally the opposite value of the current toggle value, but is reset on error conditions where two back to back 1000BASE-T1 OAM messages separated by 1000BASE-T1 OAM frames without a valid message have the same toggle value.
Values:
The toggle bit can take on values of 0 or 1.

rx_lp_ack
Acknowledge from PHY in response to link partner's 1000BASE-T1 OAM message. Indicates whether valid 1000BASE-T1 OAM message from the link partner has been sampled into the PHY's registers.
Values:
0: no acknowledge / not sampled
1: acknowledge / sampled

rx_lp_ping
Ping value received from the link partner that should be looped back.
Values:
The value can be 0 or 1.

rx_lp_toggle
The toggle bit value in the previous 1000BASE-T1 OAM frame received from the link partner.
Values:
The toggle bit alternates between 0 and 1.

rx_lp_valid
Indicates whether 1000BASE-T1 OAM message in previous 1000BASE-T1 OAM frame received from the link partner is valid or not.
Values:
0: invalid
1: valid

rx_oam_field<8:0>
Nine bit 1000BASE-T1 OAM symbol extracted from a received Reed-Solomon frame during normal power operation in the data mode, or from a received refresh cycle during low power idle operation.

rx_oam<11 to 0><8:0>
Raw 12 symbol 1000BASE-T1 OAM frame received from the link partner.

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SNR[1:0]

PHY health status.

Values:

00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame

01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled)

10: PHY SNR is marginal

11: PHY SNR is good

Both the status threshold and condition for generating this status are implementation dependent.

tx_boundary

This variable is set to true whenever the transmit data stream reaches the start of a PHY frame during normal power operation in the data mode, or at the start of a transmit refresh cycle during low power idle operation. This variable is set to false at other times.

Values:

false: transmit stream not at a boundary end

true: transmit stream at a boundary end

tx_oam_field<8:0>

Nine bit 1000BASE-T1 OAM symbol inserted into a transmitted Reed-Solomon frame during normal power operation in the data mode, or into a transmitted refresh cycle during low power idle operation.

tx_oam<11 to 0><8:0>

Raw 12 symbol 1000BASE-T1 OAM frame transmitted from the PHY.

tx_lp_ready

Indicates whether the link partner is ready to receive the next 1000BASE-T1 OAM message from the PHY. If ready, then the PHY will load the next 1000BASE-T1 OAM message from the registers and begin transmitting them.

Values:

0: not ready

1: ready

tx_toggle

The toggle bit value being send in the current 1000BASE-T1 OAM frame transmitted by the PHY.

Values:

The value can be 0 or 1.

97.3.8.4.4 Counters

rx_cnt

A count of received 1000BASE-T1 OAM frames.

Values:

The value can be any integer from 0 to 12, inclusive.

tx_cnt

1000BASE-T1 OAM frame transmit symbol count.

Values:

The value can be any integer from 0 to 12, inclusive.

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97.3.8.4.5 Functions

CRC16(10 octets)

This function outputs a 16-bit CRC value using 10-octet input as defined in 97.3.8.2.12.

CRC16_Check(12 octets)

This function checks whether the 12-octet frame has the correct CRC16 as defined in 97.3.8.2.12.

Values:

BAD: CRC16 check is bad

GOOD: CRC16 check is good

Parity(12 octets)

This function outputs 12 parity bits, one for each of the 12 input octets. An even parity bit is output for the first octet, and odd parity bits are output for each of the remaining 11 octets.

Parity_Check(9-bit symbol)

This function calculates the bit parity of the 9-bit symbol.

Values:

Even: symbol has even parity

Odd: symbol has odd parity

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97.3.8.4.6 State diagrams

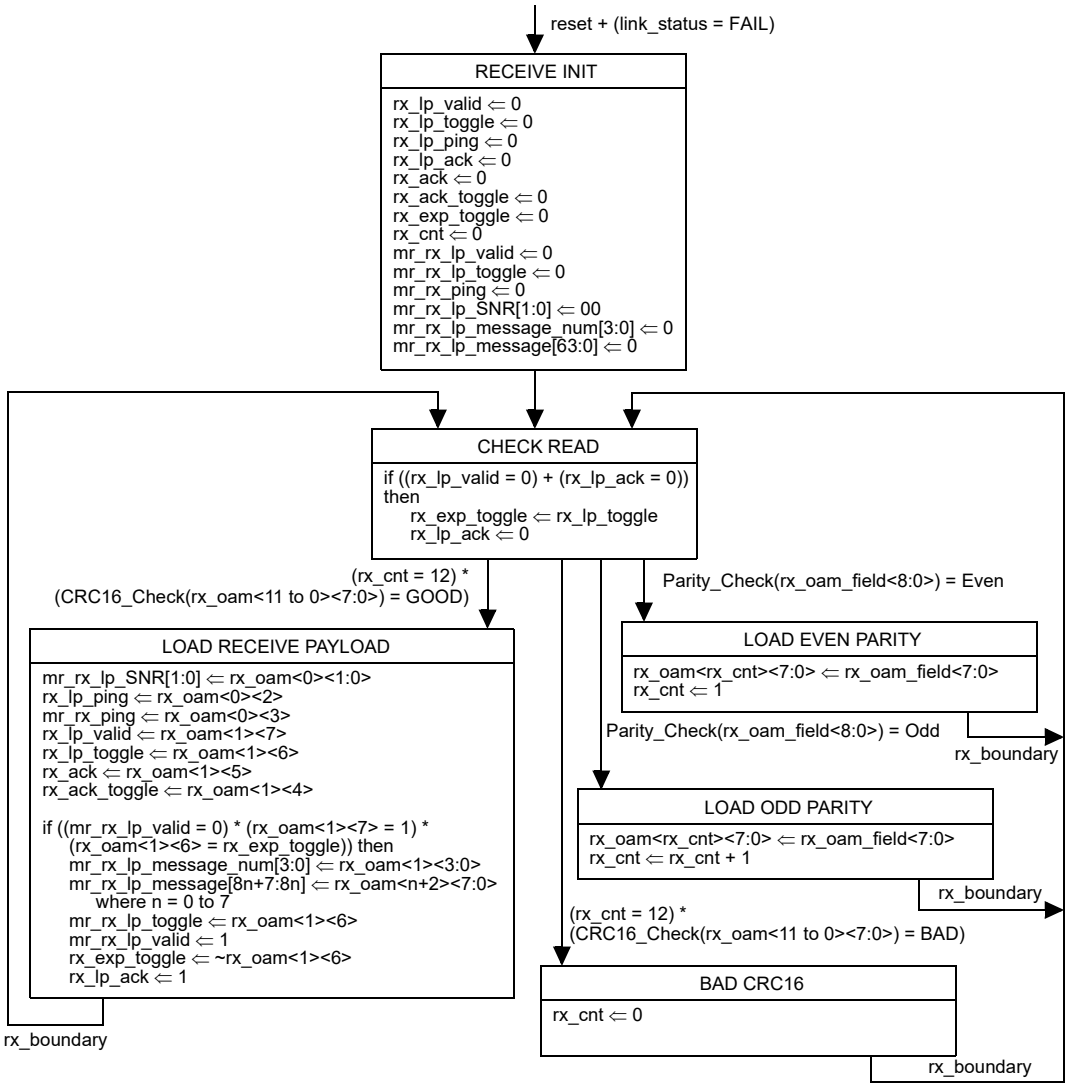

Figure 97–17—Receive state diagram

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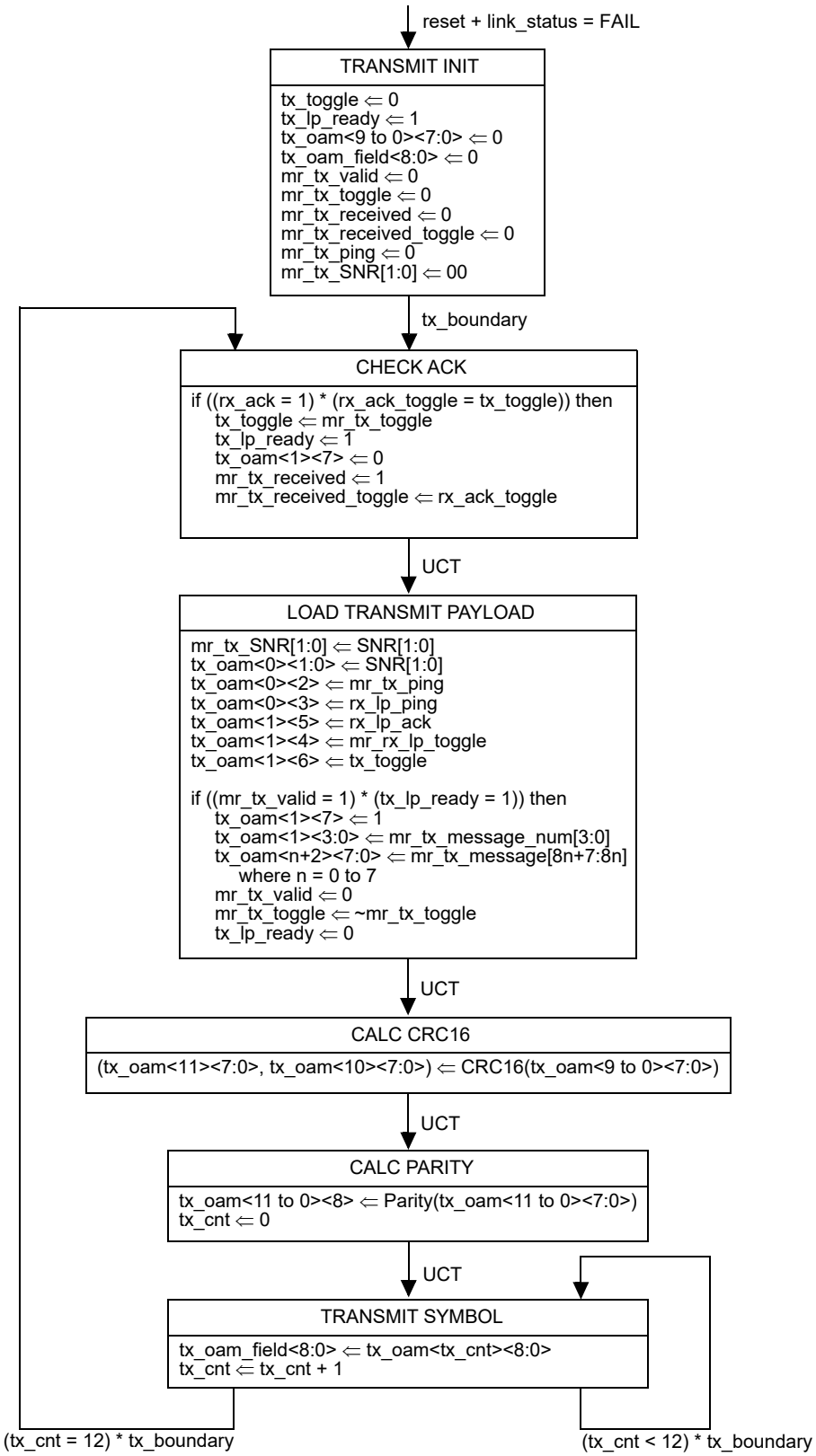

Figure 97–18—Transmit state diagram

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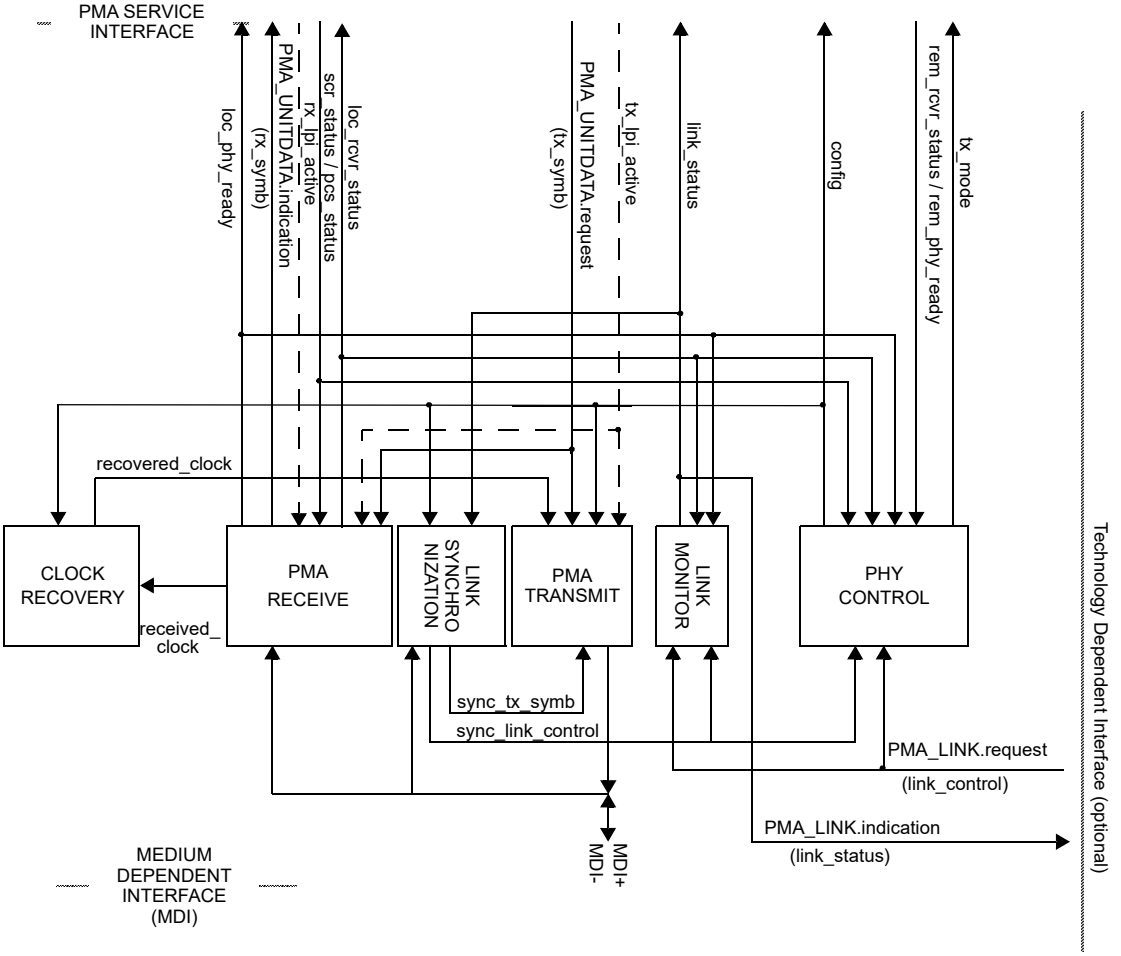
97.4 Physical Medium Attachment (PMA) sublayer

97.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 97.2.2 to the 1000BASE-T1 baseband medium, specified in 97.5.

The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 97.7.



NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

Figure 97–19—PMA reference diagram

97.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

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The PMA reference diagram, Figure 97–19, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 97–19.

97.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power for the device containing the PMA has not reached the operating state
b) The receipt of a request for reset from the management entity

PMA Reset sets pma_reset = ON while any of the above reset conditions hold true. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The 1000BASE-T1 PMA takes no longer than 100 ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 97–26).

97.4.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a three level modulated signal on the single twisted-pair copper cable. PMA Transmit shall continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb when sync_link_control = ENABLE, or the sync_tx_symb output by the PHY Link Synchronization function when sync_link_control = DISABLE, after processing with optional transmit filtering, digital-to-analog conversion (DAC) and subsequent analog filtering. The signals generated by PMA Transmit shall comply with the electrical specifications given in 97.5.

When the PMA_CONFIG.indication parameter config is MASTER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 97.5.3.3. The MASTER-SLAVE relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 97.4.2.8 while meeting the jitter requirements of 97.5.3.3.

97.4.2.2.1 Global PMA transmit disable

When the PMA_transmit_disable variable is set to true, this function shall turn off the transmitter so that the transmitter Average Launch Power of the Transmitter is less than –53 dBm.

97.4.2.3 PMA Receive function

The PMA Receive function comprises a receiver for PAM3 signals on the twisted-pair. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over receive pair and to present these sequences to the PCS Receive function. The PMA translates the signals received on the twisted-pair into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 3.6×10^{-7} after RS-FEC decoding, over a channel meeting the requirements of 97.6.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization and echo cancellation. The sequence of symbols assigned to tx_symb is needed to perform echo cancellation.

The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, and estimation functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's

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tx_mode changes to SEND_Z from any other values (see PHY Control state diagram in Figure 97–26). The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for pair polarity swaps.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.238.6.

97.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 97–26.

During PMA training (TRAINING and COUNTDOWN states in Figure 97–26), PHY Control information is exchanged between link partners with a 12-octet InfoField, which is XORed with the first 96 bits of the 15th partial PHY frame (bits 2520 to 2615) of the PHY frame. The InfoField is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions prior to the PAM2 to PAM3 transition.

The 12-octet InfoField shall include the fields in 97.4.2.4.2 through 97.4.2.4.8, also shown in the overview Figure 97–20, and the more detailed Figure 97–21 and Figure 97–22. Each InfoField shall be transmitted at least 256 times to ensure detection at link partner.

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10			octets 11/12
0xBB	0xA7	0x00	PFC24	Message	MSG24	MSG24	MSG24	CRC16

Figure 97–20—InfoField format

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	SeedUsrCfgCap	CRC16

Figure 97–21—InfoField TRAINING format

PMA_state = 01

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 97–22—InfoField COUNTDOWN format

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97.4.2.4.1 InfoField notation

For all the InfoField notations in the following subclauses, Reserved<bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The InfoField is transmitted following the notation described in 97.3.2.2.3 where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

97.4.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of 3 octets [Oct1<7:0>, Oct2<7:0>, Oct3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Oct1<7:0> and so forth.

97.4.2.4.3 Partial PHY frame Count (PFC24)

The start of partial PHY frame Count consists of 3 octets [Oct4<7:0>, Oct5<7:0>, Oct6<7:0>] and indicates the running count of partial PHY frames sent LSB first. There are 15 partial PHY frames per PHY frame and the InfoField is embedded within the 15th partial PHY frame. The first partial PHY frame is zero, thus the first partial PHY frame count field after a reset is 14.

97.4.2.4.4 Message Field

Message Field (1 octet). For the MASTER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, en_slave_tx<4>, reserved<3:0>}. For the SLAVE, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING, and PMA_state<7:6> = 01 indicates COUNTDOWN.

All possible Message Field settings are listed in Table 97–7 for the MASTER and Table 97–8 for the SLAVE. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 97–7 for the MASTER and the first or second row of Table 97–8 for the SLAVE. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the InfoField variable is set to loc_rcvr_status<5> = 1 and set to 0 otherwise.

Table 97–7—InfoField message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

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Table 97–8—InfoField message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

97.4.2.4.5 PHY Capability Bits, User Configurable Register, and Data Mode Scrambler Seed

When PMA_state<7:6> = 00, then [0ct8<7:0>, 0ct9<7:0>, 0ct10<7:0>] contains the two PHY capability bits, the user configurable register bits, and the 15-bit data mode scrambler seed (Seed). Each octet is sent LSB first.

The format of PHY capability bits is Oct9<7> = EEEen and Oct10<0> = OAMen, indicating EEE and 1000BASE-T1 OAM capability enable, respectively. The PHY shall indicate the support of optional capabilities by setting the corresponding capability bits.

The data mode scrambler seed contains bits S14 (sent first) to S0 (sent last) to indicate the initial state of the data mode transmit scrambler of the local device upon reaching the data switch partial PHY frame count. The state of the scrambler in Figure 97–9 shall be S14:S0 at the first bit of the first PHY frame when the partial PHY frame counter equals to the DataSwPFC24 value, see 97.4.2.4.6. The format of Seed is Oct8<7:0> = S<7:14> and Oct9<6:0> = S<0:6>. Seed S<14:0> shall not be all zeros.

The remaining 7-bit Oct10<7:1> form a user-configurable register. See 97.4.2.4.11 for details.

97.4.2.4.6 Data Switch partial PHY frame Count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the data switch partial PHY frame count (DataSwPFC24) sent LSB first. DataSwPFC24 indicates the partial PHY frame count when the transmitter switches from PAM2 to PAM3, which occurs at the start of an RS-FEC block. The last value of PFC24 prior to the transition is DataSwPFC24 - 1. DataSwPFC24 shall be set to an integer multiple of 15. This value of DataSwPFC24 guarantees that the switch from PAM2 to PAM3 occurs on a PHY frame boundary.

97.4.2.4.7 Reserved Fields

When PMA_state<7:6> is greater than 01, then [Oct8<1:0>, Oct9<1:0>, Oct10<7:0>] contains a reserved field. All InfoField fields denoted Reserved are reserved for future use.

97.4.2.4.8 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x+1)(x^{15}+x+1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 97–23. In Figure 97–23 the 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards Oct4 through Oct10 are used to compute the CRC16 with the switch connected, which is setting CRCgen in Figure 97–23. After all the 7 octets have

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been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

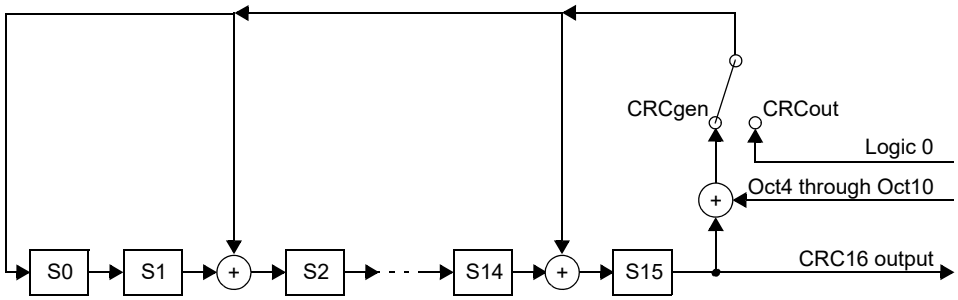

Figure 97–23—CRC16

97.4.2.4.9 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 97–9. Mapping of MDIO status variables to PMA status variables is shown in Table 97–10.

Table 97–9—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	Control register 1 / 1000BASE-T1 PMA control register	1.0.15 / 1.2304.15	pma_reset
Transmit disable	1000BASE-T1 PMA control register	1.2304.14	PMA_transmit_disable

Table 97–10—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Receive fault	1000BASE-T1 PMA status register	1.2305.1	PMA_receive_fault

97.4.2.4.10 Startup sequence

The startup sequence shall comply with the state diagram description given in Figure 97–26. If the Auto-Negotiation function is not implemented, or mr_autoneg_en = false, PMA_CONFIG is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup.

The Auto-Negotiation function is optional for 1000BASE-T1 PHYs. If the Auto-Negotiation function is used, during the Auto-Negotiation process PHY Control is in the DISABLE_TRANSMITTER state and the transmitter is disabled. If the Auto-Negotiation function is not used, during the PHY Link Synchronization stage the PHY Control remains in the DISABLE_TRANSMITTER state and the Link Synchronization function (see 97.4.2.6) is the data source for the PMA Transmit function.

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When the Auto-Negotiation asserts link_control = ENABLE, or PHY Link Synchronization process asserts sync_link_control = ENABLE, PHY Control enters the INIT_MAXWAIT_TIMER state. Upon entering the INIT_MAXWAIT_TIMER state, the maxwait_timer is started. PHY Control then transitions to the SILENT state where the minwait_timer is started and the PHY transmits zeros (tx_mode = SEND_Z).

In MASTER mode PHY Control transitions to the TRAINING state once the minwait_timer expires.

Upon entering the TRAINING state, the minwait_timer is started and the PHY Control asserts tx_mode = SEND_T sending PAM2 together with InfoFields. The PHY Control also sets PMA_state = 00 and sends the PHY capability bits, the user configurable register bits, and the Seed value used by the local device for the data mode scrambler initialization, see 97.4.2.4.5.

The optional EEE capability shall be enabled only if both PHYs set the capability bit EEEen = 1. The optional 1000BASE-T1 OAM capability shall be enabled only if both PHYs set the capability bit OAMen = 1.

Initially the MASTER is not ready for the SLAVE to respond and sets en_slave_tx = 0, which is communicated to the link partner via the InfoField. After the MASTER has sufficiently converged the necessary circuitry, the MASTER shall set en_slave_tx = 1 to allow the SLAVE to transition to TRAINING.

In SLAVE mode PHY Control transitions to the TRAINING state only after the SLAVE PHY acquires timing, converges its equalizers, acquires its descrambler state and sets loc_SNR_margin = OK. The SLAVE shall align its transmit 81B-RS frame to within +0/–1 partial PHY frames of the MASTER as seen at the SLAVE MDI. The SLAVE InfoField partial PHY frame Count shall match the MASTER InfoField partial PHY frame Count for the aligned frame.

Upon entering TRAINING state the SLAVE initially sets timing_lock_OK = 0 until it has acquired timing lock at which point the SLAVE sets timing_lock_OK = 1.

After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter InfoField value loc_rcvr_status. The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr_status. Upon expiration of the minwait_timer and when the condition loc_rcvr_status = OK and rem_rcvr_status = OK is satisfied, PHY control transitions to the COUNTDOWN state.

Upon entering the COUNTDOWN state, PHY Control sets PMA_state = 01 and DataSwPFC24 to the value of the partial PHY frame count when the transmitter switches from PAM2 to PAM3.

Upon reaching DataSwPFC24 partial PHY frame count PHY Control transitions to the SEND_IDLE1 state and forces transmission into the idle mode by asserting tx_mode = SEND_I.

Once the link partner has transitioned from PAM2 to PAM3, PHY Control transitions to the SEND_IDLE2 state and starts the minwait_timer.

Upon expiration of the minwait_timer and when the condition loc_phy_ready = OK and rem_phy_ready = OK is satisfied, PHY control transitions to the SEND_DATA state.

Upon entering the SEND_DATA state, PHY Control starts the minwait_timer and enables frame transmission to the link partner by asserting tx_mode = SEND_N.

The operation of the maxwait_timer requires that the PHY complete the startup sequence from state INIT_MAXWAIT_TIMER to SEND_DATA in the PHY Control state diagram state diagram (Figure 97–26) in less than 97.5 ms to avoid link_status being changed to FAIL by the Link Monitor state diagram (Figure 97–27).

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97.4.2.4.11 PHY Control Registers

The PHY control registers are shown in Table 97–11.

Table 97–11—PHY Control Registers

MDIO control/status variable	PMA register name	Register/bit number	PMA control/status variable
MASTER-SLAVE	BASE-T1 PMA/PMD control register	1.2100.14	force_config (see 97.4.2.6.1)
Type selection	BASE-T1 PMA/PMD control register	1.2100.3:0	force_PHY_type (see 97.4.2.6.1)
1000BASE-T1 OAM Ability	1000BASE-T1 PMA status register	1.2305.11	
EEE Ability	1000BASE-T1 PMA status register	1.2305.10	
User Field	1000BASE-T1 training register	1.2306.10:4	PMA_state<7:6> = 00, Oct10<7:1>
1000BASE-T1 OAM Advertisement	1000BASE-T1 training register	1.2306.1	PMA_state<7:6> = 00, Oct10<0>
EEE Advertisement	1000BASE-T1 training register	1.2306.0	PMA_state<7:6> = 00, Oct9<7>
Link Partner User Field	1000BASE-T1 link partner training register	1.2307.10:4	LP PMA_state<7:6> = 00, Oct10<7:1>
Link Partner 1000BASE-T1 OAM Advertisement	1000BASE-T1 link partner training register	1.2307.1	LP PMA_state<7:6> = 00, Oct10<0>
Link Partner EEE Advertisement	1000BASE-T1 link partner training register	1.2307.0	LP PMA_state<7:6> = 00, Oct9<7>

97.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel causes the PMA to set link_status to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the auto-negotiation (if enabled) or synchronization (if auto-negotiation is not enabled) process.

The Link Monitor function shall comply with the state diagram of Figure 97–27.

Upon power on, reset, or release from power down, the Auto-Negotiation function set link_control = DISABLE, or PHY Link Synchronization algorithms set sync_link_control = DISABLE. During this period, link_status = FAIL is asserted. When the Auto-Negotiation function establishes the presence of a remote 1000BASE-T1 PHY, link_control is set to ENABLE, or when the PHY Link Synchronization finishes the synchronization function, sync_link_control is set to ENABLE, and the Link Monitor state machines begins monitoring the PCS and receiver lock status. As soon as reliable transmission is achieved, the variable link_status = OK is asserted, upon which further PHY operations can take place.

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97.4.2.6 PHY Link Synchronization

If the optional Clause 98 Auto-Negotiation function is disabled or not implemented, then the Link Synchronization function is responsible for establishing the start of PHY PMA training as defined in 97.4.2.4.

When operating, the Link Synchronization function is the data source for the PMA Transmit function (see 97.4.2.2) and generates a signal, SEND_S, used by the MASTER and SLAVE to discover the link partner and synchronize the start of PMA training.

Link Synchronization employs the SEND_S signal to achieve synchronization prior to link training. If the PHY is configured as MASTER, Link Synchronization shall employ Equation (97–8) as the PN sequence generator.

$$p_M(x) = x^8 + x^4 + x^3 + x^2 + 1 \quad (97–8)$$

If the PHY is configured as SLAVE, Link Synchronization shall employ Equation (97–9) as PN sequence generator.

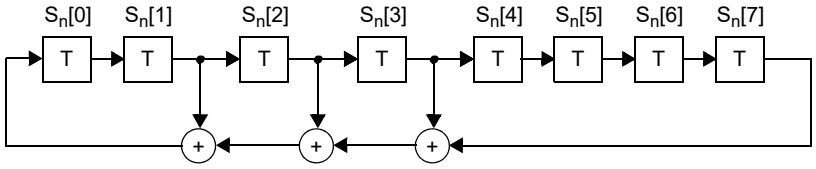
$$p_{MS}(x) = x^8 + x^6 + x^5 + x^4 + 1 \quad (97–9)$$

The period of both PN sequences is 255.

An implementation of MASTER and SLAVE PHY SEND_S PN sequence generators by linear-feedback shift registers is shown in Figure 97–24. The bits stored in the shift register delay line at time n are denoted by Sn[7:0]. At each symbol period, the shift register is advanced by one bit, and one new bit represented by Sn[0] is generated. The PN sequence generator shift registers shall be reset to a non-zero value upon entering into the TRANSMIT_DISABLE state (see Figure 97–25). The receiver may not necessarily receive a continuous PN sequence between separate periods of SEND_S.

The bit $S_n[0]$ is mapped to the transmit symbol Tn as follows: if $S_n[0] = 0$ then Tn = +1, if $S_n[0] = 1$ then Tn = –1.

MASTER PHY SEND_S PN sequence generator



SLAVE PHY SEND_S PN sequence generator

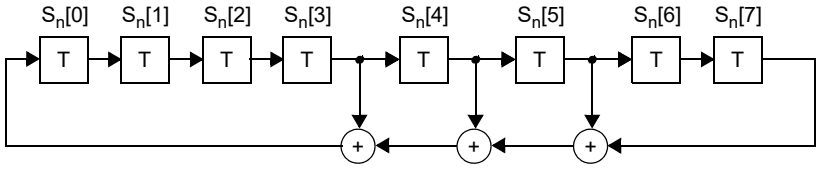


Figure 97–24—SEND_S PN sequence generator by linear feedback shift registers S_n

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The synchronization state diagram in Figure 97–25 shall be used to synchronize 1000BASE-T1 PHYs prior to the 1000BASE-T1 link training. If Clause 98 Auto-Negotiation function is enabled, then the Auto-Negotiation function shall be used as the mechanism for PHY synchronization and the synchronization state diagram in Figure 97–25 remains in the SYNC_DISABLE state.

97.4.2.6.1 State diagram variables

force_config
: This variable indicates whether the PHY operates as a MASTER or as a SLAVE. The variable takes on one of the following values:
  - MASTER: this value is continuously asserted when the PHY operates as a MASTER
  - SLAVE: this value is continuously asserted when the PHY operates as a SLAVE

force_phy_type
: This variable indicates what speed the PHY is to operate when Auto-Negotiation is disabled or not implemented. The variable takes on one of the following values:
  - 1000-T1: if Auto-Negotiation is disabled or not implemented and 1000BASE-T1 is selected
  - 100-T1: if Auto-Negotiation is disabled or not implemented and 100BASE-T1 is selected
  - None: else

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_autoneg_enable
: See 98.5.1.

mr_main_reset
: See 98.5.1.

power_on
: See 98.5.1.

send_s_sigdet
: This variable indicates whether the SEND_S pattern was detected. This variable shall be set false no later than 1 μs after the signal goes quiet on the MDI.
  Values:
  - true: SEND_S pattern detected
  - false: SEND_S pattern not detected

sync_link_control
: This variable indicates the data source for the PMA Transmit function.
  Values:
  - DISABLE: The data source is the PHY Link Synchronization function (sync_tx_symb)
  - ENABLE: The data source is PMA_UNITDATA.request (tx_symb)

sync_tx_mode
: This variable indicates what symbols are sent by the PHY Link Synchronization process.
  Values:
  - SEND_S: this value is continuously asserted to enable transmission of the PN sequence defined in 97.4.2.6
  - SEND_Z: this value is asserted to disable transmission

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97.4.2.6.2 State diagram timers

break_link_timer
: See 98.5.2.

link_fail_inhibit_timer
: See 98.5.2.

send_s_timer
: This timer is used to control the duration SEND_S is transmitted. The timer shall expire 1.0 μs ± 0.04 μs after being started.

sigdet_wait_timer
: This timer is used to control the wait time after transmitting or detecting the end of SEND_S. The timer shall expire 4 μs ± 0.1 μs after being started.

97.4.2.6.3 Messages

sync_tx_symb
: A signal sent from Link Synchronization block to PMA Transmit indicating that a PAM2 (SEND_S) or zero (SEND_Z) symbol is available. The Link Synchronization block generates sync_tx_symb synchronously with every transmit clock cycle.

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97.4.2.6.4 State diagrams

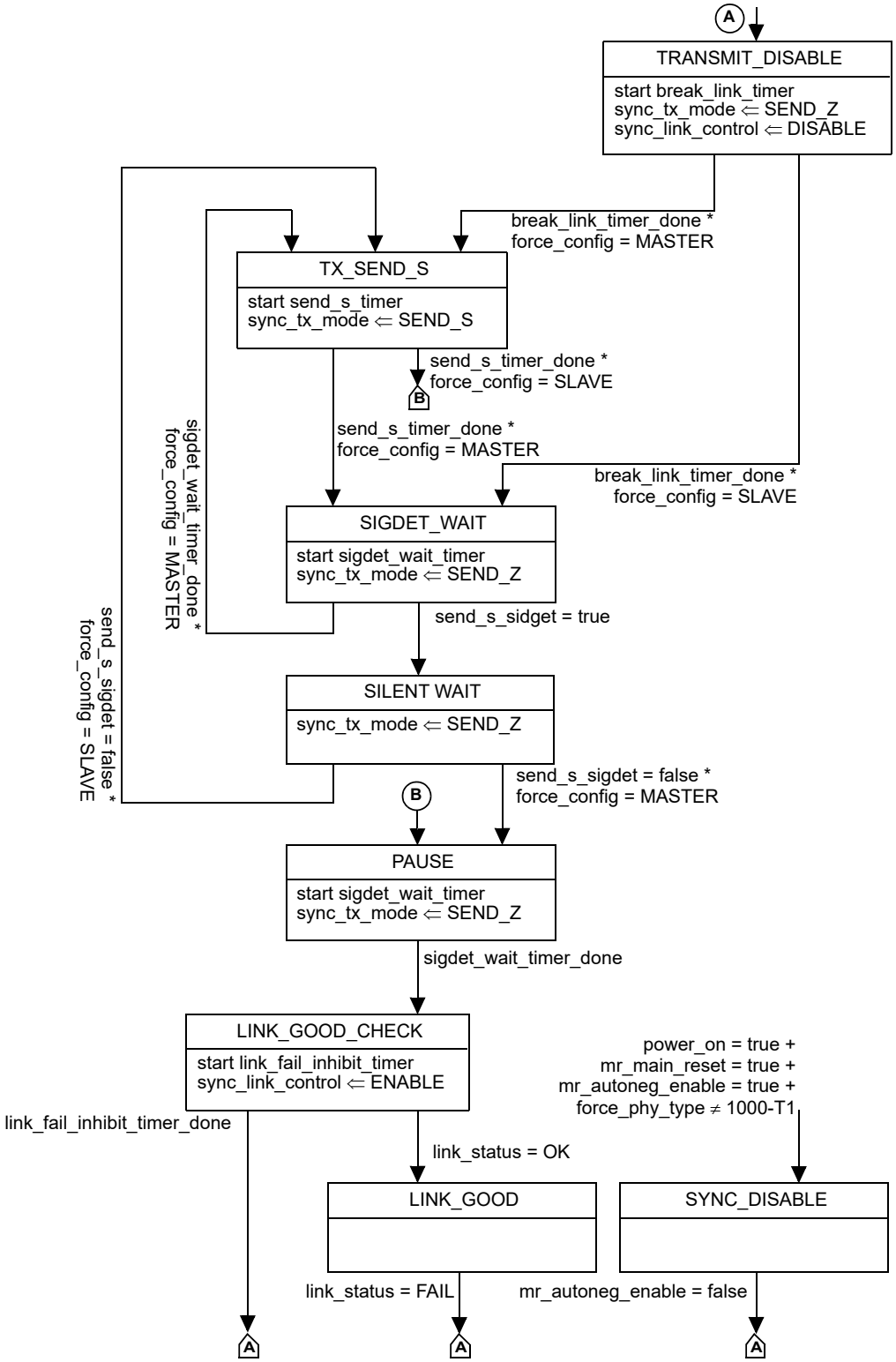

Figure 97–25—PHY Link Synchronization state diagram

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97.4.2.7 Refresh Monitor function

A 1000BASE-T1 PHY supporting the EEE capability shall implement the Refresh monitor function. The Refresh monitor operates when the PHY is in the LPI receive mode. If Refresh is not reliably detected within a moving window of 50 Q/R cycles (4.32 ms), the refresh monitor shall set PMA_refresh_status to FAIL, which sets link_status to FAIL. Subsequently the PHY restarts auto-negotiation (if auto-negotiation is enabled) or synchronization (if auto-negotiation is disabled). PMA_refresh_status shall be set to OK when the Link Monitor state diagram (Figure 97–27) enters the LINK_UP state.

97.4.2.8 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RS FER indicated in 97.4.2.3 is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by received_clock.

97.4.3 MDI

Communication through the MDI is summarized in 97.4.3.1 and 97.4.3.2.

97.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA are denoted by tx_symb. The modulation scheme used over each pair is PAM3. PMA Transmit generates a pulse-amplitude modulated signal on each pair in the following form:

$$s(t) = \sum_{n=0}^{\infty} a_n h_T(t - nT) \tag{97–10}$$

In Equation (97–10), a_n is the PAM3 modulation symbol from the set {–1, 0, 1} to be transmitted at time nT, and $h_T(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 97.5.

97.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise as follows:

$$r(t) = \sum_{n=0}^{\infty} a_n h_R(t - nT) + w(t) \tag{97–11}$$

In Equation (97–11) $h_R(t)$ denotes the symbol response of the overall channel impulse response between the transmit symbol source and the receive MDI and $w(t)$ represents the contribution of various noise sources including uncancelled echo. The receive signal is processed within the PMA Receive function to yield the received symbols rx_symb.

97.4.4 State variables

97.4.4.1 State diagram variables

auto_neg_imp
: This variable indicates if an optional Auto-Negotiation sublayer is associated with the PMA.
Values:
- true: An optional Auto-Negotiation sublayer is associated with the PMA
- false: An optional Auto-Negotiation sublayer is not associated with the PMA

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config

The PMA generates this variable continuously and passes it to the PCS via the PMA_CONFIG.indication primitive.

Values:

MASTER
SLAVE

en_slave_tx

The en_slave_tx variable in the InfoField received by the SLAVE.

Values:

0: Master is not ready for the SLAVE to transmit
1: Master is ready for the SLAVE to transmit

infofield_complete

This variable indicates that a complete set of InfoField messages has been sent (see 97.4.2.4).

Values:

false: a complete set of InfoField messages has not been sent
true: a complete set of InfoField messages has been sent

link_control

This variable is defined in 97.2.1.1.1.

link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

loc_phy_ready

This variable is set by the PMA Receive function to indicate the local PHY is ready or not ready to receive data. The value of loc_phy_ready is equal to OK only if loc_rcvr_status = OK and pcs_status = OK. Otherwise its value is NOT_OK. This variable is conveyed to the link partner by the PCS as defined in Table 97–1.

Values:

OK: the local PHY is ready to receive data
NOT_OK: the local PHY is not ready to receive data

loc_countdown_done

This variable is set to false when the PHY Control state diagram is in the DISABLE_TRANSMITTER state and is set to true immediately after transmitting the last bit of the DataSwPFC24–1 partial PHY frame.

loc_rcvr_status

Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY. This variable is transmitted in the loc_rcvr_status bit of the InfoField by the local PHY.

Values:

OK: the receive link for the local PHY is operating reliably
NOT_OK: operation of the receive link for the local PHY is unreliable

loc_SNR_margin

This variable reports whether the local device has sufficient SNR margin to continue to the next state. The criterion for setting the parameter loc_SNR_margin is left to the implementer.

Values:

OK: the local device has sufficient SNR margin
NOT_OK: the local device does not have sufficient SNR margin

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PMA_refresh_status

This variable indicates the status of the Refresh Monitor as described in 97.4.3.

Values:

OK: refresh is detected reliably

FAIL: refresh is not detected reliably

pma_reset

Allows reset of all PMA functions. It is set by PMA Reset.

Values:

ON

OFF

PMA_state

Variable for the value transmitted in the PMA_state<7:6> of the InfoField by the local PHY.

Values:

00: TRAINING state

01: COUNTDOWN state

PMA_watchdog_status

Variable indicating the status of the PAM3 monitor.

Values:

OK: the local device has received sufficient PAM3 transitions

NOT_OK: the local device has not received sufficient PAM3 transitions

During normal operation NOT_OK is assigned when:

— PAM3 symbol 0 consecutively seen on the line for longer than 2 μs ± 0.1 μs

— PAM3 symbol +1 consecutively seen on the line for longer than 3.9 μs ± 0.1 μs

— PAM3 symbol –1 consecutively seen on the line for longer than 3.9 μs ± 0.1 μs

During Low Power Idle operation NOT_OK is assigned when:

— PAM3 symbol not toggling on the line during one full refresh window

rem_countdown_done

This variable is set to false when the PHY Control state diagram is in the DISABLE_TRANSMITTER state or SILENT state and is set to true once the receiver has transitioned from PAM2 to PAM3 mode and has received a valid PHY frame containing all IDLEs.

rem_phy_ready

This variable is set by the PCS Receive function to indicate whether the remote PHY is ready or not ready to receive data. This variable is received from the link partner by the PCS as defined in Table 97–1. The variable retains its value until the next normal Inter-Frame idle is received.

Values:

OK: the remote PHY is ready to receive data

NOT_OK: the remote PHY is not ready to receive data

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not. This variable is received in the loc_rcvr_status bit in the InfoField from the remote PHY. This variable is set to NOT_OK if the PCS has not decoded a valid InfoField from the remote PHY.

Values:

OK: the receive link for the remote PHY is operating reliably

NOT_OK: reliable operation of the receive link for the remote PHY is not detected

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sync_link_control
This variable is defined in 97.4.2.6.1.

tx_mode
The PMA generates this variable continuously and passes it to the PCS via the PMA_TX-MODE.indication primitive.
Values:
SEND_N: this value is continuously asserted when transmission of sequences of symbols representing a GMII data stream take place
SEND_I: this value is continuously asserted when transmission of sequences of symbols representing an idle stream takes place
SEND_T: this value is continuously asserted when transmission of sequences of symbols representing the training sequences of symbols is to take place
SEND_Z: this value is asserted when transmission of zero symbols is to take place

97.4.4.2 Timers

All timers operate in the manner described in 14.2.3.2.

maxwait_timer
A timer used to limit the amount of time during which a receiver dwells in the SILENT and TRAINING states. The timer shall expire 97.5 ms ± 0.5 ms after being started.
This timer is used jointly in the PHY Control and Link Monitor state diagrams. The maxwait_timer is tested by the Link Monitor to force link_status to be set to FAIL if either of the following conditions is true:

— the PMA_watchdog_status is NOT_OK
— the timer expires and loc_phy_ready is NOT_OK
— the PMA_refresh_status is FAIL

See Figure 97–26 and Figure 97–27.

minwait_timer
A timer used to determine the minimum amount of time the PHY Control stays in the SILENT, TRAINING, SEND IDLE2, and SEND DATA states. The timer shall expire 975 µs ± 50 µs after being started.

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97.4.5 State diagrams

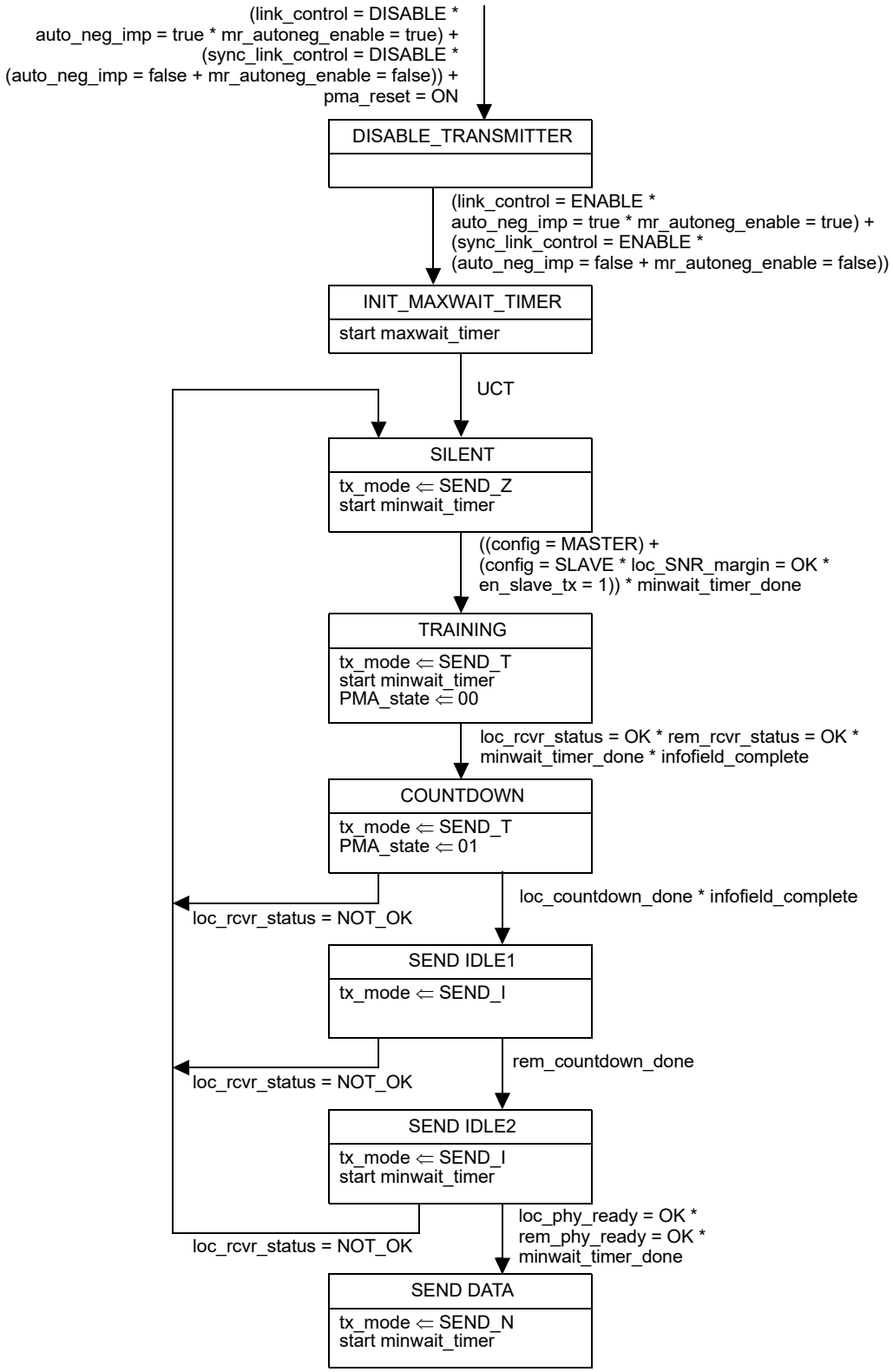

Figure 97–26—PHY Control state diagram

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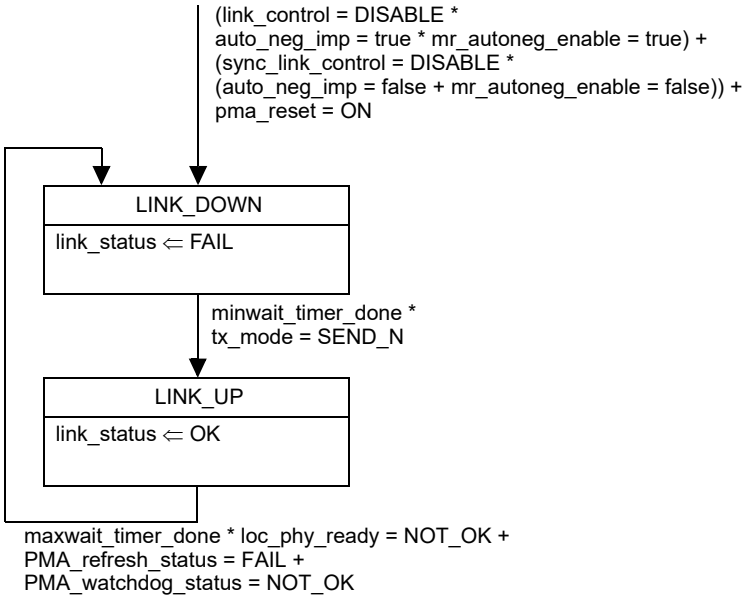

NOTE 1—maxwait_timer is started in PHY Control state diagram (see Figure 97–26).

NOTE 2—The variables link_control and link_status are designated as link_control_1GigT1 and link_status_1GigT1, respectively, by the Auto-Negotiation Arbitration state diagram (Figure 98–7) if the optional Auto-Negotiation function is implemented.

Figure 97–27—Link Monitor state diagram

97.5 PMA electrical specifications

This subclause specifies the electrical characteristics of the PMA for a 1000BASE-T1 Ethernet PHY.

97.5.1 EMC Requirements

See 96.5.1.

97.5.1.1 Immunity—DPI test

See 96.5.1.1.

97.5.1.2 Emission—150 Ω conducted emission test

See 96.5.1.2.

97.5.2 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER testing.

These test modes shall be enabled by setting a control register 1.2308.15:13 as shown in Table 97–12. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

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Table 97–12—MDIO management registers settings for test modes

Register value	Register description
000	Normal (non-test mode) operation.
001	Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
010	Test mode 2—Transmit MDI jitter test in MASTER mode.
011	Reserved.
100	Test mode 4—Transmit distortion test.
101	Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
110	Test mode 6—Transmitter droop test mode.
111	Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Test mode 1 enables testing of timing jitter on MASTER and SLAVE transmitters. MASTER and SLAVE 1000BASE-T1 PHYs are connected over a link segment defined in 97.6. When in this mode, the 1000BASE-T1 PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK125. This 125 MHz test clock is one sixth frequency divided version of TX_TCLK that times the transmitted symbols.

Test mode 2 is for transmitter jitter testing on MDI when transmitter is in MASTER timing mode. When test mode 2 is enabled, the 1000BASE-T1 PHY shall transmit a continuous pattern of three {+1} symbols followed by three {–1} symbols with the transmitted symbols timed from its local clock source of 750 MHz. The transmitter output is a 125 MHz signal.

Test mode 3 is not defined and the corresponding register is reserved for future use.

Test mode 4 is for transmitter linearity testing. When test mode 4 is enabled, 1000BASE-T1 PHY shall transmit the sequence of symbols generated by the scrambler generator polynomial per Equation (97–12).

$$g(x) = 1 + x^{9} + x^{11} \tag{97–12}$$

The maximum-length shift register used to generate the sequences defined by this polynomial shall be updated once per symbol interval (2/750 MHz). The bits stored in the shift register delay line at a particular time n are denoted by $Scr_n[10:0]$. At each symbol period the shift register is advanced by one bit and one new bit represented by $Scr_n[0]$ is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive ORed together to generate the next $Scr_n[0]$ bit. The bit sequences $x0_n$, $x1_n$, and $x2_n$ generated from combinations of the scrambler bits, as shown in Equation (97–13), shall be used to generate the ternary symbols, $T0_n$ and $T1_n$, as shown in Table 97–13. The transmitter shall time the transmitted symbols from a 750 MHz ± 0.01% clock in the MASTER timing mode. The transmit signal level and spectral shaping in this mode shall be same as normal (non-test) mode. A typical transmitter output for transmitter test mode 4 is shown in Figure 97–28.

$$\begin{aligned} x0_n &= Scr_n[0] \\ x1_n &= Scr_n[1] \wedge Scr_n[4] \\ x2_n &= Scr_n[1] \wedge Scr_n[5] \end{aligned} \tag{97–13}$$

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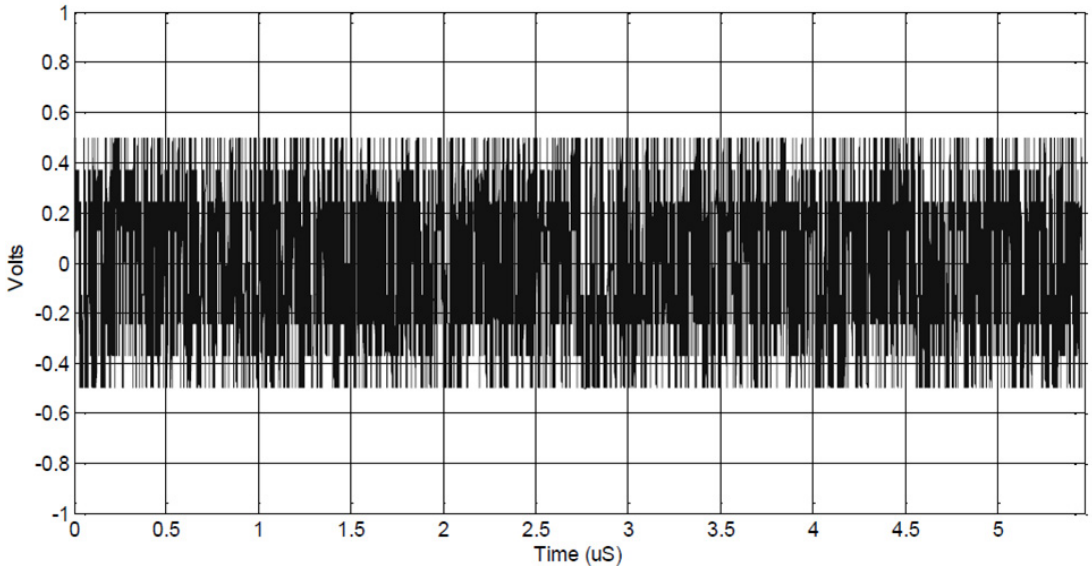

Figure 97–28—Typical transmitter output for transmitter test mode 4

Table 97–13—Transmit test mode 4 symbol mapping

$x2_n$	$x1_n$	$x0_n$	$T1_n$	$T0_n$
0	0	0	–1	–1
0	0	1	0	–1
0	1	0	–1	0
0	1	1	–1	+1
1	0	0	+1	0
1	0	1	+1	–1
1	1	0	+1	+1
1	1	1	0	+1

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, 1000BASE-T1 PHY shall transmit as in non-test operation and in the MASTER data mode with data set to normal Inter-Frame idle signals.

When test mode 6 is enabled, 1000BASE-T1 PHY shall transmit a continuous pattern of fifteen {+1} symbols followed by fifteen {–1} symbols with the transmitted symbols timed from its local clock source of 750 MHz. The transmitter output is a 25 MHz signal.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder / decoder, transmit and receive analog front ends of 1000BASE-T1 PHY, and a cable connecting two 1000BASE-T1 PHYs. This mode reuses the 1000BASE-T1 normal (non-test) mode with zero data pattern. Instead of encoding received data from MAC, continuous zero data pattern is encoded. In the receive side,

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after FEC and 80B/81B decoding, zero data sequence is expected with no error. Any non-zero data bit received is counted as error and calculated in BER.

97.5.2.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 97–29, Figure 97–30, Figure 97–31, Figure 97–32, and Figure 97–33, in stated respective tests, shall be used for measuring the transmitter specifications for data communication only. The tolerance of resistors shall be ± 0.1%.

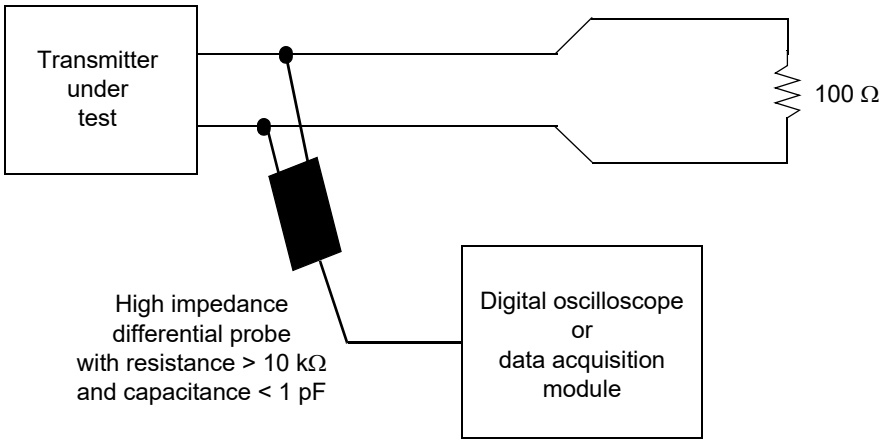

Figure 97–29—Transmitter test fixture 1 for transmitter droop measurement

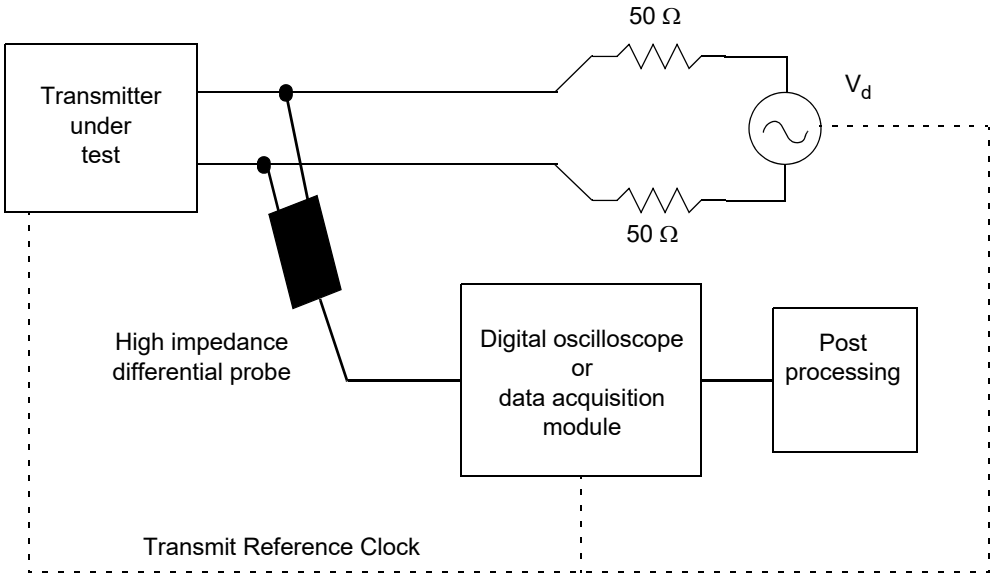

Figure 97–30—Transmitter test fixture 2 for transmitter distortion measurement

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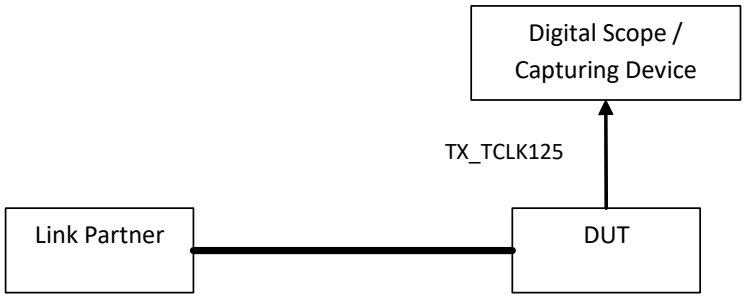

Figure 97–31—Transmitter test fixture 3 for MASTER and SLAVE clock jitter measurement

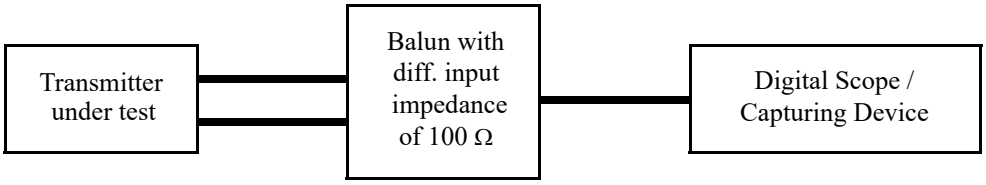

Figure 97–32—Transmitter test fixture 4 for MDI jitter measurement

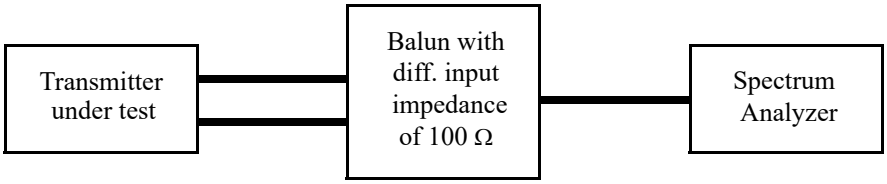

Figure 97–33—Transmitter test fixture 5 for power spectral density measurement and transmit power level measurement

97.5.3 Transmitter electrical specifications

The PMA provides the Transmit function specified in 97.4.2.2 in accordance with the electrical specifications of this clause. The PMA shall operate with AC coupling to the MDI. Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to the transmitter output.

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97.5.3.1 Maximum output droop

With the transmitter in test mode 6 and using the transmitter test fixture 1, the magnitude of both the positive and negative droop shall be less than 10%, measured with respect to an initial value at 4 ns after the zero crossing and a final value at 16 ns after the zero crossing (12 ns period).

97.5.3.2 Transmitter distortion

In Figure 97–30, the sinusoidal disturbing signal Vd, shall have amplitude of 3.6 V peak-to-peak differential, and frequency given by one-sixth of the symbol rate (125 MHz) synchronous with the test pattern. The generator of the disturbing signal shall have sufficient linearity and range so it does not introduce any appreciable distortion when connected to the transmitter output.

Transmitter distortion is measured by capturing the test mode 4 waveform using transmitter test fixture 2. The peak distortion is determined by sampling the differential signal output with the symbol rate clock at an arbitrary phase and processing a block of consecutive samples with pseudo-code given below or an equivalent. The captured block of signal shall be at least 40 μs long and be sampled with the minimum sampling rate of 7.5 Gs/s (10 times the transmit symbol rate of 750 Ms/s).

The peak distortion values, measured at a minimum of 10 equally spaced phases of a single symbol period, shall be less than 15 mV. Notice the peak signal level is normalized to 1 V in the processing code. The pseudo-code removes the sinusoidal disturbing signal from the measured data and computes the peak distortion. The code assumes the disturber signal and the data acquisition clock are frequency locked to the DUT transmit clock.

```
% Post processing pseudo-code for 1000BASE-T1 transmitter distortion
clear
Ns=2^11-1; % Scrambler length
Nc=70;  % Canceller length

% Generate scrambler sequence
scr=ones(Ns,1);
for i=12:Ns
  scr(i)=mod(scr(i-11) + scr(i-9),2);
end

% 1000BASE-T1 2D-PAM3 assignment
tm4=ones(Ns,1);
map=[-1 -1;-1 0;0 -1;1 -1;0 1;-1 1;1 1;1 0];
scr3=[scr, mod(circshift(scr,1) + circshift(scr,4),2),...
   mod(circshift(scr,1) + circshift(scr,5),2)];
data = 4*scr3(:,3)+ 2*scr3(:,2)+scr3(:,1);
for n=1:length(data)
   tm4([2*n-1,2*n]) =map(data(n)+1,:);
end
Ns=2*Ns;

% Test mode4 matrix
for i=1:Nc
    X0(i,:)=circshift(tm4,1-i);
end

% Read captured data file, 40us long, 7.5GSample/sec, high resolution capture
fid=fopen('RawData.bin','r');
tx = fread(fid,inf,'double');
fclose(fid);

% LPF 375MHz
[A,B]=butter(2,1/10,'low');
tx=filter(A,B,tx);
```


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```
% HPF 12MHz
tx = filter([1,-1],[1,-exp(-2*pi/625)],tx);

% Select six periods, 10x oversampling, a row vector
tx=tx((1:6*Ns*10)+2e3)'; % removes HPF transient

% Disturber removal and integration (average) of six periods
TX=fft(tx);
tx=ifft(TX(1:6:end));

% Level normalization to 1V
tx=tx/(max(tx)-min(tx))*2;

% Compute distortion for 10 clock phases
for n=1:10
tx1=tx(n:10:end);

% Align data and test pattern
temp=xcorr(tx1,tm4);
index=find(abs(temp)==max(abs(temp)));
X=circshift(X0, [0, mod(index(1)+Nc-10,Ns)]);

% Compute coefficients that minimize squared error
coef=tx1/X;

% Linear canceller
err=tx1-coef*X;

% Peak distortion
dist(n) = max(abs(err));
end

% Print distortion in mV (normalized) for 10 sampling phases
format bank
peakDistortion_mV = 1000*dist'
```

97.5.3.3 Transmitter timing jitter

The transmitter timing jitter is measured by capturing the TX_TCLK125 waveform in both MASTER and SLAVE configurations while in test mode 1 using the transmitter test fixture 3 shown in Figure 97–31.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the MASTER TX_TCLK125 jitter relative to an unjittered reference shall be less than 5 ps. The peak-to-peak value of the MASTER TX_TCLK125 jitter relative to an unjittered reference shall be less than 50 ps.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the SLAVE TX_TCLK125 jitter relative to an unjittered reference shall be less than 10 ps. The peak-to-peak value of the SLAVE TX_TCLK125 jitter relative to an unjittered reference shall be less than 100 ps.

TX_TCLK125 jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the capturing device shall be larger than 2 MHz. The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK125. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

For PHYs supporting LPI mode, in order for the transmit jitter to be similar to normal power mode operation, the clock reference used to clock transmit-symbols shall be continuous going from normal power mode into and out of LPI mode.

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 and using test fixture 4 as shown in Figure 97–32. The RMS value of the MDI output jitter relative to an unjittered

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reference shall be less than 5 ps. The peak-to-peak value of the MDI output jitter relative to an unjittered reference shall be less than 50 ps. Jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the measurement device shall be larger than 2 MHz. Unjittered reference is a constant clock frequency extracted from each record of captured differential output on MDI. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

$$UpperPSD(f) = \begin{cases} -80 & \text{dBm/Hz} \quad 0 < f \le 100 \\ -76 - \frac{f}{25} & \text{dBm/Hz} \quad 100 < f \le 400 \\ -85.6 - \frac{f}{62.5} & \text{dBm/Hz} \quad 400 < f \le 600 \end{cases} \tag{97–14}$$

$$LowerPSD(f) = \begin{cases} -86 & \text{dBm/Hz} \quad 40 < f \le 100 \\ -82 - \frac{f}{25} & \text{dBm/Hz} \quad 100 < f \le 400 \end{cases} \tag{97–15}$$

where

f is the frequency in MHz

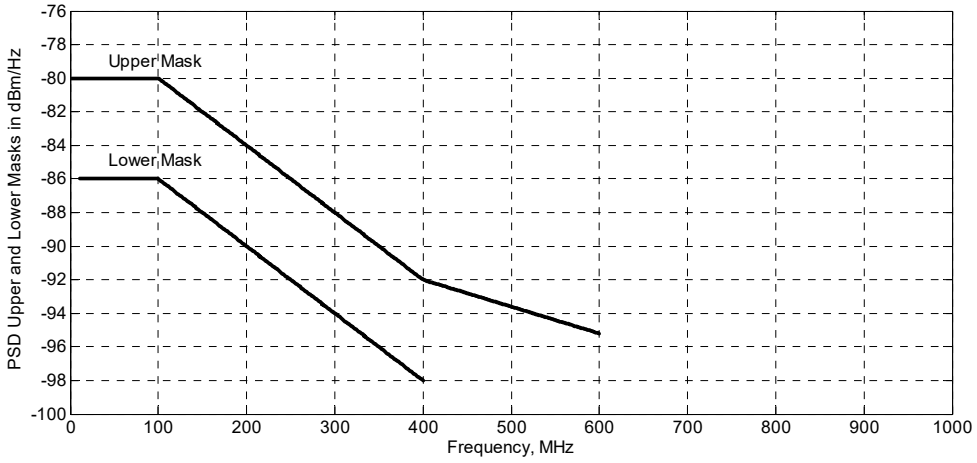

Figure 97–34—Transmitter Power Spectral Density, upper and lower masks

97.5.3.4 Transmitter Power Spectral Density (PSD) and power level

In test mode 5 (normal operation), the transmit power shall be less than 5 dBm and the power spectral density of the transmitter, measured into a 100 Ω load using the test fixture 5 shown in Figure 97–33 shall be between the upper and lower masks specified in Equation (97–14) and Equation (97–15). The masks are shown in Figure 97–34. The measurements need to be calibrated for insertion loss of the differential Balun used in the test. The resolution bandwidth of 100 kHz and sweep time of larger than 1 second are considered in PSD measurement.

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97.5.3.5 Transmitter peak differential output

When measured with 100 Ω termination, transmit differential signal at MDI shall be less than 1.30 V peak-to-peak. This limit applies to all transmit modes including SEND_S, SEND_T, SEND_I, and SEND_N modes.

97.5.3.6 Transmitter clock frequency

The symbol transmission rate of the MASTER PHY shall be within the range 750 MHz ± 100 ppm.

For a MASTER PHY, when the transmitter is in the LPI transmit mode, the transmitter clock short-term rate of frequency variation shall be less than 0.1 ppm/second. The short-term frequency variation limit shall also apply when switching to and from the LPI mode.

97.5.4 Receiver electrical specifications

97.5.4.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 97.5.3 and have passed through a link segment type A (specified in 97.6.1 and 97.6.3) are received with a BER less than 10^{-10} and sent to the PCS after link reset completion. This BER specification shall be satisfied by a frame loss ratio less than 10^{-7} for 125-octet frames. Operation on link segment type B is optional. If supported, the frame loss ratio shall also be met for link segments specified at 97.6.2 and 97.6.4.

97.5.4.2 Alien crosstalk noise rejection

This specification is provided to verify the receiver's tolerance to alien crosstalk noise. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidth of 550 MHz and magnitude of –100 dBm/Hz for devices supporting type A link segments and –110 dBm/Hz for devices supporting type B link segments. The receive DUT is connected to these noise sources through a resistive network, as shown in Figure 97–35, with a link segment as defined in 97.6. The noise is added at the MDI of the DUT. The BER is expected to be less than 10^{-10}, and to satisfy this specification the frame loss ratio is less than 10^{-7} for 125-octet packets measured at MAC/PLS service interface.

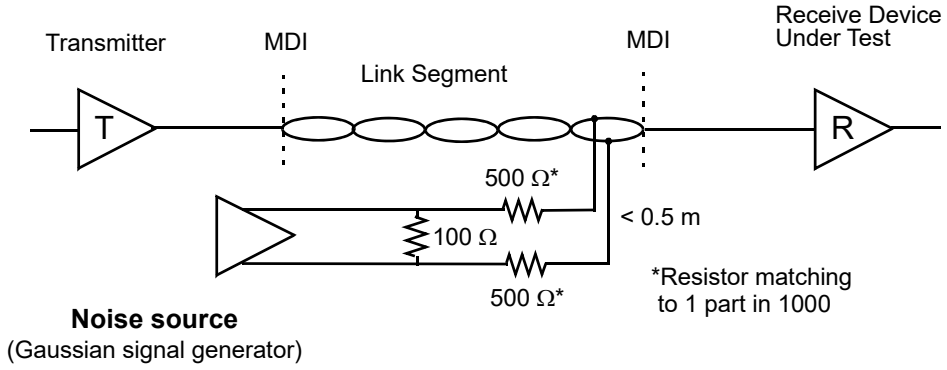

Figure 97–35—Alien crosstalk noise rejection test setup

97.6 Link segment characteristics

1000BASE-T1 is designed to operate over a single twisted-pair copper cable that meets the requirements specified in this subclause. The single twisted-pair copper cable supports an effective data rate of 1 Gb/s in

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each direction simultaneously. The term *link segment* used in this clause refers to a single twisted-pair copper cable operating in full duplex.

The following two link segments are specified:

a) A link segment optimized for use in automotive applications that supports up to four in-line connectors using a single twisted-pair copper cable for up to at least 15 m. This link segment is referred to as *link segment type A*.

b) An optional link segment supporting up to four in-line connectors using a single twisted-pair copper cable for up to at least 40 m to support applications requiring additional physical reach, such as industrial and automation controls and transportation (aircraft, railway, bus, and heavy trucks). This link segment is referred to as *link segment type B*.

97.6.1 Link transmission parameters for link segment type A

The transmission characteristics for type A link segment are specified to support operation over automotive temperature and electromagnetic conditions.

97.6.1.1 Insertion loss

The insertion loss of each type A link segment shall meet the values determined using Equation (97–16).

$$\text{InsertionLoss}(f) \le 0.0023f + 0.5907\sqrt{f} + 0.0639/\sqrt{f} \quad \text{dB} \tag{97–16}$$

where

f is the frequency in MHz; $1 \le f \le 600$

The insertion loss for the link segment calculated using Equation (97–16) accounts for the insertion loss of a single twisted-pair copper cable and four in-line connectors within each link segment. The insertion loss is illustrated in Figure 97–36.

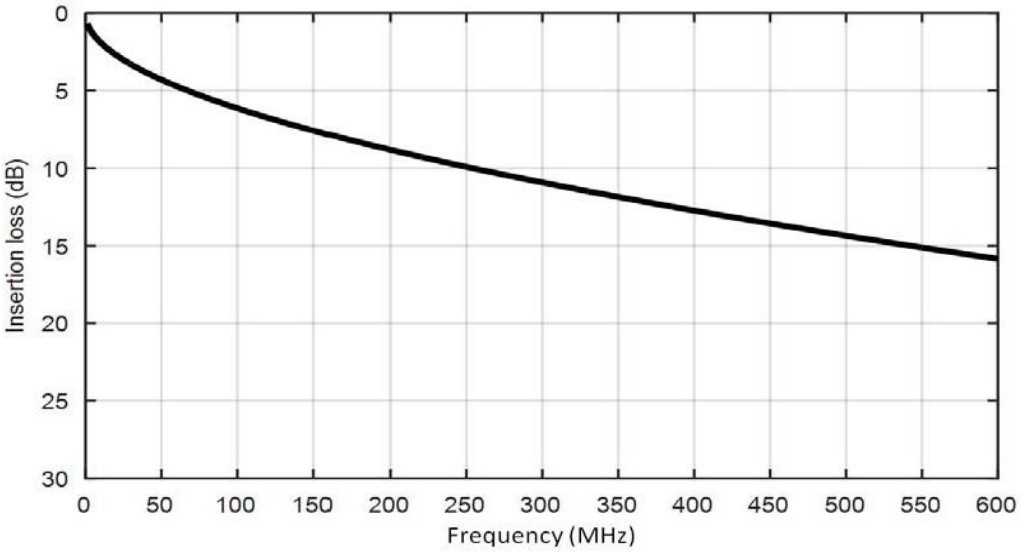

Figure 97–36—Insertion loss calculated using Equation (97–16)

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97.6.1.2 Differential characteristic impedance

The nominal differential characteristic impedance of each type A link segment is 100 Ω for all frequencies between 1 MHz and 600 MHz.

97.6.1.3 Return loss

In order to limit the noise at the receiver due to impedance mismatches each type A link segment shall meet the values determined using Equation (97–17) at all frequencies from 1 MHz to 600 MHz. The reference impedance for the return loss specification is 100 Ω.

$$\text{Return Loss} \geq \begin{cases} 19 & 1 \leq f < 10 \\ 24 - 5\log_{10} f & 10 \leq f < 40 \\ 16 & 40 \leq f < 130 \\ 37 - 10\log_{10} f & 130 \leq f < 400 \\ 11 & 400 \leq f \leq 600 \end{cases} \text{ dB} \qquad (97\text{–}17)$$

where

f is the frequency in MHz; $1 \leq f \leq 600$

The return loss is illustrated in Figure 97–37.

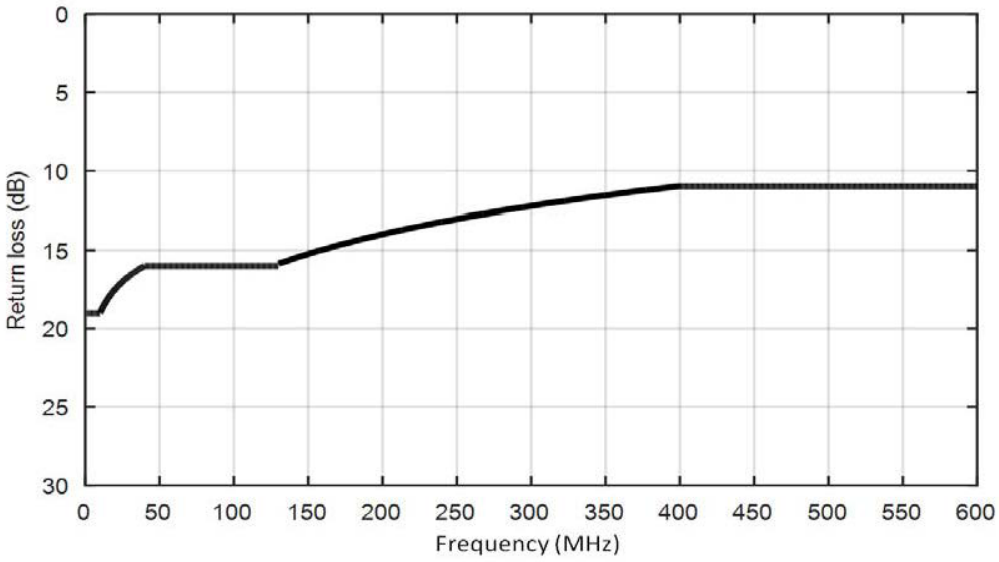

Figure 97–37—Return loss calculated using Equation (97–17)

97.6.1.4 Differential-to-common-mode conversion

The balance of the type A link segment is characterized by the differential-to-common-mode conversion. Each type A link segment shall meet the values determined using Equation (97–18) at all frequencies from 10 MHz to 600 MHz.

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$$\text{ConversionLoss}(f) \geq \left\{ \begin{array}{ll} 50 & 10 \leq f \leq 80 \\ 72 - 11.51\log_{10} f & 80 < f \leq 600 \end{array} \right\} \text{ dB} \quad (97\text{–}18)$$

where

f is the frequency in MHz; $10 \leq f \leq 600$

The function ConversionLoss(f) represents the mode conversion loss at frequency f. The conversion loss is illustrated in Figure 97–38.

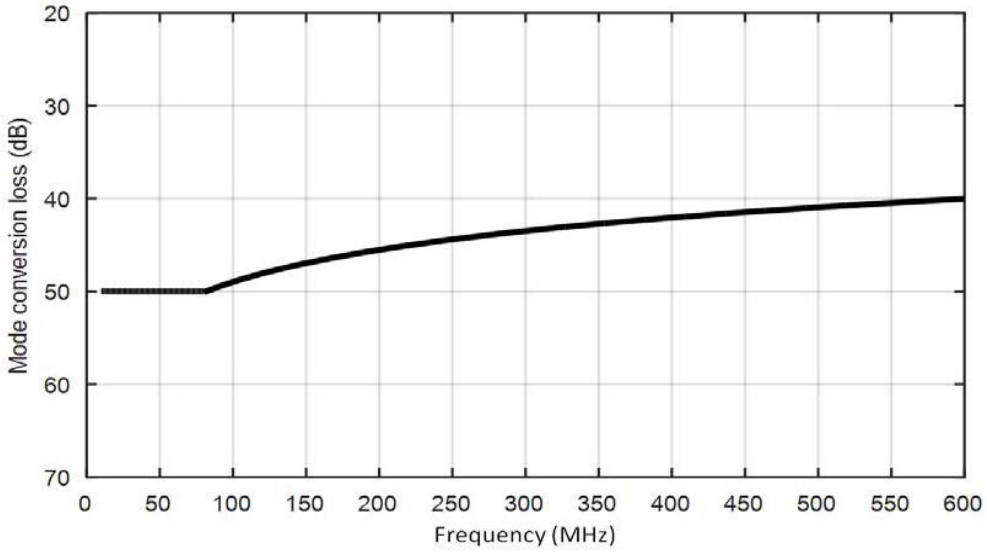

Figure 97–38—Conversion loss calculated using Equation (97–18)

The mode conversion specification applies to the following:

- Longitudinal conversion loss (LCL) with s-parameter SDC11/SDC22 and description common-to-differential-mode return loss
- Transverse conversion loss (TCL) with s-parameter SCD11/SCD22 and description differential-to-common-mode return loss
- Longitudinal conversion transmission loss (LCTL) with s-parameter SDC12/SDC21 and description common-to-differential-mode insertion loss
- Transverse conversion transmission loss (TCTL) with s-parameter SCD12/SCD21 and description differential-to-common-mode insertion loss

For compliance to the specification measurements of LCL and LCTL are sufficient as LCL and TCL are considered reciprocal and LCTL and TCTL are considered reciprocal. The differential-to-common-mode conversion loss test methodologies are specified in Annex 97A.

97.6.1.5 Maximum link delay

The propagation delay of a type A link segment shall not exceed 94 ns at all frequencies between 2 MHz and 600 MHz.

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97.6.2 Link transmission parameters for link segment type B

The transmission characteristics for type B link segment are specified to support applications requiring additional reach such as industrial and automation controls and transportation (aircraft, railway, bus, and heavy trucks) for up to at least 40 m. Type B link segment may be shielded or screened, consistent with the specification in 97.6.2.5 and 97.6.4.

97.6.2.1 Insertion loss

The insertion loss of each type B link segment shall meet the values determined using Equation (97–19).

$$\text{InsertionLoss}(f) \le 0.7131\sqrt{f} + 0.0040f + (0.1100/\sqrt{f}) + 0.08\sqrt{f} + 0.018\sqrt{f} \quad \text{dB} \qquad (97\text{–}19)$$

where

f is the frequency in MHz; $1 \le f \le 600$

The insertion loss is illustrated in Figure 97–39.

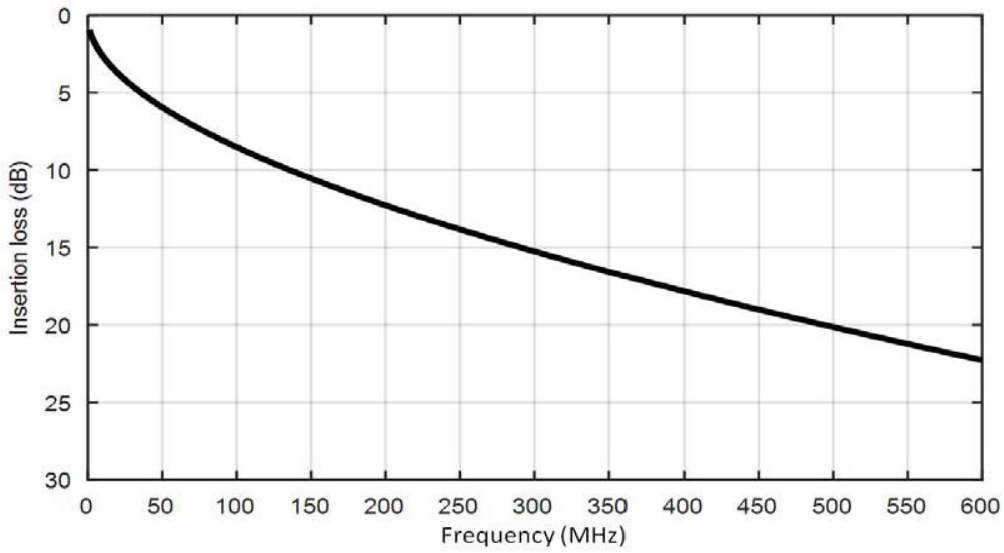

Figure 97–39—Insertion loss calculated using Equation (97–19)

The insertion loss for the link segment calculated using Equation (97–19) accounts for the insertion loss of a single twisted-pair copper cable and four in-line connectors within each link segment.

97.6.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each type B link segment is 100 Ω for all frequencies between 1 MHz and 600 MHz.

97.6.2.3 Return loss

In order to limit the noise at the receiver due to impedance mismatches each type B link segment shall meet the values determined using Equation (97–20) at all frequencies from 1 MHz to 600 MHz. The reference impedance for the return loss specification is 100 Ω.

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$$\text{Return Loss} \geq \left\{ \begin{array}{cc} 19 & 1 \leq f < 10 \\ 24 - 5\log_{10}(f) & 10 \leq f < 40 \\ 16 & 40 \leq f < 130 \\ 37 - 10\log_{10}(f) & 130 \leq f < 400 \\ 11 & 400 \leq f \leq 600 \end{array} \right\} \text{ dB} \qquad (97\text{–}20)$$

where

f is the frequency in MHz; $1 \leq f \leq 600$

The return loss is illustrated in Figure 97–40.

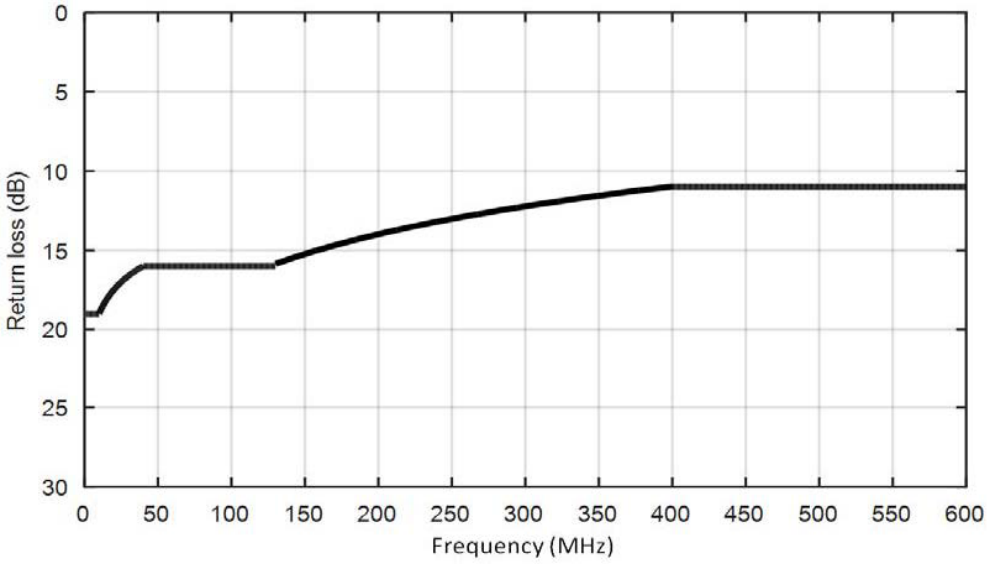

Figure 97–40—Return loss calculated using Equation (97–20)

97.6.2.4 Maximum link delay

The propagation delay of a type B link segment shall not exceed 234 ns at all frequencies between 2 MHz and 600 MHz.

97.6.2.5 Coupling attenuation

The coupling attenuation requirements of the type B link segment depend on the electromagnetic noise environment. The requirements in Table 97–14 shall be met based on the local environment as described by the electromagnetic classifications given in Table 97–15, E_1, E_2, or E_3. The coupling attenuation is tested as specified in IEC 62153-4–14.

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Table 97–14—Coupling attenuation Type B link segment

Frequency (MHz)	Minimum (dB)		
	E_1	E_2	E_3
$30 \le f \le 600$	$80 - 20\log_{10}(f)$ (Max 40 dB)	$90 - 20\log_{10}(f)$ (Max 50 dB)	$100 - 20\log_{10}(f)$ (Max 60 dB)

Table 97–15—Electromagnetic classifications Type B link segment

Electromagnetic	Minimum (dB)		
	E_1	E_2	E_3
Radiated RF – AM	3 V/m at (80 MHz to 1000 MHz) 3 V/m at (1400 MHz to 2000 MHz) 1 V/m at (2000 MHz to 2700 MHz)	3 V/m at (80 MHz to 1000 MHz) 3 V/m at (1400 MHz to 2000 MHz) 1 V/m at (2000 MHz to 2700 MHz)	10 V/m at (80 MHz to 1000 MHz) 3 V/m at (1400 MHz to 2000 MHz) 1 V/m at (2000 MHz to 2700 MHz)
Conducted RF	3 V at 150 kHz to 80 MHz	3 V at 150 kHz to 80 MHz	10 V at 150 kHz to 80 MHz

97.6.3 Coupling parameters between type A link segments

Noise coupled between the disturbed type A link segment and the disturbing type A link segment is referred to as *alien crosstalk noise*. To ensure the total alien NEXT loss and alien FEXT loss coupled between type A link segments is limited, multiple disturber alien near-end crosstalk (MDANEXT) loss and multiple disturber alien FEXT (MDAFEXT) loss is specified. The test methodologies are specified in Annex 97A and Annex 97B.

97.6.3.1 Multiple disturber alien near-end crosstalk (MDANEXT) loss

In order to limit the alien crosstalk at the near end of a type A link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between the disturbed type A link segment and the disturbing type A link segment is specified to meet the bit error ratio objective. To ensure the total alien NEXT coupled into a type A link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT disturbers.

97.6.3.2 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

PSANEXT loss is determined by summing the power of the individual pair-to-pair differential alien NEXT loss values over the frequency range 1 MHz to 600 MHz as follows in Equation (97–21).

$$\mathrm{PSANEXTloss}_N(f) \ge -10\log_{10}\left(\sum_{j=1}^{m} 10^{\frac{-\mathrm{AN}(f)_{j,N}}{10}}\right) \mathrm{dB} \qquad (97\text{–}21)$$

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where the function $AN(f)_{j,N}$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing type A link segment j (1 to m) for the disturbed type A link segment N.

The power sum ANEXT loss between a disturbed type A link segment and the disturbing type A link segment shall meet the values determined using Equation (97–22).

$$\text{PSANEXT}loss(f) \geq \left\{ \begin{array}{ll} 54 - 10\log_{10}\left(\frac{f}{100}\right) & 1 \leq f \leq 100 \\ 54 - 15\log_{10}\left(\frac{f}{100}\right) - 6\left(\frac{f-100}{400}\right) & 100 < f \leq 600 \end{array} \right\} \text{ dB} \quad (97\text{–}22)$$

where

f is the frequency in MHz

PSANEXT is illustrated in Figure 97–41.

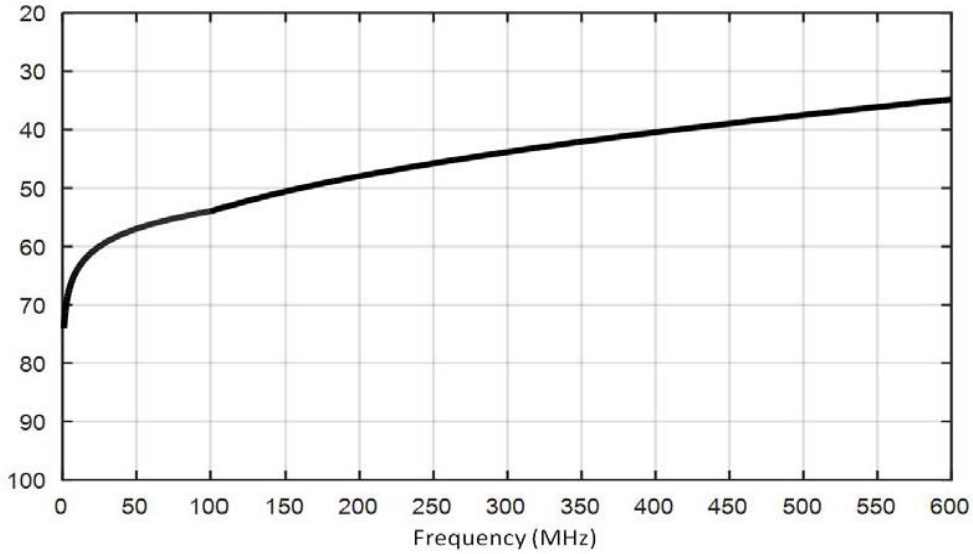

Figure 97–41—PSANEXT calculated using Equation (97–22)

97.6.3.3 Multiple disturber alien far-end crosstalk (MDAFEXT) loss

In order to limit the alien crosstalk at the far-end of a type A link segment, the differential pair-to-pair alien far-end crosstalk (FEXT) loss between the disturbed type A link segment and the disturbing type A link segment is specified to meet the bit error ratio objective. To ensure the total alien FEXT coupled into a type A link segment, multiple disturber attenuation to crosstalk ratio far-end ACRF is specified as the power sum of the individual alien ACRF disturbers.

97.6.3.4 Multiple disturber power sum alien attenuation crosstalk ratio far-end (PSAACRF)

PSAACRF is determined by summing the power of the individual pair-to-pair differential alien ACRF values over the frequency range 1 MHz to 600 MHz as follows in Equation (97–23).

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$$\mathrm{PSAACRF}_N(f) \geq -10\log_{10}\left(\sum_{j=1}^{m} 10^{\frac{-\mathrm{AF}(f)_{j,N}}{10}}\right) \text{ dB} \qquad (97\text{–}23)$$

where the function $\mathrm{AF}(f)_{j,N}$ represents the magnitude (expressed in dB) of the alien ACRF of the disturbing type A link segment j (1 to m) for disturbed type A link segment N.

The power sum AACRF between a disturbed type A link segment and the disturbing type A link segment shall meet the values determined using Equation (97–24).

$$\mathrm{PSAACRF}(f) \geq -20\log_{10}\left(10^{\frac{(-10)\log_{10}0.15 + 38.2 - 20\log_{10}\left(\frac{f}{100}\right)}{-20}} + 4 \times 10^{\frac{67 - 20\log_{10}\left(\frac{f}{100}\right)}{-20}}\right) \text{ dB} \qquad (97\text{–}24)$$

where

f is the frequency in MHz

PSAACRF is illustrated in Figure 97–42.

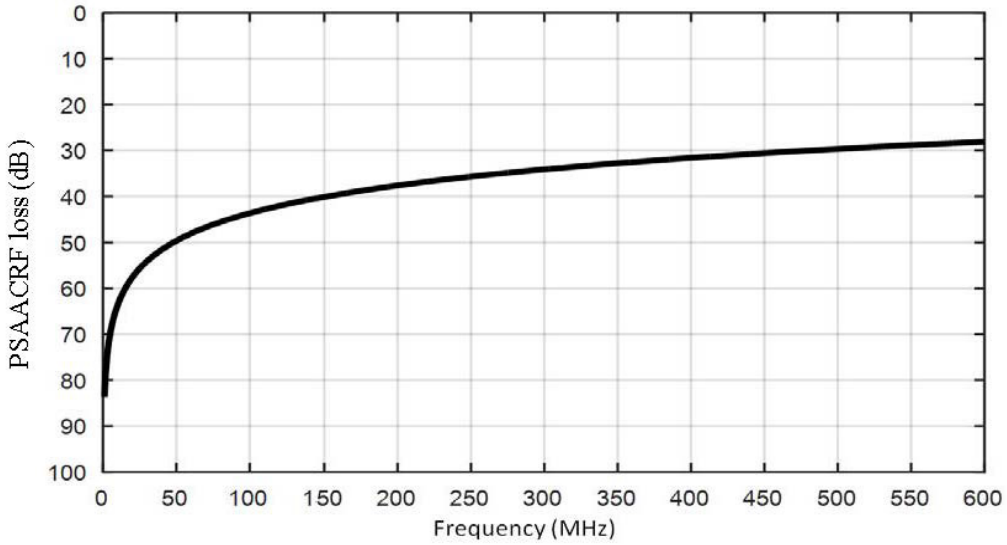

Figure 97–42—PSAACRF calculated using Equation (97–24)

97.6.4 Coupling parameters between type B link segments

Noise coupled between the disturbed type B link segment and the disturbing type B link segment is referred to as alien crosstalk noise. To ensure the total alien NEXT loss and alien FEXT loss coupled between type B link segments is limited, multiple disturber alien near-end crosstalk (MDANEXT) loss and multiple disturber alien FEXT (MDAFEXT) loss is specified.

97.6.4.1 Multiple disturber alien near-end crosstalk (MDANEXT) loss

In order to limit the alien crosstalk at the near end of a type B link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between the disturbed type B link segment and the disturbing type B link segment is specified to meet the bit error ratio objective. To ensure the total alien NEXT coupled into a type B link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT disturbers.

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97.6.4.2 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

PSANEXT loss is determined by summing the power of the individual pair-to-pair differential alien NEXT loss values over the frequency range 1 MHz to 600 MHz as follows in Equation (97–25).

$$\mathrm{PSANEXT}_N(f) \geq -10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AN}(f)_{j,N}}{10}} \ \mathrm{dB} \qquad (97–25)$$

where the function $\mathrm{AN}(f)_{j,N}$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing type B link segment j (1 to m) for the disturbed type B link segment N.

The power sum ANEXT loss between a disturbed type B link segment and the disturbing type B link segment shall meet the values determined using Equation (97–26).

$$\mathrm{PSANEXT}(f) \geq 65 \ \mathrm{dB} \qquad (97–26)$$

where

f is the frequency in MHz; $1 \leq f \leq 600$

97.6.4.3 Multiple disturber alien far-end crosstalk (MDAFEXT) loss

In order to limit the alien crosstalk at the far-end of a type B link segment, the differential pair-to-pair alien far-end crosstalk (FEXT) loss between the disturbed type B link segment and the disturbing type B link segment is specified to meet the bit error ratio objective. To ensure the total alien FEXT coupled into a type B link segment, multiple disturber attenuation to crosstalk ratio far-end ACRF is specified as the power sum of the individual alien ACRF disturbers.

97.6.4.4 Multiple disturber power sum alien attenuation crosstalk ratio far-end (PSAACRF)

PSAACRF is determined by summing the power of the individual pair-to-pair differential alien ACRF values over the frequency range 1 MHz to 600 MHz as follows in Equation (97–27).

$$\mathrm{PSAACRF}_N(f) \geq -10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AF}(f)_{j,N}}{10}} \ \mathrm{dB} \qquad (97–27)$$

where the function $\mathrm{AF}(f)_{j,N}$ represents the magnitude (expressed in dB) of the alien ACRF of the disturbing type B link segment j (1 to m) for disturbed type B link segment N.

The power sum AACRF between a disturbed type B link segment and the disturbing type B link segment shall meet the values determined using Equation (97–28) or 70 dB, whichever is less.

$$\mathrm{PSAACRF}(f) \geq 61 - 20\log_{10}(f/100) \ \mathrm{dB} \qquad (97–28)$$

where

f is the frequency in MHz; $1 \leq f \leq 600$

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97.7 Media Dependent Interface (MDI)

97.7.1 MDI connectors

The mechanical interface to the balanced cabling is a 2-pin connector or 2 pins of a multi-pin connector. Further specification of the mechanical interface is beyond the scope of this standard.

97.7.2 MDI electrical specification

The electrical requirements specified in 97.5.3 and 97.5.4 shall be met when the PHY is connected to the MDI connector mated with a specified balanced twisted-pair cable connector.

97.7.2.1 MDI return loss

The differential impedance at the MDI (see Figure 97–43) for each transmit/receive channel shall be such that any reflection (due to differential signals incident upon the MDI with a test port having a differential impedance of 100 Ω) is attenuated relative to the incident signal per Equation (97–29).

$$\text{Return Loss}(f) \geq \begin{cases} 18 - 18\log_{10}\frac{20}{f} & 2 \leq f < 20 \\ 18 & 20 \leq f < 100 \\ 18 - 16.7\log_{10}\frac{f}{100} & 100 \leq f \leq 600 \end{cases} \text{ dB} \qquad (97\text{–}29)$$

where f is the frequency in MHz.

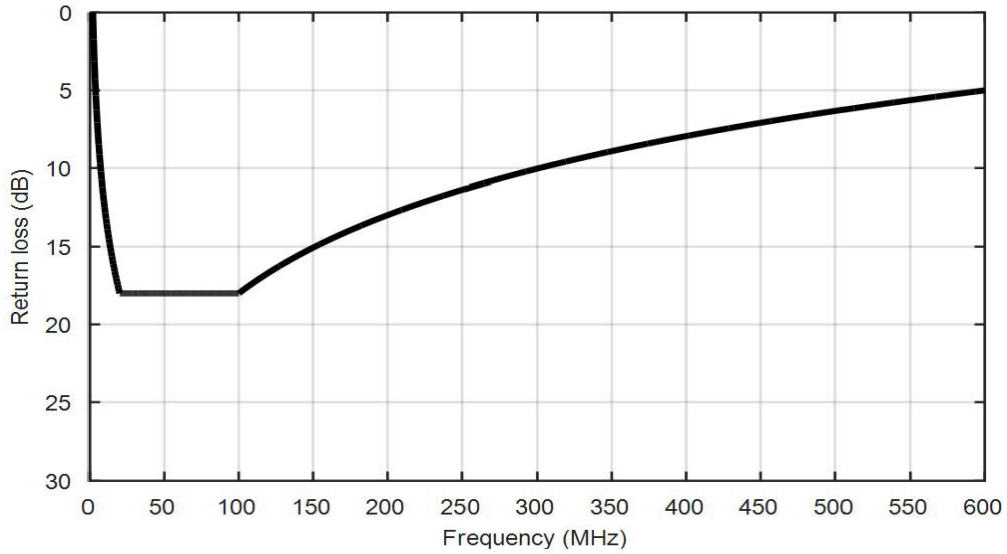

Figure 97–43—Return loss calculated using Equation (97–29)

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97.7.2.2 MDI mode conversion loss

Mode conversion LCL (Sdc11) or TCL (Scd11) of the PHY measured at MDI shall meet the values determined using Equation (97–30) at all frequencies from 10 MHz to 600 MHz.

$$\text{ConversionLoss}(f) \geq \left\{ \begin{array}{cc} 55 & 10 \leq f \leq 80 \\ 77 - 11.51\log_{10} f & 80 < f \leq 600 \end{array} \right\} \text{dB} \quad (97–30)$$

where

f is the frequency in MHz; $10 \leq f \leq 600$

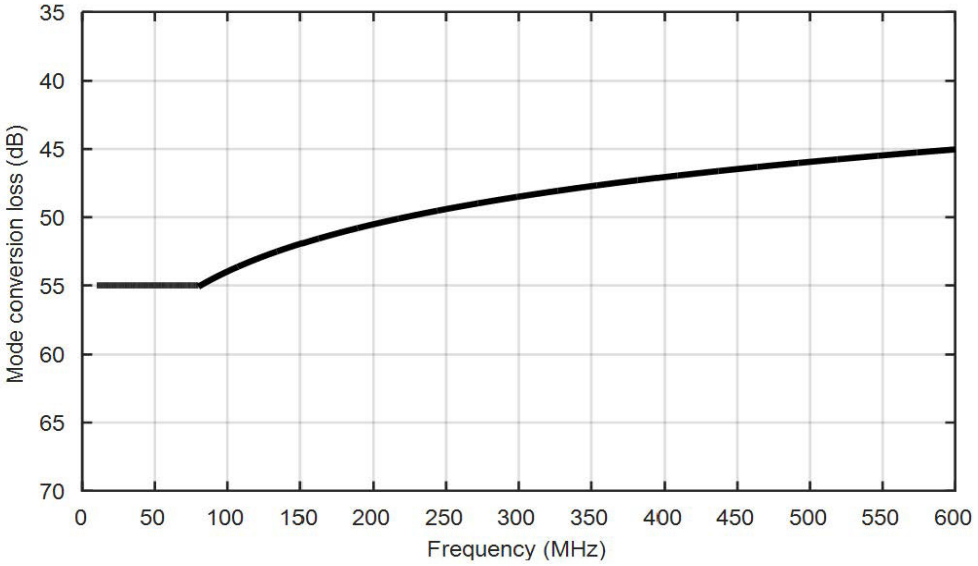

Figure 97–44—MDI mode conversion loss calculated using Equation (97–30)

97.7.3 MDI fault tolerance

See 96.8.3.

97.8 Management Interfaces

1000BASE-T1 makes extensive use of the management functions that may be provided by the MDIO (Clause 45), and the communication and self-configuration functions provided by the optional Auto-Negotiation (Clause 98).

97.8.1 Optional Support for Auto-Negotiation

If Auto-Negotiation is supported and enabled the mechanism described in Clause 98 shall be used.

Auto-Negotiation is performed as part of the initial setup of the link, and allows the PHYs at each end to advertise their capabilities and to automatically select the operating mode for communication on the link. Auto-Negotiation signaling is used for the following primary purposes for 1000BASE-T1:

a) To negotiate that the PHY is capable of supporting 1000BASE-T1 transmission

b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link

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97.9 Environmental specifications

97.9.1 General safety

All equipment subject to this clause is expected to conform to all applicable local, state, national, and application-specific standards.

97.9.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner. In automotive applications, all 1000BASE-T1 cabling is routed in way to provide maximum protection by the motor vehicle sheet metal and structural components, following SAE J1292, ISO 14229, and ISO 15764.

97.9.2.1 Environmental safety

All equipment subject to this clause, when used in the automotive environment, shall conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications:

a) General loads: ISO 16750–1
b) Electrical loads: ISO 16750-2, ISO 7637-2:2008, and ISO 8820–1
c) Mechanical loads: ISO 16750-3, ASTM D4728, and ISO 12103–1
d) Climatic loads: ISO 16750-4, IEC 60068-2-1, IEC 60068-2-27, IEC 60068-2-30, IEC 60068-2-38, IEC 60068-2-52, IEC 60068-2-64, and IEC 60068-2-78
e) Chemical loads: ISO 16750-5 and ISO 20653

Automotive environmental conditions are generally more severe than those found in many commercial and industrial environments. The target automotive, industrial, or commercial environment(s) require careful analysis prior to implementation.

97.9.2.2 Electromagnetic compatibility

A system integrating the 1000BASE-T1 PHY shall comply with all applicable local and national codes. In addition, the system may need to comply with more stringent requirements as agreed upon between customer and supplier, for the limitation of electromagnetic interference. A 1000BASE-T1 PHY shall be tested according to CISPR 25 test methods defined to measure the PHY's EMC performance in terms of radio frequency (RF) immunity and RF emissions. When used in an automotive environment, a 1000BASE-T1 PHY is expected to meet the following motor vehicle EMC requirements:

a) Radiated/conducted emissions: CISPR 25, IEC 61967–1/4, and IEC 61000-4-21
b) Radiated/conducted immunity: ISO 11452, IEC 62132–1/4, and IEC 61000-4-21
c) Electrostatic discharge: ISO 10605 and IEC 61000-4-2/3
d) Electrical disturbances: IEC 62215-3 and ISO 7637-2/3

Exact test setup and test limit values may be adapted to each specific application, subject to agreement between the customer and the supplier.

97.10 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that

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network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of a 1000BASE-T1 PHY shall not exceed 7168 bit times (14 pause_quanta or 7168 ns). Transmit data delay is measured from the input of a given unit of data at the GMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the GMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link.

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97.11 Protocol implementation conformance statement (PICS) proforma for Clause 97, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 1000BASE-T1[170]

97.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 97, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 1000BASE-T1, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

97.11.2 Identification

97.11.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

97.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 97, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 1000BASE-T1
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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97.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
GMII	PHY associated with GMII	97.1	Interface is supported	O	Yes [ ] No [ ]
*EEE	EEE capability	97.1.2.3		O	Yes [ ] No [ ]
PCS	1000BASE-T1 PCS	97.3		M	Yes [ ]
PMA	1000BASE-T1 PMA	97.4		M	Yes [ ]
AN	Auto-negotiation	97.1, 98		O	Yes [ ] No [ ]
*CHNL	Channel	97.6	Channel specification not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
*MDIO	MDIO Capability	45.1	Register and Interface supported	O	Yes [ ] No [ ]
*AUTO	Automotive environment installation	97.9		O	Yes [ ] No [ ]
*LSTB	Operation on link segment type B	97.5.4.1	Optional	O	Yes [ ] No [ ]
*OAM	PCS-level Operations, Administration, and Maintenance channel capability	97.3.8		O	Yes [ ] No [ ]

97.11.4 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	MASTER-SLAVE relationship when Auto-Negotiation is not used	97.1.2	Established by management of hardware configuration of the PHYs	M	Yes [ ]
G2	Test circuit accuracy	97.1.5	Within ±1% unless otherwise stated	M	Yes [ ]
G3	Sum of the transmit and receive data delays	97.10	Not exceed 7168 bit times (14 pause_quanta or 7168 ns)	M	Yes [ ]
G4	Auto-negotiation	97.8.1	If supported per Clause 98	O	Yes [ ] No [ ]

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97.11.5 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Value/Comment	Status	Support
PCT1	PCS Transmit state diagram	97.3.2.2	Conform to Figure 97–14	M	Yes [ ]
PCT2	PCS Transmit bit ordering	97.3.2.2	Conform to Figure 97–5 and Figure 97–7	M	Yes [ ]
PCT3	PCS data transmission	97.3.2.2	45 80B/81B blocks are aggregated, encoded by a PHY frame encode, and then scrambled by a PCS scrambler	M	Yes [ ]
PCT4	PCS data encoding	97.3.2.2	Frames are encoded into a sequence of PAM3 symbols and transferred to the PMA	M	Yes [ ]
PCT5	Transmitted Control codes	97.3.2.2.6	Values not in Table 97–1 are not to be transmitted	M	Yes [ ]
PCT5a	Received Control codes	97.3.2.2.6	Values not in Table 97–1 are treated as an error if received	M	Yes [ ]
PCT6	Idle characters	97.3.2.2.7	Not be added within a data frame	M	Yes [ ]
PCT7	LP_IDLE characters	97.3.2.2.8	Not be added within a data frame	M	Yes [ ]
PCT8	EEE IDLE conversion	97.3.2.2.8	Convert LP_IDLE to IDLE if EEE is not supported	EEE:M	Yes [ ] N/A [ ]
PCT9	FEC	97.3.2.2.11	Reed-Solomon code (450,406)	M	Yes [ ]
PCT10	RS-FEC encoder	97.3.2.2.11	Follow the bit order described in 97.3.2.2.3	M	Yes [ ]
PCT11	Parity calculation	97.3.2.2.11	Produce the same result as the shift register implementation shown in Figure 97–8	M	Yes [ ]
PCT12	RS-FEC encoder shift register initialization	97.3.2.2.11	Set to zero before the parity calculation begins	M	Yes [ ]
PCT13	PCS MASTER scrambler	97.3.2.2.12	Conform to Figure 97–9	M	Yes [ ]
PCT14	PCS SLAVE scrambler	97.3.2.2.12	Conform to Figure 97–9	M	Yes [ ]
PCT15	PCS scrambler seed values	97.3.2.2.12	Non-zero and transmitted during the InfoField exchange	M	Yes [ ]
PCT16	EEE compliant PHYs	97.3.2.2.15	Implement Figure 97–14	EEE:M	Yes [ ] N/A [ ]
PCT17	EEE RS partial IDLE	97.3.2.2.15	Transmit no PHY frames partially filled with LP_IDLES	EEE:M	Yes [ ] N/A [ ]
PCT18	EEE without SEND_N	97.3.2.2.15	lpi_tx_mode variable is ignored when the PMA_TXMODE.indication message does not have the values SEND_N	EEE:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PCT19	EEE NORMAL	97.3.2.2.15	The PCS passes coded data to the PMA via the PMA_UNITDATA.request primitive when the lpi_tx_mode variable takes the value NORMAL and when the PMA asserts SEND_N	EEE:M	Yes [ ] N/A [ ]
PCT20	EEE QUIET	97.3.2.2.15	The PCS passes zeros to the PMA via the PMA_UNITDATA.request primitive when the lpi_tx_mode variable takes the value QUIET and when the PMA asserts SEND_N	EEE:M	Yes [ ] N/A [ ]
PCT21	EEE REFRESH	97.3.2.2.15	The PCS passes zero data encoded through PCS data path to the PMA via the PMA_UNITDATA.request primitive when the lpi_tx_mode variable takes the value REFRESH and when the PMA asserts SEND_N	EEE:M	Yes [ ] N/A [ ]
PCT22	Wake frame	97.3.2.2.15	Be sent only during alternating PHY frame counts	EEE:M	Yes [ ] N/A [ ]
PCT23	PCS reset execution	97.3.2.1	Described in 97.3.2.1	M	Yes [ ]

97.11.6 PCS Receive functions

Item	Feature	Subclause	Value/Comment	Status	Support
PCR1	PCS receive state diagram	97.3.2.3	Conform to Figure 97–12	M	Yes [ ]
PCR2	PCS Receive bit ordering	97.3.2.3	Conform to Figure 97–6	M	Yes [ ]
PCR3	PAM3 stream	97.3.2.3.1	Form stream from PMA_UNITDATA.indication primitive by concatenating requests in order from rx_data<0> to rx_data<2699>	M	Yes [ ]
PCR4	PCS descrambler	97.3.2.3	Descramble the data stream for generation of RXD<7:0> to the GMII	M	Yes [ ]
PCR5	MASTER side-stream descrambler	97.3.2.3.2	Equation (97–4)	M	Yes [ ]
PCR6	SLAVE side-stream descrambler	97.3.2.3.2	Equation (97–3)	M	Yes [ ]
PCR7	Transmit PCS test pattern mode	97.3.3	Transmit continuously as illustrated in Figure 97–5	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PCR8	Receive PCS test pattern mode	97.3.3	Receive continuously as illustrated in Figure 97–6	M	Yes [ ]
PCR9	MASTER side-stream scrambler	97.3.4	Equation (97–5)	M	Yes [ ]
PCR10	SLAVE side-stream scrambler	97.3.4	Equation (97–6)	M	Yes [ ]
PCR11	Initialized scrambler state	97.3.4	Never all zeros	M	Yes [ ]
PCR12	Scramble status	97.3.4.3	Acquire and report descrambler state synchronization via scr_status	M	Yes [ ]
PCR13	DECODE function	97.3.6.2.3	Decode the block as specified in 97.3.2.2.2	M	Yes [ ]
PCR14	ENCODE function	97.3.6.2.3	Encode the block as specified in 97.3.2.2.2	M	Yes [ ]
PCR15	Encode function encode LPI_IDLE	97.3.6.2.3	Only in SEND_LPI state	EEE:M	Yes [ ] N/A [ ]
PCR16	PCS Receive, RFER monitor, and PCS Transmit state diagrams	97.3.6.4	Figure 97–12, Figure 97–13, and Figure 97–14	M	Yes [ ]

97.11.7 PCS loopback

Item	Feature	Subclause	Value/Comment	Status	Support
PCO1	PCS loopback mode	97.3.7.3	Enabled when MDIO register 3.2304.14 is set to a one	MDIO:M	Yes [ ]
PCO2	PCS loopback enabled	97.3.7.3	PCS accepts data on the transmit path from the GMII and return it on the receive path to the GMII when in loopback mode when in loopback mode	M	Yes [ ]
PCO3	PCS loopback enabled	97.3.7.3	Transmit a continuous stream of GMII data to the 81B encoder and then to PMA sublayer and ignore all data presented to it by the PMA sublayer	M	Yes [ ]

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97.11.8 OAM

Item	Feature	Subclause	Value/Comment	Status	Support
OAM1	State diagram behavior	97.3.8	Conforms to Figure 97–18 and Figure 97–19	OAM:M	Yes [ ] N/A [ ]
OAM2	OAM fields set to zero if OAM is not supported	97.3.8.2.1		!OAM:M	Yes [ ] N/A [ ]
OAM3	Reserved fields are zero	97.3.8.2.2		OAM:M	Yes [ ] N/A [ ]
OAM4	CRC16	97.3.8.2.12	Produces equivalent result to implementation shown in Figure 97–16	OAM:M	Yes [ ] N/A [ ]
OAM5	CRC initialization	97.3.8.2.12	Delay elements initialized to zero	OAM:M	Yes [ ] N/A [ ]
OAM6	OAM fields accepted and updated	97.3.8.2.13	Except if a) Incorrect parity on any of the 12 symbols, or, b) Incorrect CRC16, or c) Uncorrectable PHY frame on any of the 12 symbols	OAM:M	Yes [ ] N/A [ ]
OAM7	PHY Health indicator	97.3.8.2.14	Prevent entering quiet/refresh, or exit quiet/refresh if PHY Health indicator of 01 is received	EEE* OAM:M	Yes [ ] N/A [ ]
OAM8	mr_tx_received	97.3.8.4.3	mr_tx_received clears on read	OAM:M	Yes [ ] N/A [ ]

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97.11.9 Physical Medium Attachment (PMA)

Item	Feature	Subclause	Value/Comment	Status	Support
PMF1	PMA Reset function	97.4.2.1	Described in 97.4.2.1	M	Yes [ ]
PMF2	PMA Transmit function	97.4.2.2	Continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb after processing with optional transmit filtering.	M	Yes [ ]
PMF3	Signals generated by PMA transmit	97.4.2.2	Comply with 97.5	M	Yes [ ]
PMF4	MASTER TX_TCLK source	97.4.2.2	Local clock source while meeting the transmit jitter requirements of 97.5.3.3	M	Yes [ ]
PMF5	The MASTER-SLAVE relationship	97.4.2.2	Include loop timing	M	Yes [ ]
PMF6	SLAVE TX_TCLK source	97.4.2.2	Recovered clock of 97.4.2.8 while meeting the jitter requirements of 97.5.3.3.	M	Yes [ ]
PMF7	PMA_transmit_disable variable	97.4.2.2.1	When set to true, turn off the transmitter so that the transmitter Average Launch Power of the Transmitter is less than –53 dBm	M	Yes [ ]
PMF8	Quality of rx_symb symbols	97.4.2.3	Allow RFER of less than 3.6×10^{-7} after RS-FEC decoding, over a channel meeting the requirements of 97.6	M	Yes [ ]
PMF9	PMA receive fault function	97.4.2.3	Contribute to the receive fault bit specified in 45.2.1.238.6	MDIO:O	Yes [ ] N/A [ ]
PMF10	PHY Control	97.4.2.4	Comply with Figure 97–26	M	Yes [ ]
PMF11	12-octet InfoField	97.4.2.4	Include the fields in 97.4.2.4.2 through 97.4.2.4.8	M	Yes [ ]
PMF12	Each unique InfoField	97.4.2.4	Transmitted at least 256 times	M	Yes [ ]
PMF13	InfoField Reserved bits	97.4.2.4.1	Set to zero on transmit and ignored when received by the link partner	M	Yes [ ]
PMF14	Start of Frame Delimiter	97.4.2.4.2	Hexadecimal value 0xBBA700	M	Yes [ ]
PMF15	PMA_state<7:6>	97.4.2.4.4	Communicate the state of the transmitting transceiver to the link partner	M	Yes [ ]
PMF16	Any Message Field value not listed in Table 97–7 or Table 97–8	97.4.2.4.4	Not be transmitted and ignored at the receiver	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PMF17	The Message Field setting for the first transmitted PMA frame	97.4.2.4.4	First row of Table 97–7 for the MASTER and the first or second row of Table 97–8 for the SLAVE	M	Yes [ ]
PMF18	Indicate support of optional capabilities	97.4.2.4.5	Set the corresponding capability bits	M	Yes [ ]
PMF19	State of the scrambler	97.4.2.4.5	S14:S0 at the first bit of the first PHY frame when the partial PHY frame counter equals to the DataSwPFC24 value	M	Yes [ ]
PMF20	Seed S<14:0>	97.4.2.4.5	Not all zeros	M	Yes [ ]
PMF21	DataSwPFC24	97.4.2.4.6	Set to an integer multiple of 15	M	Yes [ ]
PMF22	CRC16 (2 octets)	97.4.2.4.8	Implement the CRC16 polynomial $(x+1)(x^{15}+x+1)$ of the previous 7 octets	M	Yes [ ]
PMF23	CRC16	97.4.2.4.8	Figure 97–23	M	Yes [ ]
PMF24	CRC16 delay elements	97.4.2.4.8	Initialized to zero	M	Yes [ ]
PMF25	Startup sequence	97.4.2.4.10	Comply with Figure 97–26	M	Yes [ ]
PMF26	Enable EEE capability	97.4.2.4.10	Enabled if both PHYs set EEEen = 1	EEE:M	Yes [ ] N/A [ ]
PMF27	Set en_slave_tx = 1	97.4.2.4.10	After the MASTER has sufficiently converged the necessary circuitry, allowing the SLAVE to transition to TRAINING	M	Yes [ ]
PMF28	Enable 1000BASE-T1 OAM capability	97.4.2.4.10	Enabled only if both PHYs set OAMen = 1	M	Yes [ ]
PMF29	SLAVE PHY TRAINING	97.4.2.4.10	Align transmit 81B-RS frame within +0/–1 partial PHY frames of the MASTER	M	Yes [ ]
PMF30	SLAVE InfoField partial PHY frame Count	97.4.2.4.10	Match MASTER InfoField partial PHY frame Count for the aligned frame	M	Yes [ ]
PMF31	Link Monitor function	97.4.2.5	Comply with Figure 97–27	M	Yes [ ]
PMF32	Refresh monitor function	97.4.3		EEE:M	Yes [ ] N/A [ ]
PMF33	Set PMA_refresh_status to FAIL	97.4.3	When Refresh is not detected within a moving window of 50 Q/R cycles	EEE:M	Yes [ ] N/A [ ]
PMF34	Set PMA_refresh_status to OK	97.4.3	When Link Monitor state diagram enters LINK_UP state	EEE:M	Yes [ ] N/A [ ]
PMF35	Clock Recovery function	97.4.2.8	Provide a clock suitable for signal sampling so that RS FER is achieved	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PMF36	maxwait_timer	97.4.4.2	Expire 97.5 ms ± 0.5 ms after being started	M	Yes [ ]
PMF37	minwait_timer	97.4.4.2	Expire 975 µs ± 50 µs after being started	M	Yes [ ]
PMF38	sigdet_wait_timer	97.4.2.6.2	Expires 4 µs ± 0.1 µs after being started	M	Yes [ ]
PMF39	send_s_timer	97.4.2.6.2	Expires 1.0 µs ± 0.04 µs after being started	M	Yes [ ]
PMF40	send_s_sigdet	97.4.2.6.1	Set to false no later than 1 µs after the signal goes quiet on the MDI	M	Yes [ ]
PMF41	Auto-Negotiation function used for PHY synchronization	97.4.2.6		M	Yes [ ]
PMF42	Function of Figure 97–25	97.4.2.6	Used to synchronize 1000BASE-T1 PHYs prior to the 1000BASE-T1 link training	M	Yes [ ]
PMF43	PN sequence generator shift registers reset	97.4.2.6	The PN sequence generator shift registers are reset to a non-zero value upon entering into the TRANSMIT_DISABLE state (see Figure 97–25)	M	Yes [ ]
PMF44a	SLAVE PN sequence generator	97.4.2.6	See Equation (97–9)	M	Yes [ ]
PMF44b	MASTER PN sequence generator	97.4.2.6	See Equation (97–8)	M	Yes [ ]
PMF45	The next Message Field setting	97.4.2.4.4	Equal to the same Message Field setting or the Message Field setting corresponding to a row below the current setting	M	Yes [ ]

97.11.10 PMA electrical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PME1	DPI and 150 Ω emission tests	97.5.1	Used to establish a baseline for PHY EMC performance	M	Yes [ ]
PME2	DPI method of IEC 62132-4	97.5.1.1	Used to test the sensitivity of the PMA receiver to radio frequency noise	M	Yes [ ]
PME3	150 Ω direct coupling method of IEC 61967-4	97.5.1.2	Used to test the conducted CM emission of the PMA transmitter to its electrical environment	M	Yes [ ]
PME4	Test modes	97.5.2	Provided to allow for testing the transmitter	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PME5	Test modes	97.5.2	Enabled by setting control register 1.2308.15:13	MDIO: M	Yes [ ] N/A [ ]
PME6	Test mode change data only	97.5.2	The test modes only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation	M	Yes [ ]
PME7	Test mode 1	97.5.2	Provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK125 when in test mode 1	M	Yes [ ]
PME8	Test mode 2	97.5.2	Transmit three {+1} symbols followed by three {–1} symbols continually	M	Yes [ ]
PME9	Test mode 3	97.5.2	Transmit three {+1} symbols followed by three {–1} symbols continually	M	Yes [ ]
PME10	Test mode 4	97.5.2	Transmit the sequence of symbols generated by the scrambler generator polynomial per Equation (97–12) when in test mode 4	M	Yes [ ]
PME10a	Test Mode 4 transmit clock	97.5.2	750 MHz ± 0.01% clock when in MASTER timing mode	M	Yes [ ]
PME10b	Test mode 4 signal level	97.5.2	Same as non-test mode	M	Yes [ ]
PME10c	Test mode 4 Sequence generator clock	97.5.2	2/750 MHz	M	Yes [ ]
PME10d	Test mode 4 ternary symbols $T0_n$ and $T1_n$	97.5.2	Generated from bits $x0_n$, $x1_n$, and $x2_n$ of the test mode 4 sequence generator	M	Yes [ ]
PME11	Test mode 5	97.5.2	Transmit as in non-test operation and in the MASTER data mode with data set to normal Inter-Frame idle signals	M	Yes [ ]
PME12	Test mode 6	97.5.2	Transmit fifteen {+1} symbols followed by fifteen {–1} symbols continually	M	Yes [ ]
PME12a	Test fixtures	97.5.2.1	Per Figure 97–29, Figure 97–30, Figure 97–31, Figure 97–32, and Figure 97–33 or equivalent	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PME12b	Disturbing signal characteristics	97.5.2.1	Sinusoidal, amplitude of 3.6 V peak-to-peak differential, and frequency of one-sixth the symbol rate (125 MHz) synchronous with the test pattern	M	Yes [ ]
PME13	Tolerance of resistors used in test fixtures	97.5.2.1	± 0.1%	M	Yes [ ]
PME14	Disturbing signal generator	97.5.2.1	Have sufficient linearity and range so it does not introduce any appreciable distortion	M	Yes [ ]
PME15	Coupling	97.5.3	Operate with AC coupling to the MDI	M	Yes [ ]
PME16	Resistive differential load	97.5.3	Meet electrical requirements of this clause with a 100 Ω resistive differential load connected to transmitter output if load is not specified	M	Yes [ ]
PME17	Magnitude of both the positive and negative droop	97.5.3.1	Less than 10% measured with respect to an initial value at 4 ns after the zero crossing and a final value at 16 ns after the zero crossing	M	Yes [ ]
ME17a	Transmitter distortion signal capture	97.5.3.2	At least 40 µs long and sampled at a rate of at least 7.5 Gs/s (10 times the transmit symbol rate of 750 Ms/s)	M	Yes [ ]
PME18	Transmitter distortion	97.5.3.2	Less than 15 mV for at least 10 measured equally spaced phases	M	Yes [ ]
PME19	Transmitter distortion test mode 4 capture	97.5.3.2	Minimum of 40 µs long and minimum sampling rate of 7.5 Gs/s	M	Yes [ ]
PME20	MASTER TX_TCLK125 jitter RMS	97.5.3.3	Less than 5 ps RMS	M	Yes [ ]
PME21	MASTER TX_TCLK125 jitter Peak-to-Peak	97.5.3.3	Less than 50 ps peak-to-peak	M	Yes [ ]
PME22	SLAVE TX_TCLK125 jitter RMS	97.5.3.3	Less than 10 ps RMS	M	Yes [ ]
PME23	SLAVE TX_TCLK125 jitter Peak-to-Peak	97.5.3.3	Less than 100 ps peak-to-peak	M	Yes [ ]
PME23b	TX_TCLK125 jitter measurement bandwidth	97.5.3.3	Larger than 2 MHz	M	Yes [ ]
PME24	Reference clock	97.5.3.3	Reference clock is continuous when transitioning into or out of LPI mode	EEE:M	Yes [ ] N/A [ ]
PME25	MDI output jitter RMS	97.5.3.3	Less than 5 ps RMS	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PME25a	MDI output jitter Peak to Peak	97.5.3.3	Less than 50 ps RMS	M	Yes [ ]
PME25b	MDI jitter measurement bandwidth	97.5.3.3	Larger than 2 MHz	M	Yes [ ]
PME26	Transmit power in test mode 5	97.5.3.4	Less than 5 dBm	M	Yes [ ]
PME27	Power spectral density in test mode 5	97.5.3.4	Between the upper and lower masks specified in Equation (97–14) and Equation (97–15), when measured into a 100 Ω load using the test fixture 5 shown in Figure 97–33	M	Yes [ ]
PME28	TX_TCLK125 jitter measurement	97.5.3.3	Measured over an interval of 1 ms ± 10%	M	Yes [ ]

97.11.11 MDI electrical requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PMI1	Transmit differential signal	97.5.3.5	Less than 1.30 V peak-to-peak for all transmit modes when measured with 100 Ω reference termination	M	Yes [ ]
PMI2	MASTER PHY symbol transmission rate	97.5.3.6	Within the range 750 MHz ± 100 ppm	M	Yes [ ]
PMI3	LPI mode the short-term rate of frequency variation	97.5.3.6	Less than 0.1 ppm/second	EEE:M	Yes [ ] N/A [ ]
PMI4	Receiver differential input signals	97.5.4.1	Frame loss ratio less than 10^{-7} for 125-octet frames	M	Yes [ ]
PMI5	Frame loss ratio for operation on link segment type B	97.5.4.1	Met for link segments specified at 97.6.2 and 97.6.4	LSTB:M	Yes [ ] N/A [ ]

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97.11.11.1 Characteristics of the link segment

Item	Feature	Subclause	Value/Comment	Status	Support
LKS2	Insertion loss of each type A link segment	97.6.1.1	Equation (97–16)	CHNL:M	Yes [ ] N/A [ ]
LKS3	Return loss (with 100 Ω reference impedance) of each type A link segment	97.6.1.3	Equation (97–17)	CHNL:M	Yes [ ] N/A [ ]
LKS4	Differential-to-common-mode conversion of each type A link segment	97.6.1.4	Equation (97–18) for all frequencies from 10 MHz to 600 MHz	CHNL:M	Yes [ ] N/A [ ]
LKS5	Maximum link delay for type A link segment	97.6.1.5	Not exceed 94 ns at all frequencies between 2 MHz and 600 MHz	CHNL:M	Yes [ ] N/A [ ]
LKS6	Insertion loss of each type B link segment	97.6.2.1	Equation (97–19)	CHNL:M	Yes [ ] N/A [ ]
LKS7	Return loss (with 100 Ω reference impedance) of each type B link segment	97.6.2.3	Equation (97–20)	CHNL:M	Yes [ ] N/A [ ]
LKS8	Maximum link delay for type B link segment	97.6.2.4	Not exceed 234 ns at all frequencies between 2 MHz and 600 MHz	CHNL:M	Yes [ ] N/A [ ]
LKS9	Coupling attenuation of the type B link segment	97.6.2.5	Table 97–14	CHNL:M	Yes [ ] N/A [ ]
LKS10	Power sum ANEXT loss between a disturbed type A link segment and the disturbing type A link segment	97.6.3.2	Equation (97–22)	CHNL:M	Yes [ ] N/A [ ]
LKS11	Power sum AACRF between a disturbed type A link segment and the disturbing type A link segment	97.6.3.4	Equation (97–24)	CHNL:M	Yes [ ] N/A [ ]
LKS12	Power sum ANEXT loss between a disturbed type B link segment and the disturbing type B link segment	97.6.4.2	Equation (97–26)	CHNL:M	Yes [ ] N/A [ ]
LKS13	Power sum AACRF between a disturbed type B link segment and the disturbing type B link segment	97.6.4.4	The lesser of Equation (97–28) and 70 dB	CHNL:M	Yes [ ] N/A [ ]

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97.11.12 MDI Requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MDI1	Symbol response	97.4.3.1	Comply with 97.5	M	Yes [ ]
MDI2	MDI electrical specification	97.7.2	Meet the electrical requirements specified in 97.5.3 and 97.5.4 when the PHY is connected to the MDI connector mated with a specified balanced twisted-pair cable connector	M	Yes [ ]
MDI3	Return loss	97.7.2.1	Equation (97–29)	M	Yes [ ]
MDI4	MDI wire pair short circuit	96.8.3	Under all operating conditions withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 96–6, for an indefinite period of time	M	Yes [ ]
MDI5	Operation after short circuit	96.8.3	Resume normal operation	M	Yes [ ]
MDI6	MDI wire pair transients and ESD	96.8.3	Under all operating conditions, withstand without damage high voltage transient noise and ESD per application requirements	M	Yes [ ]
MD17	MDI mode conversion loss	97.7.2.2	Equation (97–30)	M	Yes [ ]

97.11.13 EEE capability requirements

Item	Feature	Subclause	Value/Comment	Status	Support
EEE1	Transition to and from LPI mode	97.1.2.3	Cause no data frames be lost or corrupted.	EEE:M	Yes [ ] N/A [ ]
EEE2	Normal power resumption	97.1.2.3	Resume normal power mode on the PHY frame following a PCS transmission of a wake frame	EEE:M	Yes [ ] N/A [ ]
EEE3	LPI synchronization	97.3.5.1	Synchronize refresh intervals during LPI mode	EEE:M	Yes [ ] N/A [ ]
EEE4	Partial PHY frame count synchronization	97.3.5.1	When SLAVE, synchronize partial PHY frame count to MASTER’s partial PHY frame count within 1 partial PHY frame	EEE:M	Yes [ ] N/A [ ]
EEE5	tx_refresh_active and tx_wake_start signals	97.3.5.1	Derive tx_refresh_active and tx_wake_start signals from the transmitted PHY frames	EEE:M	Yes [ ] N/A [ ]
EEE6	Quiet period	97.3.5.2	Transmit PAM3 symbol zero on to the MDI	EEE:M	Yes [ ] N/A [ ]

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97.11.14 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Environmental safety	97.9.2.1	Conform to the potential environmental stresses with respect to their mounting location, as defined in: ISO 16750-1, ISO 16750-2, ISO 17637-2:2008, ISO 8820-1, ISO 16750-3, ASTM D4728, ISO 12103-1, ISO 16750-4, IEC 60068-2-1, IEC 60068-2-27, IEC 60068-2-30, IEC 60068-2-38, IEC 60068-2-52, IEC60068-2-64, IEC 60068-2-78, ISO 16750-5, and ISO 20653	AUTO: M	Yes [ ] N/A[ ]
ES2	Electromagnetic compatibility: local and national codes	97.9.2.2	Compliance with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]
ES3	Electromagnetic compatibility: EMC test methods	97.9.2.2	Tested according to CISPR 25 test methods defined to measure the PHY's EMC performance	M	Yes [ ]
ES4	Electromagnetic compatibility: motor vehicle EMC requirements	97.9.2.2	Meet the following motor vehicle EMC requirements: CISPR 25, IEC 61967–1/4, IEC 61000-4-21, ISO 11452, IEC 62132–1/4, IEC 61000-4-21, ISO 10605, IEC 61000-4-2/3, IEC 62215-3, ISO 7637-2/3	AUTO: M	Yes [ ] N/A[ ]

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98. Auto-Negotiation for single differential-pair media

98.1 Overview

98.1.1 Scope

Clause 98 describes the single twisted-pair Auto-Negotiation function that allows a device to advertise enhanced modes of operation it possesses to a device at the remote end of a link segment and to detect corresponding enhanced operational modes that the other device may be advertising. Annex 98A describes the Selector Field that is used by Auto-Negotiation to identify the type of message being sent.

The objective of the single twisted-pair Auto-Negotiation function is to provide the means to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. It has the additional objective of providing a common synchronization time between two devices prior to link training.

Single twisted-pair Auto-Negotiation is performed using differential Manchester encoding (DME) pages. DME provides a DC balanced signal. DME does not add packet or upper layer overhead to the network devices. DME is transferred in a half-duplex manner over the single twisted-pair copper cable.

Single twisted-pair Auto-Negotiation does not test the link segment characteristics.

The function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and understanding of the common mode(s) of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The single twisted-pair Auto-Negotiation function allows the identification of the operational mode of the link partner. Should multiple modes be present, management may select between the various offered modes. How such selection is done is beyond the scope of this standard.

98.1.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

The single twisted-pair Auto-Negotiation function is provided at the Physical Layer of the ISO/IEC OSI reference model as shown in Figure 98–2. A device that supports multiple modes of operation may advertise its capabilities using the single twisted-pair Auto-Negotiation function. The actual transfer of information is observed only at the MDI.

98.2 Functional specifications

The single twisted-pair Auto-Negotiation function provides a mechanism to control connection of a single MDI to a single PHY type, where more than one PHY type may exist. A management interface provides control and status of single twisted-pair Auto-Negotiation, but the presence of a management agent is not required.

Auto-Negotiation shall provide the following functions (as shown in Figure 98–1):

a) Transmit
b) Receive
c) Half duplex
d) Arbitration

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These functions shall comply with the state diagrams from Figure 98–7 through Figure 98–10. The single twisted-pair Auto-Negotiation functions shall interact with the technology-dependent PHYs through the Technology Dependent Interface (see 98.4).

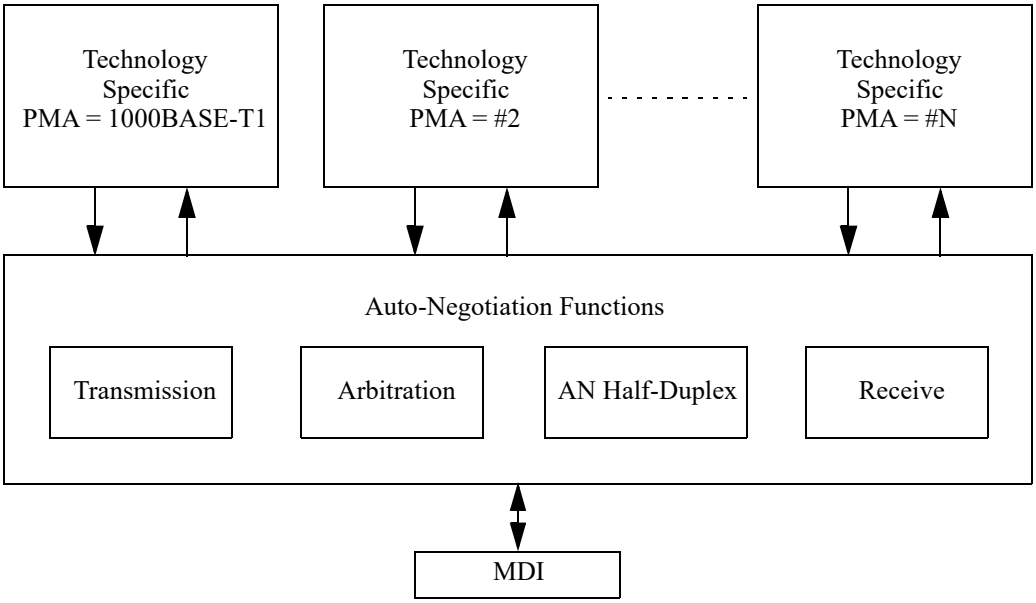

Figure 98–1—High-level model

98.2.1 Transmit function requirements

The Transmit function provides the ability to transmit pages. The first pages exchanged by the local device and its link partner after Power-On, link restart, or renegotiation contain the base link codeword defined in Table 98–2. The local device may modify the link codeword to disable an ability it possesses, but will not transmit an ability it does not possess. This makes possible the distinction between local abilities and advertised abilities so that multi-ability devices may Auto-Negotiate to a mode lower in priority than the highest common ability.

Two different Auto-Negotiation speeds are defined in this subclause. A PHY shall support at least one of these Auto-Negotiation speeds. The two speeds are referred to as *high-speed mode*, or HSM, and *low-speed mode*, or LSM. If Auto-Negotiation is implemented, 1000BASE-T1, 100BASE-T1, and 10BASE-T1S PHYs shall support HSM and may optionally support LSM. For link segments with high insertion loss and those requiring 10BASE-T1L, LSM is provided to enable the full reach capability. If Auto-Negotiation is implemented, 10BASE-T1L PHYs shall support LSM and may optionally support HSM. When performing Auto-Negotiation in high-speed mode, DME pages are transmitted at a nominal rate of 16.667 Mb/s. In low-speed mode, DME pages are transmitted at a nominal rate of 625 kb/s. Subclause 98.5.6 describes the behavior to automatically choose between the different Auto-Negotiation speeds when a PHY supports both.

98.2.1.1 DME transmission

Auto-Negotiation's method of communication builds upon the encoding mechanism known as differential Manchester encoding (DME). The DME page encodes the data that is used to control the Auto-Negotiation function. DME pages shall not be transmitted when Auto-Negotiation is complete and the highest common denominator PHY has been enabled.

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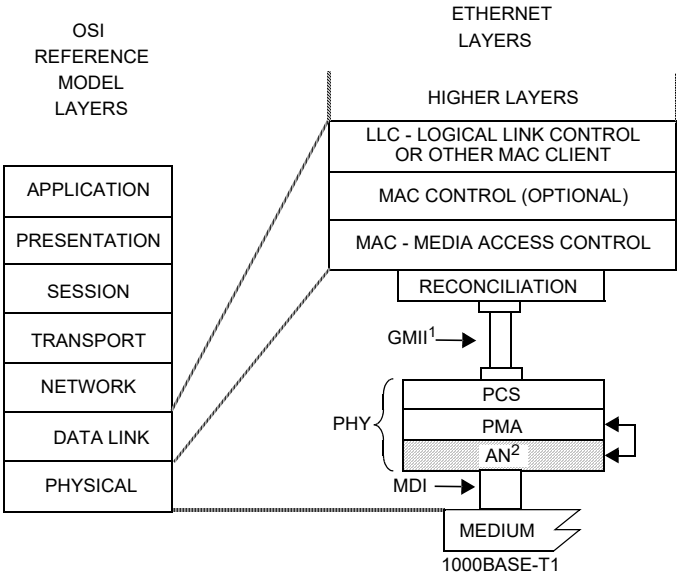
98.2.1.1.1 DME page encoding

A DME page carries a 48-bit Auto-Negotiation page. It consists of 157 evenly spaced transition positions starting from the initial transition from silent to active in the preamble. The page contains a Start Delimiter, the 48-bit page, 16-bit CRC, and an end delimiter (see Figure 98–6). The odd-numbered transition positions represent clock information. The even numbered transition positions represent data information. DME pages are alternately transmitted between the two devices with quiet period separating the DME pages. When the DME page is active, the PHY shall transmit either +1 or –1 level with the voltage levels as specified in 98.2.1.1.4.



MDI = MEDIUM DEPENDENT INTERFACE
GMII = TEN GIGABIT MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

NOTE 1—GMII is optional.
NOTE 2—Auto-Negotiation is optional. Auto-Negotiation communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indication.

Figure 98–2—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

The first 26 transition positions contain the Start Delimiter, which marks the beginning of the page. The Start Delimiter contains a transition from quiet to active at position 1. For HSM Auto-Negotiation, this transition is followed by transitions at positions 2, 3, 5, 7, 8, 12, 13, 14, 15, 19, 21, 24, 25, 26 and no transitions at the remaining positions. For LSM Auto-Negotiation, this transition is followed by transitions at positions 2, 3, 4, 5, 6, 7, 8, 9, 11, 13, 15, 16, 18, 19, 20, 22, 23, 24, 26 and no transitions at the remaining positions.

The final 2 transition positions contain the ending delimiter, which marks the end of the page. The ending delimiter contains a transition at position 155 and no transitions at the remaining positions. Position 157 contains a transition from active to quiet.

Each of the remaining 64 odd-numbered transition positions between the starting and ending delimiters shall contain a transition. The remaining 64 even-numbered transition positions shall represent data information as follows:

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— A transition present in an even-numbered transition position represents a logical one.
— A transition absent from an even-numbered transition position represents a logical zero.

The first 48 of these positions shall carry the data of the Auto-Negotiation page. The final 16 positions carry the 16-bit CRC.

The CRC16 polynomial is $x^{16} + x^{15} + x^2 + 1$. The CRC16 shall produce the same result as the implementation shown in Figure 98–3. The 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards the 48 data bits are used to compute the CRC16 with the switch connected (setting CRCgen). After all the 48 bits have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

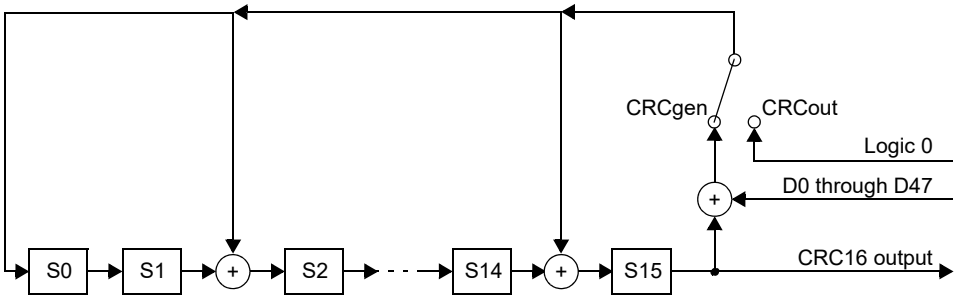

Figure 98–3—CRC16

The polarity at position 0 is randomly determined in an implementation specific manner.

The purpose of randomizing the starting polarity is to remove the spectral peaks that would otherwise occur when sending the same DME page repeatedly. Randomly choosing the starting polarity results in randomly inverting or not inverting the encoded page so that repetitions of the same page no longer produce a periodic signal.

Clock transition positions are differentiated from data transition positions by the spacing between them, as shown in Figure 98–4 and enumerated in Table 98–1.

The encoding of data using DME bits in a DME page is illustrated in Figure 98–4.

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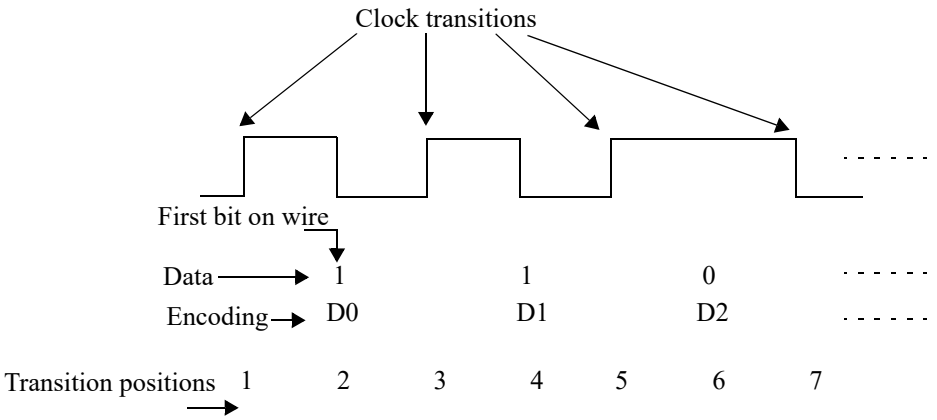

Figure 98–4—Data bit encoding within DME pages

98.2.1.1.2 DME page timing

The timing parameters for DME pages shall be followed as in Table 98–1. The transition positions within a DME page are spaced with a period of T1. T2 is the separation between clock transitions. T3 is the time from a clock transition to a data transition representing a one. When operating in high-speed mode, transitions shall occur within ± 0.8 ns of their ideal positions. When operating in low-speed mode, transitions shall occur within ± 10 ns of their ideal positions.

T5 specifies the duration of a DME page. The minimum number of transitions and maximum number of transitions in a page is represented by T4a. T4b indicates that the start of a DME page begins with a transition from 0 to ±1 and the end of the DME page is a transition from ±1 to 0.

Table 98–1 summarizes the timing parameters. The transition timing parameters are illustrated in Figure 98–5 and Figure 98–6.

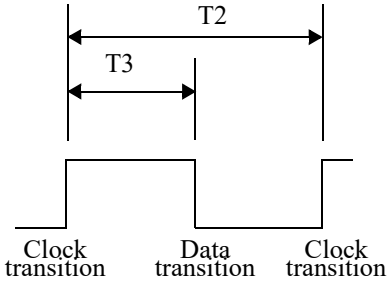

Figure 98–5—DME page transition timing

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Table 98–1—DME page timing summary

	Parameters	Mode	Min	Typ	Max	Units
T1	Transmit position spacing (period)	high-speed	29.997	30	30.003	ns
		low-speed	799.96	800	800.04	
T2	Clock transition to clock transition	high-speed	59.8	60	60.2	ns
		low-speed	1590	1600	1610	
T3	Clock transition to data transition (data = 1)	high-speed	29.9	30	30.1	ns
		low-speed	795	800	805	
T4a	+1 to –1 or –1 to +1 transitions in a DME page	high-speed	79	—	143	—
		low-speed	84	—	148	
T4b	0 to ±1 or ±1 to 0 transitions in a DME page	high-speed	2	2	2	—
		low-speed	2	2	2	
T5	DME page width	high-speed	4679	4680	4681	ns
		low-speed	124 793	124 800	124 807	

98.2.1.1.3 DME page Delimiters

The page is preceded by a unique Start Delimiter consisting of a 26 × T1 sequence that includes multiple DME transition violations. For a Start Delimiter starting with a 0 to +1 transition, the bit sequence for high-speed Auto-Negotiation mode is:

+1 –1 +1 +1 –1 –1 +1 –1 –1 –1 –1 +1 –1 +1 –1 –1 –1 –1 +1 +1 –1 –1 –1 +1 –1 +1.

For a Start Delimiter starting with a 0 to +1 transition, the bit sequence for low-speed Auto-Negotiation mode is:

+1 –1 +1 –1 +1 –1 +1 –1 +1 +1 –1 –1 +1 +1 –1 +1 +1 –1 +1 –1 –1 +1 –1 +1 +1 –1.

The DME page ends with an end delimiter that consists of an electrical 0. An example of the delimiters is shown in Figure 98–6.

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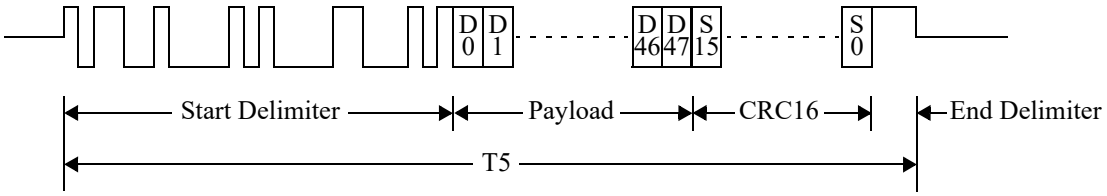

Figure 98–6—DME Page

NOTE—The Start Delimiter may begin with a 0 to +1 or 0 to –1 transition depending upon the DME page starting polarity randomizer.

98.2.1.1.4 Transmitter peak differential output

When measured with 100 Ω termination, transmit differential signal at MDI shall be within range of 1 V ± 30% peak-to-peak.

98.2.1.2 Link codeword encoding

The base link codeword (Base Page) transmitted within a DME page shall convey the encoding shown in Table 98–2. The Auto-Negotiation function supports additional pages using the Next Page function.

Encoding for the link codeword(s) used in the Next Page exchange are defined in 98.2.4.3. In a DME page, D0 shall be the first bit transmitted.

Table 98–2—Link codeword Base Page

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
S0	S1	S2	S3	S4	E0	E1	E2	E3	E4	C0	C1	M/S	RF	Ack	NP
D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
T0	T1	T2	T3	T4	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47
A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26

D[4:0] contains the Selector Field. D[9:5] contains the Echoed Nonce field. D[11:10] contains capability bits to advertise capabilities not related to the PHY. C[1:0] is used to advertise pause capability. D[12] is the force MASTER-SLAVE bit (see 98.2.1.2.5). D[15:13] contains the RF, Ack, and NP bits. The RF, Ack, and NP bits shall function as specified in 98.2.1.2.7, 98.2.1.2.8, and 98.2.1.2.9, respectively. D[20:16] contains the Transmitted Nonce field. D[47:21] contains the Technology Ability Field.

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

98.2.1.2.1 Selector Field

Selector Field (S[4:0]) is a 5-bit wide field, encoding 32 possible messages. Selector Field encoding definitions are shown in Annex 98A. Combinations not specified are reserved. Reserved combinations of the Selector Field shall not be transmitted.

The Selector Field for IEEE Std 802.3 is shown in Table 98–3.

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Table 98–3—Selector Field Encoding

S4	S3	S2	S1	S0	Selector description
0	0	0	0	1	IEEE Std 802.3

98.2.1.2.2 Echoed Nonce Field

Echoed Nonce Field (E[4:0]) is a 5-bit wide field containing the nonce received from the link partner. If the device has not received a DME page with good CRC16, the bits in this field shall contain logical zeros. If the device has received a DME page with good CRC16, the bits in this field shall contain the value received in the Transmitted Nonce Field from the link partner at the same time as the Acknowledge bit is set.

98.2.1.2.3 Transmitted Nonce Field

Transmitted Nonce Field (T[4:0]) is a 5-bit wide field whose lower 4 bits contains a random or pseudo-random number. A new value shall be generated for each entry to the Ability Detect state. The method of generating the nonce is left to the implementer. The lower 4 bits of the transmitted nonce should have a uniform distribution in the range from 0 to $2^4 – 1$. The method used to generate the value should be designed to minimize correlation to the values generated by other devices.

Bit T[4] should be set to 1 if the device prefers or is forced to be MASTER and 0 if the device prefers or is forced to be SLAVE.

If the device has received a DME page with good CRC16 and the link partner has a Transmitted Nonce Field (T[4:0]) that matches the devices generated T[4:0], the device shall invert its T[0] bit and regenerate a new random value for T[3:1] and use that as its new T[4:0] value. Since the DME pages are exchanged in a half-duplex manner, it is possible to swap to a new T[4:0] value prior to transmitting the DME page. One device will always see a DME page with good CRC16 before the other device hence this swapping will guarantee that nonce_match will never be true.

98.2.1.2.4 Technology Ability Field

Technology Ability Field (A[26:0]) is a 27-bit wide field containing information indicating supported technologies specific to the selector field value when used with the single twisted-pair Auto-Negotiation Ethernet. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. The Technology Ability Field encoding for the IEEE 802.3 selector with single twisted-pair Auto-Negotiation Ethernet is described in 98B.3.

Multiple technologies may be advertised in the link codeword. A device shall support the data service ability for a technology it advertises. It is the responsibility of the Arbitration function to determine the common mode of operation shared by a link partner and to resolve multiple common modes.

98.2.1.2.5 Force MASTER-SLAVE

The force MASTER-SLAVE bit, D12, allows a device to force its MASTER-SLAVE configuration. If this bit is set to 0 then the device is in preferred mode, otherwise it is in the forced mode. The MASTER-SLAVE resolution is shown in Table 98–4.

98.2.1.2.6 Pause Ability

Pause (C0:C1) is encoded in bits D11:D10 of the base link codeword. The 2-bit Pause is encoded as follows:

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Table 98–4—MASTER-SLAVE Configuration

Local Device		Remote Device		Local Device Resolution	Remote Device Resolution
M/S	T[4]	M/S	T[4]		
0	X	0	X	Device with higher T[4:0] is MASTER, otherwise SLAVE	Device with higher T[4:0] is MASTER, otherwise SLAVE
0	X	1	0	MASTER	SLAVE
0	X	1	1	SLAVE	MASTER
1	0	0	X	SLAVE	MASTER
1	1	0	X	MASTER	SLAVE
1	0	1	0	Configuration Fault	Configuration Fault
1	0	1	1	SLAVE	MASTER
1	1	1	0	MASTER	SLAVE
1	1	1	1	Configuration Fault	Configuration Fault

a) C0 is the same as PAUSE as defined in Annex 28B

b) C1 is the same as ASM_DIR as defined in Annex 28B

The Pause encoding is defined in 28B.2, Table 28B–2. The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. The ASM_DIR bit indicates that asymmetric PAUSE is supported. The value of the PAUSE bit when the ASM_DIR bit is set indicates the direction the PAUSE frames are supported for flow across the link. Asymmetric PAUSE configuration results in independent enabling of the PAUSE receive and PAUSE transmit functions as defined by Annex 31B. See 28B.3 regarding PAUSE configuration resolution.

98.2.1.2.7 Remote Fault

Remote Fault (RF) is encoded in bit D13 of the base link codeword. The default value is logical zero. The Remote Fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the BASE-T1 AN advertisement register (register 7.514.13) is set to logical one, the RF bit in the transmitted base link codeword is set to logical one. When the RF bit in the received base link codeword is set to logical one, the Remote Fault bit in the BASE-T1 AN LP Base Page ability register (register 7.517.13) will be set to logical one, if the management function is present.

98.2.1.2.8 Acknowledge

Acknowledge (Ack) is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's link codeword. The Acknowledge Bit is encoded in bit D14 of link codeword. If no Next Page information is to be sent, this bit shall be set to logical one in the link codeword after the reception of at least one DME page with a correct CRC. If Next Page information is to be sent, this bit shall be set to logical one after the device has successfully received at least one DME page with correct CRC, and will remain set until the Next Page information has been loaded into the BASE-T1 AN NEXT PAGE transmit register (Registers 7.520, 7.521, 7.522). In order to save the current received link codeword, it shall be read from the BASE-T1 AN LP NEXT PAGE ability register (register 7.523, 7.524, 7.525) before the Next Page of transmit information is loaded into the BASE-T1 AN NEXT PAGE transmit register. After the

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COMPLETE ACKNOWLEDGE state has been entered, the link codeword will be transmitted at least three times.

98.2.1.2.9 Next Page

Next Page (NP) is encoded in bit D15 of link codeword. Support of Next Pages is mandatory. If the device does not have any Next Pages to send, the NP bit shall be set to logical zero. If a device wishes to engage in Next Page exchange, it shall set the NP bit to logical one. If a device has no Next Pages to send and its link partner has set the NP bit to logical one, it shall transmit Next Pages with Null message codes and the NP bit set to logical zero while its link partner transmits valid Next Pages. Next page exchanges will occur if either the device or its link partner sets the Next Page bit to logical one. The Next Page function is defined in 98.2.4.3.

98.2.1.3 Transmit Switch function

The Transmit Switch function shall enable the transmit path from a single technology-dependent PHY to the MDI once a highest common denominator choice has been made and Auto-Negotiation has completed. During Auto-Negotiation, the Transmit Switch function shall connect only the DME page generator controlled by the Transmit state diagram to the MDI. When a PHY is connected to the MDI through the Transmit Switch function, the signals at the MDI shall conform to all of the PHY's specifications.

98.2.2 Receive function requirements

The Receive function detects the DME page sequence, decodes the information contained within, and stores the data in rx_link_code_word[64:1]. The receive function incorporates a receive switch to control connection to the various PMAs.

98.2.2.1 DME page reception

To be able to detect the DME bits, the receiver should have the capability to receive DME signals sent with the electrical specifications of the PHY. The DME transmit signal level is specified in 98.2.1.1.4.

98.2.2.2 Receive Switch function

The Receive Switch function shall enable the receive path from the MDI to a single technology-dependent PHY once a highest common denominator choice has been made and Auto-Negotiation has completed.

During Auto-Negotiation, the Receive Switch function shall connect the DME page receiver controlled by the Receive state diagram to the MDI and the Receive Switch function shall also connect the appropriate receivers to the MDI.

98.2.2.3 Link codeword matching

The Receive function shall generate ability_match, acknowledge_match, and consistency_match variables as defined in Arbitration state diagram Figure 98–7.

98.2.3 AN half-duplex function requirements

The AN half-duplex function is defined by Figure 98–10 and ensures that only one of the link partners is transmitting a DME page at each step during the DME page exchange process. The AN half-duplex function uses a blind timer to ensure that the receiver ignores signals reflected from the channel following the end of the device's transmitted DME page. A silent timer is used to ensure that the device does not begin transmitting the DME page until after the link partner has exited from the blind timer. The half-duplex

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backoff timer resolves concurrent transmissions by using a random wait time to listen for a DME page to arrive from the link partner before the local device transmits a DME page.

98.2.4 Arbitration function requirements

The Arbitration function is defined by Figure 98–7 and ensures proper sequencing of the Auto-Negotiation function using the Transmit function, Receive function, and AN half-duplex function. The Arbitration function enables the Transmit function to advertise and acknowledge abilities. Upon indication of acknowledgment, the Arbitration function determines the highest common denominator using the priority resolution function and enables the appropriate technology-dependent PHY via the Technology Dependent Interface (see 98.4).

98.2.4.1 Renegotiation function

A Renegotiation request from any entity, such as a management agent, shall cause the Arbitration function to disable all technology-dependent PHYs and halt any transmit data and link transition activity until the break_link_timer expires. Consequently, the link partner will go into link fail and normal Auto-Negotiation resumes. The local device shall resume Auto-Negotiation after the break_link_timer has expired by issuing DME pages with the Base Page valid in tx_link_code_word[64:1]. Once Auto-Negotiation has completed, renegotiation will take place if the Highest Common Denominator technology that receives link_control = ENABLE returns link_status = FAIL. To allow the PHY an opportunity to determine link integrity using its own link integrity test function, the link_fail_inhibit_timer qualifies the link_status = FAIL indication such that renegotiation takes place if the link_fail_inhibit_timer has expired and the PHY still indicates link_status = FAIL.

98.2.4.2 Priority Resolution function

Since a local device and a link partner may have multiple common abilities, a mechanism to resolve which mode to configure is required. The mechanism used by Auto-Negotiation is a Priority Resolution function that predefines the hierarchy of supported technologies. The single PHY enabled to connect to the MDI by Auto-Negotiation shall be the technology corresponding to the bit in the Technology Ability Field common to the local device and link partner that has the highest priority as defined in 98B.4 (listed from highest priority to lowest priority).

The common technology is referred to as the *highest common denominator*, or HCD, technology. If the local device receives a Technology Ability Field with a bit set that is reserved, the local device shall ignore that bit for priority resolution. Determination of the HCD technology occurs on entrance to the AN GOOD CHECK state. In the event that there is no common technology, HCD shall have a value of “NULL,” indicating that no PHY receives link_control = ENABLE and link_status[HCD] = FAIL.

98.2.4.3 Next Page function

The Next Page function uses the Auto-Negotiation arbitration mechanisms to allow exchange of Next Pages of information, which may follow the transmission and acknowledgment procedures used for the base link codeword. The Next Page has both Message Code Field and Unformatted Code Fields.

A dual acknowledgment system is used. Acknowledge (Ack) is used to acknowledge receipt of the information; Acknowledge 2 (Ack2) is used to indicate that the receiver is able to act on the information (or perform the task) defined in the message.

The Toggle (T) bit is used to ensure proper synchronization between the local device and the link partner.

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Next page exchange occurs after the base link codewords have been exchanged if either end of the link segment set the Next Page bit to logical one indicating that it had at least one Next Page to send. Next page exchange consists of using the normal Auto-Negotiation arbitration process to send Next Page messages.

The Next Page contains two message encodings. The message encodings are defined as follows: message code, which contains predefined 11-bit codes, and unformatted code, which contains 32-bit codes. Multiple Next Pages with appropriate message codes and unformatted codes can be transmitted to send extended messages. Each series of Next Pages shall have a Message code that defines how the Unformatted codes will be interpreted. Any number of Next Pages may be sent in any order; however, it is recommended that the total number of Next Pages sent be kept small to minimize the link startup time.

Next Page transmission ends when both ends of a link segment set their Next Page bits to logical zero, indicating that neither has anything additional to transmit. It is possible for one device to have more pages to transmit than the other device. Once a device has completed transmission of its Next Page information, it shall transmit Next Pages with Null message codes and the NP bit set to logical zero while its link partner continues to transmit valid Next Pages. An Auto-Negotiation able device shall recognize reception of Message Pages with Null message codes as the end of its link partner's Next Page information.

98.2.4.3.1 Next page encodings

The Next Page shall use the encoding shown in Table 98–5 and Table 98–6 for the NP, Ack, MP, Ack2, and T bits. These bits shall function as specified in 98.2.1.2.9, 98.2.1.2.8, 28.2.3.4.5, 28.2.3.4.6, and 28.2.3.4.7 respectively. There are two types of Next Page encodings: message and unformatted. For message Next Pages, the MP bit shall be set to logical one, the 11-bit field D[10:0] shall be encoded as a Message Code Field and D[47:16] shall be encoded as Unformatted Code Field. For Unformatted Next Pages, the MP bit shall be set to logical ZERO: D[10:0] and D[47:16] shall be encoded as the Unformatted Code Field.

Table 98–5—Message Next Page

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	T	Ack2	MP	Ack	NP
D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
U0	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15
D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47
U16	U17	U18	U19	U20	U21	U22	U23	U24	U25	U26	U27	U28	U29	U30	U31

Table 98–6—Unformatted Next Page

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
U0	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	T	Ack2	MP	Ack	NP
D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	U21	U22	U23	U24	U25	U26
D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47
U27	U28	U29	U30	U31	U32	U33	U34	U35	U36	U37	U38	U39	U40	U41	U42

98.2.4.3.2 Use of Next Pages

Next page exchange shall commence after the Base Page exchange if either device requests it by setting the NP bit to logical one.

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Next page exchange shall continue until neither device on a link has more pages to transmit as indicated by the NP bit. A Next Page with a Null Message Code Field value shall be sent if the device has no other information to transmit.

A message code can carry either a specific message or information that defines how the corresponding unformatted codes should be interpreted.

98.3 State diagram variable to Auto-Negotiation register mapping

The state diagrams of Figure 98–7 to Figure 98–10 generate and accept variables of the form "mr_x," where x is an individual signal name. These variables comprise a management interface to communicate Auto-Negotiation information to and from the management entity. Clause 45 MDIO registers are defined in MMD7 to support Auto-Negotiation. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the information is recommended.

Table 98–7 describes the MDIO register to the state diagrams variable mapping.

Table 98–7—State diagram variable to Single twisted-pair Auto-Negotiation MDIO register mapping

State diagram variable	Description / MDIO register mapping
mr_adv_ability[48:1]	{7.516.15:0, 7.515.15:0, 7.514.15:0} BASE-T1 AN advertisement registers
mr_autoneg_complete	7.513.5 Auto-Negotiation complete
mr_autoneg_enable	7.512.12 Auto-Negotiation enable
mr_lp_adv_ability[48:1]	For Base Page: {7.519.15:0, 7.518.15:0, 7.517.15:0} BASE-T1 AN LP Base Page ability registers For Next Page(s): {7.525.15:0, 7.524.15:0, 7.523.15:0} BASE-T1 AN LP NEXT PAGE ability register
mr_main_reset	7.512.15 AN reset
mr_next_page_loaded	Set on write to BASE-T1 AN NEXT PAGE transmit register; cleared by Arbitration state diagram
mr_np_tx[48:1]	{7.522.15:0, 7.521.15:0, 7.520.15:0} BASE-T1 AN NEXT PAGE transmit register
mr_page_rx	7.513.6 Page received
mr_restart_negotiation	7.512.9 Restart Auto-Negotiation
set to 1	7.513.3 Auto-Negotiation ability

98.4 Technology-Dependent Interface

The Technology-Dependent Interface is the communication mechanism between each technology's PMA and the Auto-Negotiation function. Auto-Negotiation can support multiple technologies, all of which need not be implemented in a given device. Each of these technologies may utilize its own technology-dependent link integrity test function.

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98.4.1 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium. The purpose of this primitive is to give the Auto-Negotiation function a means of determining the validity of received code elements.

98.4.1.1 Semantics of the service primitive

PMA_LINK.indication(link_status)

The link_status parameter shall assume one of two values: OK or FAIL, indicating whether the underlying receive channel is intact and enabled (OK) or not intact (FAIL).

98.4.1.2 When generated

A technology-dependent PMA generates this primitive to indicate a change in the value of link_status.

98.4.1.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the state diagram of Figure 98–7.

98.4.2 PMA_LINK.request

This primitive is generated by Auto-Negotiation to allow it to enable and disable operation of the PMA.

98.4.2.1 Semantics of the service primitive

PMA_LINK.request(link_control)

The link_control parameter shall assume one of two values: DISABLE or ENABLE.

The link_control=DISABLE mode shall be used by the Auto-Negotiation function to disable PMA processing.

The link_control=ENABLE mode shall be used by Auto-Negotiation to turn control over to a single PMA for all normal processing functions.

98.4.2.2 When generated

The Auto-Negotiation function shall generate this primitive to indicate to the PHY how to respond, in accordance with the state diagram of Figure 98–7. Upon power-on or reset, if the Auto-Negotiation function is enabled (mr_autoneg_enable=true) the PMA_LINK.request(DISABLE) message shall be issued to all technology-dependent PMAs.

98.4.2.3 Effect of receipt

This primitive affects operation of the underlying PMA.

98.5 Detailed functions and state diagrams

The notation used in state diagrams follows the conventions in Clause 28. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

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Auto-Negotiation shall implement the Transmit state diagram, Receive state diagram, half-duplex state diagram, and Arbitration state diagram. Additional requirements to these state diagrams are made in the respective functional requirements sections. Options to these state diagrams clearly stated as such in the functional requirements sections or state diagrams shall be allowed. In the case of any ambiguity between stated requirements and the state diagrams, the state diagrams shall take precedence.

98.5.1 State diagram variables

A variable with "_[x]" appended to the end of the variable name indicates a variable or set of variables as defined by "x". "x" may be as follows:

— all; represents all specific technology-dependent PMAs supported in the local device.
— HCD; represents the single technology-dependent PMA chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution.
— notHCD; represents all technology-dependent PMAs not chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution.
— 1GigT1; represents that the 1000BASE-T1 PMA is the signal source.
— 2.5GigT1; represents that the 2.5GBASE-T1 PMA is the signal source.
— 5GigT1; represents that the 5GBASE-T1 PMA is the signal source.
— 10GigT1; represents that the 10GBASE-T1 PMA is the signal source.

Variables with [48:1] appended to the end of the variable name indicate arrays that can be directly mapped to 48-bit registers. For these variables, "[x]" indexes an element or set of elements in the array, where "[x]" may be as follows:

a) Any integer
b) Any range of integers
c) Any variable that takes on integer values
d) NP; represents the index of the Next Page bit
e) ACK; represents the index of the Acknowledge bit
f) RF; represents the index of the Remote Fault bit

Variables of the form "mr_x", where x is a label, comprise a management interface that is intended to be connected to the Management function. However, an implementation-specific management interface may provide the control and status function of these bits. The mapping between state diagram variables and Single twisted-pair Auto-Negotiation MDIO registers is shown in Table 98–7.

ability_match
Indicates that at least one link codeword with good CRC16 was received.
Values:
false: at least one link codeword with good CRC16 has not been received (default)
true: at least one link codeword with good CRC16 has been received

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

ability_match_word [48:1]
A 48-bit array that is loaded upon transition to Acknowledge Detect state with the value of the link codeword that caused ability_match = true for that transition. For each element in the array transmitted.
Values:
ZERO: data bit is logical zero
ONE: data bit is logical one

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

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ack_finished

Status indicating that the final remaining_ack_cnt link codewords with the Ack bit set have been transmitted.

Values:

- false: more link codewords with the Ack bit set to logical one is transmitted
- true: all remaining link codewords with the Ack bit set to logical one have been transmitted

ack_nonce_match

Indicates whether the echoed nonce received from the link partner matches the transmitted nonce field sent by the local device. The echoed nonce value from the DME page that caused acknowledge_match to be set is used for this test.

Values:

- false: link partner echoed nonce does not equal local device transmitted nonce
- true: link partner echoed nonce equals local device transmitted nonce

acknowledge_match

Indicates that at least one link codeword with the Acknowledge bit set and with good CRC16 was received. The link codeword that initially set the ability_match variable should not be used to set this variable.

Values:

- false: at least one link codeword with the Acknowledge bit set and with good CRC16 has not been received (default)
- true: at least one link codeword with the Acknowledge bit set and with good CRC16 has been received

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

an_link_good

Indicates that Auto-Negotiation has completed.

Values:

- false: negotiation is in progress (default)
- true: negotiation is complete, forcing the Transmit and Receive functions to IDLE

an_receive_idle

Indicates that the Receive state diagram is in the IDLE state.

Values:

- false: the Receive state diagram is not in the IDLE state (default)
- true: the Receive state diagram is in the IDLE state

ANSP

This variable contains the type of the selected Auto-Negotiation speed.

Values:

- HSM: high-speed mode
- LSM: low-speed mode

base_page

Status indicating that the page currently being transmitted by Auto-Negotiation is the initial link codeword encoding used to communicate the device's abilities.

Values:

- false: a page other than base link codeword is being transmitted
- true: the base link codeword is being transmitted

code_sel

A random or pseudo-random value uniformly distributed. A new value is generated each time the

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variable code_sel is used.
Values:
ZERO: a zero has been assigned
ONE: a one has been assigned

complete_ack
Controls the counting of transmitted link codewords that have their Acknowledge bit set.
Values:
false: transmitted link codewords with the Acknowledge bit set are not counted (default)
true: transmitted link codewords with the Acknowledge bit set are counted

consistency_match
Indicates that the ability_match_word is the same as the link codeword that caused acknowledge_match to be set.
Values:
false: the link codeword that caused ability_match to be set is not the same as the link codeword that caused acknowledge_match to be set, ignoring the Acknowledge bit value and the echoed nonce value
true: the link codeword that caused ability_match to be set is the same as the link codeword that caused acknowledge_match to be set, ignoring the Acknowledge bit value and the echoed nonce value

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

detect_mv_end
Status indicating that the receiver has detected the end delimiter.
Values:
false: set to false after any Receive State Diagram state transition (default)
true: end delimiter has been detected

detect_mv_start
Status indicating that the receiver has detected a Start Delimiter as defined in 98.2.1.1.1.
Values:
false: set to false after any Receive State Diagram state transition (default)
true: Start Delimiter has been detected

detect_transition
Status indicating that the receiver has detected a transition.
Values:
false: set to false after any Receive State Diagram state transition (default)
true: set to true when a transition is received

incompatible_link
Parameter used following Priority Resolution to indicate the resolved link is incompatible with the local device settings. A device's ability to set this variable to true is optional.
Values:
false: a compatible link exists between the local device and link partner (default)
true: optional indication that Priority Resolution has determined no highest common denominator exists following the most recent negotiation

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

link_control_[x]
Controls the connection of each PMD to the MDI. When all PMD transmitters are isolated from the MDI, the AN transmitter is connected to the MDI.

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Values:
DISABLE: isolates the PMD from the MDI
ENABLE: connects the PMD (both transmit and receive) to the MDI

link_status_[x]
The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_autoneg_complete
Status indicating whether Auto-Negotiation has completed or not.
Values:
false: Auto-Negotiation has not completed
true: Auto-Negotiation has completed

mr_autoneg_enable
Controls the enabling and disabling of the Auto-Negotiation function.
Values:
false: Auto-Negotiation is disabled
true: Auto-Negotiation is enabled

mr_adv_ability[48:1]
A 48-bit array that contains the Advertised Abilities link codeword. For each element within the array:
Values:
ZERO: data bit is logical zero
ONE: data bit is logical one

mr_lp_adv_ability[48:1]
A 48-bit array that contains the link partner's Advertised Abilities link codeword. For each element within the array:
Values:
ZERO: data bit is logical zero
ONE: data bit is logical one

mr_main_reset
Controls the resetting of the Auto-Negotiation state diagrams.
Values:
false: do not reset the Auto-Negotiation state diagrams
true: reset the Auto-Negotiation state diagrams

mr_next_page_loaded
Status indicating whether a new page has been loaded into the BASE-T1 AN NEXT PAGE transmit register (see 45.2.7.24).
Values:
false: a New Page has not been loaded
true: a New Page has been loaded

mr_np_tx[48:1]
A 48-bit array that contains the new Next Page to transmit. For each element within the array:
Values:
ZERO: data bit is logical zero
ONE: data bit is logical one

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mr_page_rx

Status indicating whether a New Page has been received. A New Page has been successfully received when acknowledge_match = true and consistency_match = true and the link codeword has been written to mr_lp_adv_ability[48:1].

Values:

false: a New Page has not been received
true: a New Page has been received

mr_restart_negotiation

Controls the entrance to the TRANSMIT DISABLE state to break the link before Auto-Negotiation is allowed to renegotiate via management control.

Values:

false: renegotiation is not taking place
true: renegotiation is started

multispeed_autoneg_reset

See 98.5.6.1.

nonce_match

Indicates whether the transmitted nonce received from the link partner matches the transmitted nonce field sent by the local device.

Values:

false: link partner transmitted nonce does not equal local device transmitted nonce
true: link partner transmitted nonce equals local device transmitted nonce

np_rx

Flag to hold the value of rx_link_code_word[NP] upon entry to the COMPLETE ACKNOWLEDGE state. This value is associated with the value of rx_link_code_word[NP] when acknowledge_match was last set.

Values:

ZERO: local device np_rx bit equals a logical zero
ONE: local device np_rx bit equals a logical one

page_polarity

Starting polarity of the page.

Values:

ZERO: starting polarity of page is negative
ONE: starting polarity of page is positive

power_on

Condition that is true until such time as the power supply for the device that contains the Auto-Negotiation state diagrams has reached the operating region or the device has low-power mode set via 1000BASE-T1 PMA control register bit 1.2304.11 or via 10BASE-T1L PMA control register bit 1.2294.11.

Values:

false: the device is completely powered (default)
true: the device has not been completely powered

receive_blind

Controls whether the receiver should ignore activity on the line.

Values:

true: ignore received DME transitions
false: accept received DME transitions

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receive_DME_active

Status indicating whether or not a DME page reception is in progress.

Values:

- true: DME page reception in progress
- false: DME page reception completed

rx_link_code_word[64:1]

A 64-bit array that contains the data bits to be received from a DME page. For each element within the array:

Values:

- ZERO: data bit is a logical zero
- ONE: data bit is a logical one

rx_nonce[4:0]

A 5-bit array that contains the transmitted nonce received from the DME page that caused ability_match = true. For each element within the array:

Values:

- ZERO: data bit is a logical zero
- ONE: data bit is a logical one

TD_AUTONEG

Controls the signal sent by Auto-Negotiation on the TD_AUTONEG circuit.

Values:

- disable: transmission of Auto-Negotiation signals is disabled
- idle: Auto-Negotiation maintains the current signal level on the MDI
- mv_end_delimiter: Auto-Negotiation causes the transmission of the end delimiter on the MDI
- mv_start_delimiter: Auto-Negotiation causes the transmission of the Start Delimiter on the MDI as defined in 98.2.1.1.1
- transition: Auto-Negotiation causes a transition in the level on the MDI

toggle_rx

Flag to keep track of the state of the link partner's Toggle bit.

Values:

- ZERO: link partner's Toggle bit equals logical zero
- ONE: link partner's Toggle bit equals logical one

toggle_tx

Flag to keep track of the state of the local device's Toggle bit.

Values:

- ZERO: local device's Toggle bit equals logical zero
- ONE: local device's Toggle bit equals logical one

transmit_ability

Controls the transmission of the link codeword containing tx_link_code_word[64:1].

Values:

- false: any transmission of tx_link_code_word[64:1] is halted (default)
- true: the transmit state diagram begins sending tx_link_code_word[64:1]

transmit_ack

Controls the setting of the Acknowledge bit in the tx_link_code_word[64:1] to be transmitted.

Values:

- false: sets the Acknowledge bit in the transmitted tx_link_code_word[64:1] to a logical zero (default)

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true: sets the Acknowledge bit in the transmitted tx_link_code_word[64:1] to a logical one

transmit_disable

Controls the transmission of tx_link_code_word[64:1].

Values:

false: tx_link_code_word[64:1] transmission is allowed (default)

true: tx_link_code_word[64:1]transmission is halted

transmit_DME_done

Status indicating the DME page transmission completed.

Values:

true: DME page transmission completed

false: DME page transmission in progress

transmit_DME_wait

Control indication whether a DME page can be transmitted.

Values:

true: pause DME page transmission

false: continue DME page transmission

transmit_mv_end_done

Status indicating that the transmission of the end delimiter has completed.

Values:

false: transmission of the end delimiter is in progress

true: transmission of the end delimiter has completed

transmit_mv_start_done

Status indicating that the transmission of the Start Delimiter defined in 98.2.1.1.1 has been completed.

Values:

false: transmission of the Start Delimiter is in progress

true: transmission of the Start Delimiter has been completed

tx_link_code_word[64:1]

A 64-bit array that contains the data bits to be transmitted in an DME page. tx_link_code_word[48:1] contains the Auto-Negotiation page to be transmitted. tx_link_code_word[64:49] contains the CRC16. This array may be loaded from mr_adv_ability or mr_np_tx. For each element within the array:

Values:

ZERO: data bit is logical zero

ONE: data bit is logical one.

98.5.2 State diagram timers

All timers operate in the manner described in 40.4.5.2.

When operating in high-speed mode, the following timer value definitions shall apply:

backoff_timer_[HSM]

Timer for the random amount of time to wait for a page to arrive from the link partner before transmitting a page. The timer shall expire according to the formula below after being started. If T[4] bit is 1, the timer duration is (6805 ns to 6925 ns) + (random integer from 0 to 15) × (2120 ns to 2240 ns).

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If T[4] bit is 0, the timer duration is (7895 ns to 8015 ns) + (random integer from 0 to 15) × (2120 ns to 2240 ns).

A new random integer from 0 to 15 inclusive is generated every time the backoff_timer_[HSM] is started. The random value should be uniformly distributed.

blind_timer_[HSM]

Timer for the amount of time to blind the receiver after end of transmission to prevent the device from seeing its own echo. The timer shall expire 2000 ns to 2120 ns after being started.

break_link_timer_[HSM]

Timer for the amount of time to wait in TRANSMIT DISABLE to assure that the link partner will exit from either ACKNOWLEDGE DETECT or NEXT PAGE WAIT; effect on the link partner in other states is not defined. The timer shall expire 300 µs to 305 µs after being started.

clock_detect_max_timer_[HSM]

Timer for the maximum time between detection of differential Manchester clock transitions. The clock_detect_max_timer_[HSM] shall expire 63 ns to 75 ns after being started or restarted.

clock_detect_min_timer_[HSM]

Timer for the minimum time between detection of differential Manchester clock transitions. The clock_detect_min_timer_[HSM] shall expire 45 ns to 57 ns after being started or restarted.

data_detect_max_timer_[HSM]

Timer for the maximum time between a clock transition and the following data transition. This timer is used in conjunction with the data_detect_min_timer_[HSM] to detect whether the data bit between two clock transitions is a logical zero or a logical one. The data_detect_max_timer_[HSM] shall expire 33 ns to 45 ns from the last clock transition.

data_detect_min_timer_[HSM]

Timer for the minimum time between a clock transition and the following data transition. This timer is used in conjunction with the data_detect_max_timer_[HSM] to detect whether the data bit between two clock transitions is a logical zero or a logical one. The data_detect_min_timer_[HSM] shall expire 15 ns to 27 ns from the last clock transition.

interval_timer_[HSM]

Timer for the separation of a transmitted clock pulse from a data bit. The interval_timer_[HSM] shall expire 30 ns ± 0.01% from each clock pulse and data bit.

page_test_max_timer_[HSM]

Timer for the maximum time between detection of start and end delimiters. The page_test_max_timer_[HSM] shall expire 4800 ns to 4920 ns after being started or restarted.

receive_DME_timer_[HSM]

Timer for the maximum amount of time to receive a complete page before timeout. The timer shall expire 6805 ns to 6925 ns after being started.

rx_wait_timer_[HSM]

Timer for the maximum time between detection of DME pages. This timer is used to detect whether the link partner is transmitting DME pages. The rx_wait_timer_[HSM] shall expire 15 µs to 17 µs after being started or restarted.

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silent_timer_[HSM]

Timer for the amount of time to wait after receiving a page before transmitting a page. The timer shall expire 2120 ns to 2240 ns after being started.#

When operating in low-speed mode, the following timer value definitions shall apply:

backoff_timer_[LSM]

Timer for the random amount of time to wait for a page to arrive from the link partner before transmitting a page. The timer shall expire according to the formula below after being started.
If T[4] bit is 1, the timer duration is (156 300 ns to 159 500 ns) + (random integer from 0 to 15) × (31 400 ns to 34 600 ns).
If T[4] bit is 0, the timer duration is (172 800 ns to 176 000 ns) + (random integer from 0 to 15) × (31 400 ns to 34 600 ns).
A new random integer from 0 to 15 inclusive is generated every time the backoff_timer_[LSM] is started. The random value should be uniformly distributed.

blind_timer_[LSM]

Timer for the amount of time to blind the receiver after end of transmission to prevent the device from seeing its own echo. The timer shall expire 28 200 ns to 31 400 ns after being started.

break_link_timer_[LSM]

Timer for the amount of time to wait in TRANSMIT DISABLE to assure that the link partner will exit from either ACKNOWLEDGE DETECT or NEXT PAGE WAIT; effect on the link partner in other states is not defined. The timer shall expire 8000 µs to 8133 µs after being started.

clock_detect_max_timer_[LSM]

Timer for the maximum time between detection of differential Manchester clock transitions. The clock_detect_max_timer_[LSM] shall expire 1680 ns to 2000 ns after being started or restarted.

clock_detect_min_timer_[LSM]

Timer for the minimum time between detection of differential Manchester clock transitions. The clock_detect_min_timer_[LSM] shall expire 1200 ns to 1520 ns after being started or restarted.

data_detect_max_timer_[LSM]

Timer for the maximum time between a clock transition and the following data transition. This timer is used in conjunction with the data_detect_min_timer_[LSM] to detect whether the data bit between two clock transitions is a logical zero or a logical one. The data_detect_max_timer_[LSM] shall expire 880 ns to 1200 ns from the last clock transition.

data_detect_min_timer_[LSM]

Timer for the minimum time between a clock transition and the following data transition. This timer is used in conjunction with the data_detect_max_timer_[LSM] to detect whether the data bit between two clock transitions is a logical zero or a logical one. The data_detect_min_timer_[LSM] shall expire 400 ns to 720 ns from the last clock transition.

interval_timer_[LSM]

Timer for the separation of a transmitted clock pulse from a data bit. The interval_timer_[LSM] shall expire 800 ns ± 0.005% from each clock pulse and data bit.

page_test_max_timer_[LSM]

Timer for the maximum time between detection of start and end delimiters. The page_test_max_timer_[LSM] shall expire 128 000 ns to 131 200 ns after being started or restarted.

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receive_DME_timer_[LSM]
: Timer for the maximum amount of time to receive a complete page before timeout. The timer shall expire 156 300 ns to 159 500 ns after being started.

rx_wait_timer_[LSM]
: Timer for the maximum time between detection of DME pages. This timer is used to detect whether the link partner is transmitting DME pages. The rx_wait_timer_[LSM] shall expire 330 μs to 370 μs after being started or restarted.

silent_timer_[LSM]
: Timer for the amount of time to wait after receiving a page before transmitting a page. The timer shall expire 31 400 ns to 34 600 ns after being started.

Depending on the selected PHY type, done by Auto-Negotiation, the following timer values shall be used:

link_fail_inhibit_timer_[HCD]
: Timer for qualifying a link_status=FAIL indication or a link_status=OK indication when a specific technology link is first being established. A link will be considered "failed" only if the link_fail_inhibit_timer_[HCD] has expired and the link has still not gone into the link_status=OK state. The expiration time of the link_fail_inhibit_timer_[HCD] shall be dependent on the selected PHY type. For all PHY types, except 10BASE-T1L and 10BASE-T1S, this timer shall expire 97 ms to 98 ms after entering the AN GOOD CHECK state. For a 10BASE-T1L PHY, this timer shall expire 3030 ms to 3090 ms after entering the AN GOOD CHECK state. For a 10BASE-T1S PHY, this timer shall expire 400 ms to 405 ms after entering the AN GOOD CHECK state.

NOTE—The link_fail_inhibit_timer_[HCD] expiration value is greater than the time required for the link partner to complete Auto-Negotiation after the local device has completed Auto-Negotiation plus the time required for the specific technology to enter the link_status=OK state.

98.5.3 State diagram counters

remaining_ack_cnt
: A counter that may take on integer values from 0 to 3. The number of additional link codewords with the Acknowledge Bit set to logical one to be sent to ensure that the link partner receives the acknowledgment.
Values:
not_done: positive integers between 0 and 2 inclusive
done: positive integer 3
init: counter is reset to zero

rx_bit_cnt
: A counter that may take on integer values from 0 to 64. This counter is used to keep a count of data bits received from a DME page and to ensure that when erroneous extra transitions are received, the first 48 bits are kept while the next 16 bits are used for CRC16 check and any additional bits are ignored. When this counter reaches 64, enough data bits have been received. This counter does not increment beyond 64 and does not return to 0 until it is reinitialized.

tx_bit_cnt
: A counter that may take on integer values from 1 to 64. This counter is used to keep a count of data bits sent within a DME page. When this counter reaches 64, all data bits have been sent.

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98.5.4 Function

CRC16(x[48:1])

Returns the output of the CRC16 generator described in 98.2.1.1.1 after processing the 48-bit input x.

98.5.5 State diagrams

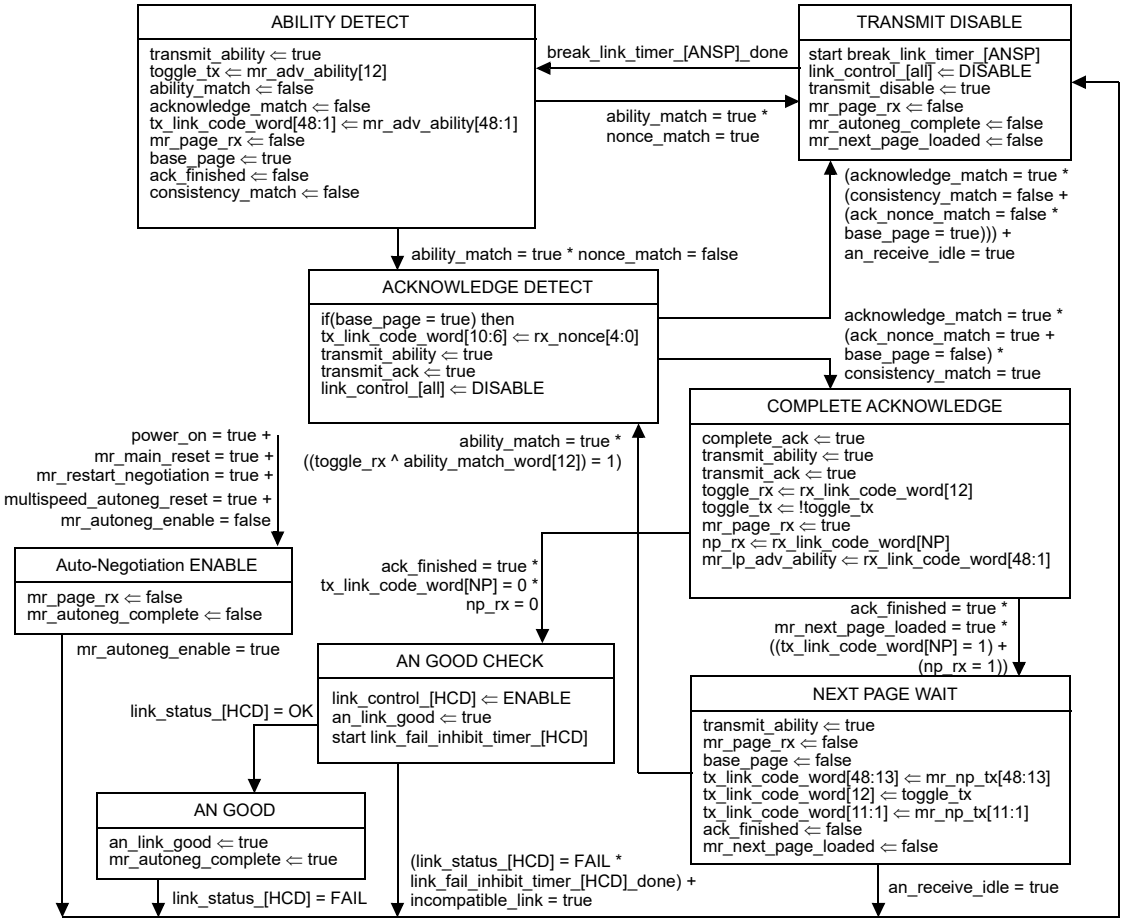

Figure 98–7—Arbitration state diagram

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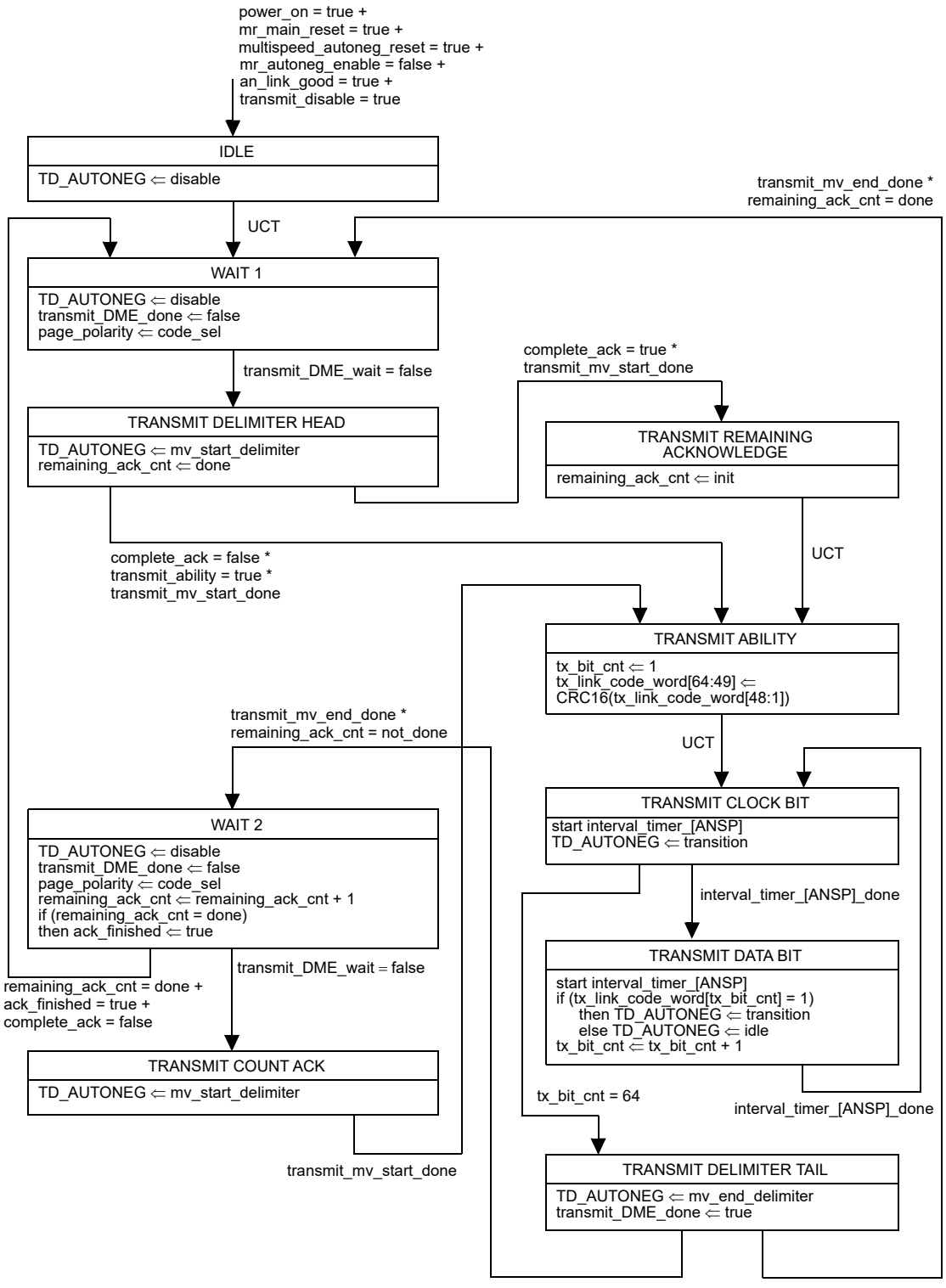

Figure 98–8—Transmit state diagram

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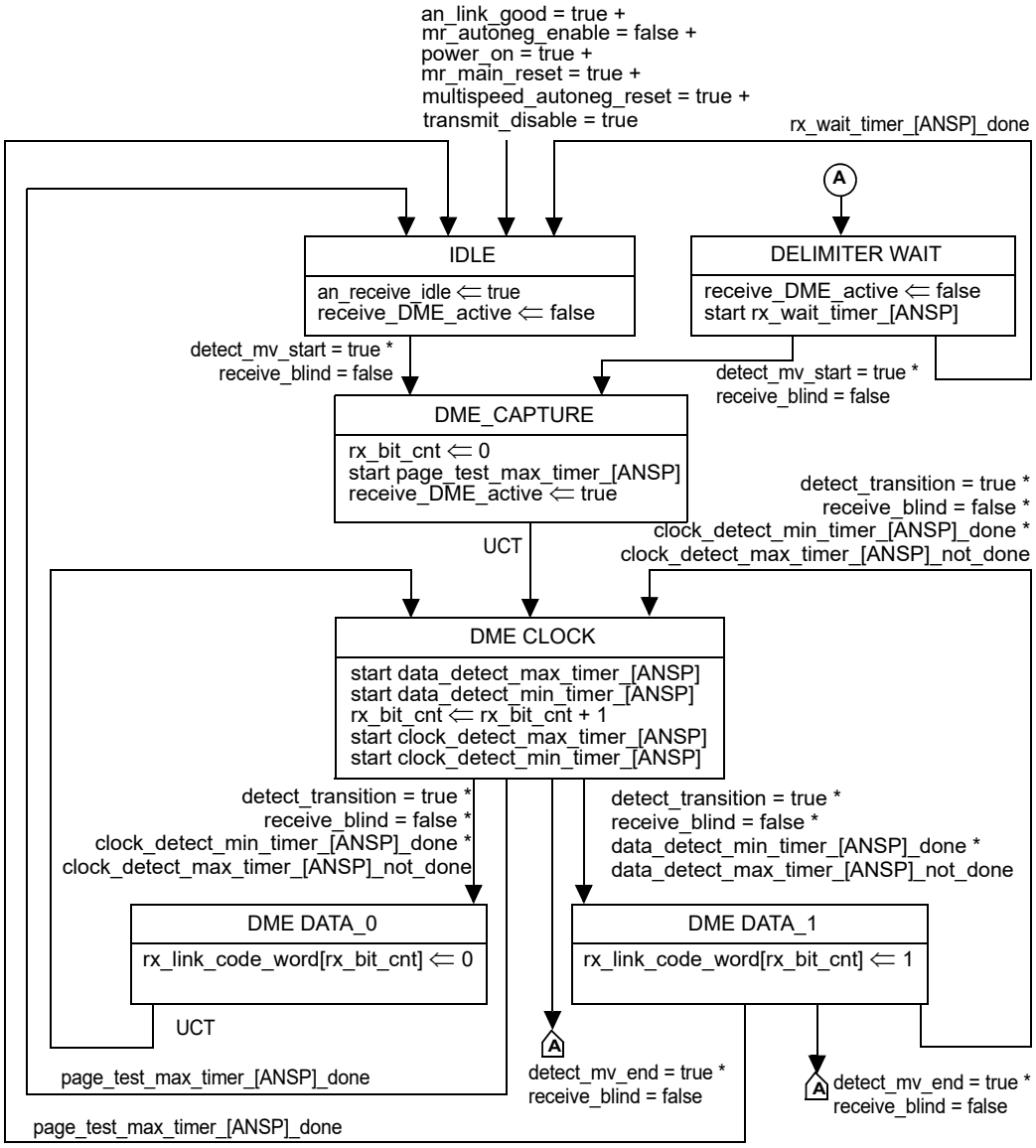

Figure 98–9—Receive state diagram

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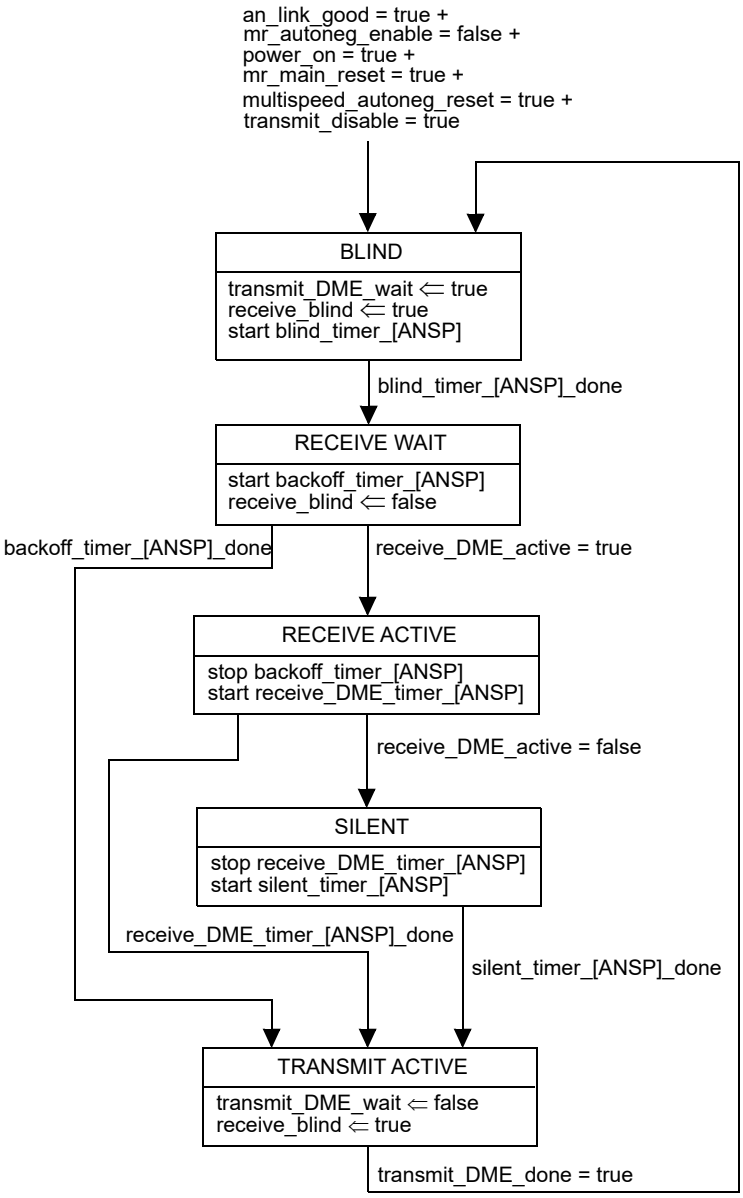

Figure 98–10—Half-duplex state diagram

98.5.6 High-speed and low-speed Auto-Negotiation modes

A PHY supporting two different Auto-Negotiation speeds, as described in 98.2.1.1.2, shall implement the behavior shown in Figure 98–11. Figure 98–11 determines the mode used for the timers in Figure 98–7, Figure 98–8, Figure 98–9, Figure 98–10, and Figure 98–11 through the variable ANSP and synchronizes them through the variable multispeed_autoneg_reset.

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A PHY supporting only one Auto-Negotiation speed shall implement the behavior as shown in Figure 98–7, Figure 98–8, Figure 98–9, and Figure 98–10, using the associated timer values for high-speed mode (HSM) or low-speed mode (LSM) Auto-Negotiation as described in 98.5.2.

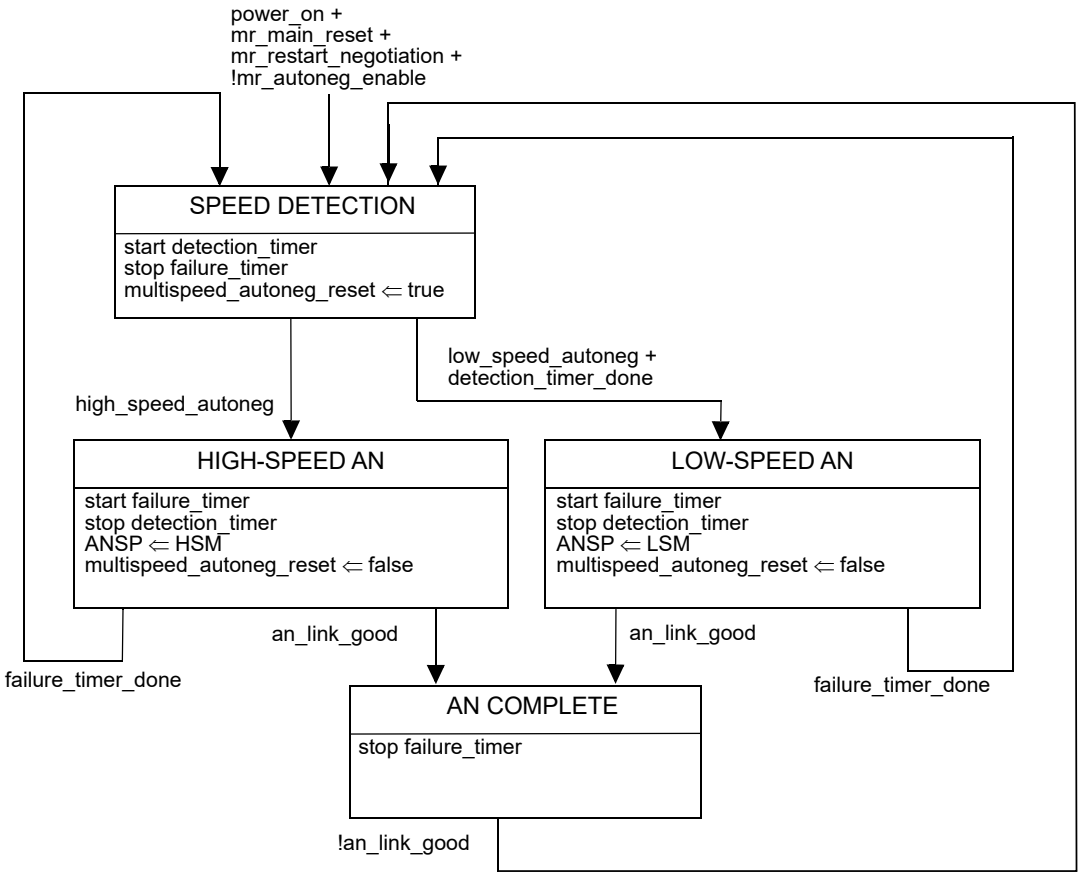

Figure 98–11—Auto-Negotiation—high-speed mode and low-speed mode selection

98.5.6.1 Variables

an_link_good
: See 98.5.1.

ANSP
: See 98.5.1.

mr_autoneg_enable
: See 98.5.1.

mr_main_reset
: See 98.5.1.

mr_restart_negotiation
: See 98.5.1.

multispeed_autoneg_reset
: If two different Auto-Negotiation speeds are implemented and this variable is set to true by the state diagram in Figure 98–11, then the state diagrams in Figure 98–7, Figure 98–8,

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Figure 98–9, and Figure 98–10 are restarted. If only single speed Auto-Negotiation is implemented, then this variable remains set to false.
Values: true: Auto-Negotiation state diagrams are restarted
false: Auto-Negotiation state diagrams are in normal operation

power_on
See 98.5.1.

98.5.6.2 Functions

high_speed_autoneg
This function returns true if at least the last 12 received DME pulses are within the allowed range for the high-speed Auto-Negotiation communication (15 ns to 135 ns pulse width) including the violations of the DME encoding within the start delimiter; otherwise, this function returns false.
Values: true or false

low_speed_autoneg
This function returns true if at least the last 12 received DME pulses are within the allowed range for the low-speed Auto-Negotiation communication (400 ns to 2000 ns pulse width) including the violations of the DME encoding within the start delimiter; otherwise, this function returns false.
Values: true or false

98.5.6.3 Timers

All timers operate in the manner described in 40.4.5.2.

detection_timer
This timer limits the maximum time for detection of Auto-Negotiation frames sent by the far end PHY, before starting to send its own Auto-Negotiation frames at low-speed. This timer is not automatically restarted after expiration. A new random integer from 0 to 15 inclusive is generated every time the detection_timer is started. The random value should be uniformly distributed.
Timer value: (10 ms ± 0.1 ms) + (random integer from 0 to 15) × (0.5 ms ± 0.05 ms)

failure_timer
This timer limits the maximum time for the underlying Auto-Negotiation state diagrams to complete the Auto-Negotiation process before restarting the Auto-Negotiation process. This timer is not automatically restarted after expiration.
Timer value: 250 ms ± 1 ms

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98.6 Protocol implementation conformance statement (PICS) proforma for Clause 98, Auto-Negotiation for Single Differential-Pair Media[171]

98.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 98, Auto-Negotiation for Single Differential-Pair Media, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

98.6.2 Identification

98.6.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

98.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 98, Auto-Negotiation for Single Differential-Pair Media
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[171] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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98.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*ANSM	Auto-Negotiation Speed Mode	98.5.6		O	Yes [ ] No [ ]
*HSM	High-Speed Mode	98.5.2, 98.5.6		O	Yes [ ] No [ ]
*LSM	Low-Speed Mode	98.5.2, 98.5.6		O	Yes [ ] No [ ]
*10T1L	10BASE-T1L PHY type	98.5.2		O	Yes [ ] No [ ]
*10T1S	10BASE-T1S PHY type	98.5.2		O	Yes [ ] No [ ]

98.6.4 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	Single twisted-pair Auto-Negotiation function	98.2	Provide Auto-Negotiation transmit, Auto-Negotiation receive, Auto-Negotiation half-duplex, and Auto-Negotiation arbitration	M	Yes [ ]
G2	Auto-Negotiation functions	98.2		M	Yes [ ]
G3	PHY support for High-Speed Mode	98.2.1, 98.5.6		ANSM: O.1	Yes [ ] No [ ] N/A [ ]
G4	PHY support for Low-Speed Mode	98.2.1, 98.5.2, 98.5.6		ANSM: O.1	Yes [ ] No [ ] N/A [ ]

98.6.5 DME transmission

Item	Feature	Subclause	Value/Comment	Status	Support
DME1	DME pages	98.2.1.1	Not be transmitted when Auto-Negotiation is complete and the highest common denominator PHY has been enabled.	M	Yes [ ]
DME2	DME page encoding levels	98.2.1.1.1	Transmit either a +1 or –1 level	M	Yes [ ]
DME3	DME Page 64 odd-numbered transmission positions	98.2.1.1.1	Contain a transition	M	Yes [ ]
DME4	DME Page 64 even-numbered transmission positions	98.2.1.1.1	Represent data	M	Yes [ ]
DME5	DME Page first 48 even-numbered positions	98.2.1.1.1	Carry the data of the Auto-Negotiation page	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DME6	CRC16	98.2.1.1.1	Comply with Figure 98–3 and initialize 16 delay elements to zero	M	Yes [ ]
DME7	Timing parameters for DME pages	98.2.1.1.2	Table 98–1	M	Yes [ ]
DME8	DME page transitions in high-speed mode	98.2.1.1.2	Occur within ± 0.8 ns of their ideal position	HSM: M	Yes [ ] N/A [ ]
DME9	DME page transitions in low-speed mode	98.2.1.1.2	Occur within ± 10 ns of their ideal position	LSM: M	Yes [ ] N/A [ ]
DME10	Transmit differential signal at the MDI	98.2.1.1.4	Within range of 1 V ± 30% peak-to-peak when measured in reference to a 100 Ω termination	M	Yes [ ]

98.6.6 Link codeword encoding

Item	Feature	Subclause	Value/Comment	Status	Support
DT1	Base Page transmitted within a DME page	98.2.1.2	Convey the encoding shown in Table 98–2	M	Yes [ ]
DT2	Encoding for link codeword(s) used inside a Next Page exchange	98.2.1.2	In a DME page, D0 is the first bit transmitted	M	Yes [ ]
DT3	RF, ACK, NP bits	98.2.1.2	Function as specified in 98.2.1.2.7, 98.2.1.2.8, and 98.2.1.2.9, respectively	M	Yes [ ]
DT4	Reserved combinations of the Selector Field	98.2.1.2.1	Not be transmitted	M	Yes [ ]
DT5	Echoes Nonce Field bad	98.2.1.2.2	Contain logical zeros when the device does not receive a DME page with good CRC16	M	Yes [ ]
DT6	Echoed Nonce Field good	98.2.1.2.2	Contain the value received in the Transmitted Nonce Field from the link partner when the device has received a DME page with good CRC16	M	Yes [ ]
DT7	Generate a new Transmitted Nonce Field value for each entry to the Ability Detect state	98.2.1.2.3		M	Yes [ ]
DT8	Matching T[4:0]	98.2.1.2.3	Invert T[0] bit and regenerate a new random value for T[3:1]	M	Yes [ ]
DT9	Support the data service ability for a technology it advertises	98.2.1.2.4		M	Yes [ ]
DT10	Acknowledge bit with no Next Page	98.2.1.2.8	Set to 1 after the reception of at least one DME page with correct CRC	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DT11	Acknowledge bit with Next Page	98.2.1.2.8	Set to 1 after the device successfully receives reception of at least one DME page with correct CRC and remain set until Next Page information has been loaded	M	Yes [ ]
DT12	No Next Page to send	98.2.1.2.9	Set Next Page to 0	M	Yes [ ]
DT13	Next Page to send	98.2.1.2.9	Set Next Page to 1	M	Yes [ ]
DT14	No Next Page to send and link partner Next Page is set to 1	98.2.1.2.9	Transmit Next Pages with Null message codes and the Next Page set to 0	M	Yes [ ]
DT15	Transmit Switch function	98.2.1.3	Enable the transmit path from a single technology-dependent PHY to the MDI once Auto-Negotiation has completed	M	Yes [ ]
DT16	Transmit Switch function during Auto-Negotiation	98.2.1.3	Connect only the DME page generator controlled by the Transmit state diagram to the MDI	M	Yes [ ]
DT17	Signal at the MDI	98.2.1.3	Conform to all the PHY's specifications when a PHY is connected to the MDI through the Transmit Switch function	M	Yes [ ]

98.6.7 Arbitration function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
AF1	Regeneration request	98.2.4.1	Cause Arbitration function to disable all technology-dependent PHYs and halt any transmit data and link transition activity until the break_link_timer expires	M	Yes [ ]
AF2	break_link_timer expires	98.2.4.1	Resume Auto-Negotiation	M	Yes [ ]
AF3	Priority Resolution function	98.2.4.2	Highest priority is assigned to the single PHY enabled to connect to the MDI by Auto-Negotiation	M	Yes [ ]
AF4	Receipt of a Technology Ability Field with a bit that is reserved	98.2.4.2	Ignore the bit for priority resolution	M	Yes [ ]
AF5	No common technology	98.2.4.2	Value "NULL" is assigned to HCD	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
AF6	Next Pages message encodings	98.2.4.3	Have a Message code that defines how the Unformatted code will be interpreted for each series of Next Pages	M	Yes [ ]
AF7	Completed transmission of Next Page information	98.2.4.3	Transmit Next Pages with Null message codes and the NP bit set to 0	M	Yes [ ]
AF8	Receipt of Message Pages with Null message codes	98.2.4.3	End of its link partner's Next Page information	M	Yes [ ]
AF9	Next Page encoding	98.2.4.3.1	Shown in Table 98–5 and Table 98–6	M	Yes [ ]
AF10	NP, Ack, MP, Ack2 and T bits	98.2.4.3.1	Function as specified in 98.2.1.2.9, 98.2.1.2.8, 28.2.3.4.5, 28.2.3.4.6, and 28.2.3.4.7, respectively	M	Yes [ ]
AF11	Message Next Pages	98.2.4.3.1	MP bit set to 1, D[10:0] encoded as a Message Code Field, and D[47:16] encoded as Unformatted Code Field	M	Yes [ ]
AF12	Unformatted Next Pages	98.2.4.3.1	MP bit set to 0, D[10:0] and D[47:16] encoded as the Unformatted Code Field	M	Yes [ ]
AF13	Next Page exchange	98.2.4.3.1	Continue until neither device on a link has more pages to transmit	M	Yes [ ]
AF14	Next Page with Null Message Code Field value	98.2.4.3.1	Sent if the device has no other information to transmit	M	Yes [ ]

98.6.8 Service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
TDI1	link_status parameter	98.4.1.1	OK, FAIL	MDIO:M	Yes [ ]
TDI2	Receipt of link_status primitive	98.4.1.3	Comply with Figure 98–7	M	Yes [ ]
TDI3	link_control parameter	98.4.2.1	DISABLE, ENABLE	M	Yes [ ]
TDI4	link_control=DISABLE	98.4.2.1	Used by Auto-Negotiation to disable PMA processing	M	Yes [ ]
TDI5	link_control=ENABLE	98.4.2.1	Used by Auto-Negotiation to turn control over to a single PMA for all normal processing functions	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TDI6	Generation of link_control primitive	98.4.2.2	Generated by Auto-Negotiation function	M	Yes [ ]
TDI7	Auto-Negotiation enabled upon power-on or reset	98.4.2.2	Issue PMA_LINK.request(DISABLE) message to all technology-dependent PMAs	M	Yes [ ]

98.6.9 State diagram and variable definitions

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Auto-Negotiation	98.5.5	Implement Figure 98–7, Figure 98–8, and Figure 98–9	M	Yes [ ]
SD2	State diagrams	98.5.5	State diagrams take precedence when ambiguity exists between state requirements and the state diagram	M	Yes [ ]
SD3	backoff_timer_[HSM]	98.5.2	Expire according to the formula described in 98.5.2	HSM:M	Yes [ ] N/A [ ]
SD4	backoff_timer_[LSM]	98.5.2	Expire according to the formula described in 98.5.2	LSM:M	Yes [ ] N/A [ ]
SD5	blind_timer_[HSM]	98.5.2	Expire 2000 ns to 2120 ns after being started	HSM:M	Yes [ ] N/A [ ]
SD6	blind_timer_[LSM]	98.5.2	Expire 28 200 ns to 31 400 ns after being started	LSM:M	Yes [ ] N/A [ ]
SD7	break_link_timer_[HSM]	98.5.2	Expire 300 µs to 305 µs after being started	HSM:M	Yes [ ] N/A [ ]
SD8	break_link_timer_[LSM]	98.5.2	Expires 8000 µs to 8133 µs after being started	LSM:M	Yes [ ] N/A [ ]
SD9	clock_detect_max_timer_[HSM]	98.5.2	Expire 63 ns to 75 ns after being started or restarted	HSM:M	Yes [ ] N/A [ ]
SD10	clock_detect_max_timer_[LSM]	98.5.2	Expires 1680 ns to 2000 ns after being started or restarted	LSM:M	Yes [ ] N/A [ ]
SD11	clock_detect_min_timer_[HSM]	98.5.2	Expire 45 ns to 57 ns after being started or restarted	HSM:M	Yes [ ] N/A [ ]
SD12	clock_detect_min_timer_[LSM]	98.5.2	Expires 1200 ns to 1520 ns after being started or restarted	LSM:M	Yes [ ] N/A [ ]
SD13	data_detect_max_timer_[HSM]	98.5.2	Expire 33 ns to 45 ns from the last clock transition	HSM:M	Yes [ ] N/A [ ]
SD14	data_detect_max_timer_[LSM]	98.5.2	Expires 880 ns to 1200 ns from the last clock transition	LSM:M	Yes [ ] N/A [ ]
SD15	data_detect_min_timer_[HSM]	98.5.2	Expire 15 ns to 27 ns from the last clock transition	HSM:M	Yes [ ] N/A [ ]
SD16	data_detect_min_timer_[LSM]	98.5.2	Expires 400 ns to 720 ns from the last clock transition	LSM:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
SD17	interval_timer_[HSM]	98.5.2	Expire 30 ns ± 0.01% from each clock pulse and data bit	HSM:M	Yes [ ] N/A [ ]
SD18	interval_timer_[LSM]	98.5.2	Expires 800 ns ± 0.005% from each clock pulse and data bit	LSM:M	Yes [ ] N/A [ ]
SD19	link_fail_inhibit_timer_[HCD]	98.5.2	Expire 97 ms to 98 ms after entering the AN GOOD CHECK state	!10T1L:M	Yes [ ] N/A [ ]
SD20	link_fail_inhibit_timer_[HCD] for 10BASE-T1L PHY	98.5.2	Expires 3030 ms to 3090 ms after entering the AN LINK GOOD CHECK state	10T1L:M	Yes [ ] N/A [ ]
SD21	link_fail_inhibit_timer_[HCD] for 10BASE-T1S PHY	98.5.2	Expires 400 ms to 405 ms after entering the AN LINK GOOD CHECK state	10T1S:M	Yes [ ] N/A [ ]
SD22	page_test_max_timer_[HSM]	98.5.2	Expire 4800 ns to 4920 ns after being started or restarted	HSM:M	Yes [ ] N/A [ ]
SD23	page_test_max_timer_[LSM]	98.5.2	Expires 128 000 ns to 131 200 ns after being started or restarted	LSM:M	Yes [ ] N/A [ ]
SD24	receive_DME_timer_[HSM]	98.5.2	Expire 6805 ns to 6925 ns after being started	HSM:M	Yes [ ] N/A [ ]
SD25	receive_DME_timer_[LSM]	98.5.2	Expires 156 300 ns to 159 500 ns after being started	LSM:M	Yes [ ] N/A [ ]
SD26	rx_wait_timer_[HSM]	98.5.2	Expire 15 µs to 17 µs after being started or restarted	HSM:M	Yes [ ] N/A [ ]
SD27	rx_wait_timer_[LSM]	98.5.2	Expires 330 µs to 370 µs after being started or restarted	LSM:M	Yes [ ] N/A [ ]
SD28	silent_timer_[HSM]	98.5.2	Expire 2120 ns to 2240 ns after being started	HSM:M	Yes [ ] N/A [ ]
SD29	silent_timer_[LSM]	98.5.2	Expires 31 400 ns to 34 600 ns after being started	LSM:M	Yes [ ] N/A [ ]

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98.6.10 High-speed and low-speed Auto-Negotiation modes

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Supports two Auto-Negotiation speeds	98.5.6	Implements the state diagram in Figure 98–11	ANSM: M	Yes [ ] N/A [ ]
SM2	Supports only high-speed mode	98.5.6	Implements Figure 98–7, Figure 98–8, Figure 98–9, and Figure 98–10 using the timer values for high-speed mode	!LSM:M	Yes [ ] N/A [ ]
SM3	Supports only low-speed mode	98.5.6	Implements Figure 98–7, Figure 98–8, Figure 98–9, and Figure 98–10 using the timer values for low-speed mode	!HSM:M	Yes [ ] N/A [ ]

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99. MAC Merge sublayer

99.1 Introduction

This clause specifies an optional MAC Merge sublayer for use with a pair of full-duplex MACs and a single PHY operating at 100 Mb/s or higher on a point-to-point link. The two MACs are as follows:

— A preemptable MAC (pMAC), which carries the preemptable traffic, and

— An express MAC (eMAC), which carries the express traffic.

The MAC Merge sublayer supports interspersing express traffic with preemptable traffic. This is achieved by using a MAC Merge sublayer to attach an express Media Access Control (MAC) and a preemptable MAC to a single Reconciliation Sublayer (RS) service. The MAC Merge sublayer supports two ways to hold transmission of preemptable traffic in the presence of express traffic:

— The MAC Merge sublayer may preempt (interrupt) preemptable traffic being currently transmitted, and

— The MAC Merge sublayer may prevent starting the transmission of preemptable traffic.

This clause also specifies a MAC Merge Service Interface (MMSI) providing a primitive that causes the transmission of preemptable traffic to be held or released, minimizing the latency for express traffic. For example, when the MAC Client supports scheduled traffic as defined in IEEE Std 802.1Q, transmission of preemptable packets can be held before express traffic is scheduled to be transmitted.

When the preemption capability is active, the MAC Merge sublayer allows frames provided over the express MAC service interface (express traffic) or the MMSI service primitive to interrupt transmission of a frame provided over the preemptable MAC service interface.

When the preemption capability is inactive, the MAC Merge sublayer does not allow express traffic or the MMSI service primitive to interrupt transmission of a frame provided over the preemptable MAC service interface.

Regardless of whether the preemption capability is active, the MAC Merge sublayer allows express traffic or the MMSI service primitive to prevent the start of transmission of frames provided over the preemptable MAC service interface (preemptable traffic).

The preemption capability is most useful at lower operating speeds. For example, the duration of a 2000 octet packet on a 100 Mb/s link is 160 µs and on a 1 Gb/s link is 16 µs. The time to transmit a maximum length packet is an upper bound on the additional delay before a MAC Client can send an Express frame when the preemption capability is not used. At higher operating speeds this additional delay gets smaller in proportion to the speed, reducing the advantage of the preemption mechanism.

Figure 99–1 shows the relationship of MAC Merge sublayer to the other sublayers and the ISO/IEC Open Systems Interconnection (OSI) reference model. The MAC Merge sublayer has two clients that are MAC sublayer instances: the eMAC and the pMAC.

Figure 99–2 shows the service interfaces of the MAC Merge sublayer and its associated MACs and Reconciliation Sublayer.

When attached to an eMAC or a pMAC, the MAC Control Sublayer shall not generate PAUSE (see Annex 31B).

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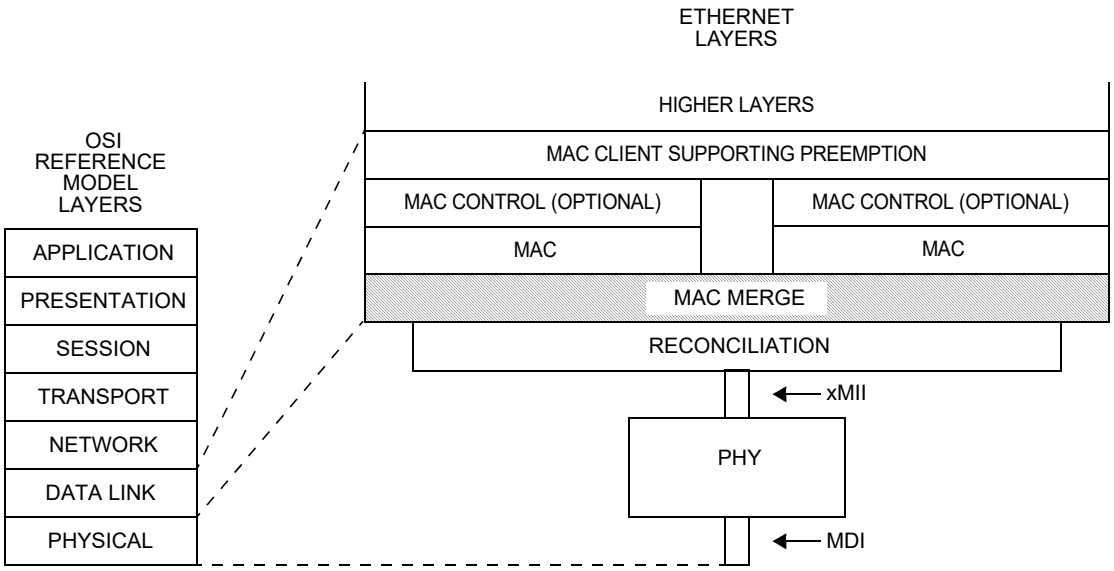

NOTE—In this figure, the xMII is used as a generic term for the Media Independent Interfaces for implementations of 10BASE-T1L, 10BASE-T1S, and 100 Mb/s and above. For example: for 100 Mb/s implementations this interface is called MII; for 1 Gb/s implementations, it is called GMII; for 10 Gb/s implementations, it is called XGMII; etc.

MAC = MEDIA ACCESS CONTROL
xMII = MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
PHY = PHYSICAL LAYER DEVICE

Figure 99–1—Relationship of MAC Merge sublayer to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

Devices that implement the MAC Merge sublayer interoperate with devices that do not implement the MAC Merge sublayer. The preemption capability is enabled only after it has been determined that the link partner supports it (see 99.4.2).

99.1.1 Relationship to other IEEE standards

MAC Merge sublayer and its MACs provide support for Frame Preemption as defined in IEEE Std 802.1Q.

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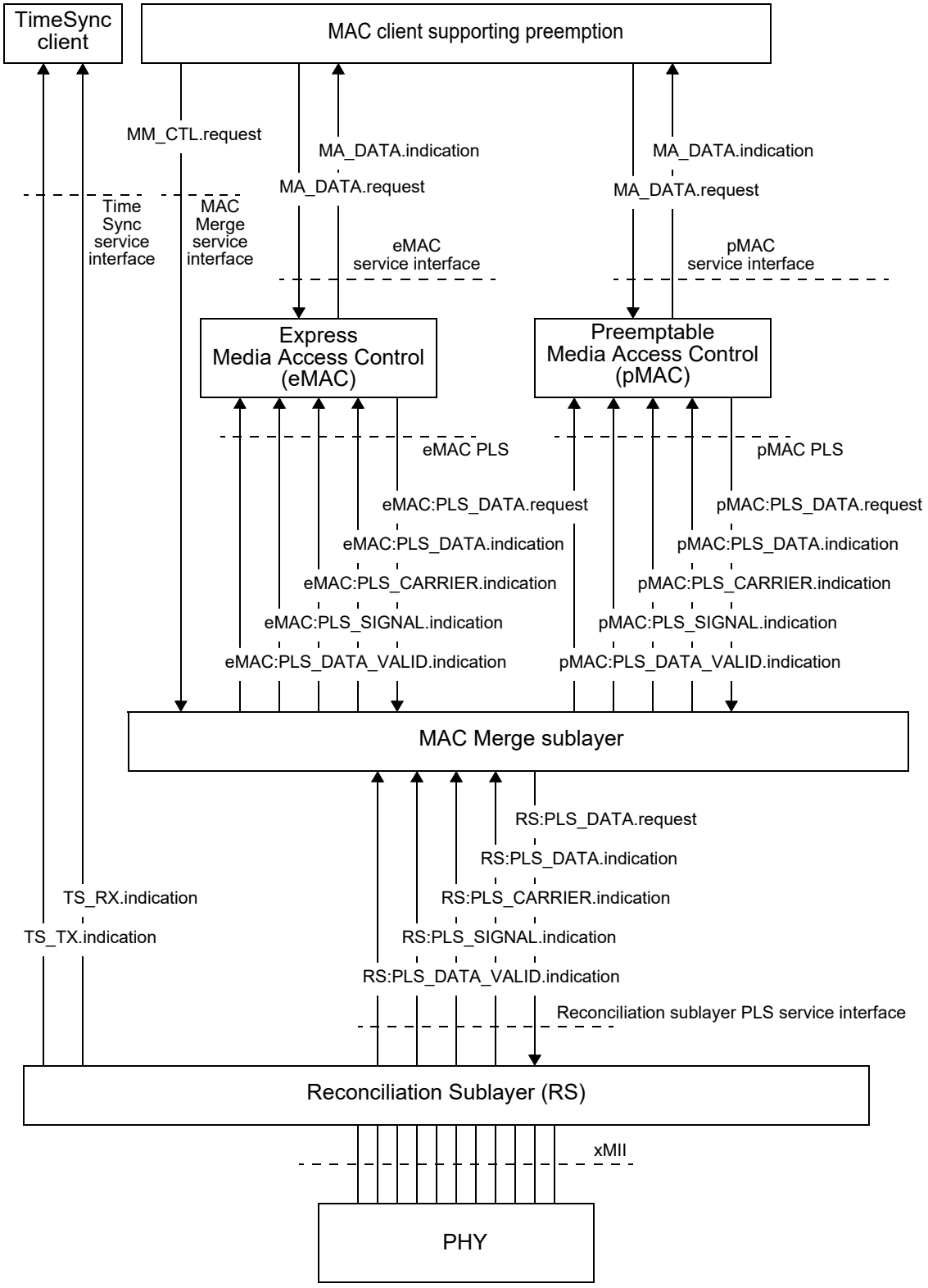

Figure 99–2—MAC Merge sublayer service interfaces diagram

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99.1.2 Functional Block Diagram

Figure 99–3 provides a functional block diagram of the MAC Merge sublayer.

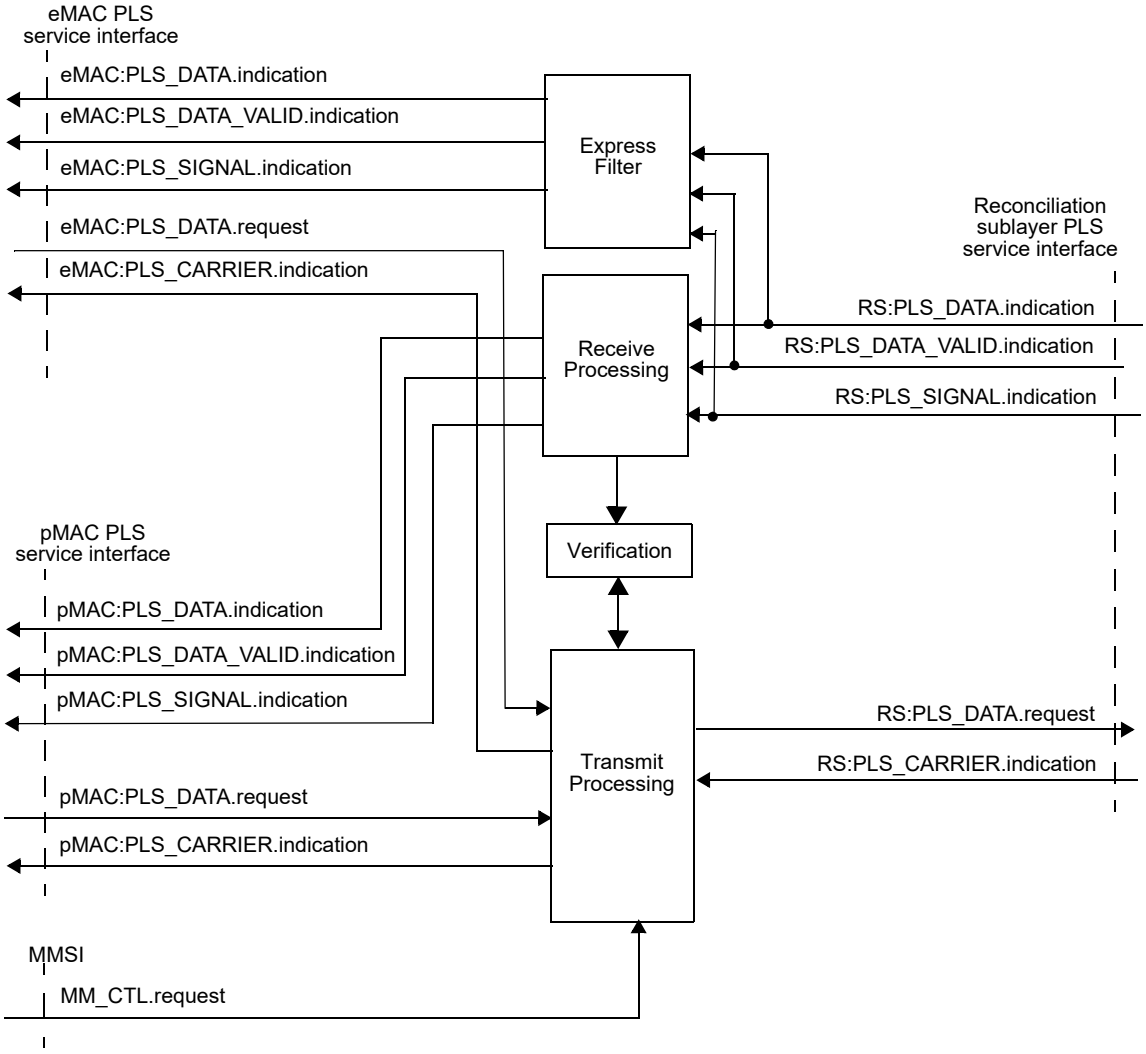

Figure 99–3—MAC Merge sublayer Functional Block Diagram

99.2 MAC Merge Service Interface (MMSI)

This subclause specifies the services provided by the MAC Merge sublayer to a MAC Client. The service interface is described in an abstract manner and does not imply any particular implementation. The model used in this service specification is identical to that used in 1.2.2.

The following primitive is defined:

— MM_CTL.request

99.2.1 MM_CTL.request

This primitive defines a request from a MAC Client to MAC Merge sublayer to hold or release transmission of preemptable traffic.

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99.2.1.1 Semantics

The semantics of the primitive are as follows:

MM_CTL.request (hold_req)

The hold_req parameter takes one of two values, HOLD or RELEASE. The value of HOLD causes the MAC Merge sublayer to hold transmission of preemptable traffic. The value of RELEASE causes the MAC Merge sublayer to release transmission of preemptable traffic.

99.2.1.2 When generated

The generation of this primitive is out of scope of this standard.

99.2.1.3 Effect of receipt

Receipt of the primitive with the hold_req parameter set to the value HOLD causes preemption when the conditions allow preemption and prevents starting transmission of pMAC packets until this primitive is received with the value RELEASE.

Receipt of the primitive with the hold_req parameter set to the value RELEASE allows MAC Merge sublayer to transmit packets from the pMAC when the eMAC does not have a packet to transmit.

99.3 MAC Merge Packet (mPacket)

When the preemption capability is active, MAC Merge sublayer sends mPackets to the Reconciliation sublayer (RS). An mPacket contains one of the following:

— a complete express packet,
— a complete preemptable packet
— an initial fragment of a preemptable packet, or
— a continuation fragment of a preemptable packet.

99.3.1 mPacket format

Part (a) of Figure 99–4 shows the format of an mPacket containing an express packet, a complete preemptable packet, or the initial fragment of a preemptable packet. Part (b) of Figure 99–4 shows the format of an mPacket containing a continuation fragment of a packet.

The mPacket format is indicated by the value of the SMD (see 99.3.3).

99.3.2 Preamble

The preamble in the mPacket shown in part (a) of Figure 99–4 contains seven octets. The preamble in the mPacket shown in part (b) of Figure 99–4 contains six octets. Each octet contains the value of 0x55 (transmitted in order from left to right 10101010).

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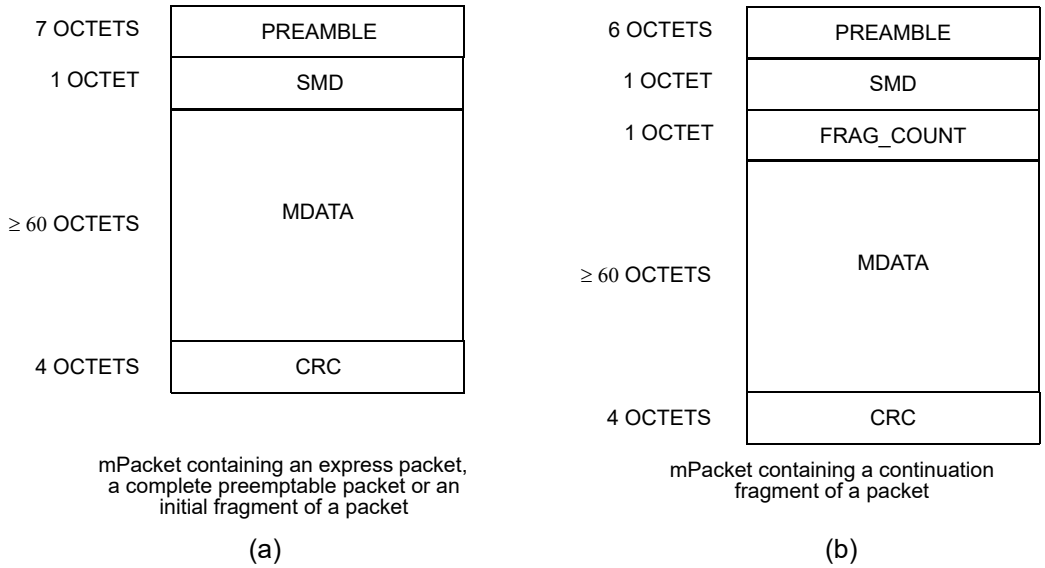

Figure 99–4—mPacket format

99.3.3 Start mPacket Delimiter (SMD)

The value of the SMD indicates whether the mPacket contains an express packet, the start of a preemptable packet (initial fragment or complete packet), or any of continuation fragments of a preemptable packet. All valid SMD values are defined in Table 99–1.

An mPacket carrying an express packet (transmitted by eMAC) has the same format as the express packet, because SMD-E (i.e., SMD value for an express packet) is same as the SFD value. An mPacket carrying a complete (non-fragmented) preemptable packet or the initial fragment of a preempted preemptable packet (transmitted by pMAC) has the SFD octet replaced with the appropriate SMD value. An mPacket carrying any of the continuation fragments of a preempted preemptable packet (transmitted by pMAC) has a continuation fragment SMD value, and includes an additional fragment counter octet (frag_count) following the SMD.

The SMD in an mPacket carrying a complete (non-fragmented) preemptable packet or any of the fragments of a preemptable packet also indicates the frame count. Information about the frame count prevents reassembling an invalid packet if the final mPacket of one preemptable packet and the initial fragment of the next preemptable packet are lost. The frame count is a modulo-4 count.

The term “SMD-S” refers to any of the four SMD values (SMD-S0, SMD-S1, SMD-S2, and SMD-S3) in an mPacket carrying the start of a preemptable packet. The term “SMD-C” refers to any of the four SMD values (SMD-C0, SMD-C1, SMD-C2, and SMD-C3) in an mPacket carrying a continuation fragment of a preemptable packet.

Two additional SMD values, SMD-V and SMD-R, identify mPackets used to verify that a link can support the preemption capability.

99.3.4 frag_count

The frag_count is a modulo-4 counter that increments for each continuation fragment of the preemptable packet. The frag_count protects against mPacket reassembly errors by enabling detection of the loss of up to 3 packet fragments.

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Table 99–1—SMD values

mPacket type	Notation	Frame count	Value
verify packet	SMD-V	—	0x07
respond packet	SMD-R	—	0x19
express packet	SMD-E	—	0xD5
preemptable packet start	SMD-S0	0	0xE6
	SMD-S1	1	0x4C
	SMD-S2	2	0x7F
	SMD-S3	3	0xB3
continuation fragment	SMD-C0	0	0x61
	SMD-C1	1	0x52
	SMD-C2	2	0x9E
	SMD-C3	3	0x2A

The frag_count field is present only in mPackets with SMD-C. The frag_count is zero in the first continuation fragment of each preemptable packet.

The valid frag_count values are shown in Table 99–2.

Table 99–2—Frag_count values

Frag_count	Value
0	0xE6
1	0x4C
2	0x7F
3	0xB3

99.3.5 mData

The contents of the frame from the MAC from the first octet after the SFD to the last octet before the FCS are sent in the mData fields of the one or more mPackets for that frame. The minimum size of the mData field is 60 octets.

NOTE—The Transmit Processing state diagram ensures that the minimum mData field size is met. There is no pad field.

99.3.6 CRC

The CRC field contains a cyclic redundancy check (CRC) and an indication of whether this is the final mPacket of a frame.

In the final mPacket of a frame, the CRC field contains the last 4 octets of the MAC frame (the FCS field).

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For other mPackets, the CRC field contains an mCRC value. This includes mPackets used to verify that a link can support the preemption capability. The mCRC shall be calculated on the octets of the frame from the first octet of the frame (i.e., the octet following the SFD sent by the pMAC) to the last octet of the frame transmitted in that mPacket by:

— performing steps a) through d) in 3.2.9, and then
— XORing the calculated 32 bits with 0x0000FFFF.

NOTE—0x0000 is XORed with two octets that contain the higher order coefficients of the CRC, and 0xFFFF is XORed with the two octets that contain the lower order coefficients of the CRC.

99.4 MAC Merge sublayer operation

The MAC Merge sublayer receiver always operates the same way regardless of whether preemption is active. This allows MAC Merge sublayers to enable and use preemption once the link partner has indicated support for it, without sychronizing the transition between the two ends of the link.

The express mPacket format is the same as the MAC packet format. As a result, any packet received from a device that does not implement the MAC Merge sublayer or that has preemption disabled is received through the eMAC.

99.4.1 MAC Merge sublayer transmit behavior when preemption is disabled

When preemption is disabled, the packets presented by the pMAC and eMAC pass through the MAC Merge sublayer without alteration, i.e., the MAC Merge sublayer transmits packets rather than mPackets. If both the eMAC and pMAC have packets ready to transmit and no packet is being transmitted, the eMAC packet is transmitted. If a pMAC packet is being transmitted and the eMAC has a packet to transmit, the packet from the eMAC is transmitted after transmission of the pMAC packet completes.

99.4.2 Determining that the link partner supports preemption

The preemption capability is enabled in the transmit direction only if it is determined that the link partner supports the preemption capability.

The process of discovering the support for the preemption capability on the link partner relies on the exchange of the Additional Ethernet Capabilities TLV (see 79.3.7).

The preemption capability shall be enabled only if the link partner announces its support for the preemption capability via an Additional Ethernet Capabilities TLV in an LLDPDU addressed to the Nearest Bridge group address (see IEEE Std 802.1Q). The preemption capability shall be disabled if the MAC Merge sublayer receives indication of link failure.

NOTE—Indication of link failure to the MAC Merge sublayer is implementation dependent.

99.4.3 Verifying preemption operation

Verification (see Figure 99–3) checks that the link can support the preemption capability.

If verification is enabled, the preemption capability shall be active only after verification has completed successfully.

If the preemption capability is enabled but has not been verified yet, the MAC Merge sublayer initiates verification. Verification relies on the transmission of a verify mPacket and receipt of a respond mPacket to confirm that the remote station supports the preemption capability. The format of a verify mPacket and a

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respond mPacket is as shown in part (a) of Figure 99–4, with the SMD values defined in Table 99–1 and an mData field containing 60 octets of 0x00.

When an mPacket with an SMD-V and a correct mCRC is received, a respond mPacket is sent. A respond mPacket has 7 octets of preamble (0x55), an SMD-R, 60 octets of 0x00, and an mCRC.

When an mPacket with an SMD-R and a correct mCRC is received, the preemption capability is verified.

Verification may be disabled. Verification disable is intended for engineered closed networks (i.e., where it is ensured by design that links can support preemption capability).

If verification is enabled, it shall be performed as specified in part (a) of Figure 99–8.

Respond shall be performed as in part (b) of Figure 99–8.

99.4.4 Transmit processing

Transmit processing (see Figure 99–3) receives packets from the eMAC and pMAC. Transmit processing preempts a preemptable packet when a MM_CTL.request primitive is received with a hold_req parameter value of HOLD or the eMAC has a packet to transmit if that can be done while meeting minimum mPacket mData field size. Therefore, preemption occurs only if at least 60 octets of the preemptable frame have been transmitted and at least 64 octets (including the frame CRC) remain to be transmitted.

The earliest starting position of preemption is controlled by the addFragSize variable. Preemption does not occur until at least 64 × (1+ addFragSize) – 4 octets of the preemptable frame have been sent. The addFragSize variable is set to the value of the addFragSize field in the received Additional Ethernet Capabilities TLV (see 79.3.7).

Transmit processing includes a CRC generator to calculate an mCRC as specified in 99.3.6.

When the preemption capability is active, transmit processing replaces the SFD of a pMAC packet with an SMD-S value. A 2-bit rolling frame count is encoded in the SMD-S value. The SMD-E value is the same as the SFD value so the SFD of an eMAC packet does not need to be replaced.

When a packet is preempted, transmit processing appends the mCRC to the non-final mPackets. For the final mPacket of a preempted frame, the CRC field contains the CRC of the preempted MAC frame (the FCS field).

Transmit processing resumes transmission of the remainder of a preempted packet by sending preamble followed by an SMD-C and frag_count before continuing transmission of the packet. The SMD-C encodes the same frame count value as the SMD-S of the initial fragment.

Transmit processing shall be performed as specified in Figure 99–5.

If a PLS_CARRIER.indication is received from the PLS, PLS_CARRIER.indications with the same CARRIER_STATUS shall be sent to the pMAC and the eMAC.

99.4.5 Receive processing

Receive processing (see Figure 99–3) checks the SMD of each received mPacket. If an mPacket contains an SMD-E, Receive processing ignores the mPacket.

An SMD containing an SMD-S indicates the initial mPacket of a preemptable packet.

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If an mPacket containing an SMD-S is received when Receive processing has not completed receiving the previous preempted packet, Receive processing shall ensure that the MAC detects a FrameCheckError in the partially received frame. This requirement may be met by producing a received frame data sequence delivered to the MAC sublayer that is guaranteed to not yield a valid CRC result, as specified by the frame check sequence algorithm (see 3.2.8). This data sequence may be produced by substituting data delivered to the MAC. It can do this by checking that the prior four octets sent to the MAC did not match the CRC of the data sent before them or by sending eight additional PLS_DATA.indication primitives to the pMAC or by implementation dependent means. Other techniques may be employed to respond to an incomplete packet provided that the result is that the MAC sublayer behaves as though a FrameCheckError occurred in the received frame.

When an SMD-S is detected, receive processing records the frame count indicated by the SMD. Receive processing sends an SFD to the pMAC in place of the SMD and then begins sending PLS_DATA.indication primitives to the pMAC.

Receive processing checks whether the last four octets of the mPacket match the mCRC. If the last four octets of the mPacket do not match, that indicates the end of the packet. The PLS_DATA.indications for the last four octets are sent to the pMAC followed by PLS_DATA_VALID.indication(DATA_NOT_VALID). If the last for octets of the mPacket match, that indicates that the packet was preempted and the PLS_DATA.indications for the last four octets are not sent to the pMAC. No further primitives are sent to the pMAC until the next mPacket of the packet is received.

An SMD containing an SMD-C indicates an mPacket that continues the data for a preempted packet.

Upon receiving an SMD value of SMD-C, Receive processing checks that:

a) There is a preempted packet in progress,
b) The frame count indicated by the SMD matches the frame count of the packet in progress, and
c) The frag_count value indicates the next fragment count.

If any of the checks fail, the mPacket is discarded and Receive processing ensures that the pMAC detects a FrameCheckError as previously described. Then PLS_DATA_VALID.indication(DATA_NOT_VALID) is sent to the pMAC.

If all the checks pass, the next fragment count is incremented modulo 4 and the PLS_DATA.indications after the frag_count field are sent to the pMAC.

Receive processing handles the last four octets of the mPacket as previously described.

Receive processing shall be performed as specified in Figure 99–6.

PLS_SIGNAL.indication is never produced by Receive processing since it does not apply to full duplex PHYs.

99.4.6 Express filter

The Express filter (see Figure 99–3) checks the SMD of each received mPacket. If an mPacket contains an SMD-E, the Express filter passes the RS PLS_DATA.indication to the eMAC. If the SMD contains any other value, Express filter ignores the mPacket.

Express processing shall be performed as specified in Figure 99–7.

PLS_SIGNAL.indication is never produced by Express filter since it does not apply to full duplex PHYs.

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99.4.7 Detailed functions and state diagrams

99.4.7.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

PLS service interface primitives are prefixed by a letter to designate the PLS service interface as follows:

— e PLS service interface between the eMAC and MAC Merge sublayer
— p PLS service interface between the pMAC and MAC Merge sublayer
— r PLS service interface between MAC Merge sublayer and RS

For example, ePLS_DATA.request is a PLS_DATA.request primitive from the eMAC.

99.4.7.2 Constants

minFrag
: the integer 64, the number of octets required for a minimum size fragment.

PREAMBLE
: 0x55

SFD
: 0xD5

verifyLimit
: the integer 3, the number of verification attempts

99.4.7.3 Variables

addFragSize
: An integer in the range 0:3 that controls the minimum non-final mPacket length, as specified in 99.4.4. Set to the value of the addFragSize field in the received Additional Ethernet Capabilities TLV (see 79.3.7).

begin
: Boolean variable that is set TRUE by implementation dependent means to initialize the state machines.

cFrameCnt
: An integer in the range 0:3 set by the SMD_DECODE function invoked on the SMD-C of a continuation packet that indicates the frame count of the continuation mPacket.

disableVerify
: Boolean variable that is set by management to control verification of preemption operation (see 99.4.3). TRUE disables verification and FALSE enables verification.

eTx
: Boolean variable that is TRUE when an ePLS_DATA.request has been received and a corresponding rPLS_DATA.request has not yet been generated. FALSE otherwise.

eTxCplt
: Boolean variable that is set TRUE when ePLS_DATA.request with the value DATA_COMPLETE is received and set FALSE when the end of frame has been processed.

keepSafterD
: Boolean variable that indicates whether an implementation is able to process the start of a

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packet while discarding an errored packet. When an SMD-S is received while Receive processing is waiting for the next mPacket of a preempted packet, the preempted packet is discarded. The value TRUE indicates that an implementation is able to process the new packet when this occurs.

hold

Boolean variable that is set TRUE when MM_CTL.request is received with a hold_req parameter value of HOLD and FALSE when MM_CTL.request is received with a hold_req parameter value of RELEASE.

link_fail

Boolean variable that is TRUE when the MAC Merge sublayer receives indication of link failure. FALSE otherwise.

NOTE—Indication of link failure to the MAC Merge sublayer is implementation dependent.

rRxDv

Boolean variable that is set TRUE when rPLS_DATA_VALID.indication is received with the value DATA_VALID and set FALSE when rPLS_DATA_VALID.indication is received with the value DATA_NOT_VALID.

pActive

Boolean variable that is TRUE when the preemption capability is active and FALSE otherwise. The value of pActive is pEnable ∗ (verified + disableVerify).

pAllow

Boolean variable that is set to the value of pActive when SEND_SMD_S state is entered.

pEnable

Boolean variable that is set TRUE to enable the preemption capability and set FALSE to disable the preemption capability.

preempt

Boolean that is TRUE when a preemptable packet is to be preempted. The value of preempt is: pAllow ∗ (eTx + hold) ∗ preemptableFragSize ∗ MIN_REMAIN.

preemptableFragSize

Boolean variable that is TRUE when a enough bits of the current preemptable packet have been transmitted to allow it to be preempted. The value of preemptableFragSize is: fragSize ≥ (minFrag × (1 + addFragSize) – 4).

pTX

Boolean variable that is TRUE when a pPLS_DATA.request has been received and a corresponding rPLS_DATA.request has not yet been generated. FALSE otherwise.

pTxCplt

Boolean variable that is set TRUE when pPLS_DATA.request with the value DATA_COMPLETE is received and set FALSE when the end of packet has been processed.

rcv_r

Boolean that is set TRUE when an mPacket with SMD-R and a correct mCRC is received and set FALSE when the INIT_VERIFICATION state of the VERIFY state diagram is entered.

rcv_v

Boolean that is set TRUE when an mPacket with SMD-V and a correct mCRC is received and set FALSE when the INIT_VERIFICATION state of the VERIFY state diagram or the SEND_RESPOND state of the Respond state diagram is entered.

resumeTx

Boolean variable that is TRUE if a preemptable packet is waiting to resume transmission.

rxFragCnt

An integer in the range 0:4 set by the FRAG_DECODE function invoked on the frag_count of a continuation packet that indicates the fragment count of the continuation mPacket.

rxFrameCnt

An integer in the range 0:3 set by the SMD_DECODE function invoked on the SMD-S of a continuation packet that indicates the frame count of the initial mPacket.

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send_r
: Boolean that is set TRUE to initiate sending a respond mPacket and set FALSE when a respond mPacket is sent.

send_v
: Boolean that is set TRUE to initiate sending a verification mPacket and set FALSE when a verify mPacket is sent.

verified
: Boolean that is set TRUE when the ability of the link to support the preemption capability has been verified and FALSE when the INIT_VERIFICATION state of the VERIFY state diagram is entered.

verify_fail
: Boolean that is set TRUE when verification attempts have failed and FALSE when the INIT_VERIFICATION state of the VERIFY state diagram is entered.

verifyTime
: An integer in the range 1:128 used to configure the number of ms after which the verify_timer expires (see 99.4.7.6). The default value of verifyTime is 10.

99.4.7.4 Functions

For functions that produce primitives based on an 8-bit vector, a primitive value is ONE if the corresponding bit is 1 and ZERO if the corresponding bit is 0. The primitives are produced from bit 0 to bit 7 in sequence.

For functions that produce an 8-bit vector based on eight primitives, a bit is 1 if the corresponding primitive value is ONE and 0 if the corresponding primitive is ZERO. The primitives are mapped to bit 0 to bit 7 in sequence.

When the value of a vector is expressed as a hexadecimal number, the LSB corresponds to bit 0 and the MSB corresponds to bit 7.

DISCARD
: Ensures that the MAC detects a FrameCheckError in that frame (see 99.4.5) and then invokes pRX_DV(FALSE). Used when Receive processing detects that the packet cannot be continued after it was preempted.

eRX_DATA(data<7:0>)
: Produces eight ePLS_DATA.indication primitives based on the 8-bit vector data<7:0>.

eRX_DV(data_valid)
: Produces an ePLS_DATA_VALID.indication. If the Boolean parameter data_valid is TRUE, the primitive value is DATA_VALID. If data_valid is FALSE, the primitive value is DATA_NOT_VALID.

eTX_DATA
: Returns an 8-bit vector based on eight ePLS_DATA.request primitives.

FRAG_ENCODE(frag_cnt)
: Creates an 8-bit vector with the frag_count encoding for a fragment count of frag_cnt (see Table 99–2). Produces eight rPLS_DATA.request primitives based on the 8-bit vector.

FRAG_DECODE
: Decodes eight rPLS_DATA.indication primitives by producing an 8-bit vector and comparing it to encoded frag_count values (see Table 99–2). If frag_count contains a valid value, places the fragment count decoded in rxFragCnt. Otherwise, it sets rxFragCnt to 4.

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MIN_REMAIN

Prescient function to check if enough octets of the current pMAC packet remain meet the minimum fragment requirement after preemption. Produces a Boolean value as follows:

TRUE ≥ minFrag octets are left to transmit
FALSE Otherwise

rRX_DATA

Returns an 8-bit vector based on eight rPLS_DATA.indication primitives.

rTX_CPLT

Produces an rPLS_DATA.request primitive with the value DATA_COMPLETE.

rTX_DATA(data<7:0>)

Produces eight rPLS_DATA.request primitives based on the 8-bit vector data<7:0>.

pRX_DATA(data<7:0>)

Produces eight pPLS_DATA.indication primitives based on the 8-bit vector data<7:0>.

pRX_DV(data_valid)

Produces a pPLS_DATA_VALID.indication. If the Boolean parameter data_valid is TRUE, the primitive value is DATA_VALID. If data_valid is FALSE, the primitive value is DATA_NOT_VALID.

pTX_DATA

Returns an 8-bit vector based on eight pPLS_DATA.request primitives.

RX_MCRC_CK

Prescient function returning a Boolean value. The value is TRUE if rPLS_DATA_VALID.indication with a value of DATA_NOT_VALID will be received after the next 32 rPLS_DATA.indication primitives and the next 32 rPLS_DATA.indications equal the computed mCRC result for the preemptable packet being received. It is FALSE otherwise.

SFD_DET

Prescient function returning a Boolean value. The value is TRUE if an 8-bit vector produced from the next eight pPLS_DATA.request primitives contains an SFD.

SMD_DECODE

Decodes the value of 8 rPLS_DATA.indication primitives by producing an 8-bit vector and returning one of the following values based on the value of the vector (see Table 99–1):

Preamble 0x55
E SMD-E encoding
S SMD-S encoding
C SMD-C encoding
V SMD-V encoding
R SMD-R encoding
ERR Any other value - error.

If S is returned, the function sets rxFrameCnt equal to the frame count indicated by the SMD-S. If C is returned, the function sets cFrameCnt equal to the frame count indicated by the SMD-C.

SMDC_ENCODE(frame_cnt)

Creates an 8-bit vector with the SMD encoding for an SMD-C with frame count of frame_cnt. Produces eight rPLS_DATA.request primitives based on the 8-bit vector.

SMDS_ENCODE(frame_cnt)

Returns an 8-bit vector with the SMD encoding for an SMD-S with frame count of frame_cnt if pAllow is TRUE. Otherwise it returns a vector containing 0xD5 (i.e., SFD). Consumes 8 pPLS_DATA.request primitives containing the SFD.

TX_MCRC

Produces 32 rPLS_DATA.requests that transmit the mCRC computation for the mPacket.

TX_R

Produces 576 rPLS_DATA.requests to send a respond mPacket: 7 octets of 0x55, 1 octet SMD-R, 60 octets of 0x00, mCRC followed by an rPLS_DATA.request with the value DATA_COMPLETE.

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TX_V
: Produces 576 rPLS_DATA.requests to send a verify mPacket: 7 octets of 0x55, 1 octet SMD-V, 60 octets of 0x00, mCRC followed by an rPLS_DATA.request with the value DATA_COMPLETE.

99.4.7.5 Counters

fragSize
: a count of the number of octets of mData transmitted in the current preemptable mPacket.

nxtRxFrag
: a modulo-4 counter containing the next expected fragment count for the next incoming continuation packet.

preambleCnt
: a count of the number of preamble octets sent for a continuation fragment.

txFrag
: a modulo-4 counter containing the fragment count for the next outgoing continuation mPacket.

txFrame
: a modulo-4 counter containing the frame count for the next outgoing preemptable packet.

verifyCnt
: a count of the number of verification attempts that have completed.

99.4.7.6 Timers

ipg_timer
: A timer counting bit times since the end of the prior packet. The timer expires 96 bit times after being started.

verify_timer
: A timer of time from when a verification mPacket was sent to initiating the next attempt. The timer expires verifyTime ms ± 20% after being started.

99.4.7.7 State diagrams

The Transmit Processing state diagram is shown in Figure 99–5. The Receive Processing state diagram is shown in Figure 99–6. The Express Filter state diagram is shown in Figure 99–7. The Verify state diagram and Respond state diagram are shown in Figure 99–8.

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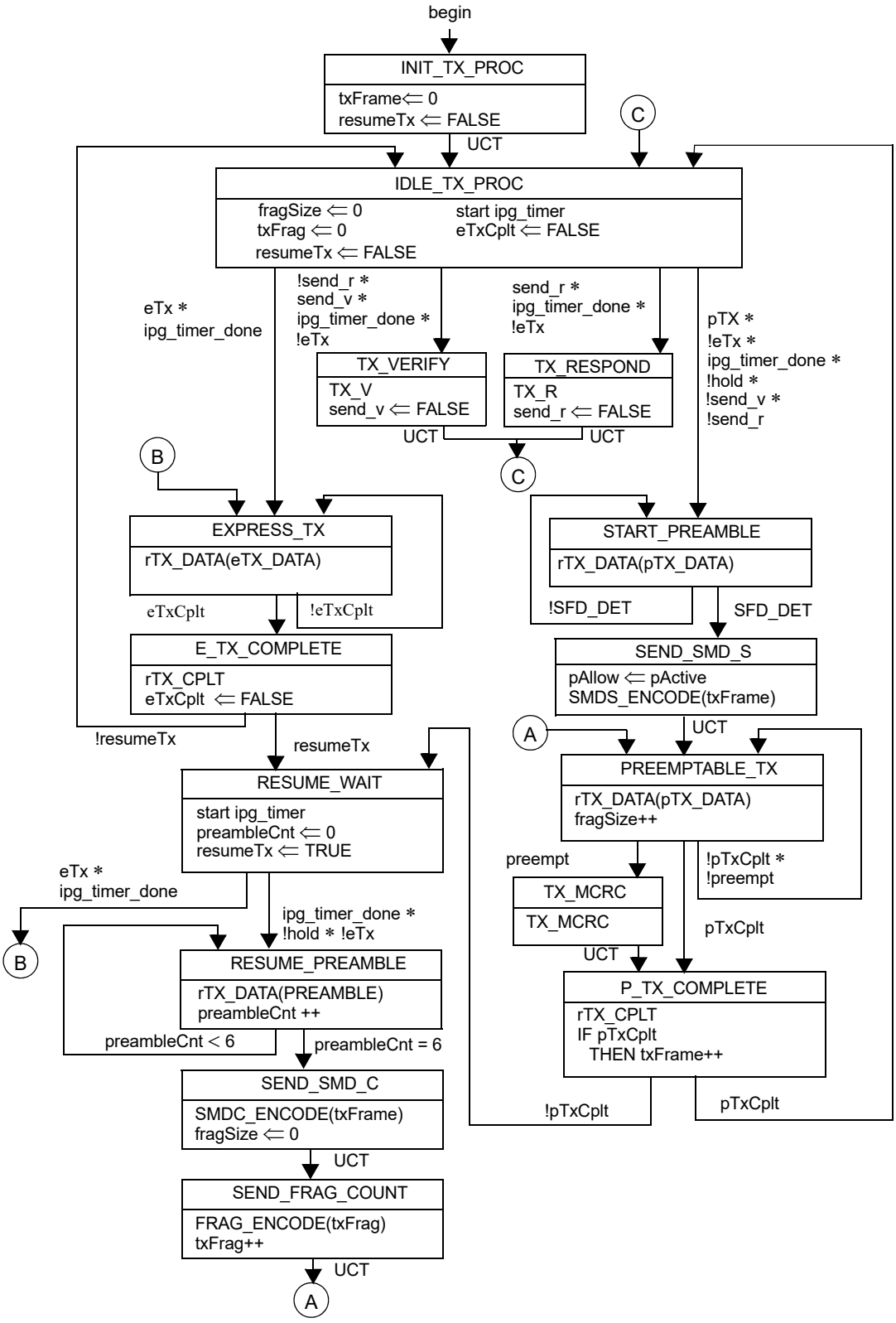

Figure 99–5—Transmit Processing state diagram

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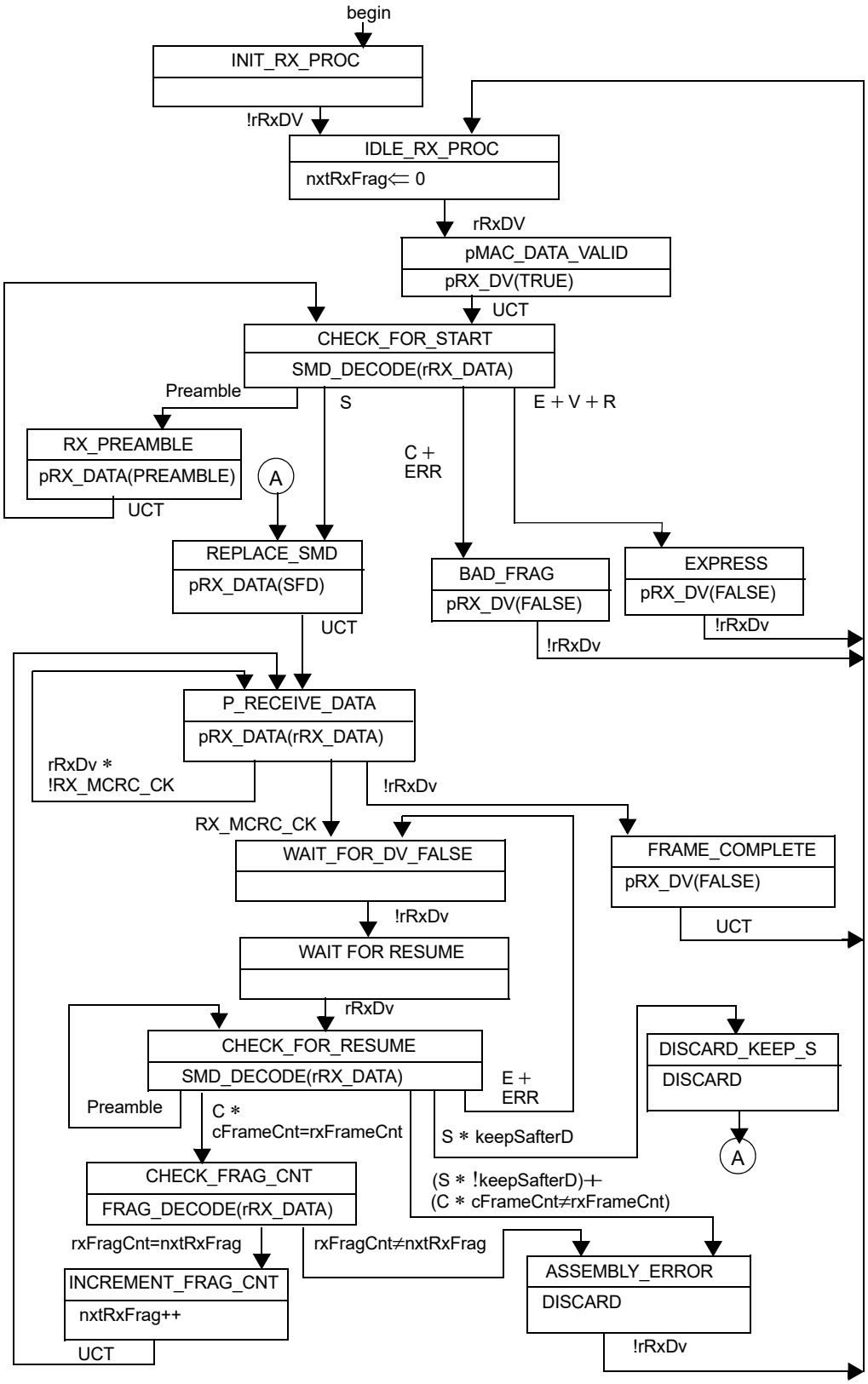

Figure 99–6—Receive Processing state diagram

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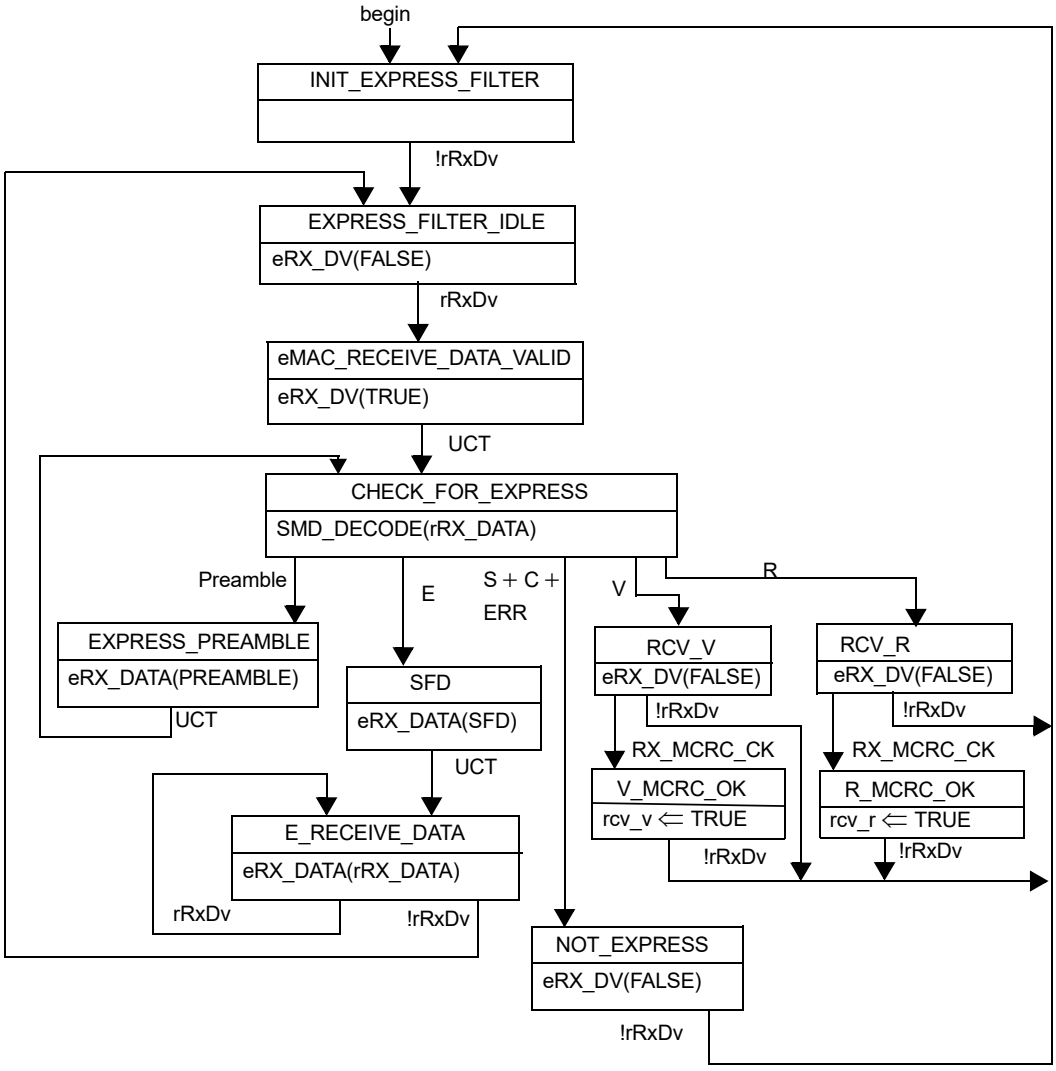

Figure 99–7—Express Filter state diagram

99.4.8 Delay Constraints

Predictable operation for time sensitive traffic (e.g., IEEE Std 802.1Q, Clause 31, Annex 31D PFC operation) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

If the preemption capability is active, transmission of preemptable traffic shall be preempted within the hold response time (HRT) after the MAC Client sends MM_CTL.request with a hold_req parameter value of HOLD. HRT is (1240 + 512 × addFragSize) bit times.

When preemptable traffic is held by an MM_CTL.request with a hold_req parameter value of HOLD sent by the MAC Client at least HRT before the MA_DATA.request, the maximum cumulative MAC Control, MAC, MAC Merge sublayer and RS delay for an express packet shall meet the delay specified for a MAC Control, MAC and RS delay based on the MAC operating speed.

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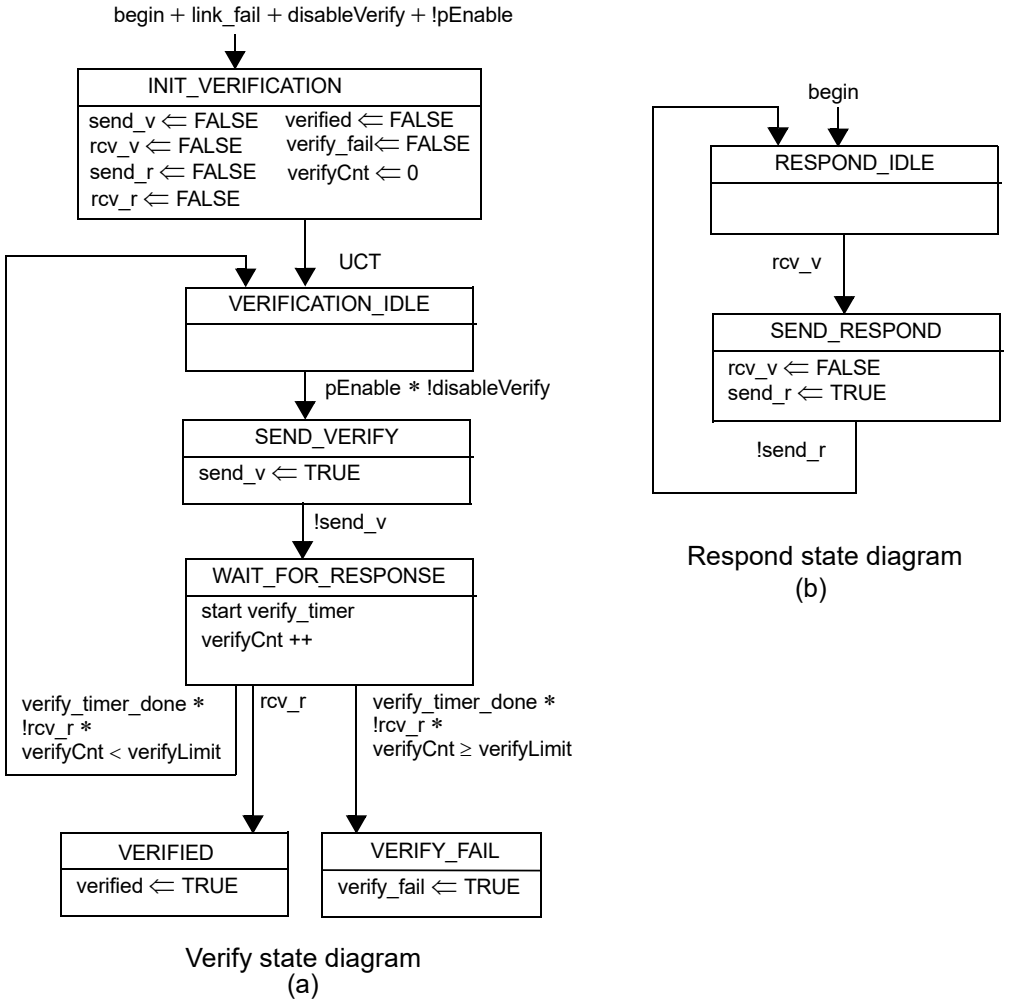

Figure 99–8—Verify state diagram (a) and Respond state diagram (b)

When preemption is active and preemptable traffic is not held by an MM_CTL.request with a hold_req parameter value of HOLD sent by the MAC Client at least HRT before the MA_DATA.request, the maximum cumulative MAC Control, MAC, MAC Merge sublayer, and RS delay for an express packet shall meet the delay specified for a MAC Control, MAC and RS delay based on the MAC operating speed delay plus HRT.

When preemptable traffic is released by an MM_CTL.request with a hold_req parameter value of RELEASE sent by the MAC Client at least 96 bit times before the MA_DATA.request and no express packets are being sent, the maximum cumulative MAC Control, MAC, MAC Merge sublayer, and RS delay for a preemptable packets shall meet the delay specified for a MAC Control, MAC and RS delay based on the MAC operating speed.

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99.5 Protocol implementation conformance statement (PICS) proforma for Clause 99, MAC Merge sublayer[172]

99.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 99, MAC Merge sublayer, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

99.5.2 Identification

99.5.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

99.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 99, MAC Merge sublayer
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[172]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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99.5.3 PICS proforma tables for MAC Merge sublayer

99.5.3.1 Functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
MM2	mCRC computation	99.3.6	Calculated as described	M	Yes [ ]
MM3	Enabling preemption capability	99.4.2	Enabled only if the link partner announces support for the preemption capability as described	M	Yes [ ]
MM5	Preemption capability disabled on link failure	99.4.2	Disabled on link failure indication	M	Yes [ ] No [ ]
MM6	Activating preemption capability	99.4.3	When verification is enabled, capability is active only after verification has completed successfully	M	Yes [ ]
MM7	Verify	99.4.3	Performed as specified in part (a) of Figure 99–8 if enabled	M	Yes [ ]
MM8	Respond	99.4.3	Performed as specified in part (b) of Figure 99–8	M	Yes [ ]
MM9	Transmit processing	99.4.4	Performed as specified in Figure 99–5	M	Yes [ ]
MM10	PLS.CARRIER.indication	99.4.4	If received, sent to the pMAC and eMAC	M	Yes [ ]
MM11	Receive processing	99.4.5	Performed as specified in Figure 99–6	M	Yes [ ]
MM12	Frame error handling	99.4.5	Ensure that the MAC detects FrameCheckError	M	Yes [ ]
MM13	Express filter	99.4.6	Performed as specified in Figure 99–7	M	Yes [ ]
MM14	No PAUSE	99.1	MAC Control sublayer does not generate PAUSE	M	Yes [ ]

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99.5.3.2 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	Time to preempt after MAC Client sends MM_CTL.request	99.4.8	No more than HRT	M	Yes [ ]
DC2	Delay to transmit express packet when preemptable traffic is held by MM_CTL.request	99.4.8	Meets the maximum cumulative MAC Control, MAC and RS delay	M	Yes [ ]
DC3	Delay to transmit express frame when preemptable traffic is not held by MM_CTL.request	99.4.8	Meets the maximum cumulative MAC Control, MAC and RS delay plus HRT	M	Yes [ ]
DC4	Delay to transmit preemptable packet when traffic is released by MM_CTL.request and no express packets are being sent.	99.4.8	Meets the maximum cumulative MAC Control, MAC and RS delay	M	Yes [ ]

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100. Physical Medium Dependent (PMD) sublayer, and medium for coaxial distribution networks, type 10GPASS-XR

100.1 Overview

This clause describes the Physical Medium Dependent (PMD) sublayer for EPON Protocol over Coax (EPoC) PHYs operating at the line rate of up to 10 Gb/s in the downstream direction and up to 1.6 Gb/s in the upstream direction.

100.1.1 Terminology and conventions

EPoC operates over a point-to-multipoint (P2MP) topology composed of passive segments of coaxial media and passive taps/couplers, optionally interconnected with active coaxial amplifiers, and/or analog optical links creating a tree-and-branch topology.

The device connected at the root of the tree is called a Coaxial Line Terminal (CLT) and the devices connected as the leaves are referred to as Coaxial Network Units (CNUs). The direction of transmission from the CLT to CNUs is referred to as the *downstream direction*, while the direction of transmission from CNUs to the CLT is referred to as the *upstream direction*.

Unless otherwise noted, the notation $\lceil x \rceil$ represents a *ceiling* function, which returns the value of its argument x rounded up to the nearest integer.

The notation $\lfloor x \rfloor$ represents a *floor* function, which returns the value of its argument x rounded down to the nearest integer.

100.1.2 Positioning of the PMD sublayer within the IEEE 802.3 architecture

Figure 100–1 depicts the relationships of the asymmetric-rate EPoC PMD sublayer (shown hatched) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

100.1.3 PMD types

In the downstream direction, the signal transmitted by the 10GPASS-XR-D type PMD is received by all 10GPASS-XR-U type PMDs. In the upstream direction, the 10GPASS-XR-D type PMD receives data bursts from each of the 10GPASS-XR-U type PMDs. The 10GPASS-XR-D and 10GPASS-XR-U PMDs both have a variable rate that is determined when configured. See Equation (100–1) and Equation (100–2) for additional information on the 10GPASS-XR-D and 10GPASS-XR-U data rates, respectively. See 102.4.3 for "reset on change" events that may affect rate calculations.

The asymmetric-rate 10GPASS-XR-D type PMD, transmitting in continuous mode and receiving in burst mode, is defined in this clause, with downstream data rate calculation in 100.3.2.1. The asymmetric-rate 10GPASS-XR-U type PMD, transmitting in burst mode and receiving in continuous mode, is defined in this clause, with upstream data rate calculation in 100.3.2.2. The data rate of a 10GPASS-XR PHY is dependent on network configuration.

100.1.4 Mapping of PMD variables

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the 10GPASS-XR PHY or are communicated between the CLT and the CNU via the PHY Link. The mapping of MDIO control and status variables to PMD variables is shown in Table 100–1. The least significant bit in each variable is mapped to the lowest numbered bit in the lowest numbered register for Clause 45 registers. These variables are used by the PHY Link for PHY management.

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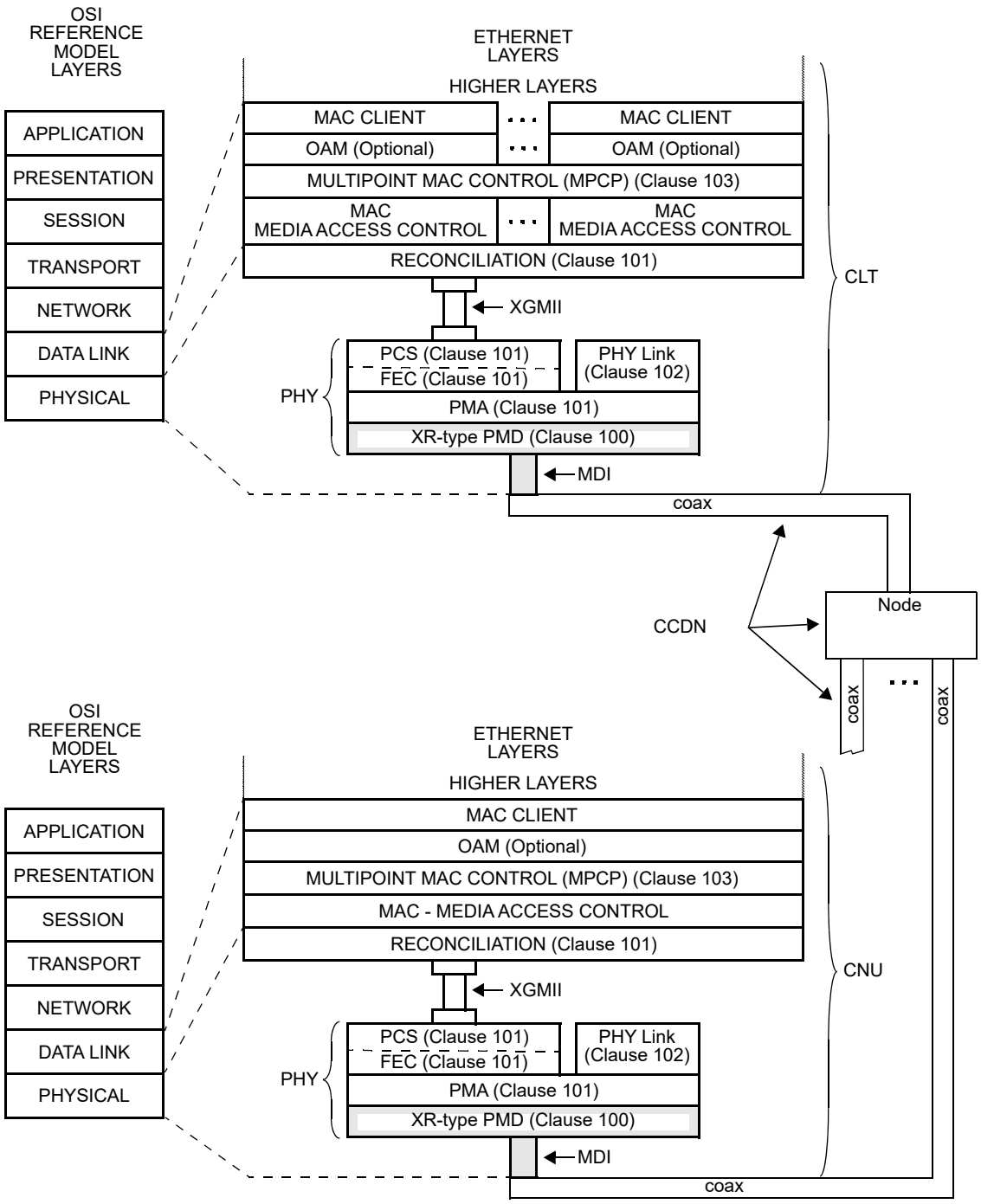

XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
CCDN= COAX CABLE DISTRIBUTION NETWORK
CLT = COAXIAL LINE TERMINAL
CNU = COAXIAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 100–1—Relationship of EPoC P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet LAN model

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Table 100–1—MDIO register to PHY variable mapping

MDIO parameter name	MDIO register name	Register/bit number	PHY variable		
			Name	Index	Bits(s)
PHY discovery enable	10GPASS-XR control	1.1900.0	*PD_Enable*	0	0
DS rate mismatch	10GPASS-XR control	1.1900.11	*DS_RateMatchFail*	0	11
US rate mismatch	10GPASS-XR control	1.1900.12	*US_RateMatchFail*	0	12
DS cyclic prefix	DS OFDM control	1.1901.3:0	*DSNcp*	1	3:0
DS windowing	DS OFDM control	1.1901.6:4	*DSNrp*	1	6:4
CLT tx mute	DS OFDM control	1.1901.15	*CLT_TxMute*	1	15
DS OFDM freq ch 1	DS OFDM channel frequency control 1	1.1902.15:0	*DS_FreqCh(1)*	2	15:0
DS OFDM freq ch 2	DS OFDM channel frequency control 2	1.1903.15:0	*DS_FreqCh(2)*	3	15:0
DS OFDM freq ch 3	DS OFDM channel frequency control 3	1.1904.15:0	*DS_FreqCh(3)*	4	15:0
DS OFDM freq ch 4	DS OFDM channel frequency control 4	1.1905.15:0	*DS_FreqCh(4)*	5	15:0
DS OFDM freq ch 5	DS OFDM channel frequency control 5	1.1906.15:0	*DS_FreqCh(5)*	6	15:0
US cyclic prefix	US OFDM control	1.1907.3:0	*USNcp*	7	3:0
US windowing	US OFDM control	1.1907.6:4	*USNrp*	7	6:4
RB size	US OFDM control	1.1907.7	*RBsize*	7	7
DS PHY data rate fractional	DS PHY data rate	1.1927.2:0	*DS_DataRate(2:0)*	27	2:0
DS PHY data rate lower	DS PHY data rate	1.1927.15:3	*DS_DataRate(15:3)*	27	15:3
DS PHY data rate mid	DS PHY data rate	1.1928.15:0	*DS_DataRate(31:16)*	28	15:0
DS PHY data rate upper	DS PHY data rate	1.1929.4:0	*DS_DataRate(36:32)*	29	4:0
US PHY data rate fractional	US PHY data rate	1.1930.2:0	*US_DataRate(2:0)*	30	2:0
US PHY data rate lower	US PHY data rate	1.1930.15:3	*US_DataRate(15:3)*	30	15:3
US PHY data rate mid	US PHY data rate	1.1931.15:0	*US_DataRate(31:16)*	31	15:0
US PHY data rate upper	US PHY data rate	1.1932.5:0	*US_DataRate(36:32)*	32	5:0
US target receive power	US target receive power	1.1950.9:0	*CLT_TargetReceivePower*	50	9:0

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Table 100–1—MDIO register to PHY variable mapping *(continued)*

MDIO parameter name	MDIO register name	Register/bit number	PHY variable		
			Name	Index	Bits(s)
DS transmit power Ch 1 through DS transmit power Ch 5	DS transmit power	1.1951.8:0 through 1.1955.8:0	*DS_PowerCh(1)* through *DS_PowerCh(5)*	51 through 55	8:0
US receive power measurement	US receive power measurement	1.1956.8:0	*RxPwr*	56	8:0
US receive power valid	US receive power valid	1.1956.15	*RxPwrValid*	56	15
US receive power CNU	US receive power CNU	1.1957.14:0	*RxPwr_CNU_ID*	57	14:0
Reported power	Reported Power	1.1958.8:0	*ReportedPwr*	58	8:0
DS OFDM channel ID	DS OFDM channel ID	*12.0.2:0*	*DS_OFDM_ID*	1000	2:0
DS Modulation type SC4	10GPASS-XR DS profile descriptor control 1	12.1.3:0	*DS_ModTypeSC(4)*	1001	3:0
DS Modulation type SC5	10GPASS-XR DS profile descriptor control 1	12.1.7:4	*DS_ModTypeSC(5)*	1001	7:4
DS Modulation type SC6	10GPASS-XR DS profile descriptor control 1	12.1.11:8	*DS_ModTypeSC(6)*	1001	11:8
DS Modulation type SC7	10GPASS-XR DS profile descriptor control 1	12.1.15:12	*DS_ModTypeSC(7)*	1001	15:12
DS Modulation type SC8 through DS Modulation type SC4095	10GPASS-XR DS profile descriptor control 2 through 10GPASS-XR DS profile descriptor control 1023	12.2 through 12.1023	*DS_ModTypeSC(8)* through *DS_ModTypeSC(4095)*	1002 through 2023	as in Index 1001
US Modulation type SC0	10GPASS-XR US profile descriptor control 0	12.1024.3:0	*US_ModTypeSC(0)*	2024	3:0
US Modulation type SC1	10GPASS-XR US profile descriptor control 0	12.1024.7:4	*US_ModTypeSC(1)*	2024	7:4
US Modulation type SC2	10GPASS-XR US profile descriptor control 0	12.1024.11:8	*US_ModTypeSC(2)*	2024	11:8
US Modulation type SC3	10GPASS-XR US profile descriptor control 0	12.1024.15:12	*US_ModTypeSC(3)*	2024	15:12
US Modulation type SC4 through US Modulation type SC4095	10GPASS-XR US profile descriptor control 1 through 10GPASS-XR US profile descriptor control 1023	12.1025 through 12.2047	*US_ModTypeSC(4)* through *US_ModTypeSC(4095)*	2025 through 3047	as in Index 2024
Real pre-equalizer coefficient SC0	10GPASS-XR US pre-equalizer coefficients 0	12.2048.15:0	*EQ_CoefR(0)*	3048	15:0
Imaginary pre-equalizer coefficient SC0	10GPASS-XR US pre-equalizer coefficients 0	12.2049.15:0	*EQ_CoefI(0)*	3049	15:0

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Table 100–1—MDIO register to PHY variable mapping *(continued)*

MDIO parameter name	MDIO register name	Register/bit number	PHY variable		
			Name	Index	Bits(s)
Real pre-equalizer coefficient SC1 through Real pre-equalizer coefficient SC4095	10GPASS-XR US pre-equalizer coefficients 1 through 10GPASS-XR US pre-equalizer coefficients 4095	12.2050 12.2052 ... 12.10238	*EQ_CoefR(1)* through *EQ_CoefR(4095)*	3050 3052 ... 11238	15:0
Imaginary pre-equalizer coefficient SC1 through Imaginary pre-equalizer coefficient SC4095	10GPASS-XR US pre-equalizer coefficients 1 through 10GPASS-XR US pre-equalizer coefficients 4095	12.2051 12.2053 ... 12.10239	*EQ_CoefI(1)* through *EQ_CoefI(4095)*	3051 3053 ... 11239	15:0
MER measurement valid	10GPASS-XR receive MER Control	12.10240.3	*RxMER_Valid*	11240	3
Receive MER Channel ID	10GPASS-XR receive MER Control	12.10240.2:0	*RxMER_ChID*	11240	2:0
MER measurement CNU ID	10GPASS-XR receive MER Control	12.10241.14:0	*RxMER_CNU_ID*	11241	14:0
Receive MER SC2	10GPASS-XR receive MER measurement	12.10242.7:0	*RxMER_SC(2)*	11242	7:0
Receive MER SC3	10GPASS-XR receive MER measurement	12.10242.15:8	*RxMER_SC(3)*	11242	15:8
Receive MER SC4 through DS receive MER SC4095	10GPASS-XR receive MER measurement	12.10443 12.10244 ... 12.13288	*RxMER_SC(4)* through *RxMER_SC(4095)*	11443 through 14288	as in Index 11241

100.2 PMD functional specification

The 10GPASS-XR type PMDs perform the transmit and receive functions that convey data between the PMD service interface and the MDI. PMD functions are implementation-dependent and include digital-to-analog conversion, analog-to-digital conversion, interpolation, analog filtering, frequency conversion, and/or RF power amplification.

100.2.1 PMD service interface

The following specifies the services provided by Clause 100 PMDs. The service interface is described in an abstract manner and does not imply any particular implementation.

The PMD service interface supports the exchange of a continuous stream of OFDM/OFDMA time domain sampled waveform between the PMA and PMD entities. The samples are encoded as complex numbers, i.e., I/Q value pairs.

The PMD translates data received from the compatible PMA to and from signals suitable for the specified coaxial medium. The following primitives are defined:

— PMD_UNITDATA.request
— PMD_UNITDATA.indication

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— PMD_SIGNAL.request

100.2.1.1 PMD_UNITDATA.request

This primitive defines the transfer of one modulated symbol encoded as an I/Q value pair from the Clause 101 PMA to the Clause 100 PMD.

The semantics of the service primitive are PMD_UNITDATA.request(*I_value*, *Q_value*, *ChNum*). The data conveyed by PMD_UNITDATA.request is a continuous stream of I/Q value pairs and target OFDM channel. Both *I_value* and *Q_value* are encoded as 32-bit signed integers. *ChNum* indicates the applicable channel.

The Clause 101 PMA continuously sends the stream of I/Q value pairs and OFDM channel number to the Clause 100 PMD for transmission on the medium, at the nominal rate of 204.8 million samples per second (Msps). Upon the receipt of this primitive, the PMD converts the received appropriately formatted I/Q value pairs into the appropriate signals at the MDI, effectively sending data across the coaxial media.

100.2.1.2 PMD_UNITDATA.indication

This primitive defines the transfer of I/Q value pair data from the Clause 100 PMD to the Clause 101 PMA.

The semantics of the service primitive are PMD_UNITDATA.indication(*I_value*, *Q_value, ChNum*). The data conveyed by PMD_UNITDATA.indication is a continuous stream of I/Q value pairs and received OFDM channel. Both *I_value* and *Q_value* are encoded as 32-bit signed integers. *ChNum* indicates the applicable channel.

The Clause 100 PMD continuously sends an appropriately formatted stream of I/Q value pairs and OFDM channel number to the Clause 101 PMA corresponding to the signals received from the MDI, at the nominal rate of 204.8 Msps.

100.2.1.3 PMD_SIGNAL.request

The semantics of the service primitive are PMD_SIGNAL.request(*Tx_Enable*). The *Tx_Enable* parameter can take on one of the following two values: ON or OFF, determining whether the PMD transmitter is on (enabled) or off (disabled). The Clause 101 PCS generates this primitive to indicate a change in the value of *Tx_Enable* parameter. Upon the receipt of this primitive, the Clause 100 PMD turns the transmitter on or off as appropriate.

As input to the PMD, PMD_SIGNAL.request is the OR product of the signal from PCS data detector (see 101.3.2.5.1) with that from the PHY Link (see 102.3.1.3) signaling RF power amplifier turn on to the PMD; either the PCS data detector or the PHY Link may signal ON. When both the PCS and the PHY Link set the value to OFF, this signals RF power amplifier turn off to the PMD.

100.2.2 Delay constraints

The PMD shall introduce a transmit delay variation of no more than 0.5 time_quanta, and a receive delay variation of no more than 0.5 time_quanta. A description for the time_quantum can be found in 77.2.2.1.

100.2.3 PMD transmit function

The PMD Transmit function conveys the I/Q value pairs requested by the PMD service interface message PMD_UNITDATA.request(*I_value, Q_value, ChNum*) to the MDI according to the PMD to MDI RF specifications in 100.3.3 and 100.3.4.

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In the upstream direction, the flow of appropriately formatted stream of I/Q value pairs is interrupted according to PMD_SIGNAL.request(*Tx_Enable*).

100.2.4 PMD receive function

The PMD Receive function conveys the bits received from the MDI to the PMD service interface using the message PMD_UNITDATA.indication(*I_value, Q_value*), creating appropriately formatted stream of I/Q value pairs and OFDM channel information.

100.2.5 PMD transmit enable function

The PMD_SIGNAL.request(*Tx_Enable*) message is defined for the CNU PMD specified in this clause. The PMD_SIGNAL.request(*Tx_Enable*) message is asserted prior to data transmission by the CNU PMDs. Note PMD_SIGNAL.request(*Tx_Enable*) message is not defined for the CLT; CLT PMD data transmission is always enabled.

100.3 PMD operational requirements

100.3.1 CLT and CNU modulation formats

The CLT and CNU transmitters and receivers shall support the mandatory modulation formats as specified in Table 100–2.

Table 100–2—Modulation formats

Modulation format[a]	MAC data path		PHY Link data path	
	CLT Tx CNU Rx	CNU Tx CLT Rx	CLT Tx CNU Rx	CNU Tx CLT Rx
BPSK[b]	M	M	M	M
QPSK	N/S	M[c]	N/S	N/S
8-QAM	O	M[c]	N/S	N/S
16-QAM	O	M	M	M
32-QAM	O	M	N/S	M
64-QAM	M	M	N/S	M
128-QAM	M	M	N/S	M
256-QAM	M	M	N/S	N/S
512-QAM	M	M	N/S	N/S
1024-QAM	M	M	N/S	N/S
2048-QAM	M	O	N/S	N/S
4096-QAM	M	O	N/S	N/S
8192-QAM	O	N/S	N/S	N/S
16384-QAM	O	N/S	N/S	N/S

[a] M = mandatory, O = optional, N/S = not supported.
[b] Used for pilots, burst markers, preambles, and probes.
[c] This modulation format is required only for low density pilots.

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See 102.2.1.2 and 102.3.1.2, respectively, for a description of downstream and upstream PHY Link modulation.

The CNU reports supported optional modulations to the CLT via *US_ModAbility* variable see 101.4.4.4.4.

100.3.2 Data rates

In baseline channel conditions, as defined in Annex 100A, a 192 MHz OFDM channel supports a data rate of at least 1.6 Gb/s at the MAC/PLS interface. The MAC date rate scales linearly with the number of OFDM channels, for the same baseline channel conditions in the upstream OFDMA channel and each downstream OFDM channel.

100.3.2.1 Downstream PHY data rate

The CLT calculates the downstream PMA data rate after any configuration update that changes the downstream profile descriptor variables *DS_ModTypeSC(n)* or for any change to the cyclic prefix size *DSNcp*. See 101.4.3.4.5 and 101.4.3.12.1. Specifically after any configuration change and after the continuous and scattered pilot map has been updated (see 101.4.3.6), the CLT shall update the value of the variable *DS_DataRate*.

The downstream PMA OFDM superframe repeats every 128 symbols. The superframe length is determined using the *DS_Extended_OFDM_Symbol* based on size of the selected cyclic prefix.

$$DS\_Frame\_Length = 128 \times DS\_Extended\ OFDM\ Symbol\ (\mu s)$$

$$DS\_Extended\_OFDM\_Symbol = 20 + DSNcp\ (\text{downstream})\ (\mu s)$$

The downstream OFDM frame data load (bits) is a summation over all active downstream OFDM channels, as defined by *DS_ChCnt*, over 128 symbols, the summation of bit per subcarrier for all active subcarriers (subcarriers that are not configured as excluded are active subcarriers).

$$DS\_Frame\_Data\_Load = \sum_{c=1}^{DS\_ChCnt} \text{active channel}_c \left(\sum_{s=1}^{128} \text{symbol}_s \left(\sum_{sc=0}^{4095} \text{bits per symbol}_{sc} \right) \right)$$

PHY Link, excluded, and unused subcarriers and continuous and scattered pilots are skipped. Note that in the definition of *DS_ModTypeSC(n)* the values binary 0011 (3 decimal) through 1110 (14 decimal) directly represent the number of data bits per active subcarrier (see 101.4.3.4.5).

DS_Frame_Data_Load has the same value every downstream OFDM frame, therefore *DS_DataRate* remains the same for any given downstream profile descriptor configuration as shown in Equation (100–1):

$$DS\_DataRate = DS\_Frame\_Data\_Load / DS\_Frame\_Length\ (\text{b/s}) \qquad (100\text{–}1)$$

Equation (100–1) establishes nominal data rate for CLT PMA_UNITDATA.request service interface.

Based on the current profile, the CLT calculates *DS_DateRate* and communicates this to the CNU. The CNU also calculates *DS_DataRate* based on the configured profile. If the CNU calculation differs from the CLT value by more than 10 b/s, the CNU sets *DS_RateMatchFail* to TRUE indicating mismatch; otherwise it is set to FALSE.

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100.3.2.2 Upstream PHY data rate

The CLT calculates the upstream PMA data rate after any configuration update that changes the upstream profile descriptor variables *US_ModTypeSC(n)* or for any change to the cyclic prefix size *USNcp*. See 101.4.4.4.4 and 101.4.4.10.1. Specifically after any configuration change and after the Type I and Type II pilot map has been updated (see 101.4.4.6), the CLT shall update the value of the variable *US_DataRate*.

The upstream PMA RB Superframe repeats every 256 + 6 symbols, where the Probe region is 6 symbols in length. The superframe length is determined using the *US_Extended_OFDM_Symbol* based on size of the selected cyclic prefix size (μs).

$$US\_Frame\_Length = (256 + 6) \times US\_Extended\ OFDM\ Symbol \ (\mu s)$$

$$US\_Extended\_OFDM\_Symbol = 20 + USNcp \ (\mu s)$$

The upstream OFDM frame data load (bits) is a summation over the 256 symbols, the summation of bits per Resource Element. For a low density type "L" pilot Resource Element, the value is the *US_ModTypeSC(n)* value minus 4 (decimal) or 1, whichever is higher. The probe region symbols are not included in this summation.

$$US\_Frame\_Data\_Load = \sum_{s=1}^{256} \text{symbol}_s \left(\sum_{RE=0}^{4095} \text{resource element}_{RE} \right)$$

PHY Link, excluded, and unused subcarriers and type "P" pilot Resource Elements are skipped. Note that in the definition of *US_ModTypeSC(n)* the values binary 0011 (3 decimal) through 1110 (14 decimal) directly represent the number of data bits per active subcarrier (see 101.4.4.4.4).

A Resource Element is a single subcarrier over the duration of a single symbol. A Resource Block is a group of 8 or 16 adjacent Resource Elements in the same subcarrier as defined by the variable *RBsize* (see 101.4.4.3.1).

US_Frame_Data_Load has the same value every upstream RB Superframe; therefore, *US_DataRate* remains the same for any given upstream profile descriptor configuration as shown in Equation (100–2):

$$US\_DataRate = US\_Frame\_Data\_Load / US\_Frame\_Length \ (\text{b/s}) \qquad (100–2)$$

Note that *US_DataRate* does not include PCS or burst marker overheads.

This establishes nominal data rate for CLT PMA_UNITDATA.request service interface and also serves as the negotiated upstream PHY data rate for each CNU.

Based on the current profile, the CLT calculates *US_DateRate* and communicates this to the CNU. The CNU also calculates *US_DataRate* based on the configured profile. If the CNU calculation differs from the CLT value by more than 10 b/s, the CNU sets *US_RateMatchFail* to TRUE indicating mismatch; otherwise it is set to FALSE.

100.3.2.3 PHY Link managed variables

DS_ChCnt

TYPE: 3-bit unsigned integer

This variable indicates the number of downstream OFDM channels in use. The value of *DS_ChCnt* is between 1 and 5.

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DS_DataRate

TYPE: UQ34.3 format

This variable indicates the downstream data rate in units of b/s and is calculated as shown in Equation (100–1).

DS_FreqCh(n)

TYPE: 16-bit unsigned integer

This variable specifies the center frequency, in units of 50 kHz, of subcarrier 0 for the downstream OFDM channel n ($1 \le n \le 5$). Subcarriers are numbered from 0 to 4095 with subcarrier 0 at the lowest frequency. This definition equates to a subcarrier 0 center frequency of 54 MHz to 3276.75 MHz. The minimum value for this register is 1080. See Table 100–3 for additional details.

DS_RateMatchFail

TYPE: Boolean

This variable is set to TRUE if the CNU calculation of *DS_DataRate* differs from the *DS_DataRate* calculation communicated from the CLT by more than 10 b/s; otherwise, the variable is set to FALSE.

US_DataRate

TYPE: UQ34.3 format

This variable indicates the upstream data rate in units of b/s and is calculated as shown in Equation (100–2).

US_FreqCh1

TYPE: 16-bit unsigned integer

This variable specifies the center frequency, in units of 50 kHz, of subcarrier 0 for the upstream OFDMA channel. Subcarriers are numbered from 0 to 4095 with subcarrier 0 at the lowest frequency. This definition equates to a subcarrier 0 center frequency of 0 MHz to 3276.75 MHz. The minimum value for this register is 148 to accommodate starting at 7.4 MHz. See Table 100–11 for additional details.

US_RateMatchFail

TYPE: Boolean

This variable is set to TRUE if the CNU calculation of *US_DataRate* differs from the *US_DataRate* calculation communicated from the CLT by more than 10 b/s; otherwise, the variable is set to FALSE.

100.3.3 CLT transmitter requirements

100.3.3.1 OFDM channel power definitions

This subclause defines the terms and concepts used when specifying the CLT RF output requirements. For an OFDM channel there is a) the number of equivalent 6 MHz channels (*Neq*), b) the encompassed spectrum, c) the modulated spectrum, and d) the number of active equivalent 6 MHz channels (*Neq*').

The number of equivalent 6 MHz channels, *Neq*, is constant and calculated for a single OFDM channel size of 192 MHz as follows: 192/6 = 32.

Neqport at the MDI is the sum of the individual *Neq* of each OFDM channel.

The total number of OFDM channels, *NOFDM* is 5. Thus, *Neqport* is 5 × 32 = 160.

The encompassed spectrum is the difference between a) the center frequency of the highest frequency active subcarrier of the highest frequency OFDM channel and b) the center frequency of the lowest frequency active subcarrier of the lowest frequency OFDM channel, plus the subcarrier spacing of 0.05 MHz (all

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expressed in MHz). The encompassed spectrum of a single OFDM channel is the difference between the center frequency of the highest frequency active subcarrier and the center frequency of the lowest frequency active subcarrier in the OFDM channel, plus the subcarrier spacing.

Occupied spectrum (*Occupiedspectrum*) as shown in Equation (100–3) is the accumulation of the bandwidth (RF spectrum) in all channel frequency allocations (e.g., 6 MHz *channelsize*) that are occupied by the OFDM channel (*OFDMchannelbandwidth*).

$$Occupiedspectrum = channelsize \times \lceil OFDMchannelbandwidth / channelsize \rceil \quad (100–3)$$

The occupied spectrum is a multiple of 6 MHz and consists of all 6 MHz channels that are included in the encompassed spectrum, plus the taper region shaped by the OFDM channels' transmit windowing; the out-of-band spurious emissions requirements in 100.3.3.5 (except for interior exclusion band spurious emissions requirements) apply outside the occupied spectrum. With a 1 MHz taper region on each band edge of the OFDM channel, shaped by the transmit windowing function, an encompassed spectrum of 190 MHz of active subcarriers has 192 MHz of occupied spectrum.

An exclusion band is a contiguous block of excluded spectrum that is 1 MHz wide or greater. An individually excluded subcarrier is any excluded subcarrier in a contiguous block of excluded spectrum less than 1 MHz.

The modulated spectrum of a single OFDM channel is the encompassed spectrum minus the total spectrum in the internal excluded subbands of the OFDM channel, where the total spectrum in the internal excluded subbands is equal to the number of subcarriers in all of the internal excluded subbands of the OFDM channel multiplied by the subcarrier spacing of the OFDM channel. For example, with 190 MHz encompassed spectrum, if there are 188 subcarriers total in three internal exclusion subbands, then the total spectrum in the internal excluded subbands (in MHz) is $188 \times 0.05 = 9.4$ MHz, and the modulated spectrum is 190 MHz – 9.4 MHz = 180.6 MHz.

The modulated spectrum at the MDI (TP1, see 100.4) is the sum of the modulated spectrum of each OFDM channel.

The number of active equivalent 6 MHz channels, *Neq'*, for an OFDM channel is a function of the modulated spectrum (MHz) of a channel as calculated in Equation (100–4).

$$Neq' = \lceil modulated\ spectrum\ of\ a\ single\ channel / channelsize \rceil \quad (100–4)$$

Neqport' at the MDI is the sum of the *Neq*' of each OFDM channel.

The CLT shall comply with all CLT transmitter requirements (see 100.3.3) operating with all *Neqport* channels on the MDI and with all requirements for the device operating with *Neqport*' active channels on the MDI for all values of *Neqport*' less than *Neqport*.

100.3.3.2 CLT output electrical requirements

For OFDM, all modulated subcarriers in an OFDM channel are set to the same average power (except pilots that are boosted by 6 dB). For the purposes of meeting spurious emissions requirements, for each OFDM channel:

— Configure the OFDM channel power using the commanded average power of an equivalent 6 MHz channel for the first OFDM channel, which is *DS_PowerCh*(1) (see Table 100–5) as follows:

  —CLT calculates power for data subcarrier and pilots using the subcarriers in the 6 MHz band centered on the PHY Link.

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NOTE—The configured average power of an equivalent 6 MHz channel for the first OFDM channel is defined as the power for the 6 MHz band centered on the PHY Link.

— For the second OFDM channel, let X dB be the commanded average power of an equivalent 6 MHz channel for the second OFDM channel minus commanded average power of an equivalent 6 MHz channel for the first OFDM channel; i.e., $X \text{ dB} = DS\_PowerCh(2) - DS\_PowerCh(1)$. Then set the data subcarrier power for the second channel equal to data subcarrier power for the first channel plus X dB.

— Data subcarrier power for the third, fourth, and fifth OFDM channels are computed relative to the first OFDM channel in the same fashion.

A CLT shall output an OFDM RF modulated signal with the characteristics defined in Table 100–3, Table 100–5, and Table 100–6. These requirements are to be met under the conditions where the configured average power of an equivalent 6 MHz channel is the same for each OFDM channel, with the exception of the following: single channel active phase noise, diagnostic carrier suppression, OFDM phase noise, OFDM diagnostic suppression, and power difference requirements, and as described for out-of-band noise and spurious requirements.

Table 100–3—CLT RF output requirements

Parameter	Value	Units
Downstream 10.24 MHz Master Clock frequency	10.24	MHz
Frequency band	258 to 1218	MHz
OFDM channel bandwidth (*OFDMchannelbandwidth*)	24 to 192	MHz
Encompassed spectrum	22 to 190	MHz
Subcarrier spacing	50	kHz
OFDM symbol rate FFT duration	20	μs
FFT size	4096	FFT bins
Maximum number of active subcarriers per FFT	3800	subcarriers
Level	See Table 100–5	
Modulation format	See Table 100–2	
Transmit MUTE when TRUE.[a] See 100.4.1.	≥ 73	dBc
Inband spurious, distortion, and noise[d]		
For measurements below 600 MHz[a]	≤ –50	dBr
For measurements from 600 MHz to 1002 MHz[a]	≤ –47	dBr
For measurements 1002 MHz to 1218 MHz[b]	≤ –45	dBr
MER in 192 MHz OFDM channel occupied spectrum 528 MHz total occupied spectrum, 88 equivalent 6 MHz channels[c, d, e, f, g]		
For measurements below 600 MHz:		
Any single subcarrier	≥ 48	dB
Average over the complete OFDM channel[h]	≥ 50	dB
For measurements from 600 MHz to 1002 MHz:		

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Table 100–3—CLT RF output requirements *(continued)*

Parameter	Value	Units
Any single subcarrier	≥ 45	dB
Average over the complete OFDM channel[g]	≥ 47	dB
For measurements 1002 MHz to 1218 MHz:		
Any single subcarrier	≥ 43	dB
Average over the complete OFDM channel[g]	≥ 45	dB
MER in 24 MHz OFDM channel occupied spectrum, single OFDM channel only, 24 MHz total occupied spectrum.[b, c, d, i] Average over the complete OFDM channel:		
For measurements below 600 MHz	≥ 48	dB
For measurements from 600 MHz to 1002 MHz	≥ 45	dB
For measurements 1002 MHz to 1218 MHz	≥ 43	dB
Output impedance	75	Ω
Output return loss. Specified for within an active output OFDM channel or in every inactive OFDM channel as noted.		
88 MHz to 750 MHz; active	> 14	dB
750 MHz to 870 MHz; active	> 13	dB
870 MHz to 1218 MHz; active	> 12	dB
54 MHz to 870 MHz; inactive	> 12	dB
870 MHz to 1218 MHz; inactive	> 10	dB
MDI Connector	F connector per ISO/IEC-61169-24 or SCTE 02	

[a]RF output power below the operationally configured aggregate power of the RF modulated signal, in every 6 MHz channel from 258 MHz to 1218 MHz.
[b]Average over center 400 kHz subcarriers within gap.
[c]Receiver OFDM channel estimation is applied in the test receiver; test receiver does best estimation possible. Transmit windowing is applied to potentially interfering channel and selected to be sufficient to suppress cross channel interference.
[d]Modulation error ratio (MER) is determined by the cluster variance caused by the transmit waveform at the output of the ideal receive matched filter. MER includes all discrete spurious, noise, subcarrier leakage, clock lines, synthesizer products, distortion, and other undesired transmitter products. Phase noise up to ± 50 kHz of the subcarrier's center frequencies is excluded from inband specification, to separate the phase noise and inband spurious requirements as much as possible. In measuring MER, record length or carrier tracking loop bandwidth may be adjusted to exclude low-frequency phase noise from the measurement. MER requirements assume measuring with a calibrated test instrument with its residual MER contribution removed.
[e]Phase noise up to 10 MHz offset is mitigated in test receiver processing or by test equipment (latter using hardline carrier from modulator, which requires special modulator test port and functionality).
[f] Up to five subcarriers in one OFDM channel can be excluded from this requirement.
[g] When the estimated channel impulse response used by the test receiver is limited to half of length of smallest transmit cyclic prefix then there is a 2 dB relief for above requirements (e.g., MER > 48 dB becomes MER > 46 dB).
[h]See 100.4.2 for average MER calculation method.
[i]A single subcarrier in the OFDM channel can be excluded from this requirement, no windowing is applied and minimum CP is selected.

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100.3.3.2.1 PHY Link managed variables

DS_PowerCh(n)

TYPE: 9-bit unsigned integer.
This variable specifies the downstream CLT transmit power, in units of 0.2 dBmV/6 MHz, for OFDM channel n ($1 \le n \le 5$). The value is set according to the requirements in Table 100–5.

100.3.3.3 Phase noise requirements

The CLT transmitted signal for each OFDM channel shall meet the phase noise requirements as per Table 100–4.

Table 100–4—Downstream phase noise requirements

Parameter	Value	Units
Phase noise, integrated double-sided maximum, 1002 MHz or lower:		
1 kHz to 10 kHz	–48	dBc
10 kHz to 100 kHz	–56	dBc
100 kHz to 1 MHz	–60	dBc
1 MHz to 10 MHz	–54	dBc
10 MHz to 100 MHz	–60	dBc

100.3.3.4 Power per OFDM channel for CLT

The CLT shall adjust the RF transmit power per Table 100–5. In Table 100–5 the value for N^*, the adjusted number of active channels combined per MDI, is calculated using Equation (100–5).

$$\text{If } \left(Neqport' < \frac{Neqport}{4}\right) \text{ then } \left(N^* = \text{minimum}\left(4Neqport', \left\lceil \frac{Neqport}{4} \right\rceil\right)\right)$$
$$\text{If } \left(Neqport' \ge \frac{Neqport}{4}\right) \text{ then } (N^* = Neqport') \quad (100\text{–}5)$$

The applicable maximum power per OFDM channel and spurious emissions requirements are defined for the CLT using the value of N^* per Equation (100–5).

Table 100–5—CLT RF output power requirements

Parameter	Value[a,b,c]	Units
Maximum value of OFDM channel power in the OFDM channel occupied spectrum normalized to 6 MHz ((OFDM signal power/occupied spectrum) × 6 MHz:		
Neqport' OFDM channels combined onto a single MDI for *Neqport*' ≥ *Neqport*/4	$60 - \lceil 3.6 \times \log_2(N^*) \rceil$ [d]	dBmV/6 MHz
Neqport' OFDM channels combined onto a single MDI for 4 ≤ *Neqport*' < *Neqport*/4[c]	$60 - \lceil 3.6 \times \log_2(N^*) \rceil$ [d]	dBmV/6 MHz

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Table 100–5—CLT RF output power requirements *(continued)*

Parameter	Value[a,b,c]	Units
Range of commanded transmit power for each OFDM channel, at least 8 dB below the required power level specified above, maintaining full fidelity over the range	≥ 8	dB
Commanded power per OFDM channel step size. Strictly monotonic.	≤ 0.2	dB
Power difference between any two adjacent OFDM channels in the 108 MHz to 1218 MHz downstream spectrum[e]	≤ 0.5	dB
Power difference (normalized for bandwidth) between any two channels' OFDM channel blocks in the 108 MHz to 1218 MHz downstream spectrum[e]	≤ 2	dB
Power per channel absolute accuracy	± 2	dB

[a]Add 3 dB relaxation to the values specified above for noise and spurious emissions requirements in all channels with 603 MHz ≤ center frequency ≤ 999 MHz. For example –73 dBc becomes –70 dBc. Also see 100.3.3.5.
[b]Add 1 dB relaxation to the values specified above for noise and spurious emissions requirements in gap channels with center frequency below 600 MHz. For example –73 dBc becomes –72 dBc. Also see 100.3.3.5.
[c]Add 5 dB relaxation to the values specified above for noise and spurious emissions requirements in all channel with 999 MHz < center frequency of the noise measurement ≤ 1215 MHz. For example –73 dBc becomes –68 dBc. Also see 100.3.3.5.
[d]These ceiling functions round to the nearest 0.5.
[e]The power difference in this context is the accuracy of measured differential power between two channels of interest as compared to the configured differential power between those two channels.

100.3.3.5 Out-of-band noise and spurious requirements for the CLT

Table 100–6 lists the out-of-band spurious requirements. In cases where the configured average power of an equivalent 6 MHz channel is not the same for each OFDM channel, 0 dBc for the spurious emissions requirements corresponds to the largest configured average power of an equivalent 6 MHz channel among all the active OFDM channels. When the configured average power of an equivalent 6 MHz channel is the same for each OFDM channel, 0 dBc should be interpreted as the measured power of the 6 MHz band centered on the PHY Link contained in OFDM channel 1.

The 10GPASS-XR-D PMD shall satisfy the out-of-band spurious emissions requirements of Table 100–6 in measurements below 600 MHz and outside the encompassed spectrum when the active OFDM channels are contiguous or when the ratio of modulated spectrum to gap spectrum within the encompassed spectrum is 4:1 or greater. Gap spectrum is spectrum between active OFDM channel's occupied spectrum and excluded bands within OFDM channel's occupied spectrum.

The 10GPASS-XR-D PMD shall satisfy the out-of-band spurious emissions requirements of Table 100–6 in gap spectrum between OFDM channels of at least 6 MHz and within exclusion bands within OFDM channels of at least 8 MHz, except for the 1 MHz of excluded subcarriers on each edge of any exclusion band, with relaxations as described in the following paragraphs when applicable.

The 10GPASS-XR-D PMD shall satisfy the out-of-band spurious emissions requirements of Table 100–6, with 1 dB relaxation, in measurements within gap spectrum in modulated spectrum below 600 MHz and within the encompassed spectrum when the ratio of modulated spectrum to gap spectrum within the encompassed spectrum is 4:1 or greater.

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The 10GPASS-XR-D PMD shall satisfy the out-of-band spurious emissions requirements of Table 100–6, with 3 dB relaxation, when the ratio of modulated spectrum to gap spectrum within the encompassed spectrum is 4:1 or greater, in measurements from 603 MHz to 999 MHz inclusive, outside the encompassed spectrum or in gap spectrum within the encompassed spectrum.

The 10GPASS-XR-D PMD shall satisfy the out-of-band spurious emissions requirements of Table 100–6, with 5 dB relaxation, when the ratio of modulated spectrum to gap spectrum within the encompassed spectrum is 4:1 or greater, in measurements from 999 MHz to 1209 MHz inclusive, outside the encompassed spectrum or in gap spectrum within the encompassed spectrum.

The 10GPASS-XR-D PMD shall satisfy the out-of-band spurious emissions requirements of Table 100–6, in addition to contributions from theoretical transmit windowing, with permissible configurations of lower edge and upper edge subband exclusions of at least 1 MHz each, cyclic prefix length (*DSNcp*) and windowing roll-off period (*DSNrp*) values. The test limit for determining compliance to the spurious emissions requirements is the power sum of the spurious emissions requirements, taken in accordance with Table 100–6 and the contributions from the theoretical transmit windowing for the configured transmissions.

The full set of *Neqport*' active equivalent 6 MHz channels is referred to throughout this specification as the modulated OFDM channels or the active OFDM channels. However, for purposes of determining the spurious emissions requirements for non-contiguous transmitted OFDM channels, each separate contiguous sub-block of channels within the active OFDM channels is identified, and the number of OFDM channels in each contiguous sub-block is denoted as *Neqi*, for $i = 1$ to K, where K is the number of contiguous blocks. Therefore,

$$Neqport' \leq \sum_{i=1}^{K} Neqi \tag{100–6}$$

Because exclusion subbands may be as small as 1 MHz with two or more contiguous sub-blocks within an OFDM channel, the number of active equivalent 6 MHz channels in each contiguous sub-block may add to more than the number of active equivalent 6 MHz channels in the full OFDM channel. Any double-counting of active subcarriers near small exclusion bands is acceptable in calculating the spurious emissions requirements; the equipment has to meet spurious emissions requirements in cases where Equation (100–6) is met with equality and the small relaxation in requirements which results from inequality is thus not compelling.

Note that $K = 1$ when and only when the entire set of active OFDM channels is contiguous. Also note that an isolated transmit OFDM channel, i.e., a transmit channel with empty adjacent OFDM channels, is described by $Neqi = 1$ and constitutes a block of one contiguous OFDM channel. Any number of the contiguous blocks may have such an isolated transmit OFDM channel; if each active OFDM channel was an isolated channel, then $K = Neq'$.

When the *Neqport*' combined active OFDM channels are not contiguous and the ratio of modulated spectrum to gap spectrum within the encompassed spectrum is 4:1 or greater, the spurious emissions requirements are determined by summing the spurious emissions power allowed in a given *Measurement Bandwidth* by each of the contiguous blocks among the occupied spectrum. In the gap spectrum within the encompassed spectrum and below 600 MHz there is a 1 dB relaxation in the spurious emissions requirements, so that within the encompassed spectrum the spurious emissions requirements (in absolute power) are 26% higher power in the measurement band determined by the summing of the contiguous blocks spurious emissions requirements. In all OFDM channels above 600 MHz there is a 3 dB relaxation in the spurious emissions requirements, so that the spurious emissions requirements (in absolute power) are double the power in the measurement band determined by the summing of the contiguous blocks spurious emissions requirements.

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The details of the spurious emissions requirements for non-contiguous OFDM channel operation outside the encompassed spectrum are as follows. Note that within the encompassed spectrum the same details apply, except there is an additional 1 dB allowance below 600 MHz and a 3 dB allowance is applied above 600 MHz for all OFDM channels.

— The noise and spurious power requirements for all contiguous blocks of transmitted channels are determined from Table 100–6, even if the block contains fewer than *Neqport*/4 active OFDM channels. The noise and spurious power requirements for the *i*th contiguous block of transmitted channels is determined from Table 100–6 using the value *Neqi* for the number of active OFDM channels combined per MDI, and using dBc relative to the highest commanded power level of a 6 MHz equivalent channel among all the active OFDM channels, and not just the highest commanded power level in the *i*th contiguous block, in cases where the *Neqport'* combined OFDM channels are not commanded to the same power. The noise and spurious emissions power in each measurement band, including harmonics, from all *K* contiguous blocks, is summed (absolute power, NOT in dB) to determine the composite noise floor for the non-contiguous channel transmission condition. For the measurement OFDM channels adjacent to a contiguous block of channels, the spurious emissions requirements from the non-adjacent blocks are divided on an equal per Hz basis for the narrow and wide adjacent measurement bands.

— For a measurement channel positioned between two contiguous blocks, adjacent to each, the measurement channel is divided into three measurement bands: one wider in the middle and two narrower bands each abutting one of the adjacent transmit channels. The wideband spurious and noise requirement is split into two parts, on an equal per Hz basis, to generate the allowed contribution of power to the middle band and to the farthest narrowband.

In Table 100–6 the value for N^* is calculated using Equation (100–5). Item 1 through item 4 list the requirements in channels adjacent to the active channels. Item 5 lists the requirements in all other channels further from the active channels. Some of these "other" channels are allowed to be excluded from meeting the item 5 specification. All the exclusions, such as 2nd and 3rd harmonics of the modulated channel, are fully identified in the table. Item 6 lists the requirements on the 2*Neqport'* 2nd harmonic channels and the 3*Neqport'* 3rd harmonic channels.

Table 100–6—CLT output out-of-band noise and spurious emissions requirements

Item	Band	Requirement (in dBc)[a,b,c]
1	Adjacent channel up to 750 kHz from channel block edge	For $N^* = 1$: ≤ -58 For $N^* = 2$: ≤ -58 For $N^* = 3$: ≤ -58 For $N^* = 4$: ≤ -58 For $N^* \geq 5$: $\leq 10 \times \log_{10} [10^{-58/10} + (0.75/6) \times (10^{-65/10} + (N^* - 2) \times 10^{-73/10})]$
2	Adjacent channel (750 kHz from channel block edge to 6 MHz from channel block edge)	For $N^* = 1$: ≤ -62 For $N^* \geq 2$: $\leq 10 \times \log_{10} [10^{-62/10} + (5.25/6) \times (10^{-65/10} + (N^* - 2) \times 10^{-73/10})]$
3	Next-adjacent channel (6 MHz from channel block edge to 12 MHz from channel block edge)	$\leq 10 \times \log_{10} [10^{-65/10} + (N^* - 1) \times 10^{-73/10}]$

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Table 100–6—CLT output out-of-band noise and spurious emissions requirements *(continued)*

Item	Band	Requirement (in dBc)[a,b,c]
4	Third-adjacent channel (12 MHz from channel block edge to 18 MHz from channel block edge)	For $N^* = 1$: ≤ -73 For $N^* = 2$: ≤ -70 For $N^* = 3$: ≤ -67 For $N^* = 4$: ≤ -65 For $N^* = 5$: ≤ -64.5 For $N^* = 6$: ≤ -64 For $N^* = 7$: ≤ -64 For $N^* \geq 8$: $\leq -73 + 10 \times \log_{10}(N^*)$
5	Noise in other channels (47 MHz to 1218 MHz) measured in each 6 MHz channel excluding the following: a) Desired channel(s) b) 1st, 2nd, and 3rd adjacent channels (see items 1, 2, 3, 4 in this table) c) Channels coinciding with 2nd and 3rd harmonics (see item 6 in this table)	For $N^* = 1$: ≤ -73; For $N^* = 2$: ≤ -70; For $N^* = 3$: ≤ -68; For $N^* = 4$: ≤ -67; For $N^* \geq 5$: $\leq -73 + 10 \times \log_{10}(N^*)$
6	In each of 2*Neqport*' contiguous 6 MHz channels or in each of 3*Neqport*' contiguous 6 MHz channels coinciding with 2nd harmonic and with 3rd harmonic components, respectively (up to 1218 MHz)	$\leq -73 + 10 \times \log_{10}(N^*)$ or –63, whichever is greater
7	Lower out of band noise in the band of 5 MHz to 47 MHz, measured in 6 MHz channel bandwidth	$\leq -50 + 10 \times \log_{10}(N^*)$
8	Higher out of band noise in the band of 1218 MHz to 3000 MHz, measured in 6 MHz channel bandwidth	For $N^* \leq 8$: $\leq -55 + 10 \times \log_{10}(N^*)$ For $N^* > 8$: $\leq -60 + 10 \times \log_{10}(N^*)$

[a]Add 3 dB relaxation to the values specified above for noise and spurious emissions requirements in all channels with 603 MHz ≤ center frequency ≤ 999 MHz. For example –73 dBc becomes –70 dBc.
[b]Add 5 dB relaxation to the values specified above for noise and spurious emissions requirements in all channels with 999 MHz < center frequency ≤ 1209 MHz. For example –73 dBc becomes –68 dBc.
[c]Add 1 dB relaxation to the values specified above for noise and spurious emissions requirements in gap channels with center frequency below 600 MHz. For example –73 dBc becomes –72 dBc.

100.3.3.6 CLT transmitter output requirements

The CLT shall provide for independent selection of center frequency with the ratio of modulated spectrum to gap spectrum in the encompassed spectrum being at least 2:1.

The CLT shall disable transmitter output when *PD_Enable* is equal to FALSE and continue in normal transmitter operation when *PD_Enable* is equal to TRUE.

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100.3.4 CNU transmitter requirements

100.3.4.1 Burst timing convention

The start time of an OFDMA transmission by a CNU is referenced to an upstream Superframe boundary that begins with a Probe region (6 OFDMA symbols) followed by 256 OFDMA symbols. The 256 OFDMA symbols are divided into 32 8-symbol Resource Blocks, or 16 16-symbol Resource Blocks, as configured by *RBsize* (see 101.4.4.3.1).

The upstream time reference is defined as the first sample of the first symbol of an upstream Superframe, pointed to by the dashed arrow of Figure 100–2. The parameter N_{FFT} refers to the length of the FFT duration of 4096, and the parameter *USNcp* is the length of the configurable cyclic prefix. The sample rate is 204.8 Msps.

The upstream time reference for construction of each OFDMA symbol is defined as the first sample of each FFT duration of each OFDMA symbol, as illustrated in Figure 100–2.

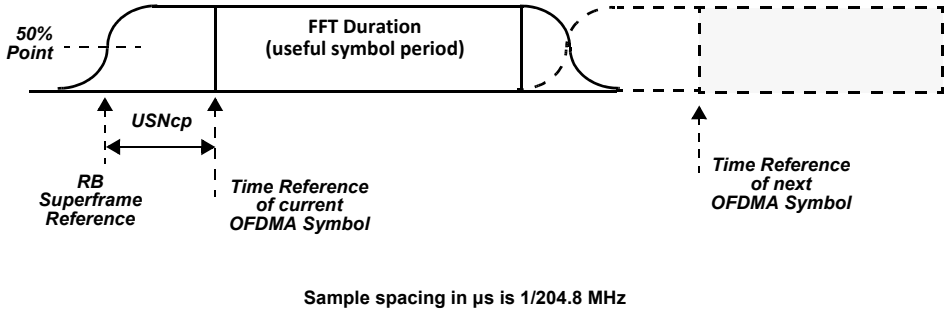

Figure 100–2—Time references for OFDMA symbol and RB Superframe

100.3.4.2 Transmit power requirements

The OFDMA channel power is defined as the average power when all active subcarriers in an OFDMA symbol are granted to the CNU. The normalized channel power of an OFDMA channel is the average power of the OFDMA subcarriers in 1.6 MHz bandwidth with no exclusions. This normalized channel power of an OFDMA channel is denoted as $P_{1.6}$. The transmit power requirements are a function of the occupied spectrum of the OFDMA channel.

The maximum value of the total power output of the CNU P_{Max} is at least 65 dBmV.

For the upstream OFDMA channel, N_{eq} is calculated per Equation (100–7).

$$N_{eq} = \lceil (BW_{OFDMA}) / 1.6 \rceil \quad (100\text{–}7)$$

BW_{OFDMA} (MHz) is the sum of the bandwidth of the modulated spectrum of the OFDMA channel.

Maximum equivalent channel power ($P_{1.6Max}$) is calculated as shown in Equation (100–8).

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$$P_{1.6Max} = P_{Max} - 10 \times \log_{10}(N_{eq}) \quad (100–8)$$

The CLT shall limit the configured $P_{1.6Max}$ to no more than 53.2 + (P_{Max} – 65) dBmV if the bandwidth of the modulated spectrum is ≤ 24 MHz. This enforces a maximum power spectral density of P_{Max} dBmV per 24 MHz.

The minimum equivalent channel power ($P_{1.6Min}$) for OFDMA channels is 17 dBmV.

During PHY Discovery ranging a CNU shall initiate communications starting from lowest power, which is set by the CLT using *PdRespInitPwr* (see 102.4.1.4). Therefore it should be noted that transmissions may use power per subcarrier that is as much as 9 dB lower than indicated by $P_{1.6Min}$ during PHY Discovery.

100.3.4.3 OFDMA transmit power calculations

The CNU determines individual subcarrier transmit power and maintains reported power level $P_{1.6r}$ in dBmV.

The CNU updates its reported power, *ReportedPwr*, by the following steps:

a) $1.P_{1.6r} = P_{1.6r} + \Delta P$ (add power level adjustment to reported power level).
b) The CNU shall report its transmit power using the variable *ReportedPwr* when requested by the CLT.

The value for $P_{1.6r}$ has the following limits:

— $P_{1.6r} \leq P_{1.6Max}$ (clip at max power limit).
— $P_{1.6r} \geq P_{1.6Min}$ (clip at min power limit per channel).

The CNU shall then transmit each data subcarrier with target power as calculated by Equation (100–9).

$$P_{t\_sc\_i} = P_{1.6r} + Pre\text{-}Eq_i - 10 \times \log_{10}(32) \quad (100–9)$$

where

$Pre\text{-}Eq_i$ is the magnitude of the ith subcarrier pre-equalizer coefficient (dB)

32 is the number of subcarriers in 1.6 MHz

That is, the reported power, normalized to 1.6 MHz, minus compensation for the pre-equalization for the subcarrier, less a factor taking into account the number of subcarriers in 1.6 MHz.

The CNU transmit power, P_t, in an upstream RB Frame is the sum of the individual transmit powers $P_{t\_sc\_i}$ of each subcarrier where the sum is performed using absolute power quantities in the non-dB domain.

The transmitted power level varies dynamically as the number and type of allocated subcarriers varies.

100.3.4.3.1 PHY Link managed variables

ReportedPwr

TYPE: 9-bit unsigned integer

This variable reports the CNU transmit power, in units of 0.25 dBmV, for the upstream OFDMA channel.

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100.3.4.4 OFDMA fidelity requirements

100.3.4.4.1 Spurious emissions

The noise and spurious power generated by the CNU shall not exceed the levels given in Table 100–7, Table 100–8, and Table 100–9. Up to five discrete spurs[173] can be excluded from the emissions requirements listed in Table 100–7, Table 100–8, and Table 100–9 and have to be less than –42 dBc relative to a single subcarrier power level.

The parameter *SpurFloor* is related to the ratio of the number of subcarriers being modulated by a CNU in an OFDMA symbol to the maximum number of subcarriers available (3840) including guard bands and is calculated in dBc per Equation (100–10).

$$SpurFloor = \max\{-57 + 10\times\log_{10}(N_{S\_Max}/3840), -60\} \quad (100–10)$$

where N_{S_Max} is the number of modulated subcarriers in an OFDMA symbol.

Maximum number of simultaneous transmitters is defined as shown in Equation (100–11).

$$N_{T\_Max} = \left\lfloor 0.2 + 10^{((-44 - SpurFloor)/10)} \right\rfloor \quad (100–11)$$

The parameter *Under-grant Subcarriers* (number of subcarriers) is defined as shown in Equation (100–12).

$$Under\text{-}grant\ Subcarriers = N_{S\_Max}/N_{T\_MAX} \quad (100–12)$$

When a CNU is transmitting with fewer subcarriers than the *Under-grant Subcarriers* the spurious emissions requirement limit is the power value (in dBmV), corresponding to the specifications for the power level associated with a grant number of subcarriers equal to *Under-grant Subcarriers*. In addition, when a CNU is transmitting such that the total power of the CNU, P_t, is less than 17 dBmV, but other requirements are met, then the CNU spurious emissions requirements limit is the power value (in dBmV) computed with all conditions and relaxations factored in, plus an amount X dB where:

$$X\ \text{dB} = 17\ \text{dBmV} - P_t$$

In Table 100–7, inband spurious emissions includes noise, carrier leakage, clock lines, synthesizer spurious products, and other undesired transmitter products. It does not include ISI. The *Measurement Bandwidth* for inband spurious for OFDM is equal to the Subcarrier Clock frequency (50 kHz) and is not a synchronous measurement. The signal reference power for OFDMA inband spurious emissions is the total transmit power measured and adjusted (if applicable), and then apportioned to a single active subcarrier (see Table 100–8 and Table 100–9).

The *Measurement Bandwidth* is 160 kHz for Between Bursts specifications of Table 100–6, except where called out as 4 MHz or 250 kHz.

The signal reference power for Between Bursts transmissions is the reported power as in 100.3.4.3.

The Transmitting Burst specifications apply during the transmission of Resource Blocks and for 20 µs before the first symbol of the OFDMA transmission and for 20 µs after the last symbol of an OFDMA transmission. The Between Bursts specifications apply except during transmission of Resource Blocks and for

[173]Discrete (narrowband) spurious emissions, such as a continuous wave (CW) sinusoid or other signal with significant power concentrated in small bandwidth.

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20 µs before the first symbol of the OFDMA transmission and for 20 µs after the last symbol of an OFDMA transmission. The signal reference power for Transmitting Burst transmissions, other than inband, is the total transmit power measured and adjusted (if applicable) as described in this subclause.

For the purpose of spurious emissions definitions, a burst refers to a burst of Resource Blocks to be transmitted at the same time from the same CNU.

For PHY Discover Ranging spurious emissions requirements use Table 100–7, Table 100–8, and Table 100–9, with *100% Grant Spectrum* equal to the bandwidth of the *modulated spectrum* of the transmission.

The spurious emissions requirements over the entire upstream spectrum given in Table 100–7 for transmission of $N_{S\_Max}/10$ or fewer subcarriers may be relaxed by 2 dB in an amount of spectrum equal to the following equation:

$$Measurement\ Bandwidth \times \lceil (100\%\ Grant\ Spectrum/10\ )/Measurement\ Bandwidth \rceil$$

where the *Measurement Bandwidth* value is defined in Table 100–8 and Table 100–9.

The 2 dB relaxation applies in the *Measurement Bandwidth*. This relaxation does not apply to between bursts emission requirements. The relaxation is added to the spurious emissions power limits calculated for the *Measurement Bandwidths* of Table 100–8 and Table 100–9 for *Measurement Bandwidth* values comprising roughly 10% of the upstream spectrum when the granted spectrum is less than 10% of the *100% Grant Spectrum*.

Table 100–7—Spurious emissions

Parameter	Transmitting	Between bursts
Inband	–45 dBc OFDMA 100% grant [a, b] –51 dBc OFDMA 5% grant [a, b]	N/S
Adjacent band	See Table 100–9	N/S
Within the upstream operating range 5 MHz to 204 MHz (excluding modulated spectrum and adjacent spectrum)	See Table 100–8	5 MHz to 20 MHz: –69 dBc[c] 20 MHz to 204 MHz: –72 dBc[c]
CNU integrated spurious emissions limits (all in 4 MHz, includes discrete spurs)[d]		
204 MHz to 258 MHz	–50 dBc	–72 dBc
258 MHz to 1218 MHz	–45 dBmV	max(–45 dBmV, –40 dB reference downstream)[d]
CNU discrete spurious emissions limits[e]		
204 MHz to 258 MHz	–50 dBc	–36 dBmV
258 MHz to 1218 MHz	–50 dBmV	–50 dBmV

[a]Up to five subcarriers within the entire upstream bandwidth with discrete spurs may be excluded from the MER calculation if they fall within transmitted bursts. These five spurs are the same spurs that may be excluded for spurious emissions and not an additional or different set.

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[b]Receive equalization is allowed if an MER test approach is used, to take ISI out of the measurement; measurements other than MER-based to find spurs or other unwanted power may be applied to this requirement.
[c]The signal reference power, 0 dBc, is the total transmit power defined in 100.3.4.4.1.
[d]"dB reference downstream" is relative to the received downstream signal level. Some spurious outputs are proportional to the receive signal level.
[e]These spec limits exclude a single discrete spur related to the tuned received channel; this single discrete spur is to be no greater than –40 dBmV.

100.3.4.4.2 Spurious emissions in the upstream frequency range

Table 100–8 lists the allowed spurious emissions for *Under-grant Hold Bandwidth* conditions. The initial measurement interval at which to start measuring the spurious emissions (from the transmitted burst's modulation edge) is 400 kHz from the edge of the transmission's modulation spectrum. Measurements should start at the initial distance and be repeated at increasing distance from the carrier until the upstream band edge or spectrum adjacent to other modulated spectrum is reached.

For OFDMA transmissions with non-zero transmit windowing, the CNU shall meet the required performance measured within the 2 MHz adjacent to the modulated spectrum using slicer values from a CLT burst receiver or equivalent, synchronized to the downstream transmission provided to the CNU.

In the remainder of the upstream spectrum, the CNU shall meet the required performance measured with a bandpass filter (e.g., an unsynchronized measurement).

For OFDMA transmissions with zero transmit windowing, CNU shall meet the required performance using synchronized measurements across the complete upstream spectrum.

The calculation for far out spurious emissions for specification in the interval values in Table 100–8 is shown in Equation (100–13).

$$\text{Round}(\textit{SpurFloor} + 10 \times \log_{10}(\textit{Measurement Bandwidth}/\textit{Under-grant Hold Bandwidth}) \quad (100\text{–}13)$$

The notation Round(x) as used in Equation (100–13), represents a rounding function that returns the value of its argument x rounded to the nearest 0.1.

The calculation for *SpurFloor* values in Table 100–8 and Table 100–9 is shown in Equation (100–14).

$$\textit{SpurFloor} = \max\{-57 + 10 \times \log_{10}(\textit{100\% Grant Spectrum}/192), -60\} \quad (100\text{–}14)$$

The calculation for *Under-grant Hold #Users* in Table 100–8 and Table 100–9 is shown in Equation (100–15).

$$\textit{Under-grant Hold \#Users} = \left\lfloor 0.2 + 10^{((-44 - \textit{SpurFloor})/10)} \right\rfloor \quad (100\text{–}15)$$

Grant Spectrum is the spectrum of the grant (number of Resource Blocks multiplied by the bandwidth of a single Resource Block) allocated to a CNU in a given upstream RB Frame (see 101.4.4.3.1). *Grant Spectrum* may vary from one RB Frame to another. *100% Grant Spectrum* is the bandwidth of the entire upstream transmission resource, which occurs with probes, that incorporate all Resource Blocks and unused subcarriers (see 101.4.4.3.1).

Under-grant Hold Bandwidth in Table 100–8 and Table 100–9 is shown in Equation (100–16).

$$\textit{Under-grant Hold Bandwidth} = \textit{100\% Grant Spectrum}/\textit{Under-grant Hold \#Users} \quad (100\text{–}16)$$

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For transmission bursts with modulation spectrum less than the *Under-grant Hold Bandwidth*, the spurious power requirement is calculated as in Equation (100–16), but increased by $10 \times \log_{10}$ (*Under-grant Hold Bandwidth*/*Grant Spectrum*).

Table 100–8—Spurious emissions requirements in the upstream frequency range for grants of Under-grant Hold Bandwidth and larger[a]

100% Grant Spectrum (MHz)	*SpurFloor* (dBc[b])	*Under-grant Hold #Users*	*Under-grant Hold Bandwidth* (MHz)	*Measurement Bandwidth* (MHz)[c]	Specification in the Interval (dBc[b])
Up to 64 [e.g., 22 MHz] (see note) [e.g., 46 MHz]	–60	40	100% Grant Spectrum/40 [0.55 MHz](see note) [1.15 MHz]	1.6	Eq (100–13) [–55.4](see note) [–58.6]
Greater than 64, up to 96 [e.g., 94 MHz]	–60	40	100% Grant Spectrum/40 [2.35 MHz]	3.2	Eq (100–13) [–58.7]
Greater than 96, up to 192 [e.g., 142 MHz] [e.g., 190 MHz]	Eq (100–14) [–58.3] [–57]	Eq (100–15) [27] [20]	Eq (100–16) [5.3] [9.5]	9.6	Eq (100–13) [–55.47 [–57]
Greater than 192 [e.g., 200 MHz]	Eq (100–14) [–56.8]	Eq (100–15) [19]	Eq (100–16) [10.5]	12.8	Eq (100–13) [–58.7]
NOTE— Each row of bracketed values represent a set of calculated examples. The value in the first column is an example value for 100% Grant Spectrum (MHz). The remaining columns are the result of the calculations for that column.					

[a]Spurious emissions requirements in the upstream frequency range relative to the per channel transmitted burst power level for each channel for grants of *Under-grant Hold Bandwidth* and larger.
[b]The signal reference power, 0 dBc, is the total transmit power defined in 100.3.4.4.1.
[c]The *Measurement Bandwidth* is a contiguous sliding measurement window.

The CNU shall control transmissions such that (within the *Measurement Bandwidth* of Table 100–8) spurious emissions measured for individual subcarriers contain no more than +3 dB power larger than the required average power of the spurious emissions in the full *Measurement Bandwidth*. When non synchronous measurements are made, only 25 kHz *Measurement Bandwidth* is used.

100.3.4.4.3 Adjacent channel spurious emissions

Table 100–9 lists the required adjacent channel spurious emission levels when there is a transmitted burst with bandwidth at the *Under-grant Hold Bandwidth*. The measurement is performed in an adjacent channel interval of 400 kHz adjacent to the transmitted burst modulation spectrum. For OFDMA transmissions, the measurement is performed starting on an adjacent subcarrier of the transmitted spectrum (both above and below), using the slicer values from a CLT burst receiver or equivalent synchronized to the downstream transmission provided to the CNU.

Note that the *Measurement Bandwidth* for Table 100–9 is less than the *Measurement Bandwidth* values in Table 100–8. Thus comparing the two tables in terms of the specification "dBc" values requires appropriate scaling. Table 100–9 provides specification "dBc" only for grants of a specific amount for each row, while Table 100–8 provides "dBc" specification for grants of all sizes from the *Under-grant Hold Bandwidth* to 100%.

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For transmission bursts with the *Grant Spectrum* less than the *Under-grant Hold Bandwidth*, the spurious power requirement is calculated as above, but increased by $10 \times \log_{10}$ (*Under-grant Hold Bandwidth*/*Grant Spectrum*).

For transmission bursts with modulation spectrum greater than the *Under-grant Hold Bandwidth*, the spurious power requirement in the adjacent 400 kHz is calculated by converting the requirement to absolute power "dBmV" for a grant of precisely *Under-grant Hold Bandwidth* from Table 100–9, and similarly computing the absolute power "dBmV" from Table 100–8 for a grant equal to the following:

Grant Spectrum – Under-grant Hold Bandwidth

Then the absolute power calculated from Table 100–8 is scaled back in exact proportion of 400 kHz compared to the *Measurement Bandwidth* in Table 100–8. Then the power from Table 100–9 is added to the scaled apportioned power from Table 100–8 to produce the requirement for the adjacent 400 kHz measurement with a larger grant than the *Under-grant Hold Bandwidth*. The requirement for adjacent spurious power in adjacent 400 kHz is as follows:

P1 (*Grant Spectrum-Under-grant Hold Bandwidth*) = absolute power derived from Table 100–8 dBmV

P2 (*Under-grant Hold Bandwidth*) = absolute power derived from Table 100–9 dBmV

$P1_{scaled} = P1 \times (0.4)/($*Measurement Bandwidth* used in Table 100–8) dBmV

$P_{spec\_limit} = P1_{scaled} + P2$ dBmV

Equation (100–17) is used in Table 100–9 for calculating the table column: "Specification in Adjacent 400 kHz with Grant of *Under-grant Hold Bandwidth* (dBc)."

$$\text{Round}(10 \times \log_{10}((10^{(SpurFloor/10)} + (10^{(-57/10)})) \times (0.4/\textit{Under-grant Hold Bandwidth}))) \quad (100–17)$$

The notation Round(x) as used in Equation (100–17), represents a rounding function that returns the value of its argument x rounded to the nearest 0.1.

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Table 100–9—Adjacent channel spurious emissions requirements relative to the per channel transmitted burst power level for each channel

100% Grant Spectrum (MHz)	*SpurFloor* (dBc[a])	*Under-grant Hold #Users*	*Under-grant Hold Bandwidth* (MHz)	*Measurement Bandwidth* (MHz)	Specification in Adjacent 400 kHz with Grant of *Under-grant Hold Bandwidth* (dBc[a])
Up to 64 [e.g., 22 MHz](see note) [e.g,: 46 MHz]	–60	40	100% Grant Spectrum/40 [0.55 MHz](see note) [1.15 MHz]	0.4 MHz	Eq (100–17) [–56.6](see note) [–59.8]
Greater than 64, up to 96 [e.g., 94 MHz]	–60	40	100% Grant Spectrum/40 [2.35 MHz]	0.4 MHz	Eq (100–17) [–62.9]
Greater than 96 [e.g., 142 MHz] [e.g., 190 MHz] [e.g., 200 MHz]	Eq (100–14) Round nearest 0.1 dB [–58.3] [–57] [–56.8]	Eq (100–15) [27] [20] [19]	Eq (100–16) [5.3] [9.5] [10.5]	0.4 MHz	Eq (100–17) [–65.8] [–67.7] [–68.1]
NOTE—Each row of bracketed values represent a set of calculated examples. The value in the first column is an example value for 100% Grant Spectrum (MHz). The remaining columns are the result of the calculations for that column.					

[a]The signal reference power, 0 dBc, is the total transmit power defined in 100.3.4.4.1.

100.3.4.4.4 Spurious emissions during burst on/off transients

The CNU shall control spurious emissions prior to and during RF power amplifier turn on, during and following turn off, and before and after a burst. See 100.3.4.7.

The CNU's on/off spurious emissions, such as the change in voltage at the upstream transmitter output, due to enabling or disabling transmission, shall be no more than 50 mV.

The CNU's voltage step at the MDI (TP2, see 100.4) shall be dissipated no faster than 4 μs of constant slewing when the CNU is transmitting at +55 dBmV or more.

At transmit levels below +55 dBmV, the CNU's maximum change in voltage shall decrease by a factor of 2 for each 6 dB decrease of power level, from +55 dBmV down to a maximum change of 3.5 mV at 31 dBmV and below. The amplifier turn on and turn off transients of this subclause (100.3.4.4.4) are not applicable when the entire CNU is being powered on or off.

100.3.4.5 Transmit MER requirements

Transmit MER measures the cluster variance caused by the CNU during upstream transmission due to transmitter imperfections. The terms "equalized MER" and "unequalized MER" refer to a measurement with linear distortions equalized or not equalized, respectively, by the test equipment receive equalizer. The requirements in this subclause refer only to unequalized MER, as described for each requirement. MER is

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measured on each modulated data subcarrier and pilot (MER is computed based on the pilot power) in a Resource Block of a burst and averaged for all the subcarriers in each Resource Block. MER includes the effects of Inter-Carrier Interference, spurious emissions, phase noise, noise, distortion, and all other undesired transmitter degradations with an exception for a select number of discrete spurs impacting a select number of subcarriers. Compliance with MER requirements is verified with the use of a calibrated test instrument that synchronizes to the OFDMA signal, applies a receive equalizer in the test instrument that removes MER contributions from nominal channel imperfections related to the measurement equipment, and calculates the value. The equalizer in the test instrument is calculated, applied and frozen for the CNU testing. Receiver equalization of CNU linear distortion is not provided; hence this is considered to be a measurement of unequalized MER, even though the test equipment contains a fixed equalizer setting.

100.3.4.5.1 Definitions

The transmitted RF waveform at the F connector of the CNU (after appropriate down conversion) is filtered, converted to baseband, sampled, and processed using standard OFDMA receiver methods, with the exception that receiver equalization is not provided. The processed values are used in Equation (100–18) and Equation (100–19). No external noise (AWGN) is added to the signal.

The carrier frequency offset, carrier amplitude, carrier phase offset, and timing are adjusted during each burst to maximize MER as follows:

a) One carrier amplitude adjustment common for all subcarriers and OFDM symbols in burst.
b) One carrier frequency offset common for all subcarriers resulting in phase offset ramping across OFDM symbols in bursts.
c) One timing adjustment resulting in phase ramp across subcarriers.
d) One carrier phase offset common to all subcarriers per OFDM symbol in addition to the phase ramp.

MER per Resource Block (RB_{MER} in dB) is computed as shown in Equation (100–18).

$$RB_{MER} = 10 \times \log_{10}\left(\frac{E_{avg}}{\left(\frac{1}{RBlen}\left(\sum_{k=1}^{RBlen} |e_{j,k}|^2\right)\right)}\right) \quad (100–18)$$

where

E_{avg} is the average constellation energy for equally likely symbols
$RBlen$ is a value of 8 when *RBsize* is FALSE and a value of 16 when *RBsize* is TRUE
$e_{j,k}$ is the error vector from the *j*th subcarrier in the burst and *k*th received symbol to the ideal transmitted QAM symbol of the appropriate modulation order

MER per burst ($BURST_{MER}$ in dB) is computed as shown in Equation (100–19).

$$BURST_{MER} = \frac{1}{N}\sum_{j=1}^{N} (RB_{MER}\, j) \quad (100–19)$$

where

j is the *j*th subbcarrier in the burst
E_{avg} is the average constellation energy for equally likely symbols
N is the number of Resource Blocks in a burst

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A sufficient number of OFDMA symbols should be included in the time average so that the measurement uncertainty from the number of symbols is less than other limitations of the test equipment.

MER with a 100% grant is defined as the condition when all OFDMA subcarriers are granted to the CNU.

MER with a 5% grant is defined as the condition when less than or equal to 5% of the available OFDMA subcarriers have been granted to the CNU.

100.3.4.5.2 Requirements

Unless otherwise stated, the CNU shall meet or exceed the following MER limits in Table 100–10 over the full transmit power range, all modulation orders, all grant configurations and over the full upstream frequency range.

The measurements indicated in Table 100–10 are made with flat channel (as nearly flat as practical in a laboratory test environment), after the pre-equalization coefficients have been set to their optimum values. The receiver uses best effort synchronization to optimize the MER measurement.

Table 100–10—Upstream MER requirements (with pre-equalization)

Parameter	Value	Units
MER (100% grant), each burst	≥ 44[a]	dB
MER (5% grant), each burst	≥ 50[a]	dB
Pre-equalizer constraints	Pre-equalization not used	

[a]Up to five subcarriers within the entire upstream bandwidth with discrete spurs may be excluded from the MER calculation if they fall within transmitted bursts. These five spurs are the same spurs that may be excluded for spurious emissions and not an additional or different set.

100.3.4.6 CNU Transmitter output requirements

The CNU shall output an RF Modulated signal with characteristics defined in Table 100–11.

Table 100–11—CNU RF output requirements

Parameter	Value	Units
Frequency band Equipment may be adapted to all or part of this frequency band to suit regional requirements. See 100.5.4.1.2.	7.4 to 204	MHz
OFDMA channel bandwidth	10 to 192	MHz
Subcarrier channel spacing	50	kHz
OFDM symbol rate FFT duration	20	µs
FFT size	4096	FFT bins
Maximum number of data subcarriers	3800	subcarriers
Total average transmit output power	up to 65	dBmV
Modulation format	See Table 100–2	

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Table 100–11—CNU RF output requirements *(continued)*

Parameter	Value	Units
R_{on} max (see 100.3.4.7)	100	μs
R_{off} max (see 100.3.4.7)	100	μs
Output impedance	75	Ω
Output return loss 7.4 MHz to f_{max} MHz (42/65/85/117/204 MHz)	> 6	dB
MDI Connector	F connector per ISO/IEC 61169-24 or SCTE 02	

100.3.4.7 CNU RF power amplifier requirements

In EPoC, the upstream CNU PMD RF power amplifier (PA) may be turned off between bursts as shown in Figure 100–3. PMD_SIGNAL.request(ON) is asserted when the first bit of the burst is conveyed from the PCS to the PMA via PMA_UNITDATA.request() (see 101.4.2.1). The delay time through the EPoC PMA (T_{PMA}) is no less than the sum of the *RBframe* size multiplied by the OFDM symbol time *RBlen*(*RBsize)* of 8 times or 16 times 20 μs, see 100.3.4.1) plus the implementation specific processing time of the IDFT (nominal range 10 μs to 40 μs). For any given implementation and upstream profile configuration, T_{PMA} is fixed and the CNU is required to meet the PMD delay variance requirements in 100.2.2. The time to turn on and stabilize the PA for meeting burst transmission fidelity requirements (see 100.3.4.2) is represented by R_{on}. The time from PMD_SIGNAL.request(ON) to initiate PA turn on is implementation specific. PMD_SIGNAL.request(OFF) is asserted when the last bit of the burst is conveyed from the PCS to the PMA. PA turn off is initiated after the T_{PMA} delay and after the last OFDM symbol of the burst. The time for the PA to turn off is represented by R_{off}.

The RF transmission of burst energy begins at the beginning of the grant after R_{on}. The R_{on} time period of one CNU may overlap completely with the R_{off} time period of another CNU. Turning the PA off achieves two purposes: to meet the energy efficiency requirements of 100.6 and to minimize the cumulative impact on CLT receiver SNR by avoiding all CNU PAs powered on 100% of the time.

R_{on} and R_{off} times are not included in burst overhead calculations (see 103.3.5). T_{PMA} in either *RBsize* configuration is longer than R_{on} maximum (see Table 100–11) and does not impact adjusting grant lead time (see 103.3.5).

The CNU shall disable transmitter output when *PD_Enable* is equal to FALSE and continue in normal transmitter operation when *PD_Enable* is equal to TRUE. This requirement has precedence over the requirements in this subclause.

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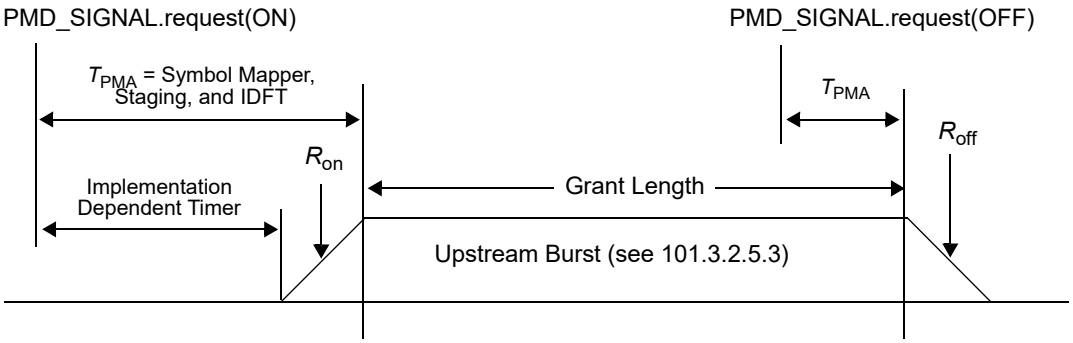

Figure 100–3—Details of RF power amplifier turn on and turn off timing

100.3.5 CLT receiver requirements

100.3.5.1 CLT receiver input power requirements

The CLT Upstream Demodulator shall operate with an average input signal level, including ingress and noise to the upstream demodulator, up to 31 dBmV. Operation above this level is not specified.

The CLT shall be configured according to Table 100–12 for intended received power normalized to 6.4 MHz of bandwidth.

When using the modulation formats and power set points shown, the CLT upstream demodulator shall operate within its defined performance specifications when received bursts are within the ranges specified in Table 100–12.

Table 100–12—Upstream OFDMA channel demodulator input power characteristics

Modulation	Minimum set point[a] (dBmV)	Maximum set point[a] (dBmV)	Range (dB)
QPSK	–4	10	–9 to +3
8-QAM	–4	10	–9 to +3
16-QAM	–4	10	–9 to +3
32-QAM	–4	10	–9 to +3
64-QAM	–4	10	–9 to +3
128-QAM	0	10	–9 to +3
256-QAM	0	10	–9 to +3
512-QAM	0	10	–3 to +3
1024-QAM	0	10	–3 to +3
2048-QAM	7	10	–3 to +3
4096-QAM	10	10	–3 to +3

[a]With respect to 6.4 MHz.

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The CLT shall provide upstream power measurements with a standard deviation of 0.33 dB or better under the test conditions given in 100.4.3.

100.3.5.1.1 PHY Link managed variables

CLT_TargetReceivePower

TYPE: signed 10-bit integer

This variable specifies the CLT receive power, in units of 0.1 dBmV/6.4 MHz. The value is set according to the requirements in Table 100–12.

100.3.5.2 CLT receiver error performance in AWGN channel

This subclause describes the conditions at which the CLT PMD when connected to a compliant PMA and PCS is required to meet the error performance in an AWGN channel.

The CLT shall achieve a received frame loss ratio of less than or equal to 10^{-6} when all of the following input load and channel conditions are met:

- A single transmitter, pre-equalized and ranged.
- A single OFDMA 192 MHz channel, using all 3800 subcarriers.
- Ranging with same CNR and input level to CLT as with data bursts, and with 6-symbol probes.
- Any valid transmit combination (frequency, transmit window, cyclic prefix, upstream OFDMA Superframe length, Resource Block size pilot patterns, etc.) as defined in this specification.
- Input power level per constellation is the minimum set point as defined in Table 100–12.
- Received signal having a CNR greater than or equal to that shown in Table 100–13.
- OFDMA phase noise and frequency offset are at the max limits as defined for the CLT transmission specification.
- Ideal AWGN channel with no other artifacts (reflections, burst noise, tilt, etc.).
- Large bursts consisting of frames of any allowed sizes, including bursts consisting only of minimum size frames (4A.2.3.2.4) and bursts consisting only of maximum size frames (4A.2.4.2).

Table 100–13—CLT minimum CNR performance in AWGN channel

Modulation	CNR[a,b] (dB)	Set point[c] (dBmV)	Offset (dB)
QPSK	11	–4	0
8-QAM	14	–4	0
16-QAM	17	–4	0
32-QAM	20	–4	0
64-QAM	23	–4	0
128-QAM	26	0	0
256-QAM	29	0	0
512-QAM	32.5	0	0
1024-QAM	35.5	0	0

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Table 100–13—CLT minimum CNR performance in AWGN channel *(continued)*

Modulation	CNR[a,b] (dB)	Set point[c] (dBmV)	Offset (dB)
2048-QAM	39	7	0
4096-QAM	43	10	0

[a]CNR is defined here as the ratio of average signal power in occupied spectrum to the average noise power in the occupied spectrum given by the noise power spectral density integrated over the same occupied spectrum.
[b]Channel CNR is adjusted to the required level by measuring the source inband noise including phase noise component and adding the required delta noise from an external AWGN generator.
[c] With respect to 6.4 MHz.

100.3.5.3 CLT upstream receive modulation error ratio requirements

This subclause provides measurements of the upstream receive modulation error ratio (RxMER) for each subcarrier. The CLT measures the RxMER using an upstream probe. For the purposes of RxMER measurement at the CLT, RxMER is defined as the ratio of the average power of the ideal BPSK constellation to the average error-vector power. The error vector is the difference between the equalized received probe value and the known correct probe value.

The CLT shall be capable of providing measurements of RxMER for all active subcarriers for any single specified CNU in the upstream OFDMA channel, using probe symbols. The CLT can use a sufficient number of upstream probe symbols for a reliable estimate of RxMER.

100.3.5.3.1 PHY Link managed variables

RxMER_ChID
: TYPE: 3-bit integer
This variable is a pointer to one of the five possible OFDM channels in the EPoC network. When set in the CNU the values in *RxMER_SC(n)* reflect the measurements of OFDM channel number *RxMER_ChID* when *RxMER_Valid* goes TRUE. In the CNU this register may have a value of between 1 and 5 inclusive. In the CLT this variable is read only and will always have a value of one.

RxMER_CNU_ID
: TYPE: unsigned 14-bit integer
This variable identifies for the CLT the CNU for which the CLT is to measure the upstream RxMER. When set in the CLT the values in *RxMER_SC(n)* reflect the measurements of the CNU whose *CNU_ID* matches *RxMER_CNU_ID* when *RxMER_Valid* goes TRUE. In the CNU this variable is read only and will always have a value of one.

RxMER_SC(n)
: TYPE: array of 8-bit unsigned integer
This variable represents the measured receive modulation error ratio (RxMER) for subcarrier index *n* for an OFDM channel in increments of 0.25 dB with a value range from 0 dB (0x00) to 63.5 dB (0xFE). Subcarriers (such as exclusion bands) that cannot be measured indicate a value of 0xFF. The default (initial) value of RxMER is 0xFF for all subcarriers.

RxMER_Valid
: TYPE: Boolean
When TRUE this variable indicates that the values *RxMER_SC(n)* for the CNU indicated by *RxMER_CNU_ID* for the OFDM channel indicated by *RxMER_ChID* are valid. When FALSE this variable indicates the some values in *RxMER_SC(n)* may be invalid.

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100.3.6 CNU receiver requirements

100.3.6.1 Input signal characteristics at CNU receiver

The CNU shall meet electrical parameters and all performance specifications when receiving a signal conformant to the parameters shown in Table 100-14.

Table 100–14—Electrical input to CNU

Parameter	Value	Units
Total input power, 54 MHz to 1.794 GHz	< 40	dBmV
OFDM channel input level range (24 MHz min occupied spectrum) Note that level range does not imply anything about BER performance or capability vs. QAM. CNU BER performance is separately described.	–9 to +21	dBmV/24 MHz
Maximum average power per MHz input to the CNU from 54 MHz to 1.794 GHz For additional Demodulated Bandwidth, B_{demod} :[a] For additional Non-Demodulated Bandwidth, $B_{no\text{-}demod}$[b] and for up to 12 MHz of occupied spectrum (analog, out of band (OOB), QAM, OFDM): For all remaining spectrum:[c]	 ≤ Min [$X - 10\times\log_{10}(24) + 10$; $21 - 10\times\log_{10}(24)$] ≤ Min [$X - 10\times\log_{10}(24) + 10$; $26 - 10\times\log_{10}(24)$] ≤ Min [$X - 10\times\log_{10}(24) + 10$; $21 - 10\times\log_{10}(24)$] where X = Average power of lowest power 24 MHz of modulated spectrum for demodulation	dBmV/MHz
Input impedance	75	Ω
Input return loss 258 MHz to 1218 MHz	> 6	dB

[a]Additional Demodulated Bandwidth represented by B_{demod} is any 1 MHz of spectrum defined by the downstream profile (see 101.4.2) for the CNU that is outside the 24 MHz of the downstream profile that has the lowest average power.
[b]Additional Non-Demodulated Bandwidth represented by $B_{no\text{-}demod}$ is any 1 MHz of spectrum outside the downstream profile (101.4.2) see for the CNU.
[c]Remaining bandwidth in 54 MHz to 1.794 GHz, excluding both the Additional Demodulated Bandwidth and the Additional Non-Demodulated Bandwidth.

100.3.6.2 CNU error performance in AWGN channel

This subclause describes the conditions at which the CNU PMD when connected to a compliant PMA and PCS is required to meet the error performance in an AWGN channel.

The CNU shall achieve a received frame loss ratio of less than or equal to 10^{-6} under the following input load and channel conditions:

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— Any valid transmit combination (frequency, Subcarrier Clock frequency, transmit window, cyclic prefix, pilot, PHY Link, subcarrier exclusions, interleaving depth, modulation profile configuration, etc.) as defined in this standard.

— P_{6AVG} (the measured OFDM channel power divided by number of occupied 6 MHz channels) ≤ 15 dBmV.

— Up to fully loaded spectrum. Note that the frame loss ratio requirements are levied on all active OFDM channels. Those requirements are to be met with a single channel operating in isolation and up to and including all of the other OFDM channels being operated. This is what is meant by "Up to fully loaded spectrum".

— Power in (both above and below) four adjacent 6 MHz channels ≤ P_{6AVG} + 3 dB.

— Power in any 6 MHz channel over the modulated spectrum ≤ P_{6AVG} + 6 dB.

— Peak envelope power in any analog channel over the modulated spectrum ≤ P_{6AVG} + 6 dB.

— Average power per channel across modulated spectrum ≤ P_{6AVG} + 3 dB.

— Received signal having a CNR greater than or equal to that shown in Table 100–15.

— OFDM channel phase noise as per Table 100–3 and Table 100–6.

— Large bursts consisting of frames of any allowed sizes, including bursts consisting only of minimum size frames (4A.2.3.2.4) and bursts consisting only of maximum size frames (4A.2.4.2).

— No other artifacts (reflections, burst noise, tilt, etc.).

Table 100–15—CNU minimum CNR performance in AWGN channel

Constellation	CNR[a] (dB) Up to 1 GHz	CNR[a] (dB) 1 GHz to 1.2 GHz	Min P_{6AVG} dBmV
4096	41	41.5	–6
2048	37	37.5	–9
1024	34	34	–12
512	30.5	30.5	–12
256	27	27	–15
128	24	24	–15
64	21	21	–15
16	15	15	–15

[a]CNR is defined here as total signal power in occupied spectrum divided by total noise in occupied spectrum. OFDM channel CNR is adjusted to the required level by measuring the source inband noise including phase noise component and adding the required delta noise from an external AWGN generator. Applicable to an OFDM channel with 192 MHz of occupied spectrum.

100.3.6.3 Receive modulation error ratio requirements

The CNU provides measurements of downstream receive modulation error ratio (RxMER) for all active subcarrier locations for each OFDM downstream channel, using pilots and PHY Link preamble symbols.

The CNU measures the RxMER using scattered pilots and PHY Link preamble symbols. Note that if a scattered pilot falls on top of a continuous pilot, it is still considered as a scattered pilot for these measurements. For the purposes of RxMER measurement at the CNU, RxMER is defined as the ratio of the average power of the ideal QAM constellation to the average error-vector power. The error vector is the difference between the equalized received pilot or preamble value and the known correct pilot value or preamble value. As a defining test case, for an ideal AWGN channel, an OFDM channel containing a mix of QAM constellations, with data-subcarrier CNR = 35 dB CNR on the QAM subcarriers, yielding an RxMER measurement of nominally 35 dB averaged over all subcarrier locations. If some subcarriers (such as exclusion bands) cannot

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be measured by the CNU, the CNU indicates that condition in the measurement data for those subcarriers as a value of 0xFF.

RxMER may be more clearly defined in mathematical notation in accordance with Figure 100–4, which shows an ideal transmit and receive model, with no intent to imply an implementation. Let *p* represent the pilot or PHY Link preamble symbol before transmit IDFT, *H* represents the channel coefficient for a given subcarrier frequency, *n* represents noise, and *y* is the unequalized received symbol after receive FFT:

$$y = (H \times p) + n$$

The receiver computes *G* as an estimate of *H*, and computes the equalized received symbol *r* as follows:

$$r = y / G$$

Using the known modulation value of the pilot or preamble symbol *p*, the receiver computes the equalized error vector *e* as follows:

$$e = r - p$$

All the above quantities are complex numbers for a given subcarrier. To compute RxMER, the receiver computes *E* as the time average of $|e|^2$ (squared absolute value) over many visits of the pilot to the given subcarrier (or PHY Link preamble symbol as applicable), and $E\_dB = 10 \times \log_{10}(E)$. Let *S_dB* be the average power of the ideal QAM data subcarrier constellation (not including pilots) expressed in dB. The CNU reports *RxMER_dB* = *S_dB* – *E_dB*.

The CNU shall provide RxMER measurements with *RxMER_std* ≤ 0.5 dB under conditions specified in 100.4.2.

Define *delta_RxMER* = (*RxMER_mean* at CNR_data_subcarrier = 35 dB) – (*RxMER_mean* at CNR_data_-subcarrier = 30 dB). The CNU shall provide RxMER measurements such that 4 dB ≤ *delta_RxMER* ≤ 6 dB under the above specified condition.

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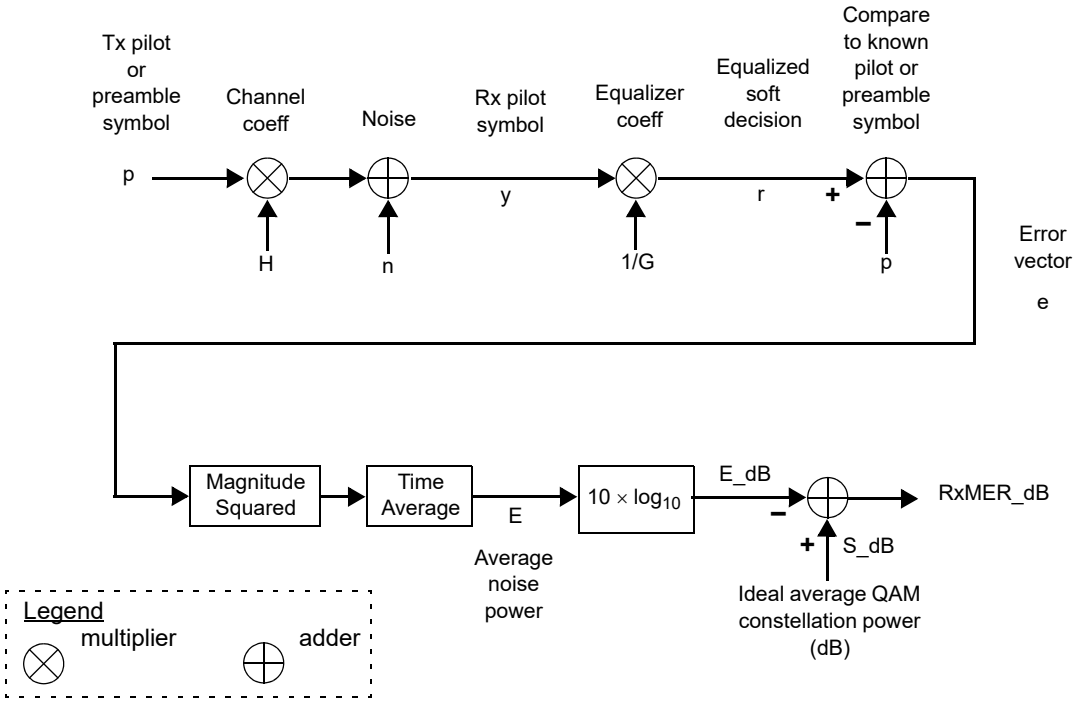

Figure 100–4—Computation of received modulation error ratio (RxMER) for a given subcarrier

100.3.7 Channel band rules

During OFDM and OFDMA channel planning, the following rules are to be observed to ensure proper operation of the CLT and CNU.

100.3.7.1 Downstream channel bandwidth rules

The encompassed spectrum of each 192 MHz downstream OFDM channel cannot exceed 190 MHz and does not exceed 3800 active subcarriers (see Table 100–3). The CLT uses the subcarriers in the range specified for IDFT Equation (101–25).

At least 1 MHz of exclusion band between the spectral edge any non-OFDM channel and the center frequency of the nearest OFDM subcarrier is required. This non-OFDM channel may be external to the OFDM channel or may be embedded within the OFDM channel.

100.3.7.2 Downstream exclusion band rules

The downstream exclusion band rules listed below apply to each OFDM channel and the composite downstream channel inclusive of OFDM and other signals using downstream spectrum concurrently with EPoC, e.g., video channels. The CLT and CNU are not expected to meet performance and fidelity requirements when the system configuration does not comply with the following downstream exclusion band rules:

— There has to be at least one contiguous modulated OFDM bandwidth of 22 MHz or greater.
— Exclusion bands may separate contiguous modulation bands.
— All contiguous modulation bands are to be 2 MHz or greater.

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— The only exception to the above is for exclusion bands that are allowed to occupy 405.925 MHz to 406.176 MHz in alignment with FCC regulations as per CFR 76. Unique FCC egress requirements exist for these bands separate from the general exclusion bands requirements.
— Exclusion bands plus individually excluded subcarriers are limited to 20% or less of the encompassed spectrum of any individual OFDM channel and modulated spectrum is to be at least 80% of the encompassed spectrum of all active channels.
— The number of individually excluded subcarriers is limited by the following:
  — The total spectrum of individually excluded subcarriers cannot exceed 5% of any contiguous modulation spectrum.
  — The total spectrum of individually excluded subcarriers cannot exceed 5% of a 6 MHz moving window across the contiguous modulation spectrum.
  — The total spectrum of individually excluded subcarriers cannot exceed 20% of a 1 MHz moving window across the contiguous modulation spectrum.
— The 6 MHz of contiguous spectrum used for the PHY Link cannot have any exclusion bands or excluded subcarriers.

100.3.7.3 Upstream channel bandwidth rules

The encompassed spectrum of the upstream OFDMA channel cannot exceed 190 MHz and does not exceed 3800 active subcarriers (see Table 100–11). The CLT uses the subcarriers in the range specified for IDFT Equation (101–25).

100.3.7.4 Upstream exclusions and unused subcarriers rules

The CLT and CNU are not expected to meet performance and fidelity requirements when the system configuration does not comply with the following downstream exclusion band rules:

— Subcarriers that lie outside the Encompassed Spectrum are excluded.
— Upstream exclusion bands may include one or more subcarriers.
— There is no restriction on the number or placement of excluded and unused subcarriers between Resource Blocks (see 101.4.4.3.1).

100.4 Test requirements and measurement methods

All testing and measurement is performed in a coax cable distribution network that conforms to Annex 100A. The test point for the CLT is located at the MDI and labeled TP1 as shown in Figure 101–1 and Figure 101–4. The test point for the CNU is located at the MDI and labeled TP2 as shown in Figure 101–2 and Figure 101–3.

100.4.1 CLT RF output muting requirement

The specified limit of 73 dB below the operationally configured aggregate power (see *CLT_TxMute* below and Table 100–3) applies with all active OFDM channels commanded to the same transmit power level. Starting with all channels commanded to the same power level, then commanding a reduction in the transmit level of any, or all but one, of the active OFDM channels does not change the specified limit for measured muted power in 6 MHz. The output return loss at TP1/MDI of the muted device complies with the Output Return Loss requirements for inactive OFDM channels given in Table 100–3.

CLT_TxMute
TYPE: Boolean
When this variable is set to TRUE the CLT sets the RF output power = 73 dBc (see Table 100–3)

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below the operationally configured aggregate power of the RF modulated signal, in every 6 MHz channel from 258 MHz to 1218 MHz. When set to FALSE the CLT is in its normal operating state.

100.4.2 CNU receive modulation error ratio testing

Performance requirements for downstream RxMER measurements are defined under the following list of specified conditions:

- Channel loading consists of a single OFDM channel with no other signals.
- The OFDM channel being measured has a fixed configuration with a 192 MHz channel bandwidth with 190 MHz modulated spectrum and no excluded subcarriers other than at band edges.
- The channel is flat without impairments other than AWGN.
- AWGN level is set to two values giving data-subcarrier CNR = 30 dB and 35 dB at the MDI (F connector) of the CNU across all data subcarriers in the OFDM channel.
- Signal level is fixed at a nominal receive level of 6 dBmV per 6 MHz.
- A minimum warm-up time of 30 min occurs before measurements are made.
- Each measurement consists of the frequency average across all subcarriers of the reported time-averaged individual subcarrier RxMER values as defined above. Frequency averaging is performed by external computation.
- An ensemble of M frequency-averaged RxMER measurements (M large enough for reliable statistics, i.e., such that the result lies within a given confidence interval) are taken in succession (e.g., over a period of up to 10 min) at both CNR values. The mean, *RxMER_mean* in dB, and standard deviation, *RxMER_std* in dB, are computed over the M measurements at both CNR values. The statistical computations are performed directly on the dB values.

The CNU shall provide RxMER measurements with *RxMER_std* ≤ 0.5 dB under the specified conditions in the previous list.

Define *delta_RxMER* = (*RxMER_mean* at CNR_data_subcarrier = 35 dB) – (*RxMER_mean* at CNR_data_subcarrier = 30 dB). The CNU shall provide RxMER measurements such that 4 dB ≤ *delta_RxMER* ≤ 6 dB under the above specified condition.

100.4.3 Upstream channel power

The purpose of the upstream OFDMA channel power metric is to provide an estimate of the total received power at the F connector input of the CLT (see “TP1 / MDI” Figure 101–4) for a single specified upstream CNU. The measurement is based on upstream probes. While digital power measurements are inherently accurate, the measurement referred to the analog input depends on available calibration accuracy.

NOTE—It is recommended that the CLT provide configurable averaging over a range at least including 1 to 32 probes.

The CLT provides upstream power measurements with a standard deviation of 0.33 dB or better under the following test conditions:

- Center frequency is fixed.
- Probe being measured has a fixed configuration containing at least 256 active subcarriers.
- Channel is without impairments other than AWGN at 25 dB CNR.
- Signal level is fixed at a value within ± 6 dB relative to a nominal receive level of 0 dBmV.
- A minimum warm up time of 5 min occurs before power measurements are made.
- Averaging is set to $N = 8$ probes per measurement.
- M measurements (M large enough for reliable statistics) are taken in succession (e.g,. over a period of up to 10 min). The standard deviation is computed over the M measurements, where each measurement is the average of N probes.

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100.4.3.1 PHY Link managed variables

RxPwr

TYPE: 9-bit signed integer
This variable is used to report the received power for the CNU indicated by *RxPwr_CNU_ID* in units of 0.1 dBmV.

RxPwr_CNU_ID

TYPE: 14-bit integer
When set to a CNU_ID this variable indicates which CNU is to be measured for receive power reporting using *RxPwr*.

RxPwrValid

TYPE: Boolean
When TRUE this flag indicates that the value of *RxPwr* is valid for the CNU indicated by *RxPwr_CNU_ID*. Any write to *RxPwr_CNU_ID* sets this variable to FALSE.

100.4.4 Guidelines for verifying compliance with downstream phase noise requirements

The CLT transmitted signal for each OFDM channel shall meet the test phase noise requirements as per Table 100–16. These are transmitter requirements only.

Table 100–16—Downstream phase noise test requirements

Parameter	Value	Units
Phase noise, integrated double sided maximum, full power CW signal 1002 MHz or lower:		
1 kHz to 10 kHz	–48	dBc
10 kHz to 100 kHz	–56	dBc
100 kHz to 1 MHz	–60	dBc
1 MHz to 10 MHz	–54	dBc
10 MHz to 100 MHz	–60	dBc
Full power 192 MHz OFDM channel block with 6 MHz in center as internal exclusion subband + 0 dBc CW signal in center, with block not extending beyond 1002 MHz.		
1 kHz to 10 kHz	–48	dBc
10 kHz to 100 kHz	–56	dBc
Full power 192 MHz OFDM channel block with 24 MHz in center as internal exclusion subband + 0 dBc CW signal in center, with block not extending beyond 1002 MHz.		
100 kHz to 1 MHz	–60	dBc
Full power 192 MHz OFDM channel block with 30 MHz in center as internal exclusion subband + 7 dBc CW signal in center, with block not extending beyond 1002 MHz.		
1 MHz to 10 MHz	–53	dBc

A CW signal can be generated via an FFT, where the CW signal is constructed as a continuous pilot selected to be on a subcarrier in proper coordination with the cyclic prefix; so there are no phase glitches on the

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subcarrier in transitioning from one OFDM symbol to another. In this configuration the EPoC OFDM continuous pilot is in fact phase continuous in the time domain; in general the continuous pilots are not phase continuous in the time domain. Continuous pilot means that subcarrier is continuously used as a pilot and in general does not mean that the phase is continuous. Placing a continuous pilot using a subcarrier where the continuous pilot does in fact have continuous phase in the time domain serves as the CW signal in the phase noise tests and allow the full FFT processing associated with compliant OFDM transmissions to be engaged (compliant except for a single active subcarrier with large power in the middle of a large exclusion subband). This is the preference for verifying phase noise requirements.

If a continuous pilot is not used (as above), the OFDM channel has real data in the non-excluded subcarriers, FFT processing is occurring for those data subcarriers. The OFDM transmitter needs to generate a time continuous phase signal on the CW signal subcarrier that is synchronous with the data subcarriers RF and OFDM Clock. The OFDM test receiver need to be functionally equivalent to: 1) phase/noise test equipment that filters out data subcarriers and 2) a modified compliant receiver that validates the data subcarriers are operating properly. This latter step can be done non-real time.

100.4.4.1 Test mode 1

A CLT shall provide a test mode of operation, for out-of-service testing, configured for *N* channels but generating one CW signal per channel, one channel at a time at the center frequency of the selected channel; all other combined channels are suppressed. One purpose of this test mode is to support one method for testing the phase noise requirements of Table 100–4 and Table 100–16. As such, the CLT generation of a CW signal test tone should exercise the signal generation chain to the fullest extent practicable, in such a manner as to exhibit phase noise characteristics typical of actual operational performance; for example, repeated selection of a constellation symbol with power close to the constellation RMS level would seemingly exercise much of the modulation and up-conversion chain in a realistic manner. The CLT test mode shall be capable of generating the CW signal tone over the full range of Center Frequency in Table 100–16. In addition, the CLT shall be configurable in either one or both of the following conditions:

— Two CW signals on a single out-of-service downstream OFDM channel, at selectable valid subcarrier center frequencies 20 MHz to 100 MHz apart within the selected channel. All other subcarriers within the selected out-of-service downstream OFDM channel are suppressed.

— One CW signal on each of two separate but synchronized downstream OFDM channels at selectable valid subcarrier center frequencies 20 MHz to 100 MHz apart within the selected channels. All other subcarriers within the selected out-of-service downstream OFDM channel are suppressed.

The purpose of this test mode is to support the ability to measure the downstream OFDM Clock jitter requirements of Table 101–7, whereby the two CW signals are mixed to create a difference product CW signal at frequency ($f_2 - f_1$), for which the jitter is measure directly and compared to the requirements stated in that section.

100.4.4.2 Test mode 2

A CLT shall provide a test mode of operation, for out-of-service testing, generating one-CW-per-channel, at the center frequency of the selected channel, with all other N – 1 of the combined channels active and containing valid data modulation at operational power levels. One purpose for this test mode is to support one method for testing the phase noise requirements of Table 100–16. As such, the generation of the CW test tone should exercise the signal generation chain to the fullest extent practicable, in such manner as to exhibit phase noise characteristics typical of actual operational performance. For example, a repeated selection of a constellation symbol, with power close to the constellation RMS level, would seemingly exercise much of the modulation and up-conversion chain in a realistic manner. For this test mode, it is acceptable that all channels operate at the same average power, including each of the N – 1 channels in valid operation, and the single channel with a CW tone at its center frequency.

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100.5 Environmental, safety, and labeling

100.5.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

100.5.2 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

100.5.3 Environment

Normative specifications in this clause should be designed to be met by a system integrating 10GPASS-XR over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the RF link, the distance and operating environmental conditions over which the specifications of this clause will be met.

100.5.4 PMD labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 10GPASS-XR).

100.5.4.1 Frequency plan

Equipment conforming to this standard shall be clearly labeled with information about the supported downstream and upstream frequency ranges.

100.5.4.1.1 Downstream frequency plan

The CLT transmitter and CNU receiver are expected to support a frequency range from 258 MHz to 1218 MHz as defined in Table 100–3. Equipment may be adapted to all or part of this frequency band to suit regional requirements.

100.5.4.1.2 Upstream frequency plan

The CNU transmitter and CLT receiver are expected to support a frequency range from 7.4 MHz to 204 MHz as defined in Table 100–11. Equipment may be adapted to all or part of this frequency band to suit regional requirements.

100.6 EEE capability

For the 10GPASS-XR-U PHY the CNU shall enable Energy-Efficient Ethernet (EEE) capability to conserve energy by deactivating power-consuming PMD Functions (e.g., RF power amplifier) between bursts using PMD_SIGNAL.request (see 100.2.1.3).

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100.7 Protocol implementation conformance statement (PICS) proforma for Clause 100, Physical Medium Dependent (PMD) sublayer and medium for coaxial cable distribution networks, type 10GPASS-XR[174]

The supplier of a protocol implementation that is claimed to conform to Clause 100, Physical Medium Dependent (PMD) sublayer and medium for passive optical networks type 10GPASS-XR shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

100.7.1 Identification

100.7.1.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

100.7.1.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 100, Physical Medium Dependent (PMD) Sublayer for 10GPASS-XR
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[174] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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100.7.2 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
DC	Delay constraints	100.2.2	Device conforms to delay constraints	M	Yes [ ]
DMM	Downstream modulation rates	100.3.1	Provides mandatory rates specified in Table 100–2	M	Yes [ ]
CLTO1	Downstream modulation rate 8-QAM	100.3.1	Optional rate in Table 100–2	CLT:O	Yes [ ] No [ ] N/A [ ]
CNUO1	Downstream modulation rate 8-QAM	100.3.1	Optional rate in Table 100–2	CNU:O	Yes [ ] No [ ] N/A [ ]
CLTO2	Downstream modulation rate 16-QAM	100.3.1	Optional rate in Table 100–2	CLT:O	Yes [ ] No [ ] N/A [ ]
CNUO2	Downstream modulation rate 16-QAM	100.3.1	Optional rate in Table 100–2	CNU:O	Yes [ ] No [ ] N/A [ ]
CLTO3	Downstream modulation rate 32-QAM	100.3.1	Optional rate in Table 100–2	CLT:O	Yes [ ] No [ ] N/A [ ]
CNUO3	Downstream modulation rate 32-QAM	100.3.1	Optional rate in Table 100–2	CNU:O	Yes [ ] No [ ] N/A [ ]
CLTO4	Downstream modulation rate 8192-QAM	100.3.1	Optional rate in Table 100–2	CLT:O	Yes [ ] No [ ] N/A [ ]
CNUO4	Downstream modulation rate 8192-QAM	100.3.1	Optional rate in Table 100–2	CNU:O	Yes [ ] No [ ] N/A [ ]
CLTO5	Downstream modulation rate 16384-QAM	100.3.1	Optional rate in Table 100–2	CLT:O	Yes [ ] No [ ] N/A [ ]
CNUO5	Downstream modulation rate 16384-QAM	100.3.1	Optional rate in Table 100–2	CNU:O	Yes [ ] No [ ] N/A [ ]
UMM	Upstream modulation rates	100.3.1	Provides mandatory rates specified in Table 100–2	M	Yes [ ]
CLTO6	Upstream modulation rate 2048-QAM	100.3.1	Optional rate in Table 100–2	CLT:O	Yes [ ] No [ ] N/A [ ]
CNUO6	Uptream modulation rate 2048-QAM	100.3.1	Optional rate in Table 100–2	CNU:O	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
CLTO7	Upstream modulation rate 4096-QAM	100.3.1	Optional rate in Table 100–2	CLT:O	Yes [ ] No [ ] N/A [ ]
CNUO7	Upstream modulation rate 4096-QAM	100.3.1	Optional rate in Table 100–2	CNU:O	Yes [ ] No [ ] N/A [ ]

100.7.3 PICS proforma tables for Physical Medium Dependent (PMD) sublayer for coax cable distribution networks, type 10GPASS-XR

100.7.3.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FN1	Transmit function	100.2.3	Conveys I/Q value pairs from PMD service interface to MDI	M	Yes [ ]
FN2	Receive function	100.2.4	Conveys I/Q value pairs from MDI to PMD service interface	M	Yes [ ]
DSRU	Update DS_DataRate	100.3.2.1	Updates after configuration or pilot change	CLT:M	Yes [ ] No [ ]
USRU	Update DS_DataRate	100.3.2.2	Updates after profile or pilot change	CLT:M	Yes [ ] No [ ]
CLTRF	CLT modulated RF signal	100.3.3.2	Meets specifications in Table 100–3, Table 100–5, and Table 100–6	CLT:M	Yes [ ] No [ ]
CLTPN	CLT phase noise	100.3.3.3	Meets specifications as per Table 100–4	CLT:M	Yes [ ] No [ ]
CLTCP	CLT power per OFDM channel	100.3.3.4	Comply with all requirements in 100.3.3	CLT:M	Yes [ ] No [ ]
CLTSE1	CLT out-of-band spurious emissions below 600 MHz	100.3.3.5	Satisfy requirements of Table 100–6 below 600 MHz or when or when ratio of modulated to gap spectrum ≥ 4:1	CLT:M	Yes [ ] No [ ]
CLTSE2	CLT out-of-band spurious emissions of at least 600 MHz	100.3.3.5	Satisfy requirements of Table 100–6 of ≥ 6 MHz and with exclusion bands within OFDM channels of at least 8 MHz	CLT:M	Yes [ ] No [ ]
CLTSE3	CLT out-of-band spurious emissions with 1 dB relaxation	100.3.3.5	Satisfy requirements of Table 100–6 in measurements within gap spectrum < 600 MHz and within encompassed spectrum	CLT:M	Yes [ ] No [ ]
CLTSE4	CLT out-of-band spurious emissions with 3 dB relaxation	100.3.3.5	Satisfy requirements of Table 100–6 when ratio of modulated to gap spectrum is ≥ 4:1 from 603 MHz to 999 MHz	CLT:M	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
CLTSE5	CLT out-of-band spurious emissions with 5 dB relaxation	100.3.3.5	Satisfy requirements of Table 100–6 when ratio of modulated to gap spectrum is ≥ 4:1 from 999 MHz to 1209 MHz	CLT:M	Yes [ ] No [ ]
CLTSE6	CLT out-of-band spurious emissions with all cylic prefix and windowing roll-off period configurations	100.3.3.5	Satisfy requirements of Table 100–6 of a least 1 MHz for all combinations of *DSNcp* and *DSNrp* values	CLT:M	Yes [ ] No [ ]
CLTCF	CLT independent selection of center frequency	100.3.3.6	Meets ratio of number of active OFDM channels to gap spectrum in encompass spectrum of a least 2:1 as per 100.3.3.6	CLT:M	Yes [ ] No [ ]
CLTPD	CLT transmitter output	100.3.3.6	Disable transmitter output when *PD_Enable* is equal to FALSE and continue in normal transmitter operation when *PD_Enable* is equal to TRUE	CLT:M	Yes [ ] No [ ]
CLTPL	CLT power limit	100.3.4.2	Limit $P1.6_{Max}$ to no more than 53.2 dBmV+ (P_{Max} – 65) if the bandwidth of the modulated spectrum is ≤ 24 MHz	CLT:M	Yes [ ] No [ ]
CNULP	CNU initial power	100.3.4.2	Initiate PHY Discovery using lowest power as set by CLT using *PdRespInitPwr*	CNU:M	Yes [ ] No [ ]
CNUTP	CNU target power for each subcarrier	100.3.4.2	Meets Equation (100–9)	CNU:M	Yes [ ] No [ ]
CNURP	CNU reported power	100.3.4.3	CNU reports its transmit power using the variable *ReportedPwr* when requested by the CLT	CNU:M	Yes [ ] No [ ]
CNUSE1	CNU noise and spurious emissions RF PA turn on and off	100.3.4.4	Meets specifications in Table 100–7, Table 100–8, and Table 100–9 during RF power amplifier turn on and turn off	CNU:M	Yes [ ] No [ ]
CNUSE2	CNU noise and spurious emissions change in voltage	100.3.4.4	No more then 50 mV due to enabling or disabling transmission	CNU:M	Yes [ ] No [ ]
CNUSE3	CNU voltage step	100.3.4.4	No faster than 4 μs when transmitting ≥ +55 dBmV	CNU:M	Yes [ ] No [ ]
CNUSE4	CNU maximum change in voltage	100.3.4.4	Decrease by a factor of 2 for each 6 dB decrease from +55 dBmV to a maximum change of 3.5 mV ≤ 31 dBmV	CNU:M	Yes [ ] No [ ]
CNUTM	CNU transmit MER	100.3.4.5	Meets requirements in Table 100–10	CNU:M	Yes [ ] No [ ]
CNURF	CNU modulated RF signal	100.3.4.6	Meets specifications in Table 100–11	CNU:M	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
CNUPD	CNU transmitter output	100.3.4.7	Disable transmitter output when *PD_Enable* is equal to FALSE and continue in normal transmitter operation when *PD_Enable* is equal to TRUE	CNU:M	Yes [ ] No [ ]
CLTRX1	CLT receiver input signal level	100.3.5.1	Operate with an average up to 31 dBmV	CLT:M	Yes [ ] No [ ]
CLTRX2	CLT receiver configuration	100.3.5.1	As per Table 100–12 for intended received power normalized to 6.4 MHz of bandwidth	CLT:M	Yes [ ] No [ ]
CLTRPW	CLT power measurements	100.3.5.1	Provide upstream power measurements with a standard deviation of 0.33 dB or better conditions given in 100.4.3	CNU:M	Yes [ ] No [ ]
CLTEP	CLT receiver error performance	100.3.5.2	Meets specifications in Table 100–13	CLT:M	Yes [ ] No [ ]
CLTRM1	CLT receiver MER all active subcarriers	100.3.5.3	Measurements of receive MER for all active subcarriers	CLT:M	Yes [ ] No [ ]
CNUSR	CNU signal reception	100.3.6.1	Meets specifications in Table 100–14	CNU:M	Yes [ ] No [ ]
CNUER	CNU receive post-FEC error ratio	100.3.6.2	$\leq 10^{-6}$ frame loss ratio when meeting specifications in 100.3.6.2 and Table 100–15	CNU:M	Yes [ ] No [ ]
CNURM2	CNU receive MER	100.3.6.3	Receive MER_std ≤ 0.5 dB and delta receiver ≤ 4 dB and ≥ 6 dB when operating conditions specified in 100.4.2	CNU:M	Yes [ ] No [ ]
EE	Energy savings	100.6	Turn off RF power amplifier between bursts	CNU:M	Yes [ ] No [ ]

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100.7.3.2 Definition of parameters and measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
TST1	CLT transmitter mute	100.4.1	Support *CLT_TxMute* as per 100.4.1	CLT:M	Yes [ ] No [ ]
TST2	CLT transmitter phase noise tests	100.4.4	Meet specifications in Table 100–16	CLT:M	Yes [ ] No [ ]
TST3	CLT test mode 1	100.4.4.1	Provide a test mode as per 100.4.4.1	CLT:M	Yes [ ] No [ ]
TST3	CLT test mode 2	100.4.4.2	Provide a test mode as per 100.4.4.2	CLT:M	Yes [ ] No [ ]

100.7.3.3 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	100.5.1	Conforms to J.2	M	Yes [ ]
ES2	Installation	100.5.2	Meets applicable local codes and regulation	M	Yes [ ]
ES3	Documentation	100.5.3	Explicitly defines requirements and usage restrictions to meet environment and safety certifications	M	Yes [ ] No [ ]
ES4	Labeling	100.5.4.1	Frequency plan labeled in a manner visible to the user	M	Yes [ ] No [ ]

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101. Reconciliation Sublayer, Physical Coding Sublayer, and Physical Media Attachment for EPoC

101.1 Overview

This clause describes the Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS) with FEC, and Physical Medium Attachment (PMA) used with 10GPASS-XR point-to-multipoint (P2MP) networks. These are multipoint coaxial cable distribution networks (CCDN) that connect multiple DTEs using a single shared coaxial link. The architecture is asymmetric, based on a tree and branch topology utilizing coaxial taps and splitters. This type of network requires that the Multipoint MAC Control sublayer exists above MAC instances, as described in Clause 103.

101.1.1 Conventions

The notation used in the state diagrams in this clause follows the conventions in 21.5. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation "++" after a counter indicates it is to be incremented by 1. The notation "––" after a counter indicates it is to be decremented by 1. Code examples given in this clause adhere to the style of the "C" programming language.

For equations used in this clause the symbol $\lceil x \rceil$ represents a ceiling function that rounds up its argument x to the next highest integer. The notation $\lfloor x \rfloor$ represents a *floor* function, which returns the value of its argument x rounded down to the nearest integer.

101.1.2 Constraints for delay through RS, PCS, and PMA

The operation of EPoC Multipoint Control Protocol (MPCP), as defined in Clause 103, relies on strict timing based on the distribution of timestamps. The actual delay is implementation-dependent but an implementation shall maintain a combined delay variation through RS, PCS, and PMA sublayers of no more than 1 time_quantum (see 64.2.2.1) so as not to interfere with the MPCP timing and operation.

101.1.3 Mapping of PCS, and PMA variables

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the 10GPASS-XR PHY or are communicated between the CLT and the CNU via the PHY Link. The mapping of MDIO control and status variables to PCS/PMA variables is shown in Table 101–1. The least significant bit in each variable is mapped to the lowest numbered bit in the lowest numbered register for Clause 45 registers. These variables are used by the PHY Link for PHY management.

101.1.4 Functional blocks supporting 10GPASS-XR PCS, PMA, and PMD sublayers

Figure 101–1 and Figure 101–4 illustrate functional blocks within the CLT PCS, PMA, and PMD sublayers, and interactions between them in the transmit direction and in the receive direction, respectively. Figure 101–2 and Figure 101–3 illustrate functional blocks within the CNU PCS, PMA, and PMD sublayers, and interactions between them in the transmit direction and in the receive direction, respectively. Clause 100 focuses on functions of the PMD sublayer, Clause 101 focuses on PCS and PMA, and Clause 102 focuses on PHY Link.

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Table 101–1—MDIO register to PHY variable mapping

MDIO parameter name	MDIO register name	Register/bit number	PHY variable		
			Name	Index	Bits(s)
CRC40 errored blocks	10GPASS-XR control and status	1900.2	*CRC40ErrCtrl*	0	2
Continuous pilot scaling factor	10GPASS-XR control and status	1.1900.9:3	*CntPltSF*	0	9:3
Time sync capable	10GPASS-XR control and status	1.1900.13	*TimeSyncCapable*	0	13
DS cyclic prefix	DS OFDM control	1.1901.3:0	*DSNcp*	1	3:0
DS windowing	DS OFDM control	1.1901.6:4	*DSNrp*	1	6:4
DS time interleaving	DS OFDM control	1.1901.11:7	*DS_TmIntrlv*	1	11:7
DS OFDM channels	DS OFDM control	1.1901.14:12	*DS_ChCnt*	1	14:12
DS OFDM freq ch 1	DS OFDM channel frequency control 1	1.1902.15:0	*DS_FreqCh(1)*	2	15:0
DS OFDM freq ch 2	DS OFDM channel frequency control 2	1.1903.15:0	*DS_FreqCh(2)*	3	15:0
DS OFDM freq ch 3	DS OFDM channel frequency control 3	1.1904.15:0	*DS_FreqCh(3)*	4	15:0
DS OFDM freq ch 4	DS OFDM channel frequency control 4	1.1905.15:0	*DS_FreqCh(4)*	5	15:0
DS OFDM freq ch 5	DS OFDM channel frequency control 5	1.1906.15:0	*DS_FreqCh(5)*	6	15:0
Resource Block size	US OFDM control	1.1907.7	*RBsize*	7	7
US windowing	US OFDM control	1.1907.6:4	*USNrp*	7	6:4
US cyclic prefix	US OFDM control	1.1907.3:0	*USNcp*	7	3:0
Type 2 repeat	US OFDMA pilot pattern	1.1909.14:12	*Type2_Repeat*	9	14:12
Type 2 start	US OFDMA pilot pattern	1.1909.11:8	*Type2_Start*	9	11:8
Type 1 repeat	US OFDMA pilot pattern	1.1909.6:4	*Type1_Repeat*	9	6:4
Type 1 start	US OFDMA pilot pattern	1.1909.3:0	*Type1_Start*	9	3:0
DS PHY data rate lower	DS PHY data rate	1.1927.15:3	*DS_DataRate(15:3)*	27	15:3
DS PHY data rate fractional	DS PHY data rate	1.1927.2:0	*DS_DataRate(2:0)*	27	2:0
DS PHY data rate mid	DS PHY data rate	1.1928.15:0	*DS_DataRate(31:16)*	28	15:0
DS PHY data rate upper	DS PHY data rate	1.1929.4:0	*DS_DataRate(36:32)*	29	4:0
US PHY data rate lower	US PHY data rate	1.19230.15:3	*US_DataRate(15:3)*	30	15:3
US PHY data rate fractional	US PHY data rate	1.1930.2:0	*US_DataRate(2:0)*	30	2:0

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Table 101–1—MDIO register to PHY variable mapping *(continued)*

MDIO parameter name	MDIO register name	Register/bit number	PHY variable		
			Name	Index	Bits(s)
US PHY data rate mid	US PHY data rate	1.1931.15:0	*US_DataRate(31:16)*	31	15:0
US PHY data rate upper	US PHY data rate	1.1932.4:0	*US_DataRate(36:32)*	32	4:0
FEC codeword counter lower	10GPASS-XR FEC codeword counter	1.1933.15:0	*FecCodeWordCount (15:0)*	33	15:0
FEC codeword counter upper	10GPASS-XR FEC codeword counter	1.1934.15:0	*FecCodeWordCount (31:16)*	34	15:0
FEC codeword success counter lower	10GPASS-XR FEC codeword success counter	1.1935.15:0	*FecCodeWordSuccess (15:0*)	35	15:0
FEC codeword success counter upper	10GPASS-XR FEC codeword success counter	1.1936.15:0	*FecCodeWordSuccess (31:16)*	36	15:0
FEC codeword fail counter lower	10GPASS-XR FEC codeword fail counter	1.1937.15:0	*FecCodeWordFail (15:0)*	37	15:0
FEC codeword fail counter upper	10GPASS-XR FEC codeword fail counter	1.1938.15:0	*FecCodeWordFail (31:16)*	38	15:0
US modulation ability	10GPASS-XR modulation ability	1.1948.9:8	*US_ModAbility*	48	9:8
DS OFDM channel ability	10GPASS-XR modulation ability	1.1948.7:5	*DS_OFDM_ChAbility*	48	7:5
DS modulation ability	10GPASS-XR modulation ability	1.1948.4:0	*DS_ModAbility*	48	4
DS OFDM channel ID	DS OFDM channel ID register	12.0.2:0	*DS_OFDM_ID*	1000	2:0
DS Modulation type SC7	10GPASS-XR DS profile descriptor control 1	12.1.15:12	*DS_ModTypeSC(7)*	1001	15:12
DS Modulation type SC6	10GPASS-XR DS profile descriptor control 1	12.1.11:8	*DS_ModTypeSC(6)*	1001	11:8
DS Modulation type SC5	10GPASS-XR DS profile descriptor control 1	12.1.7:4	*DS_ModTypeSC(5)*	1001	7:4
DS Modulation type SC4	10GPASS-XR DS profile descriptor control 1	12.1.3:0	*DS_ModTypeSC(4)*	1001	3:0
DS Modulation type SC8 through DS Modulation type SC4095	10GPASS-XR DS profile descriptor control 2 through 10GPASS-XR DS profile descriptor control 1023	12.2 through 12.1023	*DS_ModTypeSC(8)* through *DS_ModTypeSC(4095)*	1002 through 2023	as in index 1001
US Modulation type SC3	10GPASS-XR US profile descriptor control 0	12.1024.15:12	*US_ModTypeSC(3)*	2024	15:12
US Modulation type SC2	10GPASS-XR US profile descriptor control 0	12.1024.11:8	*US_ModTypeSC(2)*	2024	11:8

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Table 101–1—MDIO register to PHY variable mapping *(continued)*

MDIO parameter name	MDIO register name	Register/bit number	PHY variable		
			Name	Index	Bits(s)
US Modulation type SC1	10GPASS-XR US profile descriptor control 0	12.1024.7:4	*US_ModTypeSC(1)*	2024	7:4
US Modulation type SC0	10GPASS-XR US profile descriptor control 0	12.1024.3:0	*US_ModTypeSC(0)*	2024	3:0
US Modulation type SC4 through US Modulation type SC4095	10GPASS-XR US profile descriptor control 1 through 10GPASS-XR US profile descriptor control 1023	12.1025 through 12.2047	*US_ModTypeSC(4)* through *US_ModTypeSC(4095)*	2025 through 3047	as in index 1024
Real pre-equalizer coefficient SC0	10GPASS-XR US pre-equalizer coefficients 0	12.2048.15:0	*EQ_CoefR(0)*	3048	15:0
Imaginary pre-equalizer coefficient SC0	10GPASS-XR US pre-equalizer coefficients 0	12.2049.15:0	*EQ_CoefI(0)*	3049	15:0
Real pre-equalizer coefficient SC1 through Real pre-equalizer coefficient SC4095	10GPASS-XR US pre-equalizer coefficients 1 through 10GPASS-XR US pre-equalizer coefficients 4095	12.2050 12.2052 ... 12.10238	*EQ_CoefR(1)* through *EQ_CoefR(4095)*	3050 3052 ... 11238	15:0
Imaginary pre-equalizer coefficient SC1 through Imaginary pre-equalizer coefficient SC4095	10GPASS-XR US pre-equalizer coefficients 1 through 10GPASS-XR US pre-equalizer coefficients 4095	12.2051 12.2053 ... 12.10239	*EQ_CoefI(1)* through *EQ_CoefI(4095)*	3051 3053 ... 11239	15:0

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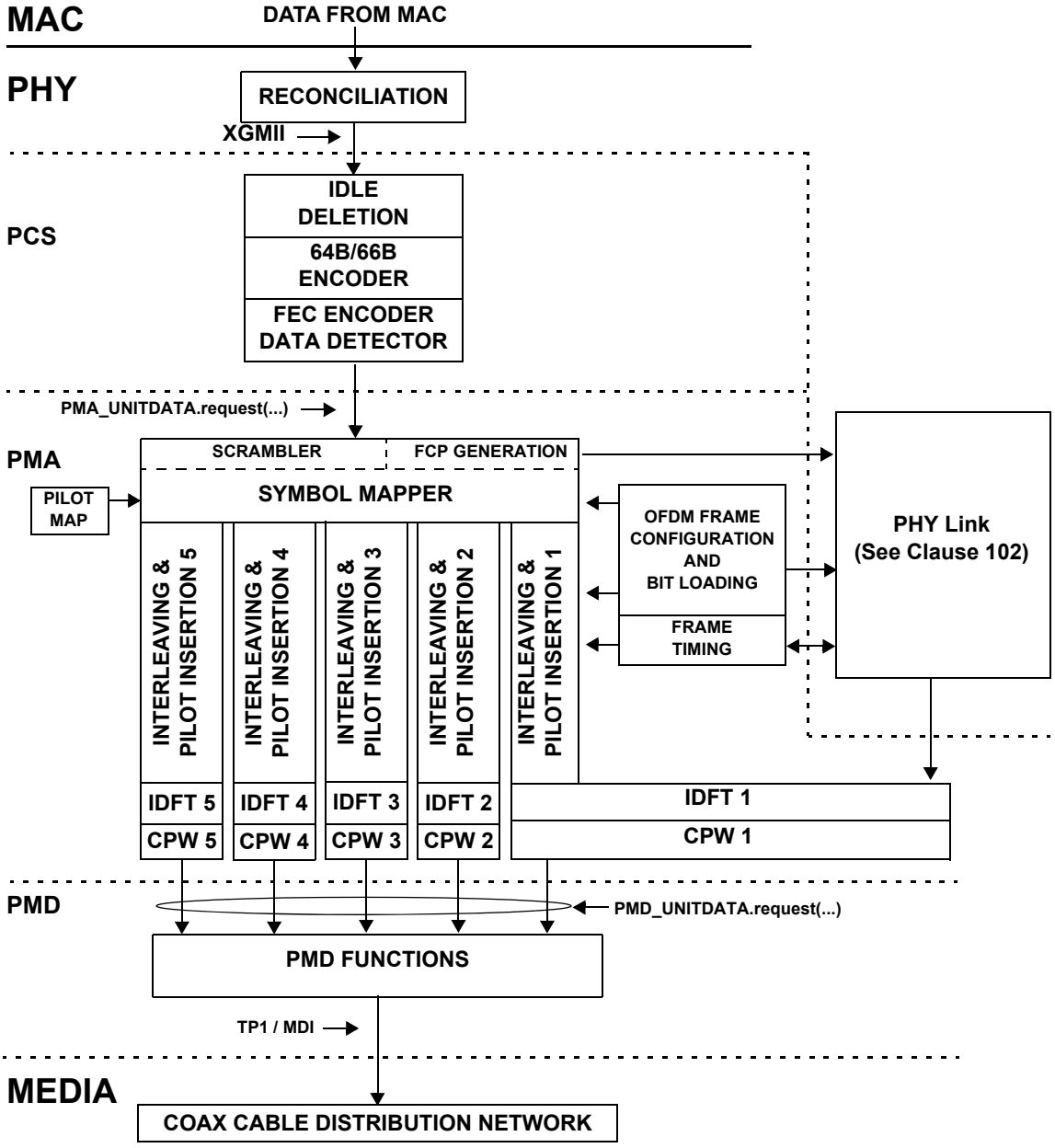
Clause 103 defines Multipoint MAC Control Protocol (MPCP) for operation in EPoC, extending Clause 77 model as necessary.



CPW = CYCLIC PREFIX AND WINDOWING
FCP = FEC CODEWORD POINTER
IDFT = INVERSE DISCRETE FOURIER TRANSFORM
TP1 = TEST POINT 1

Figure 101–1—Functional blocks within 10GPASS-XR-D CLT PCS, PMA, and PMD sublayers, transmit direction

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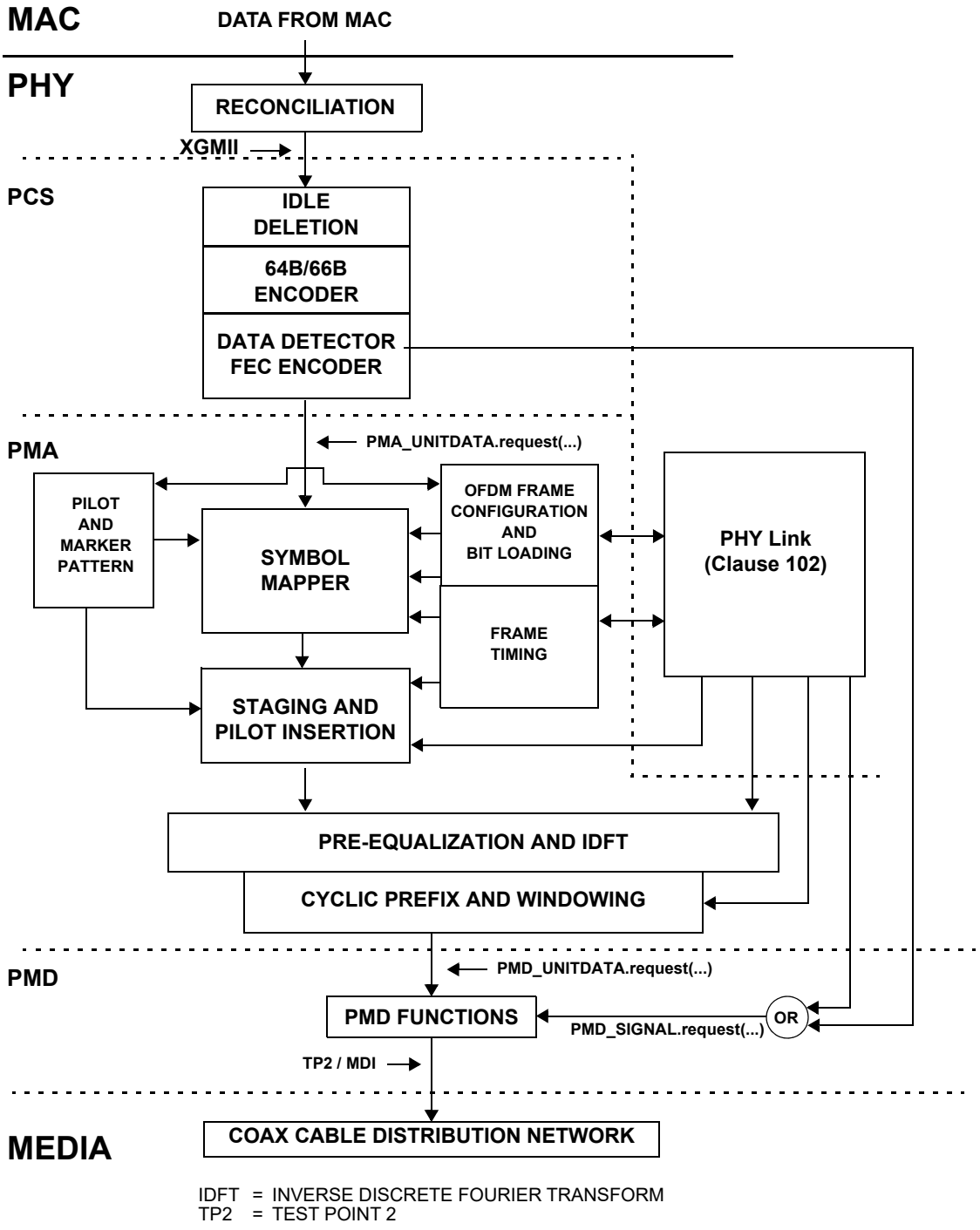

Figure 101–2—Functional blocks within 10GPASS-XR-U CNU PCS, PMA, and PMD sublayers, transmit direction

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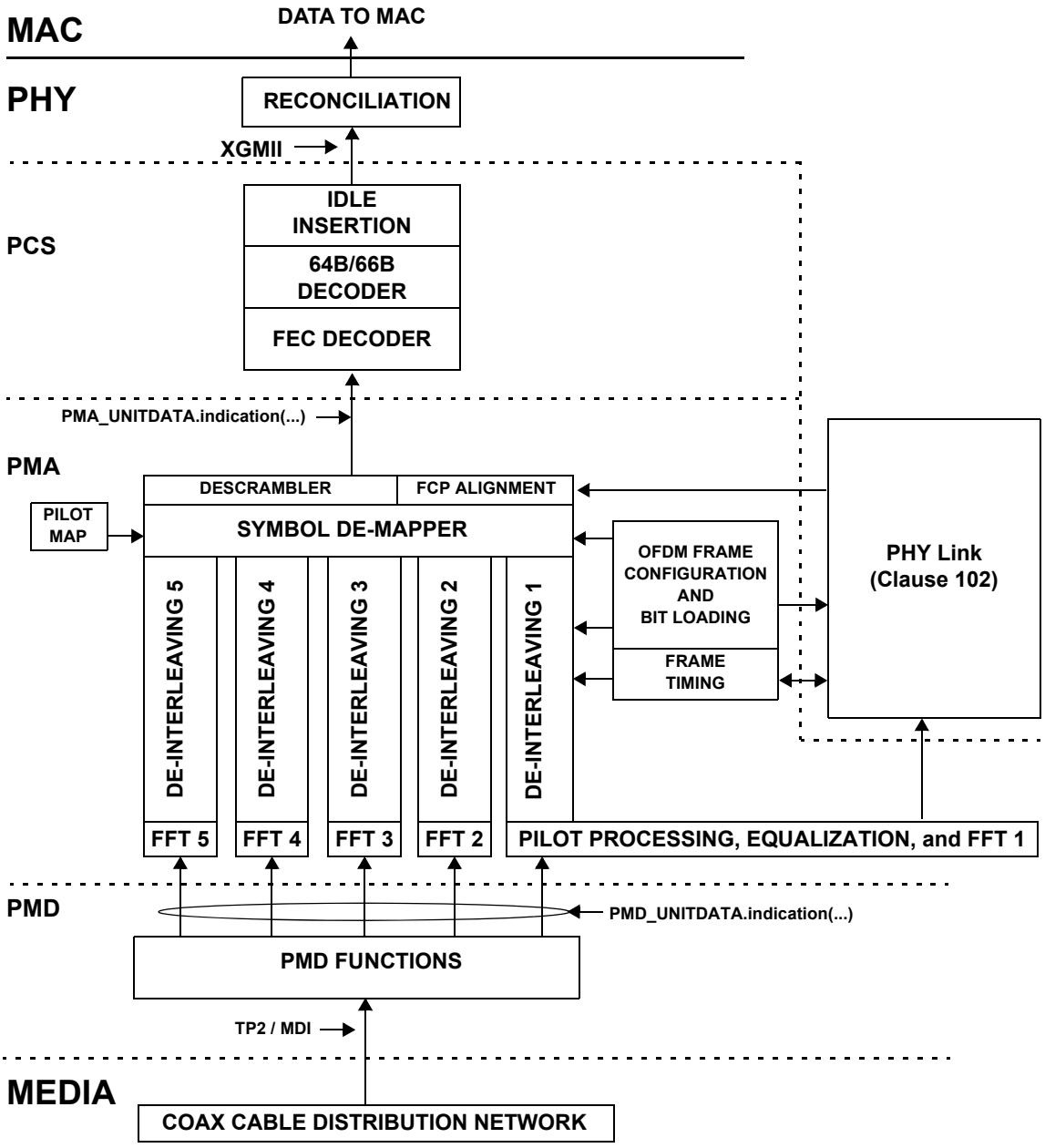

FCP = FEC CODEWORD POINTER
FFT = FAST FOURIER TRANSFORM
TP2 = TEST POINT 2

Figure 101–3—Functional blocks within 10GPASS-XR-D CNU PCS, PMA, and PMD sublayers, receive direction

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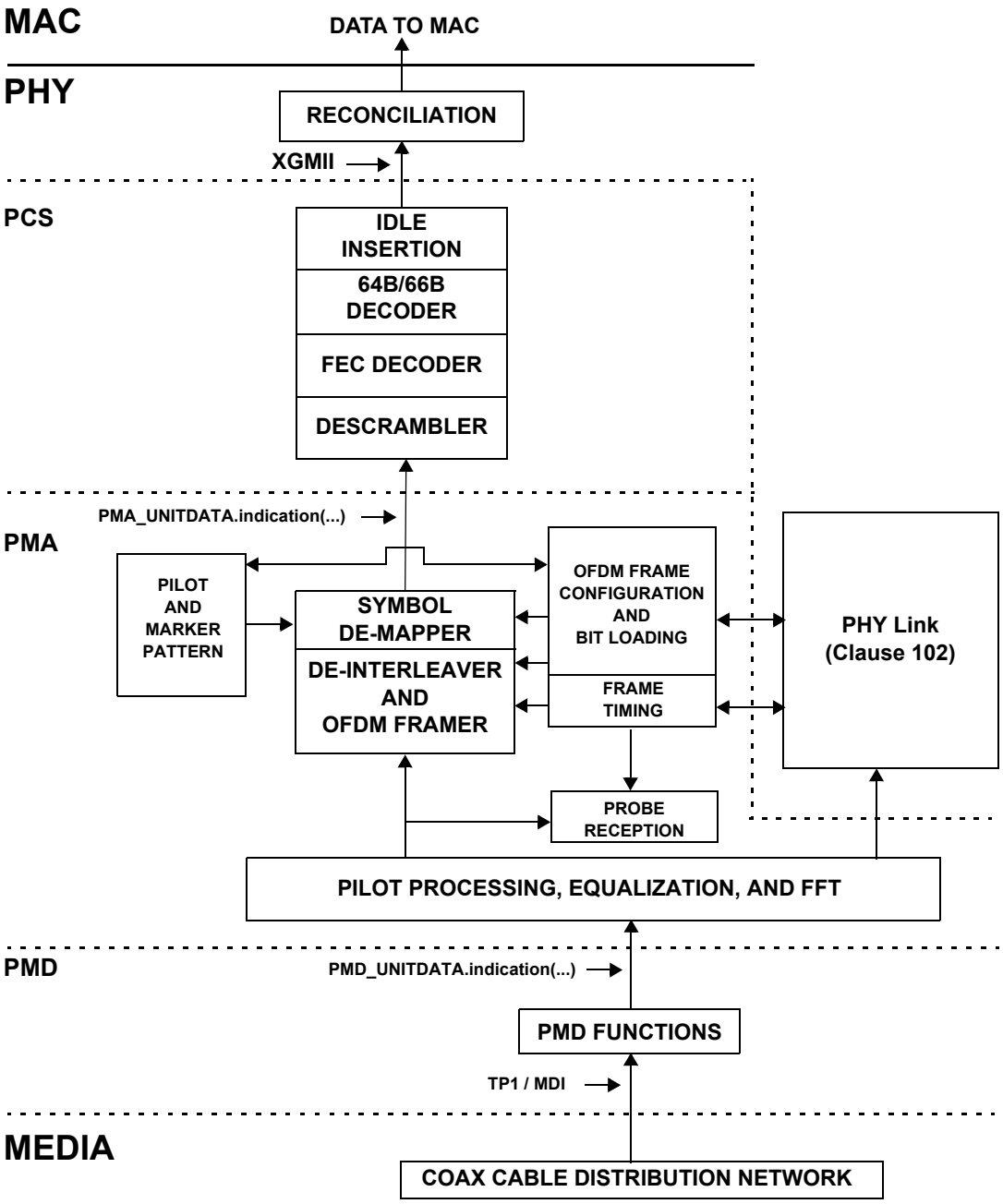

FFT = FAST FOURIER TRANSFORM
TP1 = TEST POINT 1

Figure 101–4—Functional blocks within 10GPASS-XR-U CLT PCS, PMA, and PMD sublayers, receive direction

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101.2 Reconciliation Sublayer (RS) for EPoC

The Reconciliation sublayer used for 10GPASS-XR is identical to that described in 76.2.

101.3 Physical Coding Sublayer (PCS) for EPoC

101.3.1 Overview

This subclause defines the Physical Coding Sublayer (PCS) for 10GPASS-XR, supporting operation over the point-to-multipoint coaxial cable distribution network. The EPoC PCS is specified to support the operation of up to 10 Gb/s in the downstream direction and up to 1.6 Gb/s in the upstream direction, where the upstream and downstream data rates are configured independently.

This subclause also specifies a forward error correction (FEC) as well as Idle control character insertion and deletion mechanisms. The FEC mechanism increases the available link budget. The FEC codeword additionally includes a CRC40 to ensure that mean time to false frame acceptance of 4.4×10^{17} seconds is met. The Idle control character insertion and deletion mechanisms accommodates rate adaptation between the MAC and MAC Control Clients operating at 10 Gb/s and the EPoC PCS and PMD sublayers operating at data rates below 10 Gb/s.

Figure 101–5 shows the relationship between the EPoC PCS sublayer and the ISO/IEC OSI reference model. Figure 101–1 illustrates the CLT transmitter functional block diagram, including the PCS, while Figure 101–2 illustrates the CNU transmitter functional block diagram. Figure 101–3 and Figure 101–4 illustrate the functional block diagram of the receive path in the CLT PCS and CNU PCS, respectively.

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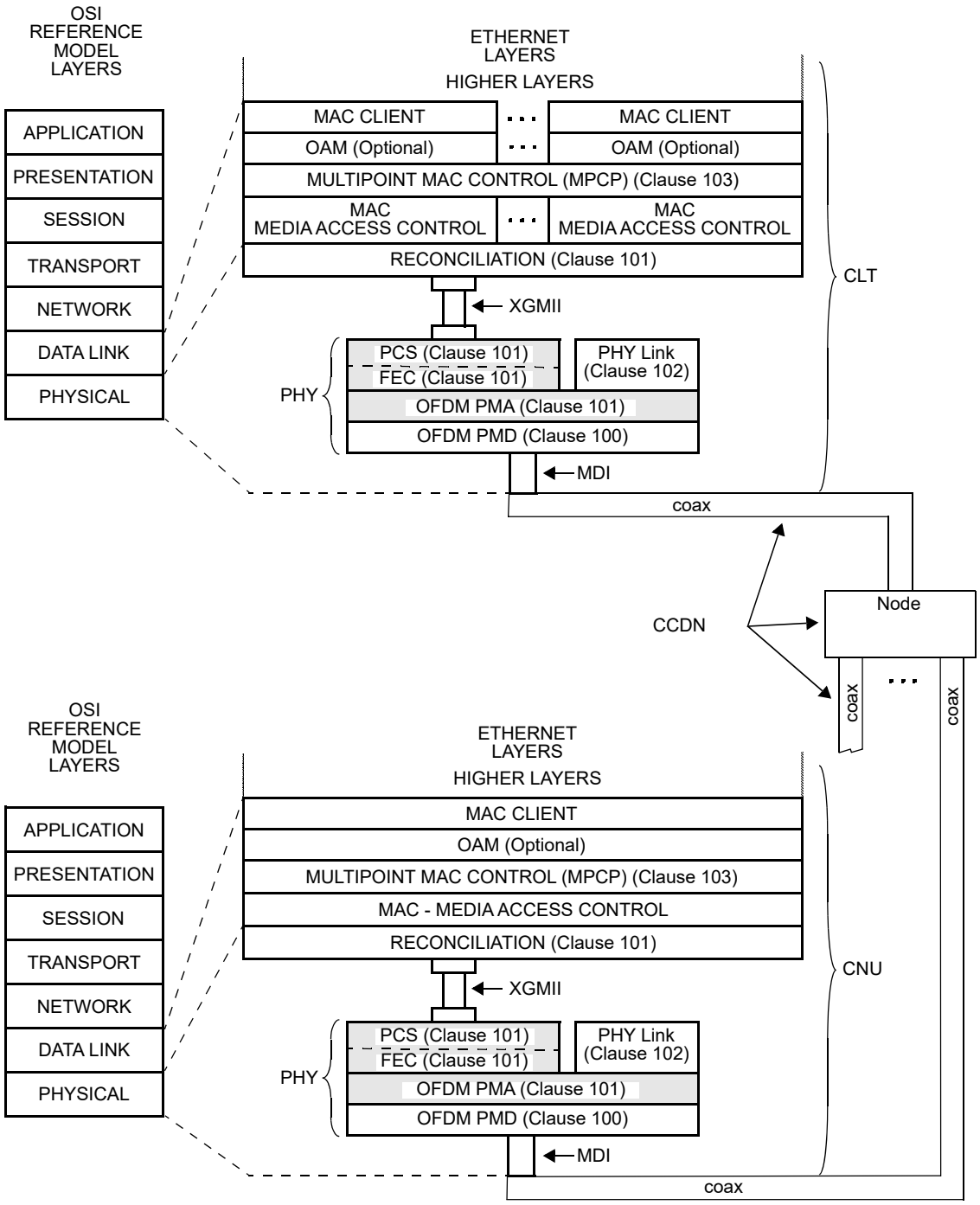

XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
CCDN= COAX CABLE DISTRIBUTION NETWORK
CLT = COAXIAL LINE TERMINAL
CNU = COAXIAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 101–5—Relationship of EPoC PCS and PMA to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet LAN model

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101.3.2 PCS transmit function

In the CLT, the PCS transmit function operates in a continuous fashion at the data rate of up to 10 Gb/s. In the CNU, the PCS transmit function operates in a burst mode at the data rate of up to 1.6 Gb/s. Figure 101–1 illustrates the CLT transmitter functional block diagram, while Figure 101–2 illustrates the CNU transmitter functional block diagram.

In the transmit direction, the EPoC PCS includes an Idle Deletion function that performs data rate adaptation and FEC overhead compensation, followed by a 64B/66B Encoder, and an FEC Encoder/Data Detector.

101.3.2.1 Idle deletion process

In the transmitting PCS, the Idle deletion process is responsible for deleting excess Idle control characters inserted between individual frames to adjust the data rate enforced by the MAC Control (as defined in Clause 103) to the effective data rate supported by the PCS and PMD. The gaps created within the data stream by the operation of the Idle deletion process are used in one of the following ways:

— Some gaps created by the removal of Idle control characters are filled with FEC parity data (FEC overhead compensation sub-process); or

— Other gaps created by the removal of Idle control characters are discarded in order to decrease the effective data rate between the MAC and PHY (data rate adaptation sub-process).

The Idle deletion process deletes a specific number of 72-bit vectors containing Idle control characters from the data stream composed of a series of 72-bit vectors received from the XGMII. The number of deleted 72-bit vectors containing Idle control characters depends on the EPoC PMD data rate, PMD overhead (including, for example, cyclic prefix), and the size of FEC parity data. The Idle deletion process performs the following two functions:

— Create gaps by Idle removal to allow for FEC parity/CRC40.

— Rate adaptation by Idle removal to adjust from the XGMII rate to the PMD rate.

The operation of the EPoC MPCP defined in Clause 103 ensures that a sufficient number of Idle control characters are present in the data stream, so that the minimum IPG between two adjacent frames is preserved once all excess Idle control characters are removed through the operation of the data rate adaptation and the FEC overhead compensation sub-processes.

101.3.2.1.1 Constants

DS_FEC_OSize
: TYPE: U5.3 format
The number of 72-bit vectors constituting the overhead (parity and CRC40) portion of a downstream FEC codeword. To normalize the downstream pre-FEC data rate, the Idle deletion process removes *DS_FEC_OSize* vectors per every *DS_PHY_DSize* vectors transferred to the 64B/66B Encoder.
Value: (1800+40)/65

DS_PHY_DSize
: TYPE: 16-bit unsigned integer
The number of 72-bit vectors constituting the payload portion of a downstream FEC codeword. To normalize the effective downstream PCS data rate, the Idle deletion process removes DS_*PHY_OSize* vectors per every DS_*PHY_DSize* vectors to compensate for FEC overhead and PMD derating processes.
Value: 220

US_FEC_OSize
: TYPE: U5.3 format

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The number of 72-bit vectors constituting the parity (overhead) portion of a upstream FEC codeword. To normalize the upstream pre-FEC data rate, the Idle deletion process removes *US_FEC_OSize* vectors per every *US_PHY_DSize* vectors transferred to the 64B/66B Encoder.
Value: (280+40)/65

US_PHY_DSize
TYPE: 16-bit unsigned integer
The number of 72-bit vectors constituting the payload portion of a upstream FEC codeword. To normalize the effective upstream PCS data rate, the Idle deletion process removes *US_PHY_OSize* vectors per every *US_PHY_DSize* vectors to the compensation of FEC overhead and PMD derating process.
Value: 12

XGMII_Rate
TYPE: unsigned integer
The data transfer rate of the XGMII interface.
Value: 10 Gb/s

101.3.2.1.2 Variables

accResidue
TYPE: U1.3 format
The variable *accResidue* tracks the accumulation of *PHY_OSizeFrac*.

BEGIN
TYPE: Boolean
This variable is used when initiating operation of the state diagram. It is set to TRUE following initialization and every reset.

DelayBound
TYPE: 16-bit unsigned integer
This value represents the number of consecutive 65-bit blocks containing Idles used by the Data Detector input and CNU output process to determine end of burst. This value represents the delay sufficient to initiate the transmitter at the CNU and to accommodate timing jitter caused by PMA overhead, such as burst markers, and pilots. This variable is used only by the CNU. By default, the value should be set the same as that for length of the *FIFO_FEC_TX* buffer.

DS_DataRate
See 100.3.2.1.

DS_PHY_OSize
TYPE: 16-bit unsigned integer
To normalize the effective PCS data rate, the Idle deletion process removes *DS_PHY_OSize* vectors per every *DS_PHY_DSize* vectors to compensate for FEC overhead and PMD derating process. *DS_PHY_OSize* is defined in Equation (101–1).

$$DS\_PHY\_OSize = \left\lfloor \frac{XGMII\_Rate - PCS\_DS\_Rate}{PCS\_DS\_Rate} \times (DS\_PHY\_DSize + DS\_FEC\_OSize) + DS\_FEC\_OSize \right\rfloor \quad (101–1)$$

PCS_DS_Rate:
TYPE: UQ34.3 format
The transmission rate of PCS data, excluding the 64B/65B sync header bit in the 64/65B line encoder, as defined in Equation (101–2).

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$$PCS\_DS\_Rate = DS\_DataRate \times \frac{64}{65} \quad (101–2)$$

PHY_OSizeFrac:

TYPE: U0.3 format

The fractional part of *DS_PHY_OSize* due to the floor operation in Equation (101–1). The *PHY_OSizeFrac* is defined in Equation (101–3).

$$PHY\_OSizeFrac = \frac{XGMII\_Rate - PCS\_DS\_Rate}{PCS\_DS\_Rate} \times (DS\_PHY\_DSize + DS\_FEC\_OSize) + DS\_FEC\_OSize - DS\_PHY\_OSize \quad (101–3)$$

tx_raw<71:0>

This variable is defined in 49.2.13.2.2.

tx_raw_out<71:0>

72-bit vector sent from the output of the Idle deletion process to the 64B/66B Encoder. This vector contains two XGMII transfers mapped as shown for *tx_raw*<71:0>.

101.3.2.1.3 Counters

countDelete

TYPE: 16-bit unsigned integer

Counts the number of 72-bit vectors that need to be deleted from the received data stream as part of the data rate adaptation and FEC overhead compensation.

countVector

TYPE: 16-bit unsigned integer

Counts the number of 72-bit vectors transmitted after the removal of Idle characters as part of data rate adaptation and FEC overhead compensation.

101.3.2.1.4 Functions

T_TYPE(*tx_raw*<71:0>)

This function is defined in 49.2.13.2.3.

101.3.2.1.5 State diagrams

The CLT PCS shall perform the Idle deletion process as shown in Figure 101–6. The CNU PCS shall perform the Idle deletion process as shown in Figure 101–7.

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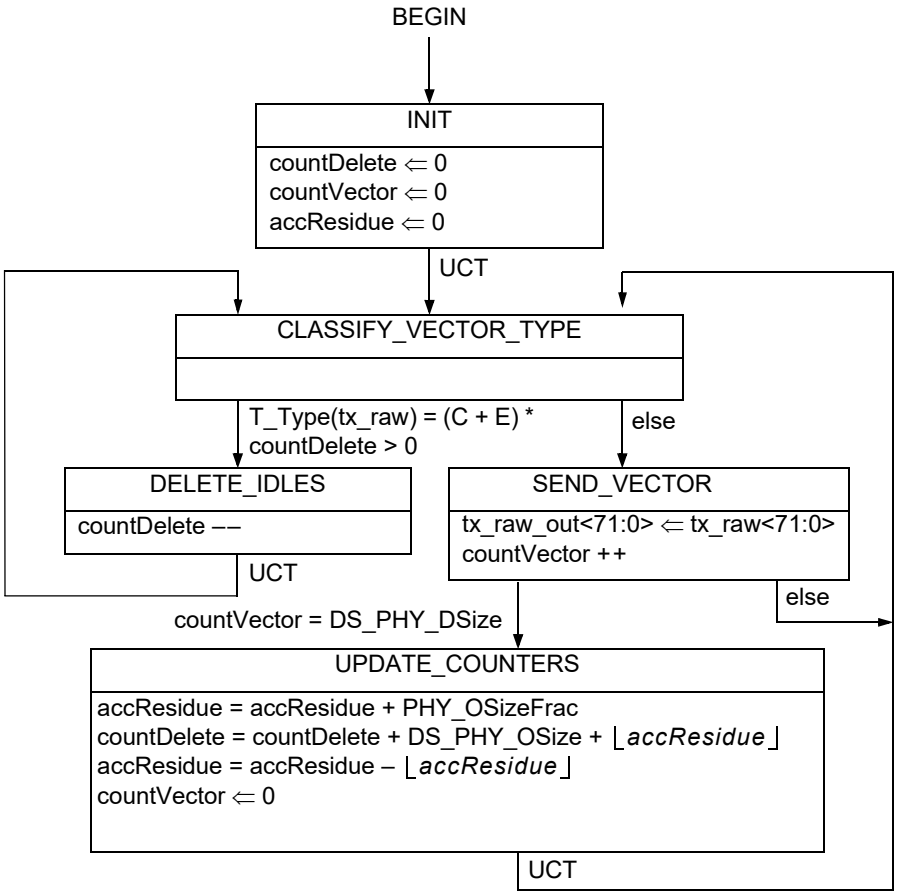

Figure 101–6—CLT Idle deletion process state diagram

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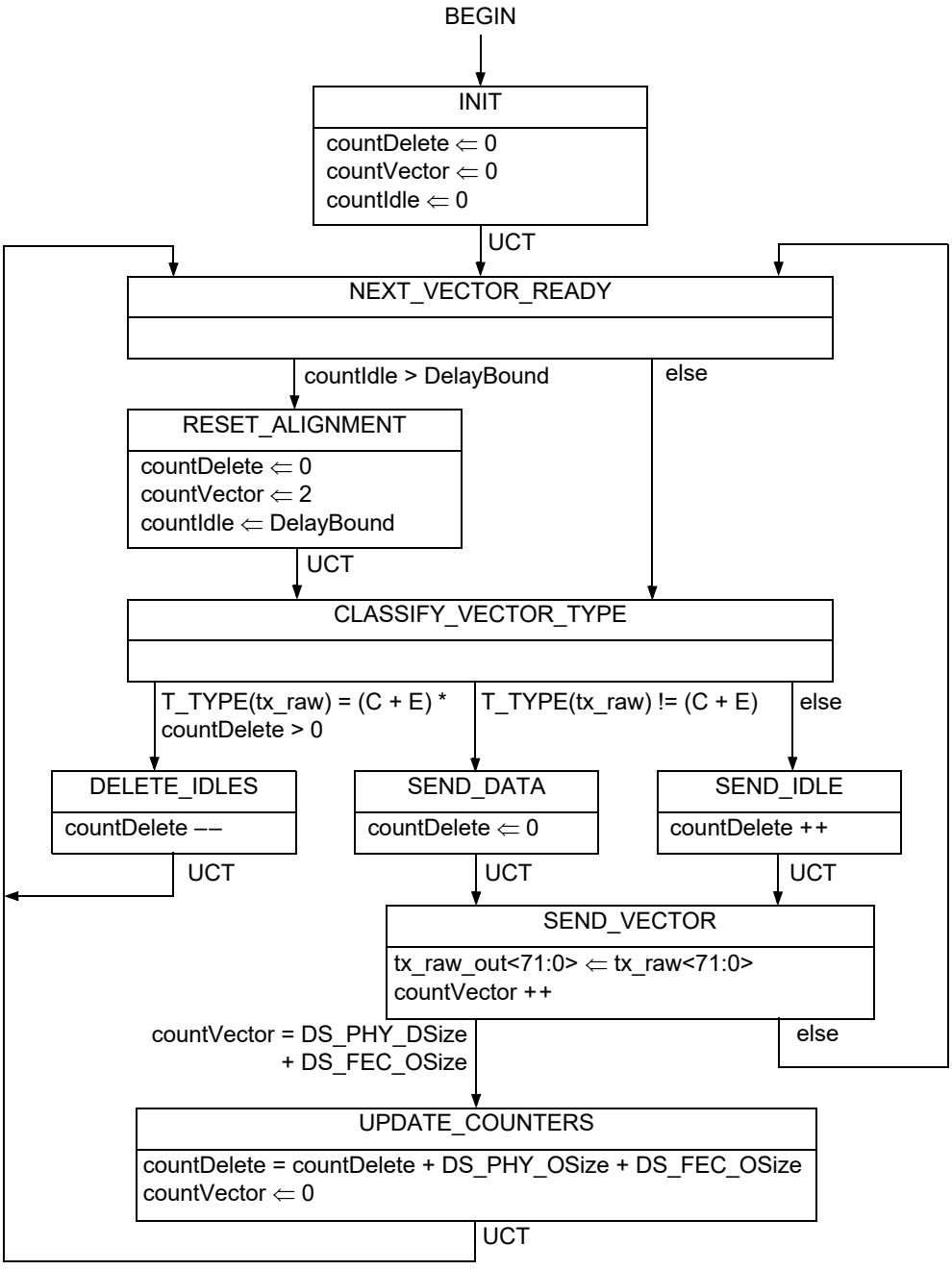

Figure 101–7—CNU Idle deletion process state diagram

101.3.2.2 64B/66B Encoder

The EPoC PHY utilizes a 64B/66B Encoder based on that described in 49.2.4 with several important differences. The EPoC 64B/66B Encoder does not include a scrambler function as described in 49.2.6 and the output is a 65B block with a single synch header bit. The state diagram found in Figure 49–16 is followed after which the sync header bit <0> is removed as illustrated in Figure 101–9.

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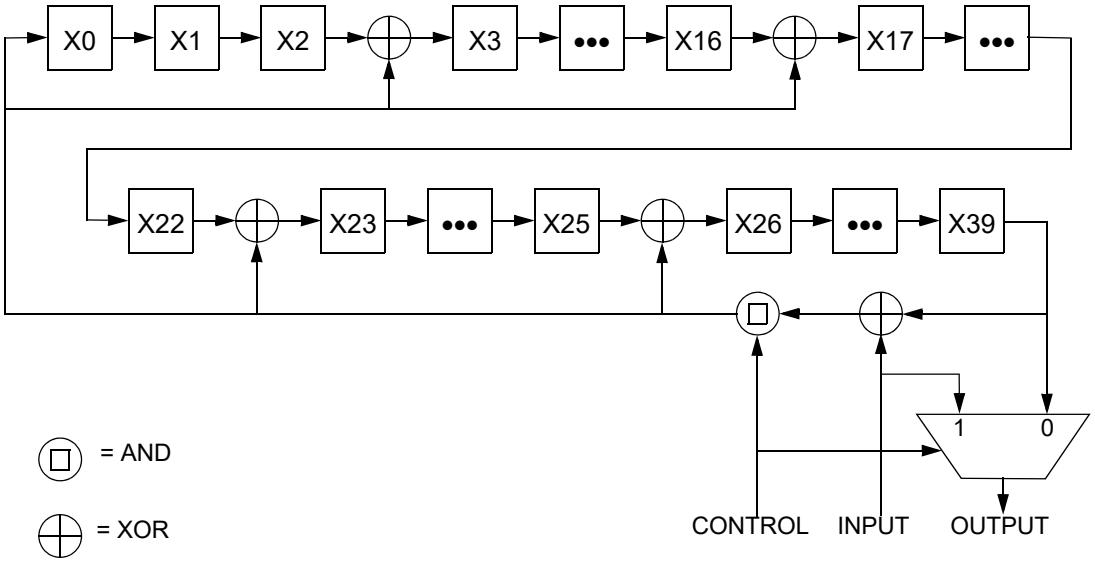
101.3.2.3 CRC40

The CRC40 field contains a 40-bit cyclic redundancy check value. This value is computed as a function of the contents of the B_Q 65-bit blocks (see Table 101–2), forming the payload portion of the FEC codeword.

The encoding is defined by the CRC40 generating polynomial shown in Equation (101–4):

$$x^{40} + x^{26} + x^{23} + x^{17} + x^3 + 1 \quad (101–4)$$

This CRC40 calculation shall produce the same result as the serial implementation shown in Figure 101–8. At the beginning of each FEC codeword (before the calculation of CRC40 begins), the shift register shall be initialized to the value zero. The content of the shift register is transmitted without inversion.



CONTROL = 1 when shifting the payload portion of FEC codeword calculation CRC40

CONTROL = 0 when transmitting the CRC40 field

Figure 101–8—CRC40 generation

101.3.2.4 Low Density Parity Check (LDPC) forward error correction (FEC) codes

The 10GPASS-XR PHY encodes the transmitted data using a systematic Low-Density Parity-Check (LDPC) (F_C, F_P) code. A LDPC Encoder encodes F_P information bits $i_{0 \ldots} i_{F_P - 1}$ into a codeword

$$cFc = (i_0, \ldots, i_{F_P - 1}, p_{F_P}, \ldots, p_{F_C - 1}) \quad (101–5)$$

by adding F_R parity bits $p_{F_p \ldots} p_{F_C - 1}$ obtained so that

$$Hc^T = 0$$

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where H is an $F_R \times F_C$ binary matrix containing mostly '0' and relatively few '1', called low-density parity-check matrix (see Gallagher [B26]). The detailed description of such parity check matrices is given in 101.3.2.4.1.

The CLT 10GPASS-XR PCS operating on a CCDN shall encode the transmitted data using the LDPC (16200, 14400) code per Table 101–2. The CNU 10GPASS-XR PCS operating on CCDN shall encode the transmitted data using one of the LDPC (F_C, F_P) codes per Table 101–2.

Table 101–2—LDPC codes used in EPoC

Upstream (US) Downstream (DS)	Codeword F_C [bits]	Payload F_P [bits]	Parity F_R [bits]	US filling threshold F_T		Payload		
				bits	65-bit blocks	65-bit blocks B_Q	CRC bits	Padding bits B_P
US/DS	16200	14400	1800	6601	101	220	40	60
US	5940	5040	900	1601	25	76	40	60
US	1120	840	280	1	1	12	40	20

101.3.2.4.1 LDPC matrix definition

The low-density parity check matrix H for LDPC (F_C, F_P) encoder can be divided into blocks of L^2 sub-matrices. Its compact circulant form is represented by an $m \times n$ block matrix:

$$H = \begin{bmatrix} H_{1,1} & H_{1,2} & H_{1,3} & \dots & H_{1,n} \\ H_{2,1} & H_{2,2} & H_{2,3} & \dots & H_{2,n} \\ H_{3,1} & H_{3,2} & H_{3,3} & \dots & H_{3,n} \\ \dots & \dots & \dots & & \dots \\ H_{m,1} & H_{m,2} & H_{m,3} & \dots & H_{m,n} \end{bmatrix}$$

where the submatrix $H_{i,j}$ is an $L \times L$ all-zero submatrix or a cyclic right-shifted identity submatrix. The last $n–m$ submatrix columns represent the parity portion of the matrix. Moreover, $nL = F_C$, $mL = F_P$ and the code rate is $(n – m)/n = (F_C – F_P)/F_C$. The submatrix size L is called the lifting factor.

The submatrix $H_{i,j}$ is represented by a value in {–1, 0,…, L–1}, where a '–1' value represents an all-zero submatrix, and the remaining values represent an $L \times L$ identity submatrix cyclically right-shifted by the specified value. Such representation of the parity-check matrix is called a base matrix.

Table 101–3 presents a 5×45 base matrix of the low-density parity-check matrix H for LDPC (16200, 14400) code listed in Table 101–2 for downstream and upstream. The lifting factor of the matrix is $L = 360$.

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Table 101–3—LDPC (16200, 14400) code matrix

Columns	Rows						Columns	Rows				
	1	2	3	4	5			1	2	3	4	5
1	93	274	134	–1	253		**24**	47	1	345	359	–1
2	271	115	355	–1	273		**25**	76	159	174	342	–1
3	–1	329	175	184	90		**26**	73	56	269	–1	232
4	83	338	24	70	–1		**27**	150	72	329	224	–1
5	26	124	253	247	–1		**28**	349	126	–1	106	21
6	208	–1	242	14	151		**29**	139	277	214	–1	331
7	245	293	–1	22	311		**30**	331	156	–1	273	313
8	200	–1	187	7	320		**31**	118	32	–1	177	349
9	–1	69	94	285	339		**32**	345	111	–1	245	34
10	175	64	26	54	–1		**33**	27	175	–1	98	97
11	331	342	87	–1	295		**34**	294	–1	218	355	187
12	17	–1	302	352	148		**35**	–1	306	104	178	38
13	86	88	–1	26	48		**36**	145	224	40	176	–1
14	–1	139	191	108	91		**37**	279	–1	197	147	235
15	337	–1	323	10	62		**38**	97	206	73	–1	52
16	–1	137	22	298	100		**39**	106	–1	229	280	170
17	238	212	–1	123	232		**40**	160	29	63	–1	58
18	81	–1	245	139	146		**41**	143	106	–1	–1	–1
19	–1	157	294	117	200		**42**	–1	334	270	–1	–1
20	307	195	240	–1	135		**43**	–1	–1	72	221	–1
21	–1	357	84	336	12		**44**	–1	–1	–1	208	257
22	165	81	76	49	–1		**45**	–1	–1	–1	–1	0
23	–1	194	342	202	179							

Table 101–4 presents a 5 × 33 base matrix of the low-density parity-check matrix H for LDPC (5940, 5040) code listed in Table 101–2 for upstream. The lifting factor of the matrix is $L = 180$.

Table 101–5 presents a 5 × 20 base matrix of the low-density parity-check matrix H for LDPC (1120, 840) code listed in Table 101–2 for upstream. The lifting factor of the matrix is $L = 56$.

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Table 101–4—LDPC (5940, 5040) code matrix

Columns	Rows						Columns	Rows				
	1	2	3	4	5			1	2	3	4	5
1	142	54	63	28	52		**18**	84	171	50	–1	168
2	158	172	11	160	159		**19**	–1	65	46	67	158
3	113	145	112	102	75		**20**	64	141	17	82	–1
4	124	28	114	44	74		**21**	66	–1	175	4	1
5	92	55	61	8	46		**22**	97	42	–1	177	49
6	44	19	123	84	71		**23**	1	83	–1	151	89
7	93	159	72	126	42		**24**	115	7	–1	131	63
8	70	22	55	9	11		**25**	8	–1	92	139	179
9	172	96	114	169	108		**26**	108	39	–1	117	10
10	3	12	20	174	153		**27**	–1	121	41	36	75
11	25	85	53	147	–1		**28**	–1	84	138	18	161
12	44	–1	114	24	72		**29**	11	101	–1	–1	–1
13	141	128	42	145	–1		**30**	–1	171	34	–1	–1
14	160	5	33	–1	163		**31**	–1	–1	74	23	–1
15	50	158	4	26	–1		**32**	–1	–1	–1	8	177
16	45	120	66	–1	9		**33**	–1	–1	–1	–1	19
17	118	51	163	–1	2							

Table 101–5—LDPC (1120, 840) code matrix

Columns	Rows						Columns	Rows				
	1	2	3	4	5			1	2	3	4	5
1	5	0	12	0	36		**11**	3	2	19	53	–1
2	14	35	28	51	6		**12**	–1	23	18	13	11
3	12	1	22	16	3		**13**	34	0	52	–1	22
4	1	26	46	31	51		**14**	7	51	–1	52	23
5	2	0	3	13	4		**15**	46	–1	37	33	43
6	37	10	16	39	19		**16**	10	49	–1	–1	–1
7	45	16	51	27	4		**17**	–1	20	34	–1	–1
8	26	16	2	33	45		**18**	–1	–1	39	38	–1
9	24	34	25	8	48		**19**	–1	–1	–1	7	14
10	0	4	29	27	9		**20**	–1	–1	–1	–1	1

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101.3.2.5 FEC Encoder and Data Detector processes

101.3.2.5.1 Data Detector process

The 10GPASS-XR PCS transmit path includes the Data Detector process. This process contains a delay line (represented by the *FIFO_FEC_TX* buffer) that stores 65-bit blocks received from the output of the 64B/66B Encoder to allow insertion of the FEC parity data into the transmitted data stream. The length of the *FIFO_FEC_TX* buffer is selected in such a way that it is large enough to compensate for the FEC overhead and PHY overhead, as discussed in 101.3.2.3 and 101.3.2.5.2.

101.3.2.5.2 LDPC encode process

The process of padding FEC codewords and appending FEC parity octets in the 10GPASS-XR PCS transmit path is illustrated in Figure 101–9. For the CLT, the FEC Encoder uses a single FEC LDPC codeword size of 16200 bits indicated by "DS" in Table 101–2 represented by constant FEC_DS_CodeWordSize (see 101.3.2.5.2). For the CNU, the FEC Encoder performs an algorithm as described in 101.3.2.5.4 for selecting the use of one or more "long" codewords (upstream size 16200 bits), a "medium" codeword (upstream size 5940), or one or more "short" codewords (upstream size 1120 bits) as detailed in Table 101–2.

The 64B/66B Encoder, as described in 101.3.2.2 and shown in Figure 101–9, delivers a stream of 65-bit blocks to the FEC Encoder and Data Detector. In the CNU only, a 65-bit Burst Time Header is added as the first 65-bit block at the start of a burst (see Figure 101–13).

Next, the FEC Encoder calculates CRC40 (see 101.3.3) over the aggregated B_Q (see Table 101–2) 65-bit blocks, placing the resulting 40 bits of CRC40 code immediately after the B_Q 65-bit blocks, forming the payload portion of the FEC codeword. Finally, based on the codeword size the FEC Encoder appends B_P (see Table 101–2) padding bits (with the binary value of "0") to the payload of the FEC codeword as shown in Figure 101–9.

The resulting F_P bits of data are then passed to the LDPC Encoder operating on a payload length of $F_P - B_P$ bits. The LDPC Encoder generates F_R bits of parity. After encoding, the encoder deletes the B_P bits of padding and constructs the output codeword with a length of $(F_P - B_P) + F_R$ bits.

101.3.2.5.3 LDPC codeword transmission order

Once the process of calculating FEC parity is complete, the payload portion of the FEC codeword and the parity portion of the FEC codeword are then transferred to the transmit PMA Client.

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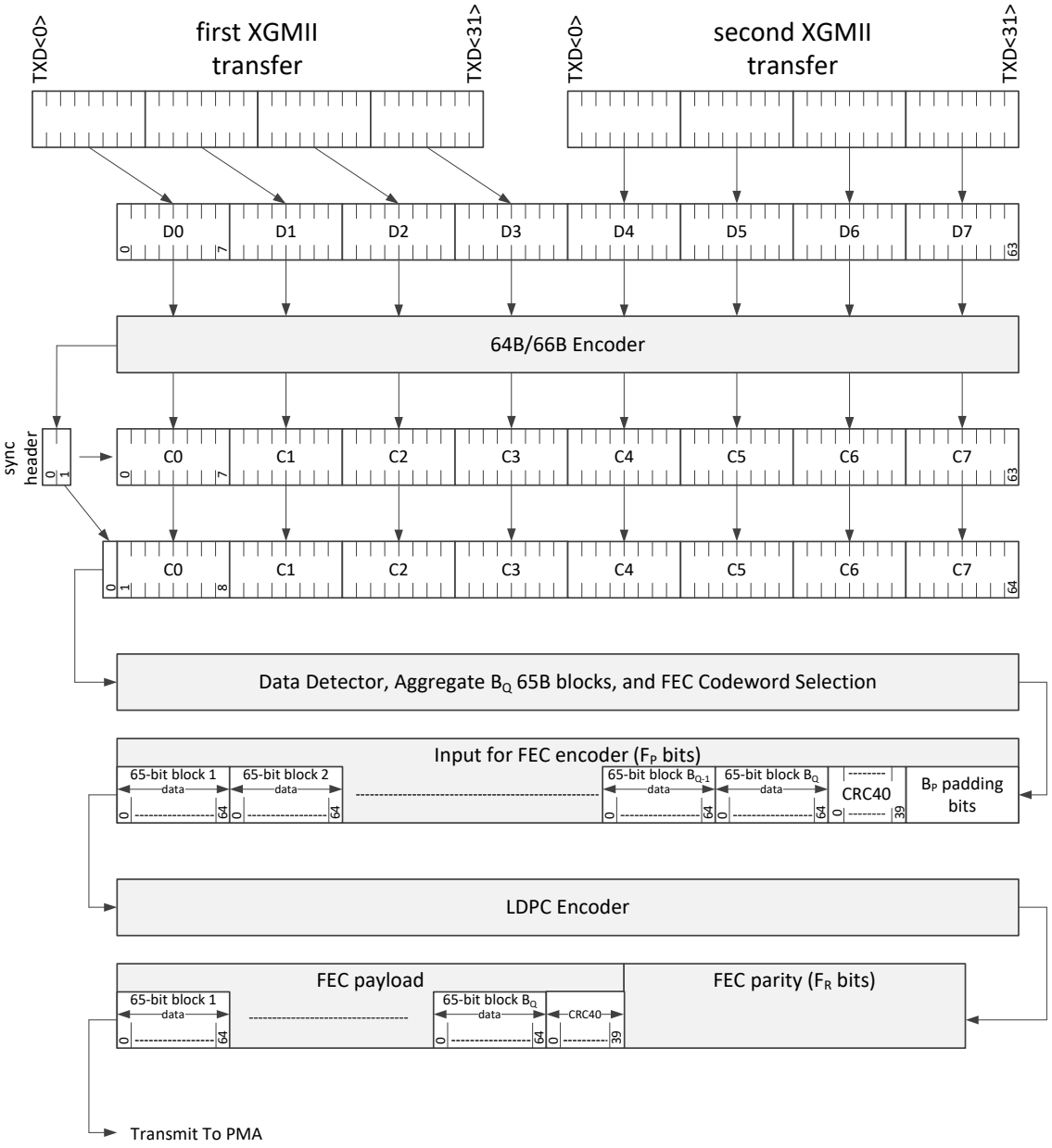

Figure 101–9—10GPASS-XR PCS transmit path processing

Figure 101–10 illustrates the details of the 10GPASS-XR CNU burst structure. In particular, this figure shows the details of the necessary burst elements and the FEC protected portions of the burst transmission, explicitly showing each FEC codeword.

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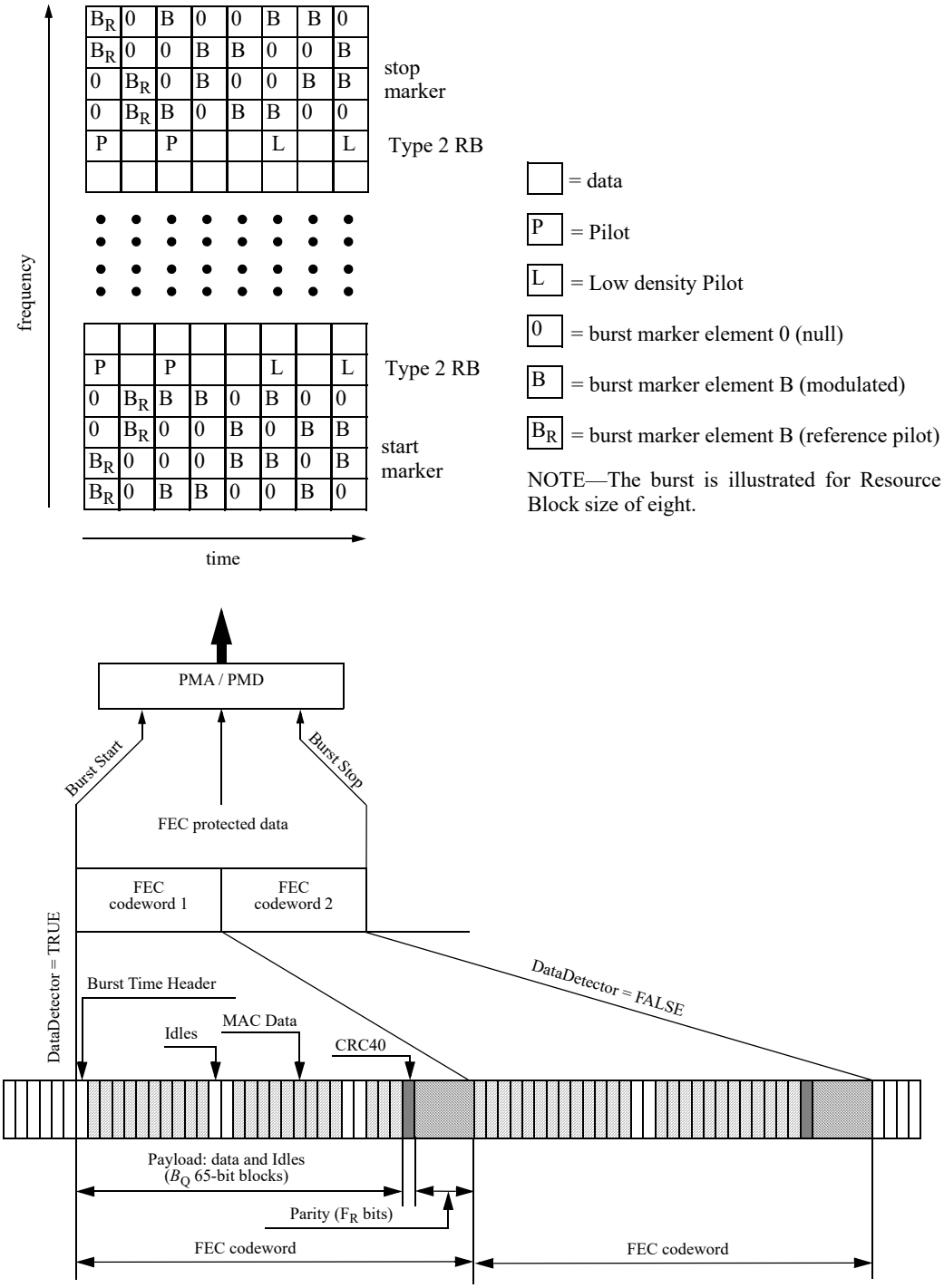

Figure 101–10—Details of burst composition

The CNU burst transmission begins with a start burst marker (see 101.4.4.8), which facilitates the detection of the start of an incoming data burst. When received at the CLT, the start burst marker enables FEC codeword alignment to the incoming data stream, even in the presence of bit errors. The start burst marker is not part of the first FEC codeword but is added by the PMA.

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The CNU burst ends with the end burst marker (see 101.4.4.8), which facilitates the detection of the end of the current data burst. When received at the CLT, the end burst marker allows for the rapid reset of the CLT FEC synchronizer, so that it can search for the next burst. The end burst marker is not part of the last FEC codeword but is added by the PMA.

101.3.2.5.4 Upstream FEC encoding

Upstream bursts in EPoC are variable in length and may contain more than one MAC frame. The upstream makes use of three different LDPC codeword sizes as described Table 101–2. Each codeword size has a specific, associated US filling threshold F_T.

Starting with a 16200 (long) codeword:

1) If the number of available 65-bit blocks (Bin) is sufficient to fill a long FEC codeword ($B_Q \geq 220$), create a long FEC codeword. If Bin ≥ 220, is true repeat step 1).
2) If 220 > Bin ≥ 101, create a shortened long FEC codeword.
3) If 101 > Bin ≥ 76, create a medium FEC codeword.
4) If 76 > Bin ≥ 25, create a shortened medium FEC codeword.
5) If 25 > Bin ≥ 12, create a shortened FEC codeword. If Bin ≥ 12, is true repeat step 5).
6) If 12 > Bin ≥ 1, create a shortened short FEC codeword.

101.3.2.5.5 Constants

FEC_DS_CodeWordSize
: TYPE: 16-bit integer
The fixed size, in bits, of the downstream FEC codeword.
Value: 16140

SH_CTRL
: See 76.3.2.5.2.

SH_DATA
: See 76.3.2.5.2.

101.3.2.5.6 Variables

blockCount
: TYPE: 16-bit unsigned integer
This variable represents the number of 65-bit blocks input to the FEC Encoder.

B_P
: TYPE: 16-bit unsigned integer
VALUE: see Table 101–2
This variable represents the number of padding bits within the payload portion of the FEC codeword.

B_Q
: TYPE: 16-bit unsigned integer
VALUE: see Table 101–2
This variable represents the number of 65-bit blocks within the payload portion of the FEC codeword.

burstEnd
: TYPE: Boolean
When TRUE this flag signals the end of burst.

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burstStart

TYPE: Boolean
When TRUE this flag signals the start of a burst.

CLK

TYPE: Boolean
This variable is TRUE on every negative edge of *TX_CLK* (see 46.3.1) and represents instances of time at which a 66-bit block is passed from the output of the 64B/66B Encoder into the FEC Encoder. This variable is reset to FALSE upon read.

dataPayload<F_P–1:0>

TYPE: Bit array
This array represents the payload portion of the FEC codeword, accounting for the necessary padding. It is initialized to the size of F_P bits and filled with the binary value of "0".

dataParity<F_R–1+B_P:0>

TYPE: Bit array
This array represents the parity portion of the FEC codeword, accounting for the necessary padding. It is initialized to the size of F_R bits and filled with the binary value of "0".

DelayBound

See 101.3.2.1.2.

DS_DataRate

See 100.3.2.1.

FIFO_FEC_TX

TYPE: Array of 65-bit blocks
A FIFO array used to store 65-bit blocks, inserted by the input process and retrieved by the output process in the FEC Encoder (see Figure 101–11, Figure 101–12, and Figure 101–13). The size of FIFO_FEC_TX buffer in the 10GPASS-XR PCS is set to 29 = ceil((1800+40)/65).

firstcodeword

TYPE: Boolean
When TRUE this flag signals the first codeword of a burst.

F_P

TYPE: 16-bit unsigned integer
VALUE: see Table 101–2
This variable represents the number of bits within the payload portion of the FEC codeword.

F_R

TYPE: 16-bit unsigned integer
VALUE: see Table 101–2
This variable represents the number of bits within the parity portion of the FEC codeword.

IdleBlockCount

TYPE: 32-bit signed integer
The number of consecutive non-data 65-bit blocks ending with the most recently received block. The non-data 65-bit blocks are represented by sync header 0 (binary).

lastcodeword

TYPE: Boolean
When TRUE this flag signals the last codeword of a burst.

loc

TYPE: 16-bit unsigned integer
This variable represents the position within the given bit array.

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Short2Payload<F_C–1:0>
TYPE: bit array
This bit array is used as a temporary buffer for the second short codeword in the Check_datapayload() function.

Short2blockCount
TYPE: 16-bit unsigned integer
This variable is used as a temporary to hold the *blockCount* of *Short2Payload<>*.

sizeFifo
TYPE: 16-bit unsigned integer
This variable represents the number of 65-bit blocks stored in the FIFO.

Transmitting
TYPE: Boolean
When TRUE this variable indicates the device is transmitting. At the CNU, the default value of *Transmitting* is FALSE. At the CLT, this variable is always set to TRUE except when *PD_Enable* is FALSE (see 102.2.7.3).

tx_coded<65:0>
TYPE: 66-bit block
This 66-bit block contains 64B/66B encoded data from the output of the 64B/66B Encoder. The format for this data block is shown in Figure 49–7. The left-most bit in the figure is *tx_coded<0>* and the right-most bit is *tx_coded<65>*.

tx_coded_out<F_C–1:0>
TYPE: bit array
This bit array contains the output of the FEC Encoder being passed to the Data Detector. The left-most bit is *tx_coded_out<0>* and the right-most bit is *tx_coded_out<F_C–1>*.

txCount
TYPE: 16-bit unsigned integer
This variable is used for counting bits in the Transfer to PMA process.

US_DataRate
See 100.3.2.2.

xfrSize
TYPE: integer
This variable is set as input to the transferToPMA process and indicates the number of bits in the ARRAY_IN.

101.3.2.5.7 Functions

BurstTimeHeader()
The BurstTimeHeader() function returns a 65-bit vector with the following values:
bit <0> = binary 1
bits<1:32> = the current PHY Link timestamp
bits<33:64> = a fixed value of 0xD858E4AB.
This 65-bit vector is transmitted as the first 65-bit block of an upstream burst.

Calculate_CRC40_and_3Parity(paritySize)
This function takes an argument of “LONG”, “MEDIUM”, or “SHORT” and then processes *dataPayload* and *tx_coded_out* to add CRC40 and appropriate LDPC parity. The *tx_coded_out* array is then passed to transferToPMA() with indicated length and *lastcodeword* status.

```
Function Calculate_CRC40_and_3Parity( paritySize ) {

    IF (paritySize == LONG)
```


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```
        parityLength = 1800;
    IF (paritySize == MEDIUM)
        parityLength = 900;
    IF (paritySize == SHORT)
        parityLength = 280;

    dataPayload<loc+39:loc> = calculateCrc(dataPayload<loc-1:0>);
    tx_coded_out<loc+39:loc> = dataPayload<loc+39:loc>;
    loc += 40;
    dataParity<parityLength-1:0> =
        calculateParity(dataPayload<loc-1:0>, loc, paritySize);
    tx_coded_out<loc+parityLength-1:loc> = dataParity<parityLength-1:0>;
    xfrSize += parityLength;
    transferToPMA(tx_coded_out, xfrSize, lastcodeword);

    // Setup for next codeword in burst if more data
    firstcodeword = FALSE;
    loc = 0;
    resetArray(dataPayload);
    resetArray(dataParity);
}
```

calculateCrc (ARRAY_IN)

This function calculates a CRC40 value for data included in ARRAY_IN (see 101.3.2.3).

calculateParity(ARRAY_IN , Length, paritySize)

This function calculates the LDPC parity (for the code per Table 101–2) for data included in ARRAY_IN up to the specified Length (bits). For any Length less than F_P, any remaining bits in ARRAY_IN after Length are considered padding bits (of length B_P bits) and will not be included in the encoder output producing a shortened codeword; i.e., codeword length will be $F_P - B_P + F_R$. When paritySize is "LONG", the values for the downstream or upstream codeword size of 16200 are used; for "MEDIUM" the values for the upstream codeword size of 5940 are used; and for "SHORT" the values for the upstream codeword size of 1120 are used.

Check_dataPayload(firstcodeword, lastcodeword)

This function performs the upstream codeword filling algorithm examining accumulated *blockCount* as per 101.3.2.5.4. This function calls Calculate_CRC40_and_3Parity() indicating the appropriate codeword size to use, as appropriate.

```
Function Check_dataPayload( firstcodeword, lastcodeword ) {

    IF (lastblock == FALSE) {
        IF (blockCount == 220 )
            Calculate_CRC40_and_3Parity(LONG);
    } ELSE {
        IF (blockCount < 200 && blockCount >= 101)
            Calculate_CRC40_and_3Parity(LONG);
        IF (blockCount < 101 && blockCount >= 76)
            Calculate_CRC40_and_3Parity(MEDIUM);
        IF (blockCount < 76 && blockCount >= 25)
            Calculate_CRC40_and_3Parity(MEDIUM);
        IF (blockCount < 24 && blockCount > 12) {
            // dataPayload<> contains two short codewords
            // first is 12 blocks, second is remainder
            Short2blockCount = blockCount - 12;
            Short2Payload<Short2loc:0> = dataPayload<loc:12*65>;
            loc = (12*65) - 1;
            blockCount = 12;
            Calculate_CRC40_and_3Parity(SHORT);
```


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```
            dataPayload<Short2loc:0> = Short2Payload<Short2loc:0>;
            tx_coded_out<Short2loc:0> = Short2Payload<Short2loc:0>;
            loc = (Short2blockCount * 65) – 1;
            blockCount = Short2blockCount;
            Calculate_CRC40_and_3Parity(SHORT);
         } ELSE IF ( blockCount >= 1 ) {
            Calculate_CRC40_and_3Parity(SHORT);
         }
      return();
   };
```

resetArray(ARRAY_IN)

This function resets the content of ARRAY_IN, removing all the elements within ARRAY_IN and setting its size to 0.

removeFifoHead(ARRAY_IN)

This function removes the first block in ARRAY_IN and decrements its size by 1.

```
   Function removeFifoHead( ARRAY_IN ){
            ARRAY_IN[0] = ARRAY_IN[1];
            ARRAY_IN[1] = ARRAY_IN[2;]
            ...
            ARRAY_IN[sizeFifo-2] = ARRAY_IN[sizeFifo-1];
            sizeFifo --;
   }
```

transferToPMA(ARRAY_IN, xfrSize, lastcodeword)

This function serially transfers a PCS FEC output codeword that is represented as bits in ARRAY_IN to the PMA using the PMA_UNITDATA.request() service primitive. Rate clocking is provided by the PMA service primitive. In the downstream direction, the PCS continuously provides codewords for transfer. For the first bit of the downstream codeword transfer, *burstStart* is set to TRUE and set to FALSE otherwise; for the last bit, *burstEnd* is set to TRUE, and set to FALSE otherwise. In the upstream direction, the PCS builds an upstream burst that consists of one or more concatenated codewords, where the length of each burst is based on MPCP scheduling. For the first bit of the first codeword of the upstream transfer, *burstStart* is set to TRUE and set to FALSE otherwise; for the last bit of the last codeword of the burst, *burstEnd* is set to TRUE and set to FALSE otherwise. The *burstStart* and *burstEnd* flags are used by the respective PMA symbol mapping functions (see 101.4.3.8 and 101.4.4.5). In the CLT the lastcodeword argument to this function is always TRUE (see Figure 101–12). This function is represented by the following pseudo code:

```
   Function transferToPMA( ARRAY_IN, xfrSize, lastcodeword) {
   burstStart = FALSE;
   burstEnd   = FALSE;
      for ( txCount = 0; txCount < xfrSize; txCount++) {
         if (txCount == 0)
            burstStart = TRUE;
         if ((txCount == (xfrSize-1)) && (lastcodeword == TRUE))
            burstEnd = TRUE;
         PMA_UNITDATA.request(ARRAY_IN[txCount], burstStart, burstEnd)
      }
   }
```


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101.3.2.5.8 State diagrams

The CLT and the CNU shall implement the Data Detector input process as depicted in Figure 101–11. The CLT shall implement the Data Detector output process as depicted in Figure 101–12. The CNU shall implement the Data Detector output process as depicted in Figure 101–13.

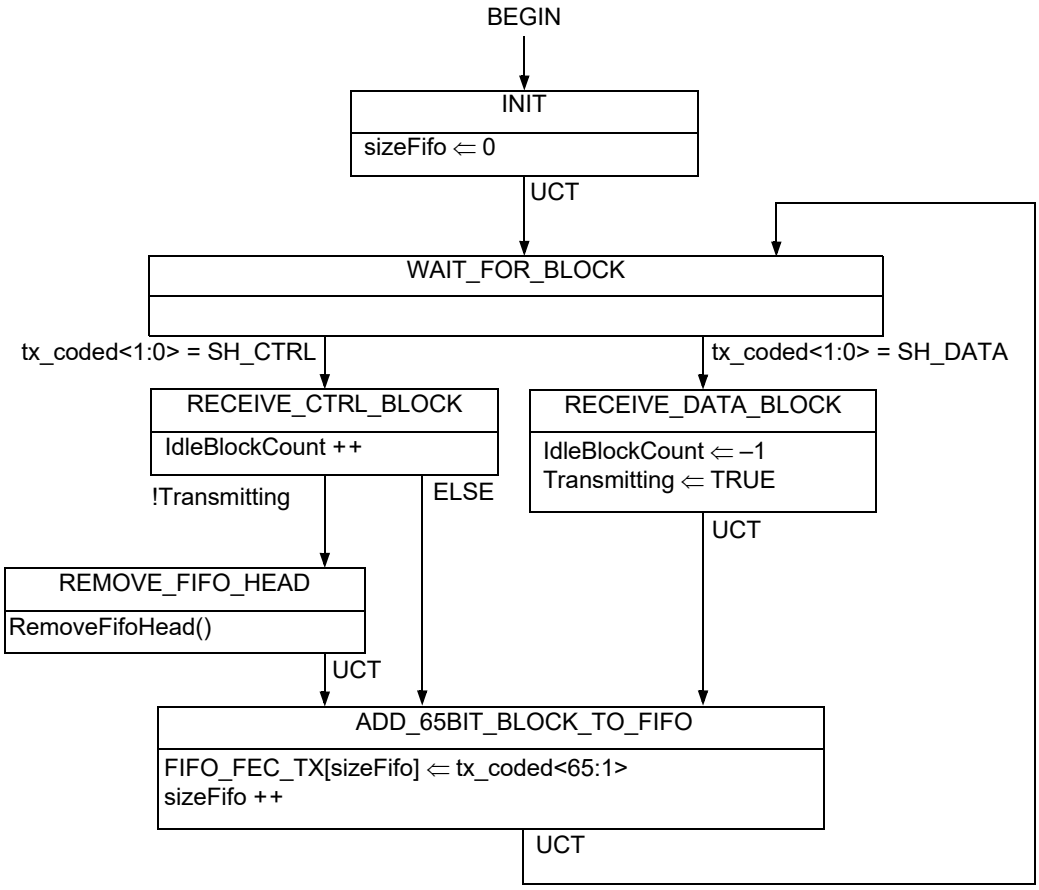

Figure 101–11— FEC Encoder and Data Detector input process state diagram

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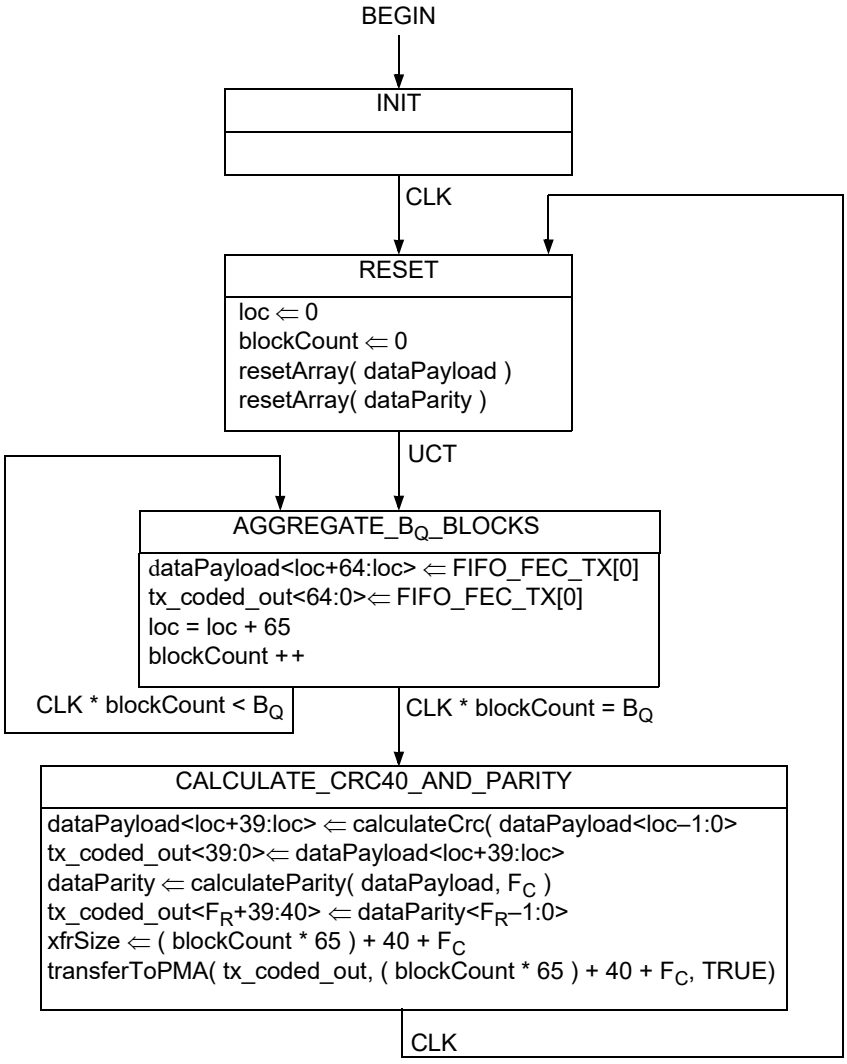

Figure 101–12—CLT FEC Encoder and Data Detector output process state diagram

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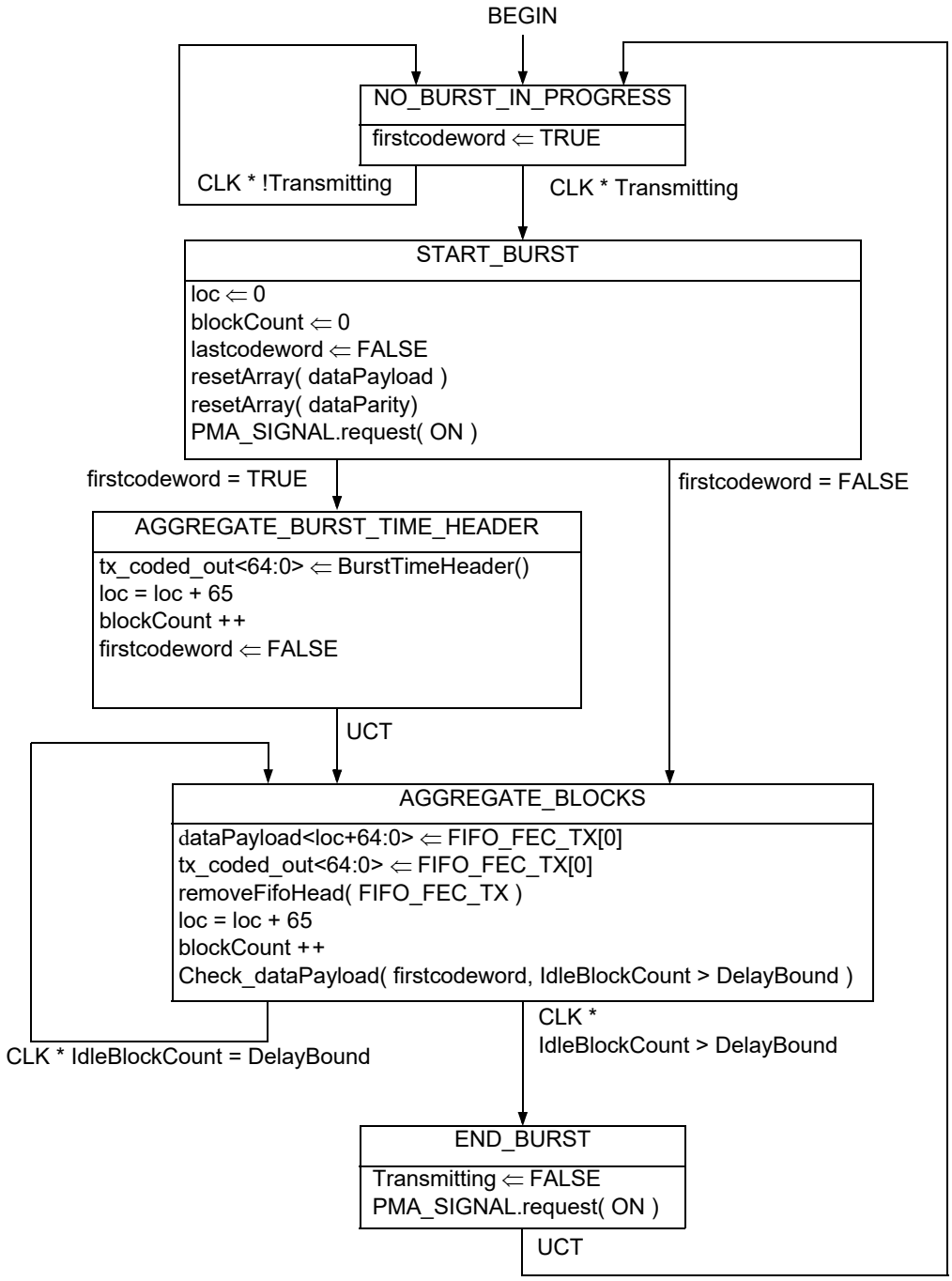

Figure 101–13—CNU FEC Encoder and Data Detector output process state diagram

101.3.3 PCS receive function

In the CLT, the PCS receive function operates in a burst fashion at the data rate of up to 10 Gb/s. In the CNU, the PCS receive function operates in a continuous fashion at the data rate of up to 10 Gb/s. Receive

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direction functional block diagrams for the CLT and CNU are illustrated in Figure 101–3 and Figure 101–4, respectively.

In the receive direction, the EPoC PCS includes a mandatory FEC Decoder, followed by a 64B/66B Decoder and an Idle control character insertion function performing the function of data rate adaptation and an FEC overhead compensation.

101.3.3.1 FEC Decoder

The 10GPASS-XR PHY decodes the received data using LDPC (F_C, F_P) code. The CLT 10GPASS-XR PCS operating on a CCDN shall decode the received data using one of the LDPC (F_C, F_P) codes per Table 101–2. The CNU 10GPASS-XR PCS operating on CCDN shall decode the received data using LDPC (16200, 14400) code per Table 101–2.

101.3.3.1.1 Upstream FEC decoding

The CLT receives an upstream burst with a length of R bits from a CNU via the PMA Client.

Start with B_Q = 220, CRC = 40, and F_R = 1800 for long codewords:

1) If $R \geq B_Q * 65 + 40 + F_R$ bits, decode a long codeword.
   Repeat and decode using long codewords if remaining bits $\geq B_Q * 65 + 40 + F_R$ bits.
   End processing burst if remaining bits ≤ 0.
2) If remaining bits < (B_Q = 220) * 65 + 40 + (F_R = 1800) and ≥ (B_Q = 101) * 65 + 40 + (F_R = 1800), decode a shortened long codeword.
   End processing burst if remaining bits ≤ 0.
3) If remaining bits ≥ (B_Q = 76) * 65 + 40 + (F_R = 900), decode a medium codeword.
   End processing burst if remaining bits ≤ 0.
4) If remaining bits < (B_Q = 76) * 65 + 40 + (F_R = 900) and ≥ (B_Q = 25) * 65) + 40 + (F_R = 900), decode a shortened medium codeword.
   End processing burst if remaining bits ≤ 0.
5) If remaining bits ≥ (B_Q = 12) * 65 + 40 + (F_R = 280), decode a short codeword.
   Repeat and decode using short codewords if remaining bits ≥ (B_Q = 12) * 65 + 40 + (F_R = 280) bits.
   End processing burst if remaining bits ≤ 0.
6) If remaining bits ≥ 65 + 40 + 280, decode a shortened short codeword.
7) If remaining bits, declare receiver burst error.

All codeword decoding follows the same procedures as the downstream with the following differences:

— The appropriate values from Table 101–2 are used for the corresponding codeword size being decoded.
— The *burstStart* indication in the PMA_UNITDATA.indication() corresponds to the first bit in the concatenated burst received from a CNU.
— The *burstEnd* indication in the PMA_UNITDATA.indication() corresponds to the last bit of the concatenated burst received from a CNU.
— The nominal data rate of the PMA_UNITDATA_request() is *US_DataRate* calculated by the CLT (see 100.3.2.2).

101.3.3.1.2 LDPC decoding process within CNU (downstream)

The process of decoding FEC codewords in the 10GPASS-XR CNU receiver is illustrated in Figure 101–14.

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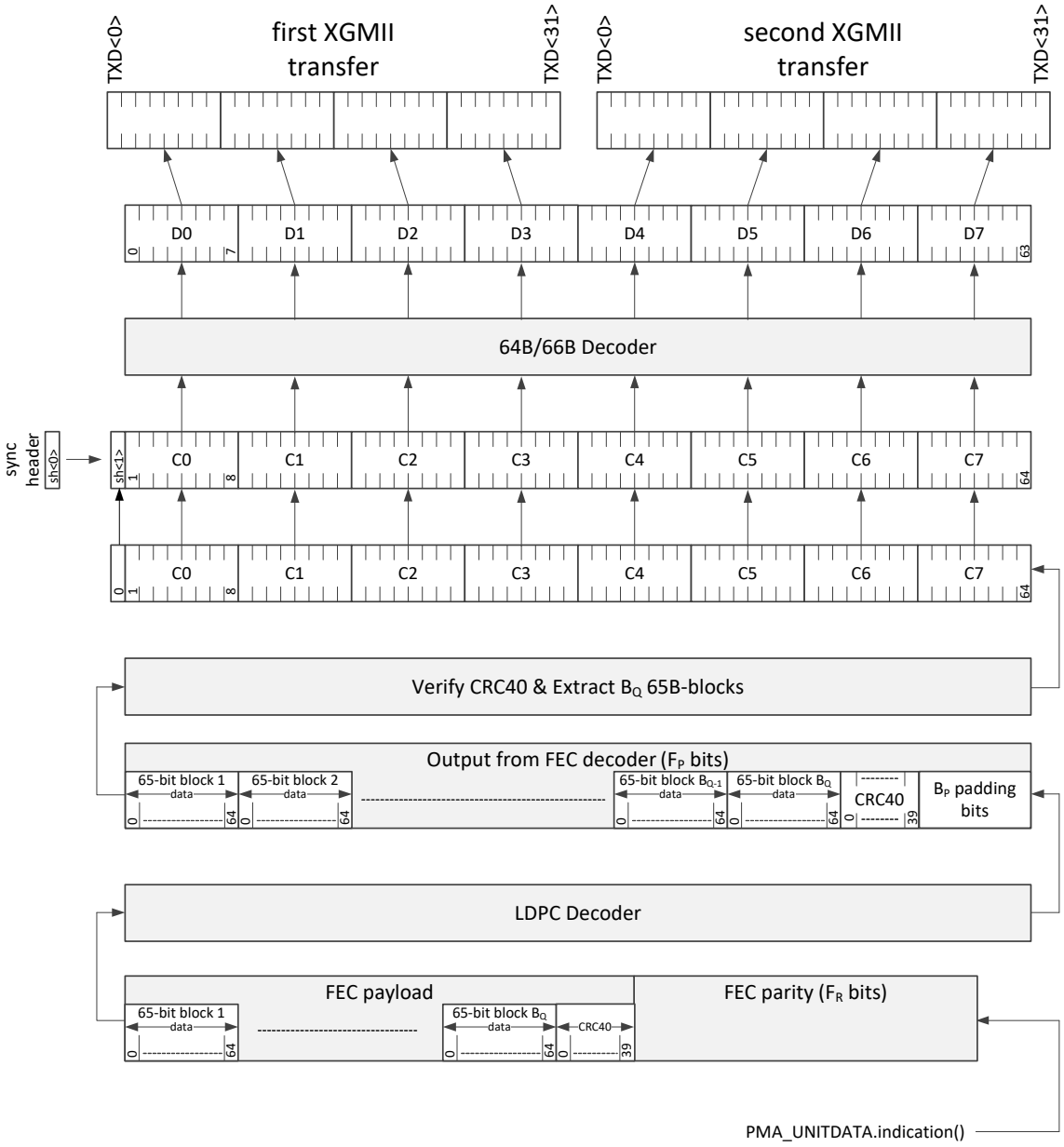

Figure 101–14—PCS receive path processing

Once the alignment to the FEC codeword is found, the 10GPASS-XR CNU receiver aggregates a total of FEC_DS_CodeWordSize bits received from the descrambler as input to the FEC Decoder. The output of the FEC Decoder contains the full FEC Payload consisting of 65-bit blocks number 1 to B_Q, the CRC40 data, and B_P padding bits with all bits set to the binary value of "0".

The FEC Decoder produces the FEC payload portion of the codeword with the size of F_P (in bits), where bits $<F_P - B_P - 1>$ ... $<F_P - 1>$ contain padding (with the binary value of "0"). Next, the CRC40 is calculated over the remaining 65-bit blocks 1 through B_Q and then compared with the value of CRC40 retrieved from the received FEC codeword. If both CRC40 codes match, the decoded FEC codeword is treated as error-free. Otherwise, the decoded FEC codeword is treated as errored.

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Finally, the FEC Decoder prepends each of the B_Q 65-bit blocks with bit <0> of the sync header containing the binary inverse of the value carried in bit <1> of the sync header, producing 66-bit blocks. This also guarantees that properly decoded blocks meet the requirements of 49.2.4.3.

The FEC Decoder maintains error monitors to detect FEC codeword successes and failures. See 101.3.3.1.4 for details.

Each resulting 66-bit block is then fed into the 64B/66B Decoder, removing the sync header information (bit <0> and bit <1>), which is used to generate control signaling for the XGMII. Finally, the resulting 64-bit block is then separated into two 32-bit portions, which are transmitted across the XGMII on two consecutive transfers, with the proper control signaling retrieved from the sync header information retrieved in the 64B/66B Decoder.

101.3.3.1.3 LDPC decoding process within CLT upstream

In the Verify CRC40 and Extract B_Q 65B Blocks function of the upstream receiver, the CLT will remove the first 65-bit block of a burst containing the Burst Time Header, the remainder of the 65-bit blocks will be passed to the 64B/66B Decoder. The 32-bit PHY Link timestamp value will be extracted. The use of this timestamp in the upstream receiver processing is implementation specific and beyond the scope of this standard. This timestamp is provided as a mechanism to minimize any jitter introduced by OFDMA framing and the 1D to 2D insertion and extraction mechanisms. For example, an implementation may implement a timestamp-based burst play out buffer prior to passing any frames contained within a burst to the XGMII.

101.3.3.1.4 Codeword error monitor

The FEC Decoder shall provide a user-configurable option (variable *CRC40ErrCtrl*) to indicate an uncorrectable FEC codeword to higher layers. If *CRC40ErrCtrl* is TRUE and the calculated value of CRC40 does not match the value of CRC40 retrieved from the received FEC codeword, the FEC Decoder replaces bit <0> and <1> in the sync headers in the first 64B/66B block and every eighth 64B/66B block, (1st, 9th, 17th, 25th, etc.) as well as the last 64B/66B block from the errored FEC codeword with the binary value of "11". The state table for replacing the sync header bits is shown in Table 101–6. For EPoC, the BER monitor state machine as defined in Clause 49 is disabled.

Table 101–6—Sync header decoding state table

		CRC40ErrCtrl	
		FALSE	**TRUE**
CRC40	matches	Pass SH as received	Pass SH as received
	does not match	Pass SH as received	Replace SH with "11"

101.3.3.1.5 Constants

IDLE

TYPE: 66-bit vector
This constant represents /I/ character with 64B/66B encoding, as defined in 49.2.4.7.

XGMII_Rate

See 101.3.2.1.1.

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101.3.3.1.6 Variables

blockCount
: See 101.3.2.5.5.

B_P
: See 101.3.2.5.5.

B_Q
: See 101.3.2.5.5.

CLK
: See 101.3.2.5.5.

CRC40ErrCtrl
: TYPE: Boolean
This variable controls the processing of codewords that fail the CRC40 checksum test. See 101.3.3.1.4.

dataInSize
: TYPE: 16-bit unsigned integer
VALUE: $(B_Q + 1) \times 65 + 40 + B_P$
This variable represents the size of the *dataIn* array in bits, containing the combination of the payload portion of the FEC codeword ($(B_Q + 1) \times 65$), the CRC40 (40), and the parity portion of the FEC codeword (B_P).

dataCrcA<39:0>
: TYPE: Bit array
This array represents the CRC40 recovered from the payload portion of the FEC codeword prior to the FEC decoding process. This array is initialized to the size of 40 bits and filled with the binary value of "0".

dataCrcB<39:0>
: TYPE: Bit array
This array represents the CRC40 calculated over B_Q 65-bit blocks in the payload portion of the FEC codeword after the FEC decoding process. This array is initialized to the size of 40 bits and filled with the binary value of "0".

dataIn<dataInSize–1:0>
: TYPE: Bit array
This array represents the combination of the payload portion of the FEC codeword, the parity portion of the FEC codeword, CRC40, and all the necessary padding. It is initialized to the size of *dataInSize* bits and filled with the binary value of "0".

dataOut<F_P–1:0>
: TYPE: Bit array
This array represents the combination of the payload portion of the FEC codeword, CRC40, and all the necessary padding. It is initialized to the size of F_P bits and filled with the binary value of "0".

FecCodeWordCount
: TYPE: 32-bit unsigned integer
This variable is incremented for every received FEC codeword. After reaching 0xFF-FF-FF-FF, this variable is set to 0x00-00-00-00.

FecCodeWordFail
: TYPE: 32-bit unsigned integer
This variable is incremented for every received FEC codeword for which the decoding process failed. After reaching 0xFF-FF-FF-FF, this variable is set to 0x00-00-00-00.

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FecCodeWordSuccess
TYPE: 32-bit unsigned integer
This variable is incremented for every received FEC codeword for which the decoding process completes successfully. After reaching 0xFF-FF-FF-FF, this variable is set to 0x00-00-00-00.

FIFO_FEC_RX
TYPE: Array of 66-bit blocks
A FIFO array used to store tx_coded<65:0> blocks, inserted by the input process in the FEC Decoder, while encoded data is then sent to 64B/66B Decoder for processing and transmission towards the XGMII.

loc
See 101.3.2.5.5.

PMA_CLK
TYPE: Boolean
This variable is to TRUE on every negative edge of a clock that is synchronized to the PMA_UNITDATA.indication data rate of *DS_DataRate* (see 101.4.2.1). This variable is set to FALSE upon read. This variable is set to FALSE upon read.

rx_coded_in<64:0>
TYPE: 65-bit block
This 65-bit block contains the input into the FEC Decoder being passed from PMA. The left-most bit is *rx_coded_in<0>* and the right-most bit is *rx_coded_in<64>*.

rx_coded_in<F_C–1:0>
TYPE: bit array
This array contains the input into the FEC Decoder being passed from PMA. The left-most bit is *rx_coded_in<0>* and the right-most bit is *rx_coded_out<F_C–1>*.

rxCount
TYPE: 16-bit unsigned integer
This variable is used for counting bits in the Transfer from PMA process.

sizeFifoRx
TYPE: 16-bit unsigned integer
This variable represents the number of 65-bit blocks stored in the FIFO.

syncFec
TYPE: Boolean
This variable indicates whether the FEC codeword alignment was found (value equal to TRUE) or not (value equal to FALSE).

tx_coded<65:0>
See 101.3.2.5.5.

101.3.3.1.7 Functions

calculateCrc (ARRAY_IN)
See 101.3.2.5.5.

decodeFec(ARRAY_IN, Length)
This function performs FEC decoding (for the codeword per Table 101–2) for data included in ARRAY_IN, comprising the combination of the FEC payload portion, CRC40, and FEC Parity (F_R). Since the FEC Parity and CRC are of constant size, if Length < F_C, the FEC payload will be shortened by F_C – Length bits (considered as padding bits B_P). The output of the decoder will be of length F_P bits composed of the received FEC payload, the received CRC40, and the added B_P padding bits. The padding bits will be set to a binary value of 0.

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resetArray(ARRAY_IN)
See 101.3.2.5.5.

transferFromPMA(ARRAY_OUT)
This function invokes the Transfer From PMA process to transfer a downstream burst (codeword) from the PMA to the FEC Decoder.

101.3.3.1.8 State diagrams

The CLT PCS shall implement the transfer from PMA process as shown in Figure 101–15.

The CNU PCS shall implement the LDPC decoding process input process, and LDPC decoding output process as shown in Figure 101–16 and Figure 101–17, respectively.

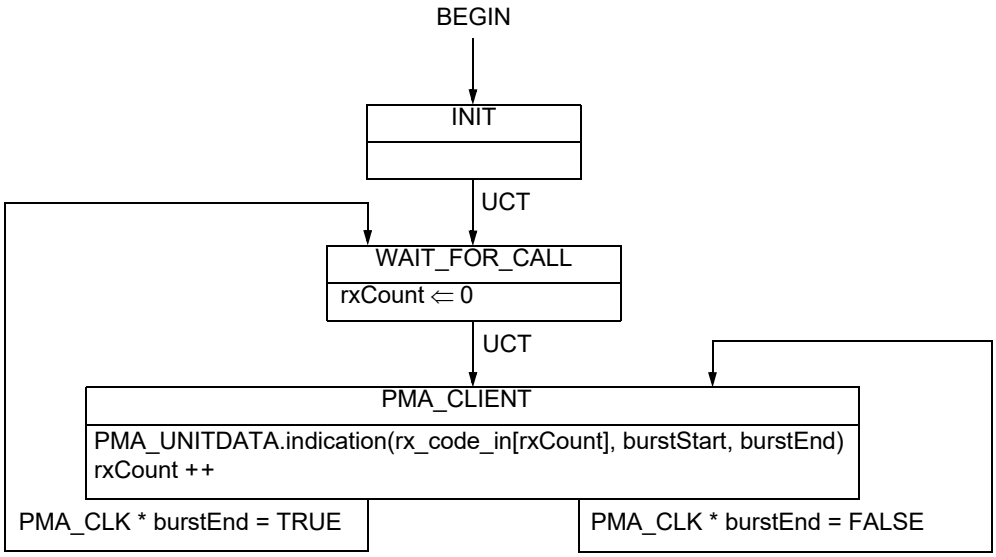

Figure 101–15—Upstream CLT transfer from PMA process state diagram

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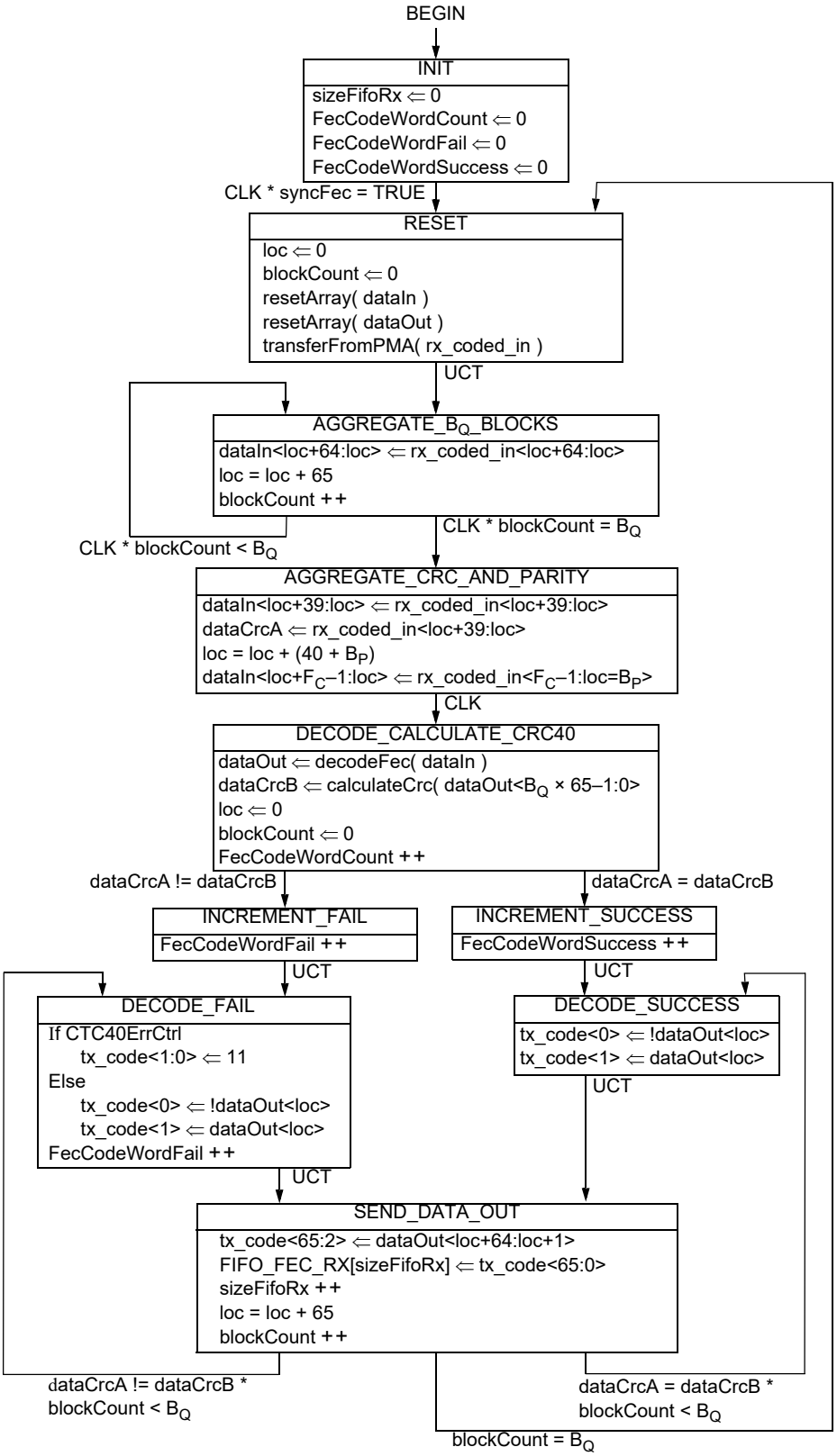

Figure 101–16—CNU FEC decoding input process state diagram

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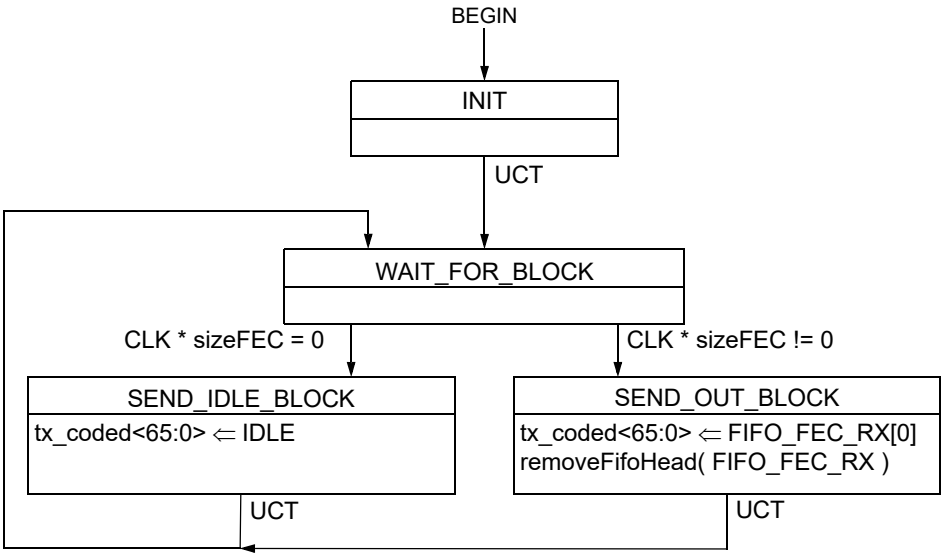

Figure 101–17—FEC Decoder, output process state diagram (CNU)

101.3.3.2 64B/66B Decoder

The EPoC PHY utilizes a 64B/66B Decoder based on that described in 49.2.11 with several important differences. The EPoC 64B/66B Decoder does not include a descrambler function as described in 49.2.10 and the input is a 65B block with a single sync header bit. The state diagram found in Figure 49–17 is followed after the addition of sync header bit <0> as illustrated in Figure 101–14.

101.3.3.3 Idle control character insertion process

In the receiving PCS, the Idle control character insertion process inserts Idle control characters into the data stream with gaps as received from the FEC Decoder and 64B/66B Decoder, adjusting the effective PCS and PMD data rate to the data rate expected by the MAC Control (as defined in Clause 103). Effectively, the Idle control character insertion process fills in the gaps created after the removal of FEC parity data, as well as compensates for the derating of the EPoC PMD relative to the EPoC MAC.

The Idle control character insertion process (see Figure 101–18) is composed of the following:

a) A receive process, receiving 72-bit vectors from the 64B/66B Decoder and writing them into the Idle Insertion FIFO (called FIFO_II); and

b) A transmit process, reading 72-bit vectors from FIFO_II and transferring them to the XGMII.

The receive process receives 72-bit vectors from the 64B/66B Decoder at a slower data rate than the nominal XGMII data rate for the following two reasons:

1) The FEC parity data is removed within the FEC Decoder, leaving behind gaps in the data stream; and

2) The data rate supported by EPoC PCS and PMD is lower than the data rate expected by MAC Control Client, requiring data rate adaptation between the PCS and MAC.

The transmit process outputs 72-bit vectors at the nominal XGMII data rate.

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To match the difference in data rates between the receive process and the transmit process, the Idle control character insertion process inserts additional 72-bit vectors containing Idle control characters. The additional blocks are inserted between frames and not necessarily at the same locations where FEC parity data was removed within the FEC Decoder.

101.3.3.3.1 Constants

IDLE_VECTOR
: TYPE: 72-bit binary array
This constant represents a 72-bit vector containing Idle control characters.

LBLOCK_R
: This constant is defined in 49.2.13.2.1.

101.3.3.3.2 Variables

BEGIN
: TYPE: Boolean
This variable is used when initiating operation of the state diagram. It is set to TRUE following initialization and every reset.

FIFO_II
: TYPE: Array of 72-bit vectors
The FIFO_II buffer is used to perform data rate adaptation between XGMII data rate and the EPoC PMD data rate. Upon initialization, all elements of this array are filled with instances of IDLE_VECTOR. The FIFO_II buffer has the size of *FIFO_II_SIZE* (see 101.3.3.3.1).

FIFO_II_SIZE
: TYPE: 16-bit unsigned integer
This variable represents the size of Idle Insertion FIFO buffer. The size of this buffer is selected in such a way that it is able to accommodate the number of 66-bit vectors sufficient to fill the gap introduced by removing the FEC parity data for a maximum size MAC frame, and compensate for the maximum supported difference between the MAC rate and PMD rate. *FIFO_II_SIZE* is dependent on the line rate the PHY is operating at and may need to be adjusted whenever the profile is changed.

RX_CLK
: TYPE: Boolean
This variable represents the *RX_CLK* signal defined in 46.3.2.1.

rx_raw_in<71:0>
: TYPE: 72-bit binary array
This variable represents a 72-bit vector received from the output of the 64B/66B Decoder. *RXD*<0> through *RXD*<31> for the second transfer are placed in *rx_raw*<40> through *rx_raw*<71>, respectively.

rx_raw_out<71:0>
: TYPE: 72-bit binary array
This variable represents a 72-bit vector passed from the Idle control character insertion process to XGMII. The vector is mapped to two consecutive XGMII transfers as follows:
Bits *rx_raw*<3:0> are mapped to *RXC*<3:0> for the first transfer.
Bits *rx_raw*<7:4> are mapped to *RXC*<3:0> for the second transfer.
Bits *rx_raw*<39:8> are mapped to *RXD*<31:0> for the first transfer.
Bits *rx_raw*<71:40> are mapped to *RXD*<31:0> for the second transfer.

countVector
: TYPE: 16-bit unsigned integer

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This variable represents the number of 72-bit vectors stored in the *FIFO_II* at the given moment of time.

101.3.3.3.3 Functions

T_TYPE(*rx_raw*<71:0>)
This function is defined in 49.2.13.2.3.

101.3.3.3.4 Messages

DECODER_UNITDATA.indicate(*rx_raw*_in<71:0>)
A signal sent by the EPoC PCS Receive process, conveying the next received 72-bit vector.

DUDI
Alias for DECODER_UNITDATA.indicate(*rx_raw*_in<71:0>).

101.3.3.3.5 State diagrams

The CLT and CNU PCS shall perform the Idle control character insertion process as shown in Figure 101–18.

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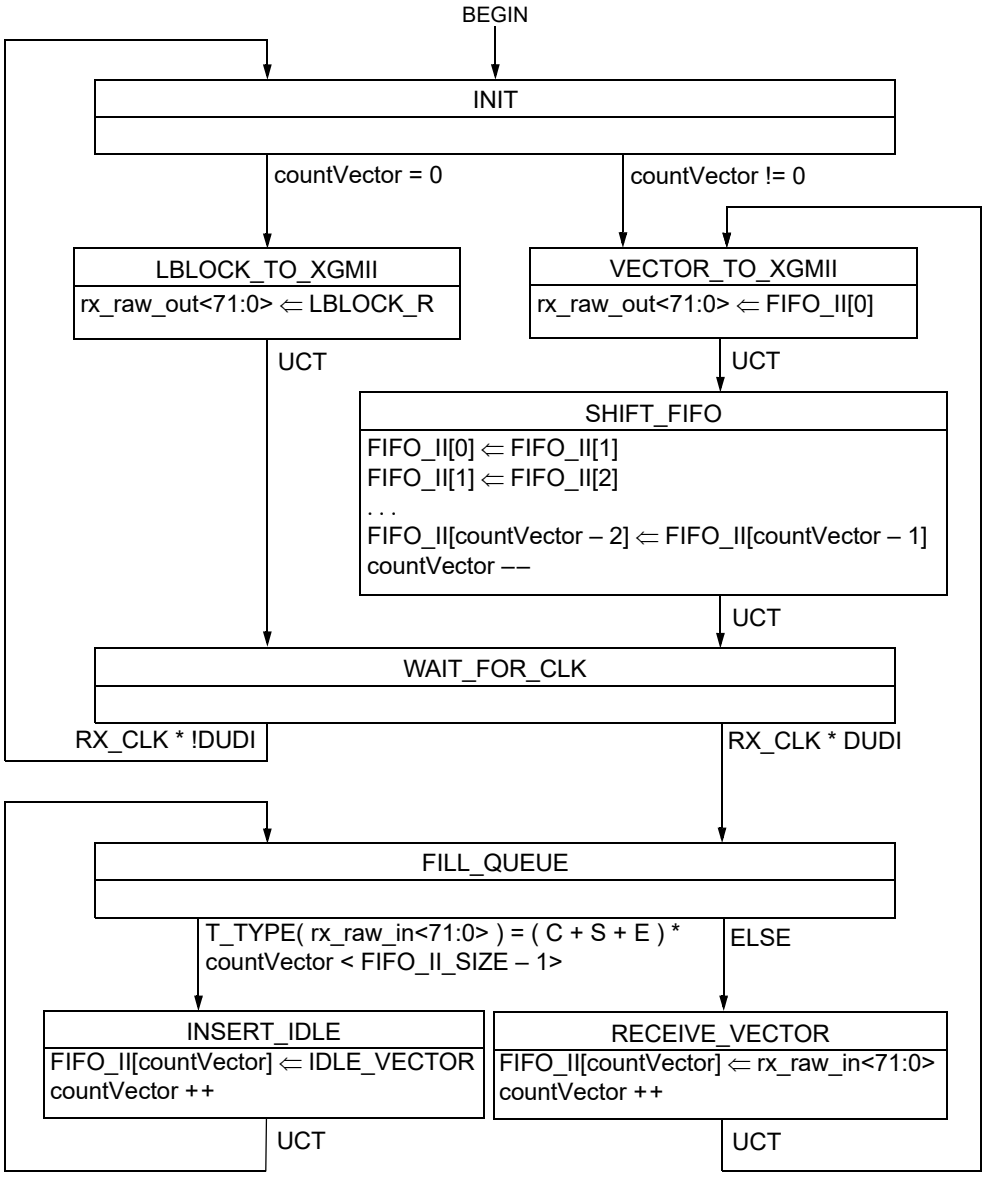

Figure 101–18—Idle control character insertion process state diagram

101.4 10GPASS-XR PMA

101.4.1 Overview

This subclause defines the Physical Media Attachment (PMA) for 10GPASS-XR, supporting operation over the point-to-multipoint coaxial cable distribution networks. The 10GPASS-XR PMA is specified to support the operation of up to 10 Gb/s in the downstream direction and up to 1.6 Gb/s in the upstream direction, where the upstream and downstream data rates are configured independently.

Figure 101–5 shows the relationship between the 10GPASS-XR PMA sublayer and the ISO/IEC OSI reference model. Figure 101–1 illustrates the CLT transmitter functional block diagram, including the PMA,

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while Figure 101–2 illustrates the CNU transmitter functional block diagram. Figure 101–3 and Figure 101–4 illustrate the functional block diagram of the receive path in the CLT and CNU, respectively in the 10GPASS-XR PMA.

The transmit PMA sublayer translates a serial data stream into a stream of I/Q value pair and channel number using the following functions: data scrambler, symbol mapper, interleaver (CLT only), Pilot Insertion, Inverse Discrete Fourier Transform (IDFT), and Cyclic Prefix insertion. The receive PMA sublayer translates a stream of I/Q value pair and channel number into a serial data stream using the following functions: Fast Fourier Transform (FFT), equalization, Pilot processing, de-interleaver (CNU only), symbol de-mapper, and data descrambler.

101.4.2 PMA Service Interface

The EPoC PMA provides a Service Interface to the 10GPASS-XR PCS sublayer, i.e., the PMA client. These services are described in an abstract manner and do not imply any particular implementation. The PMA Service Interface shall support the exchange of data between the PMA and the PMA client.

The PMA inputs serial data from the PCS and, after processing, passes serial data to the PMD and vice versa. It also generates an additional status indication for use by its client.

The following primitives are defined:
PMA_UNITDATA.request(tx_data_bit<bit>, *burstStart*, *burstEnd*)
PMA_UNITDATA.indication(rx_data_bit<bit>, *burstStart*, *burstEnd*)

101.4.2.1 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of data bits) from the PMA client to the PMA and notifies the PMA of the start and the end of the data burst.

PMA_UNITDATA.request is generated by the PMA client's transmit process.

101.4.2.1.1 Semantics of the service primitive

PMA_UNITDATA.request(tx_data_bit<bit>, *burstStart*, *burstEnd*)

The data conveyed by PMA_UNITDATA.request is a single data bit which has been prepared for transmission by the PMA client. The Boolean variable *burstStart* is set to TRUE when the data bit is the first bit at the start of transmission burst, and is set to FALSE otherwise. The Boolean variable *burstEnd* is set to TRUE when the data bit is the last bit of a transmission burst, and is set to FALSE otherwise. In the downstream direction, the CLT transmission burst is composed of a single FEC codeword; whereas, in the CNU upstream, the burst may include one or more concatenated FEC codewords (see 101.3.2.5.3).

101.4.2.1.2 When generated

The PMA client continuously sends data bits to the PMA at a nominal rate of *DS_DataRate* in the downstream direction. In the upstream direction, the nominal rate is *US_DataRate* during a burst. Refer to 100.3.2.2.

NOTE 1—*DS_DataRate* is calculated by the PMA after the downstream PHY has been configured. It is based on the sum of the available data bits per subcarrier over the timespan of a downstream OFDM frame consisting of 128 modulation symbols. *DS_DataRate* is a constant during the span of the PHY configuration. If re-configured, *DS_DataRate* is re-calculated.

NOTE 2—*US_DataRate* is calculated by the PMA after the upstream PHY has been configured. It is based on the sum of the available data bits per Resource Element over the timespan of the upstream superframe consisting of 256 symbols

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plus 6 Probe Period symbols. *US_DataRate* is a constant during the span of the PHY configuration. If reconfigured, *US_DataRate* is recalculated.

101.4.2.1.3 Effect of receipt

Upon receipt of this primitive, the PMA Symbol Mapper transfers the data bit into the OFDM frame.

In the CLT and upon the start of a downstream OFDM frame and when *burstStart* is TRUE, the PMA Symbol Mapper updates the FEC Codeword Pointer (FCP) in the downstream PHY Link. See 101.4.3.8.

In the CNU, both *burstStart* and *burstEnd* parameters are used by the upstream Symbol Mapper for placing start and end burst markers, respectively, into the appropriate Resource Elements. See 101.4.4.8.

101.4.2.2 PMA_UNITDATA.indication

This primitive defines the transfer of data in the form of bits from the PMA to its client. PMA_UNITDATA.indication is used by the client's receive path process.

101.4.2.2.1 Semantics of the service primitive

PMA_UNITDATA.indication(rx_data_bit<bit>, *burstStart*, *burstEnd*)

The data conveyed by PMA_UNITDATA.indication is single data bit that has been prepared by the PMA receive process to the PMA client. The Boolean variable *burstStart* is set to TRUE when the data bit is the first bit at the start of received burst, and is set to FALSE otherwise. The Boolean variable *burstEnd* is set to TRUE when the data bit is the last bit of a received burst, and is set to FALSE otherwise.

101.4.2.2.2 When generated

The PMA sends one rx_data_bit <bit> to the PMA client corresponding to the receipt of each bit of received from the receiver Symbol De-Mapper.

In the CNU, the PMA continuously sends data bits to the PMA client at a nominal rate of *DS_DataRate* in the downstream direction. In the upstream direction, the nominal rate is *US_DataRate* during a burst. Refer to 100.3.2.1 and 100.3.2.2.

101.4.2.2.3 Effect of receipt

The effect of receipt of this primitive by the client is specified in 101.3.3.

101.4.3 Downstream PMA transmit function

101.4.3.1 Overview

The downstream PMA transmit functional diagram is shown in Figure 101–2. The PMA supports five 190 MHz wide OFDM channels; each containing 3800 active subcarriers. Each OFDM channel is associated with the following processing functions: Time and Frequency Interleaver (see 101.4.3.9), Pilot Insertion (see 101.4.3.10), IDFT (see 101.4.3.11), and cyclic prefix and Windowing (see 101.4.3.12). The outputs of each OFDM channel are digitally combined. All OFDM channels follow the same frame timing and use the same OFDM Clock (see 100.4.4), cyclic prefix size, and window size.

OFDM channel 1 shall always be enabled but is muted during RxMER testing (see 100.4.2). Optional OFDM channels 2, 3, 4, and 5 are enabled when configured for operation via the *DS_ChCnt* variable. When enabled, each OFDM channel is configured for placement in the downstream RF frequency band of the coax

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cable distribution network (see Figure 100–1). The encompassed spectrum of any OFDM channel does not overlap with that of any other OFDM channel. The tight time skew requirements (see Table 101–7) permit the active edge subcarrier of one OFDM channel to be placed immediately adjacent to that of the adjacent OFDM channel without any guard band. CLTs shall declare the number of downstream OFDM channels it supports via the *DS_OFDM_ChAbility* variable.

The Symbol Mapper distributes PCS data over all active subcarriers that are configured to carry data (subcarriers that are not configured as excluded are active subcarriers). See 101.4.3.8.

The PHY Link is processed by the OFDM channel 1 IDFT and cyclic prefix and Windowing functions.

101.4.3.2 Time and frequency synchronization

This subclause specifies the timing and frequency synchronization requirements for CLT transmitters and CNU receivers.

The purpose of this subclause is to help ensure that the CLT transmitter can provide proper timing and frequency references for EPoC downstream OFDM operation and that the CNU receiver can acquire the system timing and subcarrier from the downstream for proper EPoC operation.

The CLT downstream OFDM symbol and subcarrier frequency and timing relationship is defined in 101.4.3.3.

Tolerances for the downstream Subcarrier Clock frequency are specified in this subclause (Table 101–7). Downstream Subcarrier Clock frequency and downstream signal generation are detailed in 101.4.3.3. The Subcarrier Clock frequency tolerance performance is coupled to the phase noise requirements of Table 100–4 and the downstream OFDM Clock requirements as follows:

— Each cycle of the downstream Subcarrier Clock is 4096 cycles (50 kHz subcarrier spacing) of the downstream OFDM Clock frequency (which is nominally 204.8 MHz).
— The downstream Subcarrier Clock waveform is locked to the 10.24 MHz Master Clock frequency (see Table 100–3, 101.4.3.3, and Equation (101–6)).
— The downstream OFDM Clock jitter requirements in Table 101–7 shall apply equivalently to the downstream Subcarrier Clock and its harmonics.

NOTE—The requirements on the OFDM Clock are effectively measured on observables in the downstream waveform, which include the downstream Subcarrier Clock frequency (manifested in the subcarrier spacing) and downstream subcarrier frequencies.

CLT transmitters and CNU receivers shall conform to the requirements given in Table 101–7.

Table 101–7—Downstream time and frequency synchronization

Item	Requirement
OFDM Clock jitter	1) $< [-21 + 20\times\log_{10}(f_{DS}/204.8)]$ dBc (i.e., < 0.07 ns RMS) 10 Hz to 100 Hz 2) $< [-21 + 20\times\log_{10}(f_{DS}/204.8)]$ dBc (i.e., < 0.07 ns RMS) 100 Hz to 1 kHz where f_{DS} is the frequency of the measured downstream OFDM Clock in MHz.[a]
Inter-OFDM channel time skew	156.25 ns
CNU Timing Acquisition Accuracy	Better than 1 OFDM Clock period (1/204.8 MHz).
Acquisition time	< 60 seconds

[a] The CLT uses a value of f_{DS} that is an integral multiple or divisor of the downstream OFDM Clock frequency. For example, an f_{DS} = 409.6 MHz clock may be measured if there is no explicit 204.8 MHz clock available.

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The CLT shall lock the 204.8 MHz downstream OFDM Clock and downstream OFDM RF transmissions to the CLT 10.24 MHz Master Clock (Table 100–3).

Inter-OFDM channel time skew is defined as the maximum transmission time skew between any two OFDM channels.

The CNU timing acquisition accuracy for the downstream clock timing is defined with respect to downstream PHY Link frame. The CNU shall adjust its 10.24 MHz Master Clock to synchronize its own clock timing with PHY Link frame for proper operation. The CNU acquires downstream clock timing from the downstream signal (pilots, preambles, or mixed pilots, preambles, and data).

Downstream OFDM channel acquisition time for a CNU is defined as the time required for a single CNU with no previous network frequency plan knowledge to achieve downstream signal acquisition (frequency and time lock, see Table 101–7).

In addition to meeting the clock jitter requirements given previously, the CLT is required to meet the phase noise specifications defined in Table 100–4. In the event of a conflict between the clock jitter and the phase noise requirement, the CLT shall meet the more stringent requirement.

101.4.3.3 Subcarrier clocking

The synchronization of the Subcarrier Clock and subcarrier frequency are defined and characterized by the following rules:

— Each OFDM symbol is defined with an FFT duration (equal to Subcarrier Clock period) of 20 μs. For each OFDM symbol, the Subcarrier Clock period (μs) may vary from nominal with limits defined in Table 101–7.

— The number of OFDM Clock periods (1/204.8 MHz) of each subcarrier generated by the CLT during one period of the Subcarrier Clock is an integer number. The CLT Subcarrier Clock shall be synchronous with the 10.24 MHz Master Clock defined by the following:

$$SC_f = ((2 \times 10)/4096) \times MC_f \tag{101–6}$$

where
SC_f is the Subcarrier Clock frequency
MC_f is the 10.24 MHz Master Clock frequency (see Table 100–3)

— The limitation on the variation from nominal of the Subcarrier Clock frequency at the output connector is defined in 101.4.3.2.

— Each OFDM symbol has a cyclic prefix that is an integer multiple of 1/128th, of the Subcarrier Clock period.

— Each OFDM symbol duration is the sum of one Subcarrier Clock period and the cyclic prefix duration.

— The carrier frequency (i.e., the center frequency of the N-th subcarrier) is an integer multiple of the subcarrier spacing and may contain phase noise with limits defined in Table 100–4. The number of cycles for each subcarrier generated by the CLT during an OFDM symbol duration (Sym_T) shall be as given in Equation (101–7).

$$Sym_T = K + K \times L/128 \tag{101–7}$$

where
K is an integer equal to the nominal RF frequency of the subcarrier (Hz) divided by the nominal subcarrier spacing (Hz)
L is an integer related to the cyclic prefix as shown in Equation (101–8)

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$$L = 128 \times (DSNcp \times 10^{-6}) \times 50000 \quad (101–8)$$

101.4.3.4 Subcarrier configuration and bit loading

Each subcarrier in an OFDM channel is configured using the *DS_ModTypeSC(n)* variables (where $0 \le n \le 4095$) in conjunction with *DS_OFDM_ID*. The OFDM channel being configured is determined by *DS_OFDM_ID*. The *DS_ModTypeSC(n)* variables configure each subcarrier to be nulled, to be a continuous pilot, to have a specific bit loading (such as 512-QAM or 1024-QAM), or to be excluded. Subcarrier configuration in an EPoC OFDM channel of 192 MHz shall conform to the rules outlined in Table 101–8.

All CNUs and the CLT in an EPoC network share the same downstream subcarrier configuration and bit loading including nulled subcarriers, continuous pilots, bit loaded subcarriers, and excluded subcarriers.

An EPoC PHY shall declare which of the optional modulation types listed in Table 100–2 it supports via the *DS_ModAbility* and *US_ModAbility* variables.

Table 101–8—Downstream subcarrier configuration rules

Parameter	Limit	Unit
Minimum number of active subcarriers in a contiguous group	40	subcarriers
Minimum OFDM channel guard band	1	MHz
Maximum excluded spectrum in the encompassed spectrum	20	%

101.4.3.4.1 Nulled subcarriers

Nulled subcarriers do not carry MAC or PHY Link data but may be used as pilots. Nulled subcarriers are BPSK modulated using the pseudo-random sequence generated by the 13-bit linear feedback shift register, illustrated in Figure 101–28 except when being used as a scattered pilot in the downstream direction (see 101.4.3.6.1).

101.4.3.4.2 Continuous pilots

In the downstream direction continuous pilots are used to help delineate the downstream PHY Link (see 101.4.3.6.2).

101.4.3.4.3 Bit loaded subcarriers

When a subcarrier is used to carry MAC data it uses the modulation type of QPSK or 2^n-QAM, where the integer n is $4 \le n \le 12$, assigned via the *DS_ModTypeSC(n)* variable except when used as a downstream scattered Pilot (see 101.4.3.6.1).

There is at least one contiguous 22 MHz or greater band of active subcarriers with an assigned non-zero bit loading in any single 192 MHz OFDM channel. This 22 MHz band may include subcarriers intended as Pilots and PHY Link subcarriers. A 1 MHz guard band of excluded subcarriers above and below this 22 MHz creates a minimum width OFDM channel of 22 MHz encompassed spectrum.

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101.4.3.4.4 Excluded subcarriers

An EPoC PHY shall not transmit energy into a subcarrier that has been excluded from the OFDM channel (i.e., excluded subcarriers have zero amplitude). Typically there is a band edge Exclusion Band at both the top and bottom of the OFDM channel and there may be up to 14 exclusion bands internal to a single 192 MHz OFDM channel.

101.4.3.4.5 PHY Link managed variables

DS_ModAbility

TYPE: 5-bit binary

This bit mapped variable is used to declare which optional modulation types the PHY supports in the downstream direction for the MAC data path. When a bit read as TRUE it indicates that the PHY supports that modulation type.

Bit	Modulation type
0	8-QAM
1	16-QAM
2	32-QAM
3	8192-QAM
4	16384-QAM

DS_ModTypeSC(n)

TYPE: 4-bit binary

This set of variables determines the modulation parameters for each of the 4096 downstream OFDM subcarriers ($0 < n < 4095$). Each variable controls one of the 4096 subcarriers that are transmitted over an OFDM channel, with *DS_ModTypeSC(0)* controlling subcarrier zero, *DS_ModTypeSC(1)* controlling subcarrier 1, etc. The assignment of bits to each modulation type is shown below:

bit 3 2 1 0

1 1 1 1 = Excluded subcarrier
1 1 1 0 = 16384-QAM
1 1 0 1 = 8192-QAM
1 1 0 0 = 4096-QAM
1 0 1 1 = 2048-QAM
1 0 1 0 = 1024-QAM
1 0 0 1 = 512-QAM
1 0 0 0 = 256-QAM
0 1 1 1 = 128-QAM
0 1 1 0 = 64-QAM
0 1 0 1 = 32-QAM
0 1 0 0 = 16-QAM
0 0 1 1 = 8-QAM
0 0 1 0 = QPSK
0 0 0 1 = reserved (used by PHY for continuous pilots only, if set via MDIO to this value the PHY treats the subcarrier as null)
0 0 0 0 = null (carries no data but used for Wideband Probing)

DS_OFDM_ChAbility

TYPE: 3-bit integer

This variable indicates the number of OFDM channels the PHY is able to support in the downstream direction. The value of these bits is between 1 and 5 inclusive.

DS_OFDM_ID

TYPE: 3-bit integer

This variable is a pointer to one of the five possible OFDM channels in the downstream EPoC

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network. Thus when *DS_OFDM_ID* is set to a value of one variables *DS_ModTypeSC(n)* reflect the OFDM descriptor for OFDM channel one. When *DS_OFDM_ID* is set to a value of two variables *DS_ModTypeSC(n)* reflect the OFDM descriptor for OFDM channel two, etc.

101.4.3.5 Framing

The downstream OFDM frame is synchronized to the downstream PHY Link frame and the downstream Timestamp (see 102.2). Each downstream OFDM frame is composed of 128 OFDM symbols as illustrated in Figure 101–19 and Figure 102–1. The first 8 symbols of the downstream OFDM frame coincide with the 8 downstream symbols of the downstream PHY Link preamble. The Timestamp marks the first subcarrier of the first symbol after the Preamble (see Figure 102–11).

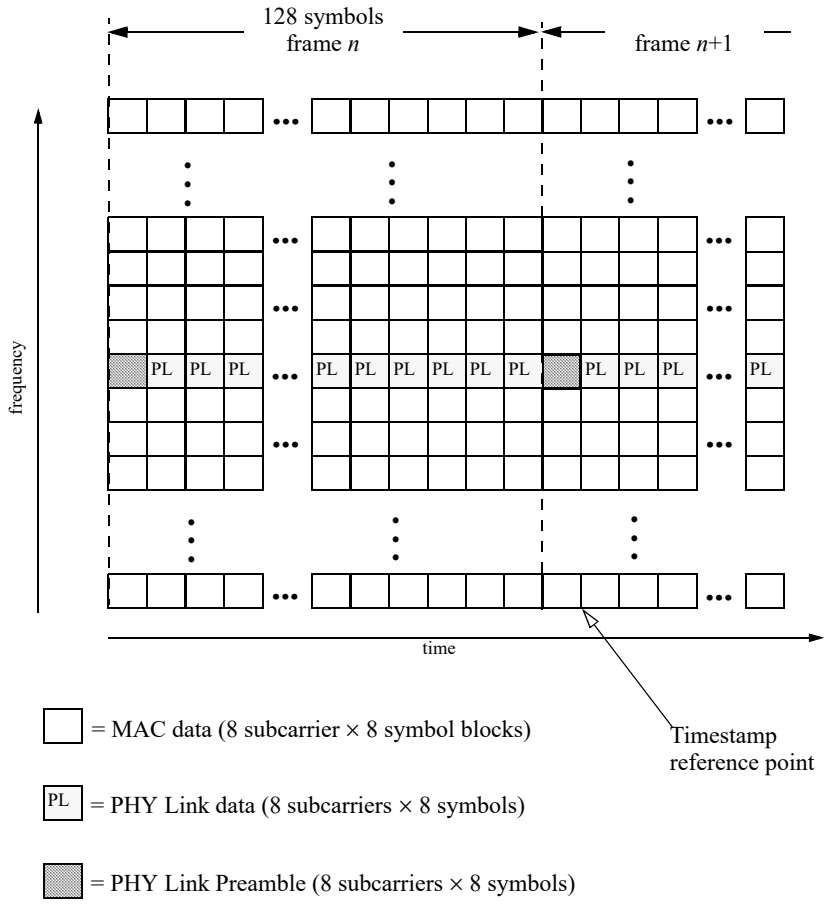

Figure 101–19—Downstream OFDM frame structure

101.4.3.6 Pilot map

Downstream pilots are composed of subcarriers modulated with a predefined data sequence known to all CNUs. The pilot data sequence is conveyed via the Pilot Insertion function (see 101.4.3.10 and Figure 101–1). Pilot Insertion follows time and frequency interleaving, before IDFT processing.

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There are two types of downstream pilots: continuous and scattered. Scattered pilots occur at different frequency locations in different symbols in a repeating cyclic pattern. Continuous pilots occur at fixed frequencies in every symbol.

101.4.3.6.1 Scattered pilots

The scattered pilot pattern is synchronized to the PHY Link as illustrated in Figure 101–20. The first OFDM symbol after the PHY Link preamble has a scattered pilot in the subcarrier just after the highest frequency subcarrier of the PHY Link.

The remainder of the scattered pilot pattern is placed so that in each symbol scattered pilots occur every 128 subcarriers. From symbol to symbol, scattered pilots are shifted by one subcarrier position in the direction of the increasing frequency. This will result in scattered pilots placed in the exclusion band and in the 400 kHz PHY Link band, such scattered pilots are not transmitted.

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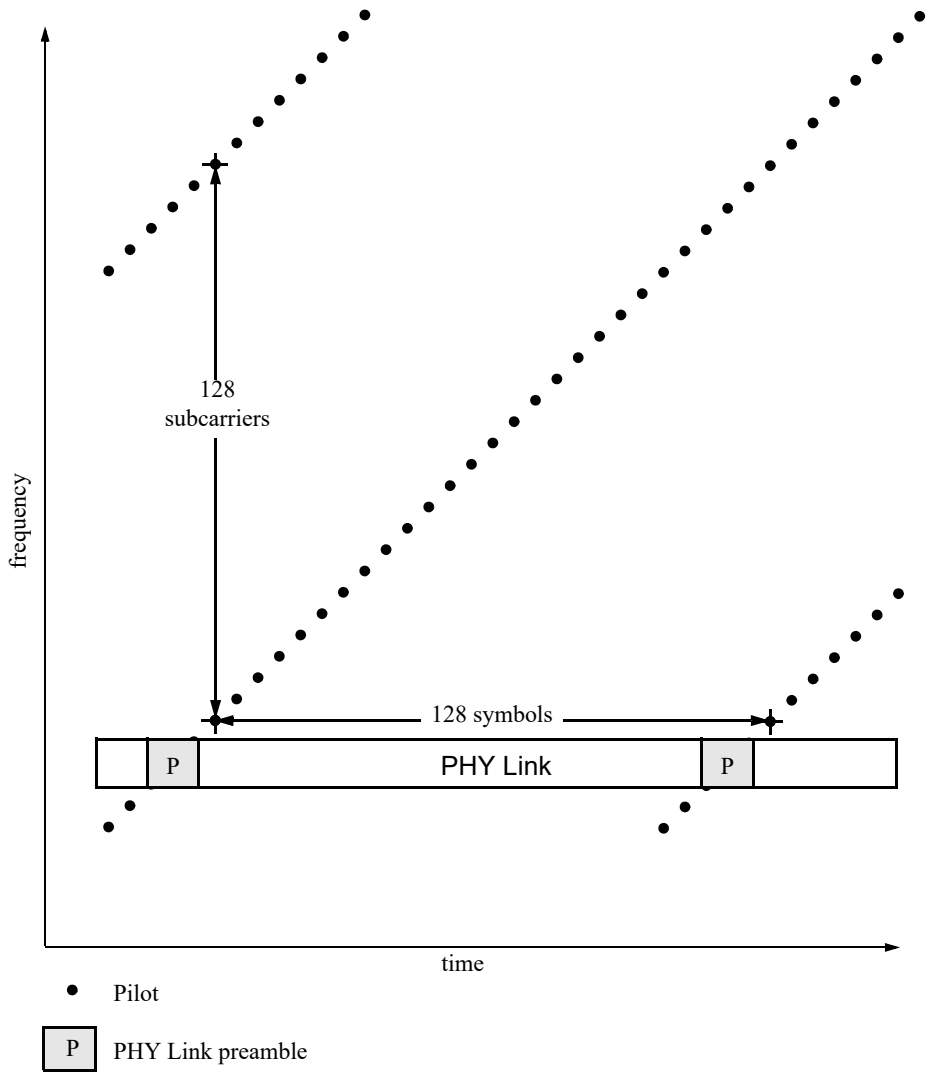

Figure 101–20—Downstream scattered pilot pattern

Mathematically, the scattered pilot pattern shall be defined as follows:

Let a subcarrier just after the PHY Link preamble be referred to as $x(m,n)$,

where

m is the frequency index
n is the time index (i.e., the OFDM symbol number)

The scattered pilots in the 128 symbols following (and including symbol n) are given by:

Symbol n:$x(n, m\pm128i)$, for all non-negative integers i
Symbol $(n+1)$:$x(n+1, m\pm128i + 1)$, for all non-negative integers i
Symbol $(n+2)$:$x(n+2, m\pm128i + 2)$, for all non-negative integers i
...
Symbol $(n+127)$:$x(n+127, m\pm128i + 127)$, for all non-negative integers i

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Each of the above locations is a scattered pilot, provided that it does not fall on a continuous pilot, on the PHY Link, on an exclusion zone or on an excluded subcarrier. If the scattered pilot coincides with a continuous pilot it is treated as a continuous pilot and not as a scattered pilot.

This pattern repeats every 128 symbols. That is, symbol (*128+n*) has the same scattered pilot pattern as symbol *n*.

101.4.3.6.2 Continuous pilots

Continuous pilots occur at the same frequency location in all symbols and are used for receiver synchronization. Placement of continuous pilots is determined in one of the following two ways:

1) Predefined continuous pilot placement around the PHY Link (see Figure 102–7), or
2) Continuous pilot placement defined via PHY Link instructions.

Note that continuous and scattered pilots can overlap; the amount of overlap, in terms of number of carriers, changes from symbol to symbol. Overlapping pilots are treated as continuous pilots.

101.4.3.6.3 Predefined continuous pilots around the PHY Link

As discussed in 102.2, the PHY Link is placed at the center of a 6 MHz spectral region. Four pairs of predefined continuous pilots shall be placed symmetrically around the PHY Link as shown in Figure 102–7 at the distances indicated in Table 101–9. The spacing between each pilot pair and the PHY Link are different to prevent all pilots from being impacted at the same time by echo or interference.

The locations of the continuous pilots are defined with reference to the edges of the PHY Link band. Hence, once the PHY Link has been detected, these continuous pilots also become known to the receiver.

Table 101–9 provides the values of d_1, d_2, d_3, and d_4, measured in number of subcarriers from the PHY Link edge. That is, d_x is the absolute value of the difference between the index of the continuous pilot and the index of the PHY Link subcarrier at the PHY Link edge nearest to the continuous pilot. The index of a subcarrier is the integer k of the IDFT definition given in 101.4.3.11. For example, let the lowest frequency subcarrier of the PHY Link have the IDFT index k equal to 972. Then according to Table 101–9 the continuous pilot nearest to this lowest frequency PHY Link subcarrier will have the IDFT index k of (972 – 15) = 957. The index k of the highest frequency PHY Link subcarrier of this OFDM channel is 979. Hence continuous pilot that is nearest upper frequency edge of the PHY Link has an index k of 994.

For each distance (d_x) defined in Table 101–9, the CLT places two pilots: one d_x subcarriers above and one d_x subcarriers below the edge of the PHY Link band.

Table 101–9—Subcarrier distances for placement of predefined pilots

	d_1	d_2	d_3	d_4
PHY Link 8 subcarriers	15	24	35	47

101.4.3.6.4 Continuous pilot placement defined by PHY Link message

The CLT defines a set of continuous pilots distributed as uniformly as possible (see paragraphs that follow) over the entire OFDM spectrum in addition to the predefined continuous pilots described in 101.4.3.6.3.

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The CLT ensures that there are no isolated active OFDM spectral regions that are not covered by continuous pilots.

The CLT provides the continuous pilot placement definition via the 10GPASS-XR downstream profile descriptor variables *DS_ModTypeSC(n)* using the PHY Link EPoC message block format contained in 102.2.3.3.

The CLT shall place continuous pilots (excluding the eight continuous pilots around the PHY Link) per the following eight steps after calculating a value for N_{PC} using Equation (101–9). This calculation occurs as the first step of activating a downstream profile (see 102.2.3.1.1).

The CLT obtains the value of N_{PC} using Equation (101–9):

$$N_{PC} = min\left(max\left(8, \left\lceil CntPltSF \times \left(\frac{F_{max} - F_{min}}{190 \times 10^6}\right)\right\rceil\right), 120\right) \quad (101–9)$$

where

F_{max} refers to frequency in Hz of the highest frequency active subcarrier of the OFDM channel
F_{min} refers to frequency in Hz of the lowest frequency active subcarrier of the OFDM channel
CntPltSF is the continuous pilot scaling factor

The number of continuous pilots is between 16 and 128. This range includes the eight continuous pilots around the PHY Link channel.

The value of *CntPltSF* in Equation (101–9) is kept as a parameter that can be adjusted by the CLT.

NOTE—The typical value proposed for *CntPltSF* is 48.

Step 1:

Merge all the subcarriers between F_{max} and F_{min} eliminating the following:

1) Exclusion bands
2) 6 MHz band containing the PHY Link

Let the merged frequency band be defined as the frequency range [0, $F_{mergedmax}$].

Step 2:

Define a set of N_{PC} frequencies using the following equation:

$$F_i = \frac{F_{mergedmax}}{2N_{PC}} + \frac{i \times F_{mergedmax}}{N_{PC}}, \text{ for } i = 0, 1, \ldots, N_{PC} - 1 \quad (101–10)$$

This yields a set of uniformly spaced N_{PC} frequencies:

$$\left\{\frac{F_{mergedmax}}{2N_{PC}}, \frac{3F_{mergedmax}}{2N_{PC}}, \ldots, F_{mergedmax} - \frac{F_{mergedmax}}{2N_{PC}}\right\} \quad (101–11)$$

Step 3:

Map the set of frequencies given above to the nearest subcarrier locations in the merged spectrum. This will give a set of N_{PC} approximately uniformly spaced subcarriers in the merged domain.

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Step 4:

De-merge the merged spectrum through the inverse of the operations through which the merged spectrum was obtained in step 1.

Step 5:

If any continuous pilot is within 1 MHz of a band edge, move this inwards (but avoiding subcarrier locations impacted by interferences like CSO/CTB) so that every continuous pilot is at least 1 MHz away from a band edge. This is to prevent continuous pilots from being impacted by external interferences. If the width of the spectral region does not allow the continuous pilot to be moved 1 MHz from the edge then the continuous pilot has to be placed at the center of the spectral region.

Step 6:

Identify any spectral regions containing active subcarriers (separated from other parts of the spectrum by exclusion bands on each side) that do not have any continuous pilots. Introduce an additional continuous pilot at the center of every such isolated active spectral region.

In the unlikely event that the inclusion of these extra pilots results in the total number of continuous pilots defined by PHY Link exceeding 120, return to step 1 and re-do the calculations after decrementing the value of N_{PC} by one.

Step 7:

Test for periodicity in the continuous pilot pattern and disturb periodicity, if any, through the perturbation of continuous pilot locations using a suitable algorithm. A simple procedure would be to introduce a random perturbation of up to ±5 subcarrier locations around each continuous pilot location, but avoiding subcarrier locations impacted by interferences like CSO/CTB.

Step 8:

The CLT transmits this continuous pilot pattern to the CNUs in the system and communicates the placement using the PHY Link.

101.4.3.6.5 PHY Link managed variables

CntPltSF

TYPE: 7-bit unsigned integer
This variable is used to determine the number of continuous pilots in the downstream OFDM channels.
$120 \geq CntPltSF \geq 48$.

101.4.3.7 Scrambler

The PHY shall scramble the output of the LDPC FEC encoding process using a linear feedback shift register mechanism as illustrated in Figure 101–21.

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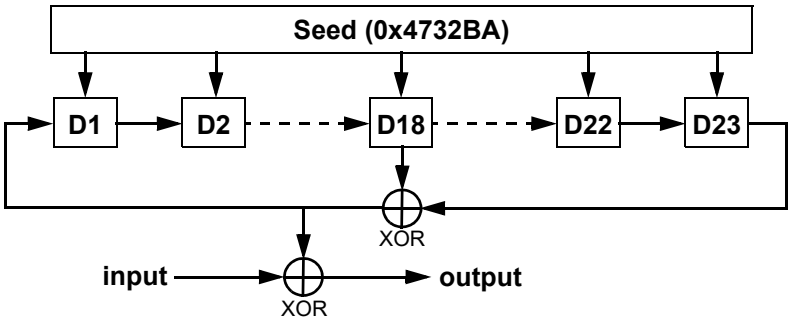

Figure 101–21—Scrambler

The scrambler is defined by the following polynomial.

$$x^{23} + x^{18} + 1$$

The scrambler is initialized to the hexadecimal value of 0x4732BA. The CLT shall initialize the scrambler at the first codeword of the downstream OFDM frame. The CNU shall initialize the scrambler with the hexadecimal value at the beginning of each grant.

101.4.3.8 Symbol mapper

101.4.3.8.1 Introduction

The Symbol Mapping function performs the following:

1) Initializes (resets) the scrambler function (see 101.4.3.7) and sets an *FCPbitCnt* to 1 (see 101.4.3.8.4), and initializes the mapping function with the lowest numbered active subcarrier.
2) Continually accepts a tx_unit (bit) from the Scrambler via the PMA_UNITDATA.request as well as monitors the Boolean state of *burstStart* and *burstEnd* (see 101.3.2.5.6) and the start of OFDM frame indication from the frame timing function. Also, the *FCPbitCnt* is incremented for each bit processed.
3) Per OFDM symbol, allocates scrambled tx_unit bits to all active OFDM data-carrying subcarriers (over all active channels) in ascending order based on a mapping configuration that anticipates frequency interleaving, staggered pilot placement and PHY Link signals per channel. While processing tx_unit bits, upon a start of frame indication, the bit counter is reset to one and the scrambler is reset before mapping the current bit to a subcarrier. Upon the next transition of *burstStart* = TRUE, the FCP update function calculates the next FCP value and updates the current PHY Link message (see 101.4.3.8.4).
4) Converts tx_unit bits to an array of QAM constellation points using a two-dimensional array with an I and Q "bin" value for each subcarrier and passes these values to the Interleaver.
5) When the last active subcarrier of the current symbol is completed, counter k is reset to 1 and processing of the next OFDM symbol begins.

The transmitter uses the number of bits per subcarrier as defined in Table 100–3 when bit mapping subcarrier (MAC) data to QAM constellations. Permissible modulation Types are listed in Table 100–2. QAM constellation mappings are described in 101.4.5.

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101.4.3.8.2 Transmitter bit loading for symbol mapping

The excluded versus non-excluded (active) status, PHY Link use, continuous pilot placement, and bit loading pattern (profile) information for each subcarrier is provided by the Subcarrier Configuration and Bit Loading Function. This information is configured by management.

The notation $S^{(E)}$ is used here to define the non-empty set of excluded subcarriers.

The notation $S^{(C)}$ is used here to define the set of continuous pilots (see 101.4.3.6.2).

The notation $S^{(P)}$ is used here to define the set of PHY Link subcarriers (see 101.4.3.6.3).

For bit loading, continuous pilots and the PHY Link are treated in the same manner as excluded subcarriers; hence, the set of subcarriers that includes the PHY Link, continuous pilots and excluded subcarriers is defined as:

$$S^{(PCE)} = S^{(P)} \cup S^{(C)} \cup S^{(E)} \tag{101–12}$$

The subcarriers in the set $S^{(PCE)}$ do not carry MAC data (PHY Link carries signaling information).

Bit loading information includes the option for nulled subcarriers (i.e., subcarriers that are not use for data transport) and are BPSK modulated, as described in 101.4.5.2.

Scattered pilots do not occur at the same frequency in every symbol; in some cases scattered pilots will overlap with continuous pilots. If a scattered pilot overlaps with a continuous pilot, then that pilot is no longer considered to be a scattered pilot. It is treated as a continuous pilot.

Because the locations of scattered pilots change from one OFDM symbol to another, the number of overlapping continuous and scattered pilots changes from symbol to symbol. Since overlapping pilots are treated as continuous pilots, the number of scattered pilots changes from symbol to symbol.

The following notation is used here:

N:The total number of subcarriers in the OFDM symbol (4096 per OFDM channel)
N_C:The number of continuous pilots in an OFDM symbol
N_S:The number of scattered pilots in an OFDM symbol
N_E:The number of excluded subcarriers in an OFDM symbol
N_P:The number of PHY Link subcarriers in an OFDM symbol
N_D:The number of data subcarriers in an OFDM symbol
N_I:The number of scattered pilots and data subcarriers in the OFDM symbol

The values of N, N_C, N_E, and N_P do not change from symbol to symbol for a given OFDM template; the values of N_S and N_D change from symbol to symbol.

The following equations holds for all symbols:

$$N = N_C + N_S + N_E + N_P + N_D \tag{101–13}$$

$$N_I = N_S + N_D \tag{101–14}$$

Interleaving and de-interleaving are applied to the set of data subcarriers and scattered pilots of size N_I.

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101.4.3.8.3 Bit loading

The bit loading pattern defines the QAM constellations assigned to each of the 4096 (N) subcarriers per OFDM channel of the OFDM transmission. Let the bit loading pattern per OFDM channel for configuration i be defined as $A_i(k)$, where:

k is the subcarrier index that goes from 0 to 4095

$A_i(k) \in \{0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14\}$. A value of 0 indicates that the subcarrier k is nulled. Other values indicate that the modulation of subcarrier k is QAM with order shown in Equation (101–15). See variable *DS_ModTypeSC(n)* defined in 101.4.3.4.5.

$$QAM\ order = 2^{A_i(k)} \tag{101–15}$$

The function $A_i(k)$ and subsequent bit loading functions are defined per OFDM channel as the interleaver function is replicated with identical operation per OFDM channel. As up to five OFDM channels are accommodated (refer to Table 101–12) with a labeling of 1 to 5 (L), the bit loading processing ordering is $L = \{1, 2, 3, 4, 5\}$. OFDM channel 1 is always present and contains active data subcarriers.

Downstream RF spectrum availability as well as device implementation will determine OFDM channel presence and actual subcarrier use. The symbol mapping function therefore shall process all active subcarriers per symbol across all OFDM channels.

Let the sequence

$\{A_i(k), k = 0, 1, \ldots, (N-1), k \notin S^{(PCE)}\}$ be arranged as N_I consecutive values of another sequence:

$B_i(k), k = 0, 1, \ldots, (N_I - 1)$.

Given the locations of the excluded subcarriers, continuous pilots and the PHY Link in the OFDM configuration, it is possible to obtain the bit-loading pattern $B_i(k)$ that is applicable only to spectral locations without excluded subcarriers, continuous pilots, and PHY Link subcarriers. However, note that $B_i(k)$ does contain the spectral locations occupied by scattered pilots; these locations change from symbol to symbol.

The bit loading pattern is defined in the domain in which subcarriers are transmitted on the media, however bit loading is processed prior to interleaving. As such there is a permutation mapping of subcarriers, defined by the interleaving function, between the domain in which bit loading is applied to subcarriers and the domain in which subcarriers are transmitted.

The total number of subcarriers that pass through the interleaver and de-interleaver is given in Equation (101–14) and does not change from symbol to symbol. The frequency interleaver introduces a one-to-one permutation mapping P on the N_I subcarriers.

NOTE—The corresponding permutation mapping applied at the receiver de-interleaver is P^{-1}.

The bit loading pattern at the input to the interleaver. This is given by:

$$C_i(k) = P^{-1}(B_i(k)) \tag{101–16}$$

The sequence $C_i(k)$ is obtained by sending $\{B_i(k), k = 0, 1, \ldots, N-1\}$ through the frequency de-interleaver.

Note that $C_i(k)$ gives the bit-loading pattern for N_I subcarriers per OFDM channel. Scattered pilots are avoided in the bit-loading process and identified by a two-dimensional binary pattern $D(k, j)$ per OFDM

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channel. The scattered pilot pattern has a periodicity of 128 in the time dimension, this binary pattern also has periodicity 128 in the column dimension *j*.

D(k, j) is defined for $k = 0, 1, ..., (N_I - 1)$ and for $j = 0, 1, ..., 127$.

The binary pattern *D(k, j)* begins with the transmitted scattered pilot pattern defined in 101.4.3.6.1.

The CLT executes the following steps to obtain the pattern *D(k, j)*:

1) Define a two-dimensional binary array *P(k, j)* per OFDM channel in the subcarrier transmitted domain that contains a one for each scattered pilot location and zero otherwise:
   P(k, j), for $k = 0, 1, ..., 4095$ and for $j = 0, 1, ...,127$
   The first column of this binary sequence corresponds to the first OFDM symbol following the preamble of the PHY Link.
2) Exclude the rows corresponding to excluded subcarriers, continuous pilots, and PHY Link from the two-dimensional array *P(k, j)* to give an array *Q(k, j)*. The number of rows of the resulting array is N_I and the number of columns is 128.
3) Pass this two-dimensional binary array *Q(k, j)* through the frequency de-interleaver and then the time de-interleaver, with each column treated as an OFDM symbol. After the 128 columns of the pattern have been input into the interleaver, re-insert the first *DS_TmIntrlv* columns, where *DS_TmIntrlv* is the depth of the time interleaver. This is equivalent to periodically extending *Q(k, j)* along the dimension *j* and passing (128 + *DS_TmIntrlv*) columns of this extended sequence through the frequency de-interleaver and the time de-interleaver.
4) Discard the first *DS_TmIntrlv* symbols coming out of the time de-interleaver and collect the remaining 128 columns into an array to give the binary two-dimensional array *D(k, j)* of size $(N_I \times 128)$.

For bit loading the CLT accesses the appropriate column *j* of the binary pattern bit *D(k, j)* together with the appropriate bit loading profile $C_i(k, j)$. If the value of the bit *D(k, j)* is 1, the CLT skips this subcarrier *k* and moves to the next subcarrier. This subcarrier is included as a placeholder for a scattered pilot that will be inserted in this subcarrier location after interleaving. After each symbol the column index *j* has to be incremented modulo 128.

The CLT uses this binary two-dimensional array *D(k, j)* of size $(N_I \times 128)$ in order to do bit-loading of OFDM subcarriers, as described earlier in this subclause.

The corresponding operation in the CNU is de-mapping the QAM subcarriers to get log-likelihood ratios corresponding to the transmitted bits. This operation, described below, is much simpler than the mapping operation in the transmitter.

The scattered pilots and data subcarriers of every received symbol are subjected to frequency and time de-interleaving. The scattered pilots have to be tagged so that these can be discarded at the output of the time and frequency de-interleavers. This gives N_I subcarriers for every OFDM symbol. The CNU accesses theses N_I de-interleaved subcarriers together with the bit-loading pattern $C_i(k)$ to implement the de-mapping of the QAM subcarriers into log-likelihood ratios. If the subcarrier *k* happens to be a scattered pilot, then this subcarrier, as well as the corresponding value $C_i(k)$, is skipped and the CNU moves to the next subcarrier $(k+1)$.

101.4.3.8.4 FCP calculation

The FCP calculation is supplied by the Symbol Mapper via a function call UpdateFCP. The Symbol Mapper resets the bit counter, FCPbitCnt, to zero at the start of each downstream OFDM frame and increments it for every bit processed in the frame. On the first transition of *burstStart* to TRUE from the PMA_UNITDATA.request after the start of a new frame the Symbol Mapper calls the UpdateFCP function with the counter value. The UpdateFCP function calculates the next (new) FCP value based on the supplied value, the *DS_Frame_Data_Load* (see 100.3.2.1) and *FEC_DS_CodeWordSize* (see 101.3.2.5.2) per

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Equation (101–17). The UpdateFCP function shall complete and pass the new FCP value to the PHY Link with sufficient time for insertion in the PHY Link frame currently being processed.

$$FCP = (FCPbitCnt + DS\_Frame\_Data\_Load) \bmod FEC\_DS\_CodeWordSize \quad (101–17)$$

where

FCPbitCnt is a counter reset to zero at the beginning of each downstream OFDM frame and is incremented for each bit that is transfered from the PMA service interface.

The downstream FEC Encoder is not aligned with the downstream OFDM frame, thus FEC codewords may straddle downstream OFDM frame boundaries. The CNU may use the FCP value in the received PHY Link messages to help locate the downstream FEC codewords. The FCP value indicates the starting bit position of the first full codeword in the next downstream OFDM frame. See 102.2.3.5.

101.4.3.9 Time and frequency interleaver

101.4.3.9.1 Overview

The CLT first applies a time interleaver to all N_I subcarriers of each OFDM symbol [see Equation (101–14)] across a group of *DS_TmIntrlv* OFDM symbols. The CLT then subjects each OFDM symbol containing these N_I time interleaved subcarriers to frequency interleaving. There is a single Time and Frequency interleaving function per OFDM channel for the MAC data path.

101.4.3.9.2 Time interleaving

The CLT shall time interleave after OFDM symbols have been mapped to QAM constellations and before they are frequency interleaved as described in this subclause.

The time interleaver is a convolutional interleaver that operates at the OFDM subcarrier level. If the depth of the interleaver is *DS_TmIntrlv*, then there are *DS_TmIntrlv* branches, as shown in Figure 101–22.

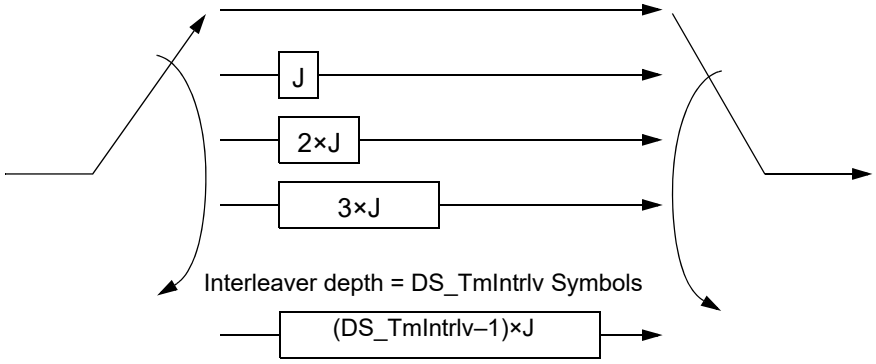

Figure 101–22—Time interleaver structure

The CLT shall support values of *DS_TmIntrlv* from 1 to 32 (see 101.4.3.9.5).

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Each branch is a delay line; the input and output will always be connected to the same delay line. This delay line will be clocked to insert a new subcarrier's data into the delay line and to extract a subcarrier's data from the delay line. Next, the commutator switches the input and the output to the next delay line in the direction shown by the arrows in Figure 101–22. After the delay line with the largest delay, the commutator will move to the delay line with zero delay.

The lowest frequency subcarrier of an OFDM symbol always goes through the branch with zero delay. Then the commutator switch at input and the corresponding commutator switch at output are rotated by one position for every new subcarrier.

The value of J is given by the following equation:

$$J = \left\lceil \frac{N_{\mathrm{I}}}{DS\_\mathrm{TmIntrlv}} \right\rceil \tag{101–18}$$

Where, N_{I} [see Equation (101–14)] is the number of data subcarriers and scattered pilots in an OFDM symbol.

If N_{I} is not divisible by *DS_TmIntrlv*, all of the branches are not filled. Therefore, "dummy subcarriers" are added to the symbol to make the number of subcarriers equal to a multiple of *DS_TmIntrlv*. The number of dummy subcarriers is given by:

$$J \times DS\_TmIntrlv - N_{\mathrm{I}} \tag{101–19}$$

The dummy subcarriers are added for definition purposes only; at the output of the interleaver these dummy subcarriers are discarded.

101.4.3.9.3 Frequency interleaving

The CLT shall perform frequency interleaving after time interleaving; subcarriers containing continuous pilots, excluded subcarriers, or PHY Link data are not frequency interleaved.

The frequency interleaver works on individual OFDM symbols. Each symbol to be interleaved consists of N_{I} subcarriers indexed from 0 to $N_{\mathrm{I}} - 1$ in ascending frequency order. These N_{I} subcarriers are made up of N_{D} data subcarriers and N_{S} scattered pilot placeholders. Although N_{D} and N_{S} are not the same for every symbol, the value of N_{I} is a constant for all OFDM symbols in the downstream OFDM frame for a given system configuration.

Conceptually, frequency interleaving of each individual OFDM symbol is performed using memory arranged in a 2D store comprising 2^{L} rows and K columns where L and K are chosen depending on the size of the FFT used for creating the OFDM symbols. If the number of data subcarriers and scattered pilots in the OFDM symbol is N_{I}, then the number of columns, K, is given by the following equation:

$$K = \left\lceil \frac{N_{\mathrm{I}}}{2^{L}} \right\rceil \tag{101–20}$$

If N_I is not an integer multiple of 2^L, then the last column will only be partially filled during the frequency interleaving process. The number of data subcarriers in the last column, C, is given by:

$$C = N_{\mathrm{I}} - 2^{L}(K - 1) \tag{101–21}$$

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The frequency interleaver follows the following process; note that rows are numbered 0 to 2^L–1, and columns are numbered from 0 to *K–1*:

1) Write successive consecutive subcarriers into the 2D store in the row given by the *L*-bit CRC (cyclic redundancy check) value of each *L*-bit row address (Figure 101–25).
2) Rotate the subcarriers in each row written by the same *L*-bit CRC value of the row address modulo the number of columns in that row (either modulo *K* for a row below *C* or modulo *K*–1 for row *C* and higher) using a right circular shift (Figure 101–23a).
3) Rotate the subcarriers in each column by the *L*-bit CRC value of [*K*–1 minus the column address] using a downward circular shift (Figure 101–23b). Note that the last column *K*–1 with a CRC value of 0 is not rotated.
4) Read the subcarriers out of the 2D store column-wise from row 0, column 0 to row *C*–1, column *K*–1.

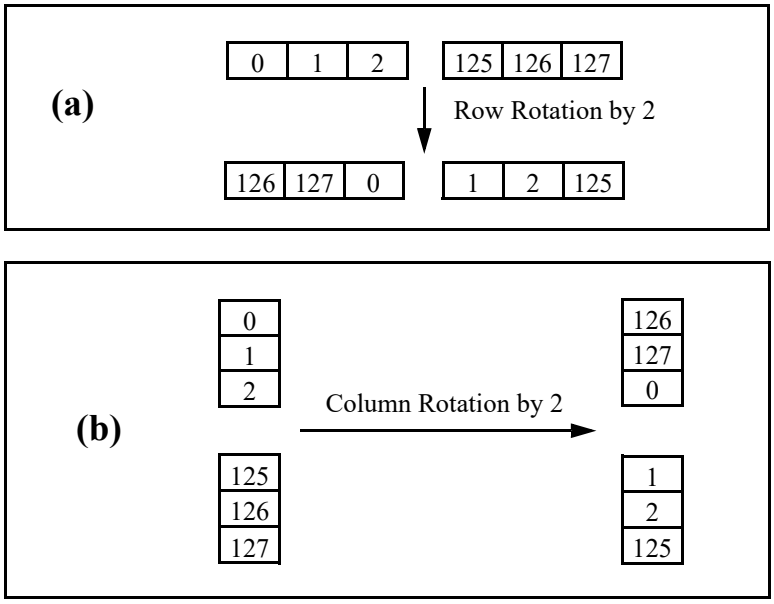

Figure 101–23—Rotation of subcarriers: a) Horizontal rows, b) Vertical columns

Assume that the input subcarriers of the OFDM symbol are initially arranged into the 2D store in sequential order column-wise from row 0, column 0 to row *C*–1, column *K*–1. The above procedure relocates each sequential input subcarrier number in row *r*, column *c* into a permuted output subcarrier number in the 2D store in that position in row *r*, column *c* as *sc(r,c)* given by Equation (101–22):

$$sc(r,c) = sc_0[(r - CRC(K-1-c))mod2^L] + (c - (r - CRC(K-1-c)mod2^L))modM \qquad (101\text{–}22)$$

where $M = K$, for $(r - CRC(K-1-c))mod2^L < C$

otherwise $M = K$–1

$sc(r,c) \in [0,1, \ldots, N_I - 1]$ and $sc_0[n]$ is defined as an array of 2^L elements where each element contains the cumulative number of subcarriers previously written into the 2D store prior to writing into the permuted output row *n*. Note that if the last column contains fewer subcarriers than 2^L, the cumulative value in $sc_0[n]$

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takes into account those previously written permuted output rows that were shorter by one subcarrier (i.e., those prior row addresses that were greater than or equal to *C*, the number of subcarriers in the last column).

The structure of the two-dimensional store is shown in Figure 101–24.

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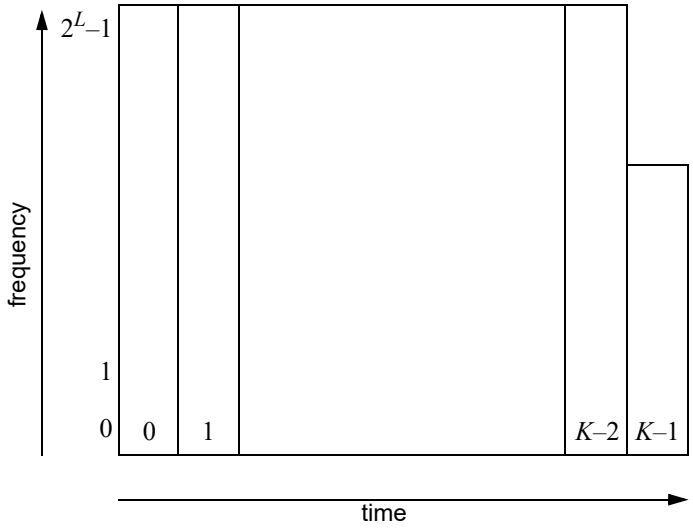

Figure 101–24—Two-dimensional store block structure

The m-stage linear feedback shift register for calculating the CRC of each row address is defined using a generator polynomial of degree $m = L$ in the finite (Galois) field GF[2]:

$$G(X) = g_m X^m + g_{m-1} X^{m-1} + g_{m-2} X^{m-2} + \ldots + g_2 X^2 + g_1 X^1 + g_0 \quad (101\text{–}23)$$

where the coefficients g_m corresponding to the feedback taps of the linear feedback shift register are chosen such that the resulting generator polynomial is primitive (i.e., if the polynomial is prime and cannot be factored, and if it is a factor that evenly divides X^N+1, where $N = 2^m–1$). This guarantees that each *L*-bit address for the 2^L rows is unique and the CRC values span the entire set of 2^L, *L*-bit addresses.

The linear feedback shift register implementing the generator polynomial is shown in Figure 101–25.

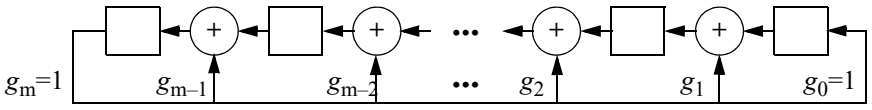

Figure 101–25—Row address linear feedback shift register

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Calculation of the CRC c_{m-1}, c_{m-2}, …, c_1, c_0 for each row address b_{m-1}, b_{m-2}, …, b_1, b_0 using this linear feedback shift register structure is shown in Figure 101–26.

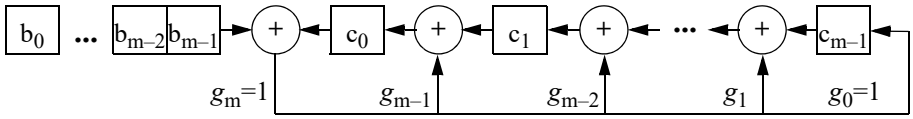

Figure 101–26—CRC calculation using a linear feedback shift register

The specific generator polynomial for the calculation of the CRC with $m = L = 6$ is given by:

$$G(X) = X^6 + X^1 + 1 \tag{101–24}$$

The corresponding linear feedback shift register is shown in Figure 101–27.

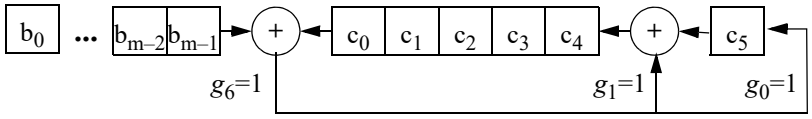

Figure 101–27—CRC calculation for $G(X) = X^6 + X^1 + 1$ with a linear feedback shift register

De-interleaving is accomplished by reversing the interleaving process described above. Each symbol to be de-interleaved consists of N_I subcarriers indexed from 0 to $N_I - 1$ in ascending frequency order. Assume that the input subcarriers of the interleaved OFDM symbol are arranged into the 2D store in sequential order column-wise from row 0, column 0 to row 2^L, column C.

The frequency de-interleaver performs the following process to reverse the interleaving process; note that rows are numbered from 0 to 2^L–1, and columns are numbered from 0 to K–1:

1) Write the subcarriers into the 2D store column-wise from column 0, row 0 to column K–1, row C.
2) Rotate the subcarriers in each column by the L-bit CRC value of [K–1 minus the column address] using an upward circular shift (reverse of Figure 101–25b). Note that the last column K–1 with a CRC value of 0 in not rotated.
3) Rotate the subcarriers in each row written by the same L-bit CRC value of the row address modulo the number of columns in that row (either modulo K for a row below C or modulo K–1 for row C and higher) using a left circular shift (reverse of Figure 101–25a).
4) Read the subcarriers out of the 2D store row-wise in the row order given by the L-bit CRC value of each L-bit row address skipping the last column at or beyond row C.

101.4.3.9.4 Interleaving impact on continuous pilots, scattered pilots, PHY Link and excluded spectral region

The CLT interleaves the subcarriers that are tagged to act as placeholders for scattered pilots. The actual BPSK modulation to these placeholder subcarriers is applied after interleaving as described in 101.4.3.9.2 and 101.4.3.9.3.

The CLT retains a reference pattern for inserting scattered pilot placeholders prior to interleaving. Since the scattered pilot pattern repeats every 128 symbols, this pattern is a ($N_I \times 128$) two-dimensional bit pattern. A

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value of one in this bit-pattern indicates the location of a scattered pilot. The CLT inserts data subcarriers where this reference pattern has a zero and scattered pilot placeholders where this pattern has a one.

This reference pattern may be derived from the following procedure:

1) In the time-frequency plane, create a two-dimensional bit-pattern of zeros and ones from the transmitted "diagonal" scattered pilot patterns described in 101.4.3.6.1. This pattern has a periodicity of 128 symbols and has a value of one for a scattered pilot location and zero otherwise. Let the time axis be horizontal and the frequency axis vertical.
2) Delete all horizontal lines containing continuous pilots, excluded subcarriers, and PHY Link from the above mentioned two-dimensional bit pattern; note that some scattered pilots could coincide with continuous pilots. These locations are treated as continuous pilot locations.
3) Send the resulting bit-pattern through the frequency de-interleaver and the time de-interleaver in succession. This will give another two-dimensional bit pattern that has a periodicity of 128 symbols. The appropriate 128-symbol segment of this bit-pattern is chosen as the reference bit pattern referred to above.

The synchronization of the scattered pilot pattern to the PHY Link preamble, as described in Figure 101–20 uniquely defines the 128-symbol segment that is used as the reference pattern.

Note that the number of OFDM subcarriers that are interleaved does not change from symbol to symbol. The insertion of continuous pilots, PHY Link, and excluded regions happens after both time and frequency interleaving. Interleaving is independent of individual subcarrier modulation and the modulation pattern of these data subcarriers may change from symbol to symbol.

101.4.3.9.5 PHY Link managed variables

DS_TmIntrlv
: TYPE: 5-bit integer
This variable indicates the number of time interleaved OFDM symbols in the downstream direction. The value is between 1 and 32.

101.4.3.10 Pilot insertion

Continuous and scattered pilots shall be BPSK modulated using the pseudo-random sequence generated by the 13-bit linear feedback shift register, illustrated in Figure 101–28 with polynomial $(x^{13}+x^{12}+x^{11}+x^{8}+1)$ and described next.

This linear feedback shift register is initialized to all ones at the k=0 index of the discrete Fourier transform defining the OFDM signal (refer to 101.4.3.11). It is then clocked after every subcarrier of the IDFT. If the subcarrier is a pilot (scattered or continuous), then the BPSK modulation for that subcarrier is taken from the linear feedback shift register output.

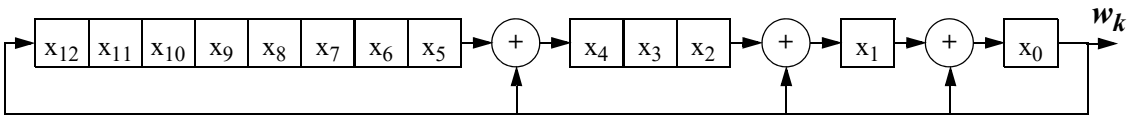

Figure 101–28—13-Bit Linear Feedback Shift Register for the pilot modulation Pseudo-Random Sequence

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Let the output of the linear feedback shift register be w_k then BPSK modulation used for the pilot is:

$w_k = 0$: BPSK constellation point = 1 + j0

$w_k = 1$: BPSK constellation point = –1 + j0

101.4.3.10.1 Pilot boosting

All active subcarriers, with the exception of pilots, are transmitted with the same average power. The CLT shall multiply the real and imaginary components of continuous and scattered pilots by a real-valued number such that the amplitude of the continuous and scattered pilots is twice the root-mean-square value of the amplitude of other subcarriers of the OFDM symbol. That is, continuous and scattered pilots are boosted by approximately 6 dB with reference to other subcarriers.

101.4.3.11 Inverse Discrete Fourier Transform (IDFT)

The CLT OFDM and CNU OFDMA signals are assembled in the frequency domain using 4096 subcarriers per OFDM/OFDMA channel. The signal is composed of: MAC data subcarriers, scattered pilots, continuous pilots, PHY Link subcarriers, zero-bit-value subcarriers, and excluded subcarriers (zero valued into the IDFT).These OFDM/OFDMA signals are described in IDFT Equation (101–25).

$$x(i) = \frac{1}{\sqrt{N}} \sum_{k=0}^{N-1} X(k) \exp\left(j \frac{2\pi i \left(k - \frac{N}{2} \right)}{N} \right), \text{ for } i = 0, 1, \ldots, (N-1) \qquad (101\text{–}25)$$

where

N equals 4096
$X(0)$ is the lowest frequency component
$X(N–1)$ is the highest frequency component
k is the spectral index of the subcarrier

The resulting time domain discrete signal, *x(i)*, is a baseband complex-valued signal, sampled at 204.8 million samples per second resulting in a subcarrier spacing of 50 kHz.

Once the CNU detects the downstream PHY Link and receives the *DS_FreqCh(1)* variable (see Table 101–1), the CNU knows the location of $k = 0$.

The encompassed spectrum of a 192 MHz OFDM channel is 190 MHz (3800 active subcarriers, see Table 100–3 and Table 100–11). These 3800 maximum active subcarriers of a CLT or CNU OFDM transmitter channel shall occupy the range $148 \leq k \leq 3947$, where k is the spectral index of the subcarrier in Equation (101–25).

101.4.3.11.1 PHY Link managed variables

DS_FreqCh(n)
See 100.3.2.3.

101.4.3.12 Cyclic prefix and windowing

CLT and CNU cyclic prefix (CP) and windowing processing begins with the N-point output of the IDFT:

$\{x(0), x(1), \ldots, x(N-1)\}$

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The variable *DSNcp* represents the provisioned duration, in OFDM Clock periods, of the downstream cyclic prefix parameter (see Table 101–10) for the CLT. The *DSNcp* samples at the end of this *N*-point IDFT are copied and prepended to the beginning of the IDFT output to give a sequence of length (*N* + *DSNcp*):

$$\{x(N - DSNcp), x(N - DSNcp + 1),\ldots, x(N - 1), x(0), x(1), \ldots, x(N - 1)\}$$

The variable *DSNrp* represents the provisioned duration, in OFDM Clock periods, of the downstream windowing parameter (see Table 101–11 for the CLT. The *DSNrp* samples at the start of the *N*-point IDFT are copied and appended to the end of the IDFT output to give a sequence of length (*N* + *DSNcp* + *DSNrp*):

$$\{x(N - DSNcp), x(N - DSNcp + 1), \ldots, x(N - 1), x(0), x(1), \ldots, x(N - 1), x(0), x(1), ..., x(DSNrp - 1)\}$$

Let this extended sequence of length (*N* + *DSNcp* + *DSNrp*) be defined as:

$$\{y(i),\ i=0, 1, ..., (N + DSNcp + DSNrp - 1)\} \tag{101–26}$$

DSNrp samples at both ends of this extended sequence are subject to tapering. This tapering is achieved using a raised-cosine window function; a window is defined to be applied to this entire extended sequence. This window has a flat top and raised-cosine tapering at the edges, as shown in Figure 101–29.

The window function *w(i)* is symmetric at the center; therefore, only the right half of the window is defined in the following equation:

$$w\left(i + \frac{N + DSNcp + DSNrp}{2}\right) = 1.0 \tag{101–27}$$

$$\text{for } i = 0, 1, \ldots, \frac{(N + DSNcp + DSNrp)}{2} - 1$$

$$w\left(i + \frac{N + DSNcp + DSNrp}{2}\right) = \frac{1}{2}\left(1 - \sin\left(\frac{\pi}{\alpha(N + DSNcp)}\left(i - \frac{N + DSNcp}{2} + \frac{1}{2}\right)\right)\right) \tag{101–28}$$

$$\text{for } i = \left(\left(\frac{N + DSNcp - DSNrp}{2}\right), \ldots, \left(\frac{N + DSNcp + DSNrp}{2} - 1\right)\right)$$

Here,

$$\alpha = \frac{DSNrp}{N + DSNcp} \tag{101–29}$$

defines the window function for (*N* + *DSNcp* + *DSNrp*)/2 samples. The complete window function of length (*N* + *DSNcp* + *DSNrp*) is defined using the symmetry property as:

$$w\left(\frac{N + DSNcp + DSNrp}{2} - i - 1\right) = w\left(\frac{N + DSNcp + DSNrp}{2} + 1\right), \tag{101–30}$$

$$\text{for } i = 0, 1, \ldots, \frac{(N + DSNcp + DSNrp)}{2} - 1$$

This yields a window function (or sequence): $\{w(i),\ i=0, 1, ..., (N + DSNcp + DSNrp - 1)\}$. The length of this sequence is an even-valued integer.

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The previous window function is applied to the sequence $\{y(i)\}$:

$$z(i) = y(i)\, w(i), \quad for\ i = 0, 1, \ldots, (N + DSNcp + DSNrp - 1) \tag{101–31}$$

Each successive set of N samples at the output of the IDFT yields a sequence $z(i)$ of length $(N + DSNcp + DSNrp)$. Each of these sequences is overlapped at each edge by *DSNrp* samples with the preceding and following sequences, as shown in the last stage of Figure 101–29. Overlapping regions are added together.

To define this "overlap and add" function mathematically, consider two successive sequences $z_1(i)$ and $z_2(i)$. The overlap and addition operations of these sequences are defined using the following equation:

$$z_1(N + DSNcp + i) + z_2(i), \quad for\ i=0, 1, \ldots, DSNrp - 1 \tag{101–32}$$

That is, the last *DSNrp* samples of sequence $z_1(i)$ are overlapped and added to the first *DSNrp* samples of sequence $z_2(i)$.

The length of the extended OFDM symbol is $(N + DSNcp + DSNrp)$ samples. Of this, ($DSNrp$/2) samples are within the preceding symbol, and ($DSNrp$/2) samples are within the following symbol. This yields a symbol period of ($N + DSNcp$) samples.

The process of cyclic prefix and windowing is illustrated in Figure 101–29. In the downstream direction the CLT shall use one of the permissible values for *DSNcp* and *DSNrp* given in Table 101–10 and Table 101–11, respectively, selected such that $DSNrp < DSNcp$.

Table 101–10—Size of cyclic prefix (*DSNcp*), downstream direction

DSNcp **[OFDM Clock period (1/204.8 MHz)]**	**[μs]**
256	1.25
512	2.5
768	3.75

Table 101–11—Size of OFDM Window (*DSNrp*), downstream direction

DSNrp **[OFDM Clock period (1/204.8 MHz)]**	**[μs]**
0	0
64	0.3125
128	0.625
192	0.9375
256	1.25

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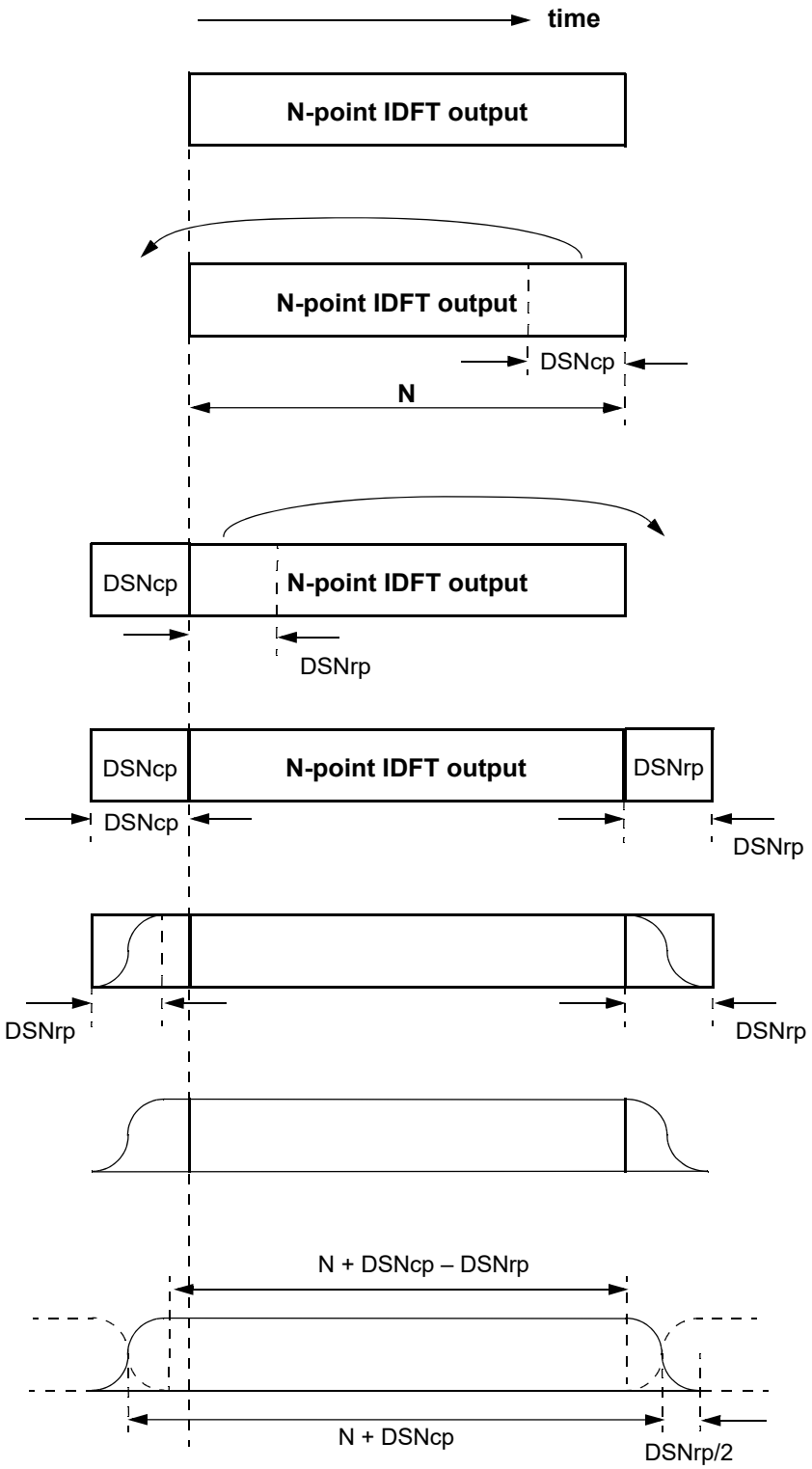

NOTE—Cyclic prefix and Windowing in the upstream direction is created in a similar fashion using USNcp and USNrp.

Figure 101–29—Cyclic prefix and windowing algorithm

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101.4.3.12.1 PHY Link managed variables

DSNcp

TYPE: 4-bit binary
This variable controls the size of the cyclic prefix in the downstream direction per the following enumeration:
bit 3 2 1 0
1 x x x = reserved
0 1 x x = reserved
0 0 1 1 = 768 OFDM Clock periods (1/204.8 MHz)
0 0 1 0 = 512 OFDM Clock periods (1/204.8 MHz)
0 0 0 1 = 256 OFDM Clock periods (1/204.8 MHz)
0 0 0 0 = reserved

DSNrp

TYPE: 3-bit binary
This variable controls the size of the windowing function in the downstream direction per the following enumeration:
bit 2 1 0
1 1 x = reserved
1 0 1 = 256 OFDM Clock periods (1/204.8 MHz)
1 0 0 = 192 OFDM Clock periods (1/204.8 MHz)
0 1 1 = 128 OFDM Clock periods (1/204.8 MHz)
0 1 0 = 64 OFDM Clock periods (1/204.8 MHz)
0 0 1 = reserved
0 0 0 = 0 samples (windowing disabled)

101.4.3.13 OFDM channel requirements

The 10GPASS-PX-D PHY shall comply with the OFDM channel operational requirements in Table 101–12.

Table 101–12—Multiple OFDM channel requirements

Item	Requirement
OFDM channel 1 configuration	OFDM channel 1 is always be enabled. OFDM channel 1 processes subcarriers for data as well as the PHY Link.
OFDM channel 2, 3, 4, 5 configuration	OFDM channels 2, 3, 4, or 5 may be enabled or disabled for operation. OFDM channels are enabled in ascending order: e.g., enable OFDM channel 2 before enabling OFDM channel 3, enable OFDM channel 3 before enabling OFDM channel 4, enable OFDM channel 4 before enabling OFDM channel 5.
OFDM channel frequency placement	An OFDM channel may be configured for operation in any portion of the downstream Frequency Band as per Table 100–3.
OFDM channel subcarrier indexing relation to RF frequency	OFDM channel 1: 0 to 4095 OFDM channel 2: 4096 to 8191 OFDM channel 3: 8192 to 12287 OFDM channel 4: 12288 to 16383 OFDM channel 5: 16384 to 20479

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Table 101–12—Multiple OFDM channel requirements *(continued)*

Item	Requirement
OFDM channel subcarrier frequency ordering	RF frequency correlates to subcarrier index; i.e., the lower the subcarrier index, the lower the RF frequency.
Minimum encompassed Spectrum	The minimum encompassed spectrum of any enabled OFDM channel is 22 MHz as per Table 100–3.
Encompassed spectrum overlap	The encompassed spectrum of any enabled OFDM channel does not overlap with that of any other enabled OFDM channel.
Adjacent OFDM channel placement	The CLT transmitter permits placement of the edge subcarrier of an OFDM channel's encompassed spectrum immediately adjacent to the edge subcarrier of another OFDM channel's encompassed spectrum without any frequency guard band.

101.4.4 Upstream PMA transmit function

101.4.4.1 Overview

101.4.4.2 Time and frequency synchronization

CNU upstream frequency and transmission timing is based on downstream channel tracking, and in the case of timing, also on receiving and applying timing adjustments commanded by the CLT using the PHY Link Channel.

This subclause describes the CNU upstream transmission performance requirements for frequency and timing that are based on tracking the downstream input to the CNU, and receiving and operating on commands from the CLT.

101.4.4.2.1 OFDM channel frequency accuracy

The CNU shall lock the frequency of the upstream Subcarrier Clock (50 kHz) and lock each upstream subcarrier frequency to the 10.24 MHz Master Clock derived from the downstream OFDM signal.

All upstream subcarrier frequency specifications assume a downstream input to the CNU per 101.4.3.2 and 101.4.3.3 and a downstream received signal per 100.3.6.3 but with a CNR of at least 32 dB and received signal level of at least –15 dBmV for 6 MHz averaged for OFDM downstream.

The frequency of the upstream Subcarrier Clock shall be accurate within 0.4 ppm. Each subcarrier frequency shall be accurate to within 30 Hz. Both of these requirements are relative to the 10.24 MHz Master Clock reference, and both for five sigma of the upstream OFDMA transmissions, for subcarrier frequencies up to 204.8 MHz.

101.4.4.2.2 OFDM channel timing accuracy

For OFDMA upstream the ranging time offset is described in 102.4.1.6. The CNU shall implement the OFDMA timing adjustment to within ± 10 ns.

101.4.4.2.3 Modulation timing jitter

CNU OFDM Clock timing error relative to the CLT 10.24 MHz Master Clock as measured at the CLT shall be within ± 10 ns in each burst measured within any 35 second measurement period. This applies to the

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worst-case jitter and frequency drift specified for the CLT 10.24 MHz Master Clock and the CLT downstream OFDM Clock. The mean error is the result of the adjustment applied by the CNU as specified in 101.4.4.3.6.

101.4.4.3 Frame timing

The frame timing function is reset by the PHY Link during link auto-negotiation. The framing timing state machine (see Figure 101–31) implements the RB Superframe structure per 101.4.4.3.1.

101.4.4.3.1 RB Superframe configuration and burst transmission

The upstream Superframe shall be composed of the Probe Period followed by 256 OFDMA symbols. Each Probe Period is six OFDMA symbols in duration. An RB Frame is one Resource Block column (i.e., one column of Resource Blocks over the entire upstream spectrum). Each Resource Block is composed of one subcarrier and has a duration of either 8 or 16 symbols and is set using the *RBsize* variable. Changing the Resource Block duration results in a network restart. The superframe structure is illustrated in Figure 101–30.

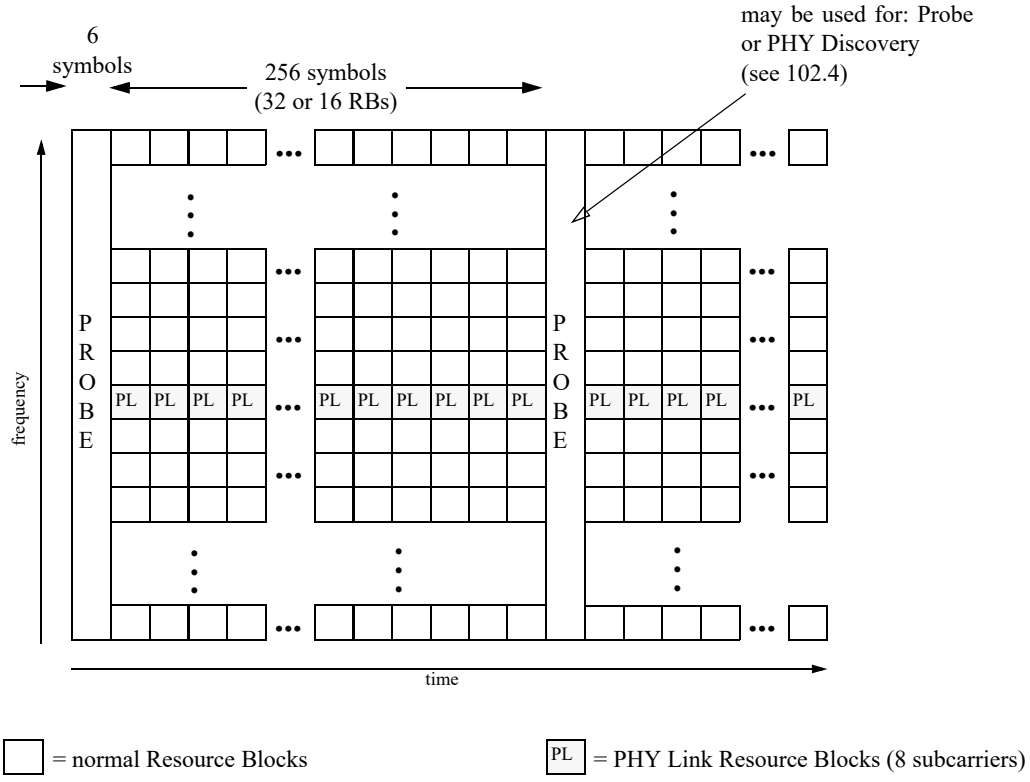

Figure 101–30—Upstream superframe structure

101.4.4.3.2 OFDMA transmission burst start

A CNU OFDMA transmission shall start with four contiguous subcarriers that include the start burst marker (see 101.4.4.8). No MAC data is transmitted during the burst marker.

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101.4.4.3.3 OFDMA transmission internal to a burst

In general Resource Blocks internal to a burst may be of Type 0, Type 1 or Type 2 as determined by the provisioned Pilot pattern (see 101.4.4.6). An OFDMA transmission may straddle excluded subcarriers, unused subcarriers, and the Probe Period. An example of this would be if the transmission burst start and stop markers straddle an exclusion band or if the burst start marker occurs in one RB Frame and the stop marker occurs in a subsequent RB Frame. In such cases, where the OFDMA transmission crosses a band edge (anywhere an excluded subcarrier is adjacent to an active subcarrier), the active subcarrier immediately adjacent to the band edge shall be of Type 2.

101.4.4.3.4 OFDMA transmission burst end

An OFDMA transmission shall end with four contiguous subcarriers that include the stop burst marker (see 101.4.4.8). No MAC data is transmitted during the burst marker.

101.4.4.3.5 Variables

RBsize

TYPE: Boolean
This variable determines the size of the upstream Resource Blocks. When *RBsize* is TRUE then Resource Block size is 16 symbols, When *RBsize* is FALSE then Resource Block size is 8 symbols.

RBlen(*RBsize*)

TYPE: integer
This integer represents the number of symbols for the configured Resource Block size. See Table 101–1.
Value: 8 when *RBsize* is FALSE, 16 when *RBsize* is TRUE.

SCLK

TYPE: Boolean
This clear on read variable is TRUE on every negative edge of a clock that is synchronized to the period of the Extended OFDM symbol time composed of the 20 μs useful symbol time plus the cyclic prefix time *USNcp*.

RBSF_reset

TYPE: Boolean
This variable is used to reset the frame timing state diagram (see Figure 101–31). A transition from FALSE to TRUE causes the state diagram to reset to the beginning of the RB_SUPERFRAME_RESET when *SCLK* goes TRUE. Upon being read this variable is reset to FALSE. The variable is set to TRUE on any reset or any Link-down condition (as defined in Table 102–14).

Probe_start

TYPE: Boolean
This variable transitions from the value of FALSE to TRUE for the first symbol of the Probe region. At the end of the first symbol of the probe region, the value transitions to FALSE until the first symbol of the next RB Superframe.

RB_Frame_start

TYPE: Boolean
This variable transitions from the value of FALSE to TRUE for the first symbol of each RB Frame in the RB Superframe as related to *RBsize*. The value is FALSE for all probe region symbols and for symbol 2 through *RBlen*(*RBsize)* for each RB Frame.

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SYMcount

TYPE: unsigned integer
This is variable is used for counting the symbols of the RB Superframe.

RBmod

TYPE: unsigned integer
This variable is used to set the symbols per RB Frame upon reset.

101.4.4.3.6 State diagram

The CLT PMA shall implement the frame timing process as shown in Figure 101–31.

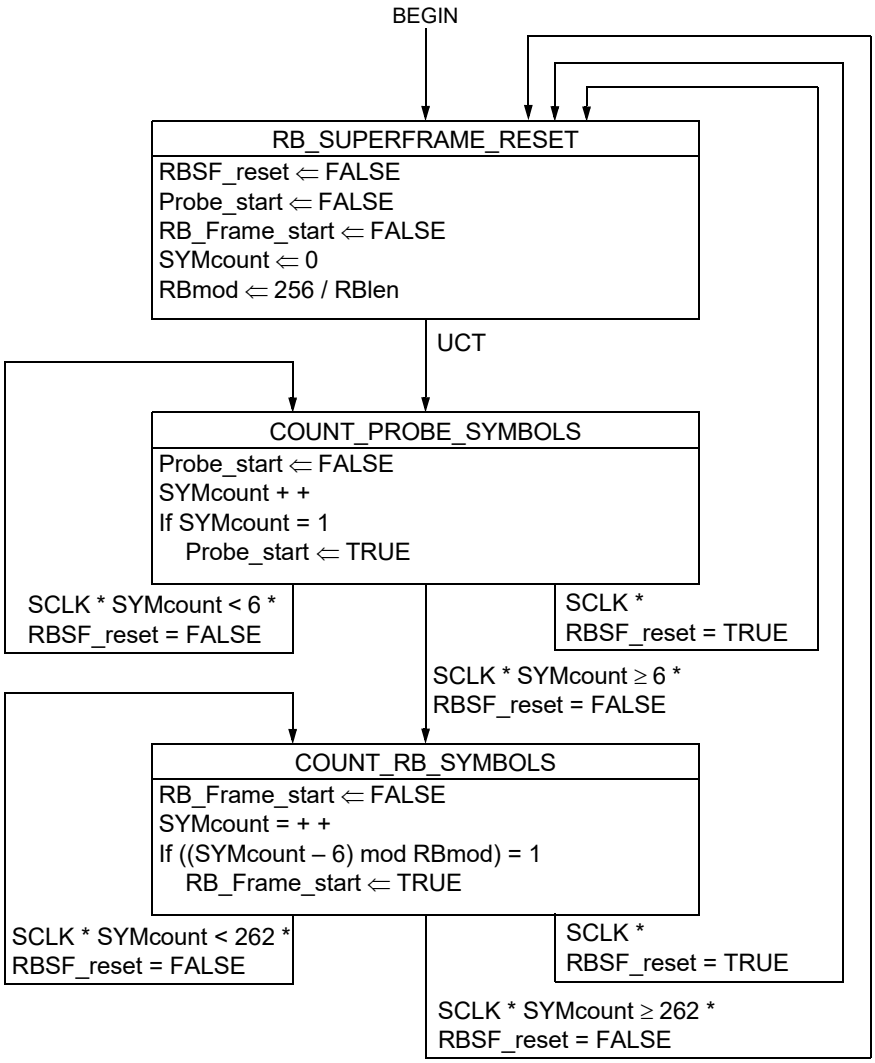

Figure 101–31—Framing timing state diagram

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101.4.4.4 Subcarrier configuration and bit loading

Each subcarrier in the OFDMA channel is configured using the *US_ModTypeSC(n)* (where $0 \le n \le 4095$) or *TypeN_Repeat/TypeN_Start* ($N = 1$ or 2) variables. These variables allow the PHY to configure each subcarrier to be nulled, to have a specific bit loading (such as 512-QAM or 1024-QAM), or to be excluded and to define the pilot pattern to be used in upstream transmissions. Subcarrier configuration in an EPoC OFDM channel of 192 MHz at the CNU shall conform to the rules outlined in Table 101–13.

All devices in an EPoC network share the same upstream subcarrier configuration and bit loading including nulled subcarriers, pilot pattern, bit loaded subcarriers, and excluded subcarriers.

Table 101–13—Upstream subcarrier configuration rules

Parameter	Limit	Unit
Minimum number of combined active and nulled subcarriers for Probe	180	Subcarriers
Minimum OFDMA channel guard band	1	MHz
Max OFDMA channel encompassed spectrum	190	MHz

101.4.4.4.1 Nulled subcarriers

Nulled subcarriers do not carry MAC or PHY Link data but may be used as probes. Nulled subcarriers are not modulated except when being used as a Probe Symbol in the upstream direction (see 102.4.2).

101.4.4.4.2 Bit loaded subcarriers

When a subcarrier is used to carry MAC data it uses the modulation type of QPSK or 2^n-QAM, where $4 \le n \le 16$, assigned via the *US_ModTypeSC(n)* variables except when used as an upstream pilot (see 101.4.4.6), Probe, PHY Discovery Response (see 102.4.1), or burst marker (see 101.4.4.8).

There is at least one contiguous 10 MHz or greater band of active subcarriers in the upstream 192 MHz OFDM channel (see Table 100–11). This may include subcarriers intended as Pilots and PHY Link subcarriers. A 1 MHz guard band of excluded subcarriers above and below this 10 MHz creates a minimum width OFDM channel of 10 MHz encompassed spectrum.

101.4.4.4.3 Excluded subcarriers

CNUs shall not transmit energy into a subcarrier that has been excluded from the OFDM channel (i.e., excluded subcarriers have zero amplitude). There is a band edge Exclusion Band at both the top and bottom of the OFDM channel.

101.4.4.4.4 PHY Link managed variables

US_ModAbility

TYPE: 2-bit binary

This bit mapped variable is used to declare which modulation types the PHY supports in the upstream direction for the MAC data path. When a bit read as TRUE it indicates that the PHY supports that modulation type.

Bit	Modulation type
0	2048-QAM
1	4096-QAM

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US_ModTypeSC(n)

TYPE: 4-bit binary

This set of provisioned variables determine the modulation parameters for each of the 4096 upstream OFDM subcarriers. $0 < n < 4095$. Each variable controls one of the 4096 subcarriers that are transmitted over the OFDMA channel, with *US_ModTypeSC(0)* controlling subcarrier zero, *US_ModTypeSC(1)* controlling subcarrier 1, etc. The assignment of bits to each modulation type is shown below:

bit 3 2 1 0
1 1 1 1 = Excluded subcarrier
1 1 1 0 = reserved
1 1 0 1 = reserved
1 1 0 0 = 4096-QAM
1 0 1 1 = 2048-QAM
1 0 1 0 = 1024-QAM
1 0 0 1 = 512-QAM
1 0 0 0 = 256-QAM
0 1 1 1 = 128-QAM
0 1 1 0 = 64-QAM
0 1 0 1 = 32-QAM
0 1 0 0 = 16-QAM
0 0 1 1 = 8-QAM
0 0 1 0 = QPSK
0 0 0 1 = BPSK (Used for continuous pilots only)
0 0 0 0 = null (carries no data)

101.4.4.5 Upstream symbol mapper

The upstream symbol mapper consists of an idle loop process and a fill process. The idle loop process is initialized when the upstream profile is configured and set to align with the start of the RB Superframe. An RB Superframe is composed of a Probe Period (first six OFDMA symbols) followed by 32 (*RBsize* value FALSE) or 16 (*RBsize* value TRUE) RB Frames (see 101.4.3.5). The main task of the idle loop is to walk through all data bits in all data carrying Resource Elements (in each RB Frame) at the clock rate established by *US_DataRate* (see 100.3.2.2). The fill process, upon an assertion of the start of a burst from the PMA Client, starts filling at the Resource Block, Resource Element, and fill bit that is at the current walk point. This includes placing the start burst marker elements, filling bits in data Resource Elements and low density pilots as specified, creating the QAM map for the fill word bits, sensing the end of burst, padding to the end of the current Resource Block, encoding and placing the end burst marker elements and then terminating. Both processes are continuous loops. During the idle walk and fill processes, two-dimensional arrays (Resource Block size by total subcarriers) termed RB Frames are allocated and passed to the staging process when complete. RB Frames initially consist of null values that correspond to excluded subcarriers. Non-null values are inserted by the fill process when mapping burst markers and filling data Resource Elements, and when later processed by the Pilot Insert process fill “P” type pilots patterns (see 101.4.4.6). Null Resource Blocks are equivalent to excluded subcarriers and produce no energy on the corresponding OFDMA subcarrier after the IDFT process.

101.4.4.5.1 Variables

BITPOS

TYPE: integer

This is an integer used by the fill process to indicate the current bit position being filled in *FillWord*.

END

TYPE: enumerated type

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This variable that ends the end state processing of the fill process, where:
FALSE indicates a *burstStart* = TRUE has not been received from received PMA_UNITDATA.request() primitive,
PAD indicates *burstStart* = TRUE has been received and the fill process is padding bits to the end of the current RB,
TRUE indicates that the fill process has reached the end of the last RB while padding.

FillWord<16:1>

TYPE: bit array
This an array that stages the bits to fill a Resource Element prior to mapping to QAM symbols.

FIRST

TYPE: Boolean
This is used within the fill process to indicate status of placing the first bit passed in the function call. If TRUE, the passed first bit is used, otherwise the bit from the processed PMA_UNITDATA.request() is used.

FRB

TYPE: integer
This variable is used to determine the current Resource Block being processed in the fill process. The range of values is from 0 to 4095.

FRE

TYPE: integer
This variable is used to determine the current Resource Element being processed in the fill process. The range of values is from –1 to 16.

ICLK

TYPE: Boolean
This clear on read variable is set to TRUE on each positive transition of a clock running at the *US_DataRate* (see 100.3.2.2).

IDLEBITS

TYPE: integer
This variable is used by the idle loop to increment through the bit loading of the current data carrying Resource Element.

IRB

TYPE: integer
This variable is used to determine the current Resource Block being processed in the idle process. The range of values is from –1 to 4095.

IRE

TYPE: integer
This variable is used to determine the current Resource Element being processed in the idle process. The range of values is from 0 to *RBlen*.

LBIT

TYPE: integer
This variable records the last bit filled in the current data Resource Element (QAM symbol) before mapping. The value can be from 1 to 15, where 1 represents the LSB. The value is set to the bit loading for the data Resource Element and then decremented during the symbol mapper fill process for mapping data burst bits to the current data Resource Element. This value is reset for each new data Resource Element being filled. The value is incremented while filling bits and stops incrementing upon receiving an end of burst indication. This value is not incremented or reset when placing padding bits.

LRE

TYPE: integer

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This variable records the last filled data Resource Element in the current Resource Block. The value can be from 1 to 16, where 1 represents the first Resource Element in the Resource Block (in time) and up to 8 or 16 (*RBlen*) representing the last Resource Element in the Resource Block (later in time). The value is reset for each new Resource Block being filled. The value is incremented to the current data Resource Element being filled and stops incrementing upon receiving an end of burst indication. This value is not incremented or reset when placing padding bits.

PILOT_MAP<4096>

TYPE: array of enumerated values

This array defines the pilot pattern use for Type 1 and Type 2 pilot patterns as defined in the upstream profile descriptor (see 101.4.4.6). The pilot pattern is fixed for the RB Superframe configuration and remains constant. The enumerated type values are as follows:

"EX": no Type 0, Type 1, or Type 2 pattern is configured for this subcarrier (i.e., nulled subcarriers and excluded)

"T0": this Resource Block, if used for data, contains a Type 0 pattern (see 101.4.4.6)

"T1": this Resource Block, if used for data, contains a Type 1 pattern (see 101.4.4.6)

"T2": this Resource Block, if used for data, contains a Type 2 pattern (see 101.4.4.6)

"PHYLINK": this Resource Block is reserved for use by the PHY Link

All other enumerated type values are reserved. For any used Resource Element containing data and not containing either a start or end burst marker, this value is used to set the *RB_Type* array element value for further processing by the pilot insertion and staging functions.

RB_Frame<4096, *RBlen*>

TYPE: Array of *I_value* and *Q_value* bin value pair.

This two-dimensional array holds the I and Q QAM symbol bin values that are passed from the symbol mapper to the staging function, then to the IDFT for transmission by the CNU. When first allocated, *RB_Frame* contains null values ("0") in all I and Q values. I and Q bin values are signed 16-bit integers. Index 4095:0 represents the total number of possible subcarriers in the upstream corresponding OFDMA channel, *RBlen* represents the number of Resource Elements in Resource Block. Subcarrier 0, RB number 1 (*RB_Frame*<0,1>) is reserved for special use in coordinating symbol mapper idle and fill processing: I_value of "0" indicates the *RB_Frame* has not transferred to the staging process, *I_value* of "1" indicates the *RB_Frame* has been passed to the staging process, *Q_value* is always "0".

RB_Type<4096>

TYPE: array of enumerated values

This array defines the use of each Resource Block, the values and descriptions are as follows:

"EX": the Resource Block is excluded (no energy output from IDFT), all Resource Elements contain null I and Q value pairs.

"T0": Resource Block in use, Type 0 pilot pattern (see 101.4.4.6)

"T1": Resource Block in use, Type 1 pilot pattern (see 101.4.4.6)

"T2": Resource Block in use, Type 2 pilot pattern (see 101.4.4.6)

"SM": Resource Block in use, contains a start marker pattern

"EM": Resource Block in use, contains an end marker pattern

All other enumerated type values are reserved. The use of this array indicates the availability and type of each used Resource Block to pilot insertion. A null (unused) Resource Block array element produces no energy output from the IDFT for the corresponding OFDMA subcarrier. (This is also true for excluded subcarriers).

RBlen(*RBsize*)

See 101.4.4.3.5.

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101.4.4.5.2 Functions

Allocate_RB_Frame(*RB_Frame*, *RB_Type*)

This function allocates a new *RB_Frame* array with all *I_value* and *Q_value* bin pairs set to null "0" and a new *RB_Type* array with all enumerations set to "EX".

BITLOAD(*resource_element*, *Resource Block*)

This function returns the current bit loading capacity of the current data carrying Resource Element or low density pilot. Bit loading is based on the setting of *US_ModTypeSC(n)* for this Resource Block (subcarrier) as well as Resource Elements containing low density pilots in Type 2 Resource Blocks (see 101.4.4.6).

Initialize_Pilot_Map()

This function initializes the *PILOT_MAP*<> array based on the descriptor information for indicating Type 0, Type 1, and Type 2 patterns. See 101.4.4.6.

Map_End_Marker (*RB_number*, *Last_Bit*, *Last_RE*)

This function starts at the current *RB_number*. This function then constructs the end burst marker by encoding the *Last_Bit* and *Last_RE* information. See 101.4.4.8.3 for end marker encoding. The value of *Last_Bit* directly indicates fill position in the current Resource Element. A values of *Last_RE* ranges from "0" which indicates the first Resource Element of the Resource Block up to *RBlen* – 1.This function then places end burst marker elements in the Resource Block according to the *RBlen* of the Superframe. This function continues to increment Resource Blocks (subcarriers) and places the remaining end burst marker elements in the next usable Resource Block as indicated in *US_ModTypeSC(n)* setting in the upstream profile descriptor. For each Resource Block used for an end burst marker element, the corresponding entry in the *RB_Type* array is set to "EM". Excluded subcarriers and null subcarriers are skipped. The next usable Resource Block is defined as an *US_ModTypeSC(n)* value from binary 0001 (BPSK) to binary 1110 (16384-QAM) and not being used by the PHY Link.

If at any time this function increments beyond the last usable Resource Block in the current *RB_Frame*<> (highest usable subcarrier configured in the profile descriptor), it examines the *I_value* of *RB_Frame*<0,1>. If "0", this function sets the value to "1" and passes the *RB_Frame*<> array and *RB_Type* array to the staging function and allocates a new *RB_Frame*<> array and *RB_Type* array use the Allocate_RB_Frame() function. If *I_value* of *RB_Frame*<0,1> is "1", the function skips passing to staging and allocations, assumes a new *RB_Frame*<> has been allocated, and increments to the first data carrying Resource Block and Resource Element in the new *RB_Frame*<>.

Map_Start_Marker (*RB_number*)

This function begins by placing the first Resource Block of a start burst marker in the current Resource Block *RB_number*, according to the *RBlen* of the Superframe (see 101.4.4.8). This function continues to increment Resource Blocks (subcarriers) and placing the remaining start burst marker elements in the next usable Resource Block(s) as indicated in *US_ModTypeSC(n)* setting in the upstream profile descriptor [defined as a *US_ModTypeSC(n)* value from binary 0001 (BPSK) to binary 1110 (16384-QAM) and not being used by the PHY Link]. Excluded subcarriers and null subcarriers are skipped. After placing the last start burst marker Resource Block, this function returns the value in *RB_number*.

For each Resource Block used for a start burst marker element, the corresponding entry in the *RB_Type*<*RB_number*> array is set to "SM". The next usable Resource Block is defined as a *US_ModTypeSC(n)* value from binary 0001 (BPSK) to binary 1110 (16384-QAM) and not being used by the PHY Link.

If at any time this function increments beyond the last usable Resource Block in the current *RB_Frame* (highest usable subcarrier configured in the profile descriptor), it examines the I_value of *RB_Frame*<0,1>. If "0", this function sets the value to "1" and passes the *RB_Frame* array and *RB_Type* array to the staging function and allocates a new *RB_Frame* array and *RB_Type* array use the Allocate_RB_Frame() function. If I_value of

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RB_Frame<0,1> is "1", skips passing to staging and allocations, assume a new *RB_Frame* has been allocated, and increments to the first data carrying Resource Block and Resource Element in the new *RB_Frame*.

Map_to_QAM(*resource_block*, *resource_element* , *FillWord*, *FILLBITS*)

This function maps the bits in *FillWord*<> into the *I* and *Q* bin value pairs for the current Resource Element in the current *resource_block* (subcarrier) in *RB_Frame*<> (see 101.4.4.3). *Fillbits* represents the bitloading of the current data Resource Element or low density pilot, where *FillWord*<*Fillbits*> represents the MSB and *FillWord*<1> represents the LSB for the mapping.

If *RB_Type*<*resource_block*> is "EX", this function overrides the value and sets *RB_Type*<*resource_block*) to *PILOT_MAP*<*resource_block*> to indicate this Resource Block is in use and contains non-null values.

Next_RE(re*source_element*, *resource_block*)

This function increments to the next usable data carrying Resource Element starting from the passed resource_element number in the passed resource_block (subcarrier). This includes data carrying Resource Elements and low density pilots, pilot Resource Elements are skipped. See 101.4.4.6. The Resource Element is returned and may have a value from 1 to *RBlen*. If *resource_element* has a value of –1, this function increments to the next Resource Block and begins with the first useable Resource Element.

This function first increments to the next usable Resource Element in the current Resource Block. If necessary, this function increments to the next data carrying Resource Block (e.g., Type 0, 1, or 2). The Resource Block number (subcarrier) is from 0 to 4095.

When advancing to the next Resource Block and *FILL_STATE* = FILL, the value from *Pilot_Map*<*Resource Block*> sets the value of *RB_Type*<*Resource Block*>.

If at any time this function increments beyond the last usable Resource Block in the current *RB_Frame* (highest usable subcarrier configured in the profile descriptor), It examines the I_value of *RB_Frame*<0,1>. If "0", this function sets the value to "1" and passes the *RB_Frame* array and *RB_Type* array to the staging function and allocates a new *RB_Frame* array and *RB_Type* array using the allocate_RB_Frame() function. If I_value of *RB_Frame*<0,1> is "1", it skips passing to staging and allocations, and assumes a new *RB_Frame* has already been allocated, and increments to the first data carrying Resource Block and Resource Element in the new RB Frame.

Upon return, the updated Resource Element index is returned via *resource_element*, and the current Resource Block (subcarrier) index returned via *resource_block*.

Reset_Scrambler()

The upstream symbol mapper utilizes a separate instantiation of the scrambler as described in 101.4.3.7 with the same seed value of 0x4732BA. This function initializes the bit scrambler with the seed value.

Scramble(*bit*)

This function provides a bit scrambler, local to the upstream data symbol mapper function. The passed *bit* is used as input to the scrambler, the output is used as the return value. See 101.4.3.7.

101.4.4.5.3 State diagrams

The CNU PMA shall perform the symbol mapper idle process as shown in Figure 101–32.

The CNU PMA shall perform the symbol mapper fill process as shown in Figure 101–33.

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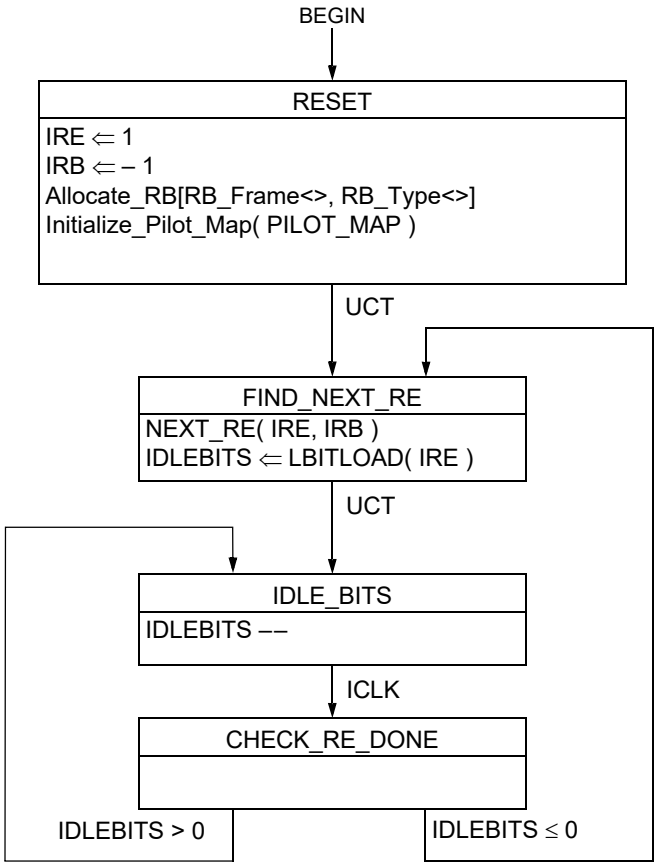

Figure 101–32—Upstream symbol mapper idle loop state diagram

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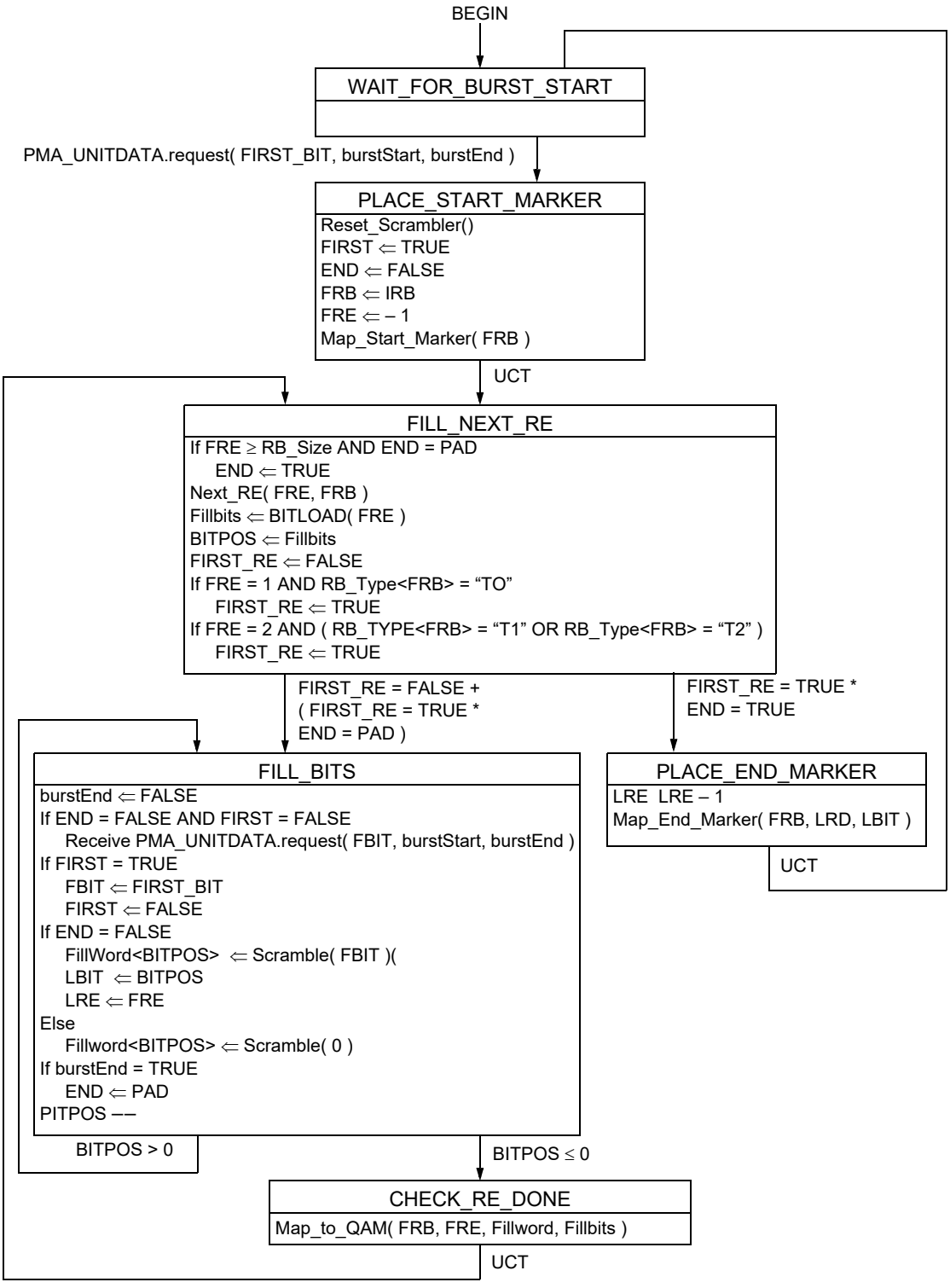

Figure 101–33—Upstream symbol mapper fill process state diagram

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101.4.4.5.4 Minimum gap time and burst marker overhead

The CLT ensures a minimum gap time between bursts from any CNU equal to the transmission time of one Resource Block expressed in units of *time_quantum*.

Let *Highestbitload* be the highest bit loading among all active subcarriers in any data carrying symbol (non-probe symbol) in an upstream RB frame, the number of *time_quantum* per Resource Block is calculated as per Equation (101–33):

$$RB\_time\_quanta = \lceil RBlen \times (Highestbitload) / (US\_DataRate) / (time\_quantum) \rceil \quad (101–33)$$

Start and end burst marker overhead is a multiple of *RB_time_quanta*. For *RBlen* of 8, total burst marker overhead is eight (8) times *RB_time_quanta*. For *RBlen* of 16, total burst marker overhead is four (4) times *RB_time_quanta*. See 101.4.4.8 for burst marker Resource Block use.

101.4.4.6 Pilot patterns

A Resource Block may be any one of three types as illustrated in Figure 101–34. Type 0 Resource Blocks contain only data Resource Elements modulated per the *ModTypeSC(n)* variable where *n* is the subcarrier index of the Resource Block. Type 1 Resource Blocks contain two pilots in the first and third Resource Element transmitted. Type 2 Resource Blocks contain a Low Density Pilot, in the last and third from last Resource Elements transmitted, in addition to the two pilots of the Type 1 Resource Block. The Low Density Pilot Resource Element is modulated using the higher modulation order of either BPSK or 4 bits lower than the bit loading specified in the *ModTypeSC(n)* variable for that subcarrier. Each RB type is configured via the variables *Type1_Start*, *Type1_Repeat*, *Type2_Start*, and *Type2_Repeat* as described next. The configuration of these variables determines the upstream transmission pilot pattern that all CNUs in the network use. However the pattern is defined over the entire 4095 subcarrier range with subcarrier 0 being the first subcarrier and subcarrier 4095 being the last subcarrier in the range. Excluded subcarrier settings override the pilot pattern definition, and Type 2 pilot definitions override Type 1 definitions. See 101.4.4.3.1 for additional rules on Pilot Type usage in burst transmissions.

The *TypeN_Start* variable determines on which subcarrier the repeating pattern for Type N pilot starts and the *TypeN_Repeat* variable determines the number of subcarriers between Type N pilots in the repeating pattern is encoded as shown in Table 101–14. *US_ModTypeSC(n)* excluded subcarriers override the repetitive pilot pattern and the Type 2 Pilot pattern overrides the Type 1 Pilot pattern.

Table 101–14—TypeN_Repeat[a] encoding

TypeN_Repeat value	Number of SC between TypeN Pilots
000	TypeN Pilot pattern disabled
001	0
010	1
011	3
100	7
101	15
11x	reserved

[a] $N = 1$ or 2

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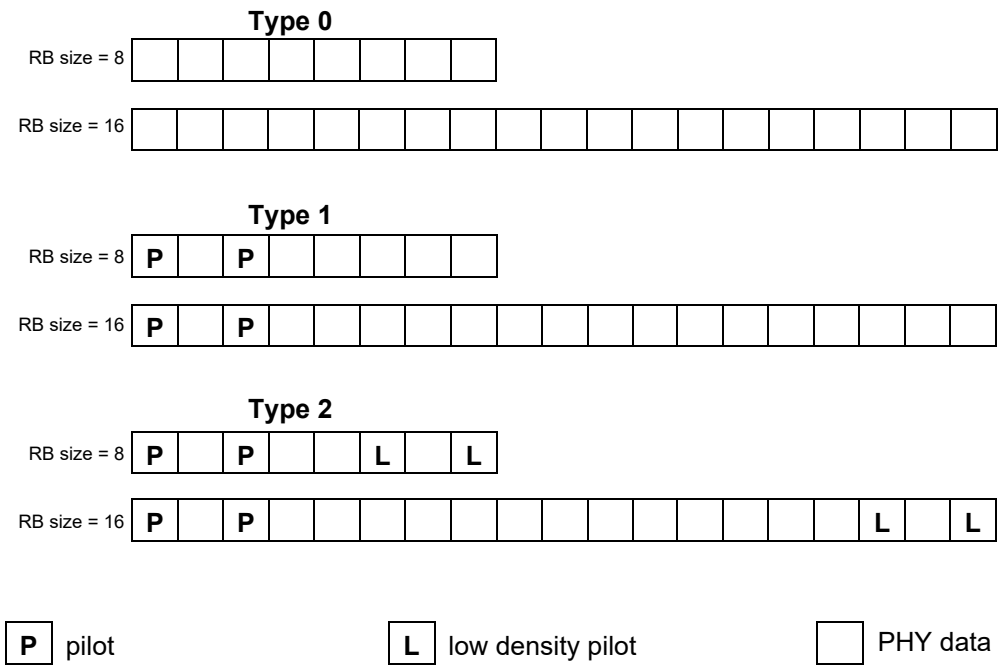

Figure 101–34—Resource Block types

101.4.4.6.1 variables

Type1_Repeat
: TYPE: 3-bit unsigned integer
This variable indicates the number of subcarriers, from 0 to 7, between repeating Type 1 Pilots.

Type1_Start
: TYPE: 4-bit unsigned integer
This variable indicates the number, between 0 and 15, of the first subcarrier designated as a Type 1 Pilot.

Type2_Repeat
: TYPE: 3-bit unsigned integer
This variable indicates the number of subcarriers, from 0 to 7, between repeating Type 2 Pilots.

Type2_Start
: TYPE: 4-bit unsigned integer
This variable indicates the number, between 0 and 15, of the first subcarrier designated as a Type 2 Pilot.

101.4.4.7 Staging and pilot insertion

101.4.4.7.1 Staging

The Staging function accepts an *RB_Frame* and *RB_Type* array from the Symbol Mapper when transferred from the Symbol Mapper. Staging then accumulates (copies) a PHY Link RB Frame (8 subcarriers by

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Resource Block size 8 or 16) if available for this *RB_Frame*. If a PHY Link RB Frame was copied, the *RB_Type* entries for the corresponding subcarriers are set to "T2" (see *RB_Type* array in 101.4.4.5.1).

Pilot insertion then proceeds as per the procedure in 101.4.4.7.2. Upon a positive transition of *RB_Frame_start* (value FALSE to value TRUE) as set by frame timing, the *RB_Frame* and *RB_Type* arrays are transferred to the IDFT process.

101.4.4.7.2 Pilot insertion

Upstream pilot insertion is performed using a BPSK mapped bit sequence generated by a pseudo-random sequence (PRBS) generator defined by the polynomial $x^{12} + x^9 + x^8 + x^5 + 1$ (illustrated in Figure 102–27). Pilots are inserted after the RB Frame is processed by the symbol mapper (see 101.4.3.8) and before the RB Frame is passed to the IDFT function.

The method for pilot insertion shall be as follows:

1) The PRBS generator is initialized with the seed value 0xBFF at the beginning of each RB Frame for the subcarrier with index k=0 of the IDFT Equation (101–25) (see 101.4.3.11).
2) the PRBS generator is clocked once for every subcarrier of the IDFT.
3) Pilots are inserted (mapped) into the "P" positions of PHY Link subcarriers in each subcarrier where a CNU is transmitting a PHY Link message (see 102.3.4) and in each Resource Block to be transmitted containing a data burst designated as Type 1 or Type 2 Resource Block (see 101.4.4.6).
4) "P" pilots are BPSK modulated with the output of the feedback shift register, with a value of 0 mapping to (1 + j0) and a value of 1 mapping to (–1 + j0).
5) The same BPSK value is used for each "P" location in a subcarrier.

When an RB Frame has been processed by this function, the RB Frame is passed to the IDFT function for further processing.

101.4.4.8 Burst markers

101.4.4.8.1 Introduction

Burst markers are used to indicate the start or end of a burst received via the PMA service interface. A burst marker is a predefined sequence of two types of burst marker elements: B's and 0's, where B's represent differential QPSK (D-QPSK) modulated symbols (see 101.4.4.8.3), and 0's represent nulls (i.e., no energy being transmitted). Each burst marker element is transmitted in one Resource Element. B burst marker elements are boosted by 3 dB. The first modulated B marker element on a subcarrier is encoded as a reference pilot. There are separate burst marker patterns for 8 and 16 symbol Resource Blocks.

Burst markers are placed by the upstream Symbol Mapper function (see 101.4.4.5).

101.4.4.8.2 Burst marker start and stop sequences

For the 8 symbol Resource Block, the start and stop burst marker sequences are defined in Figure 101–35. For the 16 symbol Resource Block, the start and stop marker sequences are defined in Figure 101–36.

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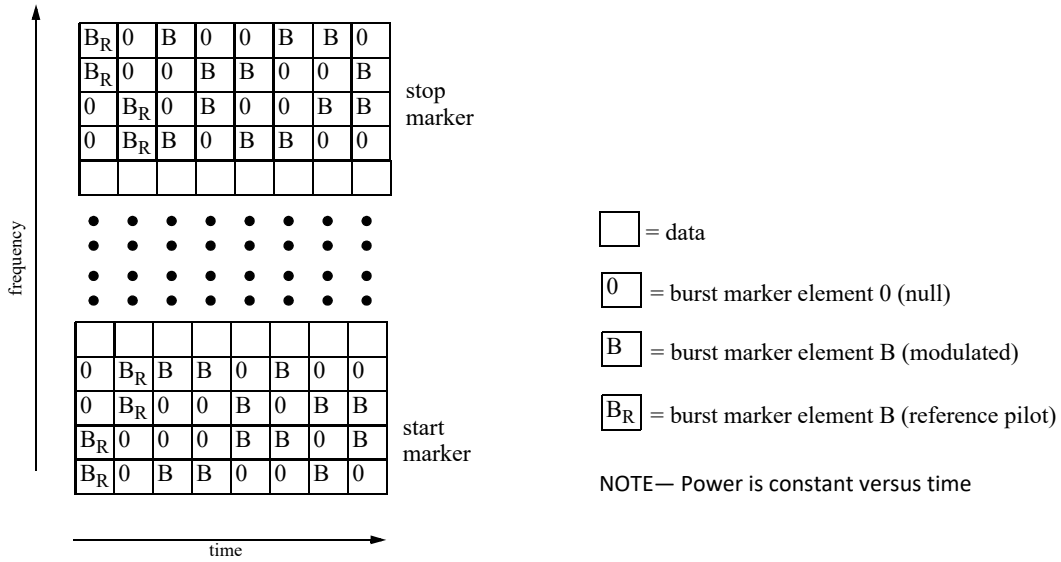
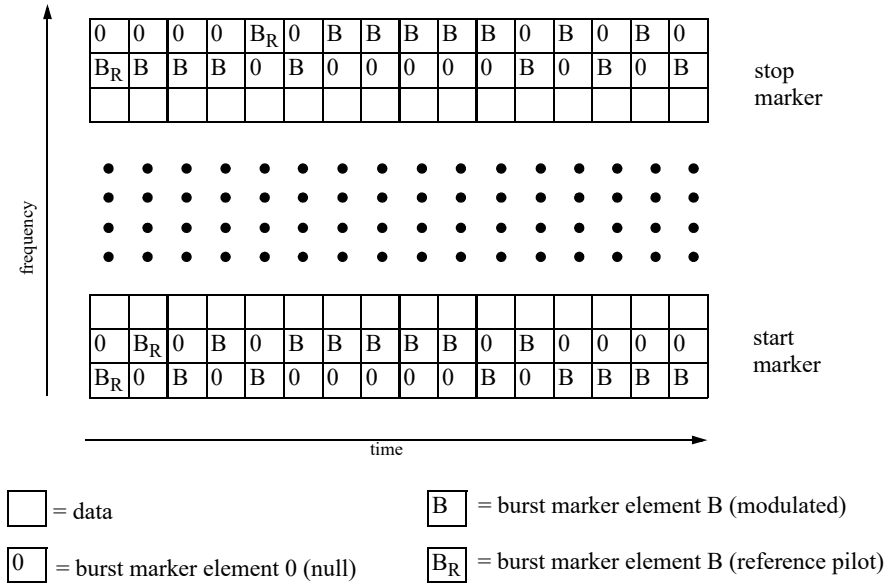


Figure 101–35—Burst marker in 8 symbol Resource Block



NOTE—Power is constant versus time.

Figure 101–36—Burst marker example in 16 symbol Resource Block

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101.4.4.8.3 Burst marker B element encoding

The first modulated D-QPSK symbol for each subcarrier of a start and end burst marker is a reference pilot and is modulated with value (11). This is indicated by the position of the B_R burst marker element in Figure 101–35, Figure 101–36, Figure 101–37, and Figure 101–38.

The remaining B burst marker elements are D-QPSK modulated with information value pairs and parity encoding value pairs. The parity encoding is a Reed-Solomon coding over GF(2^4) with $t = 2$. The Reed-Solomon code of RS(15,11) is shortened to length 6 of 7 depending on the Resource Block length. The RS generator is shown in equation Equation (101–34) where the primitive element alpha (a) is 0x2.

$$g(x) = (x + a^0)(x + a^1)(x + a^2)(x + a^3) \quad (101–34)$$

The RS primitive polynomial is shown in equation Equation (101–35).

$$p(x) = x^4 + x + 1 \quad (101–35)$$

For Resource Block size of 8, two information code symbols designated I2 and I1 contain 8 information bits and are encoded and shortened to a length of 6:

(0 0 0 0 0 0 0 0 I2 I1 P4 P3 P2 P1)

For Resource Block size of 16, three information code symbols designated I3, I2, and I1 contain 12 information bits and are encoded and shortened to a length of 7:

(0 0 0 0 0 0 0 0 I3 I2 I1 P4 P3 P2 P1)

Each information code symbol is represented by a pair of D-QPSK symbols. The high order pair is designated as $I_{\#H}$ and the low order pair by $I_{\#L}$, for # = 1, 2, or 3. For each parity code symbol high order pair is designated as $P_{\#H}$ and the low order pair by $P_{\#L}$, for # = 1, 2, 3, or 4.

For start burst markers and Resource Block size 8, the two information code symbols I2 and I1 are each set to 0xF (i.e., 0xFF, all ones in all information symbols) with the D-QPSK modulated symbol pair placement as per Figure 101–37.

For start burst markers and Resource Block size 16, the three information code symbols I3, I2, and I1 are each set to 0xF (i.e., 0xFFF, all ones in all information symbols) with the D-QPSK modulated symbol pair placement as per Figure 101–38.

The start burst marker setting of 0xFF and 0xFFF in RB Frames of size 8 and 16, respectively designates that the first bit of data for the burst starts in the MSB bit of the first usable data Resource Element in the Resource Block immediately following the start burst marker. All other values and designations are reserved.

For stop burst markers and Resource Block size 8, the two information code symbols are set as follows: L_2 encodes the last Resource Block value as designated by the symbol mapper (see 101.4.4.5) as per Table 101–15 and L_1 encodes the last fill bit position value as designated by the symbol mapper (see 101.4.4.5) as per Table 101–16 with the D-QPSK modulated symbol pair placement as per Figure 101–37.

For stop burst markers and Resource Block size 16, the three information code symbols are set as follows: L_3 encodes a pad value of 0x00 (i.e., not null), L_2 encodes the last Resource Block value as designated by the symbol mapper (see 101.4.4.5) as per Table 101–15, and L_1 encodes the last fill bit position value as desig-

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nated by the symbol mapper (see 101.4.4.5) as per Table 101–16 with the D-QPSK modulated symbol pair placement as per Figure 101–38.

Table 101–15—Last Resource Element position encoding

Last Resource Element Position in Last Resource Block	MSB Pointer Bits $(I_{2H})I_{(2L)}$ $(0_{MSB}\ 0)_H\ (0_{MSB}\ 0)_L$
0	$(00)_H(00)_L$
1	$(00)_H(01)_L$
2	$(00)_H(10)_L$
3	$(01)_H(11)_L$
4	$(01)_H(00)_L$
5	$(01)_H(01)_L$
6	$(01)_H(10)_L$
7	$(01)_H(11)_L$
8	$(10)_H(00)_L$
9	$(10)_H(01)_L$
10	$(10)_H(10)_L$
11	$(10)_H(11)_L$
12	$(11)_H(00)_L$
13	$(11)_H(01)_L$
14	$(11)_H(10)_L$
15	$(11)_H(11)_L$

.

Table 101–16—Last bit position encoding

Last Fill Bit Position in Last Resource Element	MSB Pointer Bits $(I_{1H})I_{(1L)}$ $(0_{MSB}\ 0)_H\ (0_{MSB}\ 0)_L$
0	$(00)_H(00)_L$
1	$(00)_H(01)_L$
2	$(00)_H(10)_L$
3	$(01)_H(11)_L$
4	$(01)_H(00)_L$

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Table 101–16—Last bit position encoding *(continued)*

Last Fill Bit Position in Last Resource Element	MSB Pointer Bits $(I_{1H})I_{(1L)}$ $(0_{MSB}\ 0)_H\ (0_{MSB}\ 0)_L$
5	$(01)_H(01)_L$
6	$(01)_H(10)_L$
7	$(01)_H(11)_L$
8	$(10)_H(00)_L$
9	$(10)_H(01)_L$
10	$(10)_H(10)_L$
11	$(10)_H(11)_L$
12	$(11)_H(00)_L$
13	$(11)_H(01)_L$
14	$(11)_H(10)_L$
15	$(11)_H(11)_L$

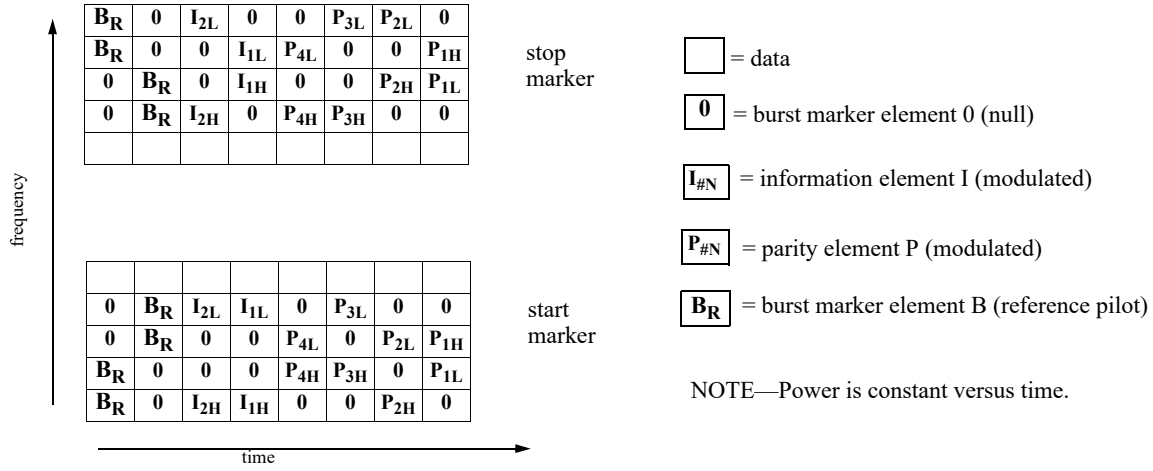

Figure 101–37—Burst marker encoding in 8 symbol Resource Block

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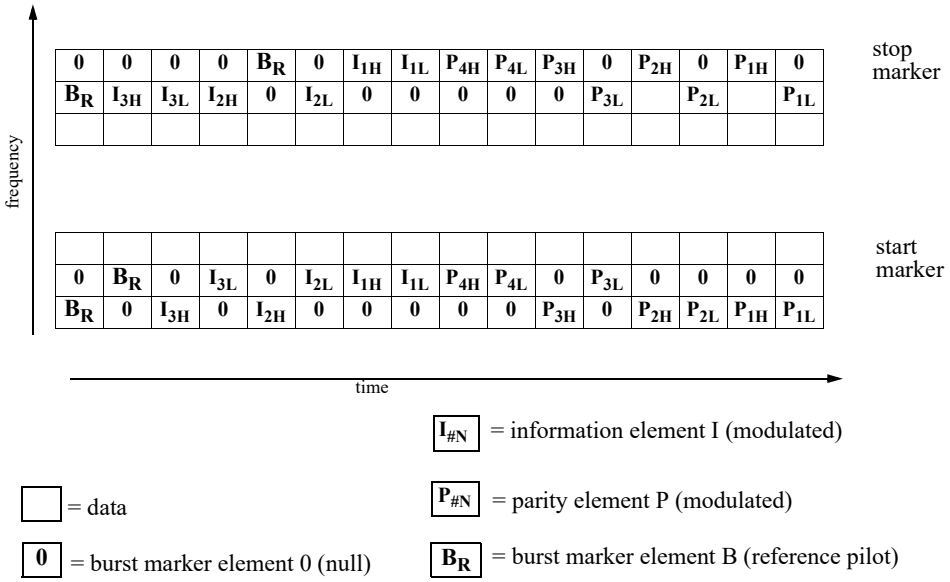

NOTE—Power is constant versus time.

Figure 101–38—Burst marker encoding in 16 symbol Resource Block

101.4.4.9 Pre-equalization and Inverse Discrete Fourier Transform (IDFT)

The CNU upstream IDFT uses the same definition as in the downstream. See 101.4.3.11.

101.4.4.9.1 Pre-equalization coefficients

Linear pre-equalization is performed in the digital domain before upstream IDFT processing. The CNU shall support a single complex coefficient (equalizer tap) per subcarrier that may be updated via the PHY Link. A CNU shall use a default value of 0 + j0 for all pre-equalizer coefficients. Changing a subcarrier from excluded to active or visa versa shall cause the pre-equalizer coefficients for that subcarrier to be automatically set to a value of 1 + j0 (for subcarriers set to active) or 0 + j0 (for subcarriers set to excluded).

On update, the PHY Link may either indicate a complex coefficient (initialization or reset) or may indicate a multiplication factor. Coefficients are updated only as part of a response to upstream probes received by the CLT. See 102.4.2.

Upon reception of a coefficient multiplication factor, the CNU processes the update per subcarrier as follows:

$$C(k) \Leftarrow C(k) \times A(k) \tag{101–36}$$

where

C(k)	is the pre-equalizer coefficient of the k-th subcarrier as used in the last probe transmission
A(k)	is the coefficient updates in variables *EQ_CoefR(k)* and *EQ_CoefI(k)* (see 101.4.4.9.2), received via the PHY Link
The symbol "×"	indicates a complex multiplication

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The CNU shall normalize the newly calculated coefficients by adjusting the mean of the absolute value of $(Ck)^2$ to be one. The summation is over all *k* active subcarriers. The CNU shall switch from the prior set of coefficients to the new set of coefficients between transmissions within 10 ms after receiving an update via a PHY Link message.

On transmissions, the CNU shall

1) Always pre-equalize all transmissions other than probe and PHY Discovery signals.
2) Transmit a probe signal with or without pre-equalization (all coefficients are reset to 1 + j0) as instructed by the CLT using the PHY Link probe instruction described in 102.4.2.

The CLT shall be able to calculate and distribute initial pre-equalizer coefficients to reduce the OFDMA channel amplitude variation, by 0.8 dB or more corresponding to a 3 dB increase in MER from 16 dB to 19 dB, given that the probe signal power into CLT burst receiver is +5.4 dBmV ± 1 dB and the upstream OFDMA channel has an encompassed spectrum of at least 22 MHz, where all subcarriers within the encompassed spectrum are active subcarriers.

Testing methodology for pre-equalizer can be found in 101.4.6.1.

101.4.4.9.2 PHY Link managed variables

EQ_CoefR(n)

TYPE: Q2.14 format signed fractional number
This set of variables determines the real and imaginary part of the pre-equalizer settings for the upstream transmitter. Each variable in the set controls one subcarrier of the 4096 subcarriers that are transmitted over the OFDMA channel, with *EQ_CoefR(0)* controlling the real number setting for subcarrier 0 and *EQ_CoefR(1)* controlling the real number setting for subcarrier 1 and so on. Thus *EQ_CoefR(4096)* controls the real settings for subcarrier 4095.

EQ_CoefI(n)

TYPE:Q2.14 format signed fractional number
This set of variables determines the real and imaginary part of the pre-equalizer settings for the upstream transmitter. Each variable in the set controls one subcarrier of the 4096 subcarriers that are transmitted over the OFDMA channel, with *EQ_CoefI(0)* controlling the imaginary number setting for subcarrier 0 and *EQ_CoefI(1)* controlling the imaginary number setting for subcarrier 1and so on. Thus *EQ_CoefI(4095)* controls the imaginary settings for subcarrier 4095.

101.4.4.10 Cyclic prefix and windowing

The CNU upstream cyclic prefix and windowing function uses the same definition as in the downstream. See 101.4.3.12. The CNU shall use one of the permissible values for *USNcp* and *USNrp* in the upstream direction given in Table 101–17 and Table 101–18, respectively. Cyclic prefix and windowing function sizes shall be selected such that the *USNrp* value is less than the *USNcp* value.

Table 101–17—Size of cyclic prefix (USNcp), upstream direction

USNcp[a]	[µs]
256	1.25
384	1.875
512	2.5

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Table 101–17—Size of cyclic prefix (USNcp), upstream direction *(continued)*

640	3.125
768	3.75

[a]USNcp is in units of OFDM Clock periods (1/204.8 MHz).

Table 101–18—Size of OFDM window (USNrp), upstream direction

USNrp[a]	[μs]
0	0
64	0.3125
128	0.625
192	0.9375
256	1.25

[a]USNrp is in units of OFDM Clock periods (1/204.8 MHz).

101.4.4.10.1 PHY Link managed variables

USNcp

TYPE: 4-bit binary
This variable controls the size of the cyclic prefix in the upstream direction per the following enumeration:
bit 3 2 1 0
1 x x x = reserved
0 1 1 1 = 768 OFDM Clock periods (1/204.8 MHz)
0 1 1 0 = 640 OFDM Clock periods (1/204.8 MHz)
0 1 0 1 = reserved
0 1 0 0 = 512 OFDM Clock periods (1/204.8 MHz)
0 0 1 1 = reserved
0 0 1 0 = 384 OFDM Clock periods (1/204.8 MHz)
0 0 0 1 = reserved
0 0 0 0 = 256 OFDM Clock periods (1/204.8 MHz)

USNrp

TYPE: 3-bit binary
This variable controls the size of the windowing function in the upstream direction per the following enumeration:
2 1 0
1 1 1 = 256 OFDM Clock periods (1/204.8 MHz)
1 1 0 = 192 OFDM Clock periods (1/204.8 MHz)
1 0 1 = reserved
1 0 0 = 128 OFDM Clock periods (1/204.8 MHz)
0 1 1 = reserved
0 1 0 = 64 OFDM Clock periods (1/204.8 MHz)
0 0 1 = reserved
0 0 0 = 0 samples (windowing disabled)

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101.4.5 Constellation structure and mapping

After LDPC encoding and scrambling for downstream and upstream transmissions, the output bit stream of the CLT and CNU Symbol Mapper shall be mapped to QAM symbols such that first bit is the least-significant bit of the first QAM subcarrier constellation m-tuple, see Figure 101–39.

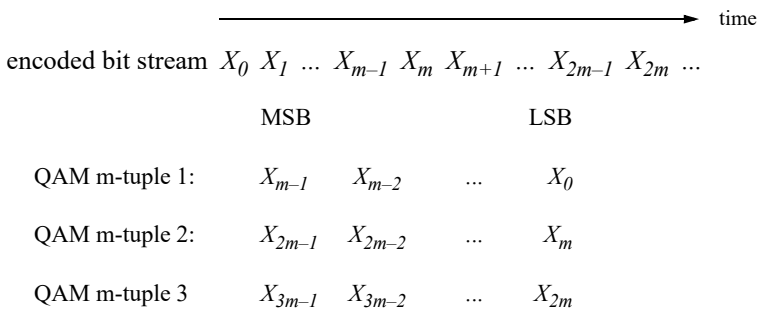

Figure 101–39—Bitstream to QAM m-tuple mapping

The m-tuples are modulated onto subcarriers using QAM constellation. As described in the following subclauses, the QAM constellation structure and mappings are defined inductively and use Gray mapping as their base.

101.4.5.1 One dimensional Gray mapping for m-tuple binary bits

1) When m=1, the Gray mapping is define to be $\text{Gray}_1(0) = 1$ and $\text{Gray}_1(1) = -1$
2) When m>1, the Gray mapping is defined inductively, i.e.,

$$\text{Gray}_m(x_{m-1} \cdot x_{m-2} \cdot \ldots \cdot x_0) = (1 - 2 \cdot x_0) \cdot \left(2^{m-1} + \text{Gray}_{m-1} \cdot (x_{m-1} \cdot x_{m-2} \cdot \ldots \cdot x_0)\right)$$

101.4.5.2 Constellation structure and mapping of BPSK

Let m = 1 and a binary bit is x. The BPSK mapping is as follows:

$$(I_1(x), Q_1(x)) = (\text{Gray}_1(x), 0) = \begin{cases} (1, 0) & (x = 0) \\ (-1, 0) & (x = 1) \end{cases}$$

Also, see Figure 101–40.

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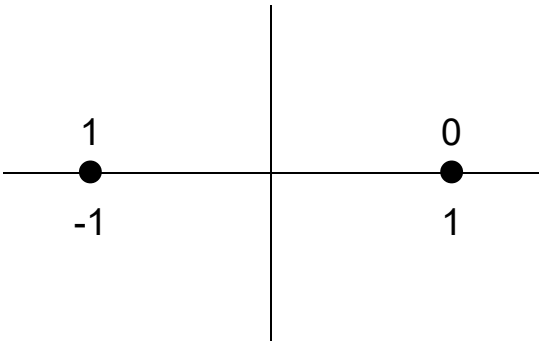

Figure 101–40—BPSK

101.4.5.3 Constellation structure and mapping of 2^{2n}–QAM

Let $m = 2 \cdot n$ and the m-tuple binary bits are $x_0, ..., x_{n-1}, x_n, ..., x_{2 \cdot n - 1}$. The mapping from that m-tuple to a 2^m–QAM is defined by

$$(I_{2n}(x_{2n-1}, ..., x_n, x_{n-1}, ..., x_0), Q_{2n}(x_{2n-1}, ..., x_n, x_{n-1}, ..., x_0)) = (\text{Gray}_n(x_{n-1}, ..., x_0), \text{Gray}_n(x_{n-1}, ..., x_0)) \quad (101–37)$$

where the Gray mapping is defined in 101.4.5.1. Some of the examples are given in the following figures.

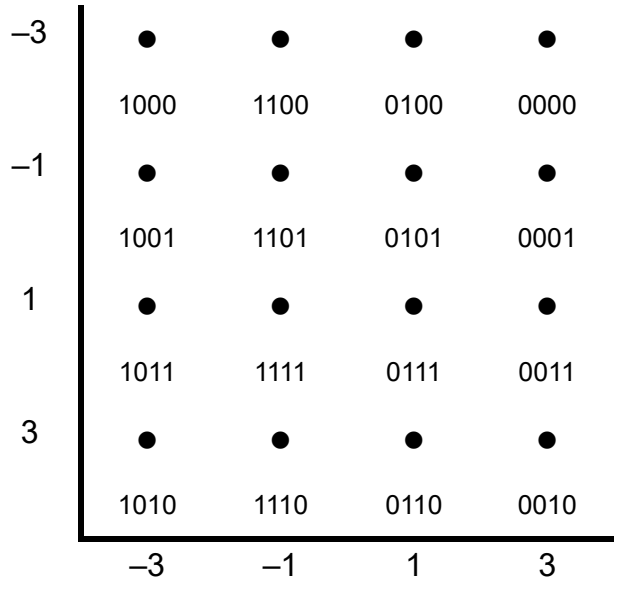

Figure 101–41—16-QAM

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101.4.5.4 Constellation structure and mapping of 2^{2n+1}–QAM (n>0)

Let $m = 2n + 1$ and the m-tuple binary bits are $x_0, ..., x_{n-1}, x_n, ..., x_{2n}$. Firstly, map this m-tuple to a rectangular constellation defined by

$$(I_{rct}(x_{2n}, ..., x_n, x_{n-1}, ..., x_0), Q_{rct}(x_{2n}, ..., x_n, x_{n-1}, ..., x_0)) = (\text{Gray}_{n+1}(x_{2n}x_{2n-1}...x_n), \text{Gray}_n(x_{n-1}, x_{n-2}, ..., x_0)) \quad (101\text{–}38)$$

where the Gray mapping is defined in 101.4.5.1. Then the structures and mappings of cross-constellations are generated in the following subclauses.

101.4.5.4.1 Constellation structure and mapping of 8–QAM

Let the constellation signal and its mapping be denoted by $(I_3(x_2x_1x_0), Q_3(x_2x_1x_0))$ then

$$\begin{cases} \begin{cases} I_3(x_2x_1x_0) = I_{rct}(x_2x_1x_0) + 1 \\ Q_3(x_2x_1x_0) = Q_{rct}(x_2x_1x_0) \end{cases} & I_{rct}(x_2x_1x_0) < 3 \\ \begin{cases} I_3(x_2x_1x_0) = 3 - I_{rct}(x_2x_1x_0) \\ Q_3(x_2x_1x_0) = sign(Q_{rct}(x_2x_1x_0)) \times (\left|Q_{rct}(x_2x_1x_0)\right| + 2) \end{cases} & \text{otherwise} \end{cases}$$

where the sign function is defined by $sign(a) = \begin{cases} 1 & a \geq 0 \\ -1 & a < 0 \end{cases}$

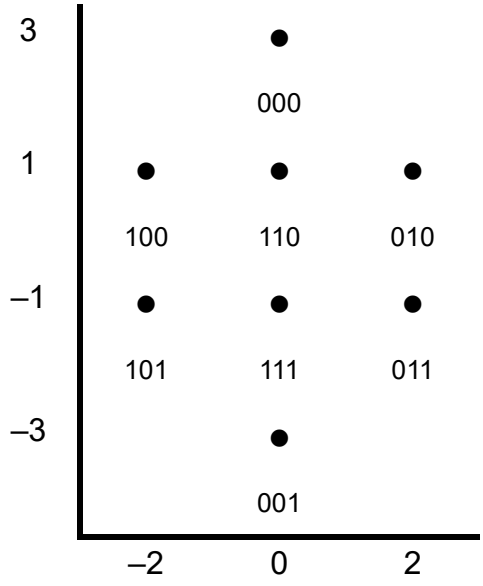

Figure 101–42—8-QAM

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101.4.5.4.2 Constellation structure and mapping of 2^{2n+1}–QAM with $n > 1$

Let the mapping be denoted by $(I_{2n+1}(x_{2n}x_{2n-1}...x_0), Q_{2n+1}(x_{2n}x_{2n-1}...x_0))$ and let $s = 2^{n-1}$.

Then, when $\left|I_{rct}(x_{2n}x_{2n-1}...x_0)\right| < 3s$

$$\begin{cases} I_{2n+1}(x_{2n}x_{2n-1}...x_0) = I_{rct}(x_{2n}x_{2n-1}...x_0) \\ Q_{2n+1}(x_{2n}x_{2n-1}...x_0) = Q_{rct}(x_{2n}x_{2n-1}...x_0) \end{cases}$$

and when $\left|I_{rct}(x_{2n}x_{2n-1}...x_0)\right| \geq 3s$

$$\begin{cases} \begin{cases} I_{2n+1}(x_{2n}x_{2n-1}...x_0) = sign(I_{rec}(x_{2n}x_{2n-1}...x_0)) \times (\left|I_{rct}(x_{2n}x_{2n-1}...x_0)\right| - 2s) \\ Q_{2n+1}(x_{2n}x_{2n-1}...x_0) = sign(Q_{rct}(x_{2n}x_{2n-1}...x_0)) \times (4s - \left|Q_{rct}(x_{2n}x_{2n-1}...x_0)\right|) \end{cases} & \text{if } \left|Q_{rct}(x_{2n}x_{2n-1}...x_0)\right| > s \\ \begin{cases} I_{2n+1}(x_{2n}x_{2n-1}...x_0) = sign(I_{rec}(x_{2n}x_{2n-1}...x_0)) \times (4s - \left|I_{rct}(x_{2n}x_{2n-1}...x_0)\right|) \\ Q_{2n+1}(x_{2n}x_{2n-1}...x_0) = sign(Q_{rct}(x_{2n}x_{2n-1}...x_0)) \times (\left|Q_{rct}(x_{2n}x_{2n-1}...x_0)\right| + 2s) \end{cases} & \text{if } \left|Q_{rct}(x_{2n}x_{2n-1}...x_0)\right| \leq s \end{cases}$$

Figure 101–43 presents the 32-QAM structure and mapping.

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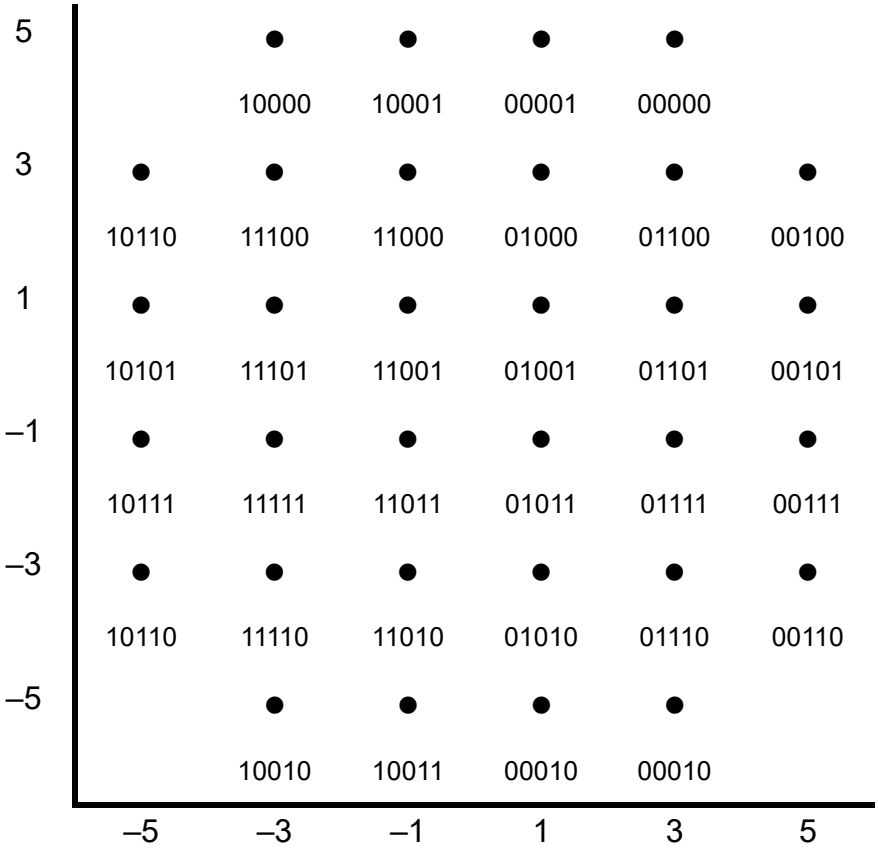

Figure 101–43—32-QAM

101.4.5.5 QAM constellation scaling

Both real and imaginary axis of a QAM constellation shall be scaled by the CLT or CNU transmitter using the scaling factors given in Table 101–19. These scaling factors ensure that the mean square value of all QAM constellations are equal to one.

Table 101–19—QAM constellation scaling factors

QAM constellation	*m* number of bits	Scaling factor
BPSK	1	1
QPSK	2	$1/(\sqrt{2})$
8-QAM	3	$1/(\sqrt{5})$
16-QAM	4	$1/(\sqrt{10})$
32-QAM	5	$1/(\sqrt{20})$
64-QAM	6	$1/(\sqrt{42})$

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Table 101–19—QAM constellation scaling factors *(continued)*

QAM constellation	*m* number of bits	Scaling factor
128-QAM	7	$1/(\sqrt{82})$
256-QAM	8	$1/(\sqrt{170})$
512-QAM	9	$1/(\sqrt{330})$
1024-QAM	10	$1/(\sqrt{682})$
2048-QAM	11	$1/(\sqrt{1322})$
4096-QAM	12	$1/(\sqrt{2730})$
8192-QAM	13	$1/(\sqrt{5290})$
16384-QAM	14	$1/(\sqrt{10922})$

101.4.6 PMA testing

101.4.6.1 Pre-equalization testing

Pre-equalization operation is verified using the following method:

1) A test modulator generates the first transmission using a compliant probe. This transmission is input into a spectrum analyzer, with an initial "flat" test channel, achieving 0.3 dB peak-to-peak amplitude variation or less after calibration of the spectrum analyzer (corresponding to a residual MER of 35 dB).
2) A micro-reflection is added into the test channel with an amplitude of –16 dB ± 0.5 dB and a delay of 312.5 ± 0.5 ns compared to main path.
3) Verify the channel (except for the echo) changes by no more than 0.3 dB peak-to-peak, in addition to the 2.78 dB peak-to-peak signal amplitude variation induced by the micro-reflection (the 0.3 dB tolerance allows the maximum amplitude variation to increase to 3.08 dB peak-to-peak corresponding to total MER of 15.3 dB or a residual MER of 35 dB).
4) The test modulator generates a second transmission using a compliant probe sent to both the spectrum analyzer and the CLT receiver (unit under test) with a CNR > 35 dB.
5) Measure and record the amplitude variation over the spectrum of subcarriers (this is the "reference amplitude variation measurement" of the test) using the spectrum analyzer.
6) The CLT OFDMA receiver develops pre-equalizer coefficients.
7) The CLT formats and transmits compliant commands for the pre-equalizer coefficients.
8) The downstream test receiver validates reception of pre-equalization coefficients.
9) The received pre-equalization coefficients are implemented by the test modulator and used to generate a third transmission.
10) Measure and record the amplitude variation over the spectrum of subcarriers for this third transmission, pre-equalized, from the test modulator.
11) Compare the amplitude variation measurement taken in step 10) to the reference amplitude variation measurement. The difference observed should be less than the required minimum reduction in amplitude variation.

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101.4.6.2 OFDM channel frequency accuracy test

The measurements of the frequency of the upstream Subcarrier Clock, and the subcarrier frequencies, are averaged over the duration of a single upstream burst. A constant temperature is maintained during the measurements within a range of 20 ºC ± 2 ºC. A minimum warm up time of 30 min occurs before the CNU frequency measurements are made.

NOTE—As an example, upstream Subcarrier Clock frequency is linked with upstream FFT duration (and subcarrier spacing in the frequency domain), and is at least one component in developing each upstream subcarrier frequency. Other components may also contribute to upstream subcarrier frequency, for example, an up conversion process from complex baseband or low intermediate frequency may contribute. All such components are locked to the derived 10.24 MHz Master Clock at the CNU. The accuracy requirements for the Subcarrier Clock frequency and for each individual subcarrier frequency necessary to support 4K-QAM upstream are not necessarily the same.

101.5 Applicability of Clause 90 and IEEE Std 802.1AS, Clause 13 for EPoC time transport

This subclause describes how the time synchronization functionality for EPON included in IEEE Std 802.1AS can also be used for EPoC time synchronization with minor adjustments to compensate for CLT and CNU PHY time delays described in Clause 90. CLTs and CNUs should use the methods described in 101.5.1 and 101.5.2.

101.5.1 CLT PHY asymmetry correction of future time transmitted by the CLT to CNU_i

In IEEE Std 802.1AS-2011 13.1.4, instead of sending a future time $ToD_{X,i}$ at a future MPCP frame X, for EPoC the following future time at the future MPCP frame is substituted for $ToD_{X,i}$:

$$ToD\_EPOC\_CLT_{X,i} = ToD_{X,i} + T\_CORR\_CLT \quad (101–39)$$

(i.e., future time sent by CLT to CNU_i = 802.1AS future time + CLT correction factor)

where

$ToD\_EPOC\_CLT_{X,i}$ is the time of day at the future MPCP counter value X being sent from the CLT to CNU_i, corrected for the EPoC CLT PHY time delay asymmetry

$ToD_{X,i}$ is the future time for CNU_i at future MPCP counter value X as defined in IEEE Std 802.1AS, 13.1.4

T_CORR_CLT is 1/2 of the CLTs differential delay as defined in Equation (101–40)

$$T\_CORR\_CLT = (MaxTxDly - MaxRxDly + MinTxDly - MinRxDly)/2 \quad (101–40)$$

where

MaxTxDly is the management variable equivalent to Clause 45 registers 1.1801 and 1.1802.

MaxRxDly is the management variable equivalent to Clause 45 registers 1.1803 and 1.1804.

MinRxDly is the management variable equivalent to Clause 45 registers 1.1805 and 1.1806.

MinRxDly is the management variable equivalent to Clause 45 registers 1.1807 and 1.1808.

101.5.2 CNU PHY asymmetry correction of future time received by CNU_i

Instead of using the $ToD\_EPOC\_CLT_{X,i}$ future time for CNU_i directly, each CNU_i is to correct the future time value received from the CLT for its own CNU PHY time delay asymmetry as follows:

$$ToD\_EPOC\_CNU_{X,i} = ToD\_EPOC\_CLT_{X,i} + T\_CORR\_CNU_i \quad (101–41)$$

(i.e., CNU time = CNU_i future time sent by CLT + CNU_i correction factor)

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where

$ToD\_EPOC\_CNU_{X,i}$ is the future time to be loaded in the time of day counter of CNU_i at the future MPCP counter value X

$ToD\_EPOC\_CLT_{X,i}$ is defined above in Equation (101–39)

$T\_CORR\_CNU_i$ is 1/2 of the CNUs differential delay as given in Equation (101–42)

$$T\_CORR\_CNU = (MaxTxDly - MaxRxDly + MinTxDly - MinRxDly)/2 \quad (101–42)$$

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101.6 Protocol implementation conformance statement (PICS) proforma for Clause 101, Reconciliation Sublayer, Physical Coding Sublayer, and Physical Media Attachment for EPoC[175]

101.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 101, Reconciliation Sublayer, Physical Coding Sublayer, and Physical Media Attachment for EPoC, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

101.6.2 Identification

101.6.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

101.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 101, Reconciliation Sublayer, Physical Coding Sublayer, and Physical Media Attachment for EPoC
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[175] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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101.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
CLT	CLT Functionality	101.3	Device supports the functionality required for CLT	O	Yes [ ] No [ ] N/A [ ]
CNU	CNU Functionality	101.3	Device supports the functionality required for NCU	O	Yes [ ] No [ ] N/A [ ]

101.6.4 PICS proforma tables for Reconciliation Sublayer, Physical Coding Sublayer, and Physical Media Attachment for EPoC

101.6.4.1 General specifications

Item	Feature	Subclause	Value/Comment	Status	Support
G1	Unidirectional mode	76.2.3	Device operates in unidirectional transmission mode	CLT: M	Yes [ ] No [ ] N/A [ ]
G2	Delay variation	101.1.2	Combined delay variation through RS, PCS, and PMA sublayers is limited to 1 time_quantum	M	Yes [ ] No [ ]
G3	PMA to PCS transfer function	101.3.3.1.8	Meets the requirements of Figure 101–15	CLT: M	Yes [ ] No [ ] N/A [ ]
G4	PMA service interface	101.4.2	Support for PMA_UNITDATA.request() and PMA_UNITDATA.indication()	M	Yes [ ] No [ ]
G5	OFDM channel number	101.4.3.1	PHY declares number of downstream OFDM channels supported	M	Yes [ ] No [ ]
G6	OFDM Modulations	101.4.3.4	PHY declares optional modulations supported	M	Yes [ ] No [ ]
G7	IDFT subcarrier index range	101.4.3.11	$148 \leq k \leq 3947$	M	Yes [ ] No [ ]
G8	Time synchronization support	101.5	Methods described in 101.5.1 and 101.5.2 supported	O	Yes [ ] No [ ]

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101.6.4.2 Transmission functions

Item	Feature	Subclause	Value/Comment	Status	Support
TX1	DS Excluded Subcarriers	101.4.3.4.4	No transmissions in excluded subcarriers	CLT:M	Yes [ ] No [ ] N/A [ ]
TX2	DS Subcarriers	101.4.3.11	Comply with Equation (101–30)	CLT:M	Yes [ ] No [ ] N/A [ ]
TX3	US Excluded Subcarriers	101.4.4.4.3	No transmissions in excluded subcarriers	CNU: M	Yes [ ] No [ ] N/A [ ]
TX4	Burst Start	101.4.4.3.2	CNU Burst begins with start burst marker	CNU: M	Yes [ ] No [ ] N/A [ ]
TX5	Burst End	101.4.4.3.4	Burst ends with start end marker	CNU: M	Yes [ ] No [ ] N/A [ ]

101.6.4.3 OFDM Configuration functions

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	OFDM channel 1	101.4.3.1	OFDM channel 1 always enabled	M	Yes [ ] No [ ]
OC2	DS frame timing	101.4.4.3.6	Meets the requirements of Figure 101–31	CNU: M	Yes [ ] No [ ] N/A [ ]
OC3	DS Subcarrier configuration	101.4.3.4	Meets the requirements of Table 101–8	M	Yes [ ] No [ ]
OC4	DS CP values	101.4.3.12	As shown in Table 101–10	CLT: M	Yes [ ] No [ ] N/A [ ]
OC5	DS Windowing values	101.4.3.12	As shown in Table 101–11 and less than CP value	CLT: M	Yes [ ] No [ ] N/A [ ]
OC6	DS Profile changes ignored	101.4.2	When DS_CpyInP is a one writes to all downstream profile variables shall be ignored and switching between profiles is prohibited	CNU: M	Yes [ ] No [ ] N/A [ ]
OC7	US Superframe	101.4.4.3.1	Six symbol Probe Period followed by 256 symbols	CNU: M	Yes [ ] No [ ] N/A [ ]
OC8	US subcarrier configuration	101.4.4.4	Meets the requirements of Table 101–13	CNU: M	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
OC9	US CP size	101.4.4.10	Per Table 101–17	CNU: M	Yes [ ] No [ ] N/A [ ]
OC10	US Windowing size	101.4.4.10	Per Table 101–18	CNU: M	Yes [ ] No [ ] N/A [ ]
OC11	US Profile changes ignored	101.4.2	When US_CpyInP is a one writes to all upstream profile variables shall be ignored and switching between profiles is prohibited	CNU: M	Yes [ ] No [ ] N/A [ ]
OC12	Activation of OFDMA timing adjustments	101.4.4.2.2	OFDMA timing adjustment accurate to within ± 10 ns	CNU:M	Yes [ ] No [ ] N/A [ ]
OC13	Bit stream to constellation mapping	101.4.5	Per Figure 101–39	M	Yes [ ] No [ ]
OC14	QAM constellation scaling	101.4.5.5	Per Table 101–19	M	Yes [ ] No [ ]

101.6.4.4 OFDM Timing

Item	Feature	Subclause	Value/Comment	Status	Support
OT1	Downstream Synchronization	101.4.3.2	CLT transmitters and CNU receivers meet the requirements of Table 101–7	M	Yes [ ] No [ ]
OT2	DS OFDM Channels	101.4.3.13	Conform to requirements of Table 101–12	CLT: M	Yes [ ] No [ ] N/A [ ]
OT3	CLT synchronization	101.4.3.2	CLT OFDM Clock and RF transmissions locked to 10.24 MHz Master Clock	CLT: M	Yes [ ] No [ ] N/A [ ]
OT4	CLT Subcarrier Clock source	101.4.3.3	Synchronous with the 10.24 MHz Master Clock	CLT: M	Yes [ ] No [ ] N/A [ ]
OT5	CLT Subcarrier Clock frequency	101.4.3.3	Meets the requirements of Equation (101–6)	CLT: M	Yes [ ] No [ ] N/A [ ]
OT6	CLT phase noise	101.4.3.2	CLT meets the more stringent requirements from Table 100–4 (Phase noise) and Table 101–7 (clock jitter)	CLT: M	Yes [ ] No [ ] N/A [ ]
OT7	CNU synchronization	101.4.3.2	CNU synchronizes its 10.24 MHz Master Clock to the PHY Link frame	CNU: M	Yes [ ] No [ ] N/A [ ]
OT8	CNU Subcarrier Clock synchronization	101.4.4.2.1	CNU Subcarrier Clock and 50 kHz subcarrier frequency locked to 10.24 MHz Master Clock	CNU:M	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
OT9	CNU Subcarrier Clock frequency accuracy	101.4.4.2.1	CNU Subcarrier Clock accurate to within 0.4 ppm	CNU:M	Yes [ ] No [ ] N/A [ ]
OT10	CNU OFDM Clock timing error	101.4.4.2.3	CNU OFDM Clock timing error relative to the CLT 10.24 MHz Master Clock as measured at the CLT within ± 10 ns in each burst measured within 35 s measurement duration	CNU:M	Yes [ ] No [ ] N/A [ ]
OT11	CNU SC frequency accuracy	101.4.4.2.1	CNU subcarrier frequency accurate to within 30 Hz	CNU:M	Yes [ ] No [ ] N/A [ ]
OT12	FCP Update	101.4.3.8.4	FPC value passed with sufficient time for insertion in PHY Link frame	CLT: M	Yes [ ] No [ ] N/A [ ]

101.6.4.5 Data Detector functions

Item	Feature	Subclause	Value/Comment	Status	Support
DD1	Data Detector input process	101.3.2.5.8	Meets the requirements of Figure 101–11	M	Yes [ ] No [ ]
DD2	CLT Data Detector output process	101.3.2.5.8	Meets the requirements of Figure 101–12	CLT: M	Yes [ ] No [ ] N/A [ ]
DD3	CNU Data Detector output process	101.3.2.5.8	Meets the requirements of Figure 101–13	CNU: M	Yes [ ] No [ ] N/A [ ]

101.6.4.6 IDLE insertion and deletion functions

Item	Feature	Subclause	Value/Comment	Status	Support
IDI1	CLT Idle Deletion function implementation	101.3.2.1.5	Meets the requirements of Figure 101–6	CLT: M	Yes [ ] No [ ] N/A [ ]
IDI2	CNU Idle Deletion function implementation	101.3.2.5.8	Meets the requirements of Figure 101–7	CNU: M	Yes [ ] No [ ] N/A [ ]
IDI3	Idle Insertion	101.3.2.5.8	Meets the requirements of Figure 101–18	M	Yes [ ] No [ ]

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101.6.4.7 FEC functions

Item	Feature	Subclause	Value/Comment	Status	Support
FE1	CLT FEC Encoder	101.3.2.4	LDPC (16200, 14400)	CLT: M	Yes [ ] No [ ] N/A [ ]
FE2	CNU FEC Decoder	101.3.3	LDPC (16200, 14400)	CNU: M	Yes [ ] No [ ] N/A [ ]
FE3	CNU FEC input/output	101.3.3.1.8	CNU FEC input process meets the requirements of Figure 101–16 and CNU FEC output process meets the requirements of Figure 101–17	CNU: M	Yes [ ] No [ ] N/A [ ]
FE4	CNU FEC Encoder	101.3.2.4	LDPC (16200, 14400), LDPC (5940, 5040) and LDPC (1120, 840)	CNU: M	Yes [ ] No [ ] N/A [ ]
FE5	CLT FEC Decoder	101.3.3	LDPC (16200, 14400), LDPC (5940, 5040) and LDPC (1120, 840)	CLT: M	Yes [ ] No [ ] N/A [ ]
FE6	CRC40 Calculation	101.3.2.3	Meets the requirements of Figure 101–8	M	Yes [ ] No [ ]
FE7	CRC40 Initialization	101.3.2.3	CRC40 calculation initialized to 0x00 at the beginning of each FEC codeword	M	Yes [ ] No [ ]
FE8	Uncorrectable FEC code-word indication	101.3.3.1.4	Uncorrectable FEC codewords marker under user configuration per Table 101–6	M	Yes [ ] No [ ]

101.6.4.8 Encoding functions

Item	Feature	Subclause	Value/Comment	Status	Support
EN1	CLT Scrambler	101.4.3.7	Downstream data scrambler meets the requirement of Figure 101–21	CLT: M	Yes [ ] No [ ] N/A [ ]
EN2	CLT scrambler initialization	101.4.3.7	at the first codeword of the downstream frame	CLT:M	Yes [ ] No [ ] N/A [ ]
EN3	CNU scrambler initialization	101.4.3.7	at the beginning of each grant	CNU:M	Yes [ ] No [ ] N/A [ ]
EN4	CLT Symbol Mapping	101.4.3.8.3	Symbol mapper processes all active subcarriers	CLT: M	Yes [ ] No [ ] N/A [ ]
EN5	CLT Time Interleaving	101.4.3.9.2	Time interleaving as described in 101.4.3.9.2	CLT: M	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
EN6	CLT Time Interleaving depth	101.4.3.9.2	Between 1 and 32 inclusive	CLT: M	Yes [ ] No [ ] N/A [ ]
EN7	CLT Frequency Interleaving	101.4.3.9.3	Frequency interleaving meets the requirements of 101.4.3.9.3	CLT: M	Yes [ ] No [ ] N/A [ ]
EN8	CNU Symbol mapper Idle function	101.4.4.5.3	Meets the requirements of Figure 101–32	CNU: M	Yes [ ] No [ ] N/A [ ]
EN9	CNU Symbol mapper fill function	101.4.4.5.3	Meets the requirements of Figure 101–33	CNU: M	Yes [ ] No [ ] N/A [ ]

101.6.4.9 Pilots

Item	Feature	Subclause	Value/Comment	Status	Support
PI1	Scattered pilot definition	101.4.3.6.1	Defined per101.4.3.6	CLT: M	Yes [ ] No [ ] N/A [ ]
PI2	Continuous Pilot placement	101.4.3.6.4	Meets the Equation (101–9) and the eight steps given in 101.4.3.6.4	CLT: M	Yes [ ] No [ ] N/A [ ]
PI3	PHY Link Continous Pilots	101.4.3.6.3	Four pairs placed symmetrically about the PHY Link as in Figure 102–7 and Table 101–9	CLT: M	Yes [ ] No [ ] N/A [ ]
PI4	Pilot modulation	101.4.3.10	BPSK using pseudo-random generator shown in Figure 101–28	CLT: M	Yes [ ] No [ ] N/A [ ]
PI5	Pilot boosting	101.4.3.10.1	Amplitude of pilots is 2 times the RMS value of the amplitude of other subcarriers	CLT: M	Yes [ ] No [ ] N/A [ ]
PI6	US Pilot Insertion	101.4.4.7.2	Meets the requirements of 101.4.4.7.2	CNU: M	Yes [ ] No [ ] N/A [ ]

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101.6.4.10 Equalization

Item	Feature	Subclause	Value/Comment	Status	Support
EQ1	Equalized subcarriers	101.4.4.9.1	All data transmissions except Probe and PHY Discovery Response. Probe equalization under control of PHY Link	CNU: M	Yes [ ] No [ ] N/A [ ]
EQ2	US Subcarrier equalization	101.4.4.9.1	Single complex coefficient per subcarrier updated by the PHY Link	CNU: M	Yes [ ] No [ ] N/A [ ]
EQ3	US Subcarrier equalization default	101.4.4.9.1	Default value of 1+j0	CNU: M	Yes [ ] No [ ] N/A [ ]
EQ4	Equalizer coefficient normalization	101.4.4.9.1	Adjusting the mean of (abs $(Ck)^2$) to be 1	CNU: M	Yes [ ] No [ ] N/A [ ]
EQ5	Equalizer coefficient activation time	101.4.4.9.1	Within 10 ms of receipt at the beginning of a transmission	CNU: M	Yes [ ] No [ ] N/A [ ]

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102. EPoC PHY Link

102.1 PHY Link overview and architecture

The PHY Link is a low level communications link used between the CLT PHY and its subordinated CNU PHYs. It is used to communicate PHY OFDM channel parameters and to negotiate initialization of CNUs that wish to join the EPoC network. A small amount of RF spectrum is dedicated to the PHY Link at network setup time for both the upstream (US) and the downstream (DS) directions (see 102.2.1 and 102.3.1). In a multi-OFDM channel PHY, only OFDM channel one has a PHY Link (see Figure 102–1 and Figure 102–3). The PHY Link uses a straightforward query response protocol with broadcast capability to transfer information in variables between the CLT and its subordinated CNUs and vice versa. Both the upstream and the downstream PHY Link include a frame structure. Each PHY Link frame is composed of message blocks containing timing, control information, status information, PHY Instructions, or PHY Responses. The frame is padded to achieve a fixed bit length and encoded in multiple FEC codewords.

The upstream superframe (see 101.4.4.3.1) begins with the Probe Period. CNU PHY Discovery Responses and probing are performed during the Probe Period. The PHY Discovery Response is used for initial CNU bring up and is fully described in 102.4.1.4. Probing is used to perform fine ranging and periodic link maintenance tasks and is described in 102.4.2.

102.1.1 PHY Link frame structure and protocol

The PHY Link frame is illustrated in Figure 102–1 and Figure 102–2.

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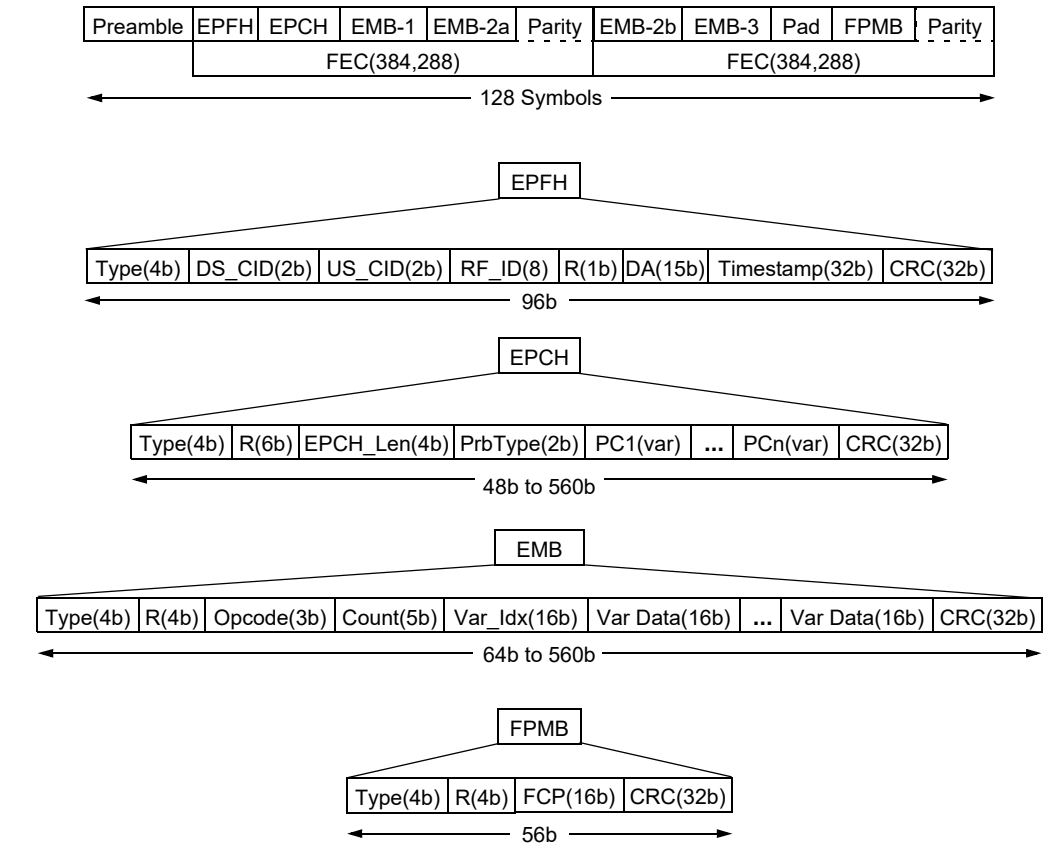
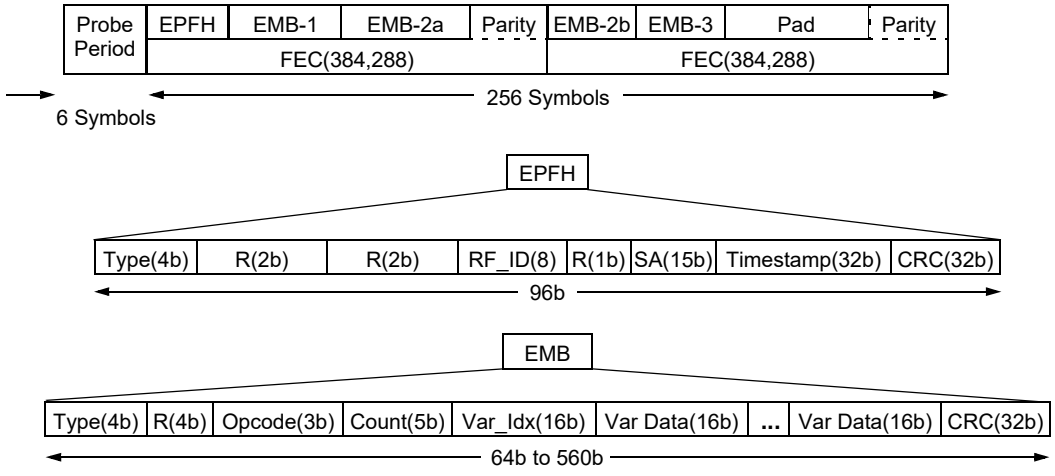


NOTE—The notation "(#b)" indicates the number of bits in the field.

Figure 102–1—Downstream PHY Link frame



NOTE—The notation "(#b)" indicates the number of bits in the field.

Figure 102–2—Upstream PHY Link frame

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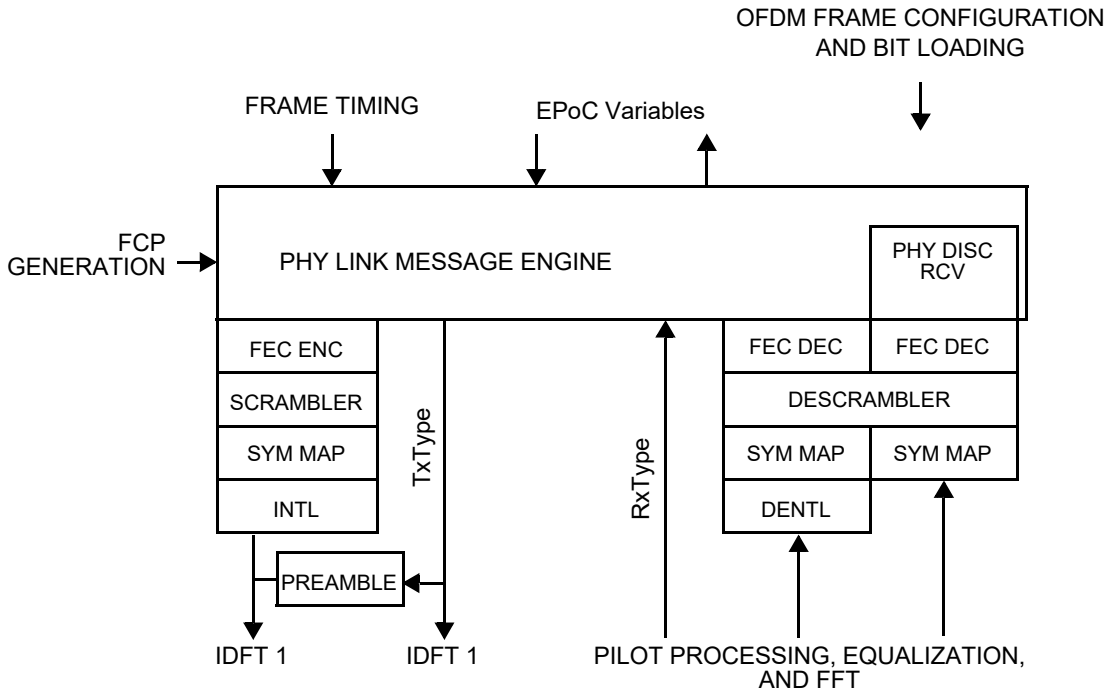
The PHY Link protocol is a query and response protocol where the CLT transmits one or more instructions enclosed in EPoC Message Blocks to a CNU or group of CNUs. Each instruction can perform a read, write or write/verify operation. Read and write/verify instructions cannot be addressed to a group of CNUs. The PHY Link frame length shall be fixed; the downstream length is 128 OFDM symbols long and the upstream length is 262 OFDM symbols long.

The CLT and the CNU shall support both an upstream and a downstream PHY Link channel.

102.1.2 PHY Link block diagram

The architecture of the PHY Link data path is illustrated in Figure 102–3 and Figure 102–4. The relationship between the PHY Link functional blocks and the rest of the 10GPASS-XR PHY is illustrated in Figure 101–1 and Figure 101–2.



KEY
DEINTL = DE-INTERLEAVER
FEC DEC = FEC DECODER
FEC ENC = FEC ENCODER
INTL = INTERLEAVER
PCS = PHYSICAL CODING SUBLAYER
PHY DISC = PHY DISCOVERY
PHY DISC RCV = PHY DISCOVERY RECEIVE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
PROBE RCV = PROBE RECEIVE
SYM MAP = SYMBOL MAPPER

Figure 102–3—PHY Link CLT architecture

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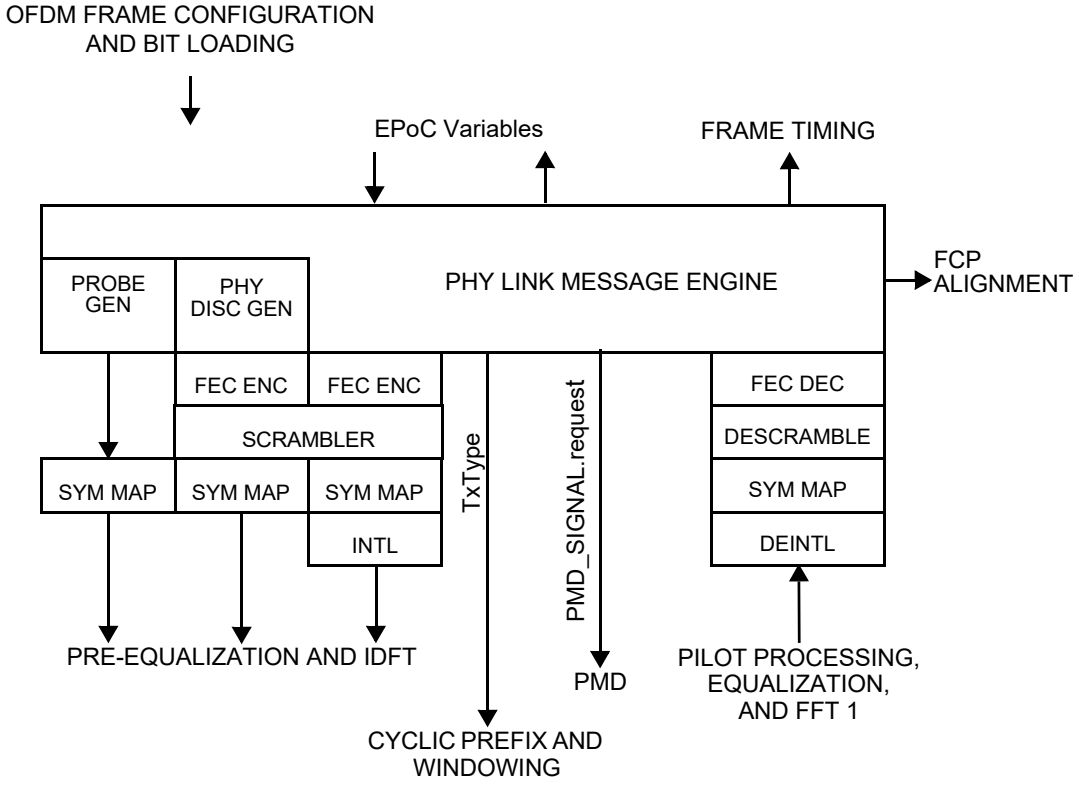

KEY
DEINTL = DE-INTERLEAVER
FEC DEC = FEC DECODER
FEC ENC = FEC ENCODER
INTL = INTERLEAVER
PCS = PHYSICAL CODING SUBLAYER
PHY DISC GEN = PHY DISCOVERY GENERATOR
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
PROBE GEN = PROBE GENERATOR
SYM MAP = SYMBOL MAPPER

Figure 102–4—PHY Link CNU architecture

102.1.3 PHY Link Message Engine

The PHY Link Message Engine block is responsible for the origination and termination of all messages passed over the PHY Link, as well as PHY to PHY signaling. In the downstream direction there are four message blocks—the EPoC PHY Frame Header (EPFH), the EPoC Probe Control Header (EPCH), the EPoC message block, and the FEC Parity message block. The upstream PHY Link Message Engine also has the two additional PHY to PHY signaling types—PHY Discovery Response and Probing.

The content of each message block is detailed in the following subclauses as is the characteristic of the two additional PHY signaling types. The details of the PHY Message Engine behavior is described in 102.2.3 and 102.3.2.

Once a PHY Link message block has been created the stream of bytes is converted into a stream of bits, MSB first.

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102.1.4 PHY Link FEC encoder

The PHY Link uses several LDPC FEC encoders. These encoders are derived from mother encoders using either puncturing only or both shortening and puncturing. A general description of LDPC codes is given in 101.3.2.4.

102.1.4.1 LDPC (480, 288) mother code

The base matrix of a parity check matrix for the (480,288) mother code is listed in Table 102–1, where the submatrix size (lifting factor) is $L = 48$ (see 101.3.2.4 for the general definition of a base matrix).

Table 102–1—Base matrix of (480,288) LDPC code parity check matrix

Columns	Rows									
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
1	16	1	28	9	40	38	16	—	—	—
2	28	42	36	11	39	9	8	38	—	—
3	5	2	18	16	25	47	—	2	19	—
4	18	18	40	18	0	34	—	—	7	32

102.1.4.2 LDPC (160, 80) mother code

The base matrix of a parity check matrix for the (160,80) mother code is listed in Table 102–2, where the submatrix size (lifting factor) is $L = 16$ (see 101.3.2.4 for the general definition of a base matrix).

Table 102–2—Base matrix for (160, 80) DPC code parity check matrix

Columns	Rows									
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
1	1	11	10	12	7	9	—	—	—	—
2	2	1	14	15	14	14	12	—	—	—
3	0	9	3	2	—	—	11	7	—	—
4	6	8	—	10	3	—	—	10	4	—
5	12	13	11	—	0	—	—	—	5	2

102.1.4.3 Shortening and puncturing encoders

Shortening encoder operationally includes the following three steps:

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a) Pad zero bits to the payload bits to fit for the codeword size of the mother code, the entire bits are called mother code information bits and the coordinates corresponded to the padded zeros are called shortening coordinates.
b) Encode the information bits obtained in step a) using mother code encoder.
c) Delete the shortening coordinates: i.e., all the padded zero bits in step a).

Puncturing encoder operationally includes the following two steps:

1) Encode the payload (with or without padding) bits using mother encoder.
2) Delete the puncturing coordinates of encoded codeword of step 1), where the puncturing coordinates are given coordinates of the mother code codeword.

102.1.4.3.1 LDPC (384, 288) puncturing encoder

The LDPC (384, 288) encoder is operated on the (480, 288) LDPC mother code encoder with the puncturing.

The mother code is defined in 102.1.4.1. The puncturing operation is as follows (also see Figure 102–5):

1) Denote the information bits sent to the mother code encoder by ($a_0, \ldots, a_{287}$)
2) Let the encoding output be ($a_0, \ldots, a_{287}, b_{288}, \ldots, b_{479}$), where ($b_{288}, \ldots, b_{479}$) are parity-check bits. The coordinates to be deleted by the puncturing step are as follows:
   — Period 1: 48 consecutive coordinates $a_{48}, \ldots, a_{95}$
   — Period 2: 48 consecutive coordinates $b_{384}, \ldots, b_{431}$

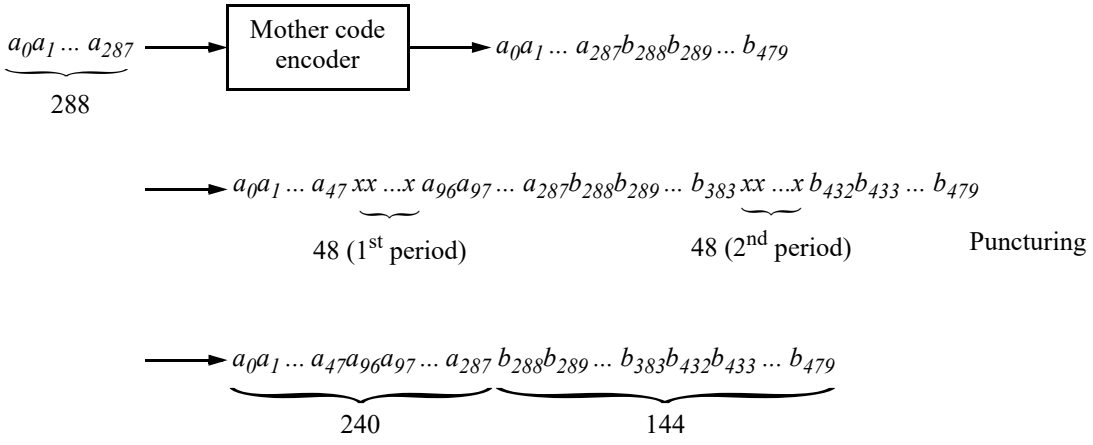

Figure 102–5—Puncturing encoder for LDPC (384,288) FEC

102.1.4.3.2 LDPC (128, 80) puncturing encoder

The LDPC (128, 80) encoder is operated on the (160, 80) LDPC mother code encoder with the puncturing.

The mother code is defined in 102.1.4.2.

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The puncturing operation is as follows (also see Figure 102–6):

Denote the information bits sent to the mother code encoder by (a_0, ... , a_{79}) and let the encoding output be (a_0, ... , a_{79}, b_{80}, ... , b_{159}), where (b_{80}, ... , b_{159}) are parity-check bits. Then do puncturing on the puncturing coordinates given by the following:

— Period 1: 16 consecutive coordinates a_0, ... , a_{15}
— Period 2: 16 consecutive coordinates b_{144}, ... , b_{159}

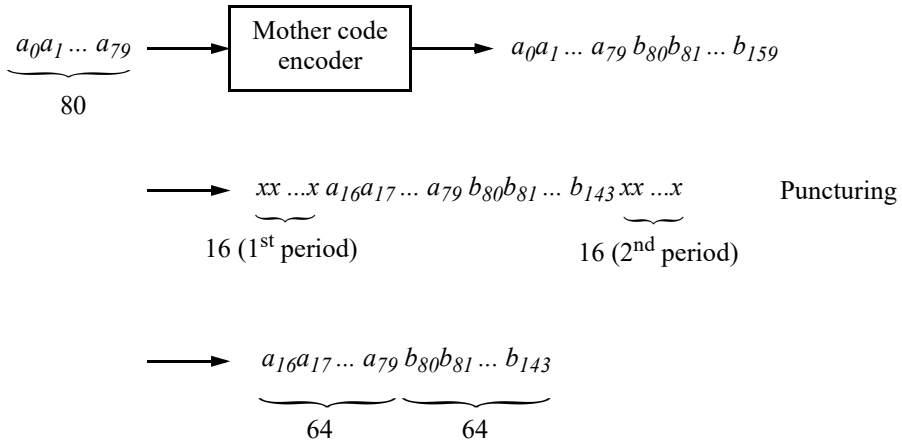

Figure 102–6—Puncturing encoder for the LDPC (128, 80) FEC

102.1.5 PHY Link scrambler

The CLT and CNU shall scramble the output of the PHY Link FEC encoding process using a linear feedback shift register mechanism as illustrated in Figure 101–21.

The scrambler is defined by the following polynomial:

$$x^{23} + x^{18} + 1$$

The scrambler is initialized to the hexadecimal value of 0x4732BA. The CLT shall initialize the scrambler with the hexadecimal value at the beginning of the first OFDM symbol following the PHY Link preamble in the downstream direction. In the upstream direction, the CNU shall initialize the scrambler at the beginning of an upstream PHY Link transmission.

The PHY shall not scramble the PHY Link preamble.

102.1.6 PHY Link symbol map and constellation mapping

The PHY maps the scrambled bit stream of normal PHY Link data into a complex number using the assigned modulation order. In the downstream direction, the assigned modulation order shall be 16-QAM and uses the mapping shown in 101.4.5. The upstream PHY Link shall be 16-QAM or a higher order modulation (see 101.4.5 for mapping structure). The PHY multiplies the real and imaginary parts by the appropriate factor in Table 101–19 to ensure that mean-square value of the QAM constellation is unity.

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102.1.7 Interleaving

Data in the PHY Link channel is time interleaved. For the downstream direction this time interleaving is described in 102.2.1.3.

Transmissions in the upstream direction for PHY Discovery Response are not time interleaved.

Control for the interleaving process is conveyed using the TxType in the CNU (see Figure 102–4) and RxType in the CLT (see Figure 102–3).

102.1.8 Mapping of PHY Link variables

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PHY Link or are communicated between CLT and CNU via the PHY Link. Mapping of MDIO control and status variables to PHY Link variables is shown in Table 102–3. The least significant bit in each variable is mapped to the lowest numbered bit in the lowest numbered register for Clause 45 registers. These variables are used by the PHY Link for PHY management.

NOTE—Most of the variables transferred via the PHY Link are reflected in Clause 45. The EPoC Index and bits are determined from Clause 45 register designations using the following rules:
If 1.1900 ≤ RegAdd ≤1.1999, then Index = (RegAdd – 1.1900) × 1000 (i.e., 0 to 99).
If 12.0000 ≤ RegAdd, then Index = (RegAdd – 12.0000) × 1000 + 1000 (i.e., 1000 +).
If variable is not in Clause 45, indexes between 500 and 999 are used and are given in the variable definition.

Table 102–3—MDIO register to PHY variable mapping

MDIO parameter name	MDIO register name	Register / bit number	PHY variable		
			Name	Index	Bit(s)
Link up ready	10GPASS-XR control and status	1.1900:10	*LinkUpRdy*	0	10
PHY Discovery complete	10GPASS-XR control and status	1.1900.1	*PhyDiscCmplt*	0	1
PHY Discovery enable	10GPASS-XR control and status	1.1900.0	*PD_Enable*	0	0
DS windowing	DS OFDM control	1.1901.6:4	*DSNrp*	1	6:4
DS cyclic prefix	DS OFDM control	1.1901.3:0	*DSNcp*	1	3:0
DS OFDM freq ch 1	DS OFDM channel frequency control 1	1.1902.15:0	*DS_FreqCh(1)*	2	15:0
DS OFDM freq ch 2	DS OFDM channel frequency control 1	1.1903.15:0	*DS_FreqCh(2)*	3	15:0
DS OFDM freq ch 3	DS OFDM channel frequency control 3	1.1904.15:0	*DS_FreqCh(3)*	4	15:0
DS OFDM freq ch 4	DS OFDM channel frequency control 4	1.1905.15:0	*DS_FreqCh(4)*	5	15:0
DS OFDM freq ch 5	DS OFDM channel frequency control 5	1.1906.15:0	*DS_FreqCh(5)*	6	15:0
Random seed	US OFDM control	1.1907.15:8	*Rnd*	7	15:8
Resource Block size	US OFDM control	1.1907.7	*RBsize*	7	7

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Table 102–3—MDIO register to PHY variable mapping *(continued)*

MDIO parameter name	MDIO register name	Register / bit number	PHY variable		
			Name	Index	Bit(s)
US windowing	US OFDM control	1.1907.6:4	*USNrp*	7	6:4
US cyclic prefix	US OFDM control	1.1907.3:0	*USNcp*	7	3:0
US OFDM freq	US OFDM channel frequency control	1.1908.15:0	*US_FreqCh1*	8	15:0
US copy in process	Profile control	1.1910.11	*US_CpyInP*	10	11
US profile copy	Profile control	1.1910.10	*US_PrflCpy*	10	10
US configuration ID	Profile control	1.1910.9:8	*US_CID*	10	9:8
DS copy channel ID	Profile control	1.1910.6:4	*DS_CpyCh*	10	6:4
DS copy in process	Profile control	1.1910.3	*DS_CpyInP*	10	3
DS profile copy	Profile control	1.1910.2	*DS_PrflCpy*	10	2
DS configuration ID	Profile control	1.1910.1:0	*DS_CID*	10	1:0
DS PHY Link start	DS PHY Link control	1.1911.11:0	*DS_PhyLinkStrt*	11	11:0
US PHY Link modulation	US PHY Link control	1.1912.15:12	*US_PhyLinkMod*	12	15:12
US PHY Link start	US PHY Link control	1.1912.11:0	*US_PhyLinkStrt*	12	11:0
PHY Discovery start lower	PHY Discovery control	1.1913.15:0	*DiscStrt*(15:0)	13	15:0
PHY Discovery start upper	PHY Discovery control	1.1914.15:0	*DiscStrt*(31:16)	14	15:0
CNU_ID assigned flag	New CNU control	1.1915.15	*AssgndCNU_ID*	15	15
Allowed CNU_ID	New CNU control	1.1915.14:0	*AllwdCNU_ID*	15	14:0
New CNU range	New CNU info	1.1916.15:0	*NewCNU_Rng*	16	15:0
New CNU MAC 0	New CNU info	1.1917.15:0	*New_MAC* (15:0)	17	15:0
New CNU MAC 1	New CNU info	1.1918.15:0	*New_MAC* (31:16)	18	15:0
New CNU MAC 2	New CNU info	1.1919.15:0	*New_MAC* (47:32)	19	15:0
PMA/PMD timing offset lower	PMA/PMD timing offset	1.1922.15:0	*PhyTimingOffset* (15:0)	22	15:0
PMA/PMD timing offset upper	PMA/PMD timing offset	1.1923.15:0	*PhyTimingOffset* (31:16)	23	15:0
PMA/PMD power offset	PMA/PMD power offset	1.1924.7:0	*PHYPowerOffset*	24	7:0
PMA/PMD ranging offset lower	PMA/PMD ranging offset	1.1925.15:0	*PhyRngOffset* (15:0)	25	15:0
PMA/PMD ranging offset upper	PMA/PMD ranging offset	1.1926.15:0	*PhyRngOffset* (31:16)	26	15:0

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Table 102–3—MDIO register to PHY variable mapping *(continued)*

MDIO parameter name	MDIO register name	Register / bit number	PHY variable		
			Name	Index	Bit(s)
DS PMA/PMD data rate lower	DS PMA/PMD data rate	1.1927.15:3	*DS_DataRate (15:3)*	27	15:3
DS PMA/PMD data rate fractional	DS PMA/PMD data rate	1.1927.2:0	*DS_DataRate (2:0)*	27	2:0
DS PMA/PMD data rate mid	DS PMA/PMD data rate	1.1928.15:0	*DS_DataRate (31:16)*	28	15:0
DS PMA/PMD data rate upper	DS PMA/PMD data rate	1.1929.4:0	*DS_DataRate (36:32)*	29	4:0
US PMA/PMD data rate lower	US PMA/PMD data rate	1.1930.15:3	*US_DataRate (15:3)*	30	15:3
US PMA/PMD data rate fractional	US PMA/PMD data rate	1.1930.2:0	*US_DataRate (2:0)*	30	2:0
US PMA/PMD data rate mid	US PMA/PMD data rate	1.1931.15:0	*US_DataRate (31:16)*	31	15:0
US PMA/PMD data rate upper	US PMA/PMD data rate	1.1932.4:0	*US_DataRate (36:32)*	32	4:0
PHY Link EPFH counter	PHY Link EPFH counter	1.1939.15:0	*EPFHcnt*	39	15:0
PHY Link EPFH error counter	PHY Link EPFH error counter	1.1940.15:0	*EPFHerr*	40	15:0
PHY Link EPCH counter	PHY Link EPCH counter	1.1941.15:0	*EPCHcnt*	41	15:0
PHY Link EPCH error counter	PHY Link EPCH error counter	1.1942.15:0	*EPCHerr*	42	15:0
PHY Link EMB counter	PHY Link EMB counter	1.1943.15:0	*EMBcnt*	43	15:0
PHY Link EMB error counter	PHY Link EMB error counter	1.1944.15:0	*EMBerr*	44	15:0
PHY Link FPMB counter	PHY Link FPMB counter	1.1945.15:0	*FPMBcnt*	45	15:0
PHY Link FPMB error counter	PHY Link FPMB error counter	1.1946.15:0	*FPMBerr*	46	15:0
US PHY Link response time	US PHY Link response time	1.1947.15:0	*PhyLinkRspTm*	47	15:0
PHY Discovery Response power step	PHY Discovery Response power control	1949.15:8	*PdRespPwrStep*	51	15:8
PHY Discover Response initial power	PHY Discovery Response power control	1949.7:0	*PdRespInitPwr*	51	7:0
DS OFDM channel ID	10GPASS-XR DS OFDM channel ID	12.0.2:0	*DS_OFDM_ID*	1000	2:0

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Table 102–3—MDIO register to PHY variable mapping *(continued)*

MDIO parameter name	MDIO register name	Register / bit number	PHY variable		
			Name	Index	Bit(s)
DS modulation type SC7	10GPASS-XR DS profile descriptor control 1	12.1.15:12	*DS_ModTypeSC(7)*	1001	15:12
DS modulation type SC6	10GPASS-XR DS profile descriptor control 1	12.1.11:8	*DS_ModTypeSC(6)*	1001	11:8
DS modulation type SC5	10GPASS-XR DS profile descriptor control 1	12.1.7:4	*DS_ModTypeSC(5)*	1001	7:4
DS modulation type SC4	10GPASS-XR DS profile descriptor control 1	12.1.3:0	*DS_ModTypeSC(4)*	1001	3:0
DS modulation type SC8 through DS modulation type SC4095	10GPASS-XR DS profile descriptor control 2 through 10GPASS-XR DS profile descriptor control 1023	12.2 through 12.1023	*DS_ModTypeSC(8)* through *DS_ModTypeSC(4095)*	1002 through 2023	as in index 1001
US modulation type SC0	10GPASS-XR US profile descriptor control 0	12.1024.3:0	*US_ModTypeSC(0)*	2024	3:0
US modulation type SC1	10GPASS-XR US profile descriptor control 0	12.1024.7:4	*US_ModTypeSC(1)*	2024	7:4
US modulation type SC2	10GPASS-XR US profile descriptor control 0	12.1024.11:8	*US_ModTypeSC(2)*	2024	11:8
US modulation type SC3	10GPASS-XR US profile descriptor control 0	12.1024.15:12	*US_ModTypeSC(3)*	2024	15:12
US modulation type SC4 through US modulation type SC4095	10GPASS-XR US profile descriptor control 1 through 10GPASS-XR US profile descriptor control 1023	12.1025 through 12.2047	*US_ModTypeSC(4)* through *US_ModTypeSC(4095)*	2025 to 3047	
Real pre-equalizer coefficient SC0	10GPASS-XR US pre-equalizer coefficients 0	12.2048.15:0	*EQ_CoefR(0)*	3048	15:0
Imaginary pre-equalizer coefficient SC0	10GPASS-XR US pre-equalizer coefficients 0	12.2049.15:0	*EQ_CoefI(0)*	3049	15:0

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Table 102–3—MDIO register to PHY variable mapping *(continued)*

MDIO parameter name	MDIO register name	Register / bit number	PHY variable		
			Name	Index	Bit(s)
Real pre-equalizer coefficient SC1 through Real pre-equalizer coefficient SC4095	10GPASS-XR US pre-equalizer coefficients 1 through 10GPASS-XR US pre-equalizer coefficients 4095	12.2050 12.2052 ... 12.10238	*EQ_CoefR(1)* through *EQ_CoefR(4095)*	3050 3052 ... 11238	15:0
Imaginary pre-equalizer coefficient SC1 through Imaginary pre-equalizer coefficient SC4095	10GPASS-XR US pre-equalizer coefficients 1 through 10GPASS-XR US pre-equalizer coefficients 4095	12.2051 12.2053 ... 12.10239	*EQ_CoefI(1)* through *EQ_CoefI(4095)*	3051 3053 ... 11239	15:0

102.2 Downstream PHY Link

102.2.1 Downstream PHY Link Physical Layer

102.2.1.1 Resource allocation

During network setup the downstream PHY Link shall be allocated 400 kHz of spectrum. The allocated spectrum for the downstream PHY Link shall reside anywhere within a 24 MHz contiguous OFDM channel spectrum (i.e., 24 MHz with no internal exclusion bands) and have at least 3 MHz of contiguous spectrum above and below it for a total band of 6 MHz. This PHY Link band also includes eight pilot tone subcarriers placed symmetrically above and below the information subcarriers as illustrated in Figure 102–7; see 101.4.3.6.3 for exact placement of pilots. No additional continuous pilots are allowed within this 6 MHz band (see 101.4.3.6). However, scattered pilots are allowed in this spectrum in subcarriers that normally carry MAC data. The downstream PHY Link is located per the *DS_PhyLinkStrt* variable (see 102.2.6) that determines the lowest frequency subcarrier of the PHY Link. The downstream PHY Link shall use the same OFDM Symbol definition (cyclic prefix duration and windowing size) as the downstream MAC data OFDM channel.

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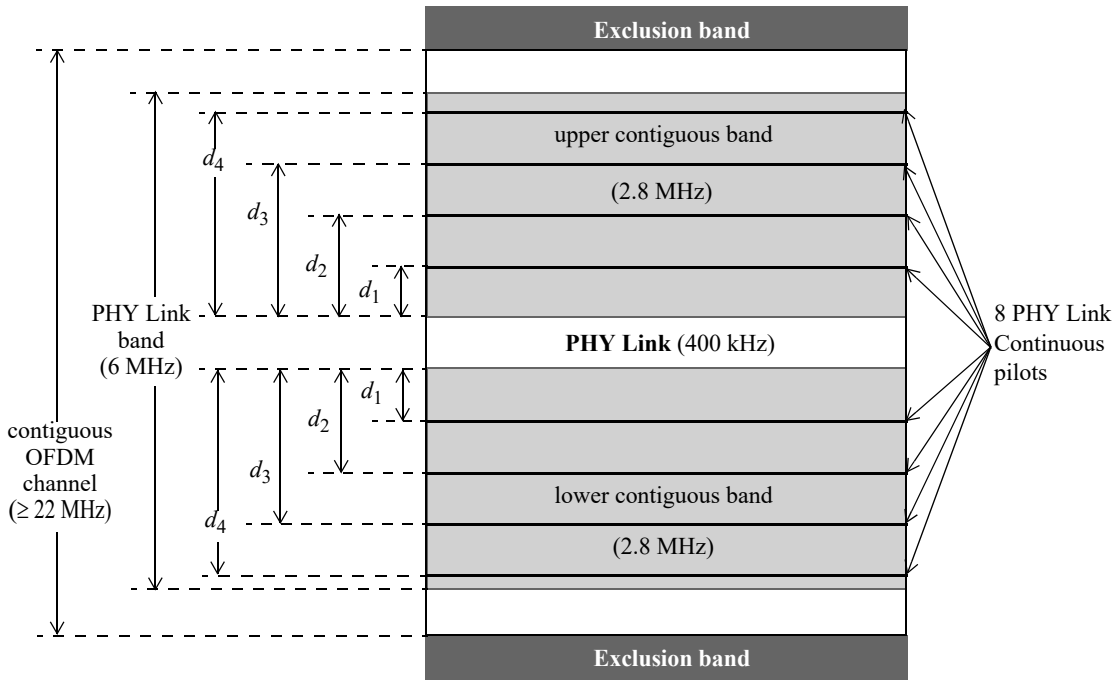

Figure 102–7—Downstream PHY Link spectrum placement

102.2.1.2 Downstream PHY Link modulation

The downstream PHY Link uses a 16-QAM constellation for all information subcarriers as specified under PHY Link CLT Tx/CNU Rx in Table 100–2.

102.2.1.3 Downstream PHY Link subcarrier block interleaving

Figure 102–5 shows 288 data bits entering the LDPC Encoder and 384 encoded bits exiting it. This sequence is in effect time-reverse ordered. The time-ordered sequence takes the form shown in Figure 102–8. The PHY shall map the 384 FEC encoded data bits, as processed by the scrambler, to 96 4-bit nibbles $\{u_i, i=0, 1, \ldots, 95\}$ as shown in Figure 102–8.

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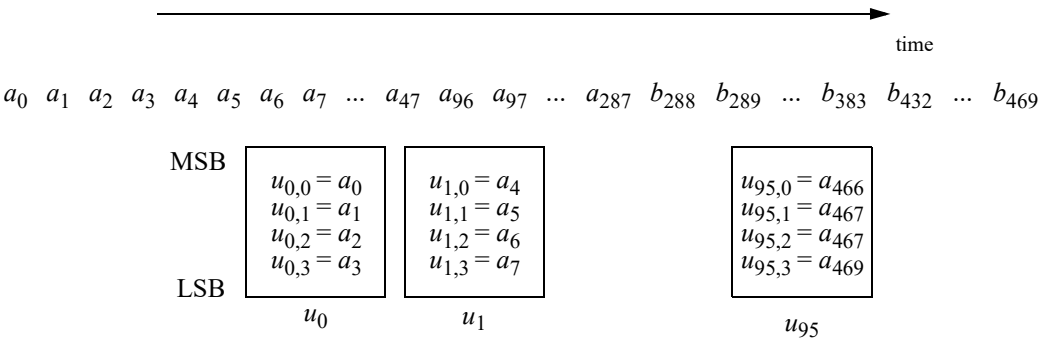

Figure 102–8—Downstream PHY Link mapping of FEC output to stream nibbles

The resulting 4-bit nibbles from this mapping operation are then time interleaved. The PHY shall interleave the 96-nibble sequence $\{u_0\ u_1\ u_2 \ldots\ u_{95}\}$ as illustrated in Figure 102–9.

Conceptually, the PHY uses an 8×2 array to perform interleaving. The PHY writes the values u_i along the rows of this two-dimensional array, as shown in Figure 102–9. The PHY reads this two-dimensional array along vertical columns to form the two-dimensional sequence $\{v_{t,f},\ t = 0,1,\ldots,11$ and $f = 0,1,\ldots,7\}$. This operation is mathematically represented as follows:

$$v_{t,f} = u_{t+12f} \tag{102–1}$$

The PHY maps each of the 8-point sequences given in Equation (102–2) to the eight successive PHY Link subcarriers of an OFDM symbol after scrambling as described in the 102.1.5.

$$V_t = \{v_{t,f}, f = 0,1,\ldots,7\} \text{ for 12 successive OFDM symbols } t = 0, 1, \ldots, 11 \tag{102–2}$$

Therefore, each FEC codeword will occupy the PHY Link segment of twelve successive OFDM symbols. There will be ten such codewords in a 128-symbol PHY Link frame, including the 8-symbol preamble.

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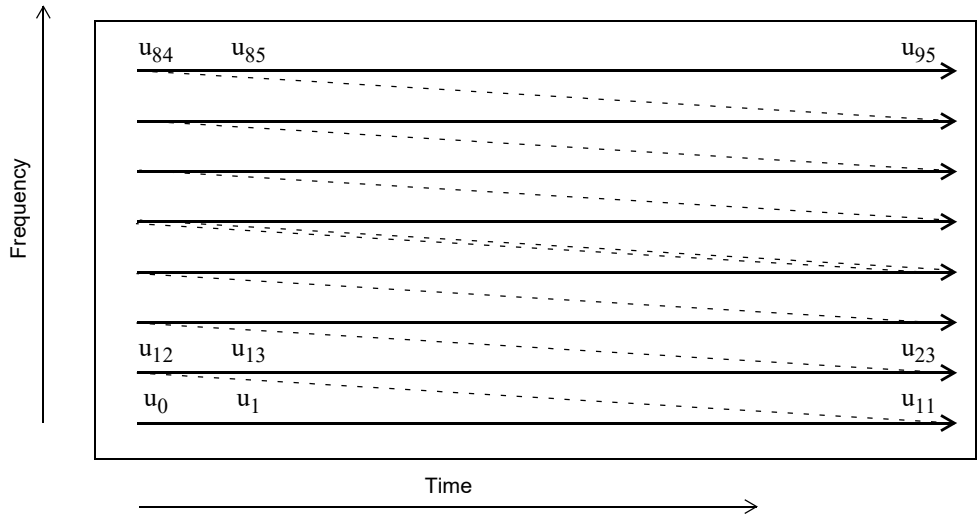

Figure 102–9—Downstream PHY Link subcarrier block interleaving

The PHY Link is time interleaved separately from the MAC data OFDM channel. The PHY Link preamble is not time interleaved.

102.2.2 Downstream preamble

The downstream Preamble shall be a fixed pattern of 64 bits as illustrated in Table 102–4, modulated using binary phase-shift keying (BPSK), that fill the first eight symbols of the PHY Link frame. The pattern is selected to enable the CNU to easily ascertain the PHY Link subcarriers without prior knowledge of the PHY Link's precise location in the RF spectrum range of an EPoC network. Detection of the PHY Link is the first action a CNU takes to join an EPoC network.

The CLT maps each of the binary bits shown in Table 102–4 to a BPSK constellation point in the complex plane using the following transformation:

$0 \rightarrow (1 + j0)$
$1 \rightarrow (-1 + j0)$

Table 102–5 is provided for information purposes and illustrates the receiver processing of the PHY Link preamble.

Table 102–4—Downstream PHY Link 2D preamble

Subcarrier	Symbol							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
8	1	0	1	0	0	0	1	1
7	1	0	1	0	0	0	1	1

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Table 102–4—Downstream PHY Link 2D preamble *(continued)*

Subcarrier	Symbol							
	1	2	3	4	5	6	7	8
6	1	0	1	0	0	0	1	1
5	0	0	0	0	1	0	0	1
4	1	0	1	0	0	0	1	1
3	0	0	0	0	1	0	0	1
2	0	0	0	0	1	0	0	1
1	1	0	1	0	0	0	1	1

Table 102–5—Downstream PHY Link differential demodulation sequence

Subcarrier	Symbol							
	1	2	3	4	5	6	7	8
8	X	1	1	1	0	0	1	0
7	X	1	1	1	0	0	1	0
6	X	1	1	1	0	0	1	0
5	X	0	0	0	1	1	0	1
4	X	1	1	1	0	0	1	0
3	X	0	0	0	1	1	0	1
2	X	0	0	0	1	1	0	1
1	X	1	1	1	0	0	1	0

102.2.3 Downstream frame

The downstream PHY Link uses a frame format, illustrated in Figure 102–1, to which the 128 symbol staggered pilot pattern is aligned with as described in 101.4.3.6. The 128 symbol downstream PHY Link frame is composed of a Preamble (see 102.2.2), one 96-bit EPoC PHY Frame Header (EPFH), one variable length EPoC Probe Control Header (EPCH), some number of variable length EPoC message blocks (EMB), one 56-bit FEC Parity message block (FPMB), and padding. The message blocks within the frame are protected with an FEC mechanism. Each message block and its included fields is described next. The number of optional EPoC message blocks contained within the frame is limited only by the frame size.

Each message block contains a Type field used to identify the contents of the block. CLTs shall use the appropriate message Type fields listed in Table 102–6 in each message block. The contents of the each message block is protected by a CRC32. See 3.2.9 for a description of how this field is calculated. The CNU

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shall calculate a CRC32 on the data fields within each message block received and, if the calculated CRC32 does not match the received CRC32 discard the message and take no action based on it.

Table 102–6—PHY Link message block Type values

Type value	Message block
0x00 to 0x08	Reserved
0x09	EPoC PHY Frame Header
0x0A	EPoC Probe Control Header
0x0B	EPoC message block
0x0C	FEC Parity message block
0x0D to 0x0F	Reserved

102.2.3.1 Downstream EPoC PHY Frame Header

The downstream EPoC PHY Frame Header includes a Type field, the Configuration ID fields (*DS_CID* and *US_CID*), the Return Frame ID field (*RF_ID*), the PHY Link DA field, the PHY Timestamp field, and a CRC32 as illustrated in Figure 102–1.

102.2.3.1.1 Configuration ID and profile activation

The Configuration ID fields are 2-bit fields used to inform a CNU to switch from one modulation profile to another. There is one field for control of the downstream profile (*DS_CID*) and one field for the upstream profile (*US_CID*). Each CNU contains two profiles in each direction, copy "A" and copy "B"; only one of which is active at any given time. The CLT shall set an identical inactive profile in all CNUs prior to its activation. The CLT updates the unused profile then, using the PHY Configuration ID field, switches the CNU to the updated profile. Once the CLT begins the switchover, as indicated by Configuration ID field values 0b01 or 0b10 it shall complete the switchover. During a switchover the value of the Configuration ID field is either incremented or decremented by one in each successive frame. The switchover is completed and the CNU activates the new profile when the Configuration ID field reaches a value of 0b00 or 0b11; thus a switchover takes three PHY Link frame times. Table 102–7 summarizes the use and meaning of the PHY Configuration ID bits and their operation is illustrated in Figure 102–10.

102.2.3.1.2 Response Frame ID

In the downstream direction, the new profile is activated at the first symbol (i.e., the symbol containing the PHY Link Preamble) in the next PHY Link frame. In the upstream direction, the new profile is activated in the first symbol of the Probe Period following the frame identified by the Return Frame ID field.

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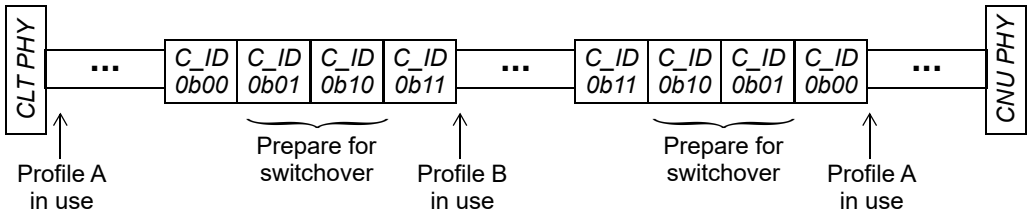
Table 102–7—Configuration ID bits

PHY Configuration ID		Meaning
bit 1	bit 0	
0	0	Copy “A” in use
0	1	Prepare for switchover
1	0	
1	1	Copy “B” in use



C_ID = Configuration ID

Figure 102–10—Configuration ID bit usage

The Response Frame ID field is an 8-bit field that indicates to the receiving CNU which RB Frame to use for the response message to this frame. The CLT shall ensure that all CNUs have sufficient time (as determined by the variable PhyLnkRspTm) to respond to the downstream PHY Link frame.

102.2.3.1.3 PHY Link DA

The PHY Link DA is an address field that identifies the CNU for which any EPoC message blocks in that PHY frame are targeted. This field is 15 bits and may be a unicast address or a broadcast address (see Table 102–8). In the CNU if the DA does not match the assigned address (*CNU_ID*) or the broadcast address, then the EMBs in the frame are discarded and no response is made. The CLT shall only transmit the valid values of the PHY DA field as given in Table 102–8.

Table 102–8—PHY DA field values

Field Values	Use
0x7F00 .. 0x7FF0	Broadcast addresses
0x7EFF ..0x0001	Unicast CNU addresses
0x0000	CLT PHY DA address

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102.2.3.1.4 PHY Timestamp

The PHY Timestamp is a 32-bit field that the EPoC PHY uses to synchronize the upstream PHY Link frame and OFDMA symbols. The *LocalTS*, from which this field is set, is clocked from the 204.8 MHz OFDM Clock. When a CNU PHY that has *PD_Enable* equal to FALSE receives a PHY Frame addressed to it or to the broadcast address, it shall reset its *LocalTS* to the value in the Timestamp. The reference point for the Timestamp shall be the first sample of the PHY Link symbol immediately following the Preamble (Figure 102–11). For additional information on the use of the Timestamp, see 101.3.3.1.3.

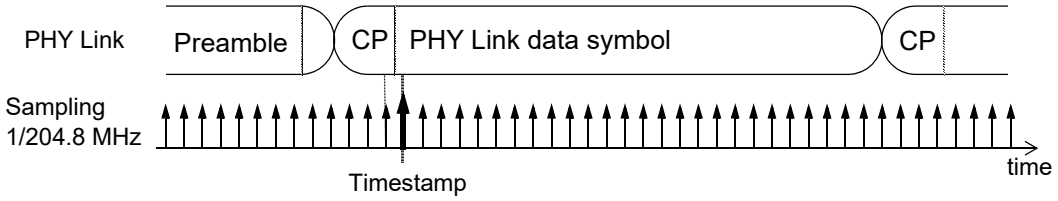

Figure 102–11—PHY Link Timestamp reference point

The CNU PHY Link receiver maintains counts of EPoC PHY Frame Headers received and those received that have CRC32 errors using the variables *EPFHcnt* and *EPFHerr*, respectively.

102.2.3.2 EPoC Probe Control Header message block

The EPoC Probe Control Header includes a Type field, the EPCH_Len field, the PrbType field, some number of Probe Control (PCn) fields, and a CRC32 as illustrated in Figure 102–1.

The EPCH_Len field is a 4-bit number that conveys the number of Probe Control fields contained in the message block. Each EPoC Probe Control Header may contain 0 to 15 Probe Control fields.

The PrbType field is a 2-bit field that conveys the type of Probe Control fields contained in the message block. There are three types of Probe Control fields; a Probe Scheduling type, a broadcast PHY Discovery type and a Unicast PHY Discovery type as shown in Table 102–9.

Table 102–9—PrbType values

PrbType value	Probe Control field	Probe Control length
0x00b	Probe Scheduling	32 bits
0x01b	Broadcast PHY Discovery	16 bits
0x10b	Unicast PHY Discovery	64 bits
0x11b	Reserved	n/a

The CNU PHY Link receiver maintains counts of EPoC Probe Control Headers received and those received that have CRC32 errors using the variables *EPCHcnt* and *EPCHerr,* respectively.

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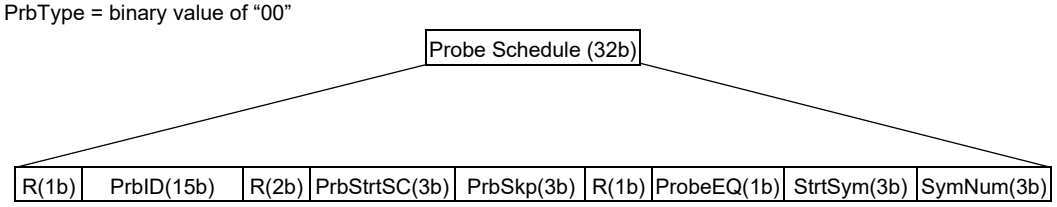
The CNU shall decode and be capable of acting on EPoC Probe Control Header instructions included in a downstream PHY Link frame within 2.5 ms after reception.

102.2.3.2.1 Probe Scheduling type Probe Control fields

The Probe Scheduling type Probe Control fields each enable one CNU to participate in the first Probe Period of the upstream PHY Link frame following the Response Frame ID. Each Probe Scheduling field contains a PrbID, PrbStrtSC, PrbSkip, PrbEQ, StrtSym, SymNum, and several reserved (R) subfields as illustrated in Figure 102–12. To enable a CNU to participate in a Probe Period the *CNU_ID* of the participating CNU is placed in PrbID subfield of the Probe Control. The remaining subfields set the corresponding variables in the designated CNU. A Probe Control field set to all zeros or any broadcast *CNU_ID* is ignored and does not enable any CNU. For additional information on use of the Probe Control fields, see 102.4.2.3.

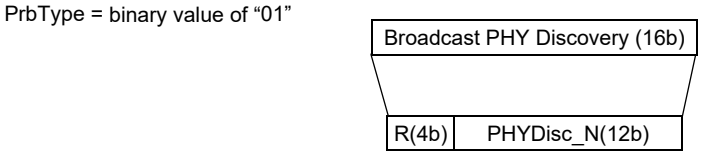


NOTE—The notation "(#b)" indicates the number of bits in the field.

Figure 102–12—Probe Scheduling type Probe Control field

102.2.3.2.2 Broadcast PHY Discovery type Probe Control fields

The Broadcast PHY Discovery type Probe Control fields each enable one PHY Discovery window within the Probe Period of the upstream PHY Link frame following the Response Frame ID. Each Broadcast PHY Discovery field contains a PHY Discovery window descriptor (PHYDisc_N), which designates the starting subcarrier of the PHY Discovery window as illustrated in Figure 102–13. For additional information on use of the Broadcast PHY Discovery type Probe Control fields, see 102.4.1.3.



NOTE—The notation "(#b)" indicates the number of bits in the field.

Figure 102–13—Broadcast PHY Discovery type Probe Control field

102.2.3.2.3 Unicast PHY Discovery type Probe Control fields

The Unicast PHY Discovery type Probe Control fields each enable a single CNU, as designated by a MAC address, to use a unique PHY Discovery window within the Probe Period of the upstream PHY Link frame following the Response Frame ID. Each Unicast PHY Discovery field contains a MAC address and a PHY Discovery window descriptor (PHYDisc_N), which designates the starting subcarrier of the PHY Discovery window as illustrated in Figure 102–13. For additional information on use of the Broadcast PHY Discovery type Probe Control fields, see 102.4.1.3.

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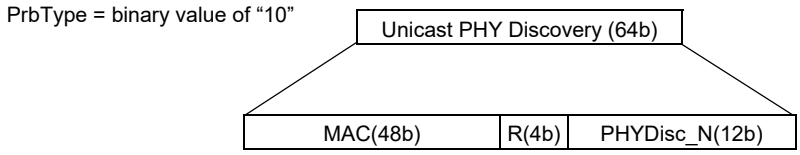

NOTE—The notation "(#b)" indicates the number of bits in the field.

Figure 102–14—Unicast PHY Discovery type Probe Control field

102.2.3.2.4 PHY Link managed variables

DiscStrt

TYPE: 32-bit unsigned integer
This variable indicates when the next PHY Discovery window is open relative to the downstream Timestamp. Setting the PHY Discovery start parameter to zero disables the PHY Discovery window.

102.2.3.3 Downstream EPoC message block

The downstream EPoC message block contains a Type field (see Table 102–6) a PHY Instruction and a CRC32.

The CLT can perform read and write operations on the EPoC variables of subordinated CNUs via PHY Instructions. Each instruction contains an OPCODE, a Variable Group Count, a Variable Index, and up to 31 Variable Group Data fields.

The PHY Link OPCODE is a 3-bit field that conveys the operation of the PHY Instruction in which it resides. The CLT shall only transmit the valid OPCODE field values as given in Table 102–10.

Table 102–10—Valid OPCODE values

Value	Operation	Description
b000	NOP	No operation, the CNU acknowledges this instruction only
b001	Read	The CNU responds with the contents of variables starting at the index specified by the Variable Group Index field and subsequent variables as specified by the Variable Group Count field
b010	Write	The CNU stores the values given in the data field starting at the variable given in the Variable Group Index field and subsequent variables as specified by the Variable Group Count field
b011	Write/Verify	The CNU first writes the variables as specified by Variable Group Index and Variable Group Count field and then responds with the values contained in those same variables
b1xx	Reserved	No operation, the CNU ignores these instructions

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The Variable Group Count field specifies the number of 16-bit EPoC Variable groups contained in a write or write/verify PHY Instruction or the number of 16-bit EPoC Variable groups that are to be returned in a read or write/verify PHY Instruction. The Variable Group Count field has a value of 0 to 31. The Variable Group Count field in a NOP instruction always has a value of 0. Whereas, for a read, write, or write/verify instruction, the Variable Group Count always has a value between 1 and 31.

The 16-bit EPoC Variable Index field specifies the variable group at which the CNU is to begin the read, write, or write/verify operation. The NOP instruction does not include an Index field.

The 16-bit Variable Group Data fields contain the data values to be written in consecutive variable groups starting with the group indicated by the Variable Index field and continuing for the number of groups indicated by Variable Group Count of the target CNU. The Variable Group Data fields are valid only for a write or write/verify PHY Instructions; or in the response to a read or write/verify PHY Instruction. In the event there is a discrepancy between the Variable Group Count field and the number of 16-bit Variable Group Data fields, the CNU shall write no data to its variables and returns a Nack indication (see 102.3.2.2).

The CNU PHY Link receiver maintains counts of EPoC message blocks received and those received that have CRC32 errors using the variables *EMBcnt* and *EMBerr,* respectively.

102.2.3.4 Downstream padding

The Pad field is used to fill the PHY frame in the event there are unused bits after the message blocks and FEC fields have been populated. The Pad field consists of all zeros and is ignored upon receipt.

102.2.3.5 Downstream FEC Parity message block

The FEC Parity message block includes a Type field, the FEC Codeword pointer (*FCP*), and a CRC32. The *FCP* is a 16-bit field used to identify the start of the first FEC codeword in the next PHY Link frame.

The CNU PHY Link receiver maintains counts of FEC Parity message blocks received and those received that have CRC32 errors using the variables *FPMEcnt* and *FPMEerr,* respectively.

102.2.4 Downstream PHY Link FEC

The downstream PHY Link shall use a binary punctured LDPC (384,288) code described in 102.1.4.1 and 102.1.4.3.1.

102.2.5 Downstream PHY Link response time.

The CNU shall decode and be capable of acting on EPoC message block instructions included in a downstream PHY Link frame within 4.8 ms. The CNU may indicate it is capable of a shorter response time to a downstream EPoC message block by setting the *PhyLinkRspTm* to a value of less than 61440 (4.8 ms).

102.2.6 PHY Link managed variables

DS_PhyLinkStrt

TYPE: 12-bit unsigned integer

This variable sets the starting subcarrier in OFDM Channel 1 of the downstream PHY Link. It specifies the lowest frequency subcarrier of the downstream PHY Link used to carry PHY Link information bits.

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102.2.7 Downstream state diagrams

102.2.7.1 Constants

EMB

TYPE: 4-bit unsigned integer
This constant represents the PHY Link message type for the EPoC message blocks.
VALUE: 0x0B

EPCHtp

TYPE: 4-bit unsigned integer
This constant represents the PHY Link message type for the EPoC Probe Control Header message block.
VALUE: 0x0A

EPFHtp

TYPE: 4-bit unsigned integer
This constant represents the PHY Link message type for the EPoC PHY Frame Header message block.
VALUE: 0x09

FPMBtp

TYPE: 4-bit unsigned integer
This value represents the PHY Link message type for the FEC Parity message block.
VALUE: 0x0C

MaxMBlen

TYPE: unsigned integer
This constant represents the maximum number of bits in the downstream PHY Link frame minus the length of the one CRC 32 and the FEC Pointer message block and excluding FEC Parity.
VALUE: 2824

102.2.7.2 Counters

EMBcnt

TYPE: 16-bit unsigned integer
This variable counts the number of EPoC message blocks received. The variable is cleared when read and does not roll over at maximum count.

EMBerr

TYPE: 16-bit unsigned integer
This variable counts the number of EPoC message blocks received with CRC32 errors. The variable is cleared when read and does not roll over at maximum count.

EPCHcnt

TYPE: 16-bit unsigned integer
This variable counts the number of EPoC Probe Control Headers received. The variable is cleared when read and does not roll over at maximum count.

EPCHerr

TYPE: 16-bit unsigned integer
This variable counts the number of EPoC Probe Control Headers received with CRC32 errors. The variable is cleared when read and does not roll over at maximum count.

EPFHcnt

TYPE: 16-bit unsigned integer

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This variable counts the number of EPoC PHY Frame Headers received. The variable is cleared when read and does not roll over at maximum count.

EPFHerr

TYPE: 16-bit unsigned integer
This variable counts the number of EPoC PHY Frame Headers received with CRC32 errors. The variable is cleared when read and does not roll over at maximum count.

FPMEcnt

TYPE: 16-bit unsigned integer
This variable counts the number of FEC Parity message blocks received. The variable is cleared when read and does not roll over at maximum count.

FPMEerr

TYPE: 16-bit unsigned integer
This variable counts the number of FEC Parity message blocks received with CRC32 errors. The variable is cleared when read and does not roll over at maximum count.

LocalTS

TYPE: 32-bit unsigned integer
This counter holds the value of the local Timestamp. The counter is advanced by the OFDM Clock and rolls over to zero from 0xFF-FF-FF-FF. At the CLT the counter shall track the transmit clock, while at the CNU the counter shall track the receive clock. For accuracy of receive clock, see 101.4.4.2.

102.2.7.3 Variables

BEGIN

TYPE: Boolean
This variable is used when initiating operation of the functional block state diagram. It is set to TRUE following initialization and every reset.

DS_CID

TYPE: 2-bit unsigned integer
This variable represents the downstream Configuration ID value as described in 102.2.3.1.

FCP

TYPE: unsigned integer
This variable represents the beginning of the first MAC data FEC codeword in the current downstream PHY Link frame as described in 102.2.3.5.

FmLen

TYPE: unsigned integer
This variable represents the total number of bits transmitted in the current PHY Link frame.

PC_Fifo

TYPE: bit array
This variable holds the Probe Scheduling, Broadcast PHY Discovery, or Unicast PHY Discovery variables to be transmitted in the next EPCH message block.

PhyDA

TYPE: 15-bit unsigned integer
This variable represents the *CNU_ID* of the intended recipient of the PHY Link frame.

PhyDA_Fifo

TYPE: bit array
This variable holds the CNU_IDs to which the PHY Link frame and each PHY Link Instruction is to be sent. For any single PHY Link Frame there is one entry for the frame and one entry for each instruction.

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PhyLinkRspTm

TYPE: 16-bit unsigned integer

This read only variable indicates the PHYs minimum response time to a downstream PHY Link instruction in units of 16/204.8 MHz. The maximum value for this variable is 61440 (4.8 ms), which is also the default value for this variable.

PhyTD

TYPE: bit array

This variable represents a bit array corresponding to data to be sent over the PHY Link.This variable is used to accumulate payload of outgoing PHY Link message blocks, for example to set the Timestamp Message Block.

PhyTxFifo

TYPE: bit array

This variable holds a series of PHY Instructions to be transmitted in the next PHY frame. Each entry in the fifo includes Opcode, Count, Variable Group Index, and Data fields for each instruction.

RF_ID

TYPE: 8-bit unsigned integer

This variable represents the Response Frame ID as described in 102.2.3.1.

RT

TYPE: Boolean

This variable represents the Response Type as described in 102.2.3.1.

PhyLnkRspTm

TYPE: 16-bit unsigned integer

The value of this variable defines the minimum time, in units of 78.125 ns (16 × 1/204.8 MHz), after receiving the last bit of the FEC, needed by the CNU to decode and prepare the response to a PHY Link Instruction.

PrbCtrl

TYPE: 32-bit binary

These variables represent the eight Probe control fields as described in 102.2.3.2.

StrtOfFm

TYPE: Boolean

When this variable transitions from FALSE to TRUE it indicates the beginning of an OFDM frame.

tmpDA

TYPE: 15-bit unsigned integer

This variable represents the *CNU_ID* of the intended recipient of the EPoC message blocks included in the PHY Link frame.

PD_Enable

TYPE: Boolean

This variable enables the device to respond to a PHY Discovery window and transmit onto the media when TRUE. It is set to FALSE following initialization and every reset. In the CNU it is set to TRUE after all elements required for PHY Discovery listed in Table 102–13 have been written by the CLT. In the CLT this variable, when set to FALSE, prevents transmissions from the CLT until it is fully configured and when TRUE permits transmissions.

TxPre

TYPE: Boolean

When TRUE, this variable indicates the PHY Link should be sending the preamble pattern as defined in 102.2.2.

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US_CID

TYPE: 2-bit binary
This variable represents the upstream Configuration ID value as described in 102.3.2.1.

102.2.7.4 Functions

CRC32(x)

This function returns a 32-bit CRC of the bit array *x* (see 3.2.9).

LEN(x)

This function returns the length of variable *x*.

PCnxt(x)

This function removes and returns the next *x* bits from the *PC_Fifo* bit array.

POP()

This function removes one record from the *PhyTxFifo*.

PUSH()

This function returns one record from the *PhyTxFifo*.

Send(x)

This function transfers the contents of variable *x* to the PHY Link FEC Encoder block. When the transfer is complete, the variable length is zero.

102.2.7.5 State diagrams

The CLT PHY Link transmit process shall conform to the state diagram shown in Figure 102–15.

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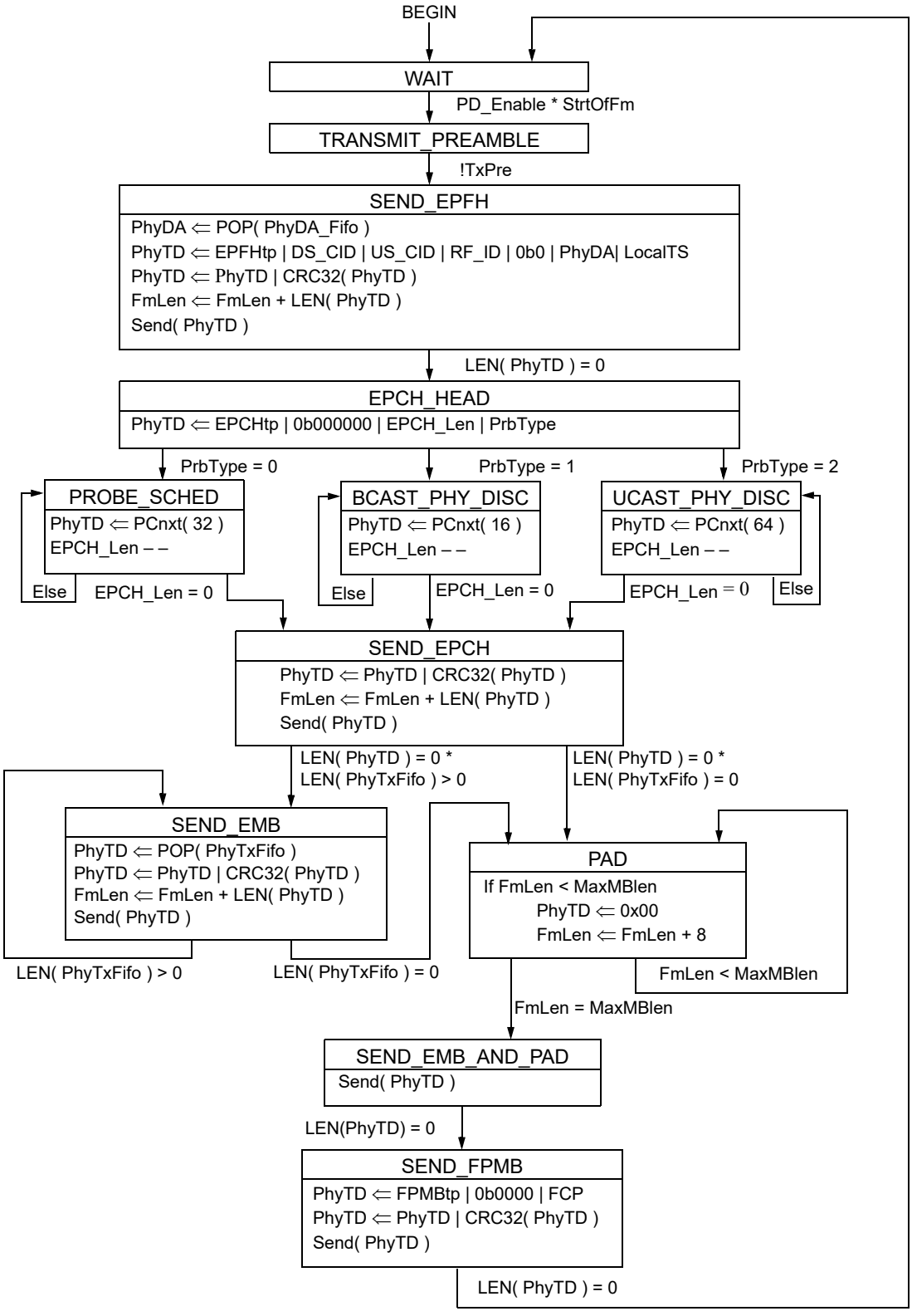

Figure 102–15—CLT PHY Link transmit process state diagram

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102.3 Upstream PHY Link

102.3.1 Upstream PHY Link Physical Layer

102.3.1.1 Upstream resource allocation

During network setup the upstream PHY Link shall be allocated 400 kHz of spectrum. The upstream PHY Link is located per the *US_PhyLinkStrt* variable (see 102.3.5.3) that determines the lowest frequency subcarrier of the PHY Link. The upstream PHY Link shall use the same cyclic prefix duration and window size as the upstream MAC data OFDM channel.

102.3.1.2 Upstream PHY Link modulation

The upstream PHY Link shall use any of the modulation formats listed under PHY Link CNU Tx/CLT Rx in Table 100–2 and is set using the *US_PhyLinkMod* variable.

102.3.1.3 Upstream PHY Link transmission

CNU only operation: upon initialization of the CNU, the PMD_SIGNAL.request(*Tx_enable*) primitive is set to the value OFF in the PHY Link. When the first bit of a PHY Link message arrives at the PHY Link symbol mapper, the CNU sets the PMD_SIGNAL.request(*Tx_enable*) primitive to the value ON, which instructs the PMD sublayer to start the process of turning the RF power amplifier ON (see Figure 101–2 and 100.3.4.6). When the last bit of a PHY Link message arrives at the PHY Link symbol mapper, the CNU sets the PMD_SIGNAL.request(*Tx_enable*) primitive to the value OFF, which instructs the PMD sublayer to start the process of turning the RF power amplifier off.

102.3.2 Upstream PHY Link frame

The upstream PHY Link frame is composed of the EPoC PHY Frame Header, optional EPoC message blocks, and an FEC. These messages are described in the paragraphs that follow.

Each message block contains a Type field used to identify the contents of the block. CNUs shall use the appropriate message Type fields listed in Table 102–6 in each message block.

The contents of the each message block is protected by a CRC32. See 3.2.9 for a description of how this field is calculated. The CLT shall calculate a CRC32 on the data fields within each message block received and, if the calculated CRC32 does not match the received CRC32, discard the message and take no action based on it. The CLT PHY Link receiver maintains count of EPoC PHY Frame Headers received and those received that have CRC32 error using the variables *EPFHcnt* and *EPFHerr*, respectively.

102.3.2.1 Upstream EPoC PHY Frame Header

The upstream EPoC PHY Frame Header includes a Type field, the Return Frame ID field, the PHY SA, the PHY Timestamp field, and a CRC32 as illustrated in Figure 102–2. The Type field and Return Frame ID field are echoes of the same fields in the downstream message to which the CNU is responding. The PHY SA is an address field that identifies the CNU from which the PHY frame is transmitted. This field is 15 bits and is always the unicast address (*CNU_ID*) associated with the CNU transmitting in the PHY Link (see Table 102–8). The CNU SA is assigned during the PHY Discovery process (see 102.4.1). The PHY Timestamp is a 32-bit field set from the *LocalTS*.

102.3.2.2 Upstream EPoC message block

The EPoC message block contains a Type field (see Table 102–6), the PHY Response and a CRC32.

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If the downstream PHY Link EPoC PHY Frame Header contains the unicast *CNU_ID* for the CNU, the addressed CNU shall respond to PHY Link instructions using the PHY Response. Each Response contains an OPCODE, a Variable Group Count, an Variable Group Index, and up to 31 Variable Group Data fields.There is a one-to-one correspondence between PHY Instructions in the downstream PHY Link and PHY Responses in the upstream PHY Link.

The PHY Response OPCODE is a 3-bit value that conveys the acknowledge type for the PHY Instruction to which the CNU is responding and the success or failure of the PHY Instruction command. CNUs shall use the valid values of the acknowledgment type given in Table 102–11.

Table 102–11—OPCODE Acknowledgement values

Value	Operation	Description
b000	NOP ACK	NOP Instruction acknowledge returned in response to a successfully received NOP Instruction
b001	Read ACK	Read Instruction acknowledge returned in response to a successfully received and executed read Instruction along with the requested variables as specified in the Variable Group Index and Variable Group Count fields of the PHY Instruction
b010	Write ACK[a]	Write Instruction acknowledge returned in response to a successfully received and executed Write Instruction
b011	Write/Verify ACK[a]	Write/Verify Instruction acknowledge returned in response to a successfully received and executed Write/Verify Instruction along with the requested variables as specified in the Variable Group Index and Variable Group Count fields of the PHY Instruction
b100	NOP NACK	NOP Instruction negative acknowledge returned in response to a unsuccessfully received NOP Instruction
b101	Read NACK	Read Instruction negative acknowledge returned in response to an unsuccessfully received or executed Read Instruction
b110	Write NACK	Write Instruction negative acknowledge returned in response to an unsuccessfully received or executed Write Instruction
b111	Write/Verify NACK	Write/Verify Instruction negative acknowledge returned in response to an un successfully received or executed Write/Verify Instruction

[a]A write or write/verify PHY Instruction to an index that contains read-only bits is considered successful when all read/write bits in the index are written.

The Variable Group Count field specifies the number of 16-bit variable groups that are being returned in response to a read or write/verify PHY Instruction. In the event the CNU is returning a Nack response (Acknowledgment values 0b100 through 0b0111) the Variable Group Count field shall be set to zero and is ignored at the CLT.

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The 16-bit Variable Group Index field specifies the first index for which the CNU is returning data due to a read or write/verify operation or the first index of the corresponding write Instruction.

The 16-bit Variable Group Data fields contain the data values read from the variables due to a read or write/verify PHY Instruction. In the event the CNU is responding to a write instruction this field is omitted. The Variable Group Data field should be omitted in Nack Responses (Acknowledgment values 0b100 to 0b111) and, if included, shall be ignored at the CLT.

The CLT PHY Link receiver maintains count of EPoC message blocks received and those received that have CRC32 error using the variables *EMBcnt* and *EMBerr,* respectively.

102.3.2.2.1 Padding

The Pad field is used to fill the PHY frame in the event there are unused bits after the message blocks and FEC fields have been accounted for.

102.3.3 Upstream PHY Link FEC

The upstream PHY Link shall use a (384,288) binary punctured LDPC code described in 102.1.4.1 and 102.1.4.3.1.

102.3.4 Upstream PHY Link pilot pattern

The upstream PHY Link utilizes a pilot pattern to assist the CLT receiver in capturing the bursting PHY Link transmissions. The PHY Link pilot pattern is illustrated in Figure 102–16. PHY Link pilots are BPSK encoded. The two edge subcarriers of the upstream PHY Link are Type 2 pilots; whereas, the six internal subcarriers are Type 1 Pilots.

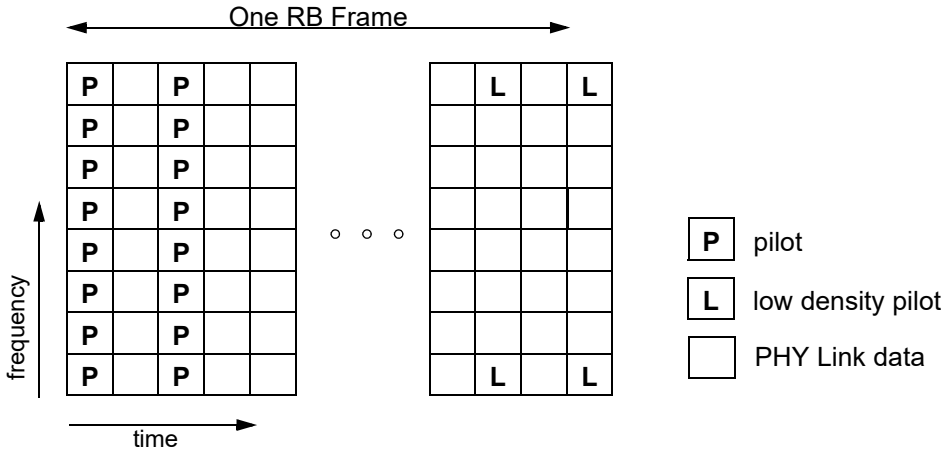

Figure 102–16—Upstream PHY Link pilot pattern

102.3.5 Upstream state diagrams

102.3.5.1 Constants

EPFHtp

See 102.2.7.1.

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USPLfec

TYPE: Integer
This constant represents the upstream PHY Link FEC data length.
Value: 288

102.3.5.2 Counters

EMBcnt

See 102.2.7.2.

EMBerr

See 102.2.7.2.

EPFHcnt

See 102.2.7.2.

EPFHerr

See 102.2.7.2.

US_FmCnt

TYPE: 9-bit unsigned
This modulo 262 counter tracks the OFDMA symbols within the upstream superframe. Symbol zero is the first symbol in the Probe Period.

102.3.5.3 Variables

CNU_ID

TYPE: 15-bit integer that carries the value of the CNU_ID assigned by the CLT to the CNU during PHY Discovery process (see 102.4.1.6).

PhyDA

See 102.2.7.3.

PhyTD

See 102.2.7.3.

PhyTxFifo

See 102.2.7.3.

RF_ID

See 102.2.7.3.

RT

See 102.2.7.3.

PD_Enable

See 102.2.7.3.

PdCmplt

TYPE: Boolean
When TRUE this variable indicates the CNU has completed the PHY Discovery process and is allowed to transmit in the OFDMA MAC and PHY Link data paths.

US_PhyLinkMod

TYPE: 4-bit binary
This variable sets the type of modulation used for the upstream PHY Link. The assignment of bits to each modulation type is shown below.
bit 3 2 1 0
1 x x x = reserved
0 1 1 1 = 128-QAM

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0 1 1 0 = 64-QAM
0 1 0 1 = 32-QAM
0 1 0 0 = 16-QAM
0 0 1 x = reserved
0 0 0 1 = BPSK

US_PhyLinkStrt

TYPE: 12-bit unsigned integer
This variable indicates the starting subcarrier of the upstream 10GPASS-XR PHY Link. It specifies the lowest frequency subcarrier of the upstream PHY Link used to carry PHY Link information bits.

102.3.5.4 Functions

CRC32()

See 102.2.7.4.

LEN()

See102.2.7.4.

Mod(x,y)

This function returns the remainder of *x/y*.

POP()

See 102.2.7.4.

Send()

See 102.2.7.4.

102.3.5.5 State diagrams

The CNU PHY Link transmit process shall conform to the state diagram shown in Figure 102–17.

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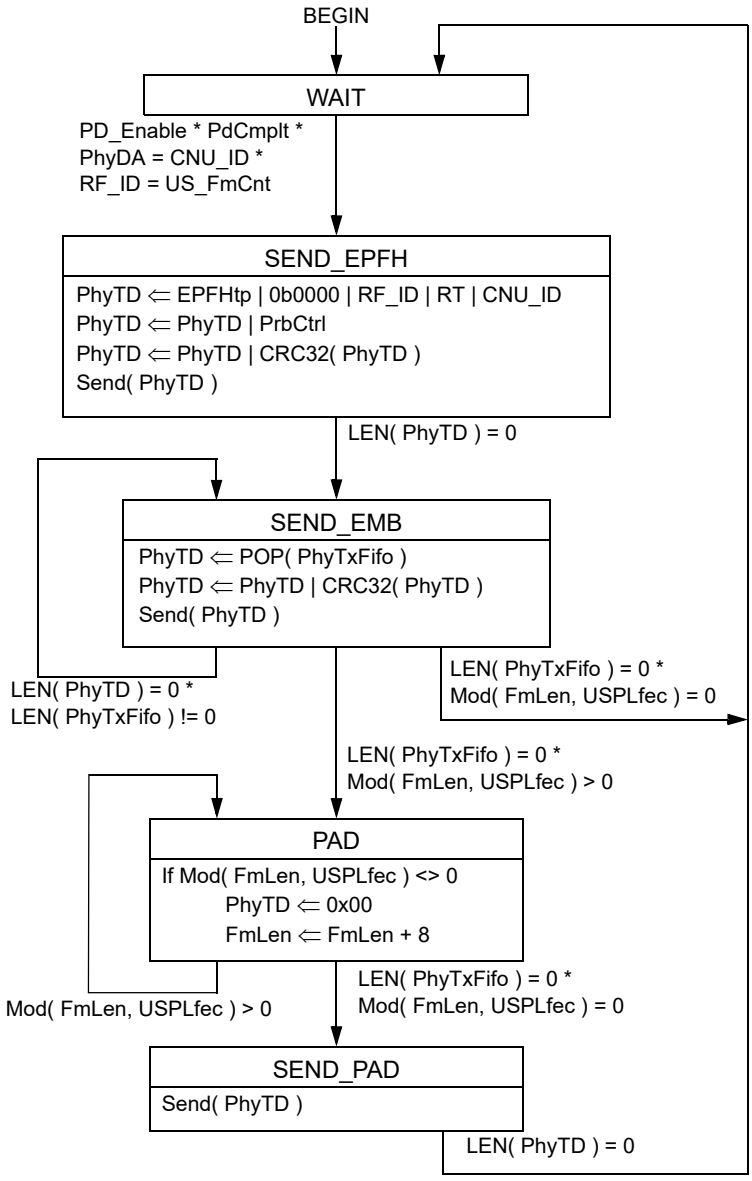

Figure 102–17—CNU PHY Link transmission control state diagram

102.4 PHY Link applications

When a CNU first joins the EPoC network it has no prior knowledge of the upstream RB Superframe configuration and timing necessary to produce transmissions that are orthogonal to the rest of the EPoC network when viewed from the perspective of the CLT receiver. PHY Discovery is the process whereby newly connected or off-line CNUs are provided timing and operating parameters necessary to function properly in the EPoC network.

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While an EPoC network is in operation, periodic verification of the CNUs OFDMA timing, transmission power, and pre-equalizer coefficients is needed to ensure orthogonality and proper reception. This is accomplished using Wideband Probing. Wideband Probing may also used during the PHY Discovery process to fine tune the timing of CNUs joining the network.

102.4.1 PHY Discovery

102.4.1.1 Overview of PHY Discovery

The PHY Discovery process is composed of PHY Link acquisition, PHY Discovery window opening, PHY Discovery Response, CNU_ID Allocation, and Wideband Probing. Each of these steps is described in detail in the following subclauses. The PHY Discovery message exchange is illustrated in Figure 102–18.

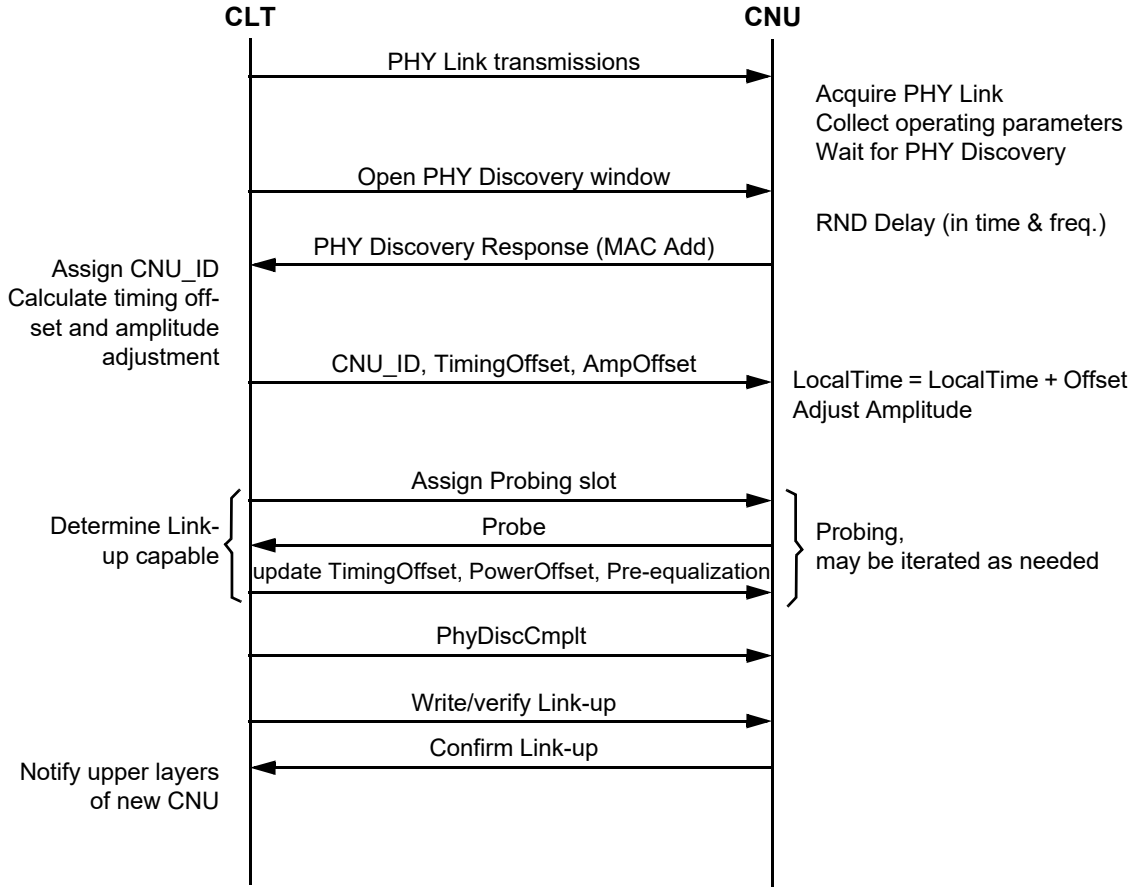

Figure 102–18—PHY Discovery message exchange

102.4.1.2 PHY Link acquisition

When a CNU joins an EPoC network it first locates the downstream PHY Link. This is typically done via a vendor specific correlation algorithm. Prior to any transmission in an EPoC network the CNU shall locate

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the downstream PHY Link, gather the required PHY Discovery operating parameters listed in Table 102–13 and synchronize its 10.24 MHz Master Clock to the downstream OFDM Clock. Once the CNU has completed the prerequisites for transmission it waits for the CLT to issue a PHY Discovery window.

102.4.1.3 PHY Discovery window opening

The CLT periodically makes available PHY Discovery windows during which off-line CNUs are given the opportunity to make themselves known to the CLT. The periodicity of these windows is unspecified. The CLT signifies that a PHY Discovery period is occurring by transmitting either a Broadcast PHY Discovery type or Unicast PHY Discovery type Probe Control message block.

The PHY Discovery window is coincident with the Probe symbols (see 101.4.3.10) but is only four symbols in duration to allow for timing ambiguity in the PHY Discovery Response.

102.4.1.4 PHY Link Discovery Response

Off-line CNUs, upon being notified of a PHY Discovery window, wait for the beginning of the PHY Discovery window and then transmit a PHY Discovery Response to the CLT. The CNU initially transmits a PHY Discovery Response using the power level indicated by *PdRespInitPwr*. If there is no acknowledgment from the CLT to the initial PHY Discovery Response the CNU increases the PHY Discovery Response transmit power by the value indicated by *PdRespPwrStep*. The CNU continues to increases the PHY Discovery Response transmit power by the value indicated by *PdRespPwrStep* until an acknowledgment is received from the CLT. If the CNU has transmitted four PHY Discovery Responses at maximum power without acknowledgment from the CLT it reverts to the power level indicated by *PdRespInitPwr* and begins incrementing its output power as described previously.

PHY Discovery windows are unique in that they are the only times when multiple CNUs can access the coax cable distribution network using the same RF spectrum simultaneously, and transmission overlap can occur in both time and frequency. In order to reduce transmission overlaps, a contention algorithm is used by all off-line CNUs. Measures are taken to reduce the probability for overlaps by artificially introducing a random distribution in the PHY Discovery window used by each CNU. Each CNU selects a random number of PHY Discovery windows it waits before transmitting the PHY Discovery Response. Multiple valid PHY Discovery Responses that overlap in time, but not frequency, may be received by the CLT during a single PHY Discovery window depending on the modulated spectrum of the upstream OFDM channel.

Included in the PHY Discovery Response is a preamble (see 102.4.1.5), the CNU's MAC address and a 32-bit CRC. See 3.2.9 for a description of how the 32-bit CRC is calculated. The data in the PHY Discovery Response shall be encoded using a (128,80) binary punctured LDPC code described in 102.1.4.3.2.

The PHY Discovery Response is composed of 128 subcarriers with a duration of four symbols and may include exclusions between these 128 subcarriers (see Figure 102–19). In a single Probe Period there may be up to 16 PHY Discovery windows. For the purposes of PHY Discovery Response contention mitigation, the broadcast PHY Discovery windows are numbered consecutively from lower starting frequency to higher starting frequency and increasing as time progresses as illustrated in Figure 102–20. Unicast PHY Discovery windows are not numbered for contention mitigation purposes.

In the event there is an analog fiber segment between the CLT and CNU, the CLT can delay the PHY Discovery Response by the amount of time specified in *PhyRngOffset*.

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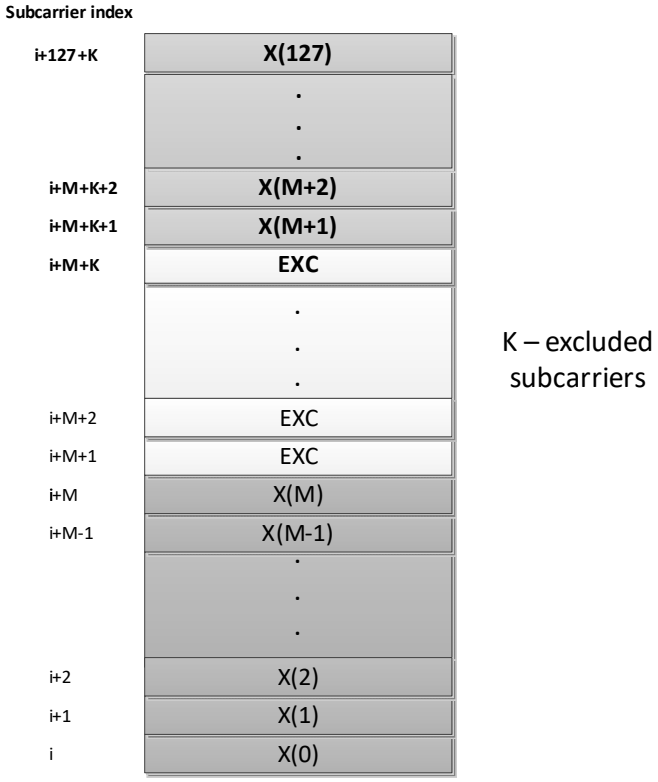

Figure 102–19—PHY Discovery Response sequence with exclusions

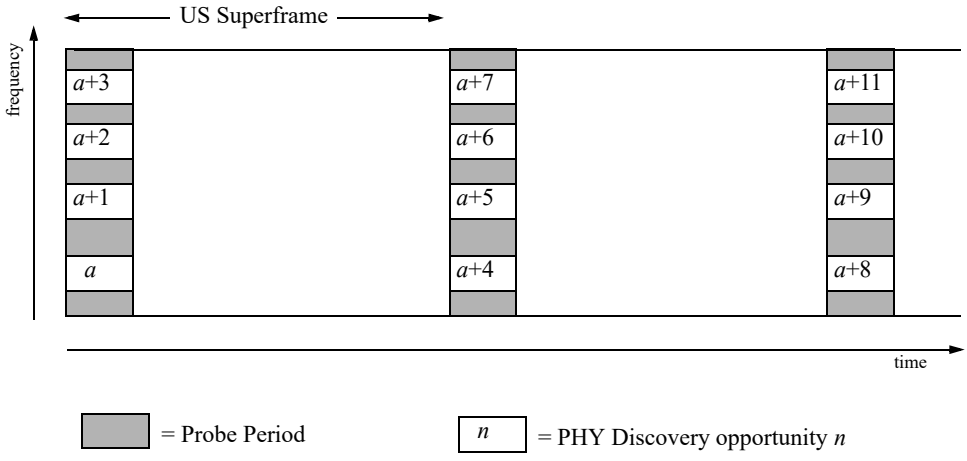

Figure 102–20—PHY Discovery opportunity numbering

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The CNU PHY Discovery Response is only allowed after a CNU has completed the PHY Discovery prerequisites (Table 102–13). In the PHY Discovery Response message, the preamble used is the special PHY Discovery Preamble (see 102.4.1.5) and the only data included is the CNU MAC address protected by a CRC32. The PHY duplicates symbols of the upstream PHY Discovery Response transmission. This duplication is accomplished by duplicating the time domain samples at the output of the iFFT in the upstream data path for these signals, and adding cyclic prefix and windowing (per variables *USNcp* and *USNrp*, respectively) as illustrated in Figure 102–21. Control for the duplication process is conveyed using the TxType in the CNU (see Figure 102–4).

The CLT calculates the range of the CNU based on the PHY Link Response and uses this to report the NewCNU_Rng when declaring the CNU link-up (see 102.4.3).

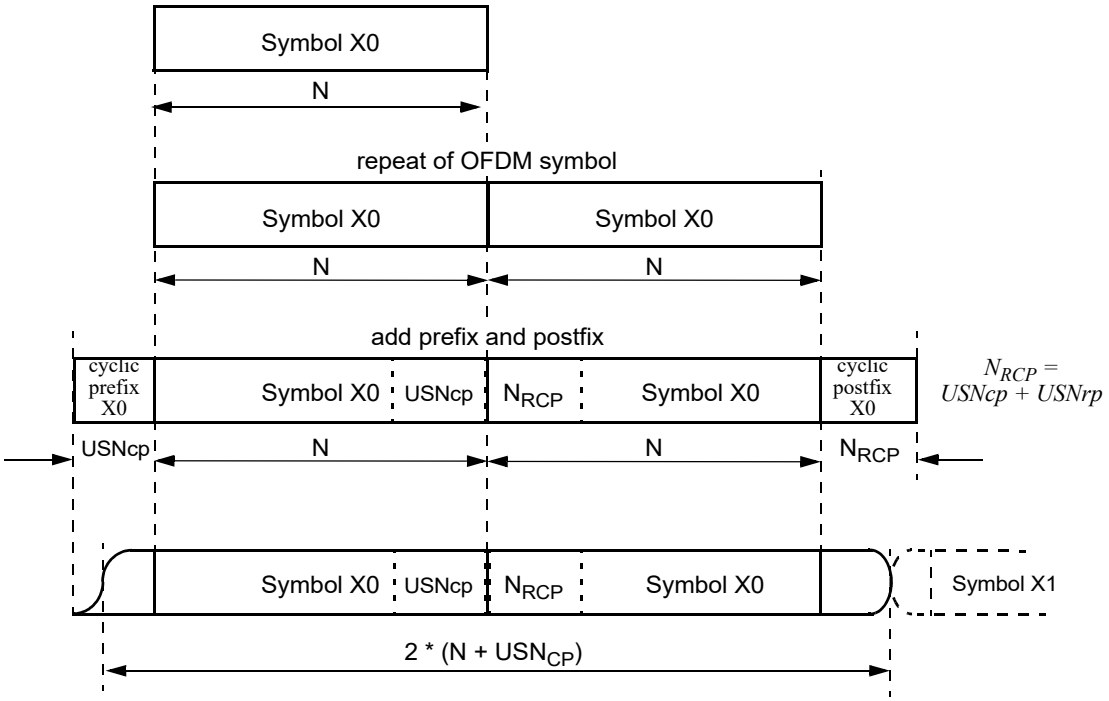

Figure 102–21—Symbol duplication, cyclic prefix, and windowing algorithm for PHY Discovery Response

102.4.1.5 PHY Discovery preamble

The PHY Discovery preamble is transmitted in the first two symbols of the PHY Discovery Response. The first symbol of the preamble shall be populated with a BPSK mapped 128-bit sequence generated by a pseudo-random sequence generator defined by the polynomial $x^7 + x^1 + 1$ seeded with a fixed bit pattern of 0x55 (see Figure 102–22) at the beginning of the PHY Discovery Response (see Figure 102–23). The output of the sequence generator is mapped using BPSK modulation (see 101.4.5.2) where a bit value of 0 is mapped to a BPSK value of plus 1 and a bit value of 1 is mapped to a BPSK value of minus 1. The second symbol of the PHY Discovery preamble shall be a duplicate copy of the first symbol as illustrated in Figure 102–21.

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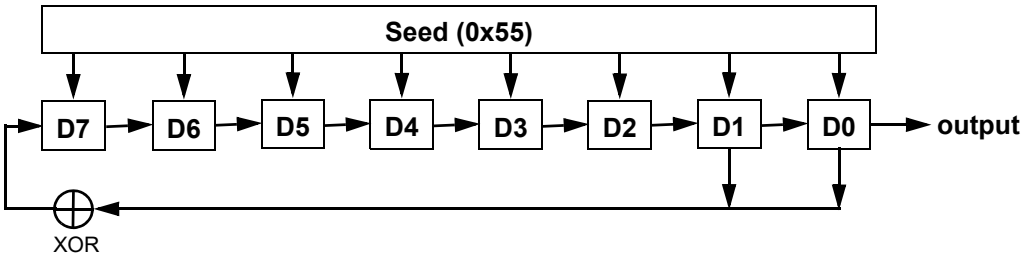

Figure 102–22—PHY Discovery Preamble generator

102.4.1.6 CNU_ID allocation

Upon receipt of a valid PHY Discovery Response, the CLT updates the CNU by allocating and assigning a new port identity (*CNU_ID*) using the *AssgndCNU_ID* and *AllwdCNU_ID* variables. To allocate the *CNU_ID* the CLT shall use the CNU_ID Allocation instruction as defined in Table 102–12. This instruction uses a broadcast DA.

The CLT calculates an OFDMA timing and power offsets and adjusts the CNU using the *PHYTimingOffset* and *PHYPowerOffset* variables, respectively. These parameters are transmitted to the CNU via the CNU_ID Allocation instruction. The first EMB of the CNU_ID Allocation instruction is a write of the *New_MACn* variables (note that this variable is read only so the actual variable value in the CNU will not change). The value written is the CNU MAC address received in the PHY Discovery Response.

The second EMB writes *AllwdCNU_ID* and sets *AssgndCNU_ID* to TRUE in the CNU. This causes the value of *AllwdCNU_ID* to be assigned in the CNU. Thereafter the CLT cannot use the same value of *AllwdCNU_ID* for another newly discovered CNU. See 102.4.3 for additional information on use of *AllwdCNU_ID* and *AssgndCNU_ID.*

Subsequent EMBs are used to write the CNU *PHYTimingOffset* and *PHYPowerOffset* variables.

Table 102–12—Special Instruction sequences

Special Instruction	EMB order	Read/Write	Variable
CNU_ID Allocation	1	Write	*New_MAC0* through *New_MAC2*
	2	Write	*AllwdCNU_ID*
	3	Write	*PHYTimingOffset* *PHYPowerOffset*

When the CNU receives the *PhyTimingOffset* variable, it shall add the new value of *PhyTimingOffset* to the *LocalTS* affecting the CNU transmit timing accordingly. When the CNU receives the *PhyPowerOffset* variable, it shall add the new value of *PhyPowerOffset* to the *PHYPowerOut* affecting the CNU transmit power accordingly.

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102.4.1.7 PHY Discovery completion

When the CLT determines [via Wideband Probing (see 102.4.2), updates to *PhyTimingOffset,* and updates to *PhyPowerOffset*] that the new CNU has successfully tuned its transmitter to be orthogonal to the rest of the CNUs on the coax cable distribution network, it sets *PhyDiscCmplt* TRUE. This signifies that the CNU has completed the process of PHY Discovery.

102.4.1.8 PHY Link managed variables

AllwdCNU_ID

TYPE: 15-bit unsigned integer

This variable is used to indicate to the 10GPASS-XR PHY a valid *CNU_ID* value. The value may be assigned to a new CNU when the associated *CNU_ID* assigned flag (*AssgndCNU_ID*) is set to zero, when the flag is set to one it is an indication that this value has already been assigned to a CNU and it should not be use for another CNU.

AssgndCNU_ID

TYPE: Boolean

The value of this variable is used to indicate if the associated *AllwdCNU_ID* value has been assigned to a CNU by the PHY. When the flag is set to TRUE the associated *AllwdCNU_ID* has been assigned to a new CNU whereas when the flag is set to FALSE the associated *AllwdCNU_ID* has not been assigned.

DS_OFDM_ID

See 101.4.3.4.5.

LinkUpRdy

TYPE: Boolean

This Boolean variable is set to TRUE by the CLT when it has verified all of the variables required for Link-Up state in Table 102–13. The variable is set to FALSE on reset or as described in 102.4.4.

NewCNU_Rng

TYPE: 16-bit unsigned integer

This variable indicates the range of the CNU corresponding to Allowed CNU_ID in units of OFDM Clock periods (1/204.8 MHz).

PhyDiscCmplt

TYPE: Boolean

When TRUE, this variable indicates that the CNU has completed PHY Discovery (see 102.4.1) on the coaxial cable distribution network. When FALSE, the variable indicates that the PHY has not completed PHY Discovery on the coaxial cable distribution network. This variable is defined in 10GPASS-XR-U PMA/PMD only. The variable is set to FALSE on any reset.

PdRespInitPwr

TYPE: 8-bit unsigned integer

This variable is used to set the initial transmit level, in units of 0.25 dBmV/1.6 MHz, for a CNUs PHY Discovery Response message. The range of this variable is from 0 to 64 dBmV/1.6 MHz.

PdRespPwrStep

TYPE: 8-bit unsigned integer

This variable is used to increase the transmit level, in units of 0.25 dB, for a CNUs PHY Discovery Response message in the event a PHY Discovery Response sent by the CNU is not acknowledged by the CLT.

PdRndDly

TYPE: unsigned integer

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This variable indicates the random delay, in PHY Discovery windows, selected by the PHY to avoid contention during PHY Discovery.

PhyPowerOffset

TYPE: signed 8-bit integer
This variable is used to set the CNU upstream transmitter power by specifying the relative change in transmission power level the CNU is to make, in units of 0.25 dB, in order that transmissions arrive at the CLT at the desired power level. Changing the value of this variable while running using Management is highly undesirable and is unspecified.

PhyRngOffset

TYPE: 32-bit unsigned integer
This variable may be used to provision a delay in the ranging response, in units of 1/204.8 MHz, in the event there is an analog optical segment between the CLT and the CNUs as described in 102.4.1.4. This variable defaults to a value of 0 on reset.

PhyTimingOffset

TYPE: signed 32-bit integer
This variable is used to align the CNU to the upstream OFDM timing in units of 1/204.8 MHz. A negative value causes the timing of the CNU transmissions to be delayed. Changing the value of this variable while running using Management is highly undesirable and is unspecified.

102.4.1.9 PHY Discovery state diagrams

102.4.1.9.1 Constants

Pad96

TYPE: 96 bit binary
This constant holds 96 bits of padding.
Value: 0

102.4.1.9.2 Variables

New_MAC

TYPE: 48-bit hex
This vairable holds the MAC address of the CNU.

NxtWin

TYPE: unsigned integer
This variable holds the subcarrier index for the next PHY Discovery window.

PdData

TYPE: bit array
This variable holds the data to be transmitted in the PHY Discovery window.

PdWinFifo

TYPE: bit array
This fifo holds the list of 12-bit subcarrier indexes for each PHY Discover window from the most recent EPoC Probe 64B/65B sync header bit message block.

PdWinTp

TYPE: Boolean
This variable indicates if the list PHY Discover windows in *PdWinFifo* are unicast or broadcast windows. *PdWinTp* has the value of Ucast when the PHY Discovery window is unicast and Bcast when the window is broadcast.

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Rnd

TYPE: 8-bit unsigned integer
This variable is used as a seed in the back-off algorithm for the PHY Discovery Response.

SoSF

TYPE: Boolean
This variable indicates the beginning of the upstream superframe and is set to TRUE for one OFDM Clock period at the beginning of the superframe.

PD_Enable

See 102.2.7.3.

102.4.1.9.3 Counters

SC_Cnt

TYPE: 12-bit
This counter tracks the subcarriers within each symbol and increments once for every subcarrier. Subcarrier zero is the first subcarrier while subcarrier 4095 is the last. The counter is reset at the beginning of every symbol.

102.4.1.9.4 Functions

CRC32()

See 102.2.7.4.

Len(x)

See 102.2.7.4.

PD_Pre

This function returns the PHY Discovery preamble as described in 102.4.1.5.

POP(x)

See 102.2.7.4.

rnd(r)

This function returns a random integer number uniformly distributed between 1 and *r*.

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102.4.1.9.5 State diagrams

The CNU PHY Discovery Response transmission control shall conform to the state diagram shown in Figure 102–23.

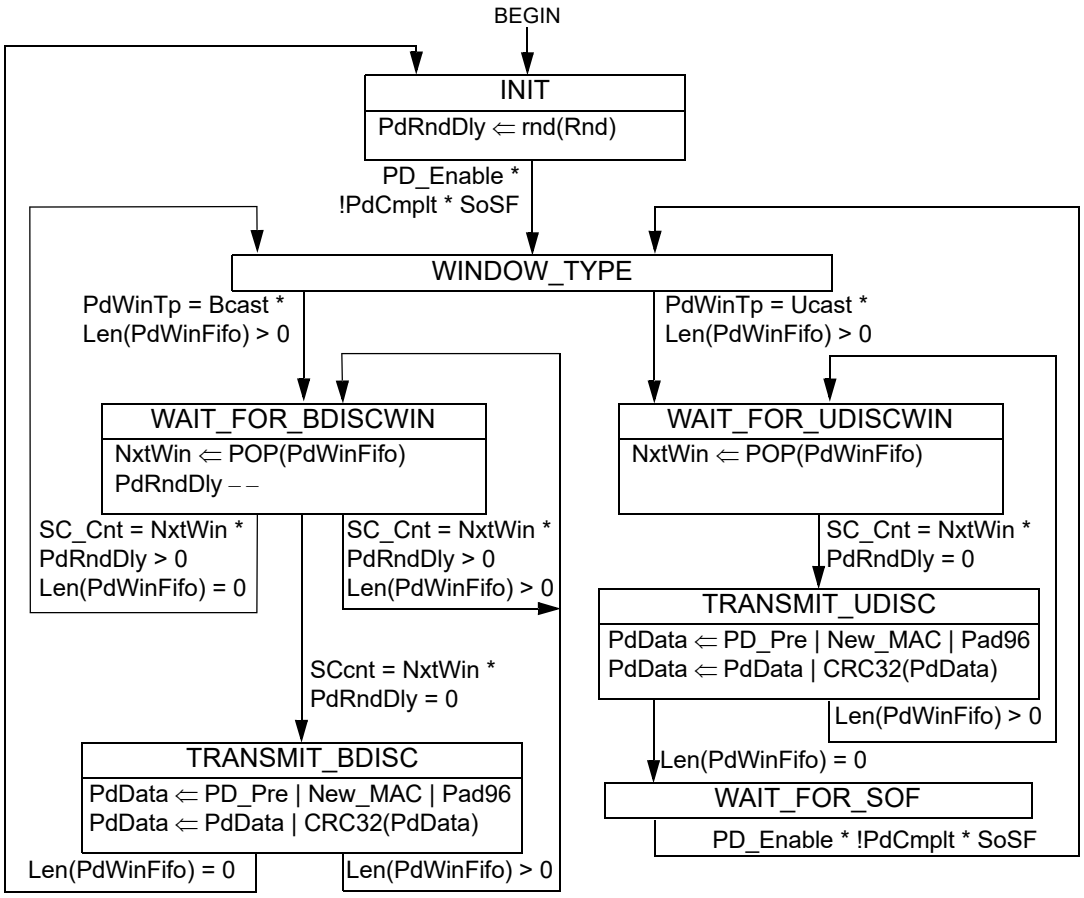

Figure 102–23—CNU PHY Discovery Response transmission control state diagram

102.4.2 Upstream Wideband Probing

102.4.2.1 Introduction

In upstream Wideband Probing a CNU transmits pilots spanning all active subcarriers. The CNU transmits one pilot per subcarrier. Each pilot is a predefined BPSK symbol. Each upstream superframe begins with six symbols, called the Probe Period, designated for probing and PHY Discovery. Each symbol within the Probe Period is referred to as a probing symbol. The CLT may use the received probing symbol for the following:

a) Upstream OFDM channel estimation. The CLT computes the coefficients of the upstream pre-equalizer for each CNU and sends them back to that CNU.
b) Upstream SNR measurement. The CLT measures the SNR per subcarrier and computes the upstream bit loading tables.
c) Upstream timing adjustment. During CNU bring up the CLT may use Wideband Probing to adjust the timing of the new CNU to the upstream RB Frame and superframe.

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102.4.2.2 Probing symbol pilots

Probing symbol pilots are BPSK symbols.

Probing symbol pilot *i* is always associated with the *i*-th subcarrier of the symbol, where:

$i = 0, 1, \ldots, 4095$

NOTE—Subcarriers are numbered in ascending order of frequency starting from 0.

102.4.2.3 Probing symbol scheduling

The CLT may allocate a one or more probing symbols to a CNU within the Probe Period and instruct the CNU to transmit the probing sequence in that symbol. CLT specifies the probing symbol within the Probe Period via the EPoC Probe Control Header message block in the downstream PHY Link frame. The CLT assigns a CNU either all the pilots of the assigned probing symbol, or a subset of (scattered) pilots of the assigned probing symbol.

The CLT allocates subcarriers within a probing symbol by sending five variables to the CNU: *PrbStrtSC*, *PrbSkp*, *PrbEQ*, *StrtSym,* and *SymNum* (see 102.4.2.6.2). Figure 102–24 and Figure 102–25 illustrate the use of *PrbStrtSC* and *PrbSkp*. The CNU uses the *PrbStrtSC* and *PrbSkp* variables to determine which subcarriers are to be used for probing transmission, as follows:

— The *PrbStrtSC* variable is the starting subcarrier number.
— The *PrbSkp* variable is the number of subcarriers to be skipped between successive pilots. *PrbSkp* = 0 implies no skipping of subcarriers (i.e., all subcarriers are used for probing).

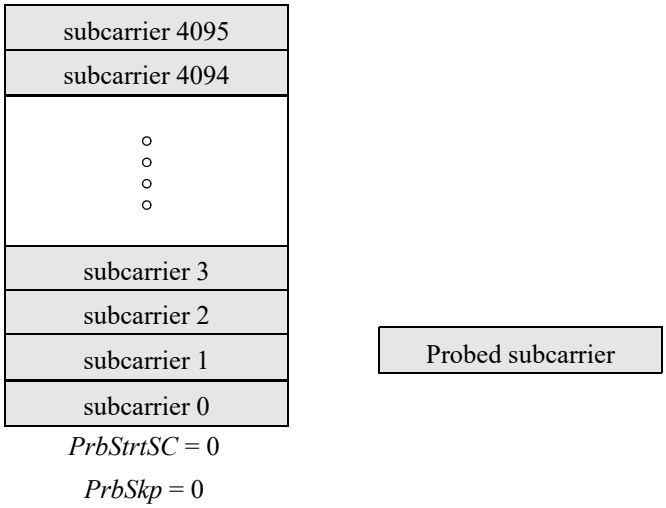

Figure 102–24—Example, all subcarriers used for probing, no skipping

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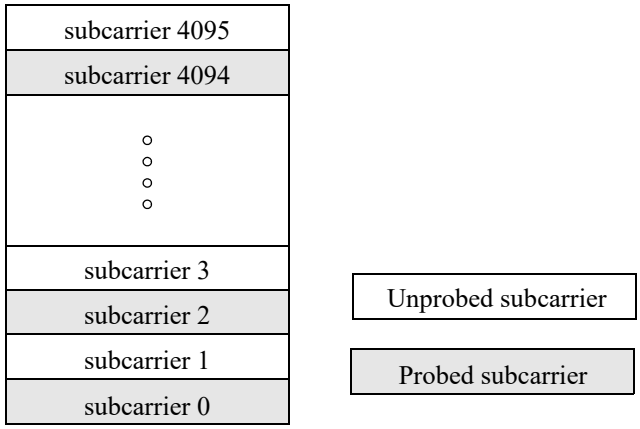

Figure 102–25—Example, alternate subcarriers used for probing

To schedule a single CNU in a probing symbol without skipping subcarriers, the CLT does the following:

- Allocate a specific probing symbol to a single CNU using *StrtSym* and *SymNum*.
- Set *PrbSkp* to zero.
- Set *PrbStrtSC* to the number of the first subcarrier.

To schedule a single CNU in a probing symbol with skipping subcarriers to create nulls (as illustrated in Figure 102–25), the CLT does the following:

- Allocate a specific probing symbol to a single CNU using *StrtSym* and *SymNum*.
- Set *PrbSkp* to a non-zero positive integer value.
- Set *PrbStrtSC* to the number of the first subcarrier.

To schedule multiple CNUs in a probing symbol (as illustrated in Figure 102–26), the CLT does the following:

- Allocate the same probing symbol at any given time to more than one CNU using *StrtSym* and *SymNum*.
- Assign a different *PrbStrtSC* number to each CNU.
- Assign the same *PrbSkp* value to every CNU within the probing symbol.

This method can be used with or without skipping subcarriers to create nulls. To create nulls, specify a *PrbSkp* value equal to, or greater than, the number of CNUs in the pattern.

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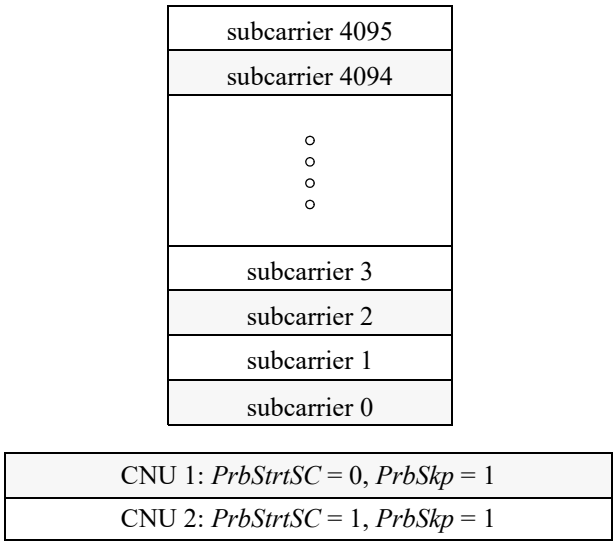

Figure 102–26—Scheduling two CNUs in the same probing symbol

The *PrbEQ* variable determines if the pilots transmitted are to be equalized (*PrbEQ* TRUE) or unequalized (*PrbEQ* FALSE).

StrtSym and *SymNum* variables determine which symbols within the Probe Period are to be used by the CNU. The value of *StrtSym* determines the first symbol within the Probe Period to begin probe transmissions and *SymNum* determines the number of adjacent symbols in which to send probe pilots. The CLT is responsible for properly setting the Probe Control fields so that the probe pilots are defined within the Probe Period. The CNU shall not transmit probe pilots in response to settings which define transmission outside the configured Probe Period. For example if *StrtSym* equals 4 and *SymNum* equals 3 the CNU does not transmit any probe pilots. The CNU is not responsible for crosschecking Probe Control settings to ensure that two CNUs are not assigned the same subcarriers for probing. Should the CLT make such an assignment it will receive a garbled response.

102.4.2.4 Probing sequence

The Probe symbol shall be populated with a BPSK mapped bit sequence generated by a pseudo-random sequence generator defined by the polynomial shown in Equation (102–3) seeded with a fixed bit pattern of 0xBFF at the beginning of each upstream superframe (illustrated in Figure 102–27). The output of the sequence generator is mapped using BPSK modulation (see 101.4.5.2) where a bit value of 0 is mapped to a BPSK value of plus 1 and a bit value of 1 is mapped to a BPSK value of minus 1.

$$x^{12} + x^{9} + x^{8} + x^{5} + 1 \tag{102–3}$$

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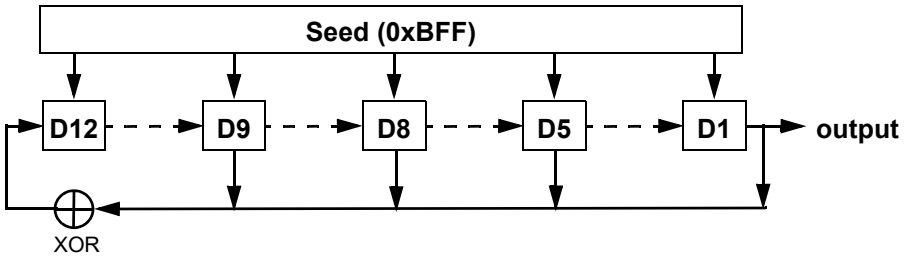

Figure 102–27—Probe sequence generator

102.4.2.5 Probe symbol repetition

Probes use all active subcarriers of a symbol. The first symbol in a Probe is generated as described in 102.4.2.4. The second symbol is a direct copy of the first symbol.

102.4.2.6 Wide Band Probing state diagrams

102.4.2.6.1 Constants

Exclude
: This constant informs the PMA that the subcarrier with which it is associated is not to be used for transmission.

102.4.2.6.2 Variables

ActPrbID
: TYPE: set of 15-bit Integers
When the *CNU_ID* of the CNU is contained in this set of variables the CNU is allowed to transmit a Probe Signal per the Probe Control variable *PrbEQ*, *PrbSkp*, *PrbStrtSC*, *StrtSym,* and *SymNum*. This set of variables is updated with each downstream PHY Link frame when *RF_ID = US_FmCnt* (see Figure 102–29). Each element in this set is one of the *PrbIDs* received in the most recent EPoC Probe Control Header.

CNU_ID
: See 102.3.5.3.

PhyDisc_N (N = 1, 2, ... 16)
: TYPE: 12-bit Integers
Each of these variables designates the starting subcarrier of a PHY Discovery window within the Probe Period.

PrbEQ
: TYPE: Boolean
When this provisioned variable is TRUE, the CNU transmits the probe symbol with equalization applied. When this variable is FALSE, the CNU transmits the probe symbol without equalization applied.

PrbSkp
: TYPE: unsigned integer
The value of this provisioned variable determines the number of subcarriers to be skipped in the probe symbol. The range of *PrbSkp* is from zero to seven.

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PrbStrtSC

TYPE: unsigned integer
The value of this provisioned variable determines the starting subcarrier to be used in the probe symbol. The range of *PrbStrtSC* is from zero to seven.

RcvPrbID

TYPE: set of 15-bit Integers
This set of provisioned variables contains the received set of *PrbID* variables from the most recent downstream PHY Link frame, *PrbID*. When *US_FrmCnt = RF_ID* the values in this set replaces the values in the *ActPrbID* set (see Figure 102–2).

PrbData

TYPE: bit array
This variable holds the probe sequence bits to be transmitted during the Probe Period.

SC_clk

TYPE: Boolean
This clear on read variable goes TRUE at the beginning of each subcarrier.

StrtSym

TYPE: unsigned integer
The value of this variable determines the starting symbol within the Probe Period in which to begin transmitting probe pilots. The range of this variable is from one to six. The sum of *StrtSym* and *SymNum* is less than or equal to six.

SymNum

TYPE: unsigned integer
The value of this variable determines the number of consecutive symbols in which to transmit probe pilots. The range of this variable is from one to six. The sum of *StrtSym* and *SymNum* is less than or equal to six.

US_ModTypeSC(n)

See 101.4.4.4.4 for the definition of these variables.

102.4.2.7 Counters

SC_Cnt

See 102.4.1.9.3.

US_FmCnt

See 102.3.5.2.

102.4.2.8 Functions

Mod(x,y)

This function returns the remainder of *x* divided by *y*.

PrbSeq

This function returns one bit worth of probe data using the sequence generator described in 102.4.2.4. The function is reset at the beginning of the Probe Period.

SndPrbData(x)

This function transfers one symbols worth of Probe data (*PrbData*) from the Probe Symbol Mapper function to the PMA. If *x* = TRUE then the probe data is to be sent with equalization, if *x* = FALSE then probe data is sent without equalization.

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102.4.2.9 State diagrams

The CNU probe transmit process shall conform to the state diagram shown in Figure 102–28.

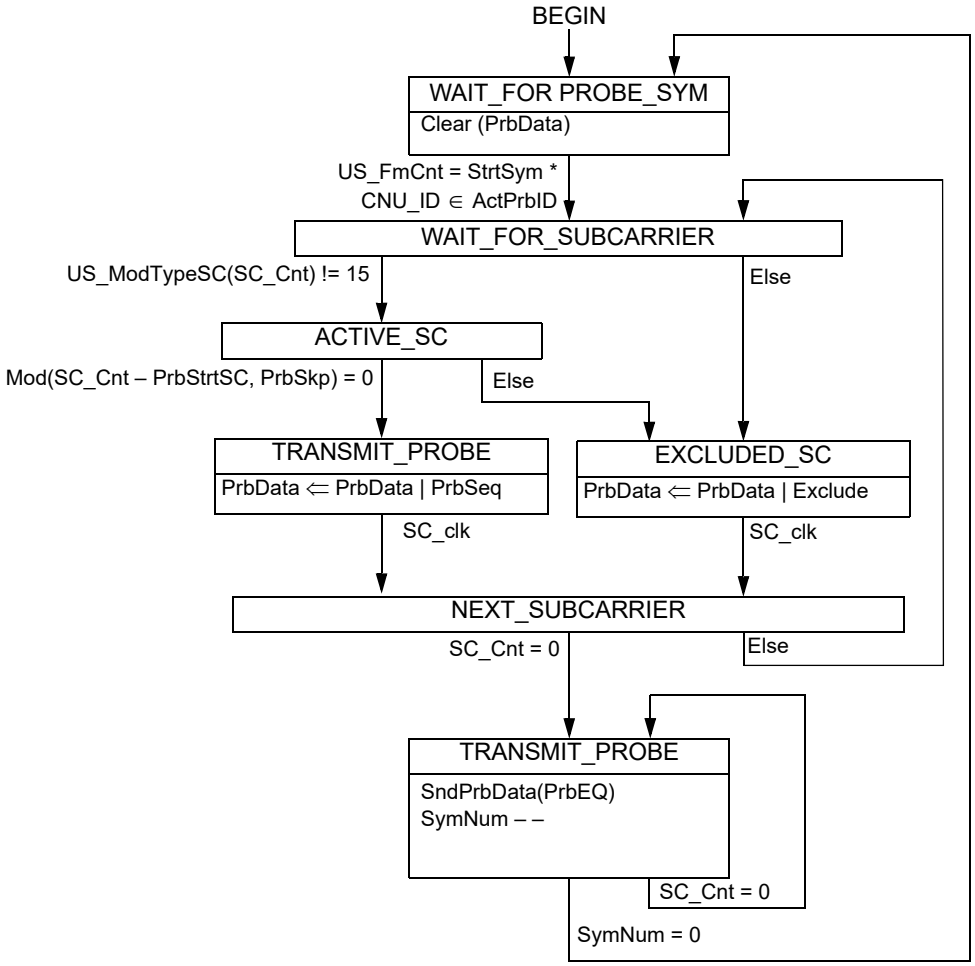

Figure 102–28—CNU Probe transmission control state diagram

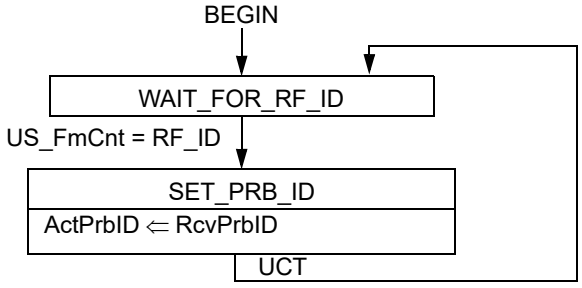

Figure 102–29—PrbID update state diagram

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102.4.3 Link-up declaration

Before declaring a CNU is in the link-up state the CLT shall ensure that a CNU joining the EPoC network is properly aligned to the upstream OFDMA timing and is cognizant of all necessary provisioning parameters needed to properly operate in the OFDMA network without adverse impact to the EPoC network or other services operating in RF spectrum unused by the EPoC network. A list of required parameters is given in Table 102–13.

Once the CLT has verified the CNU is in the link-up status by reading the variables listed in the Link-Up column of Table 102–13 it shall set the *LinkUpRdy* variable to TRUE. Once the CLT has verified the CNU is in the link-up status by reading the *PD_Enable* variable as TRUE it may set the *AssgndCNU_ID* to TRUE to notify the upper layers that the associated CNU_ID has been assigned and a device has been added to the network (see 102.4.1.9.2).

There may exist situations when the CLT requires that a CNU go through the PHY Discovery sequence again. Similarly, there may be situations where a CNU needs to inform the CLT of its desire to leave the EPoC network. The CNU can then go through the PHY Discovery sequence again.

Table 102–13—Required variables for PHY Discovery Response and Link-Up

Variable/Variable Group	Reset on change[a]	Required for[b]	
		PHY Discovery	Link-Up
LinkUpRdy	N		T
PD_Enable	N	T	T
PhyDiscCmplt	N		T
DS_ChCnt	Y		Y
DS_TmIntrlv	Y		Y
DSNrp	Y		Y
DSNcp	Y		Y
DS_FreqCh(1) through *DS_FreqCh(5)* [a]	Y		Y
Rnd	N	Y	Y
RBsize	Y	Y	Y
USNrp	Y	Y	Y
USNcp	Y	Y	Y
US_FreqCh1	Y	Y	Y
Type2_Repeat	N		Y
Type2_Start	N		Y
Type1_Repeat	N		Y
Type1_Start	N		Y
DS_PhyLinkStrt	Y	Y	Y

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Table 102–13—Required variables for PHY Discovery Response and Link-Up *(continued)*

Variable/Variable Group	Reset on change[a]	Required for[b]	
		PHY Discovery	Link-Up
US_PhyLinkStrt	Y	Y	Y
AllwdCNU_ID [c]	Y		Y
PhyTimingOffset	N		Y
PhyPowerOffset	N		Y
PhyRngOffset	Y	Y	Y
DS_DataRate	N	Y	Y
US_DataRate	N	Y	Y
DS_ModAbility	N/A		Y
US_ModAbility	N/A		Y
DS_OFDM_ChAbility	N/A		Y
DS_OFDM_ID [d]	N		Y
PdRespInitPwr	N	Y	Y
PdRespPwrStep	N	Y	Y
DS_ModTypeSC(4) through *DS_ModTypeSC(4095)* [c]	N		Y
US_ModTypeSC(0) through *US_ModTypeSC(4095)*	N	Y	Y
EQ_CoefR(0) through *EQ_CoefR(4095)*	N		Y
EQ_CoefI(0) through E*Q_CoefI(4095)*	N		Y
OFDMA_ClkSync	Y [e]	T	T

[a]Y = a network reset is required before changing this variable, N = this variable can be changed without a network reset, N/A = not applicable.
[b]T = variable is TRUE, Y = variable has been written in the CNU via the PHY Link.
[c]*AllwdCNU_ID* is set using the CNU_ID Allocation special instruction (see 102.4.1.6).
[d]The downstream OFDM descriptor is written for each OFDM channel that contains active subcarriers.
[e]See Table 102–14.

In some instances the CNU may fail to achieve link-up status. This may happen for a number of reasons; for example the CNU may be unable to support the downstream or upstream Profile due to network conditions. In these circumstances the CLT may take mitigating action outside the scope of this standard and attempt to bring up the CNU at a later time.

102.4.4 Link-down declaration

There are three ways to declare a CNU in the Link-down state—CNU PHY self declared, CLT declared, CNU Upper layer declared. These are described in 102.4.4.1 through 102.4.4.3.

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102.4.4.1 CNU PHY self declared link-down

If any of the conditions listed in Table 102–14 become TRUE the CNU shall declare itself to be link-down and sets *LinkUpRdy*, *PhyDiscComplete,* and *PD_Enable* to FALSE. If subsequent analysis indicates the device is ready to re-join the EPoC network, as described in 102.4.1 it may do so by going through the normal discover process.

Table 102–14—Link-down causal conditions

Condition	Description
CNU OFDM Clock misaligned	|Received Timestamp – *LocalTS*| > 10
DS PHY Link loss of frame	Unable to decode the DS PHY Link frame for three or more consecutive frames
Change in DS OFDM channel count	Any provisioned change to *DS_ChCnt*
Change in DS time interleaver	Any provisioned change to *DS_TmrIntrlv*
Change of cyclic prefix length	Any provisioned change to *DSNcp* or *USNcp*
Change of OFDM channel frequency	Any provisioned change to *DS_FreqCh(1), DS_FreqCh(1), DS_FreqCh(2), DS_FreqCh(3), DS_FreqCh(4), DS_FreqCh(5) or US_FreqCh1*
Change of Resource Block size	Any provisioned change to RBsize
Change of Pilot structure	Any provisioned change to *Type2_Repeat, Type2_Start, Type1_Repeat* or *Type1_Start*
Change of PHY Link	Any provisioned change to *DS_PhyLinkStrt* or *US_PhyLnkStrt*
Change of PHY ranging offset	Any provisioned change to *PhyRngOffset*

102.4.4.2 CLT declared link-down

The CLT may declare a CNU to be in a link-down state by setting *PhyDiscComplete* to FALSE. It may further force the CNU to reassess its readiness for participation on the network by setting *PD_Enable* and *LinkUpRdy* to FALSE.

102.4.4.3 Upper layer declared link-down

The upper layers may declare a CNU to be in a link-down state by setting *PhyDiscComplete* to FALSE. It may further force the CNU to reassess its readiness for participation on the network by setting *PD_Enable* and *LinkUpRdy* to FALSE.

102.4.5 OFDM Profile descriptors

In the EPoC upstream and downstream link the OFDM profile is defined by the *DS_ModTypeSC(n)* and *US_ModTypeSC(n)* variables, respectively. Two copies of each profile variable set exist—an active copy and an inactive copy. During a profile switch (see 102.2.3.1) the network switches operation from the currently active profile to the inactive profile. Note that for the downstream profile there are five OFDM channels; the channel referred to by the *DS_ModTypeSC(n)* variable set is determined by the *DS_OFDM_ID* variable.

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The currently active profile can be copied to the inactive profile via a profile copy. This is controlled via the *DS_PrflCpy*, *DS_CpyCh*, and *US_PrflCpy* variables. While the copy is in process, as indicated by the *DS_CpyInP* and *US_CpyInP* variables profile switches are prohibited and profile writes are ignored.

To update the entire downstream profile in an EPoC network that includes all five downstream OFDM channels the CLT first sets the *DS_OFDM_ID* variable to one then updates the changed *DS_ModTypeSC(n)* variables for the first OFDM channel. The CLT then proceeds to update the second OFDM channel by changing *DS_OFDM_ID* to two followed by any updates to the *DS_ModTypeSC(n)* variables for the second channel. This continues until all five OFDM channels have been updated. The final action the CLT takes is to update the *DS_CID* (see 102.2.3.1.1) to switch from the current active profile to the profile copy that was just updated by the above actions. The above description is an example only; the CLT need not update the downstream profile in its entirety nor in any particular order before the *DS_CID* switch.

102.4.5.1 PHY Link managed variables

DS_CpyCh

TYPE: 3-bit unsigned integer
This variable identifies which of the five downstream OFDM channel profiles (profile 1 to 5) is to be copied into the downstream profile variables.

DS_CpyInP

TYPE: Boolean
When set to a TRUE, this variable indicates that a copy of the currently active downstream profile to the inactive profile is in process. Note that while this variable has a value of TRUE writes to all downstream profile variables shall be ignored and switching between profiles is prohibited. This variable is set to FALSE by the PMA/PMD when the copy is completed.

DS_PrflCpy

TYPE: Boolean
When this variable is set to TRUE, a copy of the currently active downstream profile to the inactive profile is initiated. Once initiated this action continues to completion (i.e., it cannot be interrupted or aborted once initiated). This variable is set to FALSE by the PHY on or before completion of the profile copy.

US_CpyInP

TYPE: Boolean
When set to a TRUE, this variable indicates that a copy of the currently active upstream profile to the inactive profile is in process. Note that while this variable has a value of TRUE writes to all upstream profile variables shall be ignored and switching between profiles is prohibited. This variable is set to FALSE by the PMA/PMD when the copy is completed.

US_PrflCpy

TYPE: Boolean
When this variable is set to TRUE, a copy of the currently active upstream profile to the inactive profile is initiated. Once initiated this action continues to completion (i.e., it cannot be interrupted or aborted once initiated). This variable is set to FALSE by the PHY on or before completion of the profile copy.

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102.5 Protocol implementation conformance statement (PICS) proforma for Clause 102, EPoC PHY Link[176]

102.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 102, EPoC PHY Link, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

102.5.2 Identification

102.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

102.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 102, EPoC PHY Link
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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102.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
PL	PHY Link supported	102.1.1	For both upstream and downstream directions	M	Yes [ ] No [ ]

102.5.4 PICS proforma tables for EPoC PHY Link

102.5.4.1 PHY Link general specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PG1	Profile activation	102.2.3.1.1	CLT sets an identical inactive profile in all active CNU prior to its activation.	CLT:M	Yes [ ] No [ ] N/A [ ]
PG2	Profile switching	102.2.3.1.1	Once started completes	CLT:M	Yes [ ] No [ ] N/A [ ]
PG3	Transmission prerequisites	102.4.1.2	Meets the requirements of Table 102–13	CNU: M	Yes [ ] No [ ] N/A [ ]
PG4	Link-up declaration	102.4.3	CLT verifies requirements of Table 102–7 are met	CLT:M	Yes [ ] No [ ] N/A [ ]
PG5	Link-down declaration	102.4.4.1	Link-down declared by setting *PhyDiscComplete* and *PD_Enable* to FALSE if any conditions in Table 102–14 are TRUE	CNU: M	Yes [ ] No [ ] N/A [ ]
PG6	PHY Link scrambler	102.1.5	Meets the requirements of Figure 101–21	M	Yes [ ] No [ ]
PG7	CLT PHY Link scrambler initialization	102.1.5	At the beginning of the first OFDM symbol following the PHY Link preamble	CLT: M	Yes [ ] No [ ] N/A [ ]
PG8	CNU PHY Link scrambler initialization	102.1.5	At the beginning of an upstream PHY Link transmission	CNU: M	Yes [ ] No [ ] N/A [ ]
PG9	PHY Link preamble	102.1.5	Is not scrambled	M	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PG10	DS PHY Link modulation	102.1.6	16-QAM	M	Yes [ ] No [ ]
PG11	US PHY Link modulation	102.1.6	16-QAM or higher	M	Yes [ ] No [ ]

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102.5.4.2 PHY Link timing

Item	Feature	Subclause	Value/Comment	Status	Support
PT1	CLT *LocalTS* sync	102.2.7.2	Tracks transmit clock	CLT:M	Yes [ ] No [ ] N/A [ ]
PT2	CNU *LocalTS* sync	102.2.7.2	Tracks receive clock	CNU: M	Yes [ ] No [ ] N/A [ ]
PT3	*LocalTS* updates	102.2.3.1.4	*LocalTS* set to received timestamp when *PD_Enable* is FALSE	CNU: M	Yes [ ] No [ ] N/A [ ]
PT4	US OFDMA timing adjustment	102.4.1.6	Upon receipt PhyTimingOffset added to *LocalTS*	CNU: M	Yes [ ] No [ ] N/A [ ]
PT5	PHY Link response time	102.2.3.1.2	CLT ensures CNU has sufficient time to respond to DS PHY Link EMB	CNU: M	Yes [ ] No [ ] N/A [ ]
PT6	DS PHY Link response time	102.2.5	4.8 ms maximum	M	Yes [ ] No [ ]
PT7	EPoC Probe Control Header response time	102.2.3.2	Within 2.5 ms maximum	M	Yes [ ] No [ ]

102.5.4.3 Downstream framing

Item	Feature	Subclause	Value/Comment	Status	Support
DF1	DS PHY Link frame length	102.1.1	128 OFDM symbols	M	Yes [ ] No [ ]
DF2	DS Preamble	102.2.2	Meets the fixed pattern in Table 102–4 modulated with BPSK in the first 8 symbols of the DS Frame	M	Yes [ ] No [ ]
DF3	DS PHY Link Type field	102.2.3	As listed in Table 102–6	M	Yes [ ] No [ ]
DF4	DS PHY Link CRC	102.2.3	CNU rejects data if calculated and received CRC do not match	CNU: M	Yes [ ] No [ ] N/A [ ]
DF5	DS PHY Link DA	102.2.3.1.3	As listed in Table 102–8	CLT:M	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DF7	DS PHY Link OPCODE	102.2.3.3	As listed in Table 102–10	CLT:M	Yes [ ] No [ ] N/A [ ]
DF8	DS timestamp reference	102.2.3.1.4	first sample of the PHY Link symbol immediately following the Preamble per Figure 102–11	CLT:M	Yes [ ] No [ ] N/A [ ]

102.5.4.4 DS Encoding and transmission

Item	Feature	Subclause	Value/Comment	Status	Support
DET1	DS PHY Link FEC	102.2.4	(384,288) binary punctured LDPC code described in 102.1.4.1 and 102.1.4.3.1	M	Yes [ ] No [ ]
DET2	DS PHY Link bit mapping	102.2.1.3	Meets the requirements of Figure 102–8	M	Yes [ ] No [ ]
DET3	DS PHY Link interleaving	102.2.1.3	Meets the requirements of Figure 102–9	M	Yes [ ] No [ ]
DET4	DS PHY Link transmit process	102.2.7.5	Meets the requirements of Figure 102–15	CLT:M	Yes [ ] No [ ] N/A [ ]

102.5.4.5 Downstream OFDM

Item	Feature	Subclause	Value/Comment	Status	Support
DO1	DS PHY Link spectrum allocation	102.2.1.1	400 kHz	M	Yes [ ] No [ ]
DO2	DS PHY Link surrounding spectrum	102.2.1.1	24 MHz contiguous, with at lease 3 MHz above and below the PHY Link allocations	M	Yes [ ] No [ ]
DO3	DS PHY Link symbol	102.2.1.1	Same CP duration and windowing size as downstream data	M	Yes [ ] No [ ]

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102.5.4.6 Upstream encoding and transmission

Item	Feature	Subclause	Value/Comment	Status	Support
UET1	US PHY Link FEC	102.3.3	(384,288) binary punctured LDPC code described in 102.1.4.1 and 102.1.4.3.1	M	Yes [ ] No [ ]
UET2	US PHY Link transmit process	102.3.5.5	Meets the requirements of Figure 102–17	CNU: M	Yes [ ] No [ ] N/A [ ]

102.5.4.7 Upstream framing

Item	Feature	Subclause	Value/Comment	Status	Support
UF1	US PHY Link frame length	102.1.1	262 OFDM symbols	M	Yes [ ] No [ ]
UF2	US PHY Link Type field	102.3.2	As listed in Table 102–6	CNU: M	Yes [ ] No [ ] N/A [ ]
UF3	US PHY Link CRC	102.3.2	CCL rejects data if calculated and received CRC do not match	CLT:M	Yes [ ] No [ ] N/A [ ]
UF4	US PHY Link addressing	102.3.2.2	CNU responds to unicast downstream PHY Link messages if DA equals *CNU_ID*	CNU: M	Yes [ ] No [ ] N/A [ ]

102.5.4.8 Upstream OFDM

Item	Feature	Subclause	Value/Comment	Status	Support
UO1	US PHY Link spectrum allocation	102.3.1.1	400 kHz	CLT:M	Yes [ ] No [ ] N/A [ ]
UO2	US PHY Link symbol	102.3.1.1	Same CP duration and windowing size as upstream data	CNU: M	Yes [ ] No [ ] N/A [ ]
UO3	US PHY Link modulation	102.3.1.2	Meets the requirements of Table 100–2 per column “PHY Link CNU Tx/CLT Rx”	M	Yes [ ] No [ ]

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102.5.4.9 Communication Protocol

Item	Feature	Subclause	Value/Comment	Status	Support
CP1	US PHY Link ACK	102.3.2.2	As listed in Table 102–11	M	Yes [ ] No [ ]
CP2	US PHY Link NACK	102.3.2.2	Variable Group Count field set to zero and is ignored at receiver	M	Yes [ ] No [ ]
CP3	US PHY Link NACK data	102.3.2.2	Variable Group Data fields ignored if not omitted at CLT	CLT:M	Yes [ ] No [ ] N/A [ ]
CP4	DS EMB discrepancy	102.2.3.3	No action if Variable Group Count field disagrees with the number of 16-bit Variable Group Data fields, NACK returned	CNU:M	Yes [ ] No [ ] N/A [ ]

102.5.4.10 PHY Discovery

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	PHY Discovery Response FEC	102.4.1.4	(128,80) binary punctured LDPC code described in 102.1.4.3.2	M	Yes [ ] No [ ]
PD2	PHY Discovery preamble	102.4.1.5	BPSK modulated 128-bit sequence generated per Figure 102–22	M	Yes [ ] No [ ]
PD3	PHY Discovery preamble symbol	102.4.1.5	Second symbol duplicate of first per Figure 102–21	M	Yes [ ] No [ ]
PD4	CNU_ID allocation	102.4.1.6	Per Table 102–12	M	Yes [ ] No [ ]
PD5	CNU Discover Response	102.4.1.9.5	Per Figure 102–23	M: CNU	Yes [ ] No [ ] N/A [ ]

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102.5.4.11 Probes

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	Probe data	102.4.2.4	BPSK modulated sequence generated per Figure 102–27	CNU: M	Yes [ ] No [ ] N/A [ ]
PR2	Probe transmissions	102.4.2.3	No probe transmission outside configured Probe Period	CNU: M	Yes [ ] No [ ] N/A [ ]
PR3	Probe transmit process	102.4.2.9	Meets the requirements of Figure 102–28	CNU: M	Yes [ ] No [ ] N/A [ ]

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103. Multipoint MAC Control for EPoC

103.1 Overview

This clause deals with the mechanism and control protocols required in order to reconcile the EPoC (EPON protocol over coax) into the Ethernet framework. The P2MP medium is a coax cable distribution network (CCDN) in which passive and active elements are present in the signal's path from source to destination. When combined with the EPON protocol, such a network is referred to as EPON protocol over coax network (EPoC).

P2MP is an asymmetric medium based on a tree (or tree-and-branch) topology. The DTE connected to the trunk of the tree is called cable line terminal (CLT) and the DTEs connected at the branches of the tree are called cable network units (CNU). The CLT typically resides at the service provider's facility, while the CNUs are located at the subscriber premises.

The EPoC topology is similar to the P2MP topology of EPON with the optical line terminal being replaced by a CLT, the optical network units replaced by CNU and operating over a coaxial network rather than an optical network.

A simplified P2MP topology example is depicted in Figure 103–1.

Topics dealt with in this clause include allocation of upstream transmission resources to different CNUs, discovery and registration of CNUs into the network, and reporting of congestion to higher layers to allow for dynamic bandwidth allocation schemes and statistical multiplexing across the CCDN.

This clause does not deal with topics including bandwidth allocation strategies, authentication of end-devices, quality-of-service definition, provisioning, or management.

This clause specifies the multipoint control protocol (MPCP) to operate a coax cable distribution network by defining a Multipoint MAC Control sublayer as an extension of the MAC Control sublayer defined in Clause 31, and supporting current and future operations as defined in Clause 31 and annexes.

Each CCDN consists of a node located at the root of the tree assuming the role of CLT, and multiple nodes located at the tree leaves assuming roles of CNUs. The network operates by allowing CNUs multiplexed in frequency and in time to share the upstream medium. The MPCP located at the CLT is responsible for timing the different transmissions. Reporting of congestion by the different CNUs may assist in optimally allocating the bandwidth across the CCDN.

Automatic discovery of end stations is performed, culminating in registration through binding of a CNU to a CLT port by allocation of a Logical Link ID (see LLID 76.2.6.1.3.2), and dynamic binding to a MAC connected to the CLT.

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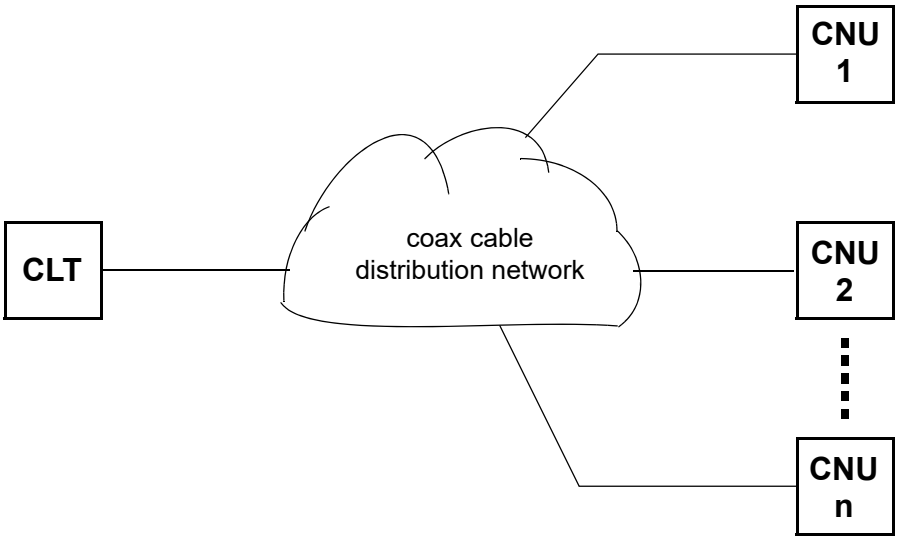

Figure 103–1—Coax cable distribution network topology example

The Multipoint MAC Control functionality shall be implemented for subscriber access devices containing point-to-multipoint Physical Layer devices defined in Clause 100, Clause 101, and Clause 102.

The EPoC Multipoint MAC Control shares much in common with the Multipoint MAC Control protocol defined in Clause 64 and Clause 77. There are a number of variables, constants and functions that are complementary to those defined for EPON Multipoint MAC Control but that are unique to EPoC. These are listed in Table 103–1.

Table 103–1—Complementary constants, variables, and functions between EPON and EPoC

Clause 77	Clause 103
guardThresholdOLT	*guardThresholdCLT*
guardThresholdONU	*guardThresholdCNU*
laserOffTime	*rfOffTime*
laserOnTime	*rfOnTime*
tqSize	*qSizeC*
fecOffset	*fecOffsetC*
OctetsRemaining	*OctetsRemainingC*
ResetBound	*ResetBoundC*
CheckGrantSize	*CheckGrantSizeC*
packet_initiate_timer	*packet_initiate_timerC*
effectiveLength	*effectiveLengthC*
minGrantLength	*minGrantLengthC*
rndDlyTmr	*rndDlyTmrC*

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103.1.1 Position of Multipoint MAC Control within the IEEE 802.3 hierarchy

The Multipoint MAC Control in this clause defines the MAC control operation for point-to-multipoint networks over coaxial cable distribution networks. Figure 103–2 depicts the architectural positioning of the Multipoint MAC Control sublayer with respect to the MAC and the MAC Control client. The Multipoint MAC Control sublayer takes the place of the MAC Control sublayer to extend it to support multiple clients and additional MAC control functionality.

Multipoint MAC Control is defined using the mechanisms and precedents of the MAC Control sublayer. The MAC Control sublayer has extensive functionality designed to manage the real-time control and manipulation of MAC sublayer operation. This clause specifies the extension of the MAC Control mechanism to manipulate multiple underlying MACs simultaneously. This clause also specifies a specific protocol implementation for MAC Control.

The Multipoint MAC Control sublayer is specified such that it can support new functions to be implemented and added to this standard in the future. MultiPoint Control Protocol (MPCP), the management protocol for P2MP is one of these protocols. Non-real-time, or quasi-static control (e.g., configuration of MAC operational parameters) is provided by Layer Management. Operation of the Multipoint MAC Control sublayer is transparent to the MAC.

As depicted in Figure 103–2, the layered system instantiates multiple MAC entities, using a single Physical Layer. The individual MAC instances offer a point-to-point emulation service between the CLT and the CNU. An additional MAC is instantiated to communicate to all EPoC CNUs at once. This instance takes maximum advantage of the broadcast nature of the downstream channel by sending a single copy of a frame that is received by all EPoC CNUs. This MAC instance is referred to as Single Copy Broadcast (SCB).

The CNU only requires one MAC instance since frame filtering operations are done at the RS layer before reaching the MAC. Therefore, MAC and layers above are emulation-agnostic at the CNU.

Although Figure 103–2 and supporting text describe multiple MACs within the CLT, a single unicast MAC address may be used by the CLT. Within the EPoC Network, MACs are uniquely identified by their LLIDs, which are dynamically assigned by the registration process.

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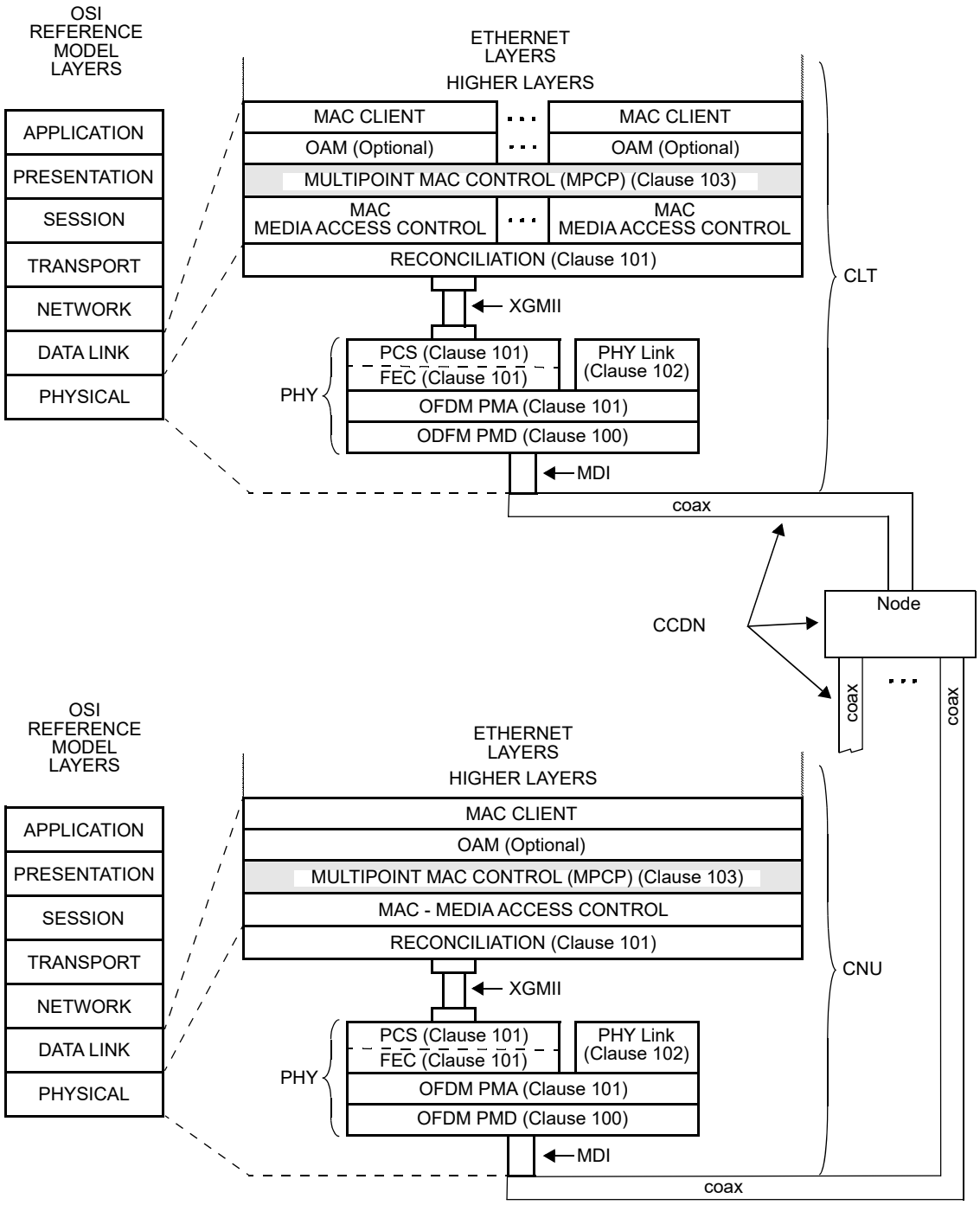

XGMII= 10 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
CCDN= COAX CABLE DISTRIBUTION NETWORK
CLT = COAXIAL LINE TERMINAL
CNU = COAXIAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 103–2—Relationship of Multipoint MAC Control and the OSI protocol stack for EPoC

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103.1.2 Functional block diagram

Figure 103–3 provides a functional block diagram of the Multipoint MAC Control architecture.

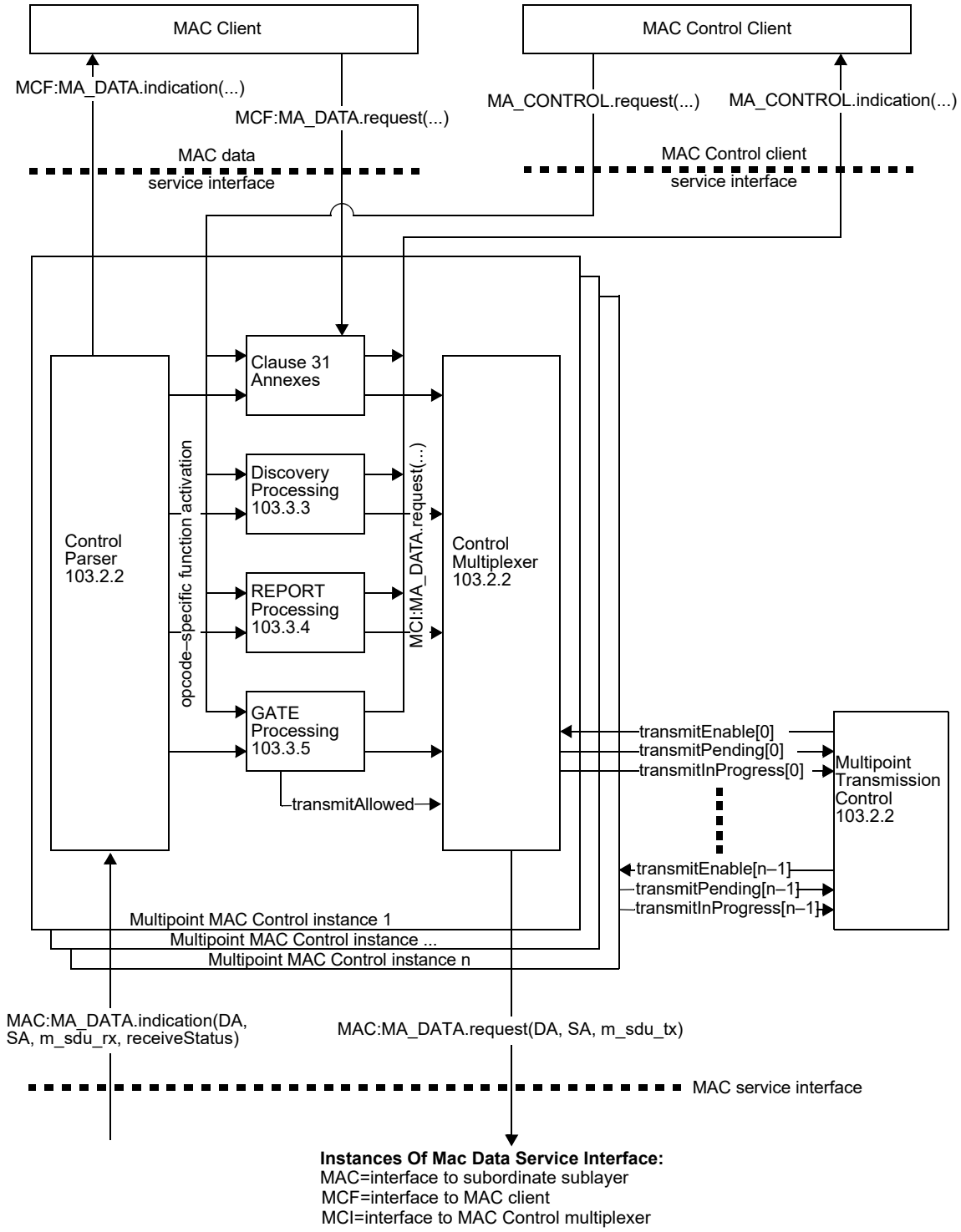

Figure 103–3—Multipoint MAC Control functional block diagram

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103.1.3 Service interfaces

See 77.1.4.

103.1.4 State diagram conventions

The body of this standard comprises state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2 augmented as follows:

a) [start x_timer, y] sets expiration of y to timer x_timer.

b) [stop x_timer] aborts the timer operation for x_timer asserting x_timer_not_done indefinitely.

The state diagrams use an abbreviation MACR as a shorthand form for MA_CONTROL.request and MACI as a shorthand form for MA_CONTROL.indication.

The vector notations used in the state diagrams for bit vector use 0 to mark the first received bit and so on (for example data[0:15]), following the conventions of 3.1 for bit ordering. When referring to an octet vector, 0 is used to mark the first received octet and so on (for example m_sdu[0..1]).

a < b: A function that is used to compare two (cyclic) time values. Returned value is TRUE when b is larger than a allowing for wrap around of a and b. The comparison is made by subtracting b from a and testing the MSB. When MSB(a – b) = 1 the value TRUE is returned, else FALSE is returned. In addition, the following functions are defined in terms of a < b:
a > b is equivalent to !(a < b or a = b)
a ≥ b is equivalent to !(a < b)
a ≤ b is equivalent to !(a > b)

103.1.5 Other conventions

For equations used in this clause the symbol $\lceil x \rceil$ represents a ceiling function that rounds up its argument x to the next highest integer; in pseudo code listing the term ceiling() is used for this function. The symbol $\lfloor x \rfloor$ represents a floor function that rounds down its argument x to the next lowest integer.

103.2 Multipoint MAC Control operation

As depicted in Figure 103–3, the Multipoint MAC Control functional block contains functions very similar to those found in Clause 77. In EPoC the CLT replaces the OLT and the CNU replaces the ONU. Significant differences are noted in 103.2.1 through 103.2.2.

103.2.1 Principles of Multipoint MAC Control

The principles of Multipoint MAC Control are the same as those described in 77.2.1 for EPON.

103.2.1.1 Ranging and timing process

The ranging and timing processes for EPoC are the same as those described in 77.2.1.1 for EPON.

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103.2.2 Multipoint transmission control, Control Parser, and Control Multiplexer

The purpose and high level functionality of multipoint transmission control is similar to those described in 77.2.2 for EPON. Detailed differences are noted in the definitions below and in Figure 103–3 through Figure 103–13.

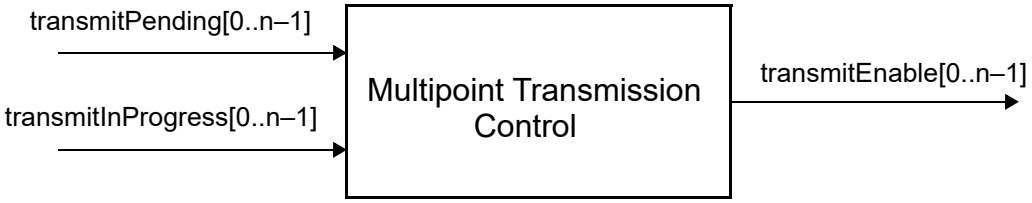

Figure 103–4—Multipoint Transmission Control service interfaces

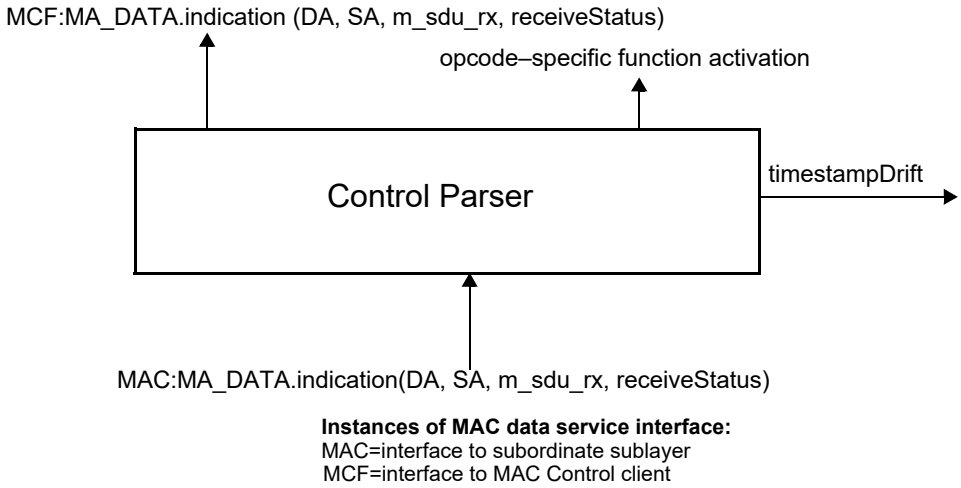

Figure 103–5—Control Parser service interfaces

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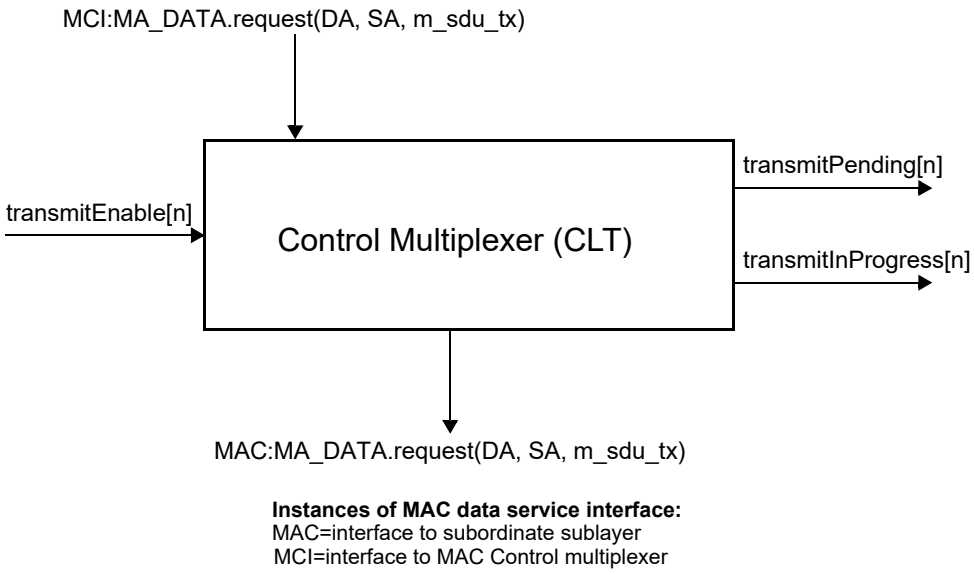
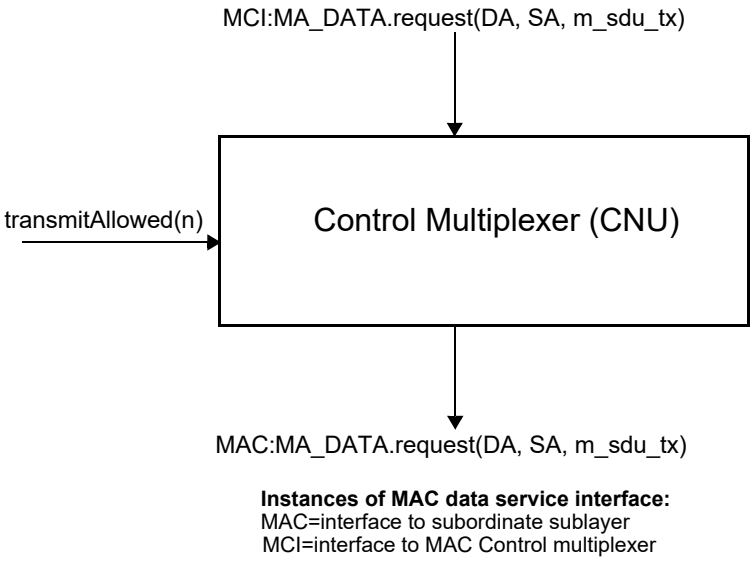


NOTE—MAC:MA_DATA.request primitive may be issued from multiple MAC Control processing blocks.

Figure 103–6—CLT Control Multiplexer service interfaces



NOTE—MAC:MA_DATA.request primitive may be issued from multiple MAC Control processing blocks.

Figure 103–7—CNU Control Multiplexer service interfaces

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103.2.2.1 Constants

DS_FEC_CW_Sz
: TYPE: unsigned integer
This constant represents the integer number of octets in the FEC codeword and is equal to the sum of *DS_FEC_Pld_Sz* and *DS_FEC_Prty_Sz*.
VALUE: 1987

DS_FEC_CW_Sz_FRAC
: TYPE: real number
This constant represents the exact size of the FEC codeword expressed in units of octets.
VALUE: 1760 + 2944/13 or 1760 + (1840 × 64/65/8)

DS_FEC_Prty_Sz
: TYPE: unsigned integer
This constant represents the size of FEC codeword parity field in units of octets.
VALUE: 227

DS_FEC_Pld_Sz
: TYPE: unsigned integer
This constant represents the size of FEC codeword payload in units of octets.
VALUE: 1760 (220 block of 64 bits as seen from the MAC Table 101–2)

guardThresholdCLT
: TYPE: unsigned integer
This constant holds the maximum amount of drift allowed for a *timestamp* received at the CLT. This value is measured in units of *time_quantum*.
VALUE: 12

guardThresholdCNU
: TYPE: unsigned integer
This constant holds the maximum amount of drift allowed for a *timestamp* received at the CNU. This value is measured in units of *time_quantum*.
VALUE: 8

MAC_Control_type
: TYPE: unsigned integer
The value of the Length/Type field as defined in 31.4.1.3.
VALUE: 0x8808

tailGuard
: TYPE: unsigned integer
This constant holds the value used to reserve space at the end of the upstream transmission at the CNU in addition to the size of last MAC service data unit (m_sdu) in units of octets. Space is allocated for the MAC overheads including: preamble, SFD, DA, SA, Length/Type, FCS, and minimum interpacket gap. The sizes of the above listed MAC overhead items are described in 3.1.1. The size of the minimum IPG is described in 4A.4.2.
VALUE: 38

time_quantum
: This constant is defined in 64.2.2.1 and is 16 ns.

XGMII_Rate
: TYPE: unsigned integer
See 101.3.2.1.1.

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103.2.2.2 Counters

localTime

TYPE: 32-bit unsigned integer
This counter is defined in 77.2.2.2 and holds the value of the local timer used to control MPCP operation.

103.2.2.3 Variables

BEGIN

TYPE: Boolean
This variable is used when initiating operation of the functional block state diagram. It is set to TRUE following initialization and every reset.

data_rx

TYPE: bit array
This variable is defined in 77.2.2.3 and represents a 0-based bit array corresponding to the payload of a received MPCPDU.

data_tx

TYPE: bit array
This variable is defined in 77.2.2.3 and represents a 0-based bit array corresponding to the payload of an MPCPDU being transmitted.

fecOffsetC

TYPE: 32-bit unsigned integer
A variable that advances by one after every octet time. In the CLT, after reaching the value of *DS_FEC_CW_Sz*, this variable is held for a period of time for PMD derating and then reset to zero as illustrated in Figure 103–8. In the CNU, this variable is assigned in Figure 103–13.

fecPldSz

TYPE: integer
fecPldSz is an alias for *DS_FEC_Pld_Sz.*

grantStart

TYPE: Boolean
This variable is defined in 77.2.2.3 and indicates beginning of a grant transmission.

IdleGapCount

TYPE: 32-bit unsigned integer
This variable defined in 77.2.2.3 represents length of gap between subsequent frames, expressed in the unit of octet time and advances by 1 after every 8-bit times.

initial_derating_delay

TYPE: 24 bit unsigned integer
This variable is used to set the time-out interval for *derating_timer* defined in 103.2.2.5 expressed in units of octets.

newRTT

TYPE: 16-bit unsigned integer
This variable is defined in 77.2.2.3 and temporarily holds a newly-measured Round Trip Time.

m_sdu_rx

TYPE: bit array
This varible is defined in 77.2.2.3 and is equal to the concatenation of the Length/Type and *data_rx* variables.

m_sdu_tx

TYPE: bit array

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This variable is defined in 77.2.2.3 and is equal to the concatenation of the Length/Type and *data_tx* variables.

m_sdu_ctl

TYPE: bit array
This varible is defined in 77.2.2.3 and is equal to the concatenation of the *MAC_Control_type* and *data_tx* variables.

Octet_CLK

TYPE: Boolean
This clear on read Boolean value is TRUE for every octet time period, i.e., the amount of time used to transmit one octet in 10Gb/s MAC data rate.

OctetsRemainingC

TYPE: 32-bit unsigned integer
This variable is an alias for the expression (((*stopTime* – *localTime*) × *tqSizeC*/128) – *tqOffset*). It denotes the number of octets that can be transmitted between the current time and the end of the grant.

OctetsRequired

TYPE: 16-bit unsigned integer
This variable is defined in 77.2.2.3 and represents a total transmission time of next packet and is used to check whether the next packet fits in the remainder of the transmission window. The value of *OctetsRequired* includes packet transmission time, *tailGuard* defined in 103.2.2.1, and FEC parity data overhead expressed in units of octets.

opcode_rx

TYPE: 16-bit unsigned integer
This variable is defined in 77.2.2.3 and holds an opcode of the last received MPCPDU.

opcode_tx

TYPE: 16-bit unsigned integer
This variable is defined in 77.2.2.3 and holds an opcode of an outgoing MPCPDU.

packet_initiate_delay

TYPE: 18-bit unsigned integer
This variable is defined in 77.2.2.3 and used to set the time-out interval for *packet_initiate_timerC* defined in 103.2.2.5 expressed in units of octets.

PCS_DS_Rate

See 101.3.2.1.2 and Equation (101–2).

ResetBoundC

TYPE: 32-bit unsigned integer
This variable represents the value of *DelayBound* (see 101.3.2.1.2) expressed in units of octet time (i.e., *ResetBoundC* = 8 × *DelayBound*).

RTT

TYPE: 16-bit unsigned integer
This variable is defined in 77.2.2.3 and holds the measured Round Trip Time to the CNU expressed in units of *time_quanta*.

stopTime

TYPE: 32-bit unsigned integer
This variable is defined in 77.2.2.3 and holds the value of the *localTime* counter corresponding to the end of the nearest grant.

timestamp

TYPE: 32-bit unsigned integer

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This variable is defined in 77.2.2.3 and holds the value of *timestamp* of the last received MPCPDU frame.

timestampDrift

TYPE: Boolean
This variable is defined in 77.2.2.3 and used to indicate whether an error is signaled as a result of uncorrectable *timestamp* drift.

tqOffset

TYPE: 8-bit unsigned integer
This variable is defined in 77.2.2.3 and denotes the offset (in octet times) of the current actual time from the *localTime* variable.

tqSizeC

TYPE: unsigned integer
This variable represents the number of octets that can be transmitted in 128 *time_quantum* units, i.e., 2048 ns.

transmitAllowed

TYPE: Boolean
This variable is defined in 77.2.2.3 and used to control PDU transmission at the CNU.

transmitEnable

TYPE: Boolean array
This array is defined in 77.2.2.3 and used to control the transmit path in the Multipoint MAC Control instance at the CLT.

transmitInProgress

TYPE: Boolean array
This array is defined in 77.2.2.3 and indicates that the Multipoint MAC Control instance is in a process of transmitting a frame.

transmitPending

TYPE: Boolean array
This array is defined in 77.2.2.3 and indicates that a Multipoint MAC Control instance is ready to transmit a frame.

103.2.2.4 Functions

abs(n)

This function returns the absolute value of the parameter *n*.

Opcode–specific function(opcode)

These functions are defined in 77.2.2.4 and exported from *opcode* specific blocks that are invoked on the arrival of a MAC Control message of the appropriate *opcode*.

CheckGrantSizeC(length)

This function calculates the future time at which the transmission of the current frame (including the FEC parity overhead) is completed.

```
Function CheckGrantSizeC( length ){
   GntSize = 0;
   length += fecOffsetC;
   while (length > fecPldSz[0]) {      // Calc # of full Lg CW's
      length -= fecPldSz[0];
      GntSize += DS_FEC_CW_Sz_FRAC[0];
   }
   // Calc remaining 1 part Lg CW <OR> 2 Med CW
   // (2 full <OR> 1 full & 1 part) <OR> 1 Sm CW (full <OR> part)
```


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```
    while (length > 0) {
       if (length > 6464) {
          GntSize += length + ceiling(length/64) + fecPrtySz[0];
       }
       else if (length >= fecPldSz[1]) {   // full Med CW
          GntSize += DS_FEC_CW_Sz_FRAC[1];
       }
       else if (length >= 1600) {          // partial Med CW
       GntSize += length + ceiling(length/64) + fecPrtySz[1];
       }
       else if (length >= fecPldSz[2]) {   // full Small CW
          GntSize += DS_FEC_CW_Sz_FRAC[2];
       }
       else {                              // partial Small CW
          GntSize += length + ceiling(length/64) + fecPrtySz[2];
       }
    }
    return GntSize - fecOffsetC;
}
```

PHY_Overhead(length)

This function calculates the additional amount of time (in octet times) that the MPCP control multiplexer waits following transmission of a frame of size *length* by the MAC. The additional time is added to allow the insertion of parity data into the frame by the PHY layer and to adjust the data rate to the effective data rate supported by the PCS and PMD. PHY_Overhead() returns the number of octets that the PHY inserts during transmission of a particular packet. Parameter *length* represents the size of an entire frame including preamble, SFD, DA, SA, Length/Type, FCS, and IPG, which are accounted for in *tailGuard*. The following formula is used to calculate the overhead:

$$PMD\_Overhead(length) =$$

$$FEC\_Overhead(length) + Derating\_Overhead(length, \frac{XGMII\_Rate}{PCS\_DS\_Rate})$$

$$FEC\_Overhead(length) = 12 + DS\_FEC\_Prty\_Sz \times \left\lfloor \frac{fecOffset + length}{DS\_FEC\_Pld\_Sz} \right\rfloor$$

$$Derating\_Overhead(length) =$$

$$\left\lceil \left(\frac{XGMII\_Rate}{PCS\_DS\_Rate} - 1 \right) \times DS\_FEC\_CW\_Sz\_FRAC \times \left\lfloor \frac{fecOffset + length}{DS\_FEC\_Pld\_Sz} \right\rfloor \right\rceil$$

select()

This function is defined in 77.2.2.4 and selects the next Multipoint MAC Control instance allowed to initiate transmission of a frame. The function returns an index to the *transmitPending* array for which the value is not FALSE. The selection criteria in the presence of multiple active elements in the list is implementation-dependent.

SelectFrame()

This function is defined in 77.2.2.4 and enables the interface that has a pending frame. If multiple interfaces have frames waiting at the same time, only one interface is enabled. The selection criteria is not specified, except for the case when some of the pending frames have

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Length/Type = MAC_Control. In this case, one of the interfaces with a pending MAC Control frame shall be enabled.

sizeof(sdu)
: This function is defined in 77.2.2.4 and returns the size of the *sdu* in octets.

transmissionPending()
: This function is defined in 77.2.2.4 and returns TRUE if any of the Multipoint MAC Control instances has a frame waiting to be transmitted.

103.2.2.5 Timers

derating_timer:
: This timer is used to suspend the advancing of *fecOffsetC* in order to derate the MAC frame transmission to be able to match the PMD rate.

packet_initiate_timerC
: This timer is used to delay frame transmission from MAC Control to avoid variable MAC delay while MAC enforces IPG after a previous frame. In addition, this timer increases inter-frame spacing just enough to accommodate the extra parity data to be added by the FEC encoder.

103.2.2.6 Messages

MAC:MA_DATA.indication(DA, SA, m_sdu, receiveStatus)
: The service primitive is defined in 31.3.

MCF:MA_DATA.indication(DA, SA, m_sdu, receiveStatus)
: The service primitive is defined in 31.3.

MAC:MA_DATA.request (DA, SA, m_sdu)
: The service primitive is defined in 31.3. The action invoked by this service primitive is not considered to end until the transmission of the frame by the MAC has concluded. The ability of the MAC control layer to determine this is implementation-dependent.

MCF:MA_DATA.request (DA, SA, m_sdu)
: The service primitive is defined in 31.3.

103.2.2.7 State diagrams

The Multipoint transmission control function in the CLT shall implement state diagrams shown in Figure 103–8 and Figure 103–9. Control parser function in the CLT shall implement the state diagram shown in Figure 103–10. Control parser function in the CNU shall implement the state diagram shown in Figure 103–11. Control multiplexer function in the CLT shall implement the state diagram shown in Figure 103–12. Control multiplexer function in the CNU shall implement the state diagram shown in Figure 103–13.

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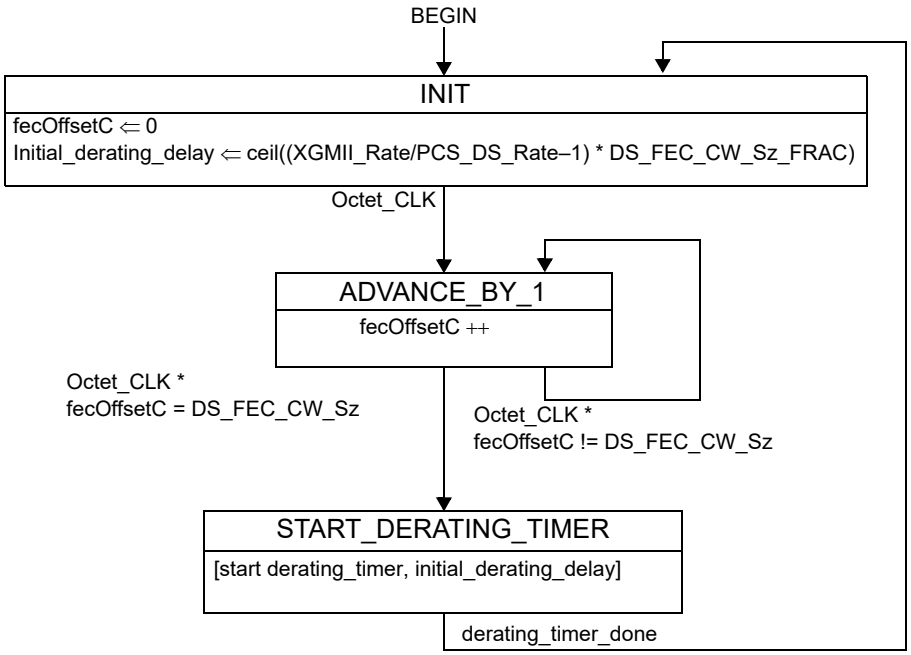

Figure 103–8—CLT fecOffsetC state diagram

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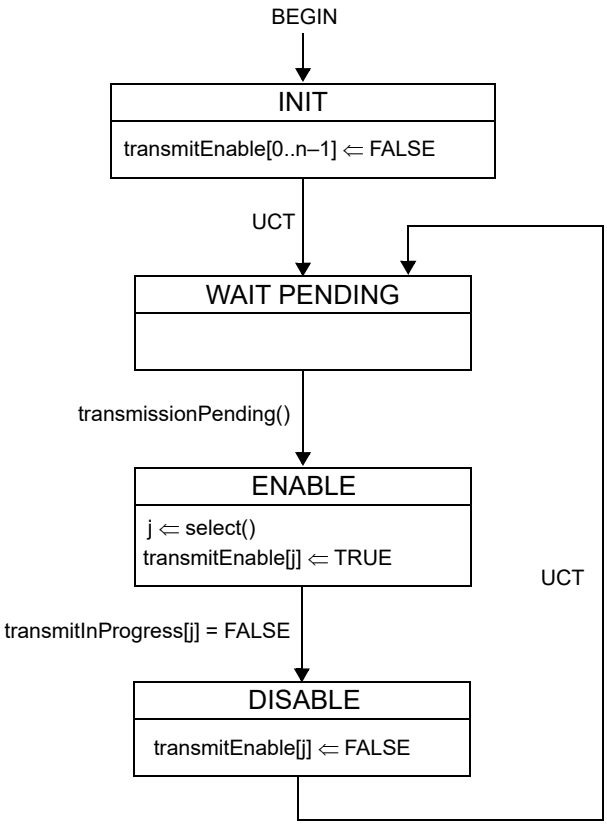

Figure 103–9—CLT Multipoint Transmission Control state diagram

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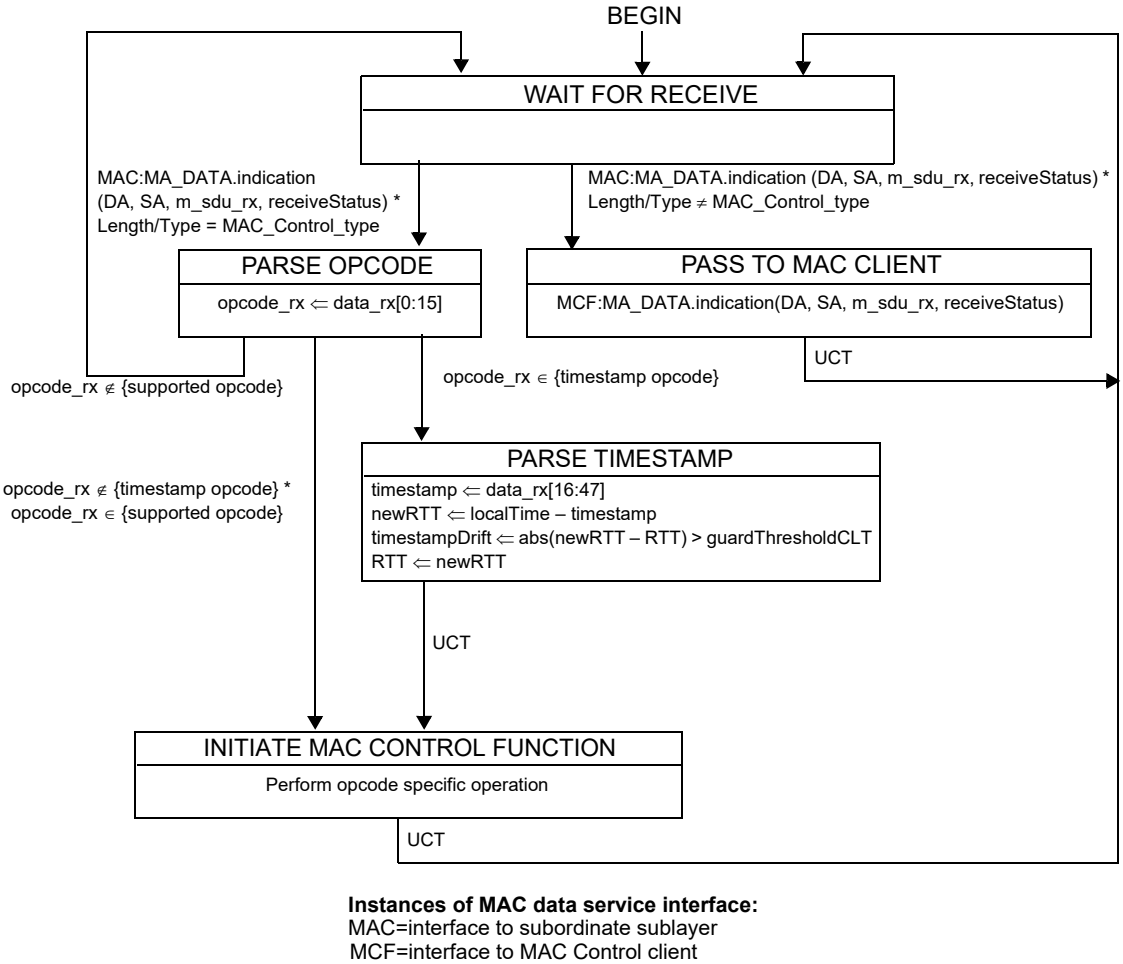

NOTE—The opcode–specific operation is launched as a parallel process by the MAC Control sublayer, and not as a synchronous function. Progress of the generic MAC Control Receive state diagram (as shown in this figure) is not implicitly impeded by the launching of the opcode specific function.

Refer to Annex 31A for list of supported opcodes and timestamp opcodes.

Figure 103–10—CLT Control Parser state diagram

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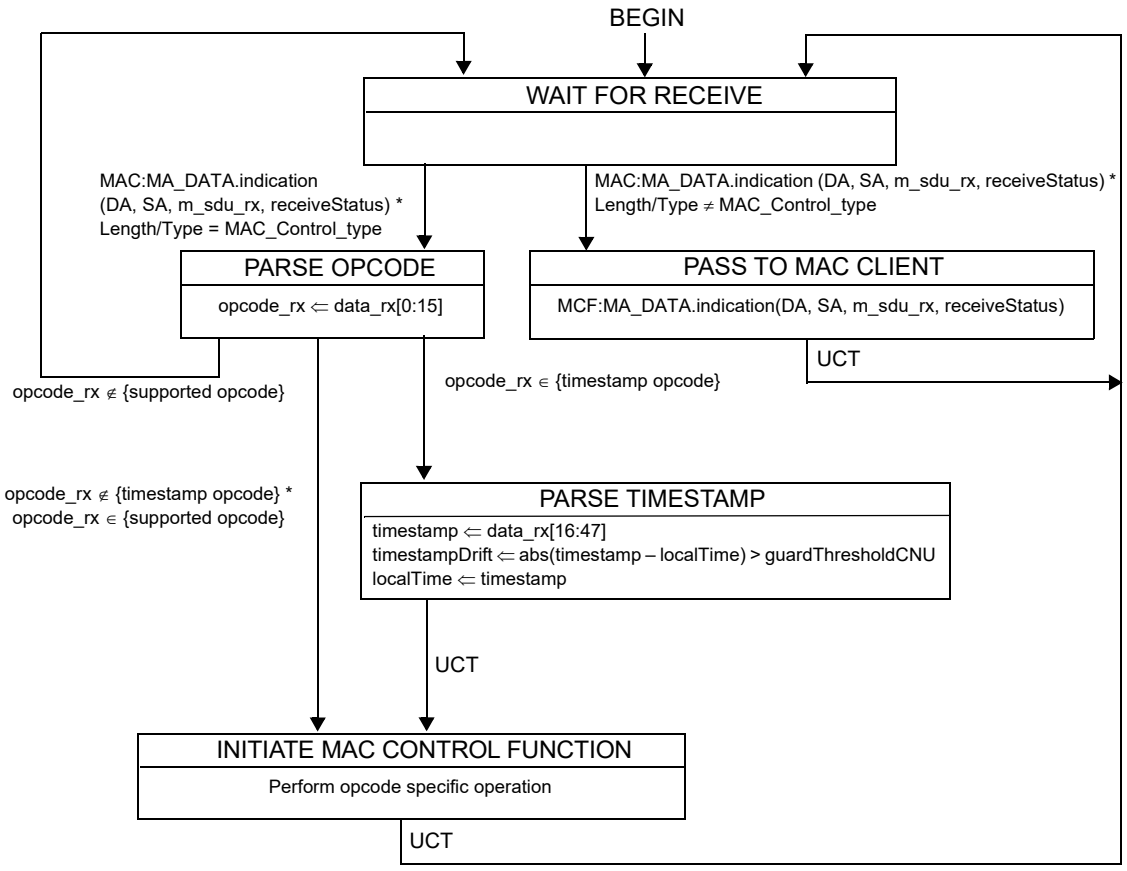

Instances of MAC data service interface:
MAC=interface to subordinate sublayer
MCF=interface to MAC Control client

NOTE—The opcode–specific operation is launched as a parallel process by the MAC Control sublayer, and not as a synchronous function. Progress of the generic MAC Control Receive state diagram (as shown in this figure) is not implicitly impeded by the launching of the opcode specific function.

Refer to Annex 31A for list of supported opcodes and timestamp opcodes.

Figure 103–11—CNU Control Parser state diagram

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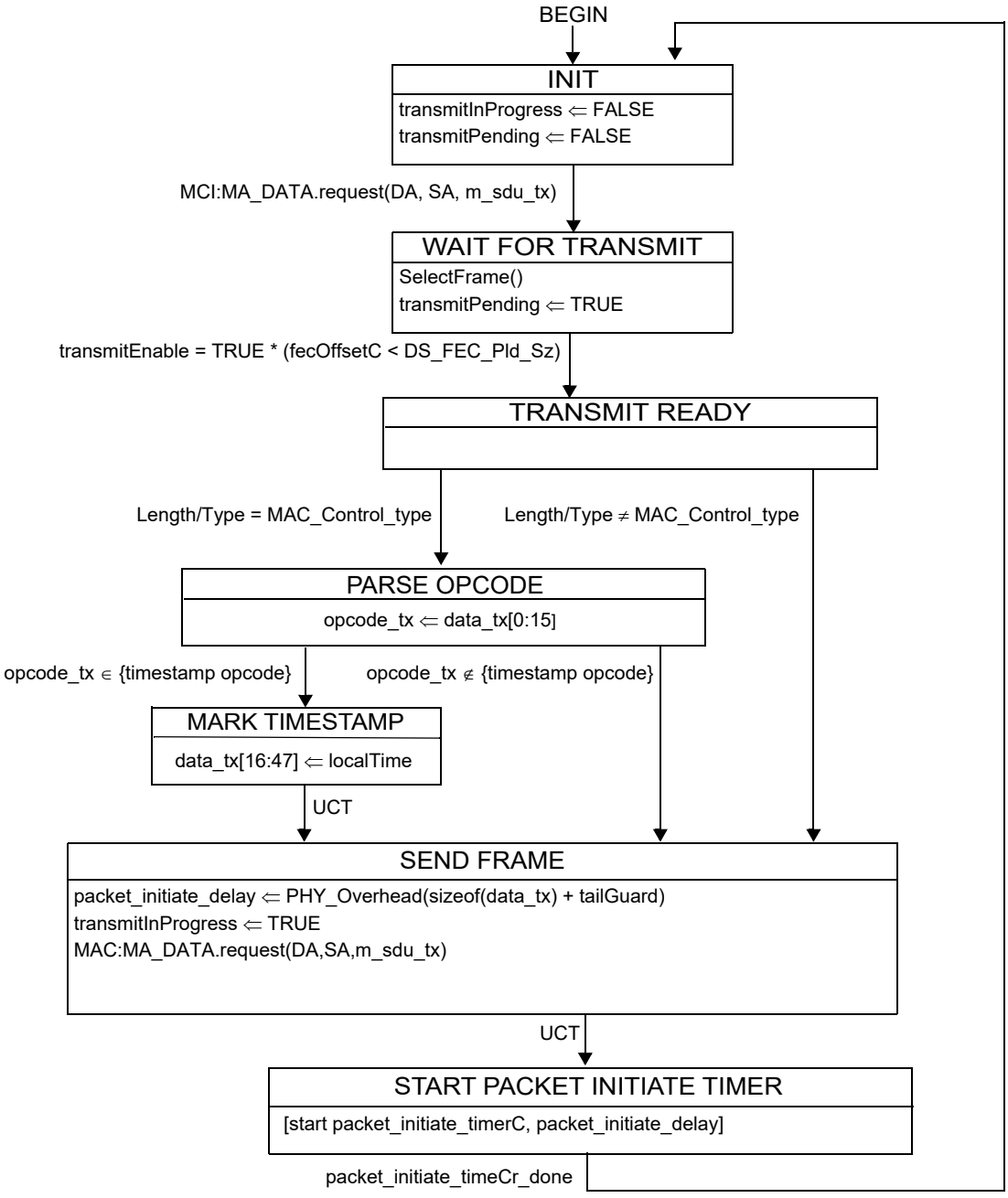

Instances of MAC data service interface:
MAC=interface to subordinate sublayer
MCI=interface to MAC Control multiplexer

Figure 103–12—CLT Control Multiplexer state diagram

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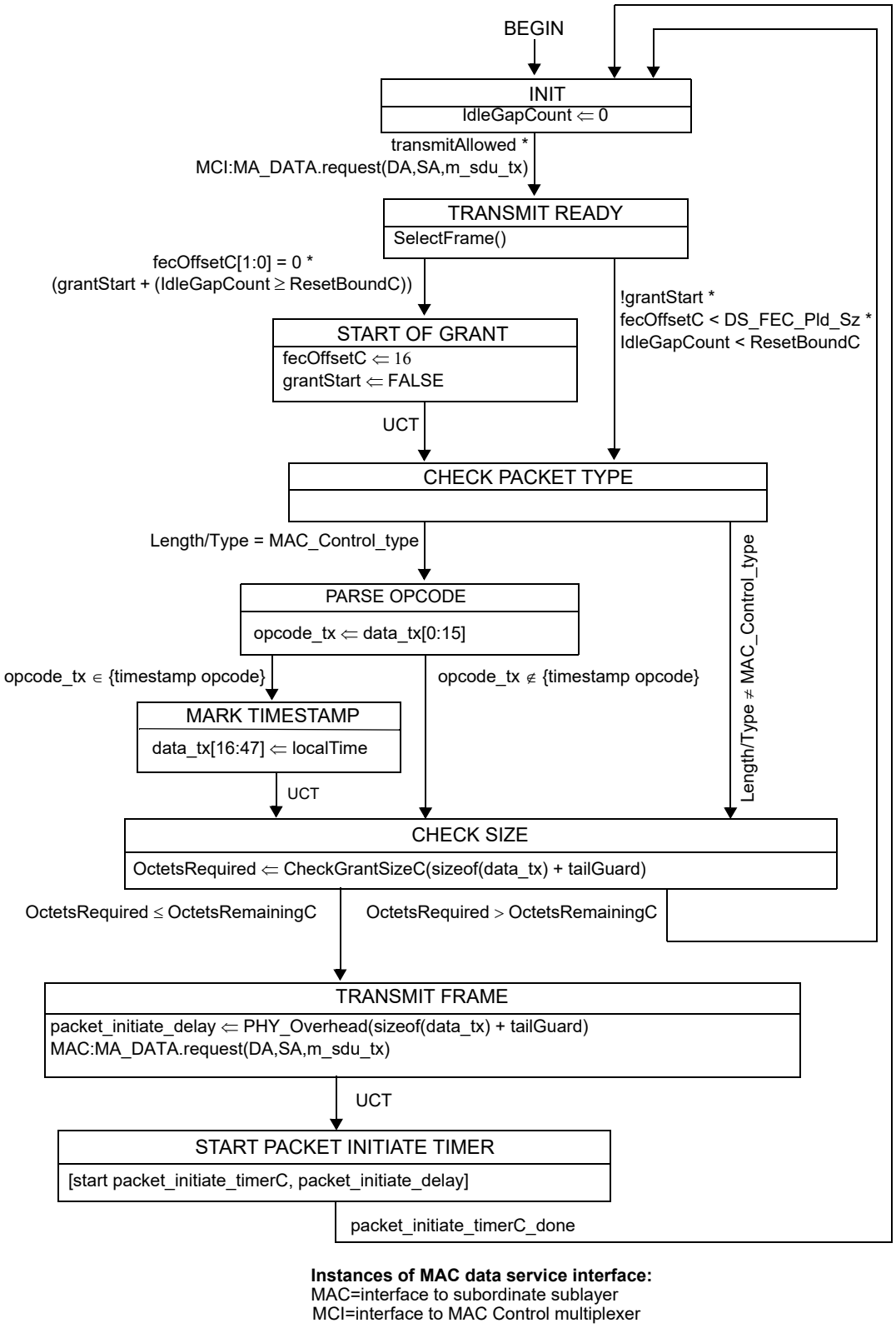

Figure 103–13—CNU Control Multiplexer state diagram

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103.3 Multipoint Control Protocol (MPCP)

As depicted in Figure 103–3, the Multipoint MAC Control functional block comprises nearly the same functions and layering system as that described in 77.3. In EPoC the CLT replaces the OLT and the CNU replaces the ONU. All other significant differences are noted in 103.3.1 through 103.3.6.

103.3.1 Principles of Multipoint Control Protocol

The principles of the Multipoint Control Protocol are the same as those found in 77.3.1 except the EPoC system uses an Orthogonal Frequency Division Multiple Access (OFDMA) method in the upstream direction. In EPON the Multipoint Control Protocol, one and only one MAC is allowed to transmit at any given time. In EPoC the Multipoint Control Protocol allows multiple MACs to transmit in any given time but coincident transmitters are separated in frequency.

103.3.2 Compatibility considerations

103.3.2.1 PAUSE operation

See 77.3.2.1 and time constraints found at 103.3.2.4.

103.3.2.2 Optional Shared LAN emulation

Optional Shared LAN emulation for EPoC is the same as described in 77.3.2.2.

103.3.2.3 Multicast and single copy broadcast support

Multicast and single copy broadcast support in EPoC is the same as described in 77.3.2.3.

103.3.2.4 Delay requirements

The MPCP protocol relies on strict timing based on distribution of timestamps. A compliant implementation needs to guarantee a constant delay through the MAC and PHY in order to maintain the correctness of the timestamping mechanism. The actual delay is implementation-dependent; however, a complying implementation shall maintain a delay variation of no more than 1 *time_quantum* through the MAC.

The CLT shall not issue a gate message more than 1024 *time_quanta* into the future. The CNU shall process all messages in less than this period. The CLT shall not issue more than one message every 1024 *time_quanta* to a single CNU. The unit of *time_quantum* is defined in 64.2.2.1. The CLT shall ensure that a minimum gap time between bursts from any two CNUs equal to *RB_time_quanta* [see Equation (101–33)].

103.3.3 Discovery processing

Discovery processing in the EPoC is the same as described in 77.3.3 with the following exceptions. In EPoC, CNUs that have not completed PHY Discovery process (see 102.4.1) will not respond to Discovery GATE MPCPDUs. In the EPoC coax cable distribution network only one upstream data rate is allowed for a given configuration. The *laserOnTime* and *laserOffTime* parameters in 77.3.3 are replaced in EPoC with *rfOnTime* and *rfOffTime*, respectively.

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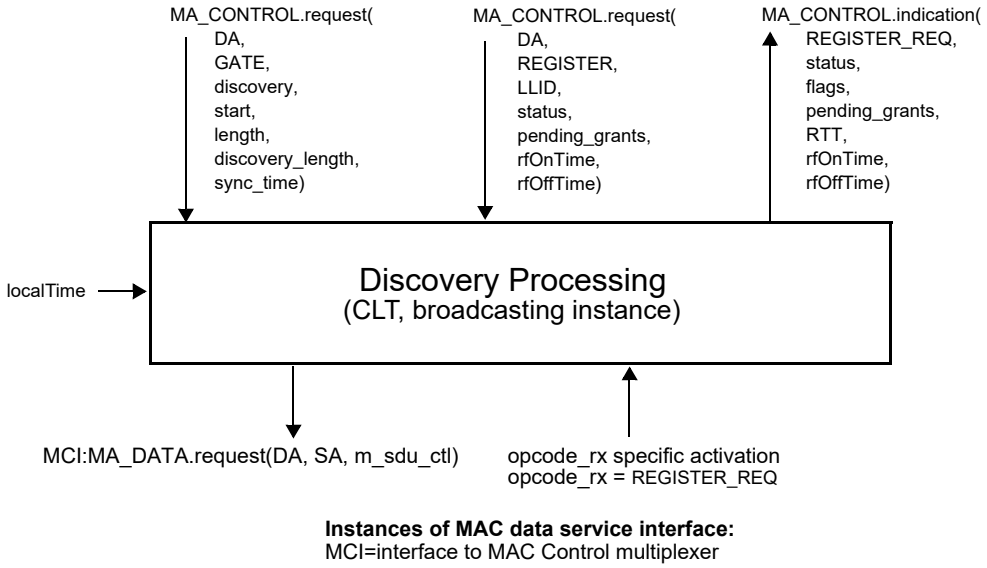

Figure 103–14—Discovery Processing service interfaces (CLT, broadcast instance)

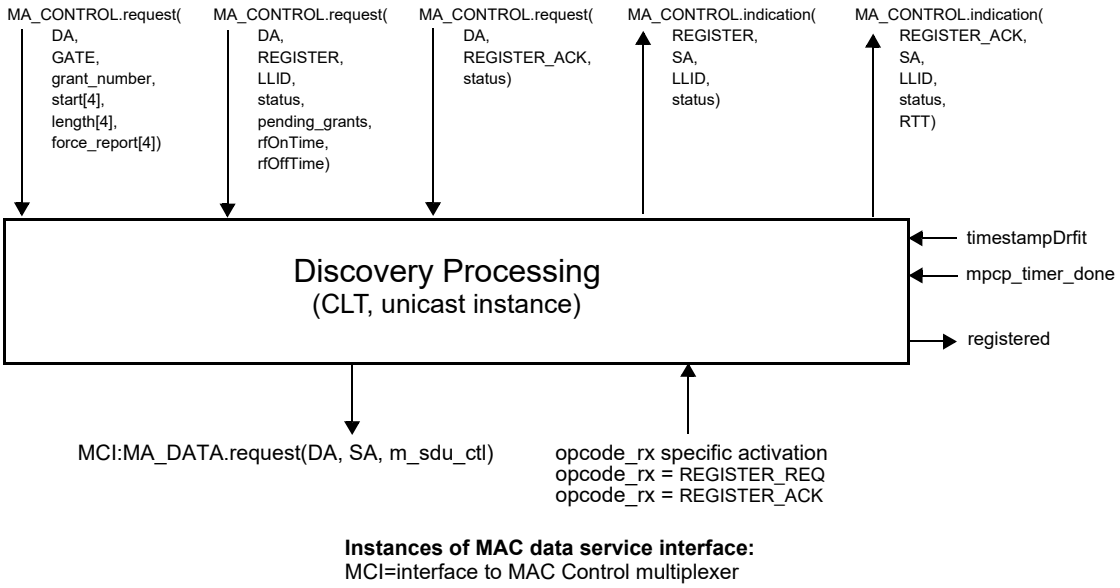

Figure 103–15—Discovery Processing service interfaces (CLT, unicast instance)

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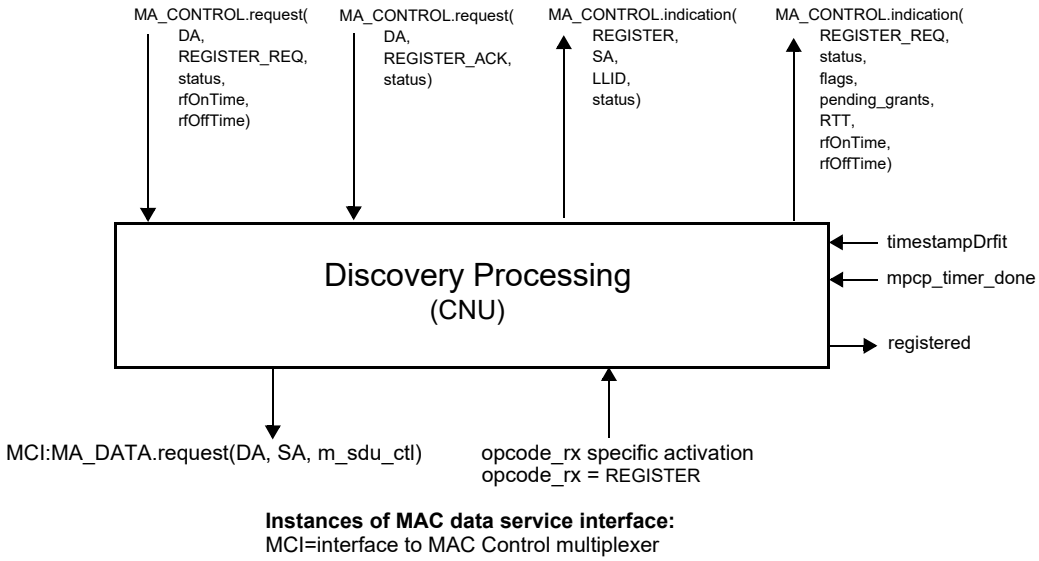

Figure 103–16—Discovery Processing service interfaces (CNU)

103.3.3.1 Constants

rfOffTime

TYPE: 8-bit unsigned integer
This variable holds the time required to terminate the RF and is included for consistency with Clause 77.
VALUE: zero

rfOnTime

TYPE: 8-bit unsigned integer
This variable holds the time required to initiate the PMD and is included for consistency with Clause 77.
VALUE: zero

103.3.3.2 Variables

BEGIN

This variable is defined in 103.2.2.3.

data_rx

This variable is defined in 103.2.2.3.

data_tx

This variable is defined in 103.2.2.3.

grantEndTime

TYPE: 32-bit unsigned integer
This variable is defined in 77.3.3.2 and holds the time at which the CLT expects the CNU grant to complete.

insideDiscoveryWindow

TYPE: Boolean
This variable is defined in 77.3.3.2 and holds the current status of the discovery window.

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localTime
: This variable is defined in 103.2.2.2.

m_sdu_ctl
: This variable is defined in 103.2.2.3.

opcode_rx
: This variable is defined in 103.2.2.3.

pendingGrants
: TYPE: 16-bit unsigned integer
This variable is defined in 77.3.3.2 and holds the maximum number of pending grants that a CNU is able to queue.

registered
: TYPE: Boolean
This variable is defined in 77.3.3.2 and holds the current result of the Discovery Process.

RB_time_quanta
: See Equation (101–33).

syncTime
: TYPE: 16-bit unsigned integer
This variable is defined in 77.3.3.2 and holds the time required to stabilize an EPON receiver at the OLT (see 76.3.2.5.3). The EPoC CLT OFDMA receiver is synchronized and stabilized during PHY Discovery and does not use a synchronization preamble as part of the upstream burst (see Figure 101–10). This variable is present to maintain compatibility with the EPON MPCP and always has a value of zero in EPoC PHYs.

timestampDrift
: This variable is defined in 103.2.2.3.

103.3.3.3 Timers

discovery_window_size_timer
: This timer is defined in 77.3.3.4 and used to wait for the event signaling the end of the discovery window.

mpcp_timer
: This timer is defined in 77.3.3.4 and used to measure the arrival rate of MPCP frames in the link.

103.3.3.4 Messages

MA_DATA.indication(DA, SA, m_sdu, receiveStatus)
: This service primitive is defined in 2.3.2.

MA_DATA.request (DA, SA, m_sdu)
: This service primitive is defined in 2.3.2.

MA_CONTROL.request(DA, GATE, discovery, start, length, discovery_length, sync_time)
: This service primitive is used by the MAC Control client at the CLT to initiate the Discovery Process. This primitive takes the following parameters:

DA:	Multicast or unicast MAC address.
GATE:	Opcode for GATE MPCPDU as defined in Table 31A–1.
discovery:	Flag specifying that the given GATE message is to be used for discovery only.
start:	Start time of the discovery window.
length:	Length of the grant given for discovery.

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discovery_length: Length of the discovery window process.
sync_time: The time interval required to stabilize the receiver at the CLT.

MA_CONTROL.request(DA, GATE, grant_number, start[4], length[4], force_report[4])

This service primitive is used by the MAC Control client at the CLT to issue the GATE message to a CNU. This primitive takes the following parameters:

DA: Multicast MAC Control address as defined in Annex 31B.
GATE: Opcode for GATE MPCPDU as defined in Table 31A–1.
grant_number: Number of grants issued with this GATE message. The number of grants ranges from 0 to 4.
start[4]: Start times of the individual grants. Only the first grant_number elements of the array are used.
length[4]: Lengths of the individual grants. Only the first grant_number elements of the array are used.
force_report[4]: Flags indicating whether a REPORT message should be generated in the corresponding grant. Only the first grant_number elements of the array are used.

MA_CONTROL.request(DA,REGISTER_REQ,status,*rfOnTime*,*rfOffTime*)

This service primitive is used by a client at the CNU to request the Discovery Process to perform a registration. This primitive takes the following parameters:

DA: Multicast MAC Control address as defined in Annex 31B.
REGISTER_REQ: opcode for REGISTER_REQ MPCPDU as defined in Table 31A–1.
status: This parameter takes on the indication supplied by the flags field in the REGISTER_REQ MPCPDU as defined in Table 77–3.
rfOnTime: This parameter holds the *rfOnTime* value, expressed in units of *time_quanta*, as reported by MAC client and specified in 103.3.6.3.
rfOffTime: This parameter holds the *rfOffTime* value, expressed in units of *time_quanta,* as reported by MAC client and specified in 103.3.6.3.

MA_CONTROL.indication(REGISTER_REQ, status, flags, pending_grants, *RTT*, *rfOnTime*, *rfOffTime*)

The service primitive is issued by the Discovery Process to notify the client and Layer Management that the registration process is in progress. This primitive takes the following parameters:

REGISTER_REQ: Opcode for REGISTER_REQ MPCPDU as defined in Table 31A–1.
status: This parameter holds the values incoming or retry. Value incoming is used at the CLT to signal that a REGISTER_REQ message was received successfully. The value retry is used at the CNU to signal to the client that a registration attempt failed and needs to be repeated.
flags: This parameter holds the contents of the flags field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the CLT.
pending_grants: This parameter holds the contents of the pending_grants field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the CLT.
RTT: The measured round trip time to/from the CNU is returned in this parameter. *RTT* is stated in *time_quanta* units. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the CLT.
rfOnTime: This parameter holds the contents of the *rfOnTime* field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the CLT.
rfOffTime: This parameter holds the contents of the *rfOffTime* field in the REGISTER_REQ message. This parameter holds a valid value only when the primitive is generated by the Discovery Process in the CLT.

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MA_CONTROL.request(DA, REGISTER, LLID, status, pending_grants, *rfOnTime*, *rfOffTime*)

The service primitive is used by the MAC Control client at the CLT to initiate acceptance of a CNU. This primitive takes the following parameters:

DA: Unicast MAC address or multicast MAC Control address as defined in Annex 31B.

REGISTER: Opcode for REGISTER MPCPDU as defined in Table 31A–1.

LLID: This parameter holds the logical link identification number assigned by the MAC Control client.

status: This parameter takes on the indication supplied by the flags field in the REGISTER MPCPDU as defined in Table 77–4.

pending_grants: This parameters echoes back the pending_grants field that was previously received in the REGISTER_REQ message.

rfOnTime: This parameter carries the target value of RF On Time for the given CNU transmitter. This value may be different than the *rfOnTime* value carried in the REGISTER_REQ MPCPDU received from the corresponding CNU MAC during Discovery stage.

rfOffTime: This parameter carries the target value of RF Off Time for the given CNU transmitter. This value may be different than the *rfOffTime* value carried in the REGISTER_REQ MPCPDU received from the corresponding CNU MAC during Discovery stage.

MA_CONTROL.indication(REGISTER, SA, LLID, status)

This service primitive is issued by the Discovery Process at the CLT or a CNU to notify the MAC Control client and Layer Management of the result of the change in registration status. This primitive takes the following parameters:

REGISTER: Opcode for REGISTER MPCPDU as defined in Table 31A–1.

SA: This parameter represents the MAC address of the CLT.

LLID: This parameter holds the logical link identification number assigned by the MAC Control client.

status: This parameter holds the value of accepted/denied/deregistered/reregistered.

MA_CONTROL.request(DA, REGISTER_ACK, status)

This service primitive is issued by the MAC Control clients at the CNU and the CLT to acknowledge the registration. This primitive takes the following parameters:

DA: Multicast MAC Control address as defined in Annex 31B.

REGISTER_ACK: Opcode for REGISTER_ACK MPCPDU as defined in Table 31A–1.

status: This parameter takes on the indication supplied by the flags field in the REGISTER MPCPDU as defined in Table 77–5.

MA_CONTROL.indication(REGISTER_ACK, SA, LLID, status, *RTT*)

This service primitive is issued by the Discovery Process at the CLT to notify the client and Layer Management that the registration process has completed. This primitive takes the following parameters:

REGISTER_ACK: Opcode for REGISTER_ACK MPCPDU as defined in Table 31A–1.

SA: This parameter represents the MAC address of the reciprocating device (CNU address at the CLT, and CLT address at the CNU).

LLID: This parameter holds the logical link identification number assigned by the MAC Control client.

status: This parameter holds the value of accepted/denied/reset/deregistered.

RTT: The measured round trip time to/from the CNU is returned in this parameter. *RTT* is stated in *time_quanta* units. This parameter holds a valid value only when the invoking Discovery Process in the CLT.

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Opcode-specific function(opcode)

Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

103.3.3.5 State diagrams

The Discovery Process in the CLT shall implement the discovery window setup state diagram shown in Figure 103–17, request processing state diagram as shown in Figure 103–18, register processing state diagram as shown in Figure 103–19, and final registration state diagram as shown in Figure 103–20. The discovery process in the CNU shall implement the registration state diagram as shown in Figure 103–21.

Instantiation of state diagrams as described in Table 103–17, Table 103–18, and Table 103–19 is performed only at the Multipoint MAC Control instances attached to the broadcast LLID (0x7FFE). Instantiation of state diagrams as described in Table 103–20 and Table 103–21 is performed for every Multipoint MAC Control instance, except the instance attached to the broadcast channel.

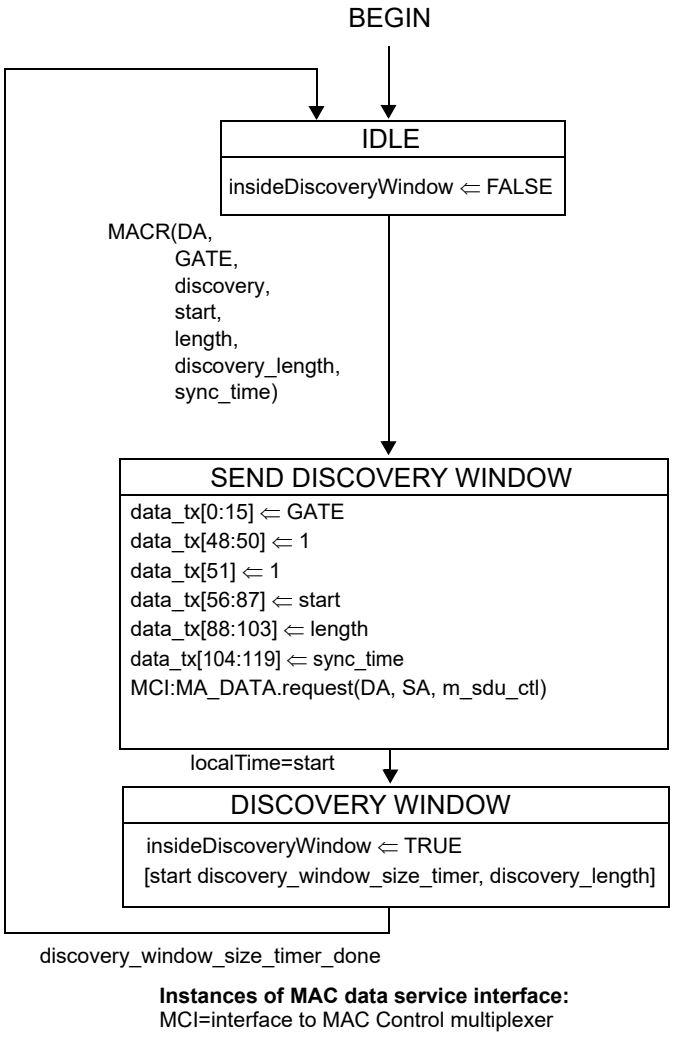

Figure 103–17—Discovery Processing CLT Window Setup state diagram

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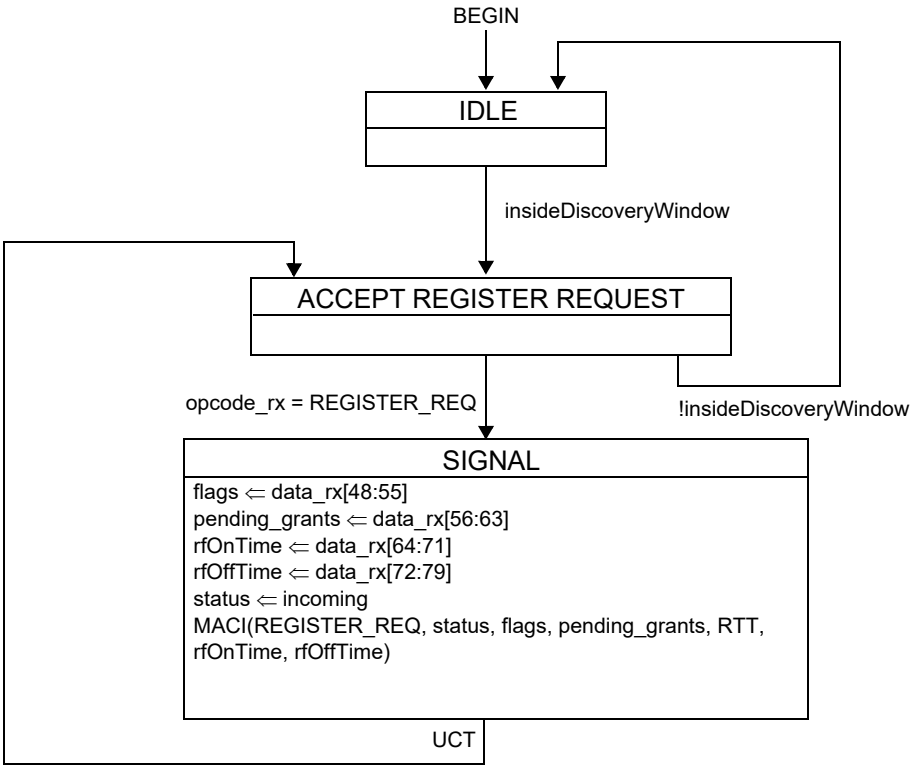

Figure 103–18—Discovery Processing CLT Process Requests state diagram

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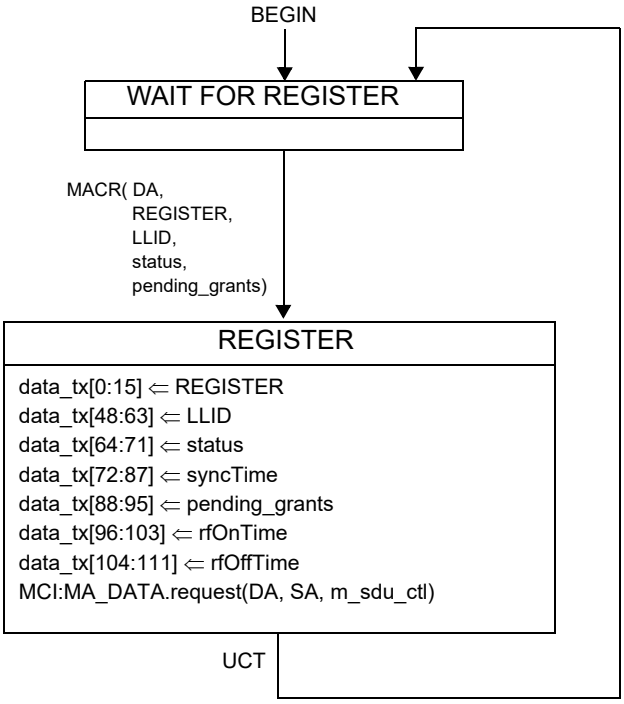

Figure 103–19—Discovery Processing CLT Register state diagram

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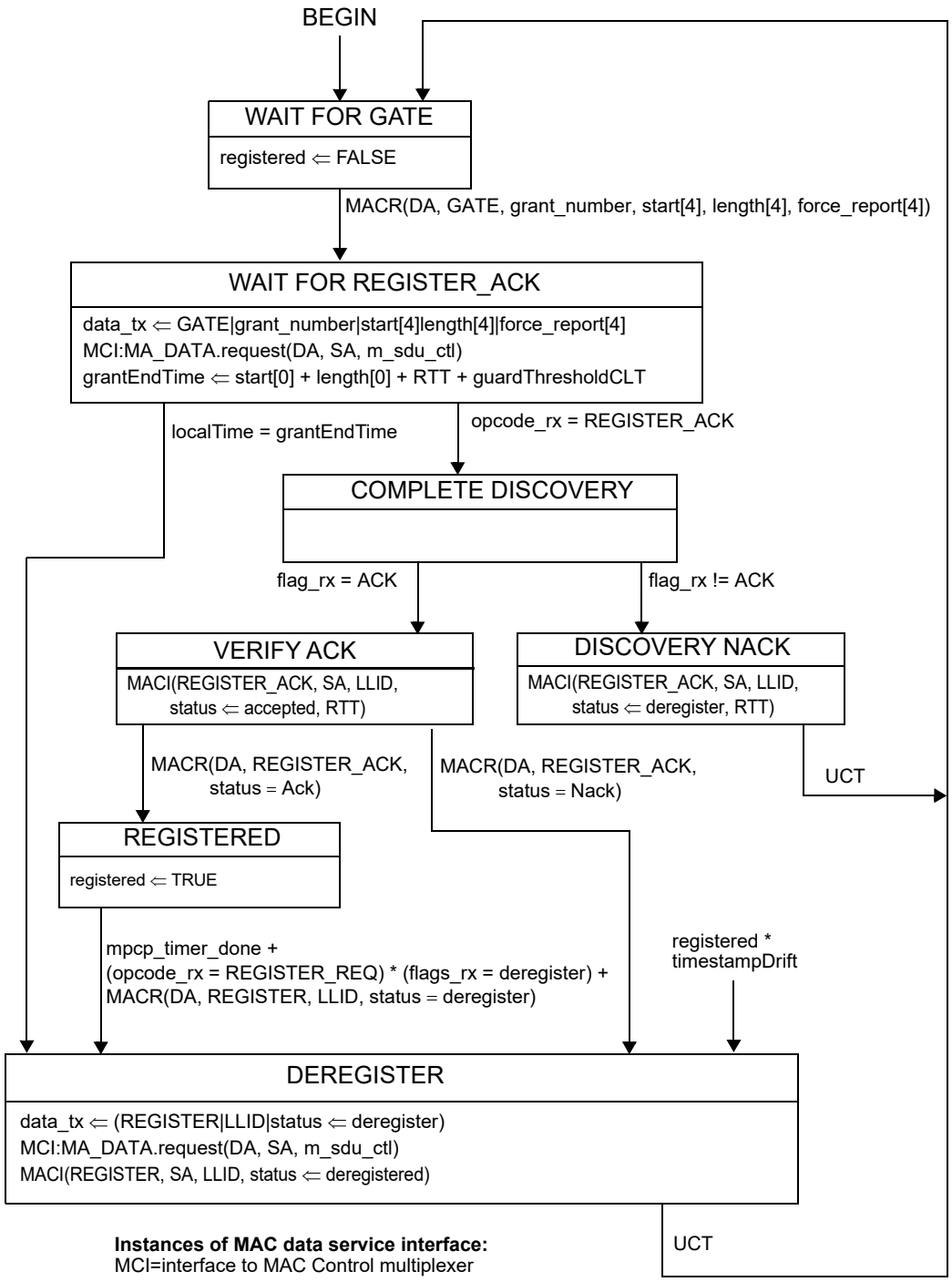

NOTE—The MAC Control Client issues the grant following the REGISTER message, taking the CNU processing delay of REGISTER message into consideration.

Figure 103–20—Discovery Processing CLT Final Registration state diagram

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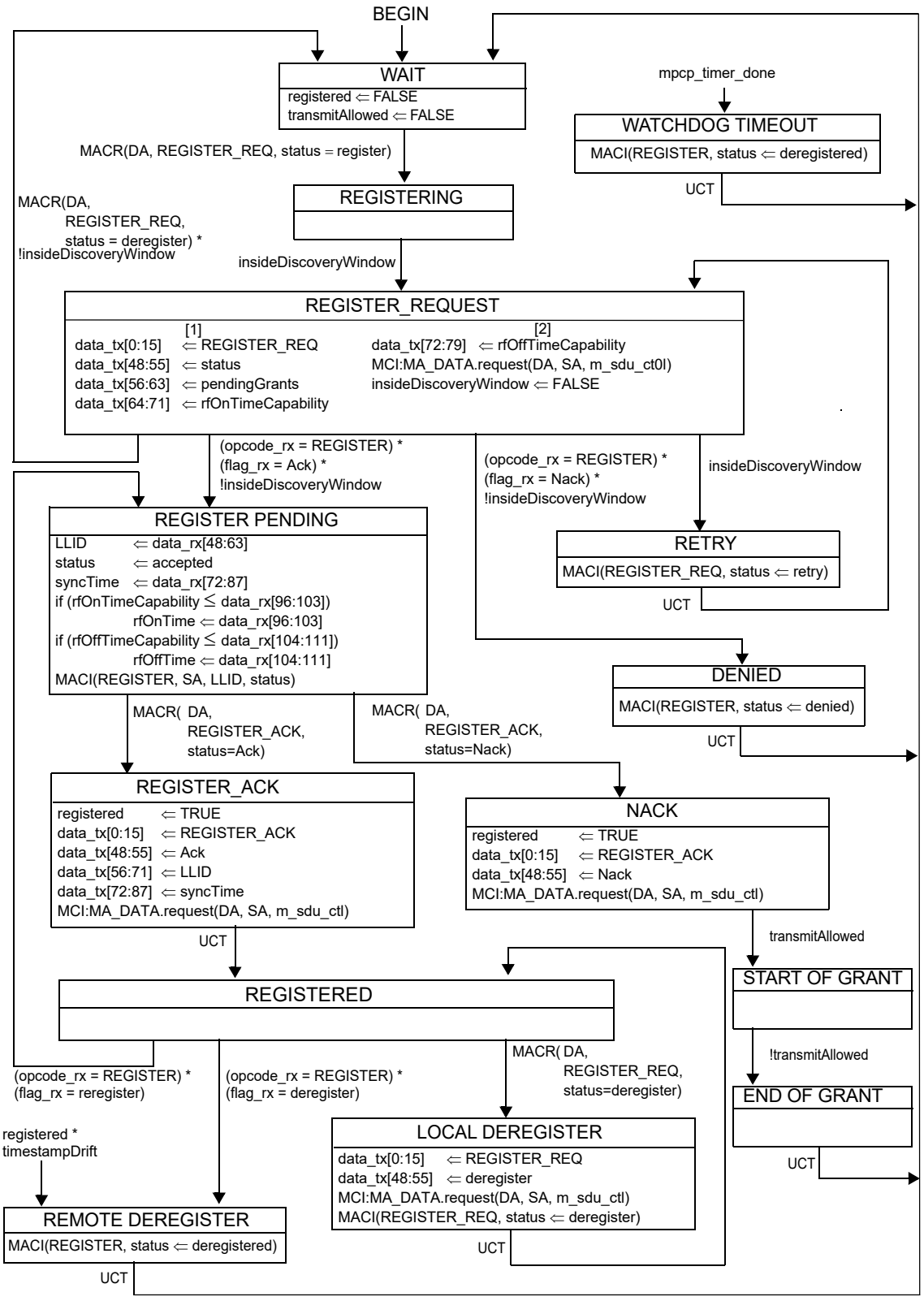

Figure 103–21—Discovery Processing CNU Registration state diagram

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103.3.4 Report Processing

Report processing in EPoC is as described in 77.3.4.

103.3.5 Gate Processing

Gate processing in EPoC is as described in 77.3.5 with the exception being that EPoC uses an RF transmitter rather than a laser.

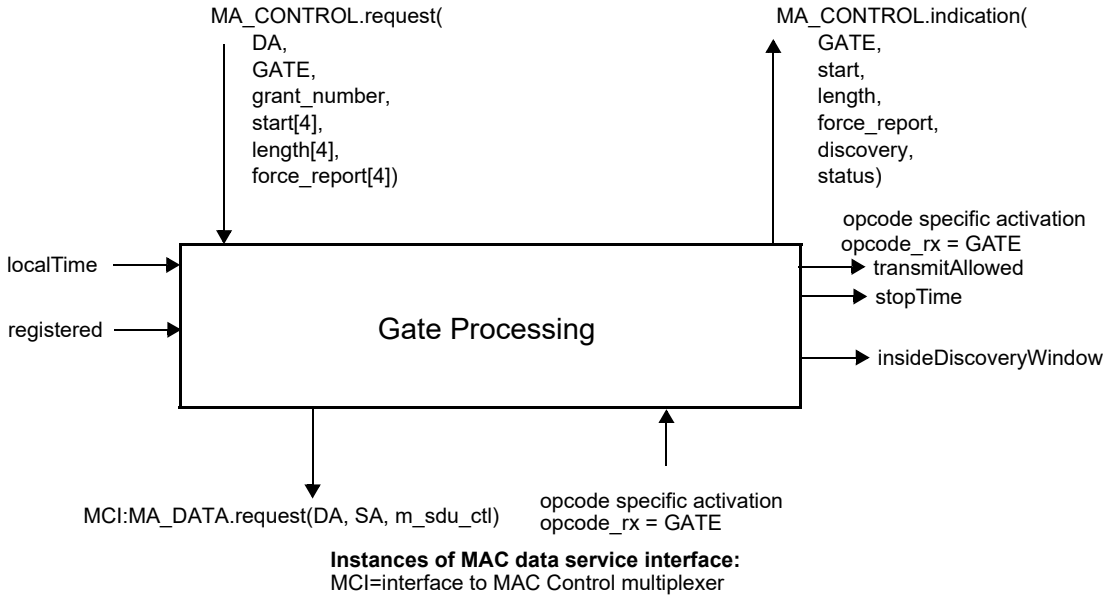

Figure 103–22—Gate Processing service interface

103.3.5.1 Constants

max_future_grant_time
: TYPE: 32-bit unsigned integer
This constant is defined in 77.3.5.1 and holds the time limiting the future time horizon for a valid incoming grant.
VALUE: 0x03-B9-AC-A0 (1 s)

min_processing_time
: TYPE: 32-bit unsigned integer
This constant is defined in 77.3.5.1and holds the time required for the CNU processing.
VALUE: 0x00-00-04-00 (16.384 μs)

103.3.5.2 Variables

BEGIN
: This variable is defined in 103.2.2.3.

BurstOverhead
: TYPE: integer

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This variable represents the burst overhead and returned by the BurstTimeHeader() function (see 101.3.2.5.7).

counter

TYPE: integer
This variable is used as a loop iterator counting the number of incoming grants in a GATE message.

currentGrant

TYPE:

```
structure
{
    DA:             48-bit unsigned, a.k.a MAC address type
    start           32-bit unsigned
    length          16-bit unsigned
    force_report    Boolean
    discovery       Boolean
}
```

This variable is defined in 77.3.5.2 and used for local storage of a pending grant state during processing. It is dynamically set by the Gate Processing functional block and is not exposed. The state is a structure field composed of multiple subfields.

data_rx

This variable is defined in 103.2.2.3.

data_tx

This variable is defined in 103.2.2.3.

effectiveLengthC

TYPE: 32-bit unsigned integer
This variable is used for temporary storage of a normalized net time value. It holds the net effective length of a grant, normalized for elapsed time.

gate_timeout

TYPE: 32-bit unsigned integer
This variable is defined in 77.3.5.2 and represents the maximum allowed interval of time between two GATE messages generated by the CLT to the same CNU, expressed in units of time_quanta.
VALUE: 0x00-2F-AF-08 (50 ms, default value)

grantList

TYPE: list of elements having the structure define in *currentGrant*
This variable is defined in 77.3.5.2 and used for storage of the list of pending grants. It is dynamically set by the Gate Processing functional block and is not exposed. Each time a grant is received it is added to the list. The list elements are structure fields composed of multiple subfields. The list is indexed by the start subfield in each element for quick searches.

grantStart

This variable is defined in 103.2.2.3.

insideDiscoveryWindow

This variable is defined in 103.3.3.2.

m_sdu_ctl

This variable is defined in 103.2.2.3.

maxDelay

TYPE: 16-bit unsigned integer
This variable is defined in 77.3.5.2 and holds the maximum delay that can be applied by a

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CNU before sending the REGISTER_REQ MPCPDU. This delay is calculated such that the CNU would have sufficient time to transmit the REGISTER_REQ message and its associated overhead (FEC parity data, end-of-frame sequence, etc.) and terminate the RF before the end of the discovery grant.

minGrantLengthC

TYPE: 32-bit unsigned integer
This variable represents the minimum data portion of a grant expressed in units of time_quanta. The *minGrantLengthC* is related to the minimum size Ethernet frame plus EPON overhead of 72 bytes (576 bits) processed as per 101.3.2.5.2 using a short codeword plus two IDLE blocks and one block for Burst Time Header. This results in a shortened codeword length of 1091 bits. The minimum grant length will include stop and end burst marker overhead based on *RBsize* and *RB_time_quanta* [see Equation (101–33)]:

Number_of_Burst_RBs is 8 for *RBsize* = FALSE or 4 for *RBsize* = TRUE

RB_total_time = *RB_time_quanta* × *Number_of_Burst_RBs*.

The value of *minGrantLengthC* is based on the *time_quanta* required for the number of Resource Blocks needed to transmit the 1091 data bits based on *US_DataRate* plus *RB_total_time*:

Data_TQ = 1091 / *US_DataRate*/*time_quantum*

minGrantLengthC = ceiling(*Data_TQ*/*RB_time_quanta*) × *RB_time_quanta* + *RB_total_time*

nextGrant

TYPE: element having same structure as defined in *currentGrant*
This variable is defined in 77.3.5.2 and used for local storage of a pending grant state during processing. It is dynamically set by the Gate Processing functional block and is not exposed. The content of the variable is the next grant to become active.

nextStopTime

TYPE: 32-bit unsigned integer
This variable is defined in 77.3.5.2 and holds the value of the *localTime* counter corresponding to the end of the next grant.

opcode_rx

This variable is defined in 103.2.2.3.

registered

This variable is defined in 103.3.3.2.

stopTime

This variable is defined in 103.2.2.3.

syncTime

This variable is defined in 103.3.3.2.

transmitAllowed

This variable is defined in 103.2.2.3.

103.3.5.3 Functions

empty(list)

This function is defined in 77.3.5.3 and used to check whether the list is empty. When there are no elements queued in the list, the function returns TRUE. Otherwise, a value of FALSE is returned.

InsertInOrder(sorted_list, inserted_element)

This function is defined in 77.3.5.2 and used to queue an element inside a sorted list. The queu-

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ing order is sorted. In the condition that the list is full the element may be discarded. The length of the list is dynamic and its maximum size equals the value advertised during registration as maximum number of pending grants.

IsBroadcast(grant)
: This function is defined in 77.3.5.3 and used to check whether its argument represents a broadcast grant, i.e., grant given to multiple CNUs. This is determined by the destination MAC address of the corresponding GATE message. The function returns the value TRUE when MAC address is a global assigned MAC Control address as defined in Annex 31B, and FALSE otherwise.

PeekHead(sorted_list)
: This function is defined in 77.3.5.3 and used to check the content of a sorted list. It returns the element at the head of the list without dequeuing the element.

Random(r)
: This function is defined in 77.3.5.3 and used to compute a random integer number uniformly distributed between 0 and *r*. The randomly generated number is then returned by the function.

RemoveHead(sorted_list)
: This function is defined in 77.3.5.3 and used to dequeue an element from the head of a sorted list. The return value of the function is the dequeued element.

103.3.5.4 Timers

gntWinTmr
: This timer is defined in 77.3.5.4 and used to wait for the event that signals the end of a grant window.
VALUE: The timer value is dynamically set according to the signaled grant length.

gate_periodic_timer
: This timer is defined in 77.3.5.4 and counts down time remaining before a forced generation of a GATE message in the CLT. The CLT is required to generate GATE MPCPDUs with a periodicity of less than *gate_timeout* value.

mpcp_timer
: This timer is defined in 103.3.3.3.

rndDlyTmrC
: This timer is used to measure a random delay inside the discovery window. The purpose of the delay is to a priori reduce the probability of transmission overlap during the registration process, and thus lowering the expectancy of registration time in the CCDN.
VALUE: A random value less than the net discovery window size less the REGISTER_REQ MPCPDU frame size less the idle period and RF turn on and off delays less the preamble size less the IFG size. The timer value is set dynamically based on the parameters passed from the client.

103.3.5.5 Messages

MA_DATA.request (DA, SA, m_sdu)
: The service primitive is defined in 2.3.2.

MA_CONTROL.request(DA, GATE, grant_number, start[4], length[4], force_report[4])
: This service primitive is defined in 103.3.3.4.

MA_CONTROL.indication(GATE, start, length, force_report, discovery, status)
: This service primitive issued by the Gate Process at the CNU to notify the MAC Control client and higher layers that a grant is pending. This primitive is invoked multiple times when a sin-

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gle GATE message arrives with multiple grants. It is also generated at the start and end of each grant as it becomes active. This primitive uses the following parameters:

GATE: Opcode for GATE MPCPDU as defined in Table 31A–1.

start: Start time of the grant. This parameter is not present when the parameter status value is equal to deactive.

length: Length of the grant. This parameter is not present when the parameter status value is equal to deactive.

force_report: Flags indicating whether a REPORT message should be transmitted in this grant. This parameter is not present when the parameter status value is equal to deactive.

discovery: This parameter holds the value TRUE when the grant is to be used for the discovery process, and FALSE otherwise. This parameter is not present when the parameter status value is equal to deactive.

status: This parameter takes the value arrive on grant reception, active when a grant becomes active, and deactive at the end of a grant.

Opcode-specific function(opcode)

Functions exported from opcode specific blocks that are invoked on the arrival of a MAC Control message of the appropriate opcode.

103.3.5.6 State diagrams

The gating process in the CLT shall implement the Gate processing state diagram as shown in Figure 103–23. The gating process in the CNU shall implement the Gate processing state diagram as shown in Figure 103–24 and Figure 103–25. Instantiation of state diagrams as described is performed for all Multipoint MAC Control instances.

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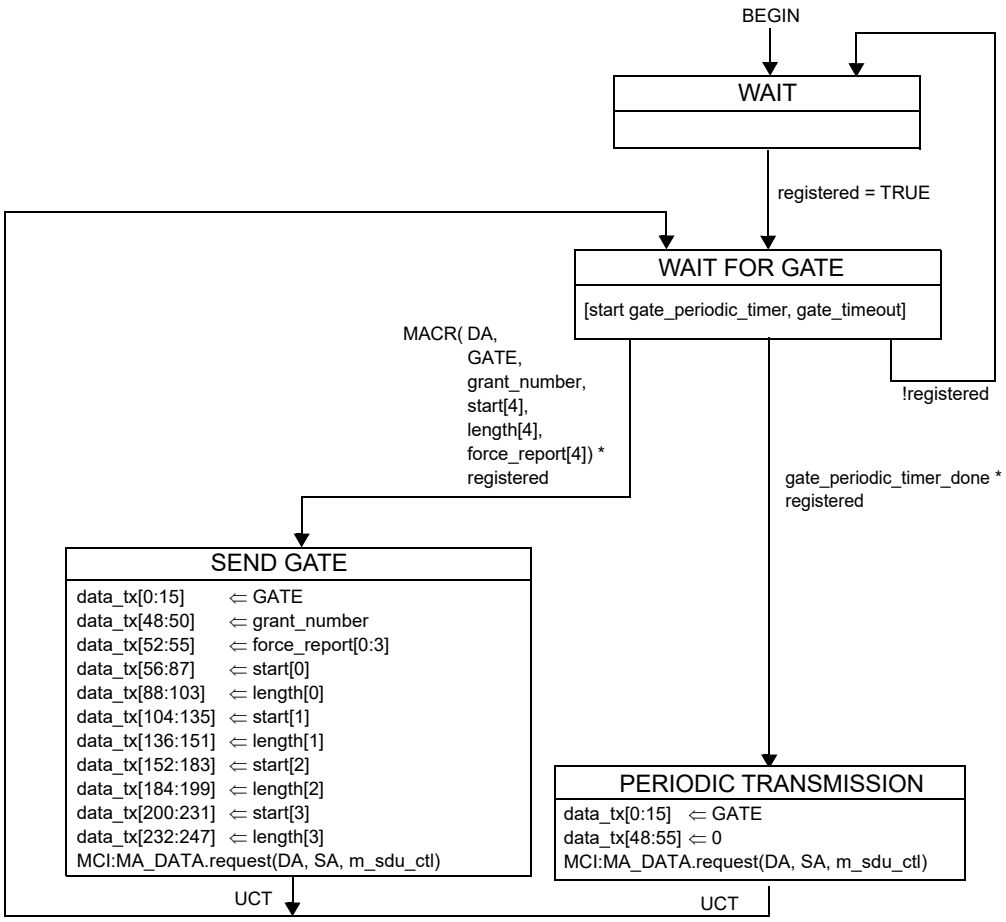

Instances of MAC data service interface:
MCI=interface to MAC Control multiplexer

Figure 103–23—Gate Processing state diagram at CLT

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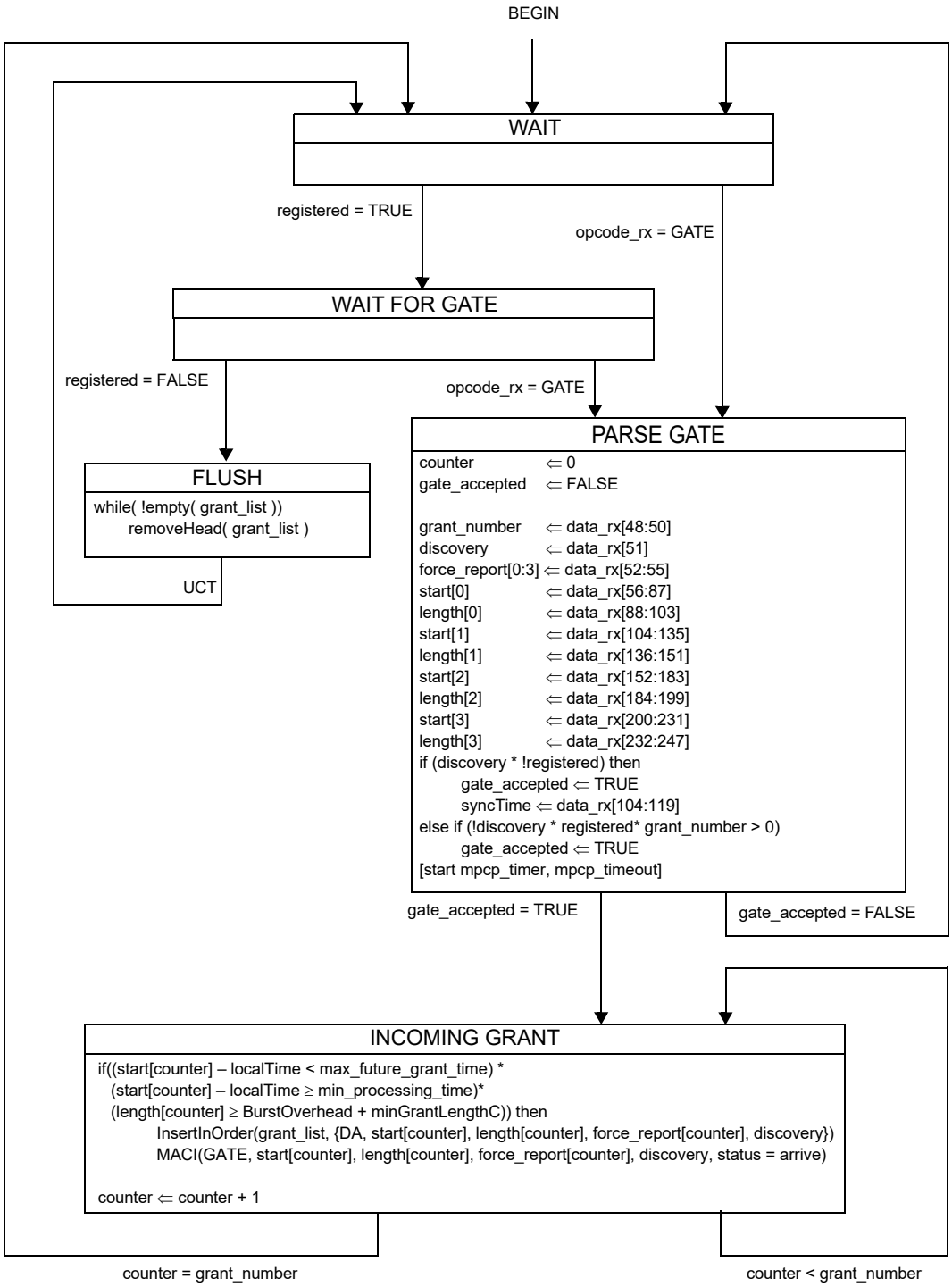

Figure 103–24—Gate Processing CNU Programing state diagram

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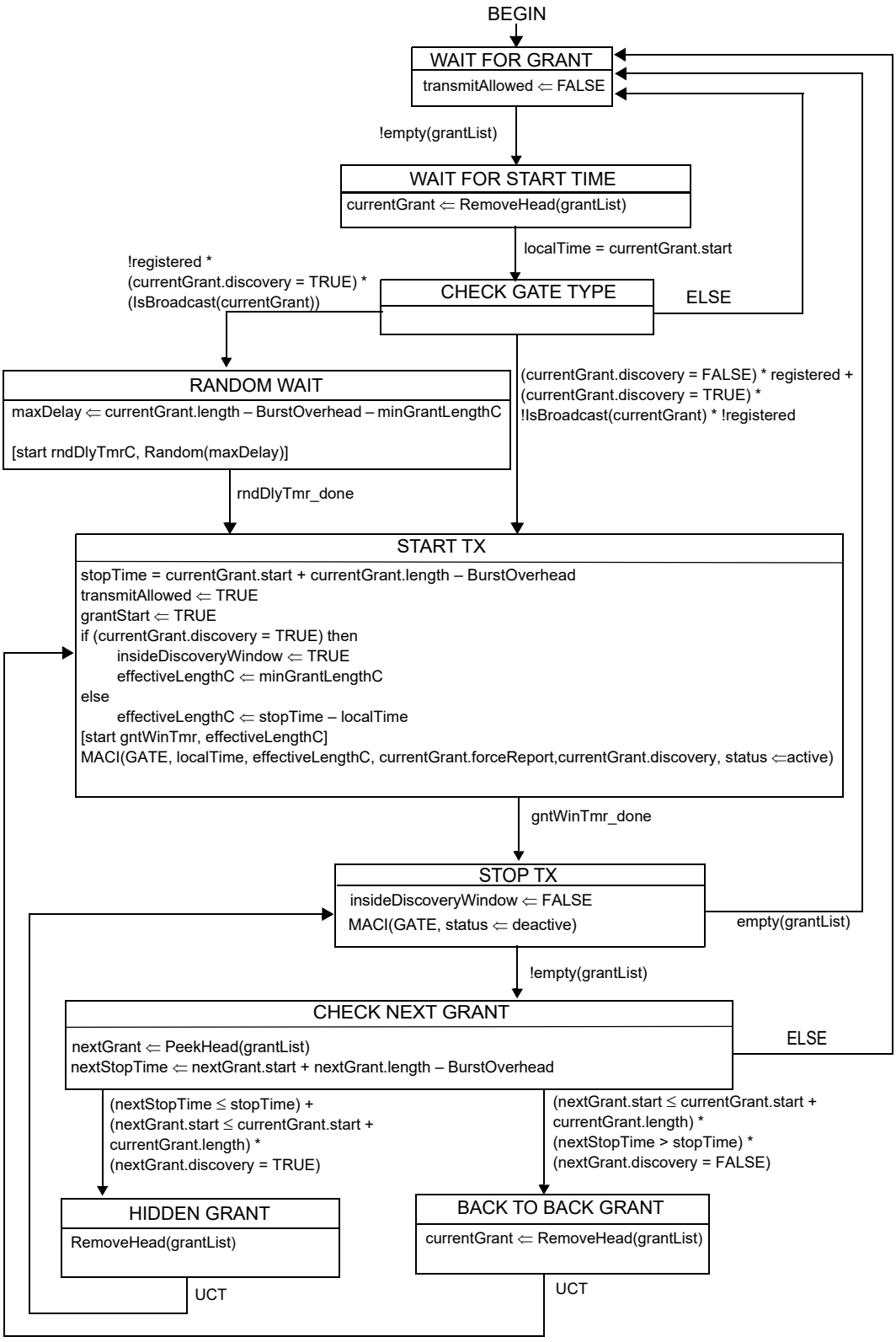

Figure 103–25—Gate Processing CNU Activation state diagram

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103.3.6 MPCPDU structure and encoding

The generic MPCPDU structure and encoding in EPoC is as described in 77.3.6 The MPCPDU structure shall be as shown in Figure 77–31. Changes to specific MPCPDU messages are noted in 103.3.6.1 through 103.3.6.5.

103.3.6.1 GATE description

The GATE MPCPDU used in EPoC is the same as that described in 77.3.6.1 with the following exceptions. In EPoC *rfOnTime* and *rfOffTime* replace *laserOnTime* and *laserOffTime*, respectively. The Sync Time and Discovery Information fields described in 77.3.6.1 are not used in EPoC and shall be set to zero on transmit and ignored on reception.

103.3.6.2 REPORT description

The REPORT MPCPDU used in EPoC is the same as that described in 77.3.6.2.

103.3.6.3 REGISTER_REQ description

The REGISTER_REQ MPCPDU used in EPoC and illustrated in Figure 103–26 is the same as that described in 77.3.6.3 with the following exceptions. The Discovery Information field described in 77.3.6.3 is not used in EPoC and shall be set to zero on transmit and ignored on reception.

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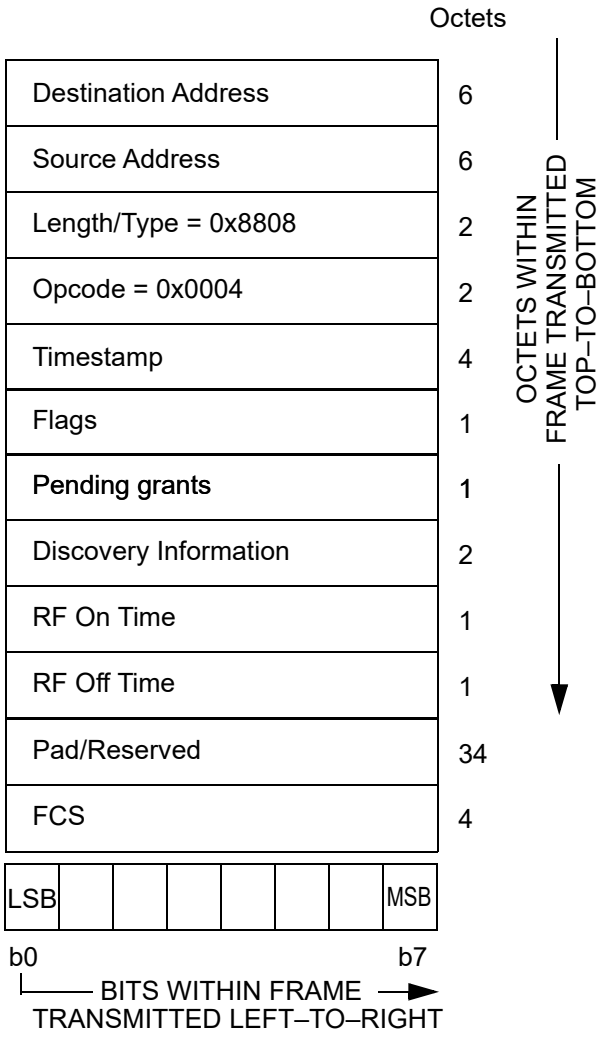

Figure 103–26—REGISTER_REQ MPCPDU

103.3.6.4 REGISTER description

The REGISTER MPCPDU used in EPoC and illustrated in Figure 103–27 is the same as that described in 77.3.6.4 with the following exceptions. In EPoC, the Sync Time field is calculated using *rfOnTime*, *rfOffTime* rather than the *laserOnTime* and *laserOffTime* used in 77.3.6.4.

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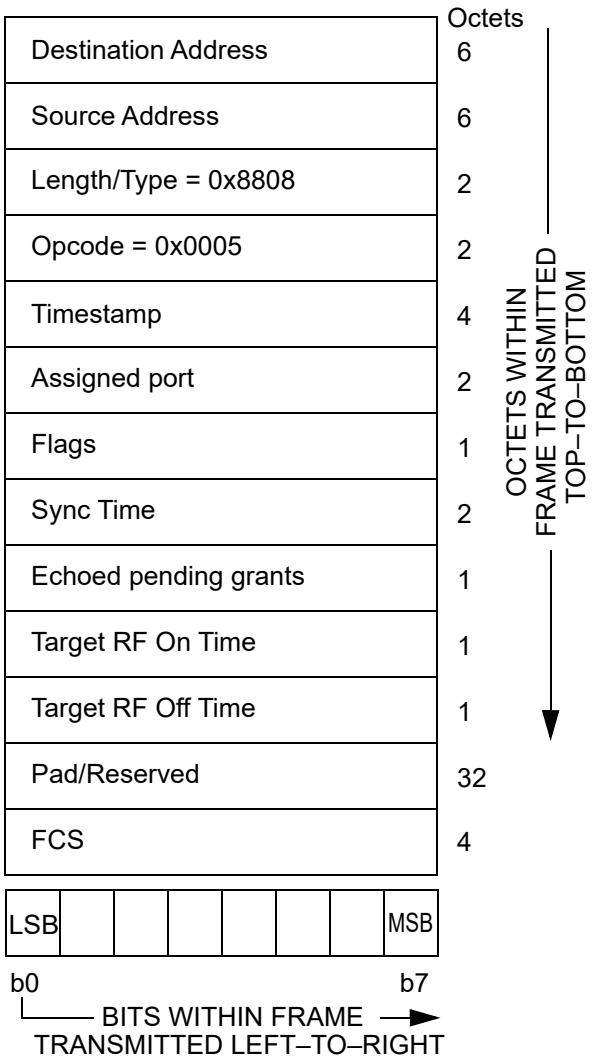

Figure 103–27—REGISTER MPCPDU

103.3.6.5 REGISTER_ACK description

The REGISTER_ACK MPCPDU used in EPoC is the same as that described in 77.3.6.5.

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103.4 Protocol implementation conformance statement (PICS) proforma for Clause 103, Multipoint MAC Control for EPoC[177]

103.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 103, Multipoint MAC Control for EPoC, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

103.4.2 Identification

103.4.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

103.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 103, Multipoint MAC Control for EPoC
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[177] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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103.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*CLT	CLT functionality	103.1	Device supports functionality required for CLT	O/1	Yes [ ] No [ ]
*CNU	CNU functionality	103.1	Device supports functionality required for CNU	O/1	Yes [ ] No [ ]

103.4.4 PICS proforma tables for Multipoint MAC Control

103.4.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Delay through MAC	103.3.2.4	Maximum delay variation of 1 *time_quantum*	M	Yes [ ] No [ ]
CC2	CLT grant time delays	103.3.2.4	Not grant nearer than 1 *time_quantum* into the future	CLT:M	Yes [ ] No [ ] N/A [ ]
CC3	CNU processing delays	103.3.2.4	Process all messages in less than 1024 *time_quanta*	CNU:M	Yes [ ] No [ ] N/A [ ]
CC4	CLT grant issuance	103.3.2.4	Not grant more than one message every 1024 *time_quanta* to a single CNU	CLT:M	Yes [ ] No [ ] N/A [ ]
CC5	CLT gap time	103.3.2.4	Minimum gap time between bursts to any two CNUs is equal to *RB_time_quanta*	CLT:M	Yes [ ] No [ ] N/A [ ]

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103.4.4.2 Multipoint MAC Control

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	CLT *localTime*	77.2.2.2	Track transmit clock	CLT:M	Yes [ ] No [ ] N/A [ ]
OM2	CNU *localTime*	77.2.2.2	Track receive clock	CNU:M	Yes [ ] No [ ] N/A [ ]
OM3	Random wait for transmitting REGISTER_REQ messages	77.3.3	Shorter than length of discovery window	CNU:M	Yes [ ] No [ ] N/A [ ]
OM4	Periodic report generation	77.3.4	Reports are generated periodically	CNU:M	Yes [ ] No [ ] N/A [ ]
OM5	Periodic granting	77.3.4	Grants are issued periodically	CLT:M	Yes [ ] No [ ] N/A [ ]
OM6	Issuing of grants	77.3.5	Not issue more than maximum supported grants	CLT:M	Yes [ ] No [ ] N/A [ ]

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103.4.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Multipoint Transmission Control	103.2.2.7	Meets the requirements of Figure 103–9	M	Yes [ ] No [ ]
SM2	CLT Control Parser	103.2.2.7	Meets the requirements of Figure 103–10	M	Yes [ ] No [ ]
SM3	CNU Control Parser	103.2.2.7	Meets the requirements of Figure 103–11	M	Yes [ ] No [ ]
SM4	CLT Control Multiplexer	103.2.2.7	Meets the requirements of Figure 103–12	CLT:M	Yes [ ] No [ ] N/A [ ]
SM5	CNU Control Multiplexer	103.2.2.7	Meets the requirements of Figure 103–13	CLT:M	Yes [ ] No [ ] N/A [ ]
SM6	Discovery Processing CLT Window Setup	103.3.3.5	Meets the requirements of Figure 103–17	CLT:M	Yes [ ] No [ ] N/A [ ]
SM7	Discovery Processing CLT Process Requests	103.3.3.5	Meets the requirements of Figure 103–18	CLT:M	Yes [ ] No [ ] N/A [ ]
SM8	Discovery Processing CLT Register	103.3.3.5	Meets the requirements of Figure 103–19	CNU:M	Yes [ ] No [ ] N/A [ ]
SM9	Discovery Processing CLT Final Registration	103.3.3.5	Meets the requirements of Figure 103–20	CLT:M	Yes [ ] No [ ] N/A [ ]
SM10	Discovery Processing CNU Registration	103.3.3.5	Meets the requirements of Figure 103–21	CNU:M	Yes [ ] No [ ] N/A [ ]
SM11	Report Processing at CLT	77.3.4.6	Meets the requirements of Figure 77–25	CLT:M	Yes [ ] No [ ] N/A [ ]
SM12	Report Processing at CNU	77.3.4.6	Meets the requirements of Figure 77–26	CNU:M	Yes [ ] No [ ] N/A [ ]
SM13	Gate Processing at CLT	103.3.5.6	Meets the requirements of Figure 103–23	CLT:M	Yes [ ] No [ ] N/A [ ]
SM14	Gate Processing at CNU	103.3.5.6	Meets the requirements of Figure 103–24	CNU:M	Yes [ ] No [ ] N/A [ ]
SM15	Gate Processing CNU Activation	103.3.5.6	Meets the requirements of Figure 103–25	CNU:M	Yes [ ] No [ ] N/A [ ]

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103.4.4.4 MPCP

Item	Feature	Subclause	Value/Comment	Status	Support
MP1	MPCPDU structure	77.3.6	As in Figure 77–31	M	Yes [ ] No [ ]
MP2	LLID for MPCPDU	77.3.6	RS generates LLID for MPCPDU	M	Yes [ ] No [ ]
MP3	Grants during discovery	77.3.6.1	Single grant in GATE message during discovery	CLT:M	Yes [ ] No [ ] N/A [ ]
MP4	Grant start time	77.3.6.1	Grants within one GATE MPCPDU are sorted by their Start time values	CLT:M	Yes [ ] No [ ] N/A [ ]
MP5	GATE generation	77.3.6.1	GATE generated for active CNU except during discovery	CLT:M	Yes [ ] No [ ] N/A [ ]
MP6	GATE LLID	77.3.6.1	Unicast LLID except for discovery	CLT:M	Yes [ ] No [ ] N/A [ ]
MP7	GATE *rfOnTime* and *rfOffTime*	103.3.6.1	Always zero	CLT:M	Yes [ ] No [ ] N/A [ ]
MP8	REGISTER_REQ Discovery Information	103.3.6.3	Always zero	CNU:M	Yes [ ] No [ ] N/A [ ]
MP9	REPORT issuing	77.3.6.2	Issues REPORT periodically	CNU:M	Yes [ ] No [ ] N/A [ ]
MP8	REPORT generation	77.3.6.2	Generated by active CNU	CNU:M	Yes [ ] No [ ] N/A [ ]
MP9	REPORT queue #n	77.3.6.2	REPORT Queue #n length rounding	CNU:M	Yes [ ] No [ ] N/A [ ]
MP10	REPORT LLID	77.3.6.2	REPORT has unicast LLID	CNU:M	Yes [ ] No [ ] N/A [ ]
MP11	REGISTER_REQ generation	77.3.6.3	Generated by undiscovered CNU	CNU:M	Yes [ ] No [ ] N/A [ ]
MP12	REGISTER_REQ LLID	77.3.6.3	Use broadcast LLID	CNU:M	Yes [ ] No [ ] N/A [ ]
MP13	REGISTER DA address	77.3.6.4	Use individual MAC address	CLT:M	Yes [ ] No [ ] N/A [ ]
MP14	REGISTER generation	77.3.6.4	Generated for all CNUs	CLT:M	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MP15	REGISTER_ACK generation	77.3.6.5	Generated by active CNU	CNU:M	Yes [ ] No [ ] N/A [ ]
MP16	REGISTER_ACK LLID	77.3.6.5	Use unicast LLID	CNU:M	Yes [ ] No [ ] N/A [ ]
MP17	MAC enable	77.2.2.4	MAC Control interface has priority over other clients (see definition of SelectFrame)	CLT:M	Yes [ ] No [ ] N/A [ ]

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104. Power over Data Lines (PoDL) of Single-Pair Ethernet

104.1 Overview

This clause defines the functional and electrical characteristics of two optional power entities, a PoDL Powered Device (PD) and PoDL Power Sourcing Equipment (PSE), for use with supported single balanced twisted-pair Ethernet Physical Layers. When used in this clause, the term PSE always means PoDL PSE, and the term PD always means PoDL PD. These entities allow devices to supply/draw power using the same cabling that may be used for data transmission. PoDL is intended to provide a single balanced twisted-pair Ethernet Physical Layer device with a single interface to both the data it requires and the power to process this data. This clause specifies the following:

a) The characteristics of a power source to add power to the 100 Ω single balanced twisted-pair cabling system.
b) The characteristics of a PD's load on the power source and the cabling.
c) Certain electrical parameters of each MDI/PI that may be different from that specified in the PHY clause when power is simultaneously transmitted with data.
d) Physical Layer protocols allowing the detection of a device that requests power from a PSE and classification of the device based on its power needs.
e) A method for Powered Devices and Power Sourcing Equipment to negotiate and allocate power.
f) A method for scaling supplied voltage back to the sleep level when full operating voltage is no longer requested or required.

This clause differentiates between the two ends of the link, defining the PSE and the PD as separate but related devices within a PoDL system.

104.1.1 Compatibility considerations

Compliant implementations of PD and PSE systems are defined as compatible at their respective Power Interfaces (PIs) when used in accordance with the restrictions of this clause. Designers are free to implement circuitry within the PD and PSE in an application-dependent manner provided that the respective PI specifications are satisfied. MDIs that incorporate compliant PoDL PIs are compatible with their respective Physical Layer standards. Such compatibility may require additional specifications found within this clause (see 104.6).

104.1.2 Relationship of PoDL to the IEEE 802.3 architecture

PoDL is an optional power entity to be used in conjunction with supported single-pair Ethernet Physical Layers. Data that is out of band to normal Ethernet traffic may be transmitted and received between the PSE and PD prior to the application of power and subsequent to the removal of full operating voltage via the MDI using the Serial Communication Classification Protocol (SCCP) which is described in 104.7.

Figure 104–1 depicts the positioning of PoDL for the PSE. Figure 104–2 depicts the positioning of PoDL in the case of the PD.

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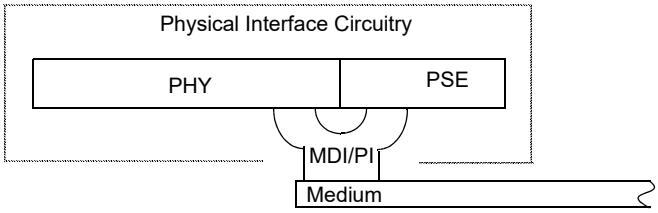
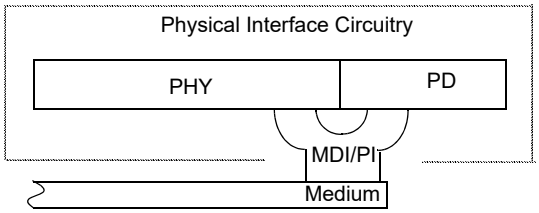


MDI = Medium Dependent Interface
PHY = Physical Layer Device
PI = Power Interface
PSE = Power Sourcing Equipment

Figure 104–1—PoDL Power Sourcing Equipment (PSE) relationship to the physical interface circuitry and the IEEE 802.3 Ethernet model



MDI = Medium Dependent Interface
PD = Powered Device
PHY = Physical Layer Device
PI = Power Interface

Figure 104–2—PoDL Powered Device (PD) relationship to the physical interface circuitry (PHY) and the IEEE 802.3 Ethernet model

The Power Interface (PI) is the generic term that refers to the mechanical and electrical interface between the PSE or PD and the transmission medium. The PI is encompassed within the MDI.

104.1.3 PoDL system types

A PoDL system consists of a PSE, a link segment, and a PD. PoDL systems are not specified for mixing segments.

A Type A or Type C PSE and Type A or Type C PD are compatible with 10BASE-T1S and 100BASE-T1 PHYs. A Type B or Type C PSE and Type B or Type C PD are compatible with 1000BASE-T1 PHYs. A Type C PSE and Type C PD are compatible with 10BASE-T1S, 100BASE-T1, and 1000BASE-T1 PHYs. Type D PSEs and Type D PDs may be incompatible with IEEE 802.3 PHYs and may lack a data entity. A Type E PSE and Type E PD are compatible with 10BASE-T1L PHYs. A Type F PSE and Type F PD are compatible with 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs.

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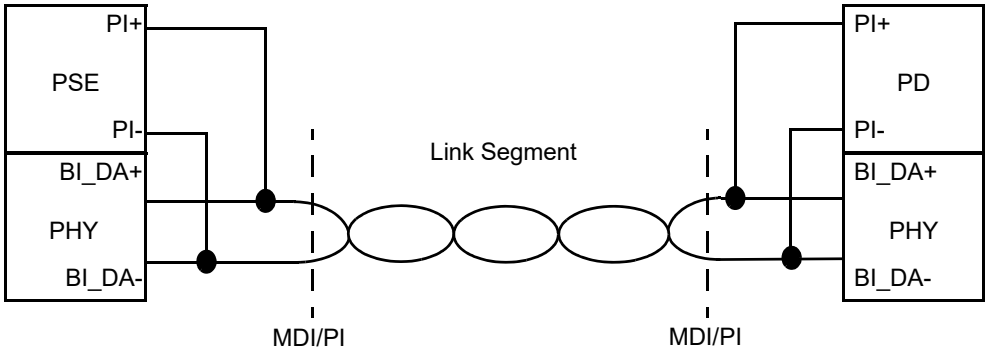
Figure 104–3 illustrates the block diagram for a PoDL system.



NOTE—PI elements that prevent loading of the data signal by the PSE and PD are not shown. PHY elements that block dc are not shown.

Figure 104–3—PoDL system block diagram

104.2 Link segment

The dc loop resistance of the link segment shall be less than 6 Ω for classes 0 and 1. The dc loop resistance shall be less than 6.5 Ω for classes 2 through 9. The link segment dc loop resistance shall be less than 65 Ω for classes 10 and 13. The link segment dc loop resistance shall be less than 25 Ω for classes 11 and 14. The link segment dc loop resistance shall be less than 9.5 Ω for classes 12 and 15.

104.3 Class power requirements

PSEs and PDs are further categorized by their class. These classes and the relevant electrical specifications are shown in Table 104–1 and Table 104–2.

Table 104–1—Class power requirements matrix for PSE, PI, and PD for classes 0 through 9

	12 V unregulated PSE		12 V regulated PSE		24 V unregulated PSE		24 V regulated PSE		48 V regulated PSE	
Class	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
$V_{PSE(max)}$ (V)[a]	18	18	18	18	36	36	36	36	60	60
$V_{PSE\_OC(min)}$ (V)[b]	6	6	14.4	14.4	12	12	26	26	48	48
$V_{PSE(min)}$ (V)	5.6	5.77	14.4	14.4	11.7	11.7	26	26	48	48
$I_{PI(max)}$ (mA)[c]	101	227	249	471	97	339	215	461	735	1 360
$P_{Class(min)}$ (W)[d]	0.566	1.31	3.59	6.79	1.14	3.97	5.59	12	35.3	65.3

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Table 104–1—Class power requirements matrix for PSE, PI, and PD for classes 0 through 9 *(continued)*

	12 V unregulated PSE		12 V regulated PSE		24 V unregulated PSE		24 V regulated PSE		48 V regulated PSE	
Class	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
$V_{PD(min)}$ (V)	4.94	4.41	12	10.6	10.3	8.86	23.3	21.7	40.8	36.7
$P_{PD(max)}$ (W)[e]	0.5	1	3	5	1	3	5	10	30	50

[a]$V_{PSE(max)}$ is the maximum allowed voltage at the PSE PI over the full range of operating conditions.
[b]$V_{PSE\_OC(min)}$ is the minimum allowed open circuit voltage measured at the PSE PI.
[c]$I_{PI(max)}$ is the maximum current flowing at the PSE and PD PIs except during inrush or an overload condition. $I_{PI(max)}$ may be exceeded during inrush or an overload (see 104.4.7.2). Users are cautioned to be aware of the ampacity of cabling, as installed, and local codes and regulations (see 104.8.1).
[d]$P_{Class(min)}$ is the minimum average available output power at the PSE PI.
[e]$P_{PD(max)}$ is the maximum average available power at the PD PI.

Table 104–2—Class power requirements matrix for PSE, PI, and PD for classes 10 through 15

Class	**10**	**11**	**12**	**13**	**14**	**15**
$V_{PSE(max)}$ (V)	30	30	30	58	58	58
$V_{PSE\_OC(min)}$ (V)	20	20	20	50	50	50
$V_{PSE(min)}$ (V)	20	20	20	50	50	50
$I_{PI(max)}$ (mA)	92	240	632	231	600	1579
$P_{class(min)}$ (W)	1.85	4.8	12.63	11.54	30	79
$V_{PD(min)}$ (V)	14	14	14	35	35	35
$P_{PD(max)}$ (W)	1.23	3.2	8.4	7.7	20	52

104.4 Power Sourcing Equipment (PSE)

The PSE provides power to the PD. The PSE's main functions are as follows:

a) To search the link segment for a PD
b) To supply power to a detected PD through the link segment
c) To monitor the power applied to a link segment
d) To remove the full operating voltage when no longer required, when transitioning to the SLEEP state, or when a short-circuit or other fault is detected

Voltage and power classification mechanisms exist via the Serial Communication Classification Protocol (SCCP) to provide the PSE with detailed information regarding the requirements of the PD and vice versa.

A PSE is specified by its electrical and logical behavior as seen at the PI.

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104.4.1 PSE types

For PoDL systems there are multiple types of PSEs—Type A, Type B, Type C, Type D, Type E, and Type F consistent with 104.1.3.

104.4.2 PI pin assignments

A PSE provides power via a single two-wire connection. Table 104–3 in conjunction with Figure 104–3 illustrates the PSE pinout.

Table 104–3—PSE pinout

Contact	PI
1	PI+
2	PI–

A PSE shall implement the PSE pinout in Table 104–3.

104.4.3 PSE classes

A PSE shall comply with the voltage and power requirements listed in Table 104–1 for the relevant class.

104.4.4 PSE state diagram

The PSE shall implement the behavior of the state diagrams shown in Figure 104–4, Figure 104–5, and Figure 104–6.

104.4.4.1 Overview

Prior to application of full operating voltage at the PI, the PSE performs detection in order to verify that a valid PD is present. A PSE may apply full operating voltage if it is able to successfully classify the PD using SCCP.

After full operating voltage has been applied, the PSE monitors the PI for a valid Maintain Full Voltage Signature (MFVS) from the PD. In the event a valid MFVS is not present, the PSE reduces the voltage at the PI to the range of V_{Sleep}. If an external wakeup request is received or if a valid wakeup current signature is detected at the PI, the PSE confirms that a valid PD is present by re-performing detection and, if enabled, classification before reapplying full operating voltage to the PI.

Additionally, while voltage is applied, the PSE monitors the current drawn and removes power if it detects an overload, short-circuit, or other fault.

104.4.4.2 Conventions

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

104.4.4.3 Variables

The PSE state diagrams use the following variables:

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detection_done
TRUE: the detection sequence has terminated since the last entry to the IDLE state either as a result of a valid or invalid signature being detected.
FALSE: the detection sequence has not terminated since the last entry to the IDLE state either as a result of a valid or invalid signature being detected.

do_classification_done
TRUE: following a detection sequence, the PSE has concluded serial communication after performing a read of the PD information and any additional implementation dependent read or write commands.
FALSE: following a detection sequence, the PSE has not concluded serial communication after performing a read of the PD information and any additional implementation dependent read or write commands.

external_wakeup
TRUE: while in the SLEEP state, the PSE has received an external wakeup request.
FALSE: while in the SLEEP state, the PSE has not received an external wakeup request.

iprebias_valid
TRUE: the PSE pre-bias output current is valid (see 104.4.7.2.3).
FALSE: the PSE pre-bias output current is invalid (see 104.4.7.2.3).

mfvs_timeout
TRUE: the MFVS dropout timer has timed out.
FALSE: the MFVS dropout timer has not timed out.

mfvs_valid
TRUE: MFVS is present (see 104.4.8.1).
FALSE: MFVS is absent (see 104.4.8.1).

mr_pse_enable
TRUE: enable operation of the PSE.
FALSE: disable operation of the PSE.

mr_sccp_enabled
TRUE: SCCP is enabled (see 104.7).
FALSE: SCCP is not enabled (see 104.7).

mr_invalid_signature
TRUE: an invalid signature has been detected during the detection cycle subsequent to the last idle sequence.
FALSE: an invalid signature has not been detected.

mr_valid_signature
TRUE: a valid PD signature has been detected during the detection cycle subsequent to the last idle sequence.
FALSE: a valid PD signature has not been detected.

overload_detected
TRUE: the PSE has detected an overload condition (see 104.4.7.2.1).
FALSE: the PSE has not detected an overload condition.

overload_held
TRUE: overload_detected has been TRUE since last entry to the IDLE state.
FALSE: overload_detected has been FALSE since last entry to the IDLE state.

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pd_wakeup
TRUE: while in the SLEEP state, the PSE has detected a valid wakeup current signature.
FALSE: while in the SLEEP state, the PSE has not detected a valid wakeup current signature.

pi_classifying
TRUE: the PSE is performing classification at the PI (see 104.7).
FALSE: the PSE is not performing classification at the PI.

pi_detecting
TRUE: the circuitry that forces a voltage limited detection current and senses the voltage at the PI is enabled (see 104.4.5).
FALSE: the circuitry that forces a voltage limited detection current and senses the voltage at the PI is disabled.

pi_discharge_en
TRUE: the circuitry that discharges the PI to V_{Sleep} is enabled.
FALSE: the circuitry that discharges the PI to V_{Sleep} is disabled.

pi_powered
TRUE: the circuitry that applies full operating voltage to the PI is enabled.
FALSE: the circuitry that applies full operating voltage to the PI is disabled.

pi_prebiased
TRUE: the circuitry that applies V_{Sleep} at the PI during the RESTART, RESTART_DELAY, and IDLE states is enabled (see 104.4.7.1).
FALSE: the circuitry that applies V_{Sleep} at the PI is disabled.

pi_sleeping
TRUE: the circuitry that applies V_{Sleep} at the PI during the SETTLE_SLEEP and SLEEP states is enabled (see 104.4.7.1).
FALSE: the circuitry that applies V_{Sleep} at the PI is disabled.

power_stable
TRUE: following inrush, the PSE has begun steady-state operation.
FALSE: the PSE is either not applying full operating voltage or has begun applying full operating voltage but is still in the POWER_UP state.

power_available
TRUE: a compatible PSE class to PD class pairing exists as defined in Table 104–4 and Table 104–5, and the PSE is able to source the required voltage and power.
FALSE: a valid PSE class to PD class pairing does not exist as defined in Table 104–4 and Table 104–5, or the PSE is not able to source the required voltage and power.

pse_ready
TRUE: the PSE is ready to probe the link segment.
FALSE: the PSE is not ready to probe the link segment.

pse_reset
Controls the resetting of the PSE state diagram. Condition that is TRUE until such time as the power supply for the device that implements the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE functionality.

valid_class
TRUE: valid class information was received from the PD during SCCP.

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FALSE: valid class information was not received from the PD during SCCP.

vsleep_valid

TRUE: V_{PSE} is in the range of V_{Sleep}.
FALSE: V_{PSE} is outside the range of V_{Sleep}.

vsig_valid

TRUE: a valid PD signature has been detected as defined in 104.4.5.2 and 104.4.5.3.
FALSE: an invalid PD signature has been detected as defined in 104.4.5.2 and 104.4.5.3.

Table 104–4—PSE power_available matrix for PSE and PD for classes 0 through 9

			PSE Class[a]									
			12V unreg		12V reg		24V unreg		24V reg		48V reg	
			0	1	2	3	4	5	6	7	8	9
PD Class[a]	12V unreg	0	x	x	x	x	—	—	—	—	—	—
		1	—	x	x	x	—	—	—	—	—	—
	12V reg	2	—	—	x	x	—	—	—	—	—	—
		3	—	—	—	x	—	—	—	—	—	—
	24V unreg	4	—	—	—	—	x	x	x	x	—	—
		5	—	—	—	—	—	x	x	x	—	—
	24V reg	6	—	—	—	—	—	—	x	x	—	—
		7	—	—	—	—	—	—	—	x	—	—
	48V reg	8	—	—	—	—	—	—	—	—	x	x
		9	—	—	—	—	—	—	—	—	—	x

[a]An ‘x’ denotes a valid PSE to PD Class pairing.

Table 104–5—PSE power_available matrix for PSE and PD for classes 10 through 15

			PSE Class[a]						
			Classes 0 to 9	30V reg			58V reg		
				10	11	12	13	14	15
PD Class[a]	Classes 0 to 9		See Table 104–4	—	—	—	—	—	—
	30V reg	10	—	x	x	x	—	—	—
		11	—	—	x	x	—	—	—
		12	—	—	—	x	—	—	—
	58V reg	13	—	—	—	—	x	x	x
		14	—	—	—	—	—	x	x
		15	—	—	—	—	—	—	x

[a]An ‘x’ denotes a valid PSE to PD Class pairing.

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104.4.4.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops counting upon entering a state where “stop x_timer” is asserted.

tclass_timer
: A timer used to limit the time allowed for classifying a PD (see T_{Class} in Table 104–7).

tdet_timer
: A timer used to limit the time allowed for attempting to detect a PD (see T_{det} in Table 104–6).

tod_timer
: A timer used to regulate a subsequent attempt to power a PD after an overload condition that causes a fault (see T_{od} in Table 104–7).

tinrush_timer
: A timer used to limit the duration of the inrush event (see T_{Inrush} in Table 104–7).

tmfvdo_timer
: A timer used to monitor the dropout of MFVS (see T_{MFVDO} in Table 104–7).

toff_timer
: A timer used to limit the time the PSE attempts to discharge the PI to the range of V_{Sleep} (see T_{OFF} in Table 104–7). If toff_timer expires during the SETTLE_SLEEP state, an overload condition exists, and the port state diagram enters the OVERLOAD state.

trestart_timer
: A timer used to regulate a subsequent attempt to power a PD after an error condition that does not result in a fault (see $T_{Restart}$ in Table 104–7).

vsig_hold_timer
: A timer used to de-glitch the PD signature voltage valid output in the detection state diagram (see T_{sig_hold} in Table 104–6).

104.4.4.5 Functions

do_classification

This function returns the following variables:

CLASS_TYPE_INFO register:
: Refer to Table 104–13 for a description of the contents.

VOLT_INFO register:
: PSEs that support cable resistance measurement also return the VOLT_INFO register. Refer to Table 104–14 for a description of the contents.

POWER_INFO register:
: PSEs that support cable resistance measurement also return the POWER_INFO register. Refer to Table 104–15 for a description of the contents.

POWER_ASSIGN register:
: PSEs that support cable resistance measurement also return the POWER_ASSIGN register. Refer to Table 104–16 for a description of the contents.

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104.4.4.6 State diagram

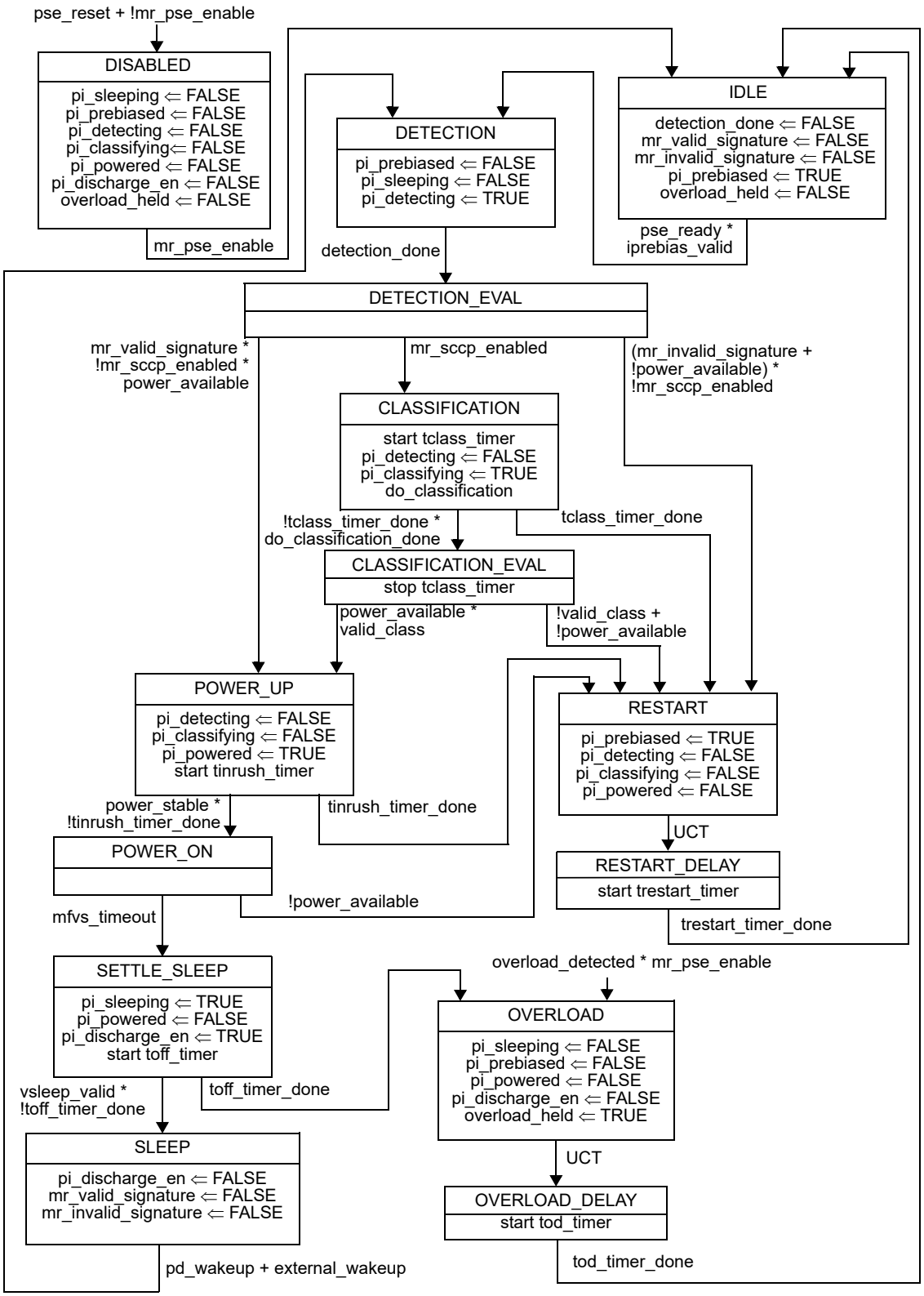

Figure 104–4—PSE state diagram

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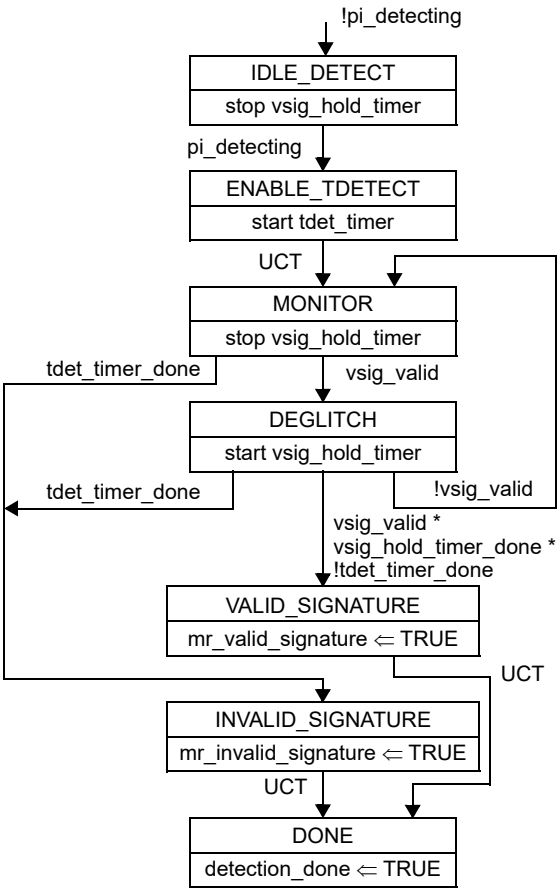

Figure 104–5—Detection state diagram

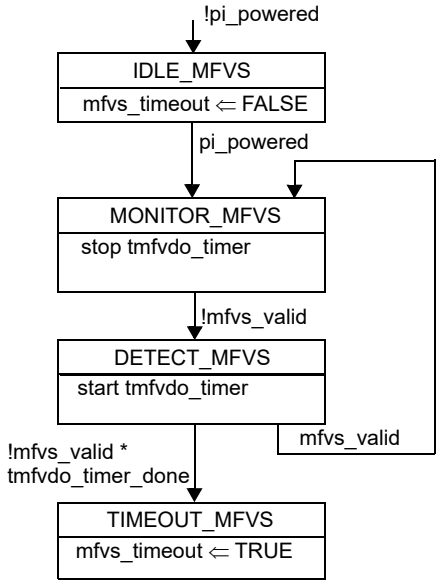

Figure 104–6—MFVS state diagram

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104.4.5 PSE detection of a PD

When in the DETECTION state, the PSE shall complete detection of a valid PD signature within T_{det} as specified in Table 104–6. If a valid signature is not detected and classification is not performed, the PSE shall wait at least $T_{Restart}$ before reattempting detection. If a valid signature is detected and classification is not performed, the PSE may proceed to the POWER_UP state. A PSE may successfully detect a PD but then opt not to power the detected PD.

104.4.5.1 Detection probe requirements

All detection currents at the PI shall be within the I_{valid} current range, as specified in Table 104–6, when connected to a valid PD detection signature as specified in Table 104–9. The detection probe shall conform to V_{OC}, I_{SC}, I_{slew}, and C_{out} as specified in Table 104–6.

Table 104–6—PSE PI detection state electrical output requirements

Item	Parameter	Symbol	Unit	Min	Max	Type	Additional information
1	Open circuit voltage	V_{OC}	V	4.75	5.5	All	
2	Short-circuit current	I_{SC}	mA	—	24	All	
3	Valid test probe current	I_{valid}	mA	9	16	All	
4	Slew rate	I_{slew}	A/ms	—	1	All	
5	Output capacitance during detection	C_{out}	µF	—	2.64	A, B, C, D	
					0.4	E	
6	Maximum detection time	T_{det}	ms	—	3.11	All	See 104.4.5
7	Valid PD detection signature range measured at PSE PI	V_{good_PSE}	V	4.05	4.7	All	See 104.4.5.2
8	Invalid PD detection signature high range measured at PSE PI	$V_{bad\_hi\_PSE}$	V	V_{oc}–0.05	—	All	See 104.4.5.3
9	Invalid PD detection signature low range measured at PSE PI	$V_{bad\_lo\_PSE}$	V	—	3.7	All	
10	Signature hold timer for validity	T_{sig_hold}	ms	1	—	All	See 104.4.5.2

104.4.5.2 Detection criteria

A PSE shall accept as a valid PD signature a link segment with a voltage in the range of V_{good_PSE} for at least T_{sig_hold} in response to a probing current in the range I_{valid} as specified in Table 104–6.

104.4.5.3 Rejection criteria

The PSE shall reject link segments as having an invalid PD signature when those link segments exhibit any of the following characteristics with a probe current, as specified in Table 104–6:

a) Voltage less than or equal to $V_{bad\_lo\_PSE}$ max
b) Voltage greater than or equal to $V_{bad\_hi\_PSE}$ min

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A PSE may accept or reject a voltage in the band between $V_{bad\_lo\_PSE}$ max and V_{good_PSE} min and in the band between V_{good_PSE} max and $V_{bad\_hi\_PSE}$ min. The values of these voltages are specified in Table 104–6.

104.4.6 PSE classification of a PD

The ability for the PSE to query the PD in order to determine the PD type and power class requirements of that PD is called classification.

Classification is optional, and is performed using SCCP. See 104.7.

A PSE with SCCP enabled shall complete classification after detection and prior to application of full operating voltage at the PI in a time less than T_{Class} as specified in Table 104–7. If classification is not completed before the T_{Class} timer expires, a new detection cycle shall be completed before any subsequent application of full operating voltage, the PSE shall transition to the RESTART state.

Valid class information is one that returns one of the defined bit patterns in Table 104–13 with a valid CRC8 result.

104.4.7 PSE output requirements

When the PSE provides power to the PSE PI, it shall conform to the electrical limits in Table 104–7.

Under all conditions, a PSE shall present an invalid PD signature with one of the attributes as specified in Table 104–10.

Table 104–7—PSE output requirements

Item	Parameter	Symbol	Unit	Min	Max	Class	Type	Additional information
1	DC output voltage during POWER_ON state	$V_{PSE(PON)}$	V	Class $V_{PSE(min)}$	Class $V_{PSE(max)}$	All	All	See 104.4.7.1 and Table 104–1
2	Continuous output current capability in POWER_ON state		mA	P_{Class}/V_{PSE}	—	All	All	See Table 104–1
3	Output slew rate dV/dt		V/ms	—	22	All	A, C	See 104.4.7.3
				—	2	All	E	See 104.4.7.3
				—	40	All	A, C, E	During inrush only
				—	200	All	B, F	See 104.4.7.3

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Table 104–7—PSE output requirements *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Class	Type	Additional information
4	Power feeding ripple and noise:							
4a	1 kHz < f < 10 MHz		V_{p-p}	—	0.1	All	A, B, C, D, E	See 104.4.7.3
					0.066		F	
4b	1 kHz < f < 10 MHz			—	0.01	All	A, B, C, D, E	
					0.0066		F	
5	Output current —at short-circuit condition	I_{LIM}	mA	$I_{PI(max)}$	1.41 × $I_{PI(max)}$	All	All	See 104.4.7.2.1
6	Short-circuit time limit	T_{LIM}	ms	10	75	Classes 0 to 9	All	
				50	75	Classes 10 to 15		
7	Inrush time	T_{Inrush}	ms	3.17	3.87	Classes 0 to 9	All	See 104.4.7.4
				50	75	Classes 10 to 15		
8	Classification time	T_{Class}	ms	—	366	Classes 0 to 9	All	See 104.4.6
					1300	Classes 10 to 15		
9	Turn off time	T_{OFF}	ms	—	500	All	All	See 104.4.7.5
10	DC output voltage during SLEEP state	V_{Sleep}	V	3.15	3.575	All	All	See 104.4.7.1 and 104.4.7.5
11	Overload delay timing	T_{od}	ms	750	—	All	All	
12	Restart timer delay	$T_{Restart}$	ms	500	—			
13	PD MFVS dropout time limit	T_{MFVDO}	ms	300	400			See 104.4.8.1
14	MFVS window time limit	T_{MFVS}	ms	6	—			
15	MFVS current threshold	I_{Hold}	mA	2.5	10			

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Table 104–7—PSE output requirements *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Class	Type	Additional information
16	Valid wakeup current signature range	I_{Wakeup}	mA	1.25	1.85	All	All	See 104.4.7.2.2
17	Wakeup current hold time required for validity	T_{Wakeup}	ms	0.1	—			
18	Invalid wakeup current signature high range	$I_{Wakeup\_bad\_hi}$	mA	2.5	—			
19	Invalid wakeup current signature low range	$I_{Wakeup\_bad\_lo}$	mA	—	0.5			
20	Output discharge current during SETTLE_SLEEP state	$I_{discharge}$	mA	1.2	24	All	All	See 104.4.7.2
21	DC output voltage during the DISABLED, OVERLOAD, and OVERLOAD_DELAY states	$V_{Disable}$	V	—	1	All	All	See 104.4.7.1
22	Disable time	$T_{Disable}$	ms	—	500	All	All	See 104.4.7.6

104.4.7.1 Output voltage

A PSE operating in the POWER_ON state shall apply a voltage in the range of $V_{PSE(PON)}$ at the PI. A PSE shall apply a voltage at the PI in the range of $V_{Disable}$ when in the OVERLOAD, OVERLOAD_DELAY, and DISABLED states (see 104.4.7.5).

The PSE shall apply a voltage at the PI in the range of V_{Sleep} while operating in the SLEEP, RESTART, RESTART_DELAY, and IDLE states (see Table 104–7).

A PSE operating in the SETTLE_SLEEP state shall discharge the PSE PI to the range of V_{Sleep} within a time less than T_{OFF} max.

104.4.7.2 Output current

A PSE operating in the POWER_ON state shall enter the SETTLE_SLEEP state if a valid MFVS is not present at the PI.

A PSE operating in the SETTLE_SLEEP state shall discharge the PI to the range of V_{Sleep} with a current in the range of $I_{discharge}$.

During the POWER_UP state, PSE output shall not exceed I_{LIM} max.

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104.4.7.2.1 Output current—at overload condition

During operation in the POWER_UP and POWER_ON states, the PSE shall limit the current to I_{LIM} for a duration of up to T_{LIM} in order to account for PSE dV/dt transients at the PI as specified in Table 104–7.

If I_{PSE} exceeds I_{LIM} min during the POWER_ON state, the PSE output voltage may drop below $V_{PSE(PON)}$ min.

During operation in any state other than POWER_UP or POWER_ON when the PSE is enabled, the PSE shall limit I_{PSE} to less than I_{SC} as specified in Table 104–6 for a duration of up to T_{LIM}.

If the PSE is limiting current in any state when pi_powered, pi_sleeping or pi_prebias are true, within T_{LIM} of the initiation of current limiting, overload_detected is set TRUE and power removal from the PI shall begin.

Measurements of I_{PSE} during a short-circuit condition shall be made 1 ms after the initial transient to allow for settling.

104.4.7.2.2 Wakeup current signature detection

A PSE shall transition from the SLEEP state to the DETECTION state when I_{PSE} is in the valid range of I_{Wakeup} for a minimum of T_{Wakeup} (see Table 104–7).

A PSE operating in the SLEEP state shall remain in the SLEEP state if I_{PSE} is greater than $I_{Wakeup\_bad\_hi}$ or less than $I_{Wakeup\_bad\_lo}$. A PSE may consider a PD wakeup request valid or invalid if I_{PSE} is in the band between $I_{Wakeup\_bad\_hi}$ and I_{Wakeup} max or the band between I_{Wakeup} min and $I_{Wakeup\_bad\_lo}$.

104.4.7.2.3 Output current requirement during idle

The PSE output current during the IDLE state shall be defined as valid if it less than I_{Wakeup} max for at least T_{Wakeup} min (see Table 104–7). A PSE may define its output current during the IDLE state as valid if the current is in the range between I_{Wakeup} max and $I_{Wakeup\_bad\_hi}$ for at least T_{Wakeup} min.

A PSE may define its output current during the IDLE state as invalid if the current is in the range between I_{Wakeup} max and $I_{Wakeup\_bad\_hi}$. A PSE shall consider its output current during the IDLE state to be invalid if the current is greater than $I_{Wakeup\_bad\_hi}$.

104.4.7.3 Power feeding ripple and transients

The ripple and transient limits specified in Table 104–7, items (4) and (3) respectively, are meant to preserve data integrity.

A digital oscilloscope or data acquisition module with a differential probe is used to observe the voltage at the MDI/PI of the PSE device under test (DUT) as shown in Figure 104–7. The input impedance, $Z_{in}(f)$, and transfer function, $H_1(f)$, of the differential probe are specified by Equation (104–1) and Equation (104–2), respectively. When measuring the ripple voltage for a Type A or Type C PSE as specified by Table 104–7 item (4a), f_1 = 31.8 kHz ± 1%. When measuring the ripple voltage for a Type B or Type F PSE as specified in Table 104–7 item (4a), f_1 = 318 kHz ± 1%. When measuring the ripple voltage for a Type E PSE as specified in Table 104–7 item (4a), f_1 = 3.18 kHz ± 1%.

$$Z_{in}(f) = \left(100 \pm 0.1\% \times \frac{\sqrt{f^2 + f_1^2}}{f}\right) \Omega \quad (104–1)$$

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$$H_1(f) = \frac{f}{\sqrt{f^2 + f_1^2}} \quad (104–2)$$

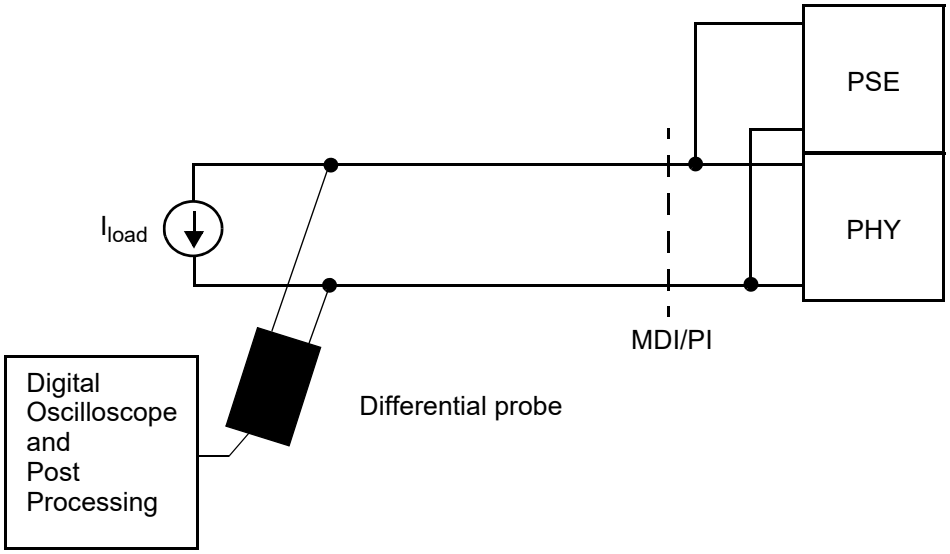

Figure 104–7—PSE ripple voltage test fixture

When measuring the ripple voltages for a Type A or Type C PSE as specified by Table 104–7 item (4b), the voltage observed at the MDI/PI with the differential probe where f_1 = 31.8 kHz ± 1% is post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 1 MHz ± 1%.

When measuring the ripple voltages for a Type B or Type F PSE as specified by Table 104–7 item (4b), the voltage observed at the MDI/PI with the differential probe where f_1 = 318 kHz ± 1% is post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 10 MHz ± 1%.

When measuring the ripple voltages for a Type E PSE as specified by Table 104–7 item (4b), the voltage observed at the MDI/PI with the differential probe where f_1 = 3.18 kHz ± 1% is post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 0.1 MHz ± 1%.

$$H_2(f) = \frac{f}{\sqrt{f^2 + f_2^2}} \quad (104–3)$$

104.4.7.4 Inrush time

The specification for T_{Inrush} in Table 104–7 applies to the PSE power-up time allowed for a PD after completion of detection and optional classification. If full operating voltage is applied within T_{Inrush} min, the PSE shall enter the POWER_ON state. If full operating voltage is not applied within T_{Inrush} max, a new detection cycle shall be initiated after a delay of $T_{Restart}$ before any subsequent application of full operating voltage. If full operating voltage is applied within the range of T_{Inrush}, the PSE may enter the POWER_ON state or begin a new detection cycle after a delay of $T_{Restart}$.

104.4.7.5 Turn off time

The specification for T_{OFF} in Table 104–7 applies to the discharge time from V_{PSE} in the POWER_ON state to V_{Sleep}. In addition, it is recommended that the PI be discharged when the PSE is not enabled. T_{OFF} starts when V_{PSE} drops 1 V below the steady-state full operating voltage value after the pi_powered variable is set to FALSE. T_{OFF} ends when $V_{PSE} < V_{Sleep}$ max.

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104.4.7.6 Disable time

The specification for $T_{Disable}$ in Table 104–7 shall apply to the discharge time from V_{PSE} to $V_{Disable}$ with a test resistor of 320 kΩ attached to the PI. $T_{Disable}$ starts when V_{PSE} drops 1 V below the steady-state value after the pi_powered, pi_classifying, pi_detecting, pi_prebiased, and pi_sleeping variables are set to FALSE (see Figure 104–4). $T_{Disable}$ ends when V_{PSE} is less than or equal to $V_{Disable}$ max.

104.4.7.7 Continuous output power in POWER_ON state

P_{Class} is the minimum continuous class power that the PSE shall be capable of supplying, as defined in Table 104–1.

Measurement of P_{Class} shall be averaged using a uniform sliding window with a width of 1 s.

A PSE may remove power from the PI when more than P_{Class} is sourced.

104.4.8 PSE power removal

While the PSE is operating in the POWER_ON state, full operating voltage shall be removed from the PSE PI in the absence of the PD MFVS or if overload_detected is TRUE.

104.4.8.1 PSE MFVS requirements

MFVS shall be defined as being present in the POWER_ON state when I_{PSE} is greater than or equal to I_{Hold} max for a minimum of T_{MFVS}.

MFVS may be defined as present or absent in the POWER_ON state if I_{PSE} is in the range of I_{Hold}.

MFVS shall be defined as absent in the POWER_ON state if I_{PSE} is less than or equal to I_{Hold} min. The PSE-PI Voltage shall be reduced to the range of V_{Sleep} when MFVS has been absent for a duration greater than T_{MFVDO}.

104.5 Powered Device (PD)

A PD is the portion of a device that is either drawing power or requesting power by participating in the PD detection or classification algorithms. A device that is capable of becoming a PD may have the ability to draw power from an alternate power source. A PD requiring power from the PI may simultaneously draw power from an alternate power source.

A PD is specified at the point of the physical connection to the PI. Limits defined for a PD are specified at the PI, not at any point internal to the PD, unless specifically stated.

104.5.1 PD types

For PoDL systems there are six types of PDs—Type A, Type B, Type C, Type D, Type E, and Type F consistent with 104.1.3.

104.5.2 PD PI

A PD may receive power in two modes, Mode A and Mode B. Table 104–8 in conjunction with Figure 104–3 illustrates the PD pinout.

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Table 104–8—PD pinout

Contact	Mode A	Mode B
1	PI+	PI–
2	PI–	PI+

Class 0 to class 9 PDs shall be able to operate per the Mode A column in Table 104–8. Class 10 to class 15 PDs shall be implemented to be insensitive to the polarity of the power supply and shall be able to operate per the Mode A column and the Mode B column in Table 104–8.

104.5.3 PD classes

A PD shall comply with the voltage and power requirements listed in Table 104–1 for the relevant class.

104.5.4 PD state diagram

The PD state diagram specifies the externally observable behavior of a PD. The PD shall provide the behavior of the state diagram shown in Figure 104–8.

104.5.4.1 Overview

A falling edge of the PD input voltage through V_{sig_enable} enables a voltage signature, as defined in 104.5.5. When the input voltage rises through the $V_{sig\_disable}$ the PD disables its voltage signature.

A PD requests detection and wakeup while the voltage signature is enabled by presenting a valid wakeup current signature. SCCP may also be used for communication with the PD by the PSE when the voltage signature is enabled.

A rising edge through the V_{On} threshold causes the PD to enable MDI power to the load after a delay of T_{power_dly}. A falling edge through the V_{Off} threshold causes the PD to disable MDI power.

104.5.4.2 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in 21.5.

104.5.4.3 Variables

The PD state diagram uses the following variables:

disconnect_pd
: TRUE: the PD no longer requires full operating voltage from the PI and has reduced its port current below the MFVS threshold current.
: FALSE: the PD still requires full operating voltage from the PI.

enable_mdi_pwr
: TRUE: the PD is enabled and ready to consume full power from the PI.
: FALSE: the PD is disabled or not ready to consume full power from the PI.

fault_detected
: TRUE: the PD no longer requires power as the result of an implementation-specific error condition.
: FALSE: no fault has been detected.

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pd_fault
TRUE: following the application of full operating voltage at the PI, the PD has gone offline as the result of an error condition.
FALSE: following the application of full operating voltage at the PI, no fault has been detected.

pd_sccp_enabled
TRUE: during detection, a PSE reset pulse has been detected by the PD and a SCCP serial transaction is pending.
FALSE: during detection, no PSE reset pulse has been detected by the PD.

pd_reset
An implementation-specific control variable that unconditionally resets the PD state diagram to the RESET state.
TRUE: the device is in reset.
FALSE: the device is not in reset (default).

present_det_sig
A variable that controls the PD detection signature as specified in 104.5.5.
TRUE: the detection signature is to be applied to the PD PI.
FALSE: the detection signature is not to be applied to the PD PI.

present_iwakeup
TRUE: the wakeup signature (I_{Wakeup_PD}) is to be applied to the PD PI.
FALSE: the wakeup signature (I_{Wakeup_PD}) is not to be applied to the PD PI.

present_mfvs
TRUE: the MFVS is to be applied to the PD PI.
FALSE: the MFVS is not to be applied to the PD PI.

sccp_reset_pulse
TRUE: during detection, a SCCP reset pulse per Figure 104–10 as described in 104.7.1.1 has been received by the PD.
FALSE: during detection, a SCCP reset pulse has not been received by the PD.

V_{Off}
PD turn off threshold voltage (see Table 104–11).

V_{On}
PD turn on threshold voltage (see Table 104–11).

V_{PD}
The voltage measured at the PI of the PD.

$V_{sig\_disable}$
PD signature disable threshold voltage (see Table 104–9).

V_{sig_enable}
PD signature enable threshold voltage (see Table 104–9).

wakeup
TRUE: the PD requires the full operating voltage at the PI.
FALSE: the PD is ready to go to sleep.

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104.5.4.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where “stop x_timer” is asserted.

tpower_dly_timer
: A timer used to prevent a PD from drawing more than inrush current during the PSE’s POWER_UP state (see T_{power_dly} in Table 104–11).

sccp_watchdog_timer
: A timer used to limit the time in the DO_CLASSIFICATION state in the event serial communication between the PSE and PD is idle or stalled (see $T_{SCCP\_watchdog}$ in Table 104–11).

104.5.4.5 Functions

do_sccp

This function returns the following variable to the PSE:

CLASS_TYPE_INFO register:
: Refer to Table 104–13 for a description of the contents.

VOLT_INFO register:
: PDs that support cable resistance measurement also return the VOLT_INFO register. Refer to Table 104–14 for a description of the contents.

POWER_INFO register:
: PDs that support cable resistance measurement also return the POWER_INFO register. Refer to Table 104–15 for a description of the contents.

POWER_ASSIGN register:
: PDs that support cable resistance measurement also return the POWER_ASSIGN register. Refer to Table 104–16 for a description of the contents.

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104.5.4.6 State diagram

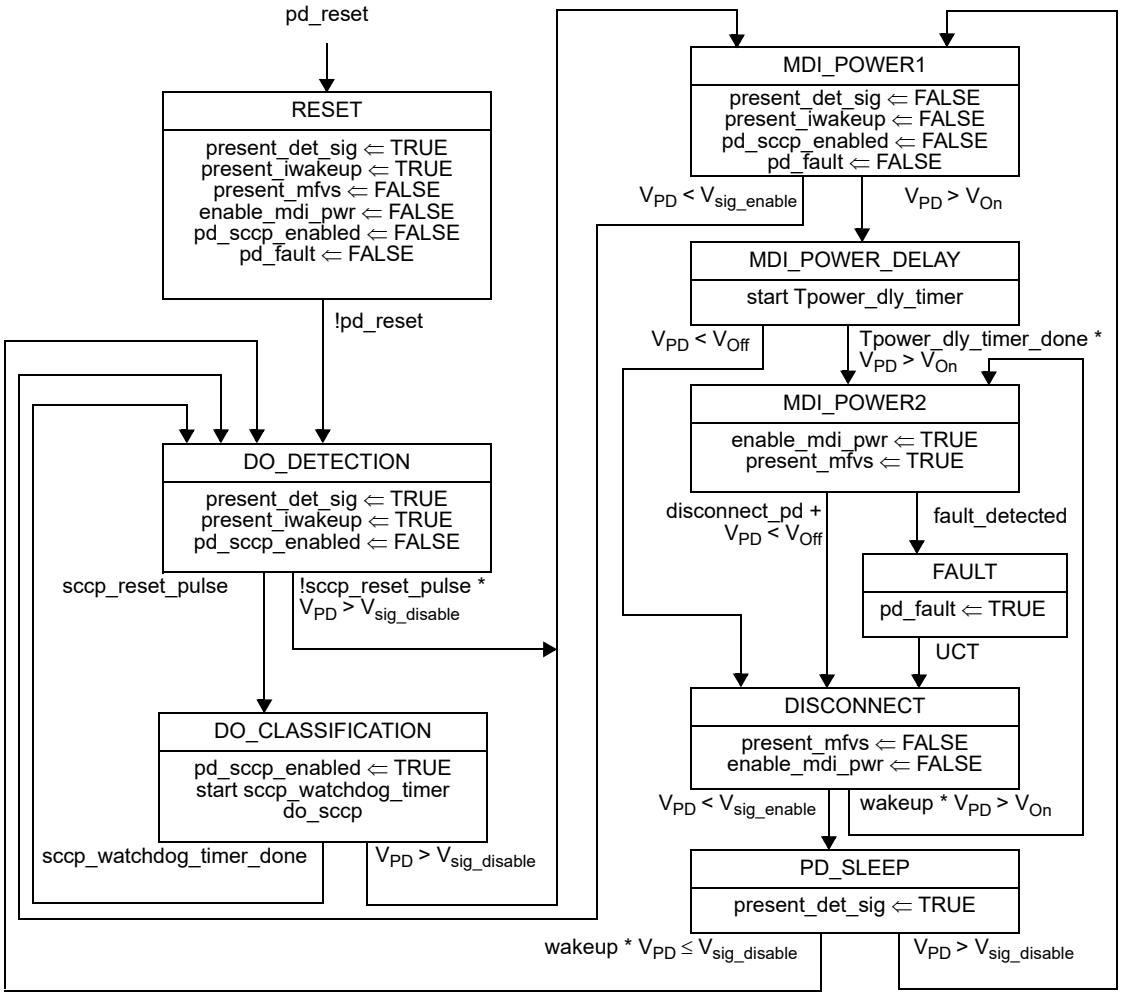

Figure 104–8—PD state diagram

104.5.5 PD signature

Class 0 and Class 1 PDs, or PDs that do not implement classification shall enable a valid detection signature when V_{PD} is less than V_{sig_enable} min and may enable a valid detection signature when V_{PD} is less than V_{sig_enable} max. A PD that presents an invalid detection signature greater than V_{bad_hi} max as specified in Table 104–10 shall implement classification as specified in 104.7.

When V_{PD} is greater than $V_{sig\_disable}$ a PD shall remove the current draw of the detection signature.

The detection signature shall consist of a current limited voltage V_{good} per Table 104–9 when measured by the PSE.

A valid PD detection signature shall have all of the characteristics of Table 104–9.

A non-valid PD detection signature shall have one of the characteristics in Table 104–10.

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A PD that presents a signature within the limits set out in Table 104–9 is assured to pass detection, while a PD that presents one of the signature characteristics of Table 104–10 is assured to fail detection.

Table 104–9—Valid PD detection signature characteristics, measured at PD PI

Parameter	Conditions	Min	Max	Unit
V_{good}	7 mA < I_{PD} < 17 mA, PD exiting RESET state	4.05	4.55	V
$I_{signature\_limit}$	V_{PD} < $V_{sig\_disable}$ max	—	24	mA
$V_{sig\_disable}$	V_{PD} rising	4.6	5.75	V
V_{sig_enable}	V_{PD} falling	3.6	4.3	V

Table 104–10—Non-valid PD detection signature characteristics, measured at PD PI

Parameter	Conditions	Min	Max	Unit
V_{bad_hi}	7 mA < I_{PD} < 17 mA, PD exiting RESET state	5.15	—	V
V_{bad_lo}	7 mA < I_{PD} < 17 mA, PD exiting RESET state	—	3.7	V

104.5.6 PD classification and mutual identification between the PSE and PD

A PD may be classified by the PSE based on SCCP information provided by the PD. The intent of PD classification is to provide information about the voltage and power required by the PD during operation. SCCP classification may also be used to establish mutual identification between a PSE and a PD. See 104.7 for more information about SCCP.

104.5.7 PD power

The PD shall operate within the characteristics in Table 104–11.

Table 104–11—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
1	Input current dI/dt		A/ms	—	1	A, C	See 104.5.7.4
				—	10	B	
				—	0.1	E	
2	Input voltage dV/dt		V/ms	—	20	A, C	
				—	200	B	
				—	2	E	

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Table 104–11—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
3	Ripple voltage						
3a	1 kHz < f < 10 MHz		V_{p-p}	—	0.1	A, B, C, D, E	See 104.5.7.4
					0.066	F	
3b	1 kHz < f < 10 MHz			—	0.01	A, B, C, D, E	
					0.0066	F	
4a	Power supply turn on voltage (unregulated 12 V classes)	V_{On}	V	—	5.75	All	See 104.5.7.2
4b	Power supply turn on voltage (regulated 12 V classes)			—	13.6		
4c	Power supply turn on voltage (unregulated 24 V classes)			—	11.4		
4d	Power supply turn on voltage (regulated 24 V classes)			—	24.7		
4e	Power supply turn on voltage (regulated 48 V classes)			—	45.6		
4f	Power supply turn on voltage (Classes 10, 11, and 12)			—	19.2		
4g	Power supply turn on voltage (Classes 13, 14, and 15)			—	49		
5a	Power supply turn off voltage (unregulated 12 V classes)	V_{Off}	V	3.6	—		
5b	Power supply turn off voltage (regulated 12 V classes)			9.56	—		
5c	Power supply turn off voltage (unregulated 24 V classes)			7.97	—		
5d	Power supply turn off voltage (regulated 24 V classes)			19.5	—		
5e	Power supply turn off voltage (regulated 48 V classes)			33	—		
5f	Power supply turn off voltage (Classes 10, 11, and 12)			11.2	—		
5g	Power supply turn off voltage (Classes 13, 14, and 15)			28	—		

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Table 104–11—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
6a	Input Capacitance during DO_DETECTION, MDI_POWER1, and MDI_POWER_DELAY states	C_{IN}	μF	—	10	All	Classes 1 to 3 and 5 to 9
				—	5		Class 4
6b	Input capacitance during DO_CLASSIFICATION state	C_{IN_Class}		—	0.2	A, B, C, D	All classes
				—	0.4	E	
7	Inrush enable delay time (Classes 0 to 9)	T_{power_dly}	ms	1.46	—	All	See 104.5.7.2
	Inrush enable delay time (Classes 10 to 15)			80	—		
8	PD MFVS duration	T_{MFVS_PD}	ms	10	—	All	See 104.5.8
9	MFVS current threshold limit	I_{hold_PD}	mA	11	—		
10	Power supply voltage during PD_SLEEP state	V_{Sleep_PD}	V	3.1	3.575		See 104.5.7.2
11	Sleep current	I_{Sleep_PD}	mA	—	0.1		See 104.5.7.3
12	Wakeup current	I_{Wakeup_PD}	mA	1.3	1.8		See 104.5.7.3
13	Input current not related to inrush	I_{PD_pwr1}	mA	—	5		See 104.5.7.3
14	Wakeup current hold time required for validity	T_{Wakeup_PD}	ms	0.2	—		See 104.5.7.3
15	SCCP watchdog timeout	$T_{SCCP\_watchdog}$	ms	150	200	A, B, C, D	See 104.5.6
				1000	1300	E	

104.5.7.1 PD discharge

At a delay of T_{OFF} max (see Table 104–7) after disconnection from the PSE, a PD shall not source greater than 410 μJ out of its PI until V_{PD} drops below V_{Sleep_PD} max.

104.5.7.2 PD input voltage

The PD shall turn on at a voltage less than or equal to V_{On} max and with a delay greater than T_{power_dly} min. After the PD turns on, the PD shall stay on over the range from V_{PD} min to V_{PSE} max. The PD shall turn off at a voltage in the range of V_{PD} min to V_{Off} min. Table 104–1 defines the values for V_{PD} min and V_{PSE} max. Table 104–11 defines the values for V_{On}, T_{power_dly}, and V_{Off}.

The PD shall turn on or off without startup oscillation and within the first trial when a voltage in the range of V_{PSE} (as defined in Table 104–1) is applied with a series resistance within the range of valid dc loop resistance (see 104.2).

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The PD shall operate in the PD_SLEEP state with an input voltage greater than V_{Sleep_PD} min as specified in Table 104–11.

When the input voltage is greater than $V_{sig\_disable}$, then the signature is disabled.

104.5.7.3 Input current

During operation in the DISCONNECT and PD_SLEEP states, the PD shall not draw current in excess of I_{Sleep_PD} as specified in Table 104–11.

A PD that requires detection and application of power shall draw current in the range of I_{Wakeup_PD} for at least T_{Wakeup_PD} when V_{PD} is within the range of V_{Sleep_PD} as specified in Table 104–11.

A PD shall draw less than I_{PD_pwr1} max of current for a constant PD input voltage between $V_{sig\_disable}$ max and V_{On} min.

104.5.7.4 PD ripple and transients

The specifications for ripple and transients in Table 104–11 apply to the voltage or current at the PD PI generated by the PD circuitry. Ripple and transient limits are provided to preserve data integrity.

The PD DUT is connected to a power supply through a dc bias coupling network as shown in Figure 104–9. The ripple and transient specifications for a Type A or Type C PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Equation (96–12), and over the range of P_{PD}. The ripple and transient specifications for a Type B PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 97, and over the range of P_{PD}. The ripple and transient specifications for a Type E PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 146 and over the range of P_{PD}. The ripple and transient specifications for a Type F PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 149, and over the range of P_{PD}.

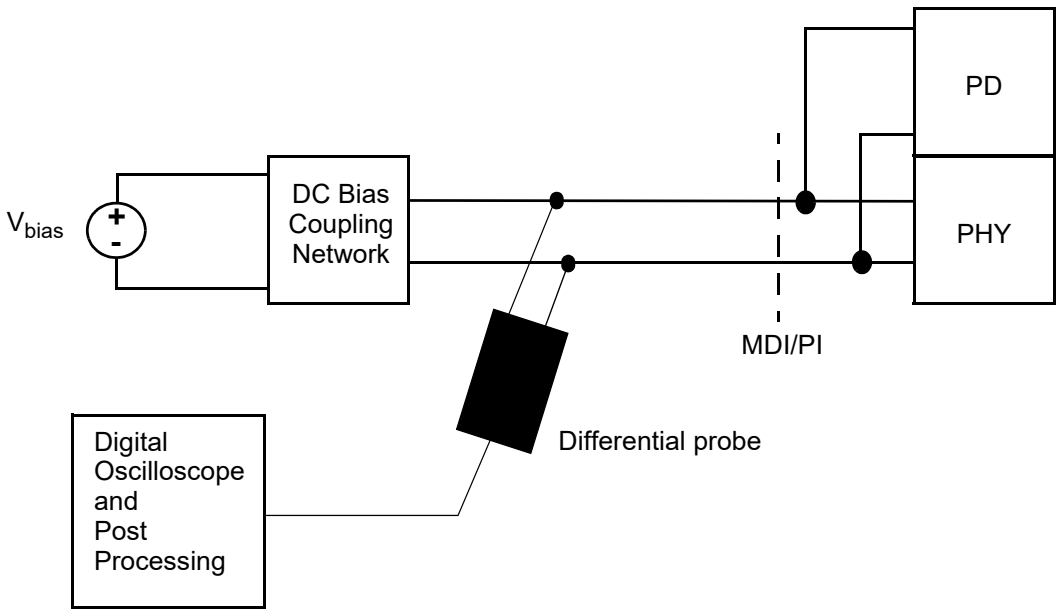

Figure 104–9—PD ripple voltage test fixture

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A digital oscilloscope or data acquisition module with a differential probe is used to observe the voltage at the MDI/PI. The input impedance, $Z_{in}(f)$, and transfer function, $H_1(f)$, of the differential probe are specified by Equation (104–1) and Equation (104–2), respectively. When measuring the ripple voltage for a Type A or Type C PD as specified by Table 104–11 item (3a), $f_1 = 31.8$ kHz ± 1%. When measuring the ripple voltage for a Type B or Type F PD as specified by Table 104–11 item (3a), $f_1 = 318$ kHz ± 1%. When measuring the ripple voltage for a Type E PD as specified by Table 104–11 item (3a), $f_1 = 3.18$ kHz ± 1%.

When measuring the ripple voltages for a Type A or Type C PD as specified by Table 104–11 item (3b), the voltage observed at the MDI/PI with the differential probe where $f_1 = 31.8$ kHz ± 1% shall be post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where $f_2 = 1$ MHz ± 1%. When measuring the ripple voltages for a Type B or Type F PD as specified by Table 104–11 item (3b), the voltage observed at the MDI/PI with the differential probe where $f_1 = 318$ kHz ± 1% shall be post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where $f_2 = 10$ MHz ± 1%. When measuring the ripple voltages for a Type E PD as specified by Table 104–11 item (3b), the voltage observed at the MDI/PI with the differential probe where $f_1 = 3.18$ kHz ± 1% shall be post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where $f_2 = 0.1$ MHz ± 1%.

104.5.7.5 Input average power

The maximum average power, $P_{PD(max)}$ in Table 104–1, shall be calculated using a uniform sliding window with a width of 1 s.

104.5.7.6 PD stability

When any voltage between V_{PSE} min and V_{PSE} max (with R_{Loop_max} in series) is applied to the PI of the PD, P_{PD} is defined as shown in Equation (104–4).

$$P_{PD} = (V_{PD} \times I_{PD}) \text{ (Watts)} \quad (104–4)$$

where

P_{PD} is the input power at the PD PI
V_{PD} is the input voltage at the PD PI
I_{PD} is the input current to the PD

NOTE—When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input.

104.5.8 PD Maintain full voltage

In order to signal the PSE to maintain full operating voltage, the PD shall provide a valid MFVS at the PI. The MFVS shall consist of current draw equal to or greater than I_{hold_PD} for a minimum duration of T_{MFVS_PD} measured at the PD PI followed by an allowed MFVS dropout for no longer than T_{MFVDO} min. PDs that do not require full operating voltage at the PI shall remove the current draw of the MFVS from the PI.

104.6 Additional electrical specifications

104.6.1 Isolation

In order to prevent the formation of a ground loop, a PD shall provide at least 1 MΩ dc isolation between all accessible external conductors, including frame ground (if any), and all MDI leads, when measured using a 5 V ± 20% source voltage. Any equipment that can be connected to a PD through a non-MDI connector that is not isolated from the MDI leads needs to provide isolation between all accessible external conductors,

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including frame ground (if any), and the non-MDI connector, so as not to negate the dc isolation provided by the PD.

104.6.2 Fault tolerance

The PI for Type A, Type B, Type C, and Type F PSEs and PDs shall meet the fault tolerance requirements as specified in 96.8.3. The PI for Type E PSEs and PDs shall meet the fault tolerance requirements as specified in 146.8.6.

A PD shall not be damaged when connected to any PSE as defined in 104.4.

The PSE PI shall withstand without damage the application of short circuits between the wires within the cable for an indefinite period of time.

104.7 Serial communication classification protocol (SCCP)

Implementation of SCCP by PSEs and PDs that present a valid detection signature is optional. PDs that present an invalid detection signature as specified in Table 104–10 shall implement SCCP. The PSE acts as a master during the SCCP exchange, controlling the PD that acts as the slave device. SCCP is a current-sinking, wired-OR (e.g., open-drain or open-collector), half-duplex bidirectional serial data bus. The PSE sources the required pull-up current. PDs can derive power from the PSE's pull-up current during classification via the PD PI.

Measurement of initial cable resistance, $R_{Cable\_initial}$, by PSEs and PDs that implement SCCP is optional. PSEs and PDs that implement cable resistance measurement support the VOLT_INFO, POWER_INFO, and POWER_ASSIGN registers (see Table 104–14, Table 104–15, and Table 104–16). PSEs that implement cable resistance measurement shall report assigned power through PoDL PSE Status 2 Register (see 45.2.9.3).

104.7.1 SCCP signaling

SCCP uses the following signal types in order to ensure data integrity: reset pulse, presence pulse, Write 0, Write 1, Read 0, and Read 1. The PSE initiates all of these signals.

104.7.1.1 Initialization procedure—reset and presence pulses

All SCCP communication with a PD shall begin with an initialization sequence that consists of a reset pulse from the PSE followed by a presence pulse from the PD. This is illustrated in Figure 104–10. See Table 104–12 for requirements on the timing relationships.

During the initialization sequence the PSE shall transmit the reset pulse by first driving V_{PSE} low and then releasing to the pull up at t_{RSTL}. The PSE shall then go into receive mode (RX). When the PD detects the rising edge at the PD PI, it shall wait t_{PDH} and then transmit a presence pulse by pulling V_{PD} low for t_{PDL}. Presence data from the PD shall be valid for the entire time window defined by t_{MSP} following the rising edge that terminated the reset pulse. Therefore, the PSE should sample the subsequent voltage within t_{MSP} from the completion of the preceding rising edge at its PI.

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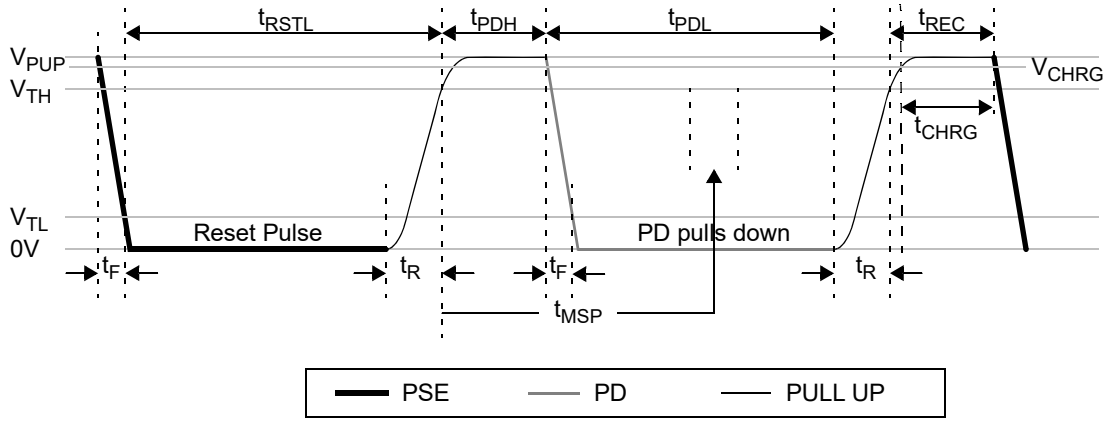

Figure 104–10—Reset command timing diagram

104.7.1.2 Write time slots

There are two types of write time slots: Write 1 and Write 0 time slots. Figure 104–11 illustrates Write 0/1 timing diagrams. The PSE shall use a Write 1 time slot to transmit a logic 1 to the PD and a Write 0 time slot to transmit a logic 0 to the PD. All write time slots shall be $t_{WRITESLOT}$ in duration. The PSE shall initiate both types of write time slots by pulling V_{PSE} low.

To generate a Write 1 time slot, after pulling V_{PSE} low, the PSE shall pull up V_{PSE} within the range of t_{W1L}. To generate a Write 0 time slot, after pulling the V_{PSE} low, the PSE shall pull up V_{PSE} within the range of t_{W0L}. The PD shall sample the V_{PD} within the range of t_{ssw} after the falling edge during a Write 1 or Write 0 operation.

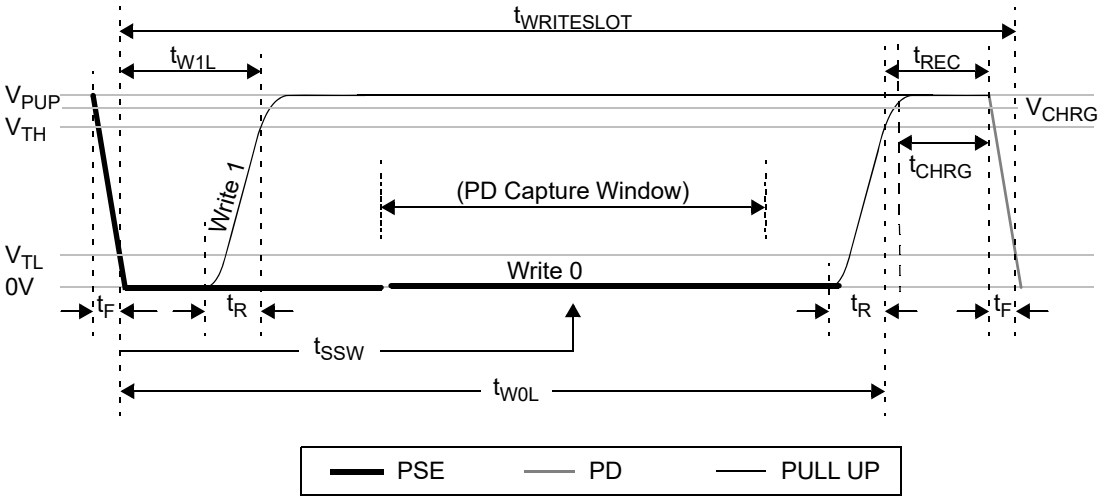

Figure 104–11—Write 0/1 slot timing diagram

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104.7.1.3 Read time slots

Figure 104–12 illustrates Read 0/1 timing diagrams. The PD can only transmit data to the PSE when the PSE issues read time slots. Therefore, the PSE shall generate read time slots immediately after issuing a function command, which requires data from the PD so that the PD can provide the requested data. In addition, the PSE can generate read time slots after issuing a manufacturer specific function command in order to determine the status of a commanded operation.

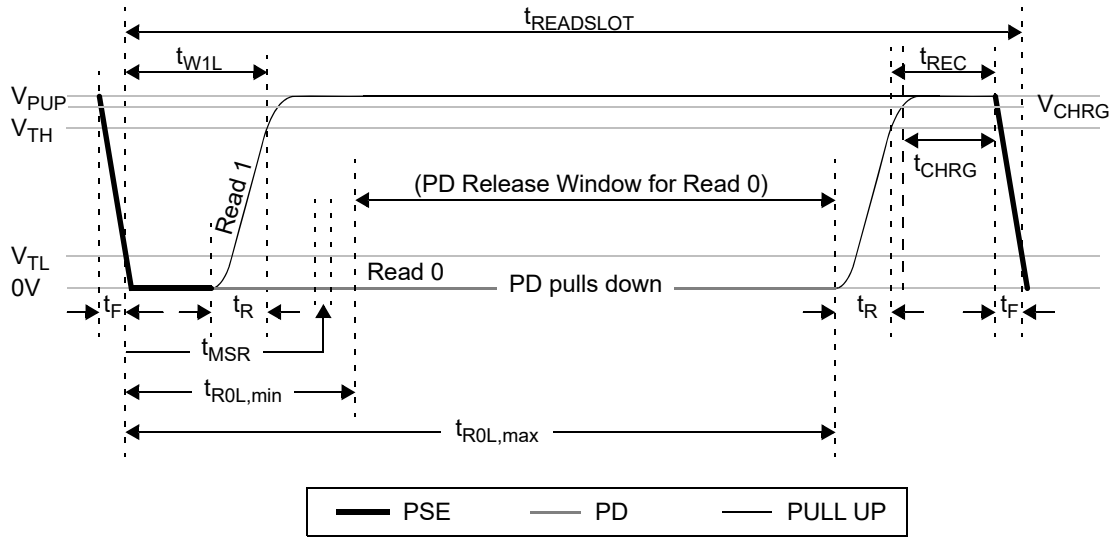

Figure 104–12—Read 0/1 slot timing diagram

All read time slots shall be $t_{READSLOT}$ in duration. The PSE shall initiate a read time slot by pulling V_{PSE} low and then pulling-up V_{PSE} within t_{W1L}. After the PSE initiates the read time slot, the PD shall begin transmitting a 1 or 0 at its PI. The PD shall transmit a 1 by leaving V_{PD} high and transmit a 0 by pulling V_{PD} low. When transmitting a 0, the PD shall hold V_{PD} low and then release V_{PD} within t_{R0L}. V_{PSE} and V_{PD} will be pulled back to the high idle state by the PSE's pull-up current. Output data from the PD is valid for t_{MSR} after the falling edge that initiated the read time slot. Therefore, the PSE shall release V_{PSE} and then sample the subsequent voltage within t_{MSR} from the start of the read time slot SCCP electrical requirements.

A PSE or PD implementing SCCP shall comply with the electrical and timing requirements in Table 104–12. All voltages are referenced to the PI, as shown in Figure 104–3. See Figure 104–10, Figure 104–11, and Figure 104–12 for timing definitions.

Table 104–12—SCCP electrical requirements

Item	Parameter	Symbol	Unit	Min	Max	PSE/PD Type	Additional information
1	PSE Pull-up Voltage (Classes 0 to 9)	V_{PUP}	V	$V_{good\_PSE\ max}$	5	All	See Table 104–6
	PSE Pull-up Voltage (Classes 10 to 15)				5.5		
2	PSE Pull-up Current	I_{PUP}	mA	9	16	All	

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Table 104–12—SCCP electrical requirements *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE/PD Type	Additional information
3	Input Logic High Voltage	V_{TH}	V	3	—	All	
4	Input Logic Low Voltage	V_{TL}	V	—	1	A, B, C, D, PSE/PD; E PD	
					2	E PSE	
5	Sink Current	I_L	mA	30	—	All	$V_{Port} > 0.8$ V
6a	Write Time Slot	$t_{WRITESLOT}$	ms	2.7	3.3	A, B, C, D	
				—	2.78	E	
6b	Read Time Slot	$t_{READSLOT}$	ms	2.7	3.3	A, B, C, D	
				—	3.83	E	
7	Recovery Time	t_{REC}	ms	0.27	0.33	All	
8	Write 0 Low Time	t_{W0L}	ms	1.8	2.2	All	
9	Write 1 Low Time	t_{W1L}	ms	0.08	0.25	A, B, C, D	
				0.09	0.61	E	
10	PD Sample Write Time	t_{SSW}	ms	0.5	1.5	A, B, C, D	
				0.77	1.43	E	
11	PSE Sample Read Time	t_{MSR}	ms	0.27	0.33	A, B, C, D	
				0.9	1.1	E	
12	Read 0 Low Time	t_{R0L}	ms	0.5	1.5	A, B, C, D	
				1.75	3.25	E	
13	Reset Time Low Time	t_{RSTL}	ms	9	11	A, B, C, D	
				8	10.5	E	
14	Presence-Detect High Time	t_{PDH}	ms	0.5	1.5	A, B, C, D	
				0.7	1.3	E	
15	Presence-Detect Low Time	t_{PDLOW}	ms	2.5	7.5	A, B, C, D	
				2.8	5.2	E	
				21	31	E	PDs that support link segment resistance measurement
16	PSE Sample Presence Time	t_{MSP}	ms	1.8	2.2	All	
17	Rise-Time	t_R	ms	0.025	0.105	A, B, C, D	
				0.025	0.5	E	

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Table 104–12—SCCP electrical requirements *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE/PD Type	Additional information
18	Fall-Time	t_F	ms	0.025	0.1	A, B, C, D	
				0.025	0.25	E	
19	Bus Capacitance	C_{BUS}	nF	—	6	A, B, C, D	
				—	80	E	
20	PD reservoir capacitor recharge voltage	V_{CHRG}	V	$0.9 \times V_{PUPmin}$	—	E	
21	PD reservoir capacitor recharge time	t_{CHRG}	ms	0.2	—	E	
22	Resistance margin factor	K_{RMF}	—	1.06	—	E	PSEs that support cable resistance measurement

104.7.1.4 Calculations for cable resistance

A PSE that implements cable resistance measurement may calculate cable resistance (dc loop resistance of the link segment) using the voltage and current at the PSE PI during the presence pulse and the voltage at the PD PI as shown in Equation (104–5). The measurement tolerances in the voltage and current values should be included in the cable resistance measurement calculation. The initial calculated link segment cable resistance, $R_{Cable\_initial}$, is defined in Equation (104–5).

$$R_{Cable\_initial} = \left(\frac{V_{PSE} - V_{Report\_PD}}{I_{PSE}} \right) \ \Omega \tag{104–5}$$

where

V_{Report_PD} is the voltage at PD's PI during the presence pulse as reported in b[7:0] of VOLT_INFO in Table 104–14

V_{PSE} is the voltage at PSE's PI during the presence pulse

I_{PSE} is the current at PSE's PI during the presence pulse

The initial cable resistance value calculated in Equation (104–5) is then margined by the Resistance Margin Factor, K_{RMF}, as shown in Equation (104–6). The margined link segment cable resistance, R_{Cable}, should not exceed the maximum allowable link segment dc loop resistance for the class as shown in Equation (104–6).

$$R_{Cable} = \min(R_{Cable\_initial} \times K_{RMF}, R_{Loop(max)}) \ \Omega \tag{104–6}$$

where

$R_{Cable\_initial}$ is the initial calculated link segment cable resistance

K_{RMF} is the Resistance Margin Factor per Table 104–12

$R_{Loop(max)}$ is the maximum allowable link segment dc loop resistance for the class per 104.2

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104.7.1.5 Calculations for power allocation

A PD that supports cable resistance measurement may request a power allocation between 0.1 W and $P_{\text{Class(max)}}$ via the PD Requested Power, $P_{\text{PD\_req}}$, field of the POWER_INFO register b[11:0]. The PD Requested Power may exceed $P_{\text{PD(max)}}$. A PSE that supports cable resistance measurement shall set PD Assigned Power ($P_{\text{PD\_assign}}$) based on PD Requested Power, $P_{\text{PD\_req}}$, and measured cable resistance as shown in Equation (104–7):

$$P_{\text{PD\_assign}} = \left\{ \begin{array}{ll} \min(P_{\text{PD\_req}}, P_{\text{Class(min)}} - {I_{\text{PI(max)}}}^2 \times R_{\text{Cable}}) & \text{for } P_{\text{PD\_req}} > P_{\text{PD(max)}} \\ P_{\text{PD\_req}} & \text{for } P_{\text{PD\_req}} \le P_{\text{PD(max)}} \end{array} \right\} \text{W} \qquad (104\text{–}7)$$

where

$P_{\text{PD\_req}}$ is the PD Requested Power as reported in b[11:0] of POWER_INFO in Table 104–15

$P_{\text{PD\_assign}}$ is the PD Assigned Power by PSE as assigned in b[11:0] of POWER_ASSIGN in Table 104–16

$P_{\text{Class(min)}}$ see Table 104–1 for description

$I_{\text{PI(max)}}$ see Table 104–1 for description

$P_{\text{PD(max)}}$ see Table 104–1 for description

For systems that implement cable resistance measurement, the PSE determines $P_{\text{PD\_assign}}$, as assigned in b[11:0] of POWER_ASSIGN in Table 104–16. Maximum average available power at the PD PI is $P_{\text{PD\_assign}}$. $P_{\text{PD\_assign}}$ may be greater or less than $P_{\text{PD(max)}}$.

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104.7.2 Serial communication classification protocols

All data and commands shall be transmitted least significant bit first using SCCP. The PSE initiates all transactions.

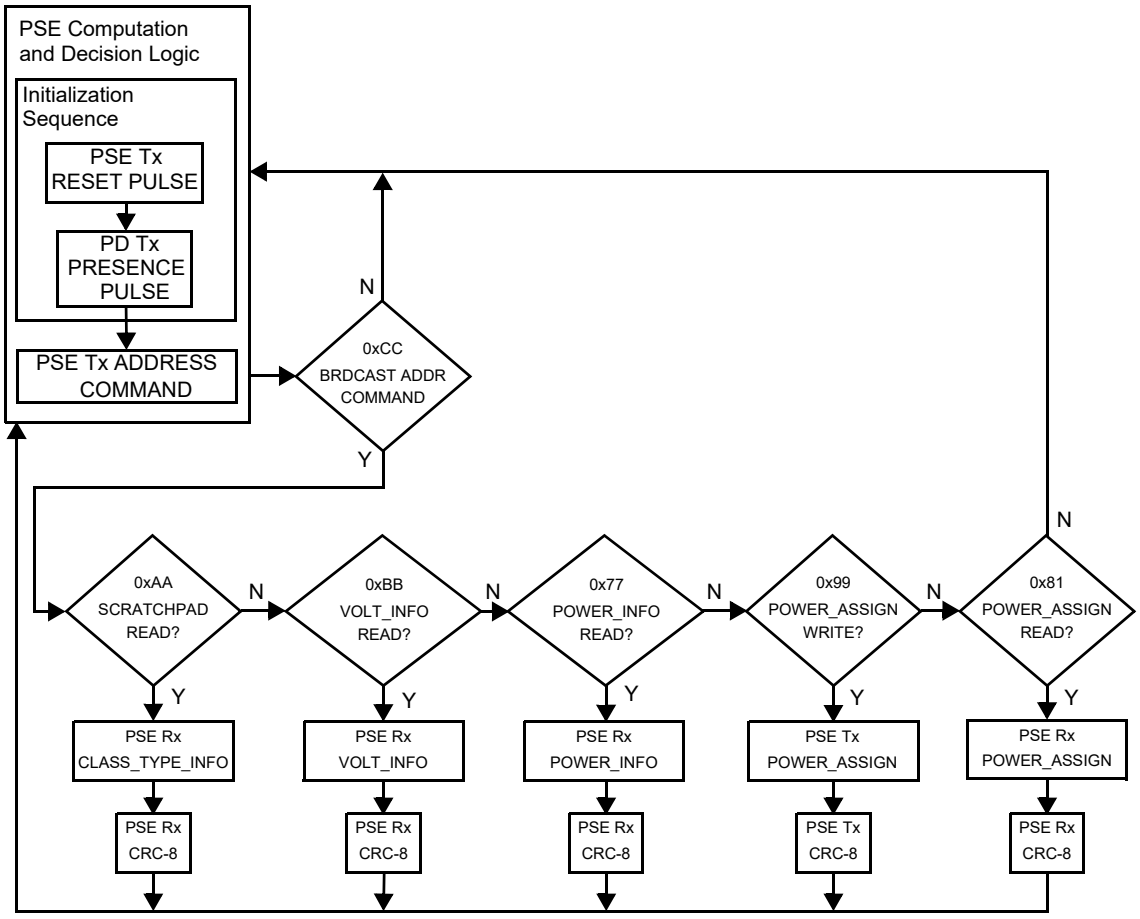

Figure 104–13—Address and Read_Scratchpad function command flowchart

104.7.2.1 SCCP transaction sequence

The transaction sequence for accessing a PD on SCCP is as follows:

a) Initialization
b) Address Command (followed by any required data exchange)
c) Function Command

104.7.2.2 Initialization

All communication with a PD shall begin with the initialization sequence that consists of a reset pulse from the PSE followed by a presence pulse from the PD.

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104.7.2.3 Address commands

All SCCP-capable PDs shall support the Broadcast Address command. The PSE shall issue an appropriate address command before issuing a function command.

104.7.2.3.1 Broadcast address [0xCC]

The PSE uses this command to address a PD on the bus without sending out unique address code information.

104.7.2.4 Read_Scratchpad function command [0xAA]

All SCCP-capable PDs shall support the 8-bit Read_Scratchpad command. After receiving a Read_Scratchpad function command the PD shall respond with a 16-bit CLASS_TYPE_INFO read payload followed by an 8-bit CRC8 field as specified in 104.7.2.5. A flowchart for operation of the address and the Read_Scratchpad function command is shown in Figure 104–13. Table 104–13 illustrates the contents of the CLASS_TYPE_INFO register.

Table 104–13—CLASS_TYPE_INFO register table

Bit(s)	Name	Description	R/W
b[15:12]	Type	15 14 13 12 1 1 1 0 = Type A 1 1 0 1 = Type B 1 0 1 1 = Type C 0 1 1 1 = Type D 1 1 0 0 = Type E 0 0 1 1 = Type F	RO
b[11]	pd_faulted	1—error condition has occurred that prevented the PD from receiving power at the PI. Set to 1 when the pd_fault variable transitions from FALSE to TRUE 0—no error condition detected	RO/ LH
b[10]	Cable resistance measurement	1 — Cable resistance measurement enabled 0 — Cable resistance measurement disabled	RO
b[9:0]	Class	9 8 7 6 5 4 3 2 1 0 1 1 1 1 1 1 1 1 1 0 = Class 0 1 1 1 1 1 1 1 1 0 1 = Class 1 1 1 1 1 1 1 1 0 1 1 = Class 2 1 1 1 1 1 1 0 1 1 1 = Class 3 1 1 1 1 1 1 0 1 1 1 = Class 4 1 1 1 1 0 1 1 1 1 1 = Class 5 1 1 1 0 1 1 1 1 1 1 = Class 6 1 1 0 1 1 1 1 1 1 1 = Class 7 1 0 1 1 1 1 1 1 1 1 = Class 8 0 1 1 1 1 1 1 1 1 1 = Class 9 0 0 0 0 0 0 0 0 0 1 =Class 10 0 0 0 0 0 0 0 0 1 0 =Class 11 0 0 0 0 0 0 0 0 1 1 =Class 12 0 0 0 0 0 0 0 1 0 0 =Class 13 0 0 0 0 0 0 0 1 0 1 =Class 14 0 0 0 0 0 0 0 1 1 0 =Class 15	RO

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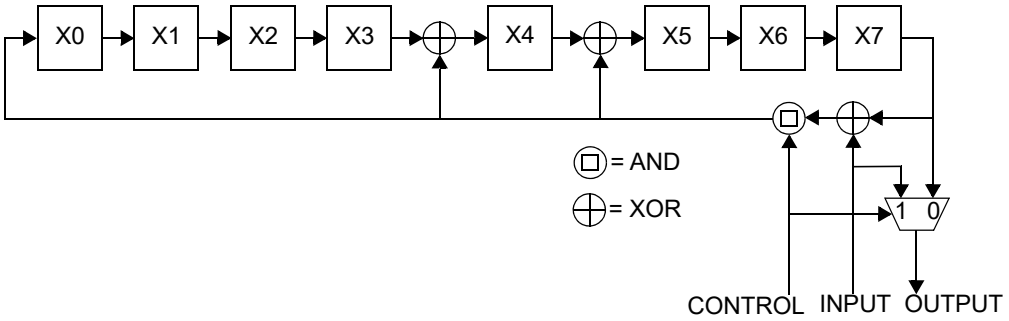
104.7.2.5 CRC8 field

The CRC8 field is an 8-bit cyclic redundancy check value. This value is computed as a function of the contents of the preceding Read/Write payload.

The encoding is defined by the generating polynomial shown in Equation (104–8):

$$G(x) = x^8 + x^5 + x^4 + 1 \quad (104–8)$$

This CRC8 calculation shall produce the same result as the serial implementation shown in Figure 104–14. Before calculation begins, the shift register shall be initialized to the value 0x00. The content of the shift register is transmitted without inversions.



CONTROL = 1 when shifting the contents of the register and calculating the CRC field
CONTROL = 0 when transmitting the CRC field

Figure 104–14—CRC8 field generation

104.7.2.6 Read_VOLT_INFO command [0xBB]

All PSEs and PDs that support cable resistance measurement shall support the 8-bit Read_VOLT_INFO command. After receiving a Read_VOLT_INFO command, the PD shall respond with a 16-bit VOLT_INFO read payload followed by an 8-bit CRC8 field as specified in 104.7.2.5. A flowchart for operation of the address and the Read_VOLT_INFO command is shown in Figure 104–13. Table 104–14 illustrates the contents of the VOLT_INFO register.

Table 104–14—VOLT_INFO register table

Bit(s)	Name	Description	R/W[a]
b[15:8]	Reserved	Value always 0	RO
b[7:0]	Voltage at PD PI during Presence Pulse	± 20 mV tolerance, 10 mV per LSB	RO

[a]RO = Read only

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104.7.2.7 Read_POWER_INFO command [0x77]

All PSEs and PDs that support cable resistance measurement shall support the 8-bit Read_POWER_INFO command. After receiving a Read_POWER_INFO command, the PD shall respond with a 16-bit POWER_INFO read payload followed by an 8-bit CRC8 field as specified in 104.7.2.5. A flowchart for operation of the address and the Read_POWER_INFO command is shown in Figure 104–13. Table 104–15 illustrates the contents of the POWER_INFO register.

Table 104–15—POWER_INFO register table

Bit(s)	Name	Description	R/W[a]
b[15:12]	Reserved	Value always 0	RO
b[11:0]	P_{PD_req} PD Requested Power	Power requested by PD, 0.025 W per LSB	RO

[a]RO = Read only

104.7.2.8 Write_POWER_ASSIGN command [0x99]

All PSEs and PDs that support cable resistance measurement shall support the 8-bit Write_POWER_ASSIGN command. After transmitting a Write_POWER_ASSIGN command, the PSE shall transmit a 16-bit POWER_ASSIGN write payload followed by an 8-bit CRC8 field as specified in 104.7.2.5. A flowchart for operation of the address and the Write_POWER_ASSIGN command is shown in Figure 104–13. Table 104–16 illustrates the contents of the POWER_ASSIGN register.

Table 104–16—POWER_ASSIGN register table

Bit(s)	Name	Description	R/W[a]
b[15:12]	Reserved	Value always 0	RO
b[11:0]	P_{PD_assign} PD Assigned Power	PD assigned power, 0.025 W per LSB	R/W

[a]RO = Read only, R/W = Read/Write

104.7.2.9 Read_POWER_ASSIGN command [0x81]

All PSEs and PDs that support cable resistance measurement shall support the 8-bit Read_POWER_ASSIGN command. After receiving a Read_POWER_ASSIGN command, the PD shall respond with a 16-bit POWER_ASSIGN read payload followed by an 8-bit CRC8 field as specified in 104.7.2.5. A flowchart for operation of the address and the Read_POWER_ASSIGN command is shown in Figure 104–13. Table 104–16 illustrates the contents of the POWER_ASSIGN register.

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104.8 Environmental

104.8.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2. In particular, the PSE shall be classified as a Limited Power Source in accordance with Annex Q of IEC 62368-1:2018, as applicable. For automotive applications, systems described in this clause may be subject to additional requirements; refer to ISO 26262.

All equipment subject to this clause may be additionally required to conform to any applicable local, state, or national standards, including national motor vehicle standards related to safety or as agreed to between the customer and supplier.

104.8.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns. The list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to verify compliance with the appropriate requirements. LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards should be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures should be taken to verify that the intended safety features are not negated during installation of a new network or during modification of an existing network.

104.8.3 Installation and maintenance guidelines

It is a mandatory requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

In particular, users are cautioned to be aware of the ampacity of cabling, as installed, and local codes and regulations, e.g., ANSI/NFPA 70—National Electric Code® (NEC®), relevant to the maximum class supported.

It is a mandatory requirement that, during installation of the cabling plant, care be taken to verify that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner.

In automotive applications, all PoDL cabling should be routed in way to provide maximum protection by the motor vehicle sheet metal and structural components, following SAE J1292, ISO 14229, and ISO 15764.

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Automotive environmental conditions are generally more severe than those found in many commercial and industrial environments. The target automotive, industrial, or commercial environment(s) require careful analysis prior to implementation.

104.8.4 Patch panel considerations

It is possible that the current carrying capability of a cabling cross-connect may be exceeded by a PSE. The designer should consult the manufacturers' specifications to verify compliance with the appropriate requirements.

104.8.5 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to a PSE or PD. Other than voice signals, the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply:

Battery voltage to a telephone line is generally 56 Vdc, applied to the line through a balanced 400 Ω source impedance. Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 Vp at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 Vdc with 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Application of any of the above voltages to the PI of a PSE or a PD in non-automotive applications shall not preclude conformance with 104.8.1 and 104.8.2.

104.8.6 Electromagnetic emissions

The PD and PSE powered cabling link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

In addition, the system may need to comply with more stringent requirements as agreed upon between customer and supplier, for the limitation of electromagnetic interference. In automotive applications, a PoDL system shall be tested according to CISPR 25 test methods, and shall meet the following motor vehicle EMC requirements:

a) Radiated/Conducted Emissions: CISPR 25, IEC 61967-1/4, and IEC 61000-4-21
b) Radiated/Conducted Immunity: ISO 11452, IEC 62132-1/4, and IEC 61000-4-21
c) Electrostatic Discharge: ISO 10605 and IEC 61000-4-2/3
d) Electrical Disturbances: IEC 62215-3 and ISO 7637-2/3

Exact test setup and test limit values may be adapted to each specific application, subject to agreement between the customer and the supplier.

104.8.7 Temperature and humidity

The PD and PSE powered cabling link segment is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling. Specific requirements and values for these parameters are beyond the scope of this standard.

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104.9 Protocol implementation conformance statement (PICS) proforma for Clause 104, Power over Data Lines (PoDL) of Single-Pair Ethernet[178]

104.9.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 104, Power over Data Lines (PoDL) of Single-Pair Ethernet, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

104.9.2 Identification

104.9.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

104.9.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 104 Power over Data Lines (PoDL) of Single-Pair Ethernet
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022)	

Date of Statement	

[178] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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104.9.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*CRM	Implements cable resistance measurement functionality	104.7		SCCP:O	Yes [ ] No [ ] N/A [ ]
*PSETA	Implements PSE Type A functionality	104.1.3	Provides support for requirements of Type A Power Sourcing Equipment	O	Yes [ ] No [ ]
*PSETB	Implements PSE Type B functionality	104.1.3	Provides support for requirements of Type B Power Sourcing Equipment	O	Yes [ ] No [ ]
*PSETC	Implements PSE Type C functionality	104.1.3	Provides support for requirements of Type C Powered Sourcing Equipment	O	Yes [ ] No [ ]
*PSETE	Implements PSE Type E functionality	104.1.3	Provides support for requirements of Type E Powered Sourcing Equipment	O	Yes [ ] No [ ]
*PSETF	Implements PSE Type F functionality	104.1.3	Provides support for requirements of Type F Power Sourcing Equipment	O	Yes [ ] No [ ]
*PDTA	Implements PD Type A functionality	104.1.3	Provides support for requirements of Type A Powered Device Equipment	O	Yes [ ] No [ ]
*PDTB	Implements PD Type B functionality	104.1.3	Provides support for requirements of Type B Powered Device Equipment	O	Yes [ ] No [ ]
*PDTC	Implements PD Type C functionality	104.1.3	Provides support for requirements of Type C Powered Device Equipment	O	Yes [ ] No [ ]
*PDTE	Implements PD Type E functionality	104.1.3	Provides support for requirements of Type E Powered Device Equipment	O	Yes [ ] No [ ]
*PDTF	Implements PD Type F functionality	104.1.3	Provides support for requirements of Type F Powered Device Equipment	O	Yes [ ] No [ ]
*SCCP	Implements SCCP Classification functionality	104.7	Provides support for classification of PDs	O	Yes [ ] No [ ]

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104.9.4 PICS proforma tables for Clause 104, Power over Data Lines (PoDL) of Single-Pair Ethernet

104.9.4.1 Link Segment

Item	Feature	Subclause	Value/Comment	Status	Support
LNK1	DC loop resistance	104.2	Less than 6 Ω for Classes 0 and 1, less than 6.5 Ω for Classes 2 through 9, less than 65 Ω for Classes 10 and 13, less than 25 Ω for Classes 11 and 14, less than 9.5 Ω for Classes 12 and 15	M	Yes [ ]

104.9.4.2 Power Sourcing Equipment (PSE)

Item	Feature	Subclause	Value/Comment	Status	Support
PSE1	PSE pinout	104.4.2	See Table 104–3	M	Yes [ ]
PSE2	Voltage and power requirements	104.4.3	As defined in Table 104–1 for each relevant class	M	Yes [ ]
PSE3	PSE behavior	104.4.4	In accordance with the state diagrams shown in Figure 104–4, Figure 104–5, and Figure 104–6	M	Yes [ ]
PSE4	Complete detection of a valid PD signature	104.4.5	Within T_{det} as specified in Table 104–6	M	Yes [ ]
PSE5	Valid signature not detected and classification not performed	104.4.5	Wait at least $T_{Restart}$ before reattempting detection	M	Yes [ ]
PSE6	Detection currents	104.4.5.1	Within I_{valid} current range, as specified in Table 104–6,when connected to a valid PD detection signature as specified in Table 104–9	M	Yes [ ]
PSE7	Detection Probe	104.4.5.1	To conform to V_{OC}, I_{SC}, I_{slew}, and C_{out} as specified in Table 104–6	M	Yes [ ]
PSE8	Accept valid PD signature	104.4.5.2	From link segment with a voltage in the range of V_{good_PSE} for at least T_{sig_hold} in response to a probing current in the range of I_{valid} as specified in Table 104–6	M	Yes[ ]
PSE9	Reject invalid PD signature	104.4.5.3	From link segment that exhibits the following characteristics outlined in Table 104–6: a) Voltage less than or equal to $V_{bad_lo_PSE}$max b) Voltage greater than or equal to $V_{bad_hi_PSE}$min	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE10	Applying full operating voltage at the PI with SCCP enabled	104.4.6	Only after detection and complete classification in a time less than T_{Class} as specified in Table 104–7	M	Yes [ ]
PSE11	T_{Class} timer expired before complete classification	104.4.6	Complete a new detection cycle before applying any subsequent full operating voltage and transition to the RESTART state	M	Yes [ ]
PSE12	Providing power to the PSE PI	104.4.7	To conform to electrical limits in Table 104–7	M	Yes [ ]
PSE13	Present invalid PD signature	104.4.7	With one of the attributes as specified in Table 104–10 under all conditions	M	Yes [ ]
PSE14	Applied voltage at the PI while in the POWER_ON state	104.4.7.1	In the range of $V_{PSE(PON)}$	M	Yes [ ]
PSE15	Applied voltage at the PI when in the OVERLOAD, OVERLOAD_DELAY, and DISABLED states	104.4.7.1	In the range of $V_{Disable}$	M	Yes [ ]
PSE16	Applied voltage at the PI while in the SLEEP, RESTART, RESTART_DELAY, and IDLE states	104.4.7.1	In the range of V_{Sleep}	M	Yes [ ]
PSE17	SETTLE_SLEEP state	104.4.7.1	Discharge the PSE PI to the range of V_{Sleep} within a time less than T_{OFF}max	M	Yes [ ]
PSE18	Enter SETTLE_SLEEP state	104.4.7.2	If a valid MFVS is not present at the PI while operating in the POWER_ON state	M	Yes [ ]
PSE19	PI discharge while in SETTLE_SLEEP state	104.4.7.2	To the range of V_{Sleep} with a current in the range of $I_{discharge}$	M	Yes [ ]
PSE20	PSE output during POWER_UP state	104.4.7.2	Not to exceed I_{LIM}max	M	Yes [ ]
PSE21	POWER_UP and POWER_ON state operation	104.4.7.2.1	Limit the current to I_{LIM} for a duration of up to T_{LIM} in order to account for PSE dV/dt transients at the PI as specified in Table 104–7	M	Yes [ ]
PSE22	PSE enabled while not in POWER_ON or POWER_UP states	104.4.7.2.1	Limit I_{PSE} to less than I_{SC} as specified in Table 104–6 for a duration of up to T_{LIM}	M	Yes [ ]
PSE23	Set overload_detected to TRUE and begin power removal from the PI within T_{LIM} of the initiation of current limiting	104.4.7.2.1	If the PSE is limiting current in any state when pi_powered, pi_sleeping, or pi_prebias are true	M	Yes [ ]
PSE24	Measuring I_{PSE} during short circuit	104.4.7.2.1	To be made 1 ms after the initial transient to allow for settling	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE25	I_{PSE} in the valid range of I_{Wakeup} for a minimum of T_{Wakeup}	104.4.7.2.2	Transition from the SLEEP state to the POWER_UP state	M	Yes [ ]
PSE26	Remain in SLEEP state	104.4.7.2.2	If I_{PSE} is greater than $I_{Wakeup\_bad\_hi}$ or less than $I_{Wakeup\_bad\_lo}$	M	Yes [ ]
PSE27	Output current during IDLE state valid	104.4.7.2.3	If less than I_{Wakeup} max for at least T_{Wakeup} min	M	Yes [ ]
PSE28	Output current during IDLE state invalid	104.4.7.2.3	If greater than $I_{Wakeup\_bad\_hi}$	M	Yes [ ]
PSE29	Enter POWER_ON state	104.4.7.4	If full operating voltage is applied within T_{Inrush}min	M	Yes [ ]
PSE30	Full operating voltage not applied within T_{Inrush}max	104.4.7.4	New detection cycle initiated after a delay of $T_{Restart}$ before any subsequent application of full operating voltage	M	Yes [ ]
PSE31	$T_{Disable}$	104.4.7.6	Applies to the discharge time from V_{PSE} to $V_{Disable}$ with a test resistor of 320 kΩ attached to the PI	M	Yes [ ]
PSE32	P_{Class}	104.4.7.7	As defined in Table 104–1	M	Yes [ ]
PSE33	Measurement of P_{Class}	104.4.7.7	Averaged from uniform sliding window with a width of 1 s	M	Yes [ ]
PSE34	Full operating voltage removal while in POWER_ON state	104.4.8	In absence of PD MFVS or if overload_detected is TRUE	M	Yes [ ]
PSE35	MFVS present	104.4.8.1	If I_{PSE} is greater than or equal to I_{Hold} max for a minimum of T_{MFVS} while in the POWER_ON state	M	Yes [ ]
PSE36	MFVS absent	104.4.8.1	If I_{PSE} is less than or equal to I_{Hold} min while in the POWER_ON state	M	Yes [ ]
PSE37	MFVS absent for duration greater than T_{MFVDO}	104.4.8.1	Reduce voltage at the PSE-PI to the range of V_{Sleep}	M	Yes [ ]
PSE38	do_classification function for PSEs that support cable resistance measurement	104.4.4.5	Return VOLT_INFO, POWER_INFO, and POWER_ASSIGN registers	SCCP:O CRM:M	Yes [ ] No [ ] N/A [ ]

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104.9.4.3 Powered Device (PD)

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	PD PI	104.5.2	Class 0 to 9 PDs operate per the Mode A column in Table 104–8. Class 10 to 15 PDs are polarity-insensitive and are able to operate per Mode A and Mode B of Table 104–8.	M	Yes [ ]
PD2	Voltage and power requirements	104.5.3	As defined in Table 104–1 for each relevant class	M	Yes [ ]
PD3	PD behavior	104.5.4	In accordance with the state diagram shown in Figure 104–8	M	Yes [ ]
PD4	Present valid detection signature when classification is not implemented or if a Class 0 or Class 1 PD	104.5.5	When V_{PD} is less than V_{sig_enable}	M	Yes [ ]
PD5	Classification implementation required	104.5.5	If PD presents an invalid detection signature greater than V_{bad_hi} max as specified in Table 104–10	M	Yes [ ]
PD6	Removal of current draw of detection signature	104.5.5	When V_{PD} is greater than $V_{sig\_disable}$	M	Yes [ ]
PD7	PD detection signature	104.5.5	To consist of a current limited, voltage, V_{good} as specified in Table 104–9 when measured by the PSE	M	Yes [ ]
PD8	Valid detection signature	104.5.5	In accordance with all of the characteristics shown in Table 104–9	M	Yes [ ]
PD9	Non-valid detection signature	104.5.5	In accordance with one of the characteristics shown in Table 104–10	M	Yes [ ]
PD10	PD power	104.5.7	In accordance with the characteristics shown in Table 104–11	M	Yes [ ]
PD11	PD discharge	104.5.7.1	At a delay of T_{OFF} max after disconnection from the PSE, a PD shall not source greater than 410 μJ out of its PI until V_{PD} drops below V_{Sleep_PD} max	M	Yes [ ]
PD12	PD turn on	104.5.7.2	At a voltage less than or equal to V_{On} max and with a delay greater than T_{power_dly} min	M	Yes [ ]
PD13	PD on voltage	104.5.7.2	Over the range from V_{PD} min to V_{PSE} max	M	Yes [ ]
PD14	PD turn off	104.5.7.2	At a voltage in the range of V_{PD} min to V_{Off} min	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD15	PD turn on or off	104.5.7.2	Without startup oscillation and within the first trial when a voltage in the range of V_{PSE} (as defined in Table 104–1) is applied with a series resistance within the range of valid dc loop resistance (as defined in 104.2)	M	Yes [ ]
PD16	PD_SLEEP state input voltage	104.5.7.2	Greater than V_{Sleep_PD} min as specified in Table 104–11	M	Yes [ ]
PD17	Input current while in DISCONNECT and PD_SLEEP states	104.5.7.3	Current drawn is not in excess of I_{Sleep_PD} as specified in Table 104–11	M	Yes [ ]
PD18	PD requiring detection and application of power	104.5.7.3	Draw current in the range of I_{Wakeup_PD} for at least T_{Wakeup_PD} when V_{PD} is in the range of V_{Sleep_PD} as specified in Table 104–11	M	Yes [ ]
PD19	Constant PD input voltage between V_{sig_disble}max and V_{On} min	104.5.7.3	Draw current less than I_{PD_pwr1}max	M	Yes [ ]
PD20	Type A or Type C PD ripple and transients	104.5.7.4	In accordance with specifications shown in Table 104–11 for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 96, and over the range of P_{PD}	PDTA:M or PDTC:M	Yes [ ] N/A [ ]
PD21	Type F PD ripple and transients	104.5.7.4	In accordance with specifications shown in Table 104–11 for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 149, and over the range of P_{PD}	PDTF:M	Yes [ ] N/A [ ]
PD22	Type B PD ripple and transients	104.5.7.4	In accordance with specifications shown in Table 104–11 for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 97, and over the range of P_{PD}	PDTB:M	Yes [ ] N/A [ ]
PD23	Type A or Type C PD measured ripple voltage post-processing	104.5.7.4	With transfer function $H_2(f)$ specified in Equation (104–3) where f_2=1 MHz ±1%	PDTA:M or PDTC:M	Yes [ ] N/A [ ]
PD24	Type F PD measured ripple voltage post-processing	104.5.7.4	With transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 10 MHz ± 1%	PDTF:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD25	Type B PD measured ripple voltage post-processing	104.5.7.4	With transfer function $H_2(f)$ specified in Equation (104–3) where f_2=10 MHz ±1%	PDTB:M	Yes [ ] N/A [ ]
PD26	Maximum average power, $P_{PD(max)}$	104.5.7.5	Calculated using a uniform sliding window with a width of 1 s	M	Yes [ ]
PD27	PD Maintain full voltage	104.5.8	Provide a valid (MFVS) at the PI	M	Yes [ ]
PD28	PD MFVS current draw	104.5.8	Equal to or greater than I_{hold_PD} for a minimum duration of T_{MFVS_PD} measured at the PD PI followed by an allowed MFVS dropout for no longer than T_{MFVDO} min	M	Yes [ ]
PD29	No longer require full operating voltage	104.5.8	Remove current draw of the MFVS from the PI	M	Yes [ ]

104.9.4.4 Common Electrical

Item	Feature	Subclause	Value/Comment	Status	Support
COMEL1	Type A, Type B, Type C, and Type F PSE and PD fault tolerance	104.6.2	The PI shall meet the fault tolerance requirements as specified in 96.8.3	PSETA:M PSETB:M PSETC:M PSETF:M PDTA:M PDTB:M PDTC:M PDTF:M	Yes [ ] N/A [ ]
COMEL2	Type E PSE and PD fault tolerance	104.6.2	The PI shall meet the fault tolerance requirements as specified in 146.8.6	PSETE:M PDTE:M	Yes [ ] N/A [ ]

104.9.4.5 PSE Electrical

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL1	PSE PI	104.6.2	Withstand the application of short circuits between the wires within the cable for an indefinite period of time without damage	M	Yes [ ]

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104.9.4.6 PD Electrical

Item	Feature	Subclause	Value/Comment	Status	Support
PDEL1	DC isolation	104.6.1	Of at least 1 MΩ provided between all accessible external conductors, including frame ground (if any), and all MDI leads, when measured using a 5 V ± 20% source voltage	M	Yes [ ]
PDEL2	PD PI	104.6.2	A PD shall not be damaged when connected to any PSE as defined in 104.4	M	Yes [ ]

104.9.4.7 SCCP

Item	Feature	Subclause	Value/Comment	Status	Support
SCCP1	SCCP implementation mandatory	104.7	For PDs that present an invalid detection signature as specified in Table 104–10	SCCP:M	Yes [ ] N/A[ ]
SCCP2	SCCP communication	104.7.1.1	Begins with an initialization sequence consisting of a result pulse from the PSE followed by a presence pulse from the PD. See Figure 104–10	SCCP:M	Yes [ ] N/A[ ]
SCCP3	Initialization sequence	104.7.1.1	PSE transmits a reset pulse by first driving V_{PSE} low and then releasing to the pull up at t_{RSTL} before going into receive mode (RX)	SCCP:M	Yes [ ] N/A[ ]
SCCP4	PD presence pulse	104.7.1.1	Transmitted after detecting rising edge at PD PI and waiting t_{PDH}	SCCP:M	Yes [ ] N/A[ ]
SCCP5	Presence data from PD	104.7.1.1	To be valid for the entire time window defined by t_{MSP} following the rising edge that terminated the reset pulse	SCCP:M	Yes [ ] N/A[ ]
SCCP6	PSE write time slots	104.7.1.2	Write 1 time slot to transmit logic 1 to PD and write 0 time slot to transmit logic 0 to PD	SCCP:M	Yes [ ] N/A[ ]
SCCP7	Write time slot duration	104.7.1.2	Defined as t_{SLOT} shown in Table 104–12	SCCP:M	Yes [ ] N/A[ ]
SCCP8	Write time slot initiation	104.7.1.2	Initiated by pulling V_{PSE} low	SCCP:M	Yes [ ] N/A[ ]
SCCP9	Write 1 time slot generation	104.7.1.2	Pull up V_{PSE} within the range of t_{W1L} after pulling V_{PSE} low	SCCP:M	Yes [ ] N/A[ ]
SCCP10	Write 0 time slot generation	104.7.1.2	Pull up V_{PSE} within the range of t_{W0L} after pulling V_{PSE} low	SCCP:M	Yes [ ] N/A[ ]
SCCP11	PD sampling during a write 1 or write 0 operation	104.7.1.2	Sample V_{PD} within the range of t_{SSW} after falling edge.	SCCP:M	Yes [ ] N/A[ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
SCCP12	Read time slot generation	104.7.1.3	Generated by the PSE immediately after issuing a function command that requires data from the PD	SCCP:M	Yes [ ] N/A[ ]
SCCP13	Read time slot duration	104.7.1.3	Defined as t_{SLOT} shown in Table 104–12	SCCP:M	Yes [ ] N/A[ ]
SCCP14	Read time slot initiation	104.7.1.3	Initiate by pulling PI port voltage low and then pulling up the PI port voltage within t_{W1L}	SCCP:M	Yes [ ] N/A[ ]
SCCP15	PD transmit	104.7.1.3	Transmit a 1 or 0 at the PD PI after PSE initiates read time slot	SCCP:M	Yes [ ] N/A[ ]
SCCP16	PD transmit 1	104.7.1.3	Leave PI port voltage high	SCCP:M	Yes [ ] N/A[ ]
SCCP17	PD transmit 0	104.7.1.3	Pull PI port voltage low	SCCP:M	Yes [ ] N/A[ ]
SCCP18	PD transmit 0 duration	104.7.1.3	While transmitting 0, hold the PI low, and then release its PI within t_{R0L}	SCCP:M	Yes [ ] N/A[ ]
SCCP19	Read time slot sample	104.7.1.3	PSE releases PI and then samples subsequent voltage within t_{MSR} from the start of the read time slot	SCCP:M	Yes [ ] N/A[ ]
SCCP20	SCCP electrical requirements	104.7.1.3	To comply with the electrical and timing requirements in Table 104–12	SCCP:M	Yes [ ] N/A[ ]
SCCP21	SCCP data and commands	104.7.2	Transmitted least significant bit first	SCCP:M	Yes [ ] N/A[ ]
SCCP22	Communication with PD	104.7.2.2	Begins with the initialization sequence that consists of a reset pulse from the PSE followed by a presence pulse from the PD	SCCP:M	Yes [ ] N/A[ ]
SCCP23	SCCP-capable PDs	104.7.2.3	Support the Broadcast Address command	SCCP:M	Yes [ ] N/A[ ]
SCCP24	Issuing function command	104.7.2.3	Only after issuing an appropriate address command	SCCP:M	Yes [ ] N/A[ ]
SCCP25	8-bit Read Scratchpad command	104.7.2.4	Supported by all SCCP-enabled PDs	SCCP:M	Yes [ ] N/A[ ]
SCCP26	Reception of Read Scratchpad function command	104.7.2.4	PD shall respond with a 16-bit CLASS_TYPE_INFO read payload followed by an 8-bit CRC8 field	SCCP:M	Yes [ ] N/A[ ]
SCCP27	CRC8 calculation	104.7.2.5	Produces the same result as the serial implementation shown in Figure 104–14	SCCP:M	Yes [ ] N/A[ ]
SCCP28	Shift register	104.7.2.5	Initialized to the value 0x00 before CRC8 calculation begins	SCCP:M	Yes [ ] N/A[ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
SCCP29	8-bit Read_VOLT_INFO command	104.7.2.6	Supported by all PSEs and PDs that implement CRM	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP30	Reception of Read_VOLT_INFO function command	104.7.2.6	PD shall respond with a 16-bit VOLT_INFO read payload followed by an 8-bit CRC8 field	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP31	8-bit Read_POWER_INFO command	104.7.2.7	Supported by all PSEs and PDs that implement CRM	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP32	Reception of Read_POWER_INFO function command	104.7.2.7	PD shall respond with a 16-bit POWER_INFO read payload followed by an 8-bit CRC8 field	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP33	8-bit Write_POWER_ASSIGN command	104.7.2.8	Supported by all PSEs and PDs that implement CRM	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP34	Reception of Write_POWER_ASSIGN function command	104.7.2.8	PSE shall transmit a 16-bit POWER_ASSIGN write payload followed by an 8-bit CRC8 field	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP35	8-bit Read_POWER_ASSIGN command	104.7.2.9	Supported by all PSEs and PDs that implement CRM	SCCP:O CRM:M	Yes [ ] N/A [ ]
SCCP36	Reception of Read_POWER_ASSIGN function command	104.7.2.9	PD shall respond with a 16-bit POWER_ASSIGN read payload followed by an 8-bit CRC8 field	SCCP:O CRM:M	Yes [ ] N/A [ ]

104.9.4.8 Environmental

Item	Feature	Subclause	Value/Comment	Status	Support
ENV1	General safety for PoDL equipment	104.8.1	To conform to J.2	M	Yes [ ]
ENV2	General safety for PoDL PSEs	104.8.1	To be classified as a Limited Power Source in accordance with Annex Q of IEC 62368-1:2018	M	Yes [ ]
ENV3	Telephony voltages for non-automotive applications	104.8.5	Shall not preclude conformance with 104.8.1 and 104.8.2 for non-automotive applications	M	Yes [ ]
ENV4	PD and PSE powered cabling link	104.8.6	To comply with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]
ENV5	PoDL systems for automotive applications	104.8.6	To be tested according to CISPR 25 test methods and meet the motor vehicle EMC requirements listed in 104.8.6	M	Yes [ ]

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105. Introduction to 25 Gb/s networks

105.1 Overview

105.1.1 Scope

25 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer, connected through a 25 Gigabit Media Independent Interface (25GMII) to Physical Layer devices such as 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-SR, 25GBASE-T, 25GBASE-LR, and 25GBASE-ER.

25 Gb/s Physical Layer devices, such as those specified in Table 105–1, provide a frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap.

25 Gigabit Ethernet is defined for full duplex operation only.

105.1.2 Relationship of 25 Gigabit Ethernet to the ISO OSI reference model

25 Gigabit Ethernet couples the IEEE 802.3 MAC to a family of 25 Gb/s Physical Layers. The relationships among 25 Gigabit Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 105–1.

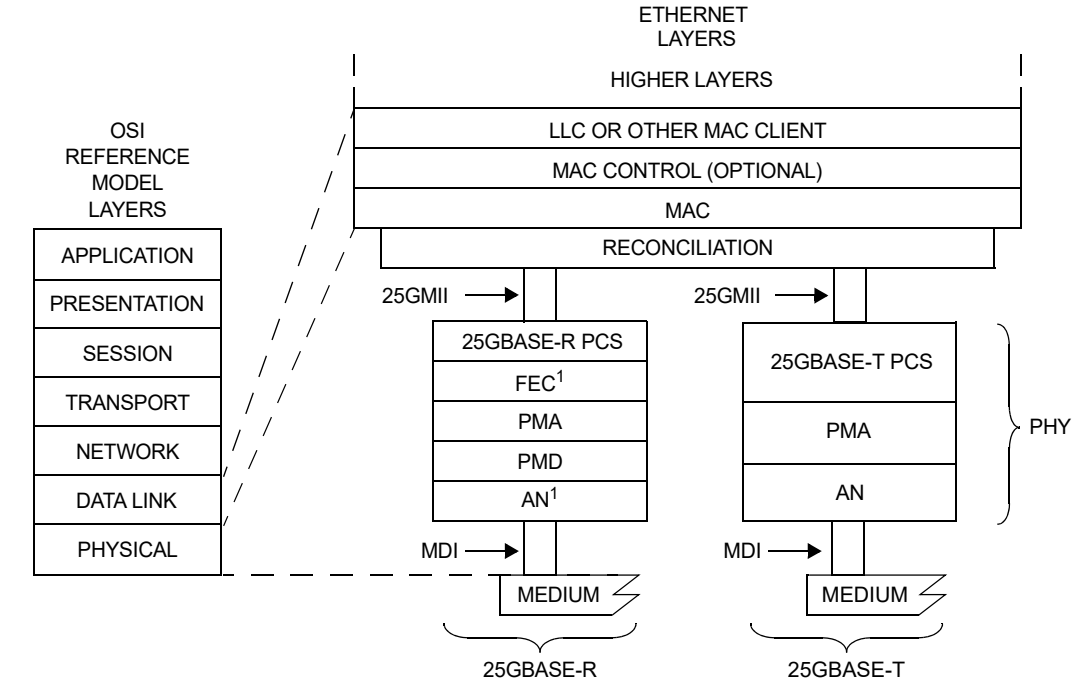

Figure 105–1—Architectural positioning of 25 Gigabit Ethernet

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It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The PMA service interface, which, when physically implemented as 25GAUI at an observable interconnection port, uses a single-lane data path as specified in Annex 109A or Annex 109B.

b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.

c) The Media Dependent Interface (MDI) as specified in Clause 110 for 25GBASE-CR and 25GBASE-CR-S, in Clause 111 for 25GBASE-KR and 25GBASE-KR-S, in Clause 112 for 25GBASE-SR, or in Clause 114 for 25GBASE-LR and 25GBASE-ER uses a single-lane data path.

d) The MDI as specified in Clause 113 for 25GBASE-T uses a four-lane data path.

105.1.3 Nomenclature

The prefix 25GBASE in the port type (e.g., 25GBASE-R) represents a family of Physical Layer devices operating at a speed of 25 Gb/s.

The term 25GBASE-R refers to a specific family of Physical Layer implementations based upon the 64B/66B data coding method specified in Clause 107. The 25GBASE-R family is composed of 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-SR, 25GBASE-LR, and 25GBASE-ER.

25GBASE-T represents Physical Layer devices using Clause 113 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, for data communication at 25 Gb/s over a point-to-point 4-pair balanced twisted-pair medium. 25GBASE-T uses a combination of Reed-Solomon-FEC (RS-FEC) and low density parity check (LDPC) FECs in its physical coding sublayer that is mapped to a 128 double-square (DSQ128) constellation for transmission on 4-pair, twisted-pair copper cabling.

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Physical Layer devices listed in Table 105–1 are defined for operation at 25 Gb/s.

Table 105–1—25 Gb/s PHYs

Name	Description
25GBASE-KR-S	25 Gb/s PHY equivalent to 25GBASE-KR without support for the RS-FEC sublayer (see Clause 111).
25GBASE-KR	25 Gb/s PHY using 25GBASE-R encoding over one lane of an electrical backplane (see Clause 111).
25GBASE-CR-S	25 Gb/s PHY equivalent to 25GBASE-CR without support for the RS-FEC sublayer (see Clause 110).
25GBASE-CR	25 Gb/s PHY using 25GBASE-R encoding over one lane of twinaxial copper cable (see 1.4.559 and Clause 110).
25GBASE-T	25 Gb/s PHY using RS-FEC and LDPC encoding over balanced twisted-pair structured cabling systems (see Clause 113).
25GBASE-SR	25 Gb/s PHY using 25GBASE-R encoding over a duplex multimode fiber (see Clause 112).
25GBASE-LR	25 Gb/s PHY using 25GBASE-R encoding over a duplex single-mode fiber, with reach up to at least 10 km (see Clause 114).
25GBASE-ER	25 Gb/s PHY using 25GBASE-R encoding over a duplex single-mode fiber, with reach up to at least 40 km (see Clause 114).

105.2 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. The generic term 25 Gigabit Ethernet refers to any use of the 25 Gb/s IEEE 802.3 MAC (the 25 Gigabit Ethernet MAC) coupled with any IEEE 802.3 25GBASE Physical Layer implementation. Table 105–2 specifies the correlation between

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nomenclature and clauses. Implementations conforming to one or more nomenclatures shall meet the requirements of the corresponding clauses.

Table 105–2—Nomenclature and clause correlation, 25 Gb/s Ethernet PHYs

Nomenclature	Clause/Annex																		
	28	73	74	78	106		107	108	109	109A	109B	110		111		112	113	114	
	Auto-Negotiation	Auto-Negotiation	BASE-R FEC	EEE	RS	25GMII	25GBASE-R PCS	25GBASE-R RS-FEC	PMA	25GAUI C2C	25GAUI C2M	25GBASE-CR PMD	25GBASE-CR-S PMD	25GBASE-KR PMD	25GBASE-KR-S PMD	25GBASE-SR PMD	25GBASE-T PCS/PMA	25GBASE-LR PMD	25GBASE-ER PMD
25GBASE-KR-S		M[a]	M	O[a]	M	O	M		M	O					M				
25GBASE-KR		M	M	O	M	O	M	M	M	O				M					
25GBASE-CR-S		M	M	O	M	O	M		M	O			M						
25GBASE-CR		M	M	O	M	O	M	M	M	O		M							
25GBASE-T	M			O	M	O											M		
25GBASE-SR				O	M	O	M	M	M	O	O					M			
25GBASE-LR				O	M	O	M	M	M	O	O							M	
25GBASE-ER				O	M	O	M	M	M	O	O								M

[a]O = Optional, M = Mandatory

105.3 Summary of 25 Gigabit Ethernet sublayers

105.3.1 Reconciliation Sublayer (RS) and 25 Gigabit Media Independent Interface (25GMII)

The 25GMII (Clause 106) provides a logical interconnection between the Media Access Control (MAC) sublayer and Physical Layer devices (PHYs). The 25GMII supports 25 Gb/s operation through its 32-bit-wide transmit and receive data paths.

The RS provides a mapping between the signals provided at the 25GMII and the MAC/PLS service definition.

While the 25GMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for a 25 Gb/s PHY.

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105.3.2 Physical Coding Sublayer (PCS)

25GBASE-R PHYs use the PCS specified in Clause 107. The 25GBASE-R PCS performs encoding of data from the 25GMII to 64B/66B code blocks and transfers the encoded data to the PMA and performs decoding of 64B/66B blocks from the PMA and transfers the decoded data to the 25GMII.

105.3.3 Forward error correction (FEC) sublayer

An FEC sublayer is available for all 25GBASE-R PHYs. The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers.

The BASE-R FEC (see Clause 74) may be used by some 25GBASE-R PHYs.

The RS-FEC (see Clause 108) may be used by some 25GBASE-R PHYs.

The requirement to implement FEC for each Physical Layer implementation is summarized in 105.2.

105.3.4 Physical Medium Attachment (PMA) sublayer

The PMA sublayer provides a medium-independent means for the PCS to support the use of a range of physical media. The PMA performs the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface and mapping of transmit and receive data streams between the PMA and PMD via the PMD service interface.

The 25GBASE-R PMA (see Clause 109) performs retiming of the received data stream when appropriate, optionally provides data loopback at the PMA or PMD service interface, and optionally provides test-pattern generation and checking. The 25GBASE-R PMA also may provide the observable electrical interface for the 25GAUI chip-to-chip (C2C) or chip-to-module (C2M) (see Annex 109A and Annex 109B).

105.3.5 Physical Medium Dependent (PMD) sublayer

The PMD sublayer is responsible for interfacing to the transmission medium.

The MDI connects the PMD to the medium and is defined in the associated PMD clause.

The 25GBASE-R PMDs and their corresponding media are specified in Clause 110, Clause 111, Clause 112, and Clause 114.

105.3.6 Auto-Negotiation (AN)

AN provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation.

Clause 28 AN is used by the 25GBASE-T PHY.

Clause 73 AN is used by the 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, and 25GBASE-KR-S PHYs.

105.3.7 Management interface (MDIO/MDC)

The MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMD) and Station Management (STA) entities.

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105.3.8 Management

Managed objects, attributes, and actions are defined for all 25 Gigabit Ethernet components. These items are defined in Clause 30.

105.4 Service interface specification method and notation

The service interface specification for 25GBASE-R Physical Layers is as per the definition in 1.2.2 and is based upon the service interface specification in 80.3, but redefined for a single lane.

105.4.1 Inter-sublayer service interface

The inter-sublayer service interface is described in an abstract manner and does not imply any particular implementation. The inter-sublayer service interface primitives are defined as follows:

IS_UNITDATA.request
IS_UNITDATA.indication
IS_SIGNAL.indication

The IS_UNITDATA.request primitive is used to define the transfer of a stream of data units from a sublayer to the next lower (closer to the medium) sublayer. The IS_UNITDATA.indication primitive is used to define the transfer of a stream of data units from a sublayer to the next higher (closer to the MAC) sublayer. The IS_SIGNAL.indication primitive is used to define the transfer of signal status from a sublayer to the next higher sublayer.

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see 78.1.3.3.1), then the inter-sublayer service interface includes some or all (depending on sublayer, see Figure 105–3) of five additional primitives defined as follows:

IS_TX_MODE.request
IS_RX_MODE.request
IS_ENERGY_DETECT.indication
IS_RX_LPI_ACTIVE.request
IS_RX_TX_MODE.indication

The IS_TX_MODE.request primitive is used to communicate the state of the PCS LPI transmit function to other sublayers in the PHY.

The IS_RX_MODE.request primitive is used to communicate the state of the PCS LPI receive function to other sublayers.

The IS_RX_TX_MODE.indication primitive is used to communicate the state of the rx_tx_mode parameter that reflects the inferred state of the link partner's tx_mode parameter from the PMA to other sublayers.

The IS_RX_LPI_ACTIVE.request primitive is used to communicate to the BASE-R FEC (see Clause 74) that the PCS has detected LPI signaling. This allows the FEC to use rapid block lock; the RS-FEC (see Clause 108) does not use this signal.

The IS_ENERGY_DETECT.indication primitive is used to communicate that the PMD has detected the return of energy on the interface following a period of quiescence.

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105.4.2 Instances of the Inter-sublayer service interface

The inter-sublayer interface can be instantiated between different sublayers, hence a prefix notation is defined to identify a specific instance of an inter-sublayer service interface. The following prefixes are defined:

a) PMD:—for primitives issued on the interface between the PMD sublayer and the PMA sublayer called the PMD service interface.
b) PMA:—for primitives issued on the interface between the PMA sublayer and the PCS (or the FEC) sublayer called the PMA service interface.
c) FEC:—for primitives issued on the interface between the FEC sublayer and the PCS (or the PMA) sublayer called the FEC service interface.

Examples of inter-sublayer service interfaces for 25GBASE-R with their corresponding instance names are illustrated in Figure 105–2 and Figure 105–3. For example, the primitives for one instance of the inter-sublayer service interface, named the PMD service interface are identified as follows:

PMD:IS_UNITDATA.request
PMD:IS_UNITDATA.indication
PMD:IS_SIGNAL.indication.

Primitives for other instances of inter-sublayer interfaces are represented in a similar manner as described above.

105.4.3 Semantics of inter-sublayer service interface primitives

The semantics of the inter-sublayer service interface primitives for the 25GBASE-R sublayers are described in 105.4.3.1 through 105.4.3.3.

105.4.3.1 IS_UNITDATA.request

The IS_UNITDATA.request primitive is used to define the transfer of a stream of data units from a sublayer to the next lower sublayer.

105.4.3.1.1 Semantics of the service primitive

IS_UNITDATA.request(tx_bit)

The data conveyed by IS_UNITDATA.request is a continuous stream of encoded bits. The tx_bit parameter can take one of two values: one or zero.

105.4.3.1.2 When generated

The sublayer continuously sends a bit stream IS_UNITDATA.request(tx_bit) to the next lower sublayer, at a nominal signaling rate of 25.78125 GBd.

105.4.3.1.3 Effect of receipt

The effect of receipt of this primitive is defined by the sublayer that receives this primitive.

105.4.3.2 IS_UNITDATA.indication

The IS_UNITDATA.indication primitive is used to define the transfer of a stream of data units from the sublayer to the next higher sublayer.

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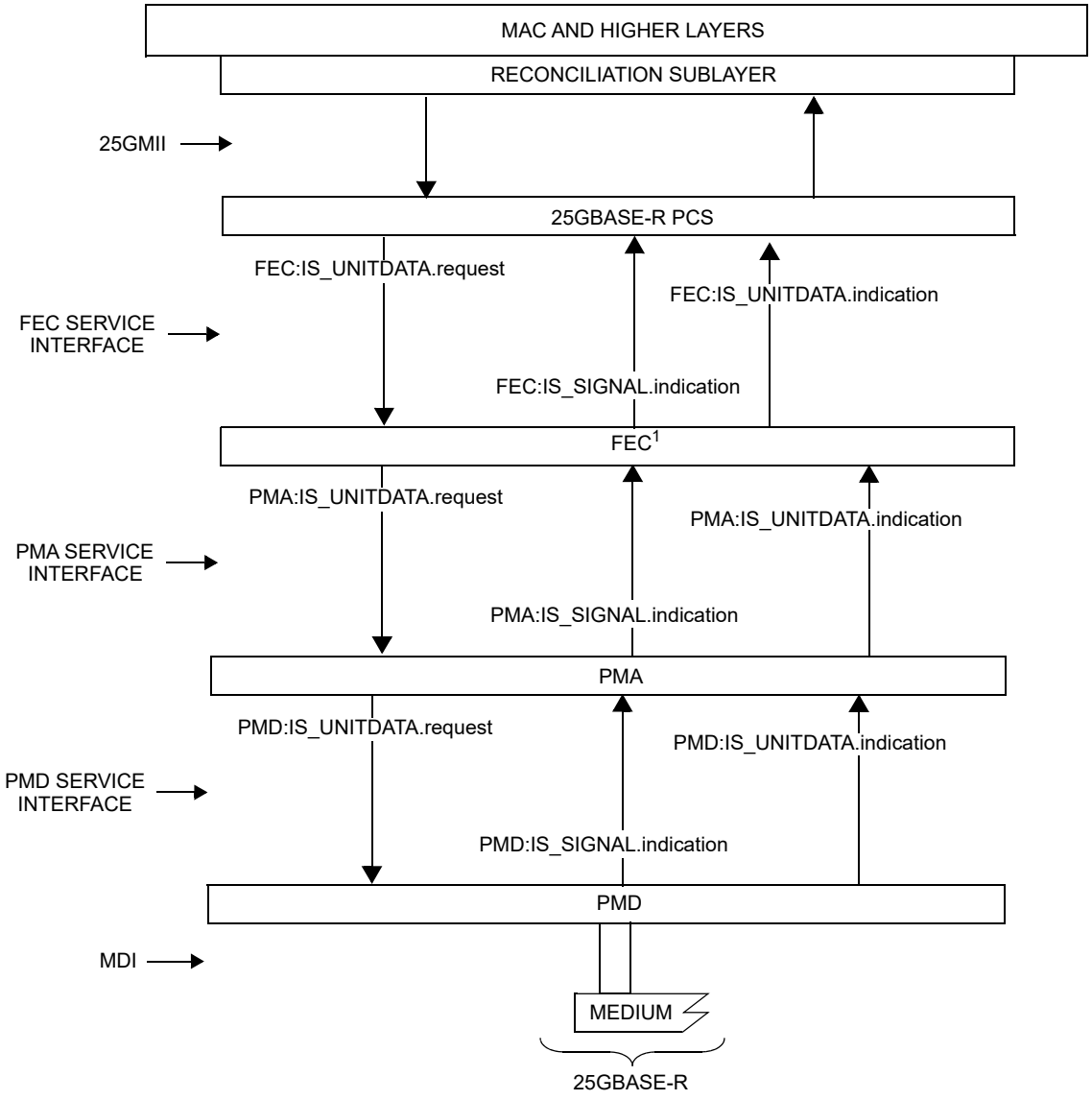

Figure 105–2—25GBASE-R inter-sublayer service interfaces

105.4.3.2.1 Semantics of the service primitive

IS_UNITDATA.indication(rx_bit)

The data conveyed by IS_UNITDATA.indication is a continuous stream of encoded bits. The rx_bit parameters can take one of two values: one or zero.

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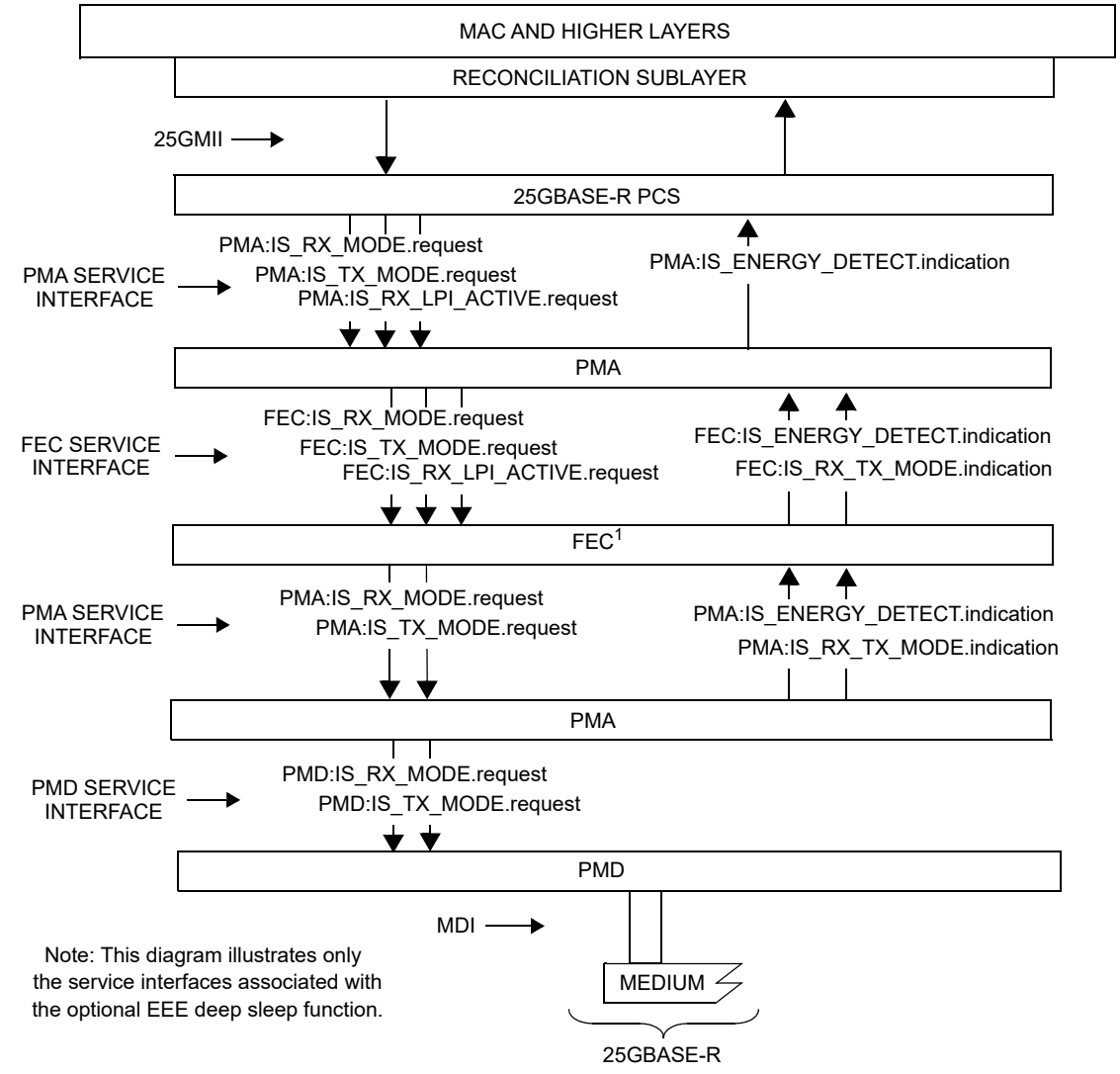

Figure 105–3—Optional inter-sublayer service interfaces for EEE deep sleep support

105.4.3.2.2 When generated

The sublayer continuously sends a bit stream IS_UNITDATA.indication(rx_bit) to the next higher sublayer, at a nominal signaling rate of 25.78125 GBd.

105.4.3.2.3 Effect of receipt

The effect of receipt of this primitive is defined by the sublayer that receives this primitive.

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105.4.3.3 IS_SIGNAL.indication

The IS_SIGNAL.indication primitive is generated by the sublayer to the next higher sublayer to indicate the status of the receive process. This primitive is generated by the receive process to propagate the detection of severe error conditions (e.g., no valid signal being received by the sublayer that generates this primitive) to the next higher sublayer.

105.4.3.3.1 Semantics of the service primitive

IS_SIGNAL.indication(SIGNAL_OK)

The SIGNAL_OK parameter can take on one of the following two values: OK or FAIL. A value of FAIL denotes that invalid data is being presented (rx_bit parameters undefined) by the sublayer to the next higher sublayer. A value of OK does not guarantee valid data is being presented by the sublayer to the next higher sublayer.

105.4.3.3.2 When generated

The sublayer generates the IS_SIGNAL.indication primitive to the next higher sublayer whenever there is change in the value of the SIGNAL_OK parameter.

105.4.3.3.3 Effect of receipt

The effect of receipt of this primitive is defined by the sublayer that receives this primitive.

105.4.3.4 IS_TX_MODE.request

The IS_TX_MODE.request primitive communicates the tx_mode parameter generated by the PCS Transmit Process for EEE capability to invoke the appropriate PMA, FEC, and PMD transmit EEE states. Without EEE deep sleep mode capability, the primitive is never invoked and the sublayers behave as if tx_mode = DATA.

105.4.3.4.1 Semantics of the service primitive

IS_TX_MODE.request(tx_mode)

The tx_mode parameter takes on one of up to three values: DATA, QUIET, or ALERT.

105.4.3.4.2 When generated

This primitive is generated to indicate the low power mode of the transmit path.

105.4.3.4.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the sublayer that receives this primitive. In general, when tx_mode is DATA, the sublayer operates normally and when tx_mode is QUIET, the sublayer may go into a low power mode.

105.4.3.5 IS_RX_MODE.request

The IS_RX_MODE.request primitive communicates the rx_mode parameter generated by the PCS LPI receive function to other sublayers.

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Without EEE deep sleep mode capability, the primitive is never invoked and the sublayers behave as if rx_mode = DATA.

105.4.3.5.1 Semantics of the service primitive

IS_RX_MODE.request(rx_mode)

The rx_mode parameter takes on one of two values: DATA or QUIET.

105.4.3.5.2 When generated

This primitive is generated to indicate the state of the PCS LPI receive function.

105.4.3.5.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the sublayer that receives this primitive. In general, when rx_mode is DATA, the sublayer operates normally and when rx_mode is QUIET, the sublayer may go into a low power mode.

105.4.3.6 IS_RX_LPI_ACTIVE.request

The IS_RX_LPI_ACTIVE.request primitive communicates to the FEC that the PCS LPI receive function is active. This primitive may be passed through a PMA sublayer but has no effect on that sublayer. This primitive is only used for a PMA sublayer that is between the PCS and a Clause 74 FEC sublayer; in all other cases the primitive is never invoked and has no effect. Without EEE deep sleep mode capability, the primitive is never invoked and has no effect.

105.4.3.6.1 Semantics of the service primitive

IS_RX_LPI_ACTIVE.request(rx_lpi_active)

The parameter rx_lpi_active is Boolean.

105.4.3.6.2 When generated

This primitive is generated to indicate the state of the PCS LPI receive function. It is FALSE when in the RX_ACTIVE state and TRUE in all other states.

105.4.3.6.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the FEC sublayer that receives this primitive. When rx_lpi_active is true, the FEC sublayer uses rapid block lock to reestablish FEC operation following a period of quiescence.

105.4.3.7 IS_ENERGY_DETECT.indication

The IS_ENERGY_DETECT.indication primitive is used to communicate that the PMD has detected the return of energy on the interface following a period of quiescence. Without EEE deep sleep mode capability, the primitive is never invoked and has no effect.

105.4.3.7.1 Semantics of the service primitive

IS_ENERGY_DETECT.indication(energy_detect)

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The parameter energy_detect is Boolean.

105.4.3.7.2 When generated

This primitive is generated by the PMA, reflecting the state of the signal_detect parameter received from the PMD.

105.4.3.7.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the PCS sublayer that receives this primitive.

This parameter is used to indicate that activity has returned on the interface following a period of quiescence.

105.4.3.8 IS_RX_TX_MODE.indication

The IS_RX_TX_MODE.indication primitive communicates the rx_tx_mode parameter. This parameter indicates the value of tx_mode that the PMA sublayer has inferred from the received signal. Without EEE deep sleep capability, the primitive is never generated and the sublayers behave as if rx_tx_mode = DATA.

105.4.3.8.1 Semantics of the service primitive

IS_RX_TX_MODE.indication(rx_tx_mode)

The parameter rx_tx_mode is assigned one of the following values: DATA, QUIET, or ALERT.

105.4.3.8.2 When generated

This primitive is generated whenever there is change in the value of the rx_tx_mode parameter.

105.4.3.8.3 Effect of receipt

The specific effect of receipt of this primitive is defined by the sublayer that receives it.

105.5 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. Table 105–3 contains the values of maximum sublayer delay (sum of transmit and receive delays at one end of the link) in bit times as specified in 1.4 and pause_quanta as specified in 31B.2. If a PHY contains an Auto-Negotiation sublayer, the delay of the Auto-Negotiation sublayer is included within the delay of the PMD and medium.

Equation (105–1) specifies the calculation of bit time per meter of fiber or electrical cable based upon the parameter *n*, which represents the ratio of the speed of electromagnetic propagation in the fiber or electrical cable to the speed of light in a vacuum. The value of *n* should be available from the fiber or electrical cable manufacturer, but if no value is known then a conservative delay estimate can be calculated using a default value of $n = 0.66$. The speed of light in a vacuum is $c = 3 \times 10^8$ m/s. Table 44–3 can be used to convert fiber or electrical cable delay values specified relative to the speed of light or in nanoseconds per meter.

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$$\text{Cable delay} = \frac{25 \times 10^9}{nc} \text{ BT/m} \quad (105\text{–}1)$$

See 31B.3.7 for PAUSE reaction timing constraints for stations at operating speeds of 25 Gb/s.

Table 105–3—Sublayer delay constraints

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
25G RS, MAC, and MAC Control	8 192	16	327.68	See 106.1.4.
25GBASE-R PCS	3 584	7	143.36	See 107.4.
25G BASE-R FEC	6 144	12	245.76	See 74.6.
25GBASE-R RS-FEC	24 576	48	983.04	See 108.4.
25GBASE-R PMA[d]	4 096	8	163.84	See 109.5.
25GBASE-CR PMD	512	1	20.48	See 110.4.
25GBASE-CR-S PMD	512	1	20.48	See 110.4.
25GBASE-KR PMD	512	1	20.48	See 111.4.
25GBASE-KR-S PMD	512	1	20.48	See 111.4.
25GBASE-SR PMD	512	1	20.48	See 112.3.
25GBASE-LR PMD	512	1	20.48	See 114.3.
25GBASE-ER PMD	512	1	20.48	See 114.3.
25GBASE-T PHY	25 600	50	1024	See 113.11.
25GBASE-BR10 PMD	512	1	20.48	See 158.3.
25GBASE-BR20 PMD	512	1	20.48	See 158.3.
25GBASE-BR40 PMD	512	1	20.48	See 158.3.

[a]1 bit time (BT) is equal to 40 ps. (See 1.4.215 for the definition of bit time.)
[b]1 pause_quantum is equal to 20.48 ns. (See 31B.2 for the definition of pause_quanta.)
[c]Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.
[d]Cumulative round-trip delay contributed by up to four PMA stages in a PHY.

105.6 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

Multiple states of a function that have a transition to a common state utilizing different qualifiers (for example, multiple exit conditions to an IDLE or WAIT state) may be indicated by a shared arrow. An exit transition arrow connects to the shared arrow, and the qualifier is met prior to termination of the transition arrow on the shared arrow. The shared arrow has no qualifier.

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105.7 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 45, Clause 73, Clause 74, Clause 106 through Clause 112, Clause 114, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the 25 Gigabit Ethernet PICS conforms to the same notation and conventions used in 21.6.

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106. Reconciliation Sublayer (RS) and Media Independent Interface (25GMII) for 25 Gb/s operation

106.1 Overview

This clause defines the characteristics for the Reconciliation Sublayer (RS) and the 25 Gigabit Media Independent Interface (25GMII) between the Ethernet MAC and PHY. Figure 106–1 shows the relationship of the RS and 25GMII to the ISO/IEC (IEEE) OSI reference model. The 25 Gb/s RS has identical logical functionality to the 10 Gb/s RS defined in Clause 46. A physical implementation and associated electrical characteristics for the 25GMII are not defined.

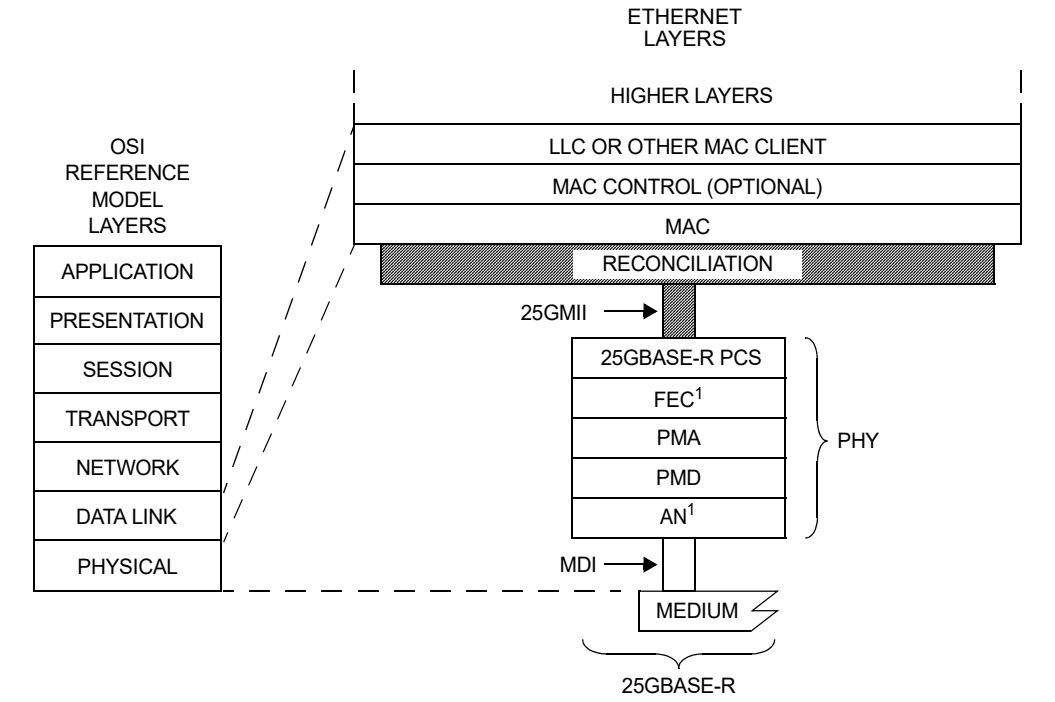

Figure 106–1—RS and 25GMII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The 25GMII is an optional logical interface between the MAC sublayer and the Physical Layer device.

The RS adapts the bit serial protocols of the MAC to the parallel format of the PCS service interface. Though the 25GMII is an optional interface, it is used extensively in this standard as a basis for specification. The 25 Gb/s Physical Coding Sublayer (PCS) is specified to the 25GMII, so if not implemented, a conforming implementation behaves functionally as if the RS and 25GMII were implemented.

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The 25GMII has the following characteristics:

a) It is capable of supporting 25 Gb/s operation.
b) Data and delimiters are synchronous to clock reference.
c) It provides independent 32-bit-wide transmit and receive data paths.
d) It provides for full duplex operation only.

106.1.1 Summary of major concepts

The following are the major concepts of 25GMII:

a) The 25GMII is functionally similar to other media independent interfaces that have been defined for other speeds, as they all define an interface allowing independent development of MAC and PHY logic.
b) The RS converts between the MAC serial data stream and the parallel data paths of the 25GMII.
c) The RS maps the signal set provided at the 25GMII to the PLS service primitives provided at the MAC.
d) Each direction of data transfer is independent and serviced by data, control, and clock signals.
e) The RS generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.
f) The RS participates in link fault detection and reporting by monitoring the receive path for status reports that indicate an unreliable link and generating status reports on the transmit path to report detected link faults to the DTE on the remote end of the connecting link.
g) The 25GMII may also support Low Power Idle (LPI) signaling for PHY types supporting Energy-Efficient Ethernet (EEE) (see Clause 78).

106.1.2 Application

This logical interface is used to provide media independence so that an identical MAC may be used with all 25GBASE PHY types.

106.1.3 Rate of operation

The 25GMII is specified to support 25 Gb/s operation.

106.1.4 Delay constraints

The maximum cumulative MAC Control, MAC, and RS round-trip (sum of transmit and receive) delay shall meet the values specified in Table 106–1. Bit time is defined in 1.4, and pause_quanta is defined in 31B.2.

Table 106–1—Round-trip delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)
MAC, RS, and MAC Control	8192	16

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106.1.5 Allocation of functions

The allocation of functions at the 25GMII balances the need for media independence with interface simplicity. The 25GMII maximizes media independence by separating the Data Link and Physical Layers of the OSI seven-layer reference model.

106.1.6 25GMII structure

The 25GMII structure is identical to the XGMII structure specified in 46.1.6.

106.1.7 Mapping of 25GMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the 25GMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 25 Gb/s; therefore, PLS service primitives supporting CSMA/CD operation are not mapped through the RS to the 25GMII. The mapping is changed if EEE capability is supported (see 78.3). This behavior and restrictions are the same as described in 22.7, with the details of the signaling described in 106.3. LPI_REQUEST shall not be set to ASSERT unless the attached link has been operational for at least one second (i.e., link_status = OK, according to the underlying PCS/PMA).

EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

Mappings for the following primitives are defined for 25 Gb/s operation:

PLS_DATA.request
PLS_DATA.indication
PLS_CARRIER.indication
PLS_SIGNAL.indication
PLS_DATA_VALID.indication

106.1.7.1 Mapping of PLS_DATA.request

The RS maps the primitive PLS_DATA.request to the 25GMII signals TXD<31:0>, TXC<3:0>, and TX_CLK in the same way as for the XGMII as specified in 46.1.7.1.

106.1.7.2 Mapping of PLS_DATA.indication

The RS maps the primitive PLS_DATA.indication to the 25GMII signals RXD<31:0>, RXC<3:0> and RX_CLK in the same way as for the XGMII as specified in 46.1.7.2.

106.1.7.3 Mapping of PLS_CARRIER.indication

25 Gb/s operation supports full duplex operation only. The RS never generates the PLS_CARRIER.indication primitive for PHYs that do not support EEE or Link Interruption.

For PHYs that support EEE capability, CARRIER_STATUS is set in the same way as specified in 46.1.7.3.

106.1.7.4 Mapping of PLS_SIGNAL.indication

25 Gb/s operation supports full duplex operation only. The RS never generates the PLS_SIGNAL.indication primitive.

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106.1.7.5 Mapping of PLS_DATA_VALID.indication

The RS maps the primitive PLS_DATA_VALID.indication to the 25GMII signals RXC<3:0> and RXD<31:0> in the same way as for the XGMII as specified in 46.1.7.5.

106.2 25GMII data stream

The 25GMII data stream has the same characteristics as the XGMII data stream described in 46.2.

106.3 25GMII functional specifications

The 25GMII functions identically to the XGMII specified in 46.3 with the exception that the TX_CLK and RX_CLK frequency shall be 390.625 MHz ±100 ppm (also one-sixty-fourth of the MAC transmit data rate).

106.4 LPI Assertion and Detection

25 Gb/s PHYs may support Clause 78 Energy-Efficient Ethernet (see Table 105–2).

LPI signaling by the 25 Gb/s RS is identical to that defined for XGMII in 46.4.

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been de-asserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake-up time is enforced by the transmit LPI state diagram using CARRIER_SENSE.indication in an identical manner to that defined in 46.4.

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106.5 Protocol implementation conformance statement (PICS) proforma for Clause 106 Reconciliation Sublayer (RS) and Media Independent Interface (25GMII) for 25 Gb/s operation[179]

106.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 106, Reconciliation Sublayer (RS) and Media Independent Interface (25GMII) for 25 Gb/s operation, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

106.5.2 Identification

106.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

106.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 106, Reconciliation Sublayer (RS) and Media Independent Interface (25GMII) for 25 Gb/s operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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106.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PHY	PHY support of 25GMII	106.2, 106.3		O	Yes [ ] No [ ]
*RS	Reconciliation Sublayer support of 25GMII	106.2, 106.3		O	Yes [ ] No [ ]
*LPI	Implementation of LPI	106.1.7		O	Yes [ ] No [ ]

106.5.3 PICS proforma Tables for Reconciliation Sublayer and 25 Gigabit Media Independent Interface

106.5.3.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	PHY support of MAC data rate	106.1.3	Support MAC data rate of 25 Gb/s	PHY:M	Yes [ ] N/A [ ]
G2	Cumulative MAC Control, MAC and RS round-trip delay	106.1.4	Per Table 106–1	RS:M	Yes [ ] N/A [ ]

106.5.3.2 Mapping of PLS service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
PL1	Mapping to Clause 6	106.1.7	RS implements mapping to Clause 6 PLS service primitives	RS:M	Yes [ ] N/A [ ]

106.5.3.3 25GMII signal functional specifications.

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	TX_CLK active edges	106.3	TXD and TXC sampled on both edges of TX_CLK	RS:M	Yes [ ] N/A [ ]
FS2	TX_CLK frequency	106.3	390.625 MHz ± 100 ppm	RS:M	Yes [ ] N/A [ ]
FS3	RX_CLK active edges	106.3	RXD and RXC sampled on both edges of RX_CLK	RS:M	Yes [ ] N/A [ ]
FS4	RX_CLK frequency	106.3	390.625 MHz ± 100 ppm when received data rate is within tolerance	RS:M	Yes [ ] N/A [ ]

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107. Physical Coding Sublayer (PCS) for 64B/66B, type 25GBASE-R

107.1 Overview

107.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) that is common to a family of 25 Gb/s Physical Layer implementations known as 25GBASE-R. The 25GBASE-R PCS is a sublayer of the 25 Gb/s PHYs listed in Table 105–1. The term 25GBASE-R is used when referring generally to Physical Layers using the PCS defined in this clause.

107.1.2 Relationship of 25GBASE-R to other standards

Figure 107–1 depicts the relationships among the 25GBASE-R sublayers, the Ethernet MAC and reconciliation layers, and the higher layers.

The 25GBASE-R PCS is identical to the 10GBASE-R PCS specified in Clause 49 with three exceptions:

1) It has a single-bit interface to the Physical Medium Attachment (PMA) sublayer rather than the 16-bit interface described in Clause 49.
2) It has the ability to generate the scrambled idle test pattern.
3) hi_ber is asserted if ber_cnt reaches 97 in a 2 ms period. This differs from the definition in 49.2.13.3, which defines hi_ber as occurring if ber_cnt reaches 16 in a 125 µs period.

107.1.3 Summary of 25GBASE-R sublayers

Figure 107–1 shows the relationship of the 25GBASE-R PCS sublayer with other sublayers to the ISO Open System Interconnection (OSI) reference model.

107.1.3.1 Physical Coding Sublayer (PCS)

The PCS service interface is the 25GMII, which is defined in Clause 106. The 25GMII is identical to the XGMII, which is the service interface of the 10GBASE-R PCS, but operates with 390.625 MHz clocks rather than 156.25 MHz clocks. The 25GMII provides a uniform interface to the Reconciliation Sublayer for all 25 Gb/s PHY implementations.

The 25GBASE-R PCS provides all services required by the 25GMII.

107.1.4 Inter-sublayer interfaces

The upper interface of the PCS may connect to the Reconciliation Sublayer through the 25GMII. The lower interface of the PCS connects to the PMA sublayer to support a PMD. If an FEC sublayer is implemented and the optional physical instantiation of 25GAUI is not implemented directly below the PCS sublayer, then the lower PCS interface connects to the FEC sublayer. The 25GBASE-R PCS has a nominal rate at the PMA (or FEC) service interface of 25.78125 Gb/s, which provides capacity for the MAC data rate of 25 Gb/s.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

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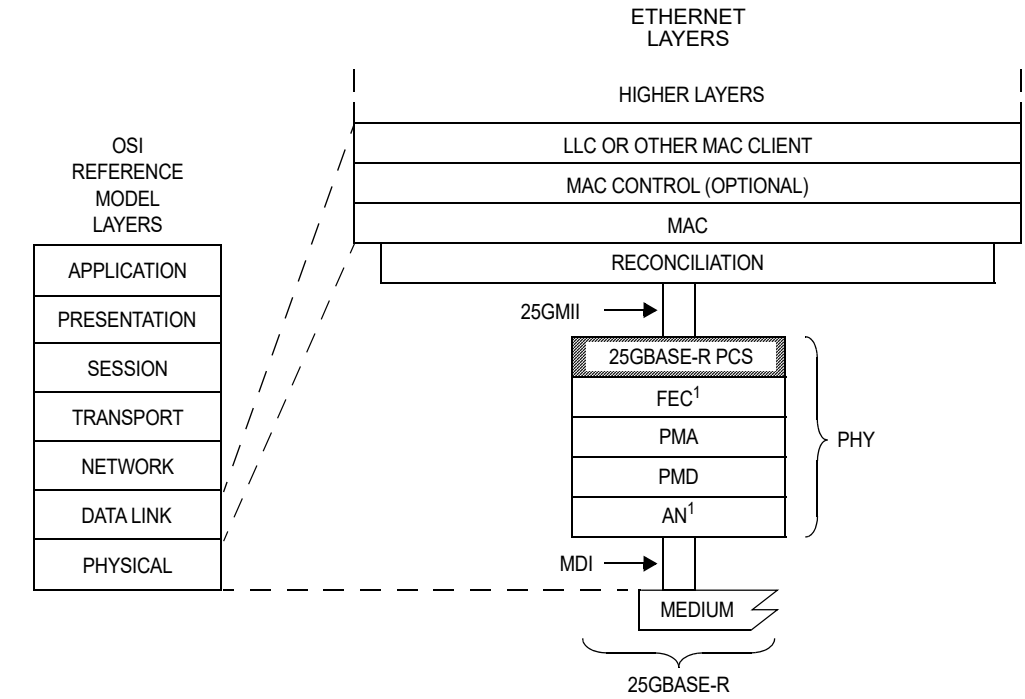

Figure 107–1—25GBASE-R PCS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

107.1.4.1 PCS service interface (25GMII)

The PCS service interface allows the 25GBASE-R PCS to transfer information to and from a PCS client. The PCS client is the Reconciliation Sublayer. The PCS service interface is defined as the 25GMII in Clause 106.

107.1.4.2 Physical Medium Attachment (PMA) service interface

The PMA (or FEC) service interface for the PCS is described in an abstract manner and does not imply any particular implementation. The PMA (or FEC) Service Interface supports the exchange of encoded data between the PCS and PMA (or FEC) sublayer. The PMA (or FEC) service interface is single-bit and defined in 109.2 and is an instance of the inter-sublayer service interface definition in 105.4.

107.2 Functions within the PCS

The 25GBASE-R PCS shall have all the functionality of the 10GBASE-R PCS specified in Clause 49. In addition, the PCS has the ability to generate the scrambled idle test-pattern generator specified in 107.2.3.

The BER monitor state diagram shown in Figure 49–15 still applies but it shall use a 2 ms timer instead of a 125 µs timer and ber_cnt is tested for a value of 97 rather than 16 in the exit conditions from state BER_BAD_SH. So:

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1) The definition of "125us_timer" in 49.2.13.2.5 is replaced with "Timer that is triggered every 2 ms +1%, –25%".
2) The definition of "ber_cnt" in 49.2.13.2.4 is replaced with "Count up to a maximum of 97 of the number of invalid sync headers within the current 2 ms period".
3) The definition of "hi_ber" in 49.2.13.2.2 is replaced with "Boolean variable that is asserted true when the ber_cnt reaches 97 indicating a bit error ratio $>10^{-4}$".

The PCS encodes data and control information into 66-bit blocks. The relationship of block bit positions to the 25GMII, PMA, and other PCS constructs is illustrated in Figure 107–2 for transmit and Figure 107–3 for receive.

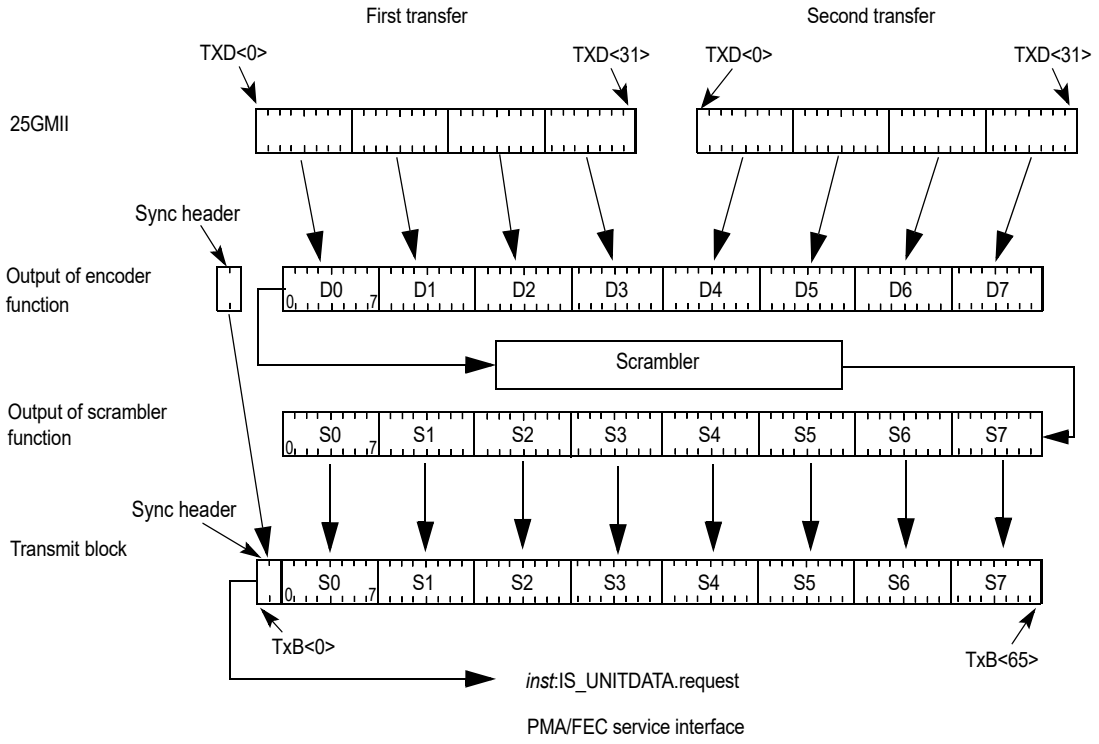

Figure 107–2—PCS Transmit bit ordering

107.2.1 Notation conventions

Values represented in binary are shown with the first transmitted bit (the LSB) on the left.

Two consecutive 25GMII transfers provide eight characters that are encoded into one 66-bit transmission block.

107.2.2 Transmission order

Block bit transmission order is illustrated in Figure 107–2 and Figure 107–3. Note that these figures show the mapping from 25GMII to 64B/66B block for a block containing eight data characters.

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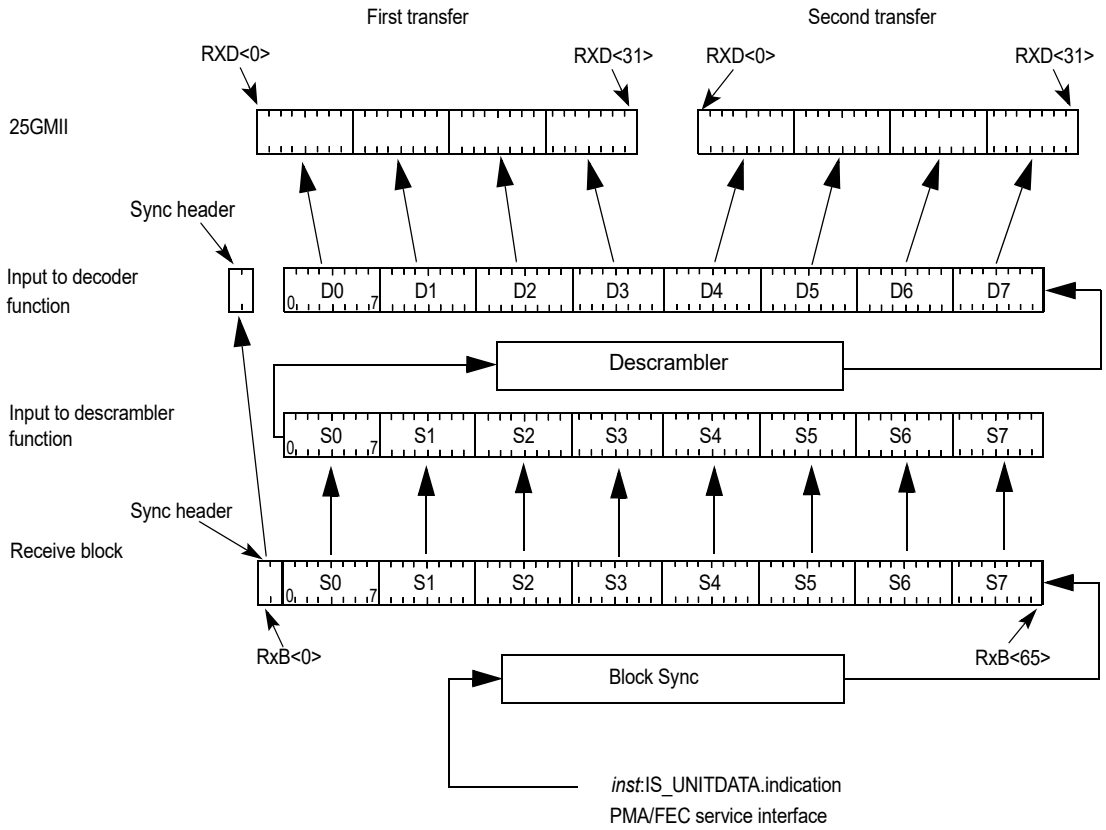

Figure 107–3—PCS Receive bit ordering

107.2.3 Test-pattern generator

In addition to those patterns specified in 49.2.8, the PCS shall have the ability to generate a scrambled idle test pattern. This test pattern is suitable for receiver tests and for certain transmitter tests.

When enabled, the scrambled idle test pattern is generated by the scrambler. The input to the scrambler is a control block (block type=0x1E) with all idles as defined in Figure 49–7. Sync headers are added to the scrambled data output.

If a Clause 45 MDIO is implemented, then control of the test-pattern generation is from the BASE-R PCS test-pattern control register (3.42).

107.3 LPI

If the 25GBASE-R PCS is part of a PHY configured for EEE deep sleep operation, the PCS shall follow the state diagrams specified in Figure 49–12 and Figure 49–13.

The LPI functions shall use the timer values in Table 107–1 and Table 107–2 for EEE deep sleep operation.

If the 25GBASE-R PCS is part of a PHY configured for EEE fast wake operation, the PCS shall encode and decode LPI when indicated but the state diagrams specified in Figure 49–12 and Figure 49–13 do not apply. Management functions may use MDIO register bit LPI_FW 3.20.0 to select fast wake operation (see 45.2.3.10.15).

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Table 107–1—Transmitter LPI timing parameters

Parameter	Description	Min	Max	Units
T_{SL}	Local Sleep Time from entering the TX_SLEEP state to when tx_mode is set to QUIET	4.9	5.1	µs
T_{QL}	Local Quiet Time from when tx_mode is set to QUIET to entry into the TX_ALERT state	1.7	1.8	ms
T_{WL}	Time spent in the TX_WAKE state	10.9	11.1	µs
T_{1U}	Time spent in the TX_ALERT and TX_SCR_BYPASS states	1.1	1.3	µs

Table 107–2—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for energy_detect to be set to TRUE while in the RX_SLEEP and RX_QUIET states before asserting receive fault	2	3	ms
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault (when scr_bypass_enable = FALSE)	—	11.5	µs
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault (when scr_bypass_enable = TRUE)	—	13.7	µs
T_{WTF}	Wake time fault recovery time	—	10	ms

107.4 Delay constraints

The maximum delay contributed by the 25GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 3584 BT (7 pause_quanta or 143.36 ns). A description of overall system delay constraints can be found in 105.5.

107.5 Support for Auto-Negotiation

A PCS used with a 25GBASE-KR PMD, 25GBASE-KR-S PMD, 25GBASE-CR PMD, or 25GBASE-CR-S PMD has the same requirements to support auto-negotiation as a PCS used with a 10GBASE-KR PMD. These are specified in 49.2.16.

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107.6 Protocol implementation conformance statement (PICS) proforma for Clause 107, Physical Coding Sublayer (PCS) for 64B/66B, type 25GBASE-R[180]

107.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 107, Physical Coding Sublayer (PCS) for 64B/66B, type 25GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

107.6.2 Identification

107.6.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

107.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 107, Physical Coding Sub-layer (PCS) for 64B/66B, type 25GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[180]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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107.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
25GE	25GMII compatibility interface	106	Compatibility interface is supported	O	Yes [ ] No [ ]
MD	MDIO	45, 49.2.14	Registers and interface supported	O	Yes [ ] No [ ]
*LPI	Implementation of LPI	107.3		O	Yes [ ] No [ ]

107.6.4 25G PCS

107.6.4.1 Clause 49 functionality

Item	Feature	Subclause	Value/Comment	Status	Support
PCS1	Supports Clause 49 functionality	107.2		M	Yes [ ] No [ ]
PCS2	BER monitor runs over a longer window than specified in Clause 49	107.2		M	Yes [ ] No [ ]

107.6.4.2 Test-pattern generator

Item	Feature	Subclause	Value/Comment	Status	Support
TP1	Scrambled idle test-pattern ability	107.2.3		M	Yes [ ] No [ ]

107.6.4.3 LPI

Item	Feature	Subclause	Value/Comment	Status	Support
LP1	EEE deep sleep	107.3, 49	PHY configured for deep sleep operation	LPI:O	Yes [ ] No [ ] N/A[ ]
LP2	Use the correct timer values	107.3	Uses values from Table 107–1 and Table 107–2	LPI:O	Yes [ ] No [ ] N/A[ ]
LP3	EEE fast wake	107.3	Fast wake operation	LPI:M	Yes [ ] No [ ]

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107.6.4.4 Delay Constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS Delay Constraint	107.4	No more than 3584 BT for sum of transmit and receive path delays	M	Yes [ ] No [ ]

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108. Reed-Solomon forward error correction (RS-FEC) sublayer for 10GBASE-R and 25GBASE-R PHYs

108.1 Overview

108.1.1 Scope

This clause specifies a Reed-Solomon forward error correction (RS-FEC) sublayer for 10GBASE-R and 25GBASE-R PHYs. The specification is closely related to that of the RS-FEC sublayer for 100GBASE-R PHYs, specified in Clause 91. Annex 91A provides examples of RS-FEC codewords constructed with the method specified in this clause.

108.1.2 Position of RS-FEC in the 10GBASE-R and 25GBASE-R PHY sublayers

Figure 108–1 shows the relationship of the 10GBASE-R and 25GBASE-R RS-FEC sublayer to the ISO/IEC Open System Interconnection (OSI) reference model.

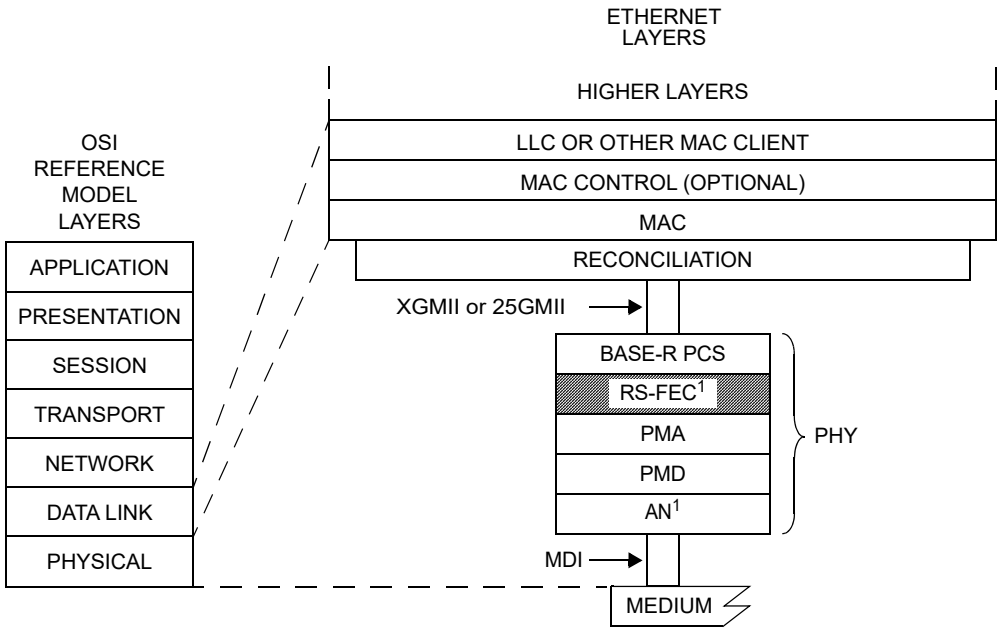

Figure 108–1—10GBASE-R and 25GBASE-R RS-FEC relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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108.1.3 Inter-sublayer interfaces

An FEC service interface is provided to allow the RS-FEC sublayer to transfer information to and from the PCS. An abstract service model is used to define the operation of this interface. For 10GBASE-R, the FEC service interface directly maps to the PMA service interface of the PCS defined in Clause 49 and the lower FEC sublayer interface maps to the service interface provided by the serial PMA sublayer defined in Clause 51. For 25GBASE-R, the FEC service interface is an instance of the inter-sublayer service interface defined in 105.4, as is the PMA service interface defined in 109.2.

This standard defines these interfaces in terms of bits, octets, data-group, data units, and signals; however, implementers may choose other data-path widths and other control mechanisms for implementation convenience, provided that the implementation adheres to the logical model of the service interface.

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108.1.3.1 Functional block diagram for 10GBASE-R PHYs

Figure 108–2 shows the functional block diagram of RS-FEC for 10GBASE-R PHYs and the relationship between the PCS and PMA sublayers.

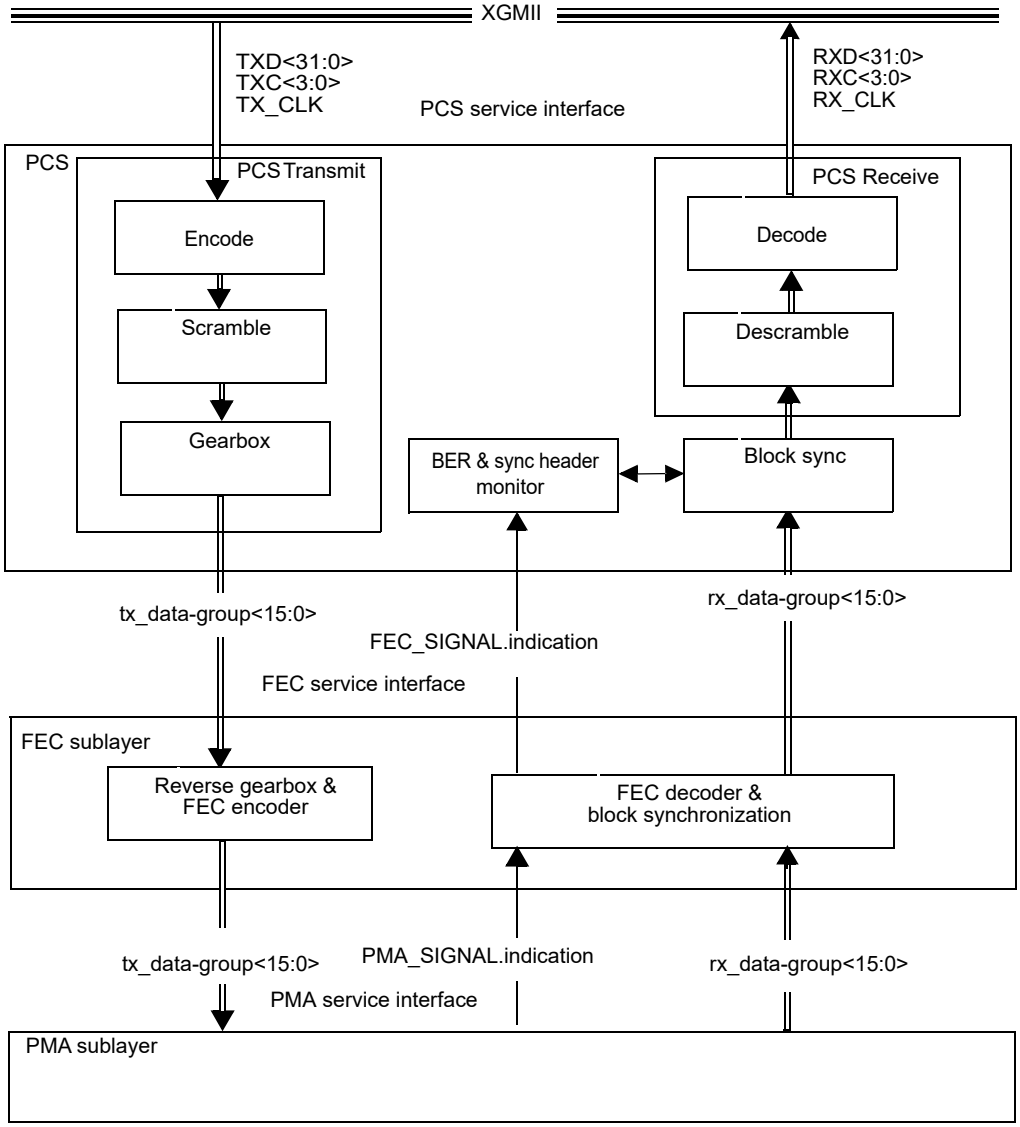

Figure 108–2—Functional block diagram for 10GBASE-R PHYs

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108.1.3.2 Functional block diagram for 25GBASE-R PHYs

Figure 108–3 shows the functional block diagram of FEC for 25GBASE-R PHYs and the relationship between the PCS and PMA sublayers.

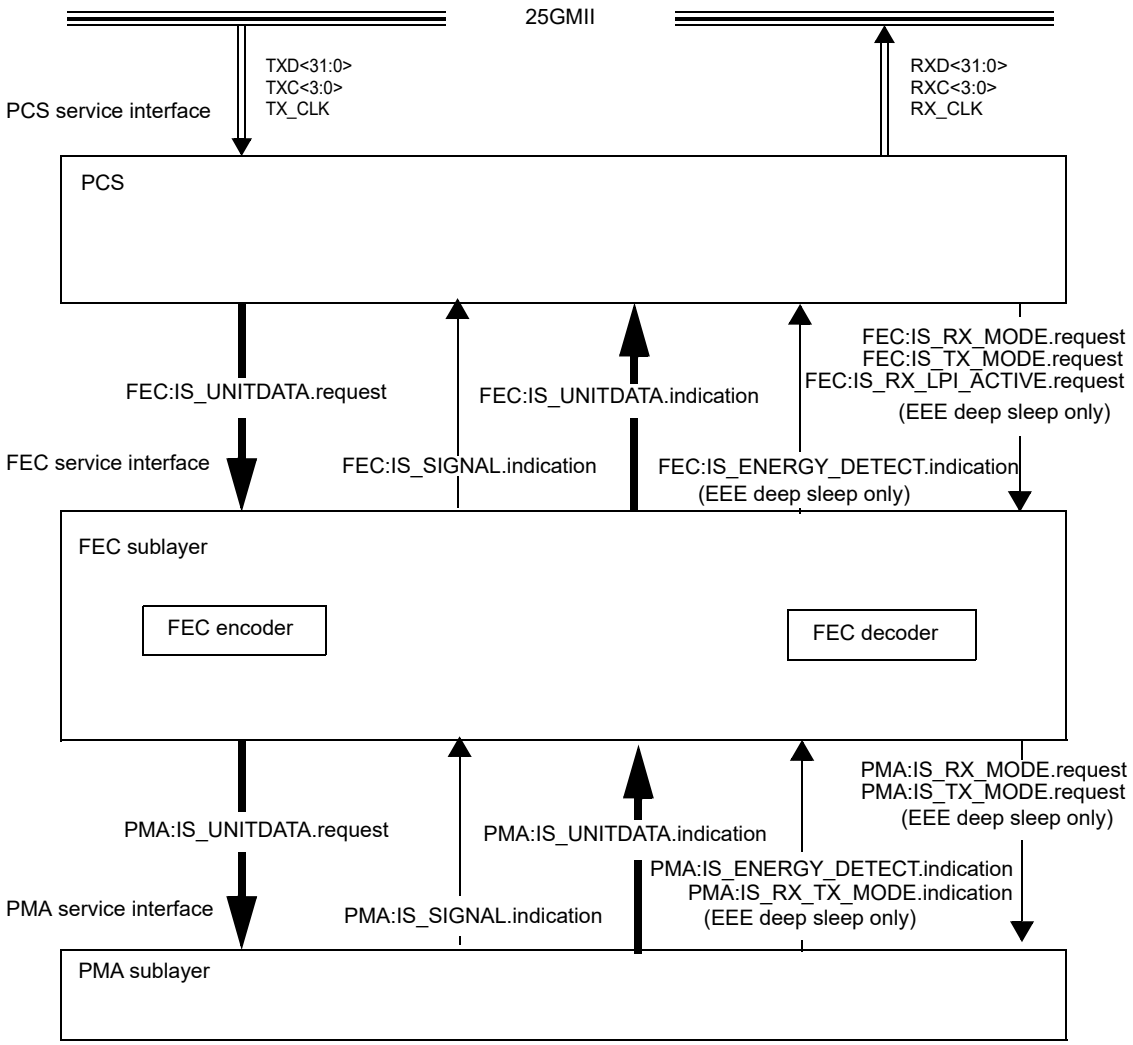

Figure 108–3—Functional block diagram for 25GBASE-R PHYs

108.2 FEC service interface

This subclause specifies the services provided by the 10GBASE-R and 25GBASE-R RS-FEC sublayer. The service interface is described in an abstract manner and does not imply any particular implementation.

The FEC service interface is provided to allow the PCS to transfer information to and from the RS-FEC. The FEC service interface is equivalent to the PMA service interface for 10GBASE-R PHYs and is an instance of the inter-sublayer service interface defined in 105.4 for 25GBASE-R PHYs.

The service primitives are defined differently for 10GBASE-R PHYs and for 25GBASE-R PHYs.

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The PCS may be connected to the 10GBASE-R and 25GBASE-R RS-FEC using an optional physical instantiation of the PMA service interface (see Clause 51 and Annex 109A), in which case a PMA is the client of the FEC service interface.

108.2.1 10GBASE-R service primitives

The following primitives are defined within the FEC service interface for 10GBASE-R PHYs:

FEC_UNITDATA.request(tx_data-group<15:0>)
FEC_UNITDATA.indication(rx_data-group<15:0>)
FEC_SIGNAL.indication(SIGNAL_OK)

The FEC service interface directly maps to the PMA service interface of the 10GBASE-R PCS defined in Clause 49. The FEC_UNITDATA.request maps to the PMA_UNITDATA.request primitive, the FEC_UNITDATA.indication maps to the PMA_UNITDATA.indication primitive, and the FEC_SIGNAL.indication maps to the PMA_SIGNAL.indication primitive of the 10GBASE-R PCS.

108.2.1.1 FEC_UNITDATA.request

This primitive defines the transfer of data in the form of constant-width data units from the PCS to the RS-FEC. The data supplied via FEC_UNITDATA.request is mapped by the RS-FEC transmit process into the payload capacity of the outgoing FEC block stream.

108.2.1.1.1 Semantics of the service primitive

FEC_UNITDATA.request(tx_data-group<15:0>)

The data conveyed by FEC_UNITDATA.request is a 16-bit vector representing a single data unit that has been prepared for transmission by the 10GBASE-R PCS Transmit process.

108.2.1.1.2 When generated

The 10GBASE-R PCS sends tx_data-group<15:0> to the RS-FEC at a nominal rate of 644.53125 MHz, corresponding to the 10GBASE-R signaling rate of 10.3125 GBd.

108.2.1.1.3 Effect of receipt

Upon receipt of this primitive, the RS-FEC transmit process maps the data conveyed by the tx_data unit<15:0> parameter into the payload of the transmitted FEC block stream, adds FEC overhead as required, scrambles the data, and transfers the result to the PMA via the PMA_UNITDATA.request primitives.

108.2.1.2 FEC_UNITDATA.indication

This primitive defines the transfer of received data in the form of constant-width data units from the RS-FEC to the PCS. FEC_UNITDATA.indication is generated by the RS-FEC receive process in response to FEC block data received from the PMA.

108.2.1.2.1 Semantics of the service primitive

FEC_UNITDATA.indication(rx_data-group<15:0>)

The rx_data-group<15:0> parameter is a 16-bit vector that represents the data unit transferred by the RS-FEC to the 10GBASE-R PCS.

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108.2.1.2.2 When generated

The RS-FEC sends one rx_data-group<15:0> to the 10GBASE-R PCS for each 16 bits received from the PMA sublayer. The nominal rate of generation of the FEC_UNITDATA.indication primitive is 644.53125 Mtransfers/s.

108.2.1.2.3 Effect of receipt

The effect of receipt of this primitive by the RS-FEC client is unspecified by the RS-FEC sublayer. See 49.2.

108.2.1.3 FEC_SIGNAL.indication

This primitive is sent by the RS-FEC to the PCS to indicate the status of the receive process. FEC_SIGNAL.indication is generated by the RS-FEC receive process in order to propagate the detection of severe error conditions (e.g., no valid signal being received from the PMA sublayer) to the PCS.

108.2.1.3.1 Semantics of the service primitive

FEC_SIGNAL.indication(SIGNAL_OK)

The SIGNAL_OK parameter can take one of two values: OK or FAIL. A value of OK denotes that the RS-FEC receive process is successfully delineating valid payload information from the incoming data stream received from the PMA sublayer indicated by the fec_signal_ok variable equal to true, and this payload information is being presented to the PCS via the FEC_UNITDATA.indication primitive. A value of FAIL denotes that errors have been detected by the Receive process indicated by the fec_signal_ok variable equal to false, that prevent valid data from being presented to the PCS, in this case the FEC_UNITDATA.indication primitive and its associated rx_data-group<15:0> parameter are meaningless.

108.2.1.3.2 When generated

The RS-FEC generates the FEC_SIGNAL.indication primitive to the 10GBASE-R PCS whenever there is a change in the value of the SIGNAL_OK parameter and FEC block synchronization is achieved.

108.2.1.3.3 Effect of receipt

The effect of receipt of this primitive by the RS-FEC client is unspecified by the RS-FEC sublayer. See 49.2.

108.2.2 25GBASE-R service primitives

For 25GBASE-R PHYs the FEC service interface is an instance of the inter-sublayer service interface defined in 105.4. The FEC service interface primitives are summarized as follows:

FEC:IS_UNITDATA.request(tx_bit)
FEC:IS_UNITDATA.indication(rx_bit)
FEC:IS_SIGNAL.indication

The PCS (or PMA) continuously sends a bit stream to the RS-FEC using the FEC:IS_UNITDATA.request(tx_bit) primitive, at a nominal signaling rate of 25.78125 GBd.

The RS-FEC continuously sends a bit stream to the PCS (or PMA) using the FEC:IS_UNITDATA.indication(rx_bit) primitive, at a nominal signaling rate of 25.78125 GBd. The actual signaling rate is equal to the underlying PMD signaling rate.

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The SIGNAL_OK parameter of the FEC:IS_SIGNAL.indication primitive can take one of two values: OK or FAIL. The value is set to OK when the RS-FEC receive function has identified codeword boundaries as indicated by FEC_align_status equal to true. That value is set to FAIL when the RS-FEC receive function is unable to reliably establish codeword boundaries as indicated by FEC_align_status equal to false.

If the optional EEE deep sleep capability is supported, then the FEC service interface includes four additional primitives as follows:

FEC:IS_TX_MODE.request
FEC:IS_RX_MODE.request
FEC:IS_RX_TX_MODE.indication
FEC:IS_ENERGY_DETECT.indication

When the tx_mode parameter of the FEC:IS_TX_MODE.request primitive is QUIET or ALERT, the RS-FEC sublayer may disable transmit functional blocks to conserve energy. Otherwise the RS-FEC transmit function operates normally. The value of tx_mode is passed to the client sublayer via the PMA:IS_TX_MODE.request primitive.

When the rx_mode parameter of the FEC:IS_RX_MODE.request primitive is QUIET, the RS-FEC sublayer may disable receive functional blocks to conserve energy. Otherwise the RS-FEC receive function operates normally. The value of rx_mode is passed to the client sublayer via the PMA:IS_RX_MODE.request primitive.

The rx_tx_mode parameter of the FEC:IS_RX_TX_MODE.indication primitive is used to communicate the link partner's value of tx_mode as inferred by the PMA. It is assigned the value that is received via the PMA:IS_RX_TX_MODE.indication primitive.

The energy_detect parameter of the FEC:IS_ENERGY_DETECT.indication primitive is used to communicate that the PMD has detected the return of energy on the interface following a period of quiescence. It is assigned the value that is received via the PMA:IS_ENERGY_DETECT.indication primitive.

108.3 PMA compatibility

For 10GBASE-R PHYs, the 10GBASE-R and 25GBASE-R RS-FEC sublayer is a client of the 10GBASE-R PMA subylayer defined in Clause 51. For 25GBASE-R PHYs, the 10GBASE-R and 25GBASE-R RS-FEC sublayer is a client of the 25GBASE-R PMA sublayer defined in Clause 109.

When 25GAUI C2C is used between a device that includes a PCS and a device that includes the RS-FEC, the 25GBASE-R PMA sublayer is the client of the 10GBASE-R and 25GBASE-R RS-FEC sublayer.

108.4 Delay constraints

The maximum delay contributed by the 10GBASE-R and 25GBASE-R RS-FEC sublayer (sum of transmit and receive delays at one end of the link) shall be no more than 24 576 bit times (48 pause_quanta). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 44.3 and 105.5.

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108.5 Functions within the RS-FEC sublayer

108.5.1 Functional block diagram

A functional block diagram of the RS-FEC sublayer is shown in Figure 108–4.

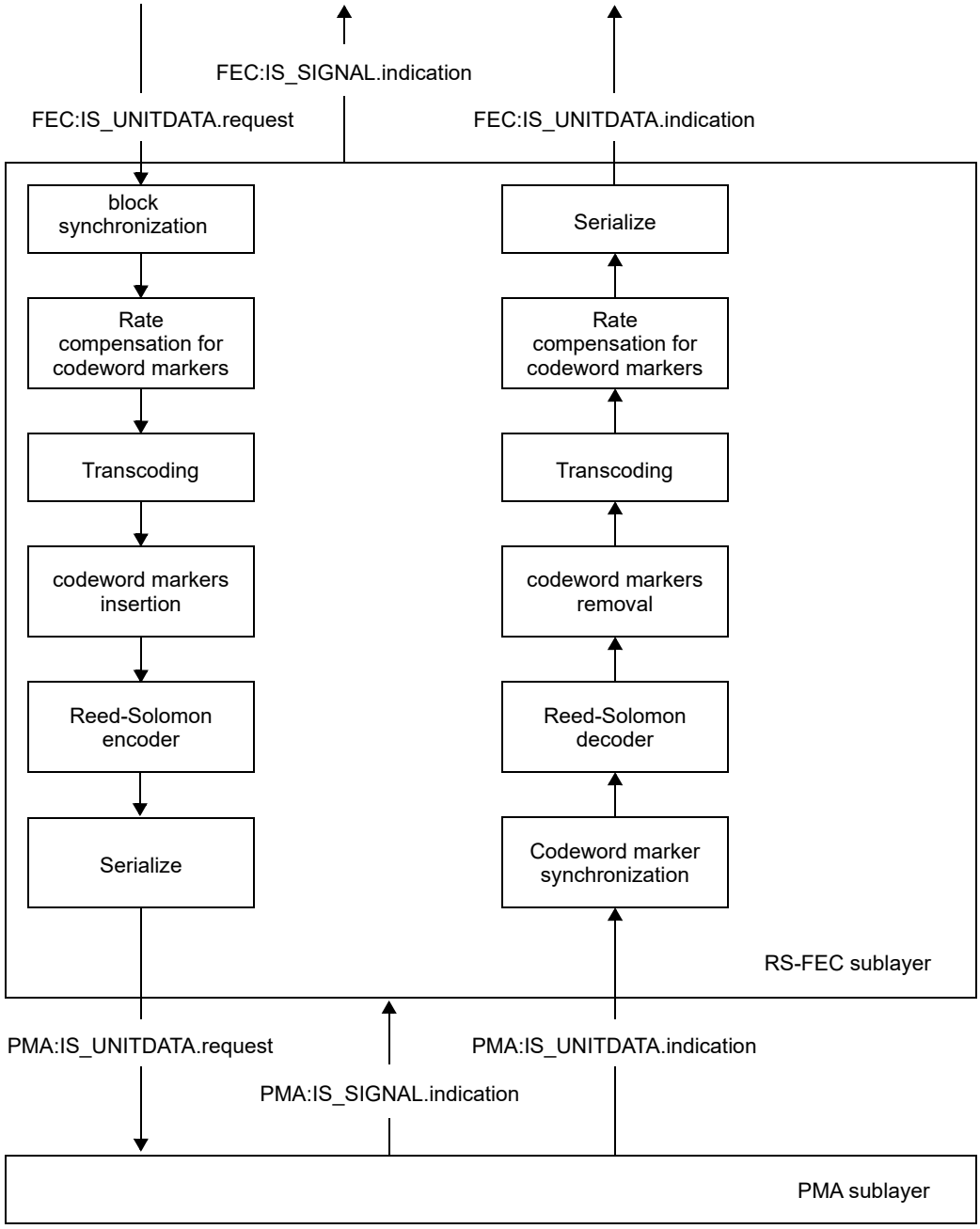

Figure 108–4—Functional block diagram

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108.5.1.1 Reverse gearbox and gearbox functions for 10GBASE-R

The reverse gearbox function adapts between the 66-bit width of the 64B/66B blocks and the 16-bit width of the PCS interface. It receives the 16-bit stream from the PCS interface and converts it back to 66-bit encoded blocks for the RS-FEC encoder to process. The reverse gearbox function operates in the same manner as the block synchronization function defined in 49.2.9.

The reverse gearbox function receives data via 16-bit FEC_UNITDATA.request primitives. It forms a bit stream from the primitives by concatenating requests with the bits of each primitive in order to form tx_data-group<0> to tx_data-group<15> (see Figure 49–6). It obtains lock to the 66-bit blocks in the bit stream using the sync headers and outputs 66-bit blocks. Lock is obtained as specified in the lock state diagram shown in Figure 49–14.

NOTE—Figure 49–6 shows rx_data-group<0> to rx_data-group<15> because the processing depicted in that figure is in the receive function. However, the reverse gearbox in this subclause is part of the transmit function, so it uses tx_data-group<0> to tx_data-group<15>.

The reverse gearbox functionality is necessary only when the optional PMA compatibility interface named XSBI is implemented between the PCS and RS-FEC functions, since that interface passes data via a 16-bit wide path. When the XSBI is not implemented, the internal data-path width between the PCS and RS-FEC is an implementation choice. Depending on the path width, the reverse gearbox function may not be necessary.

The gearbox adapts between the 66-bit width of the blocks and the 16-bit width of the PMA interface. It receives the 66-bit blocks. When the transmit channel is operating in normal mode, the gearbox sends 16 bits of transmit data at a time via the PMA_UNITDATA.request primitive. The UNITDATA.request primitive is fully packed with bits. For example, if one block happened to start with the sync header on bits 0 and 1 of a PMA_UNITDATA.request, then the last two bits of that block would be on bits 0 and 1 of a PMA_UNITDATA.request and the next block would begin with a sync header on bits 2 and 3 of that PMA_UNITDATA.request. When a PMA_UNITDATA.request contains bits from two blocks, then the bits from the first block shall be placed in the lowest numbered bits of tx_data-group<15:0>. The bits shall be packed into the tx_data-group in sequence with the lowest numbered bit of the block going into the lowest numbered bit of the part of tx_data-group<15:0> bits containing bits from that block (see Figure 49–5).

The gearbox functionality is necessary when the optional PMA compatibility interface, XSBI, is implemented since that interface passes data over a 16-bit wide path. When the XSBI is not implemented, the internal data-path width between the PCS and PMA is an implementation choice. Depending on the path width, the gearbox functionality may not be necessary.

108.5.2 Transmit function

108.5.2.1 Block synchronization

The RS-FEC transmit function uses the bit stream provided by the FEC:IS_UNITDATA.request primitive. It obtains lock to the 66-bit blocks in the bit stream using the sync headers and outputs 66-bit blocks. Block lock is obtained as specified in the lock state diagram shown in Figure 49–14.

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108.5.2.2 Rate compensation for codeword markers in the transmit direction

The RS-FEC transmit process periodically inserts codeword markers into the transcoded block stream (see 108.5.2.4). In order to maintain the same bit rate after codeword marker insertion, the RS-FEC transmit process shall perform the rate compensation function described below, or its functional equivalent:

a) Decode the PCS blocks received by descrambling (see 49.2.10) and applying the PCS receive process (see 49.2.11) to obtain the XGMII or 25GMII character stream.
b) Delete Idle control characters (/I/), Low Power Idle control characters (/LI/), and ordered sets, according to the rules in 49.2.4.7 and 49.2.4.10, to create room as necessary for the periodically occurring codeword markers.
c) Re-encode the data stream obtained, by applying the PCS transmit process (see 49.2.5) and scrambler (see 49.2.6) to obtain 64B/66B blocks.

If the optional EEE deep sleep capability is supported, when rapid codeword markers are sent, characters are deleted more frequently in item b) as necessary to maintain a constant bit rate.

NOTE—When rapid codeword markers are sent, the PCS LPI transmit state diagram (Figure 49–12) is in the TX_WAKE state, so the data encoded by the PCS comprises one of two control characters, either /I/ or /LI/. Both types of control characters can be deleted for rate compensation. See 78.1.3.1 and 78.1.3.3.1 for more details about LPI wake cycles.

108.5.2.3 64B/66B to 256B/257B transcoder

The transcoder constructs a 257-bit block, tx_scrambled<256:0>, from a group of four 66-bit blocks, tx_coded_*j*<65:0> where *j*=0 to 3. For each group of four 66-bit blocks, *j*=3 corresponds to the most recently received block. Bit 0 in each 66-bit block is the first bit received and corresponds to the first bit of the synchronization header.

The construction of the transcoded block shall be according to the process described in 91.5.2.5. For each 257-bit block, bit 0 shall be the first bit transmitted.

108.5.2.4 Codeword marker insertion

In order to support codeword alignment in the receive direction, the RS-FEC shall periodically insert codeword markers into the stream of transcoded blocks as the first 257 bits of every 1024th RS-FEC codeword (see 108.5.2.5). The distance between the beginning of successive codeword markers is therefore 20480 257-bit transcoded blocks, equivalent to 81920 64B/66B blocks.

Room for codeword markers is created by the rate compensation for codeword markers in the transmit direction process (see 108.5.2.2) such that the bit rates at the input and the output of the RS-FEC sublayer are equal.

The transmitted codeword marker is a 257-bit block, tx_cwm, constructed of four alignment markers followed by a zero bit. Each alignment marker is built from eight octets M_0, M_1, M_2, BIP_3, M_4, M_5, M_6, and BIP_7 with the bit order shown in Figure 82–9. The BIP_3 field is set to the constant value 0x33 and the BIP_7 field is set to the constant value 0xCC.

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tx_cwm is constructed as follows:

a) tx_cwm<63:0> are set to bits <65:2> of the alignment marker of PCS lane 0 defined in Table 82–2.
b) tx_cwm<127:64> are set to bits <65:2> of the alignment marker of PCS lane 1 defined in Table 82–3.
c) tx_cwm<191:128> are set to bits <65:2> of the alignment marker of PCS lane 2 defined in Table 82–3.
d) tx_cwm<255:192> are set to bits <65:2> of the alignment marker of PCS lane 3 defined in Table 82–3.
e) tx_cwm<256> is set to 0.

For the optional EEE deep sleep capability, a rapid method of codeword alignment is used following a transition of tx_mode from ALERT to DATA, by transmitting rapid codeword markers. When the value of tx_down_count is nonzero, rapid codeword markers are sent at the beginning of each codeword. Rapid codeword markers are identical to regular codeword markers, with the exception that BIP_3 is set to the value of tx_down_count instead of the constant 0x33 and BIP_7 is set to the bit-wise inversion of tx_down_count instead of the constant 0xCC.

108.5.2.5 Reed-Solomon encoder

The RS-FEC sublayer employs the Reed-Solomon code RS(528,514) operating over the Galois Field GF(2^{10}) where the symbol size is 10 bits. The encoder described in 91.5.2.7 shall be used.

108.5.2.6 Codeword serialization

Once the data has been Reed-Solomon encoded, it shall be serialized and sent to the PMA using the PMA:IS_UNITDATA.request primitive with the transmit bit ordering illustrated in Figure 108–5.

108.5.2.7 RS-FEC encoding for rapid codeword lock (EEE deep sleep)

If the optional EEE deep sleep capability is supported, the RS-FEC transmit function changes its signaling during LPI refresh and wake periods, as described in this subclause.

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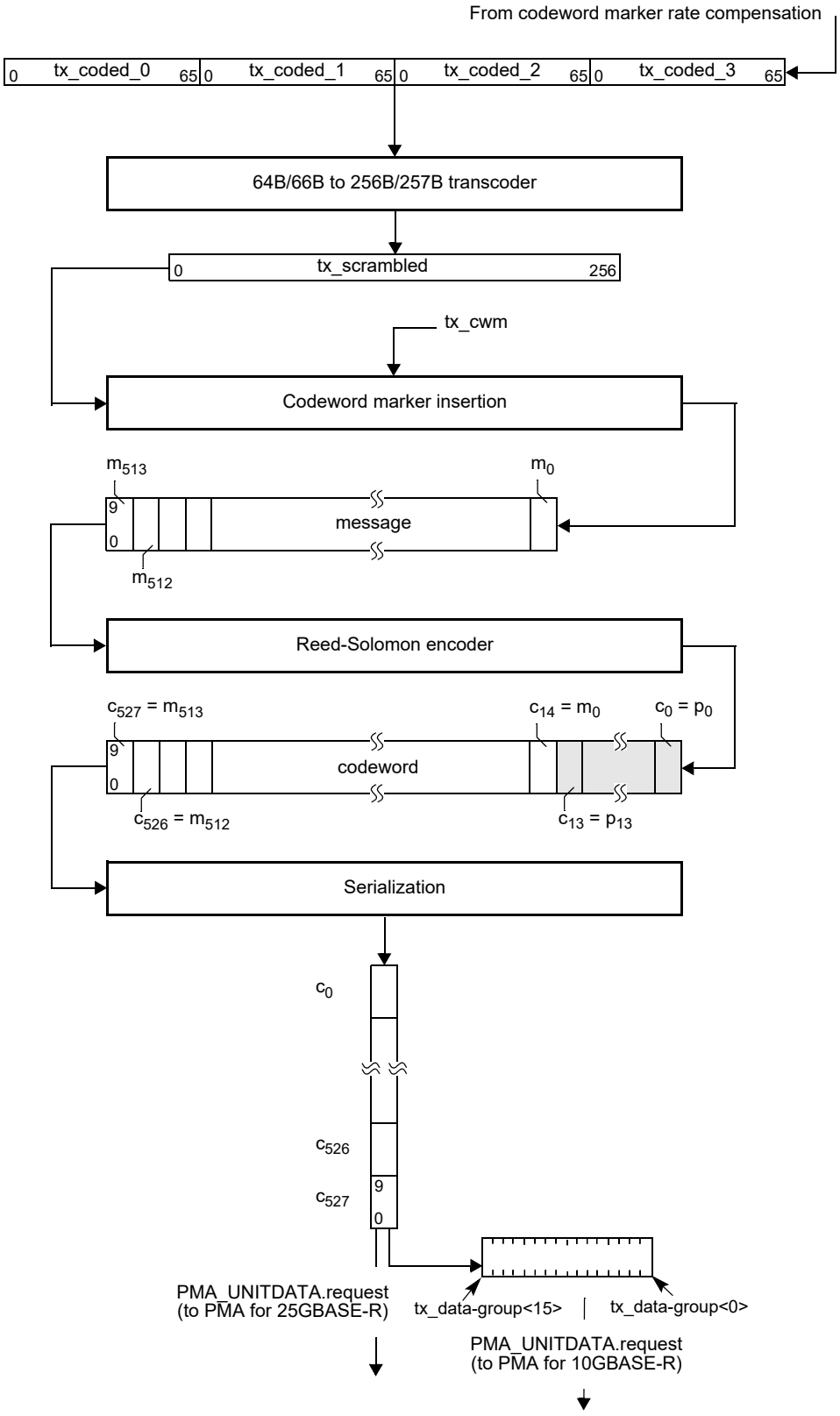

Figure 108–5—Transmit bit ordering

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The transition of the PCS LPI transmit state diagram (Figure 49–12) to TX_WAKE state is detected by the change of the tx_mode parameter of the FEC:IS_TX_MODE.request primitive from ALERT to DATA. Following this transition, the transmit function behaves as follows:

a) Set tx_down_count to 40. This causes the codeword marker insertion function (108.5.2.4) to insert a rapid codeword marker in the beginning of each of the following 40 codewords. The value of tx_down_count is encoded in each rapid codeword marker and is decremented after the rapid codeword marker is sent.

b) The rapid codeword marker with down_count=1 sets the location of the subsequent regular codeword markers, such that a codeword marker is inserted at the beginning of the 1024th codeword after it. Figure 108–6 depicts the codeword marker locations during this transition.

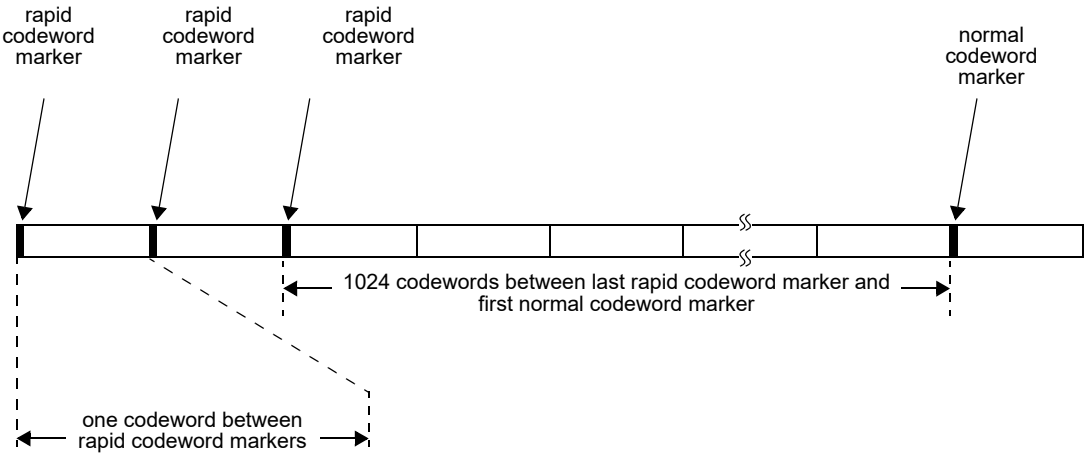

Figure 108–6—Transition from rapid to normal codeword markers

108.5.3 Receive function

108.5.3.1 Codeword marker lock

The RS-FEC shall implement the codeword marker lock process as described in this subclause.

The RS-FEC receive function forms a bit stream by concatenating the bits from the PMA:IS_UNITDATA.indication primitive in the order they are received. This process obtains lock to the codeword markers as shown in FEC synchronization state diagram (Figure 108–8). The status of the codeword marker lock process is reflected by the state variable FEC_align_status.

108.5.3.2 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the codeword, corrects them as necessary, and discards the parity symbols. The message symbols correspond to a codeword comprising 20 transcoded blocks rx_scrambled.

The RS-FEC sublayer shall be capable of correcting any combination of up to 7 symbol errors in a codeword. The RS-FEC sublayer shall also be capable of indicating when a codeword contains errors that were not corrected. The probability that the decoder fails to indicate a codeword with 8 or more symbol errors as uncorrected is expected to be lower than 10^{-6}.

The Reed-Solomon decoder may provide the option to perform error detection without error correction to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the

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assertion of the FEC_bypass_correction_ability variable (see 108.6.4). When the option is provided, it is enabled by the assertion of the FEC_bypass_correction_enable variable (see 108.6.1). This option shall not be used when the RS-FEC sublayer is used to form part of a 10GBASE-BR20, 25GBASE-SR, 25GBASE-LR, or 25GBASE-ER PHY.

NOTE 1—The PHY may rely on the error correction capability of the RS-FEC sublayer to achieve its performance objectives. It is recommended that acceptable performance of the underlying link is verified before error correction is bypassed.

The Reed-Solomon decoder shall indicate errors to the PCS sublayer by intentionally corrupting 66-bit block synchronization headers. When the decoder determines that a codeword contains errors (when the bypass correction feature is enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled), it ensures that, for every other 257-bit block within the codeword starting with the first (1st, 3rd, 5th, etc.), the synchronization header for the first 66-bit block at the output of the 256B/257B to 64B/66B transcoder, rx_coded_0<1:0>, is set to 11. In addition, it ensures that rx_coded_0<1:0> corresponding to the second 257-bit block and rx_coded_3<1:0> corresponding to the last (20th) 257-bit block in the codeword are set to 11.

NOTE 2—Setting rx_coded_0<1:0> to 11 as described causes the PCS to assign R_BLOCK_TYPE=E to the block and decode its content as EBLOCK_R (see 49.2.13.2.1 and 49.2.13.2.3). This will cause all frames 64 bytes and larger that are fully or partially within the codeword to be discarded.

The Reed-Solomon decoder may optionally provide the ability to bypass the error indication feature to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_indication_ability variable (see 108.6.5). When the option is provided it is enabled by the assertion of the FEC_bypass_indication_enable variable (see 108.6.2).

When FEC_bypass_correction_enable is asserted, the decoder shall not bypass error indication and the value of FEC_bypass_indication_enable has no effect.

When FEC_bypass_indication_enable is asserted, additional error monitoring is performed by the RS-FEC sublayer to reduce the likelihood that errors in a packet are not detected. The Reed-Solomon decoder counts the number of symbol errors detected in consecutive non-overlapping blocks of 8192 codewords. When the number of symbol errors in a block of 8192 codewords exceeds 417, the Reed-Solomon decoder shall cause synchronization header rx_coded<1:0> of each subsequent 66-bit block that is delivered to the PCS to be assigned a value of 00 or 11 for a period of 60 ms to 75 ms.

NOTE 3—This setting of rx_coded<1:0> marks the 64B/66B block as bad and inhibits processing of received packets by the PCS. The BER monitor state diagram (Figure 49–15) sets hi_ber to true and the PCS block_lock is set to false. When AN is supported and enabled, this event causes AN to restart.

For the optional EEE deep sleep capability, the error monitor employed when FEC_bypass_indication_enable is asserted shall be disabled when rx_lpi_active is true. The next block of 8192 codewords considered by the error monitor begins on the codeword boundary following the transition of rx_lpi_active from true to false.

108.5.3.3 Codeword monitor

After codeword marker lock has been achieved, this process continuously checks codeword validity as indicated by the codeword monitor state diagram (Figure 108–9). When three consecutive uncorrected codewords are detected, the codeword monitor shall restart the codeword marker lock process. In such event, it is likely that multiple blocks are marked as bad until codeword marker alignment is found.

NOTE—Marking multiple 64B/66B blocks as bad causes the PCS to assert hi_ber and lose its block lock. When AN is supported and enabled, this event causes AN to restart.

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108.5.3.4 Codeword marker removal

The first 257 message bits in every 1024th codeword is the vector rx_cwm<256:0> where bit 0 is the first bit received. The specific codewords that include this vector are indicated by the codeword marker lock function (108.5.3.1).

For the optional EEE deep sleep capability, when FEC_align_status is true and rx_down_count is nonzero, rx_cwm<256:0> is set to the first 257 message bits in every codeword.

The vector rx_cwm shall be removed prior to transcoding.

108.5.3.5 256B/257B to 64B/66B transcoder

The transcoder extracts a group of four 66-bit blocks, rx_coded_*j*<65:0> where *j*=0 to 3, from each 257-bit block rx_scrambled<256:0>. Bit 0 of the 257-bit block is the first bit received.

The transcoder described in 91.5.3.5 shall be used, with the exception that in step f2), h<3:0> is derived by cross-referencing to g<3:0> using Figure 49–7 instead of Figure 82–5, to account for the block types used by the PCS.

The transcoder creates a stream of 66-bit vectors rx_coded<65:0> from the groups of four blocks rx_coded_*j*<65:0> where *j*=0 to 3. rx_coded_0 is the first block transmitted out of each group.

108.5.3.6 Rate compensation for codeword markers in the receive direction

After the codeword markers have been discarded from transcoding and the stream of rx_coded<65:0> vectors has been obtained, to compensate for the deleted codeword markers, the RS-FEC receive process shall perform the rate compensation function described below, or its functional equivalent:

a) Decode the stream of rx_coded vectors by descrambling (see 49.2.10) and applying the PCS receive process (see 49.2.11) to obtain the XGMII or 25GMII character stream.
b) Insert /I/ or /LI/, according to the rules in 49.2.4.7, to fill in as necessary for any deleted codeword markers or rapid codeword markers.
c) Re-encode the data stream obtained, by applying the PCS transmit process (see 49.2.5) and scrambling (see 49.2.6) to obtain 64B/66B blocks rx_coded_out<65:0>.

If rx_coded<1:0> is either 00 or 11, the process in list item c) shall set rx_coded_out<1:0> to rx_coded<1:0> and the process in list item b) shall not insert idle characters at the next block after rx_coded_out.

If the optional EEE deep sleep capability is supported, this function sets rx_lpi_active according to the RX LPI state diagram (Figure 49–13).

108.5.3.7 Rapid codeword lock for EEE deep sleep

If the optional EEE deep sleep capability is supported, the RS-FEC receive function performs rapid codeword lock during LPI refresh and wake periods, as described in this subclause.

When rx_mode (or rx_tx_mode if appropriate) transitions from QUIET to DATA:

a) Start timer hold_off_timer.
b) Enable the RS-FEC rapid codeword lock mechanism, which attempts to detect rapid codeword markers sent by the remote RS-FEC transmit function (see 108.5.2.7). When two rapid codeword markers that are one codeword distance apart are detected (causing entry to state WAKE_GOOD in

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the FEC synchronization state diagram, Figure 108–8), the start location of the RS-FEC codeword is set to the start location of the rapid codeword markers. The next codeword marker position is set to 1024 codewords following the rapid codeword marker with down_count=1.

NOTE—The rapid codeword lock mechanism is implementation dependent and outside the scope of this standard.

When the start location is found, FEC_align_status is set to true and test_cw is asserted for each subsequent codeword, enabling aligned codeword decoding. Assuming the rapid codeword lock has determined the correct start of codeword location, the RS-FEC codeword monitor state diagram (Figure 108–9) reaches the CW_GOOD state, and then the decoding in item a) of 108.5.3.6 results in one of two deterministic blocks, composed of either /I/ or /LI/ control characters.

The RS-FEC sublayer shall hold off asserting SIGNAL_OK until one of the following two events occurs:

1) The RS-FEC codeword monitor state diagram (Figure 108–9) reaches the CW_GOOD state.
2) hold_off_timer_done = true.

108.5.3.8 Receive bit ordering

The receive bit ordering shall be as illustrated in Figure 108–7.

108.5.4 Detailed functions and state diagrams

108.5.4.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, functions, and counters. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

108.5.4.2 State variables

cw_bad
: Boolean variable that is set to true if the Reed-Solomon decoder (see 108.5.3.2) detects any errors in the current codeword and does not correct them, and is set to false otherwise.

cwm_counter_done
: Boolean variable that indicates that cwm_counter has reached its terminal count.

cwm_valid
: Boolean variable that is set to true if the received block rx_cwm<256:0> (as defined in 108.5.3.4) is a valid codeword marker. Codeword marker validity is tested by comparing bits 23:0 and 55:32 of rx_cwm<256:0>, on a nibble-wise basis (12 comparisons), against their respective values in tx_cwm<256:0> (as defined in 108.5.2.4). If nine or more nibbles in the candidate block match the corresponding known nibbles in the codeword marker, the candidate block is considered a valid codeword marker.

FEC_align_status
: Boolean variable that is set to true when the receiver has found the alignment of the codeword marker on the PMA service interface.

reset
: Boolean variable that controls the resetting of the RS-FEC sublayer. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the RS-FEC sublayer into low-power mode.

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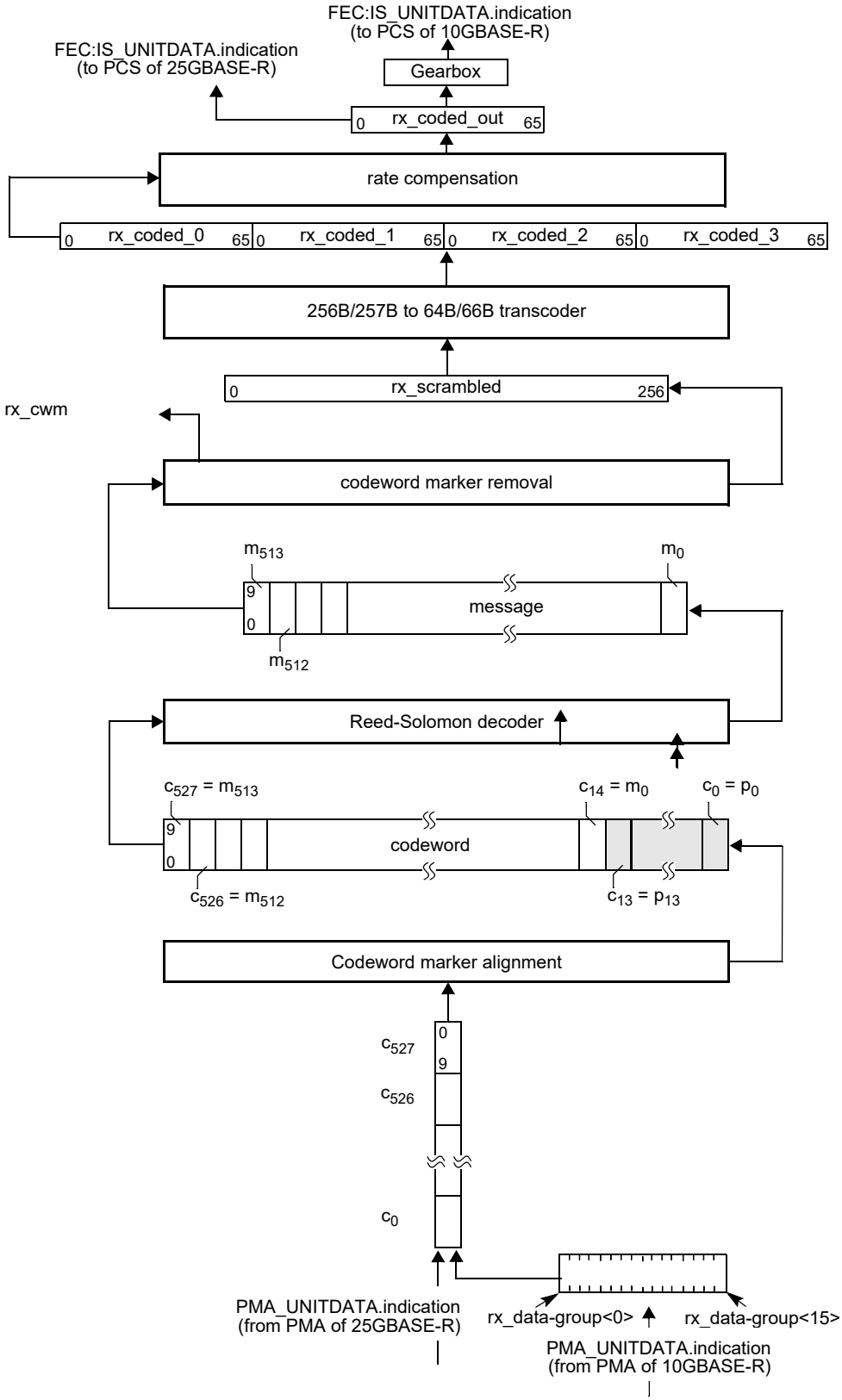

Figure 108–7—Receive bit ordering

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restart_lock
: Boolean variable that is set by the codeword monitor process to reset the synchronization process. It is set to true after 3 consecutive uncorrected codewords are received (3_BAD state) and set to false upon entry into the LOSS_OF_ALIGNMENT state.

signal_ok
: Boolean variable that is set based on the most recently received value of PMA:IS_SIGNAL.indication(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done
: Boolean variable that is set to true when the SLIP requested by the synchronization state diagram has been completed indicating that the next candidate 257-bit block position can be tested.

test_cwm
: Boolean variable that is set to true when a candidate block position is available for testing and is set to false according to the FEC synchronization state diagram in Figure 108–8.

test_cw
: Boolean variable that is set to true when a new FEC codeword is available for decoding and is set to false according to the codeword monitor state diagram in Figure 108–9.

The following variables are only used for the optional EEE deep sleep capability. If this capability is not supported, lpi_rapid_align, rx_lpi_active, and rcwm_counter_done are set to false, and rx_down_count is set to 0.

lpi_rapid_align
: Boolean variable that is set according to the FEC synchronization state diagram in Figure 108–8. Set to false when reset is true.

rx_lpi_active
: Boolean variable that is set to true when the rate compensation for codeword markers in the receive direction function (108.5.3.6) infers that the Low Power Idle is being received from the link partner, and is set to false otherwise.

rcwm_counter_done
: Boolean variable that indicates that rcwm_counter has reached its terminal count.

rx_down_count
: The countdown value of rapid codeword markers inferred by the receiver from rx_cwm. Transmitted rapid codeword markers contain four copies of tx_down_count and four copies of its bitwise-inverse, from which this value may be extracted.

108.5.4.3 Functions

SLIP
: Causes the next candidate block position to be tested. The precise method for determining the next candidate block position is not specified and is implementation dependent. However, an implementation shall ensure that all possible block positions are evaluated.

108.5.4.4 Counters

cwm_counter
: This counter counts the received codewords that separate the ends of two consecutive codeword markers. An RS-FEC codeword is 5280 bits. The terminal count of this counter is equal to the codeword offset between transmitted codeword markers, 1024.

cw_bad_count
: Counts the number of consecutive uncorrected codewords. This counter is set to zero when a codeword is received and cw_bad is false for that codeword.

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The following counters are only used for the optional EEE deep sleep capability:

tx_down_count
: A counter that is used when transmitting rapid codeword markers and is decremented each time a rapid codeword marker is sent. The counter initial value is set to 40 when the tx_mode parameter of the FEC:IS_TX_MODE.request primitive changes from ALERT to DATA. The terminal count is zero.

rcwm_counter
: This counter counts the received codewords that separate the ends of two consecutive rapid codeword markers. An RS-FEC codeword is 5280 bits. The terminal count of this counter is equal to one, which is the codeword offset between transmitted rapid codeword markers.

108.5.4.5 Timers

The following timer is only used for the optional EEE deep sleep capability.

hold_off_timer
: This timer is started when rx_mode (or rx_tx_mode if appropriate) transitions from QUIET to DATA. The timer terminal count is 11.5 μs. The timer is stopped when the terminal count is reached or when the FEC synchronization state diagram enters the 2_GOOD state. When the timer reaches the terminal count, it sets hold_off_timer_done = true.

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108.5.4.6 State diagrams

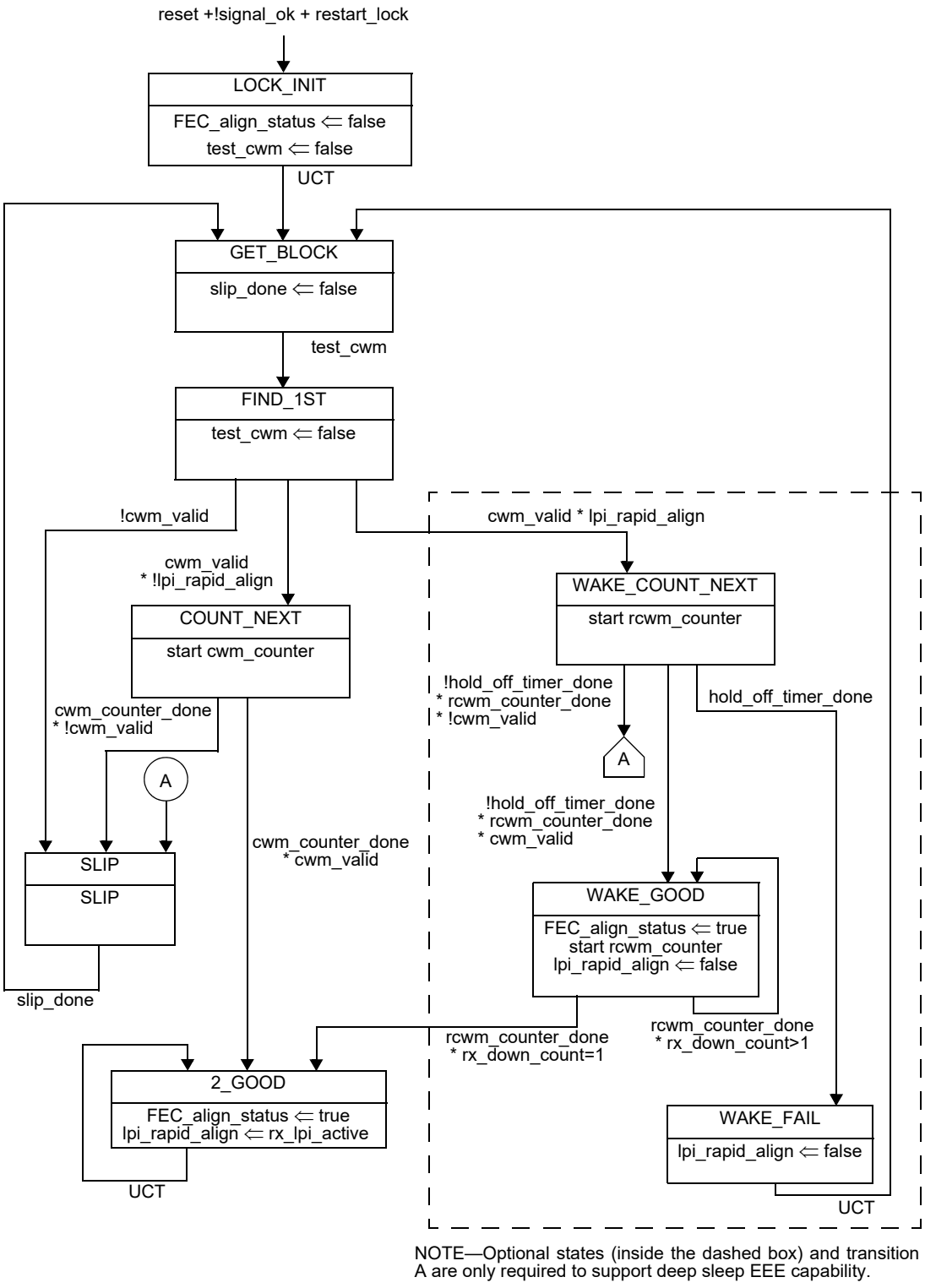

Figure 108–8—FEC synchronization state diagram

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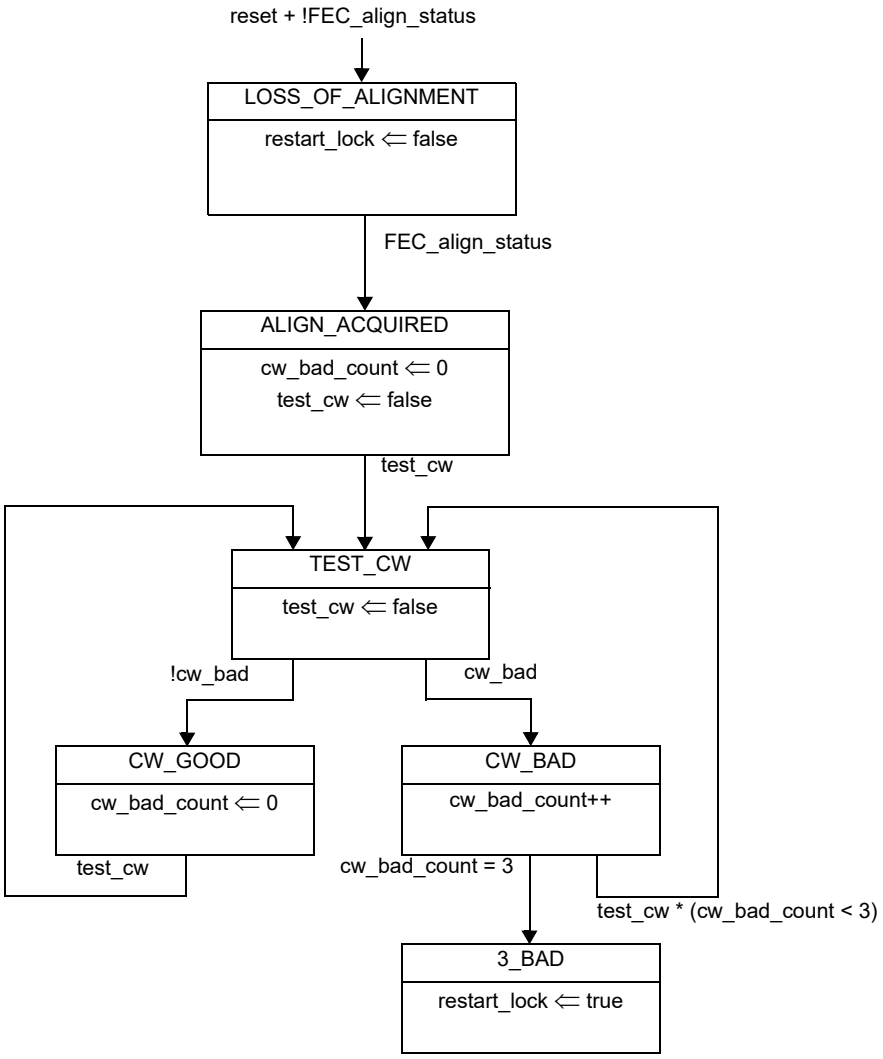

Figure 108–9—Codeword monitor state diagram

108.6 RS-FEC MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the RS-FEC. If MDIO is implemented, it shall map MDIO control bits to RS-FEC control variables as shown in Table 108–1 and MDIO status bits to RS-FEC status variables as shown in Table 108–2. If a separated PMA (see 45.2.1) is connected to the FEC service interface, the MDIO shall map additional MDIO status bits to additional RS-FEC status variables as shown in Table 108–3.

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Table 108–1—MDIO/RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass correction enable	RS-FEC control register	1.200.0	FEC_bypass_correction_enable
FEC bypass indication enable	RS-FEC control register	1.200.1	FEC_bypass_indication_enable
RS-FEC enable	RS-FEC control register	1.200.2	FEC_Enable

Table 108–2—MDIO/RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass correction ability	RS-FEC status register	1.201.0	FEC_bypass_correction_ability
FEC bypass indication ability	RS-FEC status register	1.201.1	FEC_bypass_indication_ability
RS-FEC high SER	RS-FEC status register	1.201.2	FEC_high_ser
RS-FEC align status	RS-FEC status register	1.201.14	FEC_align_status
RS-FEC corrected codewords counter	RS-FEC corrected codewords counter register	1.202, 1.203	FEC_corrected_cw_counter
RS-FEC uncorrected codewords counter	RS-FEC uncorrected codewords counter register	1.204, 1.205	FEC_uncorrected_cw_counter
RS-FEC symbol error counter, lane 0	RS-FEC symbol error counter lane 0 register	1.210, 1.211	FEC_symbol_error_counter_0

Table 108–3—MDIO/RS-FEC status variable mapping for separated PMA

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
PCS align status	RS-FEC status register	1.201.15	align_status

The following subclauses define variables that are not otherwise defined, e.g., for use by state diagrams.

108.6.1 FEC_bypass_correction_enable

When this variable is set to one, the Reed-Solomon decoder performs error detection without error correction (see 108.5.3.2). When this variable is set to zero, the decoder also performs error correction. The default value of the variable is zero. This variable is mapped to the bit defined in 45.2.1.116 (1.200.0).

108.6.2 FEC_bypass_indication_enable

This variable is set to one to bypass the error indication function (see 108.5.3.2) when this ability is supported. When this variable is set to zero, the decoder indicates errors to the PCS sublayer. This variable

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has no effect (the decoder does not bypass error indication) if FEC bypass correction enable (1.200.0) is set to one. The default value of this variable is zero. This variable is mapped to the bit defined in 45.2.1.116 (1.200.1).

108.6.3 RS-FEC Enable

The RS-FEC sublayer may have capability to enable or disable the FEC function for some PHY types. For those PHY types, an MDIO interface or an equivalent management interface shall be provided to access the variable FEC_Enable for the RS-FEC sublayer. When FEC_Enable variable is set to a one, the RS-FEC performs the transmit function as specified in 108.5.2 and the receive function as specified in 108.5.3. When the variable is set to zero, the RS-FEC transmit and receive functions are disabled, and the RS-FEC sublayer is bypassed, effectively connecting its service interface to the service interface of its underlying sublayer. Implementation of this bypass function should cause a minimal delay in the transmit and receive paths. This variable is mapped to the bit defined in 45.2.1.116.3 (1.200.2).

108.6.4 FEC_bypass_correction_ability

The Reed-Solomon decoder may have the option to perform error detection without error correction (see 108.5.3.2) to reduce the delay contributed by the RS-FEC sublayer. This variable is set to one if the decoder has the ability to bypass error correction. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.117 (1.201.0).

108.6.5 FEC_bypass_indication_ability

The Reed-Solomon decoder may have the option to bypass the error indication function (see 108.5.3.2) to reduce the delay contributed by the RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass error indication. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.117 (1.201.1).

108.6.6 FEC_high_ser

This variable is defined when the FEC_bypass_indication_ability variable is set to one. When FEC_bypass_indication_enable is set to one, this variable is set to one if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold 417 (see 108.5.3.2) and is set to zero otherwise. This variable is mapped to the bit defined in 45.2.1.117 (1.201.2).

108.6.7 FEC_corrected_cw_counter

A corrected FEC codeword is a codeword that contained errors that were corrected.

FEC_corrected_cw_counter is a 32-bit counter that counts once for each corrected FEC codeword processed when FEC_align_status is true. This variable is mapped to the registers defined in 45.2.1.118 (1.202, 1.203).

108.6.8 FEC_uncorrected_cw_counter

An uncorrected FEC codeword is a codeword that contains errors (when the bypass correction feature is supported and enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled).

FEC_uncorrected_cw_counter is a 32-bit counter that counts once for each uncorrected FEC codeword processed when FEC_align_status is true. This variable is mapped to the registers defined in 45.2.1.119 (1.204, 1.205).

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108.6.9 FEC_symbol_error_counter_0

FEC_symbol_error_counter_0, as defined in 91.6.19, is a 32-bit counter that counts once for each 10-bit symbol corrected in lane 0 when FEC_align_status is true. This variable is mapped to the registers defined in 45.2.1.121 (1.210, 1.211). For the RS-FEC defined in this clause, all symbols are assigned to lane 0 and all symbol errors are counted by this counter.

108.6.10 align_status

This variable is assigned the value of rx_block_lock as defined by the PCS lock state diagram (Figure 49–14) used in the block synchronization function (108.5.2.1). This variable is mapped to the bit defined in 45.2.1.117.1 (1.201.15).

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108.7 Protocol implementation conformance statement (PICS) proforma for Clause 108, Reed-Solomon forward error correction (RS-FEC) sublayer for 10GBASE-R and 25GBASE-R PHYs[181]

108.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 108, Reed-Solomon forward error correction (RS-FEC) sublayer for 10GBASE-R and 25GBASE-R PHYs, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

108.7.2 Identification

108.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

108.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 108, Reed-Solomon forward error correction (RS-FEC) sublayer for 10GBASE-R and 25GBASE-R PHYs
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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108.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*BR20	10GBASE-BR20		Used to form a complete 10GBASE-BR20 PHY	O	Yes [ ] No [ ]
*KR	25GBASE-KR		Used to form a complete 25GBASE-KR PHY	O	Yes [ ] No [ ]
*CR	25GBASE-CR		Used to form a complete 25GBASE-CR PHY	O	Yes [ ] No [ ]
*SR	25GBASE-SR		Used to form a complete 25GBASE-SR PHY	O	Yes [ ] No [ ]
*LR	25GBASE-LR		Used to form a complete 25GBASE-LR PHY	O	Yes [ ] No [ ]
*ER	25GBASE-ER		Used to form a complete 25GBASE-ER PHY	O	Yes [ ] No [ ]
DC	Delay constraints	108.4	Conforms to delay constraints specified	M	Yes [ ]
EF	RS-FEC enable	108.6.3	Has the capability to disable the RS-FEC function	(KR or CR):M	Yes [ ] N/A [ ]
*MD	MDIO capability	108.6	Registers and interface supported	O	Yes [ ] No [ ]
*BEC	Bypass error correction	108.5.3.2	Capability is supported	O	Yes [ ] No [ ]
*BEI	Bypass error indication	108.5.3.2	Capability is supported	O	Yes [ ] No [ ]
*AUI	25GAUI C2C	108.3	25GAUI C2C used to connect to a PCS	O	Yes [ ] No [ ]
*EEE	EEE deep sleep capability		Capability is supported	O	Yes [ ] No [ ]

108.7.4 PICS proforma tables for Reed-Solomon forward error correction (RS-FEC) sublayer for 10GBASE-R and 25GBASE-R PHYs

108.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Rate compensation for code-word markers	108.5.2.2	Performs the rate compensation function described	M	Yes [ ]
TF2	64B/66B to 256B/257B transcoder	108.5.2.3	tx_xcoded<256:0> constructed per 91.5.2.5	M	Yes [ ]
TF3	257-bit block transmission order	108.5.2.3	First bit transmitted is bit 0	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TF4	Codeword marker insertion	108.5.2.4	First 257 message bits to be transmitted from every 1024th codeword	M	Yes [ ]
TF5	Reed-Solomon encoder	108.5.2.5	As specified in 91.5.2.7	M	Yes [ ]
TF6	Codeword serialization	108.5.2.6	Transmit bit ordering as in Figure 108–5	M	Yes [ ]

108.7.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Codeword marker lock	108.5.3.1	Implemented as described	M	Yes [ ]
RF2	Reed-Solomon decoder	108.5.3.2	Capable of correcting any combination of up to 7 symbol errors in a codeword	M	Yes [ ]
RF3	Error correction not bypassed for 10GBASE-BR20, 25GBASE-SR, 25GBASE-LR, or 25GBASE-ER	108.5.3.2	Error correction is not bypassed	BEC*(SR or LR or ER or BR20):M	Yes [ ] N/A [ ]
RF4	Uncorrected error indication	108.5.3.2	Capable of indicating when a codeword contains errors that were not corrected	M	Yes [ ]
RF5	Error indication function	108.5.3.2	Corrupts 66-bit block synchronization headers as specified	M	Yes [ ]
RF6	Error indication when error correction is bypassed	108.5.3.2	Error indication is not bypassed when error correction is bypassed	BEC*BEI: M	Yes [ ] N/A [ ]
RF7	Error monitoring while error indication is bypassed	108.5.3.2	When the number of symbols errors in a block of 8192 codewords exceeds 417, corrupt 66-bit block synchronization headers for a period of 60 ms to 75 ms	BEI:M	Yes [ ] N/A [ ]
RF8	Error monitor while rx_lpi_active is true	108.5.3.2	Disabled	BEI*EEE: M	Yes [ ] N/A [ ]
RF9	Codeword monitor	108.5.3.3	Restarts the codeword marker lock when 3 consecutive uncor-rected codewords are detected	M	Yes [ ]
RF10	Alignment marker removal	108.5.3.4	rx_cwm removed prior to transcoding	M	Yes [ ]
RF11	256B/257B to 64B/66B transcoder	108.5.3.5	rx_coded_*j*<65:0>, *j*=0 to 3 constructed per 91.5.3.5 with cross-referencing to g<3:0> using Figure 49–7	M	Yes [ ]
RF12	Codeword marker bit rate compensation	108.5.3.6	Performs the rate compensation function described	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RF13	Codeword marker bit rate compensation	108.5.3.6	Content of blocks with invalid block type replaced by eight /E/ characters	M	Yes [ ]
RF14	Codeword marker bit rate compensation	108.5.3.6	Corrupted sync headers passed through and no idle characters inserted after them	M	Yes [ ]
RF15	Receive bit ordering	108.5.3.8	As illustrated in Figure 108–7	M	Yes [ ]

108.7.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	SLIP function	108.5.4.3	Ensure that all possible block positions are evaluated	M	Yes [ ]

108.7.4.4 MDIO function mapping

Item	Feature	Subclause	Value/Comment	Status	Support
MD1	MDIO control and status bit mapping	108.6	Mapped according to Table 108–1 and Table 108–2	MD:M	Yes [ ] N/A [ ]
MD2	Additional MDIO control and status bit mapping	108.6	Mapped according to Table 108–3	MD*AUI:M	Yes [ ] N/A [ ]

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109. Physical Medium Attachment (PMA) sublayer, type 25GBASE-R

109.1 Overview

109.1.1 Scope

This clause specifies the Physical Medium Attachment sublayer (PMA) that is common to a family of 25 Gb/s Physical Layer implementations, known as 25GBASE-R. The PMA allows the PCS (specified in Clause 107) to connect in a media-independent way with a range of physical media. 25GBASE-R can be extended to support any full duplex medium requiring only that the PMD be compliant with the PMA interface.

The PMA service interface is defined in an abstract manner and does not imply any particular implementation. Electrical interfaces connecting PMA sublayers, known as 25GAUI, are defined in Annex 109A and Annex 109B.

109.1.2 Position of the PMA in the 25GBASE-R sublayers

Figure 109–1 shows the relationship of the PMA sublayer (shown shaded) with other sublayers to the ISO Open System Interconnection (OSI) reference model.

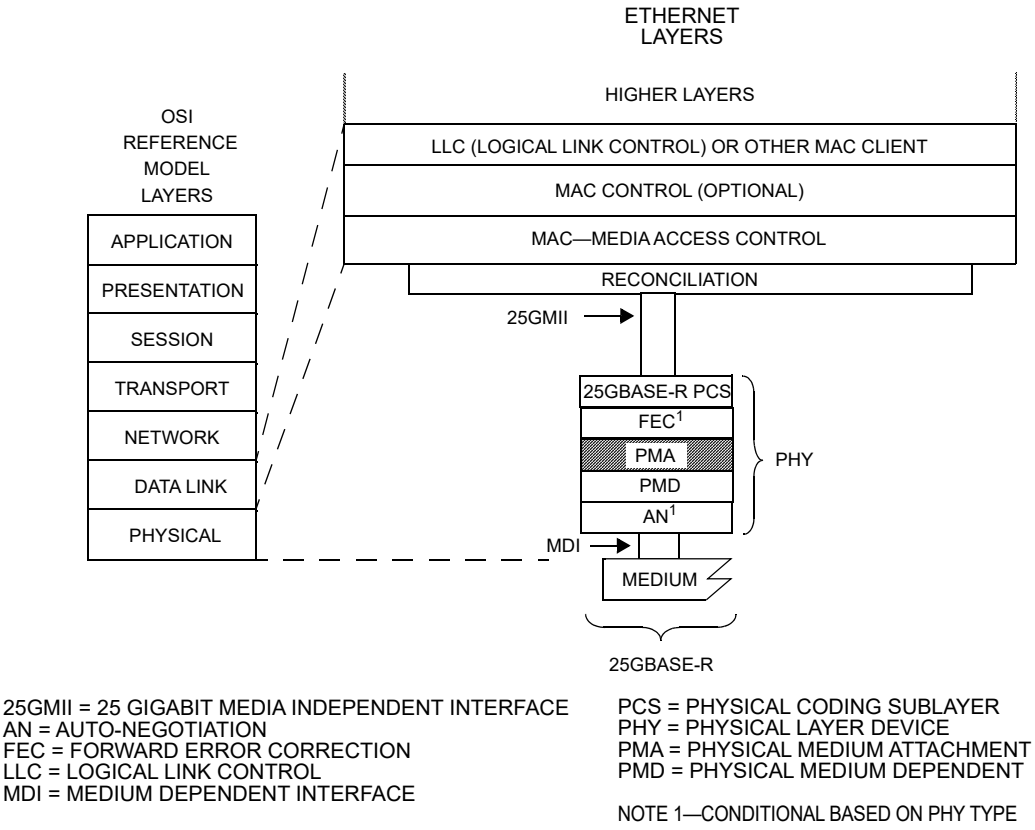

Figure 109–1—25GBASE-R PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

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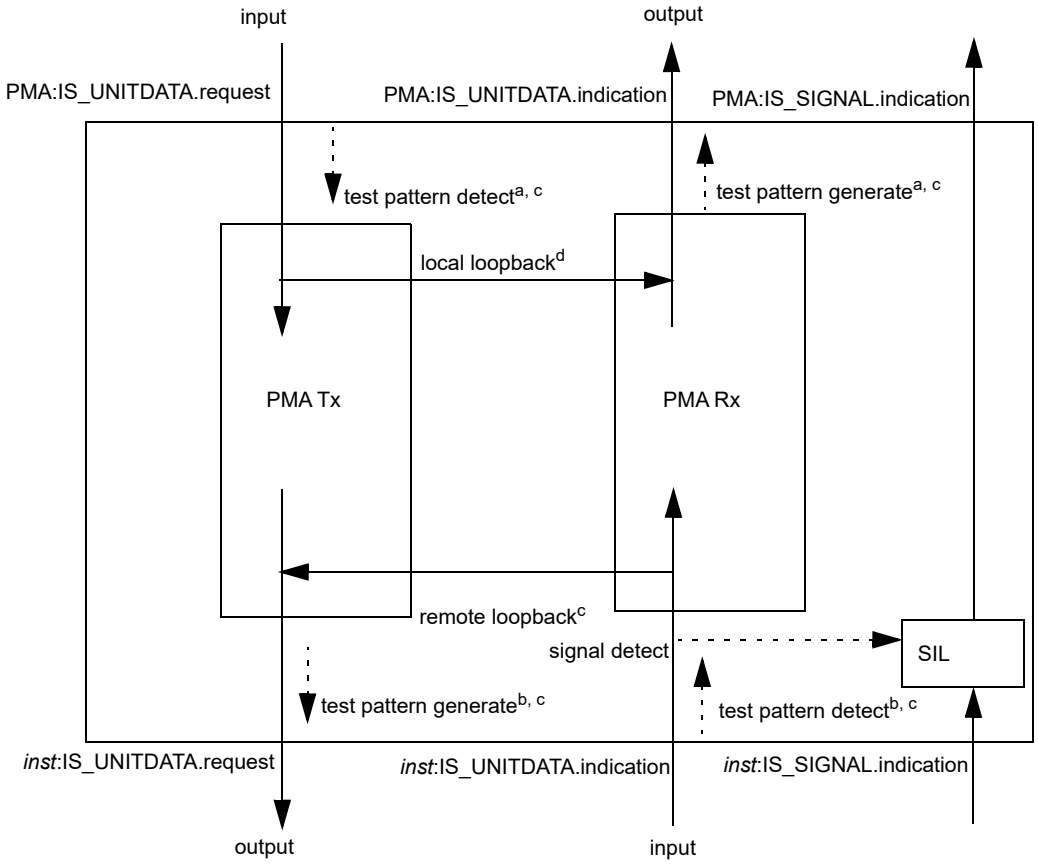
109.1.3 Summary of functions

The following is a summary of the principal functions implemented (when required) by the PMA in both the transmit and receive directions:

a) Provide clock and data recovery.
b) Provide signal drivers.
c) Optionally provide local loopback to/from the PMA service interface.
d) Optionally provide remote loopback to/from the PMD service interface.
e) Optionally provide test-pattern generation and detection.

The functional block diagram in Figure 109–2 shows the inputs, outputs, test-pattern checking and generation, loopbacks, and Signal Indication Logic (SIL, see 109.2).



inst = PMD, PMA, or FEC, depending on which sublayer is below this PMA
SIL = Signal Indication Logic

[a] If 25GAUI immediately above this PMA.
[b] If 25GAUI or PMD service interface immediately below this PMA.
[c] Optional.
[d] Conditional (see 109.4.2)

Figure 109–2—PMA Functional Block Diagram

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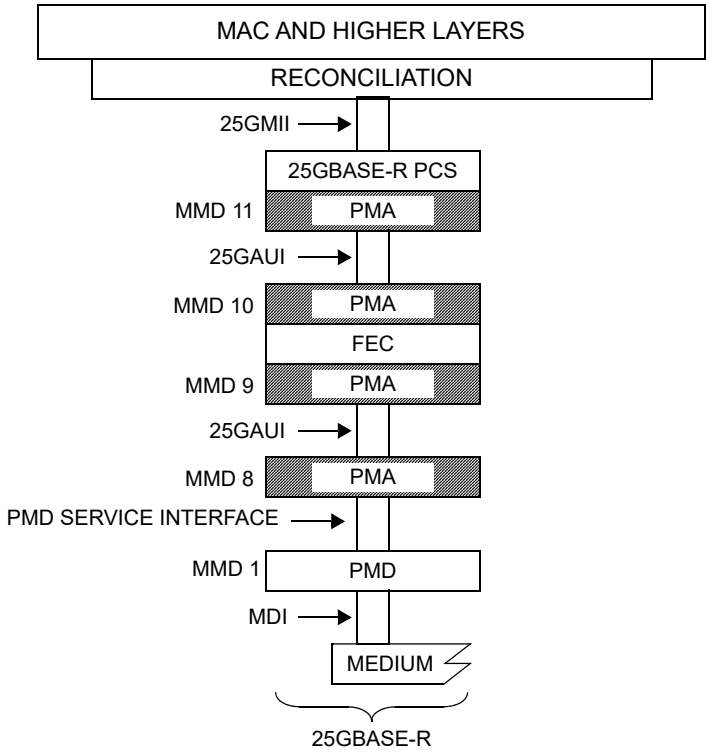
109.1.4 PMA sublayer positioning

An implementation may use one or more PMA sublayers to provide an interface with a physical electrical interface, 25GAUI, between devices. The number of PMA sublayers required depends on the partitioning of functionality for a particular implementation. An example is illustrated in Figure 109–3. This example illustrates the partitioning that might arise from implementing an FEC sublayer in a device that is separate from the PCS. Additional examples are illustrated in Annex 109C.



25GAUI = 25 GIGABIT ATTACHMENT UNIT INTERFACE
25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 109–3—Example 25GBASE-R PMA layering

Management Data Input/Output (MDIO) Manageable Device (MMD) addresses 1, 8, 9, 10, and 11 are available for addressing multiple instances of PMA sublayers (see Table 45–1 for MMD device addresses). If the PMA sublayer that is closest to the PMD is packaged with the PMD, it shares MMD 1 with the PMD. More addressable instances of PMA sublayers, each one separated from lower addressable instances by chip-to-chip interfaces, may be implemented and addressed allocating MMD addresses to PMAs in increasing numerical order going from the PMD toward the PCS. The example shown in Figure 109–3 could be implemented with four addressable instances: MMD 8 addressing the lowest PMA sublayer (note that this cannot share MMD 1 with the PMD as they are not packaged together in this example), MMD 9 addressing the PMA sublayer above the 25GAUI below the FEC, MMD 10 addressing the PMA sublayer below the 25GAUI above the FEC, and MMD 11 addressing the PMA sublayer closest to the PCS.

The following guidelines apply to the partitioning of PMAs:

a) The inter-sublayer service interface, defined in 105.4, is used for the PMA, FEC, and PMD service interfaces supporting a flexible architecture with optional FEC and multiple PMA sublayers.

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b) 25GAUI is a 25.78125 GBd serial physical instantiation of the connection between two adjacent PMA sublayers. As a physical instantiation, it defines electrical and timing specification as well as requiring a receive re-timing function.

c) Opportunities for optional test-pattern generation, optional test-pattern detection, optional local loopback and optional remote loopback are dependent upon the location of the PMA sublayer in the implementation. See Figure 109–2.

d) A minimum of one PMA sublayer is required in a PHY.

e) A maximum of four PMA sublayers are addressable as MDIO MMDs.

109.2 PMA service interface

This subclause specifies the services provided by the 25GBASE-R PMA. The service interface for this PMA is described in an abstract manner and does not imply any particular implementation. The PMA service interface supports the exchange of encoded data. The PMA translates the encoded data to and from signals suitable for the medium.

The PMA service interface is an instance of the inter-sublayer service interface defined in 105.4. The PMA service interface primitives are summarized as follows:

PMA:IS_UNITDATA.request
PMA:IS_UNITDATA.indication
PMA:IS_SIGNAL.indication

The PMA continuously sends a bit stream to the PMA client (e.g., PCS) at a nominal signaling rate of 25.78125 GBd. Likewise the PMA client continuously sends a bit stream to the PMA.

In the Tx direction, if data from a PMA:IS_UNITDATA.request primitive is received over a 25GAUI, clock and data are recovered on the lane to recover data one bit at a time. Each recovered bit is sent to the sublayer below using the *inst*:IS_UNITDATA.request primitive.

In the Rx direction, when data is received from the sublayer below the PMA using the *inst*:IS_UNITDATA.request primitive, each received bit is sent to the PMA client using the PMA:IS_UNITDATA.indication primitive.

PMA:IS_SIGNAL.indication(SIGNAL_OK) is generated based on receipt of *inst*:IS_SIGNAL.indication(SIGNAL_OK) from the sublayer below and status of the input signal as determined by the signal detect function (see Figure 109–2). When *inst*:IS_SIGNAL.indication(SIGNAL_OK) has the value FAIL or the signal detect function detects an invalid signal, PMA:IS_SIGNAL.indication(SIGNAL_OK) shall have the value FAIL, otherwise PMA:IS_SIGNAL.indication(SIGNAL_OK) shall have the value OK. The operation of the signal detect function is beyond the scope of this standard.

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78, 78.1.3.3.1) then the inter-sublayer service interface includes four additional primitives defined as follows:

PMA:IS_TX_MODE.request
PMA:IS_RX_MODE.request
PMA:IS_ENERGY_DETECT.indication
PMA:IS_RX_TX_MODE.indication

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A physically instantiated service interface with the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option (see 78.1.3.3.1) may enter a low power state to conserve energy during periods of low link utilization. The ability to support transition to a low power state in the ingress direction is indicated by register 1.1.9 (PMA Ingress AUI Stop Ability, PIASA). The ability to support transition to a low power state in the egress direction is indicated by register 1.1.8 (PMA Egress AUI Stop Ability, PEASA). Transition to the low power state in the ingress direction is enabled by register 1.7.9 (PMA Ingress AUI Stop Enable, PIASE). Transition to the low power state in the egress direction is enabled by register 1.7.8 (PMA Egress AUI Stop Enable, PEASE). The system shall not assert the enable bit for an interface unless the corresponding ability bit at the other side of the interface is also asserted. If the PIASE bit is TRUE, then the PMA may disable transmitters on the physical instantiation of the ingress AUI when aui_tx_mode is QUIET. If the PEASE bit is TRUE, then the PMA may disable transmitters on the physical instantiation of the egress AUI when tx_mode is QUIET.

109.3 Service interface below PMA

Since the architecture supports multiple PMA sublayers, there are several different sublayers that may appear below a PMA, including FEC, the PMD, or another PMA. The variable *inst* represents whichever sublayer appears below the PMA.

The sublayer below the PMA utilizes the inter-sublayer service interface defined in 105.4. The service interface primitives provided to the PMA are summarized as follows:

inst:IS_UNITDATA.request(tx_bit)
inst:IS_UNITDATA.indication(rx_bit)
inst:IS_SIGNAL.indication(SIGNAL_OK)

Note that electrical and timing specifications of the service interface are defined if the interface is physically instantiated (e.g., 25GAUI), otherwise the service interface is specified abstractly. The service interface below the PMA has an input and output for data transfer and a status input indicating a good signal sent by the sublayer below the PMA (see Figure 109–2).

In the Tx direction, data received via the PMA:IS_UNITDATA.request primitive from the PMA client at the PMA service interface is sent to the sublayer below the PMA via the *inst*:IS_UNITDATA.indication primitive.

In the Rx direction, if the bit is received over a physically instantiated interface (e.g., 25GAUI), clock and data are recovered on the lane receiving the bit. The bit is routed through the PMA to an output lane toward the PMA client, sending the bit to the PMA client using the PMA:IS_UNITDATA.indication primitive at the PMA service interface.

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78, 78.1.3.3.1) then inter-sublayer service interface for the sublayer below the PMA includes four additional primitives defined as follows:

inst:IS_TX_MODE.request
inst:IS_RX_MODE.request
inst:IS_ENERGY_DETECT.indication
inst:IS_RX_TX_MODE.indication

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109.4 Functions within the PMA

109.4.1 Signal drivers

For cases where the interface between the PMA client and the PMA, or between the PMA and the sublayer below the PMA represent a physically instantiated interface, the PMA provides electrical signal drivers for that interface.

The electrical and jitter/timing interface requirements for the 25GAUI chip-to-chip (C2C) are specified in Annex 109A.

The electrical and jitter/timing interface requirements for the 25GAUI chip-to-module (C2M) are specified in Annex 109B.

109.4.2 PMA local loopback mode

PMA local loopback shall be provided by the PMA adjacent to the PMD for 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, and 25GBASE-KR-S. PMA local loopback mode is optional for other PMDs or for PMAs not adjacent to the PMD. If it is implemented, it shall be as described in this subclause.

The PMA local loopback function involves looping back the input to the output. Each bit received from the PMA:IS_UNITDATA.request(tx_bit) primitive is looped back in the direction of the PCS using the PMA:IS_UNITDATA.indication(rx_bit) primitive.

Ability to perform the local loopback function is indicated by the Local_loopback_ability status variable. A device is placed in local loopback mode when the Local_loopback_enable control variable is set to one, and removed from local loopback mode when this variable is set to zero.

If the optional Clause 45 MDIO is implemented, the PMA receive process maps the Local_loopback_ability and Local_loopback_enable variables to the registers and bits defined in 109.6.

109.4.3 PMA remote loopback mode

PMA remote loopback mode is optional. If implemented, it shall be as described in this subclause.

When remote loopback is enabled, each bit from the service interface below the PMA via *inst*:IS_UNITDATA.indication is looped back toward the PMD via *inst*:IS_UNITDATA.request. Note that the service interface below the PMA can be provided by the FEC or PMD.

The ability to perform this function is indicated by the Remote_loopback_ability status variable. A device is placed in remote loopback mode when the Remote_loopback_enable control variable is set to one, and removed from remote loopback mode when this variable is set to zero.

If the optional Clause 45 MDIO is implemented, the PMA receive process maps the Remote_loopback_ability and Remote_loopback_enable variables to the registers and bits defined in 109.6.

109.4.4 PMA test patterns

Where the output of the PMA appears on a physically instantiated interface 25GAUI or the PMD service interface, the PMA may optionally generate and detect test patterns. These test patterns are used to test adjacent layer interfaces for an individual PMA sublayer or to perform testing between a physically instantiated interface of a PMA sublayer and external testing equipment.

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109.4.4.1 Transmit PRBS31 test-pattern generation

The ability to generate PRBS31 test patterns in the transmit direction is indicated by the PRBS31_Tx_generator_ability status variable. If supported, transmit PRBS31 test-pattern generation is enabled by the PRBS31_enable and PRBS_Tx_gen_enable control variables. When transmit PRBS31 test-pattern generation is enabled, the PMA shall generate a PRBS31 pattern as defined in 49.2.8 toward the service interface below the PMA via the *inst*:IS_UNITDATA.request primitive.

If the optional Clause 45 MDIO is implemented, the PMA transmit process maps the PRBS31_Tx_checker_ability, PRBS31_Rx_checker_ability, PRBS31_enable, and PRBS_Tx_gen_enable variables to the registers and bits defined in 109.6.

To avoid correlated crosstalk between this link and other locally implemented links, it is highly recommended that the PRBS31 patterns generated on each link use independent, random seeds or ensure a minimum offset of 20 000 UI between the PRBS31 sequence on any two links.

109.4.4.2 Receive PRBS31 test-pattern generation

The ability to generate PRBS31 test patterns in the receive direction is indicated by the PRBS31_Rx_generator_ability status variable. If supported, receive PRBS31 test-pattern generation is enabled by the PRBS31_enable and PRBS_Rx_gen_enable control variables. When receive PRBS31 test-pattern generation is enabled, the PMA shall generate a PRBS31 pattern as defined in 49.2.8 toward the PMA client via the PMA:IS_UNITDATA.indication primitive. While this test pattern is enabled, the PMA also generates PMA:IS_SIGNAL.indication(SIGNAL_OK) indicating a valid signal (SIGNAL_OK=OK) toward the PMA client independent of the status at the service interface below the PMA. When receive PRBS31 test-pattern generation is disabled, the PMA returns to normal operation.

If the optional Clause 45 MDIO is implemented, the PMA receive process maps the PRBS31_Rx_generator_ability, PRBS31_enable, and PRBS_Rx_gen_enable variables to the registers and bits defined in 109.6.

To avoid correlated crosstalk between this link and other locally implemented links, it is highly recommended that the PRBS31 patterns generated on each link use independent, random seeds or ensure a minimum offset of 20 000 UI between the PRBS31 sequence on any two links.

109.4.4.3 Transmit PRBS31 test-pattern checking

The ability to check PRBS31 test patterns in the transmit direction is indicated by the PRBS31_Tx_checker_ability status variable. If supported, the transmit PRBS31 test-pattern checking is enabled by the PRBS31_enable and PRBS_Tx_check_enable control variables. When transmit PRBS31 test-pattern checking is enabled, the PMA shall check for the PRBS31 pattern received from the PMA client via the PMA:IS_UNITDATA.request primitive. The checker shall increment the test-pattern error counter by one for each incoming bit error in the PRBS31 pattern for isolated single-bit errors. Implementations should be capable of counting at least one error whenever one or more errors occur in a sliding 1000-bit window. The transmit test-pattern error count is indicated by the Ln0_PRBS_Tx_test_err_counter status variable. When transmit PRBS31 test-pattern checking is disabled, the PMA returns to normal operation.

If the optional Clause 45 MDIO is implemented, the PMA transmit process maps the PRBS31_Tx_checker_ability, PRBS31_enable, PRBS_Tx_check_enable, and Ln0_PRBS_Tx_test_err_counter variables to the registers and bits defined in 109.6.

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109.4.4.4 Receive PRBS31 test-pattern checking

The ability to check PRBS31 test patterns in the receive direction is indicated by the PRBS31_Rx_checker_ability status variable. If supported, receive PRBS31 test-pattern checking is enabled by the PRBS31_enable and PRBS_Rx_check_enable control variables. When receive PRBS31 test-pattern checking is enabled, the PMA shall check for the PRBS31 pattern received from the service interface below the PMA via the *inst*:IS_UNITDATA.indication primitive. The receive test-pattern error count is indicated by the Ln0_PRBS_Rx_test_err_counter status variable. While the receive PRBS31 test-pattern mode is enabled, the PMA:IS_SIGNAL.indication(SIGNAL_OK) primitive does not indicate a valid signal (SIGNAL_OK=FAIL). When receive PRBS31 test-pattern checking is disabled, the PMA returns to normal operation.

If the optional Clause 45 MDIO is implemented, the PMA receive process maps the PRBS31_Rx_checker_ability, PRBS31_enable, PRBS_Rx_check_enable, and Ln0_PRBS_Rx_test_err_counter variables to the registers and bits defined in 109.6.

109.4.4.5 Transmit PRBS9 test-pattern generation

The ability to generate the PRBS9 test patterns in the transmit direction is indicated by the PRBS9_Tx_generator_ability status variable. If supported, transmit PRBS9 test-pattern generation is enabled by the PRBS9_enable and PRBS_Tx_gen_enable control variables. When transmit PRBS9 pattern generation is enabled, the PMA shall generate a PRBS9 pattern as defined in Table 68–6 toward the service interface below the PMA via the *inst*:IS_UNITDATA.request primitive. When transmit PRBS9 test-pattern generation is disabled, the PMA returns to normal operation.

If the optional Clause 45 MDIO is implemented, the PMA transmit process maps the PRBS9_Tx_generator_ability, PRBS9_enable, and PRBS_Tx_gen_enable variables to the registers and bits defined in 109.6.

Note that the transmit PRBS9 test pattern is intended to be checked by external test gear and no PRBS9 checking function is provided within the PMA.

109.4.4.6 Receive PRBS9 test-pattern generation

The ability to generate the PRBS9 test patterns in the receive direction is indicated by the PRBS9_Rx_generator_ability status variable. If supported, receive PRBS9 test-pattern generation is enabled by the PRBS9_enable and PRBS_Rx_gen_enable control variables. When receive PRBS9 test-pattern generation is enabled, the PMA shall generate a PRBS9 pattern as defined in Table 68–6 toward the PMA client via the PMA:IS_UNITDATA.indication primitive. The PMA will also generate PMA:IS_SIGNAL.indication(SIGNAL_OK) toward the PMA client independent of the status at the service interface below the PMA. When receive PRBS9 test-pattern generation is disabled, the PMA returns to normal operation.

If the optional Clause 45 MDIO is implemented, the PMA receive process maps the PRBS9_Rx_generator_ability, PRBS9_enable and PRBS_Rx_gen_enable variables to the registers and bits defined in 109.6.

Note that the receive PRBS9 test pattern is intended to be checked by external test gear and no PRBS9 checking function is provided within the PMA.

109.4.4.7 Transmit square wave test-pattern generation

The optional transmit square wave test-pattern generation applies to the PMA transmit direction towards a physically instantiated 25GAUI or towards the PMD service interface.

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The ability to generate the square wave test pattern in the transmit direction is indicated by the Square_wave_ability status variable. If supported, transmit square wave test-pattern generation is enabled by the Square_wave_enable_0 control variable. When transmit square wave test-pattern generation is enabled, the PMA shall generate a square wave test pattern composed of 8 ones followed by 8 zeros toward the service interface below the PMA via the *inst*:IS_UNITDATA.request primitive. When transmit square wave test-pattern generation is disabled, the PMA returns to normal operation.

If the optional Clause 45 MDIO is implemented, the PMA transmit process maps the Square_wave_ability and Square_wave_enable_0 variable to the registers and bits defined in 109.6.

109.4.5 Energy Efficient Ethernet for 25GAUI

When the optional Energy Efficient Ethernet (EEE) deep sleep capability is supported and the PMA service interface is physically instantiated as 25GAUI, the additional functions listed in 83.5.11 are required. These functions enable the communication of service interface parameters that are essential to the operation of the EEE deep sleep capability. The timing parameters for EEE operation are shown in Table 83–2.

PMA EEE operation for 25GAUI is specified in 83.5.11 with respect to lane 0 only. Considerations related to multiple lanes do not apply.

109.5 Delay constraints

The maximum cumulative delay contributed by up to four PMA stages in a PHY (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 109–1. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 105.5.

Table 109–1—Delay constraints

Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
4096	8	163.84

109.6 PMA MDIO function mapping

The optional MDIO capability described in Clause 45 describes several variables that provide control and status information for and about the PMA. Since a given implementation may employ more than one PMA sublayer, the PMA control and status information is organized into multiple addressable instances, one for each possible PMA sublayer. See 45.2.1 and 109.1.4 for the allocation of MMD addresses to PMA sublayers. Control and status registers for MMD 8, 9, 10, and 11 will use the Extended PMA control and status registers at identical locations to those for MMD 1.

Mapping of MDIO control variables to PMA control variables is shown in Table 109–2. Mapping of MDIO status variables to PMA status variables is shown in Table 109–3. Mapping of MDIO counter to PMA counters is shown in Table 109–4. These tables provide the register and bit numbers for the PMA addressed as MMD 1. For implementations with multiple PMA sublayers, additional PMA sublayers use the corresponding register and bit numbers in MMDs 8, 9, 10, and 11 as necessary.

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Table 109–2—MDIO/PMA control variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
PMA remote loopback	PMA/PMD control 1	1.0.1	Remote_loopback_enable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
PRBS31 pattern enable	PRBS pattern testing control	1.1501.7	PRBS31_enable
PRBS9 pattern enable	PRBS pattern testing control	1.1501.6	PRBS9_enable
Tx generator enable	PRBS pattern testing control	1.1501.3	PRBS_Tx_gen_enable
Tx checker enable	PRBS pattern testing control	1.1501.2	PRBS_Tx_check_enable
Rx generator enable	PRBS pattern testing control	1.1501.1	PRBS_Rx_gen_enable
Rx checker enable	PRBS pattern testing control	1.1501.0	PRBS_Rx_check_enable
Lane 0 SW enable	Square wave testing control	1.1510.0	Square_wave_enable_0
PIASE	PMA/PMD control 2	1.7.9	PIASE
PEASE	PMA/PMD control 2	1.7.8	PEASE

Table 109–3—MDIO/PMA status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMA status variable
PMA remote loopback ability	40G/100G PMA/PMD extended ability	1.13.15	Remote_loopback_ability
PMA local loopback ability	PMA/PMD status 2	1.8.0	Local_loopback_ability
PRBS9 Tx generator ability	Test-pattern ability	1.1500.5	PRBS9_Tx_generator_ability
PRBS9 Rx generator ability	Test-pattern ability	1.1500.4	PRBS9_Rx_generator_ability
PRBS31 Tx generator ability	Test-pattern ability	1.1500.3	PRBS31_Tx_generator_ability
PRBS31 Tx checker ability	Test-pattern ability	1.1500.2	PRBS31_Tx_checker_ability
PRBS31 Rx generator ability	Test-pattern ability	1.1500.1	PRBS31_Rx_generator_ability
PRBS31 Rx checker ability	Test-pattern ability	1.1500.0	PRBS31_Rx_checker_ability
Square wave test ability	Test-pattern ability	1.1500.12	Square_wave_ability
PIASA	PMA/PMD status 1	1.1.9	PIASA
PEASA	PMA/PMD status 1	1.1.8	PEASA

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Table 109–4—MDIO/PMA counters mapping

MDIO variable	PMA/PMD register name	Register/bit number	PMA status variable
Error counter Tx, lane 0	PRBS Tx pattern testing error counter, lane 0	1.1600	Ln0_PRBS_Tx_test_err_counter
Error counter Rx, lane 0	PRBS Rx pattern testing error counter, lane 0	1.1700	Ln0_PRBS_Rx_test_err_counter

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109.7 Protocol implementation conformance statement (PICS) proforma for Clause 109, Physical Medium Attachment (PMA) sublayer, type 25GBASE-R[182]

109.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 109, Physical Medium Attachment (PMA) sublayer, type 25GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

109.7.2 Identification

109.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

109.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 109, Physical Medium Attachment (PMA) sublayer, type 25GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[182]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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109.7.3 PICS proforma tables for the 25GBASE-R PMA Sublayer

109.7.4 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
MD	MDIO	109.6	Registers and interface supported	O	Yes [ ] No [ ]
*PIA	Physically instantiated 25GAUI above (toward PCS)	109.4.1		O	Yes [ ] No [ ]
*PIB	Physically instantiated 25GAUI below (toward PMD)	109.4.1		O	Yes [ ] No [ ]
*PMB	PMD below	109.3		O	Yes [ ] No [ ]
*LPI	Implementation of LPI with the deep sleep mode option	109.4.5		O	Yes [ ] No [ ]
*KRCR	PMA adjacent to the PMD for 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, or 25GBASE-CR-S.	109.4.2		O	Yes [ ] No [ ]
*LBL	Supports PMA local loopback	109.4.2		KRCR:M !KRCR:O	Yes [ ] No [ ] N/A [ ]
*LBR	Supports PMA remote loopback	109.4.3		O	Yes [ ] No [ ] N/A [ ]

109.7.4.1 PMA functions

Item	Feature	Subclause	Value/Comment	Status	Support
PF1	PMA local loopback	109.4.2	Meets the requirements of 109.4.2.	LBL:M	Yes [ ] No [ ]
PF2	PMA remote loopback	109.4.3	Meets the requirements of 109.4.3.	LBR:M	Yes [ ] No [ ]
PF3	Transmit PRBS31 generation	109.4.4.1	Meets the requirements of 109.4.4.1.	PMB:O	Yes [ ] No [ ]
PF4	Receive PRBS31 generation	109.4.4.2	Meets the requirements of 109.4.4.2.	PIA:O	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PF5	Transmit PRBS31 checking	109.4.4.3	Meets the requirements of 109.4.4.3.	PIA:O	Yes [ ] No [ ]
PF6	Receive PRBS31 checking	109.4.4.4	Meets the requirements of 109.4.4.4.	PMB:O	Yes [ ] No [ ]
PF7	Transmit PRBS9 generation	109.4.4.5	Meets the requirements of 109.4.4.5.	PMB:O	Yes [ ] No [ ]
PF8	Receiver PRBS9 generation	109.4.4.6	Meets the requirements of 109.4.4.6.	PIA:O	Yes [ ] No [ ]
PF9	Transmit square wave generation	109.4.4.7	Meets the requirements of 109.4.4.7.	PMB:O	Yes [ ] No [ ]

109.7.4.2 PMA characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
PC1	Cumulative round-trip delay contributed by up to four PMA stages in a PHY.	109.5	No more than 4096 BT or 8 pause quanta	M	Yes [ ] No [ ]
PC2	Electrical and timing requirements of Annex 109A or Annex 109B as appropriate met by upstream 25GAUI	109.4.1		PIA:M	Yes [ ] No [ ]
PC3	Electrical and timing requirements of Annex 109A or Annex 109B as appropriate met by downstream 25GAUI	109.4.1		PIB:M	Yes [ ] No [ ]
PC4	25GAUI deep sleep Rx direction	109.4.5	Meets the requirements of 109.4.5.	LPI*PIA:M LPI*PIB:M	Yes [ ] No [ ]
PC5	25GAUI deep sleep Tx direction	109.4.5	Meets the requirements of 109.4.5.	LPI*PIA:M LPI*PIB:M	Yes [ ] No [ ]

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110. Physical Medium Dependent (PMD) sublayer and baseband medium, type 25GBASE-CR and 25GBASE-CR-S

110.1 Overview

This clause specifies the 25GBASE-CR PMD, the 25GBASE-CR-S PMD, and the baseband medium. The specifications are closely related to those of 100GBASE-CR4 (Clause 92), but with a single lane instead of four lanes. There are three associated annexes. Annex 110A provides information on parameters with test points that may not be testable in an implemented system, Annex 110B specifies test fixtures, and Annex 110C describes 25GBASE-CR and 25GBASE-CR-S host and cable assembly form factors.

When forming a complete Physical Layer, the PMD shall be connected as illustrated in Figure 110–1, to the appropriate PMA as shown in Table 110–1, to the medium through the MDI, and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 110–1—Physical Layer clauses associated with the 25GBASE-CR and 25GBASE-CR-S PMDs

Associated clause	25GBASE-CR	25GBASE-CR-S
106—RS	Required	Required
106—25GMII[a]	Optional	Optional
107—PCS	Required	Required
74—BASE-R FEC[b]	Required	Required
108—RS-FEC[b]	Required	N/A
109—PMA	Required	Required
109A—25GAUI C2C	Optional	Optional
73—Auto-Negotiation	Required	Required
78—Energy Efficient Ethernet	Optional	Optional

[a]The 25GMII is an optional interface. However, if the 25GMII is not implemented, a conforming implementation behaves functionally as though the RS and 25GMII were present.
[b]FEC sublayers can be enabled or disabled according to the FEC mode (see 110.6).

A 25GBASE-CR PHY operates over cable assemblies of types CA-25G-N, CA-25G-S and CA-25G-L (see 110.10). A 25GBASE-CR-S PHY operates over cable assemblies of types CA-25G-N and CA-25G-S. A 25GBASE-CR-S PHY interoperates with a 25GBASE-CR PHY. Table 110–2 summarizes the cable assembly types supported by each of the PHY types.

Table 110–2—Cable assembly types supported by each PHY type

PHY type	CA-25G-N	CA-25G-S	CA-25G-L
25GBASE-CR	Yes	Yes	Yes
25GBASE-CR-S	Yes	Yes	No

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When forming a complete 25GBASE-CR or 25GBASE-CR-S Physical Layer, the link BER requirements depend on the FEC mode (see 110.6) according to the following guidelines:

a) If a PHY operates in the RS-FEC mode, and the RS-FEC decoder does not bypass error correction (see 108.5.3.2), the link is required to operate with a BER of 10^{-5} or better.
b) If a PHY operates in the BASE-R FEC mode, the link is required to operate with a BER of 10^{-8} or better.
c) If a PHY operates in the no-FEC mode, or in the RS-FEC mode with error correction bypassed, the link is required to operate with a BER of 10^{-12} or better.

In this context, a link consists of a compliant PMD transmitter, a compliant PMD receiver, and a compliant cable assembly.

For a complete Physical Layer, this specification is considered to be satisfied by a frame loss ratio (see 1.4.344) less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap.

25GBASE-CR and 25GBASE-CR-S PHYs with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization.

Figure 110–1 shows the relationship of the 25GBASE-CR and 25GBASE-CR-S PMD sublayers and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.

110.2 PMD service interface

This subclause specifies the services provided by the 25GBASE-CR and 25GBASE-CR-S PMDs. The service interface for these PMDs is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data. The PMD translates the encoded data to and from signals suitable for the medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 105.4. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA.request
PMD:IS_UNITDATA.indication
PMD:IS_SIGNAL.indication

The PMA (or the PMD) continuously sends a bit stream to the PMD (or the PMA) at a nominal signaling rate of 25.78125 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable Global_PMD_signal_detect as defined in 110.7.4. When Global_PMD_signal_detect is one, SIGNAL_OK shall be assigned the value OK. When Global_PMD_signal_detect is zero, SIGNAL_OK shall be assigned the value FAIL. When SIGNAL_OK is FAIL, the PMD:IS_UNITDATA.indication parameter is undefined.

If the optional EEE deep sleep capability is supported, then the PMD service interface includes two additional primitives as follows:

PMD:IS_TX_MODE.request
PMD:IS_RX_MODE.request

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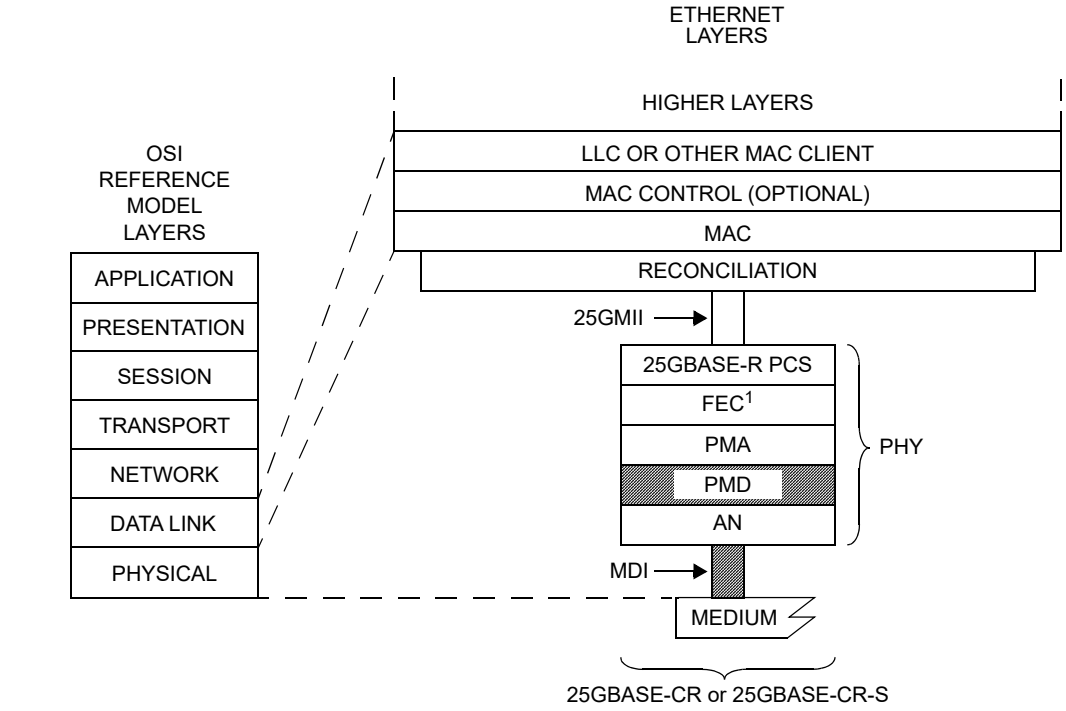

25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 110–1—25GBASE-CR and 25GBASE-CR-S relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

110.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 107.5.)

25GBASE-CR and 25GBASE-CR-S PHYs may be extended using a 25GAUI chip-to-chip (C2C) as a physical instantiation of the inter-sublayer service interface between devices. If 25GAUI C2C is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementer. As examples, the implementer may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

110.4 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the PMD and AN shall be no more than 512 bit times (1 pause_quantum or 20.48 ns). It is assumed that the one way delay through the medium is no more than 1500 bit times (60 ns).

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A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 105.5.

110.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control bits to PMD control variables as shown in Table 110–3, and MDIO status bits to PMD status variables as shown in Table 110–4.

Table 110–3—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable
Polynomial identifier 0	PMD training pattern lane 0	1.1450.12:11	identifier_0
Seed 0	PMD training pattern lane 0	1.1450.10:0	seed_0

Table 110–4—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
Receiver status 0	BASE-R PMD status	1.151.0	rx_trained
Frame lock 0	BASE-R PMD status	1.151.1	frame_lock
Startup protocol status 0	BASE-R PMD status	1.151.2	training
Training failure 0	BASE-R PMD status	1.151.3	training_failure

110.6 FEC modes

A 25GBASE-CR PHY implements the BASE-R FEC sublayer (Clause 74) and the 25GBASE-R RS-FEC sublayer (Clause 108). A 25GBASE-CR-S PHY implements the BASE-R FEC sublayer (Clause 74). Each FEC sublayer can be either enabled or disabled, according to AN resolution or management control.

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Three FEC modes are supported:

a) When the 25GBASE-R RS-FEC sublayer is enabled, the PHY is defined to operate in the RS-FEC mode.
b) When the BASE-R FEC sublayer is enabled, the PHY is defined to operate in the BASE-R FEC mode.
c) When no FEC sublayer is enabled, the PHY is defined to operate in the no-FEC mode.

A 25GBASE-CR PHY can operate in RS-FEC, BASE-R FEC, or no-FEC mode. A 25GBASE-CR-S PHY can operate in either BASE-R FEC or no-FEC mode.

The cable assembly types (CA-25G-N, CA-25G-S, or CA-25G-L, see 110.10) that the PHY supports and the required PMD receiver characteristics (110.8.4) depend on the FEC mode.

The FEC mode is determined using AN (Clause 73) if AN is enabled, or by management control if AN is disabled, and is used in both transmit direction and receive direction. It is recommended to configure the AN FEC advertisement such that only modes that are compatible with the type of the cable assembly attached to the MDI are selected.

110.7 PMD functional specifications

110.7.1 Link block diagram

One direction of a 25GBASE-CR or 25GBASE-CR-S link is shown in Figure 110–2.

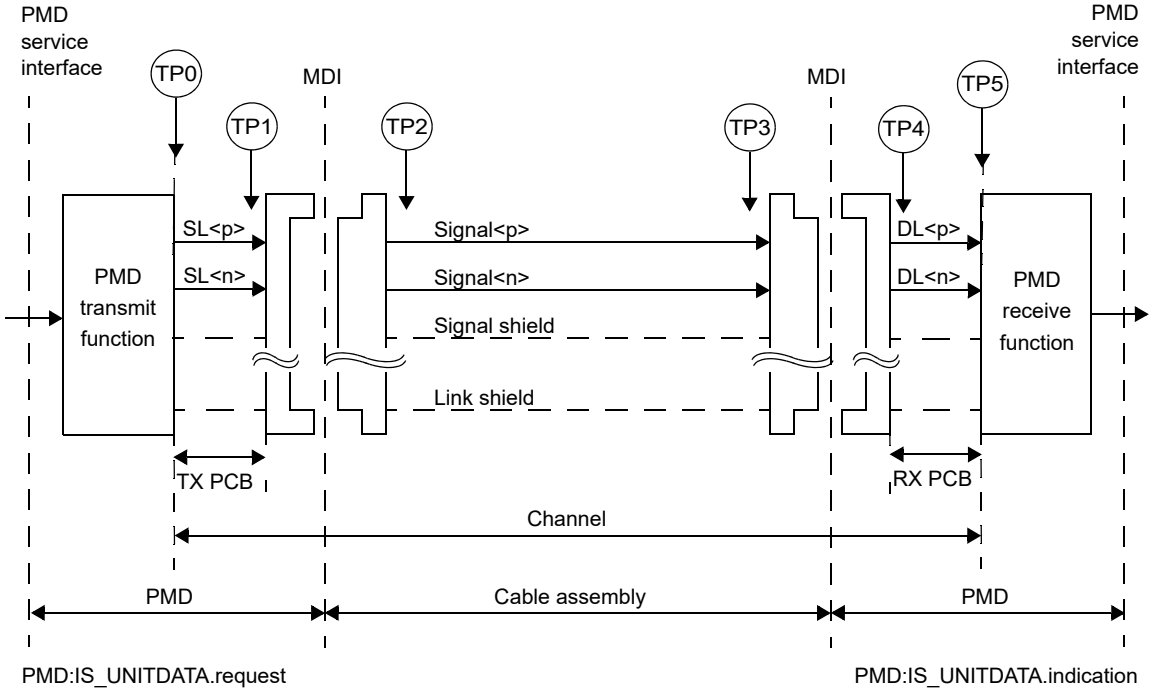

Figure 110–2—25GBASE-CR or 25GBASE-CR-S link (one direction is illustrated)

Note that the source lane (SL) signals SL<p> and SL<n> are the positive and negative sides of the transmitter's differential signal pair and the destination lane (DL) signals DL<p> and DL<n> are the positive and negative sides of the receiver's differential signal pair.

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For purposes of system conformance, the PMD sublayer is standardized at the test points described in this subclause.

The electrical transmit signal is defined at TP2. Unless specified otherwise, all transmitter measurements and tests defined in 110.8.3 are made at TP2 utilizing the test fixture specified in 110B.1.1.

The electrical receive signal is defined at TP3. Unless specified otherwise, all receiver measurements and tests defined in 110.8.4 are performed at TP3 utilizing the test fixture specified in 110B.1.1.

A mated connector pair has been included in both the transmitter and receiver specifications defined in 110.8.3 and 110.8.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is provided in 92.8.3.6. Annex 110A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system.

The channel (see 110.9) is defined between the transmitter (TP0) and receiver (TP5) blocks to include the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss, as illustrated in Figure 110–2. All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 110–2. The cable assembly test fixture of 110B.1.2, or its equivalent, is required for measuring the cable assembly specifications in 110.10 at TP1 and TP4. Two mated connector pairs and the cable assembly test fixture have been included in the cable assembly specifications defined in 110.10. Transmitter and receiver differential controlled impedance printed circuit board insertion losses defined between TP0 and the MDI and between the MDI and TP5, respectively, are provided informatively in 92A.4.

Table 110–5 describes the defined test points illustrated in Figure 110–2.

Table 110–5—Test points

Test points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 110–2. The cable assembly test fixture of 110B.1.2, or its equivalent, is required for measuring the cable assembly specifications in 110.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 110.8.3 and 110.8.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 92.8.3.6.
TP2	Unless specified otherwise, all transmitter measurements defined in 110.8.3 are made at TP2 utilizing the test fixture specified in 110B.1.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 110.8.4 are made at TP3 utilizing the test fixture specified in 110B.1.1.

110.7.2 PMD transmit function

The PMD transmit function shall convert the bit stream requested by the PMD service interface message PMD:IS_UNITDATA.request(tx_bit) into an electrical signal. The electrical signal shall then be delivered to the MDI, according to the transmit electrical specifications in 110.8.3. A positive differential output voltage (SL<p> minus SL<n>) shall correspond to tx_bit = one.

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If the optional EEE deep sleep capability is supported, the following requirements apply. When the PMD service interface message PMD:IS_TX_MODE.request(tx_mode) is received with tx_mode = ALERT, the PMD transmit function shall transmit a periodic sequence, where each period of the sequence consists of 8 ones followed by 8 zeros, with the transmit equalizer coefficients set to the preset values (see 72.6.10.2.3.1). This sequence is transmitted regardless of the value of tx_bit presented by the PMD:IS_UNITDATA.request primitive. When tx_mode is not set to ALERT, the transmit equalizer coefficients are set to the values determined via the startup protocol (see 110.7.10).

110.7.3 PMD receive function

The PMD receive function shall convert the electrical signal from the MDI into a bit stream for delivery to the PMD service interface using the messages PMD:IS_UNITDATA.indication(rx_bit). A positive differential input voltage (DL<p> minus DL<n>) shall correspond to rx_bit = one.

110.7.4 Global PMD signal detect function

The Global PMD signal detect function is used by the PMD to indicate the successful completion of the startup protocol by the PMD control function (see 110.7.10). Global_PMD_signal_detect is set to zero when the value of the variable signal_detect is set to false by the Training state diagram (see Figure 72–5). Global_PMD_signal_detect is set to one when the value of signal_detect is set to true.

If training is disabled by the management variable mr_training_enable (see 110.5), Global_PMD_signal_detect shall be set to one.

If the optional EEE deep sleep capability is supported, the following requirements apply. The value of Global_PMD_signal_detect is set to zero when the PMD service interface message PMD:IS_RX_MODE.request(rx_mode) is initially received with rx_mode = QUIET. While rx_mode is set to QUIET, Global_PMD_signal_detect shall be set to one within 500 ns of the application of the ALERT pattern defined in 110.7.2, with peak-to-peak differential voltage of 720 mV measured at TP2, to the differential pair at the input of the cable assembly that connects the transmitter to the receiver. While rx_mode is set to QUIET, Global_PMD_signal_detect shall not be set to one when the voltage input to the differential pair of the cable assembly that connects the transmitter to the receiver is less than or equal to 70 mV peak-to-peak differential.

When the MDIO is implemented, this function maps the variables to registers and bits as defined in 110.5.

110.7.5 Global PMD transmit disable function

The Global PMD transmit disable function is mandatory if EEE deep sleep capability is supported and is otherwise optional.When Global_PMD_transmit_disable variable is set to one, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max.) with Tx disabled in Table 92–6.

If a PMD fault (110.7.7) is detected, then the PMD may set Global_PMD_transmit_disable to one.

Loopback, as defined in 110.7.6, shall not be affected by Global_PMD_transmit_disable.

The following additional requirements apply when the optional EEE deep sleep capability is supported:

a) The Global PMD transmit disable function shall turn off the transmitter as specified in 92.8.3.1 when tx_mode transitions to QUIET from any other value.
b) The Global PMD transmit disable function shall turn on the transmitter as specified in 92.8.3.1 when tx_mode transitions from QUIET to any other value.

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110.7.6 Loopback mode

Local loopback mode is provided by the adjacent PMA (see Clause 109) as a test function. When loopback mode is enabled, transmission requests passed to the transmitter are sent directly to the receiver, overriding any signal detected by the receiver on its attached link. Note that loopback mode does not affect the state of the transmitter, which continues to send data (unless disabled).

Control of the loopback function is specified in 109.4.2.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

110.7.7 PMD fault function

PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault. If the MDIO interface is implemented, then PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

110.7.8 PMD transmit fault function

The PMD transmit fault function is optional. The faults detected by this function are implementation specific, but the assertion of Global_PMD_transmit_disable is not considered a transmit fault.

If PMD_transmit_fault is set to one, then Global_PMD_transmit_disable should also be set to one.

If the MDIO interface is implemented, then PMD_transmit_fault shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

110.7.9 PMD receive fault function

The PMD receive fault function is optional. The faults detected by this function are implementation specific. A fault is indicated by setting the variable PMD_receive_fault to one.

If the MDIO interface is implemented, then PMD_receive_fault shall be mapped to the Receive fault bit as specified in 45.2.1.7.5.

110.7.10 PMD control function

25GBASE-CR and 25GBASE-CR-S PMDs shall use the same control function as lane 0 of 100GBASE-CR4, as defined in 92.7.12.

The variables seed_0 and polynomial_0 control the training pattern. It is recommended that implementations with multiple PMDs use distinct values of polynomial_0 for PMDs that are coupled by crosstalk.

110.8 Electrical characteristics

110.8.1 Signal levels

The MDI (see 110.11) is a low-swing AC-coupled differential interface. AC-coupling within the plug connectors, as defined in 110.11.1, allows for interoperability between components operating from different supply voltages.

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110.8.2 Signal paths

The MDI transmit and receive paths are point-to-point connections. Each path comprises two complementary signals, which form a balanced differential pair. There is one differential path in each direction for a total of two pairs, or four connections.

110.8.3 Transmitter characteristics

Transmitter electrical characteristics at TP2 for 25GBASE-CR and 25GBASE-CR-S PHYs shall be the same as those of a single lane of 100GBASE-CR4, as summarized in Table 92–6 and detailed in 92.8.3.1 through 92.8.3.9, with the exception that the value of linear fit pulse peak (min.) is $0.49 \times v_f$. The transmitter specifications at TP0 are provided informatively in 110A.2.

110.8.4 Receiver characteristics

Receiver electrical characteristics are specified at TP3. The receiver shall meet the return loss requirements specified in 92.8.4.2 and 92.8.4.3. In addition, the requirements in 110.8.4.1, 110.8.4.2, 110.8.4.3 and 110.8.4.4 apply.

The receiver specifications at TP5 are provided informatively in 110A.3.

110.8.4.1 Receiver input amplitude tolerance

When a 25GBASE-CR or 25GBASE-CR-S PMD receiver is connected to a compliant transmitter whose peak-to-peak differential output voltage, as defined by 92.8.3.1 using preset equalizer coefficients, is 1200 mV, using a compliant cable assembly with the minimum insertion loss specified in 110.10.2, the following BER requirements apply.

a) When the RS-FEC mode is used, the PMD receiver shall operate at a BER better than 10^{-5}.
b) When the BASE-R FEC mode is used, the PMD receiver shall operate at a BER better than 10^{-8}.
c) When the no-FEC mode is used, the PMD receiver shall operate at a BER better than 10^{-12}.

The receiver is allowed to control the transmitter equalizer coefficients, using the protocol defined in 92.7.12 or an equivalent process, to meet these requirements.

110.8.4.2 Receiver interference tolerance test

Receiver interference tolerance is measured according to the requirements listed in 110.8.4.2.1 through 110.8.4.2.5.

A 25GBASE-CR PHY shall comply with the receiver interference tolerance test requirements for the RS-FEC, BASE-R FEC, and no-FEC modes. A 25GBASE-CR-S PHY shall comply with the receiver interference tolerance test requirements for the BASE-R FEC and no-FEC modes.

Two tests are defined for each FEC mode. Test 1 includes a low-loss channel, identical for all FEC modes. Test 2 includes a high-loss channel, which is different for each FEC mode. The cable assembly used in the test channel (see 110.8.4.2.2) shall meet the cable assembly Channel Operating Margin (COM) as specified in 110.10.7, with CA-25G-L COM parameter values being used for RS-FEC mode test, CA-25G-S COM parameter values being used for BASE-R FEC mode test, and CA-25G-N COM parameter values being used for no-FEC mode test.

The test requirements for the RS-FEC mode are provided in Table 110–6. The test requirements for the BASE-R FEC mode are provided in Table 110–7. The test requirements for the no-FEC mode are provided in Table 110–8.

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Table 110–6—25GBASE-CR interference tolerance parameters, RS-FEC mode

Parameter	Test 1 (low loss)		Test 2 (high loss)		Units
	Min	Max	Min	Max	
Test pattern	Scrambled idle encoded by RS-FEC				
RS-FEC symbol error ratio required[a]	$< 10^{-4}$				
Test channel insertion loss at 12.8906 GHz[b]	14.3	14.8	29.44	29.94	dB
Cable assembly insertion loss at 12.8906 GHz	8	10	20.48	22.48	dB
COM[c]	3		3		dB
b_{max} used in COM calculation	1				
DER_0 used in COM calculation	10^{-5}				

[a]The RS-FEC symbol error ratio is measured using the RS-FEC symbol error counter (see 108.6.9).
[b]Insertion loss between the two test references (see Figure 110–3b).
[c]The COM value is the target value for the SNR_TX calibration defined in 110.8.4.2.3 item f). The SNR_TX value measured at the Tx test reference should be as close as practical to the value needed to produce the target COM. If lower SNR_TX values are used, this would demonstrate margin to the specification but this is not required for compliance.

Table 110–7—25GBASE-CR and 25GBASE-CR-S interference tolerance parameters, BASE-R FEC mode

Parameter	Test 1 (low loss)		Test 2 (high loss)		Units
	Min	Max	Min	Max	
Test pattern	Scrambled idle encoded by BASE-R FEC				
BASE-R FEC corrected block ratio required[a,b]	$< 2.1 \times 10^{-5}$				
Test channel insertion loss at 12.8906 GHz[c]	14.3	14.8	23.44	23.94	dB
Cable assembly insertion loss at 12.8906 GHz	8	10	14.48	16.48	dB
COM[d]	3		3		dB
b_{max} used in COM calculation	0.5				
DER_0 used in COM calculation	10^{-8}				

[a]The BASE-R FEC corrected block ratio is measured using the FEC corrected blocks counter (see 74.8.4.1).
[b]The FEC uncorrected blocks counter (see 74.8.4.2) is required to indicate zero errors during the test unless the test duration is such that the uncorrected block ratio can be verified to be less than 4.7×10^{-10}.
[c]Insertion loss between the two test references (see Figure 110–3b).
[d]The COM value is the target value for the SNR_TX calibration defined in 110.8.4.2.3 item f). The SNR_TX value measured at the Tx test reference should be as close as practical to the value needed to produce the target COM. If lower SNR_TX values are used, this would demonstrate margin to the specification but this is not required for compliance.

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Table 110–8—25GBASE-CR and 25GBASE-CR-S interference tolerance parameters, no-FEC mode

Parameter	Test 1 (low loss)		Test 2 (high loss)		Units
	Min	Max	Min	Max	
Test pattern	Scrambled idle or PRBS31				
Bit error ratio required[a]	$< 10^{-12}$				
Test channel insertion loss at 12.8906 GHz[b]	14.3	14.8	22.48	22.98	dB
Cable assembly insertion loss at 12.9806 GHz	8	10	13.5	15.5	dB
COM[c]	3		2.2		dB
b_{max} used in COM calculation	0.35				
DER_0 used in COM calculation	10^{-12}				

[a]The bit error ratio is measured using the PCS errored blocks counter (see 49.2.14.2) or the PMA PRBS31 error counter (see 109.4.4.4) as appropriate.
[b]Insertion loss between the two test references (see Figure 110–3b).
[c]The COM value is the target value for the SNR_TX calibration defined in 110.8.4.2.3 item f). The SNR_TX value measured at the Tx test reference should be as close as practical to the value needed to produce the target COM. If lower SNR_TX values are used, this would demonstrate margin to the specification but this is not required for compliance.

110.8.4.2.1 Test setup

The interference tolerance test is performed with the setup shown in Figure 110–3a. The requirements of this subclause are verified at the test references in Figure 110–3a and Figure 110–3b. The cable assembly unused single-ended paths are terminated in 50 Ω to provide 100 Ω differential termination.

NOTE—The cable assembly provides AC-coupling as specified in 110.11.

110.8.4.2.2 Test channel

The test channel (as depicted in Figure 110–3a) consists of the following:

a) A cable assembly meeting the requirements of 110.10 and the insertion loss specified for the test being performed.
b) A cable assembly test fixture (see 110B.1.2 and 92.11.2).
c) A frequency-dependent attenuator.

NOTE—The frequency-dependent attenuator represents a Tx host channel and may be implemented with PCB traces and test cables.

110.8.4.2.3 Test channel calibration

The scattering parameters of the test channel are measured at the test references as illustrated in Figure 110–3b using the cable assembly test fixtures specified in 110B.1.

The insertion loss at 12.8906 GHz of the signal path between the test references in Figure 110–3b is within the limits in Table 110–6, Table 110–7, or Table 110–8, as appropriate for the test being performed.

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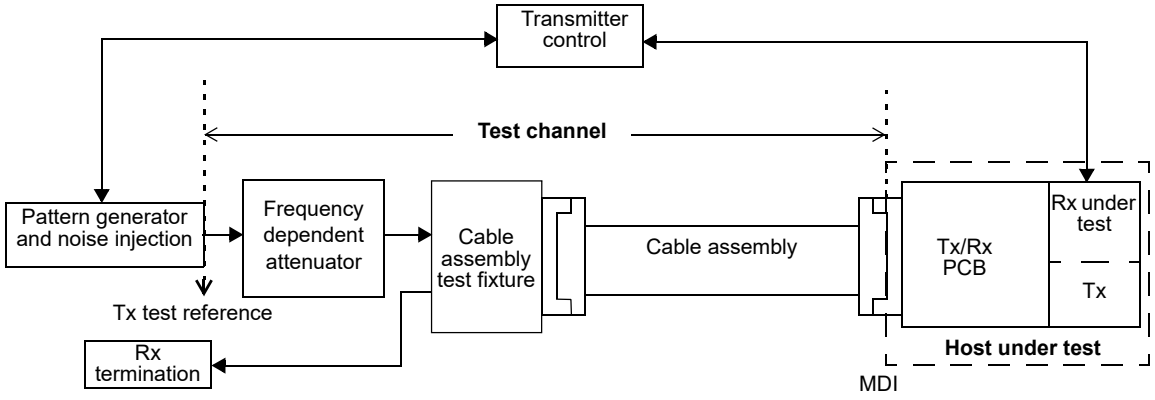

NOTE—The MDI of the host under test is not included in the test channel.

Figure 110–3a—Interference tolerance test setup

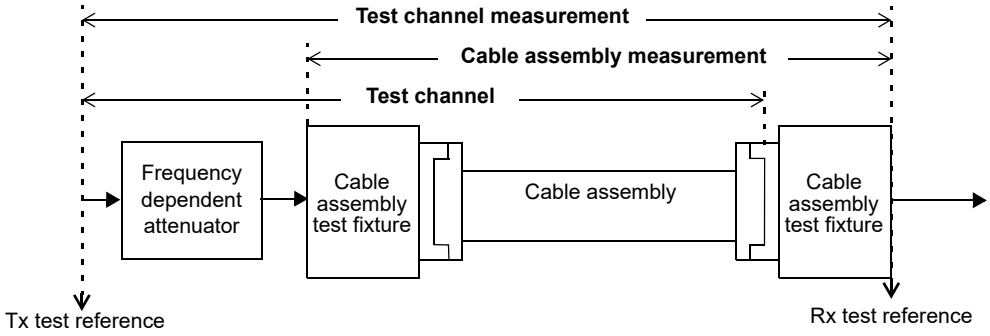

Figure 110–3b—Test channel calibration

The COM is calculated using the method and parameters of 110.10.7 with the following considerations:

a) The channel signal path is $SCHS_p$ = cascade($S^{(CTSP)}$, $S^{(HOSP)}$), where cascade() is defined in 93A.1.2.1, $S^{(HOSP)}$ is defined in 110.10.7.1.1, and $S^{(CTSP)}$ is the measured channel between the test references in Figure 110–3b.

b) The COM parameters are as modified by Table 110–6, Table 110–7, or Table 110–8, as appropriate for the test being performed.

c) COM is calculated using both Test 1 and Test 2 device package model transmission line lengths listed in Table 110–11 on the receiver side. The value of COM is taken as the lower of the two calculated values.

d) The augmented signal path in 93A.1.2 is replaced by S_p determined from Equation (110–1) (effectively omitting the transmitter device package model $S^{(tp)}$). The filtered voltage transfer function $H^{(k)}(f)$ calculated in Equation (93A–19) uses the filter $H_t(f)$ defined by Equation (93A–46), where T_r is the 20% to 80% transition time at the Tx test reference. T_r is measured using the method in 86A.5.3.3, with the exception that the observation filter bandwidth is 33 GHz instead of 12 GHz. T_r is measured with the transmit equalizer turned off (i.e., coefficients set to the preset values, see 72.6.10.2.3.1).

e) Even-odd jitter, effective bounded uncorrelated jitter and effective random jitter without noise injection (see 110.8.4.2.4) are measured at the Tx test reference and comply with the specification in 92.8.3.8.1 and 92.8.3.8.2. In the calculation of COM, A_{DD} is set to half of the value of $EBUJ$ and σ_{RJ}

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is set to the value of *ERJ*, replacing the values in Table 110–11. It is recommended to adjust the pattern generator jitter such that the effective bounded uncorrelated jitter and the effective total uncorrelated jitter (see 92.8.3.8.2) are as close as practical to their limits in Table 92–6.

f) The SNR_{TX} value that results in the required COM value for the test is calculated. The injected noise (see 110.8.4.2.4) is set such that the SNDR, as measured at the Tx test reference using the procedure in 92.8.3.7, matches the calculated SNR_{TX} value.

$$S_p = \text{cascade}(SCHS_p, S^{(rp)}) \quad (110–1)$$

where

cascade()	is defined in 93A.1.2.1
$SCHS_p$	is defined in item a) above
$S^{(rp)}$	is defined in 93A.1.2.4

110.8.4.2.4 Pattern generator and noise injection

The pattern generator transmits data to the device under test. At the start of transmitter training, the pattern generator output amplitude shall be 800 mV peak-to-peak differential when measured on an alternating one-zero pattern. The output amplitude, measured on an alternating one-zero pattern, is not permitted to exceed 800 mV peak-to-peak differential during transmitter training. The output waveform of the pattern generator shall comply with 110.8.1.

Broadband noise is added to the signal before the Tx test reference, with noise level set according to step f in 110.8.4.2.3.

110.8.4.2.5 Test procedure

The pattern generator is first configured to transmit the training pattern defined in 110.7.10. During this initialization period, the device under test (DUT) configures the pattern generator transmit equalizer to the coefficient settings it would select using the protocol described in 72.6.10 and the receiver is tuned using its optimization method. The coefficient settings may be communicated via the startup protocol or by other means.

After the pattern generator equalizer has been configured and the receiver tuned, the pattern generator is set to generate the test pattern specified in Table 110–6, Table 110–7, or Table 110–8, as appropriate for the test being performed. During the test, the transmitter in the device under test transmits the same pattern type specified for the test, with equalization turned off (preset condition).

For 25GBASE-CR and 25GBASE-CR-S PHYs, the receiver under test meets the error requirements specified for the tests in Table 110–7 and Table 110–8. For a 25GBASE-CR PHY, the receiver under test meets the error requirement specified for the test in Table 110–6.

110.8.4.3 Receiver jitter tolerance

Jitter tolerance in RS-FEC mode is measured with a channel meeting the insertion loss of Test 2 and the RS-FEC symbol error ratio requirement specified in Table 110–6. Jitter tolerance in BASE-R FEC mode is measured with a channel meeting the insertion loss of Test 2 and the corrected block ratio requirement specified in Table 110–7. Jitter tolerance in no-FEC mode is measured with a channel meeting the insertion loss of Test 2 and the bit error ratio requirement specified in Table 110–8.

Receiver jitter tolerance is verified for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 110–9. The test setup and procedure of 110.8.4.2 are used, with the exception that no noise is injected (i.e., step f in 110.8.4.2.3 is not performed). In addition, jitter with the specified frequency is applied

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to the transmitter and the jitter amplitude is adjusted to obtain the specified peak-to-peak jitter for that frequency at the Tx test reference.

For a 25GBASE-CR-S PHY, the receiver under test shall meet the error requirements specified for the tests in Table 110–7 and Table 110–8, for each case listed in Table 110–9. For a 25GBASE-CR PHY, the receiver under test shall also meet the error requirement specified for the test in Table 110–6 for each case listed in Table 110–9.

Table 110–9—Receiver jitter tolerance parameters

Parameter	Case A values	Case B values	Units
Jitter frequency	190	940	kHz
Peak-to-peak jitter amplitude	5	1	UI

110.8.4.4 Signaling rate range

25GBASE-CR and 25GBASE-CR-S PHYs shall comply with the receiver requirements of 110.8.4.2 and 110.8.4.3 for any signaling rate in the range 25.78125 GBd ± 100 ppm. The corresponding unit interval is approximately 38.787879 ps.

110.9 Channel characteristics

The channel is defined between TP0 and TP5 to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly as illustrated in Figure 110–2. The channel insertion loss, return loss, COM, and the transmitter and receiver differential controlled impedance printed circuit board parameters are provided informatively in 110A.4 through 110A.7.

Channel definitions apply for links between two PHYs that can each be either 25GBASE-CR or 25GBASE-CR-S.

110.10 Cable assembly characteristics

Cable assemblies defined in this subclause contain insulated conductors terminated in a connector at each end for use as link segments between MDIs. Cable assemblies are primarily intended as point-to-point links between 25GBASE-CR or 25GBASE-CR-S PHYs using controlled impedance cables. Since 25GBASE-CR and 25GBASE-CR-S PHYs have two specified MDI connectors, single-lane (SFP28, specified in 110.11.1) and multi-lane (QSFP28, specified in 92.12), there are three possible combinations of the connectors at each end. The possible cable assembly types are described in Annex 110C.

All cable assembly measurements are to be made between TP1 and TP4 with cable assembly test fixtures as specified in Annex 110B. These cable assembly specifications are based upon twinaxial cable characteristics, but other cable types are acceptable if the specifications of this subclause are met.

Three cable assembly types are specified, with different COM requirements:

a) Cable assembly long (CA-25G-L): Cable assembly that supports links between two PHYs that operate in RS-FEC mode with error correction enabled on both receivers, with achievable cable length of at least 5 m.

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b) Cable assembly short (CA-25G-S): Cable assembly that supports links between two PHYs that operate in BASE-R FEC mode, with achievable cable length of at least 3 m.

c) Cable assembly no-FEC (CA-25G-N): Cable assembly that supports links between two PHYs that operate in no-FEC mode, with achievable cable length of at least 3 m.

NOTE—It may be possible to construct compliant cable assemblies longer than indicated. Length of a cable assembly does not imply compliance to specifications.

Table 110–10 provides a summary of the cable assembly characteristics for CA-25G-L, CA-25G-S, and CA-25G-N, and references to the subclauses addressing each parameter. Due to the improved error correction capability in RS-FEC mode, the specified maximum insertion loss for CA-25G-L is larger than that of CA-25G-S. Likewise, due to the error correction capability provided in BASE-R FEC mode, the specified maximum insertion loss for CA-25G-S is larger than that of CA-25G-N. All other parameters except for some of the input parameters for the COM calculation are identically specified.

Table 110–10—Cable assembly characteristics summary

Description	Reference	CA-25G-L	CA-25G-S	CA-25G-N	Unit
Maximum insertion loss at 12.8906 GHz	110.10.2	22.48	16.48	15.5	dB
Minimum insertion loss at 12.8906 GHz	110.10.2	8			dB
Minimum differential return loss at 12.8906 GHz	110.10.3	6			dB
Differential to common-mode return loss	110.10.4	Equation (92–28)			dB
Differential to common-mode conversion loss	110.10.5	Equation (92–29)			dB
Common-mode to common-mode return loss	110.10.6	Equation (92–30)			dB
COM	110.10.7	See Table 110–11			dB

110.10.1 Characteristic impedance and reference impedance

The nominal differential characteristic impedance of the cable assembly is 100 Ω. The differential reference impedance for cable assembly specifications shall be 100 Ω.

110.10.2 Cable assembly insertion loss

The measured insertion loss of the CA-25G-L, CA-25G-S, and CA-25G-N cable assembly shall be greater than or equal to the minimum cable assembly insertion loss given in Equation (92–26) and illustrated in Figure 92–12.

The measured insertion loss at 12.8906 GHz of the CA-25G-L cable assembly shall be less than or equal to 22.48 dB. The measured insertion loss at 12.8906 GHz of the CA-25G-S cable assembly shall be less than or equal to 16.48 dB. The measured insertion loss at 12.8906 GHz of the CA-25G-N cable assembly shall be less than or equal to 15.5 dB.

110.10.3 Cable assembly differential return loss

The cable assembly differential return loss shall meet the requirements of 92.10.3.

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110.10.4 Differential to common-mode return loss

The cable assembly differential to common-mode return loss shall meet the requirements of 92.10.4.

110.10.5 Differential to common-mode conversion loss

The cable assembly differential to common-mode conversion loss shall meet the requirements of 92.10.5.

110.10.6 Common-mode to common-mode return loss

The cable assembly common-mode to common-mode return loss shall meet the requirements of 92.10.6.

110.10.7 Cable assembly Channel Operating Margin

The cable assembly Channel Operating Margin (COM) for each lane is derived from measurements of the cable assembly signal, near-end crosstalk and far-end crosstalk paths. COM is computed using the path calculations defined in 110.10.7.1 and the procedure in 93A.1, where T_r is 8 ps for $H_t(f)$ as used in Equation (93A–19). The specific paths used depend on cable assembly form factor (see Annex 110C), as described in 110.10.7.2.

COM parameter values for the three cable assembly types, CA-25G-L, CA-25G-S, and CA-25G-N, are provided in Table 110–11.

Table 110–11—COM parameter values

Parameter	Symbol	CA-25G-N	CA-25G-S	CA-25G-L[a]	Units
Signaling rate	f_b	25.78125			GBd
Maximum start frequency	f_{min}	0.05			GHz
Maximum frequency step[b]	Δf	0.01			GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface	 C_d z_p z_p C_p	 2.5×10^{-4} 12 30 1.8×10^{-4}			 nF mm mm nF
Single-ended reference resistance	R_0	50			Ω
Single-ended termination resistance	R_d	55			Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$			GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.62			—
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.18 0 0.02			—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.38 0 0.02			—

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Table 110–11—COM parameter values *(continued)*

Parameter	Symbol	CA-25G-N	CA-25G-S	CA-25G-L[a]	Units
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –16 0 1	 –13 0 1	 –13 0 1	 dB dB dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	$f_b / 4$			GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b / 4$ f_b			GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.4 0.6 0.6			 V V V
Number of signal levels	L	2			—
Level separation mismatch ratio	R_{LM}	1			—
Transmitter signal-to-noise ratio	SNR_{TX}	29	29	29	dB
Number of samples per unit interval	M	32			—
Decision feedback equalizer (DFE) length	N_b	14			—
Normalized DFE coefficient magnitude limit, for $n = 1$ to N_b	$b_{max}(n)$	0.35	0.5	1	—
Random jitter, RMS	σ_{RJ}	0.01			UI
Dual-Dirac jitter, peak	A_{DD}	0.05			UI
One-sided noise spectral density	η_0	5.2×10^{-8}			V^2/GHz
Target detector error ratio	DER_0	10^{-12}	10^{-8}	10^{-5}	—
Channel Operating Margin (min.)	COM	3[c]	3	3	dB

[a]The parameters for CA-25G-L are the same as those for 100GBASE-CR4 (Table 93–8), except for g_{DC}, A_{fe}, and SNR_{TX}.
[b]For cable lengths greater than 4 m, a frequency step (Δf) no larger than 5 MHz is recommended.
[c]For CA-25G-N cable assemblies with insertion loss at 12.8906 GHz greater than 12 dB, the minimum COM is relaxed to 2.2 dB.

Test 1 and Test 2 differ in the value of the device package model transmission line length z_p. COM for any channel within the cable assembly shall be greater than or equal to the Channel Operating Margin (min.) value specified in Table 110–11 for both Test 1 and Test 2.

110.10.7.1 Channel signal and crosstalk path calculations

The channel paths between TP0 and TP5 used for calculation of the cable assembly COM consist of measured cable assembly signal and crosstalk paths, representative transmitter PCB signal paths, and representative receiver PCB signal paths.

The transmitter and receiver PCB signal paths are calculated using the method defined in 93A.1.2.3. The scattering parameters for a PCB are defined by Equation (93A–13), Equation (93A–14), and the parameter

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values given in Table 92–12. The PCB trace length parameter z_p has different value for each specific signal path, as specified in 110.10.7.1.1 and 110.10.7.1.2.

The channel path calculations use the function cascade() defined in 93A.1.2.1.

110.10.7.1.1 Channel signal path

The scattering parameters of the channel signal path from TP0 to TP5 are calculated using Equation (110–2). The transmitter and receiver PCB signal paths are both denoted as $S^{(HOSP)}$ and are calculated from Equation (93A–13) and Equation (93A–14) using the parameter values given in Table 92–12 and z_p = 151 mm, representing an insertion loss of 6.26 dB at 12.8906 GHz on each PCB.

$$SCHS_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOSP)}, S^{(CASP)}), S^{(HOSP)}) \quad (110–2)$$

where

$SCHS_p^{(k)}$ is the channel signal path

$S^{(HOSP)}$ is the host (transmitter or receiver) PCB signal path

$S^{(CASP)}$ is the cable assembly signal path (TP1 to TP4)

k is equal to zero

110.10.7.1.2 Channel crosstalk paths

The MDI is the significant contributor to crosstalk and is included in and characterized by the cable assembly crosstalk measurements. Crosstalk includes a near-end path where the aggressor is the PMD transmitter, and for specific form factors, near-end and alien far-end crosstalk paths where the aggressors are other PMD transmitters that are connected to the same cable assembly.

For the channel crosstalk paths, the receiver PCB model is $S^{(HOSP)}$ as defined in 110.10.7.1.1. The aggressor transmitter host PCB model is denoted as $S^{(HOTxSP)}$ and is calculated from Equation (93A–13) and Equation (93A–14) using the parameter values given in Table 92–12 and z_p = 72 mm, representing an insertion loss of 3 dB at 12.8906 GHz. The transmitter host PCB insertion loss is lower than that used for the signal path, to allow for a reasonable worst-case crosstalk in the COM calculation.

The scattering parameters of the channel near-end crosstalk paths are calculated using Equation (110–3). The scattering parameters of the channel alien far-end crosstalk paths are calculated using Equation (110–4).

$$SCHNXT_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOTxSP)}, S^{(CANXTk)}), S^{(HOSP)}) \quad (110–3)$$

where

$SCHNXT_p^{(k)}$ is the near-end crosstalk path

$S^{(HOSP)}$ is the host receiver PCB signal path defined in 110.10.7.1.1

$S^{(HOTxSP)}$ is the aggressor transmitter PCB signal path

$S^{(CANXTk)}$ is the cable assembly near-end crosstalk path k (TP1 to TP4)

k is the index of the near-end crosstalk path

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$$SCHAFXT_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOTxSP)}, S^{(CAFXTk)}), S^{(HOSP)}) \quad (110–4)$$

where

$SCHAFXT_p^{(k)}$ is the alien far-end crosstalk path

$S^{(HOSP)}$ is the host receiver PCB signal path defined in 110.10.7.1.1

$S^{(HOTxSP)}$ is the aggressor transmitter PCB signal path

$S^{(CAFXTk)}$ is the cable assembly far-end crosstalk path k (TP1 to TP4)

k is the index of the alien far-end crosstalk path

110.10.7.2 Signal and crosstalk paths used in calculation of COM

Cable assemblies have several form factors, as described in Annex 110C. The choice of signal and crosstalk paths for calculation of COM is specific to each cable assembly form factor, as specified in 110.10.7.2.1 through 110.10.7.2.4.

110.10.7.2.1 SFP28 to SFP28

The SFP28 to SFP28 channel structure includes the signal path, one near-end crosstalk path and no alien far-end crosstalk. The signal and near-end crosstalk paths are used in calculation of COM.

The signal path is calculated using Equation (110–2).

The near-end crosstalk path is calculated using Equation (110–3).

110.10.7.2.2 QSFP28 to SFP28

The QSFP28 to SFP28 channel structure includes the signal path, three alien far-end and one near-end crosstalk path. These five paths are used in calculation of COM. Crosstalk from transmitters on other SFP28 connectors is assumed to be insignificant.

The signal path is calculated using Equation (110–2).

The near-end crosstalk path is calculated using Equation (110–3), with k equal to 1.

The three alien far-end crosstalk paths are calculated using Equation (110–4), with k values from 1 to 3.

110.10.7.2.3 SFP28 to QSFP28

The SFP28 to QSFP28 channel structure includes the signal path, three alien far-end and four near-end crosstalk paths. These eight paths are used in calculation of COM.

The signal path is calculated using Equation (110–2).

The near-end crosstalk paths are calculated using Equation (110–3), with k values from 1 to 4.

The three alien far-end crosstalk paths are calculated using Equation (110–4), with k values from 1 to 3.

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110.10.7.2.4 QSFP28 to QSFP28

The QSFP28 to QSFP28 channel structure includes the same paths defined for the SFP28 to QSFP28 channel, and COM is calculated in the same way, as defined in 110.10.7.2.3.

110.11 MDI specification

This subclause defines the 25GBASE-CR Media Dependent Interface (MDI), used for both 25GBASE-CR and 25GBASE-CR-S Physical Layers. The MDI couples the PMD (110.7 and 110.8) to the cable assembly (110.10).

The mechanical interface between the PMD and the cable assembly may be either a mated pair of connectors meeting the requirements of 110.11.1 (single-lane MDI) or a mated pair of connectors meeting the requirements of 92.12.1.1 (multi-lane MDI). The plug connector is used on the cable assembly and the receptacle is used on the PMD.

For the multi-lane MDI, each of the paired transmit and receive lanes (SL1, DL1), (SL2, DL2), (SL3, DL3) or (SL4, DL4) may be used for the transmit and receive connections (SL and DL) of a 25GBASE-CR or 25GBASE-CR-S PHY.

For 25GBASE-CR plug connectors, the receive lanes are AC-coupled; the AC-coupling shall be within the plug connectors. It should be noted that there may be various methods for AC-coupling in actual implementations. The low-frequency 3 dB cutoff of the AC-coupling shall be less than 50 kHz. It is recommended that the value of the coupling capacitors be 100 nF. The capacitor limits the inrush charge and baseline wander.

110.11.1 Single-lane MDI connectors

The single-lane MDI uses the SFP+ 28 Gb/s 1X Pluggable (SFP28) plug and receptacle as defined in SFF-8402 and SFF-8432.

The cable assembly connector shall be the SFP28 plug as illustrated in Figure 110–4. The PMD connector shall be the SFP28 receptacle with the mechanical mating interface as illustrated in Figure 110–5. These connectors shall have data signal and signal ground contact assignments as specified in Table 110–12 and electrical performance consistent with the signal quality and electrical requirements of 110.8, 110.9, and 110.10.

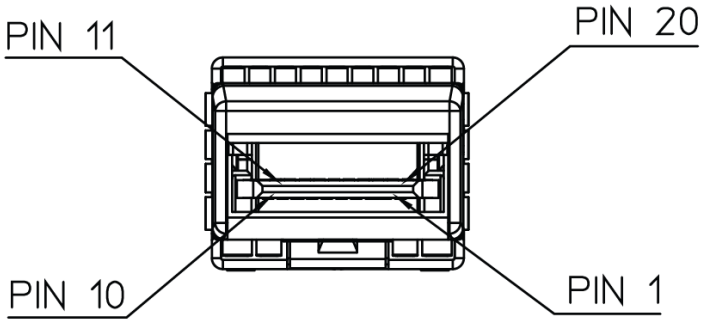

Figure 110–4—SFP28 cable assembly plug

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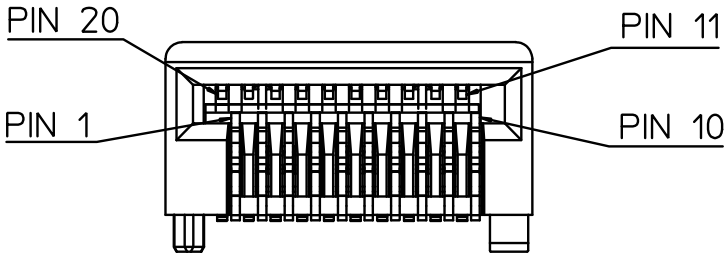

Figure 110–5—SFP28 example MDI board receptacle

Table 110–12—Lane to MDI connector contact mapping

Rx lane	MDI connector contact	Tx lane	MDI connector contact
signal gnd	S11	signal gnd	S17
DL<n>	S12	SL<p>	S18
DL<p>	S13	SL<n>	S19
signal gnd	S14	signal gnd	S20

110.12 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 14.7.

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110.13 Protocol implementation conformance statement (PICS) proforma for Clause 110, Physical Medium Dependent (PMD) sublayer and baseband medium, type 25GBASE-CR and 25GBASE-CR-S[183]

110.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 110, Physical Medium Dependent (PMD) sublayer and baseband medium, type 25GBASE-CR and 25GBASE-CR-S, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

110.13.2 Identification

110.13.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

110.13.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 110, Physical Medium Dependent (PMD) sublayer and baseband medium, type 25GBASE-CR and 25GBASE-CR-S
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[183] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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110.13.3 Major capabilities/options

Item[a]	Feature	Subclause	Value/Comment	Status	Support
*CR	25GBASE-CR	110.1	Supports requirements of 25GBASE-CR PHY	O	Yes [ ] No [ ]
CR-S	25GBASE-CR-S	110.1	Supports requirements of 25GBASE-CR-S PHY	M	Yes [ ]
25GMII	25GMII	110.1	Interface is supported	O	Yes [ ] No [ ]
PCS	25GBASE-R PCS	110.1		M	Yes [ ]
BR-FEC	BASE-R FEC	110.1	Implemented	M	Yes [ ]
RS-FEC	25GBASE-R RS-FEC	110.1	Implemented	CR:M	Yes [ ] N/A [ ]
PMA	25GBASE-R PMA	110.1		M	Yes [ ]
AUI	25GAUI C2C	110.1	Interface is supported	O	Yes [ ] No [ ]
AN	Auto-negotiation	110.1	Device implements Auto-Negotiation	M	Yes [ ]
DC	Delay constraints	110.4	Device conforms to delay constraints specified	M	Yes [ ]
*MD	MDIO capability	110.5	Registers and interface supported	O	Yes [ ] No [ ]
*EEE	EEE deep sleep capability	110.1	Capability is supported	O	Yes [ ] No [ ]
*GTD	Global PMD transmit disable function	110.7.5	Function is supported	EEE: M	Yes [ ] No [ ]
MDIS	Single-lane MDI connector	110.11	Device uses SFP28 as MDI connector	O:2	Yes [ ] N/A [ ]
MDIQ	Quad-lane MDI connector	110.11	Device uses QSFP28 as MDI connector	O:2	Yes [ ] N/A [ ]
*CBL	Cable assembly	110.10	Items marked with CBL include cable assembly specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
CAN	Cable assembly – no FEC	110.10	Cable assembly meets CA-25G-N specifications	CBL: O.1	Yes [ ] No [ ]
CAS	Cable assembly – short	110.10	Cable assembly meets CA-25G-S specifications	CBL: O.1	Yes [ ] No [ ]
CAL	Cable assembly – long	110.10	Cable assembly meets CA-25G-L specifications	CBL: O.1	Yes [ ] No [ ]
FFSS	SFP28 to SFP28	110.10.7.2.1	Cable assembly form factor is SFP28 to SFP28	CBL: O.2	Yes [ ] No [ ]

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Item[a]	Feature	Subclause	Value/Comment	Status	Support
FFQS	QSFP28 to 4×SFP28	110.10.7.2.2 and 110.10.7.2.3	Cable assembly form factor is QSFP28 to 4×SFP28	CBL: O.2	Yes [ ] No [ ]
FFQQ	QSFP28 to QSFP28	110.10.7.2.4	Cable assembly form factor is QSFP28 to 4×SFP28	CBL: O.2	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

110.13.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and base-band medium, type 25GBASE-CR and 25GBASE-CR-S

110.13.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PF1	Transmit function	110.7.2	Converts a logical bit streams from the PMD service interface into an electrical signal and delivers it to the MDI	M	Yes [ ]
PF2	Transmitter signal	110.7.2	A positive differential voltage corresponds to tx_bit = one	M	Yes [ ]
PF3	ALERT signal	110.7.2	Transmit a periodic sequence, where each period of the sequence consists of 8 ones followed by 8 zeros, when tx_mode is set to ALERT	EEE:M	Yes [ ] N/A [ ]
PF4	Receive function	110.7.2	Converts an electrical signal from the MDI into a logical bit stream and delivers it to the PMD service interface	M	Yes [ ]
PF5	Receiver signal	110.7.2	A positive differential voltage corresponds to rx_bit = one	M	Yes [ ]
PF6	When training disabled by management	110.7.2	Global_PMD_signal_detect set to one	M	Yes [ ]
PF7	Global_PMD_signal_detect asserted, rx_mode = QUIET	110.7.4	Set to one within 500 ns following the application of the signal defined in 110.7.4 to the input of the channel	EEE:M	Yes [ ]
PF8	Global_PMD_signal_detect not asserted, rx_mode = QUIET	110.7.4	Not set to one when the signal applied to the input of the channel is less than or equal to 70 mV peak-to-peak differential	EEE:M	Yes [ ]
PF9	Global_PMD_transmit_disable	110.7.5	Disables all transmitters by forcing a constant output level	GTD:M	Yes [ ] N/A [ ]
PF10	Global_PMD_transmit_disable effect on loopback	110.7.5	No effect	GTD:M	Yes [ ] N/A [ ]
PF11	Global PMD transmit disable function, tx_mode transition to QUIET	110.7.5	Turn off transmitter when tx_mode transitions to QUIET from any other value	EEE:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PF12	Global PMD transmit disable function, tx_mode transition from QUIET	110.7.5	Turn on transmitter when tx_mode transitions from QUIET to any other value	EEE:M	Yes [ ] N/A [ ]
PF13	PMD_fault variable mapping to MDIO	110.7.7	Mapped to the fault bit as specified in 45.2.1.2.3	MD:M	Yes [ ] N/A [ ]
PF14	PMD_transmit_fault variable mapping to MDIO	110.7.8	Mapped to Transmit fault bit as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
PF15	PMD_receive_fault variable mapping to MDIO	110.7.9	Mapped to Receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]
PF16	PMD control function	110.7.10	Uses the same control function as lane 0 of 100GBASE-CR4, as defined in 92.7.12	M	Yes [ ]

110.13.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	PMD_fault function	110.7.7	Mapped to the fault bit as specified in 45.2.1.2.3	MD:M	Yes [ ] N/A [ ]
MF2	PMD_transmit_fault function	110.7.8	Mapped to the PMD_transmit_fault bit as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
MF3	PMD_receive_fault function	110.7.9	Contributes to the PMA/PMD receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]

110.13.4.3 Transmitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Test fixture return loss	92.11.1.1	Meets equation constraints	M	Yes [ ]
TC2	Test fixture insertion loss	92.11.1.2	Meets equation constraints	M	Yes [ ]
TC3	Signaling rate	92.8.3.9	25.78125 GBd ± 100 ppm	M	Yes [ ]
TC4	Peak-to-peak differential output voltage	92.8.3.1	Less than or equal to 1200 mV regardless of transmit equalizer setting	M	Yes [ ]
TC5	Peak-to-peak differential output voltage, transmitter disabled	92.8.3.1	Less than or equal to 35 mV	M	Yes [ ]
TC6	DC common-mode output voltage	92.8.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC7	AC common-mode output voltage	92.8.3.1	Less than or equal to 30 mV RMS with respect to signal ground	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC8	The peak-to-peak differential output voltage	92.8.3.1	Less than 30 mV within 500 ns of the transmitter being disabled.	EEE:M	Yes [ ]
TC9	The peak-to-peak differential output voltage	92.8.3.1	Greater than 720 mV within 500 ns of the transmitter being enabled	EEE:M	Yes [ ]
TC10	The peak-to-peak differential output voltage	92.8.3.1	Meets the requirements of 92.8.3 within 1 μs of the transmitter being enabled	EEE:M	Yes [ ]
TC11	DC common-mode output voltage while the transmitter is disabled.	92.8.3.1	Maintained to within ±150 mV of the value for the enabled transmitter	EEE:M	Yes [ ]
TC12	Common-mode output voltage requirements	92.8.3.1	Met regardless of the transmit equalizer setting	M	Yes [ ]
TC13	Differential output return loss (min)	92.8.3.2	Meets equation constraints	M	Yes [ ]
TC14	Reference impedance for differential return loss measurements	92.8.3.2	100 Ω	M	Yes [ ]
TC15	Common-mode to differential-mode output return loss	92.8.3.3	Meets equation constraints	M	Yes [ ]
TC16	Steady-state voltage, v_f	92.8.3.5.2	0.34 V min, 0.6 V max	M	Yes [ ]
TC17	Linear fit pulse peak (min)	110.8.3	$0.49 \times v_f$	M	Yes [ ]
TC18	Coefficient initialization	92.8.3.5.3	Satisfies the requirements of 92.8.3.5.3.	M	Yes [ ]
TC19	Normalized coefficient step size for “increment”	92.8.3.5.4	Between 0.0083 and 0.05	M	Yes [ ]
TC20	Normalized coefficient step size for “decrement”	92.8.3.5.4	Between –0.05 and –0.0083	M	Yes [ ]
TC21	Maximum post-cursor equalization ratio	92.8.3.5.5	Greater than or equal to 4	M	Yes [ ]
TC22	Maximum pre-cursor equalization ratio	92.8.3.5.5	Greater than or equal to 1.54	M	Yes [ ]
TC23	Transmitter output SNDR	92.8.3.7	Greater than or equal to 26 dB	M	Yes [ ]
TC24	Even-odd jitter	92.8.3.8.1	Less than or equal to 0.035 UI regardless of the transmit equalization setting	M	Yes [ ]
TC25	Effective bounded uncorrelated jitter	92.8.3.8.2	Less than or equal to 0.1 UI peak-to-peak regardless of the transmit equalization setting	M	Yes [ ]
TC26	Effective total uncorrelated jitter	92.8.3.8.2	Less than or equal to 0.18 UI RMS regardless of the transmit equalization setting	M	Yes [ ]

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110.13.4.4 Receiver specifications

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Input amplitude tolerance, RS-FEC mode	110.8.4.1	PMD BER better than 10^{-5} under described conditions	CR:M	Yes [ ]
RC2	Input amplitude tolerance, BASE-R FEC mode	110.8.4.1	PMD BER better than 10^{-8} under described conditions	M	Yes [ ]
RC3	Input amplitude tolerance, no-FEC mode	110.8.4.1	PMD BER better than 10^{-12} under described conditions	M	Yes [ ]
RC4	Differential input return loss	92.8.4.2	Meets equation constraints	M	Yes [ ]
RC5	Reference impedance for differential return loss measurements	92.8.4.2	100 Ω	M	Yes [ ]
RC6	Differential to common-mode input return loss	92.8.4.3	Meets equation constraints	M	Yes [ ]
RC7	Interference tolerance, RS-FEC mode	110.8.4.2	Satisfy requirements summarized in Table 110–6	CR:M	Yes [ ] N/A [ ]
RC8	Interference tolerance, BASE-R FEC and no-FEC modes	110.8.4.2	Satisfy requirements summarized in Table 110–7 and Table 110–8	M	Yes [ ]
RC9	Interference tolerance	110.8.4.2	Cable assembly used meets COM requirements	M	Yes [ ]
RC10	Interference tolerance	110.8.4.2.4	Pattern generator amplitude and waveform	M	Yes [ ]
RC11	Jitter tolerance, RS-FEC mode	110.8.4.3	Meets the error requirement specified in Table 110–6 for each case listed in Table 110–9	CR:M	Yes [ ] N/A [ ]
RC12	Jitter tolerance, BASE-R FEC and no-FEC modes	110.8.4.3	Meets the error requirement specified in Table 110–7 and Table 110–8 for each case listed in Table 110–9	M	Yes [ ]
RC13	Signaling rate range	110.8.4.4	25.78125 GBd ± 100 ppm	M	Yes [ ]

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110.13.4.5 Cable assembly specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CA1	Differential reference impedance	92.10.1	100 Ω	CBL:M	Yes [ ] N/A [ ]
CA2	Minimum insertion loss at 12.8906 GHz	110.10.2	Per Equation (92–26)	CBL:M	Yes [ ] N/A [ ]
CA3	Maximum insertion loss at 12.8906 GHz	110.10.2	Less than or equal to 15.5 dB	CAN:M	Yes [ ] N/A [ ]
CA4	Maximum insertion loss at 12.8906 GHz	110.10.2	Less than or equal to 16.48 dB	CAS:M	Yes [ ] N/A [ ]
CA5	Maximum insertion loss at 12.8906 GHz	110.10.2	Less than or equal to 22.48 dB	CAL:M	Yes [ ] N/A [ ]
CA6	Differential return loss	110.10.3	Per Equation (92–27)	CBL:M	Yes [ ] N/A [ ]
CA7	Differential to common-mode input and output return loss	110.10.4	Per Equation (92–28)	CBL:M	Yes [ ] N/A [ ]
CA8	Differential to common-mode conversion loss	110.10.5	Per Equation (92–29)	CBL:M	Yes [ ] N/A [ ]
CA9	Common-mode to common-mode return loss	110.10.6	Per Equation (92–30)	CBL:M	Yes [ ] N/A [ ]
CA10	Cable assembly Channel Operating Margin (COM)	110.10.7	Greater than or equal to the minimum value (in Table 110–11), both Test 1 and Test 2, for all channels within the cable assembly	CBL:M	Yes [ ] N/A [ ]
CA11	AC-coupling	110.11	Within the plug connector, on the receive lane, 3 dB cutoff frequency less than 50 kHz	CBL:M	Yes [ ] N/A [ ]

110.13.4.6 MDI connector specifications

Item	Feature	Subclause	Value/Comment	Status	Support
MDC1	Single-lane MDI connector	110.11.1	SFP28 receptacle.	MDIS:M	Yes [ ] N/A [ ]
MDC2	Quad-lane MDI connector	92.12	QSFP28 receptacle.	MDIQ:M	Yes [ ] N/A [ ]

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110.13.4.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Environmental specifications	110.12	Conform to applicable requirements of 14.7	M	Yes [ ]

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111. Physical Medium Dependent (PMD) sublayer and baseband medium, type 25GBASE-KR and 25GBASE-KR-S

111.1 Overview

This clause specifies the 25GBASE-KR PMD, the 25GBASE-KR-S PMD, and the baseband medium. The specifications are closely related to those of 100GBASE-KR4 (Clause 93) but with a single lane instead of four lanes. This clause also makes use of Annex 93A, Annex 93B, and Annex 93C.

When forming a complete Physical Layer, the PMD shall be connected as illustrated in Figure 111–1, to the appropriate PMA as shown in Table 111–1, to the medium through the MDI and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 111–1—Physical Layer clauses associated with the 25GBASE-KR and 25GBASE-KR-S PMDs

Associated clause	25GBASE-KR	25GBASE-KR-S
106—RS	Required	Required
106—25GMII[a]	Optional	Optional
107—PCS	Required	Required
74—BASE-R FEC[b]	Required	Required
108—RS-FEC[b]	Required	N/A
109—PMA	Required	Required
109A—25GAUI C2C	Optional	Optional
73—Auto-Negotiation	Required	Required
78—Energy Efficient Ethernet	Optional	Optional

[a]The 25GMII is an optional interface. However, if the 25GMII is not implemented, a conforming implementation behaves functionally as though the RS and 25GMII were present.
[b]FEC sublayers can be enabled or disabled according to the FEC mode (see 111.6).

A 25GBASE-KR PHY operates over a channel meeting the requirements of 111.9.1 or 111.9.2. A 25GBASE-KR-S PHY operates over a channel meeting the requirements of 111.9.2. A 25GBASE-KR PHY interoperates with a 25GBASE-KR-S PHY.

When forming a complete 25GBASE-KR or 25GBASE-KR-S Physical Layer, the link BER requirements depend on the FEC mode (see 111.6) according to the following guidelines.

a) If a PHY operates in the RS-FEC mode, and the RS-FEC decoder does not bypass error correction (see 108.5.3.2), the link is required to operate with a BER of 10^{-5} or better.
b) If a PHY operates in the BASE-R FEC mode, the link is required to operate with a BER of 10^{-8} or better.
c) If a PHY operates in the no-FEC mode, or in the RS-FEC mode with error correction bypassed, the link is required to operate with a BER of 10^{-12} or better.

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In this context, a link consists of a compliant PMD transmitter, a compliant PMD receiver, and a channel meeting the requirements of 111.9.1 or 111.9.2.

For a complete Physical Layer, this specification is considered to be satisfied by a frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap.

25GBASE-KR and 25GBASE-KR-S PHYs with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization.

Figure 111–1 shows the relationship of the PMD and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.

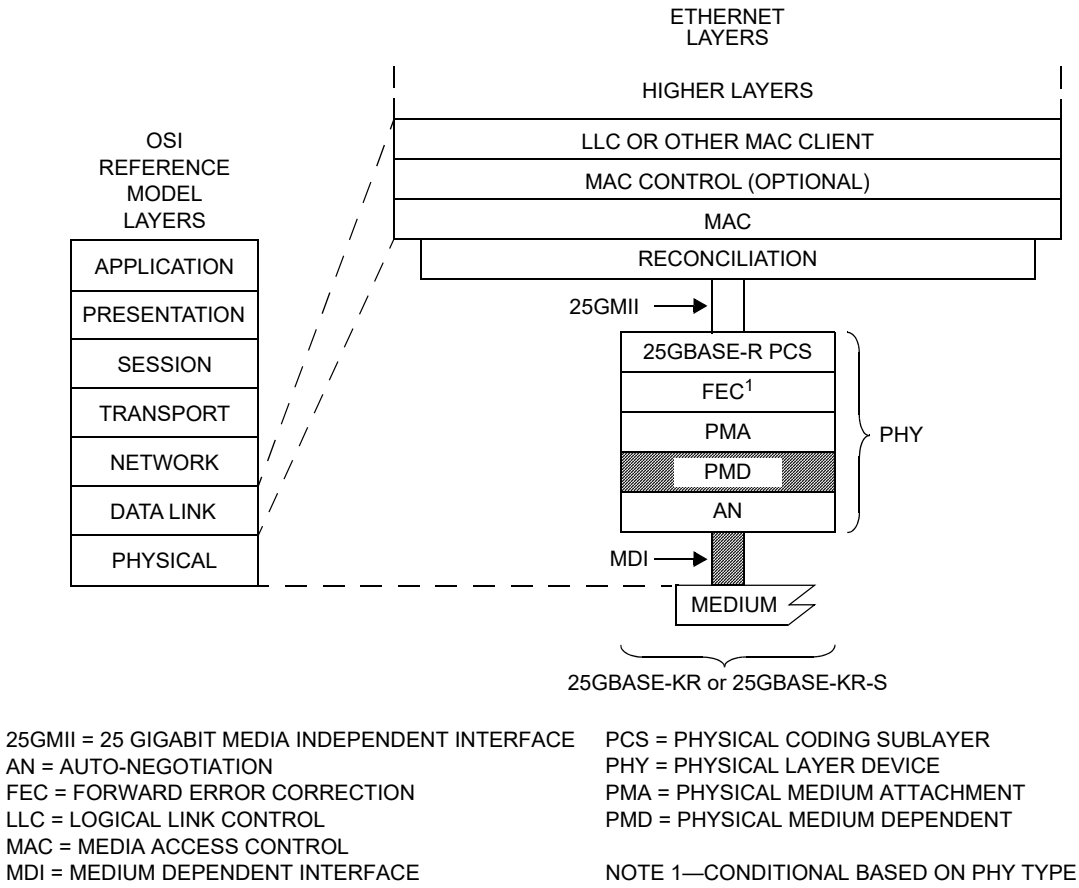

Figure 111–1—25GBASE-KR and 25GBASE-KR-S relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

111.2 PMD service interface

This subclause specifies the services provided by the 25GBASE-KR and 25GBASE-KR-S PMDs. The service interface for these PMDs is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data. The PMD translates the encoded data to and from signals suitable for the medium.

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The PMD service interface is an instance of the inter-sublayer service interface defined in 105.4. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA.request
PMD:IS_UNITDATA.indication
PMD:IS_SIGNAL.indication

The PMA (or the PMD) continuously sends a bit stream to the PMD (or the PMA) at a nominal signaling rate of 25.78125 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable Global_PMD_signal_detect as defined in 111.7.4. When Global_PMD_signal_detect is one, SIGNAL_OK shall be assigned the value OK. When Global_PMD_signal_detect is zero, SIGNAL_OK shall be assigned the value FAIL. When SIGNAL_OK is FAIL, the PMD:IS_UNITDATA.indication parameter is undefined.

If the optional EEE deep sleep capability is supported, then the PMD service interface includes two additional primitives as follows:

PMD:IS_TX_MODE.request
PMD:IS_RX_MODE.request

111.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 107.5.)

25GBASE-KR and 25GBASE-KR-S PHYs may be extended using a 25GAUI chip-to-chip (C2C) as a physical instantiation of the inter-sublayer service interface between devices. If 25GAUI C2C is instantiated, the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementer. As examples, the implementer may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

111.4 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the PMD, AN, and the medium in one direction shall be no more than 512 bit times (1 pause_quantum or 20.48 ns). It is assumed that the one way delay through the medium is no more than 200 bit times (8 ns).

A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 105.5.

111.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control bits to PMD control variables as shown in Table 111–2, and MDIO status bits to PMD status variables as shown in Table 111–3.

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Table 111–2—25GBASE-KR MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable
Polynomial identifier 0	PMD training pattern lane 0	1.1450.12:11	identifier_0
Seed 0	PMD training pattern lane 0	1.1450.10:0	seed_0

Table 111–3—25GBASE-KR MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
Receiver status 0	BASE-R PMD status	1.151.0	rx_trained
Frame lock 0	BASE-R PMD status	1.151.1	frame_lock
Startup protocol status 0	BASE-R PMD status	1.151.2	training
Training failure 0	BASE-R PMD status	1.151.3	training_failure

111.6 FEC modes

A 25GBASE-KR PHY implements the BASE-R FEC sublayer (Clause 74) and the 25GBASE-R RS-FEC sublayer (Clause 108). A 25GBASE-KR-S PHY implements the BASE-R FEC sublayer (Clause 74). Each FEC sublayer can be either enabled or disabled, according to AN resolution or management control.

Three FEC modes are supported:

a) When the 25GBASE-R RS-FEC sublayer is enabled, the PHY is defined to operate in the RS-FEC mode.
b) When the BASE-R FEC sublayer is enabled, the PHY is defined to operate in the BASE-R FEC mode.
c) When no FEC sublayer is enabled, the PHY is defined to operate in the no-FEC mode.

A 25GBASE-KR PHY can operate in RS-FEC, BASE-R FEC, or no-FEC mode. A 25GBASE-KR-S PHY can operate in either BASE-R FEC or no-FEC mode.

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The channel specification (111.9) that the PHY supports and the required PMD receiver characteristics (111.8.3) depend on the FEC mode.

The FEC mode is determined using AN (Clause 73) and is used in both transmit direction and receive direction. It is recommended to configure the AN FEC advertisement such that only modes that are compatible with the specific channel are selected.

111.7 PMD functional specifications

111.7.1 Link block diagram

One direction of a 25GBASE-KR or 25GBASE-KR-S link is shown in Figure 111–2.

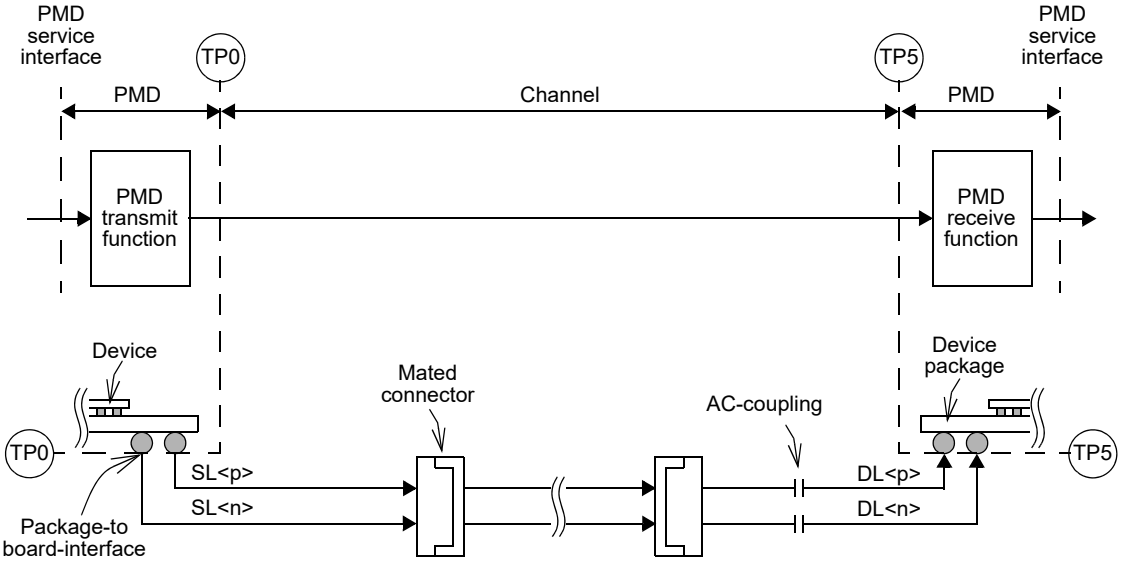

Figure 111–2—25GBASE-KR or 25GBASE-KR-S link (one direction is illustrated)

111.7.2 PMD transmit function

The PMD transmit function shall convert the bit stream requested by the PMD service interface message PMD:IS_UNITDATA.request(tx_bit) into an electrical signal. The electrical signal shall then be delivered to the MDI, according to the transmit electrical specifications in 111.8.2. A positive differential output voltage (SL<p> minus SL<n>) shall correspond to tx_bit = one.

If the optional EEE deep sleep capability is supported, the following requirements apply. When the PMD service interface message PMD:IS_TX_MODE.request(tx_mode) is received with tx_mode = ALERT, the PMD transmit function shall transmit a periodic sequence, where each period of the sequence consists of 8 ones followed by 8 zeros, with the transmit equalizer coefficients set to the preset values (see 72.6.10.2.3.1). This sequence is transmitted regardless of the value of tx_bit presented by the PMD:IS_UNITDATA.request primitive.When tx_mode is not set to ALERT, the transmit equalizer coefficients are set to the values determined via the startup protocol (see 111.7.10).

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111.7.3 PMD receive function

The PMD receive function shall convert the electrical signal from the MDI into a bit stream for delivery to the PMD service interface using the message PMD:IS_UNITDATA.indication(rx_bit). A positive differential input voltage (DL<p> minus DL<n>) shall correspond to rx_bit = one.

111.7.4 Global PMD signal detect function

The Global PMD signal detect function is used by the PMD to indicate the successful completion of the startup protocol by the PMD control function (see 111.7.10). Global_PMD_signal_detect is set to zero when the value of the variable signal_detect is set to false by the Training state diagram (see Figure 72–5). Global_PMD_signal_detect is set to one when the value of signal_detect is set to true.

If training is disabled by the management variable mr_training_enable (see 111.5), Global_PMD_signal_detect shall be set to one.

If the optional EEE deep sleep capability is supported, the following requirements apply. The value of Global_PMD_signal_detect is set to zero when the PMD service interface message PMD:IS_RX_MODE.request(rx_mode) is initially received with rx_mode = QUIET. While rx_mode is set to QUIET, Global_PMD_signal_detect shall be set to one within 500 ns of the application of the ALERT pattern defined in 111.7.2, with peak-to-peak differential voltage of 720 mV as measured at TP0a, to the differential pair at the input of the channel that connects the transmitter to the receiver. While rx_mode is set to QUIET, Global_PMD_signal_detect shall not be set to one when the voltage applied to the input of the differential pair of the channel that connects the transmitter to the receiver is less than or equal to 60 mV peak-to-peak differential.

When the MDIO is implemented, this function maps the variables to registers and bits as defined in 111.5.

111.7.5 Global PMD transmit disable function

The Global PMD transmit disable function is mandatory if the EEE deep sleep capability is supported and is otherwise optional. When this function is supported, it shall meet the following requirements:

a) When Global_PMD_transmit_disable variable is set to one, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage in Table 93–4.
b) If a PMD fault (111.7.7) is detected, then the PMD may set Global_PMD_transmit_disable to one.
c) Loopback, as defined in 111.7.6, shall not be affected by Global_PMD_transmit_disable.
d) The following additional requirements apply when the optional EEE deep sleep capability is supported. The Global PMD transmit disable function shall turn off the transmitter as specified in 93.8.1.3 when tx_mode transitions to QUIET from any other value. The Global PMD transmit disable function shall turn on the transmitter as specified in 93.8.1.3 when tx_mode transitions from QUIET to any other value.

111.7.6 Loopback mode

Local loopback mode is provided by the adjacent PMA (see Clause 109) as a test function. When loopback mode is enabled, transmission requests passed to the transmitter are sent directly to the receiver, overriding any signal detected on its attached link. Note that loopback mode does not affect the state of the transmitter, which continues to send data (unless disabled).

Control of the loopback function is specified in 109.4.2.

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NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

111.7.7 PMD fault function

PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault. If the MDIO is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

111.7.8 PMD transmit fault function

The PMD transmit fault function is optional. The faults detected by this function are implementation specific, but the assertion of Global_PMD_transmit_disable is not considered a transmit fault.

If PMD_transmit_fault is set to one, then Global_PMD_transmit_disable should also be set to one.

If the MDIO interface is implemented, then PMD_transmit_fault shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

111.7.9 PMD receive fault function

The PMD receive fault function is optional. The faults detected by this function are implementation specific. A fault is indicated by setting the variable PMD_receive_fault to one.

If the MDIO interface is implemented, then PMD_receive_fault shall be mapped to the Receive fault bit specified in 45.2.1.7.5.

111.7.10 PMD control function

25GBASE-KR and 25GBASE-KR-S PMDs shall use the same control function as lane 0 of 100GBASE-CR4, as defined in 92.7.12.

The variables seed_0 and polynomial_0 control the training pattern choice. It is recommended that implementations with multiple PMDs use distinct values of polynomial_0 for PMDs that are coupled by crosstalk.

111.8 Electrical characteristics

111.8.1 MDI

The MDI for 25GBASE-KR and 25GBASE-KR-S PHYs is an implementation-dependent direct electrical connection between the PMD and the medium. The MDI comprises two differential pairs, one for the transmit function and one for the receive function, marked by TP0 and TP5 in Figure 111–2.

Transmitter and receiver characteristics are defined at TP0a and TP5a, which are connected to the MDI through the test fixtures described in 93.8.1.1 and 93.8.2.1.

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111.8.2 Transmitter characteristics

Transmitter electrical characteristics at TP0a for 25GBASE-KR and 25GBASE-KR-S shall be the same as those of a single lane of 100GBASE-KR4, as summarized in Table 93–4 and detailed in 93.8.1.1 through 93.8.1.7, with the exception that the value of linear fit pulse peak (min.) is $0.75 \times v_f$.

111.8.3 Receiver characteristics

Receiver electrical characteristics are specified at TP5a. The receiver shall meet the return loss specified in 93.8.2.2 using the text fixture specified in 93.8.2.1. In addition, the requirements in 111.8.3.1 and 111.8.3.2 apply.

111.8.3.1 Receiver interference tolerance

The receiver interference tolerance test setup and method are as specified in 93.8.2.3, for a single lane, with the following considerations:

a) The test requirements in this subclause replace the test requirements in Table 93–6. The test requirements for RS-FEC mode are provided in Table 111–4. The test requirements for BASE-R FEC mode are provided in Table 111–5. The test requirements for no-FEC mode are provided in Table 111–6.
b) COM is calculated using both Test 1 and Test 2 device package model transmission line lengths listed in Table 111–8 on the receiver side. The value of COM is taken as the lower of the two calculated values.
c) The transmitter device package model $S^{(tp)}$ is omitted from Equation (93A–3) in the calculation of COM. The filtered voltage transfer function $H^{(k)}(f)$ calculated in Equation (93A–19) uses the filter $H_t(f)$ defined by Equation (93A–46), where T_r is calculated as $T_r = 1.09 \times T_{rm} - 4.32$ ps and T_{rm} is the measured 20% to 80% transition time of the signal at TP0a. T_{rm} is measured using the method in 86A.5.3.3, with the exception that the observation filter bandwidth is 33 GHz instead of 12 GHz. T_{rm} is measured with the transmit equalizer turned off (i.e., coefficients set to the preset values, see 72.6.10.2.3.1).

It is recommended to adjust the test transmitter jitter such that the effective bounded uncorrelated jitter and the effective total uncorrelated jitter are as close as practical to their limits in Table 93–4.

A 25GBASE-KR PHY shall comply with the receiver interference tolerance test requirements for RS-FEC mode, BASE-R FEC mode and no-FEC mode. A 25GBASE-KR-S PHY shall comply with the receiver interference tolerance test requirements for BASE-R FEC mode and no-FEC mode.

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Table 111–4—25GBASE-KR interference tolerance parameters, RS-FEC mode

Parameter	Test 1 (low loss)		Test 2 (high loss)		Units
	Min	Max	Min	Max	
Insertion loss at 12.89 GHz[a]	30	30.5	35	35.5	dB
COM[b]	3		3		dB
Test pattern	Scrambled idle encoded by RS-FEC				
RSS_DFE4[c]	0.05	—	0.05	—	
RS-FEC symbol error ratio required[d]	$< 10^{-4}$				
b_{max} used in COM calculation	1				
DER_0 used in COM calculation	10^{-5}				

[a]Measured between TPt and TP5 (see Figure 93C–4).
[b]The COM value is the target for the receiver noise level calibration defined in 93C.2 step 7. The channel noise voltage applied in 93C.2 step 8 should be as close as practical to the value needed to produce the target COM. If higher channel noise voltage values are used, this would demonstrate margin to the specification but this is not required for compliance.
[c]The parameter RSS_DFE4 is a figure of merit for the test channel that is defined in 93A.2.
[d]The RS-FEC symbol error ratio is measured using the RS-FEC symbol error counter (see 108.6.9).

Table 111–5—25GBASE-KR and 25GBASE-KR-S interference tolerance parameters, BASE-R FEC mode

Parameter	Test 1 (low loss)		Test 2 (high loss)		Units
	Min	Max	Min	Max	
Insertion loss at 12.89 GHz[a]	16	16.5	30	30.5	dB
COM[b]	3		3		dB
Test pattern	Scrambled idle encoded by BASE-R FEC				
RSS_DFE4[c]	0.05	—	0.05	—	
BASE-R FEC corrected block ratio required[d, e]	$< 2.1 \times 10^{-5}$				
b_{max} used in COM calculation	0.5				
DER_0 used in COM calculation	10^{-8}				

[a]Measured between TPt and TP5 (see Figure 93C–4).
[b]The COM value is the target for the receiver noise level calibration defined in 93C.2 step 7. The channel noise voltage applied in 93C.2 step 8 should be as close as practical to the value needed to produce the target COM. If higher channel noise voltage values are used, this would demonstrate margin to the specification but this is not required for compliance.
[c]The parameter RSS_DFE4 is a figure of merit for the test channel that is defined in 93A.2.
[d]The BASE-R FEC corrected block ratio is measured using the FEC corrected blocks counter (see 74.8.4.1).
[e]The FEC uncorrected blocks counter (see 74.8.4.2) is required to indicate zero errors during the test unless the test duration is such that the uncorrected block ratio can be verified to be less than 4.7×10^{-10}.

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Table 111–6—25GBASE-KR and 25GBASE-KR-S interference tolerance parameters, no-FEC mode

Parameter	Test 1 (low loss)		Test 2 (high loss)		Units
	Min	Max	Min	Max	
Insertion loss at 12.89 GHz[a]	16	16.5	30	30.5	dB
COM[b]	3		3		dB
Test pattern	Scrambled idle or PRBS31				
RSS_DFE4[c]	0.05	—	0.05	—	
Bit error ratio required[d]	$< 10^{-12}$				
b_{max} used in COM calculation	0.35				
DER_0 used in COM calculation	10^{-12}				

[a]Measured between TPt and TP5 (see Figure 93C–4).
[b]The COM value is the target for the receiver noise level calibration defined in 93C.2 step 7. The channel noise voltage applied in 93C.2 step 8 should be as close as practical to the value needed to produce the target COM. If higher channel noise voltage values are used, this would demonstrate margin to the specification but this is not required for compliance.
[c]The parameter RSS_DFE4 is a figure of merit for the test channel that is defined in 93A.2.
[d]The bit error ratio is measured using the PCS errored blocks counter (see 49.2.14.2) or the PMA PRBS31 error counter (see 109.4.4.4) as appropriate.

111.8.3.2 Receiver jitter tolerance

Jitter tolerance in the RS-FEC mode is measured with a channel meeting the insertion loss of Test 2 and the RS-FEC symbol error ratio requirement specified in Table 111–4. Jitter tolerance in the BASE-R FEC mode is measured with a channel meeting the insertion loss of Test 2 and the corrected block ratio requirement specified in Table 111–5. Jitter tolerance in the no-FEC mode is measured with a channel meeting the insertion loss of Test 2 and the bit error ratio requirement specified in Table 111–6.

Receiver jitter tolerance is verified for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 111–7. The test setup shown in Figure 93–12, or its equivalent, is used. The synthesizer frequency is set to the specified jitter frequency and the synthesizer output amplitude is adjusted until the specified peak-to-peak jitter amplitude for that frequency is measured at TP0a. The test procedure is the same as the one described in 111.8.3.1, with the exception that no broadband noise is added.

For 25GBASE-KR and 25GBASE-KR-S PHYs, the receiver under test shall meet the error requirement specified for the tests in Table 111–5 and Table 111–6, for each case listed in Table 111–7. For a 25GBASE-KR PHY, the receiver under test shall also meet the error requirement specified for the test in Table 111–4 for each case listed in Table 111–7.

Table 111–7—Receiver jitter tolerance parameters

Parameter	Case A values	Case B values	Units
Jitter frequency	190	940	kHz
Peak-to-peak jitter amplitude	5	1	UI

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111.9 Channel characteristics

Channel characteristics are defined by Channel Operating Margin (COM), computed using the procedure in 93A.1, where T_r is 12 ps for $H_t(f)$ as used in Equation (93A–19). The parameters used for calculation of COM are different for channels used to connect two PHYs of type 25GBASE-KR and for channels used to connect two PHYs where one or both are of type 25GBASE-KR-S.

Channels used to connect PHYs that operate in the no-FEC mode of operation or in the RS-FEC mode with error correction bypassed shall meet the COM requirement with DER_0 set to 10^{-12} and b_{max} set to 0.35.

All channels shall have AC-coupling as specified in 93.9.4 and are recommended to meet the insertion loss limits in 93.9.2 and the return loss limits in 93.9.3.

111.9.1 25GBASE-KR channel

A 25GBASE-KR channel is used as a link connecting two 25GBASE-KR PHYs. COM parameter values for this channel are provided in Table 111–8.

COM is calculated for two test cases, Test 1 and Test 2, which differ in the value of the device package model transmission line length z_p. COM shall be greater than or equal to 3 dB for each test.

111.9.2 25GBASE-KR-S channel

A 25GBASE-KR-S channel is used as a link between a pair of 25GBASE-KR-S PHYs, between a pair of 25GBASE-KR PHYs, or between a 25GBASE-KR-S PHY and a 25GBASE-KR PHY. COM parameter values for this channel are provided in Table 111–8.

COM is calculated for two test cases, Test 1 and Test 2, which differ in the value of the device package model transmission line length z_p. COM shall be greater than or equal to 3 dB for each test.

Table 111–8—COM parameter values

Parameter	Symbol	25GBASE-KR[a]	25GBASE-KR-S	Units
Signaling rate	f_b	25.78125		GBd
Maximum start frequency	$f_{\min}$	0.05		GHz
Maximum frequency step	Δf	0.01		GHz
Device package model				
Single-ended device capacitance	C_d	2.5×10^{-4}		nF
Transmission line length, Test 1	z_p	12		mm
Transmission line length, Test 2	z_p	30		mm
Single-ended package capacitance at package-to-board interface	C_p	1.8×10^{-4}		nF
Single-ended reference resistance	R_0	50		Ω
Single-ended termination resistance	R_d	55		Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$		GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.62		—

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Table 111–8—COM parameter values *(continued)*

Parameter	Symbol	25GBASE-KR[a]	25GBASE-KR-S	Units
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	–0.18 0 0.02		—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	–0.38 0 0.02		—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	–13 0 1		 dB dB dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	$f_b / 4$		GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b / 4$ f_b		GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.43 0.63 0.63		 V V V
Number of signal levels	L	2		—
Level separation mismatch ratio	R_{LM}	1		—
Transmitter signal-to-noise ratio	SNR_{TX}	27		dB
Number of samples per unit interval	M	32		—
Decision feedback equalizer (DFE) length	N_b	14		—
Normalized DFE coefficient magnitude limit, for $n = 1$ to N_b	$b_{max}(n)$	1	0.5	—
Random jitter, RMS	σ_{RJ}	0.01		UI
Dual-Dirac jitter, peak	A_{DD}	0.05		UI
One-sided noise spectral density	η_0	5.2×10^{-8}		V^2/GHz
Target detector error ratio	DER_0	10^{-5}	10^{-8}	—

[a]The parameters for the 25GBASE-KR channel are the same as those for 100GBASE-KR4 (Table 93–8), except for g_{DC}, A_v, A_{fe}, and A_{ne}.

111.10 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 93.10.

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111.11 Protocol implementation conformance statement (PICS) proforma for Clause 111, Physical Medium Dependent (PMD) sublayer and baseband medium, type 25GBASE-KR and 25GBASE-KR-S[184]

111.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 111, Physical Medium Dependent (PMD) sublayer and baseband medium, type 25GBASE-KR and 25GBASE-KR-S, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

111.11.2 Identification

111.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

111.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 111, Physical Medium Dependent (PMD) sublayer and baseband medium, type 25GBASE-KR and 25GBASE-KR-S
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[184] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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111.11.3 Major capabilities/options

Item[a]	Feature	Subclause	Value/Comment	Status	Support
*KR	25GBASE-KR	111.1	Supports requirements of 25GBASE-KR PHY	O	Yes [ ] No [ ]
KR-S	25GBASE-KR-S	111.1	Supports requirements of 25GBASE-KR-S PHY	M	Yes [ ]
25GMII	25GMII	111.1	Interface is supported	O	Yes [ ] No [ ]
PCS	25GBASE-R PCS	111.1		M	Yes [ ]
BR-FEC	BASE-R FEC	111.1	Implemented	M	Yes [ ]
RS-FEC	25GBASE-R RS-FEC	111.1	Implemented	KR:M	Yes [ ] N/A [ ]
PMA	25GBASE-R PMA	111.1		M	Yes [ ]
25GAUI	25GAUI	111.1	Interface is supported	O	Yes [ ] No [ ]
AN	Auto-negotiation	111.1		M	Yes [ ]
DC	Delay constraints	111.4	Conforms to delay constraints specified	M	Yes [ ]
*MD	MDIO capability	111.5	Registers and interface supported	O	Yes [ ] No [ ]
*EEE	EEE capability	111.1	Capability is supported	O	Yes [ ] No [ ]
*GTD	Global PMD transmit disable function	111.7.5	Function is supported	EEE:M	Yes [ ] No [ ]
*CHNL	Channel	111.9	Channel specifications not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

111.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and base-band medium, type 25GBASE-KR and 25GBASE-KR-S

111.11.4.1 Functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	PMD transmit function	111.7.2	Converts a logical bit stream from the PMD service interface into an electrical signal and delivers it to the MDI	M	Yes [ ]
FS2	Mapping of logical signals to electrical signals	111.7.2	Positive differential output voltage corresponds to tx_bit = one	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
FS3	ALERT signal	111.7.2	Transmit a periodic sequence, where each period of the sequence consists of 8 ones followed by 8 zeros, when tx_mode is set to ALERT	EEE:M	Yes [ ] N/A [ ]
FS4	PMD receive function	111.7.3	Converts an electrical signal from the MDI into a logical bit stream and delivers it to the PMD service interface	M	Yes [ ]
FS5	Mapping of electrical signals to logical signals	111.7.3	Positive differential input voltage corresponds to rx_bit = one	M	Yes [ ]
FS6	SIGNAL_OK mapping	111.2	Set to OK when Global_PMD_signal_detect is one and set to FAIL when Global_PMD_signal_detect is zero	M	Yes [ ]
FS7	Global_PMD_signal_detect	111.7.4	Set to 1 when training disabled by variable mr_training_enable	M	Yes [ ]
FS8	Global_PMD_signal_detect when rx_mode = QUIET	111.7.4	Set to one within 500 ns following the application of the signal defined in 111.7.2 to the input of the channel	EEE:M	Yes [ ] N/A [ ]
FS9	Global_PMD_signal_detect when rx_mode = QUIET	111.7.4	Not set to one when the signal applied to the input of the channel is less than or equal to 60 mV peak-to-peak differential	EEE:M	Yes [ ] N/A [ ]
FS10	Global_PMD_transmit_disable	111.7.5	When set to one, transmitter is turned off	GTD:M	Yes [ ] N/A [ ]
FS11	Global PMD transmit disable function affect on loopback	111.7.5	No effect	GTD:M	Yes [ ] N/A [ ]
FS12	Global PMD transmit disable function, tx_mode transition to QUIET	111.7.5	Turns off transmitter when tx_mode transitions to QUIET from any other value	EEE:M	Yes [ ] N/A [ ]
FS13	Global PMD transmit disable function, tx_mode transition from QUIET	111.7.5	Turns on transmitter when tx_mode transitions from QUIET to any other value	EEE:M	Yes [ ] N/A [ ]
FS14	PMD_fault variable mapping to MDIO	111.7.7	Mapped to the fault bit as specified in 45.2.1.2.3	MD:M	Yes [ ] N/A [ ]
FS15	PMD_transmit_fault variable mapping to MDIO	111.7.8	Mapped to Transmit fault bit as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
FS16	PMD_receive_fault variable mapping to MDIO	111.7.9	Mapped to Receive fault bit as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]
FS17	PMD control function	111.7.10	Defined in 92.7.12	M	Yes [ ]

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111.11.4.2 Transmitter characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Test fixture insertion loss	93.8.1.1	Between 1.2 dB and 1.6 dB at 12.89 GHz	M	Yes [ ]
TC2	Test fixture insertion loss deviation	93.8.1.1	Magnitude less than 0.1 dB	M	Yes [ ]
TC3	Test fixture differential return loss	93.8.1.1	Meets equation constraints	M	Yes [ ]
TC4	Test fixture common-mode return loss	93.8.1.1	Greater than or equal to 10 dB from 0.05 to 13 GHz	M	Yes [ ]
TC5	Signaling rate	93.8.1.2	25.78125 GBd ± 100 ppm	M	Yes [ ]
TC6	Peak-to-peak differential output voltage	93.8.1.3	Less than or equal to 1200 mV regardless of transmit equalizer setting	M	Yes [ ]
TC7	Peak-to-peak differential output voltage, transmitter disabled	93.8.1.3	Less than or equal to 30 mV	M	Yes [ ]
TC8	DC common-mode output voltage	93.8.1.3	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC9	AC common-mode output voltage	93.8.1.3	Less than or equal to 12 mV RMS with respect to signal ground	M	Yes [ ]
TC10	Common-mode output voltage requirements	93.8.1.3	Met regardless of the transmit equalizer setting	M	Yes [ ]
TC11	Transmitter disable timing	93.8.1.3	Peak-to-peak differential output voltage less than 30 mV within 500 ns of the transmitter being disabled	EEE:M	Yes [ ] N/A [ ]
TC12	Transmitter enable timing	93.8.1.3	Peak-to-peak differential output voltage greater than 720 mV within 500 ns of the transmitter being enabled and meet all requirements of 93.8.1 within 1 μs	EEE:M	Yes [ ] N/A [ ]
TC13	Common-mode output voltage, transmitter disabled	93.8.1.3	Maintained to within ±150 mV of the value for the enabled transmitter	EEE:M	Yes [ ] N/A [ ]
TC14	Differential input return loss	93.8.1.4	Meets equation constraints	M	Yes [ ]
TC15	Reference impedance for differential return loss measurements	93.8.1.4	100 Ω	M	Yes [ ]
TC16	Common-mode output return loss	93.8.1.4	Meets equation constraints	M	Yes [ ]
TC17	Reference impedance for common-mode return loss measurements	93.8.1.4	25 Ω	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC18	Steady-state voltage, v_f	93.8.1.5.2	Greater than or equal to 0.4 V and less than or equal to 0.6 V after the transmit equalizer coefficients have been set to the "preset" values	M	Yes [ ]
TC19	Linear fit pulse peak	111.8.2	Greater than 0.75 × v_f after the transmit equalizer coefficients have been set to the "preset" values	M	Yes [ ]
TC20	Coefficient initialization	93.8.1.5.3	Satisfies the requirements of 93.8.1.5.3.	M	Yes [ ]
TC21	Normalized coefficient step size for "increment"	93.8.1.5.4	Between 0.0083 and 0.05	M	Yes [ ]
TC22	Normalized coefficient step size for "decrement"	93.8.1.5.4	Between –0.05 and –0.0083	M	Yes [ ]
TC23	Maximum post-cursor equalization ratio	93.8.1.5.5	Greater than or equal to 4	M	Yes [ ]
TC24	Maximum pre-cursor equalization ratio	93.8.1.5.5	Greater than or equal to 1.54	M	Yes [ ]
TC25	Transmitter output noise and distortion	93.8.1.6	SNDR greater than or equal to 27 dB	M	Yes [ ]
TC26	Even-odd jitter	93.8.1.7	Less than or equal to 0.035 UI regardless of the transmit equalization setting	M	Yes [ ]
TC27	Effective bounded uncor-related jitter	93.8.1.7	Less than or equal to 0.1 UI peak-to-peak regardless of the transmit equalization setting	M	Yes [ ]
TC28	Effective total uncorrelated jitter	93.8.1.7	Less than or equal to 0.18 UI peak-to-peak regardless of the transmit equalization setting	M	Yes [ ]

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111.11.4.3 Receiver characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Test fixture insertion loss	93.8.2.1	Between 1.2 dB and 1.6 dB at 12.89 GHz	M	Yes [ ]
RC2	Test fixture insertion loss deviation	93.8.2.1	Magnitude less than 0.1 dB	M	Yes [ ]
RC3	Test fixture differential return loss	93.8.2.1	Meets equation constraints	M	Yes [ ]
RC4	Test fixture common-mode return loss	93.8.2.1	Greater than or equal to 10 dB from 0.05 GHz to 13 GHz	M	Yes [ ]
RC5	Differential input return loss	93.8.2.2	Meets equation constraints	M	Yes [ ]
RC6	Reference impedance for differential return loss measurements	93.8.2.2	100 Ω	M	Yes [ ]
RC7	Differential to common-mode return loss	93.8.2.2	Meets equation constraints	M	Yes [ ]
RC8	Interference tolerance, RS-FEC mode	111.8.3.1	Satisfy requirements summarized in Table 111–4	KR:M	Yes [ ] N/A [ ]
RC9	Interference tolerance, BASE-R FEC and no-FEC modes	111.8.3.1	Satisfy requirements summarized in Table 111–5 and Table 111–6	M	Yes [ ]
RC10	Jitter tolerance, RS-FEC mode	111.8.3.2	Meets the error requirement specified in Table 111–4 for each case listed in Table 111–7	KR:M	Yes [ ] N/A [ ]
RC11	Jitter tolerance, BASE-R FEC and no-FEC modes	111.8.3.2	Meets the error requirement specified in Table 111–5 and Table 111–6 for each case listed in Table 111–7	M	Yes [ ]

111.11.4.4 Channel characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	COM when PHYs use no-FEC mode or RS-FEC mode with error correction bypassed	111.9	Meet requirements with DER_0=10^{-12} and b_{max}=0.35	CHNL:M	Yes [ ] N/A [ ]
CC2	AC-coupling	111.9	As specified in 93.9.4	CHNL:M	Yes [ ] N/A [ ]
CC3	Channel Operating Margin (COM)	111.9.1	Greater than or equal to 3 dB for each test case	CHNL *KR:M	Yes [ ] N/A [ ]
CC4	Channel Operating Margin (COM)	111.9.2	Greater than or equal to 3 dB for each test case	CHNL *!KR:M	Yes [ ] N/A [ ]

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111.11.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Environmental specifications	111.10	Conform to applicable requirements of 93.10	M	Yes [ ]

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112. Physical Medium Dependent (PMD) sublayer and medium, type 25GBASE-SR

112.1 Overview

This clause specifies the 25GBASE-SR PMD together with the multimode fiber medium. The PMD sublayer provides a point-to-point 25 Gb/s Ethernet link over a pair of multimode fibers, up to at least 100 m. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 112–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 112–1—Physical Layer clauses associated with the 25GBASE-SR PMD

Associated clause	25GBASE-SR
106—RS	Required
106—25GMII[a]	Optional
107—PCS for 25GBASE-R	Required
108—RS-FEC[b]	Required
109—PMA for 25GBASE-R	Required
109A—25GAUI C2C	Optional
109B—25GAUI C2M	Optional
78—Energy Efficient Ethernet	Optional

[a]The 25GMII is an optional interface. However, if the 25GMII is not implemented, a conforming implementation behaves functionally as though the RS and 25GMII were present.
[b]The option to bypass the Clause 108 RS-FEC correction function is not supported.

Figure 112–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 25 Gigabit Ethernet is introduced in Clause 105 and the purpose of each PHY sublayer is summarized in 105.2.

25GBASE-SR PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Further relevant information may be found in Clause 1 (terminology and conventions, references, definitions, and abbreviations) and Annex A (Bibliography, referenced as [B1], [B2], etc.).

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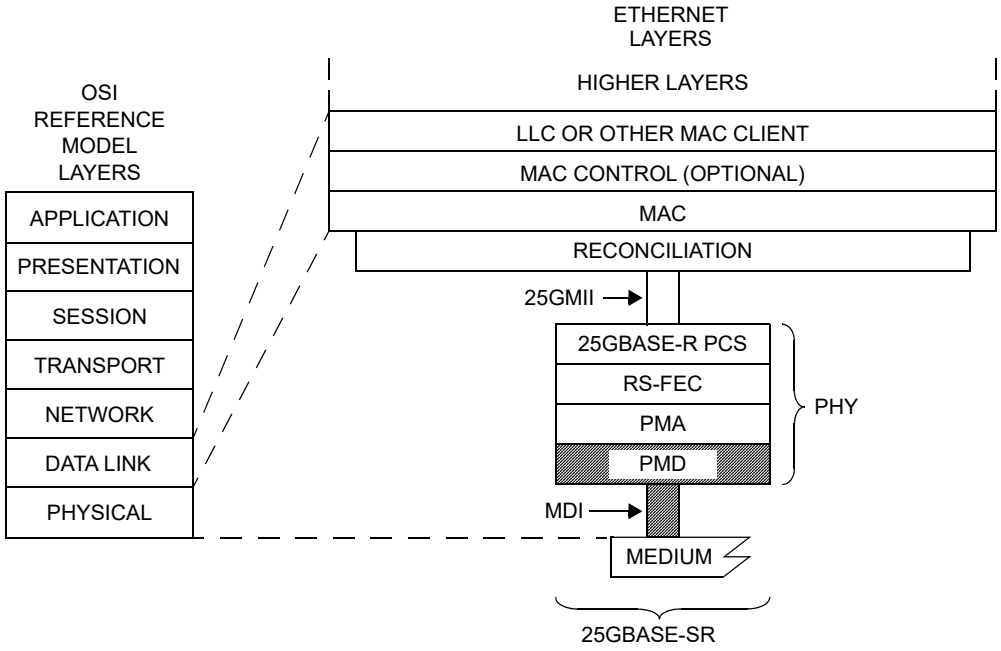

25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
SR = PMD FOR MULTIMODE FIBER

Figure 112–1—25GBASE-SR PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

112.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 5×10^{-5} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap when processed according to Clause 108.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap when processed according to Clause 108.

112.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 25GBASE-SR PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

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The PMD service interface is an instance of the inter-sublayer service interface defined in 105.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA.request
PMD:IS_UNITDATA.indication
PMD:IS_SIGNAL.indication

In the transmit direction, the PMA continuously sends a bit stream to the PMD, at a nominal signaling rate of 25.78125 GBd. The PMD converts this stream of bits into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends a bit stream to the PMA corresponding to the signals received from the MDI, at a nominal signaling rate of 25.78125 GBd.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication(SIGNAL_OK) inter-sublayer service primitive defined in 105.4.

The SIGNAL_DETECT parameter can take on one of the following two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_bit parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_bit parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 112.1.1.

112.3 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation. The sum of the transmit and receive delays at one end of the link contributed by the 25GBASE-SR PMD including 2 m of fiber in one direction shall be no more than 512 bit times (1 pause_quantum or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quantum can be found in 105.5 and its references.

112.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 112–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 112–3.

Table 112–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable

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Table 112–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect

112.5 PMD functional specifications

The 25GBASE-SR PMD performs the transmit and receive functions, which convey data between the PMD service interface and the MDI.

112.5.1 PMD block diagram

The PMD block diagram is shown in Figure 112–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a multimode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 112.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 112.10.3). Unless specified otherwise, all receiver measurements and tests defined in 112.7 are made at TP3.

TP1 and TP4 are optional reference points that may be useful to implementers for testing components (these test points will not typically be accessible in an implemented system).

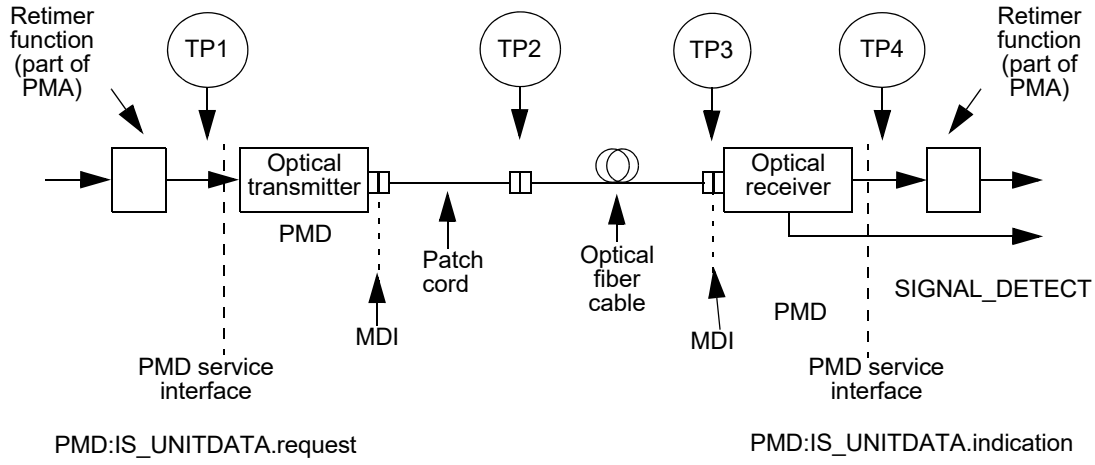

Figure 112–2—Block diagram for 25GBASE-SR transmit/receive paths

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112.5.2 PMD transmit function

The PMD transmit function shall convert the bit stream requested by the PMD service interface messages PMD:IS_UNITDATA.request into an optical signal. The optical signal shall then be delivered to the MDI, according to the transmit optical specifications in this clause. The higher optical power level in each signal shall correspond to tx_bit = one.

112.5.3 PMD receive function

The PMD receive function shall convert the optical signal received from the MDI into a bit stream for delivery to the PMD service interface using the message PMD:IS_UNITDATA.indication, all according to the receive optical specifications in this clause. The higher optical power level in the signal shall correspond to rx_bit = one.

112.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 105.4.

SIGNAL_DETECT shall be an indicator of the presence of the optical signal. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 112–4. The PMD receiver is not required to verify whether a compliant 25GBASE-SR signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 112–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
Average optical power at TP3 ≤ –30 dBm	FAIL
[(Optical power at TP3 ≥ average receive power (min) in Table 95–7) AND (compliant 25GBASE-SR signal input)]	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the PMD global signal detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal. When the MDIO is implemented, the SIGNAL_DETECT value shall be continuously set in response to the magnitude of the optical signal, according to the requirements of Table 112–4.

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112.5.5 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

112.5.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows the optical transmitter to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of the OFF transmitter in Table 95–6.
b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter.

112.5.7 PMD fault function (optional)

If the PMD has detected a local fault on the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

112.5.8 PMD transmit fault function (optional)

If the PMD has detected a local fault on the transmitter, the PMD shall set PMD_transmit_fault to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

112.5.9 PMD receive fault function (optional)

If the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

112.6 PMD to MDI optical specifications for 25GBASE-SR

The operating range for the 25GBASE-SR PMD is defined in Table 112–5. A 25GBASE-SR compliant PMD operates on 50/125 μm multimode fibers, type A1a.2 (OM3) or type A1a.3 (OM4), according to the specifications defined in Table 112–7. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 25GBASE-SR PMD operating at 120 m meets the operating range requirement of 0.5 m to 100 m). The fiber type and operating range shown in Table 112–5 are the same as 100GBASE-SR4 (See Clause 95).

Table 112–5—25GBASE-SR operating range

PMD type	Required operating range[a]
25GBASE-SR	0.5 m to 70 m for OM3
	0.5 m to 100 m for OM4

[a]The RS-FEC correction function may not be bypassed for any operating distance.

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112.6.1 25GBASE-SR transmitter optical specifications

The optical characteristics of a 25GBASE-SR transmitter shall be the same as those of a single lane of 100GBASE-SR4, as specified in Table 95–6 and 95.7.1, with the exception that the test patterns are modified as stated in 112.7.1.

112.6.2 25GBASE-SR receive optical specifications

The optical characteristics of a 25GBASE-SR receiver shall be the same as those of a single lane of 100GBASE-SR4, as specified in Table 95–7 and 95.7.2, with the exceptions that there are no receiver aggressor lanes and the test patterns are modified as stated in 112.7.1.

112.6.3 25GBASE-SR illustrative link power budget

The illustrative power budget and penalties for 25GBASE-SR channels are the same as those of a single lane of 100GBASE-SR4, as specified in Table 95–8 and 95.7.3.

112.7 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified. Optical parameters and measurement methods for 25GBASE-SR are the same as for 100GBASE-SR4, with the exceptions that the multi-lane testing considerations described in 95.8.1.1 do not apply and the test patterns are modified as stated in 112.7.1.

112.7.1 Test patterns for optical parameters

The test patterns used in this clause shall be the same as those used for 100GBASE-SR4, as described in 95.8.1 and shown in Table 95–9, with the exception that pattern 5, the scrambled idle test pattern defined in 82.2.11, is encoded by Clause 108 RS-FEC for 25GBASE-SR. The multi-lane testing considerations described in 95.8.1.1 do not apply. Table 112–6 shows the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined.

Table 112–6—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength, spectral width	3, 5, or valid 25GBASE-SR signal	112.7.2
Average optical power	3, 5, or valid 25GBASE-SR signal	112.7.3
Optical modulation amplitude (OMA)	Square wave or 4	112.7.4
Transmitter and dispersion eye closure (TDEC)	3, 5, or valid 25GBASE-SR signal	112.7.5
Extinction ratio	3, 5, or valid 25GBASE-SR signal	112.7.6
Transmitter optical waveform	3, 5, or valid 25GBASE-SR signal	112.7.7
Stressed receiver sensitivity	3, 5, or valid 25GBASE-SR signal	112.7.8
Stressed eye closure (SEC), calibration	3, 5, or valid 25GBASE-SR signal	112.7.8

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112.7.2 Center wavelength and spectral width

The center wavelength and RMS spectral width shall be within the range given in Table 95–6 if measured per IEC 61280-1-3. The transmitter is modulated using one of the test patterns specified in Table 112–6.

112.7.3 Average optical power

The average optical power shall be within the limits given in Table 95–6 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using the test pattern defined in Table 112–6.

112.7.4 Optical Modulation Amplitude (OMA)

OMA shall be within the limits given in Table 95–6 if measured as defined in 52.9.5 for measurement with a square wave (8 ones, 8 zeros) test pattern or as defined in 68.6.2 (from the variable MeasuredOMA in 68.6.6.2) for measurement with a PRBS9 test pattern. See 112.7.1 for test-pattern information.

112.7.5 Transmitter and dispersion eye closure (TDEC)

TDEC is a measure of the optical transmitter's vertical eye closure, as described in 95.8.5. TDEC shall be within the limits given in Table 95–6 if measured using the methods specified in 95.8.5.1 and 95.8.5.2. Table 112–6 specifies the test patterns to be used for measurement of TDEC. Since 25GBASE-SR is a single lane in each direction, there are no transmitter aggressor lanes.

112.7.6 Extinction ratio

The extinction ratio shall be within the limits given in Table 95–6 if measured using the methods specified in IEC 61280-2-2. The extinction ratio is measured using one of the test patterns specified for extinction ratio in Table 112–6.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 112–6).

112.7.7 Transmitter optical waveform (transmit eye)

The transmitter optical waveform of a port transmitting the test pattern specified in Table 112–6 shall meet the transmitter eye mask coordinates and hit ratio specified in Table 95–6 if measured according to the methods specified in 95.8.7, with the exception that the test patterns are modified as stated in 112.7.1.

112.7.8 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 95–7 if measured using the methods defined in 95.8.8, with the exception that the test patterns are modified as stated in 112.7.1. Since 25GBASE-SR is a single lane in each direction, the conditions for receiver aggressor lanes in Table 95–7 do not apply.

112.8 Safety, installation, environment, and labeling

112.8.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

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112.8.2 Laser safety

25GBASE-SR optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[185]

112.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

112.8.4 Environment

Normative specifications in this clause shall be met by a system integrating a 25GBASE-SR PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate, in the literature associated with the PHY, the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

112.8.5 Electromagnetic emission

A system integrating a 25GBASE-SR PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

112.8.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

112.8.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 25GBASE-SR).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 112.8.2.

[185]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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112.9 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 112–3. The fiber type and length are the same as 100GBASE-SR4 (See Clause 95).

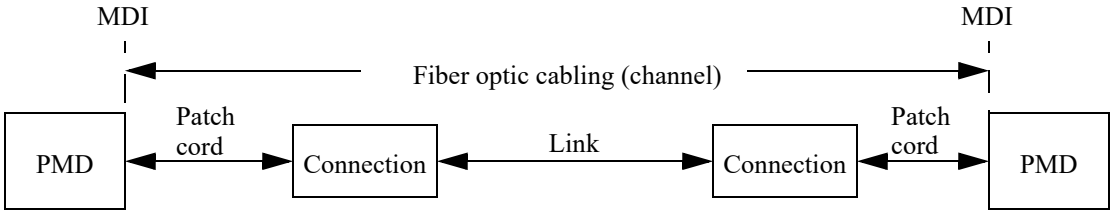

Figure 112–3—Fiber optic cabling model

The channel insertion loss is given in Table 112–7. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, modal dispersion, reflections and losses of all connectors and splices meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1 one-cord method. As OM4 optical fiber meets the requirements for OM3, a channel compliant to the "OM3" column may use OM4 optical fiber, or a combination of OM3 and OM4. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 112–7—Fiber optic cabling (channel) characteristics for 25GBASE-SR

Description	OM3	OM4	Unit
Operating distance (max)	70	100	m
Channel insertion loss[a] (max)	1.8	1.9	dB
Channel insertion loss (min)	0		dB

[a]These channel insertion loss values include cable loss plus 1.5 dB allocated for connection and splice loss, over the wavelength range 840 nm to 860 nm.

112.10 Characteristics of the fiber optic cabling (channel)

The 25GBASE-SR fiber optic cabling shall meet the specifications defined in Table 112–7. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. The requirements for the optical fiber, connection insertion loss, and maximum discrete reflectance are the same as 100GBASE-SR4 (see Clause 95).

112.10.1 Optical fiber cable

The fiber contained within the 25GBASE-SR fiber optic cabling shall comply with the specifications and parameters of Table 112–8. A variety of multimode cable types may satisfy these requirements, provided the resulting channel also meets the specifications of Table 112–7.

112.10.2 Optical fiber connection

An optical fiber connection, as shown in Figure 112–3, consists of a mated pair of optical connectors.

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Table 112–8—Optical fiber and cable characteristics

Description	OM3[a]	OM4[b]	Unit
Nominal core diameter	50		mm
Nominal fiber specification wavelength	850		nm
Effective modal bandwidth (min)[c]	2000	4700	MHz·km
Cabled optical fiber attenuation (max)	3.5		dB/km
Zero dispersion wavelength (λ_0)	$1295 \le \lambda_0 \le 1340$		nm
Chromatic dispersion slope (max) (S_0)	0.105 for $1295 \le \lambda_0 \le 1310$ and $0.000375 \times (1590 - l0)$ for $1310 \le \lambda_0 \le 1340$		ps/nm^2 km

[a]IEC 60793-2-10 type A1a.2
[b]IEC 60793-2-10 type A1a.3
[c]When measured with the launch conditions specified in Table 95–6

112.10.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an average insertion loss per connection of 0.5 dB. Connections with lower loss characteristics may be used provided the requirements of Table 112–7 are met. However, the loss of a single connection shall not exceed 0.75 dB

112.10.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –20 dB.

112.10.3 Medium Dependent Interface (MDI)

The 25GBASE-SR PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 112–3). Examples of an MDI include the following:

a) Connectorized fiber pigtail.
b) PMD receptacle.

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 112.5.1, not at the MDI.

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112.11 Protocol implementation conformance statement (PICS) proforma for Clause 112, Physical Medium Dependent (PMD) sublayer and medium, type 25GBASE-SR[186]

112.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 112, Physical Medium Dependent (PMD) sublayer and medium, type 25GBASE-SR, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

112.11.2 Identification

112.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

112.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 112, Physical Medium Dependent (PMD) sublayer and medium, type 25GBASE-SR
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[186]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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112.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
SR	25GBASE-SR PMD	112.6	Device supports requirements for 25GBASE-SR PHY	O	Yes [ ] No [ ]
*INS	Installation / cable	112.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
CTP1	Reference point TP1 exposed and available for testing	112.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
CTP4	Reference point TP4 exposed and available for testing	112.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
CDC	Delay constraints	112.3	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO capability	112.4	Registers and interface supported	O	Yes [ ] No [ ]

112.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 25GBASE-SR

112.11.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CF1	Compatible with 25GBASE-R RS-FEC, PCS, and PMA	112.1		M	Yes [ ]
CF2	Integration with management functions	112.1		O	Yes [ ] No [ ]
CF3	Bit error ratio	112.1.1	Meets the BER specified in 112.1.1	M	Yes [ ]
CF4	Transmit function	112.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
CF5	Mapping between optical signal and logical signal for transmitter	112.5.2	Higher optical power is a one	M	Yes [ ]
CF6	Receive function	112.5.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
CF7	Conversion of optical signal to electrical signals	112.5.3	For delivery to the PMD service interface	M	Yes [ ]
CF8	Mapping between optical signal and logical signal for receiver	112.5.3	Higher optical power is a one	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
CF9	Global Signal Detect function	112.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
CF10	Global Signal Detect behavior	112.5.4	SIGNAL_DETECT is a global indicator of the presence of an optical signal.	M	Yes [ ]
CF11	PMD reset function	112.5.5	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

112.11.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
CM1	Management register set	112.4		MD:M	Yes [ ] N/A [ ]
CM2	Global transmit disable function	112.5.6	Disables the optical transmitter with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
CM3	PMD_fault function	112.5.7	Sets PMD_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
CM4	PMD_transmit_fault function	112.5.8	Sets PMD_transmit_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
CM5	PMD_receive_fault function	112.5.9	Sets PMD_receive_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]

112.11.4.3 PMD to MDI optical specifications for 25GBASE-SR

Item	Feature	Subclause	Value/Comment	Status	Support
CSR1	Transmitter meets specifications in 95.7.1.	112.6.1	Per definitions in 112.6	M	Yes [ ] N/A [ ]
CSR2	Receiver meets specifications in 95.7.2	112.6.2	Per definitions in 112.6	M	Yes [ ] N/A [ ]

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112.11.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Measurement cable	112.7	2 m to 5 m in length	M	Yes [ ]
COM2	Center wavelength and spectral width	112.7.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
COM3	Average optical power	112.7.3	Per IEC 61280-1-1	M	Yes [ ]
COM4	OMA measurements	112.7.4		M	Yes [ ]
COM5	Transmitter and dispersion eye closure (TDEC)	112.7.5		M	Yes [ ]
COM6	Extinction ratio	112.7.6	Per IEC 61280-2-2	M	Yes [ ]
COM7	Transmit eye	112.7.7		M	Yes [ ]
COM8	Stressed receiver sensitivity	112.7.8	See 112.7.8	M	Yes [ ]

112.11.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CES1	General safety	112.8.1	Conforms to J.2	M	Yes [ ]
CES2	Laser safety—IEC Hazard Level 1	112.8.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
CES3	Electromagnetic interference	112.8.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

112.11.4.6 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
COC1	Fiber optic cabling	112.9	Meets requirements specified in Table 112–7	INS:M	Yes [ ] N/A [ ]
COC2	Optical fiber characteristics	112.10.1	Per Table 112–8	INS:M	Yes [ ] N/A [ ]
COC3	Maximum discrete reflectance	112.10.2.2	Less than –20 dB	INS:M	Yes [ ] N/A [ ]
COC4	MDI requirements	112.10.3	Meets IEC 61753-1 and IEC 61753-022-2	INS:M	Yes [ ] N/A [ ]

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113. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, types 25GBASE-T and 40GBASE-T

113.1 Overview

The 25GBASE-T and 40GBASE-T PHYs are members of the 25 Gb/s and 40 Gb/s Ethernet family of high-speed network specifications. The 25GBASE-T PCS, PMA, and baseband medium specifications are intended for users who want 25 Gb/s performance over balanced twisted-pair structured cabling systems. The 40GBASE-T PCS, PMA, and baseband medium specifications are intended for users who want 40 Gb/s performance over balanced twisted-pair structured cabling systems. 25GBASE-T and 40GBASE-T signaling both require four pairs of balanced cabling as specified in ISO/IEC 11801-1:2016 and ANSI/TIA-568-C.2-1-2016.

This clause defines type 25GBASE-T and 40GBASE-T PCS, PMA sublayers, and Medium Dependent Interfaces (MDI). Together, the PCS and PMA sublayers define a Physical Layer device (PHY). Functional, electrical, and mechanical specifications for the type 25GBASE-T PMA, 40GBASE-T PMA, and MDI are provided in this clause. This clause also specifies the baseband medium used with 25GBASE-T and 40GBASE-T. Management functions are optionally accessible through the management interface defined in Clause 45, or equivalent. Please refer to Table 105–2 and Table 80–2 for associated sublayers and options for assembling a 25 Gb/s system with the 25GBASE-T PHY and a 40 Gb/s system with the 40GBASE-T PHY, respectively.

This clause also specifies 25GBASE-T and 40GBASE-T Low Power Idle (LPI) as part of Energy-Efficient Ethernet (EEE). This allows the PHY to enter a low power mode of operation during periods of low link utilization as described in Clause 78.

Both 25GBASE-T and 40GBASE-T PHYs may optionally support a fast retrain mechanism. Implementation of the fast retrain option is recommended. Configurations wishing to disable fast retrain on the link may do so by advertising lack of support during Auto-Negotiation, thus preventing the link partner from attempting fast retrain and potentially dropping the link, see 45.2.7.10.

113.1.1 Nomenclature

The 25GBASE-T and 40GBASE-T PHYs described in Clause 113 represent two distinct PHY types that share the same PCS, PMA, and MDI specifications subject to frequency scaling, and differences between the 25GMII and the XLGMII specifications. In order to efficiently describe the two PHYs, the nomenclature 25G/40GBASE-T is used to describe specifications that apply to both the 25GBASE-T and 40GBASE-T PHYs. Additionally, for parameters that scale with the PHYs data rate, the parameter *S* is used for scaling. For 25GBASE-T, $S = 0.625$ and for 40GBASE-T, $S = 1$.

Where a functionality or register refers to any member of the MultiGBASE-T set of PHYs, as defined in 1.4.406, that nomenclature is used.

Additionally, because the two PHYs specify different media independent interfaces, the nomenclature 25GMII/XLGMII is used as shorthand for referring to 25GMII for 25GBASE-T and XLGMII for 40GBASE-T. Note that 25GMII uses a 4-bit control word and a 32-bit data word, so that when a transfer of 64 bits (8 octets) is referred to on the media independent interface, this results in a reference like “two/one transfer(s) on the 25GMII/XLGMII.”

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113.1.2 Relationship of 25GBASE-T and 40GBASE-T to other standards

Relations between the 25GBASE-T and 40GBASE-T PHYs, the ISO Open Systems Interconnection (OSI) reference model, and the IEEE 802.3 Ethernet model are shown in Figure 113–1. The PHY sublayers (shown shaded) in Figure 113–1 connect the IEEE 802.3 MAC to the medium.

The 25GBASE-T PHY service interface is the 25GMII, which is defined in Clause 106. The 40GBASE-T PHY service interface is the XLGMII, which is defined in Clause 81.

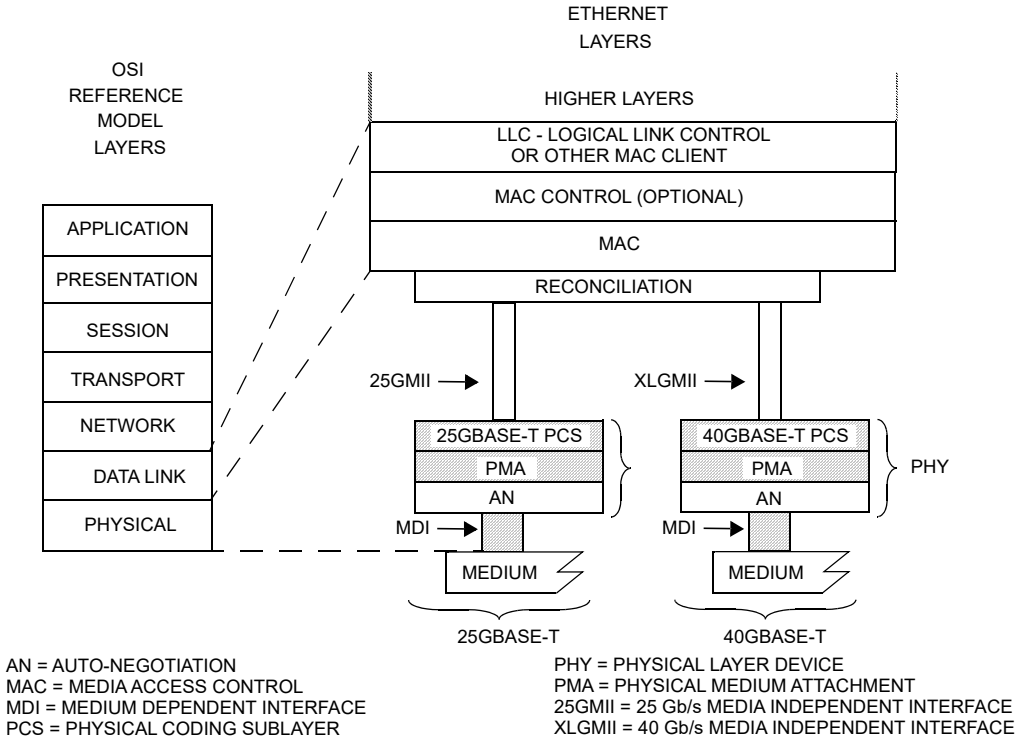

Figure 113–1—Types 25GBASE-T and 40GBASE-T PHY relationship to the ISO Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

113.1.3 Operation of 25GBASE-T and 40GBASE-T

The 25GBASE-T and 40GBASE-T PHY each employ full duplex baseband transmission over four pairs of balanced twisted-pair structured cabling. The aggregate data rates of 25 Gb/s or 40 Gb/s are achieved by transmitting one-quarter of the aggregate data rate in each direction simultaneously on each wire pair, as shown in Figure 113–2. Baseband 16-level PAM signaling with a modulation rate of 2000 MBd for 25GBASE-T and 3200 MBd for 40GBASE-T is used on each of the wire pairs. Ethernet data and control characters are encoded at a rate of 3.125 information bits per PAM16 symbol, along with auxiliary bits. Two consecutively transmitted PAM16 symbols are considered as one two-dimensional (2D) symbol. The 2D symbols are selected from a constrained constellation of 128 maximally spaced 2D symbols, called DSQ128 (double square 128).[187] After link startup, PHY frames consisting of 512 DSQ128 symbols are continuously transmitted. The DSQ128 symbols are determined by seven-bit labels, each comprising 3 RS-FEC (Reed-Solomon FEC) encoded bits and 4 LDPC-encoded bits. The 512 DSQ128 symbols of one PHY frame are

[187]The resulting checkerboard constellation is based on a lattice called RZ^2 in the literature (see Forney [B25]). DSQ constellations have previously been introduced under the name "AMPM" (see Gallagher [B26] for examples of 8 point and 32 point AMPM/DSQ constellations).

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transmitted as 4 × 256 PAM16 symbols over the four wire pairs. Data and Control symbols are embedded in a framing scheme that runs continuously after startup of the link. For 25GBASE-T, the modulation symbol rate of 2000 MBd results in a symbol period of 500 ps. For 40GBASE-T, the modulation symbol rate of 3200 MBd results in a symbol period of 312.5 ps.

A 25GBASE-T or 40GBASE-T PHY can be configured either as a MASTER PHY or as a SLAVE PHY. The MASTER-SLAVE relationship between two stations sharing a link segment is established during Auto-Negotiation (see Clause 28, 113.6, Annex 28B, Annex 28C, and Annex 28D). The MASTER PHY uses a local clock to determine the timing of transmitter operations. The MASTER-SLAVE relationship includes loop timing. The SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in Figure 113–3.

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

25GBASE-T and 40GBASE-T PHYs optionally provide support for LPI as part of EEE (see Clause 78). This extension allows PHYs to enter an LPI mode when either the local or link partner system requests low power operation. The transmit and receive functions may enter and leave the LPI mode independently so that both symmetric and asymmetric operation is supported. While the PHY is in the LPI mode, the PHY periodically transmits a refresh signal to allow the remote PHY to refresh its receiver state (e.g., timing recovery, adaptive filter coefficients) and thereby track long-term variation in the timing of the link or the underlying link segment characteristics. An easily detectable alert signal is transmitted to signal an end to the LPI mode. The alert signal is followed by a wake signal to enable a rapid transition back to the normal operational mode.

25GBASE-T and 40GBASE-T PHYs may optionally support a fast retrain mechanism. This function allows PHYs to quickly recover from link degradation without a normal two-second retrain.

The PCS and PMA subclauses of this document are summarized in 113.1.3.1 and 113.1.3.2. The EEE capability is summarized in 113.1.3.3. Figure 113–3 shows the functional block diagram.

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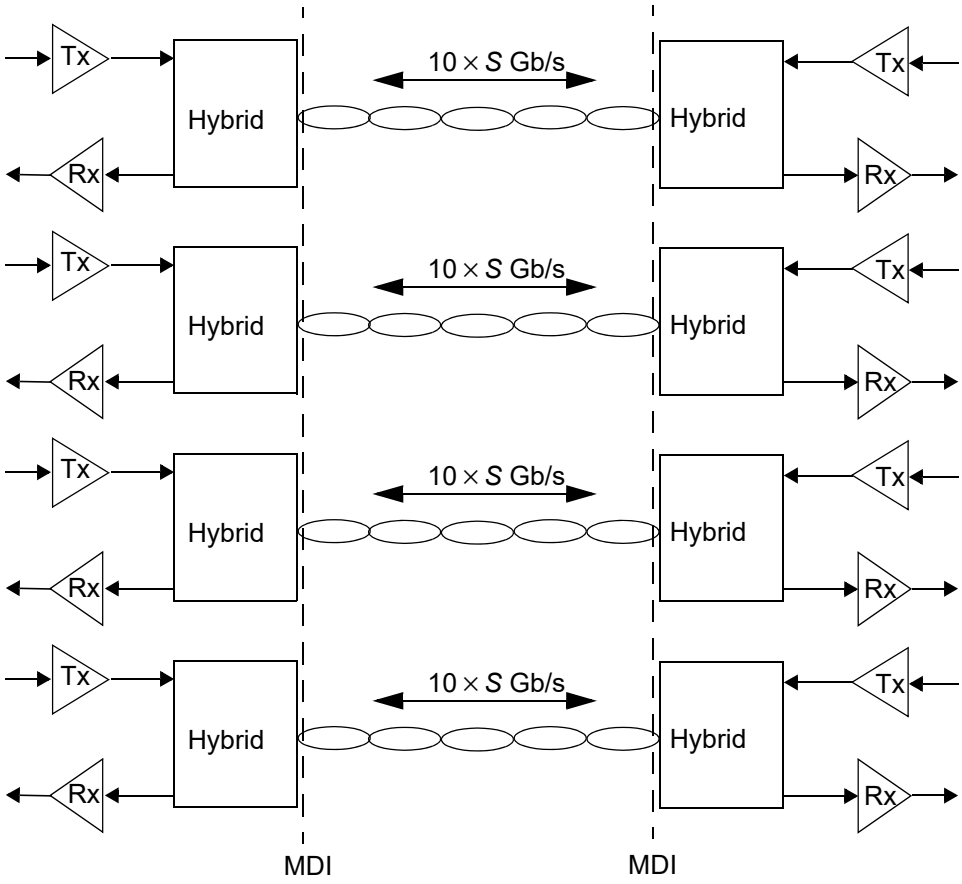

Figure 113–2—25GBASE-T and 40GBASE-T topology

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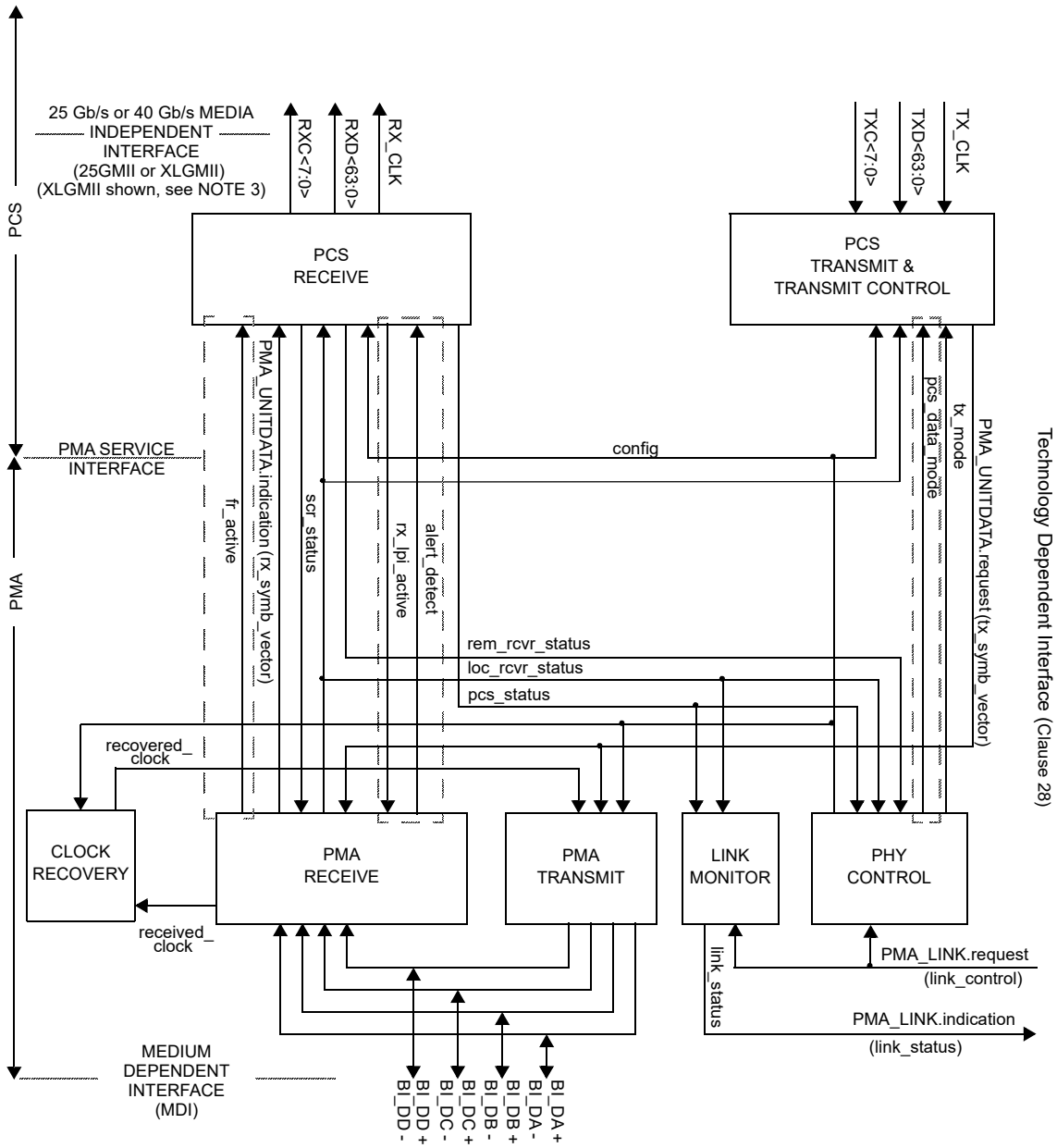

NOTE 1—The recovered_clock arc is shown to indicate delivery of the received clock signal back to PMA TRANSMIT for loop timing.

NOTE 2—pcs_data_mode is required only for the EEE or fast retrain capabilities; alert_detect and rx_lpi_active are only required for the EEE capability; fr_active is only required for the fast retrain capability. Figures and capabilities only required for EEE are noted by dashed boxes.

NOTE 3— Word widths for only the 40 Gb/s Media Independent Interface (XLGMII) are shown for clarity. For the 25 Gb/s Media Independent Interface, a four-bit control word and 32-bit data word are used, i.e., RXC<3:0>, RXD<31:0>, TXC<3:0>, and TXD<31:0>.

Figure 113–3—Functional block diagram

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113.1.3.1 Summary of Physical Coding Sublayer (PCS)

The 25GBASE-T PCS couples a 25 Gb/s Media Independent Interface (25GMII), as described in Clause 106, to the 25GBASE-T Physical Medium Attachment (PMA) sublayer.

The 40GBASE-T PCS couples a 40 Gb/s Media Independent Interface (XLGMII), as described in Clause 81, to the 40GBASE-T Physical Medium Attachment (PMA) sublayer.

In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in normal mode, the PCS receives eight 25GMII or XLGMII data octets provided by two transfers on the 25GMII service interface on TXD<31:0>, or one transfer on the XLGMII service interface of TXD<63:0>, and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the XLGMII transfer (or two 25GMII transfers). Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 50 blocks. The first 48 65-bit blocks are transcoded into six 513-bit blocks, and the subsequent two 65-bit blocks are appended to complete a 50-group block. The resulting bits are then scrambled. This yields an Ethernet payload of $6 \times 513 + 2 \times 65 = 3208$ bits. An auxiliary bit is added after scrambling to obtain a block of 3209 bits.

The 3209 bits are divided into two groups, one of 1486 bits and the other of 1723 bits. To the 1486 bits, among them the auxiliary bit, 2 zero pad bits are added, and these are encoded into 192 eight-bit symbols of an RS-FEC(192, 186, 2^8), code. After substituting 2 random fill bits for the zero pad bits, a total of $1536 = 3 \times 512$ RS-FEC-coded bits are transmitted. The 1723 bits are encoded by a systematic LDPC(1723,2048) encoder, which adds 325 LDPC check bits to form an LDPC codeword of 2048 LDPC-coded bits. The 3×512 RS-FEC-coded bits and the $2048 = 4 \times 512$ LDPC-coded bits are arranged in a frame of 512 seven-bit labels. Each seven-bit label comprises 3 RS-FEC-coded bits and 4 LDPC-coded bits.

The 512 seven-bit labels are mapped into 512 2D modulation symbols selected from a DSQ128 constellation. The DSQ128 symbols are obtained by concatenating two time-adjacent 1D PAM16 symbols and retaining among the 256 possible Cartesian product combinations, 128 maximally spaced 2D symbols.[188]

The DSQ128 constellation is partitioned into eight subsets, each subset containing 16 maximally spaced 2D symbols. The three RS-FEC-coded bits of each seven-bit label select one DSQ128 subset, and the four LDPC-coded-bits of the label select one 2D symbol in this subset.

The obtained PHY frame of 512 DSQ128 symbols is passed on to the PMA as PMA_UNITDATA.request. The PMA transmits the DSQ128 symbols over the four wire pairs in the form of 256 constituent PAM16 symbols per pair.

In the receive direction, in normal mode, the PCS processes code-groups received from the remote PHY via the PMA in 256 4D symbol blocks and maps them to the 25GMII/XLGMII service interface in the receive path. In this receive processing scheme, symbol clock synchronization is done by the PMA Receive function.

For 25GBASE-T, the signals provided by the PCS at the 25GMII conform to the interface requirements of Clause 106. For 40GBASE-T, the signals provided by the PCS at the XLGMII conform to the interface requirements of Clause 81.

[188]The resulting checkerboard constellation is based on a lattice called RZ^2 in the literature (see Forney [B25]).

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Details of the PCS functions and state diagrams are covered in 113.3. The interface to the PMA is an abstract message-passing interface specified in 113.2.

113.1.3.2 Summary of Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto the balanced cabling physical medium via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions. The PMA provides full duplex communications at $3200 \times S$ MBd over four pairs of balanced cabling up to 30 m in length.

The PMA Transmit function comprises four transmitters to generate continuous time analog signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD, as described in 113.4.3.1. In normal mode, each four-dimensional (4D) symbol received from the PCS Transmit function undergoes multiple stages of processing. First the symbol goes through a Tomlinson-Harashima precoder (THP), which maps the PAM16 input (as described in 113.3.2.2.20) in each dimension of the four-dimensional symbol into a quasi-continuous discrete-time value in the range $-16 \le x < 16$. This THP-processed four-dimensional symbol stream may be further processed by a digital transmit filter and is then passed on to four digital to analog converters (DACs). The DAC outputs may be further processed with continuous time filters to roll off the high-frequency spectral response to limit high-frequency emissions and are then applied to each of the four balanced pairs via the MDI port.

The PMA Receive function comprises four independent receivers for pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD, as described in 113.4.3.2. The receivers are responsible for acquiring symbol timing and, when operating in normal mode, for canceling echo, near-end crosstalk, far-end crosstalk, and equalizing the signal. The 4D symbols are provided to the PCS Receive function via the PMA_UNITDATA.indication message. The PMA also contains functions for Link Monitor.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control begins following the completion of Auto-Negotiation and provides the startup functions required for successful 25GBASE-T or 40GBASE-T operation. It determines whether the PHY operates in a normal mode, enabling data transmission over the link segment, or in training mode, in which it sends and receives special PAM2 code-groups and data transmission is disabled.

PMA functions and state diagrams are specified in 113.4. PMA electrical specifications are given in 113.5.

The PMA sublayer may also support a fast retrain function. The fast retrain function is specified in 113.4.2.5.16.

113.1.3.3 Summary of EEE capability

A 25GBASE-T or 40GBASE-T PHY may optionally support the EEE capability, as described in 78.1.4. The EEE capability is a mechanism by which 25GBASE-T and 40GBASE-T PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter this mode of operation after reaching PCS data mode. Each direction of the full duplex link is able to enter and exit the LPI mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full duplex link is in a period of low utilization. No data frames are lost or corrupted during the transition to or from the LPI mode.

In the transmit direction the transition to the LPI transmit mode begins when the PCS transmit function detects an LPI control character in all eight lanes of one transfer of TXD[63:0] that will be mapped into a single 64B/65B block, according to the position in the 25G/40GBASE-T LDPC frame. Following this event a sleep signal is transmitted by the PMA. The sleep signal is composed of LDPC frames that contain only LP_IDLE 512B/513B and 64B/65B blocks. The sleep signal indicates to the link partner that the transmit function of the PHY is entering the LPI transmit mode. Immediately after the transmission of the sleep

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frames, the transmit function of the local PHY enters the LPI transmit mode. While the transmit function is in the LPI mode the PHY may disable data path and control logic to save additional power. Periodically the transmit function of the local PHY transmits refresh frames that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity. The LPI mode begins with quiet signaling or with a full refresh period. Partial refreshes (defined as a refresh signal shorter than 6 LDPC frames) that immediately follow the transition to the LPI mode are replaced with quiet signaling. The quiet-refresh cycle continues until the PCS function detects IDLE characters on the 25GMII/XLGMII. These characters signal to the PHY that the LPI transmit mode should end. The PMA Transmit function in the PHY then sends an alert message to the link partner. The alert signal begins on a LDPC frame boundary, but has no fixed relationship to the quiet-refresh cycle. The alert signal wakes the link partner from sleep. The alert signal is followed by a wake signal, composed of LDPC frames containing only IDLE 512B/513B and 64B/65B blocks. After a short recovery time the normal operational mode is resumed.

In the receive direction the transition to the LPI mode is triggered when the PCS Receive function detects LPI control characters within received LDPC frames. This indicates that the link partner is about to enter the LPI transmit mode. Following these frames the link partner ceases transmission and begins quiet-refresh signaling. During the quiet time it is highly recommended that the local receiver power off circuits to reduce power consumption. Periodically the link partner transmits refresh frames that are used by the receiver to update adaptive coefficients and timing circuits. This quiet-refresh cycle continues until the link partner transmits the alert signal, initiating a transition back to the normal operational mode. The alert signal is detected in the PMA and signals that normal data frames will follow. The alert signal is followed by a wake signal that allows the local receiver time to prepare for the normal operational mode. The wake signal is composed of repeated IDLE 512B/513B and 64B/65B blocks. After a short recovery time the normal operational mode is resumed.

Support for the EEE capability is advertised in the Infofield (Octet 12 bit 7) during link startup. Transitions to and from the LPI transmit mode are controlled via 25GMII/XLGMII signaling. Transitions to and from the LPI receive mode are controlled by the link partner using sleep, alert, and wake signaling.

The PCS 64B/65B Transmit state diagram in Figure 113–18a and Figure 113–18b includes additional states for EEE. The PCS 64B/65B Receive state diagram in Figure 113–19a and Figure 113–19b includes additional states for EEE. The EEE Transmit state diagram is contained in the PCS Transmit function and is specified in Figure 113–20.

113.1.4 Signaling

25GBASE-T and 40GBASE-T signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over each wire pair. The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> for 25GBASE-T, or TXD<63:0> and TXC<7:0> for 40GBASE-T, to four-dimensional symbols in the transmit path.
c) Algorithmic mapping from the received four-dimensional signals on the MDI port to RXD<31:0> and RXC<3:0> for 25GBASE-T on the 25GMII interface, or RXD<63:0> and RXC<7:0> for 40GBASE-T on the XLGMII interface.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions on any pair combination.
f) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
g) Block framing and other control signals.
h) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
i) Ability to automatically detect and correct for pair swapping and crossover connections.
j) Ability to automatically detect and correct for incorrect polarity in the connections.

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k) Ability to automatically correct for differential delay variations across the wire pairs.
l) Ability to support refresh, quiet and alert signaling during LPI operation.

The PHY operates in two modes—normal mode or training mode. In normal mode, PCS generates a continuous stream of four-dimensional symbols that are transmitted via the PMA at one of eight power levels. In training mode, the PCS is directed to generate only PAM2 symbols for transmission by the PMA, which enable the receiver at the other end to train until it is ready to operate in normal mode. (See Figure 113–5.)

PHYs may also support the EEE capability as described in 113.1.3.3. Transitions to the LPI mode are supported after reaching normal mode.

113.1.5 Interfaces

All 25GBASE-T and 40GBASE-T PHY implementations are compatible at the MDI, and at the 25GMII/XLGMII, if implemented. Implementation of the 25GMII/XLGMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and 25GMII/XLGMII (if the 25GMII/XLGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the 25GMII/XLGMII is implemented or not.

113.1.6 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

Default initializations, unless specified, are left to the implementer.

113.2 25GBASE-T and 40GBASE-T service primitives and interfaces

25GBASE-T transfers data and control information across the following four service interfaces:

a) 25 Gb/s Media Independent Interface (25GMII)
b) Technology Dependent Interface
c) PMA service interface
d) Medium dependent interface (MDI)

The 25GMII is specified in Clause 106; the Technology Dependent Interface is specified in Clause 28. The PMA service interface is defined in 113.2.2 and the MDI is defined in 113.8.

40GBASE-T transfers data and control information across the following four service interfaces:

a1) 40 Gb/s Media Independent Interface (XLGMII)
b1) Technology Dependent Interface
c1) PMA service interface
d1) Medium dependent interface (MDI)

The XLGMII is specified in Clause 81; the Technology Dependent Interface is specified in Clause 28. The PMA service interface is defined in 113.2.2 and the MDI is defined in 113.8.

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113.2.1 Technology Dependent Interface

25G/40GBASE-T use the following service primitives to exchange status indications and control signals across the Technology Dependent Interface as specified in Clause 28:

PMA_LINK.request (link_control)

PMA_LINK.indication (link_status)

113.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation algorithm to enable and disable operation of the PMA as specified in 28.2.6.2.

113.2.1.1.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PMA reports link_status=FAIL. PHY processes are disabled.
DISABLE	Set by the Auto-Negotiation algorithm in the event fast link pulses are detected. PHY processes are disabled. This allows the Auto-Negotiation algorithm to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions.

113.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in Clause 28.

113.2.1.1.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as defined in 113.4.2.6.

113.2.1.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 28.2.6.1. This primitive informs the Auto-Negotiation algorithm about the status of the underlying link.

113.2.1.2.1 Semantics of the primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on one of the following two values: FAIL or OK.

FAIL	No valid link established.
OK	The Link Monitor function indicates that a valid 25G/40GBASE-T link is established. Reliable reception of signals transmitted from the remote PHY is possible.

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113.2.1.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 113–31.

113.2.1.2.3 Effect of receipt

Auto-Negotiation uses this primitive to detect a change in link_status as described in Clause 28.

113.2.2 PMA service interface

25G/40GBASE-T use the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication (tx_mode)

PMA_CONFIG.indication (config)

PMA_UNITDATA.request (tx_symb_vector)

PMA_UNITDATA.indication (rx_symb_vector)

PMA_SCRSTATUS.request (scr_status)

PMA_PCSSTATUS.request (pcs_status)

PMA_RXSTATUS.indication (loc_rcvr_status)

PMA_REMRXSTATUS.request (rem_rcvr_status)

EEE-capable PHYs additionally support the following service primitives:

PMA_ALERTDETECT.indication (alert_detect)

PCS_RX_LPI_STATUS.request (rx_lpi_active)

PMA_PCSDATAMODE.indication (PCS_data_mode)

Fast retrain capable PHYs additionally support the following service primitive:

PMA_FR_ACTIVE.indication (fr_active)

The use of these primitives is illustrated in Figure 113–4. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 113–4.

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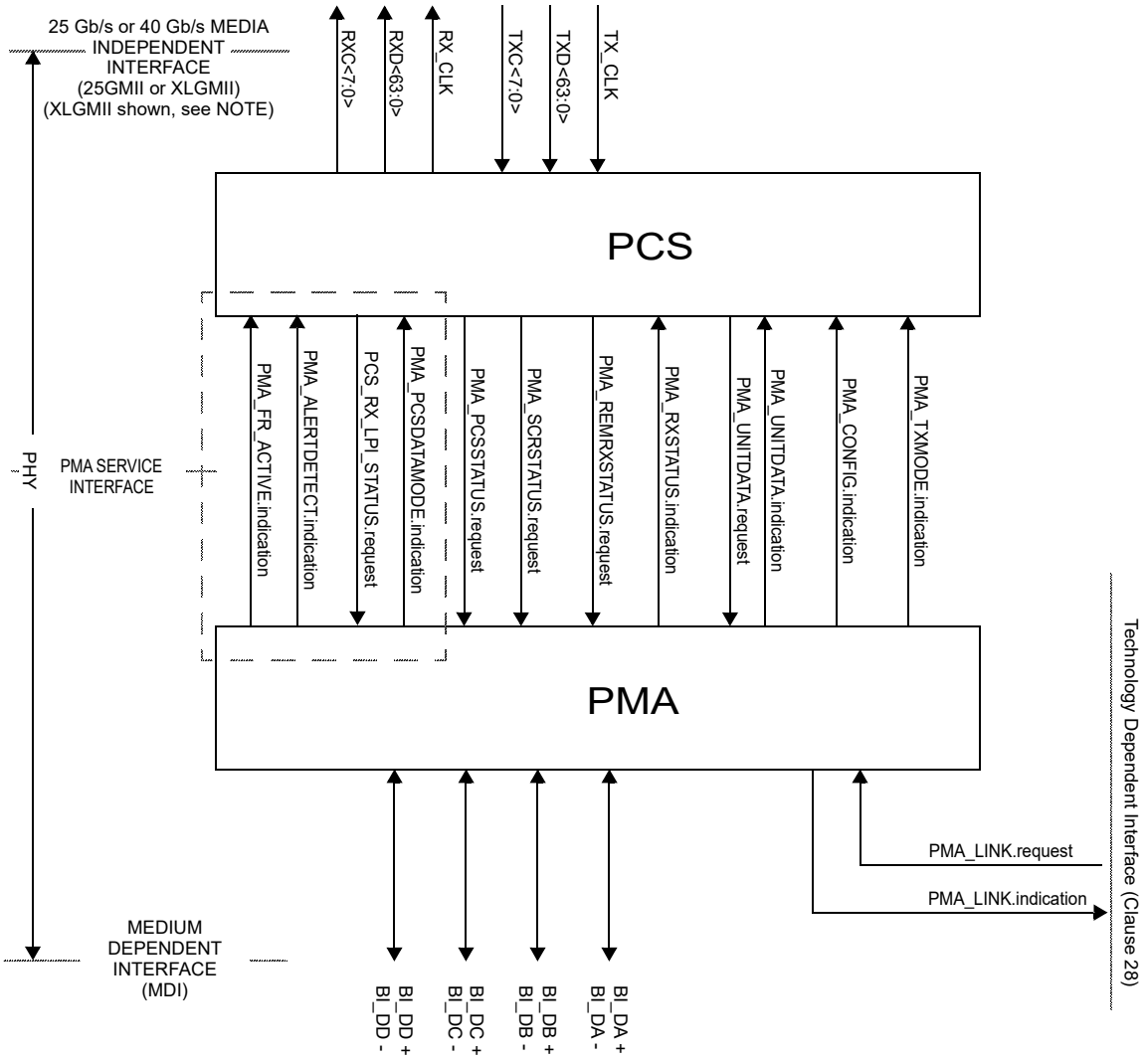

NOTE—
PMA_PCSDATAMODE.indication is required only for the EEE or fast retrain capabilities.
PMA_ALERTDETECT.indication and PCS_RX_LPI_STATUS.request are only required for the EEE capability.
PMA_FR_ACTIVE.indication is only required for the fast retrain capability.
Word widths for only the 40 Gb/s Media Independent Interface (XLGMII) are shown for clarity. For the 25 Gb/s Media Independent Interface, a four-bit control word and 32-bit data word are used, i.e., RXC<3:0>, RXD<31:0>, TXC<3:0>, and TXD<31:0>.

Figure 113–4—25GBASE-T and 40GBASE-T service interfaces

113.2.2.1 PMA_TXMODE.indication

The transmitter in a 25G/40GBASE-T link normally sends over the four pairs, four-dimensional symbols that represent a 25GMII/XLGMII data stream with framing, scrambling and encoding of data, control information, or idles.

113.2.2.1.1 Semantics of the primitive

PMA_TXMODE.indication (tx_mode)

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PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of code-groups the PCS should be transmitting. The parameter tx_mode can take on one of the following three values of the form:

SEND_N	This value is continuously asserted when transmission of sequences of four-dimensional symbols representing a 25GMII/XLGMII data stream in normal mode.
SEND_T	This value is continuously asserted in case transmission of sequences of code-groups representing the training mode is to take place.
SEND_Z	This value is continuously asserted in case transmission of zeros is required.

113.2.2.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

113.2.2.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 113.3.2.2.

113.2.2.2 PMA_CONFIG.indication

Each PHY in a 25G/40GBASE-T link is capable of operating as a MASTER PHY and as a SLAVE PHY. MASTER-SLAVE configuration is determined during Auto-Negotiation (113.6.1). The result of this negotiation is provided to the PMA.

113.2.2.2.1 Semantics of the primitive

PMA_CONFIG.indication (config)

PMA_CONFIG.indication specifies to PCS and PMA Transmit via the parameter config whether the PHY operates as a MASTER PHY or as a SLAVE PHY. The parameter config can take on one of the following two values of the form:

MASTER	This value is continuously asserted when the PHY operates as a MASTER PHY.
SLAVE	This value is continuously asserted when the PHY operates as a SLAVE PHY.

113.2.2.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in config.

113.2.2.2.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter config.

113.2.2.3 PMA_UNITDATA.request

This primitive defines the transfer of code-groups in the form of the tx_symb_vector parameter from the PCS to the PMA. The code-groups are obtained in the PCS Transmit function using the encoding rules defined in 113.3.2.2 to represent 25GMII/XLGMII data and control streams or other sequences.

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113.2.2.3.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. For EEE-capable PHYs, the vector also requests the PMA to send the ALERT signal during LPI. The tx_symb_vector parameter takes on the form:

SYMB_4D	A vector of four multi-level symbols, one for each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. In normal operation, each symbol takes on one of the values in the set {–15, –13, –11, –9, –7, –5, –3, –1, 1, 3, 5, 7, 9, 11, 13, 15}. The symbols additionally take the value 0 when zeros are to be transmitted in the following two cases: 1) when PMA_TXMODE.indication is SEND_Z during PMA training, and 2) after data mode is reached, the transmit function is in the LPI transmit mode and lpi_tx_mode is QUIET
ALERT	A vector used to indicate that the PMA should transmit the alert sequence. ALERT is asserted for a time equal to 4 LDPC frames.

The symbols that are elements of tx_symb_vector are called, according to the pair on which each is transmitted, tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD].

113.2.2.3.2 When generated

The PCS generates PMA_UNITDATA.request synchronously with every transmit clock cycle.

113.2.2.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols after processing with the THP, the transmit filter and other specified PMA Transmit processing. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD for cancelling the echo and near-end crosstalk (NEXT).

113.2.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of code-groups in the form of the rx_symb_vector parameter from the PMA to the PCS.

113.2.2.4.1 Semantics of the primitive

PMA_UNITDATA.indication (rx_symb_vector)

During reception the PMA_UNITDATA.indication simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on each of the four receive pairs BI_DA, BI_DB, BI_DC, and BI_DD. The rx_symb_vector parameter takes on the form:

SYMB_4D	A vector of the four 1D symbols that is the receiver's best estimate of the symbols that were sent by the remote transmitter across the four pairs with reliability measures.

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113.2.2.4.2 When generated

The PMA generates PMA_UNITDATA.indication (SYMB_4D) messages synchronously every four symbols received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is $3200 \times S$ MHz, as governed by the recovered clock.

113.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

113.2.2.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the training mode descrambler has achieved synchronization.

113.2.2.5.1 Semantics of the primitive

PMA_SCRSTATUS.request (scr_status)

The scr_status parameter can take on one of the following two values of the form:

OK	The training mode descrambler has achieved synchronization.
NOT_OK	The training mode descrambler is not synchronized.

113.2.2.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

113.2.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 113.4.2.4, 113.4.2.5, and 113.4.6.1.

113.2.2.6 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in data mode.

113.2.2.6.1 Semantics of the primitive

PMA_PCSSTATUS.request (pcs_status)

The pcs_status parameter can take on one of the following two values of the form:

OK	The PCS is operating reliably in data mode.
NOT_OK	The PCS is not operating reliably in data mode.

113.2.2.6.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

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113.2.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 113.4.6.

113.2.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol streams.

113.2.2.7.1 Semantics of the primitive

PMA_RXSTATUS.indication (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of the following two values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

113.2.2.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

113.2.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 113–28 and in 113.2 and 113.4.6.3.

113.2.2.8 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The criterion for setting the parameter rem_rcvr_status is left to the implementer. It can be based, for example, on asserting rem_rcvr_status is NOT_OK until loc_rcvr_status is OK and then asserting the detected value of rem_rcvr_status after proper PCS Receive decoding is achieved.

113.2.2.8.1 Semantics of the primitive

PMA_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of the following two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

113.2.2.8.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages to indicate a change in rem_rcvr_status on the basis of signals received at the MDI.

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113.2.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 113–28.

113.2.2.9 PMA_ALERTDETECT.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY when rx_lpi_active is TRUE. The parameter alert_detect conveys to the PCS receive function information regarding the detection of the LPI alert signal by the PMA receive function. The criterion for setting the parameter alert_detect is left to the implementer.

113.2.2.9.1 Semantics of the primitive

PMA_ALERTDETECT.indication (alert_detect)

The alert_detect parameter can take on one of the following two values of the form:

TRUE	The alert signal has been reliably detected at the local receiver.
FALSE	The alert signal at the local receiver has not been detected.

113.2.2.9.2 When generated

The PMA generates PMA_ALERTDETECT.indication messages to indicate a change in the alert_detect status.

113.2.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in 113.3.2.3, Figure 113–19a, and Figure 113–19b.

113.2.2.10 PCS_RX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS receive function to indicate the status of the receive link at the local PHY. The parameter PCS_RX_LPI_STATUS.request conveys to the PCS transmit and PMA receive functions information regarding whether the receive function is in the LPI receive mode. The parameter is generated by the Receive 64B/65B state diagram in Figure 113–19a.

113.2.2.10.1 Semantics of the primitive

PCS_RX_LPI_STATUS.request (rx_lpi_active)

The rx_lpi_active parameter can take on one of the following two values of the form:

TRUE	The receive function is in the LPI receive mode.
FALSE	The receive function is not in the LPI receive mode.

113.2.2.10.2 When generated

The PCS generates PCS_RX_LPI_STATUS.request messages to indicate a change in the rx_lpi_active variable as determined by the receive state diagram in Figure 113–19a.

113.2.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in 113.3.2.3 and Figure 113–32.

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113.2.2.11 PMA_PCSDATAMODE.indication

This primitive indicates whether or not the PCS state diagrams are able to transition from their initialization states. The pcs_data_mode variable is generated by the PMA PHY Control function. It is passed to the PCS Control function via the PMA_PCSDATAMODE.indication primitive.

113.2.2.11.1 Semantics of the primitive

PMA_PCSDATAMODE.indication (pcs_data_mode)

The pcs_data_mode parameter can take on one of the following two values of the form:

TRUE	PHY is in state PCS_Data (see Figure 113–28)
FALSE	PCS is not in state PCS_Data (see Figure 113–28)

113.2.2.11.2 When generated

The PMA PHY Control function generates PMA_PCSDATAMODE.indication messages continuously.

113.2.2.11.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 113.3.2.2.

113.2.2.12 PMA_FR_ACTIVE.indication

This primitive indicates whether or not the PMA is currently performing a fast retrain. The fr_active variable is generated by the PMA PHY Control function. It is passed to the PCS Receive Control function via the PMA_FR_ACTIVE.indication primitive. This primitive is only supported by PHYs with the fast retrain capability.

113.2.2.12.1 Semantics of the primitive

PMA_FR_ACTIVE.indication (fr_active)

The fr_active parameter can take on one of the following two values of the form:

TRUE	PHY is currently performing a fast retrain
FALSE	PCS is not currently performing a fast retrain

113.2.2.12.2 When generated

The PMA PHY Control function generates PMA_FR_ACTIVE.indication messages continuously.

113.2.2.12.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 113–19a.

113.3 Physical Coding Sublayer (PCS)

113.3.1 PCS service interface (25GMII/XLGMII)

The PCS service interface allows the 25G/40GBASE-T PCS to transfer information to and from a PCS client. The PCS Interface is precisely defined for 25GBASE-T as the 25 Gb/s Media Independent Interface

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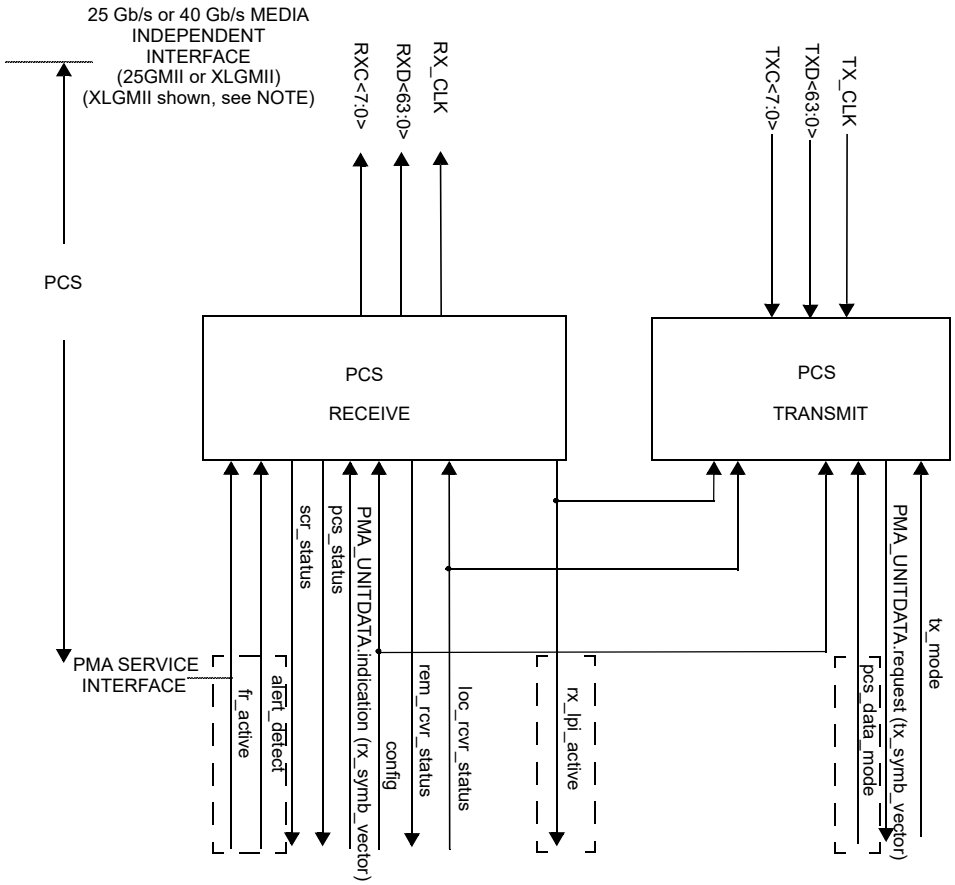
(25GMII) in Clause 106, and, for 40GBASE-T, the 40 Gb/s Media Independent Interface (XLGMII) in Clause 81.

113.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 113–5, shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 113–5.



NOTE—
pcs_data_mode is required only for the EEE or fast retrain capabilities.
alert_detect and rx_lpi_active are only required for the EEE capability.
fr_active is only required for the fast retrain capability.
Word widths for only the 40 Gb/s Media Independent Interface (XLGMII) are shown for clarity. For the 25 Gb/s Media Independent Interface, a four-bit control word and 32-bit data word are used, i.e., RXC<3:0>, RXD<31:0>, TXC<3:0>, and TXD<31:0>.

Figure 113–5—PCS reference diagram

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113.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 113.3.6.2.2).
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset = true while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

113.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 113–18a and Figure 113–18b, and to the PCS Transmit bit ordering in Figure 113–6 and Figure 113–8.

Dashed rectangles in Figure 113–18a and Figure 113–18b are used to indicate states and state transitions in the transmit process state diagram that shall be supported by PHYs with the EEE capability. PHYs without the EEE capability do not support these transitions.

When communicating with the 25GMII, the 25GBASE-T PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. When communicating with the XLGMII, the 40GBASE-T PCS uses a eight octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment to 64B/65B is performed in the PCS. The PMA sublayer operates independently of block and packet boundaries. The PCS provides the functions necessary to map packets between the 25GMII/XLGMII format and the PMA service interface format.

When the transmitter is in normal mode, the PCS Transmit process continuously generates 65B blocks based upon the TXD <31:0> and TXC <3:0> signals on the 25GMII for 25GBASE-T, or the TXD <63:0> and TXC <7:0> signals on the XLGMII for 40GBASE-T. The subsequent functions of the PCS Transmit process then transcode the first 96 25GMII transfers for 25GBASE-T, or 48 XLGMII transfers for 40GBASE-T into 512B/513B blocks, append the subsequent four 25GMII transfers (25GBASE-T), or two XLGMII transfers (40GBASE-T) as (non-transcoded) 64B/65B blocks, scramble the bits, pack the resulting blocks, appending an unscrambled auxiliary bit, and split the bits into two sets. The first set is encoded by a Reed-Solomon encoder, and the second set is processed by a low density parity check (LDPC) encoder and then the two sets are joint mapped into a transmit LDPC frame of DSQ128 symbols. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a code-group (A_n, B_n, C_n, D_n) that is transferred to the PMA via the PMA_UNITDATA.request primitive. The PMA transmits symbols A_n, B_n, C_n, D_n over wire pairs BI_DA, BI_DB, BI_DC, and BI_DD, respectively. The integer, n, is a time index that is introduced to establish a temporal relationship between different symbol periods. A symbol period, T, is 312.5/S ps.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate sequences of code-groups (TA_n, TB_n, TC_n, TD_n) defined in 113.3.4.2 to the PMA via the PMA_UNITDATA.request primitive. These code-groups are used for training mode and only transmit the values {–9, 9} to keep the transmit power in the training mode the same as the transmit power in normal mode.

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During training mode an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes requests for remote transmitter settings. (See 113.4.2.5.)

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the normal mode of operation, and the PCS Transmit function shall use a 65B coding technique, transcoded to a mixed 513B-65B-RS-FEC-LDPC encoding to generate at each symbol period code-groups that represent data or control. During transmission, the six blocks of 513B transcoded bits and the two blocks of 65B encoded bits are scrambled by the PCS using a PCS scrambler and an auxiliary bit is added, then frames are encoded into a code-group of four-dimensional symbols and transferred to the PMA. During data encoding, PCS Transmit utilizes a Reed Solomon encoder to generate 3x512 bits and an LDPC frame encoder for the remaining 4x512 bits.

After reaching the normal mode of operation, EEE-capable PHYs may enter the LPI transmit mode under the control of the MAC via the 25GMII/XLGMII. The EEE Transmit state diagram is contained within the PCS Transmit function. The EEE capability is described in 113.3.2.2.23.

113.3.2.2.1 Use of blocks

The PCS maps 25GMII/XLGMII signals into 65-bit blocks inserted into an LDPC frame, and vice versa, using a 65B-LDPC coding scheme. The PAM2 PMA training frame synchronization allow establishment of LDPC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. During the LPI mode, LDPC frame boundaries delimit sleep, wake, refresh, quiet, and alert cycles. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 113.3.2.2.2.

113.3.2.2.2 65B-LDPC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters. In addition, the code enables the receiver to achieve PCS synchronization alignment on the incoming PHY bit stream.

The relationship of block bit positions to 25GMII/XLGMII, PMA, and other PCS constructs is illustrated in Figure 113–6 for transmit and Figure 113–7 for receive. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 113.3.2.2.5 for information on how blocks containing control characters are mapped.

113.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D0 to D7. Control characters other than /O/, /S/ and /T/ are labeled C0 to C7. The control character for ordered set is labeled as O0 or O4 since it is only valid on the first octet of the 25GMII/XLGMII. The control character for start is labeled as S0 or S4 for the same reason. The control character for terminate is labeled as T0 to T7.

For 25GBASE-T, two 25GMII transfers or, for 40GBASE-T, a single XLGMII transfer provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the 25GMII/XLGMII transfer(s).

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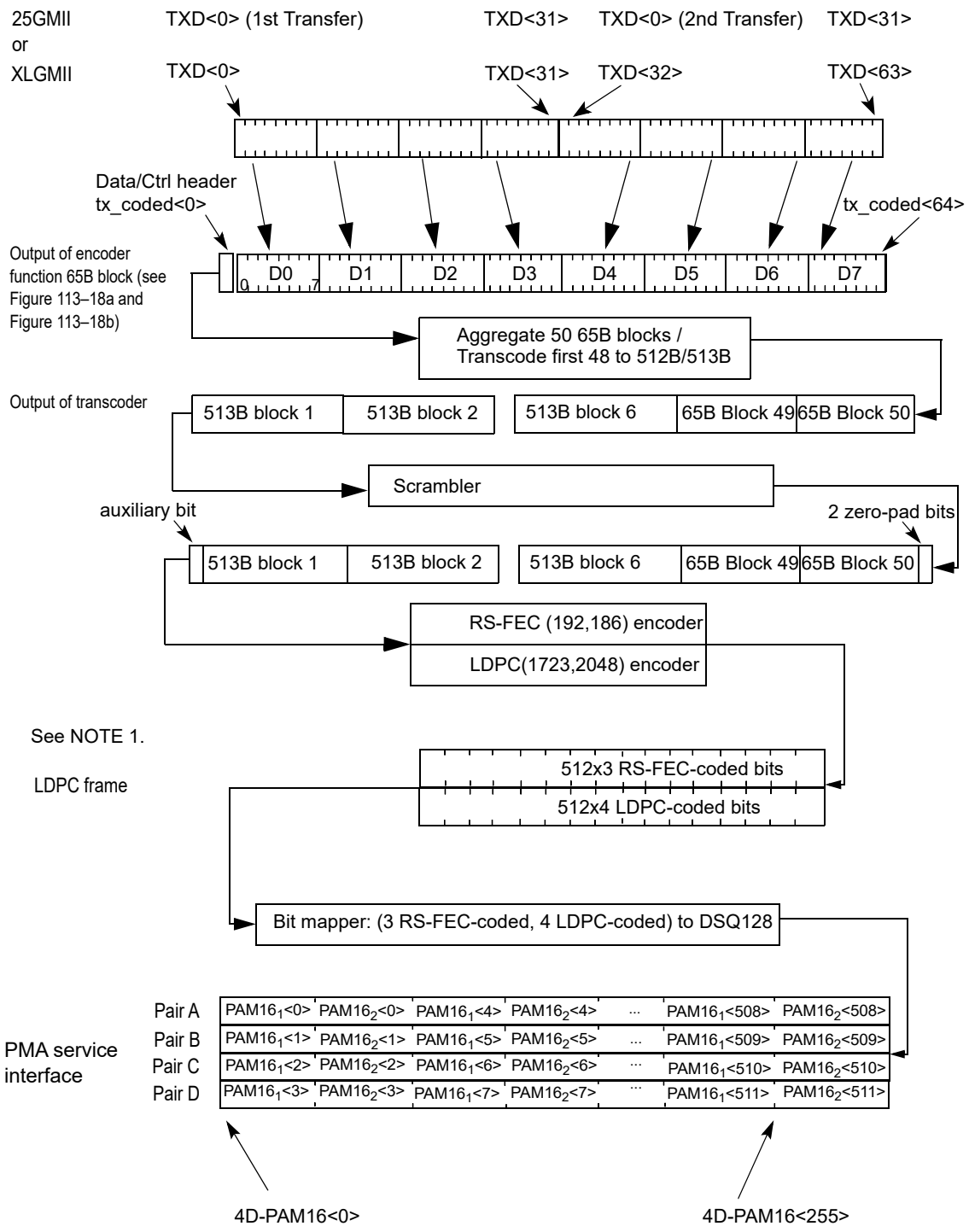

NOTE 1—Zero-pad replaced with random bits for transmission.

NOTE 2—This figure shows the mapping from the 25GMII/XLGMII to a 64B/65B block for a block containing eight data characters.

Figure 113–6—PCS Transmit bit ordering

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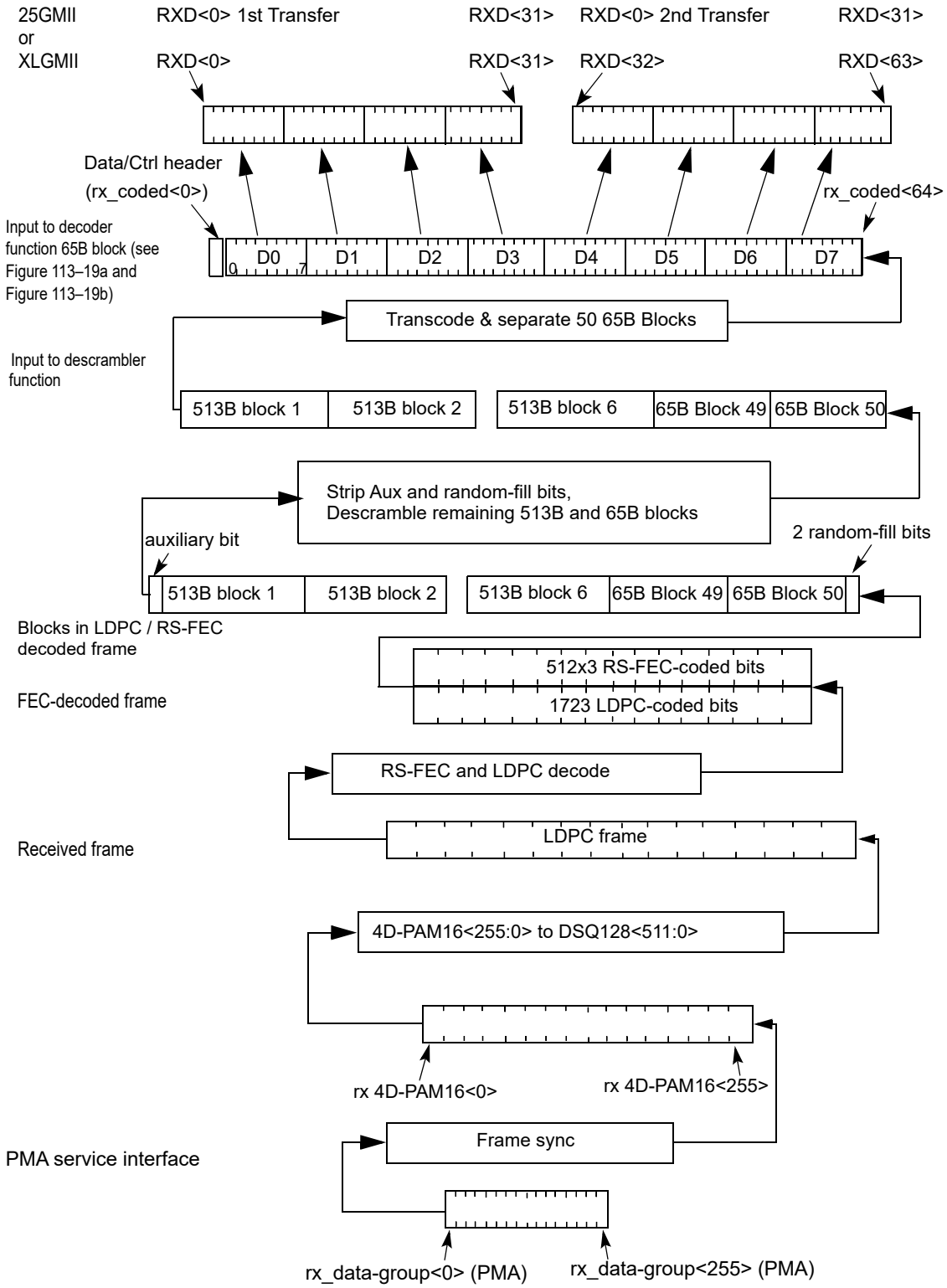

NOTE—This figure shows the mapping from a 64B/65B block a block containing eight data characters to the 25GMII/XLGMII.

Figure 113–7—PCS Receive bit ordering

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Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled TxB<31:0> and RxB<31:0> for 25GBASE-T, or TxB<64:0> and RxB<64:0> for 40GBASE-T, respectively where TxB<0> and RxB<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

113.3.2.2.4 Transmission order

The PCS Transmit bit ordering is shown in Figure 113–6 and Figure 113–8. Note that Figure 113–6 shows the mapping from the 25GMII/XLGMII to a 64B/65B block for a block containing eight data characters.

113.3.2.2.5 Block structure

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an eight-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that character is implied by the block type field. Other control characters are encoded in a seven-bit control code or a four-bit O Code. Each control block contains eight characters.

The format of the blocks for 25GBASE-T is as shown in Figure 113–9. The format of the blocks for 40GBASE-T is as shown in Figure 113–10. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the 25GMII/XLGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the Input Data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt..

Bits and field positions are shown with the least significant bit on the left. Hexadecimal numbers are shown prepended with ‘0x’, and with the least significant digit on the right. For example the block type field 0x1E is sent as 01111000 representing bits 1 through 8 of the 65-bit block. The least significant bit for each field is placed in the lowest numbered position of the field.

All unused values of block type field are reserved.[189]

113.3.2.2.6 Control codes

The same set of control characters are supported by the 25GMII/XLGMII and the 25G/40GBASE-T PCS. The representations of the control characters are the control codes. The 25GMII/XLGMII encodes a control character into an octet (an eight-bit value). The 25G/40GBASE-T PCS encodes the start and terminate control characters implicitly by the block type field. The 25G/40GBASE-T PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The 25G/40GBASE-T PCS encodes each of the other control characters into a seven-bit C code.

[189]The block type field values have been chosen to have a four-bit Hamming distance between them. The only unused value that maintains the Hamming distance is 0x00.

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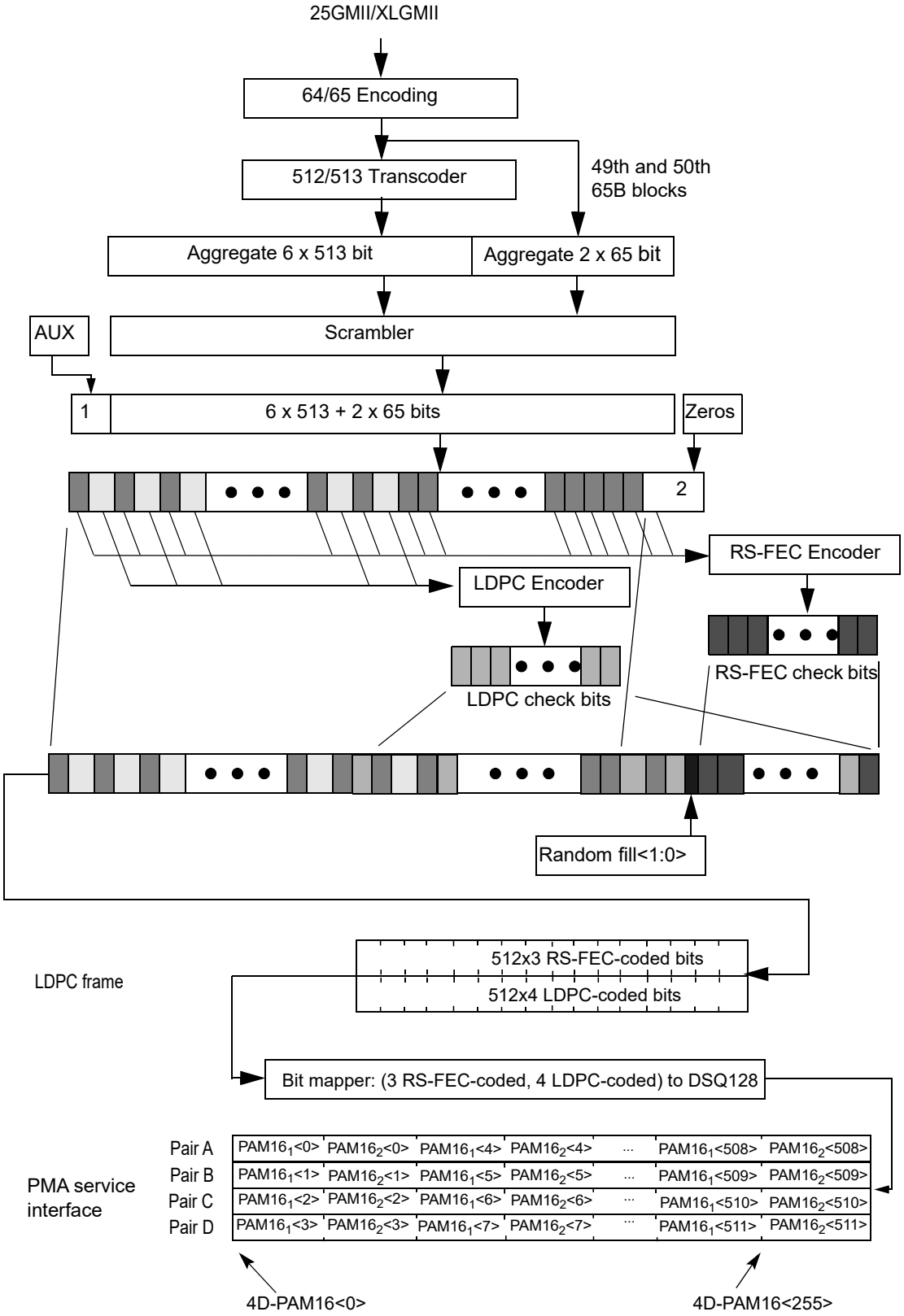

Figure 113–8—PCS detailed transmit bit ordering

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Input Data	data ctrl header	Block Payload							
Bit Position: / Data Block Format:	0	1							64
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 113–9—64B/65B block formats for 25GBASE-T

The control characters and their mappings to 25G/40GBASE-T control codes and 25GMII/XLGMII control codes are specified in Table 113–1 for 25GBASE-T and Table 113–2 for 40GBASE-T. All 25GMII/XLGMII and 25G/40GBASE-T control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

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Input Data	data ctrl header	Block Payload							
Bit Position: / Data Block Format:	0	1							64
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
$C_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$S_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,D_7$	1	0x78	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$O_0\,D_1\,D_2\,D_3/Z_4\,Z_5\,Z_6\,Z_7$	1	0x4B	D_1	D_2	D_3	O_0	0x000_0000		
$T_0\,C_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,T_1\,C_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,T_2\,C_3/C_4\,C_5\,C_6\,C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,T_3/C_4\,C_5\,C_6\,C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/T_4\,C_5\,C_6\,C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,T_5\,C_6\,C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,T_6\,C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\,D_1\,D_2\,D_3/D_4\,D_5\,D_6\,T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 113–10—64B/65B block formats for 40GBASE-T

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Table 113–1—Control codes for 25GBASE-T

Control character	Notation	25GMII control code	25GBASE-T control code	25GBASE-T O code
idle	/I/	0x07	0x00	
LPI	/LI/	0x06	0x06	
start	/S/	0xFB	Encoded by block type field	
terminate	/T/	0xFD	Encoded by block type field	
error	/E/	0xFE	0x1E	
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0
reserved0		0x1C	0x2D	reserved0
reserved1		0x3C	0x33	reserved1
reserved2		0x7C	0x4B	reserved2
reserved3		0xBC	0x55	reserved3
reserved4		0xDC	0x66	reserved4
reserved5		0xF7	0x78	reserved5
Signal ordered set[a]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF

[a]Used by INCITS T11 Fibre Channel.

Table 113–2—Control codes for 40GBASE-T

Control character	Notation	XLGMII control code	40GBASE-T control code	40GBASE-T O code
idle	/I/	0x07	0x00	
LPI[a]	/LI/	0x06	0x06	
start	/S/	0xFB	Encoded by block type field	
terminate	/T/	0xFD	Encoded by block type field	

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Table 113–2—Control codes for 40GBASE-T *(continued)*

Control character	Notation	XLGMII control code	40GBASE-T control code	40GBASE-T O code
error	/E/	0xFE	0x1E	
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0
Signal ordered set[b]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF

[a]Use of idle and LPI ordered sets per 81.3.
[b]Used by INCITS T11 Fibre Channel.

113.3.2.2.7 Ordered sets

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and local fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the 25GMII or XLGMII. 25 Gigabit and 40 Gigabit Ethernet use one kind of ordered set: the sequence ordered set (see 81.3.4). The sequence ordered set control character is denoted /Q/. An additional ordered set, the signal ordered set, is defined and it begins with another control code. The four-bit O field encodes the control code. See Table 113–1 for the mappings for 25GBASE-T, and Table 113–2 for the mappings for 40GBASE-T.

113.3.2.2.8 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the 25GMII/XLGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

113.3.2.2.9 LPI (/LI/)

Low power idle (LPI) control characters (/LI/) on the 25GMII/XLGMII indicate that the LPI client is requesting operation in the LPI transmit mode. A continuous stream of LPI control characters (/LI/) is used to maintain a link in the LPI transmit mode. Idle control characters (/I/) are used to transition from the LPI transmit mode to the normal mode. PHYs that support EEE respond to the LPI 25GMII/XLGMII control characters using the procedure outlined in 113.1.3.3. LPI characters may be added or deleted by the PCS to adapt between clock rates. /LI/ insertion and deletion shall occur in groups of four. /LI/s may be added following low power idle characters. They shall not be added while data is being received.

If EEE is not supported, then /LI/ is not a valid control character.

113.3.2.2.10 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the 25GMII (TXD<7:0> and RXD<7:0>), or XLGMII (TXD<7:0> and RXD<7:0>). Receipt of an /S/ on any other octet of TXD indicates an error. For 25 Gb/s and 40 Gb/s transmission, block type field values implicitly encode an /S/ as the first character of the block. These are the only characters of a block on which a start can occur.

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113.3.2.2.11 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the 25GMII/XLGMII interface and within any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

113.3.2.2.12 ordered set (/O/)

The ordered set control characters (/O/) indicate the start of an ordered set. There are two kinds of ordered sets: the sequence ordered set and the signal ordered set. When it is necessary to designate the control character for the sequence ordered set specifically, /Q/ is used. /O/ is only valid on the first octet of the 25GMII/XLGMII. Receipt of an /O/ on any other octet of TXD indicates an error. For 40 Gb/s transmission, block type field values implicitly encode an /O/ as the first character of the block. The four-bit O code encodes the specific /O/ character for the ordered set.

Sequence ordered sets may be deleted by the PCS to adapt between clock rates. Such deletion shall only occur when two consecutive sequence ordered sets have been received and shall delete only one of the two. Only Idles may be inserted for clock compensation. Signal ordered sets are not deleted for clock compensation.

113.3.2.2.13 Error (/E/)

The /E/ is sent whenever an /E/ is received. The /E/ allows physical sublayers such as the PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 113.3.6.2.4 for further information.

113.3.2.2.14 Transmit process

The transmit process generates blocks based upon the TXD and TXC signals received from the 25GMII/XLGMII. 100 25GMII or 50 XLGMII data transfers are encoded into an LDPC frame. It takes 256 PMA_UNITDATA transfers to send an LDPC frame of data. Therefore, for 25GBASE-T, if the PCS is connected to a 25GMII and PMA sublayer where the ratio of their transfer rates is exactly 25:64, or, for 40GBASE-T, an XLGMII and PMA sublayer where the ratio of their transfer rates is exactly 25:128, then the transmit process does not need to perform rate adaptation. Where the 25GMII or XLGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 113–18a and Figure 113–18b). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the transcoder/ scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

113.3.2.2.15 64B/65B to 512B/513B Transcoder

The 513B transcoder constructs a 513-bit block tx_xcoded<512:0>, from a group of eight 65-bit blocks, tx_coded_*j*<64:0> where *j*=0 to 7. For each group of eight 65-bit blocks, *j*=7 corresponds to the most recently received block. Bit 0 in each 65-bit block is the first bit received and corresponds to the data control header.

If for all *j*=0 to 7, tx_coded_*j*<0> = 0, tx_xcoded<512:0> shall be constructed as follows:

a) tx_xcoded<0>=1

b) tx_xcoded<(64*j*+64):(64*j*+1)>=tx_coded_*j*<64:1> for *j*=0 to 7.

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If for any *j*=0 to 7, tx_coded_*j*<0>=1, tx_xcoded<512:0> shall be constructed as follows:

a1) tx_xcoded<0>=0

b1) Within the group of eight 65-bit blocks, let *C* be the set of *k* integers corresponding to the values of *j* that have tx_coded_*j*<0> = 1, and *U* be the set of 8–*k* integers corresponding to the values of *j* that have tx_coded_*j*<0> = 0, where the integers that comprise both *C* and *U* are arranged in ascending order. For instance, if tx_coded_1<0>=1 and tx_coded_4<0>=1, *C* = {1,4}, and *U* = {0,2,3,5,6,7}.

c1) For the allowed set of 25GBASE-T 64B/65B or 40GBASE-T 64B/65B control codes (see Figure 113–9 and Figure 113–10), let the four-bit code shown in the rightmost column of Table 113–4 represent the Block Type for transcoding purposes.

Given this, a 513-bit block can be constructed consisting of a leading 1, followed by all of the transcoded control blocks in *C*, followed by all of the data blocks in *U*.

Table 113–3 shows the transcoding scheme. The first column represents a 513B control byte that replaces the eight-bit block type found in the 64B/65B control code, and contains 3 fields:

a2) A continuation flag (FC) that if set to 1 indicates that another control block is to follow, and if set to 0 indicates that this is the last control block in the group of 8 transcoded 65B blocks, followed by

b2) Three position bits (Position) used to indicate which of the eight 65B blocks in the transcoding group the control block came from, followed by

c2) Four block-type bits (BlockType), which contain the transcoded block type, as shown in the right-most column of Table 113–4.

The resulting translation can be represented as the 513B control byte = {FC, Position<2:0>, BlockType<3:0>}.

Table 113–3—513B Transcoded Blocks including Control blocks (without leading 0)

513B control byte	64/65B block payload
513B Control Byte C_0 (1, Position<2:0>, Block Type<3:0>)	tx_coded_C_0<9:64>
513B Control Byte C_1 (1, Position<2:0>, Block Type<3:0>)	tx_coded_C_1<9:64>
:	:
513B Control Byte C_{k-1}(0, Position <2:0>, Block Type<3:0>)	tx_coded_C_{k-1}<9:64>
tx_coded_U_0<1:8>	tx_coded_U_0<9:64>
tx_coded_U_1<1:8>	tx_coded_U_1<9:64>
:	:
tx_coded_U_{7-k}<1:8>	tx_coded_U_{7-k}<9:64>

The following examples are provided for clarity, shown in Figure 113–11.

Example #1: *C* = {1,4}, and *U* = {0,2,3,5,6,7}, with the first control block being 0x1E, and the second being 0x78. Thus:

1.1) 65B control words are present, so the 513B control flag bit gets set to 0

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Table 113–4—64B/65B Block field to BlockType<3:0> translation

Block field (see Figure 113–10)	BlockType<3:0>
0x1E	1000
0x2D	0100
0x33	1110
0x66	1101
0x55	1011
0x78	0111
0x4B	0001
0x87	1100
0x99	1010
0xAA	1001
0xB4	0101
0xCC	0011
0xD2	0110
0xE1	0000
0xFF	1111

1.2) The first control word is C_0 where Position = 0x1, and BlockType = 0x8. Since this is not the last control word the continuation flag FC = 1. Thus the 513B control word for this block is:
C_0 Control Word = {1,0x1, 0x8} = 1 100 0001 in bit order of transmission

1.3) The second control word is C_1 where Position = 0x4, and BlockType = 0x7. Since this is the last control word the continuation flag FC = 0. Thus the 513B control word for this block is:
C_4 Control Word = {0,0x4, 0x7} = 0 001 1110 in bit order of transmission

1.4) After this the payload of the remaining data blocks is placed

Example #2: C = {7}, and U = {0,1,2,3,4,5,6}, with the control block being 0xB4. Thus:

2.1) 65B control words are present, so the 513B control flag bit gets set to 0

2.2) The first and only control word is C_0 where Position = 0x7, and BlockType = 0x5. Since this is also the last control word the continuation flag FC = 0. Thus the 513B control word for this block is:
C_0 Control Word = {0,0x7, 0x5} = 0 111 1010 in bit order of transmission

2.3) After this the payload of the remaining data blocks is placed

Example #3: C = {}, and U = {0,1,2,3,4,5,6,7}. Thus:

3.1) No 65B control words are present, so the 513B control flag bit gets set to 1

3.2) After this the payload of all of the data blocks is placed

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0	1100 000	C0	C1	C2	C3	C4	C5	C6	C7	65B #1
	0001 111	D1	D2	D3	D4	D5	D6	D7	65B #4
	D0	D1	D2	D3	D4	D5	D6	D7	65B #0
	D0	D1	D2	D3	D4	D5	D6	D7	65B #2
	D0	D1	D2	D3	D4	D5	D6	D7	65B #3
	D0	D1	D2	D3	D4	D5	D6	D7	65B #5
	D0	D1	D2	D3	D4	D5	D6	D7	65B #6
	D0	D1	D2	D3	D4	D5	D6	D7	65B #7

Example 1: *C*={1,4}, *U*={0,2,3,5,6,7}, 1st Control block = 0x1E, 2nd = 0x78

0	0111 101	C0	C1	C2	C3	C4	C5	C6	C7	65B #7
	D0	D1	D2	D3	D4	D5	D6	D7	65B #0
	D0	D1	D2	D3	D4	D5	D6	D7	65B #1
	D0	D1	D2	D3	D4	D5	D6	D7	65B #2
	D0	D1	D2	D3	D4	D5	D6	D7	65B #3
	D0	D1	D2	D3	D4	D5	D6	D7	65B #4
	D0	D1	D2	D3	D4	D5	D6	D7	65B #5
	D0	D1	D2	D3	D4	D5	D6	D7	65B #6

Example 2: Control block 0xB4, *C*={7}, *U*={0,1,2,3,4,5,6}

1	D0	D1	D2	D3	D4	D5	D6	D7	65B #0
	D0	D1	D2	D3	D4	D5	D6	D7	65B #1
	D0	D1	D2	D3	D4	D5	D6	D7	65B #2
	D0	D1	D2	D3	D4	D5	D6	D7	65B #3
	D0	D1	D2	D3	D4	D5	D6	D7	65B #4
	D0	D1	D2	D3	D4	D5	D6	D7	65B #5
	D0	D1	D2	D3	D4	D5	D6	D7	65B #6
	D0	D1	D2	D3	D4	D5	D6	D7	65B #7

Example 3: All data blocks

Figure 113–11—Examples of the construction of tx_xcoded

113.3.2.2.16 Aggregation

The six 512B/513B transcoded blocks and two 64B/65B blocks are concatenated to form tx_aggregated<3207:0>. The tx_xcoded_*j*<512:0> is mapped into tx_aggregated<513*j*+512:513*j*> where j=0 to 5. tx_xcoded_0<512:0> is the first to be transmitted. The two 64B/65B blocks are mapped into tx_aggregated<3142:3078> and tx_aggregated<3207:3143>.

113.3.2.2.17 PCS Scrambler

The payload of the PCS PHY frame tx_aggregated<3207:0> is scrambled to tx_scrambled<3207:0> with a self-synchronizing scrambler. The scrambler for the MASTER shall produce the same result as the

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implementation shown in Figure 113–12. This implements the scrambler polynomial[190] as shown in Equation (113–1):

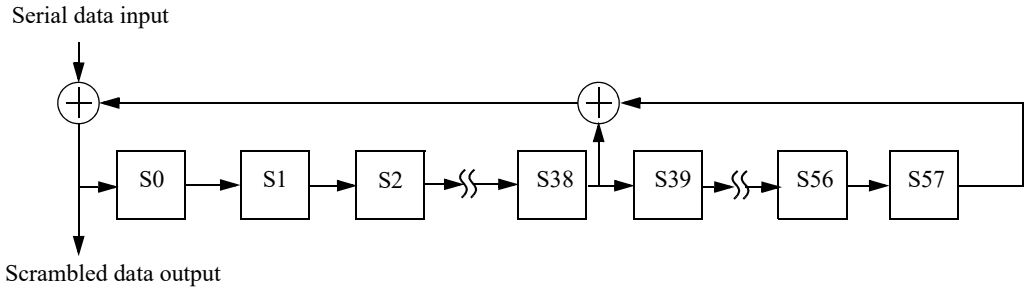
$$G(x) = 1 + x^{39} + x^{58} \quad (113–1)$$

The scrambler for the SLAVE shall produce the same result as the implementation shown in Figure 113–12. This implements the scrambler polynomial as shown in Equation (113–2):

$$G(x) = 1 + x^{19} + x^{58} \quad (113–2)$$

The initial seed values for the MASTER and SLAVE are left to the implementer. The scrambler is run continuously on all payload bits.

PCS scrambler employed by the MASTER



PCS scrambler employed by the SLAVE

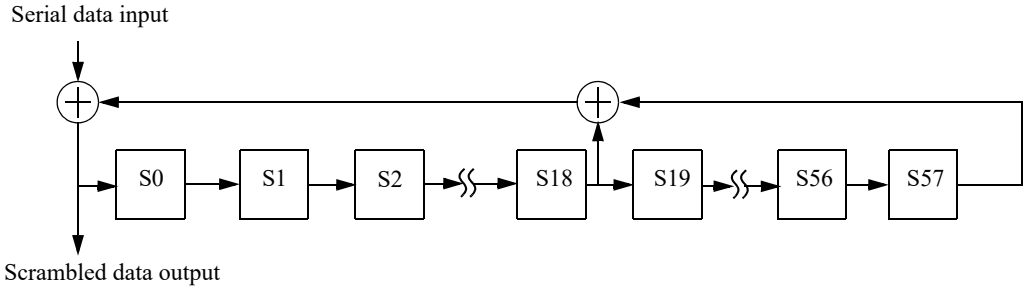


Figure 113–12—MASTER and SLAVE PCS scramblers

[190]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (113–1). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.

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113.3.2.2.18 LDPC framing and LDPC encoder

The resulting payload of scrambled six 513B transcoded blocks plus two 65B blocks, followed by two random fill bits, and six eight-bit Reed Solomon parity symbols and preceded by 1 auxiliary bit results in a total payload of 6 × 513 + 2 × 65 + 2+ 6× 8+ 1 = 3259 bits. The use of the auxiliary bit for vendor-specific communication is outside the scope of this document. It is highly recommended that the auxiliary bit be randomized. For the purposes of this standard it is ignored by the link partner, as are the random fill bits. From the total payload of 3259 bits, 1536 (3 bits for each of the 512 DSQ128 symbols) are RS-FEC-coded bits and the remaining 1723 shall be encoded by the LDPC(1723, 2048) generator matrix G. G is described in Annex 55A. See Figure 113–8 and 113.3.2.2.19 for details on PCS bit ordering and RS-FEC encoding.

The LPDC encoding takes the 1723-bit input code vector x = [x_0 x_1 x_2 ... x_{1722}], and shall generate the 2048-bit codeword c represented by the matrix multiplication c = x × G. For both x and c the encoder shall follow the notation described in 113.3.2.2.3 where the LSB (leftmost element of the vectors x and c) is the first bit into the LDPC encoder and the first transmitted bit.

113.3.2.2.19 Reed Solomon encoder

The group of 1536 bits are encoded using a Reed-Solomon encoder operating over the Galois Field GF(2^8) where the symbol size is 8 bits. The encoder processes k=186 eight-bit RS-FEC message symbols to generate 2t=6 eight-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of n=k+2t=192 eight-bit RS-FEC symbols. For the purposes of this clause, the Reed-Solomon code is denoted RS-FEC(n,k), and the particular Reed-Solomon code is RS-FEC(192,186).

The code is based on the generating polynomial given by Equation (113–3):

$$g(x) = \prod_{j=0}^{5} \left(x - \alpha^j\right) = g_6x^6 + g_5x^5 + g_4x^4 + g_3x^3 + g_2x^2 + g_1x + g_0 \quad (113–3)$$

In Equation (113–3), α , is a primitive element of the finite field defined by the primitive polynomial 0x11D = $x^8+x^4+x^3+x^2+1$.

Equation (113–4) defines the message polynomial m(x) whose coefficients are the message symbols m_{185} to m_0:

$$m(x) = m_{185}x^{191} + m_{184}x^{190} + \ldots + m_1x^7 + m_0x^6 \quad (113–4)$$

Each message symbol m_i is the bit vector ($m_{i,7}$, $m_{i,6}$, ... $m_{i,1}$,$m_{i,0}$) that is identified with the element of the finite field. The message symbols are composed of the bits in tx_RSmessage<1487:0> where

$m_{i,j}$=tx_RSmessage<(185-i)8 + j>, i=0 to 185, j=0 to 7.

tx_RSmessage<1487:0> is formed as follows:

tx_RSmessage<0> = Auxiliary bit
tx_RSmessage<2:1>=tx_scrambled<1:0>
tx_RSmessage<1292:3> = tx_RSmessage<3j+5:3j+3> = tx_scrambled<8+7j:6+7j> where j = 429 to 0
tx_RSmessage<1485:1293> = tx_scrambled<3207:3015>
tx_RSmessage<1487:1486> = 00 (It is highly recommended that two random fill bits be transmitted instead of zeros, and then this information is discarded upon receipt)

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The first symbol input to the encoder is m_{185}.

tx_scrambled<3207:0> is defined in 113.3.2.2.17.

Equation (113–5) defines the parity polynomial *p(x)* whose coefficients are the parity symbols p_5 to p_0:

$$p(x) = p_5x^5 + p_4x^4 + p_3x^3 + p_2x^2 + p_1x + p_0 \quad (113–5)$$

The parity polynomial is the remainder from the division of m(x) by g(x). This may be computed using the shift register implementation illustrated in Figure 113–13. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0, is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial c(x) is then the sum of m(x) and p(x) where the coefficient of the highest power of x, $c_{191} = m_{185}$ is transmitted first and the coefficient of the lowest power of *x*, $c_0 = p_0$ is transmitted last. The first bit transmitted from each symbol is bit 0.

The coefficients of the generator polynomial for the code are presented in Table 113–5.

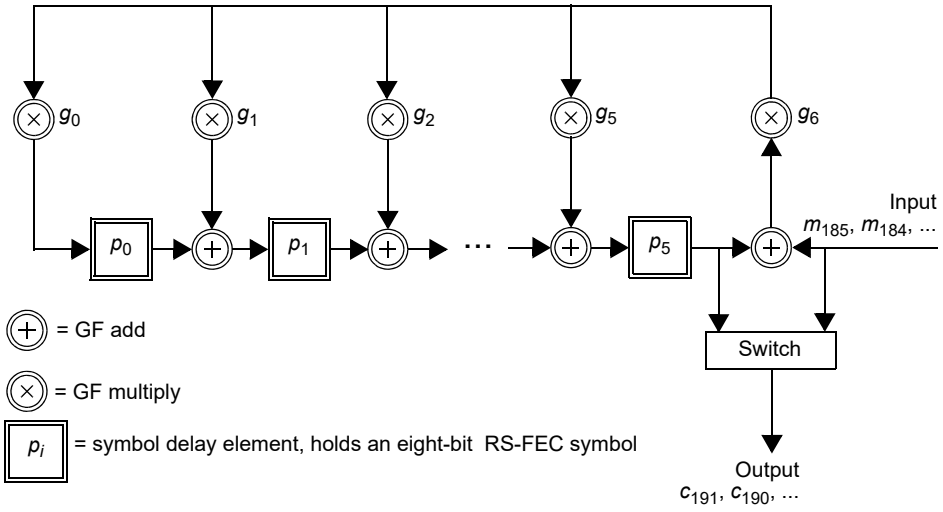

Figure 113–13—Reed-Solomon encoder functional model

113.3.2.2.20 DSQ128 bit mapping

DSQ128 refers to a two-dimensional constellation with 128 possible 2D values, such that the combined 2D symbol carries $\log_2(128)$ or 7 bits. The PHY frame of 1536 RS-FEC-coded bits and 2048 (LDPC output) LDPC-coded bits described in Figure 113–6 shall be partitioned into seven-bit groups of (3 RS-FEC-coded, 4 LDPC-coded) as described in Figure 113–8. The bit partition is as follows, the first 1290 (3 × 430) RS-FEC-coded bits are paired with the first 1720 (4 × 430) LDPC input bits. The following 3 RS-FEC-coded bits are paired with the last 3 LDPC input bits and the first LDPC parity bit. Finally the remaining 243 (3 × 81) RS-FEC-coded bits are paired with the remaining 324 (4 × 81) LDPC parity bits.

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Table 113–5—Coefficients of the generator polynomial g_i (decimal)

i	RS-FEC(192, 186)
0	38
1	227
2	32
3	218
4	1
5	63
6	1

Each 2D-DSQ128 value has two PAM16 components denoted $PAM16_1$ and $PAM16_2$ respectively. The DSQ128 can be constructed by pruning the 256 values of a 2D-PAM16 where every other point in 2D is discarded (like the black or white squares in a checkerboard). The PAM16 components $PAM16_1$ and $PAM16_2$ can each take any of the values from the set {–15, –13, –11, –9, –7, –5, –3, –1, 1, 3, 5, 7, 9, 11, 13, 15}. The mapping from 7 bits where u_0 u_1 u_2 denote the 3 RS-FEC-coded bits and c_0 c_1 c_2 c_3 denote the 4 LDPC-coded bits to the DSQ128 is described by the following four steps (the bits from the scrambler output shall be read LSB first):

Step 1:

$x_{13} = (!u_0)\ \&\ u_2$

$x_{12} = u_0\ \text{XOR}\ u_2$

$x_{11} = c_0$

$x_{10} = c_0\ \text{XOR}\ c_1$

$x_{23} = (u_1\ \&\ u_2)\ \text{OR}\ (u_0\ \&\ !u_1)$

$x_{22} = u_1\ \text{XOR}\ u_2$

$x_{21} = c_2$

$x_{20} = c_2\ \text{XOR}\ c_3$

Step 2:

$x_1 = 8x_{13} + 4x_{12} + 2x_{11} + x_{10}$

$x_2 = 8x_{23} + 4x_{22} + 2x_{21} + x_{20}$

Step 3:

$y_1 = (x_1 + x_2)\ \text{mod}16$

$y_2 = (–x_1 + x_2)\ \text{mod}16$

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Step 4:

$$PAM16_1 = 2y_1 - 15$$

$$PAM16_2 = 2y_2 - 15$$

where '*n* mod16' for an integer *n*, is defined as the integer value *p* in the range 0 to 15 (both inclusive) such that '$p = n + 16m$', for some integer *m*.

113.3.2.2.21 DSQ128 to 4D-PAM16

The DSQ mapper generates 512 2D-DSQ128 symbols per LDPC frame that are mapped onto 256 4D-PAM16 symbols prior to sending to the PMA via PMA_UNITDATA.request. The mapping of DSQ128 to 4D-PAM16 is illustrated in Figure 113–6. As shown in Figure 113–6, the two PAM16 components of each DSQ128 symbol are mapped onto two consecutive time periods on the same wire pair.

113.3.2.2.22 Block-LDPC framer

The Block-LDPC framer adapts between the mixed 513B and 65B blocks and the 4D-PAM16 width of the PMA. When the transmitter is operating in normal mode, the 65B-LDPC sends four PAM16 of transmit data at a time via PMA_UNITDATA.request primitives. The PMA_UNITDATA.request primitives are fully packed with bits.

113.3.2.2.23 EEE capability

The optional 25G/40GBASE-T EEE capability allows compliant PHYs to transition to an LPI mode of operation when link utilization is low.

PHYs that support EEE shall implement the EEE transmit state diagram, shown in Figure 113–20, within the PCS.

When PCS_Reset is asserted or pcs_data_mode is not asserted, the state diagram enters the TX_NORMAL state.

When a complete 64B/65B block of LPI characters is generated by the PCS transmit function, the PHY transmits the sleep signal to indicate to the link partner that it is transitioning to the LPI transmit mode. If the sleep signal begins on an LDPC frame boundary, then it contains 6 full LDPC frames each composed entirely of RS-FEC and LDPC encoded LP_IDLE blocks. If the sleep signal does not begin on an LDPC frame boundary, then it contains one LDPC frame partially composed of LP_IDLE blocks followed by 6 LDPC frames fully composed of LP_IDLE blocks.

Following the transmission of the sleep signal, quiet-refresh signaling begins, as described in 113.3.5.

After the sleep signal is transmitted LPI control characters shall be input to the PCS scrambler continuously until the PCS Transmit Function exits the LPI transmit mode.

While the PMA asserts SEND_N, the lpi_tx_mode variable shall control the transmit signal through the PMA_UNITDATA.request primitive described as follows:

When the PHY is not in the PCS_Data state, the lpi_tx_mode variable is ignored.

When the lpi_tx_mode variable takes the value NORMAL and the PMA asserts SEND_N, the PCS passes coded data to the PMA via the PMA_UNITDATA.request primitive as described in 113.3.2.2.

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When the lpi_tx_mode variable takes the value QUIET and the PMA asserts SEND_N, the PCS passes zeros to the PMA through the PMA_UNITDATA.request primitive.

When the lpi_tx_mode variable takes the value REFRESH_A and the PMA asserts SEND_N, the PCS passes the PMA training signal to the PMA on pair A, to allow both the local and remote PHY to refresh adaptive filters and timing loops. The PCS passes zeros to all other pairs in this condition. REFRESH_B, REFRESH_C and REFRESH_D operate in an analogous manner for the other pairs.

When the lpi_tx_mode variable takes the value ALERT and the PMA asserts SEND_N, the PCS passes the ALERT vector to the PMA.

The quiet-refresh cycle is repeated until codewords other than LP_IDLE are detected at the 25GMII/XLGMII. These codewords indicate that the local system is requesting a transition back to the normal operational mode. Following this event, the PMA_UNITDATA.request parameter tx_symb_vector is set to the value ALERT. The alert signal is not synchronized with respect to the quiet-refresh cycle but shall be synchronized so that the alert signal from the PMA begins on a LDPC frame boundary.

The PHY will also transition back to the normal operation mode if an error condition occurs. This error condition is defined as the detection of any characters other than LPI or IDLE at the 25GMII/XLGMII.

After the alert signal the PCS completes the transition from LPI mode to normal mode by sending a wake signal containing lpi_wake_time LDPC frames composed of IDLE 64B/65B blocks.

lpi_wake_time is a fixed parameter that is defined as 9 LDPC frames as shown in Table 113–6. The maximum PHY wake time when wake is requested before sleep has been completely transmitted is 1.6 μs (lpi_wake_timer=T_{w_phy} as defined by Clause 78). The maximum PHY wake time when wake is requested after sleep has been completely transmitted is 1.12 μs.

Table 113–6—LPI wake time

lpi_wake_time	lpi_wake_timer when wake starts before sleep signal is complete		lpi_wake_timer when wake starts after sleep signal is complete	
(frames)	(frames)	(μs)	(frames)	(μs)
9	20	1.6	14	1.12

113.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B receive state diagram in Figure 113–19a and Figure 113–19b and the PCS Receive bit ordering in Figure 113–7 including compliance with the associated state variables as specified in 113.3.6.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb_vector. The PCS receiver uses knowledge of the encoding rules to correctly align the 65B-LDPC frames. The received 65B-LDPC frames are decoded with error correction on both the RS-FEC and LDPC codes, and framing is checked; the six 512B/513B blocks are transcoded to 64B/65B. This process generates the 64B/65B block vector rx_coded<64:0> that is then decoded to form the 25GMII signals RXD<31:0> and RXC<3:0> for 25GBASE-T or the XLGMII signals RXD<63:0> and RXC<7:0> for 40GBASE-T, as specified in the PCS 64B/65B Receive state diagram (see Figure 113–19a and Figure 113–19b). 100 25GMII or 50 XLGMII data transfers are decoded from one LDPC frame. Where the 25GMII or XLGMII and PMA sublayer data rates are not synchronized in a 25:64 ratio or 25:128 ratio,

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respectively, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primitive to OK.

When the PCS Synchronization process has obtained synchronization, the LDPC frame error ratio (LFER) monitor process monitors the signal quality asserting hi_lfer if excessive LDPC frame errors are detected (LDPC parity error or uncorrectable RS-FEC error). If 40 consecutive LDPC frame errors are detected, the block_lock flag is de-asserted. When block_lock is asserted and hi_lfer is de-asserted, the pcs_status parameter of the PMA_PCSSTATUS.request primitive is set to OK, and the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD and RXC on the 25GMII/XLGMII.

When the receiver is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication (loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.request primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training sequence includes one-bit pattern on pair A every 256 PAM2 symbols, which is aligned with the PCS PHY frame boundary. When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.

PHYs with the EEE capability support transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. Transitions to and from the LPI mode are allowed to occur independently in the transmit and receive functions. The PCS receive function is responsible for detecting transitions to and from the LPI receive mode and indicating these transitions using signals defined in 113.2.2.

The link partner signals a transition to the LPI mode of operation by transmitting 6 LDPC frames composed entirely of 64B/65B blocks of /LI/. When blocks of /LI/ are detected at the output of the 64B/65B decoder, rx_lpi_active is asserted by the PCS receive function and the /LI/ character is continuously asserted at the receive 25GMII/XLGMII. These frames may be preceded by a frame composed partially of /LI/ characters. After these frames the link partner begins transmitting zeros, and it is recommended that the receiver power down receive circuits to reduce power consumption. The receive function uses LDPC frame counters to maintain synchronization with the remote PHY and receives periodic refresh signals that are used to update coefficients, so that the integrity of adaptive filters and timing loops in the PMA is maintained. LPI signaling is defined in 113.3.5. The quiet-refresh cycle continues until the PMA asserts alert_detect to indicate that the alert signal has been reliably detected. After the alert signal the link partner transmits repeated /I/ characters, representing a wake signal. The PHY receive function sends /I/ to the 25GMII/XLGMII for 9 LDPC frame periods and then resumes normal operation.

113.3.2.3.1 Frame and block synchronization

When the receiver is operating in normal mode, the frame and block synchronization function receives data via 4D-PAM16 PMA_UNITDATA.request primitives. It shall form a 4D-PAM16 stream from the primitives by concatenating requests with the PAM16s of each primitive in order from rx_data-group<0> to rx_data-group<255> (see Figure 113–7). It obtains block_lock to the LDPC frames during the PAM2 training pattern using synchronization bits provided on pair A. The 65-bit blocks are extracted based on their location in the LDPC frame.

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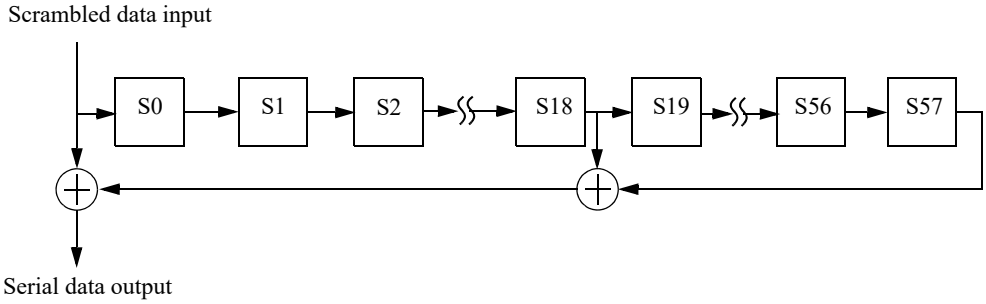
113.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. It shall produce the same result as the implementations shown in Figure 113–14 for the MASTER and the SLAVE.

PCS descrambler employed by the MASTER



PCS descrambler employed by the SLAVE

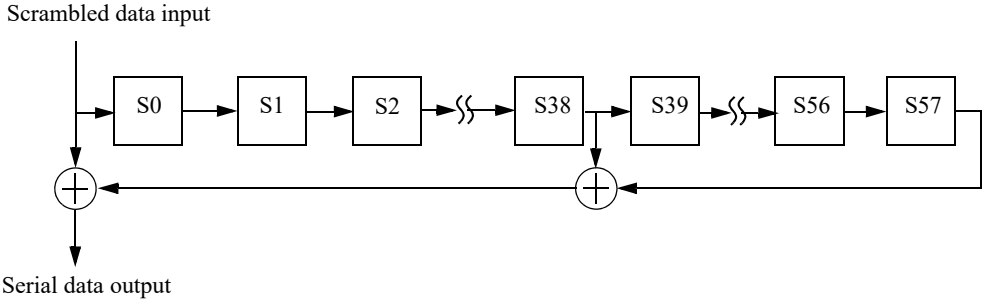


Figure 113–14—MASTER and SLAVE PCS descramblers

113.3.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exists:

a) The block type field contains a reserved value.
b) For 25GBASE-T, any control character contains a value not in Table 113–1, or Table 113–2 for 40GBASE-T.
c) For 25GBASE-T, any O code contains a value not in Table 113–1, or Table 113–2 for 40GBASE-T.
d) The block contains information from the payload of an invalid received PHY frame or the first 64B/65B block following an invalid received PHY frame.

The PCS Receive function shall check the integrity of the LDPC and RS-FEC parity bits defined in 113.3.2.2.18 and 113.3.2.2.19, respectively. If either check fails the PHY frame is invalid.

R_BLOCK_TYPE of an invalid block is set to E.

113.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, link segment, and remote receiver. When the transmit PCS is operating in test-pattern mode it shall transmit continuously

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as illustrated in Figure 113–6, with the input to the scrambler set to zero and the initial condition of the scrambler set to any non-zero value. When the receiver PCS is operating in test-pattern mode it shall receive continuously as illustrated in Figure 113–7. After acquiring the self-synchronizing scrambler state, the output of the received scrambled values should ideally be zero. Any nonzero values correspond to receiver bit errors. This mode is further described as test mode 7 in 113.5.2.

113.3.4 PMA training side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling for generating 2-level PAM PMA training sequences as shown in Figure 113–15. An implementation of MASTER and SLAVE PHY side-stream scramblers is shown in the "Main PN sequence" box. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

113.3.4.1 Generation of bits Sa_n, Sb_n, Sc_n, Sd_n

PMA training signal encoding rules are based on the generation, at time n, of the four bits Sa_n, Sb_n, Sc_n, Sd_n. These four bits are generated in a systematic fashion using the bits in $Scr_n[32:0]$, and an auxiliary generating polynomial. For both MASTER and SLAVE PHYs, they are obtained by the same linear combinations of bits stored in the transmit scrambler shift register delay line. These four bits are derived from elements of the same maximum-length shift register sequence of length $2^{33}–1$ as $Scr_n[0]$, but shifted in time. The associated delays are all large and different so that there is no short-term correlation among the bits Sa_n, Sb_n, Sc_n, Sd_n. The four bits are generated using the bit $Scr_n[0]$ and the equations in Figure 113–15 in the "Derived sequences" box.

113.3.4.2 Generation of 4D symbols TA_n, TB_n, TC_n, TD_n

The four bits Sa_n, Sb_n, Sc_n, Sd_n are mapped to a 4D symbol (TA_n, TB_n, TC_n, TD_n) as shown in Figure 113–15.

The inversion on pair A at 256 intervals ($n = k \times 256$, $k = 0, 1, 2, \ldots$) defines the LDPC boundary during data mode.

Notice that over the repeating time intervals of 16384 and of length 128, $m \times 16384 – 128 \le n < m \times 16384$, $m = 1, 2, 3, \ldots$, the PMA training pattern in pair A is XOR'ed with the Infofield. Thus, pair A transmits the Infofield, which communicates to the remote transceiver settings of THP and power backoff and other control information.

113.3.4.3 PMA training mode descrambler polynomials

The PHY shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial $g'_M(x) = 1 + x^{20} + x^{33}$ and the SLAVE PHY shall employ the receiver descrambler generator polynomial $g'_S(x) = 1 + x^{13} + x^{33}$.

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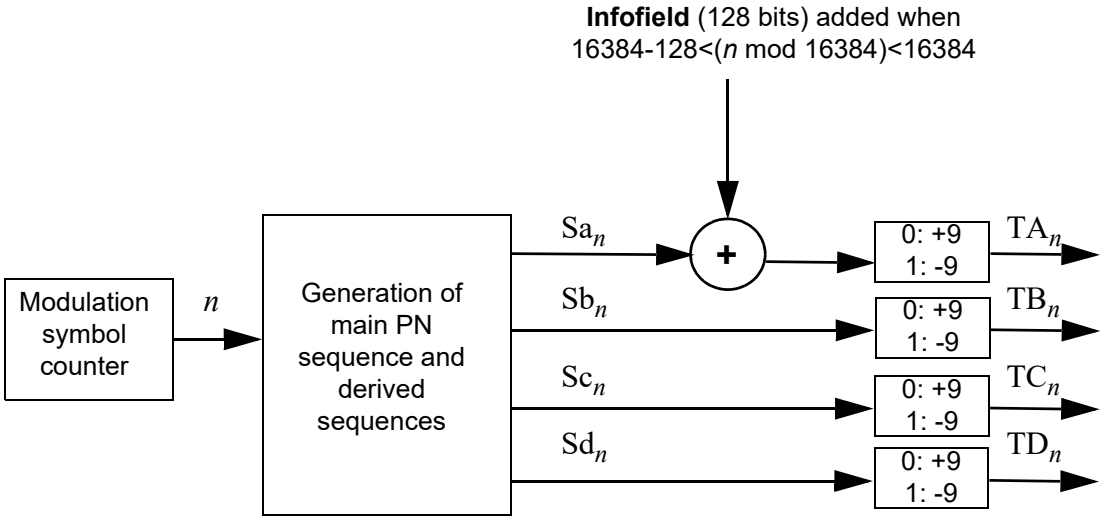

Main PN sequence:

$$Scr_n[32:1] = Scr_{n-1}[31:0]$$

$$Scr_n[0] = \begin{cases} Scr_{n-1}[12]+Scr_{n-1}[32] \text{ if PMA\_CONFIG=MASTER} \\ Scr_{n-1}[19]+Scr_{n-1}[32] \text{ if PMA\_CONFIG = SLAVE} \end{cases}$$

Derived sequences:

$$Sa_n = \begin{cases} Scr_n[0] \oplus 1 & \text{if } n \bmod 256 = 0 \\ Scr_n[0] & \text{otherwise} \end{cases}$$

$$Sb_n = Scr_n[3] \oplus Scr_n[8]$$

$$Sc_n = Scr_n[6] \oplus Scr_n[16]$$

$$Sd_n = Scr_n[9] \oplus Scr_n([14] \oplus Scr_n([19] \oplus Scr_n[24]))$$

Figure 113–15—A realization of PMA training PAM2 sequences

113.3.5 LPI signaling

PHYs with EEE capability have transmit and receive functions that can enter and leave the LPI mode independently. The PHY can transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. The transmit function of the PHY initiates a transition to the LPI transmit mode when it generates 64B/65B blocks composed entirely of LPI control characters, as described in 113.3.2.2.23. The transmit function of the link partner signals the transition using the sleep signal. When the transmitter begins to send the sleep signal, it asserts tx_lpi_active and the transmit function enters the LPI transmit mode.

Within the LPI mode PHYs use a repeating quiet-refresh cycle (see Figure 113–16). The first part of this cycle is known as the quiet period and lasts for a time lpi_quiet_time equal to 122 LDPC frame periods. The quiet period is defined in 113.3.5.2. The second part of this cycle is known as the refresh period and lasts for a time lpi_refresh_time equal to 6 LDPC frame periods. The refresh period is defined in 113.3.5.3. A cycle composed of one quiet period and one refresh period is known as a *single pair LPI cycle* and lasts for a time lpi_qr_time equal to 128 LDPC frame periods. The time taken to complete a quiet-refresh cycle for all four pairs is known as a *complete LPI cycle*.

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lpi_offset, lpi_quiet_time, lpi_refresh_time, lpi_qr_time, and lpi_allpairs_qr_time are timing parameters that are integer multiples of the LDPC frame period. lpi_offset is a fixed value equal to lpi_qr_time/2 that is used to ensure refresh signals are appropriately offset by the link partners.

PHYs begin the transition from the LPI receive mode when the alert signal is detected by the PMA as defined in 113.4.2.4.

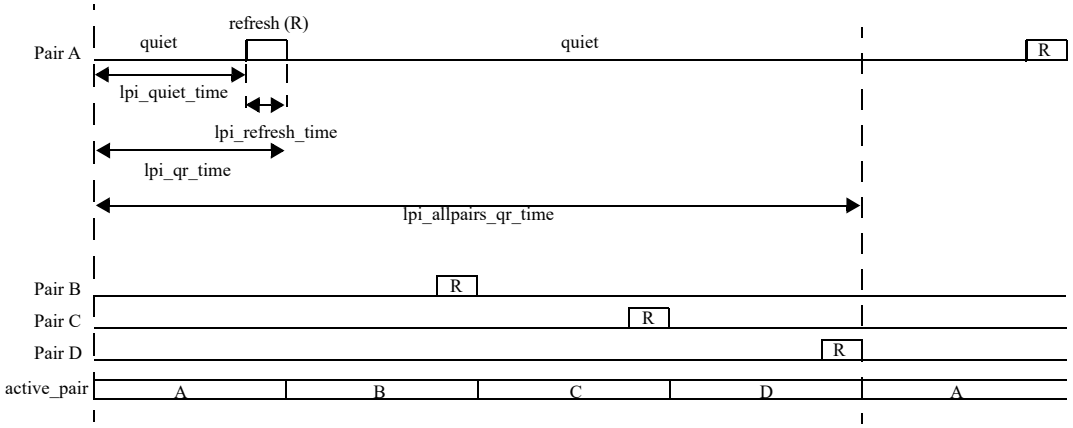

Figure 113–16—Timing periods for LPI signals

113.3.5.1 LPI Synchronization

To maximize power savings, maintain link integrity, and ensure interoperability, EEE-capable PHYs synchronize refresh intervals during the LPI mode. The transition to PCS_Test is used as a fixed timing reference for the link partners. Refresh signaling is derived by counting LDPC frames from the transition to PCS_Test.

In initial training, normal retraining, and fast retraining, with or without the EEE capability being supported, the master and slave signal when they will transition to PCS_Test using the transition counter following the procedure described in 113.4.2.5.15.

An EEE-capable PHY in slave mode is responsible for synchronizing its PMA training frame to the master's PMA training frame during the transition to PMA_Training_Init_S. The slave shall ensure that its PMA training frames are synchronized to the master's PMA training frames within 1 LDPC frame, measured at the slave MDI on pair A. In addition, the slave shall initialize its transition counter so that it transitions to PCS_Test within 1 LDPC frame of the master PHY's transition to PCS_Test, measured at the slave PHY's MDI on pair A. This mechanism ensures that the refresh offset is bounded to a small value at both MDI interfaces, thus ensuring there is no overlap of master and slave signals when both transmit and receive are in the LPI mode.

Following the transition to PCS_Test, the PCS counts transmitted and received LDPC frames, and uses these counters to generate refresh and pair control signals for the transmit and receive functions. The transmitted LDPC frame count is named tx_ldpc_frame_cnt. The received LDPC frame count is named rx_ldpc_frame_cnt.

The master and slave shall derive the active pair and refresh_active signals from the LDPC frame counters as shown in Table 113–7 and Table 113–8.

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Table 113–7—Synchronization logic derived from slave signal LDPC frame count

Slave-side variable	Master-side variable	for master u=rx_ldpc_frame_cnt for slave u=tx_ldpc_frame_cnt
tx_refresh_active=true	rx_refresh_active=true	lpi_offset – lpi_refresh_time ≤ mod(u,lpi_qr_time) < lpi_offset
tx_lpi_full_refresh=true	N/A	lpi_offset – lpi_refresh_time = mod(u,lpi_qr_time)
tx_active_pair=PAIR_A	rx_active_pair=PAIR_A	lpi_offset + lpi_qr_time £ u < lpi_offset + 2 × lpi_qr_time
tx_active_pair=PAIR_B	rx_active_pair=PAIR_B	lpi_offset + 2 × lpi_qr_time ≤ u < lpi_offset + 3 × lpi_qr_time
tx_active_pair=PAIR_C	rx_active_pair=PAIR_C	lpi_offset + 3 × lpi_qr_time ≤ u < 4 × lpi_qr_time OR 0 ≤ u < lpi_offset
tx_active_pair=PAIR_D	rx_active_pair=PAIR_D	lpi_offset ≤ u < lpi_offset + lpi_qr_time

Table 113–8—Synchronization logic derived from master signal LDPC frame count

Slave-side variable	Master-side variable	for master v=tx_ldpc_frame_cnt for slave v=rx_ldpc_frame_cnt
rx_refresh_active=true	tx_refresh_active=true	lpi_quiet_time ≤ mod(v,lpi_qr_time)
N/A	tx_lpi_full_refresh=true	lpi_quiet_time = mod(v,lpi_qr_time)
rx_active_pair=PAIR_A	tx_active_pair=PAIR_A	0 ≤ v < lpi_qr_time
rx_active_pair=PAIR_B	tx_active_pair=PAIR_B	lpi_qr_time ≤ v < 2 × lpi_qr_time
rx_active_pair=PAIR_C	tx_active_pair=PAIR_C	2 × lpi_qr_time ≤ v < 3 × lpi_qr_time
rx_active_pair=PAIR_D	tx_active_pair=PAIR_D	3 × lpi_qr_time ≤ v < 4 × lpi_qr_time

113.3.5.2 Quiet period signaling

During the quiet period the transmitters on all four pairs should be turned off. Average launch power (as measured from 28 LDPC frames after a refresh period to 28 LDPC frames before the next refresh period on the same lane) for each Transmitter shall be less than –41 dBm. This requirement does not apply to the periods when the alert signal is transmitted as defined in 113.4.2.2.1.

113.3.5.3 Refresh period signaling

During the LPI mode 25G/40GBASE-T PHYs use staggered, out-of-phase refresh signaling to maximize power savings. Two-level PAM refresh symbols are generated using the PMA side-stream scrambler polynomials described in 113.3.4 and exactly as is shown in Figure 113–15 with the exception that the Infofield consists of a sequence of 128 zeros. The training sequence shall be used during the LPI mode.

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Refresh signals shall be sent using the THP filter as described in 113.4.3.1. At the start of each refresh signal the THP feedback delay line shall be initialized with zeros.

While a transmit function is in the LPI transmit mode only one of the transmit pairs is active during a refresh period. tx_symb_vector for all transmit pairs that are not active shall be set to zero.

When tx_symb_vector has the value ALERT and the PHY is master, the transmitter on pair A shall be active and all other pairs shall be quiet. When tx_symb_vector has the value ALERT and the PHY is slave, the transmitter on pair C shall be active and all other pairs shall be quiet. If lpi_tx_mode=REFRESH_A on a MASTER PHY or lpi_tx_mode=REFRESH_C on a SLAVE PHY, and tx_symb_vector has the value ALERT, then the alert signalling shall be transmitted in place of the refresh signalling where the signals overlap.

113.3.6 Detailed functions and state diagrams

113.3.6.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

113.3.6.2 State diagram parameters

113.3.6.2.1 Constants

EBLOCK_R<71:0>
: 72-bit vector to be sent to the 25GMII/XLGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>
: 65-bit vector to be sent to the 512B/513B transcoder and block-LDPC framer containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
: 72-bit vector to be sent to the 25GMII/XLGMII interface containing a Local Fault ordered set. The Local Fault ordered set is defined in 81.3.4.

LBLOCK_T<64:0>
: 65-bit vector to be sent to the 512B/513B transcoder and block-LDPC framer containing a Local Fault ordered set.

LPBLOCK_R<71:0>
: 72-bit vector to be sent to the 25GMII/XLGMII containing /LI/ in all the eight character locations.

LPBLOCK_T<64:0>
: 65-bit vector to be sent to the 512B/513B transcoder and block-LDPC framer containing /LI/ in all the eight character locations.

IBLOCK_R<71:0>
: 72-bit vector to be sent to the 25GMII/XLGMII containing /I/ in all the eight character locations.

IBLOCK_T<64:0>
: 65-bit vector to be sent to the 512B/513B transcoder and block-LDPC framer containing /I/ in all the eight character locations.

UBLOCK_R<71:0>

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72-bit vector to be sent to the 25GMII/XLGMII containing a Link Interruption ordered set. The Link Interruption ordered set is defined in 81.3.4.

113.3.6.2.2 Variables

lfer_test_lf
: Boolean variable that is set true when a new LDPC frame is available for testing and false when LFER_TEST_LF state is entered. A new LDPC frame is available for testing when the Block Sync process has accumulated enough symbols from the PMA to evaluate the next LDPC frame.

block_lock
: Boolean variable that is set true when receiver acquires block delineation.

hi_lfer
: Boolean variable that is asserted true when the lfer_cnt reaches 16 errors in one lfer_timer interval.

pcs_reset
: Boolean variable that controls the resetting of the PCS. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rx_coded<64:0>
: Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 113–10. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_raw<71:0>
: Vector containing two successive 25GMII transfers or a single XLGMII output transfer. For 25GBASE-T, RXC<0> through RXC<3> for the first transfer are taken from rx_raw<0> through rx_raw<3>, respectively. RXC<0> through RXC<3> for the second transfer are taken from rx_raw<4> through rx_raw<7>, respectively. RXD<0> through RXD<31> for the first transfer are taken from rx_raw<8> through rx_raw<39>, respectively. RXD<0> through RXD<31> for the second transfer are taken from rx_raw<40> through rx_raw<71>, respectively. For 40GBASE-T, RXC<0> through RXC<7> for the transfer are taken from rx_raw<0> through rx_raw<7>, respectively. RXD<0> through RXD<63> for the transfer are taken from rx_raw<8> through rx_raw<71>, respectively.

lf_valid
: Boolean indication that is set true if received LDPC frame is valid. LDPC frame is valid if both:
  a. All parity checks of the LDPC-coded bits are satisfied
  b. The RS-FEC-coded bits, after decoding, form a valid RS-FEC codeword.

tx_coded<64:0>
: Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 113–10. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_raw<71:0>
: Vector containing two successive 25GMII transfers or a single XLGMII transfer. For 25GBASE-T, TXC<0> through TXC<3> for the first transfer are placed in tx_raw<0> through tx_raw<3>, respectively. TXC<0> through TXC<3> for the second transfer are placed in tx_raw<4> through tx_raw<7>, respectively. TXD<0> through TXD<31> for the first transfer are placed in tx_raw<8> through tx_raw<39>, respectively. TXD<0> through TXD<31> for the second transfer are placed in tx_raw<40> through tx_raw<71>, respectively. For 40GBASE-T, TXC<0> through TXC<7> for the transfer are placed in tx_raw<0> through tx_raw<7>, respectively. TXD<0> through TXD<63> for the transfer are placed in tx_raw<8> through tx_raw<71>, respectively.

The following variables are required for PHYs that support the EEE capability:

tx_lpi_active
: A Boolean variable that is set true when the PHY transmit function is operating in the LPI transmit

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mode and during transitions to and from the LPI transmit mode (i.e., at any time when the PHY is transmitting sleep, alert, wake, or quiet-refresh signaling). It is set false otherwise.

tx_lpi_qr_active
: A Boolean variable that is set true during the LPI transmit mode, when the PHY is transmitting quiet-refresh signaling. Set false otherwise.

rx_lpi_active
: A Boolean variable that is set true when the PHY receive function is operating in the LPI receive mode and set false otherwise. The LPI receive mode begins when the sleep signal is detected and lasts until the alert signal is detected. When the EEE capability is not supported, rx_lpi_active is set false.

tx_lpi_req
: A Boolean variable that is set true when the LPI client indicates that it is requesting operation in the LPI transmit mode via the 25GMII/XLGMII and set false otherwise.

alert_detect
: Indicates that an alert signal from the link partner has been received at the MDI as indicated by PMA_ALERTDETECT.indication(alert_detect).

tx_lpi_alert_active
: A Boolean variable that is set true when the PHY is transmitting ALERT signaling. Set false otherwise.

rx_lpi_wake
: A Boolean variable that is set true when the PHY receiver is in the WAKE state and sending IDLE to the 25GMII/XLGMII. Set false otherwise. When the EEE capability is not supported, rx_lpi_wake is set false.

tx_active_pair
: A variable indicating the transmit active pair during the LPI transmit mode. The variable may take the values PAIR_A, PAIR_B, PAIR_C, PAIR_D. This variable is defined in 113.3.5.1.

lpi_tx_mode
: A variable indicating the signaling to be used from the PCS to the PMA across the PMA_UNITDATA.request (tx_symb_vector) interface.
: lpi_tx_mode controls tx_symb_vector only when tx_mode is set to SEND_N.
: The variable is set to NORMAL when (!tx_lpi_qr_active * !tx_lpi_alert_active), indicating that the PCS is in the normal mode of operation and will encode code-groups as described in Figure 113–18a and Figure 113–18b.
: The variable is set to REFRESH_A when (tx_lpi_qr_active * (tx_active_pair=PAIR_A) * tx_refresh active).
: The variable is set to REFRESH_B when (tx_lpi_qr_active * (tx_active_pair=PAIR_B) * tx_refresh active).
: The variable is set to REFRESH_C when (tx_lpi_qr_active * (tx_active_pair=PAIR_C) * tx_refresh active).
: The variable is set to REFRESH_D when (tx_lpi_qr_active * (tx_active_pair=PAIR_D) * tx_refresh active).
: The variable is set to QUIET when (tx_lpi_qr_active * (!tx_refresh_active + tx_lpi_initial_quiet))
: The variable is set to ALERT when (tx_lpi_alert_active)

tx_refresh_active
: A Boolean value. This variable is set true following the logic described in 113.3.5.1.

tx_lpi_full_refresh
: A Boolean value. This variable is set true following the logic described in 113.3.5.1.

tx_lpi_initial_quiet
: A Boolean value. This variable is set true when the transmit function enters the LPI transmit mode and a partial refresh will be replaced by quiet signaling.

ldpc_frame_done
: A Boolean value. This variable is set true when the final symbol of each LDPC frame is transmitted and is set false otherwise.

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The following variable is only required for PHYs that support the fast retrain capability:

fr_sigtype

If fast retrain is supported, this variable controls the block type the PMA sends on the receive path during fast retrain. If MDIO is supported, this variable is set based on the value in 1.147.2:1 as follows:

00 IBLOCK_R
01 LBLOCK_R
10 UBLOCK_R
11 Reserved.

If MDIO is not supported, an equivalent method of controlling fast retrain functionality should be provided.

113.3.6.2.3 Timers

State diagram timers follow the conventions described in 14.2.3.2.

lfer_timer
: Timer that is triggered every $125/(4 \times S)$ μs +1%, –25%. When the timer reaches its terminal count, lfer_timer_done = TRUE

The following timers are required for PHYs that support the EEE capability:

lpi_tx_sleep_timer
: This timer defines the time the local transmitter sends the sleep signal to the link partner.
Values: The condition lpi_tx_sleep_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 6 LDPC frame periods.

lpi_tx_alert_timer
: This timer defines the time the local transmitter transmits the alert signal.
Values: The condition lpi_tx_alert_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 4 LDPC frame periods.

lpi_tx_wake_timer
: This timer defines the time the local transmitter transmits the wake signal.
Values: The condition lpi_tx_wake_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time LDPC frame periods.

lpi_rx_wake_timer
: This timer defines the time the receiver sends IDLE blocks to the 25GMII/XLGMII after the alert signal is detected.
Values: The condition lpi_rx_wake_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time LDPC frame periods.

113.3.6.2.4 Functions

DECODE(rx_symb_vector<64:0>)
: In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the LDPC decoder and decodes the 65B-LDPC bit vector returning a vector rx_raw<71:0>, which is sent to the 25GMII/XLGMII. The DECODE function shall decode the block based on code specified in 113.3.2.2.2.

ENCODE(tx_raw<71:0>)
: Encodes the 72-bit vector received from the 25GMII/XLGMII, returning 65-bit vector tx_coded. The ENCODE function shall encode the block as specified in 113.3.2.2.2.

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R_BLOCK_TYPE = {C, S, T, D, E, I, LI, LII}

When the EEE capability is not supported, this function classifies each 65-bit rx_coded vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.

When the EEE capability is supported, this function classifies each 65-bit rx_coded vector as belonging to the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /I/, but in every other case the vector belongs to only one type.

Values: C; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x1E and eight valid control characters other than /E/ and /LI/;
b) a block type field 0x4B, a valid O code, and zeros;
c) for 25GBASE-T only, a block type field 0x2D, a valid O code, and four valid control characters;
d) for 25GBASE-T only, a blcok type field of 0x55 and two valid O codes.

S; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x78;
b) for 25GBASE-T only, a block type field of 0x66 and a valid O code;
c) for 25GBASE-T only, a block type field of 0x33 and four valid control characters.

T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1, or 0xFF and all control characters are valid.

D; The vector contains a data/ctrl header of 0.

I; If the optional EEE capability is supported, then the I type is a special case of the C type where the vector contains a data/ctrl header of 1, a block type field of 0x1E, and eight control characters of /I/.

LI: If the optional EEE capability is supported, then the LI type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and eight control characters of /LI/.

LII: If the optional EEE capability is supported, then the LII type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and one of the following:

a) four control characters of /LI/ followed by four control characters of /I/;
b) four control characters of /I/ followed by four control characters of /LI/

E; The vector does not meet the criteria for any other value.

For 25GBASE-T, a valid control character is one containing a 25GBASE-T control code specified in Table 113–1. A valid O code is one containing an O code specified in Table 113–1,

For 40GBASE-T, a valid control character is one containing a 40GBASE-T control code specified in Table 113–2. A valid O code is one containing an O code specified in Table 113–2.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E, I, LI, LII}

When the EEE capability is not supported, this function classifies each 72-bit tx_raw vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.

When the EEE capability is supported, this function classifies each 72-bit tx_raw vector as belonging to the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /I/, but in every other case the vector belongs to only one type.

Values: C; The vector contains one of the following:

a) eight valid control characters other than /O/, /S/, /T/, /E/, and /LI/;
b) one valid ordered set followed by four data bytes and zeros for block code 0x4B;
c) for 25GBASE-T only, one valid ordered set followed by four valid control characters other than /O/, /S/ and /T/;

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d) for 25GBASE-T only, two valid ordered sets.

S; The vector contains an /S/ in its first character, or, for 25GBASE-T, its first or fifth character. Any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

I; If the optional EEE capability is supported, then the I type is a special case of the C type where the vector contains eight control characters of /I/.

LI: If the optional EEE capability is supported, then the LI type occurs when the vector contains eight control characters of /LI/.

LII: If the optional EEE capability is supported, then the LII type occurs when the vector contains one of the following:

a) four control characters of /LI/ followed by four control characters of /I/;

b) four control characters of /I/ followed by four control characters of /LI/.

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. For 25GBASE-T, a valid control character is one containing a 25GMII control code specified in Table 113–1. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 113–1. For 40GBASE-T, a valid control character is one containing an XLGMII control code specified in Table 113–2. A valid ordered set consists of a valid /O/ character in the first character and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 113–2.

T_TYPE(tx_raw<71:0>)
: Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

T_TYPE_NEXT
: Prescient end of packet check function. It returns the FRAME_TYPE of the tx_raw vector immediately following the current tx_raw vector.

113.3.6.2.5 Counters

lfer_cnt
: Count up to a maximum of 16 of the number of invalid LDPC frames within the current lfer_timer period.

The following counters are required for PHYs that support the EEE capability:

tx_ldpc_frame_cnt
: An integer value that counts transmit LDPC frame periods. The counter is reset when the first symbol of the first LDPC frame crosses the MDI on pair A in the transmit direction after normal training or fast retraining. It is incremented after the last symbol of each transmitted LDPC frame. tx_ldpc_frame_cnt is reset to 0 when tx_ldpc_frame_cnt = lpi_qr_time × 4.

rx_ldpc_frame_cnt
: An integer value that counts receive LDPC frame periods. The counter is reset when the first symbol of the first LDPC frame crosses the MDI on pair A in the receive direction after normal training or fast retraining. It is incremented after the last symbol of each received LDPC frame. rx_ldpc_frame_cnt is reset to 0 when rx_ldpc_frame_cnt = lpi_qr_time × 4.

lpi_rxw_err_cnt
: An integer value that counts the number of receive wake on error conditions. lpi_rxw_err_cnt is reset to zero during PCS_Test. The counter is reflected in register 3.22 (see 45.2.3.12).

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113.3.6.3 State diagrams

The LFER Monitor state diagram shown in Figure 113–17 monitors the received signal for high LDPC frame error ratio.

The 64B/65B Transmit state diagram shown in Figure 113–18a controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the Transmit state diagram sends Local Fault ordered sets when reset is asserted, the scrambler and 65B-LDPC are not guaranteed to be operational during reset. Thus, the Local Fault ordered sets are not guaranteed to appear on the PMA service interface.

The 64B/65B Receive state diagram shown in Figure 113–19a controls the decoding of 65B received blocks. It makes exactly one transition for each receive block processed except for the transition from RX_WE to RX_E, which occurs immediately after the RX_WE processes are complete.

The PCS shall perform the functions of LFER Monitor, Transmit, and Receive as specified in these state diagrams. The PCS shall not perform the LFER Monitor function during LPI receive operation from the time that the PCS 64B/65B Receiver enters the state RX_L, until the state RX_W is exited.

Transitions surrounded by dashed rectangles indicate requirements for 25G/40GBASE-T EEE-capable implementations.

113.3.7 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

113.3.7.1 Status

pcs_status
: Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_lfer is false. This status is reflected in MDIO register 3.32.12. A latch low view of this status is reflected in MDIO register 3.1.2 and a latch high of the inverse of this status, Receive fault, is reflected in MDIO register 3.8.10.

block_lock
: Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.32.0. A latch low view of this status is reflected in MDIO register 3.33.15.

hi_lfer
: Indicates the state of the hi_lfer variable. This status is reflected in MDIO register 3.32.1. A latch high view of this status is reflected in MDIO register 3.33.14.

Rx LPI indication
: For EEE capability, this variable indicates the current state of the receive LPI function. This flag is set to TRUE (register bit set to one) when the PCS 64B/65B Receive state diagram (Figure 113–19b) is in the RX_L or RX_W states. This status is reflected in MDIO register 3.1.8. A latch high view of this status is reflected in MDIO register 3.1.10 (Rx LPI received).

Tx LPI indication
: For EEE capability, this variable indicates the current state of the transmit LPI function. This flag is set to TRUE (register bit set to one) when the PCS 64B/65B Transmit state diagram (Figure 113–18b) is in the TX_L or TX_W states. This status is reflected in MDIO register 3.1.9. A latch high view of this status is reflected in MDIO register 3.1.11 (Tx LPI received).

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113.3.7.2 Counters

The following counters are reset to zero upon read and upon reset of the PCS. When they reach all ones, they stop counting. Their purpose is to help monitor the quality of the link.

lfer_count
: Six-bit counter that counts each time LFER_BAD_LF state is entered. This counter is reflected in MDIO register bits 3.33.13:8. The counter is reset when register 3.33 is read by management. Note that this counter counts a maximum of 16 counts per lfer_timer period since the LFER_BAD_LF can be entered a maximum of 16 times per lfer_timer window.

errored_block_count
: Eight-bit counter. When the receiver is in normal mode, errored_block_count counts once for each time RX_E state is entered. This counter is reflected in MDIO register bits 3.33.7:0

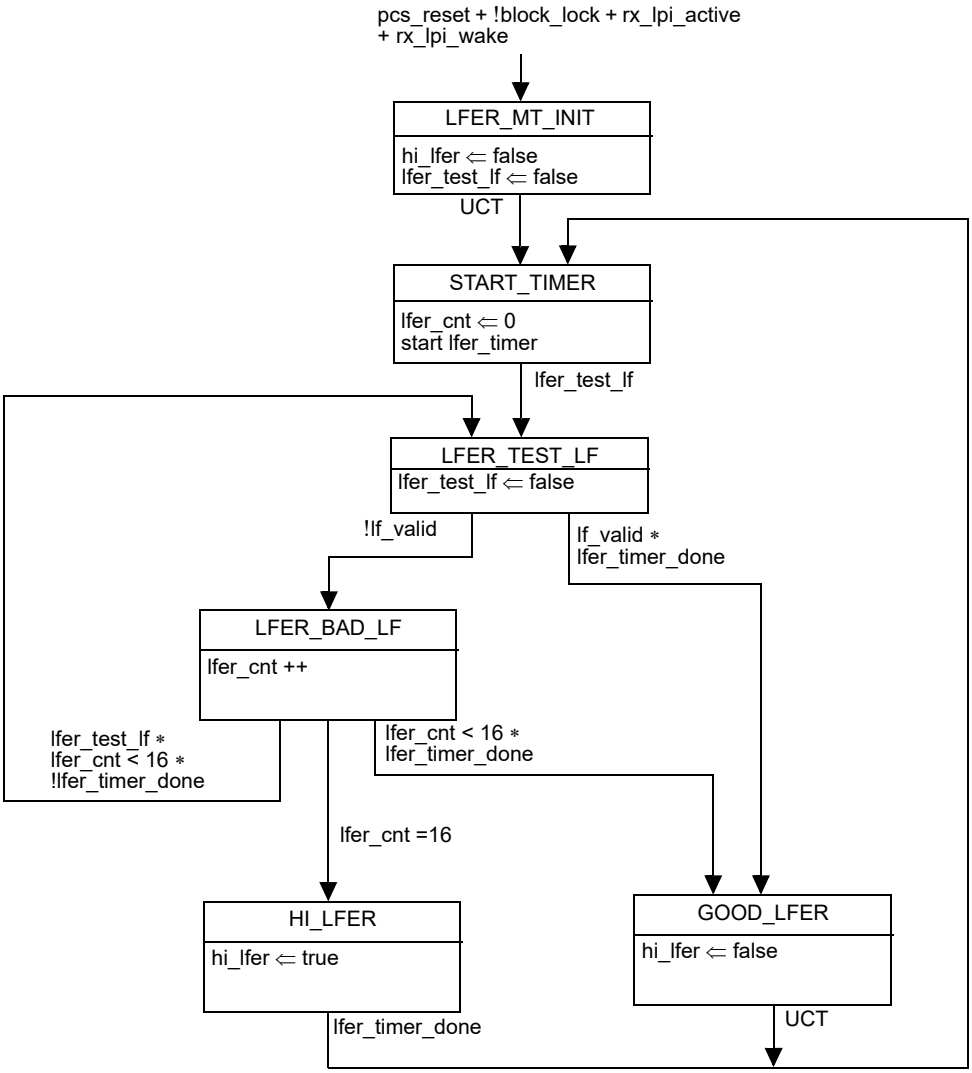

Figure 113–17—LFER monitor state diagram

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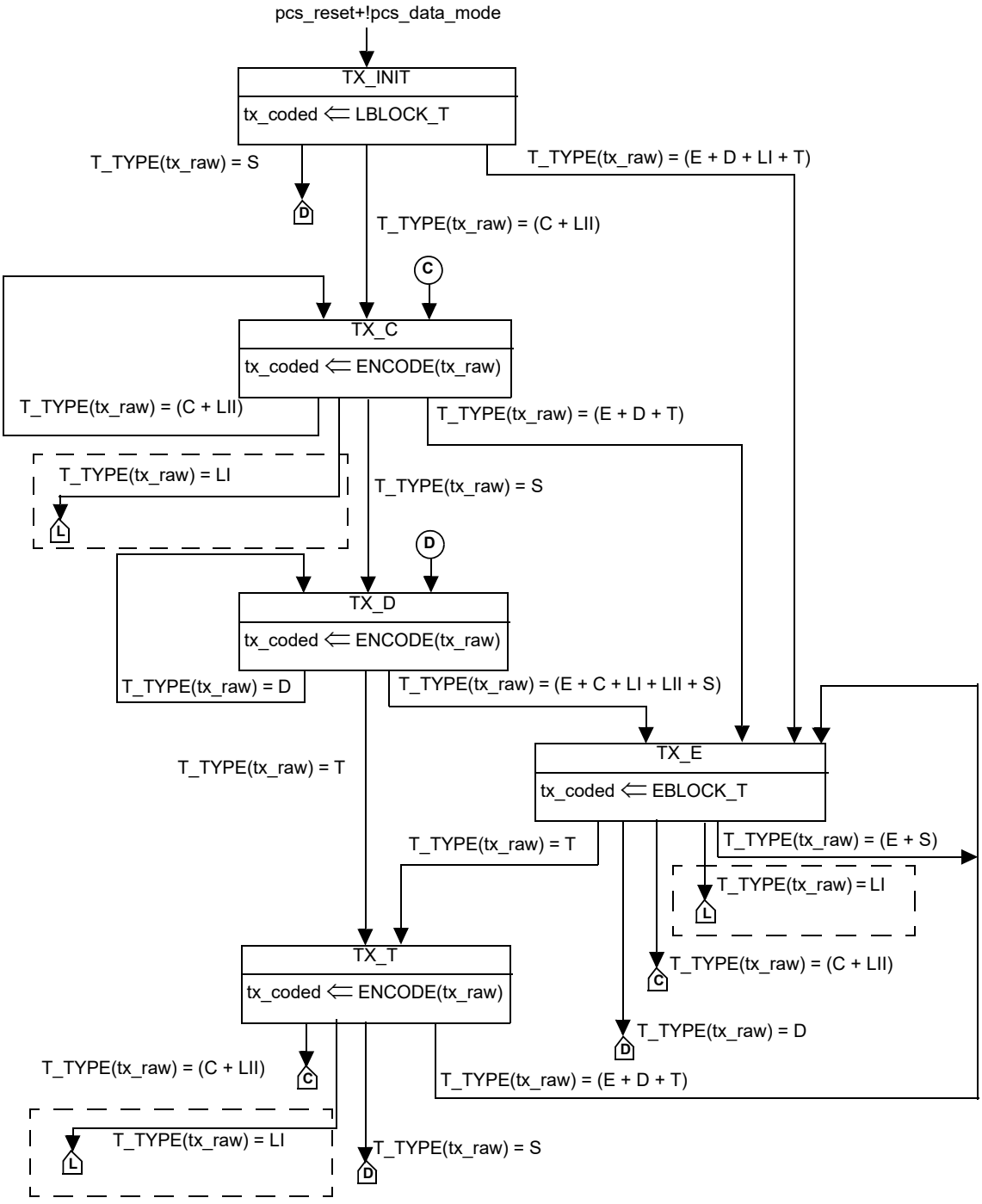

NOTE—Transitions inside dashed boxes are only required for the EEE capability.

Figure 113–18a—PCS 64B/65B Transmit state diagram, part a

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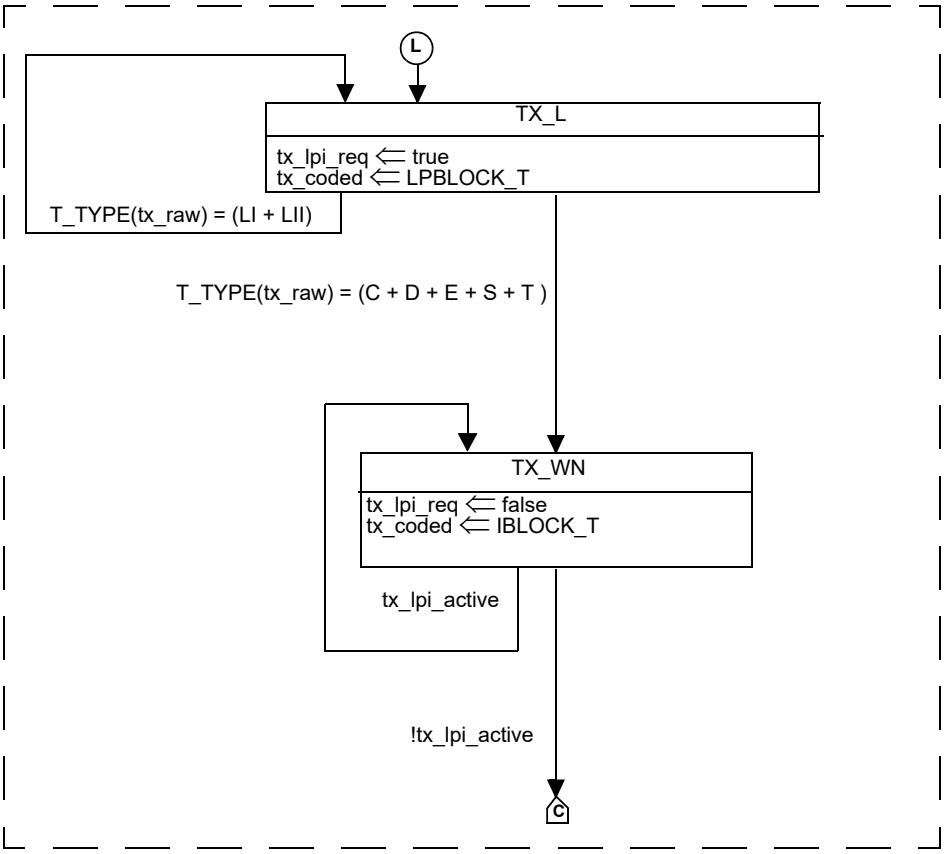

NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 113–18b—PCS 64B/65B Transmit state diagram, part b

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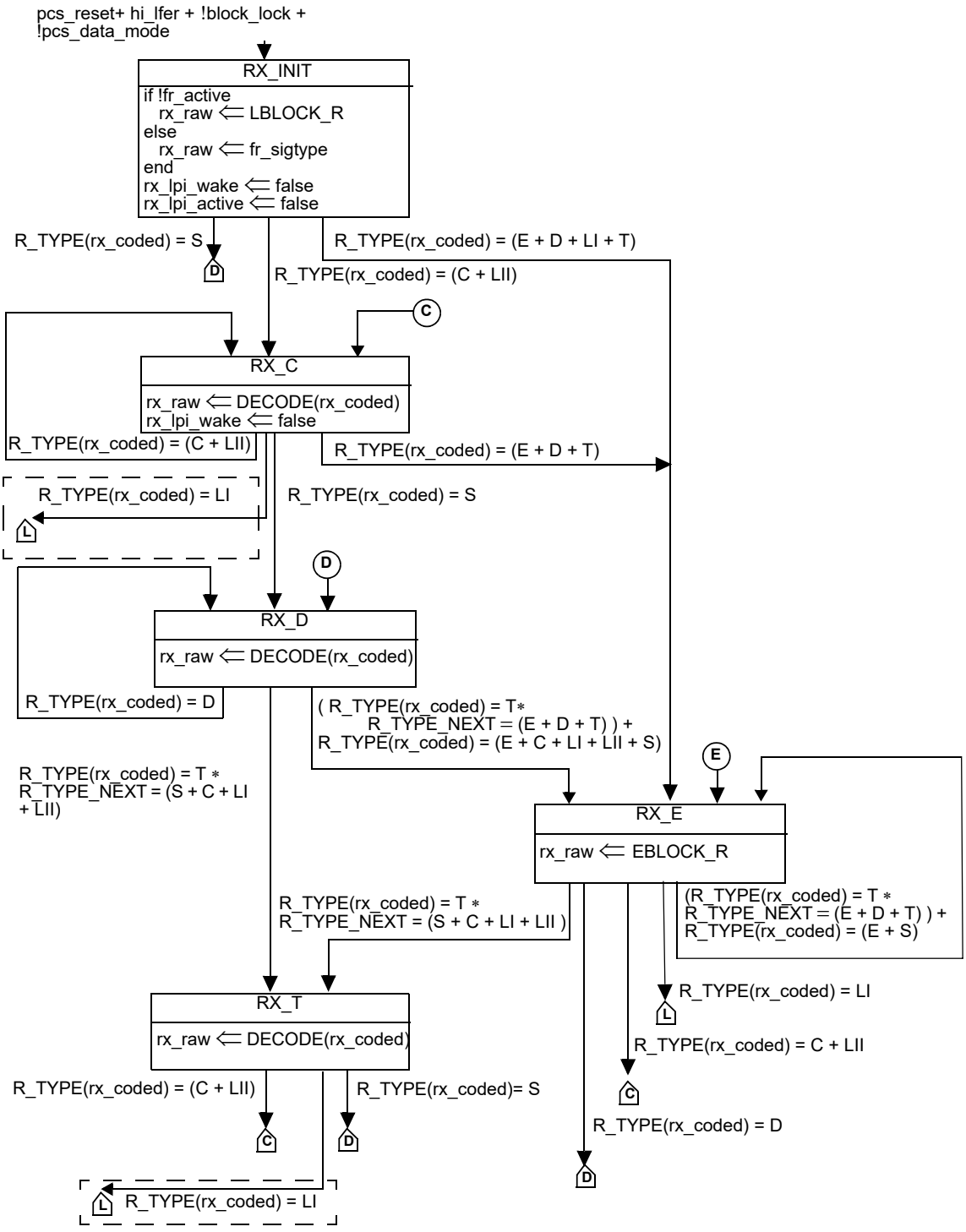

NOTE—Signals and functions shown with dashed lines are only required for the EEE capability.

Figure 113–19a—PCS 64B/65B Receive state diagram, part a

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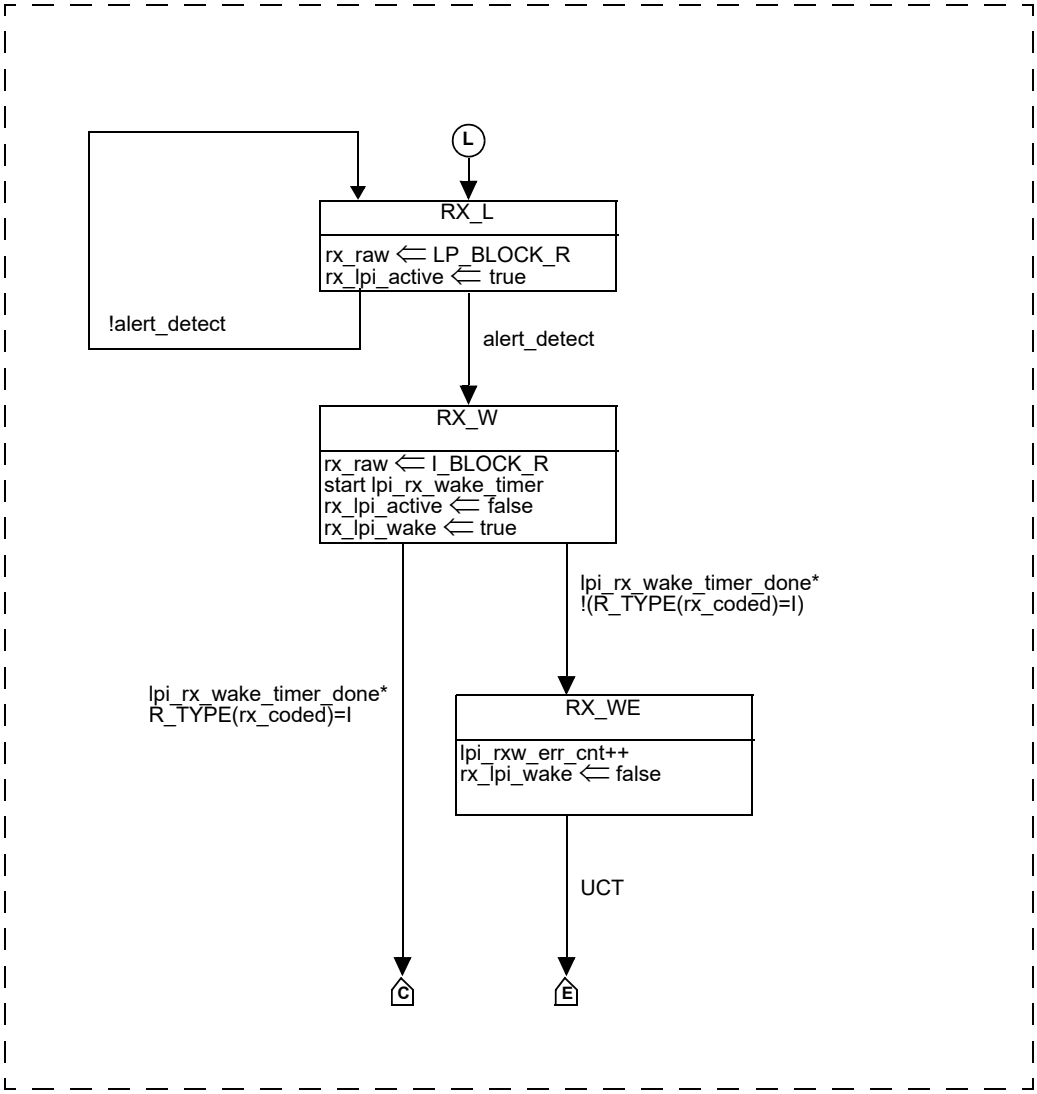

NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 113–19b—PCS 64B/65B Receive state diagram, part b

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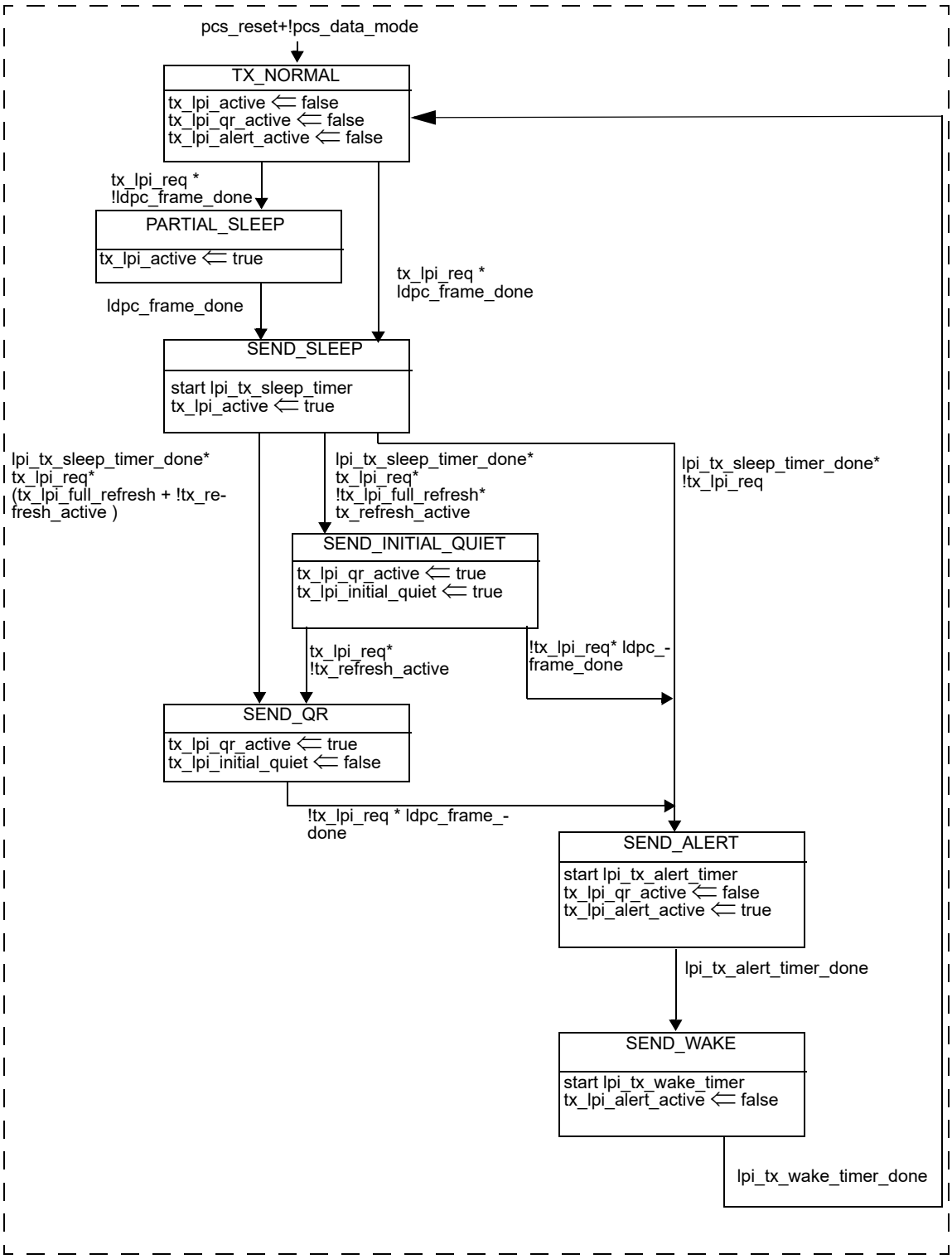

NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 113–20—EEE transmit state diagram

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113.3.7.3 Loopback

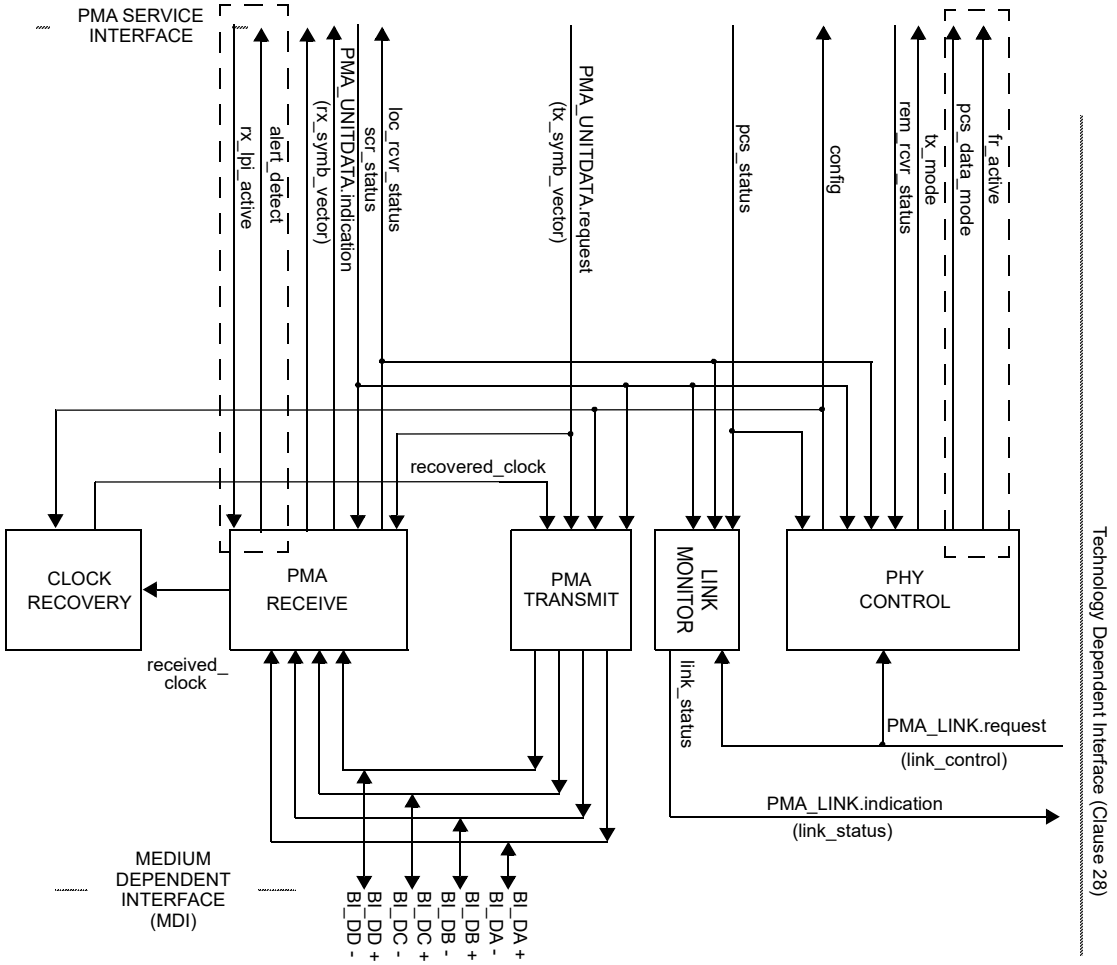
The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14 is set to a one. In this mode, the PCS shall accept data on the transmit path from the 25GMII/XLGMII and return it on the receive path to the 25GMII/XLGMII. In addition, the PCS shall transmit a continuous stream of 65B-LDPC encoded 4D-PAM16 symbols to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer.

113.4 Physical Medium Attachment (PMA) sublayer

113.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 113.2.2 to the 25G/40GBASE-T baseband medium, specified in 113.7.

The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 113.8.



NOTE 1—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

NOTE 2—pcs_data_mode is required only for the EEE or fast retrain capabilities alert_detect and rx_lpi_active are only required for the EEE capability fr_active is only required for the fast retrain capability.

Figure 113–21—PMA reference diagram

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113.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 113–21, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 113–21.

113.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power on (see 113.3.6.2.2)
b) The receipt of a request for reset from the management entity

All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

113.4.2.2 PMA Transmit function

The PMA Transmit function comprises four synchronous transmitters to generate four pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. While send_fail is FALSE and ALERT is not indicated by tx_symb_vector, PMA Transmit shall continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively, after processing with the THP, optional transmit filtering, digital to analog conversion (DAC), and subsequent analog filtering. When ALERT is indicated by tx_symb_vector, the alert signal is transmitted as specified in 113.4.2.2.1. When send_fail is TRUE, the link failure signal is transmitted as specified in 113.4.2.2.2. The four transmitters shall be driven by the same transmit clock, TX_TCLK. The signals generated by PMA Transmit shall follow the mathematical description given in 113.4.3.1 and shall comply with the electrical specifications given in 113.5.

When the PMA_CONFIG.indication parameter config is MASTER, for both normal and LPI operation, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 113.5.3.3. The MASTER/SLAVE relationship includes loop timing. If the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 113.4.2.8 while meeting the jitter requirements of 113.5.3.3.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

EEE-capable PHYs shall implement a PMA Transmit function that generates the alert signal as defined in 113.4.2.2.1. PHYs that support the fast retrain capability shall implement a PMA Transmit function that generates the link failure signal as defined in 113.4.2.2.2. If ALERT is indicated by tx_symb_vector at the same time as send_fail is TRUE, then link failure signaling is transmitted.

113.4.2.2.1 Alert signal

PHYs that support the optional EEE capability transmit the following PAM2 sequence when the PMA_UNITDATA.request parameter is set to ALERT. The alert signal is sent for a total of 4 LDPC frame

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periods and begins on a LDPC frame boundary. The alert signal is transmitted without THP filtering. The alert signal is transmitted on pair A when the PHY operates as a MASTER. The alert signal is transmitted on pair C when the PHY operates as a SLAVE. All other pairs transmit quiet as described in 113.3.5.

When the PMA_CONFIG.indication(config) is MASTER, the alert signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xpr_master =

9 9 –9 –9 –9 –9 –9 –9 9 9 –9 –9 9 9 9 9

9 9 9 9 –9 –9 9 9 9 9 –9 –9 9 9 –9 –9

–9 –9 –9 –9 –9 –9 9 9 –9 –9 –9 –9 –9 –9 9 9

–9 –9 –9 –9 –9 –9 –9 –9 9 9 –9 –9 9 9 –9 –9

–9 –9 9 9 9 9 9 9 9 9 9 9 –9 –9 –9 –9

9 9 –9 –9 –9 –9 9 9 9 9 –9 –9 9 9 –9 –9

–9 –9 –9 –9 –9 –9 –9 –9 9 9 9 9 –9 –9 9 9

9 9 –9 –9 9 9 –9 –9 9 9 9 9 –9 –9 –9 –9

When the PMA_CONFIG.indication(config) is SLAVE, the alert signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols:

xpr_slave =

–9 –9 –9 –9 9 9 9 9 –9 –9 9 9 –9 –9 9 9

9 9 –9 –9 9 9 9 9 –9 –9 –9 –9 –9 –9 –9 –9

–9 –9 9 9 –9 –9 9 9 9 9 –9 –9 –9 –9 9 9

–9 –9 –9 –9 9 9 9 9 9 9 9 9 9 9 –9 –9

–9 –9 9 9 –9 –9 9 9 –9 –9 –9 –9 –9 –9 –9 –9

9 9 –9 –9 –9 –9 –9 –9 9 9 –9 –9 –9 –9 –9 –9

–9 –9 9 9 –9 –9 9 9 9 9 –9 –9 9 9 9 9

9 9 9 9 –9 –9 9 9 –9 –9 –9 –9 –9 –9 9 9

The alert signal is followed by a wake signal composed of repeated IDLE characters encoded using the mixed 512B/513B 64B/65B RS-FEC and LDPC encoding used in normal data mode. At the start of the wake signal all THP feedback delay lines are initialized with zeros.

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113.4.2.2.2 Link failure signal

PHYs that support the fast retrain capability transmit the link failure signal under the control of the Fast Retrain state diagram. The link failure signal indicates to the link partner that a link failure has been detected and that the link partners should begin the fast retrain procedure.

The link failure signal is sent for 4 LDPC frames and begins on a LDPC frame boundary. The link failure signal is transmitted without THP filtering. The link failure signal is transmitted on pair A when the PHY operates as a MASTER. The link failure signal is transmitted on pair C when the PHY operates as a SLAVE. All other pairs transmit quiet as described in 113.3.5.

When the PMA_CONFIG.indication(config) is MASTER, the link failure signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xfr_master = xpr_master × (–1)

When the PMA_CONFIG.indication(config) is SLAVE, the link failure signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xfr_slave = xpr_slave × (–1)

113.4.2.3 PMA transmit disable function

113.4.2.3.1 Global PMA transmit disable function

The Global_PMA_transmit_disable function allows all of the transmitters to be disabled, when either:

a) When a Global_PMA_transmit_disable variable is set to TRUE, this function shall turn off all of the transmitters so that the each transmitter Average Launch Power of the OFF Transmitter is less than –53 dBm.
b) If a PMA_transmit_fault is detected, then the PMA may set the Global_PMA_transmit_disable to TRUE, turning off the transmitter on each pair.

113.4.2.3.2 PMA pair by pair transmit disable function

The PMA_transmit_disable function allows the transmitters on each pair to be selectively disabled.

When a PMA_transmit_disable_N variable is set to TRUE, this function shall turn off the transmitter associated with that variable so that the transmitter Average Launch Power of the OFF Transmitter is less than –53 dBm.

113.4.2.3.3 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 113–9. Mapping of MDIO status variables to PMA status variables is shown in Table 113–10.

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Table 113–9—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	Control register 1	1.0.15	PMA_reset
Global PMD transmit disable	Transmit disable register	1.9.0	Global_PMA_transmit_disable
Transmit disable pair D	Transmit disable register	1.9.4	PMA_transmit_disable_D
Transmit disable pair C	Transmit disable register	1.9.3	PMA_transmit_disable_C
Transmit disable pair B	Transmit disable register	1.9.2	PMA_transmit_disable_B
Transmit disable pair A	Transmit disable register	1.9.1	PMA_transmit_disable_A

Table 113–10—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Fault	Status register 1	1.1.7	PMA_fault
Transmit fault	Status register 2	1.8.11	PMA_transmit_fault
Receive fault	Status register 2	1.8.10	PMA_receive_fault

113.4.2.4 PMA Receive function

The PMA Receive function comprises four independent receivers for pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. The PMA Receive function contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over receive pairs BI_DA, BI_DB, BI_DC, and BI_DD and to present these sequences to the PCS Receive function. The signals received at the MDI are described mathematically in 113.4.3.2. The PMA translates the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD into the PMA_UNITDATA.indication parameter rx_symb_vector. The quality of these symbols shall allow an LFER of less than 3.2×10^{-9} after RS-FEC and LDPC decoding, over a link segment meeting the requirements of 113.7. The receiver shall correct for differential delay variations of up to 17 ns across the wire pairs. The delay skew is removed by computing the relative received delay of the four known transmit patterns described in 113.3.4.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization, echo, and crosstalk cancellation. The sequence of code-groups assigned to tx_symb_vector is needed to perform echo and self near-end crosstalk cancellation.

The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, estimation, and LPI functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

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The receiver uses the sequence of symbols during the training sequence to detect and correct for pair swaps and crossovers. The receiver pairs BI_DA, BI_DB, BI_DC, and BI_DD may be connected in any manner described in 113.4.4 to the corresponding transmit pairs. The receiver also detects and corrects for polarity mismatches on any pairs and corrects for differential delay variations across the wire pairs.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5.

PMA receive functions that support the optional EEE capability shall generate alert_detect when the alert signal is detected at the receiver. The PMA receive function asserts alert_detect after the entire alert signal (3.5 LDPC frame periods of the xpr_master or xpr_slave sequence and 0.5 frames of silence) has been detected. The alert signal is specified in 113.4.2.2.1. The criterion used to generate alert_detect is left to the implementer.

PHYs that support the fast retrain capability shall set link_fail_detect to TRUE when the link failure signal is reliably detected at the receiver. The PMA receive function asserts link_fail_detect after the entire link failure signal (3.5 LDPC frame periods of the xfr_master or xfr_slave sequence and 0.5 frames of silence) has been detected. The link failure signal is specified in 113.4.2.2.2. The criterion used to generate link_fail_detect is left to the implementer. It is highly recommended that the generation of link_fail_detect is qualified with repeated errored frames at the LDPC decoder output.

113.4.2.5 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 113–28.

During PMA training (includes PMA_Training_Init_M, PMA_Training_Init_S, PMA_PBO_Exch, PMA_Coeff_Exch, and PMA_Fine_Adjust states in Figure 113–28), PHY Control information is exchanged between link partners with a 16 octet Infofield, which is XOR'ed with the last 128 bits of the PMA 16384 PAM2 frame on pair A (see Figure 113–15). The link partner is not required to decode every Infofield transmitted but is required to decode Infofields at a rate that enables the correct actions to timer expiration times, transition counter values, etc. described in Figure 113–28, Figure 113–29, and Figure 113–30.

The 16-octet Infofield shall include the fields in 113.4.2.5.2 through 113.4.2.5.14, also shown in the overview Figure 113–22, and the more detailed Figure 113–23, Figure 113–24, and Figure 113–25.

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Message Field Dependent	Message Field Dependent	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	4 octets	2 octets

Figure 113–22—Infofield format

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Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Mes-sage Field	SNR Margin	Reser-ved	Transition Counter	Reser-ved/ Ability	Vendor Specific	CRC16
4 octets	3 octets	1 octet	4 bits	2 bits	10 bits	2 octets	2 octets	2 octets

Figure 113–23—Infofield transition counter format

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Coefficient Exchange	Coefficient Field	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	4 octets	2 octets

Figure 113–24—Infofield coefficient exchange format

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Mes-sage Field	SNR Margin	Reserved	Reserved /Ability	Vendor Specific	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	2 octets	2 octets	2 octets

Figure 113–25—Infofield not transition counter and not coefficient exchange format

113.4.2.5.1 Infofield notation

For all the Infofield notation in the following subclauses, Reserved<bit location> represents any unused values and shall be set to zero and ignored by the link partner. For all PBO Infofield values in the following subclauses, the PBO<6:4> are unsigned three-bit values 000, 001, 010, 011, 100, 101, 110, and 111 shall indicate power backoffs of 0 dB, 2 dB, 4 dB, 6 dB, 8 dB, 10 dB, 12 dB, and 14 dB, respectively. The Infofield is transmitted following the notation described in 113.3.2.2.3 where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Octet 1 is sent first).

113.4.2.5.2 Start of Frame Delimiter

The start of Frame Delimiter consist of 4 octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<7:0>, Octet 4<7:0>] and shall use the hexadecimal value 0xBBA70000. 0xBB corresponds to Octet 1<7:0> and so forth.

113.4.2.5.3 Current transmitter settings

Current transmitter setting (1 octet). Represented by Octet 5{Valid<7>, PBO<6:4>, Reserved<3:0>} and shown in Figure 113–26. Used to announce the current fixed PBO setting during PMA_Training_Init_M, PMA_Training_Init_S, and PMA_PBO_Exch, and the current programmable PBO setting during PMA_Coeff_Exch. For every other state this octet is set to zero and ignored by the link partner. The bit Valid

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shall be set to one if the corresponding octet information is valid and shall be set to zero if it the octet information is not valid. If Valid is set to zero, the octet is ignored by the link partner.

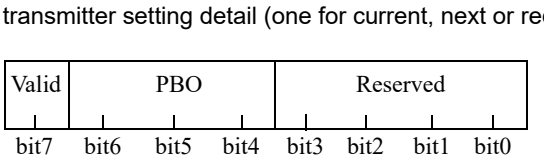

Figure 113–26—Infofield transmitter setting format

113.4.2.5.4 Next transmitter settings

Next transmitter setting (1 octet). Represented by Octet 6{Valid<7>, PBO<6:4>, Reserved<3:0>} and shown in Figure 113–26. Used to announce the next programmable PBO setting during PMA_PBO_Exch that takes effect upon entering PMA_Coeff_Exch state. For every other state, this octet is set to zero and ignored by the link partner. The bit Valid shall be set to one if the corresponding octet information is valid and shall be set to zero if it the octet information is not valid. If Valid is set to zero, the octet is ignored by the link partner.

113.4.2.5.5 Requested transmitter settings

Requested remote transmitter setting (1 octet). Represented by Octet 7{Valid<7>, PBO<6:4>, Reserved<3:0>} and shown in Figure 113–26. Used to request the remote transmitter programmable PBO setting during PMA_PBO_Exch that takes effect upon entering PMA_Coeff_Exch state. For every other state, this octet is set to zero and ignored by the link partner. The bit Valid shall be set to one if the corresponding octet information is valid and shall be set to zero if it the octet information is not valid. If Valid is set to zero, the octet is ignored by the link partner.

113.4.2.5.6 Message Field

Message Field (1 octet). For the MASTER, this field is represented by Octet 8{PMA_state<7:6>, loc_rcvr_status<5>, en_slave_tx<4>, trans_to_Coeff_Exch<3>, Coeff_exchange<2>, trans_to_Fine_Adjust<1>, trans_to_PCS_Test<0>}. For the SLAVE, this field is represented by Octet 8{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, trans_to_Coeff_Exch<3>, Coeff_exchange<2>, trans_to_Fine_Adjust <1>, trans_to_PCS_Test<0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6>=00 indicates PMA_Training_Init_M or PMA_Training_Init_S, PMA_state<7:6>=01 indicates PMA_PBO_Exch, PMA_state<7:6>=10 indicates PMA_Coeff_Exch, and PMA_state<7:6>=11 indicates PMA_Fine_Adjust.

All possible Message Field settings are listed in Table 113–11 for the MASTER and Table 113–12 for the SLAVE. No other value shall be transmitted, and all other values shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 113–11 for the MASTER and the first row of Table 113–12 for the SLAVE. Moreover, for a given Message Field setting, the following Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status=OK the Infofield variable is set to loc_rcvr_status<5>=1 and set to 0 otherwise.

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Table 113–11—Infofield message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_ status	en_slave_tx	trans_to_ Coeff_Exch	Coeff_ exchange	trans_to_ Fine_Adjust	trans_to_ PCS_Test
00	0	0	0	0	0	0
00	0	1	0	0	0	0
01	0	1	0	0	0	0
01	0	1	1	0	0	0
10	0	1	0	0	0	0
10	0	1	0	1	0	0
10	0	1	0	0	0	0
10	0	1	0	0	1	0
11	0/1	1	0	0	0	0
11	1	1	0	0	0	1

Table 113–12—Infofield message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_ status	timing_lock _OK	trans_to_ Coeff_Exch	Coeff_ exchange	trans_to_ Fine_Adjust	trans_to_ PCS_Test
00	0	0	0	0	0	0
00	0	0/1	0	0	0	0
01	0	1	0	0	0	0
01	0	1	1	0	0	0
10	0	0/1	0	0	0	0
10	0	1	0	1	0	0
10	0	1	0	0	0	0
10	0	1	0	0	1	0
11	0	0/1	0	0	0	0
11	0/1	1	0	0	0	0
11	1	1	0	0	0	1

113.4.2.5.7 SNR_margin

SNR_margin (4 bits). Represented by Octet 9<7:4>, which reports received decision point SNR margin in 1/2 dB steps. SNR_margin is relative to the SNR required for reception of LDPC-coded DSQ128 at an LDPC frame error ratio of less than 3.2×10^{-9}. The SNR_margin<7:4> four-bit values, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110 shall indicate the decision point SNR margin

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values of –1.5, –1, –0.5, 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5 dB, respectively. The value 0001 shall indicate a margin of –2 dB or less, and the value 1111 shall indicate 5 dB or more. Finally the value 0000 shall indicate that the SNR margin value is unknown.

113.4.2.5.8 Transition counter

Transition counter (10 bits). Represented by the 1.25 octets [Octet 9<1:0>, Octet 10<7:0>]. When configured as Transition counter (Coeff_exchange<2>=0 and a transition is announced to PMA_Coeff_Exch, PMA_Fine_Adjust or PCS_Test), this field is used as a 10-bit counter that counts the number of remaining frames until the next transition (PMA_Coeff_Exch, PMA_Fine_Adjust, PCS_Test).

113.4.2.5.9 Coefficient exchange handshake

Coefficient exchange handshake (12 bits). Represented by the 1.5 octets [Octet 9<3:0>, Octet 10<7:0>]. If Coeff_exchange<2>=1, this field is configured as a Coefficient exchange handshake and is used as a handshake control channel during programmable THP coefficient exchange. The details of the coefficient exchange are described in 113.4.2.5.15.

113.4.2.5.10 Ability Fields

Ability field (1 octet). Represented by Octet 12{EEE Ability<7>, THP Bypass Request<6>, Fast Retrain<5>, Reserved<4:0>}. Used to advertise the abilities of the PHY during the PMA_PBO_Exch state when Message<7:6> = 01.

For every other state, this octet is set to zero and ignored by the link partner. The Ability bits are defined as follows:

Octet 12<4:0> = Reserved

Octet 12<5> = Fast Retrain

0 = Fast Retrain not supported

1 = Fast Retrain supported

Octet 12<6> = THP Bypass Request in PMA_Coeff_Exchstate

0 = Local device requests link partner not to bypass THP during fast retrain

1 = Local device requests link partner to bypass THP during fast retrain

Octet 12<7> = EEE Ability

0 = EEE not supported

1 = EEE supported.

113.4.2.5.11 Reserved fields

All Infofield fields denoted Reserved in Figure 113–23, Figure 113–24, and Figure 113–25 are reserved for future use. This includes Octet 11 and Octet 12 when Coeff_exchange<2>=0 and Message<7:6>!=01, Octet 9<3:2> when transition counter is announced and [Octet 9<3:0>, Octet 10<7:0>] when no transition is announced and no coefficients are exchanged.

113.4.2.5.12 Vendor-specific field

If Coeff_exchange<2>=0 Octet 13 and Octet 14 are vendor-specific fields. If during Auto-Negotiation both transceivers agree on the use of the two vendor-specific octets, they may be used as a PHY communication

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channel; otherwise they are set to zero and ignored by the link partner. Represented by Octet 13<7:0> and Octet 14<7:0>.

113.4.2.5.13 Coefficient Field

Coefficient Field (4 octets). Represented by Octet 11<7:0>, Octet 12<7:0>, Octet 13<7:0>, and Octet 14<7:0>. When Coeff_exchange<2>=1, this field is used to exchange programmable THP coefficients. It transmits four 8-bit THP coefficients out of the total of 64 (16 coefficients over each of the 4 pairs). The order is pair A, coefficients 0:3, followed by coefficients 4:7, followed by 8:11 and 12:15. For all cases the first coefficient (indices 0, 4, 8 and 12) is mapped to Octet 11, the second coefficient (indices 1, 5, 9, 13) is mapped to Octet 12 and so on. The same coefficient order is followed to transmit the coefficients for pair B, followed by pair C, and finally pair D. The details of the coefficient exchange are described in 113.4.2.5.15.

113.4.2.5.14 CRC16

CRC16 (2 octets). Shall implement the CRC16 polynomial $(x+1)(x^{15}+x+1)$ of the previous 10 octets, Octet 5<7:0>, Octet 6<7:0>, Octet 7<7:0>, Octet 8<7:0>, Octet 9<7:0>, Octet 10<7:0>, Octet 11<7:0>, Octet 12<7:0>, Octet 13<7:0>, and Octet 14<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 113–27. In Figure 113–27 the 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards Octet 5 through Octet 14 are used to compute the CRC16 with the switch connected, which is setting CRCgen in Figure 113–27. After all the 10 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

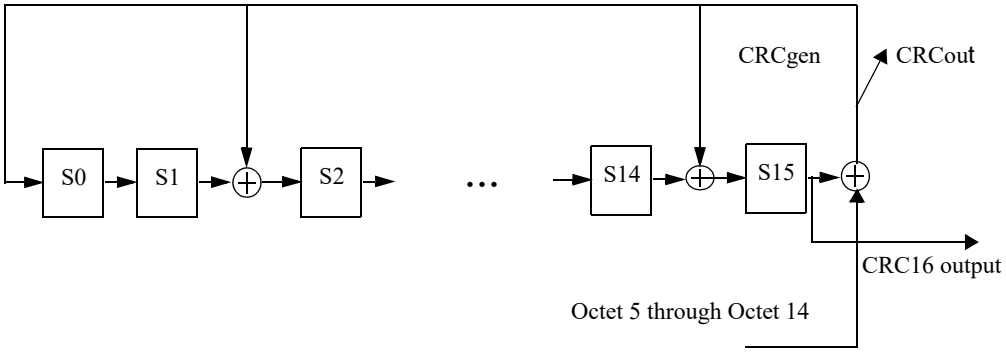

Figure 113–27—CRC16

113.4.2.5.15 Startup sequence

The startup sequence shall comply with the state diagram description given in Figure 113–28 and the transition counter state diagrams Figure 113–29 and Figure 113–30.

During Auto-Negotiation, PHY Control is in the DISABLE_25G/40GBASE-T_TRANSMITTER state and the transmitters are disabled. During normal training, prior to enabling the transmitter, the THP coefficients are set to zero.

When the Auto-Negotiation process asserts link_control=ENABLE, PHY Control enters the INIT_MAXWAIT_TIMER state. Upon entering this state, the maxwait_timer is started and PHY Control enters the SILENT state, which starts the minwait_timer and forces transmission of zeros by setting tx_mode=SEND_Z.

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In MASTER mode, after expiration of the minwait_timer, PHY Control transitions to the PMA_Training_Init_M state.

Upon entering the PMA_Training_Init_M and PMA_Training_Init_S states, the PHY Control forces transmission into the training mode by asserting tx_mode=SEND_T, which includes the transmission of Infofields.

Upon entering state PMA_Training_Init_M, the MASTER starts transmission with a fixed transmit power level, PBO=4 (corresponding to a power backoff of 8 dB). The PBO variable is communicated to the link partner via the current transmitter octet of the Infofield.

Initially the MASTER is not ready for the SLAVE to respond and sets en_slave_tx=0, which is communicated to the link partner via the Infofield. After the MASTER has sufficiently converged the necessary circuitry, the MASTER sets en_slave_tx=1 to allow the SLAVE to transition to PMA_Training_Init_S.

In SLAVE mode, PHY Control transitions to the PMA_Training_Init_S state only after the SLAVE PHY acquires timing, converges its equalizers, acquires its descrambler state, and sets loc_SNR_margin=OK. The SLAVE shall respond using the fixed PBO transmit power level, PBO=4 (corresponding to a power backoff of 8 dB). For PHYs with the EEE capability, further requirements for this transition are described in 113.3.5.1.

While in states PMA_Training_Init_S, PMA_PBO_Exch, or PMA_Coeff_Exch, whenever a SLAVE operating in loop timing mode loses the MASTER timing reference (for example, after transmit power level transitions) it sets timing_lock_OK=0, which is communicated to the link partner via the Infofield. Otherwise, timing_lock_OK is set to one.

In MASTER mode, PHY Control enters the PMA_PBO_Exch state after loc_SNR_margin=OK and in SLAVE mode PHY Control enters the PMA_PBO_Exch state after the loc_SNR_margin=OK and minwait_timer expires. In the PMA_PBO_Exch state while Infofield Message<7:6> = 01, the PHY advertises EEE and Fast Retrain capability in octet 12 of the Infofield. When both the local device and remote device advertise EEE capability then EEE is supported. When both the local device and remote device advertise Fast Retrain capability then Fast Retrain is supported. In the PMA_PBO_Exch state, after the MASTER has computed the final desired programmable PBO level, it shall request a PBO change using the requested transmitter setting in the Infofield (octet 7). In SLAVE mode, after the MASTER has requested the desired PBO level, the SLAVE shall request a desired PBO level that is within two levels (within 4 dB) of the requested MASTER PBO level. Both MASTER and SLAVE shall use the lower of the two PBO levels (i.e., that providing the larger transmit power).

Following PBO exchange for both transceivers, each PHY shall announce the next PBO setting using the next transmitter setting (octet 6). Afterwards, each PHY announces a transition to the PMA_Coeff_Exch state using the trans_to_Coeff_Exch=1 and transition_count as described in 113.4.5.1. MASTER initiates the transition to PMA_Coeff_Exch count with the trans_to_Coeff_Exch=1 flag and a transition counter value of 2^9. The SLAVE responds prior to the MASTER transition counter reaching 2^6 by setting trans_to_Coeff_Exch=1 flag and a transition counter value matching the MASTER. The PMA frame after each transceiver transition_count reaches zero, the PHYs shall enter the PMA_Coeff_Exch state and enable the requested PBO. Therefore, both PHYs will enter the PMA_Coeff_Exch state within one PMA frame.

While both MASTER and SLAVE are in state PMA_Coeff_Exch, when either end has computed the programmable THP settings, the programmable THP coefficient exchange process can begin, using the 1.5 octet Coefficient exchange handshake and the 4 octet Coefficient Field as follows:

a) During PMA_Coeff_Exch each PHY begins a coefficient exchange by setting the Coeff_Exchange flag to 1 in the Message Field.

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b) During coefficient exchange, the transition counter bits are used as the Coefficient Exchange Handshake
   1) Octet 9{Reserved<3:0>}: unused
   2) Coefficient Pair Received, Octet 10<7:6>: 01 for local transmitter pair A, 10 for B, 11 for C, and 00 for D (default). This is the handshake to tell the remote unit the last coefficients received.
   3) Coefficient Group Received, Octet 10<5:4>: 01 for coefficients 0:3, 10 for 4:7, 11 for 8:11, and 00 for 12:15 (default). This is the handshake to tell the remote unit the last coefficients received.
   4) Coefficient Pair Sent, Octet 10<3:2>: 01 for remote transmitter pair A, 10 for B, 11 for C, and 00 for D (default). This is the handshake to tell the remote unit the current coefficients being sent.
   5) Coefficient Group Sent, Octet 10<1:0>: 01 for 0:3, 10 for 4:7, 11 for 8:11, and 00 for 12:15 (default). This is the handshake to tell the remote unit the current coefficients being sent.
c) The Coefficient Field is used to send four 8-bit coefficients in each frame designated by the Coefficient Pair Sent and Coefficient Group Sent bits. The coefficient format is:
   1) 8 bits per coefficient. Use one octet per coefficient in twos complement notation
   2) Coefficient range is –2.0 to 1.984375 in steps of 0.015625
   3) The sign of the coefficients shall be consistent with Equation (113–6)
d) Each PHY begins the exchange by sending pair A coefficients 0:3 with Coefficient Pair Sent=01 and Coefficient Group Sent=01.
e) The remote unit acknowledges by setting Coefficient Pair Received=01 and Coefficient Group Received=01.
f) Following each acknowledgement, the PHY increments through the Coefficient Group and then Coefficient Pair settings until Coefficient Pair Sent=00 and Coefficient Group Sent=00 and Coefficient Pair Received=00 and Coefficient Group Received=00. At this time, coefficient exchange is done and both PHYs set Coeff_Exchange=0.

Following coefficient exchange for both transceivers, each PHY announces a transition to the PMA_Fine_Adjust state (trans_to_Fine_Adjust=1) and starts the transition_count as described in 113.4.5.1. During the first PMA frame after the transition_count reaches zero, the PHYs enter the PMA_Fine_Adjust state and enable the THP precoders with the requested coefficients. At the closure of the THP feedback loop, the initial state of the THP feedback filters shall be the last 16 symbols from the state PMA_Coeff_Exch.

The THP coefficients and PBO setting are not changed during PMA_Fine_Adjust. The final convergence of the adaptive filter parameters is completed in the PMA_Fine_Adjust state.

After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter Infofield value loc_rcvr_status. The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr_status. When the condition loc_rcvr_status=OK and rem_rcvr_status=OK is satisfied, each PHY announces a transition to the PCS_Test state (trans_to_PCS_Test=1) and start the transition counter as described in 113.4.5.1. For PHYs with the EEE capability, further requirements for this transition are described in 113.3.5.1.

The normal mode of operation corresponds to the PCS_Data state, where PHY Control asserts tx_mode=SEND_N and transmission of data over the link can take place.

PHY Control may force the transmit scrambler state to be initialized to an arbitrary value by requesting the execution of the PCS Reset function defined in 113.3.2.1.

The operation of the maxwait_timer requires that the PHY complete the startup sequence from state SILENT to PMA_Fine_Adjust in the PHY Control state diagram (Figure 113–28) in less than 2000 ms to

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avoid link_status being changed to FAIL by the Link Monitor state diagram (Figure 113–31). To ensure interoperability the timing in Table 113–13 should be observed.

After reaching the PCS_Data state PHYs with the EEE capability can transition to the LPI receive mode under the control of the link partner and to the LPI transmit mode under control of the local LPI client.

Table 113–13—Recommended startup sequence timing

Master	Recommended maximum time (ms)	Recommended average time (ms)	Slave
SILENT plus (PMA_Training_Init_M state AND en_slave_tx = 0)	350	315	SILENT
(PMA_Training_Init_M state AND en_slave_tx = 1) plus PMA_PBO_Exch state	480	432	PMA_Training_Init_S state plus PMA_PBO_Exch state
PMA_Coeff_Exch state	100	90	PMA_Coeff_Exch state with timing_lock_OK=0
	520	468	Total for PMA Coeff Exch state
PMA_Fine_Adjust state	650	585	PMA_Fine_Adjust state
Total	2000	1800	

113.4.2.5.16 Fast retrain function

PHYs that support the fast retrain capability shall implement the fast retrain state diagram shown in Figure 113–33. PHYs may request a fast retrain by setting the variable loc_fr_req to TRUE. This causes the transmission of an easily detected link failure signal specified in 113.4.2.2.2. After completing the link failure signal the PHY shall transition to the PMA_INIT_FR state followed immediately by the PMA_Coeff_Exch state. If the link partner requested THP bypass for fast retrain the PHY shall bypass the THP (or set THP coefficients to zero). Otherwise the PHY shall keep its THP turned on with its previously exchanged coefficients, and send PAM2 signaling within a time period equivalent to 9 LDPC frame periods.

After the detection of the link failure signal, a PHY shall transition to the PMA_Coeff_Exch state and respond with PAM2 signaling within a time period equivalent to 9 LDPC frame periods after receiving the link failure signal.

The PAM2 symbols are generated using the PMA sidestream scrambler polynomials shown in Figure 113–15. The training sequence in 113.3.4 shall be used during fast retraining.

Note that reliable traffic on the transmitter may be interrupted when the local receiver requests a fast retrain.

Following the link failure signal, the two link partners transition back to the PMA_Coeff_Exch state and follow the training procedure described in 113.4.2.5.15, with the exception that the initial infofield countdown values are reduced as indicated in Figure 113–29 and Figure 113–30.

To ensure interoperability the training times in Table 113–14 should be observed during the fast retrain.

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Table 113–14—Recommended fast retrain sequence timing

State	Recommended maximum time (ms)
PMA_Coeff_Exch state	20
PMA_Fine_Adjust state	10

113.4.2.6 Link Monitor function

Link Monitor determines the status of the receiver and communicates it via the variable link_status. Failure of the receiver typically causes the PMA's clients to suspend normal operation.

The Link Monitor function shall comply with the state diagram of Figure 113–31.

Upon power on, reset, or release from power down, the Auto-Negotiation algorithm sets link_control=SCAN_FOR_CARRIER and, during this period, sends fast link pulses to signal its presence to a remote station. If the presence of a remote station is sensed through reception of fast link pulses, the Auto-Negotiation algorithm sets link_control=DISABLE and exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. If the presence of a remote 25G/40GBASE-T station is established, the Auto-Negotiation algorithm permits full operation by setting link_control=ENABLE. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

113.4.2.7 Refresh Monitor function

The Refresh Monitor is required for PHYs that support the EEE capability. The Refresh Monitor operates when the PHY is in the LPI receive mode. The Refresh Monitor shall comply with the state diagram of Figure 113–19b. The function forces a link retrain if a refresh signal is not reliably detected within a moving time window equivalent to 50 complete quiet-refresh cycles (nominally equal to 2.048 ms), when the PHY is in the lower power receive mode.

113.4.2.8 Clock Recovery function

The Clock Recovery function couples to all four receive pairs. It may provide independent clock phases for sampling the signals on each of the four pairs.

The Clock Recovery function shall provide clocks suitable for signal sampling on each line so that the LDPC FER indicated in 113.4.2.4 is achieved. The received clock signal should be stable and ready for use when training has been completed (loc_rcvr_status=OK). The received clock signal is supplied to the PMA Transmit function by received_clock.

113.4.3 MDI

Communication through the MDI is summarized in 113.4.3.1 and 113.4.3.2.

113.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA on the four pairs BI_DA, BI_DB, BI_DC, and BI_DD are denoted by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively. The modulation scheme used over each pair is PAM16. PMA Transmit generates a pulse-amplitude modulated signal on each pair in the following form:

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$$x_n = M\left(a_n - \sum_{k=1}^{16} x_{n-k}c_k\right) = a_n + 32m_n - \sum_{k=1}^{16} x_{n-k}c_k \quad (113\text{–}6)$$

$$s(t) = \sum_{n=0}^{\infty} x_n h_T(t - nT) \quad (113\text{–}7)$$

In Equation (113–6), a_n is the PAM16 modulation symbol from the set {–15, –13, –11, –9, –7, –5, –3, –1, 1, 3, 5, 7, 9, 11, 13, 15} to be transmitted at time nT. Each of the 16 THP coefficients c_1, c_2,..., c_{16} per wire pair is represented in two's complement form by 8 bits described in 113.4.2.5. The nonlinear THP operation given by $M(\alpha) = (\alpha + 16) mod 32 - 16$ corresponds to changing the modulation symbol a_n to an augmented modulation symbol $\tilde{a}_n = a_n + 32m_n$ with the integer m_n chosen such that the THP output lies in the interval $-16 \le x_n < 16$. Equation (113–7) describes the convolution of the THP output signals with the transmitter symbol response $h_T(t)$ to obtain the transmit signal $s(t)$ at the MDI. The values of the programmable THP coefficients are exchanged in the Infofield during PMA_Coeff_Exch. The THP filter coefficients shall be fixed after startup.

The nominal power (denoted Ptx) and the symbol response of the PMA transmitted signal $s(t)$ shall comply with the electrical specifications given in 113.5. When the link segment does not experience the maximum insertion loss (IL), each transceiver indicates to the link partner that the link partner PMA Transmit signal shall be reduced in increments of 2 dB. The minimum power backoff level requested shall comply with the power backoff schedule in Table 113–15. If a given receiver has sufficient decision point SNR margin, it may choose to request from the link partner larger power backoff (up to 14 dB) than shown in Table 113–15. Additionally, the Slave shall select a PBO level as described in the PMA_PBO_Exch state of 113.4.2.5.15. The PMA Transmit shall be capable of eight power backoff settings in approximately 2 dB steps. The difference between each consecutive power setting shall be 2 ± 0.25 dB, and each step shall be centered at $2 \times n$ dB (n = 0 to 7) reduction from nominal, with a maximum error of ± 1 dB.

The received signal power at the MDI, P (dBm), in Table 113–15, should be the estimate of the average received power across all four pairs from the remote transmitter when the link partner PMA Transmit is at nominal power (after accounting for local transmitter power). If the remote transmitter is not at nominal power during the measurement, the estimate of the received power should be incremented by the amount of power backoff of the link partner transmitter during the measurement. Nominal power refers to the transmit power without any power backoff and is specified in 113.5.3.4. The estimate of the received signal power is stored in registers 1.141 to 1.144 as described in 45.2.1. The values in the length, L (m), column in Table 113–15 are for reference only (not required for power backoff evaluation).

Table 113–15—Power backoff schedule

Received signal power at MDI, P (dBm)	Length L(m) (reference)	Minimum power backoff (dB)
$-7.2 < P$	$0 \le L < 13$	6
$-9.4 < P \le 7.2$	$13 \le L < 19$	4
$-11.4 < P \le -9.4$	$19 \le L < 25$	2
$P \le -11.4$	$25 \le L$	0

113.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise as follows:

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$$r(t) = \sum_{n=0}^{\infty} \tilde{a}_n h_R(t - nT) + w(t) \quad (113–8)$$

In Equation (113–8), $\tilde{a}_n$ are the augmented PAM16 modulation symbols described in 113.4.3.1, $h_R(t)$ denotes the symbol response of the overall signal path from the THP precoder to the MDI at the receiver, and $w(t)$ represents the contribution of various noise sources including uncancelled crosstalk. The four signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD are processed within the PMA Receive function to yield the received symbols rx_symb_vector.

113.4.4 Automatic MDI/MDI-X configuration

Automatic MDI/MDI-X configuration is intended to eliminate the need for crossover cables between similar devices. Automatic MDI/MDI-X configuration is required for 25G/40GBASE-T devices and shall comply with 40.4.4.1 and 40.4.4.2.

Having established MDI/MDI-X configuration, the receiver shall detect and correct for several configurations of pair swaps and crossovers and arbitrary polarity swaps. The receiver pairs BI_DA, BI_DB, BI_DC, and BI_DD might be connected to the corresponding transmit pairs in any of the following ways with arbitrary polarity:

a) No crossover
b) A/B crossover only
c) C/D crossover only
d) A/B crossover and C/D crossover

For EEE-capable PHYs, the MDI/MDIX function configuration shall apply to refresh and alert signaling. For PHYs with the fast retrain capability, the MDI/MDIX function configuration shall apply to link failure signaling.

113.4.5 State variables

113.4.5.1 State diagram variables

coeff_exchange_done
: This variable reports that both transceivers have received the corresponding coefficients from the link partner.
Values: TRUE: The coefficient exchange has completed.
FALSE: The coefficient exchange has not completed.

config
: The PMA shall generate this variable continuously and pass it to the PCS via the PMA_CONFIG.indication primitive.
Values: MASTER or SLAVE

link_control
: The link_control parameter generated by Auto-Negotiation and passed to the PMA via the PMA_LINK.request primitive (see 113.2.1.1)

link_status
: The link_status parameter set by PMA Link Monitor state diagram and communicated through the PMA_LINK.indication primitive.
Values: OK or FAIL

loc_rcvr_status
: Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY.
Values: OK: The receive link for the local PHY is operating reliably.
NOT_OK: Operation of the receive link for the local PHY is unreliable.

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loc_SNR_margin

This variable reports whether the local device has sufficient SNR margin to continue to the next state. The criterion for setting the parameter loc_SNR_margin is left to the implementer.

Values: OK: The local device has sufficient SNR margin.
NOT_OK: The local device does not have sufficient SNR margin.

master_transition_counter

This variable reports the current value of the MASTER's transition counter reported in the Infofield defined in 113.4.2.5.

Values: 0 to 2^9

MessageField_IF

This variable reports that a receiver has successfully received and decoded the Infofield from the remote device. This variable takes on the value contained in the Message Field. If the Message Field cannot be decoded or no explicit action is outstanding the value Null is returned.

Values: trans_to_Coeff_Exch, trans_to_Fine_Adjust, trans_to_PCS_Test or Null

PBO

PBO is a variable that can take any integer value from 0 to 7 and indicates the power backoff level. Denoting Ptx as the maximum nominal power, the PBO values are:

Values: 0, 1, 2, 3, 4, 5, 6, 7, which correspond to transmit power levels of
Ptx, *Ptx*–2 dB, *Ptx*–4 dB, *Ptx*–6 dB, *Ptx*–8 dB, *Ptx*–10 dB, *Ptx*–12 dB, *Ptx*–14 dB, respectively

PBO_next

PBO_next is a variable that can take any integer value from 0 to 7 and indicates the next power backoff level to be used at the local transmitter. The value is taken from the fixed set of values during PMA_Training_Init_M and PMA_Training_Init_S as described in 113.4.2.5. The value is taken from the decoded value of the link partner Infofield during PMA_PBO_Exch

Values: 0, 1, 2, 3, 4, 5, 6, 7, which correspond to transmit power levels of
Ptx, *Ptx*–2 dB, *Ptx*–4 dB, *Ptx*–6 dB, *Ptx*–8 dB, *Ptx*–10 dB, *Ptx*–12 dB, *Ptx*–14 dB, respectively

PBO_tx

PBO_tx is a variable that can take any integer value from 0 to 7 and indicates the power backoff level currently used at the local transmitter.

Values: 0, 1, 2, 3, 4, 5, 6, 7, which correspond to transmit power levels of
Ptx, *Ptx*–2 dB, *Ptx*–4 dB, *Ptx*–6 dB, *Ptx*–8 dB, *Ptx*–10 dB, *Ptx*–12 dB, *Ptx*–14 dB, respectively

PBO_exchange_done

This variable reports that both transceivers have received the corresponding PBO levels from the link partner.

Values: TRUE: The PBO exchange has completed.
FALSE: The PBO exchange has not completed.

pcs_status

The pcs_status parameter generated by the PCS and passed to the PMA via the PMA_PCSTATUS.request primitive (see 113.2.2.6).

pma_reset

Allows reset of the PHY Control and Link Monitor state diagrams.

Values: ON or OFF

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not.

Values: OK: The receive link for the remote PHY is operating reliably.
NOT_OK: Reliable operation of the receive link for the remote PHY is not detected.

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THP_next

THP_next is a variable that contains sixteen eight-bit values and describes the next transmitter setting of the THP coefficients. It refers to the programmable THP coefficients selected during coefficient exchange described in 113.4.2.5.

Values: 16 coefficients of 8-bit values each. Range is –2.0 to 1.984375 in steps of 0.015625

THP_tx

THP_tx is a variable that contains sixteen 8-bit values and describes the current transmitter setting of the THP coefficients. It refers to the programmable THP coefficients selected during coefficient exchange described in 113.4.2.5.

Values: 16 coefficients of eight-bit values each. Range is –2.0 to 1.984375 in steps of 0.015625

trans_to_Coeff_Exch

Message field variable defined in 113.4.2.5 that flags a transition by the local device to the PMA_Coeff_Exch state.

Values: 1: The local device transitions to the PMA_Coeff_Exch state on expiration of the transition counter.

0: The local device does not transition to the PMA_Coeff_Exch state.

trans_to_Fine_Adjust

Message field variable defined in 113.4.2.5 that flags a transition by the local device to the PMA_Fine_Adjust state.

Values: 1: The local device transitions to the PMA_Fine_Adjust state on expiration of the transition counter.

0: The local device does not transition to the PMA_Fine_Adjust state.

trans_to_PCS_Test

Message field variable defined in 113.4.2.5 that flags a transition by the local device to the PCS_Test state.

Values: 1: The local device transitions to the PCS_Test state on expiration of the transition counter.

0: The local device does not transition to the PCS_Test state.

transition_count

This variable reports the value of the transition counter contained in the Infofield sent to the remote device. Transition_count has to comply with the state diagram description given in 113.4.6.2. When the message field contains a flag for a state transition, the transition counter denotes the remaining number of Infofield until the next state transition. MASTER initiates the transition to PMA_Coeff_Exch count with the trans_to_Coeff_Exch=1 flag and a counter value of 2^9. The SLAVE responds prior to the counter reaching 2^6 with the same flag and a count value matching the MASTER. Then both PHYs transition to PMA_Coeff_Exch within one PMA frame. The same sequence is performed in the transition to PMA_Fine_Adjust state and PCS_Test state using the trans_to_Fine_Adjust=1 and trans_to_PCS_Test=1 flags, respectively. In EEE-capable PHYs, synchronization of the PMA frames is tightly controlled as described in 113.3.5.1. When the message field does not contain a flag for a state transition, the transition counter is set to zero and ignored by the receiver.

Values: 0 to 2^9

tx_mode

PCS Transmit sends code-groups according to the value assumed by this variable.

Values: SEND_N: This value is continuously asserted when transmission of sequences of code-groups representing a 25GMII/XLGMII data stream take place.

SEND_T: This value is continuously asserted when transmission of sequences of code-groups representing the sequences of code-groups (TA_n, TB_n, TC_n, TD_n) defined in 113.3.4.2 is to take place.

SEND_Z: This value is asserted when transmission of zero code-groups is to take place.

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The following variables are required only for PHYs that support the EEE capability:

lpi_refresh_detect
: Set TRUE when the receiver has reliably detected refresh signaling and FALSE otherwise. The exact criteria left to the implementer.

pcs_data_mode
: Generated by the PMA PHY Control function and indicates whether or not the local PHY may transition its PCS state diagrams out of their initialization states. The current value of the pcs_data_mode is passed to the PCS via the PMA_PCSDATAMODE.indicate primitive. In the absence of the optional EEE and fast retrain capabilities, the PHY operates as if the value of this variable is TRUE.

mtc
: mtc is the transition count for a MASTER PHY during normal training and fast retraining. mtc shall be equal to 2^9 for normal training and 2^5 for fast retrain.

stc
: stc is the transition count for a SLAVE PHY during normal training and fast retraining. stc shall be equal to 2^6 for normal training and 2^4 for fast retrain.

The following six variables are required only for PHYs that support the fast retrain capability:

fr_enable
: This variable is set to TRUE if fast retrain is supported. The variable is set to FALSE otherwise. If MDIO is supported, this variable is based on the value of 1.147.0 with the value of TRUE corresponding to 1.147.0 set to 1. If MDIO is not supported, an equivalent method of controlling fast retrain functionality should be provided.

loc_fr_req
: Set TRUE when the receiver has detected a link failure condition and is requesting a fast retrain; set FALSE otherwise.

loc_fr_detect
: Set TRUE when the receiver has reliably detected the link failure signal. It is highly recommended that loc_fr_detect is qualified with the reception of errored blocks at the LDPC decoder output. Set FALSE when the link failure signal is not detected.

send_link_fail
: When TRUE indicates that the PMA should send the link failure signal. When FALSE the variable has no effect.

fr_active
: Set TRUE when the PHY is performing a fast retrain and set FALSE otherwise.

fast_retrain_flag
: Set TRUE after the PHY generates or detects a link failure signal and set FALSE otherwise.

113.4.5.2 Timers

All timers operate in the manner described in 14.2.3.2.

maxwait_timer
: A timer used to limit the amount of time during which a receiver dwells in the SILENT and TRAINING states. The timer shall expire 2000 ms ± 10 ms after being started. This timer is used jointly in the PHY Control and Link Monitor state diagrams. The maxwait_timer is tested by the Link Monitor to force link_status to be set to FAIL if the timer expires and loc_rcvr_status is NOT_OK. See Figure 113–28 and Figure 113–31.

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minwait_timer
: A timer used to determine the minimum amount of time the PHY Control stays in the SILENT, PMA_Training_Init_S, PCS_Test and PCS_Data states. The timer shall expire 1 ms ± 0.1 ms after being started.

The following timer is required only for PHYs that support the EEE capability:

lpi_refresh_rx_timer
: This timer is used to monitor link quality during the LPI receive mode. If the PHY does not reliably detect reliable refresh signaling before this timer expires then a full retrain is performed.
Values: The condition lpi_refresh_rx_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 50 complete quiet-refresh signal periods, equivalent to 2.048× *S* ms.

The following two timers are required only for PHYs that support the fast retrain capability:

link_fail_sig_timer
: Determines the period of time the PHY sends the link failure signal.
Values: The condition link_fail_sig_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 4 LDPC frame periods.

fr_maxwait_timer
: Determines the period of time the PHY has to transition its PCS Control State to PCS_Test following a fast retrain before the fast retrain is aborted and a full retrain performed.
Values: The condition fr_maxwait_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 30 ms.

113.4.5.3 Functions

Exchange_Final_PBO
: This function transmits and receives the final PBO settings using the Infofield as described in 113.4.2.5.

Exchange_THP_Coefficients
: This function compiles and sends to the link partner and receives from the link partner the desired programmable THP coefficients using the Infofield as described in 113.4.2.5.

113.4.5.4 Counters

The following two counters are required only for PHYs that support the fast retrain capability:

fr_tx_counter
: Counts the number of times the PHY initiates a fast link retrain by transmitting the link failure signal. This counter is reflected in MDIO register 1.147.10:6 specified in 45.2.1.94.2.

fr_rx_counter
: Counts the number of times the PHY begins a fast link retrain in response to the detection of link failure signalling from the link partner. This counter is reflected in MDIO register 1.147.15:11 specified in 45.2.1.94.1.

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113.4.6 State diagrams

113.4.6.1 PHY Control state diagram

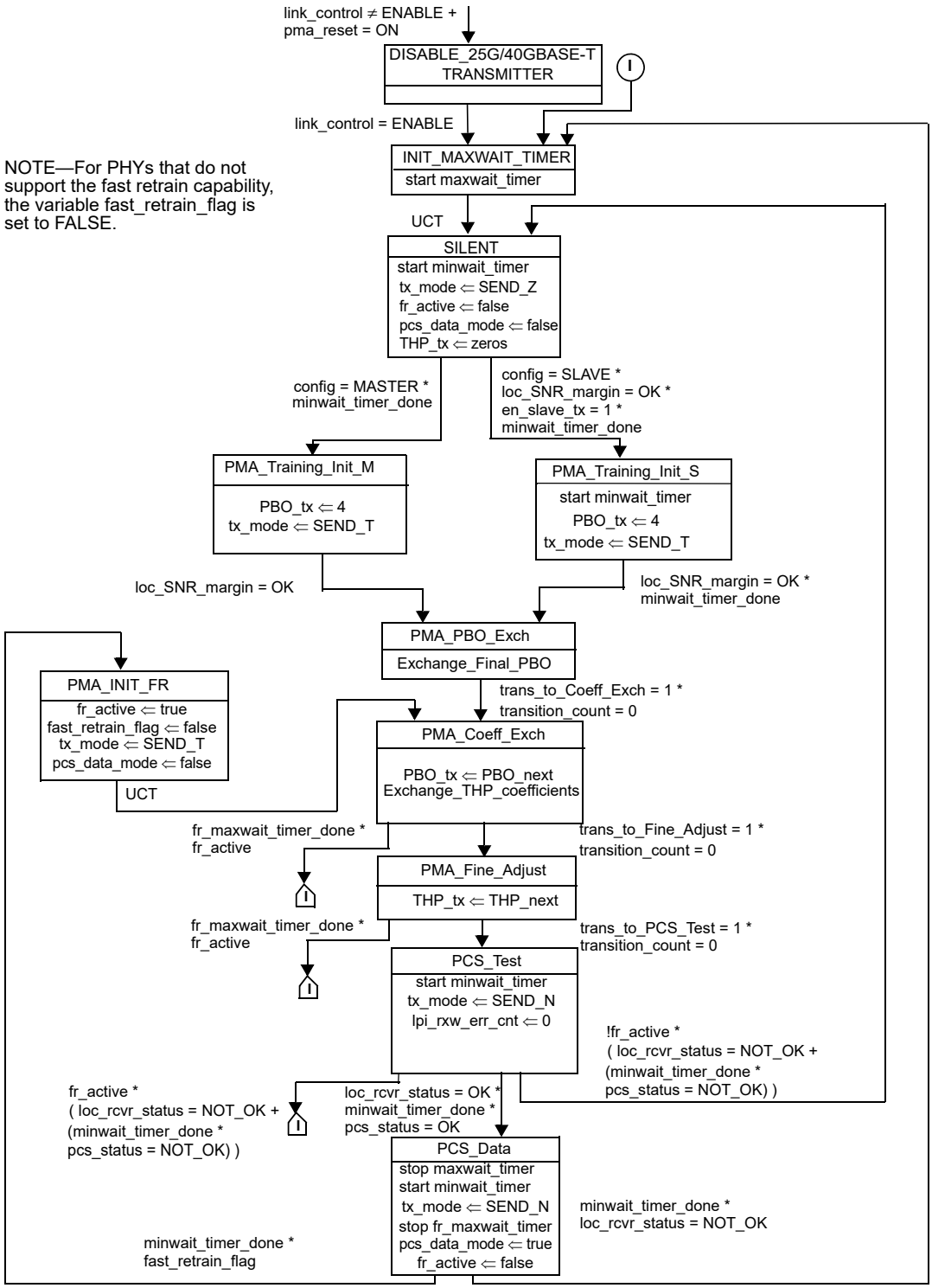

Figure 113–28—PHY Control state diagram

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113.4.6.2 Transition counter state diagrams

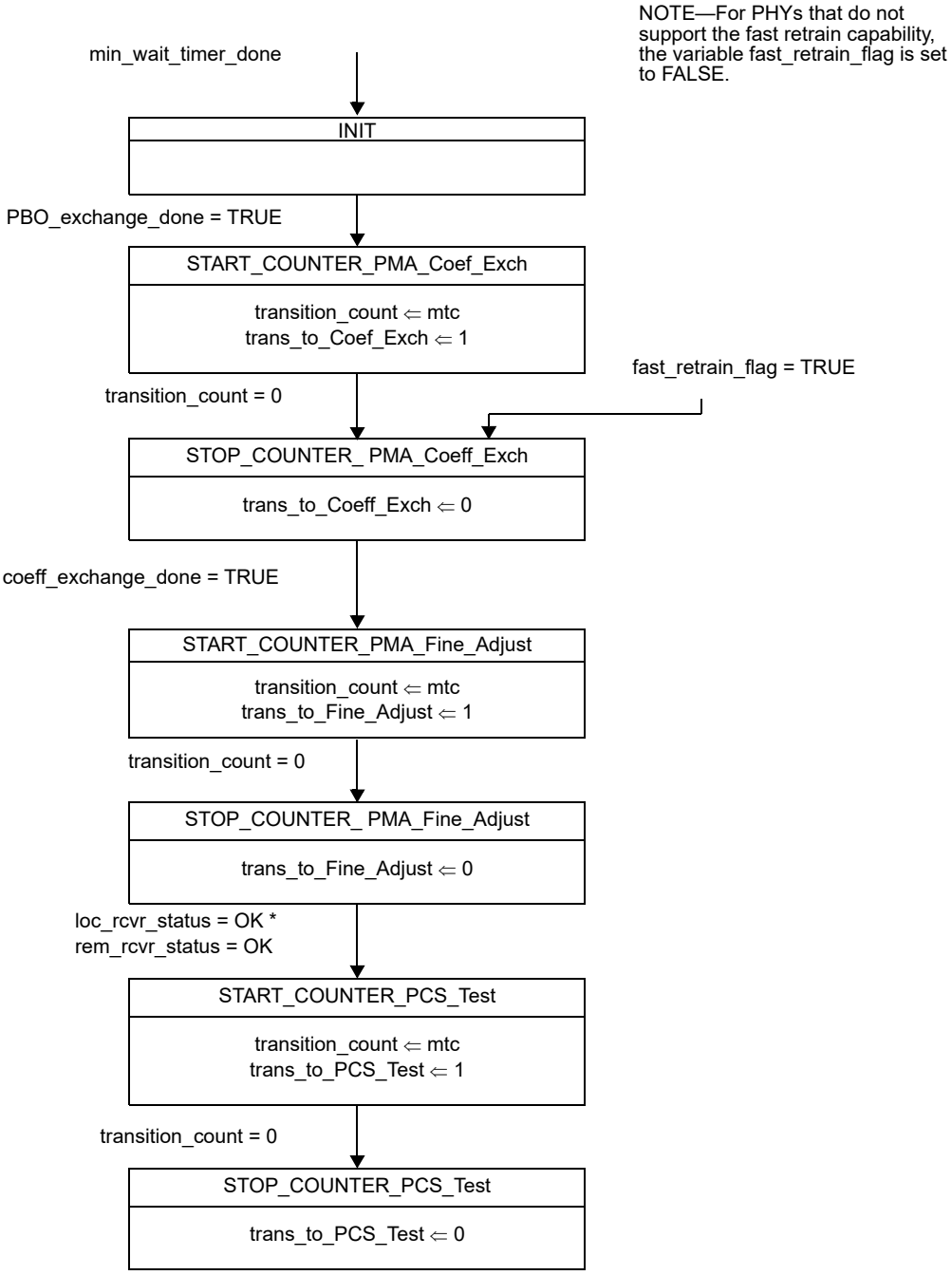

Figure 113–29—MASTER transition counter state diagram

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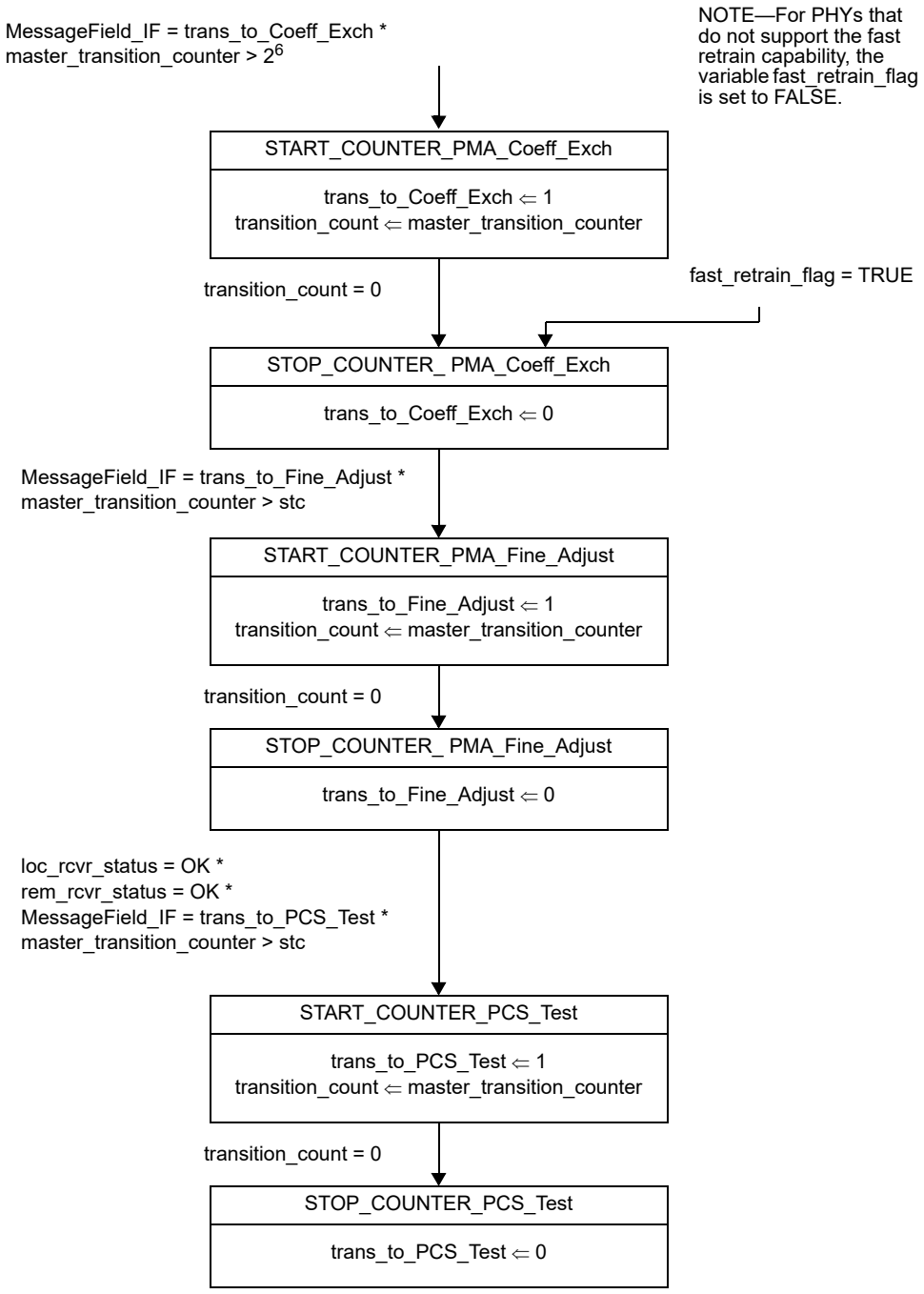

Figure 113–30—SLAVE transition counter state diagram

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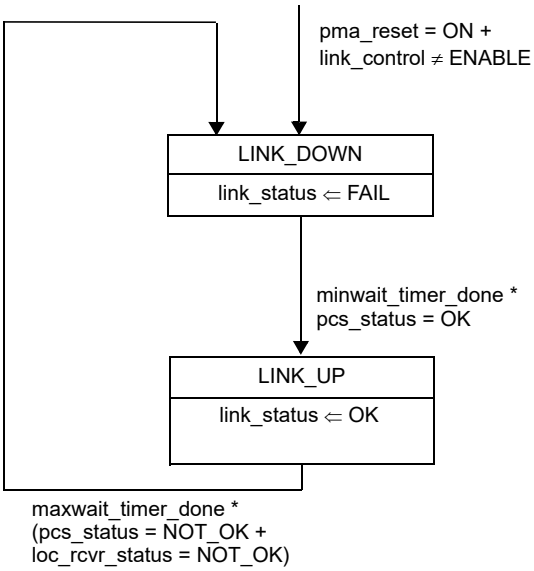
113.4.6.3 Link Monitor state diagram



NOTE 1—maxwait_timer is started in PHY Control state diagram (see Figure 113–28).

NOTE 2—The variables link_control and link_status are designated as link_control_25GigT and link_status_25GigT (for 25GBASE-T) or link_control_40GigT and link_status_40GigT (for 40GBASE-T), respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

Figure 113–31—Link Monitor state diagram

113.4.6.4 EEE Refresh monitor state diagram

113.4.6.5 Fast retrain state diagram

113.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

113.5.1 Electrical isolation

The PHY shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical isolation shall meet the isolation requirements as specified in J.1.

113.5.2 Test modes

The test modes described below shall be provided to allow for testing of the transmitter waveform, transmitter distortion, transmitted jitter, transmitter droop, and BER testing.

For a PHY with an MDIO management interface, these modes shall be enabled by setting bits 1.132.15:13 (MultiGBASE-T test mode register) of the MDIO Management register set as shown in Table 113–16. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the

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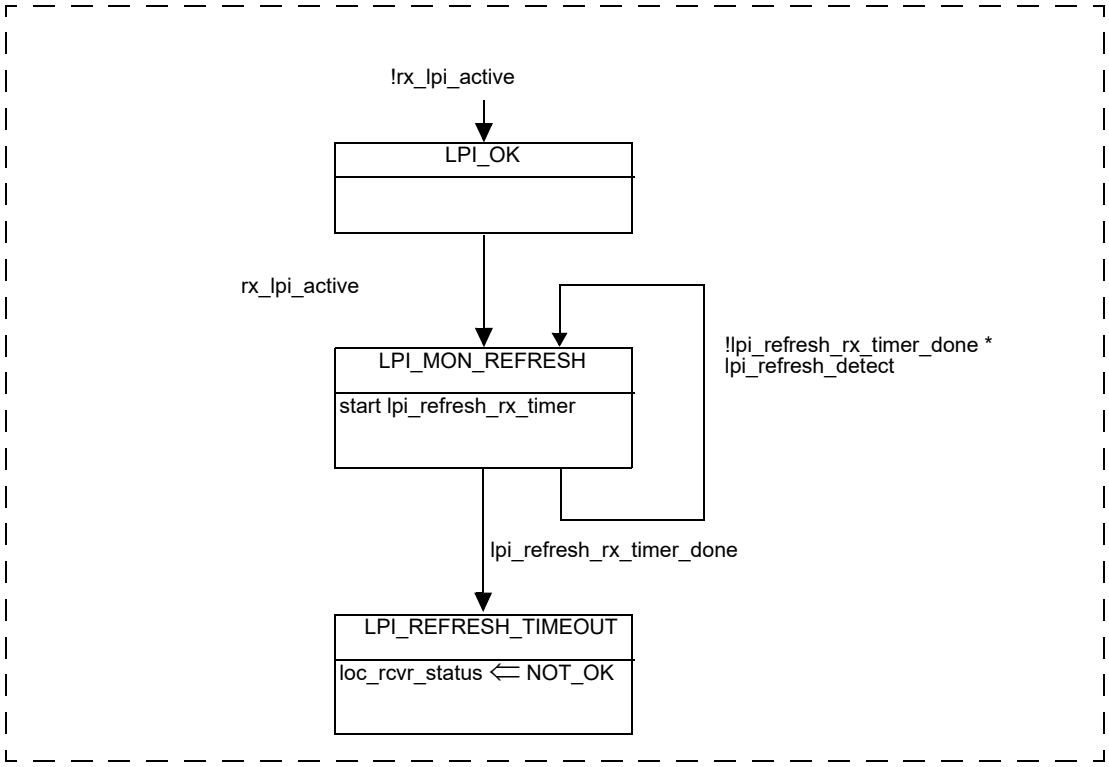

NOTE—This state diagram is only required when the PHY supports the EEE capability.

Figure 113–32—EEE Refresh monitor state diagram

electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation. PHYs without a MDIO shall provide a means to enable these modes for conformance testing.

Table 113–16—MDIO management register settings for test modes

1.132.15	1.132.14	1.132.13	Mode
0	0	0	Normal operation.
0	0	1	Test mode 1—Setting of MASTER transmitter required by SLAVE for transmit jitter test in SLAVE mode.
0	1	0	Test mode 2—Transmit jitter test in MASTER mode.
0	1	1	Test mode 3—Transmit jitter test in SLAVE mode.
1	0	0	Test mode 4—Transmit distortion test.
1	0	1	Test mode 5—Normal operation with no power backoff. This is for the PSD mask and power level test.
1	1	0	Test mode 6—Transmitter droop test mode.
1	1	1	Test mode 7—Pseudo random test mode for BER Monitor.

Test mode 1 is a mode provided for enabling testing of timing jitter on a SLAVE transmitter. When test mode 1 is enabled, the PHY shall transmit the PMA training pattern (PRBS 33) continually from all four

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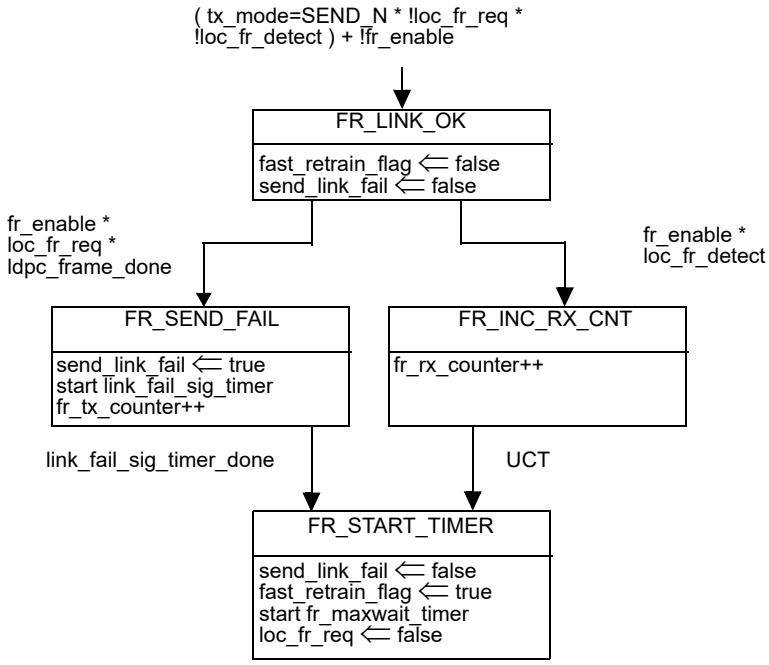

NOTE—This state diagram is only required when the PHY supports the fast retrain capability.

Figure 113–33—Fast retrain control state diagram

transmitters with the THP turned off, with no power backoff and with the transmitted symbols timed from its local clock source.

Test mode 2 is for transmitter jitter testing when transmitter is in MASTER timing mode. When test mode 2 is enabled, the PHY shall transmit {two +16 symbols followed by two –16 symbols} continually from all four transmitters with the THP turned off, with no power backoff and with the transmitted symbols timed from its local clock source. The transmitter output is a $800 \times S$ MHz signal.

When test mode 3 is enabled on a PHY, the PHY shall transmit, with THP turned off, the data symbol sequence {two +16 symbols followed by two –16 symbols} repeatedly on pair D with the symbols timed from its recovered receive data clock in SLAVE timing mode. A PHY operates in test mode 3 when there is no input signal on pair D. The transmitter output is a $800 \times S$ MHz signal on pair D and shall be silence on pairs A, B, and C.

Test mode 4 is for transmitter nonlinear distortion testing. When test mode 4 is enabled, the PHY shall transmit, with the THP turned off, transmitted symbols, timed from a transmit clock (as specified in 113.5.3.5) in the MASTER timing mode, defined by the bits1.132.12:10 and Table 113–17.

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Table 113–17—MDIO management register settings for transmit frequencies in test mode 4

1.132.12	1.132.11	1.132.10	Output waveform frequencies in MHz
			Two tone frequency pairs
0	0	0	Reserved
0	1	1	Reserved
1	1	1	Reserved
0	0	1	(3200 × *S*/1024) × 47, (3200 × *S*/1024) × 53
0	1	0	(3200 × *S*/1024) × 101, (3200 × *S*/1024) × 103
1	0	0	(3200 × *S*/1024) × 179, (3200 × *S*/1024) × 181
1	0	1	(3200 × *S*/1024) × 277, (3200 × *S*/1024) × 281
1	1	0	(3200 × *S*/1024) × 397, (3200 × *S*/1024) × 401

The peak-to-peak levels used in this test shall correspond to the ± 16 symbol levels and the relative amplitudes of the tones in a two-tone pair shall be within 0.5 dB of each other.

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit as in normal operation but with the power backoff disabled.

Test mode 6 is for testing transmitter droop. When test mode 6 is enabled, the PHY shall transmit the following sequence of data symbols A_n, B_n, C_n, D_n, of 113.4.3.1 continually from all four transmitters, with the THP turned off:

{One hundred twenty eight +16 followed by one hundred twenty eight –16 symbols}.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the LDPC encoder/decoder, the transmit and receive analog front ends of the PHY and a cable connecting two PHYs. This mode shall reuse the 25G/40GBASE-T scrambler and is defined in detail in 113.3.3.

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113.5.2.1 Test fixtures

The following fixtures (illustrated by Figure 113–34, Figure 113–35, and Figure 113–36), or their functional equivalents, can be used for measuring the transmitter specifications described in 113.5.3.

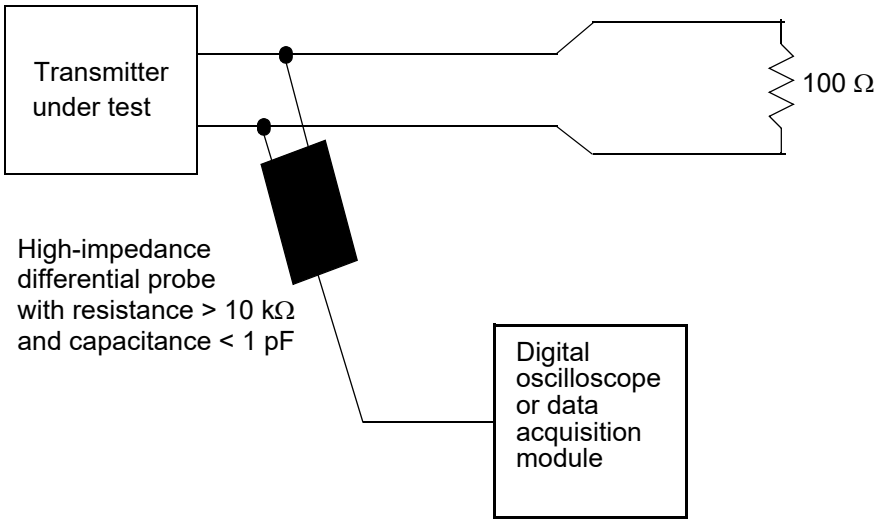

Figure 113–34—Transmitter test fixture 1 for transmitter droop measurement

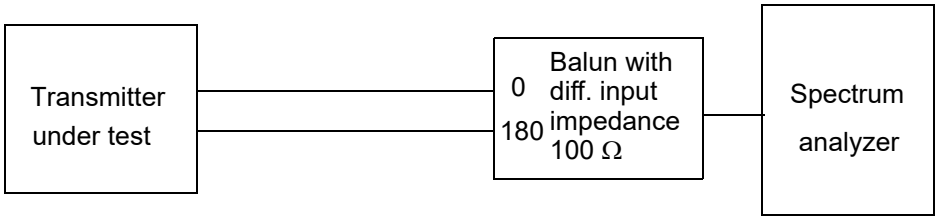

Figure 113–35—Transmitter test fixture 2 for linearity measurement, power spectral density measurement, and transmit power level measurement

The high-impedance probe shown in Figure 113–34 in transmitter test fixture 1 has resistance > 10 KΩ and capacitance < 1 pF over the frequency range of 1 MHz to 1600 MHz. Figure 113–35 includes a power summer or balun device to couple the 100 Ω differential output of the transmitter to the 50 Ω single-ended input typically found in a spectrum analyzer input. The center frequency (F_c) of the band pass filter show in Figure 113–36 is $800 \times S$ MHz ± 200 kHz and the band pass filter noise bandwidth (B_n) is 2 MHz ± 200 kHz.

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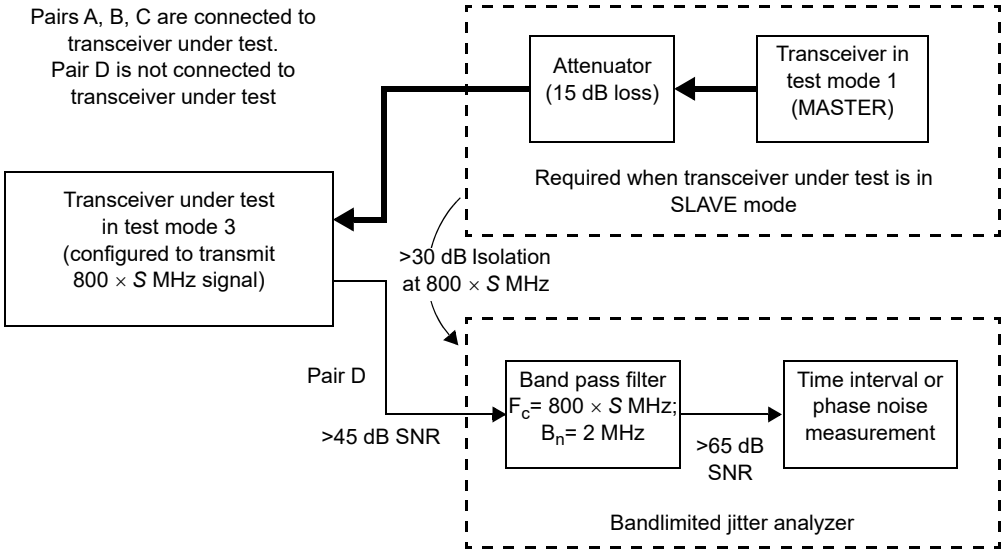

Figure 113–36—Transmitter test fixture 3 for transmitter jitter measurement

113.5.3 Transmitter electrical specifications

The PMA provides the Transmit function specified in 113.4.2.2 in accordance with the electrical specifications of this clause. The PMA shall operate with AC-coupling to the MDI.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.

113.5.3.1 Maximum output droop

With the transmitter in test mode 6 and using the transmitter test fixture 1, the magnitude of both the positive and negative droop shall be less than 10%, measured with respect to an initial value at 2.5/*S* ns after the zero crossing and a final value at 22.5/*S* ns after the zero crossing.

113.5.3.2 Transmitter nonlinear distortion

When in test mode 4 and observing the spectrum of the differential signal output at the MDI using transmitter test fixture 2, for each pair, with no intervening cable, the transmitter nonlinear distortion mask is defined as follows:

The SFDR of the transmitter, with dual tone inputs as specified in test mode 4, shall meet the requirement shown in Equation (113–9) that:

$$\text{SFDR} \geq \quad 2.5 + \ \min\{52,\ 58 - 20 \times \log_{10}(f/(100 \times S))\} \tag{113–9}$$

where f is the maximum frequency of the two test tones in MHz, and SFDR is the ratio in dB of the minimum RMS value of either input tone to the RMS value of the worst intermodulation product in the frequency range of 1 MHz to 1600 × S MHz.

This specification on transmit linearity is derived from the requirement for interoperability with the far-end device.

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113.5.3.3 Transmitter timing jitter

When in test mode 2, the PHY transmits {two +16 symbols followed by two –16 symbols} continually with the THP turned off and with no power backoff. In this mode, the transmitter output should be a $800 \times S$ MHz signal and the RMS period jitter measured at the PHY MDI output shall be less than $1.3/S$ ps. The RMS period jitter is measured as per the test configuration shown in Figure 113–36 over an integration time interval of 1 ms ± 10%.

The SLAVE mode RMS period jitter test is measured using the test configuration shown in Figure 113–36. For this test, the MASTER PHY is in test mode 1 and the SLAVE PHY is in test mode 3. The MASTER is transmitting the PMA training pattern (PRBS 33) to the SLAVE PHY on pairs A, B, and C. The SLAVE PHY is in loop timing mode, synchronizing its transmit clock to the signals received from the MASTER PHY on pairs A, B, and C. In this configuration, the transmitter output on pair D should be a $800 \times S$ MHz signal and the RMS period jitter measured at the SLAVE PHY MDI output shall be less than $1.3/S$ ps. The RMS period jitter is measured over an integration time interval of 1 ms ± 10%.

RMS period jitter over an integration time interval of 1 ms ± 10% is defined as the root mean square period difference from the average period ($T - T_{avg}$), accumulated over a sample size of 200 000 ± 20 000, as shown in Equation (113–10):

$$\text{RMS period jitter} = \sqrt{\frac{\sum[(T - T_{avg})^2]}{\text{Sample size}}} \tag{113–10}$$

113.5.3.4 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation with no power backoff), the transmit power shall be in the range –1.0 dBm to 1.0 dBm and the power spectral density of the transmitter, measured into a 100 Ω, load using the test fixture shown in Figure 113–35 shall be between the upper and lower masks specified in Equation (113–11) and Equation (113–12). The masks are shown graphically in Figure 113–37.

$$\text{Upper PSD}(f) \leq \begin{cases} -88.5 - 10\log_{10} S \text{ dBm/Hz} & 0 < \frac{f}{S} \leq 280 \\ -88.5 - 10\log_{10} S - \left(\frac{\frac{f}{S} - 280}{320}\right) \text{dBm/Hz} & 280 < \frac{f}{S} \leq 600 \\ -89.5 - 10\log_{10} S - \left(\frac{\frac{f}{S} - 600}{232}\right) \text{dBm/Hz} & 600 < \frac{f}{S} \leq 2920 \\ -89.5 - 10\log_{10} S - \left(\frac{\frac{f}{S} - 1320}{160}\right) \text{dBm/Hz} & 2920 < \frac{f}{S} \leq 7160 \\ -126 \text{ dBm/Hz} & 7160 < \frac{f}{S} \leq \frac{12000}{S} \end{cases} \tag{113–11}$$

and

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$$\text{Lower PSD}\ (f) \geq \begin{cases} -93\ \text{dBm/Hz} & 20 \leq f \leq 200 \\ -93 - \left(\dfrac{\dfrac{f}{S} - 200}{200}\right)\text{dBm/Hz} & 200 < \dfrac{f}{S} \leq 800 \\ -96 - \left(\dfrac{\dfrac{f}{S} - 800}{100}\right)\text{dBm/Hz} & 800 < \dfrac{f}{S} \leq \dfrac{1600}{S} \end{cases} \quad (113\text{–}12)$$

where f is in MHz.

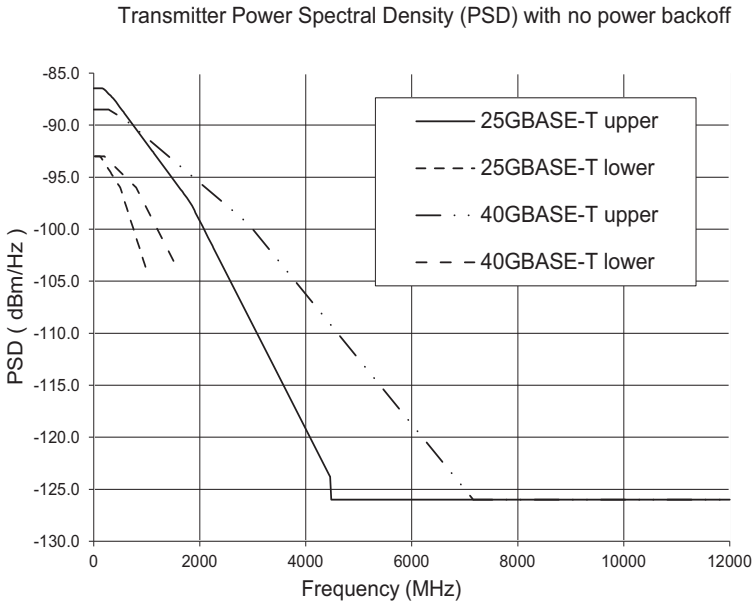

Figure 113–37—Transmitter power spectral density masks

113.5.3.5 Transmit clock frequency

The symbol transmission rate on each pair of the MASTER PHY shall be within the range 3 200× S MBd ± 50 ppm.

For a MASTER PHY, when the transmitter is in the LPI transmit mode or when the receiver is in the LPI receive mode the transmitter clock short-term rate of frequency variation shall be less than 0.1 ppm/second. The short-term frequency variation limit shall also apply when switching to and from the LPI mode.

113.5.4 Receiver electrical specifications

The PMA provides the Receive function specified in 113.4.2.4 in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 113.7.

113.5.4.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 113.5.3 and have passed through a link specified in 113.7 shall be received with a BER less

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than 10^{-12} after LDPC and RS-FEC decoding, and sent to the 25GMII/XLGMII after link reset completion. This specification can be verified by a frame error ratio less than 9.6×10^{-9} for 800 octet frames with minimum IPG or greater than 799 octet IPG.

113.5.4.2 Receiver frequency tolerance

The receive feature shall properly receive incoming data, per the requirements of 113.5.4.1, with a symbol rate within the range 3200× *S* MBd ± 50 ppm.

113.5.4.3 Rejection of External EM Fields

When the cabling system is subjected to electromagnetic fields, currents are generated in the shield that can be converted to interference. This specification is provided to limit the sensitivity of the PMA receiver to external EM fields picked up by the cabling and interconnect system. It provides an assessment method of the electromagnetic performance of the link segment and the PHY, including the MDI.

An 80 MHz to 2000 MHz test can be made based on the cable clamp test described in Annex 113A, a 30 m plug-terminated cabling span that meets the requirements of 113.7, and suitable broadband ferrites. All components that are exposed to the induced fields should remain over the ground reference plane. A sine wave with the amplitude held constant over the whole frequency range from 80 MHz to 2000 MHz, with the amplitude calibrated so that the signal power measured at the output of the clamp does not exceed 6 dBm, is used to generate the external electromagnetic field and corresponding shield current.

A system integrating a 25G/40GBASE-T PHY may perform this test to evaluate anticipated performance in regulatory test environments. Operational requirements of the transceiver during the test are determined by the manufacturer.

NOTE—The 6 dBm limit includes the 10% frequency-dependent variation mentioned in Annex 113A.3.

113.5.4.4 Alien crosstalk noise rejection

While receiving data from a transmitter compliant with specifications in 113.5.3, through a 30 m link segment compliant with the specifications in 113.7, a receiver shall operate with an Ethernet frame error ratio less than 9.6×10^{-9} for 800 octet frames with either a minimum IPG or greater than 799 octet IPG with four noise sources at the specified levels representing alien crosstalk, one connected to each of the four pairs. Independent noise sources should be injected into each MDI input using couplers that do not significantly alter the link segment characteristics. Each noise source shall have a flat noise spectrum, with 3 dB bandwidth at least 10 MHz to 2000 MHz and a power spectral density such that at the MDI port of the device under test the power spectral density of the injected noise is –154 dBm/Hz. A flat noise source is chosen to model the sum of all alien noise sources. See Figure 113–38.

The structure shown for injecting the noise in Figure 113–38 is illustrative and alternative approaches are possible. The loss of the coupling structure shown in Figure 113–38, which consists of two baluns and a coupler, is approximately 2.5 dB. The overall insertion loss of the link segment together with the insertion loss of the coupling structure should be adjusted to match the insertion loss specified in 113.7.2.1 to within ± 0.5 dB. The balun-coupler-balun structure shown in Figure 113–38 can be replaced by resistively coupling a balanced noise source to the twisted-pair using 500 Ω resistors. In either case, calibration of the test setup is required to confirm the overall insertion loss and the injected noise power at the MDI of the receiver under test.

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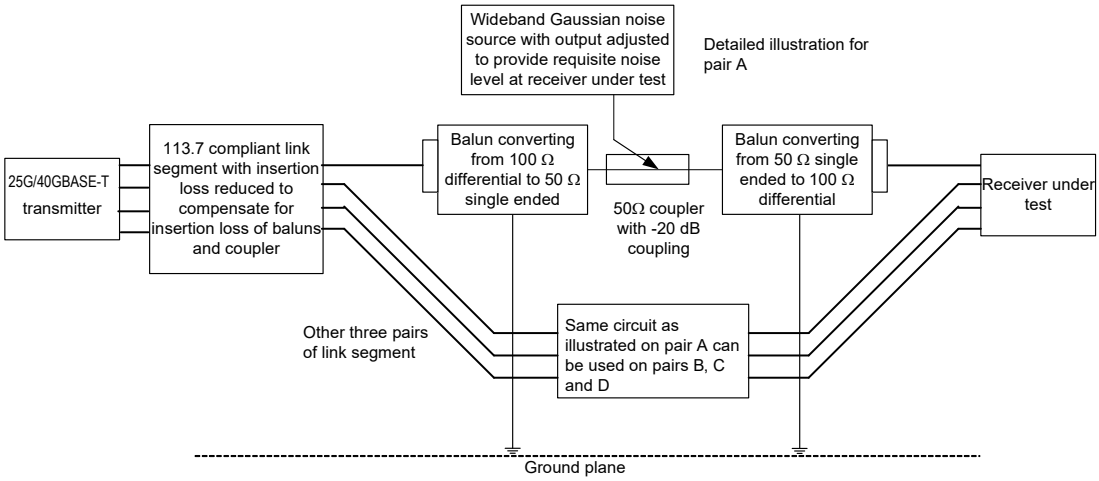

Figure 113–38—Alien crosstalk noise rejection test

113.5.4.5 Short reach mode

The PHY short reach register setting 1.131.0 indicates whether the PHY is operating in the short reach mode.

In short reach mode (indicating operation over a short reach link segment) while receiving data from a transmitter compliant with specifications in 113.5.3 (whether or not in short reach mode), through a short reach link segment meeting the requirements of 113.7.4, a receiver shall operate with a frame error ratio less than 9.6×10^{-9} for 800 octet frames with minimum IPG or greater than 799 octet IPG (e.g., operate with a BER less than 10^{-12}). When operating in short reach mode, only operation over the direct attach link segment specified in 113.7.4 is required.

113.6 Management interfaces

25G/40GBASE-T makes extensive use of the management functions that may be provided by the MDIO (Clause 45), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28). Additional Auto-Negotiation requirements are set forth within this subclause.

113.6.1 Support for Auto-Negotiation

All 25GBASE-T and 40GBASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE. All 25GBASE-T and 40GBASE-T PHYs shall provide support for Extended Next Pages as defined in 28.2.3.4.2 and shall support and use optimized FLP Burst to FLP burst timing as defined in 28.2.1.1.1, and nlp_link_test_min_timer and link_fail_inhibit_timer as defined in 28.3.2.

Auto-Negotiation is performed as part of the initial setup of the link and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-Negotiation signaling is used for the following primary purposes for 25G/40GBASE-T:

a) To negotiate that the PHY is capable of supporting 25GBASE-T or 40GBASE-T transmission.
b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.

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113.6.1.1 25G/40GBASE-T use of registers during Auto-Negotiation

When Clause 45 registers are implemented, a 25G/40GBASE-T PHY shall use the management register definitions and values specified in Table 113–18.

Table 113–18—25G/40GBASE-T registers

Register	Bit	Name	Description	Type[a]
7.0	7.0.15:0	AN control register	Defined in 45.2.7.1	R/W
7.1	7.1.15:0	AN status register	Defined in 45.2.7.2	RO
7.2, 7.3	7.2.15:0, 7.3.15:0	AN device identifier registers	Defined in 45.2.7.3	R/W
7.5, 7.6	7.5.15:0, 7.6.15:0	AN devices in package registers	Defined in 45.2.7.4	R/W
7.14, 7.15	7.14.15:0, 7.15.15:0	AN package identifier registers	Defined in 45.2.7.5	R/W
7.16	7.16.15:0	AN advertisement register	Defined in 45.2.7.6	R/W
7.19	7.19.15:0	AN LP Base Page ability register	Defined in 45.2.7.7	RO
7.22, 7.23, 7.24	7.22.15:0, 7.23.15:0, 7.24.15:0	AN XNP transmit register	Defined in 45.2.7.8	R/W
7.25, 7.26, 7.27	7.25.15:0, 7.26.15:0, 7.27.15:0	AN LP XNP ability register	Defined in 45.2.7.9	RO
7.32	7.32.15:0	MultiGBASE-T AN control 1 register	Defined in 45.2.7.10	R/W
7.33	7.33.15:0	MultiGBASE-T AN status 1 register	Defined in 45.2.7.11	RO
7.64	7.64.15:0	MultiGBASE-T AN control 2 register	Defined in 45.2.7.18	R/W
7.65	7.65.15:0	MultiGBASE-T AN status 2 register	Defined in 45.2.7.19	RO

[a]R/W = Read/Write, RO = Read only

113.6.1.2 25G/40GBASE-T Auto-Negotiation page use

25G/40GBASE-T PHYs shall exchange a MultiGBASE-T and 1000BASE-T formatted Extended Next Page, as specified in Table 113–19, immediately following the exchange of the Base Page.

Note that the Acknowledge 2 bit is not utilized and has no meaning when used for the 25G/40GBASE-T message page exchange.

113.6.1.3 Sending Next Pages

Implementers who do not wish to send additional Extended Next Pages (i.e., Extended Next Pages in addition to those required to perform PHY configuration as defined in this clause) can use Auto-Negotiation as defined in Clause 28. Implementers who wish to send additional Extended Next Pages may do so using the AN XNP transmit registers. See 45.2.7.8.

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Table 113–19—25G/40GBASE-T Base and Next Pages bit assignments

Bit	Name	Description
Base Page		
D15	Next Page	Defined in 28.2.1.2.6
D14	Acknowledge	Defined in 28.2.1.2.5
D13	Remote Fault	Defined in 28.2.1.2.4
D12	Extended Next Page	Defined in 28.2.1.2.3
D11:D5	Technology Ability Field	Defined in 28.2.1.2.2
D4:D0	Selector Field	Defined in 28.2.1.2.1
Extended Next Page (Message Code Field and Flags Field)		
M10:M0	Next Page message code	Defined in Annex 28C
T	Toggle	Defined in 28.2.3.4.7
Ack2	Acknowledge 2	Defined in 28.2.3.4.6
MP	Message Page	Defined in 28.2.3.4.5
Ack	Acknowledge	Defined in 28.2.3.4.4
NP	Next Page	Defined in 28.2.3.4.3
Extended Next Page (Unformatted Message Code Field)		
U31:U27	Reserved, transmit as 0	
U26	40GBASE-T ability (1 = support of 40GBASE-T and 0 = no support)	Defined in 45.2.7.10.5
U25	25GBASE-T ability (1 = support of 25GBASE-T and 0 = no support)	Defined in 45.2.7.10.6
U24	10GBASE-T EEE (1 = Advertise EEE capability for 10GBASE-T 0 = Do not advertise EEE capability for 10GBASE-T)	Defined in 45.2.7.14.12
U23	1000BASE-T EEE (1 = Advertise EEE capability for 1000BASE-T 0 = Do not advertise EEE capability for 1000BASE-T)	Defined in 45.2.7.14.13
U22	100BASE-TX EEE (1 = Advertise EEE capability for100BASE-TX 0 = Do not advertise EEE capability for 100BASE-TX)	Defined in 45.2.7.14.14
U21	Reserved	Value always 0
U20	10GBASE-T LD PMA training reset request 0 = Local Device requests that Link Partner run PMA training PRBS continuously) This bit is not defined for 10GBASE-T but reserved for future use.	Defined in 45.2.7.10.13
U19	10GBASE-T Fast retrain ability (1 = Advertise PHY as supporting fast retrain, 0 = Advertise PHY as not supporting fast retrain)	Defined in 45.2.7.10.14. This bit is not defined for 10GBASE-T but reserved for future use.
U18	PHY short reach mode (1 = PHY of Local Device is operating in short reach mode 0 = PHY of Local Device is operating in normal mode)	Defined in 45.2.1.79.2
U17	10GBASE-T LD loop timing ability (1 = Advertise PHY as capable of loop timing (mandatory for 25G/40GBASE-T) and 0 = do not advertise PHY as capable of loop timing)	Defined in45.2.7.10.15

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Table 113–19—25G/40GBASE-T Base and Next Pages bit assignments *(continued)*

Bit	Name	Description
U16	10GBASE-T ability (1 = support of 10GBASE-T and 0 = no support)	Defined in 45.2.7.10.4
U15	1000BASE-T half duplex (1 = half duplex and 0 = no half duplex)	
U14	1000BASE-T full duplex (1 = full duplex and 0 = no full duplex)	
U13	Port type bit (1 = multiport device and 0 = single-port device)	Defined in 45.2.7.10.3
U12	MultiGBASE-T MASTER-SLAVE config value (1 = MASTER and 0 = SLAVE) This bit is ignored if 7.32.15=0.	Defined in 45.2.7.10.2
U11	MultiGBASE-T MASTER-SLAVE manual config enable (1 = manual configuration enable) This bit is intended to be used for manual selection in a particular MASTER-SLAVE mode and is to be used in conjunction with bit 7.32.14.	Defined in 45.2.7.10.1
U10	MASTER-SLAVE seed Bit 10 (SB10) (MSB)	
U9	MASTER-SLAVE seed Bit 9 (SB9)	
U8	MASTER-SLAVE seed Bit 8 (SB8)	
U7	MASTER-SLAVE seed Bit 7 (SB7)	
U6	MASTER-SLAVE seed Bit 6 (SB6)	
U5	MASTER-SLAVE seed Bit 5 (SB5)	
U4	MASTER-SLAVE seed Bit 4 (SB4)	
U3	MASTER-SLAVE seed Bit 3 (SB3)	
U2	MASTER-SLAVE seed Bit 2 (SB2)	
U1	MASTER-SLAVE seed Bit 1 (SB1)	
U0	MASTER-SLAVE seed Bit 0 (SB0)	

113.6.2 MASTER-SLAVE configuration resolution

Since both PHYs that share a link segment are capable of being MASTER or SLAVE, a prioritization scheme exists to ensure that the correct mode is chosen. The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using Table 113–20 with the 25G/40GBASE-T Technology Ability Next Page bit values specified in Table 113–19 and information received from the link partner. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown in the Arbitration state diagram (Figure 28–18.)

The following four equations are used to determine these relationships:

manual_MASTER = U11 * U12

manual_SLAVE = U11 * !U12

single-port device = !U11 * !U13

multiport device = !U11 * U13

where

U11 is bit 11 of MultiGBASE-T and 1000BASE-T Technology message code,

U12 is bit 12 of MultiGBASE-T 1000BASE-T Technology message code,

U13 is bit 13 of MultiGBASE-T and 1000BASE-T Technology message code (see Table 113–19).

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25GBASE-T and 40GBASE-T PHYs are capable of operating either as the MASTER or SLAVE. In the scenario of a link between a single-port device and a multiport device, the preferred relationship is for the multiport device to be the MASTER PHY and the single-port device to be the SLAVE. However, other topologies can result in contention. The resolution function of Table 113–20 is defined to handle any relationship conflicts.

The resolution shown in Table 113–20 shall be used.

Table 113–20—25G/40GBASE-T MASTER-SLAVE configuration resolution table

Local device type	Remote device type	Local device resolution	Remote device resolution
single-port device	multiport device	SLAVE	MASTER
single-port device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	manual_MASTER	SLAVE	MASTER
manual_SLAVE	multiport device	SLAVE	MASTER
multiport device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	single-port device	SLAVE	MASTER
multiport device	single-port device	MASTER	SLAVE
multiport device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	manual_SLAVE	MASTER	SLAVE
manual_MASTER	single-port device	MASTER	SLAVE
single-port device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	multiport device	MASTER	SLAVE
multiport device	multiport device	The device with the higher seed value is configured as MASTER, otherwise SLAVE.	The device with the higher seed value is configured as MASTER, otherwise SLAVE.
single-port device	single-port device	The device with the higher seed value is configured as MASTER, otherwise SLAVE	The device with the higher seed value is configured as MASTER, otherwise SLAVE.
manual_SLAVE	manual_SLAVE	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault
manual_MASTER	manual_MASTER	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault

A 25G/40GBASE-T multiport device has higher priority than a single-port device to become the MASTER. In the case where both devices are of the same type, e.g., both devices are multiport devices, the device with the higher MASTER-SLAVE seed bits (SB0...SB10), where SB10 is the MSB, shall become the MASTER and the device with the lower seed value shall become the SLAVE. In case both devices have the same seed value, both should assert either link_status_25GigT=FAIL (for 25GBASE-T) or link_status_40GigT=FAIL (for 40GBASE-T) (as defined in 28.3.1) to force a new cycle through Auto-Negotiation. Successful completion of the MASTER-SLAVE resolution shall be treated as MASTER-SLAVE configuration resolution complete.

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The method of generating a random or pseudorandom seed is left to the implementer. The generated random seeds should belong to a sequence of independent, identically distributed integer numbers with a uniform distribution in the range of 0 to 2^{11}– 2. The algorithm used to generate the integer should be designed to minimize the correlation between the number generated by any two devices at any given time. A seed counter shall be provided to track the number of seed attempts. The seed counter shall be set to zero at startup and shall be incremented each time a seed is generated. When MASTER-SLAVE resolution is complete, the seed counter shall be reset to 0 and bit 7.33.15 shall be set to zero. A MASTER-SLAVE resolution fault shall be declared if resolution is not reached after the generation of seven seeds.

The MASTER-SLAVE manual configuration enable bit (control register bit 7.32.15) and the MASTER-SLAVE config value bit (control register bit 7.32.14) are used to manually set a device to become the MASTER or the SLAVE. In case both devices are manually set to become the MASTER or the SLAVE, this condition shall be flagged as a MASTER-SLAVE configuration fault condition; thus the MASTER-SLAVE configuration fault bit (status register bit 7.33.15) shall be set to logical one. The MASTER-SLAVE configuration fault condition shall be treated as MASTER-SLAVE configuration resolution complete and link_status_25GigT or link_status_40GigT shall be set to FAIL, for 25GBASE-T or 40GBASE-T, respectively, because the MASTER-SLAVE relationship was not resolved. This forces a new cycle through Auto-Negotiation after the link_fail_inhibit_timer has expired. Determination of MASTER-SLAVE values occur on the entrance to the FLP LINK GOOD CHECK state (Figure 28–18) when the highest common denominator (HCD) technology is 25GBASE-T or 40GBASE-T. The resulting MASTER-SLAVE value is used by the 25G/40GBASE-T PHY Control (113.4.2.5).

If MASTER-SLAVE manual configuration is disabled (bit 7.32.15 is set to 0) and the local device detects that both the local device and the remote device are of the same type (either multiport device or single-port device) and that both have generated the same random seed, it generates and transmits a new random seed for MASTER-SLAVE negotiation by setting link_status to FAIL and cycling through the Auto-Negotiation process again.

The MASTER-SLAVE configuration process returns one of the three following outcomes:

a) *Successful:* Bit 7.33.15 of the 25G/40GBASE-T status register is set to logical zero and bit 7.33.14 is set to logical one for MASTER resolution or for logical zero for SLAVE resolution. 25G/40GBASE-T returns control to Auto-Negotiation (at the entrance to the FLP LINK GOOD CHECK state in Figure 28–18) and passes the value MASTER or SLAVE to PMA_CONFIG.indication (see 113.2.2.2).
b) *Unsuccessful:* link_status_25GigT or link_status_40GigT is set to FAIL and Auto-Negotiation restarts (see Figure 28–18).
c) *Fault detected:* Bit 7.33.15 of the 25G/40GBASE-T status register is set to logical one to indicate that a configuration fault has been detected. This bit also is set when seven attempts to configure the MASTER-SLAVE relationship via the seed method have failed. When a fault is detected, link_status_25GigT or link_status_40GigT is set to FAIL, causing Auto-Negotiation to cycle through again.

NOTE—MASTER-SLAVE arbitration only occurs if 40GBASE-T, 25GBASE-T, 10GBASE-T, or 1000BASE-T is selected as the highest common denominator.

113.7 Link segment characteristics

25G/40GBASE-T is designed to operate over 4-pair balanced cabling listed in Table 113–21 that meets the additional requirements specified in this subclause. Each of the four pairs supports an effective data rate of 10 Gb/s for 40GBASE-T and 6.25 Gb/s for 25GBASE-T in each direction simultaneously. The term *duplex channel* used in this clause refers to a single cable pair with full duplex capability. The term *link segment* used in this clause refers to four duplex channels. All implementations of the balanced cabling link segment

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specification shall be compatible at the MDI. It is recommended that the guidelines in ISO/IEC 11801-1:2016 and ANSI/TIA-568-C.2-1 Category 8 Cabling be considered before the installation of 25G/40GBASE-T equipment for any cabling system.

The short reach link segment meeting the transmission requirements in 113.7.4 are specified to support up to 5 m.

113.7.1 Cabling system characteristics

The cabling system used to support 25G/40GBASE-T requires 4-pair balanced cabling with a nominal impedance of 100 Ω listed in Table 113–21. Operation on other classes of cabling may be supported if the link segment meets the requirements of 113.7.

Additionally:

a) 25G/40GBASE-T uses balanced cabling listed in Table 113–21 to connect PHY entities.
b) 25G/40GBASE-T is an application of the balanced cabling listed in Table 113–21 with the additional transmission requirements specified in this subclause.

NOTE—ISO/IEC TR 11801-9905 [B43] provides guidance on the use of channels constructed from components of other categories with this standard at the 25 Gb/s rate. It provides specifications for cabling, certification, and mitigation procedures suitable for use with this standard.

113.7.2 Link segment transmission parameters

A link segment consisting of up to 30 m of cabling that meets the transmission parameters of this subclause provides a reliable medium. The transmission parameters of the link segment include insertion loss, delay parameters, nominal impedance, NEXT loss, ACRF, and return loss. In addition, the requirements for the alien crosstalk coupled "between" link segments is specified. The parameter S is used in 113.7.2 to scale the data rate for each PHY. For 25GBASE-T, $S = 0.625$ and for 40GBASE-T, $S = 1$.

Table 113–21 lists the supported cabling types and distances.

Table 113–21—Cabling types and distances

Cabling	Supported link segment distances	Cabling references
ISO/IEC Class I / Class II	30 m	ISO/IEC DIS 11801-1:2016
Category 8	30 m	ANSI/TIA-568-C.2-1-2016

113.7.2.1 Insertion loss

The insertion loss of each duplex channel shall meet the values determined using Equation (113–13).

$$\text{Insertion loss}(f) \le \frac{0.0856}{\sqrt{f}} + 0.6371 \times \sqrt{f} + 0.0023 \times f + 1.0285 \times 10^{-7} \times f^2 (\text{dB}) \quad (113\text{–}13)$$

where

f is the frequency in MHz; $1 \le f \le 2000 \times S$

Calculations that result in insertion loss values less than 2 dB revert to a requirement of 2 dB.

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This includes the insertion loss of the balanced cabling pairs, including work area and equipment cables plus connector losses within each duplex channel. Note that Equation (113–13) is an approximation of the ISO/IEC Class I channel insertion loss.

113.7.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each link segment duplex channel, which includes cable cords and connecting hardware, is 100 Ω for all frequencies between 1 MHz and 2000 × *S* MHz.

113.7.2.3 Return loss

In order to limit the noise at the receiver due to impedance mismatches in the cabling system, each link segment duplex channel shall meet the values determined using Equation (113–14) at all frequencies from 1 MHz to 2000 × *S* MHz. The reference impedance for the return loss specification is 100 Ω.

$$\text{Return Loss} \geq \begin{cases} 19 & 1 \leq f < 10 \\ 24 - 5\log_{10} f & 10 \leq f < 40 \\ 16 & 40 \leq f < 130 \\ 35 - 9\log_{10} f & 130 \leq f < 1000 \\ 8 & 1000 \leq f < 1250 \\ 8 & 1250 \leq f < 1600 \text{ (for 40GBASE-T)} \\ 8 - 19\log_{10}\left(\frac{f}{1600}\right) & 1600 \leq f < 2000 \text{ (for 40GBASE-T)} \end{cases} \text{ dB} \qquad (113\text{–}14)$$

where

f is the frequency in MHz.

113.7.2.4 Coupling parameters between duplex channels comprising one link segment

In order to limit the noise coupled into a duplex channel from adjacent duplex channels, near-end crosstalk (NEXT) loss and attenuation to crosstalk ratio, far-end (ACRF) are specified for each link segment. In addition, each duplex channel can be disturbed by more than one duplex channel. To ensure the total NEXT loss and FEXT loss coupled into a duplex channel is limited, multiple disturber near-end crosstalk (MDNEXT) and multiple disturber ACRF (MDACRF) is specified.

113.7.2.4.1 Differential near-end crosstalk

In order to limit the crosstalk at the near end of a link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between a duplex channel and the other three duplex channels is specified to meet the bit error ratio objective specified in 113.1.2. The NEXT loss between any two duplex channels of a link segment shall meet the values determined using Equation (113–15) to Equation (113–17).

$$\text{NEXT loss}(f) \geq -20\log_{10}\left[10^{\frac{45.3 - 15\log_{10}\left(\frac{f}{100}\right)}{-20}} + 2 \times 10^{\frac{54 - 20\log_{10}\left(\frac{f}{100}\right)}{-20}}\right] \text{ (dB)} \qquad (113\text{–}15)$$

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where

f is the frequency in MHz $1 \le f \le 440$.

$$\text{NEXT loss}(f) \ge -20\log_{10}\left[10^{\frac{45.3 - 15\log_{10}\left(\frac{f}{100}\right)}{-20}} + 2 \times 10^{\frac{39.12 - 36.14\log_{10}\left(\frac{f}{500}\right)}{-20}}\right] \text{(dB)} \quad (113\text{–}16)$$

where

f is the frequency in MHz $440 < f \le 1486$.

$$\text{NEXT loss}(f) \ge -20\log_{10}\left[10^{\frac{45.3 - 15\log_{10}\left(\frac{f}{100}\right)}{-20}} + 2 \times 10^{\frac{40 - 38\log_{10}\left(\frac{f}{500}\right)}{-20}}\right] \text{(dB)} \quad (113\text{–}17)$$

where

f is the frequency in MHz $1486 < f \le 2000 \times S$.

Calculations that result in NEXT loss values greater than 65 dB revert to a requirement of 65 dB minimum.

113.7.2.4.2 Multiple disturber near-end crosstalk (MDNEXT) loss

Since four duplex channels are used to transfer data between PMAs, the NEXT that is coupled into a data carrying duplex channel is from the three adjacent disturbing duplex channels.

To ensure the total NEXT coupled into a duplex channel is limited, multiple disturber NEXT loss is specified as the power sum of the individual NEXT losses. The power sum loss between a duplex channel and the three adjacent disturbers shall meet the values determined using Equation (113–18) to Equation (113–20).

$$\text{MDNEXT loss}(f) \ge -20\log_{10}\left[10^{\frac{42.3 - 15\log_{10}\left(\frac{f}{100}\right)}{-20}} + 2 \times 10^{\frac{50 - 20\log_{10}\left(\frac{f}{100}\right)}{-20}}\right] \text{(dB)} \quad (113\text{–}18)$$

where

f is the frequency in MHz $1 \le f \le 500$.

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$$\text{MDNEXT loss}(f) \geq -20\log_{10}\left[10^{\frac{42.3 - 15\log_{10}\left(\frac{f}{100}\right)}{-20}} + 2\times 10^{\frac{35.95 - 34.85\log_{10}\left(\frac{f}{500}\right)}{-20}}\right] \text{ (dB)} \quad (113\text{–}19)$$

where

f is the frequency in MHz $500 < f \leq 1100$.

$$\text{MDNEXT loss}(f) \geq -20\log_{10}\left[10^{\frac{42.3 - 15\log_{10}\left(\frac{f}{100}\right)}{-20}} + 2 \times 10^{\frac{37 - 38\log_{10}\left(\frac{f}{500}\right)}{-20}}\right] \text{ (dB)} \quad (113\text{–}20)$$

where

f is the frequency in MHz $1100 < f \leq 2000 \times S$.

Calculations that result in MDNEXT loss values greater than 62 dB revert to a requirement of 62 dB minimum.

113.7.2.4.3 Multiple disturber power sum near-end crosstalk (PSNEXT) loss

PSNEXT loss is determined by summing the power of the three individual pair-to-pair differential NEXT loss values over the frequency range 1 MHz to $2000 \times S$ MHz as follows in Equation (113–21).

$$\text{PSNEXT loss}(f) = \left(-10\log_{10}\sum_{i=1}^{n} 10^{\frac{-NL(f)i}{10}}\right) \text{ (dB)} \quad (113\text{–}21)$$

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where

NL(f)i is the magnitude in dB of NEXT loss at frequency *f* (in MHz) of pair combination *i*
i is the pair-to-pair combination (1 to *n*)
n is the number of pair-to-pair combinations (*n*=3)

113.7.2.4.4 Attenuation to crosstalk ratio, far end (ACRF)

Attenuation to crosstalk ratio, far-end (ACRF) is specified in order to limit the crosstalk at the far end of each link segment duplex channel and meet the bit error ratio objective specified in 113.1.2. Far-end crosstalk (FEXT) is crosstalk that appears at the far end of a duplex channel (disturbed channel), which is coupled from another duplex channel (disturbing channel) with the noise source (transmitters) at the near end.

FEXT loss is defined in Equation (113–22) as

$$\text{FEXT loss}(f) = 20\log_{10}\left(\frac{V_{pds}(f)}{V_{pcn}(f)}\right) \quad \text{(dB)} \tag{113–22}$$

and ACRF is defined in Equation (113–23) as

$$\text{ACRF}(f) = 20\log_{10}\left(\frac{V_{pds}(f)}{V_{pcn}(f)}\right) - \text{SLS\_Loss(f)} \text{ (dB)} \tag{113–23}$$

where

Vpds is the peak voltage of disturbing signal (near-end transmitter)
Vpcn is the peak crosstalk noise at far end of disturbed channel
SLS_Loss is the insertion loss of disturbed channel in dB

The worst pair ACRF between any two duplex channels shall meet the values determined using Equation (113–24).

$$\text{ACRF loss}(f) \geq -20\log_{10}\left[10^{\frac{39.0 - 20\log_{10}\left(\frac{f}{100}\right)}{-20}} + 2 \times 10^{\frac{43.1 - 20\log_{10}\left(\frac{f}{100}\right)}{-20}}\right] \text{(dB)} \tag{113–24}$$

where

f is the frequency in MHz $1 \leq f \leq 2000 \times S$.

Calculations that result in ACRF loss values greater than 65 dB revert to a requirement of 65 dB minimum.

113.7.2.4.5 Multiple disturber attenuation to crosstalk ratio, far-end (MDACRF)

Since four duplex channels are used to transfer data between PMAs, the FEXT that is coupled into a data carrying duplex channel is from the three adjacent disturbing duplex channels. To ensure the total FEXT coupled into a duplex channel is limited, multiple disturber ACRF is specified as the power sum of the

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individual ACRF disturbers. The power sum loss between a duplex channel and the three adjacent disturbers shall meet the values determined using Equation (113–25).

$$\mathrm{MDACRF}(f) \geq -20\log_{10}\left[10^{\frac{36-20\log_{10}\left(\frac{f}{100}\right)}{-20}} + 2\times 10^{\frac{40.1-20\log_{10}\left(\frac{f}{100}\right)}{-20}}\right] \quad \text{(dB)} \qquad (113\text{–}25)$$

where

f is the frequency $1 \leq f \leq 2000 \times S$.

Calculations that result in MDACRF loss values greater than 62 dB revert to a requirement of 62 dB minimum.

113.7.2.4.6 Multiple disturber power sum attenuation to crosstalk ratio, far-end (PS-ACRF)

PS-ACRF is determined by summing the power of the three individual pair-to-pair differential ACRF values over the frequency range 1 MHz to 2000 × *S* MHz as follows in Equation (113–26):

$$\mathrm{PSACRF}\ (f) = -10\log_{10}\sum_{i=1}^{i=n} 10^{\frac{-ACRF(f)i}{10}} \quad \text{(dB)} \qquad (113\text{–}26)$$

where

ACRF(f)i is the magnitude of ACRF at frequency *f* of pair combination *i*
i is the pair-to-pair combination (1 to *n*)
f is the frequency in MHz
n is the number of pair-to-pair combinations (*n*=3)

113.7.2.5 Maximum link delay

The propagation delay of a link segment shall not exceed 185 ns at all frequencies between 2 MHz and 2000 × *S* MHz.

113.7.2.6 Link delay skew

The difference in propagation delay, or skew, between all duplex channel pair combinations of a link segment, under all conditions, shall not exceed 17 ns at all frequencies from 2 MHz to 2000 × *S* MHz. It is a further functional requirement that, once installed, the skew between any two of the four duplex channels due to environmental conditions shall not vary more than 3 ns within the above requirement.

113.7.3 Coupling parameters between link segments

Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. To ensure the total alien NEXT loss and alien FEXT loss coupled between link segments is limited, multiple disturber alien near-end crosstalk (MD ANEXT) loss and multiple disturber alien FEXT (MDAFEXT) loss is specified. In addition, to ensure the reliable operation of the link segment, a minimum alien crosstalk to insertion loss ratio are specified.

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113.7.3.1 Multiple disturber alien near-end crosstalk (MDANEXT) loss

In order to limit the alien crosstalk at the near end of a link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is specified to meet the bit error ratio objective specified in 113.1.2. To ensure the total alien NEXT coupled into a duplex channel is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT disturbers.

113.7.3.1.1 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

PSANEXT loss is determined by summing the power of the individual pair-to-pair differential alien NEXT loss values over the frequency range 1 MHz to 2000 × *S* MHz as follows in Equation (113–27):

$$\mathrm{PSANEXT}_N(f) = -10\log_{10}\sum_{j=1}^{m}\sum_{i=1}^{4} 10^{\frac{-AN(f)_{i,j,N}}{10}} \quad (\mathrm{dB}) \qquad (113\text{–}27)$$

where

$AN(f)_{i,j,N}$ is the magnitude in dB of the alien NEXT loss at frequency f of the individual pair combination i (1 to 4) of the disturbing link j (1 to m) for each disturbed pair N

Annex 55B provides additional information on identifying the number of adjacent link segments to consider in the PSANEXT calculation.

The power sum ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall meet the values determined using Equation (113–28) independent of length.

$$\mathrm{PSANEXT}(f) \geq 85 - 15\log_{10}\left(\frac{f}{100}\right) \quad (\mathrm{dB}) \qquad 1 \leq f \leq 2000 \times S \qquad (113\text{–}28)$$

where

f is the frequency in MHz

When Equation (113–28) values are greater than 75 dB, they revert to 75 dB.

113.7.3.2 Multiple disturber alien far-end crosstalk (MDAFEXT) loss

In order to limit the alien crosstalk at the far-end of a link segment, the differential pair-to-pair alien far-end crosstalk loss between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is specified to meet the bit error ratio objective specified in 113.1.2. To ensure the total alien FEXT coupled into a duplex channel is limited, multiple disturber ACRF is specified as the power sum of the individual alien ACRF disturbers.

113.7.3.2.1 Multiple disturber power sum alien attenuation to crosstalk, far end crosstalk (PSAACRF)

Power sum alien ACRF is determined by summing the power of the individual pair-to-pair differential alien ACRF values over the frequency range 1 MHz to 2000 × *S* MHz as follows in Equation (113–29):

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$$\text{PSAACRF}_N(f) = -10\log_{10}\sum_{j=1}^{m}\sum_{i=1}^{4} 10^{\frac{-AACRF(f)_{i,j,N}}{10}} \quad \text{(dB)} \qquad (113\text{–}29)$$

where

$AACRF(f)_{i,j,N}$ is the magnitude in dB of the alien ACRF at frequency f of the individual pair combination i (1 to 4) of the disturbing link j (1 to m) for each disturbed pair N

NOTE—ELFEXT used in 55.7 is changed to ACRF in Clause 113 to align with TIA and ISO/IEC cabling standards definitions.

The PSAACRF between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall meet the values determined using Equation (113–30).

$$\text{PSAACRF}(f) \geq 61 - 20\log_{10}\left(\frac{f}{100}\right) \quad \text{(dB)} \qquad 1 \leq f \leq 2000 \times S \qquad (113\text{–}30)$$

where

f is the frequency in MHz,

When Equation (113–30) values are greater than 75 dB, they revert to 75 dB.

113.7.4 Direct attach cable assembly—Short Reach Mode

The direct attach cable assembly is a 4-pair balanced twisted-pair link segment terminated in a connector at each end for use as a short reach link segment between MDIs. The direct attach cable assembly comprises a short reach link segment meeting the transmission requirements in 113.7.4 are specified to support up to 5 m. The transmission parameters of the short reach link segment include insertion loss, delay parameters, nominal impedance, NEXT loss, ACRF, and return loss. In addition, the requirements for the alien crosstalk coupled “between” link segments is specified

113.7.4.1 Insertion loss

The insertion loss of each direct attach cable assembly duplex channel shall meet the values determined using Equation (113–31):

$$\text{Insertion loss}(f) \leq 0.05 \times 1.5\left(1.8 \times \sqrt{f} + 0.005 \times f + \frac{0.25}{\sqrt{f}}\right) + 2 \times B + 0.0324 \times \sqrt{f} \quad \text{(dB)} \qquad (113\text{–}31)$$

where

f is the frequency in MHz; $1 \leq f \leq 2000 \times S$

$$B = \begin{bmatrix} 0.02 \times \sqrt{f} & 1 \leq f \leq 500 \\ 0.00649 \times \sqrt{f} + 0.000605 \times f & 500 < f \leq 2000 \times S \end{bmatrix} \quad \text{(dB)}$$

Calculations that result in insertion loss values less than 3 dB revert to a requirement of 3 dB.

113.7.4.2 Return loss

In order to limit the noise at the receiver due to impedance mismatches in the cabling system, each direct attach cable assembly link segment duplex channel shall meet the values determined using Equation (113–32)

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at all frequencies from 1 MHz to 2000 × *S* MHz. The reference impedance for the return loss specification is 100 Ω.

$$\text{Return Loss} \geq \begin{cases} 24 + 3\log_{10}\left(\frac{f}{25}\right) & 1 \leq f \leq 25 \\ 8 - 10\log_{10}\left(\frac{f}{1000}\right) & 25 < f \leq 1000 \\ 8 & 1000 \leq f < 1250 \\ 8 & 1250 \leq f < 1600 \text{ (for 40GBASE-T)} \\ 8 - 19\log_{10}\left(\frac{f}{1600}\right) & 1600 \leq f < 2000 \text{ (for 40GBASE-T)} \end{cases} \quad \text{(dB)} \qquad (113\text{–}32)$$

where

f is the frequency in MHz.

113.7.4.3 Coupling parameters between direct attach cable assembly duplex channels comprising one link segment

In order to limit the noise coupled into a direct attach cable assembly duplex channel from adjacent duplex channels, near-end crosstalk (NEXT) loss and attenuation to crosstalk ratio, far-end (ACRF) are specified for each direct attach cable assembly link segment. In addition, each duplex channel can be disturbed by more than one duplex channel. To ensure the total NEXT loss and FEXT loss coupled into a duplex channel is limited, multiple disturber near-end crosstalk (MDNEXT) and multiple disturber ACRF (MDACRF) is specified.

113.7.4.3.1 Differential near-end crosstalk

In order to limit the crosstalk at the near end of a direct attach cable assembly link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between a duplex channel and the other three duplex channels is specified to meet the bit error ratio objective specified in 113.1.2. The NEXT loss between any two duplex channels of a direct attach cable assembly link segment shall meet the values determined using Table 113–22.

Table 113–22—Direct Attach NEXT Loss

Frequency (MHz)	NEXT Loss (dB)
$1 \leq f < 250$	$82.9 - 18.5\log_{10}(f)$
$250 \leq f < 383$	$93 - 22.72\log_{10}(f)$
$383 \leq f < 500$	$109 - 28.92\log_{10}(f)$
$500 \leq f \leq 2000 \times S$	$133.5 - 38\log_{10}(f)$
Calculations that result in values greater than 65dB revert to 65dB.	

113.7.4.3.2 Multiple disturber near-end crosstalk (MDNEXT) loss

Since four direct attach cable assembly duplex channels are used to transfer data between PMAs, the NEXT that is coupled into a data carrying duplex channel is from the three adjacent disturbing duplex channels.

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To ensure the total NEXT coupled into a duplex channel is limited, multiple disturber NEXT loss is specified as the power sum of the individual NEXT losses. The power sum loss between a duplex channel and the three adjacent disturbers shall meet the values determined Table 113–23.

Table 113–23—Direct Attach MDNEXT Loss

Frequency (MHz)	MDNEXT Loss (dB)
$1 \le f < 250$	$79.4 - 18.5\log_{10}(f)$
$250 \le f < 331$	$90.65 - 23.2\log_{10}(f)$
$331 \le f < 500$	$105.26 - 29\log_{10}(f)$
$500 \le f \le 2000 \times S$	$129.5 - 38\log_{10}(f)$
Calculations that result in values greater than 62dB revert to 62dB.	

113.7.4.3.3 Multiple disturber power sum near-end crosstalk (PSNEXT) loss

PSNEXT loss is determined by summing the power of the three individual pair-to-pair differential NEXT loss values over the frequency range 1 MHz to $2000 \times S$ MHz in Equation (113–21).

113.7.4.3.4 Attenuation to crosstalk ratio, far end (ACRF)

Attenuation to crosstalk ratio, far-end (ACRF) is specified in order to limit the crosstalk at the far end of each direct attach cable assembly link segment duplex channel and meet the bit error ratio objective specified in 113.1.2. Far-end crosstalk (FEXT) is crosstalk that appears at the far end of a duplex channel (disturbed channel), which is coupled from another duplex channel (disturbing channel) with the noise source (transmitters) at the near end. FEXT loss is defined in Equation (113–22). ACRF is defined in Equation (113–23).

The worst pair ACRF between any two direct attach cable assembly duplex channels shall meet the values determined using Equation (113–33).

$$\mathrm{ACRF}(f) \ge -20\log_{10}\left[10^{\frac{10\log_{10}\left(\frac{24}{5}\right) + 40 - 20\log_{10}\left(\frac{f}{100}\right)}{-20}} + 2 \times 10^{\frac{48.1 - 20\log_{10}\left(\frac{f}{100}\right)}{-20}}\right] \text{ (dB)}$$

where (113–33)

f is the frequency in MHz $1 \le f \le 2000 \times S$.

When Equation (113–33) values are greater than 65 dB, they revert to 65 dB.

113.7.4.3.5 Multiple disturber attenuation to crosstalk ratio, far-end (MDACRF)

Since four direct attach cable assembly duplex channels are used to transfer data between PMAs, the FEXT that is coupled into a data carrying duplex channel is from the three adjacent disturbing duplex channels. To ensure the total FEXT coupled into a duplex channel is limited, multiple disturber ACRF is specified as the

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power sum of the individual ACRF disturbers. PS ACRF is determined by summing the power of the three individual pair-to-pair differential ACRF values over the frequency range 1 MHz to $2000 \times S$ MHz in Equation (113–26).

The power sum loss between a duplex channel and the three adjacent disturbers shall meet the values determined using Equation (113–34).

$$\mathrm{MDACRF}(f) \geq -20\log_{10}\left[10^{\frac{10\log_{10}\left(\frac{24}{5}\right)+37-20\log_{10}\left(\frac{f}{100}\right)}{-20}} + 2 \times 10^{\frac{45.1-20\log_{10}\left(\frac{f}{100}\right)}{-20}}\right] \text{(dB)} \quad (113\text{–}34)$$

where

f is the frequency $1 \leq f \leq 2000 \times S$.

When Equation (113–34) values are greater than 62 dB, they revert to 62 dB.

113.7.4.3.6 Maximum link delay

The propagation delay of a link segment shall not exceed 32 ns at all frequencies between 2 MHz and $2000 \times S$ MHz.

113.7.4.3.7 Link delay skew

The difference in propagation delay, or skew, between all duplex channel pair combinations of a link segment, under all conditions, shall not exceed 4.8 ns at all frequencies from 2 MHz to $2000 \times S$ MHz. It is a further functional requirement that, once installed, the skew between any two of the four duplex channels due to environmental conditions shall not vary more than 0.5 ns within the above requirement.

113.7.4.3.8 Multiple disturber alien near-end crosstalk (MDANEXT) loss

Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as *alien crosstalk noise*. In order to limit the alien crosstalk at the near end of a link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is specified to meet the bit error ratio objective specified in 113.1.2. To ensure the total alien NEXT coupled into a duplex channel is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT disturbers.

113.7.4.3.9 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

PSANEXT loss is determined by summing the power of the individual pair-to-pair differential alien NEXT loss values over the frequency range 1 MHz to $2000 \times S$ MHz in Equation (113–27).

The power sum ANEXT loss between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall meet the values determined using Equation (113–35) independent of length.

$$\mathrm{PSANEXT}(f) = 85 - 15\log_{10}\left(\frac{f}{100}\right) \text{ (dB)} \qquad 1 \leq f \leq 2000 \times S \qquad (113\text{–}35)$$

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where

f is the frequency in MHz

When Equation (113–35) values are greater than 75 dB, they revert to 75 dB.

113.7.4.3.10 Multiple disturber power sum alien attenuation to crosstalk, far end crosstalk (PSAACRF)

Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. In order to limit the alien crosstalk at the far-end of a link segment, the differential pair-to-pair alien far-end crosstalk loss between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is specified to meet the bit error ratio objective specified in 113.1.2. To ensure the total alien FEXT coupled into a duplex channel is limited, multiple disturber ACRF is specified as the power sum of the individual alien ACRF disturbers.

Power sum alien ACRF is determined by summing the power of the individual pair-to-pair differential alien ACRF values over the frequency range 1 MHz to 2000 × S MHz as follows in Equation (113–36):

$$\mathrm{PSAACRF}_N(f) = -10\log_{10}\sum_{j=1}^{m}\sum_{i=1}^{4} 10^{\frac{-AL(f)_{i,j,N}}{10}} \quad (\mathrm{dB}) \qquad (113\text{–}36)$$

where

$AL(f)_{i,j,N}$ is the magnitude in dB of the alien ACRF at frequency f of the individual pair combination i (1 to 4) of the disturbing link j (1 to m) for each disturbed pair N.

NOTE—ELFEXT used in 55.7 is changed to ACRF in Clause 113 to align with TIA and ISO/IEC cabling standards definitions.

The PSAACRF between a disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments shall meet the values determined using Equation (113–37).

$$\mathrm{PSAACRF}(f) \geq 61 - 20\log_{10}\left(\frac{f}{100}\right) \quad (dB) \qquad 1 \leq f \leq 2000 \times S \qquad (113\text{–}37)$$

where

f is the frequency in MHz,

When Equation (113–37) values are greater than 75 dB, they revert to 75 dB.

113.7.5 Noise environment

The 25G/40GBASE-T noise environment consists of the following:

a) Echo from the local transmitter on the same duplex channel (cable pair). Echo is caused by the hybrid function used to achieve simultaneous bi-directional transmission of data and by impedance mismatches in the link segment. It is impractical to achieve the objective BER without using echo cancellation. Since the symbols transmitted by the local disturbing transmitter are available to the

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cancellation processor, echo interference can be reduced to a small residual noise using echo cancellation methods.

b) Near-end crosstalk (NEXT) interference from the local transmitters on the duplex channels (cable pairs) of the link segment. Each receiver experiences NEXT interference from three adjacent transmitters. NEXT cancellers are used to reduce the interference from each of the three disturbing transmitters to a small residual noise. NEXT cancellation is possible since the symbols transmitted by the three disturbing local transmitters are available to the cancellation processor.

c) Far-end crosstalk (FEXT) noise at a receiver is from three disturbing transmitters at the far end of the duplex channel (cable pairs) of the link segment. FEXT noise can be reduced through cross coupled equalizers although the symbols from the remote transmitters are not immediately available.

d) Intersymbol interference (ISI). ISI is the extraneous energy from one signaling symbol that interferes with the reception of another symbol on the same balanced twisted pair. 25G/40GBASE-T supports the use of Tomlinson-Harashima Precoding as a mechanism to reduce the effects of ISI.

e) Noise from non-idealities in the duplex channel, transmitters, and receivers; for example, DAC/ADC non-linearity, electrical noise (shot and thermal), and nonlinear duplex channel characteristics. 25G/40GBASE-T limits the effects of some of these non-idealities by a variety of PMA electrical specifications.

f) Noise coupled between link segments. Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. Since the transmitted symbols from the alien crosstalk noise sources are not available to the cancellation processor (they are in another cable), it is very difficult to cancel the alien crosstalk noise. To ensure robust operation the alien crosstalk is specified in 113.7.3.

g) The background noise for 25G/40GBASE-T is expected not to exceed –150 dBm/Hz. A background noise limit of –150 dBm/Hz was assumed for determining the minimum signal-to-noise ratio.

113.8 MDI specification

This subclause defines the MDI. The link topology requires a crossover function in a DTE-to-DTE connection. See 113.4.4 for a description of the automatic MDI/MDI-X configuration.

113.8.1 MDI connectors

Eight-pin connectors meeting the requirements of IEC 60603-7-51 with the improved characteristics and frequency extensions specified in IEC 60603-7-81 shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figure 113–39 and Figure 113–40. The assignment of PMA signals to connector contacts for PHYs is shown in Table 113–24.

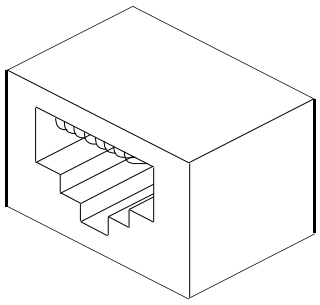

Figure 113–39—MDI connector

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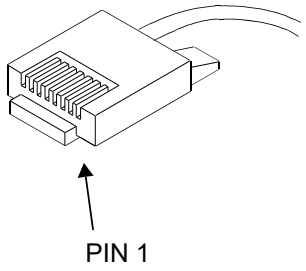

Figure 113–40—Balanced cabling connector

Table 113–24—Assignment of PMA signal to MDI and MDI-X pin-outs

Contact	MDI	MDI-X
1	BI_DA+	BI_DB+
2	BI_DA–	BI_DB–
3	BI_DB+	BI_DA+
4	BI_DC+	BI_DD+
5	BI_DC–	BI_DD–
6	BI_DB–	BI_DA–
7	BI_DD+	BI_DC+
8	BI_DD–	BI_DC–

113.8.2 MDI electrical specifications

The MDI connector (jack) when mated with a specified balanced cabling connector (plug) shall meet the FEXT requirements as specified in Equation (113–38):

$$\text{FEXT loss} \geq 43.1 - 20\log_{10}(f/100) \quad \text{(dB)} \tag{113–38}$$

where f is the frequency over the range 1 MHz to $2000 \times S$ MHz between all contact pair combinations shown in Table 113–24.

No spurious signals shall be emitted onto the MDI when the PHY is held in power-down mode (as defined in 22.2.4.1.5), when released from power-down mode, or when external power is first applied to the PHY.

113.8.2.1 MDI return loss

The differential impedance at the MDI for each duplex channel shall be such that any reflection due to differential signals incident upon the MDI from a balanced cabling having a nominal differential characteristic impedance of 100 Ω is attenuated, relative to the incident signal as per the relationship shown in Equation (113–39):

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$$\text{Return loss} \geq \begin{cases} 16 & 1 \leq f \leq 40 \quad \text{(dB)} \\ 16 - 10\log_{10}(f/40) & 40 < f \leq 400 \quad \text{(dB)} \\ 6 & 400 < f \leq 2000 \times S \quad \text{(dB)} \end{cases} \tag{113–39}$$

where f is in MHz.

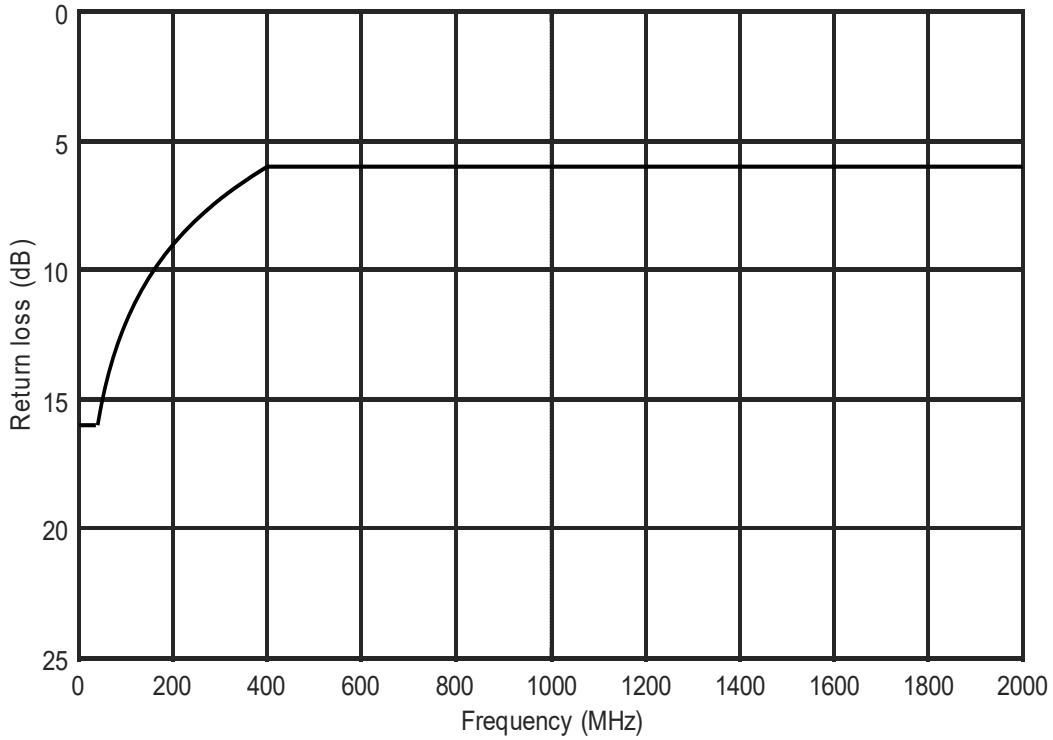

Figure 113–41—MDI return loss

113.8.2.2 MDI impedance balance

Impedance balance is a measure of the impedance-to-ground difference between the two MDI contacts used by a duplex channel and is referred to as *common-mode-to-differential-mode impedance balance*. When the transmitter is transmitting random or pseudo random data, the common-mode-to-differential-mode impedance balance, *Bal*(*f*), of each duplex channel of the MDI shall meet the relationship shown in Equation (113–40):

$$Bal(f) \geq \begin{cases} 48 & 1 \leq f \leq 40 \quad \text{(dB)} \\ 44 - 19.2\log_{10}(f/40) & 40 < f \leq 2000 \times S \quad \text{(dB)} \end{cases} \tag{113–40}$$

where f is the frequency in MHz. Test mode 5 may be used to generate an appropriate transmitter output.

The impedance balance is defined as the S parameter measurement of Sdc11 in dB at the MDI.

The impedance balance may be measured with a mixed mode four port network analyzer capable of measuring the common-mode voltage and differential mode voltage of a balanced port. Impedance balance is the S parameter measurement of Sdc11 in dB at the MDI where two ports of the four port network analyzer are connected between two MDI contacts used by a duplex channel and these two ports are configured as a single balanced port. For this test the PHY ground is connected to the network analyzer

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ground. The other two ports of the network analyzer are unconnected. The network analyzer should be capable of measuring Sdc11 to at least –60 dB and should use a differential input impedance of 100 Ω and a common-mode impedance of 75 Ω.

During the test the PHY is connected to the MDI as in normal operation.

113.8.2.3 MDI fault tolerance

Each wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to any other wire within the 4-pair cable for an indefinite period of time and shall resume normal operation after the short circuit(s) are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

A 25G/40GBASE-T PHY shall be able to sustain, without damage, connection to a PSE and shall not cause damage to the PSE as defined in 33.2.

Each wire pair shall withstand without damage a 1000 V common-mode impulse of either polarity. The shape of the impulse is 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060. See Figure 40–34 in 40.8.3.4.

113.9 Environmental specifications

113.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

113.9.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cabling systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards should be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures should be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

113.9.3 Installation and maintenance guidelines

It is recommended that sound installation practice, including screen management, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable. Installation practices for screened cabling are found in ISO/IEC 14763-2.

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It is a mandatory requirement that, during installation of the cabling plant, care be taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

113.9.4 Telephone voltages

The use of building wiring brings with it the possibility of wiring errors that connect telephony voltages to 25G/40GBASE-T. Other than voice signals (which are low voltage), the primary voltages that can be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply.

a) Battery voltage to a telephone line is generally 56 V dc applied to the line through a balanced 400 Ω source impedance.
b) Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 V dc with a 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 25G/40GBASE-T equipment is not required to survive such wiring hazards without damage, application of any of the preceding voltages shall not result in any safety hazard.

113.9.5 Electromagnetic compatibility

A system integrating the 25G/40GBASE-T shall comply with applicable local and national codes for the limitation of electromagnetic interference.

113.9.6 Temperature and humidity

A system integrating the 25G/40GBASE-T is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

113.10 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability and units thereof
b) Power level in terms of maximum current drain (for external PHYs)
c) Port type (i.e., 25GBASE-T or 40GBASE-T)
d) Any applicable safety warnings
e) EEE support
f) Fast retrain support

113.11 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of a 25GBASE-T or 40GBASE-T PHY shall not exceed 25 600 BT. Transmit data delay is measured from the input of a given unit of data at the 25GMII or XLGMII to the presentation of the same unit of data by the PHY to the MDI. Receive data

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delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the 25GMII or XLGMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link. Equation (105–1) specifies the calculation of bit time per meter of electrical cable for 25GBASE-T. Equation (80–1) specifies the delay per meter of electrical cable in nanoseconds and may be used for 40GBASE-T, given the bit time for 40 Gb/s Ethernet of 25 ps (see notes to Table 80–7).

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113.12 Protocol implementation conformance statement (PICS) proforma for Clause 113, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, types 25GBASE-T and 40GBASE-T[191]

The supplier of a protocol implementation that is claimed to conform to Clause 113, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, types 25GBASE-T and 40GBASE-T, shall complete the protocol implementation conformance statement (PICS) proforma listed in the following subclauses.

Instructions for interpreting and filling out the PICS proforma are found in Clause 21.

113.12.1 Identification

113.12.1.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

113.12.1.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 113, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, types 25GBASE-T and 40GBASE-T
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exceptions items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[191] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so it can be used for its intended purpose and may further publish the completed PICS.

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113.12.2 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
25GE	25GMII compatibility interface	106, 113.1.5	O	Yes [ ] No [ ]	Compatibility interface is supported
XGE	XLGMII compatibility interface	81, 113.1.5	O	Yes [ ] No [ ]	Compatibility interface is supported
*EEE	Support of EEE capability		O	Yes [ ] No [ ]	113.1.3.3
*FR	Support of Fast Retrain capability		O	Yes [ ] No [ ]	113.4.2.5.16
*INS	Installation / cabling	113.7	O	Yes [ ] No [ ]	Items marked with INS include installation practices and cabling specifications not applicable to a PHY manufacturer
*MDIO	MDIO capability	113.1	O	Yes [ ] No [ ]	Registers and interface supported

113.12.3 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Status	Support	Value/Comment
PCT1	PCS Transmit function state diagram	113.3.2.2	M	Yes [ ]	See Figure 113–18a
PCT2	PCS Transmit function state diagram with EEE states	113.3.2.2	EEE:M	Yes [ ]	See Figure 113–18a and Figure 113–18b
PCT3	PCS Transmit bit ordering	113.3.2.2	M	Yes [ ]	See Figure 113–6 and Figure 113–8
PCT4	SEND_Z encoding	113.3.2.2	M	Yes [ ]	
PCT5	SEND_T encoding	113.3.2.2	M	Yes [ ]	
PCT6	SEND_N encoding	113.3.2.2	M	Yes [ ]	
PCT7	Invalid control code handling	113.3.2.2.6	M	Yes [ ]	
PCT8	/I/ insertion and deletion	113.3.2.2.8	M	Yes [ ]	
PCT9	/LI/ insertion and deletion	113.3.2.2.9	EEE:M	Yes [ ]	
PCT10	/O/ deletion	113.3.2.2.12	M	Yes [ ]	
PCT11	Scrambler as MASTER	113.3.2.2.15	M	Yes [ ]	
PCT12	Scrambler as SLAVE	113.3.2.2.15	M	Yes [ ]	
PCT13	RS-FEC encoding	113.3.2.2.19	M	Yes [ ]	See Figure 113–13
PCT14	LDPC encoding	113.3.2.2.18	M	Yes [ ]	Generator matrix is described in Annex 55A
PCT15	DSQ128 mapping	113.3.2.2.20	M	Yes [ ]	
PCT16	EEE Transmit function state diagram	113.3.2.2.23	EEE:M	Yes [ ]	See Figure 113–20

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Item	Feature	Subclause	Status	Support	Value/Comment
PCT17	LP_IDLE input to scrambler during LPI mode	113.3.2.2.23	EEE:M	Yes [ ]	
PCT18	lpi_tx_mode control	113.3.2.2.23	EEE:M	Yes [ ]	
PCT19	PCS test pattern mode	113.3.3	M	Yes [ ]	See Figure 113–6
PCT20	PMA training - MASTER scrambler	113.3.4	M	Yes [ ]	
PCT21	PMA training - SLAVE scrambler	113.3.4	M	Yes [ ]	
PCT22	PMA training scrambler initial state	113.3.4	M	Yes [ ]	In no case shall the scrambler state be initialized to all zeros
PCT23	LPI active pair and refresh_active signals	113.3.5.1	EEE:M	Yes [ ]	
PCT24	Alert signaling in place of refresh signaling	113.3.5.3	EEE:M	Yes [ ]	
PCT25	Slave synchronization	113.3.5.1	EEE:M	Yes [ ]	
PCT26	Quiet launch power	113.3.5.2	EEE:M	Yes [ ]	
PCT27	LPI sleep timer	113.3.6.2.3	EEE:M	Yes [ ]	
PCT28	LPI alert timer	113.3.6.2.3	EEE:M	Yes [ ]	
PCT29	LPI wake timer	113.3.6.2.3	EEE:M	Yes [ ]	
PCT30	LPI rx wake timer	113.3.6.2.3	EEE:M	Yes [ ]	
PCT31	LPI tx wake timer	113.3.6.2.3	EEE:M	Yes [ ]	
PCT32	LPI scrambler	113.3.5.3	EEE:M	Yes [ ]	The training sequence shall be used during the LPI mode
PCT33	Refresh using THP	113.3.5.3	EEE:M	Yes [ ]	
PCT34	Reset THP at the start of refresh	113.3.5.3	EEE:M	Yes [ ]	
PCT35	Master alert on pair A, other pairs silent	113.3.5.3	EEE:M	Yes [ ]	
PCT36	Slave alert on pair C, other pairs silent	113.3.5.3	EEE:M	Yes [ ]	
PCT37	Inactive pairs transmit zeros	113.3.5.3	EEE:M	Yes [ ]	
PCT38	ENCODE function	113.3.6.2.4	M	Yes [ ]	Encode the block as specified in 113.3.2.2.2
PCT39	PCS loopback setup	113.3.7.3	M	Yes [ ]	

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113.12.3.1 PCS Receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR1	PCS Receive function state diagram	113.3.2.3	M	Yes [ ]	See Figure 113–19a and state variables as specified in 113.3.6.2.
PCR2	PCS Receive bit ordering	113.3.2.3.1	M	Yes [ ]	See Figure 113–7
PCR3	Descrambling as MASTER	113.3.2.3.2	M	Yes [ ]	
PCR4	Descrambling as SLAVE	113.3.2.3.2	M	Yes [ ]	
PCR5	PMA training descrambler-MASTER	113.3.4.3	M	Yes [ ]	
PCR6	PMA training descrambler-SLAVE	113.3.4.3	M	Yes [ ]	
PCR7	DECODE operation	113.3.6.2.4	M	Yes [ ]	Decode the block as specified in 113.3.4
PCR8	LFER monitor	113.3.6.3	M	Yes [ ]	See state diagrams in Figure 113–17, Figure 113–18a, and Figure 113–19a.

113.12.3.2 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	PCS Reset function	113.3.2.1	M	Yes [ ]	

113.12.4 Physical Medium Attachment (PMA)

Item	Feature	Subclause	Status	Support	Value/Comment
PMF1	PMA Reset function	113.4.2.1	M	Yes [ ]	
PMF2	PMA transmission	113.4.2.2	M	Yes [ ]	
PMF3	Transmitter clocking	113.4.2.2	M	Yes [ ]	All driven by TX_TCLK
PMF4	PMA Transmit mapping	113.4.2.2	M	Yes [ ]	Per mathematical description given in 113.4.3.1
PMF5	PMA Transmit electrical compliance	113.4.2.2	M	Yes [ ]	See PMA electrical specifications given in 113.5
PMF6	Clocking as MASTER	113.4.2.2	M	Yes [ ]	Source the transmit clock TX_TCLK from a local clock
PMF7	Clocking as SLAVE in loop timed mode	113.4.2.2	M	Yes [ ]	Source the transmit clock TX_TCLK from the recovered clock

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Item	Feature	Subclause	Status	Support	Value/Comment
PMF8	Transmit fault mapping	113.4.2.2	O	Yes [ ]	Contribute to the transmit fault bit as specified in 45.2.1.7.4
PMF9	Generates alert signal	113.4.2.2	EEE:M	Yes [ ]	Generates the alert signal defined in 113.4.2.2.1
PMF10	Generates link failure signaling	113.4.2.2	FR:M	Yes [ ] No [ ]	Generates the link failure signal defined in 113.4.2.2.2
PMF11	PMA Receive function performance	113.4.2.4	M	Yes [ ]	LDPC frame error ratio of less than 3.2×10^{-9}
PMF12	Receive fault mapping	113.4.2.4	O	Yes [ ]	Contribute to the receive fault bit as specified in 45.2.1.7.5
PMF13	Implement alert_detect	113.4.2.4	EEE:M	Yes [ ]	Generates alert_detect when the alert signal is detected at the receiver
PMF14	Detect link failure signaling	113.4.2.4	FR:M	Yes [ ] No [ ]	Sets link_fail_detect to true when the link failure signal is detected
PMF15	PHY Control function	113.4.2.5	M	Yes [ ]	See state diagram in Figure 113–28 and state diagrams in Figure 113–29 and Figure 113–30
PMF16	Infofield	113.4.2.5	M	Yes [ ]	All subclauses from 113.4.2.5.1 to 113.4.2.5.14
PMF17	THP initialization	113.4.2.5.15	M	Yes [ ]	Last 16 symbols of PMA_Coeff_Exch
PMF18	PBO exchange	113.4.2.5.15	M	Yes [ ]	
PMF19	Slave PBO setting	113.4.2.5.15	M	Yes [ ]	Slave's PBO final setting within two levels (4 dB) of the MASTER's PBO level
PMF20	THP coefficient exchange	113.4.2.5.15	M	Yes [ ]	
PMF21	Recommended startup sequence timing	113.4.2.5.15	O	Yes [ ] No [ ]	See Table 113–13
PMF22	Implements fast retrain state diagram	113.4.2.5.16	FR:M	Yes [ ] No [ ]	
PMF23	Behavior after fast retrain request	113.4.2.5.16	FR:M	Yes [ ] No [ ]	Transmit PAM2 within 9 LDPC frame periods following link failure request
PMF24	Behavior after fast retrain signal detection	113.4.2.5.16	FR:M	Yes [ ] No [ ]	Transmit PAM2 within 9 LDPC frame periods following link failure signal detection
PMF25	Implements THP bypass request	113.4.2.5.16	FR:M	Yes [ ] No [ ]	Bypasses THP (or sets coefficients to zeros) when LP requests THP bypass on Fast Retrain
PMF26	Link Monitor	113.4.2.6	M	Yes [ ]	See state diagram in Figure 113–31

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Item	Feature	Subclause	Status	Support	Value/Comment
PMF27	Refresh monitor state diagram	113.4.2.7	EEE:M	Yes [ ] No [ ]	Implements state diagram of Figure 113–19b
PMF28	Recommended fast retrain sequence timing	113.4.2.5.16	FR:O	Yes [ ] No [ ]	See Table 113–14
PMF29	Clock Recovery function	113.4.2.8	M	Yes [ ]	
PMF30	MDIX for EEE refreshes and alert	113.4.4	EEE:M	Yes [ ]	
PMF31	Symbol response	113.4.3.1	M	Yes [ ]	Per electrical specifications given in 113.5
PMF32	THP filter coefficient setting	113.4.3.1	M	Yes [ ]	Fixed after startup
PMF33	PMA Transmit power backoff settings	113.4.3.1	M	Yes [ ]	
PMF34	Minimum power backoff requested	113.4.3.1	M	Yes [ ]	Per Table 113–15
PMF35	Automatic configuration	113.4.4	M	Yes [ ]	Comply with the specifications of 40.4.4.1 and 40.4.4.2
PMF36	Pair/Polarity swap detection and correction	113.4.4	M	Yes [ ]	
PMF37	PMA_CONFIG.indication generation	113.4.5.1	M	Yes [ ]	
PMF38	Maxwait_timer expiration	113.4.5.2	M	Yes [ ]	
PMF39	Minwait_timer expiration	113.4.5.2	M	Yes [ ]	

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113.12.5 Management interface

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	Support for Auto-Negotiation	113.6.1	M	Yes [ ]	See Clause 28
MF2	MASTER and SLAVE operation	113.6.1	M	Yes [ ]	Capable of operating either as MASTER or SLAVE
MF3	Extended Next Page support	113.6.1	M	Yes [ ]	
MF4	Optimized FLP timing	113.6.1	M	Yes [ ]	
MF5	Management registers	113.6.1.1	M	Yes [ ]	As defined in Table 113–18
MF6	25G/40GBASE-T Extended Next Page bit assignments	113.6.1.2	M	Yes [ ]	As defined in Table 113–19
MF7	EEE advertisement	113.6.1.2	EEE:M	Yes [ ]	As defined in Table 113–19
MF8	Fast retrain ability advertisement	113.6.1.2	FR:M	Yes [ ]	As defined in Table 113–19
MF9	Resolution completion	113.6.2	M	Yes [ ]	Successful completion of resolution treated as MASTER-SLAVE configuration resolution complete.
MF10	Seed counter	113.6.2	M	Yes [ ]	Counter provided to track number of seed attempts
MF11	Counter set to zero at startup	113.6.2	M	Yes [ ]	
MF12	Counter increment	113.6.2	M	Yes [ ]	
MF13	Counter reset	113.6.2	M	Yes [ ]	After resolution is complete
MF14	Bit 7.33.15 set to zero after resolution is complete	113.6.2	M	Yes [ ]	After resolution is complete
MF15	Resolution fault declared	113.6.2	M	Yes [ ]	After generation of seven seeds
MF16	MASTER-SLAVE fault condition	113.6.2	M	Yes [ ]	Condition occurs when both devices manually select MASTER or SLAVE
MF17	MASTER-SLAVE fault condition bit	113.6.2	M	Yes [ ]	Set to one upon fault condition
MF18	MASTER-SLAVE fault resolution	113.6.2	M	Yes [ ]	Fault condition treated as MASTER-SLAVE resolution complete
MF19	MASTER-SLAVE fault condition indication	113.6.2	M	Yes [ ]	link_status_40GigT set to FAIL

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113.12.6 PMA Electrical Specifications

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	Electrical isolation	113.5.1	M	Yes [ ]	Conforms to J.1
PME2	Insulation breakdown after test	113.5.1	M	Yes [ ]	Conforms to J.1
PME3	Test modes supported	113.5.2	M	Yes [ ]	
PME4	Test mode enablement	113.5.2	M	Yes [ ]	Per management register settings shown in Table 113–16
PME5	The test modes only change the data symbols	113.5.2	M	Yes [ ]	
PME6	Provide a means to enable the test modes	113.5.2	!MDIO: M	Yes [ ] N/A [ ]	
PME7	Test mode 1 operation	113.5.2	M	Yes [ ]	
PME8	Test mode 2 operation	113.5.2	M	Yes [ ]	
PME9	Test mode 3 operation, pair D	113.5.2	M	Yes [ ]	
PME10	Test mode 3 operation, pairs A, B and C	113.5.2	M	Yes [ ]	Transmit silence
PME11	Test mode 4 waveform	113.5.2	M	Yes [ ]	Tones per Table 113–17
PME12	Test mode 4 levels	113.5.2	M	Yes [ ]	
PME13	Test mode 5 operation	113.5.2	M	Yes [ ]	
PME14	Test mode 6 operation	113.5.2	M	Yes [ ]	
PME15	Test mode 7 operation	113.5.2	M	Yes [ ]	
PME16	Text fixture 3 isolation	113.5.2	M	Yes [ ]	>30 dB between signals on any of {pairs A, B, C} and pair D
PME17	Transmitter nominal load	113.5.3	M	Yes [ ]	
PME18	AC-coupling to the MDI	113.5.3	M	Yes [ ]	
PME19	Droop test	113.5.3.1	M	Yes [ ]	
PME20	SFDR of transmitter	113.5.3.2	M	Yes [ ]	
PME21	Transmitter jitter as MASTER	113.5.3.3	M	Yes [ ]	
PME22	Transmitter jitter as loop-timed SLAVE	113.5.3.3	M	Yes [ ]	
PME23	Transmit power level	113.5.3.4	M	Yes [ ]	
PME24	Transmitter PSD	113.5.3.4	M	Yes [ ]	
PME25	MASTER symbol rate	113.5.3.5	M	Yes [ ]	
PME26	Maximum short term rate of frequency variation during LPI	113.5.3.5	EEE:M	Yes [ ]	Less than 0.1 ppm/s
PME27	Maximum short term rate of frequency variation when switching to and from LPI	113.5.3.5	EEE:M	Yes [ ]	Less than 0.1 ppm/s

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Item	Feature	Subclause	Status	Support	Value/Comment
PME28	BER over a 113.7 compliant link	113.5.4.1	M	Yes [ ]	
PME29	Receiver frequency tolerance	113.5.4.2	M	Yes [ ]	
PME30	Alien noise tolerance	113.5.4.4	M	Yes [ ]	
PME31	BER over a 113.7.4 compliant link	113.5.4.5	M	Yes [ ]	

113.12.7 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	MDI compatibility	113.7	INS:M	Yes [ ]	
LKS2	Insertion loss of each duplex channel	113.7.2.1	INS:M	Yes [ ]	See Equation (113–13)
LKS3	Return loss	113.7.2.3	INS:M	Yes [ ]	See Equation (113–14)
LKS4	NEXT loss within pairs in a link segment	113.7.2.4.1	INS:M	Yes [ ]	See Equation (113–15)
LKS5	Power sum NEXT loss	113.7.2.4.2	INS:M	Yes [ ]	See Equation (113–18), Equation (113–19), and Equation (113–20)
LKS6	Worst pair ACRF loss	113.7.2.4.4	INS:M	Yes [ ]	See Equation (113–24)
LKS7	Power sum ACRF loss	113.7.2.4.5	INS:M	Yes [ ]	See Equation (113–25)
LKS8	Propagation delay	113.7.2.5	INS:M	Yes [ ]	
LKS9	Delay skew	113.7.2.6	INS:M	Yes [ ]	
LKS10	Delay skew change	113.7.2.6	INS:M	Yes [ ]	
LKS11	Power sum ANEXT loss	113.7.3.1.1	INS:M	Yes [ ]	See Equation (113–28)
LKS12	PS AACRF loss	113.7.3.2.1	INS:M	Yes [ ]	See Equation (113–30)

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113.12.8 Characteristics of the direct attach cable assembly

Item	Feature	Subclause	Status	Support	Value/Comment
DAC1	Insertion loss of each duplex channel	113.7.4.1	INS:M	Yes [ ]	See Equation (113–31)
DAC2	Return loss	113.7.4.2	INS:M	Yes [ ]	See Equation (113–32)
DAC3	NEXT loss within pairs in a link segment	113.7.4.3.1	INS:M	Yes [ ]	See Table 113–22
DAC4	Power sum NEXT loss	113.7.4.3.2	INS:M	Yes [ ]	See Table 113–23
DAC5	Worst pair ACRF loss	113.7.4.3.4	INS:M	Yes [ ]	See Equation (113–33)
DAC6	Power sum ACRF loss	113.7.4.3.5	INS:M	Yes [ ]	See Equation (113–26)
DAC7	Propagation delay	113.7.4.3.6	INS:M	Yes [ ]	
DAC8	Delay skew	113.7.4.3.7	INS:M	Yes [ ]	
DAC9	Delay skew change	113.7.4.3.7	INS:M	Yes [ ]	
DAC10	Power sum ANEXT loss	113.7.4.3.9	INS:M	Yes [ ]	See Equation (113–35)
DAC11	PS AACRF loss	113.7.4.3.10	INS:M	Yes [ ]	See Equation (113–37)

113.12.9 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	113.8.1	M	Yes [ ]	Eight-pin connectors meeting the requirements of IEC 60603-7-51 with the improved characteristics and frequency extensions specified in IEC 60603-7-81.
MDI2	Cabling connector	113.8.1	INS:M	Yes [ ]	Plug
MDI3	PHY connector	113.8.1	M	Yes [ ]	Jack (as opposed to plug)
MDI4	MDI connector jack plus plug performance	113.8.2	INS:M	Yes [ ]	
MDI5	Mated MDI connector FEXT loss	113.8.2	INS:M	Yes [ ]	Per Equation (113–38)
MDI6	MDI power down	113.8.2	M	Yes [ ]	
MDI7	MDI return loss	113.8.2.1	M	Yes [ ]	
MDI8	MDI impedance balance	113.8.2.2	M	Yes [ ]	
MDI9	MDI fault tolerance to short circuits	113.8.2.3	M	Yes [ ]	No damage with an indefinite short
MDI10	Recovery from short	113.8.2.3	M	Yes [ ]	
MDI11	Short circuit current	113.8.2.3	M	Yes [ ]	Less than 300 mA

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Item	Feature	Subclause	Status	Support	Value/Comment
MDI12	Connection to PSE	113.8.2.3	M	Yes [ ]	No damage to PHY
MDI13	Connection to PSE	113.8.2.3	M	Yes [ ]	No damage to PSE
MDI14	Common-mode impulse tolerance	113.8.2.3	M	Yes [ ]	1000 V common-mode impulse of either polarity

113.12.10 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ENV1	Conformance to safety specifications	113.9.1	M	Yes [ ]	Conforms to J.2
ENV2	Installation isolation integrity	113.9.3	INS:M	N/A [ ] Yes [ ]	No electrical contact with unintended conductors or ground
ENV3	Phone voltage immunity	113.9.4	M	Yes [ ]	
ENV4	Electromagnetic compatibility	113.9.5	INS:M	N/A [ ] Yes [ ]	With local and national codes

113.12.11 Timing requirements

Item	Feature	Subclause	Status	Support	Value/Comment
TR1	Delay	113.11	M	Yes [ ]	

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114. Physical Medium Dependent (PMD) sublayer and medium, types 25GBASE-LR and 25GBASE-ER

114.1 Overview

This clause specifies the 25GBASE-LR PMD and 25GBASE-ER PMD together with the single-mode fiber medium. The PMD sublayer provides a point-to-point 25 Gb/s Ethernet link over a pair of single-mode fibers. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 114–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 114–1—Physical Layer clauses associated with the 25GBASE-LR and 25GBASE-ER PMDs

Associated clause	25GBASE-LR	25GBASE-ER
106—RS	Required	Required
106—25GMII[a]	Optional	Optional
107—PCS for 25GBASE-R	Required	Required
108—RS-FEC[b]	Required	Required
109—PMA for 25GBASE-R	Required	Required
109A—25GAUI C2C	Optional	Optional
109B—25GAUI C2M	Optional	Optional
78—Energy Efficient Ethernet	Optional	Optional

[a]The 25GMII is an optional interface. However, if the 25GMII is not implemented, a conforming implementation behaves functionally as though the RS and 25GMII were present.
[b]The option to bypass the Clause 108 RS-FEC correction function is not supported.

Figure 114–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 25 Gigabit Ethernet is introduced in Clause 105 and the purpose of each PHY sublayer is summarized in 105.3.

25GBASE-LR and 25GBASE-ER PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Further relevant information may be found in Clause 1 (terminology and conventions, references, definitions, and abbreviations) and Annex A (Bibliography, referenced as [B1], [B2], etc.).

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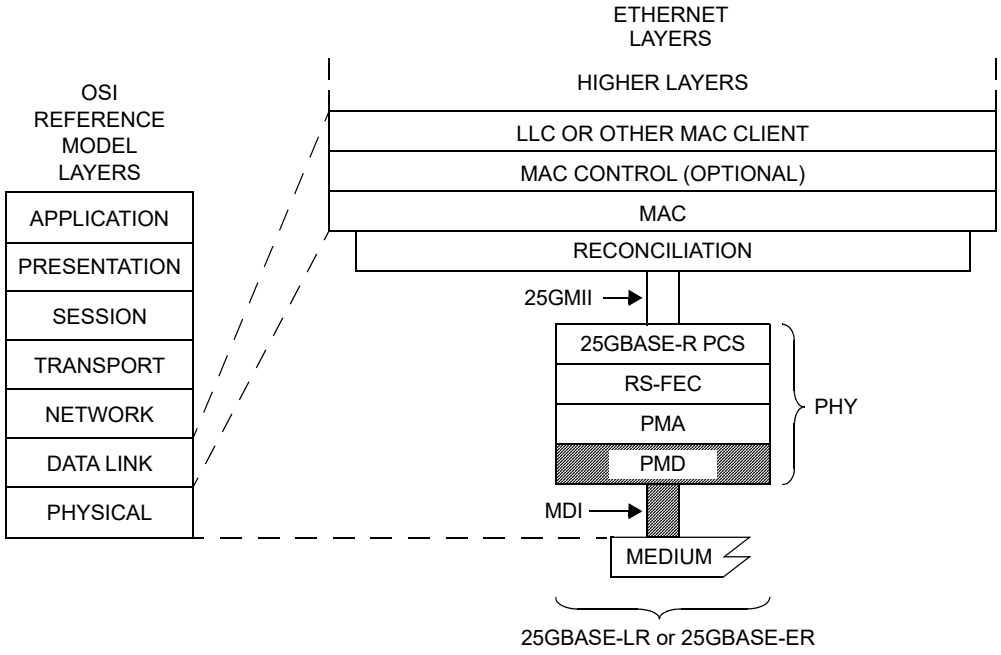

25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
LR = PMD FOR SINGLE-MODE FIBER - 10 km
ER = PMD FOR SINGLE-MODE FIBER - 40 km

Figure 114–1—25GBASE-LR and 25GBASE-ER PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

114.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 5×10^{-5} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap when processed according to Clause 108.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap when processed according to Clause 108.

114.2 Physical Medium Dependent (PMD) service interface

The PMD service interfaces for 25GBASE-LR and 25GBASE-ER are the same as PMD service interface for 25GBASE-SR as described in 112.2 with the BER as specified in 114.1.1.

114.3 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation. The sum of the transmit and receive delays at one end of the link contributed by

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the 25GBASE-LR or 25GBASE-ER PMD including 2 m of fiber in one direction shall be no more than 512 bit times (1 pause_quantum or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quantum can be found in 105.5 and its references.

114.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 114–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 114–3.

Table 114–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable

Table 114–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect

114.5 PMD functional specifications

The 25GBASE-LR and 25GBASE-ER PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

114.5.1 PMD block diagram

The PMD block diagram is shown in Figure 114–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 114.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 88.11.3). Unless specified otherwise, all receiver measurements and tests defined in 114.7 are made at TP3.

TP1 and TP4 are optional reference points that may be useful to implementers for testing components (these test points will not typically be accessible in an implemented system).

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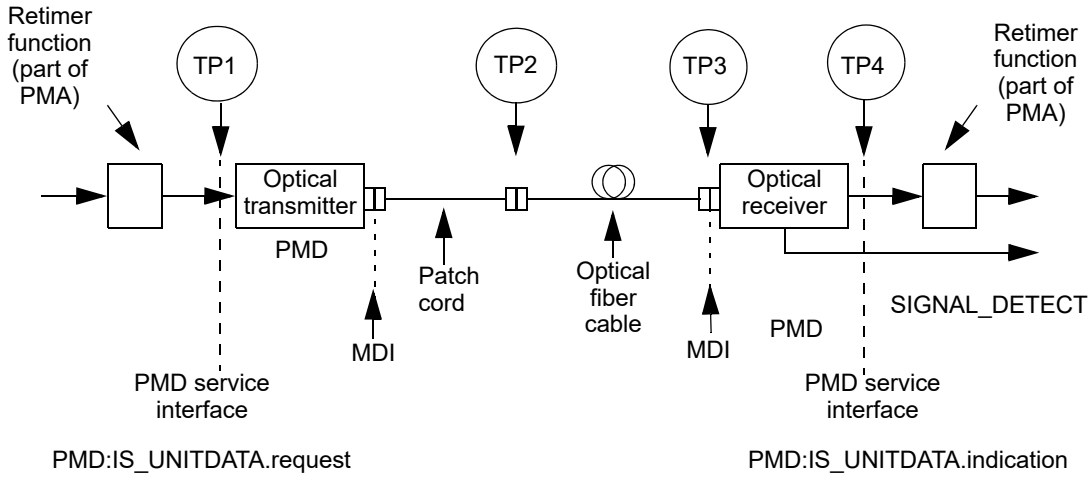

Figure 114–2—Block diagram for 25GBASE-LR and 25GBASE-ER transmit/receive paths

114.5.2 PMD transmit function

The PMD Transmit function shall convert the bit stream requested by the PMD service interface messages PMD:IS_UNITDATA.request into an optical signal. The optical signal shall then be delivered to the MDI, all according to the transmit optical specifications in this clause. The higher optical power level in the signal shall correspond to tx_bit = one.

114.5.3 PMD receive function

The PMD Receive function shall convert the optical signal received from the MDI into a bit stream for delivery to the PMD service interface using the messages PMD:IS_UNITDATA.indication, all according to the receive optical specifications in this clause. The higher optical power level in the signal shall correspond to rx_bit = one.

114.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 105.4.

SIGNAL_DETECT shall be the indicator of the presence of the optical signal. The value of the SIGNAL_-DETECT parameter shall be generated according to the conditions defined in Table 114–4. The PMD receiver is not required to verify whether a compliant 25GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT

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Table 114–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
Average optical power at TP3 ≤ –20 dBm for 25GBASE-LR and ≤ –26 dBm for 25GBASE-ER	FAIL
[(Optical power at TP3 ≥ receiver sensitivity (max) in OMA in Table 114–7) AND (compliant 25GBASE–R signal input)]	OK
All other conditions	Unspecified

parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the PMD global signal detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal. When the MDIO is implemented, the SIGNAL_DETECT value shall be continuously set in response to the magnitude of the optical signal, according to the requirements of Table 114–4.

114.5.5 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

114.5.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows the optical transmitter to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off the optical transmitter so that it meets the requirement of the average launch power of the OFF transmitter in Table 114–6.
b) If PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter.

114.5.7 PMD fault function (optional)

If the PMD has detected a local fault on the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

114.5.8 PMD transmit fault function (optional)

If the PMD has detected a local fault on the transmitter, the PMD shall set PMD_transmit_fault to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

114.5.9 PMD receive fault function (optional)

If the PMD has detected a local fault on the receiver, the PMD shall set PMD_receive_fault to one.

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If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

114.6 PMD to MDI optical specifications for 25GBASE-LR and 25GBASE-ER

The operating ranges for the 25GBASE-LR and 25GBASE-ER PMDs are defined in Table 114–5. A 25GBASE-LR or 25GBASE-ER compliant PMD operates on IEC 60793-2-50 type B1.1 (dispersion unshifted), type B1.3 (low water peak), or type B6_a (bend insensitive) single-mode fibers according to the specifications defined in Table 114–11. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 25GBASE-LR PMD operating at 12.5 km meets the operating range requirement of 2 m to 10 km). The 25GBASE-ER PMD interoperates with the 25GBASE-LR PMD provided that the channel requirements defined in 114.11 are met.

Table 114–5—25GBASE-LR and 25GBASE-ER operating ranges

PMD type	Required operating range[a]
25GBASE-LR	2 m to 10 km
25GBASE-ER	2 m to 30 km
	2 m to 40 km[b]

[a]The RS-FEC correction function may not be bypassed for any operating distance.
[b]Links longer than 30 km for the same link power budget are considered engineered links. Attenuation for such links needs to be less than the worst case specified for IEC 60793-2-50 type B1.1, type B1.3, or type B6_a single-mode fiber.

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114.6.1 25GBASE-LR and 25GBASE-ER transmitter optical specifications

The 25GBASE-LR and 25GBASE-ER transmitters shall meet the specifications in Table 114–6 per the definitions in 114.7.

Table 114–6—25GBASE-LR and 25GBASE-ER transmit characteristics

Description	25GBASE-LR	25GBASE-ER	Unit
Signaling rate (range)	25.78125 ± 100 ppm		GBd
Center wavelength (range)	1295 to 1325	1295 to 1310	nm
Side-mode suppression ratio (SMSR), (min)	30		dB
Average launch power (max)	2	6	dBm
Average launch power[a] (min)	–7	–3	dBm
Optical Modulation Amplitude (OMA), (max)	2.2	6	dBm
Optical Modulation Amplitude (OMA)[b], (min)	–4	0	dBm
Launch power in OMA minus TDP (min)	–5	–1	dBm
Transmitter and dispersion penalty (TDP), (max)	2.7	2.7	dB
Average launch power of OFF transmitter (max)	–20		dBm
Extinction ratio (min)	3	4	dB
$RIN_{20}OMA$ (max)	–130		dB/Hz
Optical return loss tolerance (max)	20		dB
Transmitter reflectance[c] (max)	–26		dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5×10^{-5} hits per sample.	{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}		

[a]Average launch power (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]Even if the TDP < 1 dB, the OMA (min) has to exceed this value.
[c]Transmitter reflectance is defined looking into the transmitter.

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114.6.2 25GBASE-LR and 25GBASE-ER receive optical specifications

The 25GBASE-LR and 25GBASE-ER receivers shall meet the specifications in Table 114–7 per the definitions in 114.7.

Table 114–7—25GBASE-LR and 25GBASE-ER receive characteristics

Description	25GBASE-LR	25GBASE-ER	Unit
Signaling rate (range)	25.78125 ± 100 ppm		GBd
Center wavelength (range)	1295 to 1325		nm
Damage threshold[a] (min)	3	–3	dBm
Average receive power (max)	2	–4	dBm
Average receive power[b] (min)	–13.3	–21	dBm
Receive power (OMA), (max)	2.2	–4	dBm
Receiver reflectance (max)	–26		dB
Receiver sensitivity (OMA)[c], (max)	–12	–19	dBm
Stressed receiver sensitivity (OMA)[d], (max)	–9.5	–16.5	dBm
Conditions of stressed receiver sensitivity test			
Stressed eye closure[e]	2.5	2.5	dB
Stressed eye J2 Jitter[e]	0.27	0.27	UI
Stressed eye J4 Jitter[e]	0.39	0.39	UI
SRS eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5×10^{-5} hits per sample.	{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}		

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
[b]Average receive power (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity (OMA), (max) is optional.
[d]Measured with conformance test signal at TP3 (see 114.7.10) for the BER specified in 114.1.1.
[e]Stressed eye closure, stressed eye J2 Jitter, and stressed eye J4 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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114.6.3 25GBASE-LR and 25GBASE-ER illustrative link power budgets

Illustrative power budgets and penalties for 25GBASE-LR and 25GBASE-ER channels are shown in Table 114–8.

Table 114–8—25GBASE-LR and 25GBASE-ER illustrative link power budgets

Parameter	25GBASE-LR	25GBASE-ER		Unit
Power budget (for maximum TDP)	9.7	20.7		dB
Operating distance	10	30	40[a]	km
Channel insertion loss	6.3[b]	15[b]	See 114.9[a]	dB
Maximum discrete reflectance	See 114.10	See 114.10		dB
Allocation for penalties[c] (for maximum TDP)	3.4	20.7 minus maximum channel insertion loss per Table 114–12		dB
Additional insertion loss allowed	0	Maximum channel insertion loss per Table 114–12 minus 15	0	dB

[a]Links longer than 30 km are considered engineered links. Attenuation for such links needs to be less than the worst case for cables containing IEC 60793-2-50 type B1.1, type B1.3, or type B6_a single-mode cabled optical fiber.
[b]The channel insertion loss is calculated using the maximum distance specified in Table 114–5 and fiber attenuation of 0.43 dB/km at 1295 nm plus an allocation for connection and splice loss given in 88.11.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

114.7 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

114.7.1 Test patterns for optical parameters

The test patterns used in this clause shall be the same as those used for 100GBASE-SR4, as described in 95.8.1 and shown in Table 95–9, with the exception that pattern 5, the scrambled idle test pattern defined in 82.2.11, is encoded by Clause 108 RS-FEC for 25GBASE-LR and 25GBASE-ER. The multi-lane testing considerations described in 95.8.1.1 do not apply. Table 114–9 shows the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined.

114.7.2 Wavelength and side mode suppression ratio (SMSR)

The wavelength and SMSR shall be within the ranges given in Table 114–6 if measured per IEC 61280-1-3. The signal is modulated using the test pattern specified in Table 114–9.

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Table 114–9—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	3, 5 or valid 25GBASE-R signal	114.7.2
Side mode suppression ratio	3, 5 or valid 25GBASE-R signal	—
Average optical power	3, 5 or valid 25GBASE-R signal	114.7.3
Optical modulation amplitude (OMA)	Square wave or 4	114.7.4
Transmitter and dispersion penalty (TDP)	3, 5 or valid 25GBASE-R signal	114.7.5
Extinction ratio	3, 5 or valid 25GBASE-R signal	114.7.6
$RIN_{20}OMA$	Square wave or 4	114.7.7
Transmitter optical waveform	3, 5 or valid 25GBASE-R signal	114.7.8
Stressed receiver sensitivity	3, 5 or valid 25GBASE-R signal	114.7.10
Calibration of OMA for receiver tests	Square wave or 4	87.8.11
Vertical eye closure penalty calibration	3, 5 or valid 25GBASE-R signal	87.8.11

114.7.3 Average optical power

The average optical power shall be within the limits given in Table 114–6 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using the test pattern specified in Table 114–9.

114.7.4 Optical Modulation Amplitude (OMA)

OMA shall be as defined in 52.9.5 for measurement with a square wave (8 ones, 8 zeros) test pattern or 68.6.2 (from the variable MeasuredOMA in 68.6.6.2) for measurement with a PRBS9 test pattern. See 114.7.1 for test pattern information.

114.7.5 Transmitter and dispersion penalty (TDP)

Transmitter and dispersion penalty (TDP) shall be as defined in 52.9.10 with the BER as specified in 114.1.1. The measurement procedure for 25GBASE-LR and 25GBASE-ER is detailed in 114.7.5.1 to 114.7.5.4.

114.7.5.1 Reference transmitter requirements

The reference transmitter is a high-quality instrument-grade device, which can be implemented by a CW laser modulated by a high-performance modulator. The basic requirements are as follows:

a) Rise/fall times of less than 12 ps at 20% to 80%.
b) The output optical eye is symmetric and passes the transmitter optical waveform test of 114.7.8.
c) In the center 20% region of the eye, the worst-case vertical eye closure penalty as defined in 87.8.11.2 is less than 0.5 dB.
d) Total Jitter less than 0.2 UI peak-to-peak.
e) RIN of less than –138 dB/Hz.

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114.7.5.2 Channel requirements

The channel requirements for testing the transmitter are described in 88.8.5.2, where the requirements for 100GBASE-LR4 apply to 25GBASE-LR and the requirements for 100GBASE-ER4 apply to 25GBASE-ER.

114.7.5.3 Reference receiver requirements

The reference receiver is required to have the bandwidth given in 114.7.8. The sensitivity of the reference receiver is limited by Gaussian noise. The receiver has minimal threshold offset, deadband, hysteresis, baseline wander, deterministic jitter, or other distortions. Decision sampling has minimal uncertainty and setup/hold times.

The nominal sensitivity of the reference receiver, S, is measured in OMA using the setup of Figure 52–12 without the test fiber and with the transversal filter removed. The sensitivity S has to be corrected for any significant reference transmitter impairments including any vertical eye closure. It is measured while sampling at the eye center or corrected for off-center sampling. It is calibrated at the wavelength of the transmitter under test.

For all transmitter and dispersion penalty measurements, determination of the center of the eye is required. Center of the eye is defined as the time halfway between the left and right sampling points within the eye where the measured BER is greater than or equal to 1×10^{-3}.

The clock recovery unit (CRU) used in the TDP measurement has a corner frequency of 10 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low-frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.

114.7.5.4 Test procedure

The test procedure is as defined in 52.9.10.4 with the BER as specified in 114.1.1.

114.7.6 Extinction ratio

The extinction ratio shall be within the limits given in Table 114–6 if measured using the methods specified in IEC 61280-2-2. The extinction ratio is measured using the test pattern defined in Table 114–9.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 114–9).

114.7.7 Relative Intensity Noise ($RIN_{20}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 20 dB.
b) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 25.8 GHz).

114.7.8 Transmitter optical waveform (transmit eye)

The required optical transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 86–4. The transmitter optical waveform of a port transmitting the test pattern specified in Table 114–9 shall meet specifications according to the methods specified in 86.8.4.6.1 with the exception that the clock recovery unit's high-frequency corner bandwidth is 10 MHz. The filter nominal reference frequency f_r is 19.34 GHz and the filter tolerances are as specified for STM-64 in ITU-T G.691. Compensation may be made for variation of the reference receiver filter response from an ideal fourth-order Bessel-Thomson response and for any excess reference receiver noise.

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114.7.9 Receiver sensitivity

Receiver sensitivity, which is defined for an ideal input signal, is optional and compliance is not required. If measured, the test signal should have negligible impairments such as intersymbol interference (ISI), rise/fall times, jitter and RIN. Instead, the normative requirement for receivers is stressed receiver sensitivity.

114.7.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 114–7 if measured using the method defined in 95.8.8 with the following exceptions:

a) The centers of the vertical histograms through the eye diagram are 0.45 UI and 0.55 UI, and the width of each histogram is 0.02 UI (see Figure 95–4).

b) Added sinusoidal jitter is as specified in Table 114–10.

c) The stressed eye J2 Jitter, stressed eye J4 Jitter, stressed eye closure, and SRS eye mask are as given in Table 114–7.

d) The test pattern is as given in Table 114–9.

e) The reference receiver used to verify the conformance test signal is required to have the bandwidth given in 114.7.8.

f) The SEC created by the selection of the appropriate bandwidth for the combination of the low-pass filter and the E/O converter with the sinusoidal jitter, sinusoidal interferer 1, sinusoidal interferer 2, and the Gaussian noise generator turned off is at least 1.5 dB.

Table 114–10—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter, peak-to-peak (UI)
$f < 100$ kHz	Not specified
100 kHz $< f \leq$ 10 MHz	5×10^5 Hz / f
10 MHz $< f <$ 10 LB[a]	0.05

[a]LB = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

g) The conditions for receiver aggressor lanes do not apply.

114.8 Safety, installation, environment, and labeling

All equipment subject to this clause shall conform to the applicable requirements of 112.8.

114.9 Fiber optic cabling model

The fiber optic cabling model for 25GBASE-LR and 25GBASE-ER is as specified for 100GBASE-LR4 and 100GBASE-ER4 in 88.10 with the exceptions that Table 88–14 is replaced by Table 114–11 and the maximum channel insertion loss for 25GBASE-ER is specified by Table 114–12.

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Table 114–11—Fiber optic cabling (channel) characteristics

Description	25GBASE-LR	25GBASE-ER		Unit
Operating distance (max)	10	30	40	km
Channel insertion loss[a, b] (max)	6.3	See Table 114–12		dB
Channel insertion loss (min)	0	10[c]		dB
Positive dispersion[b] (max)	22.6	27.6	36.8	ps/nm
Negative dispersion[b] (min)	–27.9	–83.7	–111.6	ps/nm
DGD_max[d]	8	10.3	10.3	ps
Optical return loss (min)	21	21	21	dB

[a]These channel insertion loss values include cable, connectors, and splices.
[b]Over the wavelength range 1295 nm to 1325 nm for 25GBASE-LR and 1295 nm to 1310 nm for 25GBASE-ER.
[c]Channel insertion loss (min) may be implemented with an optical attenuator.
[d]DGD_max is the maximum differential group delay that the system is required to tolerate.

Table 114–12—Maximum channel insertion loss versus number of discrete reflectances for 25GBASE-ER

Maximum channel insertion loss (dB)		Number of discrete reflectances > –55 dB and ≤ –35 dB										
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
Number of discrete reflectances > –35 dB and ≤ –26 dB	**0**	18	18	18	17.9	17.9	17.9	17.8	17.8	17.8	17.7	17.7
	1	17.9	17.9	17.9	17.8	17.8	17.7	17.7	17.6	17.6	17.5	—[a]
	2	17.8	17.8	17.7	17.7	17.6	17.6	17.5	17.4	17.4	—[a]	—[a]
	3	17.7	17.6	17.6	17.4	17.4	17.3	—[a]	—[a]	—[a]	—[a]	—[a]
	4	17.5	17.4	17.3	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]
	> 4	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]

[a]The indicated combination of reflectances is not supported.

114.10 Characteristics of the fiber optic cabling (channel)

The characteristics of the fiber optic cabling (channel) for 25GBASE-LR and 25GBASE-ER are as specified for 100GBASE-LR4 and 100GBASE-ER4 in 88.11 with the following exceptions:

— Table 88–14 is replaced by Table 114–11.

— For 25GBASE-LR, the maximum value for each discrete reflectance shall be less than or equal to the value shown in Table 114–13 corresponding to the number of discrete reflectances above –55 dB within the channel.

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— For 25GBASE-ER, the maximum value of channel insertion loss is dependent on the number and maximum value of the discrete reflectances within the channel as given in Table 114–12. Discrete reflectances below –55 dB may be ignored when determining the supported channel insertion loss.

Table 114–13—Maximum value of each discrete reflectance for 25GBASE-LR

Number of discrete reflectances above –55 dB[a]	Maximum value for each discrete reflectance for 25GBASE-LR
1 to 4	–26 dB
6	–30 dB
8	–32 dB
10	–34 dB

[a]For numbers of discrete reflectances in between two numbers shown in the table, the lower of the two corresponding maximum discrete reflectance values applies.

114.11 Requirements for interoperation between 25GBASE-LR and 25GBASE-ER

The 25GBASE-LR and 25GBASE-ER PMDs can interoperate with each other (over an engineered link) provided that the fiber optic cabling (channel) characteristics for 25GBASE-LR given in 114.9 are met, with the exception of the maximum and minimum channel insertion loss values, which are given in Table 114–14 for the two link directions separately. Attenuators may be used to achieve the required losses.

Table 114–14—Channel insertion loss requirements for interoperation

Direction	Min loss	Max loss	Unit
25GBASE-LR transmitter to 25GBASE-ER receiver	6.2	13.3	dB
25GBASE-ER transmitter to 25GBASE-LR receiver	4	10.3	dB

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114.12 Protocol implementation conformance statement (PICS) proforma for Clause 114, Physical Medium Dependent (PMD) sublayer and medium, types 25GBASE-LR and 25GBASE-ER[192]

114.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 114, Physical Medium Dependent (PMD) sublayer and medium, types 25GBASE-LR and 25GBASE-ER, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

114.12.2 Identification

114.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

114.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 114, Physical Medium Dependent (PMD) sublayer and medium, types 25GBASE-LR and 25GBASE-ER
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[192]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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114.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*LR	25GBASE-LR PMD	114.6	Device supports requirements for 25GBASE-LR PHY	O.1	Yes [ ] No [ ]
*ER	25GBASE-ER PMD	114.6	Device supports requirements for 25GBASE-ER PHY	O.1	Yes [ ] No [ ]
*INS	Installation / cable	114.9	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
CTP1	Reference point TP1 exposed and available for testing	114.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
CTP4	Reference point TP4 exposed and available for testing	114.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
CDC	Delay constraints	114.3	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO capability	114.4	Registers and interface supported	O	Yes [ ] No [ ]

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114.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, types 25GBASE-LR and 25GBASE-ER

114.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CF1	Compatible with 25GBASE-R RS-FEC, PCS, and PMA	114.1		M	Yes [ ]
CF2	Integration with management functions	114.1		O	Yes [ ] No [ ]
CF3	Bit error ratio	114.1.1	Meets the BER specified in 114.1.1	M	Yes [ ]
CF4	Transmit function	114.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
CF5	Mapping between optical signal and logical signal for transmitter	114.5.2	Higher optical power is a one	M	Yes [ ]
CF6	Receive function	114.5.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
CF7	Conversion of optical signals to electrical signals	114.5.3	For delivery to the PMD service interface	M	Yes [ ]
CF8	Mapping between optical signal and logical signal for receiver	114.5.3	Higher optical power is a one	M	Yes [ ]
CF9	Global Signal Detect function	114.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
CF10	Global Signal Detect behavior	114.5.4	SIGNAL_DETECT is an indicator of the presence of an optical signal	M	Yes [ ]
CF11	PMD reset function	114.5.5	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

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114.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
CM1	Management register set	114.4		MD:M	Yes [ ] N/A [ ]
CM2	Global transmit disable function	114.5.6	Disables the optical transmitter with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
CM3	PMD_fault function	114.5.7	Sets PMD_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
CM4	PMD_transmit_fault function	114.5.8	Sets PMD_transmit_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
CM5	PMD_receive_fault function	114.5.9	Sets PMD_receive_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]

114.12.4.3 PMD to MDI optical specifications for 25GBASE-LR

Item	Feature	Subclause	Value/Comment	Status	Support
CLR1	Transmitter meets specifications in Table 114–6	114.6.1	Per definitions in 114.7	LR:M	Yes [ ] N/A [ ]
CLR2	Receiver meets specifications in Table 114–7	114.6.2	Per definitions in 114.7	LR:M	Yes [ ] N/A [ ]

114.12.4.4 PMD to MDI optical specifications for 25GBASE-ER

Item	Feature	Subclause	Value/Comment	Status	Support
CER1	Transmitter meets specifications in Table 114–6	114.6.1	Per definitions in 114.7	ER:M	Yes [ ] N/A [ ]
CER2	Receiver meets specifications in Table 114–7	114.6.2	Per definitions in 114.7	ER:M	Yes [ ] N/A [ ]

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114.12.4.5 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Measurement cable	114.7	2 m to 5 m in length	M	Yes [ ]
COM2	Center wavelength and SMSR	114.7.2	Per IEC 61280–1–3 under modulated conditions	M	Yes [ ]
COM3	Average optical power	114.7.3	Per IEC 61280-1-1	M	Yes [ ]
COM4	OMA measurements	114.7.4		M	Yes [ ]
COM5	Transmitter and dispersion penalty	114.7.5		M	Yes [ ]
COM6	Extinction ratio	114.7.6	Per IEC 61280-2-2	M	Yes [ ]
COM7	RIN_{20}OMA measurement procedure	114.7.7		M	Yes [ ]
COM8	Transmit eye	114.7.8		M	Yes [ ]
COM9	Stressed receiver sensitivity	114.7.10		M	Yes [ ]

114.12.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CES1	General safety	112.8.1	Conforms to IEC 60950-1	M	Yes [ ]
CES2	Laser safety—IEC Hazard Level 1	112.8.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
CES3	Electromagnetic interference	112.8.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

114.12.4.7 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
COC1	Fiber optic cabling	114.10	Meets requirements specified in Table 114–11	INS:M	Yes [ ] N/A [ ]
COC2	Maximum discrete reflectance	88.11.2.2	Less than –26 dB	INS:M	Yes [ ] N/A [ ]
COC3	MDI requirements	88.11.3	Meets IEC 61753-1-1 and IEC 61753-021-2	INS:M	Yes [ ] N/A [ ]

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115. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer, types 1000BASE-RHA, 1000BASE-RHB, and 1000BASE-RHC

115.1 Overview

1000BASE-H comprises a Physical Coding Sublayer (PCS) and a Physical Medium Attachment (PMA) sublayer that supports Physical Medium Dependent (PMD) sublayers for operation at 1000 Mb/s over duplex plastic optical fiber (POF) as the transmission medium. The following three port types with different PMDs are defined: 1000BASE-RHA, 1000BASE-RHB, and 1000BASE-RHC (collectively referred to as 1000BASE-RHx).

1000BASE-RHA specifications are driven by the requirements of home and other consumer networks. Connection of the PMD to the step index plastic optical fiber (SI-POF) medium is typically not a mated connector. Rather, a bare duplex cable is attached with a clamp in the PMD receptacle.

1000BASE-RHB specifications are driven by the requirements for industrial applications. Connection of PMD to the SI-POF medium is typically with a PMD receptacle and mated plug. A harsh environment is expected (e.g., extended temperature range, dust), and the connector is typically terminated in the field to facilitate flexible equipment interconnection layout.

1000BASE-RHC specifications are driven by requirements for automotive applications. Connection of PMD to the SI-POF medium is with a PMD receptacle and mated plug. PMD and in-line connectors and the cable have to support specific requirements for installation in a vehicle: Kojiri-safe, dust protection, vibration robustness, tensile strength, etc.

115.1.1 Features

The following are the features of the 1000BASE-H set of PHYs:

a) Specified to operate with the GMII (Clause 35).
b) Full duplex operation.
c) Support for BER of 10^{-12} or better.
d) Communication side-channel for PHY management, operations, administration, and maintenance between link partners.
e) Operation in automotive, industrial, and home network environments.

115.1.2 Conventions

The notation used in the state diagrams in this clause follows the conventions in 21.5. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

115.1.3 Relationship of 1000BASE-RHx to other standards

The relationship between a 1000BASE-RHx PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model is shown in Figure 115–1. The physical layer connects one Annex 4A Media Access Control (MAC) to the medium. This clause specifies the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and Physical Medium Dependent (PMD) components of the Physical Layer device (PHY).

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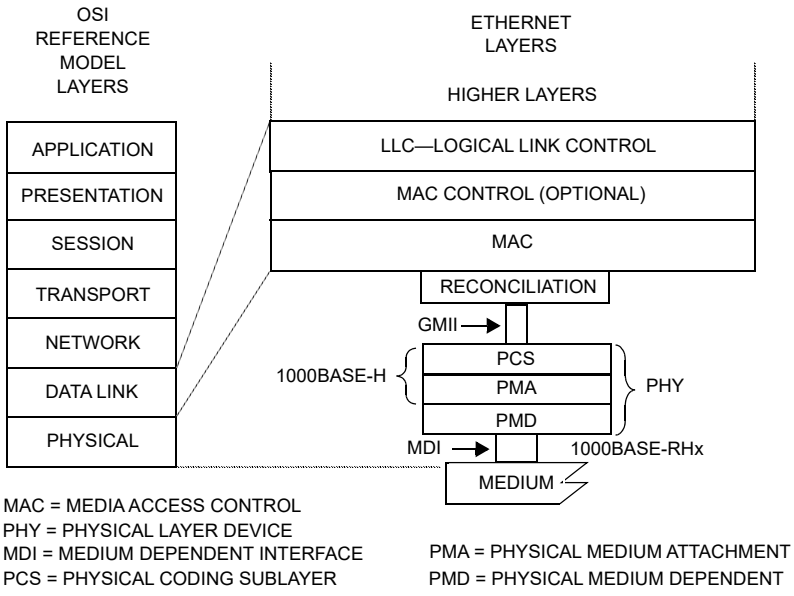

Figure 115–1—1000BASE-RHx PHY relationship to the ISO/IEC Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 Ethernet Model

115.1.4 Relationship to other Gigabit Ethernet PHY types

1000BASE-RHx PHY types are specified with the PCS interfacing to a GMII. Physical implementation of the GMII is optional. System operation from the perspective of signals at the MDI and management objects are identical whether the GMII is implemented or not. The MII Management Interface used with the initial set of Gigabit Ethernet PHYs is not used for 1000BASE-RHx PHY types.

115.1.5 Operation of 1000BASE-RHx

1000BASE-RHx PHY types support full duplex operation only, using two plastic optical fibers as the medium. Each fiber is used for unidirectional transmission with the 1000BASE-RHx port on one end of the link segment transmitting on one fiber and receiving on the second fiber. A cross-over in the cabling connects the local PMD transmitter to the link partner's PMD receiver, and the link partner's PMD transmitter to the local PMD receiver. The PMD TX and PMD RX compose the PMD sublayer.

The topology of 1000BASE-RHx is illustrated in Figure 115–2.

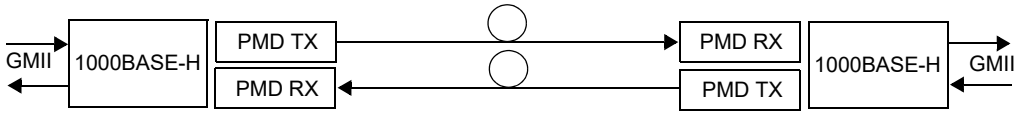

Figure 115–2—1000BASE-RHx topology

The 1000BASE-H PCS encapsulates and decapsulates the transmit and receive GMII data streams using a series of fixed length Transmit Blocks. A frame on the GMII can be contained in one or more Transmit Blocks. GMII frame boundaries have no correlation to Transmit Block boundaries.

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Transmit Blocks also include pilot signals and control information. This information keeps the receiver clock aligned with the transmitter, supports channel equalization, and provides link monitoring. These signals and control information are inserted at fixed locations within the Transmit Block interrupting the transmission of the GMII data stream also included in the Transmit Block. Encapsulation of the GMII data stream within the Transmit Block also includes forward error correction encoding in fixed-length codewords inserted at fixed locations.

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115.1.6 Functional block diagram

Figure 115–3 provides a functional block diagram of the 1000BASE-RHx PHY.

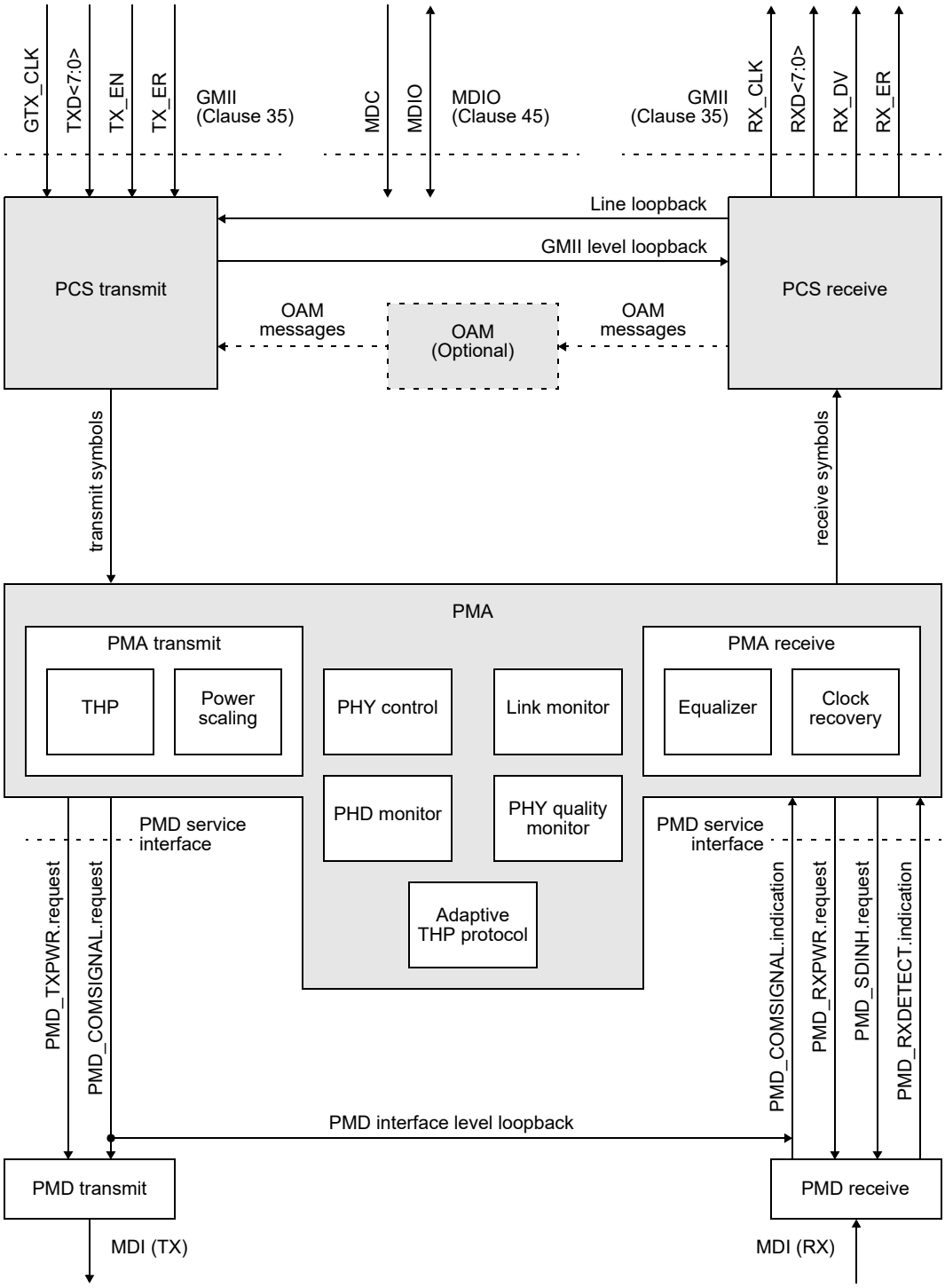

Figure 115–3—1000BASE-RHx functional block diagram

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115.2 Physical Coding Sublayer (PCS)

The 1000BASE-H PCS couples a Gigabit Media Independent Interface (GMII), see Clause 35, to the Physical Medium Attachment (PMA) sublayer.

The PCS transmit function includes several steps. The GMII transmit data stream is encapsulated and encoded into 65-bit blocks called Physical Data Blocks (PDB) and then scrambled. After that, the scrambled data is encoded and mapped using a Multi-Level Coset Code (MLCC) block-oriented encoder, which generates fixed-length codewords of PAM16 symbols. The resultant MLCC codewords are symbol-by-symbol scrambled and then time division multiplexed with control information fields using various sub-blocks to create Transmit Blocks. The control information fields in Transmit Blocks are encoded differently, but the symbol time is equal for both the PAM16 symbols carrying information from the GMII and the encoded control information fields. Symbols are transmitted at a nominal rate of 325 MBd.

The PCS receive function comprises symbol descrambling and decoding of the MLCC codewords and the control information with error correction and detection.The resultant information obtained from MLCC codewords decoding is descrambled recovering the original PDB sequence that is finally processed to extract the GMII receive data stream. The decoded control information is also provided to the PMA sublayer for control of local and remote PHYs.

115.2.1 Transmit Block

The Transmit Block is the basic structure for transmission of data and control information for 1000BASE-H. On an active link, Transmit Blocks shall be transmitted continuously to allow receivers to maintain synchronization and equalizers to maintain alignment to the channel conditions.

The Transmit Block shall consist of 1 pilot S1 sub-block (S1), 13 pilot S2 sub-blocks ($S2_0$, $S2_1$, ..., $S2_{12}$), 14 physical header subframe sub-blocks (PHS_0, PHS_1, …, PHS_{13}), and 28 payload data sub-blocks (numbered 0 through 27), which are temporally ordered as indicated in Figure 115–4. (The top part of the figure provides detail on the beginning of a Transmit Block and the bottom part of the figure the end of a Transmit Block.) The symbols composing any sub-block shall be transmitted to the PMA at the symbol rate.

The GMII data stream is encoded into the payload data sub-blocks in a stream of fixed length Transmit Blocks. Payload data sub-blocks are modified in LPI mode of operation as described in 115.4.

Each pilot S1 sub-block, pilot $S2_x$ sub-block, and PHS_x sub-block is composed of 160 symbols. For these sub-blocks the first 16 symbols (prefix) and the last 16 symbols (postfix) are zeros (see 115.3.3.1).

Each payload data sub-block is composed of 7904 symbols that span 8 MLCC codewords of 988 symbols each. The transmission of MLCC codewords are aligned with the start of the payload data sub-blocks. Since the Transmit Block includes 28 payload data sub-blocks, a total of 224 MLCC codewords (CW_0, CW_1, …, CW_{223}) are transmitted. This gives a total of 221 312 payload data symbols.

The resulting length of a Transmit Block is 225 792 symbols. Because the nominal symbol rate is 325 MBd, a Transmit Block is transmitted nominally every 694.7446 μs.

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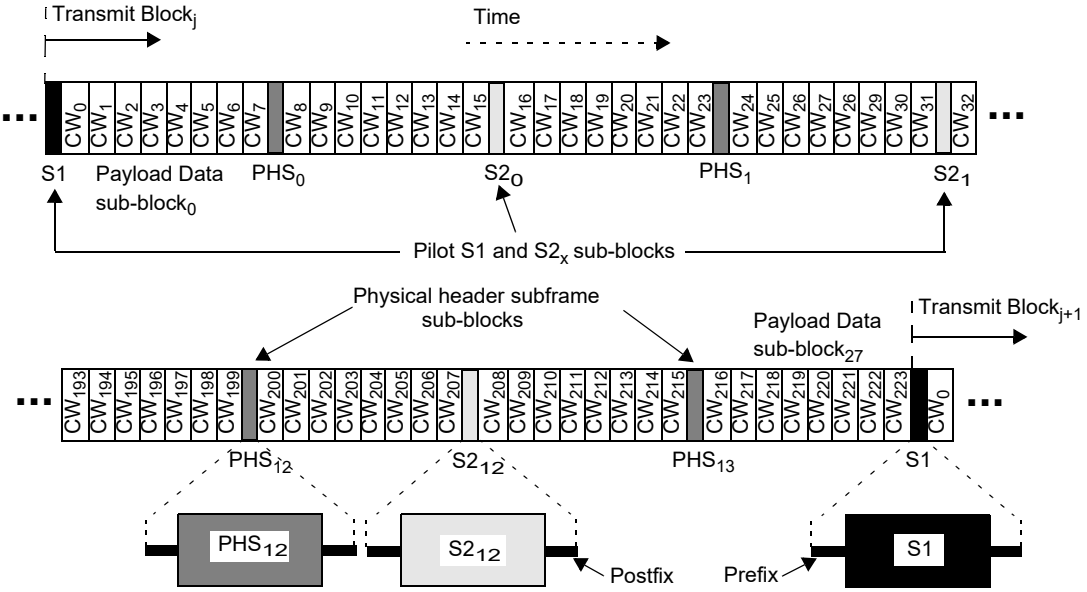

Figure 115–4—1000BASE-H Transmit Block

Transmit Blocks are generated by the multiplexer from the four data paths shown in Figure 115–5. The symbols of pilot S1, pilot $S2_x$, PHS_x, and payload data sub-blocks are generated in a different manner. Though the implementation method is not constrained, the input from each data path to the multiplexer may logically be viewed as a symbol FIFO, with the multiplexer selecting the appropriate data path symbols sequentially to create a sub-block. The sequence of sub-blocks results in the Transmit Block temporal order illustrated in Figure 115–4.

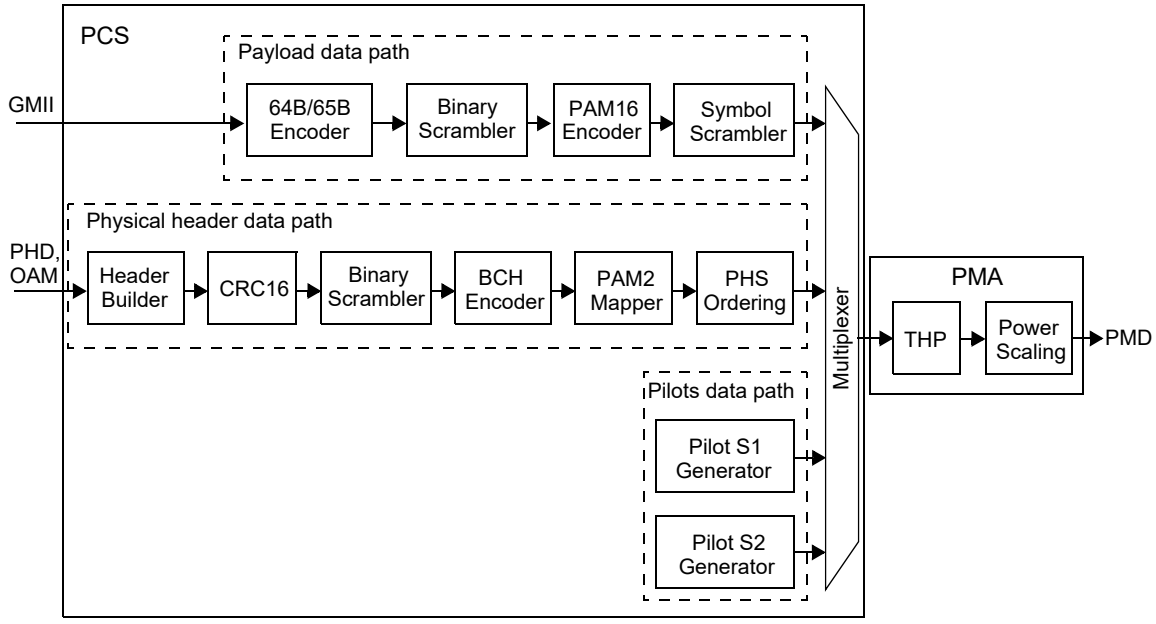

Figure 115–5—Transmit Block generation

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115.2.2 Pilots data path

Pilots S1 and S2 are predefined signals transmitted in fixed allocated time slots of the Transmit Block intended to be used by the receiver for initialization and continuous tracking purposes based on data-aided signal processing. A pilot signal S1 is transmitted at the beginning of each Transmit Block as shown in Figure 115–4 and is intended for symbol synchronization and timing recovery. Pilot S2 is divided into a series of sub-blocks ($S2_x$, x = 0 through 12) that are distributed along the Transmit Block. Pilot $S2_x$ sub-blocks are intended to facilitate timing recovery, channel estimation, and equalization by the receiver.

115.2.2.1 Pilot S1 generator

A pilot S1 sub-block is transmitted at the beginning of each Transmit Block as shown in Figure 115–4. Figure 115–6 illustrates the pilot S1 generator.

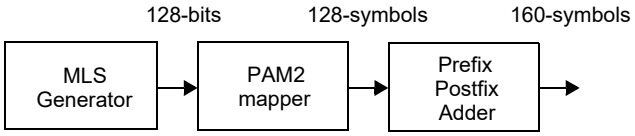

Figure 115–6—Pilot S1 generator

The S1 generator shall produce an output of one pilot S1 sub-block per Transmit Block equivalent to the following steps:

a) A maximum length sequence (MLS) generator that produces the same output as the following code is used to generate a 128-bit binary sequence.[193, 194] This code produces the same 128-bit binary sequence as the shift register shown in Figure 115–7 when the shift register is initialized for each pilot S1 sub-block generation with hexadecimal value of 0x172DB9D, where the leftmost digit of the initialization value corresponds to the initial value of register element r[0] and is taken to generate the first bit of the pilot S1.

```
function out = lfsr(len, seed)
  % Reset
  r = double(dec2bin(hex2dec(seed))) - double('0');
  r = [zeros(1, 25-length(r)) r];
  % Output generation
  for i = 1:len
    out(i) = r(1);
    r      = [mod(r(22)+r(25),2) r(1:24)];
  end
end
```

The variable *len* is the length of the sequence to be generated (*len* = 128 for S1), the variable *out* is the binary output sequence, and the variable seed is the initialization value of the shift register (*seed* = '172DB9D').

b) The bits generated in the previous step are mapped into PAM2 symbols so that bits with value 0 are mapped to {–1} and bits with value 1 are mapped to {+1}.

c) The resulting 128-symbol sequence is prefixed and postfixed by a sequence of 16 zero {0} symbols, thus obtaining the 160 symbol length for S1 sub-block.

[193]This code is written in the MATLAB programming language (see 1.3); however, use of this language does not indicate an endorsement of MATLAB by IEEE and, as such, any tool can be used to perform this calculation.

[194]*Copyright release for MATLAB code:* Users of this standard may freely reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

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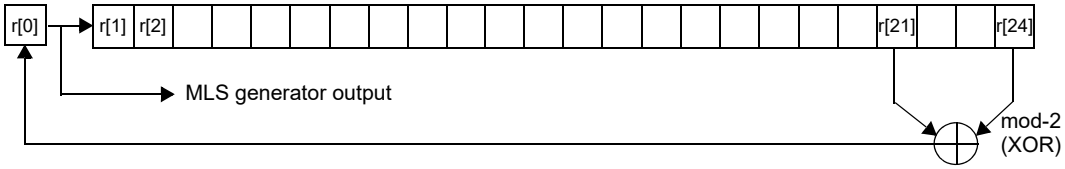

Figure 115–7—MLS generator

115.2.2.2 Pilot S2 generator

A pilot $S2_x$ sub-block is transmitted between every other payload data sub-block, alternating with PHS_x sub-blocks as shown in Figure 115–4. Figure 115–8 illustrates the pilot $S2_x$ sub-block generator.

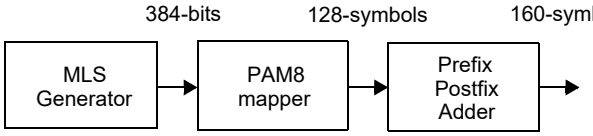

Figure 115–8—Pilot $S2_x$ sub-block generator

The S2 generator shall produce an output of 13 pilot $S2_x$ sub-blocks per Transmit Block equivalent to the following steps:

a) An MLS generator that produces the same output as the shift register shown in Figure 115–7 is used to generate 13 binary sequences of 384-bit length. The shift register is initialized for each pilot $S2_x$ sub-block generation as indicated in Table 115–1. MLS initialization and operation are as described in 115.2.2.1.

Table 115–1—Shift register initialization for $S2_x$ sub-blocks

$S2_x$ sub-block	Shift register initialization	$S2_x$ sub-block	Shift register initialization
$S2_0$	0x0945286	$S2_7$	0x050DF4E
$S2_1$	0x0F00D43	$S2_8$	0x164252F
$S2_2$	0x1AA60F3	$S2_9$	0x1E587FB
$S2_3$	0x0D89E10	$S2_{10}$	0x02CD3AD
$S2_4$	0x0DEBAC8	$S2_{11}$	0x0EE9512
$S2_5$	0x16913D1	$S2_{12}$	0x1ABFA53
$S2_6$	0x13EACDB		

b) A PAM8 mapper generates a sequence of 128 PAM8 symbols from each binary sequence generated in the previous step. The binary sequence is divided into 3-bit groups and a PAM8 symbol is

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generated from each 3-bit group according to Equation (115–1). Bit $b[0]$ is the first of each 3-bit group received from the MLS generator and S the value of the PAM8 symbol.

$$S = 2b[0] + 4b[1] + 8b[2] - 7 \quad (115–1)$$

c) Each sequence of 128 PAM8 symbols is prefixed and postfixed by a sequence of 16 zero symbols, thus obtaining the 160 symbol length for each pilot $S2_x$ sub-block.

115.2.3 Physical header encoding and scrambling

The Physical Header Data (PHD) consists of 704 bits carrying physical layer control information (see 115.3.4). The PHD is scrambled, encoded, and modulated prior to transmission as illustrated in Figure 115–9. The PHD is protected by appending a 16-bit CRC code (CRC16) for extra error detection capability after decoding. The resulting sequence of 720 bits is scrambled and encoded with a (896, 720) BCH code for error correction. The 896 coded bits are mapped to generate the resulting 1792-symbol physical header subframe (PHS), which is ordered in 14 pieces regularly distributed along the Transmit Block (PHS_0 through PHS_{13}) as indicated in Figure 115–4.

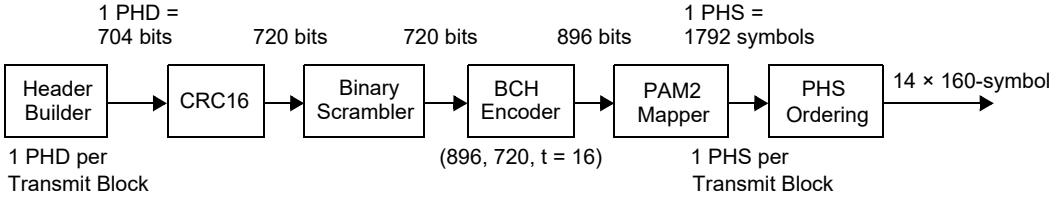

Figure 115–9—Physical header encoding and scrambling

115.2.3.1 Physical header CRC16

The 704 PHD bits from Header Builder are repeated without change and appended with 16 cyclic redundancy check bits (CRC16) for extra error detection capability after BCH decoding. The appended CRC16 shall be computed from the PHD bits and shall produce the same result as the implementation shown in Figure 115–10. The generator polynomial is $(x + 1)(x^{15} + x + 1)$. The shift register elements S_0, ..., S_{15}, shall be initialized with the value of 0x0000 for each PHD. The 704 PHD bits, in transmit bit order, are then used to compute the CRC16 with the multiplexer configured to CRCgen. After the 704 bits have been serially processed, the multiplexer is configured to CRCout and the 16 stored values are the CRC16. CRC16 is transmitted in order from S15 to S0.

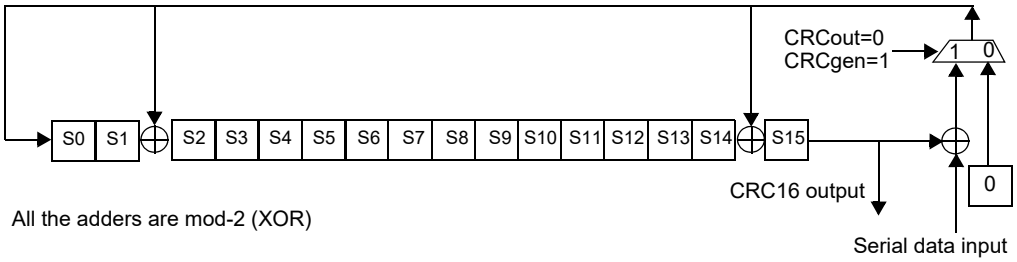

Figure 115–10—Physical header CRC16

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115.2.3.2 Physical header binary scrambler

The 720 bits from the CRC16 functional block shall be scrambled prior to transmission using a binary scrambler that produces the same result as the implementation shown in Figure 115–11. The shift register shall be initialized with the value of 0x068D332 for each Transmit Block, where the leftmost digit corresponds to the initial value of register element r[0]. The initial value of r[0] is xor-ed with the first bit from the CRC16 functional block to generate the first input bit to the BCH encoder. See 115.2.2.1 for the formal definition of the shift register.

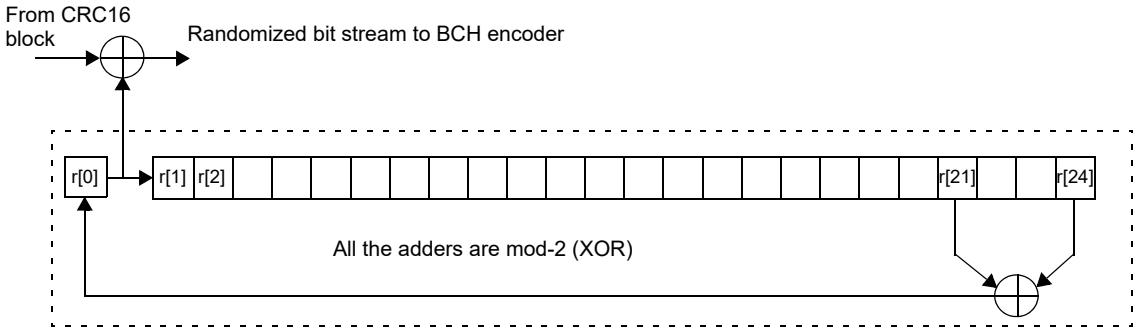

Figure 115–11—Physical header binary scrambler

115.2.3.3 Physical header BCH encoder

The scrambled 720 information bits shall be systematically encoded into 896 bits length codewords by means of a BCH (896, 720) encoder. The BCH code (896, 720) is a shortened version of the primitive BCH code (2047, 1871). It is a BCH code over Galois Field GF(2^{11}), and the error correction capability of such code is $t = 16$ bits. The number of parity bits is $p = 176$ bits. Shortening is implemented by prefixing to the 720 information bits a sequence of 1151 bits with value zero. The zero prefix sequence is not transmitted and is only used to calculate the parity from the primitive code.

The BCH code is specified by the coefficients of the generator polynomial of Equation (115–2), where $g(i)$ takes values 0 or 1.

$$G(x) = \sum_{i=0}^{p} g(i)x^i \tag{115–2}$$

The order of $G(x)$ is $p = 176$. The 177 coefficients of $G(x)$ are given by the following hexadecimal number:

0x0001 A3E8 171D BCA4 EE1E 7CDC A7DA FB8D 8F39 8072 8516 6007

with $g(0)$ being the rightmost bit.

The parity calculation shall produce the same result as the shift register implementation shown in Figure 115–19. The delay elements $s_0, s_1, \ldots, s_{p-1}$ in Figure 115–19 shall be initialized to zero before encoding. See 115.2.4.3.2 for detailed BCH encoder operation.

115.2.3.4 Physical header modulation

The 896 bits from the BCH encoder shall be mapped into 1792 PAM2 symbols so that bits with value 0 are mapped to 2 consecutive symbols {+1, –1}, and bits with value 1 are mapped to 2 consecutive symbols {–1, +1}.

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115.2.3.5 Physical header ordering

The 1792-symbol PHS sequence shall be divided for transmission into 14 pieces of 128 symbols each, regularly distributed along the Transmit Block (PHS_0 through PHS_{13}) as indicated in Figure 115–4, preserving the symbol ordering. Each piece shall be prefixed and postfixed by zero valued symbol sequences of 16 symbols length, thus obtaining the 160 symbol length of each PHS_x.

115.2.4 Payload data encoding and scrambling

The incoming data from the GMII are encapsulated and encoded into 65-bit blocks (64B/65B encoder in Figure 115–12) for transmission. The 64B/65B generates 705 600 bits per Transmit Block that are scrambled. The scrambled binary sequence is then encoded for forward error correction by a block oriented MLCC encoder that generates a 988-symbol codeword per 3150 input information bits. A total number of 224 MLCC codewords (CW_0, CW_1, …, CW_{223}) are transmitted per Transmit Block grouped in 28 payload data sub-blocks each spanning 8 MLCC codewords as specified in 115.2.1. Each payload data sub-block is composed of 8 × 988 = 7904 PAM16 symbols. The 7904 × 28 = 221 312 PAM16 symbols of a Transmit Block are symbol-by-symbol scrambled before being transmitted to the PMA sublayer.

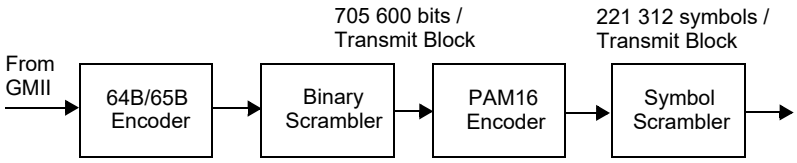

Figure 115–12—Payload data encoding and scrambling

115.2.4.1 GMII data stream encoding

The 64B/65B encoder generates a stream of 65-bit PDBs, which are serially transmitted to the binary scrambler. The nominal bit-rate of the output of the 64B/65B encoder is (65/64) × 1000 = 1015.625 Mb/s.

115.2.4.1.1 64B/65B encoding

The GMII detailed in Clause 35 supports the 1000 Mb/s operation of 1000BASE-H. It includes 8-bit transmit and receive data paths (i.e., TXD<7:0> and RXD<7:0>). Two additional signals in each direction (i.e., TX_EN, TX_ER and RX_DV, RX_ER) are used in conjunction with the data paths to delimit Ethernet packets, indicate errors, and convey other control information. The eight data and two control signals are specified relative to and sampled by a clock (GTX_CLK and RX_CLK for transmit and receive respectively).

In the transmit direction, eight consecutive GMII transfers (a GMII Chunk) are combined and then prepended by a control bit (Type) to create the PDB. TXD <7:0>, TX_EN, and TX_ER compose each GMII transfer. Two different types of PDBs, PDB.DATA and PDB.CTRL, are encoded from the set of GMII transfers defined in Table 115–2. The GMII transfers shown in Table 115–2 are the subset of permissible GMII encodings of Table 35–1 used for full duplex operation.

If the GMII Chunk only contains eight normal data transmission transfers, a PDB.DATA is generated. If the GMII Chunk contains at least one of the other three GMII control transfers shown in Table 115–2, a PDB.CTRL is generated. Both PDB.DATA and PDB.CTRL are composed of a Type bit followed by eight octets.

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Table 115–2—Supported TX GMII encodings

TX_EN	TX_ER	TXD<7:0>	CTRL<1:0>	Description
1	0	00 through FF	—	Normal data transmission
0	0	00 through FF	01	Control: normal inter-frame (idle)
0	1	01	10	Control: assert low power idle (LPI)
1	1	00 through FF	00	Control: transmit error propagation

The format of a PDB.DATA is shown in Figure 115–13. It consists of 65 bits, the first bit being the Type bit (with a value of 0) followed by eight consecutive GMII data transfers (normal data transmission as shown in Table 115–2). The eight data octets are transmitted in the same order as they were received from the GMII. Bits in an octet are transmitted from least to most significant bit.

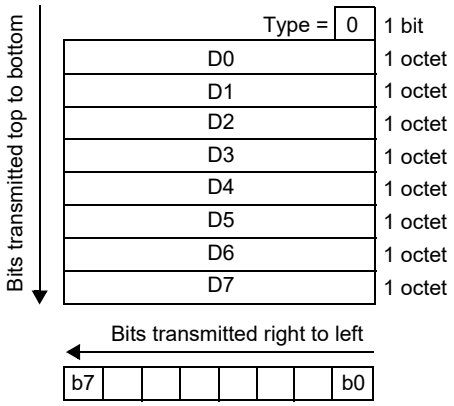

Figure 115–13—PDB.DATA format

The format of a PDB.CTRL is shown in Figure 115–14. It consists of 65 bits, encoding 8 GMII transfers [(LEN + 1) GMII control transfers and (7 – LEN) GMII data transfers, where LEN ranges from 0 through 7] preceded by the Type bit that is set to 1. The Type bit is transmitted first, followed by the 8 data and control octets generated by the encoding method described next. Bits in an octet are transmitted from least to most significant bit.

The processing of a GMII Chunk is as follows. Data octets (normal data transmission in Table 115–2) retain the value of TXD<7:0> in the GMII transfer, but every GMII control transfer is encoded in a control 8-bit byte (CB) with the following contents:

— CTRL<1:0> (CB<7:6>): This field encodes the content of the GMII control transfer as specified in Table 115–2.
— OFS<2:0> (CB<5:3>): This field indicates the offset (in GMII transfers) from the beginning of the GMII Chunk to the location of the first GMII control transfer in the GMII Chunk. This field has the same value for all CBs contained in the PDB.CTRL. The OFS value range is 0 through 7.
— LEN<2:0> (CB<2:0>): This field is the count of GMII control transfers in the GMII Chunk minus 1. This field takes the same value for all CBs contained in the PDB.CTRL. The LEN value range is 0 through 7.

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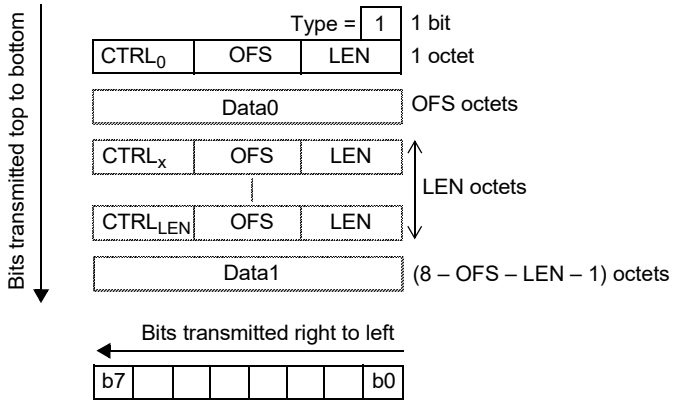

Figure 115–14—PDB.CTRL format

The octets within the PDB.CTRL are reordered as follows:

a) The CB built from the first GMII control transfer is transmitted as the first in PDB.CTRL. (This CB might encode the first GMII transfer of the GMII Chunk, or the CB might correspond to another GMII transfer of the GMII Chunk.)

b) The other seven PDB.CTRL octets are transmitted in order [not including the first CB if it was moved per step a)].

Each dotted box in Figure 115–14 represents a sequence of octets. The number of octets in a dotted box may be zero. Data0 contains OFS octets. If OFS is zero, Data0 is null. The number of CBs shown below Data0 is specified by LEN. If LEN is zero, no CB is located between Data0 and Data1. Data1 similarly may or may not be null depending on the portion of the GMII Chunk captured. Data1 completes the 8 octets included in a PDB.CTRL. It is null if 8 total octets preceded it.

NOTE—Some common example sequences of GMII transfers that illustrate the PDB.CTRL encoding include the following:

1) A GMII Chunk that only captures IPG, PDB.CTRL only includes CBs, and not Data0 or Data1.

2) A GMII Chunk that captures the end of a packet and beginning of IPG results in the first IPG GMII control transfer converted to a CB being moved ahead of the end of the packet data that is transmitted in Data0. If any more IPG GMII control transfers were captured in the GMII Chunk, they are located in the dotted boxes with control fields $CTRL_x$ through $CTRL_{LEN}$. Data1 is null.

3) A GMII Chunk that captures the end of IPG and beginning of a packet does not move any CB during encoding. The IPG is encoded in the first CB, Data0 is null and the CBs with control fields labeled $CTRL_x$ through $CTRL_{LEN}$ hold the remaining CBs encoding the IPG. The beginning of packet then appears in Data1.

4) A GMII Chunk that captures the end of a packet, shortened IPG (six or less IPG transfers), and beginning of a packet. The first IPG GMII transfer is encoded as a CB and moved ahead similar to example 2, and would have the end of packet GMII data transfer(s) in Data0, Other IPG GMII transfers are encoded as CBs in $CTRL_x$ through $CTRL_{LEN}$ and the beginning of the next packet data in Data1.

Because the minimum length of an Ethernet packet is longer than 7 octets, all the GMII control transfers in a GMII Chunk of a correct packet are contiguous. Consequently, all the CBs beyond the first are also contiguous within the PDB.CTRL.

When there are non-contiguous GMII control transfers within a GMII Chunk, the GMII data transfers between the GMII control transfers belong to an erroneous Ethernet packet. In this case, these GMII data

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transfers are replaced by GMII control transfers encoding error propagation as a previous step to the PDB.CTRL encoding. The resulting GMII Chunk is then encoded following the previous description.

A minimum delay of 8 GTX_CLK cycles at the GMII is necessary for the 64B/65B encoding, because the 64B/65B encoder requires the reception of a full GMII Chunk to start generating the first bit of the corresponding PDB.

The formal definition of the 64B/65B encoding is in 115.2.4.1.2.

115.2.4.1.2 64B/65B encoding formal definition

The 64B/65B encoder shall produce the same result as the following code.[195, 196]

```
% Variables definition
GMII.TX_ER    % GMII TX_ER signal, 1xL row vector
GMII.TX_EN    % GMII TX_EN signal, 1xL row vector
GMII.TXD      % GMII TXD bus, 1xL row vector
PCS_ENC_EN    % tx_gmii_enable (see 115.3.5.1) value for each GMII transfer,
              % 1xL vector
PDB.TYPE      % PDB type field, 1x(L/8) row vector
PDB.PAYLOAD   % PDB payload field, 8x(L/8) matrix

% 64B/65B encoding procedure
GMII.TX_EN = GMII.TX_EN & PCS_ENC_EN;
GMII.TX_ER = GMII.TX_ER & PCS_ENC_EN;

for i = 0:8:length(GMII.TXD)-1,
  TC = (GMII.TX_EN(i+1:i+8)*2 + GMII.TX_ER(i+1:i+8)) ~= 2;

  if any(TC)
    % There are at least one control byte in the 8-bytes GMII Chunk
    % The PDB is a PDB.CTRL
    PDB.TYPE(i/8 + 1) = 1;

    if any(~TC(min(find(TC)):max(find(TC))))
      % The control bytes are not contiguous in the GMII Chunk.
      % Replace data bytes that lie within control bytes with error code.
      LL=i+min(find(TC));
      UL=i+max(find(TC));
      GMII.TX_ER(LL:UL) = GMII.TX_EN(LL:UL)|GMII.TX_ER(LL:UL);

      TC(min(find(TC)):max(find(TC))) = 1;
    end

    % Valid GMII Chunk
    % OFS field computation
    OFS = min(find(TC)) - 1

    % LEN field computation
    LEN = sum(TC) - 1

    % Build the PDB.CTRL payload
    for j = 1:8,
      if TC(j)
        if ~GMII.TX_EN(i+j) & ~GMII.TX_ER(i+j)
          % Normal inter-frame
          CTRL = 1;
        elseif ~GMII.TX_EN(i+j) & GMII.TX_ER(i+j) & (GMII.TXD(i+j) == 1)
          % Assert LPI
          CTRL = 2;
        elseif GMII.TX_EN(i+j) & GMII.TX_ER(i+j)
```

[195]This code is written in the MATLAB programming language (see 1.3); however, use of this language does not indicate an endorsement of MATLAB by IEEE and, as such, any tool can be used to perform this calculation.

[196]*Copyright release for MATLAB code:* Users of this standard may freely copy or reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

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```
          % Transmit error propagation
          CTRL = 0;
        else
          % Otherwise, default case (normal inter-frame)
          CTRL = 1
        end

        B(j) = LEN + OFS*2^3 + CTRL*2^6;
      else
        B(j) = GMII.TXD(i+j);
      end
    end

    % Shift the first control byte
    PDB.PAYLOAD(1,     i/8 + 1) = B(OFS + 1);
    PDB.PAYLOAD(2:end, i/8 + 1) = [B(1:OFS) B(OFS+2:end)].';

  else
    % Pure normal data transmission bytes in the GMII Chunk
    % The PDB is a PDB.DATA
    PDB.TYPE(i/8 + 1)       = 0;
    PDB.PAYLOAD(:, i/8 + 1) = GMII.TXD(i+1:i+8).';
  end
end
```

115.2.4.1.3 PDB alignment with Transmit Block

Since the number of information bits in a Transmit Block (705 600 bits) is not a multiple of the PDB length, in general PDBs are not aligned to the start of a Transmit Block. The PHY transmitter shall encode the number of bits between the first payload bit of Transmit Block j+1 and the start of the first PDB encoded in Transmit Block j+1 in the field PHD.TX.NEXT.PDB.OFFSET of the PHD of Transmit Block j. With this control information the receiver is able to align the PCS decoder for the Transmit Block j+1 once the PHD_j (part of Transmit Block j) is fully received and decoded. This is illustrated in Figure 115–15.

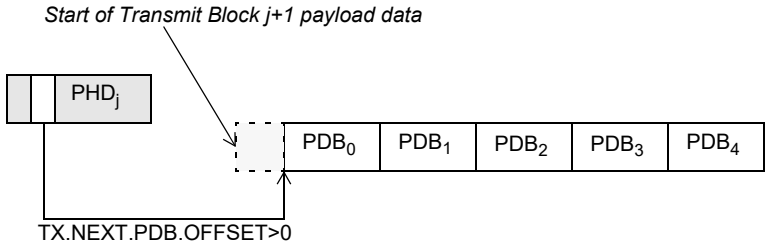

Figure 115–15—PDB alignment

The offset to the start of the first PDB in Transmit Block j+1, $\Delta(j+1)$ is calculated from the offset of the Transmit Block j, $\Delta(j)$ by using the Equation (115–3).

$$\Delta(j+1) = \mathrm{mod}(40 + \Delta(j), 65) \tag{115–3}$$

Modulo operator is defined per Equation (115–4), where floor(a) denotes the greatest integer less than or equal to the real number a.

$$\mathrm{mod}(y, x) = y - x \times \mathrm{floor}\left(\frac{y}{x}\right) \tag{115–4}$$

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115.2.4.2 Payload data binary scrambler

The 705 600 bits per Transmit Block from the 64B/65B encoder shall be scrambled prior to transmission using a binary scrambler that produces the same result as the implementation shown in Figure 115–16. The shift register shall be initialized with a hexadecimal value of 0x17C9C58 for each Transmit Block, where the leftmost digit corresponds to the initial value of register element r[0]. The initial value of r[0] is xor-ed with the first bit from the 64B/65B encoder to generate the first bit of the binary sequence that feeds the PAM16 encoder. See 115.2.2.1 for the formal definition of the shift register.

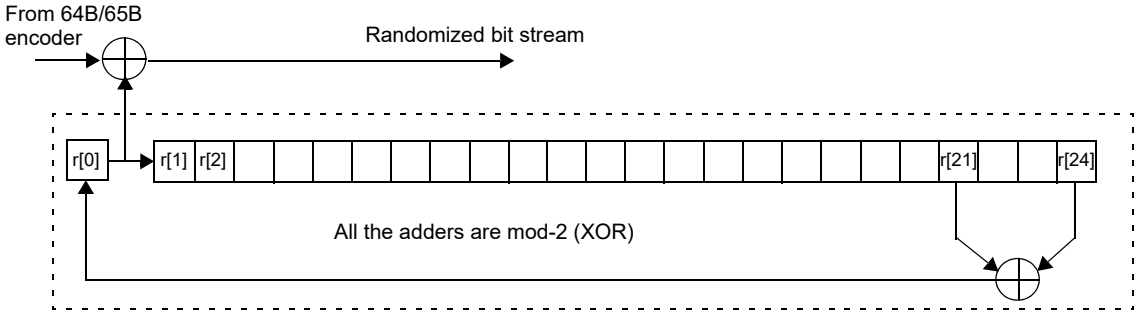

Figure 115–16—Payload data binary scrambler

115.2.4.3 PAM16 encoder

After being encapsulated and scrambled, the GMII data stream is encoded into PAM16 symbols. A two-level, block-oriented MLCC based on two-dimensional constellations is used to transmit the information with high spectral efficiency. The information is partitioned in such a way that the bits more likely to be corrupted by noise are protected by a binary BCH code, and those bits less likely to be corrupted are not additionally protected.

Figure 115–17 shows the essential parts of the MLCC encoder. A block of 3150-bit per codeword is split between the two levels that compose the encoder in an interleaved manner. The bits in the first level are encoded with a (1976, 1668) BCH code and the second level is not encoded. Bits composing the BCH codeword in the first level are mapped onto symbols of a QAM16 constellation. Bits in the second level are mapped onto symbols of a rotated QAM8 constellation. After the mapping, the two levels produce 494 2D symbols per codeword. Symbols from each level are processed by a first lattice transformation and then added to carry out the coset partitioning. The output of the adder is further processed by a second lattice transformation that produces symbols onto a rotated QAM128 constellation. Finally, in-phase and quadrature components of QAM128 symbols are multiplexed in time to generate 988 PAM16 symbols per codeword.

115.2.4.3.1 MLCC demultiplexer

The 3150 information bits to be encoded in an MLCC codeword shall be demultiplexed in two flows, where the bits $7 \times k + j$, for all k from 0 through 416 and all j from 0 through 3, are transferred to the BCH encoder of the first MLCC level, and the bits $7 \times k + j$, for all k from 0 through 416 and all j from 4 through 6, and the bits from 2919 through 3149 are transferred to the second MLCC level, preserving the relative bit ordering in each flow.

Figure 115–18 illustrates the operation of the MLCC demultiplexer. In Figure 115–18, bit quadruples a_i with i from 0 through 416 and bit triples b_i with i from 0 through 493 are the portions of information transferred to the first and to the second MLCC level, respectively. The term “4b” stands for 4-bit groups, and the term “3b” stands for 3-bit groups.

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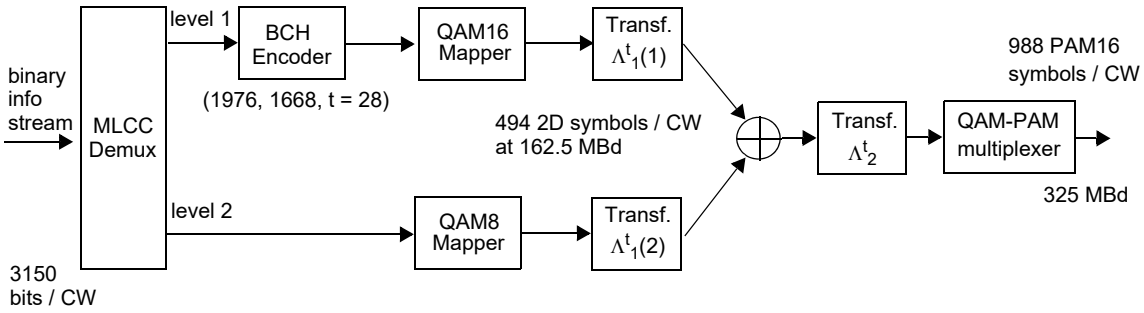

Figure 115–17—Two level coset encoder

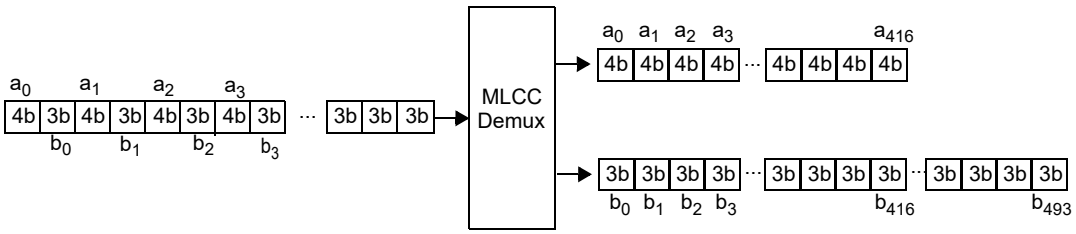

Figure 115–18—MLCC demultiplexing process

115.2.4.3.2 Payload BCH encoder

The 1668 information bits of the first level shall be systematically encoded into 1976 code bits by means of a BCH $(n, k) = (1976, 1668)$ encoder. This BCH code is a shortened version of the primitive BCH code (2047, 1739). It is a BCH code over Galois field GF(2^{11}), and the error correction capability of such code is $t = 28$. The number of parity bits is $p = 308$ bits. Shortening is implemented by prefixing to the 1668 information bits a sequence of 71 bits with value zero. The zero prefix sequence is not transmitted and is only used to calculate the parity from the primitive code.

The BCH code is specified by the coefficients of generator polynomial $G(x)$ of Equation (115–5), where $g(i)$ takes values 0 or 1. The order of $G(x)$ is $p = 308$.

$$G(x) = \sum_{i=0}^{p} g(i)x^i \tag{115–5}$$

The 309 coefficients of $G(x)$ are given by the following hexadecimal number:

0x0014 B624 90DF 0781 4D88 99E9 B9DB 6267 00D3 7A90
49DB C0C4 484A D6C5 49AB AE7E 6F58 A406 CF86 C0BD,

with $g(0)$ being the rightmost bit of the second line.

The parity calculation shall produce the same result as the shift register implementation shown in Figure 115–19. The delay elements $s_0, s_1, \ldots, s_{p-1}$ shall be initialized to zero before encoding. All the k bits

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composing the information message are used to calculate the parity and enter the BCH encoder in the same order provided by the MLCC demultiplexer with the multiplexers indicated in Figure 115–19 connected with BCHgen selected. After all the k bits have been serially processed, the multiplexers are configured to select BCHout and the p stored values $s_0, s_1, \ldots, s_{p-1}$ are the parity bits. The parity bits are then transmitted in order from s_{p-1} to s_0.

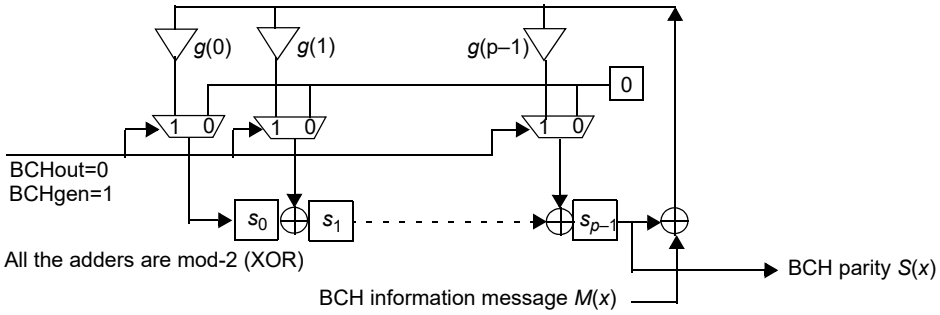

Figure 115–19—BCH encoder

The parity bits are transmitted after the information message $M(x) = m_0 + m_1x + m_2x^2 + \ldots + m_{k-1}x^{k-1}$, where m_{k-1} is the first bit of the message. To encode the message, $M(x)$ is first multiplied by x^{n-k} and the result is then divided by the generator polynomial $G(x)$. The remainder of the division of $M(x)x^{n-k}$ by $G(x)$ defines the parity $S(x) = s_0 + s_1x + s_2x^2 + \ldots + s_{p-1}x^{p-1}$, where $p = n - k$. The transmitted codeword $C(x)$ is formed by combining $M(x)$ and $S(x)$ per Equation (115–6),

$$C(x) = S(x) + M(x)x^{n-k} = s_0 + s_1x + s_2x^2 + \ldots + s_{n-k-1}x^{n-k-1} + m_0x^{n-k} + \ldots + m_{k-1}x^{n-1} \quad (115\text{–}6)$$

which shows that the codeword is produced in the required systematic form.

115.2.4.3.3 QAM16 mapper

Codewords resulting from the BCH encoding shall be mapped by means of a QAM16 mapper (see Figure 115–17) that generates 494 QAM16 symbols per 1976 bits of the MLCC codeword, doing 4-bit groups that are then mapped per Table 115–3. Bit $b[0]$ is the first received bit of each 4-bit group and S_I and S_Q are the in-phase (I) component and the quadrature (Q) component, respectively, of the QAM16 two-dimensional constellation.

Table 115–3—4B mapping to QAM16

$b[3]$	$b[2]$	$b[1]$	$b[0]$	S_I	S_Q	$b[3]$	$b[2]$	$b[1]$	$b[0]$	S_I	S_Q
0	0	0	0	–3	–3	1	0	0	0	–3	+3
0	0	0	1	–1	–3	1	0	0	1	–1	+3
0	0	1	0	–3	–1	1	0	1	0	–3	+1
0	0	1	1	–1	–1	1	0	1	1	–1	+1
0	1	0	0	+3	–3	1	1	0	0	+3	+3
0	1	0	1	+1	–3	1	1	0	1	+1	+3

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Table 115–3—4B mapping to QAM16 *(continued)*

$b[3]$	$b[2]$	$b[1]$	$b[0]$	S_I	S_Q	$b[3]$	$b[2]$	$b[1]$	$b[0]$	S_I	S_Q
0	1	1	0	+3	–1	1	1	1	0	+3	+1
0	1	1	1	+1	–1	1	1	1	1	+1	+1

115.2.4.3.4 QAM8 mapper

The uncoded bit stream from the MLCC demultiplexer shall be mapped by means of a QAM8 mapper (as illustrated in Figure 115–17) that generates 494 QAM8 symbols per 1482 bits of the MLCC codeword, doing 3-bit groups that are then mapped per Table 115–4. Bit $b[0]$ is the bit of each 3-bit group received first in time and S_I and S_Q are the in-phase (I) component and the quadrature (Q) component, respectively, of the QAM8 two-dimensional constellation.

Table 115–4—3B mapping to QAM8

$b[2]$	$b[1]$	$b[0]$	S_I	S_Q	$b[2]$	$b[1]$	$b[0]$	S_I	S_Q
0	0	0	–3	–3	1	0	0	+3	–1
0	0	1	–1	–1	1	0	1	+1	–3
0	1	0	–3	+1	1	1	0	+3	+3
0	1	1	–1	+3	1	1	1	+1	+1

115.2.4.3.5 First lattice transformation

The QAM16 symbols given by the S_I and S_Q components shall be further processed by a symbol-by-symbol lattice transformation ($\Lambda_1^t(1)$ in Figure 115–17) according to Equation (115–7) and Equation (115–8). The label $t11$ indicates the result of the lattice transformation $\Lambda_1^t(1)$.

$$S_I^{t11} = \frac{1}{2}(3 + S_I) \tag{115–7}$$

$$S_Q^{t11} = \frac{1}{2}(3 + S_Q) \tag{115–8}$$

The QAM8 symbols given by the S_I and S_Q components shall be further processed by a symbol-by-symbol lattice transformation ($\Lambda_1^t(2)$in Figure 115–17) according to Equation (115–9) and Equation (115–10). The label $t12$ indicates the result of the lattice transformation $\Lambda_1^t(2)$.

$$S_I^{t12} = S_I - S_Q \tag{115–9}$$

$$S_Q^{t12} = 6 + S_I + S_Q \tag{115–10}$$

115.2.4.3.6 Lattice addition

The symbols from the first lattice transformation of the first and second levels shall be added symbol-by-symbol according to Equation (115–11) and Equation (115–12). The resulting in-phase and quadrature

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components of the lattice addition are hereafter labeled as S_I^a and S_Q^a respectively. The label *a* indicates the result of the lattice addition.

$$S_I^a = S_I^{t11} + S_I^{t12} \tag{115–11}$$

$$S_Q^a = S_Q^{t11} + S_Q^{t12} \tag{115–12}$$

115.2.4.3.7 Second lattice transformation

The symbols from lattice addition shall be further processed by a symbol-by-symbol lattice transformation (Λ_2^t in Figure 115–17) according to Equation (115–13) and Equation (115–14). The output symbols that result of the second lattice transformation belong to a rotated QAM128 constellation. The label *t*2 indicates the result of the lattice transformation Λ_2^t.

$$S_I^{t2} = 2\text{mod}(S_I^a + S_Q^a, 16) - 15 \tag{115–13}$$

$$S_Q^{t2} = 2\text{mod}(-S_I^a + S_Q^a, 16) - 15 \tag{115–14}$$

Modulo operator is per definition of Equation (115–4).

115.2.4.3.8 QAM to PAM multiplexer

The QAM to PAM multiplexer shall generate 988 PAM16 symbols from 494 QAM128 symbols produced by the second lattice transformation per MLCC codeword, alternating the in-phase (*I*) component and the quadrature (*Q*) component, S_I^{t2} and S_Q^{t2}, respectively, of QAM128 symbols, starting the codeword with the *I* component of the first QAM symbol and ending the codeword with the *Q* component of the last QAM symbol. The PAM16 symbols generated in this way belong to the set {–15, –13, …, +13, +15}.

115.2.4.4 Payload data symbol scrambler

The 221 312 PAM16 symbols per Transmit Block from the PAM16 encoder block of Figure 115–12 shall be scrambled prior to transfer to the PMA transmit function using a scrambler implementation that produces the same output as the following steps:

a) An MLS generator that produces the same output as the shift register shown in Figure 115–7 is used to generate a 1 991 808-bit binary sequence per Transmit Block. The shift register is initialized for each Transmit Block with hexadecimal value of 0x155D559. MLS initialization and operation are as described in 115.2.2.1.

b) A mapper generates two 221 312-symbol sequences, *v* and *s*, per each binary sequence generated in the previous step, doing 9-bit groups that are then mapped so that 1 symbol of *v* and 1 symbol of *s* are generated per 9-bit group according to Equation (115–15) and Equation (115–16). Bits *b*[0] and *b*[8] are the bits of each 9-bit group received first and last in time, respectively, from the MLS generator.

$$v = -16 + 2\sum_{i=0}^{3} b[i]2^i \tag{115–15}$$

$$s = -1 + 2b[8] \tag{115–16}$$

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c) The sequences *v* and *s*, generated in the previous step, are combined symbol-by-symbol basis with the payload symbols from PAM16 encoder, *x*, to generate a 221 312-symbol scrambled sequence, *y*, according to Equation (115–17) and Equation (115–18). Modulo operator is per definition of Equation (115–4).

$$u = v + s \times x \tag{115–17}$$

$$y = \mathrm{mod}(u + 16, 32) - 16 \tag{115–18}$$

Figure 115–20 illustrates the payload data symbol scrambling process.

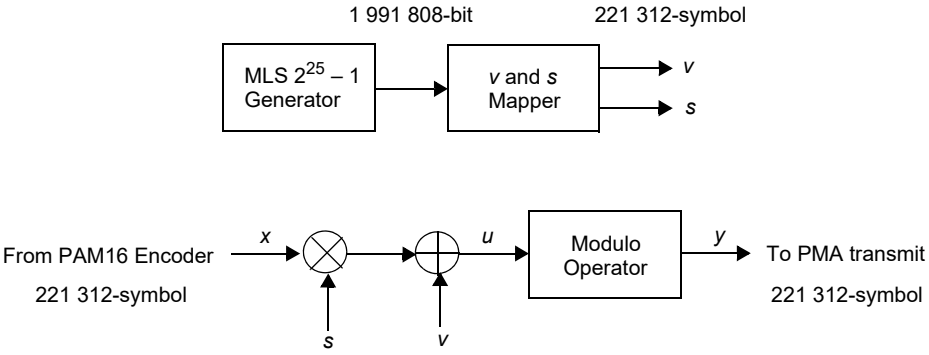

Figure 115–20—Payload data symbol scrambler

115.2.5 PCS receive function

The PCS receive function accepts equalized symbols provided by the PMA receive function. The PCS receive function knows to which part of the received Transmit Block the symbols belong, based on the symbol time alignment information provided by the clock recovery function of the PMA receive function (see 115.3.2 and 115.3.5.3). The PCS receive function shall carry out the PHD decoding, the PAM16 decoding of payload sub-blocks, and the 64B/65B decoding of payload data.

The PHD decoding comprises detection and demapping of the received PAM2 symbols, BCH decoding for error correction, binary data descrambling, and CRC16 checking for each received PHD. Only when the CRC16 computation indicates that the received PHD is correct shall the contents of the different PHD fields be available to the PMA state diagrams and to the other PCS receive functions that use this information.

The received PAM16 symbols belonging to the payload data sub-blocks are first symbol-descrambled, and the resulting symbols are MLCC decoded, with error correction and error detection. If during MLCC decoding it is detected that a codeword contains errors that could not be corrected, the resulting bits belonging to that codeword shall be marked as corrupt. The bit stream is then binary descrambled.

Using the PHD.NEXT.PDB.OFFSET field of the decoded PHD (see 115.2.4.1.3, Figure 115–15) carried in the previous Transmit Block, the PCS receiver shall determine the alignment of the first PDB of a Transmit Block to extract the PDBs from the descrambled bit stream. The PDBs are then finally processed by the 64B/65B decoder to extract the GMII receive data stream. The 64B/65B decoding also includes the information that indicates the parts of the bit stream that have been determined to be corrupted (i.e., belong to MLCC codewords that cannot be corrected). Such corrupted data is signaled on the RX GMII by setting RX_ER = 1.

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The 64B/65B decoder implementation shall produce the same result as the following code.[197, 198]

```
% Variables definition
GMII.RX_ER      % GMII RX_ER signal, 1xL row vector
GMII.RX_DV      % GMII RX_DV signal, 1xL row vector
GMII.RXD        % GMII RXD bus, 1xL row vector
PCS_DEC_EN      % rx_gmii_enable (see 115.3.5.1) value for each GMII
                % transfer, 1xL vector
PDB.TYPE        % PDB type field, 1x(L/8) row vector
PDB.PAYLOAD     % PDB payload field, 8x(L/8) matrix
PDB.PAYLOAD_ERR % PDB payload error flag, 8x(L/8) matrix. It indicates
                % if any of the bits within the corresponding byte of
                % the PDB payload belongs to a codeword that could not be
                % corrected.
PDB.TYPE_ERR    % PDB type field error flag, 1x(L/8) row vector. It
                % indicates if the type bit of the PDB belongs to a
                % codeword that could not be corrected.

% 64B/65B decoding procedure
for i = 1:length(PDB.TYPE)
   if (PDB.TYPE_ERR(i) | (PDB.TYPE(i) & PDB.PAYLOAD_ERR(1,i)))
      % Complete PDB is in error. Decode forward error propagation.
      GMII.RX_DV(8*(i-1)+1:8*(i-1)+8) = ones(1, 8);
      GMII.RX_ER(8*(i-1)+1:8*(i-1)+8) = ones(1, 8);
      GMII.RXD  (1:8, i)              = zeros(8, 1);

   elseif (PDB.TYPE(i))
      % Decode PDB.CTRL payload
      OFS  = bitand(PDB.PAYLOAD(1,i),   7*2^3)/2^3;
      LEN  = bitand(PDB.PAYLOAD(1,i),   7);
      CTRL = bitand(PDB.PAYLOAD(:,i).', 3*2^6)/2^6;

      % Assign initial data.
      if (OFS > 0)
         GMII.RX_DV(8*(i-1)+1:8*(i-1)+OFS) = ...
           ones(1,OFS);

         GMII.RX_ER(8*(i-1)+1:8*(i-1)+OFS) = ...
           PDB.PAYLOAD_ERR(2:OFS+1, i).';

         GMII.RXD(8*(i-1)+1:8*(i-1)+OFS) = ...
           PDB.PAYLOAD(2:OFS+1, i).';
      end

      % Assign control information.
      GMII.RX_DV(8*(i-1)+OFS+1:8*(i-1)+OFS+1) = ...
        (CTRL(1) == 0) | PDB.PAYLOAD_ERR(1, i).';

      GMII.RX_ER(8*(i-1)+OFS+1:8*(i-1)+OFS+1) = ...
        (CTRL(1) ~= 1) | PDB.PAYLOAD_ERR(1, i).';

      GMII.RXD(8*(i-1)+OFS+1:8*(i-1)+OFS+1) = ...
        (CTRL(1) == 2);

      if (LEN > 0)
         GMII.RX_DV(8*(i-1)+OFS+2:8*(i-1)+OFS+LEN+1) = ...
           (CTRL(OFS+2:OFS+LEN+1) == 0) | ...
           PDB.PAYLOAD_ERR(OFS+2:OFS+LEN+1, i).';

         GMII.RX_ER(8*(i-1)+OFS+2:8*(i-1)+OFS+LEN+1) = ...
           (CTRL(OFS+2:OFS+LEN+1) ~= 1) | ...
           PDB.PAYLOAD_ERR(OFS+2:OFS+LEN+1, i).';

         GMII.RXD(8*(i-1)+OFS+2:8*(i-1)+OFS+LEN+1) = ...
           (CTRL(OFS+2:OFS+LEN+1) == 2);
```

[197]This code is written in the MATLAB programming language (see 1.3); however, use of this language does not indicate an endorsement of MATLAB by IEEE and, as such, any tool can be used to perform this calculation.

[198]*Copyright release for MATLAB code:* Users of this standard may freely copy or reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

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```
        end

        % Assign final data.
        if ((OFS+LEN+1) < 8)
           GMII.RX_DV(8*(i-1)+OFS+LEN+2:8*(i-1)+8) = ...
             ones(1, 8-(OFS+LEN+1));

           GMII.RX_ER(8*(i-1)+OFS+LEN+2:8*(i-1)+8) = ...
             PDB.PAYLOAD_ERR(OFS+LEN+2:8, i)';

           GMII.RXD(8*(i-1)+OFS+LEN+2:8*(i-1)+8) = ...
             PDB.PAYLOAD(OFS+LEN+2:8, i)';
        end

     else
        % Decode PDB.DATA payload
        GMII.RX_DV(8*(i-1)+1:8*(i-1)+8) = ones(1,8);
        GMII.RX_ER(8*(i-1)+1:8*(i-1)+8) = PDB.PAYLOAD_ERR(1:8, i).';
        GMII.RXD  (8*(i-1)+1:8*(i-1)+8) = PDB.PAYLOAD(1:8, i).';
     end
  end

  % When PCS_DEC_EN = 0, idles are generated
  GMII.RX_DV = GMII.RX_DV & PCS_DEC_EN;
  GMII.RX_ER = GMII.RX_ER & PCS_DEC_EN;

  % Data reception error is signaled when PCS_DEC_EN transitions to 0
  % in the middle of a packet transfer
  idx_err = find([(diff(PCS_DEC_EN) < 0) 0] & GMII.RX_DV)+1;
  GMII.RX_DV(idx_err) = 1;
  GMII.RX_ER(idx_err) = 1;
```

115.3 Physical Medium Attachment (PMA) sublayer

The Physical Medium Attachment sublayer includes the transmit and receive functions and the protocols for management of the 1000BASE-H link. This management includes exchange of information that is encoded within the PHD and the state diagrams that control both the local and remote PHYs. PHD information is encoded into the PHS as defined in 115.2.3. PMA operational information is gathered and organized for transmission by the Header Builder (see Figure 115–9).

115.3.1 PMA transmit function

The PMA transmit function comprises the Tomlinson-Harashima precoding for the payload data sub-blocks and the power scaling for the pilot S1, pilot $S2_x$, PHS_x, and payload data sub-blocks. The resultant payload PAM16 symbols from PCS transmit function are THP processed to compensate intersymbol interference produced in the communication channel. The THP processing is not applied to pilot S1, pilot $S2_x$, and PHS_x sub-blocks. The power scaling, with different factors, is performed producing similar dynamic range in every part of the Transmit Block before the symbols are transmitted to the PMD sublayer.

115.3.1.1 Payload data Tomlinson-Harashima precoding

The PAM16 symbols from the payload data symbol scrambler (see 115.2.4.4), x, shall be processed by the Tomlinson-Harashima precoder (THP) to produce a precoded sequence of symbols, y, according to Equation (115–19), Equation (115–20), and Equation (115–21):

$$v(m) = \sum_{i=0}^{8} c(i)y(m-i-1) \tag{115–19}$$

$$u(m) = x(m) + v(m) \tag{115–20}$$

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$$y(m) = \mathrm{mod}(u(m) + 16, 32) - 16 \quad (115–21)$$

where the modulo operator is defined in Equation (115–4). The THP precoded symbols can take any value in the interval $-16 \le y(m) < +16$. The coefficients of the finite-impulse-response (FIR) feedback filter $c(i)$ are set from the PHD received from the link partner (see 115.3.6). The length of the feedback filter is 9 taps. The state of the feedback filter shall be reset before the transmission of any payload data sub-block. The Tomlinson-Harashima precoder is illustrated in Figure 115–21.

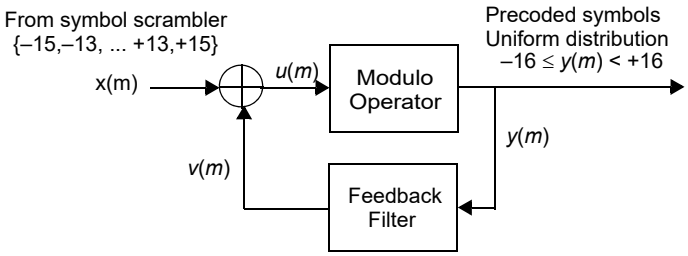

Figure 115–21—Tomlinson-Harashima precoding block diagram

115.3.1.2 Transmit power scaling

The symbols of pilot S1, pilot $S2_x$, PHS_x sub-blocks, and payload data sub-blocks shall be scaled before transmission to the PMD transmit function, by multiplying the symbols by the corresponding scaling factor specified in Table 115–5. As indicated in Table 115–5, the scaling factor used for each symbol depends on the part of the Transmit Block to which the symbol belongs.

Power scaling shall be performed directly to the symbols received from the PCS transmit for pilot S1, pilot $S2_x$, and PHS_x sub-blocks. For the payload data sub-blocks, the power scaling shall be performed to the output symbols of the Tomlinson-Harashima precoder.

Table 115–5—Transmit power scaling factors

Transmit Block part	Scaling factor
Pilot S1 sub-blocks	255/256
Pilot $S2_x$ sub-blocks	9/64
PHS_x sub-blocks	255/256
THP processed payload data sub-blocks	1/16

115.3.2 PMA receive function

The PMA receive function comprises clock recovery for correct time sampling of received symbols and adaptive channel equalization.

The PMA performs clock recovery on the received signal. The clock recovery includes coarse timing recovery for symbol synchronization and fine timing recovery to provide a stable clock to sample the received signal from the PMD with a suitable phase for reliable reception (see 115.3.7.1).

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Equalization is performed using the adaptive THP protocol (115.3.6) coordinated between the receiver and link partner transmitter to condition the transmitted signal for the characteristics of the fiber optic channel. The receiver estimates the coefficients that are to be used by the remote PHY transmitter to precode the payload data sub-blocks [coefficients $c(i)$ in 115.3.1.1]. This estimation should be based on received pilot $S2_X$ sub-blocks.

In general, harmonic distortion that affects the received signal can exist due to the non-linear response of the PMD photonics. The PMA receiver should implement non-linear channel response compensation in addition to the THP protocol. For estimation of the filters that linearize the channel, the PHY should also use the received pilot $S2_X$ sub-blocks. The channel linearization technique is up to the implementer but is to be fully implemented in the PHY receiver; it does not require coordination with the link partner transmission.

115.3.3 Interface to the PMD

The interface between the PMA and the PMD are signals for which no specific implementation is specified.

115.3.3.1 Signals transmitted to the PMD

Any signal transmitted to the PMD by the PMA transmitter can be expressed in a general form independent of the specific part of the Transmit Block (see 115.2.1) as follows:

$$x(n) = SF(n) \times F_M\left(a(n) + \sum_{i=0}^{8} x(n-i-1)c(i)\right) \tag{115–22}$$

where, $a(n)$ is a PAM-M modulation symbol that can take its value from the set $\{-M+1, -M+3, \ldots +M-3, +M-1\}$ to be transmitted at time instants $n \times T_s$, where T_s is the transmit symbol period (nominally $T_s = 1000/325$ ns), $SF(n)$ is the power scaling factor specified in Table 115–5 for each part of the Transmit Block according to 115.3.1.2, $c(i)$ are the coefficients of the THP specified in 115.3.1.1, and the nonlinear operation $F_M(\alpha) = \text{mod}(\alpha + M, 2M) - M$ corresponds to moving the signal $\alpha(n)$ to a reduced signal $\beta(n) = \alpha(n) + 2M \times m(n)$ with the integer $m(n)$ chosen for each sample such that the output lies in the interval $-M \le \beta(n) < M$, when THP is used.

When a pilot S1 sub-block or PHS_X sub-block is transmitted, $M = 2$. For generation of an $S2_X$ sub-block, $M = 8$. For the zero symbol sequences that prefix and postfix each pilot S1 sub-block, pilot $S2_X$ sub-block, and PHS_X sub-block, $a(n) = 0$.

When payload data sub-blocks are transmitted, $M = 16$. Only for this part of the Transmit Block can the coefficients $c(i)$ take a value different than zero, when the THP coefficients provided by the link partner are used according to the protocols defined in 115.3.6.

For any part of the Transmit Block, after scaling, the transmitter output signal $x(n)$ fits $-1 \le x(n) < +1$.

115.3.3.2 Signals received from PMD

Signals received from the PMD can be expressed as pulse-amplitude modulated signals that have been filtered by a non-linear channel and corrupted by noise as follows in Equation (115–23):

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$$y(n) = w_{o0} + \sum_{l_1=0}^{L} w_{o1}(l_1)x(n-l_1) + \sum_{l_1=0}^{L}\sum_{l_2=0}^{L} w_{o2}(l_1, l_2)x(n-l_1)x(n-l_2) + \ldots$$
$$\ldots + \sum_{l_1=0}^{L}\sum_{l_2=0}^{L}\ldots\sum_{l_P=0}^{L} w_{oP}(l_1, l_2, \ldots l_P)x(n-l_1)x(n-l_2)\ldots x(n-l_P) + N(n) \quad (115\text{–}23)$$

where the received signal $y(n)$ is sampled by the PMA receive function with the recovered clock, at the optimum phase and with a frequency equal to the transmit symbol clock with nominal value of 325 MBd. $x(n)$ is the transmitted signal from the PMA transmit function to the PMD transmit function, $N(n)$ is the additive noise from PMD receiver due optical signal conversion, and w_{ox} are the kernels of a truncated Volterra series that represents the non-linear response of the communication channel.

The received signal $y(n)$ of Equation (115–23) includes the effect of the end-to-end communication channel composed of all the elements from the PMA transmitter to the PMA receiver, including the conversion to optical signal carried out by the PMD transmitter, the fiber optic channel, and the conversion from optical signal carried out by the PMD receive function.

115.3.4 Physical Header Data (PHD)

The PHD shall consist of the fields detailed in Table 115–6.

Table 115–6—PHD definition

Field name	Description	Number of bits	Valid values
PHD.TX.NEXT.MODE	Transmission mode of the next Transmit Block, indicated to link partner to align its reception (see 115.5.1)	3	0: normal transmission 1: zeros transmission for BER test 2 through 7: reserved
PHD.TX.NEXT.THP.SETID	Identifier of the THP coefficients set that will be used to transmit the next Transmit Block (see 115.3.6.2)	2	0: next Transmit Block is not THP processed 1, 2, 3: THP set identifier
PHD.TX.NEXT.PDB.OFFSET	Encodes the number of bits between the first payload bit of the next Transmit Block and the start of the first PDB in that block (see 115.2.4.1.3). Offset 0 indicates the first PDB starts aligned to first payload bit of Transmit Block	7	0x00 through 0x40
PHD.RX.REQ.THP.SETID	Requested THP coefficients set identifier (see 115.3.6.3)	2	0: no request to apply the THP coefficients received in PHD.RX.REQ.THP.COEF[8:0] 1, 2, 3: THP set identifier

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Table 115–6—PHD definition *(continued)*

Field name	Description	Number of bits	Valid values
PHD.RX.REQ.THP.COEF[0]	Requested THP coefficients when PHD.RX.REQ.THP.SETID is not equal to 0 (see 115.3.6.3). These are the 9 coefficients $c(i)$ requested to be used in transmission according to Equation (115–19) (see 115.3.1.1)	12	Fixed-point formatted (12, 2) (see 115.3.8)
PHD.RX.REQ.THP.COEF[1]		12	Fixed-point formatted (12, 2)
PHD.RX.REQ.THP.COEF[2]		12	Fixed-point formatted (12, 2)
PHD.RX.REQ.THP.COEF[3]		12	Fixed-point formatted (12, 2)
PHD.RX.REQ.THP.COEF[4]		12	Fixed-point formatted (12, 2)
PHD.RX.REQ.THP.COEF[5]		12	Fixed-point formatted (12.2)
PHD.RX.REQ.THP.COEF[6]		12	Fixed-point formatted (12, 2)
PHD.RX.REQ.THP.COEF[7]		12	Fixed-point formatted (12, 2)
PHD.RX.REQ.THP.COEF[8]		12	Fixed-point formatted (12, 2)
PHD.RX.LINKSTATUS	Indicates whether the local PHY is able to receive PAM16 symbols belonging to payload data sub-blocks with reliability. The value of this field is determined by the PHY quality monitor state diagram (see 115.3.7.4). The local PHY uses this received PHD field to determine the value of the variable rem_rcvr_status (see 115.3.5.4)	1	0: NOT_OK 1: OK
PHD.RX.HDRSTATUS	Indicates whether the local PHY is able to receive the PHD from its link partner with reliability. The value of this field is determined by the local PHD reception monitor state diagram. The local PHY uses this received PHD field to determine the value of the variable rem_rcvr_hdr_lock (see 115.3.5.5)	1	0: NOT_OK 1: OK
PHD.RX.LINKMARGIN	The value of this field is determined by the PHY quality monitor state diagram (see 115.3.7.4) in response to link margin estimation as defined in 115.3.7.2. Upon PHD reception, the field is stored in bits 3.521.7:0 (see 45.2.3.56.1)	8	This field is fixed-point formatted (8, 3) and is provided in $\log_2$ units (see 115.3.7.2). See 115.3.8 for fixed-point format.
PHD.CAP.LPI	This field indicates the PHY supports and has enabled EEE, and that it is able to transmit and receive Low Power Idle (see 115.4)	1	0: EEE is not supported or is disabled 1: EEE is supported and is enabled

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Table 115–6—PHD definition *(continued)*

Field name	Description	Number of bits	Valid values
PHD.CAP.OAM	This field indicates the PHY supports and has enabled 1000BASE-H OAM, and that it is able to transmit and receive management information by using the PHD.OAM.* fields (see 115.9)	1	0: 1000BASE-H OAM is not supported or is disabled 1: 1000BASE-H OAM is supported and is enabled
	Reserved	58	0
PHD.OAM.DATA0	1000BASE-H OAM message data field 0. See 115.9	12	0x000 through 0xFFF
PHD.OAM.MSGT	1000BASE-H OAM message identification bit. See 115.9	1	0 or 1
PHD.OAM.MERT	1000BASE-H OAM STA read identification bit (see 115.9)	1	0 or 1
PHD.OAM.PHYT	1000BASE-H OAM PHY reception identification bit (see 115.9)	1	0 or 1
	Reserved	1	0
PHD.OAM.DATA1	1000BASE-H OAM message data field 1 (see 115.9)	16	0x0000 through 0xFFFF
PHD.OAM.DATA2	1000BASE-H OAM message data field 2	16	0x0000 through 0xFFFF
PHD.OAM.DATA3	1000BASE-H OAM message data field 3	16	0x0000 through 0xFFFF
PHD.OAM.DATA4	1000BASE-H OAM message data field 4	16	0x0000 through 0xFFFF
PHD.OAM.DATA5	1000BASE-H OAM message data field 5	16	0x0000 through 0xFFFF
PHD.OAM.DATA6	1000BASE-H OAM message data field 6	16	0x0000 through 0xFFFF
PHD.OAM.DATA7	1000BASE-H OAM message data field 7	16	0x0000 through 0xFFFF
PHD.OAM.DATA8	1000BASE-H OAM message data field 8	16	0x0000 through 0xFFFF
	Reserved	368	0

The fields PHD.TX.NEXT.* are used by the local PHY to provide the link partner with information about the next Transmit Block, so that the remote PHY can align its reception.

The fields PHD.RX.* are transmitted to inform the link partner of the status of the local reception. Specifically, the fields PHD.RX.REQ.THP.SETID and PHD.RX.REQ.THP.COEF[8:0] allow the PHY to request the update of link partner THP coefficients (see 115.3.6). Additionally, PHD.RX.LINKSTATUS indicates whether payload data sub-blocks are being received with reliability, and PHD.RX.HDRSTATUS

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signals the correct/incorrect reception of PHDs. The field PHD.RX.LINKMARGIN is used to report the link margin.

PHD.RX.REQ.THP.COEF[8:0] and PHD.RX.LINKMARGIN fields are fixed-point formatted (12, 2) and (8, 3), respectively. See 115.3.8 for fixed-point format definition.

PHD.CAP.* fields indicate if the local PHY is using optional features. PHD.CAP.LPI is used by the PHY to advertise that Energy-Efficient Ethernet (EEE) is supported and that it is enabled, and the field PHD.CAP.OAM signals that the PHY implements the capability to run the 1000BASE-H OAM message exchange protocol and that it is enabled.

PHD.OAM.* fields are used to transmit and receive 1000BASE-H OAM messages.

All the PHD fields are transmitted from the least to the most significant bit and are transmitted from top to bottom of Table 115–6.

Each PHY has to deal with transmit and receive PHDs simultaneously. The prefix LOCPHD refers to the fields of the PHD to be included in the next Transmit Block transmitted to the link partner (from the local PHY). LOCPHD fields assigned by the state diagrams shall be sampled at the start of a Transmit Block by the Header Builder to create the PHS included in that current Transmit Block.

The prefix REMPHD refers to the fields of the most recent PHD received, decoded, and validated from the link partner (from the remote PHY). The new values of REMPHD fields shall be available to the state diagrams and registers immediately after reception, decoding, and validation of the entire PHS (PHS_0 to PHS_{13}) and before the reception of the Transmit Block that includes that PHS is completed.

115.3.5 PHY control

115.3.5.1 PHY control state variables

hdr_crc16_status
: Result of the CRC16 evaluation for a received PHD from the link partner; this variable is assigned for each received PHD.
  Values: OK: The most recent received PHD is correct as determined by CRC16 verification
  NOT_OK: The most recent received PHD is not correct as determined by CRC16 verification

hdr_fail_count
: Variable used to count the reception of contiguous erroneous PHDs.

link_control
: Variable that controls PMA functional operation. All state diagrams respond to the open-ended link_control = DISABLE.
  Values: DISABLE: Prevent operation of PMA sublayer
  ENABLE: Permit operation of PMA sublayer

link_status
: Variable that is set by the link monitor state diagram and used by PHY TX and PHY RX control state diagrams to control the 64B/65B encoder and 64B/65B decoder operation.
  Values: OK: The link has been established between link partners with data reliability in both communication directions
  FAIL: Link is not established (one or both directions are not providing reliable payload data decoding)

loc_rcvr_hdr_lock
: Variable set by the local PHD reception monitor state diagram to indicate the reliability of PHD reception.

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Values: OK: Local PHD reception is reliable
NOT_OK: Local PHD reception is unreliable

loc_rcvr_status

Variable set by the PHY quality monitor state diagram to indicate correct or incorrect payload data decoding by the local PHY receiver.

Values: OK: Payload data reception by the local PHY is reliable
NOT_OK: Payload data reception by the local PHY is unreliable

new_rxblock_event

Signal sent by the PHY receiver to indicate the start of reception of a new Transmit Block. This event persists only long enough to cause one state diagram transition.

new_rxphd_event

Signal sent by the PHY receiver to indicate the complete reception (including data decoding and CRC16 checking) of a new PHD from the link partner. This event persists only long enough to cause one state diagram transition.

pma_reset

Variable that causes reset of all PMA functions. PMA reset occurs with power on or the PHY reset being set to one (bit 1.0.15). All state diagrams respond to the open-ended pma_reset = ON.

Values: ON: Reset is asserted
OFF: Reset is deasserted

rcvr_clock_lock

Variable set by the PMA receive clock recovery function to indicate that the clock has been properly recovered from the received signal.

Values: OK: Clock is stable and phase adjusted for sampling the received signal
NOT_OK: Clock has not been recovered from the received signal and/or it is not stable

rcvr_hdr_lock

Variable set by the PHD monitor state diagram to indicate the reliability of both the PHD transmission from local to remote PHY and the PHD reception from remote to local PHY.

Values: OK: PHD transmission and reception are reliable
NOT_OK: PHD transmission or reception are unreliable

rcvr_thp_lock

Variable set by the THP REQ state diagram (see 115.3.6.3) to indicate whether the Tomlinson-Harashima precoding is initialized, therefore the PHY is receiving payload data sub-blocks THP processed with the coefficients that were requested by the THP REQ state diagram.

Values: OK: THP is initialized; payload data are received THP processed
NOT_OK: THP is not initialized

rem_rcvr_hdr_lock

Variable set by the remote PHD reception monitor state diagram to indicate the reliability of PHD reception in the remote PHY (link partner).

Values: OK: Link partner PHD reception is reliable
NOT_OK: Link partner PHD reception is unreliable

rem_rcvr_status

Variable set by the link monitor state diagram. It indicates the receiver status of the remote (link partner) PHY payload data decoding.

Values: OK: Payload data reception by the remote PHY is reliable
NOT_OK: Payload data reception by the remote PHY is unreliable

rx_gmii_enable

Variable set by the PHY RX control state diagram to control the 64B/65B decoder operation (see 115.2.5).

Values: TRUE: The 64B/65B decoder receives PDBs from the link partner and decodes them into GMII receive data stream transfers

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FALSE: The 64B/65B decoder does not decode received PDBs from the link partner

s1_synch

Variable set by the PMA receive clock recovery function to indicate synchronization with the start of Transmit Blocks.

Values: OK: Synchronization based on pilot S1 signal has been achieved
NOT_OK: Synchronization has not been achieved

tx_enable

Variable set by the PHY TX control state diagram to enable PCS and PMA transmission.

Values: TRUE: PCS and PMA transmission is enabled
FALSE: PCS and PMA transmission is disabled

tx_gmii_enable

Variable set by the PHY TX control state diagram to control the 64B/65B encoder operation (see 115.2.4.1.2).

Values: TRUE: The 64B/65B encoder encodes the GMII transmit data stream transfers into PDBs
FALSE: The 64B/65B encoder does not encode the GMII transmit data stream. Normal inter-frame is encoded in transmitted PDBs

tx_gmii_idle

Variable that indicates the idle status of the GMII transmit data path.

Values: TRUE: The value of TX_EN signal of the current GMII transfer in GMII transmit stream is 0
FALSE: The value of TX_EN signal of the current GMII transfer in GMII transmit stream is 1

115.3.5.2 PHY TX control state diagram

Transmit operation shall conform to the PHY TX control state diagram in Figure 115–22.

Upon reset or disable of the PMA, PHY transmit operation is disabled (state PMATX_DISABLE_TX). Once the PMA is enabled (link_control = ENABLE), the local PHY starts sending Transmit Blocks as explained in 115.2.1 (state PMA_ENABLE_TX), so that the remote PHY can perform clock recovery and train its equalizers (tx_enable ⇐ TRUE).

While establishing the bi-directional link, the 64B/65B PCS encoder does not encode the GMII transmit stream (tx_gmii_enable ⇐ FALSE). Once the bidirectional link is established, the 64B/65B encoder checks, and if necessary, waits until the GMII transmit data stream transfer is not part of a packet or error propagation (link_status = OK * tx_gmii_idle = TRUE); and then begins encoding the GMII transmit stream into PDBs (tx_gmii_enable ⇐ TRUE in state PMATX_PCS_DATA). If one of the link partners fails to receive payload data sub-blocks with reliability (link_status = FAIL), the 64B/65B PCS encoder does not encode the GMII transmit stream until the bidirectional link is re-established.

115.3.5.3 PHY RX control state diagram

Receive operation shall conform to the PHY RX control state diagram in Figure 115–23.

Upon reset or disable of the PMA, PHY receive operation is disabled. Once the PMA is enabled (link_control = ENABLE), the PHY receiver begins link establishment by recovering clock from the received signal. The clock recovery comprises two stages. The first stage is coarse timing recovery in PMARX_TIMING_COARSE, where symbol synchronization shall be performed using the a priori known pilot signal contained in the S1 sub-block at the beginning of each received Transmit Block (see Figure 115–4). After symbol synchronization is achieved (s1_synch = OK), fine timing recovery shall be carried out in order to provide a stable clock that samples the received signal with a suitable phase for reliable reception

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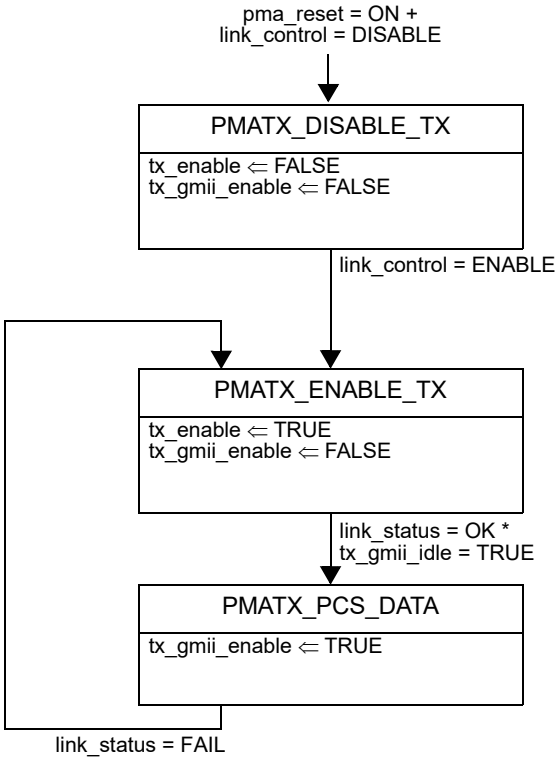

Figure 115–22—PHY TX control state diagram

(see 115.3.7.1). Fine timing recovery can be implemented with data-aided algorithms that use the received pilot S1 and pilot $S2_x$ sub-blocks.

When clock is stable (rcvr_clock_lock = OK), the PHY receiver shall train the equalizers based on the received pilot $S2_x$ sub-blocks in order to compensate the intersymbol interference caused by the communication channel. Blind tracking algorithms for timing recovery can be enabled after the equalizer training has finished.

Once the equalizers have been properly estimated, the PHY receiver processes each PHD from the link partner to determine if PHD reception is reliable in both directions. The state diagrams that monitor the reliability of PHD reception are described in 115.3.5.5.

As soon as both link partners detect reliable PHD reception (rcvr_hdr_lock = OK), the PHY receiver shall initialize the THP following the state diagram explained in 115.3.6.3. Once the local PHY is receiving payload data sub-blocks THP processed with the coefficients that were requested to the link partner (rcvr_thp_lock = OK), it has to determine according to the state diagram described in 115.3.7.3 whether this reception is reliable.

Once a bidirectional link is established (link_status = OK), the 64B/65B PCS decoder begins to decode the received PDBs onto the GMII receive data stream (rx_gmii_enable ⇐ TRUE). Furthermore, both link partners are able to properly use the PHD to carry out continuous adaptation of THP coefficients.

If one of the link partners fails to receive payload data sub-blocks with reliability (link_status = FAIL), the 64B/65B PCS decoder does not decode PDBs received from link partner into the GMII receive stream (rx_gmii_enable ⇐ FALSE) until the bidirectional link is re-established (link_status = OK).

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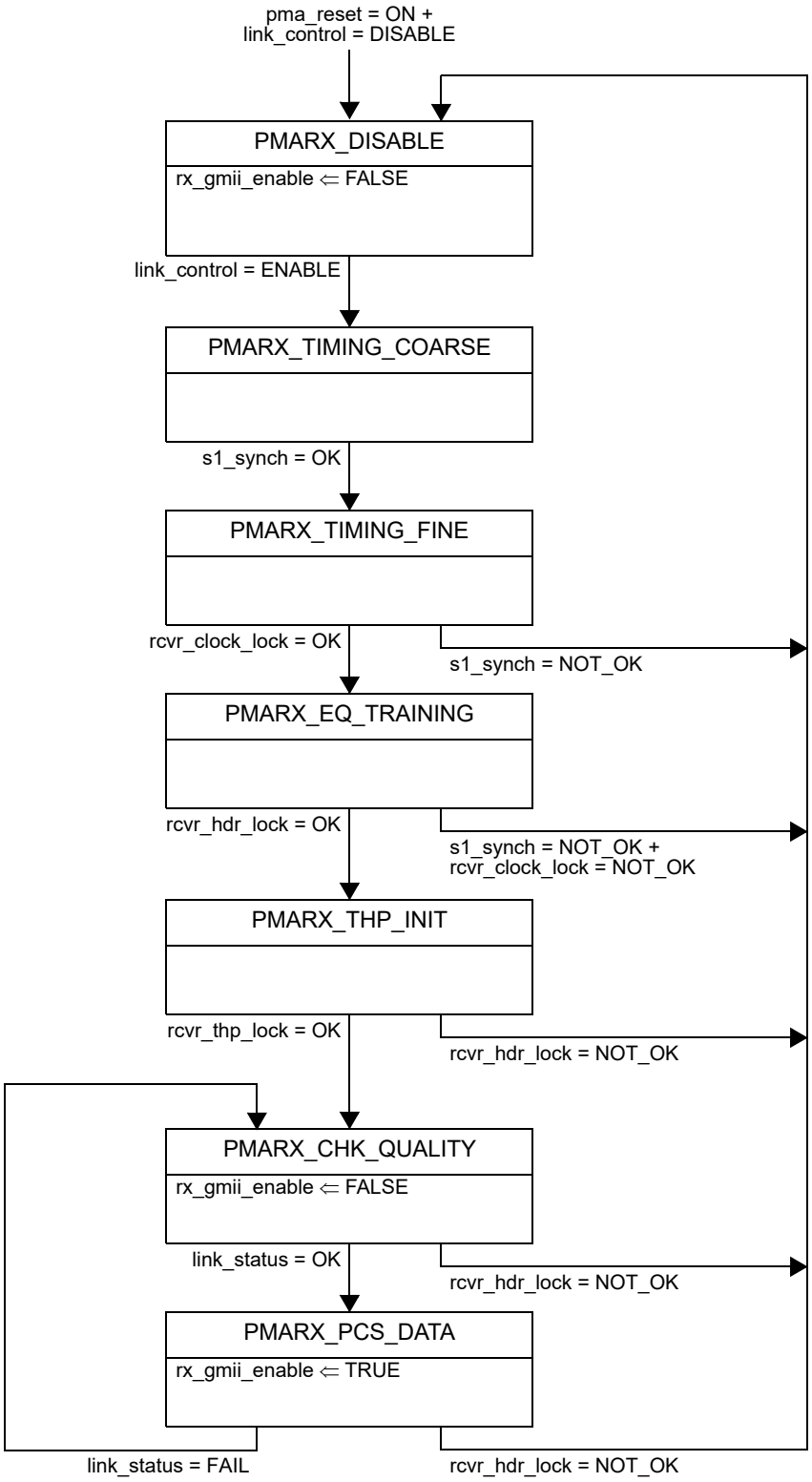

Figure 115–23—PHY RX control state diagram

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115.3.5.4 Link monitor state diagram

Link status shall be determined as specified by the link monitor state diagram in Figure 115–24. The state diagram determines the value of link_status and rem_rcvr_status state variables.

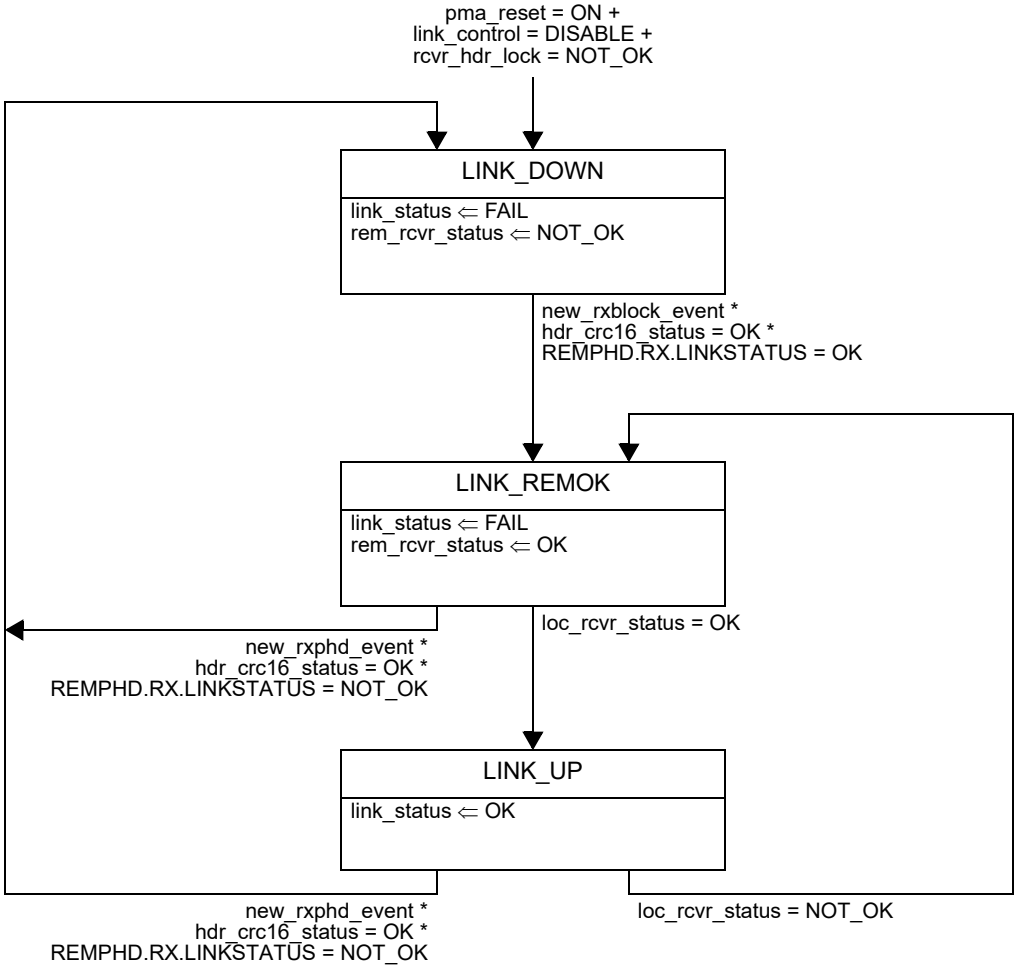

Figure 115–24—Link monitor state diagram

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Upon reset, disable of the PMA or unreliable PHD communication, the link is lost (link_status ⇐ FAIL) and the remote receiver status is unknown (rem_rcvr_status ⇐ NOT_OK). When the remote PHY indicates reliable reception (REMPHD.RX.LINKSTATUS = OK), the state diagram transitions to the LINK_REMOK state synchronously on the event of receiving a new Transmit Block (new_rxblock_event). Once in this state, the bidirectional link is established (link_status ⇐ OK) when local reliable reception is signaled by the PHY quality monitor state diagram (loc_rcvr_status = OK).

If the local PHY fails to receive payload data sub-blocks with reliability (loc_rcvr_status = NOT_OK) but the remote PHY reception is indicated as reliable (REMPHD.RX.LINKSTATUS = OK), the bidirectional link is lost and the state diagram transitions to LINK_REMOK state that waits for the local receiver reliability is recovered. If the remote PHY receiver indicates that it does not operate with reliability (REMPHD.RX.LINKSTATUS = NOT_OK), the bidirectional link is lost and the state diagram transitions to LINK_DOWN state in any case.

115.3.5.5 PHD monitor state diagrams

The reliability of PHD reception and transmission shall be determined by the PHD monitor state diagrams in Figure 115–25, Figure 115–26, and Figure 115–27.

The local PHD reception monitor state diagram of Figure 115–25 monitors the PHD reception reliability for the local PHY and indicates it via the variable loc_rcvr_hdr_lock. Upon reset or disable of the PMA, or if the local PHY fails to reliably receive PHDs (loc_rcvr_hdr_lock ⇐ NOT_OK), this is indicated to the link partner by assigning NOT_OK to the field LOCPHD.RX.HDRSTATUS. In the state LOCHDR_UNLOCK, the receiver waits for reception of a valid PHD (i.e., one with correct CRC16) on entry, and the variable hdr_fail_count (the count of contiguous PHDs received with errors) is reset (hdr_fail_count ⇐ 0).

In LOCHDR_UNLOCK, reception of one correct PHD triggers the transition to the state LOCHDR_LOCK. On entry to LOCHDR_LOCK the variable loc_rcvr_hdr_lock and the field LOCPHD.RX.HDRSTATUS are assigned the value OK. The PHY keeps checking the CRC16 of received PHDs, incrementing hdr_fail_count with each erroneous PHD (in state LOCHDR_EVAL_FAIL) and resetting hdr_fail_count with each valid PHD (in state LOCHDR_EVAL_RESET). If hdr_fail_count reaches the limit of 2, or the clock recovery function detects that the PHY has lost synchronization, then the state transitions back to LOCHDR_UNLOCK.

The remote PHD reception monitor state diagram of Figure 115–26 monitors PHD reception reliability reports from the remote PHY and indicates the status via the variable rem_rcvr_hdr_lock. Upon reset, disable of the PMA or unreliable local PHD reception, the status variable rem_rcvr_hdr_lock is assigned the value NOT_OK pending the arrival of a new PHD from the link partner (REMHDR_WAIT state). From then on, the value of the variable rem_rcvr_hdr_lock is updated with the value of the field REMPHD.RX.HDRSTATUS (rem_rcvr_hdr_lock ⇐ REMPHD.RX.HDRSTATUS).

The PHD monitor state diagram of Figure 115–27 indicates via the variable rcvr_hdr_lock if both link partners are reliably receiving PHDs. Upon reset or disable of the PMA, the PHD communication is unreliable (rcvr_hdr_lock ⇐ NOT_OK). Whenever a new PHD is received from the link partner, the status of both the local (variable loc_rcvr_hdr_lock) and remote (variable rem_rcvr_hdr_lock) PHD reception are updated as indicated in Figure 115–25 and Figure 115–26, respectively.

A transition from the HDR_UNLOCK state to the HDR_LOCK state takes place when both the local and the remote PHYs are reliably receiving PHDs (loc_rcvr_hdr_lock = OK and rem_rcvr_hdr_lock = OK). The value OK is then assigned to the variable rcvr_hdr_lock to signal the reliable transmission and reception of PHDs. Subsequently, if either of the link partners fail to receive PHDs reliably (loc_rcvr_hdr_lock = NOT_OK or rem_rcvr_hdr_lock = NOT_OK), a transition to HDR_UNLOCK occurs resulting in assigning NOT_OK to the rcvr_hdr_lock variable.

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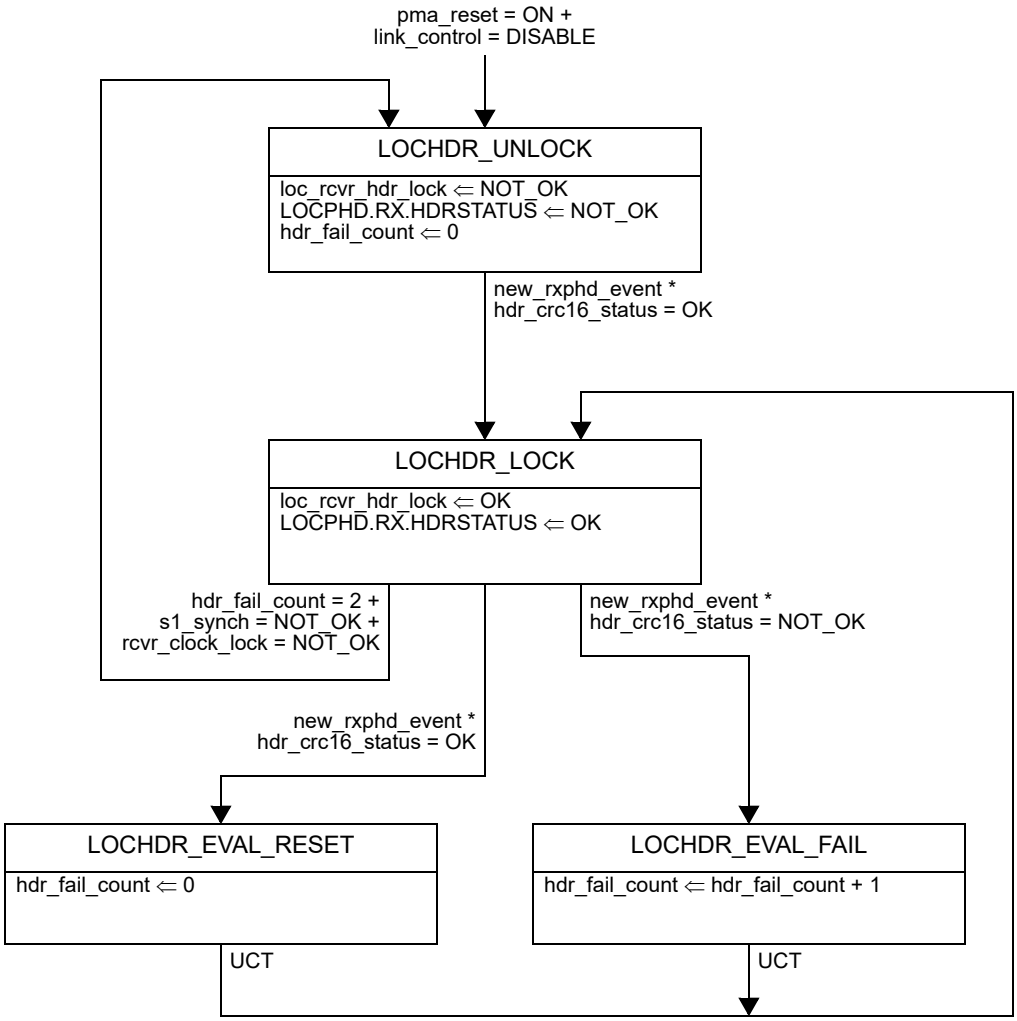

Figure 115–25—Local PHD reception monitor state diagram

115.3.6 Adaptive THP protocol

The receiver estimates the coefficients (see 115.3.2) that are used by the remote PHY transmitter for THP processing of the payload data sub-blocks [coefficients $c(i)$ in 115.3.1.1]. The state diagrams that control THP coefficients allow for dynamic adaptation of the coefficients before and after the link is established. The PHY receiver may dynamically determine variations in the channel response and request the partner to use a new set of THP coefficients. The methods to determine the channel response variation and estimate THP coefficients are implementation dependent.

The local receiver assigns a set identifier (integer number higher than 0 and lower than 4) to each new estimation to unambiguously identify it, and uses it to request the remote transmitter to apply a given set of coefficients for THP by using the field LOCPHD.RX.REQ.THP.SETID. The set of coefficients itself is sent to the link partner by using the fields LOCPHD.RX.REQ.THP.COEF[8:0].

Once the local receiver has performed the request, it waits until the remote transmitter signals via REMPHD.TX.NEXT.THP.SETID that payload data in the next Transmit Block is THP processed with the

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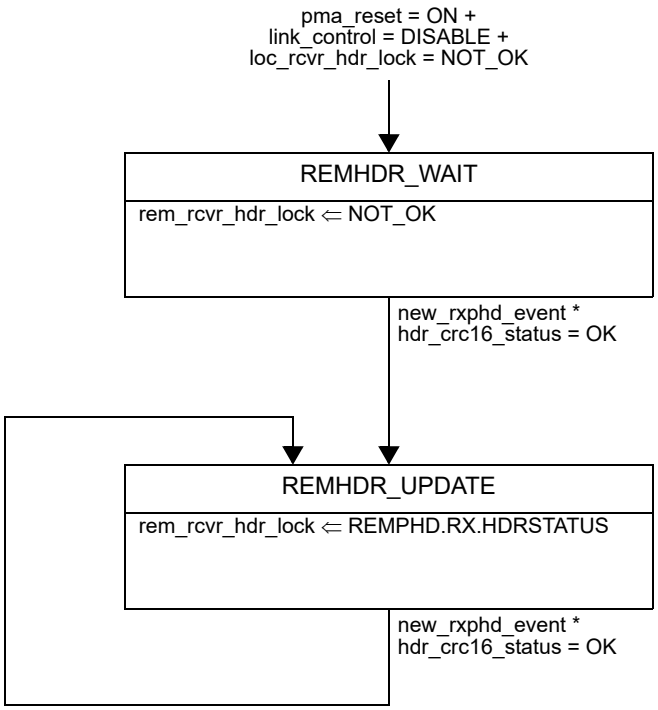

Figure 115–26—Remote PHD reception monitor state diagram

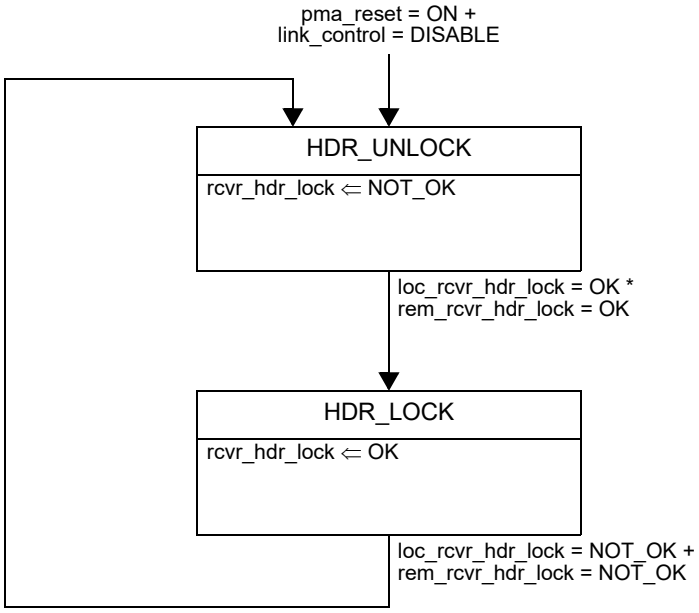

Figure 115–27—PHD monitor state diagram

requested set of coefficients. From then on, the local receiver adapts its circuitry according to the THP coefficients used at the remote transmitter and is allowed to perform a new request to change them.

A formal definition of the THP coefficients adaptation protocol is provided in the form of state diagrams in the following subclauses.

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115.3.6.1 Adaptive THP state variables

The following defines all the variables used in the adaptive THP state diagrams that have not been previously introduced:

est_thp_coef
: Variable set by the PHY receiver that contains the coefficients estimated to compensate inter-symbol interference by means of Tomlinson-Harashima Precoding. est_thp_coef is a set of 9 real numbers.
Values: Real numbers that take values such that $-2 \le$ est_thp_coef $< +2$

loc_thp_coef
: Variable set by the adaptive THP TX state diagram. It contains the local coefficients used by the PHY for THP processing of payload data sub-blocks. loc_thp_coef is a set of 9 real numbers representing the coefficients of the feedback filter of THP [$c(i)$ in 115.3.1.1].
Values: Real numbers that take values such that $-2 \le$ loc_thp_coef $< +2$

new_thp_coef_event
: Signal sent by the PHY receiver to indicate the estimation of a new set of THP coefficients is available. This event persists only long enough to cause one state diagram transition.

new_txblock_event
: Signal sent by the PHY transmitter to indicate the start of a new Transmit Block. This event persists only long enough to cause one state diagram transition.

req_thp_coef
: Variable set by the adaptive THP TX state diagram when a correct PHD is received. This variable holds the coefficients requested by the link partner to be used for THP processing of the payload data sub-blocks. req_thp_coef is a set of 9 real numbers in fixed-point format (see 115.3.8) as the fields REMPHD.RX.REQ.THP.COEF[8:0].
Values: Real numbers that take values such that $-2 \le$ req_thp_coef $< +2$

req_thp_setid
: Variable set by the adaptive THP TX state diagram when a correct PHD is received. It is the set identifier assigned to the THP coefficients requested by the link partner.
Values: 0: No request to change the THP coefficients
1, 2, 3: Requested set identifier

thp_coef
: Variable set by the adaptive THP REQ state diagram to store the last THP coefficients requested to the link partner. thp_coef is a set of 9 real numbers.
Values: Real numbers that take values such that $-2 \le$ thp_coef $< +2$

thp_setid
: Variable set by the adaptive THP REQ state diagram to store the last THP set identifier requested to the link partner.
Values: 0: Reset value
1, 2, 3: Set identifier

115.3.6.2 Adaptive THP TX state diagram

The update of the THP filter coefficients per link partner requests shall conform to the Adaptive THP TX state diagram in Figure 115–28.

Upon reset, disable of the PMA or unreliable PHD communication, transmitted payload data is no longer THP processed (THPTX_DISABLE state). This causes THP coefficients to be set to zero (loc_thp_coef $\Leftarrow$ 0) and the field LOCPHD.TX.NEXT.THP.SETID is assigned the value 0 to indicate to the remote PHY that THP is disabled.

Once the transmission and reception of PHDs are reliable (rcvr_hdr_lock = OK), the local PHY waits for a request to adapt its THP coefficients from the link partner (THPTX_WAITFOR_REQ state).

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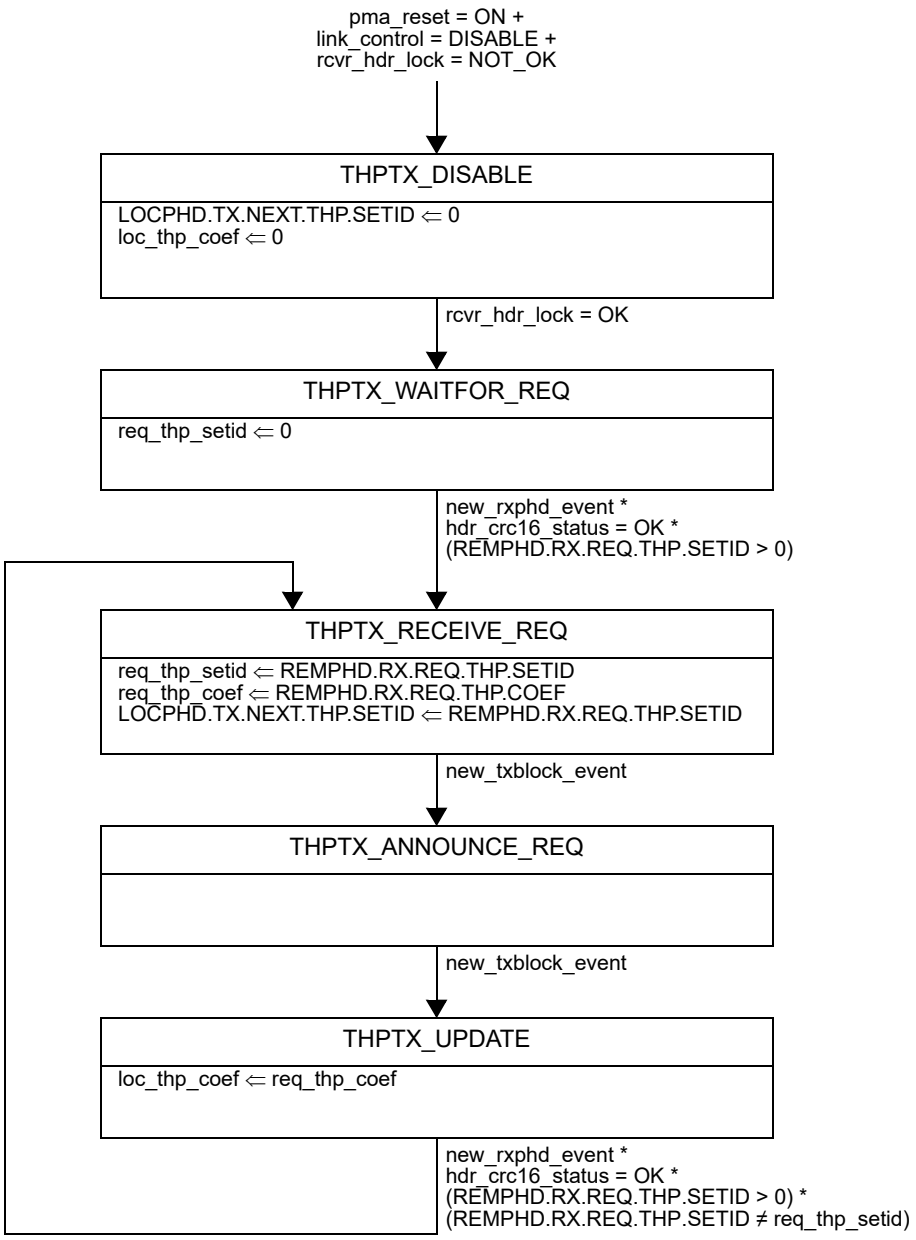

Figure 115–28—Adaptive THP TX state diagram

As soon as the value of the field REMPHD.RX.REQ.THP.SETID is not equal to zero, the field REMPHD.RX.REQ.THP.COEF also contains a THP coefficients adaptation request from the link partner. The local PHY stores both the set identifier associated with the request (req_thp_setid ⇐ REMPHD.RX.REQ.THP.SETID) and the requested coefficients (req_thp_coef ⇐ REMPHD.RX.REQ.THP.COEF). This corresponds to the state THPTX_RECEIVE_REQ.

Triggered with the start of a new Transmit Block a transition to THPTX_ANNOUNCE_REQ occurs, where the local PHY announces that requested coefficients are to be used (LOCPHD.TX.NEXT.THP.SETID ⇐ req_thp_setid assignment of previous state).

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After the announcement, the start of another new Transmit Block triggers the state transition to THPTX_UPDATE, and payload data sub-blocks of Transmit Blocks are then THP processed with the requested set of coefficients (loc_thp_coef ⇐ req_thp_coef) until a request to change THP coefficients from the link partner becomes effective. This happens when the value of the field REMPHD.RX.REQ.THP.SETID is not equal to zero and is different from the value of the variable req_thp_setid, and the new set of coefficients is stored, announced, and applied as previously explained.

115.3.6.3 Adaptive THP REQ state diagram

The requests to the link partner to update the THP filter coefficients shall conform to the Adaptive THP REQ state diagram in Figure 115–29.

Upon reset, disable of the PMA or unreliable PHD communication, the local PHY is not able to receive THP processed payload data sub-blocks (rcvr_thp_lock ⇐ NOT_OK). This is signaled to the remote PHY by assigning 0 to the field LOCPHD.RX.REQ.THP.SETID.

Once the transmission and reception of PHDs are reliable (rcvr_hdr_lock = OK) and the first set of THP coefficients are ready from the estimator (new_thp_coef_event) a transition to THPREQ_STORE occurs.

In this state, the newly estimated coefficients are stored (thp_coef ⇐ est_thp_coef) and assigned a set identifier. The set identifier is calculated based on the identifier previously requested as thp_setid ⇐ mod(thp_setid, 3) + 1, with modulo operator as defined in Equation (115–4).

The request for changing the set of THP coefficients is included in the next Transmit Block PHD (transition to THPREQ_REQUEST state). More precisely, the field LOCPHD.RX.REQ.THP.SETID indicates the associated set identifier, and the set of coefficients itself is transmitted by using the field LOCPHD.RX.REQ.THP.COEF[8:0].

In THPREQ_REQUEST, the local PHY receiver waits for the link partner to signal that the THP request has been accepted (the link partner starts using the requested coefficients for THP processing on its next Transmit Block). Once this event occurs (new_rxphd_event and hdr_crc16_status = OK and REMPHD.TX.NEXT.THP.SETID = thp_setid), a transition to THPREQ_WAITFOR_RX follows.

In THPREQ_WAITFOR_RX, the PHY receiver waits for the next Transmit Block received from the link partner. Once this event occurs, a transition to THPREQ_UPDATE is taken, where the value OK is assigned to the state variable rcvr_thp_lock, indicating that payload data sub-blocks are received with THP processing. In the THPREQ_UPDATE state the PMA receiver also adapts its circuitry to match the THP coefficients used at the remote transmitter.

Whenever a new set of THP coefficients from the estimator is available, it is stored and requested as explained previously. The local PHY receiver is not allowed to make a new THP request until the previous THP request has been acknowledged by the link partner, even if a new set of coefficients is available from the estimator.

115.3.7 PHY quality monitor

115.3.7.1 PHY quality criterion

Payload data reception is reliable when the BCH frame error ratio (BFER) is less than 8.8×10^{-11} after BCH decoding.

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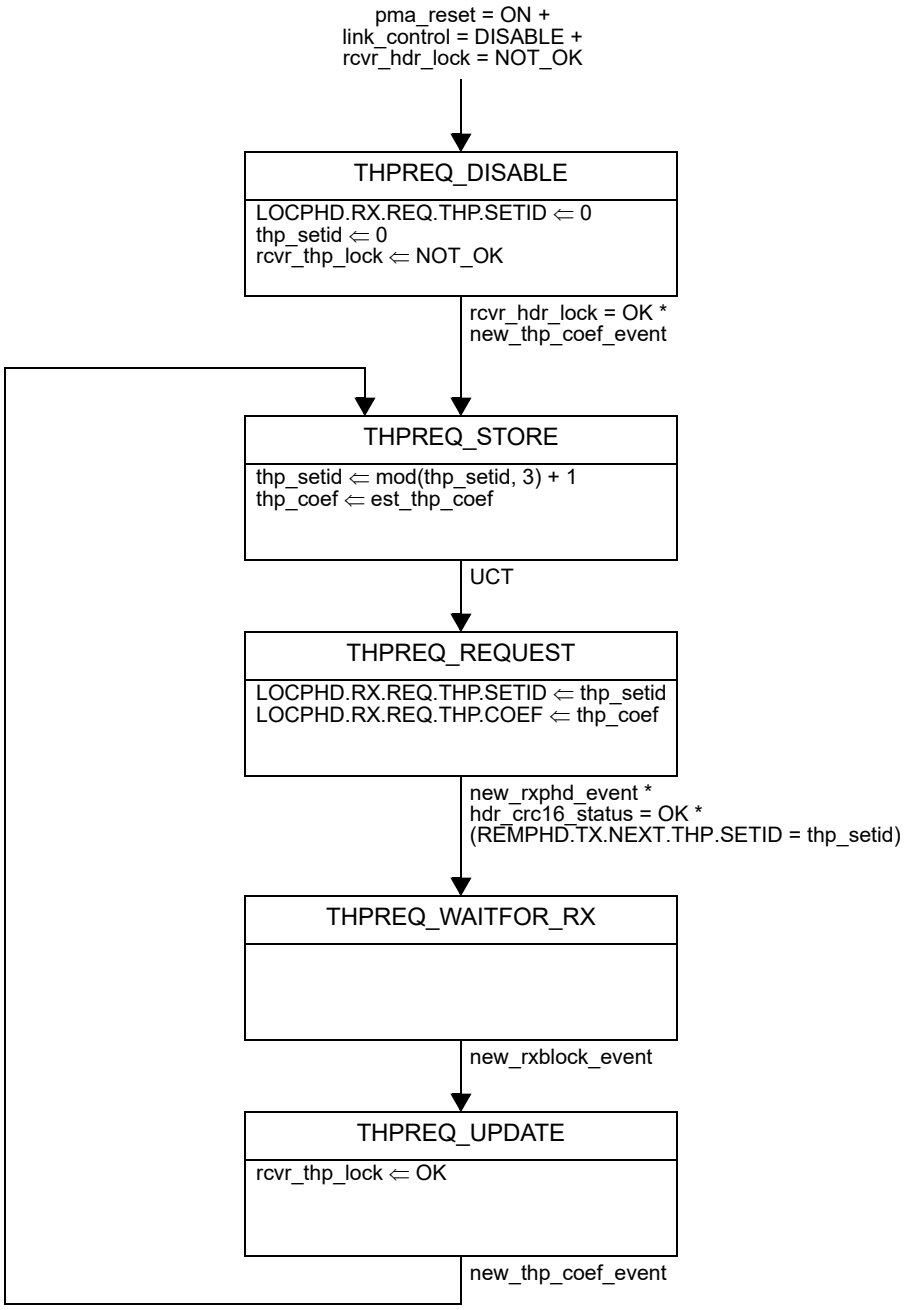

Figure 115–29—Adaptive THP REQ state diagram

115.3.7.2 PHY quality assessment

The assessment of the previously defined PHY quality criterion may be based on estimation of the noise variance at the PAM16 decoder decision points $E[n_d^2]$, which expressed in base-2 logarithmic units has to be lower than a given threshold T_{LM} to enable reliable local reception of payload data. If the condition $\log_2(E[n_d^2]) < T_{LM}$ holds, the variable loc_rcvr_status is assigned the value OK. The noise variance at the PAM16 decoder can be estimated either by measuring the Modulation Error Ratio (MER) at the decision points or measuring the ratio of corrected bits per codeword carried out by the BCH decoder of MLCC

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level 1 (see 115.2.4.3). The value of the threshold and the information used to estimate the PAM16 decoder noise variance is implementation dependent.

As defined in 115.3.4, the local PHY reports the link margin to the link partner by using the field LOCPHD.RX.LINKMARGIN. The link margin (*LM*) is defined as the SNR margin relative to the SNR required for reception of coded PAM16 with a quality per the specification in 115.3.7.1. Link margin is formally defined per Equation (115–24).

$$LM = T_{LM} - \log_2(E[n_d^2]) \quad (115–24)$$

In LPI mode of operation, the PHY can use the reception of pilot $S2_x$ sub-blocks contained in the refresh periods to estimate the link margin at the PAM16 decoder decision points.

115.3.7.3 PHY quality monitor state variables

The following defines all the variables used in the PHY quality monitor state diagram that have not been previously introduced:

new_link_margin_event
: Signal sent by the PHY receiver to indicate a new estimation of detector link margin is available. This event persists only long enough to cause one state diagram transition.

link_margin
: Variable set by the PHY receiver containing the value of the last link margin estimation.

  Values: Any value determined per Equation (115–24) with $E[n_d^2]$ and T_{LM} as defined in 115.3.7.2

115.3.7.4 PHY quality monitor state diagram

The variable loc_rcvr_status (see 115.3.5.1), which indicates if the local PHY is reliably receiving payload data per the specifications of 115.3.7.1 shall be determined as specified by the PHY quality monitor state diagram in Figure 115–30.

Upon reset, disable of the PMA or loss of PHD lock, the PHY quality monitor functionality is disabled (PMAMON_DISABLE state), and the state variable loc_rcvr_status is assigned the value NOT_OK. This is indicated to the link partner by assigning the value NOT_OK to the field LOCPHD.RX.LINKSTATUS. Additionally, the reported link margin is set to 0x80 (the smallest value representable in 8-bit signed format, see 115.3.8).

Once the local PHY begins to receive payload data sub-blocks that are properly THP processed (rcvr_thp_lock = OK), the state diagram waits for the first estimate of the link margin to be available (PMAMON_WAITING state). From then on, whenever a new estimate of the link margin is available (new_link_margin_event), it is evaluated. If link margin is larger than zero, the local reception of payload data sub-blocks is reliable.

Reliable local reception is indicated to the link partner by assigning OK to the field LOCPHD.RX.LINKSTATUS (state PMAMON_OK). After at least one locally transmitted Transmit Block, the local receiver status is signaled to the link monitor state diagram (loc_rcvr_status ⇐ OK) synchronously on the event of start of a new Transmit Block (state PMAMON_UPDATE).

Otherwise, when link margin is smaller than or equal to zero, unreliable receive link status is signaled (loc_rcvr_status ⇐ NOT_OK). This corresponds to the state PMAMON_FAIL. The local receiver status is always indicated to the link partner by using the field LOCPHD.RX.LINKSTATUS. The measured link margin is also reported via the field LOCPHD.RX.LINKMARGIN.

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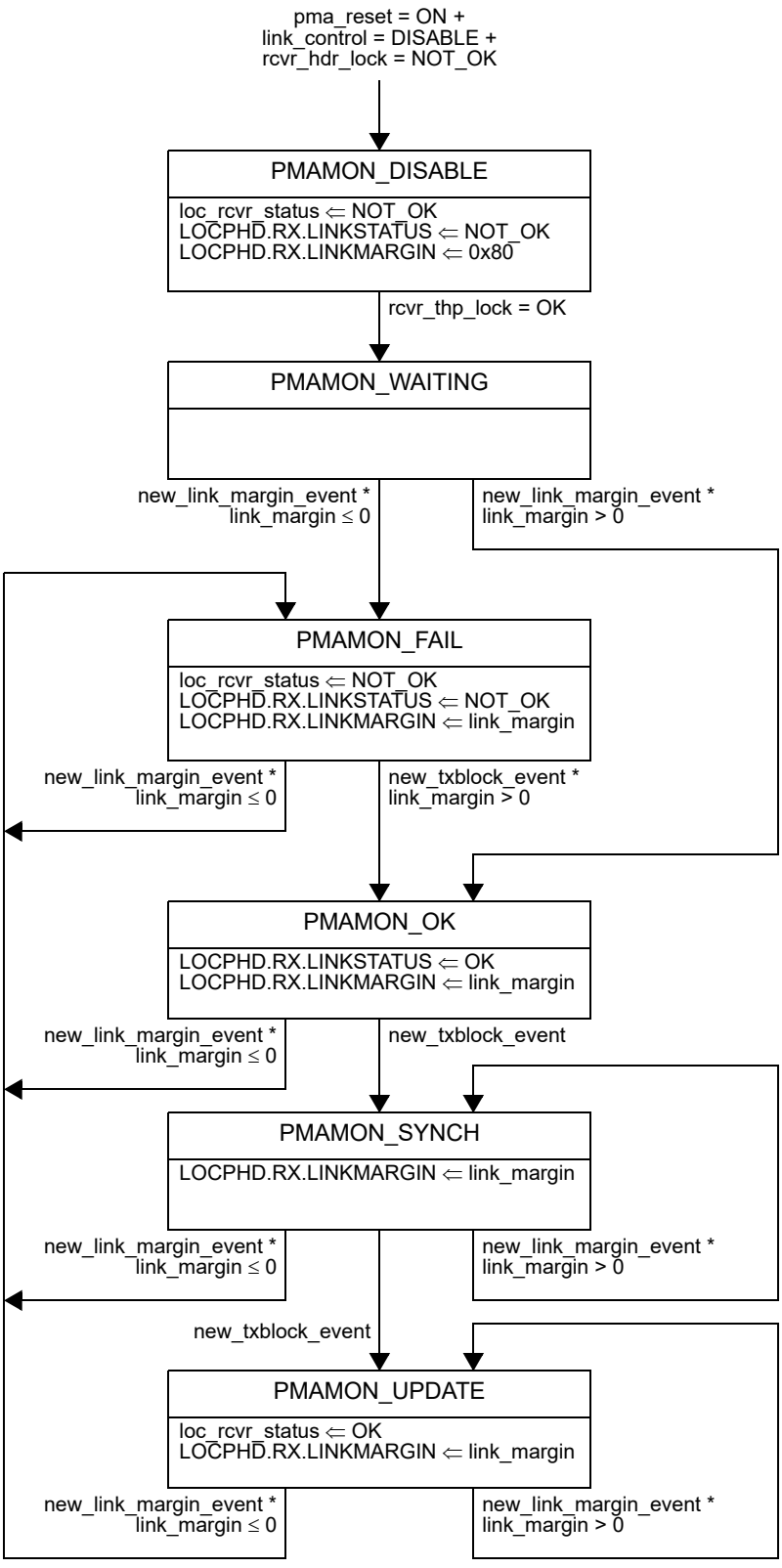

Figure 115–30—PHY quality monitor state diagram

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115.3.8 Fixed-point format formal definition

The notation (m, n) is used to represent an m-bit binary word, which is to be interpreted as a signed twos complement fixed-point rational, where n is the number of bits used to represent the integer part (sign bit included) and (m – n) bits are used to represent the fractional part. Given an m-bit binary word, it is assumed that $1 \leq n \leq m$.

Any 1000BASE-H compliant PHY shall conform to the fixed-point encoding and the fixed-point decoding provided by the codes in 115.3.8.1 and 115.3.8.2, respectively, for the fixed-point representation of Clause 45 registers and PHD fields (see 115.3.4).[199, 200]

115.3.8.1 Fixed-point encoding

```
% Parameters:
%      fdata: Row data vector in floating-point format
%      m    : Word length # of bits
%      n    : Integer part # of bits, including sign
%      rdata: Fixed-point format data vector

function rdata = float2fix(fdata, m, n)
  bdata = round(fdata*2^(m-n));
  bdata = min(bdata, 2^(m-1) - 1);
  bdata = max(bdata, -2^(m-1));
  idx_n = find(bdata < 0);
  rdata = bdata;
  rdata(idx_n) = 2^m + rdata(idx_n);
  rdata = bitand(rdata, 2^m - 1);
end
```

115.3.8.2 Fixed-point decoding

```
% Parameters:
%      rdata: Row data vector in fixed-point format
%      m    : Word length # of bits
%      n    : Integer part # of bits, including sign
%      fdata: Floating-point format data vector

function fdata = fix2float(rdata, m, n)
  % Sign extension
  bdata = bitand(rdata, 2^m - 1);
  idx_n = find(bitand(bdata, 2^(m-1)) ~= 0);
  bdata(idx_n) = bdata(idx_n) - 2^m;

  % Fix to float conversion
  fdata = bdata / (2^(m - n));
end
```

115.4 Energy-Efficient Ethernet (EEE)

Each PHY shall advertise its EEE ability to the link partner in the field PHD.CAP.LPI (see Table 115–6). PHD.CAP.LPI = 1 advertisement indicates to the link partner that the local PHY can generate Transmit Blocks as specified for the LPI mode of operation, it is able to accept Transmit Blocks from the link partner that conform to LPI operation (see 45.2.3.54.15), and that EEE is enabled (see 45.2.3.53.4).

EEE shall be operational only when both link partners indicate PHD.CAP.LPI = 1. If either link partner PHY does not advertise EEE ability (PHD.CAP.LPI = 0), then the link operates in normal mode in both

[199]This code is written in the MATLAB programming language (see 1.3); however, use of this language does not indicate an endorsement of MATLAB by IEEE and, as such, any tool can be used to perform this calculation.

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transmit and receive directions even if "Assert LPI" encoding is detected on the GMII. When two link partners do not agree on enabling EEE capability, the PCS encoding transparently carries the LPI signaling GMII to GMII, but the PHY does not enter LPI mode.

As shown in Figure 115–31, 1000BASE-H LPI mode consists of alternating refresh and quiet periods. Refresh is provided by transmitting all the pilot S1, pilot $S2_x$, and PHS_x sub-blocks; and quiet is provided by suspending transmission of the payload data sub-blocks. In quiet periods, the local PHY may turn off much of the PCS, PMA, and PMD transmitter. No optical power is injected into the fiber during these periods of quiet resulting in reduced power consumption. LPI mode is only entered or exited aligned to the beginning of a payload data sub-block.

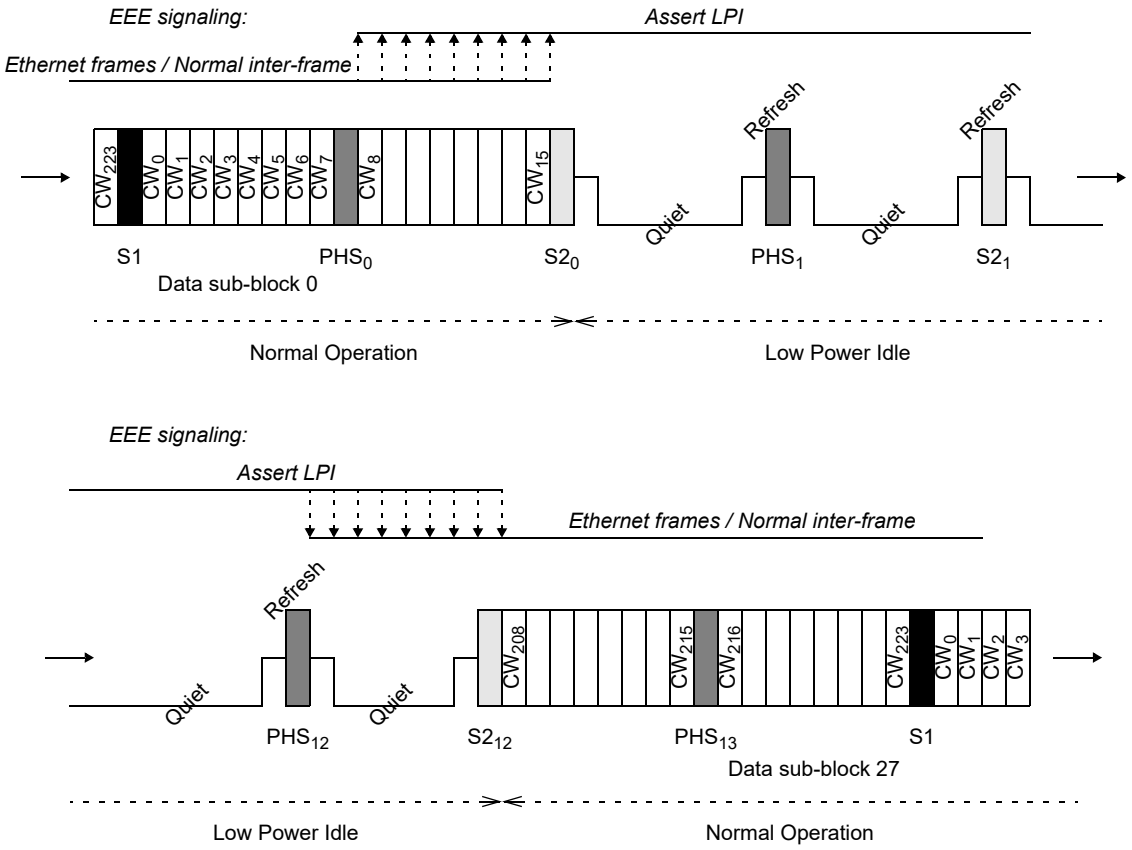

Figure 115–31— LPI operation

Pilot and PHS_x sub-blocks serve as refresh signals allowing the receiver to update adaptive filters and timing circuits in order to maintain link integrity. These sub-blocks are generated as in normal mode (see 115.2.1).

The PHY receiver detects if its link partner is operating in LPI mode based on the received signal at the beginning of each payload data sub-block. The PHY transmitter indicates to its link partner that it is entering a quiet period by the transmission of 130 contiguous zero value symbols. These follow the normal 16 zero postfix of the pilot or PHS_x sub-block. The extra zero symbols are used by the remote PHY receiver to detect that a quiet period follows, allowing the PMD receive function to save the state of circuitry and switch off the optical signal translation before the optical power is switched off at the transmitter. The transmitter then enters its quiet state until 130 symbol times before the end of the payload data sub-block, where the transmitter inserts 130 zero value symbols before the transmission of the pilot or PHS_x sub-block. This allows the link partner to prepare for reception of the sub-block that acts as a refresh signal.

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115.4.1 LPI mode transmit operation

The transmit operation of a 1000BASE-H compliant PHY in LPI mode produces alternating quiet and refresh periods as shown in Figure 115–31. LPI operating mode shall only be entered once the link has been established (link_status = OK). When an "Assert LPI" transfer occurs on the GMII, the local PCS encodes the "Assert LPI" signal into a PDB as defined in Table 115–2.

The PHY transmitter shall enter LPI mode at the beginning of the next payload data sub-block, once a PDB that contains an encoded "Assert LPI" has been completely transmitted to its link partner, unless the GMII signals normal inter-frame before the end of the current payload data sub-block.

The PHY transmitter shall be enabled periodically to transmit pilot and PHS_x sub-blocks (refresh signals) at the same time as they would be transmitted in normal operating mode.

During LPI mode, the transmitter shall replace any payload data sub-block with the following:

a) Transmission of 130 zero symbols, to indicate entry to quiet (pcspma_tx = ON, see 115.4.3)
b) No output optical power during 7644 symbols (quiet, pcspma_tx = OFF)
c) Transmission of 130 zero symbols, to prepare the remote receiver for pilot and PHS_x sub-blocks used as refresh signals (pcspma_tx = ON)

The PHY transmitter shall exit LPI mode and resume normal operation at the start of the next payload data sub-block after the reception of normal inter-frame transfers on the GMII.

The 64B/65B encoder shall preserve timing during quiet mode. The time alignment of transmitted PDBs relative to FEC codewords when the PHY re-enters normal operation is the same as it would have been in the absence of LPI mode. This preserves the PCS decoder synchronization of the link partner and coherence with information encoded in the field PHD.TX.NEXT.PDB.OFFSET.

The payload data binary scrambler of 115.2.4.2, and the payload data symbol scrambler of 115.2.4.4 shall preserve timing during quiet mode. When the PHY re-enters normal operation, the scramblers values are the same as they would have been in the absence of LPI mode.

Unlike some other EEE PHYs, neither sleep nor wake specific signals are used to enter and leave the LPI mode of operation. Instead, sleep is indicated to the link partner by the transmission of 130 zero symbols that replace the beginning of a payload data sub-block. Wake is implicit in the presence of normal PAM16 Tomlinson-Harashima precoded signal at the beginning of a payload data sub-block.

115.4.2 LPI mode receive operation

The receive operation of a 1000BASE-H compliant PHY in LPI mode processes alternating quiet and refresh periods as shown in Figure 115–31.

The PHY receiver shall enter LPI mode upon detection of a sequence of zero symbols instead of PAM16-THP signal at the beginning of a payload data sub-block, consequently encoding "Assert LPI" in GMII transfers. Some receive functionality may be disabled to reduce power consumption.

NOTE—"Assert LPI" can also be encoded on the GMII receive stream due to the reception of PDBs containing LPI signaling from the link partner (this, for example, is the case of LPI assertion on the GMII transmit stream in the middle of a payload data sub-block transmission).

In LPI mode, the PHY receiver can use received pilot S1, pilot $S2_x$, and PHS_x sub-blocks, periodically sent by the link partner, to update adaptive coefficients and timing circuits and to determine the values of state variables loc_rcvr_status and link_margin.

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The PHY receiver shall exit the LPI mode upon detection of PAM16-THP signal at the beginning of a payload data sub-block, returning to normal operation and sending the received payload to the GMII. The 64B/65B decoder shall resume normal operation after LPI mode, starting aligned to the boundary of the first complete PDB received from the beginning of the payload data sub-block. At this PDB, the local PHY begins to send normal inter-frame encoding on the GMII, since this is the initial information received from the remote PHY and the link returns the nominal operational mode.

115.4.3 PMD power control state variables

The following defines all the variables used in PMD power control state diagrams that have not been previously introduced:

lpi_cap
: Controls LPI functionality.
Values: TRUE: Both local and remote PHY have EEE ability and EEE functionality is enabled in both PHYs
FALSE: Either local or remote PHY do not have EEE ability or it is disabled

pcspma_tx
: State variable that indicates the symbols transmission from PMA.
Values: ON: Enable PCS and PMA transmit (during normal operation or LPI refresh periods)
OFF: Disable PCS and PMA transmit (LPI quiet periods)

pcspma_rx
: State variable that indicates the symbols reception by PMA.
Values: ON: Enable PCS and PMA receive (during normal operation or LPI refresh periods)
OFF: Disable PCS and PMA receive (LPI quiet periods)

rx_pwr
: Controls the PMD receive function.
Values: ON: The PMD receive function receives signal at MDI and transfer to the PMA receiver
OFF: The PMD receive function ignores signal at the MDI, saves the internal state of the circuitry, and may reduce power consumption

sd_inh
: Indicates to the PMD signal detect function to be, or not, inhibited.
Values: TRUE: The PMD signal detect function is inhibited
FALSE: The PMD signal detect function operates normally

tx_pwr
: Controls the PMD transmitter.
Values: ON: The PMD generates signal at the MDI
OFF: The PMD does not generate signal at the MDI, and may reduce power consumption

115.4.4 PMD power control state diagrams

Power control of PMD transmit function via tx_pwr shall conform to the PMD TX power control state diagram in Figure 115–32. Power control of PMD receive function via rx_pwr and sd_inh shall conform to the PMD RX power control state diagram in Figure 115–33.

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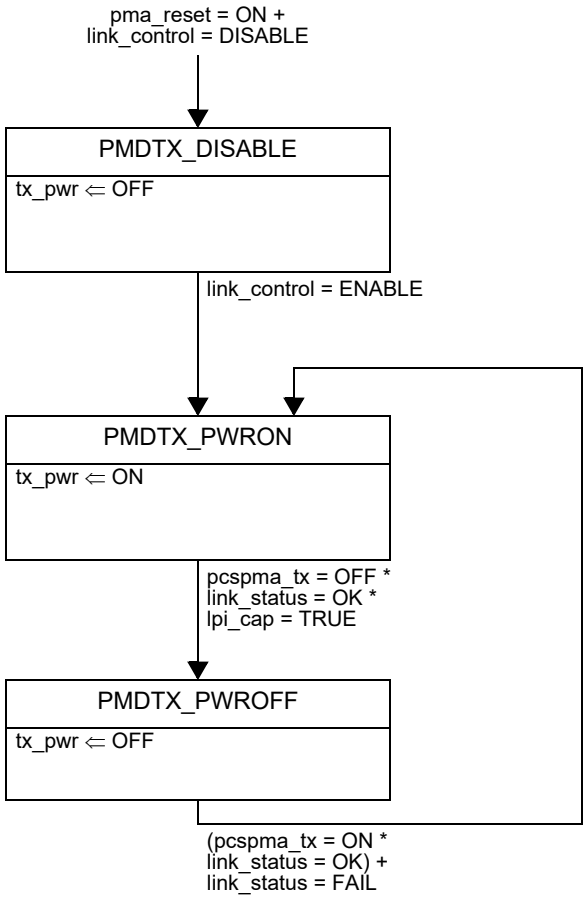

Figure 115–32—PMD TX power control state diagram

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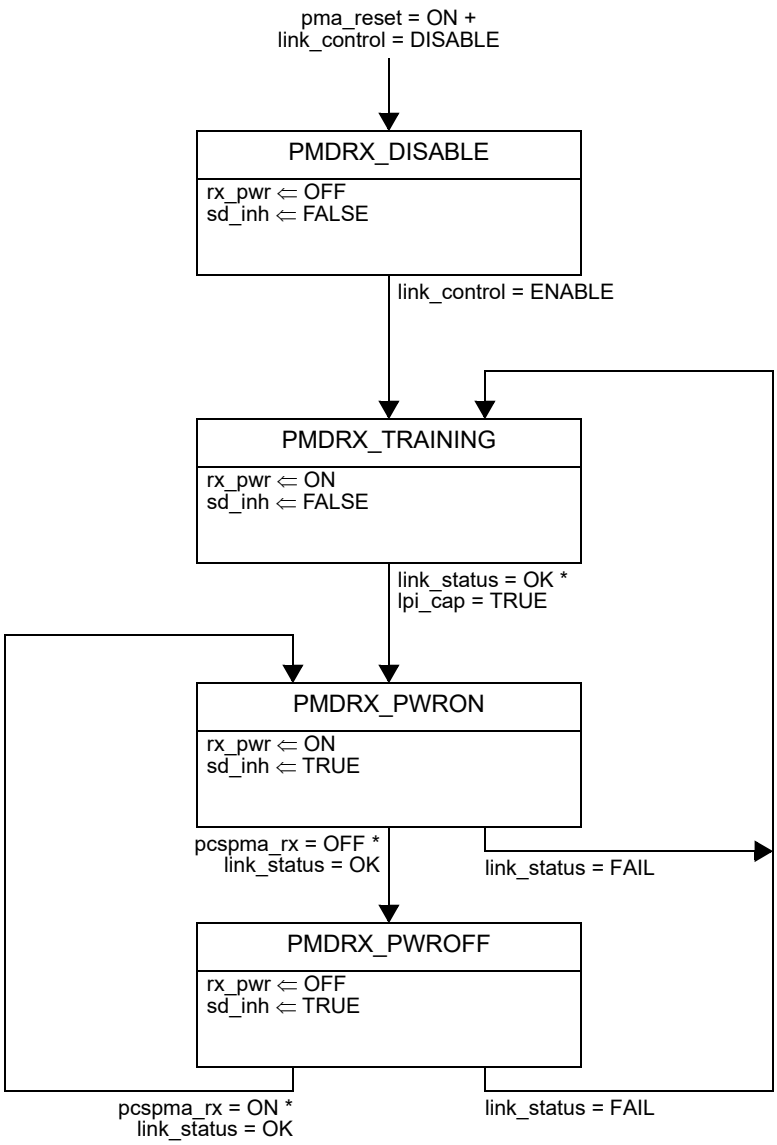

Figure 115–33—PMD RX power control state diagram

115.5 Test modes

The test mode 1 through test mode 6 shall be provided to allow PMD optical measurement requirements defined in 115.6.4 and BER testing.

These test modes shall be configured by setting the 1000BASE-H PCS control register, operation mode bits defined in 45.2.3.53. The test modes only change the symbols provided to the transmitter circuitry and do not alter the optical and jitter characteristics at the MDI from those of normal (non-test mode) operation.

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115.5.1 Test mode 1

Test mode 1 is for measurement of the bit error ratio (BER) of the link including the PCS, PMA, and PMD sublayers of two PHYs in the 1000BASE-H set and a fiber optic cable connected to them. This mode reuses the normal (non-test) mode with a zero data stream.

Operating in this test mode, the PHY shall configure the PCS transmitter to input an all zeros bit stream to the binary scrambler and ignore GMII. In the absence of errors, a zero data sequence is expected after the receiver binary descrambler. Any non-zero data bit received shall be counted as an error to be computed in the BER. The 64B/65B encoder is not used when the PCS transmitter is configured in test mode 1.

PMA and PMD functions shall operate as in normal mode (non-test) establishing the bidirectional link independent of the special configuration of the binary scrambler in PCS.

The PHY shall announce to the link partner the test mode 1 using the field PHD.TX.NEXT.MODE (see 115.3.4). The operating mode of the transmitter encoded in the field PHD.TX.NEXT.MODE is selected at PMA reset, and does not change value unless a PMA reset takes place. The receiver shall reconfigure its circuitry to support the signaled operating mode, for normal operation (the 64B/65B decoder is connected to the binary descrambler), or for BER test (a counter connected to the binary descrambler).

115.5.2 Test mode 2

When test mode 2 is enabled, the PMA shall transmit one {+1} symbol followed by one {–1} symbol continually with the transmitted symbols timed from its local symbol clock. The resulting transmitter output signal is a 162.5 MHz square wave.

115.5.3 Test mode 3

When test mode 3 is enabled, the PMA shall transmit 10 {+1} symbols followed by 10 {–1} symbols continually with the transmitted symbols timed from its local symbol clock. The transmitter output is a 16.25 MHz square wave.

115.5.4 Test mode 4

For test mode 4 definition, let $q1$ be the sub-sequence composed by 20 {+1} symbols followed by 10 {–1} symbols, and $q2$ the sub-sequence composed by 10 {+1} symbols followed by 20 {–1} symbols. When test mode 4 is enabled, the PMA shall transmit a sequence composed by 250 times the sub-sequence $q1$ followed by 250 times the sub-sequence $q2$ continually, being the transmitted symbols timed from its local symbol clock.

115.5.5 Test mode 5

When test mode 5 is enabled, the PMA shall continually transmit {0} symbols timed from its local symbol clock. The transmitter output is a dc signal.

115.5.6 Test mode 6

When test mode 6 is enabled, the PMA shall transmit the sequence of symbols s_n generated by the scrambler generator polynomials per Equation (115–25) and Equation (115–26).

$$g_0(x) = 1 + x^9 + x^{11} \quad (115–25)$$

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$$g_1(x) = 1 + x^7 + x^9 + x^{10} + x^{11} \quad (115–26)$$

The two maximum-length shift registers used to generate the sequences defined by these polynomials shall be updated once per symbol interval (nominally 1000/325 ns). The reset value of both shift registers shall be 0x7FF, so the content of both registers start aligned to all ones when the PHY is configured to generate the test mode 6 pattern.

The bits stored in the shift register at a particular time n are denoted $Scr0_n[10:0]$ for the scrambler defined per Equation (115–25). At each symbol period this shift register is advanced by one bit and one new bit represented by $Scr0_n[0]$ is generated. Bits $Scr0_n[10]$ and $Scr0_n[8]$ are exclusive OR'd together to generate the next $Scr0_n[0]$ bit.

The bits stored in the shift register at a particular time n are denoted $Scr1_n[10:0]$ for the scrambler defined per Equation (115–26). At each symbol period this shift register is advanced by one bit and one new bit represented by $Scr1_n[0]$ is generated. Bits $Scr1_n[10]$, $Scr1_n[9]$, $Scr1_n[8]$, and $Scr1_n[6]$ are exclusive OR'd together to generate the next $Scr1_n[0]$ bit.

The bit sequences $x00_n$, $x01_n$, $x02_n$, and $x03_n$ generated from combinations of bits of the two scramblers shall be used to generate the PAM16 symbols, $y0_n$, according to Equation (115–27).

$$\begin{aligned} x00_n &= Scr1_n[0] \\ x01_n &= Scr1_n[1] \wedge Scr0_n[4] \\ x02_n &= Scr1_n[2] \wedge Scr0_n[9] \\ x03_n &= Scr1_n[0] \wedge Scr0_n[10] \\ y0_n &= x00_n + 2 \times x01_n + 4 \times x02_n + 8 \times x03_n \end{aligned} \quad (115–27)$$

The bit sequences $x10_n$, $x11_n$, $x12_n$, and $x13_n$ generated from combinations of bits of the two scramblers shall be used to generate the PAM16 symbols, $y1_n$, according to Equation (115–28).

$$\begin{aligned} x10_n &= Scr0_n[0] \\ x11_n &= Scr0_n[1] \wedge Scr1_n[4] \\ x12_n &= Scr0_n[2] \wedge Scr1_n[9] \\ x13_n &= Scr0_n[0] \wedge Scr1_n[10] \\ y1_n &= x10_n + 2 \times x11_n + 4 \times x12_n + 8 \times x13_n \end{aligned} \quad (115–28)$$

From $y0_n$ and $y1_n$, the PAM256 symbols s_n shall be generated according to Equation (115–29). The transmitter shall time the transmit symbols s_n from its local symbol clock.

$$s_n = \frac{1}{256}(2 \times (16 \times y0_n + y1_n) - 255) \quad (115–29)$$

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115.6 Physical Medium Dependent (PMD) sublayer

115.6.1 PMD service interface

The following specifies the services provided by a PMD connected to 1000BASE-H. The PMD sublayer service interface is described in an abstract manner and does not imply any particular implementation.

The PMD service interface supports the exchange of analog signals between PMA and PMD sublayers. The PMD translates the transmit and receive PMA signals to and from optical signals suitable for the specified medium.

The following primitives are defined:

PMD_COMSIGNAL.request
PMD_COMSIGNAL.indication
PMD_TXPWR.request
PMD_RXPWR.request
PMD_RXDETECT.indication
PMD_SDINH.request

115.6.1.1 PMD_COMSIGNAL.request

This primitive defines the transfer of an analog signal amplitude from the PMA to the PMD.

115.6.1.1.1 Semantics of the primitive

PMD_COMSIGNAL.request(tx_signal)

During transmission, this primitive conveys to the PMD via the parameter tx_signal, the amplitude of the output signal to be produced by the PMD transmit function.

115.6.1.1.2 When generated

The PMA generates PMD_COMSIGNAL.request(tx_signal) synchronously with every transmit clock cycle.

115.6.1.1.3 Effect of receipt

Upon receipt of this primitive the PMD converts tx_signal into the MDI optical signal (see 115.6.2.2).

115.6.1.2 PMD_COMSIGNAL.indication

This primitive defines the transfer of an analog signal amplitude from the PMD to the PMA.

115.6.1.2.1 Semantics of the primitive

PMD_COMSIGNAL.indication(rx_signal)

This primitive conveys to the PMA via the parameter rx_signal the relative amplitude of the optical signal received by the PMD at the MDI (see 115.6.2.3).

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115.6.1.2.2 When generated

The PMD_COMSIGNAL.indication(rx_signal) is continuously generated by the PMD in the form of an analog signal.

115.6.1.2.3 Effect of receipt

Upon receipt of this primitive the PMA performs clock recovery for correct time sampling of received symbols and adaptive channel equalization (see 115.3.2).

115.6.1.3 PMD_TXPWR.request

This primitive is used for optional EEE capability. The primitive is generated to request no optical output power during quiet periods of LPI mode, or to request optical signal being generated at the MDI during refresh periods of LPI mode or for normal operation of the PHY transmitter.

115.6.1.3.1 Semantics of the primitive

PMD_TXPWR.request(tx_pwr)

The tx_pwr parameter can take one of the two values: ON or OFF.

ON: The PMD transmit function generates signals at the MDI.

OFF: The PMD transmit function does not generate signal at the MDI.

115.6.1.3.2 When generated

The PMD_TXPWR.request(tx_pwr) is generated by the PMA transmitter whenever the value of tx_pwr changes as specified by the state diagram of Figure 115–32 (see 115.4.4).

115.6.1.3.3 Effect of receipt

PMD_TXPWR.request(OFF) requests the PMD transmit function to produce no optical output power, and PMD_COMSIGNAL.request(tx_signal) is ignored.

PMD_TXPWR.request(ON) requests the PMD transmit function to respond to PMD_COMSIGNAL.request(tx_signal) with generation of normal optical output.

115.6.1.4 PMD_RXPWR.request

This primitive is used for optional EEE capability. It is generated to request the PMD receive function to transition between being able to respond to received optical signals and a minimum power consumption state.

115.6.1.4.1 Semantics of the primitive

PMD_RXPWR.request(rx_pwr)

The rx_pwr parameter can take one of two values: ON or OFF.

ON: The PMD receive function responds to the received MDI optical signal.

OFF: The PMD receive function ignores the received MDI optical signal.

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115.6.1.4.2 When generated

The PMD_RXPWR.request(rx_pwr) is generated by the PMA receiver whenever the value of rx_pwr changes as specified by the state diagram of Figure 115–33 (see 115.4.4).

115.6.1.4.3 Effect of receipt

PMD_RXPWR.request(OFF) requests the PMD receive function to ignore the received MDI signal and reduce power consumption.

PMD_RXPWR.request(ON) requests the PMD receive function to respond to the received MDI signal.

115.6.1.5 PMD_RXDETECT.indication

This primitive is generated by the PMD signal detect function to indicate the status of the receive optical signal from the MDI as specified in 115.6.2.4.

115.6.1.5.1 Semantics of the primitive

PMD_RXDETECT.indication(signal_detect)

The signal_detect parameter can take one of two values: OK or FAIL, indicating whether the PMD is detecting average optical power over a threshold (see 115.6.2.4) at the receiver (OK) or not (FAIL). When signal_detect = FAIL, then the rx_signal is undefined.

NOTE—signal_detect = OK does not guarantee that rx_signal provides high enough quality to allow the PHY to establish the link. It just indicates that average optical power present at the MDI exceeds a threshold. A signal_detect = OK indication with sufficient average optical power allows the PHY partners to start establishing the link and still not meet the BFER objective (see 115.3.7.1), then the PHY indicates link_status = FAIL.

115.6.1.5.2 When generated

The PMD signal detect function generates this primitive to indicate a change in the value of signal_detect.

115.6.1.5.3 Effect of receipt

PMD_RXDETECT.indication(OK) indicates that the PMD receive function is able to respond to PMD_RXPWR.request primitives (that request the PMD receive function to respond or not to the MDI signal). PMD_RXDETECT.indication(OK) also indicates to the PMA receive function that optical signal is being received from the MDI and that the link may be established with a link partner. PMD_RXDETECT.indication(OK) may be used to wake up from deep sleep in a system that includes a 1000BASE-RHx PHY.

PMD_RXDETECT.indication(FAIL) indicates the PMD receive function is not responding to the received MDI signal. PMD_RXDETECT.indication(FAIL) also indicates to the PMA receive function that optical signal is not being received so link establishment cannot be initiated. PMD_RXDETECT.indication(FAIL) may be used to transition a system that includes a 1000BASE-RHx PHY into deep sleep.

115.6.1.6 PMD_SDINH.request

This primitive supports EEE operation and is generated to request enable or inhibit of the PMD signal detect function.

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115.6.1.6.1 Semantics of the primitive

PMD_SDINH.request(sd_inh)

The sd_inh parameter can take one of the two values: TRUE or FALSE.

TRUE: The PMD signal detect function is inhibited.

FALSE: The PMD signal detect function responds to the received MDI optical signal.

115.6.1.6.2 When generated

The PMD_SDINH.request(sd_inh) is generated by the PMA receiver whenever the value of sd_inh changes as specified by the state diagram of Figure 115–33 (see 115.4.4).

115.6.1.6.3 Effect of receipt

PMD_SDINH.request(FALSE) requests normal PMD signal detect operation.

PMD_SDINH.request(TRUE) requests the PMD signal detect function to inhibit processing of the received optical signal. This keeps PMD_RXDETECT.indication(signal_detect) = OK, independently of optical signal level received at MDI.

115.6.2 PMD functional specifications

115.6.2.1 PMD block diagram

For purpose of system conformance, the PMD sublayer is defined at the following points, depicted in Figure 115–34. The optical transmit signal is defined at the output end of 1 meter of plastic optical fiber consistent with the link segment type connected to the MDI. All the specified transmitter measurements are made at TP2. The optical receive signals are specified and measured at the output of the fiber optic cabling (TP3), which in a link segment is connected to the receiver.

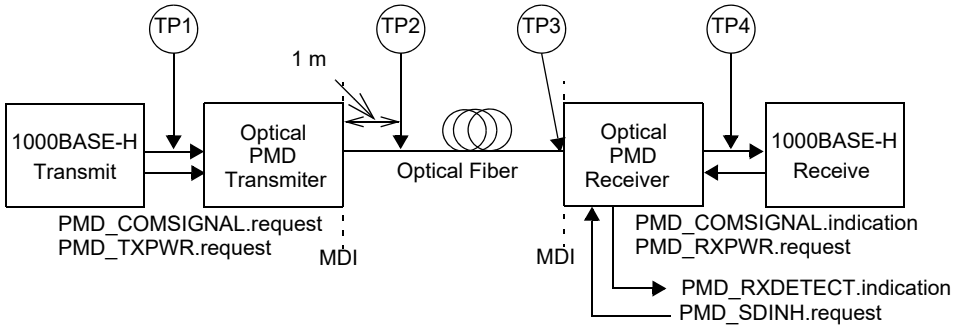

Figure 115–34—1000BASE-RHx PHY block diagram

TP1 and TP4 are standardized reference points for use by implementers to certify component conformance. The specifications of the PMD service interface (TP1 and TP4) are not system compliance points of this standard (these are not readily testable in a system implementation).

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115.6.2.2 PMD transmit function

The PMD transmit function translates abstract PMD service primitives into optical signals. The transmit signal characteristics at the MDI are specified in 115.6.3.1.

The PMD transmit function shall translate the amplitude parameter tx_signal (see 115.6.1.1) into optical signal p at TP2 according to the following function:

$$p = \frac{P_1 - P_0}{2} \times \text{tx\_signal} + \frac{P_1 + P_0}{2} \tag{115–30}$$

where P_0 and P_1 are respectively the minimum and maximum optical power at TP2, and the parameter tx_signal fits $-1 \leq \text{tx\_signal} < +1$ (see 115.3.3.1).

According to Equation (115–30), the maximum amplitude of tx_signal is translated into the highest optical power (P_1) at TP2 and the minimum amplitude of tx_signal is translated into the lowest optical power (P_0) at TP2.

Optionally, the PMD transmit function shall turn on and turn off the optical output as required by the PMD_TXPWR.request primitive. The transition times from receipt of this primitive until it takes effect at the MDI are specified in 115.6.3.1.

115.6.2.3 PMD receive function

The PMD receive function shall translate the optical signal received at the MDI into the analog signal amplitude provided by the abstract PMD_COMSIGNAL.indication(rx_signal) primitive. The receive signal at the MDI is specified in 115.6.3.3.

Optionally, the PMD receive function responds to or ignores the receive MDI signal during optional LPI mode, as requested by the PMD_RXPWR.request primitive.

PMD_RXPWR.request(OFF) shall cause the PMD receive function to save the internal state of the circuitry to not be affected by the received optical signal during quiet periods of LPI mode. The PMD receive function ignores the received MDI signal and may reduce its power consumption. The PMD receive function saves state to be able to quickly restart translation of received MDI signal during the LPI mode refresh periods or when normal operation is resumed.

The PMD receive function shall respond to the MDI optical signal in response to receiving a PMD_RXPWR.request(ON). This allows the PMD to process the refresh signals in LPI mode and when normal operation of the PHY is resumed. The transition times from receipt of a PMD_RXPWR.request primitive until it takes effect in the PMD receive function are specified in 115.6.3.3.

115.6.2.4 PMD signal detect function

The PMD signal detect function determines the value of the signal_detect parameter of the PMD_RXDETECT.indication primitive, which is signaled when the value of signal_detect changes.

The value of the signal_detect parameter shall be generated in response to the average optical power present at the MDI and the sd_inh parameter according to the conditions defined in Table 115–7. The PMD receive function is not required to verify whether a compliant 1000BASE-H signal is being received. This standard imposes no response time requirements on the generation of the signal_detect parameter.

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Table 115–7—Signal detect value definitions

sd_inh	Receive conditions	Signal detect value
FALSE	AOP at TP3 < –35 dBm	FAIL
FALSE	AOP at TP3 > –29 dBm	OK
FALSE	–35 dBm < AOP at TP3 < –29 dBm	Unspecified (uncertainty range)
TRUE	Any value of AOP at TP3	OK

115.6.3 PMD to MDI optical specifications

Different PMD to MDI optical specifications are provided for the three port types 1000BASE-RHA, 1000BASE-RHB, and 1000BASE-RHC.

1000BASE-RHA and 1000BASE-RHB PHYs have to be able to operate in a fiber optic channel type I. A 1000BASE-RHC PHY has to be able to operate in the fiber optic channel type II and type III. Fiber optic channel type I, type II, and type III are defined in 115.7.

115.6.3.1 Transmitter optical specifications

A 1000BASE-RHx transmitter shall meet the specifications at TP2 defined in Table 115–8 and the modal power distribution (MPD) shall be higher than the lower bound limits defined in Table 115–9 per measurement techniques defined in 115.6.4. Specification for transmit MPD is illustrated in Figure 115–35 and the measurement method is provided in 115.6.4.11.

Table 115–8—Transmit optical characteristics (RHA, RHB, and RHC)

Parameter	Symbol	Units	Value/Criteria					
			Min			Max		
			RHA	RHB	RHC	RHA	RHB	RHC
Average optical power	AOP	dBm	–6	–7	–9	1		
Average optical power of OFF transmitter	AOP_{OFF}	dBm	—			–35		
Optical return loss tolerance	ORLT	dB	—			14		
Extinction ratio	ER	dB	11			15		
Center wavelength	λ_c	nm	635			665		
Spectral width	λ_w	nm	—			20		
Rise time (10% – 90%)	t_r	ns	—			3		
Fall time (90% – 10%)	t_f	ns	—			3		
Rising-edge overshoot	OS_{rise}	%	0			20		
Falling-edge overshoot	OS_{fall}	%	0			$\frac{100}{10^{ER/10}-1}$ [a]		
Positive output droop	DO^+	dB	0			0.8		

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Table 115–8—Transmit optical characteristics (RHA, RHB, and RHC) *(continued)*

Parameter	Symbol	Units	Value/Criteria					
			Min			Max		
			RHA	RHB	RHC	RHA	RHB	RHC
Negative output droop	DO^{-}	dB	–0.7			0		
Timing jitter	t_J	ps	—			10		
2nd order harmonic distortion	HD_2	dB	—			–20		
3rd order harmonic distortion	HD_3	dB	—			–23		
4th order harmonic distortion	HD_4	dB	—			–34		
Residual distortion	RD	dB	—			–40		
Relative intensity noise	RIN	dB/Hz	—			–134		
Off transition time (from tx_pwr = OFF to AOP_{OFF})	t_{off}	ns	—			100		
On transition time (from tx_pwr = ON to active operation)	t_{on}	ns	—			1500		

[a]Maximum permitted falling-edge overshoot depends on the actual transmit ER. The equation gives the maximum permitted falling-edge overshoot as a function of the actual ER (dB).

Table 115–9—Transmit MPD lower bound limits per EAF (RHA, RHB, and RHC)

Angle (°)	EAF	Angle (°)	EAF	Angle (°)	EAF
0.0	0.00	10.0	0.41	27.5	0.97
1.0	0.00	15.0	0.70	30.0	0.99
2.5	0.03	20.0	0.83	35.0	1.00
5.0	0.11	22.5	0.89		
7.5	0.24	25.0	0.93		

Average optical power depends on the operation mode of the PHY transmitter (normal or LPI). AOP is defined as the average optical power at TP2 when the PMD transmit function receives primitive PMD_TXPWR.request(ON) (normal operation and LPI refresh signals). AOP_{OFF} corresponds to the optical power when the PMD transmit function receives the primitive PMD_TXPWR.request(OFF) (LPI quiet periods or link_control = DISABLE). The AOP_{OFF} maximum value is compatible with the PMD signal detect function specified in 115.6.2.4.

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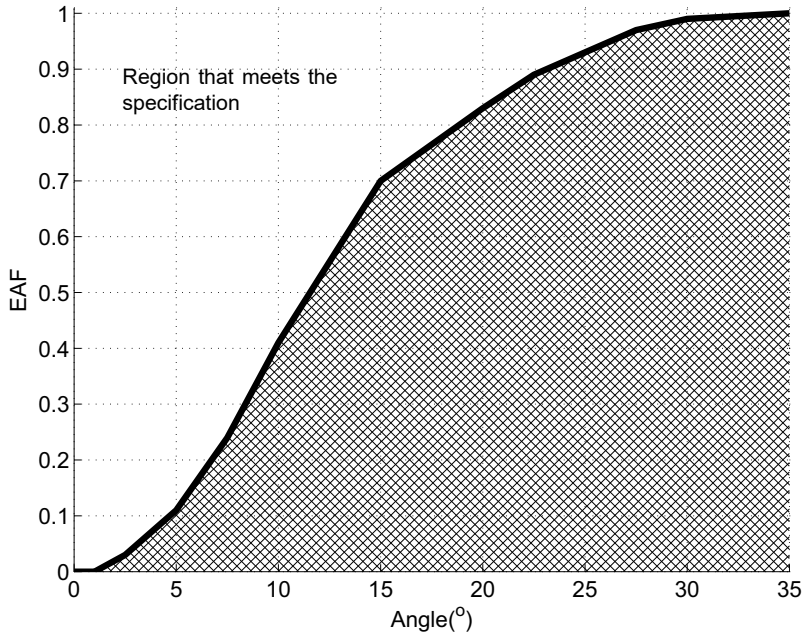

Figure 115–35—Illustration of the transmit MPD lower bound limits per EAF of Table 115–9

115.6.3.2 Transmit clock frequency

The symbol transmission rate of the PHY shall be 325.00 MBd ± 0.01%.

115.6.3.3 Receiver optical specifications

A 1000BASE-RHx receiver shall meet the specifications at TP3 defined in Table 115–10 per measurement techniques defined in 115.6.4. Each 1000BASE-RHx PHY is specified for one or two of three specified fiber optic channels (type I, type II, or type III).

A 1000BASE-RHx PHY shall be able to establish a reliable link per the specification in 115.3.7.1 throughout the average optical power (AOP) range between the minimum and maximum limit defined in Table 115–10, for signals received at the MDI that were transmitted from a remote transmitter within the specifications of 115.6.3.1, and have passed through a fiber optic channel specified in 115.7. Under these conditions, a 1000BASE-RHx PHY shall provide a BER less than 10^{-12} operating in test mode 1 (see 115.5.1), and a frame error ratio less than 1.1×10^{-10} for continuous transmission of 64-octet Ethernet frames transmitted with minimum IPG at GMII interface operating in normal (non-test) mode. These specifications apply to a complete 1000BASE-RHx link composed by two interconnected partners with their respective PCS, PMA, and PMD sublayers.

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Table 115–10—Receive optical characteristics (RHA, RHB, and RHC)

Parameter	Symbol	Units	Value/Criteria							
			Min				Max			
			RHA	RHB	RHC		RHA	RHB	RHC	
			Fiber optic channel							
			Type I	Type I	Type II	Type III	Type I	Type I	Type II	Type III
Average optical power for reliable link establishment	AOP[a]	dBm	–17	–17	–17	–18.5	1			
Receiver reflectance	RR[b]	dB	—				–14			
Wavelength range	λ	nm	600				700			
Off transition time (from rx_pwr = OFF to quiet mode)	t_{off}	ns	—				200			
On transition time (from rx_pwr = ON to active operation)	t_{on}	ns	—				400			

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal that has a power level equal to the average receive optical power (max) plus at least 1 dB.
[b] See 1.4 for definition of reflectance.

115.6.3.4 Receiver boundary condition tests

The following boundary condition tests verify the receiver optical specifications defined in 115.6.3.3. A 1000BASE-RHx PHY shall be able to establish a reliable link as specified in 115.6.3.3 under boundary conditions defined in 115.6.3.4.1 and 115.6.3.4.2.

115.6.3.4.1 Receiver minimum AOP test

This test operates the 1000BASE-RHx PHY receiver in minimum AOP conditions as defined in Table 115–11. For this test, the responses of channel type I, type II, and type III are defined by the lower bound limits specified in Table 115–13, Table 115–14, and Table 115–15, respectively. Parameters of Table 115–8 and Table 115–10 that are not specified in Table 115–11 can take any value in the specification ranges.

115.6.3.4.2 Receiver maximum AOP test

This test operates a 1000BASE-RHx PHY receiver in maximum AOP conditions as defined in Table 115–12. The local receiver under test is connected to the remote transmitter by means of a plastic optical fiber of 1 meter or less consistent with the specifications of 115.7. Parameters of Table 115–8 and Table 115–10 that are not specified in Table 115–12 can take any value in the specification ranges.

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Table 115–11—Parameters for receiver minimum AOP test

Parameter		Symbol	Units	Value/Criteria			
				RHA	RHB	RHC	
				Fiber optic channel			
				Type I	Type I	Type II	Type III
Transmitter	Extinction ratio	ER	dB	11			
	Fall time (90% – 10%)	t_f	ns	3			
	Rising-edge overshoot	OS_{rise}	%	0			
	Falling-edge overshoot	OS_{fall}	%	0			
Receiver	Receive average optical power	AOP	dBm	–17	–17	–17	–18.5

Table 115–12—Parameters for receiver maximum AOP test

Parameter		Symbol	Units	Value/Criteria		
				RHA	RHB	RHC
Transmitter	Extinction ratio	ER	dB	15		
Receiver	Receive average optical power	AOP	dBm	1		
	Receiver reflectance	RR[a]	dB	–14		

[a]See 1.4 for definition of reflectance.

115.6.4 Optical measurement requirements

All the optical measurements of the transmitter shall be made at TP2 (at the end of a 1m length of POF cable consistent with the link segment type). The optical measurements for the receiver shall be made at TP3.

The transmitter testing methodology assumes that a 1000BASE-RHx PMD is not tested standalone, but is always considered as part of a complete Physical Layer device (i.e., PCS and PMA sublayers are also included). TP1 is not used as a stimulus point; rather, the complete PHY is instructed through management to generate signals that are measured at TP2.

115.6.4.1 Center wavelength measurement

The center wavelength shall meet the specifications according to IEC 61280-1-3, under normal (non-test) mode conditions using a valid 1000BASE-H transmit signal as specified in 115.3.3.1. For this measurement, the PHY is not connected to any link partner, therefore the bidirectional link cannot be established, MLCC codewords are not THP processed, and LPI mode is disabled.

115.6.4.2 Spectral width measurement

The spectral width (RMS) shall meet the specifications according to IEC 61280-1-3, using the same test conditions as for center wavelength measurement (see 115.6.4.1).

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115.6.4.3 Average Optical Power (AOP) measurement

The AOP shall meet the specifications at TP2 and TP3 measured with a large area photo-detector able to couple all the output optical power from the optical fiber, using the same test conditions as 115.6.4.1.

115.6.4.4 Transmitter rise and fall time measurements

The transmitter rise and fall time measurements shall meet the specifications according to the following measurements procedure, using an electrical oscilloscope after optical to electrical conversion or an optical oscilloscope with a minimum bandwidth of 812.5 MHz (–3 dB cut-off frequency):

a) The PHY is configured in test mode 3 (see 115.5.3).
b) Rise time is measured as the time taken for the optical signal to transition from value ($0.1 \times P_1 + 0.9 \times P_0$) to value ($0.1 \times P_0 + 0.9 \times P_1$) and stay above the second value.
c) Fall time is measured as the time taken for the optical signal to transition from value ($0.1 \times P_0 + 0.9 \times P_1$) to value ($0.1 \times P_1 + 0.9 \times P_0$) and stay below the second value.

P_1 is the steady-state value that the optical signal reaches after a rising-edge transition and before the next falling-edge. P_1 (mW) is the average optical power measured over a 2 ns window centered 15 ns after the rising-edge crossing of the optical signal with the average optical power (AOP) level. Similarly, P_0 is the steady-state value that the optical signal reaches after a falling-edge transition and before the next rising-edge. P_0 (mW) is the average optical power measured in a 2 ns window centered 15 ns after the falling-edge AOP crossing.

115.6.4.5 Transmitter extinction ratio (*ER*) measurement

The transmitter extinction ratio (*ER*) shall meet the specifications per Equation (115–31) calculated from the optical power measurements P_1 and P_0, which are defined and measured as specified in 115.6.4.4, using the same test setup, apparatus requirements, and PHY operation mode as 115.6.4.4.

$$ER = 10 \times \log_{10}\left(\frac{P_1}{P_0}\right) \text{ (dB)} \tag{115–31}$$

115.6.4.6 Transmitter overshoot measurements

The transmitter overshoot shall meet the specifications according to Equation (115–32) and Equation (115–33) for rising edge overshoot and falling edge overshoot, respectively, using the same test setup, apparatus requirements, and PHY operation mode as 115.6.4.4.

$$OS_{\text{rise}} = \frac{P_{\max} - P_1}{P_1 - P_0} \tag{115–32}$$

$$OS_{\text{fall}} = \frac{P_0 - P_{\min}}{P_1 - P_0} \tag{115–33}$$

$P_{\max}$ (mW) is the maximum measured value of the optical signal in the time interval between a rising-edge AOP crossing and next falling-edge AOP crossing. Similarly, $P_{\min}$ (mW) is the minimum measured value in the time interval between consecutive falling and rising edges. P_0 and P_1 are defined and measured as specified in 115.6.4.4.

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115.6.4.7 Transmitter output droop measurements

The transmitter output droop shall meet the specifications according to the following measurements steps, using the same test setup and apparatus requirements as 115.6.4.4:

a) A reference of extinction ratio, ER_0, is measured as specified in 115.6.4.5.
b) The PHY is configured in test mode 4 (see 115.5.4).
c) The maximum extinction ratio (ER_{max}) and the minimum extinction ratio (ER_{min}) are measured during a period of time of at least 47 μs (which assures sampling over more than a complete test mode 4 pattern). ER_{max} is calculated from the measured P_1 and P_0 values where the ratio between them is maximum. Similarly, ER_{min} is calculated from the measured P_1 and P_0 values, where the ratio between them is minimum. P_0 and P_1 are defined and measured as specified in 115.6.4.4.
d) The positive output droop DO^+ and the negative output droop DO^- are calculated as $DO^+ = ER_{max} - ER_0$ and $DO^- = ER_{min} - ER_0$, respectively.

115.6.4.8 Transmitter distortion measurement

The transmitter distortion is determined by the following four parameters:

a) Second order harmonic distortion (HD_2).
b) Third order harmonic distortion (HD_3).
c) Fourth order harmonic distortion (HD_4).
d) Residual distortion (RD).

These four parameters HD_2, HD_3, HD_4, and RD, shall meet the specifications according to the following procedure:

1) The PHY is configured in test mode 6 (see 115.5.6).
2) Transmitted waveform is captured at TP2 using the same test setup and apparatus requirements as 115.6.4.4 with data acquisition capabilities. To reduce frequency deviation between the transmitter and the clock used to sample the transmit waveform, the test instrument and the device under test may share the same clock reference.
3) A block of consecutive samples is processed with the code given below or an equivalent.[201, 202] The captured block of signal is at least 13 μs long and is sampled with the minimum sampling rate of 3.25 GSamples/s (10 times the transmit symbol rate of nominal 325 MBd). The code assumes the data acquisition clock is frequency locked to the DUT transmit clock.

```
% Post processing code for 1000BASE-RH transmitter distortion

% Read captured data file, min 13 us long, min 3.25GSample/sec,
% high resolution capture
fid  = fopen('RawData.bin', 'r');
xcap = fread(fid, inf, 'double');
fclose(fid);
xcap = reshape(xcap, 1, []);

% Set the over sampling ratio (min 10)
osr = 10;
[HD2 HD3 HD4 RD] = txdist(xcap,osr);
```

[201]This code is written in the MATLAB programming language (see 1.3); however, use of this language does not indicate an endorsement of MATLAB by IEEE and, as such, any tool can be used to perform this calculation.
[202]*Copyright release for MATLAB code:* Users of this standard may freely copy or reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

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```
% Results
fprintf('HD2: %.2f dB\n', HD2);
fprintf('HD3: %.2f dB\n', HD3);
fprintf('HD4: %.2f dB\n', HD4);
fprintf('RD:  %.2f dB\n', RD);


% TX distortion measurement
function [HD2 HD3 HD4 RD] = txdist(xcap, ov)
  % Compensate baseline
  xcap = xcap - mean(xcap);

  % Low-pass filter at 162.5 MHz
  [hb, ha] = butter(2, 1/ov, 'low');
  xcap = filter(hb, ha, xcap);

  % Reference test mode 6 signal
  tm6 = tm6gen();

  % Synchronization
  tm6_ov  = reshape(repmat(tm6, ov, 1), 1, []);
  xc      = filter(tm6_ov(end:-1:1), 1, [xcap zeros(1, length(tm6_ov))]);
  [mv mi] = max(abs(xc));
  dly     = mi - length(tm6_ov);
  xcap    = xcap(1+dly:end);
  xcap    = xcap(1:length(tm6_ov));

  % Decimation and clock phase recovery
  alpha = 0.7;

  min_ted = Inf;
  for i = 0:ov-1,
    xcap_dec = xcap(1+i:ov:end);
    len0     = min([length(xcap_dec) length(tm6)]);
    ted      = mean((1 - alpha)*xcap_dec(2:len0).*tm6(1:len0-1) - ...
                    alpha*xcap_dec(1:len0-1).*tm6(2:len0));

    if abs(ted) < min_ted
      min_ted = abs(ted);
      dly     = i;
    end
  end
  xcap_dec = xcap(1+dly:ov:end);

  % Normalize
  xcap_dec = xcap_dec/max(abs(xcap_dec));

  % Volterra estimation & analysis
  [HD2 HD3 HD4 RD] = volest(tm6, xcap_dec, 12, 3);
end


% Generate the reference test signal pattern for test mode 6
function tm6 = tm6gen()
  Ns = 2^11 - 1;

  scr1 = lfsrgen([1 9 11],      Ns, '7FF').';
  scr2 = lfsrgen([1 7 9 10 11], Ns, '7FF').';

  x1 = [circshift(scr2, 0), ...
        mod((circshift(scr2, 1) + circshift(scr1, 4)),  2), ...
        mod((circshift(scr2, 2) + circshift(scr1, 9)),  2), ...
        mod((circshift(scr2, 0) + circshift(scr1, 10)), 2)];

  y1 = x1(:,1) + 2*x1(:,2) + 4*x1(:,3) + 8*x1(:,4);

  x2 = [circshift(scr1, 0), ...
        mod((circshift(scr1, 1) + circshift(scr2, 4)),  2), ...
        mod((circshift(scr1, 2) + circshift(scr2, 9)),  2), ...
        mod((circshift(scr1, 0) + circshift(scr2, 10)), 2)];

  y2 = x2(:,1) + 2*x2(:,2) + 4*x2(:,3) + 8*x2(:,4);
```


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```
  tm6 = ((2*(16*y1 + y2) - 255)/256).';
end


% Volterra's estimation and analysis
function [HD2 HD3 HD4 RD] = volest(x, d, n, dly)
  % Init
  R  = 0;
  rD = 0;

  % Addition autocorrelation and cross-correlation
  for k = n:length(x),
    % Volterra products
    xi = [...
      1 ...
      x(k:-1:k-n+1) ...
      x(k:-1:k-n+1)  .*x(k:-1:k-n+1)   ...
      x(k:-1:k-n+1+1).*x(k-1:-1:k-n+1) ...
      x(k:-1:k-n+1+2).*x(k-2:-1:k-n+1) ...
      x(k:-1:k-n+1)  .*x(k:-1:k-n+1)    .*x(k:-1:k-n+1)   ...
      x(k:-1:k-n+1+1).*x(k:-1:k-n+1+1)  .*x(k-1:-1:k-n+1) ...
      x(k:-1:k-n+1+2).*x(k:-1:k-n+1+2)  .*x(k-2:-1:k-n+1) ...
      x(k:-1:k-n+1+1).*x(k-1:-1:k-n+1)  .*x(k-1:-1:k-n+1) ...
      x(k:-1:k-n+1+2).*x(k-1:-1:k-n+1+1).*x(k-2:-1:k-n+1) ...
      x(k:-1:k-n+1+2).*x(k-2:-1:k-n+1)  .*x(k-2:-1:k-n+1) ...
      x(k:-1:k-n+1)  .*x(k:-1:k-n+1)  .*x(k:-1:k-n+1)  .*x(k:-1:k-n+1) ...
      x(k:-1:k-n+1+1).*x(k:-1:k-n+1+1).*x(k:-1:k-n+1+1).*x(k-1:-1:k-n+1) ...
      x(k:-1:k-n+1+1).*x(k:-1:k-n+1+1).*x(k-1:-1:k-n+1).*x(k-1:-1:k-n+1) ...
      x(k:-1:k-n+1+1).*x(k-1:-1:k-n+1).*x(k-1:-1:k-n+1).*x(k-1:-1:k-n+1)];

    % Autocorrelation matrix
    R = R + xi.'*xi;

    % Cross-correlation vector
    rD = rD + d(k-dly)*xi.';
  end

  % Wiener's MMSE solution
  hw = (R\rD).';

  % Separate the Volterra kernels per channel
  lw = [1 ...
        n ...
        n (n-1) (n-2) ...
        n (n-1) (n-2) (n-1) (n-2) (n-2) ...
        n (n-1) (n-1) (n-1)];

  ofst = 0;
  for i = 1:15,
    h{i} = hw(ofst+1:ofst+lw(i));
    ofst = ofst + lw(i);
  end

  % Calculate harmonic distortion
  HD2 = -10*log10(1/3*axc(h{2})/ ...
                  (1/5*axc(h{3}) + 1/9*axc(h{4}) + 1/9*axc(h{5})));

  HD3 = -10*log10(1/3*axc(h{2})/ ...
                  (1/7*axc(h{6})  + 1/15*axc(h{7})  + 1/15*axc(h{8}) + ...
                  1/15*axc(h{9}) + 1/27*axc(h{10}) + 1/15*axc(h{11})));

  HD4 = -10*log10(1/3*axc(h{2})/ ...
                  (1/9*axc(h{12}) + 1/21*axc(h{13})  + 1/25*axc(h{14}) + ...
                  1/21*axc(h{15})));

  % Calculate residual distortion
  z = h{1} + ...
      filter(h{2},  1, x(3:end)) + ...
      filter(h{3},  1, x(3:end).*x(3:end))   + ...
      filter(h{4},  1, x(3:end).*x(2:end-1)) + ...
      filter(h{5},  1, x(3:end).*x(1:end-2)) + ...
```


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```
      filter(h{6},  1, x(3:end).*x(3:end)  .*x(3:end))   + ...
      filter(h{7},  1, x(3:end).*x(3:end)  .*x(2:end-1)) + ...
      filter(h{8},  1, x(3:end).*x(3:end)  .*x(1:end-2)) + ...
      filter(h{9},  1, x(3:end).*x(2:end-1).*x(2:end-1)) + ...
      filter(h{10}, 1, x(3:end).*x(2:end-1).*x(1:end-2)) + ...
      filter(h{11}, 1, x(3:end).*x(1:end-2).*x(1:end-2)) + ...
      filter(h{12}, 1, x(3:end).*x(3:end)  .*x(3:end)  .*x(3:end))   + ...
      filter(h{13}, 1, x(3:end).*x(3:end)  .*x(3:end)  .*x(2:end-1)) + ...
      filter(h{14}, 1, x(3:end).*x(3:end)  .*x(2:end-1).*x(2:end-1)) + ...
      filter(h{15}, 1, x(3:end).*x(2:end-1).*x(2:end-1).*x(2:end-1));

  z = z(1+dly-2+n:end);
  d = d(1+n:end);
  l = min([length(z) length(d)]);
  e = z(1:l) - d(1:l);

  RD = -10*log10(1/3*axc(h{2})/var(e));
end


% Auto-correlation, main term
function xc = axc(x)
  xc = sum(x.^2);
end


% LFSR
function out = lfsrgen(poly, len, seed)
  r = double(dec2bin(hex2dec(seed))) - 48;
  r = [zeros(1,poly(end)-length(r)) r];

  for i = 1:len,
    out(i) = r(1);
    fb = 0;
    for j = 2:length(poly),
      fb = mod(fb + r(poly(j)), 2);
    end
    r = [fb r(1:poly(end))];
  end
end
```

115.6.4.9 Transmitter timing jitter measurement

The transmitter timing jitter shall meet the specifications per the following measurement procedure:

a) The PHY is configured in test mode 2 (115.5.2).
b) RMS (Root Mean Square) jitter of the crossing events of transmit signal with the average optical power is measured relative to the corresponding edges of an unjittered clock reference with a frequency of 162.5 MHz (one half the symbol rate), over an interval of 2 ms ± 10%.

The measurement device connected to TP2 shall meet the following specifications:

1) Capture capability.
2) High-frequency low-pass corner of at least 32.5 MHz with slope of –20 dB/decade.
3) Low-frequency high-pass corner of maximum 1 kHz with slope of +20 dB/decade.
4) The unjittered reference is a constant frequency clock extracted from each record of captured output at TP2, and is based on linear regression of frequency and phase that produces a minimum Time Interval Error.

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115.6.4.10 Transmitter relative intensity noise (RIN) measurement

This test might not be an appropriate system level test in all implementations, but all implementations shall meet the specified performance. The PHY is configured in test mode 5 (115.5.5). RIN is measured according to 58.7.7 with the following exceptions:

a) The low-pass filter bandwidth is 162.5 MHz (one half the symbol rate).
b) Step d) of the test procedure in 58.7.7.3 is replaced by measuring the value of the photocurrent of the optical to electrical converter I_{oe}.
c) Step e) of the test procedure in 58.7.7.3 is replaced by using the following equation to evaluate RIN:

$$RIN = 10 \times \log_{10}\left(\frac{P_N}{BW \times I_{oe}^{\ 2} \times R}\right) - G \text{ (dB/Hz)} \quad (115\text{–}34)$$

where

RIN	is the relative intensity noise
P_N	is the electrical noise power in Watts with modulation off
BW	is the low-pass bandwidth of the apparatus – high-pass bandwidth of the apparatus due to dc blocking capacitor
I_{oe}	is the photocurrent of the optical to electrical converter
R	is the effective load impedance of the optical to electrical converter (for example, a 50 Ω detector load in parallel with a 50 Ω power meter would give R equal to 25)
G	is the gain in dB of any amplifier in the noise measurement path

115.6.4.11 Transmitter modal power distribution measurement

The modal power distribution (MPD) at TP2 shall meet the specifications of 115.6.3.1 using an encircled angular flux (EAF) measurement method based on two-dimensional far field pattern data captured at TP2, which conforms to IEC 61300-3-53, defined for step-index multimode fibers.

When making this measurement the PHY is configured in normal (non-test) operation. A measured MPD meets the specification when it is higher than the lower bound limits defined for every angle. For the angle points not specified in Table 115–9, the EAF lower bound limit is calculated by linear interpolation.

115.7 Characteristics of the fiber optic cabling (channel)

The fiber optic cabling model is shown in Figure 115–36.

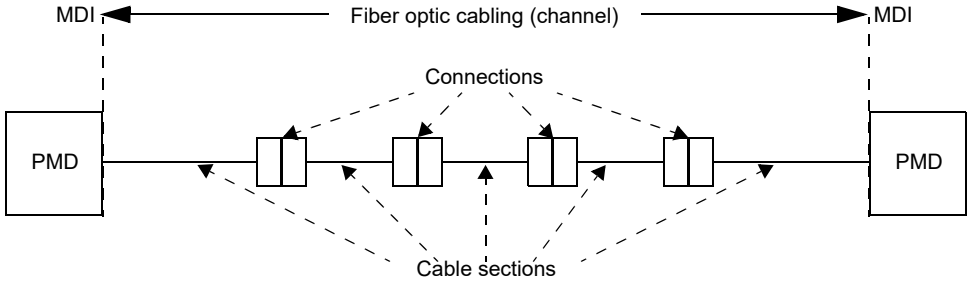

Figure 115–36—Fiber optic cabling model (channel)

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1000BASE-RHx operation requires fiber optic cable meeting the requirements of IEC 60793-2-40 sub-category A4a.2 multimode plastic optical fibers with appropriate augmentation as specified in this subclause. The link segment uses two optical fibers, one for each direction (see 115.1.5), and is composed of one or more cable sections and their in-line connections. The fiber optic cabling model (channel) defined here is a simplex fiber optic link segment, which is sufficient for testing purposes. The term channel is used here for consistency with generic cabling standards.

The following three different fiber optic channel types are specified:

a) Fiber optic channel type I supports reliable link per the specifications of 115.6.3.3 with reach up to at least 50 m. The fiber optic channel type I shall meet a maximum insertion loss of 9.5 dB without in-line connections and the transfer function specification of 115.7.1, per measurement techniques defined in 115.7.4 and 115.7.5, and under spectral distribution and launching modal power distribution at TP2 specified per EAF lower bound limits in 115.6.3.1.
b) Fiber optic channel type II supports reliable link per the specifications of 115.6.3.3 with reach up to at least 40 m. The fiber optic channel type II shall meet a maximum insertion loss of 8 dB without in-line connections and the transfer function specification of 115.7.2, per measurement techniques defined in 115.7.4 and 115.7.5, and under spectral distribution and launching modal power distribution at TP2 specified per EAF lower bound limits in 115.6.3.1. The parameters of this channel type include additional considerations for the environmental conditions of the intended application.
c) Fiber optic channel type III supports reliable link per the specifications of 115.6.3.3 with reach up to at least 15 m. The fiber optic channel type III shall meet a maximum insertion loss of 3 dB without in-line connections and the transfer function specification of 115.7.3, per measurement techniques defined in 115.7.4 and 115.7.5, and under spectral distribution and launching modal power distribution at TP2 specified per EAF lower bound limits in 115.6.3.1. The parameters of this channel type include additional considerations for the environmental conditions of the intended application.

NOTE—It may be possible to construct compliant fiber optic cables longer than indicated. Length of a fiber optic cable does not imply compliance to specifications.

The fiber optic channel transfer function captures the frequency-dependent propagation of the light through the fiber that is caused by the modal and chromatic dispersion. The transfer function is specified in magnitude normalized at dc and is given as a lower bound limit. Any fiber optic channel including in-line connections shall meet the transfer function specification of each type.

The number of supported in-line connections is not normative but instead depends on the specific in-line connection technology and the unallocated link margin (see 115.7.6).

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115.7.1 Transfer function of fiber optic channel type I

The transfer function of a fiber optic channel is compliant with type I when it is higher than the lower bound limits of Table 115–13 for any frequency less than or equal to 162.5 MHz. For the frequency points not specified, the transfer function is calculated by linear interpolation. The transfer function lower bound limits of a fiber optic channel type I are illustrated in Figure 115–37.

Table 115–13—Transfer function lower bound limits for fiber optic channel type I

Frequency (MHz)	Transfer function magnitude (dB)	Frequency (MHz)	Transfer function magnitude (dB)
0	0.0	70	–4.0
10	–0.1	85	–5.4
20	–0.3	105	–6.9
30	–0.7	125	–7.8
40	–1.3	145	–8.7
50	–2.1	162.5	–9.5
60	–3.0		

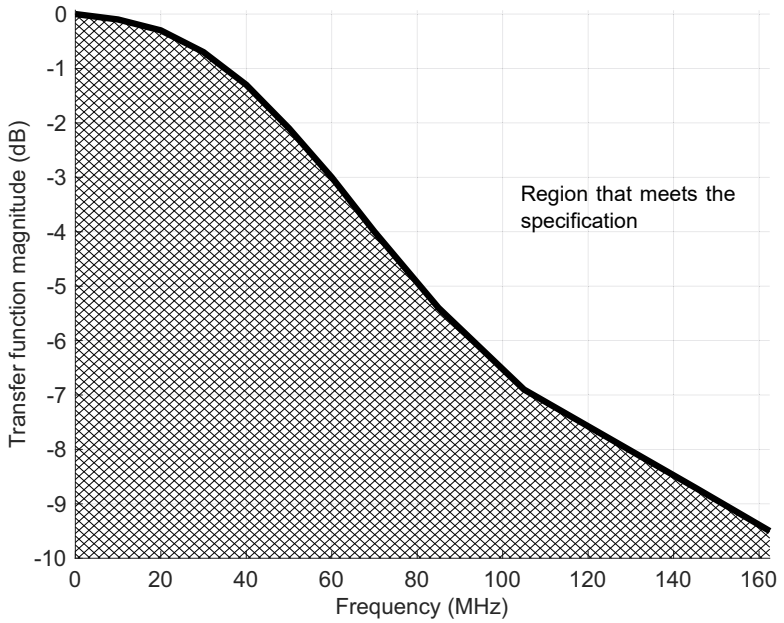

Figure 115–37—Transfer function illustration for fiber optic channel type I

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115.7.2 Transfer function of fiber optic channel type II

The transfer function of a fiber optic channel is compliant with type II when it is higher than the lower bound limits of Table 115–14 for any frequency less than or equal to 162.5 MHz. For the frequency points not specified, the transfer function is calculated by linear interpolation. The transfer function lower bound limits of a fiber optic channel type II are illustrated in Figure 115–38.

Table 115–14—Transfer function lower bound limits for fiber optic channel type II

Frequency (MHz)	Transfer function magnitude (dB)	Frequency (MHz)	Transfer function magnitude (dB)
0	0	70	–2.2
10	–0.1	85	–3.2
20	–0.2	105	–4.8
30	–0.4	125	–6.2
40	–0.7	145	–7.4
50	–1.1	162.5	–8.1
60	–1.6		

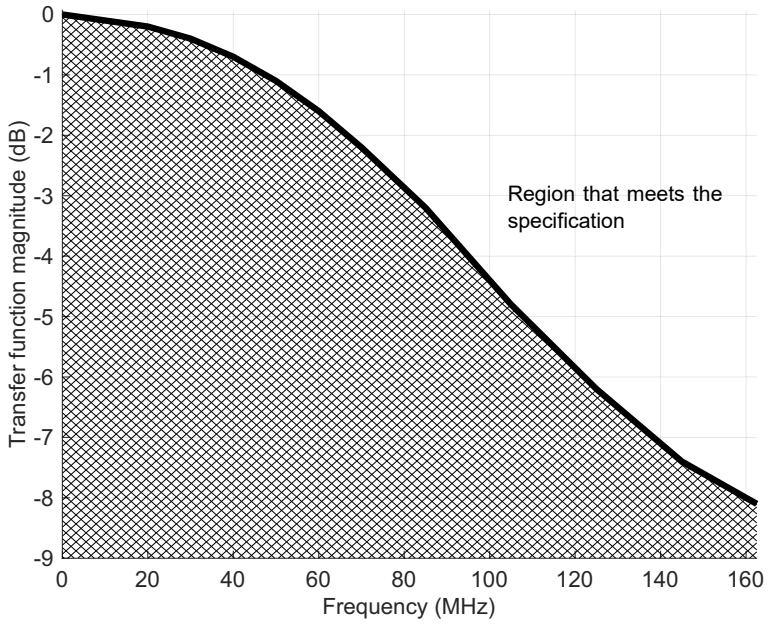

Figure 115–38—Transfer function illustration for fiber optic channel type II

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115.7.3 Transfer function of fiber optic channel type III

The transfer function of a fiber optic channel is compliant with type III when it is higher than the lower bound limits of Table 115–15 for any frequency less than or equal to 162.5 MHz. For the frequency points not specified, the transfer function is calculated by linear interpolation. The transfer function lower bound limits of a fiber optic channel type III are illustrated in Figure 115–39.

Table 115–15—Transfer function lower bound limits for fiber optic channel type III

Frequency (MHz)	Transfer function magnitude (dB)
0	0
50	–0.1
85	–0.5
125	–1.4
162.5	–2.5

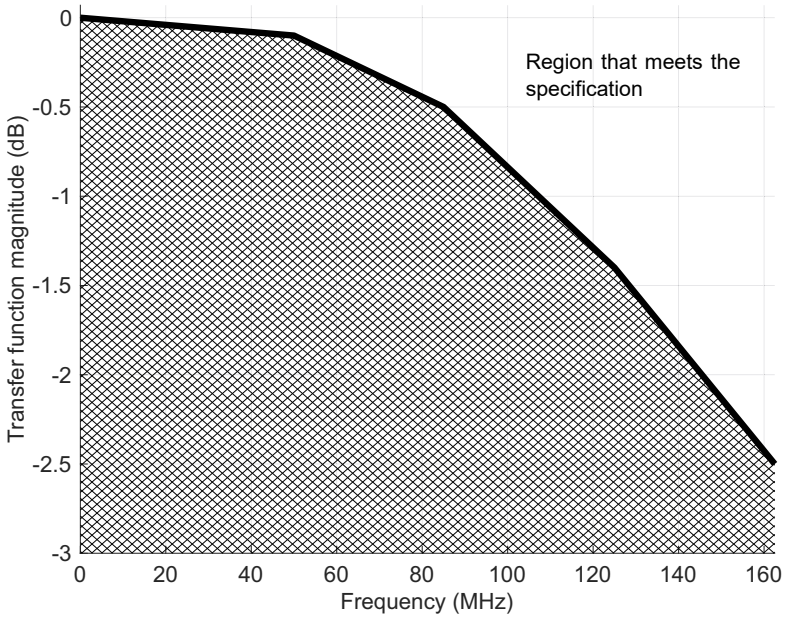

Figure 115–39—Transfer function illustration for fiber optic channel type III

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115.7.4 Fiber optic channel insertion loss measurement

The fiber optic channel shall meet the insertion loss specification per measurement according to ISO/IEC 14763-3, under spectral distribution and launch modal power distribution at TP2 specified per EAF lower bound limits in 115.6.3.1.

115.7.5 Fiber optic channel transfer function measurement

The fiber optic channel shall meet the transfer function specification per measurement according to IEC 60793-1-41:2010, under spectral distribution and launch modal power distribution at TP2 specified per EAF lower bound limits in 115.6.3.1.

115.7.6 Worst-case 1000BASE-RHx link power budget

Table 115–16 shows the worst-case link power budget and the unallocated link margin for a 1000BASE-RHx PHY, which are derived from the transmitter and the receiver optical specifications as well as fiber optic channel specifications provided in 115.6.3.1, 115.6.3.3, and 115.7, respectively.

Table 115–16—Worst case link power budget

Parameter	Units	RHA	RHB	RHC	
		Fiber optic channel			
		Type I	Type I	Type II	Type III
Link power budget (min)	dB	11	10	8	9.5
Channel insertion loss without in-line connections (max)	dB	9.5	9.5	8	3
Unallocated link margin (min)[a]	dB	1.5	0.5	0	6.5

[a] Unallocated link margin may be used for in-line connections (connectors). Maximum 1.5 dB insertion loss per in-line connection is assumed.

115.8 Medium Dependent Interface (MDI)

The 1000BASE-RHx PMD is coupled to the fiber optic cabling through a connection at the Medium Dependent Interface (MDI). The MDI mechanical interface for 1000BASE-RHA is defined in 115.8.1. An MDI mechanical interface is not specified for 1000BASE-RHB and 1000BASE-RHC.

The transmit signal characteristics are defined at the output end of a 1 meter length (TP2) of plastic optical fiber. The optical receive signal is defined at the output of the fiber optic cabling (TP3). Therefore, both the transmitter and the receiver optical characteristics are specified including the MDI mechanical implementation.

115.8.1 MDI mechanical interface for 1000BASE-RHA

The 1000BASE-RHA PMD and the associated MDI receptacle are coupled to the prepared fiber optic cabling without a plug.

The 1000BASE-RHA MDI receptacle shall be a duplex housing consisting of two separated slots (transmit and receive). Viewed from the link segment side of the connection, the 1000BASE-RHA MDI receptacle

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shall properly indicate with labeling the slot of the transmitter and the slot of the receiver. Figure 115–40 illustrates example MDI receptacle with labeling.

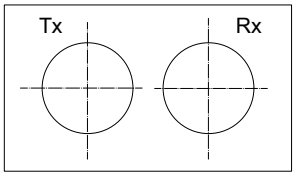

Figure 115–40—Example MDI receptacle (link segment side view)

The 1000BASE-RHA MDI receptacle shall accept link segment duplex cable compliant with specifications of buffered A4 fibers per IEC 60794-2-41.

The 1000BASE-RHA MDI receptacle shall have defined open and close states. The close state shall provide a stable and resilient connection by utilizing a retention mechanism with a minimum steady-state retention force of 4 N aligned with the center line of the receptacle hole in the direction of cable extraction for polyethylene (PE) jacket buffered fibers. Retention force per test procedure of IEC 61300-2-4 shall result in a loss of less than 0.4 dB of the AOP coupled by the PMD transmitter into the fiber while the load is applied and after the load is removed.

The duplex POF cable needs to be properly prepared and split into two single jacketed fibers for connection to the 1000BASE-RHA MDI receptacle.

The POF cable is normally prepared without polishing by using a POF cutting tool. The cutting tool may clamp the POF cable, without damaging the jacket, to prevent movement when cutting it (e.g., with a razor blade). The cutting tool shall provide the following results:

— The resultant fiber end facets are perpendicular to the cable axis with end angle error less than 2.5º.
— The flatness of the fiber end facet produces an insertion loss of less than 1.5 dB, per butt coupling of the two resultant fiber segments.

The duplex cable is split to enable the following:

— Full insertion and guidance inside the MDI receptacle slot
— Bend radius over 25 mm

The 1000BASE-RHA MDI receptacle vendor shall clearly indicate the minimum split length needed for a suitable connection. The left side of Figure 115–41 illustrates the duplex POF cable splitting and the right side illustrates the fiber cable connection to 1000BASE-RHA MDI receptacle.

One of the jackets of the duplex POF cable shall have marking. A possible marking is illustrated in Figure 115–41. Such marking can facilitate installation when the optical transmitters of the link partners are off. There may be specific application marking requirements.

Two different installation scenarios can be considered for correct link segment crossover—the scenario where visible transmit light is used and the scenario where the fiber cable marking is used.

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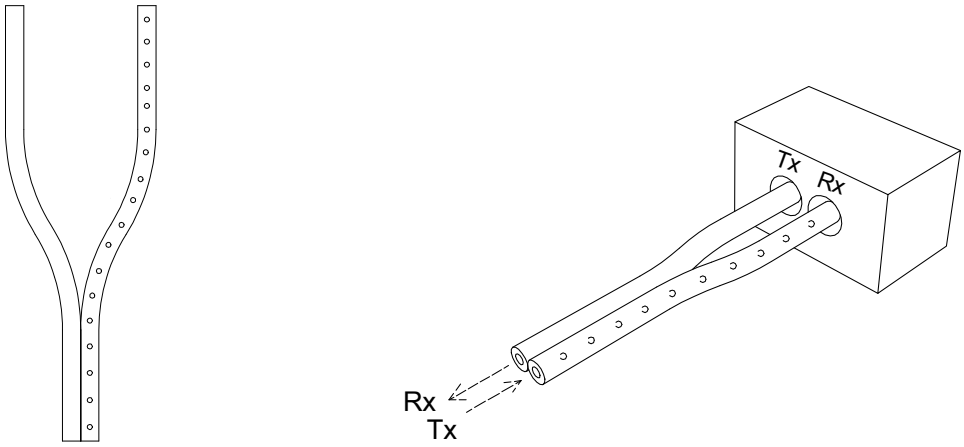

Figure 115–41—Duplex POF cable splitting and connection to the 1000BASE-RHA MDI receptacle

When the remote link partner is transmitting, the fiber used by the link partner to transmit can be easily distinguished because of the 1000BASE-RHA visible light. This fiber is connected to the local receiver, and the other fiber of duplex cable is connected from the local transmitter to the remote receiver. When the remote link partner is not transmitting, the cable specific marking can be used to implement a single crossover between the link partners identifying the correct insertion of the fiber ends into the MDI receptacle.

115.9 1000BASE-H Operations, Administration, and Maintenance (1000BASE-H OAM) channel

The optional 1000BASE-H OAM channel provides a mechanism to reliably exchange messages between station management entity (STA) peers attached to link partners. The 1000BASE-H OAM message exchange occurs in the PCS, as part of the PHD, and does not impact the normal GMII to GMII data transmission. Moreover, the 1000BASE-H OAM message exchange is not affected by EEE operation.

The 1000BASE-H OAM channel utilizes 1000BASE-H OAM transmit and receive registers accessible via the MDIO as well as capabilities specified in the following channel descriptions. All MDIO accessible registers for 1000BASE-H OAM operation are specified in 45.2.3.51 and 45.2.3.52.

The 1000BASE-H OAM channel uses several control bits (MSGT, MERT, PHYT) for message identification, message delivery notification, and flow control.

115.9.1 1000BASE-H OAM message transmission protocol

When the STA connected to the local PHY needs to transmit a new message it shall follow these steps:

a) Wait until bit TXO_REQ of register 3.500 is zero, which indicates that the 1000BASE-H OAM transmit registers are free and that a new 1000BASE-H OAM message can be written.
b) Write the 128 user data bits of the 1000BASE-H OAM message into registers 3.501 through 3.508.

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c) Write the first 12 bits of the 1000BASE-H OAM message to the bits TXO_DATA0 of register 3.500, also setting bit TXO_REQ to one at the same time to request the transmission of the new message.

When the local PHY accepts the message for transmission, it simultaneously does the following operations:

1) Set the bit TXO_REQ of register 3.500 to zero.
2) Change the bit TXO_MSGT of register 3.500, and copy the new value to LOCPHD.OAM.MSGT.
3) Copy the rest of the message to LOCPHD fields. Bits TXO_DATA0 of register 3.500 are copied to the field LOCPHD.OAM.DATA0. The contents of registers 3.501 through 3.508 are copied to the fields LOCPHD.OAM.DATA1 through LOCPHD.OAM.DATA8.

The local PHY does not accept a new message for transmission until the previous 1000BASE-H OAM message has been accepted by the remote PHY. This happens when the field REMPHD.OAM.PHYT is equal to the field LOCPHD.OAM.MSGT.

Upon PHY reset, all the LOCPHD fields that comprise the 1000BASE-H OAM channel and all the bits in 1000BASE-H OAM transmit registers 3.500 through 3.508 are set to zero.

The fields LOCPHD.OAM.MSGT and LOCPHD.OAM.DATAx always maintain the values corresponding to the last message accepted by the local PHY for transmission, or the reset value if either 1000BASE-H OAM is not enabled or no message has been accepted for transmission since the last PHY reset.

115.9.2 1000BASE-H OAM channel status

There can be up to three outstanding 1000BASE-H OAM messages in the channel from the transmitting PHY to the receiver of the link partner: the message written in the 1000BASE-H OAM transmit registers that is waiting for transmission, the message being currently transmitted by the local PHY, and the message available in the 1000BASE-H OAM receive registers of the remote PHY that is waiting for processing by the remote STA.

The status of the three possible outstanding 1000BASE-H OAM messages can be decoded from the values of the control bits of register 3.500. Table 115–17 shows all the possible values of the four control bits, and the corresponding status of the three possible outstanding 1000BASE-H OAM messages.

Table 115–17—List of all possible 1000BASE-H OAM message status

TXO_ REQ	TXO_ MSGT	TXO_ PHYT	TXO_ MERT	Message K + 1 status	Message K status	Message K – 1 status
0	a	a	a	Not written by local STA	Sent by local PHY ACK by remote PHY ACK by remote STA	Sent by local PHY ACK by remote PHY ACK by remote STA
0	a	!a	!a	Not written by local STA	Sent by local PHY No ACK by remote PHY No ACK by remote STA	Sent by local PHY ACK by remote PHY ACK by remote STA
0	a	a	!a	Not written by local STA	Sent by local PHY ACK by remote PHY No ACK by remote STA	Sent by local PHY ACK by remote PHY ACK by remote STA

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Table 115–17—List of all possible 1000BASE-H OAM message status *(continued)*

TXO_ REQ	TXO_ MSGT	TXO_ PHYT	TXO_ MERT	Message K + 1 status	Message K status	Message K – 1 status
0	a	!a	a	Not written by local STA	Sent by local PHY No ACK by remote PHY No ACK by remote STA	Sent by local PHY ACK by remote PHY No ACK by remote STA
1	a	a	a	Written by local STA Pending transmission by local PHY	Sent by local PHY ACK by remote PHY ACK by remote STA	Sent by local PHY ACK by remote PHY ACK by remote STA
1	a	!a	!a	Written by local STA Pending transmission by local PHY	Sent by local PHY No ACK by remote PHY No ACK by remote STA	Sent by local PHY ACK by remote PHY ACK by remote STA
1	a	a	!a	Written by local STA Pending transmission by local PHY	Sent by local PHY ACK by remote PHY No ACK by remote STA	Sent by local PHY ACK by remote PHY ACK by remote STA
1	a	!a	a	Written by local STA Pending transmission by local PHY	Sent by local PHY No ACK by remote PHY No ACK by remote STA	Sent by local PHY ACK by remote PHY No ACK by remote STA

The control bits can be either 0 or 1, the symbol ! denotes logical not. Message K is the message currently being transmitted by the local PHY to the remote PHY; its associated message identification bit takes the value ‘a’ as indicated by bit TXO_MSGT. Correspondingly, message K – 1 is the previous message that was transmitted by the local PHY to the remote PHY. Its associated message identification bit takes the value ‘!a’. Finally message K + 1 corresponds to the 1000BASE-H OAM message being composed or yet to be accepted for transmission by the local PHY. Its associated message identification bit takes the value ‘!a’.

115.9.3 1000BASE-H OAM message reception protocol

When the local PHY receives a new 1000BASE-H OAM message as part of REMPHD fields and the 1000BASE-H OAM receive registers are free, it does the following operations:

a) Copy the content of the new message to the 1000BASE-H OAM receive registers.
b) Set the bit RXO_VAL of register 3.509 to one, indicating the presence of a new message in the 1000BASE-H OAM receive registers to the STA attached to the PHY.
c) Copy the value of the field REMPHD.OAM.MSGT to the field LOCPHD.OAM.PHYT to indicate to the remote PHY that the new message has been received by the PHY.

When the STA connected to the local PHY reads a new 1000BASE-H OAM message, it shall follow these steps:

1) Wait until the bit RXO_VAL of register 3.509 is one, which indicates that a new 1000BASE-H OAM message is in the 1000BASE-H OAM receive registers.

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2) When RXO_VAL is one, read the bits RXO_MSGT and RXO_DATA0 of the new 1000BASE-H OAM message, as they are also stored in register 3.509.
3) Read the rest of the message that is stored in registers 3.510 through 3.517. Reading the register 3.517 last is necessary for integrity of the 1000BASE-H OAM message. (The read of register 3.517 triggers the acknowledgment to the remote partner of the 1000BASE-H OAM that message has been read by the local attached STA, and indicates to the local PHY the 1000BASE-H OAM receive registers are available for a new 1000BASE-H OAM message.)

When the local STA reads register 3.517, the local PHY copies the MSGT bit of the message that has been read by the STA to the field LOCPHD.OAM.MERT.

Upon PHY reset, the fields LOCPHD.OAM.PHYT, LOCPHD.OAM.MERT, and all the bits of the 1000BASE-H OAM receive registers are reset to zero.

The field LOCPHD.OAM.PHYT always maintains the value corresponding to the last message copied to the 1000BASE-H OAM receive registers, or zero when 1000BASE-H OAM is disabled or no message has been copied to the 1000BASE-H OAM receive registers since the last PHY reset.

The field LOCPHD.OAM.MERT always maintains the value corresponding to the last message processed by the STA, or zero when 1000BASE-H OAM is disabled or no message has been processed by the STA since the last PHY reset.

115.9.4 1000BASE-H OAM channel state diagrams descriptions

115.9.4.1 1000BASE-H OAM control state variables

The following defines all the variables used in the 1000BASE-H OAM channel state diagrams that have not been previously introduced:

oam_cap
: Enables 1000BASE-H OAM channel functionality. This variable is set to TRUE when PHD.CAP.OAM of both transmit and receive PHD is TRUE. Otherwise, it is FALSE.
Values: TRUE: Both local and remote PHY have 1000BASE-H OAM ability and 1000BASE-H OAM functionality is enabled in both PHYs
FALSE: Either local or remote PHY does not have 1000BASE-H OAM ability or it is disabled

read_RXOAM_DATA8_event
: Event indicating that the 1000BASE-H OAM receive register 3.517 has been read. This event persists only long enough to cause one state diagram transition.

rxphd_mert
: Variable equivalent to the field REMPHD.OAM.MERT.
Values: 0 and 1

rxphd_msgt
: Variable equivalent to the field REMPHD.OAM.MSGT. It contains the message identification bit of the 1000BASE-H OAM message.
Values: 0 and 1

rxphd_oamudat
: Variable equivalent to the fields REMPHD.OAM.DATAx. It is the payload of the 1000BASE-H OAM message.
Values: Any value

rxphd_phyt
: Variable equivalent to the field REMPHD.OAM.PHYT.
Values: 0 and 1

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rxr_msgt

Variable equivalent to the bit RXO_MSGT of register 3.509. This bit is the message identification bit of the message contained in the 1000BASE-H OAM receive registers.

Values: 0 and 1

rxr_oamudat

Variable equivalent to the RXO_DATA0 field of register 3.509 concatenated with the RXO_DATA1 trough RXO_DATA8 of 1000BASE-H OAM receive registers 3.510 through 3.517.

Values: Any value

rxr_rxval

Variable equivalent to the bit RXO_VAL of register 3.509 that indicates the presence of a valid message in the 1000BASE-H OAM receive registers.

Values: 1: There is a valid message in the receive registers, which is pending for processing by the local STA
0: There is no valid message in the receive registers

txphd_mert

Variable equivalent to the field LOCPHD.OAM.MERT. It informs the remote PHY of the message identification bit of the last message that has been received by the local STA.

Values: 0 and 1

txphd_msgt

Identifier of the message being transmitted by the local PHY. This variable is equivalent to the field LOCPHD.OAM.MSGT.

Values: 0 and 1

txphd_oamudat

Variable equivalent to the content of the field LOCPHD.OAM.DATAx.

Values: Any value

txphd_phyt

Variable equivalent to the field LOCPHD.OAM.PHYT. It indicates to the remote PHY the message identification bit of the last valid message written to the receive registers.

Values: 0 and 1

txr_mert

Variable equivalent to the bit TXO_MERT of register 3.500. This bit is updated in OAMTX_TRANSMIT state to reflect the identifier of the last message that has been acknowledged by the remote STA.

Values: It alternates between values 0 and 1

txr_msgt

Variable equivalent to the bit TXO_MSGT of register 3.500. This bit is updated in OAMTX_TRANSMIT state to reflect the message identification bit of the message being sent by the local PHY.

Values: It alternates between values 0 and 1

txr_oamudat

Variable equivalent to the TXO_DATA0 field of register 3.500 concatenated with the TXO_DATA1 trough TXO_DATA8 of 1000BASE-H OAM transmit registers 3.501 through 3.508.

Values: Any value

txr_phyt

Variable equivalent to the bit TXO_PHYT of register 3.500. This bit is updated in OAMTX_TRANSMIT state to reflect the identifier of the last message that has been acknowledged by the remote PHY.

Values: It alternates between values 0 and 1

txr_txreq

Variable equivalent to the bit TXO_REQ of register 3.500. It indicates if the local STA is requesting the transmission of a new 1000BASE-H OAM message.

Values: 0: There is no message transmission request

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1: A new message has been written into the 1000BASE-H OAM transmit registers and transmission is requested

115.9.4.2 1000BASE-H OAM transmit control state diagram

The PHY operation for 1000BASE-H OAM message transmission shall conform to the 1000BASE-H OAM transmit control state diagram in Figure 115–42.

Upon reset (bit 1.0.15 set to one), disable of the PMA or determination of unreliable PHD communication, 1000BASE-H OAM transmit registers are reset (OAMTX_RESET state). Moreover, the LOCPHD fields of the 1000BASE-H OAM message are reset.

Once the transmission and reception of PHDs is reliable (rcvr_hdr_lock = OK), and the 1000BASE-H OAM channel is enabled, the local PHY waits for a new 1000BASE-H OAM message transmission request from the local STA (OAMTX_NEWMSG_WAIT state). Whenever a new valid PHD is received from the remote PHY, the local PHY updates the bit TXO_MERT of register 3.500 with the value of the field REMPHD.OAM.MERT and the bit TXO_PHYT of register 3.500 with the value of the field REMPHD.OAM.PHYT.

As soon as the first 1000BASE-H OAM message transmission is requested by the local STA (txr_txreq = 1), the local PHY accepts it, entering the OAMTX_TRANSMIT state. This causes the content of transmit registers 3.501 through 3.508 and the 12-bit TXO_DATA0 field of register 3.500 to be copied to the corresponding fields LOCPHD.OAM.DATAx. Simultaneously, field LOCPHD.OAM.MSGT is changed and copied to bit TXO_MSGT of register 3.500, and bit TXO_REQ of register 3.500 is cleared to zero. Thus, the local PHY indicates to the attached STA the MSGT assigned to the message and also that the 1000BASE-H OAM transmit registers are free to accept a new message.

From then on, the local PHY keeps transmitting the same 1000BASE-H OAM message within the PHD until the remote PHY acknowledges its reception (OAMTX_PHYT_WAIT state). Simultaneously, whenever a new valid PHD is received from the remote PHY, the local PHY updates the bits TXO_PHYT and TXO_MERT of register 3.500 with the values of the fields REMPHD.OAM.PHYT and REMPHD.OAM.MERT, respectively. As soon as the 1000BASE-H OAM message that is being currently transmitted within the PHD is acknowledged by the remote PHY, the local PHY can accept a new 1000BASE-H OAM message for transmission. The transition from state OAMTX_PHYT_WAIT to state OAMTX_NEWMSG_WAIT occurs when the values of fields REMPHD.OAM.PHYT and LOCPHD.OAM.MSGT are equal (rxphd_phyt = txphd_msgt).

115.9.4.3 1000BASE-H OAM receive control state diagram

The PHY operation for 1000BASE-H OAM message reception shall conform to the 1000BASE-H OAM receive control state diagram in Figure 115–43.

Upon reset (bit 1.0.15 set to one), disable of the PMA or determination of unreliable PHD reception, 1000BASE-H OAM receive registers are reset (OAMRX_RESET state). Moreover, fields LOCPHD.OAM.MERT and LOCPHD.OAM.PHYT are assigned the value zero.

Once the transmission and reception of PHDs are reliable (rcvr_hdr_lock = OK), the local PHY waits until the field REMPHD.OAM.MSGT is different from the bit RXO_MSGT of register 3.509. This indicates that a new 1000BASE-H OAM message has been received from the remote PHY. As soon as this event occurs, transition from state OAMRX_NEWMSG_WAIT to state OAMRX_RXR_UPDT takes place.

In the state OAMRX_RXR_UPDT, the content of the fields REMPHD.OAM.DATAx are stored in 1000BASE-H OAM receive registers 3.510 to 3.517 and the bits RXO_DATA0 of register 3.509. Simultaneously bit RXO_VAL of register 3.509 is set to 1, and the bit RXO_MSGT of register 3.509 is

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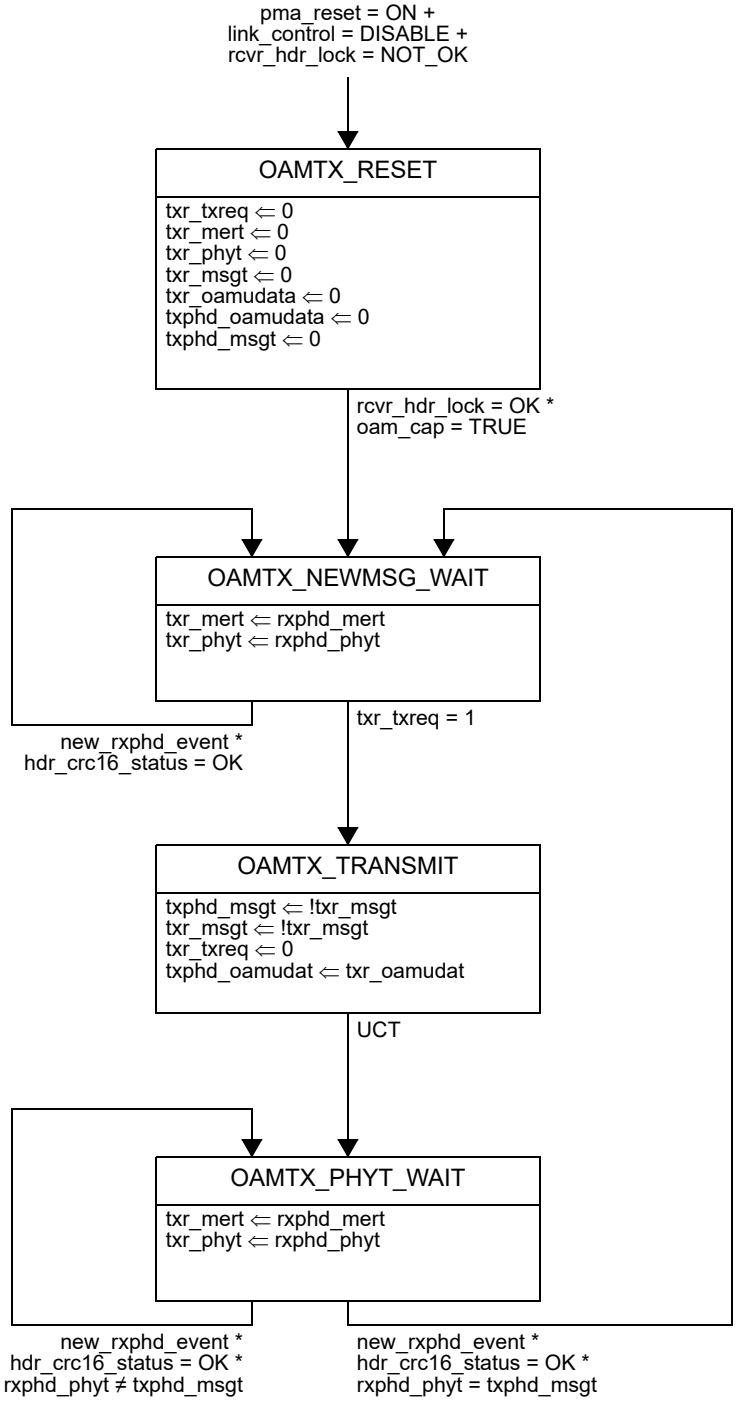

Figure 115–42—PHY 1000BASE-H OAM transmit control state diagram

updated with value of the field REMPHD.OAM.MSGT. Additionally, the local PHY notifies the remote PHY of the reception of the message by setting the field LOCPHD.OAM.PHYT to the value of the field REMPHD.OAM.MSGT (txphd_phyt ⇐ rxphd_msgt).

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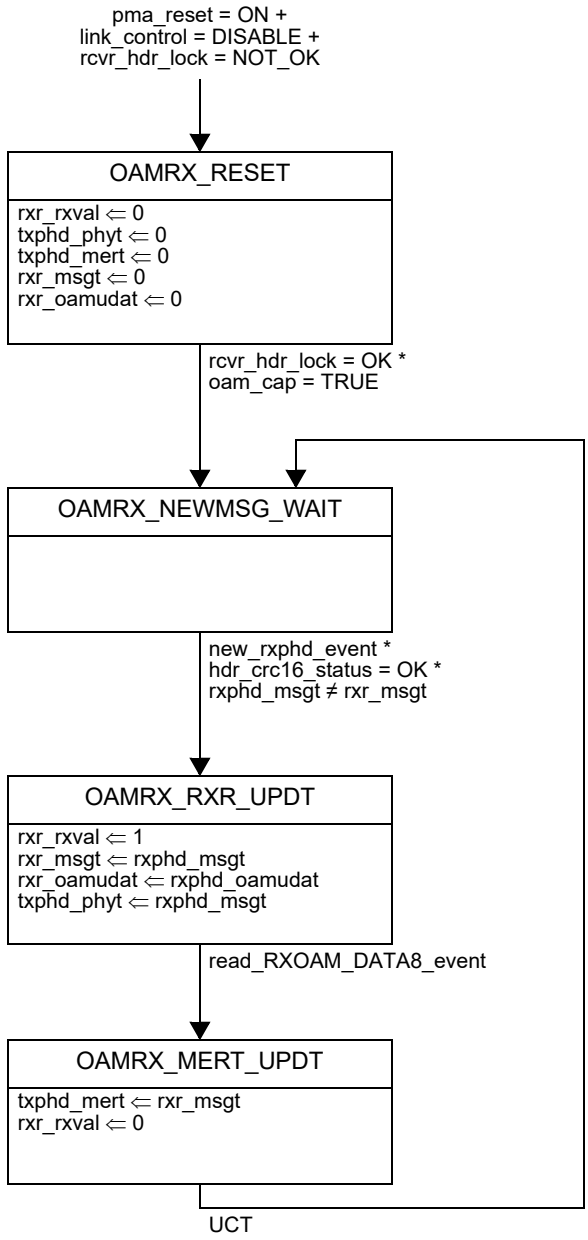

Figure 115–43—PHY 1000BASE-H OAM receive control state diagram

OAMRX_RXR_UPDT state transitions to OAMRX_MERT_UPDT state only when register 3.517 is read (read_OAMDATA8_event), so the 1000BASE-H OAM receive registers are locked until this event. State OAMRX_MERT_UPDT sets the bit RXO_VAL of register 3.509 to 0 indicating that no valid message is stored in the 1000BASE-H OAM receive registers. Also, the local PHY notifies the link partner of reception of the message by the local STA by setting the field LOCPHD.OAM.MERT to the value of the bit RXO_MSGT of register 3.509 (txphd_mert ⇐ rxr_msgt).

The local PHY then waits for a new message to be received (OAMRX_NEWMSG_WAIT).

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115.10 Loopback modes

1000BASE-H loopback modes shall be selected using bits 3.518.12:10. Loopback modes support a MAC transmit-to-self that includes selected portions of the local PHY or the local and the remote PHYs.

The default value and value upon reset (bit 1.0.15 = 1) shall be no loopback (3.518.12:10 = 000).

When GMII level loopback mode is selected (3.518.12:10 = 001), the 1000BASE-H PCS shall accept data on the transmit data path from the GMII, looping the data back to the receive path of the GMII. In this mode, the PCS transmitter and receiver are not part of the communication path, and the loopback functionality is provided independent of a link having been established with the link partner. Operations of PCS, PMA, and PMD sublayers are not specified in this loopback mode.

When PMD interface level loopback mode is selected (3.518.12:10 = 010), the loopback shall be implemented near the PMD service interface, completely exercising the PCS and PMA as in normal operation, although the PMA receiver ignores signals from the PMD receive function. PMD operation is not specified in this loopback mode.

When line loopback mode is selected (3.518.12:10 = 011), received data shall be processed and looped back near the GMII interface toward the link partner with data going back through the PCS and PMA transmit path. Received signal is equalized, decoded, and decapsulated by the PMA and PCS. Then the received data stream is forwarded to the GMII receive interface as well as to the PCS transmitter. The GMII transmit interface signals are ignored during line loopback operation. The line loopback is only operative when a bidirectional link has been established. The PCS, PMA, and PMD functions work as in normal operation. The data loopback is implemented between the output of the PCS 64B/65B decoder and the input of the encoder.

115.11 Management interface

PHYs in the 1000BASE-H set shall provide the management capabilities described in this clause and the functionality provided by the referenced Clause 45 registers and bits.

The optional MDIO capability of Clause 45 describes several variables that provide control and status for and about the PHY. If the MDIO is not implemented, an implementation shall include the functionality provided by the specified MDIO registers.

PHYs in the 1000BASE-H set use some generic control bits common with other IEEE 802.3 PHY types. PHY variables shall be mapped as shown in Table 115–18. PHYs in the 1000BASE-H set also use specific registers (1.11, 1.22, 1.900, and 3.500 through 3.522).

In addition to the normal operation capabilities specified elsewhere in this clause, test modes and loopback modes use these registers and bits to facilitate testing.

115.12 Environmental specifications

115.12.1 Temperature classes

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling appropriate to the intended environment (e.g., automotive, industrial, or home networking). A compliant 1000BASE-RHx PHY shall clearly indicate the operating temperature range of Table 115–19 over which their compliance is claimed.

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Table 115–18—1000BASE-H variable mapping

MDIO variable/value	PMA/PMD register	Register bit number	PMA/PMD variable/value
Reset = 1	PMA/PMD control 1	1.0.15	pma_reset = ON
Reset = 0	PMA/PMD control 1	1.0.15	pma_reset = OFF
Low Power = 1	PMA/PMD control 1	1.0.11	link_control = DISABLE
Low Power = 0	PMA/PMD control 1	1.0.11	link_control = ENABLE
Global PMD receive signal detect = 1	PMD receive signal detect	1.10.0	signal_detect = OK
Global PMD receive signal detect = 0	PMD receive signal detect	1.10.0	signal_detect = FAIL
Global PMD transmit disable = 1	PMD transmit disable	1.9.0	link_control = DISABLE
Global PMD transmit disable = 0	PMD transmit disable	1.9.0	link_control = ENABLE

Table 115–19—1000BASE-RHx temperature classes

Class	Low temperature (°C)	High temperature (°C)
Regular	0	+70
Extended I	–40	+85
Extended A	–40	+105

115.12.2 General safety

All equipment subject to this clause shall conform to IEC 60950-1 (for IT and motor vehicle applications) and to ISO 26262 (for motor vehicle applications only, if required by the given application). All equipment subject to this clause might additionally be required to conform to applicable local, state, or national motor vehicle standards or as agreed to between the customer and supplier.

115.12.3 Environmental safety

All equipment in automotive applications integrating a PHY subject to this clause shall conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications:

a) General loads: ISO 16750-1
b) Electrical loads: ISO 16750-2, ISO 7637-2:2008, and ISO 8820-1
c) Mechanical loads: ISO 16750-3, ASTM D4728, and ISO 12103-1
d) Climatic loads: ISO 16750-4, IEC 60068-2-1, IEC 60068-2-27, IEC 60068-2-30, IEC 60068-2-38, IEC 60068-2-52, IEC 60068-2-64, and IEC 60068-2-78
e) Chemical loads: ISO 16750-5 and ISO 20653

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Automotive environmental conditions are generally more severe than those found in many commercial environments.

The targeted application environment(s) require careful analysis.

115.12.4 Electromagnetic compatibility

A system integrating the 1000BASE-RHx PHY shall comply with all applicable local and national codes. In addition, the system might need to comply with more stringent requirements as agreed to between the customer and the supplier, for the limitation of electromagnetic interference. A 1000BASE-RHx PHY shall meet EMC requirements according to ISO 11452 and CISPR 25 test methods for radio frequency (RF) immunity and RF emissions. When used in an automotive environment, a 1000BASE-RHx PHY shall meet the following motor vehicle EMC requirements:

a) Radiated/Conducted Emissions: CISPR 25, IEC 61967-1/4, and IEC 61000-4-21
b) Radiated/Conducted Immunity: ISO 11452, IEC 62132-1/4, and IEC 61000-4-21
c) Electrostatic Discharge: ISO 10605 and IEC 61000-4-2/3
d) Electrical Disturbances: IEC 62215-3 and ISO 7637-2/3

Exact test setup and test limit values may be adapted to each specific application, subject to agreement between the customer and the supplier.

115.12.5 Optical safety

1000BASE-RHx transceivers shall be Hazard Level 1 laser certified under any condition of operation, including an LED as the optical signal source. This includes single fault conditions whether coupled into a fiber or out of an open bore. Transceivers shall be certified to be in conformance with IEC 60825-1 and IEC 60825-2.

Conformance to additional laser safety standards might be required for operation within specific geographic regions.

115.13 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays of a 1000BASE-RHx PHY shall not exceed 6500 bit-times. Transmit data delay is measured from the input of a given unit of data at the GMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the GMII.

NOTE 1—The transmit and receive delays are not independently testable in a system implementation, and only the total delay from GMII to GMII is testable.

NOTE 2—The physical medium interconnecting two PHYs introduces additional delay (approximately 5 bit-times per meter of POF). In-line connections can also introduce additional delay.

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115.14 Protocol implementation conformance statement (PICS) proforma for Clause 115, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer, types 1000BASE-RHA, 1000BASE-RHB, and 1000BASE-RHC[203]

115.14.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 115, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD), types 1000BASE-RHA, 1000BASE-RHB, and 1000BASE-RHC shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

115.14.2 Identification

115.14.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

115.14.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 115, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer, types 1000BASE-RHA, 1000BASE-RHB, and 1000BASE-RHC
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[203] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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115.14.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
GMII	PHY with exposed GMII	115.2	Interface is supported	O	Yes [ ] No [ ]
*BHOAM	1000BASE-H OAM channel	115.9	1000BASE-H OAM channel implementation	O	Yes [ ] No [ ]
*EEE	EEE capability	115.4	EEE implementation	O	Yes [ ] No [ ]
RHA	PMD type	115.6.3	Implementation of 1000BASE-RHA PMD	O/1	Yes [ ] No [ ]
RHB	PMD type	115.6.3	Implementation of 1000BASE-RHB PMD	O/1	Yes [ ] No [ ]
RHC	PMD type	115.6.3	Implementation of 1000BASE-RHC PMD	O/1	Yes [ ] No [ ]
TCR	Regular temperature class	115.12.1	Implementation of 1000BASE-RHx temperature class Regular	O/2	Yes [ ] No [ ]
TCI	Extended I temperature class	115.12.1	Implementation of 1000BASE-RHx temperature class Extended I	O/2	Yes [ ] No [ ]
TCA	Extended A temperature class	115.12.1	Implementation of 1000BASE-RHx temperature class Extended A	O/2	Yes [ ] No [ ]
*AE	Motor vehicle requirements	115.12.3, 115.12.4	Implementation of motor vehicle environmental requirement	O	Yes [ ] No [ ]
*MDIO	MDIO implemented	115.11		O	Yes [ ] No [ ]

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115.14.4 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Value/Comment	Status	Support
PCS1	Transmit Block transmission	115.2.1	Transmit Blocks transmitted continuously on active link	M	Yes [ ]
PCS2	Transmit Block format	115.2.1	Transmit Block format as specified	M	Yes [ ]
PCS3	Transmit Block symbols rate	115.2.1	Transmit Block symbols transmitted to the PMA at the symbol rate	M	Yes [ ]
PCS4	Pilot S1 generator	115.2.2.1	Pilot S1 generated as specified	M	Yes [ ]
PCS5	Pilot S2 generator	115.2.2.2	Generate 13 $S2_x$ sub-blocks per Transmit Block as specified	M	Yes [ ]
PCS6	Physical header CRC16 input	115.2.3.1	CRC16 computed from PHD bits	M	Yes [ ]
PCS7	Physical header CRC16 operation	115.2.3.1	CRC16 complies with Figure 115–10	M	Yes [ ]
PCS8	Physical header CRC16 initialization	115.2.3.1	CRC16 shift register initialized to 0x0000	M	Yes [ ]
PCS9	Physical header scrambler	115.2.3.2	Scrambler produces same results as Figure 115–11	M	Yes [ ]
PCS10	Physical header scrambler initialization	115.2.3.2	Scrambler shift register initialized with 0x068D332	M	Yes [ ]
PCS11	Physical header BCH encoder	115.2.3.3	720 bits systematically encoded into 896 bits with BCH encoder	M	Yes [ ]
PCS12	Physical header BCH encoder operation	115.2.3.3	BCH parity same as Figure 115–19	M	Yes [ ]
PCS13	Physical header BCH encoder initialization	115.2.3.3	BCH delay elements initialized to zero before encoding	M	Yes [ ]
PCS14	Physical header modulation	115.2.3.4	Physical header modulated as specified	M	Yes [ ]
PCS15	Physical header ordering, division	115.2.3.5	PHS divided in 14 pieces of 128-symbol each, preserving symbol ordering	M	Yes [ ]
PCS16	Physical header ordering, prefixing and postfixing	115.2.3.5	PHS_x pieces prefixed and postfixed with 16 {0} symbols	M	Yes [ ]
PCS17	64B/65B encoder	115.2.4.1.2	Same result of code	M	Yes [ ]
PCS18	PDB alignment signaling	115.2.4.1.3	PDB offset from beginning of first payload sub-block of Transmit Block j+1 indicated in PHD of Transmit Block j	M	Yes [ ]
PCS19	Payload data binary scrambler operation	115.2.4.2	Scrambler produces same result as Figure 115–16	M	Yes [ ]
PCS20	Payload data binary scrambler initialization	115.2.4.2	Scrambler shift register initialized with 0x17C9C58 per Transmit Block	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PCS21	MLCC demultiplexer	115.2.4.3.1	3150 bits per codeword are demultiplexed in two flows as specified	M	Yes [ ]
PCS22	Payload BCH encoder	115.2.4.3.2	1668 bits of first level systematically encoded into 1976 bits with BCH encoder	M	Yes [ ]
PCS23	Payload BCH encoder operation	115.2.4.3.2	BCH encoder produces same results as Figure 115–19	M	Yes [ ]
PCS24	Payload BCH encoder initialization	115.2.4.3.2	BCH delay elements initialized to zero before encoding	M	Yes [ ]
PCS25	QAM16 mapper	115.2.4.3.3	First level BCH coded bits mapped into QAM16 symbols per codeword as specified	M	Yes [ ]
PCS26	QAM8 mapper	115.2.4.3.4	Second level bits mapped into QAM8 symbols per codeword as specified	M	Yes [ ]
PCS27	First lattice transformation to first level QAM16 symbols	115.2.4.3.5	QAM16 symbols processed symbol-by-symbol per Equation (115–7) and Equation (115–8)	M	Yes [ ]
PCS28	First lattice transformation to second level QAM8 symbols	115.2.4.3.5	QAM8 symbols processed symbol-by-symbol per Equation (115–9) and Equation (115–10)	M	Yes [ ]
PCS29	Lattice addition	115.2.4.3.6	MLCC level 1 and level 2 symbols are added per Equation (115–11) and Equation (115–12)	M	Yes [ ]
PCS30	Second lattice transformation	115.2.4.3.7	Symbols from lattice adder processed symbol-by-symbol per Equation (115–13) and Equation (115–14)	M	Yes [ ]
PCS31	QAM to PAM multiplexer	115.2.4.3.8	988 PAM16 symbols generated from 494 QAM128 symbols per codeword as specified	M	Yes [ ]
PCS32	Payload data symbol scrambler	115.2.4.4	PAM16 payload data symbols scrambled as specified	M	Yes [ ]
PCS33	PCS receive function	115.2.5	Do PHD decoding, PAM16 decoding, and 64B/65B decoding	M	Yes [ ]
PCS34	PCS receive function, decoded PHD fields	115.2.5	PHD data discarded when CRC16 fails	M	Yes [ ]
PCS35	PCS receive function, MLCC decoding failure	115.2.5	Bits of MLCC marked as uncorrectable to 64B/65B decoder, when MLCC decoder is unable to correct	M	Yes [ ]
PCS36	PCS receive function, PHD alignment	115.2.5	Receiver determines alignment of received PDBs by using decoded PHD as specified	M	Yes [ ]
PCS37	64B/65B decoder	115.2.5	Same result of code	M	Yes [ ]

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115.14.5 Physical Medium Attachment (PMA)

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	Payload data THP	115.3.1.1	Payload data is THP processed per Equation (115–19), Equation (115–20), and Equation (115–21)	M	Yes [ ]
PMA2	Payload data THP, reset	115.3.1.1	Payload data THP state is reset before any payload data sub-block	M	Yes [ ]
PMA3	Transmit power scaling	115.3.1.2	Symbols of Transmit Block scaled with scaling factors per Table 115–5 before transmission to PMD	M	Yes [ ]
PMA4	Transmit power scaling, pilot S1, pilot $S2_x$ and PHS_x sub-blocks	115.3.1.2	Scaling factor directly applied to symbols from PCS transmit	M	Yes [ ]
PMA5	Transmit power scaling, payload data sub-blocks	115.3.1.2	Scaling factor applied to symbols from THP	M	Yes [ ]
PMA6	PHD content	115.3.4	PHD content as detailed in Table 115–6	M	Yes [ ]
PMA7	Transmit PHD commit point	115.3.4	PHD fields assigned by state diagrams are sampled at the start of a Transmit Block and transmitted in that current Transmit Block	M	Yes [ ]
PMA8	Receive PHD commit point	115.3.4	Received PHD fields are available to state diagrams and registers after reception, decoding, and validation of the entire PHS, and before Transmit Block reception is completed	M	Yes [ ]
PMA9	PHY TX control state diagram	115.3.5.2	Transmit operation conforms to Figure 115–22	M	Yes [ ]
PMA10	PHY RX control state diagram	115.3.5.3	Receive operation conforms to Figure 115–23	M	Yes [ ]
PMA11	Coarse timing recovery	115.3.5.3	Establish symbol synchronization and coarse timing recovery using pilot S1 signal	M	Yes [ ]
PMA12	Fine timing recovery	115.3.5.3	Perform fine timing recovery after symbol synchronization (s1_synch = OK) to provide stable receiver sampling clock	M	Yes [ ]
PMA13	Equalizer training using S2	115.3.5.3	After rcvr_clock_lock = OK train equalizers using received pilot $S2_x$ sub-blocks	M	Yes [ ]
PMA14	THP initialization	115.3.5.3	Initialize THP per 115.3.6.3 after rcvr_hdr_lock = OK	M	Yes [ ]
PMA15	Link monitor state diagram	115.3.5.4	Link status determined per Figure 115–24	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PMA16	PHD monitor state diagrams	115.3.5.5	Reliable PHD reception and transmission determined per state diagrams in Figure 115–25, Figure 115–26, and Figure 115–27	M	Yes [ ]
PMA17	Adaptive THP TX state diagram	115.3.6.2	The update of THP filter conforms to Figure 115–28	M	Yes [ ]
PMA18	Adaptive THP REQ state diagram	115.3.6.3	The request to link partner to adapt THP filter conforms to Figure 115–29	M	Yes [ ]
PMA19	PHY quality monitor state diagram	115.3.7.4	Local receiver status determined per state diagram of Figure 115–30	M	Yes [ ]
PMA20	Fixed-point format	115.3.8	PHY conforms to the fixed-point encoding and decoding per code in 115.3.8.1 and 115.3.8.2	M	Yes [ ]

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115.14.6 Energy-Efficient Ethernet (EEE)

Item	Feature	Subclause	Value/Comment	Status	Support
EEE1	EEE ability advertisement	115.4	EEE ability advertised by setting PHD.CAP.LPI	EEE:M	Yes [ ] N/A [ ]
EEE2	EEE operational	115.4	EEE only operational when both partners have capability and have enabled it, by advertising PHD.CAP.LPI = 1	EEE:M	Yes [ ] N/A [ ]
EEE3	LPI mode transmit operation dependency with link status	115.4.1	LPI mode only able to enter once link_status = OK.	EEE:M	Yes [ ] N/A [ ]
EEE4	LPI mode transmit, start of operation alignment	115.4.1	LPI mode enters aligned to next payload data sub-block of a PDB encoding Assert LPI, unless normal idle is restored before end of current sub-block	EEE:M	Yes [ ] N/A [ ]
EEE5	LPI mode transmit operation, refresh signals	115.4.1	PHY transmits pilot and PHS_x sub-blocks as in normal mode	EEE:M	Yes [ ] N/A [ ]
EEE6	LPI mode transmit operation, payload data sub-blocks	115.4.1	Payload data sub-blocks transmitted in LPI mode with specified signaling	EEE:M	Yes [ ] N/A [ ]
EEE7	LPI mode transmit operation, normal operation resume	115.4.1	PHY transmitter exits LPI mode at the next payload data sub-block when normal idle is transferred in the GMII data stream	EEE:M	Yes [ ] N/A [ ]
EEE8	LPI mode transmit operation, 64B/65B encoder timing preservation	115.4.1	64B/65B encoder preserves timing in LPI mode	EEE:M	Yes [ ] N/A [ ]
EEE9	LPI mode transmit operation, payload scramblers timing preservation	115.4.1	Payload binary and symbol scramblers preserves timing during LPI mode	EEE:M	Yes [ ] N/A [ ]
EEE10	LPI mode receive, start of operation alignment	115.4.2	LPI mode enters by detection of zero symbols at beginning of a payload data sub-block	EEE:M	Yes [ ] N/A [ ]
EEE11	LPI mode receive operation, normal mode resume	115.4.2	LPI mode exits by detection of PAM16-THP symbols at beginning of a payload data sub-block	EEE:M	Yes [ ] N/A [ ]
EEE12	LPI mode receive operation, 64B/65B decoder operation resume	115.4.2	64B/65B resumes operation aligned to the first received PDB	EEE:M	Yes [ ] N/A [ ]
EEE13	Power control of PMD transmit function	115.4.4	tx_pwr generation conforms to Figure 115–32	EEE:M	Yes [ ] N/A [ ]
EEE14	Power control of PMD receive function	115.4.4	rx_pwr and sd_inh generation conforms to Figure 115–33	EEE:M	Yes [ ] N/A [ ]

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115.14.7 Test modes

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Test modes	115.5	Test mode 1 through test mode 6 implemented	M	Yes [ ]
TM2	Selecting test modes	115.5	Selected with operation mode bits of the 1000BASE-H PCS control register	M	Yes [ ]
TM3	Test mode 1, PCS transmit operation	115.5.1	All zero bits sourced to binary scrambler and GMII ignored	M	Yes [ ]
TM4	Test mode 1, PCS receive operation	115.5.1	Any one bit at binary descrambler output counted as error	M	Yes [ ]
TM5	Test mode 1, PMA and PMD operation	115.5.1	PMA and PMD functions operate as in normal (non-test) mode	M	Yes [ ]
TM6	Test mode 1, transmit announcement	115.5.1	Announce to link partner using PHD.TX.NEXT.MODE as specified	M	Yes [ ]
TM7	Test mode 1 and normal mode PCS receive reconfiguration	115.5.1	PCS receive function reconfigured per PHD.TX.NEXT.MODE	M	Yes [ ]
TM8	Test mode 2 signal pattern	115.5.2	PMA transmits one {+1} symbol followed by one {–1}, continually, symbols timed with local symbol clock	M	Yes [ ]
TM9	Test mode 3 signal pattern	115.5.3	PMA transmits 10 {+1} symbol followed by 10 {–1}, continually, symbols timed with local symbol clock	M	Yes [ ]
TM10	Test mode 4 signal pattern	115.5.4	PMA transmits 250 times sequence $q1$ followed by 250 times sequence $q2$, continually, symbols timed with local symbol clock	M	Yes [ ]
TM11	Test mode 5 signal pattern	115.5.5	PMA transmits {0} symbols timed with local symbol clock	M	Yes [ ]
TM12	Test mode 6 signal pattern, scrambler generator polynomials	115.5.6	PMA transmit sequence s_n generated using scrambler generator polynomials per Equation (115–25) and Equation (115–26)	M	Yes [ ]
TM13	Test mode 6 signal pattern, shift registers update rate	115.5.6	Maximum-length shift registers updated once per symbol interval	M	Yes [ ]
TM14	Test mode 6 signal pattern, shift registers reset	115.5.6	Maximum-length shift registers reset to 0x7FF before pattern generation	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TM15	Test mode 6 signal pattern, intermediate $y0_n$ generation	115.5.6	$y0_n$ sequence of PAM16 symbols generated per Equation (115–27), from $Scr0_n$[10:0] and $Scr1_n$[10:0]	M	Yes [ ]
TM16	Test mode 6 signal pattern, intermediate $y1_n$ generation	115.5.6	$y1_n$ sequence of PAM16 symbols generated per Equation (115–28), from $Scr0_n$[10:0] and $Scr1_n$[10:0]	M	Yes [ ]
TM17	Test mode 6 signal pattern, s_n generation	115.5.6	s_n sequence of PAM256 symbols generated per Equation (115–29), from $y0_n$ and $y1_n$	M	Yes [ ]
TM18	Test mode 6 symbol clock reference	115.5.6	s_n sequence of PAM256 symbols timed with local symbol clock	M	Yes [ ]

115.14.8 Physical Medium Dependent (PMD)

Item	Feature	Subclause	Value/Comment	Status	Support
PMD1	PMD transmit function, symbol to optical signal	115.6.2.2	tx_signal amplitude translated to optical power signal per function of Equation (115–30)	M	Yes [ ]
PMD2	PMD transmit function, power control	115.6.2.2	Turn on and turn off optical power output per PMD_TXPWR.request	EEE:M	Yes [ ] N/A [ ]
PMD3	PMD receive function	115.6.2.3	Translate optical signal in MDI into analog signal provided by PMD_COMSIGNAL.indication	M	Yes [ ]
PMD4	PMD receive function, PMD_RXPWR.request(OFF)	115.6.2.3	PMD_RXPWR.request(OFF) causes save of PMD receiver state so not affected by optical signal during LPI quiet periods	EEE:M	Yes [ ] N/A [ ]
PMD5	PMD receive function, PMD_RXPWR.request(ON)	115.6.2.3	PMD_RXPWR.request(ON) resumes optical signal processing of PMD receiver	EEE:M	Yes [ ] N/A [ ]
PMD6	PMD signal detect function	115.6.2.4	signal_detect generated in response to MDI AOP and sd_inh per Table 115–7	M	Yes [ ]

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115.14.9 PMD to MDI optical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PMI1	Transmitter optical specifications	115.6.3.1	PHY transmitter meets Table 115–8 specifications measured at TP2 per techniques of 115.6.4	M	Yes [ ]
PMI2	Transmitter modal power distribution	115.6.3.1	Modal power distribution at TP2 is higher than lower bound limits of Table 115–9 per technique of 115.6.4.11	M	Yes [ ]
PMI3	Symbol transmission rate	115.6.3.2	Be within the range 325.00 MBd ± 0.01%	M	Yes [ ]
PMI4	Receiver optical specifications	115.6.3.3	PHY receiver meets Table 115–10 specifications measured at TP3 per techniques 115.6.4	M	Yes [ ]
PMI5	Damage threshold	115.6.3.3	Receiver tolerate, without damage, continuous exposure to an optical input signal having a power level as specified in Table 115–10	M	Yes [ ]
PMI6	Reliable link establishment	115.6.3.3	PHY able to establish a reliable link per 115.3.7.1 throughout minimum to maximum AOP range of Table 115–10, for received signals that were transmitted per 115.6.3.1 and have passed through a fiber optic channel per 115.7	M	Yes [ ]
PMI7	Error ratio	115.6.3.3	PHY provides a BER less than 10^{-12} in test mode 1 and a frame error ratio less than 1.1×10^{-10} for continuous transmission of 64-octet Ethernet frames in normal (non-test) mode, throughout minimum to maximum AOP range of Table 115–10, for received signals that were transmitted per 115.6.3.1 and have passed through a fiber optic channel per 115.7	M	Yes [ ]
PMI8	Receiver boundary conditions	115.6.3.4	PHY establishes reliable link as specified in 115.6.3.3 under conditions of 115.6.3.4.1 and 115.6.3.4.2	M	Yes [ ]

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115.14.10 Optical measurement requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Transmitter measurements location	115.6.4	All transmitter measurements made at TP2	M	Yes [ ]
OM2	Receiver measurements location	115.6.4	All receive measurements made at TP3	M	Yes [ ]
OM3	Center wavelength measurement	115.6.4.1	Center wavelength meets specifications per IEC 61280-1-3 under normal (non-test) operation mode signal	M	Yes [ ]
OM4	Spectral width measurement	115.6.4.2	Spectra width meets specifications per IEC 61280-1-3 under normal (non-test) operation mode signal	M	Yes [ ]
OM5	Average Optical Power (AOP) measurement	115.6.4.3	AOP meets specifications per 115.6.4.3	M	Yes [ ]
OM6	Transmitter rise and fall time measurements	115.6.4.4	Transmitter rise and fall time meets specifications per 115.6.4.4	M	Yes [ ]
OM7	Transmitter extinction ratio measurement	115.6.4.5	Transmitter extinction ratio meets specifications per 115.6.4.5	M	Yes [ ]
OM8	Transmitter overshoot measurement	115.6.4.6	Transmitter overshoot meets specifications per 115.6.4.6	M	Yes [ ]
OM9	Transmitter output droop measurement	115.6.4.7	Transmitter output droop meets specifications per 115.6.4.7	M	Yes [ ]
OM10	Transmitter distortion measurement	115.6.4.8	Transmitter distortion meets specifications per 115.6.4.8	M	Yes [ ]
OM11	Transmitter timing jitter measurement procedure	115.6.4.9	Transmitter jitter meets specifications per procedure of 115.6.4.9	M	Yes [ ]
OM12	Transmitter timing jitter measurement device	115.6.4.9	Transmitter jitter meets specifications using a measurement device per 115.6.4.9	M	Yes [ ]
OM13	Transmitter relative intensity noise (RIN) measurement	115.6.4.10	Transmitter RIN meets specifications per 115.6.4.10	M	Yes [ ]
OM14	Transmitter modal power distribution (MPD) measurement	115.6.4.11	Transmitter MPD meets specifications per 115.6.4.11	M	Yes [ ]

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115.14.11 Characteristics of the fiber optic cabling (channel)

Item	Feature	Subclause	Value/Comment	Status	Support
CH1	Fiber optic channel type I	115.7	Insertion loss is less than 9.5 dB without in-line connections, and transfer function meet specification per 115.7.1, per techniques of 115.7.4 and 115.7.5, under spectral distribution and MPD at TP2 per 115.6.3.1	M	Yes [ ]
CH2	Fiber optic channel type II	115.7	Insertion loss is less than 8 dB without in-line connections, and transfer function meet specification per 115.7.2, per techniques of 115.7.4 and 115.7.5, under spectral distribution and MPD at TP2 per 115.6.3.1	M	Yes [ ]
CH3	Fiber optic channel type III	115.7	Insertion loss is less than 3 dB without in-line connections, and transfer function meet specification per 115.7.3, per techniques of 115.7.4 and 115.7.5, under spectral distribution and MPD at TP2 per 115.6.3.1	M	Yes [ ]
CH4	Transfer function with in-line connections	115.7	Meet transfer function specifications of the particular type with in-line connections	M	Yes [ ]
CH5	Insertion loss measurement	115.7.4	Fiber optic channel meets insertion loss per ISO/IEC 14763-3	M	Yes [ ]
CH6	Transfer function measurement	115.7.5	Fiber optic channel meets transfer function per IEC 60793-1-41:2010	M	Yes [ ]

115.14.12 Medium dependent interface (MDI)

Item	Feature	Subclause	Value/Comment	Status	Support
MDI1	MDI receptacle duplex	115.8.1	MDI receptacle provides two separate slots: transmit and receive	RHA:M	Yes [ ]
MDI2	MDI receptacle labeling	115.8.1	MDI receptacle indicate with labeling the slots of the transmitter and the receiver	RHA:M	Yes [ ]
MDI3	MDI receptacle link segment acceptance	115.8.1	MDI receptacle accepts duplex cable compliant with IEC 60794-2-41	RHA:M	Yes [ ]
MDI4	MDI receptacle states	115.8.1	MDI receptacle has open and close states	RHA:M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MDI5	MDI receptacle cable retention	115.8.1	MDI receptacle has a retention mechanism of cable with a retention force of 4 N aligned with the cable insertion in the direction of cable extraction for PE jacket cables	RHA:M	Yes [ ]
MDI6	MDI receptacle cable retention test procedure	115.8.1	MDI receptacle provides a retention force per IEC 61300-2-40 with AOP loss of less than 0.4 dB	RHA:M	Yes [ ]
MDI7	Cutting tool result	115.8.1	Cutting tool provides flat fiber end facets perpendicular to cable axis as specified	RHA:M	Yes [ ]
MDI8	MDI receptacle cable split length indication	115.8.1	MDI receptacle vendor indicates minimum cable split length for suitable connection	RHA:M	Yes [ ]
MDI9	Cable marking	115.8.1	Duplex POF cable has marking on one of the jackets	RHA:M	Yes [ ]

115.14.13 1000BASE-H Operations, Administration, and Maintenance (1000BASE-H OAM) channel

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	STA write of 1000BASE-H OAM message	115.9.1	STA creates a new message to be transmitted per specified steps	BHOAM:M	Yes [ ] N/A [ ]
OC2	STA read of 1000BASE-H OAM message	115.9.3	STA reads a new received message per specified steps	BHOAM:M	Yes [ ] N/A [ ]
OC3	1000BASE-H OAM transmit	115.9.4.2	PHY operation for 1000BASE-H OAM message transmission conforms to Figure 115–42	BHOAM:M	Yes [ ] N/A [ ]
OC4	1000BASE-H OAM receive	115.9.4.3	PHY operation for 1000BASE-H OAM message reception conforms to Figure 115–43	BHOAM:M	Yes [ ] N/A [ ]

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115.14.14 Loopback modes

Item	Feature	Subclause	Value/Comment	Status	Support
LB1	Loopback mode selection	115.10	Selected using bits 3.518.12:10	M	Yes [ ]
LB2	Loopback mode reset	115.10	Default and reset value is no loopback	M	Yes [ ]
LB3	GMII level loopback	115.10	GMII TX looped back to GMII RX	M	Yes [ ]
LB4	PMD interface level loopback	115.10	Transmit path looped back to receive path near PMD service interface, with PCS and PMA operating as in normal mode, and the PMA receive ignoring PMD receive signals	M	Yes [ ]
LB5	Line loopback	115.10	Receive data looped back to transmit path (toward link partner) near GMII interface	M	Yes [ ]

115.14.15 Management Interface

Item	Feature	Subclause	Value/Comment	Status	Support
MI1	1000BASE-RHx management	115.11	Provide Clause 115 management capabilities and functionality provided by referenced Clause 45 registers and bits	M	Yes [ ]
MI2	MDIO registers functionality	115.11	Provide control and status functionalities of MDIO registers	M	Yes [ ]
MI3	MDIO interface mapping	115.11	Implement variable to register mapping as specified in Table 115–18	MDIO:M	Yes [ ] N/A [ ]

115.14.16 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
E1	Temperature class indication	115.12.1	PHY indicates the operating temperature range of Table 115–19 over which their compliance is claimed	M	Yes [ ]
E2	Conformance to IEC 60950-1	115.12.2	For IT and motor vehicle applications	M	Yes [ ]
E3	Conformance to ISO 26262	115.12.2	For motor vehicle applications only, if required by the given application	AE:O	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
E4	Environmental safety	115.12.3	Conform to environmental stresses as specified in 115.12.3	AE:M	Yes [ ] N/A [ ]
E5	Electromagnetic compatibility	115.12.4	Comply with all applicable local and national codes	M	Yes [ ]
E6	EMC requirements	115.12.4	EMC meets specifications per ISO 11452 and CISPR 25 test methods	M	Yes [ ]
E7	Motor vehicle EMC require-ments	115.12.4	Meet motor vehicle EMC requirements as specified in 115.12.4	AE:M	Yes [ ] N/A [ ]
E8	Optical safety	115.12.5	Hazard Level 1 certified under any operating contition	M	Yes [ ]
E9	Optical safety certification	115.12.5	Conformant to IEC 60825-1 and IEC 60825-2	M	Yes [ ]

115.14.17 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DLY1	Delay constraint	115.13	Sum of the transmit and receive data delays does not exceed 6500 bit times	M	Yes [ ]

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116. Introduction to 200 Gb/s and 400 Gb/s networks

116.1 Overview

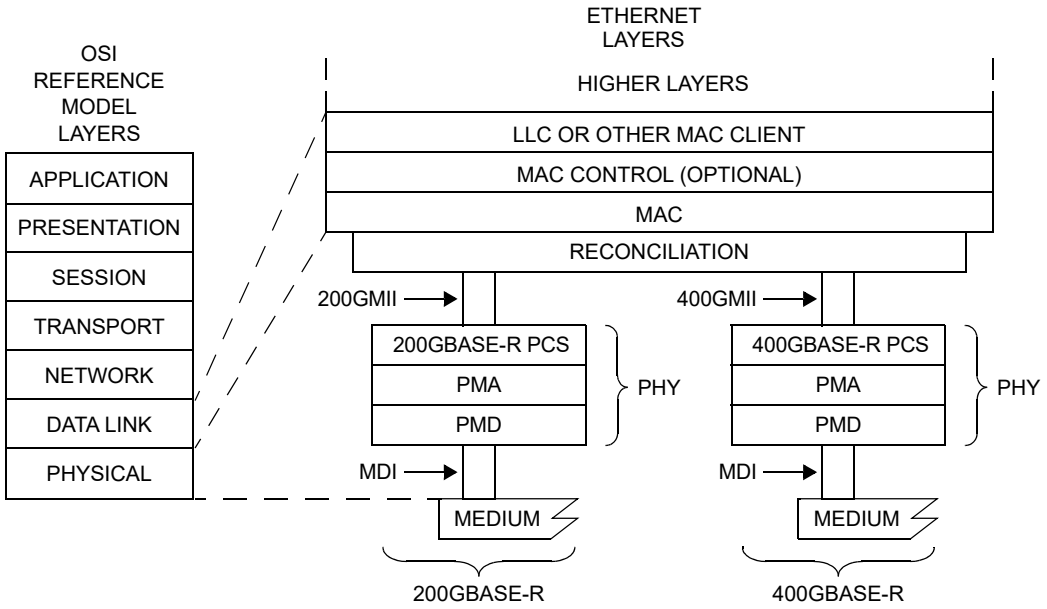
116.1.1 Scope

This clause describes the general requirements for 200 Gigabit and 400 Gigabit Ethernet.

200 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 200 Gb/s, coupled with any IEEE 802.3 200GBASE Physical Layer implementation and is defined for full duplex operation only. 400 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 400 Gb/s, coupled with any IEEE 802.3 400GBASE Physical Layer implementation and is defined for full duplex operation only.

116.1.2 Relationship of 200 Gigabit and 400 Gigabit Ethernet to the ISO OSI reference model

200 Gigabit and 400 Gigabit Ethernet couples the IEEE 802.3 MAC to a family of 200 Gb/s and 400 Gb/s Physical Layer devices. The relationships among 200 Gigabit and 400 Gigabit Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 116–1.



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 116–1—Architectural positioning of 200 Gigabit and 400 Gigabit Ethernet

While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

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a) The 200GMII and 400GMII, which, when implemented as logical interconnection points between the MAC sublayer and the Physical Layer device (PHY), use a 64-bit wide data path as specified in Clause 117. Physical instantiations of this interface may use other data-path widths.

b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.

c) The PMA service interface, which, when physically implemented as 400GAUI-16 (400 Gb/s sixteen-lane Attachment Unit Interface) at an observable interconnection port, uses a 16-lane data path as specified in Annex 120B or Annex 120C.

d) The PMA service interface, which, when physically implemented as 200GAUI-8 (200 Gb/s eight-lane Attachment Unit Interface) or 400GAUI-8 (400 Gb/s eight-lane Attachment Unit Interface) at an observable interconnection port, uses an 8-lane data path as specified in Annex 120B, Annex 120C, Annex 120D, or Annex 120E.

e) The PMA service interface, which, when physically implemented as 200GAUI-4 (200 Gb/s four-lane Attachment Unit Interface) at an observable interconnection port, uses a 4-lane data path as specified in Annex 120D or Annex 120E.

f) The MDI as specified in Clause 123 for 400GBASE-SR16 uses a 16-lane data path.

g) The MDIs as specified in:

— Clause 122 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8
— Clause 138 for 400GBASE-SR8
— Clause 150 for 400GBASE-SR4.2

all use an 8-lane data path.

h) The MDIs as specified in:

— Clause 121 for 200GBASE-DR4
— Clause 122 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4
— Clause 124 for 400GBASE-DR4
— Clause 136 for 200GBASE-CR4
— Clause 137 for 200GBASE-KR4
— Clause 138 for 200GBASE-SR4
— Clause 151 for 400GBASE-FR4 and 400GBASE-LR4-6

all use a 4-lane data path.

116.1.3 Nomenclature

The nomenclature employed by the 200 Gb/s and 400 Gb/s Physical Layer is explained as follows.

The alpha-numeric prefix 200GBASE in the port type (e.g., 200GBASE-R) represents a family of Physical Layer devices operating at a speed of 200 Gb/s. The alpha-numeric prefix 400GBASE in the port type (e.g., 400GBASE-R) represents a family of Physical Layer devices operating at a speed of 400 Gb/s.

200GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer for 200 Gb/s operation over multiple PCS lanes (see Clause 119). Physical Layer devices listed in Table 116–1 are defined for operation at 200 Gb/s.

400GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer for 400 Gb/s operation over multiple PCS lanes (see Clause 119). Physical Layer devices listed in Table 116–2 are defined for operation at 400 Gb/s.

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Table 116–1—200 Gb/s PHYs

Name	Description
200GBASE-KR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of an electrical backplane (see Clause 137)
200GBASE-CR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of twinaxial copper cable (see 1.4.559 and Clause 136)
200GBASE-SR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of multimode fiber (see Clause 138)
200GBASE-DR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of single-mode fiber, with reach up to at least 500 m (see Clause 121)
200GBASE-FR4	200 Gb/s PHY using 200GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 2 km (see Clause 122)
200GBASE-LR4	200 Gb/s PHY using 200GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 10 km (see Clause 122)
200GBASE-ER4	200 Gb/s PHY using 200GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 40 km (see Clause 122)

Table 116–2—400 Gb/s PHYs

Name	Description
400GBASE-SR16	400 Gb/s PHY using 400GBASE-R encoding over sixteen lanes of multimode fiber, with reach up to at least 100 m (see Clause 123)
400GBASE-SR8	400 Gb/s PHY using 400GBASE-R encoding over eight lanes of multimode fiber, with reach up to at least 100 m (see Clause 138)
400GBASE-SR4.2	400 Gb/s PHY using 400GBASE-R encoding over eight lanes on multimode fiber in a bidirectional WDM format, with reach up to at least 150 m (see Clause 150)
400GBASE-DR4	400 Gb/s PHY using 400GBASE-R encoding over four lanes of single-mode fiber, with reach up to at least 500 m (see Clause 124)
400GBASE-FR8	400 Gb/s PHY using 400GBASE-R encoding over eight WDM lanes on single-mode fiber, with reach up to at least 2 km (see Clause 122)
400GBASE-FR4	400 Gb/s PHY using 400GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 2 km (see Clause 151)
400GBASE-LR4-6	400 Gb/s PHY using 400GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 6 km (see Clause 151)
400GBASE-LR8	400 Gb/s PHY using 400GBASE-R encoding over eight WDM lanes on single-mode fiber, with reach up to at least 10 km (see Clause 122)
400GBASE-ER8	400 Gb/s PHY using 400GBASE-R encoding over eight WDM lanes on single-mode fiber, with reach up to at least 40 km (see Clause 122)

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116.1.4 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. Table 116–3, Table 116–4, and Table 116–5 specify the correlation between PHY types and clauses. Implementations conforming to one or more PHY types meet the requirements of the corresponding clauses.

Table 116–3—PHY type and clause correlation (200GBASE copper)

PHY type	Clause[a]										
	73	78	117		118	119	120	120B	120D	136	137
	Auto-Negotiation	EEE	RS	200GMII	200GMII Extender	200GBASE-R PCS	200GBASE-R PMA	200GAUI-8 C2C	200GAUI-4 C2C	200GBASE-CR4 PMD	200GBASE-KR4 PMD
200GBASE-KR4	M	O	M	O	O	M	M	O	O		M
200GBASE-CR4	M	O	M	O	O	M	M	O	O	M	

[a]O = Optional, M = Mandatory.

Table 116–4—PHY type and clause correlation (200GBASE optical)

PHY type	Clause[a]														
	78	117		118	119	120	120B	120C	120D	120E	121	122			138
	EEE	RS	200GMII	200GMII Extender	200GBASE-R PCS	200GBASE-R PMA	200GAUI-8 C2C	200GAUI-8 C2M	200GAUI-4 C2C	200GAUI-4 C2M	200GBASE-DR4 PMD	200GBASE-FR4 PMD	200GBASE-LR4 PMD	200GBASE-ER4 PMD	200GBASE-SR4 PMD
200GBASE-SR4	O	M	O	O	M	M	O	O	O	O					M
200GBASE-DR4	O	M	O	O	M	M	O	O	O	O	M				
200GBASE-FR4	O	M	O	O	M	M	O	O	O	O		M			
200GBASE-LR4	O	M	O	O	M	M	O	O	O	O			M		
200GBASE-ER4	O	M	O	O	M	M	O	O	O	O				M	

[a] O = Optional, M = Mandatory.

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Table 116–5—PHY type and clause correlation (400GBASE optical)

PHY type	Clause[a]																		
	78	117		118	119	120	120B	120C	120D	120E	123	138	150	124	122	151		122	
	EEE	RS	400GMII	400GMII Extender	400GBASE-R PCS	400GBASE-R PMA	400GAUI-16 C2C	400GAUI-16 C2M	400GAUI-8 C2C	400GAUI-8 C2M	400GBASE-SR16 PMD	400GBASE-SR8 PMD	400GBASE-SR4.2 PMD	400GBASE-DR4 PMD	400GBASE-FR8 PMD	400GBASE-FR4 PMD	400GBASE-LR4-6 PMD	400GBASE-LR8 PMD	400GBASE-ER8 PMD
400GBASE-SR16	O	M	O	O	M	M	O	O	O	O	M								
400GBASE-SR8	O	M	O	O	M	M	O	O	O	O		M							
400GBASE-SR4.2	O	M	O	O	M	M	O	O	O	O			M						
400GBASE-DR4	O	M	O	O	M	M	O	O	O	O				M					
400GBASE-FR8	O	M	O	O	M	M	O	O	O	O					M				
400GBASE-FR4	O	M	O	O	M	M	O	O	O	O						M			
400GBASE-LR4-6	O	M	O	O	M	M	O	O	O	O							M		
400GBASE-LR8	O	M	O	O	M	M	O	O	O	O								M	
400GBASE-ER8	O	M	O	O	M	M	O	O	O	O									M

[a] O = Optional, M = Mandatory.

116.2 Summary of 200 Gigabit and 400 Gigabit Ethernet sublayers

116.2.1 Reconciliation Sublayer (RS) and Media Independent Interface

The Media Independent Interface (Clause 117) provides a logical interconnection between the MAC sublayer and Physical Layer devices (PHYs). The Media Independent Interface is not intended to be physically instantiated, rather it can logically connect layers within a device.

The 200GMII supports 200 Gb/s operation and the 400GMII supports 400 Gb/s operation through its 64-bit-wide transmit and receive data paths. The Reconciliation Sublayer (RS) provides a mapping between the signals provided at the Media Independent Interface (200GMII and 400GMII) and the MAC/PLS service definition.

While the 200GMII and 400GMII are optional interfaces, they are used extensively in this standard as a basis for functional specification and provides a common service interface for the physical coding sublayer defined in Clause 119.

116.2.2 200GMII and 400GMII Extender Sublayers (200GXS and 400GXS)

The 200 Gigabit 200GMII Extender Sublayer (200GXS) is part of the 200GMII Extender (Clause 118). It is identical in function to the 200GBASE-R PCS in Clause 119 with the exceptions defined in Clause 118. The 400 Gigabit 400GMII Extender Sublayer (400GXS) is part of the 400GMII Extender (Clause 118). It is identical in function to the 400GBASE-R PCS in Clause 119 with the exceptions defined in Clause 118.

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The optional 200GMII Extender (Clause 118) can be inserted between the Reconciliation Sublayer and the PHY to transparently extend the reach of the 200GMII. The optional 400GMII Extender (Clause 118) can be inserted between the Reconciliation Sublayer and the PHY to transparently extend the reach of the 400GMII.

116.2.3 Physical Coding Sublayer (PCS)

The terms 200GBASE-R and 400GBASE-R refer to a specific family of Physical Layer implementations based upon the 64B/66B data coding method specified in Clause 119 and the PMA specifications defined in Clause 120. Clause 119 PCSs perform encoding (decoding) of data from (to) the 200GMII or 400GMII to 256B/257B code blocks, apply FEC, distribute the data to multiple lanes, and transfer the encoded data to the PMA.

The 200GBASE-R PCS has almost the same functionality as the 200GXS, and therefore may be configured as a 200GXS in order to implement part of the optional 200GMII Extender (see Clause 118). The 400GBASE-R PCS has almost the same functionality as the 400GXS, and therefore may be configured as a 400GXS in order to implement part of the optional 400GMII Extender (see Clause 118).

116.2.4 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS to support the use of a range of physical media. The 200GBASE-R and 400GBASE-R PMAs perform the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface, and the mapping and multiplexing of transmit and receive data streams between the PMA and PMD via the PMD service interface. In addition, the PMA performs retiming of the received data stream when appropriate, optionally provides data loopback at the PMA or PMD service interface, and optionally provides test pattern generation and checking.

The 200GBASE-R and 400GBASE-R PMAs are specified in Clause 120.

116.2.5 Physical Medium Dependent (PMD) sublayer

The Physical Medium Dependent sublayer is responsible for interfacing to the transmission medium. The PMD is located just above the Medium Dependent Interface (MDI). The MDI, logically subsumed within each PMD subclause, is the actual medium attachment for the various supported media.

The 200GBASE-R PMDs and their corresponding media are specified in Clause 121, Clause 122, and Clause 136 through Clause 138. The 400GBASE-R PMDs and their corresponding media are specified in Clause 122 through Clause 124, Clause 138, and Clause 150.

116.2.6 Management interface (MDIO/MDC)

The optional MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMDs) and Station Management (STA) entities.

116.2.7 Management

Managed objects, attributes, and actions are defined for all 200 Gigabit and 400 Gigabit Ethernet components. These items are defined in Clause 30.

116.3 Service interface specification method and notation

The service interface specification for the 200GBASE-R and 400GBASE-R Physical Layers is as per the definition in 1.2.2. Note that the 200GBASE-R and 400GBASE-R inter-sublayer service interfaces use

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multiple scalar REQUEST and INDICATION primitives, to indicate the transfer of multiple independent streams of data units, as defined in 116.3.1 through 116.3.3.

116.3.1 Inter-sublayer service interface

The inter-sublayer service interface is described in an abstract manner and does not imply any particular implementation. The inter-sublayer service interface primitives are defined as follows:

IS_UNITDATA_*i*.request
IS_UNITDATA_*i*.indication
IS_SIGNAL.indication

The IS_UNITDATA_*i*.request (where $i = 0$ to n – 1, and n is the number of streams of data units) primitive is used to define the transfer of multiple streams of data units from a sublayer to the next lower (closer to the medium) sublayer. The IS_UNITDATA_*i*.indication (where $i = 0$ to n – 1, and n is the number of streams of data units) primitive is used to define the transfer of multiple streams of data units from a sublayer to the next higher (closer to the MAC) sublayer. The IS_SIGNAL.indication primitive is used to define the transfer of signal status from a sublayer to the next higher sublayer.

116.3.2 Instances of the Inter-sublayer service interface

The inter-sublayer interface can be instantiated between different sublayers, hence a prefix notation is defined to identify a specific instance of an inter-sublayer service interface. The following prefixes are defined:

a) PMD:—for primitives issued on the interface between the PMD sublayer and the PMA sublayer called the PMD service interface.
b) PMA:—for primitives issued on the interface between the PMA sublayer and the PCS, DTE 200GXS, DTE 400GXS, or PMA sublayer above called the PMA service interface.
c) PHY XS:—for primitives issued on the interface between the PMA sublayer and the PHY 200GXS sublayer or PHY 400GXS sublayer called the PHY XS service interface.

Examples of inter-sublayer service interfaces for 200GBASE-R and 400GBASE-R with their corresponding instance names are illustrated in Figure 116–2 and Figure 116–3, respectively. For example, the primitives for one instance of the inter-sublayer service interface, named the PMD service interface, are identified as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication.

Primitives for other instances, of inter-sublayer interfaces, are represented in a similar manner as described above.

116.3.3 Semantics of inter-sublayer service interface primitives

The semantics of the inter-sublayer service interface primitives for the 200GBASE-R and 400GBASE-R sublayers are described in 116.3.3.1 through 116.3.3.3.

116.3.3.1 IS_UNITDATA_*i*.request

The IS_UNITDATA_*i*.request (where $i = 0$ to n – 1) primitive is used to define the transfer of multiple streams of data units from a sublayer to the next lower sublayer, where n is the number of parallel streams of data units.

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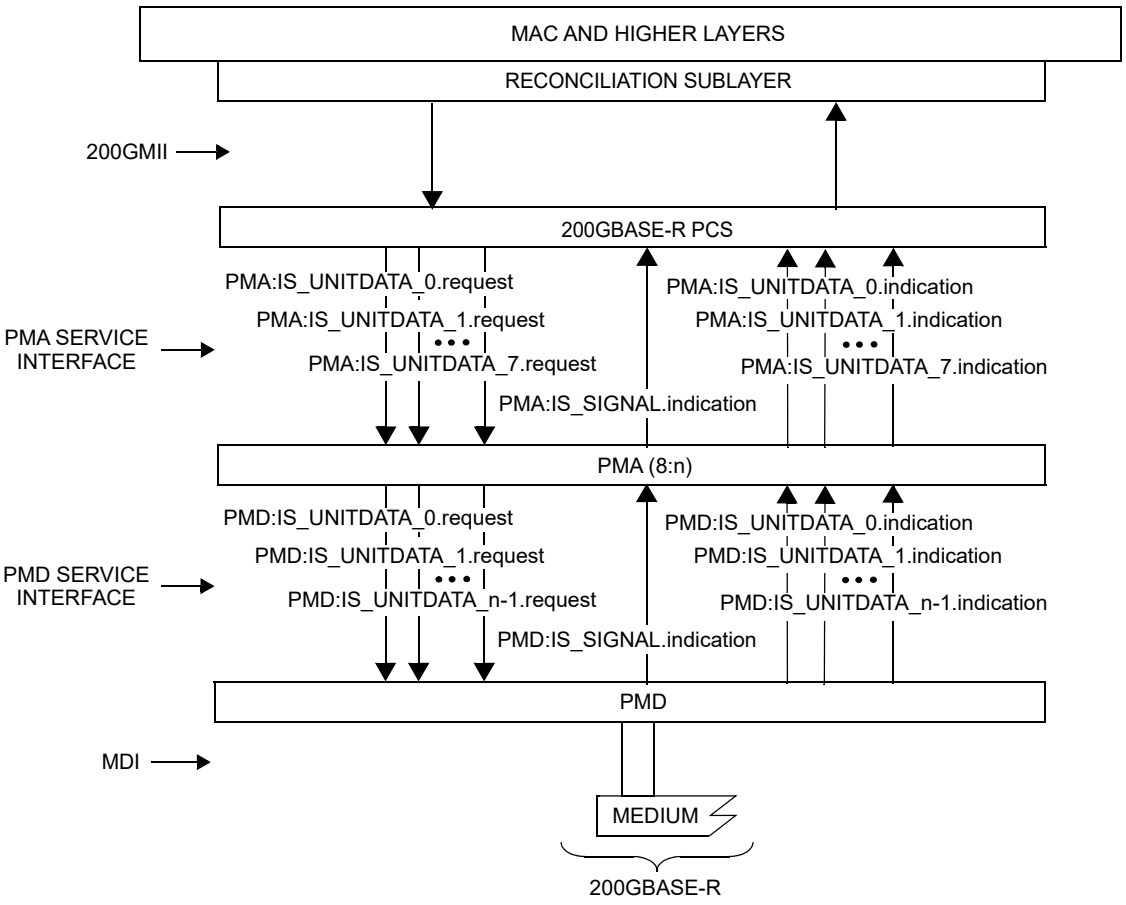

200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = NUMBER OF PARALLEL STREAMS OF DATA UNITS

Figure 116–2—200GBASE-R inter-sublayer service interfaces

116.3.3.1.1 Semantics of the service primitive

IS_UNITDATA_0.request(tx_symbol)
IS_UNITDATA_1.request(tx_symbol)
...
IS_UNITDATA_n–1.request(tx_symbol)

The data conveyed by IS_UNITDATA_0.request to IS_UNITDATA_n–1.request consists of n parallel continuous streams of encoded symbols, one stream for each lane. Depending on the specific instance of the inter-sublayer service interface each of the tx_symbol parameters can either take one of two values: zero or one; or take one of four values: zero, one, two, or three.

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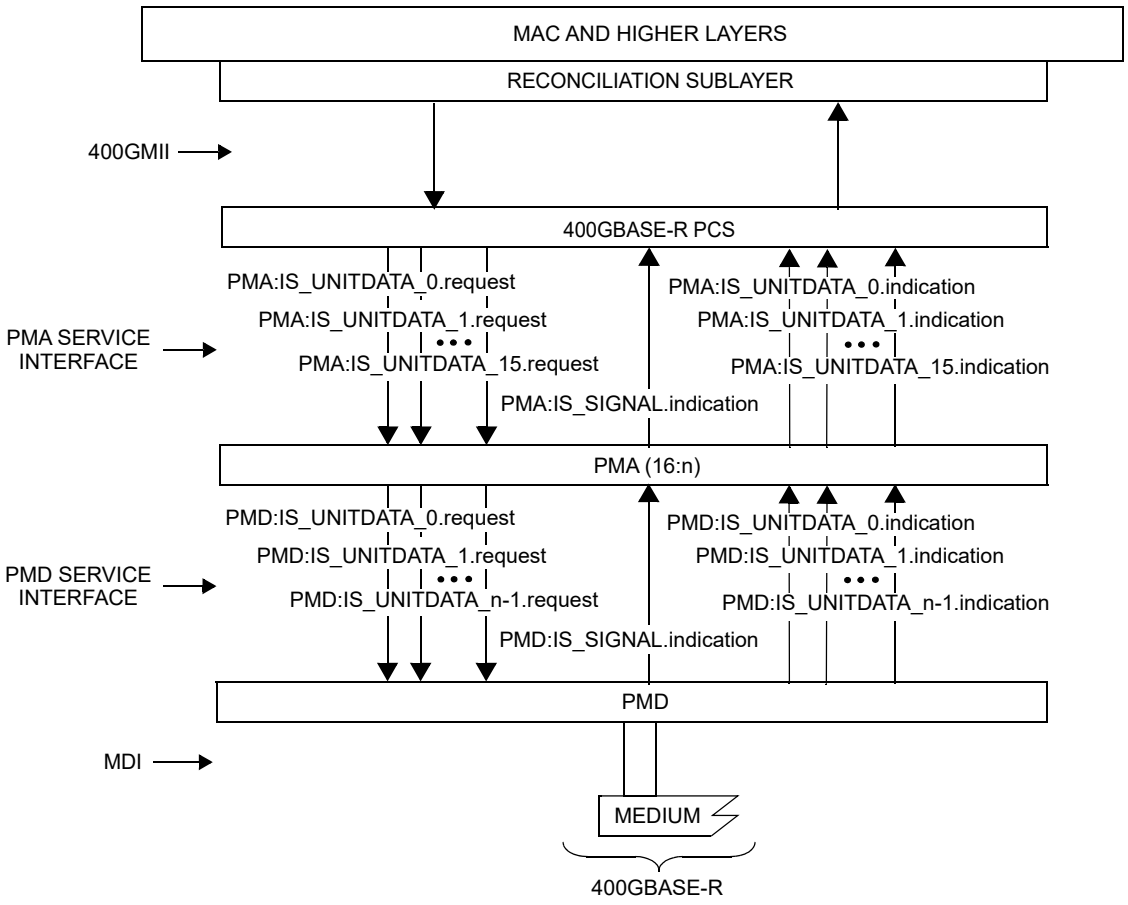

400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = NUMBER OF PARALLEL STREAMS OF DATA UNITS

Figure 116–3—400GBASE-R inter-sublayer service interfaces

116.3.3.1.2 When generated

The sublayer continuously sends n parallel symbol streams IS_UNITDATA_*i*.request(tx_symbol) to the next lower sublayer, each at a nominal signaling rate defined by a specific instance of the inter-sublayer service interface.

116.3.3.1.3 Effect of receipt

The effect of receipt of this primitive is defined by the sublayer that receives this primitive.

116.3.3.2 IS_UNITDATA_*i*.indication

The IS_UNITDATA_*i*.indication (where i = 0 to n – 1) primitive is used to define the transfer of multiple streams of data units from the sublayer to the next higher sublayer, where n is the number of parallel streams of data units.

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116.3.3.2.1 Semantics of the service primitive

IS_UNITDATA_0.indication(rx_symbol)
IS_UNITDATA_1.indication(rx_symbol)
...
IS_UNITDATA_n–1.indication(rx_symbol)

The data conveyed by IS_UNITDATA_0.indication to IS_UNITDATA_n–1.indication consists of n parallel continuous streams of encoded symbols, one stream for each lane. Depending on the specific instance of the inter-sublayer service interface each of the rx_symbol parameters can either take one of two values: zero or one; or take one of four values: zero, one, two, or three.

116.3.3.2.2 When generated

The sublayer continuously sends n parallel symbol streams IS_UNITDATA_*i*.indication(rx_symbol) to the next higher sublayer, each at a nominal signaling rate defined by a specific instance of the inter-sublayer service interface.

116.3.3.2.3 Effect of receipt

The effect of receipt of this primitive is defined by the sublayer that receives this primitive.

116.3.3.3 IS_SIGNAL.indication

The IS_SIGNAL.indication primitive is generated by the sublayer to the next higher sublayer to indicate the status of the receive process. This primitive is generated by the receive process to propagate the detection of severe error conditions (e.g., no valid signal being received by the sublayer that generates this primitive) to the next higher sublayer.

116.3.3.3.1 Semantics of the service primitive

IS_SIGNAL.indication(SIGNAL_OK)

The SIGNAL_OK parameter can take on one of two values: OK or FAIL. A value of FAIL denotes that invalid data is being presented (rx_symbol parameters undefined) by the sublayer to the next higher sublayer. A value of OK does not guarantee valid data is being presented by the sublayer to the next higher sublayer.

116.3.3.3.2 When generated

The sublayer generates the IS_SIGNAL.indication primitive to the next higher sublayer whenever there is change in the value of the SIGNAL_OK parameter.

116.3.3.3.3 Effect of receipt

The effect of receipt of this primitive is defined by the sublayer that receives this primitive.

116.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

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Table 116–6 and Table 116–7 contain the values of maximum sublayer delay (sum of transmit and receive delays at one end of the link) in bit times as specified in 1.4 and pause_quanta as specified in 31B.2 for 200 Gigabit and 400 Gigabit Ethernet, respectively. If a PHY contains an Auto-Negotiation sublayer, the delay of the Auto-Negotiation sublayer is included within the delay of the PMD and medium.

Table 116–6—Sublayer delay constraints (200GBASE)

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
200G MAC, RS, and MAC Control	49 152	96	245.76	See 117.1.4.
200GBASE-R PCS or 200GXS[d]	160 256	313	801.28	See 119.5.
200GBASE-R PMA	18 432	36	92.16	See 120.5.4.
200GBASE-KR4 PMD	8 192	16	40.96	Includes allocation of 20 ns for one direction through backplane medium. See 137.5.
200GBASE-CR4 PMD	8 192	16	40.96	Includes allocation of 20 ns for one direction through cable medium. See 137.5.
200GBASE-SR4 PMD	4 096	8	20.48	See 138.3.
200GBASE-DR4 PMD	4 096	8	20.48	Includes 2 m of fiber. See 121.3.1.
200GBASE-FR4 PMD	4 096	8	20.48	Includes 2 m of fiber. See 122.3.1.
200GBASE-LR4 PMD	4 096	8	20.48	Includes 2 m of fiber. See 122.3.1.
200GBASE-ER4 PMD	4 096	8	20.48	Includes 2 m of fiber. See 122.3.1.

[a] For 200GBASE-R, 1 bit time (BT) is equal to 5 ps. (See 1.4.215 for the definition of bit time.)
[b] For 200GBASE-R, 1 pause_quantum is equal to 2.56 ns. (See 31B.2 for the definition of pause_quanta.)
[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.
[d] If an implementation includes the 200GMII extender, the delay associated with the 200GMII extender includes two 200GXS sublayers.

Table 116–7—Sublayer delay constraints (400GBASE)

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
400G MAC, RS, and MAC Control	98 304	192	245.76	See 117.1.4.
400GBASE-R PCS or 400GXS[d]	320 000	625	800	See 119.5.
400GBASE-R PMA	36 864	72	92.16	See 120.5.4.
400GBASE-SR16 PMD	8 192	16	20.48	Includes 2 m of fiber. See 123.3.1.
400GBASE-SR8 PMD	8 192	16	20.48	Includes 2 m of fiber. See 138.3.1.
400GBASE-SR4.2 PMD	8 192	16	20.48	Includes 2 m of fiber. See 150.3.1.
400GBASE-DR4 PMD	8 192	16	20.48	Includes 2 m of fiber. See 124.3.1.

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Table 116–7—Sublayer delay constraints (400GBASE) *(continued)*

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
400GBASE-FR8 PMD	8 192	16	20.48	Includes 2 m of fiber. See 122.3.1.
400GBASE-FR4 PMD	8 192	16	20.48	Includes 2 m of fiber. See 151.3.1.
400GBASE-LR4-6 PMD	8 192	16	20.48	Includes 2 m of fiber. See 151.3.1.
400GBASE-LR8 PMD	8 192	16	20.48	Includes 2 m of fiber. See 122.3.1.
400GBASE-ER8 PMD	8 192	16	20.48	Includes 2 m of fiber. See 122.3.1.

[a] For 400GBASE-R, 1 bit time (BT) is equal to 2.5 ps. (See 1.4.215 for the definition of bit time.)
[b] For 400GBASE-R, 1 pause_quantum is equal to 1.28 ns. (See 31B.2 for the definition of pause_quanta.)
[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.
[d] If an implementation includes the 400GMII extender, the delay associated with the 400GMII extender includes two 400GXS sublayers.

See 80.4 for the calculation of bit time per meter of fiber or electrical cable.

See 31B.3.7 for PAUSE reaction timing constraints for stations at operating speeds of 200 Gb/s and 400 Gb/s.

116.5 Skew constraints

Skew (or relative delay) can be introduced between lanes by both active and passive elements of a 200GBASE-R or 400GBASE-R link. Skew is defined as the difference between the times of the earliest PCS lane and latest PCS lane for the one to zero transition of the alignment marker sync bits. The PCS deskew function (see 119.2.5.1) compensates for all lane-to-lane Skew observed at the receiver. The Skew between the lanes is kept within limits as shown in Table 116–8 so that the transmitted information on the lanes can be reassembled by the receive PCS.

Skew Variation may be introduced due to variations in electrical, thermal or environmental characteristics. Skew Variation is defined as the change in Skew between any PCS lane and any other PCS lane over the entire time that the link is in operation. From the time the link is brought up, Skew Variation is limited so that each PCS lane always traverses the same lane between any pair of adjacent sublayers while the link remains in operation.

The maximum Skew and Skew Variation at physically instantiated interfaces is specified at Skew points SP1, SP2, and SP3 for the transmit direction and SP4, SP5, and SP6 for the receive direction as illustrated in Figure 116–4 (single 200GAUI-n or 400GAUI-n interface) and Figure 116–5 (multiple 200GAUI-n or 400GAUI-n interfaces).

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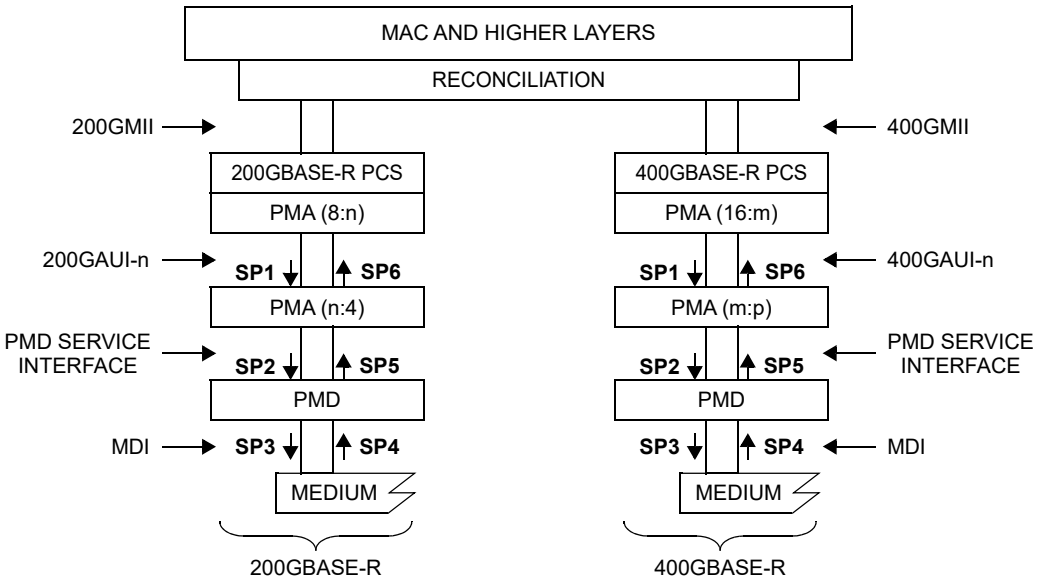

200GAUI-n = 200 Gb/s ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GAUI-n = 400 Gb/s ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = 8 or 4
m = 16 or 8
p = 16, 8, or 4

Figure 116–4—200GBASE-R and 400GBASE-R Skew points for single 200GAUI-n or 400GAUI-n

In the transmit direction, the Skew points are defined in the following locations:

— SP1 on the 200GAUI-n/400GAUI-n interface, at the input of the PMA closest to the PMD;
— SP2 on the PMD service interface, at the input of the PMD;
— SP3 at the output of the PMD, at the MDI.

In the receive direction, the Skew points are defined in the following locations:

— SP4 at the MDI, at the input of the PMD;
— SP5 on the PMD service interface, at the output of the PMD;
— SP6 on the 200GAUI-n/400GAUI-n interface, at the output of the PMA closest to the 200GBASE-R/400GBASE-R PCS or DTE 200GXS/400GXS.

The allowable limits for Skew are shown in Table 116–8 and the allowable limits for Skew Variation are shown in Table 116–9.

The Skew requirements for the PCS, PMA and PMD sublayers are specified in the respective clauses as noted in Table 116–8 and Table 116–9.

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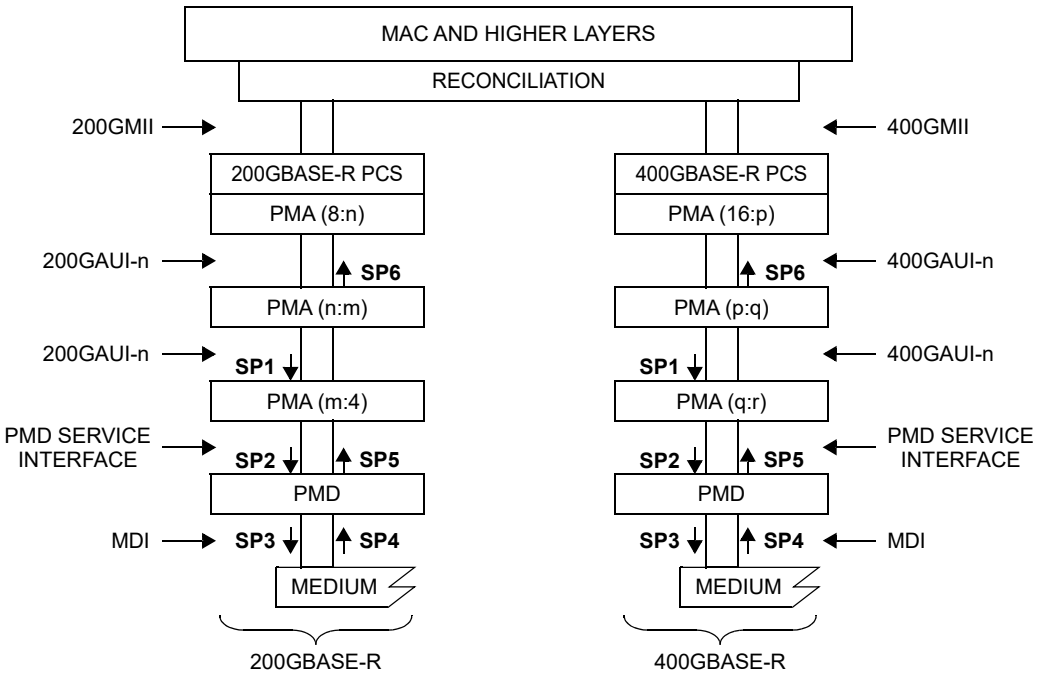

200GAUI-n = 200 Gb/s ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GAUI-n = 400 Gb/s ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = 8 or 4
m = 8 or 4
p = 16 or 8
q = 16 or 8
r = 16, 8, or 4

Figure 116–5—200GBASE-R and 400GBASE-R Skew points for multiple 200GAUI-n or 400GAUI-n

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Table 116–8—Summary of Skew constraints

Skew points	Maximum Skew (ns)[a]	Maximum Skew for 200GBASE-R or 400GBASE-R PCS lane (UI)[b]	Notes[c]
SP1	29	≈ 770	See 120.5.3.1
SP2	43	≈ 1142	See 120.5.3.3, 121.3.2, 122.3.2, 123.3.2, 124.3.2, 136.6.2, 137.6.2, 138.3.2.2, 150.3.2, or 151.3.2
SP3	54	≈ 1434	See 121.3.2, 122.3.2, 123.3.2, 124.3.2, 136.6.2, 137.6.2, 138.3.2.2, 150.3.2, or 151.3.2
SP4	134	≈ 3559	See 121.3.2, 122.3.2, 123.3.2, 124.3.2, 136.6.2, 137.6.2, 138.3.2.2, 150.3.2, or 151.3.2
SP5	145	≈ 3852	See 121.3.2, 122.3.2, 123.3.2, 124.3.2, 136.6.2, 137.6.2, 138.3.2.2, 150.3.2, or 151.3.2
SP6	160	≈ 4250	See 120.5.3.5
At PCS receive	180	≈ 4781	See 119.2.5.1

[a] The Skew limit includes 1 ns allowance for PCB traces that are associated with the Skew points.
[b] The symbol ≈ indicates approximate equivalent of maximum Skew in UI based on 1 UI equals 37.64706 ps at PCS lane signaling rate of 26.5625 GBd.
[c] Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

Table 116–9—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation (ns)	Maximum Skew Variation for 26.5625 GBd PMD lane (UI)[a]	Maximum Skew Variation for 53.125 GBd PMD lane (UI)[b]	Notes[c]
SP1	0.2	≈ 5	N/A	See 120.5.3.1
SP2	0.4	≈ 11	≈ 21	See 120.5.3.3, 121.3.2, 122.3.2, 123.3.2, 124.3.2, 136.6.2, 137.6.2, 138.3.2.2, 150.3.2, or 151.3.2
SP3	0.6	≈ 16	≈ 32	See 121.3.2, 122.3.2, 123.3.2, 124.3.2, 136.6.2, 137.6.2, 138.3.2.2, 150.3.2, or 151.3.2
SP4	3.4	≈ 90	≈ 181	See 121.3.2, 122.3.2, 123.3.2, 124.3.2, 136.6.2, 137.6.2, 138.3.2.2, 150.3.2, or 151.3.2
SP5	3.6	≈ 96	≈ 191	See 121.3.2, 122.3.2, 123.3.2, 124.3.2, 136.6.2, 137.6.2, 138.3.2.2, 150.3.2, or 151.3.2
SP6	3.8	≈ 101	N/A	See 120.5.3.5
At PCS receive	4	≈ 106	N/A	See 119.2.5.1

[a] The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI based on 1 UI equals 37.64706 ps at PMD lane signaling rate of 26.5625 GBd.

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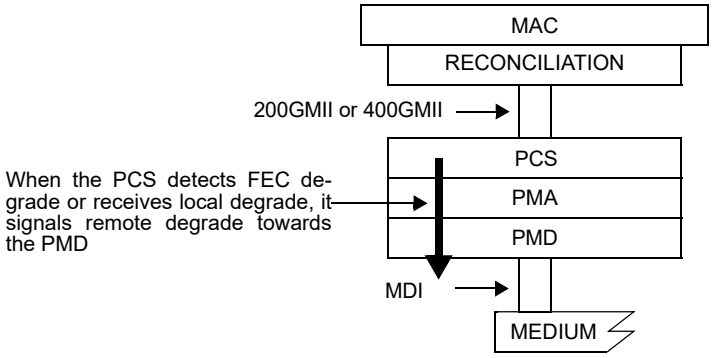
[b] The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI based on 1 UI equals 18.82353 ps at PMD lane signaling rate of 53.125 GBd.
[c] Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

116.6 FEC Degrade

FEC degrade is a feature allowing for the optional detection of a non-service affecting link degradation condition based on exceeding a threshold for FEC corrected errors. If there are multiple FEC decoders in a given direction of transmission between the MAC sublayers at each end of the link, a Local Degrade condition is cascaded in that direction of transmission to convey the fact that one or more FEC decoders in the path have exceeded their threshold of FEC corrected errors. If any FEC decoder in a given direction of transmission exceeds its provisioned threshold for FEC corrected errors, a Remote Degrade condition is indicated in the opposite direction of transmission from the PCS or XS closest to the MAC.

Figure 116–6 illustrates the signaling of the Remote Degraded condition in the case that there is no Clause 118 extender sublayer present between the MAC and the PCS. Note that the PCS will not initiate the signaling for local degrade in this configuration as there are no additional FEC decoders in the receive direction between the PCS and the MAC.



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 116–6—Remote Degrade signaling without Extender Sublayer

Figure 116–7 illustrates the signaling of the Local Degraded condition in the case that a Clause 118 extender sublayer is present between the MAC and the PCS.

Figure 116–8 illustrates the signaling of the Remote Degraded condition in the case that a Clause 118 extender sublayer is present between the MAC and the PCS.

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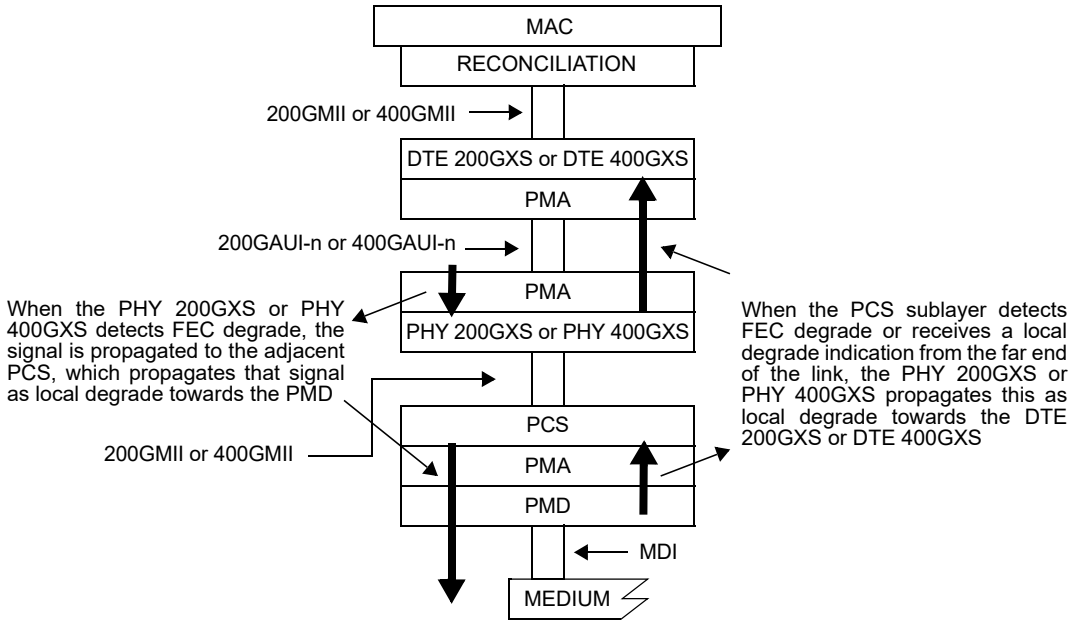

200GAUI-n = 200 Gb/s n-LANE ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
200GXS = 200GMII EXTENDER SUBLAYER
400GAUI-n = 400 Gb/s n-LANE ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
400GXS = 400GMII EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 116–7—Local Degrade Signaling with Extender Sublayer

116.7 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

Multiple states of a function that have a transition to a common state utilizing different qualifiers (for example, multiple exit conditions to an IDLE or WAIT state) may be indicated by a shared arrow. An exit transition arrow connects to the shared arrow, and the qualifier is met prior to termination of the transition arrow on the shared arrow. The shared arrow has no qualifier.

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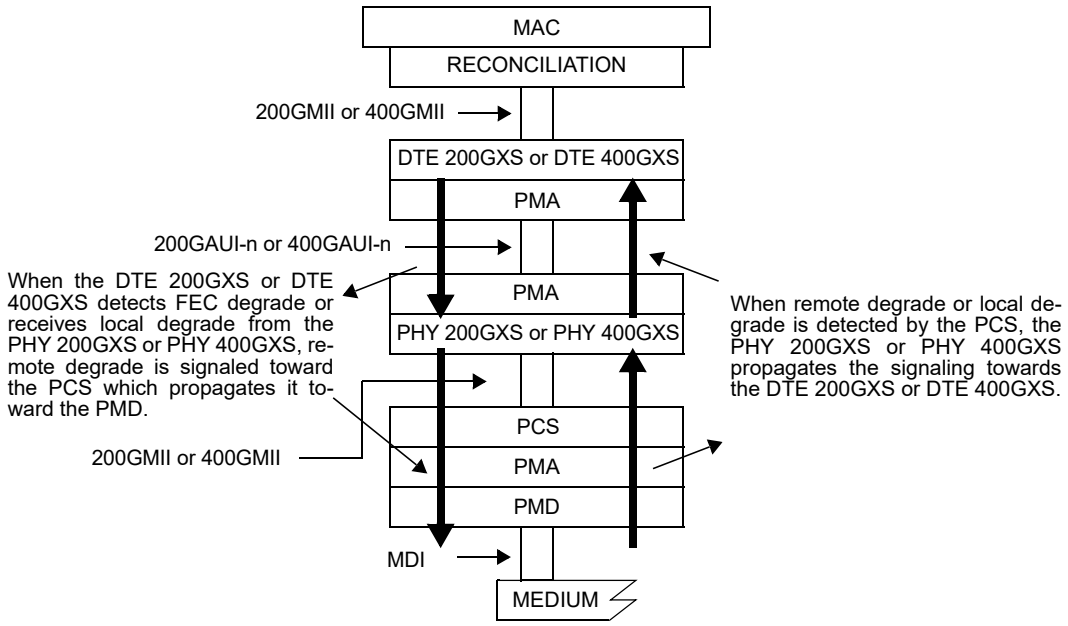

200GAUI-n = 200 Gb/s n-LANE ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
200GXS = 200GMII EXTENDER SUBLAYER
400GAUI-n = 400 Gb/s n-LANE ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
400GXS = 400GMII EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 116–8—Remote Degrade signaling with Extender Sublayer

116.8 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 117 through Clause 124, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the 200 Gigabit and 400 Gigabit Ethernet PICS conforms to the same notation and conventions used in 21.6.

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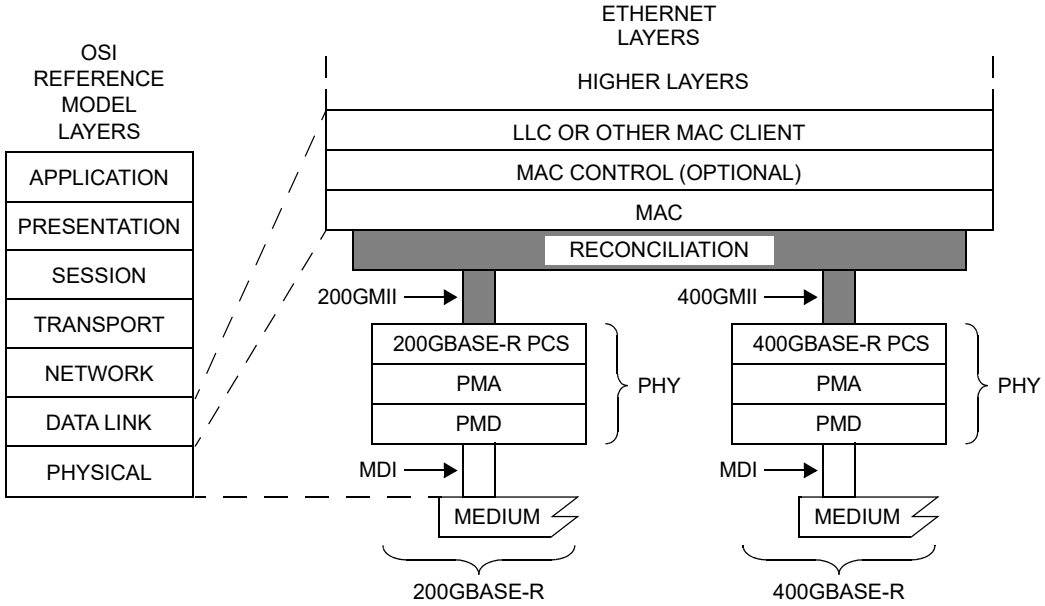
117. Reconciliation Sublayer (RS) and Media Independent Interface for 200 Gb/s and 400 Gb/s operation (200GMII and 400GMII)

117.1 Overview

This clause defines the characteristics of the Reconciliation Sublayer (RS) and the Media Independent Interface between Ethernet media access controllers and various PHYs. Figure 117–1 shows the relationship of the RS and Media Independent Interface to the ISO/IEC OSI reference model.



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 117–1—RS and MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

The 200GMII and the 400GMII are optional logical interfaces between the MAC sublayer and the Physical Layer device (PHY). The 200GXS/400GXS sublayer in conjunction with the 200GAUI-n/400GAUI-n interface may be used to optionally extend the 200GMII/400GMII.

The RS adapts the bit serial protocols of the MAC to the parallel format of the PCS service interface. Though the 200GMII and 400GMII are optional interfaces, they are used in this standard as a basis for specification. The Physical Coding Sublayer (PCS) is specified to the 200GMII/400GMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and 200GMII/400GMII were implemented.

The 200GMII/400GMII have the following characteristics:

a) The 200GMII supports a speed of 200 Gb/s.
b) The 400GMII supports a speed of 400 Gb/s.

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c) Data and delimiters are synchronous to a clock reference.

d) They provide independent 64-bit wide transmit and receive data paths.

e) They support full duplex operation only.

117.1.1 Summary of major concepts

The following are the major concepts of the 200GMII/400GMII:

a) The 200GMII/400GMII are functionally similar to other media independent interfaces that have been defined for lower speeds, as they all define an interface allowing independent development of MAC and PHY logic.

b) The RS converts between the MAC serial data stream and the parallel data paths of the 200GMII/400GMII.

c) The RS maps the signal set provided at the 200GMII/400GMII to the PLS service primitives provided at the MAC.

d) Each direction of data transfer is independent and serviced by data, control, and clock signals.

e) The RS generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.

f) The RS participates in link fault detection and reporting by monitoring the receive path for status reports that indicate an unreliable link, and generating status reports on the transmit path to report detected link faults to the DTE on the remote end of the connecting link.

g) The 200GMII/400GMII may also support Low Power Idle (LPI) signaling for PHY types supporting Energy Efficient Ethernet (EEE) (see Clause 78).

h) The 200GMII/400GMII can be extended through the use of a pair of 200GXS/400GXS sublayers (DTE XS and PHY XS) with a 200GAUI-n/400GAUI-n between them.

117.1.2 Application

This clause applies to the interface between the MAC and PHY. This logical interface is used to provide media independence so that an identical media access controller may be used with supported PHY types.

117.1.3 Rate of operation

The 200GMII is specified to support 200 Gb/s operation. The 400GMII is specified to support 400 Gb/s operation.

117.1.4 Delay constraints

The maximum cumulative MAC Control, MAC, and RS delay (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 117–1. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 116.4 and its references.

Table 117–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
200 Gb/s MAC, RS, and MAC Control	49 152	96	245.76
400 Gb/s MAC, RS, and MAC Control	98 304	192	245.76

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117.1.5 Allocation of functions

The allocation of functions at the 200GMII/400GMII balances the need for media independence with interface simplicity. The 200GMII/400GMII provides media independence by separating the Data Link and Physical Layers of the OSI seven-layer reference model.

117.1.6 200GMII/400GMII structure

The 200GMII/400GMII structure is identical to the CGMII structure specified in 81.1.6.

117.1.7 Mapping of 200GMII/400GMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the 200GMII/400GMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at either 200 Gb/s or 400 Gb/s, therefore, PLS service primitives supporting CSMA/CD operation are not mapped through the RS to the 200GMII/400GMII. This behavior and restrictions are the same as described in 22.7, with the details of the signaling described in 117.3. LPI_REQUEST shall not be set to ASSERT unless the attached link has been operational for at least one second (i.e., link_status = OK, according to the underlying PCS/PMA).

EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission until the system returns from its low power state.

Mappings for the following primitives are defined for 200 Gb/s and 400 Gb/s operation:

PLS_DATA.request
PLS_DATA.indication
PLS_CARRIER.indication
PLS_SIGNAL.indication
PLS_DATA_VALID.indication

The RS maps all primitives in an identical manner as the CGMII does and as specified in 81.1.7.

117.2 200GMII/400GMII data stream

The 200GMII/400GMII data stream has the same characteristics as the CGMII data stream described in 81.2.

117.3 200GMII/400GMII functional specifications

The 200GMII/400GMII functions identically to the CGMII specified in 81.3.

117.4 LPI Assertion and Detection

LPI assertion and detection function identically to the CGMII specified in 81.4, with the single exception that the PMA stop signaling described in 81.4.4 is not applicable.

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117.5 Protocol implementation conformance statement (PICS) proforma for Clause 117, Reconciliation Sublayer (RS) and Media Independent Interface for 200 Gb/s and 400 Gb/s operation (200GMII and 400GMII)[204]

117.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 117, Reconciliation Sublayer (RS) and Media Independent Interface for 200 Gb/s and 400 Gb/s operation (200GMII and 400GMII), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

117.5.2 Identification

117.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

117.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 117, Reconciliation Sublayer (RS) and Media Independent Interface for 200 Gb/s and 400 Gb/s operation (200GMII and 400GMII)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[204]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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117.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*MII	PHY support of either 200GMII or 400GMII	117.2, 117.3		O	Yes [ ] No [ ]
*LPI	Implementation of LPI	117.1.7		O	Yes [ ] No [ ]

117.5.4 PICS proforma tables for Reconciliation Sublayer (RS) and Media Independent Interface for 200 Gb/s and 400 Gb/s operation (200GMII and 400GMII)

117.5.4.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	Cumulative MAC Control, MAC and RS delay	117.1.4	Per Table 117–1	M	Yes [ ]
G3	Lane structure	117.1.6	Per Table 81–2	M	Yes [ ]

117.5.4.2 Mapping of PLS service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
PL1	Mapping to Clause 6	117.1.7	RS implements mapping to Clause 6 PLS service primitives	MII:M	Yes [ ] N/A [ ]
PL2	Mapping of PLS_DATA.requests	117.1.7	In sequence TXD<0> to TXD<63>	MII:M	Yes [ ] N/A [ ]
PL3	Start control character creation	117.1.7	First octet of preamble converted to Start control character	MII:M	Yes [ ] N/A [ ]
PL4	TXD and TXC generation	117.1.7	For each 64 PLS_DATA.requests	MII:M	Yes [ ] N/A [ ]
PL5	Terminate control character creation	117.1.7	DATA_COMPLETE causes creation of Terminate control character in next lane in sequence	MII:M	Yes [ ] N/A [ ]
PL6	Mapping RXD to PLS_DATA.indications	117.1.7	Create PLS_DATA.indications in sequence from RXD<0> to RXD<63>	MII:M	Yes [ ] N/A [ ]
PL7	PLS_DATA.indication generation	117.1.7	Generate 64 PLS_DATA.indications for each RXD<63:0> until Terminate then generating 0, 8, 16, 24, 32, 40, 48, or 56	MII:M	Yes [ ] N/A [ ]
PL8	Start control character conversion	117.1.7	Convert valid Start control character to preamble before generating PLS_DATA.indications	MII:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PL9	Terminate control character	117.1.7	No PLS_DATA.indications generated	MII:M	Yes [ ] N/A [ ]
PL10	PLS_DATA_VALID.indication generation	117.1.7	On change of value of DATA_VALID_STATUS	MII:M	Yes [ ] N/A [ ]
PL11	DATA_VALID_STATUS	117.1.7	Value of DATA_VALID on a lane 0 Start control character preceded by eight idles, a Sequence ordered set, or a Terminate character	MII:M	Yes [ ] N/A [ ]
PL12	DATA_VALID_STATUS	117.1.7	Value of DATA_NOT_VALID on any control character but Error	MII:M	Yes [ ] N/A [ ]
PL13	Frame not ending with Terminate control character	117.1.7	Ensure MAC detects CRC error	MII:M	Yes [ ] N/A [ ]

117.5.4.3 Data stream structure

Item	Feature	Subclause	Value/Comment	Status	Support
DS1	Frame transfer	117.2	Within 200GMII/400GMII data stream	MII:M	Yes [ ] N/A [ ]
DS2	Bit mapping	117.2	Per Figure 81–4	MII:M	Yes [ ] N/A [ ]
DS3	Content of <data>	117.2	Consist of data octets	MII:M	Yes [ ] N/A [ ]
DS4	Recognition of <efd>	117.2	Terminate recognized in any lane	MII:M	Yes [ ] N/A [ ]

117.5.4.4 200GMII/400GMII signal functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	TX_CLK active edge	117.3	TXD and TXC sampled on the rising edge of TX_CLK	MII:M	Yes [ ] N/A [ ]
FS2	TX_CLK frequency	117.3	One-sixty-fourth of the MAC transmit data rate	MII:M	Yes [ ] N/A [ ]
FS3	TXC assertion and de-assertion	117.3	De-asserted for data, asserted for control character	MII:M	Yes [ ] N/A [ ]
FS4	TXC clock	117.3	Synchronous to TX_CLK	MII:M	Yes [ ] N/A [ ]
FS5	TXD encoding	117.3	Per Table 81–3	MII:M	Yes [ ] N/A [ ]
FS6	TXD clock	117.3	Synchronous to TX_CLK	MII:M	Yes [ ] N/A [ ]
FS7	Start alignment	117.3	Start control character aligned to lane 0	MII:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
FS8	RX_CLK active edge	117.3	RXD and RXC sampled on the rising edge of RX_CLK	MII:M	Yes [ ] N/A [ ]
FS9	RX_CLK frequency	117.3	One-sixty-fourth of the MAC receive data rate	MII:M	Yes [ ] N/A [ ]
FS10	Loss of receive signal	117.3	Source RX_CLK from nominal clock	MII:M	Yes [ ] N/A [ ]
FS11	RXC assertion and de-assertion	117.3	De-asserted for data, asserted for control character	MII:M	Yes [ ] N/A [ ]
FS12	RXC clock	117.3	Synchronous to RX_CLK	MII:M	Yes [ ] N/A [ ]
FS13	RXD decoding	117.3	Per Table 81–4	MII:M	Yes [ ] N/A [ ]
FS14	RXD clock	117.3	Synchronous to RX_CLK	MII:M	Yes [ ] N/A [ ]
FS15	Received Error control character	117.3	RS cause MAC FrameCheckError	MII:M	Yes [ ] N/A [ ]
FS16	DATA_VALID assertion	117.3	RS not assert DATA_VALID unless Start control character in lane 0	MII:M	Yes [ ] N/A [ ]

117.5.4.5 Link fault signaling state diagram

Item	Feature	Subclause	Value/Comment	Status	Support
LF1	Link fault signaling state diagram	117.3	Implement per Figure 81–11	MII:M	Yes [ ] N/A [ ]
LF2	link_fault = OK and MAC frames	117.3	RS services MAC frame transmission requests	MII:M	Yes [ ] N/A [ ]
LF3	link_fault = OK and no MAC frames	117.3	In absence of MAC frames, RS transmits Idle control characters	MII:M	Yes [ ] N/A [ ]
LF4	link_fault = Local Fault	117.3	RS transmits continuous Remote Fault Sequence ordered sets	MII:M	Yes [ ] N/A [ ]
LF5	link_fault = Remote Fault	117.3	RS transmits continuous Idle control characters	MII:M	Yes [ ] N/A [ ]

117.5.4.6 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Assertion of LPI in Tx direction	117.3	As defined in Table 81–3	LPI:M	Yes [ ] N/A [ ]
L2	Assertion of LPI in Rx direction	117.3	As defined in Table 81–4	LPI:M	Yes [ ] N/A [ ]

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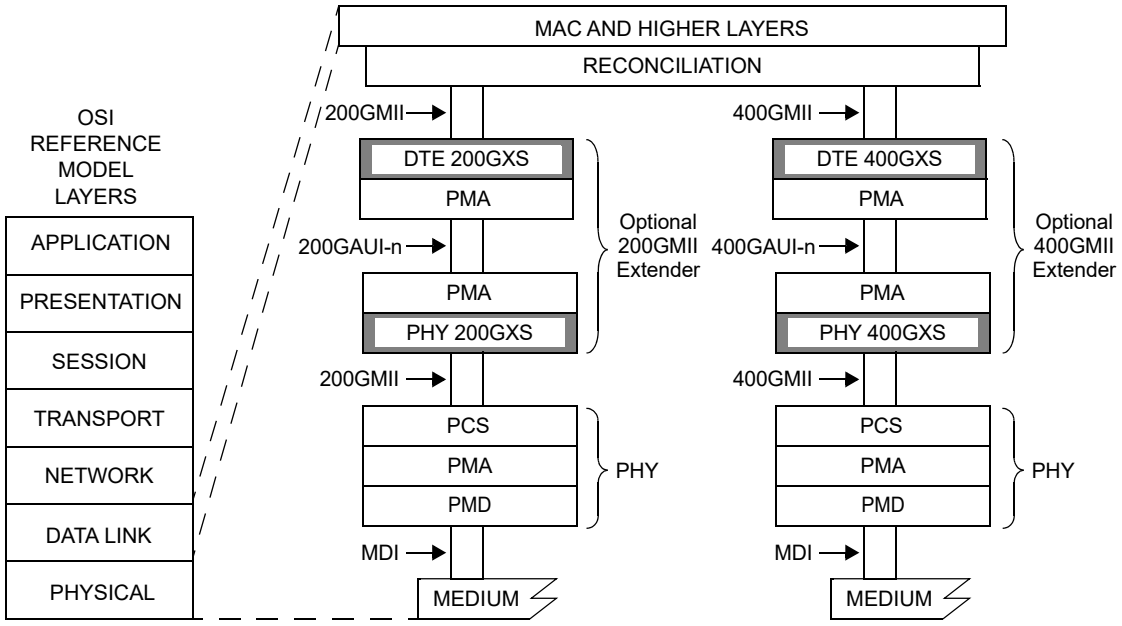
118. 200GMII Extender, 400GMII Extender, 200GMII Extender Sublayer (200GXS), and 400GMII Extender Sublayer (400GXS)

118.1 Overview

This clause defines the functional characteristics for the optional 200GMII Extender and 200GMII Extender Sublayer (200GXS), and also for the optional 400GMII Extender and 400GMII Extender Sublayer (400GXS). Figure 118–1 shows the relationship of the 200GMII/400GMII Extender and 200GXS/400GXS sublayer with other sublayers to the ISO Open System Interconnection (OSI) reference model.

The 200GMII/400GMII Extender allows the extension of the 200GMII/400GMII to the PCS via a physical instantiation. The 200GMII/400GMII Extender is composed of a 200GXS/400GXS at the RS end, a 200GXS/400GXS at the PHY end with a physical instantiation of 200GAUI-n/400GAUI-n between two adjacent PMA sublayers.

A 200GMII/400GMII Extender with the optional Energy-Efficient Ethernet (EEE) capability (see Clause 78) encodes and decodes Low Power Idle (LPI) signals. The assertion of LPI at the 200GMII/400GMII is encoded in the transmitted symbols. Detection of LPI encoding in the received symbols is indicated as LPI at the 200GMII/400GMII.



200GAUI-n = 200 Gb/s n-LANE ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
200GXS = 200GMII EXTENDER SUBLAYER
400GAUI-n = 400 Gb/s n-LANE ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
400GXS = 400GMII EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 118–1—200GXS and 400GXS relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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118.1.1 Summary of major concepts

The following is a list of the major concepts of the 200GMII/400GMII Extender:

a) Simple signal mapping to the 200GMII/400GMII
b) The optional 200GMII/400GMII Extender can be inserted between the Reconciliation Sublayer and the PHY to transparently extend the reach of the 200GMII/400GMII
c) Independent transmit and receive data paths
d) The 200GXS/400GXS leverages all functions in the Clause 119 PCS and supports physical instantiations of the 200GAUI-n/400GAUI-n
e) Optionally extends LPI signaling to the PHY for EEE

118.1.2 200GXS/400GXS Sublayer

The 200GXS, if implemented, shall be identical in function to the 200GBASE-R PCS in Clause 119 with the addition of the functions defined in 118.2. A single device may be configured as either a 200GXS or the 200GBASE-R PCS and may be managed through different optional management registers.

The 400GXS, if implemented, shall be identical in function to the 400GBASE-R PCS in Clause 119 with the addition of the functions defined in 118.2. A single device may be configured as either a 400GXS or the 400GBASE-R PCS and may be managed through different optional management registers.

118.1.3 200GAUI-n/400GAUI-n

A 200GMII Extender may use any of the following electrical interfaces for the connection between its PMA sublayers (200GAUI-n), as shown in Figure 118–1:

— 200GAUI-8 chip-to-chip (Annex 120B)
— 200GAUI-8 chip-to-module (Annex 120C)
— 200GAUI-4 chip-to-chip (Annex 120D)
— 200GAUI-4 chip-to-module (Annex 120E)

A 400GMII Extender may use any of the following electrical interfaces for the connection between its PMA sublayers (400GAUI-n), as shown in Figure 118–1:

— 400GAUI-16 chip-to-chip (Annex 120B)
— 400GAUI-16 chip-to-module (Annex 120C)
— 400GAUI-8 chip-to-chip (Annex 120D)
— 400GAUI-8 chip-to-module (Annex 120E)

118.2 FEC Degrade

The propagation of FEC degrade signaling across PCS and XS sublayers is described in 116.6 and is based on the optional FEC degrade signaling described in Clause 119 with the changes described for the DTE XS in 118.2.1 and for the PHY XS in 118.2.2.

118.2.1 DTE XS FEC Degrade signaling

The variable tx_am_sf is set as follows:

tx_am_sf<2:0> = {FEC_degraded_SER + rx_local_degraded,0,0}

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118.2.2 PHY XS FEC Degrade signaling

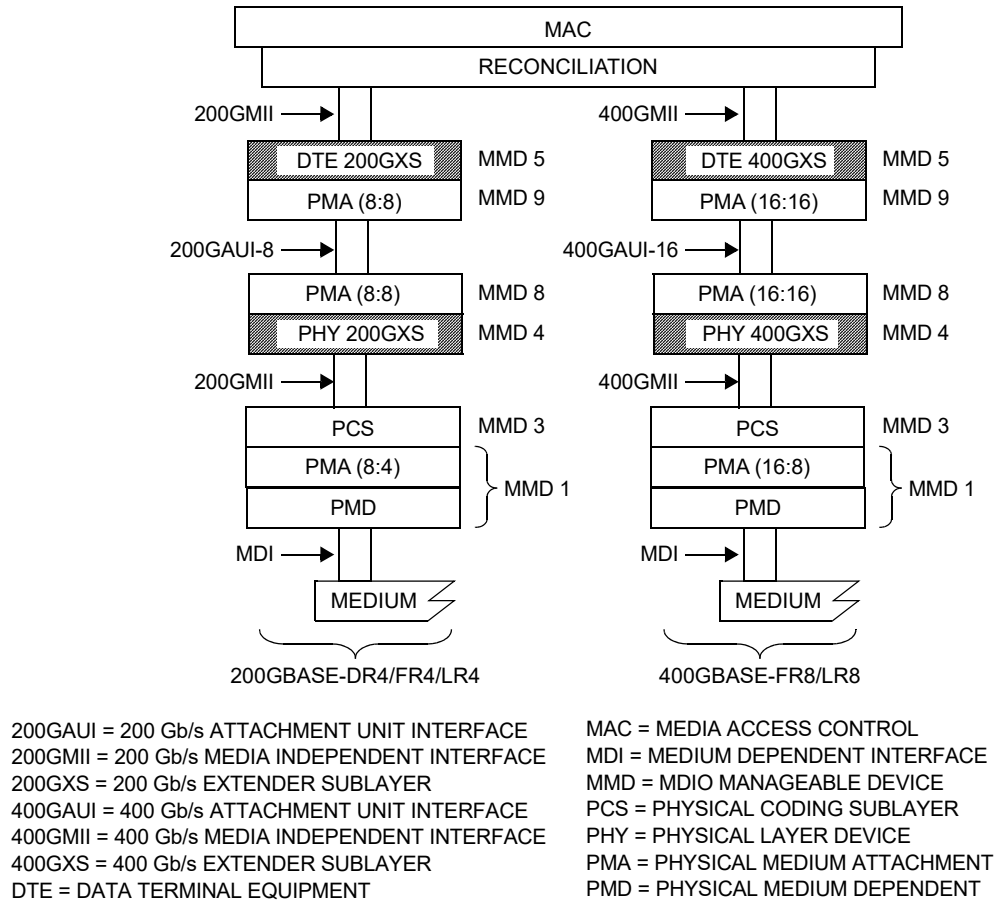
The variable tx_am_sf is set as follows:

tx_am_sf<2:0> = {PCS:rx_rm_degraded, PCS:FEC_degraded_SER + PCS:rx_local_degraded, 0}

Where PCS:rx_rm_degraded, PCS:FEC_degraded_SER, and PCS:rx_local_degraded are the rx_rm_degraded, FEC_degraded_SER, and rx_local_degraded variables from the adjacent PCS.

118.3 200GXS and 400GXS partitioning example

A partitioning example and MMD numbering using the 200GXS and 400GXS is shown in Figure 118–2.



200GAUI = 200 Gb/s ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
200GXS = 200 Gb/s EXTENDER SUBLAYER
400GAUI = 400 Gb/s ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
400GXS = 400 Gb/s EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 118–2—Example 200GBASE-DR4/FR4/LR4 and 400GBASE-FR8/LR8 PMA layering with 200GXS and 400GXS

118.4 200GXS and 400GXS MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the 200GXS or 400GXS. If MDIO is implemented, it shall map MDIO PHY XS and DTE XS control bits to Clause 119 control variables as shown in Table 118–1 and Table 118–3, respectively. Similarly, if MDIO is implemented, it shall map MDIO PHY XS and DTE XS status bits to Clause 119 status variables as shown in Table 118–2 and Table 118–4, respectively.

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Table 118–1—MDIO PHY XS to Clause 119 control variable mapping

MDIO control variable	PHY XS register name	Register/bit number	Clause 119 control variable
Reset	PHY XS control 1 register	4.0.15	reset
Loopback	PHY XS control 1 register	4.0.14	Loopback
Transmit test-pattern enable	BASE-R PHY XS test-pattern control register	4.42.3	tx_test_mode
PHY XS FEC bypass indication enable	PHY XS FEC control register	4.800.1	FEC_bypass_indication_enable
PHY XS FEC degraded SER enable	PHY XS FEC control register	4.800.2	FEC_degraded_SER_enable
PHY XS FEC degraded SER activate threshold	PHY XS FEC degraded SER activate threshold register	4.806, 4.807	FEC_degraded_SER_activate_threshold
PHY XS FEC degraded SER deactivate threshold	PHY XS FEC degraded SER deactivate threshold register	4.808, 4.809	FEC_degraded_SER_deactivate_threshold
PHY XS FEC degraded SER interval	PHY XS FEC degraded SER interval	4.810, 4.811	FEC_degraded_SER_interval

Table 118–2—MDIO PHY XS to Clause 119 status variable mapping

MDIO status variable	PHY XS register name	Register/bit number	Clause 119 status variable
BASE-R PHY XS receive link status	BASE-R PHY XS status 1	4.32.12	PCS_status
Lane *x* aligned	Multi-lane BASE-R PHY XS alignment status 3 and 4	4.52.7:0 4.53.7:0	am_lock<*x*>
PHY XS lane alignment status	Multi-lane BASE-R PHY XS alignment status 1	4.50.12	align_status
Lane *x* mapping	PHY XS lane mapping, lane 0 through lane 15	4.400 through 4.415	pcs_lane_mapping<*x*>
PHY XS FEC bypass indication ability	PHY XS FEC status	4.801.1	FEC_bypass_indication_ability
FEC corrected codewords	PHY XS FEC corrected codewords counter	4.802, 4.803	FEC_corrected_cw_counter
FEC uncorrected codewords	PHY XS FEC uncorrected codewords counter	4.804, 4.805	FEC_uncorrected_cw_counter
PHY XS FEC symbol errors, lane 0 to lane 15	PHY XS FEC symbol error counter, lane 0 to lane 15	4.600 to 4.631	FEC_symbol_error_counter_*i*
Tx LPI indication	PHY XS status 1	4.1.9	Tx LPI indication
Tx LPI received	PHY XS status 1	4.1.11	Tx LPI received
Rx LPI indication	PHY XS status 1	4.1.8	Rx LPI indication
Rx LPI received	PHY XS status 1	4.1.10	Rx LPI received
EEE wake error counter	EEE wake error counter	4.22	Wake_error_counter

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Table 118–2—MDIO PHY XS to Clause 119 status variable mapping *(continued)*

MDIO status variable	PHY XS register name	Register/bit number	Clause 119 status variable
PHY XS FEC degraded SER ability	PHY XS FEC status register	4.801.3	FEC_degraded_SER_ability
PHY XS FEC degraded SER	PHY XS FEC status register	4.801.4	FEC_degraded_SER
Remote degraded SER received	PHY XS FEC status register	4.801.5	rx_rm_degraded

Table 118–3—MDIO DTE XS to Clause 119 control variable mapping

MDIO control variable	DTE XS register name	Register/bit number	Clause 119 control variable
Reset	DTE XS control 1 register	5.0.15	reset
Loopback	DTE XS control 1 register	5.0.14	Loopback
Transmit test-pattern enable	BASE-R DTE XS test-pattern control register	5.42.3	tx_test_mode
DTE XS FEC bypass indication enable	DTE XS FEC control register	5.800.1	FEC_bypass_indication_enable
DTE XS FEC degraded SER enable	DTE XS FEC control register	5.800.2	FEC_degraded_SER_enable
DTE XS FEC degraded SER activate threshold	DTE XS FEC degraded SER activate threshold register	5.806, 5.807	FEC_degraded_SER_activate_threshold
DTE XS FEC degraded SER deactivate threshold	DTE XS FEC degraded SER deactivate threshold register	5.808, 5.809	FEC_degraded_SER_deactivate_threshold
DTE XS FEC degraded SER interval	DTE XS FEC degraded SER interval	5.810, 5.811	FEC_degraded_SER_interval

Table 118–4—MDIO DTE XS to Clause 119 status variable mapping

MDIO status variable	DTE XS register name	Register/bit number	Clause 119 status variable
BASE-R DTE XS receive link status	BASE-R DTE XS status 1	5.32.12	PCS_status
Lane *x* aligned	Multi-lane BASE-R DTE XS alignment status 3 and 4	5.52.7:0 5.53.7:0	am_lock<*x*>
DTE XS lane alignment status	Multi-lane BASE-R DTE XS alignment status 1	5.50.12	align_status
Lane *x* mapping	DTE XS lane mapping, lane 0 through lane 15	5.400 through 5.415	pcs_lane_mapping<*x*>
DTE XS FEC bypass indication ability	DTE XS FEC status	5.801.1	FEC_bypass_indication_ability
FEC corrected codewords	DTE XS FEC corrected codewords counter	5.802, 5.803	FEC_corrected_cw_counter

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Table 118–4—MDIO DTE XS to Clause 119 status variable mapping *(continued)*

MDIO status variable	DTE XS register name	Register/bit number	Clause 119 status variable
FEC uncorrected codewords	DTE XS FEC uncorrected codewords counter	5.804, 5.805	FEC_uncorrected_cw_counter
DTE XS FEC symbol errors, lane 0 to lane 15	DTE XS FEC symbol error counter, lane 0 to lane 15	5.600 to 5.631	FEC_symbol_error_counter_*i*
Tx LPI indication	DTE XS status 1	5.1.9	Tx LPI indication
Tx LPI received	DTE XS status 1	5.1.11	Tx LPI received
Rx LPI indication	DTE XS status 1	5.1.8	Rx LPI indication
Rx LPI received	DTE XS status 1	5.1.10	Rx LPI received
EEE wake error counter	EEE wake error counter	5.22	Wake_error_counter
DTE XS FEC degraded SER ability	DTE XS FEC status register	5.801.3	FEC_degraded_SER_ability
DTE XS FEC degraded SER	DTE XS FEC status register	5.801.4	FEC_degraded_SER
Remote degraded received	DTE XS FEC status register	5.801.5	rx_rm_degraded
Local degraded received	DTE XS FEC status register	5.801.6	rx_local_degraded

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118.5 Protocol implementation conformance statement (PICS) proforma for Clause 118, 200GMII Extender, 400GMII Extender, 200GMII Extender Sublayer (200GXS), and 400GMII Extender Sublayer (400GXS)[205]

118.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 118, 200GMII Extender, 400GMII Extender, 200GMII Extender Sublayer (200GXS), and 400GMII Extender Sublayer (400GXS), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

118.5.2 Identification

118.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

118.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 118, 200GMII Extender, 400GMII Extender, 200GMII Extender Sublayer (200GXS), and 400GMII Extender Sublayer (400GXS)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[205] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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118.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
MII	200GMII or 400GMII logical interface	117, 118.1	Logical interface is supported	O	Yes [ ] No [ ]
*PHYXS	PHY 200GXS or PHY 400GXS	118.1		O/2	Yes [ ] No [ ]
*DTEXS	DTE 200GXS or DTE 400GXS	118.1		O/2	Yes [ ] No [ ]
*200GXS	Using the XS for 200GBASE-R	118.1.2		O.1	Yes [ ] No [ ]
*400GXS	Using the XS for 400GBASE-R	118.1.2		O.1	Yes [ ] No [ ]
*MD	MDIO	45, 118.4	Registers and interface supported	O	Yes [ ] No [ ]
*BI	Bypass indication	119.2.5.3	Capability is supported	O	Yes [ ] No [ ]
DC	Delay constraints	119.5	Conforms to delay constraints specified in 119.5	M	Yes [ ]
EEE	EEE capability	119.2.3.3	Capability is supported	O	Yes [ ] No [ ]
JTM	Supports test-pattern mode	119.2.1, 119.2.4.9		M	Yes [ ]
FDD	Support for optional FEC degraded detection	119.2.5.3	In the FEC decoder can optionally detect FEC SER degraded at a programmable threshold	O	Yes [ ] No [ ]

118.5.4 PICS proforma tables for 200GMII Extender, 400GMII Extender, 200GMII Extender Sublayer (200GXS), and 400GMII Extender Sublayer (400GXS)

118.5.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	64B/66B to 256B/257B transcoder	119.2.4.2	tx_xcoded<256:0> constructed per 119.2.4.2	M	Yes [ ]
TF2	Transmission bit ordering	119.2.4.8	First bit transmitted is bit 0	M	Yes [ ]
TF3	Pad value	119.2.4.4	PRBS9	M	Yes [ ]
TF4	Alignment marker insertion	119.2.4.4		M	Yes [ ]
TF5	Pre-FEC distribution	119.2.4.5	Distribute the data to two FEC codewords	M	Yes [ ]
TF6	Reed-Solomon encoder	119.2.4.6	RS(544,514)	M	Yes [ ]
TF7	Symbol distribution	119.2.4.7	Distribution is based on 10b symbols	M	Yes [ ]

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118.5.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	119.2.5.1	Maximum Skew of 180 ns between PCS lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	Lane reorder and de-interleave	119.2.5.2	Order the PCS lanes according to the PCS lane number and de-interleave the FEC codewords	M	Yes [ ]
RF3	Reed-Solomon decoder	119.2.5.3	Corrects any combination of up to *t*=15 symbol errors in a codeword	M	Yes [ ]
RF4	Reed-Solomon decoder	119.2.5.3	Capable of indicating when a codeword was not corrected.	M	Yes [ ]
RF5	Error monitoring while error indication is bypassed	119.2.5.3	When the number of symbol errors in a block of 8192 codewords exceeds 5560 assert hi_ser for 60 ms to 75 ms	BI:M	Yes [ ] N/A [ ]
RF6	256B/257B to 64B/66B transcoder	119.2.5.7	rx_coded_*j*<65:0>, *j*=0 to 3 constructed per 119.2.5.7	M	Yes [ ]

118.5.4.3 64B/66B coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder (and ENCODE function) implements the code as specified	119.2.3, 119.2.6.2.3		M	Yes [ ]
C2	Decoder (and DECODE function) implements the code as specified	119.2.3, 119.2.6.2.3		M	Yes [ ]
C3	Only valid block types are transmitted	119.2.3.2		M	Yes [ ]
C4	Invalid block types are treated as an error	119.2.3.2		M	Yes [ ]
C5	Only valid control characters are transmitted	119.2.3.3		M	Yes [ ]
C6	Invalid control characters are treated as an error	119.2.3.3		M	Yes [ ]
C7	Idles do not interrupt data	119.2.3.5		M	Yes [ ]
C8	IDLE control code insertion and deletion	119.2.3.5	Insertion or Deletion in groups of 8 /I/s	M	Yes [ ]
C9	Sequence ordered set deletion	119.2.3.8	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ]

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118.5.4.4 Scrambler and descrambler

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Scrambler	119.2.4.3	Performs as shown in Figure 49–8	M	Yes [ ]
S2	Descrambler	119.2.5.6	Performs as shown in Figure 49–10	M	Yes [ ]

118.5.4.5 Alignment markers

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	Alignment marker insertion	119.2.4.4	Alignment markers are inserted periodically as in 119.2.4.4	M	Yes [ ]
AM2	Alignment marker form	119.2.4.4	Alignment markers are formed as described in 119.2.4.4	M	Yes [ ]
AM3	Lane mapping	119.2.4.4	PCS lane number is captured	MD:M	Yes [ ] N/A [ ]
AM4	Alignment marker removal	119.2.5.5	Alignment markers are removed prior to descrambling as described in 119.2.5.5	M	Yes [ ]

118.5.5 Test-pattern modes

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Scrambled idle transmit test-pattern generator is implemented	119.2.4.9		M	Yes [ ]

118.5.6 Bit order

Item	Feature	Subclause	Value/Comment	Status	Support
B1	Transmit bit order	119.2.4.8	Placement of bits into the PCS lanes as shown in Figure 119–10 or Figure 119–11	M	Yes [ ]

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118.5.7 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Equivalent access to XS management objects is provided	119.3		!MD:O	Yes [ ] No [ ] N/A [ ]
M2	Mapping of MDIO control bits and MDIO status bits for PHY 200GXS or PHY 400GXS	118.4	See Table 118–1 and Table 118–2	MD*PHY XS:M	Yes [ ] N/A [ ]
M3	Mapping of MDIO control bits and MDIO status bits for DTE 200GXS or DTE 400GXS	118.4	See Table 118–3 and Table 118–4	MD*DTEX S:M	Yes [ ] N/A [ ]

118.5.7.1 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Alignment marker lock	119.2.6	Implements 8 alignment marker lock processes as depicted in Figure 119–12	200GXS: M	Yes [ ] N/A [ ]
SM2	Alignment marker lock	119.2.6	Implements 16 alignment marker lock processes as depicted in Figure 119–12	400GXS: M	Yes [ ] N/A [ ]
SM3	The SLIP function evaluates all possible block positions	119.2.6.2.3		M	Yes [ ]
SM4	PCS synchronization state diagram	119.2.6	Meets the requirements of Figure 119–13	M	Yes [ ]
SM5	Transmit process	119.2.6	Meets the requirements of Figure 119–14	M	Yes [ ]
SM6	Receive process	119.2.6	Meets the requirements of Figure 119–15	M	Yes [ ]

118.5.7.2 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports loopback	119.4		M	Yes [ ]
L2	When in loopback, transmits what it receives from the 200GMII/400GMII	119.4		M	Yes [ ]
L3	When in loopback, ignore all data presented by the PMA sublayer	119.4		M	Yes [ ]

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118.5.7.3 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS delay constraint	119.5	No more than 160 256 BT for sum of transmit and receive path delays for 200GBASE-R.	200GXS :M	Yes [ ] N/A [ ]
TIM2	PCS delay constraint	119.5	No more than 320 000 BT for sum of transmit and receive path delays for 400GBASE-R.	400GXS :M	Yes [ ] N/A [ ]

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119. Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R

119.1 Overview

119.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) that is common to two families of Physical Layer implementation known as 200GBASE-R and 400GBASE-R. The 200GBASE-R PCS is a sublayer of the 200 Gb/s PHYs listed in Table 116–1. The 400GBASE-R PCS is a sublayer of the 400 Gb/s PHYs listed in Table 116–2. The terms 200GBASE-R and 400GBASE-R are used when referring generally to Physical Layers using the PCS defined in this clause. Both 200GBASE-R and 400GBASE-R are based on a 64B/66B code. The 64B/66B code supports transmission of data and control characters. The 64B/66B code is then transcoded to 256B/257B encoding to reduce the overhead and make room for forward error correction (FEC). The 256B/257B encoded data is then FEC encoded before being transmitted. Data distribution is introduced to support multiple lanes in the Physical Layer. Part of the distribution includes the periodic insertion of an alignment marker, which allows the receive PCS to align data from multiple lanes.

119.1.2 Relationship of 200GBASE-R and 400GBASE-R to other standards

Figure 119–1 depicts the relationship of the 200GBASE-R and 400GBASE-R sublayers (shown shaded), the Ethernet MAC and Reconciliation Sublayers, and the higher layers.

This clause borrows heavily from Clause 82 and Clause 91. 64B/66B encoding is reused with the addition of transcoding and PCS FEC.

119.1.3 Physical Coding Sublayer (PCS)

The PCS service interface is the Media Independent Interface (200GMII/400GMII), which is defined in Clause 117. The 200GMII provides a uniform interface to the Reconciliation Sublayer for all 200 Gb/s PHY implementations. The 400GMII provides a uniform interface to the Reconciliation Sublayer for all 400 Gb/s PHY implementations.

The 200GBASE-R and 400GBASE-R PCSs provide all services required by the 200GMII/400GMII, including the following:

a) Encoding (decoding) of eight 200GMII/400GMII data octets to (from) 66-bit blocks (64B/66B).
b) Transcoding from 66-bit blocks to (from) 257-bit blocks.
c) Reed-Solomon encoding (decoding) the 257-bit blocks.
d) Transferring encoded data to (from) the PMA.
e) Compensation for any rate differences caused by the insertion or deletion of alignment markers or due to any rate difference between the 200GMII/400GMII and PMA through the insertion or deletion of idle control characters.
f) Determining when a functional link has been established and informing the management entity via the MDIO when the PHY is ready for use.

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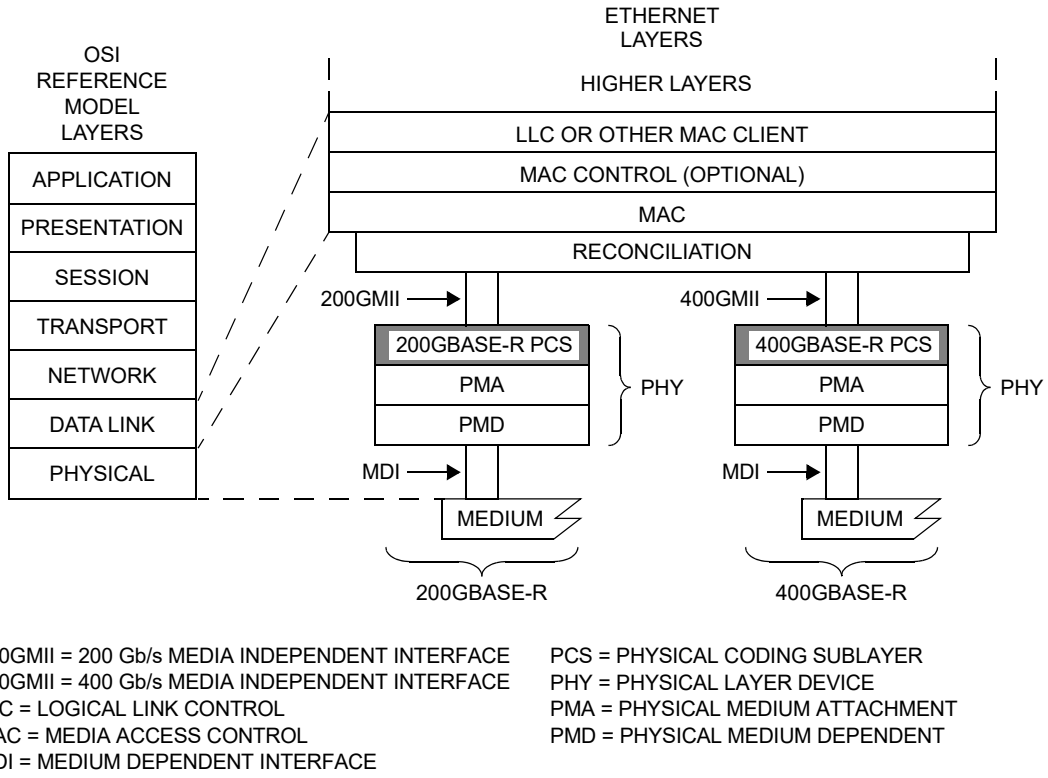

200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 119–1—200GBASE-R and 400GBASE-R PCS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

119.1.4 Inter-sublayer interfaces

The upper interface of the PCS may connect to the Reconciliation Sublayer through the 200GMII/400GMII. The lower interface of the PCS connects to the PMA sublayer to support a PMD. The 200GBASE-R PCS has a nominal rate at the PMA service interface of 26.5625 Gtransfers/s on each of 8 PCS lanes, which provides capacity for the MAC data rate of 200 Gb/s. The 400GBASE-R PCS has a nominal rate at the PMA service interface of 26.5625 Gtransfers/s on each of 16 PCS lanes, which provides capacity for the MAC data rate of 400 Gb/s.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

119.1.4.1 PCS service interface (200GMII/400GMII)

The PCS service interface allows the 200GBASE-R or 400GBASE-R PCS to transfer information to and from a PCS client. The PCS client is the Reconciliation Sublayer. The PCS Service Interface is precisely defined as the Media Independent Interface (200GMII/400GMII) in Clause 117.

119.1.4.2 Physical Medium Attachment (PMA) service interface

The PMA service interface for the PCS is described in an abstract manner and does not imply any particular implementation. The PMA Service Interface supports the exchange of encoded data between the PCS and PMA sublayer. The PMA service interface is defined in 120.3 and is an instance of the inter-sublayer service interface definition in 116.3.

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119.1.5 Functional block diagram

Figure 119–2 provides a functional block diagram of the 200GBASE-R and 400GBASE-R PCSs.

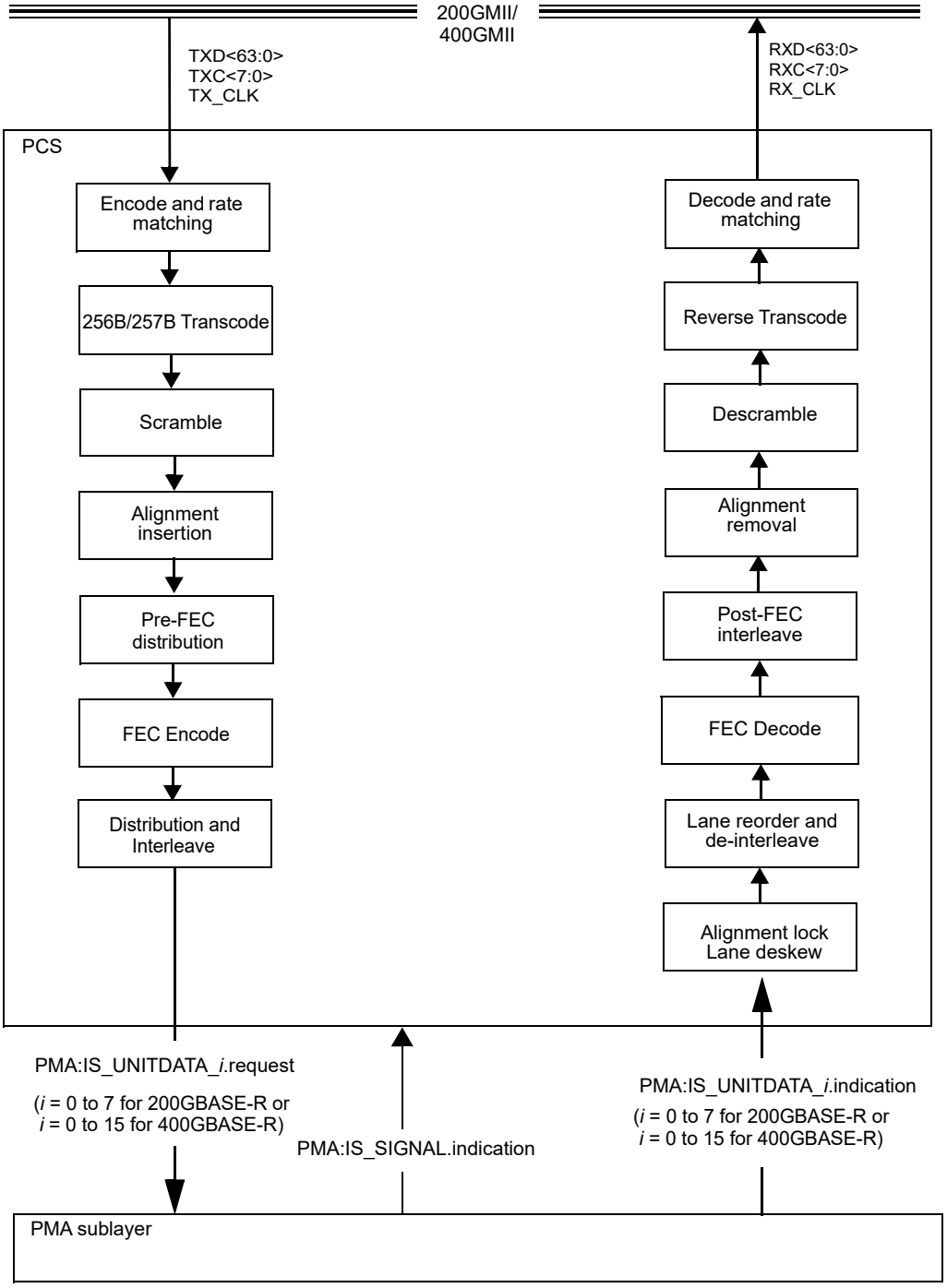

Figure 119–2—Functional block diagram

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119.2 Physical Coding Sublayer (PCS)

119.2.1 Functions within the PCS

The 200GBASE-R and 400GBASE-R PCS are composed of the PCS Transmit and PCS Receive processes. The PCS shields the Reconciliation Sublayer (and MAC) from the specific nature of the underlying channel. The PCS transmit channel can operate in normal mode or test-pattern mode.

When communicating with the 200GMII/400GMII, the PCS uses an eight octet-wide, synchronous data path, with packet delineation being provided by transmit control signals (TXC<n> = 1) and receive control signals (RXC<n> = 1). When communicating with the PMA, the 200GBASE-R PCS uses 8 encoded bit streams (also known as PCS lanes) and the 400GBASE-R PCS uses 16 encoded bit streams. Per direction (RX or TX), the PCS lanes originate from a common clock but may vary in phase and skew dynamically. The PMA sublayer operates independently of block and packet boundaries. The PCS provides the functions necessary to map packets between the 200GMII/400GMII format and the PMA service interface format.

When the transmit channel is in normal mode, the PCS Transmit process continuously generates 66-bit blocks based upon the TXD <63:0> and TXC <7:0> signals on the 200GMII/400GMII. The 66-bit blocks are transcoded to 257-bit blocks to reduce the line coding overhead. The transcoded blocks are then scrambled to control clock content and baseline wander. Alignment markers are periodically added to the data stream. The data stream is distributed to two 5140-bit blocks and then FEC encoded to control errors. The two FEC codewords are then interleaved before data is distributed to individual PCS lanes.

Transmit data-units are sent to the service interface via the PMA:IS_UNITDATA_*i*.request primitive.

When the transmit channel is in test-pattern mode, a test pattern is packed into the transmit data-units that are sent to the PMA service interface via the PMA:IS_UNITDATA_*i*.request primitive.

The PCS Synchronization process continuously monitors PMA:IS_SIGNAL.indication(SIGNAL_OK). When SIGNAL_OK indicates OK, then the PCS synchronization process accepts data-units via the PMA:IS_UNITDATA_*i*.indication primitive. It attains alignment marker lock based on the common marker (CM) portion that is periodically transmitted on every PCS lane. After alignment markers are found on all PCS lanes, the individual PCS lanes are identified using the unique marker portion (UM) and then re-ordered and deskewed. Note that a particular transmit PCS lane can be received on any receive lane of the service interface due to the skew and multiplexing that occurs in the path.

The PCS deskew process deskews, aligns and reorders the individual PCS lanes, forms a single stream, and sets the align_status flag to indicate whether the PCS has obtained alignment. The PCS then de-interleaves and processes the FEC codewords. Next the PCS re-interleaves the corrected FEC codewords on a 10-bit basis to form a single stream. The PCS then removes alignment markers, descrambles the data, transcodes the data back to 64B/66B and then decodes the 64B/66B encoded data.

The PCS shall provide transmit test-pattern mode for the scrambled idle pattern (see 119.2.4.9).

119.2.2 Use of blocks

The PCS maps 200GMII/400GMII signals into 66-bit blocks, and vice versa, using a 64B/66B coding scheme. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks as defined in 119.2.3.

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119.2.3 64B/66B code

The PCS uses 64B/66B coding to support transmission of control and data characters. The 64B/66B codestream is then transcoded into a 256B/257B stream and FEC bits are added in this PCS before transmission.

119.2.3.1 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/66B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. The control characters /I/ and /E/ are labeled C_0 to C_7. The control character /Q/ for a sequence ordered set is labeled as O_0 since it is only valid on the first octet of the 200GMII/400GMII. The control character for start is labeled as S_0 for the same reason. The control character for terminate is labeled as T_0 to T_7. The four trailing zero data octets in ordered sets are labeled as Z_4 to Z_7.

One 200GMII/400GMII transfer provides eight characters that are encoded into one 66-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the 200GMII/400GMII transfer.

Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled TxB<65:0> and RxB<65:0>, respectively, where TxB<0> and RxB<0> represent the first transmitted bit. The value of the sync header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

119.2.3.2 64B/66B block structure

Blocks consist of 66 bits. The first two bits of a block are the synchronization header (sync header). Blocks are either data blocks or control blocks. The sync header is 01 for data blocks and 10 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an 8-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start, Terminate, or ordered set, that character is implied by the block type field. Other control characters are encoded in a 7-bit control code. Each control block encodes eight characters.

The format of the blocks is as shown in Figure 82–5. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 66-bit block. These characters are either data characters or control characters and, when transferred across the 200GMII/400GMII, the corresponding TXC or RXC bit is set accordingly. Within the Input Data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control characters and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt.

All values of block type field not listed in Figure 82–5 are invalid; they shall not be transmitted and shall be considered an error if received.

119.2.3.3 Control codes

The same set of control characters are supported by the 200GMII/400GMII and the PCS. The representations of the control characters are the control codes. The 200GMII/400GMII encodes a control

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character into an octet (an eight bit value). The PCS encodes the start and terminate control characters implicitly by the block type field. The PCS encodes the ordered set control codes using the block type field. The PCS encodes each of the other control characters into a 7-bit control code.

The control characters and their mappings to 200GBASE-R/400GBASE-R control codes and 200GMII/400GMII control codes are specified in Table 82–1. All 200GMII/400GMII and 200GBASE-R/400GBASE-R control code values that do not appear in the table shall not be transmitted and shall be considered an error if received. The ability to transmit or receive Low Power Idle (LPI) is required for PHYs that support EEE (see Clause 78). If EEE has not been negotiated, LPI shall not be transmitted and shall be treated as an error if received.

119.2.3.4 Valid and invalid blocks

The valid and invalid blocks are identical to those in 82.2.3.5 with the exception that it is a 200GMII/400GMII data stream instead of XLGMII/CGMII.

119.2.3.5 Idle (/I/)

Idle and LPI control characters are identical to those in 82.2.3.6.

119.2.3.6 Start (/S/)

Start control characters are identical to those in 82.2.3.7.

119.2.3.7 Terminate (/T/)

The terminate control characteristics are identical to those in 82.2.3.8.

119.2.3.8 Ordered set (/O/)

Ordered sets are specified identically as in 82.2.3.9.

119.2.3.9 Error (/E/)

In both the 64B/66B encoder and decoder, the /E/ is generated whenever an /E/ is detected. The /E/ is also generated when invalid blocks are detected. The /E/ allows the PCS to propagate detected errors. See R_TYPE and T_TYPE function definitions in 119.2.6.2.3 for further information.

119.2.4 Transmit

119.2.4.1 Encode and rate matching

The PCS generates 66-bit blocks based upon the TXD<63:0> and TXC<7:0> signals received from the 200GMII/400GMII. One 200GMII/400GMII data transfer is encoded into one 66-bit block. If the transmit PCS spans multiple clock domains, it may also perform clock rate compensation via the deletion of idle control characters or sequence ordered sets or the insertion of idle (or LPI) control characters.

Idle (or LPI) control characters or sequence ordered sets are removed, if necessary, to accommodate the insertion of the alignment markers. See 119.2.3.5 and 119.2.3.8 for the deletion and insertion rules, and 119.2.4.4 for more details on alignment markers.

The transmit PCS generates blocks as specified in the transmit state diagram as shown in Figure 119–14. The contents of each block are contained in a vector tx_coded<65:0>, which is passed to the transcoder. tx_coded<1:0> contains the sync header and the remainder of the bits contain the block payload.

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NOTE—The stream of 66-bit blocks generated by this process, together with the FEC_degraded_SER and rx_local_degraded bits should be used as the reference signal for mapping to OTN.

119.2.4.2 64B/66B to 256B/257B transcoder

The transcoder constructs a 257-bit block, tx_xcoded<256:0>, from a group of four 66-bit blocks, tx_coded_*j*<65:0> where *j*=0 to 3. For each group of four 66-bit blocks, *j*=3 corresponds to the most recently received block. Bit 0 in each 66-bit block is the first bit received and corresponds to the first bit of the synchronization header.

NOTE—This transcoder differs from that described in 91.5.2.5, there is no scrambling of the first 5 bits since this clause scrambles the complete 257-bit blocks after transcoding.

If for all *j*=0 to 3, tx_coded_*j*<0>=0 and tx_coded_*j*<1>=1, tx_xcoded<256:0> shall be constructed as follows:

a) tx_xcoded<0> = 1

b) tx_xcoded<(64*j*+64):(64*j*+1)> = tx_coded_*j*<65:2> for *j*=0 to 3

If for all *j*=0 to 3, tx_coded_*j*<0> ≠ tx_coded_*j*<1> (valid synchronization header) and for any *j*=0 to 3, tx_coded_*j*<0>=1 and tx_coded_*j*<1>=0, tx_xcoded<256:0> shall be constructed as follows:

a1) tx_xcoded<0> = 0

b1) tx_xcoded<*j*+1> = tx_coded_*j*<1> for *j*=0 to 3

c1) Let *c* be the smallest value of *j* such that tx_coded_*c*<0>=1. In other words, tx_coded_*c* is the first 66-bit control block that was received in the current group of four blocks.

d1) Let tx_payloads<(64*j*+63):64*j*> = tx_coded_*j*<65:2> for *j*=0 to 3

e1) Omit tx_coded_*c*<9:6>, which is the second nibble (based on transmission order) of the block type field for tx_coded_*c,* from tx_xcoded per the following expressions.
tx_xcoded<(64*c*+8):5> = tx_payloads<(64*c*+3):0>
tx_xcoded<256:(64*c*+9)> = tx_payloads<255:(64*c*+8)>

If for any *j*=0 to 3, tx_coded_*j*<0> = tx_coded_*j*<1> (invalid synchronization header), tx_xcoded<256:0> shall be constructed as follows:

a2) tx_xcoded<0> = 0

b2) tx_xcoded<*j*+1> = 1 for *j*=0 to 3

c2) Let tx_payloads<(64*j*+63):64*j*> = tx_coded_*j*<65:2> for *j*=0 to 3

d2) Omit the second nibble (based on transmission order) of tx_coded_0 per the following expressions.
tx_xcoded<8:5> = tx_payloads<3:0>
tx_xcoded<256:9> = tx_payloads<255:8>

Several examples of the construction of tx_xcoded<256:0> are shown in Figure 119–3. In Figure 119–3, d_*j* indicates the *j*th 66-bit block contains only data octets, c_*j* indicates the *j*th 66-bit block contains one or more control characters, f_*j* denotes the first nibble of the block type field for 66-bit block *j*, and s_*j* denotes the second nibble of the block type field for 66-bit block *j*.

For each 257-bit block, bit 0 shall be the first bit transmitted.

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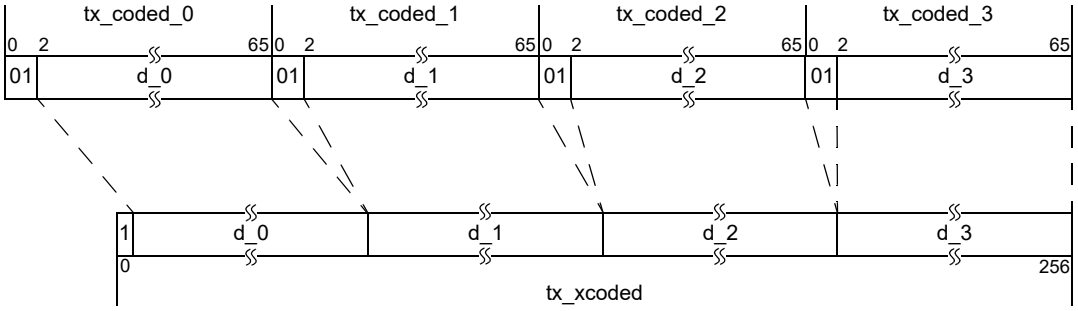
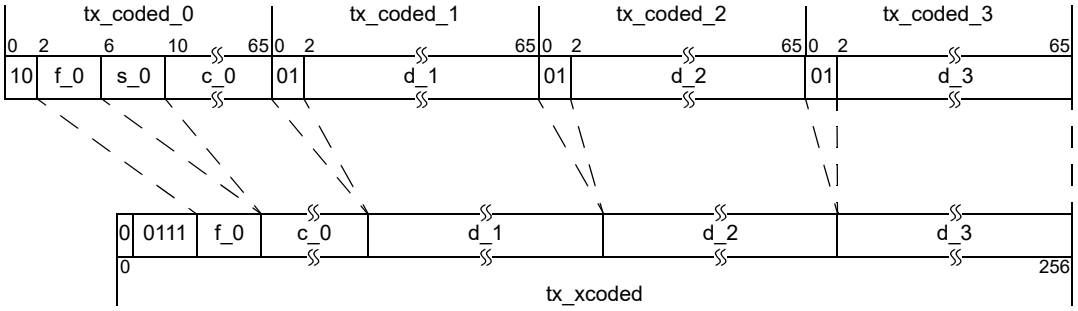
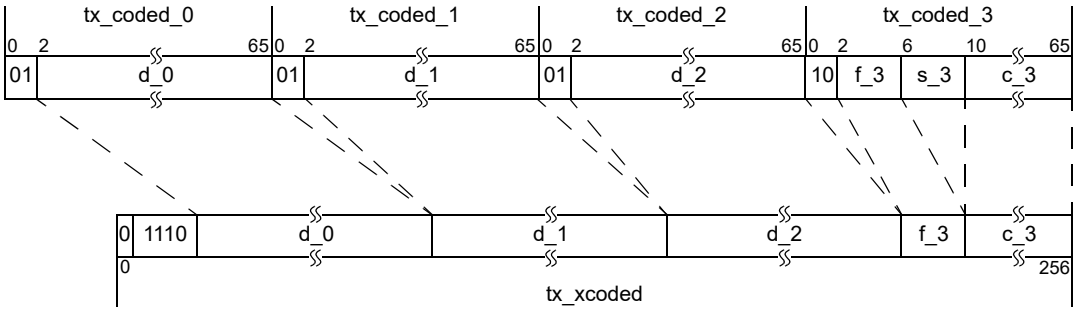


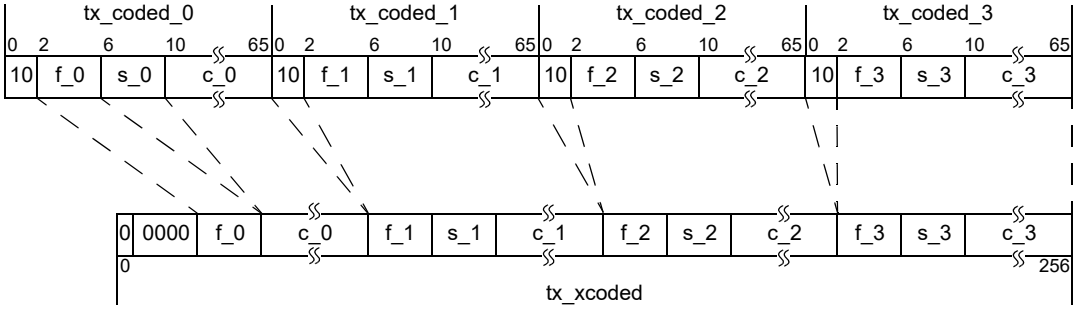
Example 1: All data blocks



Example 2: Control block followed by three data blocks



Example 3: Three data blocks followed by a control block



Example 4: All control blocks

Figure 119–3—Examples of the construction of tx_xcoded

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119.2.4.3 Scrambler

The transcoded 257-bit block, tx_xcoded<256:0>, shall be scrambled with a self-synchronizing scrambler to generate tx_scrambled<256:0>. The scrambler polynomial is identical to that in Clause 49, see Equation (49–1) for the definition of the polynomial.

119.2.4.4 Alignment marker mapping and insertion

In order to support deskew and reordering of the individual PCS lanes at the receive PCS, alignment markers corresponding to PCS lanes are periodically inserted after being processed by the alignment marker mapping function. The alignment marker mapping function compensates for the operation of the symbol distribution function and rearranges the alignment marker bits so that they appear on the PCS lanes intact and in the desired sequence. This preserves the properties of the alignment markers (e.g. DC balance, transition density) and provides a deterministic pattern for the purpose of synchronization.

For the 200GBASE-R PCS, an alignment marker group is composed of the alignment markers for all 8 PCS lanes plus an additional 65-bit pad and a 3-bit status field to yield the equivalent of four 257-bit blocks. For the 400GBASE-R PCS, an alignment marker group is composed of the alignment markers for all 16 PCS lanes plus an additional 133-bit pad and a 3-bit status field to yield the equivalent of eight 257-bit blocks. The alignment marker group is aligned to the beginning of two FEC messages, and interrupts any data transfer that is already in progress. The pad bits at the end of the alignment marker group shall be set to a free running PRBS9 pattern, defined by the polynomial $x^9 + x^5 + 1$. The initial value of the PRBS9 pattern generator may be any pattern other than all zeros.

Room for the alignment marker group is created by the transmit PCS (see 119.2.4.1). Special properties of the alignment marker group are that it is not scrambled, does not conform to the encoding rules as outlined in Figure 82–5 and is not transcoded. This is possible because the alignment marker group is added after encoding, transcoding, and scrambling, and removed before descrambling, transcoding, and 64B/66B decoding. The alignment marker group is not scrambled, which allows the receiver to directly search for and find the individual alignment markers, deskew the PCS lanes, and reassemble the aggregate stream before FEC decoding is performed. The alignment markers are formed from a known pattern that is defined to be balanced and with many transitions and therefore scrambling is not necessary.

The format of each PCS lane's alignment marker is shown in Figure 119–4. There is a portion that is common across all alignment markers (designated as CM_0 to CM_5), a unique portion per PCS lane (designated as UM_0 to UM_5), and finally a unique pad per PCS lane (designated as UP_0 to UP_2). Common synchronization logic independent of the received PCS lane number can be used with the common portion of the alignment marker. The unique pad (UP0 to UP2) within the alignment markers and the PRBS9 pad at the end of the alignment maker group are ignored on receive.

The content of the alignment markers shall be as shown in Table 119–1 for the 200GBASE-R PCS and as shown in Table 119–2 for the 400GBASE-R PCS. The contents depend on the PCS lane number and the octet number, with CM_0 through CM_5 being identical across all alignment markers to allow for common synchronization across lanes. The format shown in Table 119–1 defines how the alignment markers appear on a given PCS lane. In the FEC codewords, they appear in a permuted format due to the codeword interleaving that occurs before FEC codewords are distributed to PCS lanes.

The transmit alignment marker status field allows the local PCS to communicate the status of the FEC degraded feature to the remote PCS. If there is no extender sublayer between the PCS and the MAC, it is set as follows:

tx_am_sf<2:0> = {FEC_degraded_SER + rx_local_degraded,0,0}

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If there is a Clause 118 extender sublayer between the PCS and the MAC, it is set as follows:

tx_am_sf<2:0> = {PHY_XS:rx_rm_degraded, PHY_XS:FEC_degraded_SER, 0}

Where PHY_XS:rx_rm_degraded and PHY_XS:FEC_degraded_SER are the rx_rm_degraded and FEC_degraded_SER variables from the adjacent PHY_XS sublayer.

See 119.2.5.3 for more information on the optional FEC degrade feature.

119.2.4.4.1 AM creation for the 200GBASE-R PCS

For the 200GBASE-R PCS, the alignment marker mapping function creates a set of 8 alignment markers, and in combination with an additional 65-bit PRBS9 pad and a 3-bit status field, the PCS generates an alignment marker group. Let am_*x*<119:0> be the alignment marker for PCS lane *x*, *x*=0 to 7, where bit 0 is the first bit transmitted. The alignment markers shall be mapped to am_mapped<959:0> in a manner that yields the same result as the following process.

For *x*=0 to 7, am_*x*<119:0> is constructed as follows:

am_*x*<119:0> is set to CM_0, CM_1, CM_2, UP_0, CM_3, CM_4, CM_5, UP_1, UM_0, UM_1, UM_2, UP_2, UM_3, UM_4 and UM_5, as shown in Figure 119–4 (bits 119:0) using the values in Table 119–1 for PCS lane number *x*.

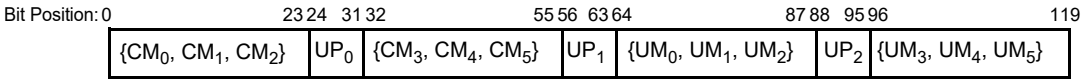

Figure 119–4—Alignment marker format

Table 119–1—200GBASE-R alignment marker encodings

PCS lane number	Encoding[a] {CM_0,CM_1,CM_2,UP_0,CM_3,CM_4,CM_5,UP_1,UM_0,UM_1,UM_2,UP_2,UM_3,UM_4,UM_5}
0	0x9A,0x4A,0x26,0x05,0x65,0xB5,0xD9,0xD6,0xB3,0xC0,0x8C,0x29,0x4C,0x3F,0x73
1	0x9A,0x4A,0x26,0x04,0x65,0xB5,0xD9,0x67,0x5A,0xDE,0x7E,0x98,0xA5,0x21,0x81
2	0x9A,0x4A,0x26,0x46,0x65,0xB5,0xD9,0xFE,0x3E,0xF3,0x56,0x01,0xC1,0x0C,0xA9
3	0x9A,0x4A,0x26,0x5A,0x65,0xB5,0xD9,0x84,0x86,0x80,0xD0,0x7B,0x79,0x7F,0x2F
4	0x9A,0x4A,0x26,0xE1,0x65,0xB5,0xD9,0x19,0x2A,0x51,0xF2,0xE6,0xD5,0xAE,0x0D
5	0x9A,0x4A,0x26,0xF2,0x65,0xB5,0xD9,0x4E,0x12,0x4F,0xD1,0xB1,0xED,0xB0,0x2E
6	0x9A,0x4A,0x26,0x3D,0x65,0xB5,0xD9,0xEE,0x42,0x9C,0xA1,0x11,0xBD,0x63,0x5E
7	0x9A,0x4A,0x26,0x22,0x65,0xB5,0xD9,0x32,0xD6,0x76,0x5B,0xCD,0x29,0x89,0xA4

[a] Each octet is transmitted LSB to MSB.

As an example, the variable am_0 is sent as (left most bit sent first, showing the first 32 bits transmitted of am_0):

01011001 01010010 01100100 10100000

The variable am_mapped is then derived from 10-bit interleaving the group of 8 alignment markers am_*x* per the following procedure:

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For all *k*=0 to 11
  For all *j*=0 to 3
    if even(*k*)
      am_mapped<80*k*+20*j*+9:80*k*+20*j*> = am_{2*j*}<10*k*+9:10*k*>
      am_mapped<80*k*+20*j*+19:80*k*+20*j*+10> = am_{2*j*+1}<10*k*+9:10*k*>
    else
      am_mapped<80*k*+20*j*+9:80*k*+20*j*> = am_{2*j*+1}<10*k*+9:10*k*>
      am_mapped<80*k*+20*j*+19:80*k*+20*j*+10> = am_{2*j*}<10*k*+9:10*k*>

The additional 65-bit pad is appended to variable am_mapped as follows:

am_mapped<1024:960> = PRBS9<64:0>

In this expression, PRBS9<0> is the first PRBS9 bit output of the 65-bit pad.

The 3-bit transmit alignment marker status field is then appended to the variable am_mapped as follows:

am_mapped<1027:1025> = tx_am_sf<2:0>

Alignment marker mapping is shown in Figure 119–5.

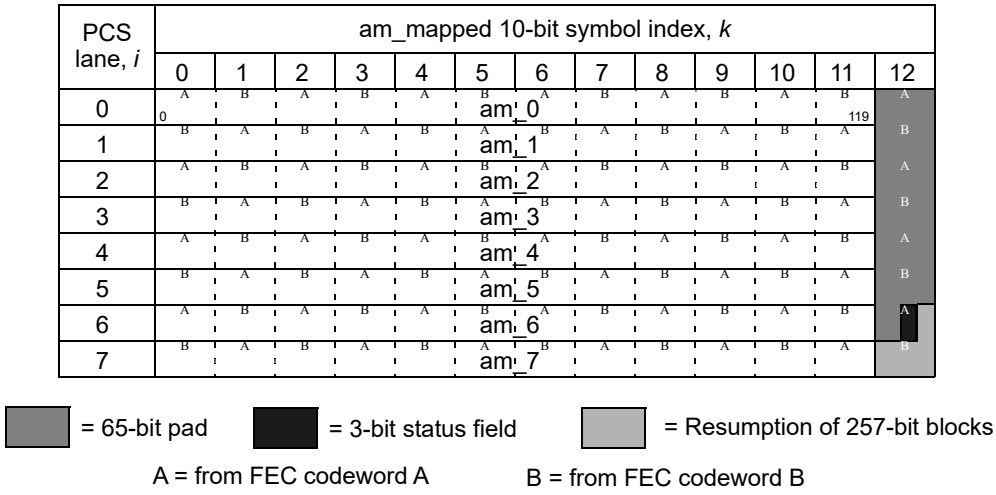

Figure 119–5—200GBASE-R alignment marker mapping to PCS lanes

The alignment marker group am_mapped<1027:0> shall be inserted so it appears in the output stream every 81 920 × 257-bit blocks. The variable tx_scrambled_am<10279:0> is constructed in one of two ways. Let the set of vectors tx_scrambled_*i*<256:0> represent consecutive values of tx_scrambled<256:0>.

For a 10280-bit block with an alignment marker group inserted:

tx_scrambled_am<1027:0> = am_mapped<1027:0>
For all *i*=0 to 35
  tx_scrambled_am<257*i*+1284:257*i*+1028> = tx_scrambled_*i*<256:0>

For a 10280-bit block without an alignment marker group:
For all *i*=0 to 39
  tx_scrambled_am<257*i*+256:257*i*> = tx_scrambled_*i*<256:0>

Alignment marker repetition rate is shown in Figure 119–6.

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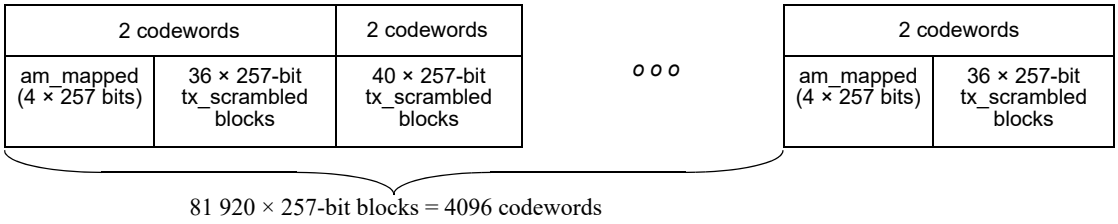

Figure 119–6—200GBASE-R alignment marker insertion period

119.2.4.4.2 AM creation for the 400GBASE-R PCS

For the 400GBASE-R PCS, the alignment marker mapping function creates a set of 16 alignment markers, and in combination with an additional 133-bit PRBS9 pad and a 3-bit status field, the PCS generates an alignment marker group.

Let am_*x*<119:0> be the alignment marker for PCS lane *x*, *x*=0 to 15, where bit 0 is the first bit transmitted. The alignment markers shall be mapped to am_mapped<1919:0> in a manner that yields the same result as the following process.

For *x*=0 to *15*, am_*x*<119:0> is constructed as follows:

am_*x*<119:0> is set to CM_0, CM_1, CM_2, UP_0, CM_3, CM_4, CM_5, UP_1, UM_0, UM_1, UM_2, UP_2, UM_3, UM_4 and UM_5, as shown in Figure 119–4 (bits 119:0) using the values in Table 119–2 for PCS lane number *x*.

Table 119–2—400GBASE-R alignment marker encodings

PCS lane number	Encoding[a] {CM_0,CM_1,CM_2,UP_0,CM_3,CM_4,CM_5,UP_1,UM_0,UM_1,UM_2,UP_2,UM_3,UM_4,UM_5}
0	0x9A,0x4A,0x26,0xB6,0x65,0xB5,0xD9,0xD9,0x01,0x71,0xF3,0x26,0xFE,0x8E,0x0C
1	0x9A,0x4A,0x26,0x04,0x65,0xB5,0xD9,0x67,0x5A,0xDE,0x7E,0x98,0xA5,0x21,0x81
2	0x9A,0x4A,0x26,0x46,0x65,0xB5,0xD9,0xFE,0x3E,0xF3,0x56,0x01,0xC1,0x0C,0xA9
3	0x9A,0x4A,0x26,0x5A,0x65,0xB5,0xD9,0x84,0x86,0x80,0xD0,0x7B,0x79,0x7F,0x2F
4	0x9A,0x4A,0x26,0xE1,0x65,0xB5,0xD9,0x19,0x2A,0x51,0xF2,0xE6,0xD5,0xAE,0x0D
5	0x9A,0x4A,0x26,0xF2,0x65,0xB5,0xD9,0x4E,0x12,0x4F,0xD1,0xB1,0xED,0xB0,0x2E
6	0x9A,0x4A,0x26,0x3D,0x65,0xB5,0xD9,0xEE,0x42,0x9C,0xA1,0x11,0xBD,0x63,0x5E
7	0x9A,0x4A,0x26,0x22,0x65,0xB5,0xD9,0x32,0xD6,0x76,0x5B,0xCD,0x29,0x89,0xA4
8	0x9A,0x4A,0x26,0x60,0x65,0xB5,0xD9,0x9F,0xE1,0x73,0x75,0x60,0x1E,0x8C,0x8A
9	0x9A,0x4A,0x26,0x6B,0x65,0xB5,0xD9,0xA2,0x71,0xC4,0x3C,0x5D,0x8E,0x3B,0xC3
10	0x9A,0x4A,0x26,0xFA,0x65,0xB5,0xD9,0x04,0x95,0xEB,0xD8,0xFB,0x6A,0x14,0x27
11	0x9A,0x4A,0x26,0x6C,0x65,0xB5,0xD9,0x71,0x22,0x66,0x38,0x8E,0xDD,0x99,0xC7
12	0x9A,0x4A,0x26,0x18,0x65,0xB5,0xD9,0x5B,0xA2,0xF6,0x95,0xA4,0x5D,0x09,0x6A
13	0x9A,0x4A,0x26,0x14,0x65,0xB5,0xD9,0xCC,0x31,0x97,0xC3,0x33,0xCE,0x68,0x3C
14	0x9A,0x4A,0x26,0xD0,0x65,0xB5,0xD9,0xB1,0xCA,0xFB,0xA6,0x4E,0x35,0x04,0x59
15	0x9A,0x4A,0x26,0xB4,0x65,0xB5,0xD9,0x56,0xA6,0xBA,0x79,0xA9,0x59,0x45,0x86

[a] Each octet is transmitted LSB to MSB.

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As an example, the variable am_0 is sent as (left most bit sent first, showing the first 32 bits transmitted of am_0):

01011001 01010010 01100100 01101101

The variable am_mapped is then derived from 10-bit interleaving the group of 16 alignment markers am_*x* per the following procedure:

For all *k*=0 to 11
  For all *j*=0 to 7
    if even(*k*)
      am_mapped<160*k*+20*j*+9:160*k*+20*j*> = am_{2*j*}<10*k*+9:10*k*>
      am_mapped<160*k*+20*j*+19:160*k*+20*j*+10> = am_{2*j*+1}<10*k*+9:10*k*>
    else
      am_mapped<160*k*+20*j*+9:160*k*+20*j*> = am_{2*j*+1}<10*k*+9:10*k*>
      am_mapped<160*k*+20*j*+19:160*k*+20*j*+10> = am_{2*j*}<10*k*+9:10*k*>

The additional 133-bit pad is appended to variable am_mapped as follows:

am_mapped<2052:1920> = PRBS9<132:0>

In this expression, PRBS9<0> is the first PRBS9 bit output of the 133-bit pad.

The 3-bit transmit alignment marker status field is then appended to the variable am_mapped as follows:

am_mapped<2055:2053> = tx_am_sf<2:0>

Alignment marker mapping is shown in Figure 119–7.

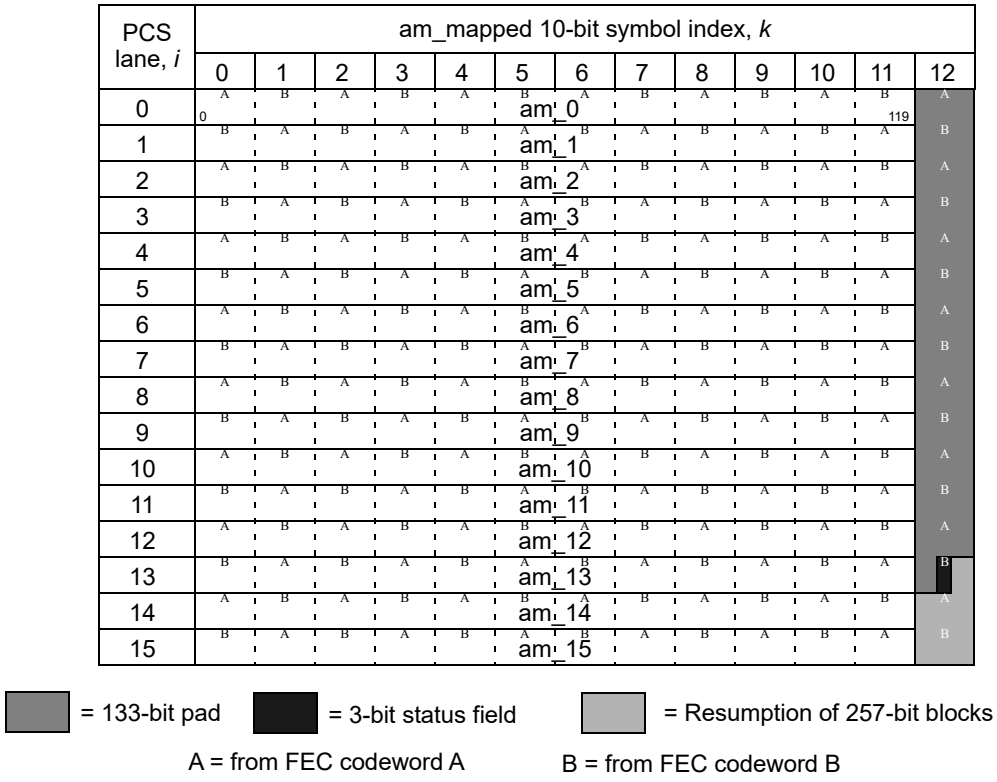

Figure 119–7—400GBASE-R alignment marker mapping to PCS lanes

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The alignment marker group am_mapped<2055:0> shall be inserted so it appears in the output stream every 163 840 × 257-bit blocks. The variable tx_scrambled_am<10279:0> is constructed in one of two ways. Let the set of vectors tx_scrambled_*i*<256:0> represent consecutive values of tx_scrambled<256:0>.

For a 10280-bit block with an alignment marker group inserted:
tx_scrambled_am<2055:0> = am_mapped<2055:0>
For all *i*=0 to 31
  tx_scrambled_am<257*i*+2312:257*i*+2056> = tx_scrambled_*i*<256:0>

For a 10280-bit block without an alignment marker group:
For all *i*=0 to 39
  tx_scrambled_am<257*i*+256:257*i*> = tx_scrambled_*i*<256:0>

Alignment marker repetition rate is shown in Figure 119–8.

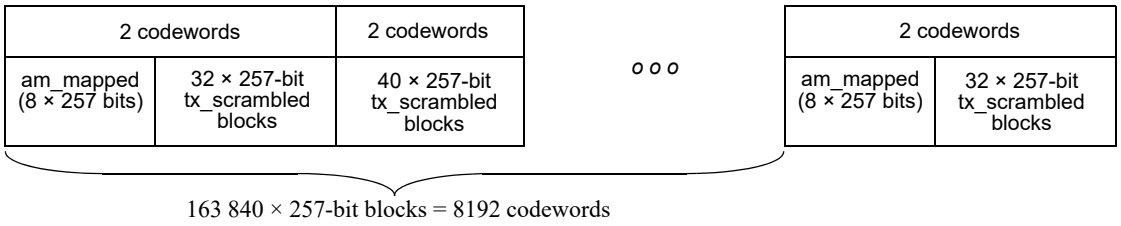

Figure 119–8—400GBASE-R alignment marker insertion period

119.2.4.5 Pre-FEC distribution

In order to improve error correction capability, each set of two consecutive Reed-Solomon FEC codewords is interleaved before being distributed to form the PCS lanes. To enable this interleaving, the Pre-FEC distribution function receives a 10280-bit block tx_scrambled_am, and shall perform a 10-bit symbol round robin distribution to form two 514-symbol FEC messages, m_A and m_B, which are subsequently each encoded by the RS FEC. The following describes the 10-bit round robin distribution process.

For all *i*=0 to 513

m_A<(513–*i*)> = tx_scrambled_am<(20*i*+9):(20*i*)>
m_B<(513–*i*)> = tx_scrambled_am<(20*i*+19):(20*i*+10)>

119.2.4.6 Reed-Solomon encoder

The PCS sublayer employs a Reed-Solomon code operating over the Galois Field GF(2^{10}) where the symbol size is 10 bits. The encoder processes *k* message symbols to generate 2*t* parity symbols, which are then appended to the message to produce a codeword of *n*=*k*+2*t* symbols. For the purposes of this clause, a particular Reed-Solomon code is denoted RS(*n*,*k*).

The PCS shall implement an RS(544,514) based FEC encoder. The PCS distributes a group of 40 × 257-bit blocks from tx_scrambled_am on a 10-bit round robin basis into two 5140-bit message blocks, $m_A$and m_B, as described in 119.2.4.5. These are then encoded using RS(544,514) encoder into codeword A and codeword B, respectively. The RS(544,514) code is based on the generating polynomial given by Equation (119–1).

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$$g(x) = \prod_{j=0}^{2t-1}(x-\alpha^j) = g_{2t}x^{2t} + g_{2t-1}x^{2t-1} + \ldots + g_1 x + g_0 \quad (119\text{–}1)$$

In Equation (119–1), α is a primitive element of the finite field defined by the polynomial $x^{10}+x^3+1$.

Equation (119–2) defines the message polynomial $m(x)$ whose coefficients are the message symbols m_{k-1} to m_0.

$$m(x) = m_{k-1}x^{n-1} + m_{k-2}x^{n-2} + \ldots + m_1 x^{2t+1} + m_0 x^{2t} \quad (119\text{–}2)$$

Each message symbol m_i is the bit vector $(m_{i,9}, m_{i,8}, \ldots, m_{i,1}, m_{i,0})$, which is identified with the element $m_{i,9}\alpha^9 + m_{i,8}\alpha^8 + \ldots + m_{i,1}\alpha + m_{i,0}$ of the finite field. The message symbols are composed of the variable m_A for codeword A and m_B for codeword B (including a group of alignment markers when appropriate). The first symbol input to the encoder is m_{k-1}.

Equation (119–3) defines the parity polynomial $p(x)$ whose coefficients are the parity symbols p_{2t-1} to p_0.

$$p(x) = p_{2t-1}x^{2t-1} + p_{2t-2}x^{2t-2} + \ldots + p_1 x + p_0 \quad (119\text{–}3)$$

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This may be computed using the shift register implementation illustrated in Figure 119–9. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0, is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

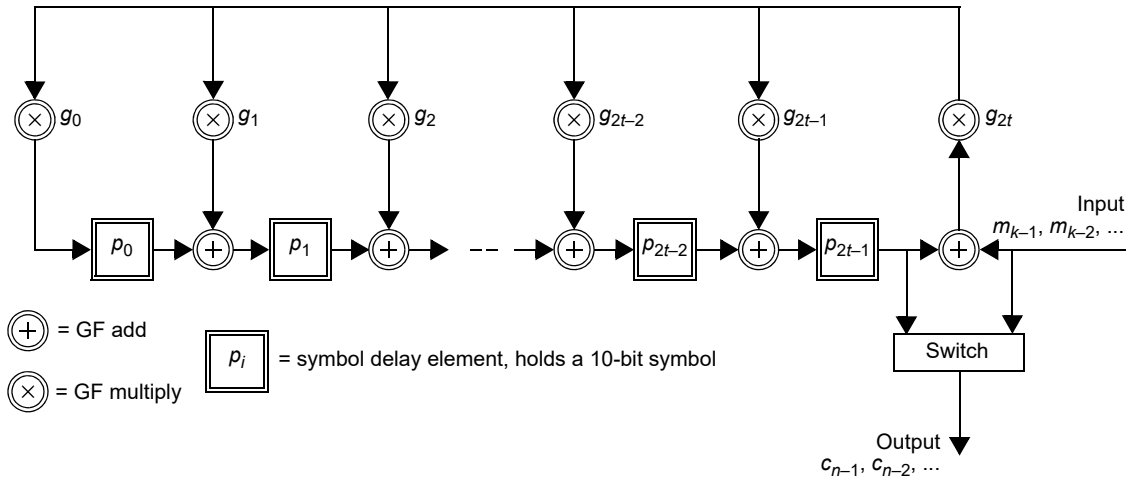

Figure 119–9—Reed-Solomon encoder functional model

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x, $c_{n-1} = m_{k-1}$ is first and the coefficient of the lowest power of x, $c_0 = p_0$ is last.

The coefficients of the generator polynomial for the RS(544,514) code are presented in Table 119–3. Example codewords for the RS(544,514) code are provided in Annex 119A.

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Table 119–3—Coefficients of the generator polynomial g_i (decimal)

i	g_i	i	g_i	i	g_i
0	523	11	883	22	565
1	834	12	503	23	108
2	128	13	942	24	1
3	158	14	385	25	552
4	185	15	495	26	230
5	127	16	720	27	187
6	392	17	94	28	552
7	193	18	132	29	575
8	610	19	593	30	1
9	788	20	249		
10	361	21	282		

119.2.4.7 Symbol distribution

Once the data has been FEC encoded, two FEC codewords (c_A<543:0> and c_B<543:0>) are interleaved on a 10-bit basis before the data is distributed to each PCS lane.

The interleaving of two codewords for the 200GBASE-R PCS shall follow this procedure:

For all k=0 to 135
For all j=0 to 3
    if even(k)
        tx_out<$8k+2j$> = c_A<$543-4k-j$>
        tx_out<$8k+2j+1$> = c_B<$543-4k-j$>
    else
        tx_out<$8k+2j$> = c_B<$543-4k-j$>
        tx_out<$8k+2j+1$> = c_A<$543-4k-j$>

The interleaving of two codewords for the 400GBASE-R PCS shall follow this procedure:

For all k=0 to 67
For all j=0 to 7
    if even(k)
        tx_out<$16k+2j$> = c_A<$543-8k-j$>
        tx_out<$16k+2j+1$> = c_B<$543-8k-j$>
    else
        tx_out<$16k+2j$> = c_B<$543-8k-j$>
        tx_out<$16k+2j+1$> = c_A<$543-8k-j$>

Once the data has been Reed-Solomon encoded and interleaved, it shall be distributed to 8 PCS lanes for a 200GBASE-R PCS and to 16 PCS lanes for a 400GBASE-R PCS, one 10-bit symbol at a time, from the lowest to the highest PCS lane. The first bit transmitted from each 10-bit symbol is bit 0.

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119.2.4.8 Transmit bit ordering and distribution

The transmit bit ordering and distribution are illustrated in Figure 119–10 for a 200GBASE-R PCS.

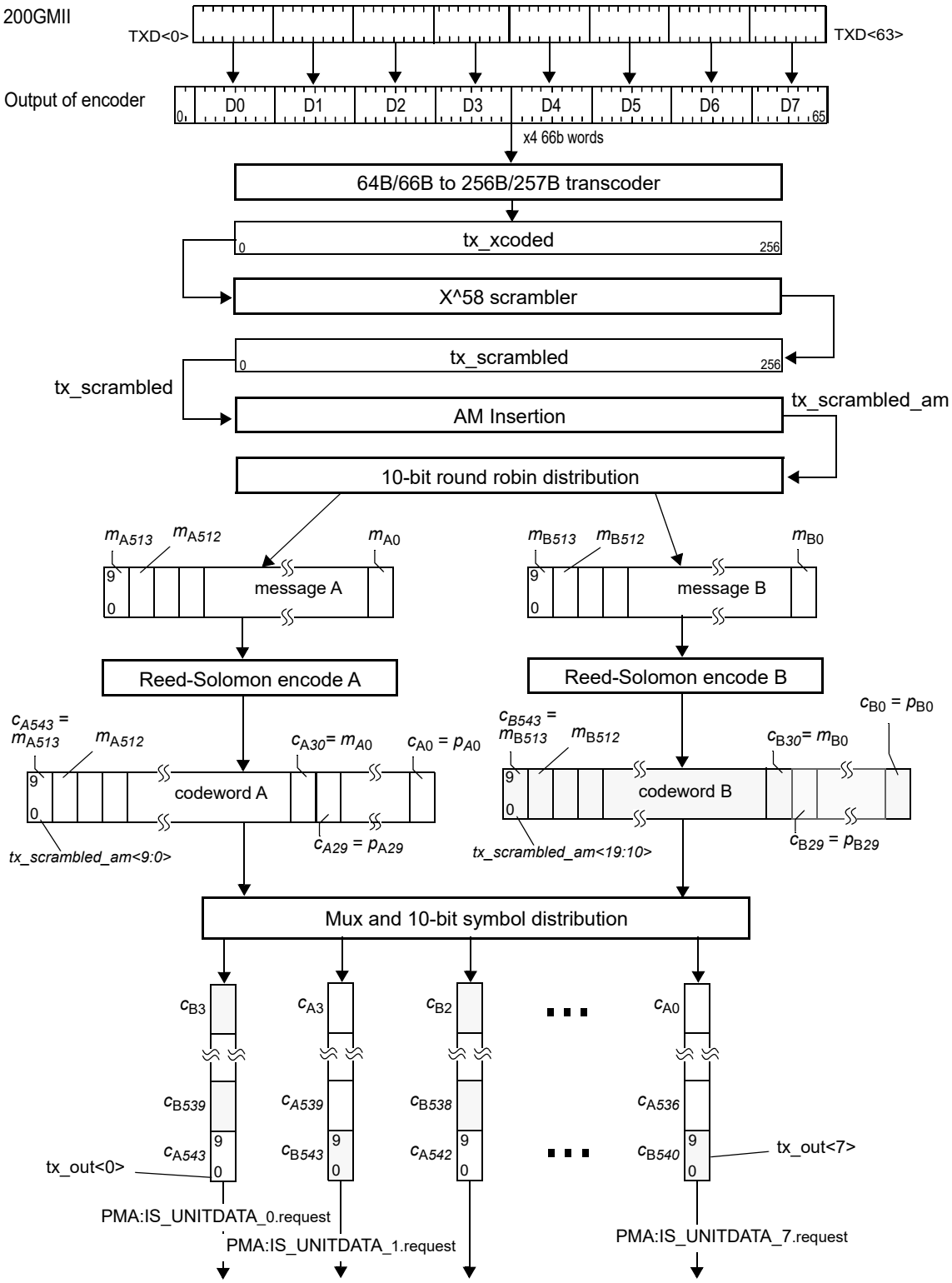

Figure 119–10—200GBASE-R Transmit bit ordering and distribution

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The transmit bit ordering and distribution is illustrated in Figure 119–11 for a 400GBASE-R PCS.

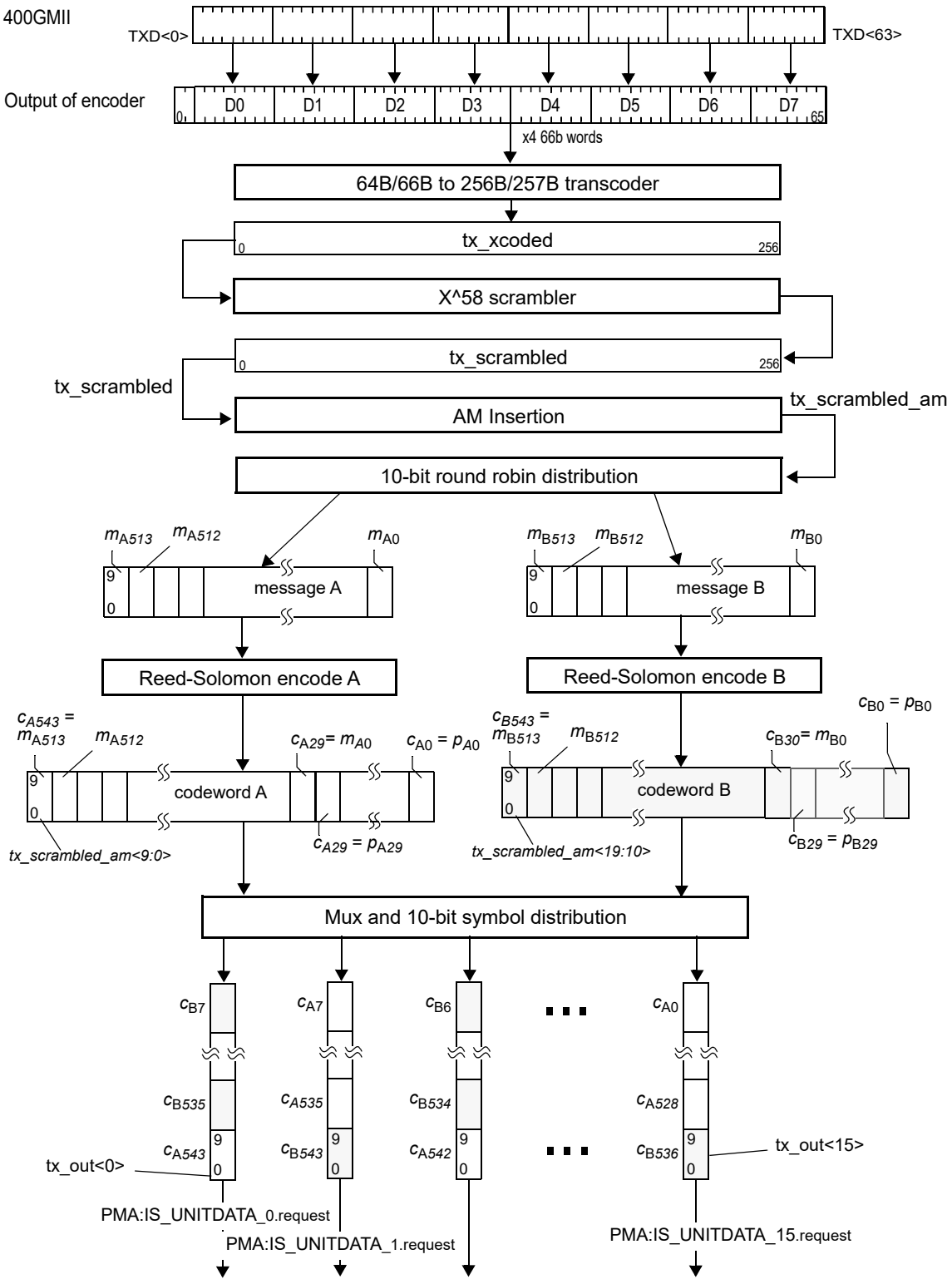

Figure 119–11—400GBASE-R Transmit bit ordering and distribution

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119.2.4.9 Test-pattern generators

The PCS shall have the ability to generate a scrambled idle test pattern which is suitable for receiver tests and for certain transmitter tests. When a scrambled idle pattern is enabled, the test pattern is generated by the PCS. The test pattern is an idle control block (block type=0x1E) with all idles as defined in Figure 82–5. The test pattern is sent continuously and is transcoded, scrambled, alignment markers are inserted and finally encapsulated by the FEC.

When the transmit channel is operating in test-pattern mode, the encoded bit stream is distributed to the PCS Lanes as in normal operation (see 119.2.4.7).

If a Clause 45 MDIO is implemented, then control of the test-pattern generation is from the BASE-R PCS test-pattern control register (bit 3.42.3).

119.2.5 Receive function

119.2.5.1 Alignment lock and deskew

The receive PCS forms *n* separate bit streams by concatenating the bits from each of the *n* PMA:IS_UNITDATA_*i*.indication primitives in the order they are received (where *n* = 8 for a 200GBASE-R PCS and *n* = 16 for a 400GBASE-R PCS). It obtains lock to the alignment markers as specified by the alignment marker lock state diagram shown in Figure 119–12. Note that alignment marker lock is achieved before FEC codewords are processed and therefore the alignment markers are processed in a high error probability environment.

After alignment marker lock is achieved on each of the *n* lanes (bit streams), all inter-lane Skew is removed as specified by the PCS synchronization state diagram shown in Figure 119–13. The PCS receive function shall support a maximum Skew of 180 ns, and maximum Skew Variation of 4 ns, between PCS lanes.

119.2.5.2 Lane reorder and de-interleave

PCS lanes can be received on different lanes of the service interface from which they were originally transmitted. The PCS receive function shall order the PCS lanes according to the PCS lane number. The PCS lane number is defined by the unique portion (UM_0 to UM_5) of the alignment marker that is mapped to each PCS lane (see 119.2.4.4).

After all PCS lanes are aligned, deskewed, and reordered, the two FEC codewords are de-interleaved to reconstruct the original stream of two FEC codewords.

119.2.5.3 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the codeword, corrects them as necessary, and discards the parity symbols.

The Reed-Solomon decoder shall be capable of correcting any combination of up to t=15 symbol errors in a codeword. The Reed-Solomon decoder shall also be capable of indicating when an errored codeword was not corrected. The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10^{-16}. This limit is also expected to apply for t+2 errors, t+3 errors, and so on.

If bypass error indication is not supported or not enabled, when the Reed-Solomon decoder determines that a codeword contains errors that were not corrected, it shall cause the PCS receive function to set every 66-bit block within the two associated codewords to an error block (set to EBLOCK_R). This may be achieved by setting the synchronization header to 11 for all 66-bit blocks created from these codewords by the 256B/257B to 64B/66B transcoder.

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The Reed-Solomon decoder may optionally provide the ability to bypass the error indication feature to reduce the delay contributed by the FEC function. The presence of this option is indicated by the assertion of the FEC_bypass_indication_ability variable (see 119.3). When the option is provided it is enabled by the assertion of the FEC_bypass_indication_enable variable (see 119.3).

When FEC_bypass_indication_enable is asserted, additional error monitoring is performed by the Reed-Solomon decoder to reduce the likelihood that errors in a packet are not detected. The Reed-Solomon decoder counts the number of symbol errors detected on all PCS lanes in consecutive non-overlapping blocks of 8192 codewords. When the number of symbol errors in a block of 8192 codewords exceeds 5560, the Reed-Solomon decoder shall assert hi_ser for a period of 60 ms to 75 ms.

The Reed-Solomon decoder may optionally provide the ability to signal a degradation of the received signal. The presence of this option is indicated by the assertion of the FEC_degraded_SER_ability variable (see 119.3). When the option is provided it is enabled by the assertion of the FEC_degraded_SER_enable variable (see 119.3).

When FEC_degraded_SER_enable is asserted, additional error monitoring is performed by the PCS. The Reed-Solomon decoder counts the number of symbol errors detected on all PCS lanes in consecutive non-overlapping blocks of FEC_degraded_SER_interval codewords (see 119.3.1), where the least significant bit of FEC_degraded_SER_interval is ignored (evaluated as 0) to make the number of codewords even. If the decoder determines that a codeword is uncorrectable, the number of symbol errors detected is increased by 16. When the number of symbol errors exceeds the threshold set in FEC_degraded_SER_activate_threshold (see 119.3.1), the FEC_degraded_SER bit (see 119.3.1) is set. At the end of each interval, if the number of symbol errors is less than FEC_degraded_SER_deactivate_threshold, the FEC_degraded_SER bit is cleared. If either FEC_degraded_SER_ability or FEC_degraded_SER_enable is de-asserted then the FEC_degraded_SER bit is cleared.

119.2.5.4 Post FEC interleave

After the Reed-Solomon decoder processes the data, data is interleaved on a 10-bit basis into rx_scrambled_am from two codewords corresponding to 40 transcoded blocks in order to recreate the transmitted data stream.

119.2.5.5 Alignment marker removal

For the 200GBASE-R PCS, every 81 920 x 257-bit blocks (corresponds to 4096 codewords) the first 1028 bits of rx_scrambled_am blocks is the vector am_rx<1027:0> where bit 0 is the first bit received. The specific codewords that include this vector are indicated by the alignment lock and deskew function. The 3-bit receive alignment marker status field is assigned from the variable am_rx as follows:

rx_am_sf<2:0> = am_rx<1027:1025>

For the 400GBASE-R PCS, every 163 840 x 257-bit blocks (corresponds to 8192 codewords) the first 2056 bits of rx_scrambled_am blocks is the vector am_rx<2055:0> where bit 0 is the first bit received. The specific codewords that include this vector are indicated by the alignment lock and deskew function. The 3-bit receive alignment marker status field is assigned from the variable am_rx as follows:

rx_am_sf<2:0> = am_rx<2055:2053>

The vector am_rx shall be removed from rx_scrambled_am to create rx_scrambled prior to descrambling.

119.2.5.6 Descrambler

The descrambler shall process rx_scrambled<256:0> to reverse the effect of the scrambler using the polynomial given in Equation (49–1).

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119.2.5.7 256B/257B to 64B/66B transcoder

The transcoder extracts a group of four 66-bit blocks, rx_coded_*j*<65:0> where *j*=0 to 3, from each 257-bit block rx_xcoded<256:0>. Bit 0 of the 257-bit block is the first bit received.

If rx_xcoded<0> is 1, rx_coded_*j*<65:0> for *j*=0 to 3 shall be derived as follows.

a) rx_coded_*j*<65:2> = rx_xcoded<(64*j*+64):(64*j*+1)> for *j*=0 to 3

b) rx_coded_*j*<0>=0 and rx_coded_*j*<1>=1 for all *j*=0 to 3

If rx_xcoded<0> is 0 and any rx_xcoded<*j*+1>=0 for *j*=0 to 3, rx_coded_*j*<65:0> for *j*=0 to 3 shall be derived as follows.

a1) Let *c* be the smallest value of *j* such that rx_xcoded<*j*+1>=0. In other words, rx_coded_*c* is the first 66-bit control block in the resulting group of four blocks.

b1) Let rx_payloads be a vector representing the payloads of the four 66-bit blocks. It is derived using the following expressions:
rx_payloads<(64*c*+3):0> = rx_xcoded<(64*c*+8):5>
rx_payloads<(64c+7):(64c+4)> is set to a value derived by cross-referencing rx_payloads<(64c+3):64c> using Figure 82–5. For example, if rx_payloads<(64c+3):64c> is 0xE then rx_payloads<(64c+7):(64c+4)> is 0x1. If no match to rx_payloads<(64c+3):64c> is found, rx_payloads<(64c+7):(64c+4)> is set to 0000
rx_payloads<255:(64*c*+8)> = rx_xcoded<256:(64*c*+9)>

c1) rx_coded_*j*<65:2> = rx_payloads<(64*j*+63):64*j*> for *j*=0 to 3

d1) If rx_xcoded<*j*+1>=0, rx_coded_*j*<0>=1 and rx_coded_*j*<1>=0 for *j*=0 to 3

e1) If rx_xcoded<*j*+1>=1, rx_coded_*j*<0>=0 and rx_coded_*j*<1>=1 for *j*=0 to 3

f1) If rx_payloads<(64c+7):(64c+4)> = 0000, rx_coded_c<1>=1 (invalidate synchronization header)

If rx_xcoded<0> is 0 and all rx_xcoded<*j*+1>=1 for *j*=0 to 3, rx_coded_*j*<65:0> for *j*=0 to 3 shall be derived as follows.

a2) Set *c* = 0

b2) Let rx_payloads be a vector representing the payloads of the four 66-bit blocks. It is derived using the following expressions.
rx_payloads<(64*c*+3):0> = rx_xcoded<(64*c*+8):5>
rx_payloads<(64*c*+7):(64*c*+4)> = 0000
rx_payloads<255:(64*c*+8)> = rx_xcoded<256:(64*c*+9)>

c2) rx_coded_*j*<65:2> = rx_payloads<(64*j*+63):(64*j*)> for *j*=0 to 3

d2) rx_coded_*j*<0>=0 and rx_coded_*j*<1>=0 for *j*=0 and 2

e2) rx_coded_*j*<0>=1 and rx_coded_*j*<1>=1 for *j*=1 and 3

The 66-bit blocks are transmitted in order from *j*=0 to 3. Bit 0 of each block is the first bit transmitted.

NOTE—The stream of 66-bit blocks generated by this process is used as the reference signal for de-mapping from OTN. See ITU-T G.709.

119.2.5.8 Decode and rate matching

The receive PCS decodes blocks to produce RXD<63:0> and RXC<7:0> for transmission to the 200GMII/400GMII. One 200GMII/400GMII data transfer is decoded from each block. The receive PCS may insert idle control characters to compensate for the removal of alignment markers. If the receive PCS spans multiple clock domains, it may also perform clock rate compensation via the deletion of idle control characters or sequence ordered sets or the insertion of idle control characters (see 82.2.3.6 and 82.2.3.9 for insertion and deletion rules).

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The PCS receive decodes blocks as specified in the receive state diagram shown in Figure 119–15.

119.2.6 Detailed functions and state diagrams

119.2.6.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, functions, and counters. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

119.2.6.2 State variables

119.2.6.2.1 Constants

EBLOCK_R<71:0>
: 72-bit vector to be sent to the 200GMII/400GMII containing /E/ in all the eight character locations.

EBLOCK_T<65:0>
: 66-bit vector to be sent to the transcoder containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
: 72-bit vector to be sent to the 200GMII/400GMII containing one Local Fault ordered set. The Local Fault ordered set is defined in 119.3.

LBLOCK_T<65:0>
: 66-bit vector to be sent to the transcoder containing one Local Fault ordered set.

119.2.6.2.2 Variables

align_status
: A variable set by the PCS synchronization process to reflect the status of PCS lane-to-lane alignment. Set to true when all lanes are synchronized and aligned and set to false when the PCS synchronization process is not complete.

all_locked
: A Boolean variable that is set to true when amps_lock<*x*> is true for all *x* and is set to false when amps_lock<*x*> is false for any *x*.

amp_counter_done
: Boolean variable that indicates that amp_counter has reached its terminal count.

amp_match
: Boolean variable that holds the output of the function AMP_COMPARE.

amp_valid
: Boolean variable that is set to true if the received 120-bit block is a valid alignment marker payload. The alignment marker payload, mapped to a PCS lane according to the process described in 119.2.4.4, consists of 96 known bits. The 48 bits of the common marker portion are compared on a nibble-wise basis (12 comparisons). If 9 or more nibbles in the candidate block match the corresponding known nibbles in the common portion of the alignment marker payload, the candidate block is considered a valid alignment marker payload.

amps_lock<*x*>
: Boolean variable that is set to true when the receiver has detected the location of the alignment marker payload sequence for a given lane on the PMA service interface, where *x* = 0:7 for 200GBASE-R and *x* = 0:15 for 400GBASE-R

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current_pcsl

A variable that holds the PCS lane number corresponding to the current alignment marker payload that is recognized on a given lane of the PMA service interface. It is compared to the variable first_pcsl to confirm that the location of the alignment marker payload sequence has been detected. The PCS lane number is determined by the alignment marker payloads based on the mapping defined in 119.2.4.4. The 48 bits that are in the positions of the unique marker bits in the received alignment marker payload are compared to the expected values for a given payload position and PCS lane on a nibblewise basis (12 comparisons). If 9 or more nibbles in the candidate block match the corresponding known nibbles for any payload position on a given PCS lane, then the PCS lane number is assigned accordingly. If a match is not found, then the AMP_COMPARE function sets amp_match to false.

cw_A_bad

A Boolean variable that is set to true if the Reed-Solomon decoder (see 119.2.5.3) fails to correct the current FEC codeword A and is set to false otherwise.

cw_B_bad

A Boolean variable that is set to true if the Reed-Solomon decoder (see 119.2.5.3) fails to correct the current FEC codeword B and is set to false otherwise.

deskew_done

A Boolean variable that is set to true when pcs_enable_deskew is set to true and the deskew process is completed. Otherwise, this variable is set to false.

first_pcsl

A variable that holds the PCS lane number that corresponds to the first alignment marker payload that is recognized on a given lane of the PMA service interface. It is compared to the PCS lane number corresponding to the second alignment marker payload that is tested.

hi_ser

When FEC_bypass_indication_enable is set to one, this bit is set to one for a period of 60 ms to 75 ms if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 119.2.5.3), and is set to zero otherwise. When FEC_bypass_indication_enable is set to zero, this bit is set to zero. This variable is mapped to the bit defined in 45.2.3.61 (3.801.2).

pcs_alignment_valid

Boolean variable that is set to true if all PCS lanes are aligned. PCS lanes are considered to be aligned when amps_lock<*x*> is true for all *x*, each PCS lane is locked to a unique alignment marker payload sequence (see 119.2.4.4), and the PCS lanes are deskewed. Otherwise, this variable is set to false.

pcs_enable_deskew

A Boolean variable that enables and disables the PCS synchronization process. Received bits may be discarded whenever deskew is enabled. It is set to true when deskew is enabled and set to false when deskew is disabled.

pcs_lane_mapping<*x*>

A variable that holds the value of the pcs_lane received on physical lane *x*.

PCS_status

A Boolean variable that is true when align_status is true and is false otherwise.

reset

Boolean variable that controls the resetting of the PCS sublayer. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS sublayer into low-power mode.

restart_lock

Boolean variable that is set by the PCS synchronization process to restart the alignment marker lock process on all PCS lanes. It is set to true after 3 consecutive uncorrected codewords are received (3_BAD state) and set to false upon entry into the LOSS_OF_ALIGNMENT state.

rx_coded<65:0>

Vector containing the input to the 64B/66B decoder. The format for this vector is shown in Figure 82–5. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<65>.

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rx_local_degraded
: Boolean variable that is asserted true when the receiver detects rx_am_sf<1> asserted true for two consecutive alignment marker periods. It is deasserted when rx_am_sf<1> is deasserted for two consecutive alignment marker periods. If a Clause 45 MDIO is implemented, the status of this variable is reflected in bit 3.801.6.

rx_raw<71:0>
: Vector containing one 200GMII/400GMII transfer. RXC<0> through RXC<7> are from rx_raw<0> through rx_raw<7>, respectively. RXD<0> through RXD<63> are from rx_raw<8> through rx_raw<71>, respectively.

rx_rm_degraded
: Boolean variable that is asserted true when the receiver detects rx_am_sf<2> asserted true for two consecutive alignment marker periods. It is deasserted when rx_am_sf<2> is deasserted for two consecutive alignment marker periods. If a Clause 45 MDIO is implemented, the status of this variable is reflected in bit 3.801.5.

signal_ok
: Boolean variable that is set based on the most recently received value of PMA:IS_SIGNAL.indication(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done
: Boolean variable that is set to true when the SLIP requested by the alignment marker lock state diagram has been completed indicating that the next candidate 120-bit block position can be tested.

test_amp
: Boolean variable that is set to true when a candidate block position is available for testing and false when the FIND_1ST state is entered.

test_cw
: Boolean variable that is set to true when a new FEC codeword is available for decoding and is set to false when the TEST_CW state is entered.

tx_coded<65:0>
: Vector containing the output from the 64B/66B encoder. The format for this vector is shown in Figure 82–5. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<65>.

tx_raw<71:0>
: Vector containing one 200GMII/400GMII transfer. TXC<0> through TXC<7> are placed in tx_raw<0> through tx_raw<7>, respectively. TXD<0> through TXD<63> are placed in tx_raw<8> through tx_raw<71>, respectively.

119.2.6.2.3 Functions

AMP_COMPARE
: This function compares the values of first_pcsl and current_pcsl to determine if a valid alignment marker payload sequence has been detected and returns the result of the comparison using the variable amp_match. If current_pcsl and first_pcsl both found a match and indicate the same PCS lane number, amp_match is set to true.

DECODE(rx_coded<65:0>)
: Decodes the 66-bit vector returning rx_raw<71:0>, which is sent to the 200GMII/400GMII. The DECODE function shall decode the block as specified in 119.2.3.

ENCODE(tx_raw<71:0>)
: Encodes the 72-bit vector returning tx_coded<65:0>. The ENCODE function shall encode the block as specified in 119.2.3.

R_TYPE(rx_coded<65:0>)
: This function classifies the current rx_coded<65:0> vector as belonging to one of the following types, depending on its contents. The classification results are returned via the r_block_type variable.

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Values: C; The vector contains a sync header of 10 and one of the following:
a) A block type field of 0x1E and eight valid control characters other than /E/ or /LI/;
b) A block type field of 0x4B.
LI; For EEE capability, the LI type is supported where the vector contains a sync header of 10, a block type field of 0x1E and eight control characters of 0x06 (/LI/).
S; The vector contains a sync header of 10 and the following:
a) A block type field of 0x78.
T; The vector contains a sync header of 10, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.
D; The vector contains a sync header of 01.
E; The vector does not meet the criteria for any other value.

Valid control characters are specified in Table 82–1.

NOTE—A PCS that does not support EEE classifies vectors containing one or more /LI/ control characters as type E.

R_TYPE_NEXT

This function classifies the 66-bit rx_coded vector that immediately follows the current rx_coded<65:0> vector as belonging to one of the five types defined in R_TYPE, depending on its contents. It is intended to perform a prescient end of packet check. The classification results are returned via the r_block_type_next variable.

SLIP

Causes the next candidate block position to be tested. The precise method for determining the next candidate block position is not specified and is implementation dependent. However, an implementation shall ensure that all possible block positions are evaluated.

T_TYPE = (tx_raw<71:0>)

This function classifies each 72-bit tx_raw vector as belonging to one of the following types depending on its contents. The classification results are returned via the t_block_type variable.

Values: C; The vector contains one of the following:
a) Eight valid control characters other than /O/, /S/, /T/, /LI/, and /E/;
b) One valid ordered set.
LI; For EEE capability, this vector contains eight /LI/ characters.
S; The vector contains an /S/ in its first character, and all characters following the /S/ are data characters.
T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.
D; The vector contains eight data characters.
E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an 200GMII/400GMII control code specified in Table 82–1. A valid ordered set consists of a valid /O/ character in the first character and data characters in the seven characters following the /O/. A valid /O/ is any character with a value for O code in Table 82–1.

NOTE—A PCS that does not support EEE classifies vectors containing one or more /LI/ control characters as type E.

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119.2.6.2.4 Counters

amp_bad_count
: Counts the number of consecutive alignment markers that don't match the expected values for a given PCS lane.

amp_counter
: This counter counts the interval of *i* FEC codewords containing normal alignment marker payload sequences (where *i* is 4096 for the 200GBASE-R PCS, and 8192 for the 400GBASE-R PCS).

cw_A_bad_count
: Counts the number of consecutive uncorrected FEC codewords for codeword A. This counter is set to zero when an FEC codeword A is received and cw_A_bad is false.

cw_B_bad_count
: Counts the number of consecutive uncorrected FEC codewords for codeword B. This counter is set to zero when an FEC codeword B is received and cw_B_bad is false.

119.2.6.3 State diagrams

The 200GBASE-R PCS shall implement eight alignment marker lock processes and the 400GBASE-R PCS shall implement sixteen alignment marker lock processes as depicted in Figure 119–12. An alignment marker lock process operates independently on each lane. The alignment marker lock state diagram shown in Figure 119–12 determines when the PCS has obtained alignment marker lock to the received bit stream for a given lane of the service interface. Each alignment marker lock process looks for two valid alignment markers 278 528 × 10-bit Reed-Solomon symbols apart, on a per PCS lane basis, to gain alignment marker lock. When the alignment marker lock process achieves lock for a lane, and if a Clause 45 MDIO is implemented, the PCS shall record the PCS lane number received on that lane of the service interface in the appropriate lane mapping register (3.400 to 3.415). Once in lock, a lane goes out of alignment marker lock when restart_lock is signaled (this occurs when the PCS synchronization process determines that three uncorrectable codewords in a row are seen) or when the alignment marker lock process sees five alignment markers in a row that fail to match the expected pattern on a given lane.

The PCS shall run the synchronization process as depicted in Figure 119–13. The PCS synchronization process is responsible for determining if the PCS is capable of presenting coherent data to the 200GMII/400GMII. The synchronization process ensures that all PCS lanes have alignment marker lock, are locked to different alignment markers, and that the Skew is within the boundaries of what the PCS can deskew. The synchronization process, along with the alignment marker lock process, are restarted if three consecutive FEC codewords from the same codeword (A or B) are uncorrectable.

The Transmit state diagram shown in Figure 119–14 controls the encoding of 66-bit transmitted blocks. It makes exactly one transition for each 66-bit transmit block processed. Though the Transmit state diagram sends Local Fault ordered sets when reset is asserted, the scrambler is not guaranteed to be operational during reset. Thus, the Local Fault ordered sets may not appear on the PMA service interface.

The Receive state diagram shown in Figure 119–15 controls the decoding of received blocks. It makes exactly one transition for each receive 66-bit block processed.

The PCS shall perform the functions of alignment marker lock, PCS synchronization, Transmit, and Receive as specified in the respective state diagrams.

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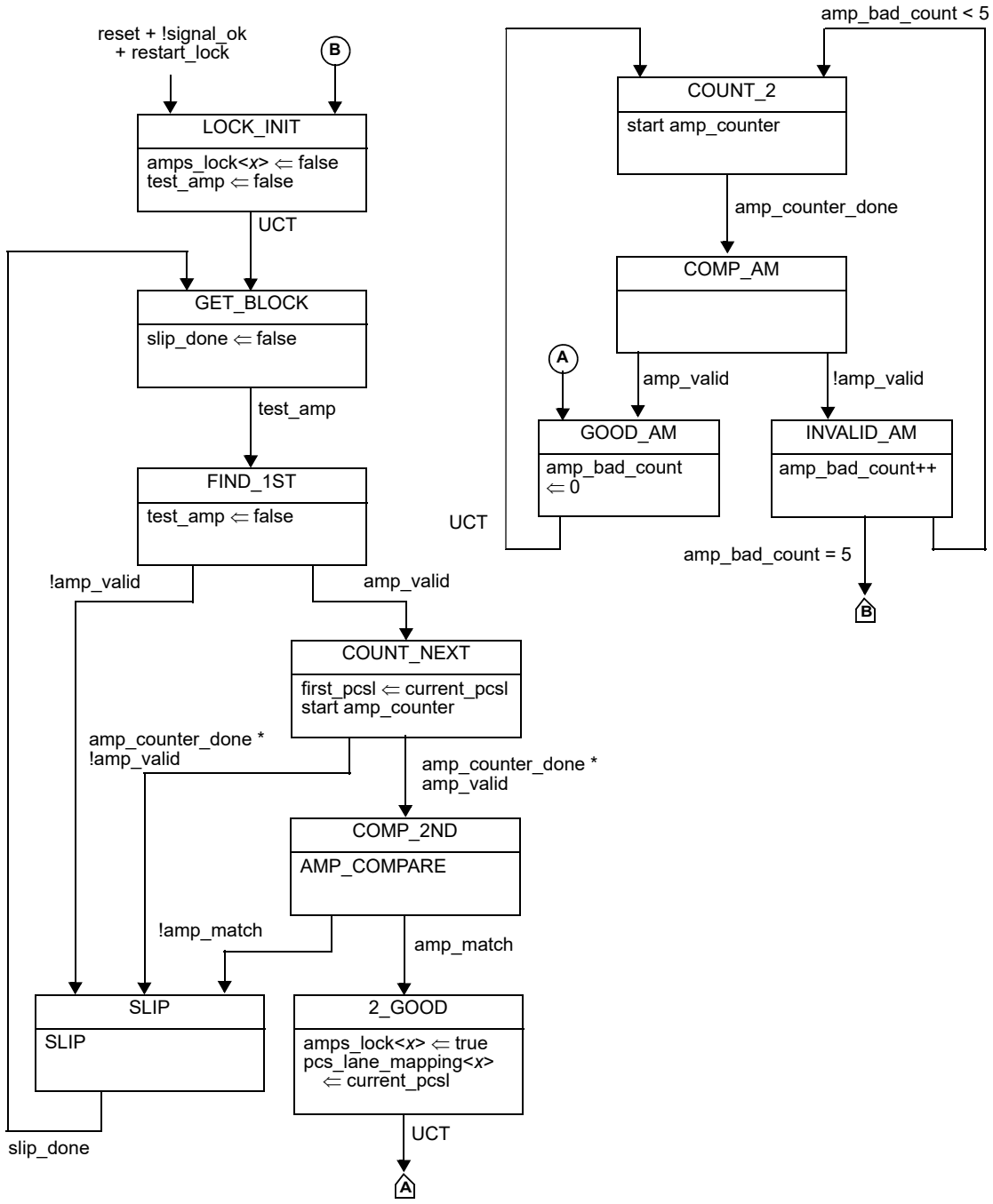

Figure 119–12—Alignment marker lock state diagram

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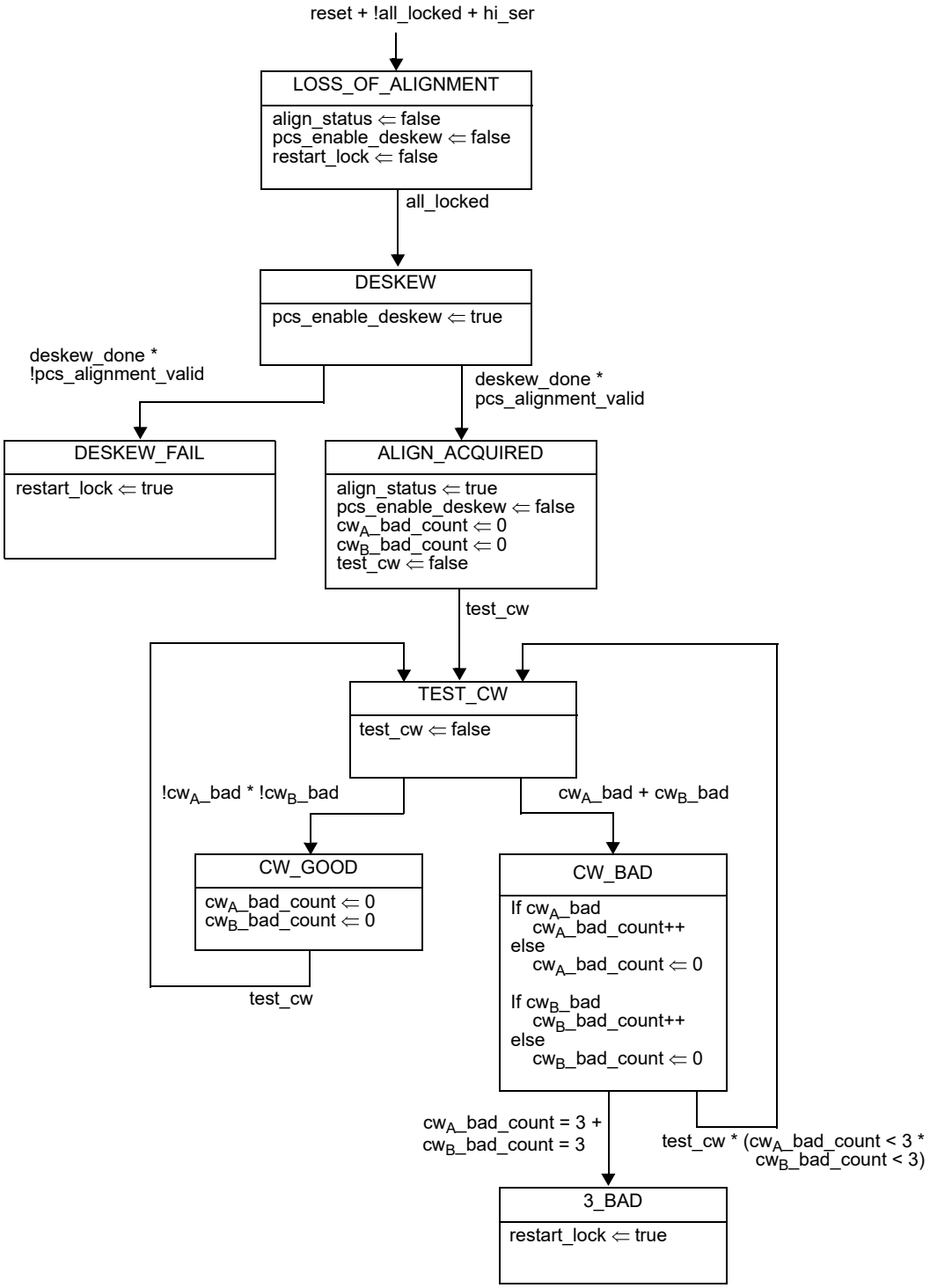

Figure 119–13—PCS synchronization state diagram

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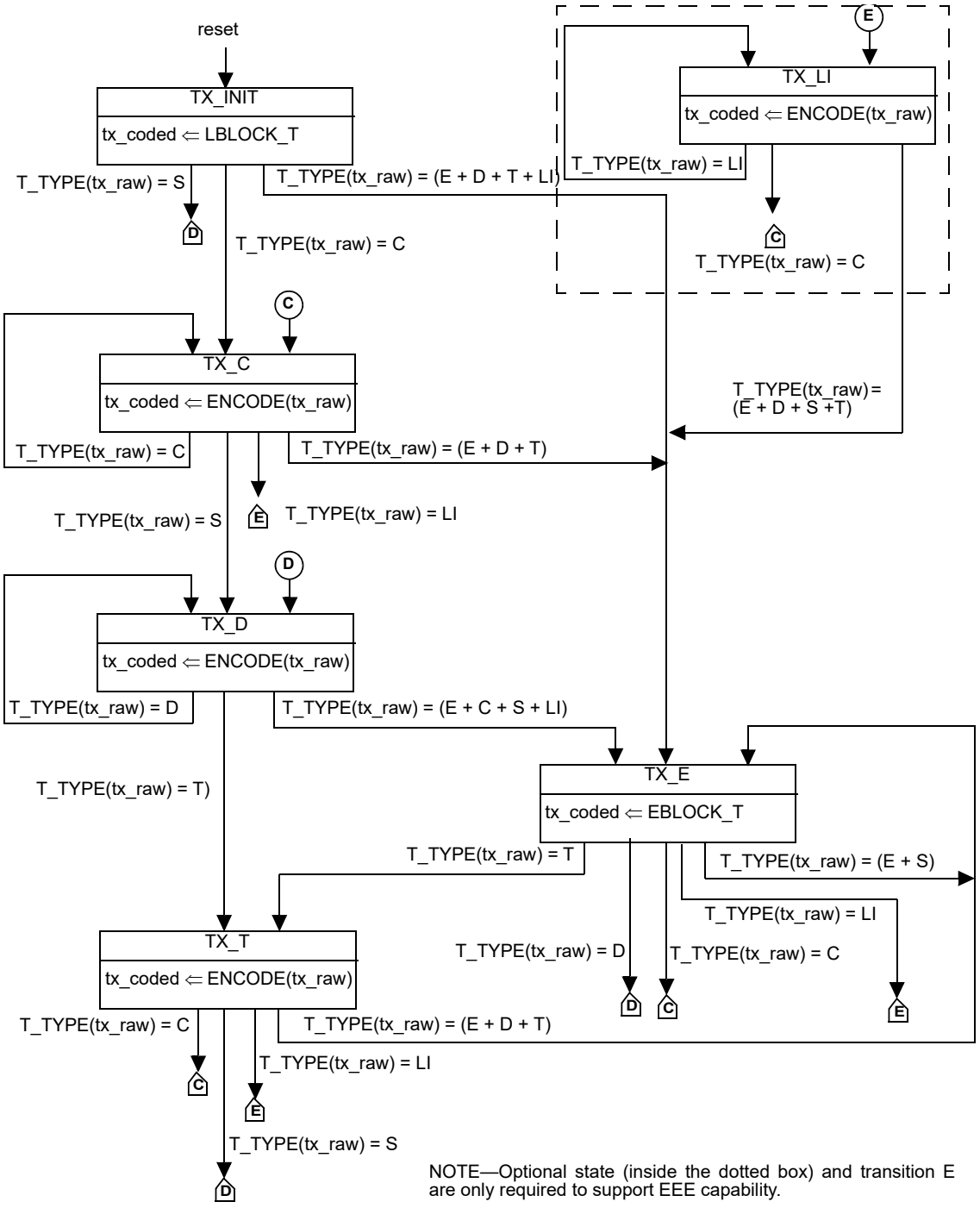

Figure 119–14—Transmit state diagram

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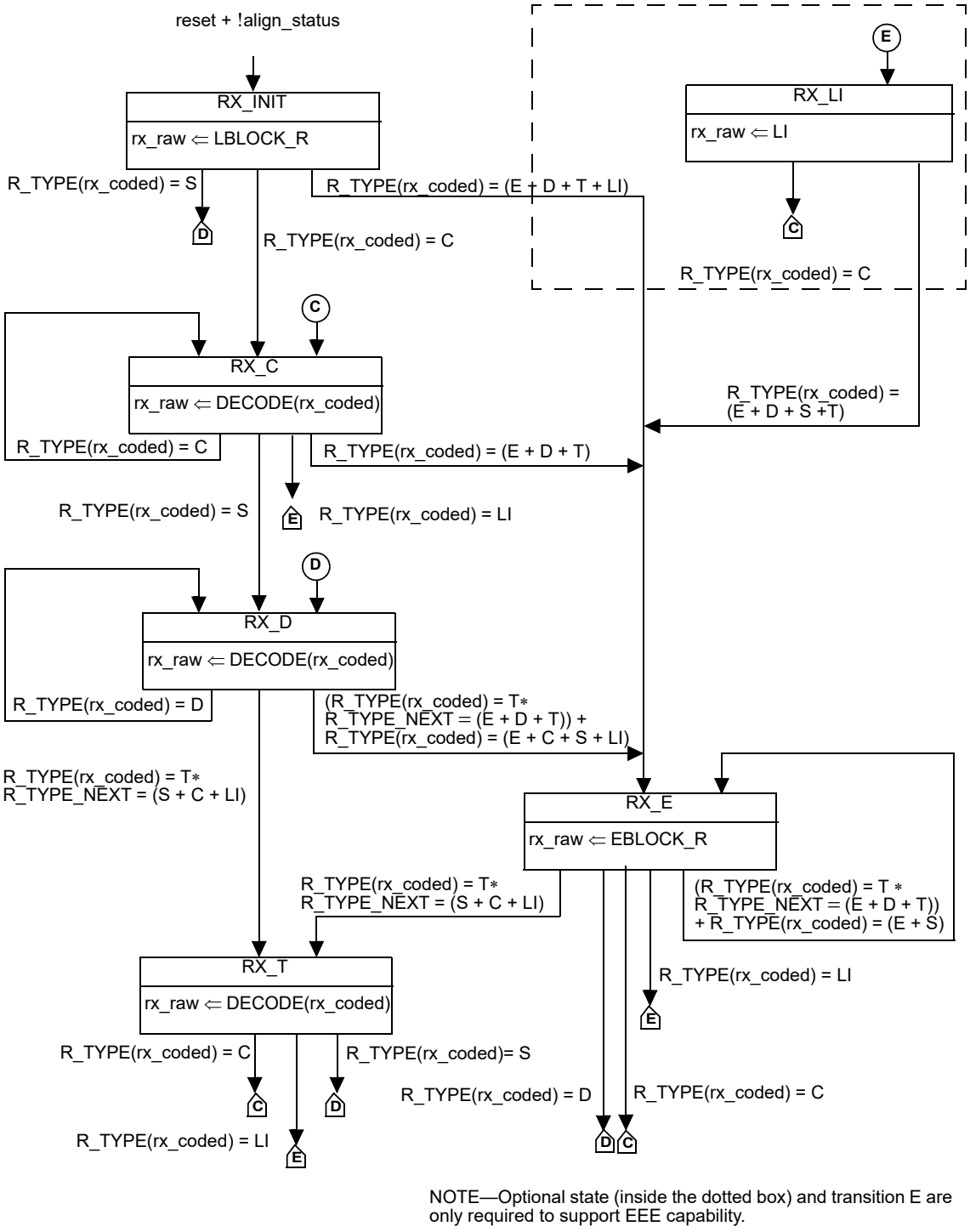

Figure 119–15—Receive state diagram

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119.3 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access is provided.

119.3.1 PCS MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PCS. If MDIO is implemented, it shall map MDIO control bits to PCS control variables, as shown in Table 119–4, and MDIO status bits to PCS status variables, as shown in Table 119–5.

Table 119–4—MDIO/PCS control variable mapping

MDIO control variable	PCS register name	Register/bit number	PCS control variable
Reset	PCS control 1 register	3.0.15	reset
Loopback	PCS control 1 register	3.0.14	Loopback
Transmit test-pattern enable	BASE-R PCS test-pattern control register	3.42.3	tx_test_mode
LPI_FW	EEE control and capability	3.20.0	LPI_FW
PCS FEC bypass indication enable	PCS FEC control register	3.800.1	FEC_bypass_indication_enable
PCS FEC degraded SER enable	PCS FEC control register	3.800.2	FEC_degraded_SER_enable
PCS FEC degraded SER activate threshold	PCS FEC degraded SER activate threshold register	3.806, 3.807	FEC_degraded_SER_activate_threshold
PCS FEC degraded SER deactivate threshold	PCS FEC degraded SER deactivate threshold register	3.808, 3.809	FEC_degraded_SER_deactivate_threshold
PCS FEC degraded SER interval	PCS FEC degraded SER interval	3.810, 3.811	FEC_degraded_SER_interval

Table 119–5—MDIO/PCS status variable mapping

MDIO status variable	PCS register name	Register/bit number	PCS status variable
BASE-R and MultiGBASE-T receive link status	BASE-R and MultiGBASE-T PCS status 1 register	3.32.12	PCS_status
Lane *x* aligned	Multi-lane BASE-R PCS alignment status 3 and 4 registers	3.52.7:0 3.53.7:0	am_lock<*x*>
PCS lane alignment status	Multi-lane BASE-R PCS alignment status 1 register	3.50.12	align_status
Lane *x* mapping	Lane *x* mapping register	3.400 through 3.415	pcs_lane_mapping<*x*>
PCS FEC bypass indication ability	PCS FEC status register	3.801.1	FEC_bypass_indication_ability

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Table 119–5—MDIO/PCS status variable mapping *(continued)*

MDIO status variable	PCS register name	Register/bit number	PCS status variable
PCS FEC corrected codewords	PCS FEC corrected codewords counter register	3.802, 3.803	FEC_corrected_cw_counter
PCS FEC uncorrected codewords	PCS FEC uncorrected codewords counter register	3.804, 3.805	FEC_uncorrected_cw_counter
PCS FEC symbol errors, PCS lanes 0 to *x*	PCS FEC symbol error counter register, lanes 0 to *x*	3.600 to 3.631	FEC_symbol_error_counter_*i*
Tx LPI indication	PCS status 1	3.1.9	Tx LPI indication
Tx LPI received	PCS status 1	3.1.11	Tx LPI received
Rx LPI indication	PCS status 1	3.1.8	Rx LPI indication
Rx LPI received	PCS status 1	3.1.10	Rx LPI received
EEE wake error counter	EEE wake error counter	3.22	Wake_error_counter
PCS FEC degraded SER ability	PCS FEC status register	3.801.3	FEC_degraded_SER_ability
PCS FEC degraded SER	PCS FEC status register	3.801.4	FEC_degraded_SER
Local degraded SER received	PCS FEC status register	3.801.6	rx_local_degraded
Remote degraded SER received	PCS FEC status register	3.801.5	rx_rm_degraded
PCS FEC high SER	PCS FEC status register	3.801.2	hi_ser

119.3.2 FEC_corrected_cw_counter

A corrected FEC codeword is a codeword that contains errors and was corrected. FEC_corrected_cw_counter is a 32-bit counter that counts once for each corrected FEC codeword processed when align_status is true. This variable is mapped to the registers defined in 45.2.3.62 (3.802, 3.803).

119.3.3 FEC_uncorrected_cw_counter

An uncorrected FEC codeword is a codeword that contains errors that were not corrected. FEC_uncorrected_cw_counter is a 32-bit counter that counts once for each uncorrected FEC codeword processed when align_status is true. This variable is mapped to the registers defined in 45.2.3.63 (3.804, 3.805).

119.3.4 FEC_symbol_error_counter_*i*

FEC_symbol_error_counter_*i* (where *i*=0 to 7 for the 200GBASE-R PCS and *i*=0 to 15 for the 400GBASE-R PCS) are 32-bit counters that count once for each 10-bit symbol corrected on PCS lane *i* when align_status is true. These variables are mapped to the registers defined in 45.2.3.58 and 45.2.3.59 (3.600 to 3.631).

119.4 Loopback

When the PCS is in loopback, the PCS shall accept data on the transmit path from the 200GMII/400GMII and return it on the receive path to the 200GMII/400GMII. In addition, the PCS shall transmit what it receives from the 200GMII/400GMII to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer. If a Clause 45 MDIO is implemented, then the PCS is placed in the loopback when the loopback bit from the PCS control 1 register (bit 3.0.14) is set to a one.

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119.5 Delay constraints

The maximum delay contributed by the 200GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 160 256 BT (313 pause_quanta or 801.28 ns). The maximum delay contributed by the 400GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 320 000 BT (625 pause_quanta or 800 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 116.4 and its references.

119.6 Auto-Negotiation

The following requirements apply to a PCS used with a 200GBASE-CR4 or 200GBASE-KR4 PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the AN_LINK.indication(link_status) primitive (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

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119.7 Protocol implementation conformance statement (PICS) proforma for Clause 119, Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R[206]

119.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 119, Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

119.7.2 Identification

119.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

119.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 119, Physical Coding Sublayer (PCS) 64B/66B, type 200GBASE-R and 400GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[206] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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119.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
MII	200GMII or 400GMII logical interface	117, 119.1.4.1	Logical interface is supported	O	Yes [ ] No [ ]
*PCS200	PCS for 200GBASE-R	119.1.1		O.1	Yes [ ] No [ ]
*PCS400	PCS for 400GBASE-R	119.1.1		O.1	Yes [ ] No [ ]
*MD	MDIO	45, 119.3	Registers and interface supported	O	Yes [ ] No [ ]
*BI	Bypass indication	119.2.5.3	Capability is supported	O	Yes [ ] No [ ]
DC	Delay constraints	119.5	Conforms to delay constraints specified in 119.5	M	Yes [ ]
*EEE	EEE capability	119.2.3.3	Capability is supported	O	Yes [ ] No [ ]
JTM	Supports test-pattern mode	119.2.1		M	Yes [ ]
FDD	Support for optional FEC degraded detection	119.2.5.3	In the FEC decoder can optionally detect FEC SER degraded at a programmable threshold	O	Yes [ ] No [ ]

119.7.4 PICS proforma tables for Physical Coding Sublayer (PCS) 64B/66B, type 200GBASE-R and 400GBASE-R

119.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	64B/66B to 256B/257B transcoder	119.2.4.2	tx_xcoded<256:0> constructed per 119.2.4.2	M	Yes [ ]
TF2	Transmission bit ordering	119.2.4.8	First bit transmitted is bit 0	M	Yes [ ]
TF3	Pad value	119.2.4.4	PRBS9	M	Yes [ ]
TF4	Alignment marker insertion	119.2.4.4		M	Yes [ ]
TF5	Pre-FEC distribution	119.2.4.5	Distribute the data to two FEC codewords	M	Yes [ ]
TF6	Reed-Solomon encoder	119.2.4.6	RS(544,514)	M	Yes [ ]
TF7	Symbol distribution	119.2.4.7	Distribution is based on 10b symbols	M	Yes [ ]

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119.7.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	119.2.5.1	Maximum Skew of 180 ns between PCS lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	Lane reorder and de-interleave	119.2.5.2	Order the PCS lanes according to the PCS lane number and de-interleave the FEC codewords	M	Yes [ ]
RF3	Reed-Solomon decoder	119.2.5.3	Corrects any combination of up to *t*=15 symbol errors in a codeword	M	Yes [ ]
RF4	Reed-Solomon decoder	119.2.5.3	Capable of indicating when a codeword was not corrected.	M	Yes [ ]
RF5	Error monitoring while error indication is bypassed	119.2.5.3	When the number of symbol errors in a block of 8192 codewords exceeds 5560 assert hi_ser for 60 ms to 75 ms	BI:M	Yes [ ] N/A [ ]
RF6	256B/257B to 64B/66B transcoder	119.2.5.7	rx_coded_*j*<65:0>, *j*=0 to 3 constructed per 119.2.5.7	M	Yes [ ]

119.7.4.3 64B/66B coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder (and ENCODE function) implements the code as specified	119.2.3, 119.2.6.2.3		M	Yes [ ]
C2	Decoder (and DECODE function) implements the code as specified	119.2.3, 119.2.6.2.3		M	Yes [ ]
C3	Only valid block types are transmitted	119.2.3.2		M	Yes [ ]
C4	Invalid block types are treated as an error	119.2.3.2		M	Yes [ ]
C5	Only valid control characters are transmitted	119.2.3.3		M	Yes [ ]
C6	Invalid control characters are treated as an error	119.2.3.3		M	Yes [ ]
C7	If EEE has not been negotiated, LPI is not transmitted	119.2.3.3		EEE:M	Yes [ ] N/A [ ]
C8	If EEE has not been negotiated, LPI is treated as an error if received	119.2.3.3		EEE:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
C9	Idles do not interrupt data	119.2.3.5		M	Yes [ ]
C10	IDLE control code insertion and deletion	119.2.3.5	Insertion or Deletion in groups of 8 /I/s	M	Yes [ ]
C11	Sequence ordered set deletion	119.2.3.8	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ]

119.7.4.4 Scrambler and descrambler

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Scrambler	119.2.4.3	Performs as shown in Figure 49–8	M	Yes [ ]
S2	Descrambler	119.2.5.6	Performs as shown in Figure 49–10	M	Yes [ ]

119.7.4.5 Alignment markers

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	Alignment marker insertion	119.2.4.4	Alignment markers are inserted periodically as in 119.2.4.4	M	Yes [ ]
AM2	Alignment marker form	119.2.4.4	Alignment markers are formed as described in 119.2.4.4	M	Yes [ ]
AM3	Lane mapping	119.2.6.3	PCS lane number is captured	MD:M	Yes [ ] N/A [ ]
AM4	Alignment marker removal	119.2.5.5	Alignment markers are removed prior to descrambling as described in 119.2.5.5	M	Yes [ ]

119.7.4.6 Test-pattern modes

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Scrambled idle transmit test-pattern generator is implemented	119.2.4.9		M	Yes [ ]

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119.7.4.7 Bit order

Item	Feature	Subclause	Value/Comment	Status	Support
B1	Transmit bit order	119.2.4.8	Placement of bits into the PCS lanes as shown in Figure 119–10 or Figure 119–11	M	Yes [ ]

119.7.4.8 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Equivalent access to PCS management object is provided	119.3		!MD:O	Yes [ ] No [ ] N/A [ ]
M2	Mapping of MDIO control bits and MDIO status bits	119.3.1	Table 119–4 and Table 119–5	MD:M	Yes [ ] N/A [ ]

119.7.4.9 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Alignment marker lock	119.2.6	Implements 8 alignment marker lock processes as depicted in Figure 119–12	PCS200:M	Yes [ ] N/A [ ]
SM2	Alignment marker lock	119.2.6	Implements 16 alignment marker lock processes as depicted in Figure 119–12	PCS400:M	Yes [ ] N/A [ ]
SM3	The SLIP function evaluates all possible block positions	119.2.6.2.3		M	Yes [ ]
SM4	PCS synchronization state diagram	119.2.6	Meets the requirements of Figure 119–13	M	Yes [ ]
SM5	Transmit process	119.2.6	Meets the requirements of Figure 119–14	M	Yes [ ]
SM6	Receive process	119.2.6	Meets the requirements of Figure 119–15	M	Yes [ ]

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119.7.4.10 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports loopback	119.4		M	Yes [ ]
L2	When in loopback, transmits what it receives from the 200GMII/400GMII	119.4		M	Yes [ ]
L3	When in loopback, ignore all data presented by the PMA sublayer	119.4		M	Yes [ ]

119.7.4.11 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS delay constraint	119.5	No more than 160 256 BT for sum of transmit and receive path delays for 200GBASE-R	PCS200:M	Yes [ ] N/A [ ]
TIM2	PCS delay constraint	119.5	No more than 320 000 BT for sum of transmit and receive path delays for 400GBASE-R	PCS400:M	Yes [ ] N/A [ ]

119.7.4.12 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
*AN	Support for use with a 200GBASE-CR4 or 200GBASE-KR4 PMD	119.6	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN1	AN_LINK.indication primitive	119.6	Support of the AN_LINK.indication(link_status) primitive	AN:M	Yes [ ] N/A [ ]
AN2	link_status parameter	119.6	Takes the value OK or FAIL, as described in 119.6	AN:M	Yes [ ] N/A [ ]
AN3	Generation of AN_LINK.indication primitive	119.6	Generated when the value of link_status changes	AN:M	Yes [ ] N/A [ ]

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120. Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R

120.1 Overview

120.1.1 Scope

This clause specifies the Physical Medium Attachment sublayer (PMA) for the families of 200 Gb/s and 400 Gb/s Physical Layer implementations, known as 200GBASE-R and 400GBASE-R. The PMA allows the PCS (specified in Clause 119) to connect in a media-independent way with a range of physical media, or for the DTE XS to connect to the PHY XS (specified in Clause 118). The 200GBASE-R PMA(s) can support any of the 200 Gb/s PMDs in Table 116–1, and the 400GBASE-R PMA(s) can support any of the 400 Gb/s PMDs in Table 116–2. The terms 200GBASE-R and 400GBASE-R are used when referring generally to Physical Layers using the PMA defined in this clause.

200GBASE-R and 400GBASE-R can be extended to support any full duplex medium requiring only that the PMD be compliant with the appropriate PMA interface.

The interfaces for the inputs of the 200GBASE-R and 400GBASE-R PMAs are defined in an abstract manner and do not imply any particular implementation. For 200GBASE-R PMAs, electrical interfaces connecting PMA sublayers, known as 200GAUI-n, are defined in Annex 120B, Annex 120C, Annex 120D, and Annex 120E. For 400GBASE-R PMAs, electrical interfaces connecting PMA sublayers, known as 400GAUI-n, are defined in Annex 120B, Annex 120C, Annex 120D, and Annex 120E.

120.1.2 Position of the PMA in the 200GBASE-R and 400GBASE-R sublayers

Figure 120–1 shows the relationship of the PMA sublayer (shown shaded) with other sublayers to the ISO Open System Interconnection (OSI) reference model.

120.1.3 Summary of functions

The following is a summary of the principal functions implemented (when required) by the PMA in both the transmit and receive directions:

a) Adapt the PCSL formatted signal to the appropriate number of abstract or physical lanes.
b) Provide per input-lane clock and data recovery.
c) Provide bit-level multiplexing.
d) Provide clock generation.
e) Provide signal drivers.
f) Optionally provide local loopback to/from the PMA service interface.
g) Optionally provide remote loopback to/from the PMD service interface.
h) Optionally provide test-pattern generation and detection.
i) Tolerate Skew Variation.
j) Perform PAM4 encoding and decoding for 200GBASE-R PMAs where the number of physical lanes is 4, and for 400GBASE-R PMAs where the number of physical lanes is 4 or 8.

In addition, the PMA provides receive link status information in the receive direction.

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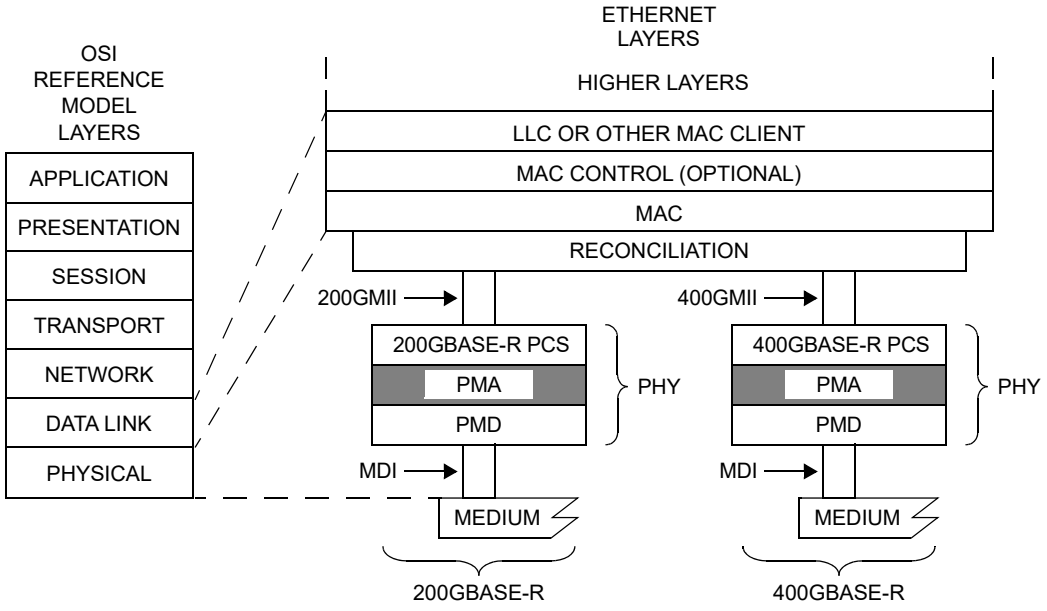

200GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120–1—200GBASE-R and 400GBASE-R PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

120.1.4 PMA sublayer positioning

An implementation may use one or more PMA sublayers to adapt the number and rate of the PCS lanes to the number and rate of the PMD lanes. The number of PMA sublayers required depends on the partitioning of functionality for a particular implementation. An example is illustrated in Figure 120–2. Additional examples are illustrated in Annex 120A. Each PMA maps the PCSLs from p PMA input lanes to q PMA output lanes in the Tx direction, and from q PMA input lanes to p PMA output lanes in the Rx direction.

Management Data Input/Output (MDIO) Manageable Device (MMD) addresses 1, 8, 9, and 10 are available for addressing multiple instances of PMA sublayers (see Table 45–1 for MMD device addresses). If the PMA sublayer that is closest to the PMD is packaged with the PMD, it shares MMD 1 with the PMD. More addressable instances of PMA sublayers, each one separated from lower addressable instances by chip-to-chip interfaces, may be implemented and addressed allocating MMD addresses to PMAs in increasing numerical order going from the PMD toward the MAC. The example shown in Figure 120–2 could be implemented with three addressable instances: MMD 1 addressing the lowest PMA sublayer (co-packaged with the PMD), MMD 8 addressing the PMA sublayer above the 200GAUI-4 below the 200GAUI-8 or above the 400GAUI-8 below the 400GAUI-16, and MMD 9 addressing the PMA sublayer below the PCS.

The number of input lanes and the number of output lanes for a PMA are always divisors of the number of PCSLs. For PMA sublayers supporting 200GBASE-R PMDs, the number of PCSLs is 8. For PMA sublayers supporting 400GBASE-R PMDs, the number of PCSLs is 16.

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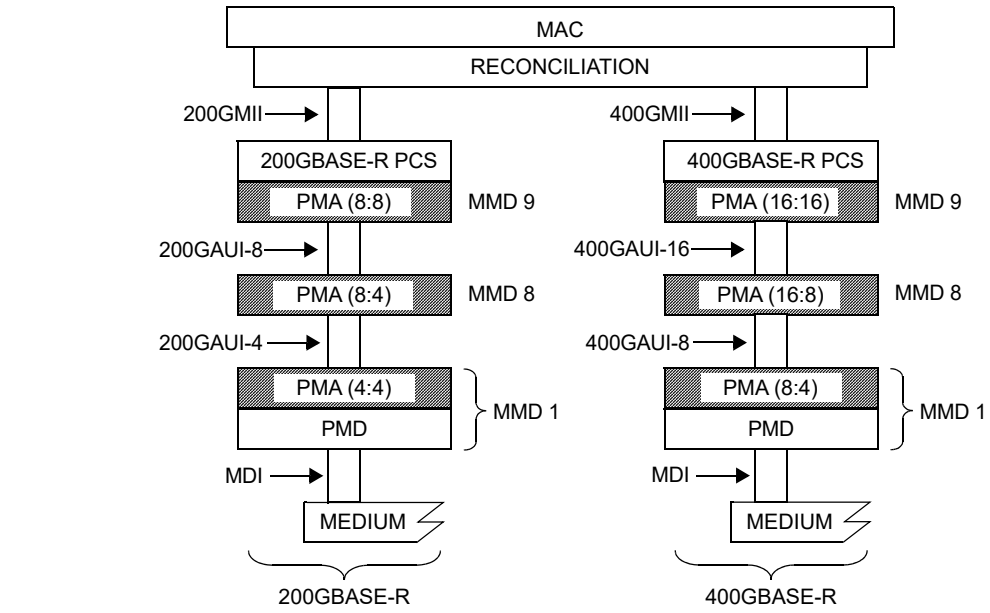

200GAUI = 200 Gb/s ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GAUI = 400 Gb/s ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120–2—Example 200GBASE-R and 400GBASE-R PMA layering

The following guidelines apply to the partitioning of PMAs:

a) The inter-sublayer service interface, defined in 116.3.1, is used for the PMA service interfaces supporting a flexible architecture with multiple PMA sublayers.
   1) An instance of this interface can only connect service interfaces with the same number of lanes, where the lanes operate at the same rate.

b) 200GAUI-n is a physical instantiation of the connection between two adjacent 200GBASE-R PMA sublayers with the exception of the inst:IS_SIGNAL.indication which is carried outside of this physically instantiated interface. 400GAUI-n is a physical instantiation of the connection between two adjacent 400GBASE-R PMA sublayers with the exception of the inst:IS_SIGNAL.indication which is carried outside of this physically instantiated interface.
   1) As physical instantiations, these define electrical and timing specification as well as requiring a receive re-timing function.
   2) 200GAUI-8 is a 26.5625 GBd by 8 lane NRZ physical instantiation of the 200 Gb/s connection. 400GAUI-16 is a 26.5625 GBd by 16 lane NRZ physical instantiation of the 400 Gb/s connection.
   3) 200GAUI-4 is a 26.5625 GBd by 4 lane PAM4 physical instantiation of the 200 Gb/s connection. 400GAUI-8 is a 26.5625 GBd by 8 lane PAM4 physical instantiation of the 400 Gb/s connection.

c) The abstract inter-sublayer service interface can be physically instantiated as a 200GAUI-n or 400GAUI-n, using associated PMAs to map to the appropriate number of lanes.

d) Opportunities for optional test-pattern generation, optional test-pattern detection, optional local loopback and optional remote loopback are dependent upon the location of the PMA sublayer in the implementation. See Figure 120–5.

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e) A minimum of one PMA sublayer is required in a PHY.

f) A maximum of four PMA sublayers are addressable as MDIO MMDs.

120.2 PMA interfaces

All PMA variants for 200GBASE-R and 400GBASE-R are based on a generic specification of a bit mux function that applies to all input/output lane counts and each direction of transmission. Each direction of transmission may employ one or more such bit muxes to adapt from the appropriate number of input lanes to the appropriate number of output lanes as illustrated in Figure 120–3.

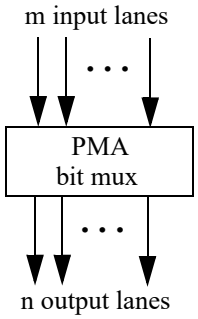

Figure 120–3—PMA bit mux used in both Tx and Rx directions

Conceptually, the PMA bit mux operates in one direction of transmission by demultiplexing PCSLs from m PMA input lanes and remultiplexing them into n PMA output lanes. The mapping of PCSLs from input to output lanes is not specified. See 120.5.2 and Figure 120–4 for details.

Figure 120–5 provides the functional block diagram of a PMA. The parameters of a PMA include the following:

— The numbers of input and output lanes in each direction.

— Whether the PMA is adjacent to a physically instantiated interface (200GAUI-n or 400GAUI-n above or below).

— Whether the PMA is adjacent to the PCS or DTE XS.

— Whether the PMA is adjacent to the PMD or PHY XS.

120.3 PMA service interface

The PMA service interface for 200GBASE-R and 400GBASE-R is an instance of the inter-sublayer service interface defined in 116.3.1. The PMA service interface primitives are summarized as follows:

PMA:IS_UNITDATA_*i*.request(tx_symbol)
PMA:IS_UNITDATA_*i*.indication(rx_symbol)
PMA:IS_SIGNAL.indication(SIGNAL_OK)

For a PMA service interface with p lanes, the primitives are defined for $i = 0$ to $p - 1$.

If the PMA client is the PCS or DTE XS, the PMA continuously sends eight (for 200GBASE-R) or sixteen (for 400GBASE-R) parallel bit streams to the PCS, each at the nominal signaling rate of the PCSL.

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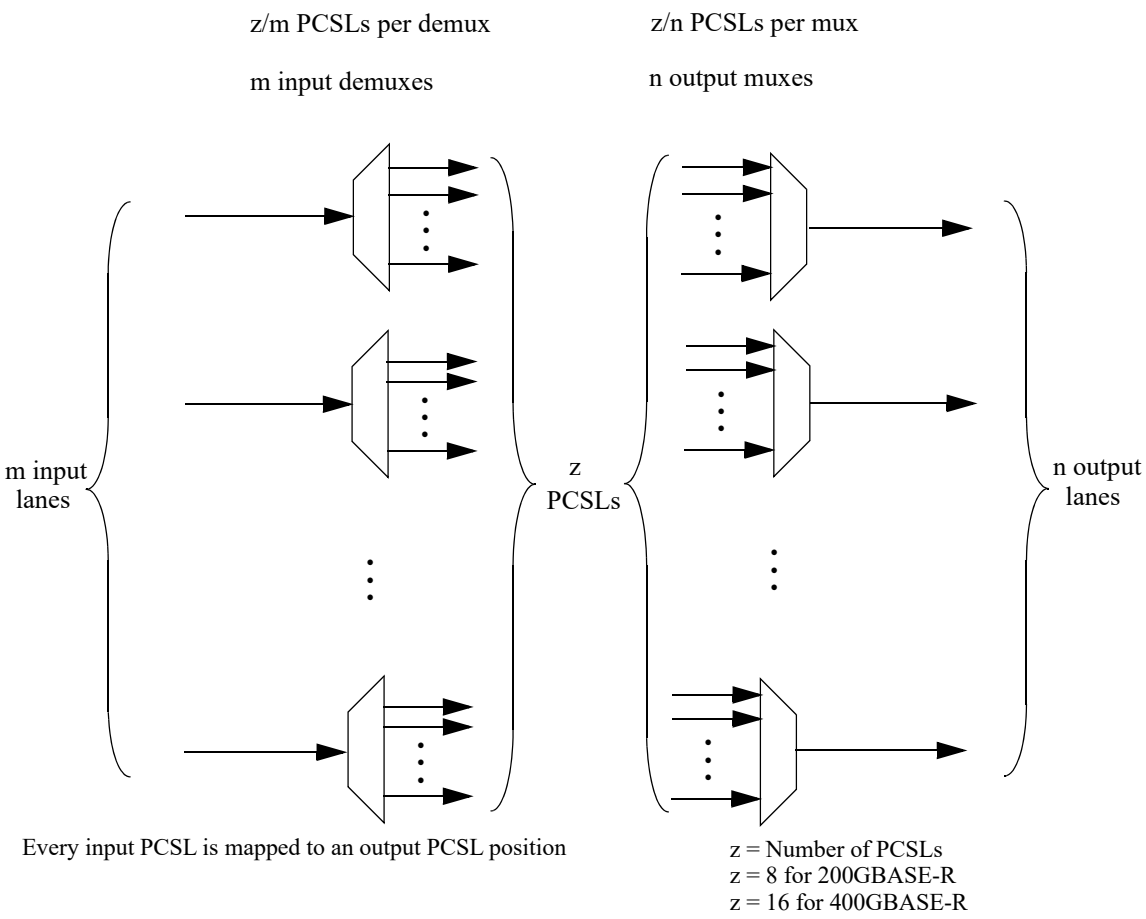

Figure 120–4—PMA bit mux operation used in both Tx and Rx directions

If a PMA client is another PMA, a 200GBASE-R PMA with p=8 or a 400GBASE-R PMA with p=16 physical input lanes receives bits from one PCSL on each of its input lanes. A 200GBASE-R PMA with p=4 physical input lanes receives PAM4 symbols on each of its input lanes at the PCSL rate, each symbol formed from two bits. A 400GBASE-R PMA with p=4 or p=8 physical input lanes receives PAM4 symbols on each of its input lanes at 8/p times the PCSL rate, each symbol formed from two bits. The bit stream represented by the input symbols carries z/p bit-multiplexed PCSLs on each physical input lane, where z=8 for 200GBASE-R and z=16 for 400GBASE-R. Skew may exist between different PCSLs received on the same physical input lane even though all PCSLs originate from the same synchronous source, so there is independence of arrival of bits from each PCSL on each physical input lane.

In the Tx direction, if the symbol from a PMA:IS_UNITDATA_*i*.request primitive is received over a physically instantiated interface (200GAUI-n or 400GAUI-n), clock and data are recovered on the lane receiving the symbol. If necessary, PAM4 symbols are converted to pairs of bits. Bits are routed through the PMA to an output lane through a process that may demultiplex PCSLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs to output lanes. If necessary, pairs of bits on output lanes are converted to PAM4 symbols. The symbols are sent on an output lane to the sublayer below using the *inst*:IS_UNITDATA_*k*.request (*k* not necessarily equal to *i*) primitive (see 120.4).

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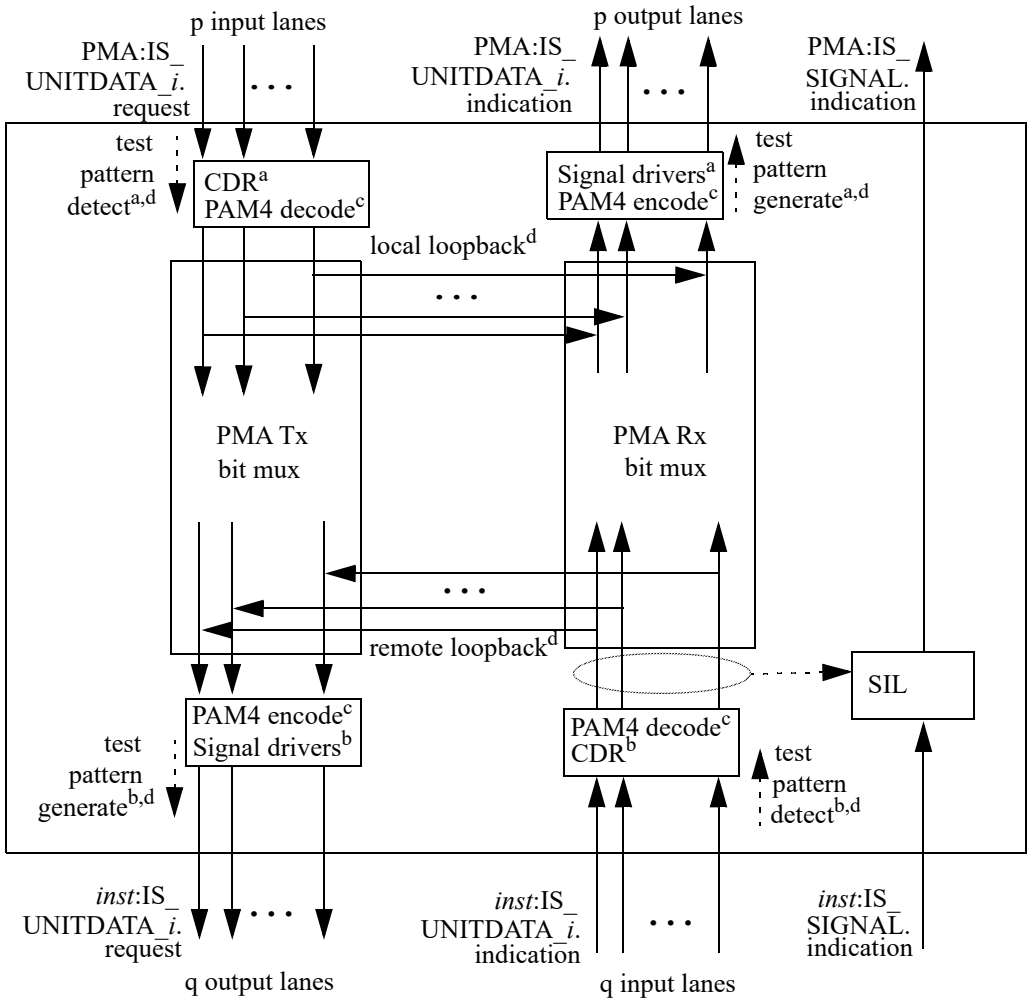

inst PMD, PMA, or PHY_XS, depending on which sublayer is below this PMA
SIL Signal Indication Logic

[a] If physically instantiated interface (200GAUI-n or 400GAUI-n) immediately above this PMA.
[b] If physically instantiated interface (200GAUI-n or 400GAUI-n) immediately below this PMA, or if this is the closest PMA to the PMD.
[c] If number of input or output lanes is 4 for a 200GBASE-R PMA, or 4 or 8 for a 400GBASE-R PMA.
[d] Optional.

Figure 120–5—PMA Functional Block Diagram

The PMA passes symbols from the input lanes to the output lanes in the Rx direction when data is being received from every input lane from the sublayer below the PMA that has a PCSL that is routed to a particular output lane at the PMA service interface, and (if necessary), buffers are filled to allow tolerating the Skew Variation that may appear between the input lanes. PCSLs are demultiplexed from the input lanes, remultiplexed to the output lanes, and symbols are transferred over each output lane to the PMA client via the PMA:IS_UNITDATA_*i*.indication primitive. If necessary, PAM4 symbols are converted to pairs of bits on the input lanes and/or pairs of bits are converted to PAM4 symbols on the output lanes.

The PMA:IS_SIGNAL.indication primitive is generated through a set of Signal Indication Logic (SIL) that reports signal health based on receipt of the *inst*:IS_SIGNAL.indication from the sublayer below, data being received on all of the input lanes from the sublayer below, buffers filled (if necessary) to accommodate Skew Variation, and symbols being sent to the PMA client on all of the output lanes. When these conditions

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are met, the SIGNAL_OK parameter sent to the PMA client via the PMA:IS_SIGNAL.indication primitive has the value OK. Otherwise, the SIGNAL_OK primitive has the value FAIL. In the case where the sublayer below the PMA is a PHY XS the PMA does not receive a PHY_XS:IS_SIGNAL.indication as an input to the SIL.

120.4 Service interface below PMA

Since the architecture supports multiple PMA sublayers for various PMD lane counts and device partitioning, there are several different sublayers that may appear below a PMA, including the PMD, an extender sublayer, or another PMA. The variable *inst* represents whichever sublayer appears below the PMA (e.g., another PMA or PMD).

The sublayer below the PMA utilizes the inter-sublayer service interface defined in 116.3. The service interface primitives provided to the PMA are summarized as follows:

inst:IS_UNITDATA_*i*.request(tx_symbol)
inst:IS_UNITDATA_*i*.indication(rx_symbol)
inst:IS_SIGNAL.indication(SIGNAL_OK)

The number of lanes q for the service interface matches the number of lanes expected by the PMA. The *inst*:IS_UNITDATA_*i* primitives are defined for each lane $i = 0$ to $q - 1$ of the service interface below the PMA. Note that electrical and timing specifications of the service interface are defined if the interface is physically instantiated (e.g., 200GAUI-n or 400GAUI-n), otherwise the service interface is specified only abstractly. The interface between the PMA and the sublayer below consists of q lanes for data transfer and a status indicating a good signal from the sublayer below the PMA (see Figure 120–5).

The PMA transfers symbols from the input lanes to the output lanes in the Tx direction when data is being received via the PMA:IS_UNITDATA_*i*.request primitive from every input lane from the PMA client at the PMA service interface (see 120.3) that has a PCSL that is routed to this output lane, and (if necessary), buffers are filled to provide the ability to tolerate the Skew Variation that may appear between the input lanes from the PMA client. PCSLs are demultiplexed from the input lanes, remultiplexed to the output lanes, and symbols are transferred over each output lane to the sublayer below the PMA.

In the Rx direction, if the symbol is received over a physically instantiated interface (200GAUI-n, 400GAUI-n, or physically instantiated PMD service interface), clock and data are recovered on the lane receiving the symbol. If necessary, PAM4 symbols received on the input lanes are converted to pairs of bits. The bits are routed through the PMA to an output lane toward the PMA client through a process that may demultiplex PCSLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs to output lanes. If necessary, pairs of bits are converted to PAM4 symbols on the output lanes. Each symbol is sent on an output lane to the PMA client using the PMA:IS_UNITDATA_*k*.indication (*k* not necessarily equal to *i*) primitive at the PMA service interface.

In the case where the sublayer below the PMA is a PHY XS, there is an additional primitive:

PHY_XS:IS_SIGNAL.request(SIGNAL_OK)

The PHY_XS:IS_SIGNAL.request primitive is generated through a set of SIL that reports signal health based on data being received on all of the input lanes from the sublayer above, buffers filled (if necessary) to accommodate Skew Variation, and symbols being sent to the PHY XS on all of the output lanes. When these conditions are met, the SIGNAL_OK parameter sent to the PHY XS via the PHY_XS:IS_SIGNAL.request primitive has the value OK. Otherwise, the SIGNAL_OK primitive has the value FAIL.

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120.5 Functions within the PMA

The purpose of the PMA is to adapt the PCSL formatted signal to an appropriate number of abstract or physical lanes, to recover clock from the received signal (if appropriate), and optionally to provide test signals and loopback. Each input (Tx direction) or output (Rx direction) lane between the PMA and the PMA client carries one or more PCSLs that are bit-multiplexed. All input and output lanes between the PMA and the PMA client carry the same number of PCSLs and operate at the same nominal signaling rate. Likewise, each input (Rx direction) or output (Tx direction) lane between the PMA and the sublayer below the PMA carries one or more PCSLs that are bit-multiplexed. All input and output lanes between the PMA and the sublayer below the PMA carry the same number of PCSLs and operate at the same nominal signaling rate. As described in 120.1.4, the number of input lanes and the number of output lanes for a given PMA are divisors of 8 for 200GBASE-R, or 16 for 400GBASE-R, which are the number of PCSLs for the respective PHYs. The symbols received from input lanes or sent on output lanes are bits for 200GBASE-R interfaces where the number of lanes is 8, or 400GBASE-R interfaces where the number of lanes is 16. The symbols received from input lanes or sent on output lanes are PAM4 symbols for 200GBASE-R interfaces where the number of lanes is 4, or 400GBASE-R interfaces where the number of lanes is 8 or 4.

120.5.1 Per input-lane clock and data recovery

If the interface between the PMA client and the PMA is physically instantiated as 200GAUI-n or 400GAUI-n, the PMA shall meet the electrical and timing specifications in Annex 120B, Annex 120C, Annex 120D, or Annex 120E as appropriate. If the interface between the sublayer below the PMA and the PMA is physically instantiated as 200GAUI-n or 400GAUI-n, the PMA shall meet the electrical and timing specifications at the service interface below the PMA as specified in Annex 120B, Annex 120C, Annex 120D, or Annex 120E as appropriate.

Test patterns that are intended for transmitter testing, such as square wave, may not be correctly recovered by an adjacent PMA.

120.5.2 Bit-level multiplexing

The PMA provides bit-level multiplexing in both the Tx and Rx directions. In the Tx direction, the function is performed among the bits received from the PMA client via the PMA:IS_UNITDATA_*i*.request primitives (for PMA client lanes $i = 0$ to $p - 1$) with the result sent to the service interface below the PMA using the *inst*:IS_UNITDATA_*i*.request primitives (for service interface lanes $i = 0$ to $q - 1$), referencing the functional block diagram shown in Figure 120–5. The bit multiplexing behavior is illustrated in Figure 120–4.

The aggregate signal carried by the group of input lanes or the group of output lanes is arranged as a set of PCSLs. The number of PCSLs z is 8 for 200GBASE-R interfaces and 16 for 400GBASE-R interfaces. The nominal bit rate R of each PCSL is 26.5625 Gb/s.

For a PMA with m input lanes (Tx or Rx direction), each input lane carries, bit multiplexed, z/m PCSLs. Each input lane has a nominal bit rate of 26.5625 × z/m Gb/s. Note that the signaling (Baud) rate is equal to the bit rate when the number of physical lanes is 8 for 200GBASE-R or 16 for 400GBASE-R (bits are sent or received on the lanes). The Baud rate is equal to half of the bit rate when the number of physical lanes is 4 for 200GBASE-R or the number of physical lanes is 8 or 4 for 400GBASE-R (PAM4 symbols are sent or received on the lanes). If necessary, PAM4 symbols are converted to pairs of bits on the input lanes and/or pairs of bits are converted to PAM4 symbols on the output lanes. If bit x received on an input lane belongs to a particular PCSL, the next bit of that same PCSL is received on the same input lane at bit position $x+(z/m)$. The z/m PCSLs may arrive in any sequence on a given input lane.

For a PMA with n output lanes (Tx or Rx direction), each output lane carries, bit multiplexed, z/n PCSLs. Each output lane has a nominal signaling rate of 26.5625 × z/n Gb/s. Each PCSL is mapped from a position

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in the sequence on one of the m input lanes to a position in the sequence on one of the n output lanes. If bit *x* sent on an output lane belongs to a particular PCSL, the next bit of that same PCSL is sent on the same output lane at bit position *x* + (z/n). The PMA shall maintain the chosen sequence of PCSLs on all output lanes while it is receiving a valid stream of bits on all input lanes.

Each PCSL received in any temporal position on an input lane is transferred into a temporal position on an output lane. As the PCS (see Clause 119) has fully flexible receive logic, an implementation is free to perform the mapping of PCSLs from input lanes to output lanes without constraint. Figure 120–6 illustrates one possible bit ordering for a 400GBASE-R 8:4 PMA bit mux. Other bit orderings are also valid.

Note that since the number of input lanes and output lanes for a 200GBASE-R or 400GBASE-R PMA is always a power of two, many PMAs converting between different numbers of lanes normally simply multiplex two or four input lanes to one output lane, or demultiplex two or four output lanes from one input lane. However, any PMA implementation which produces an allowable order of bits from all PCSLs on the output lanes is valid.

NOTE—PMA output lanes composed of some specific combinations of four PCSLs with specific skew offsets (e.g., 400GBASE-R PCSLs 0, 2, 4, and 10 with delays 0, 1, 0, and 2 bits, respectively) may have reduced transition density.

120.5.3 Skew and Skew Variation

The Skew (relative delay) between the PCSLs is kept within limits so that the information on the lanes can be reassembled by the PCS.

Any PMA that combines PCSLs from different input lanes onto the same output lane is required to tolerate Skew Variation between the input lanes without changing the PCSL positions on the output. Skew and Skew Variation are defined in 116.5. The limits for Skew and Skew Variation at physically instantiated interfaces are specified at Skew points SP1 and SP2 in the transmit direction and SP5 and SP6 in the receive direction as defined in 116.5 and illustrated in Figure 116–4 and Figure 116–5.

120.5.3.1 Skew generation toward SP1

In an implementation with one or more physically instantiated 200GAUI-n or 400GAUI-n interfaces, the PMA that sends data in the transmit direction toward the 200GAUI-n or 400GAUI-n that is closest to the PMD (SP1 in Figure 116–4 and Figure 116–5) shall produce no more than 29 ns of Skew between PCSLs toward the 200GAUI-n or 400GAUI-n, and no more than 200 ps of Skew Variation.

120.5.3.2 Skew tolerance at SP1

In an implementation with one or more physically instantiated 200GAUI-n or 400GAUI-n interfaces, the PMA service interface that receives data in the transmit direction from the 200GAUI-n or 400GAUI-n (SP1 in Figure 116–4 and Figure 116–5) shall tolerate the maximum amount of Skew Variation allowed at SP1 (200 ps) between input lanes while maintaining the bit ordering and position of each PCSL on each PMA lane in the transmit direction (toward the PMD).

120.5.3.3 Skew generation toward SP2

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, the PMA adjacent to the PMD service interface shall generate no more than 43 ns of Skew, and no more than 400 ps of Skew Variation between output lanes toward the PMD service interface (SP2 in Figure 116–4 and Figure 116–5). If there is a physically instantiated 200GAUI-n or 400GAUI-n as well, then the Skew measured at SP1 is limited to no more than 29 ns of Skew and no more than 200 ps of Skew Variation.

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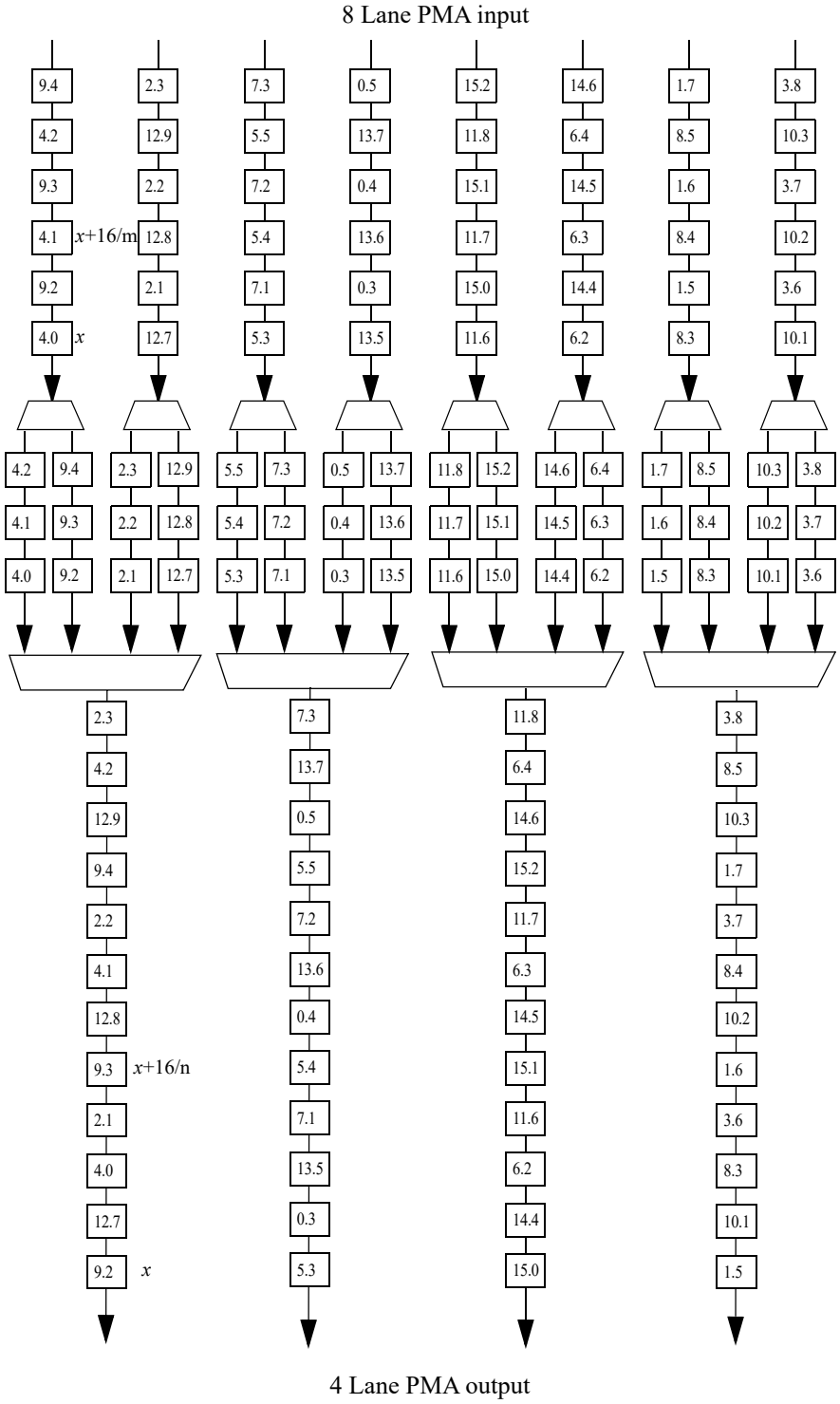

NOTE—i.k indicates bit k on PCSL i. Skew may exist between PCSLs.

Figure 120–6—Example 8:4 400GBASE-R PMA bit mux

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120.5.3.4 Skew tolerance at SP5

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, the PMA adjacent to the PMD service interface (SP5) shall tolerate the maximum amount of Skew Variation allowed at SP5 (3.6 ns) between output lanes from the PMD service interface while maintaining the bit ordering and position of each PCSL on each PMA lane in the receive direction (toward the MAC).

120.5.3.5 Skew generation at SP6

In an implementation with one or more physically instantiated 200GAUI-n or 400GAUI-n interfaces, at SP6 (the receive direction of the 200GAUI-n or 400GAUI-n closest to the PCS), the PMA or group of PMAs between the PMD and the 200GAUI-n or 400GAUI-n closest to the PCS shall deliver no more than 160 ns of Skew, and no more than 3.8 ns of Skew Variation between output lanes toward the 200GAUI-n or 400GAUI-n in the Rx direction.

If there is a physically instantiated PMD service interface that allows the Skew to be measured, the Skew measured at SP5 is limited to no more than 145 ns of Skew and no more than 3.6 ns of Skew Variation. If there is no physically instantiated PMD service interface, the Skew measured at SP4 is limited to no more than 134 ns of Skew, and no more than 3.4 ns of Skew Variation.

120.5.3.6 Skew tolerance at SP6

In an implementation with one or more physically instantiated 200GAUI-n or 400GAUI-n interfaces, the PMA between the 200GAUI-n or 400GAUI-n closest to the PCS and the PCS shall tolerate the maximum amount of Skew Variation allowed at SP6 (3.8 ns) between input lanes while maintaining the bit order and position of PCSLs on lanes sent in the receive direction towards the MAC.

120.5.4 Delay constraints

The maximum cumulative delay contributed by up to four PMA stages in a PHY (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 120–1. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 116.4 and its references.

Table 120–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
200GBASE-R PMA	18 432	36	92.16
400GBASE-R PMA	36 864	72	92.16

120.5.5 Clocking architecture

A PMA with m input lanes and n output lanes shall clock the output lanes such that the bit rate of the output lanes is m/n times the bit rate of the input lanes. For input or output lanes encoded as PAM4 (for 200GBASE-R, where the number of input or output lanes is 4, or for 400GBASE-R, where the number of input or output lanes is 4 or 8), the symbol rate is half of the bit rate. This applies in both the Tx and Rx directions of transmission. In the case where the interfaces between the PMA client and the PMA and/or the PMA and the sublayer below the PMA are physically instantiated, the PMA may derive its input clock(s)

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from the electrical interface on one or more of the input lanes, and generate the output clock(s) with an appropriate PLL multiplier/divider circuit.

NOTE—For a PMA where the signaling rate on each output lane is higher than the signaling rate on each input lane, any low frequency jitter on the input lanes may result in more jitter relative to the UI on the output lanes.

There is no requirement that the PMA clock all output lanes in unison. Examples of independent clocking of output lanes include the following:

— The case where the number of input and output lanes are equal (the PMA is provided for retiming and regeneration of the signal). This may be implemented without any rearrangement of PCSLs between input lanes and output lanes (although rearrangements are allowed), and such a PMA may be implemented by driving each output lane using the clock recovered from the corresponding input lane.
— Since the number of PCSLs is a power of 2, whenever the number of input and output lanes are unequal, each input lane could be mapped to multiple output lanes (in the case where the number of output lanes is greater), or multiple input lanes could be mapped to a single output lane.

120.5.6 Signal drivers

For cases where the interface between the PMA client and the PMA, or between the PMA and the sublayer below the PMA represent a physically instantiated interface, the PMA provides electrical signal drivers for that interface. The electrical and jitter/timing specifications for these interfaces appear in

— Annex 120B, which specifies the 200GAUI-8 and 400GAUI-16 interfaces for chip-to-chip applications.
— Annex 120C, which specifies the 200GAUI-8 and 400GAUI-16 interfaces for chip-to-module applications.
— Annex 120D, which specifies the 200GAUI-4 and 400GAUI-8 interfaces for chip-to-chip applications.
— Annex 120E, which specifies the 200GAUI-4 and 400GAUI-8 interfaces for chip-to-module applications.

For 200GAUI-8 or 400GAUI-16, the modulation format is NRZ. For 200GAUI-4 or 400GAUI-8, the modulation format is PAM4.

120.5.7 PAM4 Encoding

120.5.7.1 Gray mapping for PAM4 encoded lanes

For output lanes encoded as PAM4 (for 200GBASE-R, where the number of output lanes is 4, or for 400GBASE-R, where the number of output lanes is 4 or 8), the PMA transmit process shall map consecutive pairs of bits {A, B}, where A is the bit arriving first, to a Gray-coded symbol as follows:

{0, 0} maps to 0,
{0, 1} maps to 1,
{1, 1} maps to 2, and
{1, 0} maps to 3.

For input lanes encoded as PAM4 (for 200GBASE-R, where the number of input lanes 4, or for 400GBASE-R, where the number of input lanes is 4 or 8), the PMA receive process shall map Gray-coded PAM4 symbols to pairs of bits {A, B} where A is considered to be the first bit as follows:

0 maps to {0, 0},
1 maps to {0, 1},

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2 maps to {1, 1}, and
3 maps to {1, 0}.

120.5.7.2 Precoding for PAM4 encoded lanes

The precoding specifications in this subclause apply to the input and output lanes of a PMA that are connected to the service interface of a 200GBASE-R PMD that includes the PMD control function defined in 136.8.11 (200GBASE-CR4 or 200GBASE-KR4).

The PMA shall provide 1/(1+D) mod 4 precoding capability on each transmit lane and may optionally provide 1/(1+D) mod 4 decoding capability on each receive lane. Precoding is implemented as specified in 135.5.7.2.

The precoder is enabled independently on the Tx output (toward the PMD) and the Rx input (from the PMD) on each lane (0, 1, 2, and 3). Precoding is enabled and disabled using variables precoder_tx_out_enable_*i* and precoder_rx_in_enable_*i* (where *i* is 0, 1, 2, or 3).

If a Clause 45 MDIO is implemented, the variables precoder_tx_out_enable_*i* and precoder_rx_in_enable_*i* are accessible through register 1.600 and 1.601 (see 45.2.1.139 and 45.2.1.140).

If the PMA is connected to the service interface of a PMD that includes the PMD control function and training is enabled by the management variable mr_training_enable (see 136.7), then precoder_tx_out_enable_*i* and precoder_rx_in_enable_*i* shall be set as determined by the PMD control function in the LINK_READY state on lane *i* (see 136.8.11.7.5 and Figure 136–7). The method by which the PMD control function affects these variables is implementation dependent.

If the PMA is connected to the service interface of a PMD that includes the PMD control function and training is disabled by the management variable mr_training_enable, then precoder_tx_out_enable_*i*, precoder_rx_in_enable_*i*, precoder_tx_in_enable_*i*, and precoder_rx_out_enable_*i* are set as required by the implementation.

120.5.8 Link status

The PMA shall provide link status information to the PMA client using the PMA:IS_SIGNAL.indication primitive. The PMA continuously monitors the link status reported by the service interface below from the *inst*:IS_SIGNAL.indication primitive, and uses this as input to Signal Indication Logic (SIL) to determine the link status to report to the layer above. Other inputs to the SIL may include the status of clock and data recovery on the lanes from the service interface below the PMA and whether buffers/FIFOs have reached the required fill level to accommodate Skew Variation so that data is being sent on the output lanes.

120.5.9 PMA local loopback mode (optional)

PMA local loopback mode is optional. If it is implemented, it shall be as described in this subclause (120.5.9).

The PMA sublayer may provide a local loopback function. The function involves looping back each input lane to the corresponding output lane. Each bit received from the PMA:IS_UNITDATA_*i*.request(tx_symbol) primitive is looped back in the direction of the MAC using the PMA:IS_UNITDATA_*i*.indication(rx_symbol) primitive.

During local loopback, the PMA performs normal bit muxing of PCSLs per 120.5.2 onto the lanes in the Tx direction toward the service interface below the PMA.

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Ability to perform this function is indicated by the Local_loopback_ability status variable. If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.8.0 (45.2.1.7.15). A device is placed in local loopback mode when the Local_loopback_enable control variable is set to one, and removed from local loopback mode when this variable is set to zero. If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD control 1 register (bit 1.0.0, see 45.2.1.1.5).

120.5.10 PMA remote loopback mode (optional)

PMA remote loopback mode is optional. If implemented, it shall be as described in this subclause (120.5.10).

Remote loopback, if provided, should be implemented in a PMA sublayer close enough to the PMD to maintain the bit sequence on each individual PMD lane. When remote loopback is enabled, each symbol received over a lane of the service interface below the PMA via *inst*:IS_UNITDATA_*i*.indication is looped back to the corresponding output lane toward the PMD via *inst*:IS_UNITDATA_*i*.request. Note that the service interface below the PMA can be provided by the PHY XS, PMD, or another PMA sublayer.

During remote loopback, the PMA performs normal bit muxing of PCSLs per 120.5.2 onto the lanes in the Rx direction towards the PMA client.

The ability to perform this function is indicated by the 200G_Remote_loopback_ability and 400G_Remote_loopback_ability status variables for the 200GBASE-R PMA and 400GBASE-R PMA, respectively. If a Clause 45 MDIO is implemented, the 200G_Remote_loopback_ability and 400G_Remote_loopback_ability variables are accessible through bit 1.23.15 (45.2.1.21.1) and bit 1.24.15 (45.2.1.22.1), respectively. A device is placed in remote loopback mode when the Remote_loopback_enable control variable is set to one, and removed from remote loopback mode when this variable is set to zero. If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD Control register 1 (bit 1.0.1, see 45.2.1.1.4).

120.5.11 PMA test patterns (optional)

Where the output lanes of the PMA appear on a physically instantiated interface 200GAUI-n, 400GAUI-n or the PMD service interface (whether or not it is physically instantiated), the PMA may optionally generate and detect test patterns. These test patterns are used to test adjacent layer interfaces for an individual PMA sublayer or to perform testing between a physically instantiated interface of a PMA sublayer and external testing equipment.

120.5.11.1 Test patterns for NRZ encoded signals

For a 200GBASE-R PMA with 8 output lanes or a 400GBASE-R PMA with 16 output lanes using 2-level NRZ encoding, the test patterns in this clause may be supported.

The ability to generate each of the respective test patterns in each direction of transmission are indicated by the PRBS9_Tx_generator_ability, PRBS9_Rx_generator_ability, PRBS31_Tx_generator_ability, PRBS31_Rx_generator_ability, and Square_wave_ability status variables, which if a Clause 45 MDIO is implemented are accessible through bits 1.1500.5, 1.1500.4, 1.1500.3, 1.1500.1, and 1.1500.12, respectively (see 45.2.1.169).

120.5.11.1.1 PRBS31 test pattern

The ability to check PRBS31 test patterns in each direction of transmission are indicated by the PRBS31_Tx_checker_ability and PRBS31_Rx_checker_ability status variables, which, if a Clause 45 MDIO is implemented, are accessible through bits 1.1500.2 and 1.1500.0, respectively (see 45.2.1.169).

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If supported, when send Tx PRBS31 test pattern is enabled by the PRBS31_enable and PRBS_Tx_gen_enable control variables, the PMA shall generate a PRBS31 pattern (as defined in 49.2.8) on each of the lanes toward the service interface below the PMA via the *inst*:IS_UNITDATA_*i*.request primitive. To avoid correlated crosstalk, it is highly recommended that the PRBS31 patterns generated on each lane be generated from independent, random seeds or at a minimum offset of 20 000 UI between the PRBS31 sequence on any lane and any other lane. When send Tx PRBS31 test pattern is disabled, the PMA returns to normal operation performing bit multiplexing as described in 120.5.2. If a Clause 45 MDIO is implemented, the PRBS31_enable and PRBS_Tx_gen_enable control variables are accessible through bits 1.1501.7 and 1.1501.3 (see 45.2.1.170).

If supported, when send Rx PRBS31 test pattern is enabled by the PRBS31_enable and PRBS_Rx_gen_enable control variables, the PMA shall generate a PRBS31 pattern on each of the lanes toward the PMA client via the PMA:IS_UNITDATA_*i*.indication primitive. While this test pattern is enabled, the PMA also generates PMA:IS_SIGNAL.indication(SIGNAL_OK) toward the PMA client independent of the link status at the service interface below the PMA. When send Rx PRBS31 test pattern is disabled, the PMA returns to normal operation performing bit multiplexing as described in 120.5.2. If a Clause 45 MDIO is implemented, the PRBS31_enable and PRBS_Rx_gen_enable control variables are accessible through bits 1.1501.7 and 1.1501.1 (see 45.2.1.170).

If supported, when check Tx PRBS31 test pattern mode is enabled by the PRBS31_enable and PRBS_Tx_check_enable control variables, the PMA shall check for the PRBS31 pattern on each of the lanes received from the PMA client via the PMA:IS_UNITDATA_*i*.request primitive. The checker shall increment the test-pattern error counter by one for each incoming bit error in the PRBS31 pattern for isolated single bit errors. Implementations should be capable of counting at least one error whenever one or more errors occur in a sliding 1000-bit window. If a Clause 45 MDIO is implemented, the PRBS31_enable and PRBS_Tx_check_enable control variables are accessible through bits 1.1501.7 and 1.1501.2 (see 45.2.1.170). The Tx test-pattern error counters Ln0_PRBS_Tx_test_err_counter through Ln15_PRBS_Tx_test_err_counter count, per lane, errors in detecting the PRBS31 pattern on the lanes from the PMA client. If a Clause 45 MDIO is implemented, these counters are accessible through registers 1.1600 through 1.16015 (see 45.2.1.173). When check Tx PRBS31 test pattern is disabled, the PMA expects normal traffic and test-pattern error counting does not continue. While in check Tx PRBS31 test-pattern mode, bit multiplexing continues as described in 120.5.2. Note that bit multiplexing of per-lane PRBS31 may produce a signal which is not meaningful for downstream sublayers.

If supported, when check Rx PRBS31 test-pattern mode is enabled by the PRBS31_enable and PRBS_Rx_check_enable control variables, the PMA shall check for the PRBS31 pattern on each of the lanes received from the service interface below the PMA via the *inst*:IS_UNITDATA_*i*.indication primitive. If a Clause 45 MDIO is implemented, the PRBS31_enable and PRBS_Rx_check_enable control variables are accessible through bits 1.1501.7 and 1.1501.0 (see 45.2.1.170). The Rx test-pattern error counters Ln0_PRBS_Rx_test_err_counter through Ln15_PRBS_Rx_test_err_counter count, per lane, errors in detecting the PRBS31 pattern on the lanes from the service interface below the PMA. If a Clause 45 MDIO is implemented, these counters are accessible through registers 1.1700 through 1.1715 (see 45.2.1.174). While in check Rx PRBS31 test-pattern mode, the PMA:IS_SIGNAL.indication primitive does not indicate a valid signal. When check Rx PRBS31 test pattern is disabled, the PMA returns to normal operation performing bit multiplexing as described in 120.5.2.

120.5.11.1.2 PRBS9 test pattern

If supported, when send Tx PRBS9 test-pattern mode is enabled by the PRBS9_enable and Tx_gen_enable control variables, the PMA shall generate a PRBS9 pattern (as defined in Table 68–6) on each lane toward the service interface below the PMA via the *inst*:IS_UNITDATA_*i*.request primitive. If a Clause 45 MDIO is implemented, the PRBS9_enable and Tx_gen_enable control variables are accessible through bits 1.1501.6 and 1.1501.3 (see 45.2.1.170). When send Tx PRBS9 test-pattern mode is disabled, the PMA returns to normal operation performing bit multiplexing as described in 120.5.2.

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If supported, when send Rx PRBS9 test-pattern mode is enabled by the PRBS9_enable and Rx_gen_enable control variables, the PMA shall generate a PRBS9 pattern on each lane toward the PMA client via the PMA:IS_UNITDATA_*i*.indication primitive. The PMA also generates PMA:IS_SIGNAL.indication(SIGNAL_OK) toward the PMA client independent of the link status at the service interface below the PMA. If a Clause 45 MDIO is implemented, the PRBS9_enable and Rx_gen_enable control variables are accessible through bits 1.1501.6 and 1.1501.1 (see 45.2.1.170). When send Rx PRBS9 test-pattern mode is disabled, the PMA returns to normal operation performing bit multiplexing as described in 120.5.2.

Note that PRBS9 is intended to be checked by external test gear, and no PRBS9 checking function is provided within the PMA.

120.5.11.1.3 Square wave test pattern

Transmit square wave test-pattern mode optionally applies to each lane of the Tx direction PMA towards a physically instantiated 200GAUI-8, 400GAUI-16 or towards an NRZ PMD service interface whether or not it is physically instantiated. The ability to perform this function is indicated by the Square_wave_ability status variable. If a Clause 45 MDIO is implemented, the Square_wave_ability status variable is accessible through the Square wave test ability bit 1.1500.12 (see 45.2.1.169). If implemented, the transmit square wave test-pattern mode is enabled by control variables Square_wave_enable_0 through Square_wave_enable_15. If a Clause 45 MDIO is implemented, these control variables are accessible through the square wave testing control and status register bits 1.1510.0 through 1.1510.15 (limited to the number of lanes of the service interface below the PMA, see 45.2.1.171). When enabled, the PMA shall generate a square wave test pattern (8 ones followed by 8 zeros) on the square wave enabled lanes toward the service interface below the PMA via the *inst*:IS_UNITDATA_*i*.request primitive. Lanes for which square wave is not enabled transmit normal data resulting from the bit multiplexing operations described in 120.5.2 or test patterns as determined by other registers. When transmit square wave test pattern is disabled for all lanes, the PMA performs normal operation performing bit multiplexing as described in 120.5.2 or transmit test patterns as determined by other registers.

120.5.11.2 Test patterns for PAM4 encoded signals

For a 200GBASE-R PMA with 4 output lanes or a 400GBASE-R PMA with 4 or 8 output lanes using PAM4 encoding, the test patterns described in this clause may optionally be supported.

The patterns PRBS13Q and square wave (quaternary) can be enabled on a lane-by-lane basis. The patterns PRBS31Q and SSPRQ can be enabled on all lanes of an interface at once. If per-lane pattern(s) are enabled for a subset of the lanes and a per-interface pattern is also enabled, the per-lane patterns are generated only on the indicated lanes and the per-interface pattern is generated on the remaining lanes. The behavior if more than one per-lane pattern is enabled for the same lane or more than one per-interface pattern is enabled is not defined.

120.5.11.2.1 PRBS13Q test pattern

A PMA may optionally include a PRBS13Q pattern generator as specified in this subclause. The ability to perform this function is indicated by the PRBS13Q_gen_Tx_ability and PRBS13Q_gen_Rx_ability status variables, reflecting the ability to send this test pattern in the direction towards the PMD and towards the MAC, respectively. If a Clause 45 MDIO is implemented, the PRBS13Q_gen_Tx_ability and PRBS13Q_gen_Rx_ability status variables are accessible through the PRBS13Q Tx generator ability and PRBS13Q Rx generator ability bits 1.1500.11 and 1.1500.10 (see 45.2.1.169).

When the PRBS13Q test pattern enabled, it replaces the signal on the output lane(s) for which it is enabled. The PRBS13Q test pattern is a repeating 8191-symbol sequence formed by Gray coding pairs of bits from two repetitions of the PRBS13 pattern into PAM4 symbols as described in 120.5.7.1. The PRBS pattern

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generator produces the same result as the implementation shown in Figure 94–6, which implements the generator polynomial shown in Equation (94–3). Since the PRBS13 pattern is an odd number of bits in length, bits which are mapped as the first bit of a PAM4 symbol during one repetition of the PRBS13 sequence are mapped as the second bit of a PAM4 symbol during the next repetition of the PRBS13 sequence, and bits which are mapped as the second bit of a PAM4 symbol are mapped as the first bit of the following symbol in the next repetition of the PRBS13 sequence. For example, if the PRBS13 generator used to create the PRBS13Q sequence is initialized to a seed value of 0000010101011 (with the leftmost bit in S0 and the rightmost in S12), the PRBS13Q sequence begins with the following Gray coded PAM4 symbols, transmitted left to right: 10313202201111301031212312100121021210231311 12.

The PRBS13Q test pattern is enabled in the transmit direction by the Tx_gen_enable and PRBS13Q_enable_0 through PRBS13Q_enable_7 control variables (in the downstream direction towards the PMD), and in the receive direction by the Rx_gen_enable and PRBS13Q_enable_0 through PRBS13Q_enable_7 control variables (in the upstream direction towards the MAC). If the optional Clause 45 MDIO is implemented, the Tx_gen_enable and Rx_gen_enable control variables are accessible through the Tx generator enable and Rx generator enable bits 1.1501.3 and 1.1501.1 (see 45.2.1.170), and the PRBS13_enable_0 through PRBS13_enable_7 control variables are accessible through bits 1.1512.0 through 1.1512.7 (see 45.2.1.172).

120.5.11.2.2 PRBS31Q test pattern

A PMA may optionally include a PRBS31Q pattern generator as specified in this subclause. The ability to generate PRBS31Q patterns in each direction of transmission are indicated by the PRBS31Q_gen_Tx_ability and PRBS31Q_gen_Rx_ability status variables, reflecting the ability to send this test pattern in the direction towards the PMD and towards the MAC, respectively. The ability to check PRBS31Q patterns in each direction of transmission are indicated by the PRBS31Q_Tx_checker_ability and PRBS31Q_Rx_checker_ability status variables. If a Clause 45 MDIO is implemented, the PRBS31Q_gen_Tx_ability, PRBS31Q_gen_Rx_ability, PRBS31Q_Tx_checker_ability and PRBS31Q_Rx_checker_ability status variables are accessible through the PRBS31Q Tx generator ability, PRBS31Q Rx generator ability, PRBS31Q Tx checker ability, and PRBS31Q Rx checker ability bits 1.1500.9, 1.1500.7, 1.1500.8, and 1.1500.6 (see 45.2.1.169).

The PRBS31Q test pattern is a repeating 2^{31}–1-symbol sequence formed by Gray coding pairs of bits from two repetitions of the PRBS31 pattern defined in 49.2.8 into PAM4 symbols as described in 120.5.7.1. Since the PRBS31 pattern is an odd number of bits in length, bits that are mapped as the first bit of a PAM4 symbol during one repetition of the PRBS31 sequence are mapped as the second bit of a PAM4 symbol during the next repetition of the PRBS31 sequence, and bits that are mapped as the second bit of a PAM4 symbol during one repetition of the PRBS31 sequence are mapped as the first bit of the following symbol in the next repetition of the PRBS31 sequence. For example, if the PRBS31 generator used to create the PRBS31Q sequence is initialized to a seed value of all ones, the PRBS31Q sequence begins with the following Gray coded PAM4 symbols, transmitted left to right: 22222222222220122222222222200022222222222012012 22. To avoid correlated crosstalk, it is highly recommended that the PRBS31 patterns used to generate the PRBS31Q pattern on each lane are generated from independent, random seeds, or at a minimum offset of 20 000 UI between the PRBS31 sequence used to generate the PRBS31Q pattern on any lane and any other lane. A PRBS31Q pattern checker operates by converting PAM4 symbols received on each input lane to pairs of bits as described in 120.5.7.1 and then using a PRBS31 pattern checker on the resulting bit stream. The checker shall increment the test-pattern error counter by one for each incoming bit error in the PRBS31 pattern for isolated single bit errors. Implementations should be capable of counting at least one error whenever one or more errors occur in a sliding 1000-bit window.

If supported, when send Tx PRBS31Q test pattern is enabled by the PRBS31Q_pattern_enable and PRBS_Tx_gen_enable control variables, the PMA shall generate a PRBS31Q pattern on each of the lanes toward the service interface below the PMA via the *inst*:IS_UNITDATA_*i*.request primitive. When send Tx

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PRBS31Q test pattern is disabled, the PMA returns to normal operation performing bit multiplexing as described in 120.5.2. If a Clause 45 MDIO is implemented, the PRBS31Q_pattern_enable and PRBS_Tx_gen_enable control variables are accessible through bits 1.1501.13 and 1.1501.3 (see 45.2.1.170).

If supported, when send Rx PRBS31Q test pattern is enabled by the PRBS31Q_pattern_enable and PRBS_Rx_gen_enable control variables, the PMA shall generate a PRBS31Q pattern on each of the lanes toward the PMA client via the PMA:IS_UNITDATA_*i*.indication primitive. The PMA also generates PMA:IS_SIGNAL.indication(SIGNAL_OK) toward the PMA client independent of the link status at the service interface below the PMA. If a Clause 45 MDIO is implemented, the PRBS31Q_pattern_enable and PRBS_Rx_gen_enable control variables are accessible through bits 1.1501.13 and 1.1501.1 (see 45.2.1.170). When send Rx PRBS31Q test pattern is disabled, the PMA returns to normal operation performing bit multiplexing as described in 120.5.2.

If supported, when check Tx PRBS31Q test pattern mode is enabled by the PRBS31Q_pattern_enable and PRBS_Tx_check_enable control variables, the PMA checks for the PRBS31Q pattern on each of the lanes received from the PMA client via the PMA:IS_UNITDATA_*i*.request primitive. If a Clause 45 MDIO is implemented, the PRBS31Q_pattern_enable and PRBS_Tx_check_enable control variables are accessible through bits 1.1501.13 and 1.1501.2 (see 45.2.1.170). The Tx test-pattern error counters Ln0_PRBS_Tx_test_err_counter through either Ln3_PRBS_Tx_test_error_counter or Ln7_PRBS_Tx_test_error_counter (depending on whether the number of lanes is 4 or 8) count, per lane, errors in detecting the PRBS31 pattern resulting from converting the PAM4 symbols received on each lane to pairs of bits. If a Clause 45 MDIO is implemented, these counters are accessible through registers 1.1600 through 1.1603 or 1.1607 (depending on whether the number of lanes is 4 or 8) (see 45.2.1.173). When check Tx PRBS31Q test pattern is disabled, the PMA expects normal traffic and test pattern error counting does not continue. While in check Tx PRBS31Q mode, bit multiplexing continues as described in 120.5.2. Note that bit multiplexing of per-lane PRBS31Q may produce a signal which is not meaningful for downstream sublayers.

If supported, when check Rx PRBS31Q test pattern mode is enabled by the PRBS31Q_pattern_enable and PRBS_Rx_check_enable control variables, the PMA checks for the PRBS31Q pattern on each of the lanes received from the service interface below the PMA via the *inst*:IS_UNITDATA_*i*.indication primitive. If a Clause 45 MDIO is implemented, the PRBS31Q_pattern_enable and PRBS_Rx_check_enable control variables are accessible through bits 1.1501.13 and 1.1501.0 (see 45.2.1.170). The Rx test-pattern error counters Ln0_PRBS_Rx_test_err_counter through either Ln3_PRBS_Rx_test_error_counter or Ln7_PRBS_Rx_test_error_counter (depending on whether the number of lanes is 4 or 8) count, per lane, errors in detecting the PRBS31 pattern resulting from converting the PAM4 symbols received on each lane to pairs of bits. If a Clause 45 MDIO is implemented, these counters are accessible through registers 1.1700 through 1.1703 or 1.1707 (depending on whether the number of lanes is 4 or 8) (see 45.2.1.174). While in check Rx PRBS31Q mode, the PMA:IS_SIGNAL.indication primitive does not indicate a valid signal. When check Rx PRBS31Q test pattern is disabled, the PMA returns to normal operation performing bit multiplexing as described in 120.5.2.

120.5.11.2.3 SSPRQ test pattern

A PMA may optionally include a short stress pattern random quaternary (SSPRQ) test pattern generator as specified in this subclause. The ability to perform this function is indicated by the SSPRQ_gen_Tx_ability status variable, reflecting the ability to send this test pattern in the direction towards the PMD. If a Clause 45 MDIO is implemented, the SSPRQ_gen_Tx_ability status variable is accessible through the SSPRQ Tx generator ability bit 1.1500.13 (see 45.2.1.169).

The SSPRQ pattern is a repeating 2^{16}–1 PAM4 symbol sequence constructed as follows:

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— Bit sequence A is a 32768-bit sequence composed of three sections of the PRBS31 binary sequence (see 120.5.11.1.1) according to Table 120–2.

Table 120–2—SSPRQ bit sequence A

Pattern	Seed	Length
PRBS31	0x00000002	10924 bits
	0x34013FF7	10922 bits
	0x0CCCCCCC	10922 bits

— Each section of PRBS31 is generated as if produced by the shift register implementation shown in Figure 49–9 and the seed is a 31-bit hexadecimal value used to preset S30 through S0 (S30 is set to the MSB and S0 is set to the LSB) prior to the generation of the PRBS31 sequence for the indicated length of bits.

— Bit sequence B is a 65534-bit sequence formed by removing the first and last binary bit from a sequence consisting of two repetitions of bit sequence A.

— PAM4 sequence 1 is a 16384-symbol sequence formed by Gray coding bit sequence A according to 120.5.7.1.

— PAM4 sequence 2 is a 16384-symbol sequence formed by Gray coding bit sequence A according to 120.5.7.1, and then inverting each PAM4 symbol by replacing each PAM4 symbol *n* with the value 3–*n*.

— PAM4 sequence 3 is a 16383-symbol sequence formed by Gray coding the first 32766 bits of bit-sequence B according to 120.5.7.1.

— PAM4 sequence 4 is a 16384-symbol sequence formed by Gray coding the last 32768 bits of bit-sequence B according to 120.5.7.1, and then inverting each PAM4 symbol by replacing each PAM4 symbol *n* with the value 3–*n*.

— The repeating SSPRQ pattern formed by concatenating PAM4 sequences 1, 2, 3 and 4.

NOTE—A CSV file containing the entire PAM4 symbol sequence for the SSPRQ test pattern is available at https://standards.ieee.org/downloads/802.3/.

If supported, when send SSPRQ test pattern is enabled by the SSPRQ_pattern_enable control variable, the PMA shall generate an SSPRQ pattern on each of its lanes in the Tx direction towards the PMD with at least a 31 UI delay between the SSPRQ pattern on one lane and any other lane. If a Clause 45 MDIO is implemented, the SSPRQ_pattern_enable control variable is accessible through the SSPRQ pattern enable bit 1.1501.14 (see 45.2.1.170).

120.5.11.2.4 Square wave (quaternary) test pattern

Transmit square wave (quaternary) test-pattern mode optionally applies to each lane of the Tx direction PMA towards a physically instantiated 200GAUI-4, 400GAUI-8 or towards a PAM4 PMD service interface whether or not it is physically instantiated.

The ability to perform this function is indicated by the Square_wave_ability status variable. If a Clause 45 MDIO is implemented, the Square_wave_ability status variable is accessible through the Square wave test ability bit 1.1500.12 (see 45.2.1.169). If implemented, the transmit square wave test-pattern mode is enabled by control variables Square_wave_enable_0 through Square_wave_enable_8. If a Clause 45 MDIO is implemented, these control variables are accessible through the square wave testing control and status register bits 1.1510.0 through 1.1510.15 (limited to the number of lanes of the service interface below the PMA, see 45.2.1.171). When enabled, the PMA shall generate a square wave test pattern (8 threes followed

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by 8 zeros) on the square wave enabled lanes toward the service interface below the PMA via the *inst*:IS_UNITDATA_*i*.request primitive. Lanes for which square wave is not enabled transmit normal data resulting from the bit multiplexing operations described in 120.5.2 or test patterns as determined by other registers. When transmit square wave test pattern is disabled for all lanes, the PMA performs normal operation performing bit multiplexing as described in 120.5.2 or transmit test patterns as determined by other registers.

NOTE—A square wave transmitted over a 200GAUI-4 or 400GAUI-8 may not be correctly forwarded to the PMD transmitter output.

120.6 PMA MDIO function mapping

The optional MDIO capability described in Clause 45 describes several variables that provide control and status information for and about the PMA. Since a given implementation may employ more than one PMA sublayer, the PMA control and status information is organized into multiple addressable instances, one for each possible PMA sublayer. See 45.2.1 and 120.1.4 for the allocation of MMD addresses to PMA sublayers. Control and status registers for MMD 8, 9, and 10 use the Extended PMA control and status registers at identical locations to those for MMD 1.

Mapping of MDIO control variables to PMA control variables is shown in Table 120–3. Mapping of MDIO status variables to PMA status variables is shown in Table 120–4. Mapping of MDIO counter to PMA counters is shown in Table 120–5. These tables provide the register and bit numbers for the PMA addressed as MMD 1. For implementations with multiple PMA sublayers, additional PMA sublayers use the corresponding register and bit numbers in MMDs 8, 9, and 10 as necessary.

Table 120–3—MDIO/PMA control variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
PMA remote loopback	PMA/PMD control 1	1.0.1	Remote_loopback_enable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
Lane 0 Tx output precoder enable	PMA precoder control Tx output	1.600.0	precoder_tx_out_enable_0
Lane 1 Tx output precoder enable	PMA precoder control Tx output	1.600.1	precoder_tx_out_enable_1
Lane 2 Tx output precoder enable	PMA precoder control Tx output	1.600.2	precoder_tx_out_enable_2
Lane 3 Tx output precoder enable	PMA precoder control Tx output	1.600.3	precoder_tx_out_enable_3
Lane 0 Rx input precoder enable	PMA precoder control Rx input	1.601.0	precoder_rx_in_enable_0
Lane 1 Rx input precoder enable	PMA precoder control Rx input	1.601.1	precoder_rx_in_enable_1
Lane 2 Rx input precoder enable	PMA precoder control Rx input	1.601.2	precoder_rx_in_enable_2
Lane 3 Rx input precoder enable	PMA precoder control Rx input	1.601.3	precoder_rx_in_enable_3
PRBS31 pattern enable	PRBS pattern testing control	1.1501.7	PRBS31_enable
PRBS9 pattern enable	PRBS pattern testing control	1.1501.6	PRBS9_enable
PRBS31Q pattern enable	PRBS pattern testing control	1.1501.13	PRBS31Q_pattern_enable
SSPRQ pattern enable	PRBS pattern testing control	1.1501.14	SSPRQ_pattern_enable
Tx generator enable	PRBS pattern testing control	1.1501.3	PRBS_Tx_gen_enable

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Table 120–3—MDIO/PMA control variable mapping *(continued)*

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
Tx checker enable	PRBS pattern testing control	1.1501.2	PRBS_Tx_check_enable
Rx generator enable	PRBS pattern testing control	1.1501.1	PRBS_Rx_gen_enable
Rx checker enable	PRBS pattern testing control	1.1501.0	PRBS_Rx_check_enable
Lane 0 SW enable	Square wave testing control	1.1510.0	Square_wave_enable_0
Lane 1 SW enable	Square wave testing control	1.1510.1	Square_wave_enable_1
Lane 2 SW enable	Square wave testing control	1.1510.2	Square_wave_enable_2
Lane 3 SW enable	Square wave testing control	1.1510.3	Square_wave_enable_3
Lane 4 SW enable	Square wave testing control	1.1510.4	Square_wave_enable_4
Lane 5 SW enable	Square wave testing control	1.1510.5	Square_wave_enable_5
Lane 6 SW enable	Square wave testing control	1.1510.6	Square_wave_enable_6
Lane 7 SW enable	Square wave testing control	1.1510.7	Square_wave_enable_7
Lane 8 SW enable	Square wave testing control	1.1510.8	Square_wave_enable_8
Lane 9 SW enable	Square wave testing control	1.1510.9	Square_wave_enable_9
Lane 10 SW enable	Square wave testing control	1.1510.10	Square_wave_enable_10
Lane 11 SW enable	Square wave testing control	1.1510.11	Square_wave_enable_11
Lane 12 SW enable	Square wave testing control	1.1510.12	Square_wave_enable_12
Lane 13 SW enable	Square wave testing control	1.1510.13	Square_wave_enable_13
Lane 14 SW enable	Square wave testing control	1.1510.14	Square_wave_enable_14
Lane 15 SW enable	Square wave testing control	1.1510.15	Square_wave_enable_15
Lane 0 PRBS13Q enable	PRBS13Q testing control	1.1512.0	PRBS13Q_enable_0
Lane 1 PRBS13Q enable	PRBS13Q testing control	1.1512.1	PRBS13Q_enable_1
Lane 2 PRBS13Q enable	PRBS13Q testing control	1.1512.2	PRBS13Q_enable_2
Lane 3 PRBS13Q enable	PRBS13Q testing control	1.1512.3	PRBS13Q_enable_3
Lane 4 PRBS13Q enable	PRBS13Q testing control	1.1512.4	PRBS13Q_enable_4
Lane 5 PRBS13Q enable	PRBS13Q testing control	1.1512.5	PRBS13Q_enable_5
Lane 6 PRBS13Q enable	PRBS13Q testing control	1.1512.6	PRBS13Q_enable_6
Lane 7 PRBS13Q enable	PRBS13Q testing control	1.1512.7	PRBS13Q_enable_7

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Table 120–4—MDIO/PMA status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMA status variable
PMA remote loopback ability	200G PMA/PMD extended ability register	1.23.15	200G_Remote_loopback_ability
PMA remote loopback ability	400G PMA/PMD extended ability register	1.24.15	400G_Remote_loopback_ability
PMA local loopback ability	PMA/PMD status 2 register	1.8.0	Local_loopback_ability
PRBS9 Tx generator ability	Test-pattern ability register	1.1500.5	PRBS9_Tx_generator_ability
PRBS9 Rx generator ability	Test-pattern ability register	1.1500.4	PRBS9_Rx_generator_ability
PRBS31Tx generator ability	Test-pattern ability register	1.1500.3	PRBS31_Tx_generator_ability
PRBS31Tx checker ability	Test-pattern ability register	1.1500.2	PRBS31_Tx_checker_ability
PRBS31 Rx generator ability	Test-pattern ability register	1.1500.1	PRBS31_Rx_generator_ability
PRBS31 Rx checker ability	Test-pattern ability register	1.1500.0	PRBS31_Rx_checker_ability
Square wave test ability	Test-pattern ability register	1.1500.12	Square_wave_ability
PRBS13Q Tx generator ability	Test-pattern ability register	1.1500.11	PRBS13Q_gen_Tx_ability
PRBS13Q Rx generator ability	Test-pattern ability register	1.1500.10	PRBS13Q_gen_Rx_ability
PRBS31Q Tx generator ability	Test-pattern ability register	1.1500.9	PRBS31Q_gen_Tx_ability
PRBS31Q Rx generator ability	Test-pattern ability register	1.1500.7	PRBS31Q_gen_rx_ability
PRBS31Q Tx checker ability	Test-pattern ability register	1.1500.8	PRBS31Q_Tx_checker_ability
PRBS31Q Rx checker ability	Test-pattern ability register	1.1500.6	PRBS31Q_Rx_checker_ability
SSPRQ Tx generator ability	Test-pattern ability register	1.1500.13	SSPRQ_gen_Tx_ability

Table 120–5—MDIO/PMA counters mapping

MDIO variable	PMA/PMD register name	Register/bit number	PMA status variable
Error counter Tx, lane 0	PRBS Tx pattern testing error counter, lane 0	1.1600	Ln0_PRBS_Tx_test_err_counter
Error counter Tx, lane 1	PRBS Tx pattern testing error counter, lane 1	1.1601	Ln1_PRBS_Tx_test_err_counter
Error counter Tx, lane 2	PRBS Tx pattern testing error counter, lane 2	1.1602	Ln2_PRBS_Tx_test_err_counter
Error counter Tx, lane 3	PRBS Tx pattern testing error counter, lane 3	1.1603	Ln3_PRBS_Tx_test_err_counter
Error counter Tx, lane 4	PRBS Tx pattern testing error counter, lane 4	1.1604	Ln4_PRBS_Tx_test_err_counter

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Table 120–5—MDIO/PMA counters mapping *(continued)*

MDIO variable	PMA/PMD register name	Register/bit number	PMA status variable
Error counter Tx, lane 5	PRBS Tx pattern testing error counter, lane 5	1.1605	Ln5_PRBS_Tx_test_err_counter
Error counter Tx, lane 6	PRBS Tx pattern testing error counter, lane 6	1.1606	Ln6_PRBS_Tx_test_err_counter
Error counter Tx, lane 7	PRBS Tx pattern testing error counter, lane 7	1.1607	Ln7_PRBS_Tx_test_err_counter
Error counter Tx, lane 8	PRBS Tx pattern testing error counter, lane 8	1.1608	Ln8_PRBS_Tx_test_err_counter
Error counter Tx, lane 9	PRBS Tx pattern testing error counter, lane 9	1.1609	Ln9_PRBS_Tx_test_err_counter
Error counter Tx, lane 10	PRBS Tx pattern testing error counter, lane 10	1.1610	Ln10_PRBS_Tx_test_err_counter
Error counter Tx, lane 11	PRBS Tx pattern testing error counter, lane 11	1.1611	Ln11_PRBS_Tx_test_err_counter
Error counter Tx, lane 12	PRBS Tx pattern testing error counter, lane 12	1.1612	Ln12_PRBS_Tx_test_err_counter
Error counter Tx lane 13	PRBS Tx pattern testing error counter, lane 13	1.1613	Ln13_PRBS_Tx_test_err_counter
Error counter Tx lane 14	PRBS Tx pattern testing error counter, lane 14	1.1614	Ln14_PRBS_Tx_test_err_counter
Error counter Tx lane 15	PRBS Tx pattern testing error counter, lane 15	1.1615	Ln15_PRBS_Tx_test_err_counter
Error counter Rx, lane 0	PRBS Rx pattern testing error counter, lane 0	1.1700	Ln0_PRBS_Rx_test_err_counter
Error counter Rx, lane 1	PRBS Rx pattern testing error counter, lane 1	1.1701	Ln1_PRBS_Rx_test_err_counter
Error counter Rx, lane 2	PRBS Rx pattern testing error counter, lane 2	1.1702	Ln2_PRBS_Rx_test_err_counter
Error counter Rx, lane 3	PRBS Rx pattern testing error counter, lane 3	1.1703	Ln3_PRBS_Rx_test_err_counter
Error counter Rx, lane 4	PRBS Rx pattern testing error counter, lane 4	1.1704	Ln4_PRBS_Rx_test_err_counter
Error counter Rx, lane 5	PRBS Rx pattern testing error counter, lane 5	1.1705	Ln5_PRBS_Rx_test_err_counter
Error counter Rx, lane 6	PRBS Rx pattern testing error counter, lane 6	1.1706	Ln6_PRBS_Rx_test_err_counter
Error counter Rx, lane 7	PRBS Rx pattern testing error counter, lane 7	1.1707	Ln7_PRBS_Rx_test_err_counter
Error counter Rx, lane 8	PRBS Rx pattern testing error counter, lane 8	1.1708	Ln8_PRBS_Rx_test_err_counter
Error counter Rx, lane 9	PRBS Rx pattern testing error counter, lane 9	1.1709	Ln9_PRBS_Rx_test_err_counter

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Table 120–5—MDIO/PMA counters mapping *(continued)*

MDIO variable	PMA/PMD register name	Register/bit number	PMA status variable
Error counter Rx, lane 10	PRBS Rx pattern testing error counter, lane 10	1.1710	Ln10_PRBS_Rx_test_err_counter
Error counter Rx, lane 11	PRBS Rx pattern testing error counter, lane 11	1.1711	Ln11_PRBS_Rx_test_err_counter
Error counter Rx, lane 12	PRBS Rx pattern testing error counter, lane 12	1.1712	Ln12_PRBS_Rx_test_err_counter
Error counter Rx, lane 13	PRBS Rx pattern testing error counter, lane 13	1.1713	Ln13_PRBS_Rx_test_err_counter
Error counter Rx, lane 14	PRBS Rx pattern testing error counter, lane 14	1.1714	Ln14_PRBS_Rx_test_err_counter
Error counter Rx, lane 15	PRBS Rx pattern testing error counter, lane 15	1.1715	Ln15_PRBS_Rx_test_err_counter

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120.7 Protocol implementation conformance statement (PICS) proforma for Clause 120, Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R[207]

120.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 120, Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

120.7.2 Identification

120.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

120.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 120, Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[207] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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120.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PMA200	PMA for 200GBASE-R	120.1.1		O.1	Yes [ ] No [ ]
*PMA400	PMA for 400GBASE-R	120.1.1		O.1	Yes [ ] No [ ]
*LNS_UP-STRM	Number of lanes in direction of MAC	120.1.4	Divisor of number of PCS lanes	PMA200: M	8 [ ] 4 [ ]
				PMA400:M	16 [ ] 8 [ ]
*UP_NRZ	NRZ modulation used for PMA service interface	120.1.4		(PMA200* LNS_UPSTRM=8 or PMA400* LNS_UPSTRM=16) :M	Yes [ ] N/A [ ]
*UP_PAM4	PAM4 modulation used for PMA service interface	120.1.4		(PMA200* LNS_UPSTRM=4 or PMA400* LNS_UPSTRM=8) :M	Yes [ ] N/A [ ]
*LNS_DN-STRM	Number of lanes in the direction of PMD	120.1.4	Divisor of number of PCS lanes	PMA200: M	8 [ ] 4 [ ]
				PMA400:M	16 [ ] 8 [ ] 4 [ ]
*DN_NRZ	NRZ modulation used for service interface below the PMA	120.1.4		(PMA200* LNS_DNSTRM=8 or PMA400* LNS_DNSTRM=16) :M	Yes [ ] N/A [ ]
*DN_PAM4	PAM4 modulation used for service interface below the PMA	120.1.4		(PMA200* LNS_DNSTRM=4 or PMA400* LNS_DNSTRM<16) :M	Yes [ ] N/A [ ]
RX_CLOCK	Signaling rate of output lanes in Rx direction	120.5.5	26.5625 GBd	M	Yes [ ]
TX_CLOCK	Signaling rate of output lanes in Tx direction	120.5.5	26.5625 GBd	PMA200:M	Yes [ ] N/A [ ]
			LNS_DNSTRM= 8 or 16: 26.5625 GBd LNS_DNSTRM= 4: 53.125 GBd	PMA400:M	Yes [ ] N/A [ ]
LANE_ MAPPING	Maintain lane mapping while link is in operation	120.5.2	Maintain sequence of PCSLs on all output lanes	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
LNKS	PMA link status	120.5.8	Meets the requirements of 120.5.8	M	Yes [ ]
*LBL	PMA local loopback	120.5.9	Supports local loopback	O	Yes [ ] No [ ]
*LBR	PMA remote loopback	120.5.10	Supports remote loopback	O	Yes [ ] No [ ]
MD	MDIO	120.6	Registers and interface supported	O	Yes [ ] No [ ]
*USP1SP6	Physically instantiated 200GAUI-n or 400GAUI-n above (toward MAC)	120.5.3		O	Yes [ ] No [ ]
*DSP1SP6	Physically instantiated 200GAUI-n or 400GAUI-n below (toward PMD)	120.5.3		O	Yes [ ] No [ ]
*SP2SP5	Physically instantiated PMD service interface	120.5.3		O	Yes [ ] No [ ]
UNAUI	Electrical and timing requirements of Annex 120B, Annex 120C, Annex 120D, or Annex 120E as appropriate met by 200GAUI-n or 400GAUI-n of the PMA service interface	120.5.1, 120.5.5		USP1SP6:M	Yes [ ] N/A [ ]
DNAUI	Electrical and timing requirements of Annex 120B, Annex 120C, Annex 120D, or Annex 120E as appropriate met by 200GAUI-n or 400GAUI-n of the service interface below the PMA	120.5.1, 120.5.5		DSP1SP6:M	Yes [ ] N/A [ ]
DELAY200	Roundtrip delay limit for 200GBASE-R	120.5.4	No more than 18 432 BT or 36 pause_quanta	PMA200:M	Yes [ ] N/A [ ]
DELAY400	Roundtrip delay limit for 400GBASE-R	120.5.4	No more than 36 864 BT or 72 pause_quanta	PMA400:M	Yes [ ] N/A [ ]

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120.7.4 Skew generation and tolerance

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Skew generation toward SP1 in Tx direction	120.5.3.1	≤ 29 ns	DSP1S P6:M	Yes [ ] N/A [ ]
S2	Skew variation generation toward SP1 in Tx direction	120.5.3.1	≤ 200 ps	DSP1S P6:M	Yes [ ] N/A [ ]
S3	Skew variation tolerance at SP1	120.5.3.2	Minimum 200 ps	USP1S P6:M	Yes [ ] N/A [ ]
S4	Skew generation toward SP2 in Tx direction	120.5.3.3	≤ 43 ns	SP2SP 5:M	Yes [ ] N/A [ ]
S5	Skew variation generation toward SP2 in Tx direction	120.5.3.3	≤ 400 ps	SP2SP 5:M	Yes [ ] N/A [ ]
S6	Skew variation tolerance at SP5	120.5.3.4	Minimum 3.6 ns	SP2SP 5:M	Yes [ ] N/A [ ]
S7	Skew generation toward SP6 in Rx direction	120.5.3.5	≤ 160 ns	USP1S P6:M	Yes [ ] N/A [ ]
S8	Skew variation generation toward SP6 in Rx direction	120.5.3.5	≤ 3.8 ns	USP1S P6:M	Yes [ ] N/A [ ]
S9	Skew variation tolerance at SP6	120.5.3.6	Minimum 3.8 ns	DSP1S P6:M	Yes [ ] N/A [ ]

120.7.5 Test patterns

Item	Feature	Subclause	Value/Comment	Status	Support
*JTP1	Physically Instantiated 200GAUI-n or 400GAUI-n between PMA and PMA client	120.5.11		O	Yes [ ] No [ ]
*JTP2	Physically Instantiated 200GAUI-n or 400GAUI-n between PMA and sublayer below the PMA, or adjacent to PMD	120.5.11		O	Yes [ ] No [ ]
J1	Send PRBS31 Tx	120.5.11.1.1		JTP2* DN_NRZ:O	Yes [ ] No [ ] N/A [ ]
J2	Send PRBS31 Rx	120.5.11.1.1		JTP1* UP_NRZ:O	Yes [ ] No [ ] N/A [ ]
J3	Check PRBS31 Tx	120.5.11.1.1		JTP1* UP_NRZ:O	Yes [ ] No [ ] N/A [ ]
J4	Check PRBS31 Rx	120.5.11.1.1		JTP2* DN_NRZ:O	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
J5	Send PRBS9 Tx	120.5.11.1.2		JTP2* DN_NRZ:O	Yes [ ] No [ ] N/A [ ]
J6	Send PRBS9 Rx	120.5.11.1.2		JTP1* UP_NRZ:O	Yes [ ] No [ ] N/A [ ]
J7	Send square wave Tx	120.5.11.1.3		JTP2* DN_NRZ:O	Yes [ ] No [ ] N/A [ ]
J8	Send PRBS13Q Tx	120.5.11.2.1		JTP2* DN_PAM4:O	Yes [ ] No [ ] N/A [ ]
J9	Send PRBS13Q Rx	120.5.11.2.1		JTP1* UP_PAM4:O	Yes [ ] No [ ] N/A [ ]
J10	Send PRBS31Q Tx	120.5.11.2.2		JTP2* DN_PAM4:O	Yes [ ] No [ ] N/A [ ]
J11	Send PRBS31Q Rx	120.5.11.2.2		JTP1* UP_PAM4:O	Yes [ ] No [ ] N/A [ ]
J12	Check PRBS31Q Tx	120.5.11.2.2		JTP1* UP_PAM4:O	Yes [ ] No [ ] N/A [ ]
J13	Check PRBS31Q Rx	120.5.11.2.2		JTP2* DN_PAM4:O	Yes [ ] No [ ] N/A [ ]
J14	Send SSPRQ Tx	120.5.11.2.3		DN_PAM4:O	Yes [ ] No [ ] N/A [ ]
J15	Send square wave (quaternary) Tx	120.5.11.2.4		DN_PAM4:O	Yes [ ] No [ ] N/A [ ]

120.7.6 Loopback modes

Item	Feature	Subclause	Value/Comment	Status	Support
LB1	PMA local loopback implemented	120.5.9	Meets the requirements of 120.5.9	LBL:M	Yes [ ] N/A [ ]
LB2	PMA remote loopback implemented	120.5.10	Meets the requirements of 120.5.10	LBR:M	Yes [ ] N/A [ ]

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120.7.7 Encoding

Item	Feature	Subclause	Value/Comment	Status	Support
*CKR4	PMA is adjacent to a 200GBASE-CR4 or 200GBASE-KR4 PMD.	120.5.7.2		O	Yes [ ] No [ ]
E1	PMA supports Tx precoding	120.5.7.2		CKR4:M	Yes [ ] N/A [ ]
E2	PMA supports Rx precoding	120.5.7.2		CKR4:O	Yes [ ] No [ ] N/A [ ]

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121. Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-DR4

121.1 Overview

This clause specifies the 200GBASE-DR4 PMD together with the single-mode fiber medium. The optical signal generated by this PMD type is modulated using a 4-level pulse amplitude modulation (PAM4) format. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 121–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 121–1—Physical Layer clauses associated with the 200GBASE-DR4 PMD

Associated clause	200GBASE-DR4
117—RS	Required
117—200GMII[a]	Optional
118—200GMII Extender	Optional
119—PCS	Required
120—PMA	Required
120B—Chip-to-chip 200GAUI-8	Optional
120C—Chip-to-module 200GAUI-8	Optional
120D—Chip-to-chip 200GAUI-4	Optional
120E—Chip-to-module 200GAUI-4	Optional
78—Energy Efficient Ethernet	Optional

[a] The 200GMII is an optional interface. However, if the 200GMII is not implemented, a conforming implementation behaves functionally as though the RS and 200GMII were present.

Figure 121–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 200 Gb/s Ethernet is introduced in Clause 116 and the purpose of each PHY sublayer is summarized in 116.2.

200GBASE-DR4 PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

121.1.1 Bit error ratio

The bit error ratio (BER) when processed according to Clause 120 shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when processed according to Clause 120 and then Clause 119. For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

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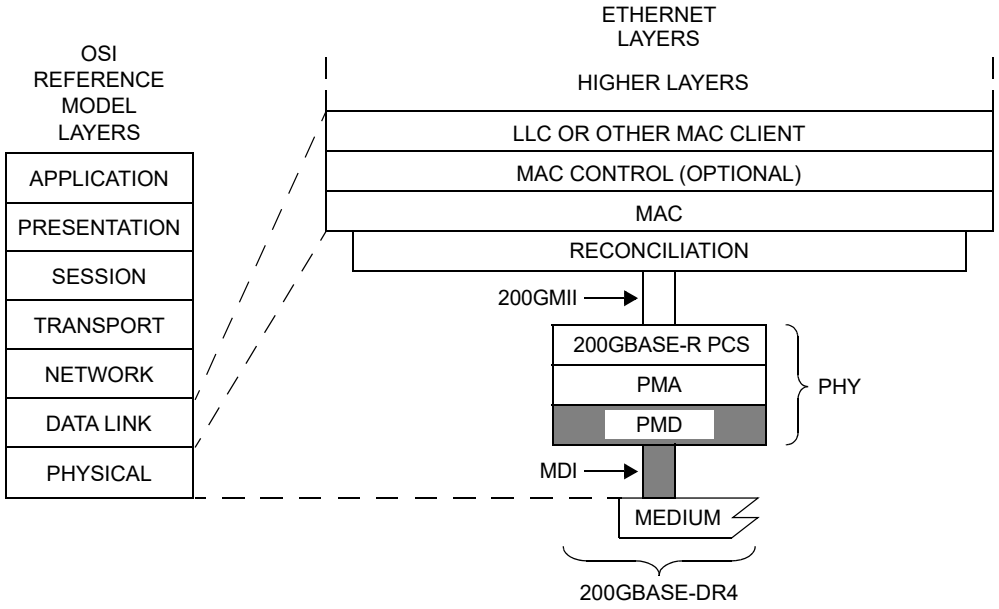

200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
DR = PMD FOR SINGLE-MODE FIBER — 500 m

Figure 121–1—200GBASE-DR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap.

121.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 200GBASE-DR4 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 116.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 200GBASE-DR4 PMD has four parallel symbol streams, hence $i = 0$ to 3.

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In the transmit direction, the PMA continuously sends four parallel symbol streams to the PMD, one per lane, each at a nominal signaling rate of 26.5625 GBd. The PMD then converts these streams of data units into the appropriate signals on the MDI.

In the receive direction, the PMD continuously sends four parallel symbol streams to the PMA corresponding to the signals received from the MDI, one per lane, each at a nominal signaling rate of 26.5625 GBd.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication(SIGNAL_OK) inter-sublayer service interface primitive defined in 116.3.

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 121.1.1.

121.3 Delay and Skew

121.3.1 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the 200GBASE-DR4 PMD including 2 m of fiber in one direction shall be no more than 4096 bit times (8 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 116.4 and its references.

121.3.2 Skew constraints

The Skew (relative delay between the lanes) and Skew Variation are kept within limits so that the information on the lanes can be reassembled by the PCS. Skew and Skew Variation are defined in 116.5 and specified at the points SP1 to SP6 shown in Figure 116–4 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 116.5. The measurements of Skew and Skew Variation are defined in 86.8.3.1.

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121.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 121–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 121–3.

Table 121–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable 3 to PMD transmit disable 0	PMD transmit disable register	1.9.4 to 1.9.1	PMD_transmit_disable_3 to PMD_transmit_disable_0

Table 121–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 0	PMD receive signal detect register	1.10.4 to 1.10.1	PMD_signal_detect_3 to PMD_signal_detect_0

121.5 PMD functional specifications

The 200GBASE-DR4 PMD performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

121.5.1 PMD block diagram

The PMD block diagram is shown in Figure 121–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 121.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 121.11.3). Unless specified otherwise, all receiver measurements and tests defined in 121.8 are made at TP3.

TP1<0:3> and TP4<0:3> are optional reference points that may be useful to implementors for testing components (these test points will not typically be accessible in an implemented system).

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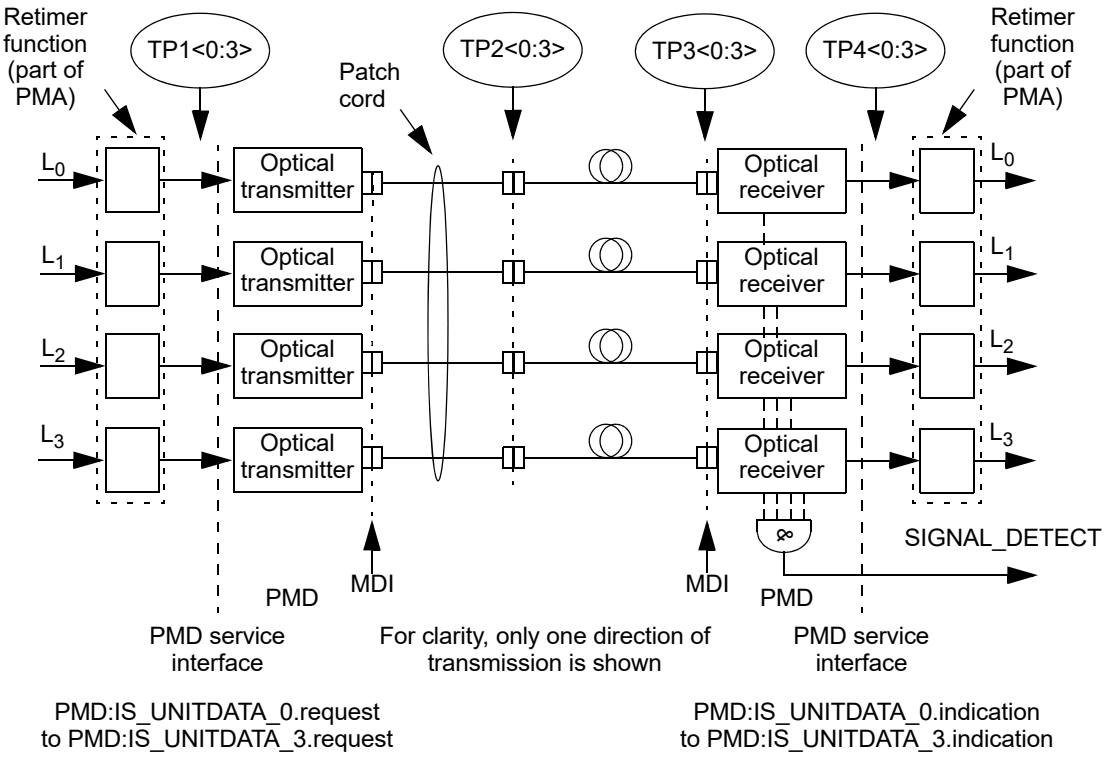

Figure 121–2—Block diagram for 200GBASE-DR4 transmit/receive paths

121.5.2 PMD transmit function

The PMD Transmit function shall convert the four symbol streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request into four separate optical signals. The four optical signals shall then be delivered to the MDI, which contains four parallel light paths for transmit, according to the transmit optical specifications in this clause. The highest optical power level in each signal shall correspond to tx_symbol = three and the lowest shall correspond to tx_symbol = zero.

121.5.3 PMD receive function

The PMD Receive function shall convert the four parallel optical signals received from the MDI into separate symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to rx_symbol = three and the lowest shall correspond to rx_symbol = zero.

121.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 116.3.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all four lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 121–4.

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The PMD receiver is not required to verify whether a compliant 200GBASE-DR4 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 121–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –16 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ average receive power, each lane (min) Table 121–7) AND (compliant 200GBASE–R signal input)]	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

121.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where i represents the lane number in the range 0:3, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 121–4.

121.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

121.5.7 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 121–6.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter in each lane.

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121.5.8 PMD lane-by-lane transmit disable function (optional)

The PMD lane-by-lane transmit disable function is optional and allows the optical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:3) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 121–6.

b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the optical transmitter in each lane.

If the optional PMD lane-by-lane transmit disable function is not implemented in MDIO, an alternative method may be provided to independently disable each transmit lane for testing purposes.

121.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

121.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

121.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

121.6 Lane assignments

There are no lane assignments (within a group of transmit or receive lanes) for 200GBASE-DR4. While it is expected that a PMD will map electrical lane *i* to optical lane *i* and vice versa, there is no need to define the physical ordering of the lanes, as the PCS sublayer is capable of receiving the lanes in any arrangement. The positioning of transmit and receive lanes at the MDI is specified in 121.11.3.1.

121.7 PMD to MDI optical specifications for 200GBASE-DR4

The operating range for the 200GBASE-DR4 PMD is defined in Table 121–5. A 200GBASE-DR4 compliant PMD operates on type B1.1, B1.3, or B6_a single-mode fibers according to the specifications defined in Table 121–14. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 200GBASE-DR4 PMD operating at 600 m meets the operating range requirement of 2 m to 500 m).

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Table 121–5—200GBASE-DR4 operating range

PMD type	Required operating range
200GBASE-DR4	2 m to 500 m

121.7.1 200GBASE-DR4 transmitter optical specifications

The 200GBASE-DR4 transmitter shall meet the specifications defined in Table 121–6 per the definitions in 121.8.

Table 121–6—200GBASE-DR4 transmit characteristics

Description	Value	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm	GBd
Modulation format	PAM4	—
Lane wavelength (range)	1304.5 to 1317.5	nm
Side-mode suppression ratio (SMSR), (min)	30	dB
Average launch power, each lane (max)	3	dBm
Average launch power, each lane[a] (min)	–5.1	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	2.8	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)[b]	–3	dBm
Launch power in OMA_{outer} minus TDECQ, each lane (min)	–4.4	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	3.2	dB
TDECQ – $10\log_{10}(C_{eq})$[c] (max)	3.2	dB
Average launch power of OFF transmitter, each lane (max)	–16	dBm
Extinction ratio, each lane (min)	3.5	dB
Transmitter transition time (max)	34	ps
$RIN_{21.4}OMA$ (max)	–132	dB/Hz
Optical return loss tolerance (max)	21.4	dB
Transmitter reflectance[d] (max)	–26	dB

[a] Average launch power, each lane (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b] Even if the TDECQ < 1.4 dB, the OMA_{outer} (min) has to exceed this value.
[c] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[d] Transmitter reflectance is defined looking into the transmitter.

121.7.2 200GBASE-DR4 receive optical specifications

The 200GBASE-DR4 receiver shall meet the specifications defined in Table 121–7 per the definitions in 121.8.

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Table 121–7—200GBASE-DR4 receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	26.5625± 100 ppm	GBd
Modulation format	PAM4	—
Lane wavelengths (range)	1304.5 to 1317.5	nm
Damage threshold[a], each lane	4	dBm
Average receive power, each lane (max)	3	dBm
Average receive power, each lane[b] (min)	–8.1	dBm
Receive power (OMA_{outer}), each lane (max)	2.8	dBm
Receiver reflectance (max)	–26	dB
Receiver sensitivity (OMA_{outer}), each lane[c] (max)	Equation (121–13)	dBm
Stressed receiver sensitivity (OMA_{outer}), each lane[d] (max)	–4.3	dBm
Conditions of stressed receiver sensitivity test:[e]		
Stressed eye closure for PAM4 (SECQ), lane under test	3.2	dB
SECQ – $10\log_{10}(C_{eq})$[f] (max), lane under test	3.2	dB
OMA_{outer} of each aggressor lane	2.8	dBm

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
[b] Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] Receiver sensitivity (OMA_{outer}), each lane (max) is optional and is defined for a transmitter with a value of SECQ up to 3.2 dB.
[d] Measured with conformance test signal at TP3 (see 121.8.10) for the BER specified in 121.1.1.
[e] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

121.7.3 200GBASE-DR4 illustrative link power budget

An illustrative power budget and penalties for 200GBASE-DR4 channels are shown in Table 121–8.

Table 121–8—200GBASE-DR4 illustrative link power budget

Parameter	Value	Unit
Power budget (for max TDECQ)	6.3	dB
Operating distance	500	m
Channel insertion loss[a]	3	dB
Maximum discrete reflectance	See 121.11.2.2	dB
Allocation for penalties[b] (for max TDECQ)	3.3	dB
Additional insertion loss allowed	0	dB

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[a] The channel insertion loss is calculated using the maximum distance specified in Table 121–5 and cabled optical fiber attenuation of 0.5 dB/km at 1304.5 nm plus an allocation for connection and splice loss given in 121.11.2.1.
[b] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

121.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

121.8.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 121–10 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 121–10 may be used to perform that test. The test patterns used in this clause are shown in Table 121–9.

Table 121–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle	119.2.4.9
6	SSPRQ	120.5.11.2.3

Table 121–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 200GBASE-R signal	121.8.2
Side mode suppression ratio	3, 5, 6 or valid 200GBASE-R signal	121.8.2
Average optical power	3, 5, 6 or valid 200GBASE-R signal	121.8.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	121.8.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	121.8.5
Extinction ratio	4 or 6	121.8.6
Transmitter transition time	Square wave or 6	121.8.7
$RIN_{21.4}OMA$	Square wave	121.8.8
Stressed receiver conformance test signal calibration	6	121.8.10.2
Stressed receiver sensitivity	3 or 5	121.8.10

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121.8.2 Wavelength and side mode suppression ratio (SMSR)

The wavelength and SMSR of each optical lane shall be within the range given in Table 121–6 if measured per IEC 61280-1-3. The lane under test is modulated using the test pattern defined in Table 121–10.

121.8.3 Average optical power

The average optical power of each lane shall be within the limits given in Table 121–6 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using the test pattern defined in Table 121–10.

121.8.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} of each lane shall be within the limits given in Table 121–6. The OMA_{outer} is measured using a test pattern specified for OMA_{outer} in Table 121–10 as the difference between the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 121–3.

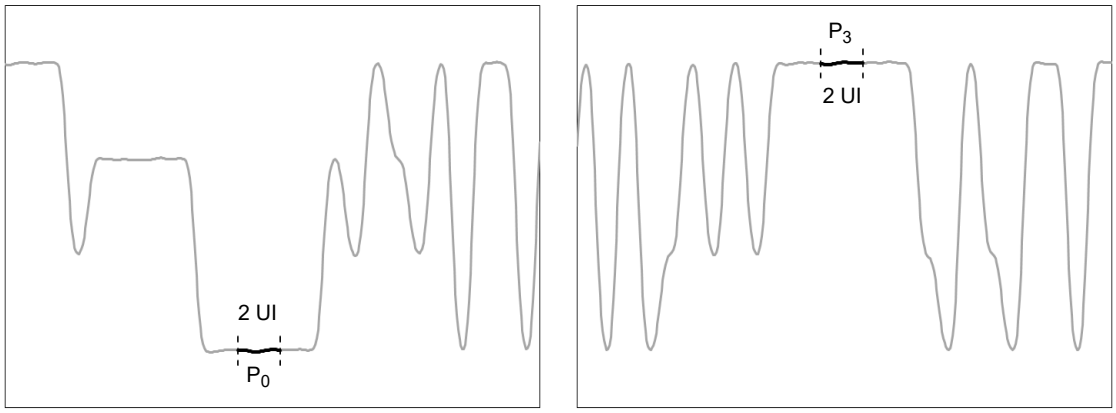

Figure 121–3—Example power levels P_0 and P_3 from PRBS13Q test pattern

121.8.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

The TDECQ and TDECQ – $10\log_{10}(C_{eq})$ of each lane shall be within the limits given in Table 121–6 if measured using the methods specified in 121.8.5.1, 121.8.5.2, and 121.8.5.3.

TDECQ is a measure of each optical transmitter's vertical eye closure when transmitted through a worst case optical channel (specified in 121.8.5.2), as measured through an optical to electrical converter (O/E) and oscilloscope with the combined frequency response given in 121.8.5.1, and equalized with the reference equalizer (as described in 121.8.5.4). The reference receiver and equalizer may be implemented in software or may be part of an oscilloscope.

Table 121–10 specifies the test patterns to be used for measurement of TDECQ.

121.8.5.1 TDECQ conformance test setup

A block diagram for the TDECQ conformance test is shown in Figure 121–4. Other equivalent measurement implementations may be used with suitable calibration.

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Each optical lane is tested individually with all other lanes in operation and all lanes using the same test pattern. There shall be at least 31 UI delay between the test pattern on one lane and the pattern on any other lane, so that the symbols on each lane are not correlated within the PMD. The optical splitter and variable reflector are adjusted so that each transmitter is tested with the optical return loss specified in Table 121–11. The state of polarization of the back reflection is adjusted to create the greatest RIN. Each optical lane is tested with the optical channel described in 121.8.5.2. The combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz, and at frequencies above 1.5 × 26.5625 GHz, the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The test pattern (specified in Table 121–10) is transmitted repetitively by the optical lane under test and the oscilloscope is set up to capture the complete pattern for TDECQ analysis as described in 121.8.5.3. The clock recovery unit (CRU) has a corner frequency of 4 MHz and a slope of 20 dB/decade. The CRU can be implemented in hardware or software depending on oscilloscope technology.

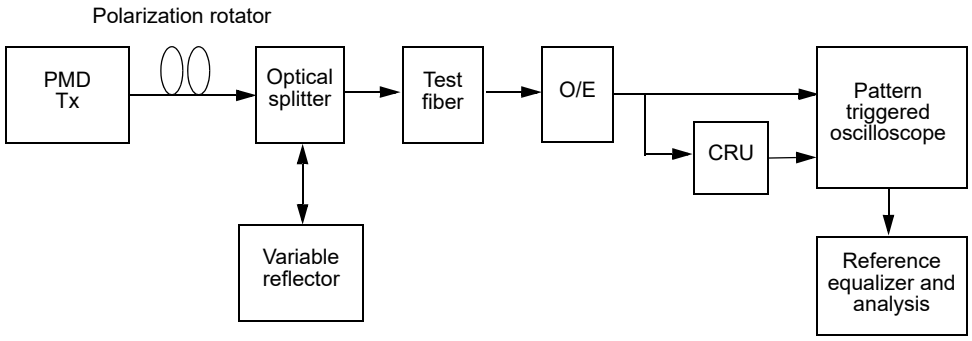

Figure 121–4—TDECQ conformance test block diagram

121.8.5.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 121–11.

Table 121–11—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]	Max mean DGD
	Minimum	Maximum			
200GBASE-DR4	$0.011625\times\lambda\times[1-(1324/\lambda)^4]$	$0.011625\times\lambda\times[1-(1300/\lambda)^4]$	Minimum	21.4 dB	0.5 ps

[a] The dispersion is measured for the wavelength of the device under test (λ in nm). The coefficient assumes 500 m for 200GBASE-DR4.
[b] There is no intent to stress the sensitivity of the O/E converter associated with the oscilloscope.
[c] The optical return loss is applied at TP2.

A 200GBASE-DR4 transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 121–11 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

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To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss specified in Table 121–11. The state of polarization of the back reflection is adjusted to create the greatest RIN.

The mean DGD of the channel is to be less than the value specified in Table 121–11.

121.8.5.3 TDECQ measurement method

The standard deviation of the noise of the O/E and oscilloscope combination, σ_S, is determined with no optical input signal and the same settings as used to capture the histograms described below.

OMA_{outer} is measured according to 121.8.4 on the equalized signal.

The test pattern specified for TDECQ (see Table 121–10) is transmitted repetitively by the optical lane under test and the oscilloscope is set up to capture samples from all symbols in the complete pattern without averaging.

If an equivalent-time sampling oscilloscope is used, the impact of the sampling process and the reference equalizer on transmitter noise has to be compensated for, so that the correct magnitude of noise is present at the output of the equalizer.

The captured waveform is processed to find the largest noise that could be combined with the signal by an ideal reference receiver when optimally equalized by a reference equalizer. The optimal equalizer tap coefficients are dependent on the amount of noise that can be added to the signal, so finding the noise that can be added and the optimal equalizer setting is an iterative process. One way of doing this, using estimated PAM4 symbol error ratio as the figure of merit for the equalized signal, is described below.

The reference equalizer (specified in 121.8.5.4) is applied to the waveform. The sum of the equalizer tap coefficients is equal to 1. An eye diagram is formed from the equalized captured waveform.

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The average optical power (P_{ave}) of the equalized eye diagram is determined, and the 0 UI and 1 UI crossing points are determined by the average of the eye diagram crossing times, as measured at P_{ave}, as illustrated in Figure 121–5.

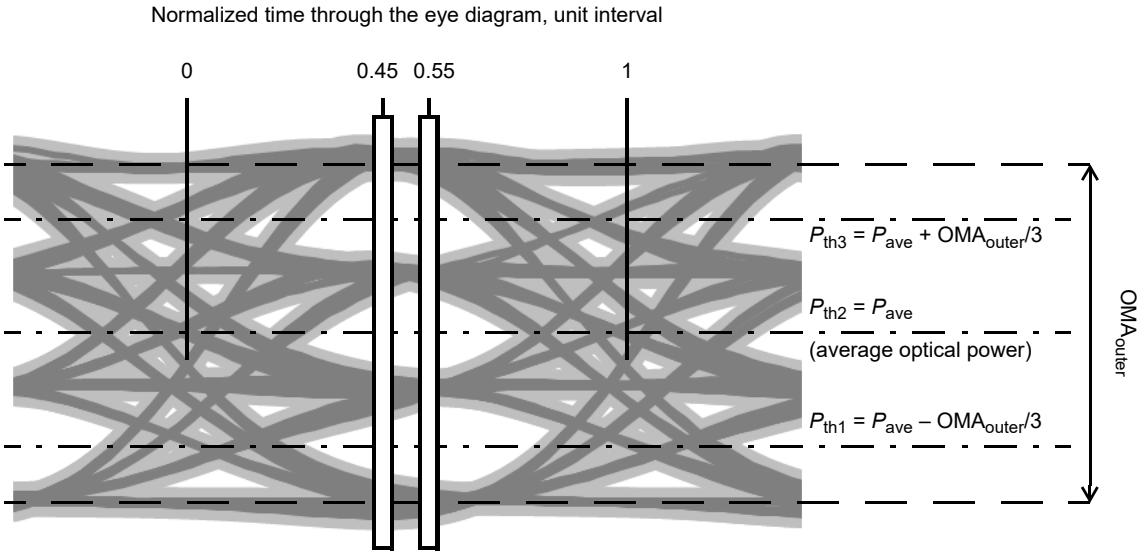

Figure 121–5—Illustration of the TDECQ measurement

Two vertical histograms are measured through the eye diagram, nominally centered at 0.45 UI and 0.55 UI. Each of the histogram windows spans all of the modulation levels of the eye diagram, as illustrated in Figure 121–5. The precise time position of the pair of histograms is adjusted to minimize TDECQ while keeping the histograms spaced 0.1 UI apart.

Each histogram window has a width of 0.04 UI. Each histogram window has outer height boundaries which are set beyond the extremes of the eye diagram (so that no further samples would be captured by increasing the vertical separation of the height boundaries).

The sub-eye threshold levels P_{th1}, P_{th2}, and P_{th3}, are determined from the OMA_{outer} and the average optical power of the eye diagram (P_{ave}) as defined in Equation (121–1), Equation (121–2), and Equation (121–3) and illustrated in Figure 121–5.

$$P_{th1} = P_{ave} - \frac{OMA_{outer}}{3} \quad (121–1)$$

$$P_{th2} = P_{ave} \quad (121–2)$$

$$P_{th3} = P_{ave} + \frac{OMA_{outer}}{3} \quad (121–3)$$

Each captured histogram is processed to, in effect, combine the PAM4 waveform with noise, in order to produce an estimate of the partial PAM4 symbol error ratio (SER) for each sub-eye. One way of doing this is described below.

The left and right histograms are each normalized, and can be represented as a series of equally spaced optical power values (y_i) with separation Δy, each with an associated fraction $F(y_i)$, equal to the number of

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samples captured in that power interval divided by the total number of samples in that histogram. The sum of all $F(y_i)$ for each histogram is equal to 1.

From the left normalized histogram $F(y_i)$, three cumulative probability functions are created, $CF_{L1}(y_i)$, $CF_{L2}(y_i)$, and $CF_{L3}(y_i)$, one around each sub-eye threshold. The right histogram is treated similarly to create three cumulative probability functions $CF_{R1}(y_i)$, $CF_{R2}(y_i)$, and $CF_{R3}(y_i)$. $CF_{L1}(y_i)$ is defined in Equation (121–4).

$$CF_{L1}(y_i) = \begin{cases} \sum_{y=P_{\text{th1}}}^{y_i} F(y) \text{ for } y_i \geq P_{\text{th1}} \\ \sum_{y=y_i}^{P_{\text{th1}}} F(y) \text{ for } y_i < P_{\text{th1}} \end{cases} \quad (121\text{–}4)$$

Each element of the cumulative probability function, $CF_{L1}(y_i)$, is multiplied by a value $G_{\text{th1}}(y_i)$, and then summed to calculate an approximation for SER_{L1}, the partial SER for threshold 1. Each element of the cumulative probability function, $CF_{L2}(y_i)$, is multiplied by a value $G_{\text{th2}}(y_i)$, and then summed to calculate an approximation for SER_{L2}. Each element of the cumulative probability function, $CF_{L3}(y_i)$, is multiplied by a value $G_{\text{th3}}(y_i)$, and then summed to calculate an approximation for SER_{L3}. The sum of the three partial SERs is the SER associated with the left histogram, SER_L.

Each element of the cumulative probability function, $CF_{R1}(y_i)$, is multiplied by a value $G_{\text{th1}}(y_i)$, and then summed to calculate an approximation for SER_{R1}, the partial SER for threshold 1. $CF_{R2}(y_i)$ and $CF_{R3}(y_i)$ are treated similarly to calculate SER_{R2}, and SER_{R3}, the partial SERs for threshold 2 and threshold 3. The sum of the three partial SERs is the SER associated with the right histogram, SER_R.

$G_{\text{th1}}(y_i)$ is equivalent to a Gaussian probability density function with an RMS value of σ_G, centered around the sub-eye threshold P_{th1}. $G_{\text{th1}}(y_i)$ is given by Equation (121–5) and can be estimated by Equation (121–6).

$$G_{\text{th1}}(y_i) = \int_{y_i-\frac{\Delta y}{2}}^{y_i+\frac{\Delta y}{2}} \frac{1}{C_{\text{eq}}\sigma_G\sqrt{2\pi}} \times \text{e}^{-\left(\frac{y-P_{\text{th1}}}{C_{\text{eq}}\sigma_G\sqrt{2}}\right)^2} dy \quad (121\text{–}5)$$

$$G_{\text{th1}}(y_i) = \frac{1}{C_{\text{eq}}\sigma_G\sqrt{2\pi}} \times \text{e}^{-\left(\frac{y_i-P_{\text{th1}}}{C_{\text{eq}}\sigma_G\sqrt{2}}\right)^2} \times \Delta y \quad (121\text{–}6)$$

$G_{\text{th2}}(y_i)$ and $G_{\text{th3}}(y_i)$ are similar Gaussian probability density functions with the same RMS value of σ_G, centered around the sub-eye thresholds P_{th2} and P_{th3} respectively. $G_{\text{th2}}(y_i)$ and $G_{\text{th3}}(y_i)$ are given by Equation (121–7) and Equation (121–8) respectively.

$$G_{\text{th2}}(y_i) = \int_{y_i-\frac{\Delta y}{2}}^{y_i+\frac{\Delta y}{2}} \frac{1}{C_{\text{eq}}\sigma_G\sqrt{2\pi}} \times \text{e}^{-\left(\frac{y-P_{\text{th2}}}{C_{\text{eq}}\sigma_G\sqrt{2}}\right)^2} dy \quad (121\text{–}7)$$

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$$G_{\text{th3}}(y_i) = \int_{y_i - \frac{\Delta y}{2}}^{y_i + \frac{\Delta y}{2}} \frac{1}{C_{\text{eq}}\sigma_G\sqrt{2\pi}} \times \text{e}^{-\left(\frac{y - P_{\text{th3}}}{C_{\text{eq}}\sigma_G\sqrt{2}}\right)^2} dy \quad (121\text{–}8)$$

where

C_{eq} is a coefficient which accounts for the reference equalizer noise enhancement

The value of C_{eq} can be calculated from the product of the normalized noise power density spectrum $N(f)$ at the input of the reference equalizer and the normalized frequency response $H_{\text{eq}}(f)$ of the reference equalizer, as shown in Equation (121–9).

$$C_{\text{eq}} = \sqrt{\int_f N(f) \times |H_{\text{eq}}(f)|^2 df} \quad (121\text{–}9)$$

where

$N(f)$ is the normalized noise power density spectrum equivalent to white noise filtered by a fourth-order Bessel-Thomson response filter with a 3 dB bandwidth of 13.28125 GHz.

and

$$\int_f N(f)df = H_{\text{eq}}(f = 0) = 1 \quad (121\text{–}10)$$

The equalizer tap coefficients are iteratively adjusted and SER_L and SER_R calculated until the largest of SER_L and SER_R is minimized. Then, if the larger of SER_L and SER_R is greater than the target SER of 4.8×10^{-4}, the value of σ_G is decreased and the process of equalizer optimization is repeated; If the larger of SER_L and SER_R is lower than the target SER of 4.8×10^{-4}, then the value of σ_G is increased and the process of equalizer optimization is repeated.

P_{th1}, P_{th2}, and P_{th3} are varied from their nominal values by up to ±1% of $\text{OMA}_{\text{outer}}$ in order to optimize TDECQ. The same three thresholds are used for both the left and the right histogram.

When the larger of SER_L and SER_R is equal to the target SER of 4.8×10^{-4}, and the value of σ_G cannot be increased by further optimization of the equalizer tap coefficients or the sub-eye threshold levels, then TDECQ is calculated.

The RMS noise, R, that could be added by a receiver is given by Equation (121–11).

$$R = \sqrt{\sigma_G{}^2 + \sigma_S{}^2} \quad (121\text{–}11)$$

TDECQ is given by Equation (121–12).

$$TDECQ = 10\log_{10}\left(\frac{OMA_{\text{outer}}}{6} \times \frac{1}{Q_t R}\right) \quad (121\text{–}12)$$

where

OMA_{outer} is the Outer Optical Modulation Amplitude as defined in 121.8.4

Q_t is 3.414 consistent with the BER and target symbol error ratio for Gray coded PAM4

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121.8.5.4 TDECQ reference equalizer

The reference equalizer for 200GBASE-DR4 is a 5-tap, T-spaced, feed-forward equalizer (FFE), where T is the symbol period. A functional model of the reference equalizer is shown in Figure 121–6. The sum of the equalizer tap coefficients is equal to 1. Tap 1, tap 2, or tap 3, has the largest magnitude tap coefficient, which is constrained to be at least 0.8.

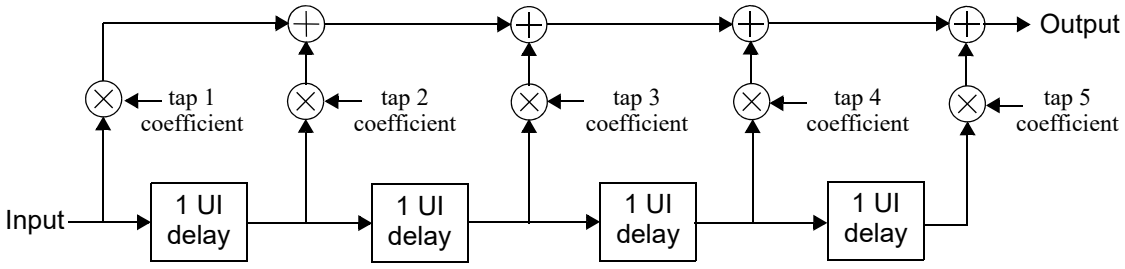

Figure 121–6—TDECQ reference equalizer functional model

NOTE—This reference equalizer is part of the TDECQ test and does not imply any particular receiver equalizer implementation.

121.8.6 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 121–6 if measured using a test pattern specified for extinction ratio in Table 121–10. The extinction ratio of a PAM4 optical signal is defined as the ratio of the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 121–3.

121.8.7 Transmitter transition time

The transmitter transition time of each lane shall be within the limits given in Table 121–6 if measured using a test pattern specified for transmitter transition time in Table 121–10.

Transmitter transition time is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer}, or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling edges respectively, as measured through an O/E converter and oscilloscope with response defined as follows. The combined response of the O/E converter and oscilloscope has a 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz. At frequencies above 1.5 × 26.5625 GHz, the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The 0% level and the 100% level are P_0 and P_3 as defined by the OMA_{outer} measurement procedure (see 121.8.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence, and the falling edge is that within the 33333000000 symbol sequence.

121.8.8 Relative intensity noise ($RIN_{21.4}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 21.4 dB.

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b) Each lane may be tested individually with the sum of the optical power from all of the lanes not under test being below –30 dBm.

c) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 26.6 GHz).

d) The test pattern is according to Table 121–10.

121.8.9 Receiver sensitivity

Receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 3.2 dB. Receiver sensitivity should meet Equation (121–13), which is illustrated in Figure 121–7.

$$RS = \max(-6.1, SECQ - 7.5) \quad \text{(dBm)} \tag{121–13}$$

where

RS is the receiver sensitivity

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

The normative requirement for receivers is stressed receiver sensitivity.

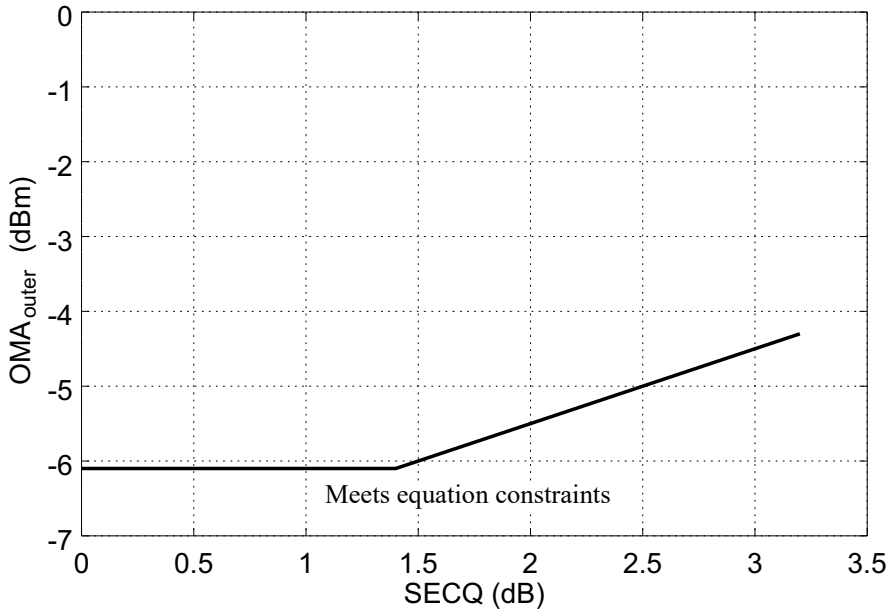

Figure 121–7—Illustration of receiver sensitivity

121.8.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 121–7 if measured using the method defined in 121.8.10.1 and 121.8.10.3, with the conformance test signal at TP3 as described in 121.8.10.2, using the test pattern specified for stressed receiver sensitivity in Table 121–10. The BER is required to be met for the lane under test on its own.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Any of the patterns specified for stressed receiver sensitivity in Table 121–10 is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal.

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121.8.10.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 121–8. The patterns used for the received conformance signal are specified in Table 121–10. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 121.8.10.2 and has sinusoidal jitter applied as specified in 121.8.10.4. A suitable test set is needed to characterize the signal used to test the receiver. Stressed receiver conformance test signal verification is described in 121.8.10.3.

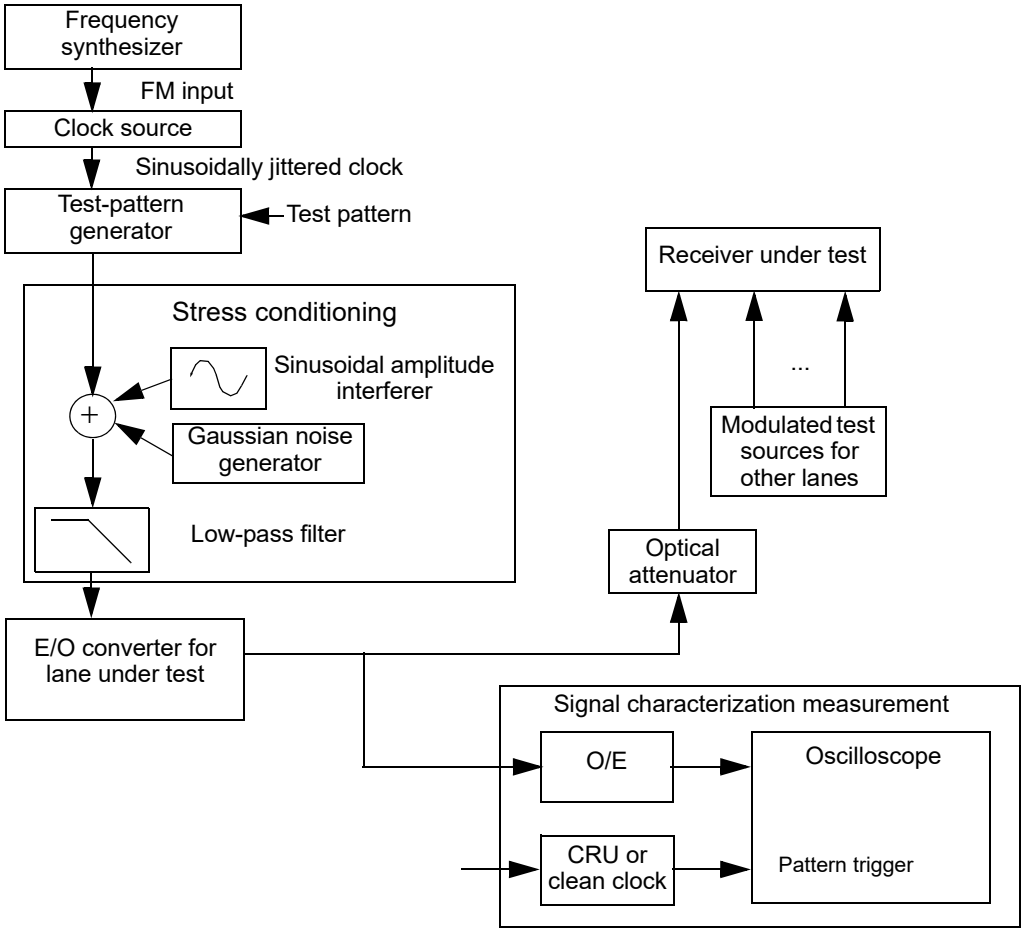

Figure 121–8—Stressed receiver conformance test block diagram

The low-pass filter is used to create ISI. The sinusoidal amplitude interferer causes additional eye closure, but in conjunction with the finite edge rates, also causes some jitter.

The sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferer may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferer, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The Gaussian noise generator, the amplitude of the sinusoidal interferer, and the low-pass filter are adjusted so that the SECQ specified in Table 121–7 is met, according to the methods specified in 121.8.10.2.

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For improved visibility for calibration, all elements in the signal path (cables, DC blocks, E/O converter, etc.) should have wide and smooth frequency response, and linear phase response, throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be negligible.

121.8.10.2 Stressed receiver conformance test signal characteristics and calibration

The conformance test signal is used to validate that each lane of the PMD receiver meets BER requirements with near worst-case waveforms at TP3.

The primary parameters of the stressed receiver conformance test signal are its stressed eye closure (SECQ), and the sinusoidal jitter applied, as specified in 121.8.10.4. The SECQ of the stressed receiver conformance test signal is measured according to 121.8.5, except that the test fiber is not used. An example stressed receiver conformance test setup is shown in Figure 121–8; however, alternative test setups that generate equivalent stress conditions may be used.

The following steps describe a possible method for setting up and calibrating a stressed receiver conformance test signal when using a stressed receiver conformance test setup as shown in Figure 121–8:

1) Set the signaling rate of the test pattern generator to meet the requirements in Table 121–6.
2) With the sinusoidal jitter, sinusoidal interferer, and the Gaussian noise generator turned off, set the extinction ratio of the E/O converter to approximately the minimum specified in Table 121–6.
3) The required value of SECQ is given in Table 121–7. Sinusoidal jitter is added as specified in Table 121–12.

When calibrating the conformance signal, the sinusoidal jitter frequency should be between 50 MHz and 10 times LB as defined in Table 121–12. Sinusoidal jitter amplitude may be calibrated by measuring the jitter on the oscilloscope, while transmitting the square wave pattern, as defined in Table 121–9, and using a clean clock in place of the CRU to trigger the oscilloscope.

Iterate the adjustments of the sinusoidal interferer, the Gaussian noise generator, and extinction ratio, until the required value of SECQ is met, while also meeting the following conditions:

— The extinction ratio is approximately the minimum specified in Table 121–6;
— The transition time of the stressed receiver conformance test signal is no greater than the value specified in Table 121–6;
— With the Gaussian noise generator on and the sinusoidal jitter and sinusoidal interferer turned off, the $RIN_{21.4}OMA$ of the conformance test signal is no greater than the value specified in Table 121–6;
— The value of SECQ − $10\log_{10}(C_{eq})$ is less than the value specified in Table 121–7; and
— Sinusoidal jitter is as specified in Table 121–12.

Each receiver lane is conformance tested in turn. The source for the lane under test is adjusted to supply a signal at the input to the receiver under test at the “Stressed receiver sensitivity (OMA_{outer}), each lane (max)” specified in Table 121–7, and the test sources for the other lanes are set to the “OMA_{outer} of each aggressor lane” specified in Table 121–7.

NOTE—A compliant PMD receiver is expected to meet the stressed receiver sensitivity requirements with a calibrated conformance test signal regardless of the proportion of the dB value of the SECQ that is due to the frequency response of the combination of the low-pass filter and the E/O converter.

121.8.10.3 Stressed receiver conformance test signal verification

The SECQ of the stressed receiver conformance test signal is measured according to 121.8.5, except that the test fiber is not used. The clock output from the clock source in Figure 121–8 is modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye jitter that includes the sinusoidal

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jitter component, a separate clock source (clean clock of Figure 121–8) is required that is synchronized to the source clock, but not modulated with the jitter source.

Care should be taken when characterizing the test signal because excessive noise/jitter in the measurement system would result in an input signal that does not fully stress the receiver under test. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. The noise/jitter introduced by the O/E, filters, and oscilloscope should be negligible or the results should be corrected for its effects. While the details of test equipment are beyond the scope of this standard, it is recommended that the implementer fully characterize the test equipment and apply appropriate guard bands so that the stressed receiver conformance input signal meets the stress and sinusoidal jitter specified in 121.8.10.2 and 121.8.10.4.

121.8.10.4 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table 121–12 and is illustrated in Figure 121–9.

Table 121–12—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter, peak-to-peak (UI)
$f < 40$ kHz	Not specified
40 kHz $< f \leq$ 4 MHz	2×10^5 Hz/ f
4 MHz $< f <$ 10 LB[a]	0.05

[a] LB = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

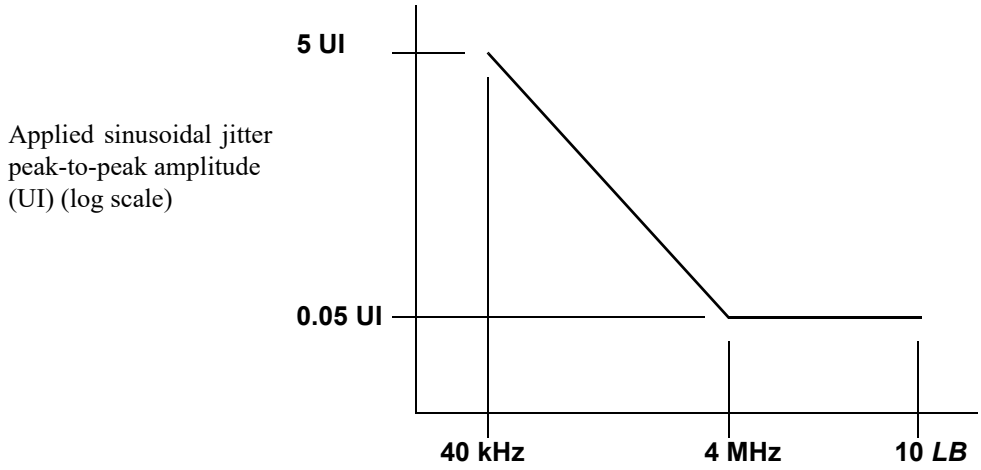

Figure 121–9—Illustration of the mask of the sinusoidal component of jitter tolerance

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121.9 Safety, installation, environment, and labeling

121.9.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1.

121.9.2 Laser safety

200GBASE-DR4 optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[208]

121.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

121.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 200GBASE-DR4 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

121.9.5 Electromagnetic emission

A system integrating a 200GBASE-DR4 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

121.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

[208] A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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121.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 200GBASE-DR4).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 121.9.2.

121.10 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 121–10.

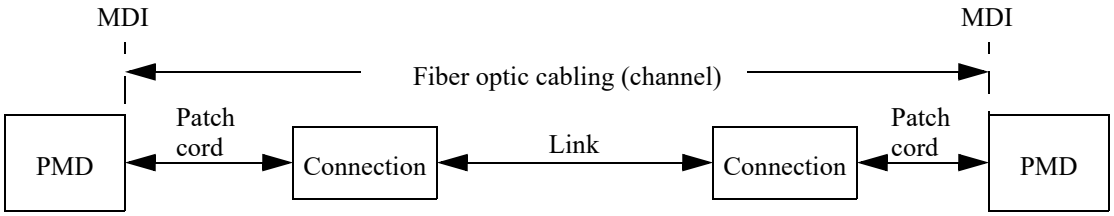

Figure 121–10—Fiber optic cabling model

The channel insertion loss is given in Table 121–13. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 121–13—Fiber optic cabling (channel) characteristics

Description	200GBASE-DR4	Unit
Operating distance (max)	500	m
Channel insertion loss[a, b](max)	3	dB
Channel insertion loss (min)	0	dB
Positive dispersion[b] (max)	0.8	ps/nm
Negative dispersion[b] (min)	–0.93	ps/nm
DGD_max[c]	2.24	ps
Optical return loss (min)	37	dB

[a] These channel insertion loss values include cable, connectors, and splices.
[b] Over the wavelength range 1304.5 nm to 1317.5 nm.
[c] Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

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121.11 Characteristics of the fiber optic cabling (channel)

The 200GBASE-DR4 fiber optic cabling shall meet the specifications defined in Table 121–14. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

121.11.1 Optical fiber cable

The fiber optic cable requirements are satisfied by cables containing IEC 60793-2-50 type B1.1 (dispersion un-shifted single-mode), type B1.3 (low water peak single-mode), or type B6_a (bend insensitive) fibers or the requirements in Table 121–14 where they differ.

Table 121–14—Optical fiber and cable characteristics

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.5[a]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \leq \lambda_0 \leq 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a] The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3.

121.11.2 Optical fiber connection

An optical fiber connection, as shown in Figure 121–10, consists of a mated pair of optical connectors.

121.11.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 2.75 dB total connection and splice loss. For example, this allocation supports five connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 121–13 are met.

121.11.2.2 Maximum discrete reflectance

The maximum value for each discrete reflectance shall be less than or equal to the value shown in Table 121–15 corresponding to the number of discrete reflectances above –55 dB within the channel. For numbers of discrete reflectances in between two numbers shown in the table, the lower of the two corresponding maximum discrete reflectance values applies.

121.11.3 Medium Dependent Interface (MDI)

The 200GBASE-DR4 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the “fiber optic cabling” (as shown in Figure 121–10). The 200GBASE-DR4 PMD is coupled to the fiber optic cabling through one connector plug into the MDI optical receptacle as shown in Figure 121–12. Example constructions of the MDI include the following:

a) PMD with a connectorized fiber pigtail plugged into an adapter
b) PMD receptacle

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Table 121–15—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance
1	–37 dB
2	–42 dB
4	–45 dB
6	–47 dB
8	–48 dB
10	–49 dB

121.11.3.1 Optical lane assignments

The four transmit and four receive optical lanes of 200GBASE-DR4 shall occupy the positions depicted in Figure 121–11 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains eight active lanes within twelve total positions. The transmit optical lanes occupy the left-most four positions. The receive optical lanes occupy the right-most four positions. The four center positions are unused.

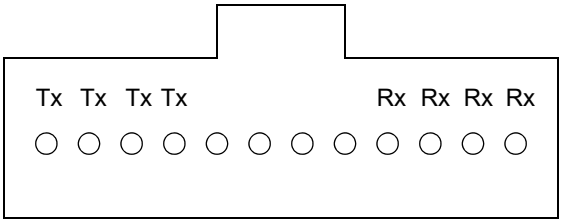

Figure 121–11—200GBASE-DR4 optical lane assignments

121.11.3.2 Medium Dependent Interface (MDI) requirements

The MDI shall meet the dimensional specifications of IEC 61754-7-1 interface 7-1-9: *MPO device receptacle, angled interface*. The plug terminating the optical fiber cabling shall meet the dimensional specifications of IEC 61754-7-1 interface 7-1-1: *MPO female plug connector, down-angled interface for 2 to 12 fibres*. The MDI shall optically mate with the plug on the optical fiber cabling. Figure 121–12 shows an MPO female plug connector with down-angled interface, and an MDI as an active device receptacle with angled interface.

The MDI shall meet the interface performance specifications of IEC 61753-021-2 for performance level D/2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 121.5.1, not at the MDI.

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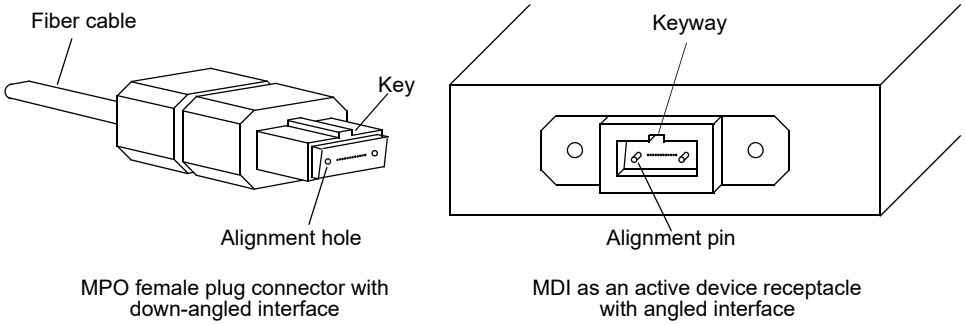

Figure 121–12—MPO female plug with down-angled interface and MDI active device receptacle with angled interface

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121.12 Protocol implementation conformance statement (PICS) proforma for Clause 121, Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-DR4[209]

121.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 121, Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-DR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

121.12.2 Identification

121.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

121.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 121, Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-DR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[209] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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121.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*INS	Installation / cable	121.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	121.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	121.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	121.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	121.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	121.4	Registers and interface supported	O	Yes [ ] No [ ]

121.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-DR4

121.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 200GBASE-R PCS and PMA	121.1		M	Yes [ ]
F2	Integration with management functions	121.1		O	Yes [ ] No [ ]
F3	Bit error ratio	121.1.1	Meets the BER specified in 121.1.1	M	Yes [ ]
F4	Transmit function	121.5.2	Conveys symbols from PMD service interface to MDI	M	Yes [ ]
F5	Mapping between optical signal and logical signal for transmitter	121.5.2	Highest optical power corresponds to tx_symbol = three	M	Yes [ ]
F6	Receive function	121.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]
F7	Conversion of four optical signals to four electrical signals	121.5.3	For delivery to the PMD service interface	M	Yes [ ]
F8	Mapping between optical signal and logical signal for receiver	121.5.3	Highest optical power corresponds to rx_symbol = three	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F9	Global Signal Detect function	121.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F10	Global Signal Detect behavior	121.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all four lanes	M	Yes [ ]
F11	Lane-by-lane Signal Detect function	121.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 121–4	MD:O	Yes [ ] No [ ] N/A [ ]
F12	PMD reset function	121.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

121.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	121.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	121.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD lane-by-lane transmit disable function	121.5.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_*i* variable	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD_fault function	121.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_transmit_fault function	121.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
M6	PMD_receive_fault function	121.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

121.12.4.3 PMD to MDI optical specifications for 200GBASE-DR4

Item	Feature	Subclause	Value/Comment	Status	Support
DR1	Transmitter meets specifications in Table 121–6	121.7.1	Per definitions in 121.8	M	Yes [ ]
DR2	Receiver meets specifications in Table 121–7	121.7.2	Per definitions in 121.8	M	Yes [ ]

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121.12.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	121.8	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and SMSR	121.8.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	121.8.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA measurements	121.8.4	Each lane	M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	121.8.5	Each lane	M	Yes [ ]
OM6	Extinction ratio	121.8.6	Each lane	M	Yes [ ]
OM7	Transmitter transition time	121.8.7	Each lane	M	Yes [ ]
OM8	Stressed receiver sensitivity	121.8.10	Each lane	M	Yes [ ]

121.12.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	121.9.1	Conforms to IEC 60950-1	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	121.9.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	121.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

121.12.4.6 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	121.11	Meets requirements specified in Table 121–13	INS:M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	121.11.2.2	Meets requirements specified in Table 121–15	INS:M	Yes [ ] N/A [ ]
OC3	MDI layout	121.11.3.1	Optical lane assignments per Figure 121–11	M	Yes [ ]
OC4	MDI dimensions	121.11.3.2	Per IEC 61754-7-1 interface 7-1-9	M	Yes [ ]
OC5	Cabling connector dimensions	121.11.3.2	Per IEC 61754-7-1 interface 7-1-1	INS:M	Yes [ ] N/A [ ]
OC6	MDI mating	121.11.3.2	MDI optically mates with plug on the cabling	M	Yes [ ]

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122. Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8

122.1 Overview

This clause specifies the 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 PMDs together with the single-mode fiber medium. The optical signals generated by these six PMD types are modulated using a 4-level pulse amplitude modulation (PAM4) format. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 122–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 122–1—Physical Layer clauses associated with the 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 PMDs

Associated clause	200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4	400GBASE-FR8, 400GBASE-LR8, 400GBASE-ER8
117—RS	Required	Required
117—200GMII[a]	Optional	Not applicable
117—400GMII[a]	Not applicable	Optional
118—200GMII Extender	Optional	Not applicable
118—400GMII Extender	Not applicable	Optional
119—PCS for 200GBASE-R	Required	Not applicable
119—PCS for 400GBASE-R	Not applicable	Required
120—PMA for 200GBASE-R	Required	Not applicable
120—PMA for 400GBASE-R	Not applicable	Required
120B—Chip-to-chip 200GAUI-8	Optional	Not applicable
120B—Chip-to-chip 400GAUI-16	Not applicable	Optional
120C—Chip-to-module 200GAUI-8	Optional	Not applicable
120C—Chip-to-module 400GAUI-16	Not applicable	Optional
120D—Chip-to-chip 200GAUI-4	Optional	Not applicable
120D—Chip-to-chip 400GAUI-8	Not applicable	Optional
120E—Chip-to-module 200GAUI-4	Optional	Not applicable
120E—Chip-to-module 400GAUI-8	Not applicable	Optional
78—Energy Efficient Ethernet	Optional	Optional

[a] 200GMII and 400GMII are optional interfaces. However, if the appropriate interface is not implemented, a conforming implementation behaves functionally as though the RS and 200GMII or 400GMII were present.

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Figure 122–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 200 Gb/s and 400 Gb/s Ethernet are introduced in Clause 116 and the purpose of each PHY sublayer is summarized in 116.2.

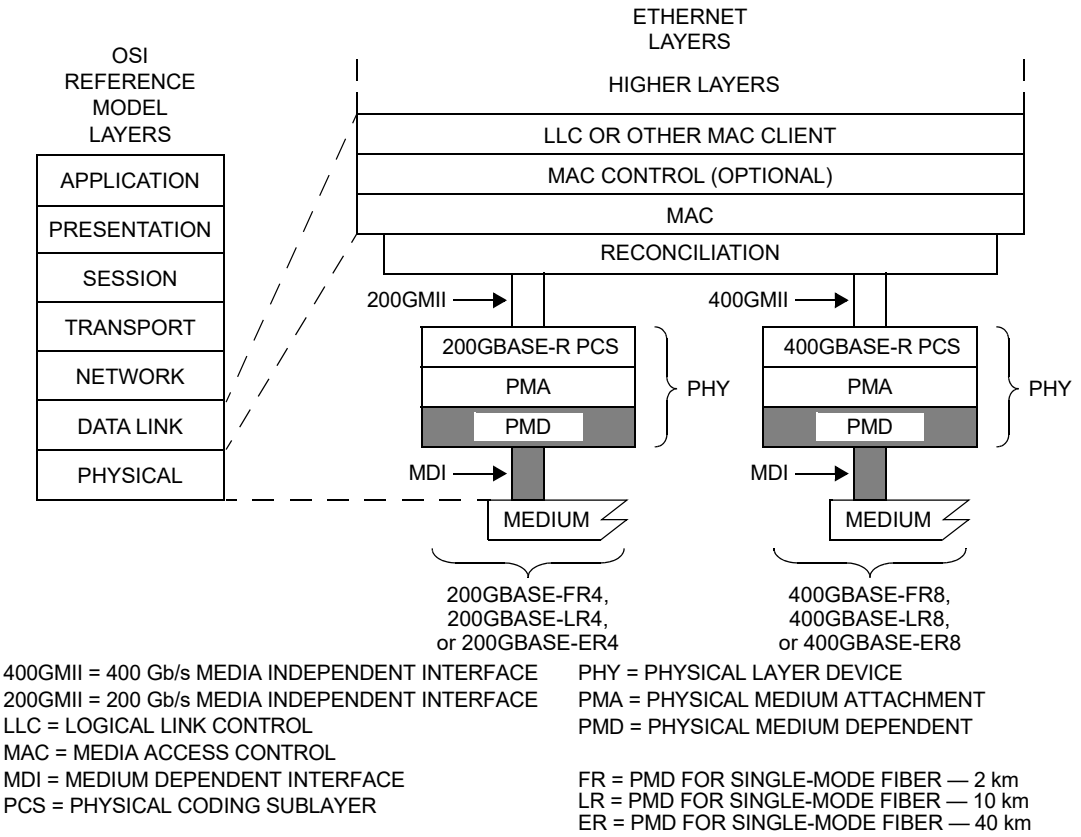

Figure 122–1—200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 use four lanes, while 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 use eight lanes. In this clause, where there are four or eight items (depending on PMD type) such as lanes, the items are numbered from 0 to $n - 1$, and an example item is numbered i. Thus n is 4 or 8.

200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

122.1.1 Bit error ratio

The bit error ratio (BER) when processed according to Clause 120 shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when processed according to Clause 120 and then Clause 119. For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

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If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap.

122.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 116.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 PMDs have four parallel symbol streams, in which case $i = 0$ to 3, and the 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 PMDs have eight parallel symbol streams, in which case $i = 0$ to 7.

In the transmit direction, the PMA continuously sends n parallel symbol streams to the PMD, one per lane, each at a nominal signaling rate of 26.5625 GBd. The PMD then converts these streams of data units into the appropriate signals on the MDI.

In the receive direction, the PMD continuously sends n parallel symbol streams to the PMA corresponding to the signals received from the MDI, one per lane, each at a nominal signaling rate of 26.5625 GBd.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication(SIGNAL_OK) inter-sublayer service interface primitive defined in 116.3.

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 122.1.1.

122.3 Delay and Skew

122.3.1 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the 200GBASE-FR4, 200GBASE-LR4, or 200GBASE-ER4 PMD including 2 m of fiber in one direction shall be no more than 4096 bit times (8 pause_quanta or 20.48 ns). The sum of the transmit and receive delays at one end of the link contributed by the 400GBASE-FR8, 400GBASE-LR8, or 400GBASE-ER8 PMD including 2 m of fiber in one direction shall be no more than 8192 bit times (16 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 116.4 and its references.

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122.3.2 Skew constraints

The Skew (relative delay between the lanes) and Skew Variation are kept within limits so that the information on the lanes can be reassembled by the PCS. Skew and Skew Variation are defined in 116.5 and specified at the points SP1 to SP6 shown in Figure 116–4 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 116.5. The measurements of Skew and Skew Variation are defined in 87.8.2.

122.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 122–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 122–3.

Table 122–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable *n*–1 to PMD transmit disable 0	PMD transmit disable register	1.9.8 to 1.9.1	PMD_transmit_disable_*n*–1 to PMD_transmit_disable_0

122.5 PMD functional specifications

The 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

122.5.1 PMD block diagram

The PMD block diagram is shown in Figure 122–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 122.8 are made at TP2. The optical receive signal is defined at

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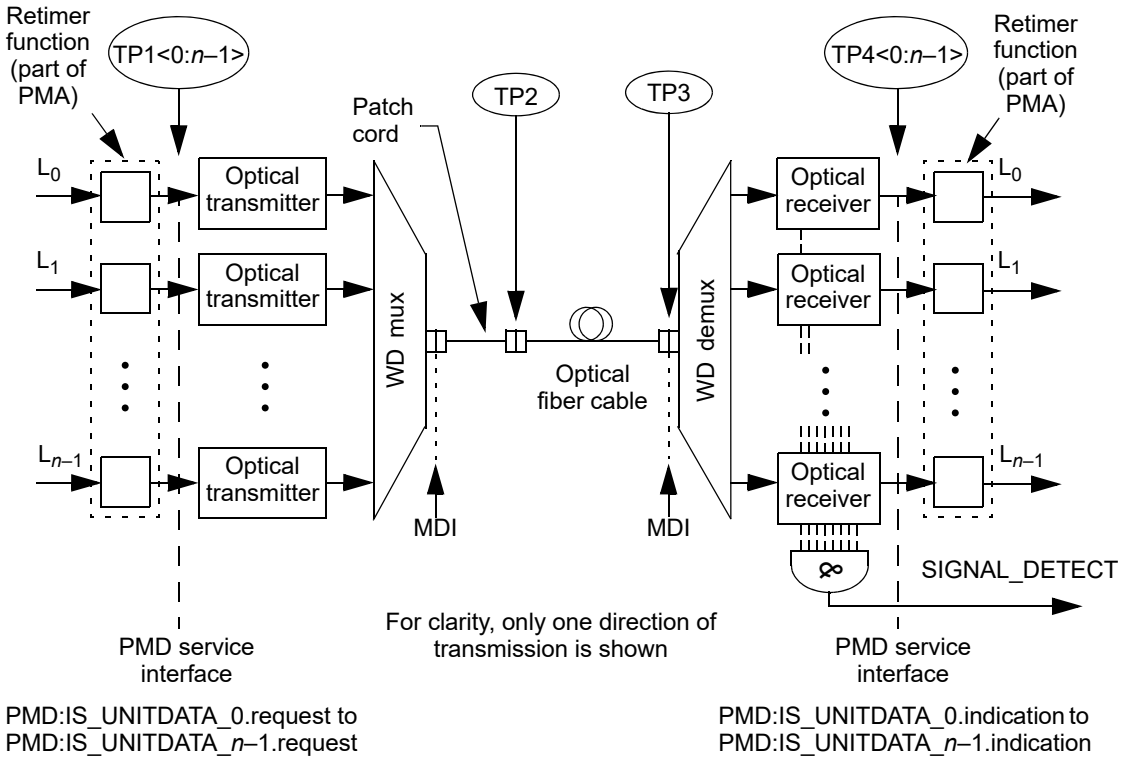
Table 122–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect *n*–1 to PMD receive signal detect 0	PMD receive signal detect register	1.10.8 to 1.10.1	PMD_signal_detect_*n*–1 to PMD_signal_detect_0

the output of the fiber optic cabling (TP3) at the MDI (see 122.11.3). Unless specified otherwise, all receiver measurements and tests defined in 122.8 are made at TP3.



NOTE—Specification of the retimer function and the electrical implementation of the PMD service interface is beyond the scope of this standard.

Figure 122–2—Block diagram for 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 transmit/receive paths

TP1<0:*n*–1> and TP4<0:*n*–1> are optional reference points that may be useful to implementers for testing components (these test points will not typically be accessible in an implemented system).

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122.5.2 PMD transmit function

The PMD Transmit function shall convert the *n* symbol streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_*n*–1.request into *n* separate optical signals. The *n* optical signals shall then be wavelength division multiplexed and delivered to the MDI, all according to the transmit optical specifications in this clause. The highest optical power level in each signal shall correspond to tx_symbol = three and the lowest shall correspond to tx_symbol = zero.

122.5.3 PMD receive function

The PMD Receive function shall demultiplex the composite optical signal received from the MDI into *n* separate optical signals. The *n* optical signals shall then be converted into *n* symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_*n*–1.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to rx_symbol = three and the lowest shall correspond to rx_symbol = zero.

122.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 116.3.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all *n* lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 122–4. The PMD receiver is not required to verify whether a compliant 200GBASE-R or 400GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 122–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –30 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ average receive power, each lane (min) in Table 122–11 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 or Table 122–12 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8) AND (compliant 200GBASE-R or 400GBASE–R signal input)]	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the

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modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

122.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:*n*–1, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 122–4.

122.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

122.5.7 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 122–9 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and Table 122–10 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter in each lane.

122.5.8 PMD lane-by-lane transmit disable function

The PMD lane-by-lane transmit disable function allows the optical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:3 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and 0:7 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 122–9 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and Table 122–10 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8.

b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the optical transmitter in each lane.

If the PMD lane-by-lane transmit disable function is not implemented in MDIO, an alternative method shall be provided to independently disable each transmit lane for testing purposes.

122.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

122.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to one.

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If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

122.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

122.6 Wavelength-division-multiplexed lane assignments

The wavelength range for each lane of the 200GBASE-FR4 PMD is defined in Table 122–5. The 200GBASE-FR4 center wavelengths are members of the CWDM wavelength grid defined in ITU-T G.694.2 and are spaced at 20 nm.

The wavelength range for each lane of the 200GBASE-LR4 and 200GBASE-ER4 PMDs is defined in Table 122–6. The wavelength range for each lane of the 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 PMDs is defined in Table 122–7. The 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 center frequencies are members of the frequency grid for 100 GHz spacing and above defined in ITU-T G.694.1 and are spaced at multiples of 800 GHz.

Table 122–5—200GBASE-FR4 wavelength-division-multiplexed lane assignments

Lane	Center wavelength	Wavelength range
L_0	1271 nm	1264.5 to 1277.5 nm
L_1	1291 nm	1284.5 to 1297.5 nm
L_2	1311 nm	1304.5 to 1317.5 nm
L_3	1331 nm	1324.5 to 1337.5 nm

Table 122–6—200GBASE-LR4 and 200GBASE-ER4 wavelength-division-multiplexed lane assignments

Lane	Center frequency	Center wavelength	Wavelength range
L_0	231.4 THz	1295.56 nm	1294.53 to 1296.59 nm
L_1	230.6 THz	1300.05 nm	1299.02 to 1301.09 nm
L_2	229.8 THz	1304.58 nm	1303.54 to 1305.63 nm
L_3	229 THz	1309.14 nm	1308.09 to 1310.19 nm

NOTE—There is no requirement to associate a particular electrical lane with a particular optical lane, as the PCS is capable of receiving lanes in any arrangement.

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Table 122–7—400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 wavelength-division-multiplexed lane assignments

Lane	Center frequency	Center wavelength	Wavelength range
L_0	235.4 THz	1273.54 nm	1272.55 to 1274.54 nm
L_1	234.6 THz	1277.89 nm	1276.89 to 1278.89 nm
L_2	233.8 THz	1282.26 nm	1281.25 to 1283.27 nm
L_3	233 THz	1286.66 nm	1285.65 to 1287.68 nm
L_4	231.4 THz	1295.56 nm	1294.53 to 1296.59 nm
L_5	230.6 THz	1300.05 nm	1299.02 to 1301.09 nm
L_6	229.8 THz	1304.58 nm	1303.54 to 1305.63 nm
L_7	229 THz	1309.14 nm	1308.09 to 1310.19 nm

122.7 PMD to MDI optical specifications for 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8

The operating ranges for the 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 PMDs are defined in Table 122–8. A 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, or 400GBASE-ER8 compliant PMD operates on type B1.1, B1.3, or B6_a single-mode fibers according to the specifications defined in Table 122–18. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 400GBASE-FR8 PMD operating at 2.5 km meets the operating range requirement of 2 m to 2 km).

The 200GBASE-ER4 PMD interoperates with the 200GBASE-LR4 PMD provided that the channel requirements defined in 122.12 are met.

The 400GBASE-LR8 PMD interoperates with the 400GBASE-FR8 PMD provided that the channel requirements for 400GBASE-FR8 are met.

The 400GBASE-ER8 PMD interoperates with the 400GBASE-FR8 PMD provided that the channel requirements defined in 122.13 are met.

The 400GBASE-ER8 PMD interoperates with the 400GBASE-LR8 PMD provided that the channel requirements defined in 122.14 are met.

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Table 122–8—200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 operating ranges

PMD type	Required operating range
200GBASE-FR4 and 400GBASE-FR8	2 m to 2 km
200GBASE-LR4 and 400GBASE-LR8	2 m to 10 km
200GBASE-ER4 and 400GBASE-ER8	2 m to 30 km
	2 m to 40 km[a]

[a] Links longer than 30 km for the same link power budget are considered engineered links. Attenuation for such links needs to be less than the worst case specified for IEC 60793-2-50 type B1.1, type B1.3, or type B6_a single-mode fiber.

122.7.1 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 transmitter optical specifications

The 200GBASE-FR4 transmitter shall meet the specifications defined in Table 122–9 per the definitions in 122.8. The 200GBASE-LR4 transmitter shall meet the specifications defined in Table 122–9 per the definitions in 122.8. The 200GBASE-ER4 transmitter shall meet the specifications defined in Table 122–9 per the definitions in 122.8. The 400GBASE-FR8 transmitter shall meet the specifications defined in Table 122–10 per the definitions in 122.8. The 400GBASE-LR8 transmitter shall meet the specifications defined in Table 122–10 per the definitions in 122.8. The 400GBASE-ER8 transmitter shall meet the specifications defined in Table 122–10 per the definitions in 122.8.

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Table 122–9—200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 transmit characteristics

Description	200GBASE-FR4	200GBASE-LR4	200GBASE-ER4	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm			GBd
Modulation format	PAM4			—
Lane wavelengths (range)	1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5	1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19		nm
Side-mode suppression ratio (SMSR), (min)	30			dB
Total average launch power (max)	10.7	11.3	12.6	dBm
Average launch power, each lane (max)	4.7	5.3	6.6	dBm
Average launch power, each lane[a] (min)	–4.2	–3.4	0.4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	4.5	5.1	7.4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)[b]	–1.2	–0.4	3.4	dBm
Difference in launch power between any two lanes (OMA_{outer}) (max)	4			dB
Launch power in OMA_{outer} minus TDECQ, each lane (min): for extinction ratio ≥ 4.5 dB for extinction ratio < 4.5 dB	 –2.6 –2.5	 –1.8 –1.7	 2 —	 dBm dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	3.1	3.2	3.2	dB
TDECQ $-10\log_{10}(C_{eq})$[c] (max)	3.1	3.2	3.2	dB
Average launch power of OFF transmitter, each lane (max)	–30			dBm
Extinction ratio, each lane (min)	3.5		6	dB
Transmitter transition time (max)	34			ps
$RIN_{17.1}OMA$ (max)	–132	—	—	dB/Hz
$RIN_{15.6}OMA$ (max)	—	–132	—	dB/Hz
$RIN_{15}OMA$ (max)	—	—	–132	dB/Hz
Optical return loss tolerance (max)	17.1	15.6	15	dB
Transmitter reflectance[d] (max)	–26			dB

[a] Average launch power, each lane (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b] Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMA_{outer} (min) has to exceed this value.
[c] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[d] Transmitter reflectance is defined looking into the transmitter.

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Table 122–10—400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 transmit characteristics

Description	400GBASE-FR8	400GBASE-LR8	400GBASE-ER8	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm			GBd
Modulation format	PAM4			—
Lane wavelengths (range)	1272.55 to 1274.54 1276.89 to 1278.89 1281.25 to 1283.27 1285.65 to 1287.68 1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19			nm
Side-mode suppression ratio (SMSR), (min)	30			dB
Total average launch power (max)	13.2		14.6	dBm
Average launch power, each lane[a] (max)	5.3		5.6	dBm
Average launch power, each lane[b] (min)	–3.5	–2.8	–0.6	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	5.5	5.7	6.4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)[c]	–0.5	0.2	2.4	dBm
Difference in launch power between any two lanes (OMA_{outer}) (max)	4			dB
Launch power in OMA_{outer} minus TDECQ, each lane (min): for extinction ratio ≥ 4.5 dB for extinction ratio < 4.5 dB	 –1.9 –1.8	 –1.2 –1.1	 1 —	 dBm dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	2.9	3.1	3.4	dB
TDECQ $-10\log_{10}(C_{eq})$[d] (max)	2.9	3.1	3.4	dB
Average launch power of OFF transmitter, each lane (max)	–30			dBm
Extinction ratio, each lane (min)	3.5		6	dB
Transmitter transition time (max)	34			ps
$RIN_{17.1}OMA$ (max)	–132	—	—	dB/Hz
$RIN_{15.6}OMA$ (max)	—	–132	—	dB/Hz
$RIN_{15}OMA$ (max)	—	—	–132	dB/Hz
Optical return loss tolerance (max)	17.1	15.6	15	dB
Transmitter reflectance[e] (max)	–26			dB

[a] As the total average launch power limit has to be met, not all of the lanes can operate at the maximum average launch power, each lane.
[b] Average launch power, each lane (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMA_{outer} (min) has to exceed this value.
[d] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[e] Transmitter reflectance is defined looking into the transmitter.

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122.7.2 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 receive optical specifications

The 200GBASE-FR4 receiver shall meet the specifications defined in Table 122–11 per the definitions in 122.8. The 200GBASE-LR4 receiver shall meet the specifications defined in Table 122–11 per the definitions in 122.8. The 200GBASE-ER4 receiver shall meet the specifications defined in Table 122–11 per the definitions in 122.8. The 400GBASE-FR8 receiver shall meet the specifications defined in Table 122–12 per the definitions in 122.8. The 400GBASE-LR8 receiver shall meet the specifications defined in Table 122–12 per the definitions in 122.8. The 400GBASE-ER8 receiver shall meet the specifications defined in Table 122–12 per the definitions in 122.8.

Table 122–11—200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 receive characteristics

Description	200GBASE-FR4	200GBASE-LR4	200GBASE-ER4	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm			GBd
Modulation format	PAM4			—
Lane wavelengths (range)	1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5	1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19		nm
Damage threshold[a], each lane	5.7	6.3	–2.4	dBm
Average receive power, each lane (max)	4.7	5.3	–3.4	dBm
Average receive power, each lane[b] (min)	–8.2	–9.7	–17.6	dBm
Receive power (OMA_{outer}), each lane (max)	4.5	5.1	–2.6	dBm
Difference in receive power between any two lanes (OMA_{outer}) (max)	4.1	4.2	4.6	dB
Receiver reflectance (max)	–26			dB
Receiver sensitivity (OMA_{outer}), each lane[c] (max)	Equation (122–1)	Equation (122–2)	Equation (122–3)	dBm
Stressed receiver sensitivity (OMA_{outer}), each lane[d] (max)	–3.8	–5.4	–13.3	dBm
Conditions of stressed receiver sensitivity test:[e]				
Stressed eye closure for PAM4 (SECQ), lane under test	3.1	3.2	3.2	dB
SECQ – $10\log_{10}(C_{eq})$[f] (max), lane under test	3.1	3.2	3.2	dB
OMA_{outer} of each aggressor lane	0.3	–1.2	–8.7	dBm

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
[b] Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] Receiver sensitivity (OMA_{outer}), each lane (max) is optional and is defined for a transmitter with a value of SECQ up to 3.1 dB for 200GBASE-FR4, 3.2 dB for 200GBASE-LR4, and 3.2 dB for 200GBASE-ER4.
[d] Measured with conformance test signal at TP3 (see 122.8.10) for the BER specified in 122.1.1.
[e] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

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Table 122–12—400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 receive characteristics

Description	400GBASE-FR8	400GBASE-LR8	400GBASE-ER8	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm			GBd
Modulation format	PAM4			—
Lane wavelengths (range)	1272.55 to 1274.54 1276.89 to 1278.89 1281.25 to 1283.27 1285.65 to 1287.68 1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19			nm
Damage threshold[a], each lane	6.3		–3.4	dBm
Average receive power, each lane (max)	5.3		–4.4	dBm
Average receive power, each lane[b] (min)	–7.5	–9.1	–18.6	dBm
Receive power (OMA_{outer}), each lane (max)	5.7		–3.6	dBm
Difference in receive power between any two lanes (OMA_{outer}) (max)	4.1	4.5	5.8	dB
Receiver reflectance (max)	–26			dB
Receiver sensitivity (OMA_{outer}), each lane[c] (max)	Equation (122–4)	Equation (122–5)	Equation (122–6)	dBm
Stressed receiver sensitivity (OMA_{outer}), each lane[d] (max)	–3.3	–4.9	–14.1	dBm
Conditions of stressed receiver sensitivity test:[e]				
Stressed eye closure for PAM4 (SECQ), lane under test	2.9	3.1	3.4	dB
SECQ – $10\log_{10}(C_{eq})$[f] (max), lane under test	2.9	3.1	3.4	dB
OMA_{outer} of each aggressor lane	0.8	–0.4	–8.3	dBm

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
[b] Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] Receiver sensitivity (OMA_{outer}), each lane (max) is optional and is defined for a transmitter with a value of SECQ up to 2.9 dB for 400GBASE-FR8, 3.1 dB for 400GBASE-LR8, and 3.4 dB for 400GBASE-ER8.
[d] Measured with conformance test signal at TP3 (see 122.8.10) for the BER specified in 122.1.1.
[e] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

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122.7.3 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 illustrative link power budgets

Illustrative power budgets and penalties for 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 channels are shown in Table 122–13.

Table 122–13—200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 illustrative link power budgets

Parameter	200GBASE-FR4	400GBASE-FR8	200GBASE-LR4	400GBASE-LR8	200GBASE-ER4		400GBASE-ER8		Unit
Power budget (for maximum TDECQ): for extinction ratio ≥ 4.5 dB for extinction ratio < 4.5 dB	7.4 7.5	7.2 7.3	10 10.1	9.9 10	21.7 —		21.9 —		dB dB
Operating distance	2		10		30	40[a]	30	40[a]	km
Channel insertion loss (max)	4[b]		6.3		15	18	15	18	dB
Channel insertion loss (min)	0				10		10		dB
Maximum discrete reflectance	See 122.11.2.2								dB
Allocation for penalties[c] (for maximum TDECQ): for extinction ratio ≥ 4.5 dB for extinction ratio < 4.5 dB	3.4 3.5	3.2 3.3	3.7 3.8	3.6 3.7	3.7 —		3.9 —		dB dB
Additional insertion loss allowed	0		0		3	0	3	0	dB

[a] Links longer than 30 km are considered engineered links. Attenuation for such links needs to be less than the worst case for cables containing IEC 60793-2-50 type B1.1, type B1.3, or type B6_a single-mode cabled optical fiber.

[b] The channel insertion loss is calculated using the maximum distance specified in Table 122–8 for 200GBASE-FR4 and 400GBASE-FR8 and fiber attenuation of 0.5 dB/km plus an allocation for connection and splice loss given in 122.11.2.1.

[c] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

122.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

122.8.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 122–15 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 122–15 may be used to perform that test. The test patterns used in this clause are shown in Table 122–14.

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Table 122–14—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle	119.2.4.9
6	SSPRQ	120.5.11.2.3

Table 122–15—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 200GBASE-R or 400GBASE-R signal	122.8.2
Side mode suppression ratio	3, 5, 6 or valid 200GBASE-R or 400GBASE-R signal	122.8.2
Average optical power	3, 5, 6 or valid 200GBASE-R or 400GBASE-R signal	122.8.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	122.8.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	122.8.5
Extinction ratio	4 or 6	122.8.6
Transmitter transition time	Square wave or 6	122.8.7
$RIN_{17.1}OMA$, $RIN_{15.6}OMA$, and $RIN_{15}OMA$	Square wave	122.8.8
Stressed receiver conformance test signal calibration	6	122.8.10.2
Stressed receiver sensitivity	3 or 5	122.8.10

122.8.2 Wavelength and side mode suppression ratio (SMSR)

The wavelength and SMSR of each optical lane shall be within the ranges given in Table 122–5 for 200GBASE-FR4, in Table 122–6 for 200GBASE-LR4 and 200GBASE-ER4 and in Table 122–7 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8, if measured per IEC 61280-1-3. The lane under test is modulated using the test pattern defined in Table 122–15.

122.8.3 Average optical power

The average optical power of each lane shall be within the limits given in Table 122–9 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and in Table 122–10 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 if measured using the methods given in IEC 61280-1-1, with the sum of the optical power from all of the lanes not under test below –30 dBm, per the test setup in Figure 53–6.

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122.8.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} of each lane shall be within the limits given in Table 122–9 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and in Table 122–10 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8. The OMA_{outer} is measured using a test pattern specified for OMA_{outer} in Table 122–15. It is the difference between the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 122–3. For this measurement the sum of the optical power from all of the lanes not under test is below –30 dBm, or if other lanes are operating, a suitable optical filter may be used to separate the lane under test.

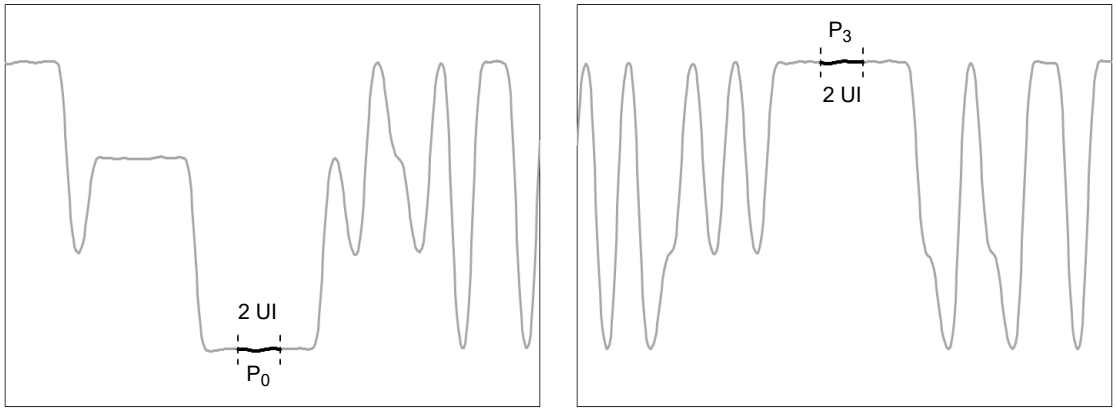

Figure 122–3—Power levels P_0 and P_3 from PRBS13Q test pattern

122.8.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

The TDECQ and TDECQ – $10\log_{10}(C_{eq})$ of each lane shall be within the limits given in Table 122–9 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and in Table 122–10 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 if measured using the methods specified in 122.8.5.1, 122.8.5.2, and 122.8.5.3.

TDECQ is a measure of each optical transmitter's vertical eye closure when transmitted through a worst case optical channel (specified in 122.8.5.2), as measured through an optical to electrical converter (O/E) with a bandwidth equivalent to a reference receiver, and equalized with the reference equalizer (as described in 122.8.5.4). The reference receiver and equalizer may be implemented in software or may be part of the oscilloscope.

Table 122–15 specifies the test patterns to be used for measurement of TDECQ.

122.8.5.1 TDECQ conformance test setup

A block diagram for the TDECQ conformance test is shown in Figure 122–4. Other equivalent measurement implementations may be used with suitable calibration.

Each optical lane is tested individually with all other lanes in operation and all lanes using the same test pattern. There shall be at least 31 UI delay between the test pattern on one lane and the pattern on any other lane, so that the symbols on each lane are not correlated within the PMD. The optical splitter and variable reflector are adjusted so that each transmitter is tested with the optical return loss specified in Table 122–16. The state of polarization of the back reflection is adjusted to create the greatest RIN. The optical filter is used to separate the lane under test from the others. Each optical lane is tested with the optical channel described in 122.8.5.2. The combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of

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approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz, and at frequencies above 1.5 × 26.5625 GHz, the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The optical filter passband ripple shall be limited to 0.5 dB peak-to-peak and the isolation is chosen such that the ratio of the power in the lane being measured to the sum of the powers of all of the other lanes is greater than 20 dB (see ITU-T G.959.1 Annex B).

The test pattern (specified in Table 122–15) is transmitted repetitively by the optical lane under test and the oscilloscope is set up to capture the complete pattern for TDECQ analysis as described in 122.8.5.3. The clock recovery unit (CRU) has a corner frequency of 4 MHz and a slope of 20 dB/decade. The CRU can be implemented in hardware or software depending on oscilloscope technology.

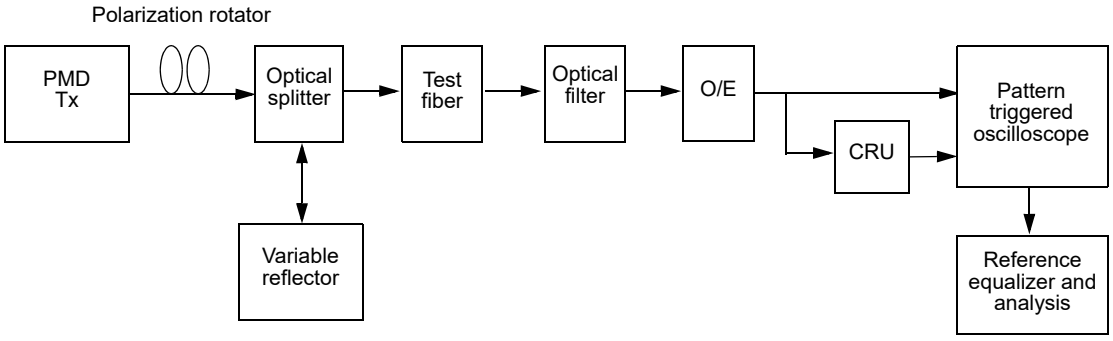

Figure 122–4—TDECQ conformance test block diagram

122.8.5.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 122–16.

Table 122–16—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]	Max mean DGD
	Minimum	Maximum			
200GBASE-FR4 or 400GBASE-FR8	$0.0465 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.0465 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	17.1 dB	0.8 ps
200GBASE-LR4 or 400GBASE-LR8	$0.2325 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.2325 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	15.6 dB	0.8 ps
200GBASE-ER4 or 400GBASE-ER8	$0.93 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.93 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	15 dB	0.8 ps

[a] The dispersion is measured for the wavelength of the device under test (λ in nm). The coefficient assumes 2 km for 200GBASE-FR4 and 400GBASE-FR8, 10 km for 200GBASE-LR4 and 400GBASE-LR8, and 40 km for 200GBASE-ER4 and 400GBASE-ER8.
[b] There is no intent to stress the sensitivity of the O/E converter associated with the oscilloscope.
[c] The optical return loss is applied at TP2.

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A 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, or 400GBASE-ER8 transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 122–16 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss specified in Table 122–16. The state of polarization of the back reflection is adjusted to create the greatest RIN.

The mean DGD of the channel is to be less than the value specified in Table 122–16.

122.8.5.3 TDECQ measurement method

TDECQ for 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 is measured as described in 121.8.5.3 with the exception that the reference equalizer is as specified in 122.8.5.4.

122.8.5.4 TDECQ reference equalizer

The reference equalizer for 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 is a 5-tap, T-spaced, feed-forward equalizer (FFE), where T is the symbol period. A functional model of the reference equalizer is shown in Figure 122–5. The sum of the equalizer tap coefficients is equal to 1. Tap 1, tap 2, or tap 3 has the largest magnitude tap coefficient, which is constrained to be at least 0.8.

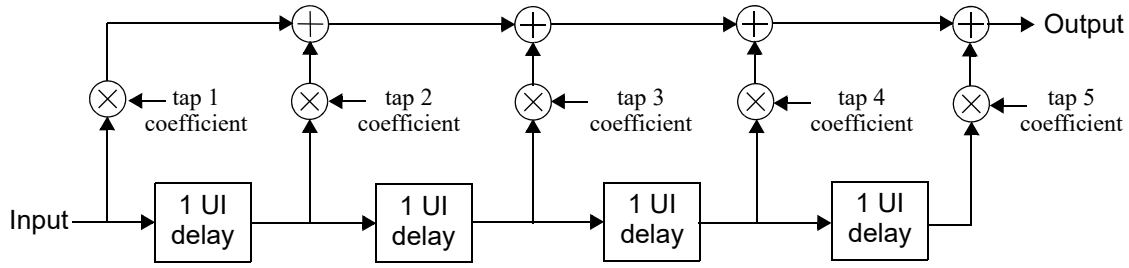

Figure 122–5—TDECQ reference equalizer functional model

NOTE—This reference equalizer is part of the TDECQ test and does not imply any particular receiver equalizer implementation.

122.8.6 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 122–9 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and in Table 122–10 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 if measured using a test pattern specified for extinction ratio in Table 122–15 with the sum of the optical power from all of the lanes not under test being below –30 dBm, or if other lanes are operating, a suitable optical filter may be used to separate the lane under test. The extinction ratio of a PAM4 optical signal is defined as the ratio of the average optical launch power level P_3, measured over the central 2 UI of

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a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 122–3.

122.8.7 Transmitter transition time

The transmitter transition time of each lane shall be within the limits given in Table 122–9 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and in Table 122–10 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8, if measured using a test pattern specified for transmitter transition time in Table 122–15.

Transmitter transition time is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer}, or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling edges respectively, as measured through an O/E converter and oscilloscope with response defined as follows. The combined response of the O/E converter and oscilloscope has a 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz. At frequencies above 1.5 × 26.5625 GHz, the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The 0% level and the 100% level are P_0 and P_3 as defined by the OMA_{outer} measurement procedure (see 121.8.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence, and the falling edge is that within the 33333000000 symbol sequence.

122.8.8 Relative intensity noise ($RIN_{17.1}OMA$, $RIN_{15.6}OMA$, and $RIN_{15}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 17.1 dB for 200GBASE-FR4 and 400GBASE-FR8, 15.6 dB for 200GBASE-LR4 and 400GBASE-LR8, and 15 dB for 200GBASE-ER4 and 400GBASE-ER8.

b) Each lane may be tested individually with the sum of the optical power from all of the lanes not under test being below –30 dBm, or if other lanes are operating, a suitable optical filter may be used to separate the lane under test.

c) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 26.6 GHz).

d) The test pattern is according to Table 122–15.

122.8.9 Receiver sensitivity

For 200GBASE-FR4, receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 3.1 dB. Receiver sensitivity should meet Equation (122–1), which is illustrated in Figure 122–6.

For 200GBASE-LR4, receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 3.2 dB. Receiver sensitivity should meet Equation (122–2), which is illustrated in Figure 122–6.

For 200GBASE-ER4, receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 3.2 dB. Receiver sensitivity should meet Equation (122–3), which is illustrated in Figure 122–6.

$$RS = \max(-5.5, SECQ - 6.9) \quad \text{(dBm)} \tag{122–1}$$

$$RS = \max(-7.2, SECQ - 8.6) \quad \text{(dBm)} \tag{122–2}$$

$$RS = \max(-15.1, SECQ - 16.5) \quad \text{(dBm)} \tag{122–3}$$

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where

RS is the receiver sensitivity

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

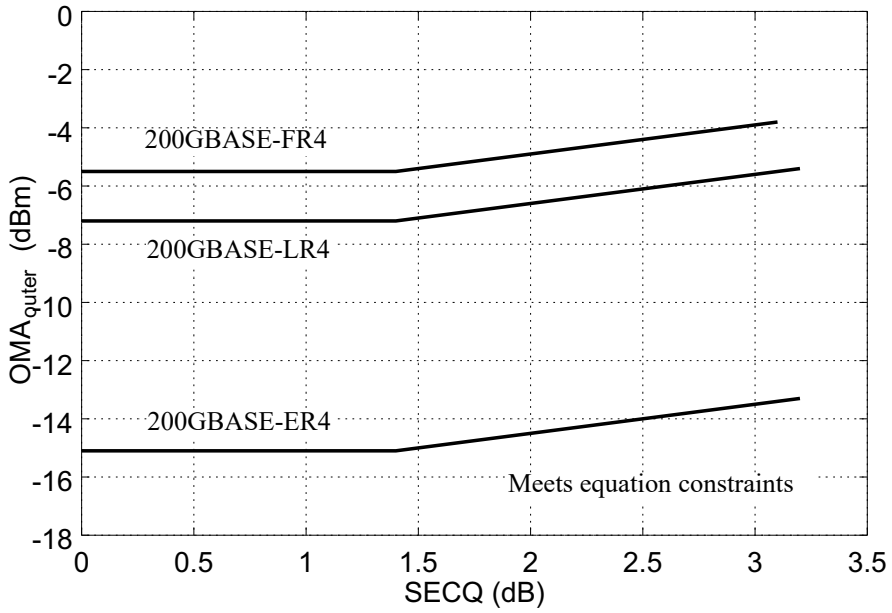

Figure 122–6—Illustration of receiver sensitivity for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4

For 400GBASE-FR8, receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 2.9 dB. Receiver sensitivity should meet Equation (122–4), which is illustrated in Figure 122–7.

For 400GBASE-LR8, receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 3.1 dB. Receiver sensitivity should meet Equation (122–5), which is illustrated in Figure 122–7.

For 400GBASE-ER8, receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 3.4 dB. Receiver sensitivity should meet Equation (122–6), which is illustrated in Figure 122–7.

$$RS = \max(-4.8, SECQ - 6.2) \quad \text{(dBm)} \tag{122–4}$$

$$RS = \max(-6.6, SECQ - 8) \quad \text{(dBm)} \tag{122–5}$$

$$RS = \max(-16.1, SECQ - 17.5) \quad \text{(dBm)} \tag{122–6}$$

where

RS is the receiver sensitivity

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

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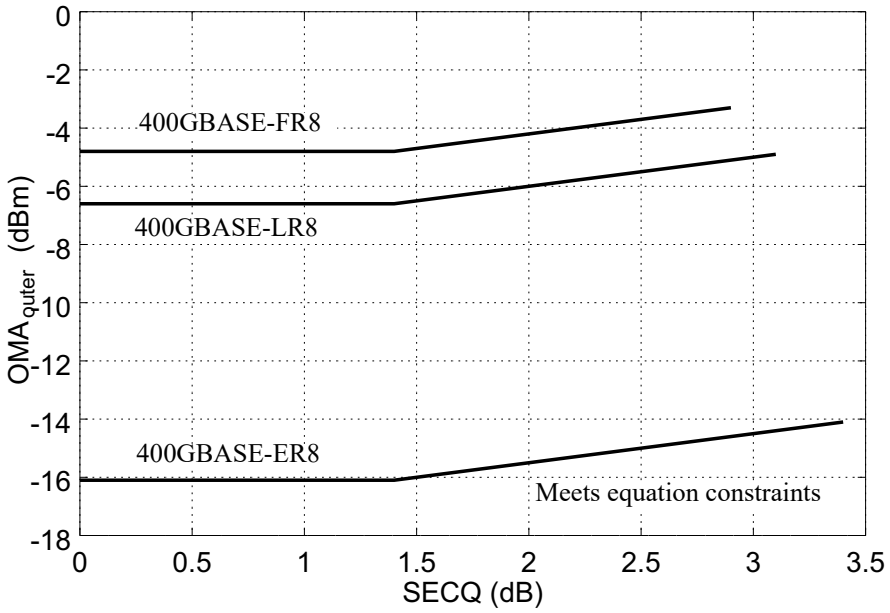

Figure 122–7—Illustration of receiver sensitivity for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8

The normative requirement for receivers is stressed receiver sensitivity.

122.8.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 122–11 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and in Table 122–12 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 if measured using the method defined in 122.8.10.1 and 122.8.10.3, with the conformance test signal at TP3 as described in 122.8.10.2, using the test pattern specified for SRS in Table 122–15. The BER is required to be met for the lane under test on its own.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Any of the patterns specified for SRS in Table 122–15 is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal.

122.8.10.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 122–8. The patterns used for the received conformance signal are specified in Table 122–15. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 122.8.10.2 and has sinusoidal jitter applied as specified in 121.8.10.4. A suitable test set is needed to characterize the signal used to test the receiver. Stressed receiver conformance test signal verification is described in 122.8.10.3.

The low-pass filter is used to create ISI. The sinusoidal amplitude interferer causes additional eye closure, but in conjunction with the finite edge rates, also causes some jitter.

The sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferer may be set at any frequency between

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100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferer, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The Gaussian noise generator, the amplitude of the sinusoidal interferer, and the low-pass filter are adjusted so that the SECQ specified in Table 122–11 or Table 122–12 is met, according to the methods specified in 122.8.10.2.

For improved visibility for calibration, all elements in the signal path (cables, DC blocks, E/O converter, etc.) should have wide and smooth frequency response, and linear phase response, throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be negligible.

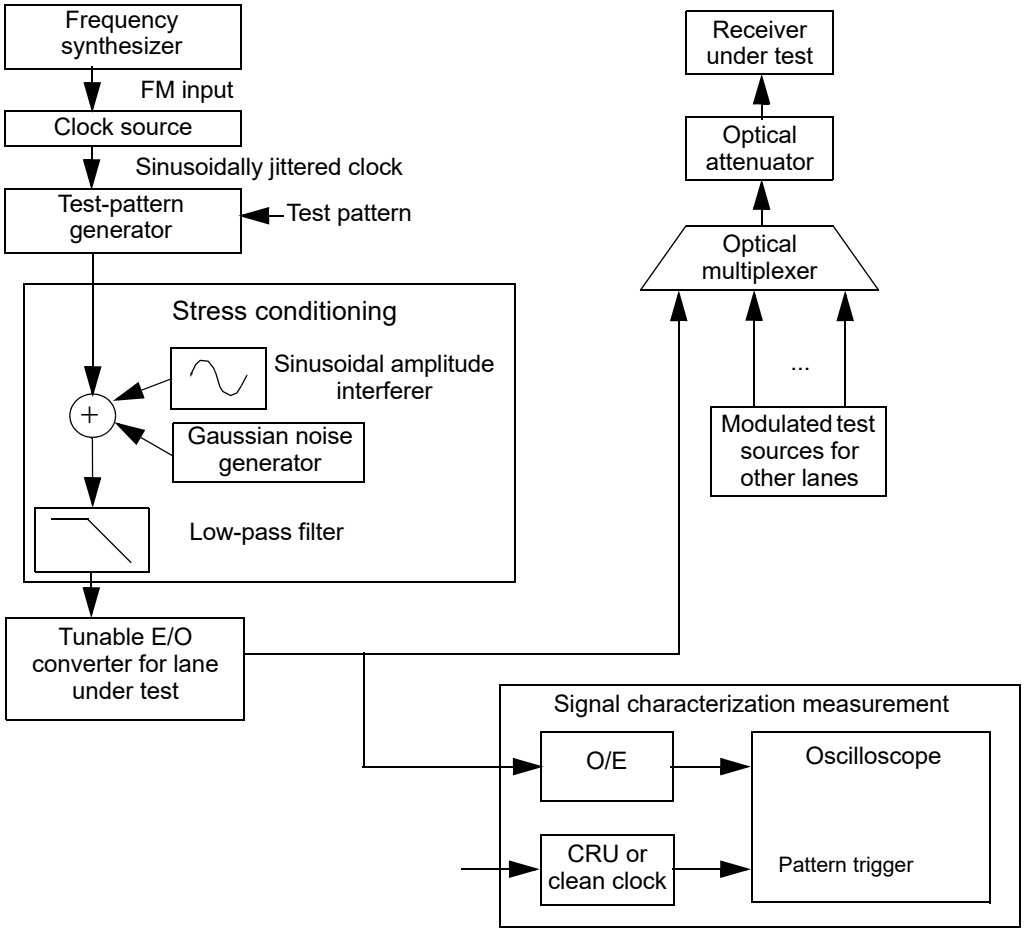

Figure 122–8—Stressed receiver conformance test block diagram

122.8.10.2 Stressed receiver conformance test signal characteristics and calibration

The stressed receiver conformance test signal characteristics and calibration methods are as described in 121.8.10.2 with the following exceptions:

— The SECQ of the stressed receiver conformance test signal is measured according to 122.8.5, except that the test fiber is not used. The transition time of the stressed receiver conformance test signal is no greater than the value specified in Table 122–9 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and in Table 122–10 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8.

— An example stressed receiver conformance test setup is shown in Figure 122–8; however, alternative test setups that generate equivalent stress conditions may be used.

— With the Gaussian noise generator on and the sinusoidal jitter and sinusoidal interferer turned off, the $RIN_{xx.x}$OMA of the SRS test source should be no greater than the value specified in Table 122–9 for

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200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and in Table 122–10 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8.

— The signaling rate of the test pattern generator and the extinction ratio of the E/O converter are as given in Table 122–9 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and in Table 122–10 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8.

— The required values of the "Stressed receiver sensitivity (OMA_{outer}), each lane (max)", "Stressed eye closure for PAM4 (SECQ), lane under test", "SECQ – $10\log_{10}(C_{eq})$ (max), lane under test", and "OMA_{outer} of each aggressor lane" are as given in Table 122–11 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4 and in Table 122–12 for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8.

122.8.10.3 Stressed receiver conformance test signal verification

The SECQ of the stressed receiver conformance test signal is measured according to 122.8.5, except that the test fiber is not used. The clock output from the clock source in Figure 122–8 is modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye jitter that includes the sinusoidal jitter component, a separate clock source (clean clock of Figure 122–8) is required that is synchronized to the source clock, but not modulated with the jitter source.

Care should be taken when characterizing the test signal because excessive noise/jitter in the measurement system would result in an input signal that does not fully stress the receiver under test. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. The noise/jitter introduced by the O/E, filters, and oscilloscope should be negligible or the results should be corrected for its effects. While the details of test equipment are beyond the scope of this standard, it is recommended that the implementer fully characterize the test equipment and apply appropriate guard bands so that the stressed receiver conformance input signal meets the stress and sinusoidal jitter specified in 122.8.10.2 and 121.8.10.4.

122.9 Safety, installation, environment, and labeling

122.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

122.9.2 Laser safety

200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, and 400GBASE-LR8 optical transceivers shall conform to Hazard Level 1 laser requirements and 400GBASE-ER8 optical transceivers shall conform to Hazard Level 1M laser requirements, as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[210]

[210]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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122.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

122.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, or 400GBASE-ER8 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

122.9.5 Electromagnetic emission

A system integrating a 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, or 400GBASE-ER8 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

122.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

122.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 400GBASE-FR8).

Labeling requirements for Hazard Level 1 and Hazard Level 1M lasers are given in the laser safety standards referenced in 122.9.2.

122.10 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 122–9.

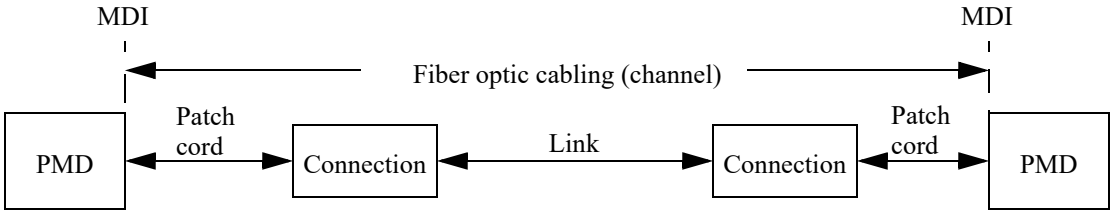

Figure 122–9—Fiber optic cabling model

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The channel insertion loss is given in Table 122–17. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 122–17—Fiber optic cabling (channel) characteristics

Description	200GBASE-FR4	400GBASE-FR8	200GBASE-LR4	400GBASE-LR8	200GBASE-ER4		400GBASE-ER8		Unit
Operating distance (max)	2		10		30	40	30	40	km
Channel insertion loss[a,b] (max)	4		6.3[c]		18		18		dB
Channel insertion loss (min)	0		0		10[d]				dB
Positive dispersion[b] (max)	6.7	1.9	9.5		28	37	28	37	ps/nm
Negative dispersion[b] (min)	–11.9	–10.2	–28.4	–50.8	–85	–114	–151	–201	ps/nm
DGD_max[e]	3		8		10.3				ps
Optical return loss (min)	25		22		19				dB

[a] These channel insertion loss values include cable, connectors, and splices.
[b] Over the wavelength range 1264.5 nm to 1337.5 nm for 200GBASE-FR4, 1294.53 nm to 1310.19 nm for 200GBASE-LR4 and 200GBASE-ER4, and 1272.55 nm to 1310.19 nm for 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8.
[c] Using 0.46 dB/km at 1272.55 nm attenuation for optical fiber cables derived from Appendix I of ITU-T G.695 may not support operation at 10 km for 400GBASE-LR8 under worst case conditions.
[d] Channel insertion loss (min) may be implemented with an optical attenuator.
[e] Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

122.11 Characteristics of the fiber optic cabling (channel)

The 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8 fiber optic cabling shall meet the specifications defined in Table 122–17. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

122.11.1 Optical fiber cable

The fiber optic cable requirements are satisfied by cables containing IEC 60793-2-50 type B1.1 (dispersion un-shifted single-mode), type B1.3 (low water peak single-mode), or type B6_a (bend insensitive) fibers or the requirements in Table 122–18 where they differ.

122.11.2 Optical fiber connection

An optical fiber connection, as shown in Figure 122–9, consists of a mated pair of optical connectors.

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Table 122–18—Optical fiber and cable characteristics

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.47[a] or 0.5[b]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \le \lambda_0 \le 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a] The 0.47 dB/km at 1264.5 nm attenuation for optical fiber cables is derived from Appendix I of ITU-T G.695.
[b] The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3. Using 0.5 dB/km may not support operation at 10 km for 200GBASE-LR4 or 400GBASE-LR8 or at 40 km for 200GBASE-ER4 or 400GBASE-ER8.

122.11.2.1 Connection insertion loss

The maximum link distance for 200GBASE-LR4, 200GBASE-ER4, 400GBASE-LR8, and 400GBASE-ER8 is based on an allocation of 2 dB total connection and splice loss. For example, this allocation supports four connections with an average insertion loss per connection of 0.5 dB. The maximum link distance for 200GBASE-FR4 and 400GBASE-FR8 is based on an allocation of 3 dB total connection and splice loss. Connections with different loss characteristics may be used provided the requirements of Table 122–17 are met.

122.11.2.2 Maximum discrete reflectance

The maximum value for each discrete reflectance shall be less than or equal to the value shown in Table 122–19 corresponding to the number of discrete reflectances above –55 dB within the channel. For numbers of discrete reflectances in between two numbers shown in the table, the lower of the two corresponding maximum discrete reflectance values applies.

Table 122–19—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance		
	200GBASE-FR4 or 400GBASE-FR8	200GBASE-LR4 or 400GBASE-LR8	200GBASE-ER4 or 400GBASE-ER8
1	–25 dB	–22 dB	–19 dB
2	–31 dB	–29 dB	–27 dB
4	–35 dB	–33 dB	–32 dB
6	–38 dB	–35 dB	–35 dB
8	–40 dB	–37 dB	–37 dB
10	–41 dB	–39 dB	–39 dB

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122.11.3 Medium Dependent Interface (MDI) requirements

The 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, or 400GBASE-ER8 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 122–9). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 122.5.1, not at the MDI.

122.12 Requirements for interoperation between 200GBASE-ER4 and 200GBASE-LR4

The 200GBASE-ER4 and 200GBASE-LR4 PMDs can interoperate with each other (over an engineered link) provided that the fiber optic cabling (channel) characteristics for 200GBASE-LR4 are met, with the exception of the maximum and minimum channel insertion loss values, which are given in Table 122–20 for the two link directions separately. Attenuators may be used to achieve the required losses.

Table 122–20—Channel insertion loss requirements for interoperation between 200GBASE-ER4 and 200GBASE-LR4

Direction	Min loss	Max loss	Unit
200GBASE-ER4 transmitter to 200GBASE-LR4 receiver	2.3	10.1	dB
200GBASE-LR4 transmitter to 200GBASE-ER4 receiver	8.7	14.2	dB

122.13 Requirements for interoperation between 400GBASE-ER8 and 400GBASE-FR8

The 400GBASE-ER8 and 400GBASE-FR8 PMDs can interoperate with each other (over an engineered link) provided that the fiber optic cabling (channel) characteristics for 400GBASE-FR8 are met, with the exception of the maximum and minimum channel insertion loss values, which are given in Table 122–21 for the two link directions separately. Attenuators may be used to achieve the required losses.

Table 122–21—Channel insertion loss requirements for interoperation between 400GBASE-ER8 and 400GBASE-FR8

Direction	Min loss	Max loss	Unit
400GBASE-ER8 transmitter to 400GBASE-FR8 receiver	0.7	6.9	dB
400GBASE-FR8 transmitter to 400GBASE-ER8 receiver	9.7	15.1	dB

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122.14 Requirements for interoperation between 400GBASE-ER8 and 400GBASE-LR8

The 400GBASE-ER8 and 400GBASE-LR8 PMDs can interoperate with each other (over an engineered link) provided that the fiber optic cabling (channel) characteristics for 400GBASE-LR8 are met, with the exception of the maximum and minimum channel insertion loss values, which are given in Table 122–22 for the two link directions separately. Attenuators may be used to achieve the required losses.

Table 122–22—Channel insertion loss requirements for interoperation between 400GBASE-ER8 and 400GBASE-LR8

Direction	Min loss	Max loss	Unit
400GBASE-ER8 transmitter to 400GBASE-LR8 receiver	0.7	8.5	dB
400GBASE-LR8 transmitter to 400GBASE-ER8 receiver	9.7	15.8	dB

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122.15 Protocol implementation conformance statement (PICS) proforma for Clause 122, Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8[211]

122.15.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 122, Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

122.15.2 Identification

122.15.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

122.15.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 122, Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[211] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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122.15.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*FR4	200GBASE-FR4 PMD	122.7	Device supports requirements for 200GBASE-FR4 PHY	O.1	Yes [ ] No [ ]
*LR4	200GBASE-LR4 PMD	122.7	Device supports requirements for 200GBASE-LR4 PHY	O.1	Yes [ ] No [ ]
*ER4	200GBASE-ER4 PMD	122.7	Device supports requirements for 200GBASE-ER4 PHY	O.1	Yes [ ] No [ ]
*FR8	400GBASE-FR8 PMD	122.7	Device supports requirements for 400GBASE-FR8 PHY	O.1	Yes [ ] No [ ]
*LR8	400GBASE-LR8 PMD	122.7	Device supports requirements for 400GBASE-LR8 PHY	O.1	Yes [ ] No [ ]
*ER8	400GBASE-ER8 PMD	122.7	Device supports requirements for 400GBASE-ER8 PHY	O.1	Yes [ ] No [ ]
*INS	Installation / cable	122.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	122.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	122.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	122.5.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	122.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	122.4	Registers and interface supported	O	Yes [ ] No [ ]

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122.15.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-FR4, 200GBASE-LR4, 200GBASE-ER4, 400GBASE-FR8, 400GBASE-LR8, and 400GBASE-ER8

122.15.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 200GBASE-R or 400GBASE-R PCS and PMA	122.1		M	Yes [ ]
F2	Integration with management functions	122.1		O	Yes [ ] No [ ]
F3	Bit error ratio	122.1.1	Meets the BER specified in 122.1.1	M	Yes [ ]
F4	Transmit function	122.5.2	Conveys symbols from PMD service interface to MDI	M	Yes [ ]
F5	Optical multiplexing and delivery to the MDI	122.5.2	Optically multiplexes the four or eight optical signals for delivery to the MDI	M	Yes [ ]
F6	Mapping between optical signal and logical signal for transmitter	122.5.2	Highest optical power corresponds to tx_symbol = three	M	Yes [ ]
F7	Receive function	122.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]
F8	Conversion of four or eight optical signals to eight electrical signals	122.5.3	For delivery to the PMD service interface	M	Yes [ ]
F9	Mapping between optical signal and logical signal for receiver	122.5.3	Highest optical power corresponds to rx_symbol = three	M	Yes [ ]
F10	Global Signal Detect function	122.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F11	Global Signal Detect behavior	122.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all four or eight lanes	M	Yes [ ]
F12	Lane-by-lane Signal Detect function	122.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 122–4	MD:O	Yes [ ] No [ ] N/A [ ]
F13	PMD reset function	122.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

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122.15.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	122.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	122.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD lane-by-lane transmit disable function	122.5.8	Disables the optical transmitter via MDIO on the lane associated with the PMD_transmit_disable_*i* variable	MD:O.2	Yes [ ] No [ ] N/A [ ]
M4	PMD lane-by-lane transmit disable	122.5.8	Disables each optical transmitter independently if M3 = No	O.2	Yes [ ] N/A [ ]
M5	PMD_fault function	122.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M6	PMD_transmit_fault function	122.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
M7	PMD_receive_fault function	122.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

122.15.4.3 PMD to MDI optical specifications for 200GBASE-FR4

Item	Feature	Subclause	Value/Comment	Status	Support
FRF1	Transmitter meets specifications in Table 122–9	122.7.1	Per definitions in 122.8	FR4:M	Yes [ ] N/A [ ]
FRF2	Receiver meets specifications in Table 122–11	122.7.2	Per definitions in 122.8	FR4:M	Yes [ ] N/A [ ]

122.15.4.4 PMD to MDI optical specifications for 200GBASE-LR4

Item	Feature	Subclause	Value/Comment	Status	Support
LRF1	Transmitter meets specifications in Table 122–9	122.7.1	Per definitions in 122.8	LR4:M	Yes [ ] N/A [ ]
LRF2	Receiver meets specifications in Table 122–11	122.7.2	Per definitions in 122.8	LR4:M	Yes [ ] N/A [ ]

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122.15.4.5 PMD to MDI optical specifications for 200GBASE-ER4

Item	Feature	Subclause	Value/Comment	Status	Support
ERF1	Transmitter meets specifications in Table 122–9	122.7.1	Per definitions in 122.8	ER4:M	Yes [ ] N/A [ ]
ERF2	Receiver meets specifications in Table 122–11	122.7.2	Per definitions in 122.8	ER4:M	Yes [ ] N/A [ ]

122.15.4.6 PMD to MDI optical specifications for 400GBASE-FR8

Item	Feature	Subclause	Value/Comment	Status	Support
FRE1	Transmitter meets specifications in Table 122–10	122.7.1	Per definitions in 122.8	FR8:M	Yes [ ] N/A [ ]
FRE2	Receiver meets specifications in Table 122–12	122.7.2	Per definitions in 122.8	FR8:M	Yes [ ] N/A [ ]

122.15.4.7 PMD to MDI optical specifications for 400GBASE-LR8

Item	Feature	Subclause	Value/Comment	Status	Support
LRE1	Transmitter meets specifications in Table 122–10	122.7.1	Per definitions in 122.8	LR8:M	Yes [ ] N/A [ ]
LRE2	Receiver meets specifications in Table 122–12	122.7.2	Per definitions in 122.8	LR8:M	Yes [ ] N/A [ ]

122.15.4.8 PMD to MDI optical specifications for 400GBASE-ER8

Item	Feature	Subclause	Value/Comment	Status	Support
ERE1	Transmitter meets specifications in Table 122–10	122.7.1	Per definitions in 122.8	ER8:M	Yes [ ] N/A [ ]
ERE2	Receiver meets specifications in Table 122–12	122.7.2	Per definitions in 122.8	ER8:M	Yes [ ] N/A [ ]

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122.15.4.9 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	122.8	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and SMSR	122.8.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	122.8.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA measurements	122.8.4	Each lane	M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	122.8.5	Each lane	M	Yes [ ]
OM6	Extinction ratio	122.8.6	Each lane	M	Yes [ ]
OM7	Transmitter transition time	122.8.7	Each lane	M	Yes [ ]
OM8	RIN_{xx}OMA measurement procedure	122.8.8	Each lane	M	Yes [ ]
OM9	Stressed receiver sensitivity	122.8.10	Each lane	M	Yes [ ]

122.15.4.10 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	122.9.1	Conforms to J.2	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	122.9.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	!ER8:M	Yes [ ] N/A [ ]
ES3	Laser safety—IEC Hazard Level 1M	122.9.2	Conforms to Hazard Level 1M laser requirements defined in IEC 60825-1 and IEC 60825-2	ER8:M	Yes [ ] N/A [ ]
ES4	Electromagnetic interference	122.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

122.15.4.11 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	122.11	Meets requirements specified in Table 122–17	INS:M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	122.11.2.2	Meets requirements specified in Table 122–19	INS:M	Yes [ ] N/A [ ]
OC3	MDI requirements	122.11.3	Meets IEC 61753-1-1 and IEC 61753-021-2	INS:M	Yes [ ] N/A [ ]

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123. Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR16

123.1 Overview

This clause specifies the 400GBASE-SR16 PMD together with the multimode fiber medium. The PMD sublayer provides a point-to-point 400 Gb/s Ethernet link over 16 pairs of multimode fiber, up to at least 100 m. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 123–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 123–1—Physical Layer clauses associated with the 400GBASE-SR16 PMD

Associated clause	400GBASE-SR16
117—RS	Required
117—400GMII[a]	Optional
118—400GMII Extender	Optional
119—PCS	Required
120—PMA	Required
120B—Chip-to-chip 400GAUI-16	Optional
120C—Chip-to-module 400GAUI-16	Optional
120D—Chip-to-chip 400GAUI-8	Optional
120E—Chip-to-module 400GAUI-8	Optional
78—Energy Efficient Ethernet	Optional

[a] The 400GMII is an optional interface. However, if the 400GMII is not implemented, a conforming implementation behaves functionally as though the RS and 400GMII were present.

Figure 123–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 400 Gb/s Ethernet is introduced in Clause 116 and the purpose of each PHY sublayer is summarized in 116.2.

400GBASE-SR16 PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Further relevant information may be found in Clause 1 (terminology and conventions, references, definitions and abbreviations) and Annex A (bibliography, referenced as [B1], [B2], etc.).

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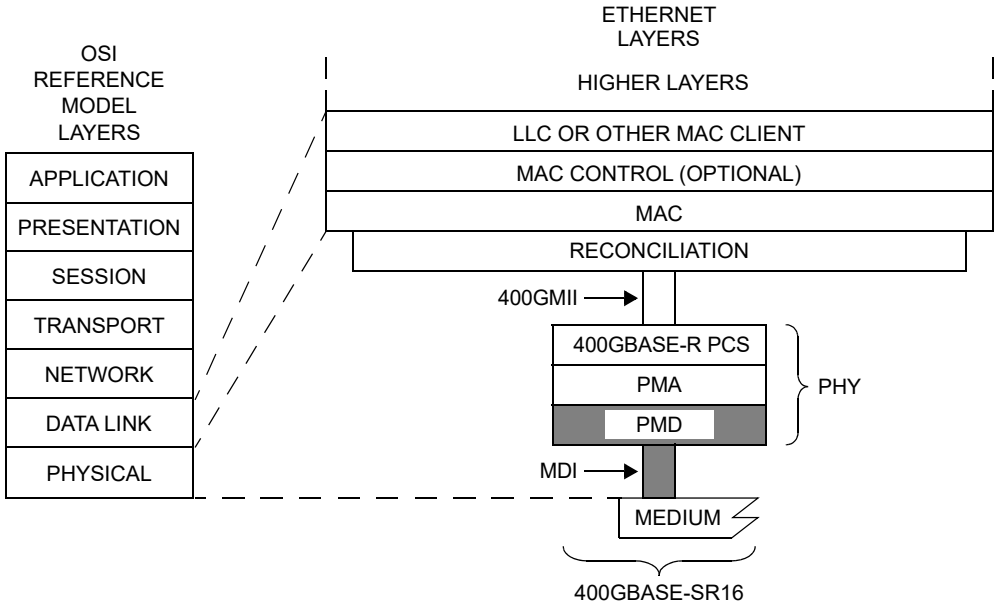

400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
SR = PMD FOR MULTIMODE FIBER

Figure 123–1—400GBASE-SR16 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

123.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when processed according to Clause 119. For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap.

123.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 400GBASE-SR16 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

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The PMD service interface is an instance of the inter-sublayer service interface defined in 116.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 400GBASE-SR16 PMD has 16 parallel bit streams, hence $i = 0$ to 15.

In the transmit direction, the PMA continuously sends 16 parallel bit streams to the PMD, one per lane, each at a nominal signaling rate of 26.5625 GBd. The PMD converts these streams of bits into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends 16 parallel bit streams to the PMA corresponding to the signals received from the MDI, one per lane, each at a nominal signaling rate of 26.5625 GBd.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication(SIGNAL_OK) inter-sublayer service primitive defined in 116.3.

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 123.1.1.

123.3 Delay and Skew

123.3.1 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation. The sum of the transmit and receive delays at one end of the link contributed by the 400GBASE-SR16 PMD including 2 m of fiber in one direction shall be no more than 8192 bit times (16 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 116.4 and its references.

123.3.2 Skew constraints

The Skew (relative delay) between the lanes is kept within limits so that the information on the lanes can be reassembled by the PCS sublayer. Skew and Skew Variation are defined in 116.5 and specified at the points SP1 to SP6 shown in Figure 116–4 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

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For more information on Skew and Skew Variation see 116.5. The measurements of Skew and Skew Variation are defined in 86.8.3.1.

123.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 123–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 123–3.

Table 123–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable 15	PMD transmit disable extension register	1.27.0	PMD_transmit_disable_15
PMD transmit disable 14 to PMD transmit disable 0	PMD transmit disable register	1.9.15 to 1.9.1	PMD_transmit_disable_14 to PMD_transmit_disable_0

Table 123–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect 15	PMD receive signal detect extension register	1.28.0	PMD_signal_detect_15
PMD receive signal detect 14 to PMD receive signal detect 0	PMD receive signal detect register	1.10.15 to 1.10.1	PMD_signal_detect_14 to PMD_signal_detect_0

123.5 PMD functional specifications

The 400GBASE-SR16 PMD performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

123.5.1 PMD block diagram

The PMD block diagram is shown in Figure 123–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a multimode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 123.8 are made at TP2. The optical receive signal is defined at

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the output of the fiber optic cabling (TP3) at the MDI (see 123.11.3). Unless specified otherwise, all receiver measurements and tests defined in 123.8 are made at TP3.

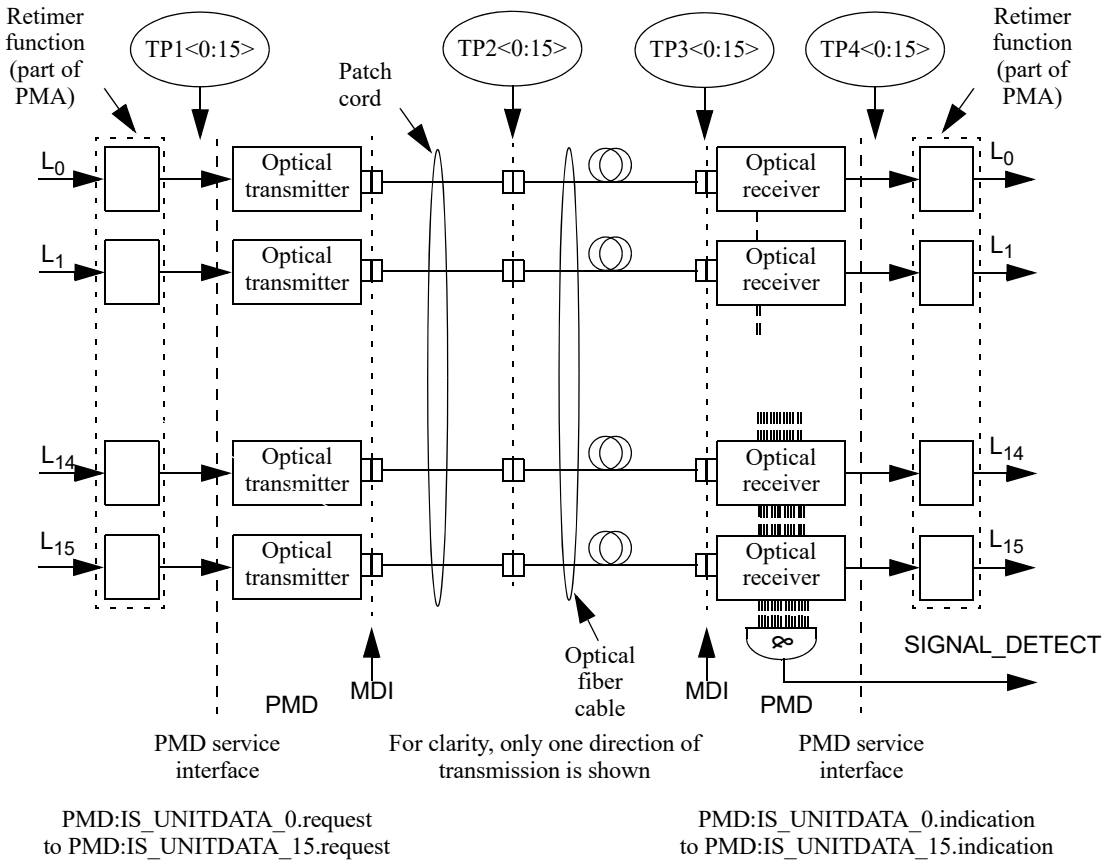

Figure 123–2—Block diagram for 400GBASE-SR16 transmit/receive paths

TP1 and TP4 are optional reference points that may be useful to implementers for testing components (these test points will not typically be accessible in an implemented system).

123.5.2 PMD transmit function

The PMD Transmit function shall convert the 16 bit streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_15.request into 16 optical signals. The optical signals shall then be delivered to the MDI which contains 16 parallel light paths for transmit, according to the transmit optical specifications in this clause. The higher optical power level in each signal shall correspond to tx_symbol = one.

123.5.3 PMD receive function

The PMD Receive function shall convert the 16 optical signals received from the MDI into separate bit streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_15.indication, all according to the receive optical specifications in this clause. The higher optical power level in the signal shall correspond to rx_symbol = one.

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123.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 116.3.

SIGNAL_DETECT shall be an indicator of the presence of the optical signals on all 16 lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 123–4. The PMD receiver is not required to verify whether a compliant 400GBASE-SR16 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 123–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –30 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ average receive power, each lane (min) in Table 95–7) AND (compliant 400GBASE-SR16 signal input)]	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the PMD global signal detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signals and implementations that respond to the average optical power of the modulated optical signals. When the MDIO is implemented, the SIGNAL_DETECT value shall be continuously set in response to the magnitude of the optical signals, according to the requirements of Table 123–4.

123.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:15, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 123–4.

123.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

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123.5.7 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 95–6.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter in each lane.

123.5.8 PMD lane-by-lane transmit disable function (optional)

The PMD lane-by-lane transmit disable function is optional and allows the optical transmitter in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:15) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 95–6.

b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the optical transmitter in each lane.

If the optional PMD lane-by-lane transmit disable function is not implemented in MDIO, an alternative method may be provided to independently disable each transmit lane.

123.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

123.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on the transmitter, the PMD shall set PMD_transmit_fault to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

123.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

123.6 Lane assignments

There are no lane assignments (within a group of transmit or receive lanes) for 400GBASE-SR16. While it is expected that a PMD will map electrical lane *i* to optical lane *i* and vice versa, there is no need to define the physical ordering of the lanes, as the PCS sublayer is capable of receiving the lanes in any arrangement. The positioning of transmit and receive lanes at the MDI is specified in 123.11.3.

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123.7 PMD to MDI optical specifications for 400GBASE-SR16

The operating range for the 400GBASE-SR16 PMD is defined in Table 123–5. A 400GBASE-SR16 compliant PMD operates on 50/125 μm multimode fibers, type A1a.2 (OM3), type A1a.3 (OM4), or type A1a.4 (OM5), according to the specifications defined in Table 123–6. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 400GBASE-SR16 PMD operating at 120 m meets the operating range requirement of 0.5 m to 100 m). The operating range shown in Table 123–5 is the same as 100GBASE-SR4 (See Clause 95).

Table 123–5—400GBASE-SR16 operating range

PMD type	Required operating range[a]
400GBASE-SR16	0.5 m to 70 m for OM3
	0.5 m to 100 m for OM4
	0.5 m to 100 m for OM5

[a] The PCS FEC correction function may not be bypassed for any operating distance.

123.7.1 400GBASE-SR16 transmitter optical specifications

The optical characteristics of each lane of a 400GBASE-SR16 transmitter shall be the same as those of a single lane of 100GBASE-SR4, as specified in Table 95–6 and 95.7.1, with the exception that the "signaling rate, each lane" is 26.5625 GBd ± 100 ppm, TDEC is as specified in 123.8.5, and the BER requirement is as specified in 123.1.1.

123.7.2 400GBASE-SR16 receive optical specifications

The optical characteristics of each lane of a 400GBASE-SR16 receiver shall be the same as those of a single lane of 100GBASE-SR4, as specified in Table 95–7 and 95.7.2, with the exception that the "signaling rate, each lane" is 26.5625 GBd ± 100 ppm, stressed receiver sensitivity is as specified in 123.8.8, and the BER requirement is as specified in 123.1.1.

123.7.3 400GBASE-SR16 illustrative link power budget

The illustrative power budget and penalties for each lane of a 400GBASE-SR16 link are the same as those of a single lane of 100GBASE-SR4, as specified in Table 95–8 and 95.7.3.

123.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified. Optical parameters and measurement methods for 400GBASE-SR16 are the same as for 100GBASE-SR4.

123.8.1 Test patterns for optical parameters

The test patterns used in this clause shall be the same as those used for 100GBASE-SR4, as described in 95.8.1 and shown in Table 95–9, with the exception that pattern 5 defined in 82.2.11 is encoded by Clause 119 PCS for 400GBASE-SR16. Table 95–10 as modified by this subclause (123.8.1) shows the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined.

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123.8.2 Center wavelength and spectral width

The center wavelength and RMS spectral width shall be within the range given in Table 95–6 if measured per IEC 61280-1-3. The transmitter is modulated using one of the test patterns specified in Table 95–10 as modified by 123.8.1.

123.8.3 Average optical power

The average optical power shall be within the limits given in Table 95–6 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using one of the test patterns specified in Table 95–10 as modified by 123.8.1.

123.8.4 Optical Modulation Amplitude (OMA)

OMA shall be within the limits given in Table 95–6 if measured as defined in 52.9.5 for measurement with a square wave (8 ones, 8 zeros) test pattern or as defined in 68.6.2 (from the variable MeasuredOMA in 68.6.6.2) for measurement with a PRBS9 test pattern. See 123.8.1 for test pattern information.

123.8.5 Transmitter and dispersion eye closure (TDEC)

TDEC is a measure of the optical transmitter's vertical eye closure, as described in 95.8.5. TDEC shall be within the limits given in Table 95–6 if measured using the methods specified in 95.8.5.1 and 95.8.5.2, with the exceptions that the clock recovery unit (CRU) has a corner frequency of 4 MHz and in Equation (95–6), 3.8906R is replaced by 3.4917R, for consistency with the BER of 2.4×10^{-4} given in 123.1.1. Table 95–10 as modified by 123.8.1 specifies the test patterns to be used for measurement of TDEC.

123.8.6 Extinction ratio

The extinction ratio shall be within the limits given in Table 95–6 if measured using the methods specified in IEC 61280-2-2. The extinction ratio is measured using one of the test patterns specified for extinction ratio in Table 95–10 as modified by 123.8.1.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 95–10).

123.8.7 Transmitter optical waveform (transmit eye)

The transmitter optical waveform of a port transmitting the test pattern specified in Table 95–10 as modified by 123.8.1 shall meet the transmitter eye mask coordinates and hit ratio specified in Table 95–6 if measured according to the methods specified in 95.8.7 with the exception that the clock recovery unit's high frequency corner bandwidth is 4 MHz.

123.8.8 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 95–7 if measured using the methods defined in 95.8.8 with the following exceptions:

- The signaling rate of the test pattern generator is set to the rate defined in 123.7.2.
- The clock recovery unit (CRU) has a corner bandwidth of 4 MHz.
- Sinusoidal jitter is added as specified in Table 87–13 instead of Table 95–11.
- When using 95.8.5 to measure the SEC of the stressed receiver conformance test signal, the BER requirement is as specified in 123.1.1 and 3.4917R replaces 3.8906R in Equation (95–6).
- The hit ratio for the stressed receiver eye mask definition is changed from 5×10^{-5} to 2.4×10^{-4}.

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123.9 Safety, installation, environment, and labeling

123.9.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1.

123.9.2 Laser safety

400GBASE-SR16 optical transceivers shall conform to Hazard Level 1M laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[212]

123.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

123.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 400GBASE-SR16 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate, in the literature associated with the PHY, the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

123.9.5 Electromagnetic emission

A system integrating a 400GBASE-SR16 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

123.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

[212]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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123.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 400GBASE-SR16).

Labeling requirements for Hazard Level 1M lasers are given in the laser safety standards referenced in 123.9.2.

123.10 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 123–3. The fiber type and length are the same as 100BASE-SR4 (see Clause 95).

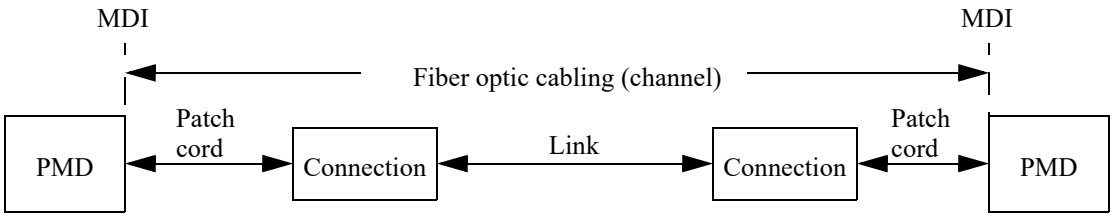

Figure 123–3—Fiber optic cabling model

The channel insertion loss is given in Table 123–6. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, modal dispersion, reflections and losses of all connectors and splices meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1 one-cord method. As OM4 and OM5 optical fiber meet the requirements for OM3, a channel compliant to the "OM3" column may use OM4 or OM5 optical fiber, or a combination of OM3, OM4, and OM5. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 123–6—Fiber optic cabling (channel) characteristics for 400GBASE-SR16

Description	OM3	OM4	OM5	Unit
Operating distance (max)	70	100	100	m
Channel insertion loss[a] (max)	1.8	1.9	1.9	dB
Channel insertion loss (min)	0			dB

[a] These channel insertion loss values include cable loss plus 1.5 dB allocated for connection and splice loss, over the wavelength range 840 nm to 860 nm.

123.11 Characteristics of the fiber optic cabling (channel)

The 400GBASE-SR16 fiber optic cabling shall meet the specifications defined in Table 123–6. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. The requirements for the optical fiber, connection insertion loss, and maximum discrete reflectance are the same as 100GBASE-SR4 (see Clause 95).

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123.11.1 Optical fiber cable

The fiber contained within the 400GBASE-SR16 fiber optic cabling shall comply with the specifications and parameters of Table 123–7. A variety of multimode cable types may satisfy these requirements, provided the resulting channel also meets the specifications of Table 123–6.

Table 123–7—Optical fiber and cable characteristics

Description	OM3[a]	OM4[b]	OM5[c]	Unit
Nominal core diameter	50			μm
Nominal fiber specification wavelength	850			nm
Effective modal bandwidth (min)[d]	2000	4700		MHz.km
Cabled optical fiber attenuation (max)	3.5			dB/km
Zero dispersion wavelength (λ_0)	$1295 \le \lambda_0 \le 1340$		$1297 \le \lambda_0 \le 1328$	nm
Chromatic dispersion slope (max) (S_0)	0.105 for $1295 \le \lambda_0 \le 1310$ and $0.000375 \times (1590 - \lambda_0)$ for $1310 \le \lambda_0 \le 1340$		$-412/(840(1-(\lambda_0/840)^4))$ for $1297 \le \lambda_0 \le 1328$	ps/nm^2 km

[a] IEC 60793-2-10 type A1a.2.
[b] IEC 60793-2-10 type A1a.3.
[c] IEC 60793-2-10 type A1a.4.
[d] When measured with the launch conditions specified in Table 95–6.

123.11.2 Optical fiber connection

An optical fiber connection, as shown in Figure 123–3, consists of a mated pair of optical connectors.

123.11.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an average insertion loss per connection of 0.5 dB. Connections with lower loss characteristics may be used provided the requirements of Table 123–6 are met. However, the loss of a single connection shall not exceed 0.75 dB.

123.11.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –20 dB.

123.11.3 Medium Dependent Interface (MDI)

The 400GBASE-SR16 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 123–3). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

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123.11.3.1 Optical lane assignments

The 16 transmit and 16 receive optical lanes of 400GBASE-SR16 shall occupy the positions depicted in Figure 123–4 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains 32 active lanes. The transmit optical lanes occupy the upper 16 positions. The receive optical lanes occupy the lower 16 positions.

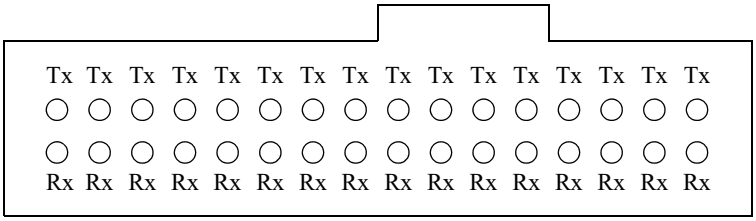

Figure 123–4—400GBASE-SR16 optical lane assignments

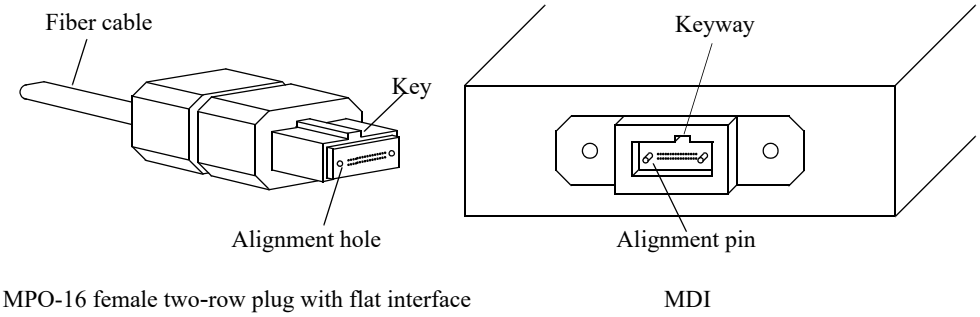

Figure 123–5—MPO-16 female two-row plug with flat interface, and an MDI

123.11.3.2 Medium Dependent Interface (MDI) requirements

The MDI adapter or receptacle shall meet the dimensional specifications for designation FOCIS 18 A-k-0 as defined in ANSI/TIA-604-18. The plug terminating the optical fiber cabling shall meet the dimensional specifications of designation FOCIS 18 P-2x16-1-0-2-2 as defined in ANSI/TIA-604-18. The MDI shall optically mate with the plug on the optical fiber cabling. Figure 123–5 shows an MPO-16 female two-row plug with flat interface, and an MDI. The MDI shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2 for performance Class Cm/2m.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 123.5.1, not at the MDI.

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123.12 Protocol implementation conformance statement (PICS) proforma for Clause 123, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR16[213]

123.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 123, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR16, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

123.12.2 Identification

123.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

123.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 123, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR16
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[213]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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123.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*INS	Installation/cable	123.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	123.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	123.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	123.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	123.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	123.4	Registers and interface supported	O	Yes [ ] No [ ]

123.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR16

123.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 400GBASE-R PCS and PMA	123.1		M	Yes [ ]
F2	Integration with management functions	123.1		O	Yes [ ] No [ ]
F3	Bit error ratio	123.1.1	Meets the BER specified in 123.1.1	M	Yes [ ]
F4	Transmit function	123.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
F5	Mapping between optical signal and logical signal for transmitter	123.5.2	Higher optical power is a one	M	Yes [ ]
F6	Receive function	123.5.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
F7	Conversion of 16 optical signals to 16 electrical signals	123.5.3	For delivery to the PMD service interface	M	Yes [ ]
F8	Mapping between optical signal and logical signal for receiver	123.5.3	Higher optical power is a one	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F9	Global Signal Detect function	123.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F10	Global Signal Detect behavior	123.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all 16 lanes	M	Yes [ ]
F11	Lane-by-lane Signal Detect function	123.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 123–4	MD:O	Yes [ ] No [ ] N/A [ ]
F12	PMD reset function	123.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

123.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	123.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	123.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD lane-by-lane transmit disable function	123.5.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_*i* variable	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD_fault function	123.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_transmit_fault function	123.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
M6	PMD_receive_fault function	123.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

123.12.4.3 PMD to MDI optical specifications for 400GBASE-SR16

Item	Feature	Subclause	Value/Comment	Status	Support
SR1	Transmitter meets specifications in 95.7.1 with the exceptions in 123.7.1	123.7.1	Per definitions in 123.8	M	Yes [ ]
SR2	Receiver meets specifications in 95.7.2 with the exceptions in 123.7.2	123.7.2	Per definitions in 123.8	M	Yes [ ]

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123.12.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	123.8	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and spectral width	123.8.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	123.8.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA measurements	123.8.4	Each lane	M	Yes [ ]
OM5	Transmitter and dispersion eye closure (TDEC)	123.8.5	Each lane	M	Yes [ ]
OM6	Extinction ratio	123.8.6	Per IEC 61280-2-2	M	Yes [ ]
OM7	Transmit eye	123.8.7	Each lane	M	Yes [ ]
OM8	Stressed receiver sensitivity	123.8.8		M	Yes [ ]

123.12.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	123.9.1	Conforms to IEC 60950-1	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1M	123.9.2	Conforms to Hazard Level 1M laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	123.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

123.12.4.6 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	123.11	Meets requirements specified in Table 123–6	INS:M	Yes [ ] N/A [ ]
OC2	Optical fiber characteristics	123.11.1	Per Table 123–7	INS:M	Yes [ ] N/A [ ]
OC3	Maximum discrete reflectance	123.11.2.2	Less than –20 dB	INS:M	Yes [ ] N/A [ ]
OC4	MDI layout	123.11.3.1	Optical lane assignments per Figure 123–4	M	Yes [ ]
OC5	MDI dimensions	123.11.3.2	Meets FOCIS 18 A-k-0 as defined in ANSI/TIA-604-18	M	Yes [ ]
OC6	Cabling connector dimensions	123.11.3.2	Meets FOCIS 18 P-2x16-1-0-2-2 as defined in ANSI/TIA-604-18	INS:M	Yes [ ] N/A [ ]
OC7	MDI mating	123.11.3.2	MDI optically mates with plug on the cabling	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
OC8	MDI requirements	123.11.3.2	Meets IEC 61753-1 and IEC 61753-022-2	INS:M	Yes [ ] N/A [ ]

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124. Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4

124.1 Overview

This clause specifies the 400GBASE-DR4 PMD together with the single-mode fiber medium. The optical signal generated by this PMD type is modulated using a 4-level pulse amplitude modulation (PAM4) format. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 124–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 124–1—Physical Layer clauses associated with the 400GBASE-DR4 PMD

Associated clause	400GBASE-DR4
117—RS	Required
117—400GMII[a]	Optional
118—400GMII Extender	Optional
119—PCS	Required
120—PMA	Required
120B—Chip-to-chip 400GAUI-16	Optional
120C—Chip-to-module 400GAUI-16	Optional
120D—Chip-to-chip 400GAUI-8	Optional
120E—Chip-to-module 400GAUI-8	Optional
78—Energy Efficient Ethernet	Optional

[a] The 400GMII is an optional interface. However, if the 400GMII is not implemented, a conforming implementation behaves functionally as though the RS and 400GMII were present.

Figure 124–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 400 Gb/s Ethernet is introduced in Clause 116 and the purpose of each PHY sublayer is summarized in 116.2.

400GBASE-DR4 PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

124.1.1 Bit error ratio

The bit error ratio (BER) when processed according to Clause 120 shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when processed according to Clause 120 and then Clause 119. For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

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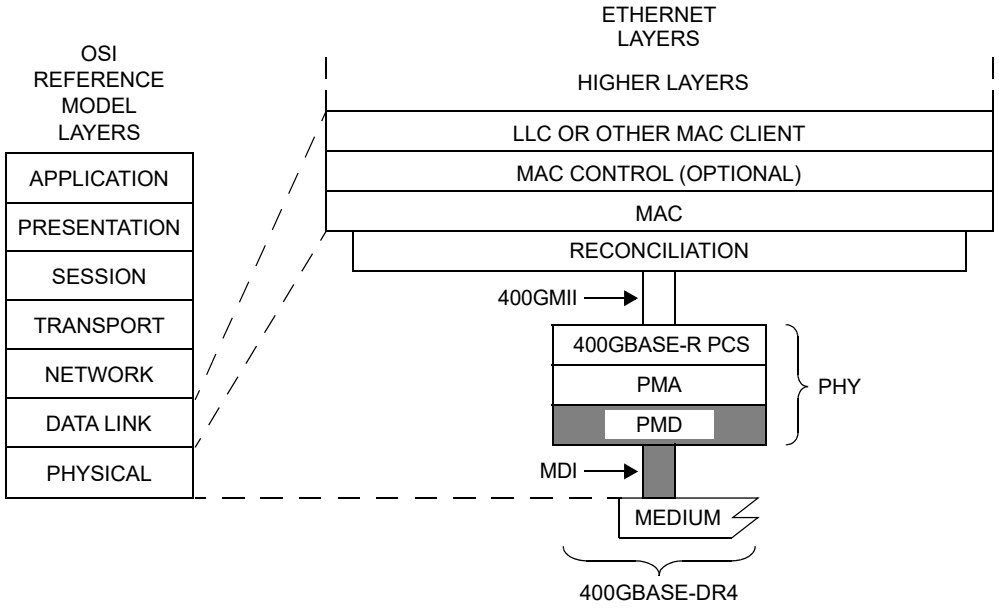

Figure 124–1—400GBASE-DR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap.

124.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 400GBASE-DR4 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 116.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 400GBASE-DR4 PMD has four parallel symbol streams, hence $i = 0$ to 3.

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In the transmit direction, the PMA continuously sends four parallel symbol streams to the PMD, one per lane, each at a nominal signaling rate of 53.125 GBd. The PMD then converts these streams of data units into the appropriate signals on the MDI.

In the receive direction, the PMD continuously sends four parallel symbol streams to the PMA corresponding to the signals received from the MDI, one per lane, each at a nominal signaling rate of 53.125 GBd. See NOTE at the end of 120.5.2 concerning the transition density of lanes operating at this nominal signaling rate.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication(SIGNAL_OK) inter-sublayer service interface primitive defined in 116.3.

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 124.1.1.

124.3 Delay and Skew

124.3.1 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the 400GBASE-DR4 PMD including 2 m of fiber in one direction shall be no more than 8192 bit times (16 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 116.4 and its references.

124.3.2 Skew constraints

The Skew (relative delay between the lanes) and Skew Variation are kept within limits so that the information on the lanes can be reassembled by the PCS. Skew and Skew Variation are defined in 116.5 and specified at the points SP1 to SP6 shown in Figure 116–4 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 116.5. The measurements of Skew and Skew Variation are defined in 86.8.3.1.

124.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO

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control variables to PMD control variables shall be as shown in Table 124–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 124–3.

Table 124–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable 3 to PMD transmit disable 0	PMD transmit disable register	1.9.4 to 1.9.1	PMD_transmit_disable_3 to PMD_transmit_disable_0

Table 124–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 0	PMD receive signal detect register	1.10.4 to 1.10.1	PMD_signal_detect_3 to PMD_signal_detect_0

124.5 PMD functional specifications

The 400GBASE-DR4 PMD performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

124.5.1 PMD block diagram

The PMD block diagram is shown in Figure 124–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 124.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 124.11.3). Unless specified otherwise, all receiver measurements and tests defined in 124.8 are made at TP3.

TP1<0:3> and TP4<0:3> are optional reference points that may be useful to implementors for testing components (these test points will not typically be accessible in an implemented system).

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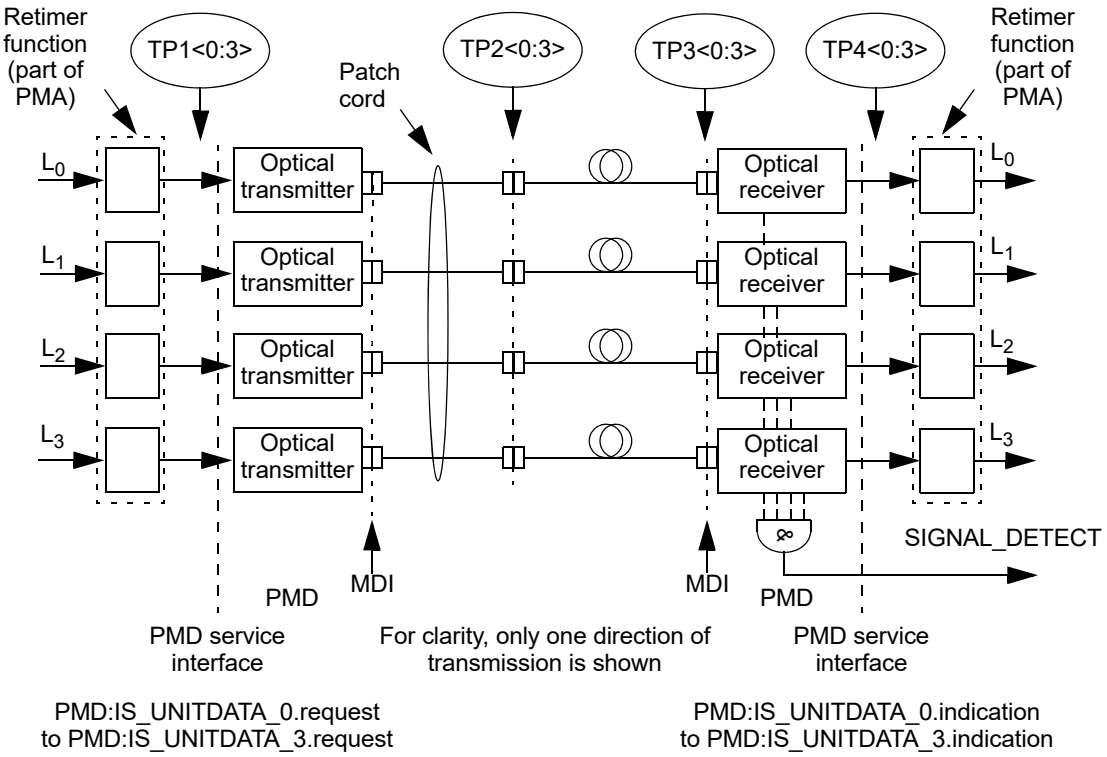

Figure 124–2—Block diagram for 400GBASE-DR4 transmit/receive paths

124.5.2 PMD transmit function

The PMD Transmit function shall convert the four symbol streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request into four separate optical signals. The four optical signals shall then be delivered to the MDI, which contains four parallel light paths for transmit, according to the transmit optical specifications in this clause. The highest optical power level in each signal shall correspond to tx_symbol = three and the lowest shall correspond to tx_symbol = zero.

124.5.3 PMD receive function

The PMD Receive function shall convert the four parallel optical signals received from the MDI into separate symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to rx_symbol = three and the lowest shall correspond to rx_symbol = zero.

124.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 116.3.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all four lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 124–4.

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The PMD receiver is not required to verify whether a compliant 400GBASE-DR4 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 124–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –15 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ average receive power, each lane (min) Table 124–7) AND (compliant 400GBASE–R signal input)]	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

124.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:3, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 124–4.

124.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

124.5.7 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 124–6.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter in each lane.

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124.5.8 PMD lane-by-lane transmit disable function (optional)

The PMD lane-by-lane transmit disable function is optional and allows the optical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:3) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 124–6.

b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the optical transmitter in each lane.

If the optional PMD lane-by-lane transmit disable function is not implemented in MDIO, an alternative method may be provided to independently disable each transmit lane for testing purposes.

124.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

124.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

124.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

124.6 Lane assignments

There are no lane assignments (within a group of transmit or receive lanes) for 400GBASE-DR4. While it is expected that a PMD will map electrical lane *i* to optical lane *i* and vice versa, there is no need to define the physical ordering of the lanes, as the PCS sublayer is capable of receiving the lanes in any arrangement. The positioning of transmit and receive lanes at the MDI is specified in 124.11.3.1.

124.7 PMD to MDI optical specifications for 400GBASE-DR4

The operating range for the 400GBASE-DR4 PMD is defined in Table 124–5. A 400GBASE-DR4 compliant PMD operates on type B1.1, B1.3, or B6_a single-mode fibers according to the specifications defined in Table 124–12. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 400GBASE-DR4 PMD operating at 600 m meets the operating range requirement of 2 m to 500 m).

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Table 124–5—400GBASE-DR4 operating range

PMD type	Required operating range
400GBASE-DR4	2 m to 500 m

124.7.1 400GBASE-DR4 transmitter optical specifications

The 400GBASE-DR4 transmitter shall meet the specifications defined in Table 124–6 per the definitions in 124.8.

Table 124–6—400GBASE-DR4 transmit characteristics

Description	Value	Unit
Signaling rate, each lane (range)	53.125 ± 100 ppm	GBd
Modulation format	PAM4	—
Lane wavelength (range)	1304.5 to 1317.5	nm
Side-mode suppression ratio (SMSR), (min)	30	dB
Average launch power, each lane (max)	4	dBm
Average launch power, each lane[a] (min)	–2.9	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	4.2	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)[b]	–0.8	dBm
Launch power in OMA_{outer} minus TDECQ, each lane (min)	–2.2	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	3.4	dB
TDECQ – $10\log_{10}(C_{eq})$[c] (max)	3.4	dB
Average launch power of OFF transmitter, each lane (max)	–15	dBm
Extinction ratio, each lane (min)	3.5	dB
Transmitter transition time (max)	17	ps
$RIN_{21.4}OMA$ (max)	–136	dB/Hz
Optical return loss tolerance (max)	21.4	dB
Transmitter reflectance[d] (max)	–26	dB

[a] Average launch power, each lane (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b] Even if the TDECQ < 1.4 dB, the OMA_{outer} (min) has to exceed this value.
[c] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[d] Transmitter reflectance is defined looking into the transmitter.

124.7.2 400GBASE-DR4 receive optical specifications

The 400GBASE-DR4 receiver shall meet the specifications defined in Table 124–7 per the definitions in 124.8. See NOTE at the end of 120.5.2 concerning the transition density of lanes operating at this nominal signaling rate.

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Table 124–7—400GBASE-DR4 receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	53.125 ± 100 ppm	GBd
Modulation format	PAM4	—
Lane wavelengths (range)	1304.5 to 1317.5	nm
Damage threshold[a], each lane	5	dBm
Average receive power, each lane (max)	4	dBm
Average receive power, each lane[b] (min)	–5.9	dBm
Receive power (OMA_{outer}), each lane (max)	4.2	dBm
Receiver reflectance (max)	–26	dB
Receiver sensitivity (OMA_{outer}), each lane[c] (max)	Equation (124–1)	dBm
Stressed receiver sensitivity (OMA_{outer}), each lane[d] (max)	–1.9	dBm
Conditions of stressed receiver sensitivity test:[e]		
Stressed eye closure for PAM4 (SECQ), lane under test	3.4	dB
SECQ – $10\log_{10}(C_{eq})$[f] (max), lane under test	3.4	dB
OMA_{outer} of each aggressor lane	4.2	dBm

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
[b] Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] Receiver sensitivity (OMA_{outer}), each lane (max) is optional and is defined for a transmitter with a value of SECQ up to 3.4 dB.
[d] Measured with conformance test signal at TP3 (see 124.8.10) for the BER specified in 124.1.1.
[e] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

124.7.3 400GBASE-DR4 illustrative link power budget

An illustrative power budget and penalties for 400GBASE-DR4 channels are shown in Table 124–8.

Table 124–8—400GBASE-DR4 illustrative link power budget

Parameter	Value	Unit
Power budget (for max TDECQ)	6.5	dB
Operating distance	500	m
Channel insertion loss[a]	3	dB
Maximum discrete reflectance	See 124.11.2.2	dB
Allocation for penalties[b] (for max TDECQ)	3.5	dB
Additional insertion loss allowed	0	dB

[a] The channel insertion loss is calculated using the maximum distance specified in Table 124–5 and cabled optical fiber attenuation of 0.5 dB/km at 1304.5 nm plus an allocation for connection and splice loss given in 124.11.2.1.

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[b] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

124.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

124.8.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 124–10 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 124–10 may be used to perform that test. The test patterns used in this clause are shown in Table 124–9.

Table 124–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle	119.2.4.9
6	SSPRQ	120.5.11.2.3

Table 124–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 400GBASE-R signal	124.8.2
Side mode suppression ratio	3, 5, 6 or valid 400GBASE-R signal	124.8.2
Average optical power	3, 5, 6 or valid 400GBASE-R signal	124.8.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	124.8.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	124.8.5
Extinction ratio	4 or 6	124.8.6
Transmitter transition time	Square wave or 6	124.8.7
$RIN_{21.4}OMA$	Square wave	124.8.8
Stressed receiver conformance test signal calibration	6	124.8.10
Stressed receiver sensitivity	3 or 5	124.8.10

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124.8.2 Wavelength and side mode suppression ratio (SMSR)

The wavelength and SMSR of each optical lane shall be within the range given in Table 124–6 if measured per IEC 61280-1-3. The lane under test is modulated using the test pattern defined in Table 124–10.

124.8.3 Average optical power

The average optical power of each lane shall be within the limits given in Table 124–6 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using the test pattern defined in Table 124–10.

124.8.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} of each lane shall be within the limits given in Table 124–6. The OMA_{outer} is measured using a test pattern specified for OMA_{outer} in Table 124–10 as the difference between the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 124–3.

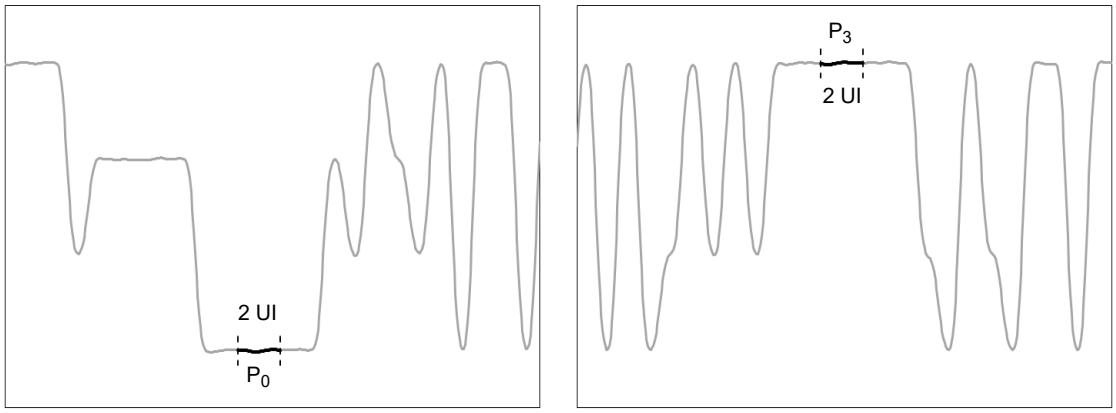

Figure 124–3—Example power levels P_0 and P_3 from PRBS13Q test pattern

124.8.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

The TDECQ and TDECQ – $10\log_{10}(C_{eq})$ of each lane shall be within the limits given in Table 124–6 if measured using the methods specified in 121.8.5.1, 121.8.5.2, and 121.8.5.3 using a reference equalizer as described in 121.8.5.4 where T is the symbol period for 400GBASE-DR4, with the following exceptions:

— The signaling rate of the test pattern generator is as given in Table 124–6 and uses the test pattern specified for TDECQ in Table 124–10.

— The combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 26.5625 GHz with a fourth-order Bessel-Thomson response to at least 1.3 × 53.125 GHz, and at frequencies above 1.3 × 53.125 GHz, the response should not exceed –20 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

— The normalized noise power density spectrum $N(f)$ is equivalent to white noise filtered by a fourth-order Bessel-Thomson response filter with a 3 dB bandwidth of 26.5625 GHz.

124.8.6 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 124–6 if measured using a test pattern specified for extinction ratio in Table 124–10. The extinction ratio of a PAM4 optical signal is

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defined as the ratio of the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 124–3.

124.8.7 Transmitter transition time

The transmitter transition time of each lane shall be within the limits given in Table 124–6 if measured using a test pattern specified for transmitter transition time in Table 124–10.

Transmitter transition time is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer}, or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling edges respectively, as measured through an O/E converter and oscilloscope with response defined as follows. The combined response of the O/E converter and oscilloscope has a 3 dB bandwidth of approximately 26.5625 GHz with a fourth-order Bessel-Thomson response to at least 1.3 × 53.125 GHz. At frequencies above 1.3 × 53.125 GHz, the response should not exceed –20 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The 0% level and the 100% level are P_0 and P_3 as defined by the OMA_{outer} measurement procedure (see 124.8.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence, and the falling edge is that within the 33333000000 symbol sequence.

124.8.8 Relative intensity noise ($RIN_{21.4}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 21.4 dB.
b) Each lane may be tested individually with the sum of the optical power from all of the lanes not under test being below –30 dBm.
c) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 53.2 GHz).
d) The test pattern is according to Table 124–10.

124.8.9 Receiver sensitivity

Receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 3.4 dB. Receiver sensitivity should meet Equation (124–1), which is illustrated in Figure 124–4.

$$RS = \max(-3.9, SECQ - 5.3) \quad \text{(dBm)} \tag{124–1}$$

where

RS	is the receiver sensitivity
$SECQ$	is the SECQ of the transmitter used to measure the receiver sensitivity

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The normative requirement for receivers is stressed receiver sensitivity.

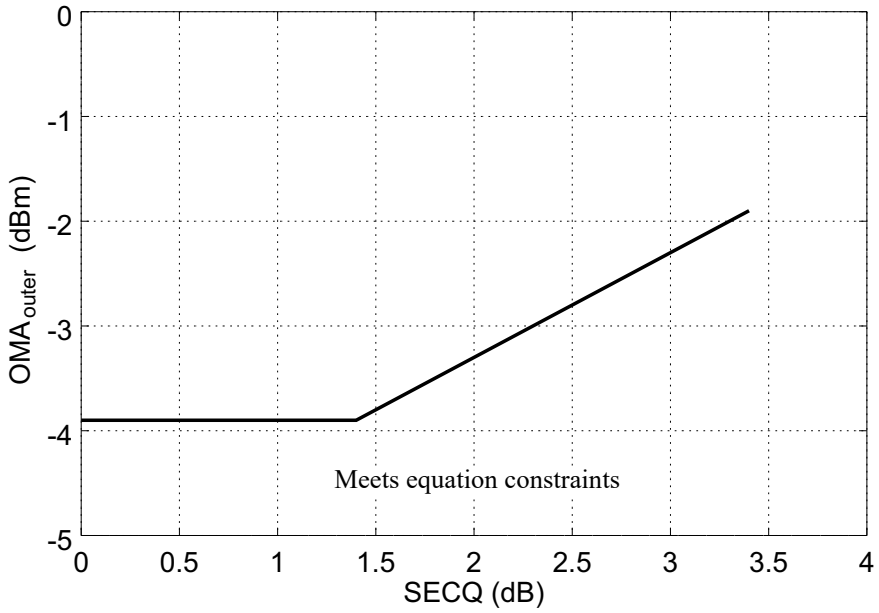

Figure 124–4—Illustration of receiver sensitivity

124.8.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 124–7 if measured using the method defined in 121.8.10 with the following exceptions:

- The SECQ of the stressed receiver conformance test signal is measured according to 124.8.5, except that the test fiber is not used. The transition time of the stressed receiver conformance test signal is no greater than the value specified in Table 124–6.
- With the Gaussian noise generator on and the sinusoidal jitter and sinusoidal interferer turned off, the $RIN_{21.4}OMA$ of the SRS test source should be no greater than the value specified in Table 124–6.
- The signaling rate of the test pattern generator and the extinction ratio of the E/O converter are as given in Table 124–6 using test patterns specified in Table 124–10.
- The required values of the "Stressed receiver sensitivity (OMA_{outer}), each lane (max)", "Stressed eye closure for PAM4 (SECQ), lane under test", "SECQ – $10\log_{10}(C_{eq})$ (max), lane under test", and "OMA_{outer} of each aggressor lane" are as given in Table 124–7.

124.9 Safety, installation, environment, and labeling

124.9.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1.

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124.9.2 Laser safety

400GBASE-DR4 optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[214]

124.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

124.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 400GBASE-DR4 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

[214]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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124.9.5 Electromagnetic emission

A system integrating a 400GBASE-DR4 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

124.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

124.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 400GBASE-DR4).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 124.9.2.

124.10 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 124–5.

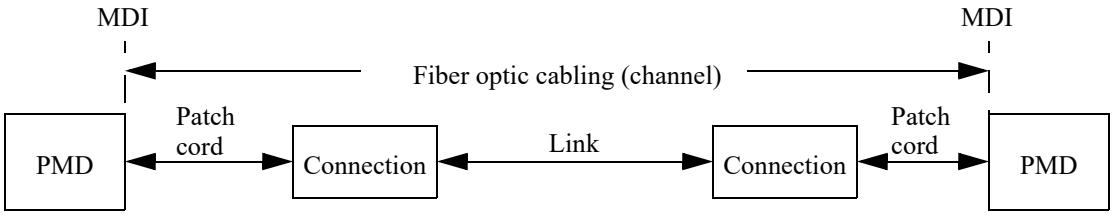

Figure 124–5—Fiber optic cabling model

The channel insertion loss is given in Table 124–11. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

124.11 Characteristics of the fiber optic cabling (channel)

The 400GBASE-DR4 fiber optic cabling shall meet the specifications defined in Table 124–12. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

124.11.1 Optical fiber cable

The fiber optic cable requirements are satisfied by cables containing IEC 60793-2-50 type B1.1 (dispersion un-shifted single-mode), type B1.3 (low water peak single-mode), or type B6_a (bend insensitive) fibers or the requirements in Table 124–12 where they differ.

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Table 124–11—Fiber optic cabling (channel) characteristics

Description	400GBASE-DR4	Unit
Operating distance (max)	500	m
Channel insertion loss[a,b] (max)	3	dB
Channel insertion loss (min)	0	dB
Positive dispersion[b] (max)	0.8	ps/nm
Negative dispersion[b] (min)	–0.93	ps/nm
DGD_max[c]	2.24	ps
Optical return loss (min)	37	dB

[a] These channel insertion loss values include cable, connectors, and splices.
[b] Over the wavelength range 1304.5 nm to 1317.5 nm.
[c] Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

Table 124–12—Optical fiber and cable characteristics

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.5[a]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \le \lambda_0 \le 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a] The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3.

124.11.2 Optical fiber connection

An optical fiber connection, as shown in Figure 124–5, consists of a mated pair of optical connectors.

124.11.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 2.75 dB total connection and splice loss. For example, this allocation supports five connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 124–11 are met.

124.11.2.2 Maximum discrete reflectance

The maximum value for each discrete reflectance shall be less than or equal to the value shown in Table 124–13 corresponding to the number of discrete reflectances above –55 dB within the channel. For numbers of discrete reflectances in between two numbers shown in the table, the lower of the two corresponding maximum discrete reflectance values applies.

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Table 124–13—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance
1	–37 dB
2	–42 dB
4	–45 dB
6	–47 dB
8	–48 dB
10	–49 dB

124.11.3 Medium Dependent Interface (MDI)

The 400GBASE-DR4 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 124–5). The 400GBASE-DR4 PMD is coupled to the fiber optic cabling through one connector plug into the MDI optical receptacle as shown in Figure 124–7. Example constructions of the MDI include the following:

a) PMD with a connectorized fiber pigtail plugged into an adapter
b) PMD receptacle

124.11.3.1 Optical lane assignments

The four transmit and four receive optical lanes of 400GBASE-DR4 shall occupy the positions depicted in Figure 124–6 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains eight active lanes within twelve total positions. The transmit optical lanes occupy the left-most four positions. The receive optical lanes occupy the right-most four positions. The four center positions are unused.

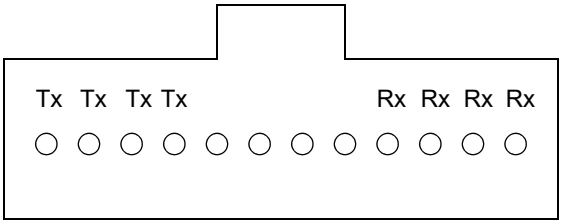

Figure 124–6—400GBASE-DR4 optical lane assignments

124.11.3.2 Medium Dependent Interface (MDI) requirements

The MDI shall meet the dimensional specifications of IEC 61754-7-1 interface 7-1-9: *MPO device receptacle, angled interface*. The plug terminating the optical fiber cabling shall meet the dimensional specifications of IEC 61754-7-1 interface 7-1-1: *MPO female plug connector, down-angled interface for 2 to 12 fibres*. The MDI shall optically mate with the plug on the optical fiber cabling. Figure 124–7 shows an MPO female plug connector with down-angled interface, and an MDI as an active device receptacle with angled interface.

The MDI shall meet the interface performance specifications of IEC 61753-021-2 for performance level D/2.

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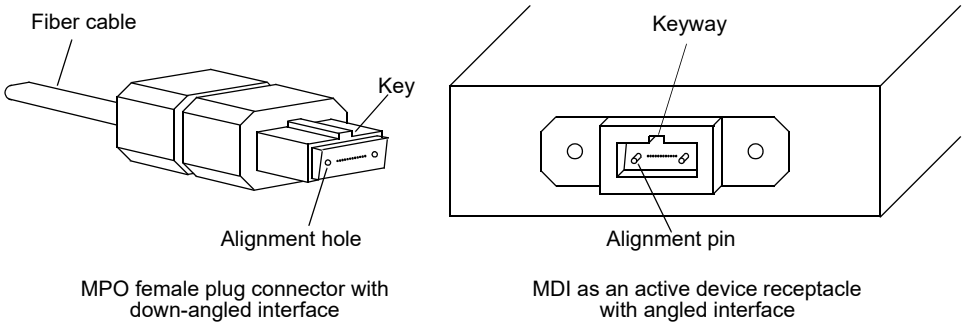

Figure 124–7—MPO female plug with down-angled interface and MDI active device receptacle with angled interface

NOTE—Transmitter compliance testing is performed at TP2 as defined in 124.5.1, not at the MDI.

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124.12 Protocol implementation conformance statement (PICS) proforma for Clause 124, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4[215]

124.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 124, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

124.12.2 Identification

124.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

124.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 124, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[215]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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124.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*INS	Installation / cable	124.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	124.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	124.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	124.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	124.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	124.4	Registers and interface supported	O	Yes [ ] No [ ]

124.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4

124.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 400GBASE-R PCS and PMA	124.1		M	Yes [ ]
F2	Integration with management functions	124.1		O	Yes [ ] No [ ]
F3	Bit error ratio	124.1.1	Meets the BER specified in 124.1.1	M	Yes [ ]
F4	Transmit function	124.5.2	Conveys symbols from PMD service interface to MDI	M	Yes [ ]
F5	Mapping between optical signal and logical signal for transmitter	124.5.2	Highest optical power corresponds to tx_symbol = three	M	Yes [ ]
F6	Receive function	124.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]
F7	Conversion of four optical signals to four electrical signals	124.5.3	For delivery to the PMD service interface	M	Yes [ ]
F8	Mapping between optical signal and logical signal for receiver	124.5.3	Highest optical power corresponds to rx_symbol = three	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F9	Global Signal Detect function	124.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F10	Global Signal Detect behavior	124.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all four lanes	M	Yes [ ]
F11	Lane-by-lane Signal Detect function	124.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 124–4	MD:O	Yes [ ] No [ ] N/A [ ]
F12	PMD reset function	124.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

124.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	124.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	124.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD lane-by-lane transmit disable function	124.5.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_*i* variable	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD_fault function	124.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_transmit_fault function	124.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
M6	PMD_receive_fault function	124.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

124.12.4.3 PMD to MDI optical specifications for 400GBASE-DR4

Item	Feature	Subclause	Value/Comment	Status	Support
DR1	Transmitter meets specifications in Table 124–6	124.7.1	Per definitions in 124.8	M	Yes [ ]
DR2	Receiver meets specifications in Table 124–7	124.7.2	Per definitions in 124.8	M	Yes [ ]

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124.12.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	124.8	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and SMSR	124.8.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	124.8.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA measurements	124.8.4	Each lane	M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	124.8.5	Each lane	M	Yes [ ]
OM6	Extinction ratio	124.8.6	Each lane	M	Yes [ ]
OM7	Transmitter transition time	124.8.7	Each lane	M	Yes [ ]
OM8	Stressed receiver sensitivity	124.8.10	Each lane	M	Yes [ ]

124.12.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	124.9.1	Conforms to IEC 60950-1	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	124.9.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	124.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

124.12.4.6 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	124.11	Meets requirements specified in Table 124–11	INS:M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	124.11.2.2	Meets requirements specified in Table 124–13	INS:M	Yes [ ] N/A [ ]
OC3	MDI layout	124.11.3.1	Optical lane assignments per Figure 124–6	M	Yes [ ]
OC4	MDI dimensions	124.11.3.2	Per IEC 61754-7-1 interface 7-1-9	M	Yes [ ]
OC5	Cabling connector dimensions	124.11.3.2	Per IEC 61754-7-1 interface 7-1-1	INS:M	Yes [ ] N/A [ ]
OC6	MDI mating	124.11.3.2	MDI optically mates with plug on the cabling	M	Yes [ ]

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125. Introduction to 2.5 Gb/s and 5 Gb/s networks

125.1 Overview

125.1.1 Scope

This clause describes the general requirements for 2.5 Gigabit and 5 Gigabit Ethernet. 2.5 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 2.5 Gb/s, coupled with any IEEE 802.3 2.5GBASE Physical Layer implementation. 5 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 5 Gb/s, coupled with any IEEE 802.3 5GBASE Physical Layer implementation. 2.5 Gb/s and 5 Gb/s Physical Layer devices, such as those specified in Table 125–1, provide a bit error ratio (BER) better than or equal to 10^{-12} at the MAC/PLS service interface.

2.5 Gigabit and 5 Gigabit Ethernet are defined for full duplex operation only.

125.1.2 Relationship of 2.5 Gigabit and 5 Gigabit Ethernet to the ISO OSI reference model

2.5 Gigabit and 5 Gigabit Ethernet couple the IEEE 802.3 MAC to a family of 2.5 Gb/s and 5 Gb/s Physical Layers. The relationships among 2.5 Gigabit and 5 Gigabit Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 125–1. While this standard defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The XGMII, which, when implemented as a logical interconnection port between the MAC sublayer and the Physical Layer device (PHY), uses a 32-bit-wide data path as specified in Clause 46.

b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit wide data path as specified in Clause 45.

c) The MDI as specified in Clause 126 for 2.5GBASE-T and 5GBASE-T uses a 4-lane data path.

d) The MDI as specified in Clause 128 for 2.5GBASE-KX and Clause 130 for 5GBASE-KR uses a single-lane data path.

e) The MDI as specified in Clause 149 for 2.5GBASE-T1 and 5GBASE-T1 uses a single-lane data path.

125.1.3 Nomenclature

The nomenclature employed by the 2.5 Gigabit and 5 Gigabit Physical Layers is explained in the following paragraphs.

The alpha-numeric prefix 2.5GBASE in the port type (e.g., 2.5GBASE-T) represents a family of Physical Layer devices operating at a speed of 2.5 Gb/s. The alpha-numeric prefix 5GBASE in the port type (e.g., 5GBASE-T) represents a family of Physical Layer devices operating at a speed of 5 Gb/s.

2.5GBASE-T represents Physical Layer devices using Clause 126 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, for transmitting 2.5 Gb/s Ethernet over a point-to-point 4-pair balanced twisted-pair medium. 2.5GBASE-T uses low density parity check (LDPC) FEC in its Physical Coding Sublayers mapped to a PAM16 constellation for transmission on 4-pair, twisted-pair copper cabling.

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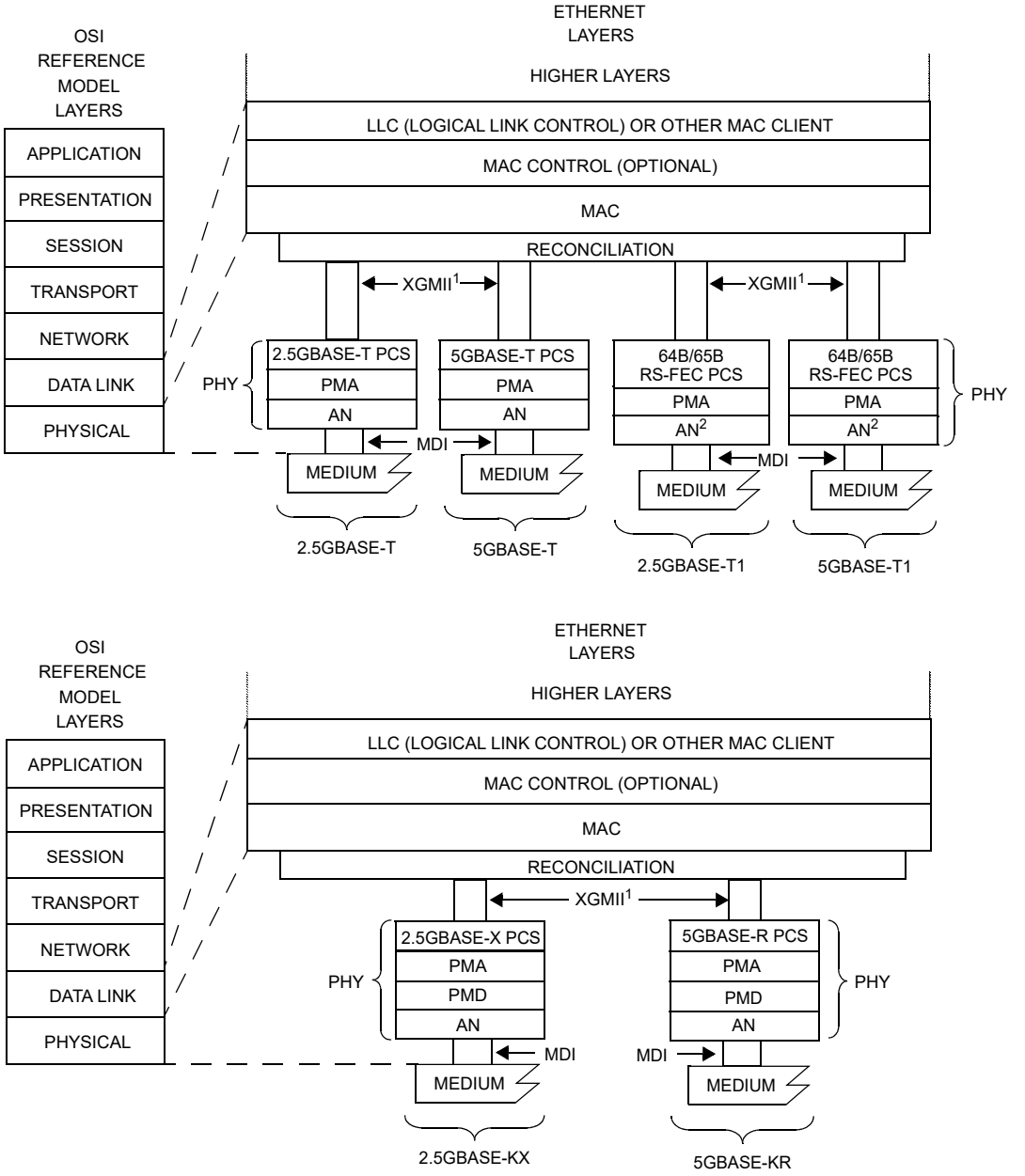

AN = AUTO-NEGOTIATION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
NOTE 1 – XGMII IS OPTIONAL
NOTE 2 – AUTO-NEGOTIATION IS OPTIONAL

Figure 125–1—Architectural positioning of 2.5 Gigabit and 5 Gigabit Ethernet

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5GBASE-T represents Physical Layer devices using Clause 126 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, for transmitting 5 Gb/s Ethernet over a point-to-point 4-pair balanced twisted-pair medium. 5GBASE-T uses low density parity check (LDPC) FEC in its Physical Coding Sublayers mapped to a PAM16 constellation for transmission on 4-pair, twisted-pair copper cabling.

2.5GBASE-X refers to a specific family of Physical Layer devices based upon the 8B/10B data coding method specified in Clause 127. The 2.5GBASE-X family is composed of 2.5GBASE-KX.

5GBASE-R refers to a specific family of Physical Layer devices based upon the 64B/66B data coding method specified in Clause 129. The 5GBASE-R family is composed of 5GBASE-KR.

2.5GBASE-T1 represents Physical Layer devices using Clause 149 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, for transmitting 2.5 Gb/s Ethernet over a point-to-point single balanced pair of conductors. 2.5GBASE-T1 uses Reed-Solomon FEC in its Physical Coding Sublayers mapped to PAM4 for transmission on a single balanced pair of conductors.

5GBASE-T1 represents Physical Layer devices using Clause 149 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, for transmitting 5 Gb/s Ethernet over a point-to-point single balanced pair of conductors. 5GBASE-T1 uses Reed-Solomon FEC in its Physical Coding Sublayers mapped to PAM4 for transmission on a single balanced pair of conductors.

125.1.4 Physical Layer signaling systems

Physical Layer devices listed in Table 125–1 are defined for operation at 2.5 Gb/s and 5 Gb/s.

Table 125–1—2.5 Gb/s and 5 Gb/s PHYs

Name	Description
2.5GBASE-KX	2.5 Gb/s PHY using 2.5GBASE-X encoding over one lane of an electrical backplane (see Clause 128)
2.5GBASE-T	2.5 Gb/s PHY using LDPC encoding and PAM16 modulation over balanced twisted-pair structured cabling systems (see Clause 126)
2.5GBASE-T1	2.5 Gb/s PHY using Reed–Solomon encoding and PAM4 modulation over a single balanced pair of conductors (see Clause 149)
5GBASE-KR	5 Gb/s PHY using 5GBASE-R encoding over one lane of an electrical backplane (see Clause 130)
5GBASE-T	5 Gb/s PHY using LDPC encoding and PAM16 modulation over balanced twisted-pair structured cabling systems (see Clause 126)
5GBASE-T1	5 Gb/s PHY using Reed–Solomon encoding and PAM4 modulation over a single balanced pair of conductors (see Clause 149)

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This standard specifies a family of Physical Layer implementations. Table 125–2 specifies the correlation between nomenclature and clauses. Implementations conforming to one or more nomenclatures meet the requirements of the corresponding clauses.

Table 125–2—Nomenclature and clause correlation

Nomenclature	Clause and annex[a]															
	28	46		73	78	98	126	126	127	128	128A	129	130	130A	149	
	Auto-Negotiation	RS	XGMII	Auto-Negotiation	EEE	Auto-Negotiation	2.5GBASE-T PCS/PMA	5GBASE-T PCS/PMA	2.5GBASE-X PCS/PMA	2.5GBASE-KX PMD	2.5GSEI	5GBASE-R PCS/PMA	5GBASE-KR PMD	5GSEI	2.5GBASE-T1 PCS/PMA	5GBASE-T1 PCS/PMA
2.5GBASE-KX		M	O	M	O				M	M	O					
2.5GBASE-T	M	M	O		O		M									
2.5GBASE-T1		M	O		O	O									M	
5GBASE-KR		M	O	M	O							M	M	O		
5GBASE-T	M	M	O		O			M								
5GBASE-T1		M	O		O	O										M

[a]O = Optional, M = Mandatory.

125.2 Summary of 2.5 Gigabit and 5 Gigabit Ethernet sublayers

125.2.1 Reconciliation Sublayer (RS) and Media Independent Interface

2.5 Gigabit and 5 Gigabit Ethernet use the 10 Gigabit Media Independent Interface defined in Clause 46, with the clock scaled to their respective data rates. The physical instantiation of the Media Independent Interface is optional, and can be used to logically connect layers within a device.

The XGMII supports 2.5 Gb/s and 5 Gb/s operation, in addition to 10 Gb/s operation, through its 32-bit wide transmit and receive data paths. The Reconciliation Sublayer (RS) provides a mapping between the signals provided at the Media Independent Interface (XGMII) and the MAC/PLS service definition.

While XGMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for the Physical Coding Sublayers defined in Clause 126.

125.2.2 Physical Coding Sublayer (PCS)

2.5GBASE-T and 5GBASE-T PHYs contain a 65B-LDPC PCS that maps the data transferred across the XGMII interface to 64B/65B blocks encoded in a 2048-bit LDPC frame. This LDPC frame is then mapped to 512 Gray-coded PAM16 symbols for transfer to the 4-lane PMA.

2.5GBASE-X uses the PCS specified in Clause 127, and 5GBASE-R uses the PCS specified in Clause 129.

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2.5GBASE-T1 and 5GBASE-T1 use the PCS specified in Clause 149.

125.2.3 Physical Medium Attachment sublayer (PMA)

The PMA provides a medium-independent means for the PCS to support the use of a range of physical media. The 2.5GBASE-T and 5GBASE-T PMAs perform the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface. The PMA provides a medium-independent means for the PCS to support the use of a range of physical media.

In the case of BASE-T, the 2.5GBASE-T and 5GBASE-T PMAs perform the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface, and the mapping and multiplexing of transmit and receive data streams between the PMA and MDI. In addition, the PMAs perform retiming of the received data stream when appropriate.

2.5GBASE-X uses the PMA specified in Clause 127, and 5GBASE-R uses the PMA specified in Clause 129.

2.5GBASE-T1 and 5GBASE-T1 use the PMA specified in Clause 149.

125.2.4 Auto-Negotiation

125.2.4.1 Auto-Negotiation, type BASE-T

Auto-Negotiation (Clause 28) is used by 2.5GBASE-T and 5GBASE-T devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of a special sequence of fast link pulses.

125.2.4.2 Auto-Negotiation, type Backplane

Auto-Negotiation (Clause 73) is used by 2.5GBASE-X and 5GBASE-R devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of differential Manchester encoding.

125.2.4.3 Auto-Negotiation, type single differential-pair media

Auto-Negotiation (Clause 98) may be used by 2.5GBASE-T1 and 5GBASE-T1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding.

The use of Clause 98 Auto-Negotiation is optional for 2.5GBASE-T1 and 5GBASE-T1 PHYs.

125.2.5 Management interface (MDIO/MDC)

The optional MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMD) and Station Management (STA) entities.

125.2.6 Management

Managed objects, attributes, and actions are defined for all 2.5 Gigabit and 5 Gigabit Ethernet components. These items are defined in Clause 30.

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125.3 Delay Constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. Table 125–3 contains the values of maximum sublayer delay (sum of transmit and receive delays at one end of the link) in bit times as specified in 1.4 and pause_quanta as specified in 31B.2. If a PHY contains an Auto-Negotiation sublayer, the delay of the Auto-Negotiation sublayer is included within the delay of the PMD and medium.

See 31B.3.7 for PAUSE reaction timing constraints for stations at operating speeds of 2.5 Gb/s and 5 Gb/s.

Table 125–3—Sublayer delay constraints

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
2.5GBASE-KX PHY	1 024	2	409.6	See 127.5 and 128.4.
2.5GBASE-T PHY	12 800	25	5120	Does not include delay of cable medium. See 126.11.
2.5GBASE-T1 PHY	10 240	20	4096	See 149.10.
5GBASE-R PCS PMA	3 584	7	716.8	See 129.5.
5GBASE-KR PMD	512	1	102.4	See 130.4.
5GBASE-T PHY	14 336	28	2867.2	Does not include delay of cable medium. See 126.11.
5GBASE-T1 PHY no interleave	10 240	20	2048	See 149.10.
5GBASE-T1 PHY 2x interleave	13 824	27	2764.8	See 149.10.

[a] For 2.5GBASE-T, 2.5GBASE-X, and 2.5GBASE-T1, 1 bit time (BT) is equal to 400 ps and for 5GBASE-T, 5GBASE-R, and 5GBASE-T1, 1 bit time (BT) is equal to 200 ps. (See 1.4.215 for the definition of bit time.)
[b] For 2.5GBASE-T, 2.5GBASE-X, and 2.5GBASE-T1, 1 pause_quantum is equal to 204.8 ns and for 5GBASE-T, 5GBASE-R, and 5GBASE-T1, 1 pause_quantum is equal to 102.4 ns. (See 31B.2 for the definition of pause_quanta.)
[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

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126. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, types 2.5GBASE-T and 5GBASE-T

126.1 Overview

The 2.5GBASE-T and 5GBASE-T PHYs are members of the 2.5 Gb/s and 5 Gb/s Ethernet family of high-speed network specifications respectively. The 2.5GBASE-T PCS, PMA, and baseband medium specifications are intended for operation over balanced twisted-pair structured cabling systems. The 5GBASE-T PCS, PMA, and baseband medium specifications are intended for operation over balanced twisted-pair structured cabling systems. 2.5GBASE-T and 5GBASE-T signaling both require four pairs of balanced cabling as specified in ISO/IEC 11801:2002 and ANSI/TIA-568-C.2.

This clause defines the types 2.5GBASE-T and 5GBASE-T PCS, PMA sublayers, and Medium Dependent Interfaces (MDI). Together, the PCS and PMA sublayers define a Physical Layer device (PHY). Functional, electrical, and mechanical specifications for the type 2.5GBASE-T PMA, 5GBASE-T PMA, and MDI are provided in this clause. This clause also specifies the baseband media used with 2.5GBASE-T and 5GBASE-T. Management functions are optionally accessible through the management interface defined in Clause 45, or equivalent. Please refer to Table 125–2 for associated sublayers and options for assembling a 2.5 Gb/s or 5 Gb/s system with the 2.5GBASE-T or 5GBASE-T PHY, respectively.

This clause also specifies 2.5GBASE-T and 5GBASE-T Low Power Idle (LPI) as part of Energy-Efficient Ethernet (EEE). This allows the PHY to enter a low power mode of operation during periods of low link utilization as described in Clause 78.

2.5GBASE-T and 5GBASE-T PHYs may optionally support a fast retrain mechanism. Implementation of the fast retrain option is recommended. Configurations wishing to disable fast retrain on the link may do so by advertising lack of support during link startup, thus preventing the link partner from attempting fast retrain and potentially dropping the link, see 45.2.7.10.

126.1.1 Nomenclature

The 2.5GBASE-T and 5GBASE-T PHYs described in this clause represent two distinct PHY types that share the same PCS, PMA, and MDI specifications subject to frequency scaling. In order to efficiently describe the two PHYs, the nomenclature 2.5G/5GBASE-T is used to describe specifications that apply to both the 2.5GBASE-T and 5GBASE-T PHYs. Additionally, for parameters that scale with the PHYs data rate, the parameter S is used for scaling. For 2.5GBASE-T, $S = 0.5$ and for 5GBASE-T, $S = 1$.

126.1.2 Relationship of 2.5GBASE-T and 5GBASE-T to other standards

The relationships between the 2.5GBASE-T and 5GBASE-T PHYs, the ISO Open Systems Interconnection (OSI) reference model, and the IEEE 802.3 Ethernet model are shown in Figure 126–1. The PHY sublayers (shown shaded) in Figure 126–1 connect the IEEE 802.3 Ethernet MAC to the medium. The 2.5GBASE-T and 5GBASE-T PHY service interface is the XGMII, which is defined in Clause 46.

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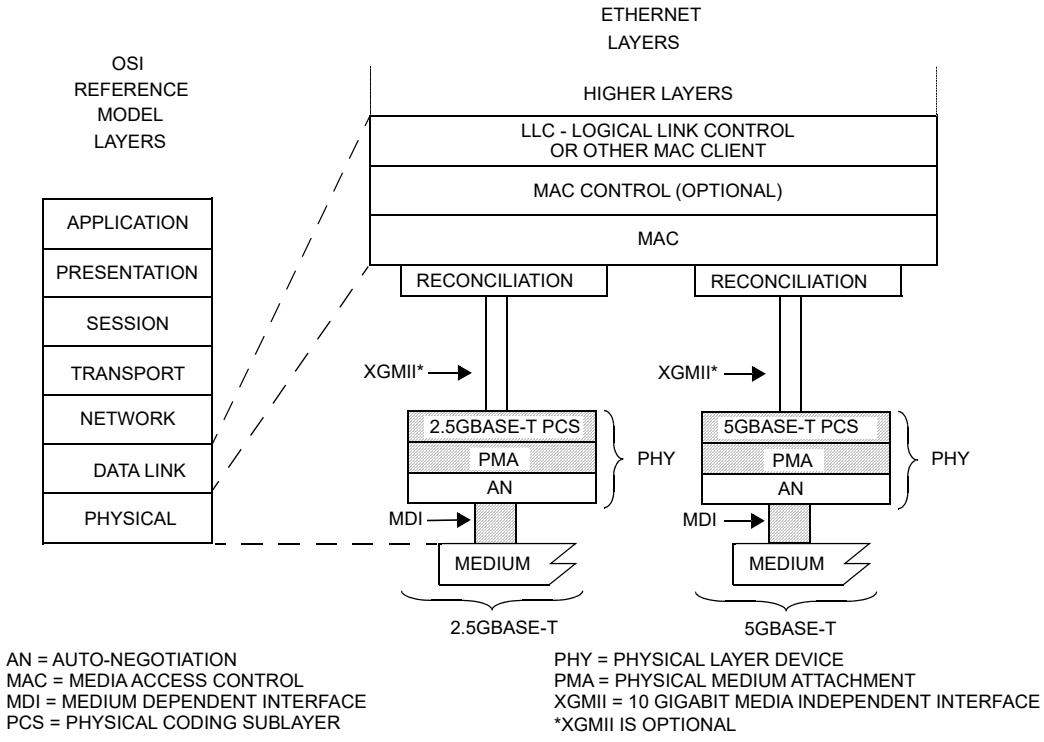

Figure 126–1—Types 2.5GBASE-T and 5GBASE-T PHYs relationship to the ISO Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

126.1.3 Operation of 2.5GBASE-T and 5GBASE-T

The 2.5GBASE-T PHY and 5GBASE-T PHY each employ full duplex baseband transmission over four pairs of balanced twisted-pair structured cabling. The aggregate data rates of 2.5 Gb/s or 5 Gb/s are achieved by transmitting one-quarter of the aggregate data rate in each direction simultaneously on each wire pair, as follows in Figure 126–2. Baseband 16-level PAM signaling with a modulation rate of 200 MBd for 2.5GBASE-T and 400 MBd for 5GBASE-T is used on each of the wire pairs. Ethernet data and control characters are encoded at a rate of 3.125 information bits per PAM16 symbol, along with auxiliary bits. Each transmitted PAM16 symbol is considered as a single one-dimensional (1D) symbol. After link startup, PHY frames consisting of 512 PAM16 symbols are continuously transmitted. The PAM16 symbols are determined by 4-bit labels, each comprising 4 LDPC-encoded bits. The 512 PAM16 symbols of one PHY frame are transmitted as 4×128 PAM16 symbols over the four wire pairs. Data and Control symbols are embedded in a framing scheme that runs continuously after startup of the link. For 2.5GBASE-T, the modulation symbol rate of 200 MBd results in a symbol period of 5 ns, and for 5GBASE-T, the modulation symbol rate of 400 MBd results in a symbol period of 2.5 ns.

A 2.5GBASE-T or 5GBASE-T PHY can be configured either as a MASTER PHY or as a SLAVE PHY. The MASTER-SLAVE relationship between two stations sharing a link segment is established during Auto-Negotiation (see Clause 28, 126.6, Annex 28B, Annex 28C, and Annex 28D). The MASTER PHY uses a local clock to determine the timing of transmitter operations. The MASTER-SLAVE relationship includes loop timing. The SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in Figure 126–3.

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

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2.5GBASE-T and 5GBASE-T PHYs optionally provide support for LPI as part of EEE (see Clause 78). This extension allows PHYs to enter an LPI mode when either the local or link partner system requests low power operation. The transmit and receive functions may enter and leave the LPI mode independently so that both symmetric and asymmetric operation is supported. While the PHY is in the LPI mode, the PHY periodically transmits a refresh signal to allow the remote PHY to refresh its receiver state (e.g., timing recovery, adaptive filter coefficients) and thereby track long-term variation in the timing of the link or the underlying channel characteristics. An easily detectable alert signal is transmitted to signal an end to the LPI mode. The alert signal is followed by a wake signal to enable a rapid transition back to the normal operational mode.

2.5GBASE-T and 5GBASE-T PHYs may optionally support a fast retrain mechanism. This function allows PHYs to quickly recover from link degradation without a normal two-second retrain.

The PCS and PMA are summarized in 126.1.3.1 and 126.1.3.2. The EEE capability is summarized in 126.1.3.3. Figure 126–3 shows the functional block diagram.

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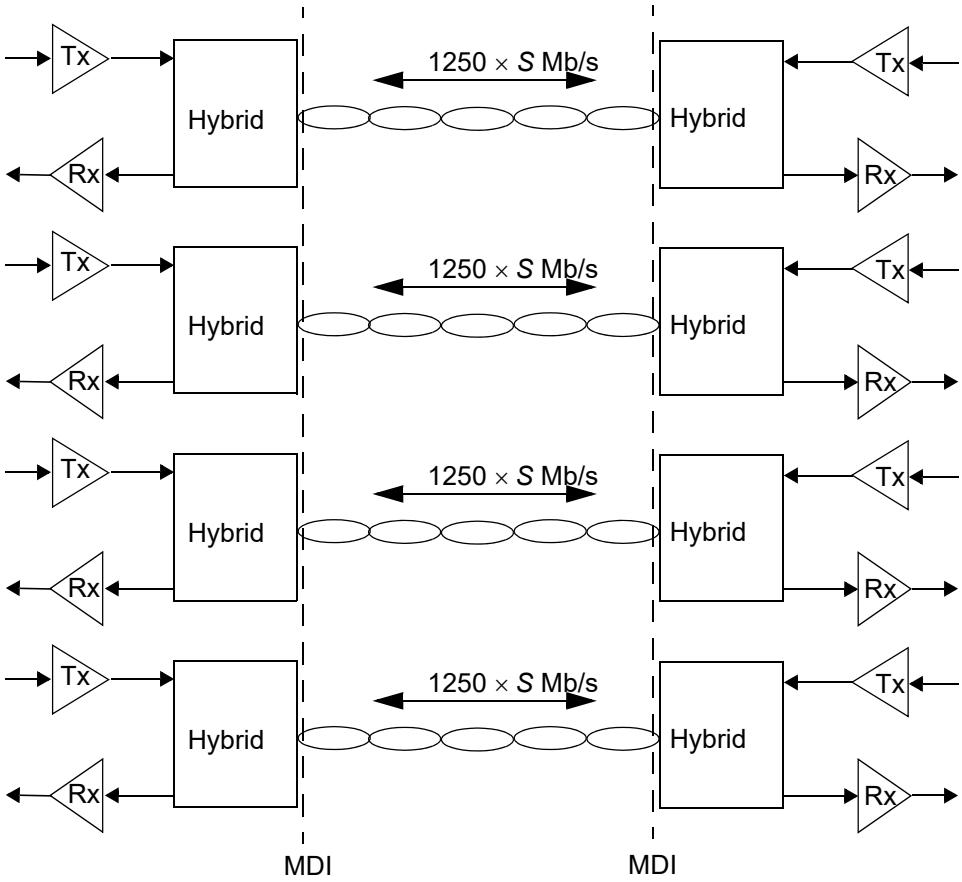

Figure 126–2—2.5GBASE-T and 5GBASE-T topology

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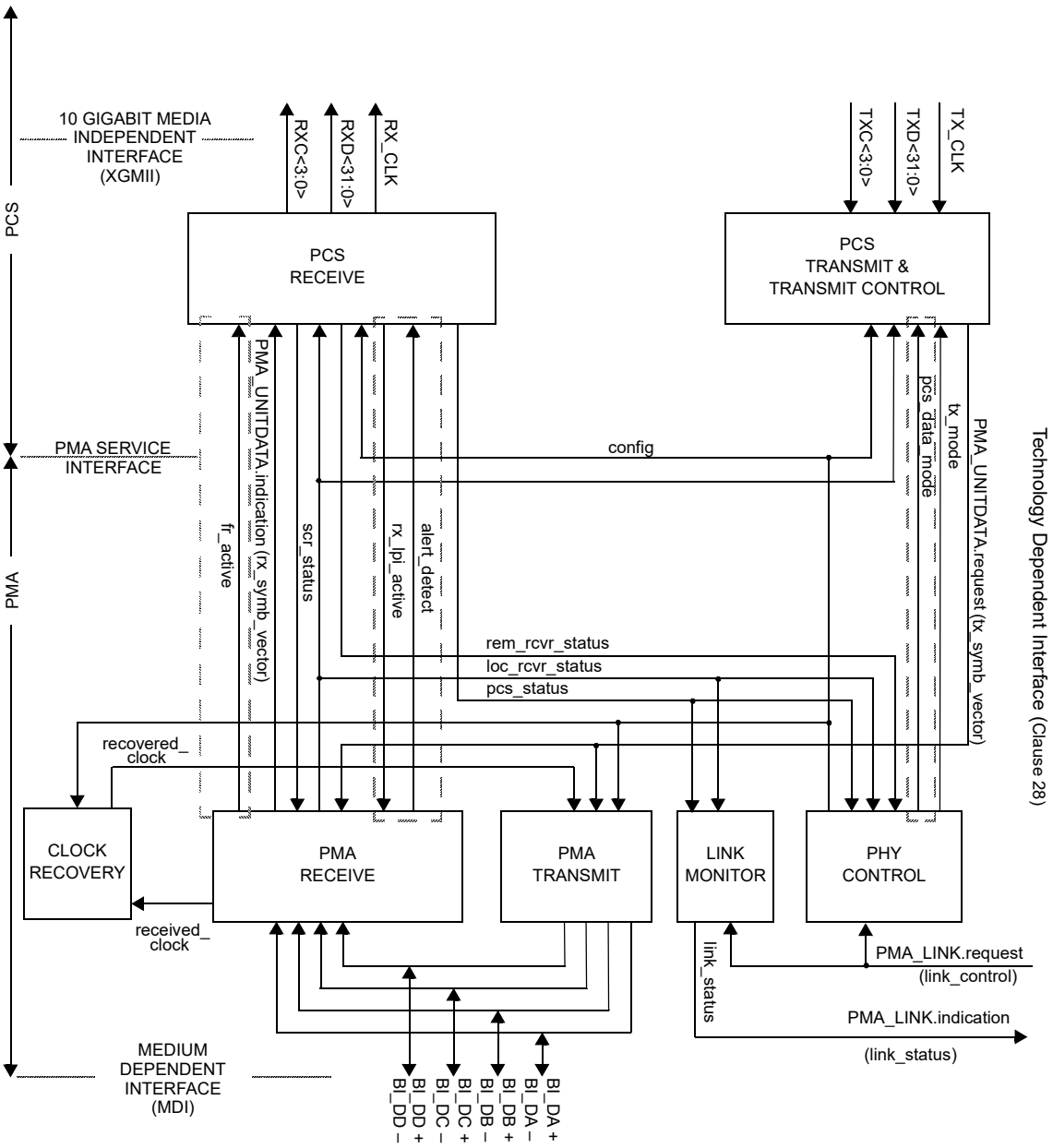

NOTE 1—The recovered_clock arc is shown to indicate delivery of the received clock signal back to PMA TRANSMIT for loop timing.

NOTE 2—pcs_data_mode is required only for the EEE or fast retrain capabilities; alert_detect and rx_lpi_active are only required for the EEE capability; fr_active is only required for the fast retrain capability. Figures and capabilities only required for EEE are noted by dashed boxes.

Figure 126–3—Functional block diagram

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126.1.3.1 Summary of Physical Coding Sublayer (PCS)

The 2.5GBASE-T or 5GBASE-T PCS couples a 10 Gigabit Media Independent Interface (XGMII), as described in Clause 46, to the 2.5GBASE-T or 5GBASE-T Physical Medium Attachment (PMA) sublayer.

In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction (see Figure 126–6), in normal mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. The resulting 65-bit blocks are scrambled and assembled in a group of 25 blocks, yielding an Ethernet payload of $25 \times 65 = 1625$ bits. Additionally, 97 zero-bits are appended, and a leading auxiliary bit is added to obtain a block of 1723 bits.

The 1723 bits are encoded by a systematic LDPC(1723,2048) encoder, which adds 325 LDPC check bits to form an LDPC codeword of 2048 coded bits. The 97 zero-bits are then replaced with vendor-defined random data. Implementers are cautioned that insufficient randomization can impact meeting PMA PSD mask requirements (see 126.5.3.4 for transmit PSD mask definition). The resulting 2048 bit LDPC frame is then divided into 512 4-bit labels, which are mapped into PAM16 modulation symbols.

The obtained PHY frame of 512 PAM16 symbols is passed on to the PMA as PMA_UNITDATA.request. The PMA transmits the PAM16 symbols over the four wire pairs in the form of 128 constituent PAM16 symbols per pair.

In the receive direction (see Figure 126–7), in normal mode, the PCS processes code-groups received from the remote PHY via the PMA in 128 four-dimensional (4D) symbol blocks and maps them to the XGMII service interface in the receive path. In this receive processing scheme, symbol clock synchronization is done by the PMA Receive function.

The signals provided by the PCS at the XGMII conform to the interface requirements of Clause 46.

Details of the PCS functions and state diagrams are covered in 126.3. The interface to the PMA is an abstract message-passing interface specified in 126.2.

126.1.3.2 Summary of Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto the balanced cabling physical medium via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions. The PMA provides full duplex communications at $400 \times S$ MBd over four pairs of balanced cabling up to 100 m in length.

The PMA Transmit function comprises four transmitters to generate continuous time analog signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD, as described in 126.4.3.1. In normal mode, each 4D symbol received from the PCS Transmit function undergoes multiple stages of processing. First the symbol goes through a Tomlinson-Harashima precoder (THP), which maps the PAM16 input (as described in 126.3.2.2.18) in each dimension of the 4D symbol into a quasi-continuous discrete-time value in the range $-16 \le x < 16$. This THP-processed 4D symbol stream may be further processed by a digital transmit filter and is then passed on to four digital-to-analog converters (DACs). The DAC outputs may be further processed with continuous time filters to roll off the high-frequency spectral response to limit high-frequency emissions and are then applied to each of the four balanced pairs via the MDI port.

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The PMA Receive function comprises four independent receivers for pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD, as described in 126.4.3.2. The receivers are responsible for acquiring symbol timing and, when operating in normal mode, for canceling echo, near-end crosstalk, far-end crosstalk, and equalizing the signal. The 4D symbols are provided to the PCS Receive function via the PMA_UNITDATA.indication message. The PMA also contains functions for Link Monitor.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control begins following the completion of Auto-Negotiation and provides the startup functions required for successful 2.5GBASE-T and 5GBASE-T operation. PHY Control determines whether the PHY operates in a normal mode, enabling data transmission over the link segment, or whether the PHY sends special PAM2 code-groups that are used in the training mode.

PMA functions and state diagrams are specified in 126.4. PMA electrical specifications are given in 126.5.

The PMA sublayer may also support a fast retrain function. The fast retrain function is specified in 126.4.2.5.16.

126.1.3.3 Summary of EEE capability

A 2.5GBASE-T or 5GBASE-T PHY may optionally support the EEE capability, as described in 78.1.4. The EEE capability is a mechanism by which 2.5GBASE-T and 5GBASE-T PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter this mode of operation after reaching PCS data mode. Each direction of the full duplex link is able to enter and exit the LPI mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full duplex link is in a period of low utilization. No data frames are lost or corrupted during the transition to or from the LPI mode.

In the transmit direction, the transition to the LPI transmit mode begins when the PCS transmit function detects an LPI control character in all four lanes of two consecutive transfers of TXD[31:0] that is then mapped into a single 64B/65B block, according to the position in the 2.5GBASE-T or 5GBASE-T LDPC frame. Following this event a sleep signal is transmitted by the PMA. The sleep signal is composed of LDPC frames that contain only LP_IDLE 64B/65B blocks. The sleep signal indicates to the link partner that the transmit function of the PHY is entering the LPI transmit mode. Immediately after the transmission of the sleep frames, the transmit function of the local PHY enters the LPI transmit mode. While the transmit function is in the LPI mode the PHY may disable data path and control logic to save additional power. Periodically the transmit function of the local PHY transmits refresh frames that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity. The LPI mode begins with quiet signaling or with a full refresh period. Partial refreshes (defined as a refresh signal shorter than eight LDPC frames) that immediately follow the transition to the LPI mode are replaced with quiet signaling. The quiet-refresh cycle continues until the PCS function detects IDLE characters on the XGMII. These characters signal to the PHY that the LPI transmit mode should end. The PMA Transmit function in the PHY then sends an alert message to the link partner. The alert signal begins on a LDPC 2-frame 256 4D-symbol boundary aligned to the inversion on pair A during PMA training, but has no fixed relationship to the quiet-refresh cycle. The alert signal wakes the link partner from sleep. The alert signal is followed by a wake signal, composed of LDPC frames containing only IDLE 64B/65B blocks. After a short recovery time the normal operational mode is resumed.

In the receive direction the transition to the LPI mode is triggered when the PCS Receive function detects LPI control characters within received LDPC frames. This indicates that the link partner is about to enter the LPI transmit mode. Following these frames the link partner ceases transmission and begins quiet-refresh signaling. During the quiet time it is highly recommended that the local receiver power off circuits to reduce power consumption. Periodically the link partner transmits refresh frames that are used by the receiver to update adaptive coefficients and timing circuits. This quiet-refresh cycle continues until the link partner transmits the alert signal, initiating a transition back to the normal operational mode. The alert signal is

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detected in the PMA and signals that normal data frames will follow. The alert signal is followed by a wake signal that allows the local receiver time to prepare for the normal operational mode. The wake signal is composed of repeated IDLE 64B/65B blocks. After a short recovery time the normal operational mode is resumed.

Support for the EEE capability is advertised in the Infofield (Octet 12 bit 7) during link startup. Transitions to and from the LPI transmit mode are controlled via XGMII signaling. Transitions to and from the LPI receive mode are controlled by the link partner using sleep, alert, and wake signaling.

The PCS 64B/65B Transmit state diagram in Figure 126–14 and Figure 126–15 includes additional states for EEE. The PCS 64B/65B Receive state diagram in Figure 126–16 and Figure 126–17 includes additional states for EEE. The EEE Transmit state diagram is contained in the PCS Transmit function and is specified in Figure 126–18.

126.1.4 Signaling

2.5GBASE-T and 5GBASE-T signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over each wire pair. The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to 4D symbols in the transmit path.
c) Algorithmic mapping from the received 4D signals on the MDI port to RXD<31:0> and RXC<3:0> on the XGMII interface.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions on any pair combination.
f) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
g) Block framing and other control signals.
h) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
i) Ability to automatically detect and correct for pair swapping and crossover connections.
j) Ability to automatically detect and correct for incorrect polarity in the connections.
k) Ability to automatically correct for differential delay variations across the wire-pairs.
l) Ability to support refresh, quiet and alert signaling during LPI operation.

The PHY operates in two modes—normal mode or training mode. In normal mode, PCS generates a continuous stream of 4D symbols that are transmitted via the PMA at one of eight power levels. In training mode, the PCS is directed to generate only PAM2 symbols for transmission by the PMA, which enable the receiver at the other end to train until it is ready to operate in normal mode. (See 126.3.2.2 for description of PCS transmit modes.)

PHYs may also support the EEE capability as described in 126.1.3.3. Transitions to the LPI mode are supported after reaching normal mode.

126.1.5 Interfaces

All 2.5GBASE-T and 5GBASE-T PHY implementations are compatible at the MDI and at the XGMII, if implemented. Implementation of the XGMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not.

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126.1.6 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

Default initializations, unless specified, are left to the implementer.

126.2 2.5GBASE-T and 5GBASE-T service primitives and interfaces

2.5GBASE-T and 5GBASE-T transfer data and control information across the following four service interfaces:

a) 10 Gigabit Media Independent Interface (XGMII)
b) Technology Dependent Interface
c) PMA service interface
d) Medium dependent interface (MDI)

The XGMII is specified in Clause 46; the Technology Dependent Interface is specified in Clause 28. The PMA service interface is defined in 126.2.2 and the MDI is defined in 126.8.

126.2.1 Technology Dependent Interface

2.5GBASE-T and 5GBASE-T use the following service primitives to exchange status indications and control signals across the Technology Dependent Interface as specified in Clause 28:

PMA_LINK.request (link_control)

PMA_LINK.indication (link_status)

126.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation algorithm to enable and disable operation of the PMA as specified in 28.2.6.2.

126.2.1.1.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PMA reports link_status=FAIL. PHY processes are disabled.
DISABLE	Set by the Auto-Negotiation algorithm in the event fast link pulses are detected. PHY processes are disabled. This allows the Auto-Negotiation algorithm to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions.

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126.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in Clause 28.

126.2.1.1.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as defined in 126.4.2.6.

126.2.1.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 28.2.6.1. This primitive informs the Auto-Negotiation algorithm about the status of the underlying link.

126.2.1.2.1 Semantics of the primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on one of two values: FAIL or OK.

FAIL	No valid link established.
OK	The Link Monitor function indicates that a valid 2.5GBASE-T or 5GBASE-T link is established. Reliable reception of signals transmitted from the remote PHY is possible.

126.2.1.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 126–29.

126.2.1.2.3 Effect of receipt

Auto-Negotiation uses this primitive to detect a change in link_status as described in Clause 28.

126.2.2 PMA service interface

2.5GBASE-T and 5GBASE-T use the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication (tx_mode)

PMA_CONFIG.indication (config)

PMA_UNITDATA.request (tx_symb_vector)

PMA_UNITDATA.indication (rx_symb_vector)

PMA_SCRSTATUS.request (scr_status)

PMA_PCSSTATUS.request (pcs_status)

PMA_RXSTATUS.indication (loc_rcvr_status)

PMA_REMRXSTATUS.request (rem_rcvr_status)

EEE-capable PHYs additionally support the following service primitives:

PMA_ALERTDETECT.indication (alert_detect)

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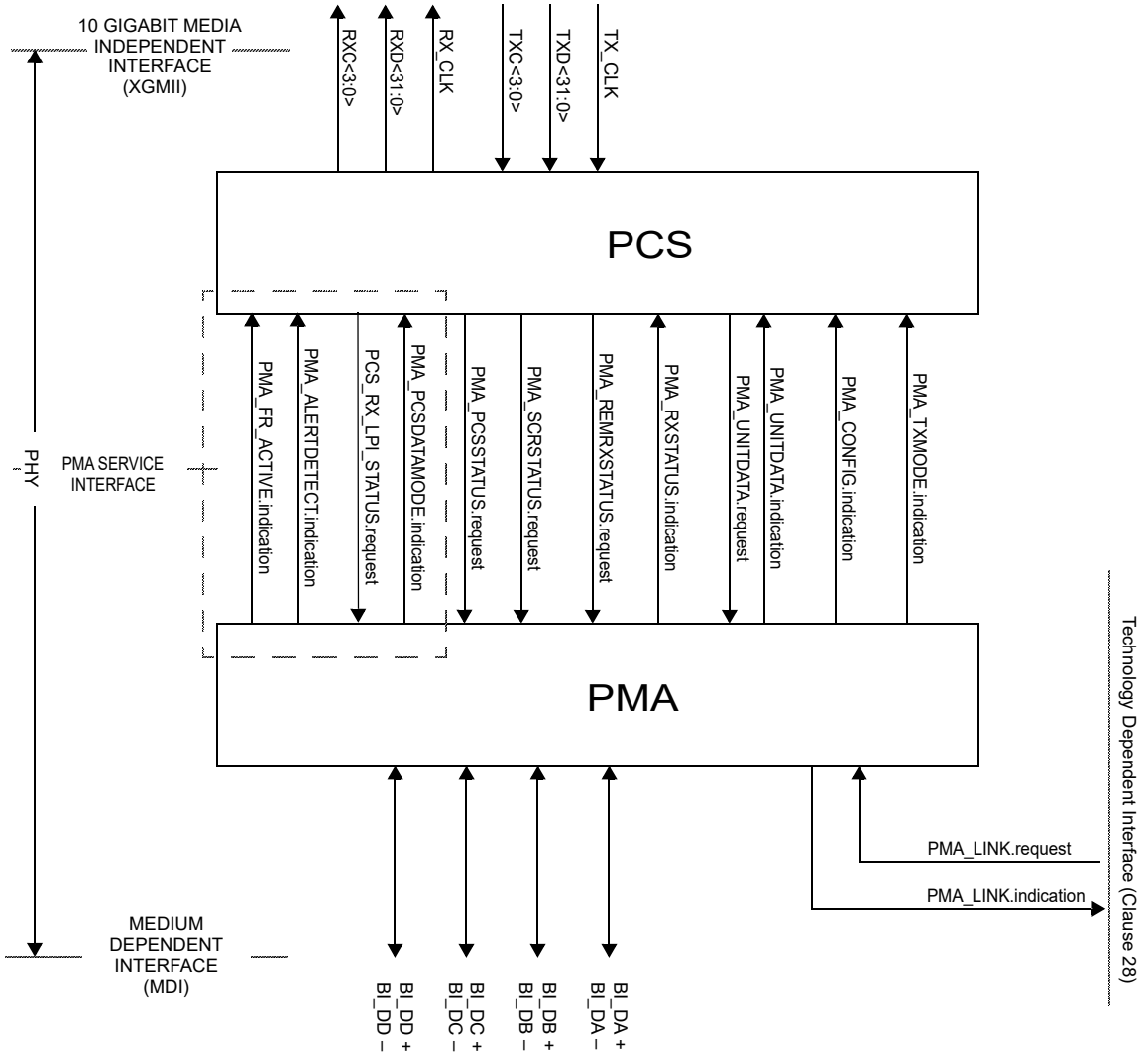
PCS_RX_LPI_STATUS.request (rx_lpi_active)

PMA_PCSDATAMODE.indication (PCS_data_mode)

Fast retrain capable PHYs additionally support the following service primitive:

PMA_FR_ACTIVE.indication (fr_active)

The use of these primitives is illustrated in Figure 126–4. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 126–4.



NOTE 1—PMA_PCSDATAMODE.indication is required only for the EEE or fast retrain capabilities.

NOTE 2—PMA_ALERTDETECT.indication and PCS_RX_LPI_STATUS.request are only required for the EEE capability.

NOTE 3—PMA_FR_ACTIVE.indication is only required for the fast retrain capability.

Figure 126–4—2.5GBASE-T and 5GBASE-T service interfaces

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126.2.2.1 PMA_TXMODE.indication

The transmitter in a 2.5GBASE-T or 5GBASE-T link normally sends over the four pairs, 4D symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

126.2.2.1.1 Semantics of the primitive

PMA_TXMODE.indication (tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of code-groups the PCS should be transmitting. The parameter tx_mode can take on one of the following three values of the form:

SEND_N	This value is continuously asserted when transmission of sequences of 4D symbols representing an XGMII data stream in normal mode.
SEND_T	This value is continuously asserted in case transmission of sequences of code-groups representing the training mode is to take place.
SEND_Z	This value is continuously asserted in case transmission of zeros is required.

126.2.2.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

126.2.2.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 126.3.2.2.

126.2.2.2 PMA_CONFIG.indication

Each PHY in a 2.5GBASE-T or 5GBASE-T link is capable of operating as a MASTER PHY and as a SLAVE PHY. MASTER-SLAVE configuration is determined during Auto-Negotiation (126.6.1). The result of this negotiation is provided to the PMA.

126.2.2.2.1 Semantics of the primitive

PMA_CONFIG.indication (config)

PMA_CONFIG.indication specifies to PCS and PMA Transmit via the parameter config whether the PHY operates as a MASTER PHY or as a SLAVE PHY. The parameter config can take on one of the following two values of the form:

MASTER	This value is continuously asserted when the PHY operates as a MASTER PHY.
SLAVE	This value is continuously asserted when the PHY operates as a SLAVE PHY.

126.2.2.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in config.

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126.2.2.2.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter config.

126.2.2.3 PMA_UNITDATA.request

This primitive defines the transfer of code-groups in the form of the tx_symb_vector parameter from the PCS to the PMA. The code-groups are obtained in the PCS Transmit function using the encoding rules defined in 126.3.2.2 to represent XGMII data and control streams or other sequences.

126.2.2.3.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. For EEE-capable PHYs, the vector also requests the PMA to send the ALERT signal during LPI. The tx_symb_vector parameter takes on the following form:

SYMB_4D	A vector of four multi-level symbols, one for each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. In normal operation, each symbol may take on one of the values in the set {–15, –13, –11, –9, –7, –5, –3, –1, 1, 3, 5, 7, 9, 11, 13, 15}. The symbols may additionally take the value 0 when zeros are to be transmitted in the following two cases: 1) when PMA_TXMODE.indication is SEND_Z during PMA training, and 2) after data mode is reached, the transmit function is in the LPI transmit mode and lpi_tx_mode is QUIET
ALERT	A vector used to indicate that the PMA should transmit the alert sequence. ALERT is asserted for a time equal to 8 LDPC frames.

The symbols that are elements of tx_symb_vector are called, according to the pair on which each is transmitted, tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD].

126.2.2.3.2 When generated

The PCS generates PMA_UNITDATA.request synchronously with every transmit clock cycle.

126.2.2.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols after processing with the THP, the transmit filter and other specified PMA Transmit processing. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD for canceling the echo and near-end crosstalk (NEXT).

126.2.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of code-groups in the form of the rx_symb_vector parameter from the PMA to the PCS.

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126.2.2.4.1 Semantics of the primitive

PMA_UNITDATA.indication (rx_symb_vector)

During reception the PMA_UNITDATA.indication simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on each of the four receive pairs BI_DA, BI_DB, BI_DC, and BI_DD. The rx_symb_vector parameter takes on the following form:

SYMB_4D A vector of the four 1D symbols that is the receiver's best estimate of the symbols that were sent by the remote transmitter across the four pairs with reliability measures.

126.2.2.4.2 When generated

The PMA generates PMA_UNITDATA.indication (SYMB_4D) messages synchronously every four symbols received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is $S \times 400$ MHz, as governed by the recovered clock.

126.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

126.2.2.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the training mode descrambler has achieved synchronization.

126.2.2.5.1 Semantics of the primitive

PMA_SCRSTATUS.request (scr_status)

The scr_status parameter can take on one of the following two values of the form:

OK The training mode descrambler has achieved synchronization.

NOT_OK The training mode descrambler is not synchronized.

126.2.2.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

126.2.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 126.4.2.4, 126.4.2.5, and 126.4.6.1.

126.2.2.6 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in data mode.

126.2.2.6.1 Semantics of the primitive

PMA_PCSSTATUS.request (pcs_status)

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The pcs_status parameter can take on one of the following two values of the form:

OK	The PCS is operating reliably in data mode.
NOT_OK	The PCS is not operating reliably in data mode.

126.2.2.6.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

126.2.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 126.4.6.

126.2.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol streams.

126.2.2.7.1 Semantics of the primitive

PMA_RXSTATUS.indication (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of the following two values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

126.2.2.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

126.2.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 126–26 and in 126.2 and 126.4.6.3.

126.2.2.8 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The criterion for setting the parameter rem_rcvr_status is left to the implementer. It can be based, for example, on asserting rem_rcvr_status is NOT_OK until loc_rcvr_status is OK and then asserting the detected value of rem_rcvr_status after proper PCS Receive decoding is achieved.

126.2.2.8.1 Semantics of the primitive

PMA_REMRXSTATUS.request (rem_rcvr_status)

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The rem_rcvr_status parameter can take on one of the following two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

126.2.2.8.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages to indicate a change in rem_rcvr_status on the basis of signals received at the MDI.

126.2.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 126–26.

126.2.2.9 PMA_ALERTDETECT.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY when rx_lpi_active is TRUE. The parameter alert_detect conveys to the PCS receive function information regarding the detection of the LPI alert signal by the PMA receive function. The criterion for setting the parameter alert_detect is left to the implementer.

126.2.2.9.1 Semantics of the primitive

PMA_ALERTDETECT.indication (alert_detect)

The alert_detect parameter can take on one of the following two values of the form:

TRUE	The alert signal has been reliably detected at the local receiver.
FALSE	The alert signal at the local receiver has not been detected.

126.2.2.9.2 When generated

The PMA generates PMA_ALERTDETECT.indication messages to indicate a change in the alert_detect status.

126.2.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in 126.3.2.3, Figure 126–16, and Figure 126–17.

126.2.2.10 PCS_RX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS receive function to indicate the status of the receive link at the local PHY. The parameter PCS_RX_LPI_STATUS.request conveys to the PCS transmit and PMA receive functions information regarding whether the receive function is in the LPI receive mode. The parameter is generated by the Receive 64B/65B state diagram in Figure 126–16.

126.2.2.10.1 Semantics of the primitive

PCS_RX_LPI_STATUS.request (rx_lpi_active)

The rx_lpi_active parameter can take on one of the following two values of the form:

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TRUE	The receive function is in the LPI receive mode.
FALSE	The receive function is not in the LPI receive mode.

126.2.2.10.2 When generated

The PCS generates PCS_RX_LPI_STATUS.request messages to indicate a change in the rx_lpi_active variable as determined by the receive state diagram in Figure 126–16.

126.2.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in 126.3.2.3 and Figure 126–30.

126.2.2.11 PMA_PCSDATAMODE.indication

This primitive indicates whether or not the PCS state diagrams are able to transition from their initialization states. The pcs_data_mode variable is generated by the PMA PHY Control function. It is passed to the PCS Control function via the PMA_PCSDATAMODE.indication primitive.

126.2.2.11.1 Semantics of the primitive

PMA_PCSDATAMODE.indication (pcs_data_mode)

The pcs_data_mode parameter can take on one of the following two values of the form:

TRUE	PHY is in state PCS_Data (see Figure 126–26).
FALSE	PHY is not in state PCS_Data (see Figure 126–26).

126.2.2.11.2 When generated

The PMA PHY Control function generates PMA_PCSDATAMODE.indication messages continuously.

126.2.2.11.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 126.3.2.2.

126.2.2.12 PMA_FR_ACTIVE.indication

This primitive indicates whether or not the PMA is currently performing a fast retrain. The fr_active variable is generated by the PMA PHY Control function. It is passed to the PCS Receive Control function via the PMA_FR_ACTIVE.indication primitive. This primitive is only supported by PHYs with the fast retrain capability.

126.2.2.12.1 Semantics of the primitive

PMA_FR_ACTIVE.indication (fr_active)

The fr_active parameter can take on one of the following two values of the form:

TRUE	PHY is currently performing a fast retrain.
FALSE	PHY is not currently performing a fast retrain.

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126.2.2.12.2 When generated

The PMA PHY Control function generates PMA_FR_ACTIVE.indication messages continuously.

126.2.2.12.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 126–16.

126.3 Physical Coding Sublayer (PCS)

126.3.1 PCS service interface (XGMII)

The PCS service interface allows the 2.5GBASE-T or 5GBASE-T PCS to transfer information to and from a PCS client. The PCS Interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

126.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 126–5, shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 126–5.

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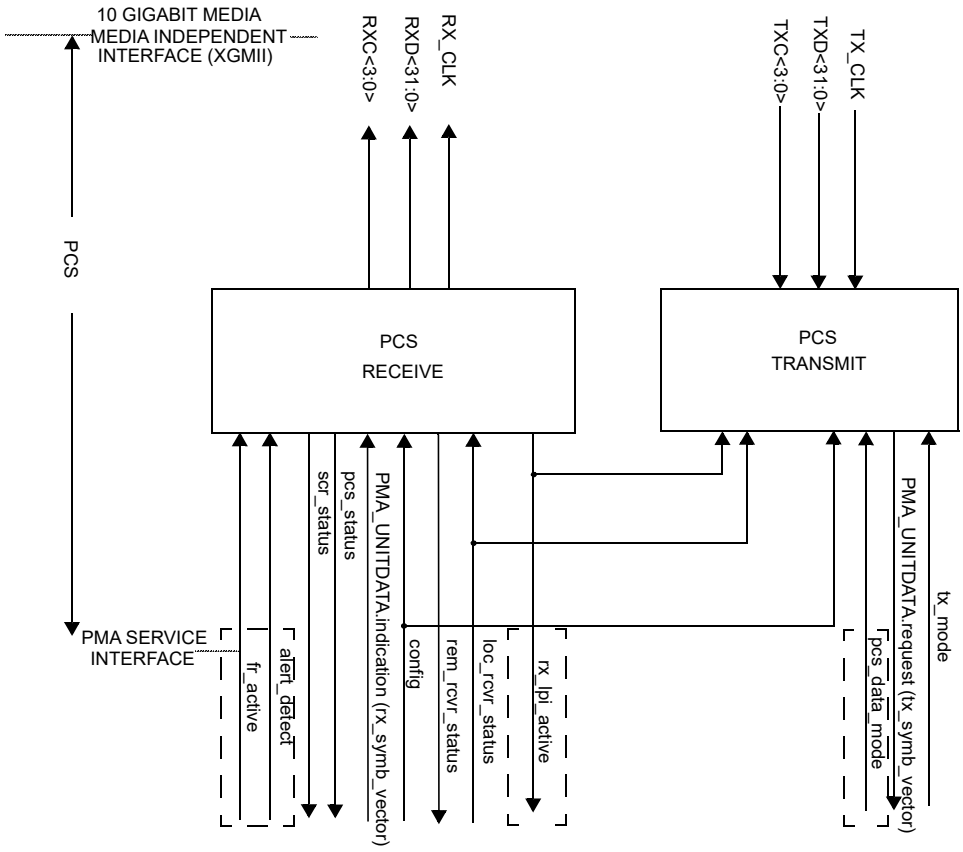

NOTE 1—pcs_data_mode is required only for the EEE or fast retrain capabilities.
NOTE 2—alert_detect and rx_lpi_active are only required for the EEE capability.
NOTE 3—fr_active is only required for the fast retrain capability.

Figure 126–5—PCS reference diagram

126.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 126.3.6.2.2).
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset = true while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

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126.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 126–14 and the PCS Transmit bit ordering in Figure 126–6.

Dashed rectangles in Figure 126–14 and Figure 126–15 are used to indicate states and state transitions in the PCS 64B/65B Transmit state diagram that shall be supported by PHYs with the EEE capability. PHYs without the EEE capability do not support these transitions.

When communicating with the XGMII, the PCS uses a 4-octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment to 64B/65B is performed in the PCS. The PMA sublayer operates independently of block and packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

When the transmit channel is in normal mode, the PCS Transmit process continuously generates 65B blocks based upon the TXD <31:0> and TXC <3:0> signals on the XGMII. The subsequent functions of the PCS Transmit process then scramble the bits of the 65B blocks, pack the resulting scrambled blocks, append 97 zeros, and attach a leading aux channel bit, all of which are then processed by a low density parity check (LDPC) encoder. The appended zeros are then replaced by vendor discretionary randomized bits. The resulting 2048-bit LDPC frame is then mapped into PAM16 symbols. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a code-group (A_n, B_n, C_n, D_n) that is transferred to the PMA via the PMA_UNITDATA.request primitive. The PMA transmits symbols A_n, B_n, C_n, D_n over wire-pairs BI_DA, BI_DB, BI_DC, and BI_DD respectively. The integer, n, is a time index that is introduced to establish a temporal relationship between different symbol periods. A symbol period, T, is 2.5/S ns.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit generates sequences of code-groups (TA_n, TB_n, TC_n, TD_n) defined in 126.3.4.2 to the PMA via the PMA_UNITDATA.request primitive. These code-groups are used for training mode and only transmit the values {–9, 9} to keep the transmit power in the training mode the same as the transmit power in normal mode.

During training mode an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes requests for remote transmitter settings. (See 126.4.2.5.)

In the normal mode of operation, the PMA_TXMODE.indication message has the value SEND_N, and the PCS Transmit function uses a 65B-LDPC coding to generate at each symbol period code-groups that represent data or control. During transmission, the 65B encoded bits are scrambled by the PCS using a PCS scrambler, 97 zero bits and an auxiliary bit are added, then frames are encoded into a code-group of 4D symbols and transferred to the PMA. During data encoding, PCS Transmit utilizes an LDPC frame encoder.

After reaching the normal mode of operation, EEE-capable PHYs may enter the LPI transmit mode under the control of the MAC via the XGMII. The EEE Transmit state diagram is contained within the PCS Transmit function. The EEE capability is described in 126.3.2.2.19.

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126.3.2.2.1 Use of blocks

The PCS translates between XGMII signals and 65-bit blocks inserted within an LDPC frame using a 65B-LDPC coding scheme. The PAM2 PMA training frame synchronization allow establishment of LDPC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. During the LPI mode, LDPC frame boundaries delimit sleep, wake, refresh, quiet, and alert cycles. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 126.3.2.2.2.

126.3.2.2.2 65B-LDPC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters. In addition, the code enables the receiver to achieve PCS synchronization alignment on the incoming PHY bit stream.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 126–6 for transmit and Figure 126–7 for receive. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 126.3.2.2.5 for information on how blocks containing control characters are mapped.

126.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. Control characters other than /O/, /S/, and /T/ are labeled C_0 to C_7. The control character for ordered set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7.

Two consecutive XGMII transfers provides eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfers.

Contents of block type fields, data octets and control characters are shown in hexadecimal notation. The LSB of the equivalent binary value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled TxB<64:0> and RxB<64:0> respectively where TxB<0> and RxB<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

126.3.2.2.4 Transmission order

The PCS Transmit bit ordering shall conform to Figure 126–6. Note that this figure shows the mapping from XGMII to 64B/65B block for a block containing eight data characters.

126.3.2.2.5 Block structure

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an 8-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that

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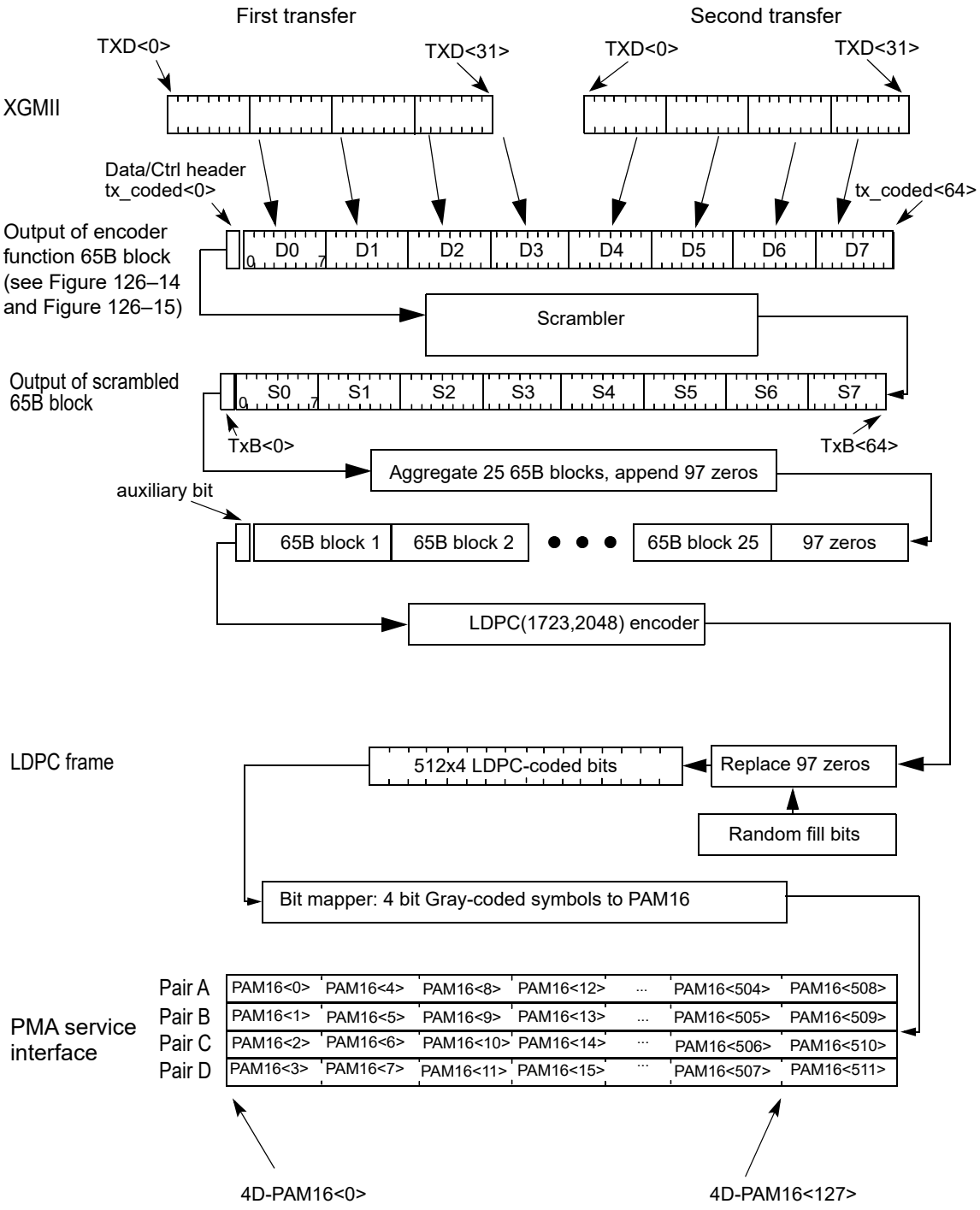

NOTE—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

Figure 126–6—PCS Transmit bit ordering

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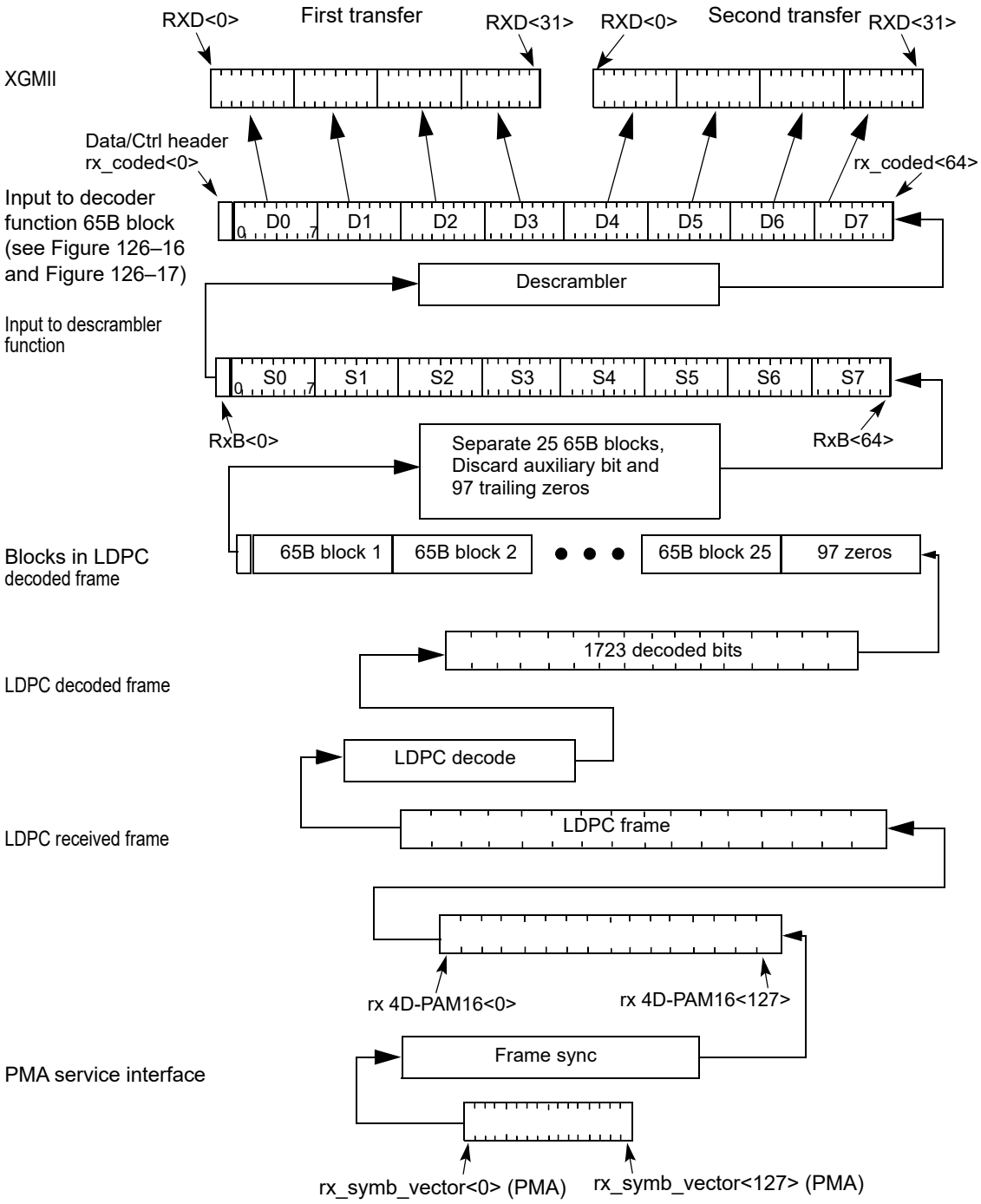

NOTE 1—This figure shows the mapping from a 64B/65B block for a block containing eight data characters to the XGMII.

NOTE 2—Conversion from 4DPAM-16 symbols to bits occurs in the LDPC decoder.

Figure 126–7—PCS Receive bit ordering

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character is implied by the block type field. Other control characters are encoded in a 7-bit control code or a 4-bit O Code. Each control block contains eight characters.

The format of the blocks is as follows in Figure 126–8. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the Input Data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt.

Bits and field positions are shown with the least significant bit on the left. Hexadecimal numbers are shown prepended with '0x', and with the least significant digit on the right. For example the block type field 0x1E is sent as 01111000 representing bits 1 through 8 of the 65-bit block. The least significant bit for each field is placed in the lowest numbered position of the field.

All unused values of block type field are reserved.[216]

126.3.2.2.6 Control codes

The same set of control characters are supported by the XGMII, 2.5GBASE-T and 5GBASE-T PCS. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an 8-bit value). The 2.5GBASE-T and 5GBASE-T PCS encode the start and terminate control characters implicitly by the block type field. The 2.5GBASE-T and 5GBASE-T PCS encode the ordered set control codes using a combination of the block type field and a 4-bit O code for each ordered set. The 2.5GBASE-T and 5GBASE-T PCS encode each of the other control characters into a 7-bit C code.

The control characters and their mappings to 2.5GBASE-T and 5GBASE-T control codes and XGMII control codes are specified in Table 126–1. All XGMII, 2.5GBASE-T, and 5GBASE-T control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

126.3.2.2.7 Ordered sets

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and local fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the XGMII. One kind of ordered set is used for 2.5 and 5 Gigabit Ethernet—the sequence ordered set (see 46.3.4). The sequence ordered set control character is denoted /Q/. An additional ordered set, the signal ordered set, has been reserved and it begins with another control code. The 4-bit O field encodes the control code. See Table 126–1 for the mappings.

126.3.2.2.8 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

[216]The block type field values have been chosen to have a 4-bit Hamming distance between them. The only unused value that maintains the Hamming distance is 0x00.

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Input Data	data ctrl header	Block Payload							
Bit Position: / Data Block Format:	0	1							64
D_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		**Block**							
C_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_0 C_1 C_2 C_3/O_4 D_5 D_6 D_7	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
C_0 C_1 C_2 C_3/S_4 D_5 D_6 D_7	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
O_0 D_1 D_2 D_3/S_4 D_5 D_6 D_7	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
O_0 D_1 D_2 D_3/O_4 D_5 D_6 D_7	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
S_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
O_0 D_1 D_2 D_3/C_4 C_5 C_6 C_7	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
T_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
D_0 T_1 C_2 C_3/C_4 C_5 C_6 C_7	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
D_0 D_1 T_2 C_3/C_4 C_5 C_6 C_7	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
D_0 D_1 D_2 T_3/C_4 C_5 C_6 C_7	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
D_0 D_1 D_2 D_3/T_4 C_5 C_6 C_7	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
D_0 D_1 D_2 D_3/D_4 T_5 C_6 C_7	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
D_0 D_1 D_2 D_3/D_4 D_5 T_6 C_7	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
D_0 D_1 D_2 D_3/D_4 D_5 D_6 T_7	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 126–8—64B/65B block formats

Table 126–1—Control codes

Control character	Notation	XGMII control code	2.5G/5GBASE-T control code	2.5G/5GBASE-T O code
idle	/I/	0x07	0x00	
LPI	/LI/	0x06	0x06	
start	/S/	0xFB	Encoded by block type field	
terminate	/T/	0xFD	Encoded by block type field	
error	/E/	0xFE	0x1E	
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0

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Table 126–1—Control codes *(continued)*

Control character	Notation	XGMII control code	2.5G/5GBASE-T control code	2.5G/5GBASE-T O code
reserved0		0x1C	0x2D	
reserved1		0x3C	0x33	
reserved2		0x7C	0x4B	
reserved3		0xBC	0x55	
reserved4		0xDC	0x66	
reserved5		0xF7	0x78	
Signal ordered set[a]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF

[a]Used by INCITS T11 Fibre Channel.

126.3.2.2.9 LPI (/LI/)

Low power idle (LPI) control characters (/LI/) on the XGMII indicate that the LPI client is requesting operation in the LPI transmit mode. A continuous stream of LPI control characters (/LI/) is used to maintain a link in the LPI transmit mode. Idle control characters (/I/) are used to transition from the LPI transmit mode to the normal mode. PHYs that support EEE respond to the LPI XGMII control characters using the procedure outlined in 126.1.3.3. LPI characters may be added or deleted by the PCS to adapt between clock rates. /LI/ insertion and deletion shall occur in groups of four. /LI/s may be added following low power idle characters. They shall not be added while data is being received.

If EEE is not supported, then /LI/ is not a valid control character.

126.3.2.2.10 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<7:0> and RXD<7:0>). Receipt of an /S/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

126.3.2.2.11 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and within any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

126.3.2.2.12 ordered set (/O/)

The ordered set control characters (/O/) indicate the start of an ordered set. There are two kinds of ordered sets: the sequence ordered set and the signal ordered set (which is reserved). When it is necessary to designate the control character for the sequence ordered set specifically, /Q/ is used. /O/ is only valid on the first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field

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values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered set.

Sequence ordered sets may be deleted by the PCS to adapt between clock rates. Such deletion shall only occur when two consecutive sequence ordered sets have been received and shall delete only one of the two. Only Idles may be inserted for clock compensation. Signal ordered sets are not deleted for clock compensation.

126.3.2.2.13 Error (/E/)

The /E/ is sent whenever an /E/ is received. The /E/ allows physical sublayers such as the PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 126.3.6.2.4 for further information.

126.3.2.2.14 Transmit process

The transmit process generates blocks based upon the TXD<31:0> and TXC<3:0> signals received from the XGMII. Two XGMII data transfers are encoded into each block. 50 XGMII data transfers are encoded into an LDPC frame. It takes 128 PMA_UNITDATA transfers to send an LDPC frame of data. Therefore, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 25:64, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 126–16 and Figure 126–17). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

126.3.2.2.15 PCS Scrambler

The payload of the PCS PHY frame is scrambled with a self-synchronizing scrambler. The scrambler for the MASTER shall produce the same result as the implementation shown in Figure 126–9. This implements the scrambler polynomial:[217]

$$G(x) = 1 + x^{39} + x^{58} \quad (126–1)$$

The scrambler for the SLAVE shall produce the same result as the implementation shown in Figure 126–9. This implements the scrambler polynomial:

$$G(x) = 1 + x^{19} + x^{58} \quad (126–2)$$

The initial seed values for the MASTER and SLAVE are left to the implementer. The scrambler is run continuously on all payload bits.

126.3.2.2.16 LDPC framing and LDPC encoder

The resulting payload of scrambled 25 65B blocks, followed by the 97 zero bits and preceded by 1 auxiliary bit results in a total payload of 25 × 65 + 97 +1 = 1723 bits. The use of the auxiliary bit is for vendor-specific

[217]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (126–1). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.

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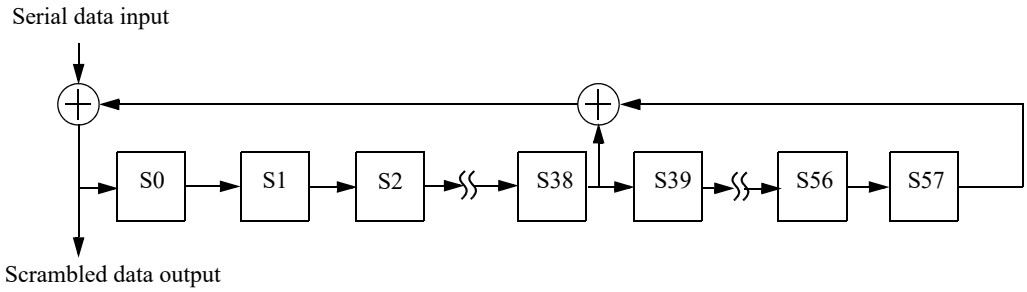
PCS scrambler employed by the MASTER



PCS scrambler employed by the SLAVE

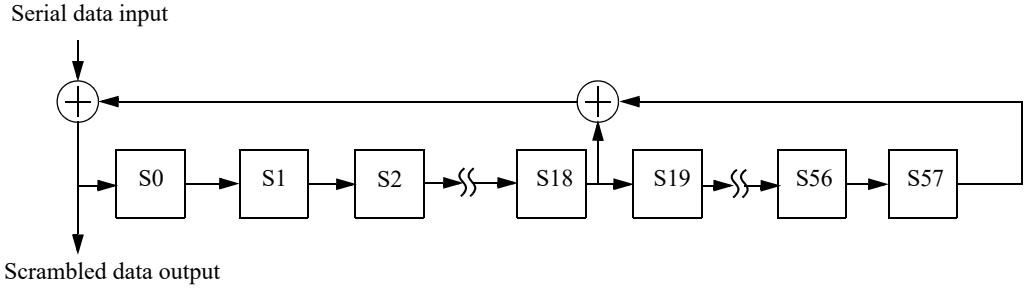


Figure 126–9—MASTER and SLAVE PCS scramblers

communication is outside the scope of this document. For the purposes of this standard it is ignored by the link partner. The 1723 bits shall be encoded by the LDPC(1723, 2048) generator matrix G. G is described in Annex 55A.

The LDPC encoding takes the 1723 bit input code vector $x = [x_0\ x_1\ x_2\ ...\ x_{1722}]$, and shall generate the 2048 bit codeword c represented by the matrix multiplication $c = x \times G$. For both x and c the leftmost element of the vector is the first bit into the LDPC encoder and the first transmitted bit.

126.3.2.2.17 Substitution for zero-bit fill

The 2048 LDPC-coded bits output from the LDPC encoder in Figure 126–6 are then divided into three groups: the first 1626 bits, representing the auxiliary bit and the 25 scrambled 65B blocks of Ethernet payload; the subsequent 97 bits, representing the zero-fill added prior to encoding, and the subsequent 325 LDPC check bits. The group of 97 zero-fill bits are then replaced by vendor discretionary, randomized bits. The randomized fill bits should approximate the autocorrelation properties of the PCS scrambler described in 126.3.2.2.15, so as not to generate tones violating the transmit spectral PSD masks in 126.5.3.4.

126.3.2.2.18 PAM16 bit mapping

The LDPC frame shall be mapped four bits at a time in bit order of transmission into Gray-coded PAM-16 as follows in Table 126–2.

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Table 126–2—PAM16 to Gray coded PAM16 mapping

Bits ($b_0b_1b_2b_3$)	Hex	Level
0100	0x4	+15
0101	0x5	+13
0111	0x7	+11
0110	0x6	+9
0010	0x2	+7
0011	0x3	+5
0001	0x1	+3
0000	0x0	+1
1000	0x8	–1
1001	0x9	–3
1011	0xB	–5
1010	0xA	–7
1110	0xE	–9
1111	0xF	–11
1101	0xD	–13
1100	0xC	–15

126.3.2.2.19 EEE capability

The optional 2.5GBASE-T or 5GBASE-T EEE capability allows compliant PHYs to transition to an LPI mode of operation when link utilization is low.

PHYs that support EEE shall conform to the EEE transmit state diagram, shown in Figure 126–18, within the PCS.

When PCS_Reset is asserted or pcs_data_mode is not asserted, the state diagram enters the TX_NORMAL state.

When a complete 64B/65B block of LPI characters is generated by the PCS transmit function, the PHY transmits the sleep signal to indicate to the link partner that it is transitioning to the LPI transmit mode. If the sleep signal begins on an even LDPC frame boundary aligned to the inversion on pair A during PMA training, then it contains 18 full LDPC frames each composed entirely of LDPC encoded LP_IDLE blocks. If the sleep signal does not begin on an even LDPC frame boundary, then it contains one to two LDPC frames partially composed of LP_IDLE blocks followed by 18 LDPC frames fully composed of LP_IDLE blocks.

Following the transmission of the sleep signal, quiet-refresh signaling begins, as described in 126.3.5.

After the sleep signal is transmitted LPI control characters shall be input to the PCS scrambler continuously until the PCS Transmit Function exits the LPI transmit mode.

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While the PMA asserts SEND_N, the lpi_tx_mode variable shall control the transmit signal through the PMA_UNITDATA.request primitive described as follows:

When the PHY is not in the PCS_Data state, the lpi_tx_mode variable is ignored.

When the lpi_tx_mode variable takes the value NORMAL and the PMA asserts SEND_N, the PCS passes coded data to the PMA via the PMA_UNITDATA.request primitive as described in 126.3.2.2.

When the lpi_tx_mode variable takes the value QUIET and the PMA asserts SEND_N, the PCS passes zeros to the PMA through the PMA_UNITDATA.request primitive.

When the lpi_tx_mode variable takes the value REFRESH_A and the PMA asserts SEND_N, the PCS passes the PMA training signal to the PMA on pair A, to allow both the local and remote PHY to refresh adaptive filters and timing loops. The PCS passes zeros to all other pairs in this condition. REFRESH_B, REFRESH_C and REFRESH_D operate in an analogous manner for the other pairs.

When the lpi_tx_mode variable takes the value ALERT and the PMA asserts SEND_N, the PCS passes the ALERT vector to the PMA.

The quiet-refresh cycle is repeated until codewords other than LP_IDLE are detected at the XGMII. These codewords indicate that the local system is requesting a transition back to the normal operational mode. Following this event, the PMA_UNITDATA.request parameter tx_symb_vector is set to the value ALERT. The alert signal is not synchronized with respect to the quiet-refresh cycle but shall be synchronized so that the alert signal from the PMA begins on a LDPC 2-frame 256 4D-symbol boundary aligned to the inversion on pair A during PMA training.

The PHY also transitions back to the normal operation mode if an error condition occurs. This error condition is defined as the detection of any characters other than LPI or IDLE at the XGMII.

After the alert signal the PCS completes the transition from LPI mode to normal mode by sending a wake signal containing lpi_wake_time LDPC frames composed of IDLE 64B/65B blocks.

lpi_wake_time is a fixed parameter that is defined as 18 LDPC frames as follows in Table 126–3. The maximum PHY wake time when wake is requested before sleep has been completely transmitted is 14.72/S μs (lpi_wake_timer=T_{w_phy} as defined by Clause 78). The maximum PHY wake time when wake is requested after sleep has been completely transmitted is 8.96/S μs.

Table 126–3—LPI wake time

lpi_wake_time	lpi_wake_timer when wake starts before sleep signal is complete		lpi_wake_timer when wake starts after sleep signal is complete	
(frames)	(frames)	(μs)	(frames)	(μs)
18	46	14.72/S	28	8.96/S

126.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B receive state diagram in Figure 126–16 and Figure 126–17 and the PCS Receive bit ordering in Figure 126–7 including compliance with the associated state variables as specified in 126.3.6.

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The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb_vector. The PCS receiver uses knowledge of the encoding rules to correctly align the 65B-LDPC frames. The randomized bits are replaced with known zeros. The received 65B-LDPC frames are decoded with error correction; the auxiliary bit and the trailing zero-fill bits are then stripped; descrambling is then performed. This process generates the 64B/65B block vector rx_coded<64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 126–16 and Figure 126–17). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized to a 25:64 ratio, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primitive to OK.

When the PCS Synchronization process has obtained synchronization, the LDPC frame error ratio (LFER) monitor process monitors the signal quality asserting hi_lfer if excessive LDPC frame errors are detected (LDPC parity error). If 40 consecutive LDPC frame errors are detected, the block_lock flag is de-asserted. When block_lock is asserted and hi_lfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication (loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training sequence includes 1 bit pattern on pair A every 256 PAM2 symbols, which is aligned with the PCS boundary of two LDPC frames. When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.

PHYs with the EEE capability support transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. Transitions to and from the LPI mode are allowed to occur independently in the transmit and receive functions. The PCS receive function is responsible for detecting transitions to and from the LPI receive mode and indicating these transitions using signals defined in 126.2.2.

The link partner signals a transition to the LPI mode of operation by transmitting 18 LDPC frames composed entirely of 64B/65B blocks of /LI/. When blocks of /LI/ are detected at the output of the 64B/65B decoder, rx_lpi_active is asserted by the PCS receive function and the /LI/ character is continuously asserted at the receive XGMII. These frames may be preceded by a frame composed partially of /LI/ characters. After these frames the link partner begins transmitting zeros, and it is recommended that the receiver power down receive circuits to reduce power consumption. The receive function uses LDPC frame counters to maintain synchronization with the remote PHY and receives periodic refresh signals that are used to update coefficients, so that the integrity of adaptive filters and timing loops in the PMA is maintained. LPI signaling is defined in 126.3.5. The quiet-refresh cycle continues until the PMA asserts alert_detect to indicate that the alert signal has been reliably detected. After the alert signal the link partner transmits repeated /I/ characters, representing a wake signal. The PHY receive function sends /I/ to the XGMII for 18 LDPC frame periods and then resumes normal operation.

126.3.2.3.1 Frame and block synchronization

When the receive channel is operating in normal mode, the frame and block synchronization function receives data via 4D-PAM16 PMA_UNITDATA.indication primitives. It shall form a 4D-PAM16 stream from the primitives by concatenating requests with the PAM16s of each primitive in order from

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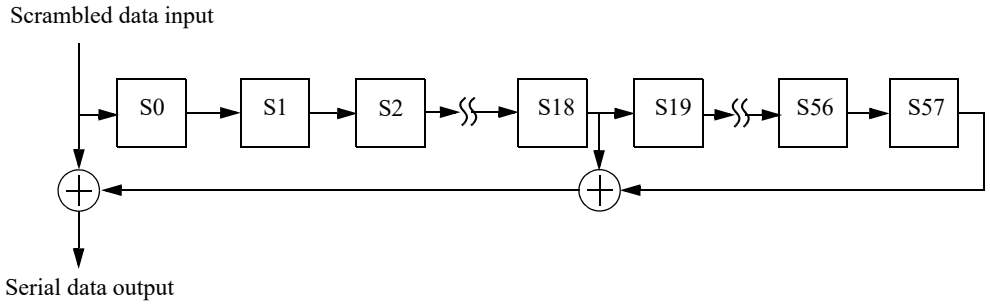
rx_symb_vector<0> to rx_symb_vector<127> (see Figure 126–7). It obtains block_lock to the LDPC frames during the PAM2 training pattern using synchronization bits provided on pair A. The 65-bit blocks are extracted based on their location in the LDPC frame.

126.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. It shall produce the same result as the implementations shown in Figure 126–10 for the MASTER and the SLAVE.

PCS descrambler employed by the MASTER



PCS descrambler employed by the SLAVE

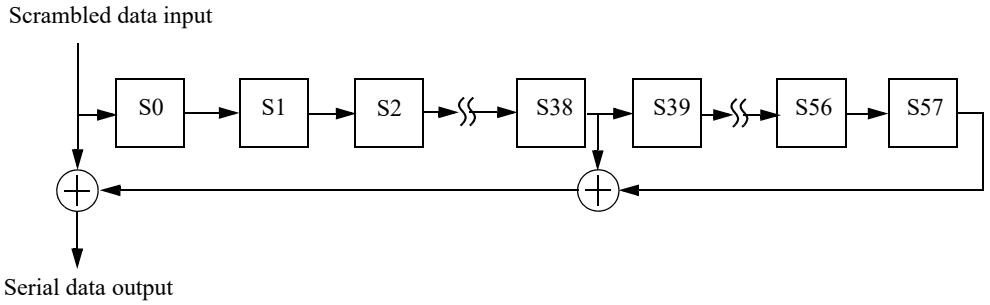


Figure 126–10—MASTER and SLAVE PCS descramblers

126.3.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exists:

a) The block type field contains a reserved value.
b) Any control character contains a value not in Table 126–1.
c) Any O code contains a value not in Table 126–1.
d) The block contains information from the payload of an invalid received PHY frame or the first 64B/65B block following an invalid received PHY frame.

The PCS Receive function shall check the integrity of the LDPC parity bits defined in 126.3.2.2.16. If the check fails the PHY frame is invalid.

R_BLOCK_TYPE of an invalid block is set to E.

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126.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel and remote receiver. When the transmit PCS is operating in test-pattern mode it shall transmit continuously as illustrated in Figure 126–6, with the input to the scrambler set to zero and the initial condition of the scrambler set to any non-zero value. When the receiver PCS is operating in test-pattern mode it shall receive continuously as illustrated in Figure 126–7. After acquiring the self-synchronizing scrambler state, the output of the received scrambled values should ideally be zero. Any nonzero values correspond to receiver bit errors. This mode is further described as test mode 7 in 126.5.2.

126.3.4 PMA training side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling for generating 2-level PAM PMA training sequences as follows in Figure 126–11. An implementation of MASTER and SLAVE PHY side-stream scramblers is shown in the "Main PN sequence" box. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

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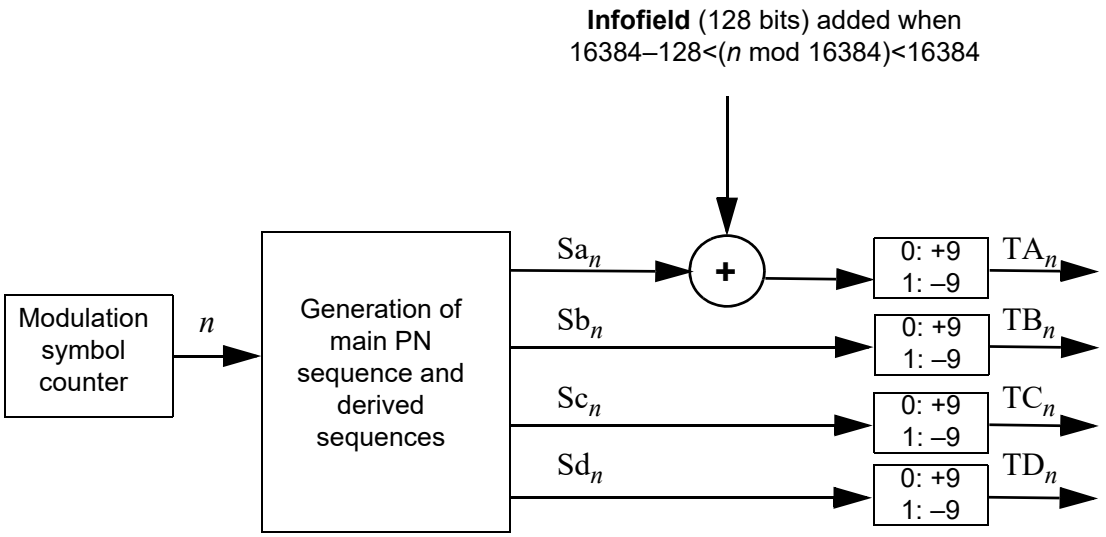

Main PN sequence:

$$Scr_n[32:1] = Scr_{n-1}[31:0]$$

$$Scr_n[0] = \begin{cases} Scr_{n-1}[12] + Scr_{n-1}[32] & \text{if PMA\_CONFIG=MASTER} \\ Scr_{n-1}[19] + Scr_{n-1}[32] & \text{if PMA\_CONFIG=SLAVE} \end{cases}$$

Derived sequences:

$$Sa_n = \begin{cases} Scr_n[0] \oplus 1 & \text{if } n \bmod 256 = 0 \\ Scr_n[0] & \text{otherwise} \end{cases}$$

$$Sb_n = Scr_n[3] \oplus Scr_n[8]$$

$$Sc_n = Scr_n[6] \oplus Scr_n[16]$$

$$Sd_n = Scr_n[9] \oplus Scr_n[14] \oplus Scr_n[19] \oplus Scr_n[24]$$

Figure 126–11—A realization of PMA training PAM2 sequences

126.3.4.1 Generation of bits Sa_n, Sb_n, Sc_n, Sd_n

PMA training signal encoding rules are based on the generation, at time *n*, of the four bits Sa_n, Sb_n, Sc_n, Sd_n. These four bits are generated in a systematic fashion using the bits in $Scr_n[32:0]$, and an auxiliary generating polynomial. For both MASTER and SLAVE PHYs, they are obtained by the same linear combinations of bits stored in the transmit scrambler shift register delay line. These four bits are derived from elements of the same maximum-length shift register sequence of length $2^{33}-1$ as $Scr_n[0]$, but shifted in time. The associated delays are all large and different so that there is no short-term correlation among the bits Sa_n, Sb_n, Sc_n, Sd_n. The four bits are generated using the bit $Scr_n[0]$ and the equations in Figure 126–11 in the "Derived sequences" box.

126.3.4.2 Generation of 4D symbols TA_n, TB_n, TC_n, TD_n

The four bits Sa_n, Sb_n, Sc_n, Sd_n are mapped to a 4D symbol (TA_n, TB_n, TC_n, TD_n) as follows in Figure 126–11.

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The inversion on pair A at 256 intervals ($n = k \times 256, k = 0, 1, 2, \ldots$) defines the LDPC boundary during data mode.

Notice that over the repeating time intervals of 16384 and of length 128, $m \times 16384 - 128 \le n < m \times 16384, m = 1, 2, 3, \ldots$, the PMA training pattern in pair A is XOR'ed with the Infofield. Thus, pair A transmits the Infofield, which communicates to the remote transceiver settings of THP and power backoff and other control information.

126.3.4.3 PMA training mode descrambler polynomials

The PHY shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial $g'_M(x) = 1 + x^{20} + x^{33}$ and the SLAVE PHY shall employ the receiver descrambler generator polynomial $g'_S(x) = 1 + x^{13} + x^{33}$.

126.3.5 LPI signaling

PHYs with EEE capability have transmit and receive functions that can enter and leave the LPI mode independently. The PHY can transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. The transmit function of the PHY initiates a transition to the LPI transmit mode when it generates 64B/65B blocks composed entirely of LPI control characters, as described in 126.3.2.2.19. The transmit function of the link partner signals the transition using the sleep signal. When the transmitter begins to send the sleep signal, it asserts tx_lpi_active and the transmit function enters the LPI transmit mode.

Within the LPI mode PHYs use a repeating quiet-refresh cycle (see Figure 126–12). The first part of this cycle is known as the quiet period and lasts for a time lpi_quiet_time equal to 120 LDPC frame periods. The quiet period is defined in 126.3.5.2. The second part of this cycle is known as the refresh period and lasts for a time lpi_refresh_time equal to 8 LDPC frame periods. The refresh period is defined in 126.3.5.3. A cycle composed of one quiet period and one refresh period is known as a single pair LPI cycle and lasts for a time lpi_qr_time equal to 128 LDPC frame periods. The time taken to complete a quiet-refresh cycle for all four pairs is known as a complete LPI cycle.

lpi_offset, lpi_quiet_time, lpi_refresh_time, lpi_qr_time, and lpi_allpairs_qr_time are timing parameters that are integer multiples of the LDPC frame period. lpi_offset is a fixed value equal to lpi_qr_time/2 that is used to ensure refresh signals are appropriately offset by the link partners.

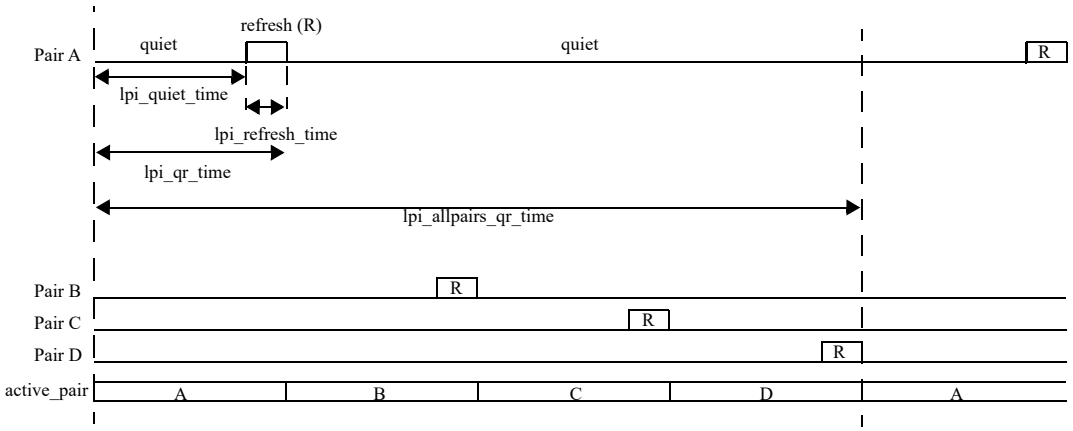

Figure 126–12—Timing periods for LPI signals

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PHYs begin the transition from the LPI receive mode when the alert signal is detected by the PMA as defined in 126.4.2.4.

126.3.5.1 LPI Synchronization

To maximize power savings, maintain link integrity, and ensure interoperability, EEE-capable PHYs synchronize refresh intervals during the LPI mode. The transition to PCS_Test is used as a fixed timing reference for the link partners. Refresh signaling is derived by counting LDPC frames from the transition to PCS_Test.

In initial training, normal retraining, and fast retraining, with or without the EEE capability being supported, the master and slave signal when they transition to PCS_Test using the transition counter following the procedure described in 126.4.2.5.15.

A EEE-capable PHY in slave mode is responsible for synchronizing its PMA training frame to the master's PMA training frame during the transition to PMA_Training_Init_S. The slave shall ensure that its PMA training frames are synchronized to the master's PMA training frames within two LDPC frames, measured at the slave MDI on pair A. In addition, the slave shall initialize its transition counter so that it transitions to PCS_Test within two LDPC frames of the master PHY's transition to PCS_Test, measured at the slave PHY's MDI on pair A. This mechanism ensures that the refresh offset is bounded to a small value at both MDI interfaces, thus ensuring there is no overlap of master and slave signals when both transmit and receive are in the LPI mode.

Following the transition to PCS_Test, the PCS counts transmitted and received LDPC frames, and uses these counters to generate refresh and pair control signals for the transmit and receive functions. The transmitted LDPC frame count is named tx_ldpc_frame_cnt. The received LDPC frame count is named rx_ldpc_frame_cnt.

The master and slave shall derive the active pair and refresh_active signals from the LDPC frame counters as follows in Table 126–4 and Table 126–5.

Table 126–4—Synchronization logic derived from slave signal LDPC frame count

Slave-side variable	Master-side variable	for master u=rx_ldpc_frame_cnt for slave u=tx_ldpc_frame_cnt
tx_refresh_active=true	rx_refresh_active=true	lpi_offset – lpi_refresh_time ≤ mod(u,lpi_qr_time) < lpi_offset
tx_lpi_full_refresh=true	N/A	lpi_offset – lpi_refresh_time = mod(u,lpi_qr_time)
tx_active_pair=PAIR_A	rx_active_pair=PAIR_A	lpi_offset + lpi_qr_time ≤ u < lpi_offset + 2 × lpi_qr_time
tx_active_pair=PAIR_B	rx_active_pair=PAIR_B	lpi_offset + 2 × lpi_qr_time ≤ u < lpi_offset + 3 × lpi_qr_time
tx_active_pair=PAIR_C	rx_active_pair=PAIR_C	lpi_offset + 3 × lpi_qr_time ≤ u < 4 × lpi_qr_time OR 0 ≤ u < lpi_offset
tx_active_pair=PAIR_D	rx_active_pair=PAIR_D	lpi_offset ≤ u < lpi_offset + lpi_qr_time

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Table 126–5—Synchronization logic derived from master signal LDPC frame count

Slave-side variable	Master-side variable	for master v=tx_ldpc_frame_cnt for slave v=rx_ldpc_frame_cnt
rx_refresh_active=true	tx_refresh_active=true	lpi_quiet_time ≤ mod(v,lpi_qr_time)
N/A	tx_lpi_full_refresh=true	lpi_quiet_time = mod(v,lpi_qr_time)
rx_active_pair=PAIR_A	tx_active_pair=PAIR_A	0 ≤ v < lpi_qr_time
rx_active_pair=PAIR_B	tx_active_pair=PAIR_B	lpi_qr_time ≤ v < 2 × lpi_qr_time
rx_active_pair=PAIR_C	tx_active_pair=PAIR_C	2 × lpi_qr_time ≤ v < 3 × lpi_qr_time
rx_active_pair=PAIR_D	tx_active_pair=PAIR_D	3 × lpi_qr_time ≤ v < 4 × lpi_qr_time

126.3.5.2 Quiet period signaling

During the quiet period the transmitters on all four pairs should be turned off. Average launch power (as measured from 56 LDPC frames after a refresh period to 56 LDPC frames before the next refresh period on the same lane) for each Transmitter shall be less than –41 dBm. This requirement does not apply to the periods when the alert signal is transmitted as defined in 126.4.2.2.1.

126.3.5.3 Refresh period signaling

During the LPI mode 2.5GBASE-T and 5GBASE-T PHYs use staggered, out-of-phase refresh signaling to maximize power savings. Two-level PAM refresh symbols are generated using the PMA side-stream scrambler polynomials described in 126.3.4 and exactly as is shown in Figure 126–11 with the exception that the Infofield consists of a sequence of 128 zeros. The training sequence described in 126.3.4 shall be used during the LPI mode, with the scramblers free-running from PCS Reset.

Refresh signals shall be sent using the THP filter as described in 126.4.3.1. At the start of each refresh signal the THP feedback delay line shall be initialized with zeros.

While a transmit function is in the LPI transmit mode only one of the transmit pairs is active during a refresh period. tx_symb_vector for all transmit pairs that are not active shall be set to zero.

When tx_symb_vector has the value ALERT and the PHY is master, the transmitter on pair A shall be active and all other pairs shall be quiet. When tx_symb_vector has the value ALERT and the PHY is slave, the transmitter on pair C shall be active and all other pairs shall be quiet. If lpi_tx_mode=REFRESH_A on a MASTER PHY or lpi_tx_mode=REFRESH_C on a SLAVE PHY, and tx_symb_vector has the value ALERT, then the alert signaling shall be transmitted in place of the refresh signaling where the signals overlap.

126.3.6 Detailed functions and state diagrams

126.3.6.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

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The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

126.3.6.2 State diagram parameters

126.3.6.2.1 Constants

EBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in 46.3.4.

LBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing two Local Fault ordered sets.

LPBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII containing /LI/ in all the eight character locations.

LPBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing /LI/ in all the eight character locations.

IBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII containing /I/ in all the eight character locations.

IBLOCK_T<64:0>
: 65 bit vector to be sent to the LDPC encoder containing /I/ in all the eight character locations.

UBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII containing two Link Interruption ordered sets. The Link Interruption ordered set is defined in 46.3.4.

126.3.6.2.2 Variables

lfer_test_lf
: Boolean variable that is set true when a new LDPC frame is available for testing and false when LFER_TEST_LF state is entered. A new LDPC frame is available for testing when the Block Sync process has accumulated enough symbols from the PMA to evaluate the next LDPC frame.

block_lock
: Boolean variable that is set true when receiver acquires block delineation.

hi_lfer
: Boolean variable that is asserted true when the lfer_cnt reaches 16 errors in one lfer_timer interval.

pcs_reset
: Boolean variable that controls the resetting of the PCS. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rx_coded<64:0>
: Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 126–8. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_raw<71:0>
: Vector containing two successive XGMII output transfers. RXC<3:0> for the first transfer are taken from rx_raw<3:0>. RXC<3:0> for the second transfer are taken from rx_raw<7:4>. RXD<31:0> for the first transfer are taken from rx_raw<39:8>. RXD<31:0> for the second transfer are taken from rx_raw<71:40>.

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lf_valid
: Boolean indication that is set true if received LDPC frame is valid. LDPC frame is valid if and only if all parity checks of the LDPC code are satisfied.

tx_coded<64:0>
: Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 126–8. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_raw<71:0>
: Vector containing two successive XGMII transfers. TXC<3:0> for the first transfer are placed in tx_raw<3:0>. TXC<3:0> for the second transfer are placed in tx_raw<7:4>. TXD<31:0> for the first transfer are placed in tx_raw<39:8>. TXD<31:0> for the second transfer are placed in tx_raw<71:40>.

The following variables are required for PHYs that support the EEE capability:

tx_lpi_active
: A Boolean variable that is set true when the PHY transmit function is operating in the LPI transmit mode and during transitions to and from the LPI transmit mode (i.e., at any time when the PHY is transmitting sleep, alert, wake, or quiet-refresh signaling). It is set false otherwise.

tx_lpi_qr_active
: A Boolean variable that is set true during the LPI transmit mode, when the PHY is transmitting quiet-refresh signaling. Set false otherwise.

rx_lpi_active
: A Boolean variable that is set true when the PHY receive function is operating in the LPI receive mode and set false otherwise. The LPI receive mode begins when the sleep signal is detected and lasts until the alert signal is detected. When the EEE capability is not supported, rx_lpi_active is set false.

tx_lpi_req
: A Boolean variable that is set true when the LPI client indicates that it is requesting operation in the LPI transmit mode via the XGMII and set false otherwise.

alert_detect
: Indicates that an alert signal from the link partner has been received at the MDI as indicated by PMA_ALERTDETECT.indication(alert_detect).

tx_lpi_alert_active
: A Boolean variable that is set true when the PHY is transmitting ALERT signaling. Set false otherwise.

rx_lpi_wake
: A Boolean variable that is set true when the PHY receiver is in the WAKE state and sending IDLE to the XGMII. Set false otherwise. When the EEE capability is not supported, rx_lpi_wake is set false.

tx_active_pair
: A variable indicating the transmit active pair during the LPI transmit mode. The variable may take the values PAIR_A, PAIR_B, PAIR_C, PAIR_D. This variable is defined in 126.3.5.1.

lpi_tx_mode
: A variable indicating the signaling to be used from the PCS to the PMA across the PMA_UNITDATA.request (tx_symb_vector) interface.
lpi_tx_mode controls tx_symb_vector only when tx_mode is set to SEND_N.
The variable is set to NORMAL when (!tx_lpi_qr_active * !tx_lpi_alert_active), indicating that the PCS is in the normal mode of operation and encodes code-groups as described in Figure 126–14 and Figure 126–15.
The variable is set to REFRESH_A when (tx_lpi_qr_active * (tx_active_pair=PAIR_A) * tx_refresh active).
The variable is set to REFRESH_B when (tx_lpi_qr_active * (tx_active_pair=PAIR_B) * tx_refresh active).
The variable is set to REFRESH_C when (tx_lpi_qr_active * (tx_active_pair=PAIR_C) *

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tx_refresh active).
The variable is set to REFRESH_D when (tx_lpi_qr_active * (tx_active_pair=PAIR_D) * tx_refresh active).
The variable is set to QUIET when (tx_lpi_qr_active * (!tx_refresh_active + tx_lpi_initial_quiet)).
The variable is set to ALERT when (tx_lpi_alert_active).

tx_refresh_active
: A Boolean value. This variable is set true following the logic described in 126.3.5.1.

tx_lpi_full_refresh
: A Boolean value. This variable is set true following the logic described in 126.3.5.1.

tx_lpi_initial_quiet
: A Boolean value. This variable is set true when the transmit function enters the LPI transmit mode and a partial refresh is replaced by quiet signaling.

ldpc_two_frame_done
: A Boolean value. This variable is set true when the final symbol of each even LDPC frame aligned to the inversion on pair A during PMA training is transmitted and is set false otherwise.

The following variable is only required for PHYs that support the fast retrain capability:

fr_sigtype
: If fast retrain is supported, this variable controls the block type the PMA sends on the receive path during fast retrain. If MDIO is supported, this variable is set based on the value in 1.147.2:1 as follows:
  00 IBLOCK_R
  01 LBLOCK_R
  10 UBLOCK_R
  11 Reserved
  If MDIO is not supported, an equivalent method of controlling fast retrain functionality should be provided.

126.3.6.2.3 Timers

State diagram timers follow the conventions described in 14.2.3.2.

lfer_timer
: Timer that is triggered every 125/*S* μs +1%, –25%. When the timer reaches its terminal count it sets lfer_timer_done = TRUE.

The following timers are required for PHYs that support the EEE capability:

lpi_tx_sleep_timer
: This timer defines the time the local transmitter sends the sleep signal to the link partner.
  Values: The condition lpi_tx_sleep_timer_done becomes true upon timer expiration.
  Duration: This timer shall have a period equal to 18 LDPC frame periods.

lpi_tx_alert_timer
: This timer defines the time the local transmitter transmits the alert signal.
  Values: The condition lpi_tx_alert_timer_done becomes true upon timer expiration.
  Duration: This timer shall have a period equal to 8 LDPC frame periods.

lpi_tx_wake_timer
: This timer defines the time the local transmitter transmits the wake signal.
  Values: The condition lpi_tx_wake_timer_done becomes true upon timer expiration.
  Duration: This timer shall have a period equal to lpi_wake_time LDPC frame periods.

lpi_rx_wake_timer
: This timer defines the time the receiver sends IDLE blocks to the XGMII after the alert signal is detected.

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Values: The condition lpi_rx_wake_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time LDPC frame periods.

126.3.6.2.4 Functions

DECODE(rx_symb_vector<64:0>)

In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the LDPC decoder and decodes the 65B-LDPC bit vector returning a vector rx_raw<71:0>, which is sent to the XGMII. The DECODE function shall decode the block based on code specified in 126.3.2.2.2.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector received from the XGMII, returning 65-bit vector tx_coded. The ENCODE function shall encode the block as specified in 126.3.2.2.2.

R_BLOCK_TYPE = {C, S, T, D, E, I, LI, LII}

When the EEE capability is not supported, this function classifies each 65-bit rx_coded vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.

When the EEE capability is supported, this function classifies each 65-bit rx_coded vector as belonging to the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /I/, but in every other case the vector belongs to only one type.

Values: C; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x1E and eight valid control characters other than /E/ and /LI/;
b) A block type field of 0x2D or 0x4B, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.

S; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.

T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1, or 0xFF and all control characters are valid.

D; The vector contains a data/ctrl header of 0.

I; If the optional EEE capability is supported, then the I type is a special case of the C type where the vector contains a data/ctrl header of 1, a block type field of 0x1E, and eight control characters of /I/.

LI: If the optional EEE capability is supported, then the LI type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and eight control characters of /LI/.

LII: If the optional EEE capability is supported, then the LII type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and one of the following:

a) Four control characters of /LI/ followed by four control characters of /I/;
b) Four control characters of /I/ followed by four control characters of /LI/.

E; The vector does not meet the criteria for any other value.

A valid control character is one containing a 2.5G/5GBASE-T control code specified in Table 126–1. A valid O code is one containing an O code specified in Table 126–1.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

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T_BLOCK_TYPE = {C, S, T, D, E, I, LI, LII}

When the EEE capability is not supported, this function classifies each 72-bit tx_raw vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.

When the EEE capability is supported, this function classifies each 72-bit tx_raw vector as belonging to the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /I/, but in every other case the vector belongs to only one type.

Values: C; The vector contains one of the following:

a) Eight valid control characters other than /O/, /S/, /T/, /E/, and /LI/;
b) One valid ordered set and four valid control characters other than /O/, /S/, and /T/;
c) Two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character, any characters before the S character are valid control characters other than /O/, /S/, and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

I; If the optional EEE capability is supported, then the I type is a special case of the C type where the vector contains eight control characters of /I/.

LI: If the optional EEE capability is supported, then the LI type occurs when the vector contains eight control characters of /LI/.

LII: If the optional EEE capability is supported, then the LII type occurs when the vector contains one of the following:

a) Four control characters of /LI/ followed by four control characters of /I/;
b) Four control characters of /I/ followed by four control characters of /LI/.

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 126–1. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 126–1.

T_TYPE(tx_raw<71:0>)

Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

T_TYPE_NEXT

Prescient end of packet check function. It returns the FRAME_TYPE of the tx_raw vector immediately following the current tx_raw vector.

126.3.6.2.5 Counters

lfer_cnt

Count up to a maximum of 16 of the number of invalid LDPC frames within the current lfer_timer period.

The following counters are required for PHYs that support the EEE capability:

tx_ldpc_frame_cnt

An integer value that counts transmit LDPC frame periods. The counter is reset when the first symbol of the first LDPC frame crosses the MDI on pair A in the transmit direction after normal training or fast retraining. It is incremented after the last symbol of each transmitted LDPC frame. tx_ldpc_frame_cnt is reset to 0 when tx_ldpc_frame_cnt = lpi_qr_time × 4.

rx_ldpc_frame_cnt

An integer value that counts receive LDPC frame periods. The counter is reset when the first symbol of the first LDPC frame crosses the MDI on pair A in the receive direction after normal

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training or fast retraining. It is incremented after the last symbol of each received LDPC frame. rx_ldpc_frame_cnt is reset to 0 when rx_ldpc_frame_cnt = lpi_qr_time × 4.

lpi_rxw_err_cnt

An integer value that counts the number of receive wake on error conditions. lpi_rxw_err_cnt is reset to zero during PCS_Test. The counter is reflected in register 3.22 (see 45.2.3.12).

126.3.6.3 State diagrams

The LFER Monitor state diagram shown in Figure 126–13 monitors the received signal for high LDPC frame error ratio.

The 64B/65B Transmit state diagram shown in Figure 126–14 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the Transmit state diagram sends Local Fault ordered sets when reset is asserted, the scrambler and 65B-LDPC may not be operational during reset. Thus, the Local Fault ordered sets may not appear on the PMA service interface.

The 64B/65B Receive state diagram shown in Figure 126–16 controls the decoding of 65B received blocks. It makes exactly one transition for each receive block processed except for the transition from RX_WE to RX_E, which occurs immediately after the RX_WE processes are complete.

The PCS shall perform the functions of LFER Monitor, Transmit, and Receive as specified in these state diagrams. The PCS shall not perform the LFER Monitor function during LPI receive operation from the time that the PCS 64B/65B Receiver enters the state RX_L, until the state RX_W is exited.

Transitions surrounded by dashed rectangles indicate requirements for 2.5GBASE-T and 5GBASE-T EEE-capable implementations.

126.3.7 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

126.3.7.1 Status

pcs_status

Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_lfer is false. This status is reflected in MDIO register 3.32.12. A latch low view of this status is reflected in MDIO register 3.1.2 and a latch high of the inverse of this status, Receive fault, is reflected in MDIO register 3.8.10.

block_lock

Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.32.0. A latch low view of this status is reflected in MDIO register 3.33.15.

hi_lfer

Indicates the state of the hi_lfer variable. This status is reflected in MDIO register 3.32.1. A latch high view of this status is reflected in MDIO register 3.33.14.

Rx LPI indication

For EEE capability, this variable indicates the current state of the receive LPI function. This flag is set to TRUE (register bit set to one) when the PCS 64B/65B Receive state diagram (Figure 126–17) is in the RX_L or RX_W states. This status is reflected in MDIO register 3.1.8. A latch high view of this status is reflected in MDIO register 3.1.10 (Rx LPI received).

Tx LPI indication

For EEE capability, this variable indicates the current state of the transmit LPI function. This flag is set to TRUE (register bit set to one) when the PCS 64B/65B Transmit state diagram

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(Figure 126–15) is in the TX_L or TX_W states. This status is reflected in MDIO register 3.1.9. A latch high view of this status is reflected in MDIO register 3.1.11 (Tx LPI received).

126.3.7.2 Counters

The following counters are reset to zero upon read and upon reset of the PCS. When they reach all ones, they stop counting. Their purpose is to help monitor the quality of the link.

lfer_count
: 6-bit counter that counts each time LFER_BAD_LF state is entered. This counter is reflected in MDIO register bits 3.33.13:8. The counter is reset when register 3.33 is read by management. Note that this counter counts a maximum of 16 counts per lfer_timer period since the LFER_BAD_LF can be entered a maximum of 16 times per lfer_timer window.

errored_block_count
: 8-bit counter. When the receiver is in normal mode, errored_block_count counts once for each time RX_E state is entered. This counter is reflected in MDIO register bits 3.33.7:0.

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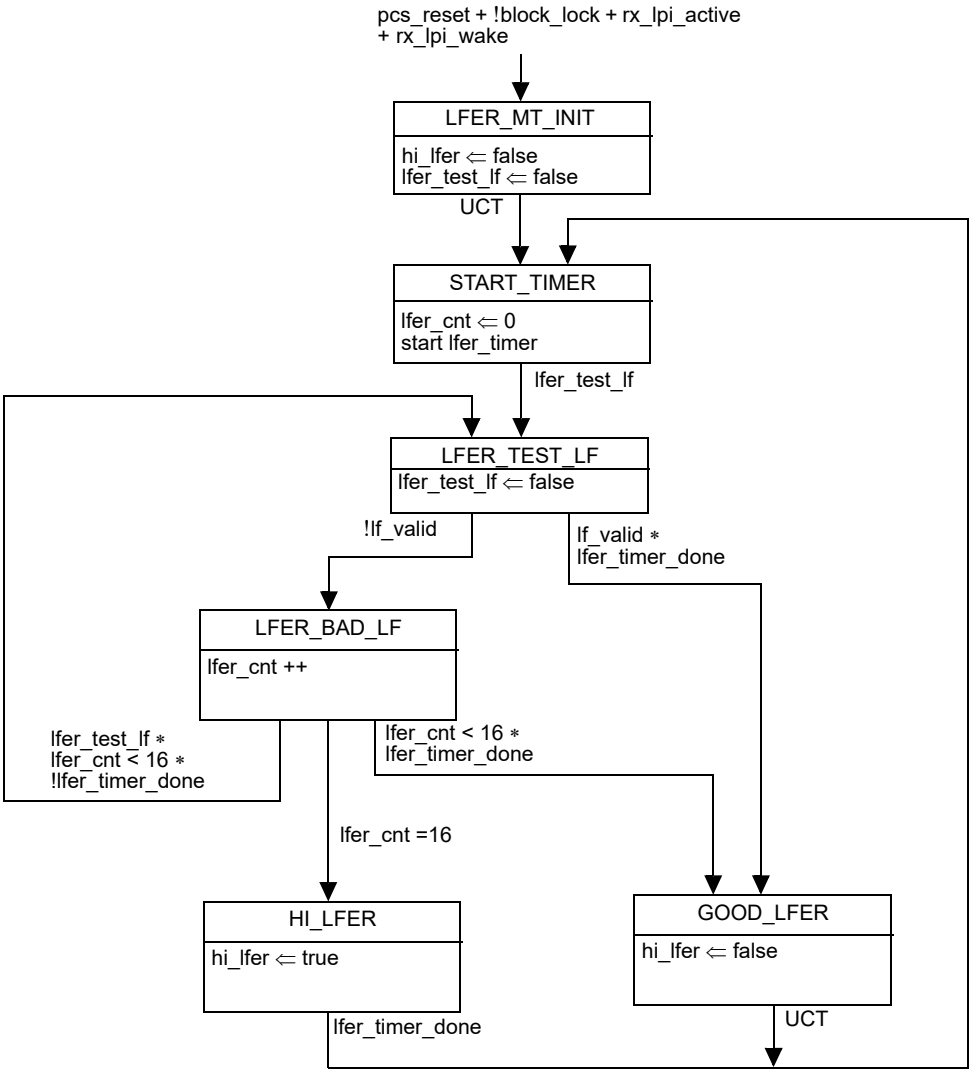

Figure 126–13—LFER monitor state diagram

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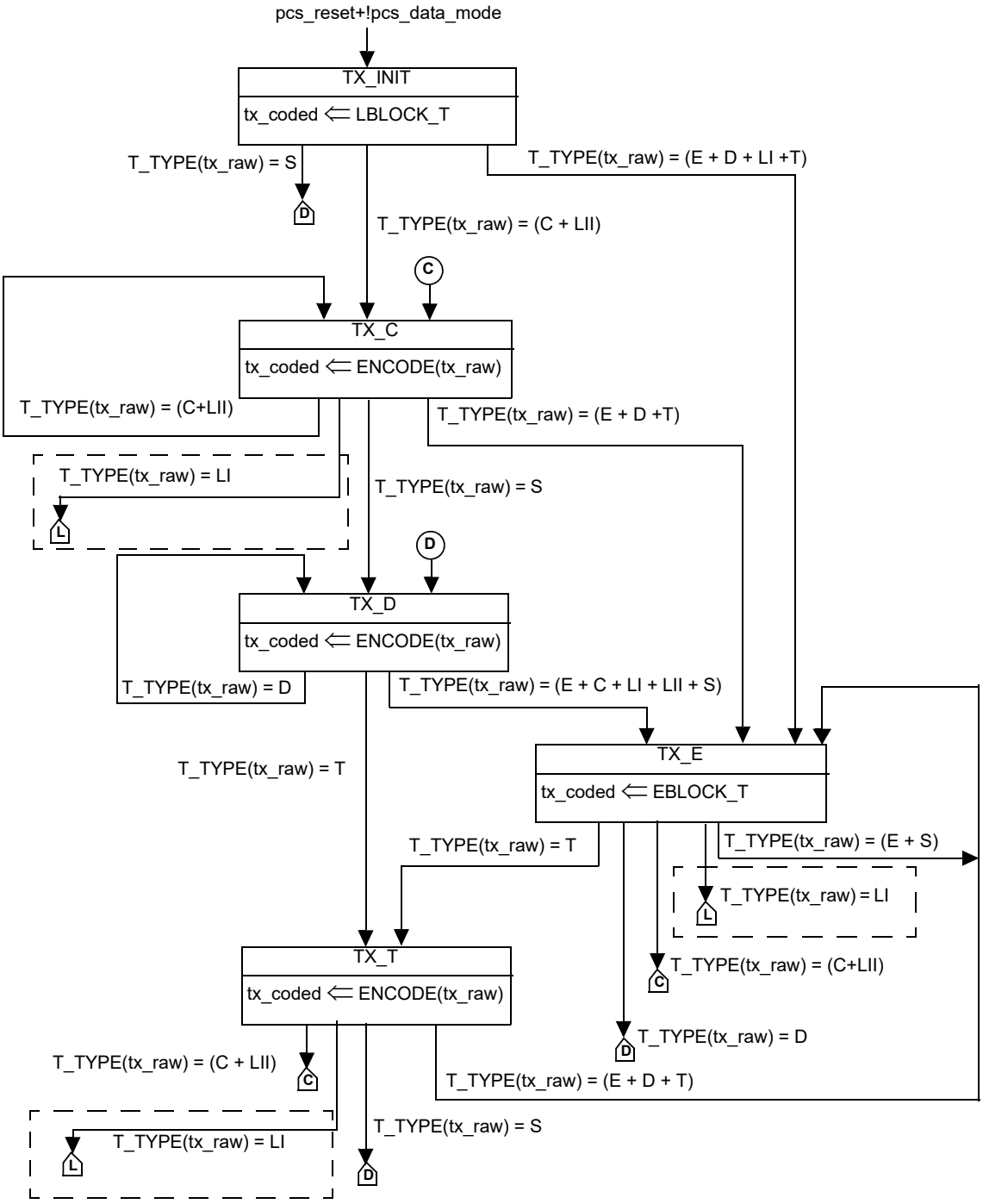

NOTE—Transitions inside dashed boxes are only required for the EEE capability.

Figure 126–14—PCS 64B/65B Transmit state diagram, part a

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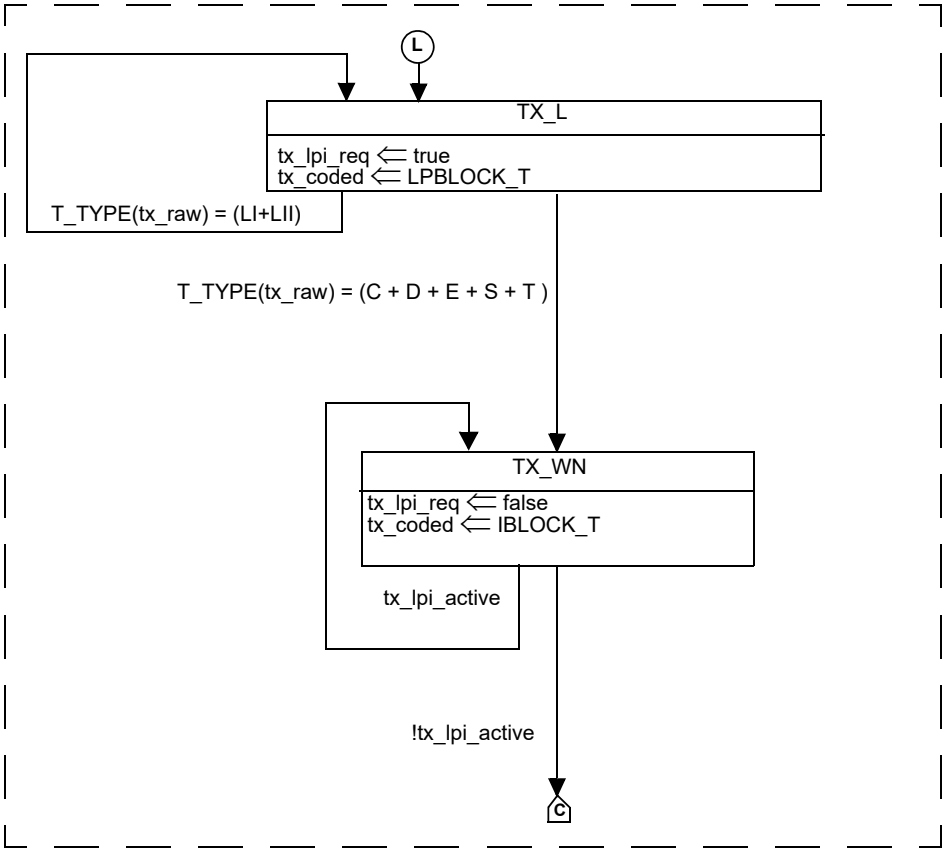

NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 126–15—PCS 64B/65B Transmit state diagram, part b

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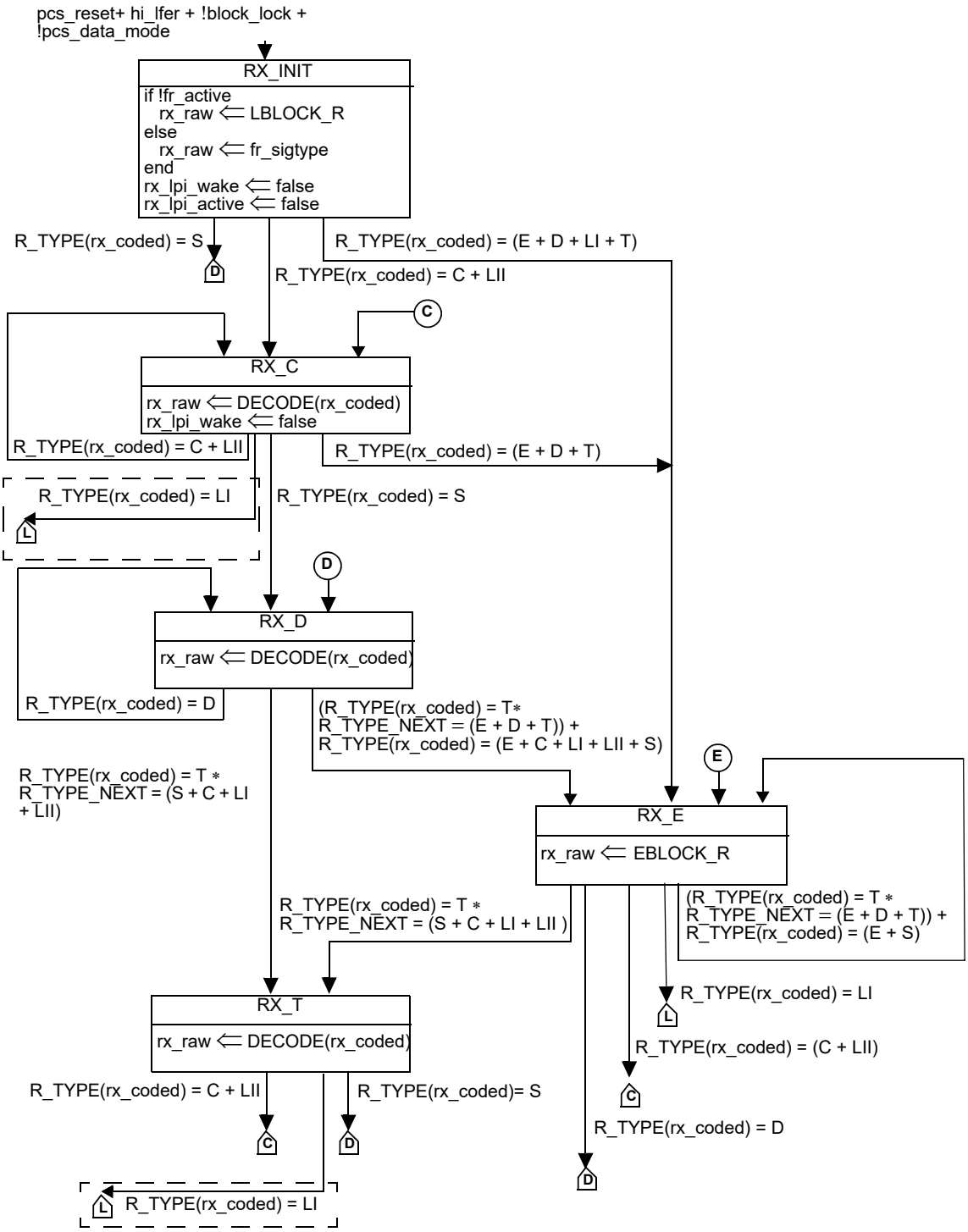

NOTE—Signals and functions shown with dashed lines are only required for the EEE capability.

Figure 126–16—PCS 64B/65B Receive state diagram, part a

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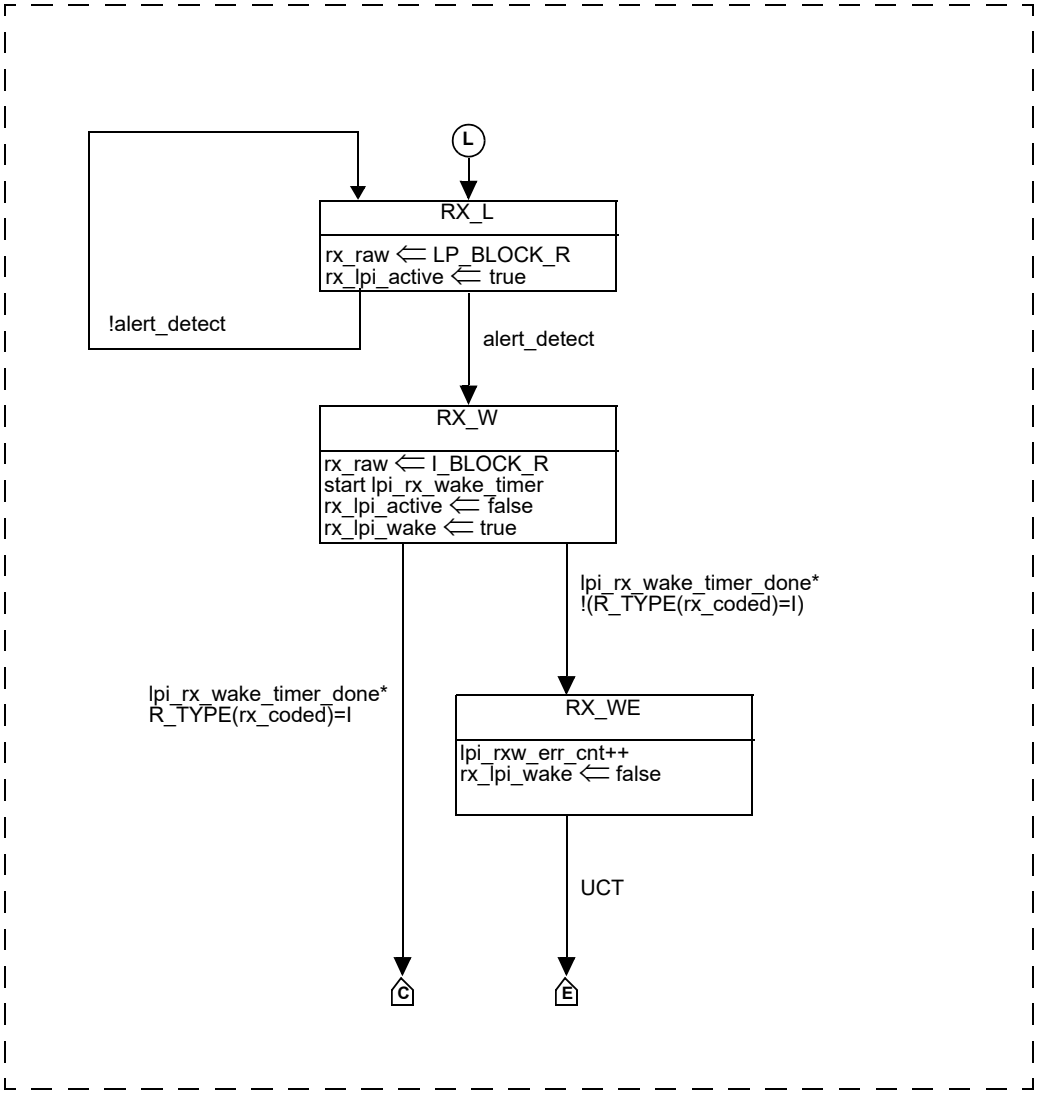

NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 126–17—PCS 64B/65B Receive state diagram, part b

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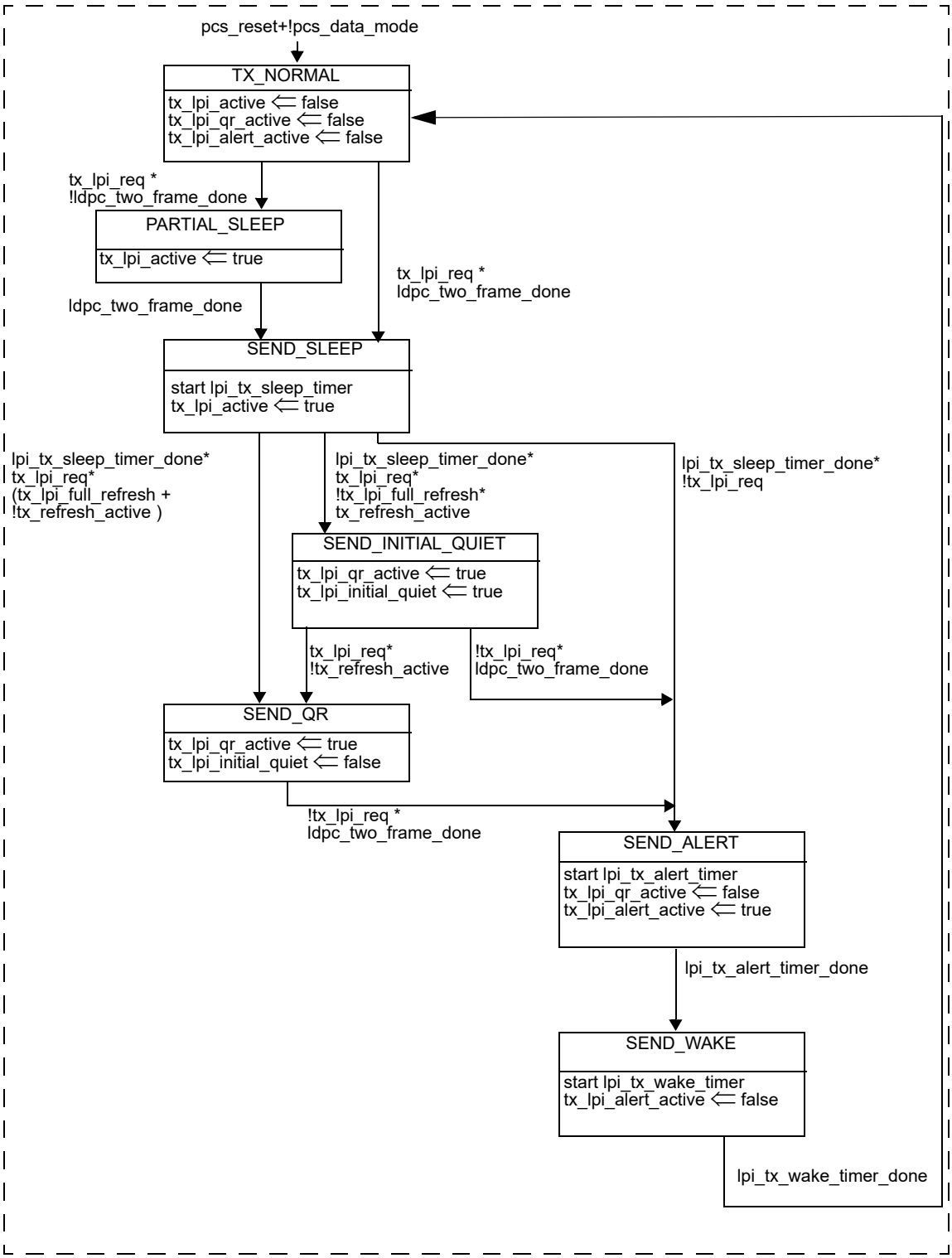

NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 126–18—EEE transmit state diagram

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126.3.7.3 Loopback

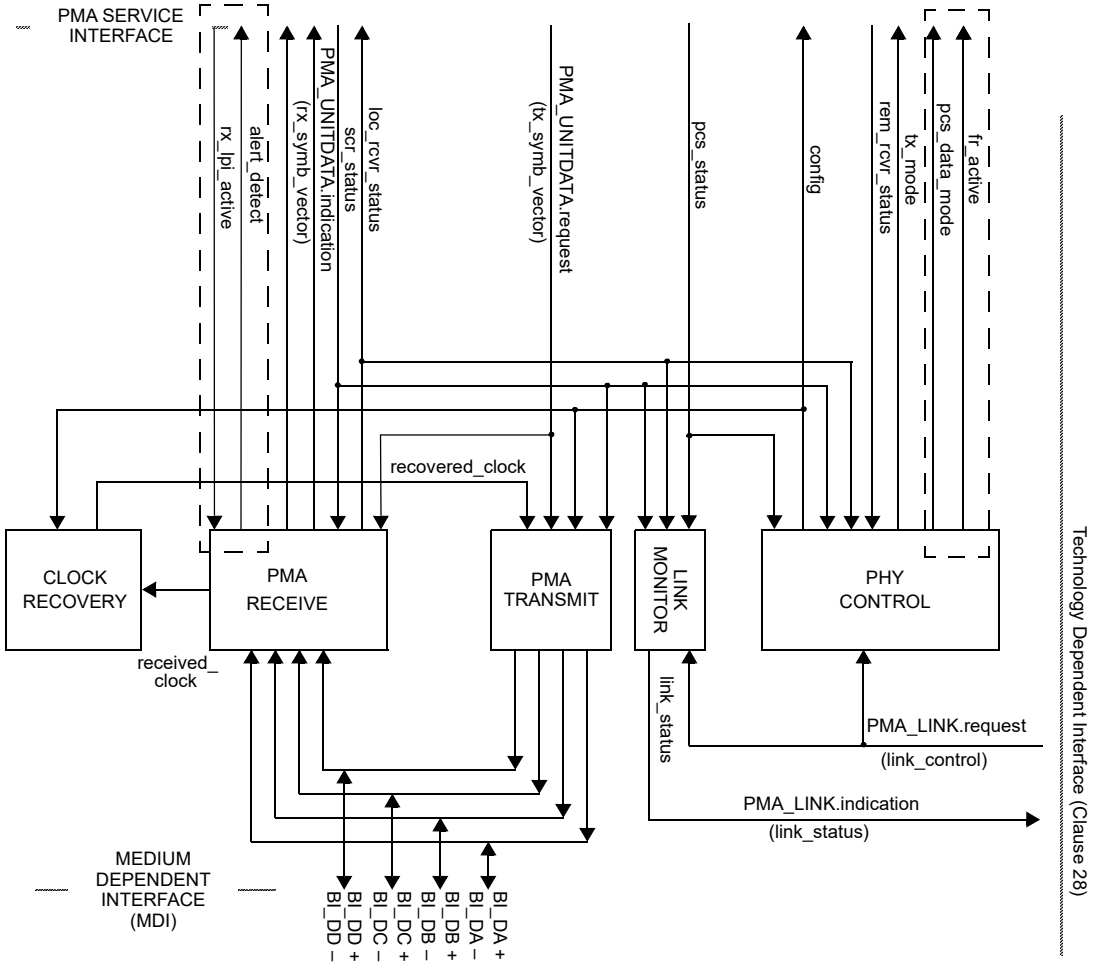
The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14 is set to a one. In this mode, the PCS shall accept data on the transmit path from the XGMII and return it on the receive path to the XGMII. In addition, the PCS shall transmit a continuous stream of 65B-LDPC encoded 4D-PAM16 symbols to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer.

126.4 Physical Medium Attachment (PMA) sublayer

126.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 126.2.2 to the 2.5GBASE-T and 5GBASE-T baseband media, specified in 126.7.

The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 126.8.



NOTE 1—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

NOTE 2—pcs_data_mode is required only for the EEE or fast retrain capabilities alert_detect and rx_lpi_active are only required for the EEE capability fr_active is only required for the fast retrain capability.

Figure 126–19— PMA reference diagram

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126.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 126–19, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 126–19.

126.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power on (see 126.3.6.2.2)
b) The receipt of a request for reset from the management entity

All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

126.4.2.2 PMA Transmit function

The PMA Transmit function comprises four synchronous transmitters to generate four pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. While send_fail is FALSE and ALERT is not indicated by tx_symb_vector, PMA Transmit shall continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively after processing with the THP, optional transmit filtering, digital to analog conversion (DAC) and subsequent analog filtering. When ALERT is indicated by tx_symb_vector, the alert signal is transmitted as specified in 126.4.2.2.1. When send_fail is TRUE, the link failure signal is transmitted as specified in 126.4.2.2.2. The four transmitters shall be driven by the same transmit clock, TX_TCLK. The signals generated by PMA Transmit shall follow the mathematical description given in 126.4.3.1, and shall comply with the electrical specifications given in 126.5.

When the PMA_CONFIG.indication parameter config is MASTER, for both normal and LPI operation, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 126.5.3.3. The MASTER/SLAVE relationship includes loop timing. If the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 126.4.2.8 while meeting the jitter requirements of 126.5.3.3.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

EEE-capable PHYs shall generate the alert signal as defined in 126.4.2.2.1. PHYs that support the fast retrain capability shall generate the link failure signal as defined in 126.4.2.2.2. If ALERT is indicated by tx_symb_vector at the same time as send_fail is TRUE, then link failure signaling is transmitted.

126.4.2.2.1 Alert signal

PHYs that support the optional EEE capability transmit the following PAM2 sequence when the PMA_UNITDATA.request parameter is set to ALERT. The alert signal is sent for a total of 8 LDPC frame periods and begins on a LDPC 2-frame 256 4D-symbol boundary aligned to the inversion on pair A during

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PMA training. The alert signal is transmitted without THP filtering. The alert signal is transmitted on pair A when the PHY operates as a MASTER. The alert signal is transmitted on pair C when the PHY operates as a SLAVE. All other pairs transmit quiet as described in 126.3.5.

When the PMA_CONFIG.indication(config) is MASTER the alert signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xpr_master =

9 9 –9 –9 –9 –9 –9 –9 9 9 –9 –9 9 9 9 9

9 9 9 9 –9 –9 9 9 9 9 –9 –9 9 9 –9 –9

–9 –9 –9 –9 –9 –9 9 9 –9 –9 –9 –9 –9 –9 9 9

–9 –9 –9 –9 –9 –9 –9 –9 9 9 –9 –9 9 9 –9 –9

–9 –9 9 9 9 9 9 9 9 9 9 9 –9 –9 –9 –9

9 9 –9 –9 –9 –9 9 9 9 9 –9 –9 9 9 –9 –9

–9 –9 –9 –9 –9 –9 –9 –9 9 9 9 9 –9 –9 9 9

9 9 –9 –9 9 9 –9 –9 9 9 9 9 –9 –9 –9 –9

When the PMA_CONFIG.indication(config) is SLAVE the alert signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xpr_slave =

–9 –9 –9 –9 9 9 9 9 –9 –9 9 9 –9 –9 9 9

9 9 –9 –9 9 9 9 9 –9 –9 –9 –9 –9 –9 –9 –9

–9 –9 9 9 –9 –9 9 9 9 9 –9 –9 –9 –9 9 9

–9 –9 –9 –9 9 9 9 9 9 9 9 9 9 9 –9 –9

–9 –9 9 9 –9 –9 9 9 –9 –9 –9 –9 –9 –9 –9 –9

9 9 –9 –9 –9 –9 –9 –9 9 9 –9 –9 –9 –9 –9 –9

–9 –9 9 9 –9 –9 9 9 9 9 –9 –9 9 9 9 9

9 9 9 9 –9 –9 9 9 –9 –9 –9 –9 –9 –9 9 9

The alert signal is followed by a wake signal composed of repeated IDLE characters encoded using the 64B/65B encoding technique. At the start of the wake signal all THP feedback delay lines are initialized with zeros.

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126.4.2.2.2 Link failure signal

PHYs that support the fast retrain capability transmit the link failure signal under the control of the Fast Retrain state diagram. The link failure signal indicates to the link partner that a link failure has been detected and that the link partners should begin the fast retrain procedure.

The link failure signal is sent for 8 LDPC frames and begins on an even LDPC frame boundary aligned to the inversion on pair A during PMA training. The link failure signal is transmitted without THP filtering. The link failure signal is transmitted on pair A when the PHY operates as a MASTER. The link failure signal is transmitted on pair C when the PHY operates as a SLAVE. All other pairs transmit quiet as described in 126.3.5.

When the PMA_CONFIG.indication(config) is MASTER, the link failure signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xfr_master = xpr_master × (−1)

When the PMA_CONFIG.indication(config) is SLAVE the link failure signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xfr_slave = xpr_slave × (−1)

126.4.2.3 PMA transmit disable function

126.4.2.3.1 Global PMA transmit disable function

The Global_PMA_transmit_disable function allows all of the transmitters to be disabled. It is used in either of the following cases:

a) When a Global_PMA_transmit_disable variable is set to TRUE, this function shall turn off all of the transmitters so that the each transmitter Average Launch Power of the OFF Transmitter is less than –53 dBm.
b) If a PMA_transmit_fault is detected, then the PMA may set the Global_PMA_transmit_disable to TRUE, turning off the transmitter on each pair.

126.4.2.3.2 PMA pair by pair transmit disable function

The PMA_transmit_disable function allows the transmitters on each pair to be selectively disabled.

When a PMA_transmit_disable_N variable is set to TRUE, this function shall turn off the transmitter associated with that variable so that the transmitter Average Launch Power of the OFF Transmitter is less than –53 dBm.

126.4.2.3.3 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 126–6. Mapping of MDIO status variables to PMA status variables is shown in Table 126–7.

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Table 126–6—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	Control register 1	1.0.15	PMA_reset
Global PMD transmit disable	Transmit disable register	1.9.0	Global_PMA_transmit_disable
Transmit disable pair D	Transmit disable register	1.9.4	PMA_transmit_disable_D
Transmit disable pair C	Transmit disable register	1.9.3	PMA_transmit_disable_C
Transmit disable pair B	Transmit disable register	1.9.2	PMA_transmit_disable_B
Transmit disable pair A	Transmit disable register	1.9.1	PMA_transmit_disable_A

Table 126–7—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Fault	Status register 1	1.1.7	PMA_fault
Transmit fault	Status register 2	1.8.11	PMA_transmit_fault
Receive fault	Status register 2	1.8.10	PMA_receive_fault

126.4.2.4 PMA Receive function

The PMA Receive function comprises four independent receivers for pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. The PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over receive pairs BI_DA, BI_DB, BI_DC, and BI_DD and to present these sequences to the PCS Receive function. The signals received at the MDI are described mathematically in 126.4.3.2. The PMA translates the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD into the PMA_UNITDATA.indication parameter rx_symb_vector. The quality of these symbols shall allow an LFER of less than 3.2×10^{-9} after LDPC decoding, over a channel meeting the requirements of 126.7. The receiver shall correct for differential delay variations of up to 50 ns across the wire-pairs. The delay skew is removed by computing the relative received delay of the four known transmit patterns described in 126.3.4.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization, echo and crosstalk cancellation. The sequence of code-groups assigned to tx_symb_vector is needed to perform echo and self near-end crosstalk cancellation.

The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, estimation, and LPI functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

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The receiver uses the sequence of symbols during the training sequence to detect and correct for pair swaps and crossovers. The receiver pairs BI_DA, BI_DB, BI_DC, and BI_DD may be connected in any manner described in 126.4.4 to the corresponding transmit pairs. The receiver also detects and corrects for polarity mismatches on any pairs and corrects for differential delay variations across the wire-pairs.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5.

PMA receive functions that support the optional EEE capability shall generate alert_detect when the alert signal is detected at the receiver. The PMA receive function asserts alert_detect after the entire alert signal (7 LDPC frame periods of the xpr_master or xpr_slave sequence and 1 frame of silence) has been detected. The alert signal is specified in 126.4.2.2.1. The criterion used to generate alert_detect is left to the implementer.

PHYs that support the fast retrain capability shall set link_fail_detect to TRUE when the link failure signal is reliably detected at the receiver. The PMA receive function asserts link_fail_detect after the entire link failure signal (7 LDPC frame periods of the xfr_master or xfr_slave sequence and 1 frame of silence) has been detected. The link failure signal is specified in 126.4.2.2.2. The criterion used to generate link_fail_detect is left to the implementer. It is highly recommended that the generation of link_fail_detect is qualified with repeated errored frames at the LDPC decoder output.

126.4.2.5 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 126–26.

During PMA training (includes PMA_Training_Init_M, PMA_Training_Init_S, PMA_PBO_Exch, PMA_Coeff_Exch, and PMA_Fine_Adjust states in Figure 126–26), PHY Control information is exchanged between link partners with a 16 octet Infofield, which is XOR'ed with the last 128 bits of the PMA 16384 PAM2 frame on pair A (see Figure 126–11). The link partner is not required to decode every Infofield transmitted but is required to decode Infofields at a rate that enables the correct actions to timer expiration times, transition counter values, etc. described in Figure 126–26, Figure 126–27, and Figure 126–28.

The 16 octet Infofield shall include the fields in 126.4.2.5.2 through 126.4.2.5.14, also shown in the overview Figure 126–20, and the more detailed Figure 126–21, Figure 126–22, and Figure 126–23.

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Message Field Dependent	Message Field Dependent	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	4 octets	2 octets

Figure 126–20—Infofield format

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Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Reser-ved	Transition Counter	Reser-ved/ Ability	Vendor Specific	CRC16
4 octets	3 octets	1 octet	4 bits	2 bits	10 bits	2 octets	2 octets	2 octets

Figure 126–21—Infofield transition counter format

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Coefficient Exchange	Coefficient Field	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	4 octets	2 octets

Figure 126–22—Infofield coefficient exchange format

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Reserved	Reserved /Ability	Vendor Specific	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	2 octets	2 octets	2 octets

Figure 126–23—Infofield not transition counter and not coefficient exchange format

126.4.2.5.1 Infofield notation

For all the Infofield notation below, Reserved<bit location> represents any unused values and shall be set to zero and ignored by the link partner. For all PBO Infofield values below, the PBO<6:4> are unsigned 3-bit values 000, 001, 010, 011, 100, 101, 110, and 111 shall indicate power backoffs of 0 dB, 2 dB, 4 dB, 6 dB, 8 dB, 10 dB, 12 dB, and 14 dB respectively. The Infofield is transmitted following the notation described in 126.3.2.2.3 where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Octet 1 is sent first).

126.4.2.5.2 Start of Frame Delimiter

The start of Frame Delimiter consist of 4 octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<7:0>, Octet 4<7:0>] and shall use the hexadecimal value 0xBBA70000. 0xBB corresponds to Octet 1<7:0> and so forth.

126.4.2.5.3 Current transmitter settings

Current transmitter setting (1 octet). Represented by Octet 5{Valid<7>, PBO<6:4>, Reserved<3:0>} and shown in Figure 126–24. Used to announce the current fixed PBO setting during PMA_Training_Init_M, PMA_Training_Init_S and PMA_PBO_Exch, and the current programmable PBO setting during PMA_Coeff_Exch. For every other state this octet is set to zero and ignored by the link partner. The bit Valid shall be set to one if the corresponding octet information is valid and shall be set to zero if it the octet information is not valid. If Valid is set to zero, the octet is ignored by the link partner.

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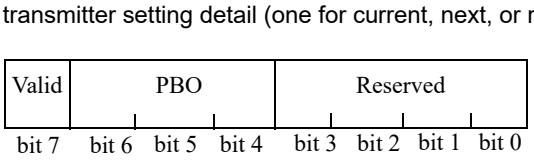

Figure 126–24—Infofield transmitter setting format

126.4.2.5.4 Next transmitter settings

Next transmitter setting (1 octet). Represented by Octet 6{Valid<7>, PBO<6:4>, Reserved<3:0>} and shown in Figure 126–24. Used to announce the next programmable PBO setting during PMA_PBO_Exch that takes effect upon entering PMA_Coeff_Exch state. For every other state, this octet is set to zero and ignored by the link partner. The bit Valid shall be set to one if the corresponding octet information is valid and shall be set to zero if it the octet information is not valid. If Valid is set to zero, the octet is ignored by the link partner.

126.4.2.5.5 Requested transmitter settings

Requested remote transmitter setting (1 octet). Represented by Octet 7{Valid<7>, PBO<6:4>, Reserved<3:0>} and shown in Figure 126–24. Used to request the remote transmitter programmable PBO setting during PMA_PBO_Exch that takes effect upon entering PMA_Coeff_Exch state. For every other state, this octet is set to zero and ignored by the link partner. The bit Valid shall be set to one if the corresponding octet information is valid and shall be set to zero if it the octet information is not valid. If Valid is set to zero, the octet is ignored by the link partner.

126.4.2.5.6 Message field

Message field (1 octet). For the MASTER, this field is represented by Octet 8{PMA_state<7:6>, loc_rcvr_status<5>, en_slave_tx<4>, trans_to_Coeff_Exch<3>, Coeff_exchange<2>, trans_to_Fine_Adjust<1>, trans_to_PCS_Test<0>}. For the SLAVE, this field is represented by Octet 8{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, trans_to_Coeff_Exch<3>, Coeff_exchange<2>, trans_to_Fine_Adjust <1>, trans_to_PCS_Test<0>}.

The two state-indicator bits PMA_state<7:6> shall indicate the state of the transmitting transceiver to the link partner as follows: PMA_state<7:6>=00 indicates PMA_Training_Init_M or PMA_Training_Init_S, PMA_state<7:6>=01 indicates PMA_PBO_Exch, PMA_state<7:6>=10 indicates PMA_Coeff_Exch, and PMA_state<7:6>=11 indicates PMA_Fine_Adjust.

All possible Message field settings are listed in Table 126–8 for the MASTER and Table 126–9 for the SLAVE. No other value shall be transmitted, and all other values shall be ignored at the receiver. The Message field setting for the first transmitted PMA frame shall be the first row of Table 126–8 for the MASTER and the first row of Table 126–9 for the SLAVE. Moreover, for a given Message field setting, the following Message field setting shall be the same Message field setting or the Message field setting corresponding to a row below the current setting. When loc_rcvr_status=OK the Infofield variable is set to loc_rcvr_status<5>=1 and set to 0 otherwise.

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Table 126–8—Infofield message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_ status	en_slave_tx	trans_to_ Coeff_Exch	Coeff_ exchange	trans_to_ Fine_Adjust	trans_to_ PCS_Test
00	0	0	0	0	0	0
00	0	1	0	0	0	0
01	0	1	0	0	0	0
01	0	1	1	0	0	0
10	0	1	0	0	0	0
10	0	1	0	1	0	0
10	0	1	0	0	0	0
10	0	1	0	0	1	0
11	0/1	1	0	0	0	0
11	1	1	0	0	0	1

Table 126–9—Infofield message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_ status	timing_lock _OK	trans_to_ Coeff_Exch	Coeff_ exchange	trans_to_ Fine_Adjust	trans_to_ PCS_Test
00	0	0	0	0	0	0
00	0	0/1	0	0	0	0
01	0	1	0	0	0	0
01	0	1	1	0	0	0
10	0	0/1	0	0	0	0
10	0	1	0	1	0	0
10	0	1	0	0	0	0
10	0	1	0	0	1	0
11	0	0/1	0	0	0	0
11	0/1	1	0	0	0	0
11	1	1	0	0	0	1

126.4.2.5.7 SNR_margin

SNR_margin (4 bits). Represented by Octet 9<7:4>, which reports received decision point SNR margin in 1/2 dB steps. SNR_margin is relative to the SNR required for reception of LDPC-coded PAM16 at an LDPC frame error ratio of less than 3.2×10^{-9}. The SNR_margin<7:4> 4-bit values, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110 shall indicate the decision point SNR margin values of –1.5,

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–1, –0.5, 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5 dB respectively. The value 0001 shall indicate a margin of –2 dB or less, and the value 1111 shall indicate 5 dB or more. Finally, the value 0000 shall indicate that the SNR margin value is unknown.

126.4.2.5.8 Transition counter

Transition counter (10 bits). Represented by the 1.25 octets [Octet 9<1:0>, Octet 10<7:0>]. When configured as Transition counter (Coeff_exchange<2>=0 and a transition is announced to PMA_Coeff_Exch, PMA_Fine_Adjust or PCS_Test) this field is used as a 10-bit counter that counts the number of remaining frames until the next transition (PMA_Coeff_Exch, PMA_Fine_Adjust, PCS_Test).

126.4.2.5.9 Coefficient exchange handshake

Coefficient exchange handshake (12 bits). Represented by the 1.5 octets [Octet 9<3:0>, Octet 10<7:0>]. If Coeff_exchange<2>=1, this field is configured as a Coefficient exchange handshake and is used as a handshake control channel during programmable THP coefficient exchange. The details of the coefficient exchange are described in 126.4.2.5.15.

126.4.2.5.10 Ability fields

Ability field (1 octet). Represented by Octet 12{EEE Ability<7>, THP Bypass Request<6>,Fast Retrain<5>, Reserved<4:0>}. Used to advertise the abilities of the PHY during the PMA_PBO_Exch state when Message<7:6> = 01.

For every other state, this octet is set to zero and ignored by the link partner. The Ability bits are defined as follows:

Octet 12<4:0> = Reserved

Octet 12<5> = Fast Retrain

0 = Fast Retrain not supported

1 = Fast Retrain supported

Octet 12<6> = THP Bypass Request in PMA_Coeff_Exch state

0 = Local device requests link partner not to bypass THP during fast retrain

1 = Local device requests link partner to bypass THP during fast retrain

Octet 12<7> = EEE Ability

0 = EEE not supported

1 = EEE supported.

126.4.2.5.11 Reserved fields

All Infofield fields denoted Reserved in Figure 126–21, Figure 126–22, and Figure 126–23 are reserved for future use. This includes Octet 11 and Octet 12 when Coeff_exchange<2>=0 and Message<7:6> is not equal to 01; Octet 9<3:2> when transition counter is announced; and [Octet 9<3:0>, Octet 10<7:0>] when no transition is announced and no coefficients are exchanged.

126.4.2.5.12 Vendor-specific field

If Coeff_exchange<2>=0, Octet 13 and Octet 14 are vendor-specific fields. If during Auto-Negotiation both transceivers agree on the use of the two vendor-specific octets, they may be used as a PHY communication

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channel; otherwise they are set to zero and ignored by the link partner. They are represented by Octet 13<7:0> and Octet 14<7:0>.

126.4.2.5.13 Coefficient field

The Coefficient field (4 octets) is represented by Octet 11<7:0>, Octet 12<7:0>, Octet 13<7:0>, and Octet 14<7:0>. When Coeff_exchange<2>=1, this field is used to exchange programmable THP coefficients. It transmits four 8-bit THP coefficients out of the total of 64 (16 coefficients over each of the 4 pairs). The order is pair A, coefficients 0:3, followed by coefficients 4:7, followed by 8:11 and 12:15. For all cases the first coefficient (indices 0, 4, 8, and 12) is mapped to Octet 11, the second coefficient (indices 1, 5, 9, 13) is mapped to Octet 12 and so on. The same coefficient order is followed to transmit the coefficients for pair B, followed by pair C, and finally pair D. The details of the coefficient exchange are described in 126.4.2.5.15.

126.4.2.5.14 CRC16

CRC16 (2 octets). This field shall contain the CRC16 value calculated using the polynomial $(x+1)(x^{15}+x+1)$ of the previous 10 octets, Octet 5<7:0>, Octet 6<7:0>, Octet 7<7:0>, Octet 8<7:0>, Octet 9<7:0>, Octet 10<7:0>, Octet 11<7:0>, Octet 12<7:0>, Octet 13<7:0>, and Octet 14<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 126–25. In Figure 126–25 the 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards Octet 5 through Octet 14 are used to compute the CRC16 with the switch set to CRCgen in Figure 126–25. After all the 10 octets have been processed, the switch is set to CRCout and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

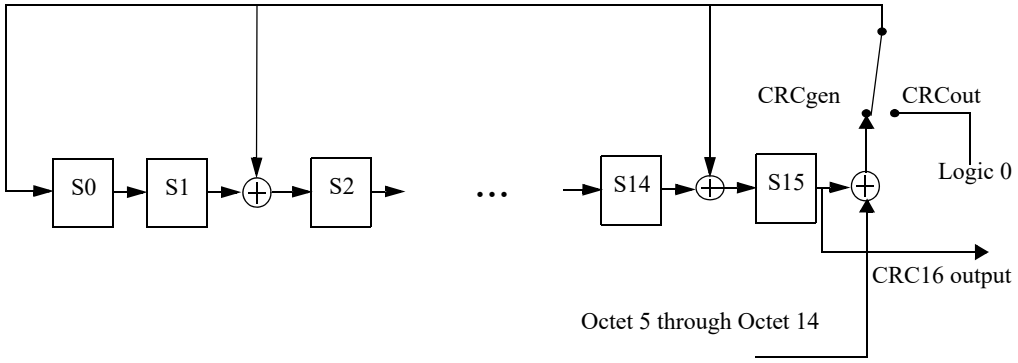

Figure 126–25—CRC16

126.4.2.5.15 Startup sequence

The startup sequence shall comply with the state diagram description given in Figure 126–26 and the transition counter state diagrams Figure 126–27 and Figure 126–28.

During Auto-Negotiation, PHY Control is in the DISABLE_2.5G/5GBASE-T_TRANSMITTER state and the transmitters are disabled. During normal training, prior to enabling the transmitter, the THP coefficients are set to zero.

When the Auto-Negotiation process asserts link_control=ENABLE, PHY Control enters the INIT_MAXWAIT_TIMER state. Upon entering this state, the maxwait_timer is started and PHY Control enters the SILENT state, which starts the minwait_timer and forces transmission of zeros by setting tx_mode=SEND_Z.

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In MASTER mode, after expiration of the minwait_timer, PHY Control transitions to the PMA_Training_Init_M state.

Upon entering the PMA_Training_Init_M and PMA_Training_Init_S states, the PHY Control forces transmission into the training mode by asserting tx_mode=SEND_T, which includes the transmission of Infofields.

Upon entering state PMA_Training_Init_M, the MASTER starts transmission with a fixed transmit power level, PBO=4 (corresponding to a power backoff of 8 dB). The PBO variable is communicated to the link partner via the current transmitter octet of the Infofield.

Initially the MASTER is not ready for the SLAVE to respond and sets en_slave_tx=0, which is communicated to the link partner via the Infofield. After the MASTER has sufficiently converged the necessary circuitry, the MASTER sets en_slave_tx=1 to allow the SLAVE to transition to PMA_Training_Init_S.

In SLAVE mode, PHY Control transitions to the PMA_Training_Init_S state only after the SLAVE PHY acquires timing, converges its equalizers, acquires its descrambler state and sets loc_SNR_margin=OK. The SLAVE shall respond using the fixed PBO transmit power level, PBO=4 (corresponding to a power backoff of 8 dB). For PHYs with the EEE capability, further requirements for this transition are described in 126.3.5.1.

While in states PMA_Training_Init_S, PMA_PBO_Exch, or PMA_Coeff_Exch, whenever a SLAVE operating in loop timing mode loses the MASTER timing reference (for example, after transmit power level transitions) it sets timing_lock_OK=0, which is communicated to the link partner via the Infofield. Otherwise, timing_lock_OK is set to one.

In MASTER mode, PHY Control enters the PMA_PBO_Exch state after loc_SNR_margin=OK and in SLAVE mode PHY Control enters the PMA_PBO_Exch state after the loc_SNR_margin=OK and minwait_timer expires. In the PMA_PBO_Exch state while Infofield Message<7:6> = 01, the PHY advertises EEE and Fast Retrain capability in octet 12 of the Infofield. When both the local device and remote device advertise EEE capability then EEE is supported. When both the local device and remote device advertise Fast Retrain capability then Fast Retrain is supported. In the PMA_PBO_Exch state, after the MASTER has computed the final desired programmable PBO level, it shall request a PBO change using the requested transmitter setting in the Infofield (octet 7). In SLAVE mode, after the MASTER has requested the desired PBO level, the SLAVE shall request a desired PBO level that is within two levels (within 4 dB) of the requested MASTER PBO level.

Following PBO exchange for both transceivers, each PHY shall announce the next PBO setting using the next transmitter setting (octet 6). Afterwards, each PHY announces a transition to the PMA_Coeff_Exch state using the trans_to_Coeff_Exch=1 and transition_count as described in 126.4.5.1. MASTER initiates the transition to PMA_Coeff_Exch count with the trans_to_Coeff_Exch=1 flag and a transition counter value of $S \times 2^8$. The SLAVE responds prior to the MASTER transition counter reaching $S \times 2^5$ by setting trans_to_Coeff_Exch=1 flag and a transition counter value matching the MASTER. The PMA frame after each transceiver transition_count reaches zero, the PHYs shall enter the PMA_Coeff_Exch state and enable the requested PBO. Therefore, both PHYs enter the PMA_Coeff_Exch state within one PMA frame.

While both MASTER and SLAVE are in state PMA_Coeff_Exch, when either end has computed the programmable THP settings, the programmable THP coefficient exchange process can begin, using the 1.5-octet Coefficient exchange handshake and the 4-octet Coefficient field as follows:

a) During PMA_Coeff_Exch each PHY begins a coefficient exchange by setting the Coeff_Exchange flag to 1 in the Message field.

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b) During coefficient exchange, the transition counter bits are used as the Coefficient Exchange Handshake
   1) Octet 9{Reserved<3:0>}: unused
   2) Coefficient Pair Received, Octet 10<7:6>: 01 for local transmitter pair A, 10 for B, 11 for C and 00 for D (default). This is the handshake to tell the remote unit the last coefficients received.
   3) Coefficient Group Received, Octet 10<5:4>: 01 for coefficients 0:3, 10 for 4:7, 11 for 8:11 and 00 for 12:15 (default). This is the handshake to tell the remote unit the last coefficients received.
   4) Coefficient Pair Sent, Octet 10<3:2>: 01 for remote transmitter pair A, 10 for B, 11 for C and 00 for D (default). This is the handshake to tell the remote unit the current coefficients being sent.
   5) Coefficient Group Sent, Octet 10<1:0>: 01 for 0:3, 10 for 4:7, 11 for 8:11 and 00 for 12:15 (default). This is the handshake to tell the remote unit the current coefficients being sent.

c) The Coefficient field is used to send four 8-bit coefficients in each frame designated by the Coefficient Pair Sent and Coefficient Group Sent bits. The coefficient format is as follows:
   1) 8 bits per coefficient. Use one octet per coefficient in twos complement notation
   2) Coefficient range is –2.0 to 1.984375 in steps of 0.015625
   3) The sign of the coefficients shall be consistent with Equation (126–3)

d) Each PHY begins the exchange by sending pair A coefficients 0:3 with Coefficient Pair Sent=01 and Coefficient Group Sent=01.

e) The remote unit acknowledges by setting Coefficient Pair Received=01 and Coefficient Group Received=01.

f) Following each acknowledgment, the PHY increments through the Coefficient Group and then Coefficient Pair settings until Coefficient Pair Sent=00 and Coefficient Group Sent=00 and Coefficient Pair Received=00 and Coefficient Group Received=00. At this time, coefficient exchange is done and both PHYs set Coeff_Exchange=0.

Following coefficient exchange for both transceivers, each PHY announces a transition to the PMA_Fine_Adjust state (trans_to_Fine_Adjust=1) and starts the transition_count as described in 126.4.5.1. During the first PMA frame after the transition_count reaches zero, the PHYs enter the PMA_Fine_Adjust state and enable the THP precoders with the requested coefficients. At the closure of the THP feedback loop, the initial state of the THP feedback filters shall be the last 16 symbols from the state PMA_Coeff_Exch.

The THP coefficients and PBO setting may not be changed during PMA_Fine_Adjust. The final convergence of the adaptive filter parameters is completed in the PMA_Fine_Adjust state.

After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter Infofield value loc_rcvr_status. The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr_status. When the condition loc_rcvr_status=OK and rem_rcvr_status=OK is satisfied, each PHY announces a transition to the PCS_Test state (trans_to_PCS_Test=1) and start the transition counter as described in 126.4.5.1. For PHYs with the EEE capability, further requirements for this transition are described in 126.3.5.1.

The normal mode of operation corresponds to the PCS_Data state, where PHY Control asserts tx_mode=SEND_N and transmission of data over the link can take place.

PHY Control may force the transmit scrambler state to be initialized to an arbitrary value by requesting the execution of the PCS Reset function defined in 126.3.2.1.

The operation of the maxwait_timer requires that the PHY complete the startup sequence from state SILENT to PMA_Fine_Adjust in the PHY Control state diagram (Figure 126–26) in less than 2000 ms to

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avoid link_status being changed to FAIL by the Link Monitor state diagram (Figure 126–29). To ensure interoperability the timing in Table 126–10 should be observed.

After reaching the PCS_Data state, PHYs with the EEE capability can transition to the LPI receive mode under the control of the link partner and to the LPI transmit mode under control of the local LPI client.

Table 126–10—Recommended startup sequence timing

Master	Recommended maximum time (ms)	Recommended average time (ms)	Slave
SILENT plus (PMA_Training_Init_M state AND en_slave_tx = 0)	350	315	SILENT
(PMA_Training_Init_M state AND en_slave_tx = 1) plus PMA_PBO_Exch state	480	432	PMA_Training_Init_S state plus PMA_PBO_Exch state
PMA_Coeff_Exch state	100	90	PMA_Coeff_Exch state with timing_lock_OK=0
	520	468	Total for PMA Coeff Exch state
PMA_Fine_Adjust state	650	585	PMA_Fine_Adjust state
Total	2000	1800	

126.4.2.5.16 Fast retrain function

PHYs that support the fast retrain capability shall conform to the fast retrain state diagram shown in Figure 126–31. PHYs may request a fast retrain by setting the variable loc_fr_req to TRUE. This causes the transmission of an easily-detected link failure signal specified in 126.4.2.2.2. After completing the link failure signal the PHY shall transition to the PMA_INIT_FR state followed immediately by the PMA_Coeff_Exch state. If the link partner requested THP bypass for fast retrain the PHY bypasses the THP (or set THP coefficients to zero). Otherwise the PHY shall keep its THP turned on with its previously exchanged coefficients, and send PAM2 signaling within a time period equivalent to 18 LDPC frame periods.

After the detection of the link failure signal, a PHY shall transition to the PMA_Coeff_Exch state and respond with PAM2 signaling within a time period equivalent to 18 LDPC frame periods after receiving the link failure signal.

The PAM2 symbols are generated using the PMA sidestream scrambler polynomials shown in Figure 126–11. The training sequence described in 126.3.4 shall be used during fast retraining, with the scramblers free-running from PCS Reset.

Note that reliable traffic on the transmitter may be interrupted when the local receiver requests a fast retrain.

Following the link failure signal, the two link partners transition back to the PMA_Coeff_Exch state and follow the training procedure described in 126.4.2.5.15, with the exception that the initial Infofield countdown values are reduced as indicated in Figure 126–27 and Figure 126–28.

To ensure interoperability the training times in Table 126–11 should be observed during the fast retrain.

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Table 126–11—Recommended fast retrain sequence timing

State	Recommended maximum time (ms)
PMA_Coeff_Exch state	20
PMA_Fine_Adjust state	10

126.4.2.6 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel typically causes the PMA's clients to suspend normal operation.

The Link Monitor function shall comply with the state diagram of Figure 126–29.

Upon power on, reset, or release from power down, the Auto-Negotiation algorithm sets link_control=SCAN_FOR_CARRIER and, during this period, sends fast link pulses to signal its presence to a remote station. If the presence of a remote station is sensed through reception of fast link pulses, the Auto-Negotiation algorithm sets link_control=DISABLE and exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. If the presence of a remote 2.5GBASE-T or 5GBASE-T station is established, the Auto-Negotiation algorithm permits full operation by setting link_control=ENABLE. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

126.4.2.7 Refresh Monitor function

The Refresh monitor is required for PHYs that support the EEE capability. The Refresh monitor operates when the PHY is in the LPI receive mode. The Refresh monitor shall comply with the state diagram of Figure 126–17. The function forces a link retrain if a refresh signal is not reliably detected within a moving time window equivalent to 50 complete quiet-refresh cycles (nominally equal to 16.384/*S* ms), when the PHY is in the lower power receive mode.

126.4.2.8 Clock Recovery function

The Clock Recovery function couples to all four receive pairs. It may provide independent clock phases for sampling the signals on each of the four pairs.

The Clock Recovery function shall provide clocks suitable for signal sampling on each line so that the LDPC FER indicated in 126.4.2.4 is achieved. The received clock signal should be stable and ready for use when training has been completed (loc_rcvr_status=OK). The received clock signal is supplied to the PMA Transmit function by received_clock.

126.4.3 MDI

Communication through the MDI is summarized in 126.4.3.1 and 126.4.3.2.

126.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA on the four pairs BI_DA, BI_DB, BI_DC, and BI_DD are denoted by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and

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tx_symb_vector[BI_DD], respectively. The modulation scheme used over each pair is PAM16. PMA Transmit generates a pulse-amplitude modulated signal on each pair in the following form:

$$x_n = M\left(a_n - \sum_{k=1}^{16} x_{n-k} c_k\right) = a_n + 32m_n - \sum_{k=1}^{16} x_{n-k} c_k \quad (126\text{–}3)$$

$$s(t) = \sum_{n=0}^{\infty} x_n h_T(t - nT) \quad (126\text{–}4)$$

In Equation (126–3), a_n is the PAM16 modulation symbol from the set {–15, –13, –11, –9, –7, –5, –3, –1, 1, 3, 5, 7, 9, 11, 13, 15} to be transmitted at time nT. Each of the 16 THP coefficients c_1, c_2,..., c_{16} per wire pair is represented in two's complement form by 8 bits described in 126.4.2.5. The nonlinear THP operation given by $M(\alpha) = (\alpha + 16) mod 32 - 16$ corresponds to changing the modulation symbol a_n to an augmented modulation symbol $\tilde{a}_n = a_n + 32m_n$ with the integer m_n chosen such that the THP output lies in the interval $-16 \le x_n < 16$. Equation (126–4) describes the convolution of the THP output signals with the transmitter symbol response $h_T(t)$ to obtain the transmit signal $s(t)$ at the MDI. The values of the programmable THP coefficients are exchanged in the Infofield during PMA_Coeff_Exch. The THP filter coefficients shall be fixed after startup.

The nominal power (denoted *Ptx*) and the symbol response of the PMA transmitted signal $s(t)$, shall comply with the electrical specifications given in 126.5. When the link segment does not experience the maximum insertion loss (IL), each transceiver indicates to the link partner that the link partner PMA Transmit signal shall be reduced in increments of 2 dB. The minimum power backoff level requested shall comply with the power backoff schedule in Table 126–12. If a given receiver has sufficient decision point SNR margin, it may choose to request from the link partner larger power backoff (up to 14 dB) than shown in Table 126–12. Additionally, the Slave shall select a PBO level as described in the PMA_PBO_Exch state of 126.4.2.5.15. The PMA Transmit shall be capable of eight power backoff settings in approximately 2 dB steps. The difference between each consecutive power setting shall be 2 ± 0.25 dB, and each step shall be centered at 2 × *n* dB (*n* = 0 to 7) reduction from nominal, with a maximum error of ± 1 dB.

The received signal power at the MDI, *P* (dBm), in Table 126–12, should be the estimate of the average received power across all four pairs from the remote transmitter when the link partner PMA Transmit is at nominal power (after accounting for local transmitter power). If the remote transmitter is not at nominal power during the measurement, the estimate of the received power should be incremented by the amount of power backoff of the link partner transmitter during the measurement. Nominal power refers to the transmit power without any power backoff and is specified in 126.5.3.4. The estimate of the received signal power is stored in registers 1.141 to 1.144 as described in 45.2.1. The values in the length, *L* (m), column in Table 126–12 are for reference only (not required for power backoff evaluation).

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Table 126–12—Power backoff schedule

5GBASE-T		
Received signal power at MDI, *P* (dBm)	**Length *L*(m) (reference)**	**Minimum power backoff (dB)**
$-5.8 < P$	$0 \le L < 35$	8
$-7.0 < P \le -5.8$	$35 \le L < 45$	6
$-9.2 < P \le -7.0$	$45 \le L < 65$	4
$-11 < P \le -9.2$	$65 \le L < 85$	2
$P \le -11$	$85 \le L$	0
2.5GBASE-T		
Received signal power at MDI, *P* (dBm)	**Length *L*(m) (reference)**	**Minimum power backoff (dB)**
$-4.3 < P$	$0 \le L < 45$	2
$P \le -4.3$	$45 \le L$	0

126.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise as follows:

$$r(t) = \sum_{n=0}^{\infty} \tilde{a}_n h_R(t - nT) + w(t) \quad (126–5)$$

In Equation (126–5), $\tilde{a}_n$ are the augmented PAM16 modulation symbols described in 126.4.3.1, $h_R(t)$ denotes the symbol response of the overall channel from the THP precoder to the MDI at the receiver, and $w(t)$ represents the contribution of various noise sources including uncancelled crosstalk. The four signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD are processed within the PMA Receive function to yield the received symbols rx_symb_vector.

126.4.4 Automatic MDI/MDI-X configuration

Automatic MDI/MDI-X configuration is intended to eliminate the need for crossover cables between similar devices. Automatic MDI/MDI-X configuration is required for 2.5GBASE-T and 5GBASE-T devices and shall comply with 40.4.4.1 and 40.4.4.2.

Having established MDI/MDI-X configuration, the receiver shall detect and correct for several configurations of pair swaps and crossovers and arbitrary polarity swaps. The receiver pairs BI_DA, BI_DB, BI_DC, and BI_DD might be connected to the corresponding transmit pairs in any of the following ways with arbitrary polarity:

a) No crossover
b) A/B crossover only
c) C/D crossover only
d) A/B crossover and C/D crossover

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For EEE-capable PHYs, the MDI/MDIX function configuration shall apply to refresh and alert signaling. For PHYs with the fast retrain capability, the MDI/MDIX function configuration shall apply to link failure signaling.

126.4.5 State variables

126.4.5.1 State diagram variables

coeff_exchange_done
: This variable reports that both transceivers have received the corresponding coefficients from the link partner.
Values: TRUE: The coefficient exchange has completed.
FALSE: The coefficient exchange has not completed.

config
: The PMA shall generate this variable continuously and pass it to the PCS via the PMA_CONFIG.indication primitive.
Values: MASTER or SLAVE.

link_control
: The link_control parameter generated by Auto-Negotiation and passed to the PMA via the PMA_LINK.request primitive (see 126.2.1.1).

link_status
: The link_status parameter set by PMA Link Monitor state diagram and communicated through the PMA_LINK.indication primitive.
Values: OK or FAIL.

loc_rcvr_status
: Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY.
Values: OK: The receive link for the local PHY is operating reliably.
NOT_OK: Operation of the receive link for the local PHY is unreliable.

loc_SNR_margin
: This variable reports whether the local device has sufficient SNR margin to continue to the next state. The criterion for setting the parameter loc_SNR_margin is left to the implementer.
Values: OK: The local device has sufficient SNR margin.
NOT_OK: The local device does not have sufficient SNR margin.

master_transition_counter
: This variable reports the current value of the MASTER's transition counter reported in the Infofield defined in 126.4.2.5.
Values: 0 to 2^9.

MessageField_IF
: This variable reports that a receiver has successfully received and decoded the Infofield from the remote device. This variable takes on the value contained in the Message field. If the Message field cannot be decoded or no explicit action is outstanding the value Null is returned.
Values: trans_to_Coeff_Exch, trans_to_Fine_Adjust, trans_to_PCS_Test or Null.

PBO
: PBO is a variable that can take any integer value from 0 to 7 and indicates the power backoff level. Denoting *Ptx* as the maximum nominal power, the PBO values are as follows:
Values: 0, 1, 2, 3, 4, 5, 6, 7, which correspond to transmit power levels of
Ptx, *Ptx*–2 dB, *Ptx*–4 dB, *Ptx*–6 dB, *Ptx*–8 dB, *Ptx*–10 dB, *Ptx*–12 dB, *Ptx*–14 dB respectively.

PBO_next
: PBO_next is a variable that can take any integer value from 0 to 7 and indicates the next power backoff level to be used at the local transmitter. The value is taken from the fixed set of values during PMA_Training_Init_M and PMA_Training_Init_S as described in 126.4.2.5. The value is

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taken from the decoded value of the link partner Infofield during PMA_PBO_Exch
Values:0, 1, 2, 3, 4, 5, 6, 7, which correspond to transmit power levels of
Ptx, *Ptx*–2 dB, *Ptx*–4 dB, *Ptx*–6 dB, *Ptx*–8 dB, *Ptx*–10 dB, *Ptx*–12 dB, *Ptx*–14 dB respectively.

PBO_tx

PBO_tx is a variable that can take any integer value from 0 to 7 and indicates the power backoff level currently used at the local transmitter.
Values:0, 1, 2, 3, 4, 5, 6, 7, which correspond to transmit power levels of
Ptx, *Ptx*–2 dB, *Ptx*–4 dB, *Ptx*–6 dB, *Ptx*–8 dB, *Ptx*–10 dB, *Ptx*–12 dB, *Ptx*–14 dB respectively.

PBO_exchange_done

This variable reports that both transceivers have received the corresponding PBO levels from the link partner.
Values:TRUE: The PBO exchange has completed.
FALSE: The PBO exchange has not completed.

pcs_status

The pcs_status parameter generated by the PCS and passed to the PMA via the PMA_PCSSTATUS.request primitive (see 126.2.2.6).

pma_reset

Allows reset of the PHY Control and Link Monitor state diagrams.
Values:ON or OFF.

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not.
Values:OK: The receive link for the remote PHY is operating reliably.
NOT_OK: Reliable operation of the receive link for the remote PHY is not detected.

THP_next

THP_next is a variable that contains sixteen 8-bit values and describes the next transmitter setting of the THP coefficients. It refers to the programmable THP coefficients selected during coefficient exchange described in 126.4.2.5.
Values:16 coefficients of 8-bit values each. Range is –2.0 to 1.984375 in steps of 0.015625.

THP_tx

THP_tx is a variable that contains sixteen 8-bit values and describes the current transmitter setting of the THP coefficients. It refers to the programmable THP coefficients selected during the coefficient exchange described in 126.4.2.5.
Values:16 coefficients of 8-bit values each. Range is –2.0 to 1.984375 in steps of 0.015625.

trans_to_Coeff_Exch

Message field variable defined in 126.4.2.5 that flags a transition by the local device to the PMA_Coeff_Exch state.
Values:1: The local device transitions to the PMA_Coeff_Exch state on expiration of the transition counter.
0: The local device does not transition to the PMA_Coeff_Exch state.

trans_to_Fine_Adjust

Message field variable defined in 126.4.2.5 that flags a transition by the local device to the PMA_Fine_Adjust state.
Values:1: The local device transitions to the PMA_Fine_Adjust state on expiration of the transition counter.
0: The local device does not transition to the PMA_Fine_Adjust state.

trans_to_PCS_Test

Message field variable defined in 126.4.2.5 that flags a transition by the local device to the PCS_Test state.
Values:1: The local device transitions to the PCS_Test state on expiration of the transition counter.
0: The local device does not transition to the PCS_Test state.

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transition_count

This variable reports the value of the transition counter contained in the Infofield sent to the remote device. Transition_count has to comply with the state diagram description given in 126.4.6.2. When the Message field contains a flag for a state transition, the transition counter denotes the remaining number of Infofield until the next state transition. MASTER initiates the transition to PMA_Coeff_Exch count with the trans_to_Coeff_Exch=1 flag and a counter value of $S \times 2^8$. The SLAVE responds prior to the counter reaching $S \times 2^5$ with the same flag and a count value matching the MASTER. Then both PHY's transition to PMA_Coeff_Exch within one PMA frame. The same sequence is performed in the transition to PMA_Fine_Adjust state and PCS_Test state using the trans_to_Fine_Adjust=1 and trans_to_PCS_Test=1 flags respectively. In EEE-capable PHYs, synchronization of the PMA frames is tightly controlled as described in 126.3.5.1. When the Message field does not contain a flag for a state transition, the transition counter is set to zero and ignored by the receiver.

Values:0 to 2^9.

tx_mode

PCS Transmit sends code-groups according to the value assumed by this variable.

Values: SEND_N: This value is continuously asserted when transmission of sequences of code-groups representing a XGMII data stream take place.

SEND_T: This value is continuously asserted when transmission of sequences of code-groups representing the sequences of code-groups (TA_n, TB_n, TC_n, TD_n) defined in 126.3.4.2 is to take place.

SEND_Z: This value is asserted when transmission of zero code-groups is to take place.

The following variables are required only for PHYs that support the EEE capability:

lpi_refresh_detect

Set TRUE when the receiver has reliably detected refresh signaling and FALSE otherwise. The exact criteria left to the implementer.

pcs_data_mode

Generated by the PMA PHY Control function and indicates whether or not the local PHY may transition its PCS state diagrams out of their initialization states. The current value of the pcs_data_mode is passed to the PCS via the PMA_PCSDATAMODE.indicate primitive. In the absence of the optional EEE and fast retrain capabilities, the PHY operates as if the value of this variable is TRUE.

mtc

mtc is the transition count for a MASTER PHY during normal training and fast retraining. mtc shall be equal to $S \times 2^8$ for normal training and $S \times 2^5$ for fast retrain.

stc

stc is the transition count for a SLAVE PHY during normal training and fast retraining. stc shall be equal to $S \times 2^5$ for normal training and $S \times 2^4$ for fast retrain.

The following six variables are required only for PHYs that support the fast retrain capability:

fr_enable

This variable is set to TRUE if fast retrain is supported. The variable is set to FALSE otherwise. If MDIO is supported, this variable is based on the value of 1.147.0 with the value of TRUE corresponding to 1.147.0 set to 1. If MDIO is not supported, an equivalent method of controlling fast retrain functionality should be provided.

loc_fr_req

Set TRUE when the receiver has detected a link failure condition and is requesting a fast retrain; set FALSE otherwise.

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loc_fr_detect
: Set TRUE when the receiver has reliably detected the link failure signal. It is highly recommended that loc_fr_detect is qualified with the reception of errored blocks at the LDPC decoder output. Set FALSE when the link failure signal is not detected.

send_link_fail
: When TRUE indicates that the PMA should send the link failure signal. When FALSE the variable has no effect.

fr_active
: Set TRUE when the PHY is performing a fast retrain and set FALSE otherwise.

fast_retrain_flag
: Set TRUE after the PHY generates or detects a link failure signal and set FALSE otherwise.

126.4.5.2 Timers

All timers operate in the manner described in 14.2.3.2.

maxwait_timer
: A timer used to limit the amount of time during which a receiver dwells in the SILENT and TRAINING states. The timer shall expire 2000 ms ± 10 ms after being started. This timer is used jointly in the PHY Control and Link Monitor state diagrams. The maxwait_timer is tested by the Link Monitor to force link_status to be set to FAIL if the timer expires and loc_rcvr_status is NOT_OK. See Figure 126–26 and Figure 126–29.

minwait_timer
: A timer used to determine the minimum amount of time the PHY Control stays in the SILENT, PMA_Training_Init_S, PCS_Test and PCS_Data states. The timer shall expire 1 ms ± 0.1 ms after being started.

The following timer is required only for PHYs that support the EEE capability:

lpi_refresh_rx_timer
: This timer is used to monitor link quality during the LPI receive mode. If the PHY does not reliably detect reliable refresh signaling before this timer expires then a full retrain is performed.
Values: The condition lpi_refresh_rx_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 50 complete quiet-refresh signal periods, equivalent to 8.192/*S* ms.

The following two timers are required only for PHYs that support the fast retrain capability:

link_fail_sig_timer
: Determines the period of time the PHY sends the link failure signal.
Values: The condition link_fail_sig_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 8 LDPC frame periods.

fr_maxwait_timer
: Determines the period of time the PHY has to transition its PCS Control State to PCS_Test following a fast retrain before the fast retrain is aborted and a full retrain performed.
Values: The condition fr_maxwait_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 30 ms.

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126.4.5.3 Functions

Exchange_Final_PBO
: This function transmits and receives the final PBO settings using the Infofield as described in 126.4.2.5.

Exchange_THP_Coefficients
: This function compiles and sends to the link partner and receives from the link partner the desired programmable THP coefficients using the Infofield as described in 126.4.2.5.

126.4.5.4 Counters

The following two counters are required only for PHYs that support the fast retrain capability:

fr_tx_counter
: Counts the number of times the PHY initiates a fast link retrain by transmitting the link failure signal. This counter is reflected in MDIO register 1.147.10:6 specified in 45.2.1.94.2.

fr_rx_counter
: Counts the number of times the PHY begins a fast link retrain in response to the detection of link failure signaling from the link partner. This counter is reflected in MDIO register 1.147.15:11 specified in 45.2.1.94.1.

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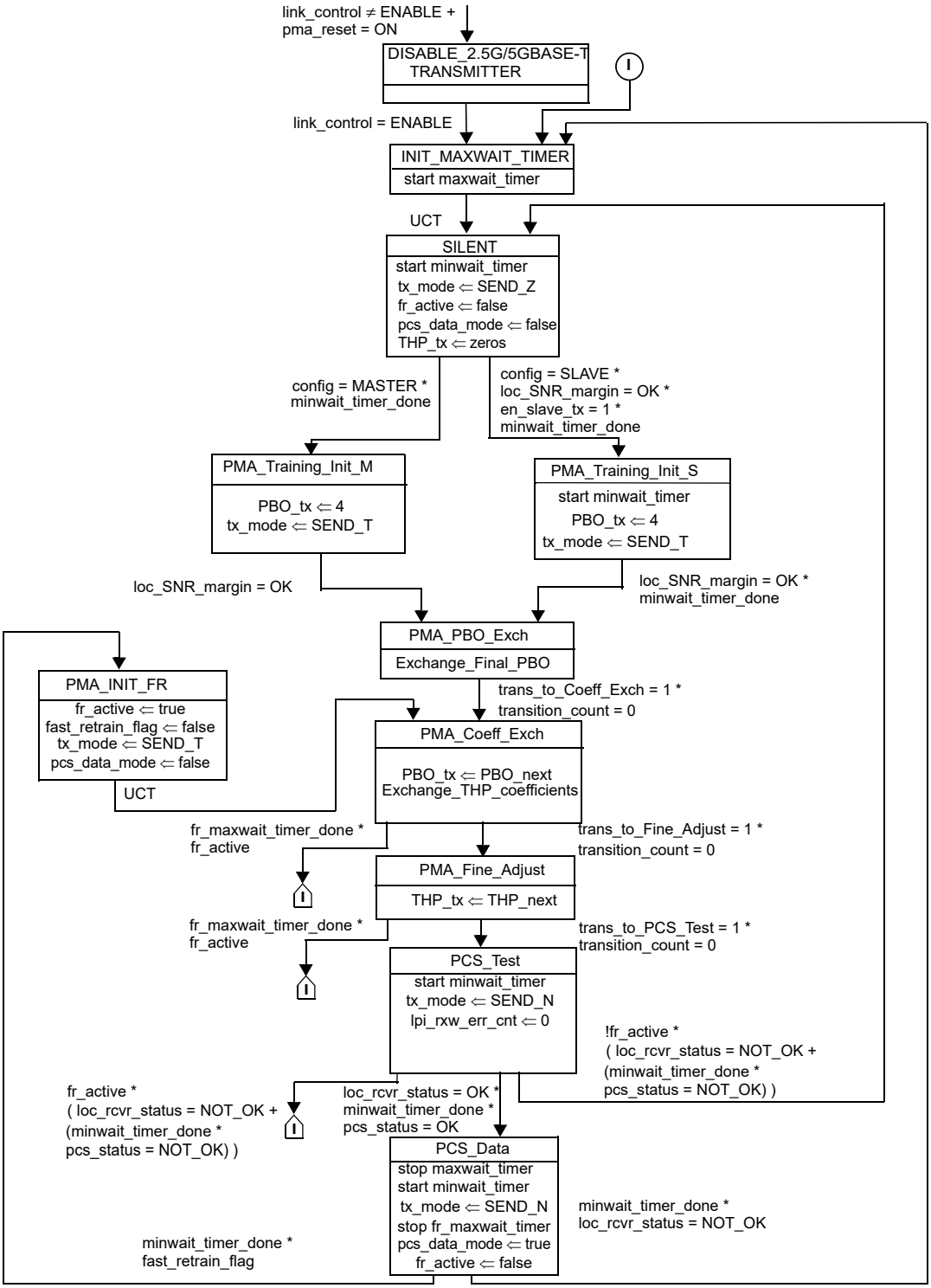
126.4.6 State diagrams

126.4.6.1 PHY Control state diagram



NOTE—For PHYs that do not support the fast retrain capability, the variable fast_retrain_flag is set to FALSE.

Figure 126–26—PHY Control state diagram

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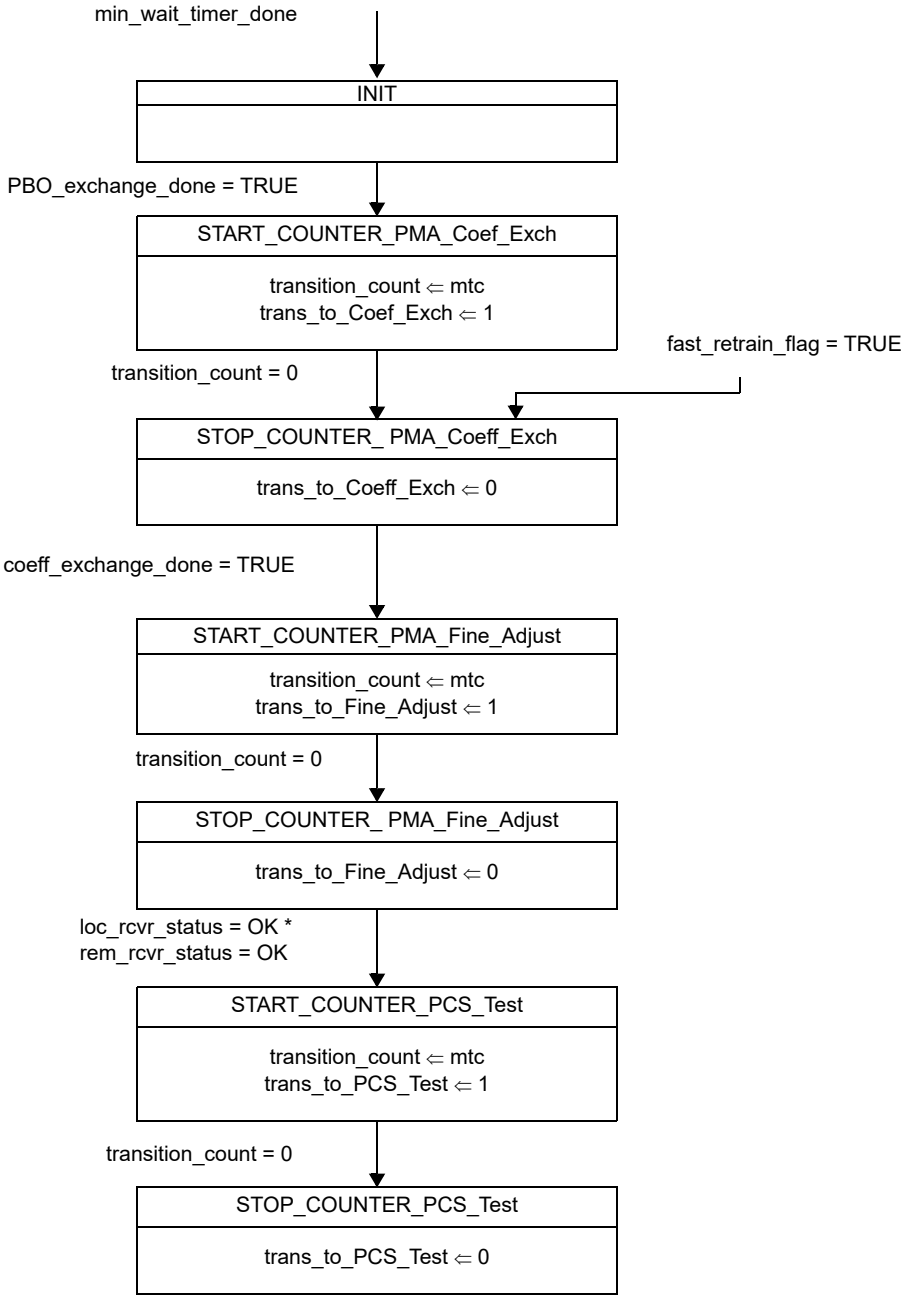
126.4.6.2 Transition counter state diagrams



NOTE—For PHYs that do not support the fast retrain capability, the variable fast_retrain_flag is set to FALSE.

Figure 126–27—MASTER transition counter state diagram

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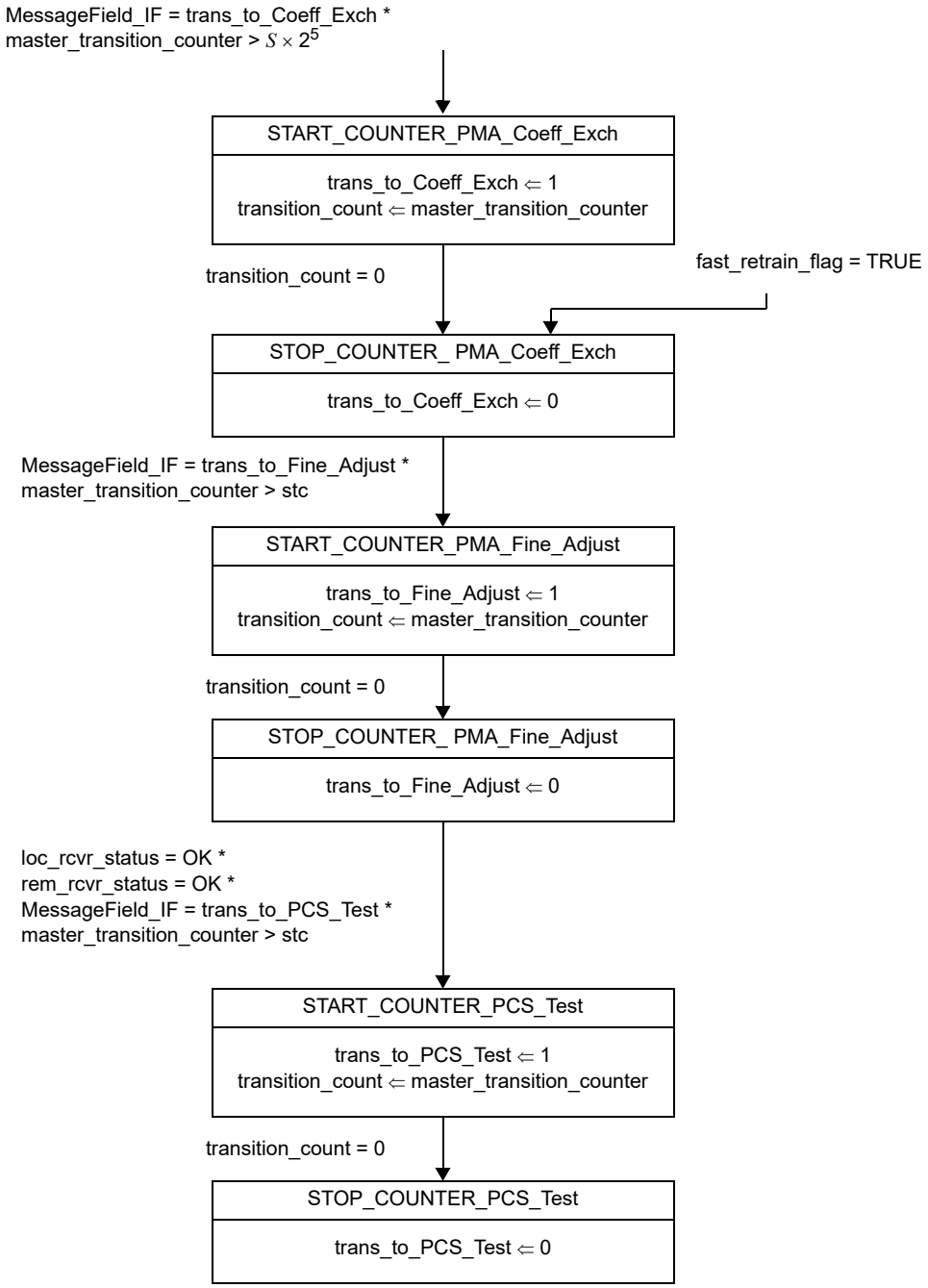

NOTE—For PHYs that do not support the fast retrain capability, the variable fast_retrain_flag is set to FALSE.

Figure 126–28—SLAVE transition counter state diagram

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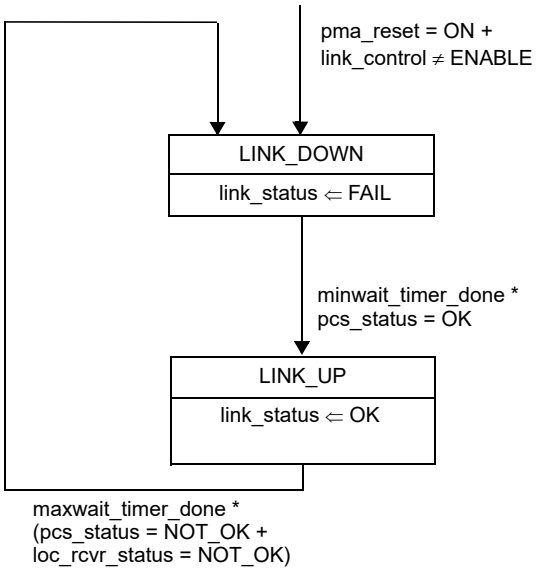
126.4.6.3 Link Monitor state diagram



NOTE 1—maxwait_timer is started in PHY Control state diagram (see Figure 126–26).
NOTE 2—The variables link_control and link_status are designated as link_control_2p5GigT and link_status_2p5GigT, respectively for 2.5GBASE-T, and link_control_5GigT and link_status_5GigT, for 5GBASE-T (by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

Figure 126–29—Link Monitor state diagram

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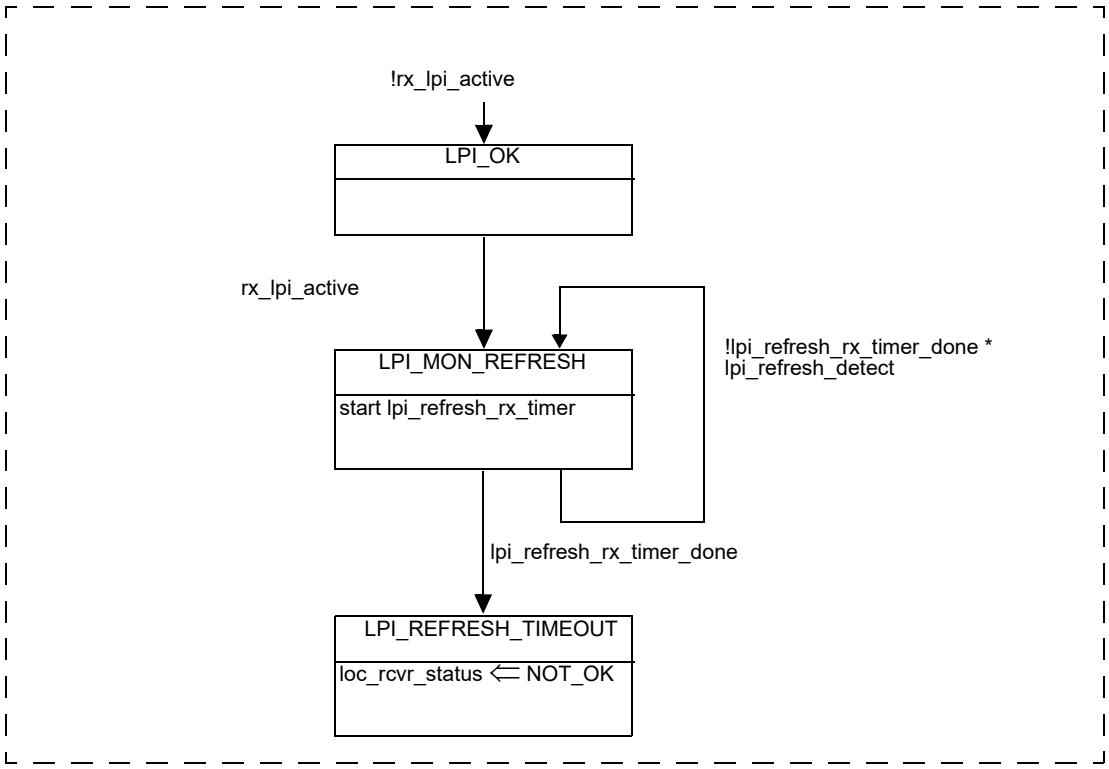
126.4.6.4 EEE Refresh monitor state diagram



NOTE—This state diagram is only required when the PHY supports the EEE capability.

Figure 126–30—EEE Refresh monitor state diagram

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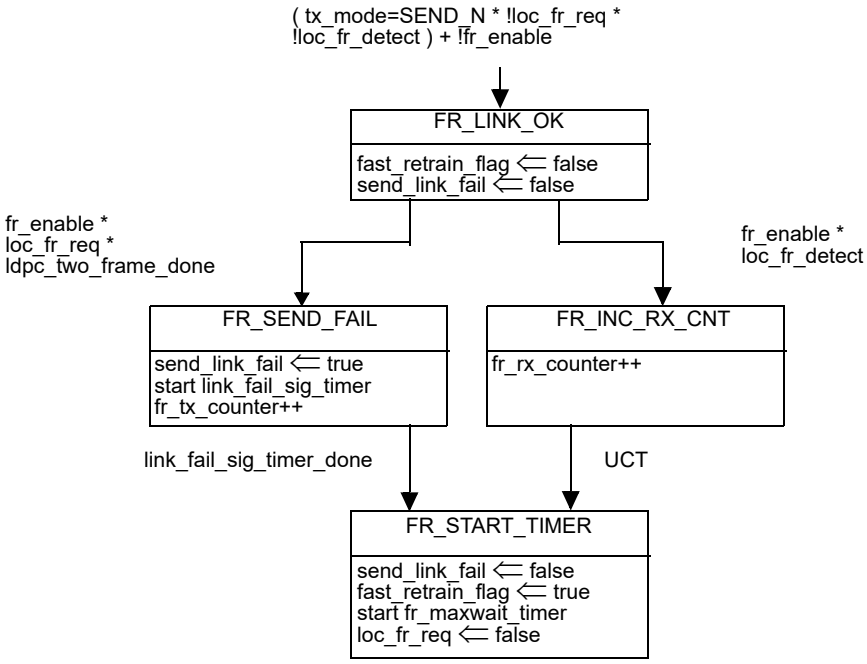
126.4.6.5 Fast retrain state diagram



NOTE—This state diagram is only required when the PHY supports the fast retrain capability.

Figure 126–31—Fast retrain control state diagram

126.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

126.5.1 Electrical isolation

A PHY with a MDI that is a PI (see 33.1.3) shall meet the isolation requirements defined in 33.4.1 or 145.4.1.

A PHY with a MDI that is not a PI shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical isolation shall meet the isolation requirements as specified in J.1.

126.5.2 Test modes

The test modes described next shall be provided to allow for testing of the transmitter waveform, transmitter distortion, transmitted jitter, transmitter droop, and BER testing.

For a PHY with an MDIO management interface, these modes shall be enabled by setting bits 1.132.15:13 (MultiGBASE-T test mode register) of the MDIO Management register set as follows in Table 126–13. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter

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the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation. PHYs without a MDIO shall provide a means to enable these modes for conformance testing.

Table 126–13—MDIO management register settings for test modes

1.132.15	1.132.14	1.132.13	Mode
0	0	0	Normal operation.
0	0	1	Test mode 1—Setting of MASTER transmitter required by SLAVE for transmit jitter test in SLAVE mode.
0	1	0	Test mode 2—Transmit jitter test in MASTER mode.
0	1	1	Test mode 3—Transmit jitter test in SLAVE mode.
1	0	0	Test mode 4—Transmit distortion test.
1	0	1	Test mode 5—Normal operation with no power backoff. This is for the PSD mask and power level test.
1	1	0	Test mode 6—Transmitter droop test mode.
1	1	1	Test mode 7—Pseudo-random test mode for BER Monitor.

Test mode 1 is a mode provided for enabling testing of timing jitter on a SLAVE transmitter. When test mode 1 is enabled, the PHY shall transmit the PMA training pattern (PRBS 33) continually from all four transmitters with the THP turned off, with no power backoff and with the transmitted symbols timed from its local clock source.

Test mode 2 is for transmitter jitter testing when transmitter is in MASTER timing mode. When test mode 2 is enabled, the PHY shall transmit {two +16 symbols followed by two –16 symbols} continually from all four transmitters with the THP turned off, with no power backoff and with the transmitted symbols timed from its local clock source. The transmitter output is a $S \times 100$ MHz signal.

When test mode 3 is enabled on a PHY, the PHY shall transmit, with THP turned off, the data symbol sequence {two +16 symbols followed by two –16 symbols} repeatedly on pair D with the symbols timed from its recovered receive data clock in SLAVE timing mode. A PHY operates in test mode 3 when there is no input signal on pair D. The transmitter output is a $S \times 100$ MHz signal on pair D and shall be silence on pairs A, B, and C.

Test mode 4 is for transmitter nonlinear distortion testing. When test mode 4 is enabled, the PHY shall transmit, with the THP turned off, transmitted symbols, timed from a transmit clock (as specified in 126.5.3.5) in the MASTER timing mode, defined by the bits1.132.12:10 and Table 126–14.

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Table 126–14—MDIO management register settings for transmit frequencies in Test mode 4

1.132.12	1.132.11	1.132.10	Output waveform frequencies in MHz
			Two tone frequency pairs
0	0	0	Reserved
0	1	1	Reserved
1	1	1	Reserved
0	0	1	$S \times (400/1024) \times 47$, $S \times (400/1024) \times 53$
0	1	0	$S \times (400/1024) \times 101$, $S \times (400/1024) \times 103$
1	0	0	$S \times (400/1024) \times 179$, $S \times (400/1024) \times 181$
1	0	1	$S \times (400/1024) \times 277$, $S \times (400/1024) \times 281$
1	1	0	$S \times (400/1024) \times 397$, $S \times (400/1024) \times 401$

The peak-to-peak levels used in this test shall correspond to the ±16 symbol levels and the relative amplitudes of the tones in a two-tone pair shall be within 0.5 dB of each other.

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit as in normal operation but with the power backoff disabled.

Test mode 6 is for testing transmitter droop. When test mode 6 is enabled, the PHY shall transmit the following sequence of data symbols A_n, B_n, C_n, D_n, of 126.4.3.1 continually from all four transmitters, with the THP turned off:

{One hundred twenty eight +16 followed by one hundred twenty eight –16 symbols}.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the LDPC encoder/decoder, the transmit and receive analog front ends of the PHY and a cable connecting two PHYs. This mode shall use the 2.5GBASE-T and 5GBASE-T scrambler and is defined in detail in 126.3.3.

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126.5.2.1 Test fixtures

The following fixtures (illustrated by Figure 126–32, Figure 126–33, and Figure 126–34), or their functional equivalents, can be used for measuring the transmitter specifications described in 126.5.3.

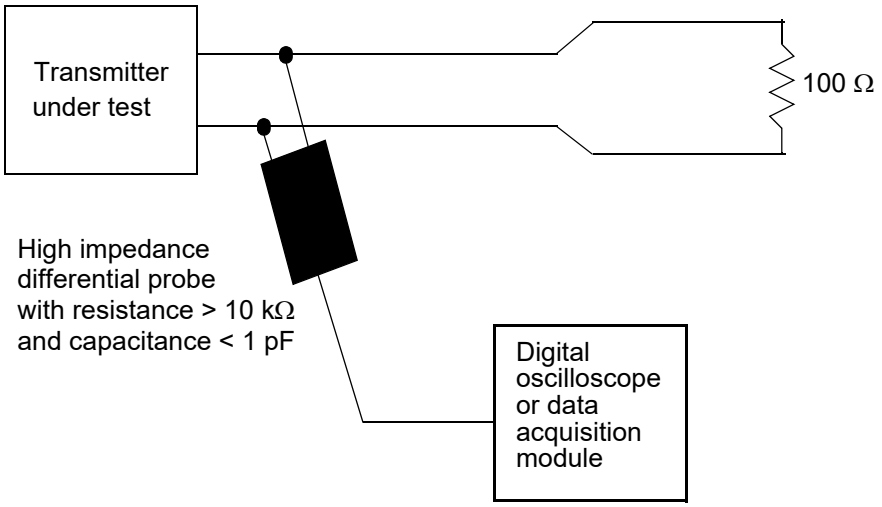

Figure 126–32—Transmitter test fixture 1 for transmitter droop measurement

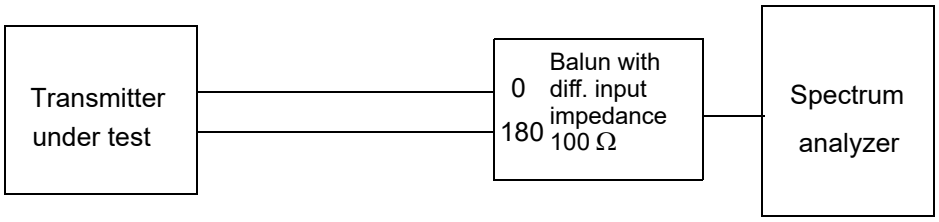

Figure 126–33—Transmitter test fixture 2 for linearity measurement, power spectral density measurement and transmit power level measurement

The high impedance probe shown in Figure 126–32 in transmitter test fixture 1 has resistance > 10 KΩ and capacitance < 1 pF over the frequency range of 1 MHz to $S \times 200$ MHz. Figure 126–33 includes a power summer or balun device to couple the 100 Ω differential output of the transmitter to the 50 Ω single-ended input typically found in a spectrum analyzer input. The center frequency (f_c) of the band pass filter shown in Figure 126–34 is $S \times 100$ MHz ± 200 kHz and the band pass filter noise bandwidth (B_n) is 2 MHz ± 200 kHz. The center frequency (f_c) of the band pass filter shown in Figure 126–35 is 45 MHz ± 200 kHz and the band pass filter noise bandwidth (B_n) is 2 MHz ± 200 kHz.

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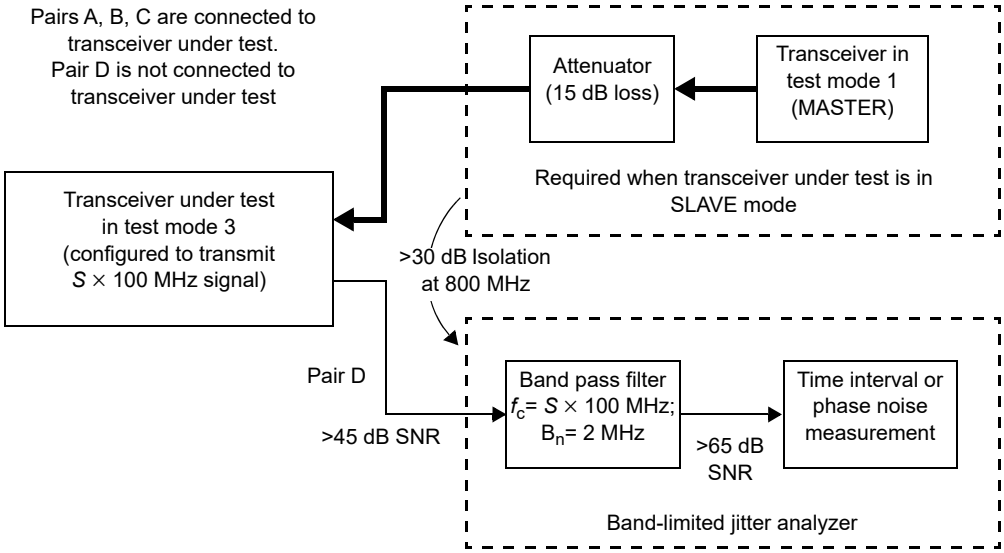

Figure 126–34—Transmitter test fixture 3 for transmitter jitter measurement

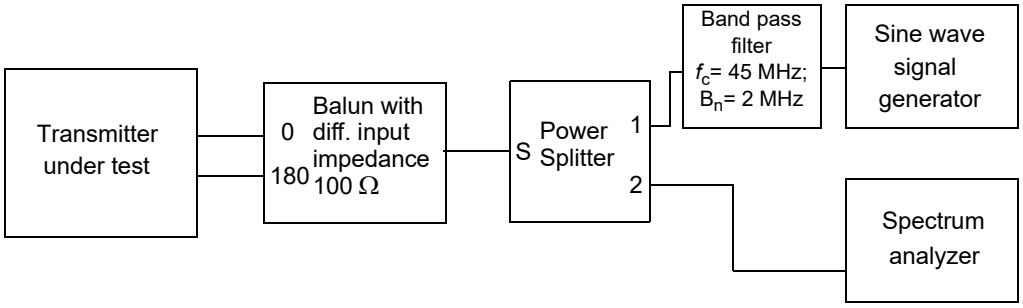

Figure 126–35—Transmitter test fixture 4 for linearity measurement of 2.5GBASE-T with sine wave injected

126.5.3 Transmitter electrical specifications

The PMA provides the Transmit function specified in 126.4.2.2 in accordance with the electrical specifications of this clause. The PMA shall operate with AC-coupling to the MDI.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.

126.5.3.1 Maximum output droop

With the transmitter in test mode 6 and using the transmitter test fixture 1, the magnitude of both the positive and negative droop shall be less than (7.5 + 5/*S*)%, measured with respect to an initial value at 10 ns after the zero crossing and a final value at (10 + 160/*S*) ns after the zero crossing.

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126.5.3.2 Transmitter nonlinear distortion

When in test mode 4 and observing the spectrum of the differential signal output at the MDI using transmitter test fixture 2, for each pair, with no intervening cable, the transmitter nonlinear distortion mask is defined as follows:

The SFDR of the transmitter, with dual tone inputs as specified in test mode 4, shall meet the requirement shown in Equation (126–6).

$$\text{SFDR} \geq \quad 2.5 + \ \min\{52, 58 - 20 \times \log_{10}(f/25)\} \tag{126–6}$$

where

f is the maximum frequency of the two test tones in MHz
SFDR is the ratio in dB of the minimum RMS value of either input tone to the RMS value of the worst intermodulation product in the frequency range of 1 MHz to $S \times 200$ MHz

Additionally, for 2.5GBASE-T, when in test mode 4, at 0 dB PBO, and observing the spectrum of the differential signal output at the MDI using transmitter test fixture 4, for each pair, while injecting a 45 MHz sine wave from the signal generator so that it has an amplitude 7 dB below the peak of the transmitter at the MDI, with no intervening cable, the transmitter nonlinear distortion mask is defined as follows: The SFDR of the transmitter, with dual tone inputs as specified in test mode 4, shall meet the requirement shown in Equation (126–7).

$$\text{SFDR} \geq \quad -5.5 + \ \min\{52, 58 - 20 \times \log_{10}(f/25)\} \tag{126–7}$$

where

f is the maximum frequency of the two test tones in MHz
SFDR is the ratio in dB of the minimum RMS value of either input tone to the RMS value of the worst intermodulation product in the frequency range of 1 MHz to 100 MHz

This specification on transmit linearity is derived from the requirement for interoperability with the far-end device.

126.5.3.3 Transmitter timing jitter

When in test mode 2, the PHY transmits {two +16 symbols followed by two –16 symbols} continually with the THP turned off and with no power backoff. In this mode, the transmitter output should be a $S \times 100$ MHz signal and the RMS period jitter measured at the PHY MDI output shall be less than 7.2 ps for 5GBASE-T and 10.0 ps for 2.5GBASE-T. The RMS period jitter is measured as per the test configuration shown in Figure 126–34 over an integration time interval of $2/S$ ms ± 10%.

The SLAVE mode RMS period jitter test is measured using the test configuration shown in Figure 126–34. For this test, the MASTER PHY is in test mode 1 and the SLAVE PHY is in test mode 3. The MASTER is transmitting the PMA training pattern (PRBS 33) to the SLAVE PHY on pairs A, B, and C. The SLAVE PHY is in loop timing mode, synchronizing its transmit clock to the signals received from the MASTER PHY on pairs A, B, and C. In this configuration, the transmitter output on pair D should be a $S \times 100$ MHz signal and the RMS period jitter measured at the SLAVE PHY MDI output shall be less than 7.2 ps for 5GBASE-T and 10.0 ps for 2.5GBASE-T. The RMS period jitter is measured over an integration time interval of $2/S$ ms ± 10%.

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RMS period jitter over an integration time interval of $2/S$ ms ± 10% is defined as the root mean square period difference from the average period ($T - T_{avg}$), accumulated over a sample size of 200 000 ± 20 000, as shown in Equation (126–8).

$$\text{RMS period jitter} = \sqrt{\frac{\sum[(T - T_{avg})^2]}{\text{Sample size}}} \tag{126–8}$$

126.5.3.4 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation with no power backoff), the transmit power shall be in the range 1.0 dBm to 3.0 dBm and the power spectral density of the transmitter, measured into a 100 Ω, load using the test fixture shown in Figure 126–33 shall be between the upper and lower masks specified in Equation (126–9) and Equation (126–10). In the highest frequency segment, the PSD mask is the maximum of the PSD specified for 2.5G/5GBASE-T, or 6 dB less than that specified in Clause 55 by Equation (55–9). The masks are shown in Figure 126–36.

$$\text{PSD1}(f) \leq \begin{cases} -77.7 - 10 \times \log_{10}(S) & \text{dBm/Hz} \quad 0 < 2\frac{f}{S} \leq 70 \\ -77.7 - 10 \times \log_{10}S - \frac{\left(2\frac{f}{S} - 70\right)}{80} & \text{dBm/Hz} \quad 70 < 2\frac{f}{S} \leq 150 \\ -78.7 - 10 \times \log_{10}S - \frac{\left(2\frac{f}{S} - 150\right)}{58} & \text{dBm/Hz} \quad 150 < 2\frac{f}{S} \leq 730 \\ -78.7 - 10 \times \log_{10}S - \frac{\left(2\frac{f}{S} - 330\right)}{40} & \text{dBm/Hz} \quad 730 < 2\frac{f}{S} \leq 1822 - 400 \times \log_{10}(S) \\ -116 & \text{dBm/Hz} \quad S \times (911 - 200 \times \log_{10}(S)) < f \leq 3000 \end{cases}$$

$$\text{UpperPSD}(f) \leq \max(\text{PSD1}(f), (\text{Equation 55-9}) - 6\ \text{dB})$$

(126–9)

and

$$\text{Lower PSD}\ (f) \geq \begin{cases} -82.2 - 10 \times \log_{10}(S) & \text{dBm/Hz} \quad 5 < 2\frac{f}{S} \leq 50 \\ -82.2 - 10 \times \log_{10}S - \frac{\left(2\frac{f}{S} - 50\right)}{50} & \text{dBm/Hz} \quad 50 < 2\frac{f}{S} \leq 200 \\ -85.2 - 10 \times \log_{10}S - \frac{\left(2\frac{f}{S} - 200\right)}{25} & \text{dBm/Hz} \quad 200 < 2\frac{f}{S} \leq 400 \end{cases} \tag{126–10}$$

where

f is in MHz

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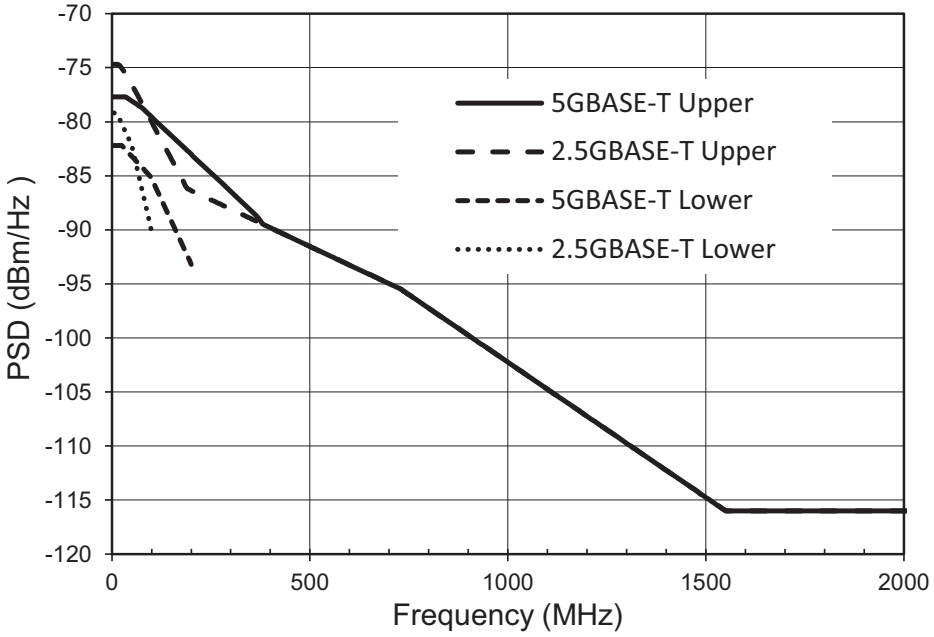

Figure 126–36—Transmitter power spectral density mask

126.5.3.5 Transmit clock frequency

The symbol transmission rate on each pair of the MASTER PHY shall be within the range $S \times 400$ MHz ± 50 ppm.

For a MASTER PHY, when the transmitter is in the LPI transmit mode or when the receiver is in the LPI receive mode the transmitter clock short-term rate of frequency variation shall be less than 0.1 ppm/second. The short-term frequency variation limit shall also apply when switching to and from the LPI mode.

126.5.4 Receiver electrical specifications

The PMA provides the Receive function specified in 126.4.2.4 in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 126.7.

126.5.4.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 126.5.3 and have passed through a link specified in 126.7 shall be received with a BER less than 10^{-12} after LDPC decoding, and sent to the XGMII after link reset completion. This specification can be verified by a frame error ratio less than 7.8×10^{-9} for 800 octet frames with minimum IPG or greater than 220 octet IPG.

126.5.4.2 Receiver frequency tolerance

The receive feature shall properly receive incoming data, per the requirements of 126.5.4.1, with a symbol rate within the range $S \times 400$ MHz ± 50 ppm.

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126.5.4.3 Rejection of External EM Fields

When the cabling system is subjected to electromagnetic fields, currents are generated that may be converted to interference. This specification is provided to limit the sensitivity of the PMA receiver to external EM fields picked up by the cabling and interconnect system. It provides an assessment method of the electromagnetic performance of the link segment and the PHY, including the MDI.

An 80 MHz to 1000 MHz test can be made based on the cable clamp test described in Annex 113A, a 30 meter plug-terminated link segment that meets the requirements of 126.7, and suitable broadband ferrites. All components that are exposed to the induced fields should remain over the ground reference plane. A sine wave with the amplitude held constant over the whole frequency range from 80 MHz to 1000 MHz, with the amplitude calibrated so that the signal power measured at the output of the clamp does not exceed 6 dBm, is used to generate the external electromagnetic field and corresponding currents.

A system integrating a 2.5GBASE-T or 5GBASE-T PHY may perform this test to evaluate anticipated performance in regulatory test environments. Operational requirements of the transceiver during the test are determined by the manufacturer.

NOTE—The 6 dBm limit includes the 10% frequency-dependent variation mentioned in 113A.3.

126.5.4.4 Alien crosstalk noise rejection

While receiving data from a transmitter compliant with specifications in 126.5.3, through a 100 m link segment compliant with the specifications in 126.7, a receiver shall operate with an Ethernet frame error ratio less than 7.8×10^{-9} for 800 octet frames with either a minimum IPG or greater than 220 octet IPG with four noise sources at the specified levels representing alien crosstalk, one connected to each of the four pairs. Independent noise sources should be injected into each MDI input using couplers that do not significantly alter the link segment characteristics. The injected noise shall have a flat spectrum within the following limits: a 3 dB bandwidth extending over at least 10 MHz to $200 \times S$ MHz and a power spectral density such that at the MDI port of the device under test the power spectral density of the injected noise is –137 dBm/Hz and –125 dBm/Hz for 5GBASE-T and 2.5GBASE-T, respectively. A flat noise source is chosen to model the sum of all alien noise sources. See Figure 126–37.

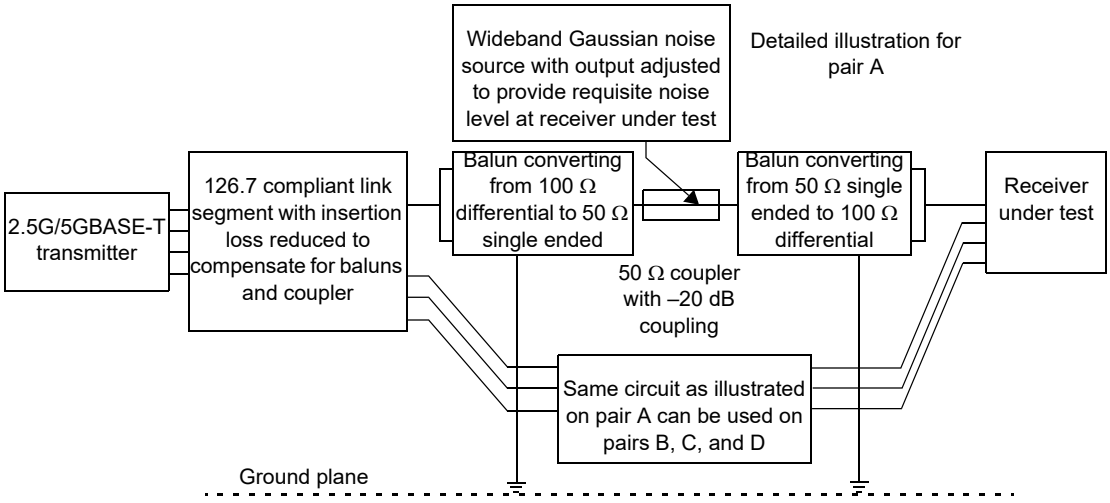

Figure 126–37—Alien crosstalk noise rejection test

The structure shown for injecting the noise in Figure 126–37 is illustrative and alternative approaches are possible. The loss of the coupling structure shown in Figure 126–37, which consists of two baluns and a

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coupler, is approximately 2.5 dB. The overall insertion loss of the link segment together with the insertion loss of the coupling structure should be adjusted to match the insertion loss specified in 126.7.2.1 to within ± 0.5 dB. The balun-coupler-balun structure shown in Figure 126–37 can be replaced by resistively coupling a balanced noise source to the twisted pair using 500 Ω resistors. In either case, calibration of the test setup is required to confirm the overall insertion loss and the injected noise power at the MDI of the receiver under test.

126.6 Management interfaces

2.5GBASE-T and 5GBASE-T make extensive use of the management functions that may be provided by the MDIO (Clause 45), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28). Additional Auto-Negotiation requirements are set forth within this subclause.

126.6.1 Support for Auto-Negotiation

All 2.5GBASE-T and 5GBASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE. All 2.5GBASE-T and 5GBASE-T PHYs shall provide support for Extended Next Pages as defined in 28.2.3.4.2 and shall support and use optimized FLP Burst to FLP burst timing as defined in 28.2.1.1.1, and nlp_link_test_min_timer and link_fail_inhibit_timer as defined in 28.3.2.

Auto-Negotiation is performed as part of the initial set-up of the link, and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-Negotiation signaling is used for the following primary purposes for 2.5GBASE-T and 5GBASE-T:

a) To negotiate that the PHY is capable of supporting 2.5GBASE-T or 5GBASE-T transmission.
b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.

126.6.1.1 2.5GBASE-T and 5GBASE-T use of registers during Auto-Negotiation

When Clause 45 registers are implemented, a 2.5GBASE-T and 5GBASE-T PHYs shall use the management register definitions and values specified in Table 126–15.

Table 126–15—2.5GBASE-T and 5GBASE-T registers

Register	Bit	Name	Description	Type[a]
7.0	7.0.15:0	AN control register	Defined in 45.2.7.1	R/W
7.1	7.1.15:0	AN status register	Defined in 45.2.7.2	RO
7.2, 7.3	7.2.15:0, 7.3.15:0	AN device identifier registers	Defined in 45.2.7.3	R/W
7.5, 7.6	7.5.15:0, 7.6.15:0	AN devices in package registers	Defined in 45.2.7.4	R/W
7.14, 7.15	7.14.15:0, 7.15.15:0	AN package identifier registers	Defined in 45.2.7.5	R/W
7.16	7.16.15:0	AN advertisement register	Defined in 45.2.7.6	R/W

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Table 126–15—2.5GBASE-T and 5GBASE-T registers *(continued)*

Register	Bit	Name	Description	Type[a]
7.19	7.19.15:0	AN LP Base Page ability register	Defined in 45.2.7.7	RO
7.22, 7.23, 7.24	7.22.15:0, 7.23.15:0, 7.24.15:0	AN XNP transmit register	Defined in 45.2.7.8	R/W
7.25, 7.26, 7.27	7.25.15:0, 7.26.15:0, 7.27.15:0	AN LP XNP ability register	Defined in 45.2.7.9	RO
7.32	7.32.15:0	MultiGBASE-T AN control register	Defined in 45.2.7.10	R/W
7.33	7.33.15:0	MultiGBASE-T AN status register	Defined in 45.2.7.11	RO

[a]R/W = Read/Write, RO = Read only

126.6.1.2 2.5GBASE-T and 5GBASE-T Auto-Negotiation page use

2.5GBASE-T and 5GBASE-T PHYs shall exchange a MultiGBASE-T and 1000BASE-T formatted Extended Next Page, as specified in Table 126–16, immediately following the exchange of the Base Page.

Note that the Acknowledge 2 bit is not utilized and has no meaning when used for the 2.5GBASE-T and 5GBASE-T message page exchange.

Table 126–16—2.5GBASE-T and 5GBASE-T Base and Next Pages bit assignments

Bit	Name	Description
Base Page		
D15	Next Page	Defined in 28.2.1.2.6
D14	Acknowledge	Defined in 28.2.1.2.5
D13	Remote Fault	Defined in 28.2.1.2.4
D12	Extended Next Page	Defined in 28.2.1.2.3
D11:D5	Technology Ability Field	Defined in 28.2.1.2.2
D4:D0	Selector Field	Defined in 28.2.1.2.1
Extended Next Page (Message Code Field and Flags Field)		
M10:M0	Next Page message code	Defined in Annex 28C
T	Toggle	Defined in 28.2.3.4.7
Ack2	Acknowledge 2	Defined in 28.2.3.4.6
MP	Message Page	Defined in 28.2.3.4.5
Ack	Acknowledge	Defined in 28.2.3.4.4
NP	Next Page	Defined in 28.2.3.4.3
Extended Next Page (Unformatted Message Code Field)		
U31:U29	Reserved, transmit as 0	

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Table 126–16—2.5GBASE-T and 5GBASE-T Base and Next Pages bit assignments *(continued)*

Bit	Name	Description
U28	2.5GBASE-T ability (1 = support of 2.5GBASE-T and 0 = no support)	Defined in 45.2.7.10.9
U27	5GBASE-T ability (1 = support of 5GBASE-T and 0 = no support)	Defined in 45.2.7.10.8
U26	40GBASE-T ability (1 = support of 40GBASE-T and 0 = no support)	Defined in 45.2.7.10.5
U25	25GBASE-T ability (1 = support of 25GBASE-T and 0 = no support)	Defined in 45.2.7.10.6
U24	10GBASE-T EEE (1 = Advertise EEE capability for 10GBASE-T 0 = Do not advertise EEE capability for 10GBASE-T)	Defined in 45.2.7.14.12
U23	1000BASE-T EEE (1 = Advertise EEE capability for 1000BASE-T 0 = Do not advertise EEE capability for 1000BASE-T)	Defined in 45.2.7.14.13
U22	100BASE-TX EEE (1 = Advertise EEE capability for100BASE-TX 0 = Do not advertise EEE capability for 100BASE-TX)	Defined in 45.2.7.14.14
U21	Reserved	Value always 0
U20	10GBASE-T LD PMA training reset request 0 = Local Device requests that Link Partner run PMA training PRBS continuously) This bit is not defined for 10GBASE-T but reserved for future use.	Defined in 45.2.7.10.13
U19	10GBASE-T Fast retrain ability (1 = Advertise PHY as supporting fast retrain, 0 = Advertise PHY as not supporting fast retrain)	Defined in 45.2.7.10.14. This bit is not defined for 10GBASE-T but reserved for future use
U18	PHY short reach mode (1 = PHY of Local Device is operating in short reach mode 0 = PHY of Local Device is operating in normal mode)	Defined in 45.2.1.79.2
U17	10GBASE-T LD loop timing ability (1 = Advertise 10GBASE-T PHY as capable of loop timing (mandatory for 2.5G, 5G and 40GBASE-T) and 0 = do not advertise PHY as capable of loop timing)	Defined in45.2.7.10.15
U16	10GBASE-T ability (1 = support of 10GBASE-T and 0 = no support)	Defined in 45.2.7.10.4
U15	1000BASE-T half duplex (1 = half duplex and 0 = no half duplex)	
U14	1000BASE-T full duplex (1 = full duplex and 0 = no full duplex)	
U13	Port type bit (1 = multiport device and 0 = single-port device)	Defined in 45.2.7.10.3
U12	MultiGBASE-T MASTER-SLAVE config value (1 = MASTER and 0 = SLAVE) This bit is ignored if 7.32.15 = 0	Defined in 45.2.7.10.2
U11	MultiGBASE-T MASTER-SLAVE manual config enable (1 = manual configuration enable) This bit is intended to be used for manual selection in a particular MASTER-SLAVE mode and is to be used in conjunction with bit 7.32.14.	Defined in 45.2.7.10.1

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Table 126–16—2.5GBASE-T and 5GBASE-T Base and Next Pages bit assignments *(continued)*

Bit	Name	Description
U10	MASTER-SLAVE seed Bit 10 (SB10) (MSB)	
U9	MASTER-SLAVE seed Bit 9 (SB9)	
U8	MASTER-SLAVE seed Bit 8 (SB8)	
U7	MASTER-SLAVE seed Bit 7 (SB7)	
U6	MASTER-SLAVE seed Bit 6 (SB6)	
U5	MASTER-SLAVE seed Bit 5 (SB5)	
U4	MASTER-SLAVE seed Bit 4 (SB4)	
U3	MASTER-SLAVE seed Bit 3 (SB3)	
U2	MASTER-SLAVE seed Bit 2 (SB2)	
U1	MASTER-SLAVE seed Bit 1 (SB1)	
U0	MASTER-SLAVE seed Bit 0 (SB0)	

126.6.1.3 Sending Next Pages

Implementers who do not wish to send additional Extended Next Pages (i.e., Extended Next Pages in addition to those required to perform PHY configuration as defined in this clause) can use Auto-Negotiation as defined in Clause 28. Implementers who wish to send additional Extended Next Pages may do so using the AN XNP transmit registers. See 45.2.7.8.

126.6.2 MASTER-SLAVE configuration resolution

Since both PHYs that share a link segment are capable of being MASTER or SLAVE, a prioritization scheme exists to ensure that the correct mode is chosen. The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using Table 126–17 with the 2.5GBASE-T and 5GBASE-T Technology Ability Next Page bit values specified in Table 126–16 and information received from the link partner. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown in the Arbitration state diagram (see Figure 28–18).

The following four equations are used to determine these relationships:

manual_MASTER = U11 * U12
manual_SLAVE = U11 * !U12
single-port device = !U11 * !U13
multiport device = !U11 * U13

where

U11 is bit 11 of MultiGBASE-T and 1000BASE-T Technology message code
U12 is bit 12 of MultiGBASE-T and 1000BASE-T Technology message code
U13 is bit 13 of MultiGBASE-T and 1000BASE-T Technology message code (see Table 126–16)

A 2.5GBASE-T or 5GBASE-T PHY is capable of operating either as the MASTER or SLAVE. In the scenario of a link between a single-port device and a multiport device, the preferred relationship is for the multiport device to be the MASTER PHY and the single-port device to be the SLAVE. However, other

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topologies may result in contention. The resolution function of Table 126–17 is defined to handle any relationship conflicts.

The resolution shown in Table 126–17 shall be used.

Table 126–17—2.5GBASE-T and 5GBASE-T MASTER-SLAVE configuration resolution table

Local device type	Remote device type	Local device resolution	Remote device resolution
single-port device	multiport device	SLAVE	MASTER
single-port device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	manual_MASTER	SLAVE	MASTER
manual_SLAVE	multiport device	SLAVE	MASTER
multiport device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	single-port device	SLAVE	MASTER
multiport device	single-port device	MASTER	SLAVE
multiport device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	manual_SLAVE	MASTER	SLAVE
manual_MASTER	single-port device	MASTER	SLAVE
single-port device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	multiport device	MASTER	SLAVE
multiport device	multiport device	The device with the higher seed value is configured as MASTER, otherwise SLAVE	The device with the higher seed value is configured as MASTER, otherwise SLAVE
single-port device	single-port device	The device with the higher seed value is configured as MASTER, otherwise SLAVE	The device with the higher seed value is configured as MASTER, otherwise SLAVE
manual_SLAVE	manual_SLAVE	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault
manual_MASTER	manual_MASTER	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault

A 2.5GBASE-T or 5GBASE-T multiport device has higher priority than a single-port device to become the MASTER. In the case where both devices are of the same type, e.g., both devices are multiport devices, the device with the higher MASTER-SLAVE seed bits (SB0, ..., SB10), where SB10 is the MSB, shall become the MASTER and the device with the lower seed value shall become the SLAVE. In case both devices have the same seed value, both should assert link_status_2p5GigT = FAIL for 2.5GBASE-T and link_status_5GigT = FAIL for 5GBASE-T (as defined in 28.3.1) to force a new cycle through Auto-Negotiation. Successful completion of the MASTER-SLAVE resolution shall be treated as MASTER-SLAVE configuration resolution complete.

The method of generating a random or pseudorandom seed is left to the implementer. The generated random seeds should belong to a sequence of independent, identically distributed integer numbers with a uniform distribution in the range of 0 to 2^{11}– 2. The algorithm used to generate the integer should be designed to minimize the correlation between the number generated by any two devices at any given time. A seed

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counter shall be provided to track the number of seed attempts. The seed counter shall be set to zero at startup and shall be incremented each time a seed is generated. When MASTER-SLAVE resolution is complete, the seed counter shall be reset to 0 and bit 7.33.15 shall be set to zero. A MASTER-SLAVE resolution fault shall be declared if resolution is not reached after the generation of seven seeds.

The MASTER-SLAVE manual configuration enable bit (control register bit 7.32.15) and the MASTER-SLAVE config value bit (control register bit 7.32.14) are used to manually set a device to become the MASTER or the SLAVE. In case both devices are manually set to become the MASTER or the SLAVE, this condition shall be flagged as a MASTER-SLAVE configuration fault condition; thus the MASTER-SLAVE configuration fault bit (status register bit 7.33.15) shall be set to logical one. The MASTER-SLAVE configuration fault condition shall be treated as MASTER-SLAVE configuration resolution complete and link_status_2p5GigT, for 2.5GBASE-T, or link_status_5GigT, for 5GBASE-T, shall be set to FAIL, because the MASTER-SLAVE relationship was not resolved. This forces a new cycle through Auto-Negotiation after the link_fail_inhibit_timer has expired. Determination of MASTER-SLAVE values occur on the entrance to the FLP LINK GOOD CHECK state (Figure 28–18) when the highest common denominator (HCD) technology is 2.5GBASE-T or 5GBASE-T. The resulting MASTER-SLAVE value is used by the 2.5GBASE-T or 5GBASE-T PHY Control (126.4.2.5).

If MASTER-SLAVE manual configuration is disabled (bit 7.32.15 is set to 0) and the local device detects that both the local device and the remote device are of the same type (either multiport device or single-port device) and that both have generated the same random seed, it generates and transmits a new random seed for MASTER-SLAVE negotiation by setting link_status to FAIL and cycling through the Auto-Negotiation process again.

The MASTER-SLAVE configuration process returns one of the three following outcomes:

a) *Successful:* Bit 7.33.15 of the MultiGBASE-T status register is set to logical zero and bit 7.33.14 is set to logical one for MASTER resolution or for logical zero for SLAVE resolution. 2.5GBASE-T or 5GBASE-T return control to Auto-Negotiation (at the entrance to the FLP LINK GOOD CHECK state in Figure 28–18) and passes the value MASTER or SLAVE to PMA_config.indication (see 126.2.2.2).
b) *Unsuccessful:* link_status_2p5GigT (2.5GBASE-T) or link_status_5GigT (5GBASE-T) is set to FAIL and Auto-Negotiation restarts (see Figure 28–18).
c) *Fault detected:* Bit 7.33.15 of the MultiGBASE-T status register is set to logical one to indicate that a configuration fault has been detected. This bit also is set when seven attempts to configure the MASTER-SLAVE relationship via the seed method have failed. When a fault is detected, link_status_2p5GigT (2.5GBASE-T) or link_status_5GigT (5GBASE-T) is set to FAIL, causing Auto-Negotiation to cycle through again.

NOTE—MASTER-SLAVE arbitration only occurs if 2.5GBASE-T, 5GBASE-T, 10GBASE-T, 25GBASE-T, 40GBASE-T, or 1000BASE-T is selected as the highest common denominator.

126.7 Link segment characteristics

2.5GBASE-T and 5GBASE-T are designed to operate over Category 5e/Class D 4-pair balanced cabling that meets the additional requirements specified in this subclause. Each of the 2.5GBASE-T four pairs supports an effective data rate of 625 Mb/s per pair, in each direction simultaneously. Each of the 5GBASE-T four pairs supports an effective data rate of 1250 Mb/s per pair, in each direction simultaneously. The term “link segment” used in this clause refers to four twisted pairs operating in full duplex termed “duplex channels.” Specifications for a link segment apply equally to each of the four twisted pairs. All implementations of the balanced cabling link segment specification shall be compatible at the MDI. It is recommended that the guidelines in TIA TSB-5021, ISO/IEC TR 11801-9904, ANSI/TIA-568-C.2, and ISO/IEC 11801:2002/Amendment 1 be considered before the installation of 2.5G/5GBASE-T equipment for any cabling system.

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126.7.1 Cabling system characteristics

2.5G/5GBASE-T requires 4 pair Class D cabling with a nominal impedance of 100 Ω., as specified in ISO/IEC 11801:2002. Operation on other classes of cabling may be supported if the link segment meets the requirements of 126.7.

Additionally:

a) 2.5GBASE-T is an ISO/IEC 11801-2002 Class D and ANSI/TIA-568-C.2 Category 5e application, with additional installation requirements and transmission parameters specified in this clause.
b) 5GBASE-T is an ISO/IEC 11801-2002 Class D and ANSI/TIA-568-C.2 Category 5e application, with additional installation requirements and transmission parameters specified in this clause, including extended frequency performance beyond that specified for Class D and Category 5e.
c) Refer to ISO/IEC TR 11801-9904 and TIA TSB-5021 for support of 2.5GBASE-T and 5GBASE-T over installed cabling.
d) Supported cabling types and distances for 2.5GBASE-T and 5GBASE-T are listed in Table 126–18 and Table 126–19 respectively.

126.7.2 Link segment transmission parameters

A link segment consisting of up to 100 m of Category 5e/Class D 4-pair balanced cabling that meets the transmission parameters of this subclause (including extended frequency specifications for 5GBASE-T) provides a reliable medium for support of 2.5GBASE-T and 5GBASE-T. The transmission parameters of the link segment include insertion loss, delay parameters, nominal impedance, NEXT loss, ACRF, and return loss. In addition, the requirements for the alien crosstalk coupled "between" link segments is specified.

Table 126–18 lists the 2.5GBASE-T supported cabling types and distances.

Table 126–18—2.5 GBASE-T Cabling types and distances

Cabling	Supported link segment distances[a, b]	Cabling references
Class D/ Category 5e	100 m	ISO/IEC 11801-2002, ISO/IEC TR 11801-9904, TIA TSB-5021
Class E/ Category 6	100 m	ISO/IEC 11801-2002, ISO/IEC TR 11801-9904, TIA TSB-5021

[a]Supported link segments up to 100 m shall meet the signal-to-alien crosstalk noise margin criteria specified in 126.7.3.1.
[b]A link segment consisting of up to 100 m of Category 6A/Class EA or better will meet the transmission parameters of 126.7 and provide a reliable medium for 2.5GBASE-T without further qualification.

Table 126–19 lists the 5GBASE-T supported cabling types and distances.

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Table 126–19—5GBASE-T Cabling types and distances

Cabling	Supported link segment distances[a, b]	Cabling references
Class D/Category 5e	100 m	ISO/IEC 11801-2002, ISO/IEC TR 11801-9904, TIA TSB-5021
Class E/Category 6	100 m	ISO/IEC 11801-2002, ISO/IEC TR 11801-9904, TIA TSB-5021

[a]Supported link segments up to 100 m shall meet the signal-to-alien crosstalk noise margin criteria specified in 126.7.3.1.
[b]A link segment consisting of up to 100 m of Category 6A/Class EA or better will meet the transmission parameters of 126.7 and provide a reliable medium for 5GBASE-T without further qualification.

126.7.2.1 Insertion loss

The insertion loss of each duplex channel shall meet the values determined using Equation (126–11).

$$\text{Insertion loss}(f) \leq 1.02\left(1.967 \times \sqrt{f} + 0.023 \times f + \frac{0.05}{\sqrt{f}}\right) + 4 \times 0.04 \times \sqrt{f} \quad \text{(dB)} \qquad (126\text{–}11)$$

where

f is the frequency in MHz; $1 \leq f \leq 100$ for 2.5GBASE-T; $1 \leq f \leq 250$ for 5GBASE-T

This includes the insertion loss of the balanced cabling pairs, including work area and equipment cables plus connector losses within each duplex channel. The factor of 4 in Equation (126–11) corresponds to the number of connectors in the duplex channel.

126.7.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each link segment duplex channel, which includes cable cords and connecting hardware, is 100 Ω.

126.7.2.3 Return loss

In order to limit the noise at the receiver due to impedance mismatches in the cabling system, each link segment duplex channel shall meet the values determined using Equation (126–12). The reference impedance for the return loss specification is 100 Ω.

$$\text{Return loss} \geq \left\{ \begin{array}{ll} 17 & 1 \leq f < 20 \\ 17 - 10\log_{10}\left(\frac{f}{20}\right) & 20 \leq f \leq 250 \end{array} \right\} \quad \text{(dB)} \qquad (126\text{–}12)$$

where

f is the frequency in MHz; $1 \leq f \leq 100$ for 2.5GBASE-T; $1 \leq f \leq 250$ for 5GBASE-T

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126.7.2.4 Coupling parameters between duplex channels comprising one link segment

In order to limit the noise coupled into a duplex channel from adjacent duplex channels, near-end crosstalk (NEXT) loss and attenuation to crosstalk ratio, far-end (ACRF) are specified for each link segment. In addition, each duplex channel can be disturbed by more than one duplex channel. To ensure the total NEXT loss and FEXT loss coupled into a duplex channel is limited, multiple disturber near-end crosstalk (MDNEXT) and multiple disturber ACRF (MDACRF) are specified.

126.7.2.4.1 Differential near-end crosstalk

Since four duplex channels are used to transfer data between PMAs, the NEXT that is coupled into a data carrying channel is from the three adjacent disturbing duplex channels.

In order to limit the crosstalk at the near end of a link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between a duplex channel and the other three duplex channels is specified to meet the bit error ratio specified in 126.5.4.1. The NEXT loss between any two duplex channels of a link segment shall meet the values determined using Equation (126–13). Additionally, the NEXT loss between any two 5GBASE-T duplex channels of a link segment shall meet the values determined using Equation (126–14). The factor of 2 in Equation (126–13) and Equation (126–14) corresponds to the number of connectors at the near-end of the duplex channels.

$$\text{NEXT loss}(f) \geq -20\log_{10}\left(10^{\frac{35.3 - 15\log_{10}(f/100)}{-20}} + 2 \times 10^{\frac{43 - 20\log_{10}(f/100)}{-20}}\right) \quad \text{(dB)} \qquad (126\text{–}13)$$

where

f is the frequency in MHz; $1 \leq f \leq 100$

$$\text{NEXT loss}(f) \geq -20\log_{10}\left(10^{\frac{35.3 - 15\log_{10}(f/100)}{-20}} + 2 \times 10^{\frac{43 - 40\log_{10}(f/100)}{-20}}\right) \quad \text{(dB)} \qquad (126\text{–}14)$$

where

f is the frequency in MHz; $100 < f \leq 250$

Calculations that result in NEXT loss values greater than 60 dB shall revert to a requirement of 60 dB minimum.

126.7.2.4.2 Multiple disturber near-end crosstalk (MDNEXT) loss

Since four duplex channels are used to transfer data between PMAs, the NEXT that is coupled into a data carrying channel is from the three adjacent disturbing duplex channels.

To ensure the total NEXT coupled into a duplex channel is limited, multiple disturber NEXT loss is specified as the power sum of the individual NEXT losses. The power sum loss between a duplex channel and the three adjacent disturbers shall meet the values determined using Equation (126–15). Additionally, the power sum of the individual NEXT loss of each 5GBASE-T duplex channel shall meet the values determined using

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Equation (126–16). The factor of 2 in Equation (126–15) and Equation (126–16) corresponds to the number of connectors at the near-end of the duplex channels.

$$\text{MDNEXT loss}(f) \geq -20\log_{10}\left(10^{\frac{32.3-15\log_{10}(f/100)}{-20}} + 2\times 10^{\frac{40-20\log_{10}(f/100)}{-20}}\right) \quad \text{(dB)} \quad (126\text{–}15)$$

where

f is the frequency in MHz; $1 \leq f \leq 100$

$$\text{MDNEXT loss}(f) \geq -20\log_{10}\left(10^{\frac{32.3-15\log_{10}(f/100)}{-20}} + 2\times 10^{\frac{40-40\log_{10}(f/100)}{-20}}\right) \quad \text{(dB)} \quad (126\text{–}16)$$

where

f is the frequency in MHz; $100 < f \leq 250$

Calculations that result in MDNEXT loss values greater than 57 dB shall revert to a requirement of 57 dB minimum.

126.7.2.4.3 Multiple disturber power sum near-end crosstalk (PSNEXT) loss

PS NEXT loss is determined by summing the power of the three individual pair-to-pair differential NEXT loss values over the frequency range 1 MHz to 100 MHz for 2.5GBASE-T and 1 MHz to 250 MHz for 5GBASE-T as follows in Equation (126–17).

$$\text{PSNEXT loss}(f) = \left(-10\log_{10}\sum_{i=1}^{n} 10^{\frac{-NL(f)i}{10}}\right) \quad \text{(dB)} \quad (126\text{–}17)$$

where

$NL(f)i$ is the magnitude in dB of NEXT loss at frequency f (in MHz) of pair combination i

i is the pair-to-pair combination (1 to n)

n is the number of pair-to-pair combinations ($n = 3$)

126.7.2.4.4 Attenuation to crosstalk ratio, far-end (ACRF)

Attenuation to crosstalk ratio, far-end (ACRF) is specified in order to limit the crosstalk at the far end of each link segment duplex channel and meet the bit error ratio objective specified in 126.5.4.1. Far-end crosstalk (FEXT) is crosstalk that appears at the far end of a duplex channel (disturbed channel), which is coupled from another duplex channel (disturbing channel) with the noise source (transmitters) at the near end.

FEXT loss is defined in Equation (126–18).

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$$\text{FEXT loss}(f) = 20\log_{10}\left(\frac{V_{pds}(f)}{V_{pcn}(f)}\right) \quad \text{(dB)} \tag{126–18}$$

and ACRF is defined in Equation (126–19).

$$\text{ACRF}\ (f) = 20\log_{10}\left(\frac{V_{pds}(f)}{V_{pcn}(f)}\right) - \text{SLS\_Loss}\ (f)\ \text{(dB)} \tag{126–19}$$

where

V_{pds} is the peak voltage of disturbing signal (near-end transmitter)
V_{pcn} is the peak crosstalk noise at far end of disturbed channel
SLS_Loss is the insertion loss of disturbed channel in dB

The worst pair ACRF between any two duplex channels shall meet the values determined using Equation (126–20). The factor of 4 in Equation (126–20) corresponds to the number of connectors the duplex channels.

$$\text{ACRF} \geq -20\log_{10}\left(10^{\frac{23.8 - 20\log_{10}(f/100)}{-20}} + 4 \times 10^{\frac{35.1 - 20\log_{10}(f/100)}{-20}}\right) \quad \text{(dB)} \tag{126–20}$$

where

f is the frequency in MHz; $1 \leq f \leq 100$ for 2.5GBASE-T; $1 \leq f \leq 250$ for 5GBASE-T

ACRF values that correspond to FEXT loss values of greater than 70 dB are for information only.

126.7.2.4.5 Multiple disturber attenuation to crosstalk ratio, far-end (MDACRF)

Since four duplex channels are used to transfer data between PMAs, the FEXT that is coupled into a data carrying channel is from the three adjacent disturbing duplex channels. To ensure the total FEXT coupled into a duplex channel is limited, multiple disturber ACRF is specified as the power sum of the individual ACRF disturbers. The power sum loss between a duplex channel and the three adjacent disturbers shall meet the values determined using Equation (126–21). The factor of 4 in Equation (126–21) corresponds to the number of connectors the duplex channels.

$$\text{MDACRF} \geq -20\log_{10}\left(10^{\frac{20.8 - 20\log_{10}(f/100)}{-20}} + 4 \times 10^{\frac{32.1 - 20\log_{10}(f/100)}{-20}}\right) \quad \text{(dB)} \tag{126–21}$$

where

f is the frequency in MHz; $1 \leq f \leq 100$ for 2.5GBASE-T; $1 \leq f \leq 250$ for 5GBASE-T

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126.7.2.4.6 Multiple disturber power sum attenuation to crosstalk ratio, far-end (PS ACRF)

PS ACRF is determined by summing the power of the three individual pair-to-pair differential ACRF values over the frequency range 1 MHz to 100 MHz for 2.5GBASE-T and 1 MHz to 250 MHz for 5GBASE-T as follows in Equation (126–22):

$$\text{PSACRF}\ (f) = -10\log_{10}\sum_{i=1}^{i=n} 10^{\frac{-ACR(f)i}{10}} \quad \text{(dB)} \qquad (126\text{–}22)$$

where

ACRF(f)i is the magnitude of ACRF at frequency *f* of pair combination *i*
i is the pair-to-pair combination (1 to *n*)
f is the frequency in MHz
n is the number of pair-to-pair combinations (*n* = 3)

126.7.2.5 Maximum link delay

The propagation delay of a link segment shall not exceed 570 ns at all frequencies between 2 MHz and 250 MHz.

126.7.2.6 Link delay skew

The difference in propagation delay, or skew, between all duplex channel pair combinations of a link segment, under all conditions, shall not exceed 50 ns at all frequencies from 2 MHz to 250 MHz. It is a further functional requirement that, once installed, the skew between any two of the four duplex channels due to environmental conditions shall not vary more than 10 ns within the above requirement.

126.7.3 Coupling parameters between link segments

Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. An signal-to-alien crosstalk noise criteria is specified to ensure the total alien NEXT loss and alien FEXT loss coupled between link segments is limited. See TIA TSB-5021 and ISO/IEC TR 11801-9904 for guidance on identifying link segments and use cases for 2.5GBASE-T and 5GBASE-T.

126.7.3.1 Alien crosstalk limited signal-to-noise ratio criteria

Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. To ensure the total alien NEXT loss and alien FEXT loss coupled between link segments are limited a figure of merit denoted as the alien crosstalk limited signal-to-noise ratio criteria ($ALSNR_{\text{criteria}}$) is specified. The $ALSNR_{\text{criteria}}$ is the numerical difference between the *ALSNR* derived from measurements of its alien crosstalk and insertion loss parameters, denoted $ALSNR_{\text{link}}$ and the link segment SNR sufficient to support the objective BER, denoted SNR_{linkreq}. SNR_{linkreq} includes SNR margin to account for power backoff uncertainties and the differences between what is theoretically possible and what is feasible in the implementation of receivers. An additional noise term is added to better model receiver losses which change the achievable ALSNR criterion with insertion loss.

The $ALSNR_{\text{criteria}}$ algorithm enables determination of $ALSNR_{\text{link}}$ for disturbed link segments with 2.5G and 5G signaling rates from any number of disturbing link segments with all possible combinations of 1G/2.5G/5G/10G signaling rates. Guidelines for evaluating the ALSNR criterion in installed cabling,

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including the selection of the number of disturbing link segments and signaling rates to consider are addressed in TIA TSB-5021 and ISO/IEC TR 11801-9904.

For a compliant 2.5GBASE-T link segment, $ALSNR_{\text{criteria}}$ shall be greater than zero for every possible permutation of 1000BASE-T and 2.5GBASE-T running on the disturbing link segments. For a compliant 5GBASE-T link segment, $ALSNR_{\text{criteria}}$ shall be greater than zero for every possible permutation of 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T on the disturbing link segments.

The $ALSNR_{\text{criteria}}$ may be determined by the result of the following nine-step procedure:

Indices

i is the 1-4 pair of the disturbed link segment

k is the 1-4 pair of the disturbing link segment

m is the index of the disturbing link segment

M is the number of disturbing link segments

Step 1. Measure the insertion loss of all the pairs in the disturbed link segment and the disturbing link segments in the frequency range given by Table 126–20.

Table 126–20—Frequency range of IL measurements

Application running on the disturbed link segment	Frequency range of measurement
2.5GBASE-T	$1 \le f \le 100$ MHz
5GBASE-T	$1 \le f \le 200$ MHz

Denote each pair of the disturbed link segment insertion loss as $IL\_disturbed_i$. Denote each pair of the disturbing link segment insertion loss as $IL\_disturbing_{k,m}$. Where i denotes the pair of the disturbed link segment, k denotes the pair of the disturbing link segment and M denotes the index number of the disturbing link segment.

NOTE—While disturbing signals may contain higher frequencies, the received power that determines the power backoff is dominated by the power below 100 MHz, for 2.5GBASE-T and 5GBASE-T, and neglecting the frequencies above 100 MHz has no appreciable effect in computing the 2.5GBASE-T or 5GBASE-T power backoff. When 10GBASE-T power backoff is to be computed, frequencies up to at least 200 MHz should be used.

Step 2. Determine the Received Signal Transmit Power including PBO, S_i, for each pair, i, of the disturbed link segment, at each frequency point.

Step 2a. Determine the nominal (i.e., without power backoff) Received Signal Transmit Power for each pair of the disturbed link segment, $RxTPdBmdisturbed_i$ at each frequency point by using Equation (126–23).

$$RxTPdBmdisturbed_i(f) = TemplatePSDdisturbed_i(f) + ILdisturbed_i(f) \quad \text{(dBm/Hz)} \qquad (126\text{–}23)$$

where

$TemplatePSDdisturbed_i$ is provided by Table 126–21, according to which application is running on the disturbed link segment. This is calculated over the frequency range selected in Step 1.

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Table 126–21— Template PSD for disturbed link segment

Application running on the disturbed link segment	Template PSD (dBm/Hz)
2.5GBASE-T	$-77.9 + 20\log_{10}\left(\frac{\lvert\sin(\pi f/200)\rvert}{\pi f/200}\right) - 10\log_{10}\left(1+\left(\frac{f}{490}\right)^4\right)$
5GBASE-T	$-80.7 + 20\log_{10}\left(\frac{\lvert\sin(\pi f/400)\rvert}{\pi f/400}\right) - 10\log_{10}\left(1+\left(\frac{f}{490}\right)^4\right)$

Step 2b. Calculate the Received Signal Transmit power, for each pair of the disturbed link segment, *i*, at each frequency point, to a linear magnitude and multiply by the frequency step size in Hz using Equation (126–24).

$$RxTPmWdisturbed_i(f) = \Delta f \left(10^{\frac{(RxTPdBmdisturbed_i(f))}{10}} \right) \quad \text{(mW)} \tag{126–24}$$

where

Δf is the step size between frequency points at that data point in Hz

Step 2c. Determine the Total Received Power in dBm, $TotalRxTPdBmdisturbed_i$, for each pair, *i*, of the disturbed cable using Equation (126–25).

$$TotalRxTPdBmdisturbed_i = 10\log_{10}\left(\sum_{f=fmin}^{fmax} RxTPmWdisturbed_i(f) \right) \quad \text{(dBm)} \tag{126–25}$$

where

fmin and fmax are given in Table 126–20

Step 2d. Determine the power backoff for the disturbed cable, $PBO_{\text{disturbed}}$, by calculating the mean value of $TotalRxTPdBmdisturbed_i$ across the pairs using Equation (126–26), and determine $PBO_{\text{disturbed}}$ from Table 126–12 for 2.5GBASE-T, or for 5GBASE-T, depending on for which PHY the disturbed link segment is being qualified.

For each value of *m*:

$$\overline{RxTPdisturbed} = \frac{\left(\sum_{i=1}^{4} TotalRxTPdBmdisturbed_i \right)}{4} \tag{126–26}$$

Step 2e. Calculate the Received Signal Transmit PSD including PBO, S_i, for each pair of the disturbed link segment at each frequency point by using Equation 126-28.

For *i*=1 to 4:

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$$S_i(f) = RxTPdBmdisturbed_i(f) - PBO_{\text{disturbed}} \quad (126–27)$$

Step 3. For each disturber type being evaluated on a disturbing link segment, determine the power backoff for the disturber type running on each disturbing link segment, PBO_m. This step involves selecting which application is running on each disturbing link segment (see Step 9 for further details of calculations for all possible permutations).

NOTE 1—The PBO for 1000BASE-T is always 0 dB, and the calculations of this step do not apply.

NOTE 2—When 2.5GBASE-T is running on the disturbed link segment, then the calculations only need to consider 2.5GBASE-T and 1000BASE-T running on the disturbing link segments.

Step 3a. Determine the nominal (i.e., without power backoff applied) Received Signal Transmit Power, $RxTPdBmdisturbing_{k,m}$, for each pair, k, of the disturbing link segment, m, at each frequency point by using Equation (126-29).

$$RxTPdBmdisturbing_{k,m}(f) = TemplatePSD_m(f) + ILdisturbing_{k,m}(f) \text{ (dBm/Hz)} \quad (126–28)$$

where

$TemplatePSD_m(f)$ is provided by Table 126–22, for the disturber type being evaluated

Table 126–22—Template PSD for disturbing link segment

Application running on the disturbed link segment	Template PSD (dBm/Hz)
1000BASE-T	$-72.38 + 20\log_{10}\left(\frac{\lvert\sin(\pi f/125)\rvert}{\pi f/125}\right) - 10\log_{10}\left(1+\left(\frac{f}{100}\right)^2\right) + 10\log_{10}\left(0.625 + 0.375 \times \cos\frac{2\pi f}{125}\right)$
2.5GBASE-T	$-77.9 + 20\log_{10}\left(\frac{\lvert\sin(\pi f/200)\rvert}{\pi f/200}\right) - 10\log_{10}\left(1+\left(\frac{f}{490}\right)^4\right)$
5GBASE-T	$-80.7 + 20\log_{10}\left(\frac{\lvert\sin(\pi f/400)\rvert}{\pi f/400}\right) - 10\log_{10}\left(1+\left(\frac{f}{490}\right)^4\right)$
10GBASE-T	$-80.89 + 20\log_{10}\left(\frac{\lvert\sin(\pi f/800)\rvert}{\pi f/800}\right) - 10\log_{10}\left(1+\left(\frac{f}{490}\right)^4\right)$

Step 3b. Convert the Received Signal Transmit power for each pair, k, of each disturbing link segment, m, at each frequency point to a linear magnitude and multiply by the frequency step size using Equation (126–29).

$$RxTPmWdisturbing_{k,m}(f) = \Delta f \left(10^{\frac{RxTPdBmdisturbing_{k,m}(f)}{10}} \right) \text{ (mW)} \quad (126–29)$$

where

Δf is the step size between frequency points at that data point in Hz

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Step 3c. Calculate the Total Received Power in dBm, for each pair, *k*, of each disturbing link segment, *m*, by adding the values at each frequency point and converting to dBm using Equation (126–30).

$$TotalRxTPdBmdisturbing_{k,m} = 10\log_{10}\left(\sum_{f=fmin}^{fmax} RxTPmWdisturbing_{k,m}(f)\right) \quad \text{(dBm)} \quad (126–30)$$

where

fmin and fmax are given in Table 126–20

Step 3d. Determine the power backoff, PBO_m,for each disturbing link segment, *m*, by calculating the mean value of $TotalRxTPdBmdisturbing_{k,m}$ across the pairs, using Equation (126–31) for each link segment, and then determining, PBO_m, from Table 126–12 for 2.5GBASE-T and 5GBASE-T, and Table 55–11 for 10GBASE-T running on the disturbing link segment. The PBO for 1000BASE-T is always 0 dB.

For each value of *m*:

$$\overline{RxTPdisturbing_m} = \frac{\left(\sum_{i=1}^{4} TotalRxTPdBmdisturbing_{k,m}\right)}{4} \quad (126–31)$$

Step 4. Measure the ANEXT and AFEXT combinations for each disturbing link segment, *m*. Each disturbing link segment will provide 16 ANEXT combinations and 16 AFEXT combinations.

Denote the measurements as $\text{ANEXTmeasurement}_{i,k,m}$ and $\text{AFEXTmeasurement}_{i,k,m}$.

where

i is the 1-4 pair of the disturbed link segment
k is the 1-4 pair of the disturbing link segment
m is the 1- *M* index of the disturbing link segment
M is the number of disturbing link segments

Step 5. Calculate the alien crosstalk components including PBO for each alien crosstalk measurement for each disturbing link segment at each frequency point using Equation (126–32) and Equation (126–33). Note that the frequency points are measured or interpolated to the same frequencies used for the insertion loss measurements.

$$\text{ANEXTcomponent}_{i,k,m}(f) = TemplatePSD_m(f) - \text{ANEXTmeasurement}_{i,k,m}(f) - PBO_m \quad \text{(dBm/Hz)} \quad (126–32)$$

$$\text{AFEXTcomponent}_{i,k,m}(f) = TemplatePSD_m(f) - \text{AFEXTmeasurement}_{i,k,m}(f) - PBO_m \quad \text{(dBm/Hz)} \quad (126–33)$$

where

$TemplatePSD_m(f)$ and PBO_m are from Step 3a and Step 3d, respectively

Step 6. Determine the total noise received by each pair, *i*, of the disturbed link segment by the power summation of the ANEXT and AFEXT Components together at each frequency point using Equation (126–34).

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$$N_i(f) = 10\log_{10}\left(\sum_{m=1}^{M}\left(\sum_{k=1}^{4}\left(10^{\frac{\text{ANEXTcomponent}_{i,k,m}(f)}{10}} + 10^{\frac{\text{AFEXTcomponent}_{i,k,m}(f)}{10}}\right)\right) + 10^{\frac{addnoise}{10}}\right) \text{ (dBm/Hz)} \quad (126\text{–}34)$$

where

addnoise is given in Table 126–23

Table 126–23—Values of *addnoise* noise term

Application running on the disturbed link segment	*addnoise* noise term
2.5GBASE-T	–129 dBm/Hz
5GBASE-T	–135 dBm/Hz

Step 7. Determine the alien signal-to-noise ratio, ALSNR for each pair, *i*, of the disturbed link segment using Equation (126–35).

$$ALSNR_i = \left(\frac{1}{fmax}\right)\sum_{f=fmin}^{fmax}(S_i(f) - N_i(f))\Delta f \qquad \text{(dB)} \quad (126\text{–}35)$$

where

$fmin$ *and* $fmax$ are given in Table 126–20, and Δf is the step size between frequency points at each data point in the same frequency units (e.g., both MHz or both Hz)

Determine the minimum of $ALSNR_i$ across all pairs, providing $ALSNR_{\text{link}}$.

Step 8. Determine the $ALSNR_{\text{criteria}}$ using Equation (126–36).

$$ALSNR_{\text{criteria}} = ALSNR_{\text{link}} - SNR_{\text{linkreq}} \quad (126\text{–}36)$$

where

$SNR_{\text{linkreq}} = 28$ dB

Step 9. Multiplicity

Steps 1–8 determine the $ALSNR_{\text{link}}$ for a given application running on the disturbed link segment, and a given permutation of applications running on the disturbing link segments.

To calculate the worst case permutation of disturbers running on the disturbing link segments, repeat steps 3–8 using every possible permutation of disturbers running on the disturbing link segments, and determine $ALSNR_{\text{criteria}}$ for each permutation of disturbing applications.

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126.8 MDI specification

This subclause defines the MDI. The link topology requires a crossover function in a DTE-to-DTE connection. See 126.4.4 for a description of the automatic MDI/MDI-X configuration.

126.8.1 MDI connectors

Eight-pin connectors meeting the requirements of IEC 60603-7-4 (unscreened) or IEC 60603-7-5 (screened) shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figure 126–38 and Figure 126–39. The assignment of PMA signals to connector contacts for PHYs is shown in Table 126–24.

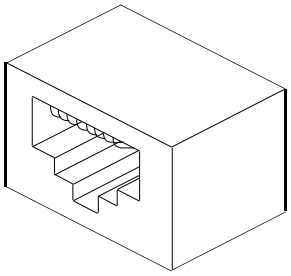

Figure 126–38—MDI connector

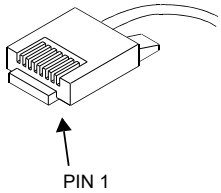

Figure 126–39—Balanced cabling connector

Table 126–24—Assignment of PMA signal to MDI and MDI-X pin-outs

Contact	MDI	MDI-X
1	BI_DA+	BI_DB+
2	BI_DA–	BI_DB–
3	BI_DB+	BI_DA+
4	BI_DC+	BI_DD+
5	BI_DC–	BI_DD–
6	BI_DB–	BI_DA–
7	BI_DD+	BI_DC+
8	BI_DD–	BI_DC–

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126.8.2 MDI electrical specifications

The MDI connector (jack) shall meet the following requirements for FEXT, Return Loss, and Impedance Balance when mated with a nominal balanced cabling connector (plug). The mated connection shall meet transmission performance requirements for category 5e connecting hardware found in ANSI/TIA 568-C.2, section 6.8.

NOTE—Use of a compliant test plug as defined in ANSI/TIA 568-C.2, annex C, section C.4.10 will help ensure connecting hardware transmission performance for these purposes.

126.8.2.1 MDI FEXT

The MDI connector (jack) shall meet the FEXT requirements as specified in Equation (126–37) between all contact pair combinations shown in Table 126–24.

$$\text{FEXT loss} \geq 43.1 - 20\log_{10}(f/100) \quad \text{(dB)} \tag{126–37}$$

where

f is the frequency over the range 1 MHz to 100 MHz for 2.5GBASE-T, and 1 MHz to 250 MHz for 5GBASE-T

No spurious signals shall be emitted onto the MDI when the PHY is held in power-down mode (as defined in 22.2.4.1.5), when released from power-down mode, or when external power is first applied to the PHY.

126.8.2.2 MDI return loss

The differential impedance at the MDI for each transmit/receive channel shall be such that any reflection due to differential signals incident upon the MDI from a balanced cabling having a nominal differential characteristic impedance of 100 Ω is attenuated, relative to the incident signal as per the relationship shown in Equation (126–38):

$$\text{Return loss} \geq \begin{cases} 16 & 1 \leq f \leq 40 \quad \text{(dB)} \\ 16 - 10\log_{10}(f/40) & 40 < f \leq f_{\max} \quad \text{(dB)} \end{cases} \tag{126–38}$$

where

f is in MHz
$f_{\max}$ is 125 MHz for 2.5GBASE-T and 250 MHz for 5GBASE-T

126.8.2.3 MDI impedance balance

Impedance balance is a measure of the impedance-to-ground difference between the two MDI contacts used by a duplex link channel and is referred to as common-mode-to-differential-mode impedance balance. MDI impedance balance is specified beyond the Nyquist frequency of the PHY to account for system performance variation. When the transmitter is transmitting random or pseudo-random data, the common-mode-to-differential-mode impedance balance, *Bal*(*f*), of each channel of the MDI shall meet the relationship:

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For 2.5GBASE-T: (126–39)

$$Bal(f) \geq \begin{cases} 48 & 1 \leq f < 10 \quad \text{(dB)} \\ 48 - 20\log_{10}(f/10) & 10 \leq f < 20 \quad \text{(dB)} \\ 42 - 15\log_{10}(f/20) & 20 \leq f \leq 125 \quad \text{(dB)} \end{cases}$$

For 5GBASE-T:

$$Bal(f) \geq \begin{cases} 48 & 1 \leq f \leq 30 \quad \text{(dB)} \\ 44 - 19.2\log_{10}(f/50) & 30 < f \leq 250 \quad \text{(dB)} \end{cases}$$

where

f is the frequency in MHz

Test mode 5 may be used to generate an appropriate transmitter output.

The impedance balance is defined as the S parameter measurement of Sdc11 in dB at the MDI.

The impedance balance may be measured with a mixed mode four port network analyzer capable of measuring the common-mode voltage and differential mode voltage of a balanced port. Impedance balance is the S parameter measurement of Sdc11 in dB at the MDI where two ports of the four port network analyzer are connected between two MDI contacts used by a duplex link channel and these two ports are configured as a single balanced port. For this test the PHY ground is connected to the network analyzer ground. The other two ports of the network analyzer are unconnected. The network analyzer should be capable of measuring Sdc11 to at least –60 dB and should use a differential input impedance of 100 Ω and a common-mode impedance of 75 Ω.

During the test the PHY is connected to the MDI as in normal operation.

NOTE—The measurement may use narrow IF bandwidth settings and averaging to better distinguish between impedance balance and the transmitted test pattern.

126.8.2.4 MDI fault tolerance

Each wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to any other wire within the 4-pair cable for an indefinite period of time and shall resume normal operation after the short circuit(s) are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

A 2.5GBASE-T or 5GBASE-T PHY shall be able to sustain, without damage, connection to a PSE and shall not cause damage to the PSE as defined in 33.2.

Each wire pair shall withstand without damage a 1000 V common-mode impulse of either polarity. The shape of the impulse is 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060. See Figure 40–34 in 40.8.3.4.

126.9 Environmental specifications

126.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

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126.9.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cabling systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards should be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures should be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

126.9.3 Installation and maintenance guidelines

It is recommended that sound installation practice, including screen management, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable. In addition, Annex 55B provides additional cabling guidelines for 10GBASE-T deployment on balanced copper cabling systems, which may be helpful to 2.5G/5GBASE-T installations.

It is a mandatory requirement that, during installation of the cabling plant, care be taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

126.9.4 Telephone voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 2.5GBASE-T or 5GBASE-T. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the “battery” and ringing voltages. Although there is no universal standard, the following maximums generally apply:

a) Battery voltage to a telephone line is generally 56 V dc applied to the line through a balanced 400 Ω source impedance.
b) Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 V dc with a 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 2.5GBASE-T and 5GBASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not preclude conformance with 126.9.1 and 126.9.2.

126.9.5 Electromagnetic compatibility

A system integrating the 2.5GBASE-T or 5GBASE-T shall comply with applicable local and national codes for the limitation of electromagnetic interference.

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126.9.6 Temperature and humidity

A system integrating the 2.5GBASE-T or 5GBASE-T is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

126.10 PHY labeling

It is recommended that each PHY (or supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability and units thereof
b) Power level in terms of maximum current drain (for external PHYs)
c) Port type (i.e., 2.5GBASE-T or 5GBASE-T)
d) Any applicable safety warnings
e) EEE support
f) Fast retrain support

126.11 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of a 2.5GBASE-T PHY shall not exceed 12 800 BT. The sum of the transmit and receive data delays for an implementation of a 5GBASE-T PHY shall not exceed 14 336 BT. Transmit data delay is measured from the input of a given unit of data at the XGMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the XGMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link. Equation (80–1) specifies the calculation of delay per meter of electrical cable, which may be converted to bit times using 2.5 BT per ns for 2.5GBASE-T, and 5 BT per ns for 5GBASE-T (see Table 125–3).

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126.12 Protocol implementation conformance statement (PICS) proforma for Clause 126—Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, types 2.5GBASE-T and 5GBASE-T[218]

The supplier of a protocol implementation that is claimed to conform to this clause shall complete the protocol implementation conformance statement (PICS) proforma listed in the following subclauses.

Instructions for interpreting and filling out the PICS proforma may be found in Clause 21.

126.12.1 Identification

126.12.1.1 Implementation identification

Supplier	
Contact point for queries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

126.12.1.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 126, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, types 2.5GBASE-T and 5GBASE-T
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exceptions items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[218]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so it can be used for its intended purpose and may further publish the completed PICS.

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126.12.2 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
XGE	XGMII compatibility interface	46, 126.1.5	O	Yes [ ] No [ ]	Compatibility interface is supported
*EEE	Support of EEE capability		O	Yes [ ] No [ ]	126.1.3.3
*FR	Support of Fast Retrain capability		O	Yes [ ] No [ ]	126.4.2.5.16
*MD	MDIO capability	126.6	O	Yes [ ] No [ ]	Registers and interface supported
*INS	Installation / cable	126.7	O	Yes [ ] No [ ]	

126.12.3 Physical Coding Sublayer (PCS)

126.12.3.1 PCS Transmit functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCT1	PCS Transmit function state diagram	126.3.2.2	M	Yes [ ]	See Figure 126–14 and Figure 126–15
PCT2	PCS Transmit function state diagram with EEE states	126.3.2.2	EEE:M	Yes [ ] N/A [ ]	See Figure 126–14 and Figure 126–15
PCT3	SEND_Z Operation	126.3.2.2	M	Yes [ ]	PMA_TXMODE.indication message
PCT4	SEND_N Operation	126.3.2.2	M	Yes [ ]	PMA_TXMODE.indication message
PCT5	SEND_T Operation	126.3.2.2	M	Yes [ ]	PMA_TXMODE.indication message
PCT6	PCS Transmit bit ordering	126.3.2.2	M	Yes [ ]	See Figure 126–6
PCT7	Invalid control code handling	126.3.2.2.6	M	Yes [ ]	
PCT8	/I/ insertion and deletion	126.3.2.2.8	M	Yes [ ]	
PCT9	/LI/ insertion and deletion	126.3.2.2.9	EEE:M	Yes [ ] N/A [ ]	
PCT10	/O/ deletion	126.3.2.2.12	M	Yes [ ]	
PCT11	Scrambler as MASTER	126.3.2.2.15	M	Yes [ ]	Equation (126–1)
PCT12	Scrambler as SLAVE	126.3.2.2.15	M	Yes [ ]	Equation (126–2)
PCT13	LDPC encoding	126.3.2.2.16	M	Yes [ ]	Generator matrix is described in Annex 55A
PCT14	PAM16 mapping	126.3.2.2.18	M	Yes [ ]	
PCT15	EEE Transmit function state diagram	126.3.2.2.19	EEE:M	Yes [ ] N/A [ ]	See Figure 126–18

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Item	Feature	Subclause	Status	Support	Value/Comment
PCT16	LP_IDLE input to scrambler during LPI mode	126.3.2.2.19	EEE:M	Yes [ ] N/A [ ]	
PCT17	lpi_tx_mode control	126.3.2.2.19	EEE:M	Yes [ ] N/A [ ]	
PCT18	PCS test pattern mode	126.3.3	M	Yes [ ]	See Figure 126–6
PCT19	PMA training - MASTER scrambler	126.3.4	M	Yes [ ]	
PCT20	PMA training - SLAVE scrambler	126.3.4	M	Yes [ ]	
PCT21	PMA training scrambler initial state	126.3.4	M	Yes [ ]	In no case shall the scrambler state be initialized to all zeros
PCT22	LPI active pair and refresh_active signals	126.3.5.1	EEE:M	Yes [ ] N/A [ ]	
PCT23	Alert signaling in place of refresh signaling	126.3.5.3	EEE:M	Yes [ ] N/A [ ]	
PCT24	Slave synchronization	126.3.5.1	EEE:M	Yes [ ] N/A [ ]	
PCT25	Quiet launch power	126.3.5.2	EEE:M	Yes [ ] N/A [ ]	
PCT26	LPI sleep timer	126.3.6.2.3	EEE:M	Yes [ ] N/A [ ]	
PCT27	LPI alert timer	126.3.6.2.3	EEE:M	Yes [ ] N/A [ ]	
PCT28	LPI wake timer	126.3.6.2.3	EEE:M	Yes [ ] N/A [ ]	
PCT29	LPI rx wake timer	126.3.6.2.3	EEE:M	Yes [ ] N/A [ ]	
PCT30	LPI tx wake timer	126.3.6.2.3	EEE:M	Yes [ ] N/A [ ]	
PCT31	LPI scrambler	126.3.5.3	EEE:M	Yes [ ] N/A [ ]	The training sequence described in 126.3.5 shall be used
PCT32	Refresh using THP	126.3.5.3	EEE:M	Yes [ ] N/A [ ]	
PCT33	Reset THP at the start of refresh	126.3.5.3	EEE:M	Yes [ ] N/A [ ]	
PCT34	Master alert on pair A, other pairs silent	126.3.5.3	EEE:M	Yes [ ] N/A [ ]	
PCT35	Slave alert on pair C, other pairs silent	126.3.5.3	EEE:M	Yes [ ] N/A [ ]	

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Item	Feature	Subclause	Status	Support	Value/Comment
PCT36	Inactive pairs transmit zeros	126.3.5.3	EEE:M	Yes [ ] N/A [ ]	
PCT37	ENCODE function	126.3.6.2.4	M	Yes [ ]	Encode the block as specified in 126.3.2.2.2
PCT38	PCS loopback setup	126.3.7.3	M	Yes [ ]	

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126.12.3.2 PCS Receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR1	PCS Receive function state diagram	126.3.2.3	M	Yes [ ]	See Figure 126–16 and state variables as specified in 126.3.6.2
PCR2	PCS Receive bit ordering	126.3.2.3.1	M	Yes [ ]	See Figure 126–7
PCR3	Descrambling as MASTER	126.3.2.3.2	M	Yes [ ]	
PCR4	Descrambling as SLAVE	126.3.2.3.2	M	Yes [ ]	
PCR5	PMA training descrambler - MASTER	126.3.4.3	M	Yes [ ]	
PCR6	PMA training descrambler - SLAVE	126.3.4.3	M	Yes [ ]	
PCR7	DECODE operation	126.3.6.2.4	M	Yes [ ]	Decode the block as specified in 126.3.4
PCR8	LFER monitor	126.3.6.3	M	Yes [ ]	See state diagrams in Figure 126–13, Figure 126–14, and Figure 126–16

126.12.3.3 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	PCS Reset function	126.3.2.1	M	Yes [ ]	

126.12.4 Physical Medium Attachment (PMA)

Item	Feature	Subclause	Status	Support	Value/Comment
PMF1	PMA Reset function	126.4.2.1	M	Yes [ ]	
PMF2	PMA transmission	126.4.2.2	M	Yes [ ]	
PMF3	Transmitter clocking	126.4.2.2	M	Yes [ ]	All driven by TX_TCLK
PMF4	PMA Transmit mapping	126.4.2.2	M	Yes [ ]	Per mathematical description given in 126.4.3.1
PMF5	PMA Transmit electrical compliance	126.4.2.2	M	Yes [ ]	See PMA electrical specifications given in 126.5
PMF6	Clocking as MASTER	126.4.2.2	M	Yes [ ]	Source the transmit clock TX_TCLK from a local clock
PMF7	Clocking as SLAVE in loop timed mode	126.4.2.2	M	Yes [ ]	Source the transmit clock TX_TCLK from the recovered clock

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Item	Feature	Subclause	Status	Support	Value/Comment
PMF8	Transmit fault mapping	126.4.2.2	O	Yes [ ] No [ ]	Contribute to the transmit fault bit as specified in 45.2.1.7.4
PMF9	Generates alert signal	126.4.2.2	EEE:M	Yes [ ] N/A [ ]	Generates the alert signal defined in 126.4.2.2.1
PMF10	Generates link failure signaling	126.4.2.2	FR:M	Yes [ ] N/A [ ]	Generates the link failure signal defined in 126.4.2.2.2
PMF11	PMA Receive function performance	126.4.2.4	M	Yes [ ]	LDPC frame error ratio of less than 3.2×10^{-9}
PMF12	Receive fault mapping	126.4.2.4	O	Yes [ ] No [ ]	Contribute to the receive fault bit as specified in 45.2.1.7.5
PMF13	Implement alert_detect	126.4.2.4	EEE:M	Yes [ ] N/A [ ]	Generates alert_detect when the alert signal is detected at the receiver
PMF14	Detect link failure signaling	126.4.2.4	FR:M	Yes [ ] N/A [ ]	Sets link_fail_detect to true when the link failure signal is detected
PMF15	PHY Control function	126.4.2.5	M	Yes [ ]	See state diagram in Figure 126–26 and state diagrams in Figure 126–27 and Figure 126–28
PMF16	Infofield	126.4.2.5	M	Yes [ ]	All subclauses from 126.4.2.5.1 to 126.4.2.5.14
PMF17	THP initialization	126.4.2.5.15	M	Yes [ ]	Last 16 symbols of PMA_Coeff_Exch
PMF18	PBO exchange	126.4.2.5.15	M	Yes [ ]	
PMF19	Slave PBO setting	126.4.2.5.15	M	Yes [ ]	Slave's PBO final setting within two levels (4 dB) of the MASTER's PBO level
PMF20	THP coefficient exchange	126.4.2.5.15	M	Yes [ ]	
PMF21	Recommended startup sequence timing	126.4.2.5.15	O	Yes [ ] No [ ]	See Table 126–10
PMF22	Implements fast retrain state diagram	126.4.2.5.16	FR:M	Yes [ ] N/A [ ]	
PMF23	Behavior after fast retrain request	126.4.2.5.16	FR:M	Yes [ ] N/A [ ]	Transmit PAM2 within 18 LDPC frame periods following link failure request
PMF24	Behavior after fast retrain signal detection	126.4.2.5.16	FR:M	Yes [ ] N/A [ ]	Transmit PAM2 within 18 LDPC frame periods following link failure signal detection
PMF25	Link Monitor	126.4.2.6	M	Yes [ ]	See state diagram in Figure 126–29
PMF26	Refresh monitor state diagram	126.4.2.7	EEE:M	Yes [ ] N/A [ ]	Implements state diagram of Figure 126–17
PMF27	Recommended fast retrain sequence timing	126.4.2.5.16	FR:O	Yes [ ] No [ ] N/A [ ]	See Table 126–11

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Item	Feature	Subclause	Status	Support	Value/Comment
PMF28	Clock Recovery function	126.4.2.8	M	Yes [ ]	
PMF29	MDIX for EEE refreshes and alert	126.4.4	EEE:M	Yes [ ] N/A [ ]	
PMF30	Symbol response	126.4.3.1	M	Yes [ ]	Per electrical specifications given in 126.5
PMF31	THP filter coefficient setting	126.4.3.1	M	Yes [ ]	Fixed after startup
PMF32	PMA Transmit power backoff settings	126.4.3.1	M	Yes [ ]	
PMF33	Minimum power backoff requested	126.4.3.1	M	Yes [ ]	Per Table 126–12
PMF34	Automatic configuration	126.4.4	M	Yes [ ]	Comply with the specifications of 40.4.4.1and 40.4.4.2
PMF35	Pair/Polarity swap detection and correction	126.4.4	M	Yes [ ]	
PMF36	PMA_config.indication generation	126.4.5.1	M	Yes [ ]	
PMF37	Maxwait_timer expiration	126.4.5.2	M	Yes [ ]	
PMF38	Minwait_timer expiration	126.4.5.2	M	Yes [ ]	

126.12.5 PMA Electrical Specifications

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	Electrical isolation	126.5.1	M	Yes [ ]	Conforms to J.1
PME2	Insulation breakdown after test	126.5.1	M	Yes [ ]	Conforms to J.1
PME3	Test modes supported	126.5.2	M	Yes [ ]	
PME4	Test mode enablement	126.5.2	M	Yes [ ]	Per management register settings shown in Table 126–13
PME5	The test modes only change the data symbols	126.5.2	M	Yes [ ]	
PME6	Provide a means to enable the test modes	126.5.2	!MD:M	Yes [ ] N/A [ ]	
PME7	Test mode 1 operation	126.5.2	M	Yes [ ]	
PME8	Test mode 2 operation	126.5.2	M	Yes [ ]	
PME9	Test mode 3 operation, pair D	126.5.2	M	Yes [ ]	
PME10	Test mode 3 operation, pairs A, B, and C	126.5.2	M	Yes [ ]	Transmit silence
PME11	Test mode 4 waveform	126.5.2	M	Yes [ ]	Tones per Table 126–14
PME12	Test mode 4 levels	126.5.2	M	Yes [ ]	

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Item	Feature	Subclause	Status	Support	Value/Comment
PME13	Test mode 5 operation	126.5.2	M	Yes [ ]	
PME14	Test mode 6 operation	126.5.2	M	Yes [ ]	
PME15	Test mode 7 operation	126.5.2	M	Yes [ ]	
PME16	Text fixture 3 isolation	126.5.2	M	Yes [ ]	>30 dB between signals on any of {pairs A, B, C} and pair D
PME17	Transmitter nominal load	126.5.3	M	Yes [ ]	
PME18	AC-coupling to the MDI	126.5.3	M	Yes [ ]	
PME19	Droop test	126.5.3.1	M	Yes [ ]	
PME20	SFDR of transmitter	126.5.3.2	M	Yes [ ]	
PME21	Transmitter jitter	126.5.3.3	M	Yes [ ]	
PME22	Transmit power level	126.5.3.4	M	Yes [ ]	
PME23	Transmitter PSD	126.5.3.4	M	Yes [ ]	
PME24	MASTER symbol rate	126.5.3.5	M	Yes [ ]	
PME25	Maximum short term rate of frequency variation during LPI	126.5.3.5	EEE:M	Yes [ ] N/A [ ]	Less than 0.1 ppm/s
PME26	Maximum short term rate of frequency variation when switching to and from LPI	126.5.3.5	EEE:M	Yes [ ] N/A [ ]	Less than 0.1 ppm/s
PME27	BER over a 126.7 compliant link	126.5.4.1	M	Yes [ ]	
PME28	Receiver frequency tolerance	126.5.4.2	M	Yes [ ]	
PME29	Alien noise tolerance	126.5.4.4	M	Yes [ ]	

126.12.6 PMA Management Interface

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	Support for Auto-Negotiation	126.6.1	M	Yes [ ]	See Clause 28
MF2	MASTER and SLAVE operation	126.6.1	M	Yes [ ]	Capable of operating either as MASTER or SLAVE
MF3	Extended Next Page support	126.6.1	M	Yes [ ]	
MF4	Optimized FLP timing	126.6.1	M	Yes [ ]	
MF5	Management registers	126.6.1.1	M	Yes [ ]	As defined in Table 126–15
MF6	2.5G/5GBASE-T Extended Next Page bit assignments	126.6.1.2	M	Yes [ ]	As defined in Table 126–16
MF7	EEE advertisement	126.6.1.2	EEE:M	Yes [ ] N/A [ ]	As defined in Table 126–16
MF8	Fast retrain ability advertisement	126.6.1.2	FR:M	Yes [ ] N/A [ ]	As defined in Table 126–16

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Item	Feature	Subclause	Status	Support	Value/Comment
MF9	Resolution completion	126.6.2	M	Yes [ ]	Successful completion of resolution treated as MASTER-SLAVE configuration resolution complete
MF10	Seed counter	126.6.2	M	Yes [ ]	Counter provided to track number of seed attempts
MF11	Counter set to zero at startup	126.6.2	M	Yes [ ]	
MF12	Counter increment	126.6.2	M	Yes [ ]	
MF13	Counter reset	126.6.2	M	Yes [ ]	After resolution is complete
MF14	Bit 7.33.15 set to zero after resolution is complete	126.6.2	M	Yes [ ]	After resolution is complete
MF15	Resolution fault declared	126.6.2	M	Yes [ ]	After generation of seven seeds
MF16	MASTER-SLAVE fault condition	126.6.2	M	Yes [ ]	Condition occurs when both devices manually select MASTER or SLAVE
MF17	MASTER-SLAVE fault condition bit	126.6.2	M	Yes [ ]	Set to one upon fault condition
MF18	MASTER-SLAVE fault resolution	126.6.2	M	Yes [ ]	Fault condition treated as MASTER-SLAVE resolution complete
MF19	MASTER-SLAVE fault condition indication	126.6.2	M	Yes [ ]	link_status_2p5GigT (2.5GBASE-T) or link_status_5GigT (5GBASE-T) set to FAIL

126.12.7 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	MDI compatibility	126.7	INS:M	Yes [ ] N/A [ ]	
LKS2	Insertion loss of each duplex channel	126.7.2.1	INS:M	Yes [ ] N/A [ ]	See Equation (126–11)
LKS3	Return loss	126.7.2.3	INS:M	Yes [ ] N/A [ ]	See Equation (126–12)
LKS4	NEXT loss within pairs in a link segment	126.7.2.4.1	INS:M	Yes [ ] N/A [ ]	See Equation (126–13), Equation (126–14)
LKS5	Power sum NEXT loss	126.7.2.4.2	INS:M	Yes [ ] N/A [ ]	See Equation (126–15), Equation (126–16)
LKS6	Worst pair ACRF loss	126.7.2.4.4	INS:M	Yes [ ] N/A [ ]	See Equation (126–20), Equation (126–19)
LKS7	Power sum ACRF loss	126.7.2.4.5	INS:M	Yes [ ] N/A [ ]	See Equation (126–21)

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Item	Feature	Subclause	Status	Support	Value/Comment
LKS8	Propagation delay	126.7.2.5	INS:M	Yes [ ] N/A [ ]	
LKS9	Delay skew	126.7.2.6	INS:M	Yes [ ] N/A [ ]	
LKS10	Delay skew change	126.7.2.6	INS:M	Yes [ ] N/A [ ]	
LKS11	Power sum ANEXT loss	126.7.3.1	INS:M	Yes [ ] N/A [ ]	$ALSNR_{\text{criteria}} > 0$
LKS12	PS AACRF loss	126.7.3.1	INS:M	Yes [ ] N/A [ ]	$ALSNR_{\text{criteria}} > 0$

126.12.8 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	126.8.1	M	Yes [ ]	Eight-pin connectors meeting the requirements of IEC 60603-7-4 (unscreened) or IEC 60603-7-5 (screened)
MDI2	Cabling connector	126.8.1	INS:M	Yes [ ] N/A [ ]	Plug
MDI3	PHY connector	126.8.1	M	Yes [ ]	Jack (as opposed to plug)
MDI4	MDI connector jack plus plug performance	126.8.2	INS:M	Yes [ ] N/A [ ]	
MDI5	Mated MDI connector FEXT loss	126.8.2	INS:M	Yes [ ] N/A [ ]	Per Equation (126–37)
MDI6	MDI power down	126.8.2	M	Yes [ ]	
MDI7	MDI return loss	126.8.2.2	M	Yes [ ]	
MDI8	MDI impedance balance	126.8.2.3	M	Yes [ ]	
MDI9	MDI fault tolerance to short circuits	126.8.2.4	M	Yes [ ]	No damage with an indefinite short
MDI10	Recovery from short	126.8.2.4	M	Yes [ ]	
MDI11	Short circuit current	126.8.2.4	M	Yes [ ]	Less than 300 mA
MDI12	Connection to PSE	126.8.2.4	M	Yes [ ]	No damage to PHY
MDI13	Connection to PSE	126.8.2.4	M	Yes [ ]	No damage to PSE
MDI14	Common-mode impulse tolerance	126.8.2.4	M	Yes [ ]	1000 V common-mode impulse of either polarity

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126.12.9 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ENV1	Conformance to safety specifications	126.9.1	M	Yes [ ]	Conforms to J.2
ENV2	Installation isolation integrity	126.9.3	INS:M	Yes [ ] N/A [ ]	No electrical contact with unintended conductors or ground
ENV3	Phone voltage immunity	126.9.4	M	Yes [ ]	See ENV1 after exposure to telephone voltages
ENV4	Electromagnetic compatibility	126.9.5	INS:M	Yes [ ] N/A [ ]	With local and national codes

126.12.10 Timing requirements

Item	Feature	Subclause	Status	Support	Value/Comment
TR1	Delay	126.11	M	Yes [ ]	

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127. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer for 2.5 Gb/s 8B/10B 2.5GBASE-X

127.1 Overview

127.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer that are common to a family of 2.5 Gb/s Physical Layer implementations known as 2.5GBASE-X. The 2.5GBASE-X PCS and 2.5GBASE-X PMA are sublayers of the 2.5 Gb/s BASE-X PHY listed in Table 125–1. The term 2.5GBASE-X is used when referring generally to Physical Layers using the PCS and PMA defined in this clause.

2.5GBASE-X PCS and PMA sublayers map the interface characteristics of the PMD sublayer (including MDI) to the services expected by the Reconciliation sublayer. 2.5GBASE-X can be extended to support any other full duplex medium requiring only that the medium be compliant at the PMD level.

127.1.2 Relationship of 2.5GBASE-X to other standards

Figure 125–1 depicts the relationships among the 2.5GBASE-X sublayers, Ethernet MAC and reconciliation layers, and the higher layers. The 2.5GBASE-X service interface is the XGMII, which is defined in Clause 46.

127.1.3 Summary of 2.5GBASE-X sublayers

Figure 127–1 shows the relationship of the 2.5GBASE-X PCS sublayer with other sublayers to the ISO Open System Interconnection (OSI) reference model.

127.1.3.1 Physical Coding Sublayer (PCS)

The PCS service interface is the XGMII that provides a uniform interface to the Reconciliation sublayer for all 2.5 Gb/s PHY implementations. The 2.5GBASE-X PCS provides all services required by the XGMII including encoding (decoding) of XGMII data octets to (from) ten-bit code-groups (8B/10B) for communication with the underlying PMA.

127.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS to support the use of serial-bit-oriented physical media. The 2.5GBASE-X PMA performs the following functions:

a) Mapping of transmit and receive code-groups between the PCS and PMA via the PMA Service Interface.
b) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMD.
c) Recovery of clock from the 8B/10B-coded data supplied by the PMD.
d) Mapping of transmit and receive bits between the PMA and PMD via the PMD Service Interface.

127.1.3.3 Physical Medium Attachment (PMA) service interface rates

2.5GBASE-X Physical Layer specification has nominal rate at the PMA service interface of 3.125 Gb/s, which provides MAC data rate of 2.5 Gb/s.

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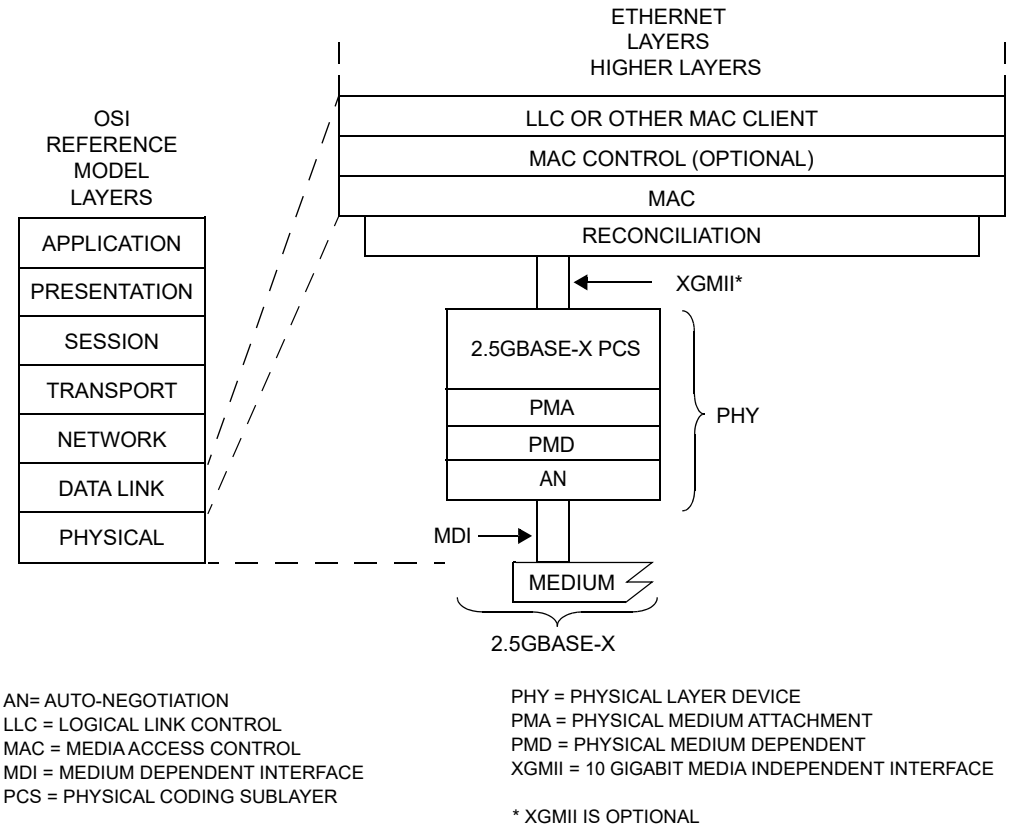

Figure 127–1—2.5GBASE-X PCS and PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

127.1.4 Inter-sublayer interfaces

There are a number of interfaces employed by 2.5GBASE-X. Some (such as the PMA Service Interface) use an abstract service model to define the operation of the interface. An optional physical instantiation of the PCS Interface is the XGMII. Figure 127–2 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 2.5GBASE-X.

While this specification defines interfaces in terms of bits, octets, and code-groups, implementers may choose other data path widths for implementation convenience. The only exception is the XGMII, which, when implemented at an observable interconnection port, uses a 32-bit-wide data path as specified in Clause 46.

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127.1.5 Functional block diagram

Figure 127–2 provides a functional block diagram of the 2.5GBASE-X PHY.

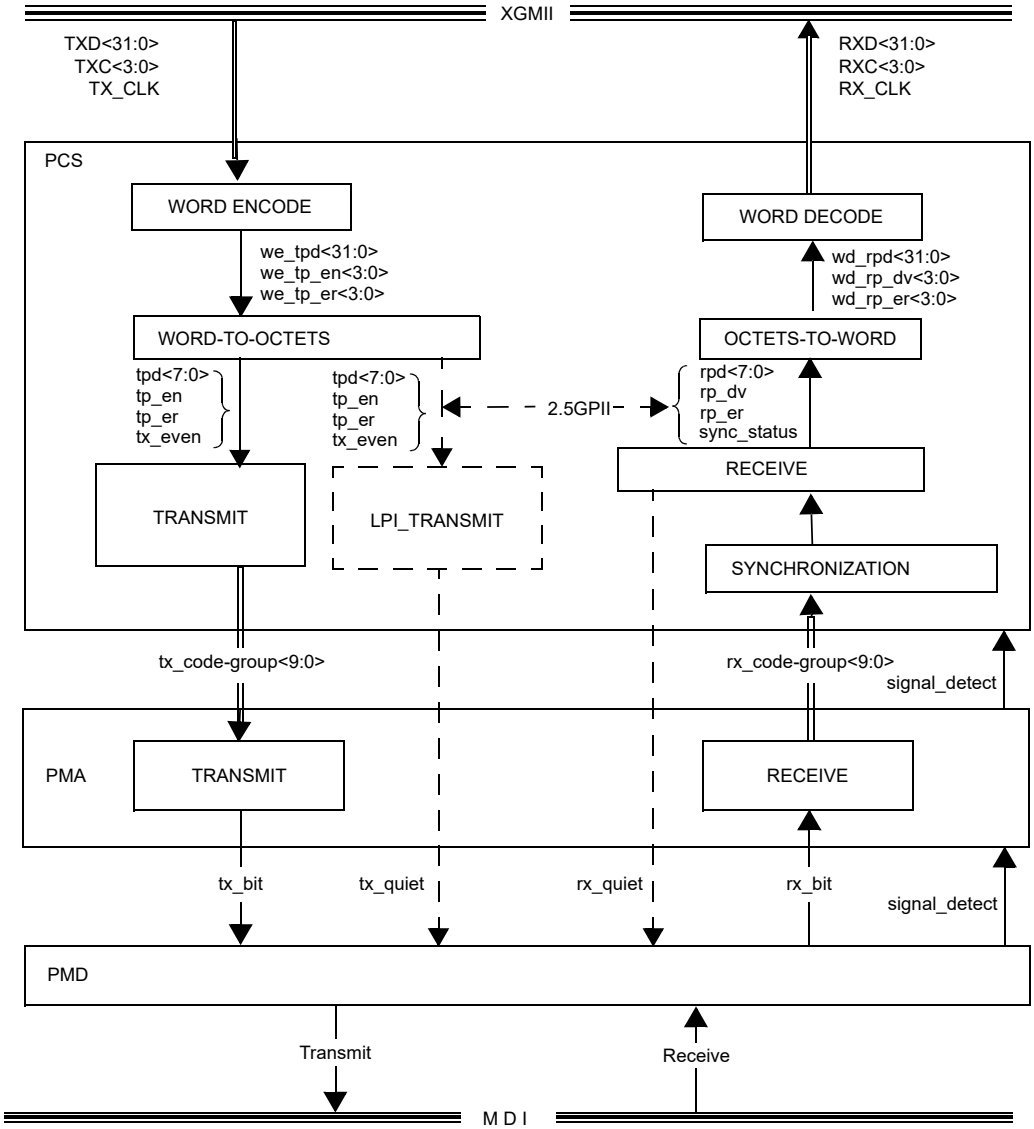

Figure 127–2—Functional block diagram of 2.5GBASE-X PHY

127.2 Physical Coding Sublayer (PCS)

127.2.1 PCS Interface (XGMII)

The PCS Service Interface allows the 2.5GBASE-X PCS to transfer information to and from a PCS client. PCS clients include the MAC (via the Reconciliation sublayer). The PCS Interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

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127.2.2 Functions within the PCS

The PCS includes the Word Encode, Word-to-Octets, Transmit, Synchronization, Receive, Octets-to-Word, and Word Decode processes for 2.5GBASE-X. The PCS shields the RS (and MAC) from the specific nature of the underlying channel.

When communicating with the XGMII, the PCS uses, in each direction, 32 data signals (TXD <31:0> and RXD <31:0>), four control signals (TXC <3:0> and RXC <3:0>), and a clock (TX_CLK and RX_CLK).

When communicating with the PMA, the PCS uses a ten-bit-wide synchronous data path, tx_code-group<9:0> and rx_code-group<9:0>, which conveys ten-bit code-groups. At the PMA Service Interface, code-group alignment and MAC packet delimiting are made possible by embedding special non-data code-groups in the transmitted code-group stream. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

The Word Encode process continuously generates four 2.5GPII symbols (we_tpd<31:0>) and associated four bits of transmit enable (we_tp_en<3:0>) and four bits of transmit error (we_tp_er<3:0>) based upon the TXD <31:0> and TXC <3:0> signals on the XGMII, sending them to the Word-to-Octets process.

The Word-to-Octets process takes the four 2.5GPII symbols, and associated transmit enable and transmit error, and transmits one 2.5GPII symbol (tpd<7:0>) and its associated transmit enable (tp_en) and transmit error (tp_er) at a time to the PCS Transmit Process.

The Word-to-Octets process takes the output of the Word Encoder and presents one symbol at a time (tp_en, tp_er, tpd<7:0>) to the PCS transmit process. we_tpd<7:0> is presented first and we_tpd<31:24> is presented last.

The PCS Synchronization process continuously accepts code-groups via the PMA_UNITDATA.indication primitive and conveys received code-groups to the PCS Receive process via the SYNC_UNITDATA.indication primitive. The PCS Synchronization process sets the sync_status flag to indicate whether the PMA is functioning dependably.

The PCS Receive process continuously accepts code-groups via the SYNC_UNITDATA.indication primitive. The PCS Receive process monitors these code-groups and generates rpd<7:0>, rp_dv, and rp_er on the 2.5GPII.

The Octets-to-Word process queues the received 2.5GPII symbols and aligns them in groups of four 2.5GPII symbols. Symbols may be deleted or idle symbols added in order to do the alignment.

The Word Decode process continuously accepts the four 2.5GPII symbols from the Octets-to-Word process and generates RXD <31:0> and RXC <3:0> on the XGMII.

All PCS processes are described in detail in the state diagrams in 127.2.7.2.

127.2.3 PCS used with 2.5GBASE-KX PMD

The following requirements apply to a PCS used with a 2.5GBASE-KX PMD. Support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when code_sync_status=FAIL and the value OK when code_sync_status =OK. The primitive shall be generated when the value of link_status changes.

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127.2.4 Use of code-groups

The transmission code used by the PCS, referred to as 8B/10B, is identical to that specified in Clause 36. The PCS maps XGMII characters into an intermediate 2.5GPII which is then mapped to 10-bit code-groups, and vice versa, using the 8B/10B block coding scheme. Implicit in the definition of a code-group is an establishment of code-group boundaries by a PCS Synchronization process. The 8B/10B transmission code as well as the rules by which the PCS ENCODE and DECODE functions generate, manipulate, and interpret code-groups are specified in 127.2.6. The XGMII to 2.5GPII mapping and vice versa are specified in 127.2.5. Code-groups and the 2.5GPII are unobservable and have no meaning outside the PCS.

127.2.5 XGMII to 2.5GPII mapping

The Word Encode, Word-to-Octets, Octets-to-Word, and Word Decode processes together define the XGMII to 2.5GPII mapping. This mapping function formats and serializes/deserializes the data between the four XGMII lanes and the single lane of the PCS transmit/receive process.

127.2.5.1 2.5 Gb/s PCS Internal Interface (2.5GPII)

The 2.5 Gb/s PCS Internal Interface (2.5GPII) is a logical interface that is internal to the 2.5GBASE-X PCS and exists solely for the purposes of defining the 2.5GBASE-X PCS functionality. Physical implementation of the 2.5GPII is optional and is not exposed outside of the PCS.

A 2.5GPII symbol is defined to be a set of tp_en, tp_er, tpd<7:0> variables on the transmit path, and rp_dv, rp_er, rpd<7:0> variables on the receive path. The permissible encodings are shown in Table 127–1 and Table 127–2. The Word Encode and Word Decode processes maps between the four XGMII lanes to four 2.5GPII symbols. The 2.5GPII symbols are indexed as we_tp_en<3:0>, we_tp_er<3:0>, we_tpd<31:0>, wd_rp_dv<3:0>, wd_rp_er<3:0>, and wd_rpd<31:0>. The nominal rate of operation is 78.125 Msymbols/s ± 100 ppm.

The Word-to-Octets and Octets-to-Word processes serializes/de-serializes four 2.5GPII symbols, and their associated enable and error bits, to/from four consecutive single 2.5GPII symbols. The nominal rate of operation of 2.5GPII symbols is 312.5 Msymbols/s ± 100 ppm.

Table 127–1—Permissible encodings of tpd<7:0>, tp_en, tp_er at 2.5GPII

tp_en	tp_er	tpd<7:0>	Description	Mnemonic
0	0	0x00 to 0xFF	Normal Inter-frame	Idle
0	1	0x00	Reserved	
0	1	0x01	Assert LPI	LPI
0	1	0x02 to 0x9B	Reserved	
0	1	0x9C	Sequence	Seq
0	1	0x9D to 0xFF	Reserved	
1	0	0x00 to 0xFF	Data	Data X
1	1	0x00 to 0xFF	Transmit Error	Err

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Table 127–2—Permissible encodings of rpd<7:0>, rp_dv, rp_er at 2.5GPII

rp_dv	rp_er	rpd<7:0>	Description	Mnemonic
0	0	0x00 to 0xFF	Normal Inter-frame	Idle
0	1	0x00	Reserved	
0	1	0x01	Assert LPI	LPI
0	1	0x02 to 0x0D	Reserved	
0	1	0x0E	False carrier indication	FCI
0	1	0x0F	Carrier Extend (odd byte packets)	CE
0	1	0x10 to 0x9B	Reserved	
0	1	0x9C	Sequence	Seq
0	1	0x9D to 0xFF	Reserved	
1	0	0x00 to 0xFF	Data	Data X
1	1	0x00 to 0xFF	Receive Error	Err

127.2.5.2 Word Encode

The Word Encode process maps the four XGMII lanes (see Table 46–2) onto four 2.5GPII symbols, and their associated transmit enable and transmit error bits, as shown in Table 127–3. The XGMII encoding is specified in Table 46–3. The 2.5GPII encoding is specified in Table 127–1. The mapping of the sequence ordered set is dependent on the current state of the wencode_state variable as shown in column 5. The state of wencode_state is updated once the mapping occurs per the last column.

A sequence ordered set ||Q|| appears to the PMA as /K28.5/W/K28.5/W/K28.5/W/K28.5/W/. On the 2.5GPII this appears as Seq, Data S0, Seq, Data S1, Seq, Data S2, Seq, Data S3. The same sequence ordered set is assumed to be repeating over multiple XGMII cycles. Every alternating consecutive sequence ordered set on the XGMII is ignored. If a sequence ordered set occurs over odd number of cycles on the XGMII, then the final one will be truncated as Seq, Data S0, Seq, Data S1 and Seq, Data S2, Seq, Data S3 are not sent.

The 24-bit Data X, Data Y, and Data Z from the sequence ordered set is mapped to Data S0, Data S1, Data S2, Data S3 as shown in Equation (127-1).

S0<7> = S3<7> = 0, S1<7> = S2<7> = 1
S0<5:0> = Data X<5:0>
S1<5:0> = Data Y<3:0>, Data X<7:6>
S2<5:0> = Data Z<1:0>, Data Y<7:4>
S3<5:0> = Data Z<7:2>
Sn<6> = Sn<7> if Sn<2> = 0
Sn<6> = Sn<5> if Sn<2> = 1 (127-1)

The signal ordered set |Fsig| uses the same equation except S2<7> is set to 0.

Since sequence ordered set can be sent back to back it is necessary to determine the boundaries of the ordered set. {S0<7>, S1<7>, S2<7>, S3<7>} can be used to determine the boundary. {S0<7>, S1<7>} will always be 01, while the 01 combination will never occur over {S1<7>, S2<7>}, {S2<7>, S3<7>}, or {S3<7>, S0<7>}.

Only 128 combinations of Sn<7:0> are possible. When encoded to their 10-bit equivalent, these 128 code-groups are defined to be in the set of /W/ (see 127.2.7.1.2).

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Table 127–3—Word Encode mapping

XGMII				wencode _state (n)		2.5GPII				wencode _state (n+1)
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**			**wd_tpd<7:0> we_tp_en<0> we_tp_er<0>**	**wd_tpd<15:8> we_tp_en<1> we_tp_er<1>**	**wd_tpd<23:16> we_tp_en<2> we_tp_er<2>**	**wd_tpd<31:24> we_tp_en<3> we_tp_er<3>**	
Data A or Err	Data B or Err	Data C or Err	Data D or Err	Don't care	=>	Data A or Err	Data B or Err	Data C or Err	Data D or Err	DATA
Idle	Idle	Idle	Idle	Don't care	=>	Idle	Idle	Idle	Idle	IDLE
LPI	LPI	LPI	LPI	Don't care	=>	LPI	LPI	LPI	LPI	DATA
Start	Data A or Err	Data B or Err	Data C or Err	Don't care	=>	Data 0x55	Data A or Err	Data B or Err	Data C or Err	DATA
Terminate	Idle	Idle	Idle	Don't care	=>	Idle	Idle	Idle	Idle	IDLE
Data A or Err	Terminate	Idle	Idle	Don't care	=>	Data A or Err	Idle	Idle	Idle	DATA
Data A or Err	Data B or Err	Terminate	Idle	Don't care	=>	Data A or Err	Data B or Err	Idle	Idle	DATA
Data A or Err	Data B or Err	Data C or Err	Terminate	Don't care	=>	Data A or Err	Data B or Err	Data C or Err	Idle	DATA
Sequence	Data X	Data Y	Data Z	IDLE	=>	Seq	Data S0	Seq	Data S1	SEQ
Sequence	Data X	Data Y	Data Z	SEQ	=>	Seq	Previous Data S2 [a]	Seq	Previous Data S3 [a]	IDLE
Sequence	Data X	Data Y	Data Z	DATA	=>	Idle	Idle	Idle	Idle	IDLE
else				Don't care	=>	Err	Err	Err	Err	DATA

[a] Previous Data S2 and Previous Data S3 are the values of S2 and S3 respectively as calculated by Equation (127-1) during the previous mapping.

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127.2.5.3 Word-to-Octets

The Word-to-Octets process takes the output of the Word Encoder and presents one symbol at a time (tp_en, tp_er, tpd<7:0>) to the PCS transmit process. we_tpd<7:0> is presented first and we_tpd<31:24> is presented last.

The Word-to-Octets process shall be synchronized to the PCS transmit process such that the we_tpd<7:0>and we_tpd<23:16> symbols are presented to the PCS transmit process which will result in the corresponding ordered set to be output to the PMA when the variable tx_even is TRUE and we_tpd<15:8>and we_tpd<31:24> variables when tx_even is FALSE.

127.2.5.4 Octets-to-Word

The Octets-to-Word process de-serializes the output of the PCS receive process to four symbols (wd_rp_dv<3:0>, wd_rp_er<3:0>, wd_rpd<31:0>). wd_rpd<7:0> is the earliest to arrive and wd_rpd<31:24> is the last.

The Octets-to-Word process inserts idle symbols or deletes symbols from the sequence of rpd<7:0> symbols received to achieve the following conditions:

a) A transition of a 2.5GPII idle symbol to a data or error symbol shall place the data or error symbol on wd_rpd<7:0>.
b) A transition of a 2.5GPII idle symbol to a LPI symbol shall place the LPI symbol on either wd_rpd<7:0> or wd_rpd<23:16>.
c) A transition of a 2.5GPII LPI symbol to an idle symbol shall place the idle symbol on either wd_rpd<7:0> or wd_rpd<23:16>.
d) The start of ||Q|| or ||Fsig|| set shall always occur on wd_rpd<7:0>. 127.2.5.2 describes how the start of |Q| and |Fsig| can be determined.

The Octets-to-Word process maintains a Deficit Idle Count (DIC) that represent the cumulative count of idle symbols in rpd<7:0> added or deleted from the sequence of received symbols. The DIC is incremented by one for each idle symbol deleted and decremented by one for each idle symbol added. The DIC shall be bounded to a minimum of 0 and a maximum of 3.

Note that in a properly behaved system, deletion of idle symbols from rpd<7:0> onto wd_rpd<31:0> should only occur at most once at the beginning of link, and afterwards no further insertions or deletions are required. In order to interoperate with the application described in Annex 127A, additional symbol insertions and deletions may be required during normal operation.

The only symbol that may be inserted is a idle symbol. However any symbol may be deleted. Usually this will either be idle or LPI symbols, though in pathological error conditions (e.g., unterminated packet followed immediately with sequence ordered set) some other symbol may be deleted.

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127.2.5.5 Word Decode

The Word Decode process maps the four 2.5GPII symbols onto the four XGMII lanes (see Table 46–2) as shown in Table 127–4. The XGMII encoding is specified in Table 46–4. The seq_s2_s3 variable indicates whether the next four 2.5GPII symbols are of the form Sequence, Data, Sequence, Data. The 2.5GPII encoding is specified in Table 127–2. The mapping is dependent on the current state of the wdecode_state and next_seq_s2_s3 variables as shown in columns 5 and 6. The state of wdecode_state is updated once the mapping occurs per the last column.

The 24-bit Data X, Data Y, and Data Z from the sequence ordered is reconstructed from Data S0, Data S1, Data S2, Data S3 according to Equation (127-2).

$$\begin{aligned} &\text{Data X<7:0> = S1<1:0>, S0<5:0>} \\ &\text{Data Y<7:0> = S2<3:0>, S1<5:2>} \\ &\text{Data Z<7:0> = S3<5:0>, S2<5:4>} \end{aligned} \tag{127-2}$$

127.2.6 8B/10B transmission code

The transmission code used by the PCS, referred to as 8B/10B, is identical to that specified in Clause 36. In addition to the requirements in this clause, a 2.5GBASE-X PCS shall also meet the 8B/10B transmission code requirements specified in 36.2.4.1 through 36.2.4.6, 36.2.4.8, and 36.2.4.9. The relationship of code-group bit positions to PMA and other PCS constructs is illustrated in Figure 127–3.

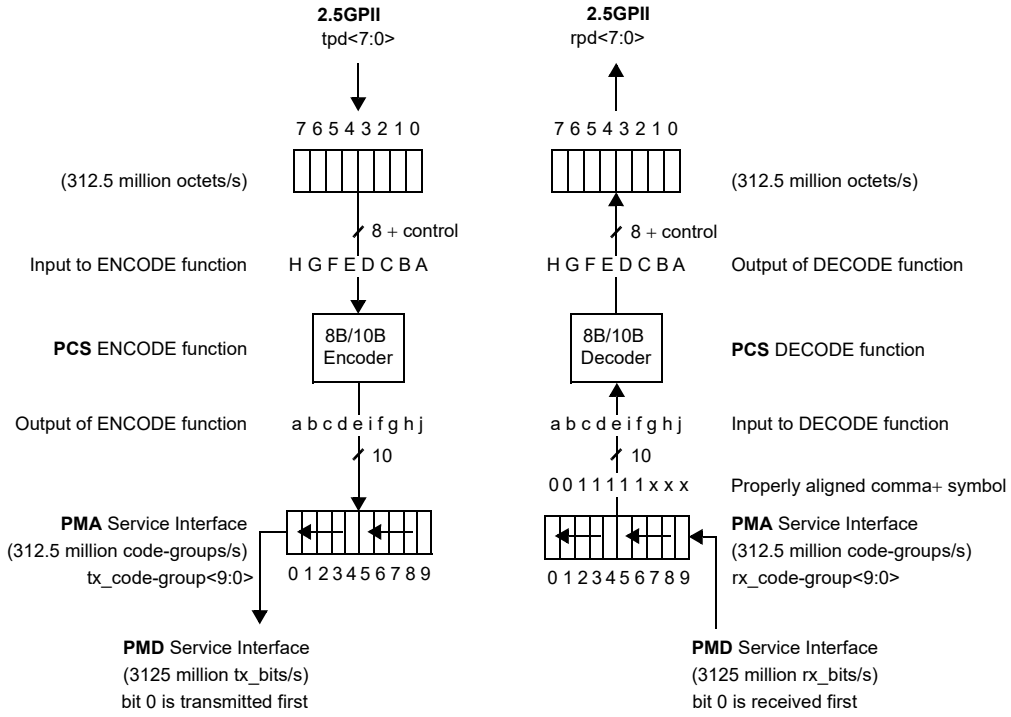

Figure 127–3—PCS 8B/10B reference diagram

127.2.6.1 Notation conventions

The 8B/10B transmission code uses letter notation for describing the bits of an unencoded information octet and a single control variable according to 36.2.4.1.

127.2.6.2 Transmission order

Code-group bit transmission order is illustrated in Figure 127–3 and defined in 36.2.4.2.

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Table 127–4—Word Decode mapping

2.5GPII				wdecode_state (n)	next_seq_s2_s3 [a]		XGMII				wdecode_state (n+1)
wd_rpd<7:0> we_rp_en<0> we_rp_er<0>	wd_rpd<15:8> we_rp_en<1> we_rp_er<1>	wd_rpd<23:16> we_rp_en<2> we_rp_er<2>	wd_rpd<31:24> we_rp_en<3> we_rp_er<3>				Lane 0	Lane 1	Lane 2	Lane 3	
Data A or Err	Data B or Err	Data C or Err	Data D or Err	≠IDLE	Don't care	=>	Data A or Err	Data B or Err	Data C or Err	Data D or Err	DATA
Data	Data A or Err	Data B or Err	Data C or Err	IDLE	Don't care	=>	SOP	Data A or Err	Data B or Err	Data C or Err	DATA
Idle	Idle	Idle	Idle	≠ DATA	Don't care	=>	Idle	Idle	Idle	Idle	IDLE
Idle	Idle	Idle	Idle	DATA	Don't care	=>	Terminate	Idle	Idle	Idle	IDLE
Data A or Err	Idle or CE	Idle	Idle	DATA	Don't care	=>	Data A or Err	Terminate	Idle	Idle	IDLE
Data A or Err	Data B or Err	Idle	Idle	DATA	Don't care	=>	Data A or Err	Data B or Err	Terminate	Idle	IDLE
Data A or Err	Data B or Err	Data C or Err	Idle or CE	DATA	Don't care	=>	Data A or Err	Data B or Err	Data C or Err	Terminate	IDLE
LPI	LPI	LPI	LPI	≠ DATA	Don't care	=>	LPI	LPI	LPI	LPI	IDLE
Idle	Idle	LPI	LPI	Don't care	Don't care	=>	LPI	LPI	LPI	LPI	IDLE
LPI	LPI	Idle	Idle	≠ DATA	Don't care	=>	Idle	Idle	Idle	Idle	IDLE
Seq	Data S0	Seq	Data S1	≠ DATA	TRUE	=>	Sequence	Data X	Data Y	Data Z	SEQ
Seq	Data S0	Seq	Data S1	≠ DATA	FALSE	=>	Idle	Idle	Idle	Idle	IDLE
Seq	Data S2	Seq	Data S3	SEQ	Don't care	=>	Sequence	Data X	Data Y	Data Z	IDLE
else				Don’t care		=>	Err	Err	Err	Err	ERR

[a] next_seq_s2_s3 is TRUE when the next four GPII octets represent the S2 and S3 sequence ordered set and FALSE otherwise.

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127.2.6.3 Generating code-groups and checking the validity of received code

Valid code-groups are defined in 36.2.4.3.

The running disparity rules are defined in 36.2.4.4.

The code-group generation is defined in 36.2.4.5.

The check on the validity of received code-groups is defined in 36.2.4.6.

127.2.6.4 Ordered sets

Table 127–5 lists the defined ordered sets, consisting of a single special code-group or combinations of special and data code-groups. Ordered sets which include /K28.5/ provide the ability to obtain bit and code-group synchronization and establish ordered set alignment (see 36.2.4.9 and 127.3.2.4). Ordered sets provide for the delineation of a packet and synchronization between the transmitter and receiver circuits at opposite ends of a link. Certain PHYs include an option (see 78.3) to transmit or receive /LI/, /LI1/ and /LI2/ to support Energy-Efficient Ethernet (see Clause 78).

Table 127–5—Defined ordered sets

Code	Ordered Set	Number of Code-Groups	Encoding
/I/	**IDLE**		Correcting /I1/, Preserving /I2/
/I1/	IDLE 1	2	/K28.5/D5.6/
/I2/	IDLE 2	2	/K28.5/D16.2/
	Encapsulation		
/R/	Carrier_Extend	1	/K23.7/
/S/	Start_of_Packet	1	/K27.7/
/T/	End_of_Packet	1	/K29.7/
/V/	Error_Propagation	1	/K30.7/
/LI/	**LPI**		Correcting /LI1/, Preserving /LI2/
/LI1/	LPI 1	2	/K28.5/D6.5/
/LI2/	LPI 2	2	/K28.5/D26.4/
	Link Status		
/Q/	Sequence ordered set	8	/K28.5/W0/K28.5/W1/K28.5/W2/ K28.5/W3[a]
	Reserved		
/Fsig/	Signal ordered set	8	/K28.5/W0/K28.5/W1/K28.5/W2/ K28.5/W3[a]

[a] /W0/, /W1/, /W2/, /W3/ are the 10-bit /Dx.y/ version of S0, S1, S2, S3 as defined per 127.2.5.2 and will never have a value of /D5.6/, /D16.2/, /D6.5/, /D26.4/.

Ordered sets are specified according to the following rules:

a) Ordered sets consist of either one, two, or eight code-groups.
b) The first code-group of all ordered sets is always a special code-group.
c) The second code-group of all multi-code-group ordered sets is always a data code-group. The second code-group is used to distinguish the ordered set from all other ordered sets.

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127.2.6.5 Comma considerations

The comma considerations are described in 36.2.4.8 and 36.2.4.9.

127.2.6.6 Sequence (/Q/)

A sequence ordered set is used to convey various optional link status such as local fault or remote fault. The 24-bit data of the sequence ordered set on the XGMII,when implemented, are mapped to S0, S1, S2, S3 (see 127.2.5.2), and /W0/, /W1/, /W2/, /W3/ are the 8B/10B mapped version.

S0, S1, S2, S3 are constructed such that each /Wn/ can be mapped to only 128 out of 256 possible /Dx.y/ code-groups. /W/ is defined to be the set of 128 /Dx.y/ code-groups that can appear in a sequence ordered set. /W/ does not contain /D5.6/, /D16.2/, /D6.5/, /D26.4/.

It is possible for the transmitter to send out a truncated sequence ordered set that appears as /K28.5/W0/K28.5/W1/. When a truncated sequence ordered set is received, the Word Decode process will convert it to idles.

127.2.6.7 Data (/D/)

A data code-group, when not used to distinguish or convey information for a defined ordered set, conveys one octet of arbitrary data supplied on the XGMII. The sequence of data code-groups is arbitrary, where any data code-group can be followed by any other data code-group. Data code-groups are coded and decoded but not interpreted by the PCS. Successful decoding of the data code-groups depends on proper receipt of the Start_of_Packet delimiter, as defined in 127.2.6.10 and the checking of validity, as defined in 36.2.4.6.

127.2.6.8 IDLE (/I/)

IDLE ordered sets (/I/) are transmitted continuously and repetitively whenever the XGMII is idle. /I/ provides a continuous fill pattern to establish and maintain clock synchronization. /I/ is emitted from, and interpreted by, the PCS. /I/ consists of one or more consecutively transmitted /I1/ or /I2/ ordered sets, as defined in Table 127–5.

The /I1/ ordered set is defined such that the running disparity at the end of the transmitted /I1/ is opposite that of the beginning running disparity. The /I2/ ordered set is defined such that the running disparity at the end of the transmitted /I2/ is the same as the beginning running disparity. The first /I/ following a packet or a sequence order set restores the current positive or negative running disparity to a negative value. All subsequent /I/s are /I2/ to ensure negative ending running disparity.

Distinct carrier events are separated by /I/s.

A received ordered set that consists of two code-groups, the first of which is /K28.5/ and the second of which is a data code-group other than any of the 128 possible /W/, /D21.5/, or /D2.2/ (or /D6.5/ or /D26.4/ to support EEE capability), is treated as an /I/ ordered set.

127.2.6.9 Low Power Idle (/LI/)

LPI is transmitted in the same manner as IDLE. LPI ordered sets (/LI/) are transmitted continuously and repetitively whenever the XGMII is indicating “Assert LPI”.

127.2.6.10 Start_of_Packet delimiter (SPD)

A Start_of_Packet delimiter (SPD) is used to delineate the starting boundary of a data transmission sequence. Upon initiation of packet transmission, the PCS replaces the first octet of the MAC preamble with

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SPD. Upon initiation of packet reception, the PCS replaces the received SPD delimiter with the data octet value associated with the first preamble octet. A SPD delimiter consists of the code-group /S/, as defined in Table 127–5.

127.2.6.11 End_of_Packet delimiter (EPD)

An End_of_Packet delimiter (EPD) is used to delineate the ending boundary of a packet. The EPD is transmitted by the PCS following the last data octet comprising the FCS of the MAC packet. On reception, EPD is interpreted by the PCS as terminating a packet. A EPD consists of the code-groups /T/R/. If /R/ is transmitted in an even-numbered code-group position, the PCS appends a single additional /R/ to the code-group stream to ensure that the subsequent /I/ is aligned on an even numbered code-group boundary. An /I/ always follows the conclusion of EPD. The /T/R/ or /T/R/R/ occupies part of the region considered by the MAC to be the IPG. The code-group /T/ and /R/ are defined in Table 127–5.

127.2.6.12 Error_Propagation (/V/)

Error_Propagation (/V/) indicates that the PCS client wishes to indicate a transmission error to its peer entity. /V/ is emitted from the PCS when the XGMII indicates transmit error propagation, or when the XGMII presents a mapping that is undefined in Table 127–3 to the Word Encode process. The code group /V/ is defined in Table 127–5.

The presence of Error_Propagation or any invalid code-group on the medium denotes an error condition. Invalid code-groups are not intentionally transmitted onto the medium.

127.2.7 Detailed functions and state diagrams

The body of this subclause comprises state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2.

127.2.7.1 State variables

127.2.7.1.1 Notation conventions

/x/
: Denotes the constant code-group specified in 127.2.7.1.2 (valid code-groups have to follow the rules of running disparity as per 127.2.6.3).

[/x/]
: Denotes the latched received value of the constant code-group (/x/) specified in 127.2.7.1.2 and conveyed by the SYNC_UNITDATA.indication message described in 127.2.7.1.6.

127.2.7.1.2 Constants

/COMMA/
: The set of special code-groups which include a comma as specified in 36.2.4.9 and listed in Table 36–2.

/D/
: The set of 256 code-groups corresponding to valid data, as specified in 127.2.6.7.

/Dx.y/
: One of the set of 256 code-groups corresponding to valid data, as specified in 127.2.6.7.

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/I/
: The IDLE ordered set group, comprising either the /I1/ or /I2/ ordered sets, as specified in 127.2.6.8.

/INVALID/
: The set of invalid data or special code-groups, as specified in 36.2.4.6.

/Kx.y/
: One of the set of 12 code-groups corresponding to valid special code-groups, as specified in Table 36–2.

/Q/
: Sequence ordered set as specified in 127.2.6.6. A properly formed sequence order set appears as /K28.5/W/K28.5/W/K28.5/W/K28.5/W/. A truncated sequence order set appears as /K28.5/W/K28.5/W/.

/R/
: The code-group used for the second and, if present, the third code-group in an End_of_Packet delimiter as specified in 127.2.6.11.

/S/
: The code-group corresponding to the Start_of_Packet delimiter (SPD) as specified in 127.2.6.10.

/T/
: The code-group used for the first code-group in the End_of_Packet delimiter as specified in 127.2.6.11.

/V/
: The Error_Propagation code-group, as specified in 127.2.6.12.

/W/
: The set of 128 code-groups that is generated by ENCODE(s<7:0>) where for all 128 possible values of x<6:0>
s<7> = x<6>, s<5:0> = x<5:0>,
s<6> is set to x<5> when x<2> = 1; and s<6> is set to x<6> when x<2> = 0
NOTE— /W/ is a subset of /D/.

PL_LIMIT
: The number of 2.5GPII symbols to preload in the Octets-to-Word process after release from the RESET state. The number of symbols to preload is implementation dependent and should be minimized to reduce latency. The minimum number has to be 3 to account for the deficit idle counting in 127.2.5.4.

The following constant is used only for the EEE capability:

/LI/
: The LP_IDLE ordered set group, comprising either the /LI1/ or /LI2/ ordered sets, as specified in 127.2.6.9.

127.2.7.1.3 Variables

assert_seq
: Alias used for sequence ordered set, consisting of the following terms:
tp_en=0 * tp_er=1 * (tpd<7:0> = 0x9C)

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cgbad

Alias for the following terms: ((rx_code-group∈/INVALID/) + (rx_code-group=/COMMA/*rx_even=TRUE)) * PMA_UNITDATA.indication

cggood

Alias for the following terms: !((rx_code-group∈/INVALID/) + (rx_code-group=/COMMA/*rx_even=TRUE)) * PMA_UNITDATA.indication

EVEN

The latched state of the rx_even variable, when rx_even=TRUE, as conveyed by the SYNC_UNITDATA.indication message described in 127.2.7.1.6.

mr_loopback

A Boolean that indicates the enabling and disabling of data being looped back through the PHY. Loopback of data through the PHY is enabled when Control register bit 3.0.14 is set to one.

Values: FALSE; Loopback through the PHY is disabled.
TRUE; Loopback through the PHY is enabled.

mr_main_reset

Controls the resetting of the PCS via control register bit 3.0.15.

Values: FALSE; Do not reset the PCS.
TRUE; Reset the PCS.

ODD

The latched state of the rx_even variable, when rx_even=FALSE, as conveyed by the SYNC_UNITDATA.indication message described in 127.2.7.1.6.

power_on

Condition that is true until such time as the power supply for the device that contains the PCS has reached the operating region. The condition is also true when the device has low power mode set via Control register bit 3.0.11.

Values: FALSE; The device is completely powered (default).
TRUE; The device has not been completely powered.

NOTE—Power_on evaluates to its default value in each state where it is not explicitly set.

rpd<7:0>

Single lane 2.5GPII receive data from the PCS receive process.

wd_rpd<31:0>

Receive data from the Octets-to-Word process. x= 0, 1, 2, 3 for the four sets of 2.5GPII.

rp_dv

Single lane 2.5GPII receive data valid from the PCS receive process.

Values: 0 or 1.

wd_rp_dv<3:0>

Receive data valid from the Octets-to-Word process.

Values: 0 or 1.

rp_er

Single lane 2.5GPII receive error from the PCS receive process.

Values: 0 or 1.

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wd_rp_er<3:0>
Receive error from the Octets-to-Word process.

Values: 0 or 1.

rx_bit
A binary parameter conveyed by the PMD_UNITDATA.indication service primitive, as specified in 128.2.2, to the PMA.

Values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

rx_code-group<9:0>
A 10-bit vector represented by the most recently received code-group from the PMA. The element rx_code-group<0> is the least recently received (oldest) rx_bit; rx_code-group<9> is the most recently received rx_bit (newest). When code-group alignment has been achieved, this vector contains precisely one code-group.

rx_even
A Boolean set by the PCS Synchronization process to designate received code-groups as either even- or odd-numbered code-groups as specified in 127.2.6.2.

Values: TRUE; Even-numbered code-group being received.
FALSE; Odd-numbered code-group being received.

RXC<3:0>
The RXC<3:0> signal of the XGMII as specified in Clause 46. Set by the Word Decode process.

RXD<31:0>
The RXD<31:0> signal of the XGMII as specified in Clause 46. Set by the Word Decode process.

signal_detect
A Boolean set by the PMD continuously via the PMD_SIGNAL.indication(SIGNAL_DETECT) message to indicate the status of the incoming link signal.

Values: FAIL; A signal is not present on the link.
OK; A signal is present on the link.

sync_status
Alias used by the PCS receive state diagram, consisting of the following terms:

sync_status = code_sync_status + rx_lpi_active.

Values: FAIL; A signal is not present on the link.
OK; A signal is present on the link.

NOTE—If EEE is not supported, the variable rx_lpi_active is always false, and this variable is identical to code_sync_status controlled by the synchronization state diagram.

tpd<7:0>
Single lane 2.5GPII transmit data to the PCS transmit process.

tpd_t1<7:0>
The value of tpd<7:0> latched by cg_timer_done = TRUE.

Values: 0 or 1.

we_tpd<31:0>
Transmit data output of the WORD ENCODE process.

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tp_en
: Single lane 2.5GPII transmit data enable to the PCS transmit process.

  Values: 0 or 1.

we_tp_en<3:0>
: Transmit data valid output of the WORD ENCODE process.

  Values: 0 or 1.

tp_er
: Single lane 2.5GPII transmit error to the PCS transmit process.

  Values: 0 or 1.

we_tp_er<3:0>
: Transmit error output of the WORD ENCODE process.

  Values: 0 or 1.

tx_bit
: A binary parameter used to convey data from the PMA to the PMD via the PMD_UNITDATA.request service primitive as specified in 128.2.1.

  Values: ZERO; Data bit is a logical zero.
  ONE; Data bit is a logical one.

tx_code-group<9:0>
: A vector of bits representing one code-group, as specified in Table 36–1a through Table 36–1e, or Table 36–2, which has been prepared for transmission by the PCS Transmit process. This vector is conveyed to the PMA as the parameter of the PMD_UNITDATA.request(tx_bit) service primitive. The element tx_code-group<0> is the first tx_bit transmitted; tx_code-group<9> is the last tx_bit transmitted.

tx_disparity
: A Boolean set by the PCS Transmit process to indicate the running disparity at the end of code-group transmission as a binary value. Running disparity is described in 36.2.4.4.

  Values: POSITIVE
  NEGATIVE

tx_even
: A Boolean set by the PCS Transmit process to designate transmitted code-groups as either even or odd numbered code-groups as specified in 127.2.6.2.

  Values: TRUE; Even-numbered code-group being transmitted.
  FALSE; Odd-numbered code-group being transmitted.

tx_o_set
: One of the following defined ordered sets: /T/, /R/, /I/, /S/, /V/, /LI/, or one of the following code-groups: /K28.5/ or /D/.

TXC<3:0>
: The TXC<3:0> signal of the XGMII as specified in Clause 46.

TXD<31:0>
: The TXD<31:0> signal of the XGMII as specified in Clause 46.

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wdecode_state
: Word Decoder State used by the Word Decode process to properly assemble the next XGMII value to output.

  Values: DATA;
  IDLE;
  SEQ;

wencode_state
: Word Encoder State used by the Word Encode process to properly assemble the Sequence ordered set.

  Values: DATA;
  IDLE;
  SEQ;

xgmii_txc_lo<3:0>
: The value of xgmii_txc_lo_neg<3:0> latched by the rising edge of TX_CLK.

xgmii_txc_lo_neg<3:0>
: The value of TXC<3:0> latched by the falling edge of TX_CLK.

xgmii_txc_hi<3:0>
: The value of TXC<3:0> latched by the rising edge of TX_CLK.

xgmii_txd_lo<31:0>
: The value of xgmii_txd_lo_neg<31:0> latched by the rising edge of TX_CLK.

xgmii_txd_lo_neg<31:0>
: The value of TXD<3:0> latched by the falling edge of TX_CLK.

xgmii_txd_hi<31:0>
: The value of TXD<31:0> latched by the rising edge of TX_CLK.

The following variables are used only for the EEE capability:

assert_lpidle
: Alias used for the optional LPI function, consisting of the following terms:

  (tp_en=0 * tp_er=1 * (tpd<7:0> = 0x01))

code_sync_status
: A parameter set by the PCS Synchronization process to reflect the status of the link as viewed by the receiver.

  Values: FAIL; The receiver is not synchronized to code-group boundaries.
  OK; The receiver is synchronized to code-group boundaries.

idle_d
: Alias for the following terms:

  SUDI(![/D21.5/] * ![/D2.2/]) when EEE is not supported, or

  SUDI(![/D21.5/] * ![/D2.2/] * ![/D6.5/] * ![/D26.4/]) when EEE is supported.

rx_lpi_active
: A Boolean variable that is set to TRUE when the receiver is in a low power state and set to FALSE when it is in an active state and capable of receiving data.

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rx_quiet

A Boolean variable set to TRUE while in the RX_QUIET state and set to FALSE otherwise.

tx_quiet

A Boolean variable set to TRUE when the transmitter is in the TX_QUIET state and set to FALSE otherwise. When set to TRUE, the PMD will disable the transmitter as described in 128.6.5.

127.2.7.1.4 Functions

carrier_detect

In the PCS Receive process, this function uses for input the latched code-group ([/x/]) and latched rx_even (EVEN/ODD) parameters of the SYNC_UNITDATA.indication message from the PCS Synchronization process. When SYNC_UNITDATA.indication message indicates EVEN, the carrier_detect function detects carrier when either:

a) A two or more bit difference between [/x/] and both /K28.5/ encodings exists (see Table 36–2); or

b) A two to nine bit difference between [/x/] and the expected /K28.5/ (based on current running disparity) exists.

Values: TRUE; Carrier is detected.
FALSE; Carrier is not detected.

check_end

Prescient End_of_Packet function used by the PCS Receive process. The check_end function returns the current and next two code-groups in rx_code-group<9:0>.

DECODE([/x]/)

In the PCS Receive process, this function takes as its argument the latched value of rx_code-group<9:0> ([/x/]) and the current running disparity, and returns the corresponding 2.5GPII rpd<7:0>, as per Table 36–1a to Table 36–1e. DECODE also updates the current running disparity per the running disparity rules outlined in 36.2.4.4.

ENCODE(x)

In the PCS Transmit process, this function takes as its argument (x), where x is a 2.5GPII tpd<7:0> octet, and the current running disparity, and returns the corresponding ten-bit code-group as per Table 36–1a to Table 36–1e. ENCODE also updates the current running disparity variable tx_disparity per the running disparity rules outlined in 36.2.4.4.

NEXTSEQ

Prescient function used by the Word Decode process that returns whether the next four 2.5GPII symbols presented to the Word Decode process is of the form: Sequence, Data, Sequence, Data.

Values: TRUE; Next four 2.5GPII symbols are Sequence, Data, Sequence, Data.
FALSE; Next four 2.5GPII symbols are not Sequence, Data, Sequence, Data.

signal_detectCHANGE

In the PCS Synchronization process, this function monitors the signal_detect variable for a state change. The function is set upon state change detection.

Values: TRUE; A signal_detect variable state change has been detected.
FALSE; A signal_detect variable state change has not been detected (default).

NOTE—signal_detectCHANGE is set by this function definition; it is not set explicitly in the state diagrams. signal_detectCHANGE evaluates to its default value upon state entry.

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SINSERT(x)

Add a single 2.5GPII symbol to the end of a queue that stores the 2.5GPII symbol presented by the receive process. The variable x is the 2.5GPII symbol (rp_dv, rp_er, rpd<7:0>). If x is a null set, then all content in the queue is emptied. The depth of the queue is implementation dependent.

VOID(x)

x ∈ /D/, /T/, /R/, /K28.5/. Substitutes /V/ on a per code-group basis as requested by the 2.5GPII.

If [tp_en=0 * tp_er=1 * tpd<7:0>≠(0000 1111)],

then return /V/;

Else if [tp_en=1 * tp_er=1],

then return /V/;

Else return x.

WALIGN

In the PCS Octets-to-Word process, this function performs the alignment according to 127.2.5.4. Four 2.5GPII symbols (wd_rp_dv<3:0>, wd_rp_er<3:0>, wd_rpd<31:0>) are returned by this function. wd_rpd<7:0> is the earliest to arrive and wd_rpd<31:24> is last. The SINSERT(x) function adds 2.5GPII symbols to the queue. The WALIGN functions removes one to seven 2.5GPII symbols from the front of the queue every time it is called.

When no 2.5GPII symbols are inserted or deleted, this function will return the first four 2.5GPII symbols in the queue and remove them from the queue.

When X 2.5GPII idles symbols are inserted, then X 2.5GPII idles symbols and the first 4 – X 2.5GPII symbols are returned by the function, and the first 4 - X 2.5GPII symbols are removed from the queue.

When X 2.5GPII symbols are deleted, then the first X 2.5GPII symbols are removed from the queue, and the next four in the queue are returned by the function and then removed from the queue.

WDECODE(x, y, z)

In the PCS Word Decode process, this function performs the mapping according to 127.2.5.5. The variable x is four sets of 2.5GPII variables wd_rp_dv<3:0>, wd_rp_er<3:0>, wd_rpd<31:0>, the variable y is the current state of the wdecode_state variable, and the variable z indicates whether the next four 2.5GPII symbols are of the form: Sequence, Data, Sequence, Data.

The output is XGMII RXC<3:0>, RXD<31:0>, wdecode_state.

WENCODE(x, y)

In the PCS Word Encode process, this function performs the mapping according to 127.2.5.2. The variable x is xgmii_txc_lo<3:0> or xgmii_txc_hi<3:0>, xgmii_txd_lo<31:0> or xgmii_txd_hi<31:0>, and the variable y is the current state of the wencode_state variable.

The output is four sets of 2.5GPII variables and the updated state of the wencode_state variable and is ordered as follows: we_tp_en<3:0>, we_tp_er<3:0>, we_tpd<31:0>, wencode_state.

127.2.7.1.5 Counters

good_cgs

Count of consecutive valid code-groups received.

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plcnt

Count of number the number of 2.5GPII symbols to preload in the Octets-to-Word process after release from the RESET state. The number of symbols to preload is implementation dependent and should be minimized to reduce latency.

The following counter is used only for the EEE capability:

wake_error_counter

A counter that is incremented each time that the LPI receive state diagram enters the RX_WTF state indicating that a wake time fault has been detected. The counter is reflected in register 3.22 (see 45.2.3.12).

127.2.7.1.6 Messages

PMA_UNITDATA.indication(rx_code-group<9:0>)

A signal sent by the PMA Receive process conveying the next code-group received over the medium (see 127.3.1.2).

PMA_UNITDATA.request(tx_code-group<9:0>)

A signal sent to the PMA Transmit process conveying the next code-group ready for transmission over the medium (see 127.3.1.1).

PMD_SIGNAL.indication(SIGNAL_DETECT)

A signal sent by the PMD to indicate the status of the signal being received on the MDI.

PUDI

Alias for PMA_UNITDATA.indication(rx_code-group<9:0>).

PUDR

Alias for PMA_UNITDATA.request(tx_code-group<9:0>).

SUDI

Alias for SYNC_UNITDATA.indication(parameters).

SYNC_UNITDATA.indication(parameters)

A signal sent by the PCS Synchronization process to the PCS Receive process conveying the following parameters:

Parameters: [/x/]; the latched value of the indicated code-group (/x/);
EVEN/ODD; the latched state of the rx_even variable;

Value: EVEN; passed when the latched state of rx_even=TRUE.
ODD; passed when the latched state of rx_even=FALSE.

TX_OSET.indication

A signal sent to the PCS Transmit ordered set process from the PCS Transmit code-group process signifying the completion of transmission of one ordered set.

The following messages are used only for the EEE capability:

PMD_RXQUIET.request(rx_quiet)

A signal sent by the PCS/PMA LPI receive state diagram to the PMD. This message is ignored by devices that do not support EEE capability.

Values: TRUE: The receiver is in a quiet state and is not expecting incoming data.
FALSE: The receiver is ready to receive data.

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PMD_TXQUIET.request(tx_quiet)

A signal sent by the PCS/PMA LPI transmit state diagram to the PMD. This message is ignored by devices that do not support the optional LPI mechanism.

Values: TRUE: The transmitter is in a quiet state and may cease to transmit a signal on the medium.
FALSE: The transmitter is ready to transmit data.

127.2.7.1.7 Timers

cg_timer

A continuous free-running timer. If XGMII is implemented, cg_timer shall expire synchronously with the rising edge of TX_CLK as well as every one-eighth of the TX_CLK cycle time (see tolerance required for TX_CLK in 46.3.1.1). In the absence of XGMII, cg_timer shall expire every 3.2 ns ± 100 ppm.

Values: The condition cg_timer_done becomes true upon timer expiration.

Restart when: immediately after expiration; restarting the timer resets the condition cg_timer_done.

Duration: 3.2 ns nominal.

TX_CLK_timer

A continuous free-running timer. TX_CLK_timer shall expire synchronously with the rising edge of TX_CLK (see tolerance required for TX_CLK in 46.3.1.1).

Restart when: immediately after expiration.

Duration: 25.6 ns nominal.

The following timers are used only for the EEE capability:

rx_tq_timer

This timer is started when the PCS receiver enters the START_TQ_TIMER state. The timer terminal count is set to T_{QR}. When the timer reaches terminal count, it will set the rx_tq_timer_done = TRUE.

rx_tw_timer

This timer is started when the PCS receiver enters the RX_WAKE state. The timer terminal count shall not exceed the maximum value of T_{WR} in Table 127–7. When the timer reaches terminal count, it will set the rx_tw_timer_done = TRUE.

rx_wf_timer

This timer is started when the PCS receiver enters the RX_WTF state, indicating that the receiver has encountered a wake time fault. The rx_wf_timer allows the receiver an additional period in which to synchronize or return to the quiescent state before a link failure is indicated. The timer terminal count is set to T_{WTF}. When the timer reaches terminal count, it will set the rx_wf_timer_done = TRUE.

tx_tq_timer

This timer is started when the PCS transmitter enters the TX_QUIET state. The timer terminal count is set to T_{QL}. When the timer reaches terminal count, it will set the tx_tq_timer_done = TRUE.

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tx_tr_timer
: This timer is started when the PCS transmitter enters the TX_REFRESH state. The timer terminal count is set to T_{UL}. When the timer reaches terminal count, it will set the tx_tr_timer_done = TRUE.

tx_ts_timer
: This timer is started when the PCS transmitter enters the TX_SLEEP state. The timer terminal count is set to T_{SL}. When the timer reaches terminal count, it will set the tx_ts_timer_done = TRUE.

127.2.7.2 State diagrams

127.2.7.2.1 Word Encode and Word-to-Octets

The Word Encode process (see 127.2.5.2) and Word-to-Octets process (see 127.2.5.3) are merged into one state diagram depicted in Figure 127–4, including compliance with the associated state variables as specified in 127.2.7.1.

The Word Encode process continuously maps the four XGMII lanes to four 2.5GPII symbols via the WENCODE function in the TX_XGMII_LO and TX_XGMII_HI states. The four 2.5GPII symbols are then serialized and output one at a time by the Word-to-Octets process. The presentation of the 2.5GPII symbols are synchronized to the PCS transmit process such that the 2.5GPII index 0 and 2 symbols are presented to the PCS transmit process which will result in the corresponding ordered set to be output to the PMA when the variable tx_even is TRUE and index 1 and 3 variables when tx_even is FALSE.

127.2.7.2.2 Transmit

The PCS Transmit process is depicted in two state diagrams: PCS Transmit ordered set and PCS Transmit code-group. The PCS shall implement its Transmit process as depicted in Figure 127–5 and Figure 127–6, including compliance with the associated state variables as specified in 127.2.7.1.

The Transmit ordered set process continuously sources ordered sets to the Transmit code-group process. Upon the assertion of tp_en by the 2.5GPII, the SPD ordered set is sourced. Following the SPD, /D/ code-groups are sourced until tp_en is deasserted. Following the de-assertion of tp_en, EPD ordered sets are sourced. If tp_en and tp_er are both deasserted, the /R/ ordered set may be sourced, after which the sourcing of /I/ is resumed. If, while tp_en is asserted, the tp_er signal is asserted, the /V/ ordered set is sourced except when the SPD ordered set is selected for sourcing. If the 2.5GPII indicates sequence, then /Q/ ordered sets are sourced. If the optional EEE is enabled and the 2.5GPII indicates low power idles, then /LI/ ordered sets are sourced.

The Transmit code-group process continuously sources tx_code-group<9:0> to the PMA based on the ordered sets sourced to it by the Transmit ordered set process. The Transmit code-group process determines the proper code-group to source based on even/odd-numbered code-group alignment, running disparity requirements, and ordered set format.

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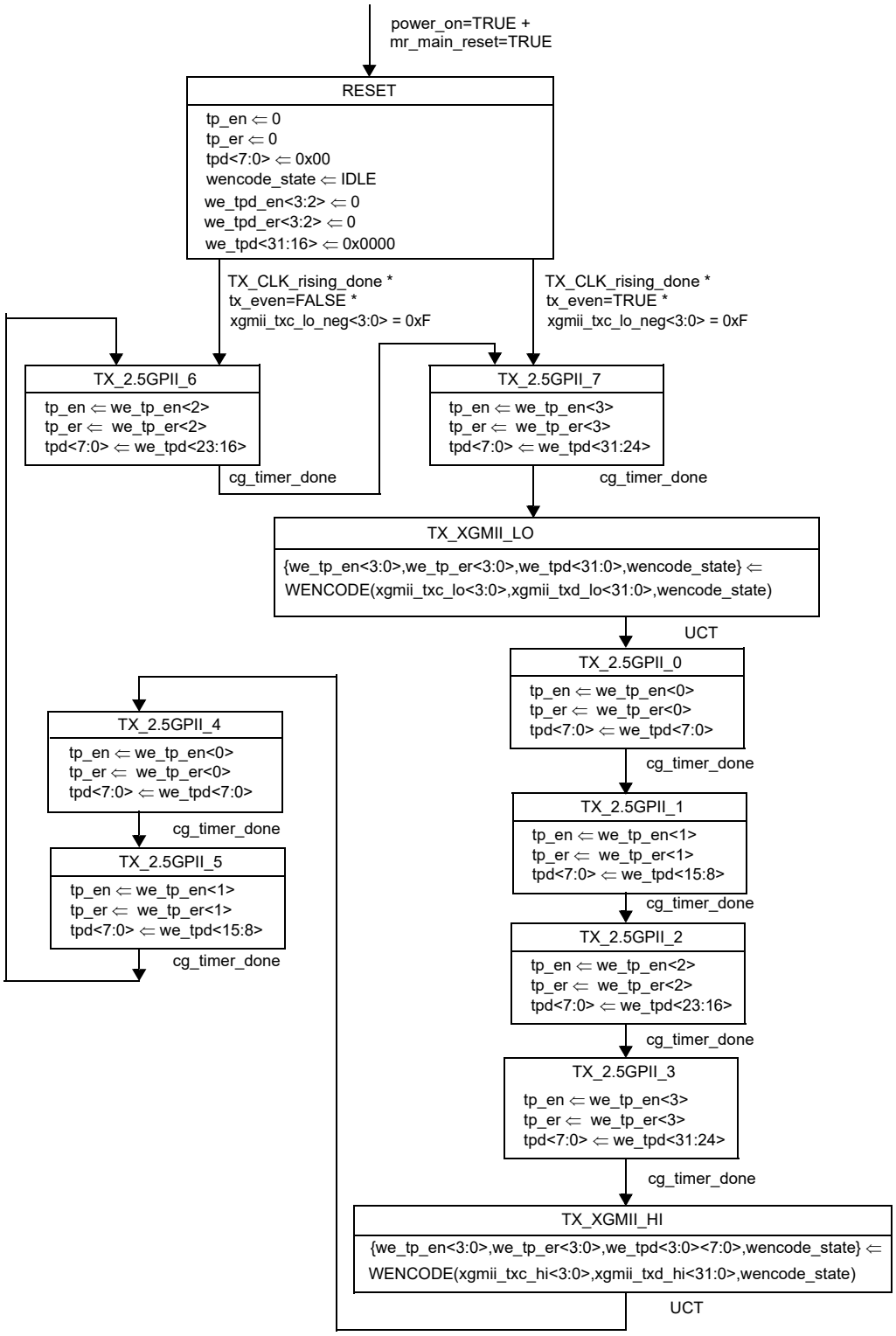

Figure 127–4—PHY TX control state diagram

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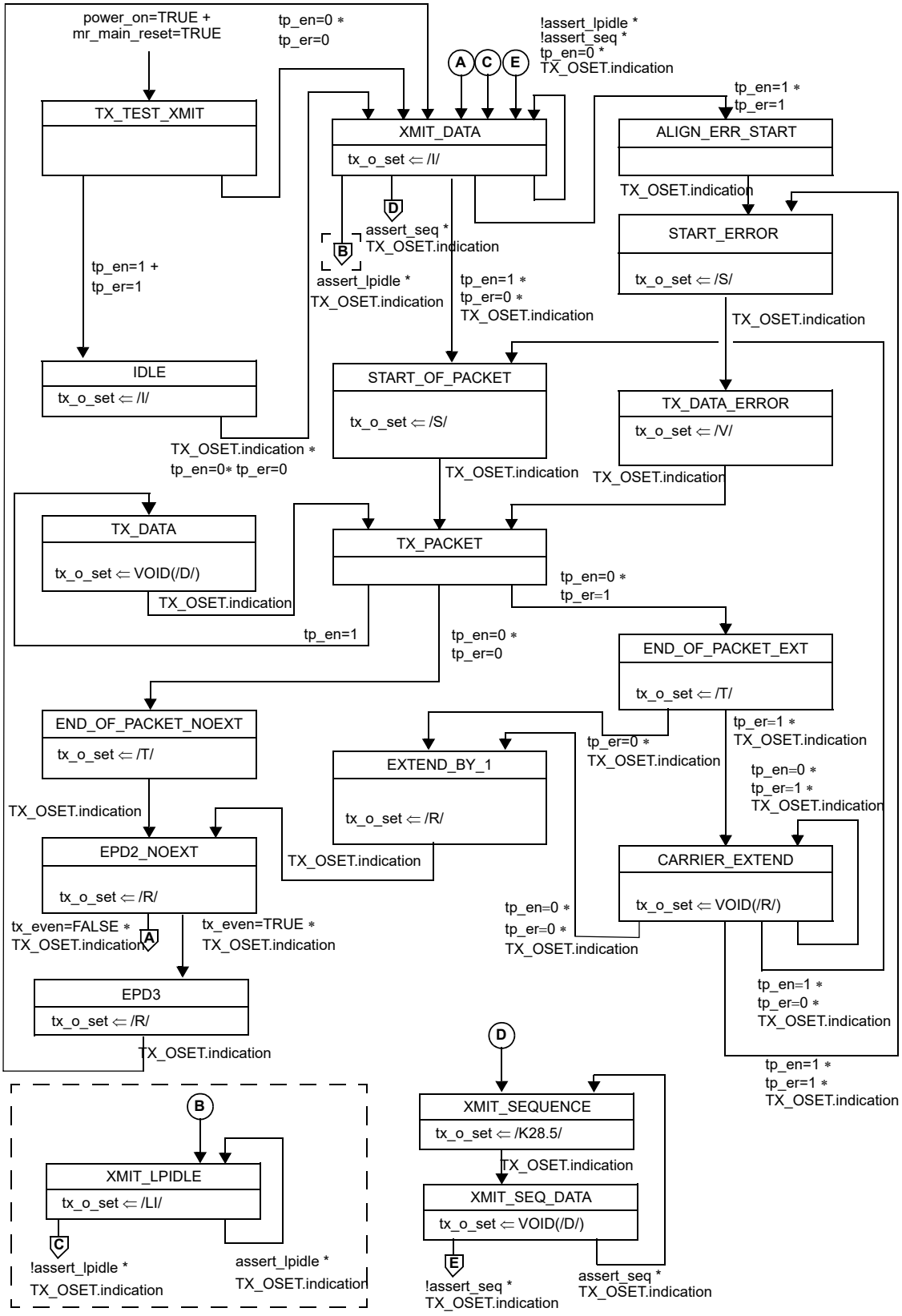

NOTE—A transition inside a dashed box is only required for the EEE capability.

Figure 127–5—PCS transmit ordered set state diagram

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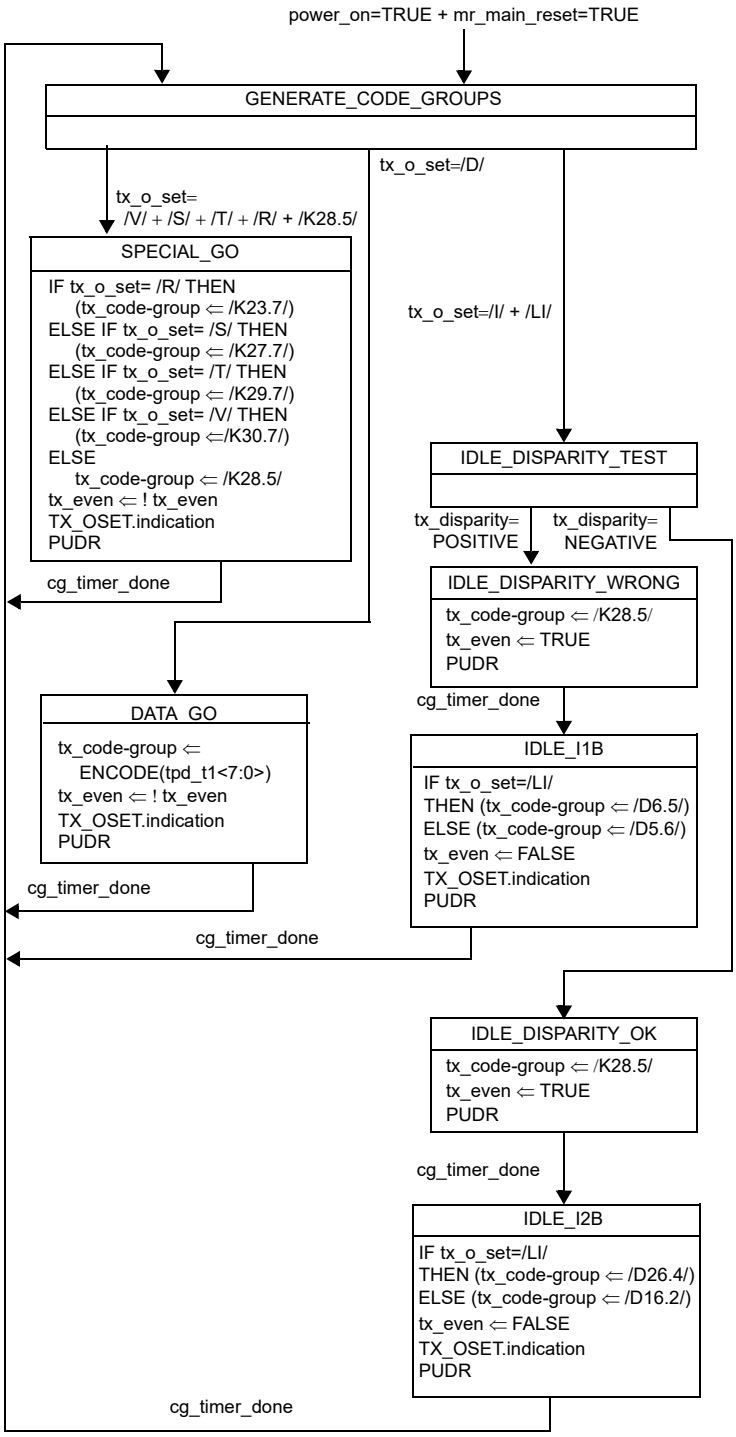

Figure 127–6—PCS transmit code-group state diagram

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127.2.7.2.3 Synchronization

The PCS shall implement the Synchronization process as depicted in Figure 127–7 including compliance with the associated state variables as specified in 127.2.7.1. The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PMA client to suspend normal actions.

A receiver that is in the LOSS_OF_SYNC state and that has acquired bit synchronization attempts to acquire code-group synchronization via the Synchronization process. Code-group synchronization is acquired by the detection of three ordered sets containing commas in their leftmost bit positions without intervening invalid code-group errors. Upon acquisition of code-group synchronization, the receiver enters the SYNC_ACQUIRED_1 state. Acquisition of synchronization ensures the alignment of multi-code-group ordered sets to even-numbered code-group boundaries.

Once synchronization is acquired, the Synchronization process tests received code-groups in sets of four code-groups and employs multiple sub-states, to move between the SYNC_ACQUIRED_1 and LOSS_OF_SYNC states.

For EEE capability the relationship between sync_status and code_sync_status is given by the definition of the sync_status variable in 127.2.7.1.3; otherwise sync_status is identical to code_sync_status.

127.2.7.2.4 Receive

The PCS shall implement its Receive process as depicted in Figure 127–8a and Figure 127–8b, including compliance with the associated state variables as specified in 127.2.7.1. The PCS shall implement Figure 127–8c if the optional EEE is present and enabled.

The PCS Receive process continuously passes rpd<7:0> and sets the rp_dv and rp_er signals to the 2.5GPII based on the received code-group from the PMA.

127.2.7.2.5 Octets-to-Word and Decode

The Octets-to-Word process and Word decode process are merged into one state diagram depicted in Figure 127–9, including compliance with the associated state variables as specified in 127.2.7.1.

The Octets-to-Word process continuously queues the incoming 2.5GPII symbols from the PCS receive process and outputs four 2.5GPII symbols at a time using the WALIGN function. Symbols may be dropped or idles symbols added by the WALIGN function. The Word Decode process continuously maps the four 2.5GPII symbols and presents them on the XGMII using the WDECODE function in the RX_XGMII state.

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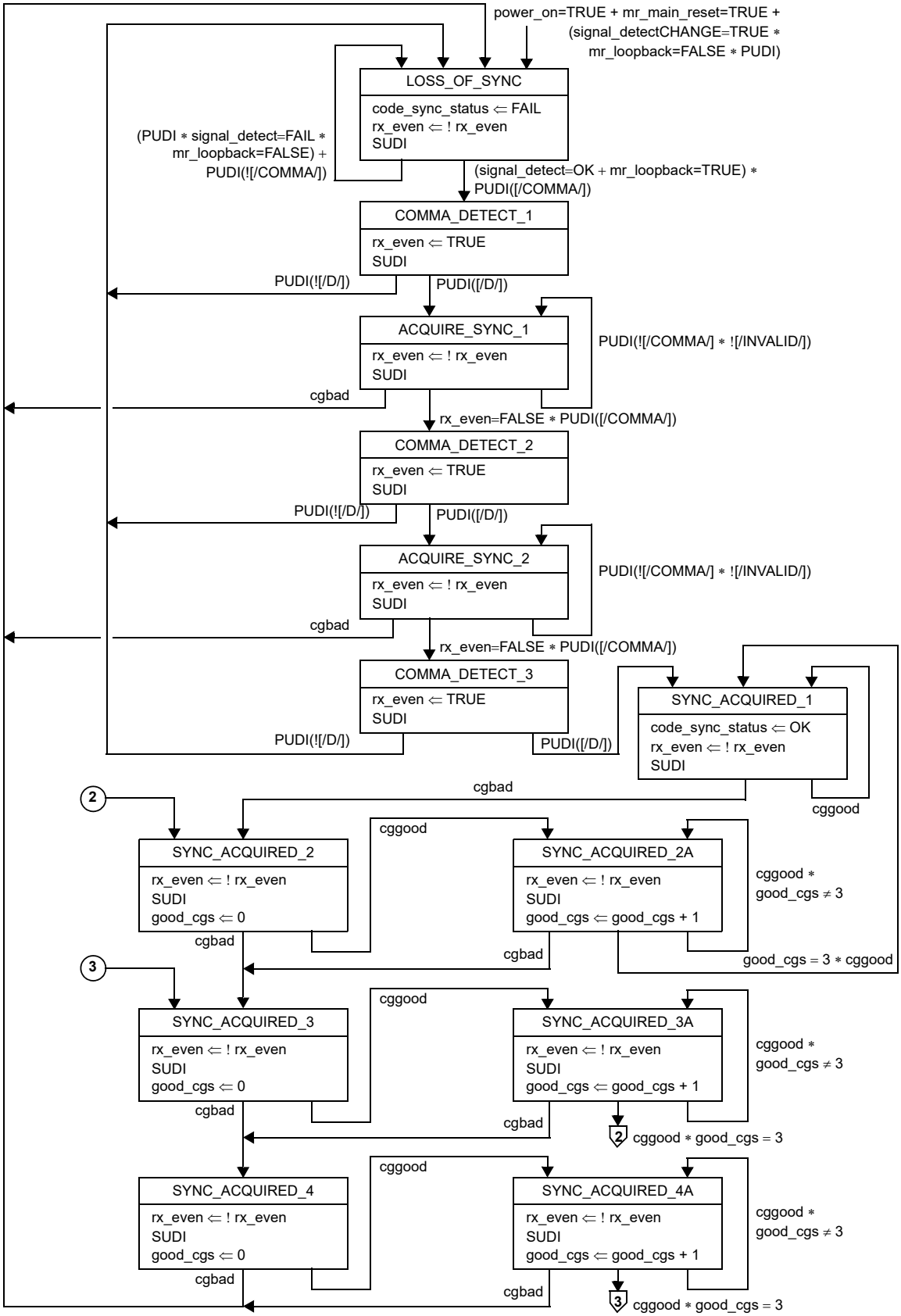

Figure 127–7—Synchronization state diagram

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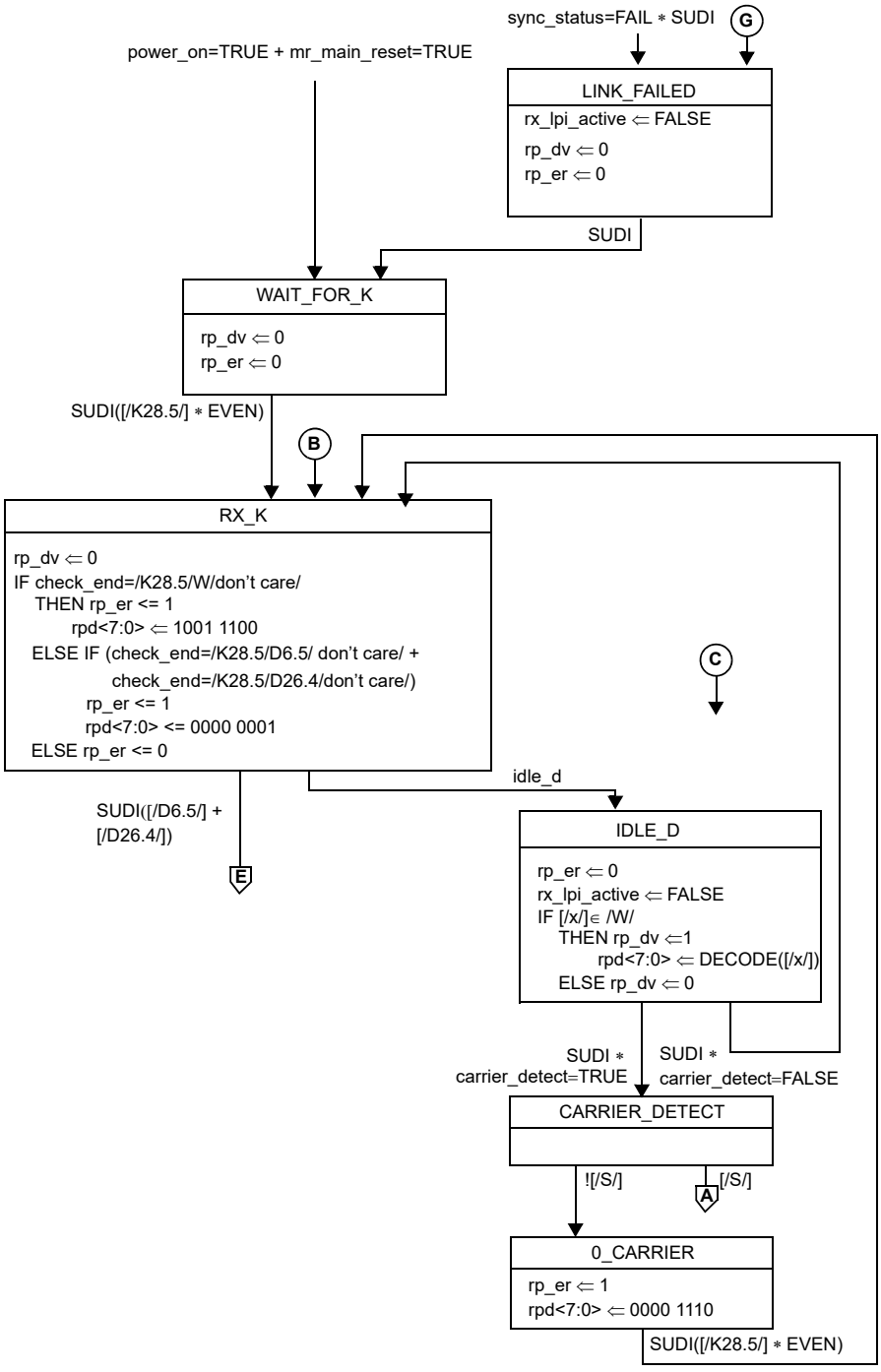

NOTE 1 —Outgoing arcs leading to labeled polygons flow off page to corresponding incoming arcs leading from labeled circles on Figure 127–8b and Figure 127–8c, and vice versa.

NOTE 2—The transitions from the CARRIER_DETECT state is a test against the codegroup obtained from the SUDI that caused the transition to the CARRIER_DETECT state.

Figure 127–8a—PCS receive state diagram, part a

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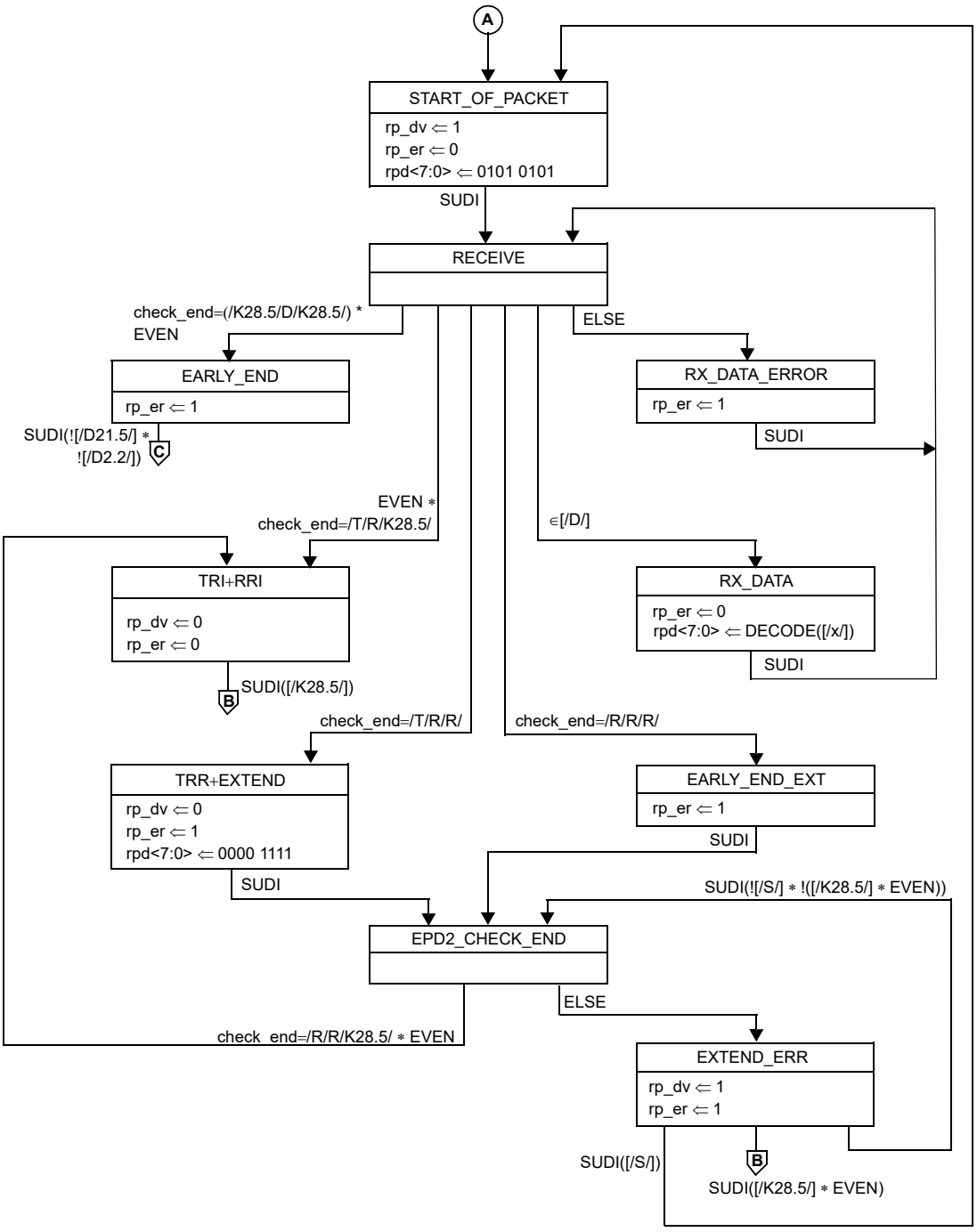

NOTE 1—Outgoing arcs leading to labeled polygons flow off page to corresponding incoming arcs leading from labeled circles on Figure 127–8a, and vice versa.

NOTE 2—In the transition from RECEIVE to RX_DATA state the transition condition is a test against the code-group obtained from the SUDI that caused the transition to RECEIVE state.

Figure 127–8b—PCS receive state diagram, part b

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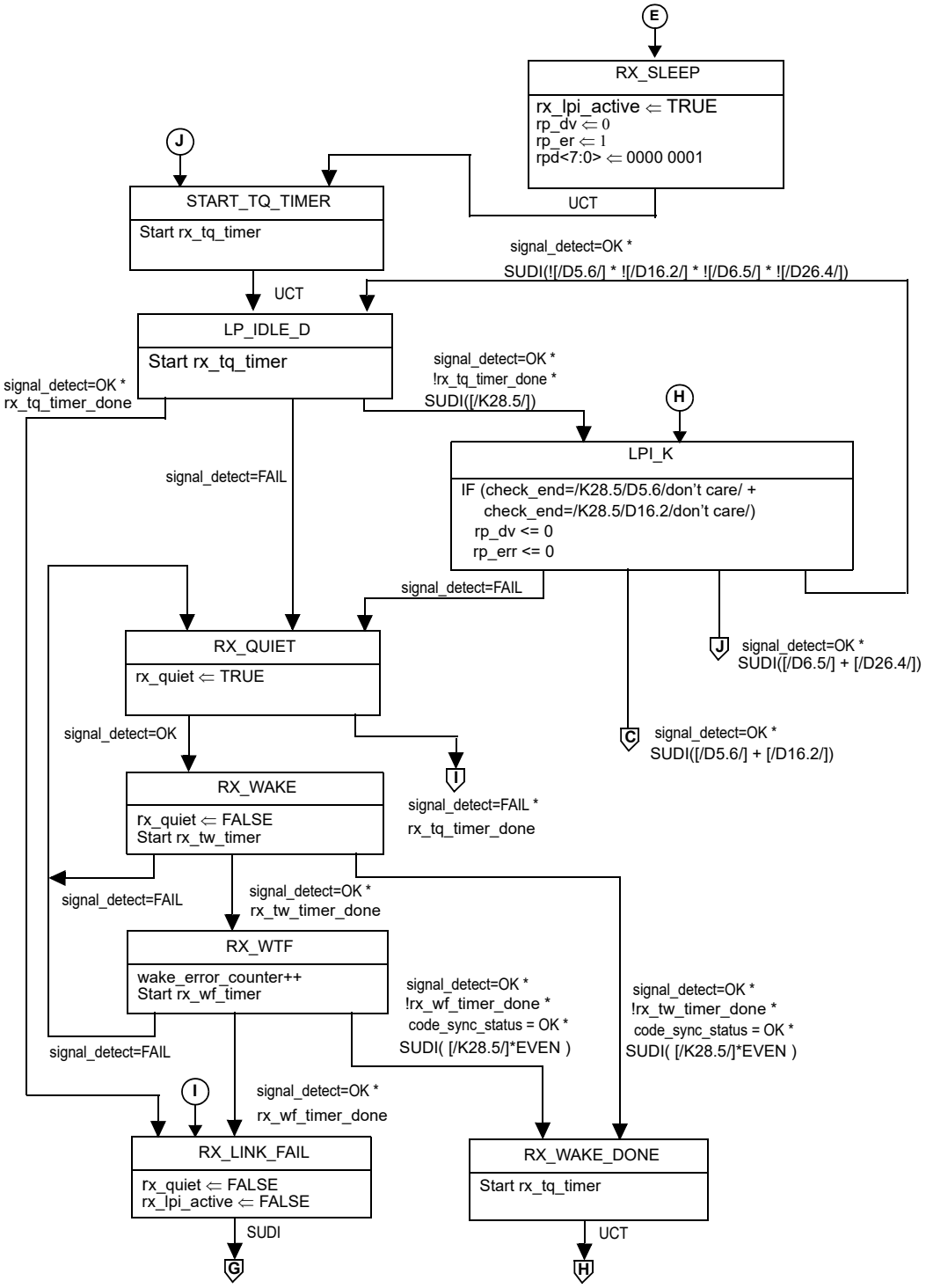

NOTE—Outgoing arcs leading to labeled polygons flow off page to corresponding incoming arcs leading from labeled circles on Figure 127–8a, and vice versa.

Figure 127–8c—PCS Receive state diagram, part c
(only required for the optional EEE capability)

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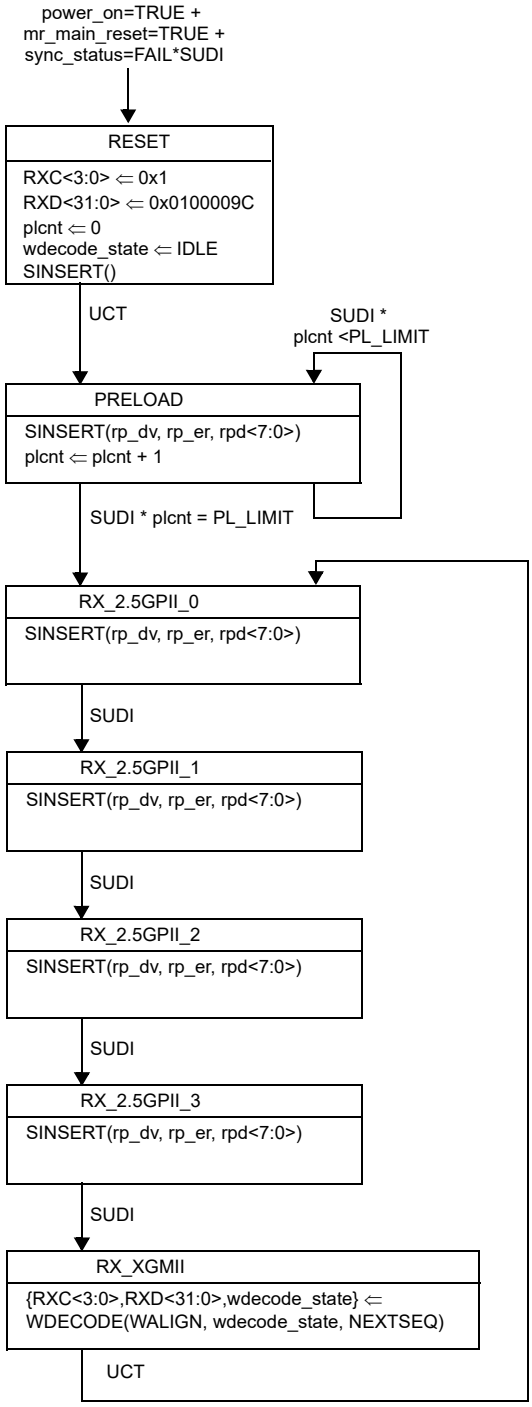

Figure 127–9—Octets-to-Word and Decode state diagram

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127.2.7.2.6 LPI state diagram

A PCS that supports the EEE capability shall implement the LPI transmit process as shown in Figure 127–10. The transmit LPI state diagram controls tx_quiet, which disables the transmitter when true.

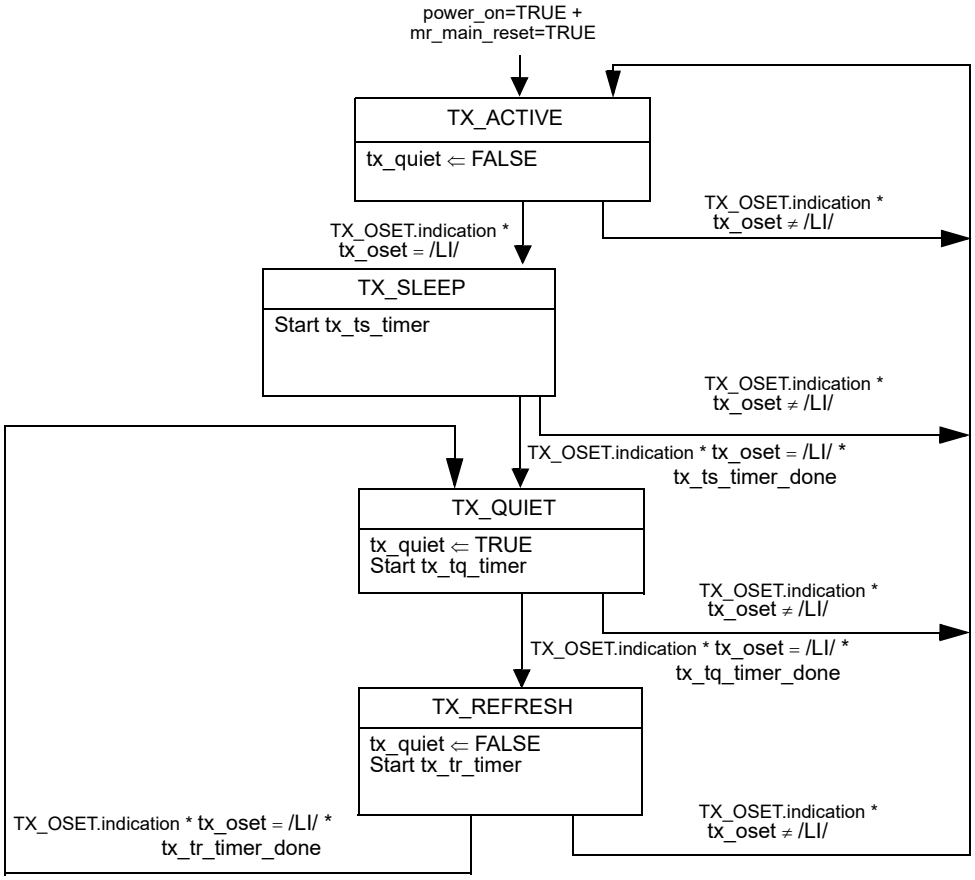

Figure 127–10—LPI Transmit state diagram

The timer values for these state diagrams are shown in Table 127–6 for transmit and Table 127–7 for receive.

Table 127–6—Transmitter LPI timing parameters

Parameter	Description	Min	Max	Units
T_{SL}	Local Sleep Time from entering the TX_SLEEP state to when tx_quiet is set to TRUE	19.9	20.1	µs
T_{QL}	Local Quiet Time from when tx_quiet is set to TRUE to entry into the TX_REFRESH state	2.5	2.6	ms
T_{UL}	Local Refresh Time from entry into the TX_REFRESH state to entry into the TX_QUIET state	19.9	20.1	µs

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Table 127–7—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for signal detect to be set to OK while in the LP_IDLE_D, LPI_K and RX_QUIET states before asserting a rx_fault	3	4	ms
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault (WTF)		11	µs
T_{WTF}	Wake time fault recovery time		1	ms

127.2.7.2.7 LPI status and management

For EEE capability, the PCS indicates to the management system that LPI is currently active in the receive and transmit directions using the status variables shown in Table 36–10.

127.3 Physical Medium Attachment (PMA) sublayer

127.3.1 Service Interface

The PMA provides a Service Interface to the PCS. These services are described in an abstract manner and do not imply any particular implementation. The PMA Service Interface supports the exchange of code-groups between PCS entities. The PMA converts code-groups into bits and passes these to the PMD, and vice versa. It also generates an additional status indication for use by its client.

The following primitives are defined:

PMA_UNITDATA.request(tx_code-group<9:0>)

PMA_UNITDATA.indication(rx_code-group<9:0>)

127.3.1.1 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of code-groups) from the PCS to the PMA. PMA_UNITDATA.request is generated by the PCS Transmit process.

127.3.1.1.1 Semantics of the service primitive

PMA_UNITDATA.request(tx_code-group<9:0>)

The data conveyed by PMA_UNITDATA.request is the tx_code-group<9:0> parameter defined in 127.2.7.1.3.

127.3.1.1.2 When generated

The PCS continuously sends, at a nominal rate of 312.5 MHz, tx_code-group<9:0> to the PMA.

127.3.1.1.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a series of ten PMD_UNITDATA.request primitives, requesting transmission of the indicated tx_bit to the PMD.

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127.3.1.2 PMA_UNITDATA.indication

This primitive defines the transfer of data (in the form of code-groups) from the PMA to the PCS. PMA_UNITDATA.indication is used by the PCS Synchronization process.

127.3.1.2.1 Semantics of the service primitive

PMA_UNITDATA.indication(rx_code-group<9:0>)

The data conveyed by PMA_UNITDATA.indication is the rx_code-group<9:0> parameter defined in 127.2.7.1.3.

127.3.1.2.2 When generated

The PMA continuously sends one rx_code-group<9:0> to the PCS corresponding to the receipt of each code-group aligned set of ten PMD_UNITDATA.indication primitives received from the PMD. The nominal rate of the PMA_UNITDATA.indication primitive is 312.5 MHz, as governed by the recovered bit clock.

127.3.1.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

127.3.2 Functions within the PMA

Figure 127–2 and Figure 127–3 depict the mapping of the four octet-wide data path of the XGMII to the ten-bit code-groups of the PMA Service Interface and on to the serial PMD Service Interface. The PMA comprises the PMA Transmit and PMA Receive processes for 2.5GBASE-X.

The PMA Transmit process serializes tx_code-groups into tx_bits and passes them to the PMD for transmission on the underlying medium, according to Figure 127–3. Similarly, the PMA Receive process deserializes rx_bits received from the PMD according to Figure 127–3. The PMA continuously conveys ten bit code-groups to the PCS, independent of code-group alignment. After code-group alignment is achieved, based on comma detection, the PCS converts code-groups into XGMII data octets, according to 127.2.7.2.4 and 127.2.7.2.5.

The proper alignment of a comma used for code-group synchronization is depicted in Figure 127–3.

127.3.2.1 Data delay

The PMA maps a nonaligned one-bit data path from the PMD to an aligned, ten-bit-wide data path to the PCS, on the receive side. Logically, received bits have to be buffered to facilitate proper code-group alignment. These functions necessitate an internal PMA delay of at least ten bit times. In practice, code-group alignment may necessitate even longer delays of the incoming rx_bit stream.

127.3.2.2 PMA transmit function

The PMA Transmit function passes data unaltered (except for serializing) from the PCS directly to the PMD. Upon receipt of a PMA_UNITDATA.request primitive, the PMA Transmit function shall serialize the ten bits of the tx_code-group<9:0> parameter and transmit them to the PMD in the form of ten successive PMD_UNITDATA.request primitives, with tx_code-group<0> transmitted first, and tx_code-group<9> transmitted last.

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127.3.2.3 PMA receive function

The PMA Receive function passes data unaltered (except for deserializing and possible code-group slipping upon code-group alignment) from the PMD directly to the PCS. Upon receipt of ten successive PMD_UNITDATA.indication primitives, the PMA shall assemble the ten received rx_bits into a single ten-bit value and pass that value to the PCS as the rx_code-group<9:0> parameter of the primitive PMA_UNITDATA.indication, with the first received bit installed in rx_code-group<0> and the last received bit installed in rx_code-group<9>. An exception to this operation is specified in 127.3.2.4.

127.3.2.4 Code-group alignment

In the event the PMA sublayer detects a comma+ within the incoming rx_bit stream, it may realign its current code-group boundary, if necessary, to that of the received comma+ as shown in Figure 36–3. This process is referred to in this document as code-group alignment. During the code-group alignment process, the PMA sublayer may delete or modify up to four, but shall delete or modify no more than four, ten-bit code-groups in order to align the correct receive clock and code-group containing the comma+. This process is referred to as code-group slipping.

In addition, the PMA sublayer is permitted to realign the current code-group boundary upon receipt of a comma-pattern.

127.3.3 Loopback mode

Loopback mode shall be provided, as specified in this subclause, by the transmitter and receiver of a device as a test function to the device. When Loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. A device is explicitly placed in Loopback mode (i.e., Loopback mode is not the normal mode of operation of a device). The method of implementing Loopback mode is not defined by this standard.

NOTE—Loopback mode may be implemented either in the parallel or the serial circuitry of a device.

127.3.3.1 Receiver considerations

A receiver may be placed in Loopback mode. Entry into or exit from Loopback mode may result in a temporary loss of synchronization.

127.3.3.2 Transmitter considerations

A transmitter may be placed in Loopback mode. While in Loopback mode, the transmitter output is not defined.

127.3.4 Test functions

A limited set of test functions may be provided as an implementation option for testing of the transmitter function or for testing of an attached receiver.

Some test functions that are not defined by this standard may be provided by certain implementations. Compliance with the standard is not affected by the provision or exclusion of such functions by an implementation. The patterns described in Annex 36A may be used for 2.5GBASE-X except the nominal bit rate is 2.5 times faster and any references to the GMII applies to the XGMII.

A typical test function is the ability to transmit invalid code-groups within an otherwise valid PHY bit stream. Certain invalid PHY bit streams may cause a receiver to lose word and/or bit synchronization. See

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ANSI INCITS 230-1994 (FC-PH), subclause 5.4, for a more detailed discussion of receiver and transmitter behavior under various test conditions.

127.3.4.1 PMA PRBS9 test pattern (optional)

The PMA may optionally generate a PRBS9 test pattern in the transmit direction.

The ability to generate the test pattern is indicated by the PRBS9_Tx_generator_ability status variable, which, if a Clause 45 MDIO is implemented, is accessible through bit 1.1500.5 (see 45.2.1.169).

If supported, when send Tx PRBS9 test-pattern mode is enabled by the PRBS9_enable and PRBS_Tx_gen_enable control variables, the PMA shall generate a PRBS9 pattern (as defined in footnote a of Table 68–6) toward the service interface below the PMA via the PMA_UNITDATA.request primitive. If a Clause 45 MDIO is implemented, the PRBS9_enable and PRBS_Tx_gen_enable control variables are accessible through bits 1.1501.6 and 1.1501.3 (see 45.2.1.170). When send Tx PRBS9 test-pattern mode is disabled, the PMA returns to normal operation.

Note that PRBS9 is intended to be checked by external test gear, and no PRBS9 checking function is provided within the PMA.

127.4 Compatibility considerations

There is no requirement for a compliant device to implement or expose any of the interfaces specified for the PCS or PMA. Implementations of a XGMII shall comply with the requirements as specified in Clause 46.

127.5 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the backplane channel and concatenation of devices.

The sum of transmit and receive delay contributed by the 2.5GBASE-X PCS and PMA shall be no more than 768 bit-times.

127.6 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 71.9.

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127.7 Protocol implementation conformance statement (PICS) proforma for Clause 127, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer for 2.5 Gb/s 8B/10B 2.5GBASE-X[219]

127.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 127, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer for 2.5 Gb/s 8B/10B 2.5GBASE-X, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

127.7.2 Identification

127.7.2.1 Implementation identification

Supplier (Note 1)	
Contact point for inquiries about the PICS (Note 1)	
Implementation Name(s) and Version(s) (Notes 1 and 3)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) (Note 2)	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

127.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 127, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer for 2.5 Gb/s 8B/10B 2.5GBASE-X
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[219]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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127.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*XGE	XGMII compatibility interface	127.1.4, Clause 46	Compatibility interface is supported	O	Yes [ ] No [ ]
MD	MDIO	Clause 45, 49.2.14	Registers and interface supported	O	Yes [ ] No [ ]
*LPI	Implementation of LPI	Clause 78		O	Yes [ ] No [ ]
LNKS	Implementation of PCS Link Status Signalling	127.2.6.6		O	Yes [ ] No [ ]

127.7.4 PICS proforma tables for the PCS and PMA sublayer, type 2.5GBASE-X

127.7.4.1 PCS

Item	Feature	Subclause	Value/Comment	Status	Support
PCS1	Word-to-Octet Synchronization	127.2.5.3		M	Yes [ ]
PCS2	A transition of a 2.5GPII idle symbol to data or error symbol	127.2.5.4	Place data or error symbol on index 0	M	Yes [ ]
PCS3	A transition of a 2.5GPII idle symbol to LPI symbol	127.2.5.4	Place LPI symbol on either index 0 or 2	M	Yes [ ]
PCS4	A transition of a 2.5GPII LPI symbol to idle symbol	127.2.5.4	Place idle symbol on either index 0 or 2	M	Yes [ ]
PCS5	Q or Fsig set start	127.2.5.4	Always occur on index 0	M	Yes [ ]
PCS6	Deficit Idle Count limits	127.2.5.4	Bounded to a min of 0, max of 3	M	Yes [ ]
PCS7	2.5GBASE-X 8B/10B requirement	127.2.6		M	Yes [ ]
PCS8	PCS Transmit Process	127.2.7.2.2	State diagrams Figure 127–5, and Figure 127–6 including compliance with variables in 127.2.7.1	M	Yes [ ]
PCS9	PCS Synchronization	127.2.7.2.3	State diagram Figure 127–7, including compliance with variables in 127.2.7.1	M	Yes [ ]
PCS10	PCS Receive Process	127.2.7.2.4	State diagrams Figure 127–8a, and Figure 127–8b including compliance with variables in 127.2.7.1	M	Yes [ ]

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127.7.4.2 Code-group functions

Item	Feature	Subclause	Value/Comment	Status	Support
CG1	Word-to-Octets process shall be synchronized to the PCS transmit process	127.2.5.3	Ordered set to be output to the PMA	M	Yes [ ]
CG2	A transition of a 2.5GPII idle symbol to a data or error symbol	127.2.5.4	Data or error symbol on index 0	M	Yes [ ]
CG3	A transition of a 2.5GPII idle symbol to a LPI symbol	127.2.5.4	LPI symbol on either index 0 or 2	M	Yes [ ]
CG4	A transition of a 2.5GPII LPI symbol to an idle symbol	127.2.5.4	Idle symbol on either index 0 or 2	M	Yes [ ]
CG5	The start of |Q| or |Fsig| set	127.2.5.4	Always occur on index 0	M	Yes [ ]
CG6	Deficit Idle Count (DIC) limits	127.2.5.4	Bounded to a min of 0, max of 3	M	Yes [ ]
CG7	2.5GBASE-X 8B/10B requirement	127.2.6		M	Yes [ ]

127.7.4.3 EEE

Item	Feature	Subclause	Value/Comment	Status	Support
EEE1	Word-to-Octet Transitions - idle to data or error	127.2.5.4	Place LP1 symbol on index 0 or 2	LPI:M	Yes [ ] N/A [ ]
EEE2	rx_tw_timer terminal count	127.2.7.1.7	Timer terminal count not to exceed TWR in Table 127–7	LPI:M	Yes [ ] N/A [ ]
EEE3	PCS Receive Process when EEE is present	127.2.7.2.4	State diagram Figure 127–8c including compliance with variables in 127.2.7.1	LPI:M	Yes [ ] N/A [ ]
EEE4	PCS that supports EEE capability	127.2.7.2.6	Implement LPI transmit process shown in Figure 127–10	LPI:M	Yes [ ] N/A [ ]

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127.7.4.4 PMA functions

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	Transmit function	127.3.2.2	Serialize 10 bits of tx_code-group	M	Yes [ ]
PMA2	Receive function	127.3.2.3	PMA assembles received rx_bits into a single ten-bit value and passes it to PCS	M	Yes [ ]
PMA3	Code-group alignment	127.3.2.4	PMA sublayer shall delete or modify ≤ 4, ten-bit code groups	M	Yes [ ]
PMA4	Loopback mode	127.3.3		M	Yes [ ]

127.7.4.5 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	XGMII	127.4, 46		XGE:M	Yes [ ] N/A [ ]
CC2	Transmit and Receive PCS/PMA delay constraints	127.5	Delay contributions by 2.5GBASE-X PCS and PMA sublayers ≤ 768 bit times	M	Yes [ ]
CC3	Environmental specifications	127.6	Conform to 71.9	M	Yes [ ]

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128. Physical Medium Dependent sublayer and baseband medium, type 2.5GBASE-KX

128.1 Overview

This clause specifies the 2.5GBASE-KX PMD and baseband medium. When forming a complete PHY, a PMD shall be combined with the appropriate sublayers (see Table 128–1), and with the management functions that are optionally accessible through the management interface defined in Clause 45. References to the MDI (Media Dependent Interface) should be considered to be TP1 for the transmitter and TP4 for the receiver, as measurement points.

Table 128–1—Physical Layer clauses associated with the 2.5GBASE-KX PMD

Associated clause	2.5GBASE-KX
46—XGMII [a]	Optional
73—Auto-Negotiation for Backplane	Required
78—EEE	Optional
127—2.5GBASE-X PCS/PMA	Required

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation behaves functionally as though the RS and XGMII were present.

A 2.5GBASE-KX PHY with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization.

128.2 Physical Medium Dependent (PMD) service interface

The following specifies the services provided by the 2.5GBASE-KX PMDs. These PMD sublayer service interfaces are described in an abstract manner and do not imply any particular implementation.

The PMD Service Interface supports the exchange of bit streams representing 2.5GBASE-X 8B/10B encoded data between the PMA and PMD entities. The PMD translates the serialized data of the PMA to and from signals suitable for the specified medium.

The following primitives are defined:

PMD_UNITDATA.request(tx_bit)
PMD_UNITDATA.indication(rx_bit)
PMD_SIGNAL.indication(SIGNAL_DETECT)

If EEE is supported, the following primitives are also defined on the PMD Service Interface:

PMD_RXQUIET.request(rx_quiet)
PMD_TXQUIET.request(tx_quiet)

These messages affect the PCS variables as described in 127.2.7.1.6.

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128.2.1 PMD_UNITDATA.request

This primitive defines the transfer of a serial data stream from the PMA to the PMD.

128.2.1.1 Semantics of the service primitive

PMD_UNITDATA.request(tx_bit)

The data conveyed by PMD_UNITDATA.request is a continuous stream of bits. The tx_bit parameter can take one of two values: ONE or ZERO.

128.2.1.2 When generated

The PMA continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at the signaling speed for 2.5GBASE-KX PMD types specified in Table 128–4.

128.2.1.3 Effect of receipt

Upon receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals on the MDI.

128.2.2 PMD_UNITDATA.indication

This primitive defines the transfer of a serial data stream from the PMD to the PMA.

128.2.2.1 Semantics of the service primitive

PMD_UNITDATA.indication(rx_bit)

The data conveyed by PMD_UNITDATA.indication is a continuous stream of bits. The rx_bit parameter can take one of two values: ONE or ZERO.

128.2.2.2 When generated

The PMD continuously sends a stream of bits to the PMA corresponding to the signals received from the MDI.

128.2.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

128.2.3 PMD_SIGNAL.indication

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

128.2.3.1 Semantics of the service primitive

PMD_SIGNAL.indication(SIGNAL_DETECT)

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting signal at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, then rx_bit is undefined, but consequent actions based on PMD_UNITDATA.indication, where necessary, interpret rx_bit as a logic ZERO.

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NOTE—SIGNAL_DETECT = OK does not guarantee that PMD_UNITDATA.indication(rx_bit) is known good. It is possible for a poor quality link to provide sufficient signal for a SIGNAL_DETECT = OK indication and still not meet the BER objective.

128.2.3.2 When generated

The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT. If the MDIO interface is implemented, then PMD_global_signal_detect shall be continuously set to the value of SIGNAL_DETECT.

128.2.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

128.2.4 PMD_RXQUIET.request

This primitive is generated by the PCS Receive Process when EEE is supported to indicate that the input signal is quiet and the PMA and PMD receiver may go into low power mode. When EEE is not supported, the primitive is never invoked, and the PMD behaves as if rx_quiet = FALSE.

128.2.4.1 Semantics of the service primitive

PMD_RXQUIET.request(rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE.

128.2.4.2 When generated

The PCS generates this primitive to request the appropriate PMD receive LPI state.

128.2.4.3 Effect of receipt

This variable is from the receive process of the PCS to control the power-saving function of the local PMD receiver. The 2.5GBASE-KX PHY receiver should put unused functional blocks into a low power state to save energy.

128.2.5 PMD_TXQUIET.request

This primitive is generated by the PCS Transmit Process when EEE is supported to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. See 128.6.5. When EEE is not supported, the primitive is never invoked, and the PMD behaves as if tx_quiet = FALSE.

128.2.5.1 Semantics of the service primitive

PMD_TXQUIET.request(tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE.

128.2.5.2 When generated

The PCS generates this primitive to request the appropriate PMD transmit LPI state.

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128.2.5.3 Effect of receipt

This primitive affects operation of the PMD Transmit disable function as described in 128.6.5. The 2.5GBASE-KX PHY transmitter should put unused functional blocks into a lower power state to save energy.

128.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD shall support the AN service interface primitive AN_LINK.indication as defined in 73.9.

128.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers consider the delay maxima, and that network planners and administrators consider the delay constraints regarding the physical topology and concatenation of devices.

The sum of transmit and receive delays contributed by the 2.5GBASE-KX PMD and medium shall be no more than 256 bit times. It is assumed that the round-trip delay through the medium is less than or equal to 80 bit times.

128.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. If the MDIO is implemented, it shall map MDIO control variables to PMD control variables as shown in Table 128–2 and MDIO status variables to PMD status variables as shown in Table 128–3.

Table 128–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
PMD Transmit Disable	1000BASE-KX/2.5GBASE-KX control register	1.160.0	PMD_transmit_disable

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Table 128–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
Transmit fault ability	1000BASE-KX/2.5GBASE-KX status register	1.161.13	PMD_Transmit_fault_ability
Receive fault ability	1000BASE-KX/2.5GBASE-KX status register	1.161.12	PMD_Receive_fault_ability
Transmit fault	1000BASE-KX/2.5GBASE-KX status register	1.161.11	PMD_transmit_fault
Receive fault	1000BASE-KX/2.5GBASE-KX status register	1.161.10	PMD_receive_fault
PMD transmit disable ability	1000BASE-KX/2.5GBASE-KX status register	1.161.8	PMD_transmit_disable_ability
Signal detect from PMD	1000BASE-KX/2.5GBASE-KX status register	1.161.0	PMD_signal_detect

128.6 PMD functional specifications

128.6.1 Link block diagram

For purposes of system conformance, the PMD sublayer is standardized at test points TP1 and TP4 as shown in Figure 128–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

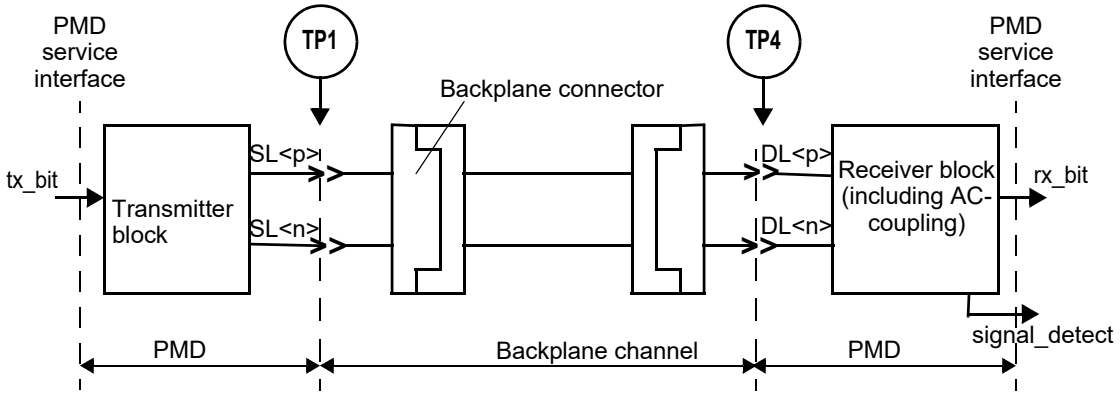

Figure 128–1—Link block diagram

The electrical path from the transmitter block to TP1, and from TP4 to the receiver block, will affect link performance and the measured values of electrical parameters used to verify conformance to this standard. Therefore, it is recommended that this path be carefully designed.

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128.6.2 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the electrical specifications in 128.7.1. A positive output voltage of SL<p> minus SL<n> (differential voltage) shall correspond to tx_bit = ONE.

128.6.3 PMD receive function

The PMD Receive function shall convey the bits received at the MDI in accordance with the electrical specifications of 128.7.2 to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). A positive input voltage of DL<p> minus DL<n> (differential voltage) shall correspond to rx_bit = ONE.

128.6.4 PMD signal detect function

For 2.5GBASE-KX operation PMD signal detect is mandatory if EEE is supported. When EEE is not supported, the PMD signal detect is optional for 2.5GBASE-KX, and its definition is beyond the scope of this specification. When PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

If EEE is supported, a local PMD signal detect function shall report to the PMD service interface using the message PMD_SIGNAL.indication(SIGNAL_DETECT). This message is signaled continuously. For EEE, the SIGNAL_DETECT parameter can take on one of two values, OK or FAIL, indicating whether the PMD is detecting electrical energy at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication is undefined. The signal energy from a compliant transmitter shall set SIGNAL_DETECT to OK within 750 ns when transitioning from LPI quiet to active and set SIGNAL_DETECT to FAIL within 750 ns when transitioning from active to LPI quiet.

128.6.5 PMD transmit disable function

The PMD_transmit_disable function is mandatory if EEE is supported and is otherwise optional. When this function is supported, it shall meet the following requirements.

a) When the PMD_transmit_disable variable is set to ONE, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum peak-to-peak differential output voltage specified in Table 128–4.
b) If a PMD_fault (128.6.7) is detected, then the PMD may turn off the electrical transmitter.
c) Loopback, as defined in 128.6.6, shall not be affected by PMD_transmit_disable.
d) For EEE capability, the PMD_transmit_disable function shall turn off the transmitter after tx_quiet is asserted within the time and voltage level specified in 128.7.1.4. The PMD_transmit_disable function shall turn on the transmitter after tx_quiet is de-asserted within a time and voltage level specified in 128.7.1.4.

128.6.6 Loopback mode

Loopback mode shall be provided for the 2.5GBASE-KX PMA/PMD by the transmitter and receiver of a device as a test function to the device. When loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. Transmitter operation shall be independent of loopback mode. The method of implementing loopback mode within the PMD is not defined by this standard.

Control of the loopback function is specified in 45.2.1.1.5.

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NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

128.6.7 PMD fault function

If the MDIO is implemented and the PMD has detected a local fault, the PMD shall set PMD_fault to ONE; otherwise, the PMD shall set PMD_fault to ZERO.

128.6.8 PMD transmit fault function

If the MDIO is implemented and the PMD has detected a local fault on the transmitter, the PMD shall set the PMD_transmit_fault variable to ONE; otherwise, the PMD shall set PMD_transmit_fault to ZERO.

128.6.9 PMD receive fault function

If the MDIO is implemented and the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to ONE; otherwise, the PMD shall set PMD_receive_fault to ZERO.

128.6.10 PMD LPI function

The PMD LPI function responds to PMD_TXQUIET and PMD_RXQUIET requests generated by the LPI transmit state diagram (See 127.2.7.2.7) and the LPI receive state diagram (see 49.2.13.3.1 and Figure 49–13). Implementation of the function is optional. EEE capabilities and parameters are advertised during the Backplane Auto-Negotiation as described in 45.2.7.16. The transmitter on the local device informs the link partner's receiver when to sleep, refresh, and wake. The local receiver's transitions are controlled by the link partner's transmitter and change independently from the local transmitter's states and transitions.

If EEE is supported, the PMD transmit function enters into a low power mode when tx_quiet is set to TRUE and exits when tx_quiet is set to FALSE. While tx_quiet is TRUE the PMD transmitter functional blocks should be deactivated to conserve energy. The PMD receive function enters into a low power mode when rx_quiet is set to TRUE and exits when rx_quiet is set to FALSE. While rx_quiet is TRUE the PMD receiver functional blocks should be deactivated to conserve energy.

The "Assert LPI" request at the XGMII is encoded in the transmitted symbols. Detection of LPI signaling in the received symbols is indicated as "Assert LPI" at the XGMII. Upon the detection of "Assert LPI" at the XGMII, an energy-efficient 2.5GBASE-KX PHY continues transmitting for a predefined period, then ceases transmission and deactivates transmit functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g., timing recovery, adaptive filter coefficients) and thereby track long-term variations in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal interframes resume at the XGMII, the PHY reactivates transmit functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the LPI mode.

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128.7 2.5GBASE-KX electrical characteristics

128.7.1 Transmitter characteristics

Transmitter characteristics at TP1 (see Figure 129–1) are summarized in Table 128–4 and detailed in 128.7.1.1 through 128.7.2.

Table 128–4—Transmitter characteristics for 2.5GBASE-KX

Parameter	Subclause reference	Value	Units
Signaling speed	128.7.1.3	3.125 ± 100 ppm	GBd
Peak-to-peak differential output voltage (max)	128.7.1.4	1200	mV
Peak-to-peak differential output voltage (min)	128.7.1.4	800	mV
Peak-to-peak differential output voltage (max) with TX disabled	128.6.5	30	mV
Common-mode voltage limits[c]	128.7.1.4	0 to +1.9	V
Differential output return loss (min)	128.7.1.5	See Equation (128–3)	dB
Common-mode output return loss (min)	128.7.1.6	See Equation (128–4)	dB
Transition time (20%–80%)	128.7.1.7	30 to 100	ps
Maximum Output jitter (peak-to-peak)			
Random jitter	128.7.1.9	0.2	UI
Deterministic jitter	128.7.1.9	0.12	UI
Duty Cycle Distortion[a]	128.7.1.9	0.035	UI
Total jitter[b]	128.7.1.9	0.32	UI

[a]Duty Cycle Distortion is considered part of deterministic jitter distribution.
[b]Jitter is specified at BER 10^{-12}.
[c]Defined with respect to signal ground as measured at Vcom in Figure 128–2.

128.7.1.1 Test fixtures

The test fixture of Figure 128–2, or its functional equivalent, is required for measuring the transmitter specifications described in 128.7.1, with the exception of return loss.

128.7.1.2 Test fixture characteristics

The differential load impedance applied to the transmitter output by the test fixture depicted in Figure 128–2 shall be 100 Ω. The differential return loss, in dB, of the test fixture shall meet the requirements of Equation (128–1) and Equation (128–2).

$$Return\_loss(f) \geq 20 \tag{128–1}$$

for 100 MHz ≤ f < 1562.5 MHz and

$$Return\_loss(f) \geq Return\_loss_{min} = 20 - 20\log_{10}\left(\frac{f}{1562.5\,\text{MHz}}\right) \tag{128–2}$$

for 1562.5 MHz ≤ f ≤ 2000 MHz.

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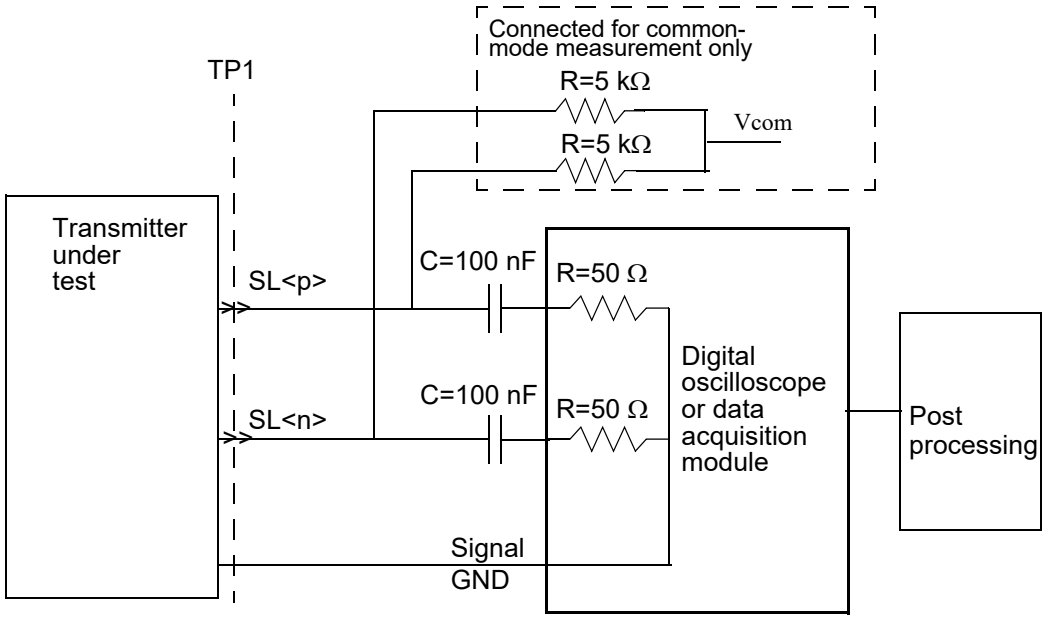

Figure 128–2—Transmit test fixture for 2.5GBASE-KX

128.7.1.3 Signaling speed

The 2.5GBASE-KX signaling speed shall be as specified in Table 128–4.

128.7.1.4 Output amplitude

The peak-to-peak differential output voltage shall be as specified in Table 128–4. See Figure 128–3. The differential output voltage test pattern is the test pattern specified in 48A.2. .

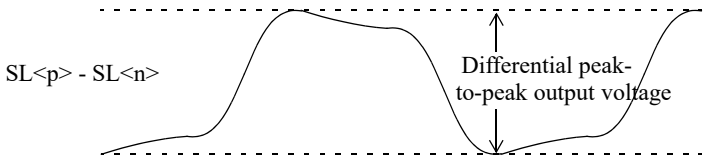

Figure 128–3—Transmitter peak-to-peak differential output voltage definition

NOTE—SL<p> and SL<n> are the positive and negative sides of the differential signal pair.

DC-referenced voltage levels are not defined since the receiver is AC-coupled. The common-mode voltage of SL<p> and SL<n>, with respect to signal ground, as measured at Vcom in Figure 128–2 is specified in Table 128–4.

For EEE capability, the transmitter shall meet the Table 128–4 requirement for Differential peak to peak output voltage when TX is disabled within 500 ns of tx_mode being set to QUIET and remain so while tx_mode is set to QUIET. Furthermore, the transmitter's peak-to-peak differential output voltage shall be greater than 720 mV within 500 ns of tx_mode being set to ALERT. The transmitter output shall be fully compliant within 5 μs after tx_mode is set to DATA. During LPI mode, the common-mode voltage shall be maintained to within ± 150 mV of the pre-LPI value.

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128.7.1.5 Differential output return loss

For frequencies from 100 MHz to 2000 MHz, the differential output return loss, in dB, of the transmitter shall meet the requirements of Table 128–4. This output impedance requirement applies to all valid output levels. The reference impedance for differential output return loss measurements shall be 100 Ω.

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 10 & 100 \leq f < 625 \\ 10 - 10\log_{10}(f/625) & 625 \leq f \leq 2000 \end{array} \right\} (\text{dB}) \quad (128\text{–}3)$$

where

f is the frequency in MHz

The minimum differential output return loss is shown in Figure 128–4.

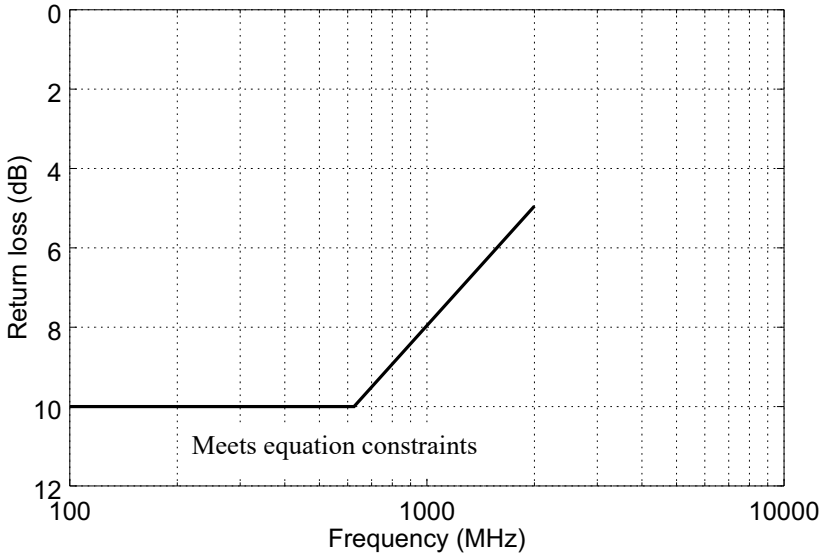

Figure 128–4—Transmitter differential-mode return loss limit

128.7.1.6 Common-mode output return loss

The transmitter common-mode return loss shall meet the requirements of Table 128–4. The reference impedance for common-mode return loss measurements is 25 Ω.

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 7 & 100 \leq f < 625 \\ 7 - 10\log_{10}(f/625) & 625 \leq f \leq 2000 \end{array} \right\} (\text{dB}) \quad (128\text{–}4)$$

where

f is the frequency in MHz

The minimum common-mode output return loss is shown in Figure 128–5.

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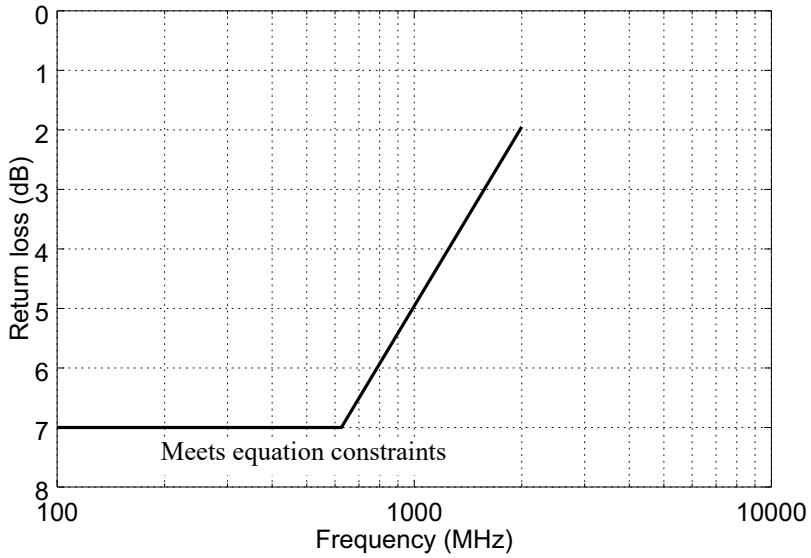

Figure 128–5—Transmitter common-mode return loss limit

128.7.1.7 Transition time

The rising and falling edge transition times shall be as specified in Table 128–4 when measured with respect to the peak-to-peak differential value of the waveform using the high-frequency test pattern of 48A.1.

128.7.1.8 Transmit jitter test requirements

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in 48B.3. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements shall be a high-frequency test pattern as defined in 48A.1. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal.

The duty cycle distortion test pattern shall be the high-frequency test pattern as defined in 48A.1.

128.7.1.9 Transmit jitter

The transmit jitter shall be as specified in Table 128–4. Duty cycle distortion (DCD) is considered a component of deterministic jitter. The peak-to-peak duty cycle distortion is defined as the absolute value of the difference in the mean pulse width of a 1 pulse or the mean pulse width of a 0 pulse (as measured at the mean of the high and low voltage levels in a repeating 0101 bit sequence) and the nominal pulse width. Jitter specifications are specified for BER = 10^{-12}. Transmit jitter test requirements are specified in 128.7.1.8.

NOTE—Duty cycle distortion (DCD) is also referred to as Even-odd jitter (see 92.8.3.8.1).

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128.7.2 Receiver characteristics

Receiver characteristics at TP4 (see Figure 129–1) are summarized in Table 128–5 and detailed in 128.7.2.1 through 128.7.2.5.

Table 128–5—Receiver characteristics for 2.5GBASE-KX

Parameter	Subclause reference	Value	Units
Bit error ratio	128.7.2.1	10^{-12}	
Signaling speed	128.7.2.2	3.125 ± 100 ppm	GBd
Differential input peak-to-peak amplitude (max)[a]	128.7.2.4	1200	mV
Differential input return loss (min)[b]	128.7.2.5	See Equation (128–3)	dB

[a]The receiver shall tolerate amplitudes up to a maximum voltage of 1200mV without permanent damage.
[b]Relative to 100 Ω differential.

128.7.2.1 Receiver interference tolerance

The receiver interference tolerance consists of the test as described in Annex 69A with the parameters specified in Table 128–6. The data pattern for the interference tolerance test shall be the test pattern as defined in 48A.5. The receiver shall satisfy the requirements for interference tolerance specified in Annex 69A for the test.

Table 128–6—2.5GBASE-KX interference tolerance parameters

Parameter	Value	Units
Target BER	10^{-12}	
m_{TC}[a] (min)	1	
Amplitude of broadband noise (min RMS)	8.1	mV
Applied transition time (20%–80%, min)	100	ps
Applied sinusoidal jitter (min peak-to-peak)	0.12	UI
Applied random jitter (min peak-to-peak)[b]	0.2	UI

[a]m_{TC} is defined in Equation (69A–6) in Annex 69A.
[b]Applied random jitter is specified at a BER of 10^{-12}.

128.7.2.2 Signaling speed range

The signaling speed of a 2.5GBASE-KX receiver shall comply with the requirements of Table 128–5.

128.7.2.3 AC-coupling

The 2.5GBASE-KX receiver shall be AC-coupled to the backplane to allow for maximum interoperability between various 2.5 Gb/s components. AC-coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC-coupling in actual implementations.

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NOTE—It is recommended that the maximum value of the coupling capacitors be limited to 100 nF. This will limit the inrush currents to the receiver that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

128.7.2.4 Input signal amplitude

2.5GBASE-KX receivers shall accept differential input signal peak-to-peak amplitudes produced by compliant transmitters connected without attenuation to the receiver, and still meet the BER requirement specified in 128.7.2.1. Note that this may be larger than the differential maximum of 128.7.1.4 due to the actual transmitter output and receiver input impedances. The input impedance of a receiver can cause the minimum signal into a receiver to differ from that measured when the receiver is replaced with a 100 Ω test load. Since the receiver is AC-coupled, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

128.7.2.5 Differential input return loss

For frequencies from 100 MHz to 2000 MHz, the differential input return loss, in dB, of the receiver shall meet the requirements of Table 128–5.

128.8 Interconnect characteristics

Informative interconnect characteristics are provided in Annex 69B.

128.9 Environmental specifications

128.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

128.9.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

128.9.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

128.9.4 Electromagnetic compatibility

A system integrating the 2.5GBASE-KX PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

128.9.5 Temperature and humidity

A system integrating the 2.5GBASE-KX PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

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128.10 Protocol implementation conformance statement (PICS) proforma for Clause 128, Physical Medium Dependent sublayer and baseband medium, type 2.5GBASE-KX[220]

128.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3, Clause 128, Physical Medium Dependent sublayer and baseband medium type 2.5GBASE-KX, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

128.10.2 Identification

128.10.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

128.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 128, Physical Medium Dependent sublayer and baseband medium type 2.5GBASE-KX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022)	
Date of Statement	

[220] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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128.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XGMII	XGMII	128.1, Clause 46	Interface is supported	O	Yes [ ] No [ ]
PCS	Support of 2.5GBASE-X PCS/PMA	128.1, 73.9		M	Yes [ ]
AN	Auto-Negotiation for Back-plane Ethernet	128.1, Clause 73	Device implements Auto-Negotiation for Backplane Ethernet	M	Yes [ ]
PCS	PCS associated with PMD supports AN service primitive AN_LINK	128.3, 73.9	Required generation of PMD primitive	M	Yes [ ]
DC	Delay Constraints	128.4	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO Capability	128.5	If MDIO is implemented, map control variables as described in 128.5	O	Yes [ ] No [ ]
*LPI	LPI	128.6.10	LPI function implemented if EEE is supported	O	Yes [ ] No [ ]
*SD	Signal Detect Generation	128.6.4	Signal detect implemented if EEE is supported	LPI:M	Yes [ ] N/A [ ]
*TD	PMD_transmit_disable	128.6.5	PMD transmit disable function implemented if EEE is supported	LPI:M	Yes [ ] N/A [ ]

128.10.4 PICS proforma tables for Clause 128, Physical Medium Dependent (PMD) sublayer and baseband medium, type 2.5GBASE-KX.

128.10.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	PMD_global_signal_detect set to the value of SIGNAL_DETECT	128.2.3.2	Required generation of PMD primitive	M	Yes [ ]
FS2	Tx+Rx delays from 2.5GBASE-KX PMD and medium ≤ 256 bit times	128.4	Required timing	M	Yes [ ]
FS3	PMD Transmit function	128.6.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FS4	PMD Transmitter signal	128.6.2	A positive differential voltage corresponds to tx_bit = ONE	M	Yes [ ]
FS5	PMD Receive function	128.6.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FS6	PMD Receiver signal	128.6.3	A positive differential voltage corresponds to rx_bit = ONE	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
FS7	PMD Signal Detect function - not implemented	128.6.4	Continuously reported OK via PMD_SIGNAL.indication (SIGNAL_DETECT).	!SD:M	Yes [ ] N/A [ ]
FS8	PMD Signal Detect during LPI - implemented	128.6.4	Report to the PMD service interface using the message PMD_SIGNAL.indication (SIGNAL_DETECT) if EEE supported	LPI:M	Yes [ ] N/A [ ]
FS9	PMD Signal Detect timing LPI quiet to active	128.6.4	Set SIGNAL_DETECT to OK within 750 ns	LPI:M	Yes[ ] N/A [ ]
FS10	PMD Signal Detect timing active to LPI quiet	128.6.4	Set SIGNAL_DETECT to FAIL within 750 ns	LPI:M	Yes [ ] N/A [ ]
FS11	Transmit Disable	128.6.5	Disables Transmitter when PMD_Transmit_disable set to ONE	TD:M	Yes [ ] N/A [ ]
FS12	Transmit Disable during LPI	128.6.5	Disable transmitter during tx_quiet	LPI:M	Yes [ ] N/A [ ]
FS13	PMD_fault	128.6.5	Transmit disabled if detected	TD:O	Yes [ ] No [ ] N/A [ ]
FS14	PMD_transmit_disable	128.6.5	Loopback function not affected	TD:M	Yes [ ] N/A [ ]
FS15	tx_quiet disabled transmitter	128.7.1	Disables Transmitter when tx_quiet is asserted as specified in 128.7.1.5	LPI:M	Yes [ ] N/A [ ]
FS16	Loopback Function	128.6.6	Loopback function provided	M	Yes [ ]
FS17	Loopback effect on Transmitter	128.6.6	Loopback function does not disable transmitter	M	Yes [ ]

128.10.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	MDIO Variable Mapping	128.5	Map MDIO variables to PMD variables as shown in Table 128–2 and Table 128–3	MD:M	Yes [ ] N/A [ ]
MF2	PMD_fault function	128.6.7	Sets PMD_fault to a logical 1 if any local fault is detected; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]
MF3	PMD_transmit_fault function	128.6.8	Sets PMD_transmit_fault to a logical 1 if any local fault is detected on the transmit path; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]
MF4	PMD_receive_fault function	128.6.9	Sets PMD_receive_fault to a logical 1 if any local fault is detected on the receive path; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]

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128.10.4.3 Transmitter electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	100 Ω differential test fixture	128.7.1.2	As shown in Figure 128–2	M	Yes [ ]
TC2	Differential return loss of test fixture	128.7.1.2	Per Equation (128–1) and Equation (128–2)	M	Yes [ ]
TC3	Signaling speed	128.7.1.3	3.125 GBd ± 100 ppm	M	Yes [ ]
TC4	Maximum transmitter differential peak-to-peak voltage	128.7.1.4	1200 mV, pk-pk, using the pattern as defined in 48A.2	M	Yes [ ]
TC5	Minimum transmitter differential peak-to-peak voltage	128.7.1.4	800 mV, pk-pk, using the pattern as defined in 48A.2	M	Yes [ ]
TC6	Maximum transmitter differential peak-to-peak voltage when TX disabled	128.6.5	30 mV, pk-pk	M	Yes [ ]
TC7	Common-mode output voltage	128.7.1.4	0V to +1.9V	M	Yes [ ]
TC8	Common-mode output return loss	128.7.1.6	Per Equation (128–3)	M	Yes [ ]
TC9	Reference Impedance	128.7.1.6	100 Ω for differential return loss measurements	M	Yes [ ]
TC10	Transmit jitter, peak-to-peak	128.7.1.8	Max TJ of 0.32 UI. Max DJ of 0.12 UI	M	Yes [ ]
TC11	Output Amplitude LPI voltage	128.7.1.4	Less than 30 mV within 500 ns of tx_mode = QUIET	LPI:M	Yes [ ] N/A [ ]
TC12	Output Amplitude ON voltage	128.7.1.4	Greater than 720 mV within 500 ns of tx_mode = ALERT	LPI:M	Yes [ ] N/A [ ]
TC13	Output to DATA compliance timing	128.7.1.4	Fully compliant ≤ 5 μsec from tx_mode = DATA	LPI:M	Yes [ ] N/A [ ]
TC14	Common-mode voltage in LPI mode	128.7.1.4	output within ±150 mV of the pre-LPI value	LPI:M	Yes [ ] N/A [ ]
TC15	Tx output waveform measurement	128.7.1.4	Measured as shown in Figure 128–3	M	Yes [ ]
TC16	Differential Output Return Loss	128.7.1.5	Equation (128–3) and Equation (128–3) at reference impedance of 100 Ω	M	Yes [ ]
TC17	TX common-mode return loss	48A.1	Equation (128–4)	M	Yes [ ]
TC18	TX rise time and fall time	128.7.1.7	30 ps to 100 ps, 20%/80% of peak-to-peak differential with pattern in 48A.1	M	Yes [ ]
TC19	Jitter test pattern	128.7.1.8	See pattern definition in 128.7.1.8	M	Yes [ ]
TC20	DCD test pattern	128.7.1.8	See pattern definition in 128.7.1.8	M	Yes [ ]
TC21	TX jitter limit	128.7.1.9	≤ 0.32 UI, peak-to-peak	M	Yes [ ]
TC22	TX DCD limit	128.7.1.9	≤ 0.035 UI, peak-to-peak	M	Yes [ ]

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128.10.4.4 Receiver electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Receiver interference tolerance measurement method	128.7.2.1	Per Annex 69A with parameters specified in Table 128–6	M	Yes [ ]
RC2	Receiver interference tolerance test pattern	128.7.2.1	test patterns 2 or 3 as defined in 48A.4	M	Yes [ ]
RC3	Receiver interference tolerance requirements	128.7.2.1	Satisfy requirements per Annex 69A	M	Yes [ ]
RC4	Input signaling speed in the range of 3.125 GBd ± 100 ppm	128.7.2.2	Receiver meets requirements of Table 128–5	M	Yes [ ]
RC5	Receiver coupling	128.7.2.3	AC-coupled	M	Yes [ ]
RC6	Input signal amplitude	128.7.2.4	BER still met when compliant transmitter is connected with no attenuation	M	Yes [ ]
RC7	Differential input return loss	128.7.2.5	Per Equation (128–3)	M	Yes [ ]
RC8	Reference Impedance	128.7.2.5	100 Ω for differential return loss measurements	M	Yes [ ]

128.10.4.5 Environmental and safety specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	128.9.1	Conforms to J.2	M	Yes [ ]
ES2	Electromagnetic compatibility	128.9.4	Comply with applicable local and national codes	M	Yes [ ]

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129. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer for 5 Gb/s 64B/66B, type 5GBASE-R

129.1 Overview

129.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) Sublayer that is common to a family of 5 Gb/s Physical Layer implementations, known as 5GBASE-R. The 5GBASE-R PCS and 5GBASE-R PMA are sublayers of the 5 Gb/s BASE-R PHY listed in Table 125–1. The term 5GBASE-R is used when referring generally to Physical Layers using the PCS and PMA defined in this clause.

129.1.2 Relationship of 5GBASE-R to other standards

Figure 125–1 depicts the relationships among the 5GBASE-R sublayers, the Ethernet MAC and reconciliation layers, and the higher layers. The 5GBASE-R service interface is the XGMII, which is defined in Clause 46.

The 5GBASE-R PCS is identical to the 10GBASE-R PCS specified in Clause 49 with the exception that the BER Monitor process asserts hi_ber if ber_cnt reaches 16 in a 250 μs period. This differs from the definition in 49.2.13.3 where it asserts hi_ber if ber_cnt reaches 16 in a 125 μs period.

The purpose of the serial PMA is to attach the PMD of choice to its client. The PMA service interface is defined in an abstract manner and does not imply any particular implementation. The nominal bit rate of the PMA is 5.15625 Gb/s.

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129.1.3 Summary of 5GBASE-R sublayers

Figure 129–1 depicts the relationship between the 5GBASE-R PCS and its associated sublayers.

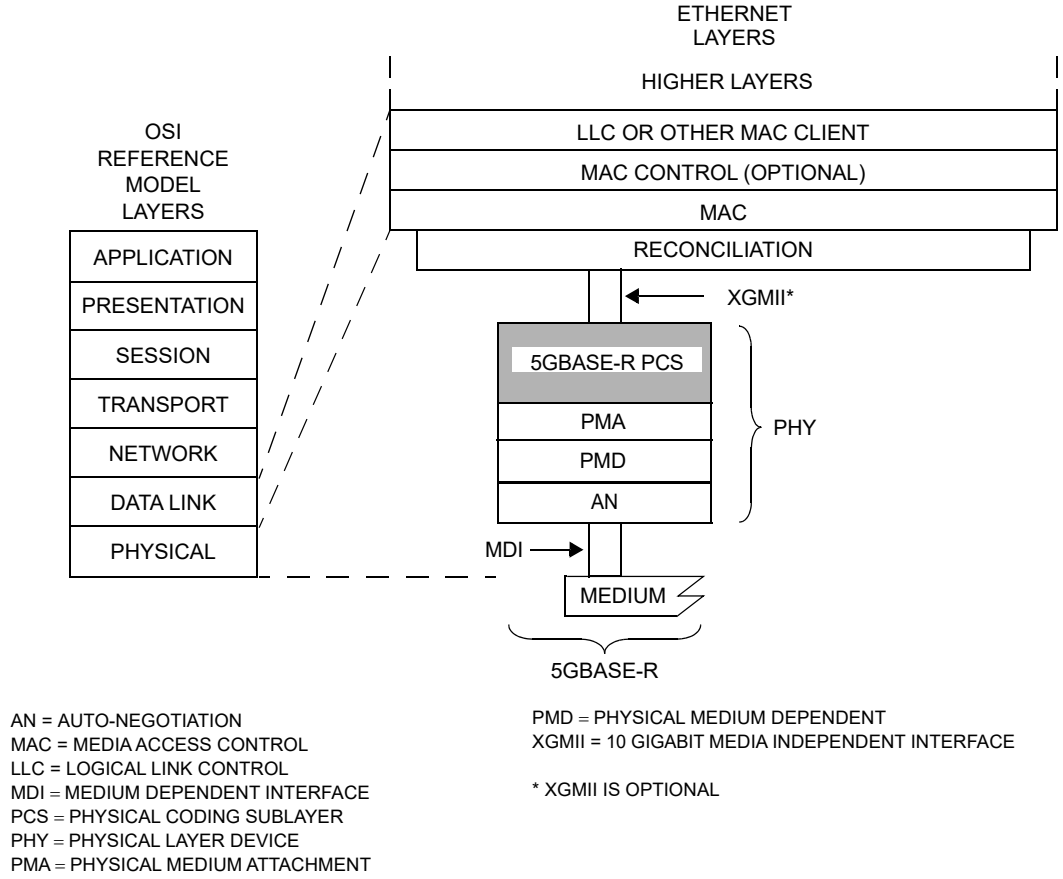

Figure 129–1—5GBASE-R PCS and PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

129.1.3.1 Physical Coding Sublayer (PCS)

The PCS service interface is the XGMII, which is defined in Clause 46 operating at 5 Gb/s. The 5GBASE-R PCS provides all services required by the XGMII, including encoding (decoding) of eight XGMII data octets to (from) 66-bit blocks (64B/66B) for communication with the underlying PMA.

129.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS to support the use of serial-bit oriented physical media. The 5GBASE-R PMA performs the following functions:

In the transmit direction (i.e., transmitting data from the PMA client to the PMD), the PMA performs the following functions:

a) Provide transmit source clock to PMA client
b) Serialization of 16-bit data to serial bit stream.
c) Transmission of serial data to PMD.

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In the receive direction (i.e., serial data from PMD to the PMA client), the PMA performs the following functions:

a1) Bit clock recovery of serial data from PMD.
b1) Provide receive clock to PMA client.
c1) Deserialization of serial data to16-bit parallel data.
d1) Transmission of parallel data to PMA client.
e1) Provide link status information.

129.1.4 Inter-sublayer interfaces

There are a number of interfaces employed by 5GBASE-R. Some (such as the PMA service interface) use an abstract service model to define the operation of the interface. The PCS service interface is the XGMII running at 5 Gb/s that is defined in Clause 46. The XGMII has an optional physical instantiation.

The upper interface of the PCS may connect to the Reconciliation Sublayer through the XGMII. The lower interface of the PCS connects to the PMA sublayer to support a 5GBASE-KR PMD. The nominal rate of the PMA service interface is 322.265625 Mtransfers/s, which provides capacity for the MAC data rate of 5 Gb/s.

The nominal rate of the PMD service interface is 5.15625 Gb/s.

If the optional Energy-Efficient Ethernet (EEE) capability is supported (see Clause 78, 78.3), then the interface with the PMA sublayer includes rx_mode and tx_mode to control power states in lower sublayers and energy_detect that indicates whether the PMD sublayer has detected a signal at the receiver.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

129.2 Physical Coding Sublayer (PCS)

129.2.1 Functions within the PCS

The 5GBASE-R PCS shall have all the functionality of the 10GBASE-R PCS specified in Clause 49.

The BER monitor state diagram shown in Figure 49–15 applies but the definition of “ber_cnt” in 49.2.13.2.4 is replaced with “Count up to a maximum of 16 of the number of invalid sync headers within the current 250 μs period.” and the ber_cnt definition in 49.2.14.2 is similarly modified.

The PCS encodes data and control information into 66-bit blocks. The relationship of block bit positions to the XGMII, PMA, and other PCS constructs is illustrated in Figure 129–2 for transmit and Figure 129–3 for receive (see figures in 129.2.3).

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129.2.2 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

Two consecutive XGMII transfers provide eight characters that are encoded into one 66-bit transmission block.

129.2.3 Transmission order

Block bit transmission order is illustrated in Figure 129–2 and Figure 129–3. These figures show the mapping from XGMII to 64B/66B block for a block containing eight data characters.

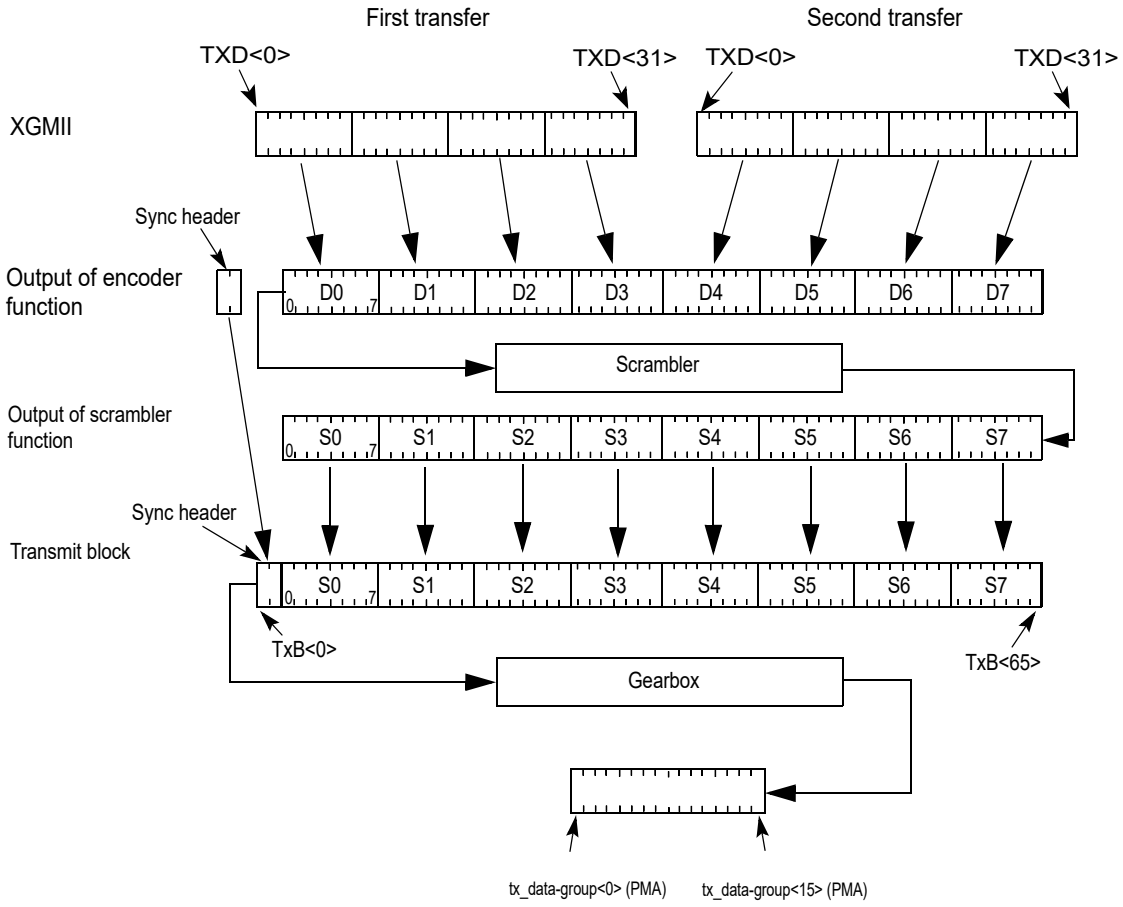

Figure 129–2—PCS Transmit bit ordering

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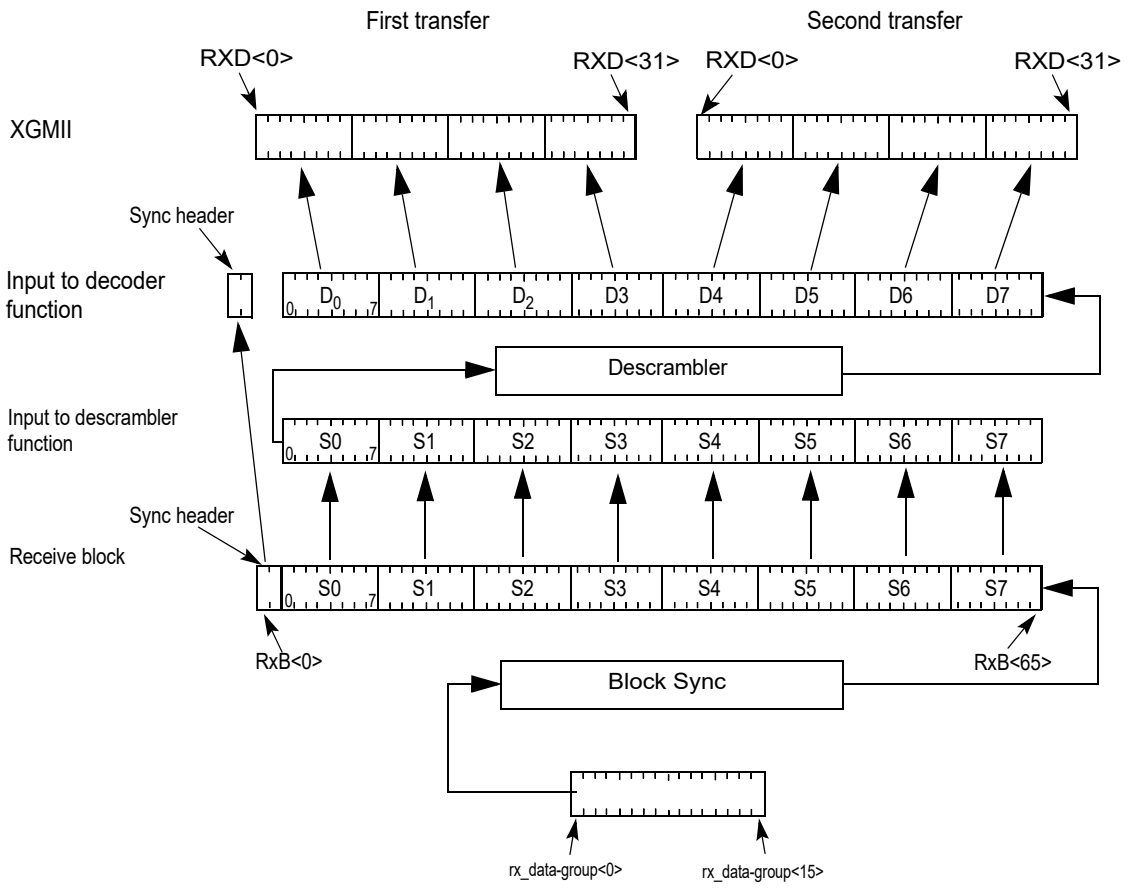

Figure 129–3—PCS Receive bit ordering

129.2.4 Low Power Idle

If the 5GBASE-KR PCS is a part of a PHY configured for EEE operation, the PCS shall follow the state diagrams specified in Figure 49–12 and Figure 49–13.

The LPI functions shall use timer values for these state diagrams as shown in Table 129–1 for transmit and Table 129–2 for receive.

Table 129–1—Transmitter LPI timing parameters

Parameter	Description	Min	Max	Units
T_{SL}	Local Sleep Time from entering the TX_SLEEP state to when tx_mode is set to QUIET	4.9	5.1	µs
T_{QL}	Local Quiet Time from when tx_mode is set to QUIET to entry into the TX_ALERT state	1.7	1.8	ms
T_{WL}	Time spent in the TX_WAKE state	10.9	11.1	µs
T_{1U}	Time spent in the TX_ALERT and TX_SCR_BYPASS states	1.1	1.3	µs

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Table 129–2—Receiver LPI timing parameters

Parameter	Description	Min	Max	Units
T_{QR}	The time the receiver waits for energy_detect to be set to TRUE while in the RX_SLEEP and RX_QUIET states before asserting receive fault	2	3	ms
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault (when scr_bypass_enable = FALSE)	—	11.5	μs
T_{WR}	Time the receiver waits in the RX_WAKE state before indicating a wake time fault (when scr_bypass_enable = TRUE)	—	13.7	μs
T_{WTF}	Wake time fault recovery time	—	10	ms

129.2.5 PCS used with 5GBASE-KR PMD

The following requirements apply to a PCS used with a 5GBASE-KR PMD. Support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

129.3 Physical Medium Attachment (PMA) sublayer

129.3.1 Service Interface

The Serial PMA provides a Service Interface to the 5G BASE-R PCS. These services are described in an abstract manner and do not imply any particular implementation. The PMA Service Interface shall support the exchange of data-groups between the PMA and the PMA client. The PMA converts data-groups into bits and passes these to the PMD, and vice versa. It also generates an additional status indication for use by its client.

The following primitives are defined:

PMA_UNITDATA.request(tx_data-group<15:0>)
PMA_UNITDATA.indication (rx_data-group<15:0>)
PMA_SIGNAL.indication(SIGNAL_OK)
PMA_RXMODE.request(rx_mode)
PMA_TXMODE.request(tx_mode)
PMA_ENERGY.indication(energy_detect)

The definitions of these primitives are found in 51.2.

129.3.2 Functions within the PMA

The PMA comprises the PMA Transmit and PMA Receive processes for 5GBASE-R. The PMA Transmit process serializes the tx_data-groups and passes them to the PMD for transmission on the underlying medium. Similarly, the PMA Receive process deserializes received data from the PMD and presents the data as rx_data-groups to the PMA client. The PMA receiver continuously conveys 16-bit data-groups to the PMA client, independent of data-group alignment.

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129.3.2.1 PMA transmit function

The PMA Transmit function passes data unaltered (except for serializing) from the PMA client directly to the PMD. Upon receipt of a PMA_UNITDATA.request primitive, the PMA Transmit function shall serialize the 16 bits of the tx_data-group<15:0> parameter and transmit them to the PMD in the form of 16 successive PMD_UNITDATA.request primitives.

129.3.2.2 PMA receive function

The PMA Receive function passes data unaltered from the PMD directly to the PMA client. Upon receipt of 16 successive PMD_UNITDATA.indication primitives, the PMA shall assemble the 16 received bits into a single 16-bit value and pass that value to the PMA client as the rx_data-group<15:0> parameter of the primitive PMA_UNITDATA.indication. The PMA receive function does not align rx_datagroup<15:0> to the original tx_data-group<15:0> from the remote end of the link.

129.3.3 PMA loopback mode (optional)

PMA loopback is optional. If PMA loopback is implemented, it shall conform to the requirements of 51.8.

129.4 Compatibility considerations

There is no requirement for a compliant device to implement or expose any of the interfaces specified for the PCS or PMA. Implementations of a XGMII shall comply with the requirements as specified in Clause 46.

129.5 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of transmit and receive delay contributed by the 5GBASE-R PCS and PMA shall be no more than 3584 bit-times.

129.6 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 51.9.

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129.7 Protocol implementation conformance statement (PICS) proforma for Clause 129, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer for 5 Gb/s 64B/66B, type 5GBASE-R [221]

129.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 129, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer for 5 Gb/s 64B/66B, type 5GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

129.7.2 Identification

129.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

129.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 129, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer for 5 Gb/s 64B/66B, type 5GBASE-R.
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[221] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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129.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XGE	XGMII compatibility interface	129.1.4	Compatibility interface is supported	O	Yes [ ] No [ ]
*MD	MDIO	Clause 45, 49.2.14	Registers and interface supported	O	Yes [ ] No [ ]
PCS	5GBASE-R PCS	129.2.1, 49	Support PCS in Clause 49 as modified in 129.2.1	M	Yes [ ]
BER	BER Monitor test counter	129.2.1, 49	ber_cnt of 16 in a period of 250 µs	M	Yes [ ]
*LPI	Implementation of LPI	Clause 78		O	Yes [ ] No [ ]

129.7.4 PICS Proforma Tables for PCS, type 5GBASE-R

129.7.4.1 Coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder implements the code as specified	49.2.13.2.3 and 49.2.4		M	Yes [ ]
C2	Decoder implements the code as specified	49.2.13.2.3 and 49.2.4		M	Yes [ ]
C3	IDLE control code insertion and deletion	49.2.4.7	Insertion or Deletion in groups of 4 /I/s	M	Yes [ ]
C4	IDLE control code deletion	49.2.4.7	When deleting /I/s, the first four characters after a /T/ shall not be deleted.	M	Yes [ ]
C5	Sequence ordered set deletion	49.2.4.10	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ]

129.7.4.2 Scrambler and Descrambler

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Scrambler	49.2.6	Performs as shown in Figure 49–8	M	Yes [ ]
S2	Descrambler	49.2.10	Performs as shown in Figure 49–10	M	Yes [ ]

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129.7.5 Test-pattern modes

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Square wave and pseudo-random transmit test-pattern generators are implemented	49.2.8	Performs as in 49.2.8	M	Yes [ ]
JT2	Pseudo-random receive test-pattern checker is implemented	49.2.12	Performs as in 49.2.12	M	Yes [ ]
*JT3	Support for PRBS31 test pattern	49.2.8		O	Yes [ ] No [ ]
JT4	PRBS31 test-pattern generator is implemented	49.2.8	Performs as in 49.2.8	JT3:M	Yes [ ] N/A[ ]
JT5	PRBS31 test-pattern checker is implemented	49.2.12	Performs as in 49.2.12	JT3:M	Yes [ ] N/A[ ]
*JT6	Support for PRBS9 transmit test pattern	49.2.8		O	Yes [ ] No [ ]
JT7	PRBS9 transmit test pattern is implemented	49.2.8	Performs as in 49.2.8	JT6:M	Yes [ ] N/A[ ]

129.7.5.1 Bit order

Item	Feature	Subclause	Value/Comment	Status	Support
B1	Transmit bit order	49.2.7	Placement of bits into tx_data-group<15:0> as specified in 49.2.7	M	Yes [ ]
B2	Receive bit order	49.2.9	Placement of bits from rx_data-group<15:0> into blocks as specified in 49.2.9	M	Yes [ ]

129.7.6 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Equivalent access to PCS Management objects is provided	49.2.14		!MD:O	Yes [ ] No [ ] N/A [ ]

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129.7.6.1 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Lock	49.2.13.3	Meets the requirements of Figure 49–14	M	Yes [ ]
SM2	BER Monitor	49.2.13.3	Meets the requirements of Figure 49–15	M	Yes [ ]
SM3	Transmit	49.2.13.3	Meets the requirements of Figure 49–16	M	Yes [ ]
SM4	Receive	49.2.13.3	Meets the requirements of Figure 49–17	M	Yes [ ]

129.7.6.2 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
LB1	PMA Loopback	129.3.3	Conform to the requirements of 51.8	O	Yes [ ] No [ ]

129.7.6.3 Delay Constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS Delay Constraint	49.2.15	No more than 3584 BT for sum of transmit and receive path delays	M	Yes [ ]

129.7.6.4 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
AN1	Support for use with a 5GBASE-KR PMD	49.2.16	AN technology dependent interface described in Clause 73	M	Yes [ ]
AN2	AN_LINK.indication primitive	49.2.16 and 129.2.5	Support of the primitive AN_LINK.indication(link_status), when the PCS is used with 5GBASE-KR PMD. Primitive generated when link_status changes.	M	Yes [ ]
AN3	link_status parameter	49.2.16 and 129.2.5	Takes the value OK or FAIL, as described in 49.2.16	M	Yes [ ]
AN4	Generation of AN_LINK.indication primitive	49.2.16 and 129.2.5	Generated when the value of link_status changes	M	Yes [ ]

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129.7.6.5 LPI functions

Item	Feature	Subclause	Value/Comment	Status	Support
LP1	Insertion and deletion of LPIs in groups of four	49.2.4.7		LPI:M	Yes [ ] N/A [ ]
LP2	Unscrambled data transmitted when scrambler_bypass = TRUE	49.2.6		LPI:M	Yes [ ] N/A [ ]
LP3	Scrambler continues to operate as normal when scrambler_bypass = TRUE	49.2.6		LPI:M	Yes [ ] N/A [ ]
LP4	Transmit state diagrams	49.2.13.3	Support additions to Figure 49–16 for EEE capability	LPI:M	Yes [ ] N/A [ ]
LP5	Receive state diagrams	49.2.13.3	Support additions to Figure 49–17 for EEE capability	LPI:M	Yes [ ] N/A [ ]
LP6	LPI transmit state diagrams	49.2.13.3.1	Meets the requirements of Figure 49–12	LPI:M	Yes [ ] N/A [ ]
LP7	LPI receive state diagrams	49.2.13.3.1	Meets the requirements of Figure 49–13	LPI:M	Yes [ ] N/A [ ]
LP8	LPI transmit timing	129.2.4, 49.2.13.3.1	Meets the requirements of Table 129–1 instead of Table 49–2	LPI:M	Yes [ ] N/A [ ]
LP9	LPI receive timing	129.2.4, 49.2.13.3.1	Meets the requirements of Table 129–2 instead of Table 49–3	LPI:M	Yes [ ] N/A [ ]

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130. Physical Medium Dependent sublayer and baseband medium, type 5GBASE-KR

130.1 Overview

This clause specifies the 5GBASE-KR PMD and the baseband medium. When forming a complete PHY, a PMD shall be connected to the appropriate sublayers (see Table 130–1), and with the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent. References to the MDI (Media Dependent Interface) should be considered to be TP1 for the transmitter and TP4 for the receiver, as measurement points.

Table 130–1—Physical Layer clauses associated with the 5GBASE-KR PMD

Associated clause	5GBASE-KR
46—XGMII[a]	Optional
73—Auto Negotiation for Backplane	Required
78—EEE	Optional
129—PCS and PMA for 64B/66B	Required

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation behaves functionally as though the RS and XGMII were present.

A 5GBASE-KR PHY with the optional Energy-Efficient Ethernet (EEE) capability may optionally enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization.

130.2 Physical Medium Dependent (PMD) service interface

The following specifies the services provided by the 5GBASE-KR PMDs. These PMD sublayer service interfaces are described in an abstract manner and do not imply any particular implementation.

The PMD Service Interface supports the exchange of encoded and scrambled 64B/66B blocks between the PMA and PMD entities. The PMD translates the serialized data of the PMA to and from signals suitable for the specified medium.

The following primitives are defined:

PMD_UNITDATA.request(tx_bit)
PMD_UNITDATA.indication(rx_bit)
PMD_SIGNAL.indication(SIGNAL_DETECT)

If EEE is supported, the following primitives are also defined on the PMD Service Interface:

PMD_RX_MODE.request(rx_mode)
PMD_TX_MODE.request(tx_mode)

These messages affect the PCS variables as described in 49.2.13.2.2.

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130.2.1 PMD_UNITDATA.request

This primitive defines the transfer of a serial data stream from the PMA to the PMD.

130.2.1.1 Semantics of the service primitive

PMD_UNITDATA.request(tx_bit)

The data conveyed by PMD_UNITDATA.request is a continuous stream of bits. The tx_bit parameter can take one of two values: ONE or ZERO.

130.2.1.2 When generated

The PMA continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at the signaling speed specified in Table 130–4 for 5GBASE-KR PMD types.

130.2.1.3 Effect of receipt

Upon receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals on the MDI.

130.2.2 PMD_UNITDATA.indication

This primitive defines the transfer of data (in the form of serialized data) from the PMD to the PMA.

130.2.2.1 Semantics of the service primitive

PMD_UNITDATA.indication(rx_bit)

The data conveyed by PMD_UNITDATA.indication is a continuous stream of bits. The rx_bit parameter can take one of two values: ONE or ZERO.

130.2.2.2 When generated

The PMD continuously sends a stream of bits to the PMA corresponding to the signals received from the MDI.

130.2.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

130.2.3 PMD_SIGNAL.indication

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

130.2.3.1 Semantics of the service primitive

PMD_SIGNAL.indication(SIGNAL_DETECT)

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting signal at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication(rx_bit) is undefined.

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NOTE—SIGNAL_DETECT = OK does not guarantee that PMD_UNITDATA.indication(rx_bit) is known good. It is possible for a poor quality link to provide sufficient signal for a SIGNAL_DETECT = OK indication and still not meet the BER objective.

130.2.3.2 When generated

The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT. If the MDIO interface is implemented, then PMD_global_signal_detect shall be continuously set to the value of SIGNAL_DETECT.

130.2.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

130.2.4 PMD_RX_MODE.request

This primitive is generated by the PCS Receive Process when EEE is supported to indicate that the input signal is quiet and the PMA and PMD receiver may go into a low power mode. When EEE is not supported, the primitive is never invoked, and the PMD behaves as if rx_mode = DATA.

130.2.4.1 Semantics of the service primitive

PMD_RX_MODE.request(rx_mode)

The rx_mode parameter takes on one of two values: QUIET or DATA.

130.2.4.2 When generated

The PCS generates this primitive to request the appropriate PMD receive LPI state.

130.2.4.3 Effect of receipt

When rx_mode is QUIET, the PMD receive function may deactivate functional blocks to conserve energy. When rx_mode is DATA, the PMD receive function operates normally.

130.2.5 PMD_TX_MODE.request

This primitive is generated by the PCS Transmit Process when EEE is supported to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. See 130.6.5. When EEE is not supported, the primitive is never invoked, and the PMD behaves as if tx_mode = DATA.

130.2.5.1 Semantics of the service primitive

PMD_TX_MODE.request(tx_mode)

The tx_mode parameter takes on one of three values: QUIET, ALERT, or DATA.

130.2.5.2 When generated

The PCS generates this primitive to request appropriate PMD transmit LPI state.

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130.2.5.3 Effect of receipt

When tx_mode is QUIET, the PMD Transmit function may deactivate functional blocks to conserve energy. When tx_mode is ALERT, the PMD Transmit function transmits the alert pattern. When tx_mode is DATA, the PMD Transmit function operates normally.

130.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD shall support the AN service interface primitive AN_LINK.indication defined in 73.9.

130.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers consider the delay maxima, and that network planners and administrators consider the delay constraints regarding concatenation of devices.

The sum of the transmit and the receive delays contributed by the 5GBASE-KR PMD and medium shall be no more than 512 bit times. It is assumed that the round-trip delay through the medium is 80 bit times.

130.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control variables to PMD control variables as shown in Table 130–2 and MDIO status variables to PMD status variables as shown in Table 130–3.

Table 130–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
Global PMD Transmit Disable	Transmit disable register	1.9.0	Global_PMD_transmit_disable

Table 130–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD Receive signal detect	Receive signal detect register	1.10.0	Global_PMD_signal_detect

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130.6 PMD functional specifications

130.6.1 Link block diagram

For purposes of system conformance, the PMD sublayer is standardized at test points TP1 and TP4 as shown in Figure 130–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

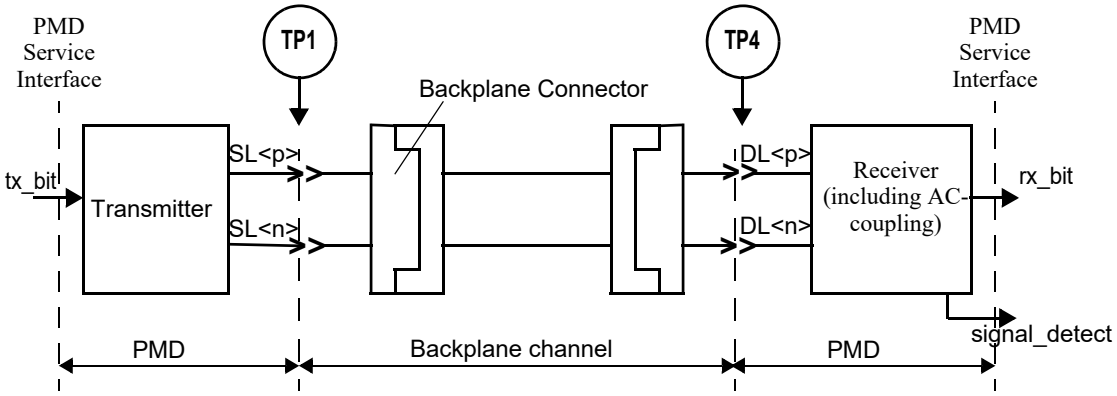

Figure 130–1—Link block diagram

The electrical path from the transmitter block to TP1, and from TP4 to the receiver block, will affect link performance and the measured values of electrical parameters used to verify conformance to this standard. Therefore, it is recommended that this path be carefully designed.

130.6.2 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the specifications in this clause. A positive output voltage of SL<p> minus SL<n> (differential voltage) shall correspond to tx_bit = ONE.

If the optional Energy-Efficient Ethernet (EEE) capability is supported (see Clause 78), then when tx_mode is set to ALERT, the PMD shall transmit a repeating 16-bit pattern, hexadecimal 0xFF00.

130.6.3 PMD receive function

The PMD Receive function shall convey the bits received from the MDI according to the electrical specifications in this clause to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). A positive input voltage of DL<p> minus DL<n> (differential voltage) shall correspond to rx_bit = ONE.

130.6.4 PMD signal detect function

The Global_PMD_signal_detect function reports to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indication is used by 5GBASE-R PHYs as an indicator of valid signal presence. SIGNAL_DETECT shall be set to FAIL following system reset.

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When the PMD signal detect function is implemented, its definition is beyond the scope of this specification. When PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive. PMD signal detect is mandatory if EEE is supported.

When the PHY supports the optional EEE capability, PMD_SIGNAL.indication is used to indicate when the ALERT signal is detected, which corresponds to the beginning of a refresh or a wake. If the MDIO interface is implemented, then Global_PMD_signal_detect (1.10.0) shall be continuously set to the value of SIGNAL_DETECT as described in 45.2.1.9.7.

When the PHY supports the EEE capability, SIGNAL_DETECT is set to FAIL following a transition from rx_mode = DATA to rx_mode = QUIET. When rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input that is the output of a channel that satisfies the requirements of all the parameters of both interference tolerance test channels defined in 130.7.2.1 when driven by a square wave pattern with a period of 16 unit intervals and peak-to-peak differential output amplitude of 720 mV. While rx_mode = QUIET, SIGNAL_DETECT changes from FAIL to OK only after a valid ALERT signal is applied to the channel.

SIGNAL_DETECT shall be set to FAIL following system reset.

130.6.5 PMD transmit disable function

The Global_PMD_transmit_disable function is mandatory if EEE is supported and is otherwise optional. When this function is supported, it shall meet the following requirements:

a) When the Global_PMD_transmit_disable variable is set to ONE, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum peak-to-peak differential output voltage specified in Table 130–4.
b) If a PMD_fault (130.6.7) is detected, then the PMD may turn off the electrical transmitter.
c) Loopback, as defined in 130.6.6, shall not be affected by Global_PMD_transmit_disable.
d) For EEE capability, the PMD_transmit_disable function shall turn off the transmitter after tx_mode is set to QUIET within a time and voltage level specified in 130.7.1.4. The PMD_transmit_disable function shall turn on the transmitter after tx_mode is set to DATA or ALERT within the time and voltage level specified in 130.7.1.4.

If the MDIO interface is implemented, then this function shall map to the Global_PMD_transmit_disable bit as specified in 45.2.1.8.7.

130.6.6 Loopback mode

Loopback mode shall be provided for the 5GBASE-KR PMD by the transmitter and receiver of a device as a test function to the device. When loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. This bit does not affect the state of the transmitter. The method of implementing loopback mode within the PMD is not defined by this standard.

Control of the loopback function is specified in 45.2.1.1.5.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

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130.6.7 PMD_fault function

If the MDIO is implemented, PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault.

130.6.8 PMD transmit fault function

The PMD_transmit_fault function is optional. The faults detected by this function are implementation specific, but should not include the assertion of the Global_PMD_transmit_disable function.

If a PMD_transmit_fault (optional) is detected, then the Global_PMD_transmit_disable function should also be asserted.

If the MDIO interface is implemented, then this function shall be mapped to the PMD_transmit_fault bit as specified in 45.2.1.7.4.

130.6.9 PMD receive fault function

The PMD_receive_fault function is optional. The faults detected by this function are implementation specific.

If the MDIO interface is implemented, then this function shall contribute to PMA/PMD receive fault bit as specified in 45.2.1.7.5.

130.6.10 PMD LPI function

The PMD LPI function responds to the transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD_TX_MODE and PMD_RX_MODE requests. Implementation of the function is optional. The PMD LPI function responds to the transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD_TX_MODE and PMD_RX_MODE requests. Implementation of the function is optional. EEE capabilities and parameters will be advertised during the Backplane Auto-negotiation, as described in 45.2.7.16. The transmitter on the local device will inform the link partner's receiver when to sleep, refresh and wake. The local receiver transitions are controlled by the link partner's transmitter and can change independent of the local transmitter states and transitions.

The “Assert LPI” request at the XGMII is encoded in the transmitted symbols. Detection of LPI signaling in the received symbols is indicated as “Assert LPI” at the XGMII. Upon the detection of “Assert LPI” at the XGMII, an energy-efficient 5GBASE-KR PHY continues transmitting for a predefined period, then ceases transmission and deactivates transmit functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g., timing recovery, adaptive filter coefficients) and thereby track long-term variations in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal interframes resume at the XGMII, the PHY reactivates transmit functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the LPI mode.

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130.7 5GBASE-KR electrical characteristics

130.7.1 Transmitter characteristics

Transmitter characteristics at TP1 (see Figure 130–1) are summarized in Table 130–4 and detailed in 130.7.1.1 through 130.7.1.10.

Table 130–4—Transmitter characteristics for 5GBASE-KR

Parameter	Subclause reference	Value	Units
Signaling speed	130.7.1.3	5.15625 ± 100 ppm	GBd
Peak-to-peak differential output voltage (max)	130.7.1.4	1200	mV
Peak-to-peak differential output voltage (min)	130.7.1.4	800	mV
Peak-to-peak differential output voltage (max) with TX disabled	130.6.5	30	mV
Pre-cursor equalization ratio (R_{pre})	130.7.1.10	1.25 ± 0.05	
Common-mode voltage limits[c]	130.7.1.4	0 to +1.9	V
Common-mode voltage deviation (max) during LPI	130.7.1.4	150	mV
Differential output return loss (min)	130.7.1.5	See Equation (130–3) and Equation (130–4)	dB
Common-mode output return loss (min)	130.7.1.6	See Equation (130–5) and Equation (130–6)	dB
Transition time (20%–80%)	130.7.1.7	20 to 60	ps
Max output jitter (peak-to-peak) Random jitter[a] Deterministic jitter Duty Cycle Distortion[b] Total jitter	 130.7.1.9 130.7.1.9 130.7.1.9 130.7.1.9	 0.15 0.12 0.035 0.27	 UI UI UI UI

[a]Jitter is specified at BER 10^{-12}.
[b]Duty Cycle Distortion is considered part of the deterministic jitter distribution.
[c]Defined with respect to signal ground as measured at Vcom in Figure 130–2.

130.7.1.1 Test fixture

The test fixture of Figure 130–2, or its functional equivalent, is required for measuring the transmitter specifications described in 130.7.1, with the exception of return loss.

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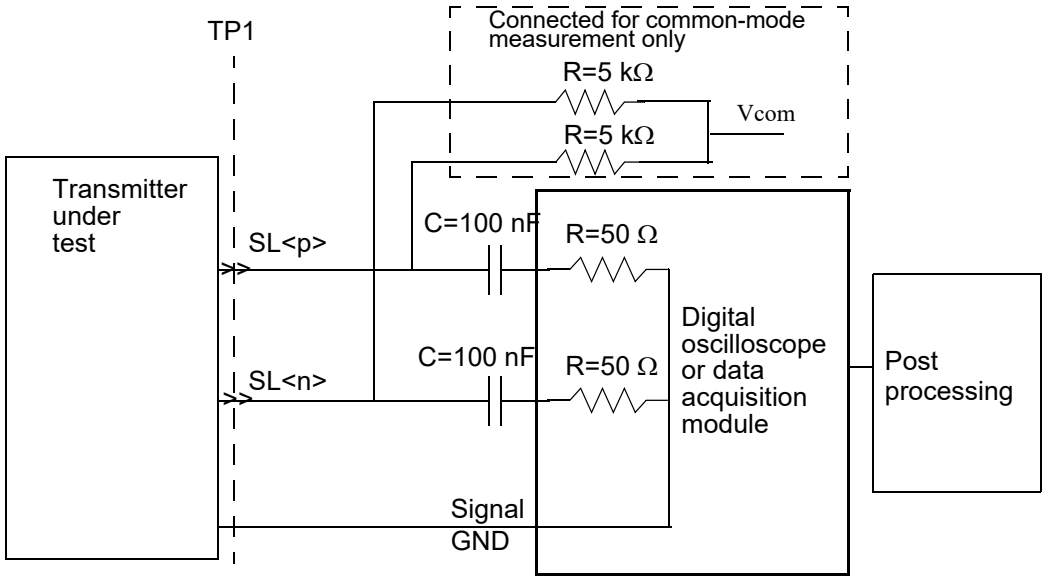

Figure 130–2—Transmit test fixture for 5GBASE-KR

130.7.1.2 Test fixture characteristics

The differential load impedance applied to the transmitter output by the test fixture depicted in Figure 130–2 shall be 100 Ω. The differential return loss, in dB, of the test fixture shall meet the requirements of Equation (130–1) and Equation (130–2).

$$Return\_loss(f) \geq 20 \tag{130–1}$$

for 100 MHz ≤ f < 2579 MHz

$$Return\_loss(f) \geq Return\_loss_{min} = 20 - 26.55\log_{10}\left(\frac{f}{2579\text{MHz}}\right) \tag{130–2}$$

for 2579 MHz ≤ f ≤ 5156.25 MHz

130.7.1.3 Signaling speed

The 5GBASE-KR signaling speed shall be as specified in Table 130–4.

130.7.1.4 Output amplitude

The differential output voltage is constrained via the transmitter output waveform requirements specified in 130.7.1.10. The peak-to-peak differential output voltage shall be as specified in Table 130–4. See Figure 130–3. The differential output voltage test pattern is the square wave test pattern defined in 52.9.1.2, with a run of at least eight consecutive ones followed by an equal number of consecutive zeros.

NOTE—SL<p> and SL<n> are the positive and negative sides of the differential signal pair.

DC-referenced voltage levels are not defined since the receiver is AC-coupled. The common-mode voltage of SL<p> and SL<n>, with respect to signal ground, shall be measured at Vcom in Figure 130–2, with the value as specified in Table 130–4.

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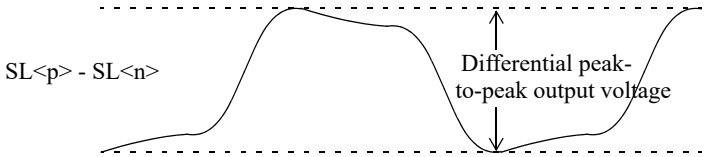

Figure 130–3—Transmitter peak-to-peak differential output voltage definition

For EEE capability, the transmitter shall meet the Table 130–4 requirement for differential peak to peak output voltage when TX is disabled within 500 ns of tx_mode being set to QUIET and remain so while tx_mode is set to QUIET. Furthermore, the transmitter's peak-to-peak differential output voltage shall be greater than 720 mV within 500 ns of tx_mode being set to ALERT. The transmitter output shall be fully compliant within 5 μs after tx_mode is set to DATA. During LPI mode, the common-mode voltage shall not deviate from the pre-LPI value by more than that allowed in Table 130–4.

130.7.1.5 Differential output return loss

For frequencies from 100 MHz to 3750 MHz, the differential output return loss, in dB, of the transmitter shall meet the requirements of Table 130–4. This output impedance requirement applies to all valid output levels. The reference impedance for differential output return loss measurements shall be 100 Ω.

$$Return\_loss \geq 10 \tag{130–3}$$

for 100 MHz ≤ f < 1289 MHz and,

$$Return\_loss(f) \geq Return\_loss_{min} = 10 - 13.275\log_{10}\left(\frac{f}{1289\,\text{MHz}}\right) \tag{130–4}$$

for 1289 MHz ≤ f ≤ 3750 MHz.

The minimum differential output return loss is shown in Figure 130–4.

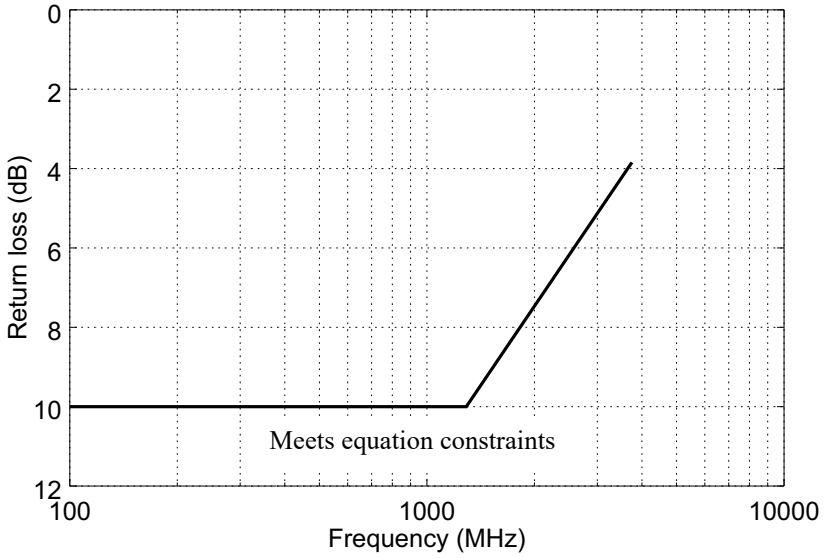

Figure 130–4—Transmit output differential-mode return loss limit

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130.7.1.6 Common-mode output return loss

The transmitter common-mode return loss shall meet the requirements of Table 130–4. The reference impedance for common-mode return loss measurements is 25 Ω.

$$Return\_loss \geq 7 \tag{130–5}$$

for 100 MHz ≤ f < 1250 MHz,

$$Return\_loss(f) \geq 7 - 13.275 \log_{10}\left(\frac{f}{1250\text{MHz}}\right) \tag{130–6}$$

for 1250 MHz ≤ f ≤ 3750 MHz.

The minimum common-mode output return loss is shown in Figure 130–5.

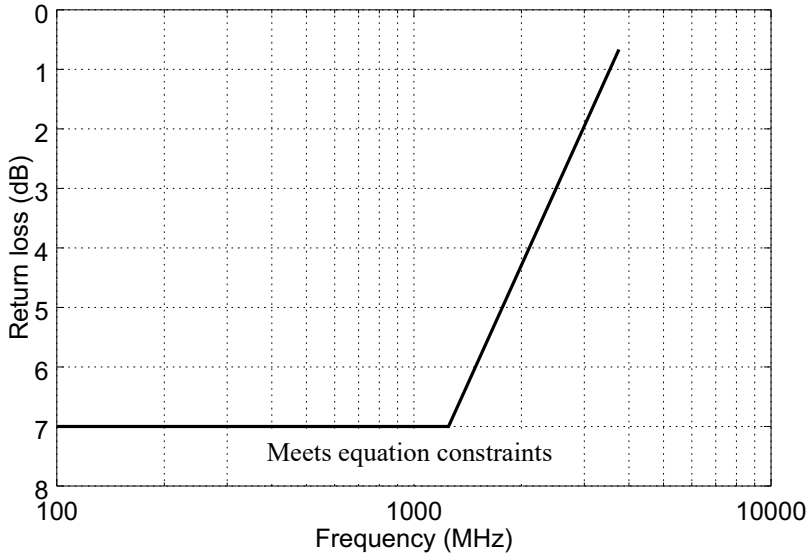

Figure 130–5—Transmit common-mode output return loss limit

130.7.1.7 Transition time

The rising and falling edge transition times shall be as specified in Table 130–4 when measured with respect to v_1 and v_3 as defined in Figure 130–7. Measurement is done using the square wave test pattern defined in 52.9.1.2, with no equalization (bit 1.150.2 in Table 45–75 set to '1') and a run of at least eight consecutive ones followed by an equal number of consecutive zeros.

The BASE-R PMD control register is also used by 5GBASE-KR described in Clause 130 to disable the transmitter equalizer for test purposes. 5GBASE-KR does not use the startup protocol.

130.7.1.8 Transmit jitter test requirements

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in Annex 48B.3. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 4 MHz is applied to the jitter. The data pattern for jitter measurements shall be test

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patterns 2 or 3 as defined in 52.9.1.1. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal. Equalization shall be off during jitter testing (bit 1.150.2 in Table 45–75 set to '1').

The duty cycle distortion test pattern shall consist of no fewer than eight symbols of alternating polarity (e.g., a 10101010… bit sequence).

130.7.1.9 Transmit jitter

The transmitter shall be as specified in Table 130–4. Duty cycle distortion (DCD) is considered a component of deterministic jitters. The peak-to-peak duty cycle distortion is defined as the absolute value of the difference in the mean pulse width of a 1 pulse or the mean pulse width of a 0 pulse (as measured at the mean of the high and low voltage levels in a repeating 0101 bit sequence) and the nominal pulse width. Jitter specifications are specified for BER 10^{-12}. Transmit jitter test requirements are specified in 130.7.1.8.

NOTE—Duty cycle distortion (DCD) is also referred to as Even-odd jitter (see 92.8.3.8.1).

130.7.1.10 Transmitter output waveform

The 5GBASE-KR transmitter includes pre-emphasis to compensate for frequency-dependent loss in the backplane channel and facilitate data recovery at the receiver. This equalization may be accomplished with a two-tap finite impulse response (FIR) structure as shown in Figure 130–6.

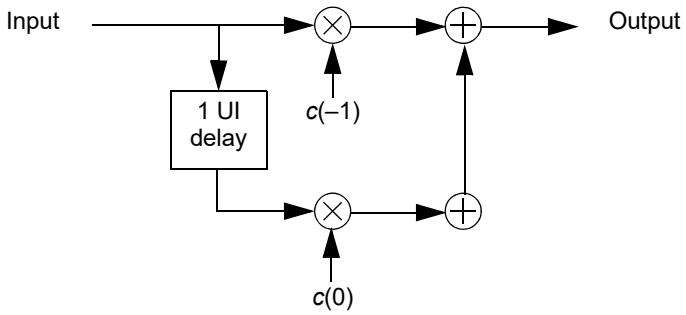

Figure 130–6—Transmit equalizer example

The test pattern for the transmitter output waveform is the square wave test pattern defined in 52.9.1.2, with a run of at least eight consecutive ones followed by an equal number of consecutive zeros. The transmitter output waveform test is based on the voltages v_1 through v_4, which are illustrated in Figure 130–7 and described below. These measurements are used to calculate R_{pre}, defined in Equation (130–7). R_{pre} shall be within the limits specified in Table 130–4.

From these voltages, the pre-equalization ratio R_{pre} is derived from Equation (130–7).

$$R_{pre} = \frac{v_2}{v_1} \tag{130–7}$$

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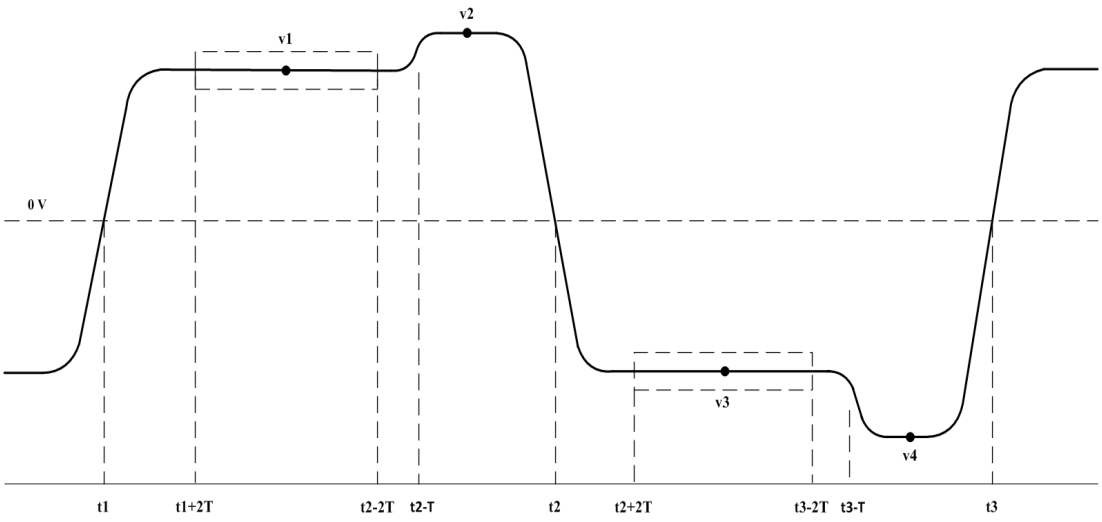

T = symbol period
t_1 = zero-crossing point of the first rising edge of the AC-coupled signal
t_2 = zero-crossing point of the falling edge of the AC-coupled signal
t_3 = zero-crossing point of the second rising edge of the AC-coupled signal
v_1 = positive steady-state voltage measured as the average voltage in the interval t_1 + 2T to t_2 – 2T
v_2 = maximum voltage measured in the interval t_2 – T to t_2
v_3 = negative steady-state voltage measured as the average voltage in the interval t_2 + 2T to t_3 – 2T
v_4 = minimum voltage measured in the interval t_3 – T to t_3

Figure 130–7—Transmitter output waveform

130.7.2 Receiver characteristics

Receiver characteristics at TP4 (see Figure 130–1) are summarized in Table 130–5 and detailed in 130.7.2.1 through 130.7.2.5.

Table 130–5—Receiver characteristics for 5GBASE-KR

Parameter	Subclause reference	Value	Units
Bit error ratio	130.7.2.1	10^{-12}	
Signaling speed	130.7.2.2	5.15625 ± 100 ppm	GBd
Differential input peak-to-peak amplitude (max)	130.7.2.4	1200[a]	mV
Differential input return loss (min)[b]	130.7.2.5	Equation (130–3) and Equation (130–4)	dB

[a]The receiver shall tolerate input amplitudes up to a maximum of 1600 mV without permanent damage.
[b]Relative to 100 Ω differential.

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130.7.2.1 Receiver interference tolerance

The receiver interference tolerance consists of two separate tests as described in Annex 69A with the parameters specified in Table 130–6. The data pattern for the interference tolerance test shall be the test patterns 2 or 3 as defined in 52.9.1.1. The receiver shall satisfy the requirements for interference tolerance specified in Annex 69A for both tests.

Table 130–6—5GBASE-KR interference tolerance parameters

Parameter	Test 1 values	Test 2 values	Units
Target BER	10^{-12}	10^{-12}	
m_{TC} (min)[a]	1	0.5	
Amplitude of broadband noise (min RMS)	5.2	12	mV
Applied transition time (20%–80%, min)	60	60	ps
Applied Sinusoidal jitter (min peak-to-peak)	0.115	0.115	UI
Applied random jitter (min peak-to-peak)[b]	0.13	0.13	UI

[a]m_{TC} is defined in Equation (69A–5)in Annex 69A.
[b]Applied random jitter is specified at a BER of 10^{-12}.

130.7.2.2 Signaling speed range

A signaling speed of a 5GBASE-KR receiver shall comply with the requirements of Table 130–5 for any signaling speed in the range 5.15625 GBd ± 100 ppm.

130.7.2.3 AC-coupling

The 5GBASE-KR receiver shall be AC-coupled to the backplane to allow for maximum interoperability between various 5 Gb/s components. AC-coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. There may be various methods for AC-coupling in actual implementations.

NOTE—It is recommended that the maximum value of the coupling capacitors be limited to 100 nF. This will limit the inrush currents to the receiver that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

130.7.2.4 Input signal amplitude

5GBASE-KR receivers shall accept differential input signal peak-to-peak amplitudes produced by compliant transmitters connected without attenuation to the receiver, and still meet the BER requirement specified in 130.7.2.1. This may be larger than the differential maximum in 130.7.1.4 due to the actual transmitter output and receiver input impedances. The input impedance of a receiver can cause the minimum signal into a receiver to differ from that measured when the receiver is replaced with a 100 Ω test load. Since the channel is AC-coupled, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

130.7.2.5 Differential input return loss

For frequencies from 100 MHz to 3750 MHz, the differential input return loss, in dB, of the receiver shall be as specified in Table 130–5.

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130.8 Interconnect characteristics

Informative interconnect characteristics are provided in Annex 69B.

130.9 Environmental specifications

130.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

130.9.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

130.9.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

130.9.4 Electromagnetic compatibility

A system integrating the 5GBASE-KR PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

130.9.5 Temperature and humidity

A system integrating the 5GBASE-KR PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

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130.10 Protocol implementation conformance statement (PICS) proforma for Clause 130, Physical Medium Dependent (PMD) sublayer and baseband medium, type 5GBASE-KR[222]

130.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3, Clause 130, Physical Medium Dependent (PMD) sublayer and baseband medium type 5GBASE-KR, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

130.10.2 Identification

130.10.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

130.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 130, Physical Medium Dependent (PMD) sublayer and baseband medium type 5GBASE-KR
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[222]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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130.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XGE	XGMII	130.1, Clause 46	Interface is supported	O	Yes [ ] No [ ]
PCS	Support of 5GBASE-R PCS/PMA	130.1, Clause 49		M	Yes [ ]
AN	Auto-Negotiation for Backplane Ethernet	130.1, Clause 73	Device implements Auto-Negotiation for Backplane Ethernet	M	Yes [ ]
DC	Delay Constraints	130.4	Device conforms to delay constraints	M	Yes [ ]
*LPI	LPI	130.6.10	LPI	O	Yes [ ] No [ ]
*MD	MDIO interface	130.5	Device implements MDIO	O	Yes [ ] No [ ]
*TD	Global_PMD_transmit_disable	130.6.5		O	Yes [ ] No [ ]

130.10.4 PICS proforma tables for Clause 130, Physical Medium Dependent (PMD) sublayer and baseband medium, type 5GBASE-KR

130.10.4.1 PCS requirements for AN service interface

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	AN service interface primitive	130.3	The PCS associated with this PMD supports the primitive AN_LINK.indication defined in 73.9	M	Yes [ ]

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130.10.4.2 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	PMD combined with sublayers through interface defined in Clause 45.	130.1	5GBASE-KR PHY layer associations. See Table 130–1	M	Yes [ ]
FS2	PMD_global_signal_detect set to the value of SIGNAL_DETECT	130.2.3.2	Required generation of PMD primitive	M	Yes [ ]
FS3	Tx+Rx delays from 5GBASE-KR PMD and medium <= 1024 bit times	130.4		M	Yes [ ]
FS4	PMD Transmit function	130.6.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FS5	PMD Transmitter signal	130.6.2	A positive differential voltage corresponds to tx_bit = ONE	M	Yes [ ]
FS6	PMD Receive function	130.6.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FS7	PMD Receiver signal	130.6.3	A positive differential voltage corresponds to rx_bit = ONE	M	Yes [ ]
FS8	PMD_fault indicates local fault in MDIO implementation	130.6.3	As specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
FS9	PMD Signal detect function	130.6.4	Report to PMD service interface	M	Yes [ ]
FS10	Global signal detect	130.6.4	Value described in 45.2.1.9.7	M	Yes [ ]
FS11	Global_PMD_signal_detect set to SIGNAL_DETECT	130.6.4	As described in Table 130–3	MD:M	Yes [ ] N/A [ ]
FS12	SIGNAL_DETECT value	130.6.4	Set to FAIL	M	Yes [ ]
FS13	PMD Signal detect during LPI	130.6.4	Detect signal energy during LPI	LPI:M	Yes [ ] N/A[ ]
FS14	PMD Signal detect for EEE	130.6.4	Transition timing to set SIGNAL_DETECT	LPI:M	Yes [ ] N/A [ ]
FS15	PMD Transmit disable requirements	130.6.5	Requirements of 130.6.5 and Table 130–4	TD:M	Yes [ ] N/A[ ]
FS16	Loopback not affected by Global_PMD_transmit_disable	130.6.5		M	Yes [ ]
FS17	PMD Transmit disable during LPI	130.6.5	Disable transmitter during tx_mode = QUIET	LPI:M	Yes [ ] N/A[ ]
FS18	Loopback support	130.6.6	Provided for 5GBASE-KR PMD by transmitter and receiver	M	Yes [ ]
FS19	Pre-cursor equalization ratio	130.7.1.10	As described in Table 130–4	M	Yes [ ]

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130.10.4.3 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	MDIO Variable Mapping	130.5	Per Table 130–2 and Table 130–3	MD:M	Yes [ ] N/A [ ]
MF2	PMD_transmit_fault function	130.6.8	Sets PMD_transmit_fault as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
MF3	PMD_receive_fault function	130.6.9	Sets PMD_receive_fault as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]

130.10.4.4 PMD Transmitter electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Test fixture impedance	130.7.1.2	100 Ω	M	Yes [ ]
TC2	Differential output return loss of test fixture	130.7.1.2	Per Equation (130–1) and Equation (130–2)	M	Yes [ ]
TC3	Signaling speed	130.7.1.3	5.15625 GBd ± 100 ppm	M	Yes [ ]
TC4	Transmitter differential peak-to-peak voltage	130.7.1.4	1200 mV, pk-pk, using the pattern as defined in 130.7.1.4	M	Yes [ ]
TC5	Maximum transmitter differential peak-to-peak voltage when TX disabled	130.7.1.4	30 mV	M	Yes [ ]
TC6	Common-mode output voltage	130.7.1.4	0V to +1.9V	M	Yes [ ]
TC7	Tx output to DATA compliance timing	130.7.1.4	Fully compliant ≤ 5 μsec from tx_mode = DATA	M	Yes [ ]
TC8	Output Amplitude LPI voltage	130.7.1.4	Less than or equal to 30 mV within 500 ns of tx_quiet	LPI:M	Yes [ ] N/A [ ]
TC9	Output Amplitude ON voltage	130.7.1.4	Less than or equal to 720 mV within 500 ns of tx_quiet deasserted	LPI:M	Yes [ ] N/A [ ]
TC10	Common-mode maintained within voltage limits	130.7.1.4	Output within ± 150 mV of the pre-LPI value	LPI:M	Yes [ ] N/A [ ]
TC11	Differential output return loss	130.7.1.5	Per Equation (130–3) and Equation (130–4)	M	Yes [ ]
TC12	Differential output reference impedance	130.7.1.5	100 Ω	M	Yes [ ]
TC13	Common-mode output return loss	130.7.1.6	Per Equation (130–5) and Equation (130–6)	M	Yes [ ]
TC14	Rising edge transition time	130.7.1.7	As specified in Table 130–4 when measured with respect to v_1 and v_3 as defined in Figure 130–7 with no equalization	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC15	Falling edge transition time	130.7.1.7	As specified in Table 130–4 when measured with respect to v_1 and v_3 as defined in Figure 130–7 with no equalization	M	Yes [ ]
TC16	Transmit jitter, peak-to-peak	130.7.1.9	Max Tj of 0.27 UI	M	Yes [ ]
TC17	Duty Cycle Distortion	130.7.1.9	Not to exceed 0.035 UI	M	Yes [ ]
TC18	Jitter test patterns	130.7.1.8	Test patterns 2 or 3 as defined in 52.9.1.1	M	Yes [ ]
TC19	DCD test pattern	130.7.1.8	Test patterns 2 or 3 as defined in 130.7.1.8.	M	Yes [ ]
TC20	Tx output waveform measurement criteria: v_1, v_2, v_3, v_4,	130.7.1.10	Measured as per Figure 130–7.	M	Yes [ ]

130.10.4.5 Receiver electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Receiver amplitude tolerance	130.7.2	Amplitudes of ≤1600 mV without permanent damage	M	Yes [ ]
RC2	Receiver interference tolerance	130.7.2.1	Measured as described in Annex 69A with parameters in Table 130–6	M	Yes [ ]
RC3	Receiver interference tolerance	130.7.2.1	Test patterns 2 or 3 as defined in 52.9.1.1	M	Yes [ ]
RC4	Receiver interference tolerance	130.7.2.1	Satisfy the requirements specified in Annex 69A	M	Yes [ ]
RC5	Signaling speed	130.7.2.2	5.15625 GBd ±100 ppm	M	Yes [ ]
RC6	Receiver coupling	130.7.2.3	AC-coupled	M	Yes [ ]
RC7	Input signal amplitude	130.7.2.4	BER met when compliant transmitter is connected with no attenuation	M	Yes [ ]
RC8	Differential input return loss	130.7.2.5	Per Equation (130–3) and Equation (130–4)	M	Yes [ ]
RC9	Differential input return loss reference impedance	130.7.2.5	100 Ω	M	Yes [ ]

130.10.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	130.9.1	Conforms to J.2	M	Yes [ ]
ES2	Electromagnetic interference	130.9.4	Complies with applicable local and national codes	M	Yes [ ]

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131. Introduction to 50 Gb/s networks

131.1 Overview

131.1.1 Scope

This clause describes the general requirements for 50 Gigabit Ethernet.

50 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 50 Gb/s, coupled with any IEEE 802.3 50GBASE Physical Layer implementation and is defined for full duplex operation only.

50 Gb/s Physical Layer devices, such as those specified in Table 131–1, provide a frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap.

131.1.2 Relationship of 50 Gigabit Ethernet to the ISO OSI reference model

50 Gigabit Ethernet couples the IEEE 802.3 MAC to a family of 50 Gb/s Physical Layers. The relationships among 50 Gigabit Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 131–1.

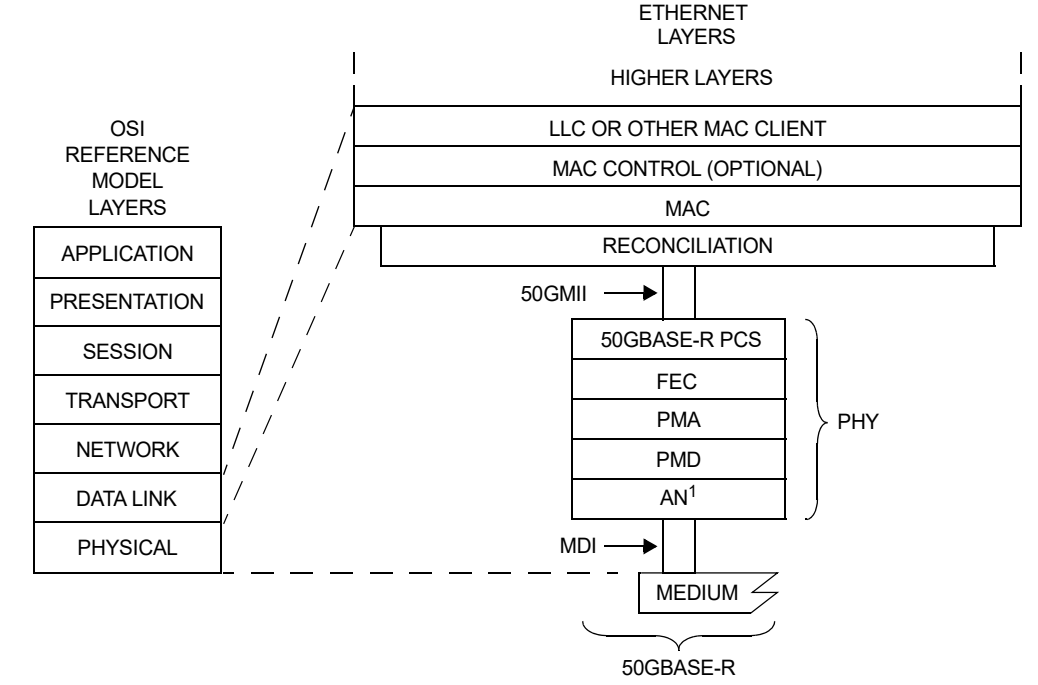

Figure 131–1—Architectural positioning of 50 Gigabit Ethernet

While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

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a) The 50GMII, which, when implemented as logical interconnection point between the MAC sublayer and the Physical Layer device (PHY), uses a 64-bit-wide data path as specified in Clause 132. Physical instantiations of this interface may use other data-path widths.

b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.

c) The PMA service interface, which, when physically implemented as LAUI-2, as specified in Annex 135B and Annex 135C, or as 50GAUI-2 (50 Gb/s two-lane Attachment Unit Interface), as specified in Annex 135D and Annex 135E, at an observable interconnection port, uses a two-lane data path.

d) The PMA service interface, which, when physically implemented as 50GAUI-1 (50 Gb/s one-lane Attachment Unit Interface) at an observable interconnection port, uses a one-lane data path as specified in Annex 135F or Annex 135G.

e) The MDI as specified in Clause 136 for 50GBASE-CR, Clause 137 for 50GBASE-KR, Clause 138 for 50GBASE-SR, and Clause 139 for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER uses a one-lane data path.

131.1.3 Nomenclature

The nomenclature employed by the 50 Gb/s Physical Layer is explained as follows.

The alpha-numeric prefix 50GBASE in the port type (e.g., 50GBASE-R) represents a family of Physical Layer devices operating at a speed of 50 Gb/s.

50GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) for 50 Gb/s operation over multiple PCS lanes (see Clause 133). Physical Layer devices listed in Table 131–1 are defined for operation at 50 Gb/s.

Table 131–1—50 Gb/s PHYs

Name	Description
50GBASE-KR	50 Gb/s PHY using 50GBASE-R encoding over an electrical backplane (see Clause 137).
50GBASE-CR	50 Gb/s PHY using 50GBASE-R encoding over twinaxial copper cable (see 1.4.559 and Clause 136).
50GBASE-SR	50 Gb/s PHY using 50GBASE-R encoding over multimode fiber (see Clause 138).
50GBASE-FR	50 Gb/s PHY using 50GBASE-R encoding over single-mode fiber, with reach up to at least 2 km (see Clause 139).
50GBASE-LR	50 Gb/s PHY using 50GBASE-R encoding over single-mode fiber, with reach up to at least 10 km (see Clause 139).
50GBASE-ER	50 Gb/s PHY using 50GBASE-R encoding over single-mode fiber, with reach up to at least 40 km (see Clause 139).

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131.1.4 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. Table 131–2 and Table 131–3 specify the correlation between PHY types and clauses. Implementations conforming to one or more PHY types meet the requirements of the corresponding clauses.

Table 131–2—PHY types and clause correlation (50GBASE copper)

PHY type	Clause[a]											
	73	78	132		133	134	135	135B	135D	135F	136	137
	Auto-Negotiation	EEE	RS	50GMII	50GBASE-R PCS	50GBASE-R RS-FEC	50GBASE-R PMA	LAUI-2 C2C	50GAUI-2 C2C	50GAUI-1 C2C	50GBASE-CR PMD	50GBASE-KR PMD
50GBASE-KR	M	O	M	O	M	M	M	O	O	O		M
50GBASE-CR	M	O	M	O	M	M	M	O	O	O	M	

[a]O = Optional, M = Mandatory.

Table 131–3—PHY types and clause correlation (50GBASE optical)

PHY type	Clause[a]															
	78	132		133	134	135	135B	135C	135D	135E	135F	135G	138	139		
	EEE	RS	50GMII	50GBASE-R PCS	50GBASE-R RS-FEC	50GBASE-R PMA	LAUI-2 C2C	LAUI-2 C2M	50GAUI-2 C2C	50GAUI-2 C2M	50GAUI-1 C2C	50GAUI-1 C2M	50GBASE-SR PMD	50GBASE-FR PMD	50GBASE-LR PMD	50GBASE-ER PMD
50GBASE-SR	O	M	O	M	M	M	O	O	O	O	O	O	M			
50GBASE-FR	O	M	O	M	M	M	O	O	O	O	O	O		M		
50GBASE-LR	O	M	O	M	M	M	O	O	O	O	O	O			M	
50GBASE-ER	O	M	O	M	M	M	O	O	O	O	O	O				M

[a]O = Optional, M = Mandatory.

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131.2 Summary of 50 Gigabit Ethernet sublayers

131.2.1 Reconciliation Sublayer (RS) and Media Independent Interface (50GMII)

The Media Independent Interface specified in Clause 132 provides a logical interconnection between the MAC sublayer and Physical Layer devices (PHYs). The Media Independent Interface is not intended to be physically instantiated, rather it can logically connect layers within a device.

The 50GMII supports 50 Gb/s operation through its 64-bit-wide transmit and receive data paths. The Reconciliation Sublayer (RS) provides a mapping between the signals provided at the 50GMII and the MAC/PLS service definition.

While the 50GMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for the physical coding sublayer defined in Clause 133.

131.2.2 Physical Coding Sublayer (PCS)

50GBASE-R PHYs use the PCS specified in Clause 133. The 50GBASE-R PCS performs encoding of data from the 50GMII to 64B/66B code blocks and transfers the encoded data to the PMA (or FEC) and performs decoding of 64B/66B blocks from the PMA (or FEC) and transfers the decoded data to the 50GMII.

131.2.3 Forward error correction (FEC) sublayer

50GBASE-R PHYs use the FEC sublayer specified in Clause 134. The FEC sublayer can be placed between the PCS and PMA sublayers or between two PMA sublayers.

131.2.4 Physical Medium Attachment (PMA) sublayer

The 50GBASE-R PMA specified in Clause 135 provides a medium-independent means for the PCS to support the use of a range of physical media.

The 50GBASE-R PMA performs the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface, the mapping of transmit and receive data streams between the FEC and the PMA via the PMA service interface, and the mapping and multiplexing of transmit and receive data streams between the PMA and PMD via the PMD service interface. In addition, the PMA performs retiming of the received data stream when appropriate, optionally provides data loopback at the PMA or PMD service interface, and optionally provides test-pattern generation and checking.

131.2.5 Physical Medium Dependent (PMD) sublayer

The Physical Medium Dependent sublayer is responsible for interfacing to the transmission medium. The PMD is located just above the Medium Dependent Interface (MDI). The MDI, logically subsumed within each PMD subclause, is the actual medium attachment for the various supported media.

The 50GBASE-R PMDs and their corresponding media are specified in Clause 136 through Clause 139.

131.2.6 Management interface (MDIO/MDC)

The optional MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMDs) and Station Management (STA) entities.

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131.2.7 Management

Managed objects, attributes, and actions are defined for all 50 Gigabit Ethernet components. These items are defined in Clause 30.

131.3 Service interface specification method and notation

The service interface specification for the 50GBASE-R Physical Layers is as per the definition in 1.2.2. Note that the 50GBASE-R inter-sublayer service interfaces use multiple scalar REQUEST and INDICATION primitives, to indicate the transfer of multiple independent streams of data units, as defined in 131.3.1 through 131.3.3.

131.3.1 Inter-sublayer service interface

The inter-sublayer service interface is defined in 116.3.1.

131.3.2 Instances of the inter-sublayer service interface

The inter-sublayer interface can be instantiated between different sublayers, hence a prefix notation is defined to identify a specific instance of an inter-sublayer service interface. The following prefixes are defined:

a) PMD:—for primitives issued on the interface between the PMD sublayer and the PMA sublayer called the PMD service interface.
b) PMA:—for primitives issued on the interface between the PMA sublayer and the PCS or the FEC sublayer called the PMA service interface.
c) FEC:—for primitives issued on the interface between the FEC sublayer and the PCS or the PMA sublayer called the FEC service interface.

Examples of inter-sublayer service interfaces for 50GBASE-R with their corresponding instance names are illustrated in Figure 131–2. For example, the primitives for one instance of the inter-sublayer service interface, named the PMD service interface, are identified as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication.

Primitives for other instances, of inter-sublayer interfaces, are represented in a similar manner as described above.

131.3.3 Semantics of inter-sublayer service interface primitives

The semantics of the inter-sublayer service interface primitives for the 50GBASE-R sublayers are described in 116.3.3.1 through 116.3.3.3.

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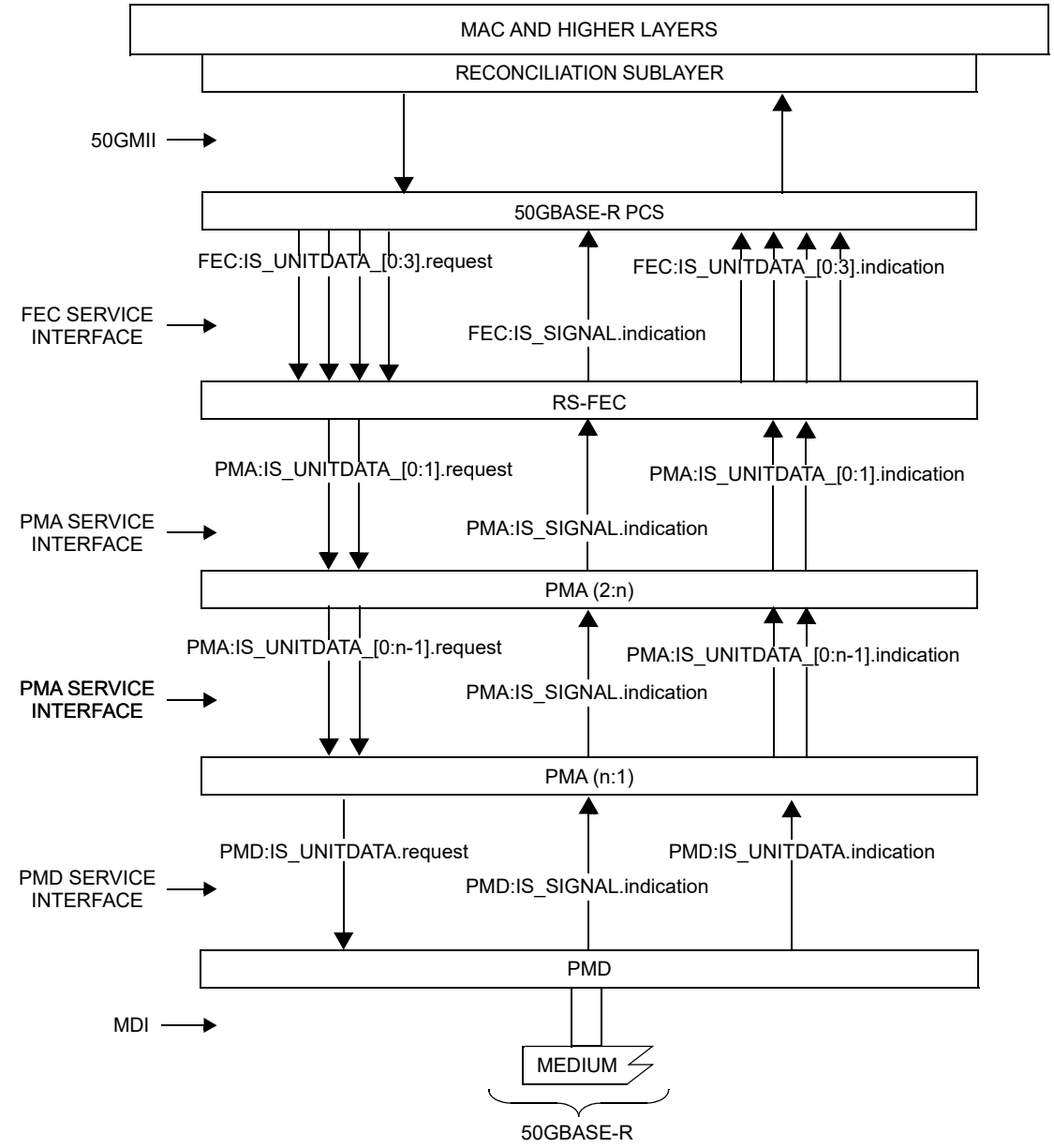

50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = NUMBER OF PARALLEL STREAMS
n = 1 or 2

Figure 131–2—50GBASE-R inter-sublayer service interfaces

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131.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. Table 131–4 contains the values of maximum sublayer delay (sum of transmit and receive delays at one end of the link) in bit times as specified in 1.4 and pause_quanta as specified in 31B.2 for 50 Gigabit Ethernet. If a PHY contains an Auto-Negotiation sublayer, the delay of the Auto-Negotiation sublayer is included within the delay of the PMD and medium.

Table 131–4—Sublayer delay constraints (50GBASE)

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
50G MAC, RS, and MAC Control	16 384	32	327.68	See 132.1.4.
50GBASE-R PCS	11 264	22	225.28	See 133.3.
50GBASE-R RS-FEC	25 600	50	512	See 134.4.
50GBASE-R PMA	4 608	9	92.16	See 135.5.4.
50GBASE-KR PMD	2 048	4	40.96	See 137.5. Includes allocation of 20 ns for the medium.
50GBASE-CR PMD	2 048	4	40.96	See 136.5. Includes allocation of 20 ns for the medium.
50GBASE-SR PMD	1 024	2	20.48	Includes 2 m of fiber. See 138.3.1.
50GBASE-FR PMD	1 024	2	20.48	Includes 2 m of fiber. See 139.3.
50GBASE-LR PMD	1 024	2	20.48	Includes 2 m of fiber. See 139.3.
50GBASE-ER PMD	1 024	2	20.48	Includes 2 m of fiber. See 139.3.
50GBASE-BR10 PMD	1 024	2	20.48	Includes 2 m of fiber. See 160.3.1.
50GBASE-BR20 PMD	1 024	2	20.48	Includes 2 m of fiber. See 160.3.1.
50GBASE-BR40 PMD	1 024	2	20.48	Includes 2 m of fiber. See 160.3.1.

[a]For 50GBASE-R, 1 bit time is equal to 20 ps. (See 1.4.215 for the definition of bit time.)
[b]For 50GBASE-R, 1 pause_quantum is equal to 10.24 ns. (See 31B.2 for the definition of pause_quanta.)
[c]Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

See 80.4 for the calculation of bit time per meter of fiber or electrical cable.

See 31B.3.7 for PAUSE reaction timing constraints for stations at operating speeds of 50 Gb/s.

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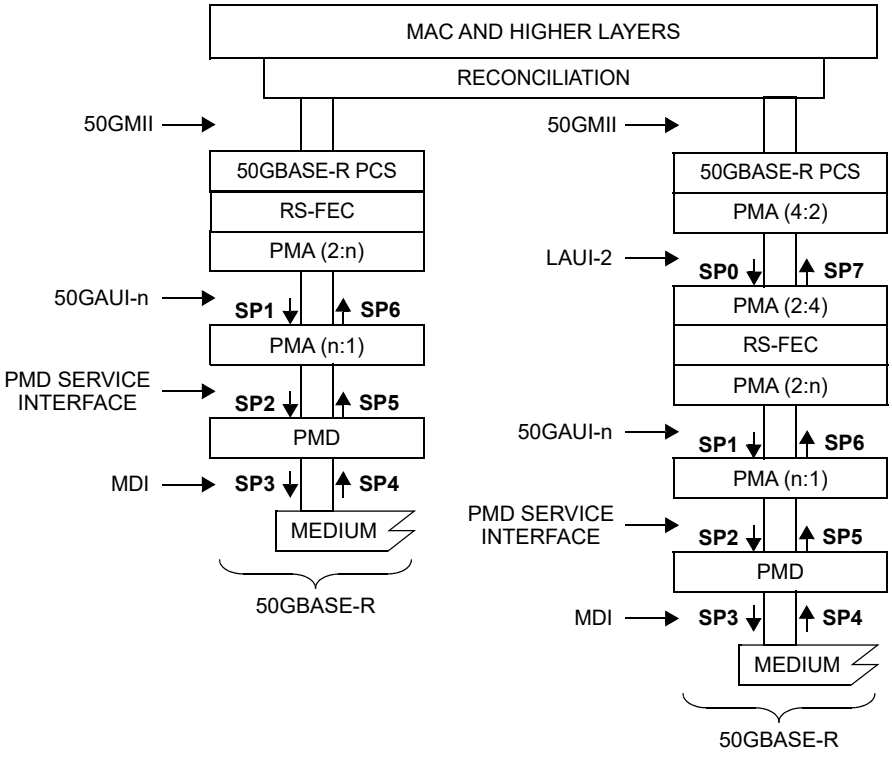
131.5 Skew constraints

Skew (or relative delay) can be introduced between lanes by both active and passive elements of a 50GBASE-R link. Skew is defined as the difference between the times of the earliest PCS lane and latest PCS lane for the one to zero transition of the alignment marker sync bits. The PCS deskew function (see 133.2.3) compensates for all lane-to-lane Skew observed at the receiver. The Skew between the lanes is kept within limits as shown in Table 131–5 so that the transmitted information on the lanes can be reassembled by the receive PCS.

Skew Variation may be introduced due to variations in electrical, thermal or environmental characteristics. Skew Variation is defined as the change in Skew between any PCS lane and any other PCS lane over the entire time that the link is in operation. From the time the link is brought up, Skew Variation is limited to ensure that each PCS lane always traverses the same lane between any pair of adjacent sublayers while the link remains in operation.

The maximum Skew and Skew Variation at physically instantiated interfaces is specified at Skew points SP0, SP1, SP2, and SP3 for the transmit direction and SP4, SP5, SP6, and SP7 for the receive direction as illustrated in Figure 131–3.



50GAUI-n = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
LAUI-2 = 50 Gb/s ATTACHMENT UNIT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = 1 or 2

Figure 131–3—50GBASE-R Skew points

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In the transmit direction, the Skew points are defined in the following locations:

— SP0 on the LAUI-2 interface, at the input of the PMA above the RS-FEC;
— SP1 on the 50GAUI-n interface, at the input of the PMA closest to the PMD;
— SP2 on the PMD service interface, at the input of the PMD;
— SP3 at the output of the PMD, at the MDI.

In the receive direction, the Skew points are defined in the following locations:

— SP4 at the MDI, at the input of the PMD;
— SP5 on the PMD service interface, at the output of the PMD;
— SP6 on the 50GAUI-n interface, at the output of the PMA below the RS-FEC;
— SP7 on the LAUI-2 interface, at the output of the PMA above the RS-FEC.

The allowable limits for Skew are shown in Table 131–5 and the allowable limits for Skew Variation are shown in Table 131–6.

The Skew requirements for the PCS, PMA and PMD sublayers are specified in the respective clauses as noted in Table 131–5 and Table 131–6.

Table 131–5—Summary of Skew constraints

Skew points	Maximum Skew (ns)[a]	Maximum Skew for 50GBASE-R PCS lane (UI)[b]	Maximum Skew for 50GBASE-R FEC lane (UI)[c]	Notes[d]
SP0	29	≈ 374	N/A	See 135.5.3.1
SP1	29	N/A	≈ 770	See 135.5.3.3
SP2	43	N/A	≈ 1142	See 135.5.3.3, 136.6, 137.6, 138.3.2, 139.3
SP3	54	N/A	≈ 1434	See 136.6, 137.6, 138.3.2, 139.3
SP4	134	N/A	≈ 3559	See 136.6, 137.6, 138.3.2, 139.3
SP5	145	N/A	≈ 3852	See 135.5.3.3, 136.6, 137.6, 138.3.2, 139.3
SP6	160	N/A	≈ 4250	See 135.5.3.7
SP7	29	≈ 374	N/A	See 135.5.3.8
At FEC transmit	49	N/A	≈ 1302	See 134.5.2.2
At FEC receive	180	N/A	≈ 4781	See 134.5.2.2
At PCS receive	49	≈ 632	N/A	See 133.2.3

[a]The Skew limit includes 1 ns allowance for PCB traces that are associated with the Skew points.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew in UI based on 1 UI equals 77.5758 ps at PCS lane signaling rate of 12.890625 Gb/s.
[c]The symbol ≈ indicates approximate equivalent of maximum Skew in UI based on 1 UI equals 37.6471 ps at FEC lane signaling rate of 26.5625 Gb/s.
[d]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

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Table 131–6—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation (ns)	Maximum Skew Variation for 25.78125 GBd lane (UI)[a]	Maximum Skew Variation for 26.5625 GBd lane (UI)[b]	Notes[c]
SP0	0.2	≈ 5	N/A	See 135.5.3.1
SP1	0.2	N/A	≈ 5	See 135.5.3.3
SP2	0.4	N/A	≈ 11	See 135.5.3.5
SP3	0.6	N/A	≈ 16	
SP4	3.4	N/A	≈ 90	
SP5	3.6	N/A	≈ 96	See 135.5.3.6
SP6	3.8	N/A	≈ 101	See 135.5.3.7
SP7	0.2	≈ 6	N/A	See 135.5.3.8
At FEC transmit	0.4	N/A	≈ 11	See 134.5.2.2
At FEC receive	4	N/A	≈ 106	See 134.5.2.2
At PCS receive	0.4	≈ 10	N/A	See 133.2.3

[a]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI based on 1 UI equals 38.7879 ps at LAUI-2 lane signaling rate of 25.78125 GBd.
[b]The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI based on 1 UI equals 37.6471 ps at 50GAUI-2 lane signaling rate of 26.5625 GBd.
[c]Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

131.6 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

Multiple states of a function that have a transition to a common state utilizing different qualifiers (for example, multiple exit conditions to an IDLE or WAIT state) may be indicated by a shared arrow. An exit transition arrow connects to the shared arrow, and the qualifier is met prior to termination of the transition arrow on the shared arrow. The shared arrow has no qualifier.

131.7 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 132 through Clause 140, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the 50 Gigabit Ethernet PICS conforms to the same notation and conventions used in 21.6.

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132. Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation

132.1 Overview

This clause defines the characteristics of the Reconciliation Sublayer (RS) and the Media Independent Interface between Ethernet media access controllers and various PHYs. Figure 132–1 shows the relationship of the RS and Media Independent Interface to the ISO/IEC OSI reference model. The 50 Gb/s RS has identical logical functionality to the 40 Gb/s RS defined in Clause 81.

The 50GMII is an optional logical interface between the MAC sublayer and the Physical Layer device (PHY).

The RS adapts the bit serial protocols of the MAC to the parallel format of the PCS service interface. Though the 50GMII is an optional interface, it is used in this standard as a basis for specification. The Physical Coding Sublayer (PCS) is specified to the 50GMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and 50GMII were implemented.

The 50GMII has the following characteristics:

a) The 50GMII supports a speed of 50 Gb/s.
b) Data and delimiters are synchronous to a clock reference.
c) It provides independent 64-bit-wide transmit and receive data paths.
d) It supports full duplex operation only.

132.1.1 Summary of major concepts

The following are the major concepts of the 50GMII:

a) The 50GMII is functionally similar to other media independent interfaces that have been defined for other speeds, as they all define an interface allowing independent development of MAC and PHY logic.
b) The RS converts between the MAC serial data stream and the parallel data paths of the 50GMII.
c) The RS maps the signal set provided at the 50GMII to the PLS service primitives provided at the MAC.
d) Each direction of data transfer is independent and serviced by data, control, and clock signals.
e) The RS generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.
f) The RS participates in link fault detection and reporting by monitoring the receive path for status reports that indicate an unreliable link, and generating status reports on the transmit path to report detected link faults to the DTE on the remote end of the connecting link.
g) The 50GMII may also support Low Power Idle (LPI) signaling for PHY types supporting Energy-Efficient Ethernet (EEE) (see Clause 78).

132.1.2 Application

This clause applies to the interface between the MAC and PHY. This logical interface is used to provide media independence so that an identical media access controller may be used with all 50GBASE PHY types.

132.1.3 Rate of operation

The 50GMII is specified to support 50 Gb/s operation.

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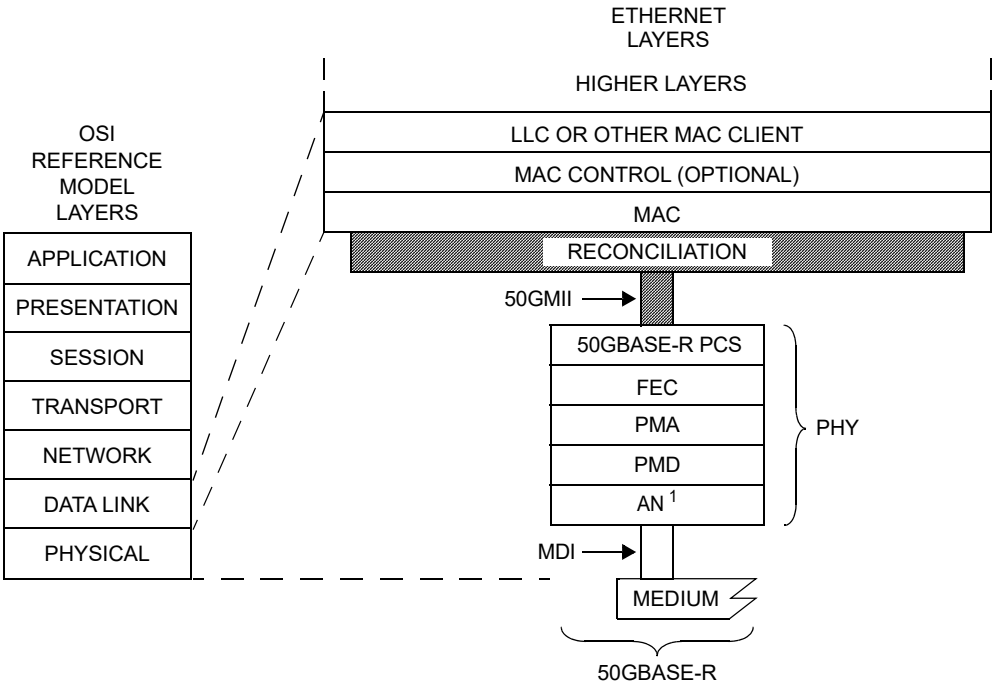

50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 132–1—RS and MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

132.1.4 Delay constraints

The maximum cumulative MAC Control, MAC, and RS delay (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 132–1. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

Table 132–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
50 Gb/s MAC, RS, and MAC Control	16 384	32	327.68

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132.1.5 Allocation of functions

The allocation of functions at the 50GMII balances the need for media independence with interface simplicity. The 50GMII maximizes media independence by separating the Data Link and Physical Layers of the OSI seven-layer reference model.

132.1.6 50GMII structure

The 50GMII structure is identical to the XLGMII/CGMII structure specified in 81.1.7.

132.1.7 Mapping of 50GMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the 50GMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 50 Gb/s; therefore, PLS service primitives supporting CSMA/CD operation are not mapped through the RS to the 50GMII. This behavior and restrictions are the same as described in 22.7, with the details of the signaling described in 132.3. LPI_REQUEST shall not be set to ASSERT unless the attached link has been operational for at least one second (i.e., link_status = OK, according to the underlying PCS/PMA).

EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

Mappings for the following primitives are defined for 50 Gb/s:

PLS_DATA.request
PLS_DATA.indication
PLS_CARRIER.indication
PLS_SIGNAL.indication
PLS_DATA_VALID.indication

The RS maps all primitives in an identical manner as the XLGMII/CGMII does and as specified in 81.1.7.

132.2 50GMII data stream

The 50GMII data stream has the same characteristics as the XLGMII/CGMII data stream described in 81.2.

132.3 50GMII functional specifications

The 50GMII functions identically to the XLGMII/CGMII specified in 81.3.

132.4 LPI assertion and detection

LPI assertion and detection function identically to the XLGMII/CGMII specified in 81.4, with the single exception that the PMA stop signaling is not applicable.

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been deasserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake-up time is enforced by the transmit LPI state diagram using CARRIER_SENSE.indication in an identical manner to that defined in 81.4, with the single exception that the PMA stop signaling described in 81.4.4 is not applicable.

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132.5 Protocol implementation conformance statement (PICS) proforma for Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation[223]

132.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

132.5.2 Identification

132.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

132.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[223] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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132.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PHY	PHY support of 50GMII	132.2		O	Yes [ ] No [ ]
*RS	Reconciliation Sublayer support of 50GMII	132.2		O	Yes [ ] No [ ]
*LPI	Implementation of LPI	132.4		O	Yes [ ] No [ ]

132.5.3 PICS proforma tables for Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation

132.5.3.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	PHY support of MAC data rate	132.1	Support MAC data rate of 50 Gb/s	PHY:M	Yes [ ] N/A [ ]
G2	Cumulative MAC Control, MAC, and RS round-trip delay	132.1.4	Per Table 132–1	RS:M	Yes [ ] N/A [ ]

132.5.3.2 Mapping of PLS service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
PL1	Mapping to Clause 6	132.1.7	RS implements mapping to Clause 6 PLS service primitives	RS:M	Yes [ ] N/A [ ]

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133. Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R

133.1 Overview

133.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) that is common to a family of 50 Gb/s Physical Layer implementations known as 50GBASE-R. The 50GBASE-R PCS is a sublayer of the 50 Gb/s PHYs listed in Table 131–1.

133.1.2 Relationship of 50GBASE-R to other standards

Figure 133–1 depicts the relationships among the 50GBASE-R sublayers, the Ethernet MAC and Reconciliation Sublayers, and the higher layers.

The 50GBASE-R PCS specifications are based on the 40GBASE-R PCS specifications in Clause 82, with the modifications listed in 133.2 and 133.3.

133.1.3 Summary of 50GBASE-R sublayers

Figure 133–1 shows the relationship of the 50GBASE-R PCS sublayer (shown shaded) with other sublayers to the ISO Open System Interconnection (OSI) reference model.

133.1.3.1 Physical Coding Sublayer (PCS)

The PCS service interface is the 50GMII, which is defined in Clause 132. The 50GMII provides a uniform interface to the Reconciliation Sublayer for all 50 Gb/s PHY implementations

The 50GBASE-R PCS provides all services required by the 50GMII.

133.1.4 Inter-sublayer interfaces

The upper interface of the PCS may connect to the Reconciliation Sublayer through the 50GMII.

The lower interface of the PCS connects to the FEC sublayer. If the optional LAUI-2 interface (see 135B.1 and 135C.1) is physically instantiated directly below the PCS sublayer, then the lower interface of the PCS instead connects to the PMA. The 50GBASE-R PCS is based on 4 PCS lanes and has a nominal rate at the FEC or PMA service interface of 12.890625 Gb/s per PCS lane, which provides capacity for the MAC data rate of 50 Gb/s.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

133.1.4.1 PCS service interface (50GMII)

The PCS service interface allows the 50GBASE-R PCS to transfer information to and from a PCS client. The PCS client is the Reconciliation Sublayer. The PCS Service Interface is defined as the 50GMII in Clause 132.

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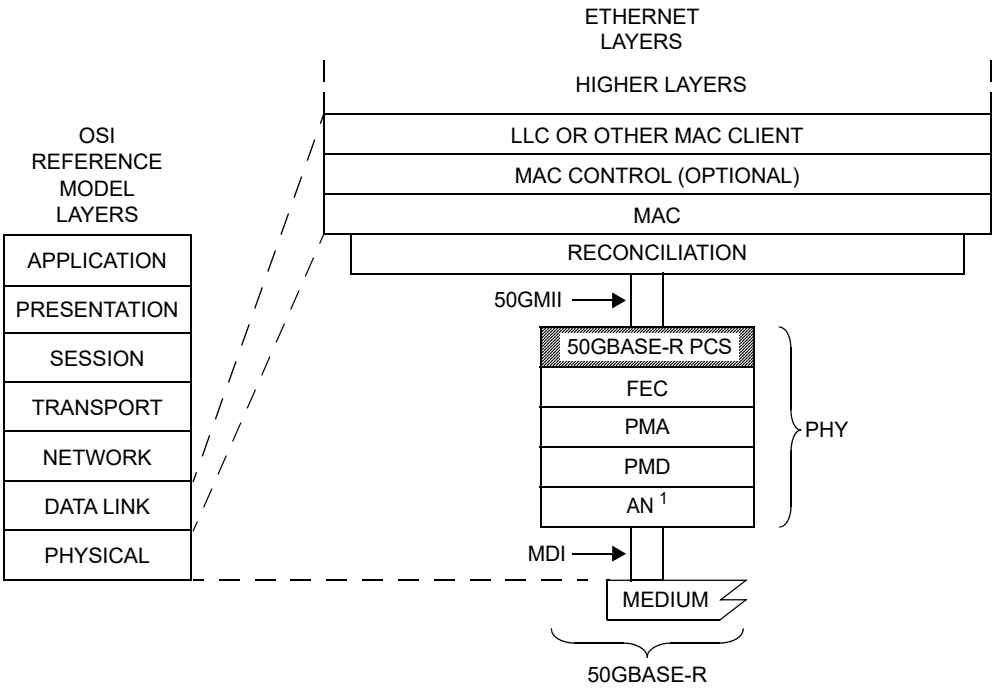

50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
FEC = FORWARD ERROR CORRECTION

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 133–1—50GBASE-R PCS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

133.1.4.2 Forward error correction (FEC) or Physical Medium Attachment (PMA) service interface

The FEC or PMA service interface for the PCS is described in an abstract manner and does not imply any particular implementation. The FEC or PMA Service Interface supports the exchange of encoded data between the PCS and the FEC or PMA sublayer. The FEC service interface is defined in 134.2. The PMA service interface is defined in 135.3.

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133.1.5 Functional block diagram

Figure 133–2 provides a functional block diagram of the 50GBASE-R PCS.

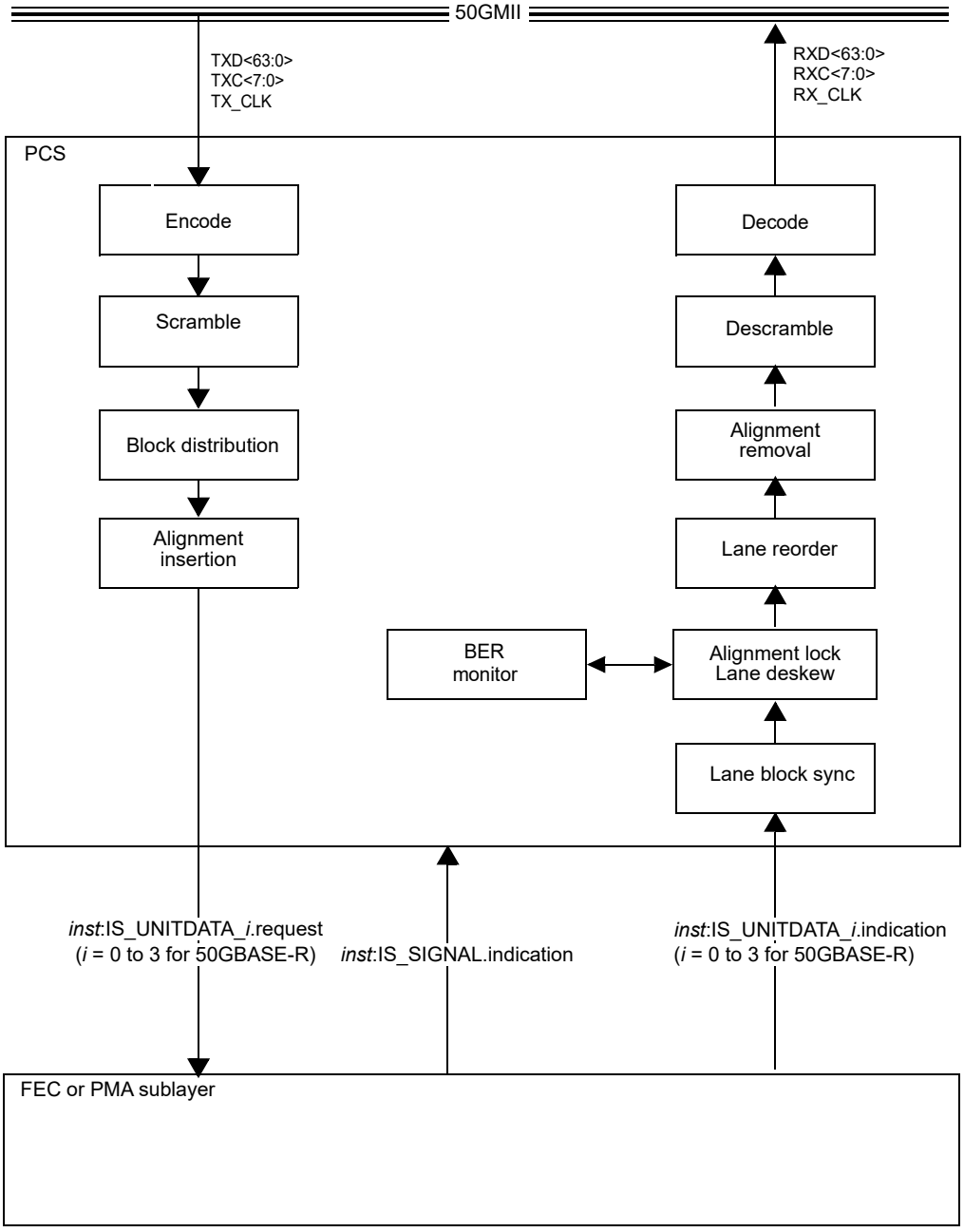

Figure 133–2—50GBASE-R PCS functional block diagram

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133.2 Physical Coding Sublayer (PCS)

133.2.1 Functions within the PCS

The 50GBASE-R PCS shall have all of the functionality of the 40GBASE-R PCS specified in Clause 82 with the following exceptions:

a) The nominal rate at the FEC or PMA service interface is 12.890625 Gb/s per PCS lane, rather than 10.3125 Gb/s per PCS lane.

b) The alignment marker spacing is modified such that alignment markers are inserted after every 20 479 66-bit blocks on each PCS lane, rather than after every 16 383 66-bit blocks on each PCS lane as described in 82.2.7. (See 133.2.2.)

c) The definition of the variables current_am, am_counter, ber_cnt, and xus_timer in the state diagrams defined in 82.2.19 are modified to account for the different alignment marker spacing and the different data rate. (See 133.2.4.)

d) The optional deep sleep mode of EEE is not supported.

133.2.2 Alignment marker insertion

The alignment marker insertion for the 50GBASE-R PCS is identical to the alignment marker insertion for the 40GBASE-R PCS described in 82.2.7, with the exception that the alignment markers shall be inserted after every 20 479 66-bit blocks on each PCS lane, rather than after every 16 383 66-bit blocks on each PCS lane as described in 82.2.7. Alignment marker insertion is illustrated in Figure 133–3 and Figure 133–4.

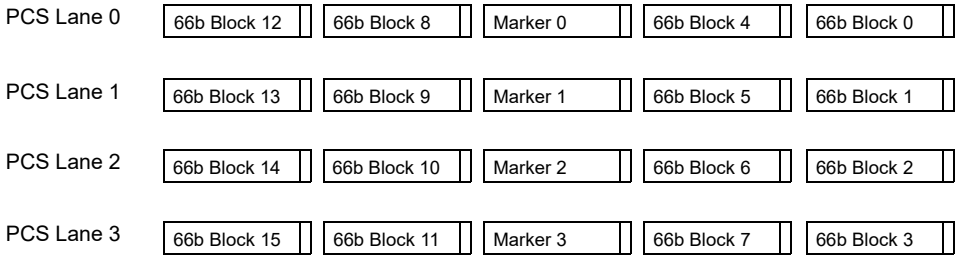

Figure 133–3—Alignment marker insertion

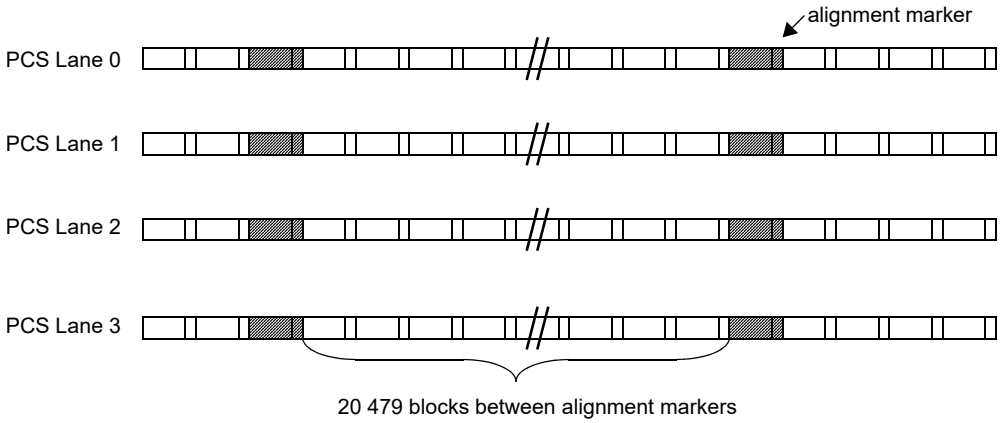

Figure 133–4—Alignment marker insertion period

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The format of the 50GBASE-R PCS alignment markers is identical to the format of the 40GBASE-R PCS alignment markers described in 82.2.7 and shown in Figure 82–9.

The content of the 50GBASE-R PCS alignment markers is identical to the content of the 40GBASE-R PCS alignment markers described in 82.2.7 and shown in Table 82–3.

133.2.3 PCS lane deskew

The 50GBASE-R PCS receiver shall support a maximum Skew of 49 ns and a maximum Skew Variation of 0.4 ns.

Skew and Skew Variation are defined in 131.5.

133.2.4 Detailed functions and state diagrams

The state diagrams are identical to those for the 40GBASE-R PCS defined in 82.2.19 with the exception that some variables, counters and timers are redefined as follows:

current_am
: This variable holds the lane number of the current alignment marker. This is compared to the variable first_am to determine if we have alignment marker lock and is always n × 20 480 66-bit blocks away from the first_am.

am_counter
: This counter counts 66-bit blocks that separate two consecutive alignment markers. The terminal count is 20 479.

ber_cnt
: This counter counts up to a maximum of 97 of the number of invalid sync headers within the current 1 ms period.

xus_timer
: Timer that is triggered every 1 ms +1%, –25%.

133.3 Delay constraints

The maximum delay contributed by the 50GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 11 264 bit times (22 pause_quanta or 225.28 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

133.4 Auto-Negotiation

The following requirements apply to a PCS used with a 50GBASE-CR or 50GBASE-KR PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

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133.5 Protocol implementation conformance statement (PICS) proforma for Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R[224]

133.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

133.5.2 Identification

133.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

133.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[224]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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133.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
PCS	Supports 50GBASE-R PCS functionality	133.1.1		M	Yes [ ]
XGE50	50GMII logical interface	132, 133.1.4	Logical interface is supported	O	Yes [ ] No [ ]
*MD	MDIO	45, 82.3	Registers and interface supported	O	Yes [ ] No [ ]
PMA	Supports operation directly connected to a PMA	133.1.4.2		O.1	Yes [ ] No [ ]
FEC	Supports operation directly connected to an FEC sublayer	133.1.4.2		O.1	Yes [ ] No [ ]
*JTM	Supports test-pattern mode	82.2.1		PMA:M	Yes [ ] N/A[ ]

133.5.4 PICS proforma tables for Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R

133.5.4.1 Coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder (and ENCODE function) implements the code as specified	82.2.3 and 82.2.19.2.3		M	Yes [ ]
C2	Decoder (and DECODE function) implements the code as specified	82.2.3 and 82.2.19.2.3		M	Yes [ ]
C3	Only valid block types are transmitted	82.2.3.3		M	Yes [ ]
C4	Invalid block types are treated as an error	82.2.3.3		M	Yes [ ]
C5	Only valid control characters are transmitted	82.2.3.4		M	Yes [ ]
C6	Invalid control characters are treated as an error	82.2.3.4		M	Yes [ ]
C7	Idles do not interrupt data	82.2.3.6		M	Yes [ ]
C8	IDLE control code insertion and deletion	82.2.3.6	Insertion or Deletion in groups of 8 /I/s	M	Yes [ ]
C9	Sequence ordered set deletion	82.2.3.9	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ]

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133.5.4.2 Scrambler and Descrambler

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Scrambler	82.2.5	Performs as shown in Figure 49–8	M	Yes [ ]
S2	Descrambler	82.2.16	Performs as shown in Figure 49–10	M	Yes [ ]

133.5.4.3 Deskew and Reordering

Item	Feature	Subclause	Value/Comment	Status	Support
DR1	Deskew	82.2.13, 133.2.3	Able to deskew up to the value in 133.2.3.	M	Yes [ ]
DR2	Reordering	82.2.14	Performs reordering.	M	Yes [ ]

133.5.4.4 Alignment Markers

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	Alignment marker insertion	133.2.2	Alignment markers are inserted periodically as described in section 133.2.2	M	Yes [ ]
AM2	Alignment marker format	133.2.2	Alignment markers are formed as described in Figure 82–9 and Table 82–3	M	Yes [ ]
AM3	Lane mapping	82.2.19.3	PCS lane number is captured	MD:M	Yes [ ] N/A [ ]

133.5.4.5 Test-pattern modes

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Scrambled idle transmit test-pattern generator is implemented	82.2.11	Performs as in 82.2.11	JTM:M	Yes [ ] N/A[ ]
JT2	Scrambled idle receive test-pattern checker is implemented	82.2.18	Performs as in 82.2.18	JTM:M	Yes [ ] N/A[ ]
JT3	Transmit and receive test-pattern modes can operate simultaneously	82.2.1		JTM:M	Yes [ ] N/A[ ]

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133.5.4.6 Bit order

Item	Feature	Subclause	Value/Comment	Status	Support
B1	Transmit bit order	133.2.1, 82.2.3.2	Placement of bits into the PCS lanes as shown in Figure 82–3	M	Yes [ ]
B2	Receive bit order	133.2.1, 82.2.3.2	Placement of bits into the 50GMII as shown in Figure 82–4	M	Yes [ ]

133.5.4.7 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Equivalent access to PCS Management objects is provided	82.3		!MD:O	Yes [ ] No [ ] N/A [ ]

133.5.4.8 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	50GBASE-R Block Lock	133.2.4	Implements 4 block lock processes as depicted in Figure 82–12	M	Yes [ ]
SM2	The SLIP function evaluates all possible bit positions	133.2.4		M	Yes [ ]
SM3	50GBASE-R Alignment Marker Lock	133.2.4	Implements 4 alignment marker lock processes as depicted in Figure 82–13	M	Yes [ ]
SM4	The AM_SLIP functions evaluates all possible blocks	133.2.4		M	Yes [ ]
SM5	50GBASE-R PCS deskew state diagram	133.2.4	Meets the requirements of Figure 82–14	M	Yes [ ]
SM6	50GBASE-R BER Monitor	133.2.4	Meets the requirements of Figure 82–15 with xus_timer_done set to 1 ms	M	Yes [ ]
SM7	50GBASE-R Transmit process	133.2.4	Meets the requirements of Figure 82–16	M	Yes [ ]
SM8	50GBASE-R Receive process	133.2.4	Meets the requirements of Figure 82–17	M	Yes [ ]

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133.5.4.9 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports loopback	82.4	Performs as in 82.4	M	Yes [ ]
L2	When in loopback, transmits what it receives from the 50GMII	82.4	Performs as in 82.4	M	Yes [ ]

133.5.4.10 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS Delay Constraint	133.3	No more than 11 264 bit times for sum of transmit and receive path delays for 50GBASE-R	M	Yes [ ]

133.5.4.11 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
*AN	Support for use with a 50GBASE-CR or 50GBASE-KR PMD	82.6	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN1	AN_LINK.indication primitive	82.6	Support of the primitive AN_LINK.indication(link_status)	AN:M	Yes [ ] N/A[ ]
AN2	link_status parameter	82.6	Takes the value OK or FAIL, as described in 82.6	AN:M	Yes [ ] N/A[ ]
AN2	Generation of AN_LINK.indication primitive	82.6	Generated when the value of link_status changes	AN:M	Yes [ ] N/A[ ]

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134. Reed-Solomon forward error correction (RS-FEC) sublayer for 50GBASE-R PHYs

134.1 Overview

134.1.1 Scope

This clause specifies a Reed-Solomon forward error correction (RS-FEC) sublayer for 50GBASE-R PHYs.

The RS-FEC sublayer for 50GBASE-R PHYs is identical to the RS-FEC sublayer for 100GBASE-R PHYs specified in Clause 91 with the following exceptions:

a) The service interface has four PCS lanes instead of 20 PCS lanes, and the nominal rate of each PCS lane is 12.890625 Gb/s rather than 5.15625 Gb/s. (See 134.2.)

b) It only implements the RS(544,514) Reed-Solomon encoder option defined in 91.5.2.7. (See 134.5.2.7.)

c) The output of the Reed-Solomon encoder is distributed to two FEC lanes, rather than the four FEC lanes described in 91.5.2.8.

d) The alignment marker processing is modified to account for the difference in the alignment marker format between the 50GBASE-R PCS (Clause 133) and the 100GBASE-R PCS (Clause 82), for the fact that the alignment markers are mapped to two FEC lanes rather than four FEC lanes, and the alignment marker mapping to the two FEC lanes needs to maintain a 10-bit alignment. (See 134.5.2.6.)

e) The definition of some of the variables and counters for the state diagrams in 91.5.4 are modified to support the different alignment marker spacing and the different number of FEC lanes. (See 134.5.4.)

f) The states identified as optional in the FEC synchronization state diagram in 91.5.4.3 (Figure 91–8) are mandatory for the 50GBASE-R RS-FEC.

g) The optional EEE deep sleep capability is not supported.

h) The optional FEC bypass correction feature (see 91.5.3.3) is not supported.

134.1.2 Position of RS-FEC in the 50GBASE-R sublayers

Figure 134–1 shows the relationship of the RS-FEC sublayer to the ISO/IEC Open System Interconnection (OSI) reference model.

134.2 FEC service interface

This subclause specifies the services provided by the RS-FEC sublayer. The service interface is described in an abstract manner and does not imply any particular implementation.

The FEC service interface is provided to allow the PCS to transfer information to and from the RS-FEC. The PCS may be connected to the RS-FEC using an optional instantiation of the PMA service interface (see Annex 135B) in which case a PMA is the client of the FEC service interface.

The FEC service interface is an instance of the inter-sublayer service interface defined in 131.3. The FEC service interface primitives are summarized as follows:

FEC:IS_UNITDATA_*i*.request
FEC:IS_UNITDATA_*i*.indication
FEC:IS_SIGNAL.indication

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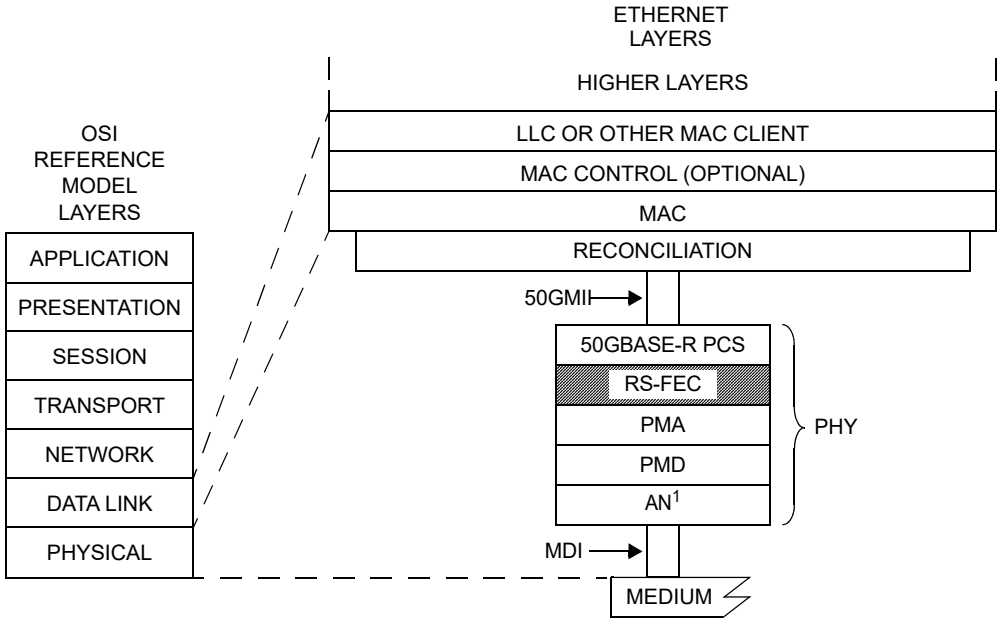

50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 134–1—RS-FEC relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The RS-FEC operates on four parallel bit streams, hence i = 0 to 3.

The PCS or PMA continuously sends four parallel bit streams to the RS-FEC, one per PCS lane, each at a nominal signaling rate of 12.890625 Gb/s. The RS-FEC continuously sends four parallel bit streams to the PCS or PMA, one per PCS lane, each at a nominal signaling rate of 12.890625 Gb/s.

The SIGNAL_OK parameter of the FEC:IS_SIGNAL.indication primitive can take one of two values: OK or FAIL. The value is set to OK when the FEC receive function has identified codeword boundaries as indicated by fec_align_status equal to true. That value is set to FAIL when the FEC receive function is unable to reliably establish codeword boundaries as indicated by fec_align_status equal to false. When SIGNAL_OK is FAIL, the rx_symbol parameters of the FEC:IS_UNITDATA_*i*.indication primitives are undefined.

134.3 PMA compatibility

The RS-FEC sublayer requires that the PMA service interface consist of exactly two upstream FEC lanes and exactly two downstream FEC lanes, with each lane running at a nominal signaling rate of 26.5625 Gb/s. Therefore, the RS-FEC sublayer may be a client of the 50GBASE-R PMA sublayer defined in Clause 135, when the PMA service interface width, p, is set to 2.

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134.4 Delay constraints

The maximum delay contributed by the RS-FEC sublayer (sum of transmit and receive delays at one end of the link) shall be no more than 25 600 bit times (50 pause_quanta or 512 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

134.5 Functions within the RS-FEC sublayer

134.5.1 Functional block diagram

A functional block diagram of the RS-FEC sublayer is shown in Figure 134–2.

134.5.2 Transmit function

134.5.2.1 PCS Lane block synchronization

The RS-FEC transmit function forms four bit streams by concatenating the bits from each of the four FEC:IS_UNITDATA_*i*.request primitives in the order they are received. It obtains lock to the 66-bit blocks in each bit stream using the sync headers and outputs 66-bit blocks. Block lock is obtained as specified in the block lock state diagram shown in Figure 82–12, but using the variable definitions from 133.2.4.

134.5.2.2 PCS Alignment lock and deskew

Once the RS-FEC transmit function achieves block lock on a PCS lane, it then begins obtaining alignment marker lock as specified by the alignment marker lock state diagram shown in Figure 82–13, but using the variable definitions from 133.2.4. This process identifies the PCS lane number received on a particular lane of the service interface. After alignment marker lock is achieved on all four PCS lanes, all inter-lane Skew is removed as specified by the PCS deskew state diagram shown in Figure 82–14, but using the variable definitions from 133.2.4. The RS-FEC transmit function shall support a maximum Skew of 49 ns and a maximum Skew Variation of 0.4 ns. Skew and Skew Variation are defined in 131.5.

134.5.2.3 PCS Lane reorder

PCS lanes can be received on different lanes of the service interface from which they were originally transmitted due to Skew between lanes and multiplexing by the PMA. The RS-FEC transmit function shall order the PCS lanes according to the PCS lane number.

134.5.2.4 Alignment marker removal

After all PCS lanes are aligned and deskewed, the PCS lanes are multiplexed together in the proper order to reconstruct the original stream of blocks and the alignment markers are removed from the data stream. Note that an alignment marker is always removed when am_lock is true for a given PCS lane even if it does not match the expected alignment marker value (due to a bit error for example). Repeated alignment marker errors result in am_lock being set to false for a given PCS lane, but until that happens it is sufficient to remove the block in the alignment marker position.

As part of the alignment marker removal process, the BIP_3 field is compared to the calculated Bit Interleaved Parity (BIP) value (see 82.2.8) for each PCS lane. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 1.230 to 1.233) is incremented by one each time the calculated BIP value does not equal the value received in the BIP_3 field. The bit error ratio in the data received from the local PCS can be estimated by dividing the BIP block error ratio by a factor of 1 351 680.

NOTE—The data received from the local PCS is processed by the RS-FEC transmit function without error correction.

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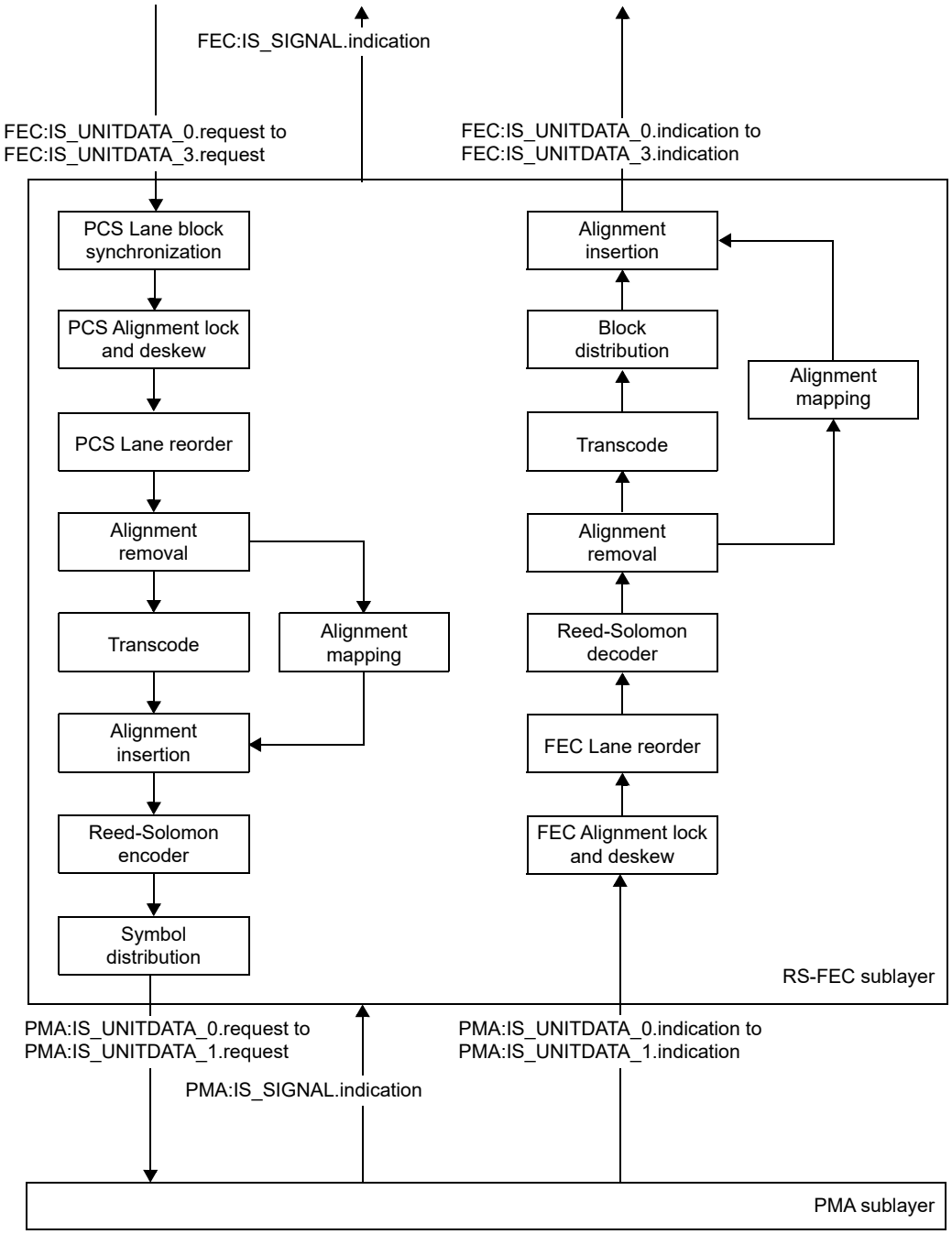

Figure 134–2—Functional block diagram

134.5.2.5 64B/66B to 256B/257B transcoder

The 64B/66B to 256B/257B transcoder is identical to the transcoder for the 100GBASE-R RS-FEC sublayer defined in 91.5.2.5.

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134.5.2.6 Alignment marker mapping and insertion

The alignment markers that were removed per 134.5.2.4 are re-inserted after being processed by the alignment marker mapping function. The alignment marker mapping function compensates for the operation of the symbol distribution function defined in 134.5.2.8 and rearranges the alignment marker bits so that they appear on the FEC lanes intact and in the desired sequence. This preserves the properties of the alignment markers (e.g., DC balance, transition density) and provides a deterministic pattern for the purpose of synchronization at the receiver. The RS-FEC receive function uses knowledge of this mapping to determine the FEC lane that is received on a given lane of the PMA service interface, to compensate for skew between FEC lanes, and to identify RS-FEC codeword boundaries.

The alignment marker mapping function operates on a group of four aligned and reordered alignment markers received from the PCS. Let am_tx_*x*<65:0> be the alignment marker for PCS lane *x*, *x*=0 to 3, where bit 0 is the first bit transmitted. The alignment markers shall be mapped to am_txmapped<256:0> in a manner that yields the same result as the following process.

For *x*=0 to 3, amp_tx_*x*<63:0> is constructed as follows:

— Set $y = 0$ when $x \leq 1$, otherwise set $y = x$.

— amp_tx_*x*<23:0> is set to M_0, M_1, and M_2 as shown in Figure 82–9 (bits 25 to 2) using the values in Table 82–3 for PCS lane number *y*.

— amp_tx_*x*<31:24> = am_tx_*x*<33:26>

— amp_tx_*x*<55:32> is set to M_4, M_5, and M_6 as shown in Figure 82–9 (bits 57 to 34) using the values in Table 82–3 for PCS lane number *y*.

— amp_tx_*x*<63:56> = am_tx_*x*<65:58>

This process replaces the fixed bytes of the alignment markers received from the PCS, possibly with errors, with the values from Table 82–3. In addition it substitutes the fixed bytes of the alignment markers corresponding to PCS lane 1 with the fixed bytes for the alignment marker corresponding to PCS lane 0. The variable bytes of the alignment markers received from the PCS (BIP_3 and BIP_7) are unchanged. This simplifies the synchronization process at the RS-FEC receiver, as the receiver only needs to search for the fixed alignment marker bytes corresponding to PCS lane 0 on each FEC lane.

am_txpayloads<0,129:0> and am_txpayloads<1,125:0> are then constructed from amp_tx as follows:

— am_txpayloads<0, 63:0> = amp_tx_0<63:0>

— am_txpayloads<0, 127:64> = amp_tx_2<63:0>

— am_txpayloads<0, 129:128> = amp_tx_3<57:56>

— am_txpayloads<1, 63:0> = amp_tx_1<63:0>

— am_txpayloads<1, 119:64> = amp_tx_3<55:0>

— am_txpayloads<1, 125:120> = amp_tx_3<63:58>

This process is an intermediate step in the generation of am_txmapped<256:0>, and is illustrated in Figure 134–3.

Given *i*=0 to 1, *k*=0 to 12, and $y=i+2k$, am_txmapped<255:0> is constructed from am_txpayloads as follows:

— If ($y < 25$) then am_txmapped<(10*y*+9):10*y*> = am_txpayloads<*i*, (10*k*+9):10*k*>

— am_txmapped<255:250> = am_txpayloads<1, 125:120>

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A 1-bit pad is appended to the mapped alignment markers to yield the equivalent of one 257-bit block. The pad bit, am_txmapped<256>, shall be set to 0 or 1 in an alternating pattern.

am_txmapped<256:0> is inserted into the data path prior to the Reed-Solomon encoder (see Figure 134–4) every $4 \times 20\,480$ 66-bit blocks, corresponding to every 1024 Reed-Solomon codewords. The mapped alignment markers, am_txmapped<256:0> shall be inserted as the first 257 message bits to be transmitted every 1024th codeword. The first 257-bit block inserted after am_txmapped shall correspond to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective PCS lane.

The result of this alignment mapping process is that after Reed-Solomon encoding and symbol distribution (134.5.2.7 and 134.5.2.8 respectively), the alignment marker bit patterns shown in Figure 134–3 appear on the two FEC output lanes and aligned with the start of every 1024th FEC codeword. The FEC receiver uses this information to lock onto the two FEC lanes and to identify the FEC codeword boundaries.

An additional result of this alignment mapping process, is that the BIP_3 and BIP_7 fields from normal PCS alignment markers are carried across the link protected by FEC. These fields cannot be used to monitor errors on the link protected by FEC as 64B/66B to 256B/257B transcoding and Reed-Solomon encoding alters the bit sequence. However, these fields may again be used to monitor errors after the original bit sequence is restored, i.e., following Reed-Solomon decoding and 256B/257B to 64B/66B transcoding.

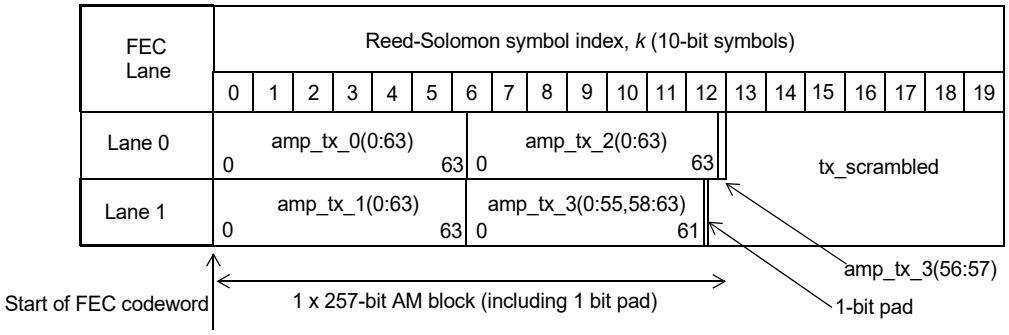

Figure 134–3—Alignment marker mapping to FEC lanes

134.5.2.7 Reed-Solomon encoder

The Reed-Solomon encoder is identical to the RS(544,514) Reed-Solomon encoder defined in 91.5.2.7.

134.5.2.8 Symbol distribution

Once the data has been Reed-Solomon encoded, it is distributed to two FEC lanes, one 10-bit symbol at a time alternating between FEC lanes 0 and 1. The distribution process is shown in Figure 134–4.

134.5.2.9 Transmit bit ordering

The transmit bit ordering is illustrated in Figure 134–4.

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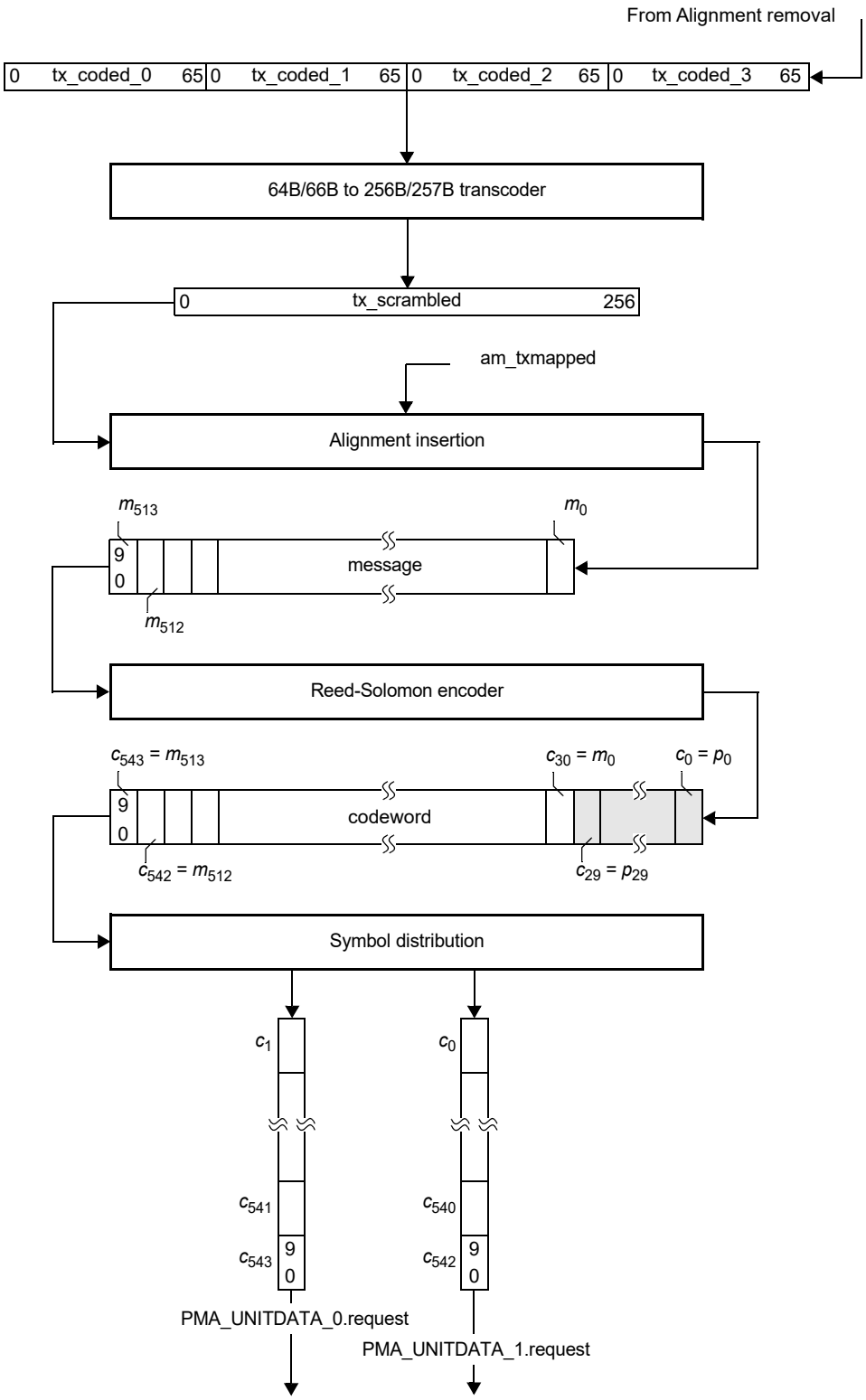

Figure 134–4—Transmit bit ordering

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134.5.3 Receive function

134.5.3.1 Alignment lock and deskew

The RS-FEC receive function forms two bit streams by concatenating the bits from each of the two PMA:IS_UNITDATA_*i*.indication primitives in the order they are received. It obtains lock to the alignment markers as specified by the FEC synchronization state diagram shown in Figure 91–8, but using the variable definitions from 134.5.4.

After alignment marker lock is achieved on the two FEC lanes, all inter-lane Skew is removed as specified by the FEC alignment state diagram shown in Figure 91–9. The FEC receive function shall support a maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns.

134.5.3.2 FEC Lane reorder

FEC lanes can be received on different lanes of the service interface from which they were originally transmitted. The FEC receive function shall order the FEC lanes according to the FEC lane number (see 134.5.2.6). The FEC lane number is defined by the sequence of alignment markers that are mapped to each FEC lane.

After both FEC lanes are aligned, deskewed, and reordered, the FEC lanes are multiplexed together in the proper order to reconstruct the original stream of FEC codewords.

134.5.3.3 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the codeword, corrects them as necessary, and discards the parity symbols.

The RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword. The RS-FEC sublayer shall also be capable of indicating when an errored codeword was not corrected. The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10^{-16}. This limit is also expected to apply for t+2 errors, t+3 errors, and so on.

The Reed-Solomon decoder shall indicate errors to the PCS sublayer by intentionally corrupting 66-bit block synchronization headers. When the decoder determines that a codeword contains errors that were not corrected, it ensures that for every other 257-bit block within the codeword starting with the first (1st, 3rd, 5th, etc.), the synchronization header for the first 66-bit block at the output of the 256B/257B to 64B/66B transcoder, rx_coded_0<1:0>, is set to 11. In addition, it shall ensure that rx_coded_0<1:0> corresponding to the second 257-bit block and rx_coded_3<1:0> corresponding to the last (20th) 257-bit block in the codeword are set to 11. Setting rx_coded_0<1:0> to 11 as described causes the PCS to assign R_BLOCK_TYPE=E to the 66-bit block and decode its content as EBLOCK_R (see 49.2.13.2.1 and 49.2.13.2.3). This causes the PCS to discard all frames 64 bytes and larger that are fully or partially contained within the codeword.

134.5.3.3.1 FEC Error indication bypass (optional)

The Reed-Solomon decoder may optionally provide the ability to bypass the error indication feature to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_indication_ability variable (see 134.6.6). When the option is provided it is enabled by the assertion of the FEC_bypass_indication_enable variable (see 134.6.1).

When FEC_bypass_indication_enable is asserted, additional error monitoring is performed by the RS-FEC sublayer to reduce the likelihood that errors in a packet are not detected. The Reed-Solomon decoder counts the number of symbol errors detected in consecutive non-overlapping blocks of 8192 codewords. When the

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number of symbol errors in a block of 8192 codewords exceeds 6380, the Reed-Solomon decoder shall cause synchronization header rx_coded<1:0> of each subsequent 66-bit block that is delivered to the PCS to be assigned a value of 00 or 11 for a period of 60 ms to 75 ms. As a result, the PCS sets hi_ber = true, which inhibits the processing of received packets. When Auto-Negotiation is supported and enabled, assertion of hi_ber causes Auto-Negotiation to restart.

134.5.3.3.2 FEC Degraded SER (optional)

The Reed-Solomon decoder may optionally provide the ability to indicate a degradation of the received signal. The presence of this option is indicated by the assertion of the FEC_degraded_SER_ability variable (see 134.6.8). When the option is provided it is enabled by the assertion of the FEC_degraded_SER_enable variable (see 134.6.2).

When FEC_degraded_SER_enable is asserted, additional error monitoring is performed by the FEC. The Reed-Solomon decoder counts the total number of symbol errors detected in consecutive non-overlapping blocks of FEC_degraded_SER_interval codewords (see 134.6.5). If the decoder determines that a codeword is uncorrectable, the number of symbol errors detected is increased by 16. When the number of symbol errors exceeds the threshold set in FEC_degraded_SER_activate_threshold (see 134.6.3), the FEC_degraded_SER bit (see 134.6.9) is set. At the end of each interval, if the number of symbol errors is less than the threshold set in FEC_degraded_SER_deactivate_threshold (see 134.6.4), the FEC_degraded_SER bit is cleared. The value of the FEC_degraded_SER bit is unspecified if the value of FEC_degraded_SER_activate_threshold is less than the value of FEC_degraded_SER_deactivate_threshold.

If either FEC_degraded_SER_ability or FEC_degraded_SER_enable is deasserted then the FEC_degraded_SER bit is cleared.

134.5.3.4 Alignment marker removal

The first 257 message bits in every 1024th codeword is the vector am_rxmapped<256:0> where bit 0 is the first bit received. The specific codewords that include this vector are indicated by the alignment lock and deskew function (see 134.5.3.1).

The vector am_rxmapped shall be removed prior to transcoding.

134.5.3.5 256B/257B to 64B/66B transcoder

The 256B/257B to 64B/66B transcoder is identical to the transcoder for the 100GBASE-R RS-FEC sublayer defined in 91.5.3.5.

134.5.3.6 Block distribution

After the data has been transcoded, it shall be distributed to four PCS lanes, one 66-bit block at a time in a round robin distribution from the lowest to the highest numbered PCS lanes. The distribution process is shown in Figure 82–6.

134.5.3.7 Alignment marker mapping and insertion

The alignment marker mapping function compensates for operation of the lane reorder function (see 134.5.2.3) to derive the PCS lane alignment markers, am_rx_*x*<65:0> for *x*=0 to 3, from am_rxmapped<256:0> (see 134.5.3.4).

The alignment markers shall be derived from am_rxmapped<256:0> in a manner that yields the same result as the following process.

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Given *i*=0 to 1, *k*=0 to 12, and *y*=*i*+2*k*, am_rxpayloads is constructed from am_rxmapped as follows:

— If (*y* < 25) then am_rxpayloads<*i*, (10*k*+9):10*k*> = am_rxmapped<(10*y*+9):10*y*>

— am_rxpayloads<1, 125:120> = am_rxmapped<255:250>

The one bit pad am_rxmapped<256> is ignored by the receiver.

For *x*=0 to 3, amp_rx_*x*<63:0> is constructed from am_rxpayloads as follows:

— amp_rx_0<63:0> = am_rxpayloads<0, 63:0>

— amp_rx_1<63:0> = am_rxpayloads<1, 63:0>

— amp_rx_2<63:0> = am_rxpayloads<0, 127:64>

— amp_rx_3<55:0> = am_rxpayloads<1, 119:64>

— amp_rx_3<57:56> = am_rxpayloads<0, 129:128>

— amp_rx_3<63:58> = am_rxpayloads<1, 125:120>

For *x*=0 to 3, am_rx_*x*<65:0> is constructed as follows:

— am_rx_*x*<0>=1 and am_rx_*x*<1>=0.

— am_rx_*x*<25:2> is set to M_0, M_1, and M_2 as shown in Figure 82–9 using the values in Table 82–3 for PCS lane number *x*.

— am_rx_*x*<33:26> = amp_rx_*x*<31:24>.

— am_rx_*x*<57:34> is set to M_4, M_5, and M_6 as shown in Figure 82–9 using the values in Table 82–3 for PCS lane number *x*.

— am_rx_*x*<65:58> = amp_rx_*x*<63:56>

One vector is mapped to four alignment markers every 1024 Reed-Solomon codewords (see 134.5.3.4). The alignment markers are simultaneously transmitted on the four PCS lanes after every 20 479th column of four 66-bit blocks.

The alignment markers am_rx_0 to am_rx_3 shall be inserted so that they are immediately followed by rx_coded_0 to rx_coded_3, respectively, as derived from the first 257-bit block following am_rxmapped.

134.5.3.8 Receive bit ordering

The receive bit ordering is illustrated in Figure 134–5. This illustration shows the case where the FEC lanes appear across the PMA:IS_UNITDATA_*i*.indication primitives in the correct order.

134.5.4 Detailed functions and state diagrams

The state diagrams, including the associated definitions of variables, functions and counters, are identical to those for the 100GBASE-R RS-FEC sublayer defined in 91.5.4, with the exception that some of the variables and counters are redefined to account for the differences in alignment marker spacing and number of FEC lanes.

In addition, EEE optional deep sleep capability is not supported for 50GBASE-R PHYs and therefore any reference to the optional EEE deep sleep capability in 91.5.4 can be ignored.

134.5.4.1 State diagram conventions

The state diagram conventions are identical to those defined in 91.5.4.1.

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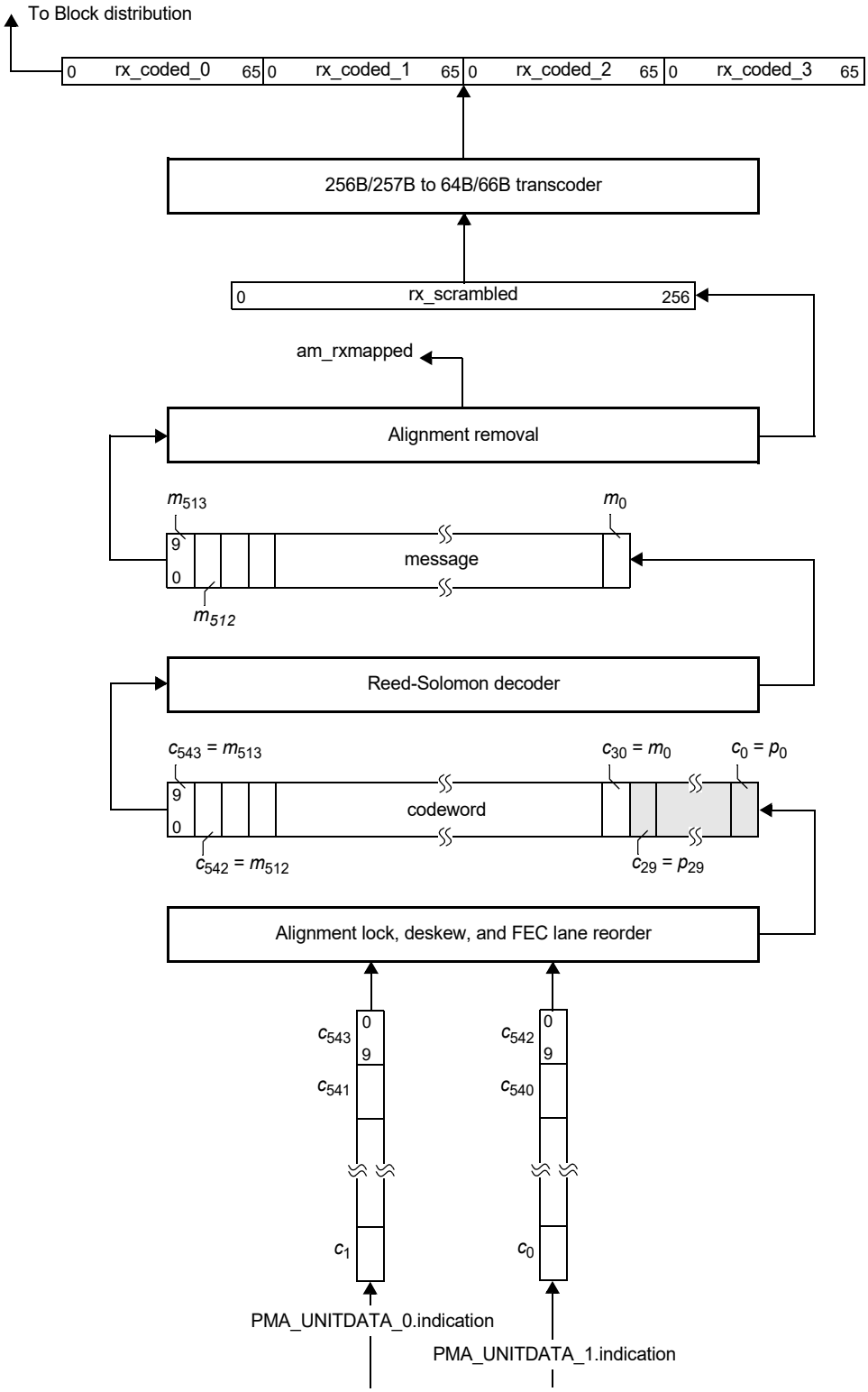

Figure 134–5—Receive bit ordering

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134.5.4.2 State variables

134.5.4.2.1 Variables

This following variables are redefined from what is described in 91.5.4.2.1:

amp_valid
: Boolean variable that is set to true if the received 64-bit block is a valid alignment marker payload. The alignment marker payload, mapped to an FEC lane according to the process described in 134.5.2.6, consists of 48 known bits and 16 variable bits (the BIP3 field and its complement BIP7 see 82.2.7). The bits of the candidate block that are in the positions of the known bits in the alignment marker payload are compared on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles in the alignment marker payload, the candidate block is considered a valid alignment marker payload. Each FEC lane compares the candidate block to the alignment marker payload for PCS lane 0.

amps_lock<*x*>
: Boolean variable that is set to true when the receiver has detected the location of the alignment marker payload sequence for a given lane on the PMA service interface, where $x = 0{:}1$.

fec_lane
: A variable that holds the FEC lane number (0 to 1) received on lane *x* of the PMA service interface when amps_lock<*x*> = true. The FEC lane number is determined by the alignment marker payloads in the 2nd position of the sequence based on the mapping defined in 134.5.2.6. The 48 bits that are in the positions of the known bits in the received alignment marker payload are compared to the expected values for a given payload position and FEC lane on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles on a given FEC lane, then the FEC lane number is assigned accordingly.

fec_lpi_fw
: Boolean variable that controls the behavior of the Transmit LPI and Receive LPI state diagrams. This variable is set to true when the local PCS is configured to use the fast wake mechanism and set to false otherwise. This variable shall always be set to true.

fec_optional_states
: Boolean variable that is always set to true to indicate that the optional states in the FEC synchronization state diagram in Figure 91–8 are implemented.

134.5.4.2.2 Functions

The functions are identical to those defined in 91.5.4.2.2.

134.5.4.2.3 Counters

This following counters are redefined from what is described in 91.5.4.2.3:

amp_counter
: This counter counts the 1024 FEC codewords that separate the ends of two consecutive normal alignment marker payload sequences. An FEC codeword is 2720 bits per FEC lane.

134.5.4.3 State diagrams

The state diagrams are identical to those defined in 91.5.4.3.

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134.6 RS-FEC MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the RS-FEC. If MDIO is implemented, it shall map MDIO control bits to RS-FEC control variables as shown in Table 134–1, and MDIO status bits to RS-FEC status variables as shown in Table 134–2, and if a separated PMA (see 45.2.1) is connected to the FEC service interface (e.g., if the RS-FEC and PCS are separated via a LAUI-2 interface) it shall map additional MDIO status bits to additional RS-FEC status variables as shown in Table 134–3.

Table 134–1—MDIO/RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass indication enable	RS-FEC control register	1.200.1	FEC_bypass_indication_enable
FEC degraded SER enable	RS-FEC control register	1.200.4	FEC_degraded_SER_enable
FEC degraded SER activate threshold	RS-FEC degraded SER activate threshold register	1.650, 1.651	FEC_degraded_SER_activate_threshold
FEC degraded SER deactivate threshold	RS-FEC degraded SER deactivate threshold register	1.652, 1.653	FEC_degraded_SER_deactivate_threshold
FEC degraded SER interval	RS-FEC degraded SER interval register	1.654, 1.655	FEC_degraded_SER_interval

Table 134–2—MDIO/RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass indication ability	RS-FEC status register	1.201.1	FEC_bypass_indication_ability
RS-FEC high SER	RS-FEC status register	1.201.2	hi_ser
FEC degraded SER ability	RS-FEC status register	1.201.3	FEC_degraded_SER_ability
FEC degraded SER	RS-FEC status register	1.201.4	FEC_degraded_SER
FEC optional states supported	RS-FEC status register	1.201.7	fec_optional_states
FEC AM lock *x*, *x*=0 to 1	RS-FEC status register	1.201.8:9	amps_lock<*x*>
RS-FEC align status	RS-FEC status register	1.201.14	fec_align_status
FEC corrected codewords	RS-FEC corrected codewords counter register	1.202, 1.203	FEC_corrected_cw_counter
FEC uncorrected codewords	RS-FEC uncorrected codewords counter register	1.204, 1.205	FEC_uncorrected_cw_counter
FEC lane *x* mapping	RS-FEC lane mapping register	1.206	FEC_lane_mapping<*x*>
FEC symbol errors, FEC lanes 0 to 1	RS-FEC symbol error counter register, FEC lanes 0 to 1	1.210 to 1.213	FEC_symbol_error_counter_*i*

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Table 134–3—MDIO/RS-FEC status variable mapping for separated PMA

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
PCS align status	RS-FEC status register	1.201.15	align_status
BIP errors, PCS lanes 0 to 3	RS-FEC BIP error counter register, PCS lanes 0 to 3	1.230 to 1.233	BIP_error_counter_*i*
PCS lane *x* mapping	PCS lane *x* mapping register	1.250 to 1.253	lane_mapping<*x*>
Block *x* lock	RS-FEC PCS alignment status 1 register	1.280	block_lock<*x*>
Lane *x* aligned	RS-FEC PCS alignment status 3 register	1.282	am_lock<*x*>

The following subclauses define variables that are not otherwise defined, e.g., for use by state diagrams.

134.6.1 FEC_bypass_indication_enable

This variable is set to one to bypass the error indication function (see 134.5.3.3.1) when this ability is supported. When this variable is set to zero, the decoder indicates errors to the PCS sublayer. The default value of this variable is zero. This variable is mapped to the bit defined in 45.2.1.116.4 (1.200.1).

134.6.2 FEC_degraded_SER_enable

This variable enables the FEC decoder to indicate the presence of a degraded SER when the ability is supported (see 134.5.3.3.2). When set to a one, this variable enables degraded SER detection. When set to a zero, degraded SER detection is disabled. Writes to this bit are ignored and reads return a zero if the FEC does not have the ability to signal the presence of a degraded SER. This variable is mapped to the bit defined in 45.2.1.116.1 (1.200.4).

134.6.3 FEC_degraded_SER_activate_threshold

This variable controls the threshold used to set the FEC_degraded_SER bit as defined in 134.5.3.3.2. It is mapped to the registers defined in 45.2.1.146 (1.650, 1.651).

134.6.4 FEC_degraded_SER_deactivate_threshold

This variable controls the threshold used to clear the FEC_degraded_SER bit as defined in 134.5.3.3.2. It is mapped to the registers defined in 45.2.1.147 (1.652, 1.653).

134.6.5 FEC_degraded_SER_interval

This variable controls the interval used to set and clear the FEC_degraded_SER bit as defined in 134.5.3.3.2. It is mapped to the registers defined in 45.2.1.148 (1.654, 1.655).

134.6.6 FEC_bypass_indication_ability

The Reed-Solomon decoder may have the option to bypass the error indication function (see 134.5.3.3.1) to reduce the delay contributed by the RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass error indication. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.117.11 (1.201.1).

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134.6.7 hi_ser

This variable is defined when the FEC_bypass_indication_ability variable is set to one. When FEC_bypass_indication_enable is set to one, this bit is set to one if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 134.5.3.3) and is set to zero otherwise. This variable is mapped to the bit defined in 45.2.1.117.10 (1.201.2).

134.6.8 FEC_degraded_SER_ability

The FEC decoder may have the option to indicate the presence of a degraded SER (see 134.5.3.3.2). This variable is set to one to indicate that the FEC decoder has the ability to indicate the presence of a degraded SER. This variable is set to zero if this ability is not supported. It is mapped to the bit defined in 45.2.1.117.9 (1.201.3).

134.6.9 FEC_degraded_SER

When FEC_degraded_SER_enable is asserted, this variable indicates the presence of a degraded SER as defined in 134.5.3.3.2. This variable is mapped to the bit defined in 45.2.1.117.8 (1.201.4).

134.6.10 fec_optional_states

This variable is always set to true to indicate that the optional states in the FEC synchronization state diagram in Figure 91–8 are implemented. This variable is mapped to the bit defined in 45.2.1.117.8 (1.201.7).

134.6.11 amps_lock<*x*>

These variables are assigned by the FEC alignment state diagram shown in Figure 91–9 (see 91.5.4.3 and 134.5.4). They are mapped to the bits defined in 45.2.1.117 (1.201.8 to 1.201.9 for FEC lanes 0 to 1, respectively).

134.6.12 fec_align_status

This variable assigned by the FEC alignment state diagram shown in Figure 91–9 (see 91.5.4.3). It is mapped to the bit defined in 45.2.1.117.2 (1.201.14).

134.6.13 FEC_corrected_cw_counter

A corrected FEC codeword is a codeword that contains errors and was corrected.

FEC_corrected_cw_counter is a 32-bit counter that counts once for each corrected FEC codeword processed when fec_align_status is true. This variable is mapped to the registers defined in 45.2.1.118 (1.202, 1.203).

134.6.14 FEC_uncorrected_cw_counter

An uncorrected FEC codeword is a codeword that contains errors that were not corrected.

FEC_uncorrected_cw_counter is a 32-bit counter that counts once for each uncorrected FEC codeword processed when fec_align_status is true. This variable is mapped to the registers defined in 45.2.1.119 (1.204, 1.205).

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134.6.15 FEC_lane_mapping<*x*>

When the RS-FEC receive function detects and locks to an alignment marker payload on PMA service interface lane *x*, the FEC lane number corresponding to the detected alignment marker payload is assigned to the variable FEC_lane_mapping<*x*>. These variables are mapped to the register defined in 45.2.1.120 (1.206).

134.6.16 FEC_symbol_error_counter_*i*

FEC_symbol_error_counter_*i*, where *i*=0 to 1, is a 32-bit counter that counts once for each 10-bit symbol corrected on FEC lane *i* when fec_align_status is true. These variables are mapped to the registers defined in 45.2.1.121 and 45.2.1.122 (1.210 to 1.213).

134.6.17 align_status

This variable is assigned the value of rx_align_status as defined by the PCS deskew state diagram shown in Figure 82–14 (see 134.5.2.2). It is mapped to the bit defined in 45.2.1.117.1 (1.201.15).

134.6.18 BIP_error_counter_*i*

BIP_error_counter_*i*, where *i*=0 to 3, is a 16-bit counter that holds the BIP error count for PCS lane *i* as calculated by the RS-FEC transmit function (see 134.5.2.4). These variables are mapped to the registers defined in 45.2.1.123 and 45.2.1.124 (1.230 to 1.233).

134.6.19 lane_mapping<*x*>

When the RS-FEC transmit function detects and locks to an alignment marker on FEC service interface lane *x*, the PCS lane number corresponding to the detected alignment marker is assigned to the variable lane_mapping<*x*>. These variables are mapped to the registers defined in 45.2.1.125 and 45.2.1.126 (1.250 to 1.253).

134.6.20 block_lock<*x*>

These variables are assigned by the block lock state diagram shown in Figure 82–12 (see 134.5.2.1). They are mapped to the registers defined in 45.2.1.127 (1.280).

134.6.21 am_lock<*x*>

These variables are assigned by the alignment marker lock state diagram shown in Figure 82–13 (see 134.5.2.2). They are mapped to the registers defined in 45.2.1.129 (1.282).

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134.7 Protocol implementation conformance statement (PICS) proforma for Clause 134, Reed-Solomon forward error correction (RS-FEC) sublayer for 50GBASE-R PHYs[225]

134.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 134, Reed-Solomon forward error correction (RS-FEC) sublayer for 50GBASE-R PHYs, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

134.7.2 Identification

134.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

134.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 134, Reed-Solomon forward error correction (RS-FEC) sublayer for 50GBASE-R PHYs
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[225] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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134.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
RS-FEC	Supports 50GBASE-R RS-FEC functionality	134.1.1		M	Yes [ ]
*MD	MDIO capability	45, 134.6	Registers and interface supported	O	Yes [ ] No [ ]
*BEI	Bypass error indication	134.5.3.3.1	Capability is supported	O	Yes [ ] No [ ]
*FDD	Support for optional FEC degraded SER detection	134.5.3.3.2		O	Yes [ ] No [ ]

134.7.4 PICS proforma tables for Reed-Solomon forward error correction (RS-FEC) sublayer for 50GBASE-R PHYs

134.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Skew tolerance	134.5.2.2	Maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps.	M	Yes [ ]
TF2	Lane reorder	134.5.2.3	Order the PCS lanes according to the PCS lane number	M	Yes [ ]
TF3	64B/66B to 256B/257B transcoder	134.5.2.5	tx_xcoded<256:0> constructed per 134.5.2.5	M	Yes [ ]
TF4	257-bit block transmission order	134.5.2.5	First bit transmitted is bit 0	M	Yes [ ]
TF5	Alignment maker mapping	134.5.2.6	Map to am_txmapped<256:0> per 134.5.2.6	M	Yes [ ]
TF6	Pad value	134.5.2.6	Set to 0 or 1 in an alternating pattern	M	Yes [ ]
TF7	Alignment marker insertion	134.5.2.6	First 257 message bits to be transmitted from every 1024th codeword	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TF8	First 257-bit block inserted after am_txmapped	134.5.2.6	First 257-bit block inserted after am_txmapped corresponds to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective lane	M	Yes [ ]
TF9	Reed-Solomon encoder	134.5.2.7		M	Yes [ ]
TF10	Symbol distribution	134.5.2.8	Distributed to 2 FEC lanes, one 10-bit symbol at a time alternating between FEC lanes 0 and 1	M	Yes [ ]

134.7.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	134.5.3.1	Maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	Lane reorder	134.5.2.3	Order the FEC lanes according to the FEC lane number	M	Yes [ ]
RF3	Reed-Solomon decoder for RS(544,514)	134.5.3.3	Corrects any combination of up to t=15 symbol errors in a codeword.	M	Yes [ ]
RF4	Reed-Solomon decoder	134.5.3.3	Capable of indicating when a codeword was not corrected.	M	Yes [ ]
RF5	Error indication function	134.5.3.3	Corrupts 66-bit block synchronization headers for uncorrected errored codewords.	M	Yes [ ]
RF6	Error monitoring while error indication is bypassed	134.5.3.3.1	When the number of symbols errors in a block of 8192 codewords exceeds K, corrupt 66-bit block synchronization headers	BEI:M	Yes [ ] N/A [ ]
RF7	Symbol error threshold for RS(544,514)	134.5.3.3.1	K=6380	BEI:M	Yes [ ] N/A [ ]
RF8	FEC decoder detects FEC degraded SER at a program-mable threshold	134.5.3.3.2		FDD:M	Yes [ ] N/A [ ]
RF9	Alignment marker removal	134.5.3.4	am_rxmapped removed prior to transcoding	M	Yes [ ]
RF10	256B/257B to 64B/66B transcoder	134.5.3.5	rx_coded_j<65:0>, j=0 to 3 constructed per 134.5.3.5	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RF11	Block distribution	134.5.3.6	One 66-bit block at a time in a round robin fashion from the lowest to the highest numbered PCS lane	M	Yes [ ]
RF12	Alignment marker mapping	134.5.3.7	Map to am_rx_*x*, *x*=0 to 3 per 134.5.3.7	M	Yes [ ]
RF13	Alignment marker insertion point	134.5.3.7	Alignment markers immediately followed by the 66-bit blocks derived from the 257-bit blocks immediately following am_rxmapped	M	Yes [ ]

134.7.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	SLIP function	134.5.4.2.2	Ensure that all possible block positions are evaluated	M	Yes [ ]
SD2	Synchronization process	134.5.4.3	One instance per FEC lane per Figure 91–8	M	Yes [ ]
SD3	Alignment process	134.5.4.3	Per Figure 91–9	M	Yes [ ]

134.7.4.4 Delay Constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	RS-FEC Delay Constraint	134.4	No more than 25 600 bit times for sum of transmit and receive path delays	M	Yes [ ]

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135. Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P

135.1 Overview

135.1.1 Scope

This clause specifies the Physical Medium Attachment sublayer (PMA) for the families of 50 Gb/s and 100 Gb/s PAM4 Physical Layer implementations known as 50GBASE-R (see 131.1.3) and 100GBASE-P (see 80.1.4). The PMA allows the PCS (see Clause 133 and Clause 82) and FEC (see Clause 134 and Clause 91) to connect in a media-independent way with a range of physical media. The 50GBASE-R PMA can support any of the 50 Gb/s PMDs in Table 131–1 and the 100GBASE-P PMA can support any of the 100 Gb/s PAM4 PMDs according to Table 80–3 and Table 80–5.

50GBASE-R and 100GBASE-P PHYs can be extended to support any full duplex medium requiring only that the PMD be compliant with the appropriate PMA interface.

The interfaces for the inputs of the 50GBASE-R and 100GBASE-P PMAs are defined in an abstract manner and do not imply any particular implementation. For 50GBASE-R PMAs, electrical interfaces connecting PMA sublayers, known as LAUI-2 and 50GAUI-n, are defined in Annex 135B through Annex 135G. For 100GBASE-P PMAs, electrical interfaces connecting PMA sublayers, known as 100GAUI-n, are defined in Annex 135D through Annex 135G.

135.1.2 Position of the PMA in the 50GBASE-R and 100GBASE-P sublayers

Figure 135–1 shows the relationship of the PMA sublayer (shown shaded) with other sublayers to the ISO Open System Interconnection (OSI) reference model.

135.1.3 Summary of functions

The following is a summary of the principal functions implemented (when required) by the PMA in both the transmit and receive directions:

a) Adapt the PCSL/FECL-formatted signal to the appropriate number of abstract or physical lanes.
b) Provide per-input-lane clock and data recovery.
c) Provide bit-level multiplexing.
d) Provide clock generation.
e) Provide signal drivers.
f) Optionally provide local loopback to/from the PMA service interface.
g) Optionally provide remote loopback to/from the PMD service interface.
h) Optionally provide test-pattern generation and checking.
i) Tolerate Skew Variation.
j) Perform PAM4 encoding and decoding, including Gray mapping and optional precoding, when required.

PAM4 encoding and decoding is required for 50GBASE-R PMAs where the number of physical lanes is 1 and for 100GBASE-P PMAs where the number of physical lanes is 1 or 2.

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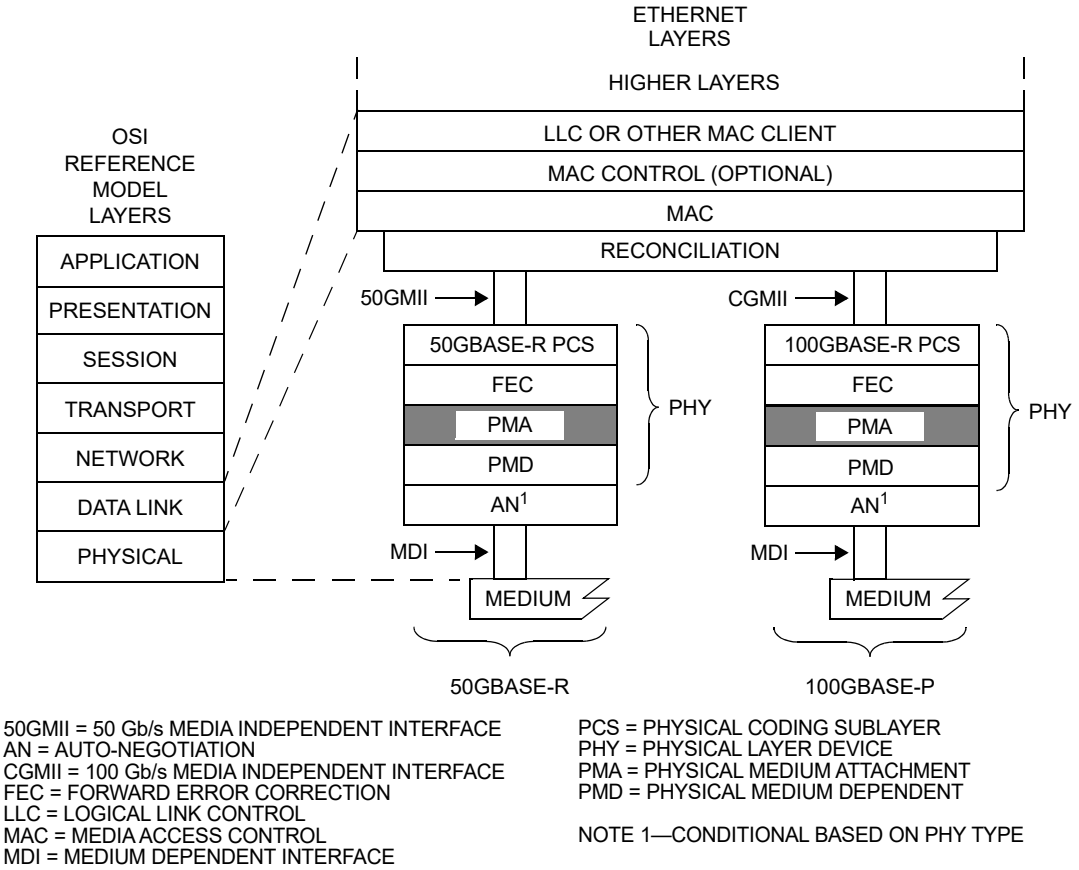

Figure 135–1—50GBASE-R and 100GBASE-P PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

135.1.4 PMA sublayer positioning

An implementation may use one or more PMA sublayers to adapt the number and rate of the PCS lanes to the number and rate of the PMD lanes. The number of PMA sublayers required depends on the partitioning of functionality for a particular implementation. An example is illustrated in Figure 135–2. Additional examples are illustrated in Annex 135A. Each PMA maps the PCSLs/FECLs from p PMA input lanes to q PMA output lanes in the Tx direction, and from q PMA input lanes to p PMA output lanes in the Rx direction.

Management Data Input/Output (MDIO) Manageable Device (MMD) addresses 1, 8, 9, and 10 are available for addressing multiple instances of PMA sublayers (see Table 45–1 for MMD device addresses). If the PMA sublayer that is closest to the PMD is packaged with the PMD, it shares MMD 1 with the PMD. More addressable instances of PMA sublayers, each one separated from lower addressable instances by chip-to-chip interfaces, may be implemented and addressed allocating MMD addresses to PMAs in increasing numerical order going from the PMD toward the MAC. The examples shown in Figure 135–2 could be implemented with three addressable instances: MMD 1 addressing the lowest PMA sublayer (co-packaged with the PMD), MMD 8 addressing the middle PMA sublayer, and MMD 9 addressing the highest PMA sublayer (immediately below the FEC).

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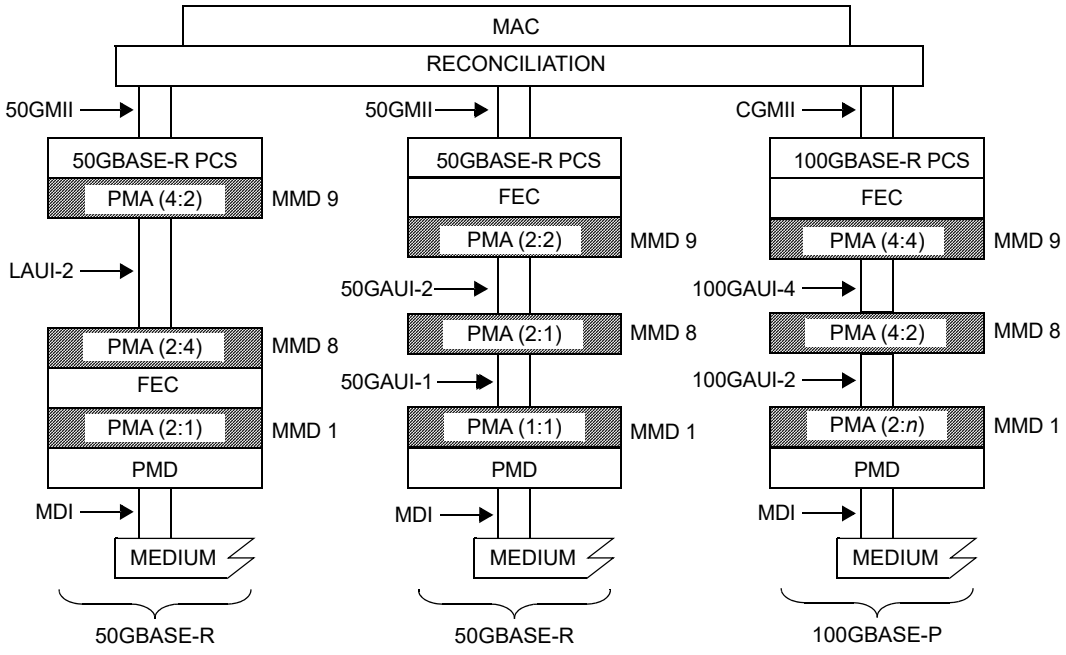

100GAUI = 100 Gb/s ATTACHMENT UNIT INTERFACE
50GAUI = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LAUI = 50 Gb/s ATTACHMENT UNIT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

n = 1 or 2

Figure 135–2—Example 50GBASE-R and 100GBASE-P PMA layering

The number of input lanes and the number of output lanes for a PMA are always divisors of the number of PCSLs/FECLs. For PMA sublayers supporting 50GBASE-R PMDs, the number of PCSLs (above the FEC) is 4 and the number of FECLs (below the FEC) is 2. For PMA sublayers supporting 100GBASE-P PMDs, the number of FECLs is 4.

The following guidelines apply to the partitioning of PMAs:

a) The inter-sublayer service interface, defined in 131.3.1, is used for the PMA service interfaces supporting a flexible architecture with multiple PMA sublayers.
   1) An instance of this interface can only connect service interfaces with the same number of lanes, where the lanes operate at the same rate.

b) The abstract PMA service interface can be physically instantiated as a LAUI-2, 50GAUI-n, or 100GAUI-n, using associated PMAs to map to the appropriate number of lanes.

c) For physical instantiations of the PMA service interface, the PMA:IS_SIGNAL.indication is conveyed outside of this physically instantiated interface.

d) Physical instantiations of the PMA service interface define electrical and timing specification as well as requiring a receive re-timing function.

e) LAUI-2 is a physical instantiation of the PMA service interface between two adjacent 50GBASE-R PMA sublayers above the FEC.
   1) LAUI-2 provides bit-multiplexing of 4 PCSLs.
   2) LAUI-2 is a 25.78125 GBd by two-lane NRZ physical instantiation of the 50 Gb/s connection.

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f) 50GAUI-n is a physical instantiation of the PMA service interface between two adjacent 50GBASE-R PMA sublayers below the FEC and contains 2 FECLs.
   1) 50GAUI-n provides bit-multiplexing of 2 FECLs.
   2) 50GAUI-2 is a 26.5625 GBd by two-lane NRZ physical instantiation of the 50 Gb/s connection.
   3) 50GAUI-1 is a 26.5625 GBd by one-lane PAM4 physical instantiation of the 50 Gb/s connection.

g) CAUI-n is a physical instantiation of the PMA service interface between two adjacent 100GBASE-R PMA (see Clause 83) sublayers above the FEC for a 100GBASE-P PHY or between adjacent sublayers below the PCS for a 100GBASE-R PHY. CAUI-n is not specified in this clause, but is listed here for completeness.
   1) CAUI-n provides bit-multiplexing of 20 PCSLs.
   2) CAUI-4 is a 25.78125 GBd by four-lane NRZ physical instantiation of the 100 Gb/s connection. CAUI-4 is specified in Clause 83 and associated annexes.
   3) CAUI-10 is a 10.3125 GBd by ten-lane NRZ physical instantiation of the 100 Gb/s connection. CAUI-10 is specified in Clause 83 and associated annexes.

h) 100GAUI-n is a physical instantiation of the PMA service interface between two adjacent 100GBASE-P PMA sublayers below the FEC for a 100GBASE-P PHY.
   1) 100GAUI-n provides bit-multiplexing of 4 FECLs.
   2) 100GAUI-4 is a 26.5625 GBd by four-lane NRZ physical instantiation of the 100 Gb/s connection.
   3) 100GAUI-2 is a 26.5625 GBd by two-lane PAM4 physical instantiation of the 100 Gb/s connection.

i) Opportunities for optional test-pattern generation, optional test-pattern detection, optional local loopback and optional remote loopback are dependent upon the location of the PMA sublayer in the implementation. See Figure 135–5.

j) A minimum of one PMA sublayer is required in a PHY.

k) A maximum of four PMA sublayers are addressable as MDIO MMDs.

135.2 PMA interfaces

All PMA variants for 50GBASE-R and 100GBASE-P are based on a generic specification of a bit mux function that applies to all input/output lane counts and each direction of transmission. Each direction of transmission may employ one or more such bit muxes to adapt from the appropriate number of input lanes to the appropriate number of output lanes as illustrated in Figure 135–3.

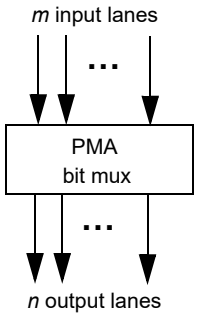

Figure 135–3—PMA bit mux used in both Tx and Rx directions

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Conceptually, the PMA bit mux operates in one direction of transmission by demultiplexing PCSLs/FECLs from *m* PMA input lanes and remultiplexing them into *n* PMA output lanes. The mapping of PCSLs/FECLs from input to output lanes is not specified. See 135.5.2 and Figure 135–4 for details.

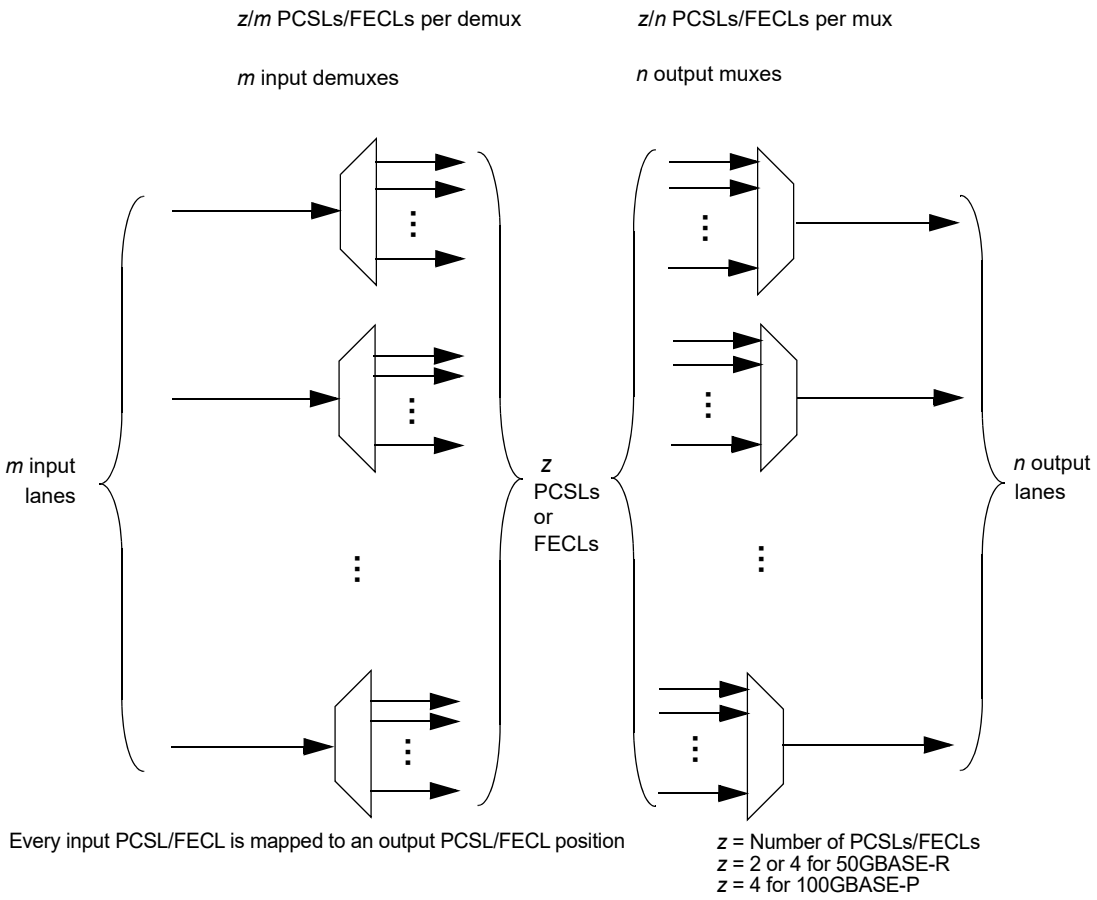

Figure 135–4—PMA bit mux operation used in both Tx and Rx directions

135.3 PMA service interface

The PMA service interface for 50GBASE-R and 100GBASE-P is an instance of the inter-sublayer service interface defined in 131.3.1. The PMA service interface primitives are summarized as follows:

PMA:IS_UNITDATA_*i*.request
PMA:IS_UNITDATA_*i*.indication
PMA:IS_SIGNAL.indication

For a PMA service interface with *p* lanes, the primitives are defined for $i = 0$ to $p - 1$.

If the PMA client is the 50GBASE-R PCS, the PMA continuously sends four parallel bit streams to the PCS, each at the nominal signaling rate of the PCSL.

If a PMA client is another PMA, a 50GBASE-R PMA with p=2 physical input lanes receives NRZ symbols on each of its input lanes at the FECL rate or at 2 times the PCSL rate. A 50GBASE-R PMA with p=1

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physical input lane receives PAM4 symbols on that input lane at the FECL rate, with each symbol formed from two bits.

If a PMA client is another PMA, 100GBASE-P PMA with *p*=4 physical input lanes receives NRZ symbols on each of its input lanes at the FECL rate. A 100GBASE-P PMA with *p*=1 or *p*=2 physical input lanes receives PAM4 symbols on each of its input lanes at 2 or 1 times, respectively, the FECL rate, with each symbol formed from two bits. The bit stream represented by the input symbols carries *z*/*p* bit-multiplexed FECLs on each physical input lane, where *z*=4 for 100GBASE-P.

Skew may exist between different PCSLs/FECLs received on the same physical input lane even though all PCSLs/FECLs originate from the same synchronous source, so there is independence of arrival of bits from each PCSL/FECL on each physical input lane.

In the Tx direction, if the symbol from a PMA:IS_UNITDATA_*i*.request primitive is received over a physically instantiated interface (LAUI-2, 50GAUI-n, or 100GAUI-n), clock and data are recovered on the lane receiving the symbol. If necessary, PAM4 symbols are converted to pairs of bits. Bits are routed through the PMA to an output lane through a process that may demultiplex PCSLs/FECLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs/FECLs to output lanes. If necessary, pairs of bits on output lanes are converted to PAM4 symbols. The symbols are sent on an output lane to the sublayer below using the *inst*:IS_UNITDATA_*k*.request (*k* not necessarily equal to *i*) primitive (see 135.4).

In the Rx direction, the PMA passes the bits represented by the symbols from the input lane(s) received from the sublayer below the PMA into encoded symbols on the output lanes. If necessary, buffers are filled to allow tolerating the Skew Variation that may appear between the input lanes. PCSLs/FECLs are demultiplexed from the input lanes, remultiplexed to the output lanes, and symbols are transferred over each output lane to the PMA client via the PMA:IS_UNITDATA_i.indication primitive.

The PMA:IS_SIGNAL.indication primitive is generated by a Signal Indication Logic (SIL) function that reports signal health based on receipt of the *inst*:IS_SIGNAL.indication from the sublayer below, data being received on all of the input lanes from the sublayer below, buffers filled (if necessary) to accommodate Skew Variation, and symbols being sent to the PMA client on all of the output lanes. When these conditions are met, the SIGNAL_OK parameter sent to the PMA client via the PMA:IS_SIGNAL.indication primitive has the value OK. Otherwise, the SIGNAL_OK primitive has the value FAIL.

135.4 Service interface below PMA

Since the architecture supports multiple PMA sublayers for various PMD lane counts and device partitioning, there are several different sublayers that may appear below a PMA, including the FEC, PMD, or another PMA. The variable *inst* represents whichever sublayer appears below the PMA (e.g., another PMA, FEC, or PMD).

The sublayer below the PMA utilizes the inter-sublayer service interface defined in 131.3. The service interface primitives provided to the PMA are summarized as follows:

inst:IS_UNITDATA_*i*.request
inst:IS_UNITDATA_*i*.indication
inst:IS_SIGNAL.indication

The number of lanes *q* for the service interface matches the number of lanes expected by the PMA. The *inst*:IS_UNITDATA_*i* primitives are defined for each lane $i = 0$ to $q - 1$ of the service interface below the PMA. Note that electrical and timing specifications of the service interface are defined if the interface is physically instantiated (e.g., LAUI-2, 50GAUI-n, or 100GAUI-n), otherwise the service interface is

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specified only abstractly. The interface between the PMA and the sublayer below consists of *q* lanes for data transfer and a status indicating a good signal from the sublayer below the PMA (see Figure 135–5).

In the Tx direction, the PMA passes the bits represented by the symbols from the input lane(s) received via the PMA:IS_UNITDATA_i.request primitive(s) into encoded symbols on the output lanes. If necessary, buffers are filled to provide the ability to tolerate the Skew Variation that may appear between the input lanes from the PMA client. PCSLs/FECLs are demultiplexed from the input lanes, remultiplexed to the output lanes, and symbols are transferred over each output lane to the sublayer below the PMA.

In the Rx direction, if the symbol is received over a physically instantiated interface (50GAUI-n, 100GAUI-n, or physically instantiated PMD service interface), clock and data are recovered on the lane receiving the symbol. If necessary, PAM4 symbols received on the input lanes are converted to pairs of bits. The bits are routed through the PMA to an output lane toward the PMA client through a process that may demultiplex PCSLs/FECLs from the input, perform any necessary buffering to tolerate Skew Variation across input lanes, and multiplex PCSLs/FECLs to output lanes. If necessary, pairs of bits are converted to PAM4 symbols on the output lanes. Each symbol is sent on an output lane to the PMA client using the PMA:IS_UNITDATA_*k*.indication (*k* not necessarily equal to *i*) primitive at the PMA service interface.

135.5 Functions within the PMA

The purpose of the PMA is to adapt the PCSL/FECL-formatted signal to an appropriate number of abstract or physical lanes, to recover clock from the received signal (if appropriate), and optionally to provide test signals and loopback. Each input (Tx direction) or output (Rx direction) lane between the PMA and the PMA client carries one or more PCSLs/FECLs that are bit-multiplexed. All input and output lanes between the PMA and the PMA client carry the same number of PCSLs/FECLs and operate at the same nominal signaling rate. Likewise, each input (Rx direction) or output (Tx direction) lane between the PMA and the sublayer below the PMA carries one or more PCSLs/FECLs that are bit-multiplexed. All input and output lanes between the PMA and the sublayer below the PMA carry the same number of PCSLs/FECLs and operate at the same nominal signaling rate. As described in 135.1.4, the number of input lanes and the number of output lanes for a given PMA are divisors of 2 (below the FEC) or 4 (above the FEC) for 50GBASE-R, or 4 for 100GBASE-P, which are the number of PCSLs/FECLs for the respective PHYs.

Figure 135–5 provides the functional block diagram of a PMA. The parameters of a PMA include the following:

- The numbers of input and output lanes in each direction.
- Whether the PMA is adjacent to a physically instantiated interface (LAUI-2, 50GAUI-n, or 100GAUI-n above or below).
- Whether the PMA is adjacent to the PCS.
- Whether the PMA is adjacent to the PMD.
- Whether the PMA is adjacent to the FEC.

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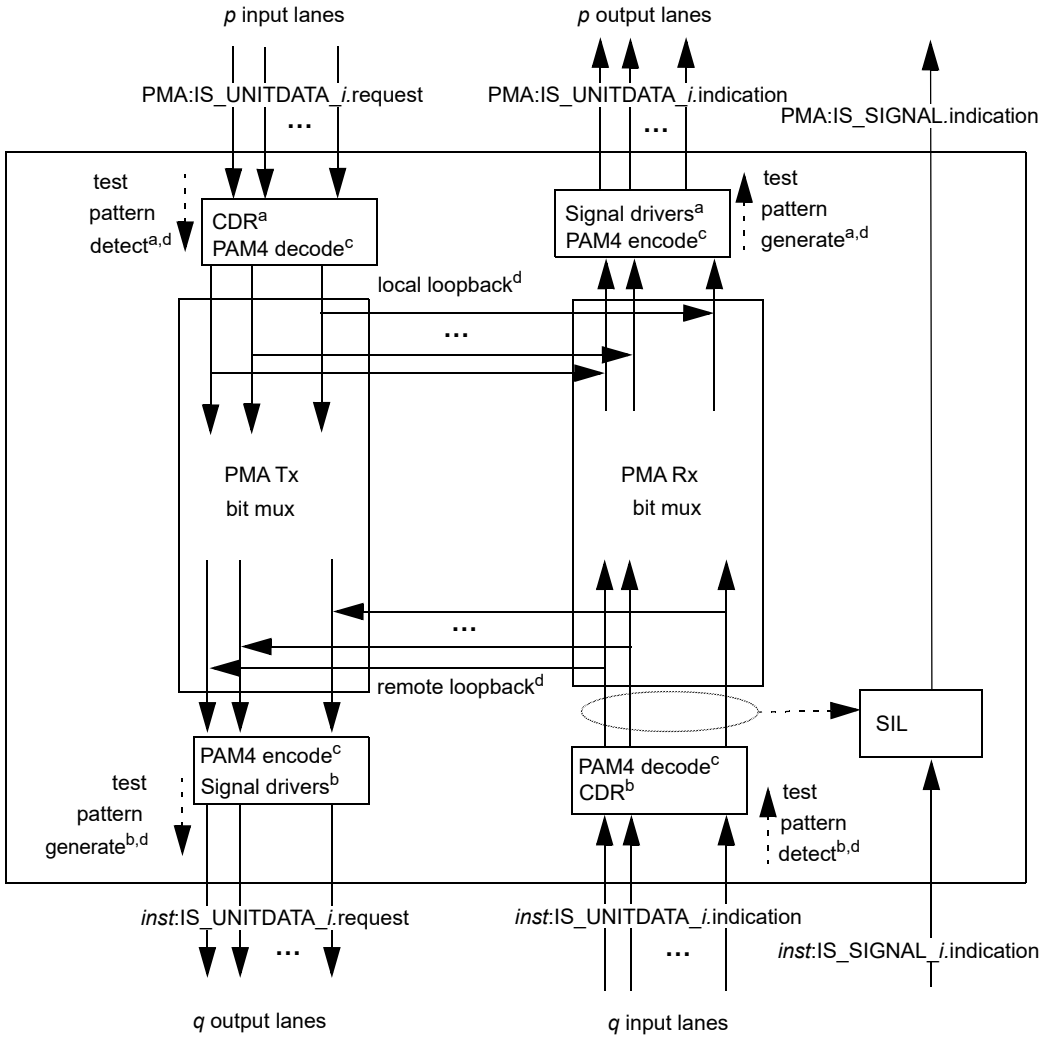

inst = PMD, PMA, depending on which sublayer is below this PMA
SIL = Signal Indication Logic

[a] If LAUI-2, 50GAUI-n, or 100GAUI-n immediately above this PMA.
[b] If LAUI-2, 50GAUI-n, or 100GAUI-n immediately below this PMA or if this is the closest PMA to the PMD.
[c] If number of input or output lanes is 1 for a 50GBASE-R PMA, or 1 or 2 for a 100GBASE-P PMA.
[d] Optional.

Figure 135–5—PMA Functional Block Diagram

135.5.1 Per input-lane clock and data recovery

If the interface between the PMA client and the PMA is physically instantiated as LAUI-2, 50GAUI-n, or 100GAUI-n, the PMA shall meet the electrical and timing specifications above the PMA in Annex 135B through Annex 135G, as appropriate.

If the interface between the sublayer below the PMA and the PMA is physically instantiated as LAUI-2, 50GAUI-n, or 100GAUI-n, the PMA shall meet the electrical and timing specifications below the PMA at the service interface as specified in Annex 135B through Annex 135G, as appropriate.

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135.5.2 Bit-level multiplexing

The PMA provides bit-level multiplexing in both the Tx and Rx directions. In the Tx direction, the function is performed among the bits received from the PMA client via the PMA:IS_UNITDATA_*i*.request primitives (for PMA client lanes $i = 0$ to $p - 1$) with the result sent to the service interface below the PMA using the *inst*:IS_UNITDATA_*i*.request primitives (for service interface lanes $i = 0$ to $q - 1$), referencing the functional block diagram shown in Figure 135–5. The bit multiplexing behavior is illustrated in Figure 135–4.

The aggregate signal carried by the group of input lanes or the group of output lanes is arranged as a set of PCSLs/FECLs. The number of PCSLs/FECLs z is 2 FECLs (below the FEC) and 4 PCSLs (above the FEC) for 50GBASE-R interfaces and 4 FECLs for 100GBASE-P interfaces. For 50GBASE-R, the nominal bit rate R_{lane} is 12.890625 Gb/s for each PCSL and 26.5625 Gb/s for each FECL. For 100GBASE-P, the nominal bit rate R_{lane} is 26.5625 Gb/s for each FECL.

For a PMA with m input lanes (Tx or Rx direction), each input lane carries, bit multiplexed, z/m PCSLs/FECLs. Each input lane has a nominal bit rate of $z/m \times R_{\text{lane}}$. Note that the signaling rate is equal to the bit rate when the signal modulation is NRZ. The signaling rate is equal to half of the bit rate when the signal modulation is PAM4. If necessary, PAM4 symbols are converted to pairs of bits on the input lanes and/or pairs of bits are converted to PAM4 symbols on the output lanes. If bit x received on an input lane belongs to a particular PCSL/FECL, the next bit of that same PCSL/FECL is received on the same input lane at bit position $x+(z/m)$. The z/m PCSLs/FECLs may arrive in any sequence on a given input lane.

For a PMA with n output lanes (Tx or Rx direction), each output lane carries, bit multiplexed, z/n PCSLs/FECLs. Each output lane has a nominal signaling rate of $z/n \times R_{\text{lane}}$. Each PCSL/FECL is mapped from a position in the sequence on one of the m input lanes to a position in the sequence on one of the n output lanes. If bit x sent on an output lane belongs to a particular PCSL/FECL, the next bit of that same PCSL/FECL is sent on the same output lane at bit position $x + (z/n)$. The PMA shall maintain the chosen sequence of PCSLs/FECLs on all output lanes while it is receiving a valid stream of bits on all input lanes.

Each PCSL/FECL received in any temporal position on an input lane is transferred into a temporal position on an output lane. As the PCS (see Clause 133 and Clause 82) and FEC (See Clause 91 and Clause 134) have fully flexible receive logic, an implementation is free to perform the mapping of PCSLs/FECLs from input lanes to output lanes without constraint. Figure 135–6 illustrates one possible bit ordering for a 100GBASE-P 4:2 PMA bit mux. Other bit orderings are also valid.

Note that since the number of input lanes and output lanes for a 50GBASE-R or 100GBASE-P PMA is always a power of two, many PMAs converting between different numbers of lanes normally simply multiplex two or four input lanes to one output lane, or demultiplex two or four output lanes from one input lane. However, any PMA implementation which produces an allowable order of bits from all PCSLs/FECLs on the output lanes is valid.

135.5.3 Skew and Skew Variation

The Skew (relative delay) between the PCSLs/FECLs is kept within limits so that the information on the lanes can be reassembled by the PCS and FEC.

Any PMA that combines PCSLs/FECLs from different input lanes onto the same output lane is required to tolerate Skew Variation between the input lanes without changing the PCSL/FECL positions on the output. Skew and Skew Variation are defined in 131.5. The limits for Skew and Skew Variation at physically instantiated interfaces are specified at Skew points SP0, SP1, and SP2 in the transmit direction and SP5, SP6, and SP7 in the receive direction as defined in 131.5 and illustrated in Figure 131–3 for 50GBASE-R and as defined in 80.5 and illustrated in Figure 80–9 for 100GBASE-P.

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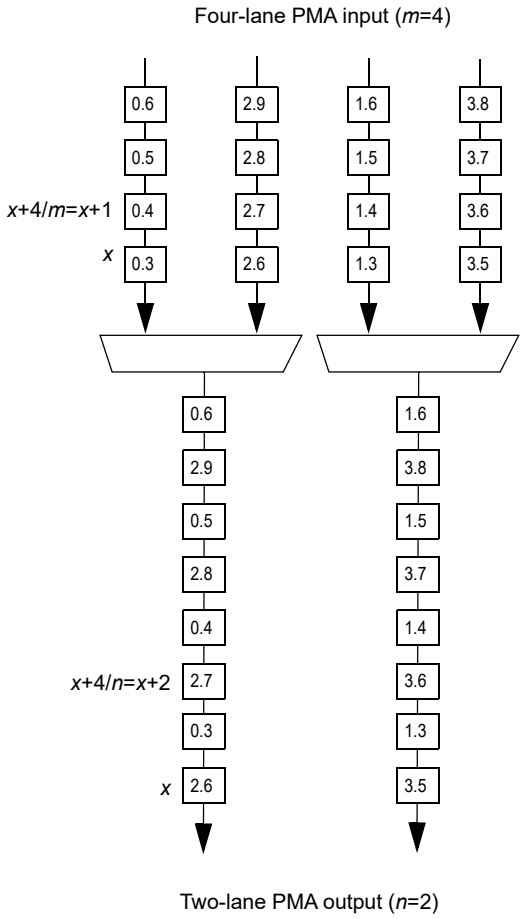

NOTE—*i.k* indicates bit *k* on FECL *i*. Skew may exist between FECLs.

Figure 135–6—Example 4:2 100GBASE-P PMA bit mux

135.5.3.1 Skew generation toward SP0

In an implementation with an instantiated LAUI-2 interface between the PCS and the FEC, the PMA that sends data in the transmit direction toward the LAUI-2 (SP0 in Figure 131–3) shall produce no more than 29 ns of Skew between PCSLs and no more than 0.2 ns of Skew Variation.

135.5.3.2 Skew tolerance at SP0

In an implementation with an instantiated LAUI-2 interface, the PMA service interface that receives data in the transmit direction from the LAUI-2 (SP0 in Figure 131–3) shall tolerate the maximum amount of Skew Variation allowed at SP0 (0.2 ns) between input lanes while maintaining the bit ordering and position of each PCSL on each PMA lane in the transmit direction (toward the PMD).

135.5.3.3 Skew generation toward SP1

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, the PMA that sends data in the transmit direction toward the 50GAUI-n or 100GAUI-n that is closest to the PMD (SP1 in Figure 131–3 and Figure 80–9) shall produce no more than 29 ns of Skew between FECLs toward the 50GAUI-n or 100GAUI-n and no more than 0.2 ns of Skew Variation.

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135.5.3.4 Skew tolerance at SP1

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, the PMA service interface that receives data in the transmit direction from the 50GAUI-n or 100GAUI-n (SP1 in Figure 131–3 and Figure 80–9) shall tolerate the maximum amount of Skew Variation allowed at SP1 (0.2 ns) between input lanes while maintaining the bit ordering and position of each FECL on each PMA lane in the transmit direction (toward the PMD).

135.5.3.5 Skew generation toward SP2

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, the PMA adjacent to the PMD service interface shall generate no more than 43 ns of Skew, and no more than 0.4 ns of Skew Variation between output lanes toward the PMD service interface (SP2 in Figure 80–9 and Figure 131–3). If there is a physically instantiated 50GAUI-n or 100GAUI-n as well, then the Skew measured at SP1 is limited to no more than 29 ns of Skew and no more than 0.2 ns of Skew Variation.

135.5.3.6 Skew tolerance at SP5

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, the PMA adjacent to the PMD service interface (SP5 in Figure 131–3 and Figure 80–9) shall tolerate the maximum amount of Skew Variation allowed at SP5 (0.4 ns) between output lanes from the PMD service interface while maintaining the bit ordering and position of each FECL on each PMA lane in the receive direction (toward the MAC).

135.5.3.7 Skew generation at SP6

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, at SP6 (the receive direction of the 50GAUI-n or 100GAUI-n closest to the FEC), the PMA or group of PMAs between the PMD and the 50GAUI-n or 100GAUI-n closest to the FEC shall deliver no more than 160 ns of Skew, and no more than 3.8 ns of Skew Variation between output lanes toward the 50GAUI-n or 100GAUI-n in the Rx direction.

If there is a physically instantiated PMD service interface that allows the Skew to be measured, the Skew measured at SP5 is limited to no more than 145 ns of Skew and no more than 3.6 ns of Skew Variation. If there is no physically instantiated PMD service interface, the Skew measured at SP4 is limited to no more than 134 ns of Skew, and no more than 3.4 ns of Skew Variation.

135.5.3.8 Skew tolerance at SP6

In an implementation with one or more physically instantiated 50GAUI-n or 100GAUI-n interfaces, the PMA between the 50GAUI-n or 100GAUI-n closest to the FEC and the FEC shall tolerate the maximum amount of Skew Variation allowed at SP6 (3.8 ns) between input lanes while maintaining the bit order and position of FECLs on lanes sent in the receive direction towards the MAC.

135.5.3.9 Skew generation at SP7

In an implementation with an instantiated LAUI-2 interface between the PCS and the FEC, the PMA that sends data in the receive direction toward the LAUI-2 (SP7 in Figure 131–3) shall produce no more than 29 ns of Skew between PCSLs and no more than 0.2 ns of Skew Variation.

135.5.3.10 Skew tolerance at SP7

In an implementation with an instantiated LAUI-2 interface between the PCS and the FEC, the PMA service interface that receives data in the receive direction from the LAUI-2 (SP7 in Figure 131–3) shall tolerate the

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maximum amount of Skew Variation allowed at SP7 (0.2 ns) between input lanes while maintaining the bit ordering and position of each PCSL on each PMA lane in the transmit direction (toward the PMD).

135.5.4 Delay constraints

The maximum cumulative delay contributed by up to three PMA stages in a PHY (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 135–1. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 131.4 and its references.

Table 135–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
50GBASE-R PMA	4608	9	92.16
100GBASE-P PMA	9216	18	92.16

135.5.5 Clocking architecture

A PMA with *m* input lanes and *n* output lanes shall clock the output lanes such that the bit rate of the output lanes is *m*/*n* times the bit rate of the input lanes. For input or output lanes encoded as PAM4, the symbol rate is half of the bit rate. This applies in both the Tx and Rx directions of transmission. In the case where the interfaces between the PMA client and the PMA and/or the PMA and the sublayer below the PMA are physically instantiated, the PMA may derive its input clock(s) from the electrical interface on one or more of the input lanes, and generate the output clock(s) with an appropriate PLL multiplier/divider circuit.

NOTE—For a PMA where the signaling rate on each output lane is higher than the signaling rate on each input lane, any low-frequency jitter on the input lanes may result in more jitter relative to the UI on the output lanes.

There is no requirement that the PMA clock all output lanes in unison. Examples of independent clocking of output lanes include the following:

— The case where the number of input and output lanes are equal (the PMA is provided for retiming and regeneration of the signal). This may be implemented without any rearrangement of PCSLs/FECLs between input lanes and output lanes (although rearrangements are allowed). Such a PMA may be implemented by driving each output lane using the clock recovered from the corresponding input lane.

— Since the number of PCSLs/FECLs is a power of 2, whenever the number of input and output lanes are unequal, each input lane could be mapped to multiple output lanes (in the case where the number of output lanes is greater), or multiple input lanes could be mapped to a single output lane.

135.5.6 Signal drivers

For cases where the interface between the PMA client and the PMA or between the PMA and the sublayer below the PMA represent a physically instantiated interface, the PMA provides electrical signal drivers for that interface. The electrical and jitter/timing specifications for these interfaces appear in

— Annex 135B for LAUI-2 C2C applications
— Annex 135C for LAUI-2 C2M applications
— Annex 135D for 50GAUI-2 and 100GAUI-4 C2C applications
— Annex 135E for 50GAUI-2 and 100GAUI-4 C2M applications
— Annex 135F for 50GAUI-1 and 100GAUI-2 C2C applications
— Annex 135G for 50GAUI-1 and 100GAUI-2 C2M applications

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The modulation format is NRZ for LAUI-2, 50GAUI-2, and 100GAUI-4 and the modulation format is PAM4 for 50GAUI-1 and 100GAUI-2.

135.5.7 PAM4 encoding

135.5.7.1 Gray mapping for PAM4 encoded lanes

For output lanes encoded as PAM4, the PMA transmit process shall map consecutive pairs of bits to Gray-coded symbols G(*j*) with one of four levels as specified in 120.5.7.1.

For input lanes encoded as PAM4, the PMA receive process shall map Gray-coded symbols G(*j*) with one of four levels to pairs of bits as specified in 120.5.7.1.

135.5.7.2 Precoding for PAM4 encoded lanes

The precoding specifications in this subclause apply to the input and output lanes of a PMA that are connected to the service interface of a 50GBASE-R or 100GBASE-R PMD that includes the PMD control function defined in 136.8.11 (50GBASE-CR, 50GBASE-KR, 100GBASE-CR2, or 100GBASE-KR2), or are part of a 50GAUI-1 C2C or 100GAUI-2 C2C link.

The PMA shall provide 1/(1+D) mod 4 precoding capability on each output lane and may optionally provide 1/(1+D) mod 4 decoding capability on each input lane.

On each output lane, for each Gray-coded symbol G(*j*), a precoded symbol P(*j*) shall be determined by the following algorithm, where *j* is an index indicating the symbol number:

$$P(j) = (G(j) - P(j\text{-}1)) \bmod 4, \text{ when precoding is enabled} \quad (135\text{–}1)$$

$$P(j) = G(j), \text{ when precoding is disabled} \quad (135\text{–}2)$$

On each input lane, for each precoded symbol P(*j*), a Gray-code symbol G(*j*) shall be determined by the following algorithm:

$$G(j) = (P(j) + P(j\text{-}1)) \bmod 4, \text{ when precoding is enabled} \quad (135\text{–}3)$$

$$G(j) = P(j), \text{ when precoding is disabled} \quad (135\text{–}4)$$

The precoder is enabled independently for the input and output in each direction (Tx direction toward the PMD and Rx direction toward the MAC) and on each lane. Precoding is enabled and disabled using variables precoder_tx_out_enable_*i*, precoder_rx_in_enable_*i,* precoder_rx_out_enable_*i*, and precoder_tx_in_enable_*i*. If a Clause 45 MDIO is implemented, these variables are accessible through registers 1.600, 1.601, 1.602, and 1.603 (see 45.2.1.139 through 45.2.1.142). An example relating the variables with input and outputs is provided in Figure 135–7.

If the PMA is connected to the service interface of a PMD that includes the PMD control function and training is enabled by the management variable mr_training_enable (see 136.7), then precoder_tx_out_enable_*i* and precoder_rx_in_enable_*i* shall be set as determined by the PMD control function in the LINK_READY state on lane *i* (see 136.8.11.7.5 and Figure 136–7). The method by which the PMD control function affects these variables is implementation dependent.

If the PMA is connected to the service interface of a PMD that supports the PMD control function and training is disabled by the management variable mr_training_enable, or if the PMA is part of a 50GAUI-1 C2C or a 100GAUI-2 C2C link, then precoder_tx_out_enable_*i*, precoder_rx_in_enable_*i*,

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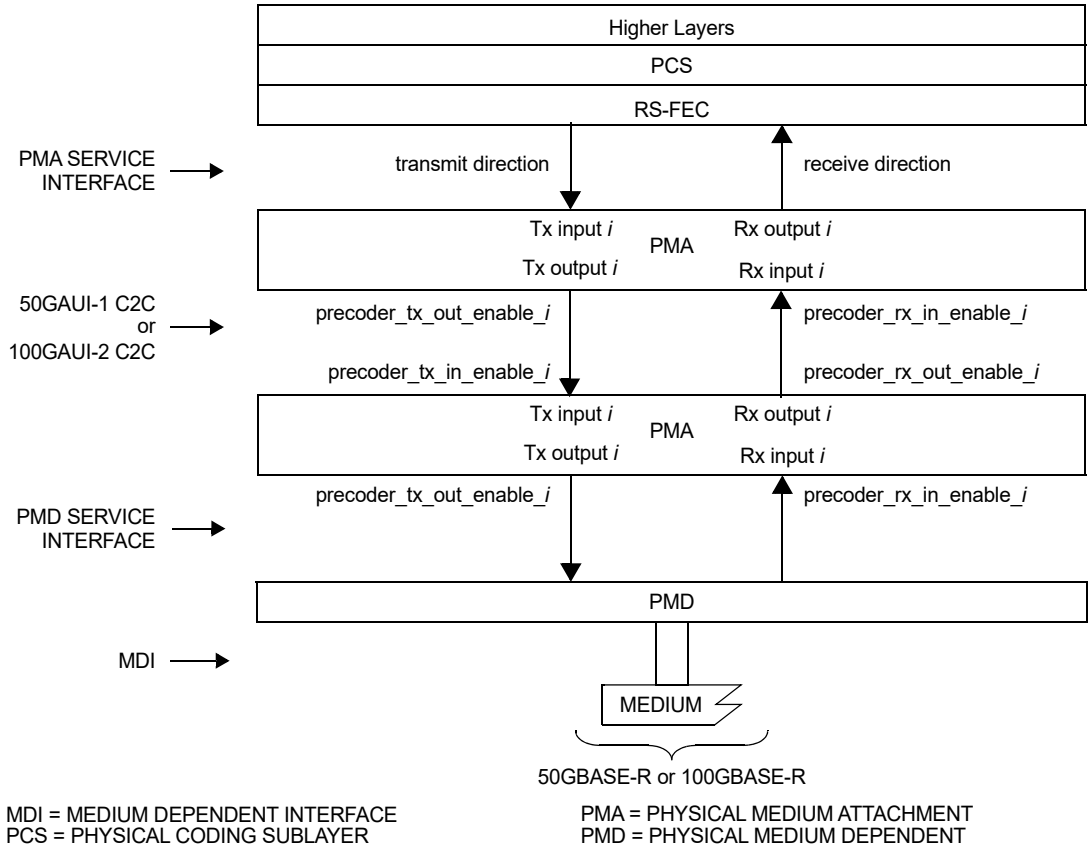

Figure 135–7—Example relating PMA precoder variables to inputs and outputs

precoder_tx_in_enable_*i*, and precoder_rx_out_enable_*i* are set as required by the implementation. The method described in 135F.3.2.1 may be used for 50GAUI-1 C2C or 100GAUI-2 C2C.

135.5.8 PMA local loopback mode (optional)

PMA local loopback mode is optional. If it is implemented, it shall be as specified in this subclause.

The PMA sublayer may provide a local loopback function. The function involves looping back each input lane to the corresponding output lane. Each bit received from the PMA:IS_UNITDATA_*i*.request(tx_symbol) primitive is looped back toward the MAC using the PMA:IS_UNITDATA_*i*.indication(rx_symbol) primitive.

During local loopback, the PMA performs normal bit muxing of PCSLs/FECLs per 135.5.2 onto the lanes in the Tx direction toward the service interface below the PMA.

Ability to perform this function is indicated by the Local_loopback_ability status variable. If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.8.0 (45.2.1.7.15).

A device is placed in local loopback mode when the Local_loopback_enable control variable is set to one, and removed from local loopback mode when this variable is set to zero. If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD control 1 register (bit 1.0.0, see 45.2.1.1.5).

NOTE—Placing a network port into loopback mode can be disruptive to a network.

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135.5.9 PMA remote loopback mode (optional)

PMA remote loopback mode is optional. If implemented, it shall be as described in this subclause.

Remote loopback, if provided, should be implemented in a PMA sublayer close enough to the PMD to maintain the bit sequence on each individual PMD lane. When remote loopback is enabled, each symbol received over a lane of the service interface below the PMA via *inst*:IS_UNITDATA_*i*.indication is looped back to the corresponding output lane toward the PMD via *inst*:IS_UNITDATA_*i*.request. Note that the service interface below the PMA can be provided by the PMD, FEC (LAUI-2 only), or another PMA sublayer.

During remote loopback, the PMA performs normal bit muxing of PCSLs/FECLs per 135.5.2 onto the lanes in the Rx direction towards the PMA client.

The ability to perform this function is indicated by the 50G_Remote_loopback_ability status variable for 50GBASE-R 100G_Remote_loopback_ability status variable for 100GBASE-P.

A device is placed in remote loopback mode when the Remote_loopback_enable control variable is set to one and removed from remote loopback mode when this variable is set to zero.

If a Clause 45 MDIO is implemented, this variable is accessible through bit 1.13.15 (45.2.1.12.1).

If a Clause 45 MDIO is implemented, this variable is accessible through PMA/PMD Control register 1 (bit 1.0.1, see 45.2.1.1.4).

135.5.10 PMA test patterns (optional)

Where the output lanes of the PMA appear on a physically instantiated interface LAUI-2, 50GAUI-n, 100GAUI-n or the PMD service interface (whether or not it is physically instantiated), the PMA may optionally generate and detect test patterns. These test patterns are used to test adjacent-layer interfaces for an individual PMA sublayer or to perform testing between a physically instantiated interface of a PMA sublayer and external test equipment.

135.5.10.1 Test patterns for NRZ encoded signals

For a 50GBASE-R PMA with NRZ encoding, the test patterns in this subclause may be supported.

135.5.10.1.1 PRBS31 test pattern

A PMA may optionally include a PRBS31 test-pattern generator on output lanes in either direction as specified in 120.5.11.1.1.

A PMA may optionally include a PRBS31 test-pattern checker on input lanes in either direction as specified in 120.5.11.1.1.

135.5.10.1.2 PRBS9 test pattern

A PMA may optionally include a PRBS9 test-pattern generator on output lanes in either direction as specified in 120.5.11.1.2.

135.5.10.1.3 Square-wave test pattern

A PMA may optionally include a square-wave test-pattern generator on output lanes in either direction as specified in 120.5.11.1.3.

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135.5.10.2 Test patterns for PAM4 encoded signals

For a 50GBASE-R PMA with PAM4 encoding, the test patterns described in this subclause may be supported.

The PRBS13Q and quaternary square wave test patterns are enabled on a lane-by-lane basis. The patterns PRBS31Q and SSPRQ are enabled on all lanes of an interface at once. If a per-lane pattern is enabled on one or more of the lanes and a per-interface pattern is also enabled, the per-lane patterns are generated only on the indicated lanes and the per-interface pattern is generated on the remaining lanes. The behavior if more than one per-lane pattern is enabled for the same lane or more than one per-interface pattern is enabled is not defined.

135.5.10.2.1 PRBS13Q test pattern

A PMA may optionally include a PRBS13Q test-pattern generator as specified in 120.5.11.2.1.

135.5.10.2.2 PRBS31Q test pattern

A PMA may optionally include a PRBS31Q test-pattern generator on output lanes in either direction as specified in 120.5.11.2.2.

A PMA may optionally include a PRBS31Q test-pattern checker on input lanes in either direction as specified in 120.5.11.2.2.

135.5.10.2.3 SSPRQ test pattern

A PMA may optionally include a short stress pattern random quaternary (SSPRQ) test-pattern generator as specified in 120.5.11.2.3.

135.5.10.2.4 Square wave (quaternary) test pattern

Transmit square wave (quaternary) test-pattern generator optionally applies to each lane of the Tx direction PMA towards a physically instantiated 50GAUI-1 or 100GAUI-1, or towards a PAM4 PMD service interface whether or not it is physically instantiated as specified in 120.5.11.2.4.

135.6 PMA MDIO function mapping

The optional MDIO capability described in Clause 45 describes several variables that provide control and status information for and about the PMA. Since a given implementation may employ more than one PMA sublayer, the PMA control and status information is organized into multiple addressable instances, one for each possible PMA sublayer. See 45.2.1 and 135.1.4 for the allocation of MMD addresses to PMA sublayers. Control and status registers for MMD 8, 9, and 10 use the Extended PMA control and status registers at identical locations to those for MMD 1.

Mapping of MDIO control variables to PMA control variables is shown in Table 135–2. Mapping of MDIO status variables to PMA status variables is shown in Table 135–3. Mapping of MDIO counter to PMA counters is shown in Table 135–4. These tables provide the register and bit numbers for the PMA addressed as MMD 1. For implementations with multiple PMA sublayers, additional PMA sublayers use the corresponding register and bit numbers in MMDs 8, 9, and 10 as necessary.

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Table 135–2—MDIO/PMA control variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
PMA remote loopback	PMA/PMD control 1	1.0.1	Remote_loopback_enable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
Lane 1 Tx output precoder enable	PMA precoder control Tx output	1.600.1	precoder_tx_out_enable_1
Lane 0 Tx output precoder enable	PMA precoder control Tx output	1.600.0	precoder_tx_out_enable_0
Lane 1 Rx input precoder enable	PMA precoder control Rx input	1.601.1	precoder_rx_in_enable_1
Lane 0 Rx input precoder enable	PMA precoder control Rx input	1.601.0	precoder_rx_in_enable_0
Lane 1 Rx output precoder enable	PMA precoder control Rx output	1.602.1	precoder_rx_out_enable_1
Lane 0 Rx output precoder enable	PMA precoder control Rx output	1.602.0	precoder_rx_out_enable_0
Lane 1 Tx input precoder enable	PMA precoder control Tx input	1.603.1	precoder_tx_in_enable_1
Lane 0 Tx input precoder enable	PMA precoder control Tx input	1.603.0	precoder_tx_in_enable_0
PRBS31 pattern enable	PRBS pattern testing control	1.1501.7	PRBS31_enable
PRBS9 pattern enable	PRBS pattern testing control	1.1501.6	PRBS9_enable
PRBS31Q pattern enable	PRBS pattern testing control	1.1501.13	PRBS31Q_pattern_enable
SSPRQ pattern enable	PRBS pattern testing control	1.1501.14	SSPRQ_pattern_enable
Tx generator enable	PRBS pattern testing control	1.1501.3	PRBS_Tx_gen_enable
Tx checker enable	PRBS pattern testing control	1.1501.2	PRBS_Tx_check_enable
Rx generator enable	PRBS pattern testing control	1.1501.1	PRBS_Rx_gen_enable
Rx checker enable	PRBS pattern testing control	1.1501.0	PRBS_Rx_check_enable
Lane 0 SW enable	Square wave testing control	1.1510.0	Square_wave_enable_0
Lane 1 SW enable	Square wave testing control	1.1510.1	Square_wave_enable_1
Lane 2 SW enable	Square wave testing control	1.1510.2	Square_wave_enable_2
Lane 3 SW enable	Square wave testing control	1.1510.3	Square_wave_enable_3
Lane 0 PRBS13Q enable	PRBS13Q testing control	1.1512.0	PRBS13Q_enable_0

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Table 135–2—MDIO/PMA control variable mapping *(continued)*

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
Lane 1 PRBS13Q enable	PRBS13Q testing control	1.1512.1	PRBS13Q_enable_1
Lane 2 PRBS13Q enable	PRBS13Q testing control	1.1512.2	PRBS13Q_enable_2
Lane 3 PRBS13Q enable	PRBS13Q testing control	1.1512.3	PRBS13Q_enable_3

Table 135–3—MDIO/PMA status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMA status variable
PMA local loopback ability	PMA/PMD status 2	1.8.0	Local_loopback_ability
PMA remote loopback ability	40G/100G PMA extended ability	1.13.15	100G_Remote_loopback_ ability
50G PMA remote loopback ability	50G PMA extended ability	1.22.15	50G_Remote_loopback_ ability
PRBS9 Tx generator ability	Test-pattern ability	1.1500.5	PRBS9_Tx_generator_ability
PRBS9 Rx generator ability	Test-pattern ability	1.1500.4	PRBS9_Rx_generator_ability
PRBS31Tx generator ability	Test-pattern ability	1.1500.3	PRBS31_Tx_generator_ability
PRBS31Tx checker ability	Test-pattern ability	1.1500.2	PRBS31_Tx_checker_ability
PRBS31 Rx generator ability	Test-pattern ability	1.1500.1	PRBS31_Rx_generator_ability
PRBS31 Rx checker ability	Test-pattern ability	1.1500.0	PRBS31_Rx_checker_ability
Square wave test ability	Test-pattern ability	1.1500.12	Square_wave_ability
PRBS13Q Tx generator ability	Test-pattern ability	1.1500.11	PRBS13Q_gen_Tx_ability
PRBS13Q Rx generator ability	Test-pattern ability	1.1500.10	PRBS13Q_gen_Rx_ability
PRBS31Q Tx generator ability	Test-pattern ability	1.1500.9	PRBS31Q_gen_Tx_ability
PRBS31Q Rx generator ability	Test-pattern ability	1.1500.7	PRBS31Q_gen_rx_ability
PRBS31Q Tx checker ability	Test-pattern ability	1.1500.8	PRBS31Q_Tx_checker_ability
PRBS31Q Rx checker ability	Test-pattern ability	1.1500.6	PRBS31Q_Rx_checker_ ability
SSPRQ Tx generator ability	Test-pattern ability	1.1500.13	SSPRQ_gen_Tx_ability

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Table 135–4—MDIO/PMA counters mapping

MDIO variable	PMA/PMD register name	Register/bit number	PMA status variable
Error counter Tx, lane 0	PRBS Tx pattern testing error counter, lane 0	1.1600	Ln0_PRBS_Tx_test_err_counter
Error counter Tx, lane 1	PRBS Tx pattern testing error counter, lane 1	1.1601	Ln1_PRBS_Tx_test_err_counter
Error counter Tx, lane 2	PRBS Tx pattern testing error counter, lane 2	1.1602	Ln2_PRBS_Tx_test_err_counter
Error counter Tx, lane 3	PRBS Tx pattern testing error counter, lane 3	1.1603	Ln3_PRBS_Tx_test_err_counter
Error counter Rx, lane 0	PRBS Rx pattern testing error counter, lane 0	1.1700	Ln0_PRBS_Rx_test_err_counter
Error counter Rx, lane 1	PRBS Rx pattern testing error counter, lane 1	1.1701	Ln1_PRBS_Rx_test_err_counter
Error counter Rx, lane 2	PRBS Rx pattern testing error counter, lane 2	1.1702	Ln2_PRBS_Rx_test_err_counter
Error counter Rx, lane 3	PRBS Rx pattern testing error counter, lane 3	1.1703	Ln3_PRBS_Rx_test_err_counter

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135.7 Protocol implementation conformance statement (PICS) proforma for Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P[226]

135.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135.7.2 Identification

135.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[226]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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135.7.3 Major capabilities/options

Item	Feature	Subclause	Value/ Comment	Status	Support
*P50	PMA for 50GBASE-R	135.1.1		O.1	Yes [ ] No [ ]
*P100	PMA for 100GBASE-P	135.1.1		O.1	Yes [ ] No [ ]
*BPCS	PMA is immediately below PCS	135.1.4		O.2	Yes [ ] No [ ]
*AFEC	PMA is immediately above FEC	135.1.4		O.2	Yes [ ] No [ ]
*BFEC	PMA is below FEC and not immediately above PMD.	135.1.4		O.2	Yes [ ] No [ ]
*APMD	PMA is immediately above PMD	135.1.4		O.2	Yes [ ] No [ ]
*PSIA	PMA connected to a physically instantiated PMA service interface	135.1.4		O	Yes [ ] No [ ]
*PSID	PMA connected to a physically instantiated PMD service interface	135.1.4		APMD:O	Yes [ ] N/A [ ]
*NLA	Number of lanes on physically instantiated PMA service interface	135.1.4		50G*PSIA:M	1 [ ] 2 [ ] N/A [ ]
				100G*PSIA:M	2 [ ] 4 [ ] N/A [ ]
*NLD	Number of lanes on PMD service interface	135.1.4		50G*APMD:M	1 [ ] N/A [ ]
				100G*APMD:M	1 [ ] 2 [ ] N/A [ ]
*50GL	Physical instantiation of the PMA service interface is LAUI-2	135.1.4		50G*(BPCS+AFEC)* PSIA:M	Yes [ ] N/A [ ]
*50GA1	Physical instantiation of the PMA service interface is 50GAUI-1	135.1.4		50G*(BFEC+APMD)* PSIA*NLA=1:M	Yes [ ] N/A [ ]
*50GA2	Physical instantiation of the PMA service interface is 50GAUI-2	135.1.4		50G*(BFEC+APMD)* PSIA*NLA=2:M	Yes [ ] N/A [ ]
*100GA2	Physical instantiation of the PMA service interface is 100GAUI-2	135.1.4		100G*(BFEC+APMD) *PSIA*NLA=2:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/ Comment	Status	Support
*100GA4	Physical instantiation of the PMA service interface is 100GAUI-4	135.1.4		100G*(BFEC+APMD) *PSIA*NLA=4:M	Yes [ ] N/A [ ]
*AT	AUI type, C2C or C2M	135.5.6		PSIA:M	C2C [ ] C2M [ ] N/A [ ]
*NRZ	NRZ modulation	135.1.4		50GL+50GA2+ 100GA4:M	Yes [ ] N/A [ ]
*PAM4A	PAM4 modulation on physically instantiated PMA service interface	135.1.4		50GA1+100GA2:M	Yes [ ] N/A [ ]
*PAM4D	PAM4 modulation on PMD service interface	135.1.4		APMD:M	Yes [ ] N/A [ ]
*PMDE	PMD is 50GBASE-CR, 50GBASE-KR, 100GBASE-CR2, 100GBASE-KR2	135.5.7.2		APMD:O	Yes [ ] N/A [ ]
MD	MDIO	135.6	Registers and interface supported	O	Yes [ ] No [ ]

135.7.4 PICS proforma tables for Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P

135.7.4.1 Functions

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Maintain lane mapping while link is in operation	135.5.2	Maintain sequence of PCSLs/FECLs on all output lanes	M	Yes [ ]

135.7.4.2 Timing

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Skew generation toward SP0 in Tx direction	135.5.3.1	≤ 29 ns	BPCS*PSIA:M	Yes [ ] N/A [ ]
S2	Skew Variation generation toward SP0 in Tx direction	135.5.3.1	≤ 200 ps	BPCS*PSIA:M	Yes [ ] N/A [ ]
S3	Skew Variation tolerance at SP0	135.5.3.2	Minimum 200 ps	AFEC*PSIA:M	Yes [ ] N/A [ ]
S4	Skew generation toward SP1 in Tx direction	135.5.3.3	≤ 29 ns	BFEC*PSIA:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
S5	Skew Variation generation toward SP1 in Tx direction	135.5.3.3	≤ 200 ps	BFEC*PSIA:M	Yes [ ] N/A [ ]
S6	Skew Variation tolerance at SP1	135.5.3.4	Minimum 200 ps	APMD*PSIA:M	Yes [ ] N/A [ ]
S7	Skew generation toward SP2 in Tx direction	135.5.3.5	≤ 43 ns	APMD*PSID:M	Yes [ ] N/A [ ]
S8	Skew Variation generation toward SP2 in Tx direction	135.5.3.5	≤ 400 ps	APMD*PSID:M	Yes [ ] N/A [ ]
S9	Skew Variation tolerance at SP5	135.5.3.6	Minimum 3.6 ns	APMD*PSID:M	Yes [ ] N/A [ ]
S10	Skew generation toward SP6 in Rx direction	135.5.3.7	≤ 160 ns	(BFEC+APMD)* PSIA:M	Yes [ ] N/A [ ]
S11	Skew Variation generation toward SP6 in Rx direction	135.5.3.7	≤ 3.8 ns	(BFEC+APMD)* PSIA:M	Yes [ ] N/A [ ]
S12	Skew Variation tolerance at SP6	135.5.3.8	Minimum 3.8 ns	BFEC*PSIA:M	Yes [ ] N/A [ ]
S13	Skew generation toward SP7 in Rx direction	135.5.3.9	≤ 160 ns	AFEC*PSIA:M	Yes [ ] N/A [ ]
S14	Skew Variation generation toward SP7 in Rx direction	135.5.3.9	≤ 3.8 ns	AFEC*PSIA:M	Yes [ ] N/A [ ]
S15	Skew Variation tolerance at SP7	135.5.3.10	Minimum 3.8 ns	BPCS*PSIA:M	Yes [ ] N/A [ ]
S16	Round-trip delay limit for 50GBASE-R	135.5.4	No more than 18 432 bit times or 36 pause_quanta	P50:M	Yes [ ] N/A [ ]
S17	Round-trip delay limit for 100GBASE-P	135.5.4	No more than 36 864 bit times or 72 pause_quanta	P100:M	Yes [ ] N/A [ ]

135.7.4.3 Electrical

Item	Feature	Subclause	Value/Comment	Status	Support
E1	Lane signaling rate for LAUI-2	135.1.4	25.78125 GBd	50GL:M	Yes [ ] N/A [ ]
E2	Lane signaling rate for 50GAUI-n, 100GAUI-n	135.1.4	26.5625 GBd	50GA1+50GA2+ 100GA2+ 100GA4:M	Yes [ ] N/A [ ]
E3	Lane signaling rate for one-lane 50 Gb/s PMD service interface	135.1.4	26.5625 GBd	APMD*50G:M	Yes [ ] N/A [ ]
E4	Lane signaling rate for two-lane 100 Gb/s PMD service interface	135.1.4	26.5625 GBd	APMD*100G* NLD=2:M	Yes [ ] N/A [ ]
E5	Lane signaling rate for one-lane 100 Gb/s PMD service interface	135.1.4	53.125 GBd	APMD*100G* NLD=1:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
E6	Electrical and timing requirements of Annex 135B met by LAUI-2	135.5.1, 135.5.5		50GL* (AT=C2C):M	Yes [ ] N/A [ ]
E7	Electrical and timing requirements of Annex 135D met by 50GAUI-2 or 100GAUI-4	135.5.1, 135.5.6		(50GA2+ 100GA4)* (AT=C2C):M	Yes [ ] N/A [ ]
E8	Electrical and timing requirements of Annex 135E met by 50GAUI-2 or 100GAUI-4	135.5.1, 135.5.6		(50GA2+ 100GA4)* (AT=C2M):M	Yes [ ] N/A [ ]
E9	Electrical and timing requirements of Annex 135F met by 50GAUI-1 or 100GAUI-2	135.5.1, 135.5.6		(50GA1+ 100GA2)* (AT=C2C):M	Yes [ ] N/A [ ]
E10	Electrical and timing requirements of Annex 135G met by 50GAUI-1 or 100GAUI-2	135.5.1, 135.5.6		(50GA1+ 100GA2)* (AT=C2M):M	Yes [ ] N/A [ ]

135.7.4.4 Diagnostics

Item	Feature	Subclause	Value/Comment	Status	Support
*LBL	PMA local loopback	135.5.8	Supports local loopback	O	Yes [ ] No [ ]
*LBR	PMA remote loopback	135.5.9	Supports remote loopback	O	Yes [ ] No [ ]
D1	PMA local loopback implemented	135.5.8	Meets the requirements of 135.5.8	LBL:M	Yes [ ] N/A [ ]
D2	PMA remote loopback implemented	135.5.9	Meets the requirements of 135.5.9	LBR:M	Yes [ ] N/A [ ]
D3	Send PRBS31 Tx	135.5.10.1.1		NRZ:O	Yes [ ] No [ ] N/A[ ]
D4	Send PRBS31 Rx	135.5.10.1.1		NRZ:O	Yes [ ] No [ ] N/A[ ]
D5	Check PRBS31 Tx	135.5.10.1.1		NRZ:O	Yes [ ] No [ ] N/A[ ]
D6	Check PRBS31 Rx	135.5.10.1.1		NRZ:O	Yes [ ] No [ ] N/A[ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
D7	Send PRBS9 Tx	135.5.10.1.2		NRZ:O	Yes [ ] No [ ] N/A[ ]
D8	Send PRBS9 Rx	135.5.10.1.2		NRZ:O	Yes [ ] No [ ] N/A[ ]
D9	Send NRZ square wave Tx	135.5.10.1.3		NRZ:O	Yes [ ] No [ ] N/A[ ]
D10	Send PRBS13Q Tx	135.5.10.2.1		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D11	Send PRBS13Q Rx	135.5.10.2.1		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D12	Send PRBS31Q Tx	135.5.10.2.2		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D13	Send PRBS31Q Rx	135.5.10.2.2		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D14	Check PRBS31Q Tx	135.5.10.2.2		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D15	Check PRBS31Q Rx	135.5.10.2.2		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D16	Send SSPRQ Tx	135.5.10.2.3		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]
D17	Send quaternary square wave Tx	135.5.10.2.4		PAM4A+PAM4D:O	Yes [ ] No [ ] N/A[ ]

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135.7.7 Encoding

Item	Feature	Subclause	Value/Comment	Status	Support
C1	PMA supports Gray coding	135.5.7.1		PAM4A+PAM4D:M	Yes [ ] N/A [ ]
C2	PMA supports output precoding for physically instantiated PMA service interface	135.5.7.2		(50GA1+100GA2)* (AT=C2C):M	Yes [ ] N/A [ ]
C3	PMA supports input precoding for physically instantiated PMA service interface	135.5.7.2		(50GA1+100GA2)* (AT=C2C):O	Yes [ ] No [ ] N/A [ ]
C4	PMA supports output precoding for PMD service interface	135.5.7.2		PMDE:M	Yes [ ] N/A [ ]
C4	PMA supports input precoding for PMD service interface	135.5.7.2		PMDE:O	Yes [ ] No [ ] N/A [ ]

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136. Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136.1 Overview

This clause specifies the 50GBASE-CR PMD, the 100GBASE-CR2 PMD, the 200GBASE-CR4 PMD, and the baseband medium. The specifications for the three PMDs are similar, except for the number of lanes and associated parameters and the MDI.

There are four associated annexes. Annex 136A provides information on parameters with test points that may not be testable in an implemented system. Annex 136B specifies test fixtures. Annex 136C specifies MDIs. Annex 136D describes 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 host and cable assembly form factors.

When forming a complete Physical Layer, a PMD shall be connected as illustrated in Figure 136–1, to the appropriate sublayers (as specified in Table 136–1, Table 136–2, and Table 136–3), to the medium through the appropriate MDI, and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 136–1—Physical Layer clauses associated with the 50GBASE-CR PMD

Associated clause	50GBASE-CR
132—RS	Required
132—50GMII[a]	Optional
133—PCS for 50GBASE-R	Required
134—RS-FEC	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135D—50GAUI-2 C2C	Optional
135F—50GAUI-1 C2C	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The 50GMII is an optional interface. However, if the 50GMII is not implemented, a conforming implementation behaves functionally as though the RS and 50GMII were present.

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Table 136–2—Physical Layer clauses associated with the 100GBASE-CR2 PMD

Associated clause	100GBASE-CR2
80—RS	Required
80—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R	Optional[b]
83A—CAUI-10	Optional
83D—CAUI-4 C2C	Optional
135—PMA for 100GBASE-P	Required
135D—100GAUI-4 C2C	Optional
135F—100GAUI-2 C2C	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation behaves functionally as though the RS and CGMII were present.
[b]PMA for 100GBASE-R is required when either CAUI-10 or CAUI-4 is used.

Table 136–3—Physical Layer clauses associated with the 200GBASE-CR4 PMD

Associated clause	200GBASE-CR4
117—RS	Required
117—200GMII[a]	Optional
118—200GMII extender	Optional
119—PCS for 200GBASE-R	Required
120—PMA for 200GBASE-R	Required
120B—200GAUI-8 C2C	Optional
120D—200GAUI-4 C2C	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The 200GMII is an optional interface. However, if the 200GMII is not implemented, a conforming implementation behaves functionally as though the RS and 200GMII were present.

For the 50GBASE-CR and 100GBASE-CR2 PHYs, in order to support the required frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are expected to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 10^{-10} after processing by the RS-FEC (Clause 134 or Clause 91) and the PCS (Clause 133 or Clause 82) if

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there are negligible errors due to other electrical interfaces (50GAUI-n or 100GAUI-n). If the PMD and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 10^{-10}.

For the 200GBASE-CR4 PHY, in order to support the required frame loss ratio (see 1.4.344) of less than 6.2×10^{-11} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are expected to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 9.2×10^{-13} after processing by the PCS (Clause 119) if there are negligible errors due to other electrical interfaces (200GAUI-n). If the PMD and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 9.2×10^{-13}.

A compliant input signal is a transmitter output of a compliant PHY that has passed through a compliant cable assembly.

50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Figure 136–1 shows the relationship of the 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMD sublayers and MDIs to the ISO/IEC Open System Interconnection (OSI) reference model.

136.2 Conventions

Clause 136 describes three PMDs, 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMD, which have one, two, and four lanes, respectively. For efficient description, the parameter n is used to describe the number of lanes in a specific PMD. Accordingly, n = 1 for 50GBASE-CR, n = 2 for 100GBASE-CR2, and n = 4 for 200GBASE-CR4.

The parameter *i* is used as an index or a suffix to identify a specific lane, and takes the values 0 to n – 1.

Within this clause, the unqualified term “PMD” refers to any of 50GBASE-CR PMD, 100GBASE-CR2 PMD, or 200GBASE-CR4 PMD.

136.3 PMD service interfaces

This subclause specifies the services provided by the 50GBASE-CR, 100GBASE-CR2 and 200GBASE-CR4 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The 50GBASE-CR PMD service interface is an instance of the inter-sublayer service interface defined in 131.3, with a single symbol stream (n = 1).

The 100GBASE-CR2 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with the exception that there are two parallel symbol streams (n = 2).

The 200GBASE-CR4 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with four parallel symbol streams (n = 4).

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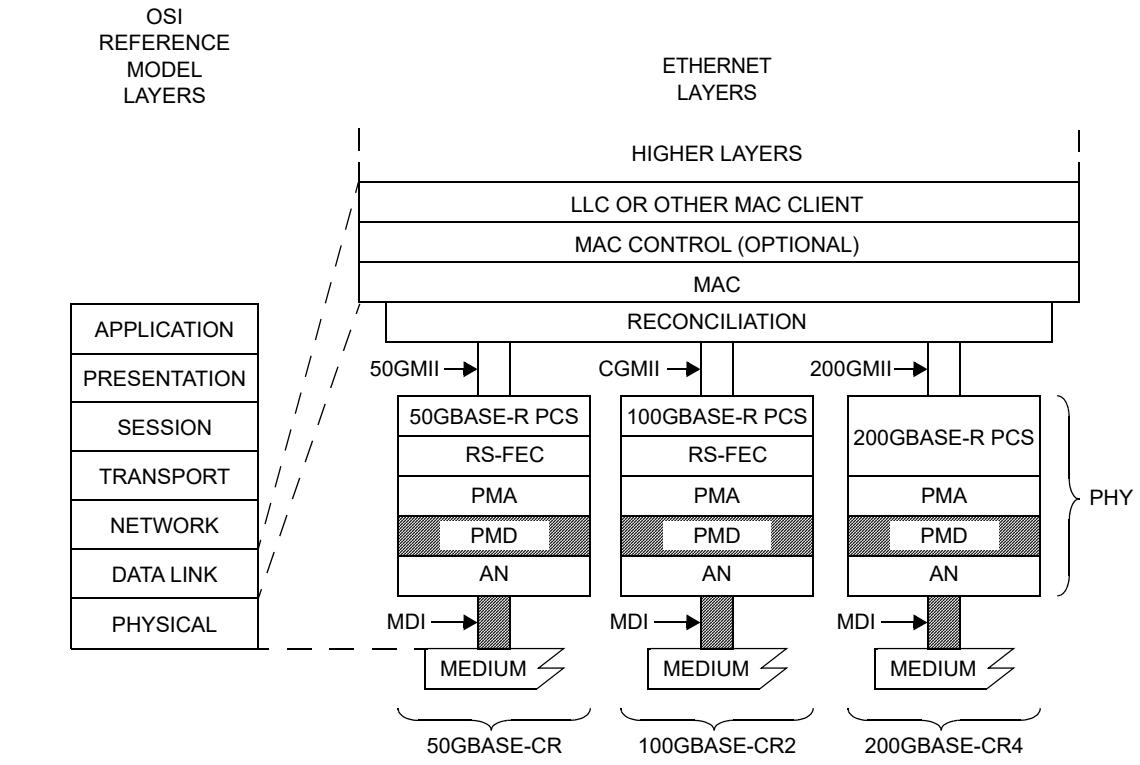

200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 136–1—50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 50GBASE-CR PMD has a single symbol stream, hence $i = 0$.

The 100GBASE-CR2 PMD has two parallel symbol streams, hence $i = 0$ to 1.

The 200GBASE-CR4 PMD has four parallel symbol streams, hence $i = 0$ to 3.

In the transmit direction, the PMA continuously sends n streams of PAM4 symbols to the PMD, one per lane, using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 26.5625 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

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In the receive direction, the PMD continuously sends *n* streams of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, one per lane, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 26.5625 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable Global_PMD_signal_detect as defined in 136.8.4. When Global_PMD_signal_detect is one, SIGNAL_OK shall be assigned the value OK. When Global_PMD_signal_detect is zero, SIGNAL_OK shall be assigned the value FAIL. When SIGNAL_OK is FAIL, the PMD:IS_UNITDATA_*i*.indication parameter is undefined.

136.4 PCS requirements for Auto-Negotiation (AN) service interface

The PCSs associated with the 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMDs are required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 133.4, 82.6, and 119.6.)

50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR-4 PHYs may be extended using chip-to-chip (C2C) 50GAUI-n/LAUI-2, 100GAUI-n/CAUI-n, and 200GAUI-n, respectively, as physical instantiations of the inter-sublayer service interface between devices. If such extension is used, then the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementer. As examples, the implementer may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

136.5 Delay constraints

The sum of the transmit and the receive delays at one end of the link contributed by the PMD and AN including the medium in one direction shall be no more than the maximum delays listed in Table 136–4. It is assumed that the one-way delay through the medium is no more than 20 ns.

Table 136–4—Delay constraints

PMD	Maximum (bit times)[a]	Maximum (pause_quanta)[b]	Maximum (ns)
50GBASE-CR	2048	4	40.96
100GBASE-CR2	4096	8	40.96
200GBASE-CR4	8192	16	40.96

[a]One bit time is equal to 20 ps for 50GBASE-CR, 10 ps for 100GBASE-CR2, and 5 ps for 200GBASE-CR4. (See 1.4.215 for the definition of bit time.)
[b]One pause_quantum is equal to 10.24 ns for 50GBASE-CR, 5.12 ns for 100GBASE-CR2, and 2.56 ns for 200GBASE-CR4. (See 31B.2 for the definition of pause_quanta.)

Descriptions of overall system delay constraints can be found in 131.4 for 50GBASE-CR, in 80.4 for 100GBASE-CR2, and in 116.3 for 200GBASE-CR4.

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136.6 Skew constraints

The Skew (relative delay) between the PCS or FEC lanes is kept within limits so that the information on the PCS or FEC lanes can be reassembled by the PCS or FEC. The Skew Variation is also limited to ensure that a given PCS or FEC lane always traverses the same physical lane.

136.6.1 Skew Constraints for 50GBASE-CR

Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2 with the exception that the measurement clock and data recovery unit high-frequency corner bandwidth is 4 MHz.

136.6.2 Skew Constraints for 100GBASE-CR2 and 200GBASE-CR4

Skew and Skew Variation are defined in 80.5 and 116.5 and specified at the points SP1 to SP6 shown in Figure 80–9 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5 and 116.5.

136.7 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control bits to PMD

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control variables as shown in Table 136–5, and MDIO status bits to PMD status variables as shown in Table 136–6.

Table 136–5—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 3 to PMD transmit disable 2[a]	PMD transmit disable	1.9.4:3	PMD_transmit_disable_3, PMD_transmit_disable_2
PMD transmit disable 1[b]	PMD transmit disable	1.9.2	PMD_transmit_disable_1
PMD transmit disable 0	PMD transmit disable	1.9.1	PMD_transmit_disable_0
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable
Polynomial identifier 3[a]	PMD training pattern lane 3	1.1453.12:11	identifier_3
Seed 3[a]	PMD training pattern lane 3	1.1453.15:14 1.1453.10:0	seed_3
Polynomial identifier 2[a]	PMD training pattern lane 2	1.1452.12:11	identifier_2
Seed 2[a]	PMD training pattern lane 2	1.1452.15:14 1.1452.10:0	seed_2
Polynomial identifier 1[b]	PMD training pattern lane 1	1.1451.12:11	identifier_1
Seed 1[b]	PMD training pattern lane 1	1.1451.15:14 1.1451.10:0	seed_1
Polynomial identifier 0	PMD training pattern lane 0	1.1450.12:11	identifier_0
Seed 0	PMD training pattern lane 0	1.1450.15:14 1.1450.10:0	seed_0
Initial condition request 3[a]	BASE-R PAM4 PMD training LP control, lane 3	1.1123.13:12	ic_req
Coefficient select 3[a]	BASE-R PAM4 PMD training LP control, lane 3	1.1123.4:2	coef_sel
Coefficient request 3[a]	BASE-R PAM4 PMD training LP control, lane 3	1.1123.1:0	coef_req
Initial condition request 2[a]	BASE-R PAM4 PMD training LP control, lane 2	1.1122.13:12	ic_req
Coefficient select 2[a]	BASE-R PAM4 PMD training LP control, lane 2	1.1122.4:2	coef_sel
Coefficient request 2[a]	BASE-R PAM4 PMD training LP control, lane 2	1.1122.1:0	coef_req
Initial condition request 1[b]	BASE-R PAM4 PMD training LP control, lane 1	1.1121.13:12	ic_req
Coefficient select 1[b]	BASE-R PAM4 PMD training LP control, lane 1	1.1121.4:2	coef_sel

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Table 136–5—MDIO/PMD control variable mapping *(continued)*

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Coefficient request 1[b]	BASE-R PAM4 PMD training LP control, lane 1	1.1121.1:0	coef_req
Initial condition request 0	BASE-R PAM4 PMD training LP control, lane 0	1.1120.13:12	ic_req
Coefficient select 0	BASE-R PAM4 PMD training LP control, lane 0	1.1120.4:2	coef_sel
Coefficient request 0	BASE-R PAM4 PMD training LP control, lane 0	1.1120.1:0	coef_req

[a]Available only in 200GBASE-CR4.
[b]Available only in 100GBASE-CR2 and 200GBASE-CR4.

Table 136–6—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 2[a]	PMD receive signal detect	1.10.4:3	PMD_signal_detect_3 to PMD_signal_detect_2
PMD receive signal detect 1[b]	PMD receive signal detect	1.10.2	PMD_signal_detect_1
PMD receive signal detect 0	PMD receive signal detect	1.10.1	PMD_signal_detect_0
Receiver status 3[a]	BASE-R PMD status	1.151.12	local_trained_3
Frame lock 3[a]	BASE-R PMD status	1.151.13	local_tf_lock_3
Startup protocol status 3[a]	BASE-R PMD status	1.151.14	training_3
Training failure 3[a]	BASE-R PMD status	1.151.15	training_failure_3
Receiver status 2[a]	BASE-R PMD status	1.151.8	local_trained_2
Frame lock 2[a]	BASE-R PMD status	1.151.9	local_tf_lock_2
Startup protocol status 2[a]	BASE-R PMD status	1.151.10	training_2
Training failure 2[a]	BASE-R PMD status	1.151.11	training_failure_2
Receiver status 1[b]	BASE-R PMD status	1.151.4	local_trained_1
Frame lock 1[b]	BASE-R PMD status	1.151.5	local_tf_lock_1
Startup protocol status 1[b]	BASE-R PMD status	1.151.6	training_1
Training failure 1[b]	BASE-R PMD status	1.151.7	training_failure_1
Receiver status 0	BASE-R PMD status	1.151.0	local_trained_0

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Table 136–6—MDIO/PMD status variable mapping *(continued)*

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Frame lock 0	BASE-R PMD status	1.151.1	local_tf_lock_0
Startup protocol status 0	BASE-R PMD status	1.151.2	training_0
Training failure 0	BASE-R PMD status	1.151.3	training_failure_0
Receiver ready[a]	BASE-R PAM4 PMD training LP status, lane 3	1.1223.15	remote_rx_ready
Modulation and precoding status[a]	BASE-R PAM4 PMD training LP status, lane 3	1.1223.11:10	remote_tp_mode
Receiver frame lock[a]	BASE-R PAM4 PMD training LP status, lane 3	1.1223.9	remote_tf_lock
Initial condition status[a]	BASE-R PAM4 PMD training LP status, lane 3	1.1223.8	ic_sts
Coefficient status[a]	BASE-R PAM4 PMD training LP status, lane 3	1.1223.2:0	coef_sts
Receiver ready[a]	BASE-R PAM4 PMD training LP status, lane 2	1.1222.15	remote_rx_ready
Modulation and precoding status[a]	BASE-R PAM4 PMD training LP status, lane 2	1.1222.11:10	remote_tp_mode
Receiver frame lock[a]	BASE-R PAM4 PMD training LP status, lane 2	1.1222.9	remote_tf_lock
Initial condition status[a]	BASE-R PAM4 PMD training LP status, lane 2	1.1222.8	ic_sts
Coefficient status[a]	BASE-R PAM4 PMD training LP status, lane 2	1.1222.2:0	coef_sts
Receiver ready[b]	BASE-R PAM4 PMD training LP status, lane 1	1.1221.15	remote_rx_ready
Modulation and precoding status[b]	BASE-R PAM4 PMD training LP status, lane 1	1.1221.11:10	remote_tp_mode
Receiver frame lock[b]	BASE-R PAM4 PMD training LP status, lane 1	1.1221.9	remote_tf_lock
Initial condition status[b]	BASE-R PAM4 PMD training LP status, lane 1	1.1221.8	ic_sts
Coefficient status[b]	BASE-R PAM4 PMD training LP status, lane 1	1.1221.2:0	coef_sts
Receiver ready	BASE-R PAM4 PMD training LP status, lane 0	1.1220.15	remote_rx_ready
Modulation and precoding status	BASE-R PAM4 PMD training LP status, lane 0	1.1220.11:10	remote_tp_mode

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Table 136–6—MDIO/PMD status variable mapping *(continued)*

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Receiver frame lock	BASE-R PAM4 PMD training LP status, lane 0	1.1220.9	remote_tf_lock
Initial condition status	BASE-R PAM4 PMD training LP status, lane 0	1.1220.8	ic_sts
Coefficient status	BASE-R PAM4 PMD training LP status, lane 0	1.1220.2:0	coef_sts

[a]Available only in 200GBASE-CR4.
[b]Available only in 100GBASE-CR2 and 200GBASE-CR4.

136.8 PMD functional specifications

136.8.1 Link block diagram

One direction of a 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4 link is shown in Figure 136–2.

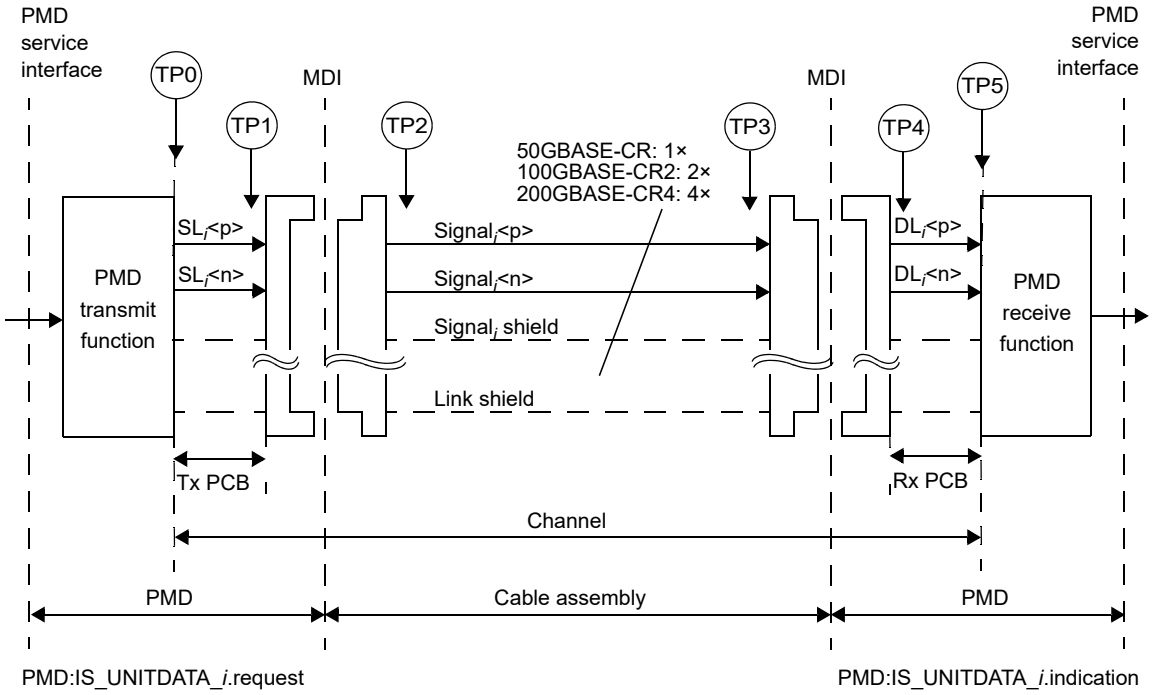

Figure 136–2—50GBASE-CR, 100GBASE-CR2 or 200GBASE-CR4 link (one direction is illustrated)

Note that the source lane (SL) signals SL$_i$<p> and SL$_i$<n> are the positive and negative sides of the transmitter's differential signal pair on lane *i* and the destination lane (DL) signals DL$_i$<p> and DL$_i$<n> are the positive and negative sides of the receiver's differential signal pair on lane *i*.

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For purposes of system conformance, the PMD sublayer is standardized at the test points described in this subclause.

The electrical transmit signal is defined at TP2. Unless specified otherwise, all transmitter measurements and tests defined in 136.9.3 are made at TP2 utilizing the test fixture specified in Annex 136B.

The electrical receive signal is defined at TP3. Unless specified otherwise, all receiver measurements and tests defined in 136.9.4 are performed at TP3 utilizing the test fixture specified in Annex 136B.

A mated connector pair has been included in both the transmitter and receiver specifications defined in 136.9.3 and 136.9.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is provided in 136.9.3.2. Annex 136A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system.

The channel (see 136.10) is defined between the transmitter (TP0) and receiver (TP5) blocks to include the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss, as illustrated in Figure 136–2. All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 136–2. The cable assembly test fixture of 136B.1, or its equivalent, is required for measuring the cable assembly specifications in 136.10 at TP1 and TP4. Two cable assembly test fixtures have been included in the cable assembly specifications defined in 136.10. Transmitter and receiver differential controlled impedance printed circuit board insertion losses defined between TP0 and the MDI and between the MDI and TP5, respectively, are provided informatively in 136A.4.

Table 136–7 describes the defined test points illustrated in Figure 136–2.

Table 136–7—Test points

Test points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 136–2. The cable assembly test fixture of Annex 136B, or its equivalent, is required for measuring the cable assembly specifications in 136.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 136.9.3 and 136.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 136.9.3.2.
TP2	Unless specified otherwise, all transmitter measurements defined in 136.9.3 are made at TP2 utilizing the test fixture specified in Annex 136B.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 136.9.4 are made at TP3 utilizing the test fixture specified in Annex 136B.

136.8.2 PMD transmit function

The PMD transmit function has three operating modes: DATA, TRAINING, and QUIET. The operating mode is controlled by the PMD control state diagram (Figure 136–7). Support for the QUIET operating mode is only required when the variable use_quiet_in_training (see 136.8.11.7.1) is set to TRUE.

When operating in DATA mode, the PMD transmit function shall convert the symbol stream requested by the PMD service interface message PMD:IS_UNITDATA_*i*.request(tx_symbol) of each lane into an

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electrical signal, and deliver the electrical signals to the MDI, according to the transmit electrical specifications in 136.9.3. The differential output voltage (SL_i<p> minus SL_i<n>) meets the specifications in 136.9.3.1.1 where the PAM4 symbol values 0, 1, 2, and 3 correspond to the tx_symbol values zero, one, two, and three, respectively, with the highest differential output voltage corresponding to tx_symbol = three and the lowest differential output voltage corresponding to tx_symbol = zero.

When operating in TRAINING mode, the PMD transmit function shall convert the symbol stream generated by the PMD control function of each lane into an electrical signal, and deliver the electrical signals to the MDI, according to the transmit electrical specifications in 136.9.3. The differential output voltage (SL_i<p> minus SL_i<n>) meets the specifications in 136.9.3.1.1, with the highest differential output voltage corresponding to the PAM4 symbol 3 and the lowest differential output voltage corresponding to the PAM4 symbol 0.

When operating in QUIET mode the PMD transmit function shall turn off the transmitter such that the transmitter drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max) with Tx disabled in Table 136–11.

136.8.3 PMD receive function

The PMD receive function shall convert the electrical signal from each of the lanes on the MDI into a symbol stream for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_*i*.indication(rx_symbol). The highest differential input voltage (DL_i<p> minus DL_i<n>) shall correspond to rx_symbol = three and the lowest differential input voltage shall correspond to rx_symbol = zero.

136.8.4 PMD global signal detect function

For the 50GBASE-CR PMD, the variable Global_PMD_signal_detect is set to PMD_signal_detect_0 (see 136.8.5). For the 100GBASE-CR2 and 200GBASE-CR4 PMDs, the variable Global_PMD_signal_detect is set to the logical AND of the values of PMD_signal_detect_*i* from each of the PMD lanes.

136.8.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal detect function is used by the PMD to indicate the successful completion of the startup protocol by the PMD control function (see 136.8.11). PMD_signal_detect_*i* shall be set to zero when signal_detect on lane *i* is set to false, and to one when signal_detect on lane *i* is set to true. The signal_detect variables are set independently on each lane by the PMD control state diagram (Figure 136–7).

If training is disabled by the management variable mr_training_enable (see 136.7), PMD_signal_detect_*i* shall be set to one for all lanes.

When the MDIO is implemented, this function maps the variables to registers and bits as defined in 136.7.

136.8.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional. When implemented, it allows the transmitters on all lanes to be disabled with a single variable.

When Global_PMD_transmit_disable variable is set to one, this function shall turn off all the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max.) with Tx disabled in Table 136–11.

If a PMD fault (136.8.8) is detected, then the PMD may set Global_PMD_transmit_disable to one.

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136.8.7 PMD lane-by-lane transmit disable function (optional)

The PMD lane-by-lane transmit disable function is optional and allows the transmitter in each lane to be selectively disabled. When this function is supported, it shall meet the following requirements:

— When a PMD_transmit_disable_*i* variable is set to one, this function shall turn off the transmitter in lane *i* so that it drives a constant level (i.e., no transitions) and does not exceed the differential peak-to-peak output voltage (max.) with Tx disabled in Table 136–11.

— If a PMD fault (136.8.8) is detected, then the PMD may set each PMD_transmit_disable_*i* to one, turning off the transmitter in each lane.

136.8.8 PMD fault function

PMD_fault is the logical-OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault. If the MDIO interface is implemented, then PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

136.8.9 PMD transmit fault function (optional)

The PMD transmit fault function is optional. The faults detected by this function are implementation specific, but the assertion of Global_PMD_transmit_disable is not considered a transmit fault.

If PMD_transmit_fault is set to one, then Global_PMD_transmit_disable should also be set to one.

If the MDIO interface is implemented, then PMD_transmit_fault shall be mapped to the Transmit fault bit as specified in 45.2.1.7.4.

136.8.10 PMD receive fault function (optional)

The PMD receive fault function is optional. The faults detected by this function are implementation specific. A fault is indicated by setting the variable PMD_receive_fault to one.

If the MDIO interface is implemented, then PMD_receive_fault shall be mapped to the Receive fault bit as specified in 45.2.1.7.5.

136.8.11 PMD control function

The PMD control function performs the PMD startup protocol. This protocol facilitates timing recovery and equalization while providing a mechanism through which the receiver can configure the transmitter to optimize performance. The protocol supports these functions through the continuous exchange of fixed-length training frames.

The PMD shall implement one instance of the PMD control function described in this subclause for each lane. The PMD control functions operate independently on each lane.

136.8.11.1 Training frame structure

The training frame is a sequence of PAM4 symbols whose values correspond to the possible values of the tx_symbol and rx_symbol variables (the PAM4 symbol values 0, 1, 2, and 3 correspond to tx_symbol or rx_symbol values zero, one, two, and three, respectively). The structure of a training frame is shown in Figure 136–3.

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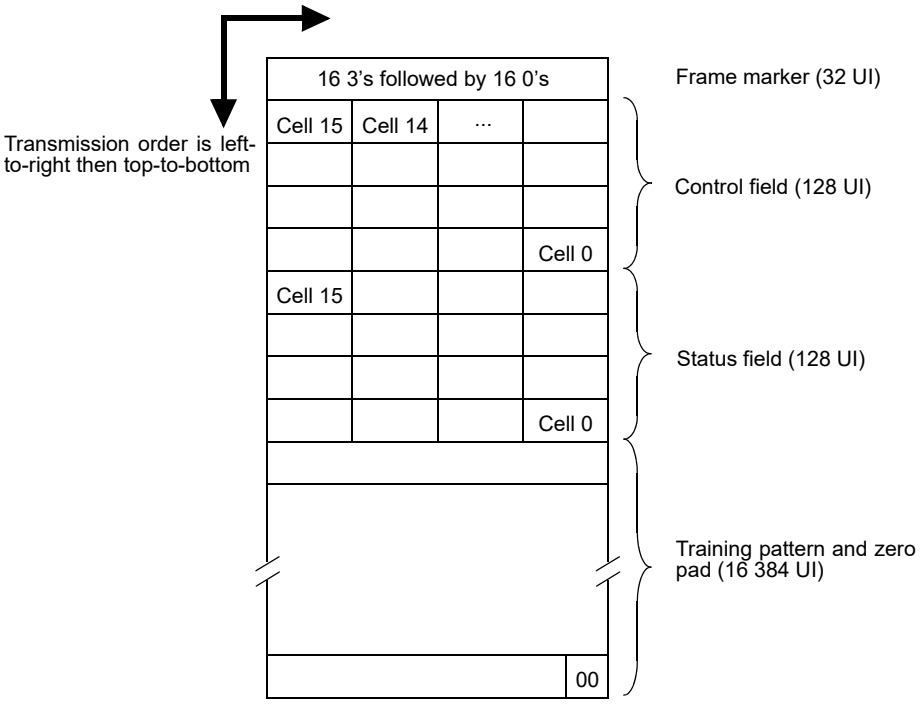

Figure 136–3—Training frame structure

136.8.11.1.1 Frame marker

Training frames are delimited by a specific sequence of PAM4 symbols. The training frame marker is a run of 16 consecutive "3" symbols followed by a run of 16 consecutive "0" symbols. This sequence is not found in the control field, status field, or training pattern and it uniquely identifies the beginning of a training frame.

136.8.11.1.2 Control and status fields

The control field comprises 16 bits with the structure defined in 136.8.11.2. The status field comprises 16 bits with the structure defined in 136.8.11.3.

Each bit of the control and status fields is sent as a differential Manchester encoded (DME) cell, where each cell is eight unit intervals in length. The specific rules for this encoding follow.

a) A transition from 0 to 3 or from 3 to 0 occurs at the start of each cell.
b) A transition from 0 to 3 or from 3 to 0 at the midpoint of a cell, i.e., four unit intervals from the transition at the beginning of the cell, corresponds to a logical one.
c) The absence of a transition at the midpoint of a cell corresponds to a logical zero.

The control field is transmitted immediately after the frame marker. The status field is transmitted immediately after the control field. Within each field, the order of transmission is from bit 15 to bit 0.

When a training frame is received, if a violation of the DME encoding rules is detected within the control field or the status field, the contents of both fields in that frame are ignored.

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136.8.11.1.3 Training pattern

The training pattern is the result of a training pattern generator equivalent to the structure shown in Figure 136–4.

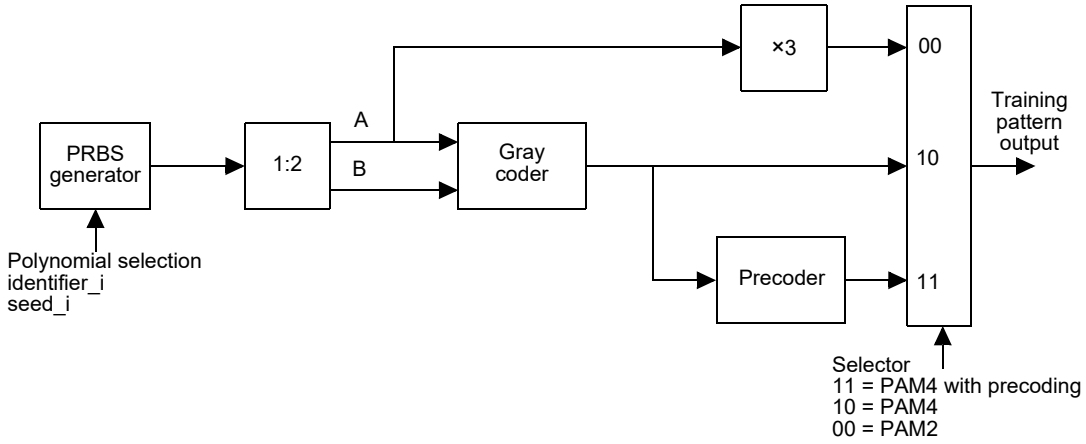

Figure 136–4—Training pattern generator

A set of four PRBS generator polynomials are defined to minimize correlated interference between PMDs, or physical lanes within a PMD, during the startup protocol. The PRBS generator for each lane shall implement each of four generator polynomials defined in Table 136–8. The polynomial used in each lane *i* is selectable by identifier_*i*. The default identifier for each lane is its lane number (e.g., the default value for identifier_0 is 0 which selects polynomial_0). A sample implementation of the PRBS generator for identifier_*i* = 0 is shown in Figure 136–5.

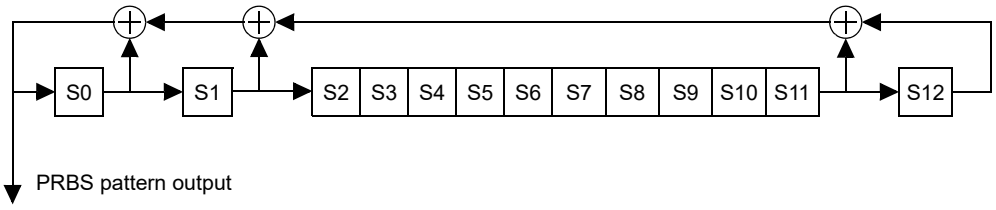

Figure 136–5—Training pattern PRBS generator (identifier_*i* = 0)

At the start of the training pattern, the state of the PRBS generator shall be set to the value seed_*i*. The default value of seed_*i* shall be the value given in Table 136–8 for $p = i$. A seed of all zeros is not valid.

The polynomials for each identifier value p and the default seeds, as well as the first 13 symbols of the training pattern for each modulation and precoding mode, using the default seed, are provided in Table 136–8.

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Table 136–8—Training patterns

p	Polynomial_*p*, *G*(*x*)	Default seed bits[a]	Initial output, PAM2	Initial output, PAM4	Initial output, PAM4 with precoding
0	$1+x+x^2+x^{12}+x^{13}$	0000010101011	0030330330000	1031320220111[b]	1301200200101
1	$1+x^2+x^3+x^7+x^{13}$	0011101000001	3030303030333	3030213021333	3122012201212
2	$1+x^2+x^4+x^8+x^{13}$	1001000101100	0303333033030	1212332133031	1102120121301
3	$1+x^2+x^5+x^9+x^{13}$	0100010000010	3330300030330	2231210121221	2032013201110

[a]The leftmost bit in the sequence corresponds to the initial value of S0 and the rightmost bit corresponds to the initial value of S12.
[b]This is equivalent to the PRBS13Q test pattern defined in 120.5.11.2.1.

For a given configuration of the PRBS generator, there are three possible training patterns. The construction of each training pattern begins by demultiplexing the PRBS generator output into pairs of bits {A, B} where A corresponds to the 1st, 3rd, 5th, etc. bits output by the PRBS generator and B corresponds to the 2nd, 4th, 6th, etc. bits output by the PRBS generator. There is a new pair of bits each unit interval which implies that the PRBS generator is required to generate bits at twice the signaling rate. Given these pairs of bits, the three different training patterns correspond to three modulation and precoding modes: PAM2, PAM4, PAM4 with precoding.

When the modulation and precoding mode is set to PAM2, the training pattern is the sequence of 16 382 PAM4 symbols derived by mapping only the A bits such that logical 0 is transmitted as 0 and logical 1 is transmitted as 3.

When the modulation and precoding mode is set to PAM4, the training pattern is the sequence of 16 382 PAM4 symbols derived by Gray coding the {A, B} pairs as specified in 135.5.7.1.

When the modulation and precoding mode is set to PAM4 with precoding, the training pattern is the sequence of 16 382 PAM4 symbols derived by Gray coding the {A, B} pairs as specified in 135.5.7.1 and precoding the result as specified in 135.5.7.2. The precoder state is initialized to 0 at the beginning of each training pattern, so that P(j–1)=0 in Equation (135–1) for the first PAM4 symbol of the training pattern.

The modulation and precoding mode is set to PAM2 upon entry to the INITIALIZE state of the PMD control state diagram (see Figure 136–7).

NOTE—Exiting TRAINING mode requires both sides to use PAM4 modulation, thus the request and the status of the modulation and precoding are both required to have values other than PAM2 (either “PAM4” or “PAM4 with precoding”).

136.8.11.1.4 Zero pad

Two “0” symbols are transmitted immediately after the training pattern. This zero pad ensures the training frame is DC balanced and helps to delineate the start of the frame marker for the next training frame.

136.8.11.2 Control field structure

The structure of the control field shall be as shown in Table 136–9.

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Table 136–9—Control field structure

Bit(s)	Name	Description
15:14	Reserved	Transmit as 0, ignore on receipt
13:12	Initial condition request	13 12 1 1 = Preset 3 1 0 = Preset 2 0 1 = Preset 1 0 0 = Individual coefficient control
11:10	Reserved	Transmit as 0, ignore on receipt
9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2
7:5	Reserved	Transmit as 0, ignore on receipt
4:2	Coefficient select	4 3 2 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$
1:0	Coefficient request	1 0 1 1 = No equalization 1 0 = Decrement 0 1 = Increment 0 0 = Hold

136.8.11.2.1 Initial condition request

The initial condition request bits are used to select one of the three predefined transmitter equalizer configurations (presets) specified in 136.9.3.1.3. When the initial condition request bits are 00, the coefficient select and coefficient request bits are used to update the transmitter equalizer configuration.

136.8.11.2.2 Modulation and precoding request

The modulation and precoding request bits are used to request that the link partner transmitter transmit one of the three training pattern formats defined in 136.8.11.1.3.

136.8.11.2.3 Coefficient select

The coefficient select bits are used to identify the coefficient that is the target of a coefficient request. The value of the field is the two's complement encoding of the coefficient index. For example, binary value 111 corresponds to a coefficient index of –1.

136.8.11.2.4 Coefficient request

The coefficient request bits are used to change the value of the coefficient specified by the coefficient select bits. A coefficient may be changed by incrementing or decrementing its value or by setting it to "No equalization". The "No equalization" value is 1 for $c(0)$ and 0 for $c(-2)$, $c(-1)$, and $c(1)$.

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136.8.11.3 Status field structure

The structure of the status field is shown in Table 136–10.

Table 136–10—Status field structure

Bit(s)	Name	Description
15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue
14:12	Reserved	Transmit as 0, ignore on receipt
11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2
9	Receiver frame lock	1 = Frame boundaries identified 0 = Frame boundaries not identified
8	Initial condition status	1 = Updated 0 = Not updated
7	Parity	Even parity bit
6	Reserved	Transmit as 0, ignore on receipt
5:3	Coefficient select echo	5 4 3 1 1 0 = $c(-2)$ 1 1 1 = $c(-1)$ 0 0 0 = $c(0)$ 0 0 1 = $c(1)$
2:0	Coefficient status	2 1 0 1 1 1 = Reserved 1 1 0 = Coefficient at limit and equalization limit 1 0 1 = Reserved 1 0 0 = Equalization limit 0 1 1 = Coefficient not supported 0 1 0 = Coefficient at limit 0 0 1 = Updated 0 0 0 = Not updated

136.8.11.3.1 Receiver ready

The receiver ready bit is used to signal the local receiver state to the link partner. When this bit is 1, it indicates that the local receiver has completed training and is prepared to receive data (local_rx_ready = true). When this bit is 0, it indicates that the local receiver is requesting that training continue (local_rx_ready = false).

136.8.11.3.2 Modulation and precoding status

The modulation and precoding status bits encode the value of local_tp_mode.

136.8.11.3.3 Receiver frame lock

When the receiver frame lock bit is set to 1, the receiver is indicating that it has identified training frame marker positions and is in a state where the response time requirements specified in 136.8.11.6 are met.

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Receiver frame lock shall be set to 0 when the variable training is false, and shall not be set to 1 until training and local_tf_lock are both true.

136.8.11.3.4 Initial condition status

The initial condition status bit acknowledges the initial condition request bits received from the link partner. The acknowledgment reflects the value of ic_sts resulting from the procedure described in 136.8.11.4.1.

136.8.11.3.5 Parity bit

The parity bit is calculated based on the other bits in the control field and status field to create even parity for these fields. Even parity ensures that the transmitted control and status fields (see 136.8.11.1.2) are DC balanced. This field is ignored on receipt.

136.8.11.3.6 Coefficient select echo

The coefficient select echo bits acknowledge the coefficient select bits received from the link partner. When a change to the coefficient select bits is detected, the coefficient select echo bits are updated to represent the same coefficient index. This serves as a confirmation to the link partner that subsequent coefficient requests will act on the targeted coefficient.

136.8.11.3.7 Coefficient status

The coefficient status bits acknowledge the coefficient request bits received from the link partner. The acknowledge reflects the value of coef_sts resulting from the procedure described in 136.8.11.4.3.

136.8.11.4 Equalization control

When the PMD control state diagram (Figure 136–7) is in the TRAIN_LOCAL state, a PMD may request its link partner to change the transmitter equalization coefficients, either to predefined initial conditions or by individual coefficient control. The criteria for initiating such requests are implementation dependent.

A new individual coefficient update request or initial condition update request is not initiated until after the prior request has completed.

136.8.11.4.1 Initial condition setting request process

A request to change the initial condition of the link partner's transmitter is made by using the following procedure:

a) Set the initial condition request bits (136.8.11.2.1) to the desired predefined transmitter equalizer configuration (preset) and the coefficient request bits (136.8.11.2.4) to "hold".
b) Wait until the initial condition status bits (136.8.11.3.4) indicate "updated" and the coefficient status bits (136.8.11.3.7) indicate "not updated".
c) Set the initial condition request bits (136.8.11.2.1) to individual coefficient control and the coefficient request bits (136.8.11.2.4) to "hold".
d) Wait until both the initial condition status bits (136.8.11.3.4) and the coefficient status bits (136.8.11.3.7) indicate "not updated".

136.8.11.4.2 Initial condition setting response process

The handling of incoming requests is specified by the coefficient update state diagram (Figure 136–9). The behavior of the UPDATE_IC function is consistent with the following algorithm.

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```
if ic_req = ind_ctl
   ic_sts = not_upd
else
   if ic_req = preset 1
      Set coefficients to preset 1
   else if ic_req = preset 2
      Set coefficients to preset 2
   else if ic_req = preset 3
      Set coefficients to preset 3
   end if
   ic_sts = updated
end if
```

The variables ic_req and ic_sts are defined in 136.8.11.7.1. The transmitter equalizer coefficients corresponding to each of the three presets shall be within the ranges specified in Table 136–12.

The transmitter equalizer is set to preset 1 upon entry to the INITIALIZE state of the PMD control state diagram.

136.8.11.4.3 Coefficient update request process

A request to change an individual equalizer coefficient of the link partner's transmitter is made by using the following procedure:

a) In the transmitted control field, set the initial condition request bits (136.8.11.2.1) to individual control, and set the coefficient select bits (136.8.11.2.3) and coefficient request bits (136.8.11.2.4) to the desired values. This may be done in one step (all fields updated in the same training frame) or sequentially.

b) Wait until the received coefficient status bits (136.8.11.3.7) do not indicate "not updated" and the coefficient select echo bits (136.8.11.3.6) indicate the requested coefficient select value.

c) If the subsequent request is to change the same coefficient or request a new initial condition, set the coefficient request bits (136.8.11.2.4) to "hold" and wait until the received coefficient status bits (136.8.11.3.7) indicate "not updated".

136.8.11.4.4 Coefficient update response process

The handling of incoming requests is specified by the coefficient update state diagram (Figure 136–9). The behavior of the UPDATE_C(k) function is consistent with the following algorithm.

```
if k in k_list

   if coef_req = INCREMENT
      ck_ask = c(k) + ck_stp
   else if coef_req = DECREMENT
      ck_ask = c(k) – ck_stp
   else if coef_req = NO EQUALIZATION
      if k = 0
         ck_ask = 1
      else
         ck_ask = 0
      end if
   else
      ck_ask = c(k)
   end if

   if ck_ask > ck_max
      c(k) = ck_max
```


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```
      if CHECK_EQ(ck_ask,k)
         coef_sts = COEFFICIENT AT LIMIT AND EQUALIZATION LIMIT
      else
         coef_sts = COEFFICIENT AT LIMIT
      end if
   else if ck_ask < ck_min
      c(k) = ck_min
      if CHECK_EQ(ck_ask,k)
         coef_sts = COEFFICIENT AT LIMIT AND EQUALIZATION LIMIT
      else
         coef_sts = COEFFICENT AT LIMIT
      end if
   else if CHECK_EQ(ck_ask,k)
      coef_sts = EQUALIZATION LIMIT
   else
      c(k) = ck_ask
      coef_sts = UPDATED
   end if
else
   coef_sts = COEFFICIENT NOT SUPPORTED
end if
```

The variables coef_req, coef_sts, and k are defined in 136.8.11.7.1. The following additional variables and functions are used.

c(k)
: Variable that contains the current value of the coefficient *c*(k).

ck_ask
: Variable that contains the value of *c*(k) that would result from the requested update.

ck_min
: Variable that contains the minimum supported value of *c*(k).

ck_max
: Variable that contains the maximum supported value of *c*(k).

ck_stp
: Variable that contains the magnitude of the change in *c*(k) for one step up or one step down from its current value.

k_list
: The set of valid transmitter equalizer coefficient indices {–2, –1, 0, 1}.

CHECK_EQ(ck_ask,k)
: Compares the transmitter's steady-state voltage that would result from setting transmit equalization coefficient *c*(k) value to ck_ask, while keeping all other coefficients unchanged, against the transmitter's steady-state voltage (see 136.9.3.1.2) and equalization capability. Returns true if the resulting combination of coefficients would exceed the maximum steady-state voltage or the transmitter's equalization capability. Otherwise returns false.

136.8.11.5 Modulation and precoding setting

When a change to the modulation and precoding request bits is detected, the modulation and precoding mode of the transmitted training pattern (see 136.8.11.1.3) is set accordingly, and the local_tp_mode variable is then set to the value of the modulation and precoding request bits to confirm that the change to the format of the training pattern was completed. local_tp_mode is encoded in the status field (see 136.8.11.3.2).

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136.8.11.6 Handshake timing

Changes to the configuration of the transmitter equalizer or the transmitted training pattern may occur at any point between the time the request for the new configuration is received and the time that the request is acknowledged.

When the receiver frame lock bit in the status field of transmitted training frames is set to 1, the time from the receipt of a new request to the acknowledgment of that request shall be less than 2 ms. A new request is defined to be a received training frame whose control field differs from the control field of the preceding training frame. An acknowledgment is defined as the first transmitted training frame that contains a status field encoding that is an appropriate response for the requested action. For example, a change in the coefficient select bits in the control field would be acknowledged by a change in the coefficient select echo bits of the status field. Similarly, a change in the modulation and precoding request bits in the control field would be acknowledged by a change in the modulation and precoding status bits in the status field. All timing measurements are referred to a common reference point within the training frame (e.g., the 3 to 0 transition in the training frame marker).

The timing of requests and acknowledgment is illustrated in Figure 136–6.

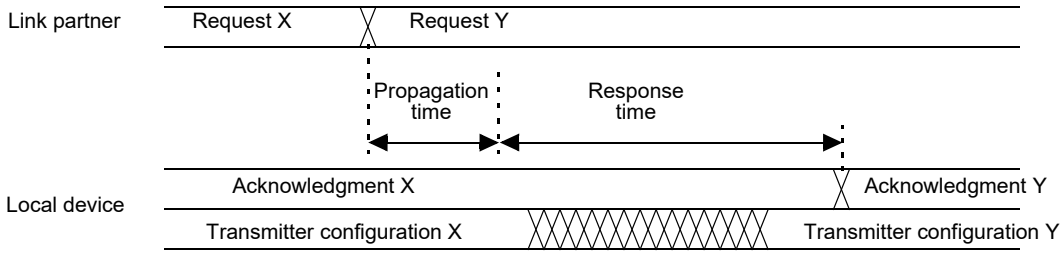

Figure 136–6—Transmitter update timing

136.8.11.7 Variables, functions, timers, counters, and state diagrams

The PMD implements one instance of each of the PMD control state diagrams, and the set of associated variables, functions, counters and timers defined in this subclause, independently for each of the n physical lanes.

136.8.11.7.1 Variables

coef_req

Enumerated variable derived from the “coefficient request” bits from the control field of the received training frames (see 136.8.11.2). This variable may be one of the following values: hold, decrement, increment, no equalization.

coef_sel

Variable derived from the “coefficient select” bits from the control field of the received training frames (see 136.8.11.2). It is assigned a signed integer value that is the two’s complement interpretation of the bits.

coef_sts

Enumerated variable that may be assigned one of the following values (abbreviations used by the state diagram are included in parentheses): not updated (not_upd), updated, coefficient at limit, coefficient not supported, equalization limit, coefficient at limit and equalization limit. The value is assigned by the UPDATE_C(k) function and Coefficient update state diagram

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(Figure 136–9), and then encoded in the status field of transmitted training frames via the ENCODE_STS function.

ic_req

Enumerated variable derived from the "initial condition request" bits from the control field of the received training frames (see 136.8.11.2). This variable may be assigned one of the following values (abbreviations used by the state diagram are included in parentheses): individual control (ind_ctl), preset 1, preset 2, preset 3.

ic_sts

Enumerated variable that may be assigned one of the following values (abbreviations used by the state diagram are included in parentheses): not updated (not_upd), updated.

k

Variable that stores the most recent value of coef_sel.

local_rx_ready

Boolean variable that is set to true by the training state diagram when local_trained is asserted and is set to false otherwise. This value is encoded as the "receiver ready" bit in the status field of transmitted training frames.

local_tf_lock

Boolean variable that is true when the training frame marker positions have been identified and is false otherwise.

local_tp_mode

Enumerated variable that controls the modulation and precoding mode in the transmitted training pattern (see 136.8.11.1.3) and may be assigned one of the following values: pam2, pam4, pam4 with precoding.

local_trained

Boolean variable that is set to true when the local receiver has determined that the remote transmit and local receive equalizers have been optimized and normal data transmission may commence. It is set to false otherwise. The exact criteria for setting this variable to true are implementation specific.

lost_training_lock

Boolean variable that indicates disruption in the reception of training frames from the link partner. When use_quiet_in_training is TRUE and the PMD control function (see Figure 136–7) is in TRAIN_LOCAL or TRAIN_REMOTE states, this variable is set to TRUE if local_tf_lock is FALSE continuously for a period of 20 ms, and may also be set to TRUE upon detection of an input signal consistent with a transmitter operating in the QUIET operating mode (see 136.8.2). It is set to FALSE otherwise.

marker_valid

Boolean variable that is set to true when the candidate frame marker matches the frame marker pattern defined in 136.8.11.1.1 and is set to false otherwise.

mr_restart_training

Boolean variable used by system management to restart the startup protocol. When set to true, it forces the PMD control state diagram to the INITIALIZE state.

mr_training_enable

Boolean variable used by system management to enable or disable the startup protocol. When set to true it enables the startup protocol, and when set to false it disables the startup protocol.

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new_marker
: Boolean variable that is set to true when a new candidate frame marker is available for testing and is set to false when the TEST_MARKER state is entered. A new frame marker is available for testing when the training frame lock process has accumulated 32 consecutive symbols starting at the candidate frame start position.

remote_rx_ready
: Boolean variable derived from the "receiver ready" bit of the status field of received training frames. The value of remote_rx_ready shall not be set to TRUE until no fewer than three consecutive training frames have been received with the "receiver ready" bit asserted.

remote_tf_lock
: Boolean variable derived from the "receiver frame lock" bit of the status field of received training frames. The value of remote_tf_lock shall not be set to TRUE until no fewer than three consecutive training frames have been received with the "receiver frame lock" bit asserted.

remote_tp_mode
: Enumerated variable that corresponds to the "modulation and precoding status" bits in the status field of received training frames. It may be assigned one of the following values: pam2, pam4, pam4 with precoding.

reset
: Boolean variable that resets the PMD. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PMD into low-power mode. It is false otherwise.

signal_detect
: Boolean variable that is set to true when the training process is complete and is set to false otherwise. The value of signal_detect is used by the PMD lane-by-lane signal detect function (136.8.5).

slip_done
: Boolean variable that is set to TRUE when the SLIP requested by the Training frame lock state diagram (Figure 136–8) is completed indicating that the next candidate frame sync position can be tested.

tf_offset
: Boolean variable that is set to true when receiving one full training frame (16 672 symbols, see 136.8.11.1) following the recent frame start position, such that a new frame marker is expected. Otherwise it is set to false

training
: Boolean variable that is set to true when the startup protocol is in progress and is set to false otherwise.

training_failure
: Boolean variable that is set to true when training failed to complete successfully within the allotted time limit. Otherwise it is set to false.

use_quiet_in_training
: Boolean variable that is TRUE if the PMD control function (see Figure 136–7) can enter the QUIET state. The value of this variable is implementation dependent.

136.8.11.7.2 Functions

ENCODE_STS
: Encodes portions of the status field of transmitted training frames. k is mapped to the coefficient select echo bits, coef_sts is mapped to the coefficient status bits, and ic_sts is mapped to the initial condition status bit.

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SLIP

Causes the next candidate frame marker position to be tested. Repeated invocations of SLIP cause all possible positions to be evaluated. The precise method for determining the next candidate frame marker position is implementation dependent and beyond the scope of this standard.

TRANSMIT(tx_mode)

Controls the output of the PMD transmit function on the current lane. When tx_mode = DATA, the PMD transmit function output is the parameter of the PMD:IS_UNITDATA_*i*.request primitive (see 136.3). When tx_mode = TRAINING, the PMD transmit function output is the stream of symbols generated by the PMD control function. When tx_mode = QUIET, the PMD transmitter is turned off, equivalent to setting PMD_transmit_disable_*i* to one (see 136.8.7)

UPDATE_C(k)

Updates the value of *c*(k) based on the current values of the variables k and coef_req. The result of the update is stored in the variable coef_sts. This function implements the algorithm specified in 136.8.11.4.4.

UPDATE_IC

Updates all transmit equalizer coefficients based on the current value of the variable ic_req. The result is stored in the variable ic_sts. This function implements the algorithm specified in 136.8.11.4.2.

136.8.11.7.3 Timers

holdoff_timer

This timer is started when the PMD control state diagram enters the TIMEOUT state or the QUIET state. The terminal count of holdoff_timer is 80 ms ± 2%.

max_wait_timer

This timer sets the limit for how long the PMD startup protocol is allowed to operate. If the timer expires before the LINK_READY state is reached, then a failure to train is indicated. The terminal count of max_wait_timer is 3 s ± 2%.

wait_timer

This timer is started when the local receiver has completed training and detects that the remote receiver is ready to receive data. The local transmitter sends additional training frames until the timer expires to ensure that the link partner correctly detects the local receiver state. The terminal count of wait_timer is between 25 µs and 125 µs, equivalent to approximately 40 to 200 training frames.

136.8.11.7.4 Counters

bad_markers

Count of the number of consecutive frame marker mismatches.

good_markers

Count of the number of consecutive frame marker matches.

136.8.11.7.5 State diagrams

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter indicates that its value is to be incremented.

The PMD control state diagram (Figure 136–7) defines the operation of the startup protocol.

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If the LINK_READY state is entered with local_tp_mode set to “PAM4 with precoding”, then the PMD shall cause the adjacent PMA to transmit all subsequent data on the corresponding lane with precoding (see 135.5.7.2 and 120.5.7.2).

If the LINK_READY state is entered with remote_tp_mode set to “PAM4 with precoding”, then the PMD shall inform the adjacent PMA that all subsequently received data on the corresponding lane includes precoding (see 135.5.7.2 and 120.5.7.2).

The PMD control state diagram is supported by the training frame lock and coefficient update state diagrams. The training frame lock state diagram (Figure 136–8) determines when the PMD control function has detected training frame boundaries. The coefficient update state diagram (Figure 136–9) defines the process for updating the local transmitter equalizer coefficients in response to requests from the link partner.

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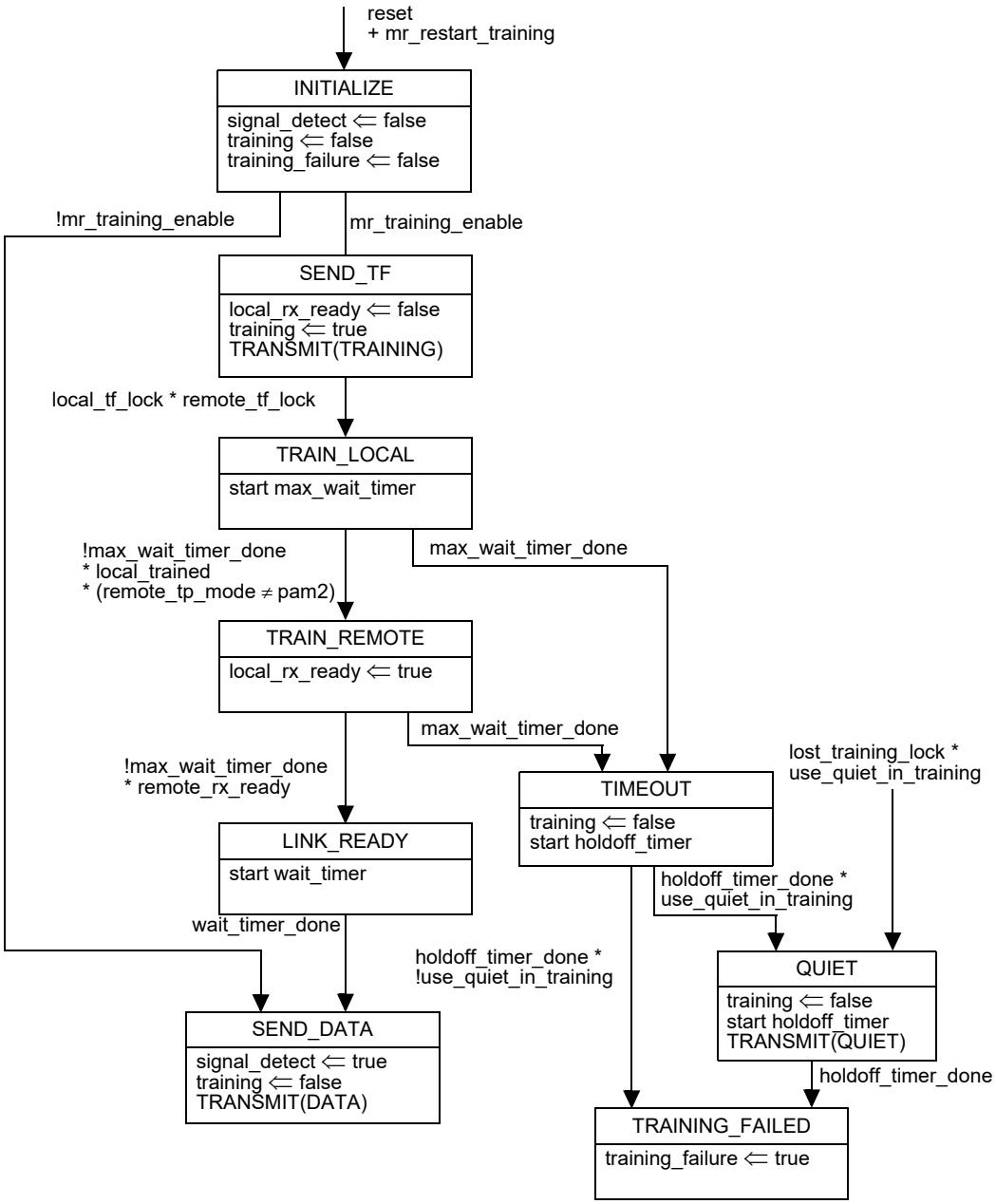

Figure 136–7—PMD control state diagram

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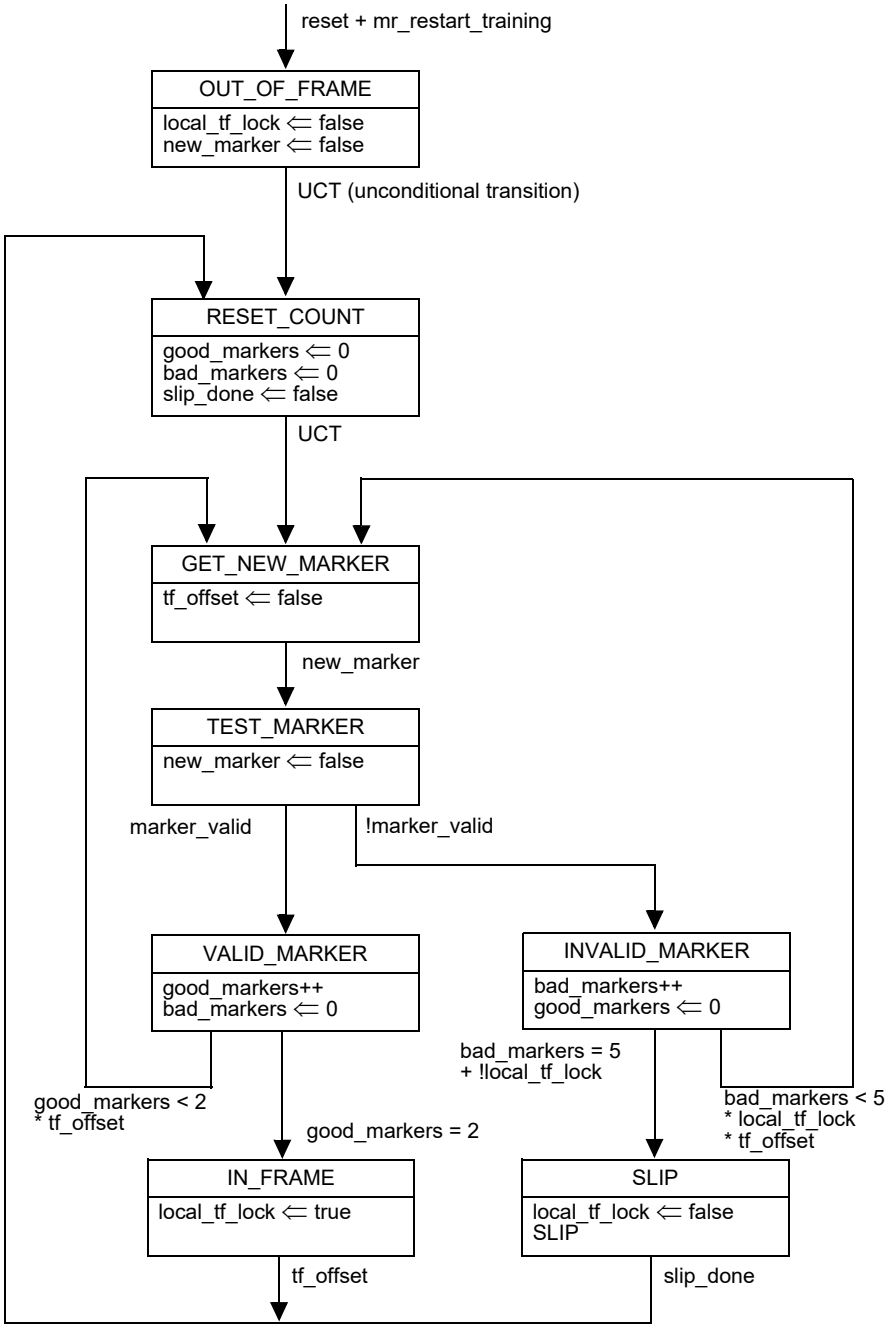

Figure 136–8—Training frame lock state diagram

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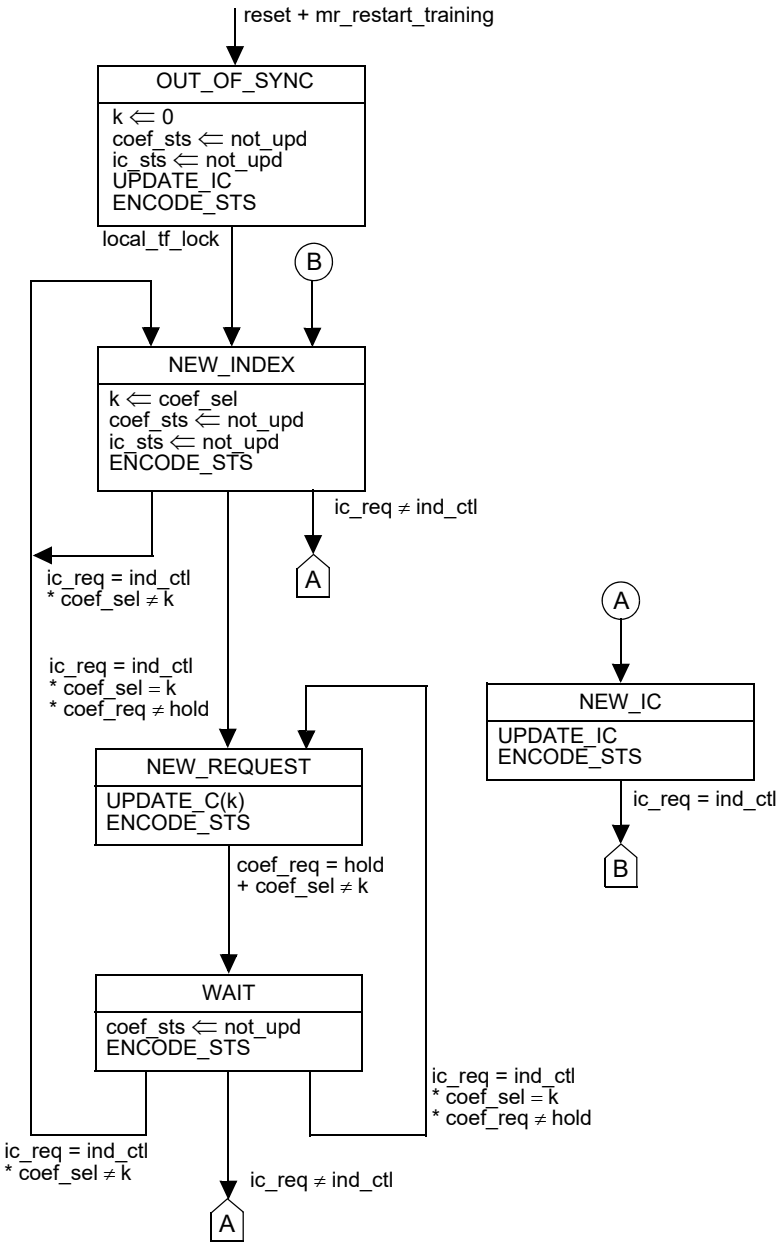

Figure 136–9—Coefficient update state diagram

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136.9 PMD electrical characteristics

136.9.1 AC-coupling

Interoperability between PMD components operating from different supply voltages is facilitated by AC-coupling within the cable assembly (as specified in 136.11).

136.9.2 Signal paths

The MDI transmit and receive paths are point-to-point connections. Each path corresponds to one MDI lane and comprises two complementary signals, which form a balanced differential pair.

For 50GBASE-CR, there is one differential path in each direction for a total of two pairs, or four connections. For 100GBASE-CR2, there are two differential paths in each direction for a total of four pairs, or eight connections. For 200GBASE-CR4, there are four differential paths in each direction for a total of eight pairs, or sixteen connections.

136.9.3 Transmitter characteristics

The transmitter on each lane shall meet the specifications given in Table 136–11 and detailed in the referenced subclauses. Unless specified otherwise, all transmitter measurements are made for each lane separately, at TP2, utilizing the test fixtures specified in Annex 136B, using a test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth. The connection from TP2 to the test equipment is AC-coupled.

Measurement of the DC common-mode voltage is made with a high-impedance connection to TP2 where each conductor of the differential pair is AC-coupled to a 50 Ω termination.

The transmitter characteristics at TP0 are provided informatively in 136A.2.

Table 136–11—Summary of transmitter specifications at TP2

Parameter	Subclause reference	Value	Units
Differential pk-pk output voltage (max.) with Tx disabled[a]	93.8.1.3	30	mV
DC common-mode voltage (max.)[a]	93.8.1.3	1.9	V
AC common-mode RMS output voltage, v_{cmi} (max.)[a]	93.8.1.3	30	mV
Differential pk-pk voltage, v_{di} (max.)[a]	93.8.1.3	1200	mV
Effective return loss (ERL) (min.)	136.9.3.4	See Equation (136–6)	dB
Common-mode to differential mode output return loss (min.)	92.8.3.3	See Equation (92–2)	dB
Common-mode to common-mode output return loss (min.)	92.8.3.4	See Equation (92–3)	dB
Transmitter steady-state voltage, v_f (min.) Transmitter steady-state voltage, v_f (max.)	136.9.3.1.2	0.354 0.6	V
Linear fit pulse peak (min.)	136.9.3.1.2	$0.49 \times v_f$	V
Level separation mismatch ratio R_{LM} (min.)	120D.3.1.2	0.95	—

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Table 136–11—Summary of transmitter specifications at TP2 *(continued)*

Parameter	Subclause reference	Value	Units
Transmitter output waveform			
abs step size for $c(-1)$, $c(0)$, and $c(1)$ (min.)	136.9.3.1.4	0.005	—
abs step size for $c(-1)$, $c(0)$, and $c(1)$ (max.)	136.9.3.1.4	0.05	—
abs step size for $c(-2)$ (min.)	136.9.3.1.4	0.005	—
abs step size for $c(-2)$ (max.)	136.9.3.1.4	0.025	—
value at minimum state for $c(-1)$ and $c(1)$ (max.)	136.9.3.1.5	−0.25	—
value at maximum state for $c(-2)$ (min.)	136.9.3.1.5	0.1	—
Signal-to-noise-and-distortion ratio SNDR (min.)	120D.3.1.6	32.2	dB
Output jitter (max.)[b]			
J_{RMS}	120D.3.1.8	0.023	UI
J3u	136.9.3.3	0.115	UI
Even-odd jitter, pk-pk[c]	120D.3.1.8	0.019	UI
Signaling rate		26.5625 ± 100 ppm	GBd
Unit interval nominal		37.64706	ps

[a]Measurement uses the method described in 93.8.1.3 with the exception that the PRBS13Q test pattern is used.
[b]J3u, J_{RMS}, and even-odd jitter measurements are made with a single transmit equalizer setting selected to compensate for the loss of the host channel.
[c]If the measuring instrument is triggered by a clock based on the signaling rate divided by an even number, the even-odd jitter may not be correctly observed.

136.9.3.1 Transmitter output waveform

The transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer on each lane is the four-tap transversal filter shown in Figure 136–10.

The state of the transmit equalizer and hence the transmitted output waveform may be manipulated via the PMD control function defined in 136.8.11 or via the management interface. The transmit function responds to a set of commands issued by the link partner's receive function and conveyed by a back-channel communications path. This command set includes instructions to increment, decrement, hold, or set to zero a selected coefficient $c(k)$, where $k = -2$ to 1. In addition, it includes commands to set all coefficients to one of three initial conditions.

In response, the transmit function relays status information to the link partner's receive function. The status messages indicate the selected coefficient index k, the status of the coefficient $c(k)$ (updated, not updated, or at limit), and the status of the initial condition (updated or not updated).

136.9.3.1.1 Linear fit to the measured waveform

The following procedure is used to determine the linear fit pulse response, linear fit error, and normalized transmitter coefficient values.

Set the transmitter under test to transmit the PRBS13Q test pattern (defined in 120.5.11.2.1). For each configuration of the transmit equalizer, capture at least one complete cycle of the test pattern at TP2, as specified in 85.8.3.3.4. The clock recovery unit (CRU) used in the measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade.

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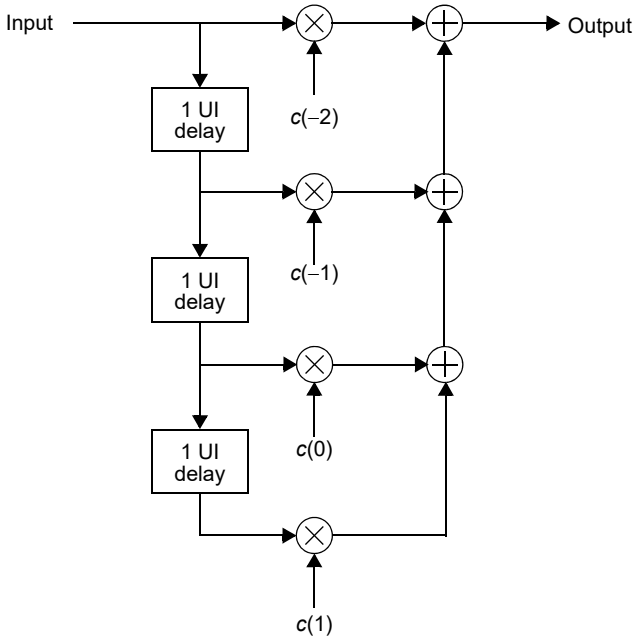

Figure 136–10—Transmit equalizer functional model

In the following calculations, M should be an integer not less than 32. Interpolation of the captured waveform may be used to achieve this.

Compute the linear fit pulse response $p(k)$, k=1 to $M \times N_p$, from the captured waveform, as specified in 85.8.3.3.5, with $N_p = 200$ and $D_p = 3$, where the aligned symbols $x(n)$ are assigned normalized amplitudes −1, −*ES*, *ES*, and 1 to represent the PAM4 symbol values 0, 1, 2, and 3 respectively. *ES* is defined as $(|ES1| + |ES2|)/2$ where *ES1* and *ES2* are calculated according to 120D.3.1.2.

Define $r(k)$ to be the linear fit pulse response when transmit equalizer coefficients have been set to the "pre-set 1" values. The normalized coefficients for any configuration of the transmit equalizer are computed using the following method.

For each value of m in the range $-M/2$ to $M/2-1$ when M is even and $-(M-1)/2$ to $(M-1)/2$ when M is odd:

a) Define an $M \times N_p$-by-4 matrix R_m. The elements of R_m are assigned values per Equation (136–1) where $i = -2$ to 1 and $j = 1$ to $M \times N_p$.

$$R_m(j, i+3) = \left\{ \begin{array}{ll} r(m+j-M\times i) & \text{if } 1 \le m+j-M\times i \le M\times N_p \\ 0 & \text{otherwise} \end{array} \right\} \tag{136–1}$$

b) The normalized coefficients of the transmit equalizer are computed using Equation (136–2).

$$\begin{bmatrix} c_m(-2) \\ c_m(-1) \\ c_m(0) \\ c_m(1) \end{bmatrix} = (R_m^T R_m)^{-1} R_m^T \begin{bmatrix} p(1) \\ \dots \\ p(M\times N_p) \end{bmatrix} \tag{136–2}$$

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c) The linear fit pulse response is reconstructed from the matrix R_m and the normalized coefficients using Equation (136–3).

$$\begin{bmatrix} p_m(1) \\ \cdots \\ p_m(M \times N_p) \end{bmatrix} = R_m \begin{bmatrix} c_m(-2) \\ c_m(-1) \\ c_m(0) \\ c_m(1) \end{bmatrix} \quad (136\text{–}3)$$

d) $\varepsilon^2(m)$ is computed using Equation (136–4).

$$\varepsilon^2(m) = \sum_{k=1}^{M \times N_p} (p(k) - p_m(k))^2 \quad (136\text{–}4)$$

The normalized transmit equalizer coefficients $c(i)$ for a given linear fit pulse $p(k)$ are the values $c_m(i)$ for the value of m that minimizes $\varepsilon^2(m)$.

136.9.3.1.2 Steady-state voltage and linear fit pulse peak

The steady-state voltage v_f is defined to be the sum of the linear fit pulse $p(1)$ through $p(M \times N_v)$ divided by M (refer to 85.8.3.3 step 3), where N_v represents the number of symbols to take into account and has a value of 13. The steady-state voltage shall be greater than or equal to 0.354 V and less than or equal to 0.6 V after the transmit equalizer initial condition has been set to preset 1 (no equalization).

The peak value of $p(k)$ shall be greater than $0.49 \times v_f$ after the transmit equalizer initial condition has been set to preset 1 (no equalization).

136.9.3.1.3 Coefficient initialization

When the Coefficient update state diagram (Figure 136–9) is in either the OUT_OF_SYNC state or the NEW_IC state, the coefficients of the transmit equalizer shall be configured to values within the ranges specified in Table 136–12 (according to the value of the variable ic_req). These requirements apply upon the assertion of Initial condition status of "Updated".

Table 136–12—Coefficient initial conditions

Coefficient update state	ic_req	$c(-2)$	$c(-1)$	$c(0)$	$c(1)$
OUT_OF_SYNC	N/A	0 ± 0.025	0 ± 0.05	1 ± 0.05	0 ± 0.05
NEW_IC	preset 1	0 ± 0.025	0 ± 0.05	1 ± 0.05	0 ± 0.05
	preset 2	0 ± 0.025	–0.15 ± 0.05	0.75 ± 0.05	–0.1 ± 0.05
	preset 3	0 ± 0.025	–0.25 ± 0.05	0.75 ± 0.05	0 ± 0.05

136.9.3.1.4 Coefficient step size

When coef_sel is –1, 0, or 1, the change in the normalized transmit equalizer coefficient c(coef_sel) corresponding to a request to "increment" shall be between 0.005 and 0.05, and the change in the normalized

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transmit equalizer coefficient c(coef_sel) corresponding to a request to "decrement" shall be between –0.05 and –0.005.

When coef_sel is –2, the change in the normalized transmit equalizer coefficient c(–2) corresponding to a request to "increment" shall be between 0.005 and 0.025, and the change in the normalized transmit equalizer coefficient c(coef_sel) corresponding to a request to "decrement" shall be between –0.025 and –0.005.

The coefficients other than c(coef_sel) are not expected to change. The absolute change in any coefficient other than c(coef_sel) shall be less than 0.005.

The change in the normalized transmit equalizer coefficient is defined to be the difference in the value measured prior to the assertion of the "increment" or "decrement" request (i.e., coef_req is "Hold") and the value upon the assertion of a coefficient status of "updated".

136.9.3.1.5 Coefficient range

When sufficient "increment" or "decrement" requests have been received for a given coefficient, the coefficient reaches a lower or upper bound based on the range of that coefficient or the combination of coefficients.

With $c(-2)$ and $c(-1)$ both set to zero and both $c(0)$ and $c(1)$ having received sufficient "decrement" requests so that they are at their respective minimum values, $c(1)$ shall be less than or equal to −0.25.

With $c(-2)$ and $c(1)$ set to zero and both $c(-1)$ and $c(0)$ having received sufficient "decrement" requests so that they are at their respective minimum values, $c(-1)$ shall be less than or equal to −0.25.

With $c(-1)$ and $c(1)$ set to zero, $c(0)$ having received sufficient "decrement" requests so that it is at its minimum value, and $c(-2)$ having received sufficient "increment" requests so that it is at its maximum value, $c(-2)$ shall be greater than or equal to 0.1.

NOTE—Any coefficient except c(0) may be set to zero by asserting a coefficient request of "no equalization" for that coefficient, using the control function specified in 136.8.11, or by implementation specific means.

136.9.3.2 Insertion loss, TP0 to TP2 or TP3 to TP5

The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is given by Equation (136–5). Note that the recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 is 10.07 dB at 13.28 GHz.

$$Insertion\_loss(f) \le \left\{ \begin{array}{ll} 0.08 + 0.57\sqrt{f} + 0.596f & 0.01 \le f < 14 \\ -19.109 + 2.119f & 14 \le f \le 19 \end{array} \right\} \text{(dB)} \qquad (136\text{–}5)$$

136.9.3.3 J3u jitter

J3u is calculated from a jitter measurement specified in 120D.3.1.8.1. J3u is defined as the time interval that includes all but 10^{-3} of $f_J(t)$, from the 0.05th to the 99.95th percentile of $f_J(t)$.

136.9.3.4 Transmitter effective return loss (ERL)

ERL of the transmitter at TP2 is computed using the procedure in 93A.5 with the values in Table 136–13. Parameters that do not appear in Table 136–13 take values from Table 136–18. The value of T_{fx} is twice the delay associated with the TP2 test fixture being used. N_{bx} is set to the value of N_b in Table 136–18.

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Table 136–13—Transmitter and receiver ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.0189	ns
Incremental available signal loss factor	β_x	1.7	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.3	—
Length of the reflection signal	N	300	UI

Transmitter ERL at TP2 shall meet Equation (136–6).

$$ERL \geq 40\log_{10}\left(\frac{v_f}{\max\limits_{k}(p(k))}\right) \quad \text{(dB)} \tag{136–6}$$

where

v_f is the steady-state voltage, defined in 136.9.3.1.2

$p(k)$ is the linear fit pulse at preset 1 (no equalization) (see 136.9.3.1.2)

136.9.4 Receiver characteristics

The receiver on each lane shall meet the specifications given in Table 136–14 and detailed in the referenced subclauses. Unless specified otherwise, all receiver measurements are made for each lane separately, at TP3, utilizing the test fixtures specified in Annex 136B.

The receiver specifications at TP5 are provided informatively in 136A.3.

Table 136–14—Summary of receiver specifications at TP3

Parameter	Subclause reference	Value	Units
Input amplitude tolerance	136.9.4.1	1200[a]	mV
Interference tolerance	136.9.4.2	Table 136–15	—
Jitter tolerance	136.9.4.3	Table 120D–7	—
Signaling rate	136.9.4.4	26.5625 ± 100 ppm	GBd
ERL (min.)	136.9.4.5	10	dB
Differential to common-mode input return loss	92.8.4.3	Equation (92–21)	dB

[a]Amplitude is measured at TP2.

136.9.4.1 Receiver input amplitude tolerance

When a PMD receiver is connected to a compliant transmitter whose peak-to-peak differential output voltage (see Table 136–11 footnote a) measured at the preset 1 equalizer setting is 1200 mV, using a compliant cable assembly with the minimum insertion loss specified in 136.11.2, the PMD receiver operation shall enable an FEC symbol error ratio better than 10^{-3} assuming errors are sufficiently

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uncorrelated to support the required frame loss ratio (see 136.1). If errors are not sufficiently uncorrelated, the FEC symbol error ratio shall be lower as appropriate to support the required frame loss ratio.

The receiver is allowed to control the transmitter equalizer coefficients, using the PMD control function defined in 136.8.11 or an equivalent process, to meet these requirements.

136.9.4.2 Receiver interference tolerance

Receiver interference tolerance is measured according to the procedure described in 136.9.4.2.1 through 136.9.4.2.5. Receiver interference tolerance test requirements are specified in Table 136–15.

Two tests are defined. Test 1 includes a low-loss channel. Test 2 includes a high-loss channel. The cable assembly used in the test channel (see 110.8.4.2.2) shall meet the cable assembly Channel Operating Margin (COM) as specified in 136.11.7.

Table 136–15—Interference tolerance test parameters

Parameter	Test 1 (low loss)		Test 2 (high loss)		Units
	Min	Max	Min	Max	
Test pattern	Scrambled idle encoded by RS-FEC				
FEC symbol error ratio required[a]	$< 10^{-3}$				
Test channel insertion loss at 13.28 GHz[b]	14.3	14.8	24.34	24.84	dB
Cable assembly insertion loss at 13.28 GHz	8	10	15.16	17.16	dB
COM[c]	3		3		dB

[a]See 136.9.4.2.5 for definition of FEC symbol error ratio.
[b]Insertion loss between the two test references (see Figure 110–3b).
[c]The COM value is the target value for the SNR_{TX} calibration defined in 136.9.4.2.3 item f. The SNR_{TX} value measured at the Tx test reference should be as close as practical to the value needed to produce the target COM. If lower SNR_{TX} values are used, this would demonstrate margin to the specification but this is not required for compliance.

136.9.4.2.1 Test setup

The interference tolerance test is performed with the setup similar to the one described in 110.8.4.2.1. The test setup includes noise injection for all lanes of the pattern generator.

136.9.4.2.2 Test channel

The test channel is the same as the one defined in 110.8.4.2.2, except that the cable assembly meets the requirements of 136.11 and the cable assembly test fixture meets the requirements of Annex 136B.

136.9.4.2.3 Test channel calibration

The scattering parameters of the test channel are measured at the test references as illustrated in Figure 110–3b using the cable assembly test fixtures specified in Annex 136B.

The insertion loss at 13.28 GHz of the signal path between the test references in Figure 110–3b is within the limits in Table 136–15.

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The COM is calculated using the method and parameters of 136.11.7 with the following considerations:

a) The channel signal path is $SCHS_p$ = cascade($S^{(CTSP)}$, $S^{(HOSP)}$), where cascade() is defined in 93A.1.2.1, $S^{(HOSP)}$ is defined in 136.11.7.1.1, and $S^{(CTSP)}$ is the measured channel between the test references in Figure 110–3b.

b) The COM parameters are as modified by Table 136–15.

c) COM is calculated using both Test 1 and Test 2 device package model transmission line lengths listed in Table 136–18 on the receiver side. The value of COM is taken as the lower of the two calculated values.

d) The augmented signal path in 93A.1.2 is replaced by S_p determined from Equation (136–7) (effectively omitting the transmitter device package model $S^{(tp)}$). The filtered voltage transfer function $H^{(k)}(f)$ calculated in Equation (93A–19) uses T_r equal to the 20% to 80% transition time at the Tx test reference. T_r is measured using the method in 120E.3.1.5 with the transmit equalizer turned off (i.e., coefficients set to the preset 1 values, see 136.9.3.1.3).

e) Even-odd jitter, J3u, and J_{RMS} without noise injection (see 136.9.4.2.4) are measured at the Tx test reference and comply with the specification in Table 136–11. In the calculation of COM, A_{DD} and σ_{RJ} are calculated from the measured values of J3u and J_{RMS} using Equation (136–8) and Equation (136–9), replacing the values in Table 136–18. It is recommended to adjust the pattern generator jitter such that J3u and J_{RMS} are as close as practical to their limits in Table 136–11.

f) The SNR_{TX} value that results in the required COM value for the test is calculated. The injected noise (see 136.9.4.2.4) is set such that the SNDR matches the calculated SNR_{TX} value. SNDR is measured at the Tx test reference using the procedure in 120D.3.1.6, with the exception that the linear fit in 120D.3.1.3 is performed with a pulse length (N_p) of 15 UI.

$$S_p = \text{cascade}(SCHS_p, S^{(rp)}) \tag{136–7}$$

where

cascade()	is defined in 93A.1.2.1
$SCHS_p$	is defined in item a) above
$S^{(rp)}$	is defined in 93A.1.2.4

$$A_{DD} = \frac{\frac{J3u}{2} + Q3\sqrt{(Q3^2+1)\times J_{RMS}^2 - \left(\frac{J3u}{2}\right)^2}}{Q3^2+1} \tag{136–8}$$

$$\sigma_{RJ} = \frac{\frac{J3u}{2} - A_{DD}}{Q3} \tag{136–9}$$

where $Q3 = 3.2905$

NOTE 1—$Q3$ is an approximated solution of $Q(Q3) = 5 \times 10^{-4}$, where the Q function is defined in Equation (95–1).

NOTE 2—Calculation of A_{DD} requires that $(Q3^2+1)\times J_{RMS}^2 \geq \left(\frac{J3u}{2}\right)^2$. If this does not hold, a different transmitter should be used in the test setup.

136.9.4.2.4 Pattern generator and noise injection

The pattern generator transmits data to all lanes of the device under test. At the start of transmitter training, the pattern generator output amplitude on all lanes shall be 800 mV peak-to-peak differential when measured on an alternating zero-three pattern. The output amplitude, measured on an alternating zero-three pattern, is not permitted to exceed 800 mV peak-to-peak differential during transmitter training. The output waveform and the ERL of the pattern generator shall comply with 136.9.3.

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Broadband noise is added to the signal before the Tx test reference, with noise level set according to step f in 136.9.4.2.3.

The broadband noise required for each lane is calibrated. The noise may be added either to one lane at a time or using multiple noise sources to all lanes at the same time.

136.9.4.2.5 Test procedure

The pattern generator is first configured to transmit the training pattern defined in 136.8.11. During this initialization period, the device under test (DUT) configures the pattern generator transmit equalizer to the coefficient settings it would select using the protocol described in 136.8.11 and the receiver is tuned using its optimization method. The coefficient settings may be communicated via the startup protocol or by other means.

After the pattern generator equalizer has been configured and the receiver tuned, the pattern generator is set to generate the test pattern specified in Table 136–15. During the test, the transmitters in the device under test transmit the same pattern type specified for the test, with equalization turned off (preset 1 condition).

Symbol error ratio is measured using the per-lane RS-FEC symbol error counters (see 91.6) in the adjacent RS-FEC sublayer, or the per-lane PCS symbol error counters (see 119.3.1) in the adjacent PCS, as appropriate.

The FEC symbol error ratio is defined as the sum of the symbol error counters on all lanes divided by the number of symbols transmitted on all lanes, which may be estimated from the test time.

A PHY shall meet the FEC symbol error ratio requirement in all tests defined in Table 136–15 with broadband noise added to all lanes (see 136.9.4.2.4). The FEC symbol error ratio requirement assumes errors are sufficiently uncorrelated to support the required frame loss ratio (see 136.1). If errors are not sufficiently uncorrelated, the FEC symbol error ratio shall be lower as appropriate to support the required frame loss ratio.

NOTE—If noise is applied to each of the n lanes one at a time, results of the n measurements are summed to yield the FEC symbol error ratio. The result may need to be corrected based on the FEC symbol error ratio with no noise added on any lane.

136.9.4.3 Receiver jitter tolerance

136.9.4.3.1 Test setup

Jitter tolerance is measured with a channel meeting the insertion loss of Test 2 as specified in Table 136–15. The pattern generator includes sinusoidal jitter injection.

136.9.4.3.2 Test procedure

The jitter tolerance test procedure is similar to that of 136.9.4.2, with the exception that no noise is injected (i.e., step f in 136.9.4.2.3 is not performed). Instead, jitter with the specified frequency and amplitude is applied to the pattern generator and the jitter amplitude is adjusted to obtain the peak-to-peak jitter specified for that frequency in Table 120D–7 at the Tx test reference (see Figure 110–3a). The test channel COM, calculated per 136.9.4.2.3 with the jitter-stressed transmitter output, shall not be lower than the value in Table 136–15.

A PHY shall meet the FEC symbol error ratio requirement defined in Table 136–15 for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 120D–7 with jitter added to all lanes (see 136.9.4.2.4).

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NOTE 1—If jitter is applied to each of the n lanes one at a time, results of the n measurements are summed to yield the FEC symbol error ratio. The result may need to be corrected based on the FEC symbol error ratio with no jitter applied on any lane.

NOTE 2—The A_{DD} (Equation (136–8)) and σ_{RJ} (Equation (136–9)) calculated from transmitter measurements in this test may be higher than the values in Table 136–18. A suitable channel should be chosen in order to meet the COM requirement with these values.

136.9.4.4 Signaling rate range

A PHY shall comply with the receiver requirements of 136.9.4.2 and 136.9.4.3 for any signaling rate in the range 26.5625 GBd ± 100 ppm. This translates to a nominal unit interval of 37.64706 ps.

136.9.4.5 Receiver ERL

ERL of the receiver at TP3 is computed using the procedure in 93A.5 with the values in Table 136–13. Parameters that do not appear in Table 136–13 take values from Table 136–18. The value of T_{fx} is twice the delay associated with the TP3 test fixture being used. N_{bx} is set to the value of N_b in Table 136–18.

Receiver ERL at TP3 shall be greater than or equal to 10 dB.

136.10 Channel characteristics

The channel is defined between TP0 and TP5 to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly as illustrated in Figure 136–2. The channel insertion loss, return loss, COM, and the transmitter and receiver differential controlled impedance printed circuit board parameters are provided informatively in 136A.4 through 136A.7.

Channel definitions apply for links between two PHYs of the same type, 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4.

136.11 Cable assembly characteristics

Cable assemblies defined in this subclause contain insulated conductors terminated in a connector at each end for use as link segments between MDIs. Cable assemblies are primarily intended as point-to-point links between 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4 PHYs using controlled impedance cables.

Three cable assembly types are specified:

a) 50GBASE-CR: Cable assembly that supports single-lane links between two 50GBASE-CR PHYs with achievable cable length of at least 3 m.

b) 100GBASE-CR2: Cable assembly that supports two-lane links between two 100GBASE-CR2 PHYs with achievable cable length of at least 3 m.

c) 200GBASE-CR4: Cable assembly that supports four-lane links between two 200GBASE-CR4 PHYs with achievable cable length of at least 3 m.

NOTE—It may be possible to construct compliant cable assemblies longer than indicated. Length of a cable assembly does not imply compliance to specifications.

50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 cable assembly form factors are described in Annex 136D. There are five possible MDIs which are defined in Annex 136C.

For 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4, the lanes are AC-coupled. The AC-coupling shall be within the cable assembly. It is recommended that it is within the plug connectors. It should be noted that there may be various methods for AC-coupling in actual implementations. The low-frequency 3 dB

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cutoff of the AC-coupling shall be less than 50 kHz. It is recommended that the value of the coupling capacitors be 100 nF. The capacitor limits the inrush charge and baseline wander.

All cable assembly measurements are to be made between TP1 and TP4 with cable assembly test fixtures as specified in Annex 136B. These cable assembly specifications are based upon twinaxial cable characteristics, but other cable types are acceptable if the specifications of this subclause are met.

Table 136–16 provides a summary of the cable assembly characteristics for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4, and references to the subclauses addressing each parameter.

The specifications for the three cable assembly types are identical except the number of lanes.

Table 136–16—Cable assembly characteristics summary

Description	Reference	Value	Unit
Maximum insertion loss at 13.28 GHz	136.11.2	17.16	dB
Minimum insertion loss at 13.28 GHz	136.11.2	8	dB
Minimum cable assembly ERL[a]	136.11.3	11	dB
Differential to common-mode return loss	136.11.4	Equation (92–28)	dB
Differential to common-mode conversion loss	136.11.5	Equation (92–29)	dB
Common-mode to common-mode return loss	136.11.6	Equation (92–30)	dB
Minimum COM	136.11.7	3	dB

[a]Cable assemblies with a COM greater than 4 dB are not required to meet minimum ERL.

136.11.1 Characteristic impedance and reference impedance

The nominal differential characteristic impedance of the cable assembly is 100 Ω. The differential reference impedance for cable assembly specifications shall be 100 Ω.

136.11.2 Cable assembly insertion loss

The measured insertion loss of a cable assembly shall be greater than or equal to the minimum cable assembly insertion loss given in Equation (92–26) and illustrated in Figure 92–12.

The measured insertion loss at 13.28 GHz of a cable assembly shall be less than or equal to 17.16 dB.

136.11.3 Cable assembly ERL

ERL of the cable assembly at TP1 and at TP4 are computed using the procedure in 93A.5 with the values in Table 136–17. Parameters that do not appear in Table 136–17 take values from Table 136–18. The value of T_{fx} is twice the delay associated with the specific cable assembly test fixture being used. Note that test fixtures are specified in 136B.1. N_{bx} is set to the value of N_b in Table 136–18.

Cable assembly ERL at TP1 and at TP4 shall be greater than or equal to 11 dB for cable assemblies that have a COM less than 4 dB.

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Table 136–17—Cable assembly ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.0189	ns
Incremental available signal loss factor	β_x	1.7	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.25	—
Length of the reflection signal	N	1000	UI

136.11.4 Differential to common-mode return loss

The cable assembly differential to common-mode return loss shall meet the requirements of 92.10.4.

136.11.5 Differential to common-mode conversion loss

The cable assembly differential to common-mode conversion loss shall meet the requirements of 92.10.5.

136.11.6 Common-mode to common-mode return loss

The cable assembly common-mode to common-mode return loss shall meet the requirements of 92.10.6.

136.11.7 Cable assembly Channel Operating Margin

The cable assembly Channel Operating Margin (COM) for each lane is derived from measurements of the cable assembly signal, near-end crosstalk and far-end crosstalk paths. COM is computed using the path calculations defined in 136.11.7.1 and the procedure in 93A.1, where T_r is 12 ps for $H_t(f)$ as used in Equation (93A–19). The specific paths used depend on cable assembly form factor (see Annex 136D), as described in 136.11.7.2.

COM parameter values for the three cable assembly types are provided in Table 136–18.

Test 1 and Test 2 differ in the value of the device package model transmission line length z_p. COM for any channel within the cable assembly shall be greater than or equal to 3 dB for both Test 1 and Test 2.

Table 136–18—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	26.5625	GBd
Maximum start frequency	$f_{\min}$	0.05	GHz
Maximum frequency step[a]	Δf	0.01	GHz
Device package model			
Single-ended device capacitance	C_d	1.8×10^{-4}	nF
Transmission line length, Test 1	z_p	12	mm
Transmission line length, Test 2	z_p	30	mm
Single-ended package capacitance at package-to-board interface	C_p	1.1×10^{-4}	nF
Package transmission line characteristic impedance	Z_c	95	Ω
Single-ended reference resistance	R_0	50	Ω

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Table 136–18—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.6	—
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.25 0 0.05	—
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.1 0.025	—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –20 0 1	 dB dB dB
Continuous time filter, DC gain 2 Minimum value Maximum value Step size	g_{DC2}	 –6 0 1	 dB dB dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	f_b / 2.5	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b / 2.5 $2 \times f_b$	GHz GHz
Continuous time filter, low-frequency pole/zero	f_{LF}	f_b / 40	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.415 0.415 0.604	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	12	UI
Normalized DFE coefficient magnitude limit for $n = 1$ for $n = 2$ to N_b	$b_{max}(n)$	 0.7 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI

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Table 136–18—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	1.64×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-4}	—

[a]For cable lengths greater than 4 m, a frequency step (Δf) no larger than 5 MHz is recommended.

136.11.7.1 Channel signal and crosstalk path calculations

The channel paths between TP0 and TP5 used for calculation of the cable assembly COM consist of measured cable assembly signal and crosstalk paths, representative transmitter PCB signal paths, and representative receiver PCB signal paths.

The transmitter and receiver PCB signal paths are calculated using the method defined in 93A.1.2.3. The scattering parameters for a PCB are defined by Equation (93A–13), Equation (93A–14), and the parameter values given in Table 92–12, with the exception that Z_c is 100 Ω. The PCB trace length parameter z_p has different value for each specific signal path, as specified in 136.11.7.1.1 and 136.11.7.1.2.

The channel path calculations use the function cascade() defined in 93A.1.2.1.

136.11.7.1.1 Channel signal path

The scattering parameters of the channel signal path from TP0 to TP5 are calculated using Equation (136–10). The transmitter and receiver PCB signal paths are both denoted as $S^{(HOSP)}$ and are calculated from Equation (93A–13) and Equation (93A–14) using z_p = 151 mm in length and the parameter values given in Table 92–12, with the exception that Z_c is 100 Ω, representing an insertion loss of 6.42 dB at 13.28 GHz on each PCB.

$$SCHS_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOSP)}, S^{(CASP)}), S^{(HOSP)}) \quad (136\text{–}10)$$

where

$SCHS_p^{(k)}$ is the channel signal path

$S^{(HOSP)}$ is the host (transmitter or receiver) PCB signal path

$S^{(CASP)}$ is the cable assembly signal path (TP1 to TP4)

k is equal to zero

136.11.7.1.2 Channel crosstalk paths

The MDI is the significant contributor to crosstalk and is included in and characterized by the cable assembly crosstalk measurements. Crosstalk includes a near-end path where the aggressor is the PMD transmitter, and in some cases, additional near-end, far-end, and alien far-end crosstalk paths where the aggressors are other PMD transmitters that are connected to the same cable assembly.

For the channel crosstalk paths, the receiver PCB model is $S^{(HOSP)}$ as defined in 136.11.7.1.1. The aggressor transmitter host PCB model is denoted as $S^{(HOTxSP)}$ and is calculated from Equation (93A–13) and Equation (93A–14) using z_p = 110 mm in length and the parameter values given in Table 92–12, with the exception that Z_c is 100 Ω, representing an insertion loss of 4.68 dB at 13.28 GHz. The transmitter host PCB

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insertion loss is lower than that used for the signal path, to allow for a reasonable worst-case crosstalk in the COM calculation.

The scattering parameters of the channel near-end crosstalk paths are calculated using Equation (136–11). The scattering parameters of the channel alien far-end crosstalk paths are calculated using Equation (136–12).

$$SCHNXT_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOTxSP)}, S^{(CANXTk)}), S^{(HOSP)}) \quad (136–11)$$

where

$SCHNXT_p^{(k)}$ is the near-end crosstalk path

$S^{(HOSP)}$ is the host receiver PCB signal path defined in 136.11.7.1.1

$S^{(HOTxSP)}$ is the aggressor transmitter PCB signal path

$S^{(CANXTk)}$ is the cable assembly near-end crosstalk path k (TP1 to TP4)

k is the index of the near-end crosstalk path

$$SCHAFXT_p^{(k)} = \text{cascade}(\text{cascade}(S^{(HOTxSP)}, S^{(CAFXTk)}), S^{(HOSP)}) \quad (136–12)$$

where

$SCHAFXT_p^{(k)}$ is the alien far-end crosstalk path

$S^{(HOSP)}$ is the host receiver PCB signal path defined in 136.11.7.1.1

$S^{(HOTxSP)}$ is the aggressor transmitter PCB signal path

$S^{(CAFXTk)}$ is the cable assembly far-end crosstalk path k (TP1 to TP4)

k is the index of the alien far-end crosstalk path

136.11.7.2 Signal and crosstalk paths used in calculation of COM

Cable assemblies have several form factors, as described in Annex 136D. The choice of signal and crosstalk paths for calculation of COM is specific to each cable assembly form factor, as specified in Table 136–19.

The signal path is calculated using Equation (136–10).

The near-end crosstalk paths are calculated using Equation (136–11), with k values from 1 to n; where n is the number of near-end crosstalk paths given in Table 136–19 for the cable assembly form factor considered.

The far-end crosstalk paths are calculated using Equation (136–12), with k values from 1 to n; where n is the number of far-end crosstalk paths given in Table 136–19 for the cable assembly form factor considered.

Annex 136C specifies the MDIs for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4.

The specifications for the cable assembly types are identical except the number of lanes.

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The crosstalk paths for each MDI type are given in Table 136–19; the crosstalk paths are from the aggressors given in columns two through four to the victim given in the first column.

Table 136–19—Number of crosstalk paths used in COM

	SFP28		QSFP28 or microQSFP		QSFP-DD or OSFP	
	NEXT	**FEXT**	**NEXT**	**FEXT**	**NEXT**	**FEXT**
SFP28	1	0	1	3	1	7
QSFP28 or microQSFP	4	3	4	3	4	7
QSFP-DD or OSFP	8	7	8	7	8	7

136.12 MDI specifications

The MDI couples the PMD (specified in 136.8 and 136.9) to the cable assembly (specified in 136.11).

50GBASE-CR has five specified MDI connectors: SFP28, QSFP28, microQSFP, QSFP-DD, and OSFP.

100GBASE-CR2 and 200GBASE-CR4 have four specified MDI connectors: QSFP28, microQSFP, QSFP-DD, and OSFP.

Annex 136C specifies the MDIs for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4.

136.13 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 14.7.

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136.14 Protocol implementation conformance statement (PICS) proforma for Clause 136, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4[227]

136.14.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 136, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

136.14.2 Identification

136.14.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

136.14.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 136, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[227] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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136.14.3 Major capabilities/options

Item[a]	Feature	Subclause	Value/Comment	Status	Support
*CR	50GBASE-CR PMD	136.1	Can operate as a 50GBASE-CR PMD	O.1	Yes [ ] No [ ]
*CR2	100GBASE-CR2 PMD	136.1	Can operate as a 100GBASE-CR2 PMD	O.1	Yes [ ] No [ ]
*CR4	200GBASE-CR4 PMD	136.1	Can operate as a 200GBASE-CR4 PMD	O.1	Yes [ ] No [ ]
PMA50	50GBASE-R PMA	136.1	Device implements Clause 135 PMA for 50GBASE-R	CR:M	Yes [ ] N/A [ ]
PMA100	100GBASE-P PMA	136.1	Device implements Clause 135 PMA for 100GBASE-P	CR2:M	Yes [ ] N/A [ ]
PMA200	200GBASE-R PMA	136.1	Device implements Clause 120 PMA for 200GBASE-R	CR4:M	Yes [ ] N/A [ ]
*AUIPMD	50GAUI-n C2C, 100GAUI-n C2C, or 200GAUI-n C2C	136.1	Service interface of PMA adjacent to PMD is physically instantiated	O.2	Yes [ ] No [ ]
AUIFEC	LAUI-2 C2C or CAUI-n C2C	136.1	Service interface of PMA between PCS and RS-FEC is physically instantiated	!CR4:O.2	Yes [ ] No [ ] N/A [ ]
*nGMII	50GMII, CGMII or 200GMII and RS	136.1	Interface is implemented or functionally equivalent	O.2	Yes [ ] No [ ]
AN	Auto-negotiation	136.1	Device implements auto-negotiation	M	Yes [ ]
FEC50	50GBASE-R RS-FEC	136.1	Device implements Clause 134 RS-FEC	CR* !AUIPMD :M	Yes [ ] N/A [ ]
PCS50	50GBASE-R PCS	136.1	Device implements Clause 133 PCS	CR* nGMII:M	Yes [ ] N/A [ ]
FEC100	100GBASE-R RS-FEC	136.1	Device implements Clause 91 RS-FEC with RS(544,514)	CR2* !AUIPMD :M	Yes [ ] N/A [ ]
PCS100	100GBASE-R PCS	136.1	Device implements Clause 82 100GBASE-R PCS	CR2* nGMII:M	Yes [ ] N/A [ ]
PCS200	200GBASE-R PCS	136.1	Device implements Clause 119 200GBASE-R PCS	CR4* nGMII:M	Yes [ ] N/A [ ]
*EEE	EEE fast wake capability	136.1	Capability is supported	nGMII:O	Yes [ ] No [ ] N/A [ ]
PCSAN	PCS requirements for AN service interface	136.4	PCS supports service interface primitive AN_LINK.indication	nGMII:M	Yes [ ] N/A [ ]
DC	Delay constraints	136.5	Conforms to constraints	M	Yes [ ]
SC	Skew and Skew Variation constraints	136.6	Conforms to constraints	M	Yes [ ]

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Item[a]	Feature	Subclause	Value/Comment	Status	Support
*MD	MDIO capability	136.7	Device implements Clause 45 MDIO	O	Yes [ ] No [ ]
*QM	QUIET operating mode	136.8.2	Device supports QUIET operating mode	O	Yes [ ] No [ ]
*CBL	Cable assembly	136.11	Item marked with CBL are cable assembly specifications, these items are the only ones applicable to cable assemblies and are not applicable to PHYs.	O	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

136.14.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136.14.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PF1	Transmit function in DATA mode	136.8.2	Converts each symbol stream from the PMD service interface into an electrical signal as specified, and delivers it to the MDI	M	Yes [ ]
PF2	Transmit function in TRAINING mode	136.8.2	Converts each symbol stream generated by the PMD control function into an electrical signal as specified, and delivers it to the MDI	M	Yes [ ]
PF3	Transmit function in QUIET mode	136.8.2	Transmitter output is disabled.	QM:M	Yes [ ] N/A [ ]
PF4	Receive function	136.8.3	Converts each electrical signal from the MDI into a symbol stream as specified, and delivers it to the PMD service interface	M	Yes [ ]
PF5	Lane-by-lane signal detect	136.8.5	Set to one if training is disabled, otherwise set according to signal_detect	M	Yes [ ]
PF6	Global PMD transmit disable	136.8.6	Function is implemented as specified	O	Yes [ ] No [ ]
PF7	Lane-by-lane PMD transmit disable	136.8.7	Function is implemented as specified	O	Yes [ ] No [ ]
PF8	PMD fault	136.8.8	PMD_fault variable mapped to the fault bit as specified in 45.2.1.2.3	MD:M	Yes [ ] N/A [ ]
PF9	PMD transmit fault	136.8.9	Implemented, PMD_transmit_fault variable mapped to the Transmit fault bit as specified in 45.2.1.7.4	MD:O	Yes [ ] No [ ] N/A [ ]
PF10	PMD receive fault	136.8.10	Implemented, PMD_receive_fault variable mapped to the Transmit fault bit as specified in 45.2.1.7.5	MD:O	Yes [ ] No [ ] N/A [ ]

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136.14.4.2 PMD control function

Item	Feature	Subclause	Value/Comment	Status	Support
PC1	PMD control function	136.8.11	Implemented as specified, one instance for each lane, operating independently	M	Yes [ ]
PC2	Training pattern	136.8.11.1.3	Each lane implements four generator polynomials defined in Table 136–8	M	Yes [ ]
PC3	Training pattern	136.8.11.1.3	State set to the value of seed_*i* at the start of the training pattern	M	Yes [ ]
PC4	Control field structure	136.8.11.2	As shown in Table 136–9	M	Yes [ ]
PC5	Receiver frame lock bit	136.8.11.3.3	Initially set to zero, not set to 1 until local_tf_lock is true	M	Yes [ ]
PC6	Initial condition setting	136.8.11.4.1	When requested, set according to the request, with values per Table 136–12	M	Yes [ ]
PC7	Handshake timing	136.8.11.6	When the transmitted frame lock bit is 1, acknowledge requests within less than 2 ms	M	Yes [ ]
PC8	Transmit precoded data	136.8.11.7.5	PMD causes adjacent PMA to use or not use precoding on transmitted data according to modulation and precoding status bit	M	Yes [ ]
PC9	Receive precoded data	136.8.11.7.5	PMD informs adjacent PMA about precoding of received data according to modulation and precoding request bit	M	Yes [ ]

136.14.4.3 Transmitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Output voltage specifications	93.8.1.3	Per Table 136–11	M	Yes [ ]
TC2	ERL	136.9.3.4	Meets equation constraints	M	Yes [ ]
TC3	Common-mode to differential mode output return loss	92.8.3.3	Meets equation constraints	M	Yes [ ]
TC4	Common-mode to common-mode output return loss	92.8.3.4	Meets equation constraints	M	Yes [ ]
TC5	Steady-state voltage, v_f	136.9.3.1.2	Per Table 136–11	M	Yes [ ]
TC6	Linear fit pulse peak (min.)	136.9.3.1.2	Per Table 136–11	M	Yes [ ]
TC7	Level separation mismatch ratio	120D.3.1.2	Per Table 136–11	M	Yes [ ]
TC8	Absolute coefficient step size	136.9.3.1.4	Per Table 136–11	M	Yes [ ]
TC9	Absolute change in coefficients other than *c*(coef_sel)	136.9.3.1.4	Less than 0.005	M	Yes [ ]
TC10	Coefficient range	136.9.3.1.5	Per Table 136–11	M	Yes [ ]
TC11	Signal-to-noise-and-distortion ratio	120D.3.1.6	Per Table 136–11	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC12	Output jitter	120D.3.1.8	Per Table 136–11	M	Yes [ ]
TC13	Transmitter signaling rate	136.9.3	26.5625 GBd ± 100 ppm	M	Yes [ ]

136.14.4.4 Receiver specifications

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	ERL	136.9.4.5	Greater than or equal to 10 dB	M	Yes [ ]
RC2	Differential to common-mode return loss at TP3	92.8.3.4	Meets equation constrains	M	Yes [ ]
RC3	Input amplitude tolerance	136.9.4.1	Meets FEC symbol error ratio requirement under described conditions	M	Yes [ ]
RC4	Interference tolerance	136.9.4.2	PHY meets FEC symbol error ratio requirement in all tests defined in Table 136–15 with the specified test setup and procedure	M	Yes [ ]
RC5	Jitter tolerance	136.9.4.3	PHY meets FEC symbol error ratio requirement with the specified test setup and procedure	M	Yes [ ]
RC6	Signaling rate range	136.9.4.4	PHY complies with receiver requirements for signaling rate of 26.5625 GBd ± 100 ppm	M	Yes [ ]

136.14.4.5 Cable assembly specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CA1	Differential reference impedance	136.11.1	100 Ω	CBL:M	Yes [ ] N/A [ ]
CA2	Minimum insertion loss	136.11.2	Per Equation (92–26)	CBL:M	Yes [ ] N/A [ ]
CA3	Maximum insertion loss at 13.28 GHz	136.11.2	17.16 dB	CBL:M	Yes [ ] N/A [ ]
CA4	ERL	136.11.3	Greater than or equal to 11 dB for cable assemblies that have a COM less than 4 dB	CBL:M	Yes [ ] N/A [ ]
CA5	Differential to common-mode input and output return loss	92.10.4	Per Equation (92–28)	CBL:M	Yes [ ] N/A [ ]
CA6	Differential to common-mode conversion loss	92.10.5	Per Equation (92–29)	CBL:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
CA7	Common-mode to common-mode return loss	92.10.6	Per Equation (92–30)	CBL:M	Yes [ ] N/A [ ]
CA8	Cable assembly Channel Operating Margin (COM)	136.11.7	Greater than or equal to 3 dB for both Test 1 and Test 2, for all channels within the cable assembly	CBL:M	Yes [ ] N/A [ ]
CA9	AC-coupling	136.11	3 dB cutoff frequency less than 50 kHz	CBL:M	Yes [ ] N/A [ ]

136.14.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Environmental specifications	136.13	Conform to applicable requirements of 14.7	M	Yes [ ]

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137. Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4

137.1 Overview

This clause specifies the 50GBASE-KR PMD, the 100GBASE-KR2 PMD, the 200GBASE-KR4 PMD, and the baseband medium. The specifications for the three PMDs are similar, except for the number of lanes and associated parameters and the MDI.

When forming a complete Physical Layer, a PMD shall be connected as illustrated in Figure 137–1, to the appropriate sublayers (as specified in Table 137–1, Table 137–2, and Table 137–3), to the medium through the appropriate MDI, and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 137–1—Physical Layer clauses associated with the 50GBASE-KR PMD

Associated clause	50GBASE-KR
132—RS	Required
132—50GMII[a]	Optional
133—PCS for 50GBASE-R	Required
134—RS-FEC	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135D—50GAUI-2 C2C	Optional
135F—50GAUI-1 C2C	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The 50GMII is an optional interface. However, if the 50GMII is not implemented, a conforming implementation behaves functionally as though the RS and 50GMII were present.

For the 50GBASE-KR and 100GBASE-KR2 PHYs, in order to support the required frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are expected to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 10^{-10} after processing by the RS-FEC (Clause 134 or Clause 91) and the PCS (Clause 133 or Clause 82) if there are negligible errors due to other electrical interfaces (50GAUI-n or 100GAUI-n). If the PMD and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 10^{-10}.

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Table 137–2—Physical Layer clauses associated with the 100GBASE-KR2 PMD

Associated clause	100GBASE-KR2
80—RS	Required
80—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R	Optional[b]
83A—CAUI-10	Optional
83D—CAUI-4 C2C	Optional
135—PMA for 100GBASE-P	Required
135D—100GAUI-4 C2C	Optional
135F—100GAUI-2 C2C	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation behaves functionally as though the RS and CGMII were present.
[b]PMA for 100GBASE-R is required when either CAUI-10 or CAUI-4 is used.

Table 137–3—Physical Layer clauses associated with the 200GBASE-KR4 PMD

Associated clause	200GBASE-KR4
117—RS	Required
117—200GMII[a]	Optional
118—200GMII extender	Optional
119—PCS for 200GBASE-R	Required
120—PMA for 200GBASE-R	Required
120B—200GAUI-8 C2C	Optional
120D—200GAUI-4 C2C	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

[a]The 200GMII is an optional interface. However, if the 200GMII is not implemented, a conforming implementation behaves functionally as though the RS and 200GMII were present.

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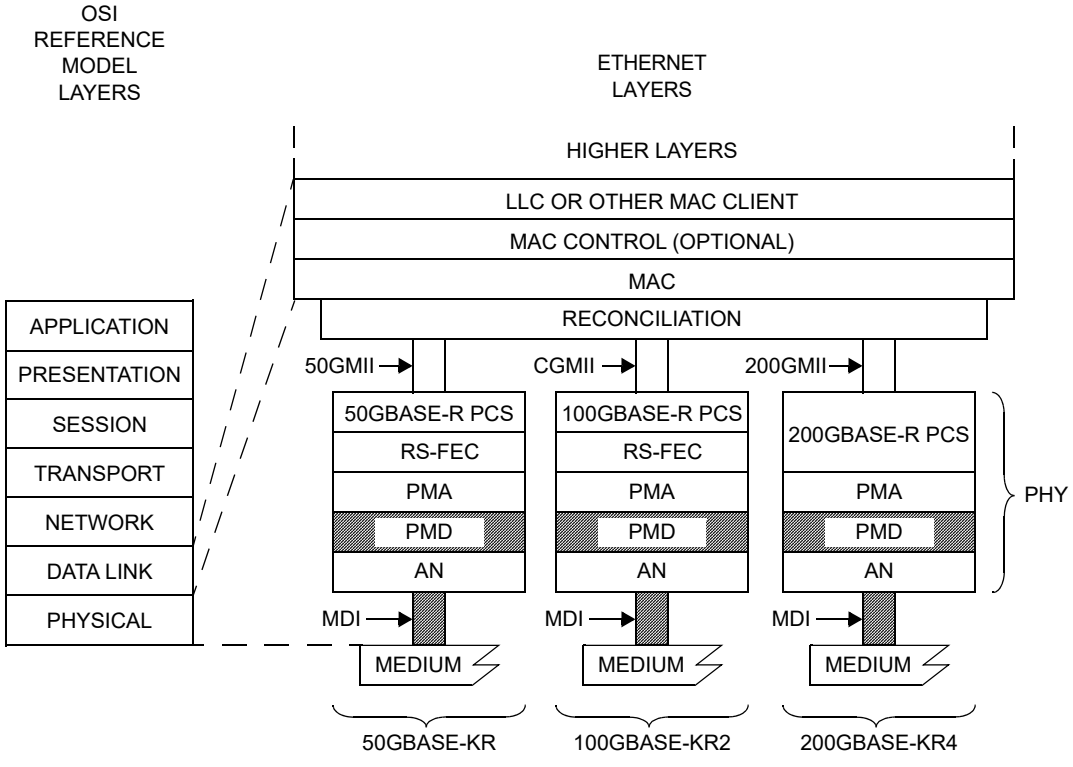
For the 200GBASE-KR4 PHY, in order to support the required frame loss ratio (see 1.4.344) of less than 6.2×10^{-11} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are expected to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 9.2×10^{-13} after processing by the PCS (Clause 119) if there are negligible errors due to other electrical interfaces (200GAUI-n). If the PMD and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 9.2×10^{-13}.

A compliant input signal is a transmitter output of a compliant PHY that has passed through a compliant channel.

50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Figure 137–1 shows the relationship of the PMD and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 137–1—50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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137.2 Conventions

Clause 137 describes three PMDs, 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4, which have one, two, and four lanes, respectively. For efficient description, the parameter n is used to describe the number of lanes in a specific PMD. Accordingly, n = 1 for 50GBASE-KR, n = 2 for 100GBASE-KR2, and n = 4 for 200GBASE-KR4.

The parameter *i* is used as an index or a suffix to identify a specific lane, and takes the values 0 to n – 1.

Within this clause, the unqualified term "PMD" refers to any of 50GBASE-KR PMD, 100GBASE-KR2 PMD, or 200GBASE-KR4 PMD.

137.3 PMD service interfaces

The service interfaces of the 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4 PMDs are identical to those of the 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4 PMDs, respectively (see 136.3).

137.4 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with the PMD is required to support the AN service interface primitive AN_LINK.indication defined in 73.9. The requirements are the same as those specified in 136.4.

137.5 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the PMD and AN including the medium in one direction shall be no more than the maximum delays listed in Table 137–4. It is assumed that the one-way delay through the medium is no more than 20 ns.

Table 137–4—Delay constraints

PMD	Maximum (bit times)[a]	Maximum (pause_quanta)[b]	Maximum (ns)
50GBASE-KR	2048	4	40.96
100GBASE-KR2	4096	8	40.96
200GBASE-KR4	8192	16	40.96

[a]One bit time is equal to 20 ps for 50GBASE-KR, 10 ps for 100GBASE-KR2, and 5 ps for 200GBASE-KR4. (See 1.4.215 for the definition of bit time.)
[b]One pause_quantum is equal to 10.24 ns for 50GBASE-KR, 5.12 ns for 100GBASE-KR2, and 2.56 ns for 200GBASE-KR4. (See 31B.2 for the definition of pause_quanta.)

Descriptions of overall system delay constraints can be found in 131.4 for 50GBASE-KR, in 80.4 for 100GBASE-KR2, and in 116.3 for 200GBASE-KR4.

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137.6 Skew constraints

The Skew (relative delay) between the PCS or FEC lanes is kept within limits so that the information on the PCS or FEC lanes can be reassembled by the PCS or FEC. The Skew Variation is also limited to ensure that a given PCS or FEC lane always traverses the same physical lane.

137.6.1 Skew Constraints for 50GBASE-KR

Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2.

137.6.2 Skew Constraints for 100GBASE-KR2 and 200GBASE-KR4

Skew and Skew Variation are defined in 80.5 and 116.5 and specified at the points SP1 to SP6 shown in Figure 80–9 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5 and 116.5.

137.7 PMD MDIO function mapping

The PMD MDIO function mapping requirements for the PMDs defined in this clause are identical to those of 136.7.

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137.8 PMD functional specifications

137.8.1 Link block diagram

One direction of a 50GBASE-KR, 100GBASE-KR2, or 200GBASE-KR4 link is shown in Figure 137–2.

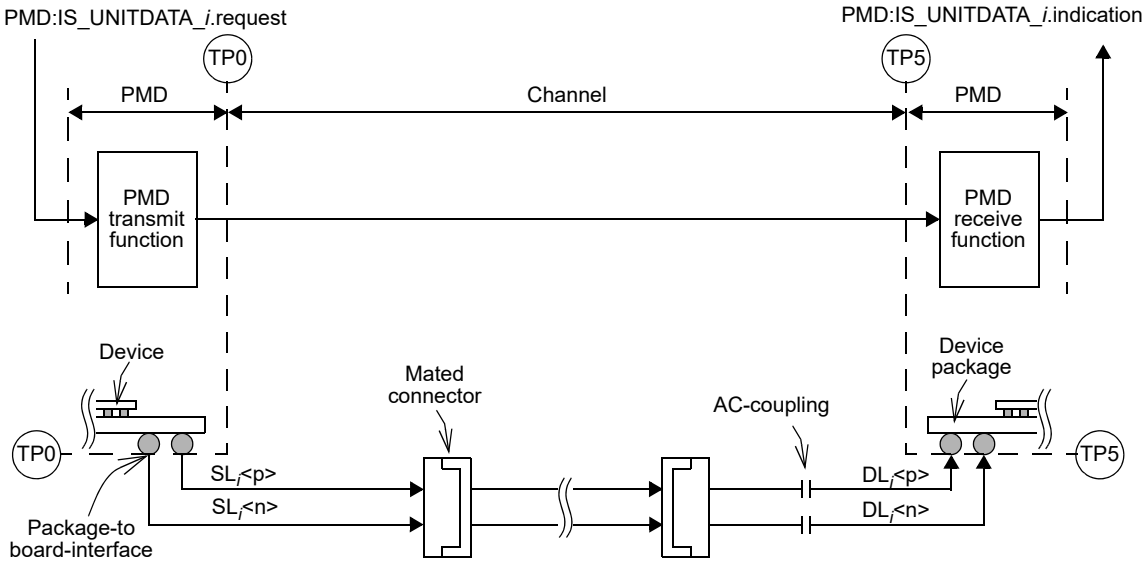

Figure 137–2—50GBASE-KR, 100GBASE-KR2 or 200GBASE-KR4 link (one direction for one lane is illustrated)

137.8.2 PMD transmit function

The PMD transmit function specification is identical to that of 136.8.2 with the exception that electrical signals are delivered to the MDI, according to the transmit electrical specifications in 137.9.2.

137.8.3 PMD receive function

The PMD receive function specification is identical to that of 136.8.3 with the exception that electrical signals are received from the MDI, according to the receive electrical specifications in 137.9.3.

137.8.4 PMD global signal detect function

The PMD global signal detect function specification is identical to that of 136.8.4.

137.8.5 PMD lane-by-lane signal detect function

The PMD lane-by-lane signal detect function specification is identical to that of 136.8.5.

137.8.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional. Its specification is identical to that of 136.8.6.

137.8.7 PMD lane-by-lane transmit disable function (optional)

The PMD lane-by-lane transmit disable function is optional. Its specification is identical to that of 136.8.7.

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137.8.8 PMD fault function

The PMD fault function specification is identical to that of 136.8.8.

137.8.9 PMD transmit fault function (optional)

The PMD transmit fault function is optional. Its specification is identical to that of 136.8.9.

137.8.10 PMD receive fault function (optional)

The PMD receive fault function is optional. Its specification is identical to that of 136.8.10.

137.8.11 PMD control function

The PMD control function specification is identical to that of 136.8.11.

137.9 Electrical characteristics

137.9.1 MDI

The MDI for the 50GBASE-KR, 100GBASE-KR2 and 200GBASE-KR4 PHYs is an implementation-dependent direct electrical connection between the PMD and the medium. The MDI comprises $2 \times n$ differential pairs, one pair for the transmit function and one pair for the receive function on each lane, marked by TP0 and TP5 in Figure 137–2.

Transmitter and receiver characteristics are defined at TP0a and TP5a.

The location of TP0a and the electrical characteristics of the test fixture used to measure transmitter characteristics are defined in Figure 93–5 and 93.8.1.1, respectively, with the exception that the upper frequency for Equation (93–1) and Equation (93–2) is 26.5625 GHz.

The location of TP5a and the electrical characteristics of the test fixture used to measure receiver characteristics are defined in Figure 93–10 and 93.8.2.1, respectively, with the exception that the upper frequency for Equation (93–1) and Equation (93–2) is 26.5625 GHz.

137.9.2 Transmitter characteristics

The transmitter shall meet the specifications given in Table 120D–1 with a measurement system as specified in 120D.3.1, with the following exceptions:

a) The value of linear fit pulse peak (min) is $0.75 \times v_f$. Linear fit pulse peak is measured with transmit equalization off (preset 1, see 136.9.3.1.3).
b) The output waveform Pre-cursor equalization and Post-cursor equalization parameters are replaced by the “Transmitter output waveform” specifications summarized in Table 136–11 and detailed in 136.9.3.1. The state of the transmit equalization may be manipulated and controlled by the PMD control function specified in 136.8.11, or by equivalent means.
c) The differential output return loss (min) and SNR_{ISI} (min) requirements are replaced by the transmitter effective return loss (ERL) specification in 137.9.2.1.
d) The value of SNDR (min) is 32.5 dB.
e) The J4u limit in Table 120D–1 does not apply. The maximum J3u (see 136.9.3.3) is 0.106 UI.

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137.9.2.1 Transmitter ERL

ERL of the transmitter at TP0a is computed using the procedure in 93A.5 with the values in Table 137–5. Parameters that do not appear in Table 137–5 take values from Table 137–6. The value of T_{fx} is twice the delay from TP0 to TP0a. N_{bx} is set to the value of N_b in Table 137–6.

Table 137–5—Transmitter and receiver ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.0189	ns
Incremental available signal loss factor	β_x	1.7	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.32	—
Length of the reflection signal	N	100	UI

Transmitter ERL at TP0a shall be greater than or equal to 15 dB.

137.9.3 Receiver characteristics

Receiver electrical characteristics are specified at TP5a. The receiver shall meet the specifications given in Table 120D–5 with the following exceptions:

a) PCS FEC symbol error ratio (max) values in Table 120D–6 and Table 120D–7 are all 10^{-3}. For 50GBASE-KR and 100GBASE-KR2, RS-FEC symbol error ratio is used instead of PCS FEC symbol error ratio.

b) Insertion loss at 13.2813 GHz values for Test 1 are 14.5 (min) and 15.5 (max).

c) Insertion loss at 13.2813 GHz values for Test 2 are 29.5 (min) and 30.5 (max).

d) RSS_DFE4 value for Test 1 is 0.05.

e) Receiver jitter tolerance (see 120D.3.2.2) is tested using the test channel used for receiver interference tolerance Test 2 (see item c).

f) The differential input return loss (min) requirements are replaced by the receiver ERL specification in 137.9.3.1.

137.9.3.1 Receiver ERL

ERL of the receiver at TP5a is computed using the procedure in 93A.5 with the values in Table 137–5. Parameters that do not appear in Table 137–5 take values from Table 137–6. The value of T_{fx} is twice the delay from TP5a to TP5. N_{bx} is set to the value of N_b in Table 137–6.

Receiver ERL at TP5a shall be greater than or equal to 15 dB.

137.10 Channel characteristics

The Channel Operating Margin (COM) is computed using the procedure in 93A.1 with the values in Table 137–6, where T_r is 12 ps for $H_t(f)$ as used in Equation (93A–19). COM shall be greater than or equal to 3 dB.

Channels shall have AC-coupling as specified in 93.9.4.

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Channels are recommended to meet the insertion loss limits in 137.10.1. Channels shall meet the ERL requirement in 137.10.2. The reference differential impedance for channel specifications is 100 Ω.

Table 137–6—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	26.5625	GBd
Maximum start frequency	$f_{\min}$	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface Package transmission line nominal characteristic impedance	 C_d z_p z_p C_p Z_c	 1.8×10^{-4} 12 30 1.1×10^{-4} 95	 nF mm mm nF Ω
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.6	—
Transmitter equalizer, 1st pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.25 0 0.05	—
Transmitter equalizer, 2nd pre-cursor coefficient Minimum value Maximum value Step size	$c(-2)$	 0 0.1 0.025	—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –20 0 1	 dB dB dB
Continuous time filter, DC gain 2 Minimum value Maximum value Step size	g_{DC2}	 –6 0 1	 dB dB dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	f_b / 2.5	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b / 2.5 $2 \times f_b$	GHz GHz
Continuous time filter, low-frequency pole/zero	f_{LF}	f_b / 40	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.415 0.415 0.604	 V V V

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Table 137–6—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	—
Transmitter signal-to-noise ratio	SNR_{TX}	32.5	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	12	UI
Normalized DFE coefficient magnitude limit $n = 1$ $n = 2$ to N_b	$b_{\max}(n)$	 0.7 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	1.64×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-4}	—

137.10.1 Channel insertion loss

The maximum recommended insertion loss of the channel is given by Equation (137–1).

$$IL(f) \le \left\{ \begin{array}{ll} 1.25 + 3.9\sqrt{f} + 1.095f & 0.01 \le f \le f_b/2 \\ -12.5 + 3.2f & f_b/2 < f \le f_b \end{array} \right\} \text{ (dB)} \qquad (137\text{–}1)$$

where

f is the frequency in GHz
f_b is the signaling rate (26.5625) in GHz
$IL(f)$ is the insertion loss at frequency f

The insertion loss limit is illustrated by Figure 137–3.

137.10.2 Channel ERL

ERL of the channel at TP0 and at TP5 are computed using the procedure in 93A.5 with the values in Table 137–7. Parameters that do not appear in Table 137–7 take values from Table 137–6. The value of T_{fx} is 0. N_{bx} is set to the value of N_b in Table 137–6.

Channel ERL at TP0 and at TP5 shall be greater than or equal to 10 dB.

137.11 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 93.10.

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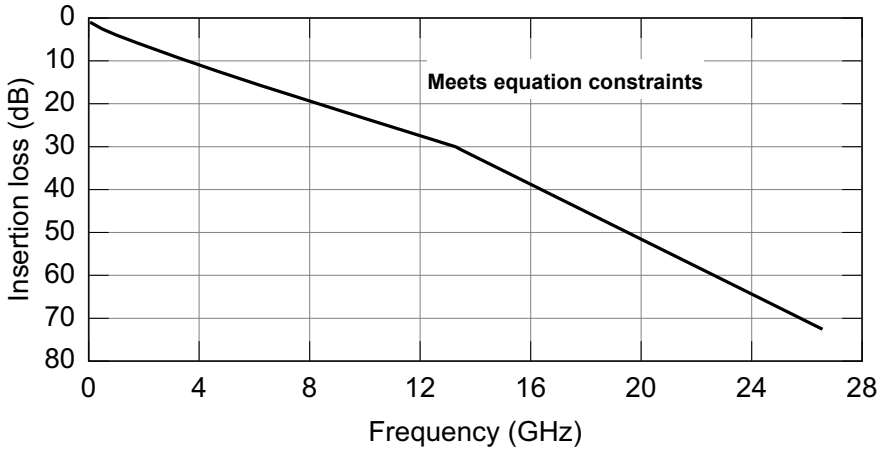

Figure 137–3—Channel insertion loss limit

Table 137–7—Channel ERL parameter values

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	0.0189	ns
Incremental available signal loss factor	β_x	1.7	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.18	—
Length of the reflection signal	N	1000	UI

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137.12 Protocol implementation conformance statement (PICS) proforma for Clause 137, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4[228]

137.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 137, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

137.12.2 Identification

137.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

137.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 137, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[228] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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137.12.3 Major capabilities/options

Item[a]	Feature	Subclause	Value/Comment	Status	Support
*KR	50GBASE-KR PMD	137.1	Can operate as a 50GBASE-KR PMD	O.1	Yes [ ] No [ ]
*KR2	100GBASE-KR2 PMD	137.1	Can operate as a 100GBASE-KR2 PMD	O.1	Yes [ ] No [ ]
*KR4	200GBASE-KR4 PMD	137.1	Can operate as a 200GBASE-KR4 PMD	O.1	Yes [ ] No [ ]
PMA50	50GBASE-R PMA	137.1	Device implements Clause 135 PMA for 50GBASE-R	KR:M	Yes [ ] N/A [ ]
PMA100	100GBASE-P PMA	137.1	Device implements Clause 135 PMA for 100GBASE-P	KR2:M	Yes [ ] N/A [ ]
PMA200	200GBASE-R PMA	137.1	Device implements Clause 120 PMA for 200GBASE-R	KR4:M	Yes [ ] N/A [ ]
*AUIPMD	50GAUI-n C2C, 100GAUI-n C2C, or 200GAUI-n C2C	137.1	Service interface of PMA adjacent to PMD is physically instantiated	O.2	Yes [ ] No [ ]
AUIFEC	LAUI-2 C2C or CAUI-n C2C	137.1	Service interface of PMA between PCS and RS-FEC is physically instantiated	!KR4:O.2	Yes [ ] No [ ] N/A [ ]
*nGMII	50GMII, CGMII or 200GMII and RS	137.1	Interface is implemented or functionally equivalent	O.2	Yes [ ] No [ ]
AN	Auto-negotiation	137.1	Device implements auto-negotiation	M	Yes [ ]
FEC50	50GBASE-R RS-FEC	137.1	Device implements Clause 134 RS-FEC	KR* !AUIPMD :M	Yes [ ] N/A [ ]
PCS50	50GBASE-R PCS	137.1	Device implements Clause 133 PCS	KR* nGMII:M	Yes [ ] N/A [ ]
FEC100	100GBASE-R RS-FEC	137.1	Device implements Clause 91 RS-FEC with RS(544,514)	KR2* !AUIPMD :M	Yes [ ] N/A [ ]
PCS100	100GBASE-R PCS	137.1	Device implements Clause 82 100GBASE-R PCS	KR2* nGMII:M	Yes [ ] N/A [ ]
PCS200	200GBASE-R PCS	137.1	Device implements Clause 119 200GBASE-R PCS	KR4* nGMII:M	Yes [ ] N/A [ ]
*EEE	EEE fast wake capability	137.1	Capability is supported	nGMII:O	Yes [ ] No [ ] N/A [ ]
PCSAN	PCS requirements for AN service interface	137.4	PCS supports service interface primitive AN_LINK.indication	nGMII:M	Yes [ ] N/A [ ]
DC	Delay constraints	137.5	Conforms to constraints	M	Yes [ ]
SC	Skew and Skew Variation constraints	137.6	Conforms to constraints	M	Yes [ ]

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Item[a]	Feature	Subclause	Value/Comment	Status	Support
*MD	MDIO capability	137.7	Device implements Clause 45 MDIO	O	Yes [ ] No [ ]
*CHNL	Channel	137.10	Item marked with CHNL are channel specifications, these items are the only ones applicable to channels and are not applicable to PHYs.	O	Yes [ ] No [ ]

[a]A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

137.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4

137.12.4.1 Functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PF1	Transmit function in DATA mode	136.8.2	Converts each symbol stream from the PMD service interface into an electrical signal as specified, and delivers it to the MDI, with the electrical specifications in 137.9.2	M	Yes [ ]
PF2	Transmit function in TRAINING mode	136.8.2	Converts each symbol stream generated by the PMD control function into an electrical signal as specified, and delivers it to the MDI, with the electrical specifications in 137.9.2	M	Yes [ ]
PF4	Receive function	136.8.3	Converts each electrical signal from the MDI into a symbol stream as specified, and delivers it to the PMD service interface	M	Yes [ ]
PF5	Lane-by-lane signal detect	136.8.5	Set to one if training is disabled, otherwise set according to signal_detect	M	Yes [ ]
PF6	Global PMD transmit disable	136.8.6	Function is implemented as specified	O	Yes [ ] No [ ]
PF7	Lane-by-lane PMD transmit disable	136.8.7	Function is implemented as specified	O	Yes [ ] No [ ]
PF8	PMD fault	136.8.8	PMD_fault variable mapped to the fault bit as specified in 45.2.1.2.3	MD:M	Yes [ ] N/A [ ]
PF9	PMD transmit fault	136.8.9	Implemented, PMD_transmit_fault variable mapped to the Transmit fault bit as specified in 45.2.1.7.4	MD:O	Yes [ ] No [ ] N/A [ ]
PF10	PMD receive fault	136.8.10	Implemented, PMD_receive_fault variable mapped to the Transmit fault bit as specified in 45.2.1.7.5	MD:O	Yes [ ] No [ ] N/A [ ]

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137.12.4.2 PMD control function

Item	Feature	Subclause	Value/Comment	Status	Support
PC1	PMD control function	136.8.11	Implemented as specified, one instance for each lane, operating independently	M	Yes [ ]
PC2	Training pattern	136.8.11.1.3	Each lane implements four generator polynomials defined in Table 136–8	M	Yes [ ]
PC3	Training pattern	136.8.11.1.3	State set to the value of seed_*i* at the start of the training pattern	M	Yes [ ]
PC4	Control field structure	136.8.11.2	As shown in Table 136–9	M	Yes [ ]
PC5	Receiver frame lock bit	136.8.11.3.3	Initially set to zero, not set to 1 until local_tf_lock is true	M	Yes [ ]
PC6	Initial condition setting	136.8.11.4.1	When requested, set according to the request, with values per Table 136–12	M	Yes [ ]
PC7	Handshake timing	136.8.11.6	When the transmitted frame lock bit is 1, acknowledge requests within less than 2 ms	M	Yes [ ]
PC8	Transmit precoded data	136.8.11.7.5	PMD causes adjacent PMA to use or not use precoding on transmitted data according to modulation and precoding status bit	M	Yes [ ]
PC9	Receive precoded data	136.8.11.7.5	PMD informs adjacent PMA about precoding of received data according to modulation and precoding request bit	M	Yes [ ]

137.12.4.3 Transmitter characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	TP0-TP0a test fixture	137.9.1	Meets specifications	M	Yes [ ]
TC2	Output voltage specifications	93.8.1.3	Per Table 120D–1	M	Yes [ ]
TC3	ERL at TP0a	137.9.2.1	Greater than or equal to 15 dB	M	Yes [ ]
TC4	Common-mode to common-mode output return loss	93.8.1.4	Per Table 120D–1	M	Yes [ ]
TC5	Steady-state voltage, v_f	120D.3.1.4	Per Table 120D–1	M	Yes [ ]
TC6	Linear fit pulse peak (min)	137.9.2	$0.75 \times v_f$	M	Yes [ ]
TC7	Level separation mismatch ratio	120D.3.1.2	Per Table 120D–1	M	Yes [ ]
TC8	Absolute coefficient step size	136.9.3.1.4	Per Table 136–11	M	Yes [ ]
TC9	Coefficient range	136.9.3.1.5	Per Table 136–11	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC10	Signal-to-noise-and-distortion ratio	137.9.2	Greater than specified minimum	M	Yes [ ]
TC11	Output jitter	120D.3.1.8	Per Table 136–11	M	Yes [ ]
TC12	Transmitter signaling rate	120D.3.1	26.5625 GBd ± 100 ppm	M	Yes [ ]

137.12.4.4 Receiver characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	TP5-TP5a test fixture	137.9.1	Meets specifications	M	Yes [ ]
RC2	ERL at TP5a	137.9.3.1	Greater than or equal to 15 dB	M	Yes [ ]
RC3	Input differential to common-mode return loss	137.9.3	Meets constraints of Equation (93–5)	M	Yes [ ]
RC4	Interference tolerance	137.9.3	PHY meets FEC symbol error ratio requirement in all tests defined in Table 120D–6 with the specified test setup and procedure, and the exceptions listed in 137.9.3	M	Yes [ ]
RC5	Jitter tolerance	137.9.3	PHY meets FEC symbol error ratio requirement in all cases defined in Table 120D–7 with the specified test setup and procedure, and the exceptions listed in 137.9.3	M	Yes [ ]

137.12.4.5 Channel characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	ERL	137.10.2	Greater than or equal to 10 dB	CHNL:M	Yes [ ] N/A [ ]
CC2	Channel Operating Margin (COM)	137.10	Greater than or equal to 3 dB	CHNL:M	Yes [ ] N/A [ ]
CC3	AC-coupling	93.9.4	Between TP0 and TP5, 3 dB cutoff frequency less than 50 kHz	CHNL:M	Yes [ ] N/A [ ]

137.12.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Environmental specifications	137.11	Conform to applicable requirements of 93.10	M	Yes [ ]

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138. Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, 400GBASE-SR8

138.1 Overview

This clause specifies the 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8 PMDs together with the multimode fiber medium. The optical signals generated by these PMD types are modulated using a 4-level pulse amplitude modulation (PAM4) format. The PMD sublayers provide point-to-point 50, 100, 200, and 400 Gigabit Ethernet links over one, two, four, or eight pairs of multimode fiber, with a reach of up to at least 100 m.

When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA, as shown in Table 138–1, Table 138–2, or Table 138–3, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 138–1—Physical Layer clauses associated with the 50GBASE-SR PMD

Associated clause	50GBASE-SR
132—RS	Required
132—50GMII[a]	Optional
133—PCS	Required
134—RS-FEC	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135C—LAUI-2 C2M	Optional
135D—50GAUI-2 C2C	Optional
135E—50GAUI-2 C2M	Optional
135F—50GAUI-1 C2C	Optional
135G—50GAUI-1 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a]The 50GMII is an optional interface. However, if the 50GMII is not implemented, a conforming implementation behaves functionally as though the RS and 50GMII were present.

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Table 138–2—Physical Layer clauses associated with the 100GBASE-SR2 PMD

Associated clause	100GBASE-SR2
80—RS	Required
80—CGMII[a]	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC[b]	Required
83—PMA for 100GBASE-R	Optional
83A—CAUI-10	Optional
83D—CAUI-4 C2C	Optional
83E—CAUI-4 C2M	Optional
135—PMA for 100GBASE-P	Required
135D—100GAUI-4 C2C	Optional
135E—100GAUI-4 C2M	Optional
135F—100GAUI-2 C2C	Optional
135G—100GAUI-2 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation behaves functionally as though the RS and CGMII were present.
[b]The option to bypass the Clause 91 RS-FEC correction function is not supported.

Table 138–3—Physical Layer clauses associated with the 200GBASE-SR4 and 400GBASE-SR8 PMDs

Associated clause	200GBASE-SR4	400GBASE-SR8
117—RS	Required	Required
117—200GMII[a]	Optional	Not applicable
117—400GMII[a]	Not applicable	Optional
118—200GMII Extender	Optional	Not applicable
118—400GMII Extender	Not applicable	Optional
119—PCS for 200GBASE-R	Required	Not applicable
119—PCS for 400GBASE-R	Not applicable	Required
120—PMA for 200GBASE-R	Required	Not applicable
120—PMA for 400GBASE-R	Not applicable	Required
120B—200GAUI-8 C2C	Optional	Not applicable
120B—400GAUI-16 C2C	Not applicable	Optional
120C—200GAUI-8 C2M	Optional	Not applicable
120C—400GAUI-16 C2M	Not applicable	Optional

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Table 138–3—Physical Layer clauses associated with the 200GBASE-SR4 and 400GBASE-SR8 PMDs *(continued)*

Associated clause	200GBASE-SR4	400GBASE-SR8
120D—200GAUI-4 C2C	Optional	Not applicable
120D—400GAUI-8 C2C	Not applicable	Optional
120E—200GAUI-4 C2M	Optional	Not applicable
120E—400GAUI-8 C2M	Not applicable	Optional
78—Energy-Efficient Ethernet	Optional	Optional

[a]The 200GMII and 400GMII are optional interfaces. However, if the appropriate interface is not implemented, a conforming implementation behaves functionally as though the RS and 200GMII or 400GMII were present.

Figure 138–1 shows the relationship of the PMDs and MDIs (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 50 Gigabit Ethernet is introduced in Clause 131 and the purpose of each PHY sublayer is summarized in 131.2. 100 Gigabit Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2. 200 Gigabit Ethernet and 400 Gigabit Ethernet are introduced in Clause 116 and the purpose of each PHY sublayer is summarized in 116.2.

50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Further relevant information may be found in Clause 1 (terminology and conventions, references, definitions and abbreviations) and Annex A (bibliography, referenced as [B1], [B2], etc.). The 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8 sublayers provide point-to-point 50, 100, 200, and 400 Gigabit Ethernet links over one, two, four, or eight pairs of multimode fiber, up to at least 100 m.

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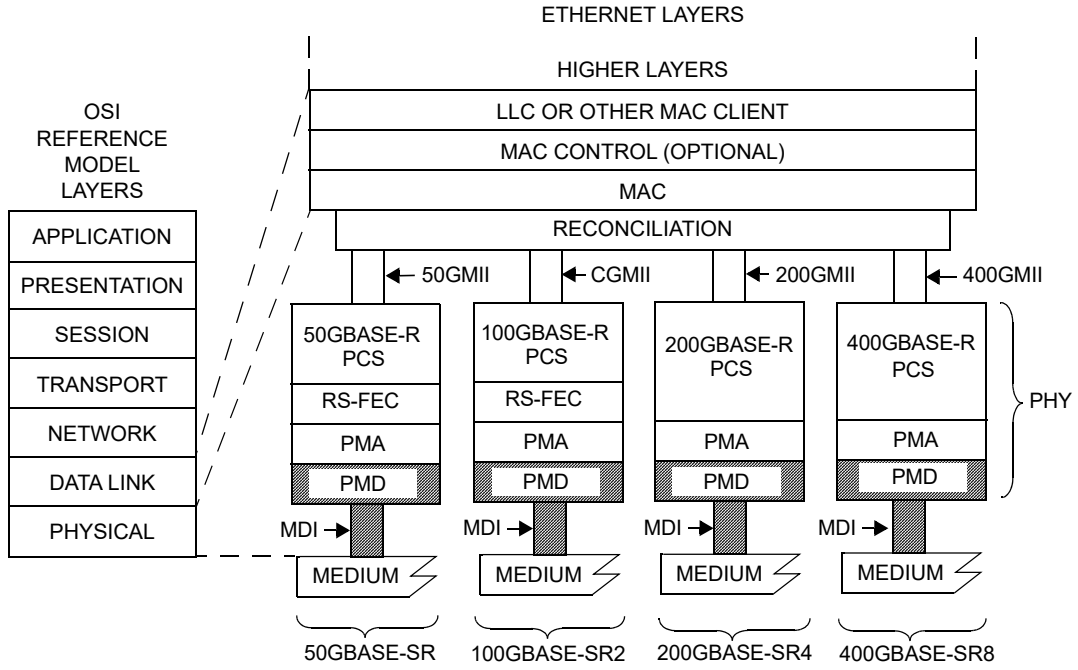

400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
SR = PMD FOR MULTIMODE FIBER

Figure 138–1—50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, 400GBASE-SR8 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

138.1.1 Bit error ratio

For the 50GBASE-SR and 100GBASE-SR2 PMDs, the bit error ratio (BER) when processed by the PMA (Clause 135) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap when additionally processed by the FEC (Clause 134 or Clause 91) and PCS (Clause 133 or Clause 82). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-10} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces. If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap.

For the 200GBASE-SR4 and 400GBASE-SR8 PMDs, the bit error ratio (BER) when processed by the PMA (Clause 120) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when additionally processed by the PCS (Clause 119). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces. If the error statistics are not sufficiently random to meet this

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requirement, then the BER shall be less than that required to give a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap.

138.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The 50GBASE-SR PMD service interface is an instance of the inter-sublayer service interface defined in 131.3, with a single symbol stream (n = 1).

The 100GBASE-SR2 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with two parallel symbol streams (n = 2).

The 200GBASE-SR4 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with four parallel symbol streams (n = 4).

The 400GBASE-SR8 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with eight parallel symbol streams (n = 8).

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 50GBASE-SR PMD has a single symbol stream, hence $i = 0$.

The 100GBASE-SR2 PMD has two parallel symbol streams, hence $i = 0$ to 1.

The 200GBASE-SR4 PMD has four parallel symbol streams, hence $i = 0$ to 3.

The 400GBASE-SR8 PMD has eight parallel symbol streams, hence $i = 0$ to 7.

In the transmit direction, the PMA continuously sends *n* streams of PAM4 symbols to the PMD, one per lane, using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 26.5625 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends *n* streams of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, one per lane, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 26.5625 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable SIGNAL_DETECT parameter as defined in 138.5.4. The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 138.1.1.

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138.3 Delay and Skew

138.3.1 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation.

The sum of the transmit and receive delays at one end of the link contributed by the 50GBASE-SR PMD including 2 m of fiber in one direction shall be no more than 1024 bit times (2 pause_quanta or 20.48 ns).

The sum of the transmit and receive delays at one end of the link contributed by the 100GBASE-SR2 PMD including 2 m of fiber in one direction shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns).

The sum of the transmit and receive delays at one end of the link contributed by the 200GBASE-SR4 PMD including 2 m of fiber in one direction shall be no more than 4096 bit times (8 pause_quanta or 20.48 ns).

The sum of the transmit and receive delays at one end of the link contributed by the 400GBASE-SR8 PMD including 2 m of fiber in one direction shall be no more than 8192 bit times (16 pause_quanta or 20.48 ns).

Descriptions of overall system delay constraints and the definitions for bit times and pause_quanta, can be found in 131.4 for 50GBASE-SR, in 80.4 for 100GBASE-SR2, and in 116.4 and its references for 200GBASE-SR4 and 400GBASE-SR8.

138.3.2 Skew constraints

The Skew (relative delay) between the PCS or FEC lanes is kept within limits so that the information on the PCS or FEC lanes can be reassembled by the PCS or FEC. The Skew Variation is also limited to ensure that a given PCS or FEC lane always traverses the same physical lane.

138.3.2.1 Skew Constraints for 50GBASE-SR

Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2 with the exception that the measurement clock and data recovery unit high-frequency corner bandwidth is 4 MHz.

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138.3.2.2 Skew Constraints for 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8

Skew and Skew Variation are defined in 80.5 and 116.5 and specified at the points SP1 to SP6 shown in Figure 80–9 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 80.5 and 116.5.

138.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 138–4, and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 138–5.

Table 138–4—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable *n*–1 to PMD transmit disable 0	PMD transmit disable register	1.9.*n* to 1.9.1	PMD_transmit_disable_*n*–1 to PMD_transmit_disable_0

Table 138–5—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect *n*–1 to PMD receive signal detect 0	PMD receive signal detect register	1.10.*n* to 1.10.1	PMD_signal_detect_*n*–1 to PMD_signal_detect_0

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138.5 PMD functional specifications

The 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8 PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

138.5.1 PMD block diagram

The PMD block diagram for 200GBASE-SR8 is shown in Figure 138–2. The block diagrams for 200GBASE-SR4, 100GBASE-SR2, and 50GBASE-SR are equivalent to Figure 138–2, but for four lanes, two lanes, and one lane per direction, respectively.

For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a multimode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 138.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 138.10.3). Unless specified otherwise, all receiver measurements and tests defined in 138.8 are made at TP3.

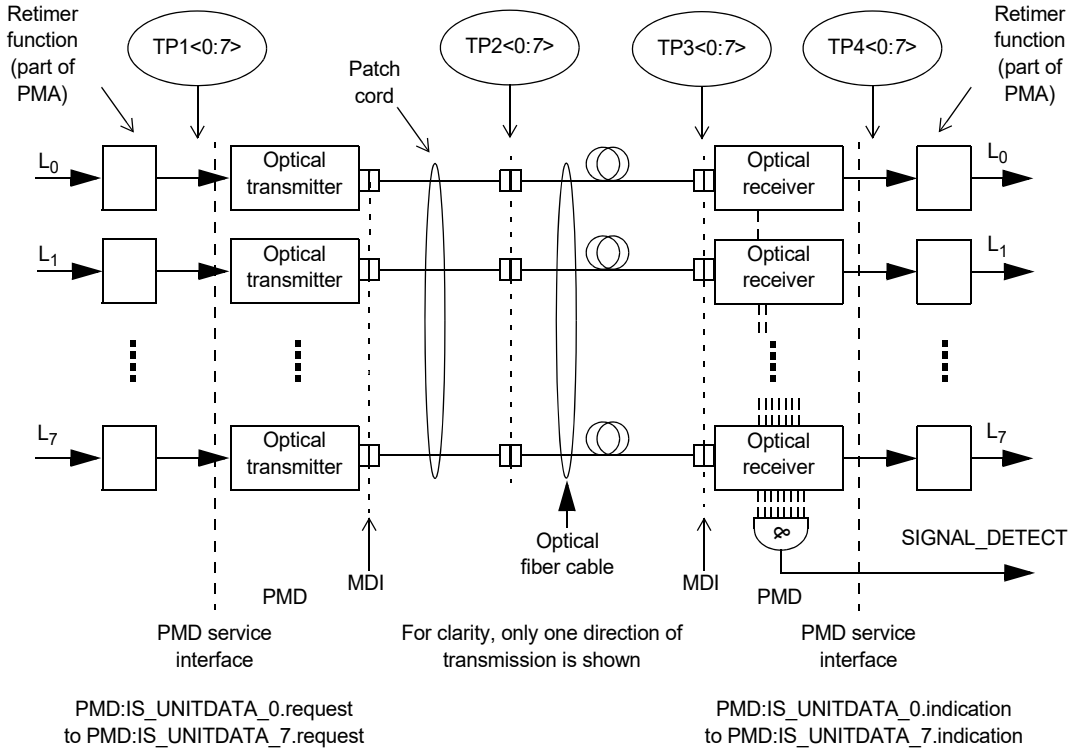

Figure 138–2—Block diagram for 400GBASE-SR8 transmit/receive paths

TP1<0:7> and TP4<0:7> are optional reference points that may be useful to implementers for testing components (these test points will not typically be accessible in an implemented system).

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138.5.2 PMD transmit function

The PMD Transmit function shall convert the one, two, four, or eight symbol streams requested by the PMD service interface messages PMD:IS_UNITDATA_*i*.request into one, two, four, or eight separate optical signals. The 50GBASE-SR PMD has a single symbol stream, hence $i = 0$. The 100GBASE-SR2 PMD has two parallel symbol streams, hence $i = 0$ to 1. The 200GBASE-SR4 PMD has four parallel symbol streams, hence $i = 0$ to 3. The 400GBASE-SR8 PMD has eight parallel symbol streams, hence $i = 0$ to 7. Each optical signal shall then be delivered to the MDI, which contains one, two, four, or eight parallel light paths for transmit, according to the transmit optical specifications in this clause. The four optical power levels in the signal in order from lowest to highest shall correspond to tx_symbol values zero, one, two, and three, respectively.

Editor's note (to be removed after D3.1): According to the resolution of comment I-19, the phrase "signal streams requested by the PMD service interface" was to be changed to "signals requested by the PMD service interface". However, the editor's understanding is that the change should be to "symbol streams requested by the PMD service interface" instead.

138.5.3 PMD receive function

The PMD Receive function shall convert the one, two, four, or eight parallel optical signals received from the MDI into separate symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_7.indication, all according to the receive optical specifications in this clause. The four optical power levels in each signal in order from lowest to highest shall correspond to rx_symbol values zero, one, two, and three, respectively.

138.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 80.3.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 138–6. The PMD receiver is not required to verify whether a compliant 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, or 400GBASE-SR8 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 138–6—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –30 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ average receive power, each lane (min) in Table 138–8) AND (compliant 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, or 400GBASE-SR8 signal input)]	OK
All other conditions	Unspecified

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As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

138.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:7, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 138–6.

138.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

138.5.7 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 138–8.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter in each lane.

138.5.8 PMD lane-by-lane transmit disable function (optional)

The PMD lane-by-lane transmit disable function is optional and allows the optical transmitter in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:7) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 138–8.

b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* to one, turning off the optical transmitter in each lane.

If the optional PMD lane-by-lane transmit disable function is not implemented in MDIO, an alternative method may be provided to independently disable each transmit lane.

138.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

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138.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set PMD_transmit_fault to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4

138.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

138.6 Lane assignments

There are no lane assignments (within a group of transmit or receive lanes) for 100GBASE-SR2, 200GBASE-SR4, or 400GBASE-SR8. While it is expected that a PMD will map electrical lane *i* to optical lane *i* and vice versa, there is no need to define the physical ordering of the lanes, as the RS-FEC or PCS sublayer is capable of receiving the lanes in any arrangement. The positioning of transmit and receive lanes at the MDI is specified in 138.10.3.1.

138.7 PMD to MDI optical specifications for 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8

The operating range for the 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8 PMDs is defined in Table 138–7. A compliant PMD operates on 50/125 μm multimode fibers, type A1a.2 (OM3), type A1a.3 (OM4), or type A1a.4 (OM5), according to the specifications defined in Table 138–14. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 50GBASE-SR PMD operating at 120 m meets the operating range requirement of 0.5 m to 100 m).

Table 138–7—Operating range

PMD type	Required operating range[a]
50GBASE-SR 100GBASE-SR2 200GBASE-SR4 400GBASE-SR8	0.5 m to 70 m for OM3
	0.5 m to 100 m for OM4
	0.5 m to 100 m for OM5

[a]The PCS FEC correction function may not be bypassed for any operating distance.

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138.7.1 Transmitter optical specifications

Each lane of a 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8 transmitter shall meet the specifications in Table 138–8 per the definitions in 138.8.

Table 138–8—Transmit characteristics

Description	Value	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm	GBd
Modulation format	PAM4	—
Center wavelength (range)	840 to 860	nm
RMS spectral width[a] (max)	0.6	nm
Average launch power, each lane (max)	4	dBm
Average launch power, each lane (min)	–6.5	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	3	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)[b]	–4.5	dBm
Launch power in OMA_{outer} minus TDECQ (min)	–5.9	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	4.5	dB
TDECQ – $10\log_{10}(C_{eq})$[c], each lane (max)	4.5	dB
Average launch power of OFF transmitter, each lane (max)	–30	dBm
Extinction ratio, each lane (min)	3	dB
Transmitter transition time, each lane (max)	34	ps
$RIN_{12}OMA$ (max)	–128	dB/Hz
Optical return loss tolerance (max)	12	dB
Encircled flux[d]	≥ 86% at 19 μm ≤ 30% at 4.5 μm	—

[a]RMS spectral width is the standard deviation of the spectrum.
[b]Even if the TDECQ < 1.4 dB, the OMA (min) has to exceed this value.
[c]C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[d]If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4:2009.

138.7.2 Receiver optical specifications

Each lane of a 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8 receiver shall meet the specifications in Table 138–9 per the definitions in 138.8.

Table 138–9—Receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm	GBd
Modulation format	PAM4	—
Center wavelength (range)	840 to 860	nm

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Table 138–9—Receive characteristics *(continued)*

Description	Value	Unit
Damage threshold[a] (min)	5	dBm
Average receive power, each lane (max)	4	dBm
Average receive power, each lane[b] (min)	–8.4	dBm
Receive power, each lane (OMA_{outer}) (max)	3	dBm
Receiver reflectance (max)	–12	dB
Stressed receiver sensitivity (OMA_{outer}), each lane[c] (max)	–3.4	dBm
Receiver sensitivity (OMA_{outer}), each lane[d] (max)	Equation (138–1)	dBm
Conditions of stressed receiver sensitivity test:[e]		
Stressed eye closure for PAM4 (SECQ), lane under test	4.5	dB
SECQ – $10\log_{10}(C_{eq})$[f] (max), lane under test	4.5	dB
OMA_{outer} of each aggressor lane[g]	3	dBm

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
[b]Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Measured with conformance test signal at TP3 (see 138.8.10) for the BER specified in 138.1.1.
[d]Receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 4.5 dB.
[e]These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f]C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[g]Only applies to 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8.

138.7.3 Illustrative link power budget

An illustrative power budget and penalties for 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8 channels are shown in Table 138–10.

Table 138–10—Illustrative link power budget

Parameter	OM3	OM4	OM5	Unit
Effective modal bandwidth at 850 nm[a]	2000	4700		MHz.km
Power budget (for max TDECQ)	6.5			dB
Operating distance	0.5 to 70	0.5 to 100		m
Channel insertion loss[b]	1.8	1.9		dB
Allocation for penalties[c] (for max TDECQ)	4.6			dB
Additional insertion loss allowed	0.1	0		dB

[a]Per IEC 60793-2-10.
[b]The channel insertion loss is calculated using the maximum distance specified in Table 138–7 and cabled optical fiber attenuation of 3.5 dB/km at 850 nm plus an allocation for connection and splice loss given in 138.10.2.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

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138.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

138.8.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 138–12 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 138–12 may be used to perform that test. The test patterns used in this clause are shown in Table 138–11.

Table 138–11—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle	119.2.4.9
6	SSPRQ	120.5.11.2.3

Table 138–12—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength, spectral width	3, 4, 5, 6, or valid 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, or 400GBASE-SR8 signal	138.8.2
Average optical power	3, 4, 5, 6, or valid 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, or 400GBASE-SR8 signal	138.8.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	138.8.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	138.8.5
Extinction ratio	4 or 6	138.8.6
Transmitter transition time	Square wave or 6	138.8.7
$RIN_{12}OMA$	Square wave	138.8.8
Stressed receiver sensitivity	3, 5, or valid 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, or 400GBASE-SR8 signal	138.8.10
Stressed eye closure (SEC), calibration	6	138.8.10

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138.8.1.1 Multi-lane testing considerations

Stressed receiver sensitivity is defined for each lane at the BER specified in 138.1.1. Measurements with Pattern 3 (PRBS31Q) allow lane-by-lane BER measurements. In stressed receiver sensitivity measurements, unstressed lanes may be created by setting the power at the receiver under test well above its sensitivity and/or not stressing those lanes with ISI and jitter, or by other means. Each receive lane is stressed in turn while all are operated. All aggressor lanes are operated as specified. Where relevant, parameters are defined with all co-propagating and counter-propagating lanes operational so that crosstalk effects are included. Where not otherwise specified, the maximum amplitude (OMA_{outer}) for a particular situation is used. Alternative test methods that generate equivalent results may be used. While the lanes in a particular direction may share a common clock, the Tx and Rx directions are not synchronous to each other. If Pattern 3 is used for the lanes not under test using a common clock, there is at least 31 UI delay between the PRBS31Q patterns on one lane and any other lane so that the symbols on each lane are not correlated within the PMD.

138.8.2 Center wavelength and spectral width

The center wavelength and RMS spectral width of each optical lane shall be within the range given in Table 138–8 if measured per IEC 61280-1-3. The lane under test is modulated using one of the test patterns specified in Table 138–12.

138.8.3 Average optical power

The average optical power of each lane shall be within the limits given in Table 138–8 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using one of the test patterns defined in Table 138–12.

138.8.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} of each lane shall be within the limits given in Table 138–8 if measured as defined in 121.8.4.

138.8.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

TDECQ is a measure of each optical transmitter's vertical eye closure as measured through an optical to electrical converter (O/E) with a bandwidth equivalent to a combined reference receiver and worst case optical channel, and equalized with the reference equalizer specified in 138.8.5.1. Table 138–9 specifies the test pattern to be used for measurement of TDECQ.

The TDECQ and TDECQ – $10\log_{10}(C_{eq})$ of each lane shall be within the limits given in Table 138–8 if measured using the methods specified in 121.8.5, with the following exceptions:

- The polarization rotator and test fiber shown in Figure 121–4 are not used.
- The optical channel requirements in 121.8.5.2 do not apply. For 400GBASE-SR8, the optical splitter and variable reflector are adjusted so that each transmitter is tested with an optical return loss equal to the "Optical return loss tolerance (max)" given in Table 138–8.
- The combination of the O/E converter and the oscilloscope used to measure the optical waveform has a 3 dB bandwidth of approximately 11.2 GHz with a fourth-order Bessel-Thomson response to at least 1.5×22.4 GHz and at frequencies above 1.5×22.4 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.
- The reference equalizer to be used for TDECQ for 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8 is specified in 138.8.5.1.

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138.8.5.1 TDECQ reference equalizer

The reference equalizer for 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8 is a 5-tap, T-spaced, feed-forward equalizer (FFE), where T is the symbol period. A functional model of the reference equalizer is shown in Figure 138–3. The sum of the equalizer tap coefficients is equal to 1. Tap 1, tap 2, or tap 3, has the largest magnitude tap coefficient, which is constrained to be at least 0.8.

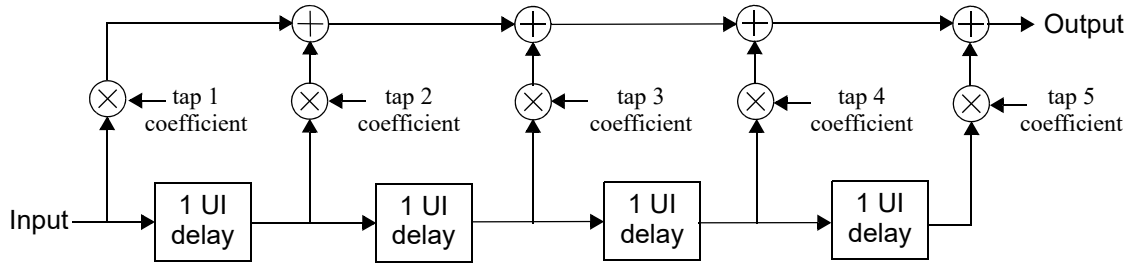

Figure 138–3—TDECQ reference equalizer functional model

NOTE—This reference equalizer is part of the TDECQ test and does not imply any particular receiver implementation.

138.8.6 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 138–8 if measured using the methods specified in 121.8.6.

138.8.7 Transmitter transition time

The transmitter transition time of each lane shall be within the limits given in Table 138–8 if measured using a test pattern specified for transmitter transition time in Table 138–12.

Transmitter transition time is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer}, or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling edges respectively, as measured through an O/E converter and oscilloscope with a combined 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz and at frequencies above 1.5 × 26.5625 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The 0% level and the 100% level are P_0 and P_3 as defined by the OMA_{outer} measurement procedure (see 138.8.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence and the falling edge is that within the 33333000000 symbol sequence.

138.8.8 Relative intensity noise ($RIN_{12}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 12 dB.
b) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 26.6 GHz).
c) The test pattern is according to Table 138–12.

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138.8.9 Receiver sensitivity

Receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 4.5 dB. Receiver sensitivity should meet Equation (138–1), which is illustrated in Figure 138–4.

$$RS = \max(-6.5, SECQ - 7.9) \quad \text{(dBm)} \tag{138–1}$$

where

RS is the receiver sensitivity

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

The normative requirement for receivers is stressed receiver sensitivity.

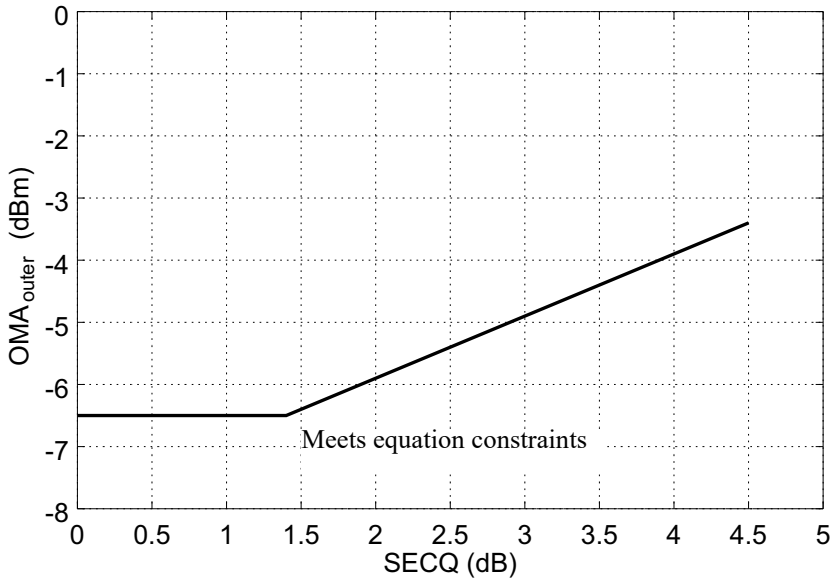

Figure 138–4—Illustration of receiver sensitivity

138.8.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 138–9 if measured using the methodology defined in 121.8.10.1 and 121.8.10.3, with the conformance test signal at TP3 as described in 121.8.5.2, with the following exceptions:

- The SECQ of the stressed receiver conformance test signal is measured according to 138.8.5, except that the combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz and at frequencies above 1.5 × 26.5625 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response. The optical splitter and variable reflector shown in Figure 121–4 are not used, and the transition time is no greater than the value specified in Table 138–8.
- With the Gaussian noise generator on and the sinusoidal jitter and sinusoidal interferer turned off, the $RIN_{12}OMA$ of the SRS test source should be no greater than the $RIN_{12}OMA$ (max) specified for the transmit characteristics in Table 138–8.
- The test patterns used for stressed receiver sensitivity are specified in Table 138–12.
- The signaling rate, the required stressed eye closure (SECQ), and the maximum $SECQ - 10\log_{10}(C_{eq})$ of the stressed receiver conformance test signal is as specified in Table 138–9.

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— The applied sinusoidal jitter is specified in 138.8.10.1.
— For 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8, the OMA_{outer} of the aggressor lanes is specified in Table 138–9.

The BER is required to be met for each lane under test on its own. Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Any of the patterns specified for stressed receiver sensitivity in Table 138–12 is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal.

138.8.10.1 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table 138–13.

Table 138–13—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter peak-to-peak (UI)
$f < 40$ kHz	Not specified
40 kHz $< f \leq 4$ MHz	2×10^5 Hz/f
4 MHz $< f \leq 10$ LB[a]	0.05

[a]LB = loop bandwidth; upper frequency bound for added sinusoidal jitter should be at least 10 times the loop bandwidth of the receiver being tested.

138.9 Safety, installation, environment, and labeling

138.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

138.9.2 Laser safety

50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8 optical transceivers shall conform to Hazard Level 1M laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[229]

[229]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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138.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

138.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, or 400GBASE-SR8 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate, in the literature associated with the PHY, the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

138.9.5 Electromagnetic emission

A system integrating a 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, or 400GBASE-SR8 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

138.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

138.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, or 400GBASE-SR8).

Labeling requirements for Hazard Level 1M lasers are given in the laser safety standards referenced in 138.9.2.

138.10 Fiber optic cabling model

The fiber optic cabling (channel) contains 1, 2, 4, or 8optical fibers for each direction to support 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, or 400GBASE-SR8, respectively. The fiber optic cabling interconnects the transmitters at the MDI on one end of the channel to the receivers at the MDI on the other end of the channel. As defined in 138.10.3, the optical lanes appear in defined locations at the MDI but the locations are not assigned specific lane numbers within this standard because any transmitter lane may be connected to any receiver lane.

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138.10.1 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 138–5.

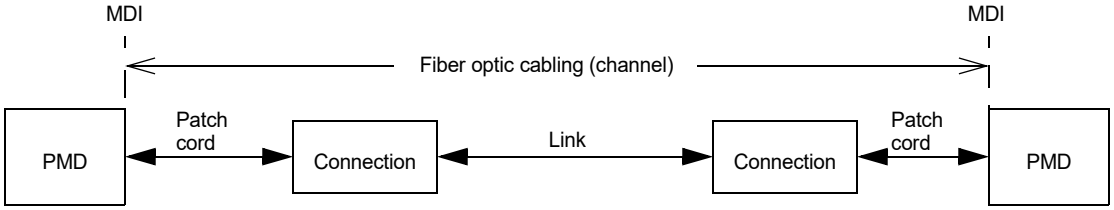

Figure 138–5—Fiber optic cabling model

The channel insertion loss is given in Table 138–14. A channel may contain additional connectors as long as the optical characteristics of the channel (such as attenuation, modal dispersion, reflections and losses of all connectors and splices) meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1 one-cord method. As OM4 and OM5 optical fiber meet the requirements for OM3, a channel compliant to the "OM3" column may use OM4 or OM5 optical fiber, or a combination of OM3, OM4, and OM5. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 138–14—Fiber optic cabling (channel) characteristics

Description	OM3	OM4	OM5	Unit
Operating distance (max)	70	100		m
Cabling Skew (max)[a]	79			ns
Cabling Skew Variation[ab] (max)	2.4			ns
Channel insertion loss[c] (max)	1.8	1.9		dB
Channel insertion loss (min)	0			dB

[a]Applies only to 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8.
[b]An additional 400 ps of Skew Variation could be caused by wavelength changes, which are attributable to the transmitter not the channel.
[c]These channel insertion loss values include cable loss plus 1.5 dB allocated for connection and splice loss, over the wavelength range 840 nm to 860 nm.

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138.10.2 Characteristics of the fiber optic cabling (channel)

The fiber optic cabling shall meet the specifications defined in Table 138–14. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

138.10.2.1 Optical fiber cable

The fiber contained within the fiber optic cabling shall comply with the specifications and parameters of Table 138–15. A variety of multimode cable types may satisfy these requirements, provided the resulting channel also meets the specifications of Table 138–14.

Table 138–15—Optical fiber and cable characteristics

Description	OM3[a]	OM4[b]	OM5[c]	Unit
Nominal core diameter	50			μm
Nominal fiber specification wavelength	850			nm
Effective modal bandwidth (min)[d]	2000	4700		MHz.km
Cabled optical fiber attenuation (max)	3.5			dB/km
Zero dispersion wavelength (λ_0)	$1295 \le \lambda_0 \le 1340$		$1297 \le \lambda_0 \le 1328$	nm
Chromatic dispersion slope (max) (S_0)	0.105 for $1295 \le \lambda_0 \le 1310$ and $0.000375 \times (1590 - \lambda_0)$ for $1310 \le \lambda_0 \le 1340$		$-412/(840(1 - (\lambda_0/840)^4))$	ps/nm^2 km

[a]IEC 60793-2-10 type A1a.2
[b]IEC 60793-2-10 type A1a.3
[c]IEC 60793-2-10 type A1a.4
[d]When measured with the launch conditions specified in Table 138–8

138.10.2.2 Optical fiber connection

An optical fiber connection, as shown in Figure 138–5, consists of a mated pair of optical connectors.

138.10.2.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an average insertion loss per connection of 0.5 dB. Connections with lower loss characteristics may be used provided the requirements of Table 138–14 are met. However, the loss of a single connection shall not exceed 0.75 dB.

138.10.2.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –20 dB.

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138.10.3 Medium Dependent Interface (MDI)

The 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, or 400GBASE-SR8 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 138–5). Examples of an MDI include the following:

a) PMD with a connectorized fiber pigtail plugged into an adapter;

b) PMD receptacle.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 138.5.1, not at the MDI.

138.10.3.1 Optical lane assignments for 100GBASE-SR2, 200GBASE-SR4, and 400GBASE-SR8

The two transmit and two receive optical lanes of 100GBASE-SR2 shall occupy the positions depicted in Figure 138–6 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains four active lanes within 12 total positions. The eight center positions are unused. The transmit optical lanes occupy the leftmost two positions. The receive optical lanes occupy the rightmost two positions.

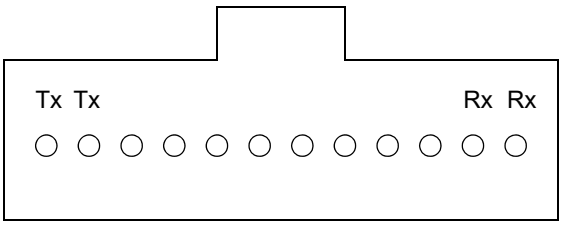

Figure 138–6—Optical lane assignments for 100GBASE-SR2

The four transmit and four receive optical lanes of 200GBASE-SR4 shall occupy the positions depicted in Figure 138–7 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains eight active lanes within 12 total positions. The four center positions are unused. The transmit optical lanes occupy the leftmost four positions. The receive optical lanes occupy the rightmost four positions.

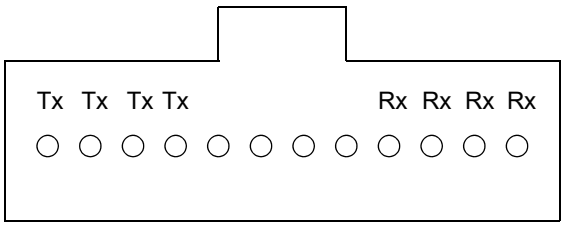

Figure 138–7—Optical lane assignments for 200GBASE-SR4

400GBASE-SR8 has two optical lane assignment options: Option A for a dual-row twelve-fiber interface, and option B for a single-row sixteen-fiber interface.

For a dual-row twelve-fiber interface, the eight transmit and eight receive optical lanes of 400GBASE-SR8 shall occupy the positions depicted in Figure 138–8 (option A) when looking into the MDI receptacle with the connector keyway feature on top. The interface contains sixteen active lanes within 24 total positions.

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The four center positions in each row are unused. The transmit optical lanes occupy the leftmost four positions in each row. The receive optical lanes occupy the rightmost four positions in each row.

For a single-row sixteen-fiber interface, the eight transmit and eight receive optical lanes of 400GBASE-SR8 shall occupy the positions depicted in Figure 138–8 (option B) when looking into the MDI receptacle with the connector keyway feature on top. The interface contains sixteen active lanes within sixteen total positions. The transmit optical lanes occupy the leftmost eight positions. The receive optical lanes occupy the rightmost eight positions.

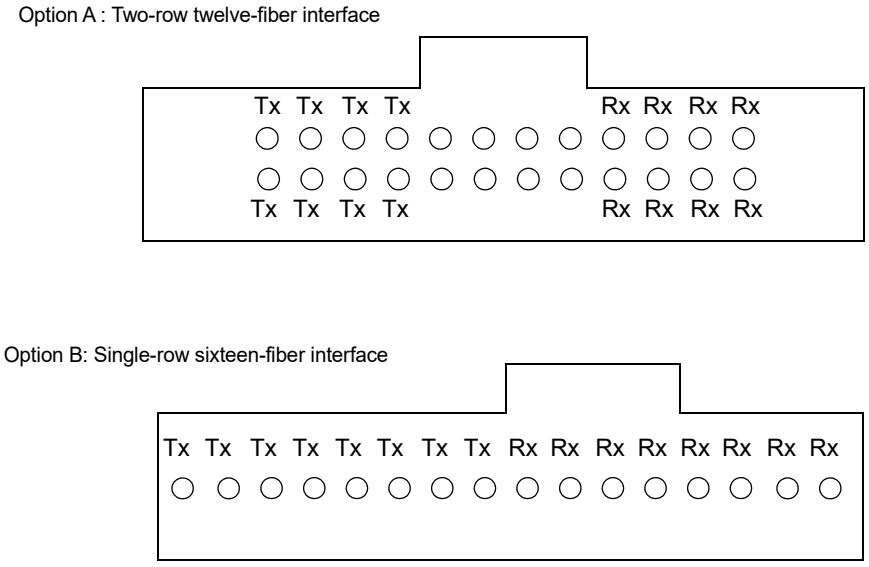

Figure 138–8—Optical lane assignments for 400GBASE-SR8

138.10.3.2 MDI requirements for 50GBASE-SR

The MDI shall optically mate with the compatible plug on the optical fiber cabling. For 50GBASE-SR, when the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2 for performance grade Bm/2m.

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138.10.3.3 MDI requirements for 100GBASE-SR2 and 200GBASE-SR4

The MDI shall optically mate with the compatible plug on the optical fiber cabling. For 100GBASE-SR2 and 200GBASE-SR4 the MDI adapter or receptacle shall meet the dimensional specifications for interface 7-1-3: *MPO adapter interface - opposed keyway configuration*, or interface 7-1-10: *MPO active device receptacle, flat interface*, as defined in IEC 61754-7-1. The plug terminating the optical fiber cabling shall meet the dimensional specifications of interface 7-1-4: *MPO female plug connector, flat interface for 2 to 12 fibers*, as defined in IEC 61754-7-1. Figure 138–9 shows an MPO female plug connector with flat interface, and an MDI. The MDI connection shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2 for performance grade Bm/2m.

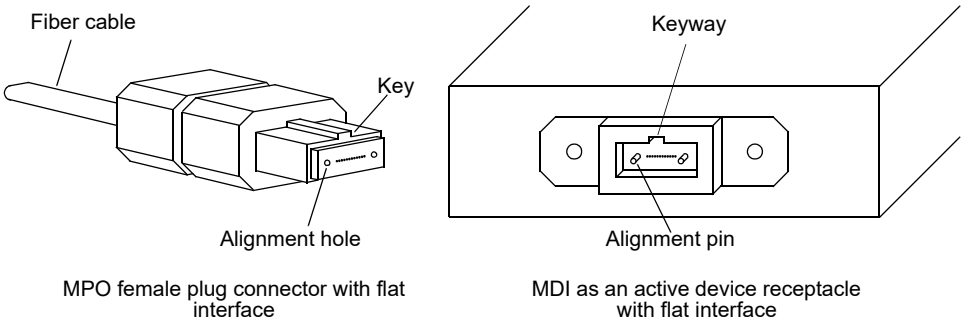

Figure 138–9—MPO female plug with flat interface and MDI active device receptacle with flat interface

138.10.3.4 MDI requirements for 400GBASE-SR8

The MDI shall optically mate with the compatible plug on the optical fiber cabling. The MDI connection shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2 for performance grade Bm/2m. 400GBASE-SR8 has two optical lane assignment options: Option A for a dual-row twelve-fiber interface, and option B for a single-row sixteen-fiber interface.

For Option A, the MDI adapter or receptacle shall meet the dimensional specifications for interface 7-2-3: *MPO adapter interface - opposed keyway* configuration, or interface 7-2-10: *MPO active device receptacle, flat interface*, as defined in IEC 61754-7-2. The plug terminating the optical fiber cabling shall meet the dimensional specifications of interface 7-2-4: *MPO female plug connector, flat interface for 16 to 24 fibers*, as defined in IEC 61754-7-2. The MPO female plug connector and MDI are structurally similar to those depicted in Figure 138–9, but with two rows of fibers.

For Option B, the MDI adapter or receptacle shall meet the dimensional specifications for designation FOCIS 18 A-1-0, or designation FOCIS 18 R-1x16-1-0-1-2-0, as defined in ANSI/TIA-604-18-A. The plug terminating the optical fiber cabling shall meet the dimensional specifications of designation FOCIS 18 P-1x16-1-0-2-2-0, as defined in ANSI/TIA-604-18-A. The MPO female plug connector and MDI are structurally similar to those depicted in Figure 138–9, but with sixteen fibers and an offset keyway as well as a different pin diameter and location.

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138.11 Protocol implementation conformance statement (PICS) proforma for Clause 138, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, 400GBASE-SR8[230]

138.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 138, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, 400GBASE-SR8, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

138.11.2 Identification

138.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

138.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 138, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, 400GBASE-SR8
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[230]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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138.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*SR	50GBASE-SR PMD	138.7	Device supports requirements for 50GBASE-SR PHY	O	Yes [ ] No [ ]
*SR2	100GBASE-SR2 PMD	138.7	Device supports requirements for 100GBASE-SR2 PHY	O	Yes [ ] No [ ]
*SR4	200GBASE-SR4 PMD	138.7	Device supports requirements for 200GBASE-SR4 PHY	O	Yes [ ] No [ ]
*SR8	400GBASE-SR8 PMD	138.7	Device supports requirements for 400GBASE-SR8 PHY	O	Yes [ ] No [ ]
*SR8A	400GBASE-SR8 MDI option A	138.10.3.4	Device has MDI with dual-row twelve-fiber interface	SR8:O.1	Yes [ ] No [ ]
*SR8B	400GBASE-SR8 MDI option B	138.10.3.4	Device has MDI with single-row sixteen-fiber interface	SR8:O.1	Yes [ ] No [ ]
*INS	Installation / cable	138.10.1	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	138.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	138.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	138.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	138.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	138.4	Registers and interface supported	O	Yes [ ] No [ ]

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138.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4, 400GBASE-SR8

138.11.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 50GBASE-R, 100GBASE-R, 200GBASE-R, or 400GBASE-R PCS and PMA	138.1		M	Yes [ ]
F2	Integration with management functions	138.1		O	Yes [ ] No [ ]
F3	Bit error ratio	138.1.1	Meets the BER specified in 138.1.1	M	Yes [ ]
F4	Transmit function	138.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
F5	Mapping between optical signal and logical signal for transmitter	138.5.2	Optical power levels from lowest to highest correspond to tx_symbol values zero, one, two, and three, respectively	M	Yes [ ]
F6	Receive function	138.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]
F7	Conversion of n optical signals to n electrical signals	138.5.3	For delivery to the PMD service interface	M	Yes [ ]
F8	Mapping between optical signal and logical signal for receiver	138.5.3	Optical power levels from lowest to highest correspond to rx_symbol values zero, one, two, and three, respectively	M	Yes [ ]
F9	Global Signal Detect function	138.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
F10	Global Signal Detect behavior	138.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all n lanes	M	Yes [ ]
F11	Lane-by-lane Signal Detect function	138.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 138–6	MD:O	Yes [ ] No [ ] N/A [ ]
F12	PMD reset function	138.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

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138.11.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	138.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	138.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD_lane_by_lane_transmit_disable function	138.5.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_*i* variable	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD lane-by-lane transmit disable	138.5.8	Disables each optical transmitter independently if M3 = No	!MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_fault function	138.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M6	PMD_transmit_fault function	138.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
M7	PMD_receive_fault function	138.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

138.11.4.3 PMD to MDI optical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Transmitter meets specifications in Table 138–8	138.7.1	Per definitions in 138.8	M	Yes [ ]
S2	Receiver meets specifications in Table 138–9	138.7.2	Per definitions in 138.8	M	Yes [ ]

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138.11.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	138.8	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and spectral width	138.8.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	138.8.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA_{outer} measurements	138.8.4	Each lane	M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	138.8.5	Each lane	M	Yes [ ]
OM6	Extinction ratio	138.8.6	Per IEC 61280-2-2	M	Yes [ ]
OM7	Transmitter transition time	138.8.7	Each lane	M	Yes [ ]
OM8	$RIN_{12}OMA$ measurement procedure	138.8.8	Each lane	M	Yes [ ]
OM9	Stressed receiver sensitivity	138.8.10	See 138.8.10	M	Yes [ ]

138.11.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	138.9.1	Conforms to J.2	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1M	138.9.2	Conforms to Hazard Level 1M laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	138.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

138.11.4.6 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	138.10	Meets requirements specified in Table 138–14	INS:M	Yes [ ] N/A [ ]
OC2	Optical fiber characteristics	138.10.1	Per Table 138–15	INS:M	Yes [ ] N/A [ ]
OC3	Maximum discrete reflectance	138.10.2.2	Less than –20 dB	INS:M	Yes [ ] N/A [ ]
OC4	MDI layout for 100GBASE-SR2	138.10.3.1	Optical lane assignments per Figure 138–6	SR2:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
OC5	MDI layout for 200GBASE-SR4	138.10.3.1	Optical lane assignments per Figure 138–7	SR4:M	Yes [ ] N/A [ ]
OC6	MDI layout for 400GBASE-SR8 option A	138.10.3.1	Optical lane assignments per Figure 138–8	SR8A:M	Yes [ ] N/A [ ]
OC7	MDI layout for 400GBASE-SR8 option B	138.10.3.1	Optical lane assignments per Figure 138–8	SR8B:M	Yes [ ] N/A [ ]
OC8	MDI mating, 50GBASE-SR	138.10.3.2	MDI optically mates with plug on the cabling, performance grade Bm/2m	SR:M	Yes [ ] N/A [ ]
OC9	MDI requirements for 50GBASE-SR	138.10.3.2	Per IEC 61753-1 and IEC 61753-022-2	INS:M	Yes [ ] N/A [ ]
OC10	MDI mating, 100GBASE-SR2 and 200GBASE-SR4	138.10.3.3	MDI optically mates with plug on the cabling	(SR2 or SR4):M	Yes [ ] N/A [ ]
OC11	MDI mating 400GBASE-SR8	138.10.3.4	MDI optically mates with plug on the cabling	SR8:M	Yes [ ] N/A [ ]
OC12	MDI dimensions for 100GBASE-SR2 and 200GBASE-SR4	138.10.3.3	Per IEC 61754-7-1 interface 7-1-3 or interface 7-1-10	(SR2 or SR4):M	Yes [ ] N/A [ ]
OC13	Cabling connector dimensions for 100GBASE-SR2 and 200GBASE-SR4	138.10.3.3	Per IEC 61754-7-1 interface 7-1-4	INS*(SR2 or SR4):M	Yes [ ] N/A [ ]
OC14	MDI dimensions for 400GBASE-SR8	138.10.3.4	Per IEC 61754-7-2 interfaces 7-2-3 or 7-2-10, or per ANSI/TIA-604-18-A designation FOCIS 18 A-1-0 or FOCIS 18 R-1x16-1-0-1-2-0	SR8:M	Yes [ ] N/A [ ]
OC15	Cabling connector dimensions for 400GBASE-SR8	138.10.3.4	Per IEC 61754-7-2 interface 7-2-4 or ANSI/TIA-604-18-A designation FOCIS 18 P-1x16-1-0-2-2-0	INS*SR8:M	Yes [ ] N/A [ ]
OC16	MDI requirements for 100GBASE-SR2 and 200GBASE-SR4	138.10.3.3	Per IEC 61753-1 and IEC 61753-022-2, performance grade Bm/2m	INS*(SR2 or SR4):M	Yes [ ] N/A [ ]
OC17	MDI requirements for 400GBASE-SR8	138.10.3.4	Per IEC 61753-1 and IEC 61753-022-2, performance grade Bm/2m	INS*SR8:M	Yes [ ] N/A [ ]

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139. Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER

139.1 Overview

This clause specifies the 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER PMDs together with the single-mode fiber medium. The optical signals generated by these three PMD types are modulated using a 4-level pulse amplitude modulation (PAM4) format. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 139–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 139–1—Physical Layer clauses associated with the 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER PMDs

Associated clause	50GBASE-FR, 50GBASE-LR, 50GBASE-ER
132—RS	Required
132—50GMII[a]	Optional
133—PCS for 50GBASE-R	Required
134—RS-FEC for 50GBASE-R	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135C—LAUI-2 C2M	Optional
135D—50GAUI-2 C2C	Optional
135E—50GAUI-2 C2M	Optional
135F—50GAUI-1 C2C	Optional
135G—50GAUI-1 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a]50GMII is an optional interface. However, if the appropriate interface is not implemented, a conforming implementation behaves functionally as though the RS and 50GMII were present.

Figure 139–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 50 Gigabit Ethernet is introduced in Clause 131 and the purpose of each PHY sublayer is summarized in 131.2.

50GBASE-FR, 50GBASE-LR, and 50GBASE-ER PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

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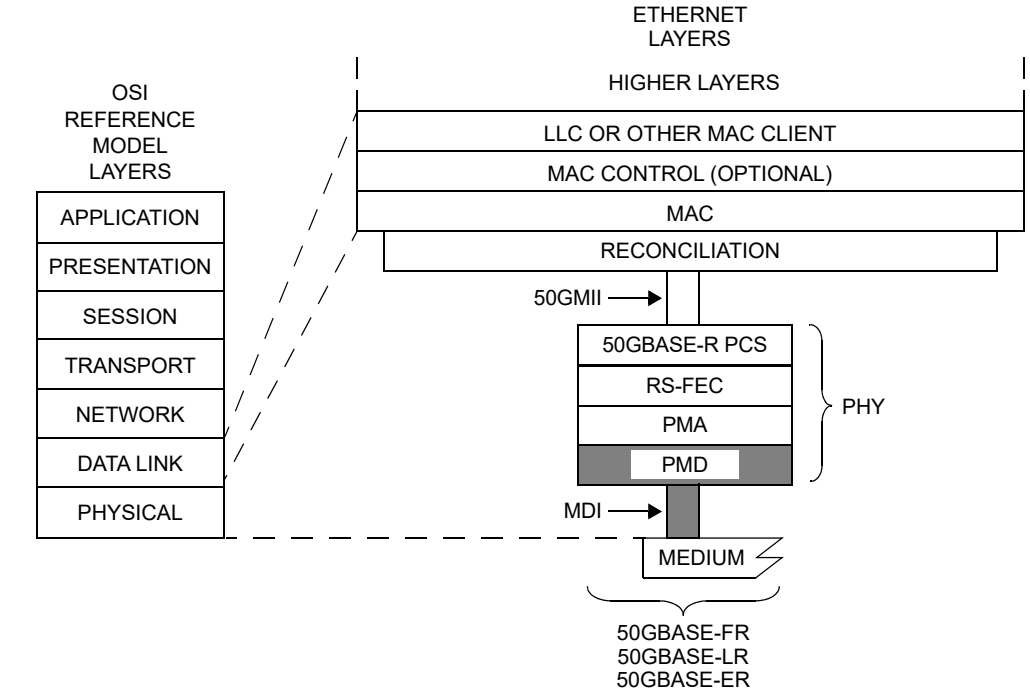

Figure 139–1—50GBASE-FR, 50GBASE-LR, and 50GBASE-ER PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

139.1.1 Bit error ratio

The bit error ratio (BER) when processed by the PMA (Clause 135) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap when additionally processed by the FEC (Clause 134) and PCS (Clause 133). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-10} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap.

139.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER PMDs. The service interface for these PMDs is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the

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PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER PMD service interface is an instance of the inter-sublayer service interface defined in 131.3, with a single symbol stream (n = 1).

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_0.request
PMD:IS_UNITDATA_0.indication
PMD:IS_SIGNAL.indication

In the transmit direction, the PMA continuously sends one stream of PAM4 symbols to the PMD using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 26.5625 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends one stream of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 26.5625 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable SIGNAL_DETECT parameter as defined in 139.5.4. The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 139.1.1.

139.3 Delay and Skew

139.3.1 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation. The sum of the transmit and receive delays at one end of the link contributed by the 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER PMDs including 2 m of fiber in one direction shall be no more than 1024 bit times (2 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quantum can be found in 131.4 and its references.

139.3.2 Skew constraints

The Skew (relative delay) between the FEC lanes is kept within limits so that the information on the lanes can be reassembled by the FEC. The Skew Variation is also limited to ensure that a given FEC lane always traverses the same physical lane. Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

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If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2 with the exception that the measurement clock and data recovery unit high-frequency corner bandwidth is 4 MHz.

139.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 139–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 139–3.

Table 139–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable

Table 139–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect

139.5 PMD functional specifications

The 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

139.5.1 PMD block diagram

The PMD block diagram is shown in Figure 139–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 139.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 139.10.3). Unless specified otherwise, all receiver measurements and tests defined in 139.7 are made at TP3.

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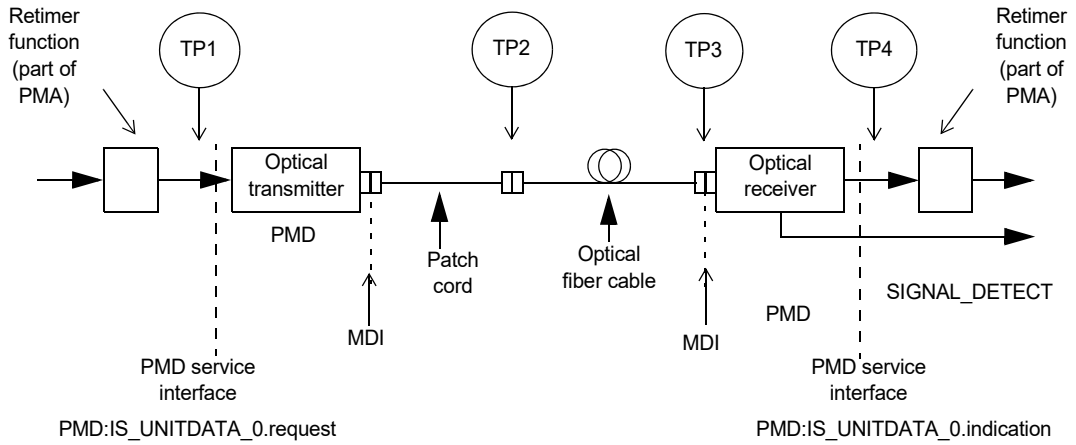

Figure 139–2—Block diagram for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER transmit/receive paths

139.5.2 PMD transmit function

The PMD Transmit function shall convert the symbol stream requested by the PMD service interface messages PMD:IS_UNITDATA_0.request into an optical signal. The optical signal shall then be delivered to the MDI, according to the transmit optical specifications in this clause. The four optical power levels in the signal in order from lowest to highest shall correspond to tx_symbol values zero, one, two, and three, respectively.

139.5.3 PMD receive function

The PMD receive function shall convert the optical signal received from the MDI into a symbol stream for delivery to the PMD service interface using the message PMD:IS_UNITDATA_0.indication, all according to the receive optical specifications in this clause. The four optical power levels in each signal in order from lowest to highest shall correspond to rx_symbol values zero, one, two, and three, respectively.

139.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 131.3.

SIGNAL_DETECT shall be a global indicator of the presence of the optical signal. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 139–4. The PMD receiver is not required to verify whether a compliant 50GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

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Table 139–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
Average optical power at TP3 ≤ –16 dBm	FAIL
[(Optical power at TP3 ≥ average receive power in Table 139–7) AND (compliant 50GBASE-R signal input)]	OK
All other conditions	Unspecified

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

139.5.5 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

139.5.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows the optical transmitter to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of the OFF transmitter in Table 139–6.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter.

139.5.7 PMD fault function (optional)

If the PMD has detected a local fault on the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

139.5.8 PMD transmit fault function (optional)

If the PMD has detected a local fault on the transmitter, the PMD shall set the PMD_transmit_fault variable to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

139.5.9 PMD receive fault function (optional)

If the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

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139.6 PMD to MDI optical specifications for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER

The operating ranges for the 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER PMDs are defined in Table 139–5. A 50GBASE-FR, 50GBASE-LR, or 50GBASE-ER compliant PMD operates on type B1.1, B1.3, or B6_a single-mode fibers according to the specifications defined in Table 139–13. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 50GBASE-FR PMD operating at 2.5 km meets the operating range requirement of 2 m to 2 km).

The 50GBASE-LR PMD interoperates with the 50GBASE-FR PMD provided that the channel requirements for 50GBASE-FR are met.

The 50GBASE-ER PMD interoperates with the 50GBASE-FR PMD provided that the channel requirements defined in 139.11 are met.

The 50GBASE-ER PMD interoperates with the 50GBASE-LR PMD provided that the channel requirements defined in 139.12 are met,

Table 139–5—50GBASE-FR, 50GBASE-LR, and 50GBASE-ER operating ranges

PMD type	Required operating range
50GBASE-FR	2 m to 2 km
50GBASE-LR	2 m to 10 km
50GBASE-ER	2 m to 30 km
	2 m to 40 km[a]

[a] Links longer than 30 km for the same link power budget are considered engineered links. Attenuation for such links needs to be less than the worst case specified for IEC 60793-2-50 type B1.1, type B1.3, or type B6_a single-mode fiber.

139.6.1 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER transmitter optical specifications

The 50GBASE-FR transmitter shall meet the specifications defined in Table 139–6 per the definitions in 139.7. The 50GBASE-LR transmitter shall meet the specifications defined in Table 139–6 per the definitions in 139.7. The 50GBASE-ER transmitter shall meet the specifications defined in Table 139–6 per the definitions in 139.7.

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Table 139–6—50GBASE-FR, 50GBASE-LR, and 50GBASE-ER transmit characteristics

Description	50GBASE-FR	50GBASE-LR	50GBASE-ER	Unit
Signaling rate (range)	26.5625 ± 100 ppm			GBd
Modulation format	PAM4			—
Wavelengths (range)	1304.5 to 1317.5			nm
Side-mode suppression ratio (SMSR), (min)	30			dB
Average launch power (max)	3	4.2	6.6	dBm
Average launch power[a] (min)	–4.1	–4.5	0.4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (max)	2.8	4	7.4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (min)[b]	–2.5	–1.5	3.4	dBm
Launch power in OMA_{outer} minus TDECQ (min)	–3.9	–2.9	2	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ) (max)	3	3.2	3.2	dB
TDECQ – $10\log_{10}(C_{eq})$[c] (max)	3	3.2	3.2	dB
Average launch power of OFF transmitter (max)	–16		–15	dBm
Extinction ratio (min)	3.5		6	dB
Transmitter transition time (max)	34			ps
$RIN_{17.1}OMA$ (max)	–132	—	—	dB/Hz
$RIN_{15.6}OMA$ (max)	—	–132	—	dB/Hz
$RIN_{15}OMA$ (max)	—	—	–132	dB/Hz
Optical return loss tolerance (max)	17.1	15.6	15	dB
Transmitter reflectance[d] (max)	–26			dB

[a] Average launch power (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b] Even if the TDECQ < 1.4 dB, the OMA_{outer} (min) has to exceed this value.
[c] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[d] Transmitter reflectance is defined looking into the transmitter.

139.6.2 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER receive optical specifications

The 50GBASE-FR receiver shall meet the specifications defined in Table 139–7 per the definitions in 139.7.
The 50GBASE-LR receiver shall meet the specifications defined in Table 139–7 per the definitions in 139.7.
The 50GBASE-ER receiver shall meet the specifications defined in Table 139–7 per the definitions in 139.7.

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Table 139–7—50GBASE-FR, 50GBASE-LR, and 50GBASE-ER receive characteristics

Description	50GBASE-FR	50GBASE-LR	50GBASE-ER	Unit
Signaling rate (range)	26.5625 ± 100 ppm			GBd
Modulation format	PAM4			—
Wavelengths (range)	1304.5 to 1317.5			nm
Damage threshold[a]	5.2	5.2	–2.4	dBm
Average receive power (max)	3	4.2	–3.4	dBm
Average receive power[b] (min)	–8.1	–10.8	–17.6	dBm
Receive power (OMA_{outer}) (max)	2.8	4	–2.6	dBm
Receiver reflectance (max)	–26			dB
Receiver sensitivity (OMA_{outer})[c] (max)	Equation (139–1)	Equation (139–2)	Equation (139–3)	dBm
Stressed receiver sensitivity (OMA_{outer})[d] (max)	–5.3	–6.6	–13.3	dBm
Conditions of stressed receiver sensitivity test:[e]				
Stressed eye closure for PAM4 (SECQ)	3	3.2	3.2	dB
SECQ – $10\log_{10}(C_{eq})$[f] (max)	3	3.2	3.2	dB

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
[b] Average receive power (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] Receiver sensitivity (OMA_{outer}) (max) is optional and is defined for a transmitter with a value of SECQ up to 3 dB for 50GBASE-FR and 3.2 dB for 50GBASE-LR and 50GBASE-ER.
[d] Measured with conformance test signal at TP3 (see 139.7.10) for the BER specified in 139.1.1.
[e] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

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139.6.3 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER illustrative link power budgets

Illustrative power budgets and penalties for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER channels are shown in Table 139–8.

Table 139–8—50GBASE-FR, 50GBASE-LR, and 50GBASE-ER illustrative link power budgets

Parameter	50GBASE-FR	50GBASE-LR	50GBASE-ER		Unit
Power budget (for maximum TDECQ)	7.4	10.1	21.7		dB
Operating distance	2	10	30	40[a]	km
Channel insertion loss	4[b]	6.3[c]	15	18	dB
Maximum discrete reflectance	See 139.10.2.2	See 139.10.2.2	See 139.10.2.2		dB
Allocation for penalties[d] (for maximum TDECQ)	3.4	3.8	3.7		dB
Additional insertion loss allowed	0	0	3	0	dB

[a] Links longer than 30 km are considered engineered links. Attenuation for such links needs to be less than the worst case for cables containing IEC 60793-2-50 type B1.1, type B1.3, or type B6_a single-mode cabled optical fiber.
[b] The channel insertion loss is calculated using the maximum distance specified in Table 139–5 for 50GBASE-FR and fiber attenuation of 0.5 dB/km plus an allocation for connection and splice loss given in 139.10.2.1.
[c] The channel insertion loss is calculated using the maximum distance specified in Table 139–5 for 50GBASE-LR and fiber attenuation of 0.43 dB/km at 1304.5 nm plus an allocation for connection and splice loss given in 139.10.2.1.
[d] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

139.7 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

139.7.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 139–10 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 139–10 may be used to perform that test. The test patterns used in this clause are shown in Table 139–9.

Table 139–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle encoded by RS-FEC	82.2.11[a], 134
6	SSPRQ	120.5.11.2.3

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[a]As modified by Clause 133.

Table 139–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 50GBASE-R signal	139.7.2
Side-mode suppression ratio	3, 5, 6 or valid 50GBASE-R signal	139.7.2
Average optical power	3, 5, 6 or valid 50GBASE-R signal	139.7.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	139.7.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	139.7.5
Extinction ratio	4 or 6	139.7.6
Transmitter transition time	Square wave or 6	139.7.7
$RIN_{15.1}OMA$, $RIN_{16.5}OMA$, and $RIN_{15}OMA$	Square wave	139.7.8
Stressed receiver conformance test signal calibration	6	139.7.10.2
Stressed receiver sensitivity	3 or 5	139.7.10

139.7.2 Wavelength and side-mode suppression ratio (SMSR)

The wavelength and SMSR shall be within the ranges given in Table 139–6 for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER, if measured per IEC 61280-1-3. The transmitter is modulated using the test pattern defined in Table 139–10.

139.7.3 Average optical power

The average optical power shall be within the limits given in Table 139–6 for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER if measured using the methods given in IEC 61280-1-1.

139.7.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} shall be within the limits given in Table 139–6 for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER. The OMA_{outer} is measured using a test pattern specified for OMA_{outer} in Table 139–10 as the difference between the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 139–3.

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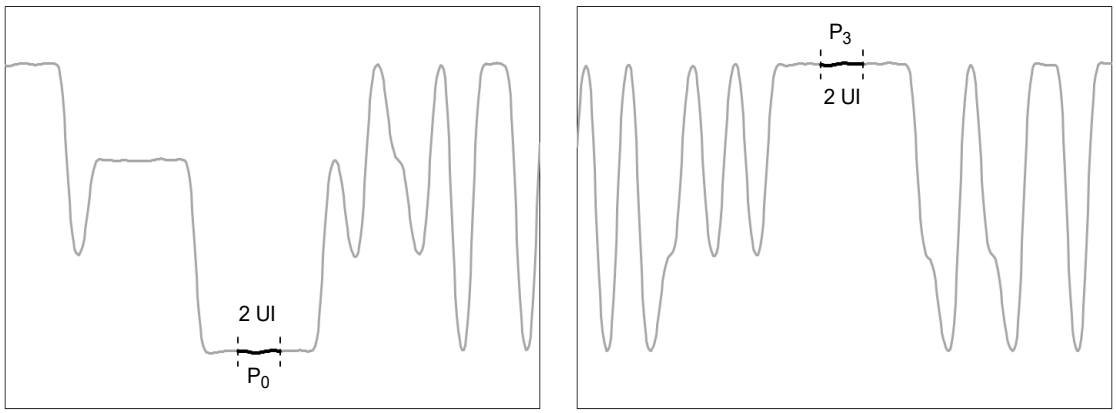

Figure 139–3—Example power levels P_0 and P_3 from PRBS13Q test pattern

139.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

The TDECQ and TDECQ – $10\log_{10}(C_{eq})$ shall be within the limits given in Table 139–6 for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER if measured using the methods specified in 139.7.5.1, 139.7.5.2, and 139.7.5.3.

TDECQ is a measure of each optical transmitter's vertical eye closure when transmitted through a worst case optical channel (specified in 139.7.5.2), as measured through an optical to electrical converter (O/E) with a bandwidth equivalent to a reference receiver, and equalized with the reference equalizer (as described in 139.7.5.4). The reference receiver and equalizer may be implemented in software or may be part of the oscilloscope.

Table 139–10 specifies the test patterns to be used for measurement of TDECQ.

139.7.5.1 TDECQ conformance test setup

A block diagram for the TDECQ conformance test is shown in Figure 139–4. Other equivalent measurement implementations may be used with suitable calibration.

The optical splitter and variable reflector are adjusted so that each transmitter is tested with the optical return loss specified in Table 139–11. The state of polarization of the back reflection is adjusted to create the greatest RIN. The signal is tested with the optical channel described in 139.7.5.2. The combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz and at frequencies above 1.5 × 26.5625 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The test pattern (specified in Table 139–11) is transmitted repetitively and the oscilloscope is set up to capture the complete pattern for TDECQ analysis as described in 139.7.5.3. The clock recovery unit (CRU) has a corner frequency of 4 MHz and a slope of 20 dB/decade. The CRU can be implemented in hardware or software depending on oscilloscope technology.

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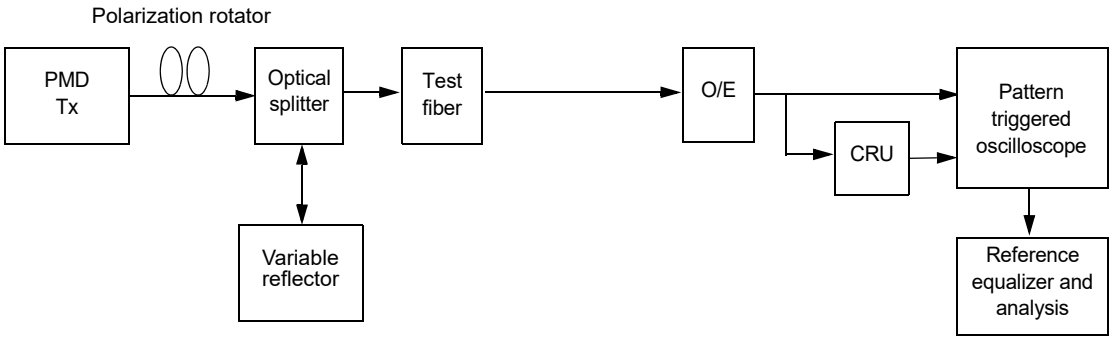

Figure 139–4—TDECQ conformance test block diagram

139.7.5.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 139–11.

Table 139–11—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]	Max mean DGD
	Minimum	Maximum			
50GBASE-FR	$0.0465 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.0465 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	17.1 dB	0.8 ps
50GBASE-LR	$0.2325 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.2325 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	15.6 dB	0.8 ps
50GBASE-ER	$0.93 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.93 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	15 dB	0.8 ps

[a]The dispersion is measured for the wavelength of the device under test (λ in nm). The coefficient assumes 2 km for 50GBASE-FR, 10 km for 50GBASE-LR, and 40 km for 50GBASE-ER.
[b]There is no intent to stress the sensitivity of the O/E converter associated with the oscilloscope.
[c]The optical return loss is applied at TP2.

A 50GBASE-FR, 50GBASE-LR, or 50GBASE-ER transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 139–11 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss specified in Table 139–11. The state of polarization of the back reflection is adjusted to create the greatest RIN.

The mean DGD of the channel is to be less than the value specified in Table 139–11.

139.7.5.3 TDECQ measurement method

TDECQ for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER is measured as described in 121.8.5.3 with the exception that the reference equalizer is as specified in 139.7.5.4.

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139.7.5.4 TDECQ reference equalizer

The reference equalizer for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER is a 5-tap, T-spaced, feed-forward equalizer (FFE), where T is the symbol period. A functional model of the reference equalizer is shown in Figure 139–5. The sum of the equalizer tap coefficients is equal to 1. Tap 1, tap 2, or tap 3, has the largest magnitude tap coefficient, which is constrained to be at least 0.8.

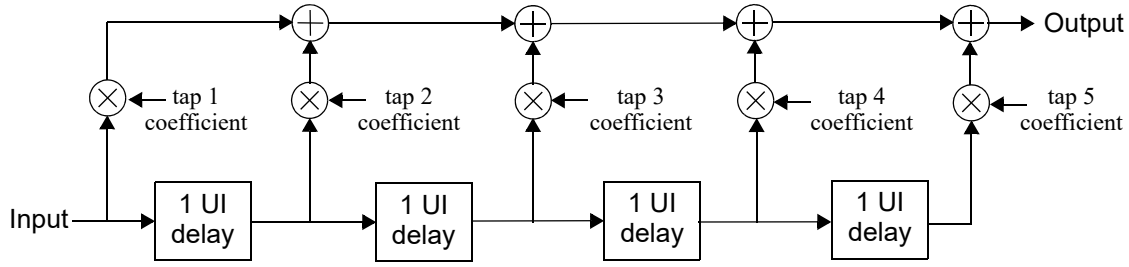

Figure 139–5—TDECQ reference equalizer functional model

NOTE—This reference equalizer is part of the TDECQ test and does not imply any particular receiver equalizer implementation.

139.7.6 Extinction ratio

The extinction ratio shall be within the limits given in Table 139–6 for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER if measured using a test pattern specified for extinction ratio in Table 139–10. The extinction ratio of a PAM4 optical signal is defined as the ratio of the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 139–3.

139.7.7 Transmitter transition time

The transmitter transition time of each lane shall be within the limits given in Table 139–6 if measured using a test pattern specified for transmitter transition time in Table 139–10.

Transmitter transition time is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer}, or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling edges respectively, as measured through an O/E converter and oscilloscope with a combined 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz and at frequencies above 1.5 × 26.5625 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The 0% level and the 100% level are P_0 and P_3 as defined by the OMA_{outer} measurement procedure (see 139.7.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence and the falling edge is that within the 33333000000 symbol sequence.

139.7.8 Relative intensity noise ($RIN_{17.1}OMA$, $RIN_{15.6}OMA$, and $RIN_{15}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 17.1 dB for 50GBASE-FR, 15.6 dB for 50GBASE-LR, and 15 dB for 50GBASE-ER.
b) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 26.6 GHz).

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c) The test pattern is according to Table 139–10.

139.7.9 Receiver sensitivity

For 50GBASE-FR, receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 3 dB. Receiver sensitivity should meet Equation (139–1), which is illustrated in Figure 139–6.

For 50GBASE-LR, receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 3.2 dB. Receiver sensitivity should meet Equation (139–2), which is illustrated in Figure 139–6.

For 50GBASE-ER, receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 3.2 dB. Receiver sensitivity should meet Equation (139–3), which is illustrated in Figure 139–6.

$$RS = \max(-6.9, SECQ - 8.3) \quad \text{(dBm)} \tag{139–1}$$

$$RS = \max(-8.4, SECQ - 9.8) \quad \text{(dBm)} \tag{139–2}$$

$$RS = \max(-15.1, SECQ - 16.5) \quad \text{(dBm)} \tag{139–3}$$

where

RS is the receiver sensitivity
SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

The normative requirement for receivers is stressed receiver sensitivity.

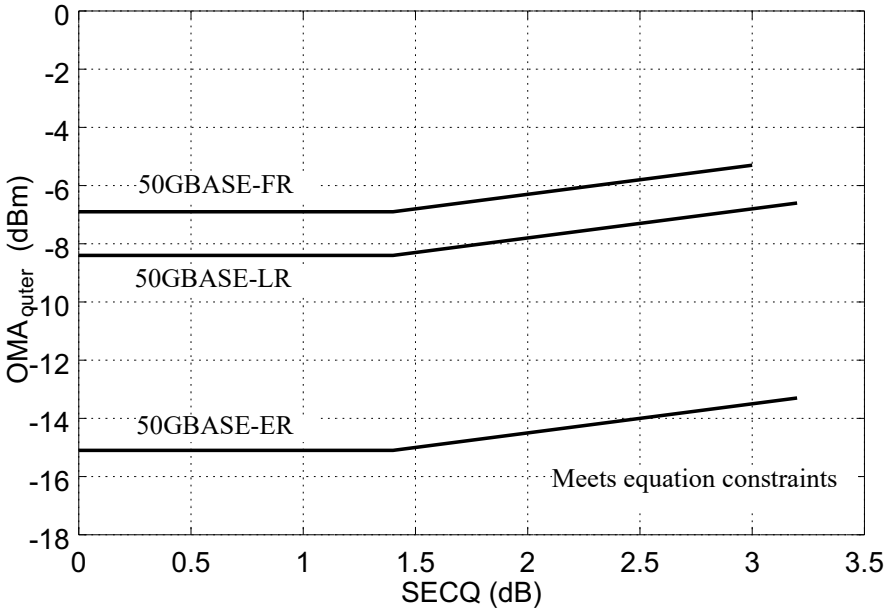

Figure 139–6—Illustration of receiver sensitivity

139.7.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 139–7 for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER if measured using the method defined in 139.7.10.1 and 139.7.10.3, with

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the conformance test signal at TP3 as described in 139.7.10.2, using the test pattern specified for SRS in Table 139–10.

Any of the patterns specified for SRS in Table 139–10 is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal.

139.7.10.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 139–7. The patterns used for the received conformance signal are specified in Table 139–10. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 139.7.10.2 and has sinusoidal jitter applied as specified in 121.8.10.4. A suitable test set is needed to characterize the signal used to test the receiver. Stressed receiver conformance test signal verification is described in 139.7.10.3.

The low-pass filter is used to create ISI. The sinusoidal amplitude interferer causes additional eye closure, but in conjunction with the finite edge rates, also causes some jitter.

The sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferer may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferer, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The Gaussian noise generator, the amplitude of the sinusoidal interferer, and the low-pass filter are adjusted so that the SECQ specified in Table 139–7 is met, according to the methods specified in 139.7.10.2.

For improved visibility for calibration, all elements in the signal path (cables, DC blocks, E/O converter, etc.) should have wide and smooth frequency response, and linear phase response, throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be negligible.

139.7.10.2 Stressed receiver conformance test signal characteristics and calibration

The stressed receiver conformance test signal characteristics and calibration methods are as described in 121.8.10.2 with the following exceptions:

- The SECQ of the stressed receiver conformance test signal is measured according to 139.7.5, except that the test fiber is not used. The transition time of the stressed receiver conformance test signal is no greater than the value specified in Table 139–6.
- With the Gaussian noise generator on and the sinusoidal jitter and sinusoidal interferer turned off, the $RIN_{17.1}OMA$, $RIN_{15.6}OMA$, and $RIN_{15}OMA$ of the SRS test source for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER, respectively, should be no greater than the values specified in Table 139–6.
- An example stressed receiver conformance test setup is shown in Figure 139–7; however, alternative test setups that generate equivalent stress conditions may be used.
- The signaling rate of the test pattern generator and the extinction ratio of the E/O converter are as given in Table 139–6 for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER.
- The required values of the “Stressed receiver sensitivity (OMA_{outer}) (max)”, “Stressed eye closure for PAM4 (SECQ)”, and “SECQ – $10\log_{10}(C_{eq})$ (max)” are as given in Table 139–7 for 50GBASE-FR and 50GBASE-LR.

139.7.10.3 Stressed receiver conformance test signal verification

The SECQ of the stressed receiver conformance test signal is measured according to 139.7.5, except that the test fiber is not used. The clock output from the clock source in Figure 139–7 is modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye jitter that includes the sinusoidal

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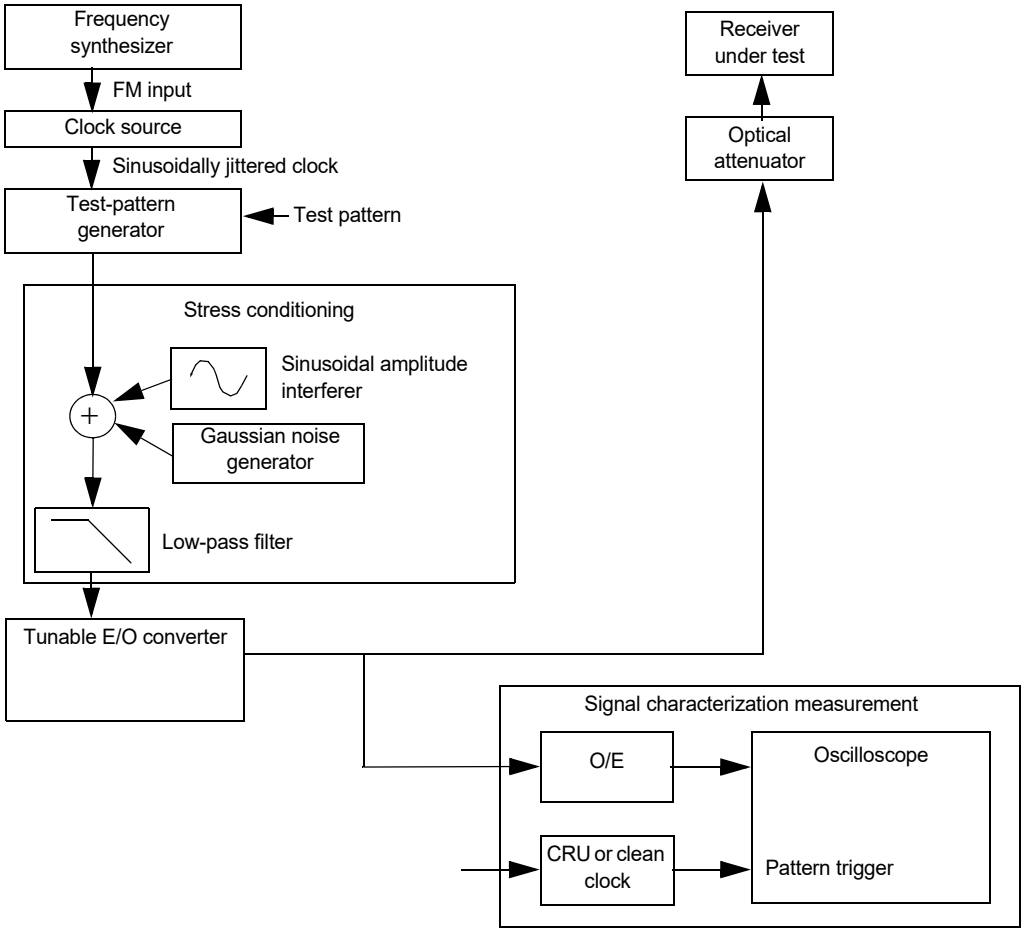

Figure 139–7—Stressed receiver conformance test block diagram

jitter component, a separate clock source (clean clock of Figure 139–7) is required that is synchronized to the source clock, but not modulated with the jitter source.

Care should be taken when characterizing the test signal because excessive noise/jitter in the measurement system would result in an input signal that does not fully stress the receiver under test. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. The noise/jitter introduced by the O/E, filters, and oscilloscope should be negligible or the results should be corrected for its effects. While the details of test equipment are beyond the scope of this standard, it is recommended that the implementer fully characterize the test equipment and apply appropriate guard bands to ensure that the stressed receiver conformance input signal meets the stress and sinusoidal jitter specified in 139.7.10.2 and 121.8.10.4.

139.8 Safety, installation, environment, and labeling

139.8.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

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139.8.2 Laser safety

50GBASE-FR, 50GBASE-LR, and 50GBASE-ER optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[231]

139.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

139.8.4 Environment

Normative specifications in this clause shall be met by a system integrating a 50GBASE-FR, 50GBASE-LR, or 50GBASE-ER PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

139.8.5 Electromagnetic emission

A system integrating a 50GBASE-FR, 50GBASE-LR, or 50GBASE-ER PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

139.8.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

139.8.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 50GBASE-FR).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 139.8.2.

[231] A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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139.9 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 139–8.

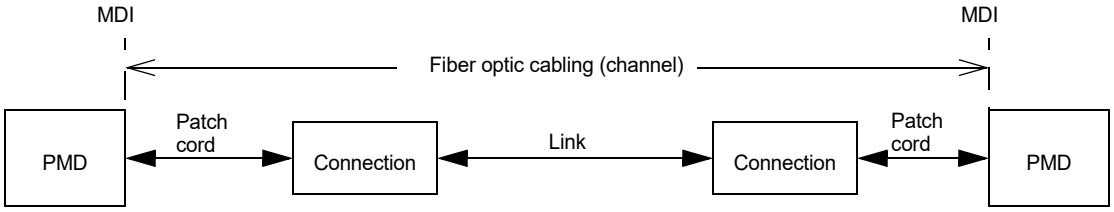

Figure 139–8—Fiber optic cabling model

The channel insertion loss is given in Table 139–12. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 139–12—Fiber optic cabling (channel) characteristics

Description	50GBASE-FR	50GBASE-LR	50GBASE-ER		Unit
Operating distance (max)	2	10	30	40	km
Channel insertion loss[a, b] (max)	4	6.3	18		dB
Channel insertion loss (min)	0	0	10[c]		dB
Positive dispersion[b] (max)	3.2	16	48	64	ps/nm
Negative dispersion[b] (min)	–3.7	–18.6	–56	–74	ps/nm
DGD_max[d]	3	8	10.3		ps
Optical return loss (min)	25	22	19		dB

[a] These channel insertion loss values include cable, connectors, and splices.
[b] Over the wavelength range 1304.5 nm to 1317.5 nm for 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER.
[c] Channel insertion loss (min) may be implemented with an optical attenuator.
[d] Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

139.10 Characteristics of the fiber optic cabling (channel)

The 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER fiber optic cabling shall meet the specifications defined in Table 139–12. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

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139.10.1 Optical fiber cable

The fiber optic cable requirements are satisfied by cables containing IEC 60793-2-50 type B1.1 (dispersion unshifted single-mode), type B1.3 (low water peak single-mode), or type B6_a (bend insensitive) fibers or the requirements in Table 139–13 where they differ.

Table 139–13—Optical fiber and cable characteristics

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.43[a] or 0.5[b]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \leq \lambda_0 \leq 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a]The 0.43 dB/km at 1304.5 nm attenuation for optical fiber cables is derived from Appendix I of ITU-T G.695.
[b]The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3. Using 0.5 dB/km may not support operation 10 km for 50GBASE-LR or 40 km for 50GBASE-ER.

139.10.2 Optical fiber connection

An optical fiber connection, as shown in Figure 139–8, consists of a mated pair of optical connectors.

139.10.2.1 Connection insertion loss

The maximum link distance for 50GBASE-LR and 50GBASE-ER is based on an allocation of 2 dB total connection and splice loss. For example, this allocation supports four connections with an average insertion loss per connection of 0.5 dB. The maximum link distance for 50GBASE-FR is based on an allocation of 3 dB total connection and splice loss. Connections with different loss characteristics may be used provided the requirements of Table 139–12 are met.

139.10.2.2 Maximum discrete reflectance

The maximum value for each discrete reflectance shall be less than or equal to the value shown in Table 139–14 corresponding to the number of discrete reflectances above –55 dB within the channel. For numbers of discrete reflectances in between two numbers shown in the table, the lower of the two corresponding maximum discrete reflectance values applies.

139.10.3 Medium Dependent Interface (MDI) requirements

The 50GBASE-FR, 50GBASE-LR, or 50GBASE-ER PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the “fiber optic cabling” (as shown in Figure 139–8). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 139.5.1, not at the MDI.

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Table 139–14—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance		
	50GBASE-FR	50GBASE-LR	50GBASE-ER
1	–25 dB	–22 dB	–19 dB
2	–31 dB	–29 dB	–27 dB
4	–35 dB	–33 dB	–32 dB
6	–38 dB	–35 dB	–35 dB
8	–40 dB	–37 dB	–37 dB
10	–41 dB	–39 dB	–39 dB

139.11 Requirements for interoperation between 50GBASE-ER and 50GBASE-FR

The 50GBASE-ER and 50GBASE-FR PMDs can interoperate with each other (over an engineered link) provided that the fiber optic cabling (channel) characteristics for 50GBASE-FR are met, with the exception of the maximum and minimum channel insertion loss values, which are given in Table 139–15 for the two link directions separately. Attenuators may be used to achieve the required losses.

Table 139–15—Channel insertion loss requirements for interoperation between 50GBASE-ER and 50GBASE-FR

Direction	Min loss	Max loss	Unit
50GBASE-ER transmitter to 50GBASE-FR receiver	4.6	8.5	dB
50GBASE-FR transmitter to 50GBASE-ER receiver	6.4	12.2	dB

139.12 Requirements for interoperation between 50GBASE-ER and 50GBASE-LR

The 50GBASE-ER and 50GBASE-LR PMDs can interoperate with each other (over an engineered link) provided that the fiber optic cabling (channel) characteristics for 50GBASE-LR are met, with the exception of the maximum and minimum channel insertion loss values, which are given in Table 139–16 for the two link directions separately. Attenuators may be used to achieve the required losses.

Table 139–16—Channel insertion loss requirements for interoperation between 50GBASE-ER and 50GBASE-LR

Direction	Min loss	Max loss	Unit
50GBASE-ER transmitter to 50GBASE-LR receiver	3.4	11.2	dB
50GBASE-LR transmitter to 50GBASE-ER receiver	7.6	13	dB

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139.13 Protocol implementation conformance statement (PICS) proforma for Clause 139, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER[232]

139.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 139, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

139.13.2 Identification

139.13.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

139.13.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 139, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[232]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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139.13.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*FR	50GBASE-FR PMD	139.6	Device supports requirements for 50GBASE-FR PHY	O.1	Yes [ ] No [ ]
*LR	50GBASE-LR PMD	139.6	Device supports requirements for 50GBASE-LR PHY	O.1	Yes [ ] No [ ]
*ER	50GBASE-ER PMD	139.6	Device supports requirements for 50GBASE-ER PHY	O.1	Yes [ ] No [ ]
*INS	Installation / cable	139.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	139.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	139.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	139.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	139.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	139.4	Registers and interface supported	O	Yes [ ] No [ ]

139.13.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR, 50GBASE-LR, and 50GBASE-ER

139.13.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 50GBASE-R PCS and PMA	139.1		M	Yes [ ]
F2	Integration with management functions	139.1		O	Yes [ ] No [ ]
F3	Bit error ratio	139.1.1	Meets the BER specified in 139.1.1	M	Yes [ ]
F4	Transmit function	139.5.2	Conveys symbols from PMD service interface to MDI	M	Yes [ ]
F6	Mapping between optical signal and logical signal for transmitter	139.5.2	Optical power levels from lowest to highest correspond to tx_symbol values zero, one, two, and three, respectively	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F7	Receive function	139.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]
F8	Conversion of optical signal to electrical signal	139.5.3	For delivery to the PMD service interface	M	Yes [ ]
F9	Mapping between optical signal and logical signal for receiver	139.5.3	Optical power levels from lowest to highest correspond to rx_symbol values zero, one, two, and three, respectively	M	Yes [ ]
F10	Global Signal Detect function	139.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F11	Global Signal Detect behavior	139.5.4	SIGNAL_DETECT is a global indicator of the presence of an optical signal	M	Yes [ ]
F12	PMD reset function	139.5.5	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

139.13.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	139.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	139.5.6	Disables the optical transmitter with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD_fault function	139.5.7	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD_transmit_fault function	139.5.8	Sets PMD_transmit_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_receive_fault function	139.5.9	Sets PMD_receive_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]

139.13.4.3 PMD to MDI optical specifications for 50GBASE-FR

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Item	Feature	Subclause	Value/Comment	Status	Support
FRF1	Transmitter meets specifications in Table 139–6	139.6.1	Per definitions in 139.7	FR:M	Yes [ ] N/A [ ]
FRF2	Receiver meets specifications in Table 139–7	139.6.2	Per definitions in 139.7	FR:M	Yes [ ] N/A [ ]

139.13.4.4 PMD to MDI optical specifications for 50GBASE-LR

Item	Feature	Subclause	Value/Comment	Status	Support
LRF1	Transmitter meets specifications in Table 139–6	139.6.1	Per definitions in 139.7	LR:M	Yes [ ] N/A [ ]
LRF2	Receiver meets specifications in Table 139–7	139.6.2	Per definitions in 139.7	LR:M	Yes [ ] N/A [ ]

139.13.4.5 PMD to MDI optical specifications for 50GBASE-ER

Item	Feature	Subclause	Value/Comment	Status	Support
ERF1	Transmitter meets specifications in Table 139–6	139.6.1	Per definitions in 139.7	ER:M	Yes [ ] N/A [ ]
ERF2	Receiver meets specifications in Table 139–7	139.6.2	Per definitions in 139.7	ER:M	Yes [ ] N/A [ ]

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139.13.4.6 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	139.7	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and SMSR	139.7.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	139.7.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA measurements	139.7.4		M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	139.7.5		M	Yes [ ]
OM6	Extinction ratio	139.7.6		M	Yes [ ]
OM7	Transmitter transition time	139.7.7		M	Yes [ ]
OM8	RIN_{xx}OMA measurement procedure	139.7.8		M	Yes [ ]
OM9	Stressed receiver sensitivity	139.7.10		M	Yes [ ]

139.13.4.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	139.8.1	Conforms to J.2	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	139.8.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	139.8.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

139.13.4.8 Characteristics of the fiber optic cabling and MD

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	139.10	Meets requirements specified in Table 139–12	INS:M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	139.10.2.2	Meets requirements specified in Table 139–14	INS:M	Yes [ ] N/A [ ]
OC3	MDI requirements	139.10.3	Meets IEC 61753-1-1 and IEC 61753-021-2	INS:M	Yes [ ] N/A [ ]

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140. Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1

140.1 Overview

This clause specifies the 100GBASE-DR, 100GBASE-FR1, and the 100GBASE-LR1 PMDs together with the single-mode fiber medium. The optical signals generated by these PMD types are modulated using a 4-level pulse amplitude modulation (PAM4) format. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 140–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 140–1—Physical Layer clauses associated with the 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 PMDs

Associated clause	100GBASE-DR, 100GBASE-FR1, 100GBASE-LR1
81—RS	Required
81—CGMII[a]	Optional
82—PCS	Required
83—100GBASE-R PMA	Optional
91—RS-FEC	Required
83A—CAUI-10 C2C	Optional
83B—CAUI-10 C2M	Optional
83D—CAUI-4 C2C	Optional
83E—CAUI-4 C2M	Optional
135—100GBASE-P PMA	Required
135D—100GAUI-4 C2C	Optional
135E—100GAUI-4 C2M	Optional
135F—100GAUI-2 C2C	Optional
135G—100GAUI-2 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation behaves functionally as though the RS and CGMII were present.

Figure 140–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 100 Gigabit Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2.

100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

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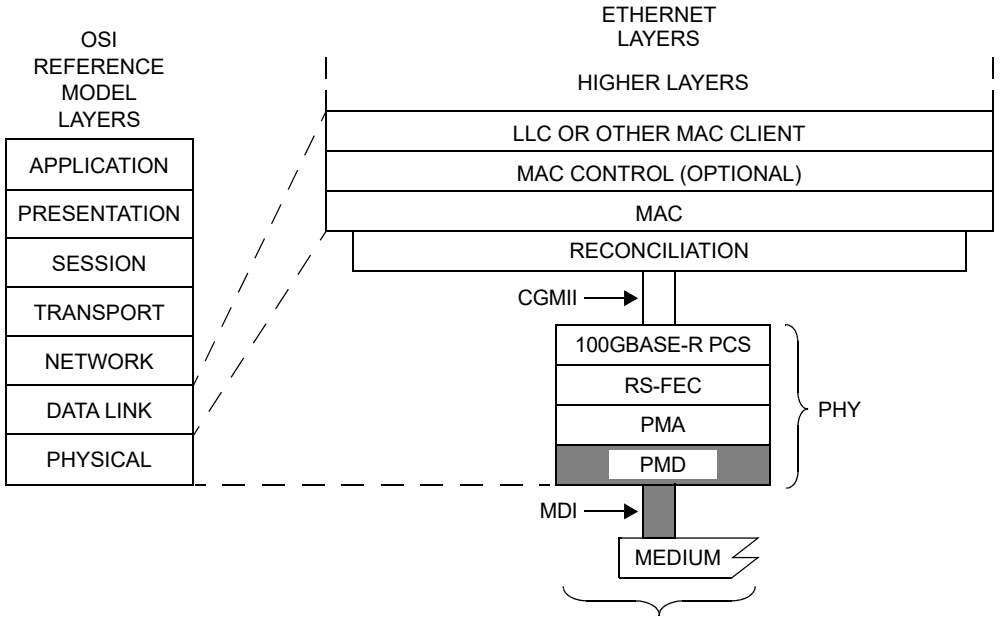

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

DR = PMD FOR SINGLE-MODE FIBER — 500 m
FR1 = PMD FOR SINGLE-MODE FIBER — 2 km
LR1 = PMD FOR SINGLE-MODE FIBER — 10 km

Figure 140–1—100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

140.1.1 Bit error ratio

The bit error ratio (BER) when processed by the PMA (Clause 135) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap when additionally processed by the FEC (Clause 91) and PCS (Clause 82). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-10} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap.

140.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

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The 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with a single symbol stream (n = 1).

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_0.request
PMD:IS_UNITDATA_0.indication
PMD:IS_SIGNAL.indication

In the transmit direction, the PMA continuously sends one stream of PAM4 symbols to the PMD using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 53.125 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends one stream of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 53.125 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable SIGNAL_DETECT parameter as defined in 140.5.4. The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 140.1.1.

140.3 Delay and Skew

140.3.1 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PMD including 2 m of fiber in one direction shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

140.3.2 Skew constraints

The Skew (relative delay) between the FEC lanes is kept within limits so that the information on the FEC lanes can be reassembled by the FEC. The Skew Variation is also limited to ensure that a given FEC lane always traverses the same physical lane. Skew and Skew Variation are defined in 80.5 and specified at the points SP0 to SP7 shown in Figure 80–9.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 83.5.3.4. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

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For more information on Skew and Skew Variation, see 80.5. The measurements of Skew and Skew Variation are defined in 89.7.2 with the exception that the measurement clock and data recovery unit high-frequency corner bandwidth is 4 MHz.

140.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 140–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 140–3.

Table 140–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable

Table 140–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect

140.5 PMD functional specifications

The 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PMD performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

140.5.1 PMD block diagram

The PMD block diagram is shown in Figure 140–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 140.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 140.10.3). Unless specified otherwise, all receiver measurements and tests defined in 140.7 are made at TP3.

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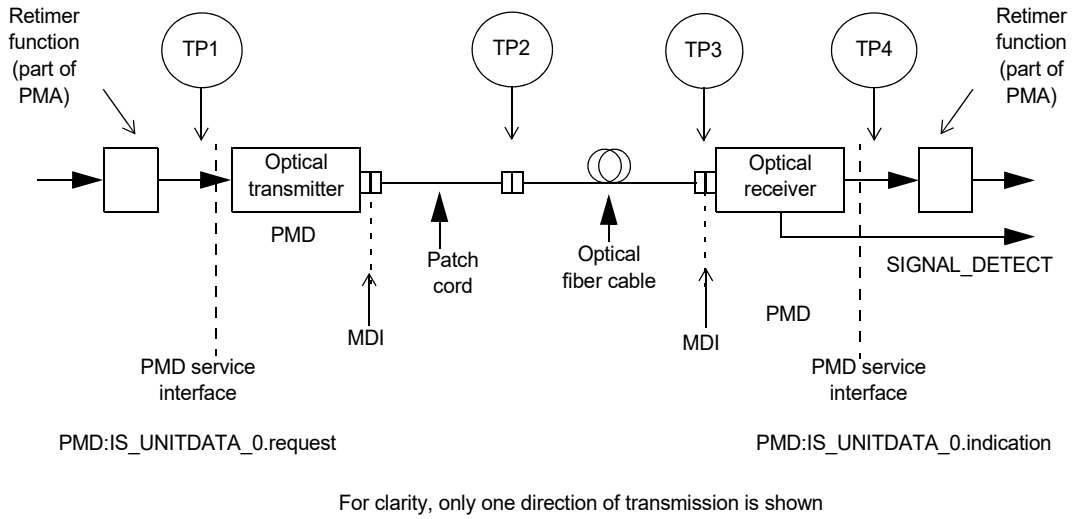

Figure 140–2—Block diagram for 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 transmit/receive paths

140.5.2 PMD transmit function

The PMD Transmit function shall convert the symbol stream requested by the PMD service interface messages PMD:IS_UNITDATA_0.request into an optical signal. The optical signal shall then be delivered to the MDI, according to the transmit optical specifications in this clause. The four optical power levels in the signal in order from lowest to highest shall correspond to tx_symbol values zero, one, two, and three, respectively.

140.5.3 PMD receive function

The PMD receive function shall convert the optical signal received from the MDI into a symbol stream for delivery to the PMD service interface using the message PMD:IS_UNITDATA_0.indication, all according to the receive optical specifications in this clause. The four optical power levels in each signal in order from lowest to highest shall correspond to rx_symbol values zero, one, two, and three, respectively.

140.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 131.3.

SIGNAL_DETECT shall be a global indicator of the presence of the optical signal. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 140–4. The PMD receiver is not required to verify whether a compliant 100GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

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Table 140–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
Average optical power at TP3 ≤ –15 dBm	FAIL
[(Optical power at TP3 ≥ average receive power (min) Table 140–7) AND (compliant 100GBASE–R signal input)]	OK
All other conditions	Unspecified

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

140.5.5 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

140.5.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows the optical transmitter to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of the OFF transmitter in Table 140–6.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter.

140.5.7 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

140.5.8 PMD transmit fault function (optional)

If the PMD has detected a local fault on the transmitter, the PMD shall set the PMD_transmit_fault variable to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

140.5.9 PMD receive fault function (optional)

If the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

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140.6 PMD to MDI optical specifications for 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1

The operating ranges for the 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 PMDs are defined in Table 140–5. A 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 compliant PMD operates on type B1.1, B1.3, or B6_a single-mode fibers according to the specifications defined in Table 140–14. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 100GBASE-DR PMD operating at 600 m meets the operating range requirement of 2 m to 500 m).

The 100GBASE-FR1 PMD interoperates with the 100GBASE-DR PMD provided that the channel and power guidelines in 140.11.1 are met.

The 100GBASE-LR1 PMD interoperates with the 100GBASE-DR PMD provided that the channel guidelines in 140.11.2 are met.

The 100GBASE-LR1 PMD interoperates with the 100GBASE-FR1 PMD provided that the channel guidelines in 140.11.3 are met.

Table 140–5—100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 operating ranges

PMD type	Required operating range
100GBASE-DR	2 m to 500 m
100GBASE-FR1	2 m to 2 km
100GBASE-LR1	2 m to 10 km

140.6.1 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 transmitter optical specifications

The 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 transmitter shall meet the specifications defined in Table 140–6 per the definitions in 140.7.

Table 140–6—100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 transmit characteristics

Description	100GBASE-DR	100GBASE-FR1	100GBASE-LR1	Unit
Signaling rate (range)	53.125 ± 100 ppm			GBd
Modulation format	PAM4			—
Wavelength (range)	1304.5 to 1317.5			nm
Side-mode suppression ratio (SMSR), (min)	30			dB
Average launch power (max)	4	4	4.8	dBm
Average launch power[a] (min)	–2.9	–3.1	–1.9	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (max)	4.2	4.2	5	dBm

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Table 140–6—100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 transmit characteristics *(continued)*

Description	100GBASE-DR	100GBASE-FR1	100GBASE-LR1	Unit
Outer Optical Modulation Amplitude (OMA_{outer}) (min)[b]	–0.8	—	—	dBm
for TDECQ < 1.4 dB	—	–0.1	1.1	dBm
for 1.4 dB ≤ TDECQ ≤ 3.4 dB	—	–1.5 + TDECQ	–0.3 + TDECQ	dBm
Launch power in OMA_{outer} minus TDECQ (min):				
for extinction ratio ≥ 5 dB	–2.2	—	—	dBm
for extinction ratio < 5 dB	–1.9	—	—	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ) (max)	3.4	3.4	3.4	dB
TDECQ – $10\log_{10}(C_{eq})$[c] (max)	3.4	—	—	dB
Transmitter eye closure for PAM4 (TECQ) (max)	—	3.4	3.4	dB
| TDECQ – TECQ | (max)	—	2.5	2.5	dB
Over/under-shoot (max)	—	22	22	%
Transmitter power excursion (max)	—	2	2.8	dBm
Extinction ratio (min)	3.5	3.5	3.5	dB
Transmitter transition time (max)	17	17	17	ps
Average launch power of OFF transmitter (max)	–15	–15	–15	dBm
RIN_xOMA (max), where *x* is the optical return loss tolerance (max)	–136	–136	–136	dB/Hz
Optical return loss tolerance (max)	15.5	17.1	15.6	dB
Transmitter reflectance[d] (max)	–26	–26	–26	dB

[a] Average launch power (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b] For 100GBASE-DR, the requirement on the OMA_{outer} (min) applies even in the cases where TDECQ < 1.4 dB for an extinction ratio of ≥ 5 dB or where TDECQ < 1.1 dB for an extinction ratio of < 5 dB.
[c] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[d] Transmitter reflectance is defined looking into the transmitter.

The values for OMA_{outer} (min) in Table 140–6 vary with TDECQ. Figure 140–3 illustrates this for 100GBASE-FR1 and 100GBASE-LR1, along with the values for OMA_{outer} (max).

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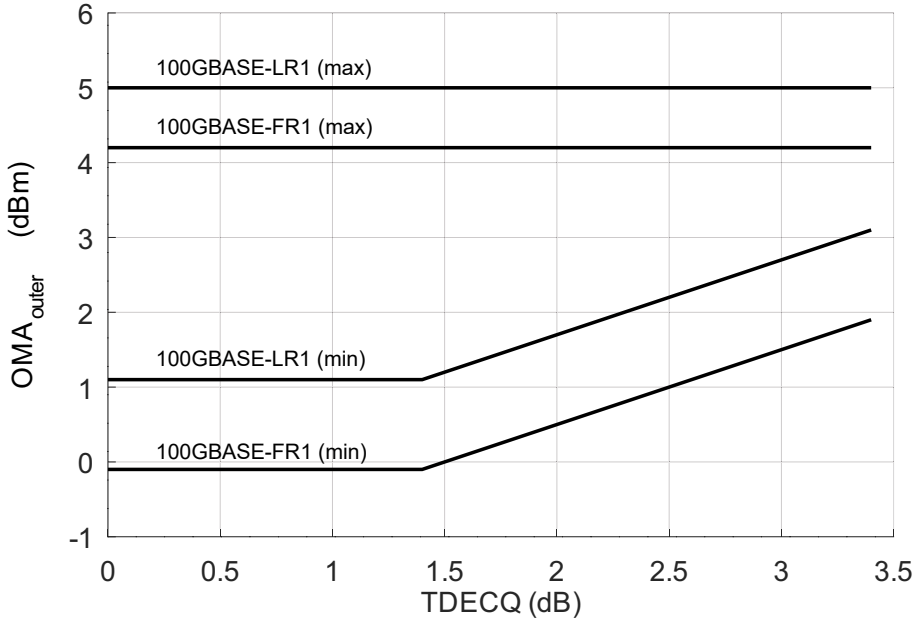

Figure 140–3—OMAouter (max) and OMAouter (min) versus TDECQ for 100GBASE-FR1 and 100GBASE-LR1

140.6.2 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 receive optical specifications

The 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 receiver shall meet the specifications defined in Table 140–7 per the definitions in 140.7.

Table 140–7—100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 receive characteristics

Description	100GBASE-DR	100GBASE-FR1	100GBASE-LR1	Unit
Signaling rate (range)	53.125 ± 100 ppm			GBd
Modulation format	PAM4			—
Wavelengths (range)	1304.5 to 1317.5			nm
Damage threshold[a]	5	5	5.8	dBm
Average receive power (max)	4	4	4.8	dBm
Average receive power[b] (min)	–5.9	–7.1	–8.2	dBm
Receive power (OMA_{outer}) (max)	4.2	4.2	5	dBm
Receiver reflectance (max)	–26	–26	–26	dB
Receiver sensitivity (OMA_{outer}) (max) for TECQ < 1.4 dB for 1.4 dB ≤ TECQ ≤ 3.4 dB	Equation (140–1)[c] — —	— –4.5 –5.9 + TECQ	— –6.1 –7.5 + TECQ	dBm dBm dBm

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Table 140–7—100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 receive characteristics *(continued)*

Description	100GBASE-DR	100GBASE-FR1	100GBASE-LR1	Unit
Stressed receiver sensitivity (OMA_{outer})[d] (max)	–1.9	–2.5	–4.1	dBm
Conditions of stressed receiver sensitivity test:[e]				
Stressed eye closure for PAM4 (SECQ)	3.4	3.4	3.4	dB
SECQ – $10\log_{10}(C_{eq})$[f] (max)	3.4	—	—	dB

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
[b] Average receive power (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] Receiver sensitivity (OMA_{outer}) (max) for 100GBASE-DR is optional and is defined for a transmitter with a value of SECQ up to 3.4 dB.
[d] Measured with conformance test signal at TP3 (see 140.7.13) for the BER specified in 140.1.1.
[e] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

The values for receiver sensitivity (OMAouter) (max) in Table 140–7 vary depending on the value of TECQ of the test source used for measurement. Figure 140–4 illustrates this for 100GBASE-FR1 and 100GBASE-LR1.

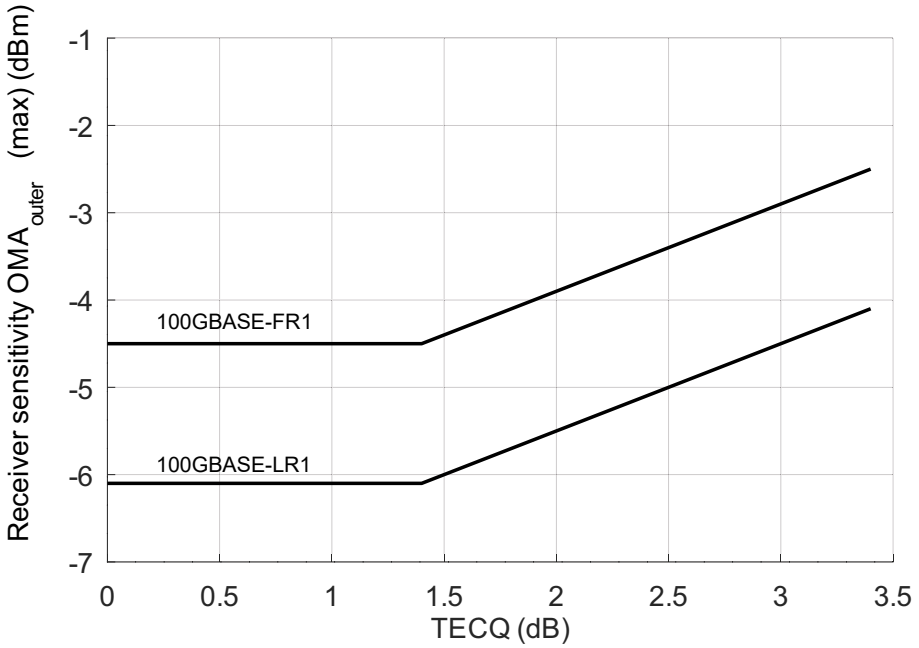

Figure 140–4—Receiver sensitivity (OMA_{outer}) (max) for 100GBASE-FR1 and 100GBASE-LR1

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140.6.3 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 illustrative link power budgets

Illustrative power budgets and penalties for 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 channels are shown in Table 140–8.

Table 140–8—100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 illustrative link power budgets

Parameter	100GBASE-DR	100GBASE-FR1	100GBASE-LR1	Unit
Power budget (for max TDECQ): for extinction ratio ≥ 5 dB for extinction ratio < 5 dB	— 6.5 6.8	7.8 — —	10.6 — —	dB dB dB
Operating distance	500	2 000	10 000	m
Channel insertion loss	See 140.9[a]	4[a]	6.3[b]	dB
Maximum discrete reflectance	–35	–35[c, d]	–35[c, e]	dB
Allocation for penalties[f] (for max TDECQ): for extinction ratio ≥ 5 dB for extinction ratio < 5 dB	— 6.5 minus max channel insertion loss per Table 140–13 6.8 minus max channel insertion loss per Table 140–13	3.8 — —	4.3 — —	dB dB dB
Additional insertion loss allowed	0	0	0	dB

[a] The channel insertion losses for 100GBASE-DR and 100GBASE-FR1 are calculated using the maximum distances specified in Table 140–5 and cabled optical fiber attenuation of 0.5 dB/km plus an allocation for connection and splice loss given in 140.10.2.1.
[b] The channel insertion loss for 100GBASE-LR1 is calculated using the maximum distance specified in Table 140–5 and fiber attenuation of 0.43 dB/km plus an allocation for connection and splice loss given in 140.10.2.1.
[c] See 140.10.2.2 for details and specifications as a function of the number of discrete reflectances within the channel.
[d] Maximum value for each discrete reflectance with 4 discrete reflectances above –55 dB within the channel.
[e] Maximum value for each discrete reflectance with 6 discrete reflectances above –55 dB within the channel.
[f] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

The values of transmitter OMA_{outer} (max), transmitter OMA_{outer} (min) versus TDECQ, and receiver sensitivity (OMA_{outer}) (max) versus TECQ are illustrated in Figure 140–5 for 100GBASE-FR1 and in Figure 140–6 for 100GBASE-LR1.

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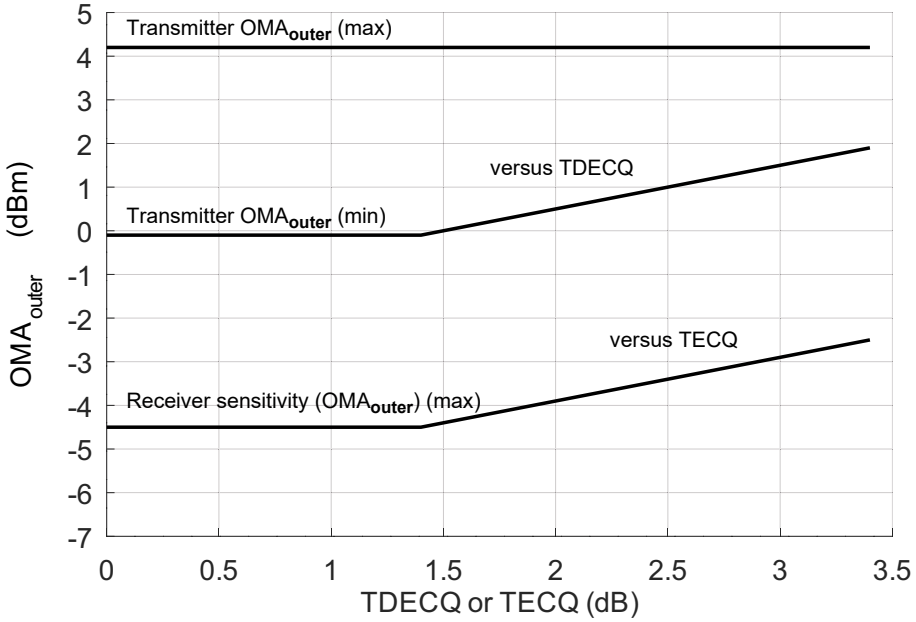

Figure 140–5—Transmitter OMA_{outer} versus TDECQ and receiver sensitivity (OMA_{outer}) versus TECQ for 100GBASE-FR1

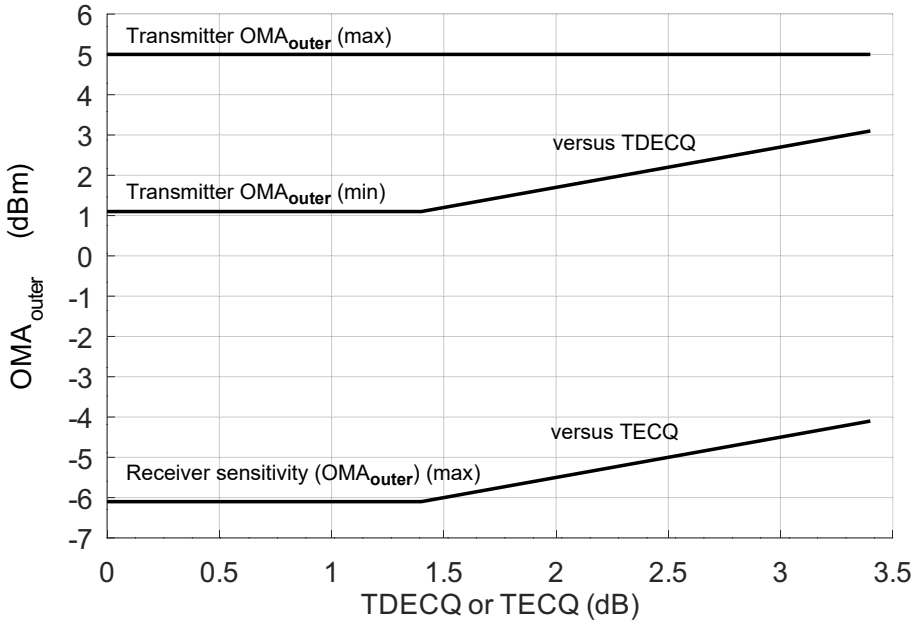

Figure 140–6—Transmitter OMA_{outer} versus TDECQ and receiver sensitivity (OMA_{outer}) versus TECQ for 100GBASE-LR1

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140.7 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

140.7.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 140–10 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 140–10 may be used to perform that test. The test patterns used in this clause are shown in Table 140–9.

Table 140–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle encoded by RS-FEC	82.2.11, 91
6	SSPRQ	120.5.11.2.3

Table 140–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 100GBASE-R signal	140.7.2
Side-mode suppression ratio	3, 5, 6 or valid 100GBASE-R signal	140.7.2
Average optical power	3, 5, 6 or valid 100GBASE-R signal	140.7.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	140.7.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	140.7.5
Transmitter eye closure for PAM4 (TECQ)	6	140.7.6
Over/under-shoot	6	140.7.7
Transmitter power excursion	6	140.7.8
Extinction ratio	4 or 6	140.7.9
Transmitter transition time	Square wave or 6	140.7.10
$RIN_x OMA$	Square wave	140.7.11
Receiver sensitivity	3 or 5	140.7.12
Stressed receiver conformance test signal calibration	6	140.7.13
Stressed receiver sensitivity	3 or 5	140.7.13

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140.7.2 Wavelength and side-mode suppression ratio (SMSR)

The wavelength and SMSR shall be within the range given in Table 140–6 if measured per IEC 61280-1-3. The transmitter is modulated using the test pattern defined in Table 140–10.

140.7.3 Average optical power

The average optical power shall be within the limits given in Table 140–6 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using the test pattern defined in Table 140–10, per the test setup in Figure 53–6.

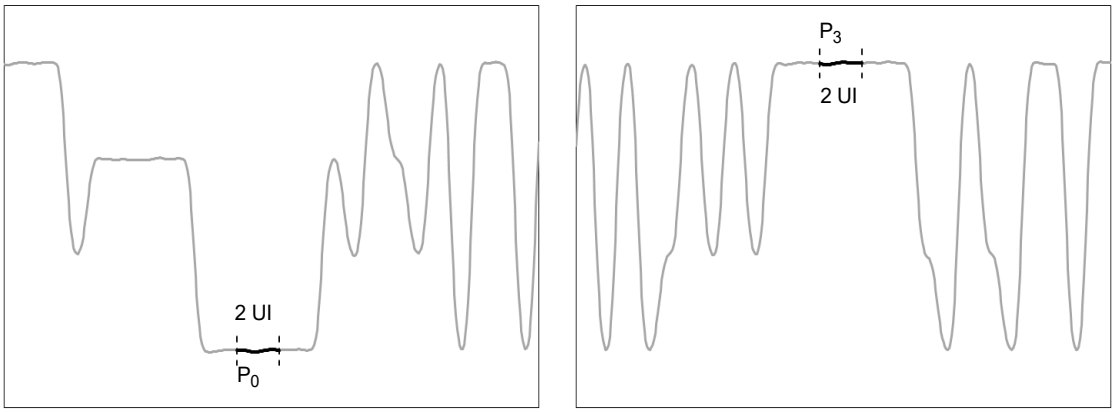

Figure 140–7—Example power levels P_0 and P_3 from PRBS13Q test pattern

140.7.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} shall be within the limits given in Table 140–6. The OMA_{outer} is measured using a test pattern specified for OMA_{outer} in Table 140–10 as the difference between the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 140–7.

140.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

TDECQ, and for 100GBASE-DR only, TDECQ – $10\log_{10}(C_{eq})$ shall be within the limits given in Table 140–6 if measured using the test setup specified in 121.8.5.1, with an optical channel specified in 140.7.5.2, using the measurement method specified in 121.8.5.3, and using a reference equalizer as described in 140.7.5.1, with the following exceptions:

- The signaling rate of the test pattern generator is as given in Table 140–6 and uses a test pattern specified for TDECQ in Table 140–10.
- There are no interfering optical lanes and therefore the delay requirement of at least 31 UI between test pattern on one lane and any other lane, as specified in 121.8.5.1, is redundant.
- The combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 26.5625 GHz with a fourth-order Bessel-Thomson response to at least 1.3 × 53.125 GHz and at frequencies above 1.3 × 53.125 GHz the response should not exceed –20 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.
- The normalized noise power density spectrum, $N(f)$ in Equation (121–9), is equivalent to white noise filtered by a fourth-order Bessel-Thomson response filter with a 3 dB bandwidth of 26.5625 GHz.

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140.7.5.1 TDECQ reference equalizer

The reference equalizer is a 5-tap, T-spaced, feed-forward equalizer (FFE), where T is the symbol period. A functional model of the reference equalizer is shown in Figure 140–8. The sum of the equalizer tap coefficients is equal to 1. Tap 1, tap 2, or tap 3 has the largest magnitude tap coefficient, which is constrained to be at least 0.8.

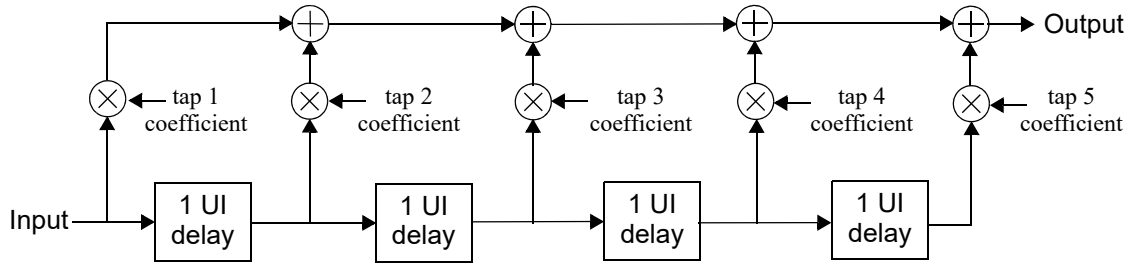

Figure 140–8—TDECQ reference equalizer functional model

NOTE—This reference equalizer is part of the TDECQ test and does not imply any particular receiver implementation.

140.7.5.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements in Table 140–11.

Table 140–11—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]	Max mean DGD
	Minimum	Maximum			
100GBASE-DR	$0.011625\times\lambda\times[1-(1324 / \lambda)^4]$	$0.011625\times\lambda\times[1-(1300 / \lambda)^4]$	Minimum	15.5 dB	0.5 ps
100GBASE-FR1	$0.046\times\lambda\times[1-(1324 / \lambda)^4]$	$0.046\times\lambda\times[1-(1300 / \lambda)^4]$	Minimum	17.1 dB	0.8 ps
100GBASE-LR1	$0.230\times\lambda\times[1-(1324 / \lambda)^4]$	$0.230\times\lambda\times[1-(1300 / \lambda)^4]$	Minimum	15.6 dB	0.8 ps

[a] The dispersion is measured for the wavelength of the transmitter under test (λ in nm). The coefficient assumes 500 m for 100GBASE-DR, 2 km for 100GBASE-FR1, and 10 km for 100GBASE-LR1.
[b] There is no intent to stress the sensitivity of the O/E converter associated with the oscilloscope.
[c] The optical return loss is applied at TP2.

A 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 140–11 for the wavelength of the transmitter under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss specified in Table 140–11. The state of polarization of the back reflection is adjusted to create the greatest RIN.

The mean DGD of the channel is to be less than the value specified in Table 140–11.

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140.7.6 Transmitter eye closure for PAM4 (TECQ)

The transmitter eye closure for PAM4 (TECQ) is a measure of the optical transmitter's eye closure at TP2. TECQ shall be within the limits given in Table 140–6 for 100GBASE-FR1 and 100GBASE-LR1 if measured using a test pattern specified for TECQ in Table 140–10. TECQ is measured using the methods specified for TDECQ in 140.7.5, except that the test fiber is not used.

140.7.7 Over/under-shoot

The over/under-shoot shall be within the limits given in Table 140–6 for 100GBASE-FR1 and 100GBASE-LR1 if measured using a test pattern specified for over/under-shoot in Table 140–10.

Over/under-shoot is measured using the waveforms captured for the TDECQ test (see 140.7.5) and the waveform captured for the TECQ test (see 140.7.6), but without the reference equalizer being applied in either case.

Overshoot is defined as the maximum power above the level three power and relative to the OMA_{outer} according to:

$$\text{Overshoot} = (P_{max} - P_3) / (OMA_{outer}) \times 100$$

Undershoot is defined as the minimum power from the transmitter (P_{min}) below the level zero power and relative to the OMA_{outer} according to:

$$\text{Undershoot} = (P_0 - P_{min}) / (OMA_{outer}) \times 100$$

where

P_{max}	is based on a 10^{-2} hit ratio, where P_{max} is the smallest power level that results in the number of samples above that level not exceeding the product of hit ratio and total number of observed samples, with all samples acquired in a single unit interval eye diagram.
P_{min}	is based on a 10^{-2} hit ratio, where P_{min} is the largest power level that results in the number of samples below that level not exceeding the product of hit ratio and total number of observed samples, with all samples acquired in a single unit interval eye diagram.
P_3	is the power of the PAM4 level three defined in 122.8.4.
P_0	is the power of the PAM4 level zero defined in 122.8.4.
OMA_{outer}	is the outer optical modulation amplitude defined in 122.8.4.

140.7.8 Transmitter power excursion

The transmitter power excursion shall be within the limits given in Table 140–6 for 100GBASE-FR1 and 100GBASE-LR1 if measured using a test pattern specified for transmitter power excursion in Table 140–10.

Transmitter power excursion is measured using the waveforms captured for the TECQ test (see 140.7.6), but without the reference equalizer being applied. Transmitter power excursion is defined as:

$$\text{Transmitter power excursion} = \max (P_{max} - P_{average} , P_{average} - P_{min})$$

where

P_{max} and P_{min}	are defined in 140.7.7
$P_{average}$	is the average optical power defined in 140.7.3

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140.7.9 Extinction ratio

The extinction ratio shall be within the limits given in Table 140–6 if measured using a test pattern specified for extinction ratio in Table 140–10. The extinction ratio of a PAM4 optical signal is defined as the ratio of the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 140–7.

140.7.10 Transmitter transition time

The transmitter transition time of each lane shall be within the limits given in Table 140–6 if measured using a test pattern specified for transmitter transition time in Table 140–10.

Transmitter transition time is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer}, or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling edges respectively, as measured through an O/E converter and oscilloscope with a combined 3 dB bandwidth of approximately 26.5625 GHz with a fourth-order Bessel-Thomson response to at least 1.3 × 53.125 GHz and at frequencies above 1.3 × 53.125 GHz the response should not exceed –20 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The 0% level and the 100% level are P_0 and P_3 as defined by the OMA_{outer} measurement procedure (see 140.7.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence and the falling edge is that within the 33333000000 symbol sequence.

140.7.11 Relative intensity noise ($RIN_x OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is *x* dB, where *x* is the optical return loss tolerance (max) in Table 140–6.

b) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 53.2 GHz).

140.7.12 Receiver sensitivity

140.7.12.1 Receiver sensitivity for 100GBASE-DR

The receiver sensitivity for 100GBASE-DR is optional and is defined for a transmitter with a value of SECQ up to 3.4 dB. Receiver sensitivity for 100GBASE-DR should meet Equation (140–1), which is illustrated in Figure 140–9. The normative requirement for the 100GBASE-DR receiver is stressed receiver sensitivity.

$$RS = \max(-3.9, SECQ - 5.3) \quad \text{(dBm)} \tag{140–1}$$

where

RS	is the receiver sensitivity
SECQ	is the SECQ of the transmitter used to measure the receiver sensitivity

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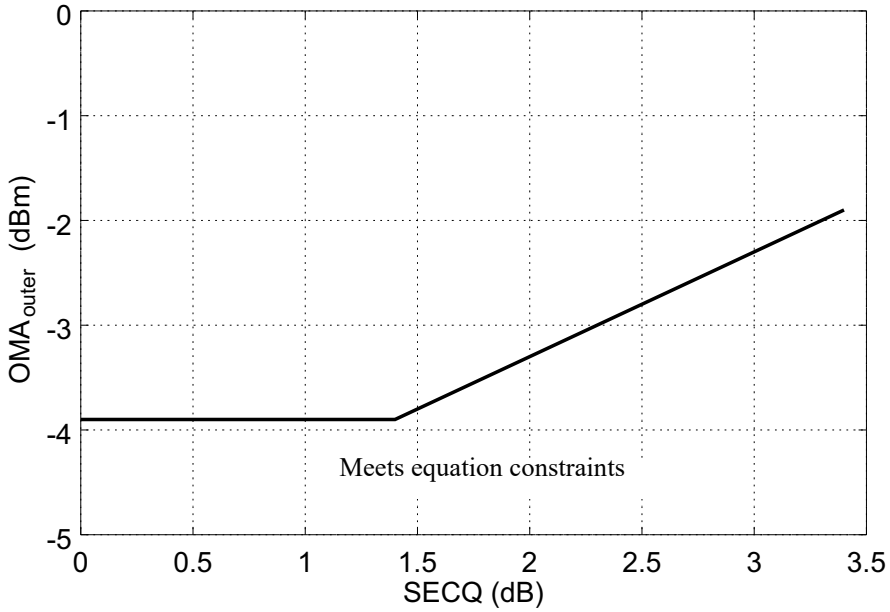

Figure 140–9—Illustration of receiver sensitivity

140.7.12.2 Receiver sensitivity for 100GBASE-FR1 and 100GBASE-LR1

The receiver sensitivity (OMA_{outer}) for 100GBASE-FR1 and 100GBASE-LR1 shall be within the limits given in Table 140–7 if measured using a test pattern for receiver sensitivity in Table 140–10.

The conformance test signal at TP3 meets the requirements for a 100GBASE-FR1 or 100GBASE-LR1 transmitter followed by an attenuator.

The TECQ of the conformance test signal is measured according to 140.7.5, except that the test fiber is not used. The measured value of TECQ is then used to calculate the limit for receiver sensitivity (OMA_{outer}) as specified in Table 140–7.

140.7.13 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 140–7 if measured using the method defined in 121.8.10, using the test pattern specified for SRS in Table 140–10, with the following exceptions:

— The SECQ of the stressed receiver conformance test signal is measured according to 140.7.5, except that the test fiber is not used. The transition time of the stressed receiver conformance test signal is no greater than the value specified in Table 140–6.

— With the Gaussian noise generator on and the sinusoidal jitter and sinusoidal interferer turned off, the RIN_xOMA of the SRS test source (where x is the value for optical return loss tolerance from Table 140–6) should be no greater than the value specified in Table 140–6.

— An example stressed receiver conformance test setup is shown in Figure 139–7; however, alternative test setups that generate equivalent stress conditions may be used.

— The signaling rate of the test pattern generator and the extinction ratio of the E/O converter are as given in Table 140–6 using test patterns specified in Table 140–10.

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— For 100GBASE-FR1 and 100GBASE-LR1 the values of over/under-shoot and transmitter power excursion of the stressed receiver conformance test signal are within the limits specified in Table 140–6.

— The required values of the "Stressed receiver sensitivity (OMA_{outer}) (max)", "Stressed eye closure for PAM4 (SECQ)", and for 100GBASE-DR only, "SECQ – $10\log_{10}(C_{eq})$ (max)" are as given in Table 140–7.

140.8 Safety, installation, environment, and labeling

140.8.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

140.8.2 Laser safety

100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[233]

140.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

140.8.4 Environment

Normative specifications in this clause shall be met by a system integrating a 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

140.8.5 Electromagnetic emission

A system integrating a 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

[233]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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140.8.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

140.8.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 100GBASE-DR).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 140.8.2.

140.9 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 140–10.

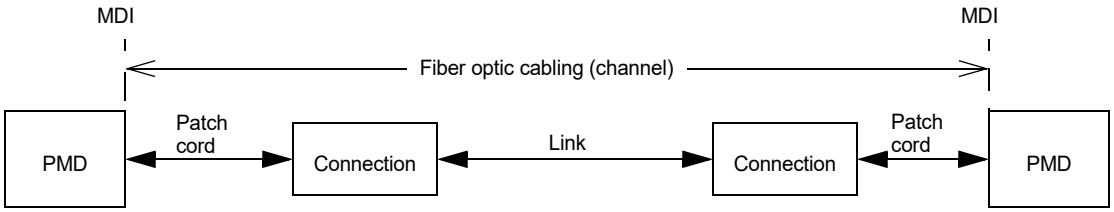

Figure 140–10—Fiber optic cabling model

The channel insertion loss is given in Table 140–12. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. The maximum value of channel insertion loss is dependent on the number and maximum value of the discrete reflectances within the channel as given in Table 140–13. Discrete reflectances below –55 dB may be ignored when determining the supported channel insertion loss. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 140–12—Fiber optic cabling (channel) characteristics

Description	100GBASE-DR	100GBASE-FR1	100GBASE-LR1	Unit
Operating distance (max)	500	2 000	10 000	m
Channel insertion loss[a, b] (max)	See Table 140–13	4	6.3	dB
Channel insertion loss (min)	0	0	0	dB
Positive dispersion[b] (max)	0.8	3.2	16	ps/nm
Negative dispersion[b] (min)	–0.93	–3.7	–18.6	ps/nm
DGD_max[c]	2.24	2.3	5	ps
Optical return loss (min)	27	25	22	dB

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[a] These channel insertion loss values include cable, connectors, and splices.
[b] Over the wavelength range 1304.5 nm to 1317.5 nm
[c] Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

Table 140–13—100GBASE-DR maximum channel insertion loss versus number of discrete reflectances

Maximum channel insertion loss (dB)		Number of discrete reflectances > –55 dB and ≤ –45 dB								
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Number of discrete reflectances > –45 dB and ≤ –35 dB	**0**	3	3	3	3	3	3	3	3	3
	1	3	3	3	3	3	3	3	3	3
	2	3	3	3	2.9	2.9	2.9	2.9	2.9	2.9
	3	2.9	2.9	2.9	2.9	2.9	2.8	2.8	2.8	—[a]
	4	2.8	2.8	2.8	2.8	2.7	2.7	2.7	—[a]	—[a]
	5	2.8	2.8	2.7	2.7	2.7	2.6	—[a]	—[a]	—[a]
	6	2.6	2.6	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]

[a]The indicated combination of reflectances does not provide a supported maximum channel insertion loss.

140.10 Characteristics of the fiber optic cabling (channel)

The 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 fiber optic cabling shall meet the specifications defined in Table 140–14. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

140.10.1 Optical fiber cable

The fiber optic cable requirements are satisfied by cables containing IEC 60793-2-50 type B1.1 (dispersion unshifted single-mode), type B1.3 (low water peak single-mode), or type B6_a (bend insensitive) fibers or the requirements in Table 140–14 where they differ.

Table 140–14—Optical fiber and cable characteristics

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.43[a] or 0.5[b]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \leq \lambda_0 \leq 1324$	nm
Dispersion slope (max) (S_0)	0.093	ps/nm^2 km

[a] The 0.43 dB/km at 1304.5 nm attenuation for optical fiber cables is derived from Appendix I of ITU-T G.695.
[b]The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3. Using 0.5 dB/km may not support operation over 10 km for 100GBASE-LR1.

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140.10.2 Optical fiber connection

An optical fiber connection, as shown in Figure 140–10, consists of a mated pair of optical connectors.

140.10.2.1 Connection insertion loss

For 100GBASE-DR, the maximum link distance is based on an allocation of 2.75 dB total connection and splice loss. For example, this allocation supports five connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 140–12 are met.

For 100GBASE-FR1, the maximum link distance is based on an allocation of 3 dB total connection and splice loss. For example, this allocation supports six connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 140–12 are met.

For 100GBASE-LR1, the maximum link distance is based on an allocation of 2 dB total connection and splice loss. For example, this allocation supports four connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 140–12 are met.

140.10.2.2 Maximum discrete reflectance

For 100GBASE-DR, the maximum discrete reflectance shall be less or equal than –35 dB. The number of maximum discrete reflectances in the ranges, > –45 dB and ≤ –35 dB, and, > –55 dB and ≤ –45 dB, is limited to the numbers given in Table 140–13 in relation to the maximum channel insertion loss.

For 100GBASE-FR1 and 100GBASE-LR1, the maximum value for each discrete reflectance shall be less than or equal to the value shown in Table 140–15 corresponding to the number of discrete reflectances above –55 dB within the channel. For numbers of discrete reflectances in between two numbers shown in the table, the lower of the two corresponding maximum discrete reflectance values applies.

Table 140–15—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance		Unit
	100GBASE-FR1	100GBASE-LR1	
1	–25	–22	dB
2	–31	–29	dB
4	–35	–33	dB
6	–38	–35	dB
8	–40	–37	dB
10	–41	–39	dB

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140.10.3 Medium Dependent Interface (MDI)

The 100GBASE-DR, 100GBASE-FR1, or 100GBASE-LR1 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 140–10). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

For 100GBASE-DR, when the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-021-2. For 100GBASE-FR1 and 100GBASE-LR1, when the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 140.5.1, not at the MDI.

140.11 Interoperation between 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1

The 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1 PMDs can interoperate with each other as described here.

140.11.1 Interoperation between 100GBASE-FR1 and 100GBASE-DR

The 100GBASE-FR1 and 100GBASE-DR PMDs can interoperate with each other provided that the fiber optic cabling (channel) characteristics for 100GBASE-DR (see 140.10 and Table 140–13) are met and the 100GBASE-FR1 transmitter average power is greater than or equal to the value for average launch power (min) for 100GBASE-DR in Table 140–6.

140.11.2 Interoperation between 100GBASE-LR1 and 100GBASE-DR

The 100GBASE-LR1 and 100GBASE-DR PMDs can interoperate with each other provided that the fiber optic cabling (channel) characteristics for 100GBASE-DR (see 140.10 and Table 140–13) are met, with the exception of the maximum and minimum channel insertion loss values, which are given in Table 140–16 for the two link directions separately. Attenuators may be used to achieve the required losses.

Table 140–16—Channel insertion loss for interoperation between 100GBASE-LR1 and 100GBASE-DR

Direction	Min loss	Max loss	Unit
100GBASE-LR1 transmitter to 100GBASE-DR receiver	0.8	4	dB
100GBASE-DR transmitter to 100GBASE-LR1 receiver	0	5.2	dB

140.11.3 Interoperation between 100GBASE-LR1 and 100GBASE-FR1

The 100GBASE-LR1 and 100GBASE-FR1 PMDs can interoperate with each other provided that the fiber optic cabling (channel) characteristics for 100GBASE-FR1 (see 140.10) are met, with the exception of the

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maximum and minimum channel insertion loss values, which are given in Table 140–17 for the two link directions separately. Attenuators may be used to achieve the required losses.

Table 140–17—Channel insertion loss for interoperation between 100GBASE-LR1 and 100GBASE-FR1

Direction	Min loss	Max loss	Unit
100GBASE-LR1 transmitter to 100GBASE-FR1 receiver	0.8	5.2	dB
100GBASE-FR1 transmitter to 100GBASE-LR1 receiver	0	5.1	dB

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140.12 Protocol implementation conformance statement (PICS) proforma for Clause 140, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1, 100GBASE-FR1, and 100GBASE-LR1[234]

140.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 140, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1, 100GBASE-FR1, and 100GBASE-LR1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

140.12.2 Identification

140.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

140.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 140, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1, 100GBASE-FR1, and 100GBASE-LR1
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[234]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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140.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*DR	100GBASE-DR	140.6	Device supports requirements for 100GBASE-DR PHY	O.1	Yes [ ] No [ ]
*FR1	100GBASE-FR1	140.6	Device supports requirements for 100GBASE-FR1 PHY	O.1	Yes [ ] No [ ]
*LR1	100GBASE-LR1	140.6	Device supports requirements for 100GBASE-LR1 PHY	O.1	Yes [ ] No [ ]
*INS	Installation / cable	140.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	140.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	140.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	140.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	140.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	140.4	Registers and interface supported	O	Yes [ ] No [ ]

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140.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR, 100GBASE-FR1, and 100GBASE-LR1, 100GBASE-FR1, and 100GBASE-LR1

140.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 100GBASE-R PCS and PMA	140.1		M	Yes [ ]
F2	Integration with management functions	140.1		O	Yes [ ] No [ ]
F3	Bit error ratio	140.1.1	Meets the BER specified in 140.1.1	M	Yes [ ]
F4	Transmit function	140.5.2	Conveys symbols from PMD service interface to MDI	M	Yes [ ]
F5	Mapping between optical signal and logical signal for transmitter	140.5.2	Optical power levels from lowest to highest correspond to tx_symbol values zero, one, two, and three, respectively	M	Yes [ ]
F6	Receive function	140.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]
F7	Conversion of optical signal to electrical signal	140.5.3	For delivery to the PMD service interface	M	Yes [ ]
F8	Mapping between optical signal and logical signal for receiver	140.5.3	Optical power levels from lowest to highest correspond to rx_symbol values zero, one, two, and three, respectively	M	Yes [ ]
F9	Global Signal Detect function	140.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F10	Global Signal Detect behavior	140.5.4	SIGNAL_DETECT is a global indicator of the presence of an optical signal	M	Yes [ ]
F11	PMD reset function	140.5.5	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

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140.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	140.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	140.5.6	Disables the optical transmitter with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD_fault function	140.5.7	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD_transmit_fault function	140.5.8	Sets PMD_transmit_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_receive_fault function	140.5.9	Sets PMD_receive_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]

140.12.4.3 PMD to MDI optical specifications for 100GBASE-DR

Item	Feature	Subclause	Value/Comment	Status	Support
DR1	Transmitter meets specifications in Table 140–6	140.6.1	Per definitions in 140.7	DR:M	Yes [ ] N/A [ ]
DR2	Receiver meets specifications in Table 140–7	140.6.2	Per definitions in 140.7	DR:M	Yes [ ] N/A [ ]

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140.12.4.4 PMD to MDI optical specifications for 100GBASE-FR1

Item	Feature	Subclause	Value/Comment	Status	Support
FR1	Transmitter meets specifications in Table 140–6	140.6.1	Per definitions in 140.7	FR1:M	Yes [ ] N/A [ ]
FR2	Receiver meets specifications in Table 140–7	140.6.2	Per definitions in 140.7	FR1:M	Yes [ ] N/A [ ]

140.12.4.5 PMD to MDI optical specifications for 100GBASE-LR1

Item	Feature	Subclause	Value/Comment	Status	Support
LR1	Transmitter meets specifications in Table 140–6	140.6.1	Per definitions in 140.7	LR1:M	Yes [ ] N/A [ ]
LR2	Receiver meets specifications in Table 140–7	140.6.2	Per definitions in 140.7	LR1:M	Yes [ ] N/A [ ]

140.12.4.6 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	140.7	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and SMSR	140.7.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	140.7.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA measurements	140.7.4		M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	140.7.5		M	Yes [ ]
OM6	Transmitter eye closure for PAM4 (TECQ)	140.7.6		FR1:M LR1:M	Yes [ ] N/A [ ]
OM7	Over/under-shoot	140.7.7		FR1:M LR1:M	Yes [ ] N/A [ ]
OM8	Transmitter power excursion	140.7.8		FR1:M LR1:M	Yes [ ] N/A [ ]
OM9	Extinction ratio	140.7.9		M	Yes [ ]
OM10	Transmitter transition time	140.7.10		M	Yes [ ]
OM11	Relative intensity noise	140.7.11		M	Yes [ ]
OM12	Receiver sensitivity	140.7.12		FR1:M LR1:M	Yes [ ] N/A [ ]
OM13	Stressed receiver sensitivity	140.7.13		M	Yes [ ]

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140.12.4.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	140.8.1	Conforms to J.2	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	140.8.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	140.8.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

140.12.4.8 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	140.10	Meets requirements specified in 140.10.2.2	INS:M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	140.10.2.2	Meets requirements specified in Table 140–13	INS:M	Yes [ ] N/A [ ]
OC3	MDI Requirements	140.10.3	Meets IEC 61753-1 and IEC 61753-021-2	FR1:M LR1:M	Yes [ ] N/A [ ]

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141. Physical Medium Dependent (PMD) sublayer and medium for Nx25G-EPON passive optical networks

141.1 Overview

This clause describes the Physical Medium Dependent (PMD) sublayer for Nx25G Ethernet passive optical networks (Nx25G-EPON) operating at a MAC data rate of 25 Gb/s or 50 Gb/s in the downstream direction and a MAC data rate of 10 Gb/s, 25 Gb/s, or 50 Gb/s in the upstream direction. These PMDs are collectively referred to by the term Nx25G-EPON. All Nx25G-EPON PMDs supporting the downstream MAC data rate of 50 Gb/s are collectively referred to as 50G-EPON PMDs while Nx25G-EPON PMDs supporting the downstream MAC data rate of 25 Gb/s are collectively referred to as 25G-EPON PMDs.

141.1.1 Terminology

Nx25G-EPON operates over a point-to-multipoint (P2MP) topology, also called a tree or trunk-and-branch topology. The device connected at the root of the tree is called an optical line terminal (OLT) and the devices connected as the leaves are referred to as optical network units (ONUs). The direction of transmission from the OLT to ONUs is referred to as the downstream direction, while the direction of transmission from the ONU to the OLT is referred to as the upstream direction.

141.1.2 Positioning of the PMD sublayer within the IEEE 802.3 architecture

Figure 141–1 depicts the relationships of Nx25G-EPON PMD sublayers (shown hatched) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

141.1.3 PHY link types

Characteristics of Nx25G-EPON PHY link types are summarized in Table 141–1 through Table 141–5. The indicated characteristics of PHY link types are the results of specific pairings of an OLT PMD and an ONU PMD. The supported PMD pairs are specified in Table 141–8 and Table 141–9. Nx25G-EPON PHY link types supporting 50 Gb/s use wavelength division multiplexing on two wavelengths and hence two wavelengths are listed for these links in Table 141–1 through Table 141–5.

Table 141–1—PHY links supporting 25 Gb/s downstream and 10 Gb/s upstream

Description	25/10-PQ20G	25/10-PQ20X	25/10-PQ30G	25/10-PQ30X	Units
Number of fibers	1				—
Nominal downstream line rate	25.78125				GBd
Nominal upstream line rate	10.3125				GBd
Downstream wavelength	1358 ± 2				nm
Upstream wavelength	1270 ± 10	1300 ± 10	1270 ± 10	1300 ± 10	nm
Maximum reach	≥20				km
Maximum channel insertion loss	24		29		dB
Minimum channel insertion loss	10		15		dB
Coexistent PON technology	GPON	10G-EPON	GPON	10G-EPON	—

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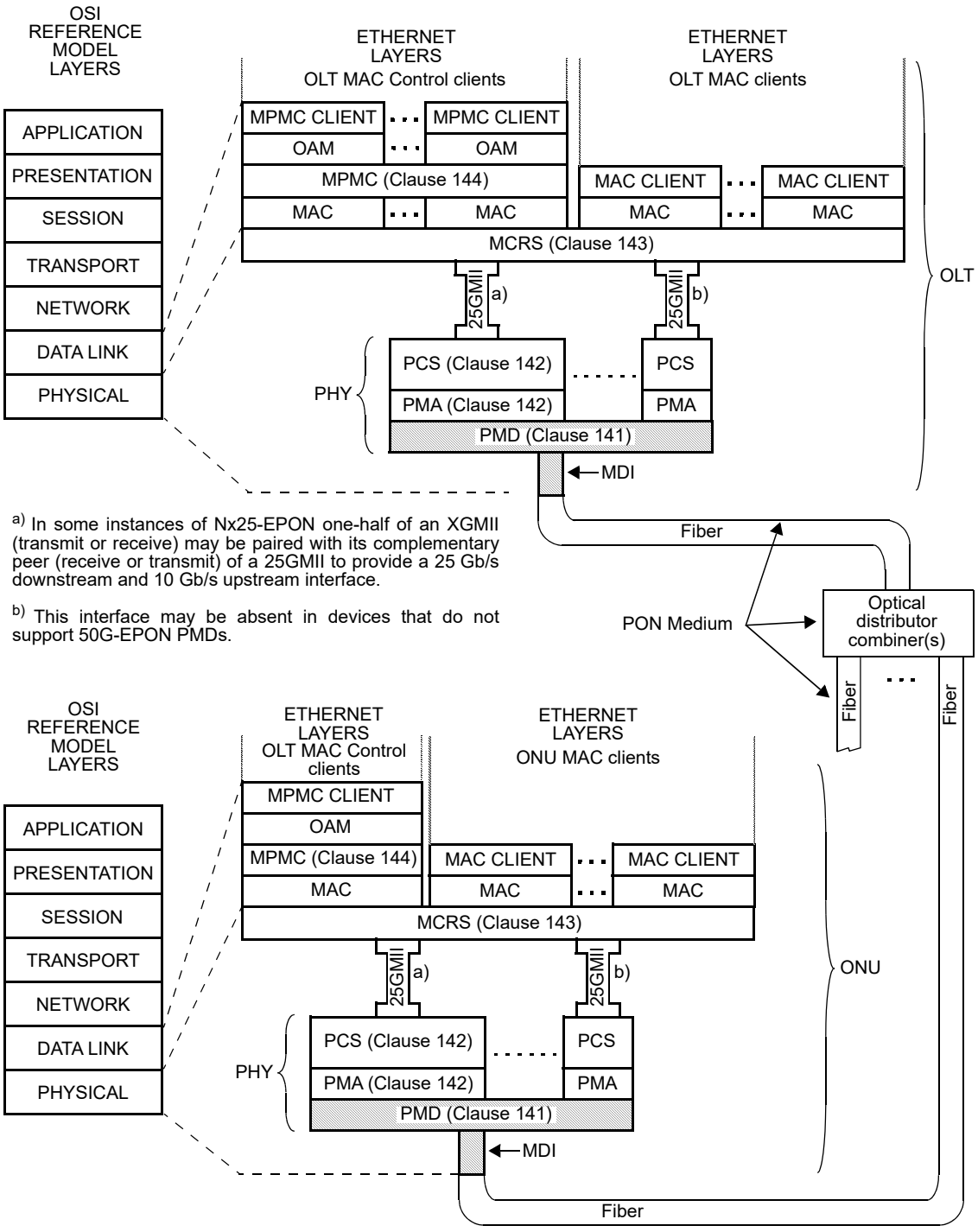

Figure 141–1—Relationship of Nx25G-EPON P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

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Table 141–2—PHY links supporting 25 Gb/s downstream and 25 Gb/s upstream

Description	25/25-PQ20G	25/25-PQ20X	25/25-PQ30G	25/25-PQ30X	Units
Number of fibers	1				—
Nominal downstream line rate	25.78125				GBd
Nominal upstream line rate	25.78125				GBd
Downstream wavelength	1358 ± 2				nm
Upstream wavelength	1270 ± 10	1300 ± 10	1270 ± 10	1300 ± 10	nm
Maximum reach	≥20				km
Maximum channel insertion loss	24		29		dB
Minimum channel insertion loss	10		15		dB
Coexistent PON technology	GPON	10G-EPON	GPON	10G-EPON	—

Table 141–3—PHY links supporting 50 Gb/s downstream and 10 Gb/s upstream

Description	50/10-PQ20G	50/10-PQ20X	50/10-PQ30G	50/10-PQ30X	Units
Number of fibers	1				—
Nominal downstream line rate	25.78125				GBd
Nominal upstream line rate	10.3125				GBd
Downstream wavelength	1358 ± 2 1342 ± 2				nm nm
Upstream wavelength	1270 ± 10	1300 ± 10	1270 ± 10	1300 ± 10	nm
Maximum reach	≥20				km
Maximum channel insertion loss	24		29		dB
Minimum channel insertion loss	10		15		dB
Coexistent PON technology	GPON	10G-EPON	GPON	10G-EPON	—

Table 141–4—PHY links supporting 50 Gb/s downstream and 25 Gb/s upstream

Description	50/25-PQ20G	50/25-PQ20X	50/25-PQ30G	50/25-PQ30X	Units
Number of fibers	1				—
Nominal downstream line rate	25.78125				GBd
Nominal upstream line rate	25.78125				GBd
Downstream wavelength	1358 ± 2 1342 ± 2				nm nm
Upstream wavelength	1270 ± 10	1300 ± 10	1270 ± 10	1300 ± 10	nm
Maximum reach	≥20				km
Maximum channel insertion loss	24		29		dB
Minimum channel insertion loss	10		15		dB
Coexistent PON technology	GPON	10G-EPON	GPON	10G-EPON	—

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Table 141–5—PHY links supporting 50 Gb/s downstream and 50 Gb/s upstream

Description	50/50-PQ20G	50/50-PQ20X	50/50-PQ30G	50/50-PQ30X	Units
Number of fibers	1				—
Nominal downstream line rate	25.78125				GBd
Nominal upstream line rate	25.78125				GBd
Downstream wavelength	1358 ± 2 1342 ± 2				nm nm
Upstream wavelength	1270 ± 10 1300 ± 10	1300 ± 10 1320 ± 2	1270 ± 10 1300 ± 10	1300 ± 10 1320 ± 2	nm nm
Maximum reach	≥20				km
Maximum channel insertion loss	24		29		dB
Minimum channel insertion loss	10		15		dB
Coexistent PON technology	N/A	10G-EPON	N/A	10G-EPON	—

141.2 PMD nomenclature

141.2.1 Introduction

Nx25G-EPON PMDs are classified based on transmit and receive rate, coexistence type, transmission direction, and power level.

141.2.2 PMD rate classes

Nx25G-EPON PMDs defined in this clause fall into several rate classes depending on the upstream and downstream aggregate rate supported. Possible downstream rates are either 25 Gb/s or 50 Gb/s. Possible upstream rates are 10 Gb/s, 25 Gb/s, or 50 Gb/s. The rate(s) at which a PMD operates is indicated in the PMD name.

141.2.3 PMD coexistence classes

Nx25G-EPON PMDs defined in this clause support WDM coexistence with 10G-EPON or GPON. PMDs coexisting with 10G-EPON are denoted with the letter X in the PMD name while PMDs coexisting with GPON are denoted with the letter G.

141.2.4 PMD transmission direction classes

Nx25G-EPON PMDs defined in this clause are defined for either the OLT and face the downstream direction or for the ONU and face the upstream direction. OLT PMDs are denoted with the letter D in the PMD name while ONU PMDs are denoted with the letter U.

141.2.5 PMD power classes

Nx25G-EPON PMDs defined in this clause are defined as being in one of two power classes (a power class is a differentiator for PMD specifications based of their launch powers and sensitivities); the medium or the high power budget class:

— The medium PMD power class supports a P2MP media channel insertion loss of ≤ 24 dB e.g., a PON with a split ratio of 1:16 and the distance of 20 km or a PON with a split ratio of 1:32 and the distance of 10 km.

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— The high PMD power class supports a P2MP media channel insertion loss of ≤ 29 dB e.g., a PON with a split ratio of 1:32 and the distance of 20 km.

The medium PMD power class is indicated in the PMD name with the numeral 2 while the high PMD power class is indicated with the numeral 3.

141.2.6 PMD naming

Nx25G-EPON PMD naming conforms to Table 141–6.

Table 141–6—PMD naming

Naming template	r_1/r_2GBASE-PQc-db	
Naming element	**Description**	**Allowed values**
r_1	PMD downstream rate class (see 141.2.2)	25, 50
r_2[a]	PMD upstream rate class (see 141.2.2)	10, 25, 50
G	PMDs operate at Gb/s rates	
BASE		
P	PMD for PON (P2MP media)	
Q	256B/257B line code	
c	Coexistence class (see 141.2.3)	G, X
d	Transmission direction class (see 141.2.4)	D, U
b	Power class (see 141.2.5)	2, 3

[a]If r_1 is equal to r_2 (i.e., symmetric-data rate PMDs), r_2 is omitted.

141.2.7 Supported combinations of OLT and ONU PMDs

The PHY link power budget (a power budget is a characteristic of a link type and depends on the paired PMDs' transmitter launch powers and receiver sensitivities) is determined by the PMDs located at the ends of the physical media. This subclause describes how OLT (D type) and ONU (U type) PMDs may be combined to achieve the power budgets listed in Table 141–1 through Table 141–5. Table 141–7 shows the list of all supported PMD types. Connection between G and X coexistence type PMDs is not supported, e.g., 25/10GBASE-PQG-D2 OLT PMD is not interoperable with 25/10GBASE-PQX-U2 due to non-overlapping OLT receiver sensitivity window and ONU transmitter wavelength range.

Table 141–7—List of supported PMD types

Upstream/ Downstream MAC data rate	**Downstream wavelengths[a]**	**Upstream wavelengths[b]**	**OLT PMDs**	**ONU PMDs**
25G/10G	DW0	UW0	25/10GBASE-PQG-D2 25/10GBASE-PQG-D3	25/10GBASE-PQG-U2 25/10GBASE-PQG-U3
	DW0	UW1	25/10GBASE-PQX-D2 25/10GBASE-PQX-D3	25/10GBASE-PQX-U2 25/10GBASE-PQX-U3
25G/25G	DW0	UW0	25GBASE-PQG-D2 25GBASE-PQG-D3	25GBASE-PQG-U2 25GBASE-PQG-U3
	DW0	UW1	25GBASE-PQX-D2 25GBASE-PQX-D3	25GBASE-PQX-U2 25GBASE-PQX-U3

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Table 141–7—List of supported PMD types *(continued)*

Upstream/ Downstream MAC data rate	Downstream wavelengths[a]	Upstream wavelengths[b]	OLT PMDs	ONU PMDs
50G/10G	DW0 + DW1	UW0	50/10GBASE-PQG-D2 50/10GBASE-PQG-D3	50/10GBASE-PQG-U2 50/10GBASE-PQG-U3
	DW0 + DW1	UW1	50/10GBASE-PQX-D2 50/10GBASE-PQX-D3	50/10GBASE-PQX-U2 50/10GBASE-PQX-U3
50G/25G	DW0 + DW1	UW0	50/25GBASE-PQG-D2 50/25GBASE-PQG-D3	50/25GBASE-PQG-U2 50/25GBASE-PQG-U3
	DW0 + DW1	UW1	50/25GBASE-PQX-D2 50/25GBASE-PQX-D3	50/25GBASE-PQX-U2 50/25GBASE-PQX-U3
50G/50G	DW0 + DW1	UW0 + UW1	50GBASE-PQG-D2 50GBASE-PQG-D3	50GBASE-PQG-U2 50GBASE-PQG-U3
	DW0 + DW1	UW1 + UW2	50GBASE-PQX-D2 50GBASE-PQX-D3	50GBASE-PQX-U2 50GBASE-PQX-U3

[a]Downstream wavelengths are defined in Table 141–13.
[b]Upstream wavelengths are defined in Table 141–14.

141.2.7.1 PHY Links supporting medium power budget

Table 141–8 illustrates pairings of OLT PMDs with ONU PMDs to achieve the medium power budgets as shown in Table 141–1 through Table 141–5.

Table 141–8—Supported combinations of OLT and ONU PMDs and the resulting PHY link types, medium power budget[a]

		ONU PMD				
		25/10GBASE-PQ*-U2	**50/10GBASE-PQ*-U2**	**25GBASE-PQ*-U2**	**50/25GBASE-PQ*-U2**	**50GBASE-PQ*-U2**
OLT PMD	**25/10GBASE-PQ*-D2**	25/10-PQ20	25/10-PQ20	N/A		
	50/10GBASE-PQ*-D2	25/10-PQ20	50/10-PQ20			
	25GBASE-PQ*-D2	N/A		25/25-PQ20	25/25-PQ20	25/25-PQ20
	50/25GBASE-PQ*-D2			25/25-PQ20	50/25-PQ20	50/25-PQ20
	50GBASE-PQ*-D2			25/25-PQ20	50/25-PQ20	50/50-PQ20

[a](*) - On an ODN, OLT and ONU PMDs support the same coexistence mode, either X or G.

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141.2.7.2 PHY Links supporting high power budget

Table 141–9 illustrates pairings of OLT PMDs with ONU PMDs to achieve the high power budgets as shown in Table 141–1 through Table 141–5.

Table 141–9—Supported combinations of OLT and ONU PMDs and the resulting PHY link types, high power budget[a]

		ONU PMD				
		25/10GBASE-PQ*-U3	**50/10GBASE-PQ*-U3**	**25GBASE-PQ*-U3**	**50/25GBASE-PQ*-U3**	**50GBASE-PQ*-U3**
OLT PMD	**25/10GBASE-PQ*-D3**	25/10-PQ30	25/10-PQ30	N/A		
	50/10GBASE-PQ*-D3	25/10-PQ30	50/10-PQ30			
	25GBASE-PQ*-D3	N/A		25/25-PQ30	25/25-PQ30	25/25-PQ30
	50/25GBASE-PQ*-D3			25/25-PQ30	50/25-PQ30	50/25-PQ30
	50GBASE-PQ*-D3			25/25-PQ30	50/25-PQ30	50/50-PQ30

[a](*) - On an ODN, OLT and ONU PMDs support the same coexistence mode, either X or G.

141.3 PMD functional specifications

The Nx25G-EPON PMDs perform the transmit and receive functions that convey data between the PMD service interface and the MDI.

141.3.1 PMD service interface

The following specifies the services provided by Nx25G-EPON PMDs. These PMD sublayer service interfaces are described in an abstract manner and do not imply any particular implementation.

The PMD service interface supports the exchange of a continuous stream of bits between the PMA[*i*] and PMD entities. The PMD translates the serialized data received from the compatible PMA to and from signals suitable for the specified medium. The following primitives are defined:

— PMD_UNITDATA[*i*].request
— PMD_UNITDATA[*i*].indication
— PMD_SIGNAL[*i*].request
— PMD_SIGNAL[*i*].indication

where "[*i*]" represents the PMA Channel: 0 or 1.

141.3.1.1 Channel-to-wavelength mapping

An Nx25G-EPON PMD provides multiple instances of the PMD service interface that connect to multiple PMA channels (see 142.4.1). Within the PMD sublayer, each instance of the PMD service interface maps to a specific pair of wavelengths. This mapping is different for the two coexistence classes, and shall be as defined in Table 141–10 for the OLT and in Table 141–11 for the ONU.

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Table 141–10—OLT Channel-to-wavelength mapping

PMA channel	PMD service primitives	Wavelength (coexistence class G)	Wavelength (coexistence class X)
0	PMD_UNITDATA[0].request PMD_SIGNAL[0].request	DW0	DW0
	PMD_UNITDATA[0].indication PMD_SIGNAL[0].indication	UW0	UW1
1	PMD_UNITDATA[1].request PMD_SIGNAL[1].request	DW1	DW1
	PMD_UNITDATA[1].indication PMD_SIGNAL[1].indication	UW1	UW2

Table 141–11—ONU Channel-to-wavelength mapping

PMA channel	PMD service primitives	Wavelength (coexistence class G)	Wavelength (coexistence class X)
0	PMD_UNITDATA[0].request PMD_SIGNAL[0].request	UW0	UW1
	PMD_UNITDATA[0].indication PMD_SIGNAL[0].indication	DW0	DW0
1	PMD_UNITDATA[1].request PMD_SIGNAL[1].request	UW1	UW2
	PMD_UNITDATA[1].indication PMD_SIGNAL[1].indication	DW1	DW1

141.3.1.2 Delay constraints

The Nx25G-EPON PMD delay variation within the PMD shall be less than 0.25 EQT (see 1.4.313).

141.3.1.3 PMD_UNITDATA[*i*].request

This primitive defines the transfer of a serial data stream from the PMA defined in 142.4 to the PMD.

The semantics of the service primitive are PMD_UNITDATA[*i*].request(tx_bit) (where $i = 0$ or 1). The data conveyed by PMD_UNITDATA[*i*].request is a continuous stream of bits. The tx_bit parameter can take one of two values: ONE or ZERO. The PMA defined in 142.4 continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal signaling rate of 25.78125 GBd in the case of Nx25G-EPON OLT and ONU PMDs. The PMA defined in 142.4 continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal signaling rate of 10.3125 GBd in the case of 25/10G-EPON and 50/10G–EPON ONU PMDs. Upon the receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals at the MDI.

141.3.1.4 PMD_UNITDATA[*i*].indication

This primitive defines the transfer of data from the PMD to the PMA defined in 142.4.

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The semantics of the service primitive are PMD_UNITDATA[*i*].indication(rx_bit) (where *i* = 0 or 1). The data conveyed by PMD_UNITDATA[*i*].indication is a continuous stream of bits. The rx_bit parameter can take one of two values: ONE or ZERO. The PMD continuously sends a stream of bits to the PMA defined in 142.4 corresponding to the signals received from the MDI, at the nominal signaling rate of 25.78125 GBd in the case of Nx25G–EPON OLT and ONU PMDs or to the PMA defined in 142.4 at the nominal signaling rate of 10.3125 GBd in the case of 25/10G–EPON and 50/10G-EPON OLT PMDs.

141.3.1.5 PMD_SIGNAL[*i*].request

In the upstream direction, this primitive is generated by the PMA defined in 142.4 to turn on and off the transmitter according to the granted time. A signal for laser control is generated as described in 142.2.5.4.3 for the PCS defined in 142.2.

The semantics of the service primitive are PMD_SIGNAL[*i*].request(tx_enable) (where *i* = 0 or 1). The tx_enable parameter can take on one of two values: ENABLE or DISABLE, determining whether the PMD transmitter is on (enabled) or off (disabled). The PMA defined in 142.4 generates this primitive to indicate a change in the value of tx_enable. Upon the receipt of this primitive, the PMD turns the transmitter on or off as appropriate.

141.3.1.6 PMD_SIGNAL[*i*].indication

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI. The semantics of the service primitive are PMD_SIGNAL[*i*].indication(SIGNAL_DETECT) (where *i* = 0 or 1). The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting light at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA[*i*].indication(rx_bit) is undefined. The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT. If the MDIO interface is implemented, then PMD_global_signal_detect shall be continuously set to the value of SIGNAL_DETECT.

NOTE—SIGNAL_DETECT = OK does not guarantee that PMD_UNITDATA[*i*].indication(rx_bit) is known good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the specified bit error ratio. PMD_SIGNAL[*i*].indication(SIGNAL_DETECT) has different characteristics for upstream and downstream links, see 141.3.5.

141.3.2 PMD block diagram

The PMD sublayer is defined at the reference points shown in Figure 141–2 for Nx25G-EPON PMDs. For any indexed test point (e.g., TP1[*i*]), [*i*] indicates the channel index, where *i* = 0 or 1.

For Nx25G-EPON PMDs, test points TP1[*i*], TP2, TP3, and TP4[*i*] refer to the downstream channel, while test points TP5[*i*], TP6, TP7, and TP8[*i*] refer to the upstream channel. In the downstream channel, TP2 and TP3 are compliance points, while in the upstream channel TP6 and TP7 are compliance points. TP1[*i*], TP4[*i*], TP5[*i*], and TP8[*i*] are reference points for use by implementers, defined on a per-channel basis. The optical transmit signal is defined at the output end of a patch cord (TP2 for the downstream channel and TP6 for the upstream channel), between 2 m and 5 m in length, of a fiber type consistent with the link type connected to the transmitter. Unless specified otherwise, all transmitter measurements and tests defined in 141.7 are made at TP2 or TP6. The optical receive signal is defined at the output of the fiber optic cabling (TP3 for the downstream channel and TP7 for the upstream channel) connected to the receiver. Unless specified otherwise, all receiver measurements and tests defined in 141.7 are made at TP3 or TP7.

The electrical specifications of the PMD service interface (TP1[*i*] and TP4[*i*] for the downstream channel and TP5[*i*] and TP8[*i*] for the upstream channel) are not system compliance points (these are not readily testable in a system implementation).

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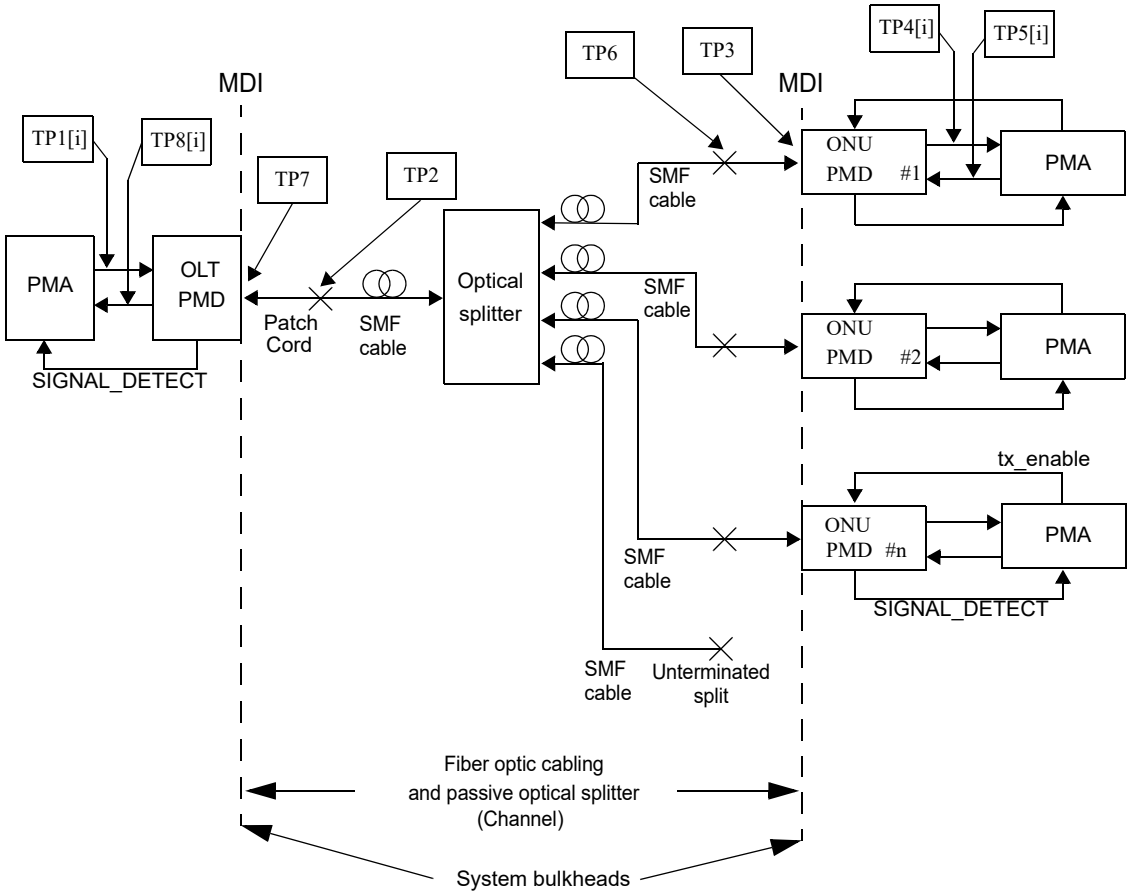

Figure 141–2—Nx25G-EPON PMD test points

141.3.3 PMD transmit function

The PMD transmit function shall convey the bits requested by the PMD service interface primitive PMD_UNITDATA[*i*].request(tx_bit) to the MDI according to the optical specifications in this clause. In the upstream direction, the flow of bits is interrupted according to PMD_SIGNAL[*i*].request(tx_enable). This implies three optical levels, 1, 0, and dark, the latter corresponding to the transmitter being in the OFF state. The highest optical power level shall correspond to tx_bit = ONE.

141.3.4 PMD receive function

The PMD receive function shall convey the bits received from the MDI according to the optical specifications in this clause to the PMD service interface using the primitive PMD_UNITDATA[*i*].indication(rx_bit). The higher optical power level shall correspond to rx_bit = ONE.

141.3.5 PMD signal detect function

141.3.5.1 ONU PMD signal detect

The PMD signal detect function for the continuous mode downstream signal shall report to the PMD service interface, using the primitive PMD_SIGNAL[*i*].indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL[*i*].indication is intended to be an indicator of the presence of the optical

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signal. The ONU PMD receiver is not required to verify whether a compliant Nx25G-EPON signal is being received.

141.3.5.2 OLT PMD signal detect

The response time for the PMD signal detect function for the burst mode upstream signal may be longer or shorter than a burst length; thus, it may not fulfill the traditional requirements placed on signal detect. PMD_SIGNAL.indication is intended to be an indicator of optical signal presence. The signal detect function in the OLT may be realized in the PMD or the PMA defined in 142.4. The OLT PMD receiver is not required to verify whether a compliant Nx25G-EPON signal is being received.

141.3.5.3 Nx25G-EPON signal detect functions

The value of the SIGNAL_DETECT parameter for Nx25G–EPON PMDs shall be generated according to the conditions defined in Table 141–12.

Table 141–12—SIGNAL_DETECT value definitions for Nx25G-EPON PMDs

PMD type	Receive conditions	SIGNAL_DETECT value
Nx25G-EPON PMD	Average input optical power ≤ Signal detect threshold (min) in Table 141–17 or Table 141–18 at the specified receiver wavelength, as applicable	FAIL
	Average input optical power ≥ Receive sensitivity (max) in Table 141–17 or Table 141–18 with a compliant signal input at the specified receiver wavelength, as applicable	OK
	All other conditions	Unspecified

141.4 Wavelength allocation

Downstream wavelength assignments are defined in Table 141–13. Upstream wavelength assignments are defined in Table 141–14.

Table 141–13—Downstream wavelength assignments

Wavelength name	Center wavelength (nm)	Wavelength range (nm)
DW0	1358	± 2
DW1	1342	± 2

Table 141–14—Upstream wavelength assignments

Wavelength name	Center wavelength (nm)	Wavelength range (nm)
UW0	1270	± 10
UW1	1300	± 10
UW2	1320	± 2

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141.5 PMD to MDI optical specifications for OLT PMDs

This subclause details the PMD to MDI optical specifications for OLT PMDs. Specifically, 141.5.1 defines the OLT transmit parameters, while 141.5.2 defines the OLT receive parameters.

The operating parameters for Nx25G-EPON PHY link types are defined in Table 141–1 through Table 141–5. An Nx25G-EPON compliant transceiver operates over the media meeting the dispersion shown in Table 141–23 according to the specifications described in 141.9. A transceiver that exceeds the maximum reach requirement while meeting all other optical specifications is considered compliant.

NOTE—The specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is defined in 58.7.6.

141.5.1 Transmitter optical specifications

A medium power class Nx25G-EPON OLT PMD transmitter shall comply with the parameters shown in Table 141–15. A high power class Nx25G-EPON OLT PMD transmitter shall comply with the parameters shown in Table 141–16.

141.5.2 Receiver optical specifications

A medium power class Nx25G-EPON OLT PMD receiver shall comply with the parameters shown in Table 141–17. A high power class Nx25G-EPON OLT PMD receiver shall comply with the parameters shown in Table 141–18.

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Table 141–15—OLT transmit characteristics, medium power class

Parameter	25/10GBASE-PQG-D2 25/10GBASE-PQX-D2 25GBASE-PQG-D2 25GBASE-PQX-D2	50/10GBASE-PQG-D2 50/10GBASE-PQX-D2 50/25GBASE-PQG-D2 50/25GBASE-PQX-D2 50GBASE-PQG-D2 50GBASE-PQX-D2	Unit
Signaling rate (range)	25.78125 ± 100 ppm		GBd
Channel wavelength ranges	1356 to 1360	1356 to 1360 1340 to 1344	nm
Side-mode suppression ratio (SMSR) (min)	30		dB
Total average launch power (max)	—	8	dBm
Average launch power, each channel (max)	5		dBm
Optical Modulation Amplitude (OMA), each channel (min)[a]	2.6		dBm
Difference in launch power between any two channels (OMA) (max)	—	3	dB
Launch power in OMA minus TDP, each channel (min)(see note) for extinction ratio ≥ 9 dB for extinction ratio < 9 dB	 2 2.1		 dBm dBm
Transmitter and dispersion penalty (TDP), each channel (max)	1.5		dB
Average launch power of OFF transmitter, each channel (max)	–39		dBm
Extinction ratio (min)	8		dB
$RIN_{15}OMA$ (max)	–128		dB/Hz
Optical return loss tolerance (max)	15		dB
Transmitter reflectance[b] (max)	–10		dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}[c]	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}		UI
NOTE—For reference, this implies that the minimum average launch power per channel at minimum extinction ratio and maximum TDP is 2 dBm. This minimum average launch power value is informative only.			

[a] Even if the TDP < 0.5 dB, the OMA (min) exceeds this value.
[b] Transmitter reflectance is defined looking into the transmitter.
[c] As defined in Figure 86–4.

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Table 141–16—OLT transmit characteristics, high power class

Parameter	25/10GBASE-PQG-D3 25/10GBASE-PQX-D3 25GBASE-PQG-D3 25GBASE-PQX-D3	50/10GBASE-PQG-D3 50/10GBASE-PQX-D3 50/25GBASE-PQG-D3 50/25GBASE-PQX-D3 50GBASE-PQX-D3 50GBASE-PQG-D3	Unit
Signaling rate (range)	25.78125 ± 100 ppm		GBd
Channel wavelength ranges	1356 to 1360	1356 to 1360 1340 to 1344	nm
Side-mode suppression ratio (SMSR) (min)	30		dB
Total average launch power (max)	—	10.8	dBm
Average launch power, each channel (max)	7.8		dBm
Optical Modulation Amplitude (OMA), each channel (min)[a]	4.9		dBm
Difference in launch power between any two channels (OMA) (max)	—	3	dB
Launch power in OMA minus TDP, each channel (min)(see note) for extinction ratio ≥ 9 dB for extinction ratio < 9 dB	 4.8 4.9		 dBm dBm
Transmitter and dispersion penalty (TDP), each channel (max)	1.5		dB
Average launch power of OFF transmitter, each channel (max)	–39		dBm
Extinction ratio (min)	8		dB
$RIN_{15}OMA$ (max)	–128		dB/Hz
Optical return loss tolerance (max)	15		dB
Transmitter reflectance[b] (max)	–10		dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}[c]	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}		UI
NOTE—For reference, this implies that the minimum average launch power per channel at minimum extinction ratio and maximum TDP is 4.8 dBm. This minimum average launch power value is informative only.			

[a] Even if the TDP < 0.5 dB, the OMA (min) exceeds this value.
[b] Transmitter reflectance is defined looking into the transmitter.
[c] As defined in Figure 86–4.

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Table 141–17—OLT receive characteristics, medium power class

Parameter	25GBASE-PQG-D2 50/25GBASE-PQG-D2	25GBASE-PQX-D2 50/25GBASE-PQX-D2	50GBASE-PQG-D2	50GBASE-PQX-D2	25/10GBASE-PQG-D2 50/10GBASE-PQG-D2	25/10GBASE-PQX-D2 50/10GBASE-PQX-D2	Unit
Signaling rate (range)	25.78125 ± 100 ppm				See Table 75–6[a]		GBd
Channel wavelengths (range)	1260 to 1280	1290 to 1310	1260 to 1280 1290 to 1310	1290 to 1310 1318 to 1322	See Table 75–6[a]	1290 to 1310	nm
Bit error ratio (max)[b]	10^{-2}						—
Damage threshold[c]	–2				See Table 75–6[a]		dBm
Average receive power, each channel (max)	–3						dBm
Receiver reflectance (max)	–12						dB
Receiver sensitivity (OMA), each channel[d] (max)(see note)	–22.7						dBm
Signal detect threshold, each channel (min)	–40						dBm
Stressed receiver sensitivity (OMA), each channel[e] (max)	–21.2						dBm
Receiver settling time (max)	800						ns
Conditions of stressed receiver sensitivity test							
Vertical eye closure penalty,[f] each channel	2				See Table 75–6[a]		dB
Stressed eye J2 Jitter,[e,f] each channel	0.3				—		UI
Stressed eye J9 Jitter,[e,f] each channel	0.47				—		UI
NOTE—For reference, this implies that the maximum average power unstressed receiver sensitivity measured with an ideal transmitter signal at minimum extinction ratio is –22 dBm. This value is informative only.							

[a] Individual 10G-EPON PMD parameters are reused without change at a higher pre-FEC bit error ratio shown in Table 141–17.
[b] The BER of 10^{-12} is achieved by the utilization of FEC as described in 142.2.4.1.
[c] The receiver tolerates, without damage, continuous exposure to an optical input signal having this average power level.
[d] Receiver sensitivity (OMA), each channel (max) is optional and is defined for a transmitter with VECP = 0.5 dB.
[e] Measured with conformance test signal at TP3 (see 141.7.11) for BER = 10^{-2}.
[f] Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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Table 141–18—OLT receive characteristics, high power class

Parameter	25GBASE-PQG-D3 50/25GBASE-PQG-D3	25GBASE-PQX-D3 50/25GBASE-PQX-D3	50GBASE-PQG-D3	50GBASE-PQX-D3	25/10GBASE-PQG-D3 50/10GBASE-PQG-D3	25/10GBASE-PQX-D3 50/10GBASE-PQX-D3	Unit
Signaling rate (range)	25.78125 ± 100 ppm				See Table 75–6[a]		GBd
Channel wavelength ranges	1260 to 1280	1290 to 1310	1260 to 1280 1290 to 1310	1290 to 1310 1318 to 1322	See Table 75–6[a]	1290 to 1310	nm
Bit error ratio (max)[b]	10^{-2}						—
Damage threshold[c]	–5				See Table 75–6[a]		dBm
Average receive power, each channel (max)	–6				—		dBm
Receiver reflectance (max)	–12				See Table 75–6[a]		dB
Receiver sensitivity (OMA), each channel[d] (max)(see note)	–24.3						dBm
Signal detect threshold, each channel (min)	–40						dBm
Stressed receiver sensitivity (OMA), each channel[e] (max)	–22.8						dBm
Receiver settling time (max)	800						ns
Conditions of stressed receiver sensitivity test							
Vertical eye closure penalty,[f] each channel	2				See Table 75–6[a]		dB
Stressed eye J2 Jitter,[e,f] each channel	0.3				—		UI
Stressed eye J9 Jitter,[e,f] each channel	0.47				—		UI
NOTE—For reference, this implies that the maximum average power unstressed receiver sensitivity measured with an ideal transmitter signal at minimum extinction ratio is –25 dBm. This value is informative only.							

[a] Individual 10G-EPON PMD parameters are reused without change at a higher pre-FEC bit error ratio shown in Table 141–17.
[b] The BER of 10^{-12} is achieved by the utilization of FEC as described in 142.2.4.1.
[c] The receiver tolerates, without damage, continuous exposure to an optical input signal having this average power level. Direct ONU–OLT connection may result in damage of the receiver.
[d] Receiver sensitivity (OMA) is measured with a signal with VECP = 0.5 dB and is optional.
[e] Measured with conformance test signal at TP7 (see 141.7.11) for BER = 10^{-2}.
[f] Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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141.6 PMD to MDI optical specifications for ONU PMDs

This subclause details the PMD to MDI optical specifications for ONU PMDs. Specifically, 141.6.1 defines the ONU transmit parameters, while 141.6.2 defines the ONU receive parameters.

The operating parameters for Nx25G-EPON PHY link types are defined in Table 141–1 through Table 141–5. An Nx25G-EPON compliant transceiver operates over the media meeting the dispersion shown in Table 141–23 according to the specifications described in 141.9. A transceiver that exceeds the maximum reach requirement while meeting all other optical specifications is considered compliant.

NOTE—The specifications for OMA have been derived from extinction ratio and average launch power (minimum) or receiver sensitivity (maximum). The calculation is defined in 58.7.6.

141.6.1 Transmitter optical specifications

A medium power class Nx25G-EPON ONU PMD transmitter shall comply with the parameters shown in Table 141–19. A high power class Nx25G-EPON ONU PMD transmitter shall comply with the parameters shown in Table 141–20.

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Table 141–19—ONU transmit characteristics, medium power class

Parameter	25GBASE-PQG-U2 50/25GBASE-PQG-U2	25GBASE-PQX-U2 50/25GBASE-PQX-U2	50GBASE-PQG-U2	50GBASE-PQX-U2	25/10GBASE-PQG-U2 50/10GBASE-PQG-U2 25/10GBASE-PQX-U2 50/10GBASE-PQX-U2	Unit
Signaling rate (range)	25.78125 ± 100 ppm				See Table 75–8	GBd
Channel wavelengths (range)	1260 to 1280	1290 to 1310	1260 to 1280 1290 to 1310	1290 to 1310 1318 to 1322		nm
Side-mode suppression ratio (SMSR) (min)	30					dB
Total average launch power (max)	—		10			dBm
Average launch power, each channel (max)	7					dBm
Optical Modulation Amplitude (OMA), each channel (min)[a]	1.3					dBm
Difference in launch power between any two channels (OMA) (max)	—		3			dB
Launch power in OMA minus TDP, each channel (min)(see note) for extinction ratio ≥ 5.5 dB for extinction ratio ≥ 4.5 dB for extinction ratio < 4.5 dB	0.2 0.5 0.8					dBm
Transmitter and dispersion penalty (TDP), each channel (max)	2					dB
Average launch power of OFF transmitter, each channel (max)	–45					dBm
Extinction ratio (min)	3.5					dB
$RIN_{15}OMA$ (max)	–128					dB/Hz
Optical return loss tolerance (max)	15					dB
Transmitter reflectance[b] (max)	–10					dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}[c]	{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}					UI
Turn-on time (max)	128					ns
Turn-off time (max)	128					ns
NOTE—For reference, this implies that the minimum average launch power per channel at minimum extinction ratio and maximum TDP is 4 dBm. This minimum average launch power value is informative only.						

[a] Even if the TDP < 0.5 dB, the OMA (min) exceeds this value.
[b] Transmitter reflectance is defined looking into the transmitter.
[c] As defined in Figure 86–4.

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Table 141–20—ONU transmit characteristics, high power class

Parameter	25GBASE-PQG-U3 50/25GBASE-PQG-U3	25GBASE-PQX-U3 50/25GBASE-PQX-U3	50GBASE-PQ22G-U3	50GBASE-PQ22X-U3	Unit
Signaling rate (range)	25.78125 ± 100 ppm				GBd
Channel wavelength ranges	1260 to 1280	1290 to 1310	1260 to 1280 1290 to 1310	1290 to 1310 1318 to 1322	nm
Side-mode suppression ratio (SMSR) (min)	30				dB
Total average launch power (max)	—		12		dBm
Average launch power, each channel (max)	9				dBm
Optical Modulation Amplitude (OMA), each channel (min)[a]	4.7				dBm
Difference in launch power between any two channels (OMA) (max)	—		3		dB
Launch power in OMA minus TDP, each channel (min)(see note) for extinction ratio ≥ 6 dB for extinction ratio < 6 dB	4 4.2				dBm
Transmitter and dispersion penalty (TDP), each channel (max)	2				dB
Average launch power of OFF transmitter, each channel (max)	–45				dBm
Extinction ratio (min)	5				dB
$RIN_{15}OMA$ (max)	–128				dB/Hz
Optical return loss tolerance (max)	15				dB
Transmitter reflectance[b] (max)	–10				dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}[c]	{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				UI
Turn-on time (max)	128				ns
Turn-off time (max)	128				ns
NOTE—For reference, this implies that the minimum average launch power per channel at minimum extinction ratio and maximum TDP is 6 dBm. This minimum average launch power value is informative only.					

[a] Even if the TDP < 0.5 dB, the OMA (min) exceeds this value.
[b] Transmitter reflectance is defined looking into the transmitter.
[c] As defined in Figure 86–4.

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141.6.2 Receiver optical specifications

A medium power class Nx25G-EPON ONU PMD receiver shall comply with the parameters shown in Table 141–21. A high power class Nx25G-EPON ONU PMD receiver shall comply with the parameters shown in Table 141–22.

Table 141–21—ONU receive characteristics, medium power class

Parameter	25/10GBASE-PQG-U2 25/10GBASE-PQX-U2 25GBASE-PQG-U2 25GBASE-PQX-U2	50/10GBASE-PQG-U2 50/10GBASE-PQX-U2 50/25GBASE-PQG-U2 50/25GBASE-PQX-U2 50GBASE-PQX-U2 50GBASE-PQG-U2	Unit
Signaling rate (range)	25.78125 ± 100 ppm		GBd
Channel wavelengths (range)	1356 to 1360	1356 to 1360 1340 to 1344	nm
Bit error ratio (max)[a]	10^{-2}		—
Damage threshold[b]	–4		dBm
Average receive power, each channel (max)	–5		dBm
Receiver reflectance (max)	–12		dB
Receiver sensitivity (OMA), each channel[c] (max)(see note)	–21.4		dBm
Detect threshold, each channel (min)	–40		dBm
Stressed receiver sensitivity (OMA), each channel[d] (max)	–20.4		dBm
Conditions of stressed receiver sensitivity test			
Vertical eye closure penalty,[e] each channel	1.5		dB
Stressed eye J2 Jitter,[e] each channel	0.3		UI
Stressed eye J9 Jitter,[e] each channel	0.47		UI
NOTE—For reference, this implies that the maximum average power unstressed receiver sensitivity measured with an ideal transmitter signal at minimum extinction ratio is –23.5 dBm. This value is informative only.			

[a] The BER of 10^{-12} is achieved by the utilization of FEC as described in 142.2.4.1.
[b] The receiver tolerates, without damage, continuous exposure to an optical input signal having this average power level.
[c] Receiver sensitivity (OMA), each channel (max) is optional and is defined for a transmitter with VECP = 0.5 dB.
[d] Measured with conformance test signal at TP3 (see 141.7.11) for BER = 10^{-2}.
[e] Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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Table 141–22—ONU receive characteristics, high power class

Parameter	25/10GBASE-PQG-U3 25/10GBASE-PQX-U3 25GBASE-PQG-U3 25GBASE-PQX-U3	50/10GBASE-PQG-U3 50/10GBASE-PQX-U3 50/25GBASE-PQG-U3 50/25GBASE-PQX-U3 50GBASE-PQX-U3 50GBASE-PQG-U3	Unit
Channel wavelength ranges	1356 to 1360	1356 to 1360 1340 to 1344	nm
Signaling rate (range)	25.78125 ± 100 ppm		GBd
Bit error ratio (max)[a]	10^{-2}		—
Damage threshold[b]	–6.2		dBm
Average receive power, each channel (max)	–7.2		dBm
Receiver reflectance (max)	–12		dB
Receiver sensitivity (OMA), each channel[c] (max)	–24.1		dBm
Detect threshold, each channel (min)	–40		dBm
Stressed receiver sensitivity (OMA), each channel[d] (max)	–22.6		dBm
Conditions of stressed receiver sensitivity test			
Vertical eye closure penalty,[e] each channel	1.5		dB
Stressed eye J2 Jitter,[e] each channel	0.3		UI
Stressed eye J9 Jitter,[e] each channel	0.47		UI

[a] The BER of 10^{-12} is achieved by the utilization of FEC as described in 142.2.4.1.
[b] The receiver tolerates, without damage, continuous exposure to an optical input signal having this average power level. Direct ONU–OLT connection may result in damage of the receiver.
[c] Receiver sensitivity (OMA), each channel (max) is optional.
[d] Measured with conformance test signal at TP3 (see 141.7.11) for BER = 10^{-2}.
[e] Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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141.7 Definitions of optical parameters and measurement methods

The following subclauses describe definitive patterns and test procedures for Nx25G-EPON PMDs. Implementers using alternative verification methods need to ensure adequate correlation and allow adequate margin such that specifications are met by reference to the definitive methods. All optical measurements, except TDP and $RIN_{15}OMA$ shall be made through a short patch cable between 2 m and 5 m in length.

141.7.1 Insertion loss

Insertion loss for SMF fiber optic cabling (channel) is defined at the wavelengths specified in Table 141–13 and Table 141–14, depending on the particular PMD. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280–4–2.

141.7.2 Test patterns

The test patterns used in this clause shall be the same as those used for 100GBASE-LR4, as described in 88.8.1 and shown in Table 88–10, with the exception of Pattern 5. Table 88–11 shows the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. A valid 25G-EPON signal is substituted for the 100GBASE-R signal specified in Table 88–11.

141.7.3 Wavelength and spectral width measurement

The center wavelength and spectral width (RMS) shall meet the specifications when measured according to the centroidal wavelength and RMS spectral width definitions in IEC 61280-1-3 under modulated conditions using an appropriate PRBS or a valid Nx25G-EPON signal, or another representative test pattern.

NOTE—The allowable range of central wavelengths is narrower than the operating wavelength range by the actual RMS spectral width at each extreme.

141.7.4 Optical power measurements

Optical power shall meet specifications according to the methods specified in IEC 61280–1–1. A measurement may be made with the port transmitting any valid Nx25G-EPON signal.

141.7.5 Extinction ratio measurements

The extinction ratio shall meet the specifications when measured according to IEC 61280–2–2 with the port transmitting a valid Nx25G-EPON signal, and with minimal back reflections into the transmitter, lower than –20 dB. The test receiver has the frequency response as specified for the transmitter optical waveform measurement.

141.7.6 Optical Modulation Amplitude (OMA) test procedure

See 88.8.4.

141.7.7 Relative intensity noise optical modulation amplitude (RIN_xOMA) measuring procedure

See 88.8.7, with exception of the optical return loss value of 15 dB.

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141.7.8 Transmit optical waveform (transmit eye)

The required transmitter pulse shape characteristics for Nx25G-EPON PMDs are specified in the form of a mask of the transmitter eye diagram as shown in Figure 86–4 and the test method shall be according to 88.8.8.

141.7.9 Transmitter and dispersion penalty (TDP) for 25G

TDP measurement tests transmitter impairments, including chromatic dispersion effects, due to signal propagation in SMF used in PON. Possible causes of impairment include intersymbol interference, jitter, and RIN. Meeting the separate requirements (e.g., eye mask, spectral characteristics) does not in itself guarantee the TDP. The TDP limit shall be met. TDP is measured as defined in 88.8.5 with the exceptions in 141.7.9.2 and 141.7.9.4.

141.7.9.1 Reference transmitter requirements

The reference transmitter shall meet the requirements listed in 88.8.5.1.

141.7.9.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed below.

An Nx25G-EPON OLT or ONU transmitter is to be compliant with a total dispersion at least as negative as the minimum dispersion given by Equation (141–1) and at least as positive as the maximum dispersion given by Equation (141–2) for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

$$D_{\min} = \min\left(0,\ 0.465 \times \lambda \times \left(1 - \left(\frac{1324}{\lambda}\right)^4\right)\right) \tag{141–1}$$

$$D_{\max} = \max\left(0,\ 0.465 \times \lambda \times \left(1 - \left(\frac{1300}{\lambda}\right)^4\right)\right) \tag{141–2}$$

where

λ is the wavelength of the device under test in nm

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss of 15 dB. The state of polarization of the back reflection is adjusted to create the greatest RIN.

The mean DGD of the channel is to be less than 0.8 ps.

141.7.9.3 Reference receiver requirements

The reference receiver shall meet the requirements listed in 88.8.5.3.

141.7.9.4 Test procedure

The test procedure is as defined in 88.8.5.4, with the exception that a BER of 10^{-2} shall be used for the channel (wavelength) under test.

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141.7.10 Receive sensitivity

The test patterns in 75.7.3 (10G) and 141.7.2 (25G) are used to test receiver sensitivity.

The test signal is required to have negligible impairments such as intersymbol interference (ISI), rise/fall times, jitter, and RIN. The measurement procedure is described in 52.9.8 for 10 Gb/s PHYs and 88.8.9 for 25 Gb/s PHYs. The sensitivity shall be met for the bit error ratio defined in Table 141–17, Table 141–18, Table 141–21, or Table 141–22 as appropriate.

141.7.11 Stressed receiver conformance test

Compliance with stressed receiver sensitivity is mandatory for PMDs listed in Table 141–7. The stressed receiver conformance test is intended to screen against receivers with poor frequency response or timing characteristics that could cause errors when combined with a distorted but compliant signal. To be compliant with stressed receiver sensitivity, the receiver shall meet the specified bit error ratio at the power level and signal quality defined in Table 141–17, Table 141–18, Table 141–21, or Table 141–22 as appropriate, according to the measurement procedures of 52.9.9 for 10 Gb/s PHYs and 88.8.10 for 25 Gb/s PHYs.

141.7.12 Jitter measurements

When measuring jitter at TP1[*i*] and TP5[*i*], it is recommended that jitter contributions at frequencies below receiver corner frequencies (i.e., 10 MHz for 25.78125 GBd receiver and 4 MHz for 10.3125 GBd receiver) are filtered at the measurement unit.

141.7.13 Laser on/off timing measurement

T_{on} is defined in 141.7.13.1 and has the value of less than or equal to 128 ns (defined in Table 141–19 and Table 141–20).

T_{off} is defined in 141.7.13.1 and has the value of less than or equal to 128 ns (defined in Table 141–19 and Table 141–20).

141.7.13.1 Definitions

For each of the channels, T_{on} is denoted as the time beginning from the falling edge of the tx_enable line to the ONU PMD and ending at the time that the optical signal at TP2 of the ONU PMD is within 15% of its steady-state parameters (average launched power, wavelength, RMS spectral width, transmitter and dispersion penalty, optical return loss tolerance, jitter, $RIN_{15}OMA$, extinction ratio and eye mask opening) as defined in Table 141–19 and Table 141–20. T_{on} is presented in Figure 141–3. The data transmitted may be any valid 256B/257B symbols.

For each of the channels, T_{off} is denoted as the time beginning from the rising edge of the tx_enable line to the ONU PMD and ending at the time that the optical signal at TP2 of the ONU PMD reaches the specified maximum average launch power of OFF transmitter as defined in Table 141–19 and Table 141–20. T_{off} is presented in Figure 141–3. The data transmitted may be any of the patterns listed in Table 88–10.

141.7.13.2 Test specification

The test setup for measuring T_{on} and T_{off} is shown in Figure 141–4. An O/E converter is used to convert the optical signal at TP3 to an electrical signal at TP4[*i*] where it is assumed that the response time of the converter is considerably shorter that the T_{on} value under measurement. A scope, with a variable delay, is able to measure the time from the tx_enable trigger to the time the optical signal reaches all its specified conditions. The delay to the scope trigger is adjusted until the point that the received signal meets all its specified conditions. This is the T_{on} in question.

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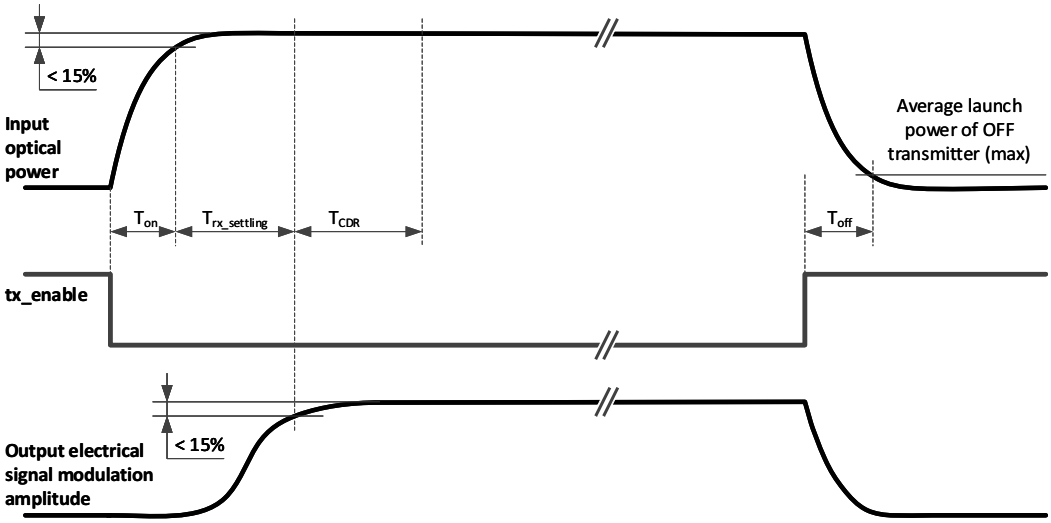

Figure 141–3—P2MP timing parameter definition, per channel

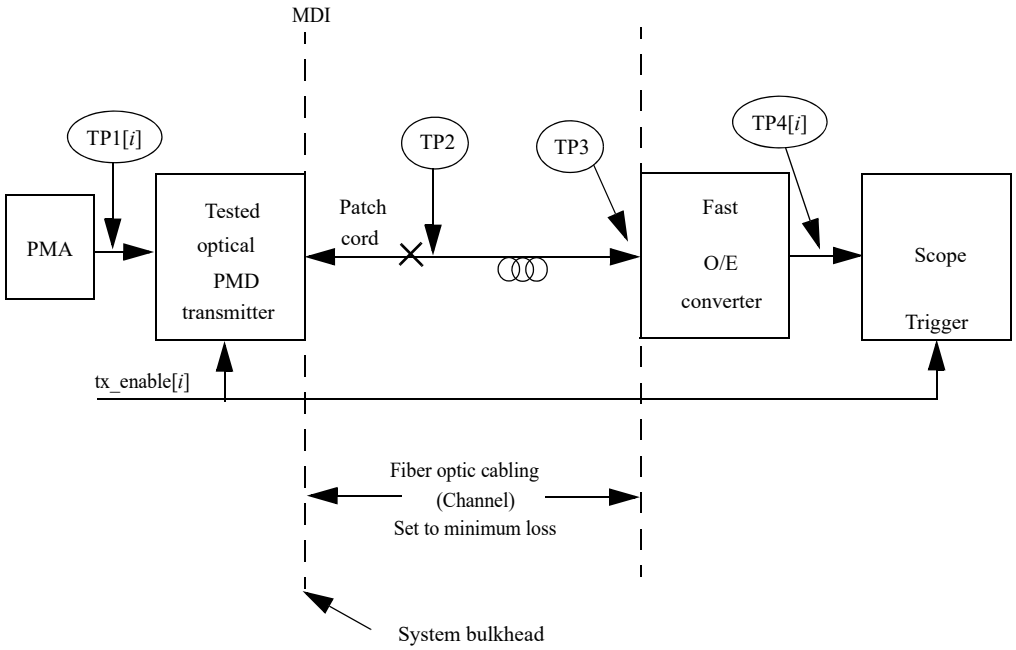

Figure 141–4—ONU PMD laser on/off time measurement setup

A non-rigorous way to describe this test setup would be: for a PMD with a declared T_{on} and T_{off}, measure all PMD optical parameters after T_{on} and T_{off} from the tx_enable trigger, confirming their conformance to being within 15% of the steady-state values. Notice that only the average launch power being below the average launch power of OFF transmitter is confirmed when measuring T_{off} time, since that is the only relevant parameter.

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141.7.14 Receiver settling timing measurement

$T_{rx\_settling}$ is defined in 141.7.14.1 and has a value of less than 800 ns (defined in Table 141–17 and Table 141–18). A method for measuring $T_{rx\_settling}$ is illustrated in Figure 141–5.

141.7.14.1 Definitions

$T_{rx\_settling}$ is defined to be the time between the moment when the optical power at TP7 reaches the conditions specified in 141.7.13.1 for T_{on} and the moment after which the electrical modulation (peak-to-peak) at TP8[*i*] remains within 15% of its steady-state amplitude and jitter (see Table 141–17 and Table 141–18). The $T_{rx\_settling}$ time interval is illustrated in Figure 141–3. The data transmitted may be any valid 256B/257B symbols (or a specific power synchronization sequence). The optical signal at TP7, at the beginning of the locking, may have any valid 256B/257B pattern, optical power level, jitter, or frequency shift matching the standard specifications.

141.7.14.2 Test specification

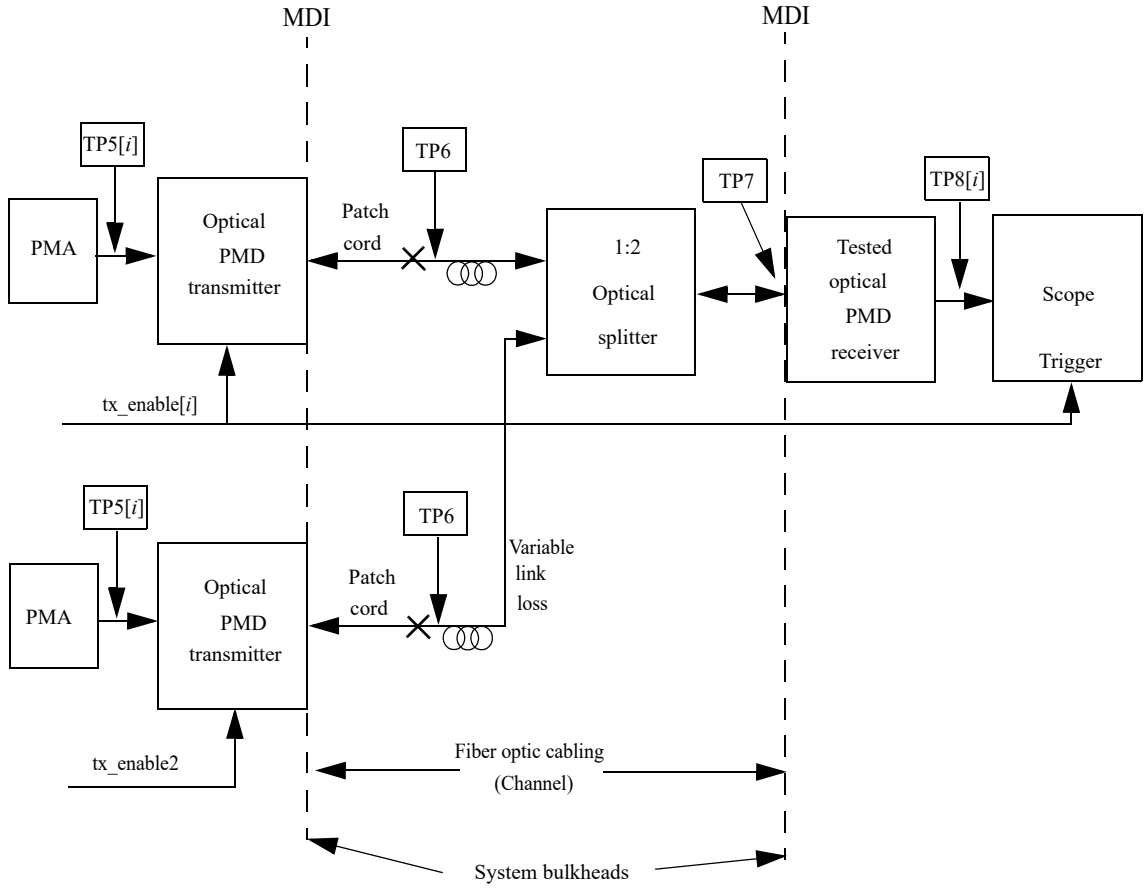

Figure 141–5—Receiver settling time measurement setup

Figure 141–5 illustrates the test setup for measuring the OLT PMD receiver (upstream) $T_{rx\_settling}$ time. The optical PMD transmitter has well–known parameters, with a fixed known T_{on} time. After T_{on} time the parameters of the reference transmitter, at TP6 and therefore at TP7, reach within 15% of their steady-state values as specified in Table 141–19 and Table 141–20.

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Define $T_{rx\_settling}$ time as the time from the tx_enable assertion, minus the known T_{on} time, to the time the electrical signal at TP8 reaches within 15% of its steady-state conditions.

Conformance needs to be assured for an optical signal at TP7 with any level of its specified parameters before the tx_enable assertion. Especially, the $T_{rx\_settling}$ time is expected to be met in the following scenarios:

— Switching from a 'weak' (minimal received power at TP7) ONU to a 'strong' (maximal received power at TP7) ONU, with minimal guard band between.
— Switching from a 'strong' ONU to a 'weak' ONU, with minimal guard band between.
— Switching from noise level, with maximal duration interval, to 'strong' ONU power level.

For a tested PMD receiver with a declared $T_{rx\_settling}$ time, measure all PMD receiver electrical parameters at TP8[*i*] after $T_{rx\_settling}$ from the tx_enable trigger minus the reference transmitter T_{on}, assuring conformance to within 15% of their specified steady-state values.

141.8 Environmental, safety, and labeling

141.8.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

141.8.2 Laser safety

Nx25G-EPON optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.

141.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

141.8.4 Environment

The Nx25G-EPON operating environment specifications are as defined in 52.11, as defined in 52.11.1 for electromagnetic emission, and as defined in 52.11.2 for temperature, humidity, and handling.

See Annex 67A for additional environmental information. Two optional temperature ranges are defined in Table 60–15. Implementations shall be declared as compliant over one or both complete ranges, or not so declared (compliant over parts of these ranges or another temperature range).

141.8.5 PMD labeling

The Nx25G-EPON labeling recommendations and requirements are as defined in 52.12.

The list of all supported PMDs is shown in Table 141–7.

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Each field-pluggable component shall be clearly labeled with its operating temperature range over which compliance is ensured.

141.9 Characteristics of the fiber optic cabling

The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. It also includes a connector plug at each end to connect to the MDI. The fiber optic cabling spans from one MDI to another MDI, as shown in Figure 141–2.

141.9.1 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 141–2.

NOTE—The optical splitter presented in Figure 141–2 may be replaced by a number of smaller 1:n splitters such that a different topology may be implemented while preserving the link characteristics and power budget.

The maximum channel insertion losses shall meet the requirements specified in Table 141–1 through Table 141–5. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term *channel* is used here for consistency with generic cabling standards.

141.9.2 Optical fiber and cable

The fiber optic cabling shall meet the dispersion specifications defined in ITU-T G.652, Section 6.10. Maximum and minimum dispersion levels at the maximum 20 km reach at the nominal transmission wavelengths bands are summarized in Table 141–23.

Table 141–23—Optical fiber and cable characteristics

Parameter	UW0	UW1	UW2	DW0	DW1	Unit
Nominal wavelength	1270	1300	1320	1358	1342	nm
Max Dispersion (at 20 km) [a,b]	–45.4	0	36	100.1	73.7	ps/nm
Min Dispersion (at 20 km) [a,b]	–105.9	–45.4	–7.4	47.8	25.8	ps/nm

[a] These dispersion values were calculated using inequalities specified in ITU-T G.652, section 6.10
[b] These dispersion requirements are satisfied by G.652.D fibers specified in ITU-T G.652 (low water peak, dispersion unshifted SMF) and G.657.A fibers specified in ITU-T G.657 (bend–insensitive SMF).

141.9.3 Optical fiber connection

An optical fiber connection consists of a mated pair of optical connectors or an optical splice point. The number of splices/connectors is not predefined; the number of individual fiber sections between the OLT MDI and the ONU MDI is not defined. The only requirements are that the resulting channel insertion loss at all specified transmission wavelengths is within the limits specified in Table 141–1 through Table 141–5. Other fiber arrangements (e.g., increasing the split ratio while decreasing the fiber length) are supported as long as the limits for the channel insertion loss specified in Table 141–1 through Table 141–5 are observed.

The maximum discrete reflectance for single-mode connections shall be less than –26 dB.

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141.9.4 Medium Dependent Interface (MDI)

The Nx25G-EPON PMD is coupled to the fiber cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" as shown in Figure 141–2. Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a remateable connection, it shall meet the interface performance specifications of IEC 61753-1. The MDI carries the signal in both directions for Nx25G-EPON PMDs and couples to a single fiber.

NOTE—Transmitter compliance testing is performed at TP2 or TP6 as defined in 141.3.2, not at the MDI.

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141.10 Protocol implementation conformance statement (PICS) proforma for Clause 141, Physical Medium Dependent (PMD) sublayer and medium for Nx25G-EPON passive optical networks[235]

141.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 141, Physical Medium Dependent (PMD) sublayer and medium for Nx25G-EPON passive optical networks, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

141.10.2 Identification

141.10.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

141.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 141, Physical Medium Dependent (PMD) sublayer and medium for Nx25G-EPON passive optical networks
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[235] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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141.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
HT	High temperature operation	141.8.4	–5 ºC to 85 ºC	O	Yes [ ] No [ ]
LT	Low temperature operation	141.8.4	–40 ºC to 60 ºC	O	Yes [ ] No [ ]
*PQG2510U2	25/10GBASE-PQG-U2 PHY or 25/10GBASE-PQG-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG2510D2	25/10GBASE-PQG-D2 PHY or 25/10GBASE-PQG-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG2510U3	25/10GBASE-PQG-U3 PHY or 25/10GBASE-PQG-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG2510D3	25/10GBASE-PQG-D3 PHY or 25/10GBASE-PQG-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQX2510U2	25/10GBASE-PQX-U2 PHY or 25/10GBASE-PQX-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX2510D2	25/10GBASE-PQX-D2 PHY or 25/10GBASE-PQX-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX2510U3	25/10GBASE-PQX-U3 PHY or 25/10GBASE-PQX-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX2510D3	25/10GBASE-PQX-D3 PHY or 25/10GBASE-PQX-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQG25U2	25GBASE-PQG-U2 PHY or 25GBASE-PQG-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG25D2	25GBASE-PQG-D2 PHY or 25GBASE-PQG-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG25U3	25GBASE-PQG-U3 PHY or 25GBASE-PQG-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG25D3	25GBASE-PQG-D3 PHY or 25GBASE-PQG-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
*PQX25U2	25GBASE-PQX-U2 PHY or 25GBASE-PQX-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX25D2	25GBASE-PQX-D2 PHY or 25GBASE-PQX-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX25U3	25GBASE-PQX-U3 PHY or 25GBASE-PQX-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX25D3	25GBASE-PQX-D3 PHY or 25GBASE-PQX-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQG5010U2	50/10GBASE-PQG-U2 PHY or 50/10GBASE-PQG-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG5010D2	50/10GBASE-PQG-D2 PHY or 50/10GBASE-PQG-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG5010U3	50/10GBASE-PQG-U3 PHY or 50/10GBASE-PQG-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG5010D3	50/10GBASE-PQG-D3 PHY or 50/10GBASE-PQG-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQX5010U2	50/10GBASE-PQX-U2 PHY or 50/10GBASE-PQX-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX5010D2	50/10GBASE-PQX-D2 PHY or 50/10GBASE-PQX-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX5010U3	50/10GBASE-PQX-U3 PHY or 50/10GBASE-PQX-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX5010D3	50/10GBASE-PQX-D3 PHY or 50/10GBASE-PQX-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQG5025U2	50/25GBASE-PQG-U2 PHY or 50/25GBASE-PQG-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG5025D2	50/25GBASE-PQG-D2 PHY or 50/25GBASE-PQG-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
*PQG5025U3	50/25GBASE-PQG-U3 PHY or 50/25GBASE-PQG-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG5025D3	50/25GBASE-PQG-D3 PHY or 50/25GBASE-PQG-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQX5025U2	50/25GBASE-PQX-U2 PHY or 50/25GBASE-PQX-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX5025D2	50/25GBASE-PQX-D2 PHY or 50/25GBASE-PQX-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX5025U3	50/25GBASE-PQX-U3 PHY or 50/25GBASE-PQX-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX5025D3	50/25GBASE-PQX-D3 PHY or 50/25GBASE-PQX-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQG50U2	50GBASE-PQG-U2 PHY or 50GBASE-PQG-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG50D2	50GBASE-PQG-D2 PHY or 50GBASE-PQG-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG50U3	50GBASE-PQG-U3 PHY or 50GBASE-PQG-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQG50D3	50GBASE-PQG-D3 PHY or 50GBASE-PQG-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with GPON	O.1	Yes [ ] No [ ]
*PQX50U2	50GBASE-PQX-U2 PHY or 50GBASE-PQX-U2 PMD	141.6	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX50D2	50GBASE-PQX-D2 PHY or 50GBASE-PQX-D2 PMD	141.5	Maximum channel insertion loss of 24 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX50U3	50GBASE-PQX-U3 PHY or 50GBASE-PQX-U3 PMD	141.6	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]
*PQX50D3	50GBASE-PQX-D3 PHY or 50GBASE-PQX-D3 PMD	141.5	Maximum channel insertion loss of 29 dB, coexistence with 10G-EPON	O.1	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
*INS	Installation/Cable	141.9	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
*OLT	OLT functionality		Device supports functionality required for OLT	O/2	Yes [ ] No [ ]
*ONU	ONU functionality		Device supports functionality required for ONU	O/2	Yes [ ] No [ ]

141.10.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium for passive optical networks, type 25/10GBASE-PQ, 25GBASE-PQ, 50/10GBASE-PQ, 50/25GBASE-PQ, and 50GBASE-PQ

141.10.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FN1	Transmit function	141.3.3	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FN2	Transmitter optical signal	141.3.3	Highest optical power transmitted is a logic one	M	Yes [ ]
FN3	Receive function	141.3.4	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FN4	Receiver optical signal	141.3.4	Higher optical power received is a logic one	M	Yes [ ]
FN5	ONU signal detect function	141.3.5.1	Mapping to PMD service interface	M	Yes [ ]
FN6	ONU signal detect parameter	141.3.5.1	Generated according to Table 141–12	M	Yes [ ]
FN7	OLT signal detect function	141.3.5.2	Mapping to PMD service interface	O/3	Yes [ ] No [ ]
FN8	OLT signal detect function	141.3.5.2	Provided by higher layer	O/3	Yes [ ] No [ ]
FN9	OLT signal detect parameter	141.3.5.2	Generated according to Table 141–12	O	Yes [ ] No [ ]
FN10	Delay variation	141.3.1.2	Less than 0.25 EQT	M	Yes [ ]
FN11	Receiver sensitivity	141.7.10	The sensitivity is met for the bit error ratio defined in Table 141–17, Table 141–18, Table 141–21, or Table 141–22 as appropriate	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
FN12	Stressed received sensitivity test	141.7.11	The receiver meets the specified bit error ratio at the power level and signal quality defined in Table 141–17, Table 141–18, Table 141–21, or Table 141–22 as appropriate, according to the measurement procedures of 52.9.9 for 10 Gb/s PHYs and 88.8.10 for 25 Gb/s PHYs.	M	Yes [ ]
FN13a	Channel-to-wavelength mapping, ONU	141.3.1.1	Channel-to-wavelength mapping for ONU	ONU:M	Yes [ ] N/A [ ]
FN13b	Channel-to-wavelength mapping, OLT	141.3.1.1	Channel-to-wavelength mapping for OLT	OLT:M	Yes [ ] N/A [ ]

141.10.4.2 PMD to MDI optical specifications for 25/10GBASE-PQG-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG2510D2F1	25/10GBASE-PQG-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQG2510D2:M	Yes [ ] N/A [ ]
PQG2510D2F2	25/10GBASE-PQG-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQG2510D2:M	Yes [ ] N/A [ ]

141.10.4.3 PMD to MDI optical specifications for 25/10GBASE-PQG-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG2510D3F1	25/10GBASE-PQG-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQG2510D3:M	Yes [ ] N/A [ ]
PQG2510D3F2	25/10GBASE-PQG-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQG2510D3:M	Yes [ ] N/A [ ]

141.10.4.4 PMD to MDI optical specifications for 25/10GBASE-PQX-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX2510D2F1	25/10GBASE-PQX-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQX2510D2:M	Yes [ ] N/A [ ]
PQX2510D2F2	25/10GBASE-PQX-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQX2510D2:M	Yes [ ] N/A [ ]

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141.10.4.5 PMD to MDI optical specifications for 25/10GBASE-PQX-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX2510D3F1	25/10GBASE-PQX-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQX2510D3:M	Yes [ ] N/A [ ]
PQX2510D3F2	25/10GBASE-PQX-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQX2510D3:M	Yes [ ] N/A [ ]

141.10.4.6 PMD to MDI optical specifications for 25GBASE-PQG-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG25D2F1	25GBASE-PQG-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQG25D2:M	Yes [ ] N/A [ ]
PQG25D2F2	25GBASE-PQG-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQG25D2:M	Yes [ ] N/A [ ]

141.10.4.7 PMD to MDI optical specifications for 25GBASE-PQG-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG25D3F1	25GBASE-PQG-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQG25D3:M	Yes [ ] N/A [ ]
PQG25D3F2	25GBASE-PQG-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQG25D3:M	Yes [ ] N/A [ ]

141.10.4.8 PMD to MDI optical specifications for 25GBASE-PQX-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX25D2F1	25GBASE-PQX-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQX25D2:M	Yes [ ] N/A [ ]
PQX25D2F2	25GBASE-PQX-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQX25D2:M	Yes [ ] N/A [ ]

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141.10.4.9 PMD to MDI optical specifications for 25GBASE-PQX-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX25D3F1	25GBASE-PQX-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQX25D3:M	Yes [ ] N/A [ ]
PQX25D3F2	25GBASE-PQX-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQX25D3:M	Yes [ ] N/A [ ]

141.10.4.10 PMD to MDI optical specifications for 50/10GBASE-PQG-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5010D2F1	50/10GBASE-PQG-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQG5010D2:M	Yes [ ] N/A [ ]
PQG5010D2F2	50/10GBASE-PQG-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQG5010D2:M	Yes [ ] N/A [ ]

141.10.4.11 PMD to MDI optical specifications for 50/10GBASE-PQG-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5010D3F1	50/10GBASE-PQG-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQG5010D3:M	Yes [ ] N/A [ ]
PQG5010D3F2	50/10GBASE-PQG-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQG5010D3:M	Yes [ ] N/A [ ]

141.10.4.12 PMD to MDI optical specifications for 50/10GBASE-PQX-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5010D2F1	50/10GBASE-PQX-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQX5010D2:M	Yes [ ] N/A [ ]
PQX5010D2F2	50/10GBASE-PQX-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQX5010D2:M	Yes [ ] N/A [ ]

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141.10.4.13 PMD to MDI optical specifications for 50/10GBASE-PQX-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5010D3F1	50/10GBASE-PQX-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQX5010D3:M	Yes [ ] N/A [ ]
PQX5010D3F2	50/10GBASE-PQX-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQX5010D3:M	Yes [ ] N/A [ ]

141.10.4.14 PMD to MDI optical specifications for 50/25GBASE-PQG-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5025D2F1	50/25GBASE-PQG-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQG5025D2:M	Yes [ ] N/A [ ]
PQG5025D2F2	50/25GBASE-PQG-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQG5025D2:M	Yes [ ] N/A [ ]

141.10.4.15 PMD to MDI optical specifications for 50/25GBASE-PQG-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5025D3F1	50/25GBASE-PQG-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQG5025D3:M	Yes [ ] N/A [ ]
PQG5025D3F2	50/25GBASE-PQG-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQG5025D3:M	Yes [ ] N/A [ ]

141.10.4.16 PMD to MDI optical specifications for 50/25GBASE-PQX-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5025D2F1	50/25GBASE-PQX-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQX5025D2:M	Yes [ ] N/A [ ]
PQX5025D2F2	50/25GBASE-PQX-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQX5025D2:M	Yes [ ] N/A [ ]

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141.10.4.17 PMD to MDI optical specifications for 50/25GBASE-PQX-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5025D3F1	50/25GBASE-PQX-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQX5025D3:M	Yes [ ] N/A [ ]
PQX5025D3F2	50/25GBASE-PQX-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQX5025D3:M	Yes [ ] N/A [ ]

141.10.4.18 PMD to MDI optical specifications for 50GBASE-PQG-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG50D2F1	50GBASE-PQG-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQG50D2:M	Yes [ ] N/A [ ]
PQG50D2F2	50GBASE-PQG-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQG50D2:M	Yes [ ] N/A [ ]

141.10.4.19 PMD to MDI optical specifications for 50GBASE-PQG-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG50D3F1	50GBASE-PQG-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQG50D3:M	Yes [ ] N/A [ ]
PQG50D3F2	50GBASE-PQG-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQG50D3:M	Yes [ ] N/A [ ]

141.10.4.20 PMD to MDI optical specifications for 50GBASE-PQX-D2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX50D2F1	50GBASE-PQX-D2 transmitter	141.5.1	Meets specifications in Table 141–15	PQX50D2:M	Yes [ ] N/A [ ]
PQX50D2F2	50GBASE-PQX-D2 receiver	141.5.2	Meets specifications in Table 141–17	PQX50D2:M	Yes [ ] N/A [ ]

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141.10.4.21 PMD to MDI optical specifications for 50GBASE-PQX-D3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX50D3F1	50GBASE-PQX-D3 transmitter	141.5.1	Meets specifications in Table 141–16	PQX50D3:M	Yes [ ] N/A [ ]
PQX50D3F2	50GBASE-PQX-D3 receiver	141.5.2	Meets specifications in Table 141–18	PQX50D3:M	Yes [ ] N/A [ ]

141.10.4.22 PMD to MDI optical specifications for 25/10GBASE-PQG-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG2510U2F1	25/10GBASE-PQG-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQG2510U2:M	Yes [ ] N/A [ ]
PQG2510U2F2	25/10GBASE-PQG-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQG2510U2:M	Yes [ ] N/A [ ]

141.10.4.23 PMD to MDI optical specifications for 25/10GBASE-PQG-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG2510U3F1	25/10GBASE-PQG-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQG2510U3:M	Yes [ ] N/A [ ]
PQG2510U3F2	25/10GBASE-PQG-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQG2510U3:M	Yes [ ] N/A [ ]

141.10.4.24 PMD to MDI optical specifications for 25/10GBASE-PQX-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX2510U2F1	25/10GBASE-PQX-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQX2510U2:M	Yes [ ] N/A [ ]
PQX2510U2F2	25/10GBASE-PQX-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQX2510U2:M	Yes [ ] N/A [ ]

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141.10.4.25 PMD to MDI optical specifications for 25/10GBASE-PQX-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX2510U3F1	25/10GBASE-PQX-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQX2510U3:M	Yes [ ] N/A [ ]
PQX2510U3F2	25/10GBASE-PQX-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQX2510U3:M	Yes [ ] N/A [ ]

141.10.4.26 PMD to MDI optical specifications for 25GBASE-PQG-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG25U2F1	25GBASE-PQG-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQG25U2:M	Yes [ ] N/A [ ]
PQG25U2F2	25GBASE-PQG-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQG25U2:M	Yes [ ] N/A [ ]

141.10.4.27 PMD to MDI optical specifications for 25GBASE-PQG-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG25U3F1	25GBASE-PQG-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQG25U3:M	Yes [ ] N/A [ ]
PQG25U3F2	25GBASE-PQG-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQG25U3:M	Yes [ ] N/A [ ]

141.10.4.28 PMD to MDI optical specifications for 25GBASE-PQX-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX25U2F1	25GBASE-PQX-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQX25U2:M	Yes [ ] N/A [ ]
PQX25U2F2	25GBASE-PQX-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQX25U2:M	Yes [ ] N/A [ ]

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141.10.4.29 PMD to MDI optical specifications for 25GBASE-PQX-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX25U3F1	25GBASE-PQX-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQX25U3:M	Yes [ ] N/A [ ]
PQX25U3F2	25GBASE-PQX-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQX25U3:M	Yes [ ] N/A [ ]

141.10.4.30 PMD to MDI optical specifications for 50/10GBASE-PQG-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5010U2F1	50/10GBASE-PQG-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQG5010U2:M	Yes [ ] N/A [ ]
PQG5010U2F2	50/10GBASE-PQG-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQG5010U2:M	Yes [ ] N/A [ ]

141.10.4.31 PMD to MDI optical specifications for 50/10GBASE-PQG-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5010U3F1	50/10GBASE-PQG-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQG5010U3:M	Yes [ ] N/A [ ]
PQG5010U3F2	50/10GBASE-PQG-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQG5010U3:M	Yes [ ] N/A [ ]

141.10.4.32 PMD to MDI optical specifications for 50/10GBASE-PQX-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5010U2F1	50/10GBASE-PQX-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQX5010U2:M	Yes [ ] N/A [ ]
PQX5010U2F2	50/10GBASE-PQX-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQX5010U2:M	Yes [ ] N/A [ ]

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141.10.4.33 PMD to MDI optical specifications for 50/10GBASE-PQX-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5010U3F1	50/10GBASE-PQX-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQX5010U3:M	Yes [ ] N/A [ ]
PQX5010U3F2	50/10GBASE-PQX-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQX5010U3:M	Yes [ ] N/A [ ]

141.10.4.34 PMD to MDI optical specifications for 50/25GBASE-PQG-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5025U2F1	50/25GBASE-PQG-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQG5025U2:M	Yes [ ] N/A [ ]
PQG5025U2F2	50/25GBASE-PQG-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQG5025U2:M	Yes [ ] N/A [ ]

141.10.4.35 PMD to MDI optical specifications for 50/25GBASE-PQG-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG5025U3F1	50/25GBASE-PQG-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQG5025U3:M	Yes [ ] N/A [ ]
PQG5025U3F2	50/25GBASE-PQG-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQG5025U3:M	Yes [ ] N/A [ ]

141.10.4.36 PMD to MDI optical specifications for 50/25GBASE-PQX-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5025U2F1	50/25GBASE-PQX-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQX5025U2:M	Yes [ ] N/A [ ]
PQX5025U2F2	50/25GBASE-PQX-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQX5025U2:M	Yes [ ] N/A [ ]

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141.10.4.37 PMD to MDI optical specifications for 50/25GBASE-PQX-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX5025U3F1	50/25GBASE-PQX-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQX5025U3:M	Yes [ ] N/A [ ]
PQX5025U3F2	50/25GBASE-PQX-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQX5025U3:M	Yes [ ] N/A [ ]

141.10.4.38 PMD to MDI optical specifications for 50GBASE-PQG-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQG50U2F1	50GBASE-PQG-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQG50U2:M	Yes [ ] N/A [ ]
PQG50U2F2	50GBASE-PQG-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQG50U2:M	Yes [ ] N/A [ ]

141.10.4.39 PMD to MDI optical specifications for 50GBASE-PQG-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQG50U3F1	50GBASE-PQG-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQG50U3:M	Yes [ ] N/A [ ]
PQG50U3F2	50GBASE-PQG-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQG50U3:M	Yes [ ] N/A [ ]

141.10.4.40 PMD to MDI optical specifications for 50GBASE-PQX-U2

Item	Feature	Subclause	Value/Comment	Status	Support
PQX50U2F1	50GBASE-PQX-U2 transmitter	141.6.1	Meets specifications in Table 141–19	PQX50U2:M	Yes [ ] N/A [ ]
PQX50U2F2	50GBASE-PQX-U2 receiver	141.6.2	Meets specifications in Table 141–21	PQX50U2:M	Yes [ ] N/A [ ]

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141.10.4.41 PMD to MDI optical specifications for 50GBASE-PQX-U3

Item	Feature	Subclause	Value/Comment	Status	Support
PQX50U3F1	50GBASE-PQX-U3 transmitter	141.6.1	Meets specifications in Table 141–20	PQX50U3:M	Yes [ ] N/A [ ]
PQX50U3F2	50GBASE-PQX-U3 receiver	141.6.2	Meets specifications in Table 141–22	PQX50U3:M	Yes [ ] N/A [ ]

141.10.4.42 Definitions of optical parameters and measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	141.7.1	2 m to 5 m in length	M	Yes [ ]
OM2	Wavelength and RMS spectral width	141.7.3	Per the centroidal wavelength and RMS spectral width definitions in IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	141.7.4	Per IEC 61280-1-1	M	Yes [ ]
OM4	Extinction ratio	141.7.5	Per IEC 61280-2-2 with minimal back reflections	M	Yes [ ]
OM5	Optical modulation amplitude (OMA) test procedure	141.7.6		M	Yes [ ]
OM6	RIN_xOMA	141.7.7		M	Yes [ ]
OM7	Transmit optical waveform (transmit eye)	141.7.8		M	Yes [ ]
OM8	Transmitter and dispersion penalty	141.7.9		M	Yes [ ]
OM9	Receiver sensitivity	141.7.10		M	Yes [ ]
OM10	Stressed receiver conformance test	141.7.11		O	Yes[ ] No[ ]
OM11	Jitter measurements	141.7.12		M	Yes [ ]
OM12	Laser On/Off timing measurement	141.7.13		M	Yes [ ]
OM13	Receiver settling timing measurement	141.7.14		O	Yes [ ] No [ ]

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141.10.4.43 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
FO1	Fiber optic cabling	141.9	Specified in Table 141–23	INS:M	Yes [ ] N/A[ ]
F02	End–to–end channel loss	141.9	Meeting the requirements of Table 141–1 through Table 141–5	INS:M	Yes [ ] N/A[ ]
FO3	Maximum discrete reflectance – single-mode fiber	141.9.3	Less than –26 dB	INS:M	Yes [ ] N/A [ ]
FO4	MDI requirements	141.9.4	Meet the interface performance specifications of IEC 61753-1, if remateable	INS:O	Yes [ ] No [ ] N/A [ ]

141.10.4.44 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	141.8.1	Conforms to J.2	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	141.8.2	Conform to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Documentation	141.8.2	Explicitly defines requirements and usage restrictions to meet safety certifications	M	Yes [ ]
ES4	Operating temperature range	141.8.4	The operating temperature range is declared	M	Yes [ ]
ES5	Operating temperature range label	141.8.5	Provided for field-pluggable components	M	Yes [ ]

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142. Physical Coding Sublayer and Physical Media Attachment for Nx25G-EPON

142.1 Overview

This clause describes the Physical Coding Sublayer (PCS) with forward error correction (FEC) and Physical Medium Attachment (PMA) used with Nx25G-EPON point-to-multipoint (P2MP) networks. P2MP networks are passive optical networks (PONs) that connect multiple DTEs using a single shared fiber. The architecture is asymmetric, based on a tree and branch topology utilizing passive optical splitters. This type of network requires that the Multipoint MAC Control sublayer exists above the MACs, as described in Clause 144 (see Figure 142–1).

In this clause the term xMII is used to refer to both the 25GMII and the XGMII interfaces.

Figure 142–2 illustrates the functional block diagram of the Nx25G-EPON PHY with emphasis placed on the PCS. The Nx25G-EPON PCS is specified to support Nx25G-EPON PMDs, where:

— Both the receive and transmit paths operate at 25.78125 GBd rate (25/25G-EPON, 50/25G-EPON, and 50/50G-EPON), or
— The receive path operates at 25.78125 GBd rate and the transmit path operates at 10.3125 GBd (25/10G-EPON and 50/10G-EPON ONU), or
— The transmit path operates at 25.78125 GBd rate and the receive path operates at 10.3125 GBd (25/10G-EPON and 50/10G-EPON OLT).

See 143.3.1.1 for definition of TXD, TXC, TX_CLK, RXD, RXD, and RX_CLK.

142.1.1 Conventions

142.1.1.1 State diagrams

The body of this clause includes state diagrams and the associated definitions of variables, constants, and functions. The notation used in the state diagrams follows the conventions in 21.5, with extensions listed in the following subclauses. In case of any discrepancies between a state diagram and descriptive text, the state diagram prevails.

142.1.1.2 Hexadecimal notation

In addition to the rules for hexadecimal notation described in 1.2.5, the following conventions are used:

— Individual octets of a hexadecimal number are separated by hyphens, e.g., 0x1E-EE-80-23-CA.
— A part of a hexadecimal number enclosed in parenthesis followed by a subscripted decimal number *n* indicates that the parenthetical portion is to be repeated *n* times. For example, $0x12\text{-}34\text{-}56\text{-}(AB\text{-}CD)_6\text{-}EF$ is equivalent to the following expanded representation of a 128-bit number: 0x12-34-56-AB-CD-AB-CD-AB-CD-AB-CD-AB-CD-EF.

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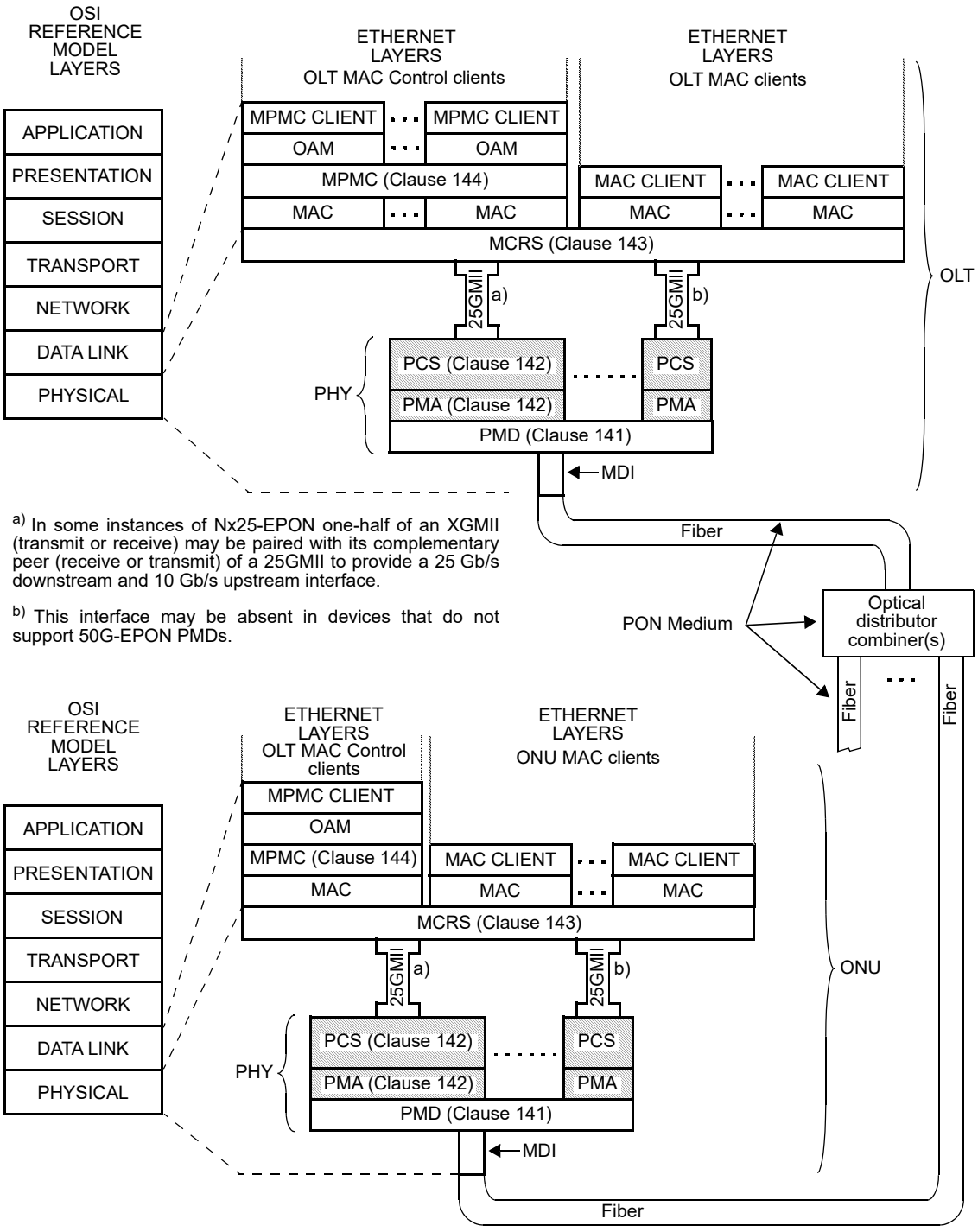

Figure 142–1—Relationship of Nx25G-EPON P2MP PCS and PMA to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

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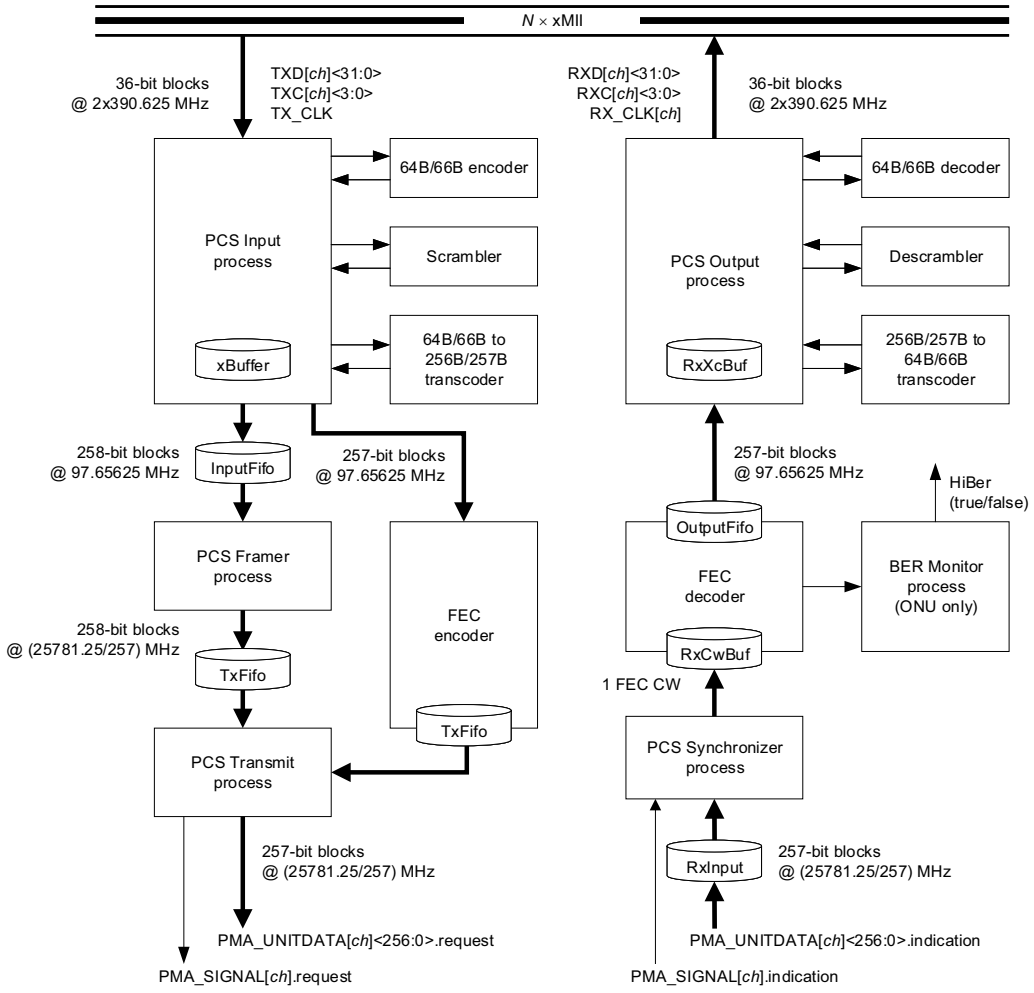

a) PCS transmit path **b) PCS receive path**

NOTE—All clock frequencies in this figure are shown for the nominal MAC data rate of 25 Gb/s. For PCS devices supporting the nominal MAC data rate of 10 Gb/s, all clock frequencies are scaled down by a multiplicative coefficient of 0.4.

Figure 142–2—PCS functional block diagram

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142.1.1.3 Timers

Some state diagrams may utilize timers. Timers follow the conventions of 14.2.3.2 augmented as follows:

a) [start x_timer, *y*] sets expiration of *y* to timer x_timer.
b) Upon expiration of timer x_timer, a Boolean variable x_timer_done gets asserted automatically. Restarting the timer x_timer deasserts the value of x_timer_done.
c) [stop x_timer] aborts the timer operation for x_timer deasserting x_timer_done indefinitely.

142.1.1.4 Operations on variables

The operators used in state diagrams and in associated definitions of variables, constants, and functions are defined in Table 142–1. The operators are listed in decreasing order of precedence.

Table 142–1—Operators used in state diagrams and functions

Operator	Meaning
(…)	Indicates precedence or a set of function arguments
[…]	Array subscript
++	Unary operator placed after a variable; increments the variable by 1
– –	Unary operator placed after a variable; decrements the variable by 1
!	Boolean NOT
*	Multiplication
/	Division
+	Addition
–	Subtraction
<	Less than (see 142.1.1.5)
>	More than (see 142.1.1.5)
≤	Less than or equal to (see 142.1.1.5)
≥	More than or equal to (see 142.1.1.5)
= =	Equals (a test of equality)
!=	Not equals
AND	Logical or bitwise AND. If one or both operands are defined as Boolean values, the operation is logical AND. Otherwise, the operation is considered the bitwise AND (each bit of the first operand is logically AND-ed with the corresponding bit of the second operand).
XOR	Logical or bitwise exclusive OR. If one or both operands are defined as Boolean values, the operation is logical XOR. Otherwise, the operation is considered the bitwise XOR (each bit of the first operand is logically XOR-ed with the corresponding bit of the second operand).

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Table 142–1—Operators used in state diagrams and functions *(continued)*

Operator	Meaning
OR	Logical or bitwise OR. If one or both operands are defined as Boolean values, the operation is logical OR. Otherwise, the operation is considered the bitwise OR (each bit of the first operand is logically OR-ed with the corresponding bit of the second operand).
|	Concatenation operation that combines several subfields or parameters into a single aggregated field or parameter
∈	Is a member of
∉	Is not a member of
⇐ =	Assignment operator (in state diagrams) Assignment operator (in function code)
+=	Increments left operand value by the value of the operand on the right (x += y is equivalent to x ⇐ x + y)
–=	Decrements left operand value by the value of the operand on the right (x –= y is equivalent to x ⇐ x – y)

Variables that allow access to individual bits are called vectors. The vector notations use 0 to mark the first received bit. Individual bits are accessed using the following notation:

a) data_vector<*k*> accesses the *k*th bit of the vector.
b) data_vector<*m*:*n*> accesses bits *n* through *m* inclusively. The *n*th bit is received earlier than the *m*th bit. Refer to 3.1.1 for the conventions on bit ordering.

142.1.1.5 Operations on wrap-around variables

Various integer variables/counters defined in this clause wrap around on overflow, i.e., reset to zero when incremented by one after reaching the maximum value. A subtraction operation ($a - b$) on such variables is straightforward and may be replaced by addition of the first operand a and two's complement of the second operand b. Unless explicitly stated, the result of such subtraction is a signed integer of the same size (bit width) as the largest of the two operands. In other words, the subtraction operation assumes that the maximum absolute difference between the two operands does not exceed half of their maximum range.

A function $a < b$ is used to compare two wrap-around values. Returned value is true when b is larger than a allowing for wrap-around of a and b. The comparison is made by subtracting b from a and testing the MSB. If MSB($a - b$) = 1 (i.e., if the result of $a - b$ is negative) the value true is returned, else false is returned. In addition, the following functions are defined in terms of $a < b$:

a) $a > b$ is equivalent to !*(a < b or a = b)*
b) $a \geq b$ is equivalent to !*(a < b)*
c) $a \leq b$ is equivalent to !*(a > b)*

142.1.1.6 FIFO access operations

State diagrams make extensive use of first-in, first-out (FIFO) buffers. These buffers support a common set of operations, defined as follows:

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a) Buf.Append(*e*) adds the element *e* to the input of FIFO buffer Buf.
b) Buf.Clear() removes all elements from the FIFO buffer Buf.
c) Buf.Fill(*e*) writes element/value *e* into each position of FIFO buffer Buf.
d) Buf.GetHead() returns the oldest (head) element in the FIFO buffer Buf, and removes that element from the FIFO, decreasing its length by one.
e) Buf.IsEmpty() returns true if the FIFO buffer is empty (has no elements), otherwise the function returns false.
f) Buf.IsFull() returns true if the FIFO buffer Buf is full (i.e., Buf has no unoccupied positions), otherwise the function returns false.
g) Buf.PeekHead() returns the oldest (head) element in the FIFO buffer Buf without removing that element from the FIFO.

All of the FIFO access operations are assumed to be non-blocking and to take zero time to complete the execution.

142.1.2 Delay constraints

The combined delay variation through the transmit path of the Nx25G-EPON PCS and PMA is expected to be less than 6 EQTs (see 1.4.313) for channels operating at 25.78125 GBd and less than 15 EQTs for channels operating at 10.3125 GBd.

The combined delay variation through the receive path of the Nx25G-EPON PCS and PMA is expected to be less than 2 EQTs for channels operating at 25.78125 GBd and less than 5 EQTs for channels operating at 10.3125 GBd.

The aforementioned delay variation limits are applicable only for the data units (either EQ or the corresponding 257-bit block) located at the fixed offset within the FEC codeword.

142.1.3 Burst transmission

Figure 142–3 presents the details of the ONU burst transmission, in particular, details of the FEC-unprotected and the FEC-protected areas of the upstream burst with three distinct synchronization pattern zones.

The upstream burst begins with a synchronization pattern, which is not FEC protected. The synchronization pattern comprises: SP1 zone, optimized for laser on (T_{on}) and automatic gain control (AGC, $T_{rx\_settling}$); SP2 zone, optimized for clock and data recovery (CDR, T_{CDR}); and SP3 zone, optimized for the start-of-burst delimiter (SBD) pattern. Each SP zone is a multiple of 257 bits, aligning with the PCS (defined in 142.2 and 142.3) line code of 256B/257B.

Bit patterns transmitted within each SP zone are configured by the OLT using three SYNC_PATTERN MPCPDUs (see 144.3.6.7).

In the bursts transmitted during the discovery operation, the SBD is followed by a single (shortened) FEC codeword carrying a single REGISTER_REQ MPCPDU. In normal operation the SBD is followed by a number of FEC codewords, where the last codeword may be shortened to reduce the unused QC-LDPC codeword payload at the end of the burst (see 142.2.4). Each FEC codeword comprises a series of 256B/257B encoded and scrambled data blocks, followed by a series of 257-bit long parity blocks. Within a non-shortened FEC codeword, the FEC payload portion includes 56 of these 257-bit data blocks and 10 257-bit blocks carrying QC-LDPC parity and codeword delimiter. Within a shortened FEC codeword, the FEC payload portion may be truncated to a number of data blocks smaller than 56, while the size of the FEC parity portion remains unchanged.

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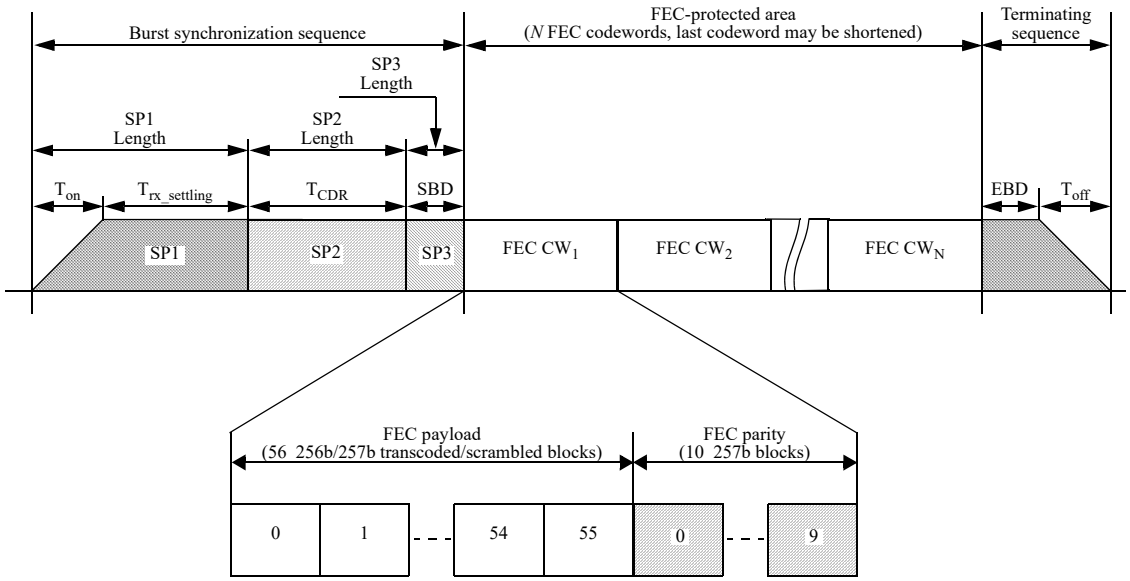

Figure 142–3—ONU burst structure, 3 zones

The upstream burst ends with an end-of-burst delimiter (EBD). When received at the OLT, the EBD pattern allows for the rapid reset of the OLT FEC synchronizer, preparing the OLT for the next incoming upstream burst. The EBD pattern is not part of the last FEC codeword.

142.1.3.1 Default synchronization pattern parameters

To assist the device development, testing/verification, and interoperability efforts, this subclause provides a set of default synchronization pattern parameters.

SP1 and SP2 synchronization patterns have the value of 0x1-$(AA)_{32}$ and are transmitted in a balanced form, i.e., every 257-bit block starting with the second one is an inversion of the previous block. The transmission bit sequence consists of 257 bits of alternating 1s and 0s, starting with 1.

The SP3 synchronization pattern zone represents the start-of-burst delimiter (SBD). It has the length of one block (257 bits) and the value of 0x1-BF-40-18-E5-C5-49-BB-59-6B-F8-D8-12-D8-58-E4-AB-40-BF-E7 -1A-3A-B6-44-A6-94-07-27-ED-27-A7-1B-54. The transmission bit sequence is:

```
(first bit)   1  1111 1101 0000 0010 0001 1000 1010 0111
                 1010 0011 1001 0010 1101 1101 1001 1010
                 1101 0110 0001 1111 0001 1011 0100 1000
                 0001 1011 0001 1010 0010 0111 1101 0101
                 0000 0010 1111 1101 1110 0111 0101 1000
                 0101 1100 0110 1101 0010 0010 0110 0101
                 0010 1001 1110 0000 1110 0100 1011 0111
                 1110 0100 1110 0101 1101 1000 0010 1010   (last bit)
```


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This combination of SP2 and SP3 synchronization pattern values is characterized by the Hamming distance of 110 or higher between the SP3 and any preceding 257-bit long pattern, i.e., concatenation of x bits of SP2 and y bits of SP3, where x is between 1 and 257, and $x + y = 257$.

142.2 PCS transmit data path

This subclause defines the transmit direction of the Nx25G-EPON PCS. In the OLT, the PCS transmit function operates in a continuous mode at 25.78125 GBd rate.

In the ONU, the PCS transmit function operates in burst mode at 25.78125 GBd rate (25/25G-EPON, 50/25G-EPON, and 50/50G-EPON) or at 10.3125 GBd rate (25/10G-EPON and 50/10G-EPON).

The PCS transmit function includes a mandatory QC-LDPC FEC encoder. The functional block diagram for the PCS transmit function is shown in Figure 142–2. The PCS transmit function consists of the following functional blocks:

— PCS Input process (see 142.2.5.4.1),
— PCS Framer process (see 142.2.5.4.2), and
— PCS Transmit process (see 142.2.5.4.3).

As shown in Figure 142–4, the PCS transmitter first inputs two transfers from the xMII and consolidates these into a single 72-bit block that is then encoded into a 66-bit block. Four 66-bit blocks are accumulated, scrambled, and transcoded into a 257-bit block that is transferred to the InputFifo and also copied to the FEC encoder. Data is transferred to the TxFifo, along with framing information (see 142.2.5.4.2) by the PCS Framer process. The PCS Transmit process transfers 257-bit blocks containing framing, information, and parity bits to the PMA. The PCS shall transmit bits in the order shown in Figure 142–4.

NOTE—Figure 142–4 only shows the bits that are being transmitted and does not show the bit that is added and removed within PCS for control purposes.

142.2.1 64B/66B line encoder

The Nx25G PCS encodes a 72-bit block into a 64B/66B block structure as defined in 49.2.4, using all the block type fields in Figure 49–7 except block type field values of: 0x2D, 0x33, 0x66, 0x55, and 0x4B.

The control characters and their mappings to Nx25G-EPON control codes are specified in Table 142–2. The representations of the control characters are the control codes. Control characters are transferred over the xMII as 7-bit values. The Nx25G-EPON PCS encodes the start and terminate control characters implicitly using the block type field. The Nx25G-EPON PCS does not support ordered set control codes. All control code values that do not appear in Table 142–2 shall not be transmitted and are treated as an error if received.

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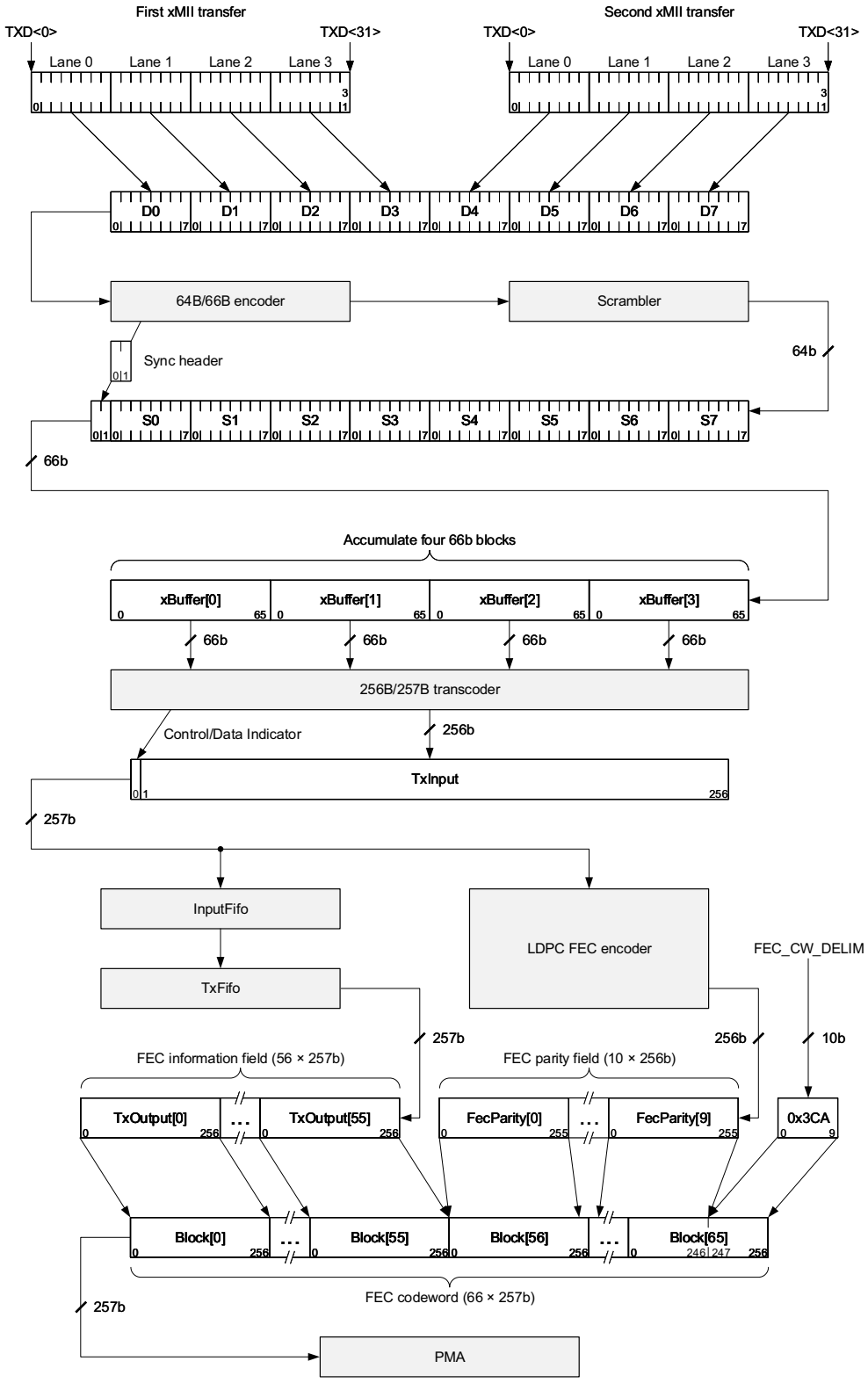

Figure 142–4—Transmit bit ordering

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Table 142–2—Control codes

Control character	Notation	xMII control code	Nx25GBASE-PQ control code
Idle	/I/	0x07	0x00
Inter-envelope idle	/IEI/	0x08	0x08
Rate adjust	/RA/	0x09	0x09
Inter-burst idle	/IBI/	0x0A	0x0A
Start	/S/	0xFB	Encoded by block type field
Terminate	/T/	0xFD	Encoded by block type field
Error	/E/	0xFE	0x1E

142.2.2 Scrambler

The Nx25G PCS scrambles the payload of each 66-bit block. It then accumulates 66-bit blocks into groups of four and transcodes each group into a single 257-bit block. The payload of each 66-bit block is scrambled using the scrambling function defined in 49.2.6.

In the ONU, at the beginning of each burst, the scrambler is reset to a known initialization value (see the definition of ResetScrambler() function in 142.2.5.3).

142.2.3 64B/66B to 256B/257B transcoder

The 64B/66B to 256B/257B transcoder converts four consecutive scrambled 64B/66B blocks into one scrambled 256B/257B block as described in 91.5.2.5.

142.2.4 FEC encoder

The Nx25G-EPON PCS shall encode the transmitted data stream using a quasi-cyclic QC-LDPC FEC, defined in 142.2.4.1. FEC encoder test vectors are provided in Annex 142A.

142.2.4.1 Low-density parity-check coding

The full QC-LDPC code is defined by a $(M + P) \times (K + S + M + P) = 3\,072 \times 17\,664$ size parity-check matrix H composed of a 12×69 array of 256×256 sub-matrices $A_{i,j}$:

$$H = \begin{bmatrix} A_{1,1} & \cdots & A_{1,69} \\ \cdots & & \cdots \\ A_{12,1} & \cdots & A_{12,69} \end{bmatrix}$$

The sub-matrices $A_{i,j}$ are either a cyclic shifted version of identity matrix or a zero matrix, and have a size of 256×256. The parity-check matrix is described in its compact form:

$$H_C = \begin{bmatrix} a_{1,1} & \cdots & a_{1,69} \\ \cdots & & \cdots \\ a_{12,1} & \cdots & a_{12,69} \end{bmatrix}$$

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where $a_{i,j} = -1$ for a zero sub-matrix in position (i, j), and a positive integer number $a_{i,j}$ defines the number of right column shifts of the identity matrix.

The compact form of parity-check matrix H_c is shown in Table 142–3.

Table 142–3—Compact form of parity-check matrix H_c

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
80	–1	–1	105	–1	–1	137	–1	–1	0	209	53
–1	0	91	–1	170	46	–1	118	208	–1	–1	–1
–1	–1	–1	–1	250	–1	104	15	0	–1	252	93
60	0	74	87	–1	37	–1	–1	–1	123	–1	–1
169	–1	–1	–1	–1	–1	238	93	0	–1	39	216
–1	0	237	43	195	49	–1	–1	–1	41	–1	–1
11	–1	202	–1	139	150	–1	–1	0	191	–1	–1
–1	0	–1	165	–1	–1	228	228	–1	–1	159	57
143	–1	–1	–1	–1	65	–1	–1	0	211	69	9
–1	0	201	180	135	–1	225	78	–1	–1	–1	–1
–1	–1	136	–1	–1	–1	247	–1	0	217	37	130
222	0	–1	80	92	177	–1	16	–1	–1	–1	–1
–1	–1	178	227	–1	144	–1	0	–1	243	134	–1
59	0	–1	–1	147	–1	191	–1	251	–1	–1	130
–1	–1	239	221	–1	70	–1	48	0	97	–1	–1
218	0	–1	–1	1	–1	177	–1	–1	–1	201	238
–1	–1	183	77	–1	95	–1	0	–1	252	49	–1
–1	0	–1	–1	–1	–1	255	–1	44	–1	–1	–1
178	0	–1	–1	–1	–1	–1	–1	123	–1	–1	–1
–1	–1	217	0	–1	221	–1	–1	–1	–1	–1	–1
–1	0	–1	–1	13	–1	–1	62	–1	–1	–1	–1
–1	–1	232	–1	–1	–1	–1	–1	–1	0	104	–1
–1	–1	–1	–1	–1	–1	192	0	–1	–1	–1	144
–1	–1	–1	–1	98	192	–1	–1	0	–1	–1	–1
105	0	–1	16	–1	–1	–1	–1	–1	–1	–1	–1
–1	–1	169	–1	–1	128	–1	0	–1	–1	–1	–1
–1	–1	–1	–1	142	–1	–1	–1	0	–1	129	–1
19	0	–1	–1	–1	–1	51	–1	–1	–1	–1	–1
–1	–1	–1	–1	–1	214	–1	–1	–1	0	–1	162

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Table 142–3—Compact form of parity-check matrix H_c *(continued)*

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
–1	–1	–1	252	–1	–1	–1	–1	–1	–1	157	0
126	–1	–1	–1	225	–1	–1	0	–1	–1	–1	–1
–1	–1	–1	96	–1	–1	–1	–1	0	41	–1	–1
–1	0	129	–1	–1	–1	195	–1	–1	–1	–1	–1
–1	–1	60	0	–1	–1	–1	–1	–1	–1	222	–1
211	–1	–1	–1	–1	51	0	–1	–1	–1	–1	–1
–1	–1	–1	–1	–1	–1	–1	–1	0	29	–1	175
–1	0	–1	–1	23	–1	–1	112	–1	–1	–1	–1
–1	–1	–1	–1	108	–1	172	–1	–1	0	–1	–1
–1	–1	–1	17	–1	100	–1	0	–1	–1	–1	–1
–1	0	19	–1	–1	–1	–1	–1	–1	–1	–1	145
247	–1	76	–1	–1	–1	–1	–1	0	–1	–1	–1
–1	–1	–1	–1	–1	19	–1	–1	–1	–1	139	0
255	–1	–1	–1	–1	–1	–1	–1	–1	0	39	–1
–1	0	–1	–1	–1	–1	219	–1	153	–1	–1	–1
–1	–1	–1	219	0	235	–1	–1	–1	–1	–1	–1
85	–1	–1	–1	–1	–1	–1	0	–1	–1	–1	36
–1	–1	77	–1	0	–1	236	–1	–1	–1	–1	–1
–1	0	–1	198	–1	–1	–1	–1	–1	193	–1	–1
–1	–1	–1	165	–1	–1	–1	–1	0	–1	203	–1
–1	–1	–1	–1	–1	–1	136	0	–1	145	–1	–1
–1	–1	2	–1	–1	–1	–1	0	–1	–1	94	–1
–1	–1	–1	–1	135	–1	–1	–1	0	–1	–1	91
246	0	–1	–1	–1	4	–1	–1	–1	–1	–1	–1
94	–1	–1	36	–1	–1	0	–1	–1	–1	–1	–1
–1	–1	101	–1	–1	–1	–1	–1	–1	0	–1	22
–1	–1	–1	–1	–1	251	–1	22	0	–1	–1	–1
–1	0	–1	–1	121	–1	–1	–1	–1	–1	194	–1
–1	–1	217	–1	0	–1	159	–1	–1	–1	–1	–1
–1	–1	–1	171	–1	109	–1	–1	–1	–1	–1	0
242	–1	–1	–1	–1	–1	–1	–1	–1	–1	3	0
–1	0	–1	–1	–1	–1	10	–1	–1	–1	–1	212
–1	–1	48	–1	–1	–1	–1	0	–1	140	–1	–1

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Table 142–3—Compact form of parity-check matrix H_c *(continued)*

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
–1	–1	–1	–1	–1	–1	–1	0	–1	46	43	–1
–1	–1	–1	228	0	–1	–1	–1	–1	–1	153	–1
129	–1	–1	–1	–1	140	–1	–1	–1	–1	–1	0
–1	–1	–1	–1	–1	–1	5	–1	0	58	–1	–1
19	–1	–1	–1	46	–1	–1	–1	0	–1	–1	–1
58	0	172	39	242	193	25	120	16	202	207	69
27	–1	42	234	228	241	94	192	0	215	109	88

NOTE—A CSV file containing the entire parity-check matrix H_c shown in Table 142–3 is available at https://standards.ieee.org/downloads/802.3/.

142.2.4.2 FEC encoding process

The FEC encoder is shown in Figure 142–5. The encoder consists of a systematic QC–LDPC encoding engine followed by a shortening and puncturing mechanism and the addition of a 10-bit delimiter. The parameters of the FEC encoder are as follows:

- The QC-LDPC parity-check matrix is a 12×69 array of circulant sub-matrices (see 142.2.4.1) with circulant size $Z = 256$; QC-LDPC user bit length before shortening is $57 \times 256 = 14\,592$, the parity bit length before puncturing is $12 \times 256 = 3072$; the codeword length before any shortening and puncturing is 17 664.
- The number of transmitted information bits, K (with maximum user length $K_{max} = 14\,392$).
- The number of shortened information bits, S ($S = 14\,592 - K$).
- The number of punctured parity-check bits, P ($P = 512$).
- The number of parity-check bits after puncturing, M ($M = 3072 - P = 2560$).
- The length of the FEC encoder output + delimiter is N where $N = K + M + 10$ bits and $N_{max} = K_{max} + M + 10$ bits = 16 962.
- The code rate, $R = K / N$, defined as the code rate after puncturing and after shortening.

The encoder supports a highest code rate $R_{max} = K_{max} / N_{max} = 0.848$. Codes with lower code rates/shorter block length shall be obtained through shortening. The puncturing length and location are fixed for all scenarios.

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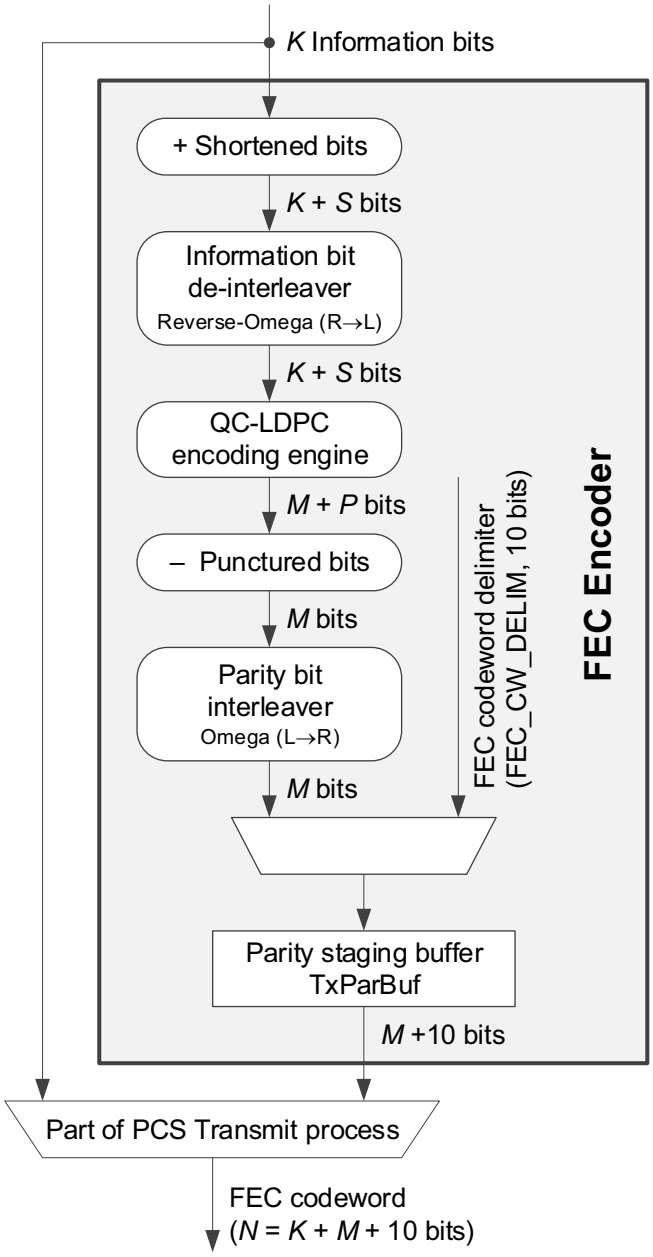

Figure 142–5—FEC encoder

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The encoding process therefore shall be as follows:

— A group of K information bits $u = [u_1, u_2, \ldots, u_K]$ are collected and copied to the output of the encoder to form a block of systematic code bits. They are also the input to the zero-padding block.
— A total of S zero padding bits are appended at the end of u to form the full-length information bit block $u^* = [u \mid 0, \ldots, 0]$, which is then sent to the information bit de-interleaver module, which in turn produces the bit-de-interleaved sequence $u'' = \pi^{-1}_{\text{info}}(u^*)$. π^{-1}_{info} represents the de-interleaver mapping of information bits that permutes u^* to u''.
— The de-interleaved QC-LDPC information bits u'' are sent to the QC-LDPC encoding engine, and used to compute parity-check bits p'' with the parity-check matrix H.
— $M + P$ parity bits $p'' = [p_1, p_2, \ldots, p_M \mid p_{M+1}, \ldots, p_{M+P}]$ are sent to the puncturing block. The last P bits of p'' are truncated, and M parity bits $p = [p_1, p_2, \ldots, p_M]$ are passed to the interleaver module.
— M parity bits p'' are interleaved to get $p^* = \pi_{\text{parity}}(\text{p''})$. π_{parity} represents the interleaver mapping of parity bits that permutes p'' to p^*.
— M interleaved parity bits $p^* = [p_1, p_2, \ldots, p_M]$ are copied to the output of the encoder to form the parity-check bits p.
— The FEC codeword without delimiter is $c = [u \mid p] = [u_1, u_2, \ldots, u_K \mid p_1, p_2, \ldots, p_M]$, such that $[u'' \mid p''] H^T = 0$.

The QC-LDPC encoder in Figure 142–5 places M bits of FEC parity into the parity staging buffer (TxParBuf) for use by the PCS Transmit process (see 142.2.5.4.3) and the FecParity() function. The buffer comprises 2560 bits of calculated parity along with the 10-bit codeword delimiter (FEC_CW_DELIM). This results in the parity bits assigned to TxParBuf<2559:0> and the 10-bit FEC_CW_DELIM value to TxParBuf<2569:2560>. The transmission order starts with bit 0 and ends with bit 2569.

142.2.4.3 Interleaver

The interleaver and de-interleaver are realized by using Omega networks and reverse Omega networks. An Omega network is a multi-stage interconnection network that uses multiple stages of switches. At each stage, the switches may be controlled independently to “pass-through” or “cross”.

The outputs from each stage are connected to the inputs of the next stage using an interconnection system. The details of interconnection and switch programming are shown in Figure 142–8.

“De-interleaver” refers to the mapping from transmitted sequence to encoding/decoding sequence (including user and parity). This is implemented using “reverse Omega (R→L)” (i.e., data input from the right side and output from the left). “Interleaver” refers to the mapping from encoding/decoding sequence to transmitted sequence. This is implemented as “Omega (L→R)” (i.e., data input from the left side and output from the right).

The information bit de-interleaver consists of 57 independent reverse Omega (R→L) networks of size 256 × 256 as illustrated in Figure 142–6. The information bits after zero padding are divided into 57 data chunks, and each data chunk has 256 bits, which is sent to one of the 256 × 256 reverse Omega (R→L) networks.

The parity bit interleaver consists of 10 independent Omega (L→R) networks (see Figure 142–7). Each 256-bit parity-check bit segment is sent to one of the 256 × 256 Omega (L→R) networks. Because the puncturing length is fixed (512) and 512 bits make up two whole data chunks, the last two parity Omega networks [B51] are bypassed. In implementation, the parity bit interleaver consists of 10 Omega networks.

Note that the interleaver (Omega L→R) and de-interleaver (reverse Omega R→L) are just reverse permutations of each other. To clarify, with the Omega (L→R) network architecture data is input from the

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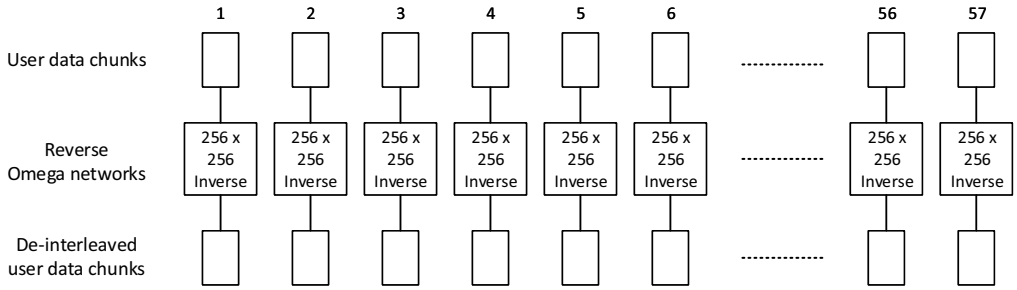

Figure 142–6—Information bit de-interleaver

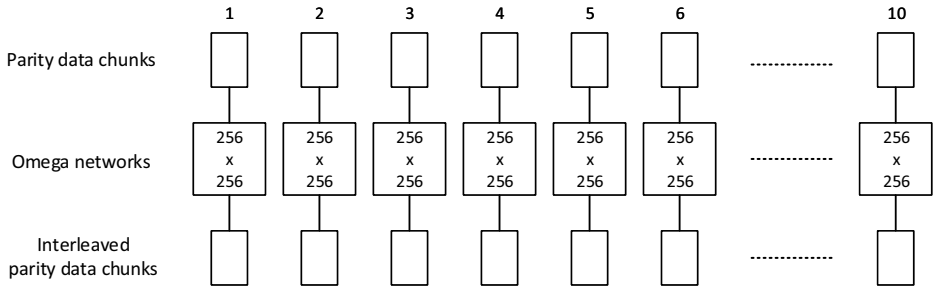

Figure 142–7—Parity bit interleaver

left side and output from the right; while the reverse Omega (R→L) network are obtained just by feeding the data to the right side and output from the left side. This is illustrated in Figure 142–8 where each Omega network is made of an interconnection network with 8 stages of switches, each stage has 128 switches, and each switch has two inputs and two outputs as shown. The inputs and outputs of switch i (i = 0...127) are connected to bits $i \times 2$ and $i \times 2 + 1$ of a 256-bit data chunk.

Each switch is individually programmed. If the switch is programmed to be 1, then this switch performs a swap of the input bits, otherwise, the input will be pass-through.

The interconnection between each stage of switches is deterministic and is described as follows. Denote the two output ports of switch i in stage k as $S^k_{i,0}$ and $S^k_{i,1}$, k = 0, …, 7 and i = 0, …, 127:

— Switch output port at stage k, $S^k_{i,0}$ is connected to switch input port at stage $k + 1$:

$$S^{k+1}_{\left\lfloor \frac{i}{2} \right\rfloor, \bmod(i,2)}$$

NOTE—The notation $\lfloor x \rfloor$ represents a floor function, which returns the value of its argument x rounded down to the nearest integer.

— Switch output port at stage k, $S^k_{i,1}$ is connected to switch input port at stage $k + 1$:

$$S^{k+1}_{\left\lfloor \frac{i}{2} \right\rfloor + 64, \bmod(i,2)}$$

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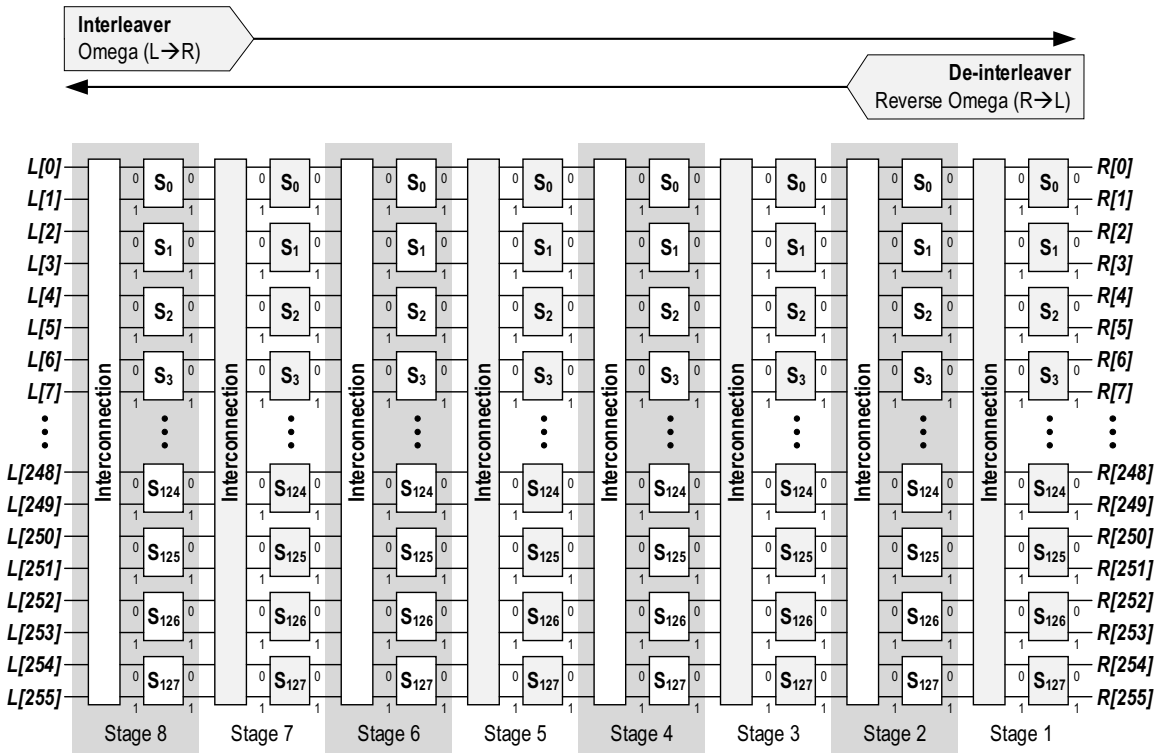

Figure 142–8—Omega network 256 interconnection network

In implementation one 256 × 256 Omega network of 8 × 128 switches is programmed based on a 128-bit control seed (see Table 142–5 and Table 142–6). The 128-bit switch programming sequence is derived by a circular bit shift of the control seed by *x* positions where *x* is given in Table 142–4 for each of the 8 stages.

Table 142–4—Control seed circular bit shift for stage 1 through 8

Stage	Circular shift *x* (bits)
1	17
2	34
3	51
4	68
5	85
6	102
7	119
8	8

The control seeds for the 57 independent user Omega networks are shown in Table 142–5 where each row is a 128-bit seed sequence.

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Table 142–5—User interleaver control seed values

User interleaver	128-bit control seed sequence (represented by a 32-character hex value)
1	0xE3-88-B0-9A-74-F4-94-8E-5D-C0-CC-8A-18-9A-B9-B2
2	0xC3-0A-B4-F4-92-08-FF-EA-24-FF-17-5D-94-96-70-72
3	0x88-31-C5-46-D3-EC-8B-9F-FF-48-44-9F-A9-4E-8F-20
4	0x92-43-32-87-0C-22-37-A3-E1-06-6A-9F-F8-F2-CC-1E
5	0x90-F6-C1-30-A0-3E-70-CF-60-81-79-53-6C-35-3F-7E
6	0x03-77-AA-71-8A-AC-D3-6D-1B-30-CA-20-D1-56-31-A9
7	0x97-28-EB-4E-AE-3B-93-6C-32-EA-07-9D-F8-18-47-EF
8	0xC1-E5-23-3A-D2-1A-92-00-B7-8B-34-65-90-E1-BD-40
9	0x8F-DC-FC-E6-E3-B0-EA-DF-96-42-7F-93-98-CE-3F-0C
10	0x3F-C4-29-23-C9-01-DE-E0-0B-BB-DD-19-40-B4-13-DA
11	0x42-95-0A-45-CF-AB-F1-6E-86-8D-96-F0-5E-F1-8F-7B
12	0x87-36-32-E9-5D-0D-99-BB-1F-57-46-5C-55-5E-E9-D2
13	0x05-11-38-7F-A6-EB-93-A2-43-91-96-F1-9C-EE-67-3A
14	0x4C-EF-11-A0-1D-FB-A0-5E-C0-01-9E-80-78-C1-B5-88
15	0x40-7C-C3-9F-D5-DE-6C-9A-C2-C0-1E-3B-45-FB-EE-B2
16	0xAE-FC-16-6F-9D-15-ED-E0-8C-7F-2B-14-74-85-36-14
17	0x8E-6D-B3-3B-C7-C8-9A-F9-08-AD-1D-C3-63-37-9B-43
18	0xE7-E0-B9-86-90-29-7B-7C-68-D8-6B-0E-52-79-8F-4F
19	0xA1-F1-78-71-4B-B7-D3-6B-13-41-90-A4-68-1C-88-8A
20	0x51-BD-15-AB-A9-88-5B-F8-11-C0-97-5C-FC-1B-65-E1
21	0xDA-5C-9A-8E-A2-F8-93-53-D9-F0-68-A5-F8-7F-2D-8E
22	0x31-69-A5-9D-01-B3-CD-B1-27-0C-8C-B5-E8-F7-A2-D2
23	0x04-E2-36-BE-89-46-7E-08-D5-63-DA-41-67-A2-DC-A5
24	0x4E-BB-16-BF-E6-19-C8-E3-44-98-AF-C4-88-18-53-B0
25	0xEF-BB-12-28-66-47-EC-22-C7-1D-F6-49-6F-BE-A0-3A
26	0x63-0F-7E-0F-AF-3C-47-15-2D-A7-20-E0-D2-EC-69-61
27	0x7C-3D-14-A5-BE-9E-E4-A4-71-64-BF-1B-71-C5-3E-D6
28	0xA4-66-0B-F8-27-EB-63-A4-C1-29-69-EC-81-D4-C0-89
29	0xF6-30-95-91-A5-F5-ED-B0-33-39-B6-72-75-CC-B1-93
30	0x13-93-BD-21-44-16-85-C3-5F-A1-A3-DE-89-A7-5B-A2
31	0xE2-32-7B-D2-31-11-CB-0E-D1-54-CC-59-E0-A4-55-4B
32	0x54-AC-4C-7E-58-74-32-DF-CE-54-F6-AE-65-F7-54-F8
33	0x7E-D1-D3-B8-7D-3A-1D-EF-DF-13-70-FB-6D-AF-79-49

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Table 142–5—User interleaver control seed values *(continued)*

User interleaver	128-bit control seed sequence (represented by a 32-character hex value)
34	0x27-CC-FF-46-F2-C9-4A-45-A9-35-80-D2-44-69-A4-CE
35	0x99-27-52-B8-96-3F-C0-90-98-9F-6D-A0-7C-FC-D3-B3
36	0x13-D3-9E-3C-5A-B4-AD-76-CF-8B-82-5F-E9-02-A5-EA
37	0xB3-AD-1C-D1-ED-F5-17-4B-AF-4B-07-54-F6-30-5E-81
38	0x22-76-62-36-B9-92-4F-83-AB-04-E7-37-B6-4C-D2-7D
39	0x5F-3C-DE-A1-05-AE-02-99-24-CC-A2-89-8D-57-C3-E7
40	0xAF-E4-7D-A0-B9-F6-CC-51-2D-B8-C9-FD-B6-8A-E9-B2
41	0x94-E7-58-DF-61-7B-DA-BF-C0-C4-72-15-C7-76-99-5C
42	0x34-64-0A-89-2E-46-63-46-C0-A8-26-FD-46-60-F3-C7
43	0x89-54-48-83-50-C6-B4-72-35-F4-C8-47-6C-2B-D2-50
44	0xFB-68-B2-9B-CA-E6-F1-50-4B-ED-AA-C9-9F-DC-77-66
45	0x08-34-F8-F3-5F-4A-B4-E5-49-85-F1-C7-91-BF-A7-6A
46	0x9D-C7-37-D5-C6-91-7C-D0-60-CC-66-3A-AF-A6-A7-91
47	0x01-89-6B-6C-8C-6E-35-B5-12-B4-BB-BC-41-AA-DF-EC
48	0xF0-73-F8-02-02-9B-8B-38-1B-78-F2-70-51-96-2A-5C
49	0x67-AE-64-C5-1B-B3-B0-CE-E6-89-B1-6F-B3-57-8C-80
50	0x84-C3-F1-40-85-82-DE-32-FB-43-EF-1C-A0-02-15-D4
51	0x6E-73-3D-34-85-62-EF-E1-F1-8F-C6-09-6D-19-B9-5A
52	0x57-89-78-DB-42-D9-19-C5-11-2A-79-B4-77-F7-E4-28
53	0x87-03-83-E6-F6-C6-A0-F3-D5-65-84-63-83-07-42-4A
54	0x4F-B7-69-FC-30-0E-5A-5B-0E-E8-D8-97-68-43-F0-74
55	0xCF-AF-92-E6-AA-BF-CE-5C-B3-F2-2E-03-02-F1-C8-EC
56	0x43-29-FB-56-A6-57-01-9F-91-3F-BA-7A-B0-A5-7F-B3
57	0x1C-61-92-BE-C8-C3-FA-E3-B5-8B-B8-D0-7A-9B-B1-D7

The control seeds for the 10 independent parity Omega networks are in Table 142–6 where each row is a 128-bit seed sequence.

NOTE—A file containing the interleaver seeds shown in Table 142–5 and Table 142–6 is available at https://standards.ieee.org/downloads/802.3/.

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Table 142–6—Parity interleaver control seed values

Parity interleaver	128-bit control seed sequence (represented by a 32-character hex value)
1	0x11-C7-DC-59-9A-61-76-D9-E3-44-BF-75-2E-AA-34-AF
2	0x5F-5C-F0-20-9A-E9-B4-4B-CD-F9-52-C8-22-8D-F0-89
3	0x89-34-9C-4B-F1-90-13-0B-F8-BE-47-6B-29-BB-96-3C
4	0xA2-6D-3B-8D-CC-B1-D9-C4-5E-FC-11-9F-AE-07-A6-C6
5	0xAC-45-29-CC-E5-2C-C7-D0-60-47-ED-32-76-4F-84-7B
6	0x92-3A-DC-97-5B-23-62-9A-FB-81-BE-93-EC-AB-25-BF
7	0x2C-4D-73-01-D3-01-D8-B8-9A-73-4A-3F-0A-E4-B6-F5
8	0xEF-CA-A9-2F-10-18-34-42-46-D4-BD-83-48-59-6A-BE
9	0x72-18-53-70-16-E0-84-4B-8E-D7-96-F8-07-AA-A5-8D
10	0x4D-F0-5D-35-75-9E-07-C9-56-6E-B1-4F-2B-22-43-90

142.2.5 Transmit data path state diagrams

Various variables and buffers in the PCS are structured as 258-bit wide blocks. Bits 0 through 256 of each 258-bit block hold one line-coding unit (a 257-bit block) and bit 257 indicates the 257-bit block has been scrambled and transcoded (bit 257 is equal to 1) or that the block has not been scrambled and transcoded (bit 257 is equal to 0). The value of bit 257 also implies the origin of the block as being either the PCS Input process (bit 257 is equal to 1) or the PCS Framer process (bit 257 is equal to 0).

142.2.5.1 Constants

EBD258
Type: 258-bit block
Description: The EBD258 constant holds the value of the end-of-burst delimiter.
Value: EBD257 (see 142.3.5.1) with a bit having value 0 appended as MSB

FEC_CW_DELIM
Type: 10-bit block
Description: The codeword delimiter bit pattern found at the end of each FEC parity block.
Value: 0x3-CA

FEC_PARITY_SIZE
Type: Integer
Description: The FEC_PARITY_SIZE constant indicates the size of the parity portion of an FEC codeword.
Value: 10
Unit: 257-bit block

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FEC_PAYLOAD_SIZE
Type: Integer
Description: The FEC_PAYLOAD_SIZE constant indicates the size of the payload portion of an FEC codeword.
Value: 56
Unit: 257-bit block

IBI258
Type: 258-bit block
Description: The IBI258 constant represents an inter-burst idle block that is generated by the PCS Framer process in the absence of any burst framing blocks, data blocks, or FEC parity blocks.
Value: $0x0\text{-}(0A)_{32}$

IBI_EQ
See 143.3.3.3

PAR_PLACEHLDR
Type: 258-bit block
Description: The PAR_PLACEHLDR constant represents the value of a 258-bit block inserted into the data stream by the PCS Framer process in order to reserve the location where FEC parity and the 10-bit FEC codeword delimiter is to be inserted into the data stream by the PCS Transmit process.
Value: $0x0\text{-}(09)_{32}$

RATE_ADJ_EQ
See 143.3.3.3

SCRAMBLED
Type: binary
Description: This constant indicates that the contents of the 257-bit block are scrambled. When the bit TxInput<257> or TxOutput<257> is set to 1, then bits TxInput<256:0> or TxOutput<256:0> in the same block carry scrambled data.
Value: 1

142.2.5.2 Variables

BEGIN
TYPE: Boolean
Description: This variable is used when initiating operation of the functional block state diagram. It is set to true following initialization and every reset, and it is reset to false on read.

ClkIn
Type: Boolean
Description: The clear-on-read variable ClkIn is set to true on each rising edge of the xMII clock.

ClkOut
Type: Boolean
Description: The clear-on-read variable ClkOut is set to true once for each 257-bit block output by the PMA, i.e., the ClkOut tracks the transmit clock of the corresponding PMA channel (see 142.4.4).

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ClkXfr

Type: Boolean

Description: The clear-on-read variable ClkXfr is set to true once for each 257-bit block output by the PMA, i.e., the ClkXfr tracks the transmit clock of the corresponding PMA channel (see 142.4.4).

InputFifo[]

Type: array of 258-bit blocks

Description: The InputFifo receives data from the PCS Input process and hands it off to the PCS Framer process. Its primary function is to absorb data while the PCS is transmitting burst overhead or FEC parity. This FIFO holds SpLength elements and supports FIFO access operations as defined in 142.1.1.6.

TxParBuf

Type: 2570-bit block

Description: This variable holds the 2560-bit calculated parity value along with the 10-bit FEC_CW_DELIM value (see 142.2.5.1). The total size of 2570 bits represents the same size as ten 257-bit line encoding blocks.

TxFifo[]

Type: array of 258-bit blocks

Description: The TxFifo holds information queued by the Framer process for output by the PCS and enforces a fixed delay that is implementation dependent. The fixed delay ensures the PHY has sufficient time to generate FEC parity given that the Framer process inserts SpLength 257-bit blocks at the beginning of the burst. This FIFO holds either (FEC_DELAY – SpLength) or two elements, whichever is greater. The TxFifo supports FIFO access operations as defined in 142.1.1.6.

ParityLeft

Type: Integer

Description: The ParityLeft variable indicates the number of 257-bit parity blocks needed to complete the current FEC codeword being processed by the PCS Framer process.

PayloadLeft

Type: Integer

Description: The PayloadLeft variable indicates the number of 257-bit payload blocks needed to complete the current FEC codeword being processed by the PCS Framer process.

SyncPattern[]

Type: array of 258-bit blocks

Description: The SyncPattern array is set to the provisioned value of the synchronization pattern as determined by the most recent settings of SP1, SP2, SP3, and their corresponding length parameters by the MPCP. The MSB of each cell is set to zero, indicating the 257-bit block has not been scrambled and transcoded.

SpLength

Type: unsigned integer

Description: The SpLength variable represents the length of the synchronization pattern as determined by the sum of the most recent settings of SP1Length, SP2Length, and SP3Length provisioned in an ONU (see 144.3.6.4 and 144.3.6.6).

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SpIndex
: Type: integer
Description: The SpIndex variable is a pointer into the SyncPattern array that indicates which 258-bit block from the array is sent to the TxFifo.

Transmitting
: Type: Boolean
Description: The Transmitting variable indicates whether the device is transmitting or not.

TxInput
: Type: 258-bit block
Description: This variable holds one transcoded 257-bit block prepended with a binary 1 indicating the 257-bit block has been scrambled and transcoded.

TxNext
: Type: 72-bit block
Description: The next 72-bit block to be processed by the PCS Input process.

TxLast
: Type: 258-bit block
Description: This variable holds the 258-bit that was read from TxFifo in the previous ClkOut cycle.

TxOutput
: Type: 258-bit block
Description: This variable holds one 258-bit block retrieved from the TxFifo.

TxPrev
: Type: 72-bit block
Description: This variable holds one 72-bit block received by the PCS Input process from the xMII in the previous ClkIn cycle.

xBuffer[]
: Type: array of 66-bit blocks
Description: This buffer holds four 66-bit blocks of 64B/66B encoded data to be transcoded into one 257-bit block.

xIndex
: Type: Integer
Description: An index into the xBuffer indicating the number of encoded blocks contained in the buffer that are ready to be transcoded.

142.2.5.3 Functions

FecParity()
: Upon initiation, the first call to this function returns a block containing the first 257 bits from the TxParBuf, i.e., TxParBuf<256:0>. Each subsequent call returns the subsequent 257 bits from the buffer. On the 10th call, the last 257 bits are returned, i.e., TxParBuf<2569:2312>, and the function resets to return TxParBuf<256:0> on the next call. This emulates a circular buffer of size 10 × 257 bits.

Encode(v)
: This function performs 64B/66B encoding of a 72-bit block v per 49.2.13.2.3 and returns the result.

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PassToFecEncoder(v)

This function passes a 257-bit block v to the FEC engine for calculating the LDPC code parity.

NextTxVector()

This function returns a 72-bit block carrying a single EQ as shown in Figure 142–2. The block is constructed from the data received from the xMII over two subsequent 36-bit transfers: the first transfer is on rising TX_CLK edge and the second transfer is on the falling TX_CLK edge.

PassToPMA(v)

This function passes a 257-bit block v to the PMA using PMA_UNITDATA[*i*].request(v) (see 142.4.1.1).

ResetScrambler()

Description: This function resets the scrambler to the value of $0x3\text{-}(FF)_7$, i.e., each of the bits S0 through S57 of the scrambler shift register is set to 1 (see Figure 49–8).

Scramble(blk)

This function accepts one 66-bit block blk and performs the scrambling operation on the 64-bit payload of the block, as described in 49.2.6. The returned value is a scrambled 66-bit block.

Transcode(a[4])

This function transcodes four 64B/66B-encoded blocks into a single 256B/257B encoded block per 91.5.2.5 and returns the result. It takes four 64B/66B encoded blocks a[4] as an argument and returns a 257-bit block.

142.2.5.4 State diagrams

142.2.5.4.1 PCS Input process

The PCS Input process accepts two consecutive 36-bit transfers from the xMII interface and converts them into a single 72-bit block. The Input process discards all RATE_ADJ_EQs to allow for insertion of FEC parity blocks by the PCS Transmit process (see 142.2.5.4.3). IBI_EQs not required to complete a 256B/257B block at the end of an upstream burst are also discarded by the Input process. All other 72-bit blocks are encoded into 64B/66B blocks. Four 64B/66B blocks are accumulated, scrambled, and transcoded into a single 256B/257B block and copied to the FEC encoder. A single bit indicating the accompanying 256B/257B block has been scrambled and transcoded is appended to the block that is then stored in the InputFifo.

The PCS Input process shall implement the state diagram as depicted in Figure 142–9.

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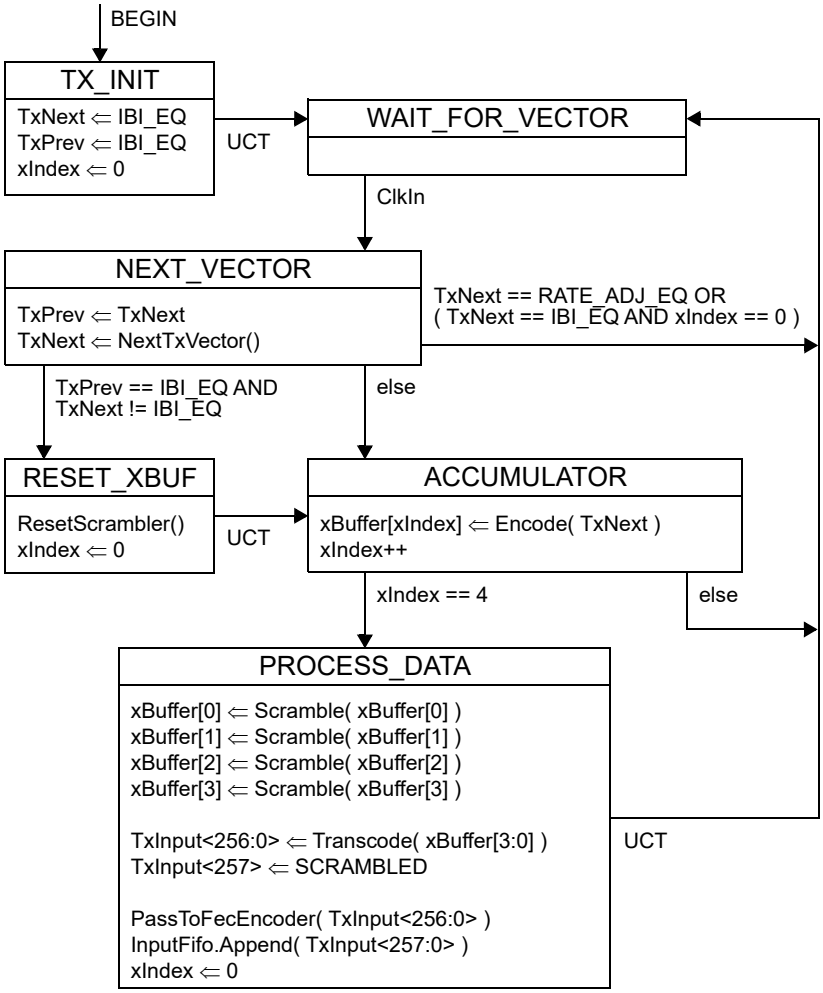

Figure 142–9—PCS Input process state diagram

142.2.5.4.2 PCS Framer process

The PCS Framer process monitors data from the InputFifo and transfers it to the TxFifo, inserting inter-burst idle blocks (IBI258), SyncPattern, parity placeholders (PAR_PLACEHLDR), and EBD258 as appropriate. While the InputFifo is empty, the PCS Framer process appends IBI258 to the TxFifo. When the InputFifo first becomes not empty, indicating the beginning of a burst, the SyncPattern is appended to the TxFifo. Once the complete SyncPattern is appended to the TxFifo, the Framer process begins transferring data from the InputFifo to the TxFifo. When sufficient data for a full FEC payload has been transferred to the TxFifo, or the end of the burst is detected as indicated by an empty InputFifo, the PCS Framer process appends sufficient PAR_PLACEHLDR blocks to the TxFifo to allow insertion of the contents of TxParBuf (FEC codeword parity and FEC codeword delimiter) into the data stream by the PCS Transmit process. Additional FEC codewords are allowed for until the end of the transmission is indicated by an empty InputFifo, at which point the Framer process appends the EBD258 to the TxFifo followed by IBI258.

The PCS Framer process shall implement the state diagram as depicted in Figure 142–10.

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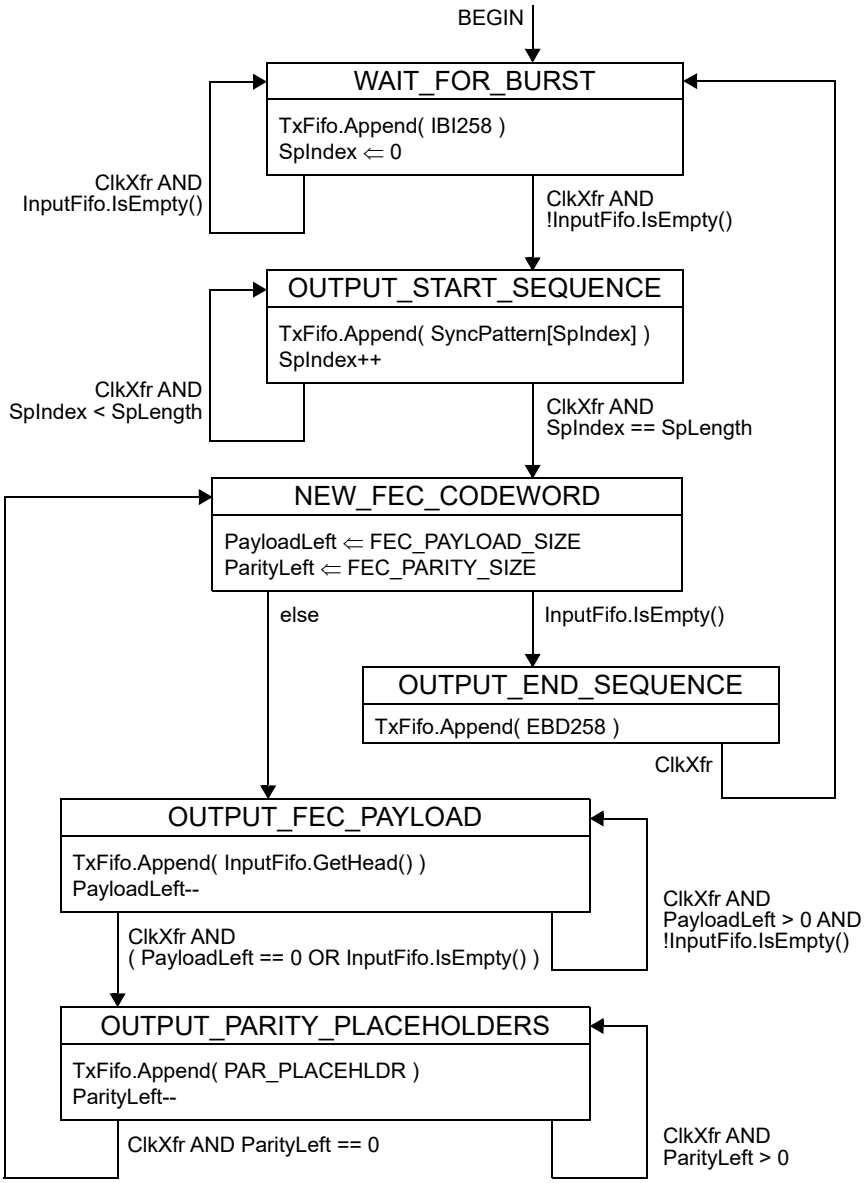

Figure 142–10—PCS Framer process state diagram

142.2.5.4.3 PCS Transmit process

The PCS Transmit process transfers data from the TxFifo or FEC encoder to the PMA. On each transition of the ClkOut to true the Transmit process retrieves one 258-bit block of data from the TxFifo. If the retrieved 258-bit block indicates the start of the burst and the ONU is currently not transmitting, the laser is turned on and data is sent towards the PMA for transmission. If the retrieved 258-bit block indicates the end of the burst and the ONU is currently transmitting, the laser is turned off and end of the burst delimiter is sent towards the PMA for transmission. If the retrieved 258-bit block indicates the FEC parity placeholder, the calculated FEC parity and 10 bits of FEC codeword delimiter are sent towards the PMA for transmission. Otherwise, data from the TxFifo is sent towards the PMA for transmission.

The PCS Transmit process shall implement the state diagram as depicted in Figure 142–11.

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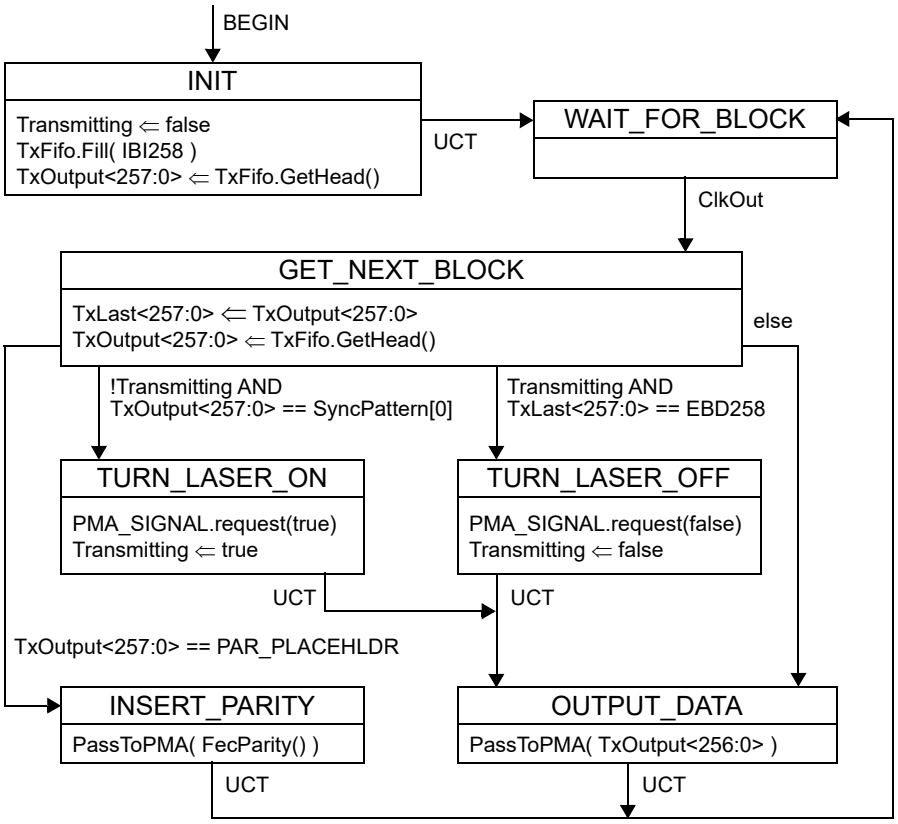

Figure 142–11—PCS Transmit state diagram

142.3 PCS receive data path

This subclause defines the PCS receive data path. In the ONU, the PCS receive data path operates in a continuous mode at a 25.78125 GBd rate. In the OLT, the PCS receive data path operates in burst mode at a 25.78125 GBd rate (25/25G-EPON, 50/25G-EPON, and 50/50G-EPON) or at a 10.3125 GBd rate (25/10G-EPON and 50/10G-EPON). The PCS receive data path includes a mandatory QC-LDPC FEC decoder (see 142.3.1.1).

The functional block diagram for the PCS receive data path is shown in Figure 142–2 and consists of the following processes:

— PCS Synchronizer process (see 142.3.5.4 and 142.3.5.5)
— PCS BER Monitor process (see 142.3.5.6)
— PCS Output process (see 142.3.5.7)

142.3.1 FEC decoder

Figure 142–12 illustrates the receiver QC-LDPC decoder with shortening/puncturing, interleaver/de-interleaver data path.

142.3.1.1 Receive interleaving

See 142.2.4.3.

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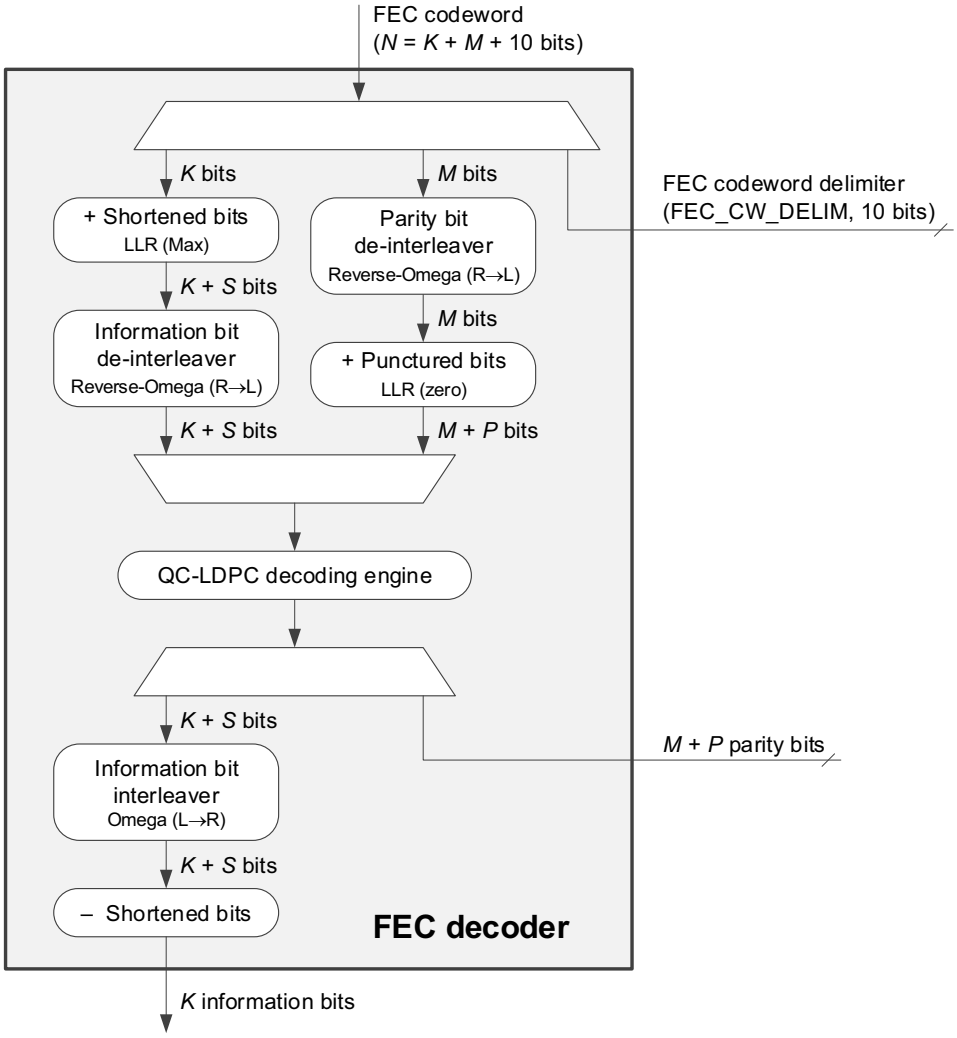

Figure 142–12—FEC decoder

142.3.2 256B/257B to 64B/66B transcoder

The 256B/257B to 64B/66B transcoder converts one scrambled 257-bit block received from the FEC decoder into four consecutive scrambled 66-bit blocks as described in 91.5.3.5 and returns the result to the PCS Output process.

142.3.3 Descrambler

The PCS uses the descrambler specified in 49.2.10.

In the OLT, at the beginning of each burst, the descrambler is reset to a known initialization value (see the definition of ResetDescrambler() function in 142.3.5.3).

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142.3.4 64B/66B decoder

See 49.2.11. The 64B/66B decoder shall perform functions specified in the state diagram shown in Figure 49–17. The PCS bit reception order is illustrated in Figure 142–13.

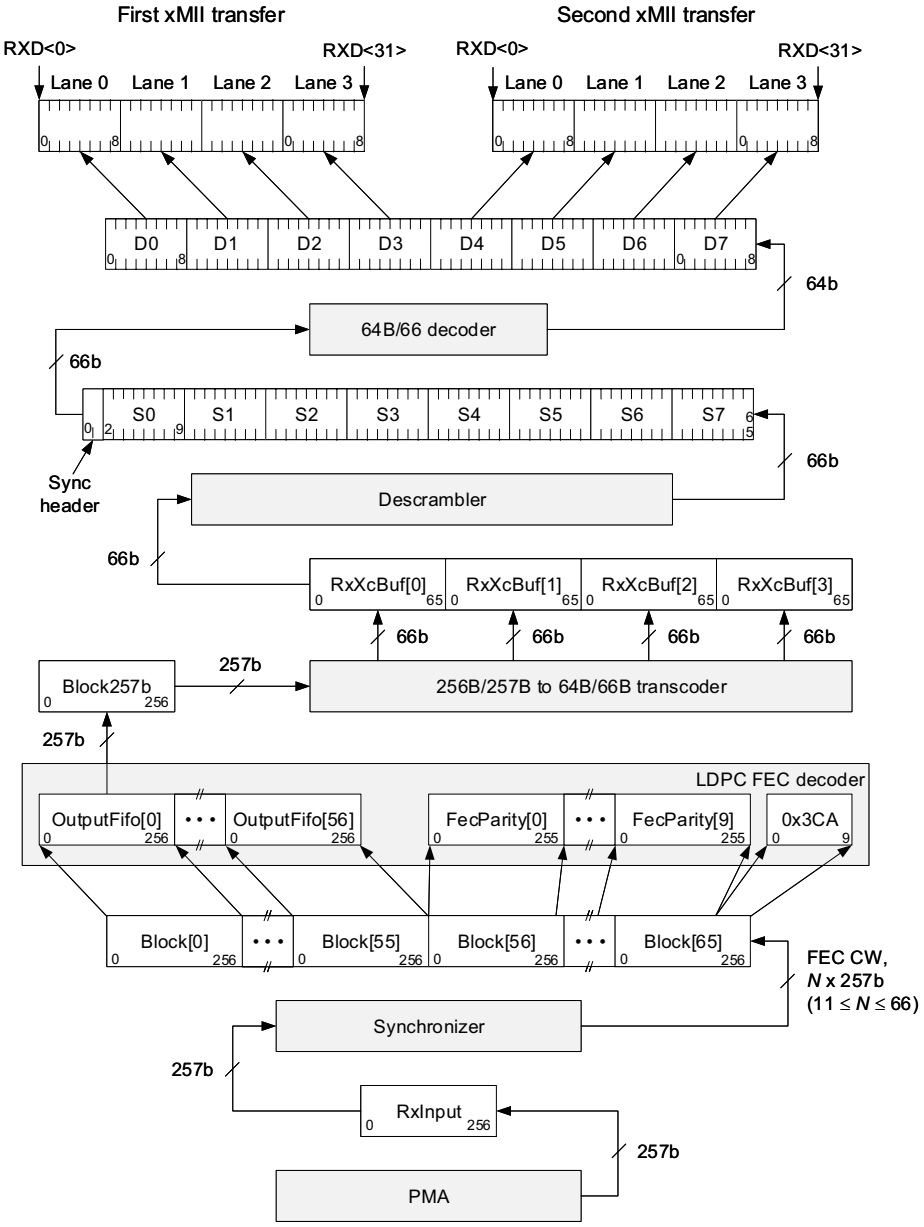

Figure 142–13—PCS receive bit ordering

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142.3.5 Receive data path state diagrams

142.3.5.1 Constants

EBD257
Type: 257-bit block
Description: The EBD257 constant holds the value of the end-of-burst delimiter.
Value: A single 0 bit followed by 0x0F–10–$(01–EE–E8–02–D3–CA)_3$–$(EB–D2–57)_4$

NOTE—The transmission bit order is as defined in SBD257 (see 142.1.3.1).

EBD_TH
Type: Integer
Description: The EBD_TH constant holds the value of the Hamming threshold required to match the end-of-burst delimiter.
Value: 36

FEC_CW_DELIM
See 142.2.5.1

FEC_PAYLOAD_SIZE
See 142.2.5.1

FEC_CW_BIT_SZ
Type: Integer
Description: This constant represents the size of a full-length FEC codeword in bits.
Value: 16 962 (i.e., 257 × 66)

IBI_EQ
See 143.3.3.3.

MATCH_TARGET
Type: Integer
Description: The number of FEC codeword delimiters required to match in order to declare the block alignment in the ONU (i.e., in the continuous reception mode).
Value: 4

PCS_BLK_SZ
Type: Unsigned integer
Description: The PCS_BLK_SZ constant holds the size of the PCS data block.
Value: 257
Unit: bits

RATE_ADJ_EQ
See 143.3.3.3

RATE_ADJ_SIZE
See 143.3.3.3

SBD_TH
Type: Integer
Description: The SBD_TH constant holds the value of the Hamming threshold required to match

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the start-of-burst delimiter.
Value: 60

142.3.5.2 Variables

All variable definitions in this section assume an independent instance of the variable per each enabled receive channel.

BadCwCount
: Counts the number of invalid QC-LDPC codewords within the current BER monitoring interval period.

BEGIN
: See 142.2.5.2

BerMonitorInterval
: Indicates the length of the interval window period associated with the QC-LDPC BER Monitor in units of QC-LDPC codewords (see 45.2.3.43). This value is reflected in MDIO register 3.80.

BerThreshold
: Indicates the threshold value of invalid QC-LDPC codeword errors within the QC-LDPC BER Monitor function. At the end of each monitor interval period, HiBer is updated. The value of BerThreshold is reflected in MDIO register 3.82

Block257b
: Type: 257-bit block
Description: The Block257b variable temporarily holds one 257-bit block removed from the head of OutputFifo.

Block66b
: Type: 66-bit block
Description: The Block66b variable temporarily holds one descrambled 66-bit block.

Block72b
: Type: 72-bit block
Description: The Block72b variable temporarily holds the value being passed to the xMII.

CwAvailable
: Boolean variable that is set true when a new QC-LDPC codeword is available for testing by the BER Monitor process and set to false when the WAIT_FOR_CODEWORD state is entered. A new QC-LDPC codeword is available for testing by the BER Monitor process when the ONU Synchronizer process has accumulated enough blocks from the PMA to evaluate the next QC-LDPC codeword (see Figure 142–15).

CwLeft
: Counts the remaining number of QC-LDPC codewords within the current BER monitoring interval.

CwValid
: Boolean indication that is set true if a received QC-LDPC codeword is valid. As an example, a QC-LDPC codeword is valid if and only if all parity checks of the QC-LDPC code are satisfied thereby terminating iterations without exceeding the maximum count (e.g., 15). The specific method for evaluating codeword validity is implementation dependent within the QC-LDPC decoder and outside the scope of this standard.

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HiBer

Boolean variable that is asserted true if BadCwCount reaches or exceeds BerThreshold QC-LDPC codeword errors within one BER monitor interval period, otherwise set to false. The value of HiBer is reflected in MDIO register 3.81.

MatchCount

Type: Integer

Description: This counter tracks the number of consecutive successful detections of FEC codeword delimiters (FEC_CW_DELIM) while the ONU is not synchronized to the proper 257-bit block boundary.

OutputFifo[]

Type: Array of 257-bit blocks

Description: The OutputFifo buffer holds one FEC codeword payload after it has been processed by the FEC decoder. The OutputFifo supports FIFO access operations as defined in 142.1.1.6.

PayloadLeft

Type: Integer

Description: This variable holds the number of EQs remaining until one maximum-length FEC codeword payload has been sent to the xMII.

PersistentFecFail

Type: Boolean

Description: This variable is set to true if the FEC decoder is unable to correct all errors in the three FEC codewords most recently received on a given channel. Otherwise, this variable is set to false. In the OLT, the PersistentFecFail value is reset when SignalFail becomes true, or the EBD is detected, i.e., the uncorrectable FEC codewords from the previous burst do not result in PersistentFecFail becoming true during the next burst.

RateAdjLeft

Type: Integer

Description: This variable holds the number of EQs remaining to be generated in the PCS Output process to fill the gap left by the removal of FEC codeword parity data from the current FEC codeword.

RxCwBuf[]

Type: An array of 257-bit blocks

Description: The RxCwBuf is a buffer capable of storing one full FEC codeword. The RxCwBuf supports FIFO access operations as defined in 142.1.1.6.

RxInput

Type: 257-bit block

Description: The RxInput is a buffer containing the 257 bits most recently received from the PMA sublayer on a given channel.

RxXcBuf[3:0]

Type: Array of four 66-bit blocks

Description: This buffer holds four 66-bit blocks resulting from the decoding of a 257-bit block.

SBD257

Type: 257-bit block

Description: The SBD257 variable represents the start-of-burst delimiter, and its value is equal to

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SP3 for the most recently provisioned synchronization pattern (see 142.1.3.1).
Value: see 142.1.3.1

SignalFail
Type: Boolean
Description: This Boolean variable is set based on the most recently received value of PMA_SIGNAL.indication(SIGNAL_OK) received on a given channel. It is true if the value of SIGNAL_OK was FAIL and false if the value was OK.

XcIndex
Type: Integer
Description: The XcIndex variable is an index to the RxXcBuf array and has a value ranging between 0 and 3, inclusive.

142.3.5.3 Functions

Decode257b(blk)
Description: This function accepts one 256B/257B encoded block blk and transcodes it into four 64B/66B encoded blocks. The result is returned as an array of four 66-bit blocks.

Decode66b(blk)
Description: This function accepts one 64B/66B encoded block blk and performs the decoding operation as described in 49.2.11 and Figure 49–17. The returned value is a 72-bit block.

Descramble(blk)
Description: This function accepts one 66-bit block blk and performs the descrambling operation on the 64-bit payload of the block, as described in 49.2.10. The returned value is a descrambled 66-bit block.

PassToFecDecoder(cw)
Description: The PassToFecDecoder function passes one complete FEC codeword cw to the FEC decoder. The FEC codeword may be full-length or shortened. The codeword length is intrinsic to the parameter cw.

MatchFound(value1, value2, threshold)
Description: This function compares bit by bit its arguments value1 and value2 and returns a Boolean true if the number of bits that are different is less or equal to the threshold, otherwise the function returns false.

OutputBlock(eq)
Description: This function accepts one 72-bit block eq and outputs two 36-bit blocks over the xMII. This is a blocking function and the control is not returned to the calling state until after the second 36-bit block is sent.

ResetDescrambler()
Description: This function resets the descrambler to the value of $0x3\text{-}(FF)_7$, i.e., each of the bits S0 through S57 of the descrambler shift register is set to 1 (see Figure 49–10).

Shift(buffer, *n*)
Description: This function receives 257-bit blocks from the PMA via the PMA_UNITDATA.indication(rx_code_group<256:0>) primitive and inserts *n* new bits at the end of the FIFO buffer, while removing the same number of old bits at the head of the buffer. The Shift() function is blocking and its execution takes exactly *n* bit times at the given receiving line rate.

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142.3.5.4 OLT Synchronizer process state diagram

The OLT Synchronizer process is responsible for receiving unaligned 257-bit blocks from the PMA sublayer and aligning these blocks to the correct 257-bit block boundary. This process hunts for SBD257 and EBD257 values, allowing for a certain Hamming distance (see SBD_TH and EBD_TH). The 257-bit blocks that are received between the SBD and the EBD are accumulated in the RxCwBuf buffer. When a complete full-length or shortened FEC codeword is stored in the RxCwBuf, the buffer content is passed to the FEC decoder function (see 142.3.1).

The OLT shall implement an instance of the Synchronizer process as depicted in Figure 142–14 for every enabled receive channel.

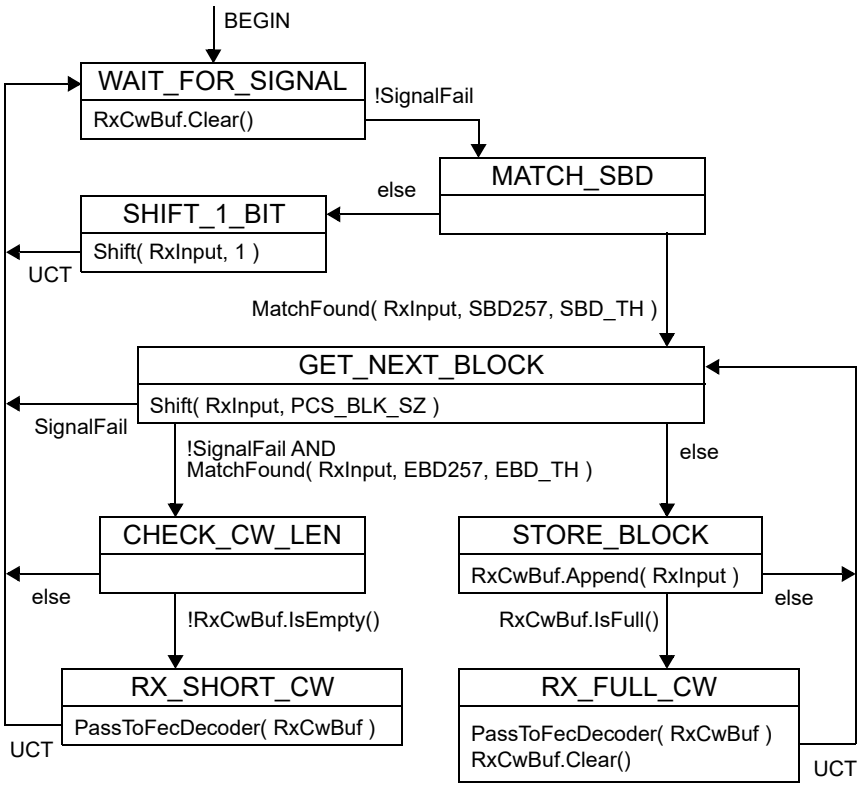

Figure 142–14—OLT Synchronizer process state diagram

142.3.5.5 ONU Synchronizer process state diagram

The ONU Synchronizer process is responsible for receiving unaligned 257-bit blocks from the PMA sublayer and aligning these blocks to the correct 257-bit block boundary. This process hunts for 10-bit FEC codeword delimiters FEC_CW_DELIM. The delimiter is expected to have the exact match and the block alignment is declared when the FEC_CW_DELIM values are matched MATCH_TARGET times and are exactly one FEC codeword size apart.

The received blocks are accumulated in the RxCwBuf buffer. When a complete full-length FEC codeword is stored in the RxCwBuf, the buffer content is passed to the FEC decoder function (see 142.3.1). In the ONU receive path, shortened FEC codewords are disallowed.

The ONU shall implement an instance of the Synchronizer process as depicted in Figure 142–15 for every enabled receive channel.

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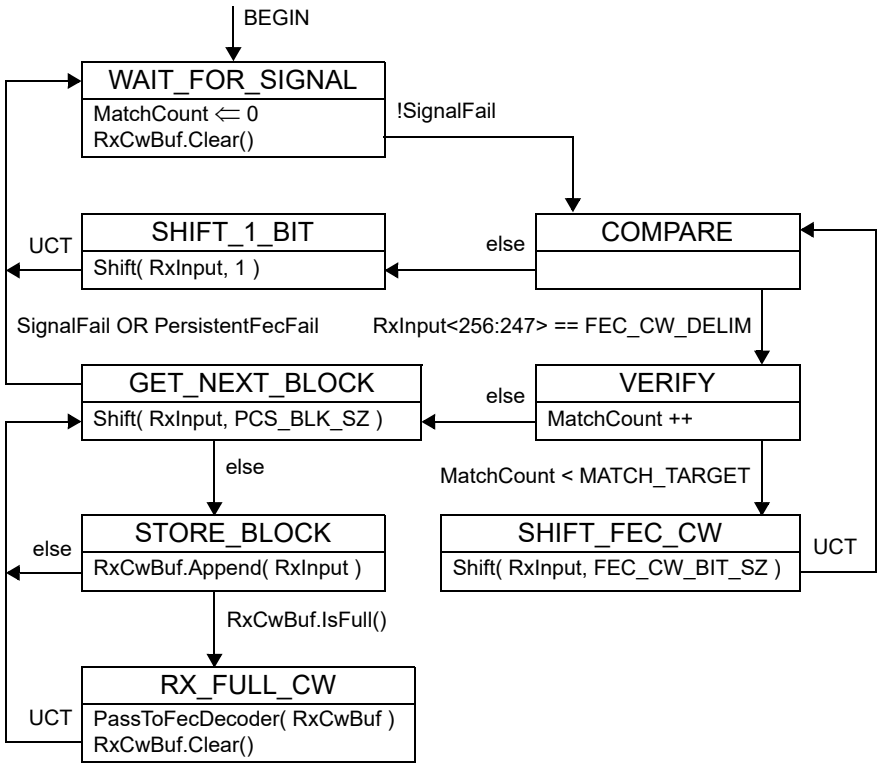

Figure 142–15—ONU Synchronizer process state diagram

142.3.5.6 PCS ONU BER Monitor process

When the ONU Synchronizer process has obtained block synchronization, the QC-LDPC BER Monitor process monitors the signal quality, asserting HiBer if a count of QC-LDPC parity errors reaches BerThreshold within the timer interval. The ONU shall implement an instance of the QC-LDPC BER Monitor shown in Figure 142–16 for each active downstream channel.

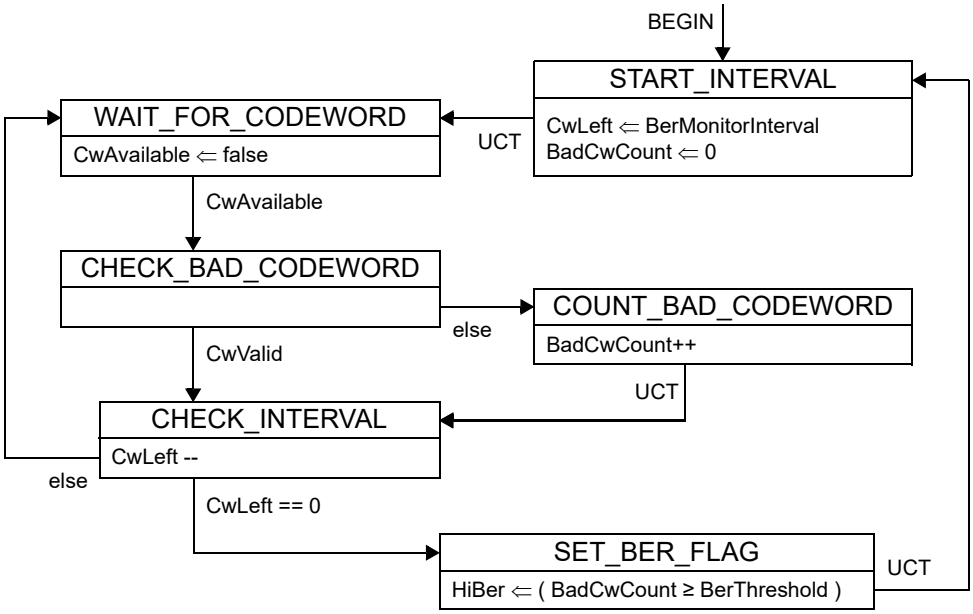

Figure 142–16—QC-LDPC BER Monitor state diagram (ONU only)

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142.3.5.7 PCS Output process

The PCS Output process receives corrected information bits from the FEC decoder. The FEC decoder outputs an entire payload of an FEC codeword into the OutputFifo buffer. The FEC codeword payload consists of 56 257-bit blocks, however, in the OLT, the payload of a last codeword in a burst may contain fewer than 56 blocks.

The PCS Output process converts the 257-bit blocks into EQs by first transcoding each 257-bit block into four 66-bit blocks, then descrambling each block, and finally, decoding each 66-bit block into a 72-bit block. The 72-bit blocks are passed to xMII for transfer to the MCRS.

The PCS shall implement an instance of the Output process as depicted in Figure 142–17 for every enabled receive channel.

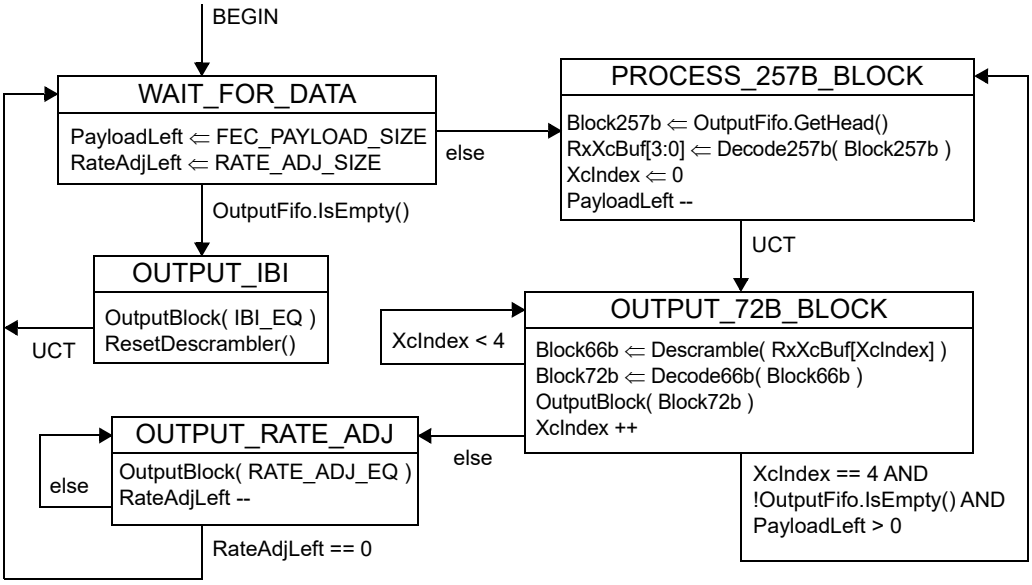

Figure 142–17—PCS Output process state diagram

142.4 Nx25G-EPON PMA

The PMA adapts the serial PMD service interface (PMD_UNITDATA, see 141.3.3 and 141.3.4) to the 257-bit wide interface of the PCS (PMA_UNITDATA, see 142.4.1). Where Nx25G-EPON operates over multiple channels, the PMA sublayer includes multiple identical instances of the transmit data path and/or the receive data path.

In the downstream direction (from the OLT to the ONUs), the PMA includes a differential encoding option (see 142.4.2 and 142.4.3). This encoding technique facilitates the use of lower bandwidth receivers at the ONUs.

142.4.1 Service Interface

The PMA provides a service interface to the PCS. These services are described in an abstract manner and do not imply any particular implementation. The PMA service interface supports the exchange of 257-bit single data-unit vectors between PCS entities. The PMA converts 257-bit single data-unit vectors into bits and passes these to the PMD, and vice versa.

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The following primitives are defined:

— PMA_UNITDATA[*i*].request(tx_code_group<256:0>)
— PMA_UNITDATA[*i*].indication(rx_code_group<256:0>)
— PMA_SIGNAL[*i*].request(tx_enable)
— PMA_SIGNAL[*i*].indication(SIGNAL_OK)

where "[*i*]" represents the PMA Channel: 0 or 1.

142.4.1.1 PMA_UNITDATA[*i*].request

This primitive defines the transfer of data (in the form of 257-bit single data-unit vectors) from the PCS to the PMA by the PCS Transmit process, see 142.2.

142.4.1.1.1 Semantics of the service primitive

PMA_UNITDATA[*i*].request(tx_code_group<256:0>)

Data is conveyed to PMA_UNITDATA[*i*].request() as described in the PCS Transmit state diagram via the PassToPMA function, see Figure 142–11.

142.4.1.1.2 When generated

The PCS continuously sends tx_code_group<256:0> single data-unit vectors to the PMA according to the PMA transmit clock at either (25.78125 / 257) GHz or (10.3125 / 257) GHz as defined in 142.4.4.

142.4.1.1.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a serial bit stream for conveying data to the PMD using PMD_UNITDATA[*i*].request(tx_bit), see 141.3.1.2.

142.4.1.2 PMA_UNITDATA[*i*].indication

This primitive defines the transfer of data (in the form of 257-bit single data-unit vectors) from the PMA to the PCS. PMA_UNITDATA[*i*].indication is used by the PCS receive path processes, see 142.3.5.

142.4.1.2.1 Semantics of the service primitive

PMA_UNITDATA[*i*].indication(rx_code_group<256:0>)

The data conveyed by PMA_UNITDATA[*i*].indication is the rx_code_group<256:0> parameter that is used in the Shift() function (see 142.3.5.3). Shift() is used in the OLT Synchronizer process, see Figure 142–14, and in the ONU Synchronizer process, see Figure 142–15.

142.4.1.2.2 When generated

The PMA continuously sends rx_code_group<256:0> single data-unit vectors to the PCS according to the PMA transmit clock at either (25.78125 / 257) GHz or (10.3125 / 257) GHz as defined in 142.4.4.

142.4.1.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

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142.4.1.3 PMA_SIGNAL[*i*].request

This primitive is used to turn the laser on and off at the PMD sublayer. In the OLT, this primitive shall always take the value ON. In the ONU, the value of this variable is controlled by the PCS Transmit function, see Figure 142–11.

142.4.1.4 PMA_SIGNAL[*i*].indication

PMA_SIGNAL[*i*].indication is generated by the PMA receive process to propagate the loss of optical signal from the PMD sublayer to the PMA client.

142.4.1.4.1 Semantics of the service primitive

PMA_SIGNAL[*i*].indication (SIGNAL_OK)

The SIGNAL_OK parameter can take one of two values: OK or FAIL. A value of FAIL denotes that invalid data is being presented to the PMA client. A value of OK does not guarantee valid data is being presented to the PMA client.

142.4.1.4.2 When generated

The PMA generates a PMA_SIGNAL[*i*].indication primitive to the PMA client whenever there is change in the value of the SIGNAL_OK parameter.

142.4.1.4.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

142.4.2 Differential encoder

Differential encoding as shown in Figure 142–18 shall be implemented in the transmit path of the OLT PMA. The use of differential encoding is optional. Setting the MDIO control bit 1.29.15 (see 45.2.1.27.1) to a one enables the differential encoding.

X_i = Input serial bit stream from OLT PCS FEC encoder
Y_i = Output serial bit stream to OLT PMD

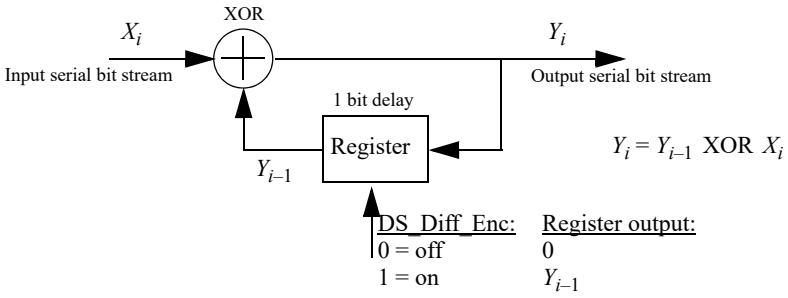

Figure 142–18—Differential encoding

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142.4.3 Differential decoder

Differential decoding shall be implemented in the receive path of the ONU PMA as shown in Figure 142–19. The ONU shall implement automatic detection of receive path differential encoding, and switch in the decoder as appropriate. The DS_Diff_Enc bit is mapped to Clause 45 bit 1.29.15 (see 45.2.1.27.1). This bit is controlled by a local differential encoding detection function (outside the scope of this standard).

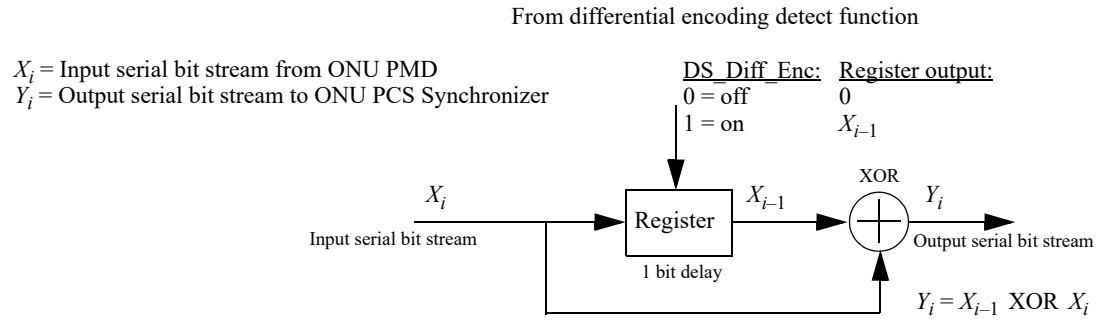

Figure 142–19—Differential decoding

142.4.4 PMA transmit clock

The data conveyed by PMA_UNITDATA.request() is a 257-bit vector representing a single data unit, which has been prepared for transmission by the PMA client. For the PMA devices transmitting at 25.78125 GBd, the PMA transmit clock is equal to (25.78125 / 257) GHz. For the PMA devices transmitting at 10.3125 GBd, the PMA transmit clock is equal to (10.3125 / 257) GHz. In PMA devices supporting multiple transmit channels, the transmit clocks for all channels are phase aligned.

142.4.4.1 Loop-timing specifications for ONUs

ONUs shall operate at the same time basis as the OLT, i.e., the ONU PMA transmit clock tracks the ONU PMA receive clock. Jitter transfer masks are defined in 141.6.2. For the ONUs supporting 10G transmission (i.e., 25/10G-EPON and 50/10G-EPON ONUs), the PMA transmit clock is derived from the PMA receive clock by dividing the latter by 2.5. In the ONUs supporting multiple receive channels, the PMA transmit clock tracks the received clock of the active (enabled) receive channel with the lowest index.

142.4.5 T_{CDR} measurement

142.4.5.1 Definitions

Clock and data recovery (CDR) lock time (denoted T_{CDR}) is defined as a time interval required by the receiver to acquire phase lock on the incoming data stream. T_{CDR} is measured as the time elapsed from the moment when the electrical signal after the PMD at TP8, as illustrated in Figure 141–3, reaches the conditions specified in 141.7.14 for receiver settling time to the moment when the signal phase is recovered and jitter is maintained for an input signal with BER of no worse than 10^{-2}.

A PMA instantiated in an OLT shall become synchronized at the bit level within 400 ns (T_{CDR}) after the appearance of a valid synchronization pattern (as defined in 142.1.3) at TP8.

142.4.5.2 Test specification

The test of the OLT PMA receiver T_{CDR} time assumes that there is an optical PMD transmitter at the ONU with a well-known T_{on} time as defined in 141.7.13, and an optical PMD receiver at the OLT with a

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well-known $T_{rx\_settling}$ time as defined in 141.7.14. After the T_{on} + $T_{rx\_settling}$ time, the parameters at TP8 reach within 15 % of their steady-state values.

Set up the test ONU/OLT test system for 10^{-2} BER. Assuming a 3-zone SP1, SP2, and SP3 upstream ONU burst structure as shown in Figure 142–3, program the ONU SP1 TX pattern length so that the SP1 pattern ends at the precise end of the well-known OLT receiver settling time (within one 257-bit block of SP1, or ~10 ns granularity). Starting with the SP2 pattern of zero length (zero 257-bit blocks), test for SP3 detection. If the detection fails, increase the SP2 length by one and repeat the test until SP3 pattern is detected reliably. The number of 257-bit SP2 blocks times the length of each block is the T_{CDR} time, with a margin of error of one 257-bit block time. To reduce hysteresis, increase the number of 257-bit SP2 blocks several hundred nanoseconds beyond this point (20 to 30 additional 257-bit SP2 blocks), and then start decrementing the number of 257-bit SP2 blocks, testing for the SP3 detection at each decrement, until the SP3 SBD is not detected at the OLT. If the SP2 block time counting both forward and backward is less than the specified T_{CDR} maximum time of 400 ns, then the CDR performance meets the requirement.

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142.5 Protocol implementation conformance statement (PICS) proforma for Clause 142, Physical Coding Sublayer and Physical Media Attachment for Nx25G-EPON[236]

142.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 142, Physical Coding Sublayer and Physical Media Attachment for Nx25G-EPON, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

142.5.2 Identification

142.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

142.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 142, Physical Coding Sublayer and Physical Media Attachment for Nx25G-EPON
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[236]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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142.5.3 PCS capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
PCS1	Transmission bit order	142.2	Per Figure 142–4	M	Yes [ ]
PCS2	Control code values treated as errors	142.2.1	All control code values that do not appear in Table 142–2 are not to be transmitted and are treated as an error if received	M	Yes [ ]
*OLT	OLT functionality		Device supports functionality required for OLT	O/1	Yes [ ] No [ ]
*ONU	ONU functionality		Device supports functionality required for ONU	O/1	Yes [ ] No [ ]

142.5.4 PCS processes

Item	Feature	Subclause	Value/Comment	Status	Support
PSD1	FEC encoder	142.2.4	Encodes the transmitted data stream using a quasi-cyclic QC-LDPC FEC, defined in 142.2.4.1	M	Yes [ ]
PSD1a	FEC codeword shortening	142.2.4.2	Supports FEC shortening	M	Yes [ ]
PSD1b	FEC encoding process	142.2.4.2	Per 142.2.4.2	M	Yes [ ]
PSD2	Input process	142.2.5.4.1	As depicted in Figure 142–9	M	Yes [ ]
PSD3	Framer process	142.2.5.4.2	As depicted in Figure 142–10	M	Yes [ ]
PSD4	Transmit process	142.2.5.4.3	As depicted in Figure 142–11	M	Yes [ ]
PSD5	64B/66B decoder	142.3.4	As depicted in Figure 49–17	M	Yes [ ]
PSD6a	Synchronizer process in OLT	142.3.5.4	As depicted in Figure 142–14, for every enabled receive channel	OLT:M	Yes [ ] N/A [ ]
PSD6b	Synchronizer process in ONU	142.3.5.5	As depicted in Figure 142–15, for every enabled receive channel	ONU:M	Yes [ ] N/A [ ]
PSD7	Output process	142.3.5.7	As depicted in Figure 142–17, for every enabled receive channel	M	Yes [ ]
PSD8	PCS ONU BER Monitor process	142.3.5.6	As depicted in Figure 142–16 for every enabled receive channel	ONU:M	Yes [ ] N/A [ ]

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142.5.5 PMA processes

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	Differential encoder in OLT	142.4.2	As depicted in Figure 142–18	OLT:M	Yes [ ] N/A [ ]
PMA2a	Differential decoder in ONU	142.4.3	As depicted in Figure 142–19	ONU:M	Yes [ ] N/A [ ]
PMA2b	Automatic detection of differential encoding	142.4.3	ONU implements automatic detection of Rx path differential encoding and enables decoder as appropriate	ONU:M	Yes [ ] N/A [ ]
PMA3	ONU loop-timing	142.5	ONU PMA transmit clock tracks the ONU PMA receive clock	ONU:M	Yes [ ] N/A [ ]
PMA4	OLT PMA CDR synchronization time	142.4.5.1	OLT PMA becomes synchronized at the bit level within 400 ns (T_{CDR}) after the appearance of a valid synchronization pattern (as defined in 142.1.3) at TP8	OLT:M	Yes [ ] N/A [ ]
PMA5	PMA_SIGNAL[*i*].request, value in OLT	142.4.1.3	In OLT, this primitive always takes on the value of ON	OLT:M	Yes [ ] N/A [ ]

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143. Multi-Channel Reconciliation Sublayer

143.1 Overview

This clause describes the Multi-Channel Reconciliation Sublayer (MCRS) which enables multiple MACs to interface with multiple xMIIs. Figure 143–1 shows the relationship between this MCRS and the ISO/IEC OSI reference model. Generally, single-channel RS specifications enabled a single MAC to interface to a single PHY in point-to-point (P2P) links, or multiple MACs to interface to a single PHY in P2MP links (e.g., EPON architectures). This concept is expanded in this clause to allow single or multiple MACs to interface with multiple PHYs in either P2P or P2MP applications.

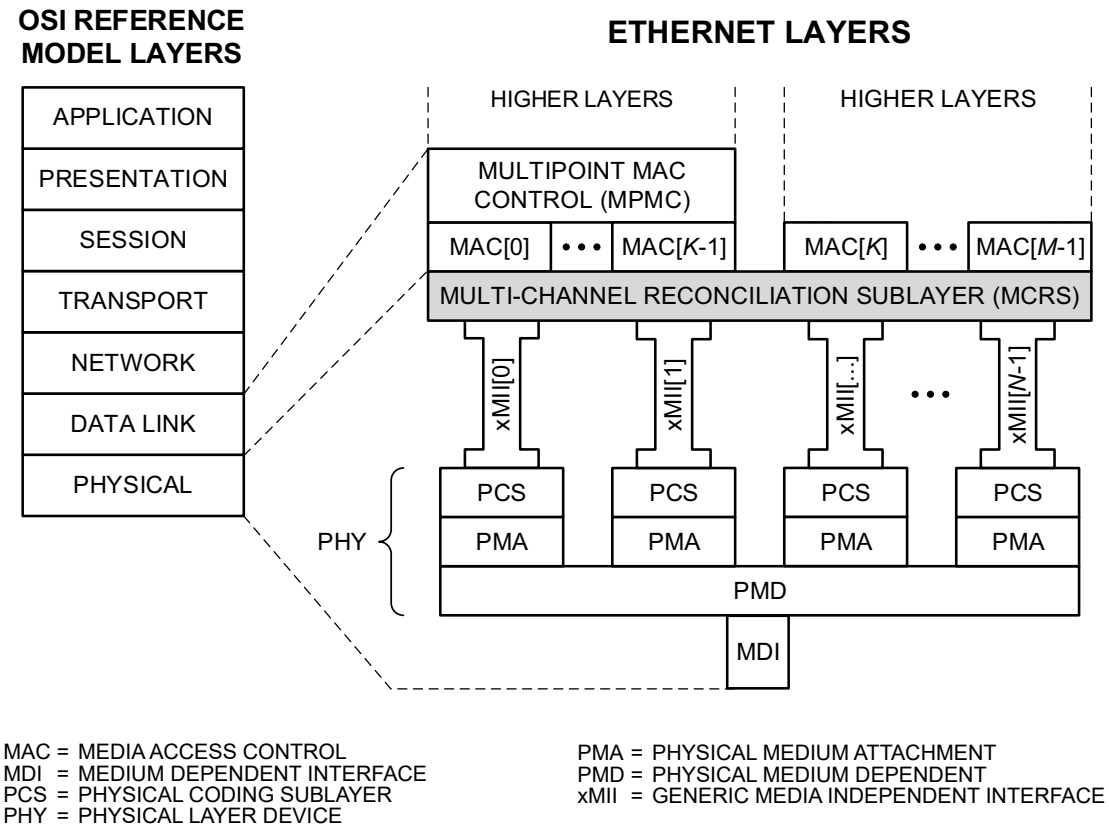

Figure 143–1—Relationship of MCRS to the OSI reference model

The MCRS adapts the bit-serial protocols of the MAC to the parallel format of the Physical Coding Sublayer (PCS) service interface. This clause defines an MCRS as an interface between the MAC sublayer and one or more xMIIs. In this clause, xMII is used as a generic term for the Media Independent Interfaces for implementations of 10 Gb/s and above. For example: for 10 Gb/s implementations, it is called XGMII; for 25 Gb/s implementations, it is called 25GMII. Though the xMII is an optional logical interface between the MAC sublayers and the Physical Layer devices, it is used extensively in this clause as a basis for specification.

143.2 Summary of major concepts

The following are the major concepts of the MCRS:

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a) The MCRS transmission is controlled by a higher layer (e.g., Multipoint MAC Control sublayer defined in Clause 144) via the use of MCRS_CTRL primitives, which indicate envelope start time, durations, and transmission channels.
b) The MCRS establishes a temporary binding of a single MAC instance to one or more xMII instances with all xMIIs operating at the same rate.
c) In the transmit direction, the MCRS converts the MAC serial data stream into the parallel data paths of multiple xMIIs servicing separate PHYs.
d) In the receive direction, the MCRS maps the signal sets provided by the xMIIs to the PLS service primitives of individual MACs.
e) Each direction of data transfer is independent and serviced by data, control, and clock signals.
f) The MCRS generates continuous data or control characters in the transmit path and expects continuous data or control characters in the receive path.

143.2.1 Concept of a logical link and LLID

In point-to-multipoint architectures, such as EPON, the transmitting and receiving stations may include multiple MAC instances. Such architectures are best viewed as a collection of logical point-to-point and/or point-to-multipoint links. A point-to-point logical link connects a single MAC instance at the transmitting station to a single MAC instance at the receiving station. A point-to-multipoint logical link takes advantage of the P2MP topology and connects a single MAC instance at the transmitting station to multiple MAC instances at multiple receiving stations. The transmitting and receiving stations may be logically connected with each other via multiple logical links.

A logical link is created in the MCRS (below the MAC) by tagging each frame (or frame fragment) with a logical link identifier (LLID) value. The MCRS transmit function inserts a specific LLID value depending on which instance of MAC has sourced the frame. The MCRS receive function directs the received frame (or frame fragment) to the specific MAC instance mapped to this LLID value, or to multiple MAC instances, in case of a point-to-multipoint logical link. The concept of a logical link is further defined in 144.1.1.2.

143.2.2 Concept of an MCRS channel

An MCRS channel is a single unidirectional transmission path through the MCRS. The number of channels contained within an MCRS generally corresponds to the number of xMII instances connected to the MCRS. Thus, an MCRS implementation that connects to *N* xMII instances contains *N* transmit MCRS channels and *N* receive MCRS channels. Some architectures (e.g., EPON) allow an xMII interface to only implement either receive or a transmit data path. In such architectures, the number of receive and transmit MCRS channels may be different. For example, in a 50/10G-EPON OLT, there are two transmit MCRS channels attached to two 25GMIIs and one receive MCRS channel attached to one XGMII.

143.2.3 Binding of multiple MACs to multiple xMII instances

The key function of the MCRS is the dynamic binding of a PLS_DATA[*m*] interface to one or more MCRS channels (*m* represents the index of the MAC instance). The dynamic nature of the binding means that such a binding exists only for a predetermined interval of time during which a given MAC instance is expected to transmit or receive data. After that time, the binding no longer exists, and a different MAC instance may bind to the same MCRS channels.

The dynamic binding of MAC instances to MCRS transmit channels is controlled by the MCRS_CTRL.request() primitive described in 143.3.1.2.1. The dynamic binding of MAC instances to receive MCRS channels is determined by the LLID value of the incoming data.

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143.2.4 Transmission and reception over multiple MCRS channels

143.2.4.1 Transmission unit

Within the MCRS, the basic unit of transmission is the envelope quantum (EQ). One EQ is represented by a 72-bit block consisting of 64 data bits and eight control bits. For 36-bit wide xMIIs, such as 25GMII, an EQ is mapped to two successive xMII transfers as shown in Figure 143–2.

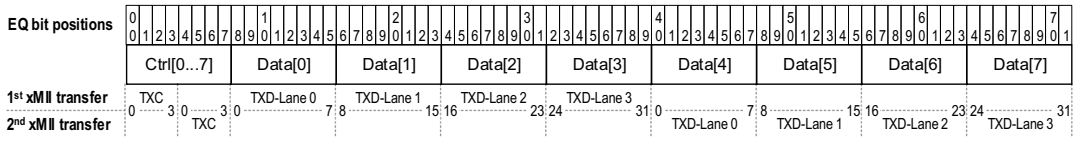

Figure 143–2—Envelope quantum (EQ) format

143.2.4.2 Transmission envelopes

The MCRS encapsulates data transmitted by a MAC instance in transmission envelopes. A transmission envelope represents a continuous transmission by a specific MAC instance (LLID) on a specific MCRS channel. A transmission envelope is transmitted on a single MCRS channel. In a system with a single channel an envelope includes one or more data frames and may contain at most two partial frames (one at the beginning and one at the end of the envelope) and any number of non-fragmented frames. In systems with multiple channels, envelopes may overlap (see 143.2.5) and a frame may be striped over multiple channels with each channel transporting parts of this frame. However, at the conclusion of the overlapped transmission, only a single frame may remain fragmented.

143.2.4.3 Envelope headers

Each transmission envelope begins with an envelope header (see Figure 143–3). The envelope header consists of multiple fields, such as LLID, Envelope Length, EnvType flag, and other fields defined in 143.3.2.

The LLID field identifies a specific logical link.

The size of the envelope header is exactly one EQ. The envelope header includes the Envelope Length field that shows the length of the entire envelope in units of EQ. The envelope header itself is counted as part of the envelope, therefore the minimum value of the Envelope Length field is one.

There are two distinct types of envelope headers; an envelope start header (ESH) and an envelope continuation header (ECH).

The ESH is inserted into the transmission stream at the beginning of every envelope, while no data is being taken from the corresponding MAC instance. At the receiving end, the ESH is processed by the MCRS and then discarded and no bits are passed to the corresponding MAC instance.

The ECH is inserted into the transmission stream in place of a data frame preamble. The length field of the ECH shows the residual length of the envelope. At the receiving end, the ECH is replaced with a normal frame preamble, which is passed to the corresponding MAC instance.

To distinguish the ESH and ECH, the envelope header includes a field called the EnvType flag. In ESH, the EnvType flag carries the value of 1 and in ECH, the flag carries the value of 0. Figure 143–3 illustrates a

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transmission sequence for a single LLID *L* transmitting three frames (the first and the last frames are fragments). The format of the envelope header and field definitions are specified in 143.3.2.

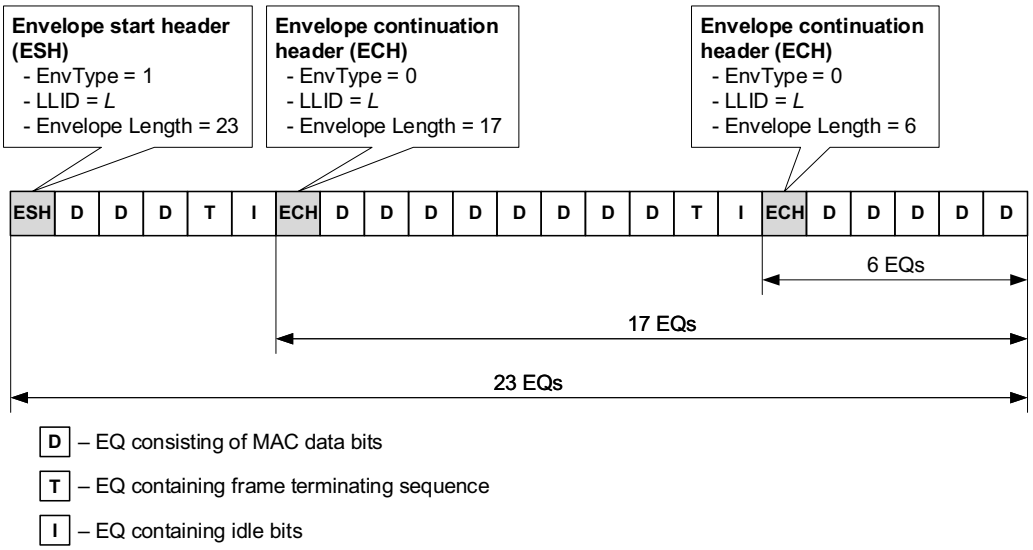

Figure 143–3—An illustration of transmission sequence consisting of three frames

143.2.4.4 Interpacket gap adjustment

Multi-lane xMIIs, such as 25GMII, require the alignment of the Start control character (first octet of preamble) to lane 0. Generally, a technique called Deficit Idle Count is used to accomplish this task (see 46.3.1.4).

However, because the MCRS replaces the frame preamble with an ECH, there is an additional requirement for the Start control character to be aligned to octet 0 of an EQ, such that the entire preamble occupies exactly one EQ and is not split across two consecutive EQs. To achieve such alignment, rather than maintaining a deficit idle count, the interpacket gap (IPG) is either unchanged or reduced, but is not expanded. The IPG may be reduced by up to seven octets from its default size of 96 bits. For back-to-back data frames, the minimum guaranteed IPG is five octets.

The exact size of the IPG depends on the length of the previous data frame (for the case of back-to-back frames). Figure 143–4 illustrates the IPG reduction for all possible positions of the end of frame character. The default IPG generated by the MAC and the reduced IPG are highlighted.

The minimum IPG of five octets is consistent with the requirements of 46.2.1 for XGMII (and hence applicable to 25GMII). Since the IPG either remains unchanged or is reduced, in order to prevent the MAC data rate from exceeding the specified maximum limit, the MCRS provides a rate adjustment mechanism, whereby a MAC is paused for a predefined duration of time at a predefined repeating interval.

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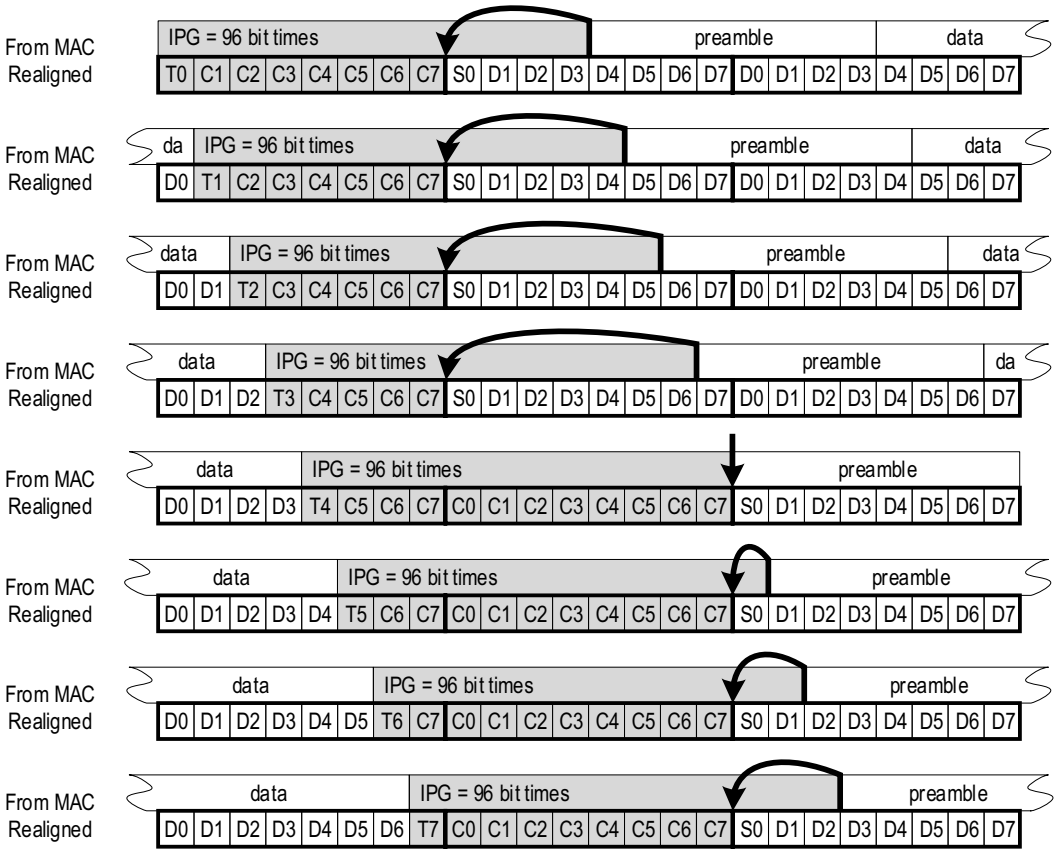

Figure 143–4—An illustration of Start control character alignment to octet 0

143.2.5 Dynamic channel bonding

If the PLS_DATA[*m*] interface is bound to a single MCRS channel that is connected to an xMII instance, the corresponding MAC instance is able to transmit and receive at a data rate corresponding to that xMII data rate. For example, if the MCRS sublayer is connected to a 25GMII, that MAC instance is able to transmit and receive at 25 Gb/s.

However, in a system that supports multiple MCRS channels (i.e., MCRS is connected to multiple xMII instances), a single PLS_DATA[*m*] interface may be simultaneously bound to N_{TX} MCRS transmit channels and N_{RX} MCRS receive channels, where N_{TX} may not equal N_{RX}. In this case, again assuming the 25GMII, the corresponding MAC instance supports the transmit data rate of $N_{TX} \times 25$ Gb/s and the receive data rate of $N_{RX} \times 25$ Gb/s.

The channel bonding takes place when an LLID is assigned transmission envelopes on more than one channel. Such envelopes may happen to activate at the same time and to have the same duration, as illustrated in Figure 143–5 for LLID A. But most often the envelopes are not mutually aligned and just partially overlap as shown for LLID B.

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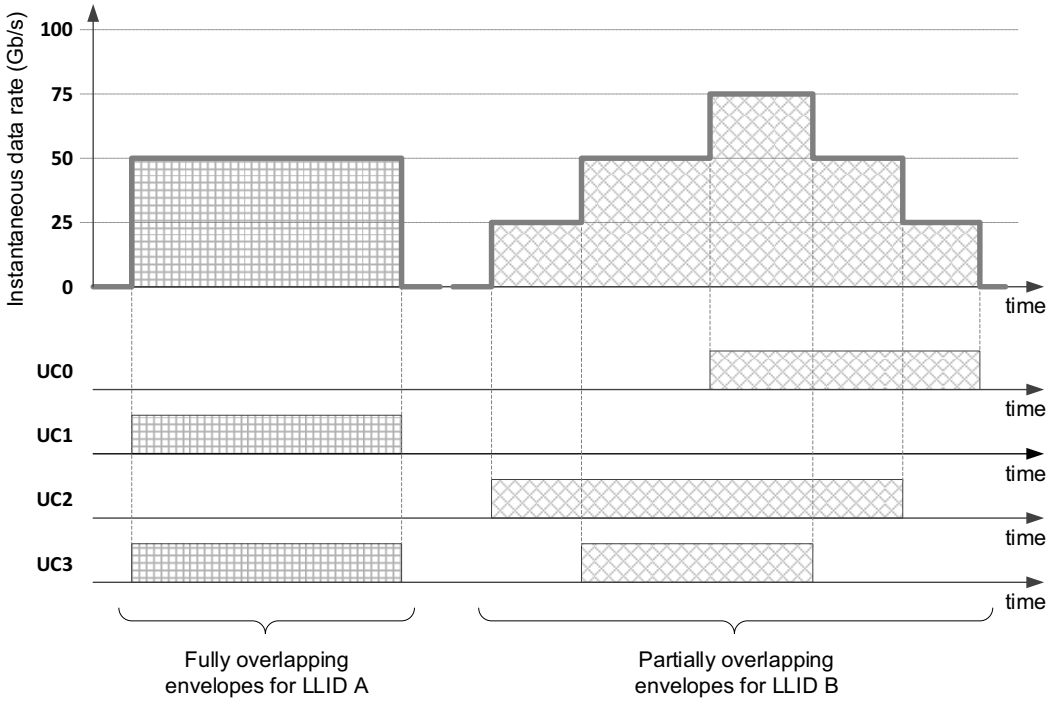

Figure 143–5—Full or partial envelope overlap and the resulting instantaneous data rate

An LLID (i.e., a MAC instance) that is given two or more overlapping envelopes on several MCRS channels is able to seamlessly increase its transmission data rate to the aggregated data rate of all the MCRS channels with the overlapping envelopes. This is referred to as dynamic channel bonding and it gives the system an ability to achieve a higher instantaneous transmission or reception rate than is available for any single MCRS channel. For example, a MAC instance connected to an MCRS with four channels of 25 Gb/s each can achieve an instantaneous transmission rate of 25 Gb/s, 50 Gb/s, 75 Gb/s, or 100 Gb/s by varying, in real time, the number of channels that are bonded to send data from a single LLID.

143.2.5.1 LLID transmission over multiple MCRS channels

The dynamic channel bonding is achieved by interleaving data belonging to a single LLID (i.e., data from a single MAC instance) over multiple envelopes on multiple MCRS channels. Figure 143–6 illustrates a dynamic channel bonding example based on the partially overlapping envelopes scenario in Figure 143–5. Each EQ is transmitted on the channel that has the earliest transmission availability. If there are multiple such channels, the one with the lowest channel index is selected. In other words, the overlapping envelopes are filled with EQs in the increasing order of MCRS channel index.

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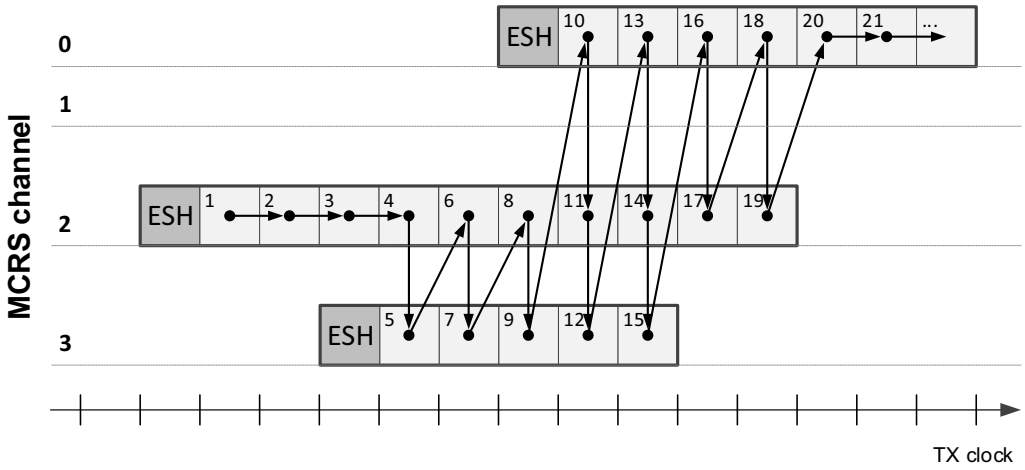

Figure 143–6—Fill order of overlapping envelopes

143.2.5.2 MCRS channel skew remediation mechanism

In a multi-channel system that uses multiple wavelengths to carry different MCRS channels, the channels have unequal propagation delays. This variable propagation delay results in a timing skew between signals received on separate MCRS channels. Other timing variability may accumulate in the sublayers below the MCRS, exacerbating this timing skew.

To properly restore the order of data transmitted over multiple bonded MCRS channels, the skew between the channels has to be eliminated at the receiver. The skew remediation mechanism is based on two buffers: an envelope transmission buffer (EnvTx) in the transmitting MCRS and an envelope reception buffer (EnvRx) in the receiving MCRS. As envelopes traverse the EnvTx buffer (before the skew has impacted any of the MCRS channels), their relative position in the EnvTx buffer is recorded and transmitted to the EnvRx buffer. At the receiving station, the envelopes received on multiple channels are aligned in the EnvRx buffer using the position information received from the transmitting device. The relative alignment of envelopes in EnvRx becomes identical to their relative alignment that existed in EnvTx. This envelope alignment method results in the complete elimination of any skew between the channels, as well as any timing variability that may accumulate in the sublayers below MCRS.

143.2.5.3 EnvTx and EnvRx buffers

The EnvTx and EnvRx buffers are two-dimensional buffers organized into rows and columns. The number of columns is equal to the number of channels supported by the device. If the number of rows is set to 32, this provides sufficient buffering to mitigate approximately 80 ns of skew between any two channels (assuming a 25GMII). If an application requires additional skew mitigation, up to ±81.92 ns of skew may be accommodated by increasing the number of buffer rows.

The EQs are written into the EnvTx and read from EnvRx buffers first by row, then by column, as shown in Figure 143–7.

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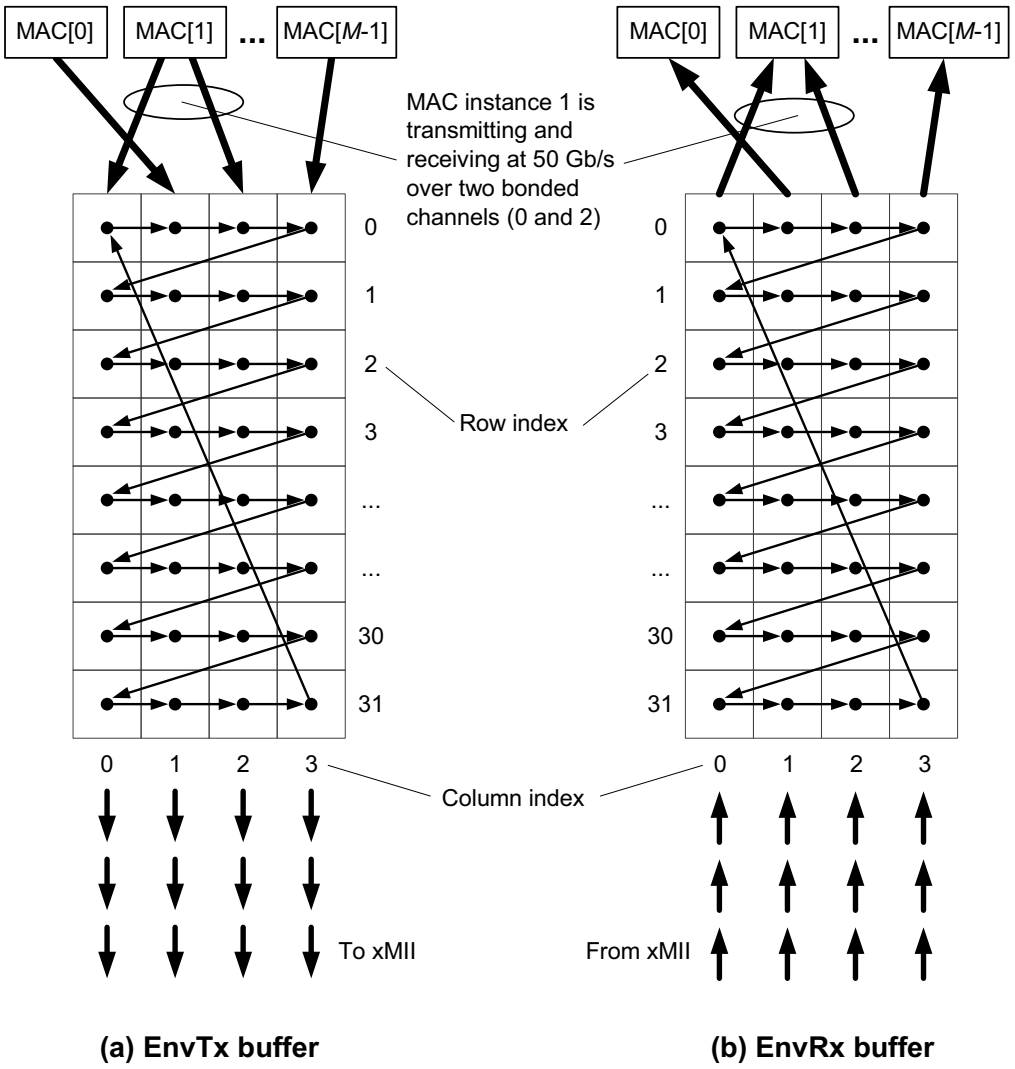

Figure 143–7—Internal structure of EnvTx and EnvRx buffers

In the EnvTx buffer all columns of a row are written before the write pointer shifts to the next row. The EQs written into each column may be sourced by different MAC instances, if the envelopes on different channels belonged to different LLIDs, or from the same MAC instance, in case of multiple channels bonded to serve the same LLID (see Figure 143–7).

Similarly, in the receiving device, the EQs read from different columns may be passed to different MAC instances, if the envelope headers on different channels carried different LLID values, or the EQs may be passed to the same MAC instance, if the envelope headers carried the same LLID value. In case of EQs from different columns being passed to the same MAC instance, the EQ from a column with the lower index is passed before an EQ from a column with the higher index.

EnvTx and EnvRx are circular buffers – after reading the last row, the read pointer shifts back to row 0. In EnvTx, the read and write pointers advance synchronously with the xMII transmit clock (TX_CLK). In

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EnvRx, the read and write pointers advance synchronously with the xMII receive clock (RX_CLK). However, the value of the receive channel write pointer is updated whenever an envelope header is received.

143.2.5.4 Envelope position alignment marker

The relative envelope position recorded in an envelope header by the MCRS transmit function is simply the logical equivalent of the EnvTx buffer row index into which the given envelope header was written. This information is placed in an envelope header field called the envelope position alignment marker (EPAM). When an envelope header is received by the MCRS receive function, the EPAM field is extracted and its value is used to update the write pointer (row index) into which this envelope header is to be written. The remainder of the envelope is then written sequentially into the same column following the envelope header.

Figure 143–8 illustrates (a) the initial envelope positions in the EnvTx buffer, (b) the accumulated channel-dependent skew of the received channels at the EnvRx buffer, and (c) the restored alignment based on EPAM value carried in each envelope header. As the true relative positions of the envelopes are restored, reading the data in the same order as shown in Figure 143–8 properly serializes the data received over the multiple bonded channels.

At the receiving station, regardless of the amount of accumulated skew, EQs transmitted at the same time from the same MCRS are placed in the same row of the EnvRx. As the EnvRx is read out in a row-by-row order over all channels the receiver effectively realigns the EQs to the same order they were transmitted in.

143.2.6 MDIO addressing model for multi-channel architecture

The MDIO addressing model for multi-channel architecture is defined as follows:

— Separate physical ports on the OLT are managed by separate Station Management entities (STAs, see 45.1.2).
— Within each physical port, separate channels are addressed via port address (PRTAD, see 45.3.5).
— Within each channel, separate layers (PMA, PCS, etc.) are addressed via device address (DEVAD, see 45.3.6) as shown in Table 45–1.
— A common PMD that spans multiple channels is addressed via the numerically-lowest PRTAD associated with that PMD.

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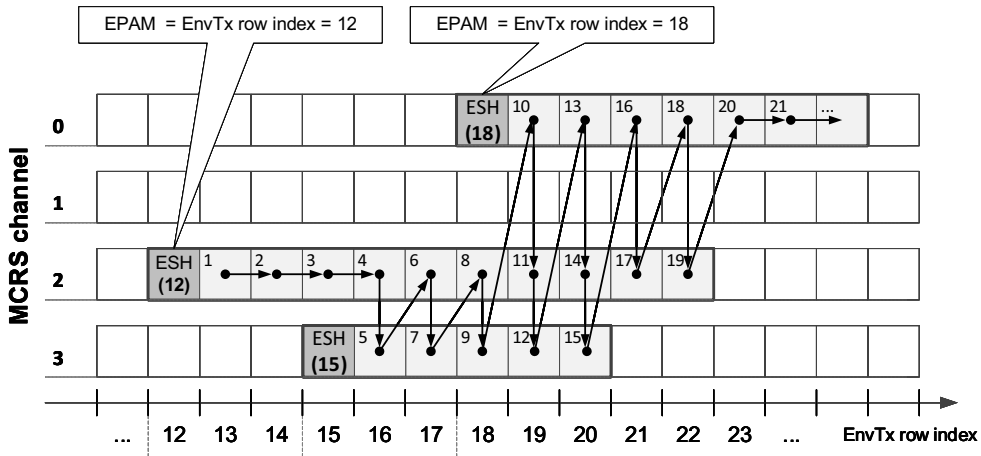
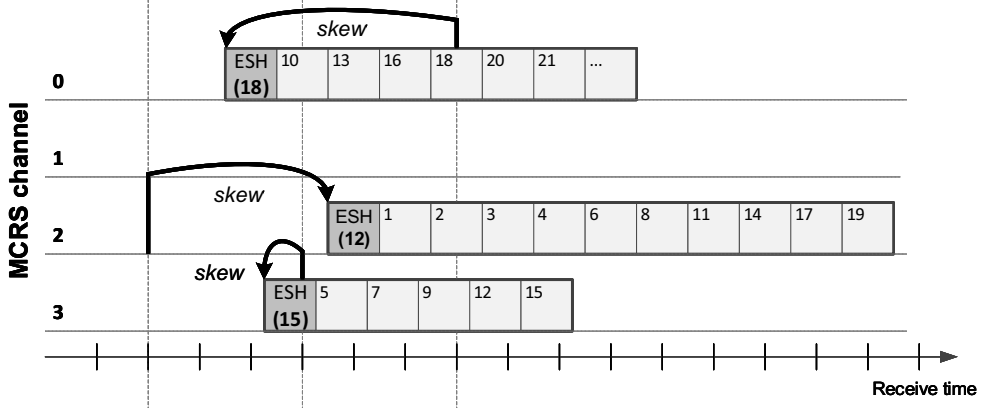
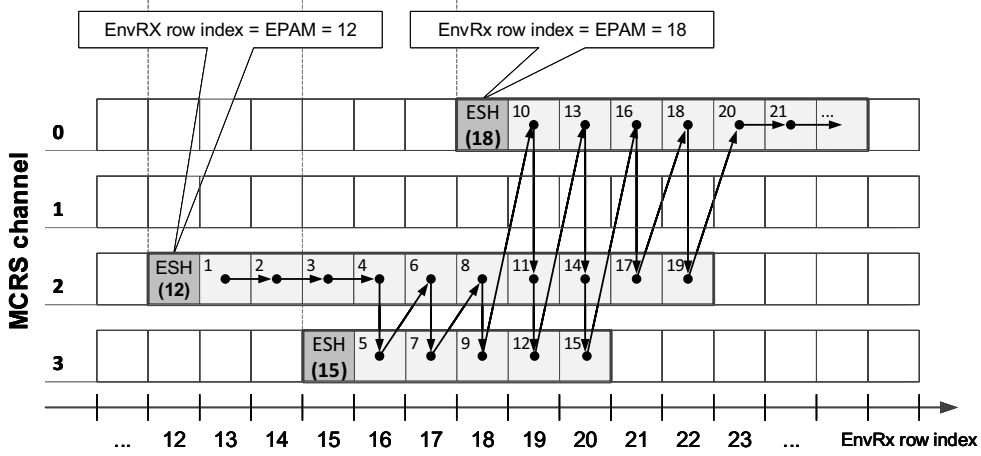


(a) Envelope header records the row index of this header in the EnvTx buffer



(b) Data is received on multiple channels with different propagation delays (skew)



(c) Envelopes are positioned in the EnvRx buffer in a row index as recorded in the ESH

Figure 143–8—Illustration of skew elimination by envelope position alignment in the EnvRx buffer

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143.3 MCRS functional specifications

143.3.1 MCRS interfaces

Interfaces to the MCRS are illustrated in Figure 143–9. In addition to the *M* instances of the PLS service interface (one per MAC) and *N* xMII instances, there is an MCRS_CTRL interface that connects to the higher layers (see Figure 143–1).

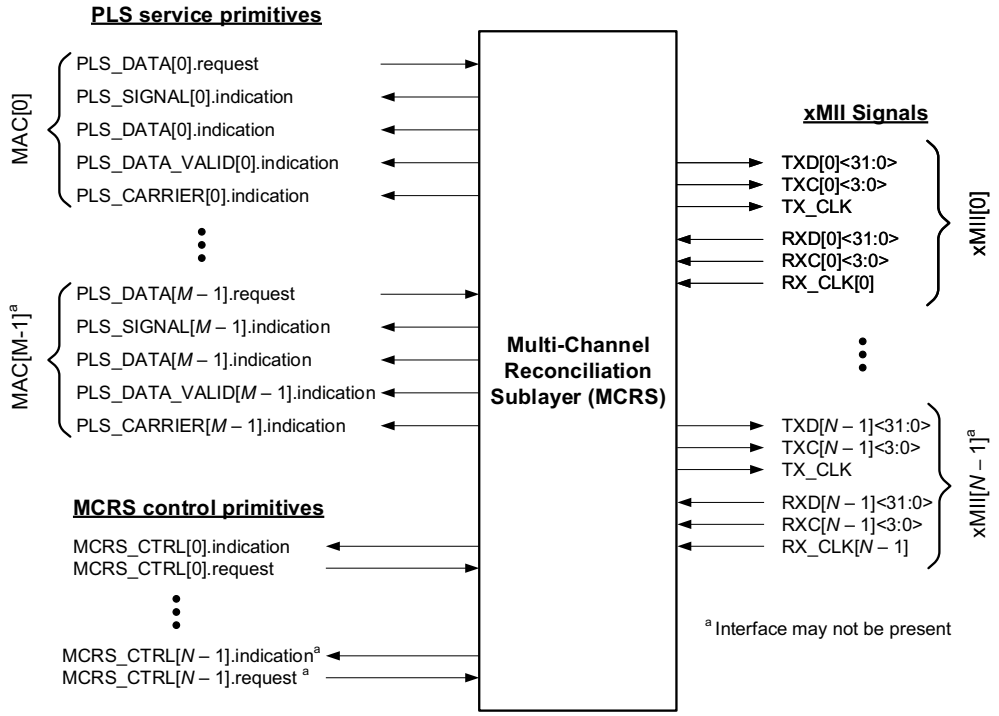

Figure 143–9—Multi-Channel Reconciliation Sublayer (MCRS) inputs and outputs

143.3.1.1 PLS service primitives

In all single-channel RS definitions, only one PLS service interface is active at any given moment; this is still true for systems with only one active MCRS channel. However, for systems with more than one MCRS channel there may be multiple PLS service interfaces active at any given time.

The mapping of the PLS service primitives to xMII signals are shown in 143.3.1.1.1 for PLS_DATA[].request primitives and in 143.3.1.1.3 for PLS_DATA[].indication primitives. These are similar to the mappings described in 46.1.7. However, in systems with multiple MCRS channels there are multiple xMIIs and therefore an index is added to the xMII signals to indicate which of the xMIIs to use.

Depending on the MAC operating speed, the PLS_DATA.request primitive maps to one or multiple xMII transmit interfaces (see Table 143–1).

Depending on the MAC operating speed, the PLS_DATA.indication primitive maps to one or multiple xMII receive interfaces (see Table 143–2).

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Table 143–1—Mapping of PLS_DATA.request primitives

MAC operating speed	MCRS channels	Transmit interface	Signals
10 Gb/s	1	XGMII[0]	TXD[0]<31:0>, TXC[0]<3:0> and TX_CLK
25 Gb/s	1	25GMII[0]	TXD[0]<31:0>, TXC[0]<3:0> and TX_CLK
50 Gb/s	2	25GMII[0] 25GMII[1]	TXD[0]<31:0>, TXC[0]<3:0> and TX_CLK[a] TXD[1]<31:0>, TXC[1]<3:0>
N × 25 Gb/s	*N*	25GMII[0] 25GMII[1] 25GMII[2] … 25GMII[*N* – 1]	TXD[0]<31:0>, TXC[0]<3:0> and TX_CLK[a] TXD[1]<31:0>, TXC[1]<3:0> TXD[2]<31:0>, TXC[2]<3:0> … TXD[*N* – 1]<31:0>, TXC[*N* – 1]<3:0>

[a] All transmit 25GMII interfaces share a common clock.

Table 143–2—Mapping of PLS_DATA.indication primitives

MAC operating speed	MCRS channels	Receive interface	Signals
10 Gb/s	1	XGMII[0]	RXD[0]<31:0>, RXC[0]<3:0> and RX_CLK[0]
25 Gb/s	1	25GMII[0]	RXD[0]<31:0>, RXC[0]<3:0> and RX_CLK[0]
50 Gb/s	2	25GMII[0] 25GMII[1]	RXD[0]<31:0>, RXC[0]<3:0> and RX_CLK[0] RXD[1]<31:0>, RXC[1]<3:0> and RX_CLK[1]
N × 25 Gb/s	*N*	25GMII[0] 25GMII[1] 25GMII[2] … 25GMII[*N* – 1]	RXD[0]<31:0>, RXC[0]<3:0> and RX_CLK[0] RXD[1]<31:0>, RXC[1]<3:0> and RX_CLK[1] RXD[2]<31:0>, RXC[2]<3:0> and RX_CLK[2] … RXD[*N* – 1]<31:0>, RXC[*N* – 1]<3:0> and RX_CLK[*N* – 1]

143.3.1.1.1 Mapping of PLS_DATA[*ch*].request primitive

The MCRS maps the primitive PLS_DATA.request to the xMII signals TXD[*ch*]<31:0>, TXC[*ch*]<3:0>, and TX_CLK in the same way as for the XGMII as specified in 46.1.7.1.

143.3.1.1.2 Mapping of PLS_SIGNAL[*ch*].indication primitive

The MCRS support full duplex operation only and does not generate the PLS_SIGNAL.indication primitive.

143.3.1.1.3 Mapping of PLS_DATA[*ch*].indication primitive

The MCRS maps the primitive PLS_DATA.indication to the xMII signals RXD[*ch*]<31:0>, RXC[*ch*]<3:0> and RX_CLK[*ch*] in the same way as for the XGMII as specified in 46.1.7.2.

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143.3.1.1.4 Mapping of PLS_DATA_VALID[*ch*].indication primitive

The MCRS maps the primitive PLS_DATA_VALID.indication to the xMII signals RXC[*ch*]<3:0> and RXD[*ch*]<31:0> in the same way as for the XGMII as specified in 46.1.7.5.

143.3.1.1.5 Mapping of PLS_CARRIER[*ch*].indication primitive

The MCRS supports full duplex operation only and does not generate the PLS_CARRIER.indication primitive.

143.3.1.2 MCRS control primitives

The MCRS inputs the MCRS_CTRL[*ch*].request primitives from the Multipoint Control Protocol (MPCP) and outputs to the MPCP the MCRS_CTRL[*ch*].indication primitives.

143.3.1.2.1 MCRS_CTRL[*ch*].request(link_id, epam, env_length) primitive

The MPCP requests the MCRS to transmit the next envelope using the MCRS_CTRL[*ch*].request(link_id, epam, env_length) primitive. This opens an envelope on channel *ch* for the LLID specified by link_id with a length (in EQs) of env_length. If all channels are idle, the EnvPam variable (see 143.3.3.4) is set to the value of epam (see EnvStartHeader() function definition in 143.3.3.5).

143.3.1.2.2 MCRS_CTRL[*ch*].indication() primitive

The Input process (see Figure 143–12) requests the next envelope from the MPCP after the completion of the previous envelope using the MCRS_CTRL[*ch*].indication() primitive. This primitive indicates to the MPCP that the MCRS is available for the next envelope in a given channel. In the absence of an active envelope, the MCRS_CTRL[*ch*].indication() primitive is generated continuously on every InClk transition (see 143.3.3.4). The MPCP may decide whether to issue a new envelope immediately adjacent to the previous envelope for envelopes that are expected to be packed in the same transmission burst. If the MPCP has determined that a transmission opportunity has ended, it signals that condition by issuing an envelope with link_id set to ESC_LLID (see Table 144–1).

143.3.1.2.3 MCRS_ECH[*ch*].indication(Llid) primitive

The Output process (see Figure 143–16) generates the MCRS_ECH[*ch*].indication(Llid) primitive every time an ESH EQ is read from the EnvRx buffer. This primitive causes the MPMC Control Parser process (see 144.2.1) to generate a local timestamp (i.e., to latch the local MPCP time) representing the arrival time of the ESH EQ.

143.3.1.3 XGMII interfaces

The XGMII is specified to support 10 Gb/s operation. The structure of each of the XGMII interfaces in an MCRS system is as specified in 46.1.6.

For mapping between the XGMII signals and the PLS service interface, see 143.3.1.1.1 and 143.3.1.1.3.

For multi-channel MCRS systems the transmit XGMIIs are synchronous and only one TX_CLK is required.

143.3.1.4 25GMII interfaces

The 25GMII is specified to support 25 Gb/s operation. The structure of each of the 25GMII interfaces in an MCRS system is identical to the XGMII structure specified in 46.1.6. The 25GMII data stream has the same

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characteristics as the XGMII data stream described in 46.2 with the exception of the clock rate, which is 390.625 MHz for the 25GMII.

For mapping between the 25GMII signals and the PLS service interface, see 143.3.1.1.1 and 143.3.1.1.3.

For multi-channel MCRS systems the transmit 25GMIIs are synchronous and only one TX_CLK is required.

143.3.2 Envelope header format

Each envelope initiated by the MCRS begins with a 72-bit envelope header. The envelope header shall be as shown in Figure 143–10. The envelope header includes a Start control code, an EnvType flag bit, a 22-bit Envelope Length field, an envelope position alignment marker (EPAM) field, two bits (E and K) reserved for encryption purposes, an LLID field, and an 8-bit cyclic redundancy check (CRC8).

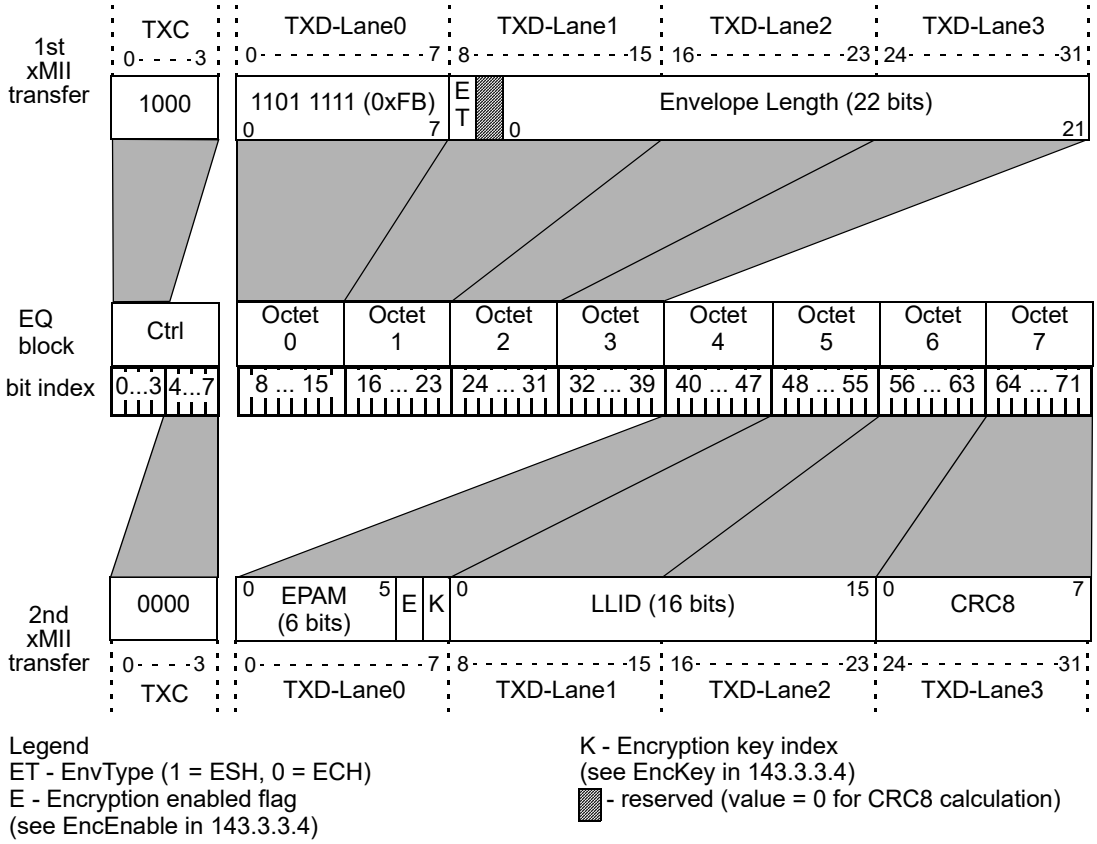

Figure 143–10—Mapping of envelope header fields into two xMII transfers

When the xMII is 36 bits wide, the transmission envelope header includes two successive transfers over the xMII, as illustrated in Figure 143–10. Each 36-bit transfer includes four control bits followed by 32 information bits. Octets within each envelope header field are transmitted from least significant to most significant. Bits within each octet are transmitted from LSB to MSB. An EQ contains eight octets of information so the length of the envelope header equals one EQ.

The envelope header is identified by a Start control code (Block type 0xFB, see Table 142–2).

The ESH has the EnvType flag set to one whereas the ECH has the EnvType flag set to zero. The ESH is used to indicate the beginning of a transmission from a specific LLID.

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Following the EnvType flag, there is one reserved bit (EQ<17>) and it is set to zero at the transmitter and its value is ignored at the receiver except for the purposes of calculating the CRC8.

The Envelope Length field represents the number of EQs in the envelope, including the envelope header itself (1 EQ).

The EPAM is used by the receiving MCRS to remove any timing skew that may have occurred during the transmission of the envelope from the source MCRS to the destination MCRS.

The LLID field is set to the value of the LLID (MAC instance) associated with the data in the envelope.

The CRC8 field is used for error detection within the header. CRC8 uses the same generating polynomial as described in 65.1.3.2.3. The CRC8 checksum is calculated over EQ bits 8 through 63. The envelope header bits are processed by the CRC8 calculating function in the same order they are transmitted, i.e., for each field the bits are processed starting with the LSB and ending with the MSB.

143.3.2.1 CRC8 calculation test sequences

The test sequences in Table 143–3, Table 143–4, and Table 143–5 show several example envelope header field values and the resulting CRC8 value computed by a compliant implementation.

Table 143–3—CRC8 computation example #1[a]

Envelope header fields	Start control code	EnvType	Reserved	Envelope Length	EPAM	E	K	LLID
Envelope header fields	0xFB	1	0	64	15	0	0	0xAB-CD
Envelope header with CRC8 (hex)	E5-AB-CD-0F-00-01-01-FB (transmitted LSB first)							
Envelope header with CRC8 (bin)	(last bit) | 1110-0101-1010-1011-1100-1101-0000-1111-0000-0000-0000-0001-0000-0001-1111-1011 | (first bit)							

[a]Gray highlight indicates location and calculated value of CRC8 field

Table 143–4—CRC8 computation example #2[a]

Envelope header fields	Start control code	EnvType	Reserved	Envelope Length	EPAM	E	K	LLID
Envelope header fields	0xFB	0	0	960	5	1	0	0x00-01
Envelope header with CRC8 (hex)	23-00-01-45-00-0F-00-FB (transmitted LSB first)							
Envelope header with CRC8 (bin)	(last bit) | 0010-0011-0000-0000-0000-0001-0100-0101-0000-0000-0000-1111-0000-0000-1111-1011 | (first bit)							

[a]Gray highlight indicates location and calculated value of CRC8 field

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Table 143–5—CRC8 computation example #3[a]

Envelope header fields	Start control code	EnvType	Reserved	Envelope Length	EPAM	E	K	LLID
Envelope header fields	0xFB	1	0	10 000	1	1	1	0x12-34
Envelope header with CRC8 (hex)	B6-12-34-C1-00-9C-41-FB (transmitted LSB first)							
Envelope header with CRC8 (bin)	(last bit) | 1011-0110-0001-0010-0011-0100-1100-0001-0000-0000-1001-1100-0100-0001-1111-1011 | (first bit)							

[a]Gray highlight indicates location and calculated value of CRC8 field

143.3.3 Transmit functional specifications

A functional block diagram of the MCRS transmit path is illustrated in Figure 143–11. The MCRS interfaces are described in 143.3.1. The MCRS transmit path is composed of two processes and one buffer.

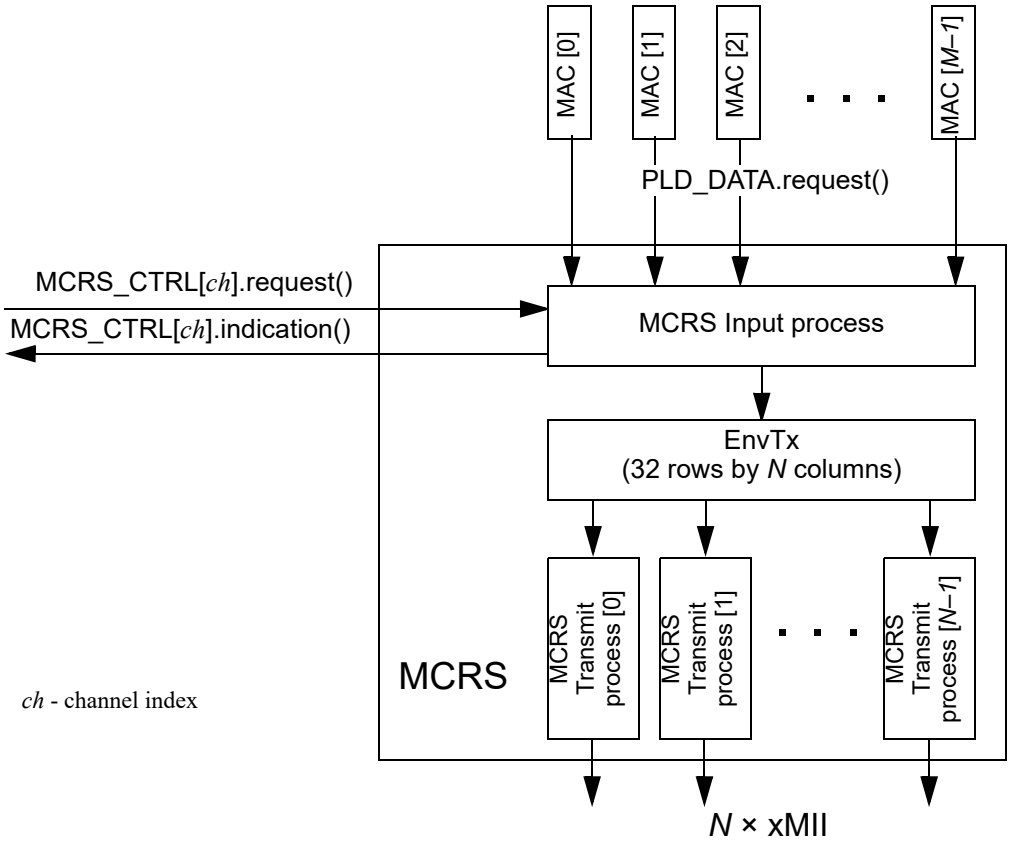

Figure 143–11—MCRS transmit functional block diagram

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The Input process, described in 143.3.3.6.1, accepts MAC data, formats it into EQs and stores these EQs in the EnvTx buffer. The Transmit process, described in 143.3.3.6.2, pulls EQs from the EnvTx buffer and feeds them to two successive transfers on the appropriate xMII.

143.3.3.1 Conventions

See 142.1.1.

143.3.3.2 Application-specific parameter definitions

Some constants and variables in this sub-clause have characteristics that are application-specific. For Nx25G-EPON specific parameter definitions refer to 143.4.1.3.

NOTE—References to future application-specific parameters are to be added only to this subclause.

143.3.3.3 Constants

ADJ_BLOCK_SIZE
: Type: integer
Description: The ADJ_BLOCK_SIZE constant represents the block size (in EQs) that is used to adjust the rate between the MAC and the PHY in the MCRS-based device.
Value: application-specific (see 143.3.3.2)

ESC_LLID
: See Table 144–1

IBI_EQ
: Type: 72-bit block
Description: The IBI_EQ constant indicates to the PCS that the burst is terminated.
Value: 0x0A-0A-0A-0A-0A-0A-0A-FF

IEI_EQ
: Type: 72-bit block
Description: The IEI_EQ represents an EQ value transmitted between envelopes.
Value: 0x08-08-08-08-08-08-08-FF

NUM_CH
: Type: unsigned integer
Description: The NUM_CH constant represents the number of channels supported by an MCRS-based device.
Value: application-specific (see 143.3.3.2)

PREAMBLE_EQ
: Type: 72-bit block
Description: The value of an EQ returned by the GetMacBlock() function that represents a preamble.
Value: 0x5D-55-55-55-55-55-55-FB-01

RATE_ADJ_EQ
: Type 72-bit block
Description: The value of an EQ that is used as a placeholder to allow for rate differences between the MAC and the PHY layers.
Value: 0x09-09-09-09-09-09-09-FF

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RATE_ADJ_SIZE

Type: integer

Description: The RATE_ADJ_SIZE constant represents the number of EQs within the ADJ_BLOCK_SIZE block during which the MAC transmission is deferred. The effective MAC rate (per channel) is equal to (nominal MAC rate) × (1 – RATE_ADJ_SIZE / ADJ_BLOCK_SIZE).

Value: application-specific (see 143.3.3.2)

143.3.3.4 Variables

ch

Type: integer

Description: The ch variable represents the index of a specific xMII channel bound to an instance of the MCRS Transmit or MCRS Receive process. The values of ch range from 0 to (NUM_CH – 1). Within each instance of the MCRS Transmit or MCRS Receive process, the value of ch remains constant.

BEGIN

See 142.2.5.2

BlkLeft[ch]

Type: integer

Description: The BlkLeft variable represents the number of EQs remaining in the envelope currently being processed by the MCRS.

EncEnable

Type: Boolean

Description: Encryption enabled flag, not for use by IEEE Std 802.3.

EncKey

Type: one-bit integer

Description: Encryption key index, not for use by IEEE Std 802.3.

EnvTx

Type: array of 72-bit blocks

Description: The EnvTx buffer is used to transfer information between the MCRS Input process and the MCRS Transmit process. In this buffer, each cell, represented by the variables EnvTx[ch][r], stores one EQ (a 72-bit block) of information. The number of columns in the EnvTx buffer is NUM_CH (see 143.3.3.3). The number of rows is 64, as determined by the size of the EPAM field in the envelope header (see 143.3.3.2). The buffer is filled sequentially by the MCRS Input process and is emptied in parallel by NUM_CH instances of the MCRS Transmit process. For additional details, refer to 143.2.5.3.

EnvLeft[ch]

Type: 23-bit signed integer

Description: The EnvLeft variable represents the length remaining in the current envelope for channel ch.

EnvPam

Type: 6-bit integer

Description: The EnvPam variable is used to remove delay variability (including skew) accumulated during transport between two or more channels from a single transmitter. EnvPam is also used as the row index for the EnvRx buffer into which the received data is to be written (see 143.3.4).

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InClk

Type: Boolean

Description: The InClk clear-on-read variable is set to true on each rising edge of the TX_CLK signal.

InEQ

Type: 72-bit binary array

Description: A temporary holding variable for one EQ used in the Input process.

LinkId[ch]

Type: 16-bit integer

Description: The LinkId[ch] variables represent the MAC (LLID) being transferred by the Input process or Output process for channel ch.

rCol

Type: integer

Description: The rCol variable represents the EnvTx buffer column currently being read by the MCRS Transmit process. Each column corresponds to a separate transmission channel, i.e., a separate xMII interface.

rRow

Type: 6-bit integer

Description: The rRow variable represents the row in the EnvTx buffer currently being read by the MCRS Transmit process. The value of this variable is synchronized to wRow and is equal to wRow – 1.

TxClk[ch]

Type: Boolean

Description: Description: The TxClk[ch] variable represents the MCRS transmit clock for channel ch. Each TxClk[ch] clear-on-read variable is set to true on each edge, rising and falling, of the TX_CLK signal (see Table 143–1).

TxActive[ch]

Type: Boolean

Description: When set to true, the TxActive[ch] variable indicates that channel ch is currently enabled for transmission. The channel transmits the envelopes or inter-envelope idle EQs (IEI_EQ values) in the absence of envelopes. When set to false, transmission on channel ch is prohibited and this channel generates only inter-burst idle EQs (IBI_EQ values) towards the xMII.

wCol

Type: integer

Description: The wCol variable represents the EnvTx buffer column currently being written by the MCRS Input process. Each column corresponds to a separate transmission channel, i.e., a separate xMII interface.

wRow

Type: 6-bit integer

Description: The variable wRow represents the EnvTx buffer row index currently being written by the MCRS Input process. The value of rRow is synchronized to this variable and is equal to wRow – 1.

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143.3.3.5 Functions

EnvContHeader(wCol)

The EnvContHeader() function returns a new envelope header with the EnvType flag equal to 0, indicating that it is a continuation of the current envelope.

```
EQ EnvContHeader(int col)
{
   EQ hdr;
   hdr<7:0> = 0x01;                 // Control bits
   hdr<15:8> = 0xFB;                // S character
   hdr<16> = 0;                     // EnvType identifies ECH
   hdr<17> = 0;                     // Reserved
   hdr<39:18> = EnvLeft[col];       // EnvLength
   hdr<45:40> = EnvPam;             // EPAM
   hdr<46> = EncEnable;             // Encryption enabled flag
   hdr<47> = EncKey;                // Encryption key index
   hdr<63:48> = LinkId[col];        // LLID
   hdr<71:64> = CRC8(hdr<63:8>);    // Calculate CRC8
   return hdr;
}
```

EnvStartHeader(wCol, epam)

The EnvStartHeader() function returns a new envelope header with the EnvType flag equal to 1, indicating that it is a start of a new envelope. If this envelope starts a new burst (i.e., all channels are idle) it updates EnvPam to the value of the epam variable provided in the MCRS_CTRL[].request primitive.

```
EQ EnvStartHeader(int col, int6 epam)
{
   EQ hdr;

   // Use provided 'epam' value if this envelope starts a new burst
   if(!TxActive[0] AND !TxActive[1] AND … AND !TxActive[NUM_CH-1])
      EnvPam = epam;

   hdr<7:0> = 0x01;                 // Control bits
   hdr<15:8> = 0xFB;                // S character
   hdr<16> = 1;                     // EnvType identifies ESH
   hdr<17> = 0;                     // Reserved
   hdr<39:18> = EnvLeft[col];       // EnvLength
   hdr<45:40> = EnvPam;             // EPAM
   hdr<46> = EncEnable;             // Encryption enabled flag
   hdr<47> = EncKey;                // Encryption key index
   hdr<63:48> = LinkId[col];        // LLID
   hdr<71:64> = CRC8(hdr<63:8>);    // Calculate CRC8
   return hdr;
}
```

GetFillerEQ(int col)

The GetFillerEQ() function returns an EQ value used to fill the transmit channel when no active envelopes are available. If this function is called when the transmission channel is active, it returns an inter-envelope idle EQ (IEI_EQ). Otherwise, it returns an inter-burst idle EQ (IBI_EQ).

```
EQ GetFillerEQ( int col)
{
   if( TxActive[col] )
```


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```
        return IEI_EQ; //Inter-Envelope Idle
    else
        return IBI_EQ; //Inter-Burst Idle
}
```

GetMacBlock(link_id)

The GetMacBlock() function retrieves eight octets (64 bits) of data from a MAC identified by the link_id parameter and returns an EQ (72 bits) that contains both the data and the corresponding eight control bits. If the retrieved bits contain a partial frame preamble, the preamble is shifted forward such that the entire preamble is returned in one EQ in which case the function invokes the PLS_DATA.request() primitive up to 127 times. If no data is available from the MAC for a particular byte, the function returns an IDLE control code for that octet. This is a blocking function that returns control to the calling routine after 64 or more successive invocations of the PLS_DATA.request() primitive.

```
IdleFlag[.] = {true};
// Previous octet from a MAC (link_id)
// was an Idle. Global array of Booleans
// that retain their values between successive
// calls to GetMacBlock()
EQ GetMacBlock(int16 link_id)
{
    EQ eq; // Consists of 8 bits of control (Ctrl[0…7])
           // and 8 octets of data (Data[0…7]), as shown in Figure 143–2
    if( link_id == ESC_LLID )
        return IBI_EQ; // Inter-burst Idle
    for( octet_index = 0; octet_index < 8; octet_index++ )
    {
        tx_data = GetMacOctet( link_id ); // Get 8 bits from MAC
        if( IsIdle(tx_data) AND !IdleFlag[link_id] ) // 1st Idle after Data
        {
            IdleFlag[link_id] = true;
            eq.Ctrl[octet_index] = 1; // Store /T/ character
            eq.Data[octet_index] = 0xFD;
        }
        else if( IsIdle(tx_data) ) // Idle after Idle
        {
            eq.Ctrl[octet_index] = 1; // Store /I/ character
            eq.Data[octet_index] = 0x07;
        }
        else if( IdleFlag[link_id] ) // 1st Data after Idle
        {
            IdleFlag[link_id] = false;
            octet_index = 0; // Shift to octet 0
            eq.Ctrl[octet_index] = 1; // Store /S/ character
            eq.Data[octet_index] = 0xFB;
        }
        else // Data after Data
        {
            eq.Ctrl[octet_index] = 0; // Store Data octet
            eq.Data[octet_index] = tx_data;
        }
    }
    return eq;
}
```


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GetMacOctet(link_id)

This function returns an eight-bit vector from a MAC identified by the link_id parameter. When the MAC sublayer has data available, the return value is composed of eight OUTPUT_UNIT values (see 46.1.7.1.2) delivered by eight consecutive invocations of the PLS_DATA[link_id].request(OUTPUT_UNIT) primitive (see Figure 143–9). When the MAC sublayer has no data available (i.e., if the last seen OUTPUT_UNIT value was equal to DATA_COMPLETE), the return value is composed of eight DATA_COMPLETE values.

IsIdle(octet)

This function returns a Boolean value indicating whether the parameter octet represents a data octet or an idle octet. This function returns true if any bit in octet has a value of DATA_COMPLETE (see 46.1.7.1.2), otherwise, false is returned. Note that since MAC data output is aligned to octet boundaries, all bits in the parameter octet are either equal to DATA_COMPLETE or all bits are not equal to DATA_COMPLETE.

143.3.3.6 State diagrams

143.3.3.6.1 Input process

The MCRS shall implement the Input process as depicted in Figure 143–12.

The Input process accepts data from a MAC interface and transfers that data to the EnvTx buffer one EQ at a time. The process prepends an ESH to each envelope and overwrites each preamble with an ECH. Only one instance of the process is needed. The Input process fills one full row (all columns) of the EnvTx buffer on each cycle of InClk (InClk is half the effective rate of TX_CLK). In case of overlapping envelopes, blocks in multiple columns are retrieved from the same MAC.

The process keeps track of the envelope sizes for each LLID and does not exceed the allowed number of EQs for a given envelope. The process adjusts the MAC rate to account for FEC parity insertion in the PCS.

143.3.3.6.2 Transmit process

The MCRS shall implement the Transmit process as depicted in Figure 143–13.

The Transmit process outputs one 36-bit block (TXD[*ch*]<31:0> + TXC[*ch*]<3:0>) to its associated xMII interface on each edge of the TX_CLK signal. There is one instantiation of the Transmit process for each channel implemented in the device. The main function of the process is to transmit a column of one row from the EnvTx buffer on an existing channel. The Transmit process is synchronized to TX_CLK.

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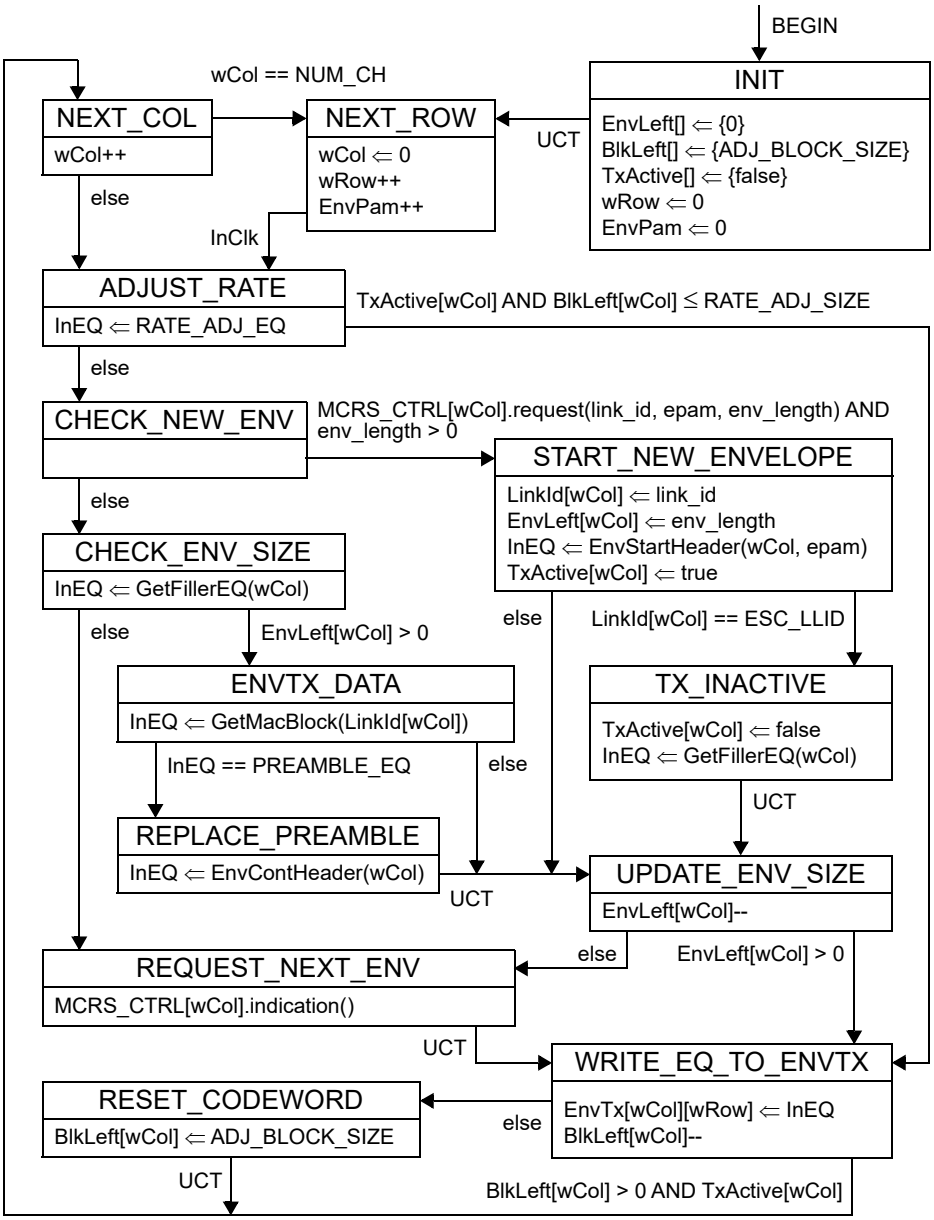

Figure 143–12—MCRS transmit function, Input process state diagram

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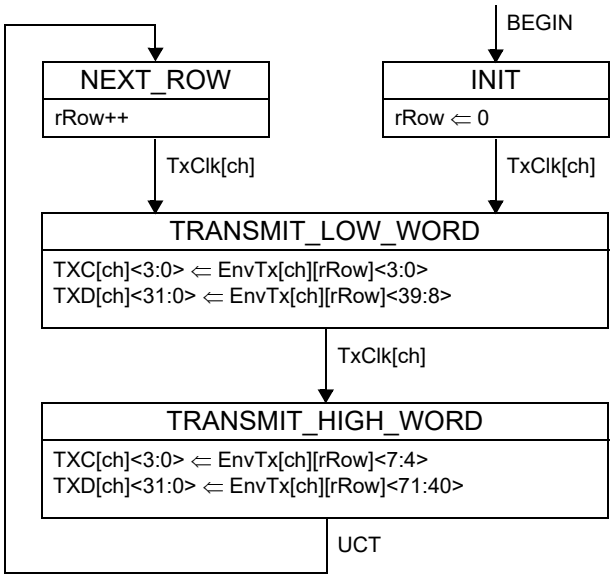

Figure 143–13—MCRS transmit function, Transmit process state diagram

143.3.4 Receive functional specifications

A functional block diagram of the MCRS receive path is illustrated in Figure 143–14. The MCRS interfaces are described in 143.3.1. The MCRS receive path is composed of two processes and one buffer. The Receive process, described in greater detail in 143.3.4.5.1, accepts two successive transfers from the associated xMII and consolidates them into an EQ, which is stored in the appropriate row of the EnvRx buffer. The Output process, described in greater detail in 143.3.4.5.2, pulls EQs from the EnvRx buffer and feeds them to the appropriate MAC as specified by the current LLID for that receive channel.

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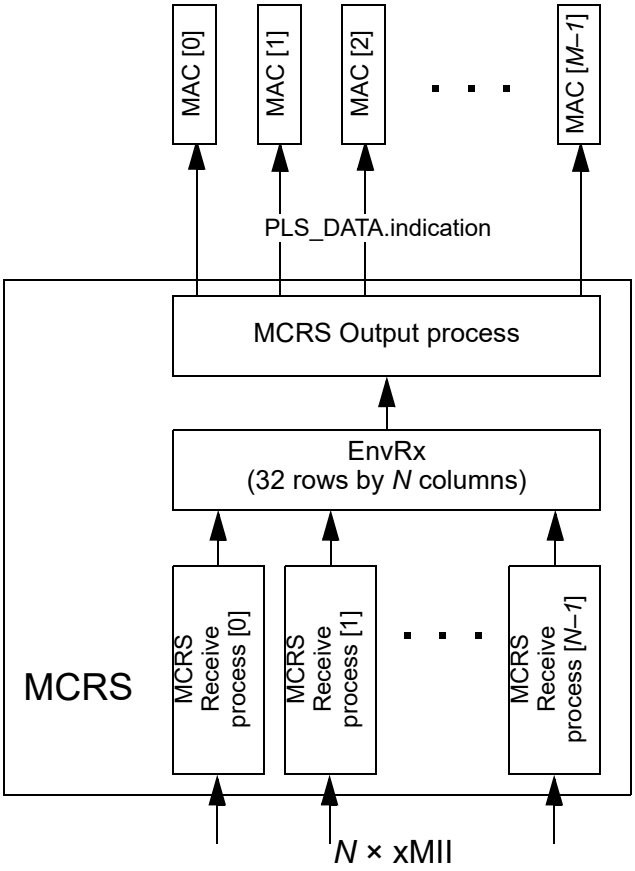

Figure 143–14—MCRS receive functional block diagram

143.3.4.1 Conventions

See 142.1.1

143.3.4.2 Constants

ES_HEADER
: Type: Integer
Description: The value of the envelope EnvType flag indicating the header is an envelope start header.
Value: 1

IEI_EQ
: See 143.3.3.3

RATE_ADJ_EQ
: See 143.3.3.3

PREAMBLE_EQ
: See 143.3.3.3

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143.3.4.3 Variables

BEGIN
See 142.2.5.2

ch
See 143.3.3.4

EnvRx
Type: array of 72-bit blocks
Description: The EnvRx buffer is used to transfer information between the MCRS Receive process and the MCRS Output process. In this buffer, each cell, represented by the variable EnvRx stores one EQ (a 72-bit block) of information. The number of columns in EnvRx buffer is NUM_CH (see 143.3.3.3). The maximum number of rows is 64, as determined by the size of EPAM field in the envelope header (see 143.3.2). For some applications, fewer rows may be sufficient. The buffer is filled in parallel by NUM_CH instances of MCRS Receive process and is emptied sequentially by the MCRS Output process. For additional details, refer to 143.2.5.3.

EnvLeft[ch]
See 143.3.3.4

LinkId[ch]
See 143.3.3.4

OutClk
Type: Boolean
Description: The OutClk clear-on-read variable is set to true on each rising edge of TX_CLK.

OutEQ
Type: 72-bit binary array
Description: A temporary holding variable for one EQ used in the Output process.

rCol
Type: Integer
Description: The rCol variable represents the EnvRx buffer column currently being read by the MCRS Output process. Each column corresponds to a separate reception channel, i.e., a separate xMII interface.

rRow
Type: 6-bit integer
Description: The rRow variable represents the EnvRx buffer row index currently being read by the MCRS Output process.

RxClk[ch]
Type: Boolean
Description: The RxClk[ch] clear-on-read variables are set to true on each edge of the RX_CLK[ch] signals and represent the continuous clock that provides the timing reference for the transfer of the RXC[ch]<3:0> and RXD[ch]<31:0> signals received on the xMII channel ch.

RxEQ
Type: 72-bit binary
Description: The RxEQ variable represents the most recent EQ received from an xMII interface.

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wCol

Type: Integer

Description: The wCol variable represents the EnvRx buffer column currently being written by the MCRS Receive process. Each column corresponds to a separate reception channel, i.e., a separate xMII interface.

wRow

Type: 6-bit integer

Description: The wRow variable represents the EnvRx buffer row index currently being written by the MCRS Receive process.

143.3.4.4 Functions

IsHeader(eq)

The IsHeader(eq) function returns true if the parameter eq represents an envelope header. An envelope header begins with a /S/ Start control character.

```
bool IsHeader(EQ eq)
{
   return(   eq<7:0> == 0x01 AND              // Control bits
             eq<15:8> == 0xFB AND             // Start Control Code /S/
             eq<71:64> == CRC8(eq<63:8>));    // Matching CRC8
}
```

IsMisaligned(eq)

The IsMisaligned(eq) function returns true if the parameter eq is misaligned, i.e., shifted by a half EQ.

```
bool IsMisaligned(EQ eq)
{
   return (  eq<7:0> == 0x1F AND           // Control bits
             eq<39:8> == IBI_EQ<71:40> AND // 1st Transfer: IBI_EQ
             eq<47:40> == 0xFB );          // 2nd Transfer: Env. Header
}
```

OutputToMac(LinkId[rCol], OutEQ)

The OutputToMac(LinkId[rCol], OutEQ) function transfers the eight information bytes in the OutEQ parameter to the MAC associated with the LLID value of LinkId[rCol] per the eight control bits in the OutEQ parameter.

```
OutputToMac(int16 link_id, EQ eq)
{
   for( octet_index = 0; octet_index < 8; octet_index++ )
   {
      if ( eq.Ctrl[octet_index] == 0 ) // Receive data octet
      {
         data_valid = true;
         rx_data = eq.Data[octet_index];
      }
      else if ( eq.Data[octet_index] == 0xFB ) // Rx /S/ character
      {
         data_valid = true;
         rx_data = 0x55; // Replace /S/ with preamble
      }
      else // Rx other ctrl. character, including /T/ (value 0xFD)
      {
```


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```
            data_valid = false;
            rx_data = 0x07; // Replace with /I/
        }
        SetMacOctet( link_id, rx_data, data_valid ); // Set 8 bits to MAC
    }
}
```

SetMacOctet(link_id, rx_data, data_valid)

This function passes eight bits of rx_data vector to the MAC instance identified by the link_id parameter. The rx_data value is passed to the MAC using eight consecutive invocations of the PLS_DATA[link_id].indication(INPUT_UNIT) primitive (see 46.1.7.2), along with eight invocations of the PLS_DATA_VALID[link_id].indication(DATA_VALID_STATUS) primitive (see 46.1.7.5). When the parameter data_valid is equal to true, the DATA_VALID_STATUS has the value of DATA_VALID. When the parameter data_valid is equal to false, the DATA_VALID_STATUS has the value of DATA_NOT_VALID.

143.3.4.5 State diagrams

143.3.4.5.1 Receive process

The ONU and OLT MCRS shall implement the Receive process as depicted in Figure 143–15.

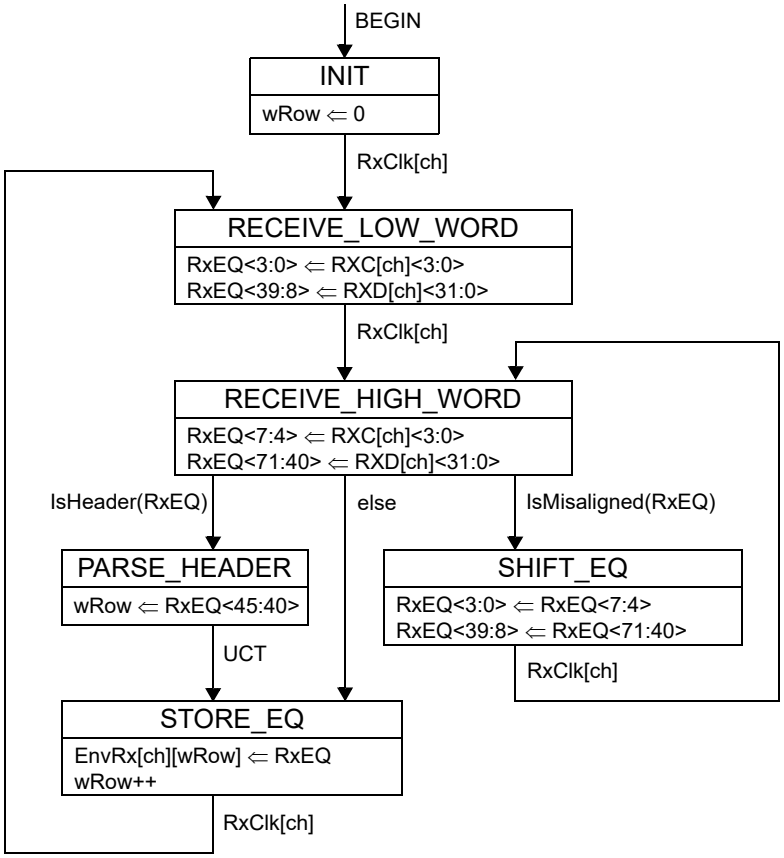

Figure 143–15—MCRS receive function, Receive process state diagram

This process forms an EQ from two successive xMII transfers. The process first verifies proper alignment of the EQ and, if misaligned, shifts the input by half of an EQ (four bytes). No other error checking is performed by this process. When an envelope header is received, the EPAM field is extracted and used as a

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write position into the EnvRx buffer. Because the phase of the receive clock (RX_CLK[ch]) in every channel is different, due to different delay and transport skew, a separate instance of the Receive process is required for each channel implemented.

143.3.4.5.2 Output process

The ONU and OLT MCRS shall implement the MCRS Output process as depicted in Figure 143–16.

The Output process outputs EQs to the proper MAC. In the case of overlapping envelopes from the same LLID, data from multiple channels is properly serialized. A corrupted header may lead to loss of a frame, but no subsequent frames are lost due to the error since the next ECH resynchronizes the process for the following frame.

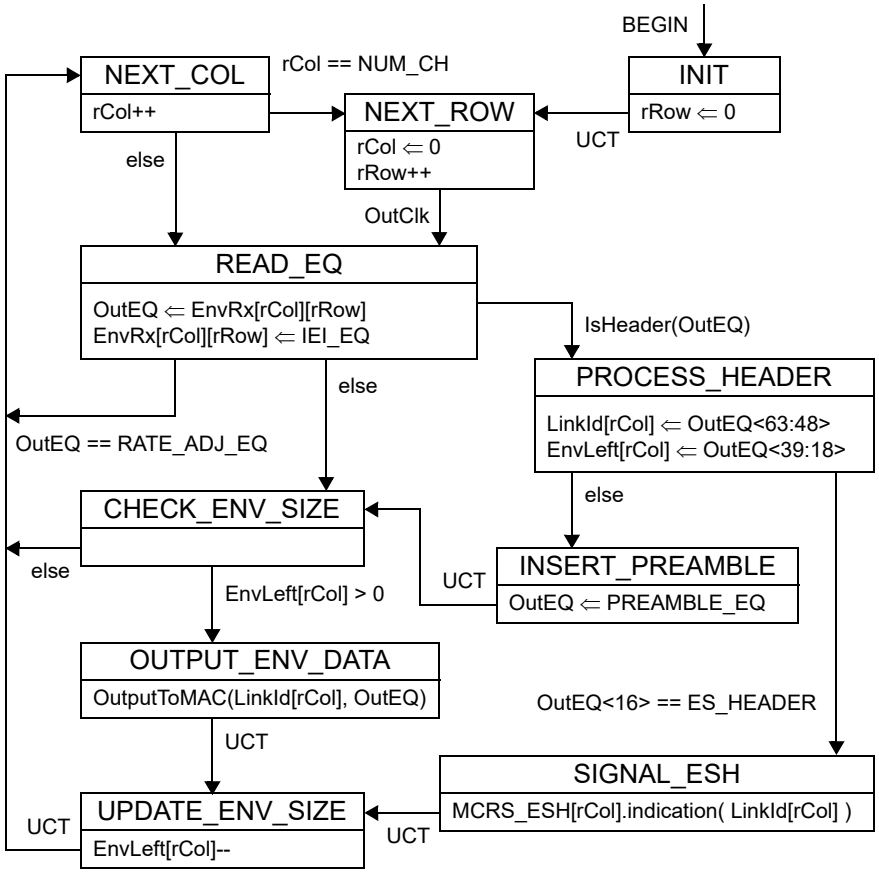

Figure 143–16—MCRS receive function, Output process state diagram

143.4 Nx25G-EPON MCRS requirements

143.4.1 Nx25G-EPON architecture

This subclause describes the MCRS requirements for Nx25G-EPON point-to-multipoint (P2MP) networks. P2MP networks are passive optical networks (PONs) that connect multiple optical network units (ONUs) to a single optical line terminal (OLT). The architecture is asymmetric, based on a tree and branch topology utilizing passive optical splitters.

A transmission direction from the OLT towards the ONUs is referred as the downstream direction and transmission direction from an ONU toward the OLT is referred as the upstream direction.

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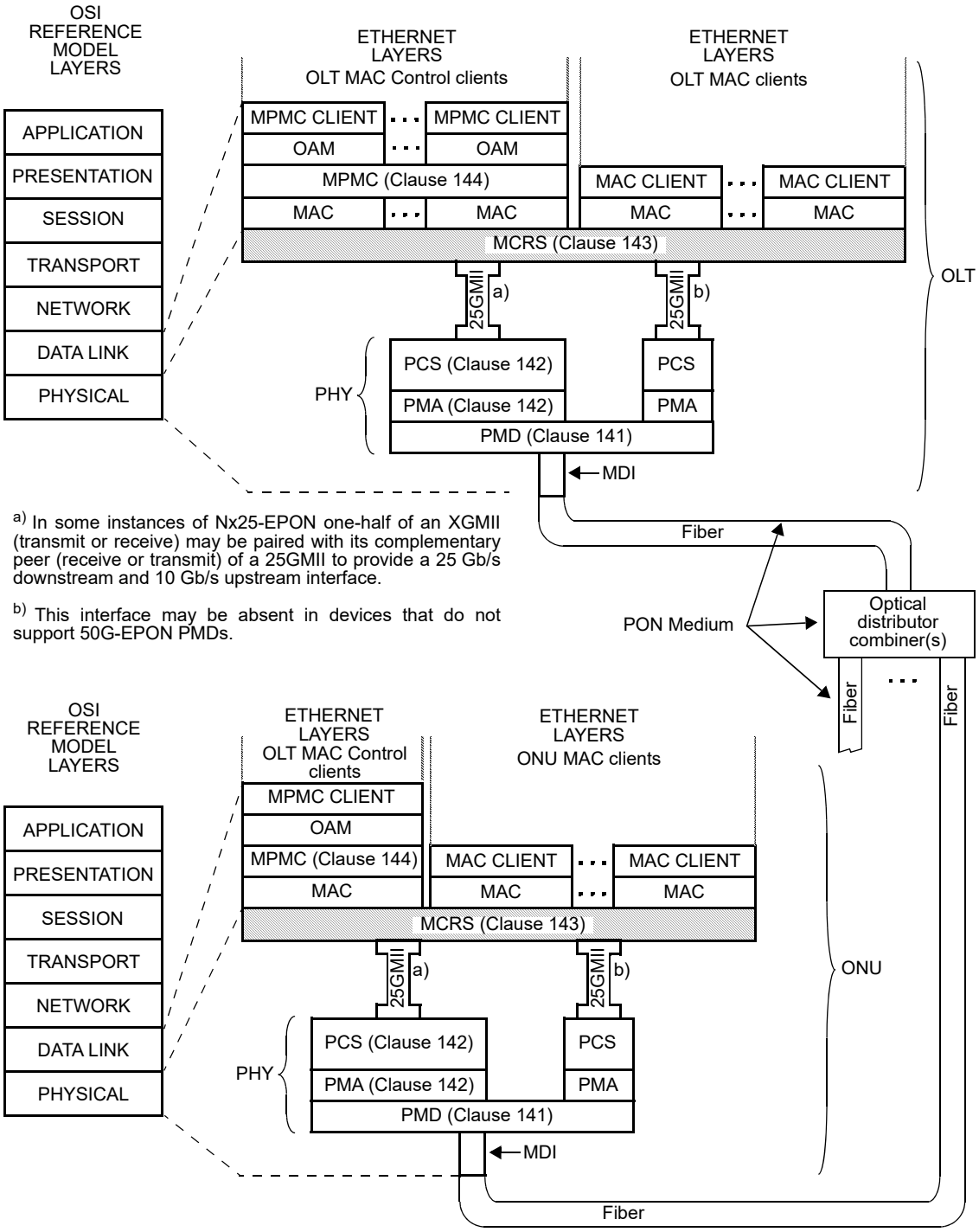

Figure 143–17—Relationship of Nx25G-EPON P2MP PMD to the ISO/IEC OSI reference model

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The MCRS is used with Nx25G-EPON point-to-multipoint (P2MP) networks in order to interface multiple MAC instances with one or two 25GMII channels in each direction. Figure 143–17 illustrates the relationship of the MCRS and the OSI protocol stack for Nx25G–EPON.

Nx25G-EPON OLT and ONU PMDs are defined in Clause 141, with the respective Nx25G-EPON PCS defined in 142.2 and 142.3.

The MCRS in Nx25G-EPON architecture serves as an interfaces sublayer between the MAC sublayer and 25GMII. The 25GMII interface is defined in Clause 106.

143.4.1.1 MCRS channels

An MCRS channel that carries information from the OLT to the ONU is referred to as the downstream channel, and the channel that carries information from an ONU to the OLT is referred to as the upstream channel.

The 25/10G-EPON and 25G/25G-EPON architectures shall implement a single MCRS channel in each direction.

The 50/10G-EPON and 50/25G-EPON architectures shall implement two MCRS channels in the downstream direction and a single channel in the upstream direction.

The 50/50G-EPON architecture shall implement two channels in each direction.

When two channels are implemented in the same direction, channel bonding of these two channels shall be supported. Table 143–6 summarizes MCRS channels for Nx25G-EPON.

Each MCRS channel is bound to a separate PCS instance via a separate xMII instance. Channels operating at 25 Gb/s are bound to 25GMII, whereas the channel operating at 10 Gb/s is bound to an XGMII instance. Thus, for any given system, there is a one-to-one correspondence between the MCRS channel count and the number of xMII instances supported.

Table 143–6—MCRS channel designation and capabilities

Designation	MCRS channel	MCRS channel function
DC0	Downstream channel 0	All ONUs receive this MCRS channel, broadcast.
DC1	Downstream channel 1	Only ONUs capable of receiving at 50 Gb/s support this MCRS channel.
UC0	Upstream channel 0	All ONUs transmit on this MCRS channel.
UC1	Upstream channel 1	Only ONUs capable of transmitting at 50 Gb/s support this MCRS channel.

143.4.1.2 Symmetric and asymmetric data rates

The Nx25G-EPON architecture supports symmetric and asymmetric data rates. The symmetric data rate systems include 25/25G-EPON or 50/50G-EPON. The asymmetric rate systems include 25/10G-EPON, 50/10G-EPON, and 50/25G-EPON.

A distinction is made regarding the underlying mechanisms of achieving the asymmetric data rates. In 25/10G-EPON systems, the asymmetric data rate is achieved via the MCRS channel rate asymmetry, where a single downstream MCRS channel DC0 operates at 25 Gb/s and a single upstream MCRS channel UC0 operates at 10 Gb/s. Additional details for MCRS implementations supporting the channel rate asymmetry are provided in 143.4.4. In 50/25G-EPON systems, the asymmetric data rate is achieved via the MCRS

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channel number asymmetry, where two MCRS channels are active in the downstream direction (DC0 and DC1), but only a single MCRS channel UC0 is active in the upstream direction. In 50/25G-EPON systems, upstream and downstream MCRS channels operate at the data rate of 25 Gb/s.

Both the channel rate asymmetry and the channel number asymmetry mechanisms may be combined, as is the case in 50/10G-EPON systems, where there are two downstream MCRS channels operating at 25 Gb/s and a single upstream MCRS channel operating at 10 Gb/s.

An Nx25G-EPON system may serve ONUs that support different numbers of MCRS channels (see 143.4.1). Therefore, some ONUs are only able to receive and transmit data on MCRS channels DC0 and UC0, some are able to receive on DC0 and DC1 and transmit on UC0 and UC1 or just on UC0.

143.4.1.3 Nx25G-EPON application-specific parameters

For definitions of constants, variables, and functions, see 143.3.3 (transmit direction) and 143.3.4 (receive direction).

143.4.1.3.1 Constants

ADJ_BLOCK_SIZE
: Value: 257

NUM_CH
: Value: 1 for devices supporting only 10 Gb/s or 25 Gb/s operation over a single channel; 2 for devices supporting 50 Gb/s operation over two channels.

RATE_ADJ_SIZE
: Value: 33

143.4.1.3.2 Transmit variables

EnvTx
: Description: Since there is no timing jitter or channel skew to be removed at the transmitting device, the size of the EnvTx buffer may be reduced to only two rows. If this optimization is implemented, the variables rRow and wRow are represented by 1-bit unsigned integers.

143.4.2 MCRS time synchronization

For MCRS to provide the intended skew and jitter remediation capabilities, a sufficient delay margin has to be built into the MCRS buffering at the ONU and the OLT. Such delay margin is established at the ONU registration time by proper setting of MCRS EnvRx read and write pointers at the OLT and the ONU.

Upon power-up or reset, an unregistered ONU synchronizes to the received clock and aligns to 257-bit block and FEC codeword boundaries on each of its active (enabled) receive channels (see ONU Synchronizer process, 142.3.5.5). After that, the received data is passed to FEC decoder, which introduces a near-constant delay. Corrected data from the FEC decoder is passed to xMII and is received into the ONU MCRS EnvRx buffer.

The following are the ONU rules for setting the EnvRx write and read pointers:

a) Write pointer
   1) The ONU MCRS always sets the write pointer for the EnvRx buffer to equal the EPAM value in any envelope header it receives, regardless of the LLID value in that envelope header.

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2) If multiple receive channels are active, the write pointers are set independently for each channel based on EPAM values in envelope headers received on each channel.

b) Read Pointer
   1) The read pointer increments synchronously with the LocalTime counter, which is locked to the xMII receive clock of the active (enabled) receive channel with the lowest index.
   2) In an unregistered ONU, upon every update of a write pointer associated with the receive channel with the lowest index, the read pointer is also updated according to the following equation:

$$ReadPointer = WritePointer \text{ XOR } 0x20 \quad (143–1)$$

In the OLT, the PCS receiver synchronizes on start-of-burst delimiter (see OLT Synchronizer process, 142.3.5.5) independently on each active (enabled) receive channel. After that, the received data is passed to the FEC decoder, which introduces a near-constant delay. Corrected data from the FEC decoder is passed to the xMII and is received into the OLT MCRS EnvRx buffer. The following are the OLT rules for setting the EnvRx write and read pointers:

a) Write pointer
   1) When receiving an envelope from a registered ONU, the OLT MCRS sets the write pointer for the EnvRx buffer to equal the EPAM value in the envelope header.
   2) When receiving an envelope from an unregistered ONU, the OLT MCRS sets the write pointer according to the following equation:

$$WritePointer = ReadPointer \text{ XOR } 0x20 \quad (143–2)$$

NOTE—The OLT MCRS determines that an envelope is from an unregistered ONU by either checking the LLID value in the envelope header (DISC_PLID) or by checking that an envelope header is received during the discovery window (see 144.1.1.3). Otherwise, the envelope is assumed to be received from a registered ONU.

b) Read Pointer
   1) The read pointer increments synchronously with the LocalTime counter, which is locked to the xMII transmit clock.
   2) If the OLT implements multiple transmit channels, all these channels share the same xMII transmit clock. Correspondingly, the read pointers for all channels increment synchronously and maintain equal values.

The above set of rules produces a delay of 32 EQT that is built into the ONU MCRS receive path and a similar delay of 32 EQT that is built into the OLT MCRS receive path. Therefore, the total round-trip delay measured by the MPCP (see 144.3.1.1) during an ONU discovery and registration includes a built-in margin of 64 EQT that is used to eliminate skew between different channels or the timing jitter within a channel.

143.4.3 Delay variability constraints

The MPCP relies on strict timing based on the distribution of timestamps. The MCRS is designed to allow a delay variability of up to 64 EQTs. During the normal operation of a registered ONU, the delay any EQ experiences in the EnvRx buffer is complementary to the accumulated skew and jitter that this EQ encounters after leaving the EnvTx buffer in the transmitting MCRS, such that the sum of the two delays remains constant.

143.4.4 Asymmetric rate operation

The 25/10G-EPON and 50/10G-EPON systems are characterized by channel rate asymmetry. In such systems, downstream transmission uses one or two channels operating at 25 Gb/s, while the upstream transmission uses a single channel operating at 10 Gb/s.

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Figure 143–18 illustrates the layering diagram of a 25/10G-EPON OLT and ONU. In the OLT, the MCRS sublayer serves MAC entities supporting the transmit data rate of 25 Gb/s and the receive data rate of 10 Gb/s. In turn, the MCRS sublayer is connected to the transmit path of a 25GMII and the receive path of an XGMII. In the ONU, the MCRS sublayer serves MAC entities supporting the transmit data rate of 10 Gb/s and the receive data rate of 25 Gb/s. The MCRS sublayer is connected to the transmit path of an XGMII and the receive path of a 25GMII.

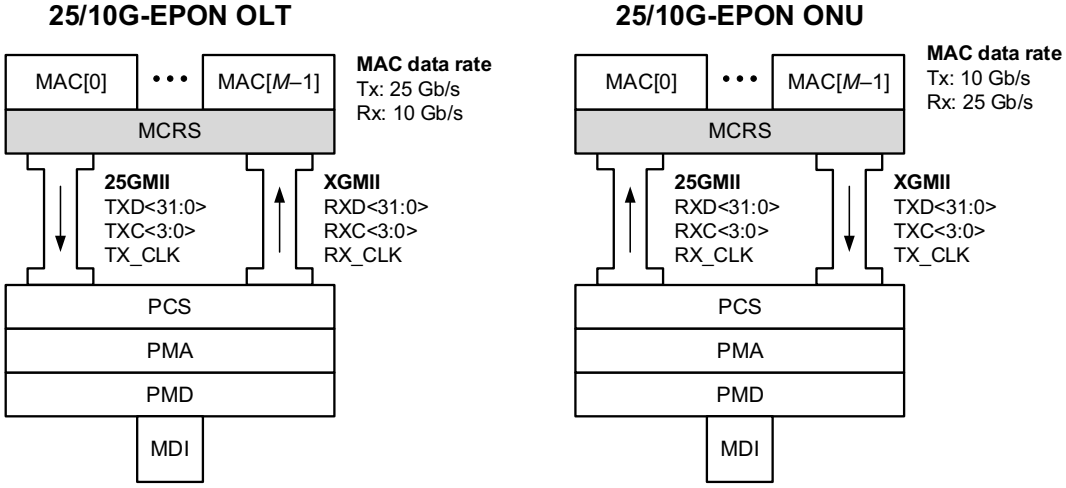

Figure 143–18—25G/10G-EPON OLT and ONU layering diagram

Because of the required close coupling between the MCRS clock (InClk, see 143.3.3.4 and OutClk, see 143.3.4.3) and MPCP clock (LocalTime, see 144.2.1.2), the MCRS buffer read pointers advance by one every EQT, i.e., both downstream and upstream channels within MCRS operate at a nominal data rate of 25 Gb/s. To adapt the MCRS channel rate to the MAC data rate of 10 Gb/s, the MCRS channel is throttled by inserting a padding EQ at the rate of 3 padding EQs per every 5 EQTs. The transfer of information through the 10 Gb/s MCRS channel is illustrated in Figure 143–19.

The padding EQs are interleaved with information EQs using the following pattern:

<information EQ> <padding EQ> <padding EQ> <information EQ> <padding EQ>

The usage of the padding EQs is entirely confined to the MCRS sublayer and does not affect the definition of interfaces to either of the adjacent sublayers. Therefore the definition of the padding EQ format and values are left to implementations.

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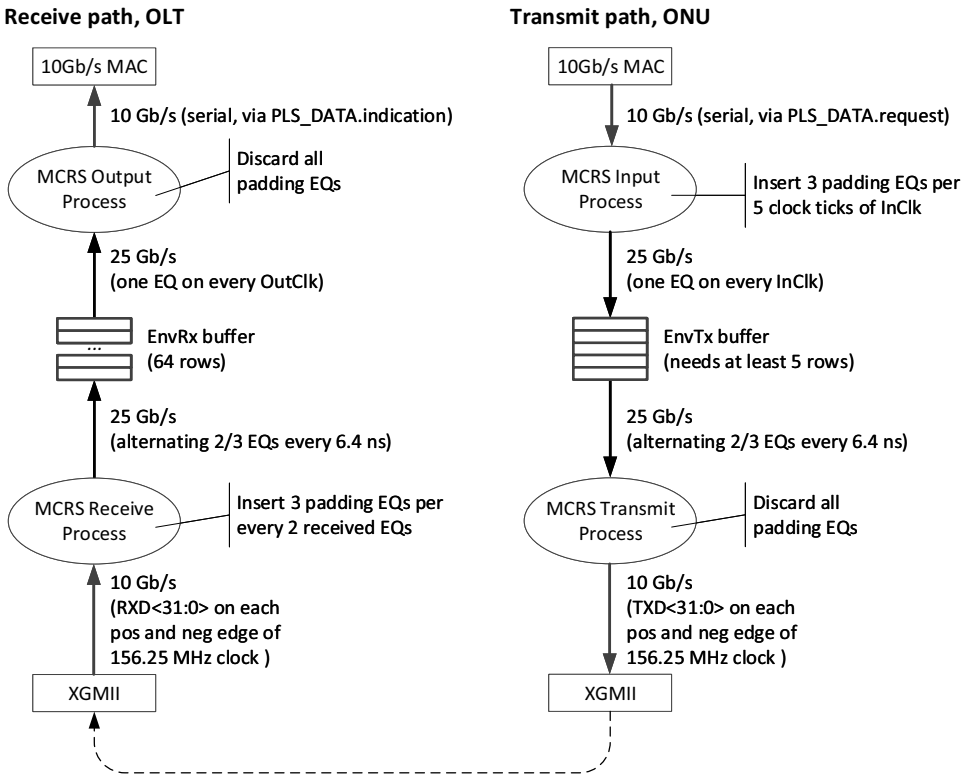

Figure 143–19—Upstream channel operating at 10 Gb/s

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143.5 Protocol implementation conformance statement (PICS) proforma for Clause 143, Multi-Channel Reconciliation Sublayer[237]

143.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 143, Multi-Channel Reconciliation Sublayer, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

143.5.2 Identification

143.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

143.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 143, Multi-Channel Reconciliation Sublayer
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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143.5.3 Generic MCRS

Item	Feature	Subclause	Value/Comment	Status	Support
MC1	Envelope header structure	143.3.2	Uses the format shown in Figure 143–10	M	Yes [ ]
MC2	Input process	143.3.3.6.1	Implements the state diagram as depicted in Figure 143–12	M	Yes [ ]
MC3	Transmit process	143.3.3.6.2	Implements the state diagram as depicted in Figure 143–13	M	Yes [ ]
MC4	Receive process	143.3.4.5.1	Implements the state diagram as depicted in Figure 143–15	M	Yes [ ]
MC5	Output process	143.3.4.5.2	Implements the state diagram as depicted in Figure 143–16	M	Yes [ ]

143.5.4 MCRS in Nx25G-EPON

143.5.4.1 Major capabilities/option

Item	Feature	Subclause	Value/Comment	Status	Support
*2510G	25/10G-EPON functionality	143.4.1.1	Device supports functionality required for 25/10G-EPON	O.1	Yes [ ] No [ ]
*2525G	25/25G-EPON functionality	143.4.1.1	Device supports functionality required for 25/25G-EPON	O.1	Yes [ ] No [ ]
*5010G	50/10G-EPON functionality	143.4.1.1	Device supports functionality required for 50/10G-EPON	O.1	Yes [ ] No [ ]
*5025G	50/25G-EPON functionality	143.4.1.1	Device supports functionality required for 50/25G-EPON	O.1	Yes [ ] No [ ]
*5050G	50/50G-EPON functionality	143.4.1.1	Device supports functionality required for 50/50G-EPON	O.1	Yes [ ] No [ ]

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143.5.4.2 MCRS implementation in Nx25G-EPON

Item	Feature	Subclause	Value/Comment	Status	Support
EPON1	Number of MCRS channels	143.4.1.1	Implement a single channel in downstream direction and a single channel in upstream direction	2510G:M or 2525G:M	Yes [ ] N/A [ ]
EPON2	Number of MCRS channels	143.4.1.1	Implement two channels in downstream direction and a single channel in upstream direction	5010G:M or 5025G:M	Yes [ ] N/A [ ]
EPON3	Number of MCRS channels	143.4.1.1	Implement two channels in downstream direction and two channels in upstream direction	5050G:M	Yes [ ] N/A [ ]
EPON4	Channel bonding	143.4.1.1	Device supports channel bonding	50G10G:M or 50G25G:M or 50G50G:M	Yes [ ] N/A [ ]

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144. Multipoint MAC Control for Nx25G-EPON

144.1 Overview

This clause defines the mechanisms and control protocols required in order to reconcile the 25 Gb/s or 50 Gb/s passive optical network (PON) into the Ethernet framework. A PON is an optical network with no active elements in the signal's path from source to destination. The only interior elements used in a PON are passive optical components, such as optical fiber, splices, and splitters. When combined with the Ethernet protocol, such a network is referred to as an Ethernet passive optical network (EPON).

Topics covered in this clause include allocation of transmission resources in EPON, discovery and registration of EPON devices, and reporting queue occupancy to higher layers to facilitate dynamic bandwidth allocation schemes and statistical multiplexing across the PON.

This clause does not address specific bandwidth allocation strategies, authentication of end devices, quality-of-service definitions, provisioning, or management.

The Multipoint MAC Control (MPMC) sublayer defined in this clause includes two protocols:

— Multipoint Control Protocol (MPCP) responsible for arbitration of TDM-based access to the P2MP medium
— Channel Control Protocol (CCP) responsible for querying and control of multiple channels within the Nx25G-EPON PHY

The MPMC functionality shall be implemented for subscriber access devices containing point-to-multipoint (P2MP) Physical Layer devices defined in Clause 141 and Clause 142.

144.1.1 Principles of point-to-multipoint operation

A P2MP medium is an asymmetric medium based on a tree (or trunk-and-branch) topology. The DTE connected to the trunk of the tree is called an optical line terminal (OLT) and the DTEs connected at the branches of the tree are called optical network units (ONUs). The OLT typically resides at the service provider's facility, while the ONUs are located at the subscriber premises. A simplified P2MP topology example is depicted in Figure 144–1. Clause 67 provides additional examples of P2MP topologies.

144.1.1.1 Transmission arbitration

In the downstream direction (from the OLT to an ONU), signals transmitted by the OLT pass through a 1:*N* passive splitter (or cascade of splitters) and reach each ONU.

In the upstream direction (from the ONUs to the OLT), the signal transmitted by an ONU would only reach the OLT, but not other ONUs. To avoid upstream data collisions, transmission windows (grants) for all ONUs are controlled in such a way that only a single ONU's transmission reaches the OLT at any given time. The MPCP (see 144.3) is responsible for timing and arbitrating the ONU transmissions. This arbitration is achieved by allocating transmission windows (grants) to ONUs. An ONU defers its transmission until the start of its transmission window. When the transmission window starts, the ONU transmits its queued frames at full line rate for the duration of this transmission window.

Reporting of a queue occupancy state or congestion by different ONUs assists in optimal allocation of the transmission windows across the PON.

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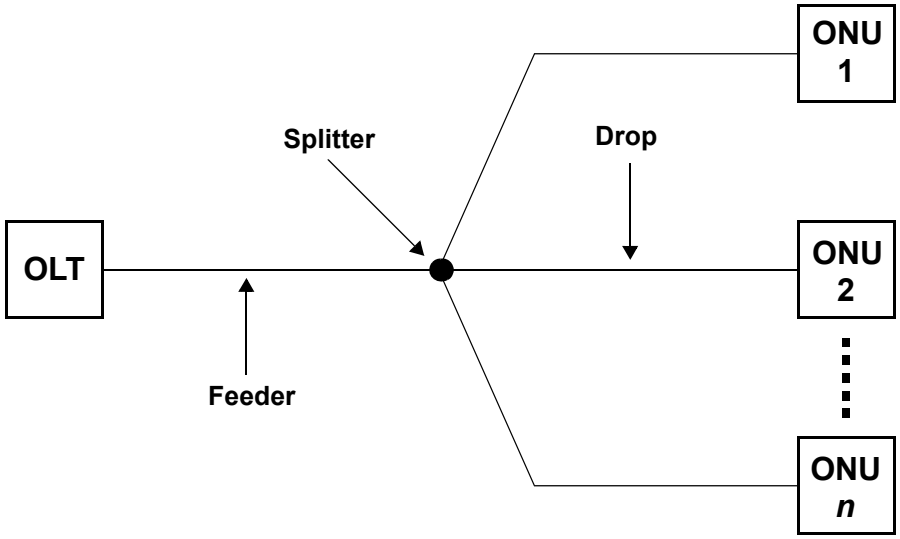

Figure 144–1—PON topology example

144.1.1.2 Concept of logical links

OLT and ONU devices instantiate multiple MAC instances (see Figure 144–2). P2MP architectures are best viewed as a collection of logical point-to-point and/or P2MP links. A logical link is created in the Multi-Channel Reconciliation Sublayer (MCRS), below the MAC by tagging each frame (or frame fragment) with a logical link identification (LLID) value and binding each instance of a MAC to a specific LLID value. See 143.2.1 for explanation of the mechanism of logical link operation.

A logical connection is formed when a MAC instance at the OLT and a MAC instance at the ONU are bound to the same LLID value. A point-to-point logical link connects a single MAC instance at the OLT to a single MAC instance at the ONU. A P2MP logical link takes advantage of the broadcasting nature of the P2MP topology and connects a single MAC instance at the OLT to multiple MAC instances in different ONUs. In a P2MP logical link, MAC instances in multiple ONUs are bound to the same LLID value.

By default, the OLT is connected to each ONU via two point-to-point logical links: one link is used for MPMC traffic, such as MPCPDUs (see 144.3) and the other link is used for management traffic, such as OAMPDUs (see Clause 57). These two connections per each ONU are established during the Discovery process (see 144.3.5).

Several single-copy broadcast logical links are pre-defined for specific purposes (see Table 144–1).

Additional point-to-point and/or P2MP links between the OLT and ONUs may be provisioned by network management based on specific access network configuration and service requirements. Provisioning of such additional logical links is outside the scope of this standard. Different types of logical links are described in 144.3.4.

Although the OLT and ONUs instantiate multiple MAC entities, each device may use a single MAC address. Within the EPON Network, MAC instances are uniquely identified by their LLID.

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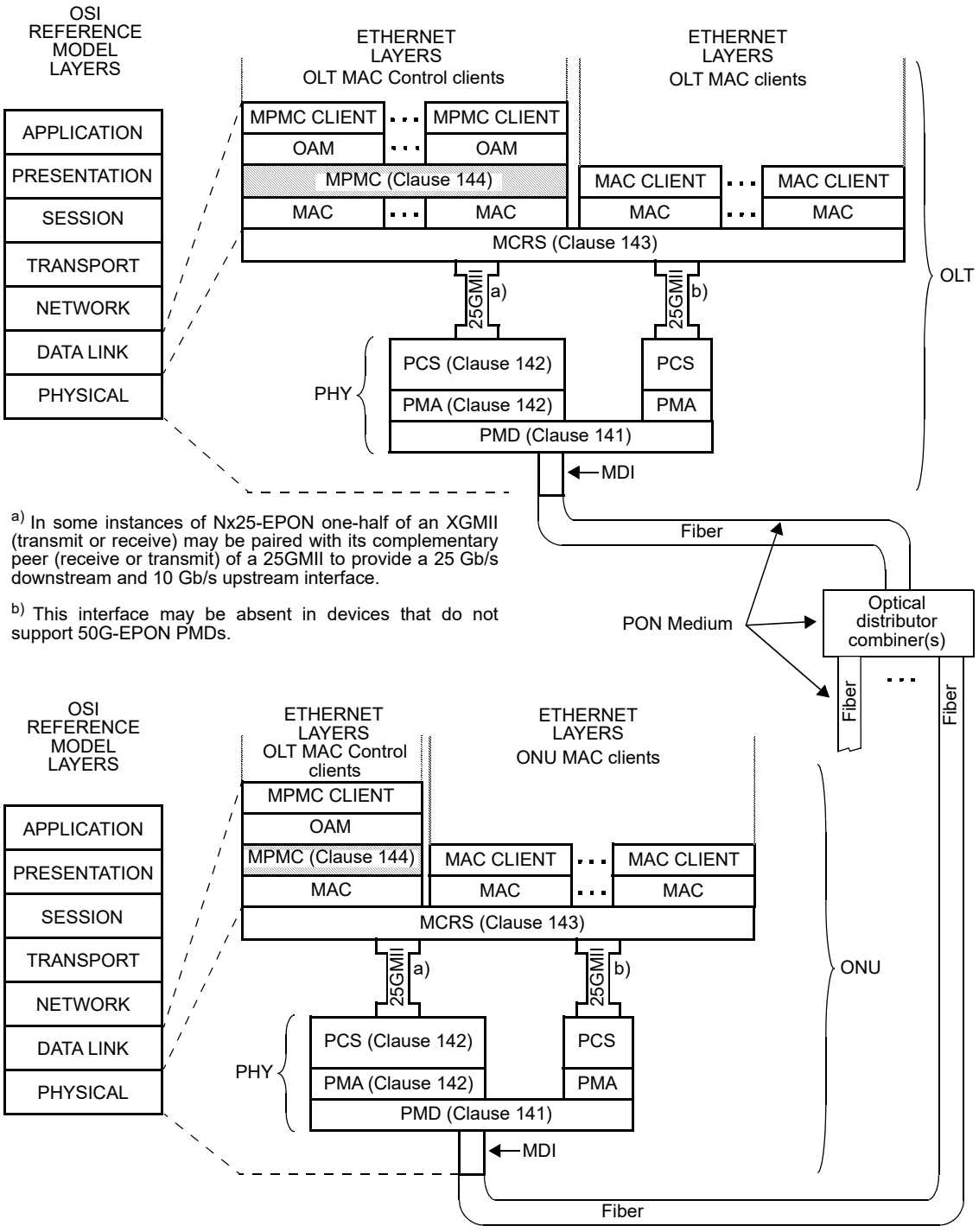

a) In some instances of Nx25-EPON one-half of an XGMII (transmit or receive) may be paired with its complementary peer (receive or transmit) of a 25GMII to provide a 25 Gb/s downstream and 10 Gb/s upstream interface.

b) This interface may be absent in devices that do not support 50G-EPON PMDs.

MPMC described in this clause

25GMII= 25 GIGABIT MEDIA INDEPENDENT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE
OLT = OPTICAL LINE TERMINAL
MCRS= MULTI-CHANNEL RECONCILIATION SUBLAYER
MPMC= MULTI-POINT MAC CONTROL
ONU = OPTICAL NETWORK UNIT
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 144–2—Relationship of EPON P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

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144.1.1.3 ONU discovery and registration

As was explained in 144.1.1.1, the upstream transmissions in an EPON are arbitrated by the OLT. Before any newly connected ONU can be scheduled for the upstream transmission, it needs to be discovered by the OLT. The Discovery process is used to detect the newly-connected ONUs.

At a high level, the Discovery process schedules a periodic discovery window – a timeslot during which only the unregistered ONUs are allowed to transmit their registration request. These registration request messages allow the OLT to learn the MAC address and to measure the round-trip propagation time of each new ONU. As part of the Discovery process, the new ONU is assigned its initial LLID values (see 144.1.1.2) and that allows this ONU to receive downstream traffic and also be scheduled for the upstream transmission.

The Discovery process is described in more detail in 144.3.7.

144.1.2 Position of Multipoint MAC Control (MPMC) within the IEEE 802.3 hierarchy

Figure 144–2 depicts the architectural positioning of the MPMC sublayer with respect to the MAC and the MPMC client. The MPMC sublayer extends the MAC Control sublayer to support multiple clients and additional MAC control functionality.

144.1.3 Functional block diagram

Figure 144–3 and Figure 144–4 provide a functional block diagram of the MPMC architecture for the OLT and the ONU, respectively.

144.1.4 Service interfaces

The MAC clients communicate directly with dedicated MAC instances using the standard service interface specified in 2.3. The MPMC does not interface with any MAC Clients.

The MPMC clients communicate with MPMC instances using the service interface defined in this clause. Each MPMC instance communicates with the underlying MAC sublayer using the standard service interface specified in 4A.3.2. Similarly, MPMC communicates internally using primitives and interfaces consistent with definitions in Clause 31.

144.1.4.1 MAC Control service (MCS) interface

The MCS interface is an interface between the MAC Control sublayer and the MPMC client above it (see Figure 144–3 and Figure 144–4). The definition and behavior of the MPMC client is outside the scope of this standard.

The MAC Control sublayer and the MPMC client communicate via MCS:MA_CONTROL.indication and MCS:MA_CONTROL.request primitives. In the state diagrams used in this clause, the following abbreviations are used:

- MCSI(indication_operand_list) is equivalent to:
  MCS:MA_CONTROL.indication(opcode, indication_operand_list), as defined in 31.3.2.
- MCSR(request_operand_list) is equivalent to:
  MCS:MA_CONTROL.request(destination_address, opcode, request_operand_list), as defined in 31.3.1.

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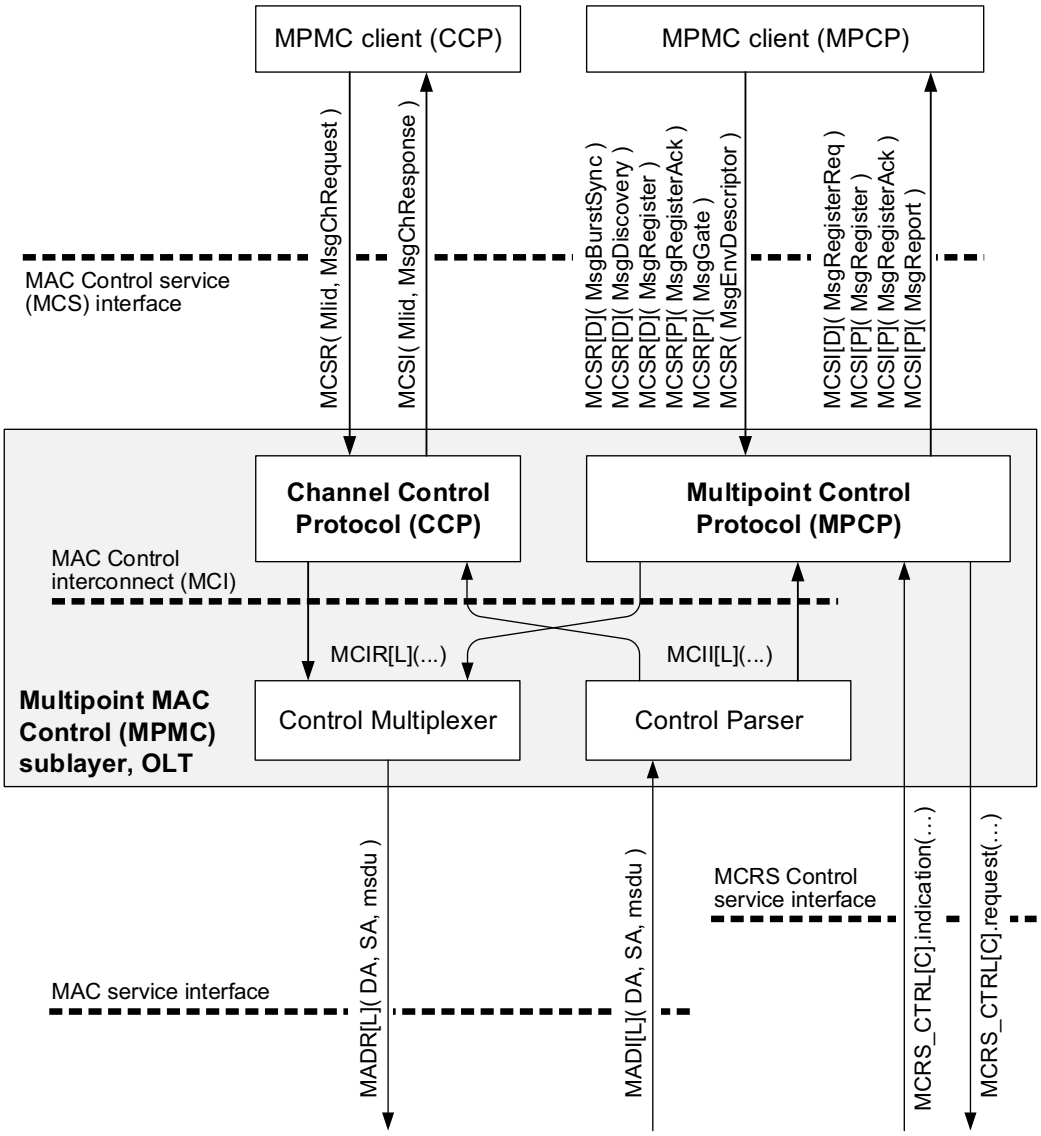

Figure 144–3—OLT Multipoint MAC Control (MPMC) sublayer functional block diagram

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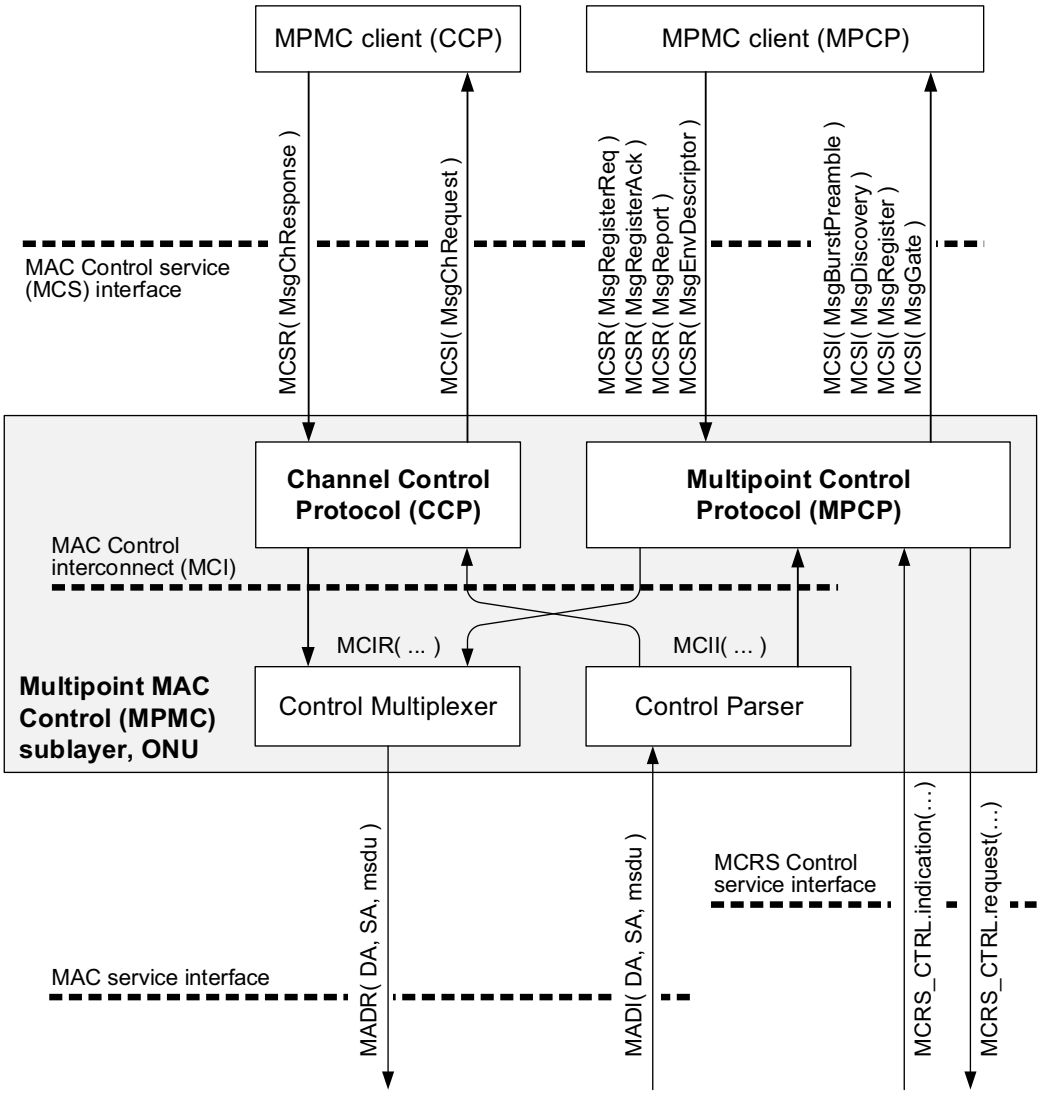

Figure 144–4—ONU Multipoint MAC Control (MPMC) sublayer functional block diagram

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144.1.4.2 MAC Control interconnect (MCI)

MCI is an internal interface between the Control Parser/Control Multiplexer and other opcode-specific functions of the MAC Control sublayer (see Figure 144–3 and Figure 144–4).

The Control Parser and Control Multiplexer communicate with opcode-specific functions via MCI:MA_CONTROL.indication and MCI:MA_CONTROL.request primitives. In the state diagrams used in this clause, the following abbreviations are used:

— MCII(indication_operand_list) is equivalent to:
MCI:MA_CONTROL.indication(opcode, indication_operand_list), as defined in 31.3.2.
— MCIR(request_operand_list) is equivalent to:
MCI:MA_CONTROL.request(destination_address, opcode, request_operand_list), as defined in 31.3.1.

144.1.4.3 MAC service Interface

The MAC service interface is an interface between the MAC sublayer and the MAC Control sublayer above it (see Figure 144–3 and Figure 144–4).

The MAC sublayer and MAC Control sublayer communicate via MAC:MA_DATA.indication and MAC:MA_DATA.request primitives. The following abbreviations are used in this clause:

— MADI(destination_address, source_address, mac_service_data_unit) is equivalent to:
MAC:MA_DATA.indication(destination_address, source_address, mac_service_data_unit, frame_check_sequence, reception_status), as defined in 2.3.2.
— MADR(destination_address, source_address, mac_service_data_unit) is equivalent to:
MAC:MA_DATA.request(destination_address, source_address, mac_service_data_unit, frame_check_sequence), as defined in 2.3.1.

144.1.4.4 MCRS Control interface

The MCRS Control interface is an interface between the MAC Control sublayer and the Multi-Channel Reconciliation Sublayer (see Clause 143). The MCRS Control interface is used to control the timing of envelope transmission over a multi-channel P2MP media.

The MAC Control sublayer and the MCRS communicate via the MCRS_CTRL.indication and MCRS_CTRL.request primitives.

144.1.5 Conventions

See 142.1.1

144.2 Protocol-independent operation

As depicted in Figure 144–3 and Figure 144–4, the MPMC comprises the following functional blocks:

a) Control Parser. This block is responsible for parsing MAC Control frames, as well as interfacing with Clause 31 entities, and opcode-specific blocks.
b) Control Multiplexer. This block is responsible for selecting the source of the frames to be transmitted.

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144.2.1 Control Parser and Control Multiplexer

The Control Parser (see Figure 144–5) is responsible for opcode-independent parsing of MAC frames and forwarding these frames to other processes for opcode-specific operations. The Control Parser also extracts the value of the Timestamp field from all MPCPDUs that contain this field and checks whether the timestamp drift value is within the acceptable range. There are no interfaces connecting the Control Parser to MAC Clients.

The Control Multiplexer (see Figure 144–6) is responsible for forwarding frames received from multiple opcode-specific processes to the underlying MAC sublayer. The Control Multiplexer inserts the timestamp value into all MPCPDUs that carry the Timestamp field. There are no interfaces connecting the Control Multiplexer to MAC Clients.

144.2.1.1 Constants

DRIFT_THOLD
: Type: Integer
Description: This constant holds the maximum amount of drift allowed before a timestamp drift error is declared. Exceeding this drift causes ONU deregistration (either self-deregistration or deregistration by the OLT).
Value: 2 (for the receive channels operating at 25 Gb/s) or 3 (for the receive channels operating at 10 Gb/s)
Unit: EQT

144.2.1.2 Counters

LocalTime
: Type: 32-bit unsigned
Description: This variable holds the value of the local timer used to control MPCP operation. This variable is advanced by a timer at 390.625 MHz, and is equivalent to one EQT. At the OLT the counter shall track the 25GMII transmit clock, while at the ONU the counter shall track the 25GMII receive clock. For accuracy of the receive clock, see 142.4.4.1. In the ONU, this variable is updated with the received timestamp value by the Control Parser process (see 144.2.1.5).

144.2.1.3 Variables

BEGIN
: See 142.2.5.2

FirstTimestamp[Plid]
: Type: Boolean
Description: This variable indicates whether any MPCPDU with the given Physical Layer ID (PLID) value has been seen before or not. The FirstTimestamp[Plid] variable is initialized to true for any PLID value. After an MPCPDU is received from the MAC instance corresponding to the given PLID, the FirstTimestamp[Plid] is reset to false and does not change for the given PLID anymore.

msdu
: See the definition of mac_service_data_unit in 2.3.1.2.

opcode
: Type: 16-bit unsigned integer
Description: This variable represents the opcode value of the outgoing (in the Control Multiplexer) or incoming (in the Control Parser) MPCPDU.

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LatchedTime[]

Type: An array of 32-bit unsigned integers

Description: Each element of this array represents the value of the LocalTime counter (see 144.2.1.2) latched at the moment when the MCRS_ESH.indication(Llid) primitive was generated. The elements of the array are indexed by the Llid values.

Rtt[Plid]

Type: 24-bit unsigned integer

Description: This variable holds the measured round-trip time to the ONU. At the OLT, Rtt[DISC_PLID] is zero. At the ONU, Rtt[PLID] is zero.

Unit: EQT

SupportedOpcodes

Type: list of 16-bit unsigned integers

Description: A list of all supported opcodes (see Table 31A–1).

Timestamp

Type: 32-bit unsigned integer

Description: In the Control Multiplexer state diagram, this variable holds the PLID-specific value of timestamp to be inserted into an outgoing MPCPDU. In the Control Parser state diagram this variable represents the value of the Timestamp field of the received MPCPDU.

TsDelta

Type: 32-bit signed integer

Description: This variable represents the difference between the time that ESH was read from the MCRS EnvRx buffer (i.e., the LatchedTime[Plid]) and the Timestamp value in an MPCPDU that followed that ESH. In the ONU, the TsDelta is used to adjust the LocalTime value, while in the OLT it is used as the measurement of the round-trip time to the ONU that sourced the given MPCPDU.

TimestampOpcodes

Type: list of 16-bit unsigned integers

Description: A list of all MPCPDU opcodes that contain the Timestamp field (see Table 31A–1).

TimestampDrift

Type: Boolean

Description: This variable is used to indicate whether an uncorrectable timestamp drift was detected (when set to true) or not (when set to false). An uncorrectable timestamp drift causes an immediate PLID deregistration (see DeregistrationTrigger in 144.3.7.3, Figure 144–21, and Figure 144–22).

144.2.1.4 Functions

ProcessTimestamp (Plid, TsDelta)

This function takes the PLID and a parameter TsDelta, which represents the difference between the local time and the timestamp value in a received MPCPDU. This function checks whether the timestamp drift has exceeded the predefined device-specific threshold DRIFT_THOLD. In the ONU, this function sets the LocalTime counter based on the value of the received Timestamp field (see 144.3.1.1). In the OLT, this function measures the RTT value when the first timestamped MPCPDU is received on a given PLID link. Note that in the ONU, the RTT value is always zero. The ProcessTimestamp function is defined as follows:

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```
ProcessTimestamp( Plid, TsDelta )
{
   if( FirstTimestamp[Plid] )
   {
      // The following line is executed only in the ONU
      LocalTime -= TsDelta;

      // The following line is executed only in the OLT
      Rtt[Plid] = TsDelta;

      TimestampDrift[Plid] = false;
      FirstTimestamp[Plid] = false;
   }
   else
      TimestampDrift[Plid] = abs(TsDelta) > DRIFT_THOLD
}
```

144.2.1.5 Control Parser state diagram

The OLT and ONU shall implement the Control Parser state diagram shown in Figure 144–5.

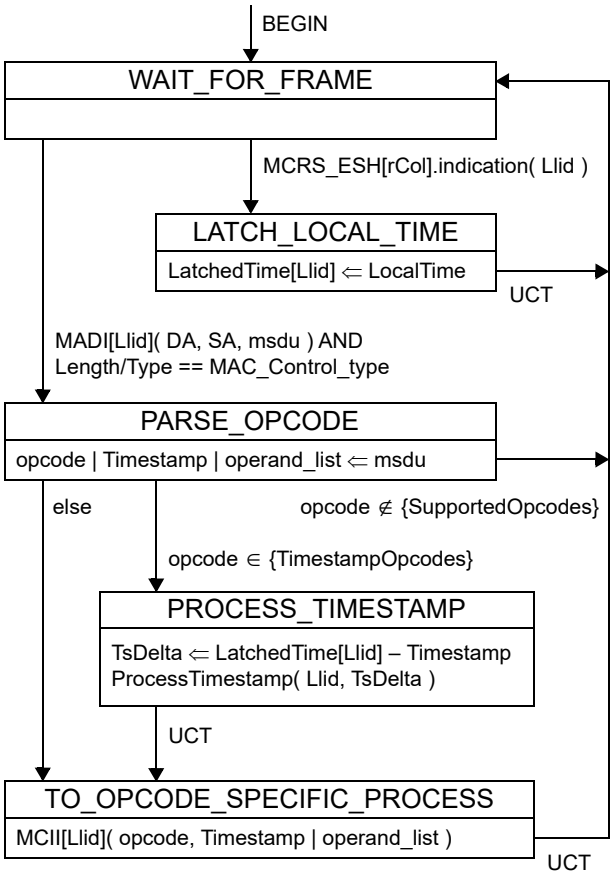

Figure 144–5—Control Parser state diagram

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144.2.1.6 Control Multiplexer state diagram

The OLT and ONU shall implement the Control Multiplexer state diagram shown in Figure 144–6.

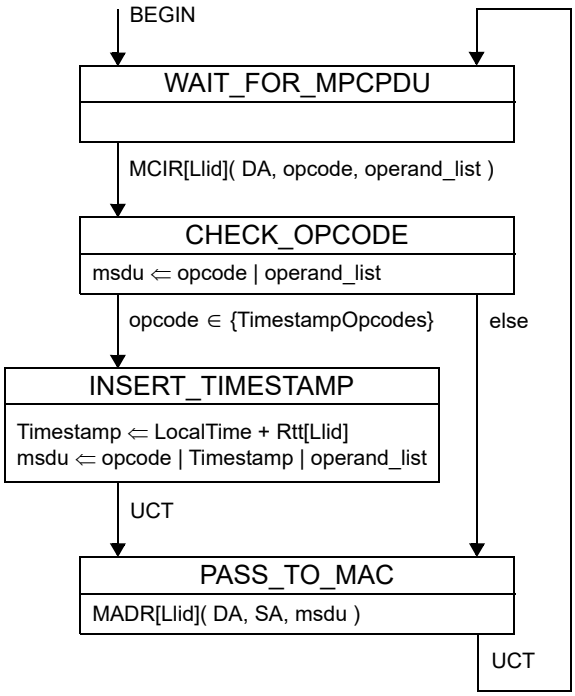

Figure 144–6—Control Multiplexer state diagram

144.3 Multipoint Control Protocol (MPCP)

144.3.1 Principles of Multipoint Control Protocol (MPCP)

In a TDM-based PON, the access to the shared physical medium needs to be arbitrated (see 144.1.1.1). The main purpose of the MPCP described in this subclause is to arbitrate transmissions in Nx25G-EPON. To achieve this goal, the MPCP includes processes that measure the range (i.e., round-trip propagation time) and maintain time synchronization between the OLT and ONUs (see 144.3.1.1) and processes that allow the OLT to assign transmission windows to individual logical links (see 144.3.3).

144.3.1.1 Ranging measurement and time synchronization

Both the OLT and the ONU have 32-bit counters (LocalTime) that increment by one every EQT. In the OLT, the LocalTime counter is synchronized with the OLT 25GMII transmit clock and increments synchronously with InClk (see 143.3.3.4). In the ONU, the LocalTime counter is synchronized with the 25GMII receive clock and increments synchronously with OutClk (see 143.3.3.4). In the ONUs supporting multiple downstream (receive) channels, the LocalTime counter is synchronized with the 25GMII receive clock of the active (enabled) channel with the lowest index.

The LocalTime counters supply the timestamp value for MPCPDUs transmitted by either device. The time reference point for the timestamp value is the transmission time of the envelope start header (ESH) of the envelope that includes the MPCPDU (see 143.3.2). In situations where multiple MPCPDUs are transmitted within a single envelope, all these MPCPDUs shall have the same timestamp value, referencing the transmission time of the ESH.

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Note that the actual arrival times of MPCPDUs to the MAC Control sublayer do not affect the timing synchronization mechanism. MPCPDUs may get delayed in the transmitting MAC if, for example, the MAC is paused to allow for the MCRS rate adjustment or FEC parity insertion between the ESH and the MPCPDU.

The ONU ranging (i.e., round-trip propagation time) is measured during the ONU initial discovery and registration. The measured range value also includes the nominal delays of 32 EQT through the ONU MCRS receive data path and 32 EQT through the OLT MCRS receive data path (see 143.4.2).

The method of ranging measurement is illustrated in Figure 144–7. It consists of the following steps:

1) The OLT Discovery process transmits a DISCOVERY MPCPDU with a timestamp value equal to the LocalTime counter at the time when the MCRS_CTRL.request primitive is generated by the Envelope Activation process. This is also the time when the ESH is written into the EnvTx FIFO (see 143.3.1.2.1). Accordingly, the EPAM field of the ESH header matches the six least-significant bits of the LocalTime (LocalTime<5:0>).
2) When an unregistered ONU receives the DISCOVERY MPCPDUs, it sets its LocalTime counter based on the value in the Timestamp field in the received MPCPDU. From this moment, the LocalTime counter continues to increment synchronously with the 25GMII receive clock.
3) After the ONU's LocalTime counter reaches the value of GrantStartTime and an additional random delay, the ONU Registration process transmits the REGISTER_REQ MPCPDU with Timestamp field value equal to the LocalTime counter at the time when the MCRS_CTRL.request primitive is generated by the Envelope Activation process. This is also the time when the ESH is written into the EnvTx FIFO (see 143.3.1.2.1). Accordingly, the EPAM field of the ESH header matches the six least-significant bits of the LocalTime (LocalTime<5:0>).
4) When the OLT receives MPCPDUs, it uses the received Timestamp field value to calculate the round-trip time between the OLT and the ONU. The round-trip time (RTT) is equal to the difference between the OLT's LocalTime counter at the moment when the ESH is read from the MCRS EnvRx buffer and the Timestamp field value in the REGISTER_REQ MPCPDU.

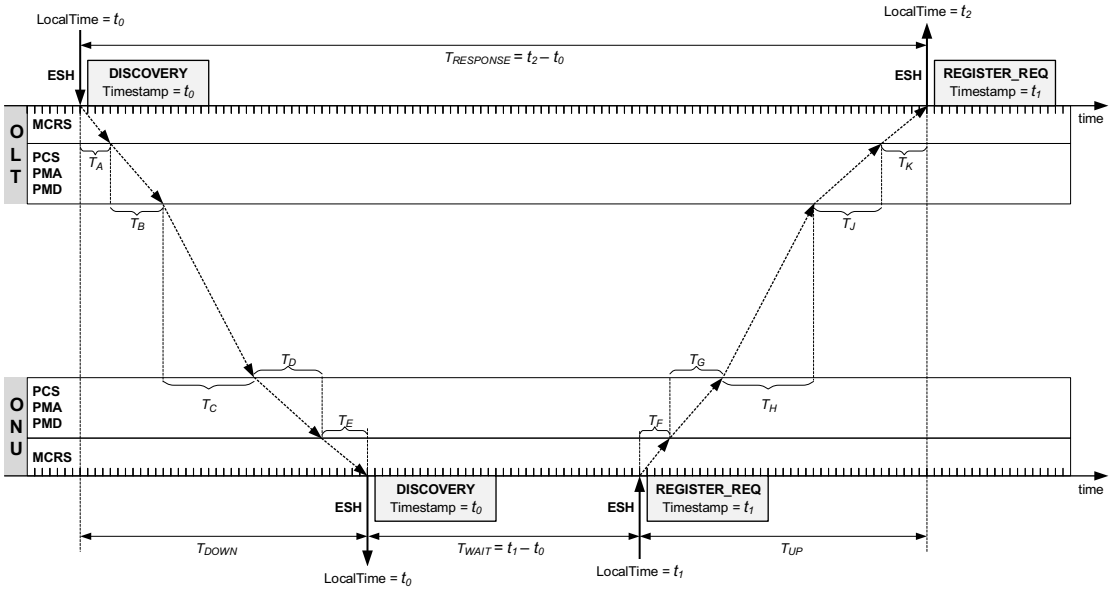

Figure 144–7—Ranging measurement

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In the downstream direction, the combined delay T_{DOWN} includes the following delay components:

— T_A – delay through the transmit data path of the OLT MCRS sublayer.
— T_B – delay through the transmit data path of the OLT PCS, PMA, and PMD sublayers. This delay also includes FEC encoding delay.
— T_C – downstream optical signal propagation delay in fiber. In EPON systems supporting multiple downstream channels, this delay may be different on different channels.
— T_D – delay through the receive data path of the ONU PCS, PMA, and PMD sublayers. This delay also includes FEC decoding (correction) delay.
— T_E – delay through the receive data path of the ONU MCRS sublayer. During initial ranging, this delay is equal to 32 EQT (see 143.4.2). After the initial ranging, the delay T_E becomes inversely-correlated with the sum of delays T_A, T_B, T_C, and T_D, such that T_{DOWN} remains nearly-constant with only ± 1 EQT of variability.

In the upstream direction, the combined delay T_{UP} includes the following delay components:

— T_F – Delay through the transmit data path of the ONU MCRS sublayer.
— T_G – Delay through the transmit data path of the ONU PCS, PMA, and PMD sublayers. This delay also includes FEC encoding delay.
— T_H – Upstream optical signal propagation delay in fiber. In EPON systems supporting multiple upstream channels, this delay may be different on different channels.
— T_J – Delay through the receive data path of the OLT PCS, PMA, and PMD sublayers. This delay also includes FEC decoding (correction) delay.
— T_K – Delay through the receive data path of the OLT MCRS sublayer. During initial ranging, this delay is equal to 32 EQT (see 143.4.2). After the initial ranging, the delay T_K becomes inversely-correlated with the sum of delays T_F, T_G, T_H, and T_J, such that T_{UP} remains nearly-constant with only ± 1 EQT of variability.

As was stated above, the RTT value is equal to the difference between t_2 (the OLT's LocalTime counter at the moment when the ESH is received) and t_1 (the Timestamp field value in the REGISTER_REQ MPCPDU). Below is the derivation of this RTT value:

a) From the illustration in Figure 144–7, the total response time $T_{RESPONSE}$ (an interval of time from sending ESH with the DISCOVERY MPCPDU to the ONU and receiving ESH with the REGISTER_REQ MPCPDU from the ONU) is: $T_{RESPONSE} = t_2 - t_0$.
b) On the other hand, $T_{RESPONSE} = T_{DOWN} + T_{WAIT} + T_{UP}$, where $T_{WAIT} = t_1 - t_0$.
c) Thus, $t_2 - t_0 = T_{DOWN} + t_1 - t_0 + T_{UP}$.
d) RTT = $T_{DOWN} + T_{UP} = t_2 - t_1$.

Once the RTT is measured, the GATE Generation process for the new PLID is instantiated. That process is responsible for generating the GATE MPCPDUs to the registered ONU (PLID). All MPCPDUs sent by the OLT on unicast PLIDs have the Timestamp field value pre-compensated by the RTT associated with this PLID:

Timestamp[LLID] = LocalTime + RTT[LLID]

The effect of such pre-compensation is that the first ESH in any burst from an ONU arrives to the OLT MCRS EnvRx buffer approximately 32 EQT before their GrantStartTime values and this ESH is read from the EnvRx buffer into the associated MAC instance at the time when the OLT's LocalTime counter value is equal to GrantStartTime (see Figure 144–8).

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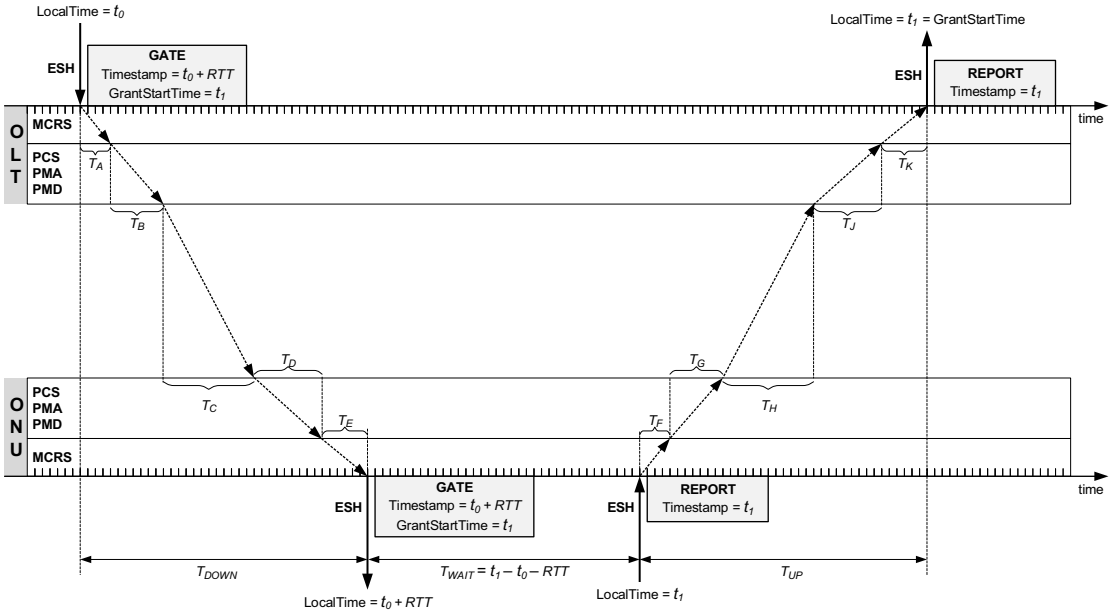

Figure 144–8—Illustration of GrantStartTime alignment

Another effect of the timestamp pre-compensation is that the Timestamp field value in a received MPCPDU is expected to match the LocalTime value at the time the MPCPDU is received. (As stated above, the timestamp reference point is the time the ESH is read from the EnvRx buffer).

A condition of timestamp drift error occurs if the OLT's and ONU's LocalTime counters lose their synchronization or mutual alignment. This condition can be independently detected by the OLT or an ONU. This condition is detected when an absolute difference between the Timestamp value received in an MPCPDU and the LocalTime counter exceeds the timestamp drift threshold limit DRIFT_THOLD (see 144.2.1.4). The timestamp drift error causes an immediate ONU deregistration.

After the ONU receives the REGISTER MPCPDU with its assigned PLID and management link ID (MLID), it stops processing any MPCPDUs received in envelopes with DISC_PLID. At this time, the ONU is ready to accept its first GATE received on the newly-assigned unicast PLID. The timestamp in this GATE MPCPDU is pre-compensated with ONU's RTT, and therefore, the ONU is expected to measure a large difference between the received Timestamp value and its LocalTime counter. This large difference that is detected immediately after registration is expected and the ONU does not recognize it as a timestamp drift error (see ProcessTimestamp in 144.2.1.4).

144.3.1.2 Granting access to the PON media by the OLT

To allow ONUs' access to the PON media, the OLT issues GATE MPCPDUs (see 144.3.6.1). A GATE MPCPDU contains a transmission start time (StartTime field) and transmission allocations (EnvAlloc[i] field) for up to seven LLIDs. The OLT may grant more than seven LLIDs by issuing multiple GATE MPCPDUs with the same StartTime value.

A GATE MPCPDU may be transmitted on any downstream channel and it may allocate upstream transmission windows on any or all upstream channels. An ONU ignores all the transmission allocations for the upstream channels that are not enabled in that ONU.

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The ONU processes the GATE MPCPDUs in the order they are received and generates the upstream envelopes following the order of EnvAlloc[i] fields in each GATE MPCPDU. Therefore, it is possible for an LLID to be allocated multiple disjoint envelopes within the same grant.

As is explained in 143.3.1.2.3 and in 144.3.1.1, the value of the Timestamp field in MPCPDUs references the transmission (and reception) time of the ESH preceding these MPCPDUs. For that reason, the OLT shall never allocate overlapping envelopes to the PLID, except the fully-overlapping envelopes (see Figure 143–5).

In the case that the ONU is given partially overlapping PLID envelope allocations, it shall choose only one of these envelopes for MPCPDU transmission, and only if the envelope length is enough for at least one complete MPCPDU. The ONU ignores the rest of the overlapping PLID envelope allocations.

144.3.2 MPCP block diagram

Figure 144–9 illustrates a functional block diagram of the MPCP for the OLT. The MPCP in the OLT includes the following processes:

— GATE Generation process (see 144.3.8.7)
— Discovery Initiation process (see 144.3.7.6)
— Registration Completion process (see 144.3.7.7)
— Envelope Commitment process (see 144.3.8.9)
— Envelope Activation process (see 144.3.8.11)

In the OLT, a separate instance of the GATE Generation process and a separate instance of the Registration Completion process are created for each registered ONU (PLID, see 144.3.4).

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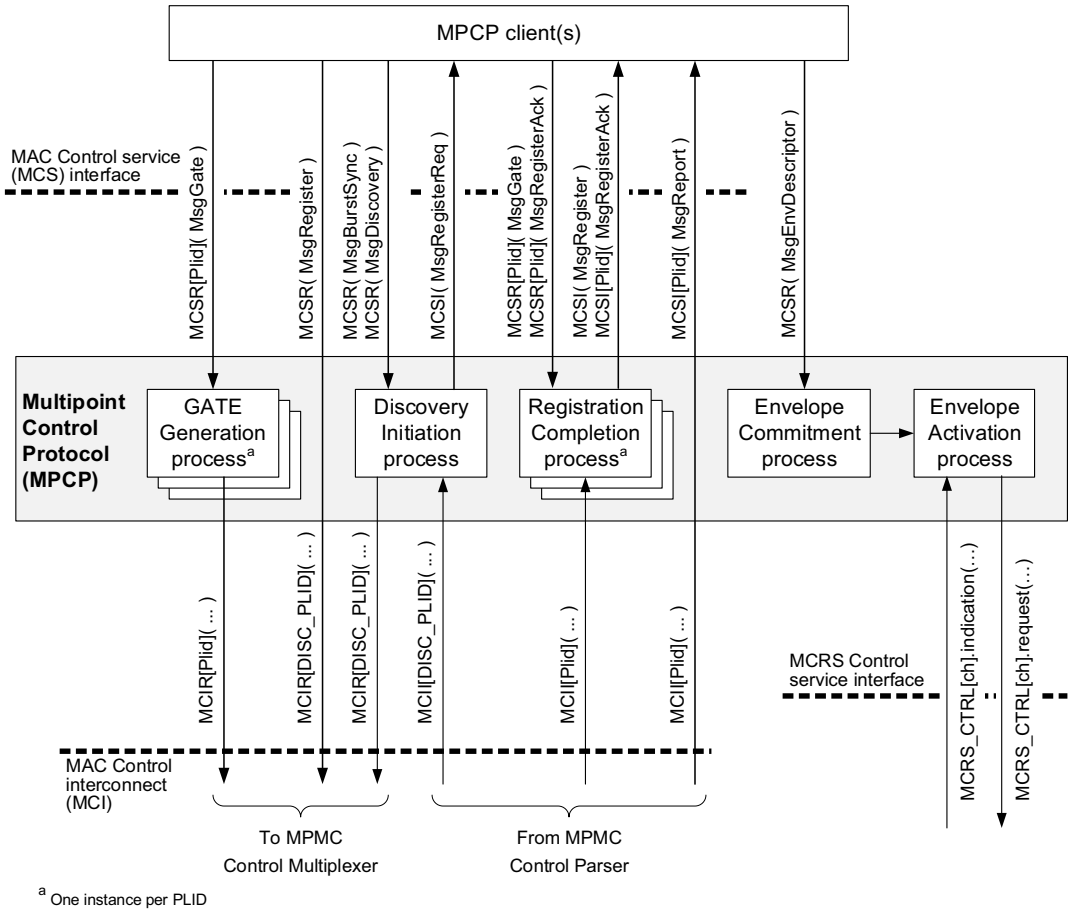

Figure 144–9—OLT Multipoint Control Protocol (MPCP) functional block diagram

Figure 144–10 illustrates a functional block diagram of the MPCP for the ONU. The MPCP in the ONU includes the following processes:

— ONU Registration process (see 144.3.7.8)
— GATE Reception process (see 144.3.8.8)
— Envelope Commitment process (see 144.3.8.10)
— Envelope Activation process (see 144.3.8.11)

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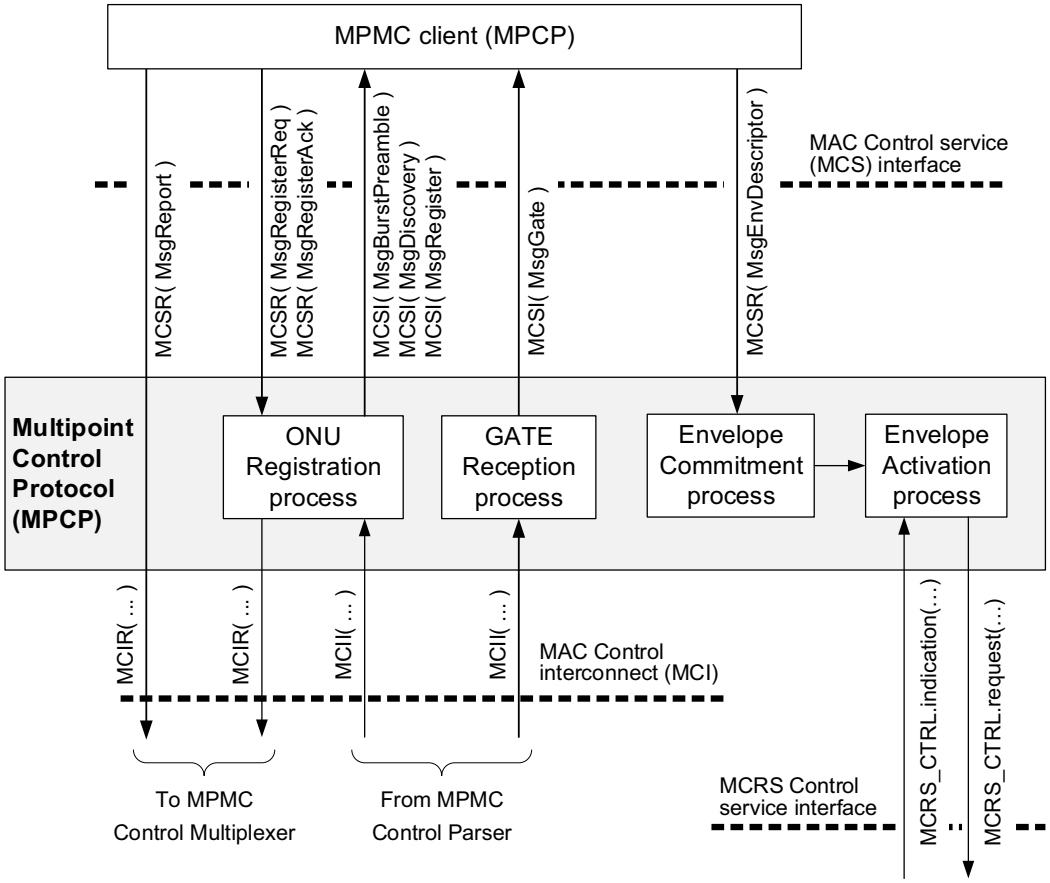

Figure 144–10—ONU Multipoint Control Protocol (MPCP) functional block diagram

144.3.3 Delay variability requirements

The MPCP protocol relies on strict timing based on distribution of timestamps. A compliant implementation needs to guarantee a constant delay through the MAC and PHY in order to maintain the correctness of the timestamping mechanism. The actual delay is implementation dependent; however, a complying implementation shall maintain the combined delay variation through the MAC and PHY of less than one EQT for channels operating at 25.78125 GBd and less than two EQTs for channels operating at 10.3125 GBd.

144.3.4 Logical link identifier (LLID) types

144.3.4.1 Physical Layer ID (PLID)

The PLID carries messages used to control critical Nx25G-EPON operations, such as ONU registrations and arbitration of ONUs' access to the PON medium. All Multipoint Control Protocol data units (MPCPDUs) are transported using the PLID. A successful ONU Discovery and Registration process, described in 144.3.7.8, results in the assignment of a single unique PLID value to the ONU.

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144.3.4.2 Management link ID (MLID)

The MLID carries management traffic flows, such as OAMPDUs (see 57.4) and CCPDUs (see 144.4). Each ONU is assigned a single unique MLID value as part of the ONU Discovery and Registration process, described in 144.3.7.8.

144.3.4.3 User link ID (ULID)

User link IDs (ULIDs) carry subscriber traffic. It is expected that a single subscriber may be assigned one or more ULIDs to allow for separation of traffic classes and types. ULID values are assigned (provisioned) to an ONU using an appropriate management protocol outside the scope of this standard. ULID values need not have a one-to-one binding of an OLT MAC to an ONU MAC. A ULID that binds a single OLT MAC to multiple MACs in different ONUs represents a multicast ULID.

144.3.4.4 Group link ID (GLID)

To assist in traffic management the Nx25G-EPON system supports consolidation of several LLIDs into arbitrary groups using the group link ID (GLID). For example, all LLIDs for a specific subscriber hosted on an ONU servicing numerous subscribers could be grouped together into a single GLID; in another example all LLIDs supporting a specific traffic class (e.g., best-effort traffic) on a multi-subscriber ONU could be grouped together. GLID values are used only for the purposes of bandwidth granting by the OLT and reporting by the ONU. The GLID report contains the sum of all queue lengths of member LLIDs from that ONU. The bandwidth granted to a GLID is distributed among its member LLIDs. The method by which the granted bandwidth is distributed among the member LLIDs is outside the scope of this standard. The actual envelope transmission is identified by a PLID, an MLID, or a ULID value, associated with a specific MAC instance that sourced the data (i.e., the LLID field in the envelope headers may only contain a PLID, MLID, or ULID, but never a GLID).

144.3.5 Allocation of LLID values

Table 144–1 shows the allocation of LLID values.

Table 144–1—Allocation of LLID values

LLID value	Designation	Description
0x00-00	ESC_LLID	The ESC_LLID is used in the GATE MPCPDU to indicate an empty EnvAlloc[n] field or in the REPORT MPCPDU to indicate an empty LlidStatus field. The ESC_LLID is also used in the MCRS_CTRL.request primitive to mark the end of an upstream burst.
0x00-01	DISC_PLID	PLID value used for discovery of unregistered ONUs.
0x00-02	BCAST_PLID	PLID value reserved for MPCPDU broadcast.
0x00-03	BCAST_MLID	MLID value reserved for broadcast of management frames (OAMPDUs).
0x00-04 to 0x0F-FF	N/A	Reserved.
0x10-00 to 0xFF-FF	N/A	The range of LLID values available for allocation to PLID, MLID, ULID, or GLID. The values may be allocated to form unicast, multicast, or broadcast connections. LLID allocation policy is outside the scope of this standard.

The OLT and the ONUs shall not transmit envelopes with ESC_LLID or a reserved value in the LLID field, and they shall ignore the received envelopes with any of these LLID values.

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An unregistered ONU shall accept only the envelopes containing the DISC_PLID value in the LLID field. The envelopes with other LLID values shall be ignored.

Upon successful registration, an ONU shall no longer accept envelopes with DISC_PLID. Instead, a registered ONU shall accept all envelopes containing any of the following LLID values:

— The specific PLID value assigned to this ONU during registration
— The specific MLID value assigned to this ONU during registration
— Broadcast PLID (BCAST_PLID)
— Broadcast MLID (BCAST_MLID)
— Any ULID or GLID assigned to this ONU by management[238]

144.3.6 MPCPDU structure and encoding

The MPCPDU structure is shown in Figure 144–11, and is further defined as follows:

— DestinationAddress:
In MPCPDUs, the DestinationAddress is the MAC Control Multicast address as specified in the annexes to Clause 31, or the individual MAC address associated with the PLID to which the MPCPDU is destined.

— SourceAddress:
In MPCPDUs, the SourceAddress is the individual MAC address associated with the PLID through which the MPCPDU is transmitted. For MPCPDUs originating at the OLT, this may be the address of any individual MAC. These MACs may all share a single unicast address, as explained in 144.1.1.2.

— Length/Type:
In MPCPDUs this field carries the MAC_Control_type field value as specified in 31.4.1.3.

— Opcode:
This field identifies the specific MPCPDU being encapsulated. Opcode field values are defined in Table 31A–1.

— OperandList:
A set of opcode-specific fields as defined in 144.3.6.1 through 144.3.6.7.

— Pad:
This field is present only when the total length of the OperandList is below 44 octets. The Pad field is added to bring the MPCPDU length up to the minimum frame size (see 4A.2.3.2.4). This field is filled with zeros on transmission, and is ignored on reception.

— FCS:
This is the frame check sequence, typically generated by the MAC.

[238]After registration, an ONU may be configured to use multiple ULID or GLID values via management. The method of provisioning of these additional ULID or GLID values is outside the scope of this standard.

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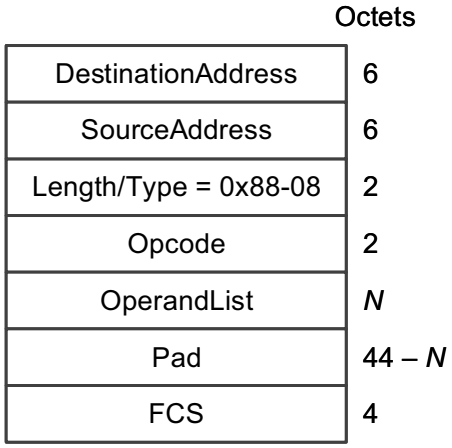

Figure 144–11—Generic MPCPDU

Fields within a frame are transmitted from top to bottom. When consecutive octets are used to represent a single numerical value, the most significant octet is transmitted first, followed by successively less significant octets. Bits within each octet are transmitted from LSB to MSB.

144.3.6.1 GATE description

The purpose of the GATE message is to grant transmission windows to ONUs for upstream transmission on the shared medium. A single grant to an ONU may consist of multiple GATE MPCPDUs, all having the same StartTime value. Up to seven envelope allocations can be carried in a single GATE MPCPDU. Only envelope allocations with a non-zero value for the LLID field are processed by the ONU. A GATE MPCPDU with no EnvAlloc (i.e., all LLID fields equal to zero) is valid and may be used as an MPCP keep alive from the OLT to the ONU.

The GATE MPCPDU is an instantiation of the Generic MPCPDU and shall be as shown in Figure 144–12.

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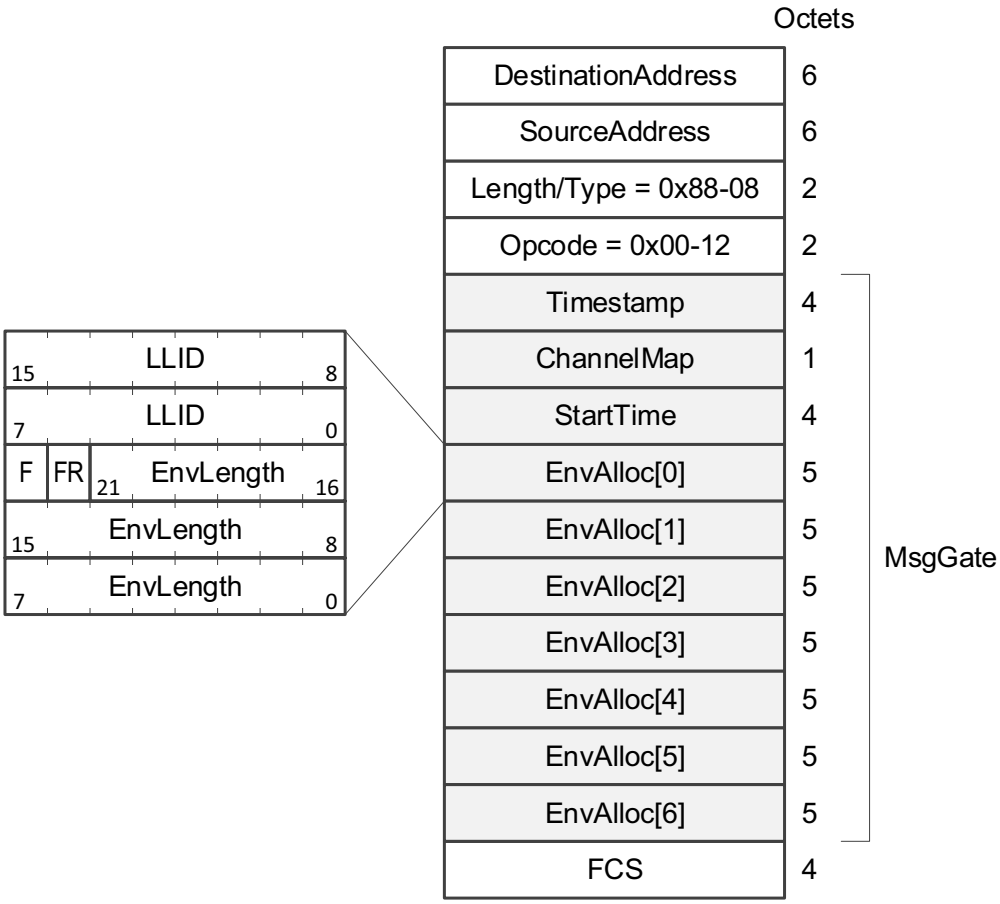

Figure 144–12—GATE MPCPDU

The GATE MPCPDU is identified by the Opcode field value of 0x00-12. The MsgGate structure represents a set of opcode-specific fields, defined as follows:

— Timestamp:
This field conveys the content of the OLT's MPCP local time counter (see LocalTime counter in 144.2.1.2) compensated for the RTT of the PLID to which the GATE MPCPDU is sent. This field is used for MPCP time synchronization (see 144.3.1.1). This field carries a 32-bit unsigned integer value that represents time in the units of EQT.

— ChannelMap:
This 8-bit field identifies the upstream channel(s) granted to the ONU in a given GATE MPCPDU. Table 144–2 shows the mapping between individual bits and upstream channels. When multiple channels are allowed in a single GATE MPCPDU, the transmission on each channel shall start at the ONU's local time equal to the StartTime value and have the length as necessary to transmit all allocated envelopes (the sum of all EnvLength fields) together with the associated optical and FEC overhead.

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Table 144–2—ChannelMap bit assignment

Bit	Channel field	Values
0	Upstream channel 0	0 – do not use upstream channel 0 for transmission 1 – use upstream channel 0 for transmission
1	Upstream channel 1	0 – do not use upstream channel 1 for transmission 1 – use upstream channel 1 for transmission
7:2	Reserved	set to 0

— StartTime:
This 32-bit unsigned integer value represents the start time of the transmission window (burst), expressed in the units of EQT. The start time is compared to the LocalTime to correlate the start of the grant.

— EnvAlloc:
This is a 40-bit structure that describes the transmission window assigned to a specific LLID. Up to seven EnvAlloc elements can be carried by a single GATE MPCPDU. The EnvAlloc structure consists of the following sub-fields:

  — LLID:
  This 16-bit unsigned integer value represents the logical link that is being allocated a transmission slot. When this field is set to the value of ESC_LLID (see Table 144–1) then it signifies an empty EnvAlloc structure.

  — EnvLength:
  This 22-bit unsigned value represents the length of the envelope assigned to this specific LLID. The length of the envelope is expressed in units of EQ. The EnvLength represents the number of EQs to be sourced from a corresponding (virtual) MAC, less one EQ reserved for the ESH. The EnvLength does not include any transmission overhead components (FEC overhead or optical burst-mode overhead).

  — Fragmentation (F):
  When set to 1, this flag informs the ONU that it is allowed to fragment new frames transmitted on the given LLID. When this flag set to 0, the ONU shall not fragment new frames. If a frame fragment remains queued in this LLID since the previous envelope transmission, this old fragment is transmitted first, regardless of the value of the Fragmentation flag. The ONU shall not fragment MPCPDU frames, regardless of the value of the Fragmentation flag in the EnvAlloc structure that allocates a PLID envelope.

  — ForceReport (FR):
  When this flag is set to 1, the ONU shall report the total length of the frames (including IPG and preamble), queued for transmission on this specific LLID. When the respective bit is set to 0, the ONU is not required to report the length of the given queue.

144.3.6.2 REPORT description

The purpose of the REPORT message is to report to the OLT the amount of data queued per individual LLID in an ONU. Up to seven LLIDs can be reported by a single REPORT MPCPDU. REPORT MPCPDUs also carry the Timestamp field. The value of this field is used by the OLT to check for the timestamp drift error (see 144.3.1.1).

The REPORT MPCPDU is an instantiation of the Generic MPCPDU and shall be as shown in Figure 144–13.

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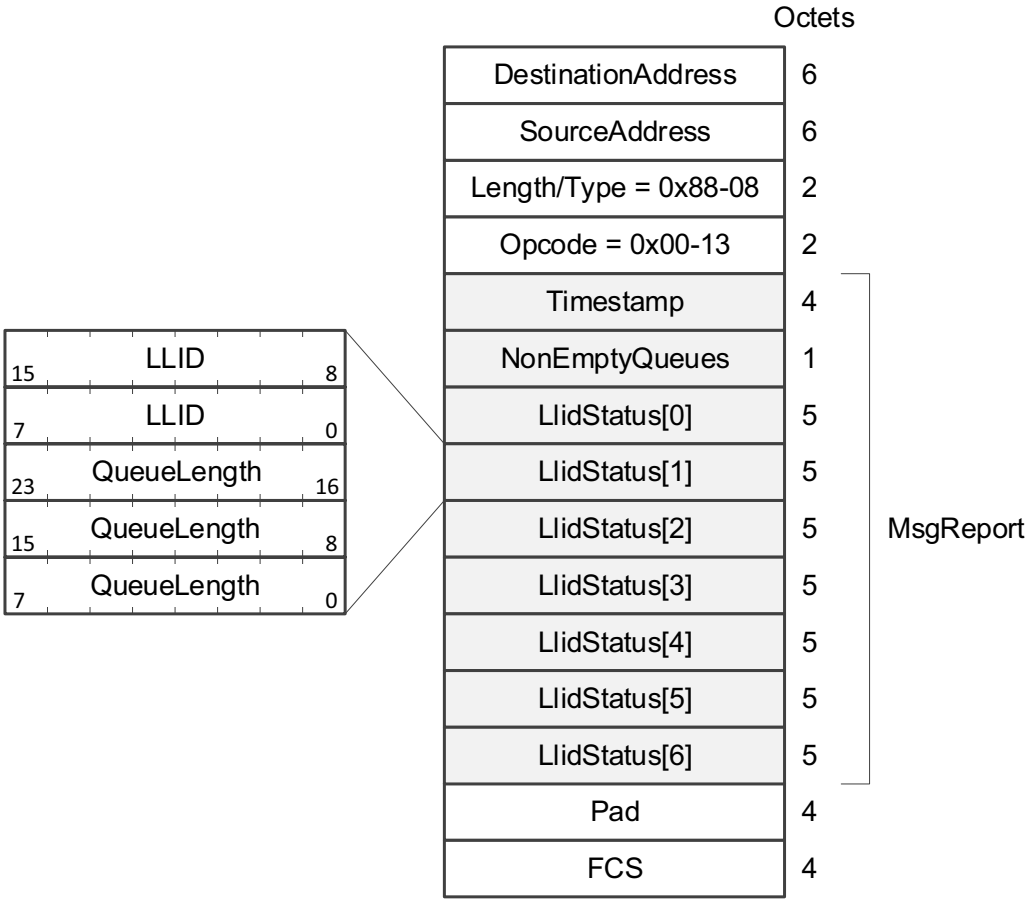

Figure 144–13—REPORT MPCPDU

The REPORT MPCPDU is identified by the Opcode field value of 0x00-13. The MsgReport structure represents a set of opcode-specific fields, defined as follows:

— Timestamp:
This field conveys the content of the ONU's MPCP local time counter (see LocalTime counter in 144.2.1.2) used for MPCP time synchronization (see 144.3.1.1). This field carries a 32-bit unsigned integer value that represents time in the units of EQT.

— NonEmptyQueues:
The number of LLIDs in the ONU with queues that were non-empty at the time of the REPORT MPCPDU transmission.

— LlidStatus:
This is a 40-bit structure that describes the occupancy of the queue assigned to a specific LLID. The occupancy reports for up to seven queues may be included into a single REPORT MPCPDU. The LlidStatus structure consists of the following sub-fields:

  — LLID:
  This 16-bit unsigned integer value represents the logical link that is being reported. When this

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field is set to the value of ESC_LLID (see Table 144–1) then it signifies an empty LlidStatus structure.

— QueueLength:
This 24-bit value represents the length of the queue assigned to the given logical link (as indicated by the value of LLID sub-field), including the associated framing overhead (IPG and preamble). The QueueLength value is expressed in the units of EQ.

144.3.6.3 REGISTER_REQ description

The purpose of the REGISTER_REQ message is to inform the OLT of an ONU's attempt to register or unregister. When multiple ONUs attempt registration, the REGISTER_REQ MPCPDUs are transmitted in the shared discovery window and may collide. The REGISTER_REQ MPCPDUs are transmitted in envelopes with the LLID equal to DISC_PLID (see 144.3.3). The REGISTER_REQ MPCPDUs carry the Timestamp field. The value of this field is used by the OLT to measure the round-trip time of that ONU (see 144.3.1.1).

The REGISTER_REQ MPCPDU is an instantiation of the Generic MPCPDU and shall be as shown in Figure 144–14.

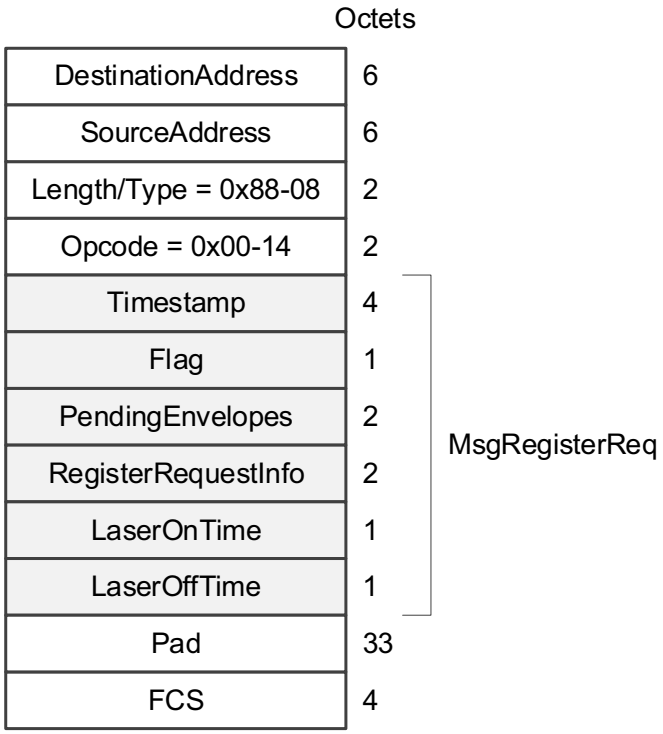

Figure 144–14—REGISTER_REQ MPCPDU

The REGISTER_REQ MPCPDU is identified by the Opcode field value of 0x00-14. The MsgRegisterReq structure represents a set of opcode-specific fields, defined as follows:

— Timestamp:
This field conveys the content of the ONU's MPCP local time counter (see LocalTime counter in 144.2.1.2) used for MPCP time synchronization (see 144.3.1.1). This field carries a 32-bit unsigned integer value that represents time in the units of EQT.

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— Flag:
This is an 8-bit field that indicates special requirements for the registration, as presented in Table 144–3.

Table 144–3—REGISTER_REQ MPCPDU Flag field

Value	Indication	Comment
0	ACK	ONU is requesting registration by the OLT
1	NACK	ONU is requesting deregistration by the OLT
2 to 255	Reserved	Ignored on reception

— PendingEnvelopes:
This is an unsigned 16-bit value signifying the maximum number of envelope allocations the ONU is capable of buffering. The OLT should not grant the ONU more than this maximum number of envelope allocations into the future.

— RegisterRequestInfo:
This is a 16-bit flag register that informs the OLT about the ONU's supported transmission rate on the channel on which this MPCPDU is transmitted. Table 144–4 presents the structure of the RegisterRequestInfo field.

Table 144–4—RegisterRequestInfo field

Bit	Flag field	Values
0	Reserved	Ignored on reception
1	ONU is 10G upstream capable	0 – ONU transmitter is not capable of 10 Gb/s 1 – ONU transmitter is capable of 10 Gb/s
2	ONU is 25G upstream capable	0 – ONU transmitter is not capable of 25 Gb/s 1 – ONU transmitter is capable of 25 Gb/s
4:3	Reserved	Ignored on reception
5	10G registration attempt	0 – 10 Gb/s registration is not attempted 1 – 10 Gb/s registration is attempted
6	25G registration attempt	0 – 25 Gb/s registration is not attempted 1 – 25 Gb/s registration is attempted
15:7	Reserved	Ignored on reception

— LaserOnTime:
This field is one octet long and carries the time required to turn the ONU transmitter on. The value of LaserOnTime is expressed in the units of EQT.

— LaserOffTime:
This field is one octet long and carries the time required to turn the ONU transmitter off. The value of LaserOffTime is expressed in the units of EQT.

144.3.6.4 REGISTER description

The REGISTER message is used to convey to the registering ONU the assigned PLID and MLID values. As the ONU is not yet aware of its assigned PLID value, the REGISTER MPCPDUs are transmitted in envelopes with the LLID equal to DISC_PLID (see 144.3.5); however, they use the ONU's MAC address as the REGISTER MPCPDU DestinationAddress.

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The OLT also may send the REGISTER MPCPDU to an already-registered ONU to request it to de-register or re-register. Such REQUEST MPCPDUs are sent in the envelopes with the unicast PLID assigned to the given ONU.

The REGISTER MPCPDU is an instantiation of the Generic MPCPDU and shall be as shown in Figure 144–15.

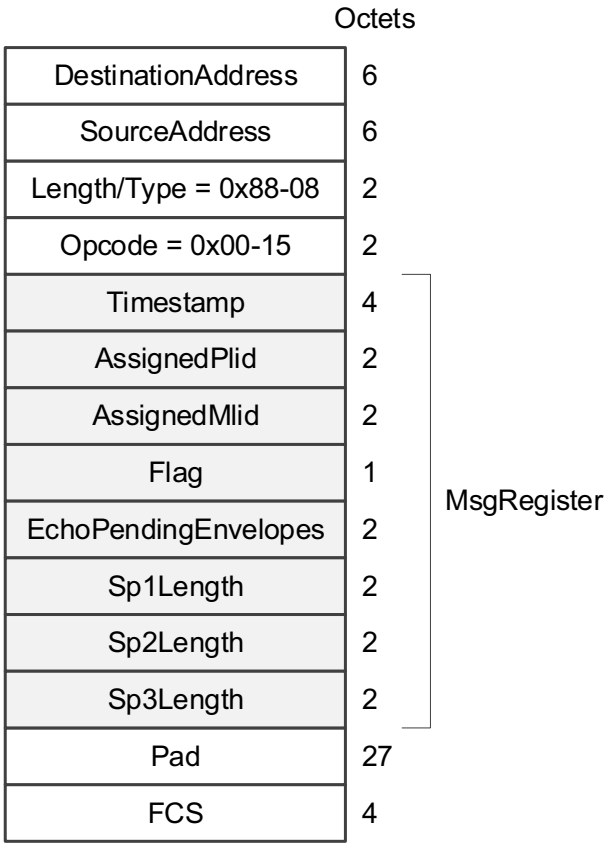

Figure 144–15—REGISTER MPCPDU

The REGISTER MPCPDU is identified by the Opcode field value of 0x00-15. The MsgRegister structure represents a set of opcode-specific fields, defined as follows:

— Timestamp:
This field conveys the content of the OLT's MPCP local time counter (see LocalTime counter in 144.2.1.2) used for MPCP time synchronization (see 144.3.1.1). This field carries a 32-bit unsigned integer value that represents time in the units of EQT.

— AssignedPlid:
This field holds a 16-bit unsigned value reflecting the PLID (see 144.3.4.1) assigned to the ONU during the registration.

— AssignedMlid:
This field holds a 16-bit unsigned value reflecting the MLID (see 144.3.4.2) assigned to the ONU during the registration.

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— Flag:
This is an 8-bit flag register that indicates special requirements for the registration, as presented in Table 144–5.

Table 144–5—REGISTER MPCPDU Flag field

Value	Indication	Comment
0	ACK	The ONU's requested registration is successful or a registered ONU is asked to re-register
1	NACK	The registration request is denied or a registered ONU is asked to deregister
2 to 255	Reserved	Ignored on reception

— EchoPendingEnvelopes:
This is an unsigned 16-bit value holding the number of envelope descriptors the ONU is able to buffer for a future activation. This is a confirmation of the PendingEnvelopes value received in the REGISTER_REQ MPCPDU.

— SP1Length:
This is a 16-bit field indicating the number of times SP1 is to be repeated at the beginning of a burst (see 142.1.3).

— SP2Length:
This is a 16-bit field indicating the number of times SP2 is to be repeated at the beginning of a burst (see 142.1.3).

— SP3Length:
This is a 16-bit field indicating the number of times SP3 is to be repeated at the beginning of a burst (see 142.1.3).

144.3.6.5 REGISTER_ACK description

The REGISTER_ACK message is transmitted by the ONU to acknowledge the completion of the Registration process. This is the first MPCPDU that the ONU transmits on its unique assigned PLID.

The REGISTER_ACK MPCPDU is an instantiation of the Generic MPCPDU and shall be as shown in Figure 144–16.

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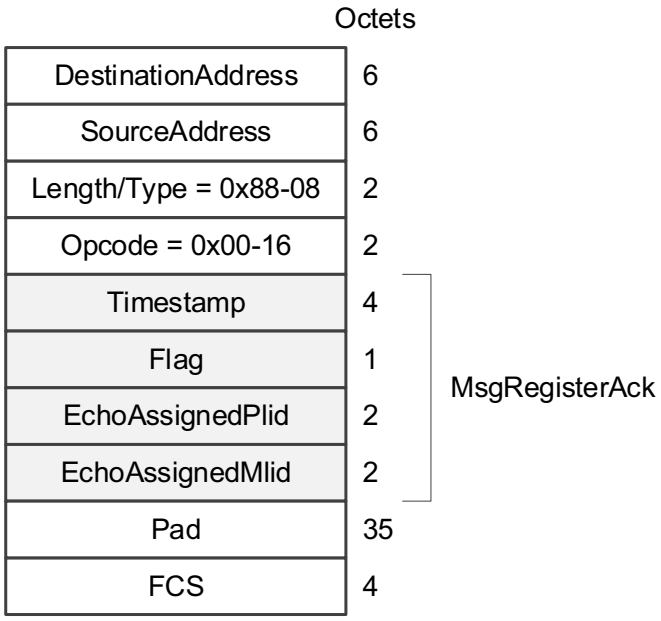

Figure 144–16—REGISTER_ACK MPCPDU

The REGISTER_ACK MPCPDU is identified by the Opcode field value of 0x00-16. The MsgRegisterAck structure represents a set of opcode-specific fields, defined as follows:

— Timestamp:
This field conveys the content of the ONU's MPCP local time counter (see LocalTime counter in 144.2.1.2) used for MPCP time synchronization (see 144.3.1.1). This field carries a 32-bit unsigned integer value that represents time in the units of EQT.

— Flag:
This is an 8-bit flag register that indicates special requirements for the registration, as presented in Table 144–6.

Table 144–6—REGISTER_ACK MPCPDU Flag field

Value	Indication	Comment
0	ACK	The Registration process is successfully acknowledged
1	NACK	The requested registration attempt is denied by the MPMC client
2 to 255	Reserved	Ignored on reception

— EchoAssignedPlid:
This field holds a 16-bit unsigned value of the PLID (see 144.3.4.1) assigned to the ONU in the process of registration (see 144.3.4.1).

— EchoAssignedMlid:
This field holds a 16-bit unsigned value of the MLID (see 144.3.4.1) assigned to the ONU in the process of registration (see 144.3.4.1).

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144.3.6.6 DISCOVERY description

The DISCOVERY message is used by the OLT to announce a discovery grant to all unregistered ONUs. The DISCOVERY MPCPDUs are transmitted in envelopes with the LLID equal to DISC_PLID (see 144.3.5). All registered ONUs ignore the DISC_PLID, and therefore do not respond to the DISCOVERY MPCPDUs.

The DISCOVERY MPCPDU is an instantiation of the Generic MPCPDU and shall be as shown in Figure 144–17.

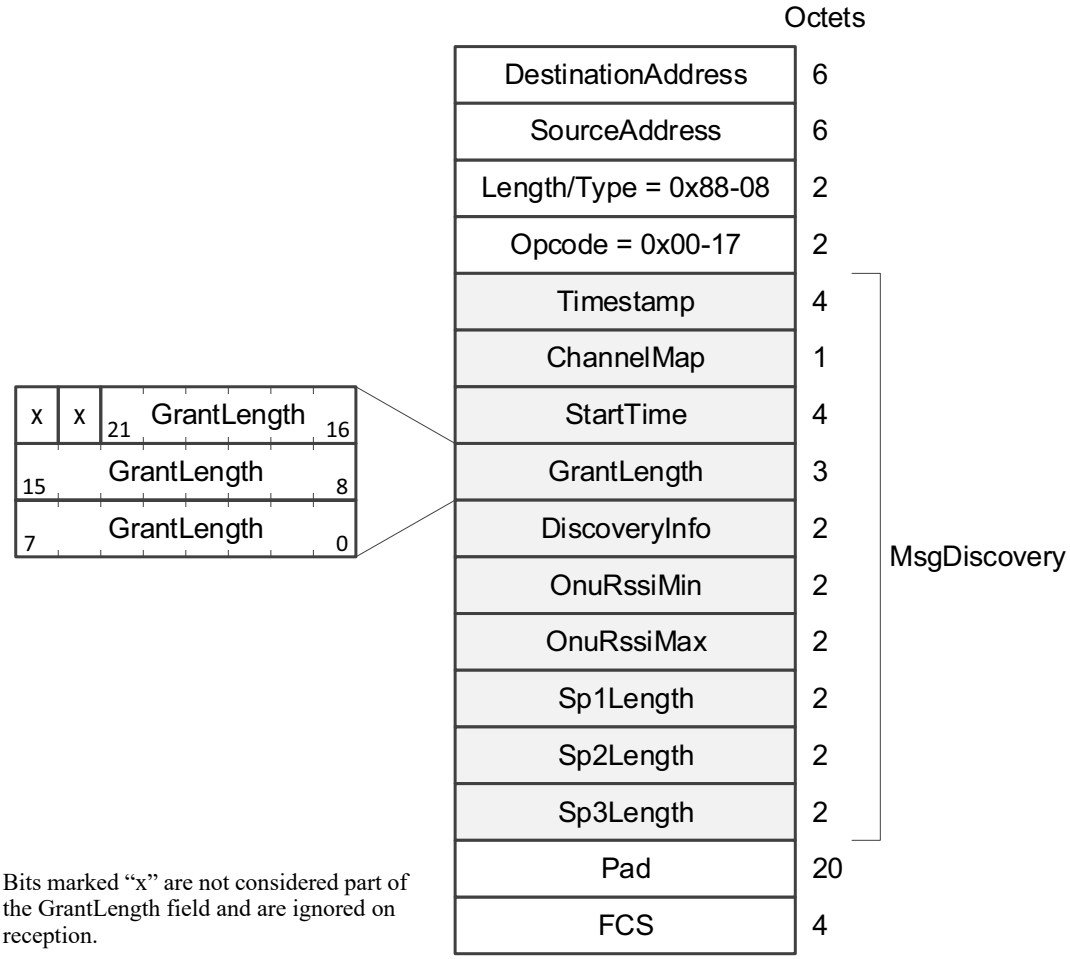

Figure 144–17—DISCOVERY MPCPDU

The DISCOVERY MPCPDU is identified by the Opcode field value of 0x00-17. The MsgDiscovery structure represents a set of opcode-specific fields, defined as follows:

— Timestamp:
This field conveys the content of the OLT's MPCP local time counter (see LocalTime counter in 144.2.1.2) used for MPCP time synchronization (see 144.3.1.1). This field carries a 32-bit unsigned integer value that represents time in the units of EQT.

— ChannelMap:
This 8-bit field identifies the upstream channel(s) granted to the ONU in a given DISCOVERY MPCPDU. Table 144–2 shows the mapping between individual bits and upstream channels. When

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multiple channels are allowed in a single DISCOVERY MPCPDU, an unregistered ONU shall attempt to register on a single channel only. The choice of the channel is implementation-specific.

— StartTime:
This 32-bit unsigned integer value represents the start time of the discovery window (burst), expressed in the units of EQT. The start time is compared to LocalTime, to correlate the start of the grant. The ONU's burst typically does not start at the advertised discovery grant StartTime, but is delayed by a random time interval to avoid persistent collisions of REGISTER_REQ messages from multiple unregistered ONUs (see 144.3.7).

— GrantLength:
This 22-bit unsigned value represents the length of the discovery grant expressed in the units of EQ. The GrantLength does not include any transmission overhead components (FEC overhead or optical burst-mode overhead).

— DiscoveryInfo:
This is a 16-bit flag register. Table 144–7 presents the internal structure of the DiscoveryInfo field.

Table 144–7—DiscoveryInfo field

Bit	Flag field	Values
0	Reserved	Ignored on reception
1	OLT is 10G upstream capable	0 – OLT does not support 10 Gb/s reception 1 – OLT supports 10 Gb/s reception
2	OLT is 25G upstream capable	0 – OLT does not support 25 Gb/s reception 1 – OLT supports 25 Gb/s reception
4:3	Reserved	Ignored on reception
5	OLT is opening 10G discovery window	0 – OLT is not capable of receiving 10 Gb/s data in this window 1 – OLT is capable of receiving 10 Gb/s data in this window
6	OLT is opening 25G discovery window	0 – OLT is not capable of receiving 25 Gb/s data in this window 1 – OLT is capable of receiving 25 Gb/s data in this window
13:7	Reserved	Ignored on reception
14	Coexistence class G	0 – ONUs supporting PMDs coexistence class G are not allowed to register 1 – ONUs supporting PMDs coexistence class G are allowed to register
15	Coexistence class X	0 – ONUs supporting PMDs coexistence class X are not allowed to register 1 – ONUs supporting PMDs coexistence class X are allowed to register

The flags in the DiscoveryInfo field allow the OLT to exercise discovery admission control over the unregistered ONUs. Specifically, the following ONU behavior is defined:

— The ONU shall not generate/transmit a REGISTER_REQ MPCPDU using the 10 Gb/s upstream channel if the OLT did not open the 10 Gb/s discovery window, i.e., if bit 5 was set to 0.

— The ONU shall not generate/transmit a REGISTER_REQ MPCPDU using the 25 Gb/s upstream channel if the OLT did not open the 25 Gb/s discovery window, i.e., if bit 6 was set to 0.

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— An ONU supporting PMD coexistence class G (see 141.2.3 and Table 141–7) shall not generate/transmit a REGISTER_REQ MPCPDU if the OLT does not allow the G-type coexistence, i.e., if bit 14 was set to 0.

— An ONU supporting PMD coexistence class X (see 141.2.3 and Table 141–7) shall not generate/transmit a REGISTER_REQ MPCPDU if the OLT does not allow the X-type coexistence, i.e., if bit 15 was set to 0.

The values of the DiscoveryInfo field flags are set by the OLT MPMC client and may change from one discovery attempt to the next. The OLT MPMC client may allow a concurrent registration of ONUs with different rates by setting both bits 5 and 6 to 1. The processing of DiscoveryInfo flags by the ONU and the ONU behavior in dual-rate systems is further specified in 144.3.9. The OLT MPMC client may also allow a concurrent registration of ONUs with different coexistence options by setting both bits 14 and 15 to 1. For ONUs that support both coexistence types, the choice of which type to attempt to register is implementation-dependent.

— OnuRssiMin:
This is a 16-bit unsigned integer field, representing the minimum received signal strength indicator (RSSI) threshold for the given discovery attempt. Only the ONUs with measured RSSI greater or equal to OnuRssiMin shall generate a REGISTER_REQ message in the given discovery window. The unit of OnuRssiMin value is 0.1 μW, allowing the entire field to cover the range of 0 to 6.5535 mW (~ –40 dBm to +8.2 dBm).

— OnuRssiMax:
This is a 16-bit unsigned integer field, representing the maximum RSSI threshold for the given discovery attempt. Only the ONUs with measured RSSI lower or equal to OnuRssiMax shall generate a REGISTER_REQ message in the given discovery window. The unit of OnuRssiMax value is 0.1 μW, allowing the entire field to cover the range of 0 to 6.5535 mW (~ –40 dBm to +8.2 dBm).

— SP1Length:
This is a 16-bit unsigned integer field indicating the number of times SP1 is to be repeated at the beginning of a burst carrying the REGISTER_REQ MPCPDU (see 142.1.3).

— SP2Length:
This is a 16-bit unsigned integer field indicating the number of times SP2 is to be repeated at the beginning of a burst carrying the REGISTER_REQ MPCPDU (see 142.1.3).

— SP3Length:
This is a 16-bit unsigned integer field indicating the number of times SP3 is to be repeated at the beginning of a burst carrying the REGISTER_REQ MPCPDU (see 142.1.3).

144.3.6.7 SYNC_PATTERN description

The SYNC_PATTERN message is transmitted by the OLT to announce a synchronization pattern (257-bit sequence) to be used by ONUs at the beginning of each upstream burst (i.e., as a burst preamble). The OLT announces three distinct patterns to be used at the beginning of every burst (see 142.1.3). An unregistered ONU does not respond to a DISCOVERY message if it did not receive all three SYNC_PATTERN MPCPDUs before it received the DISCOVERY MPCPDU. As part of the Discovery process, the SYNC_PATTERN MPCPDUs are transmitted in envelopes with the LLID equal to DISC_PLID (see 144.3.5) to allow unregistered ONUs to obtain the synchronization pattern. An ONU that received three synchronization patterns and subsequently registered with the OLT, continues to use the same synchronization patterns after the registration.

The SYNC_PATTERN MPCPDU is an instantiation of the Generic MPCPDU and shall be as shown in Figure 144–18.

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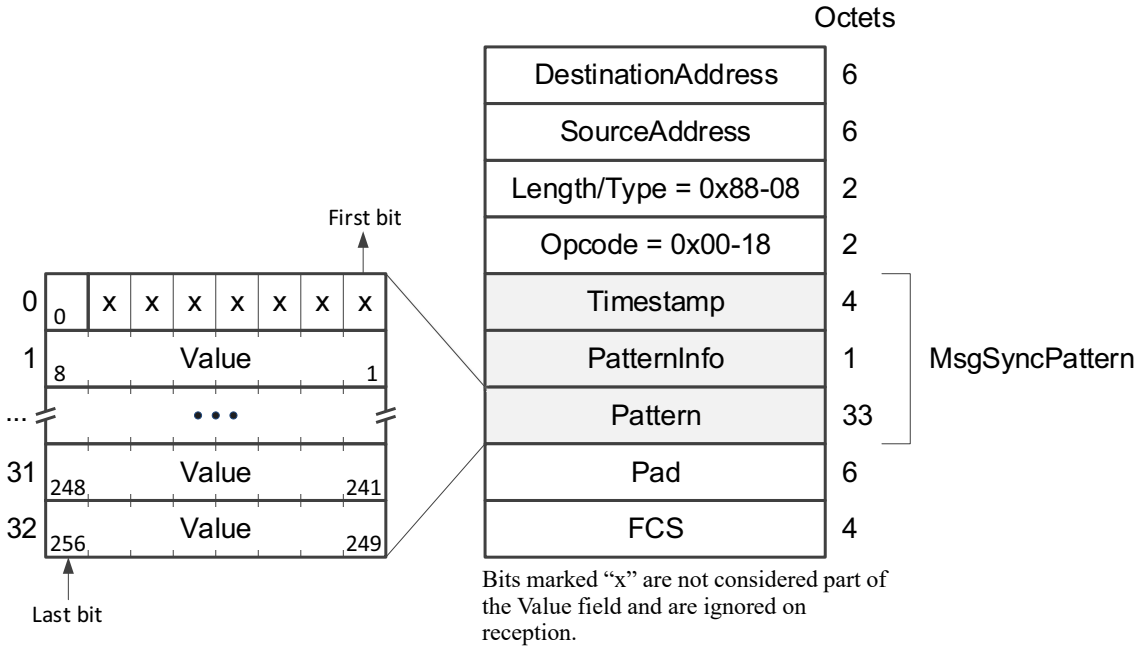

Figure 144–18—SYNC_PATTERN MPCPDU

The SYNC_PATTERN MPCPDU is identified by the Opcode field value of 0x00-18. The MsgSyncPattern structure represents a set of opcode-specific fields, defined as follows:

— Timestamp:
This field conveys the content of the OLT's MPCP local time counter (see LocalTime counter in 144.2.1.2) used for MPCP time synchronization (see 144.3.1.1). This field carries a 32-bit unsigned integer value that represents time in the units of EQT.

— PatternInfo:
This is an 8-bit field, with individual bits defined per Table 144–8.

Table 144–8—PatternInfo field value

Bit(s)	Field Name	Meaning
1:0	Index	Indicates the index of the synchronization pattern element being configured by the OLT. Valid values for index are 0, 1, or 2.
6:2	Reserved	Ignored on reception
7	Balanced	Indicates whether the given synchronization pattern element is to be balanced or not: 0 – synchronization pattern is to remain unbalanced, i.e., synchronization pattern value is repeated unchanged 1 – synchronization pattern is to be balanced, i.e., each 257-bit block of synchronization pattern element (starting with the second block) is an inversion of its preceding block

— Pattern:
This is a 33-octet field, containing a 257-bit synchronization pattern element (sub-field Value). The ONU transmits the corresponding burst synchronization pattern matching the exact bit sequence that it received in the Value sub-field.

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144.3.7 Discovery process

Discovery is the process whereby newly connected or unregistered ONUs are provided access to the PON. The process is driven by the OLT, which periodically makes available discovery windows during which unregistered ONUs are given the opportunity to make themselves known to the OLT. The periodicity of these windows is unspecified.

The Discovery process begins with the announcement of the MsgSyncPattern structure using the SYNC_PATTERN MPCPDU exchange between the OLT and the ONU. Three separate SYNC_PATTERN MPCPDUs are sent by the OLT, announcing the value of SP1, SP2, and SP3 portions of the FEC unprotected area in the head of the upstream burst (see 142.1.3). Repeat counts for SP1, SP2, and SP3 during the discovery window are announced within the DISCOVERY MPCPDU. Repeat counts for SP1, SP2, and SP3 outside of the discovery window (normal granting operation) are announced within the REGISTER MPCPDU. Combined, this allows the OLT to effectively configure the synchronization pattern structure and optimize it for the specific OLT receiver implementation. If a SYNC_PATTERN MPCPDU is received prior to the transmission of a REGISTER_REQ MPCPDU of an ONU responding to a previous discovery window (see Figure 144–22) that registration is aborted and the ONU waits for a subsequent MsgSyncPattern announcement and the discovery window to register.

Upon completion of the MsgSyncPattern announcement, the OLT signals that a discovery period is occurring by broadcasting a DISCOVERY MPCPDU, which includes the starting time and length of the discovery window, along with the DiscoveryInfo field, as defined in 144.3.6.6. With the appropriate settings of individual flags contained in this 16-bit wide field, the OLT notifies all the ONUs about its upstream and downstream channel transmission capabilities. Note that the OLT may simultaneously support more than one data rate in the given transmission direction.

Unregistered ONUs, upon receiving a DISCOVERY MPCPDU, wait for the period to begin and then transmit a REGISTER_REQ MPCPDU to the OLT. Discovery windows are unique in that they are the only times when multiple ONUs are allowed to access the same upstream channel simultaneously, and transmission overlap may occur. In order to reduce transmission overlaps, a contention algorithm is used by all ONUs. Measures are taken to reduce the probability for overlaps by artificially simulating a random distribution of distances from the OLT. Each ONU waits a random amount of time before transmitting the REGISTER_REQ MPCPDU. The wait time together with the REGISTER_REQ MPCPDU transmission time (including optical overhead, burst synchronization sequence, and FEC parity data) does not exceed the length of the discovery window. Note that multiple valid REGISTER_REQ MPCPDUs may be received by the OLT during a single discovery window. Included in the REGISTER_REQ MPCPDU is the ONU's MAC address and number of maximum pending envelopes. Additionally, a registering ONU notifies the OLT of its transmission capabilities in the current upstream channel by setting appropriately the flags in the RegisterRequestInfo field, as specified in 144.3.6.3.

Note that even though a compliant ONU may be capable of supporting more than one data rate in any transmission channel, it is expected that an ONU only attempts to register at a single rate as indicated in the RegisterRequestInfo field bits 5 and 6. Moreover, in order to improve the upstream channel utilization and to decrease the required size of the guard band between individual data bursts, the registering ONU notifies the OLT of the laser on/off times, by setting appropriate values in the LaserOnTime and LaserOffTime fields.

Upon receipt of a valid REGISTER_REQ MPCPDU, the OLT registers the ONU, allocating and assigning two new port identities (PLID and MLID), and binding them to corresponding MACs in the OLT.

The next step in the process is for the OLT to transmit a REGISTER MPCPDU containing the PLID and MLID to the newly discovered ONU. The REGISTER MPCPDU also contains the OLT's required synchronization time. Moreover, the OLT echoes the maximum number of pending envelopes.

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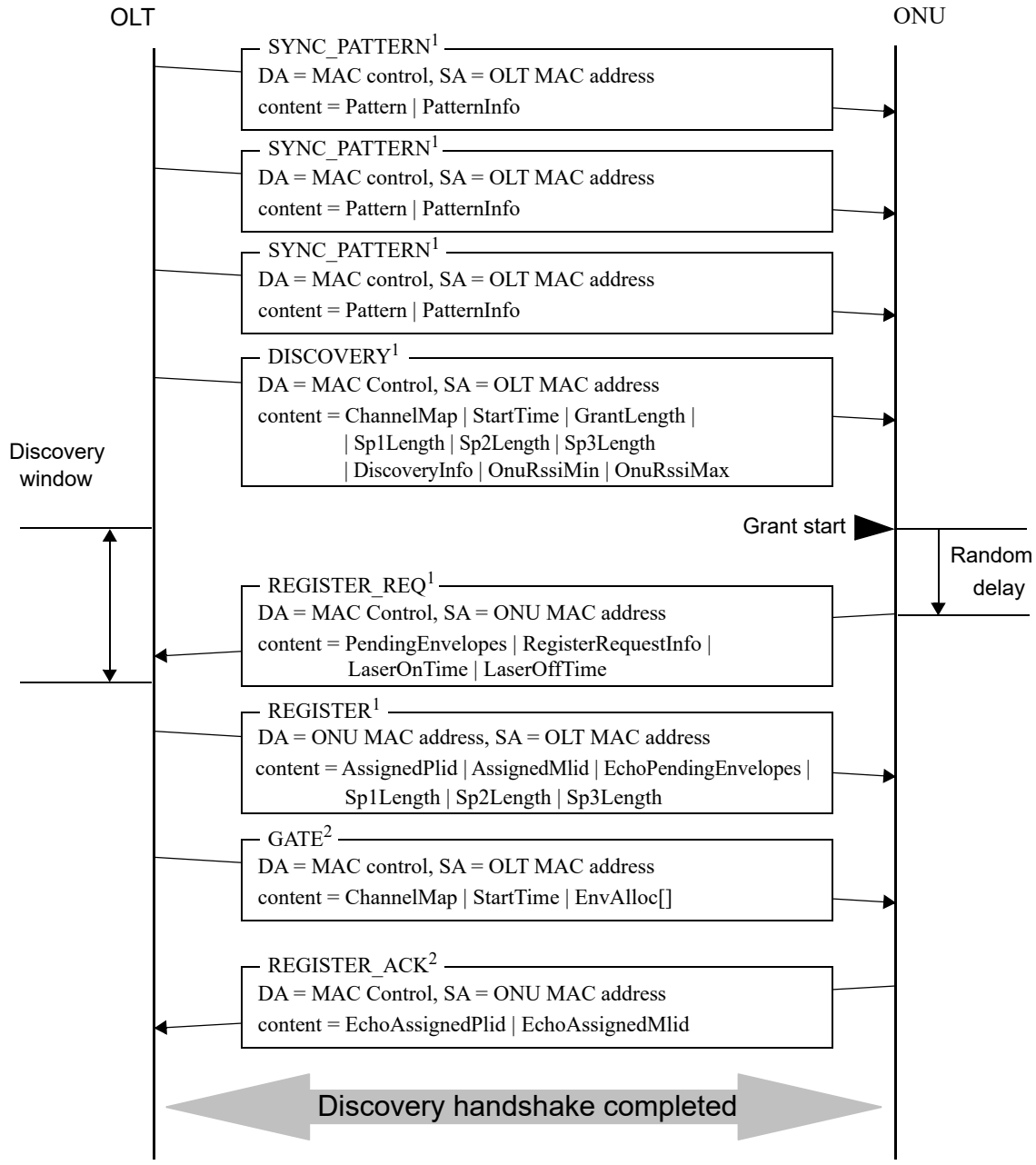
After processing the REGISTER_REQ MPCPDU received from a given ONU, the OLT has enough information to schedule that ONU for access to the PON. The OLT transmits a GATE MPCPDU allowing the ONU to transmit a REGISTER_ACK MPCPDU. Upon receipt of the REGISTER_ACK MPCPDU, the Discovery process for that ONU is complete, the ONU is registered and normal message traffic may begin. It is the responsibility of Layer Management to perform the MAC binding, and start transmission from/to the newly registered ONU. The discovery message exchange is illustrated in Figure 144–19.



[1] Messages sent on discovery PLID (DISC_PLID)
[2] Messages sent on unicast PLID

Figure 144–19—Discovery handshake message exchange

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There may exist situations when the OLT requires an ONU to re-register. The OLT initiates such reregistration by transmitting a REGISTER MPCPDU to the ONU. This MPCPDU is transmitted in an envelope with unicast PLID assigned to this ONU.

If the Flag field in the REGISTER MPCPDU has the value of ACK, the ONU performs a fast registration sequence where it simply responds with the REGISTER_ACK MPCPDU, while remaining registered at all times. If the Flag field in the REGISTER MPCPDU has the value of NACK, the ONU deregisters and goes through a complete discovery sequence, as outlined above.

There may also be situations when the MPMC client (MPCP) in the ONU determines that this ONU needs to deregister. The ONU transmits a REGISTER_REQ MPCPDU with the Flag field equal to NACK before unconditionally deregistering itself. Depending on the causes for such a deregistration, the MPMC client (MPCP) determines whether the ONU is allowed to participate in a new discovery sequence or not; the criteria for such a determination is outside the scope of this standard.

144.3.7.1 Constants

ACK_GATE_LIMIT
Type: Integer
Description: The maximum number of GATE MPCPDUs that the OLT issues to a registering ONU to provide an opportunity for REGISTER_ACK MPCPDU transmission.
Value: 8

DISCOVERY_MARGIN
Type: Integer
Description: This constant holds the extra margin reserved at the end of a discovery grant to accommodate the largest possible round-trip time on a given ODN. The round-trip time also includes any internal delays in the OLT and ONU, such as FEC encoding and decoding delays.
Value: 80 078 (205 μs for ODN with 20 km reach)
Unit: EQT

MISSED_REPORT_LIMIT
Type: Integer
Description: This constant represents the number of missed REPORT MPCPDUs that cause the OLT to deregister the given ONU.
Value: 8

REQ_LENGTH
Type: Integer
Description: This constant holds the envelope length sufficient to carry a single REGISTER_REQ MPCPDU.
Value: 10
Unit: EQT

SP_COUNT
Type: Integer
Description: The number of synchronization patterns used at the beginning of each burst.
Value: 3

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144.3.7.2 Counters

GateCount

Description: This counter counts the number of remaining GATE MPCPDUs to be issued to a registering ONU before the registration attempt is deemed to have failed due to a lack of acknowledgment (i.e., missing REGISTER_ACK MPCPDU).

LocalTime

See 144.2.1.2

144.3.7.3 Variables

BEGIN

See 142.2.5.2

ChState

Type: Array of eight Boolean values

Description: The value of this variable represents a binary-encoded status of upstream channels at the ONU. Bit 0 corresponds to channel 0 and bit 1 corresponds to channel 1. Bits 2 through 7 are set to 0. The value of each bit has the following meaning:

1 = channel is enabled

0 = channel is disabled

DeregistrationTrigger

Type: Boolean

Description: This variable is set to true when at least one of multiple conditions for ONU deregistration becomes true. Otherwise, the variable is set to false. The DeregistrationTrigger is an alias for the following code:

```
DeregistrationTrigger =
   // 1) ONU MPCP is unresponsive
   MissedReportCount == MISSED_REPORT_LIMIT OR

   // 2) Timestamp drift exceeded the safe margin
   TimestampDrift == true OR

   // 3) ONU requested deregistration
   ( MCII(MsgRegisterReq) AND MsgRegisterReq.Flag == NACK )
```

GrantEndTime

Type: 32-bit unsigned integer

Description: This variable holds the time at which the ONU grant ends. Failure of a REGISTER_ACK message from an ONU to arrive at the OLT before GrantEndTime for more than ACK_GATE_LIMIT times is a fatal error in the Discovery process, and causes registration to fail for the specified ONU.

Unit: EQT

GrantMargin

Type: 22-bit unsigned integer

Description: This variable represents the total time required for an ONU to terminate one burst and immediately initiate another burst. The variable includes the following burst overhead components:

a) The length of end-of-burst delimiter (EBD)
b) The length of SP1 synchronization pattern (SP1Length)
c) The length of SP2 synchronization pattern (SP2Length)
d) The length of SP3 synchronization pattern (SP3Length).

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e) The FEC Parity overhead (2560 parity bits + 10 bits of FEC codeword delimiter)

All the above overhead components are represented in terms of 257-bit line coding blocks. The sum of these values S is converted into units of EQ as S × 4.

Value: GrantMargin is calculated the first time when the ONU receives DISCOVERY MPCPDU with Sp1Length, Sp2Length, and Sp3Length. Then, it is recalculated when the ONU receives REGISTER MPCPDU, which may have the same Sp1Length, Sp2Length, and Sp3Length values or different.

NOTE—If an ONU receives a grant with a StartTime within the GrantMargin from the end of the previous grant, then the ONU ignores such a grant.

MaxDelay

Type: 32-bit unsigned integer

Description: This variable indicates the maximum delay the ONU may apply to REGISTER_REQ MPCPDU transmission while remaining within the allocated discovery grant.

Unit: EQT

MissedReportCount

Type: 8-bit unsigned integer

Description: This variable counts the number of missed REPORT MPCPDUs from a given PLID. A REPORT MPCPDU is considered missing if the OLT has allocated an envelope for the PLID and has not received any REPORT MPDCPDUs in the corresponding PLID envelope. The MissedReportCount counter is incremented by one per each PLID envelope that did not contain any REPORT MPCPDUs, regardless of the length of that envelope. If a REPORT MPCPDU is received from a given PLID, the value of MissedReportCount is reset to zero.

Onu10GCapable

Type: Boolean

Description: This variable is set to true if the ONU is capable of transmitting at a line rate of 10.3125 GBd. Otherwise, it is set to false

Onu25GCapable

Type: Boolean

Description: Description: This variable is set to true if the ONU is capable of transmitting at a line rate of 25.78125 GBd. Otherwise, it is set to false.

OnuCoexType

Type: 2-bit integer

Description: This variable represents the coexistence types supported by the ONU transceiver (see 141.2.3). Bit 0 represents G-type coexistence and bit 1 represents X-type coexistence. Therefore, this variable takes the following values:

0x1: The ONU transceiver supports G-type coexistence

0x2: The ONU transceiver supports X-type coexistence

0x3: The ONU transceiver supports both G-type and X-type coexistence

OnuRssiLocal

Type: 16-bit unsigned integer

Description: This variable holds the RSSI value measured by the ONU receiver. Only the ONUs whose OnuRssiLocal value is within the RSSI limits advertised in the DISCOVERY MPCPDU are allowed to register in the given discovery window. Refer to definitions of OnuRssiMin and OnuRssiMax in 144.3.6.6.

Unit: 0.1 μW

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RegAllowed

Type: Boolean

Description: This variable is set to true if upon the verification of the various fields of the DISCOVERY MPCPDU, the ONU has determined that it is allowed to transmit a REGISTER_REQ in the current discovery window. The RegAllowed is an alias for the following code:

```
RegAllowed =

      // 1) Upstream channel is available
      ((MsgDiscovery.ChannelMap AND ChState) != 0) AND

      // 2) RSSI is within the allowed limits
      OnuRssiLocal ≥ MsgDiscovery.OnuRssiMin AND
      OnuRssiLocal ≤ MsgDiscovery.OnuRssiMax AND

      // 3) OLT and ONU support the same coexistence mode (G or X)
      ((MsgDiscovery.DiscoveryInfo[15:14] AND OnuCoexType) != 0) AND

      // 4) 25G discovery is open and ONU is 25G-capable,
      // OR (10G discovery is open and ONU is 10G-capable
      // AND the OLT and/or the ONU are not 25G-capable)
      // (see Discovery in dual-rate systems, 144.3.7)
      ((MsgDiscovery.DiscoveryInfo[6] == 1 AND Onu25GCapable) OR
      ((MsgDiscovery.DiscoveryInfo[5] == 1 AND Onu10GCapable) AND
      (MsgDiscovery.DiscoveryInfo[2] == 0 OR !Onu25GCapable)));
```

Registered

Type: Boolean

Description: This variable holds the current registration status of a PLID. It is set to true once the Discovery process is complete and registration is acknowledged.

RegStart

Type: 32-bit unsigned integer

Description: This variable indicates the local time at which the REGISTER_REQ MPCPDU is to be transmitted by the ONU. The RegStart is delayed from the discovery grant start time by a random amount to prevent persistent collisions of REGISTER_REQ MPCPDUs from multiple registering ONUs.

Unit: EQT

SpSeq

Type: 2-bit unsigned integer

Description: This variable indicates the index of the synchronization pattern announced by the OLT in the SYNC_PATTERN MPCPDU. The SpSeq variable takes values 0, 1, or 2. Details about individual synchronization pattern elements are covered in 142.1.3.

144.3.7.4 Functions

BurstLength(env_length)

This function takes the envelope length (or a total of multiple envelope lengths) and calculates the total length of the upstream burst, including the following overhead components:

a) The length of SP1 synchronization pattern (SP1Length)
b) The length of SP2 synchronization pattern (SP2Length)
c) The length of SP3 synchronization pattern (SP3Length)
d) Rounding overhead due to 256B/257B line coding

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e) The FEC Parity overhead, including the 10-bit FEC codeword delimiter
f) The length of burst terminating sequence, including the EBD and laser off time

The result is converted into EQT and is rounded up to the next integer value.

Random(min_value, max_value)

This function returns a random value uniformly distributed in the range from min_value to max_value, inclusive.

144.3.7.5 Messages

MsgBurstSync

A set of parameters (operand_list) carried in multiple SYNC_PATTERN MPCPDUs. Within the OLT Discovery Initiation process (see 144.3.7.6), the MsgBurstSync set is received from the MPMC client and is transmitted in three SYNC_PATTERN MPCPDUs. Within the ONU Registration process (see 144.3.7.8), the parameters received in multiple SYNC_PATTERN MPCPDUs are combined and passed to the MPMC client as a single MsgBurstSync set. The MsgBurstSync set includes the following parameters:

Balanced[SP_COUNT]: An array of SP_COUNT Boolean values, where the *n*th element of the array indicates whether the *n*th synchronization pattern is balanced or not.

Value[SP_COUNT]: An array of SP_COUNT 257-bit values, where the *n*th element of the array represents the *n*th synchronization pattern.

MsgDiscovery

A set of parameters (operand_list) carried in the DISCOVERY MPCPDU, as defined in 144.3.6.6.

MsgGate

A set of parameters (operand_list) carried in the GATE MPCPDU, as defined in 144.3.6.1.

MsgRegister

A set of parameters (operand_list) carried in the REGISTER MPCPDU, as defined in 144.3.6.4.

MsgRegisterAck

A set of parameters (operand_list) carried in the REGISTER_ACK MPCPDU, as defined in 144.3.6.5.

MsgRegisterReq

A set of parameters (operand_list) carried in the REGISTER_REQ MPCPDU, as defined in 144.3.6.3.

MsgSyncPattern

A set of parameters (operand_list) carried in the SYNC_PATTERN MPCPDU, as defined in 144.3.6.7.

144.3.7.6 Discovery Initiation state diagram

The OLT MPCP shall implement a single instance of the OLT Discovery Initiation process shown in Figure 144–20. This instance shall be associated with the DISC_PLID value, i.e., it only receives and generates MPCPDUs that are carried in envelopes with the DISC_PLID value.

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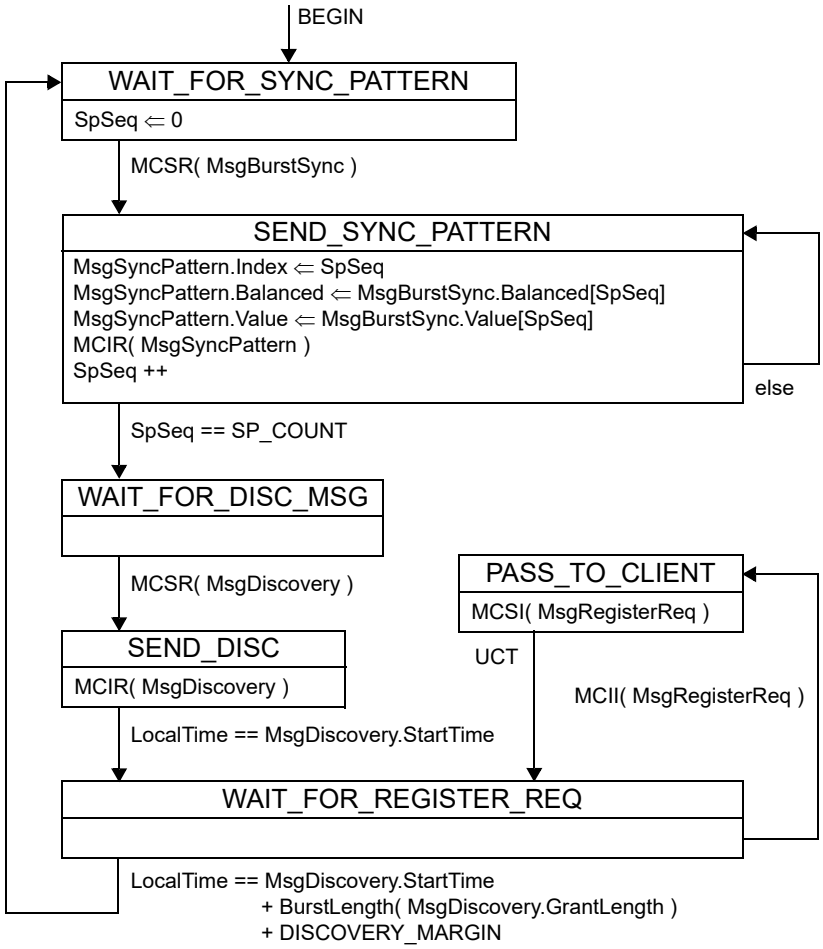

Figure 144–20—OLT Discovery Initiation state diagram

144.3.7.7 Registration Completion state diagram

The OLT MPCP shall implement multiple instances of the OLT Registration Completion state diagram shown in Figure 144–21 where each instance is associated with a unicast PLID being registered.

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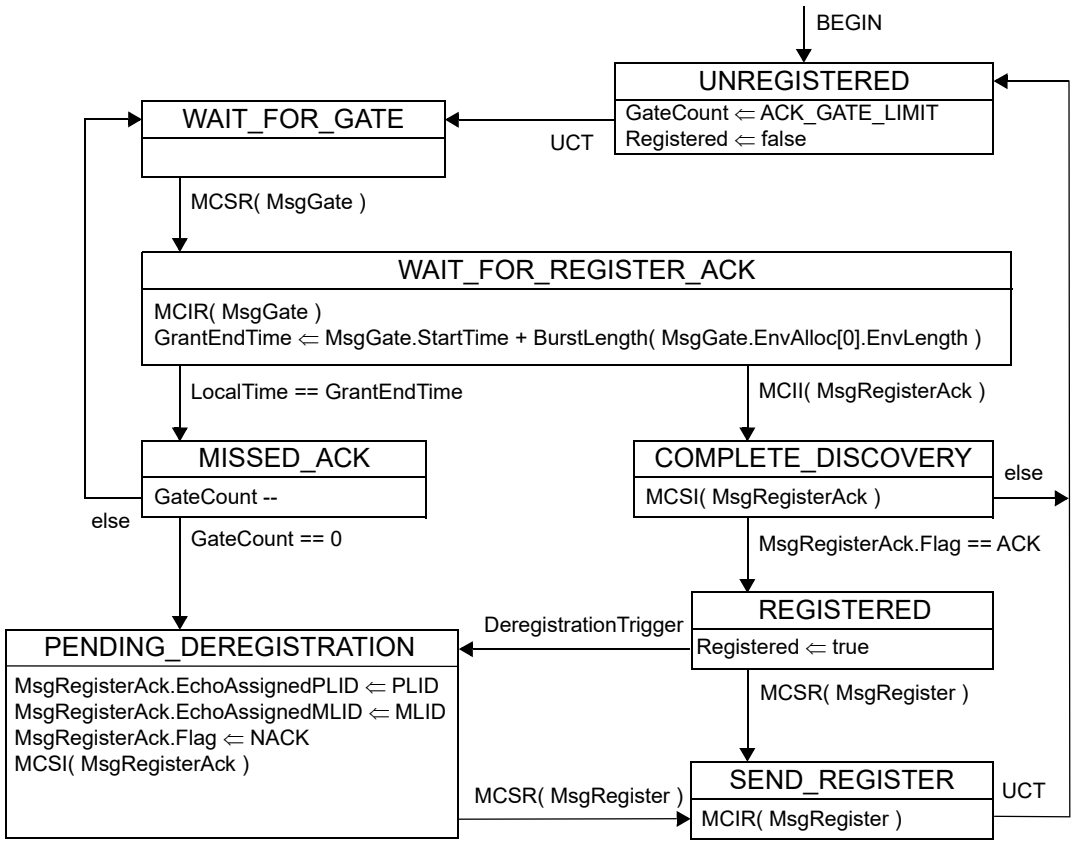

Figure 144–21—OLT Registration Completion state diagram

144.3.7.8 ONU Registration state diagram

The ONU MPCP shall implement a single instance of the ONU Registration state diagram as shown in Figure 144–22. This instance is associated with the DISC_PLID value when the Registered variable is equal to false, and it is associated with unicast PLID and BCAST_PLID values, when the Registered variable is equal to true.

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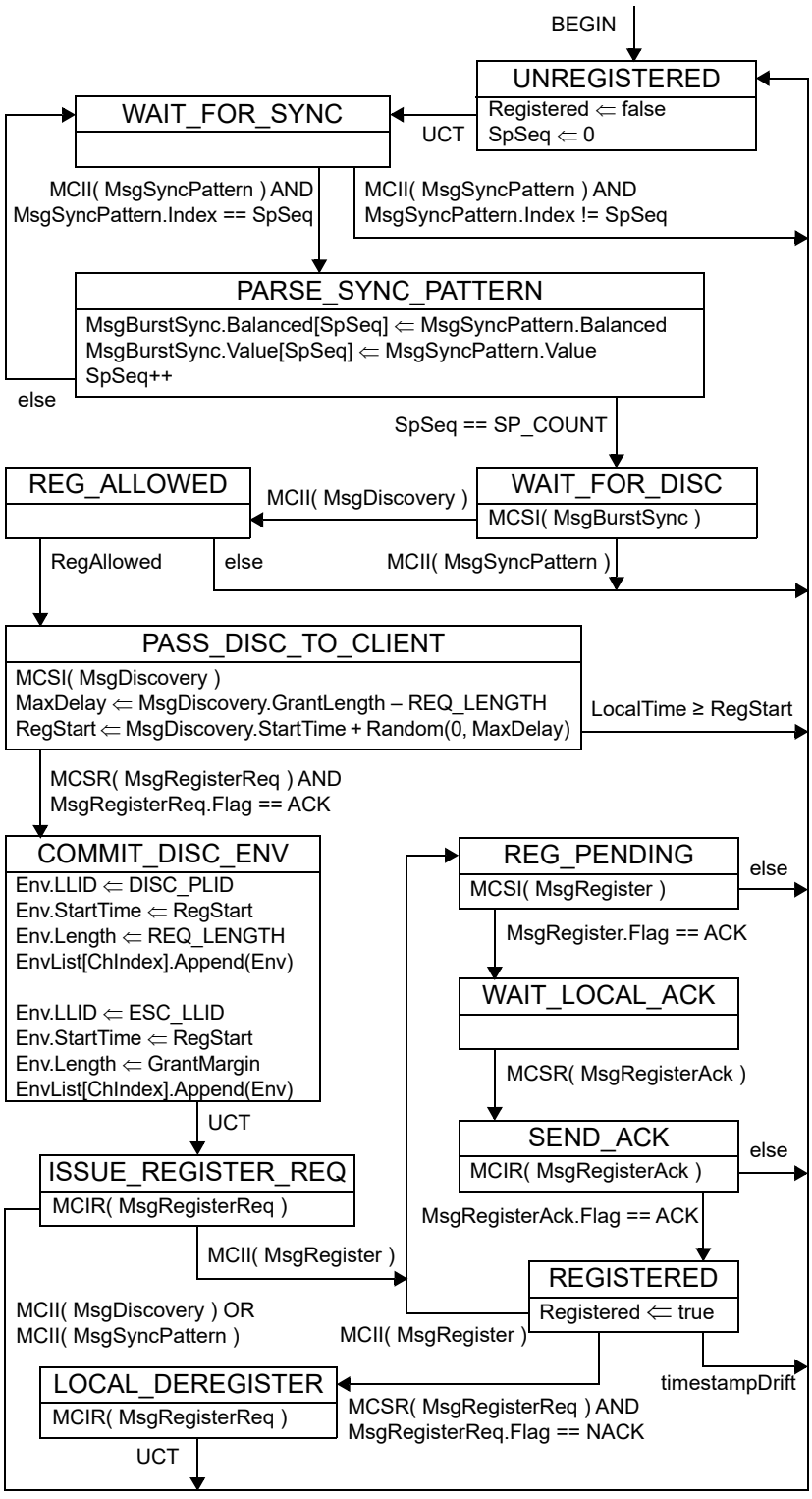

Figure 144–22—ONU Registration state diagram

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144.3.8 Granting process

As noted in 144.1.1.1, upstream transmissions in a PON network are arbitrated by the OLT. The OLT sends an ONU a grant (see 1.4.348) to allow an upstream transmission by that ONU to begin at a specific time and have a specific duration. A grant is defined by the envelope allocations in one or more GATE messages (see 144.3.6.1). Multiple envelope allocations apply to a single grant if they have the same start time and apply to the same ONU. How the OLT MPMC client determines the start time and duration of grants is out of scope for this standard, but may be based on REPORT messages (see 144.3.6.2) received from an ONU. The following description of the granting process makes use of the interfaces and functional blocks found in Figure 144–3 and Figure 144–4.

The upstream granting process begins when the OLT MPMC client defines a transmission opportunity for an ONU and compiles a GATE message using the MsgGate structure (see 144.3.6.1), which is sent to the MPMC sublayer via the MCSR interface. This generates a GATE MPCPDU using the process defined in the GATE Generation state diagram (see 144.3.8.7). The GATE MPCPDU is transmitted to an ONU.

Upon receiving the GATE message, the ONU processes the message as defined in the GATE Reception state diagram (see 144.3.8.8) and passes the included information to the MPMC client via the MCSI using the MsgGate message. The ONUs MPMC client determines when its next transmission opportunity is and generates an appropriate envelope descriptor, which may be grouped with other envelope descriptors, and is sent to the ONU's MPMC in a MsgEnvGroup message (see 144.3.8.3) over the MCSR interface. The MsgEnvGroup message is processed using the ONU Envelope Commitment state diagram (see 144.3.8.10). This results in an envelope being added to the EnvList[] (see 144.3.8.3).

The EnvList[] is processed by the ONU Envelope Commitment state diagram (see 144.3.8.10), which results in an MCRS_CTRL[*ch*].request being generated in the Envelope Activation state diagram (see 144.3.8.11) for the indicated channel or channels at the start of the next burst.

Since the OLT transmits continuously, grants are not explicitly used by the OLT in the downstream direction. However, the OLT does use the envelope descriptors, OLT Envelope Commitment process (see 144.3.8.9), and Envelope Activation process (see 144.3.8.11) in a manner similar to how these processes are used in the ONUs. In the case of the OLT, the transition from inter-envelope idle to data transmission begins with the issuing of an envelope descriptor by the OLT MPMC client (MPCP). The envelope descriptor is processed by the OLT Envelope Commitment state diagram and Envelope Activation state diagram as described for the ONU.

144.3.8.1 Constants

MPCP_PROCESS_DLY
: Type: 32-bit unsigned integer
Description: This constant represents the maximum time allowed for the ONU to complete MPCPDU processing.
Value: 6400 (16.384 μs)
Unit: EQT

GATE_TIMEOUT
: Type: 32-bit unsigned integer
Description: This constant represents the maximum allowed interval of time between two GATE messages generated by the OLT to the same ONU.
Value: 19 531 250 (50 ms)
Unit: EQT

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144.3.8.2 Counters

LocalTime
See 144.2.1.2

144.3.8.3 Variables

Back2BackEnv[]
Type: 2-element array of Boolean values
Description: Each element of this array is associated with the respective MCRS channel and represents whether the next envelope is to be transmitted immediately upon completion of the previous envelope (if both envelopes belong to the same grant). The value is set to true upon activation of the first envelope in a grant and it is reset to false upon activation of the grant-terminating envelope (i.e., an envelope with LLID = ESC_LLID).

BEGIN
See 142.2.5.2

ChIndex
Type: 1-bit unsigned integer
Description: The value of this variable indicates the channel the envelope descriptor is intended for, where the value of 0 corresponds to channel 0, and the value of 1 corresponds to channel 1.

ChState
See 144.3.7.3

Env
Type: structure
Description: Env is a structure representing a single envelope descriptor. It includes the following fields:
LLID: the 16-bit LLID value of an envelope descriptor
StartTime: the 32-bit start time of the given envelope. Within a single burst, all envelope descriptions have the same StartTime value. The StartTime is expressed in units of EQT.
Length: the 22-bit length of the envelope, including the envelope header. The Length value is expressed in units of EQ.

EnvIndex
Type: 16-bit unsigned integer
Description: The value of this variable indicates the index of the envelope descriptor in the MsgEnvGroup message.

EnvList[]
Type: an array of lists (FIFO) containing envelope descriptors (see Env variable).
Description: Each element of the array is associated with the respective MCRS channel. Each EnvList[ch] list supports FIFO access operations as defined in 142.1.1.6.

GrantMargin
See 144.3.7.3

NextEnv
See Env variable.

Registered
See 144.3.7.3

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144.3.8.4 Functions

IsValid(llid)

This function returns true if the LLID value llid is active (i.e., is registered and is eligible to transmit data). Otherwise, false is returned.

144.3.8.5 Timers

GateTxTimer

Each instance of the OLT Gate Generation state diagram generates GATE MPCPDUs with a periodicity of less than GATE_TIMEOUT. This timer counts down the time remaining before a forced generation of a GATE MPCPDU by the given instance of this state diagram.

144.3.8.6 Messages

MsgEnvGroup

A set of parameters (operand_list) representing multiple envelope descriptors for a given channel. In the OLT, the MsgEnvGroup is generated by the MPMC client based on local traffic queue status and downstream frame scheduling policies. In the ONU, the MsgEnvGroup is generated by the MPMC client based on envelope allocations (EnvAlloc[n]) received in GATE MPCPDUs. The MsgEnvGroup set includes the following parameters:

ChIndex: A 1-bit integer indicating whether the following envelope descriptors are intended for channel 0 or channel 1.

StartTime: A 32-bit unsigned integer representing the start time of an envelope. This value is expressed in units of EQT.

EnvCount: A 16-bit unsigned integer representing the number of envelope descriptors carried in the message.

EnvLLID[EnvCount]: An array of 16-bit elements, where the *n*th element of the array represents the LLID value for the *n*th envelope descriptor.

EnvLength[EnvCount]: An array of 22-bit elements, where the *n*th element of the array represents the envelope length for the *n*th envelope descriptor.

MsgGate

A set of parameters (operand_list) carried in the GATE MPCPDU, as defined in 144.3.6.1.

144.3.8.7 GATE Generation state diagram

The OLT shall implement an instance of the GATE Generation state diagram, as shown in Figure 144–23, per each registered ONU (PLID).

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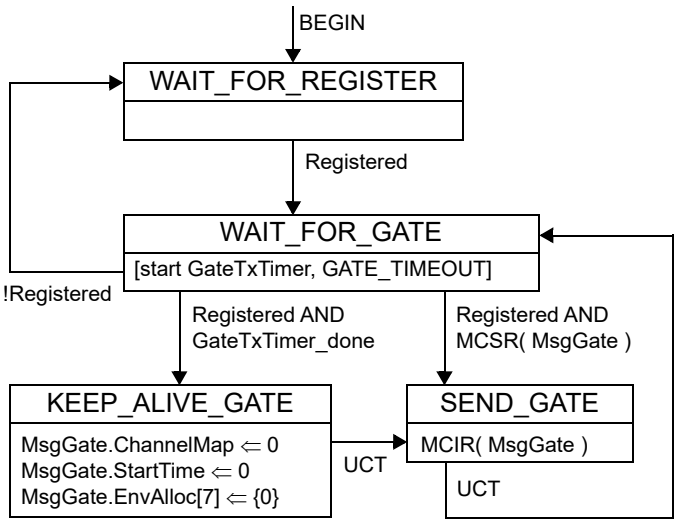

Figure 144–23—GATE Generation state diagram

144.3.8.8 GATE Reception state diagram

The ONU shall implement a single instance of the GATE Reception state diagram as shown in Figure 144–24.

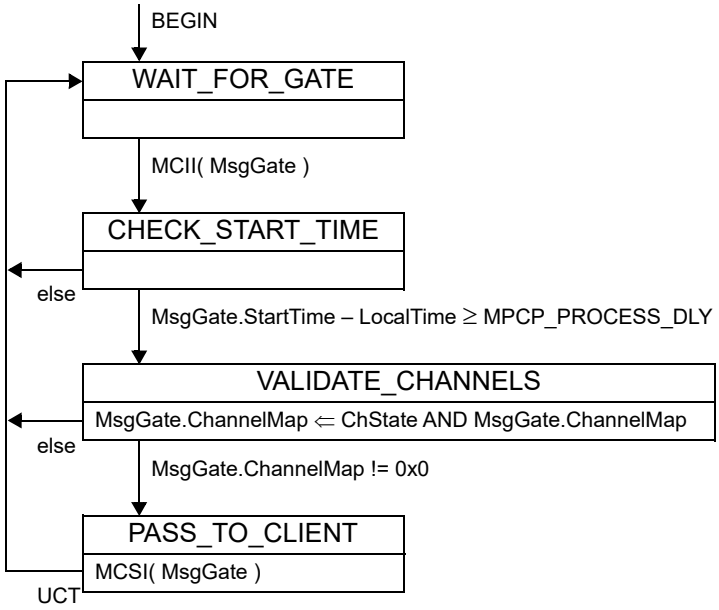

Figure 144–24—GATE Reception state diagram

144.3.8.9 OLT Envelope Commitment state diagram

The OLT shall implement a single instance of the Envelope Commitment state diagram as shown in Figure 144–25.

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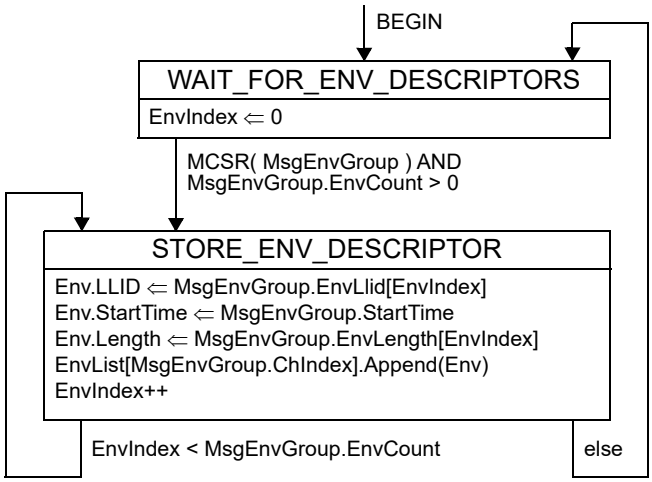

Figure 144–25—OLT Envelope Commitment state diagram

144.3.8.10 ONU Envelope Commitment state diagram

The ONU shall implement a single instance of the Envelope Commitment state diagram as shown in Figure 144–26.

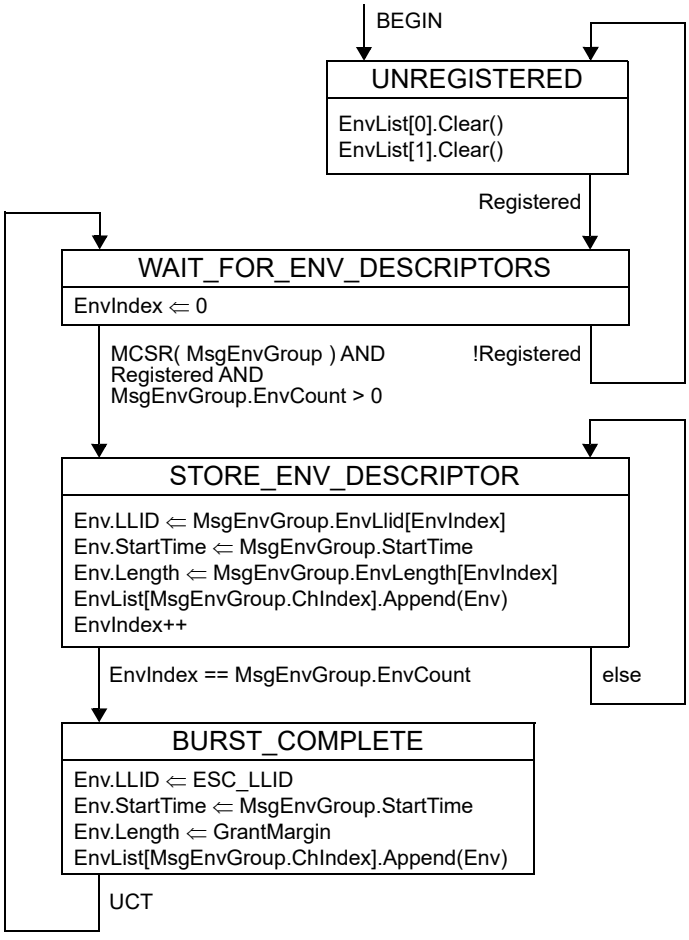

Figure 144–26—ONU Envelope Commitment state diagram

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144.3.8.11 Envelope Activation state diagram

The OLT and the ONU shall implement a single instance of the Envelope Activation state diagram, as depicted in Figure 144–27.

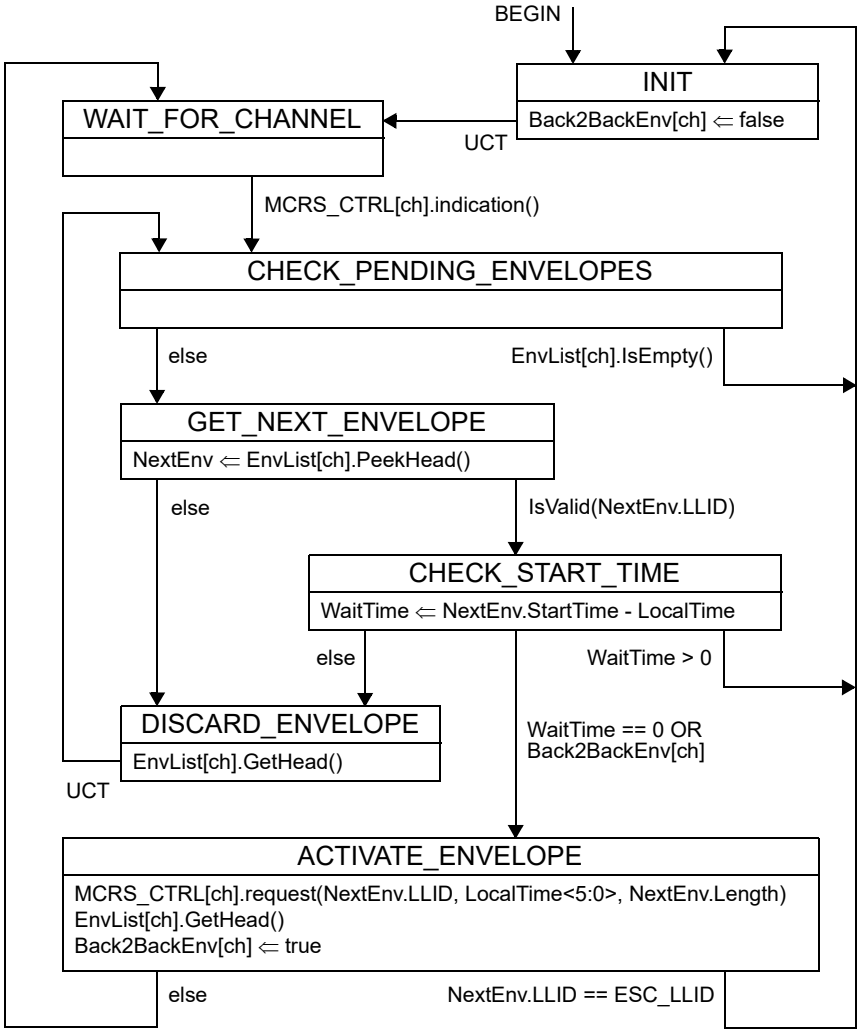

Figure 144–27—Envelope Activation state diagram

144.3.9 Discovery process in dual-rate systems

The MPCP Discovery process (see 144.3.7) facilitates the coexistence of different types of Nx25G-EPON ONUs on the same PON. The coexistence mode allows, for example, 25/10G-EPON, 50/10G-EPON, and 50/25G-EPON ONUs to be deployed on the same ODN and to be connected to the same Nx25G-EPON OLT.

144.3.9.1 OLT rate-specific discovery

The DISCOVERY MPCPDU (see 144.3.6.6) includes the DiscoveryInfo field, which gives the Nx25G-EPON OLT control over the types of ONUs allowed to participate in the given discovery window. Using the DiscoveryInfo field, the OLT indicates its receive line rate capabilities (10 Gb/s and/or 25 Gb/s) as

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well as the specific line rate(s) allowed in the given discovery window. The OLT may open separate (non-overlapping) discovery windows for 10 Gb/s and 25 Gb/s transmission using two separate DISCOVERY MPCPDUs or it may open a single discovery window for both 10 Gb/s and 25 Gb/s line rates using a single DISCOVERY MPCPDU.

Table 144–9 illustrates the different types of ONUs that may respond to a DISCOVERY MPCPDU with the given settings of the DiscoveryInfo sub-fields.

Table 144–9—DISCOVERY MPCPDUs for various Nx25G-EPON ONU types

ONU types targeted by DISCOVERY MPCPDU					DiscoveryInfo field value			
					Upstream capable		Discovery window	
25/10G-EPON	25G-EPON	50/10G-EPON	50/25G-EPON	50G-EPON	10G	25G	10G	25G
X		X			1	0/1	1	0
	X		X	X	0/1	1	0	1
X	X	X	X	X	1	1	1	1

144.3.9.2 ONU rate-specific registration

An unregistered Nx25G-EPON ONU is capable of receiving a DISCOVERY MPCPDU transmitted by the OLT on the DISC_PLID. When received by a 25/10G-EPON or 50/10G-EPON ONU, the DISCOVERY MPCPDU is parsed, and if a 10 Gb/s discovery window is opened, the ONU may attempt to register in the EPON, if other conditions are also satisfied (see definition of the RegAllowed variable in 144.3.7.3). When received by a 25/25G-EPON, 50/25G-EPON, or 50/50G-EPON ONU, the DISCOVERY MPCPDU is parsed, and if a 25 Gb/s discovery window is opened, the ONU may attempt to register in the EPON.

In general, the ONUs attempt to register using the highest upstream transmission rate supported by both the OLT and the ONU. If the OLT advertised itself as 25G capable, but in the current DISCOVERY MPCPDU it has not enabled the 25 Gb/s discovery window, the 25G-capable ONU skips such discovery attempts and waits for a future discovery window in which 25 Gb/s transmission is enabled.

Table 144–10 shows the action the ONU shall take based on the ONU transmit capabilities and the received discovery information.

Table 144–10—ONU action during discovery window

DiscoveryInfo field				ONU upstream capability		ONU action
Upstream capability		Discovery window				
10G	25G	10G	25G	10G	25G	
1	0	1	0	1	0/1	Attempt 10G registration
1	0/1	1	0/1	1	0	Attempt 10G registration
0/1	1	0/1	1	0/1	1	Attempt 25G registration
1	1	0	1	1	0	Wait for 10G discovery window
1	1	1	0	0/1	1	Wait for 25G discovery window

The ONU transmits the REGISTER_REQ MPCPDU in envelopes with the discovery PLID (DISC_PLID, see 144.3.5).

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144.4 Channel Control Protocol (CCP)

The CCP allows the OLT to query and control the state of individual channels (see Table 143–6) through the exchange of CC_REQUEST and CC_RESPONSE CCPDUs, as defined in 144.4.3. Individual channels on the ONU and/or OLT may need to be disabled in a controlled manner for a variety of operational reasons, including power saving, scheduled diagnostic/maintenance activities, optical protection, and others. Any of the channels on the ONU and/or OLT may also fail, requiring a timely notification of the peer station of this fact.

144.4.1 CCP block diagram

Figure 144–28 illustrates a functional block diagram of the CCP for the OLT. The CCP in the OLT includes the CCPDU processing state diagram (see 144.4.4.5).

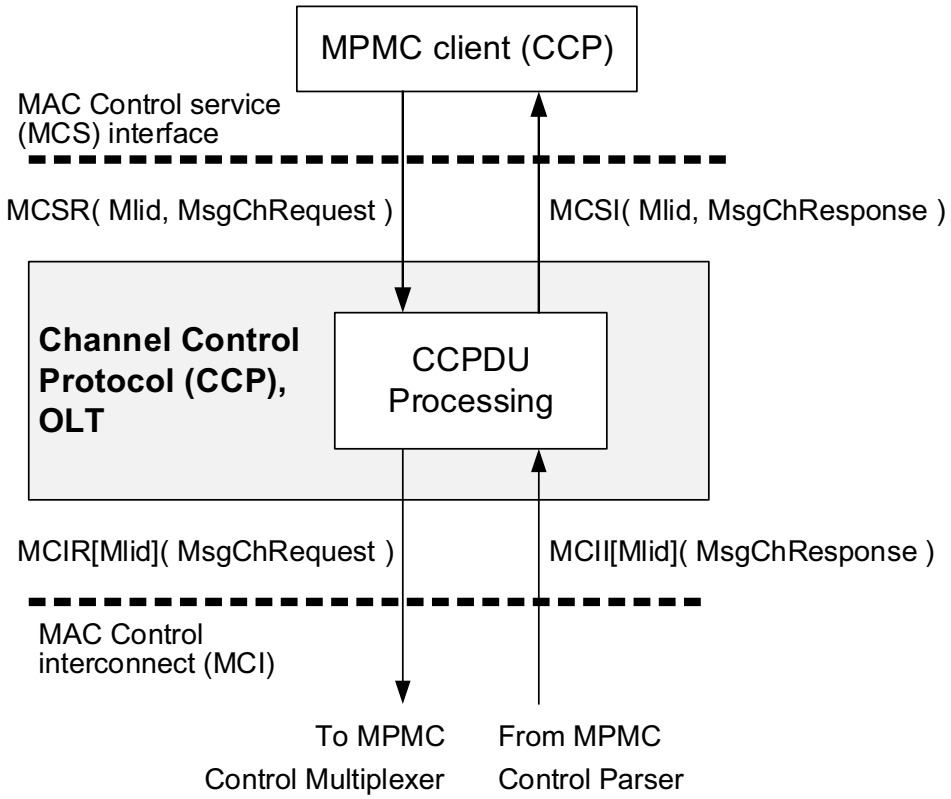

Figure 144–28—OLT CCP functional block diagram

Figure 144–29 illustrates a functional block diagram of the CCP for the ONU. The CCP in the ONU includes the CCPDU processing state diagram (see 144.4.4.6).

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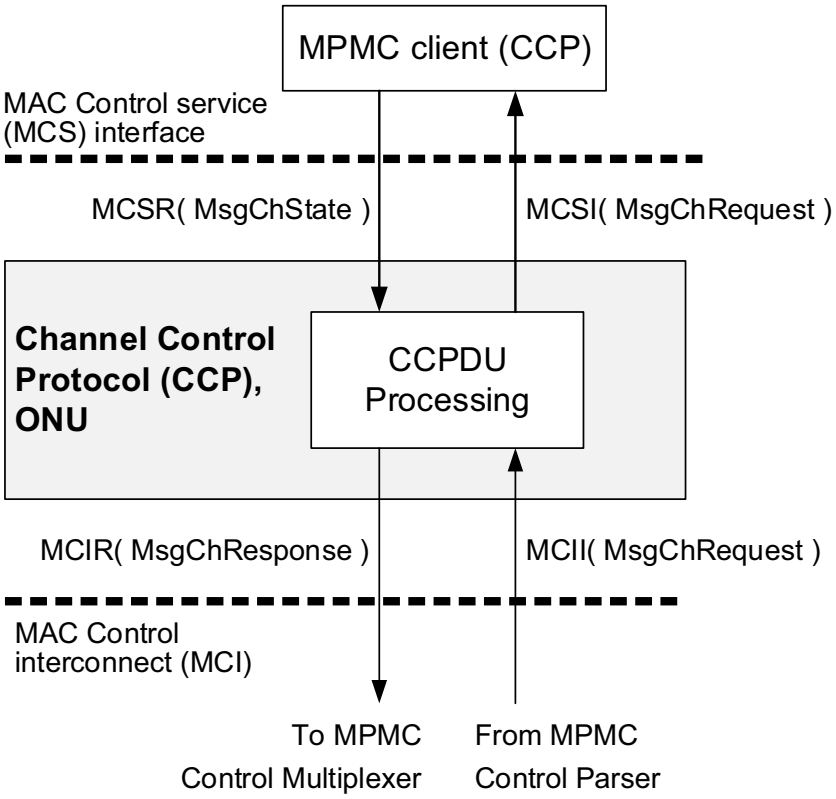

Figure 144–29—ONU CCP functional block diagram

144.4.2 Principles of Channel Control Protocol

The ONU channel status discovery is accomplished via an exchange of a CC_REQUEST and CC_RESPONSE Channel Control PDUs (CCPDUs). Using the CC_REQUEST CCPDU, the OLT polls the state of all downstream and upstream channels, without altering the state of any channels.

The ONU channel status discovery process may be initiated by the OLT MPMC client at any time.

Furthermore, the ONU may send an unsolicited CC_RESPONSE CCPDU to notify the OLT about any local changes in the channel status, including imminent transceiver element (transmitter and/or receive) failure, local channel disabling, power failure and resulting channel shutdown.

Once the CC_RESPONSE CCPDU from the ONU is received, the OLT saves the channel status information associated with the given ONU in the local MPMC client.

Once the ONU channel status discovery has been completed, the OLT MPMC client may change the state of any of the channels on the ONU by requesting the transmission of a CC_REQUEST CCPDU, with specific action encoded for each and every downstream and upstream channel for the given ONU. The OLT may enable a channel, disable a channel, or poll the current channel status.

The OLT may request the ONU to implement changes for the given channel in a persistent or non-persistent manner. Any persistent changes are preserved across ONU reset events. Any non-persistent changes are reverted upon ONU reset and re-registration.

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The ONU receives the CC_REQUEST CCPDU, saves the request information in the local MPMC client, and attempts to implement the requested changes to the channel status. The CC_RESPONSE CCPDU is transmitted back to the OLT with the outcome of the configuration changes for each and every supported channel as well as the current channel state after the change. The ONU updates the ChState variable to match the new upstream channel status (see 144.3.8.3) and purges any pending transmission envelopes for disabled upstream channels.

The sequence of events on the OLT and ONU, when enabling/disabling one of the downstream or upstream channels, is outlined in the following subclauses.

144.4.2.1 Disabling a downstream channel at an ONU

Disabling a downstream channel at an ONU results in the ONU receiver for the given channel being powered down. It is an ONU implementation choice to also shut down the associated receive path through the PCS and MCRS sublayers. If the receive path associated with a disabled channel remains active, it does not result in any accumulation of statistics or increment of error counters on this channel, such as invalid receive blocks or uncorrectable FEC codewords. Disabling a downstream channel at an ONU does not result in the given channel also being disabled at the OLT.

To disable a downstream channel (DC_n) at an ONU, the CCP performs the following sequence of steps:

1) The OLT MPMC client stops transmitting any data to the target ONU on the channel being disabled. The said ONU shortly thereafter stops receiving any data on this downstream channel.
2) The MPMC client initiates transmission of a CC_REQUEST CCPDU to the target ONU, requesting the ONU to disable the downstream channel DC_n.
3) Once the ONU has completed the request, the ONU sends a CC_RESPONSE CCPDU to the OLT, indicating the outcome of the requested configuration changes and the new state of all of its downstream and upstream channels.

144.4.2.2 Enabling a downstream channel at an ONU

Enabling a downstream channel at an ONU results in the ONU receiver for the given channel being powered up. Depending on the ONU implementation, the associated receive path through PCS and MCRS sublayers in the ONU may also need to be powered up.

To enable a downstream channel (DC_n) at an ONU, the CCP performs the following sequence of steps:

1) The MPMC client initiates transmission of a CC_REQUEST CCPDU to the target ONU, requesting the ONU to enable the downstream channel DC_n.
2) Once the ONU has completed the request, the ONU sends a CC_RESPONSE CCPDU to the OLT, indicating the outcome of the requested configuration changes and the new state of all of its downstream and upstream channels.
3) The OLT MPMC client starts transmitting data to the target ONU on the channel being enabled only when the given downstream channel is confirmed to have been enabled on the ONU. The said ONU shortly thereafter starts receiving data on this downstream channel.

144.4.2.3 Disabling an upstream channel at an ONU

Disabling an upstream channel at an ONU results in the ONU transmitter for the given channel being powered down. It is an ONU implementation choice to also shut down the associated transmit path through the PCS and MCRS sublayers. If the transmit path associated with a disabled channel remains active, it does not result in any accumulation of statistics or increment of error counters on this channel, such as packets or

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octets transmitted. Disabling an upstream channel at an ONU does not result in the given channel also being disabled at the OLT.

To disable an upstream channel (UC_n) at an ONU, the CCP performs the following sequence of steps:

1) The MPMC client initiates transmission of a CC_REQUEST CCPDU to the target ONU, requesting the ONU to disable the upstream channel UC_n.
2) The OLT MPMC client continues to grant the upstream channel UC_n on the target ONU.
3) Once the ONU has completed the request, the ONU sends a CC_RESPONSE CCPDU to the OLT, indicating the outcome of the requested configuration changes and the new state of all of its downstream and upstream channels. ONU also purges any pending upstream transmission envelopes scheduled for the now disabled upstream channel.
4) The OLT MPMC client stops granting the upstream channel UC_n on the target ONU only when the given upstream channel is confirmed to have been disabled on the ONU.

144.4.2.4 Enabling an upstream channel at an ONU

Enabling an upstream channel at an ONU results in the ONU transmitter for the given channel being powered up. Depending on the ONU implementation, the associated transmit path through PCS and MCRS sublayers in the ONU may also need to be powered up.

To enable an upstream channel (UC_n) at an ONU, the CCP performs the following sequence of steps:

1) The MPMC client initiates transmission of a CC_REQUEST CCPDU to the target ONU, requesting the ONU to enable the upstream channel UC_n.
2) Once the ONU has completed the request, the ONU sends a CC_RESPONSE CCPDU to the OLT, indicating the outcome of the requested configuration changes and the new state of all of its downstream and upstream channels.
3) The OLT MPMC client starts granting the upstream channel UC_n on the target ONU only when the given upstream channel is confirmed to have been enabled on the ONU.

144.4.2.5 Local channel state changes at an ONU

The MPMC client may monitor and react to the changes in the state of the downstream and/or upstream channels, allowing the ONU to notify the OLT of observed or expected channel state changes. For example, the MPMC client may have ability to detect a failure of one of the channel receivers.

To notify the MPMC client at the OLT about a local channel state change, the CCP performs the following sequence of steps:

1) When a channel state change is identified, the MPMC client at the ONU sends an unsolicited CC_RESPONSE CCPDU to the OLT, indicating the new state of all of its downstream and upstream channels.
2) If a state change for an upstream channel is being reported, the OLT MPMC client may adjust granting for the affected upstream channel. Similarly, if a state change for a downstream channel is being reported, the OLT MPMC client may adjust downstream transmission on the affected downstream channel.

144.4.3 CCPDU structure and encoding

The CCPDU structure is shown in Figure 144–30, and is further defined as follows:

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— DestinationAddress:
In CCPDUs, the DestinationAddress is the MAC Control Multicast address as specified in the annexes to Clause 31.

— SourceAddress:
In CCPDUs, the SourceAddress is the individual MAC address associated with the MLID through which the CCPDU is transmitted. For CCPDUs originating at the OLT, this may be the address of any individual MAC. These MACs may all share a single unicast address, as explained in 144.1.1.2.

— Length/Type:
In CCPDUs, this field carries the MAC_Control_type field value as specified in 31.4.1.3.

— Opcode:
This field identifies the specific CCPDU being encapsulated. Opcode field values are defined in Table 31A–1.

— OperandList:
A set of opcode-specific fields as defined in 144.4.3.1 and 144.4.3.2.

— Pad:
This field is present only when the total length of the OperandList is below 44 octets. The Pad field is added to bring the CCPDU length up to the minimum frame size (see 4A.2.3.2.4). This field is filled with zeros on transmission, and is ignored on reception.

— FCS:
This is the frame check sequence, typically generated by the MAC.

Fields within a frame are transmitted from top to bottom. When consecutive octets are used to represent a single numerical value, the most significant octet is transmitted first, followed by successively less significant octets. Bits within each octet are transmitted from LSB to MSB.

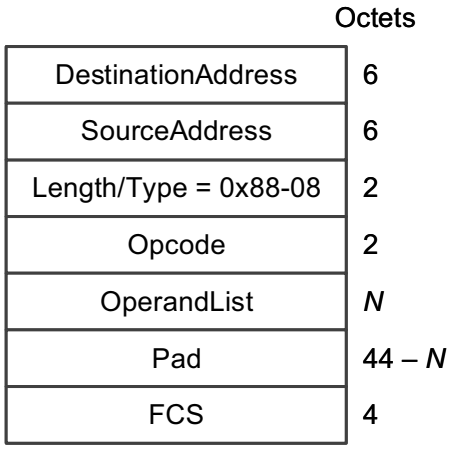

Figure 144–30—Generic CCPDU

144.4.3.1 CC_REQUEST description

The CC_REQUEST CCPDU is used by the OLT to query the state of ONU's channel(s) or change the state of ONU's channel(s), depending on the specific action code carried in the action field associated with the given upstream or downstream channel.

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The CC_REQUEST CCPDU is an instantiation of the Generic CCPDU and shall be as shown in Figure 144–31.

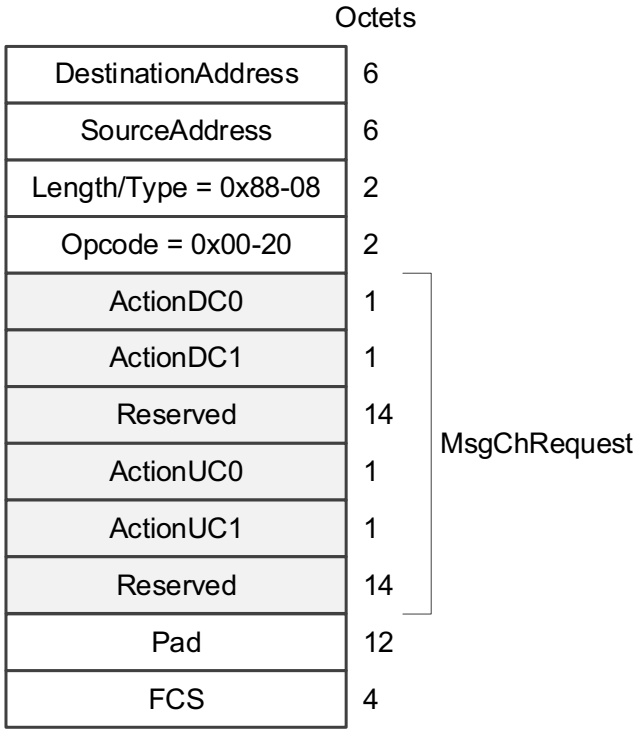

Figure 144–31—CC_REQUEST CCPDU

The CC_REQUEST CCPDU is identified by the Opcode field value of 0x00-20. The MsgChRequest structure represents a set of opcode-specific fields, defined as follows:

— ActionDC0:
This 8-bit field conveys the action requested for the downstream channel 0 (DC0). The encoding of this field is defined in Table 144–11.

— ActionDC1:
This 8-bit field conveys the action requested for the downstream channel 1 (DC1). The encoding of this field is defined in Table 144–11.

— ActionUC0:
This 8-bit field conveys the action requested for the upstream channel 0 (UC0). The encoding of this field is defined in Table 144–11.

— ActionUC1:
This 8-bit field conveys the action requested for the upstream channel 1 (UC1). The encoding of this field is defined in Table 144–11.

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Table 144–11—Channel Action field [a]

Bit	Field name	Value	Description
3:0	ActionCode	0x0	No action
		0x1	Disable channel
		0x2	Enable channel
		0x3–0xF	Reserved, ignored on reception
6:4	Reserved, ignored on reception		
7	PersistenceFlag	0	The channel action is non-persistent, i.e., the requested channel state is not preserved across the reset event. Upon reset, the channel reverts to its previous persistent state.
		1	The channel action is persistent, i.e., the requested channel state is to preserved across the reset event.

[a] Persistently disabling all downstream and/or all upstream channels in an ONU makes that ONU non-operational.

144.4.3.2 CC_RESPONSE description

The CC_RESPONSE CCPDU is generated by the ONU to report its current channel(s) state and/or convey to the OLT the result code for the last requested action (CC_REQUEST CCPDU).

The CC_RESPONSE CCPDU is an instantiation of the Generic CCPDU and shall be as shown in Figure 144–32.

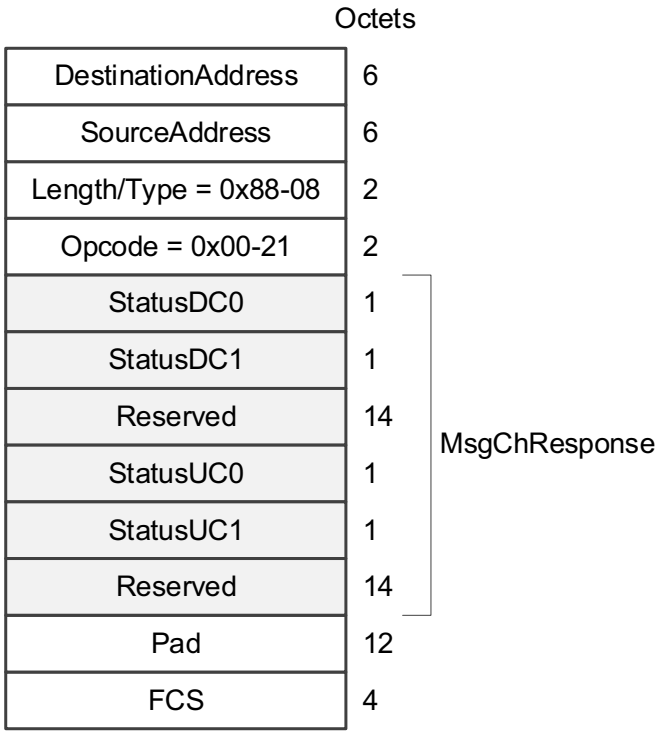

Figure 144–32—CC_RESPONSE CCPDU

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The CC_RESPONSE CCPDU is identified by the Opcode field value of 0x00-21. The MsgChResponse structure represents a set of opcode-specific fields, defined as follows:

— StatusDC0:
This 8-bit field carries the channel state and the action response code for the downstream channel 0 (DC0). The encoding of this field is defined in Table 144–12.

— StatusDC1:
This 8-bit field carries the channel state and the action response code for the downstream channel 1 (DC1). The encoding of this field is defined in Table 144–12.

— StatusUC0:
This 8-bit field carries the channel state and the action response code for the upstream channel 0 (UC0). The encoding of this field is defined in Table 144–12.

— StatusUC1:
This 8-bit field carries the channel state and the action response code for the upstream channel 1 (UC1). The encoding of this field is defined in Table 144–12.

Table 144–12—Encoding of the channel status

Bit	Field name	Value	Description
3:0	ChannelState	0x0	Channel absent
		0x1	Channel enabled
		0x2	Channel disabled remotely (by the OLT)
		0x3	Channel disabled locally (by the ONU)
		0x4	Channel failure (PMD failure)
		0x5–0xF	Reserved, ignored on reception
7:4	ActionResultCode	0x0	No action requested
		0x1	Action succeeded
		0x2	Action failed
		0x3	No change required, i.e., the channel is already in the requested state
		0x4	Invalid command, i.e., the operation was requested for a non-existing channel
		0x5–0xF	Reserved, ignored on reception

144.4.4 Channel Control operation

144.4.4.1 Constants

ACTION_FAILED
Description: This constant represents the value of ActionResultCode corresponding to “Action failed”, per Table 144–12.
Value: 0x2

ACTION_SUCCEEDED
Description: This constant represents the value of ActionResultCode corresponding to “Action succeeded”, per Table 144–12.
Value: 0x1

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ACT_DISABLE
Description: This constant represents the value of ActionCode corresponding to “Disable channel”, per Table 144–11.
Value: 0x1

ACT_ENABLE
Description: This constant represents the value of ActionCode corresponding to “Enable channel”, per Table 144–11.
Value: 0x2

ACT_NONE
Description: This constant represents the value of ActionCode corresponding to “No action”, per Table 144–11.
Value: 0x0

CH_STATE_ABSENT
Description: This constant represents the value of ChannelState corresponding to “Channel absent”, per Table 144–12.
Value: 0x0

CH_STATE_DISABLED_REMOTE
Description: This constant represents the value of ChannelState corresponding to “Channel disabled remotely (by the OLT)”, per Table 144–12.
Value: 0x2

CH_STATE_ENABLED
Description: This constant represents the value of ChannelState corresponding to “Channel enabled”, per Table 144–12.
Value: 0x1

INVALID_COMMAND.
Description: This constant represents the value of ActionResultCode corresponding to “Invalid command”, per Table 144–12.
Value: 0x4.

NO_ACTION_REQUESTED
Description: This constant represents the value of ActionResultCode corresponding to “No action requested”, per Table 144–12.
Value: 0x0

NO_CHANGE_REQUIRED
Description: This constant represents the value of ActionResultCode corresponding to “No change required”, per Table 144–12.
Value: 0x3

144.4.4.2 Variables

ActionCode[]
Type: 4-element array of 4-bit unsigned integers
Description: Each element of this array stores a copy of the action request for the given channel, as received in the CC_REQUEST CCPDU, with individual admissible values per Table 144–11, ActionCode field. This array is indexed with the channel designator, i.e., DC0, DC1, UC0, and UC1.

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BEGIN
See 142.2.5.2

ChState
See 144.3.7.3

PrevChState[]
Type: 4-element array of 4-bit unsigned integers
Description: Each element of this array indicates the previous (old) status of the given upstream or downstream channel, with individual admissible values per Table 144–12, ChannelState field. This array is indexed with the channel designator, i.e., DC0, DC1, UC0, and UC1.

144.4.4.3 Functions

GetResponseCode(chIndex)
This function generates an action response code for a channel identified by chIndex. The response code is determined by the channel state before the action was requested (OldState), the type of the requested action (ActionCode), and the channel state after the action was implemented (NewState).

```
int4 GetResponseCode( int chIndex )
{
    OldState = PrevChState[ chIndex ];
    NewState = MsgChState[ chIndex ];
    Action = ActionCode[ chIndex ];

    if( Action == ACT_NONE )
        return NO_ACTION_REQUESTED;

    if( NewState == CH_STATE_ABSENT )
        return INVALID_COMMAND;

    if( Action == ACT_ENABLE )
    {
        if( NewState != CH_STATE_ENABLED )
            return ACTION_FAILED;
        else if( NewState == OldState )
            return NO_CHANGE_REQUIRED;
        else
            return ACTION_SUCCEEDED;
    }

    if( Action == ACT_DISABLE )
    {
        if( NewState != CH_STATE_DISABLED_REMOTE )
            return ACTION_FAILED;
        else if( NewState == OldState )
            return NO_CHANGE_REQUIRED;
        else
            return ACTION_SUCCEEDED;
    }

return INVALID_COMMAND;
}
```


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UpdateChState (chIndex, NewState)

This function updates the state record (ChState) for the given upstream channel chIndex, in the function of the new channel state NewState. When an upstream channel is disabled, this function purges the list of envelope descriptors for the given channel, stored in the EnvList array (see 144.3.8.3).

```
UpdateChState( int chIndex, int NewState )
{
    if (NewState == CH_STATE_ENABLED )
         ChState<chIndex> = 1;
    else
    {
         ChState<chIndex> = 0;
         EnvList[chIndex].Clear();
    }
}
```

144.4.4.4 Messages

MsgChRequest

A set of parameters (operand_list) carried in a CC_REQUEST CCPDU, as defined in 144.4.3.1.

MsgChResponse

A set of parameters (operand_list) carried in a CC_RESPONSE CCPDU, as defined in 144.4.3.2.

MsgChState

A set of parameters (operand_list) representing the current states of ONU's downstream and upstream channels. The operand_list is treated as an array, such that an individual channel state (array element) may be accessed using one of the channel index designators: DC0, DC1, UC0, and UC1 (see Table 143–6). Each channel state is represented by a 4-bit integer with permissible values as defined for the field ChannelState per Table 144–12. The MsgChState is generated by the MPMC client and is processed (consumed) by the CCPDU processing state diagram in the ONU.

144.4.4.5 OLT CCPDU processing state diagram

The OLT CCP shall implement a single instance of the CCPDU processing state diagram shown in Figure 144–33.

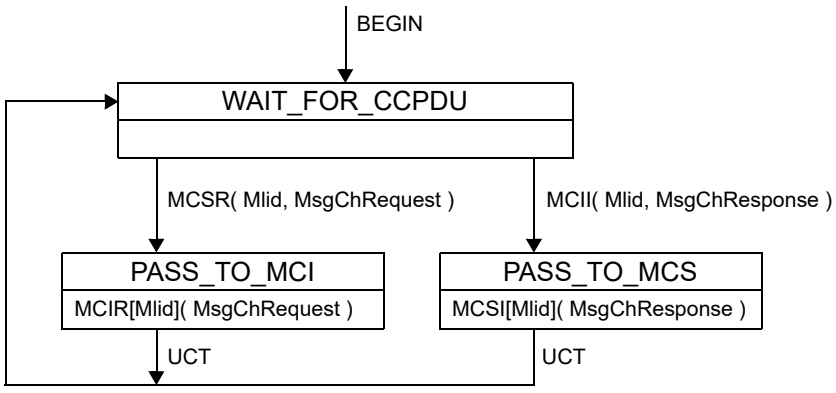

Figure 144–33—CCPDU processing state diagram, OLT

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144.4.4.6 ONU CCPDU processing state diagram

The ONU CCP shall implement a single instance of the CCPDU processing state diagram, as shown in Figure 144–34.

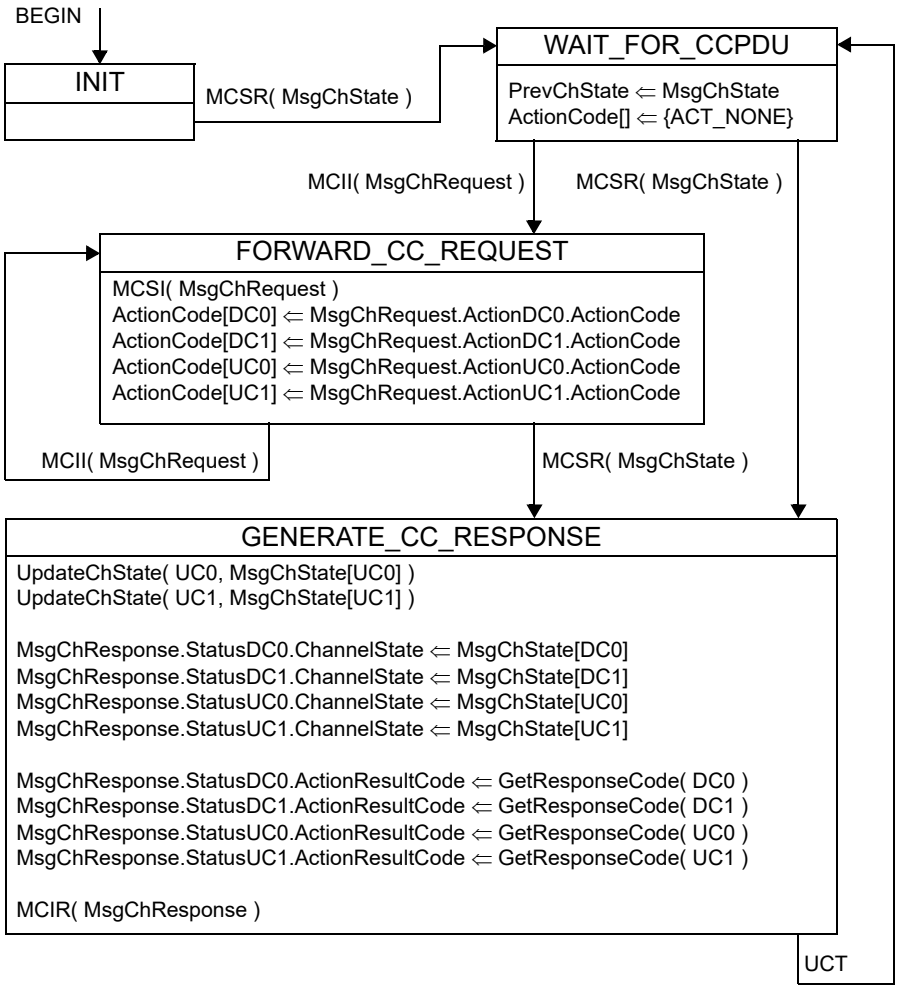

Figure 144–34—CCPDU processing state diagram, ONU

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144.5 Protocol implementation conformance statement (PICS) proforma for Clause 144, Multipoint MAC Control for Nx25G-EPON[239]

144.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 144, Multipoint MAC Control for Nx25G-EPON, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

144.5.2 Identification

144.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

144.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 144, Multipoint MAC Control for Nx25G-EPON
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[239]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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144.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*OLT	OLT functionality	144.1	Device supports functionality required for OLT	O/1	Yes [ ] No [ ]
*ONU	ONU functionality	144.1	Device supports functionality required for ONU	O/1	Yes [ ] No [ ]

144.5.4 PICS proforma tables for Multipoint MAC Control

144.5.4.1 Clock tracking

Item	Feature	Subclause	Value/Comment	Status	Support
CLK1	Clock tracking at OLT	144.2.1.2	LocalTime tracks the 25GMII transmit clock	OLT:M	Yes [ ] N/A [ ]
CLK2	Clock tracking at ONU	144.2.1.2	LocalTime tracks the 25GMII receive clock	ONU:M	Yes [ ] N/A [ ]

144.5.4.2 LLID

Item	Feature	Subclause	Value/Comment	Status	Support
LL1a	Reserved LLID values, transmit	144.3.5	Do not transmit envelopes with ESC_LLID or a reserved value in the LLID field	M	Yes [ ]
LL1b	Reserved LLID values, receive	144.3.5	Ignore envelopes with ESC_LLID or a reserved value in the LLID field	M	Yes [ ]
LL2a	Unregistered ONU, accept envelopes	144.3.5	Accept only the envelopes containing the DISC_PLID value in the LLID field	ONU:M	Yes [ ] N/A [ ]
LL2b	Unregistered ONU, ignore envelopes	144.3.5	Ignore envelopes containing values other than DISC_PLID in the LLID field	ONU:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
LL3a	Registered ONU, accept envelopes	144.3.5	Accept envelopes containing the following values in the LLID field: — The specific PLID value assigned to this ONU during registration — The specific MLID value assigned to this ONU during registration — Broadcast PLID (BCAST_PLID) — Broadcast MLID (BCAST_MLID) — Any ULID or GLID assigned to this ONU by management	ONU:M	Yes [ ] N/A [ ]
LL3b	Registered ONU, ignore envelopes	144.3.5	Ignore envelopes containing the DISC_PLID value in the LLID field	ONU:M	Yes [ ] N/A [ ]

144.5.4.3 Protocol-independent state diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Control Parser	144.2.1.5	Meets the requirements of Figure 144–5	M	Yes [ ]
SM2	Control Multiplexer	144.2.1.6	Meets the requirements of Figure 144–6	M	Yes [ ]

144.5.4.4 MPCP

Item	Feature	Subclause	Value/Comment	Status	Support
MP1	GATE structure	144.3.6.1	As in Figure 144–12	M	Yes [ ]
MP1a	Grant start time and size	144.3.6.1	Transmission on each channel starts at the ONU's local time equal to the StartTime value and has the length as necessary to transmit all allocated envelopes (the sum of all EnvLength fields) together with the associated optical and FEC overhead	ONU:M	Yes [ ] N/A [ ]
MP1b	Fragmentation	144.3.6.1	When flag F is set to 0, do not fragment new frames	ONU:M	Yes [ ] N/A [ ]
MP1c	Forced report	144.3.6.1	When flag FR is set to 1, report the total length of the frames (including IPG and preamble), queued for transmission on this specific LLID	ONU:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MP1d	MPCPDU fragmentation	144.3.6.1	ONU does not fragment MPCPDU frames, regardless of the value of the Fragmentation flag in the EnvAlloc structure that allocates a PLID envelope	ONU:M	Yes [ ] N/A [ ]
MP2	REPORT structure	144.3.6.2	As in Figure 144–13	M	Yes [ ]
MP3	REGISTER_REQ structure	144.3.6.3	As in Figure 144–14	M	Yes [ ]
MP4	REGISTER structure	144.3.6.4	As in Figure 144–15	M	Yes [ ]
MP5	REGISTER_ACK structure	144.3.6.5	As in Figure 144–16	M	Yes [ ]
MP6	DISCOVERY structure	144.3.6.6	As in Figure 144–17	M	Yes [ ]
MP6a	Discovery attempt	144.3.6.6	Attempt to register on a single channel only	ONU:M	Yes [ ] N/A [ ]
MP6b	OnuRssiMin trigger	144.3.6.6	Generate a REGISTER_REQ message in the given discovery window only when measured RSSI is greater or equal to OnuRssiMin	ONU:M	Yes [ ] N/A [ ]
MP6c	OnuRssiMax trigger	144.3.6.6	Generate a REGISTER_REQ message in the given discovery window only when measured RSSI is smaller than or equal to OnuRssiMax	ONU:M	Yes [ ] N/A [ ]
MP6d	Discovery attempt at 10 Gb/s	144.3.6.6	ONU does not generate REGISTER_REQ MPCPDU using the 10 Gb/s upstream channel if the OLT did not open the 10 Gb/s discovery window, i.e., if bit 5 was set to 0	ONU:M	Yes [ ] N/A [ ]
MP6e	Discovery attempt at 25 Gb/s	144.3.6.6	ONU does not generate REGISTER_REQ MPCPDU using the 25 Gb/s upstream channel if the OLT did not open the 25 Gb/s discovery window, i.e., if bit 6 was set to 0	ONU:M	Yes [ ] N/A [ ]
MP6f	Discovery attempt for ONU supporting coexistence class G	144.3.6.6	ONU does not generate a REGISTER_REQ MPCPDU if the OLT does not allow the G-type coexistence, i.e., if bit 14 was set to 0	ONU:M	Yes [ ] N/A [ ]
MP6g	Discovery attempt for ONU supporting coexistence class X	144.3.6.6	ONU does not generate a REGISTER_REQ MPCPDU if the OLT does not allow the X-type coexistence, i.e., if bit 15 was set to 0	ONU:M	Yes [ ] N/A [ ]
MP7	SYNC_PATTERN structure	144.3.6.7	As in Figure 144–18	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MP8	MPCPDU timing on transmit	144.3.1.1	When multiple MPCPDUs are transmitted within a single envelope, all these MPCPDUs have the same Timestamp field value, referencing the transmission time of the ESH	M	Yes [ ]
MP9a	Discovery Initiation in OLT	144.3.7.6	Meets the requirements of Figure 144–20, single instance associated with DISC_PLID	OLT:M	Yes [ ] N/A [ ]
MP9b	Registration Completion in OLT	144.3.7.7	Meets the requirements of Figure 144–21, one instance for each unicast PLID being registered	OLT:M	Yes [ ] N/A [ ]
MP9c	Registration in ONU	144.3.7.8	Meets the requirements of Figure 144–22, single instance	ONU:M	Yes [ ] N/A [ ]
MP10a	GATE Generation	144.3.8.7	Meets the requirements of Figure 144–23, one instance for each registered unicast PLID	OLT:M	Yes [ ] N/A [ ]
MP10b	GATE Reception	144.3.8.8	Meets the requirements of Figure 144–24, single instance	ONU:M	Yes [ ] N/A [ ]
MP11a	Envelope Commitment in OLT	144.3.8.9	Meets the requirements of Figure 144–25, single instance	OLT:M	Yes [ ] N/A [ ]
MP11b	Envelope Commitment in ONU	144.3.8.10	Meets the requirements of Figure 144–26, single instance	ONU:M	Yes [ ] N/A [ ]
MP11c	Envelope Activation	144.3.8.11	Meets the requirements of Figure 144–27, single instance	M	Yes [ ]
MP12	ONU multi-rate discovery	144.3.9.2	ONU takes action based on the ONU transmit capabilities and the received discovery information, as shown in Table 144–10	ONU:M	Yes [ ] N/A [ ]
MP13	MPCP delay variability	144.3.3	Maintain the combined delay variation through the MAC and PHY of less than one EQT for channels operating at 25.78125 GBd and less than two EQTs for channels operating at 10.3125 GBd	M	Yes [ ]
MP14a	Granting overlapping envelopes to the PLID	144.3.1.2	OLT does not allocate overlapping envelopes to the PLID, except the fully overlapping envelopes (see Figure 143–5)	OLT:M	Yes [ ] N/A [ ]
MP14b	processing partially overlapping PLID envelope allocations	144.3.1.2	If ONU receives partially overlapping PLID envelope allocations, it chooses only one of these envelopes for MPCPDU transmission, and only if the envelope length is enough for at least one complete MPCPDU	ONU:M	Yes [ ] N/A [ ]

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144.5.4.5 CCP

Item	Feature	Subclause	Value/Comment	Status	Support
CP1	CCPDU structure	144.4.3	As in Figure 144–30	M	Yes [ ]
CP2	CC_REQUEST structure	144.4.3.1	As in Figure 144–31	M	Yes [ ]
CP3	CC_RESPONSE structure	144.4.3.2	As in Figure 144–32	M	Yes [ ]
CP4a	CCP processing in OLT	144.4.4.5	Meets the requirements of Figure 144–33, single instance	OLT:M	Yes [ ] N/A [ ]
CP4b	CCP processing in ONU	144.4.4.6	Meets the requirements of Figure 144–34, single instance	ONU:M	Yes [ ] N/A [ ]

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145. Power over Ethernet

145.1 Overview

This clause defines the functional and electrical characteristics of an enhanced Power over Ethernet (PoE) system. The original PoE system is defined in Clause 33. Clause 145 includes the capability to provide power over 4 pairs while maintaining compatibility with equipment designed in accordance with Clause 33.

A PoE system consists of three separately specified major elements. They are the power supply, a non-data entity which is called the Power Sourcing Equipment (PSE), the powered load, another non-data entity which is called the Powered Device (PD), and the standards based, balanced, twisted-pair cabling connecting the two.

The cabling portion of the system is defined as the link section. The link section shares use of the cabling with the link segment used for data transmission. The PSE is normally an element of the powering DTE but may, instead, be located within the cabling portion of the system. PSEs located within the cabling portion of the system are called Midspan PSEs, or simply Midspans. The PD is an element of the powered DTE.

The system specified here is for use with IEEE 802.3 MAUs connected by 4-pair twisted pair cabling that have been qualified as being compatible with this clause. Those MAUs are defined in Clause 14 and the PHYs are defined in Clause 25, Clause 40, Clause 55, and Clause 126. Use in other environments is outside the scope of this standard. Power over Ethernet allows devices to supply / use power using the same generic cabling as is used for data transmission.

PSEs and PDs are categorized by Type. This clause specifies Type 3 and Type 4 devices as well as their interaction with Type 1 and Type 2 devices. References in this clause to PSEs and PDs without a Type qualifier refer exclusively to Type 3 and Type 4 devices. See Clause 33 for the specification of Type 1 and Type 2 devices.

Power over Ethernet is intended to provide a 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, or 10GBASE-T device with a single cabling interface for both data and power. This clause specifies the following:

a) A PSE to add power to the 100 Ω balanced cabling system
b) The characteristics of a PD's load on the PSE and the structured cabling
c) A protocol allowing the detection of a PD that requests power from a PSE
d) Methods to classify a PD based on its power needs
e) A method for a connected PSE and PD to dynamically negotiate power
f) A method for scaling supplied power back to the detect level when power is no longer requested or required

The importance of item c) above should not be overlooked. Given the large number of legacy devices (both IEEE 802.3 and other types of devices) that could be connected to a 100 Ω balanced cabling system, and the possible consequences of applying power to such devices, the protocol to distinguish compatible devices and non-compatible devices is important to prevent damage to non-compatible devices.

The detection and powering algorithms are likely to be compromised by cabling that is not point-to-point, resulting in unpredictable performance and possibly damaged equipment.

This clause differentiates between the two ends of the powered portion of the link, i.e. the link section, defining the PSE and the PD as separate but related devices.

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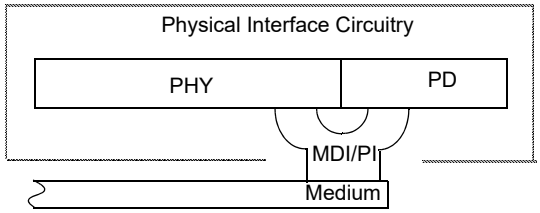
145.1.1 Compatibility considerations

The requirements in this Clause are designed such that PSEs and PDs that meet these requirements are compatible at their respective Power Interfaces (PIs). Designers are free to implement circuitry within the PD and PSE in an application-dependent manner provided that the respective PI specifications are satisfied.

145.1.2 Relationship of Power over Ethernet to the IEEE 802.3 Architecture

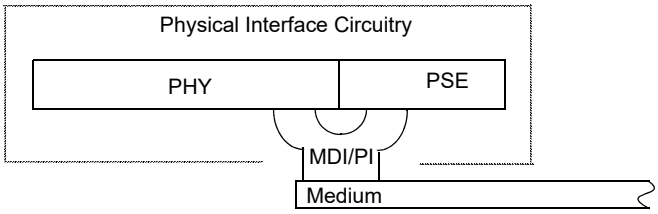
Power over Ethernet comprises an optional non-data entity. As a non-data entity, it does not appear in a depiction of the OSI Reference Model. Figure 145–1 depicts the positioning of PoE in the case of the PD.



MDI = Medium Dependent Interface
PD = Powered Device
PHY = Physical Layer Device
PI = Power Interface

Figure 145–1—Power over Ethernet powered device relationship to the physical interface circuitry and the IEEE 802.3 Ethernet LAN model

Figure 145–2 and Figure 145–3 depict the positioning of PoE in the cases of the Endpoint PSE and the Midspan PSE, respectively.



MDI = Medium Dependent Interface
PHY = Physical Layer Device
PI = Power Interface
PSE = Power Sourcing Equipment

Figure 145–2—Power over Ethernet Endpoint power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 Ethernet LAN model

The Power Interface (PI) is the mechanical and electrical interface between the PSE or PD and the transmission medium as defined in 1.4.484.

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In an Endpoint PSE and in a PD, the PI is the MDI as defined in 1.4.395.

In the case of a Midspan PSE, the PI is physically separate from the MDI and is contained within the cabling portion of the data transmission system.

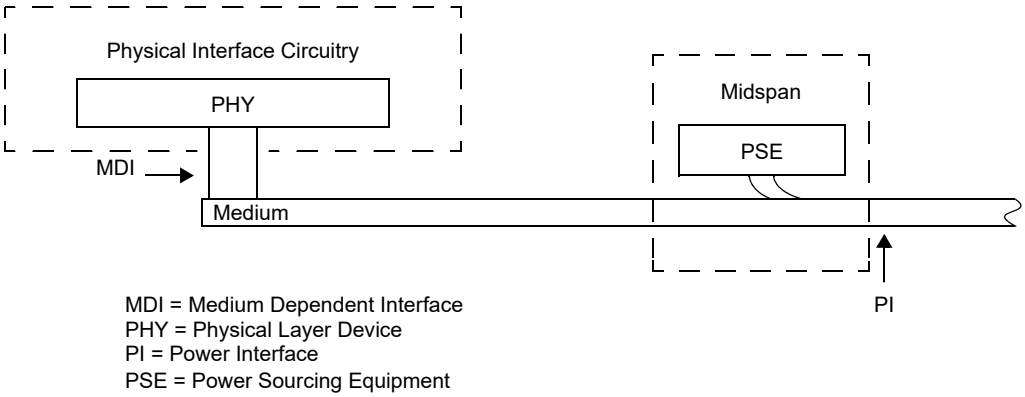

Figure 145–3—Power over Ethernet Midspan power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 Ethernet LAN model

145.1.3 System parameters

A valid power system consists only of a single PSE sourcing power, a single PD, and the link section connecting them. The PSE and PD can each be of a Type defined in Clause 33 or Clause 145, in any combination. The power system has certain basic parameters defined according to Table 145–1. See 33.1.4 for these parameters as applicable to Type 1 and Type 2 devices. These parameters define not only certain performance characteristics of the system, but are also used in calculating the various electrical characteristics of PSEs and PDs as described in 145.2 and 145.3.

Table 145–1—System parameters

PSE Type	Nominal highest current per pair (I_{Cable}, A)	Number of powered pairs	Channel pairset maximum DC loop resistance (R_{Ch}, Ω)	Minimum cabling type
Type 3	0.6	2 or 4	12.5	Class D (ISO/IEC11801:1995) or Category 5 (ANSI/EIA/TIA-568-A:1995)
Type 4	0.6	2	12.5	
	0.96	4	12.5	
NOTE—The current on the pairs may be impacted by pair-to-pair system resistance unbalance. See 145.2.10.6.1. For additional information on pair-to-pair resistance unbalance in structured cabling systems, see TIA TSB-184-A [B66] and ISO/IEC TS 29125.				

I_{Cable}, specified in Table 145–1, is the current on one twisted pair in the balanced twisted-pair cable. When power is delivered over 2 pairs, two twisted pairs are required to source I_{Cable}, one carrying (+ I_{Cable}) and one carrying (– I_{Cable}), from the perspective of the PI.

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When power is delivered over 4 pairs, four twisted pairs are required to source 2 × I_{Cable}, two each carrying a nominal current (+ I_{Cable}) and two each carrying a nominal current (– I_{Cable}), from the perspective of the PI. Greater than Class 4 power delivery requires 4 pairs.

I_{Cable} is the highest nominal current on a pair for a system without pair-to-pair current unbalance. When power is provided over 4 pairs, the current may be unbalanced, causing one pair to have a higher current than I_{Cable}, while the other pair of the same polarity carries a corresponding lower current than I_{Cable}. The maximum nominal total 4-pair current is twice the value of I_{Cable}. See TIA TSB-184-A [B66] and ISO/IEC TS 29125 for additional information on pair-to-pair resistance unbalance.

The cable references use "DC loop resistance," which refers to two single conductors in series. This clause uses "pairset DC loop resistance" (R_{Ch}), which refers to two pairs in series. Therefore, R_{Ch} is related to, but not equivalent to, the "DC loop resistance" called out in the cable references. In addition to I_{Cable}, the requirements of this clause reference the total current and the per pairset current, which are described here.

I_{Port} is the total current on both pairs with the same polarity and is defined in Equation (145–7).

$I_{Port\text{-}2P}$ is the current on the negative pair of a pairset and is derived from $I_{Port\text{-}2P\text{-}pri}$ and $I_{Port\text{-}2P\text{-}sec}$ in Equation (145–5).

Pairset current is the current on the negative pair associated with a given pairset. Note that the positive pair and the negative pair of a pairset may carry a different amount of current, caused by the independent pair-to-pair current unbalance in the positive pairs, and in the negative pairs, when the system is providing power over more than 2 pairs.

2-pair mode refers to power delivery using either one pair at positive V_{PSE} and one at negative V_{PSE}, or to using two pairs at positive V_{PSE} and one at negative V_{PSE}.

4-pair mode refers to power delivery using two pairs at positive V_{PSE} and two at negative V_{PSE}.

R_{Ch} is the maximum pairset DC loop resistance, as defined in Table 145–1.

R_{Chan} is the actual DC resistance from the PSE PI to the PD PI and back. R_{Chan} has a maximum value of R_{Ch} / 2 when operating in 4-pair mode. R_{Chan} has a maximum value of R_{Ch} when operating in 2-pair mode.

$R_{Chan\text{-}2P}$ is the actual pairset DC resistance from the PSE PI to the PD PI and back. $R_{Chan\text{-}2P}$ has a maximum value of R_{Ch}.

V_{PD} is the voltage at the PD PI. For a single-signature PD, V_{PD} is measured between any positive conductor of a pairset and any negative conductor of the corresponding pairset, for the pairset with the highest voltage. For a dual-signature PD, V_{PD} is measured between any positive conductor of a pairset and any negative conductor of the corresponding pairset, for the given Mode.

V_{PSE} is the voltage at the PSE PI. When connected to a single-signature PD and operating in 4-pair mode, V_{PSE} is measured between any positive conductor and any negative conductor. When connected to a dual-signature PD, when operating in 2-pair mode, or when the PD signature configuration has not yet been identified, V_{PSE} is measured between any positive conductor of the pairset and any negative conductor of the corresponding pairset, for the given Alternative.

145.1.4 Cabling requirements

Class D or better cabling as specified in ISO/IEC 11801:1995, with the additional requirement that the channel DC loop resistance is 25 Ω or less, is required to support operation as specified in this Clause. These requirements are also met by Class D or better cabling as specified by ISO/IEC 11801:2002, Category 5e or

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better cable and components as specified in ANSI/TIA-568-C.2, or Category 5 cable and components as specified in ANSI/TIA/EIA-568-A-1995.

Cable ambient operating temperature guidelines for Type 3 and Type 4 operation are provided in ISO/IEC TR 29125 [B44][240] and TIA TSB-184A [B66]. For Type 3 and Type 4 PoE systems, managing the temperature rise can require a reduction in the maximum number of cables bundled. See ISO/IEC TS 29125, TIA TSB-184-A, as well as applicable local codes and regulations, e.g., the National Electrical Code® (NEC®) (NFPA 70®, 2017 Edition) [B56], for more information.

Planning considerations for PoE systems are provided in ISO/IEC CD 14763-2 supported by the information in ISO/IEC TS 29125 and TIA TSB-184-A, as well as applicable local codes and regulations.

Within Clause 145 and its annexes, the term link section refers to the point-to-point medium connection between two and only two active Power Interfaces (PIs). Type 3 and Type 4 operation requires link sections to comply with the intra-pair resistance unbalance requirements for twisted-pair cabling as specified in ISO/IEC 11801:2002 and ANSI/TIA-568-C.2. Refer to Annex 145A for more information including the requirements for pair-to-pair resistance unbalance when operating over 4 pairs.

145.2 Power sourcing equipment (PSE)

The PSE is the portion of the end station or midspan equipment that provides the power to a single PD. The PSE's main functions are as follows:

— To search the link section for a PD
— To supply power to the detected PD through the link section
— To monitor the power on the link section
— To remove power when no longer requested or required, returning to the searching state

An unplugged link section is one instance when power is no longer required.

In addition, power classification mechanisms exist to provide the PSE with detailed information regarding the power needs of the PD.

A PSE is electrically specified at the point of the physical connection to the cabling.

Additional electrical specifications that apply to the PSE are specified in 145.4.

145.2.1 PSE Type descriptions

A PSE can be categorized as either a Type 1, Type 2, Type 3 or Type 4 PSE. See 33.2 for the specification of Type 1 and Type 2 PSEs.

Type 1, Type 2, Type 3, and Type 4 PSEs interoperate with Type 1, Type 2, Type 3, and Type 4 PDs, subject to power limitations. See 145.2.8.

Table 145–2 summarizes the supported parameters of Type 3 and Type 4 PSEs. The PSE Type can only change when the PSE state diagram (Figure 145–13) is in IDLE.

[240]The numbers in brackets correspond to those of the bibliography in Annex A.

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Table 145–2—PSE supported parameters

PSE Type	Supports 4-pair power	Highest Class supported[a]	Short MPS support[b]	Physical Layer classification[a]	Data Link Layer classification[a]	Autoclass[c]
Type 3	No / Yes	1 to 4	Yes	Multiple-Event	Optional	Optional
	Yes	1 to 6				
Type 4	Yes	7 to 8				

[a] See 145.2.8, Table 145–11 and Table 145–12.
[b] See 145.2.12.
[c] See 145.2.8.2 and 145.3.6.2.

145.2.2 PSE location

PSEs may be placed in two locations with respect to the link segment, either coincident with the DTE/Repeater or midspan. A PSE that is coincident with the DTE/Repeater is an “Endpoint PSE”. A PSE that is located within a link segment that is distinctly separate from and between the MDIs is a “Midspan PSE”. The requirements of this document apply equally to Endpoint and Midspan PSEs unless the requirement contains an explicit statement that it applies to only one implementation. The location of various Endpoint and Midspan PSEs are illustrated in Figure 145–4 to Figure 145–11.

PSEs can be compatible with any of the following: 10BASE-T, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, 10GBASE-T.

145.2.3 Midspan PSE variants

There are several variants of Midspan PSEs defined.

10BASE-T/100BASE-TX Midspan PSE:
A Midspan PSE that results in a link that can support only 10BASE-T and 100BASE-TX operation (see Figure 145–8 and Figure 145–10). Note that this limitation is due to the presence of the Midspan PSE whether it is supplying power or not.

1000BASE-T Midspan PSE:
A Midspan PSE that results in a link that can support 10BASE-T, 100BASE-TX, and 1000BASE-T operation (see Figure 145–9 and Figure 145–11).

2.5GBASE-T Midspan PSE:
A Midspan PSE that results in a link that can support 1000BASE-T and 2.5GBASE-T operation, and optionally support 10BASE-T and 100BASE-TX operation (see Figure 145–9 and Figure 145–11).

5GBASE-T Midspan PSE:
A Midspan PSE that results in a link that can support 1000BASE-T, 2.5GBASE-T, and 5GBASE-T operation, and optionally support 10BASE-T and 100BASE-TX operation (see Figure 145–9 and Figure 145–11).

10GBASE-T Midspan PSE:
A Midspan PSE that results in a link that can support 1000BASE-T, 2.5GBASE-T, 5GBASE-T,

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and 10GBASE-T operation, and optionally support 10BASE-T and 100BASE-TX operation (see Figure 145–9 and Figure 145–11).

NOTE—See 145.4.9.3 for Alternative A Midspan PSEs.

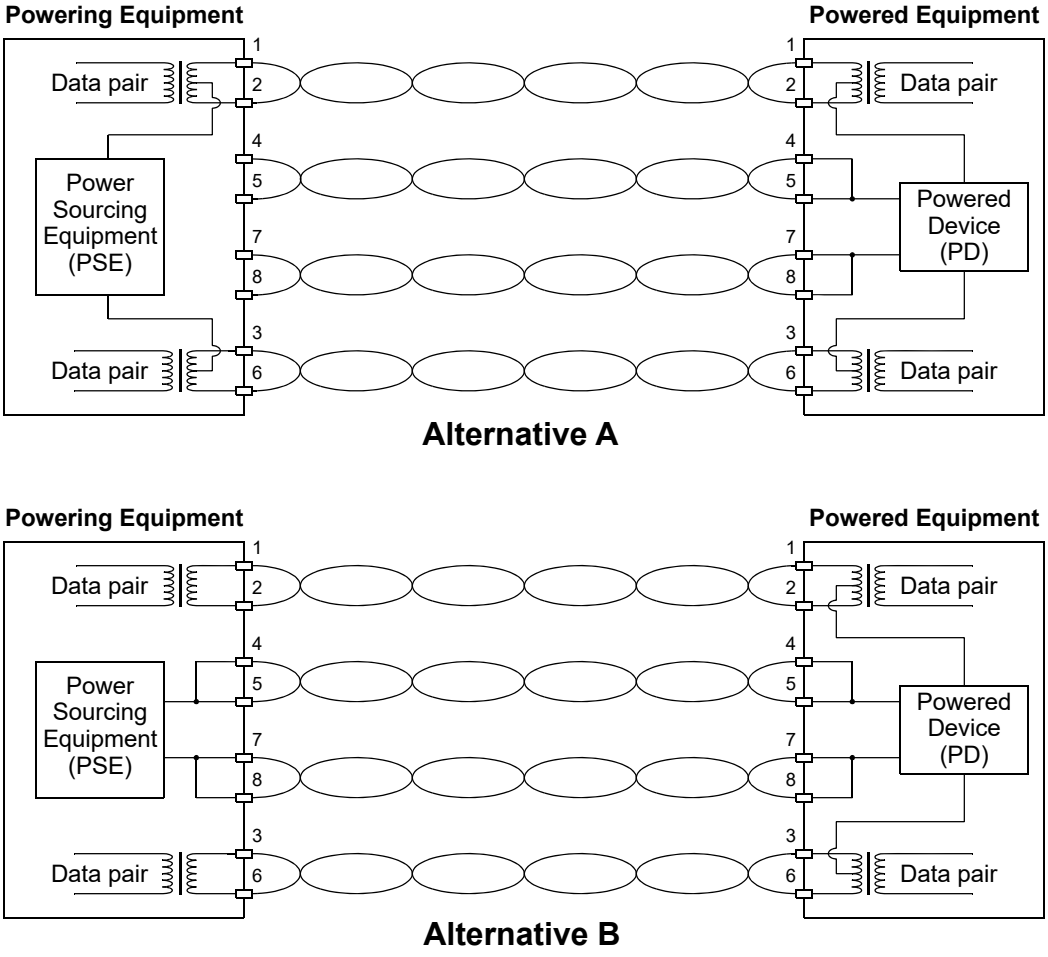

Figure 145–4—10BASE-T/100BASE-TX 2-pair Endpoint PSE location overview

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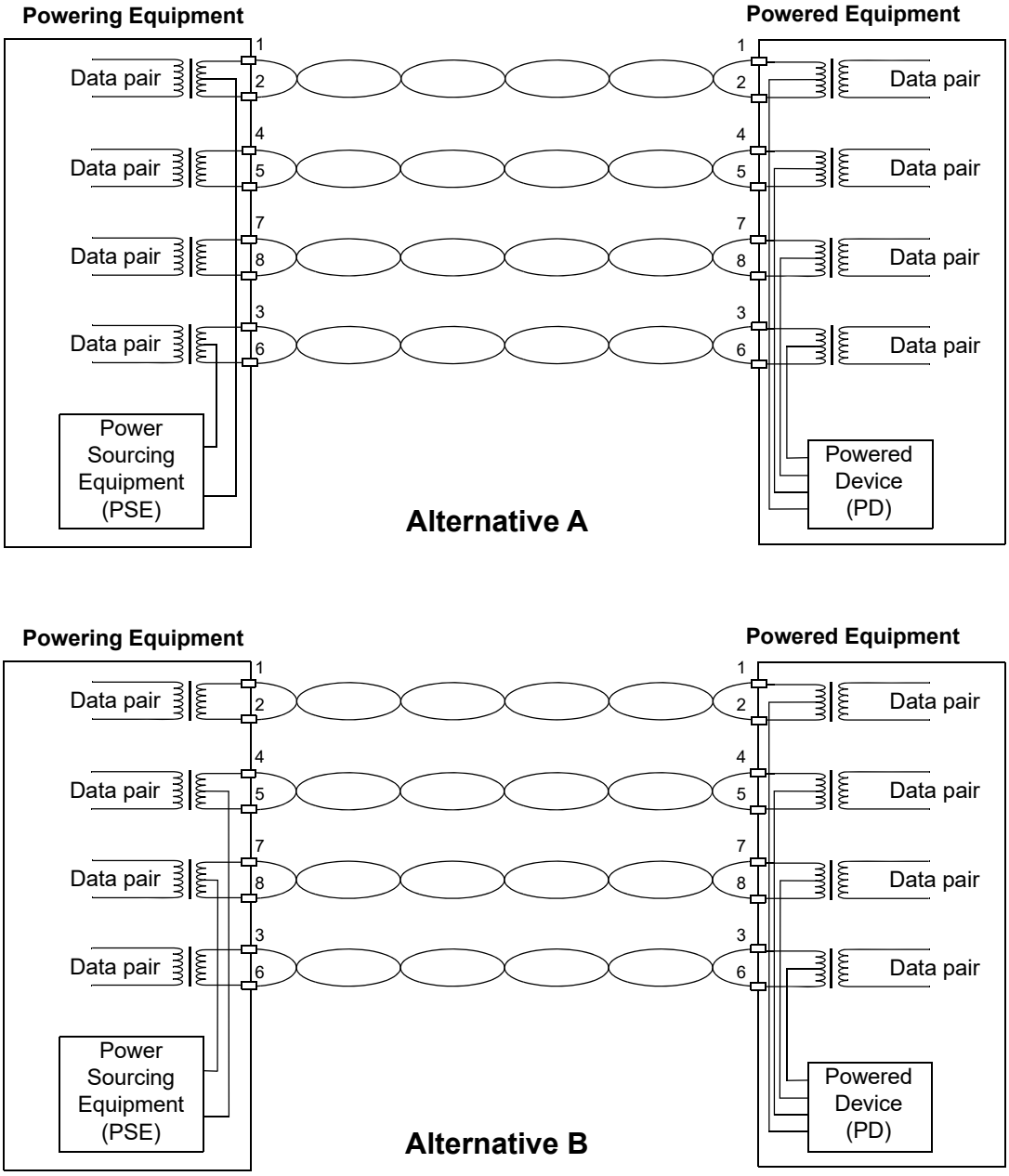

Figure 145–5—1000/2.5G/5G/10GBASE-T 2-pair Endpoint PSE location overview

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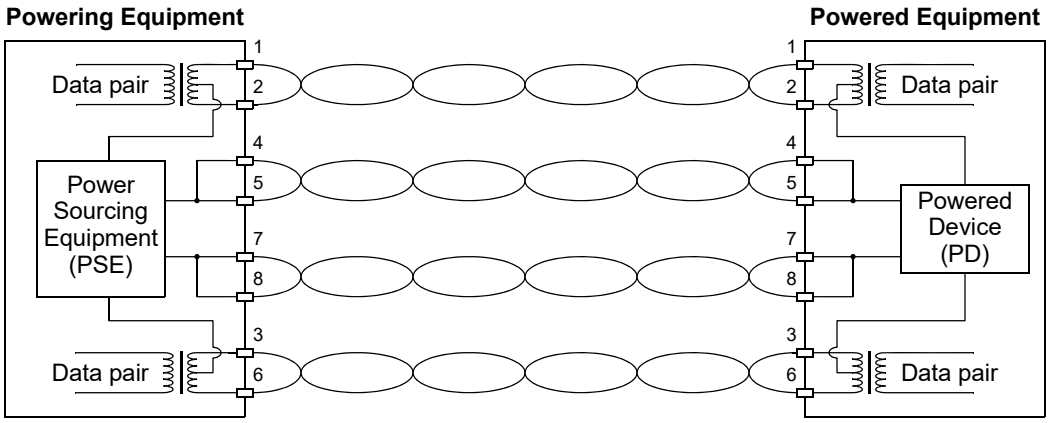

Figure 145–6—10BASE-T/100BASE-TX 4-pair Endpoint PSE location overview

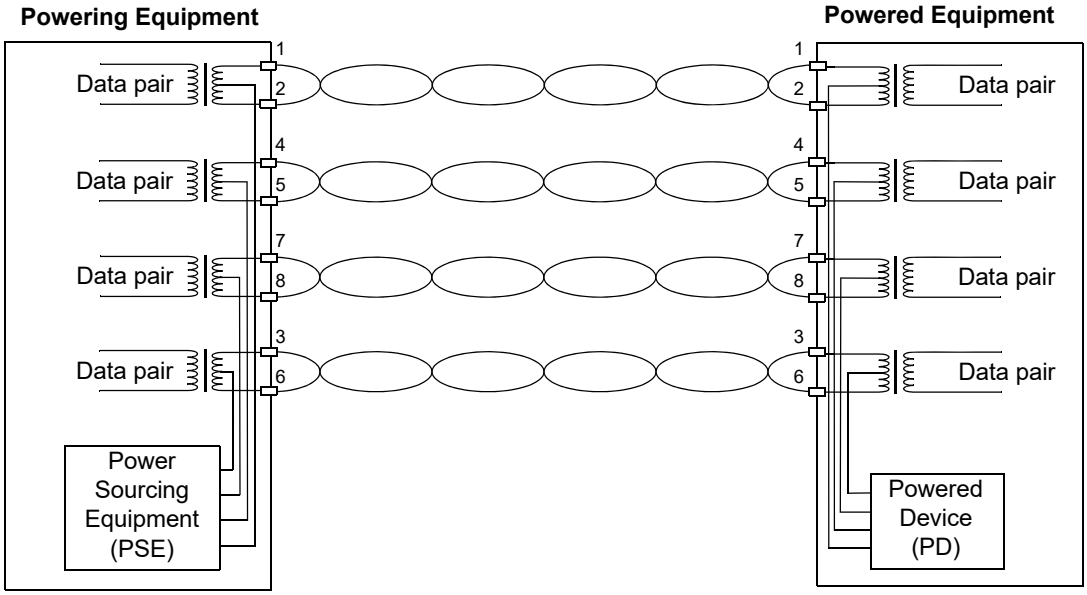

Figure 145–7—1000/2.5G/5G/10GBASE-T 4-pair Endpoint PSE location overview

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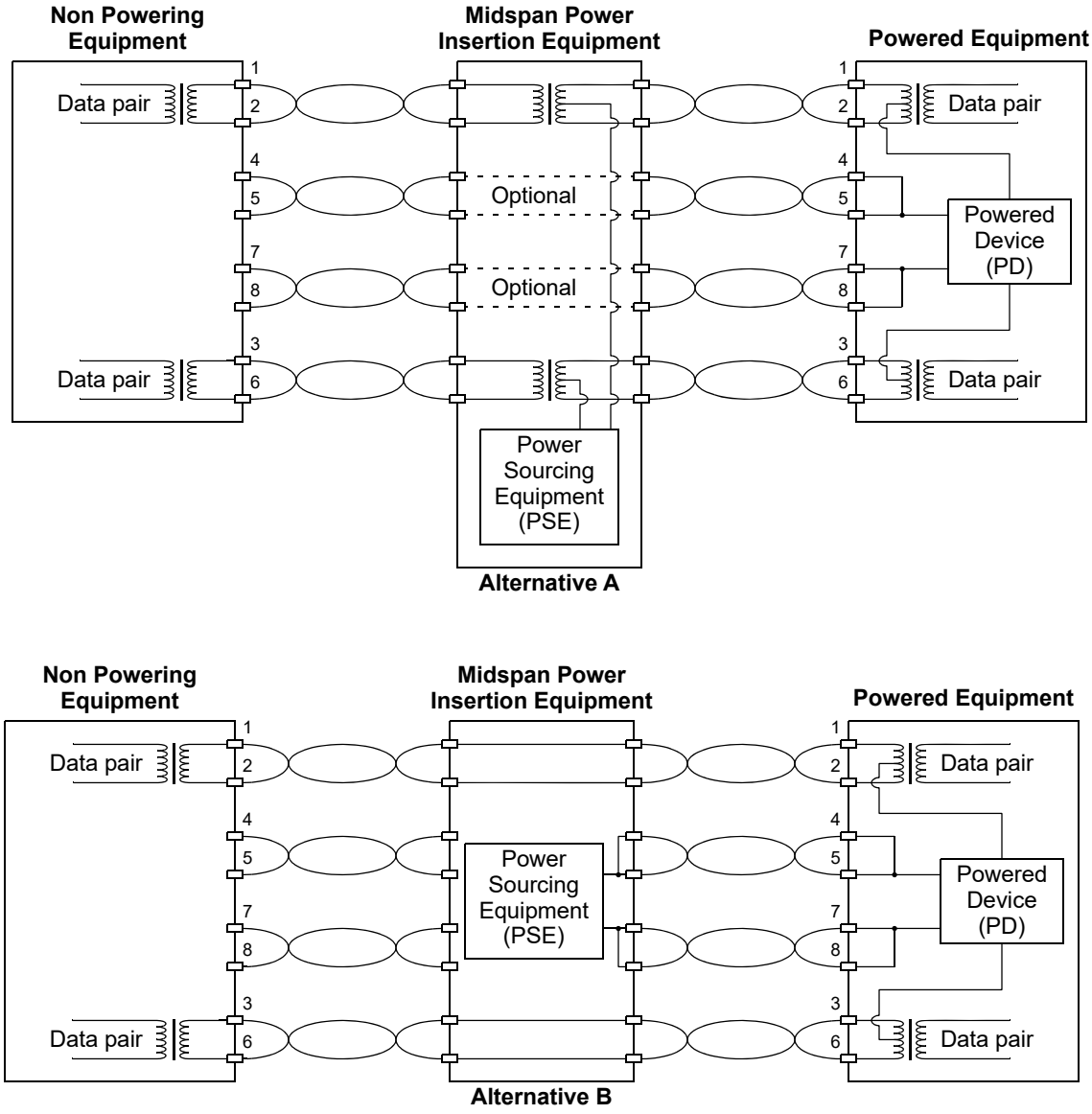

Figure 145–8—10BASE-T/100BASE-TX 2-pair Midspan PSE location overview

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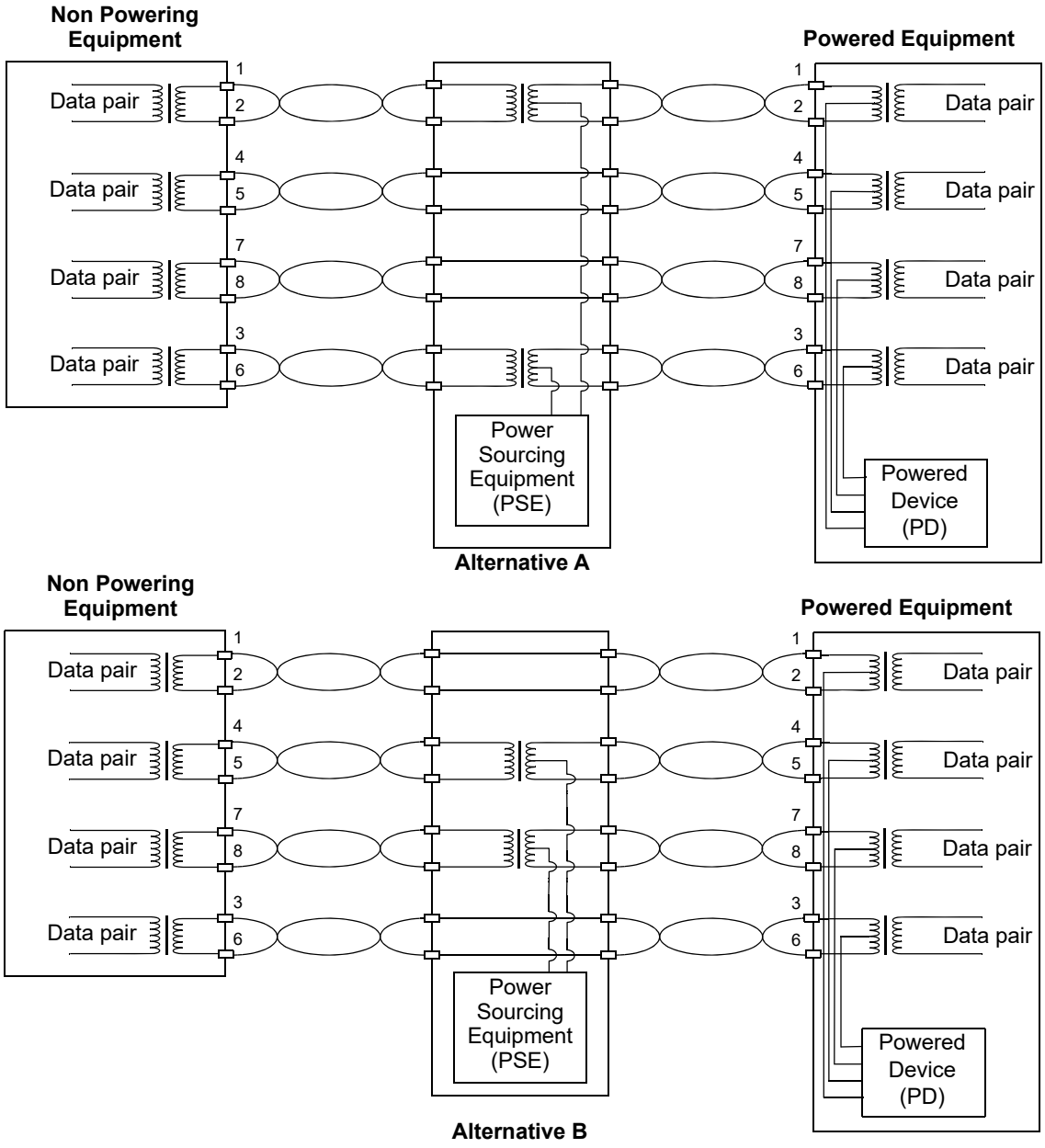

Figure 145–9—1000BASE-T, 2.5G, 5G, or 10GBASE-T 2-pair Midspan PSE location overview

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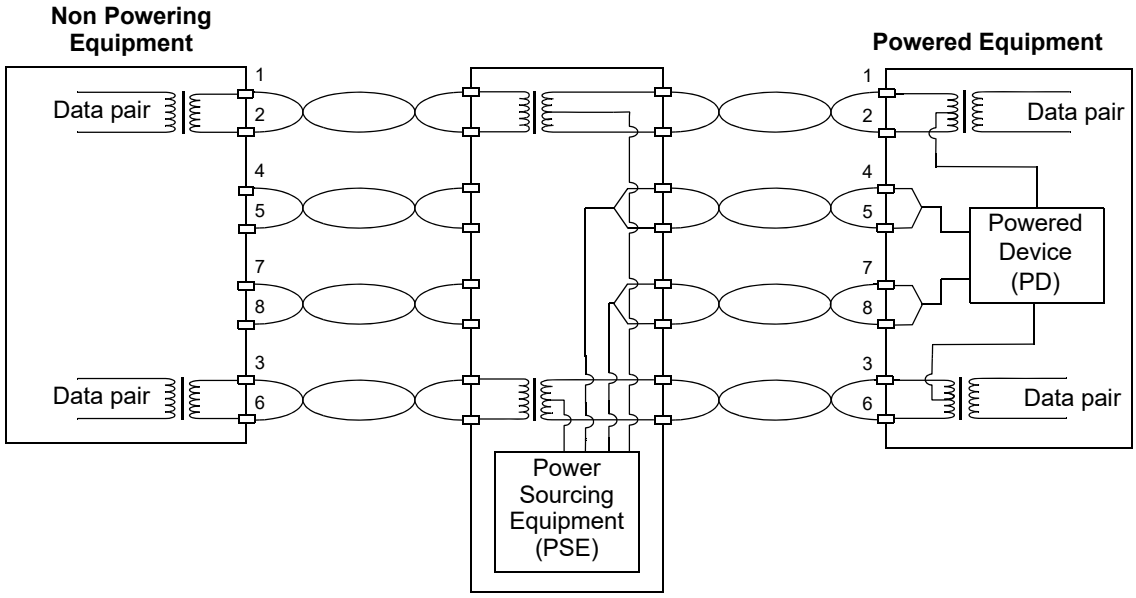

Figure 145–10—10BASE-T/100BASE-TX 4-pair Midspan PSE location overview

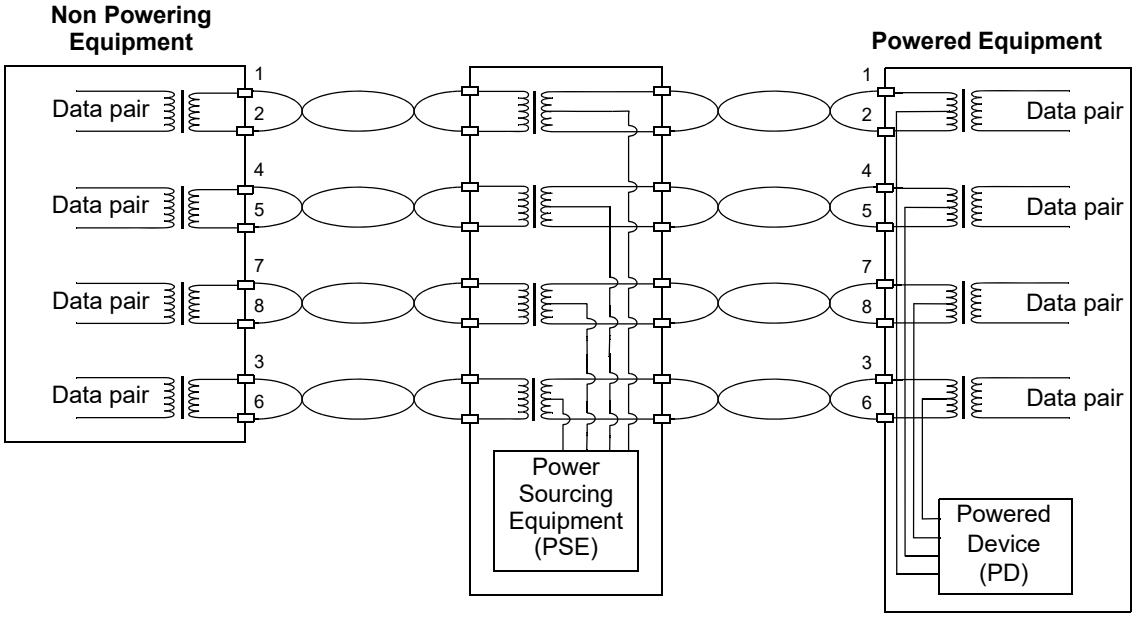

Figure 145–11—1000BASE-T, 2.5G, 5G, or 10GBASE-T 4-pair Midspan PSE location overview

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145.2.4 PSE PI

A PSE device may provide power via one or both of the two valid four-conductor connections, named pairsets. A pairset consists of a pair at the positive V_{PSE} and a pair at the negative V_{PSE}. The two conductors associated with a pair each carry the same nominal current in both magnitude and polarity. Figure 145–12, in conjunction with Table 145–3, illustrates the pairsets, which for PSEs are named Alternative A and Alternative B.

PSEs are required to switch the negative pairs, and may switch the positive pairs as defined in 145.4.1.1. This may lead to both positive pairs providing current in 2-pair mode.

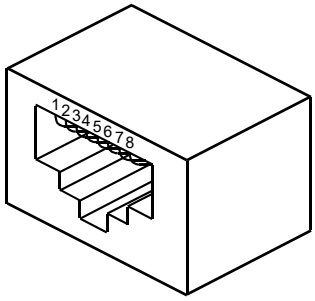

Figure 145–12—PD and PSE eight-pin modular jack

Table 145–3—PSE Pinout Alternatives

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B(X)	Alternative B(S)
1	Negative V_{PSE}	Positive V_{PSE}	—	—
2	Negative V_{PSE}	Positive V_{PSE}	—	—
3	Positive V_{PSE}	Negative V_{PSE}	—	—
4	—	—	Negative V_{PSE}	Positive V_{PSE}
5	—	—	Negative V_{PSE}	Positive V_{PSE}
6	Positive V_{PSE}	Negative V_{PSE}	—	—
7	—	—	Positive V_{PSE}	Negative V_{PSE}
8	—	—	Positive V_{PSE}	Negative V_{PSE}

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PSEs shall use only the permitted polarity configurations associated with Alternative A and Alternative B listed in Table 145–4 corresponding with their Type. For further information on the placement of MDI vs. MDI-X, see 14.5.2.

Table 145–4—Permitted Pinout Alternatives per Type

PSE Type	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B(X)	Alternative B(S)
Type 3	Yes	Yes	Yes	Yes
Type 4	Yes	No	No	Yes

Type 3 PSEs shall implement Alternative A, Alternative B, or both. Type 3 PSEs providing Class 5 or Class 6 power levels and Type 4 PSEs shall implement Alternative A and Alternative B. PSEs may operate simultaneously on both Alternatives, when the requirements of 145.2.9 are met.

The PSE specifications related to current apply on the negative pair or pairs unless otherwise noted.

145.2.5 PSE state diagrams

PSEs shall provide the behavior of the state diagrams shown in Figure 145–13 to Figure 145–18.

145.2.5.1 State diagram overview and timing

If power is to be applied, the PSE turns on power after a valid detection in less than T_{pon} as defined in Table 145–16. If the PSE cannot supply power within T_{pon}, it initiates and successfully completes a new detection cycle before applying power. See 145.2.10.14 for details.

It is possible that two separate PSEs, one that implements Alternative A and one that implements Alternative B (see 145.2.2), may be attached to the same link segment. In such a configuration, and without the required backoff algorithm, the PSEs could prevent each other from ever detecting a PD by interfering with the detection process of the other.

A PSE performing detection using only Alternative B may fail to detect a valid PD detection signature. When this occurs, the PSE shall not apply a voltage greater than V_{Off} to the PI until after at least T_{dbo}, as defined in Table 145–16, has passed before attempting another detection, except in the case of an open circuit as defined in 145.2.6.5. See 145.2.6.5 for more information on Alternative B detection backoff requirements.

If a PSE performing detection using Alternative A detects an invalid detection signature, it should complete a second detection in less than T_{dbo} after the beginning of the first detection attempt. This allows an Alternative A PSE to complete a successful detection cycle prior to an Alternative B PSE present on the same link section that may have caused the invalid detection signature.

Connection check timing requirements are specified in Table 145–10. Detection and power turn-on timing requirements are specified in Table 145–16. Classification timing requirements are specified in Table 145–14. Autoclass timing requirements are specified in Table 145–15.

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In the state diagram, each Alternative serves a distinct role during 4-pair operation. In any implementation, the roles of the Alternatives shall be established in IDLE and be maintained in every other state. In the state diagram, the roles of the Alternatives are named Primary Alternative and Secondary Alternative.

NOTE—During 4-pair operation, it may be necessary to swap the roles of Alternative A and Alternative B in IDLE in order to detect a PD.

The state diagram consists of multiple state diagrams that operate concurrently. Depending on the connected PD being identified as single-signature or dual-signature, the state diagram operates in a different manner. The top level state diagram consists of Figure 145–13.

If the connected PD is identified as dual-signature, the top level state diagram will proceed to SISM_START and remain in that state, at which point the semi-independent state diagrams for the Primary and Secondary Alternative become active. The dual-signature semi-independent state diagram is defined in Figure 145–15 and Figure 145–16 for the Primary and Secondary Alternative respectively.

Monitoring of MPS is described by the state diagrams in Figure 145–17 and Figure 145–18.

145.2.5.2 Conventions

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5. In addition a precedence order for operators is established in Table 145–5. Operators of equal precedence are evaluated left-to-right. Operator precedence in qualifiers is a local convention for this clause.

Table 145–5—State diagram operators in order of precedence (highest to lowest)

Operator	Meaning
( )	Indicates precedence
<, ≤ , >, ≥, =, ≠	Less than, less than or equal to, greater than, greater than or equal to, equals, not equals
!	Boolean NOT
*	Boolean AND
^	Boolean XOR
+	Boolean OR
⇐	Assignment operator

Some states in the state diagrams use an IF-THEN-ELSE-END construct to condition which actions are taken within the state. If the logical expression associated with the IF evaluates TRUE all the actions listed between THEN and ELSE will be executed. In the case where ELSE is omitted, the actions listed between THEN and END will be executed. If the logical expression associated with the IF evaluates FALSE the actions listed between ELSE and END will be executed. After executing the actions listed between THEN and ELSE, between THEN and END, or between ELSE and END, the actions following the END, if any, will be executed.

State diagrams may span over multiple pages. Arcs between states located on a different page within the same state diagram are drawn using a label containing the destination state's name at the originating state. An empty label is used at the destination state to indicate that there exists an entry, or entries, from another state.

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145.2.5.2.1 Alternative designation

Alternative information is obtained by replacing the X in the desired variable or function with the letter of the Alternative of interest. The Alternative is referred to in general as follows:

X
: Generic Alternative designator. When X is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams.
Values:
A: Alternative A
B: Alternative B

NOTE—The variables alt_pri and alt_sec map Alternatives to Primary and Secondary.

145.2.5.3 Constants

CC_DET_SEQ
: A constant indicating the sequence in which the PSE performs connection check and detection. See Annex 145B for timing diagrams.
Values:
0: Connection check is followed by staggered detection for a single-signature PD and parallel or staggered detection for a dual-signature PD.
1: Detection on a pairset is followed by connection check and then detection on the other pairset for a single-signature PD and parallel or staggered (starting with first pairset) detection for a dual-signature PD.
2: Connection check and detection on both pairsets are performed within a single T_{det} window.
3: Connection check is followed by staggered detection.

Parallel detection refers to detection on both pairsets being performed in the same T_{det} time period. Staggered detection refers to detection on both pairsets being performed in a different T_{det} cycle.

145.2.5.4 Variables

ac_measurement_completed
: A variable that indicates that an Autoclass measurement has been completed. This variable is set by the state diagram.
Values:
FALSE: The Autoclass measurement has not completed.
TRUE: An Autoclass measurement has been completed.

alt_done_pri
: A variable used to coordinate the main single-signature state diagram with the semi-independent dual-signature state diagram for the Primary Alternative.
Values:
FALSE: The semi-independent state diagram is not ready to return to IDLE within the single-signature state diagram.
TRUE: The semi-independent state diagram is ready to return to IDLE within the single-signature state diagram.

alt_done_sec
: A variable used to coordinate the main single-signature state diagram with the semi-independent dual-signature state diagram for the Secondary Alternative.
Values:
FALSE: The semi-independent state diagram is not ready to return to IDLE within the single-signature state diagram.

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TRUE: The semi-independent state diagram is ready to return to IDLE within the single-signature state diagram.

alt_pri

A variable used to select which Alternative assumes the role of Primary Alternative in the state diagram.

Values:

a: Alternative A assumes the role of Primary Alternative. When operating over 4 pairs, Alternative B assumes the role of Secondary Alternative.

b: Alternative B assumes the role of Primary Alternative. When operating over 4 pairs, Alternative A assumes the role of Secondary Alternative.

alt_pwrd_pri

A variable that controls the circuitry that the PSE uses to power the PD over the Alternative that has been assigned as Primary.

Values:

FALSE: The circuitry that applies operating voltage to the Primary Alternative is disabled.

TRUE: The circuitry that applies operating voltage to the Primary Alternative is enabled.

alt_pwrd_sec

A variable that controls the circuitry that the PSE uses to power the PD over the Alternative that has been assigned as Secondary.

Values:

FALSE: The circuitry that applies operating voltage to the Secondary Alternative is disabled.

TRUE: The circuitry that applies operating voltage to the Secondary Alternative is enabled.

autoclass_enable

A variable indicating that the PSE is enabled to check if the PD is requesting Autoclass via Physical Layer classification; see 145.2.8.2 and 145.3.6.2.

Values:

FALSE: Autoclass is disabled in the PSE.

TRUE: Autoclass is enabled in the PSE.

class_4PID_mult_events_pri

A variable indicating if the PSE generates 3 class events on the Primary Alternative to determine if a dual-signature PD is a candidate for 4-pair power.

Values:

FALSE: The PSE does not need to generate 3 class events to determine if the PD is a candidate for 4-pair power.

TRUE: The PSE generates at least 3 class events to determine if the PD is a candidate for 4-pair power.

class_4PID_mult_events_sec

A variable indicating if the PSE generates 3 class events on the Secondary Alternative to determine if a dual-signature PD is a candidate for 4-pair power.

Values:

FALSE: The PSE does not need to generate 3 class events to determine if the PD is a candidate for 4-pair power.

TRUE: The PSE generates at least 3 class events to determine if the PD is a candidate for 4-pair power.

det_once_sec

This variable indicates if the PSE has probed the Secondary Alternative at least once following exit from ENTRY_SEC.

Values:

FALSE: The PSE has not probed the Secondary Alternative since entering the Secondary Alternative state diagram.

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TRUE: The PSE has probed the Secondary Alternative at least once since entering the Secondary Alternative state diagram.

det_start_pri

A variable that indicates to the Secondary Alternative that the Primary Alternative is between START_DETECT and POWER_UP.

Values:

FALSE: The Primary Alternative is not between START_DETECT and POWER_UP.
TRUE: The Primary Alternative is between START_DETECT and POWER_UP.

det_start_sec

A variable that indicates to the Primary Alternative that the Secondary Alternative is between START_DETECT and POWER_UP.

Values:

FALSE: The Secondary Alternative is not between START_DETECT and POWER_UP.
TRUE: The Secondary Alternative is between START_DETECT and POWER_UP.

det_temp

A variable that indicates whether a 4-pair PSE has completed detection on one and only one Alternative or if the PSE has completed detection on neither or both Alternatives.

Values:

both_neither: The PSE has completed detection on both Alternatives or neither Alternatives.
only_one: The PSE has completed detection on only one Alternative.

error_condition

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 145–16 and that require the PSE not to source power. This variable may be set by the PSE at any time.

Values:

FALSE: No fault indication.
TRUE: A fault indication exists.

error_condition_pri

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 145–16 and that require the PSE not to source power over the Primary Alternative. This variable may be set by the PSE at any time.

Values:

FALSE: No fault indication.
TRUE: A fault indication exists.

error_condition_sec

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 145–16 and that require the PSE not to source power over the Secondary Alternative. This variable may be set by the PSE at any time.

Values:

FALSE: No fault indication.
TRUE: A fault indication exists.

error_pri

Alias for the following terms: short_det_pri + ovld_det_pri + option_vport_lim_pri.

error_sec

Alias for the following terms: short_det_sec + ovld_det_sec + option_vport_lim_sec.

iclass_lim_det

A variable indicating if any I_{Class} measured by the PSE during do_classification is invalid or equal to or greater than I_{Class_LIM} min as defined in Table 145–14. This variable is set per this description.

Values:

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FALSE: Measured I_{Class} is not invalid or is less than I_{Class_LIM} min during do_classification or this function is not active.

TRUE: Measured I_{Class} is invalid or equal to or greater than I_{Class_LIM} min during do_classification.

iclass_lim_det_pri

A variable indicating if any I_{Class} measured by the PSE over the Primary Alternative during do_classification_pri is invalid or equal to or greater than I_{Class_LIM} min as defined in Table 145–14. This variable is set per this description.

Values:

FALSE: Measured I_{Class} over the Primary Alternative is not invalid or is less than I_{Class_LIM} min during do_classification_pri or this function is not active.

TRUE: Measured I_{Class} over the Primary Alternative is invalid or equal to or greater than I_{Class_LIM} min during do_classification_pri.

iclass_lim_det_sec

A variable indicating if any I_{Class} measured by the PSE over the Secondary Alternative during do_classification_sec is invalid or equal to or greater than I_{Class_LIM} min as defined in Table 145–14. This variable is set per this description.

Values:

FALSE: Measured I_{Class} over the Secondary Alternative is not invalid or is less than I_{Class_LIM} min during do_classification_sec or this function is not active.

TRUE: Measured I_{Class} over the Secondary Alternative is invalid or equal to or greater than I_{Class_LIM} min during do_classification_sec.

MirroredPDAutoclassRequest

The copy of the ‘PD Autoclass request’ field in the Power via MDI TLV that the PSE receives from the remote system. This variable is mapped from aLldpXdot3RemAutoclassRequest (30.12.3.1.35) and assigned through Table 145–38.

Values:

FALSE: The PSE has not received an Autoclass measurement request from PD.

TRUE: The PSE has received an Autoclass measurement request from PD.

mps_valid

The PSE monitors the Maintain Power Signature (MPS, see 145.2.12). This variable indicates the presence or absence of a valid MPS, when the connected PD is a single-signature PD, or the PSE is operating in 2-pair mode. This variable is set per this description.

Values:

FALSE: MPS is absent.

TRUE: MPS is present.

mps_valid_pri

The PSE monitors the Maintain Power Signature (MPS, see 145.2.12) on the Primary Alternative. This variable indicates the presence or absence of a valid MPS on the Primary Alternative, when the connected PD is a dual-signature PD. This variable is set per this description.

Values:

FALSE: MPS is absent.

TRUE: MPS is present.

mps_valid_sec

The PSE monitors the Maintain Power Signature (MPS, see 145.2.12) on the Secondary Alternative. This variable indicates the presence or absence of a valid MPS on the Secondary Alternative, when the connected PD is a dual-signature PD. This variable is set per this description.

Values:

FALSE: MPS is absent.

TRUE: MPS is present.

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option_2ev

This variable indicates if PSE will generate 2 or 3 class events when pse_avail_pwr is 4.

Values:

FALSE: The PSE is not restricted to 2 class events when pse_avail_pwr is 4.

TRUE: The PSE is restricted to 2 class events when pse_avail_pwr is 4.

option_class_probe

This variable indicates if the PSE should determine the PD requested Class via the do_class_probe function. When set to TRUE, the PSE will issue 3 class events to determine the PD requested Class, perform a classification reset by applying V_{Reset} for at least T_{Reset} to the PI (see Table 145–14), followed by a normal classification procedure.

Values:

FALSE: The PSE will not probe for the PD requested Class.

TRUE: The PSE probes for the PD requested Class.

option_class_probe_pri

This variable indicates if the PSE should determine the PD requested Class on the Primary Alternative via the do_class_probe_pri function. When set to TRUE, the PSE will issue 3 class events to determine the PD requested Class, perform a classification reset by applying V_{Reset} for at least T_{Reset} to the Primary Alternative (see Table 145–14).

Values:

FALSE: The PSE will not probe for the PD requested Class.

TRUE: The PSE probes for the PD requested Class.

option_class_probe_sec

This variable indicates if the PSE should determine the PD requested Class on the Secondary Alternative via the do_class_probe_sec function. When set to TRUE, the PSE will issue 3 class events to determine the PD requested Class, perform a classification reset by applying V_{Reset} for at least T_{Reset} to the Secondary Alternative (see Table 145–14).

Values:

FALSE: The PSE will not probe for the PD requested Class.

TRUE: The PSE probes for the PD requested Class.

option_detect_ted

This variable indicates if detection can be performed by the PSE during the ted_timer interval.

Values:

FALSE: Do not perform detection during ted_timer interval.

TRUE: Perform detection during ted_timer interval.

option_detect_ted_pri

This variable indicates if detection can be performed by the PSE on the Primary Alternative during the ted_timer_pri interval.

Values:

FALSE: Do not perform detection during ted_timer_pri interval.

TRUE: Perform detection during ted_timer_pri interval.

option_detect_ted_sec

This variable indicates if detection can be performed by the PSE on the Secondary Alternative during the ted_timer_sec interval.

Values:

FALSE: Do not perform detection during ted_timer_sec interval.

TRUE: Perform detection during ted_timer_sec interval.

option_MEC_after_probe

This variable indicates if Multiple-Event classification is allowed after a class probe in the dual-signature state diagrams.

Values:

FALSE: Only allow Single-Event classification after class probe.

TRUE: Allow Multiple-Event classification after class probe.

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option_probe_alt_sec

This variable indicates if the PSE will continue to detect and conditionally perform Physical Layer classification on the Secondary Alternative in the event power is not applied to the Primary Alternative.

Values:

FALSE: PSE does not probe the Secondary Alternative if power is not applied to the Primary Alternative.

TRUE: PSE does probe the Secondary Alternative if power is not applied to the Primary Alternative.

option_vport_lim_pri

This variable indicates if V_{PSE} on the Primary Alternative is out of the operating range during normal operating state. This variable is set per this description.

Values:

FALSE: V_{PSE} on the Primary Alternative is within the $V_{Port\_PSE\text{-}2P}$ operating range as defined in Table 145–16 or the PSE does not implement this option.

TRUE: V_{PSE} on the Primary Alternative is outside of the $V_{Port\_PSE\text{-}2P}$ operating range as defined in Table 145–16.

option_vport_lim_sec

This variable indicates if V_{PSE} on the Secondary Alternative is out of the operating range during normal operating state. This variable is set per this description.

Values:

FALSE: V_{PSE} on the Secondary Alternative is within the $V_{Port\_PSE\text{-}2P}$ operating range as defined in Table 145–16 or the PSE does not implement this option.

TRUE: V_{PSE} on the Secondary Alternative is outside of the $V_{Port\_PSE\text{-}2P}$ operating range as defined in Table 145–16.

ovld_det_pri

A variable indicating if the PSE output current has been in an overload condition on the Primary Alternative; see 145.2.10.8. This variable is set per this description.

Values:

FALSE: The PSE has not detected an overload condition on the Primary Alternative.

TRUE: The PSE has detected an overload condition on the Primary Alternative.

ovld_det_sec

A variable indicating if the PSE output current has been in an overload condition on the Secondary Alternative; see 145.2.10.8. This variable is set per this description.

Values:

FALSE: The PSE has not detected an overload condition on the Secondary Alternative.

TRUE: The PSE has detected an overload condition on the Secondary Alternative.

pd_4pair_cand

This variable is used by the PSE to indicate that a connected PD is a candidate to receive power on both Modes. This variable is a function of the results of detection, connection check, Physical Layer classification, and PD 4PID; see 145.2.9.

Values:

FALSE: The PD is not a candidate to receive power on both Modes.

TRUE: The PD is a candidate to receive power on both Modes.

pd_autoclass_cancelled

A variable that indicates whether the PD cancelled Autoclass by drawing less than Class 1 power during the Autoclass measurement period.

Values:

FALSE: The PD did not cancel Autoclass or did not request Autoclass.

TRUE: The PD requested Physical Layer Autoclass and cancelled.

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pd_cls_4PID_pri

This variable indicates that the Type of the dual-signature PD has been established on the Primary Alternative by Physical Layer classification.

Values:

FALSE: The PD is not a candidate for 4-pair power or the PSE has not used Physical Layer classification to determine the PD Type.

TRUE: The PD is a candidate for 4-pair power and has been identified as a Type 3 or Type 4 PD, see Table 145–27.

pd_cls_4PID_sec

This variable indicates that the Type of the dual-signature PD has been established on the Secondary Alternative by Physical Layer classification.

Values:

FALSE: The PD is not a candidate for 4-pair power or the PSE has not used Physical Layer classification to determine the PD Type.

TRUE: The PD is a candidate for 4-pair power and has been identified as a Type 3 or Type 4 PD, see Table 145–27.

pd_req_pwr

The variable indicates the PD requested Class. When a PD requests a higher Class than a PSE can support, the PSE assigns the PD to Class 3, Class 4, or Class 6, whichever is the highest Class it can support. If pse_avail_pwr is less than 4 and option_class_probe is FALSE, this variable may not contain the PD requested Class; do_class_probe also returns this variable.

Values:

0: Class 0
1: Class 1
2: Class 2
3: Class 3
4: Class 4
5: Class 5
6: Class 6
7: Class 7
8: Class 8

power_available

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power to support the attached PD. Sufficient power is defined by classification; see 145.2.8. This variable may be set by the PSE at any time.

Values:

FALSE: PSE is no longer capable of sourcing power to a PD.

TRUE: PSE is capable to continue to source power to a PD.

power_available_pri

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power on the Primary Alternative to support the attached PD. Sufficient power is defined by classification; see 145.2.8. This variable may be set by the PSE at any time.

Values:

FALSE: PSE is no longer capable of sourcing power on the Primary Alternative.

TRUE: PSE is capable to continue to source power on the Primary Alternative.

power_available_sec

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power on the Secondary Alternative to support the attached PD. Sufficient power is defined by classification; see 145.2.8. This variable may be set by the PSE at any time.

Values:

FALSE: PSE is no longer capable of sourcing power on the Secondary Alternative.

TRUE: PSE is capable to continue to source power on the Secondary Alternative.

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pse_allocated_pwr

A variable that indicates the Class that has been assigned to the PD.

Values:

- 0: No power has been assigned to the PD
- 1: Class 1
- 2: Class 2
- 3: Class 3
- 4: Class 4
- 5: Class 5
- 6: Class 6
- 7: Class 7
- 8: Class 8

pse_alternative

This variable indicates which Pinout Alternative the PSE uses to apply power to the PI (see Table 145–3).

Values:

- a: The PSE uses PSE pinout Alternative A.
- b: The PSE uses PSE pinout Alternative B.
- both: The PSE uses both Alternative A and Alternative B.

pse_avail_pwr

This variable indicates the highest Class the PSE may assign to the PD by Physical Layer classification. The value is restricted to the allowed range defined in Table 145–6 and set in an implementation-specific manner.

Values:

- 1: Class 1
- 2: Class 2
- 3: Class 3
- 4: Class 4
- 5: Class 5
- 6: Class 6
- 7: Class 7
- 8: Class 8

pse_avail_pwr_pri

This variable indicates the highest Class the PSE may assign to the PD by Physical Layer classification on the Primary Alternative. The value is restricted to the allowed range defined in Table 145–6 and set in an implementation-specific manner.

Values:

- 1: Class 1
- 2: Class 2
- 3: Class 3
- 4: Class 4
- 5: Class 5

pse_avail_pwr_sec

This variable indicates the highest Class the PSE may assign to the PD by Physical Layer classification on the Secondary Alternative. The value is restricted to the allowed range defined in Table 145–6 and set in an implementation-specific manner.

Values:

- 1: Class 1
- 2: Class 2
- 3: Class 3
- 4: Class 4
- 5: Class 5

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pse_dll_capable

This variable indicates whether the PSE is capable of performing optional Data Link Layer classification. See 145.5 for a description of Data Link Layer functionality. A variable that is set in an implementation-dependent manner.

Values:

FALSE: The PSE's Data Link Layer classification capability is not enabled.
TRUE: The PSE's Data Link Layer classification capability is enabled.

pse_dll_enable

A variable indicating whether the Data Link Layer classification mechanism is enabled. See 145.5.

Values:

FALSE: Data Link Layer classification is not enabled.
TRUE: Data Link Layer classification is enabled.

pse_dll_ready

An implementation-specific variable that indicates that the PSE has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.61). This variable may be set by the PSE at any time.

Values:

FALSE: Data Link Layer classification has not completed initialization.
TRUE: Data Link Layer classification has completed initialization.

pse_enable

A variable that selects PSE operation. This variable may be set by the PSE at any time.

Values:

disable: All PSE functions disabled (behavior is as if there was no PSE functionality).
enable: Normal PSE operation.

pse_power_update

A variable that is set when the PSEAllocatedPowerValue in the DLL state diagram in Figure 145–40 has been updated. This variable may be set by the PSE at any time.

Values:

FALSE: The value of PSEAllocatedPowerValue has not changed.
TRUE: The value of PSEAllocatedPowerValue has changed.

pse_power_update_pri

A variable that is set when the PSEAllocatedPowerValue_alt(X) in the DLL state diagram in Figure 145–42 or Figure 145–43 has been updated, where X is the Primary Alternative. This variable may be set by the PSE at any time.

Values:

FALSE: The value of PSEAllocatedPowerValue_alt(X) has not changed.
TRUE: The value of PSEAllocatedPowerValue_alt(X) has changed.

pse_power_update_sec

A variable that is set when the PSEAllocatedPowerValue_alt(X) in the DLL state diagram in Figure 145–42 or Figure 145–43 has been updated, where X is the Secondary Alternative. This variable may be set by the PSE at any time.

Values:

FALSE: The value of PSEAllocatedPowerValue_alt(X) has not changed.
TRUE: The value of PSEAllocatedPowerValue_alt(X) has changed.

pse_ready

Variable that is asserted in an implementation-dependent manner to probe the link segment. This variable may be set by the PSE at any time.

Values:

FALSE: PSE is not ready to probe the link segment.
TRUE: PSE is ready to probe the link segment.

NOTE—Care should be taken when negating this variable in a PSE performing detection using Alternative A after an invalid detection signature is detected due to the delay it introduces between detection attempts (see 145.2.5.1).

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pse_ready_pri

Variable that is asserted in an implementation-dependent manner to probe the Primary Alternative. This variable may be set by the PSE at any time.

Values:

FALSE: PSE is not ready to probe the primary link segment.
TRUE: PSE is ready to probe the primary link segment.

pse_ready_sec

Variable that is asserted in an implementation-dependent manner to probe the Secondary Alternative. This variable may be set by the PSE at any time.

Values:

FALSE: PSE is not ready to probe the secondary link segment.
TRUE: PSE is ready to probe the secondary link segment.

pse_reset

Controls the resetting of the PSE state diagram. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE functionality. This variable is set per this description.

Values:

FALSE: Do not reset the PSE state diagram.
TRUE: Reset the PSE state diagram.

pse_reset_pri

Controls the resetting of the PSE state diagram on Primary Alternative. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE Primary Alternative functionality. This variable is set per this description.

Values:

FALSE: Do not reset the PSE state diagram.
TRUE: Reset the PSE state diagram.

pse_reset_sec

Controls the resetting of the PSE state diagram on Secondary Alternative. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE Secondary Alternative functionality. This variable is set per this description.

Values:

FALSE: Do not reset the PSE state diagram.
TRUE: Reset the PSE state diagram.

pse_ss_mode

A variable that controls whether the PSE provides power over 2 pair or 4 pair to a single-signature PD assigned to Class 1 through Class 4. This variable may be set by the PSE at any time.

0: Single-signature PD is powered over 2 pair.
1: Single-signature PD is powered over 4 pair.

pse_ss_mode_update

A variable that is used to cause the PSE to re-evaluate the value of pse_ss_mode when it is in POWER_ON. This variable may be set by the PSE at any time.

Values:

FALSE: pse_ss_mode is not re-evaluated.
TRUE: pse_ss_mode will be re-evaluated.

pwr_app_pri

A variable indicating that the PSE has begun steady state operation on the Primary Alternative by having asserted alt_pwrd_pri, completed the ramp up of voltage, is not in a current limiting mode, and is operating beyond the POWER_UP requirements of 145.2.10.7. This variable is set per this description.

Values:

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FALSE: The PSE is either not applying power or has begun applying power but is still in POWER_UP on the Primary Alternative.
TRUE: The PSE has begun steady state operation on the Primary Alternative.

pwr_app_sec

A variable indicating that the PSE has begun steady state operation on the Secondary Alternative by having asserted alt_pwrd_sec, completed the ramp up of voltage, is not in a current limiting mode, and is operating beyond the POWER_UP requirements of 145.2.10.7. This variable is set per this description.

Values:

FALSE: The PSE is either not applying power or has begun applying power but is still in POWER_UP on the Secondary Alternative.
TRUE: The PSE has begun steady state operation on the Secondary Alternative.

semi_pwr_en

A variable indicating if, in the case of a single-signature PD, the PSE uses the method consisting of turning off only the pairset on which a short-circuit, overload or out of range V_{PSE} is detected.

Values:

TRUE: Only the pairset with the fault condition is turned off.
FALSE: Both pairsets are turned off if there is a fault on one pairset.

short_det_pri

A variable indicating if the PSE output current has been in a short circuit condition on the Primary Alternative. This variable is set per this description. See 145.2.10.9.

Values:

FALSE: The PSE has not detected a short circuit condition on the Primary Alternative.
TRUE: The PSE has detected a short circuit condition on the Primary Alternative.

short_det_sec

A variable indicating if the PSE output current has been in a short circuit condition on the Secondary Alternative. This variable is set per this description. See 145.2.10.9.

Values:

FALSE: The PSE has not detected a short circuit condition on the Secondary Alternative.
TRUE: The PSE has detected a short circuit condition on the Secondary Alternative.

sism

A variable used by the single-signature state diagram to initiate the semi-independent dual-signature state diagrams.

Values:

FALSE: Single-signature state diagram has control of the Alternatives.
TRUE: Single-signature state diagram has passed control of the Alternatives to the semi-independent dual-signature state diagrams.

temp_var

A variable used to store the previous value of the variable pd_class_sig.

temp_var_pri

A variable used to store the previous value of the variable pd_class_sig_pri for the Primary Alternative.

temp_var_sec

A variable used to store the previous value of the variable pd_class_sig_sec for the Secondary Alternative.

PSEs shall set pse_avail_pwr, pse_avail_pwr_pri, and pse_avail_pwr_sec from the range in Table 145–6.

145.2.5.5 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops counting upon entering a state where “stop *x*_timer” is asserted.

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Table 145–6—Allowed Type 3 and Type 4 PSE permutations for pse_avail_pwr

PSE Type	pse_avail_pwr	pse_avail_pwr_pri, pse_avail_pwr_sec
Type 3	1 to 6	1 to 4
Type 4	1 to 8	1 to 5

tauto_pse1_timer
: A timer used to delay Autoclass power measurement following transition into POWER_ON; see T_{AUTO_PSE1} in Table 145–15.

tauto_pse2_timer
: A timer used to limit Autoclass power measurement following transition into POWER_ON; see T_{AUTO_PSE2} in Table 145–15.

tcc2det_timer
: A timer used to limit the time between connection check and detection when CC_DET_SEQ = 0 or CC_DET_SEQ = 3. See T_{cc2det} in Table 145–10.

tcev_timer
: A timer used to limit the second through fifth class event time in Multiple-Event classification; see T_{CEV} in Table 145–14.

tcev_timer_pri
: A timer used to limit the second through fourth class event time in Multiple-Event classification on the Primary Alternative; see T_{CEV} in Table 145–14.

tcev_timer_sec
: A timer used to limit the second through fourth class event time in Multiple-Event classification on the Secondary Alternative; see T_{CEV} in Table 145–14.

tclass_acs_timer
: A timer used to indicate when the PSE may measure the class current during the first long class event, to check if the PD is requesting Autoclass. See T_{Class_ACS} in Table 145–14.

tclass_reset_timer
: A timer used to limit the classification reset time; See T_{Reset} in Table 145–14.

tclass_reset_timer_pri
: A timer used to limit the classification reset time on the Primary Alternative; see T_{Reset} in Table 145–14.

tclass_reset_timer_sec
: A timer used to limit the classification reset time on the Secondary Alternative; see T_{Reset} in Table 145–14.

tdbo_timer
: A timer used to regulate backoff upon detection of an invalid detection signature; see T_{dbo} in Table 145–16.

tdet_timer
: A timer used to limit an attempt to detect a PD; see T_{det} in Table 145–16.

tdet_timer_pri
: A timer used to limit an attempt to detect a PD on the Primary Alternative; see T_{det} in Table 145–16.

tdet_timer_sec
: A timer used to limit an attempt to detect a PD on the Secondary Alternative; see T_{det} in Table 145–16.

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tdet2det_timer
: A timer used to limit the time between the completion of a detection on one pairset and the beginning of a detection on the other; see $T_{det2det}$ in Table 145–10.

ted_timer
: A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal; see T_{ed} in Table 145–16. The default state of this timer is ted_timer_done.

ted_timer_pri
: A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal from the Primary Alternative; see T_{ed} in Table 145–16. The default state of this timer is ted_timer_pri_done.

ted_timer_sec
: A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal from the Secondary Alternative; see T_{ed} in Table 145–16. The default state of this timer is ted_timer_sec_done.

tinrush_timer_pri
: A timer used to monitor the duration of the inrush event on the Primary Alternative; see T_{Inrush} in Table 145–16.

tinrush_timer_sec
: A timer used to monitor the duration of the inrush event on the Secondary Alternative; see T_{Inrush} in Table 145–16.

tlce_timer
: A timer used to limit the first class event time in Multiple-Event classification; see T_{LCE} in Table 145–14.

tlce_timer_pri
: A timer used to limit the first class event time in Multiple-Event classification on the Primary Alternative; see T_{LCE} in Table 145–14.

tlce_timer_sec
: A timer used to limit the first class event time in Multiple-Event classification on the Secondary Alternative; see T_{LCE} in Table 145–14.

tme1_timer
: A timer used to limit mark event times for all but the last mark event time during Multiple-Event classification; see T_{ME1} in Table 145–14.

tme1_timer_pri
: A timer used to limit mark event times for all but the last mark event time during Multiple-Event classification on the Primary Alternative; see T_{ME1} in Table 145–14.

tme1_timer_sec
: A timer used to limit mark event times for all but the last mark event time during Multiple-Event classification on the Secondary Alternative; see T_{ME1} in Table 145–14.

tme2_timer
: A timer used to limit the final mark event time in Multiple-Event classification; see T_{ME2} in Table 145–14.

tme2_timer_pri
: A timer used to limit the final mark event time in Multiple-Event classification on the Primary Alternative; see T_{ME2} in Table 145–14.

tme2_timer_sec
: A timer used to limit the final mark event time in Multiple-Event classification on the Secondary Alternative; see T_{ME2} in Table 145–14

tmpdo_timer
: A timer used to monitor the dropout of the MPS; see T_{MPDO} in Table 145–16.

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tmpdo_timer_pri
: A timer used to monitor the dropout of the MPS on the Primary Alternative; see T_{MPDO} in Table 145–16.

tmpdo_timer_sec
: A timer used to monitor the dropout of the MPS on the Secondary Alternative; see T_{MPDO} in Table 145–16.

tpon_timer
: A timer used to limit the time for power turn-on; see T_{pon} in Table 145–16.

tpon_timer_pri
: A timer used to limit the time on the Primary Alternative for power turn-on; see T_{pon} in Table 145–16.

tpon_timer_sec
: A timer used to limit the time on the Secondary Alternative for power turn-on; see T_{pon} in Table 145–16.

145.2.5.6 Functions

The variable formed by the function name appended with "_done" is used to indicate when the function has completed. This variable is set to FALSE when the function is called and is set to TRUE once the function is complete and its output variables are valid.

do_autoclass_measure
: This function measures $P_{Autoclass}$ as defined in 145.2.8.2. This function returns the following variable:

  $P_{Autoclass}$: The power measured by the PSE during Physical Layer classification as defined in 145.2.8.2.

do_autoclassification
: This function returns the following variable:

  pd_autoclass: This variable indicates whether the PD requests Autoclass during Physical Layer classification. pd_autoclass is set to True when a class signature of '0' is detected during the T_{Class_ACS} window, as defined in Table 145–14, otherwise it is set to False.
  Values:
  FALSE: The PD does not request Autoclass.
  TRUE: The PD requests Autoclass.

do_class_probe
: This function discovers the PD requested Class by producing a number of class events. The class events produced are limited to CLASS_EV1_LCE to MARK_EV3. The tlce_timer in CLASS_EV1_LCE may be replaced with the tcev_timer to allow abbreviated class timing duration. This function returns the following variable:

  pd_req_pwr: See pd_req_pwr in 145.2.5.4.

do_class_probe_pri
: This function discovers the PD requested Class by producing a number of class events on the Primary Alternative. The class events produced are limited to CLASS_EV1_LCE_PRI to MARK_EV3_PRI. The tlce_timer_pri in CLASS_EV1_LCE_PRI may be replaced with the tcev_timer_pri to allow abbreviated class timing duration. This function returns the following variables:

  pd_req_pwr_pri: See do_classification_pri function.
  pd_cls_4PID_pri: See pd_cls_4PID_pri in 145.2.5.4.

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do_class_probe_sec

This function discovers the PD requested Class by producing a number of class events on the Secondary Alternative. The class events produced are limited to CLASS_EV1_LCE_SEC to MARK_EV3_SEC. The tlce_timer_sec in CLASS_EV1_LCE_SEC may be replaced with the tcev_timer_sec to allow abbreviated class timing duration. This function returns the following variables:

pd_req_pwr_sec: See do_classification_sec function.
pd_cls_4PID_sec: See pd_cls_4PID_sec in 145.2.5.4.

do_class_reset

This function produces the classification reset voltage; See V_{Reset} in Table 145–14. This function does not return any variables.

do_class_reset_pri

This function produces the classification reset voltage on the Primary Alternative; See V_{Reset} in Table 145–14. This function does not return any variables.

do_class_reset_sec

This function produces the classification reset voltage on the Secondary Alternative; See V_{Reset} in Table 145–14. This function does not return any variables.

do_classification

This function produces the classification event voltage and determines the PD's class signature. This function returns the following variable:

pd_class_sig: The PD class signature seen on the negative pair or pairs during the most recent class event; see Table 145–13 and 145.2.8.
Values:

0: class signature 0
1: class signature 1
2: class signature 2
3: class signature 3
4: class signature 4

do_classification_pri

This function produces the classification event voltage and determines the PD's class signature for the Primary Alternative. This function returns the following variables for the Primary Alternative:

pd_req_pwr_pri: This variable indicates the PD requested Class. When a PD requests a higher Class than a PSE can support, the PSE assigns the PD Class 3 or 4, whichever is the highest that it can support. See 145.2.8. The returned value is based on all previous do_classification_pri function calls since the last time in DETECT_EVAL_PRI or CLASS_RESET_PRI. See Table 145–27 for a determination of the PD requested Class.
Values:

1: Class 1
2: Class 2
3: Class 3
4: Class 4
5: Class 5

pse_allocated_pwr_pri: This variable indicates the Class assigned to the PD for the Primary Alternative. The returned value is based on all previous do_classification_pri function calls since the last time in DETECT_EVAL_PRI or CLASS_RESET_PRI. See Table 145–11 for a determination of the PSE assigned Class.
Values:

1: Class 1
2: Class 2
3: Class 3

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4: Class 4
5: Class 5

pd_class_sig_pri: The PD class signature seen on the negative pair associated with the Primary Alternative during the most recent class event; see Table 145–13 and 145.2.8.
Values:
0: class signature 0
1: class signature 1
2: class signature 2
3: class signature 3
4: class signature 4

do_classification_sec

This function produces the classification event voltage and determines the PD's class signature for the Secondary Alternative. This function returns the following variables for the Secondary Alternative:

pd_req_pwr_sec: This variable indicates the PD requested Class. When a PD requests a higher Class than a PSE can support, the PSE assigns the PD Class 3 or 4, whichever is the highest that it can support. See 145.2.8. The returned value is based on all previous do_classification_sec function calls since the last time in DETECT_EVAL_SEC or CLASS_RESET_SEC. See Table 145–27 for a determination of the PD requested Class.
Values:
1: Class 1
2: Class 2
3: Class 3
4: Class 4
5: Class 5

pse_allocated_pwr_sec: This variable indicates the Class assigned to the PD for the Secondary Alternative. The returned value is based on all previous do_classification_sec function calls since the last time in DETECT_EVAL_SEC or CLASS_RESET_SEC. See Table 145–11 for a determination of the PSE assigned Class.
Values:
1: Class 1
2: Class 2
3: Class 3
4: Class 4
5: Class 5

pd_class_sig_sec: The PD class signature seen on the negative pair associated with the Secondary Alternative during the most recent class event; see Table 145–13 and 145.2.8.
Values:
0: class signature 0
1: class signature 1
2: class signature 2
3: class signature 3
4: class signature 4

do_cxn_chk

This function initiates the connection check as defined in 145.2.7. This function returns the following variable:

sig_type: This variable indicates the PD signature configuration connected to the PI, with respect to 4-pair operation.
Values:

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invalid: Neither a single-signature nor a dual-signature configuration has been found. This includes an open circuit condition on either pairset.
single: The PSE has determined there is a single-signature PD configuration connected to the PI.
dual: The PSE has determined there is a dual-signature PD configuration connected to the PI.

do_detect_pri

This function returns the following variables (see 145.2.6):

sig_pri: This variable indicates the presence or absence of a valid PD detection signature on the Primary Alternative.
Values:
open_circuit: The PSE has detected an open circuit.
valid: The PSE has detected a valid PD detection signature.
invalid: Neither an open circuit nor a valid PD detection signature has been found.

do_detect_sec

This function returns the following variables (see 145.2.6):

sig_sec: This variable indicates the presence or absence of a valid PD detection signature on the Secondary Alternative.
Values:
open_circuit: The PSE has detected an open circuit.
valid: The PSE has detected a valid PD detection signature.
invalid: Neither an open circuit nor a valid PD detection signature has been found.

do_initialize

This function returns the following variables (see 145.2.5.4):

alt_pri
autoclass_enable
class_4PID_mult_events_pri
class_4PID_mult_events_sec
option_2ev
option_class_probe
option_class_probe_pri
option_class_probe_sec
option_detect_ted
option_detect_ted_pri
option_detect_ted_sec
option_MEC_after_probe
option_probe_alt_sec
pse_alternative
pse_avail_pwr
pse_avail_pwr_pri
pse_avail_pwr_sec
pse_dll_capable
semi_pwr_en

do_mark

This function produces the classification mark event voltage. This function does not return any variables.

do_mark_pri

This function produces the classification mark event voltage on the Primary Alternative. This function does not return any variables.

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do_mark_sec

This function produces the classification mark event voltage on the Secondary Alternative. This function does not return any variables.

do_update_pse_allocated_pwr

A function that updates the pse_allocated_pwr based on the value of PSEAllocatedPowerValue as defined in Table 145–12. This function returns the following variable:

pse_allocated_pwr: See pse_allocated_pwr in 145.2.5.4.

do_update_pse_allocated_pwr_pri

A function that updates the pse_allocated_pwr_pri value based on the value of PSEAllocatedPowerValue_alt(X) as defined in Table 145–12. This function returns the following variable:

pse_allocated_pwr_pri: See do_classification_pri function.

do_update_pse_allocated_pwr_sec

A function that updates the pse_allocated_pwr_sec value based on the value of PSEAllocatedPowerValue_alt(X) as defined in Table 145–12. This function returns the following variable:

pse_allocated_pwr_sec: See pse_allocated_pwr_sec in 145.2.5.6.

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145.2.5.7 State diagrams

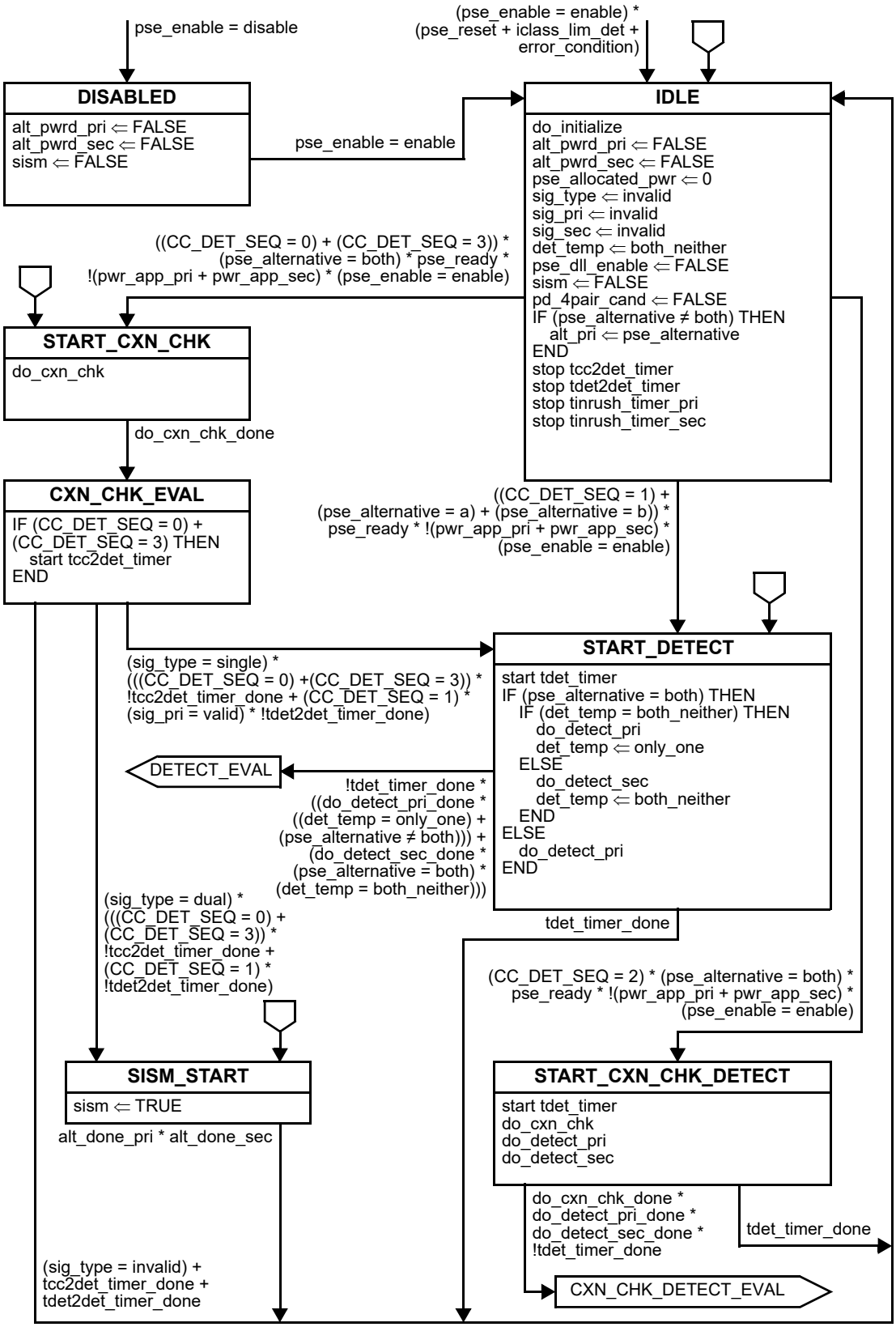

Figure 145–13—Top level PSE state diagram

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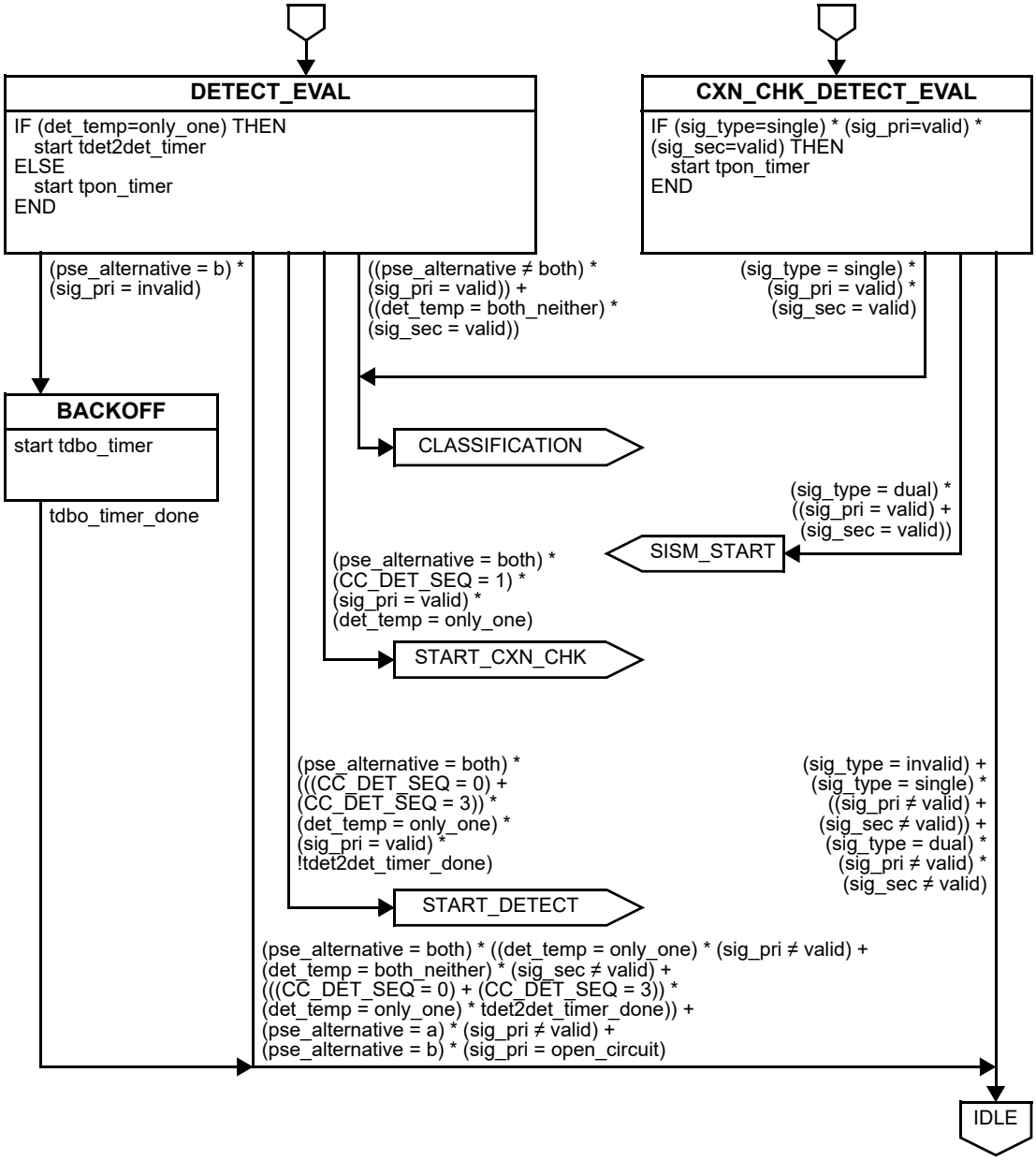

Figure 145–13—Top level PSE state diagram *(continued)*

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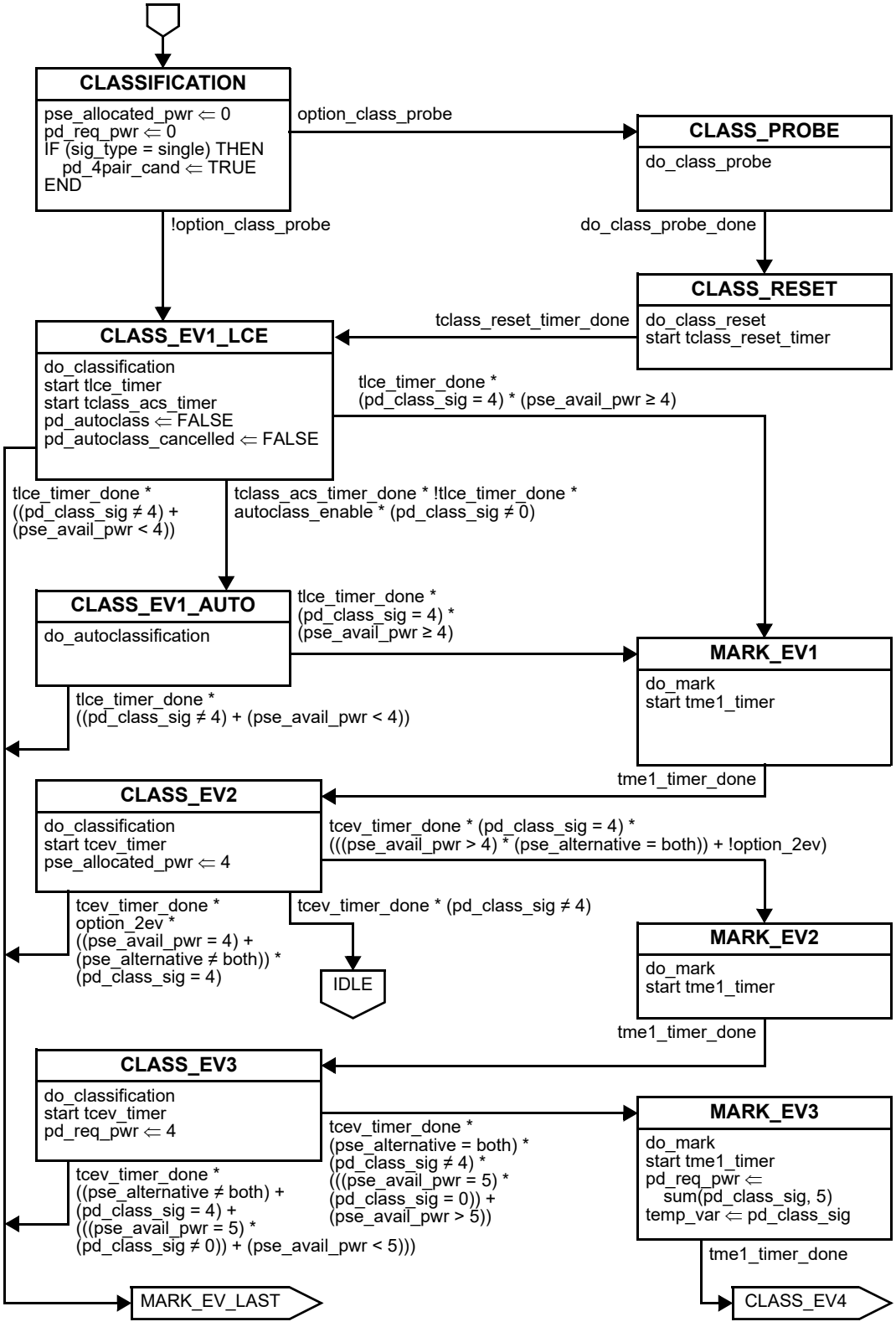

Figure 145–13—Top level PSE state diagram *(continued)*

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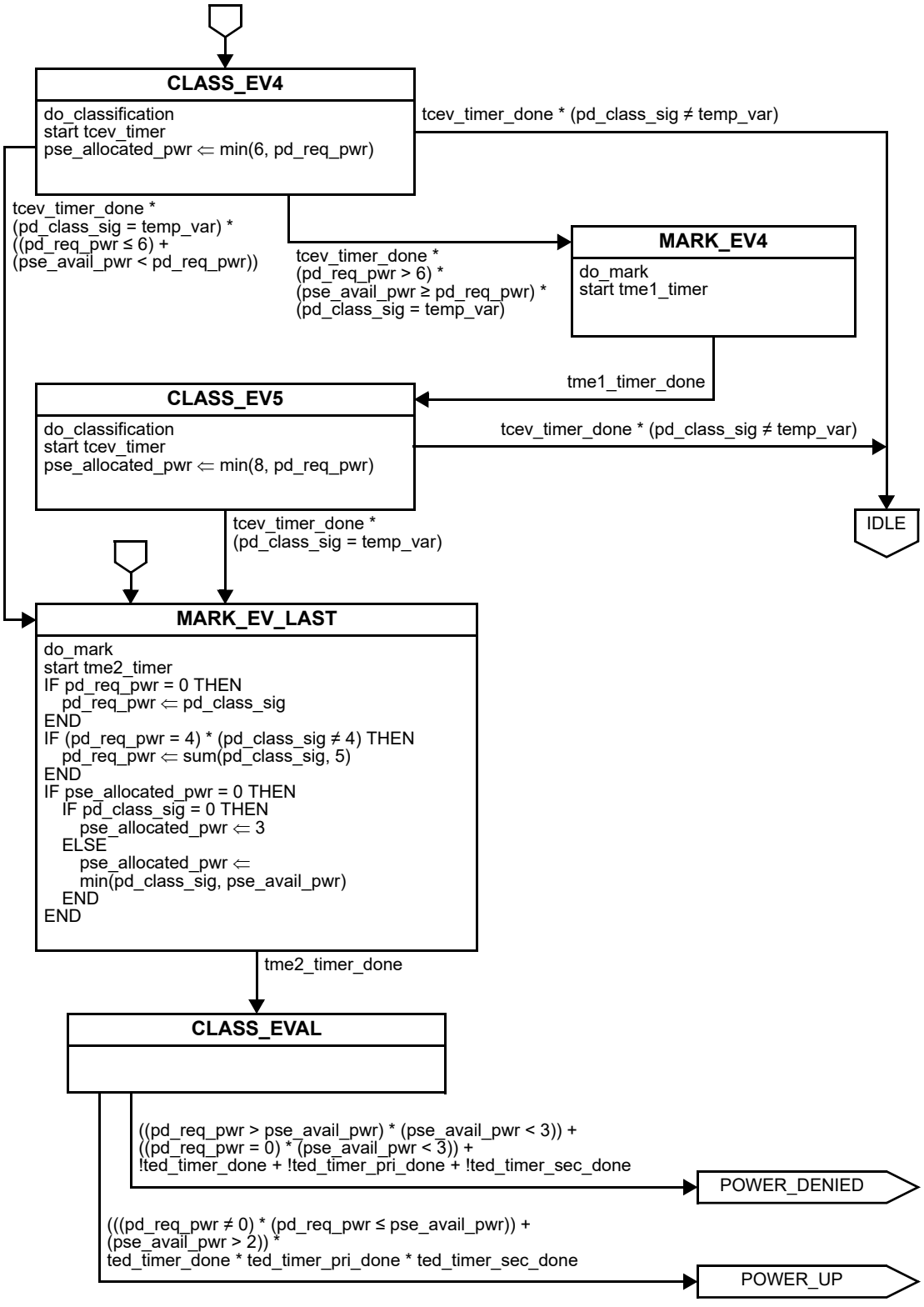

Figure 145–13—Top level PSE state diagram *(continued)*

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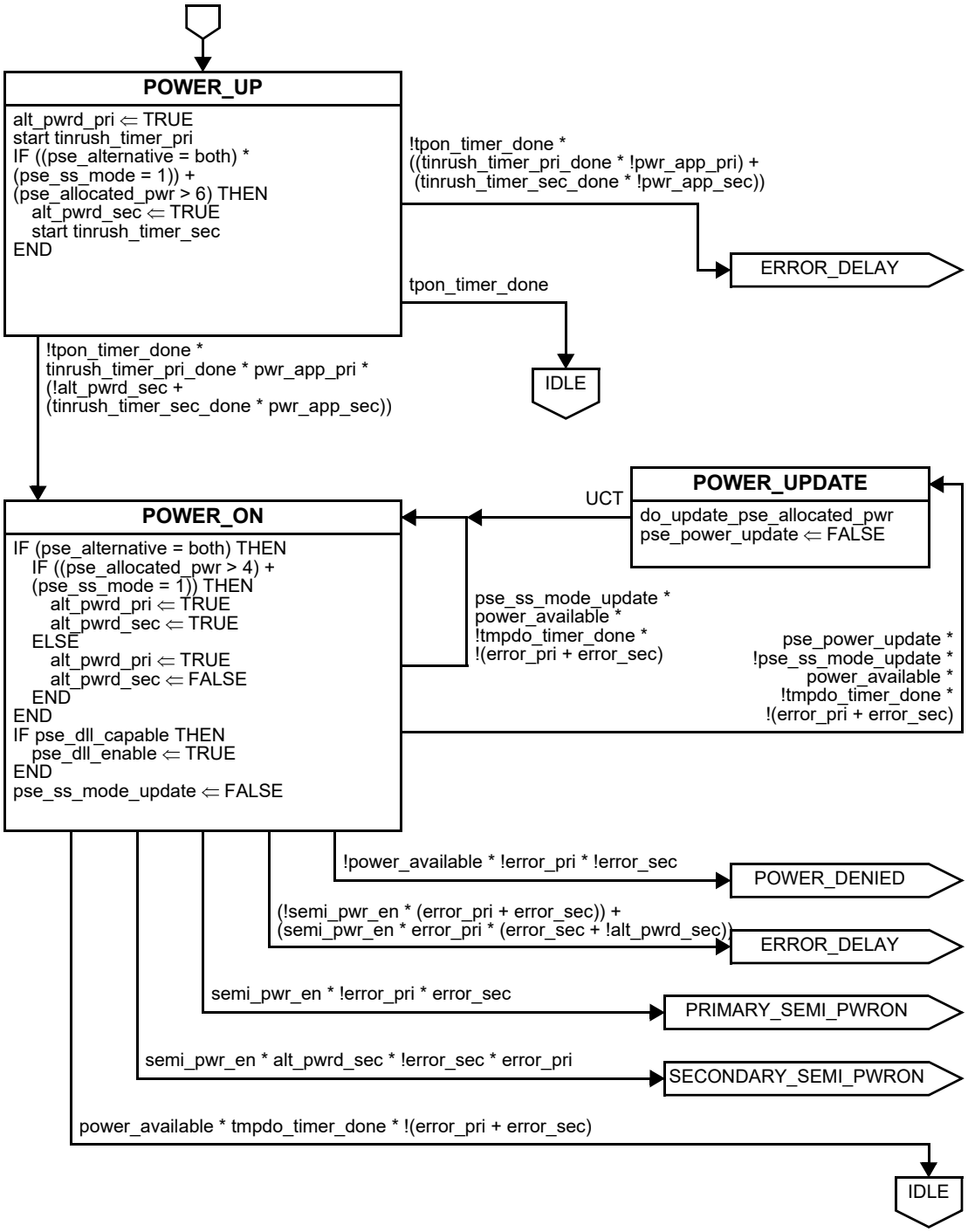

Figure 145–13—Top level PSE state diagram *(continued)*

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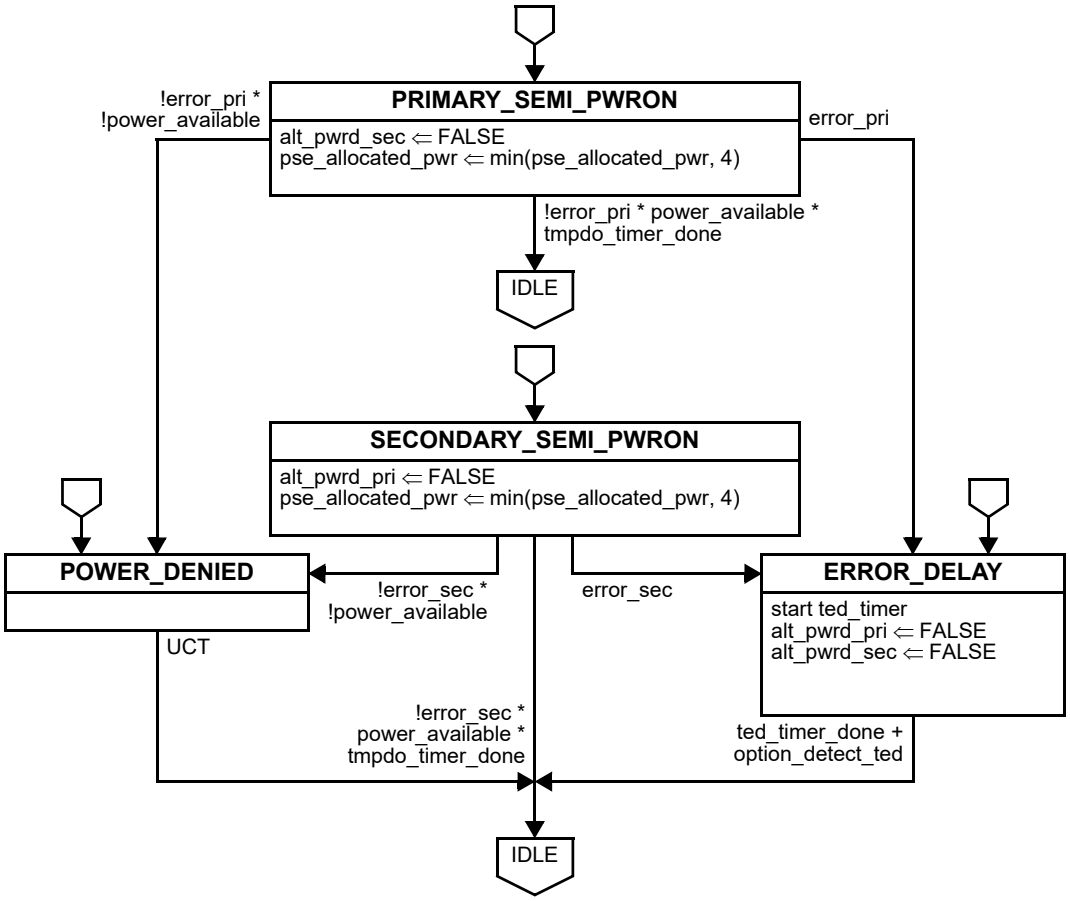

Figure 145–13—Top level PSE state diagram *(continued)*

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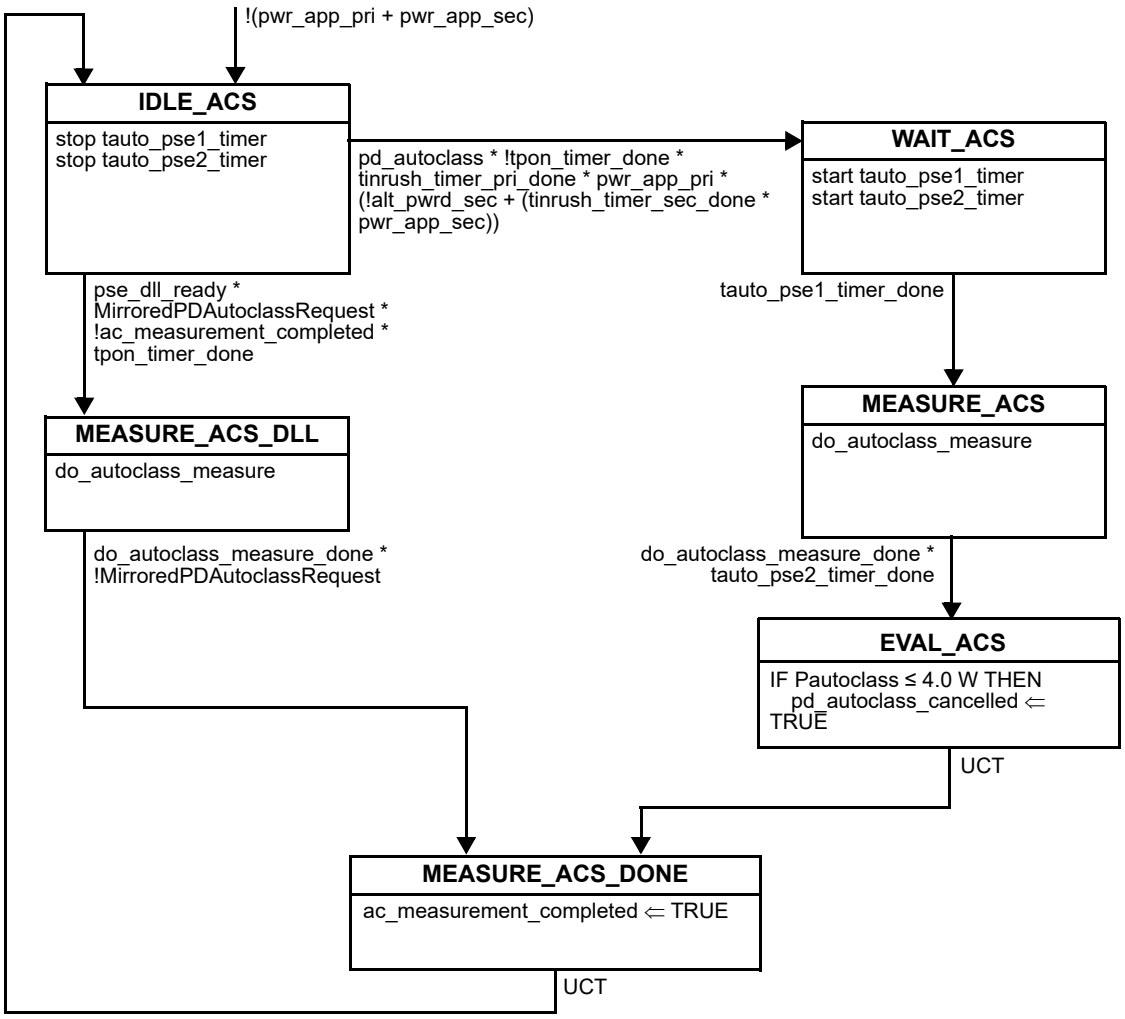

Figure 145–14—PSE Autoclass state diagram

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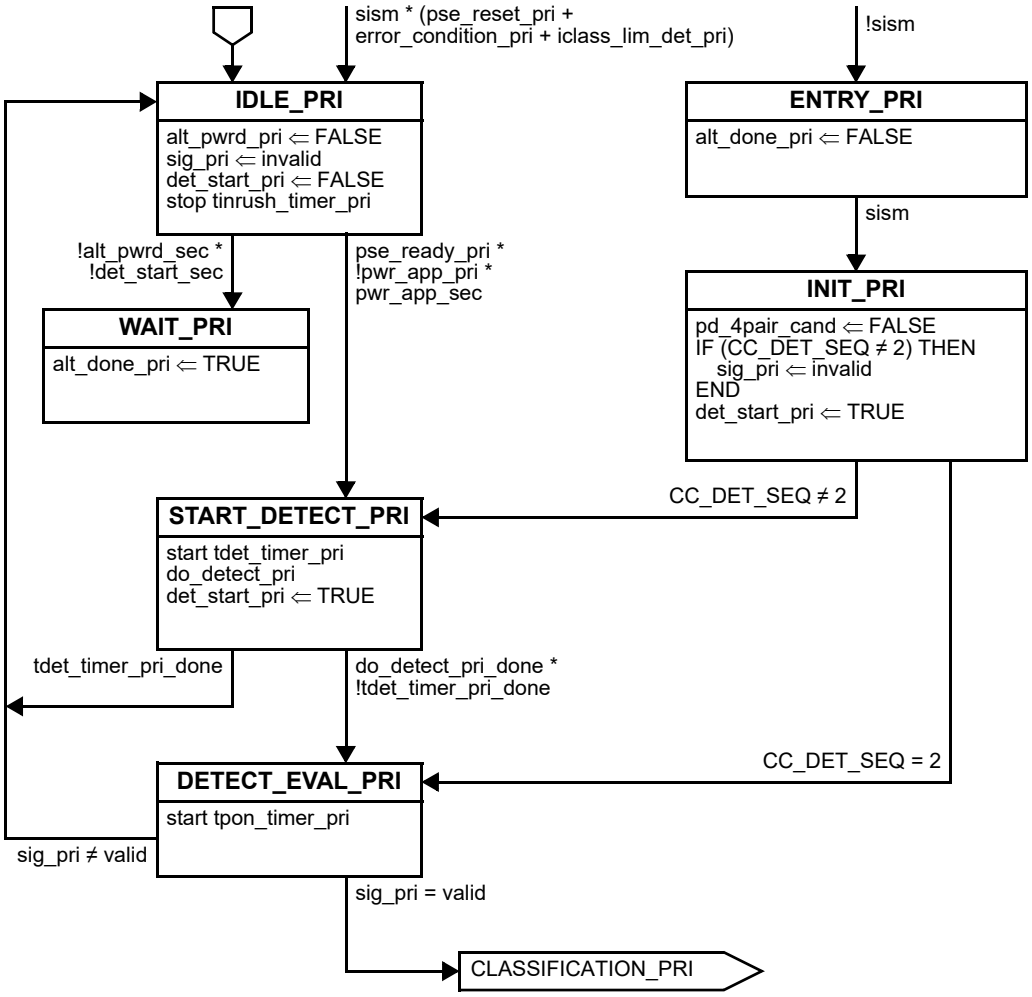

Figure 145–15—Primary Alternative dual-signature semi-independent PSE state diagram

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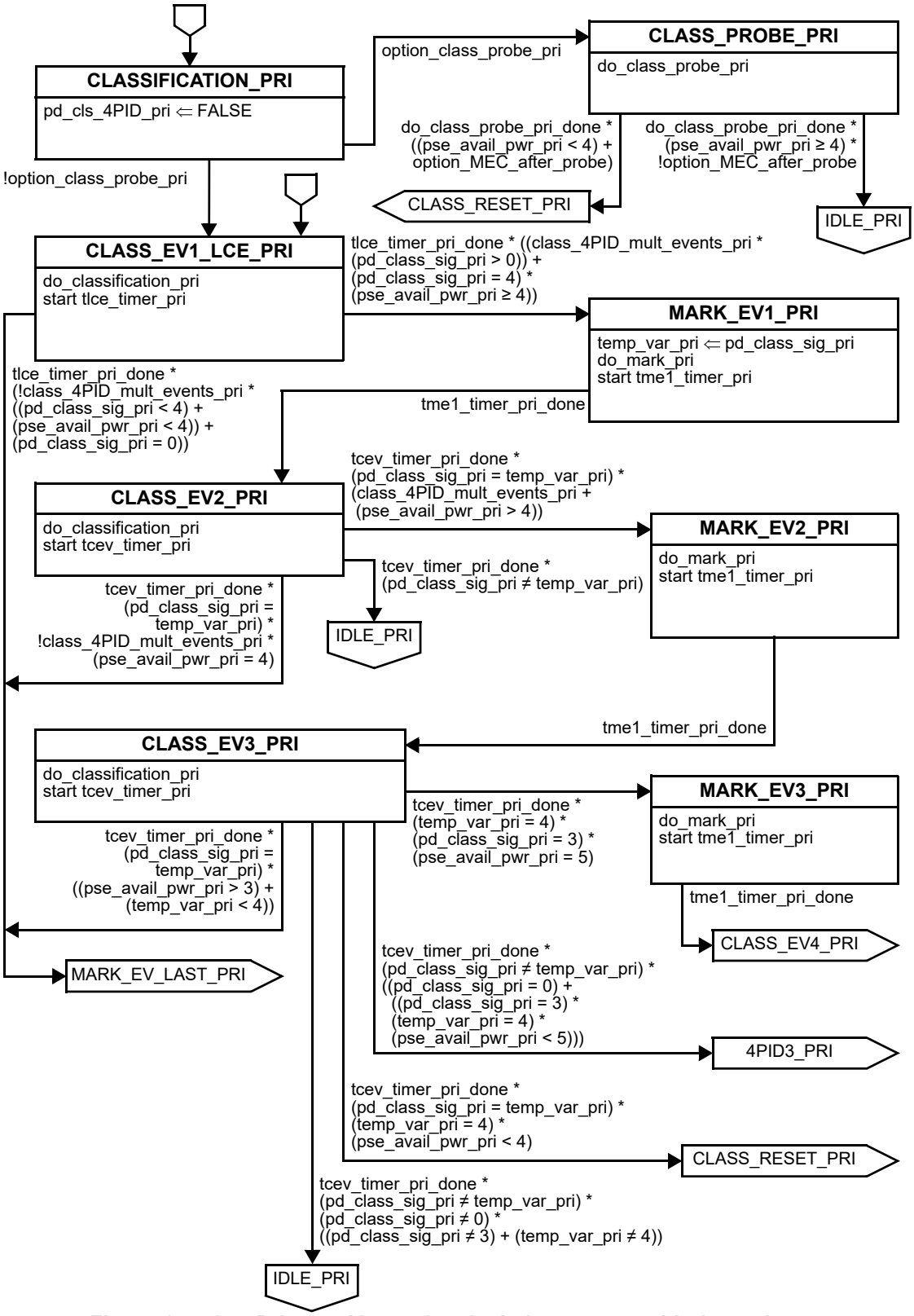

Figure 145–15—Primary Alternative dual-signature semi-independent PSE state diagram *(continued)*

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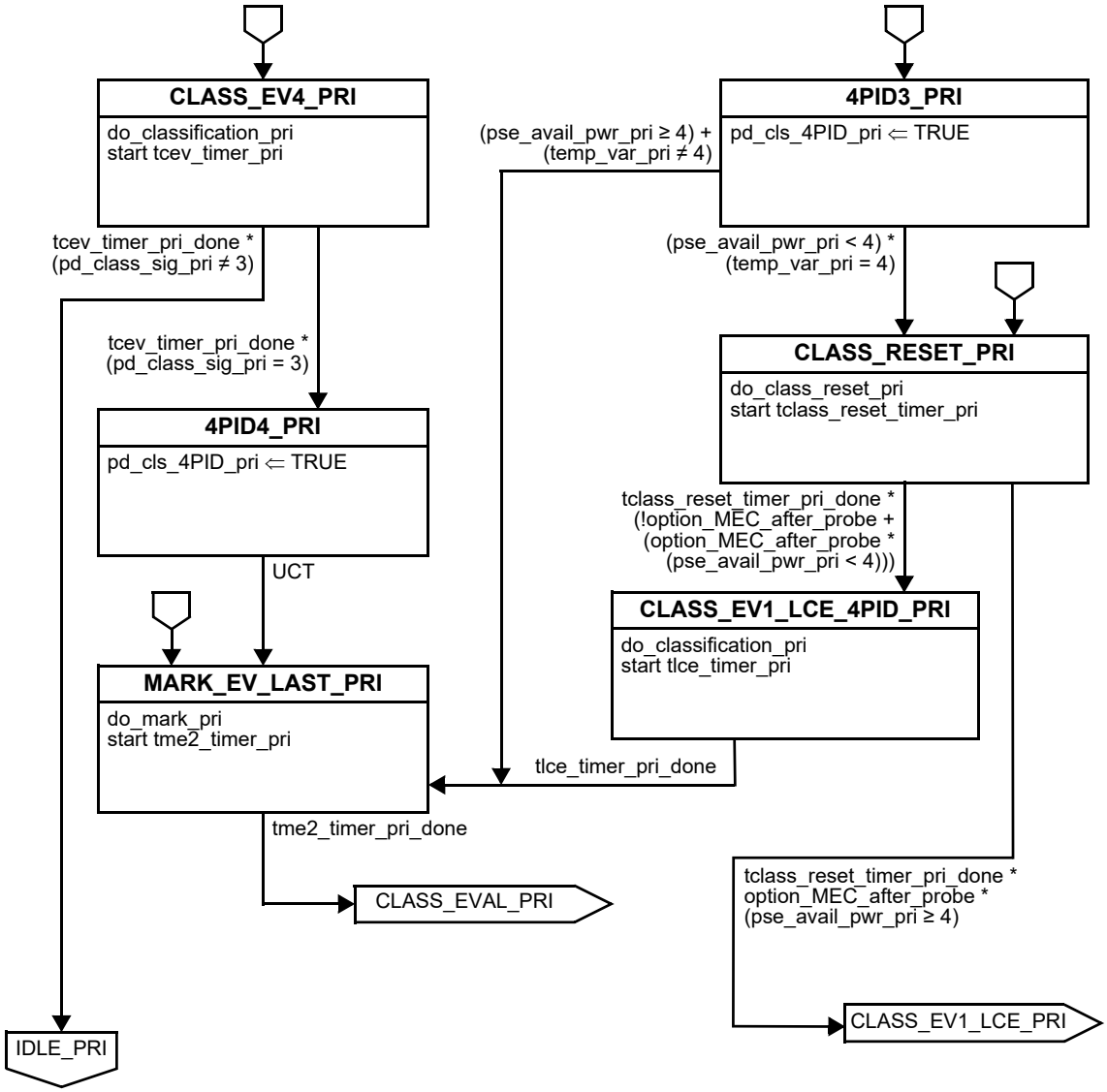

Figure 145–15—Primary Alternative dual-signature semi-independent PSE state diagram *(continued)*

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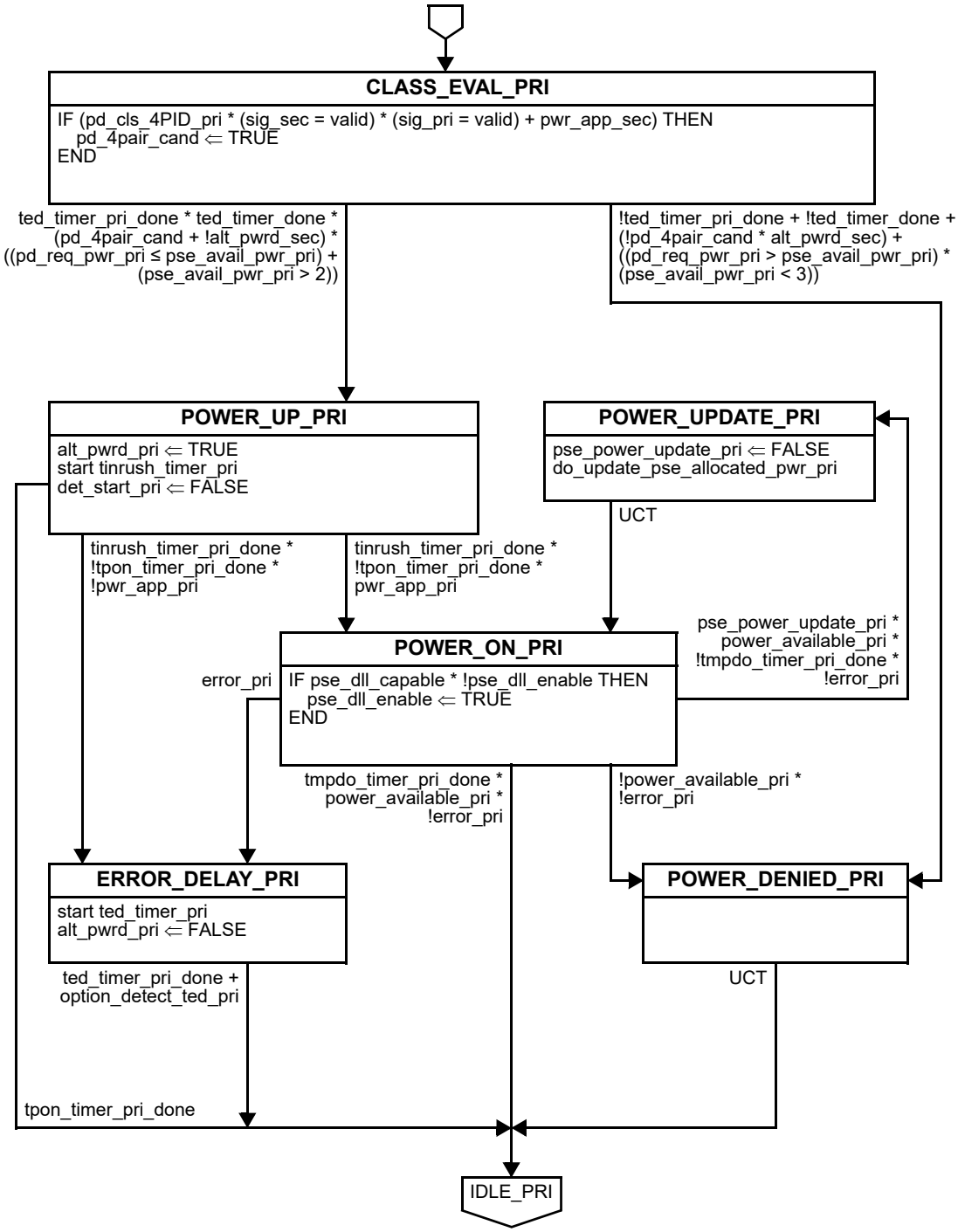

Figure 145–15—Primary Alternative dual-signature semi-independent PSE state diagram *(continued)*

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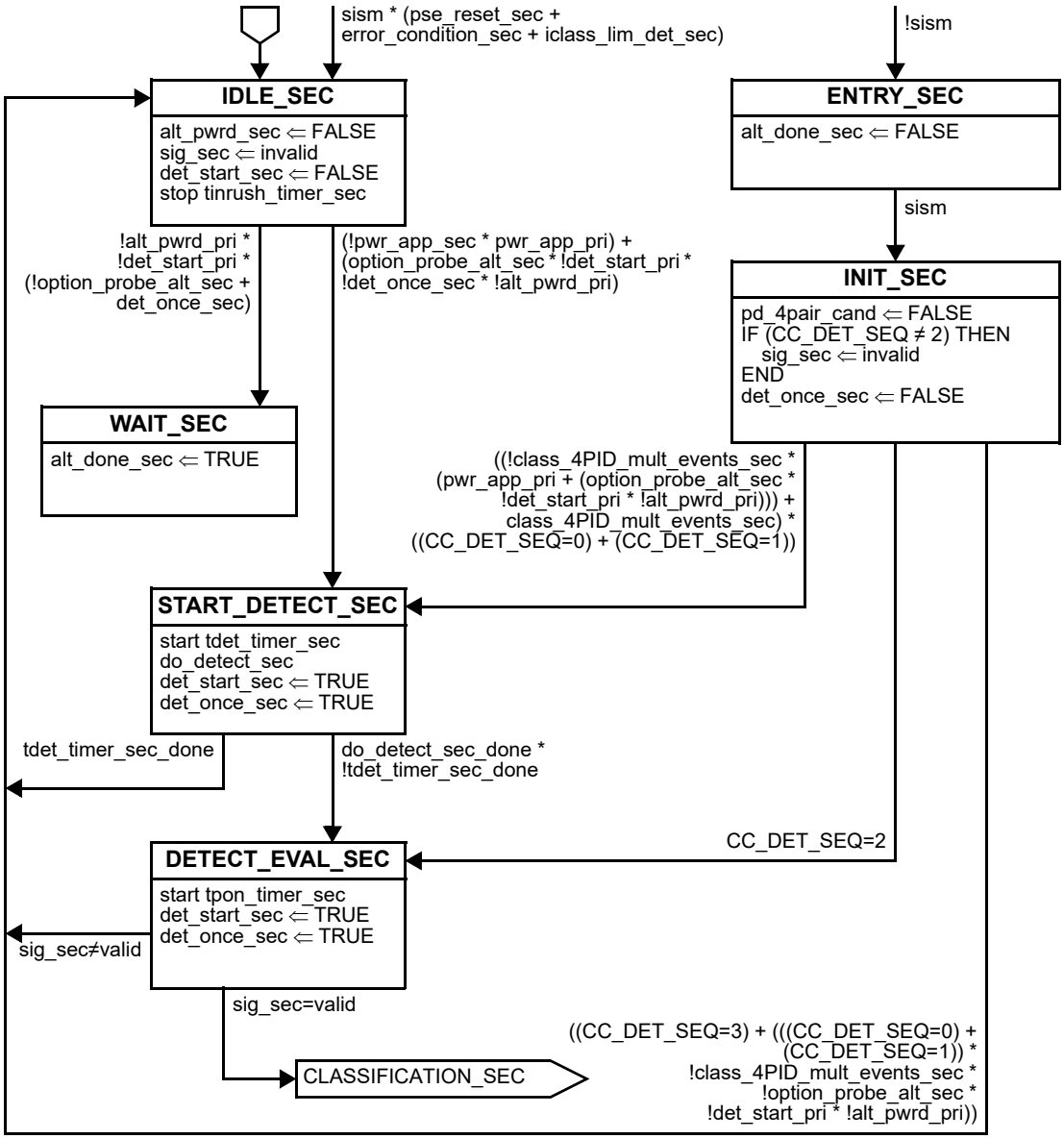

Figure 145–16—Secondary Alternative dual-signature semi-independent PSE state diagram

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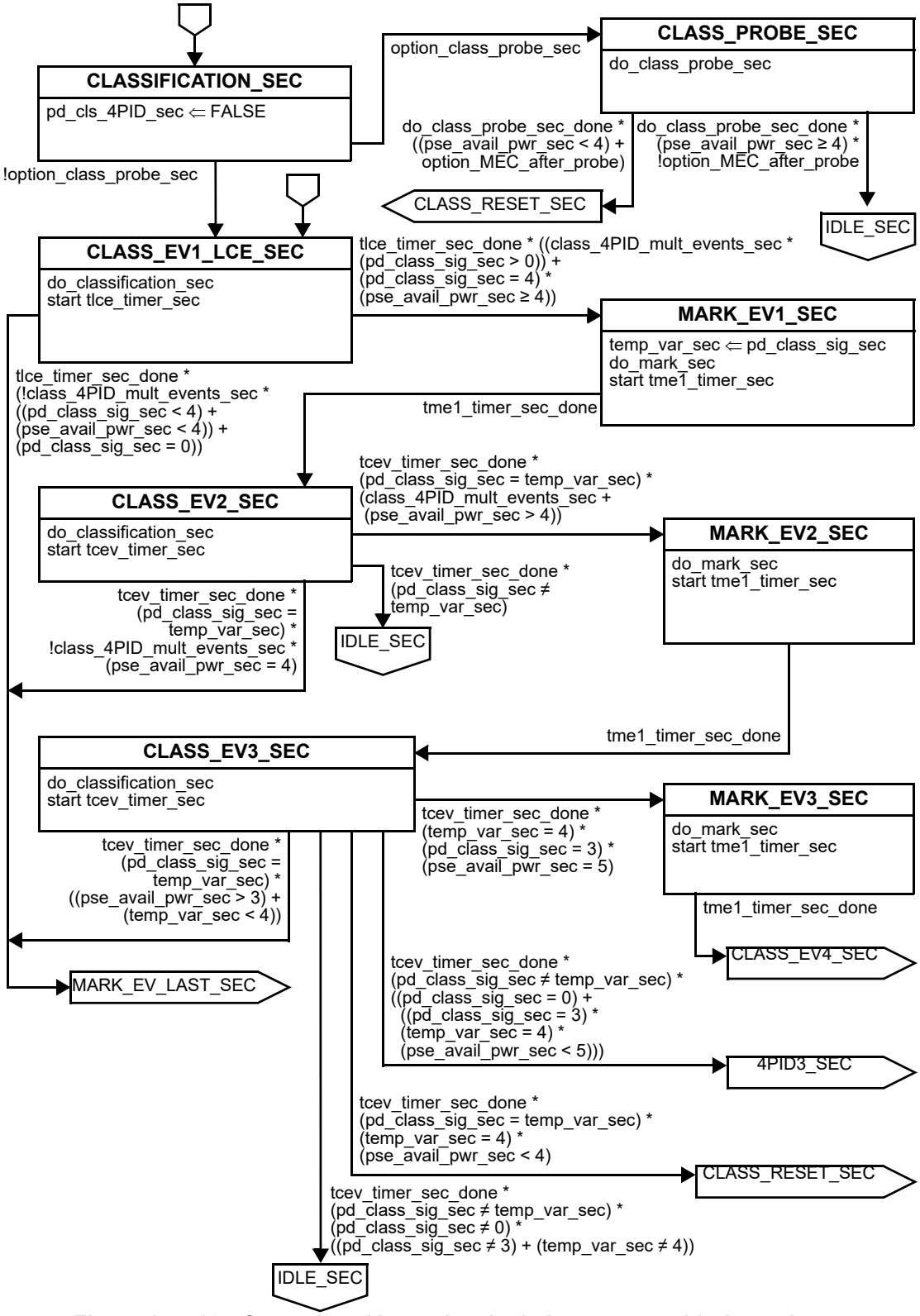

Figure 145–16—Secondary Alternative dual-signature semi-independent PSE state diagram *(continued)*

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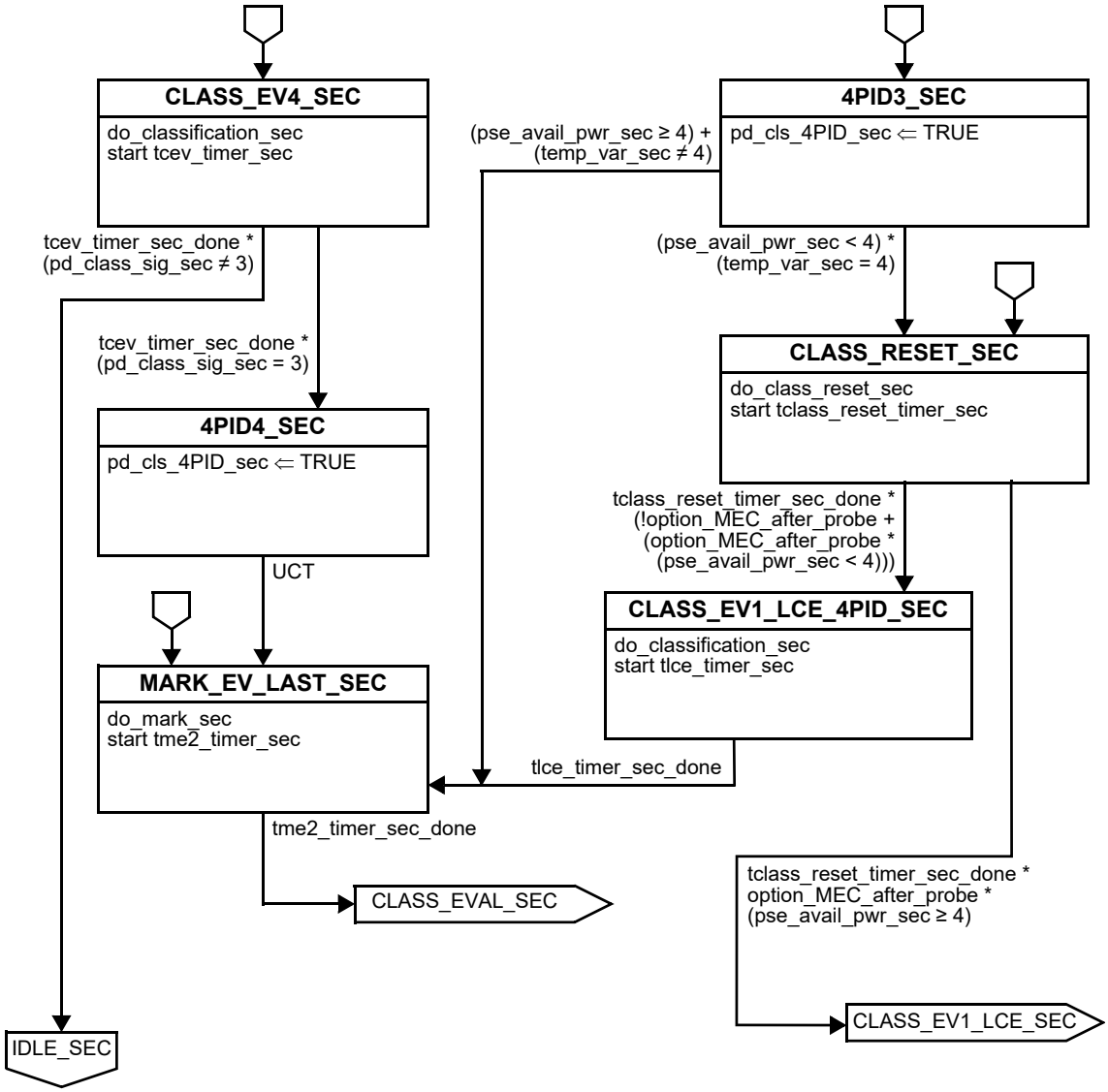

Figure 145–16—Secondary Alternative dual-signature semi-independent PSE state diagram *(continued)*

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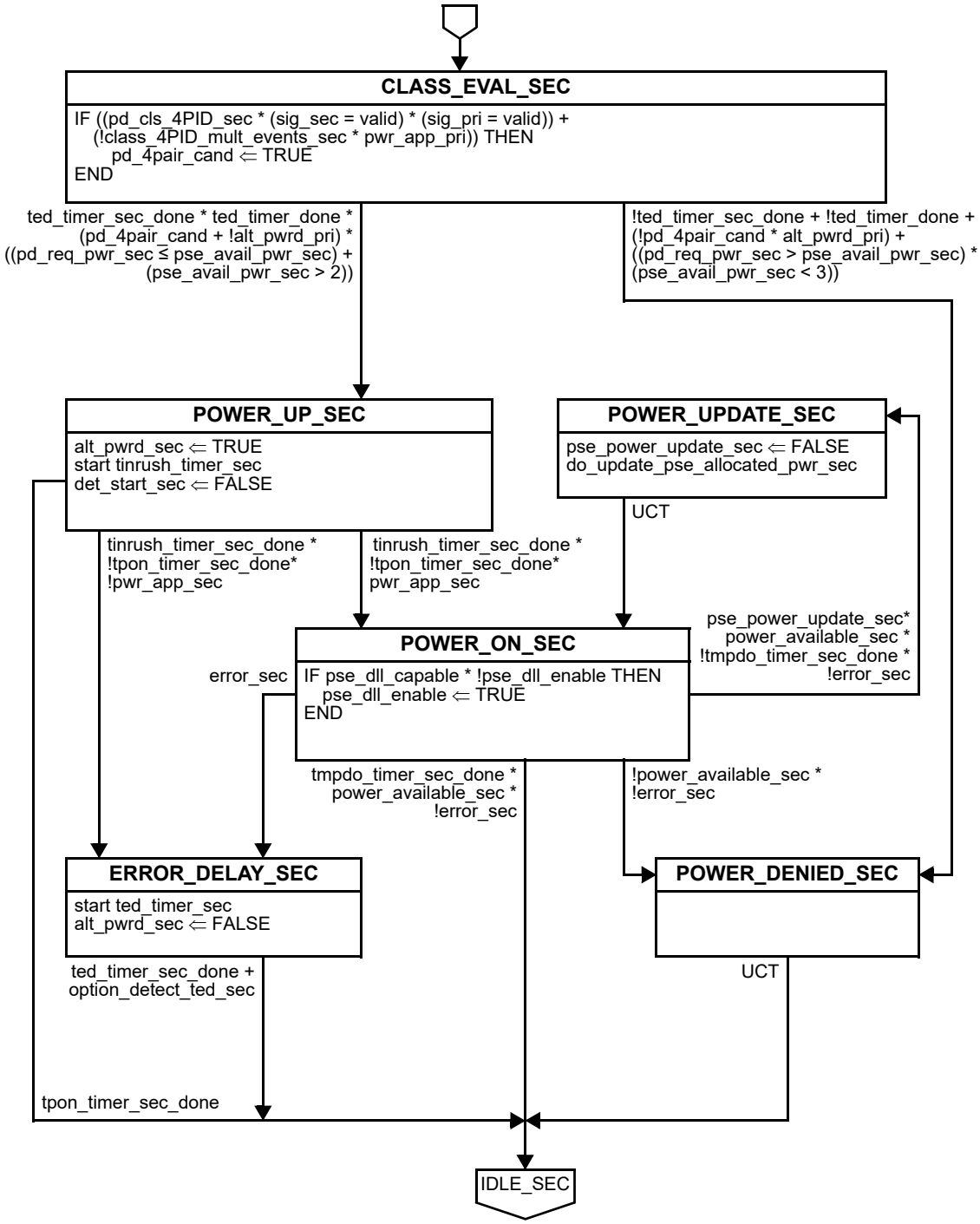

Figure 145–16—Secondary Alternative dual-signature semi-independent PSE state diagram *(continued)*

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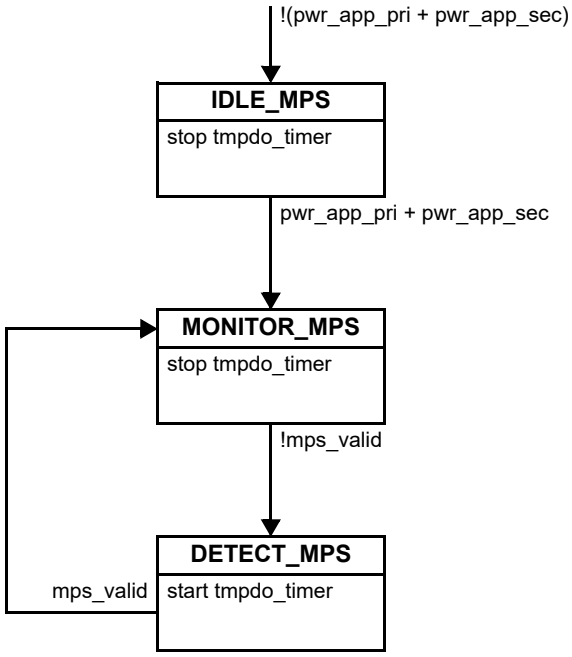

Figure 145–17—PSE MPS monitor state diagram for single-signature PDs or 2-pair operation

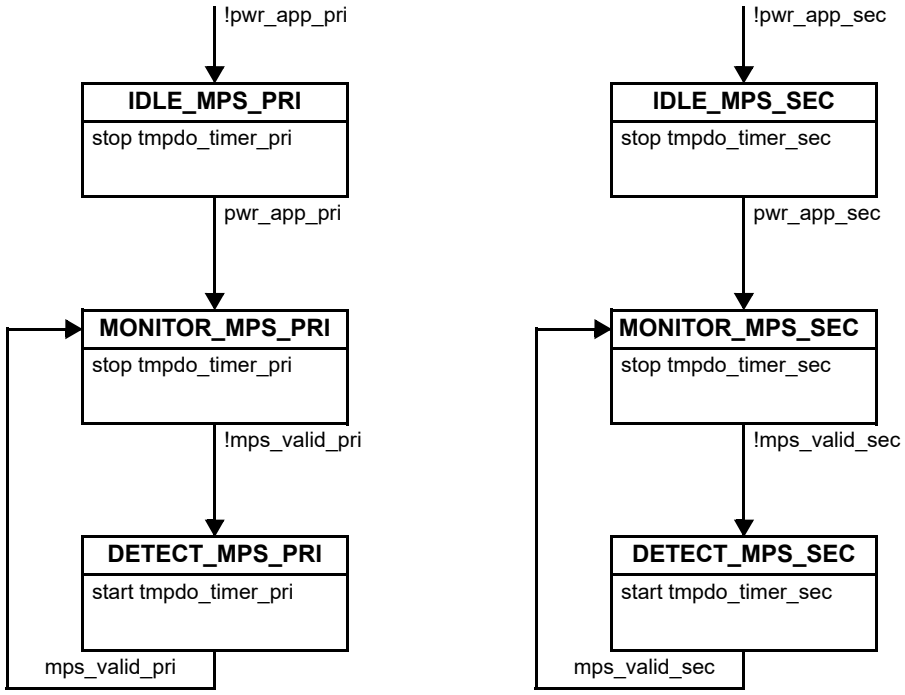

Figure 145–18—PSE MPS monitor state diagram for dual-signature PDs

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145.2.6 PSE detection of PDs

The PSE shall not apply operating voltage to a pairset until the PSE has successfully detected a valid signature over that pairset. When a PSE is already in POWER_ON, it may transition between 2-pair and 4-pair power without redoing detection as described in 145.2.10.1.

The PSE PI is connected to a PD through a link section. The PSE probes the link section in order to detect a valid PD detection signature. In the following subclauses, the link is not called out to preserve clarity.

The PSE is not required to continuously probe to detect a PD detection signature. The period of time when a PSE is not attempting to detect a PD detection signature is implementation dependent. Also, a PSE may successfully detect a PD or detect and classify a PD, but then opt not to power the detected PD.

A PSE detecting an invalid PD signature on either Alternative may perform detection on the other Alternative, and if valid may perform classification on that pairset.

145.2.6.1 PSE detection validation circuit

The PSE shall detect the PD by probing via the PSE PI. The PSE shall present a non-valid PD detection signature as defined in Table 145–22 when probed in either polarity by another PSE. An illustrative embodiment of a detection circuit is shown in Figure 145–19.

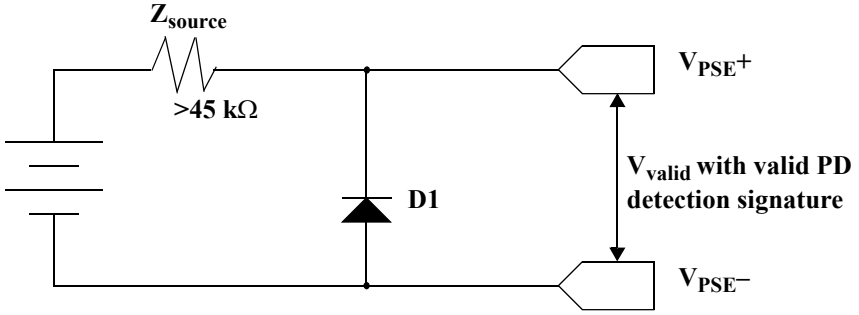

Figure 145–19—PSE detection source

A functional equivalent of the detection circuit that has no source impedance limitation but restricts the PSE detection circuit to the first quadrant is shown in Figure 145–20.

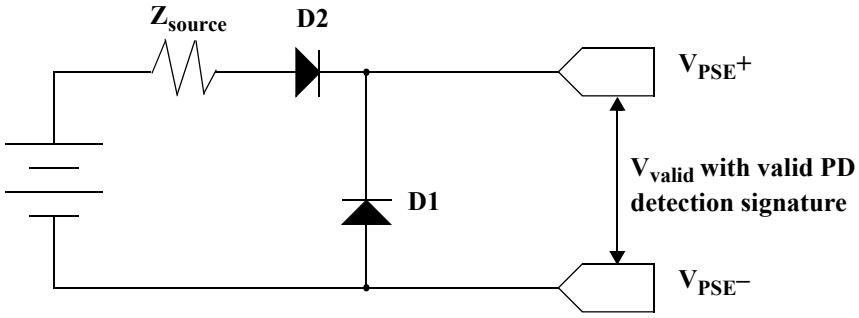

Figure 145–20—Alternative PSE detection source

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In Figure 145–19 and Figure 145–20, the diode D1 presents a non-valid PD detection signature for a reversed voltage PSE to PSE connection.

The open circuit voltage and short circuit current shall meet the specifications in Table 145–7. The PSE shall not be damaged by up to 5 mA backdriven current over the range of V_{oc} as defined in Table 145–7. Output capacitance shall be as defined in Table 145–7 when V_{PSE} is in the range of 0 V to V_{valid} max.

145.2.6.2 Detection probe requirements

The detection voltage at the PSE PI shall be within the V_{valid} voltage range, as defined in Table 145–7, with a valid PD detection signature connected, as defined in Table 145–21.

Table 145–7—PSE PI per pairset detection state electrical requirements

Item	Parameter	Symbol	Unit	Min	Max
1	Open circuit voltage	V_{oc}	V	0	30
2	Short circuit current	I_{sc}	mA	—	5
3	Valid test voltage	V_{valid}	V	2.8	10
4	Voltage difference between test points	ΔV_{test}	V	1	—
5	Slew rate	V_{slew}	V/µs	—	0.1
6	Pairset output capacitance	C_{out}	nF	—	520

In evaluating the presence of a valid PD, the PSE shall make at least two measurements with V_{PSE} values that create at least a ΔV_{test} difference as defined in Table 145–7. An effective resistance is calculated from two or more measurements made during the detection process.

The resistance is calculated with Equation (145–1):

$$R = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \tag{145–1}$$

where

V_1 and V_2 are the first and second voltage measurements made on the pairset, respectively
I_1 and I_2 are the first and second current measurements made on the negative pair of the pairset, respectively
R is the effective resistance

Attached PI capacitance may be determined using these measurements and the port RC time-constant charging characteristics.

NOTE—Settling time before voltage or current measurement: the voltage or current measurement should be taken after V_{PSE} has settled to within 1 % of its steady state condition with a valid PD detection signature connected (as defined in Table 145–21).

The PSE shall control the slew rate of the probing detection voltage when switching between detection voltages to be less than V_{slew} as defined in Table 145–7.

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145.2.6.3 Detection criteria

A PSE shall accept as a valid PD detection signature a pairset with all of the characteristics specified in Table 145–8.

Table 145–8—Valid PD detection signature electrical characteristics, as measured at the PSE PI

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Accept signature resistance	R_{good}	kΩ	19	26.5	—
2	Accept signature capacitance	C_{good}	µF	—	0.15	—
3	Signature offset voltage tolerance	V_{os}	V	0	2	—
4	Signature offset current tolerance	I_{os}	µA	0	12	—

145.2.6.4 Rejection criteria

The PSE shall reject as an invalid detection signature, a pairset which exhibits any of the following characteristics:

a) Resistance less than or equal to R_{bad} min, or
b) Resistance greater than or equal to R_{bad} max, or
c) Capacitance greater than or equal to C_{bad} min.

R_{bad} min, R_{bad} max, and C_{bad} min are defined in Table 145–9.

NOTE—Detection and rejection criteria for Clause 145 remain unchanged from Clause 33, for the purpose of maintaining interoperability with Clause 33 devices (see also 145.2.6.3).

A PSE may accept or reject a signature resistance in the band between R_{good} min and R_{bad} min, and in the band between R_{good} max and R_{bad} max. A PSE may accept or reject a parallel signature capacitance in the band between C_{good} max and C_{bad} min.

In instances where the resistance and capacitance meet the detection criteria, but one or both of the offsets are exceeded, the detection behavior of the PSE is undefined.

Table 145–9—Invalid PD detection signature electrical characteristics, as measured at the PSE PI

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Reject signature resistance	R_{bad}	kΩ	15	33	—
2	Reject signature capacitance	C_{bad}	µF	10	—	—
3	Open circuit resistance	R_{open}	MΩ	0.5	—	—

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145.2.6.5 Open circuit criteria

If a PSE that is performing detection using Alternative B (see 145.2.4) determines that the impedance at the PI is greater than R_{open} as defined in Table 145–9, it may optionally consider the link to be open circuit and omit the tdbo_timer interval.

145.2.7 Connection check

PSEs that will source power on both pairsets shall complete a connection check prior to the classification of a PD as defined in 145.2.8 to determine if the PSE is connected to a single-signature PD configuration, a dual-signature PD configuration, or neither.

NOTE—When a link segment is connected to an MDI, not all contacts are made simultaneously. A link segment connection or removal may occur at any time during connection check. PSE implementations should take these considerations into account.

During connection check the PSE shall meet the specifications for open circuit voltage, V_{oc}, and short circuit current, I_{sc}, in Table 145–7. The connection check voltage at the PSE PI shall be within the V_{valid} voltage range, as defined in Table 145–7, when a single-signature PD or a dual-signature PD is connected.

The specification of T_{cc2det}, defined in Table 145–10, applies to the time between the end of connection check and the beginning of detection on at least one pairset. If the connection check takes place after the beginning of detection, this specification does not apply.

The specification of $T_{det2det}$, defined in Table 145–10, applies to the time between the end of detection on the first pairset to the beginning of detection on the other pairset when the second detection occurs before power up on the first pairset.

Table 145–10—Connection check timing requirements

Item	Parameter	Symbol	Unit	Min	Max	Additional Information
1	Connection check to detection time	T_{cc2det}	s	—	0.4	Applies only when connection check is performed before the start of detection.
2	Detection to detection time	$T_{det2det}$	s	—	0.4	—

The connection check is rerun before applying power if power up fails to meet the timing requirements in both Table 145–10 and 145.2.10.14 or if power is absent on both pairsets simultaneously.

If the voltage on either pairset rises above V_{valid} max, as defined in Table 145–7, during connection check, the PSE shall reset the PD by bringing the voltage at the PI below V_{off} max, as defined in Table 145–16, for at least T_{Reset}, as defined in Table 145–14, before performing classification.

145.2.8 PSE classification of PDs and mutual identification

The ability for the PSE to query the PD in order to determine the power requirements of that PD is called classification. The interrogation and power classification function is intended to establish mutual identification and is intended for use with advanced features such as power management.

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Mutual identification is the mechanism that allows a PSE to differentiate between Type 1, Type 2, Type 3, and Type 4 PDs. Additionally, mutual identification allows PDs to differentiate between Type 1, Type 2, Type 3, and Type 4 PSEs.

There are two forms of classification: Multiple-Event Physical Layer classification and Data Link Layer (DLL) classification.

Physical Layer classification occurs after a valid detection and before a PSE supplies power to a PD, when the PSE asserts a voltage in the range of V_{Class} as defined in Table 145–14 onto one or both pairsets. This is called a class event. The PD responds to each class event with a current representing one of a limited number of class signatures. The class signatures generated by the PD indicate the PD requested Class. See Table 145–26 and Table 145–27 for a mapping of class signature to the PD requested Class.

NOTE—Requested Class 0 is not defined for Type 3 PDs. A Type 1 PD that does not implement Physical Layer classification requests Class 0, with a power level equivalent to Class 3. Such PDs are assigned to Class 3 by Type 3 and Type 4 PSEs.

The assigned Class is the result of the PD requested Class and the number of class events produced by the PSE as shown in Table 145–11. See 145.3.6 for PD classification behavior.

When a single-signature PD requests a higher Class than a PSE can support, the PSE assigns the PD Class 3, 4, or 6, whichever is the highest that it can support. When a dual-signature PD requests a higher Class than a PSE can support, the PSE assigns the PD Class 3 or 4, whichever is the highest that it can support. The minimum output power a PSE supports depends on the assigned Class.

The minimum output power a PSE supports when powering a single-signature PD, or supplying power in 2-pair mode, is defined by Equation (145–2). PSE implementations may use $V_{PSE} = V_{Port\_PSE\text{-}2P}$ min and $R_{Chan\text{-}2P} = R_{Ch}$ when the assigned Class is 1 through 4, or $R_{Chan} = R_{Ch}/2$ when the assigned Class is 5 through 8 to arrive at over-margined values as shown in Table 145–11. P_{Class} may subsequently be adjusted using Data Link Layer classification.

$$P_{Class} = \left\{ \begin{array}{ll} V_{PSE} \times \left(\dfrac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan\text{-}2P} \times P_{Class\_PD}}}{2 \times R_{Chan\text{-}2P}} \right) & \text{for assigned Class 1 through 4} \\ V_{PSE} \times \left(\dfrac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan} \times P_{Class\_PD}}}{2 \times R_{Chan}} \right) & \text{for assigned Class 5 through 8} \end{array} \right\}_{W} \quad (145\text{–}2)$$

where

V_{PSE} is the voltage across the pairset at the PSE PI as defined in 145.1.3
R_{Chan} is the link section DC loop resistance
$R_{Chan\text{-}2P}$ is the pairset DC loop resistance
P_{Class_PD} is the maximum power at the PD PI per the PDs assigned Class, as defined in Table 145–29

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When connected to a dual-signature PD, a PSE operating over 4 pairs treats the requested power over each pairset independently. The minimum output power a PSE supports on a pairset when powering a dual-signature PD is defined by Equation (145–3). PSE implementations may use $V_{PSE} = V_{Port\_PSE\text{-}2P}$ min and $R_{Chan\text{-}2P} = R_{Ch}$ to arrive at over-margined values as shown in Table 145–11. $P_{Class\text{-}2P}$ may subsequently be adjusted using Data Link Layer classification or Autoclass.

$$P_{\text{Class-2P}} = \left\{ V_{\text{PSE}} \times \left(\frac{V_{\text{PSE}} - \sqrt{V_{\text{PSE}}^2 - 4 \times R_{\text{Chan-2P}} \times P_{\text{Class\_PD-2P}}}}{2 \times R_{\text{Chan-2P}}} \right) \right\}_{\text{W}} \tag{145–3}$$

where

V_{PSE} is the voltage across the pairset at the PSE PI as defined in 145.1.3

$R_{Chan\text{-}2P}$ is the pairset DC loop resistance

$P_{Class\_PD\text{-}2P}$ is the maximum power at the PD PI for a pairset per the PDs assigned Class, as defined in Table 145–29

P_{Class} and $P_{Class\text{-}2P}$ are valid over the range of $V_{Port\_PSE\text{-}2P}$ defined in Table 145–16.

If the PD connected to the PSE performs Autoclass (see 145.2.8.2 and 145.3.6.2), the PSE may set the minimum supported output power based on $P_{Autoclass}$, the power drawn during the Autoclass measurement window. $P_{Autoclass}$ shall be increased by at least P_{ac_margin}, as defined in Table 145–15, in order to account for potential increase in link section resistance due to temperature increase, up to the value defined in Table 145–11 of the Class assigned to the PD. If $P_{Autoclass}$ is less than or equal to 4 W then the minimum supported output power shall be P_{Class} per the assigned Class.

When the PSE assigns Class 5 through 8 prior to a fault and then transitions to PRIMARY_SEMI_PWRON or SECONDARY_SEMI_PWRON, it shall revert the allocation of power to Class 4 and assert local_system_change to update PSEAllocatedPowerValue.

A PSE that measured $P_{Autoclass}$ while providing power over 4 pairs, shall increase the power allocation by at least P_{ac_extra}, as defined in Equation (145–4), when it provides power over 2 pairs.

$$P_{\text{ac\_extra}} = \left\{ \left(\frac{P_{\text{Autoclass}}}{V_{\text{Port\_PSE-2P}}\text{min}} \right)^2 \times \frac{R_{\text{Ch}}}{2} \right\}_{\text{W}} \tag{145–4}$$

where

$P_{Autoclass}$ is the amount of power measured by the PSE during the Autoclass measurement

$V_{Port\_PSE\text{-}2P}$ min is the minimum PSE operating voltage

R_{Ch} is the maximum pairset DC loop resistance, as defined in Table 145–1

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Table 145–11—Physical Layer power classifications

PD Requested Class	Number of PSE class events	Assigned Class	P_{Class}	$P_{Class-2P}$
PSEs connected to a single-signature PD				
1	1	1	4 W	—
2	1	2	6.7 W	—
0, 3 to 8	1	3	14 W	—
4 to 8	2 or 3	4	30 W	—
5	4	5	45 W	—
6 to 8	4	6	60 W	—
7	5	7	75 W	—
8	5	8	90 W	—
PSEs connected to a dual-signature PD (classification per pairset)				
1	1, 2, or 3	1	—	4 W
2	1, 2, or 3	2	—	6.7 W
3	1, 2, or 3	3	—	14 W
4 or 5	1	3	—	14 W
4 or 5	2 or 3	4	—	30 W
5	4	5	—	45 W

NOTE 1—P_{Class} in Table 145–11 is the minimum required power at the PSE PI calculated using minimum $V_{Port\ PSE-2P}$ and maximum R_{Chan}. Use Equation (145–2) for other values of $V_{Port\ PSE-2P}$ and R_{Chan}. For PD requested power levels, see Table 145–26.

NOTE 2—$P_{Class-2P}$ in Table 145–11 is the minimum required power for a pairset calculated using minimum $V_{Port\ PSE-2P}$ and maximum $R_{Chan-2P}$. Use Equation (145–3) for other values of $V_{Port\ PSE-2P}$ and $R_{Chan-2P}$. For PD requested power levels, see Table 145–27.

NOTE 3—The number of PSE class events refers to the number of class events since the most recent PD reset.

NOTE 4—The values of P_{Class} and $P_{Class-2P}$ are calculated for the lowest Type PSE that is able to support that power level.

With Data Link Layer classification, the PSE and PD communicate using the Data Link Layer Protocol (see 145.5) after the data link is established. The Data Link Layer classification has finer power resolution and the ability for the PSE and PD to participate in dynamic power allocation wherein allocated power to the PD may change one or more times during PD operation. Data Link Layer classification takes precedence over Physical Layer classification.

After a successful DLL classification, the assigned Class changes depending on the value of the PSEAllocatedPowerValue or PSEAllocatedPowerValue_alt(X) variable, as defined in Table 145–12. The PSEAllocatedPowerValue or PSEAllocatedPowerValue_alt(X) values correspond with the maximum power a PD may draw, P_{Class_PD} or P_{Class_PD-2P} respectively; see Table 145–29 and 145.5.3.2.2.

Subsequent to successful detection, PSEs shall perform Multiple-Event Physical Layer classification and may perform Data Link Layer classification. PSEs that will source power over 4-pair to a dual-signature PD shall perform Physical Layer classification on each pairset.

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Table 145–12—Relation of assigned Class and DLL

Single-signature		Dual-signature	
PSEAllocatedPowerValue	**Assigned Class**	**PSEAllocatedPowerValue_alt(X)**	**Assigned Class on Alternative X**
1 to 39	1	1 to 39	1
40 to 65	2	40 to 65	2
66 to 130	3	66 to 130	3
131 to 255	4	131 to 255	4
256 to 400	5	256 to 499	5
401 to 510	6		
511 to 620	7		
621 to 999	8		

A PSE shall be capable of assigning the highest Class it can support by means of Multiple-Event Physical Layer classification.

A PSE shall return to IDLE if it fails to complete classification after successfully completing detection of a single-signature PD. A PSE shall return to IDLE_PRI or IDLE_SEC, whichever corresponds to the appropriate Alternative, if it successfully completes detection on a pairset of a dual-signature PD but fails to complete classification on that pairset.

145.2.8.1 PSE Multiple-Event Physical Layer classification

Classification consists of a series of classification and mark events as defined in the state diagram in Figure 145–13, Figure 145–15, and Figure 145–16.

Voltages V_{Class}, V_{Mark}, and V_{Reset} and currents I_{Class_LIM} and I_{Mark_LIM} are specified in Table 145–14. PD class signature measurements of I_{Class} are specified in Table 145–13. Classification times, T_{LCE}, T_{CEV}, T_{ME1}, T_{ME2}, T_{Class}, and T_{Reset} are specified in Table 145–14. Autoclass timing, T_{Class_ACS} is specified in Table 145–14. See Annex 145B for more details and timing diagrams.

Type 3 PSEs:

— Shall provide a maximum of four class events and four mark events for single-signature PDs.
— Shall provide a maximum of three class events and three mark events on each pairset for dual-signature PDs.

Type 4 PSEs:

— Shall provide a maximum of five class events and five mark events for single-signature PDs.
— Shall provide a maximum of four class events and four mark events on each pairset for dual-signature PDs.

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Table 145–13—Class signatures evaluated at the PSE PI

Measured I_{Class}	Class signature
0 mA to 5 mA	Class signature 0
> 5 mA and < 8 mA	Either class signature 0 or 1
8 mA to 13 mA	Class signature 1
> 13 mA and < 16 mA	Either class signature 1 or 2
16 mA to 21 mA	Class signature 2
> 21 mA and < 25 mA	Either class signature 2 or 3
25 mA to 31 mA	Class signature 3
> 31 mA and < 35 mA	Either class signature 3 or 4
35 mA to 45 mA	Class signature 4
> 45 mA and < 51 mA	Either class signature 4 or invalid class signature

Table 145–14—PSE Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max
1	Class event voltage	V_{Class}	V	15.5	20.5
2	Mark event voltage	V_{Mark}	V	7	10
3	Classification reset voltage	V_{Reset}	V	0	2.8
4	Class event current limitation	I_{Class_LIM}	A	0.051	0.1
5	Mark event current limitation	I_{Mark_LIM}	A	0.005	0.1
6	Classification reset timing	T_{Reset}	ms	15	—
7	Class event I_{Class} measurement timing	T_{Class}	ms	6	—
8	LCE I_{Class} measurement timing	T_{Class_LCE}	ms	T_{Class}	75
9	Autoclass I_{Class} measurement timing	T_{Class_ACS}	ms	88	—
10	Long first class event timing	T_{LCE}	ms	88	105
11	Second through fifth class event timing	T_{CEV}	ms	6	20
12	Mark event timing (except last mark event)	T_{ME1}	ms	6	12
13	Last mark event timing[a]	T_{ME2}	ms	6	—

[a] The maximum value of T_{ME2} is limited by T_{pon}, as defined in 145.2.10.14

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PSEs connected to a single-signature PD shall issue no more class events than the Class they are able to support and no more than

— One class event when the PD requests Class 0 through 3
— Three class events when the PD requests Class 4
— Four class events when the PD requests Class 5 or 6
— Five class events when the PD requests Class 7 or 8

between the most recent time V_{PSE} was at V_{Reset} for at least T_{Reset} and a transition to any of the power up states.

PSEs connected to a dual-signature PD shall issue, for a given pairset, no more class events than the Class they are able to support and no more than

— Three class events when the PD requests Class 1 through 4 on the given pairset
— Four class events when the PD requests Class 5 on the given pairset

between the most recent time V_{PSE} was at V_{Reset} for at least T_{Reset} and a transition to any of the power up states.

PSEs that issue more class events than the Class they are capable of supporting, in order to determine the PD requested Class, transition to CLASS_RESET to reset the PD's class event count.

When the PSE is in CLASS_EV1_LCE, CLASS_EV1_AUTO, CLASS_EV1_LCE_PRI, CLASS_EV1_LCE_SEC, CLASS_EV1_LCE_4PID_PRI, or CLASS_EV1_LCE_4PID_SEC, it shall provide to the PI or pairset V_{Class}, subject to T_{LCE} timing specification.

The PSE in CLASS_EV1_AUTO shall measure I_{Class} on the negative pair or pairs after T_{Class_ACS}, referenced from the application of the first class event, to determine if the PD will perform Autoclass. If the Autoclass enabled PSE in CLASS_EV1_AUTO measures I_{Class} in the range of class signature 0 this indicates the PD will perform Autoclass; see 145.2.8.2 and 145.3.6.2.

When the PSE is in CLASS_EV2, CLASS_EV2_PRI, CLASS_EV2_SEC, CLASS_EV3, CLASS_EV3_PRI, CLASS_EV3_SEC, CLASS_EV4, CLASS_EV4_PRI, CLASS_EV4_SEC, or CLASS_EV5, it shall provide to the PI or pairset V_{Class}, subject to the T_{CEV} timing specification.

In all CLASS states except CLASS_EV1_AUTO, the PSE shall measure I_{Class} on the negative pair or pairs after T_{Class}. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

The timing specification for PSEs in a DO_CLASS_PROBE state may be reduced to T_{CEV} for all class events.

When the PSE is in MARK_EV1, MARK_EV1_PRI, MARK_EV1_SEC, MARK_EV2, MARK_EV2_PRI, MARK_EV2_SEC, MARK_EV3, MARK_EV3_PRI, MARK_EV3_SEC, or MARK_EV4, it shall provide to the PI or pairset V_{Mark}. The timing specification shall be as defined by T_{ME1}.

When a PSE is in MARK_EV_LAST, MARK_EV_LAST_PRI or MARK_EV_LAST_SEC, it shall provide to the PI or pairset V_{Mark}. The timing specification shall be as defined by T_{ME2}.

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The V_{Mark} requirement is to be met with load currents in the range of I_{Mark} as defined in Table 145–25.

NOTE—In a properly operating system, the port may or may not discharge to the V_{Mark} range due to the combination of the overall channel and PD capacitance and PD current loading. This is normal and acceptable system operation. For compliance testing, it is necessary to discharge the port in order to observe the V_{Mark} voltage. Discharge can be accomplished with a 2 mA load for 3 ms, after which V_{Mark} can be observed with minimum and maximum load current.

If any measured I_{Class} is equal to or greater than I_{Class_LIM} min, a PSE returns to IDLE, IDLE_PRI, or IDLE_SEC as appropriate. The PSE shall limit class event currents to I_{Class_LIM} and shall limit mark event currents to I_{Mark_LIM}.

All class event voltages and mark event voltages shall have the same polarity as defined for V_{Port_PSE-2P} in 145.2.4. PSEs may issue class events on one or both pairsets, when connected to a single-signature PD and operating over 4 pairs. The PSE shall complete Multiple-Event Physical Layer classification and transition to POWER_ON, POWER_ON_PRI, or POWER_ON_SEC without allowing the voltage at the PI or pairset to go below V_{Mark} min, unless in CLASS_RESET, CLASS_RESET_PRI, or CLASS_RESET_SEC. If the PSE returns to IDLE, it shall maintain the PI voltage in the range of V_{Reset} for a period of at least T_{Reset} min before starting a new detection cycle. If the PSE returns to IDLE_PRI or IDLE_SEC, it shall maintain the PI voltage on the corresponding pairset in the range of V_{Reset} for a period of at least T_{Reset} min before starting a new detection cycle. If the PSE is in any of the CLASS_RESET states it shall maintain the PI or pairset voltage in the range of V_{Reset} for a period of at least T_{Reset} min.

A PSE that implements 4PID based on Physical Layer classification and is restricted to Class 3 power or less, when connected to a dual-signature PD, shall issue three initial class events to determine the Type of the connected PD, then transition to either CLASS_RESET_PRI or CLASS_RESET_SEC.

145.2.8.2 Autoclass (optional)

PSEs may implement an extension of Physical Layer classification known as Autoclass. The purpose of Autoclass is to allow the PSE to determine the actual maximum power draw of the connected PD. Autoclass is only defined for single-signature PDs. See Figure 145B–15 for Autoclass timing diagrams.

If the PSE implements Autoclass it shall measure $P_{Autoclass}$ when it reaches POWER_ON and pd_autoclass is TRUE. $P_{Autoclass}$ is the power provided by the PSE measured throughout the period bounded by T_{AUTO_PSE1} and T_{AUTO_PSE2}, defined in Table 145–15. P_{ac_margin}, defined in Table 145–15, is the minimum amount of power the PSE adds to $P_{Autoclass}$ in order to allocate enough power to cope with increases in the link section resistance due to temperature increase.

P_{ac_extra} is the minimum amount of additional power allocation (above $P_{Autoclass}$ and P_{ac_margin}) that a PSE allocates while providing power in 2-pair mode, when it performed the measurement of $P_{Autoclass}$ in 4-pair mode. This extra allocation covers the additional losses incurred by the increase in link section resistance in 2-pair mode. P_{ac_extra} does not apply for PSEs that performed the $P_{Autoclass}$ measurement in 2-pair mode.

T_{AUTO_PSE1} and T_{AUTO_PSE2} timing is referenced from the transition of POWER_UP to POWER_ON. The power consumption shall be defined as the highest average power measured throughout the period bounded by T_{AUTO_PSE1} and T_{AUTO_PSE2}. Average power is measured using a sliding window with a width in the range of T_{AUTO_Window} as defined in Table 145–15.

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Table 145–15—Autoclass electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional information
1	Autoclass power measurement start	T_{AUTO_PSE1}	ms	1400	1600	Measured from the transition of POWER_UP to POWER_ON
2	Autoclass power measurement end	T_{AUTO_PSE2}	ms	3100	3500	
3	Autoclass average power sliding window width	T_{AUTO_Window}	ms	150	300	—
4	Autoclass power margin per the assigned Class					—
	Class 1 to 4	P_{ac_margin}	W	0.5	—	
	Class 5 to 6			0.75	—	
	Class 7 to 8			1.5	—	

145.2.9 4PID requirements

PSEs determine whether an attached PD is a candidate to receive power on both pairsets prior to applying operating voltage to both pairsets. This determination is referred to as 4PID. 4PID is a logical function of the detection state of both pairsets, the result of connection check as described in 145.2.7, and mutual identification. The variable pd_4pair_cand, defined in 145.2.5.4, contains the result of this determination.

A PSE shall not apply 4-pair power unless the PSE has detected a valid detection signature on both pairsets and one or more of the following conditions are met:

a) The connected PD is a single-signature PD.
b) The PSE detects a valid detection signature on the unpowered pairset when power is provided in 2-pair mode.
c) The PSE has identified the PD as Type 3 or Type 4.

145.2.10 Power supply output

When the PSE provides power to the PI, it shall conform with Table 145–16. Table 145–16 values support worst-case operating conditions. These ranges may be narrowed when additional information is known and applied in accordance with this specification. Power may be removed from both pairsets any time power is removed from one pairset.

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Table 145–16—PSE output PI electrical requirements for all PD Classes, unless otherwise specified

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
1	Output voltage per pairset in a power on state	V_{Port_PSE-2P}	V	50	57	3	See 145.2.10.1.
				52		4	
2	Pair-to-pair voltage difference	$V_{Port\_PSE\_diff}$	V	—	0.01	3, 4	See 145.2.10.2.
3	Output voltage during transient	$V_{Tran-2P}$	V	45.3	—	3	See 145.2.10.3.
				48.4	—	4	
4	Power feeding ripple and noise:						
	f < 500 Hz	V_{Noise}	V_{pp}	—	0.5	3, 4	See 145.2.10.5.
	500 Hz to 150 kHz				0.2		
	150 kHz to 500 kHz				0.15		
	500 kHz to 1 MHz				0.1		
5	Supported pair current to account for unbalance per the assigned Class (for single-signature PDs)						
	Class 1 to 4	$I_{Con-2P-unb}$	A	I_{Con}[a]	—	3, 4	See 145.2.10.6 and 145.2.10.6.1.
	Class 5			0.56	—	3, 4	
	Class 6			0.692	—	3, 4	
	Class 7			0.794	—	4	
	Class 8			0.948	—	4	
6	Total output current of both pairs of the same polarity during POWER_UP per the assigned Class						
	Single-signature PD, Class 1 to 4	I_{Inrush}	A	0.4	0.45	3, 4	See 145.2.10.7 and maximum value definition in Figure 145–22.
	Single-signature PD, Class 5 to 6			0.4	0.9	3, 4	
	Single-signature PD, Class 7 to 8			0.8	0.9	4	
7	Current per pairset during power up per the assigned Class						
	Single-signature PD, Class 1 to 4	$I_{Inrush-2P}$	A	—	0.45	3, 4	See 145.2.10.7 and maximum value definition in Figure 145–22.
	Single-signature PD, Class 5 to 6			—	0.6	3, 4	
	Single-signature PD, Class 7 to 8			—	0.6	4	
	Dual-signature PD, Class 1 to 4			0.4	0.45	3, 4	
	Dual-signature PD, Class 5			0.4	0.45	4	
8	Inrush time	T_{Inrush}	ms	50	75	3, 4	See 145.2.10.7.

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Table 145–16—PSE output PI electrical requirements for all PD Classes, unless otherwise specified *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
9	Overload current per pairset detection range	I_{CUT-2P}	A	I_{Con-2P}	—	3, 4	Optional limit; see 145.2.10.6, 145.2.10.8, Table 145–11.
10	Overload time limit	T_{CUT}	ms	50	75	3, 4	See 145.2.10.9.
11	Output current per pairset – at short circuit condition, per the assigned Class, single-signature PD						
	Class 1 to 3	I_{LIM-2P}	A	0.4	See info	3, 4	See 145.2.10.9. Max value defined by Figure 145–23 and Figure 145–24.
	Class 4			0.684[b]		3, 4	
	Class 5			0.58		3, 4	
	Class 6			0.72		3, 4	
	Class 7			0.85		4	
	Class 8			1.005		4	
	Output current per pairset – at short circuit condition, per the assigned Class, dual-signature PD						
	Class 1 to 3	I_{LIM-2P}	A	0.4	See info	3, 4	See 145.2.10.9. Max value defined by Figure 145–23 and Figure 145–24.
	Class 4			0.684		3, 4	
	Class 5			0.99		4	
12	Short circuit time limit	T_{LIM}	ms	10	75	3	See 145.2.10.1 and 145.2.10.9.
				6		4	
13	PSE Type power	P_{Type}	W	4	—	3	See 145.2.10.13
				75	99.9	4	
14	Power turn on time	T_{pon}	ms	—	400	3, 4	See 145.2.10.14.
15	Turn on rise time per pairset	T_{Rise}	ms	0.015	—	3, 4	See 145.2.10.1
16	Turn off time per pairset	T_{Off}	ms	—	500	3, 4	See 145.2.10.10.
17	Turn off voltage per pairset	V_{Off}	V	—	2.8	3, 4	See 145.2.10.11.
18	Unpowered negative pair reverse current						
	Highest $V_{PSE} > 21$ V	I_{rev}	A	—	0.0013	3, 4	See 145.2.10.4, 145.3.8.8.
	Highest $V_{PSE} \leq 21$ V				0.0005		

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Table 145–16—PSE output PI electrical requirements for all PD Classes, unless otherwise specified *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
19	DC MPS current on at least one pairset, per the assigned Class						See 145.2.12.
	Single-signature PD, Class 1 to 4, 2-pair	$I_{Hold-2P}$	A	0.004	0.009	3, 4	
	Single-signature PD, Class 1 to 4, 4-pair			0.002	0.005		
	Single-signature PD, Class 5 to 8			0.002	0.007		
	DC MPS current on each pairset						
	Dual-signature PD	$I_{Hold-2P}$	A	0.002	0.007	3, 4	
20	DC MPS total current on both pairs of the same polarity, per the assigned Class						See 145.2.12.
	Single-signature PD, Class 1 to 4	I_{Hold}	A	0.004	0.009	3, 4	
	Single-signature PD, Class 5 to 8			0.004	0.014	3, 4	
21	PD MPS dropout time limit	T_{MPDO}	ms	320	400	3,4	See 145.2.12.
22	PD MPS time for validity	T_{MPS}	ms	6	—	3,4	See 145.2.12.
23	Alternative B detection backoff time	T_{dbo}	ms	2000	—	3, 4	—
24	Detection timing	T_{det}	ms	—	500	3, 4	Time to complete detection on a pairset.
25	Error delay timing	T_{ed}	ms	750	—	3, 4	See 145.2.10.15

[a] The $I_{Con-2P-unb}$ value is higher than the value for Class 5 as unbalance for Class 4 is not restricted.
[b] Unbalance at Class 4 is not restricted. The I_{LIM-2P} value is higher than the value for Class 5 for PSEs operating in 4-pair mode.

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145.2.10.1 Output voltage in the power on states

The specification for $V_{Port\_PSE\text{-}2P}$ in Table 145–16 shall be met with a load step of (I_{Hold} max × $V_{Port\_PSE\text{-}2P}$ min) to the maximum power per the PSE's assigned Class at a rate of change of up to 15 mA/µs. The voltage transients as a result of load changes up to 35 mA/µs shall be limited to 3.5 V/µs.

A PSE that has assigned Class 1 to 4 to a single-signature PD and is in a power on state may transition between 2-pair and 4-pair power at any time, including after the expiration of T_{pon}. A PSE that has assigned Class 5 to 8 to a single-signature PD shall apply power to both pairsets while in POWER_ON.

T_{Rise}, as defined in Table 145–16, is referenced from 10% to 90% of the voltage difference between the positive and the negative conductors of a pairset in a power on state from the beginning of a power up state.

145.2.10.2 Output voltage pair-to-pair difference

$V_{Port\_PSE\_diff}$, as defined in Table 145–16, is the maximum voltage difference between pairs with the same polarity, at no load condition, when operating over 4 pairs, in a power on state.

145.2.10.3 Voltage transients

A PSE shall maintain an output voltage no less than $V_{Tran\text{-}2P}$ for transient conditions lasting more than 30 µs and less than 250 µs, and meet the requirements of 145.2.10.9. Transients less than 30 µs in duration may cause the voltage at the PI to fall below $V_{Tran\text{-}2P}$. See 145.3.8.6 for PD transient requirements. Transients lasting more than 250 µs shall meet the $V_{Port\_PSE\text{-}2P}$ specification.

NOTE—The occurrence of voltage transients lasting more than 250 µs or voltage steps of significant amplitude (within the $V_{Port\_PSE\text{-}2P}$ specification) should be limited to rare circumstances such as those involving switchover of backup power supplies or those involving significant change in current demand on the PSE power supply due to a large load step spread over multiple powered ports.

145.2.10.4 Reflected voltage

When a 4-pair capable PSE provides power in 2-pair mode, whereby two pairs are connected to the positive V_{PSE}, and one pair is connected to the negative V_{PSE}, a single-signature PD may reflect a voltage of up to V_{PSE} back onto the unpowered pairset. See 145.3.8.8. This can cause a reverse current, I_{rev} as defined in Table 145–16, to flow. Reverse current is current flowing out of the PSE on a negative pair.

The PSE shall not source a current higher than I_{rev}, as defined in Table 145–16, on a negative pair. This requirement holds only when no power is being sourced into the PSE.

145.2.10.5 Power feeding ripple and noise

V_{Noise}, the specification for power feeding ripple and noise in Table 145–16, shall be met for common-mode and pair-to-pair noise values at all static PSE output voltages. The limits are meant to preserve data integrity. To meet EMI standards, lower values may be needed. For higher frequencies, see 145.4.4, 145.4.5, and 145.4.6.

145.2.10.6 Continuous current capability in the power on states

$I_{Port\text{-}2P}$ and $I_{Port\text{-}2P\text{-}other}$ are the currents on the negative pairs and are defined in Equation (145–5) and in Equation (145–6).

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$$I_{\text{Port-2P}} = \left\{ \begin{array}{l} I_{\text{Port-2P-pri}} \text{ for the Primary Alternative} \\ I_{\text{Port-2P-sec}} \text{ for the Secondary Alternative} \end{array} \right\}_{\text{A}} \quad (145\text{–}5)$$

$$I_{\text{Port-2P-other}} = \left\{ \begin{array}{l} I_{\text{Port-2P-sec}} \text{ for the Primary Alternative} \\ I_{\text{Port-2P-pri}} \text{ for the Secondary Alternative} \end{array} \right\}_{\text{A}} \quad (145\text{–}6)$$

I_{Port} is the total current on both pairs with the same polarity and is defined in Equation (145–7).

$$I_{\text{Port}} = \{ I_{\text{Port-2P}} + I_{\text{Port-2P-other}} \}_{\text{A}} \quad (145\text{–}7)$$

where

$I_{\text{Port-2P-pri}}$ is the current supplied on the negative pair of the Primary Alternative
$I_{\text{Port-2P-sec}}$ is the current supplied on the negative pair of the Secondary Alternative

PSEs shall be able to supply $I_{\text{Con-2P}}$, the current the PSE supports on both pairs of each powered pairset, as defined in Equation (145–8). $I_{\text{Con-2P}}$ should be measured using a sliding window with a width of 1 second.

$$I_{\text{Con-2P}} = \left\{ \begin{array}{ll} P_{\text{Class}} / V_{\text{PSE}} & \text{when in 2-pair mode} \\ \min(I_{\text{Con}} - I_{\text{Port-2P-other}},\ I_{\text{Con-2P-unb}}) & \text{when 4-pair powering a single-signature PD} \\ P_{\text{Class-2P}} / V_{\text{PSE}} & \text{when 4-pair powering a dual-signature PD} \end{array} \right\}_{\text{A}} \quad (145\text{–}8)$$

where

P_{Class} is P_{Class} as defined in Equation (145–2)
$P_{\text{Class-2P}}$ is $P_{\text{Class-2P}}$ as defined in Equation (145–3)
V_{PSE} is the voltage across the pairset at the PSE PI as defined in 145.1.3
I_{Con} is the total current a PSE is able to source as defined in Equation (145–9)
$I_{\text{Con-2P-unb}}$ is the current a PSE is able to supply on each pair to account for pair-to-pair unbalance as defined in Table 145–16
$I_{\text{Port-2P-other}}$ is the current on the other negative pair as defined in Equation (145–6)

When powering a single-signature PD over 4 pairs, a PSE supports both:

— A total current of I_{Con}, defined in Equation (145–9), over both pairs with the same polarity;
— A minimum current of $I_{\text{Con-2P-unb}}$ on both the positive pair and the negative pair with the highest current to account for pair-to-pair unbalance.

$$I_{\text{Con}} = \left\{ \frac{P_{\text{Class}}}{V_{\text{PSE}}} \right\}_{\text{A}} \quad (145\text{–}9)$$

where

P_{Class} is P_{Class} as defined in Equation (145–2)
V_{PSE} is the voltage across the pairset at the PSE PI as defined in 145.1.3

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The PSE shall support the AC current waveform parameter $I_{Peak\text{-}2P}$, defined in Equation (145–10), on both pairs of each powered pairset, while within the operating voltage range of $V_{Port\_PSE\text{-}2P}$, for a minimum of T_{CUT} and a duty cycle of at least 5%.

$$I_{Peak\text{-}2P} = \left\{ \begin{array}{ll} I_{Peak} & \text{when in 2-pair mode} \\ \min(I_{Peak} - I_{Port\text{-}2P\text{-}other},\ I_{Peak\text{-}2P\text{-}unb}) & \text{when 4-pair powering a single-signature PD} \\ \dfrac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan\text{-}2P} \times P_{Peak\_PD\text{-}2P}}}{2 \times R_{Chan\text{-}2P}} & \text{when 4-pair powering a dual-signature PD} \end{array} \right\}_A \quad (145\text{–}10)$$

where

I_{Peak} is the total peak current a PSE supports per Equation (145–11)
$I_{Port\text{-}2P\text{-}other}$ is the current on the other negative pair as defined in Equation (145–6)
$I_{Peak\text{-}2P\text{-}unb}$ is the minimum peak current supported to account for unbalance, defined in Equation (145–12)
V_{PSE} is the voltage across the pairset at the PSE PI as defined in 145.1.3
$R_{Chan\text{-}2P}$ is the pairset loop resistance; this parameter has a worst-case value of R_{Ch} defined in 145.1.3 and Table 145–1
$P_{Peak\_PD\text{-}2P}$ is the peak power a dual-signature PD may draw per its assigned Class on a pairset; see Table 145–29

I_{Peak}, defined in Equation (145–11), is the total current of the powered pairs with the same polarity that a PSE supports, when powering a PD over 2 pairs or powering a single-signature PD over 4 pairs.

$$I_{Peak} = \left\{ \frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan} \times P_{Peak\_PD}}}{2 \times R_{Chan}} \right\}_A \quad (145\text{–}11)$$

where

V_{PSE} is the voltage across the pairset at the PSE PI as defined in 145.1.3
R_{Chan} is the link section loop resistance as defined in 145.1.3
P_{Peak_PD} is the total peak power a PD may draw for its Class; see Table 145–29

$I_{Peak\text{-}2P\text{-}unb}$, defined in Equation (145–12), is the minimum current that a PSE is able to supply on both the positive pair and the negative pair with the highest current, when powering a single-signature PD over 4 pairs.

$$I_{Peak\text{-}2P\text{-}unb} = \{I_{LIM\text{-}2P} - 0.002\}_A \quad (145\text{–}12)$$

where

$I_{LIM\text{-}2P}$ is the $I_{LIM\text{-}2P}$ min value per pairset for the PSE, as defined in Table 145–16

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145.2.10.6.1 PSE pair-to-pair current unbalance

When a PSE supplies power to a PD using all 4 pairs, the current may not equally divide between the pairs that are at the same polarity. This is referred to as pair-to-pair current unbalance. The degree to which the current is unbalanced depends on the specific combination of PSE, cabling, and PD.

The maximum pair current in a system depends on the assigned Class (see 145.2.8), and is defined in Table 145–17.

Table 145–17—Maximum pair-to-pair current unbalance

Parameter	Assigned Class	Unit	Value
$I_{Unbalance\text{-}2P}$	1 to 4	A	I_{Con} [a]
	5 to 8		$I_{Con\text{-}2P\text{-}unb} - 0.01$

[a] Unbalance current for these assigned Classes is not restricted.

PSEs that operate over 4 pairs are subject to unbalance requirements. The contribution of PSE PI pair-to-pair effective resistance unbalance to the system end-to-end effective resistance unbalance is specified by PSE maximum (R_{PSE_max}) and minimum (R_{PSE_min}) common-mode effective resistance in the powered pairs of same polarity, see Figure 145A–1. Effective resistances of R_{PSE_min} and R_{PSE_max} include the effects of $V_{Port\_PSE\_diff}$ as defined in Table 145–16 and the PSE PI resistive elements. See definition and measurements in Annex 145A.

The PSE PI pair-to-pair effective resistance unbalance determined by R_{PSE_max} and R_{PSE_min}, along with any other parts of the system, i.e., the cabling and the PD, bounds the current such that the pair with the highest current including unbalance does not exceed $I_{Unbalance\text{-}2P}$ as defined in Table 145–17 during normal operating conditions. $I_{Unbalance\text{-}2P}$ is the highest pair current in case of maximum unbalance and will be higher than $I_{Con} / 2$. $I_{Unbalance\text{-}2P}$ applies to link section common-mode pair resistances from 0.2 Ω to R_{Ch}, as defined in 145.1.3.

R_{PSE_max} and R_{PSE_min} are specified and measured under maximum P_{Class_PD} load conditions, measured at the PD PI, over the $V_{Port\_PSE\text{-}2P}$ operating range. R_{PSE_max} and R_{PSE_min} for the positive pairs are not necessarily the same values as for the negative pairs.

PSEs that meet R_{PSE_min} and R_{PSE_max}, as defined by Equation (145–13) meet the unbalance requirements under worst case conditions of link section pair to pair unbalance and PD PI pair to pair unbalance. Equation (145–13) is only applicable for R_{PSE_min} up to a value of 1 Ω for Class 5 and Class 6, and 0.5 Ω for Class 7 and Class 8.

$$0 < R_{PSE\_max} \leq \left\{ \begin{array}{ll} 2.182 \times R_{PSE\_min} - 0.04 & \text{for Class 5} \\ 1.999 \times R_{PSE\_min} - 0.04 & \text{for Class 6} \\ 1.904 \times R_{PSE\_min} - 0.03 & \text{for Class 7} \\ 1.832 \times R_{PSE\_min} - 0.03 & \text{for Class 8} \end{array} \right\}_{\Omega} \quad (145\text{–}13)$$

where

R_{PSE_max} is, given R_{PSE_min}, the highest supported common-mode effective resistance in the powered pairs of the same polarity

R_{PSE_min} is the lower PSE common-mode effective resistance in the powered pairs of the same polarity

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R_{PSE_min} or R_{PSE_max} common-mode effective resistance is the resistance of the two internal conductors (including the internal components on each conductor) in a powered pair of the same polarity connected in parallel.

A PSE shall not source more than $I_{Unbalance\text{-}2P}$ on any pair when connected to a load as shown in Figure 145–21, using values of R_{load_min} and R_{load_max} as defined in Equation (145–14) and Equation (145–15). This unbalance current requirement applies at the PSE PI connector (jack) when mated with a specified balanced cabling connector (plug).

R_{load_min} and R_{load_max}, defined in Equation (145–14) and Equation (145–15), are respectively the minimum and maximum common-mode effective load resistances in the powered pairs of the same polarity.

Table 145–18 specifies the resistance values used to compute R_{load_min} and R_{load_max} according to Equation (145–14) and Equation (145–15). The load resistances R_{load_min} and R_{load_max} are split into two series resistances R_{load1_min} and R_{load2_min}, and R_{load1_max} and R_{load2_max} respectively, as shown in Figure 145–21, so the power sink can be set such that the power consumption inside the P_{load} box equals P_{Class_PD}.

$$R_{load\_min} = R_{load1\_min} + R_{load2\_min} \quad (145\text{–}14)$$

$$R_{load\_max} = R_{load1\_max} + R_{load2\_max} \quad (145\text{–}15)$$

where

R_{load1_max} is, given R_{load1_min}, the higher resistance value representing the link section resistance
R_{load1_min} is the lower resistance representing the link section resistance
R_{load2_max} is, given R_{load2_min}, the higher resistance value representing the PD contribution to unbalance
R_{load2_min} is the lower resistance representing the PD contribution to unbalance

Table 145–18—PSE unbalance test fixture resistances

PSE Class	R_{load1_min} (Ω)	R_{load1_max} (Ω)	R_{load2_min} (Ω)	R_{load2_max} (Ω)	Additional information
5	0.087	0.101	0.638	1.518	Low link section resistance conditions.
6			0.538	1.183	
7			0.483	1.017	
8			0.439	0.894	
5	5.41	6.25	0.704	1.026	High link section resistance conditions.
6			0.564	0.822	
7			0.491	0.717	
8			0.43	0.629	

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The values for $I_{Unbalance\text{-}2P}$ and the relation between R_{PSE_max} and R_{PSE_min}, as defined in Equation (145–13), are valid given that $R_{Chan\text{-}2P}$ (see 145.1.3) ranges from 0.2 Ω to 12.5 Ω. See 145A.4 for guidelines on how to support low resistance link sections.

Figure 145–21 shows a verification circuit for the PSE current unbalance requirements measurement. Other methods for measuring R_{PSE_min} and R_{PSE_max} are described in Annex 145A.

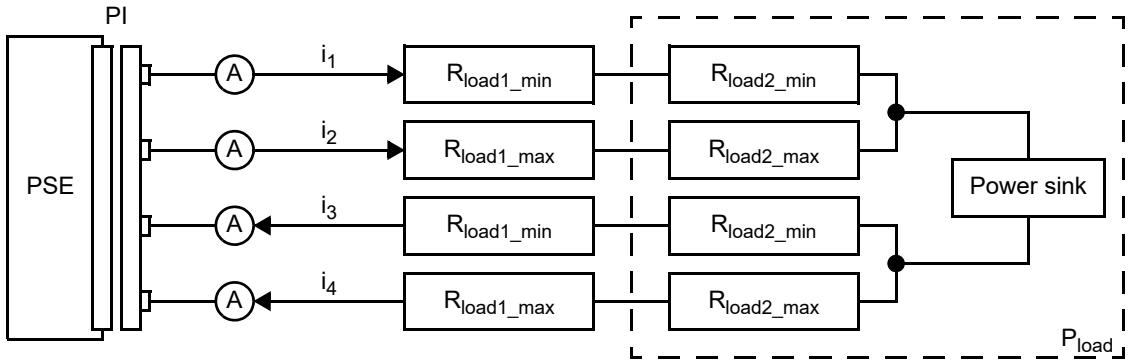

Figure 145–21—PSE current unbalance verification circuit

The evaluation method is as follows:

a) Use R_{load_min} and R_{load_max} from Equation (145–14) and Equation (145–15) for low channel resistance conditions.
b) Adjust the power sink such that P_{load} (the power consumed by the R_{load2} resistances and the power sink) equals P_{Class_PD} for the given Class.
c) Verify that currents i_1, i_2, i_3, and i_4 are lower than $I_{Unbalance\text{-}2P}$, as defined in Table 145–17.
d) Exchange R_{load_max} and R_{load_min}. Repeat steps b) and c).
e) Repeat steps b) through d) for R_{load_min} and R_{load_max} components from Equation (145–14) and Equation (145–15) for high channel resistance conditions.

145.2.10.7 Current during power up

Power up occurs on each pairset between the transition to a power up state on that pairset and the expiration of T_{Inrush}. A PSE that provides current on both pairsets during POWER_UP shall complete power up within T_{Inrush} max, starting when the first pairset exceeds a voltage of 30 V. PSEs that have assigned Class 1 through 6 to a single-signature PD may perform inrush over 2 pairs or over 4 pairs. PSEs that have assigned Class 5 or Class 6 to a single-signature PD transition to 4-pair mode by T_{Inrush}. PSEs that have assigned Class 7 or Class 8 to a single-signature PD perform inrush over 4 pairs.

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The PSE shall limit the current on each powered negative pair to $I_{Inrush\text{-}2P}$ and the total current on the negative pairs to I_{Inrush} during power up per the requirements of Table 145–16, with the exception of the initial per pairset transient described in Equation (145–16).

$$I_{PSEIT\text{-}2P}(t) = \left\{ \begin{array}{ll} I_{Inrush\text{-}2P}\text{max} & \text{for } 0 \le t < t_0 \\ 50 & \text{for } t_0 \le t < (t_0 + 10\times10^{-6}) \\ I_{Inrush\text{-}2P}\text{max} + \dfrac{(50 - I_{Inrush\text{-}2P}\text{max}) \times (0.001 + t_0 - t)}{99\times10^{-5}} & \text{for } (t_0 + 10\times10^{-6}) \le t < (t_0 + 0.001) \\ I_{Inrush\text{-}2P}\text{max} & \text{for } (t_0 + 0.001) \le t < 0.075 \end{array} \right\}_A \quad (145\text{–}16)$$

where

t is the time in seconds

$I_{Inrush\text{-}2P}$ max is the maximum value of $I_{Inrush\text{-}2P}$ as defined in Table 145–16

t_0 is the time when $I_{Port\text{-}2P}$ exceeds $I_{Inrush\text{-}2P}$ max for the first time during the power up states. The range for t_0 is $0 \le t_0 \le 49$ ms.

The PSE inrush maximum limit, $I_{PSEIT\text{-}2P}$, shown in Figure 145–22, is defined by Equation (145–16).

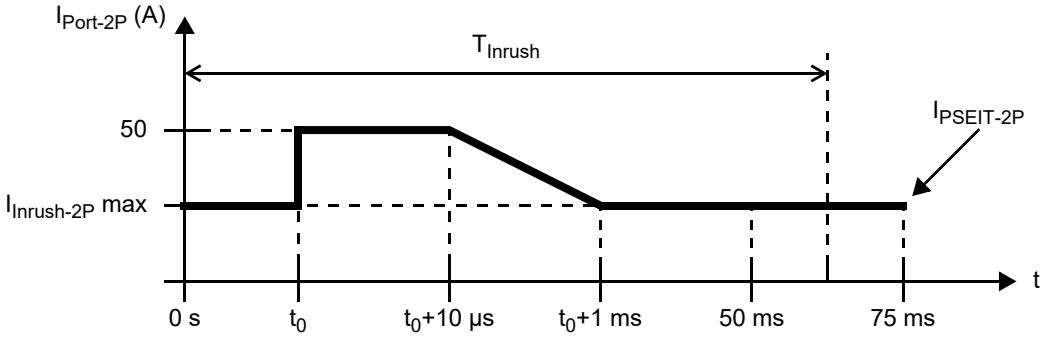

Figure 145–22—Per pairset PSE inrush maximum current

The minimum I_{Inrush} and $I_{Inrush\text{-}2P}$ current capability as defined in Table 145–16 applies when V_{PSE} exceeds 30 V. During a power up state, the PSE shall support the following:

— When powering a single-signature PD, a minimum I_{Inrush} of 5 mA when V_{PSE} is between 0 V and 10 V, and 60 mA when V_{PSE} is between 10 V and 30 V.

— When powering a dual-signature PD, a minimum $I_{Inrush\text{-}2P}$ of 5 mA when V_{PSE} is between 0 V and 10 V, and 60 mA when V_{PSE} is between 10 V and 30 V.

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145.2.10.8 Overload current

If the current on either pair of a pairset exceeds $I_{CUT\text{-}2P}$ for longer than T_{CUT}, the PSE may remove power from that pairset. The cumulative duration of T_{CUT} is measured using a sliding window of at least 1 second width.

145.2.10.9 Short circuit current

The PSE shall limit the pairset current to $I_{LIM\text{-}2P}$ for a duration of at least T_{LIM} min, when V_{PSE} is in the range of $V_{Port\_PSE\text{-}2P}$. The cumulative duration of the current limit event may be measured with a sliding window of at most 1 second width.

The maximum value of $I_{LIM\text{-}2P}$ is the PSE upperbound template described by Equation (145–17), Equation (145–18), Figure 145–23, and Figure 145–24. The $I_{LIM\text{-}2P}$ minimum value in Table 145–16 for Class 5 and above includes the effective system end-to-end resistance unbalance effect.

The PSE shall remove power from a pairset before a current limit event persists on that pairset continuously for T_{LIM} max as defined in Table 145–16.

A PSE in a power on state may remove power from a pairset without regard to T_{LIM} when the voltage on that pairset no longer meets the $V_{Port\_PSE\text{-}2P}$ specification for longer than 250 μs or the voltage no longer meets the $V_{Tran\text{-}2P}$ specification.

If $I_{Port\text{-}2P}$ exceeds the PSE lowerbound template, the PSE output voltage may drop below $V_{Port\_PSE\text{-}2P}$ min.

A PSE may remove power from the PI if the current on any pair exceeds the “PSE lowerbound template” in Figure 145–23 or Figure 145–24. Power shall be removed from a pairset of a PSE before the pairset current exceeds the “PSE upperbound template” in Figure 145–23 or Figure 145–24. When connected to a single-signature PD, the PSE should remove power from both pairsets before the current exceeds the “PSE upperbound template” on either pairset.

The right side vertical axis in Figure 145–23 and Figure 145–24 indicates the total current over both pairsets when the PSE supplies 4-pair power to a single-signature PD.

— For Type 3 PSEs, Figure 145–23, Equation (145–17) and Equation (145–19) apply.
— For Type 4 PSEs, Figure 145–24, Equation (145–18) and Equation (145–20) apply.

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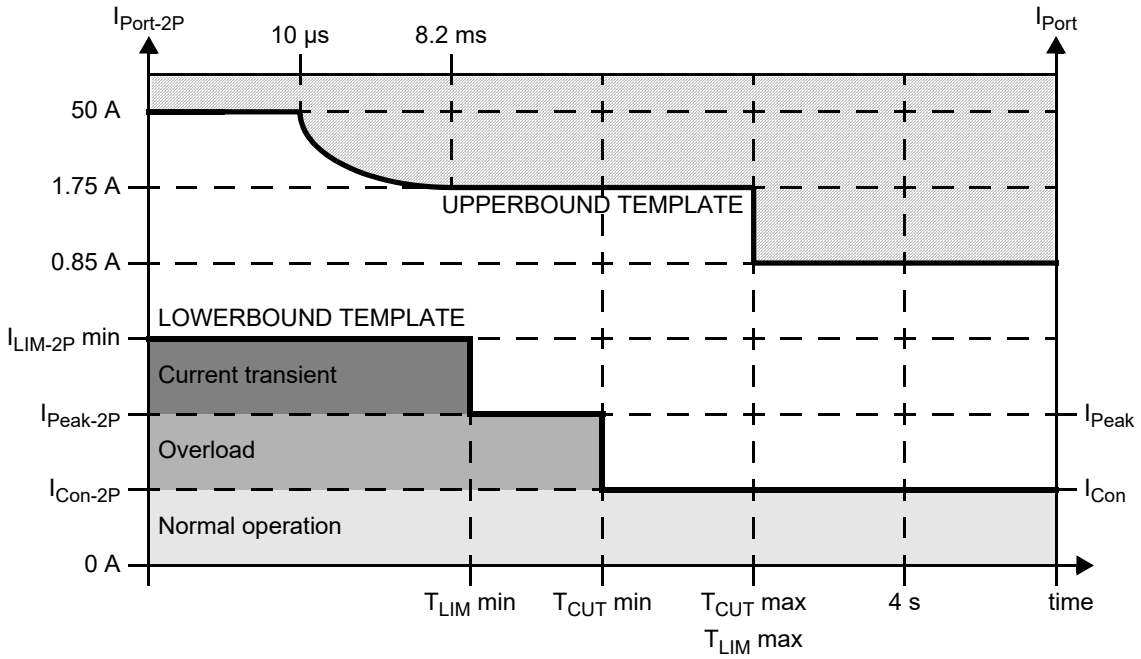

Figure 145–23—Power on states, per pairset operating current template for Type 3 PSEs

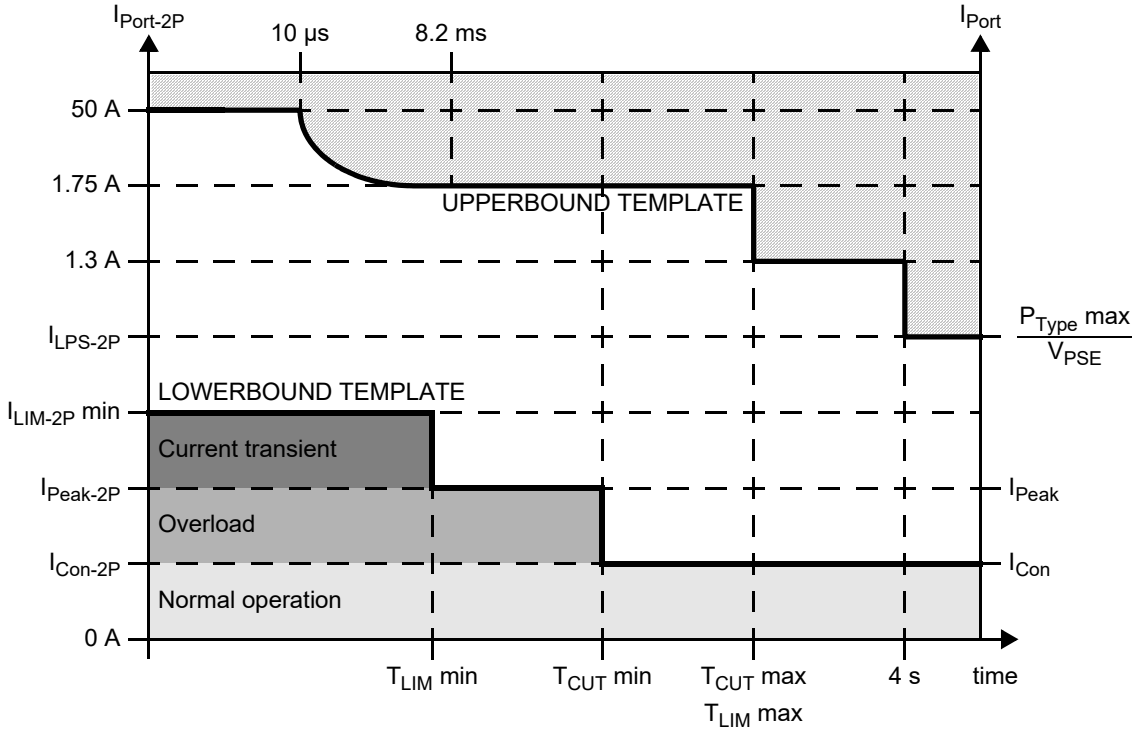

Figure 145–24—Power on states, per pairset operating current template for Type 4 PSEs

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The PSE upperbound templates, $I_{PSEUT\text{-}Type3\text{-}2P}$ and $I_{PSEUT\text{-}Type4\text{-}2P}$, are defined by the following segments:

$$I_{PSEUT\text{-}Type3\text{-}2P}(t) = \left\{ \begin{array}{ll} 50 & \text{for } (0 \le t < 10\times10^{-6}) \\ \sqrt{\frac{K}{t}} & \text{for } (10\times10^{-6} \le t < 8.2\times10^{-3}) \\ 1.75 & \text{for } (8.2\times10^{-3} \le t < T_{CUT}\text{max}) \\ 0.85 & \text{for } (T_{CUT}\text{max} \le t) \end{array} \right\}_A \quad (145\text{–}17)$$

$$I_{PSEUT\text{-}Type4\text{-}2P}(t) = \left\{ \begin{array}{ll} 50 & \text{for } (0 \le t < 10\times10^{-6}) \\ \sqrt{\frac{K}{t}} & \text{for } (10\times10^{-6} \le t < 8.2\times10^{-3}) \\ 1.75 & \text{for } (8.2\times10^{-3} \le t < T_{CUT}\text{max}) \\ 1.3 & \text{for } (T_{CUT}\text{max} \le t < 4) \\ I_{LPS\text{-}2P} & \text{for } (4 \le t) \end{array} \right\}_A \quad (145\text{–}18)$$

where

t	is the duration in seconds that the PSE sources $I_{Port\text{-}2P}$
K	is 0.025 A^2s, an energy limitation constant for the pairset current when it is not in steady state normal operation
T_{CUT} max	is T_{CUT} max per pairset, as defined in Table 145–16
$I_{LPS\text{-}2P}$	is the current defined in 145.2.10.13

The PSE lowerbound templates, $I_{PSELT\text{-}Type3\text{-}2P}$ and $I_{PSELT\text{-}Type4\text{-}2P}$, are defined by the following segments:

$$I_{PSELT\text{-}Type3\text{-}2P}(t) = \left\{ \begin{array}{ll} I_{LIM\text{-}2P}\text{min} & \text{for } (0 \le t < T_{LIM}\text{min}) \\ I_{Peak\text{-}2P} & \text{for } (T_{LIM}\text{min} \le t < T_{CUT}\text{min}) \\ I_{Con\text{-}2P} & \text{for } (T_{CUT}\text{min} \le t) \end{array} \right\}_A \quad (145\text{–}19)$$

$$I_{PSELT\text{-}Type4\text{-}2P}(t) = \left\{ \begin{array}{ll} I_{LIM\text{-}2P}\text{min} & \text{for } (0 \le t < T_{LIM}\text{min}) \\ I_{Peak\text{-}2P} & \text{for } (T_{LIM}\text{min} \le t < T_{CUT}\text{min}) \\ I_{Con\text{-}2P} & \text{for } (T_{CUT}\text{min} \le t) \end{array} \right\}_A \quad (145\text{–}20)$$

where

t	is the duration that the PI sources $I_{Port\text{-}2P}$
$I_{LIM\text{-}2P}$ min	is the $I_{LIM\text{-}2P}$ min value per pairset for the PSE as defined in Table 145–16
T_{LIM} min	is T_{LIM} min per pairset as defined in Table 145–16
T_{CUT} min	is T_{CUT} min per pairset, as defined in Table 145–16
$I_{Peak\text{-}2P}$	is the minimum peak current supported on each powered pair, as defined in Equation (145–12)
$I_{Con\text{-}2P}$	is the minimum supported continuous current on each powered pair as defined in 145.2.10.6

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145.2.10.10 Turn off time

The specification for T_{Off} in Table 145–16 shall apply to the discharge time from $V_{Port\_PSE\text{-}2P}$ min to V_{Off} of a pairset with a test resistor of 320 kΩ attached to that pairset. In addition, it is recommended that the pairset be discharged when operating voltage is not applied. T_{Off} ends when $V_{PSE} \leq V_{Off}$.

145.2.10.11 Turn off voltage

The voltage at the PI shall be equal or less than V_{Off}, as defined in Table 145–16, when the PSE is in DISABLED, IDLE, BACKOFF, or ERROR_DELAY. The voltage at the corresponding pairset shall be equal or less than V_{Off}, as defined in Table 145–16, when the PSE is in IDLE_PRI, WAIT_PRI, ERROR_DELAY_PRI, IDLE_SEC, WAIT_SEC, or ERROR_DELAY_SEC.

145.2.10.12 Intra-pair current unbalance

The PSE shall support an intra-pair current unbalance of I_{unb}, as defined in Equation (145–21). The intra-pair current unbalance is the current unbalance between the two conductors of a power pair over the current load range.

$$I_{unb} = \{3\% \times I_{Peak\text{-}2P\text{-}unb\_max}\}_A \quad (145\text{–}21)$$

A 100BASE-TX transmitter in a Type 3 or Type 4 Endpoint PSE shall meet the requirements of 25.4.5 in the presence of (I_{unb} / 2).

145.2.10.13 Type power

P_{Type} min is the minimum power a PSE is capable of sourcing.

Type 4 PSEs shall not source more power than P_{Type} max, as defined in Table 145–16, measured using a sliding window with a width up to 4 seconds. $I_{LPS\text{-}2P}$ is defined in Equation (145–22) and is the maximum current per pairset that results in less than P_{Type} max being sourced by the PSE.

$$I_{LPS\text{-}2P} = \left\{ \begin{array}{ll} 0.85 & \text{when in 2-pair mode} \\ \min\left(\frac{P_{Type}\text{max}}{V_{PSE}} - I_{Port\text{-}2P\text{-}other},\ 1.3 \right) & \text{when in 4-pair mode} \end{array} \right\}_A \quad (145\text{–}22)$$

where

P_{Type} max is the maximum power allowed for a given Type as defined in Table 145–16
V_{PSE} is the voltage across the pairset at the PSE PI as defined in 145.1.3
$I_{Port\text{-}2P\text{-}other}$ is the output current on the other pairset (see 145.2.10.6)

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145.2.10.14 Power turn on time

The specification for T_{pon} in Table 145–16 applies to the PSE power up time for a PD after completion of detection.

PSEs, when connected to a single-signature PD, shall reach POWER_ON within T_{pon} after completing detection on the last pairset. When connected to a dual-signature PD, PSEs shall reach the respective power on state for a pairset within T_{pon} after completing detection on the same pairset.

145.2.10.15 Error delay timing

T_{ed}, defined in Table 145–16, is the minimum delay time before a PSE may attempt subsequent powering of a pairset after power removal from that pairset because of an error condition.

145.2.10.16 PSE stability

When connected together as a system, the PSE and PD might exhibit instability at the PSE side or the PD side or both due to the presence of negative impedance at the PD input. See Annex 33A for PSE design guidelines for stable operation.

145.2.11 Power supply allocation

A PSE does not initiate power provision to one or both pairsets if the PSE has less than Class 3 power available and the connected PD requests more than the available power.

The PSE may manage the allocation of power based on additional information beyond the classification of the attached PD. Allocating power based on additional information about the attached PD, and the mechanism for obtaining that additional information, is beyond the scope of this standard with the exception that the allocation of power shall not be based solely on the historical data of the power consumption of the attached PD.

See 145.5 for a description of Data Link Layer classification.

If the system implements a power allocation algorithm, no additional behavioral requirement is placed on the system as it approaches or reaches its maximum power subscription. Specifically, the interaction between one PSE PI and another PSE PI in the same system is beyond the scope of this standard.

145.2.12 PSE Maintain Power Signature (MPS) requirements

A PSE removes power when a connected PD no longer draws a minimum amount of current. This is referred to as the "Maintain Power Signature." The PSE state diagrams in Figure 145–17 and Figure 145–18 monitor for the absence of MPS.

A PSE, depending on the PD assigned Class and PD signature configuration, shall use the applicable I_{Hold}, $I_{Hold\text{-}2P}$, T_{MPS} and T_{MPDO} values as defined in Table 145–16. The specification for T_{MPS} in Table 145–16 applies only to the DC MPS component.

A PSE powering a PD over a single pairset

- Shall consider the DC MPS component to be present if $I_{Port\text{-}2P}$ is greater than or equal to $I_{Hold\text{-}2P}$ max continuously for a minimum of T_{MPS}.
- Shall consider the DC MPS component to be absent if $I_{Port\text{-}2P}$ is less than or equal to $I_{Hold\text{-}2P}$ min.
- May consider the DC MPS component to be either present or absent if $I_{Port\text{-}2P}$ is in the range of $I_{Hold\text{-}2P}$.

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— Shall remove power from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.
— Shall not remove power from the PI when DC MPS has been present within the $T_{MPS} + T_{MPDO}$ window. This allows a PD to minimize its power consumption.

A PSE powering a single-signature PD over both pairsets

— Shall consider the DC MPS component to be present if $I_{Port-2P}$ of the pairset with the highest current is greater than or equal to $I_{Hold-2P}$ max and I_{Port} is greater than or equal to I_{Hold} max continuously for a minimum of T_{MPS}.
— Shall consider the DC MPS component to be absent if $I_{Port-2P}$ of the pairset with the highest current is less than or equal to $I_{Hold-2P}$ min and I_{Port} is less than or equal to I_{Hold} min.
— May consider the DC MPS component to be either present or absent if $I_{Port-2P}$ of the pairset with the highest current is within the range of $I_{Hold-2P}$ or I_{Port} is within the range of I_{Hold}.
— Shall remove power from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.
— Shall not remove power from the PI when DC MPS has been present within the $T_{MPS} + T_{MPDO}$ window. This allows a PD to minimize its power consumption.

NOTE—The DC MPS requirements for PSEs connected to a single-signature PD are such that the PSE may measure either the total current over both pairsets (I_{Hold}), the current on the pairset with the highest current ($I_{Hold-2P}$), or both.

A PSE powering a dual-signature PD over both pairsets

— Shall consider the DC MPS component to be present or absent on each pairset independently.
— Shall consider the DC MPS component to be present on a pairset if $I_{Port-2P}$ is greater than or equal to $I_{Hold-2P}$ max continuously for a minimum of T_{MPS}.
— Shall consider the DC MPS component to be absent on a pairset if $I_{Port-2P}$ is less than or equal to $I_{Hold-2P}$ min.
— May consider the DC MPS component on a pairset to be either present or absent if $I_{Port-2P}$ is within the range of $I_{Hold-2P}$.
— Shall remove power from a pairset when DC MPS has been absent on that pairset for a duration greater than T_{MPDO}.
— Shall not remove power from a pairset when DC MPS has been present on both pairsets within the $T_{MPS} + T_{MPDO}$ window.
— May maintain power on a pairset when DC MPS has been present on that pairset within the $T_{MPS} + T_{MPDO}$ window. This allows a PD to minimize its power consumption.

145.3 Powered devices (PDs)

A PD is the portion of a device that is either drawing power or requesting power by participating in the PD detection algorithm. A device that is capable of becoming a PD may have the ability to draw power from an alternate power source. A PD requiring power from the PI may simultaneously draw power from an alternate power source. PD capable devices that are neither drawing nor requesting power are also covered in this subclause.

A PD is specified at the point of the physical connection to the cabling. Characteristics such as the losses due to voltage correction circuits, power supply inefficiencies, separation of internal circuits from external ground or other characteristics induced by circuits after the PI connector are not specified. Limits defined for the PD are specified at the PI, not at any point internal to the PD, unless specifically stated.

Additional electrical specifications that apply to the PD are specified in 145.4.

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145.3.1 PD Type descriptions

PDs can be categorized as either Type 1, Type 2, Type 3, or Type 4. See 33.3 for the specification of Type 1 and Type 2 PDs. PDs can be implemented as either a single-signature configuration or a dual-signature configuration as defined in 1.4 and 145.3.5 and shown in Table 145–19. Table 145–19 shows the supported parameters of PDs.

Table 145–19—PD supported parameters

PD Type	Signature configuration	PD Class	Physical Layer classification	Data Link Layer classification	Optional Capabilities
Type 3	Single	1 to 3	Multiple-Event	Optional	Autoclass
		4 to 6	Multiple-Event	Mandatory	Autoclass
	Dual	1 to 3	Multiple-Event	Optional	—
		4	Multiple-Event	Mandatory	—
Type 4	Single	7 to 8	Multiple-Event	Mandatory	Autoclass
	Dual	5	Multiple-Event	Mandatory	—

NOTE 1—See Table 145–26 and Table 145–27 for the allowed PD power for each Type and Class.
NOTE 2—Data Link Layer classification for dual-signature PDs is optional only if the PD requested Class on both Modes is less than or equal to 3.
NOTE 3—Type 4 dual-signature PDs request Class 5 on at least one pairset

145.3.2 PD PI

The PD's PI consists of 8 conductors. The two conductors associated with a pair are at the same nominal voltage. A pairset consists of two pairs, as defined in 145.2.4. The two pairsets are named Mode A and Mode B, which correspond with Alternative A and Alternative B. Figure 145–12 in conjunction with Table 145–20 illustrate the two power modes.

PDs shall be capable of accepting power in any valid 2-pair configuration and any valid 4-pair configuration as defined in Table 145–20.

A PD shall meet the requirements of detection (145.3.4), PD signature configuration (145.3.5), and PD classification (145.3.6) in any valid 2-pair configuration, as defined in Table 145–20.

NOTE—This includes configurations with two pairs connected to the same positive potential and one pair connected to the negative potential.

A single-signature PD shall meet all specifications related to current by meeting the specified total current, where total current is the combined current of the two pairs at the same polarity, unless otherwise noted (see 145.3.8.9). A dual-signature PD shall meet all specifications related to current by meeting the specified current on the negative pair of a given Mode, unless otherwise noted (see 145.3.8.9).

The PD shall be insensitive to the polarity of the voltage applied on each Mode regardless of the polarity of the voltage applied on the other Mode. Single-signature PDs that request Class 4 or less shall be able to operate if power is supplied with any valid configuration defined in Table 145–20. All other PDs may require being supplied with a valid 4-pair configuration to operate at their nominal power level.

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NOTE—PDs that support only Mode A or Mode B are specifically not allowed by this standard. PDs that are sensitive to polarity are specifically not allowed by this standard.

PDs interoperate with Type 1, Type 2, Type 3, and Type 4 PSEs, subject to power limitations. See 145.3.6.

The PD shall not source power on its PI.

The PD shall withstand any voltage from 0 V to 57 V applied to the PD PI per any of the valid configurations defined in Table 145–20 indefinitely without permanent damage.

Table 145–20—PD input power configurations

Pairsets	**Mode A**		**Mode B**	
Pairs	**Pair 1**	**Pair 2**	**Pair 3**	**Pair 4**
Conductor	**1 and 2**	**3 and 6**	**4 and 5**	**7 and 8**
	Valid 2-pair configurations			
	P	N	—	—
	N	P	—	—
	—	—	P	N
	—	—	N	P
	P	N	P	—
	P	N	—	P
	N	P	P	—
	N	P	—	P
	P	—	P	N
	—	P	P	N
	P	—	N	P
	—	P	N	P
	Valid 4-pair configurations			
	N	P	N	P
	N	P	P	N
	P	N	N	P
	P	N	P	N

N denotes a pair connected to negative potential
P denotes a pair connected to positive potential
— denotes a pair not connected to a supply rail
PSEs are required to switch the negative pairs, and may switch the positive pairs as defined in 145.4.1.1.1. This may lead to both positive pairs providing current in 2-pair mode.

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145.3.3 PD state diagrams

The PD state diagrams specify the externally observable behavior of a PD.

145.3.3.1 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in 145.2.5.2.

145.3.3.2 Mode designation

Dual-signature PDs are implemented on Mode A and Mode B as defined in 145.3.2. Mode information is obtained by replacing the X in the desired variable or function with the letter of the Mode of interest. Modes are referred to in general as follows:

X
: Generic Mode designator. When X is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams.
Values:
A: Mode A
B: Mode B

145.3.3.3 Single-signature PD state diagrams

Single-signature PDs shall provide the behavior of the state diagram shown in Figure 145–25 and Figure 145–26.

145.3.3.3.1 Constants

$I_{Inrush\_PD\_max}$
: The maximum PD inrush current I_{Inrush_PD} max (see Table 145–29)

$V_{Off\_PD\_min}$
: The minimum PD off voltage V_{Off_PD} min (see Table 145–29)

$V_{Reset\_PD\_max}$
: The maximum PD reset voltage V_{Reset_PD} max (see Table 145–25)

145.3.3.3.2 Variables

I_{Port}
: is the total PD input current as defined in 145.1.3.

mdi_power_required
: A variable indicating the PD is enabled and should request power from the PSE by applying a PD detection signature to the PI, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. This variable may be set by the PD at any time.
Values:
FALSE: PD functionality is disabled.
TRUE: PD functionality is enabled.

nopower
: A variable that indicates the PD has been in POWEROFF, which indicates V_{PD} was below V_{Off_PD} while being powered, since the last time V_{PD} was below V_{Reset} for at least T_{Reset}.
Values:
FALSE: The PD has not been in POWEROFF.
TRUE: The PD has been in POWEROFF.

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pd_acs_cancel

This variable indicates that the PD is aborting the Autoclass procedure. See 145.3.6.2.

Values:

FALSE: The PD does not abort the Physical Layer Autoclass procedure.

TRUE: The PD aborts the Physical Layer Autoclass procedure.

pd_acs_full_power

This variable indicates whether the PD is required to draw maximum power, $P_{Autoclass\_PD}$. See 145.3.6.2.

Values:

FALSE: The PD is not required to draw maximum power.

TRUE: The PD is required to draw maximum power for Autoclass measurement.

pd_acs_req

This variable indicates if a PD draws $P_{Autoclass\_PD}$ in the Autoclass time window after reaching POWERED. See 145.3.6.2.

Values:

FALSE: The PD does not request Autoclass.

TRUE: The PD requests Autoclass.

pd_autoclass_enable

A variable indicating that the PD is enabled to perform Autoclass by changing its class signature to class signature 0 during the first class event (see 145.3.6.2).

Values:

FALSE: Autoclass is disabled.

TRUE: Autoclass is enabled.

pd_dll_capable

This variable indicates whether the PD implements Data Link Layer classification.

Values:

FALSE: The PD does not implement Data Link Layer classification.

TRUE: The PD does implement Data Link Layer classification.

pd_dll_enable

A variable indicating whether the Data Link Layer classification mechanism is enabled.

Values:

FALSE: Data Link Layer classification is not enabled.

TRUE: Data Link Layer classification is enabled.

pd_inrush_lim

A variable indicating that the PD limits the inrush current below I_{Inrush_PD} and $I_{Inrush\_PD\text{-}2P}$ for the duration of the PD inrush time as defined in 145.3.8.3. This variable is set per this description.

Values:

FALSE: The PD does not limit the inrush current.

TRUE: The PD does limit the inrush current.

pd_max_power

A variable indicating the maximum power that the PD may draw from the PSE. See power classifications in Table 145–29.

Values:

inrush: There is no maximum power limit on the PD

0: The PD may draw up to 44 mA of current

1: PD may draw Class 1 power

2: PD may draw Class 2 power

3: PD may draw Class 3 power

4: PD may draw Class 4 power

5: PD may draw Class 5 power

6: PD may draw Class 6 power

7: PD may draw Class 7 power

8: PD may draw Class 8 power

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pd_overload

A variable that indicates if the PD is drawing peak power in excess of P_{Class_PD}, as defined in 145.3.8.4, or when the PD is exposed to a transient condition as defined in 145.3.8.6.

Values:

FALSE: The PD is not drawing peak power or is exposed to a transient condition.
TRUE: The PD is drawing peak power and is not exposed to a transient condition.

pd_power_update

A variable that is set when the PDMaxPowerValue in the DLL state diagram in Figure 145–44 has been updated.

Values:

FALSE: The value of PDMaxPowerValue has not changed.
TRUE: The value of PDMaxPowerValue has changed.

pd_req_class

A variable indicating the PD requested Class.

Values:

1: The PD requests Class 1.
2: The PD requests Class 2.
3: The PD requests Class 3.
4: The PD requests Class 4.
5: The PD requests Class 5.
6: The PD requests Class 6.
7: The PD requests Class 7.
8: The PD requests Class 8.

pd_reset

An implementation-specific variable that unconditionally resets the PD state diagram to OFFLINE. This variable may be set by the PD at any time.

Values:

FALSE: The device has not been reset.
TRUE: The device has been reset.

PDAutoclassRequest

A variable output by the PD power control state diagram indicating whether the PD requests Autoclass via the Data Link Layer. See 145.5.

Values:

FALSE: The PD does not request an Autoclass measurement to be performed.
TRUE: The PD requests an Autoclass measurement to be performed.

present_class_sig_0

Controls presenting the class signature '0' during T_{ACS} of the first class event (see 145.3.6.2).

Values:

FALSE: Class signature 0 is not to be applied to the PI.
TRUE: Class signature 0 is to be applied to the PI.

present_class_sig_A

Controls presenting the class signature that is used during first two class events (see 145.3.6) by the PD.

Values:

FALSE: The class signature corresponding with class_sig_A is not to be applied to the PI.
TRUE: The class signature corresponding with class_sig_A is to be applied to the PI.

present_class_sig_B

Controls presenting the class signature that is used during the third class event and all subsequent class events (see 145.3.6) by the PD.

Values:

FALSE: The class signature corresponding with class_sig_B is not to be applied to the PI.
TRUE: The class signature corresponding with class_sig_B is to be applied to the PI.

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present_det_sig

Controls presenting the detection signature (see 145.3.4) by the PD.

Values:

invalid: A non-valid PD detection signature is to be applied to both pairsets.

valid: A valid PD detection signature is to be applied to both pairsets.

either: Either a valid or non-valid PD detection signature may be applied to each pairset.

present_mark_sig

Controls presenting the mark event current and impedance (see 145.3.6.1.1) by the PD.

Values:

FALSE: The PD does not present mark event behavior.

TRUE: The PD does present mark event behavior.

present_mps

Controls applying the Maintain Power Signature MPS (see 145.3.9) to the PI.

Values:

FALSE: The MPS is not to be applied to the PI.

TRUE: The MPS is to be applied to the PI.

pse_assigned_class

A variable that indicates the assigned Class. This variable is initially set by Physical Layer classification and may be updated through DLL classification.

Values:

1: Class 1
2: Class 2
3: Class 3
4: Class 4
5: Class 5
6: Class 6
7: Class 7
8: Class 8

pse_power_level

A variable that indicates to the PD the level of power the PSE is supplying.

Values:

3: The PSE has allocated the PD requested Class or Class 3 power, whichever is less.
4: The PSE has allocated Class 4 power.
6: The PSE has allocated the PD requested Class or Class 6 power, whichever is less.
8: The PSE has allocated the PD requested Class or Class 8 power, whichever is less.

V_{Mark_th}

Mark event voltage threshold (see Table 145–25)

V_{Off_PD}

PD power supply turn off voltage (see Table 145–29)

V_{On_PD}

PD power supply turn on voltage (see Table 145–29)

V_{PD}

Voltage at the PD PI as defined in 145.1.3.

V_{Reset_th}

Reset voltage threshold (see Table 145–25)

145.3.3.3.3 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where “stop x_timer” is asserted.

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tacspd_timer
: A timer used to change the classification current to class signature ‘0’ when a PD uses Autoclass; see T_{ACS} in Table 145–28.

tauto_pd1_timer
: A timer indicating maximum delay until start of Autoclass power draw. Applies to Autoclass requests by Physical Layer classification; see T_{AUTO_PD1} in 145.3.6.2.

tauto_pd2_timer
: A timer indicating minimum delay until end of Autoclass power draw. Applies to Autoclass requests by Physical Layer classification; see T_{AUTO_PD2} in 145.3.6.2.

tinrushpdmax_timer
: A timer used to determine when the PD exits INRUSH; see T_{Inrush_PD} max in Table 145–29.

tpowerdly_timer
: A timer used to limit the PD’s current and power draw from T_{Inrush_PD} to T_{delay}; see T_{delay} in Table 145–29.

145.3.3.3.4 Functions

do_class_timing
: This function is used to evaluate the Type of PSE connected to the PI by measuring the length of the first class event. PDs that do not measure the length of the first class event return FALSE. The class event timing requirements are defined in Table 145–25. This function returns the following variable:

  long_class_event: A variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 145.3.9) the PD should use. See 145.3.7.
  Values:
  - FALSE: The PSE is identified as a Type 1 or Type 2 PSE, or the PD has not measured the length of the first class event.
  - TRUE: The PSE is identified as a Type 3 or Type 4 PSE.

do_initialize
: This function returns the following variables (see 145.3.3.3.2):

  pd_autoclass_enable
  pd_req_class
  pd_dll_capable

do_update_pse_assigned_class
: A function that updates the pse_assigned_class based on the value of PDMaxPowerValue as defined in Table 145–23. This function returns the following variable:

  pse_assigned_class: See pse_assigned_class defined in 145.3.3.3.2.

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145.3.3.3.5 State diagrams

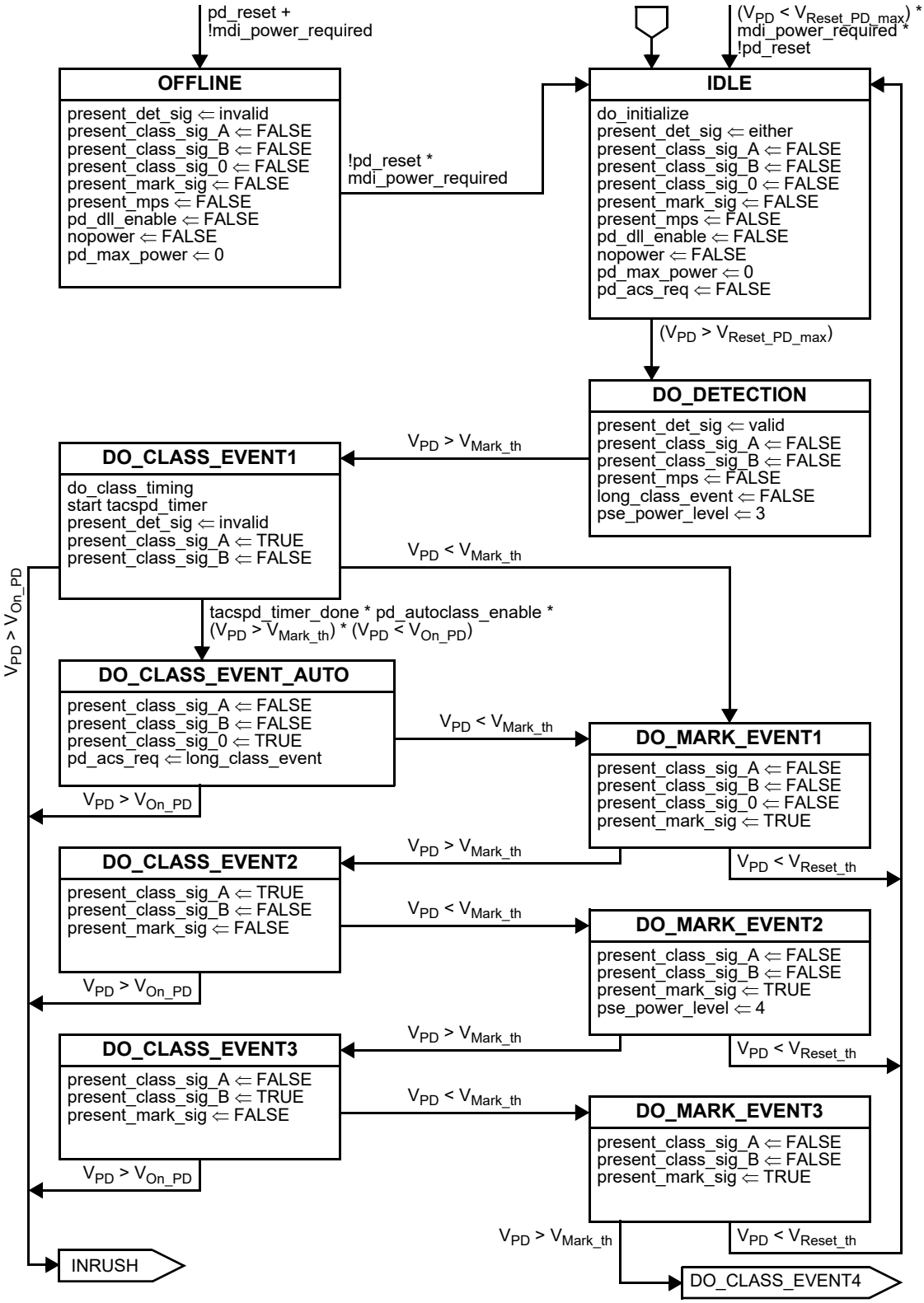

Figure 145–25—Single-signature PD state diagram

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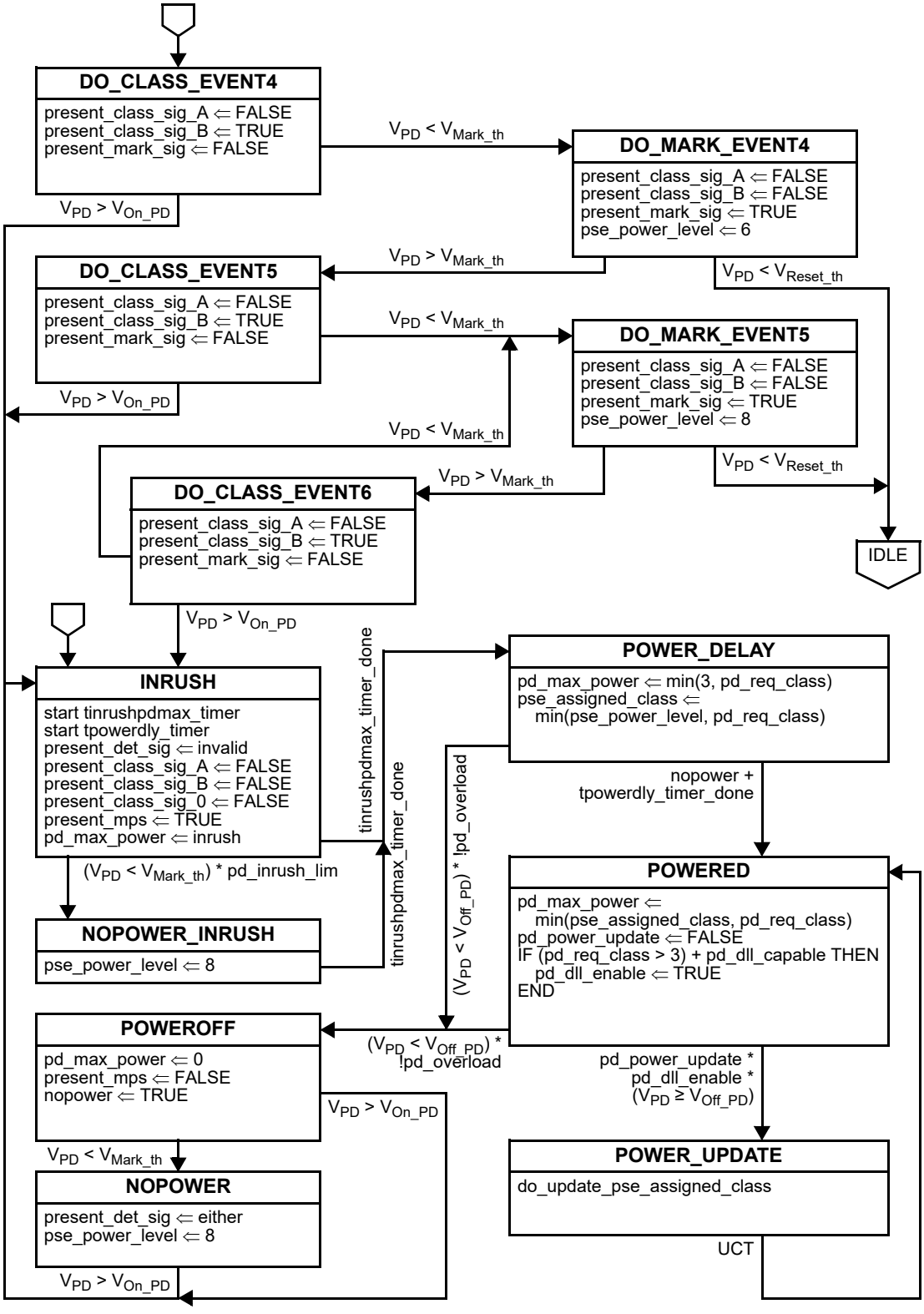

Figure 145–25—Single-signature PD state diagram *(continued)*

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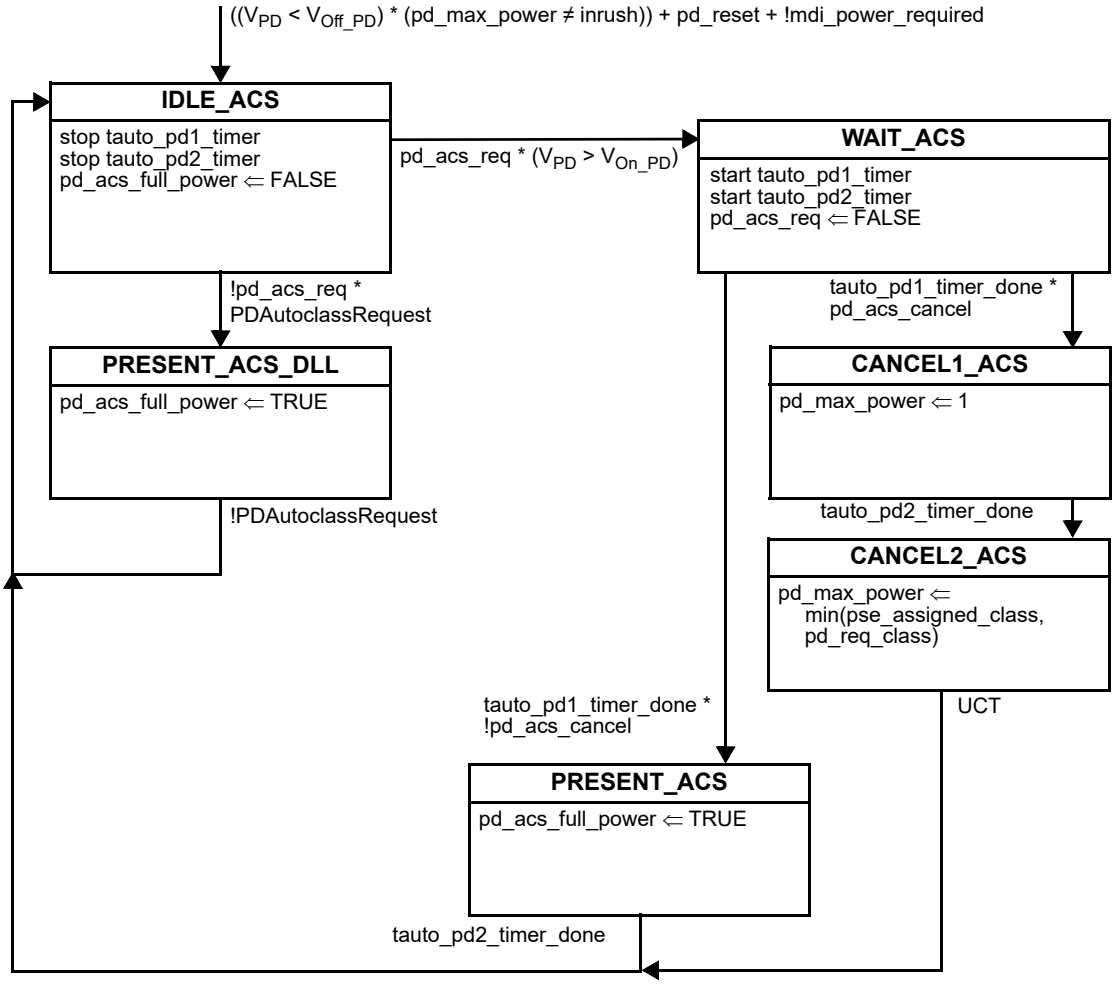

Figure 145–26—Single-signature PD Autoclass state diagram

NOTE 1—DO_CLASS_EVENT6 creates a defined behavior for a Type 3 or Type 4 PD that is brought into the classification range more than 5 times.

NOTE 2—In general, there is no requirement for a PD to respond with a valid class signature for any DO_CLASS_EVENT duration less than T_{Class_PD} as defined in Table 145–25.

145.3.3.4 Dual-signature PD state diagram

Dual-signature PDs shall provide the behavior of the state diagram shown in Figure 145–27 over each pairset independently unless otherwise specified. All the parameters that apply to Mode A and Mode B are denoted with the suffix "_mode(X)" where "X" can be "A" or "B". A parameter that ends with the suffix "_mode(X)" may have different values for Mode A and Mode B in the independent state diagrams.

145.3.3.4.1 Constants

$I_{Inrush\_PD\_2P\_max}$
: The maximum inrush current per pairset $I_{Inrush\_PD\text{-}2P}$ max (see Table 145–29)

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$V_{Off\_PD\_min}$
: The minimum PD off voltage V_{Off_PD} min (see Table 145–29)

$V_{Reset\_PD\_max}$
: The maximum PD reset voltage V_{Reset_PD} max (see Table 145–25)

145.3.3.4.2 Variables

$I_{Port_2P_}$mode(X)
: Is the current on the negative pair ($I_{Port\text{-}2P}$) of the Mode X pairset; see 145.1.3.

mdi_power_required
: A variable indicating that the PD is enabled and should request power from the PSE by applying a PD detection signature, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. This variable may be set by the PD at any time.
Values:
FALSE: PD functionality is disabled.
TRUE: PD functionality is enabled.

nopower_mode(X)
: A variable that indicates the PD has been in POWEROFF on Mode X, which indicates V_{PD} was below V_{Off_PD} while being powered, since the last time V_{PD} was below V_{Reset} for at least T_{Reset}.
Values:
FALSE: The PD has not been in POWEROFF.
TRUE: The PD has been in POWEROFF.

pd_dll_capable
: This variable indicates whether the PD implements Data Link Layer classification.
Values:
FALSE: The PD does not implement Data Link Layer classification.
TRUE: The PD does implement Data Link Layer classification.

pd_dll_enable
: A variable indicating whether the Data Link Layer classification mechanism is enabled.
Values:
FALSE: Data Link Layer classification is not enabled.
TRUE: Data Link Layer classification is enabled.

pd_inrush_lim_mode(X)
: A variable indicating that the PD limits the inrush current on Mode X below $I_{Inrush\_PD\text{-}2P}$ for the duration of the PD inrush time as defined in 145.3.8.3. This variable is set per this description.
Values:
FALSE: The PD does not limit the inrush current on Mode X.
TRUE: The PD does limit the inrush current on Mode X.

pd_max_power_mode(X)
: A variable indicating the maximum power that the PD may draw from the PSE on Mode X. See power classifications in Table 145–29.
Values:
inrush: There is no maximum power limit
0: The PD may draw up to 44 mA of current
1: The PD may draw Class 1 power
2: The PD may draw Class 2 power
3: The PD may draw Class 3 power
4: The PD may draw Class 4 power
5: The PD may draw Class 5 power

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pd_overload_mode(X)

A variable that indicates if the PD is drawing peak power in excess of P_{Class_PD}, as defined in 145.3.8.4, or when the PD is exposed to a transient condition as defined in 145.3.8.6, on Mode X.

Values:

FALSE: The PD is not drawing peak power or is exposed to a transient condition.

TRUE: The PD is drawing peak power and is not exposed to a transient condition.

pd_power_update_mode(X)

A variable that is set when the PDMaxPowerValue_mode(X) in the DLL state diagram in Figure 145–46 or Figure 145–47 has been updated.

Values:

FALSE: The value of PDMaxPowerValue_mode(X) has not changed.

TRUE: The value of PDMaxPowerValue_mode(X) has changed.

pd_req_class_mode(X)

A constant indicating the PD requested Class on Mode X

Values:

1: The PD requests Class 1.

2: The PD requests Class 2.

3: The PD requests Class 3.

4: The PD requests Class 4.

5: The PD requests Class 5.

pd_reset_mode(X)

An implementation-specific variable that unconditionally resets the PD state diagram on Mode X to OFFLINE. This variable may be set by the PD at any time.

Values:

FALSE: The device has not been reset.

TRUE: The device has been reset.

present_class_sig_A_mode(X)

Controls presenting the class signature that is used during first two class events (see 145.3.6) by the PD on Mode X.

Values:

FALSE: The class signature corresponding with class_sig_A is not to be applied to the pairset.

TRUE: The class signature corresponding with class_sig_A is to be applied to the pairset.

present_class_sig_B_mode(X)

Controls presenting the class signature that is used during the third class event and all subsequent class events (see 145.3.6) by the PD on Mode X.

Values:

FALSE: The class signature corresponding with class_sig_B is not to be applied to the pairset.

TRUE: The class signature corresponding with class_sig_B is to be applied to the pairset.

present_det_sig_mode(X)

Controls presenting the detection signature (see 145.3.4) by the PD on Mode X.

Values:

invalid: A non-valid PD detection signature is to be applied to the pairset on Mode X.

valid: A valid PD detection signature is to be applied to the pairset on Mode X.

either: Either a valid or non-valid PD detection signature may be applied to the pairset.

present_mark_sig_mode(X)

Controls presenting the mark event current and impedance (see 145.3.6.1.1) by the PD on Mode X.

Values:

FALSE: The PD does not present mark event behavior.

TRUE: The PD does present mark event behavior.

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present_mps_mode(X)

Controls applying MPS (see 145.3.9) to the PD's PI on Mode X.

Values:

FALSE: The Maintain Power Signature (MPS) is not to be applied to the PD's PI.

TRUE: The MPS is to be applied to the PD's PI.

pse_assigned_class_mode(X)

A variable (generated by the PD) that indicates the PSE assigned Class on Mode X to the PD. This variable is initially set by Physical Layer classification and may be updated through DLL classification.

Values:

1: Class 1.

2: Class 2.

3: Class 3.

4: Class 4.

5: Class 5.

pse_power_level_mode(X)

A variable that indicates to the PD the level of power the PSE is supplying on Mode X.

Values:

3: The PSE has allocated the PD requested Class or Class 3 power, whichever is less.

4: The PSE has allocated Class 4 power.

5: The PSE has allocated Class 5 power.

V_{Mark_th}

Mark event voltage threshold (see Table 145–25)

V_{Off_PD}

PD power supply turn off voltage (see Table 145–29)

V_{On_PD}

PD power supply turn on voltage (see Table 145–29)

$V_{PD_}$mode(X)

V_{PD} of the Mode X pairset; see 145.1.3.

V_{Reset_th}

Reset voltage threshold (see Table 145–25)

145.3.3.4.3 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

tinrushpdmax_timer_mode(X)

A timer used to determine when the PD exits INRUSH on Mode X; see T_{Inrush_PD} max in Table 145–29.

tpowerdly_timer_mode(X)

A timer used to limit the PD's current and power draw on Mode X from T_{Inrush_PD} to T_{delay}; see T_{delay} in Table 145–29.

145.3.3.4.4 Functions

do_class_timing_mode(X)

This function is used by a PD to evaluate the Type of PSE connected to the pairset by measuring the length of the class event on Mode X. The class event timing requirements are defined in Table 145–25. This function returns the following variable:

long_class_event_mode(X): A variable that indicates to the PD the Type of PSE to which it is

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connected. This variable is used to indicate which MPS timing requirements (see 145.3.9) the PD should use. See 145.3.7.

Values:

FALSE: The PSE is identified as a Type 1 or Type 2 PSE.

TRUE: The PSE is identified as a Type 3 or Type 4 PSE.

do_initialize_mode(X)

This function returns the following variables (see 145.3.3.4.2):

pd_req_class_mode(X)

pd_dll_capable

do_update_pse_assigned_class_mode(X)

A function that updates the pse_assigned_class_mode(X) based on the value of PDMaxPowerValue_mode(X) as defined in Table 145–23. This function returns the following variable:

pse_assigned_class_mode(X): See pse_assigned_class_mode(X) defined in 145.3.3.4.2.

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145.3.3.4.5 State diagram

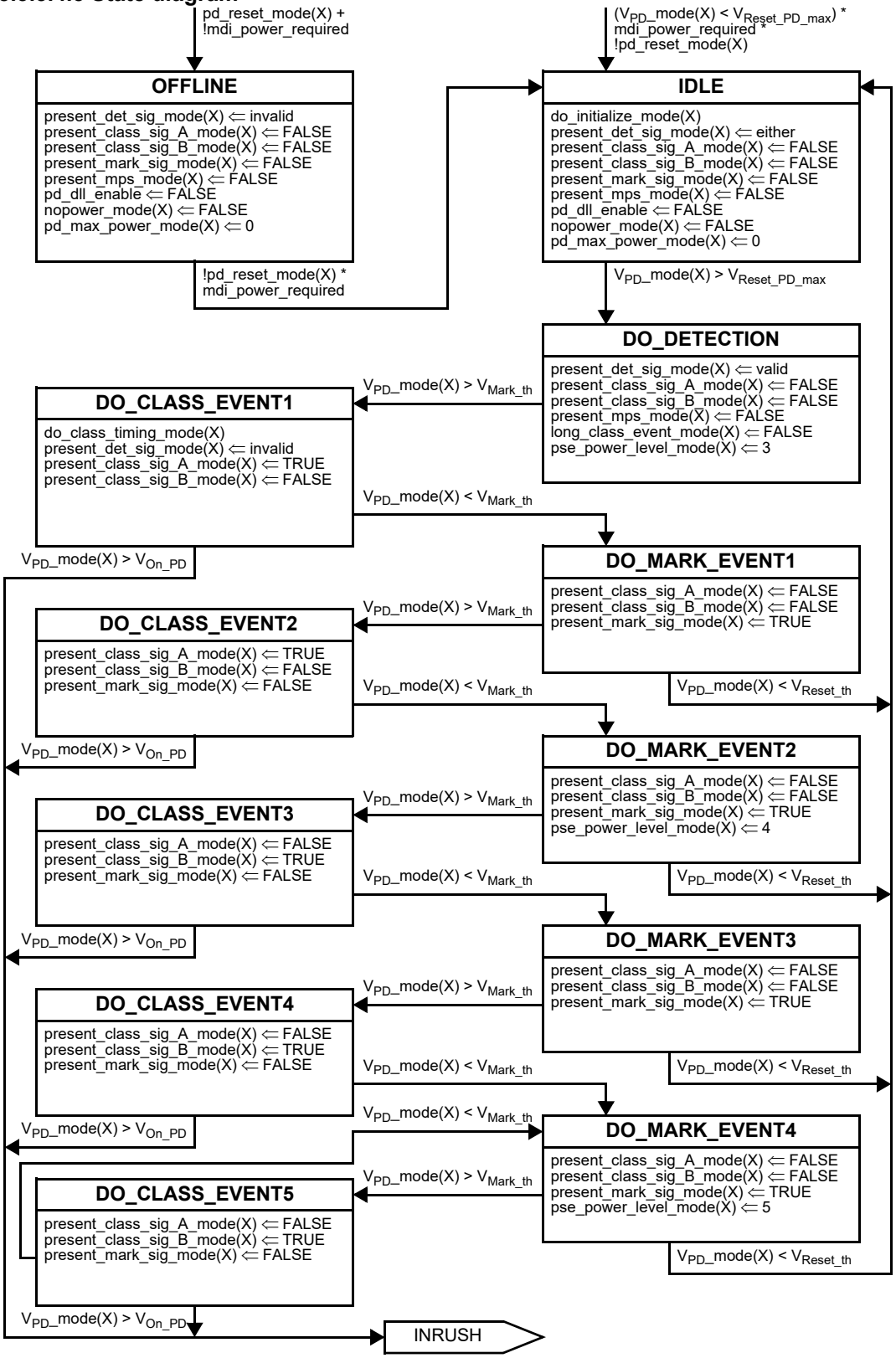

Figure 145–27—Dual-signature PD state diagram

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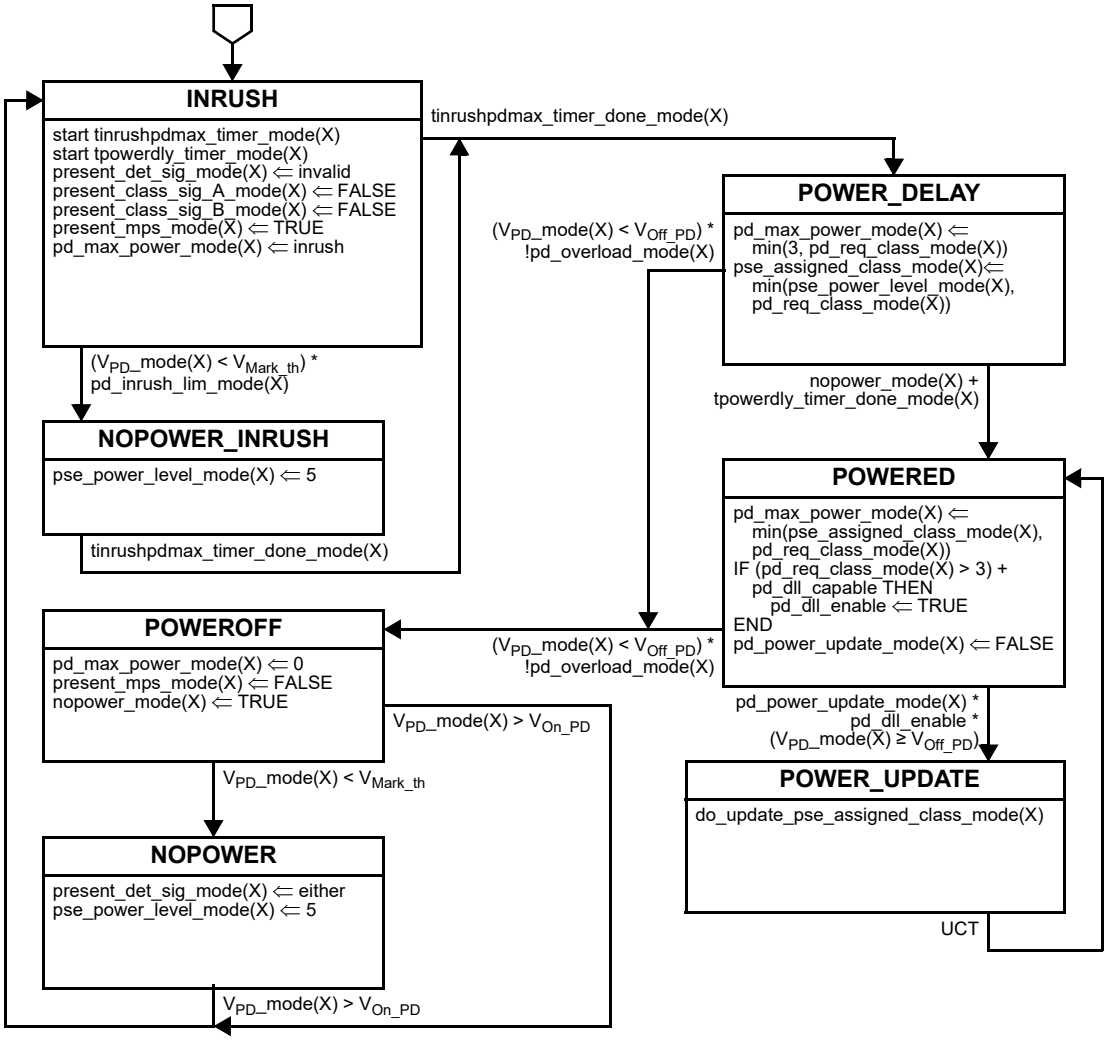

Figure 145–27—Dual-signature PD state diagram *(continued)*

145.3.4 PD valid and non-valid detection signatures

A PD presents a valid detection signature when it is in DO_DETECTION per Figure 145–25 or Figure 145–27. See 145.3.5.

A PD presents a non-valid detection signature on both pairsets while it is in a state where it does not accept power via the PI per Figure 145–25 or Figure 145–27.

A PD presents a non-valid detection signature when in a mark event state per Figure 145–25 or Figure 145–27.

When a PD presents a valid or non-valid detection signature, it shall present the detection signature at the PI between Positive V_{PD} and Negative V_{PD} of PD Mode A and PD Mode B as defined in 145.3.2.

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While a PD presents a valid detection signature on a given Mode, that detection signature shall be valid when presented under each of the following conditions (see Figure 145–28):

— With any resistance greater than 45 kΩ across the other Mode
— With any resistance greater than 45 kΩ across the other Mode and one pair of the other Mode connected to the positive potential of the given Mode

A single-signature PD that is powered over only one pairset shall present a non-valid detection signature on the unpowered pairset. A dual-signature PD that is powered over only one pairset shall present a valid detection signature on the unpowered pairset.

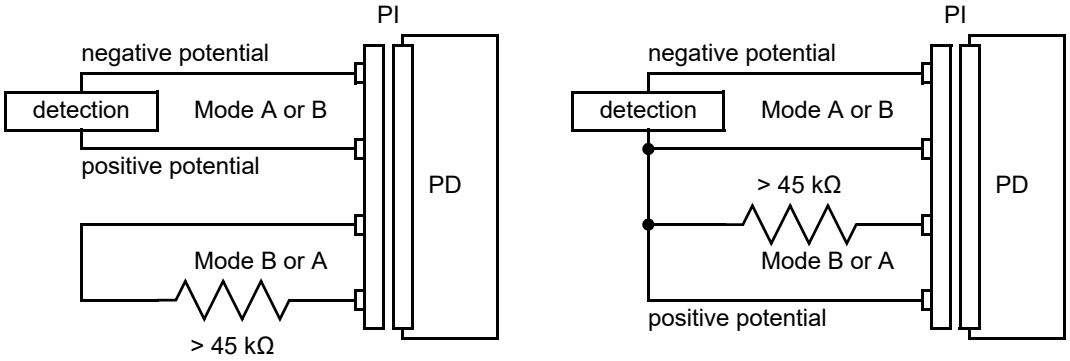

Figure 145–28—Detection signature requirements connection configurations

A PD may or may not present a valid detection signature when in IDLE.

The detection signature is a resistance calculated from two voltage/current measurements made during the detection process as defined in Equation (145–23).

$$R_{\text{detect}} = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \tag{145–23}$$

where

V_1 and V_2 are the first and second voltage measurements made at the PD PI, respectively
I_1 and I_2 are the first and second current measurements made at the PD PI, respectively
R_{detect} is the effective resistance

A valid PD detection signature shall have the characteristics of Table 145–21.

A non-valid detection signature shall have one or both of the characteristics in Table 145–22.

A PD that presents a detection signature outside of Table 145–21 is non-compliant, while a PD that presents the signature of Table 145–22 is assured to fail detection.

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Table 145–21—Valid PD detection signature characteristics, measured at the PD PI

Parameter	Conditions	Min	Max	Unit	Additional information
R_{detect} (at any 1 V or greater chord within the voltage range conditions)	2.7 V to 10.1 V	23.7	26.3	kΩ	—
V_{offset}	—	0	1.9	V	See Figure 145–29
Voltage at the PI	$I_{Port-2P}$ = 124 μA	2.7	—	V	—
Input capacitance	2.7 V to 10.1 V	0.05	0.12	μF	—
Series input inductance	2.7 V to 10.1 V	—	100	μH	—

Table 145–22—Non-valid PD detection signature characteristics, measured at PD PI

Parameter	Conditions	Range of values	Unit
R_{detect}	V_{PD} < 10.1 V	Either greater than 45 or less than 12	kΩ
Input capacitance	V_{PD} < 10.1 V	Greater than 10	μF

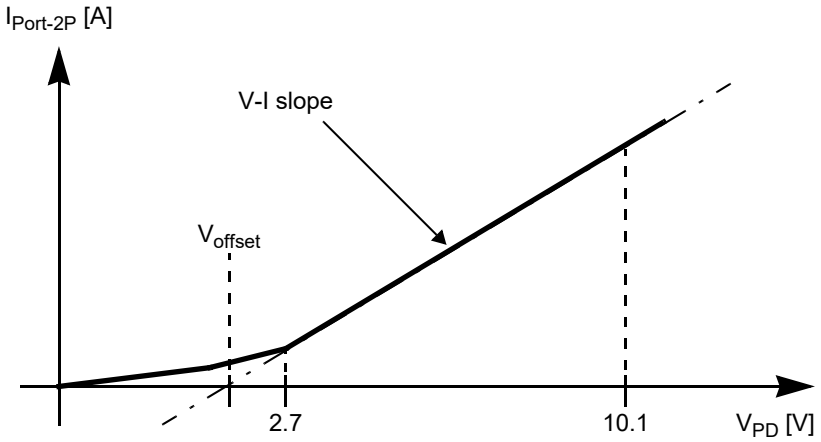

Figure 145–29—Valid PD detection signature offset

145.3.5 PD signature configurations

A single-signature PD shall present a valid detection signature, as defined in Table 145–21, on a given Mode when no voltage or current is applied across the other Mode, and shall not present a valid detection signature on the given Mode when any voltage in the range of 3.7 V to 57 V is applied across the other Mode or any current greater than 124 μA is drawn from the negative pair of the other Mode. These requirements apply to both Mode A and Mode B.

NOTE—A valid detection signature meets every requirement in Table 145–21 across all specified conditions. A failure under any allowed condition is considered “not a valid signature.”

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A dual-signature PD shall present a valid detection signature, as defined in Table 145–21, on a given Mode, regardless of any voltage between 0 V and 57 V applied to the other Mode. This requirement applies to both Mode A and Mode B.

These requirements allow the PD to be correctly identified by a PSE performing connection check as defined in 145.2.7.

145.3.6 PD classification

A PD may be classified by the PSE based on Physical Layer classification, Data Link Layer (DLL) classification, or a combination of both provided by the PD. The intent of PD classification is to provide information about the maximum power required by the PD during operation. Additionally, classification is used by the PSE and the PD to mutually identify the Type of the device to which they are connected.

See 145.2.8 for a general description of classification mechanisms. See 145.2.8.2 and 145.3.6.2 for a description of the optional Autoclass mechanism.

The requested Class of the PD is the Class the PD advertises during Physical Layer classification. It represents the amount of power the PD requires for operation. The PD shall draw no more power across any voltage in the range of $V_{Port\_PD\text{-}2P}$ than defined for the requested Class in Table 145–26 and Table 145–27. Up to 3 class events may be required to discover the requested Class of the PD.

Depending on the number of class events produced by the PSE, the assigned Class is equal to or lower than the PD requested Class. The PD shall conform to the assigned Class, regardless of its requested Class. After a successful DLL classification, the assigned Class changes depending on the value of PDMaxPowerValue for single-signature PDs and PDMaxPowerValue_mode(X) for dual-signature PDs, as defined in Table 145–23.

Table 145–23—Relation of assigned Class and DLL

Single-signature		Dual-signature	
PDMaxPowerValue	**Assigned Class**	**PDMaxPowerValue_mode(X)**	**Assigned Class on Mode X**
1 to 39	1	1 to 39	1
40 to 65	2	40 to 65	2
66 to 130	3	66 to 130	3
131 to 255	4	131 to 255	4
256 to 400	5	256 to 499	5
401 to 510	6		
511 to 620	7		
621 to 999	8		

PDs shall provide Multiple-Event Physical Layer classification as defined in 145.3.6.1.

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Single-signature PDs that request Class 1, 2, or 3 may provide Data Link Layer classification (see 145.5). Single-signature PDs that request Class 4 or higher and dual-signature PDs that request Class 4 or higher on at least one of its Modes shall provide DLL classification.

PD classification behavior shall conform to the state diagram in Figure 145–25 or Figure 145–27, and shall conform to the electrical specifications defined in Table 145–24 and Table 145–25.

A PD that is assigned to a Class lower than the Class it requested shall provide the user with an active indication if underpowered. The method of active indication is left to the implementer.

145.3.6.1 PD Multiple-Event class signature

The response of the PD to Multiple-Event Physical Layer classification consists of two class signatures, class_sig_A and class_sig_B as described by Table 145–26 or Table 145–27.

PDs shall present class_sig_A during DO_CLASS_EVENT1 and DO_CLASS_EVENT2 and class_sig_B during DO_CLASS_EVENT3, DO_CLASS_EVENT4, DO_CLASS_EVENT5, and DO_CLASS_-EVENT6, as shown in Figure 145–25 and Figure 145–27, with the corresponding classification signatures specified in Table 145–24. PDs implementing Autoclass shall present class signature 0, as defined in Table 145–24, during DO_CLASS_EVENT_AUTO as defined in 145.3.6.2.

After entering a DO_CLASS_EVENT state, the PD Physical Layer class signature shall be valid within T_{Class_PD} as defined in Table 145–25 and remain valid for the remainder of the class event.

V_{Reset_PD}, as defined in Table 145–25, is the voltage range in which the PD remains in IDLE.

Single-signature PDs shall advertise class signatures according to the PD Type and PD requested Class, as defined in Table 145–26. For single-signature PDs, the PD requested Class on either pairset is the maximum amount of power requested by the PD.

NOTE—Requested Class 0 is not defined for Type 3 PDs. A Type 1 PD that does not implement Physical Layer classification requests Class 0, with a power level equivalent to Class 3. Such PDs are assigned to Class 3 by Type 3 and Type 4 PSEs.

Dual-signature PDs shall advertise class signatures according to the PD Type and PD requested Class on each pairset, as defined in Table 145–27. For dual-signature PDs, the PD requested Class on a pairset is the maximum amount of power requested by the PD on that pairset. Dual-signature PDs may advertise different class signatures on each pairset. A dual-signature PD that is powered over only one pairset shall present a valid class signature on the unpowered pairset.

After a successful Multiple-Event Physical Layer classification has completed, a single-signature PD sets the pse_power_level variable to either 3, 4, 6 or 8. Based on the value of pse_power_level and the PD requested Class, pd_req_class, the assigned Class is derived in the variable pse_assigned_class.

After a successful Multiple-Event Physical Layer classification has completed, a dual-signature PD sets the pse_power_level_mode(X) variable to either 3, 4, or 5. Based on the value of pse_power_level_mode(X) and the PD requested Class, pd_req_class_mode(X), the assigned Class is derived in the variable pse_assigned_class_mode(X).

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Table 145–24—Class signatures generated at the PD PI

Parameter	Conditions	Minimum	Maximum	Unit
Current for class signature 0	14.5 V to 20.5 V	1	4	mA
Current for class signature 1		9	12	
Current for class signature 2		17	20	
Current for class signature 3		26	30	
Current for class signature 4		36	44	

Table 145–25—Multiple-Event Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional information
1	Class event voltage	V_{Class_PD}	V	14.5	20.5	—
2	Mark event voltage	V_{Mark_PD}	V	6.9	10.1	—
3	Mark event current	I_{Mark}	mA	0.25	4	See 145.3.6.1.1
4	Mark event threshold	V_{Mark_th}	V	10.1	14.5	See 145.3.6.1.1
5	Classification reset threshold	V_{Reset_th}	V	2.81	6.9	See 145.3.6.1.1
6	Classification reset voltage	V_{Reset_PD}	V	0	2.81	See 145.3.6.1
7	Long first class event timing	T_{LCE_PD}	ms	75.5	87.5	See 145.3.7
8	PD classification stability time	T_{Class_PD}	ms	—	5	See 145.3.6.1

Table 145–26—Physical Layer classifications and Multiple Event Responses for single-signature PDs

PD Type	Requested Class	class_sig_A class signature	class_sig_B class signature	Requested power (W)
3	1	1	1	3.84
	2	2	2	6.49
	3	3	3	13
	4	4	4	25.5
	5	4	0	40
	6	4	1	51
4	7	4	2	62
	8	4	3	71.3

NOTE 1—See Table 145–24 for definition of class signatures 0 to 4.
NOTE 2—PDs may be assigned to a lower Class than the PD requested Class, which results in a lower value of P_{Class_PD}.

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Table 145–27—Physical Layer classifications and Multiple Event Responses for dual-signature PDs

PD Type	Requested Class per pairset	class_sig_A class signature	class_sig_B class signature	Requested power (W)
3	1	1	0	3.84
	2	2	0	6.49
	3	3	0	13
	4	4	0	25.5
4	5	4	3	35.6

NOTE 1—See Table 145–24 for definition of class signatures 0 to 4.
NOTE 2—PDs may be assigned to a lower Class than the PD requested Class, which results in a lower value of P_{Class_PD-2P}.

145.3.6.1.1 Mark Event behavior

When the PD is presenting a mark event signature in a DO_MARK_EVENT state, as shown in the state diagram of Figure 145–25 and Figure 145–27, the PD shall draw I_{Mark} as defined in Table 145–25 and present a non-valid detection signature as defined in Table 145–22.

The PD shall not exceed the I_{Mark} current limits when voltage at the PI enters the V_{Mark_PD} specification as defined in Table 145–25.

V_{Mark_th} is the PI voltage threshold at which the PD transitions into, and one of the voltage thresholds to transition out of, the DO_CLASS_EVENT states as shown in Figure 145–25 and Figure 145–27.

Implementations should employ appropriate methods (such as hysteresis in V_{Mark_th}) to avoid erroneous transitions between class and mark states when the PSE switches from a class voltage to a mark voltage or vice versa.

V_{Reset_th} is the PI voltage threshold at which the PD transitions from a DO_MARK_EVENT state to IDLE as shown in Figure 145–25 and Figure 145–27.

145.3.6.2 Autoclass (optional)

Single-signature PDs may choose to implement an extension of Physical Layer classification known as Autoclass. Autoclass is only defined for single-signature PDs. The purpose of Autoclass is to allow the PSE to determine the actual maximum power draw of the connected PD. See 145.2.8.2.

A PD that implements Autoclass shall change its current during the first class event to class signature 0 no earlier than T_{ACS} min and no later than T_{ACS} max, as defined in Table 145–28.

After power up, a PD that implements Autoclass shall draw its highest required power, $P_{Autoclass\_PD}$, subject to the requirements on P_{Class_PD} in 145.3.8.2, throughout the period bounded by T_{AUTO_PD1} and T_{AUTO_PD2}, measured from when V_{PD} rises above V_{On_PD}. The PD is restricted to a maximum power draw of $P_{Autoclass\_PD}$ until the PD successfully negotiates a higher power level through Data Link Layer classification as defined in 145.5. A PD that draws less than P_{Class_PD} max for Class 1 during the period bounded by T_{AUTO_PD1} and T_{AUTO_PD2} indicates to the PSE that the power allocation should be determined by the assigned Class. By doing this the PD can abort the Physical Layer Autoclass procedure.

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Table 145–28—Autoclass PD timing requirements

Item	Parameter	Symbol	Units	Min	Max	Additional Information
1	Autoclass signature timing	T_{ACS}	ms	75.5	87.5	Measured from transition to DO_CLASS_EVENT1
2	Autoclass power draw start time	T_{AUTO_PD1}	ms	—	1350	Measured from when V_{PD} rises above V_{On_PD}
3	Autoclass power draw end time	T_{AUTO_PD2}	ms	3650	—	

145.3.7 PSE Type identification

PDs may determine the Type of the PSE they are connected to by measuring the duration of the first class event. Such a PD may set long_class_event to TRUE if the first class event is longer than T_{LCE_PD} min and shall set long_class_event to TRUE if the first class event is longer than T_{LCE_PD} max. If long_class_event is FALSE, this indicates the PSE is a Type 1 or Type 2 PSE. If long_class_event is TRUE this indicates the PSE is a Type 3 or Type 4 PSE. This determination allows the PD to make use of short MPS to reduce standby power.

145.3.8 PD power

The PD shall operate within the characteristics in Table 145–29.

The PD may be capable of drawing power from a local power source. When a local power source is provided, the PD may draw some, none, or all of its power from the PI.

Table 145–29—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Input DC voltage per pairset per the assigned Class					
	Class 1	V_{Port_PD-2P}	V	42.8	57	See 145.3.8.1, Table 145–1
	Class 2			42		
	Class 3			39.9		
	Class 4			42.5		
	Class 5, single-signature PD			44.3		
	Class 5, dual-signature PD			41.1		
	Class 6			42.5		
	Class 7			42.9		
	Class 8			41.1		
2	Transient operating input voltage per pairset	V_{Tran_PD-2P}	V	36	—	See 145.3.8.6

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Table 145–29—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Additional information
3	Input voltage range during overload for a single-signature PD per the assigned Class					See 145.3.8.4
	Class 1 to 6	$V_{Overload-2P}$	V	39.4	—	
	Class 7 to 8			40.4	—	
	Input voltage range during overload for a dual-signature PD per the assigned Class					
	Class 1 to 4	$V_{Overload-2P}$	V	39.4	—	
	Class 5			40.4	—	
4	Input inrush current for a single-signature PD per the assigned Class					
	Class 1 to 6	I_{Inrush_PD}	A	—	0.4	See 145.3.8.3
	Class 7 to 8			—	0.8	
5	Input inrush current per pairset per the assigned Class					
	Single-signature PD, Class 1 to 6	I_{Inrush_PD-2P}	A	—	0.4	See 145.3.8.3
	Single-signature PD, Class 7 to 8			—	0.6	
	Dual-signature PD, Class 1 to 5			—	0.4	
6	Inrush to PD current control delay	T_{Inrush_PD}	ms	—	50	See 145.3.8.3
7	Inrush to operating state delay	T_{delay}	ms	80	—	See 145.3.8.3
8	Input average power for single-signature PDs per the assigned Class					
	Class 1	P_{Class_PD}	W	—	3.84	See 145.3.8.2, 145.3.6, Table 145–1, Table 145–26
	Class 2			—	6.49	
	Class 3			—	13	
	Class 4			—	25.5	
	Class 5			—	40	
	Class 6			—	51	
	Class 7			—	62	
	Class 8			—	71.3	
9	Input average power for a pairset for dual-signature PDs per the assigned Class					
	Class 1	P_{Class_PD-2P}	W	—	3.84	See 145.3.8.2, 145.3.6, Table 145–1, Table 145–27
	Class 2			—	6.49	
	Class 3			—	13	
	Class 4			—	25.5	
	Class 5			—	35.6	

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Table 145–29—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Additional information
10	Peak operating power for single-signature PDs per the assigned Class					
	Class 1	P_{Peak_PD}	W	—	5	See 145.3.8.4
	Class 2			—	8.36	
	Class 3			—	14.4	
	Class 4			—	28.3	
	Class 5			—	42	
	Class 6			—	53.5	
	Class 7			—	65.1	
	Class 8			—	74.9	
11	Peak operating power for a pairset for dual-signature PDs per the assigned Class					
	Class 1	$P_{Peak\_PD\text{-}2P}$	W	—	5	See 145.3.8.4
	Class 2			—	8.36	
	Class 3			—	14.4	
	Class 4			—	28.3	
	Class 5			—	37.4	
12	Input current slew rate	$I_{Slewrate}$	mA/µs	—	4.7	See 145.3.8.5
13	Single-signature PD capacitance while in INRUSH, POWER_DELAY, or POWERED					
	Class 1 to 4	C_{Port}	µF	5	—	See 145.3.8.3, 145.3.8.6
	Class 5 to 6			10	—	
	Class 7 to 8			20	—	
14	Dual-signature PD pairset capacitance while in INRUSH, POWER_DELAY, or POWERED					
	Class 1 to 4	$C_{Port\text{-}2P}$	µF	5	—	See 145.3.8.3, 145.3.8.6
	Class 5			10	—	
15	Ripple and noise					
	< 500 Hz	V_{Noise_PD}	V_{pp}	—	0.5	See 145.3.8.7
	500 Hz to 150 kHz			—	0.2	
	150 kHz to 500 kHz			—	0.15	
	500 kHz to 1 MHz			—	0.1	
16	PD power supply turn on voltage	V_{On_PD}	V	30	42	See 145.3.8.1
17	PD power supply turn off voltage	V_{Off_PD}	V	30	$V_{Port\_PD\text{-}2P}$ min	See 145.3.8.1
18	Reflected voltage	V_{refl}	V	—	2.8	See 145.3.8.8

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145.3.8.1 Input voltage

The specification for $V_{Port\_PD\text{-}2P}$ in Table 145–29 is for the input voltage range after startup (see 145.3.8.3), and accounts for loss in the cabling plant.

The PD shall turn on at a voltage in the range of V_{On_PD}. After the PD turns on, the PD shall stay on over the entire $V_{Port\_PD\text{-}2P}$ range. After reaching POWER_DELAY, the PD shall turn off at a voltage in the range of V_{Off_PD}. For dual-signature PDs the requirements for V_{On_PD} and V_{Off_PD} apply to each pairset individually. A PD shall not turn off due to peak power draw, causing V_{PD} to go as low as $V_{Overload\text{-}2P}$, as specified in 145.3.8.4, or due to a voltage transient as defined in 145.3.8.6. This behavior is encoded in the variable pd_overload and pd_overload_mode(X).

The PD shall turn on or off without startup oscillation and within the first trial at any load value when fed by $V_{Port\_PSE\text{-}2P}$ min to $V_{Port\_PSE\text{-}2P}$ max (as defined in Table 145–16):

— With a series resistance less than or equal to R_{Ch} for assigned Class 1 through 4 to a single-signature PD.
— With a series resistance less than or equal to R_{Ch} / 2 for assigned Class 5 through 8 to a single-signature PD.
— With a series resistance less than or equal to R_{Ch} connected to a given Mode of a dual-signature PD.

V_{On_PD} min is set at 30 V to align with V_{Off_PD} min. It is recommended that a PD implements hysteresis between V_{On_PD} and V_{Off_PD}.

When the PD is in POWEROFF and V_{PD} falls below V_{Mark_th}, the PD transitions to NOPOWER and may show a valid or invalid detection signature, and may or may not draw mark current, draw any class current, and show MPS. Interoperability between PSE and PD is no longer guaranteed when the nopower variable is TRUE or the PD has entered NOPOWER_INRUSH since the last time V_{PD} was below V_{Reset_PD} max.

145.3.8.2 Input average power

P_{Port_PD} is the average power drawn by a single-signature PD, measured using a sliding window with a width of 1 second. $P_{Port\_PD\text{-}2P}$ is the average power drawn by a given Mode of a dual-signature PD, measured using a sliding window with a width of 1 second.

For single-signature PDs, P_{Port_PD} shall not exceed P_{Class_PD} for the assigned Class. For dual-signature PDs, $P_{Port\_PD\text{-}2P}$ shall not exceed $P_{Class\_PD\text{-}2P}$ for the assigned Class.

A PD that has either enabled Autoclass during Physical Layer classification and drew a power higher than Class 1 power during the period bounded by T_{AUTO_PD1} and T_{AUTO_PD2} or has requested Autoclass through DLL, shall not draw more power than $P_{Autoclass\_PD}$, unless the PD successfully negotiates a different power level, up to the PD requested Class, through Data Link Layer classification as defined in 145.5.

P_{Class_PD} and $P_{Class\_PD\text{-}2P}$ defined in Table 145–29 are determined per the assigned Class. The assigned PSE Class is determined by the number of class events and the PD requested Class, as shown in Table 145–11. P_{Class_PD} is the maximum average PI power and applies to single-signature PDs. $P_{Class\_PD\text{-}2P}$ is the maximum average power on a pairset and applies to dual-signature PDs.

PDs may dynamically adjust their maximum required operating power below P_{Class_PD} or $P_{Class\_PD\text{-}2P}$ as described in 145.5. PDs may also adjust their maximum required operating power below P_{Class_PD} by using Autoclass (see 145.3.6.2).

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Single-signature PDs that have successfully completed DLL classification shall not exceed a power consumption of PDMaxPowerValue as defined in 145.5.3.3.1. Dual-signature PDs that have successfully completed DLL classification shall not exceed a power consumption of PDMaxPowerValue_mode(X) on Mode X as defined in 145.5.3.4.2.

145.3.8.2.1 Input average power exceptions

For single-signature PDs assigned to Class 8 and PDMaxPowerValue set to 713 or greater, when additional information is available to the PD regarding actual link section DC resistance between the PSE PI and the PD PI, the PD may consume greater than P_{Class_PD} but shall not consume greater than P_{Class} at the PSE PI and shall not draw a total 4-pair current in excess of $2 \times I_{Cable}$ as defined in Table 145–1.

For dual-signature PDs assigned to Class 5 and PDMaxPowerValue_mode(X) set to 356 or greater, when additional information is available to the PD regarding actual link section DC resistance between the PSE PI and the PD PI, the PD may consume greater than $P_{Class\_PD\text{-}2P}$ but shall not consume greater than $P_{Class\text{-}2P}$ on the pairset at the PSE PI and shall not draw current in excess of I_{Cable} as defined in Table 145–1.

145.3.8.2.2 System stability test conditions during startup and steady state operation

When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input. See Annex 33A for PD design guidelines for stable operation.

Stable operation may be verified by confirming that the PD meets V_{Noise_PD}, as defined in Table 145–29, when the PD is powered by a voltage source set in the range of $V_{Port\_PSE\text{-}2P}$, as defined in Table 145–16, through a series resistance of R_{Ch}, as defined in Table 145–1, and the PD is operating at or below P_{Class_PD} or $P_{Class\_PD\text{-}2P}$.

145.3.8.3 Input inrush current

The PD inrush time duration is defined as beginning with the application of input voltage at the PI when V_{PD} crosses the PD power supply turn on voltage, V_{On_PD} as defined in Table 145–29, and ends after T_{delay}.

The inrush current is the initial current drawn by the PD, which is used to charge C_{Port} or $C_{Port\text{-}2P}$. A PD may limit the inrush current below I_{Inrush_PD} and $I_{Inrush\_PD\text{-}2P}$ to allow for large values of C_{Port} and $C_{Port\text{-}2P}$.

The PSE limits the inrush current to I_{Inrush} and $I_{Inrush\text{-}2P}$, for at least T_{Inrush_PD} max, as defined in Table 145–16 and Table 145–29.

PDs shall draw less than I_{Inrush_PD} and $I_{Inrush\_PD\text{-}2P}$ from T_{Inrush_PD} max until T_{delay} min, when connected to a source that meets the requirements of 145.2.10.7. This delay is required so that the PD does not enter a high power state before the PSE has had time to change the available current from the POWER_UP to the POWER_ON limits. A PD can meet this requirement by either having C_{Port} or $C_{Port\text{-}2P}$ charged within T_{Inrush_PD} max or by limiting the input inrush current.

Single-signature PDs assigned to Class 1, 2, or 3 shall conform to P_{Class_PD} and P_{Peak_PD} within T_{Inrush_PD} max as defined in Table 145–29. Dual-signature PDs assigned to Class 1, 2, or 3 shall conform to $P_{Class\_PD\text{-}2P}$ and $P_{Peak\_PD\text{-}2P}$ within T_{Inrush_PD} max as defined in Table 145–29 on that pairset.

NOTE—PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltage reaches 99% of steady state or after T_{Inrush_PD} max. PD requirements are impacted by PSE current limits. See 145.2.10.7 for details.

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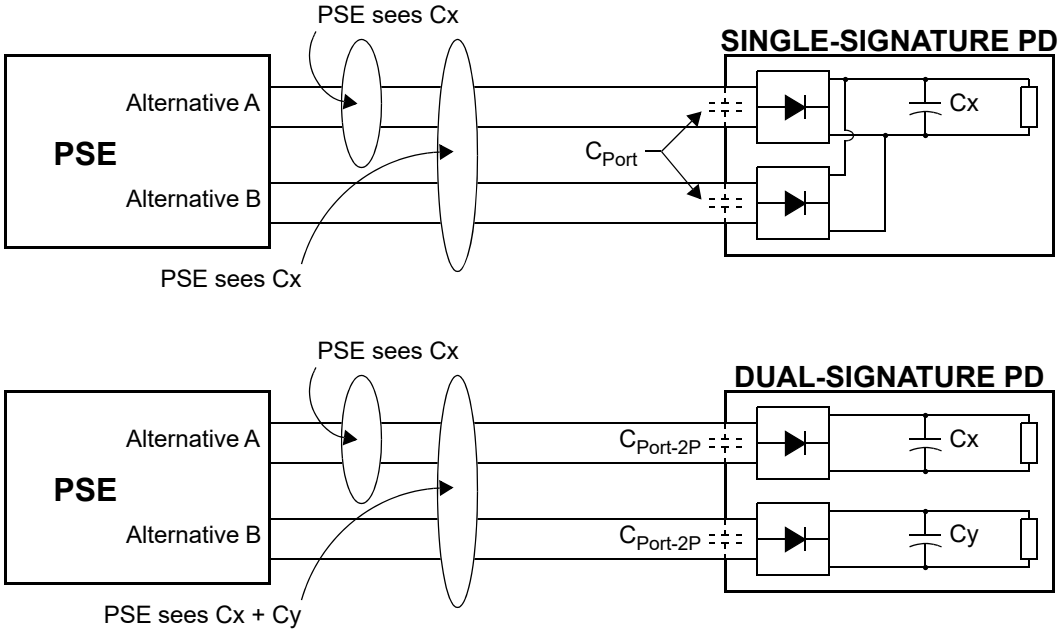
C_{Port} in Table 145–29 is the PD input capacitance during POWER_UP and POWER_ON that a PSE sees as load when operating one or both pairsets, when connected to a single-signature PD. $C_{Port\text{-}2P}$ in Table 145–29 is the PD input capacitance during POWER_UP_PRI, POWER_UP_SEC, POWER_ON_PRI, and POWER_ON_SEC that a PSE sees as load on each pairset independently, when connected to a dual-signature PD. See Figure for a simplified PSE-PD C_{Port} and $C_{Port\text{-}2P}$ interpretation model.



NOTE—The “dual-signature PD” in Figure represents a PD with two completely isolated circuits connected to Mode A and Mode B. The PSE will see a capacitance of Cx + Cy. A dual-signature PD can also be implemented with a single load, resulting in a lower than Cx + Cy capacitance value as seen by the PSE.

Figure 145–30—C_{Port} interpretation model

145.3.8.4 Peak operating power

$V_{Overload\text{-}2P}$ is the PD PI voltage when the PD is drawing the permissible P_{Peak_PD} for single-signature PDs, or $P_{Peak\_PD\text{-}2P}$ for dual-signature PDs.

At any static voltage at the PI, and any PD operating condition, with the exception described in 145.3.8.4.1, the peak power for single-signature PDs shall not exceed P_{Class_PD} for more than T_{CUT} min, as defined in Table 145–16 and 5% duty cycle. P_{Peak_PD} is the maximum peak operating power and applies to single-signature PDs.

At any static voltage at the PI, and any PD operating condition, with the exception described in 145.3.8.4.1, the peak power for a dual-signature PD shall not exceed $P_{Class\_PD\text{-}2P}$ for more than T_{CUT} min, as defined in Table 145–16 and 5% duty cycle. $P_{Peak\_PD\text{-}2P}$ is the maximum peak operating power on a pairset and applies to dual-signature PDs.

NOTE—The duty cycle of the peak current is measured using a sliding window with a width of 1 second.

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Peak power is defined in Table 145–29 and depends on the Class assigned by the PSE. Equation (145–24) and Equation (145–25) are used to approximate the ratiometric peak powers of Class 1 through Class 8. These equations may be used to calculate P_{Peak_PD} or $P_{Peak\_PD\text{-}2P}$ after Data Link Layer classification and for Autoclass by substituting PDMaxPowerValue with the corresponding value of $P_{Autoclass\_PD}$.

$$P_{Peak\_PD} = \left\{ \begin{array}{l} 0.129 \times \text{PDMaxPowerValue for assigned Class 1 and 2} \\ 0.111 \times \text{PDMaxPowerValue for assigned Class 3 and 4} \\ 0.105 \times \text{PDMaxPowerValue for assigned Class 5 to 8} \end{array} \right\}_{W} \quad (145\text{–}24)$$

$$P_{Peak\_PD\text{-}2P} = \left\{ \begin{array}{l} 0.129 \times \text{PDMaxPowerValue\_mode(X) for assigned Class 1 and 2} \\ 0.111 \times \text{PDMaxPowerValue\_mode(X) for assigned Class 3 and 4} \\ 0.105 \times \text{PDMaxPowerValue\_mode(X) for assigned Class 5} \end{array} \right\}_{W} \quad (145\text{–}25)$$

where

PDMaxPowerValue	is the actual maximum input average the PD may draw under the current power allocation; see 145.5.3.3.1
PDMaxPowerValue_mode(X)	is the actual maximum input average the PD may draw under the current power allocation on Mode X; see 145.5.3.4.2

145.3.8.4.1 Peak operating power exceptions

For single-signature PDs assigned to Class 8 and for dual-signature PDs assigned to Class 5, when additional information is available to the PD regarding actual link section DC resistance between the PSE PI and the PD PI, in any operating condition with any static voltage at the PI, the peak power shall not exceed P_{Port_PD} max for single-signature PDs and $P_{Port\_PD\text{-}2P}$ max for dual-signature PDs for more than T_{CUT} min, as defined in Table 145–16 and with 5% duty cycle. Peak operating power shall not exceed $1.05 \times P_{Port\_PD}$ max for single-signature PDs and shall not exceed $1.05 \times P_{Port\_PD\text{-}2P}$ max for dual-signature PDs on each pairset. P_{Port_PD} max and $P_{Port\_PD\text{-}2P}$ max refer to the maximum power draw as permitted by 145.3.8.2.1.

145.3.8.5 Input current slew rate

When the input voltage at the PI is static and in the range of $V_{Port\_PD\text{-}2P}$ defined by Table 145–29, the input current drawn by a single-signature PD shall not change faster than $I_{Slewrate}$ defined in Table 145–29, in either polarity. Each pairset current drawn by a dual-signature PD shall not change faster than $I_{Slewrate}$ defined in Table 145–29, in either polarity. This limitation applies after inrush has completed (see 145.3.8.3) and before the PD has disconnected.

145.3.8.6 PD behavior during transients at the PSE PI

A PD shall continue to operate without interruption in the presence of transients

- Lasting longer than 30 µs and less than 250 µs at the PSE PI as defined in 145.2.10.3, and causing the voltage at the PD PI to fall to no less than $V_{Tran\_PD\text{-}2P}$, as defined in Table 145–29.
- Lasting less than 30 µs and causing the voltage at the PD PI to fall to not less than 34 V.

During a transient the input power of the PD may exceed P_{Peak_PD} or $P_{Peak\_PD\text{-}2P}$. Table 145–30 defines three PSE output voltage transients.

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Table 145–30—Transient conditions

Item	Assigned Class	2-pair/ 4-pair	$T_{Transient}$	Initial voltage	Final voltage	Source dv / dt	Source resistance	Source current[a]
TR1	1 to 4	2-pair	10 ms	50 V	56 V	2.25 V/ms	12.5 Ω	Limit to I_{LIM-2P} + 5 mA
	1 to 6	4-pair					6.25 Ω	
TR2	1 to 4	2-pair	6 ms	52 V			12.5 Ω	
	1 to 8	4-pair					6.25 Ω	
TR3	1 to 8	both	4 ms	52 V	54.5 V	3500 V/ms	1.5 Ω	> 5 A capability

[a] The source current for TR1 and TR2 is the current limit per powered pairset.

When transient TR1 or TR2 is applied, the PD shall meet the operating power limits within $T_{Transient}$, as defined in Table 145–30, referenced from when the 'final voltage' is reached at the source. When transient TR1 or TR2 is applied, the PD shall not cause the source to be in current limit for longer than T_{LIM} min.

When transient TR3 is applied, the PD shall meet the operating power limits within 4 ms, referenced from the beginning of the TR3 transient.

The TR1, TR2, and TR3 tests consists of a voltage source, with a current limit (for TR1 and TR2), driven from the 'initial voltage' to the 'final voltage' at the 'source dv/dt' rate. A source resistance, as defined in Table 145–30 is in series with this voltage source and the PD.

These requirements apply to each pairset individually for a dual-signature PD.

145.3.8.7 Ripple and noise

The PD shall meet V_{Noise_PD}, defined in Table 145–29, the common-mode or differential pair-to-pair noise at the PD PI generated by the PD circuitry. V_{Noise_PD} applies for all operating voltages in the range of V_{Port_PD-2P}, over the range of input power of the device, and when connected to any source resistance up to R_{Ch}.

The PD shall operate correctly in the presence of ripple and noise generated by the PSE that appears at the PD PI. These levels are specified in Table 145–16.

145.3.8.8 Reflected voltage

For a single-signature PD, when any voltage in the range of 0 V to V_{Port_PD-2P} max is applied per any of the valid 2-pair configurations, defined in Table 145–20, that have only a single pair connected to the positive potential (see Figure 145–31), the voltage on the Mode not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed V_{refl} as defined in Table 145–29.

For a dual-signature PD, when any voltage in the range of 0 V to V_{Port_PD-2P} max is applied per any of the valid 2-pair configurations, defined in Table 145–20, including those with two pairs connected to the positive potential (see Figure 145–31), the voltage on the Mode with at least one pair not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed V_{refl} as defined in Table 145–29.

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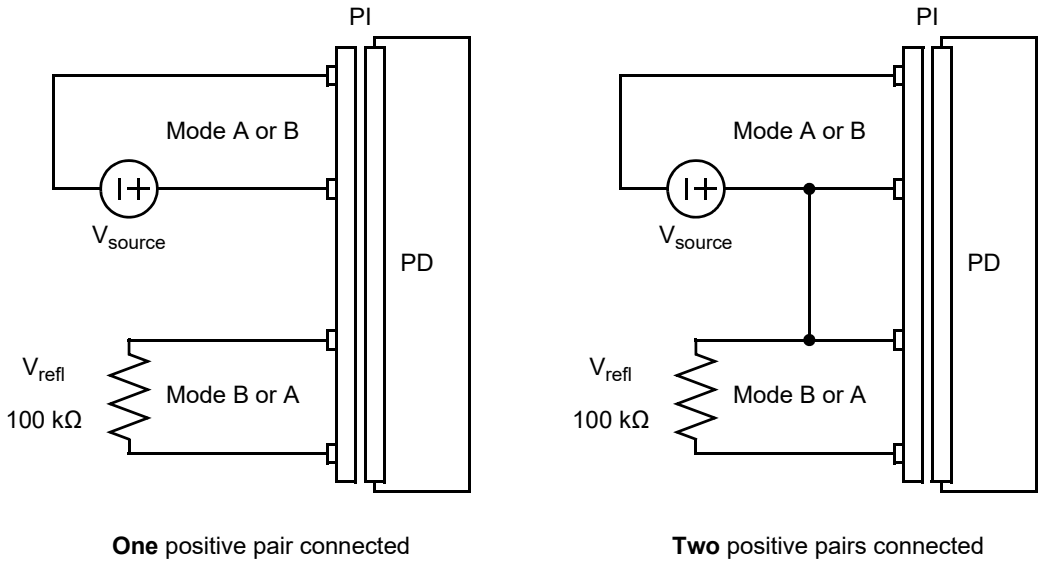

Figure 145–31—Reflected voltage requirements

145.3.8.9 PD pair-to-pair current unbalance

When a PSE supplies power to a PD using all 4 pairs, the current may not equally divide between the pairs that are at the same polarity. This is referred to as pair-to-pair current unbalance. The degree to which the current is unbalanced depends on the specific combination of PSE, cabling, and PD.

The maximum pair current in a system depends on the assigned Class (see 145.3.6), and is defined in Table 145–31.

Table 145–31—Maximum pair-to-pair current unbalance

Parameter	Assigned Class	Unit	Value
$I_{Unbalance\_PD\text{-}2P}$	1 to 4[a]	A	P_{Class_PD} / V_{PD}
	5 to 8		$I_{Con\text{-}2P\text{-}unb} - 0.01$
$I_{Unbalance\_peak\text{-}2P}$	1 to 4[a]	A	P_{Peak_PD} / V_{PD}
	5 to 8		$I_{LIM\text{-}2P} - 0.002$

[a] There is no maximum unbalance current requirement for these assigned Classes.

This subclause describes unbalance requirements for PDs that operate over 4 pairs. The contribution of PD PI pair-to-pair effective resistance unbalance to the effective system end-to-end resistance unbalance is determined by PD maximum (R_{PD_max}) and minimum (R_{PD_min}) common mode effective resistance in the powered pairs of same polarity. See Figure 145A–3. Effective resistances of R_{PD_min} and R_{PD_max} include the effects of PD pair to pair voltage difference and the PD PI resistive elements. See definition and measurements in Annex 145A.5.

R_{PD_max}, defined in Equation (145–26), for a given R_{PD_min}, is the highest supported common mode effective resistance in the powered pairs of the same polarity. PDs that meet Equation (145–26) intrinsically

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meet unbalance requirements. Equation (145–26) is only applicable for R_{PD_min} up to a value of 1 Ω and power draw up to P_{Class_PD}.

$$0 < R_{PD\_max} \leq \left\{ \begin{array}{ll} 2.182 \times R_{PD\_min} + 0.125 & \text{for assigned Class 5} \\ 1.988 \times R_{PD\_min} + 0.105 & \text{for assigned Class 6} \\ 1.784 \times R_{PD\_min} + 0.08 & \text{for assigned Class 7} \\ 1.727 \times R_{PD\_min} + 0.074 & \text{for assigned Class 8} \end{array} \right\}_{\Omega} \quad (145\text{–}26)$$

where

R_{PD_max} is, given R_{PD_min}, the highest supported common mode effective resistance in the powered pairs of the same polarity

R_{PD_min} is the lower PD common mode effective resistance in the powered pairs of the same polarity

Common mode effective resistance is the resistance of the two conductors (including their components on each conductor) in a powered pair of the same polarity connected in parallel.

Figure 145A–1 illustrates the relationship between R_{PD_max} and R_{PD_min} effective resistances at the PD PI as defined by Equation (145–26) and the rest of the end-to-end pair to pair effective resistance components.

Single-signature PDs shall not exceed $I_{Unbalance\_PD\text{-}2P}$ for longer than T_{CUT} min and 5 % duty cycle, and shall not exceed $I_{Unbalance\_peak\text{-}2P}$, as defined in Table 145–31 on any pair when the PD is connected per any valid 4-pair configuration, as defined in Table 145–20, to any voltage in the range of $V_{Port\_PSE\text{-}2P}$ min + 0.31 V to $V_{Port\_PSE\text{-}2P}$ max through two common mode resistances, R_{source_min} and R_{source_max}, as defined in Equation (145–27) and shown in Figure 145–32.

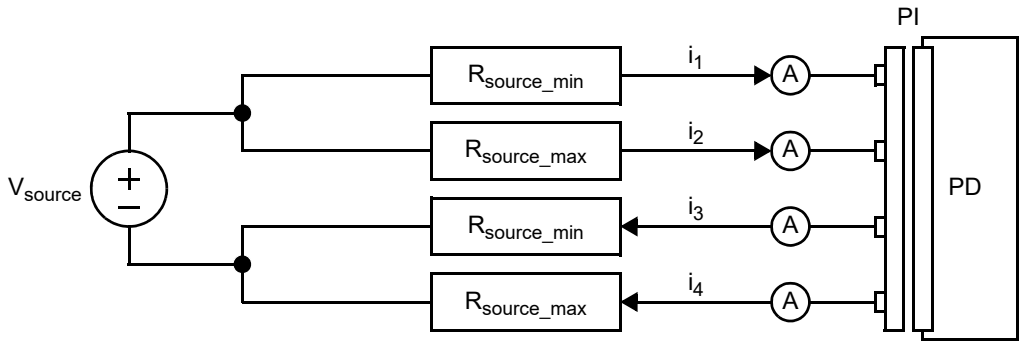

Figure 145–32—PD current unbalance verification circuit

Dual-signature PDs shall not exceed $I_{Con\_PD\text{-}2P}$, as defined in Equation (145–28), for longer than T_{CUT} min and 5 % duty cycle, as defined in Table 145–16, and shall not exceed $I_{Peak\_PD\text{-}2P}$, as defined in Equation (145–29), on any pair when the PD is connected per any valid 4-pair configuration, as defined in Table 145–20, to any voltage in the range of $V_{Port\_PSE\text{-}2P}$ min + 0.31 V to $V_{Port\_PSE\text{-}2P}$ max through two common mode resistances, R_{source_min} and R_{source_max}, as defined in Equation (145–27) and shown in Figure 145–32.

The unbalance current requirements for PDs apply at the PD PI connector (jack) when mated with a specified balanced cabling connector (plug).

NOTE 1—The duty cycle of the peak current is measured using a sliding window with a width of 1 second.

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$$R_{source\_max} = \left\{ \begin{array}{l} (-0.03 \times R_{source\_min} + 1.324) \times R_{source\_min} \text{ for } (0.145\Omega \le R_{source\_min} \le 5.47\Omega) \end{array} \right\}_{\Omega} \quad (145\text{–}27)$$

$$I_{Con\_PD\text{-}2P} = \left\{ \frac{P_{Class\_PD\text{-}2P}}{V_{PD}} \right\}_{A} \quad (145\text{–}28)$$

$$I_{Peak\_PD\text{-}2P} = \left\{ \frac{P_{Peak\_PD\text{-}2P}}{V_{PD}} \right\}_{A} \quad (145\text{–}29)$$

where

R_{source_min} is the lowest supported common mode effective source resistance in the powered pairs of the same polarity

$P_{Class\_PD\text{-}2P}$ is the maximum power at the PD PI per the PDs assigned Class, as defined in Table 145–29

$P_{Peak\_PD\text{-}2P}$ is the peak power a dual-signature PD may draw per its assigned Class on a pairset; see Table 145–29

V_{PD} is the voltage at the PD PI as defined in 145.1.3

R_{source_min} and R_{source_max} represent the V_{source} source common mode effective resistance that consists of the PSE PI components (R_{PSE_min} and R_{PSE_max} as defined in 145.2.10.6.1, $V_{Port\_PSE\_diff}$ as defined in Table 145–16, the link section resistance, and influence of R_{PD_min} and R_{PD_max} as function of system end-to-end unbalance). Common mode effective resistance is the resistance of two conductors of the same pair and their other components, which form R_{source}, connected in parallel including the effect of the system (PSE and PD) pair to pair voltage difference.

R_{PD_min}, R_{PD_max}, along with any other parts of the system, i.e., link section and the PSE, bounds the maximum current such that the maximum pair current including unbalance does not exceed $I_{Unbalance\_PD\text{-}2P}$ as defined in Table 145–16 during normal operating conditions. See Annex 145A.

NOTE 2—The pairset current limit requirement also holds when R_{source_max} and R_{source_min} are exchanged.

145.3.9 PD Maintain Power Signature

A PD that requires power from the PI shall provide a valid Maintain Power Signature (MPS) at the PI. A PD that does not maintain the MPS components may have its power removed within the limits of T_{MPDO} as defined in Table 145–16. I_{Port_MPS}, $I_{Port\_MPS\text{-}2P}$, T_{MPS_PD}, and T_{MPDO_PD}, are defined in Table 145–32. T_{LCE_PD} is defined in Table 145–25.

For single-signature PDs the MPS shall consist of current draw equal to or above I_{Port_MPS} for a minimum duration of T_{MPS_PD} followed by an optional MPS dropout for no longer than T_{MPDO_PD}. A single-signature PD shall use the I_{Port_MPS} value associated with assigned Class 1 to 4 when pse_assigned_class is 1, 2, 3, or 4, and MirroredPSEAllocatedPowerValue and PDRequestedPowerValue are less or equal to 255. A single-signature PD shall use the I_{Port_MPS} value associated with assigned Class 5 to 8 when pse_assigned_class is 5, 6, 7, or 8, or when PDRequestedPowerValue is in the range of 256 to 999. When PDRequestedPowerValue or PSEAllocatedPowerValue is equal to 0xACAC, the PD shall use the I_{Port_MPS} value associated with the assigned Class.

For dual-signature PDs the MPS shall consist of current draw equal to or above $I_{Port\_MPS\text{-}2P}$ on each powered pairset independently for a minimum duration of T_{MPS_PD} followed by an optional MPS dropout for no longer than T_{MPDO_PD}.

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Table 145–32—PD DC Maintain Power Signature

Item	Parameter	Symbol	Units	Min	Max	Conditions
1	Total input current per the assigned Class, for single-signature PDs					
	Class 1 to 4	I_{Port_MPS}	A	0.01	—	See 145.3.9
	Class 5 to 8			0.016		
2	Input current on each powered pairset for dual-signature PDs					
	Class 1 to 5	I_{Port_MPS-2P}	A	0.01	—	—
3	PD Maintain Power Signature Time	T_{MPS_PD}	ms	75	—	long_class_event = FALSE
				7	—	long_class_event = TRUE
4	PD Drop Out Period	T_{MPDO_PD}	ms	—	250	long_class_event = FALSE
				—	310	long_class_event = TRUE
NOTE—PDs may not be able to meet the I_{Port_MPS} or I_{Port_MPS-2P} specification in Table 145–32 during the maximum allowed port voltage droop (V_{Port_PSE-2P} max to V_{Port_PSE-2P} min with series resistance R_{Ch}). Such a PD should increase its I_{Port} or $I_{Port-2P}$ or make other such provisions to meet the Maintain Power Signature.						

A PD connected to a Type 1 or Type 2 PSE, shall also present input impedance with resistive and capacitive components defined in Table 145–33.

Table 145–33—PD Maintain Power Signature

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Input resistance	R_{pd_d}	kΩ	—	26.3	—
2	Input capacitance	C_{pd_d}	µF	0.05	—	—

PDs that detect a long first class event in the range of T_{LCE_PD} may use the shorter T_{MPS_PD} in order to draw a lower standby MPS power. In the absence of a long first class event, the minimum T_{MPS_PD} is higher and the standby MPS power is also higher.

A PD shall meet the T_{MPS_PD} and T_{MPDO_PD} requirements with any series resistance less than or equal to R_{Chan} max between the PD PI and the source.

Powered PDs that no longer require power, and identify the PSE as Type 1 or Type 2, shall remove both the current draw and impedance components of the MPS. To cause Type 1 and Type 2 PSE power removal, the impedance of the PI should rise above 1980 kΩ.

Powered PDs that no longer require power, and identify the PSE as Type 3 or Type 4, shall remove the current draw component and may remove the impedance components of the MPS. See 145.2.12, 145.2.10.4, and 145.3.8.8.

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145.4 Additional electrical specifications

This clause defines additional electrical specifications for a fully connected PoE system (that is, PSE, cabling, PD, and related PHYs) and therefore to each element of such a system. The specifications apply for all PSE and PD operating conditions at the cabling side of the mated connection of the PI. The requirements apply during data transmission only when specified as an operating condition.

The requirements of 145.4 are consistent with the requirements of the 10BASE-T MAU and the 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T PHYs.

145.4.1 Electrical isolation

PDs and PSEs shall provide isolation between all accessible external conductors, including frame ground (if any), and all MDI leads including those not used by the PD or PSE. Any equipment that can be connected to a PSE or PD through a non-MDI connector that is not isolated from the MDI leads needs to provide isolation between all accessible external conductors, including frame ground (if any), and the non-MDI connector. External accessibility to conductors is specified in Section 5.4.10.1 b) of IEC 62368-1:2018.

This electrical isolation shall meet the isolation requirements as specified in J.1 with electrical strength test c) details being replaced by: “An impulse test consisting of a 1500 V, 10/700 waveform, applied 10 times, with a 60 s interval between pulses. The shape of the impulses is 10/700 (10 μs virtual front time, 700 μs virtual time to half value), as defined in ITU-T Recommendation K.44.”

Conductive link segments that have differing isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of network interface devices (NID).

In a multiport system, the implementer should maintain DC isolation through the termination circuitry to eliminate cross-port leakage currents. See 145.2.10.4.

Dual-signature PDs shall have less than or equal to 10 μA of current between any negative conductor of Mode A and any negative conductor of Mode B when V_{PD}, as defined in 145.1.3, is less than V_{Off_PD} min, as defined in Table 145–29, on either Mode. See Table 79–15.

145.4.1.1 Electrical isolation environments

There are two electrical power distribution environments to be considered that require different electrical isolation properties. They are as follows:

— **Environment A:** When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.
— **Environment B:** When a LAN crosses the boundary between separate power distribution systems or the boundaries of a single building.

145.4.1.1.1 Environment A requirements

Attachment of network segments via NIDs that have multiple instances of a twisted-pair MDI requires electrical isolation between each segment and the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or PHY (see 14.3.1.1, 25.4.6, and 40.6.1.1). Equipment with multiple instances of PSE, PD, or both shall meet or exceed the isolation requirement of the MAU/PHY with which they are associated.

An Environment A multiport NID does not require electrical power isolation between link segments.

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An Environment A PSE shall switch the more negative conductor. It is allowed to switch both conductors.

145.4.1.1.2 Environment B requirements

The attachment of network segments that cross Environment A boundaries requires electrical isolation between each segment and all other attached segments as well as to the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or PHY (see 14.3.1.1, 25.4.6, and 40.6.1.1). Equipment with multiple instances of PSE, PD, or both shall meet or exceed the isolation requirement of the MAU/PHY with which each is associated.

An environment B PSE that supports 4-pair power shall switch the more negative conductor. It is allowed to switch both conductors.

The requirements for interconnected electrically conducting link segments that are partially or fully external to a single building environment may require additional protection against lightning strikes or other hazards. Protection requirements for such hazards are beyond the scope of this standard. Guidance on these requirements may be found in Section 6 of IEC 60950-1:2001 and throughout IEC 62368-1, as well as any local and national codes related to safety.

145.4.2 Fault tolerance

Each conductor pair of the PI, when it is also an MDI (e.g., an Endpoint PSE or PD), shall meet the fault tolerance requirements of the appropriate specifying clause. (See 14.3.1.2.7, 25.4, 40.8.3.4, 55.8.2.3, and 126.8.2.4.) When a PI is not an MDI (e.g., a Midspan PSE), the PSE PI shall meet the fault tolerance requirements of this subclause.

The PSE shall withstand without damage the application of short circuits of any conductors within the cable for an indefinite period of time. The magnitude of the current caused by a short circuit of any one conductor to another conductor in the cable

— Shall not exceed $I_{PSEUT\text{-}Type3\text{-}2P}$, as defined in Equation (145–17), for Type 3 PSEs.
— Shall not exceed $I_{PSEUT\text{-}Type4\text{-}2P}$, as defined in Equation (145–18), for Type 4 PSEs.

Each conductor pair shall withstand, without damage, a 1000 V common-mode impulse applied at E_{cm} of either polarity. The shape of the impulse shall be (0.3/50) μs (300 ns virtual front time, 50 μs virtual time of

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half value), as defined in IEC 60060, where E_{cm} is an externally applied AC voltage as shown in Figure 145–33.

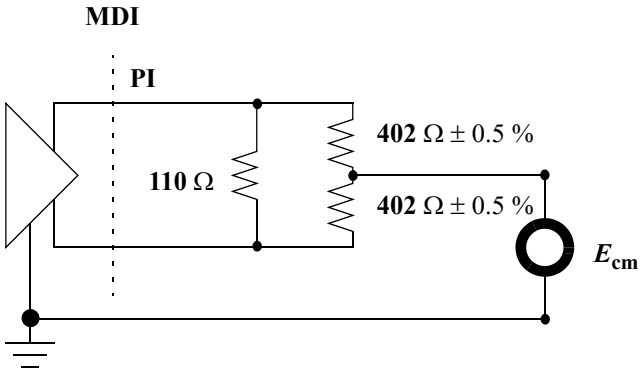

Figure 145–33—PI fault tolerance test circuit

NOTE—PDs may receive power from a PSE over fewer conductors than specified when a link section has a fault of one or more conductor open failures.

145.4.3 Impedance balance

Impedance balance is a measurement of the common-mode-to-differential-mode offset of the PI. The common-mode-to-differential-mode impedance balance for the transmit and receive pairs shall exceed the limits in Table 145–34 for all supported PHY speeds.

Table 145–34—Impedance balance limits for supported speeds

Supported speed	Impedance balance limit (dB)	Frequency range
10 Mb/s MAU	$29 - 17 \times \log_{10}(f/10)$	$1 \le f \le 20$ MHz
100 Mb/s or 1000 Mb/s PHY	$34 - 19.2 \times \log_{10}(f/50)$	$1 \le f \le 100$ MHz
2.5 Gb/s PHY	48	$1 \le f < 10$ MHz
	$48 - 20 \times \log_{10}(f/10)$	$10 \le f < 20$ MHz
	$42 - 15 \times \log_{10}(f/20)$	$20 \le f \le 125$ MHz
5 Gb/s PHY	48	$1 \le f < 30$ MHz
	$44 - 19.2 \times \log_{10}(f/50)$	$30 \le f \le 250$ MHz
10 Gb/s PHY	48	$1 \le f < 30$ MHz
	$44 - 19.2 \times \log_{10}(f/50)$	$30 \le f \le 500$ MHz

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The impedance balance is defined as shown in Equation (145–30):

$$\left\{20 \times \log_{10}\left(\frac{E_{cm}}{E_{dif}}\right)\right\}_{dB} \quad (145–30)$$

where

E_{cm} is an externally applied sinusoidal voltage as shown in Figure 145–34
E_{dif} is the voltage of the resulting waveform due only to the applied sine wave measured as shown in Figure 145–34

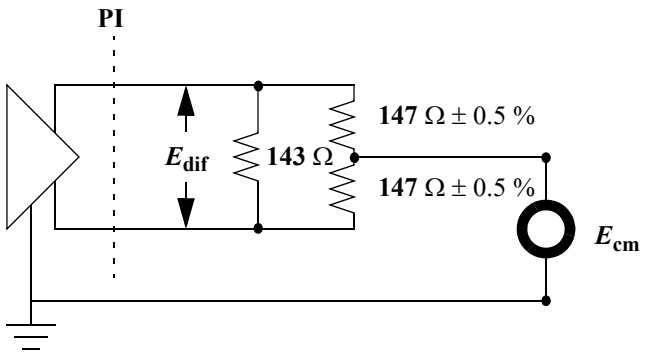

Figure 145–34—PI impedance balance test circuit

145.4.4 Common-mode output voltage

The magnitude of the common-mode AC output voltage measured according to Figure 145–35 and Figure 145–36 at the transmit PI while transmitting data and with power applied, E_{cm_out}, shall not exceed the values in Table 145–35 while operating at the specified speed, when measured over the specified bandwidth.

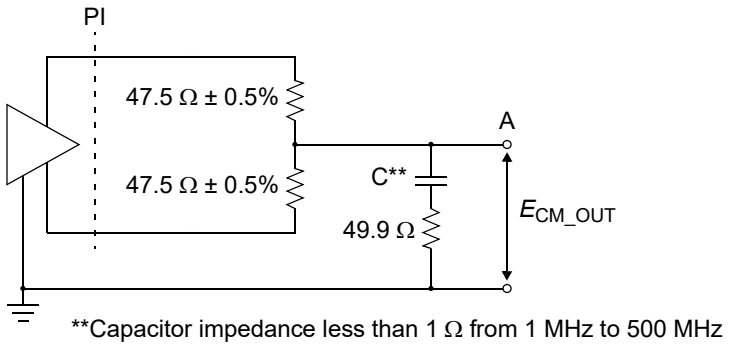

Figure 145–35—Common-mode output voltage test

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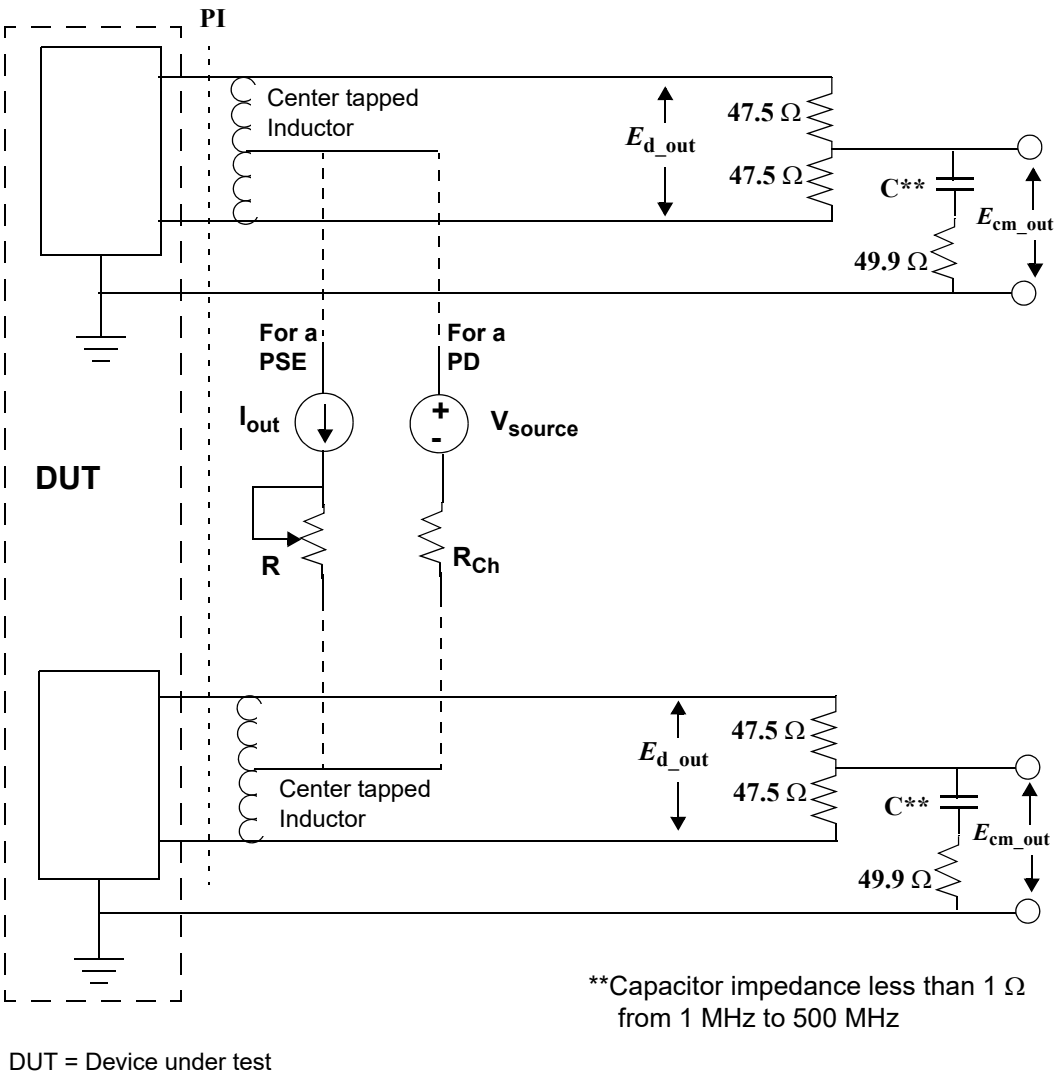

Figure 145–36—PSE and PD terminations for common-mode output voltage test

Table 145–35—Common-mode output voltage for given operating speed

Operating speed	Common-mode output voltage (E_{cm_out})	Measurement bandwidth
10 Mb/s MAU	50 mV peak	$1 \leq f \leq 100$ MHz
100 Mb/s or 1000 Mb/s PHY	50 mV_{pp}	$1 \leq f \leq 100$ MHz
2.5 Gb/s PHY	50 mV_{pp}	$1 \leq f \leq 100$ MHz
5 Gb/s PHY	50 mV_{pp}	$1 \leq f \leq 250$ MHz
10 Gb/s PHY	50 mV_{pp}	$1 \leq f \leq 500$ MHz

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The common-mode AC output voltage shall be measured while the PHY is transmitting data, the PSE or PD is operating with the following PSE load or PD source:

1) For a PSE, the PI that supplies power is terminated as illustrated in Figure 145–36. The PSE load, R, in Figure 145–36 is adjusted so that the PSE output current, I_{out}, is 16 mA and then I_{Cable} for 2-pair operation or 2 × I_{Cable} for 4-pair operation, while measuring E_{cm_out} on the PI.
2) For a PD, the PI that requires power shall be terminated as illustrated in Figure 145–36. V_{source} in Figure 145–36 is adjusted to 36 Vdc and 57 Vdc, while measuring E_{cm_out} on the PI.

NOTE—The implementer should consider any applicable local, national, or international regulations that may require more stringent specifications. One such specification can be found in the European Standard EN 55022:1998.

145.4.5 Pair-to-pair output noise voltage

The pair-to-pair output noise voltage (see Figure 145–37) is limited by the resulting electromagnetic interference due to this AC voltage. This AC voltage can be ripple from the power supply, Table 145–16, 'power feeding ripple and noise', or from any other source. A system integrating a PSE shall comply with applicable local and national codes for the limitation of electromagnetic interference.

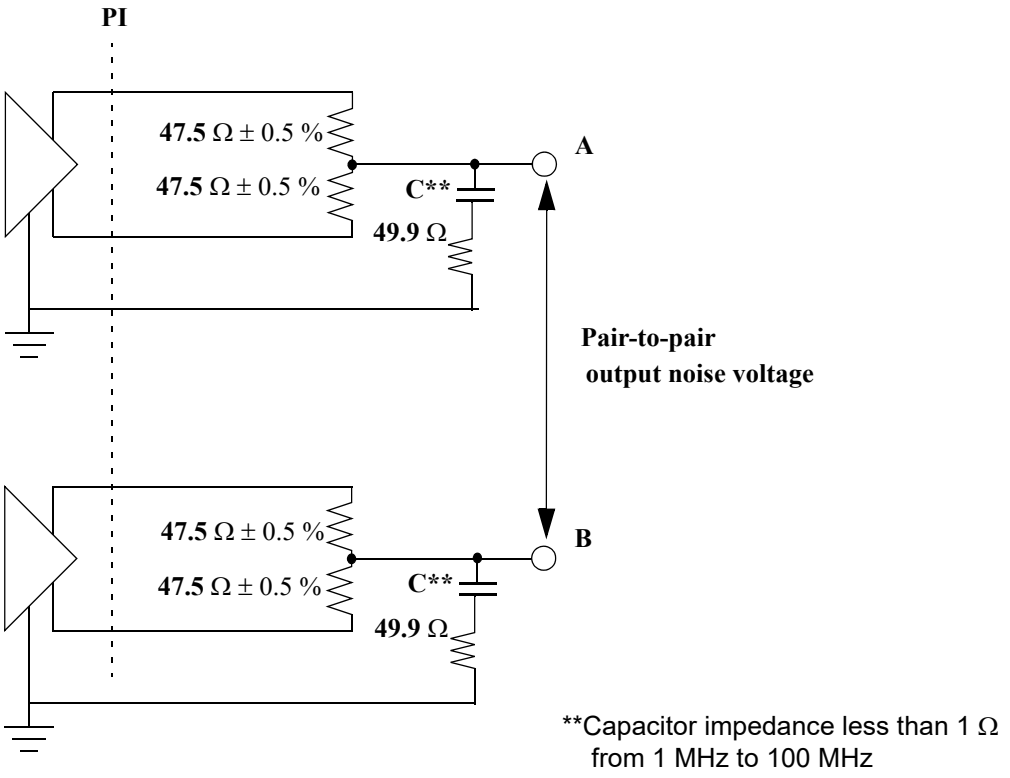

Figure 145–37—Pair-to-pair output noise voltage test

145.4.6 Differential noise voltage

For 10/100/1000 Mb/s, the coupled noise, E_{d_out} in Figure 145–36, from a PSE or PD to the differential transmit and receive pairs shall not exceed 10 mV peak-to-peak when measured from 1 MHz to 100 MHz under the conditions specified in 145.4.4, item 1) and item 2).

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For 2.5GBASE-T, 5GBASE-T, or 10GBASE-T, the coupled noise, E_{d_out} in Figure 145–36, from a PSE or PD to the differential transmit and receive pairs shall not exceed 10 mV peak-to-peak when measured in the band from 1 MHz to 10 MHz and shall not exceed 1 mV peak-to-peak when measured in the band from 10 MHz to 100 MHz for 2.5GBASE-T, 10 MHz to 250 MHz for 5GBASE-T, and 10 MHz to 500 MHz for 10GBASE-T under the conditions specified in 145.4.4, item 1) and item 2).

145.4.7 Return loss

The differential impedance of the transmit and receive pairs at the PHY's MDI shall be such that any reflection shall meet the return loss requirements as specified

— In 14.3.1.3.4 for a 10 Mb/s PHY.
— In ANSI INCITS 263-1995 for a 100 Mb/s PHY.
— In 40.8.3.1 for a 1000 Mb/s PHY.
— In 126.8.2.2 for a 2.5 Gb/s or 5 Gb/s PHY.
— In 55.8.2.1 for a 10 Gb/s PHY.

In addition, all pairs terminated at an MDI should maintain a nominal common-mode impedance of 75 Ω. The common-mode termination is affected by the presence of the power supply, and this should be considered to determine proper termination.

145.4.8 100BASE-TX transformer droop

100BASE-TX systems may contain a legacy PHY receiver that expects to be connected to a PHY transmitter with 350 μH open circuit inductance (OCL). Alternative A Midspan PSEs that support 100BASE-TX shall enforce intra-pair current unbalance (see 145A.1) less than or equal to I_{unb} (see 145.2.10.12) or meet 145.4.9.3.

100BASE-TX Endpoint PSEs and 100BASE-TX PDs shall meet the requirements of Clause 25 in the presence of (I_{unb}/2).

145.4.9 Midspan PSE device additional requirements

The cabling specifications for 100 Ω balanced cabling are described in ISO/IEC 11801:2002. Cable conforming to ANSI/TIA-568-C.2 also meets these requirements. Some cable category specifications that only appear in earlier editions are also supported. The terms "channel" and "permanent link" are defined in ISO/IEC 11801-1 subsection 5.3.5. Midspan PSE cabling system requirements are specified in 145.1.4.

ISO/IEC 11801-1 defines in 5.1 two types of Equipment interface to the cabling system: "Interconnect model" and the "cross-connect model." An equivalent "Interconnect model" and "cross-connect model" may be found in ANSI/TIA-568.0-D, 5.1. See Figure 145–38.

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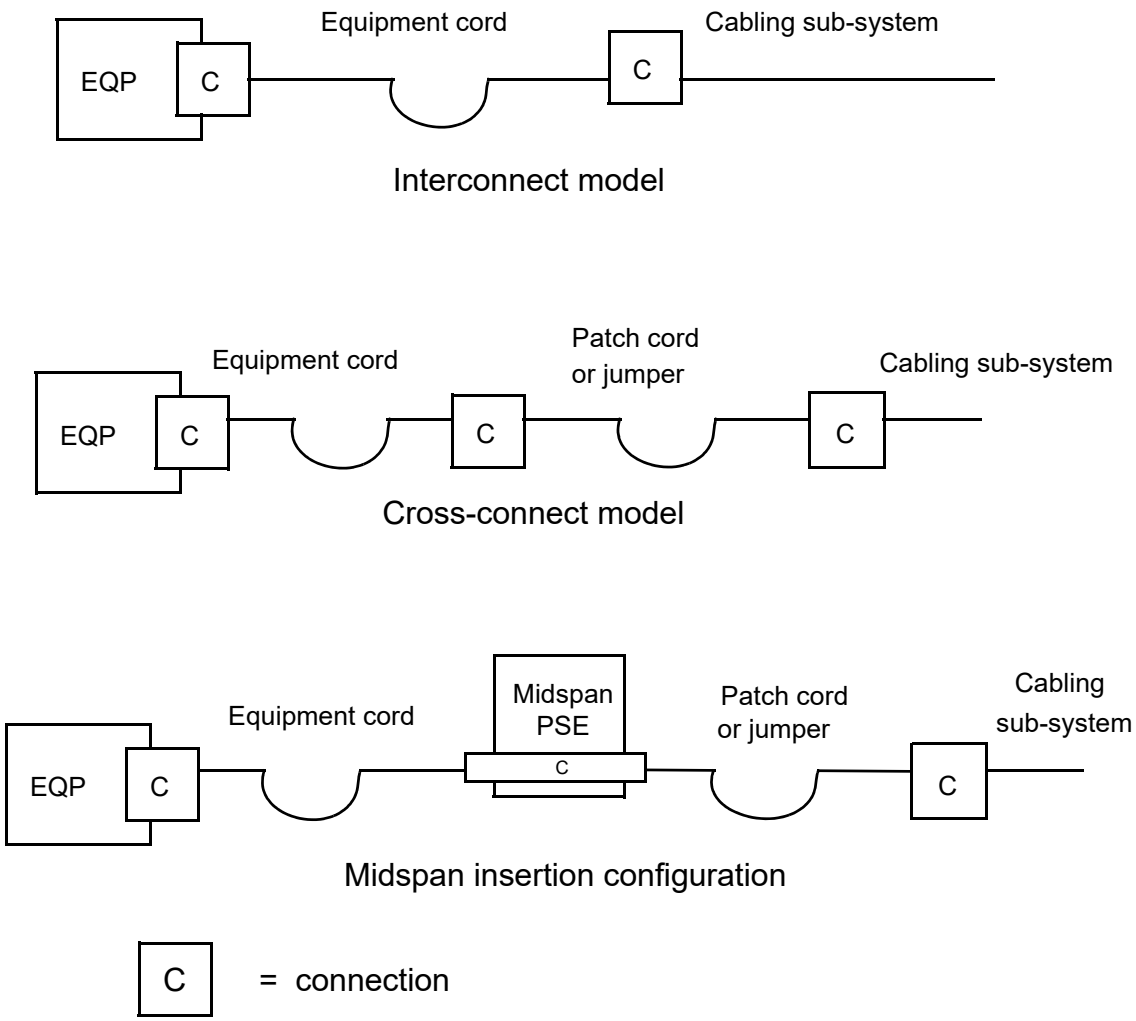

Figure 145–38—Interconnect model, cross-connect model, and midspan insertion configuration

The insertion of a Midspan PSE at the Floor Distributor (FD) shall comply with the following guidelines:

a) If the existing FD configuration is of the “Interconnect model” type, the Midspan PSE can be added, provided it does not increase the insertion loss of the resulting “channel” to more than specified for the same Class or category 100 m channel defined in ISO/IEC 11801-1 or ANSI/TIA-568.0-D.

b) If the existing FD configuration is of the “Cross-connect model” type, the Midspan PSE can be installed instead of one of the connection pairs in the FD. In addition, the installation of the Midspan PSE shall not increase the insertion loss of the resulting “channel” to more than specified for the same Class or category 100 m channel defined in ISO/IEC 11801-1 or ANSI/TIA-568.0-D.

c) For a 10GBASE-T midspan PSE, in meeting either of the above requirements, the Midspan PSE may be substituted for up to two connection pairs in the FD.

Configurations with the Midspan PSE in the cabling “channel” shall not alter the transmission requirements of the “permanent link.” A Midspan PSE shall not provide DC continuity between the two sides of the segment for the pairs that inject power.

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The requirements for the two pair Category 5 link segment are found in 25.4.9. Specification of 4-pair cabling is beyond the scope of Clause 25.

NOTE—Appropriate terminations may be applied to the interrupted pairs on both sides of the Midspan device.

145.4.9.1 Connector Midspan PSE device transmission requirements

A connector Midspan PSE replaces one of the connectors in the link segment and shall meet the following transmission parameters. These parameters should be measured using the test procedures of ISO/IEC 11801-1 or ANSI/TIA-568-C.2 for connecting hardware.

There are five variants of Midspan PSEs defined with respect to transmission requirements:

1) 10BASE-T/100BASE-TX connector Midspan PSE
2) 1000BASE-T connector Midspan PSE
3) 2.5GBASE-T connector Midspan PSE
4) 5GBASE-T connector Midspan PSE
5) 10GBASE-T connector Midspan PSE

145.4.9.1.1 Near End Crosstalk (NEXT)

NEXT loss is a measure of the unwanted signal coupling from a transmitter at the near-end into neighboring pairs measured at the near-end. NEXT loss is expressed in dB relative to the received signal level. For operation with 2.5GBASE-T and lower rates, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–31) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. For 5GBASE-T, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–31) when measured for the transmit and receive pairs from 1 MHz to 250 MHz. For operation with 5GBASE-T and lower rates, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB.

$$\{NEXTconn\}_{\text{dB}} \geq 43 - 20 \times \log_{10}\left(\frac{f}{100}\right) \tag{145–31}$$

where

NEXTconn is the Near End Crosstalk loss in dB
f is the frequency expressed in MHz

For 10GBASE-T operation, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–32) when measured for the transmit and receive pairs from 1 MHz to 500 MHz. However, for frequencies that correspond to calculated values greater than 75 dB, the requirement reverts to the minimum requirement of 75 dB.

$$\{NEXTconn\}_{\text{dB}} \leq \left\{ \begin{array}{ll} 54 - 20 \times \log_{10}\left(\frac{f}{100.}\right) & \text{for } (1 \leq f \leq 250) \\ 46.04 - 40 \times \log_{10}\left(\frac{f}{250}\right) & \text{for } (250 < f \leq 500) \end{array} \right\}_{\text{dB}} \tag{145–32}$$

where

NEXTconn is the Near End Crosstalk loss in dB
f is the frequency expressed in MHz

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145.4.9.1.2 Insertion loss

Insertion loss is a measure of the signal loss between the transmitter and receiver, expressed in dB relative to the received signal level. For other than 5GBASE-T or 10GBASE-T operation, insertion loss for Midspan PSE devices shall meet the values determined by Equation (145–33) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. For 5GBASE-T capable midspans, insertion loss for Midspan PSE devices shall meet the values determined by Equation (145–33) when measured for the transmit and receive pairs from 1 MHz to 250 MHz. For 10GBASE-T operation, insertion loss for Midspan PSE devices shall meet the values determined by Equation (145–33) when measured from the transmit and receive pairs from 1 MHz to 500 MHz. For frequencies that correspond to calculated values less than 0.1 dB, the requirement reverts to the maximum requirement of 0.1 dB.

$$\{ILconn\}_{\text{dB}} \leq 0.04 \times \sqrt{f} \qquad (145–33)$$

where

ILconn is the insertion loss in dB
f is the frequency expressed in MHz

145.4.9.1.3 Return loss

Return loss is a measure of the reflected energy caused by impedance mismatches in the cabling system and is expressed in dB relative to the reflected signal level. Return loss for Midspan PSE devices shall meet or exceed the values specified in Table 145–36.

Table 145–36—Connector return loss

Midspan PSE Variant	Frequency	Return loss
10/100/1000BASE-T	1 MHz ≤ f < 20 MHz	23 dB
	20 MHz ≤ f ≤ 100 MHz	14 dB
2.5GBASE-T	1 MHz ≤ f < 31.5 MHz	30 dB
	31.5 MHz ≤ f < 100 MHz	20 – 20 $\log_{10}$(f/100)
5GBASE-T	1 MHz ≤ f < 31.5 MHz	30 dB
	31.5 MHz ≤ f < 250 MHz	20 – 20 $\log_{10}$(f/100)
10GBASE-T	1 MHz ≤ f < 79 MHz	30 dB
	79 MHz ≤ f ≤ 500 MHz	28 – 20 $\log_{10}$(f/100)

145.4.9.2 Cord Midspan PSE

A Midspan PSE replaces an element in a link segment and shall meet or exceed the insertion loss, NEXT, and return loss values specified Table 145–37 for all data transmitting pairs.

There are five variants of Midspan PSEs defined with respect to transmission requirements:

1) 10BASE-T/100BASE-TX cord Midspan PSE
2) 1000BASE-T cord Midspan PSE
3) 2.5GBASE-T cord Midspan PSE

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4) 5GBASE-T cord Midspan PSE
5) 10GBASE-T cord Midspan PSE

Table 145–37—Cord specifications for use with Midspan PSEs

Highest PHY rate supported	Cord specification	Frequency range
Up to 1000BASE-T	Category 5 cord in ISO/IEC 11801:2002 or ANSI/TIA-568-A:1995	1 MHz ≤ f ≤ 100 MHz
Up to 2.5GBASE-T	Category 5e cord in ISO/IEC 11801:2002 or ANSI/TIA-568-C.2	1 MHz ≤ f ≤ 100 MHz
Up to 5GBASE-T	Category 6 cord in ISO/IEC 11801:2002 or ANSI/TIA-568-C.2	1 MHz ≤ f ≤ 250 MHz
Up to 10GBASE-T	Category 6A cord in ISO/IEC 11801-1 or ANSI/TIA-568-C.2	1 MHz ≤ f ≤ 500 MHz

145.4.9.2.1 Maximum link delay

The propagation delay contribution of the Midspan PSE device shall not exceed 2.5 ns from 1 MHz to the highest referenced frequency.

145.4.9.2.2 Maximum link delay skew

The propagation delay skew of the Midspan PSE device shall not exceed 1.25 ns from 1 MHz to the highest referenced frequency.

145.4.9.3 Midspan signal path requirements

An Alternative A Midspan PSE transfer function gain shall be greater than that expressed by Equation (145–34) for the frequency range from 0.1 MHz to 1 MHz, at the pins of the PI used as 100BASE-TX transmit pins.

$$\left\{ -0.1 + 37.5 \times \log_{10}\left(\frac{22.4 \times f}{\sqrt{1 + 521 \times f^2}} \right) \right\}_{\text{dB}} \quad (145\text{–}34)$$

where

f is the frequency expressed in MHz

The requirements shall be met with a DC bias current, I_{bias}, between 0 mA and (I_{unb}/2) mA (I_{unb} is defined in Table 145–16).

145.4.9.3.1 Alternative A Midspan PSE signal path transfer function

The transfer function is measured by applying a test signal to the Midspan PSE signal input through a source impedance of 100 Ω ± 1 %. The Midspan PSE signal input and output may be connected to a 0.5 m maximum length of cable, meeting the requirements of 25.4.9, terminated with 100 Ω ± 1 %.

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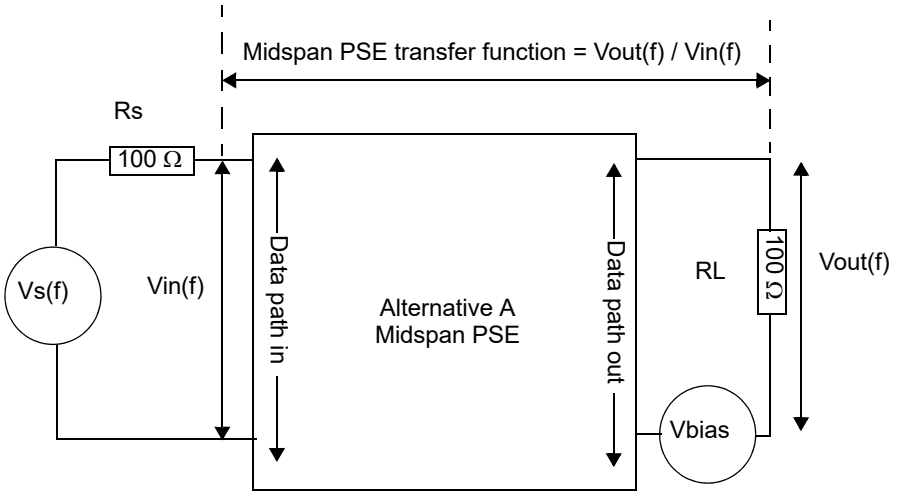
The transfer function is defined from the output termination to the Midspan PSE input. See Figure 145–39.



Vin(f) is the sine wave signal to be used to measure the Midspan PSE transfer function.
Vbias is the DC offset voltage to be applied in series with RL in order to generate I_{bias}.
Vout(f) is the Midspan PSE response to Vin(f).
Some test equipment may require isolation between measurement ports.

Figure 145–39—Measurement setup for Alternative A Midspan PSE transfer function

145.4.9.4 Coupling parameters between link segments

Midspan PSEs intended for operation with 2.5G/5G/10GBASE-T (variants 3 through 5 in 145.4.9.1 and 145.4.9.2) are additionally required to meet the following specifications for PSANEXT and PSAFEXT for coupling signals between ports relating to different link segments. Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. To bound the total alien NEXT loss and alien FEXT loss coupled between link segments, multiple disturber alien near-end crosstalk (MDANEXT) loss and multiple disturber alien FEXT (MDAFEXT) loss is specified.

145.4.9.4.1 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

PSANEXT loss for 2.5G/5G/10GBASE-T capable Midspan PSE devices shall meet or exceed the values determined using Equation (145–35). For other than 5GBASE-T or 10GBASE-T operation, PSANEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–35) from 1 MHz to 100 MHz. For 5GBASE-T capable midspans, PSANEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–35) from 1 MHz to 250 MHz. For 10GBASE-T capable midspans, PSANEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–35) from 1 MHz to 500 MHz. When the computed PSANEXT value at a certain frequency exceeds 67 dB, the PSANEXT result at that frequency is for information only.

$$\text{PSANEXT loss} = 70.5 - 20 \times \log_{10}(f/100) \quad (145–35)$$

145.4.9.4.2 Multiple disturber power sum alien far-end crosstalk (PSAFEXT) loss

PSAFEXT loss for 2.5G/5G/10GBASE-T capable Midspan PSE devices shall meet or exceed the values determined in Equation (145–36). For other than 5GBASE-T or 10GBASE-T operation, PSAFEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–36) from 1 MHz to 100 MHz. For

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5GBASE-T capable midspans, PSAFEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–36) from 1 MHz to 250 MHz. For 10GBASE-T capable midspans, PSAFEXT loss for Midspan PSE devices shall meet the values determined by Equation (145–36) from 1 MHz to 500 MHz. When the computed PSAFEXT value at a certain frequency exceeds 67 dB, the PSAFEXT result at that frequency is for information only.

$$\text{PSAFEXT loss} = 67 - 20 \times \log_{10}(f / 100) \quad (145\text{–}36)$$

145.5 Data Link Layer classification

Additional control and classification functions are supported using Data Link Layer classification using frames based on the IEEE 802.3 Organizationally Specific TLVs defined in Clause 79. Single-signature PDs that request Class 4 or higher and dual-signature PDs that request Class 4 or higher on either Mode support Data Link Layer classification (see 145.3.6). Data Link Layer classification is optional for all other devices.

145.5.1 TLV frame definition

Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB-2016; shall support the Power via MDI Type, Length, Value (TLV) defined in 79.3.2 and may support the Power via MDI Measurements TLV defined in 79.3.8.

All reserved fields in transmitted Power via MDI TLVs shall contain zero, and all reserved fields in received Power via MDI TLVs shall be ignored.

145.5.2 Data Link Layer classification timing requirements

PSEs shall send an LLDPDU containing a Power via MDI TLV within 10 seconds of Data Link Layer classification being enabled in the PSE as indicated by the variable pse_dll_enable (145.2.5.4, 145.5.3.2.2).

PDs shall set the variable pd_dll_ready within 5 minutes of Data Link Layer classification being enabled in a PD as indicated by the variable pd_dll_enable (145.3.3.3.2, 145.3.3.4.2, and 145.5.3.3.1).

The PSE shall send an LLDPDU containing a Power via MDI TLV with an updated value for the ‘PSE allocated power value’ field, ‘PSE allocated power value Alternative A’ field, and ‘PSE allocated power value Alternative B’ field within 10 seconds of receiving an LLDPDU containing a Power via MDI TLV where the ‘PD requested power value’ field, ‘PD requested power value for Mode A’ field, or ‘PD requested power value for Mode B’ field is different from the previously communicated value.

The PD shall send an LLDPDU containing a Power via MDI TLV with an updated value for the ‘PD requested power value’ field, ‘PD requested power value for Mode A’ field, and ‘PD requested power value for Mode B’ field within 10 seconds of receiving an LLDPDU containing a Power via MDI TLV where the ‘PSE allocated power value’ field, ‘PSE allocated power value Alternative A’ field, or ‘PSE allocated power value Alternative B’ field is different from the previously communicated value.

145.5.3 Power control state diagrams

The power control state diagrams for PSEs and PDs specify the externally observable behavior of a PSE and PD Data Link Layer classification respectively.

Data Link Layer classification of PSEs shall provide the behavior in the state diagrams defined in Figure 145–40, Figure 145–41, Figure 145–42, and Figure 145–43.

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Single-signature PD Data Link Layer classification shall provide the behavior of the state diagrams defined in Figure 145–44 and Figure 145–45. Dual-signature PD Data Link Layer classification shall provide the behavior of the state diagram defined in Figure 145–46 and Figure 145–47.

145.5.3.1 Conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 145.2.5.2.

145.5.3.2 PSE power control state diagrams

145.5.3.2.1 Alternative designation

Dual-signature PSEs provide the behavior of the state diagram shown in Figure 145–46 over each pairset independently unless otherwise specified. All the parameters that apply to Alternative A and Alternative B are denoted with the suffix "_alt(X)" where "X" can be "A" or "B", or "_alt(P)" where "P" can be "A" or "B". A parameter that ends with the suffix "_alt(X)" may have different values for Alternative A and Alternative B.

PSEs providing power to a dual-signature PD operate over two semi-independent state diagrams, one for Alternative A, another for Alternative B. Alternative information is obtained by replacing the X in the desired variable or function with the letter of the Alternative of interest. Alternatives are referred to in general as follows:

X

Generic Alternative designator. When X is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams.
Values:
A: Alternative A
B: Alternative B

P

Powered Alternative designator. When P is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams. "P" refers to the Alternative that is currently powered. Its value is only defined when the PSE operates in 2-pair mode.
Values:
A: Alternative A
B: Alternative B

145.5.3.2.2 Variables

The PSE power control state diagrams in Figure 145–40, Figure 145–41, Figure 145–42, and Figure 145–43 use the following variables:

MirroredPDAutoclassRequest

The copy of the 'PD Autoclass request' field in the Power via MDI TLV that the PSE receives from the remote system. This variable is mapped from aLldpXdot3RemAutoclassRequest (30.12.3.1.35) and assigned through Table 145–38.
Values:
FALSE: The PD does not request an Autoclass measurement to be performed.
TRUE: The PD requests an Autoclass measurement to be performed.

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MirroredPDRequestedPowerValue

The copy of the ‘PD Requested Power Value’ field in the Power Via MDI TLV that the PSE receives from the remote system in units of 0.1 W. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17) and set through Table 145–38.

Values: 0 through 999, and 0xACAC

MirroredPDRequestedPowerValue_alt(X)

The copy of the ‘PD Requested Power Value’ field for Alternative(X) in the Power Via MDI TLV that the PSE receives from the remote system in units of 0.1 W. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValueA and aLldpXdot3RemPDRequestedPowerValueB attribute (30.12.3.1.18 and 30.12.3.1.19) and set through Table 145–38.

Values: 0 through 499

MirroredPSEAllocatedPowerValueEcho

The copy of the ‘PSE Allocated Power Value’ field in the Power Via MDI TLV that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.20) and set through Table 145–38.

Values: 0 through 999, and 0xACAC

MirroredPSEAllocatedPowerValueEcho_alt(X)

The copy of the ‘PSE Allocated Power Value’ field for Alternative(X) in the Power Via MDI TLV that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValueA and aLldpXdot3RemPSEAllocatedPowerValueB attribute (30.12.3.1.21 and 30.12.3.1.22) and set through Table 145–38.

Values: 0 through 499

PDRequestedPowerValueEcho

This variable is updated by the PSE state diagram. This variable maps into the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).

Values: 0 through 999, and 0xACAC

PDRequestedPowerValueEcho_alt(X)

This variable is updated by the PSE state diagram. This variable maps into the aLldpXdot3LocPDRequestedPowerValueA and aLldpXdot3LocPDRequestedPowerValueB attribute (30.12.2.1.18 and 30.12.2.1.19).

Values: 0 through 499

PSEAllocatedPowerValue

Integer that indicates the PSE allocated power value in the PSE in units of 0.1 W. The value is the maximum input average power (see 145.3.8.2) the PD ever draws. This variable maps to the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.20). A value higher than 713 indicates that the PSE is capable of supporting a power level beyond P_{Class_PD} at the PD PI. This may require an output power level higher than P_{Type} min. See 145.2.8.

Values: 0 through 999, and 0xACAC

PSEAllocatedPowerValue_alt(X)

Integer that indicates the PSE allocated power value in the PSE in units of 0.1 W. The value is the maximum input average power (see 145.3.8.2) the PD ever draws. This variable maps to the aLldpXdot3LocPSEAllocatedPowerValueA and aLldpXdot3LocPSEAllocatedPowerValueB attribute (30.12.2.1.21 and 30.12.2.1.22). A value higher than 356 indicates that the PSE is capable of supporting a power level beyond P_{Class_PD} at the PD PI. This may require an output power level higher than P_{Type} min. See 145.2.8.

Values: 0 through 499

PSEAutoclassCompleted

A Boolean that indicates the PSE has completed the PD Autoclass request. This variable is mapped into the aLldpXdot3LocAutoclassCompleted (30.12.2.1.34) attribute.

Values:

FALSE: The PSE has not completed the Autoclass measurement, or it is not performing an Autoclass measurement.

TRUE: The PSE has completed the Autoclass measurement.

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PSEAutoclassSupport

A Boolean variable that indicates if the PSE supports Autoclass in the PSE. This variable is mapped into the aLldpXdot3LocPSEAutoclassSupport (30.12.2.1.33) attribute.

Values:

FALSE: The PSE does not support Autoclass.

TRUE: The PSE supports Autoclass.

TempVar

A variable used to store Power Value in units of 0.1 W.

Values: 0 through 999, and 0xACAC

TempVar_alt(X)

A variable used to store a Power Value in units of 0.1 W.

Values: 0 through 499.

alt_pri

A variable used to select which Alternative assumes the role of Primary Alternative in the PSE state diagram in Figure 145–13.

Values:

a: Alternative A assumes the role of Primary Alternative. When operating over 4 pairs, Alternative B assumes the role of Secondary Alternative.

b: Alternative B assumes the role of Primary Alternative. When operating over 4 pairs, Alternative A assumes the role of Secondary Alternative.

fourpairmode

Alias for the following term: (alt_pwrd_pri * alt_pwrd_sec)

local_system_change

An implementation-specific variable that indicates that the local system wants to change the allocated power value. This indicates the PSE is going to change the power allocated to the PD. This variable may be set by the PSE at any time.

Values:

FALSE: The PSE does not want to change the power allocation.

TRUE: The PSE wants to change the power allocation.

local_system_change_alt(X)

An implementation-specific variable that indicates that the local system wants to change the allocated power value. This indicates the PSE is going to change the power allocated to the PD for Alternative(X). This variable may be set by the PSE at any time.

Values:

FALSE: The PSE does not wants to change the power allocation.

TRUE: The PSE wants to change the power allocation.

pse_alternative

This variable defined in 145.2.5.4 indicates which Pinout Alternative the PSE uses to apply power to the PI (see Table 145–3).

Values:

a: The PSE uses PSE pinout Alternative A.

b: The PSE uses PSE pinout Alternative B.

both: The PSE uses both Alternative A and Alternative B.

pse_dll_enable

A variable output by the PSE state diagram (Figure 145–13) to indicate if the PSE Data Link Layer classification mechanism is enabled.

Values:

FALSE: PSE Data Link Layer classification is not enabled.

TRUE: PSE Data Link Layer classification is enabled.

pse_dll_ready

See pse_dll_ready in 145.2.5.4.

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pse_initial_value

The value of this variable is valid after classification and is derived from the pse_allocated_pwr, pd_autoclass, and pd_autoclass_cancelled variables (145.2.5.4), which are used in the PSE state diagrams in 145.2.5.7. The value is quantized to fit the available resolution. Additional information on power levels for Class 8 may be found in 145.3.8.2.1. This variable is set per this description.

Values:

pse_allocated_pwr	pse_initial_value
1	39
2	65
3	130
4	255
5	400
6	510
7	620
8	713
Autoclass	44 204

NOTE—If pd_autoclass is TRUE and pd_autoclass_cancelled is FALSE, then pse_initial_value is set to the value 0xACAC (decimal 44 204).

pse_initial_value_alt(X)

The value of this variable is valid after classification and is derived from pse_allocated_pwr_pri and pse_allocated_pwr_sec variables (145.2.5.6), which are used in the PSE state diagrams in 145.2.5.7. The value is quantized to fit the available resolution. Additional information on power levels for Class 5 may be found in 145.3.8.2.1. This variable is set per this description.

Values:

pse_allocated_pwr_pri/sec	pse_initial_value_alt(X)
1	39
2	65
3	130
4	255
5	356

pse_power_update

A variable that is set when the PSEAllocatedPowerValue in the DLL state diagram in Figure 145–40 has been updated.

Values:

FALSE: The value of PSEAllocatedPowerValue has not changed.
TRUE: The value of PSEAllocatedPowerValue has changed.

pse_power_update_pri

A variable that is set when the PSEAllocatedPowerValue_alt(X) in the DLL state diagram in Figure 145–42 or Figure 145–43 has been updated.

Values:

FALSE: The value of PSEAllocatedPowerValue_alt(X) has not changed.
TRUE: The value of PSEAllocatedPowerValue_alt(X) has changed.

pse_power_update_sec

A variable that is set when the PSEAllocatedPowerValue_alt(X) in the DLL state diagram in Figure 145–42 or Figure 145–43 has been updated.

Values:

FALSE: The value of PSEAllocatedPowerValue_alt(X) has not changed.
TRUE: The value of PSEAllocatedPowerValue_alt(X) has changed.

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sig_type

A variable generated from the do_cxn_chk function of the PSE state diagram in Figure 145–13, which indicates if the PSE is connected to a single-signature PD or a dual-signature PD.

Values:

- invalid: Neither a single-signature PD nor a dual-signature PD connection check signature has been found. This includes an open circuit condition.
- single: The PSE has determined there is a single-signature PD configuration connected to the PI.
- dual: The PSE has determined there is a dual-signature PD configuration connected to the PI.

twopairmode

Alias for the following term: (alt_pwrd_pri ^ alt_pwrd_sec)

A summary cross-references between the Power over Ethernet classification local and remote object class attributes and the PSE power control state diagrams, including the direction of the mapping, is provided in Table 145–38.

145.5.3.2.3 Functions

do_autoclass_measure

A function defined in the PSE state diagram, which measures $P_{Autoclass}$ as defined in 145.2.8.2.

do_pse_power_review

This function evaluates the power allocation or budget of the PSE based on local system changes or changes of the PD requested power value.

The function returns the following variable:

pse_new_value:

The new maximum power value that the PSE expects the PD to draw in units of 0.1 W.

Valid values: 1 through 999, and 0xACAC

do_pse_power_review_alt(X)

This function evaluates the power allocation or budget of the PSE based on local system changes.

The function returns the following variable:

pse_new_value_alt(X):

The new maximum power value that the PSE expects the PD to draw in units of 0.1 W.

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145.5.3.2.4 Attribute to state diagram variable mapping

Table 145–38 shows the mapping between state diagram variables and Clause 30 attributes for PSEs.

Table 145–38—Attribute to state diagram variable cross reference for PSEs

Attribute	Mapping	State diagram variable
oLldpXdot3LocSystemsGroup Object Class		
aLldpXdot3LocPDRequestedPowerValue	⇐	PDRequestedPowerValueEcho
aLldpXdot3LocPSEAllocatedPowerValue	⇐	PSEAllocatedPowerValue
aLldpXdot3LocReady	⇐	pse_dll_ready
aLldpXdot3LocPSEAutoclassSupport	⇐	PSEAutoclassSupport
aLldpXdot3LocAutoclassCompleted	⇐	PSEAutoclassCompleted
aLldpXdot3LocPDRequestedPowerValueA	⇐	PDRequestedPowerValueEcho_alt(A)
aLldpXdot3LocPDRequestedPowerValueB	⇐	PDRequestedPowerValueEcho_alt(B)
aLldpXdot3LocPSEAllocatedPowerValueA	⇐	PSEAllocatedPowerValue_alt(A)
aLldpXdot3LocPSEAllocatedPowerValueB	⇐	PSEAllocatedPowerValue_alt(B)
oLldpXdot3RemSystemsGroup Object Class		
aLldpXdot3RemPDRequestedPowerValue	⇒	MirroredPDRequestedPowerValue
aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValueEcho
aLldpXdot3RemAutoclassRequest	⇒	MirroredPDAutoclassRequest
aLldpXdot3RemPDRequestedPowerValueA	⇒	MirroredPDRequestedPowerValue_alt(A)
aLldpXdot3RemPDRequestedPowerValueB	⇒	MirroredPDRequestedPowerValue_alt(B)
aLldpXdot3RemPSEAllocatedPowerValueA	⇒	MirroredPSEAllocatedPowerValueEcho_alt(A)
aLldpXdot3RemPSEAllocatedPowerValueB	⇒	MirroredPSEAllocatedPowerValueEcho_alt(B)

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145.5.3.2.5 State diagrams

The general state change procedure for PSEs is shown in Figure 145–40 through Figure 145–43.

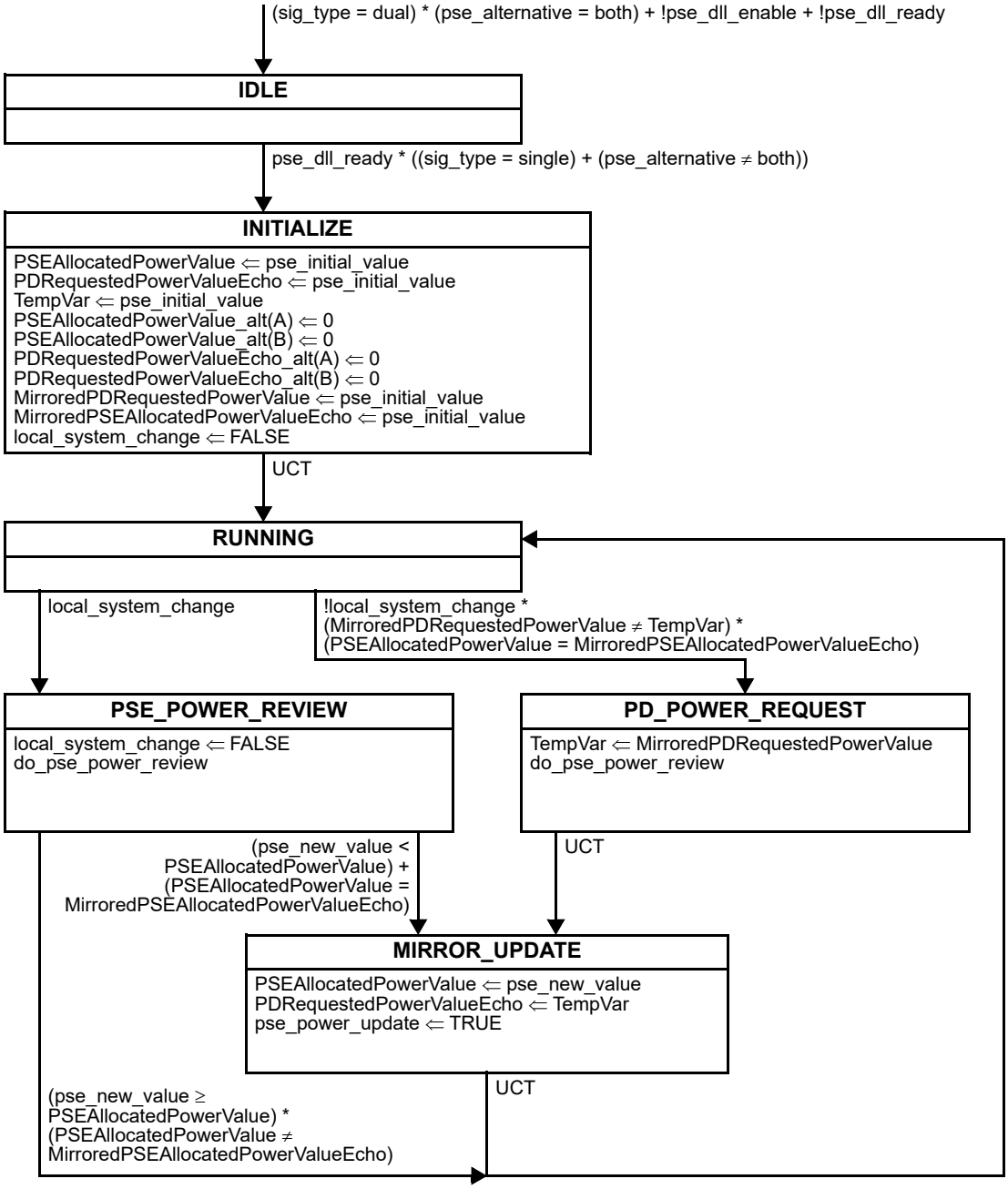

Figure 145–40—PSE power control state diagram for single-signature PDs

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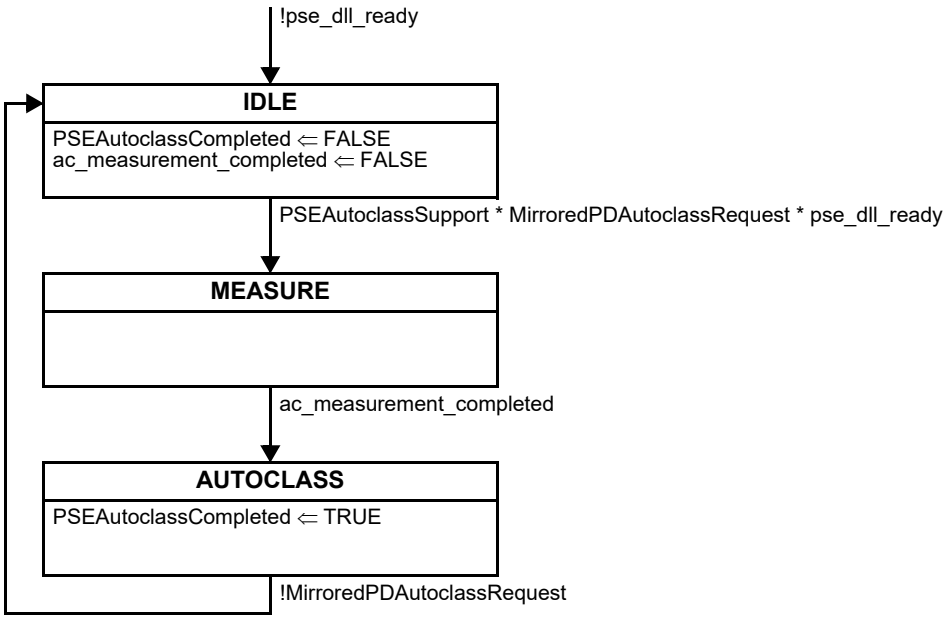

Figure 145–41—PSE DLL Autoclass control state diagram

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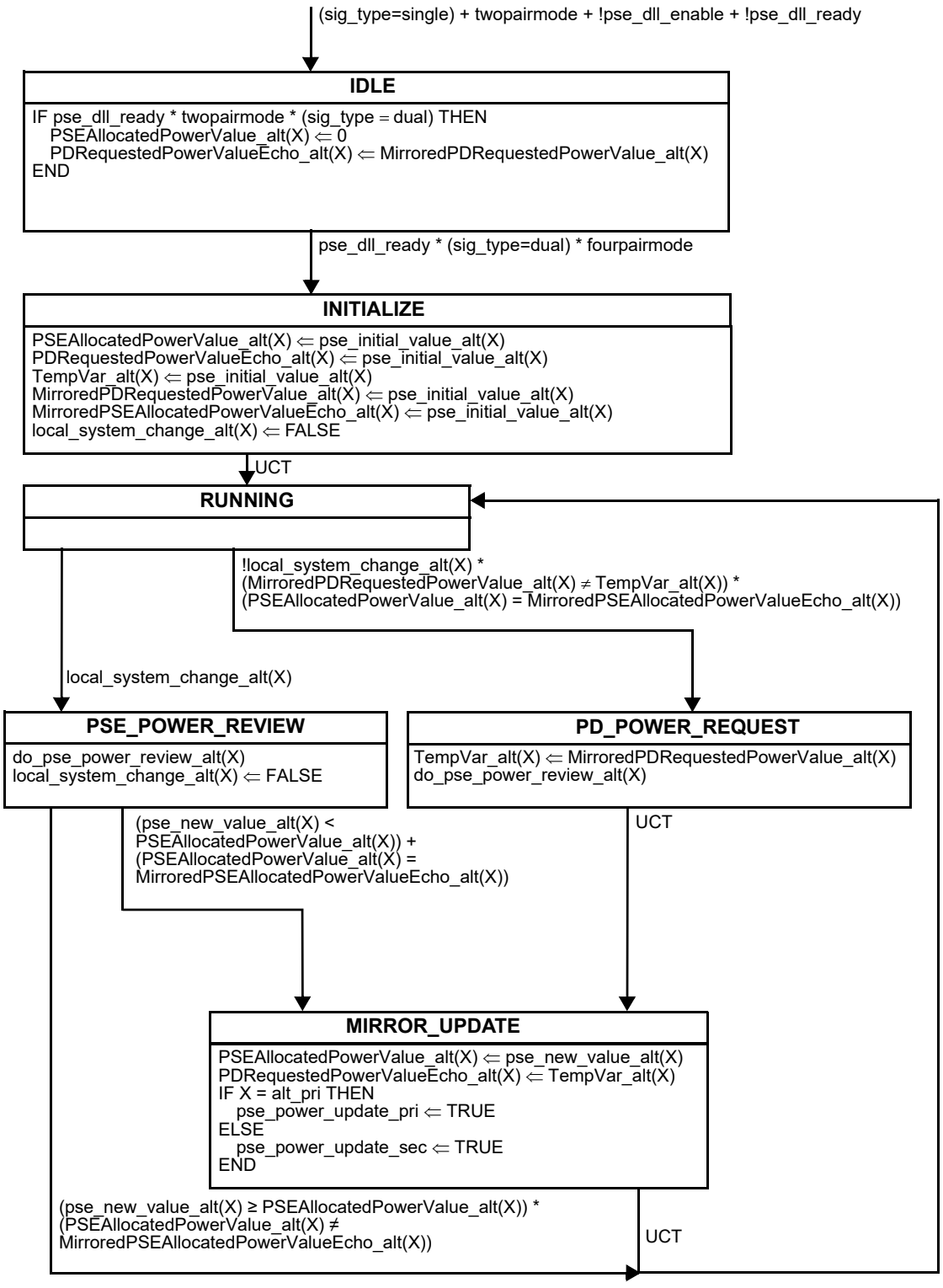

Figure 145–42—PSE power control state diagram for dual-signature PDs in 4-pair mode

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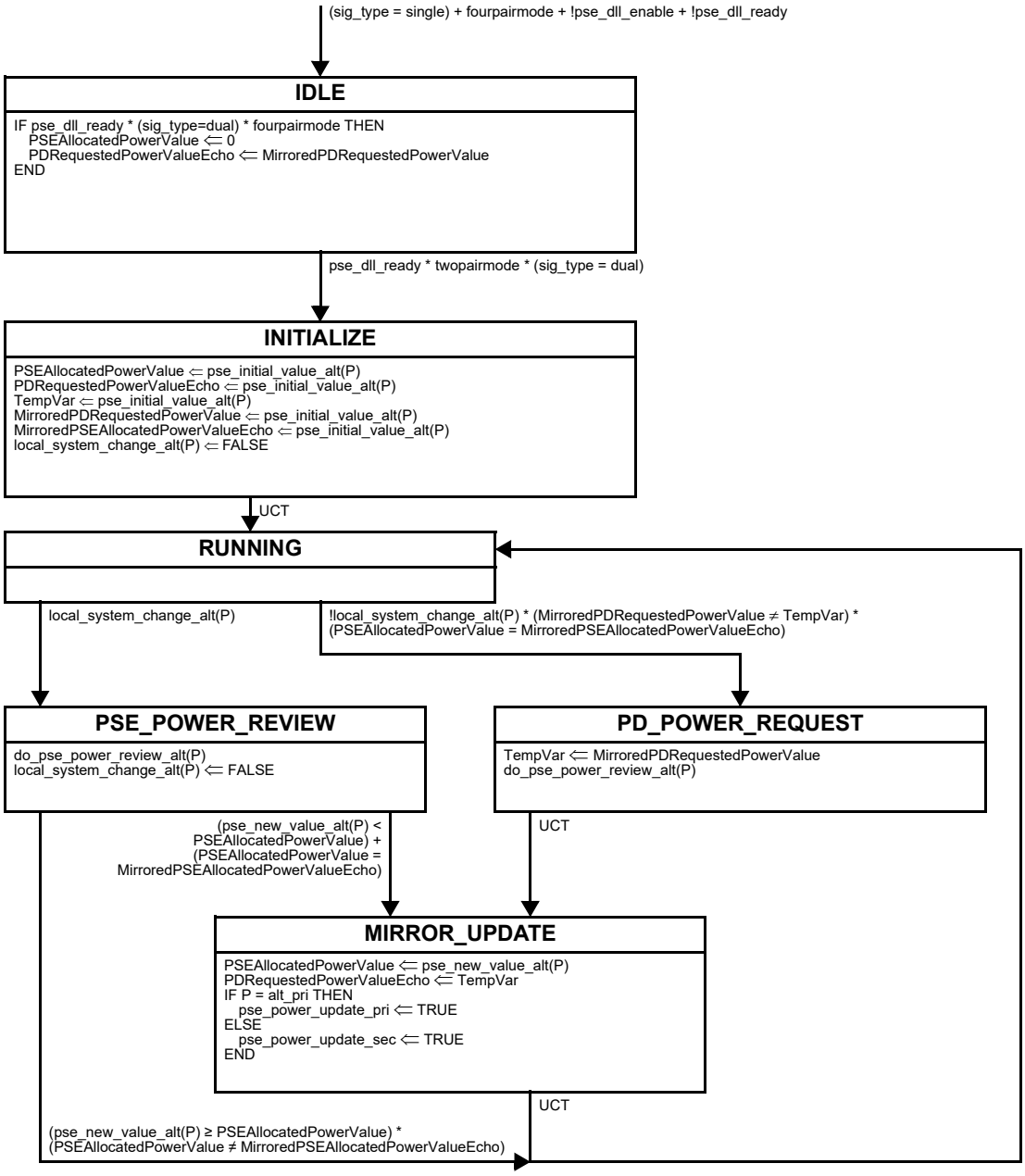

Figure 145–43—PSE power control state diagram for dual-signature PDs in 2-pair mode

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145.5.3.3 Single-signature PD power control state diagrams

This state diagram controls the PDRequestedPowerValue variable, which is used to request power from a PSE, for single-signature PDs.

145.5.3.3.1 Variables

The PD power control state diagram (Figure 145–44 and Figure 145–45) uses the following variables:

MirroredPDRequestedPowerValueEcho
: The copy of the 'PD Requested Power Value' field in the Power Via MDI TLV that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17).
Values: 1 through 999, and 0xACAC

MirroredPSEAllocatedPowerValue
: The copy of the 'PSE Allocated Power Value' field in the Power Via MDI TLV that the PD receives from the remote system in units of 0.1 W. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.20).
Values: 1 through 999, and 0xACAC

MirroredPSEAutoclassCompleted
: The copy of the 'PSE Autoclass completed' field in the Power via MDI TLV that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemAutoclassCompleted (30.12.3.1.34) attribute.
Values:
  FALSE: The PSE has not completed the Autoclass measurement, or it is not performing an Autoclass measurement.
  TRUE: The PSE has completed the Autoclass measurement.

MirroredPSEAutoclassSupport
: The copy of the 'PSE Autoclass support' field in the Power via MDI TLV that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAutoclassSupport (30.12.3.1.33) attribute.
Values:
  FALSE: The PSE does not support Autoclass
  TRUE: The PSE supports Autoclass

PDAutoclassRequest
: A Boolean that indicates if the PD requests Autoclass in the PD. This variable is mapped into aLldpXdot3LocAutoclassRequest (30.12.2.1.35).
Values:
  FALSE: The PD does not request an Autoclass measurement to be performed.
  TRUE: The PD requests an Autoclass measurement to be performed.

PDMaxPowerValue
: Integer that indicates the actual PD power value of the local system in units of 0.1 W. The actual PD power value for a PD is the maximum input average power (see 145.3.8.2) the PD ever draws under the current power allocation. See 145.3.8.2 for values higher than 713.
Values: 1 through 999, and 0xACAC

PDRequestedPowerValue
: Integer that indicates the PD requested power value in the PD in units of 0.1 W. The value is the maximum input average power (see 145.3.8.2) the PD requests. This variable is mapped into the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17). A value higher than 713 requires the PSE to support a power level higher than P_{Class_PD} at the PD PI.
Values: 1 through pd_dllmax_value, and 0xACAC

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PDRequestedPowerValue_mode(X)

Integer that indicates the PD requested power value in the PD in units of 0.1 W. This variable is set to 0 by the single-signature PD power control state diagram. This variable is mapped into the aLldpXdot3LocPDRequestedPowerValueA and aLldpXdot3LocPDRequestedPowerValueB attribute (30.12.2.1.18 and 30.12.2.1.19).

Values: 0

PSEAllocatedPowerValueEcho

This variable is updated by the PD state diagram. This variable maps into the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.20).

Values: 1 through 999, and 0xACAC

PSEAllocatedPowerValueEcho_mode(X)

This variable is updated by the PD state diagram. This variable is set to 0 by the single-signature PD power control state diagram. This variable maps into the aLldpXdot3LocPSEAllocatedPowerValueA and aLldpXdot3LocPSEAllocatedPowerValueB attribute (30.12.2.1.21 and 30.12.2.1.22).

Values: 0

TempVar

A variable used to store Power Value in units of 0.1 W.

Values: 0 through 999, and 0xACAC

dll_4PID

A variable indicating the state of the PD 4PID bit in the ‘Power type/source/priority’ field, as defined in Table 79–7. This variable is assigned through Table 145–39.

Values:

FALSE: The PD does not support powering of both Modes simultaneously.
TRUE: The PD supports powering of both Modes simultaneously.

local_system_change

An implementation-specific variable that indicates that the local system wants to change the allocated power value. In a PD, this indicates it is going to request a new power allocation from the PSE. This value may be set by the PD at any time.

Values:

FALSE: The PD does not want to change the power allocation.
TRUE: The PD wants to change the power allocation.

pd_dllmax_value

This value is derived from pd_req_class (145.3.3.3.2). The value is quantized to fit the available resolution. Additional information on power levels for Class 8 may be found in 145.3.8.2.1. This variable is set per this description.

pd_req_class	pd_dllmax_value
1	39
2	65
3	130
4	255
5	400
6	510
7	620
8	999

pd_dll_enable

A variable output by the PD state diagram (Figure 145–25) to indicate if the PD Data Link Layer classification mechanism is enabled.

Values:

FALSE: PD Data Link Layer classification is not enabled.
TRUE: PD Data Link Layer classification is enabled.

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pd_dll_ready

An implementation-specific variable that indicates that the PD has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.61).

Values:

FALSE: Data Link Layer classification has not completed initialization.
TRUE: Data Link Layer classification has completed initialization.

pd_initial_value

The value of this variable is valid after classification and is derived from the pd_max_power, pd_acs_cancel, and pd_autoclass_enable variables (145.3.3.3.2) used in the Single-signature PD state diagram (Figure 145–25). The value is quantized to fit the available resolution. Additional information on power levels for Class 8 may be found in 145.3.8.2.1. This variable is set per this description.

Values:

pd_max_power	pd_initial_value
1	≤ 39
2	≤ 65
3	≤ 130
4	≤ 255
5	≤ 400
6	≤ 510
7	≤ 620
8	≤ 713
Autoclass	44 204

NOTE—If pd_autoclass_enable is TRUE and pd_acs_cancel is FALSE, then pd_initial_value is set to the value 0xACAC (decimal 44 204).

pd_power_update

A variable that is set when the PDMaxPowerValue in the DLL state diagram in Figure 145–44 has been updated.

Values:

FALSE: The value of PDMaxPowerValue has not changed.
TRUE: The value of PDMaxPowerValue has changed.

trigger_autoclass

A variable used in the PD to trigger a new Autoclass measurement request to the PSE.

Values:

FALSE: The PD does not want to trigger a new Autoclass measurement.
TRUE: The PD wants to trigger a new Autoclass measurement.

A summary cross-references between the Power over Ethernet classification local and remote object class attributes and the PD power control state diagrams, including the direction of the mapping, is provided in Table 145–39.

145.5.3.3.2 Timers

tautoclass_timeout

A timer used to detect the timeout of a pending Autoclass request by the PD. The value of this timer may be set to any value greater than 30 seconds.

145.5.3.3.3 Functions

do_pd_power_review

This function evaluates the power requirements of the PD based on local system changes or changes in the PSE allocated power value. The function returns the following variable:

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pd_new_value:
The new maximum power value that the PD wants to draw in units of 0.1 W.
Valid values: 1 through 999, and 0xACAC

145.5.3.3.4 Attribute to state diagram variable mapping

Table 145–39 shows the mapping between state diagram variables and Clause 30 attributes for single-signature PDs.

Table 145–39—Attribute to state diagram variable cross reference for single-signature PDs

Attribute	Mapping	State diagram variable
oLldpXdot3LocSystemsGroup Object Class		
aLldpXdot3LocPDRequestedPowerValue	⇐	PDRequestedPowerValue
aLldpXdot3LocPSEAllocatedPowerValue	⇐	PSEAllocatedPowerValueEcho
aLldpXdot3LocReady	⇐	pd_dll_ready
aLldpXdot3LocPD4PID	⇐	dll_4PID
aLldpXdot3LocAutoclassRequest	⇐	PDAutoclassRequest
oLldpXdot3RemSystemsGroup Object Class		
aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValue
aLldpXdot3RemPDRequestedPowerValue	⇒	MirroredPDRequestedPowerValueEcho
aLldpXdot3RemPSEAutoclassSupport	⇒	MirroredPSEAutoclassSupport
aLldpXdot3RemAutoclassCompleted	⇒	MirroredPSEAutoclassCompleted

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145.5.3.3.5 State diagrams

The general state change procedure for single-signature PDs is shown in Figure 145–44 and Figure 145–45.

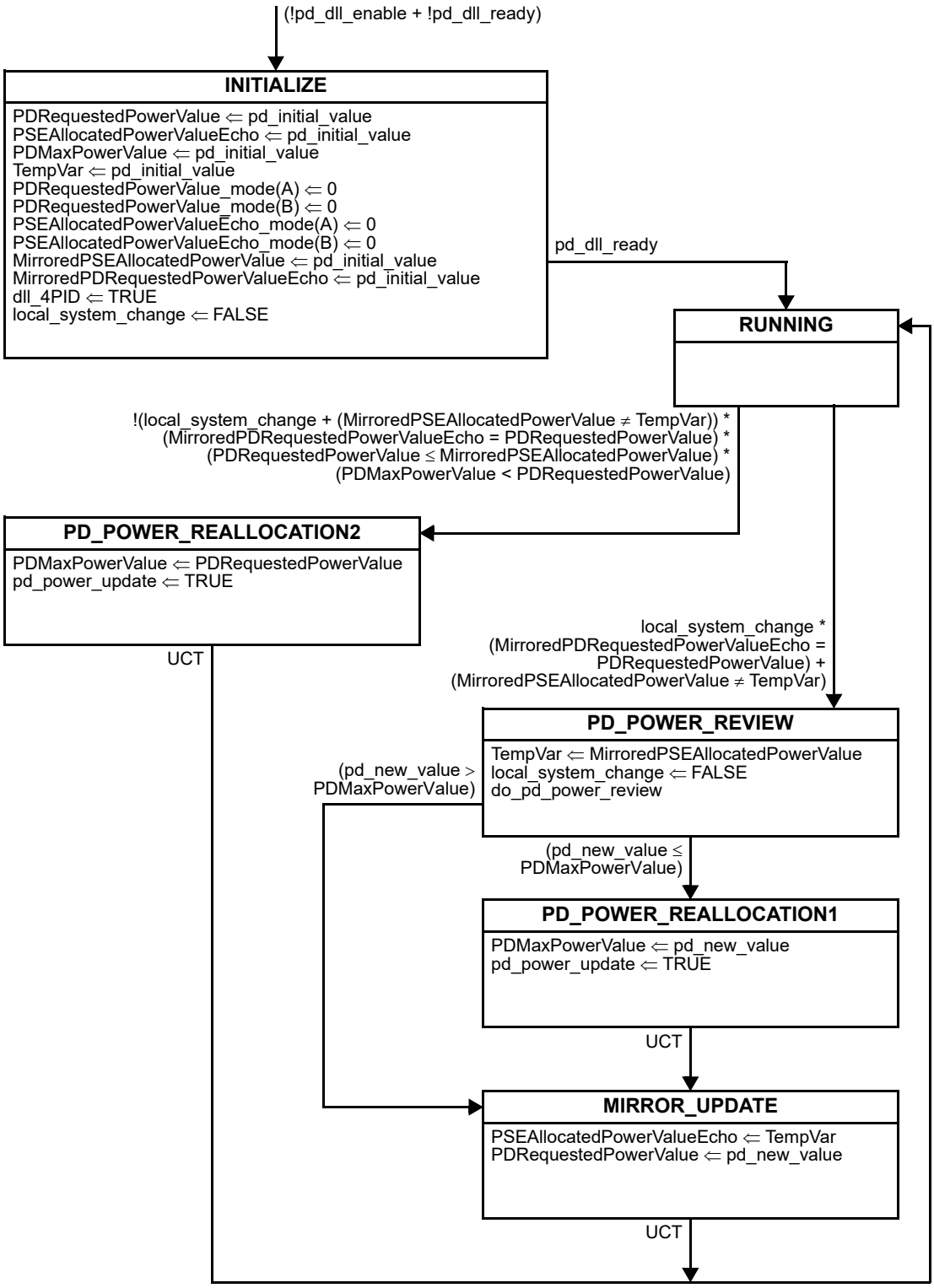

Figure 145–44—Single-signature PD power control state diagram

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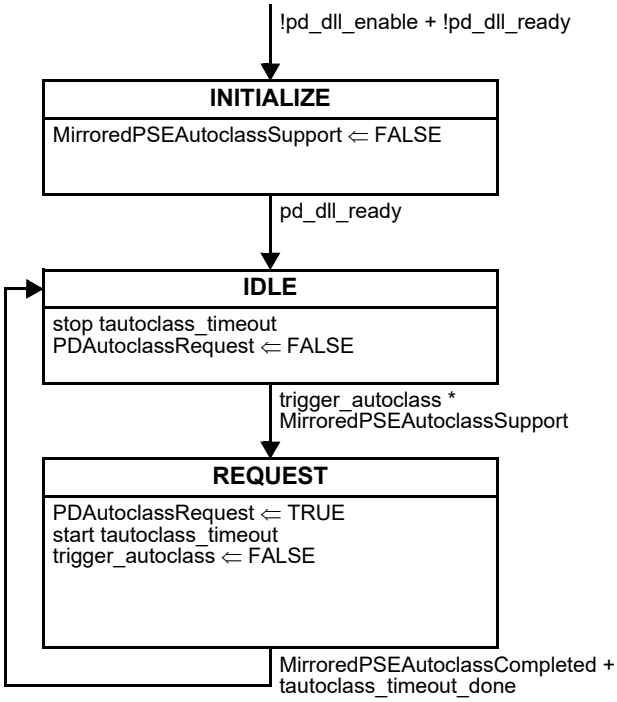

Figure 145–45—PD DLL Autoclass control state diagram

145.5.3.4 Dual-signature PD power control state diagrams

This state diagram controls the PDRequestedPowerValue_mode(X) variables, which are used to allocate power to the individual Modes of a dual-signature PD. It is applicable when the PD is a dual-signature PD that is supplied in 4-pair mode.

145.5.3.4.1 Mode designation

Dual-signature PDs provide the behavior of the state diagram shown in Figure 145–46 over each pairset independently unless otherwise specified. All the parameters that apply to Mode A and Mode B are denoted with the suffix "_mode(X)" where "X" can be "A" or "B", or "_mode(P)" where "P" can be "A" or "B". A parameter that ends with the suffix "_mode(X)" may have different values for Mode A and Mode B.

Dual-signature PDs are implemented on Mode A and Mode B as defined in 145.3.2. Mode information is obtained by replacing the X in the desired variable or function with the letter of the Mode of interest. Modes are referred to in general as follows:

X

Generic Mode designator. When X is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams.
Values:

A: Mode A
B: Mode B

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P

Powered Mode designator. When P is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams. “P” refers to the Mode that is currently powered. Its value is only defined when the PD is powered over 2-pair.

Values:

A: Mode A

B: Mode B

145.5.3.4.2 Variables

The PD power control state diagram (Figure 145–46 and Figure 145–47) use the following variables:

MirroredPDRequestedPowerValueEcho

The copy of the ‘PD Requested Power Value’ field in the Power Via MDI TLV that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17).

Values: 0 through 999

MirroredPDRequestedPowerValueEcho_mode(X)

The copy of the ‘PD Requested Power Value’ field for Mode(X) in the Power Via MDI TLV that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValueA and aLldpXdot3RemPDRequestedPowerValueB attribute (30.12.3.1.18 and 30.12.3.1.19).

Values: 0 through 499

MirroredPSEAllocatedPowerValue

The copy of the ‘PSE Allocated Power Value’ field in the Power Via MDI TLV that the PD receives from the remote system in units of 0.1 W. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.20).

Values: 0 through 999

MirroredPSEAllocatedPowerValue_mode(X)

The copy of the ‘PSE Allocated Power Value’ field for Mode(X) in the Power Via MDI TLV that the PD receives from the remote system in units of 0.1 W. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValueA and aLldpXdot3RemPSEAllocatedPowerValueB attribute (30.12.3.1.21 and 30.12.3.1.22).

Values: 0 through 499

PDMaxPowerValue_mode(X)

Integer that indicates the actual PD power value of the local system in units of 0.1 W. The actual PD power value for a PD is the maximum input average power (see 145.3.8.2) the PD ever draws under the current power allocation.

Values: 1 through 499

PDRequestedPowerValue

Integer that indicates the PD requested power value in the PD in units of 0.1 W. The value is the maximum input average power (see 145.3.8.2) the PD requests. This variable is mapped into the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17). A value higher than 713 requires the PSE to support a power level higher than P_{Class_PD} at the PD PI.

Values: 0 through pd_dllmax_value_mode(P)

PDRequestedPowerValue_mode(X)

Integer that indicates the PD requested power value in the PD in units of 0.1 W. The value is the maximum input average power (see 145.3.8.2) the PD requests. This variable is updated by the PD state diagram. This variable is mapped into the aLldpXdot3LocPDRequestedPowerValueA and aLldpXdot3LocPDRequestedPowerValueB attribute (30.12.2.1.18 and 30.12.2.1.19). A value higher than 356 requires the PSE to support a power level higher than P_{Class_PD} at the PD PI.

Values: 0 through pd_dllmax_value_mode(X)

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PSEAllocatedPowerValueEcho

This variable is updated by the PD state diagram. This variable maps into the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.20).

Values: 0 through 999

PSEAllocatedPowerValueEcho_mode(X)

This variable is updated by the PD state diagram. This variable maps into the aLldpXdot3LocPSEAllocatedPowerValueA and aLldpXdot3LocPSEAllocatedPowerValueB attribute (30.12.2.1.21 and 30.12.2.1.22).

Values: 0 through 499

TempVar

A variable used to store Power Value in units of 0.1 W.

Values: 0 through 999

TempVar_mode(X)

A variable used to store a Power Value in units of 0.1 W.

Values: 0 through 499.

dll_4PID

A variable indicating the state of the PD 4PID bit in the 'Power type/source/priority' field, as defined in Table 79–7. This variable is updated by the PD state diagram. This variable is mapped into the aLldpXdot3LocPD4PID attribute (30.12.2.1.31).

Values:

FALSE: The PD does not support powering of both Modes simultaneously.

TRUE: The PD supports powering of both Modes simultaneously.

fourpairmode

Alias for the following term: (present_mps_mode(A) * present_mps_mode(B))

local_system_change_mode(X)

An implementation-specific variable that indicates that the local system wants to change the allocated power value. This indicates the PD is going to request a new power allocation from the PSE over Mode(X).

Values:

FALSE: The local system does not wants to change the power allocation.

TRUE: The local system wants to change the power allocation.

pd_dllmax_value_mode(X)

This value is derived from pd_req_class_mode(X) (145.3.3.4.1). The value is quantized to fit the available resolution. Additional information on power levels for Class 5 may be found in 145.3.8.2.1. This variable is set per this description.

pd_req_class_mode(X)	pd_dllmax_value_mode(X)
1	39
2	65
3	130
4	255
5	356

pd_dll_enable

A variable output by the PD state diagram (Figure 145–25) to indicate if the PD Data Link Layer classification mechanism is enabled.

Values:

FALSE: PD Data Link Layer classification is not enabled.

TRUE: PD Data Link Layer classification is enabled.

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pd_dll_ready

An implementation-specific variable that indicates that the PD has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReadyattribute (30.12.2.1.61).

Values:

FALSE: Data Link Layer classification has not completed initialization.

TRUE: Data Link Layer classification has completed initialization.

pd_initial_value_mode(X)

The value of this variable is valid after classification and is derived from the pd_max_power_mode(X) (145.3.3.4.2) variable used in the PD state diagrams; defined in Figure 145–27. The value is quantized to fit the available resolution. Additional information on power levels for Class 5 may be found in 145.3.8.2.1.

Values:

pd_max_power_mode(X)	pd_initial_value_mode(X)
1	≤ 39
2	≤ 65
3	≤ 130
4	≤ 255
5	≤ 356

pd_power_update_mode(X)

A variable that is set when the PDMaxPowerValue_mode(X) has been updated.

Values:

FALSE: The value of PDMaxPowerValue_mode(X) has not changed.

TRUE: The value of PDMaxPowerValue_mode(X) has changed.

pd_requested_value_mode(X)

The value of this variable is used by the dual-signature PD to indicate the amount of power it requires on Mode A and Mode B, while it is being powered in 2-pair mode.

Values: 1 through 499

twopairmode

Alias for the following term: (present_mps_mode(A) ^ present_mps_mode(B))

145.5.3.4.3 Functions

do_pd_power_review_mode(X)

This function evaluates the power requirements of the PD based on local system changes or changes in the PSE allocated power value.

The function returns the following variable:

pd_new_value_mode(X):

The new maximum power value that the PD wants to draw in units of 0.1 W.

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145.5.3.4.4 Attribute to state diagram variable mapping

Table 145–40 shows the mapping between state diagram variables and Clause 30 attributes for dual-signature PDs.

Table 145–40—Attribute to state diagram variable cross reference for dual-signature PDs

Attribute	Mapping	State diagram variable
oLldpXdot3LocSystemsGroup Object Class		
aLldpXdot3LocReady	⇐	pd_dll_ready
aLldpXdot3LocPD4PID	⇐	dll_4PID
aLldpXdot3LocPDRequestedPowerValue	⇐	PDRequestedPowerValue
aLldpXdot3LocPDRequestedPowerValueA	⇐	PDRequestedPowerValue_mode(A)
aLldpXdot3LocPDRequestedPowerValueB	⇐	PDRequestedPowerValue_mode(B)
aLldpXdot3LocPSEAllocatedPowerValue	⇐	PSEAllocatedPowerValueEcho
aLldpXdot3LocPSEAllocatedPowerValueA	⇐	PSEAllocatedPowerValueEcho_mode(A)
aLldpXdot3LocPSEAllocatedPowerValueB	⇐	PSEAllocatedPowerValueEcho_mode(B)
oLldpXdot3RemSystemsGroup Object Class		
aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValue
aLldpXdot3RemPSEAllocatedPowerValueA	⇒	MirroredPSEAllocatedPowerValue_mode(A)
aLldpXdot3RemPSEAllocatedPowerValueB	⇒	MirroredPSEAllocatedPowerValue_mode(B)
aLldpXdot3RemPDRequestedPowerValue	⇒	MirroredPDRequestedPowerValueEcho
aLldpXdot3RemPDRequestedPowerValueA	⇒	MirroredPDRequestedPowerValueEcho_mode(A)
aLldpXdot3RemPDRequestedPowerValueB	⇒	MirroredPDRequestedPowerValueEcho_mode(B)

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145.5.3.4.5 State diagrams

The general state change procedure for PDs is shown in Figure 145–46 and Figure 145–47.

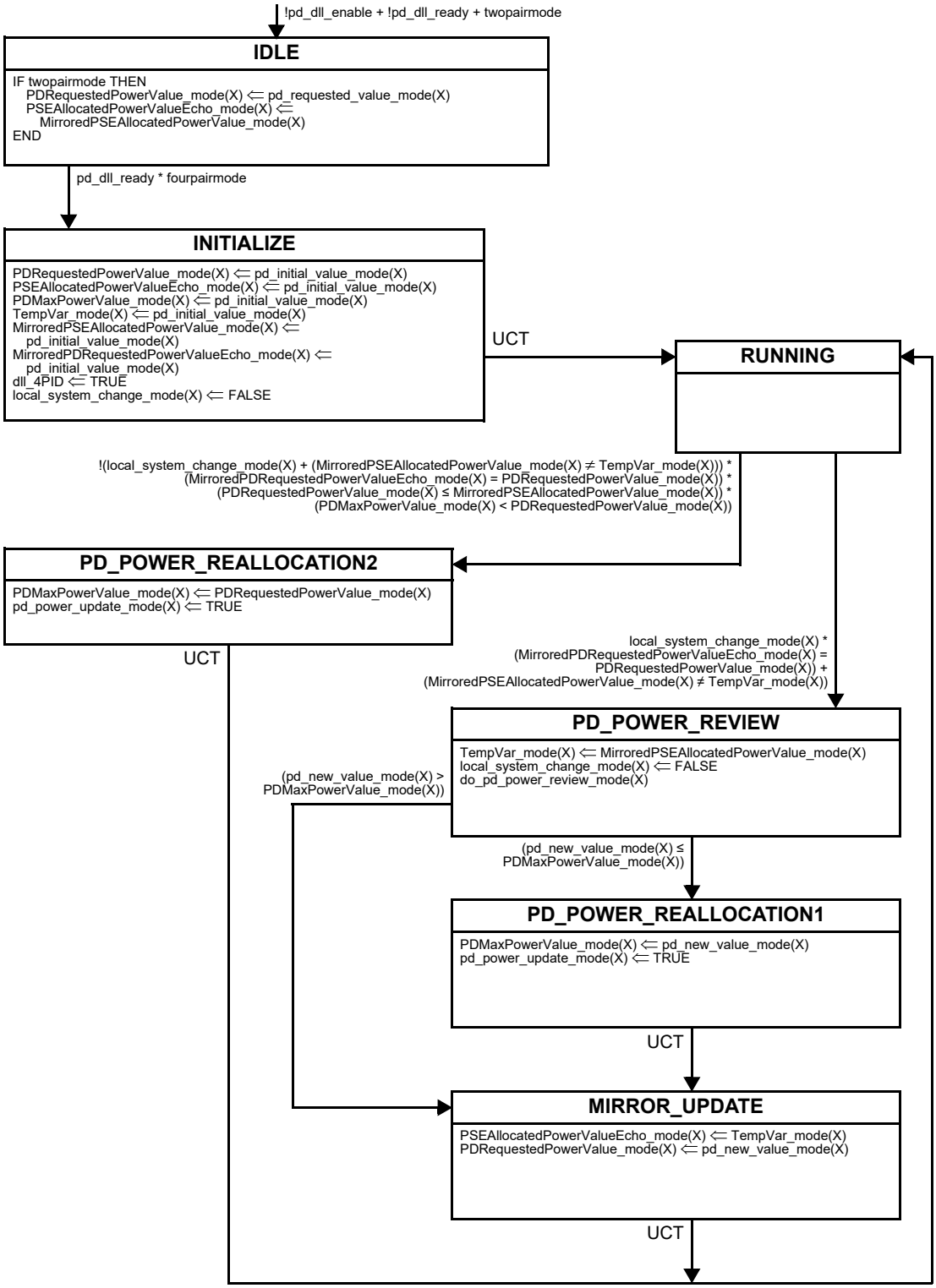

Figure 145–46—Dual-signature PD power control state diagram in 4-pair mode

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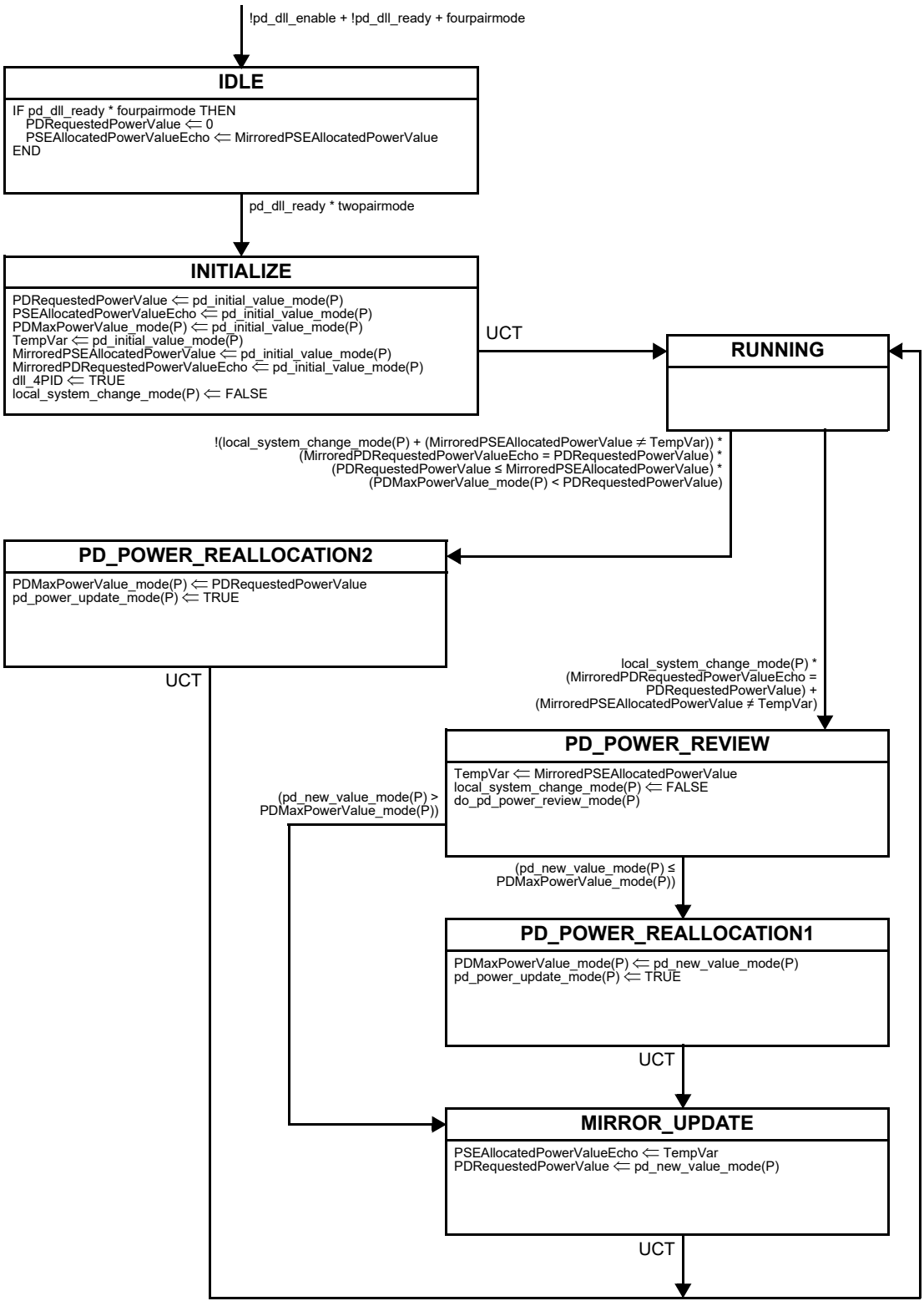

Figure 145–47—Dual-signature PD power control state diagram in 2-pair mode

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145.5.4 Power requests and allocations

The variables PDRequestedPowerValue and PDRequestedPowerValue_mode(X) allow a PD to request an amount of power from the PSE. The variables PSEAllocatedPowerValue and PSEAllocatedPowerValue_alt(X) allow the PSE to allocate an amount of power to the PD.

PSEs shall use values in the range defined in Table 145–41 for PSEAllocatedPowerValue and PSEAllocatedPowerValue_alt(X) where X can be A or B. PDs shall use the values in the range defined in Table 145–42 for PDRequestedPowerValue and PDRequestedPowerValue_mode(X) where X can be A or B.

Table 145–41—Permitted values for PSEAllocatedPowerValue and PSEAllocatedPowerValue_alt(X)

Powering mode	PD configuration	PSEAllocatedPowerValue	PSEAllocatedPowerValue_alt(X)
2-pair	—	1 to 255[a]	0
4-pair	single-signature	1 to 999	0
	dual-signature	0	1 to 499

[a] A PSE that has encountered a fault that requires to operate in 2-pair mode, may use values 1 to 499 for this variable.

Table 145–42—Permitted values for PDRequestedPowerValue and PDRequestedPowerValue_mode(X)

Powering mode	PD configuration	PDRequestedPowerValue	PDRequestedPowerValue_mode(X)
—	single-signature	1 to 999	0
2-pair	dual-signature	1 to 255[a]	1 to 499
4-pair		0	1 to 499

[a] A PD that has encountered a fault that requires to operate in 2-pair mode, may use values 1 to 499 for this variable.

Power requests and allocations greater than 713 (for single-signature PDs) or greater than 356 (for dual-signature PDs) are only used after the PSE and PD are in sync using the initial values that are assigned in INITIALIZE, as defined in Figure 145–40 through Figure 145–47.

145.5.5 State change procedure across a link (single-signature)

The PSE and PD utilize the LLDPDUs to advertise their various attributes to the other entity.

The PD may request a new power value through the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE responds to the PD's request through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.20) attribute in the oLldpXdot3LocSystemsGroup object class. The PSE also copies the value of the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) in the oLldpXdot3RemSystemsGroup object class to the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) in the oLldpXdot3LocSystemsGroup object

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class. This appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.20) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE may allocate a new power value through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.20) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.20) attribute in the oLldpXdot3RemSystemsGroup object class. The PD responds to a PSE's request through the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The PD also copies the value of the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.20) attribute in the oLldpXdot3RemSystemsGroup object class to the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.20) attribute in the oLldpXdot3LocSystemsGroup object class. This appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup object class.

The state diagrams in Figure 145–40 and Figure 145–44 describe the behavior above.

145.5.5.1 PSE state change procedure across a link (single-signature)

A PSE is considered to be in sync with the PD when the value of PSEAllocatedPowerValue matches the value of MirroredPSEAllocatedPowerValueEcho.

During normal operation, the PSE is in RUNNING. If the PSE wants to initiate a change in the PD allocation, the local_system_change is asserted and the PSE enters PSE_POWER_REVIEW, where a new power allocation value, pse_new_value, is computed. If the PSE is in sync with the PD or if pse_new_value is smaller than PSEAllocatedPowerValue, it enters MIRROR_UPDATE where pse_new_value is assigned to PSEAllocatedPowerValue. It also updates PDRequestedPowerValueEcho and returns to RUNNING.

If the PSE's previously stored MirroredPDRequestedPowerValue changes, a request by the PD to change its power allocation is recognized. It entertains this request only when it is in sync with the PD. The PSE examines the request by entering PD_POWER_REQUEST. A new power allocation value, pse_new_value, is computed. It then enters MIRROR_UPDATE where pse_new_value is assigned to PSEAllocatedPowerValue. It also updates PDRequestedPowerValueEcho and returns to RUNNING.

145.5.5.2 PD state change procedure across a link (single-signature)

A PD is considered to be in sync with the PSE when the value of PDRequestedPowerValue matches the value of MirroredPDRequestedPowerValueEcho. The PD is not allowed to change its maximum power draw or the requested power value when it is not in sync with the PSE.

During normal operation, the PD is in RUNNING. If the PD's previously stored MirroredPSEAllocatedPowerValue is changed or local_system_change is asserted by the PD so as to change its power allocation, the PD enters PD_POWER_REVIEW. In this state, the PD evaluates the change and generates an updated power value called pd_new_value. If pd_new_value is less than PDMaxPowerValue, it updates PDMaxPowerValue in PD_POWER_REALLOCATION1. The PD then finally enters MIRROR_UPDATE where pd_new_value is assigned to PDRequestedPowerValue. It also updates PSEAllocatedPowerValueEcho and returns to RUNNING.

In the above flow, if pd_new_value is greater than PDMaxPowerValue, the PD waits until it is in sync with the PSE and the PSE grants the higher power value. When this condition arises, the PD enters PD_POWER_REALLOCATION2. In this state, the PD assigns PDMaxPowerValue to PDRequestedPowerValue and returns to RUNNING.

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145.5.6 State change procedure across a link (dual-signature)

The PSE and PD use the LLDP protocol (see Clause 79) to advertise their various attributes to the other entity.

The PD may request a new power value through the aLldpXdot3LocPDRequestedPowerValueA and aLldpXdot3LocPDRequestedPowerValueB (30.12.2.1.18 and 30.12.2.1.19) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValueA and aLldpXdot3RemPDRequestedPowerValueB (30.12.3.1.18 and 30.12.3.1.19) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE responds to the PD's request through the aLldpXdot3LocPSEAllocatedPowerValueA and aLldpXdot3LocPSEAllocatedPowerValueB (30.12.2.1.21 and 30.12.2.1.22) attribute in the oLldpXdot3LocSystemsGroup object class. The PSE also copies the value of the aLldpXdot3RemPDRequestedPowerValueA and aLldpXdot3RemPDRequestedPowerValueB (30.12.3.1.18 and 30.12.3.1.19) in the oLldpXdot3RemSystemsGroup object class to the aLldpXdot3LocPDRequestedPowerValueA and aLldpXdot3LocPDRequestedPowerValueB (30.12.2.1.18 and 30.12.2.1.19) in the oLldpXdot3LocSystemsGroup object class. This appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValueA and aLldpXdot3RemPSEAllocatedPowerValueB (30.12.3.1.21 and 30.12.3.1.22) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE may allocate a new power value through the aLldpXdot3LocPSEAllocatedPowerValueA and aLldpXdot3LocPSEAllocatedPowerValueB (30.12.2.1.18 and 30.12.2.1.19) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValueA and aLldpXdot3RemPSEAllocatedPowerValueB (30.12.3.1.21 and 30.12.3.1.22) attribute in the oLldpXdot3RemSystemsGroup object class. The PD responds to a PSE's request through the aLldpXdot3LocPDRequestedPowerValueA and aLldpXdot3LocPDRequestedPowerValueB (30.12.2.1.18 and 30.12.2.1.19) attribute in the oLldpXdot3LocSystemsGroup object class. The PD also copies the value of the aLldpXdot3RemPSEAllocatedPowerValueA and aLldpXdot3RemPSEAllocatedPowerValueB (30.12.3.1.21 and 30.12.3.1.22) attribute in the oLldpXdot3RemSystemsGroup object class to the aLldpXdot3LocPSEAllocatedPowerValueA and aLldpXdot3LocPSEAllocatedPowerValueB (30.12.2.1.18 and 30.12.2.1.19) attribute in the oLldpXdot3LocSystemsGroup object class. This appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValueA and aLldpXdot3RemPDRequestedPowerValueB (30.12.3.1.18 and 30.12.3.1.19) attribute in the oLldpXdot3RemSystemsGroup object class.

The state diagrams in Figure 145–40, Figure 145–42, Figure 145–43, Figure 145–46, and Figure 145–47 describe the behavior above.

145.5.6.1 Transitions between 2-pair and 4-pair mode (dual-signature)

When a PSE, connected to a dual-signature PD, transitions from 4-pair to 2-pair operation, it shall assign the value of PSEAllocatedPowerValue_alt(X), where X is the powered Alternative, to PSEAllocatedPowerValue. The purpose of this is that the PD can continue operating over the remaining powered Mode.

When a PSE, connected to a dual-signature PD, transitions from 2-pair to 4-pair operation, it shall assign the value of PSEAllocatedPowerValue to PSEAllocatedPowerValue_alt(X), where X is the Alternative that was initially powered.

A dual-signature PD that is switched from 4-pair to 2-pair mode requests the amount of power it needs for 2-pair operation in the PDRequestedPowerValue variable. Per Table 145–42 this is the requested power for the powered Mode.

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145.5.6.2 PSE state change procedure across a link (dual-signature)

A PSE is considered to be in sync with the PD when the value of PSEAllocatedPowerValue_alt(X) matches the value of MirroredPSEAllocatedPowerValueEcho_alt(X).

During normal operation, the PSE is in RUNNING. If the PSE wants to initiate a change in the PD allocation, the local_system_change_alt(X) is asserted and the PSE enters PSE_POWER_REVIEW, where a new power allocation value, pse_new_value_alt(X), is computed. If the PSE is in sync with the PD or if pse_new_value_alt(X) is smaller than PSEAllocatedPowerValue_alt(X), it enters MIRROR_UPDATE where pse_new_value_alt(X) is assigned to PSEAllocatedPowerValue_alt(X). It also updates PDRequestedPowerValueEcho_alt(X) and returns to RUNNING.

If the PSE's previously stored MirroredPDRequestedPowerValue_alt(X) changes, a request by the PD to change its power allocation is recognized. It entertains this request only when it is in sync with the PD. The PSE examines the request by entering PD_POWER_REQUEST. A new power allocation value, pse_new_value_alt(X), is computed. It then enters MIRROR_UPDATE where pse_new_value_alt(X) is assigned to PSEAllocatedPowerValue_alt(X). It also updates PDRequestedPowerValueEcho_alt(X) and returns to RUNNING.

145.5.6.3 PD state change procedure across a link (dual-signature)

A PD is considered to be in sync with the PSE when the value of PDRequestedPowerValue_mode(X) matches the value of MirroredPDRequestedPowerValueEcho_mode(X). The PD is not allowed to change its maximum power draw or the requested power value when it is not in sync with the PSE.

During normal operation, the PD is in RUNNING. If the PD's previously stored MirroredPSEAllocatedPowerValue_mode(X) is changed or local_system_change_mode(X) is asserted by the PD so as to change its power allocation, the PD enters PD_POWER_REVIEW. In this state, the PD evaluates the change and generates an updated power value called pd_new_value_mode(X). If pd_new_value_mode(X) is less than PDMaxPowerValue_mode(X), it updates PDMaxPowerValue_mode(X) in PD_POWER_REALLOCATION1. The PD finally enters MIRROR_UPDATE where pd_new_value_mode(X) is assigned to PDRequestedPower-Value_mode(X). It also updates PSEAllocatedPowerValueEcho_mode(X) and returns to RUNNING.

In the above flow, if pd_new_value_mode(X) is greater than PDMaxPowerValue_mode(X), the PD waits until it is in sync with the PSE and the PSE grants the higher power value. When this condition arises, the PD enters PD_POWER_REALLOCATION2. In this state, the PD assigns PDMaxPowerValue_mode(X) to PDRequestedPowerValue_mode(X) and returns to RUNNING.

145.5.7 Autoclass

A PSE can indicate it supports DLL Autoclass by means of the aLldpXdot3LocPSEAutoclassSupport (30.12.2.1.33) attribute in the oLldpXdot3LocSystemsGroup object class. This property appears to the PD as a change to aLldpXdot3RemPSEAutoclassSupport (30.12.3.1.33) attribute in the oLldpXdot3RemSystemsGroup object class.

A PD connected to a PSE that supports Autoclass can initiate an Autoclass request, to optimize the allocated power budget, through the aLldpXdot3LocAutoclassRequest (30.12.2.1.35) attribute in the oLldpXdot3LocSystemsGroup object class. This request will appear to the PSE as a change in the aLldpXdot3RemAutoclassRequest (30.12.3.1.35) attribute in the oLldpXdot3RemSystemsGroup object class. When the PD sends this request, it needs to be in a state where it consumes the amount of power that, from that moment onward, will be the maximum power drawn.

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When the PSE receives the request for Autoclass, and Autoclass is enabled, it shall measure the power consumption per the requirements in 145.2.8.2. After this measurement has been completed, the PSE may update the PSEAllocatedPowerValue and follow the procedure in 145.5.5.1. The PSE also communicates the completion of the Autoclass procedure by means of the aLldpXdot3LocAutoclassCompleted (30.12.2.1.34) attribute in the oLldpXdot3LocSystemsGroup object class. This will appear to the PD as a change in the aLldpXdot3RemAutoclassCompleted (30.12.3.1.34) attribute in the oLldpXdot3LocSystemsGroup object class.

A PD that receives the indication that Autoclass is completed through the MirroredPSEAutoclassCompleted then resets the PDAutoclassRequest variable, thereby completing the procedure.

145.6 Environmental

145.6.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2. In particular, the PSE shall be classified as a Limited Power Source in accordance with Annex Q of IEC 62368-1:2018, as applicable.

Equipment shall comply with all applicable local and national codes related to safety.

145.6.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns. The list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to verify compliance with the appropriate requirements. LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards should be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures should be taken to verify that the intended safety features are not negated during installation of a new network or during modification of an existing network.

145.6.3 Installation and maintenance guidelines

It is a mandatory requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable. In particular, users are cautioned to be aware of the ampacity of cabling, as installed, and local codes and regulations, e.g., the National Electrical Code® (NEC®) (NFPA 70®, 2017 Edition) [B56], relevant to the maximum class supported.

It is a mandatory requirement that, during installation of the cabling plant, care be taken to verify that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

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145.6.4 Patch panel considerations

It is possible that the current carrying capability of a cabling cross-connect may be exceeded by a PSE. The designer should consult the manufacturers' specifications to verify compliance with the appropriate requirements.

145.6.5 Electromagnetic emissions

The PD and PSE powered cabling link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

145.6.6 Temperature and humidity

The PD and PSE powered cabling link segment is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling. Specific requirements and values for these parameters are beyond the scope of this standard.

145.6.7 Labeling

It is recommended that the PSE or PD (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Power classification and power level in terms of maximum current drain over the operating voltage range, 36 V to 57 V, applies for PD only
b) Port type (e.g., 100BASE-TX, TIA Category, or ISO Class)
c) Any applicable safety warnings
d) "PSE" or "PD" as appropriate
e) Indicate "single-signature PD" or "dual-signature PD" as appropriate.
f) Type (e.g., "Type 3" or "Type 4")

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145.7 Protocol implementation conformance statement (PICS) proforma for Clause 145, Power over Ethernet[241]

145.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 145, Power over Ethernet, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

145.7.2 Identification

145.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

145.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 145, Power over Ethernet
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[241] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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145.7.2.3 PD Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PDT3	Type 3 PD implementation	145.3.1	PD is Type 3	O	Yes [ ] No [ ]
*PDT3L	Type 3 PD implementation	145.3.1	PD is Type 3 and requests Class 1, Class 2, or Class 3	O	Yes [ ] No [ ]
*PDT3H	Type 3 PD implementation	145.3.1	PD is Type 3 and requests Class 4, Class 5, or Class 6	O	Yes [ ] No [ ]
*PDT4	Type 4 PD implementation	145.3.1	PD is Type 4	O	Yes [ ] No [ ]
*PDSS	Single-signature PD	145.3.1	PD is single-signature	O	Yes [ ] No [ ]
*PDDS	Dual-signature PD	145.3.1	PD is dual-signature	O	Yes [ ] No [ ]
*PDAC	Autoclass implementation	145.3.6.2	PD supports Autoclass	O	Yes [ ] No [ ]
*WEXP	Implementation supports exceeding P_{Class_PD}	145.3.8.2.1, 145.3.8.4.1	PD supports behavior described in 145.3.8.2.1 and 145.3.8.4.1	PDT4:O	Yes [ ] No [ ]
*PDRP	PD required power	145.3.9	Show valid MPS when power is required	O	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	145.5	PD supports Data Link Layer classification	PDT3L:O PDT3H:M PDT4:M	Yes [ ] No [ ]

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145.7.2.4 PSE Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PSET3	Type 3 PSE implementation	145.2.1	PSE is a Type 3 PSE	O	Yes [ ] No [ ]
*PSET3L	Type 3 PSE implementation	145.2.1	Type 3 PSE that supports up to Class 4 power	O	Yes [ ] No [ ]
*PSET4H	Type 3 PSE implementation	145.2.1	Type 3 PSE that support more than Class 4 power	O	Yes [ ] No [ ]
*PSET4	Type 4 PSE implementation	145.2.1	PSE is a Type 4 PSE	O	Yes [ ] No [ ]
*PSE4P	4-pair capability	145.2.1	PSE supports powering over 4 pairs	PSET3L:O PSET3H:M PSET4:M	Yes [ ] No [ ]
*MID	Midspan PSE	145.2.3	PSE implemented as a midspan device	O/1	Yes [ ] No [ ]
*MIDA	Alternative A Midspan PSE	145.2.3	Midspan PSE implements Alternative A	MID:O	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	145.5	PSE supports Data Link Layer classification	O	Yes [ ] No [ ]
*PSEAC	Autoclass implementation	145.2.8.2	PSE implements Autoclass	O	Yes [ ] No [ ]

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145.7.3 PICS proforma tables for Power over Ethernet

145.7.3.1 Power sourcing equipment

Item	Feature	Subclause	Value/Comment	Status	Support
PSE1	PSE polarity configurations	145.2.4	As defined in Table 145–4	M	Yes [ ]
PSE2	Alternative implementation	145.2.4	Implement Alternative A, Alternative B, or both	PSET3L:M	Yes [ ] N/A [ ]
PSE3	Alternative implementation	145.2.4	Implement Alternative A and Alternative B	PSET3H:M PSET4:M	Yes [ ] N/A [ ]
PSE4	PSE behavior (state diagrams)	145.2.5	Per Figure 145–13 to Figure 145–18	M	Yes [ ]
PSE5	PSE performing detection only on Alternative B fails to detect a valid PD detection signature	145.2.5.1	Shall not apply a voltage greater than V_{Off} for at least T_{dbo} as defined in Table 145–16	M	Yes [ ]
PSE6	Alternative roles establishment	145.2.5.1	Established in IDLE and maintained in every other state	M	Yes [ ]
PSE7	Set pse_avail_pwr, pse_avail_pwr_pri, and pse_avail_pwr_sec	145.2.5.4	Set from the range described in Table 145–6	M	Yes [ ]
PSE8	Applying operating voltage to a pairset	145.2.6	Not until a valid signature has been detected on that pairset	M	Yes [ ]
PSE9	Detecting PDs	145.2.6.1	Performed by probing the PSE PI	M	Yes [ ]
PSE10	PSE detection signature	145.2.6.1	Invalid as defined in Table 145–22	M	Yes [ ]
PSE11	Open circuit voltage and short circuit current	145.2.6.1	Meet specifications in Table 145–7	M	Yes [ ]
PSE12	Backdriven current	145.2.6.1	Not be damaged by up to 5 mA over the range of V_{oc}	M	Yes [ ]
PSE13	Output capacitance	145.2.6.1	C_{out} in Table 145–7	M	Yes [ ]
PSE14	Detection voltage with a valid PD signature connected	145.2.6.2	Meets V_{valid} in Table 145–7	M	Yes [ ]
PSE15	Detection voltage measurements	145.2.6.2	At least two measurements that create at least ΔV_{test} difference	M	Yes [ ]
PSE16	Control slew rate when switching detection voltages	145.2.6.2	Less than V_{slew} as defined in Table 145–7	M	Yes [ ]
PSE17	Accept as a valid signature	145.2.6.3	A pairset with all of the characteristics specified in Table 145–8	M	Yes [ ]
PSE18	Reject as an invalid signature	145.2.6.4	A pairset which exhibits any of characteristics as defined in Table 145–9	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE19	Connection check	145.2.7	Complete connection check prior to the classification of a PD	PSE4P:M	Yes [ ] N/A [ ]
PSE20	Open circuit voltage and short circuit voltage during connection check	145.2.7	Meet the specifications in Table 145–7	PSE4P:M	Yes [ ] N/A [ ]
PSE21	Connection check voltage when a single- or dual-signature PD is connected	145.2.7	Within the V_{valid} range as defined in Table 145–7	PSE4P:M	Yes [ ] N/A [ ]
PSE22	Voltage on either pairset rises above V_{valid} max during connection check	145.2.7	Reset the PD	PSE4P:M	Yes [ ] N/A [ ]
PSE23	Channel resistance considerations for $P_{Autoclass}$	145.2.8	Increase $P_{Autoclass}$ by at least P_{ac_margin}	PSEAC:M	Yes [ ] N/A [ ]
PSE24	Minimum supported output power if $P_{Autoclass}$ is less than or equal to 4 W	145.2.8	Output power is P_{Class}	M	Yes [ ]
PSE25	Power allocation after a fault	145.2.8	Revert to Class 4 power	PSE4P:M	Yes [ ] N/A [ ]
PSE26	Autoclass measurement and 2-pair/4-pair power	145.2.8	Increase the power allocation by at least P_{ac_extra}	PSEAC:M	Yes [ ] N/A [ ]
PSE27	Perform Multiple-Event Physical Layer classification	145.2.8	Subsequent after detection	M	Yes [ ]
PSE28	Dual-signature classification	145.2.8	Perform Physical Layer classification on each pairset	PSE4P:M	Yes [ ] N/A [ ]
PSE29	Support Multiple-Event Physical Layer Classification	145.2.8	Can assign the highest supported Class through Physical Layer Classification	M	Yes [ ]
PSE30	Failure to complete classification (single-signature)	145.2.8	Return to IDLE	M	Yes [ ]
PSE31	Failure to complete classification (dual-signature)	145.2.8	Return to IDLE corresponding to the appropriate Alternative	M	Yes [ ]
PSE32	Type 3 PSE class and mark event limit (single-signature)	145.2.8.1	As defined in 145.2.8.1	PSET3:M	Yes [ ] N/A [ ]
PSE33	Type 3 PSE class and mark event limit (dual-signature)	145.2.8.1	As defined in 145.2.8.1	PSET3:M	Yes [ ] N/A [ ]
PSE34	Type 4 PSE class and mark event limit (single-signature)	145.2.8.1	As defined in 145.2.8.1	PSET4:M	Yes [ ] N/A [ ]
PSE35	Type 4 PSE class and mark event limit (dual-signature)	145.2.8.1	As defined in 145.2.8.1	PSET4:M	Yes [ ] N/A [ ]
PSE36	Maximum class events based on available power and requested Class (single-signature)	145.2.8.1	As defined in 145.2.8.1	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE37	Maximum class events based on available power and requested Class (dual-signature)	145.2.8.1	As defined in 145.2.8.1	M	Yes [ ]
PSE38	Long class event voltage/timing	145.2.8.1	Per V_{Class} and T_{LCE}	M	Yes [ ]
PSE39	Measure I_{Class} in CLASS_EV1_AUTO	145.2.8.1	After T_{Class_ACS}	PSEAC:M	Yes [ ] N/A [ ]
PSE40	Class event voltage/timing	145.2.8.1	Per V_{Class} and T_{CEV}	M	Yes [ ]
PSE41	I_{Class} measurement	145.2.8.1	After T_{Class} on negative pair	M	Yes [ ]
PSE42	Mark event voltage	145.2.8.1	Per V_{Mark}	M	Yes [ ]
PSE43	Mark event timing	145.2.8.1	Per T_{ME1}	M	Yes [ ]
PSE44	Last mark event voltage	145.2.8.1	Per V_{Mark}	M	Yes [ ]
PSE45	Last mark event timing	145.2.8.1	Per T_{ME2}	M	Yes [ ]
PSE46	I_{Class} exceeds I_{Class_LIM} min	145.2.8.1	Return to IDLE, IDLE_PRI, or IDLE_SEC	M	Yes [ ]
PSE47	Class event currents	145.2.8.1	Limit to I_{Class_LIM}	M	Yes [ ]
PSE48	Mark event currents	145.2.8.1	Limit to I_{Mark_LIM}	M	Yes [ ]
PSE49	Class event and mark event voltages polarity	145.2.8.1	Same as defined for V_{Port_PSE-2P} in 145.2.4	M	Yes [ ]
PSE50	Transition from classification to power on	145.2.8.1	Maintain voltage above V_{Mark} min	M	Yes [ ]
PSE51	PSE returns to IDLE	145.2.8.1	$V_{PSE} \leq V_{Reset}$ for a at least T_{Reset} min	M	Yes [ ]
PSE52	PSE returns to IDLE_PRI or IDLE_SEC	145.2.8.1	Maintains the PI voltage on the corresponding pairset in the range of V_{Reset} for a period of at least T_{Reset} min before starting a new detection cycle	M	Yes [ ]
PSE53	PI or pairset voltage during class reset	145.2.8.1	$V_{PSE} \leq V_{Reset}$ for a at least T_{Reset} min	M	Yes [ ]
PSE54	Dual-signature 4PID with Class 3 or less power available	145.2.8.1	Identify Type using classification followed by class reset	M	Yes [ ]
PSE55	pd_autoclass is TRUE when PSE reaches POWER_ON	145.2.8.2	Measure $P_{Autoclass}$	PSEAC:M	Yes [ ] N/A [ ]
PSE56	$P_{Autoclass}$ power consumption	145.2.8.2	Highest average power measured during T_{AUTO_PSE}	PSEAC:M	Yes [ ] N/A [ ]
PSE57	Applying 4-pair power	145.2.9	Only when conditions in 145.2.9 have been met	PSE4P:M	Yes [ ] N/A [ ]
PSE58	Power supply output	145.2.10	When providing power conform with Table 145–16	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE59	Output voltage regulation	145.2.10.1	Under load step conditions defined in 145.2.10.1	M	Yes [ ]
PSE60	Voltage transients	145.2.10.1	Limited to 3.5 V/µs max for load changes up to 35 mA/µs	M	Yes [ ]
PSE61	4-pair power for assigned Class 5 to 8	145.2.10.1	Apply power to both pairsets while in POWER_ON	M	Yes [ ]
PSE62	Output voltage during transients from 30 µs to 250 µs	145.2.10.3	Maintain $V_{PSE} > V_{Tran\text{-}2P}$	M	Yes [ ]
PSE63	Output voltage during transients lasting more than 250 µs	145.2.10.3	Meet $V_{Port\_PSE\text{-}2P}$	M	Yes [ ]
PSE64	Reverse negative pair current	145.2.10.4	Limited to I_{rev}	M	Yes [ ]
PSE65	Output voltage noise	145.2.10.5	V_{Noise} as defined in Table 145–16	M	Yes [ ]
PSE66	Support $I_{Con\text{-}2P}$ on each powered pair	145.2.10.6	As defined in Equation (145–8)	M	Yes [ ]
PSE67	Support $I_{Peak\text{-}2P}$ on each powered pair	145.2.10.6	As defined in Equation (145–10)	M	Yes [ ]
PSE68	PSE unbalance contribution	145.2.10.6.1	Limited to $I_{Unbalance\text{-}2P}$ on any pair	M	Yes [ ]
PSE69	Complete power up	145.2.10.7	Within T_{Inrush} max	M	Yes [ ]
PSE70	$I_{Inrush\text{-}2P}$ and I_{Inrush} limits during power up	145.2.10.7	Per the requirements of Table 145–16	M	Yes [ ]
PSE71	I_{Inrush} and $I_{Inrush\text{-}2P}$ when V_{PSE} is less than 30 V	145.2.10.7	Per minimum in 145.2.10.7	M	Yes [ ]
PSE72	Pairset current limiting	145.2.10.9	Limit to $I_{LIM\text{-}2P}$ for at least T_{LIM} as defined in Table 145–16	M	Yes [ ]
PSE73	Power removal when current limit persists	145.2.10.9	Maximum T_{LIM} max per Table 145–16	M	Yes [ ]
PSE74	Upperbound template	145.2.10.9	Remove pairset power before the pairset current exceeds the upperbound template	M	Yes [ ]
PSE75	Turn off time	145.2.10.10	From $V_{Port\_PSE\text{-}2P}$ min to V_{Off}	M	Yes [ ]
PSE76	PI voltage when idle	145.2.10.11	Equal to or less than V_{Off}, as defined in Table 145–16	M	Yes [ ]
PSE77	Pairset voltage when idle	145.2.10.11	Equal to or less than V_{Off}, as defined in Table 145–16	M	Yes [ ]
PSE78	Supported intra-pair current unbalance	145.2.10.12	I_{unb} in Equation (145–20)	M	Yes [ ]
PSE79	Endpoint PSEs transmitting 100BASE-TX in the presence of (I_{unb} / 2)	145.2.10.12	Meet the requirements of 25.4.5	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE80	Type 4 PSE output power limit	145.2.10.13	Not more than P_{Type} max	PSET4:M	Yes [ ] N/A [ ]
PSE81	Detection to POWER_ON time (single-signature)	145.2.10.14	Within T_{pon} after completing detection on the last pairset	M	Yes [ ]
PSE82	Detection to POWER_ON time per pairset (dual-signature)	145.2.10.14	Within T_{pon} after completing detection on the same pairset	M	Yes [ ]
PSE83	Power allocation	145.2.11	Not based solely on historical data of power consumption	M	Yes [ ]
PSE84	MPS applicable parameters	145.2.12	I_{Hold}, $I_{Hold-2P}$, T_{MPS}, and T_{MPDO} values as defined in Table 145–16	M	Yes [ ]
PSE85	Consider DC MPS component present (2-pair)	145.2.12	$I_{Port-2P} \geq I_{Hold-2P}$ max continuously for at least T_{MPS}	M	Yes [ ]
PSE86	Consider DC MPS component absent (2-pair)	145.2.12	$I_{Port-2P} \leq I_{Hold-2P}$ min	M	Yes [ ]
PSE87	Power removal (2-pair)	145.2.12	DC MPS has been absent for longer than T_{MPDO}	M	Yes [ ]
PSE88	Maintain power (2-pair)	145.2.12	DC MPS has been present within the $T_{MPS} + T_{MPDO}$ window	M	Yes [ ]
PSE89	Consider DC MPS component present (4-pair, single-signature)	145.2.12	$I_{Port-2P}$ of the pairset with the highest current $\geq I_{Hold-2P}$ max and I_{Port} is $\geq I_{Hold}$ max continuously for a minimum of T_{MPS}	M	Yes [ ]
PSE90	Consider DC MPS component absent (4-pair, single-signature)	145.2.12	$I_{Port-2P}$ of the pairset with the highest current $\leq I_{Hold-2P}$ min and $I_{Port} \leq I_{Hold}$ min	M	Yes [ ]
PSE91	Power removal (4-pair, single-signature)	145.2.12	DC MPS has been absent for longer than T_{MPDO}	M	Yes [ ]
PSE92	Maintain power (4-pair, single-signature)	145.2.12	DC MPS has been present within the $T_{MPS} + T_{MPDO}$ window	M	Yes [ ]
PSE93	Dual-signature PD independent MPS	145.2.12	Considered to be present or absent on each pairset independently	M	Yes [ ]
PSE94	Consider DC MPS component present (4-pair, dual-signature)	145.2.12	$I_{Port-2P} \geq I_{Hold-2P}$ max continuously for a minimum of T_{MPS}	M	Yes [ ]
PSE95	Consider DC MPS component absent (4-pair, dual-signature)	145.2.12	$I_{Port-2P} \leq I_{Hold-2P}$ min	M	Yes [ ]
PSE96	Pairset power removal (4-pair, dual-signature)	145.2.12	DC MPS has been absent on that pairset for longer than T_{MPDO}	M	Yes [ ]
PSE97	Maintain power on pairset (4-pair, dual-signature)	145.2.12	DC MPS has been present on both pairsets within the $T_{MPS} + T_{MPDO}$ window	M	Yes [ ]

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145.7.3.2 Powered devices

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Accept power	145.3.2	Per any configuration defined in Table 145–20	M	Yes [ ]
PD2	Two positive pairs	145.3.2	Meet requirements of detection, signature configuration, and classification	M	Yes [ ]
PD3	Meet specification related to current (single-signature PD)	145.3.2	Total current	PDSS:M	Yes [ ] N/A [ ]
PD4	Meet specification related to current (dual-signature PD)	145.3.2	Current on the negative pair of the given Mode	PDDS:M	Yes [ ] N/A [ ]
PD5	Mode polarity	145.3.2	Insensitive to the polarity of the voltage	M	Yes [ ]
PD6	Operation of single-signature PDs that request Class 4 or less	145.3.2	Per any configuration defined in Table 145–20	PDSS:M	Yes [ ] N/A [ ]
PD7	Source power	145.3.2	Do not source power on the PI	M	Yes [ ]
PD8	Voltage tolerance	145.3.2	Withstand 0 V to 57 V at the PI indefinitely without permanent damage	M	Yes [ ]
PD9	Single-signature PD behavior	145.3.3.3	According to state diagram shown in Figure 145–25 and Figure 145–26	PDSS:M	Yes [ ] N/A [ ]
PD10	Dual-signature PD behavior	145.3.3.4	According to state diagram shown in Figure 145–27 over each pairset independently	PDDS:M	Yes [ ] N/A [ ]
PD11	Valid and non-valid detection signatures	145.3.4	Presented between positive V_{PD} and negative V_{PD} of PD Mode A and PD Mode B as defined in 145.3.2	M	Yes [ ]
PD12	Valid detection signature powering conditions	145.3.4	Per the list in 145.3.4	M	Yes [ ]
PD13	Single-signature PDs powered over only one pairset	145.3.4	Present a non-valid detection signature on the unpowered pairset	PDSS:M	Yes [ ] N/A [ ]
PD14	Dual signature PDs powered over only one pairset	145.3.4	Present a valid detection signature on the unpowered pairset	PDDS:M	Yes [ ] N/A [ ]
PD15	Valid detection signature	145.3.4	Characteristics defined in Table 145–21	M	Yes [ ]
PD16	Non-valid detection signature	145.3.4	Exhibit one or both of the characteristics described in Table 145–22	M	Yes [ ]
PD17	Single-signature PD configuration	145.3.5	Valid detection signature when no voltage/current applied across the other Mode	PDSS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD18	Single-signature PD configuration	145.3.5	Invalid detection signature when voltage/current applied across the other Mode	PDSS:M	Yes [ ] N/A [ ]
PD19	Dual-signature PD configuration	145.3.5	Valid detection signature regardless of voltage applied to the other Mode	PDDS:M	Yes [ ] N/A [ ]
PD20	Maximum power drawn	145.3.6	No more than defined for the requested Class in Table 145–26 and Table 145–27	M	Yes [ ]
PD21	Conform to the assigned Class	145.3.6	Regardless of requested Class	M	Yes [ ]
PD22	Multiple-Event classification	145.3.6	Supported by the PD	M	Yes [ ]
PD23	Data Link Layer classification	145.3.6	Supported by single-signature PDs that request Class 4 or higher, and dual-signature PDs that request Class 4 or higher on at least one of its Modes	M	Yes [ ]
PD24	PD classification behavior	145.3.6	Conforms to the state diagram in Figure 145–25, and Figure 145–27	M	Yes [ ]
PD25	PD classification electrical specifications	145.3.6	As defined in Table 145–24 and Table 145–25	M	Yes [ ]
PD26	Underpowered PDs	145.3.6	Provide user with active indication if underpowered	M	Yes [ ]
PD27	Class signature presented during classification events	145.3.6.1	Present class_sig_A during first and second event, class_sig_B during subsequent events	M	Yes [ ]
PD28	Class signature during Autoclass	145.3.6.1	Present class_sig_0	PDAC:M	Yes [ ] N/A [ ]
PD29	Class signature validity	145.3.6.1	Valid within T_{Class_PD} as defined in Table 145–29	M	Yes [ ]
PD30	Advertised class signatures for single-signature PDs	145.3.6.1	Per PD Type and requested Class, as defined in Table 145–26	PDSS:M	Yes [ ] N/A [ ]
PD31	Advertised class signature for dual-signature PDs	145.3.6.1	Per PD Type and requested Class, as defined in Table 145–27	PDDS:M	Yes [ ] N/A [ ]
PD32	Dual-signature PDs powered over only one pairset	145.3.6.1	Present a valid classification signature on the unpowered pairset	PDDS:M	Yes [ ] N/A [ ]
PD33	PD current draw when in a DO_MARK_EVENT state	145.3.6.1.1	Draw I_{Mark} and present a non-valid detection signature	M	Yes [ ]
PD34	Mark event current limits	145.3.6.1.1	Not exceed I_{Mark}	M	Yes [ ]
PD35	Autoclass class signature timing	145.3.6.2	Show class signature 0 between T_{ACS} min and T_{ACS} max	PDAC:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD36	Autoclass power draw	145.3.6.2	Draw $P_{Autoclass_PD}$between T_{AUTO_PD1} and T_{AUTO_PD2}	PDAC:M	Yes [ ] N/A [ ]
PD37	PSE Type identification	145.3.7	Set long_class_event to TRUE if the first class event is longer than T_{LCE_PD} max	M	Yes [ ]
PD38	PD operation	145.3.8	Operate within the characteristics in Table 145–29	M	Yes [ ]
PD39	PD turn on voltage	145.3.8.1	At a voltage in the range of V_{On_PD}	M	Yes [ ]
PD40	PD stay on voltage	145.3.8.1	Over the entire V_{Port_PD-2P} range	M	Yes [ ]
PD41	PD turn off voltage	145.3.8.1	At a voltage in the range of V_{Off_PD}	M	Yes [ ]
PD42	Peak power draw or voltage transients present	145.3.8.1	PD not to turn off	M	Yes [ ]
PD43	Startup oscillations	145.3.8.1	Turn on or off without startup oscillations and within the first trial at any load value	M	Yes [ ]
PD44	P_{Port_PD} (single-signature PD)	145.3.8.2	Not to exceed P_{Class_PD} for the assigned class	PDSS:M	Yes [ ] N/A [ ]
PD45	P_{Port_PD-2P} (dual-signature PD)	145.3.8.2	Not to exceed P_{Class_PD-2P} for the assigned class	PDDS:M	Yes [ ] N/A [ ]
PD46	Power draw for Autoclass PDs	145.3.8.2	Not more than $P_{Autoclass\_PD}$	PDAC:M	Yes [ ] N/A [ ]
PD47	Power consumption after DLL classification	145.3.8.2	PDMaxPowerValue as defined in 145.5.3.3.1	PDSS:M	Yes [ ] N/A [ ]
PD48	Power consumption after DLL classification	145.3.8.2	PDMaxPowerValue_mode(X) as defined in 145.5.3.4.2	PDDS:M	Yes [ ] N/A [ ]
PD49	Input average power exceptions for single-signature PDs	145.3.8.2.1	Limited to P_{Class} at the PSE PI and current draw of 2 x I_{Cable}	WEXP:M	Yes [ ] N/A [ ]
PD50	Input average power exceptions for dual-signature PDs	145.3.8.2.1	Limited to $P_{Class-2P}$ at the PSE PI and current draw of I_{Cable}	WEXP:M	Yes [ ] N/A [ ]
PD51	PD input inrush current	145.3.8.3	Draw less than I_{Inrush_PD} and I_{Inrush_PD-2P} from T_{Inrush_PD} max until T_{delay} min	M	Yes [ ]
PD52	P_{Class_PD} and P_{Peak_PD} for single-signature PDs assigned to Class 1, 2, or 3	145.3.8.3	Within T_{Inrush_PD} max as defined in Table 145–29	PDSS:M	Yes [ ] N/A [ ]
PD53	P_{Class_PD-2P} and P_{Peak_PD-2P} for dual-signature PDs assigned to Class 1, 2, or 3	145.3.8.3	Within T_{Inrush_PD} max as defined in Table 145–29 on that pairset	PDDS:M	Yes [ ] N/A [ ]
PD54	Peak power	145.3.8.4	Not to exceed P_{Class_PD} for more than T_{CUT} min and 5% duty cycle	!WEXP*PDSS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD55	Peak power	145.3.8.4	Not to exceed P_{Class_PD-2P} for more than T_{CUT} min and 5% duty cycle	!WEXP*PDDS: M	Yes [ ] N/A [ ]
PD56	Peak operating power exceptions	145.3.8.4.1	Not to exceed P_{Port_PD} max or P_{Port_PD-2P} max at the PSE PI for more than T_{CUT} min with 5% duty cycle	WEXP:M	Yes [ ] N/A [ ]
PD57	Peak operating power limit	145.3.8.4.1	Not to exceed $1.05 \times P_{Port\_PD}$ max for single-signature PDs and $1.05 \times P_{Port\_PD-2P}$ max for dual-signature PDs on each pairset	WEXP:M	Yes [ ] N/A [ ]
PD58	Peak transient current for single-signature PDs	145.3.8.5	Maximum $I_{Slewrate}$ as defined in Table 145–29	PDSS:M	Yes [ ] N/A [ ]
PD59	Peak transient current for dual-signature PDs	145.3.8.5	Maximum $I_{Slewrate}$ per pairset as defined in Table 145–29	PDDS:M	Yes [ ] N/A [ ]
PD60	Behavior during transients at the PSE PI	145.3.8.6	Continue to operate without interruption	M	Yes [ ]
PD61	Transient TR1 or TR2 applied (power limit)	145.3.8.6	Meet power limit within $T_{Transient}$	M	Yes [ ]
PD62	Transient TR1 or TR2 applied (source current limit)	145.3.8.6	Not cause source the limit current for longer than T_{LIM} min	M	Yes [ ]
PD63	Transient TR3 applied	145.3.8.6	PD meet operating power limits within 4 ms	M	Yes [ ]
PD64	Ripple and noise	145.3.8.7	As specified in Table 145–29 for the common-mode and/or differential pair-to-pair noise at the PD PI	M	Yes [ ]
PD65	Ripple and noise presence	145.3.8.7	Operate correctly in the presence of ripple and noise generated by the PSE that appears at the PD PI	M	Yes [ ]
PD66	Reflected voltage (single-signature PD)	145.3.8.8	Limited to V_{refl} with one positive pair connected	PDSS:M	Yes [ ]
PD67	Reflected voltage (dual-signature PD)	145.3.8.8	Limited to V_{refl} with one or two positive pairs connected	PDDS:M	Yes [ ]
PD68	Pair-to-pair current unbalance for single-signature PDs	145.3.8.9	Not to exceed $I_{Unbalance-2P}$ under conditions specified in 145.3.8.9	PDSS:M	Yes [ ] N/A [ ]
PD69	Pair-to-pair peak current unbalance for single-signature PDs	145.3.8.9	Not to exceed $I_{Unbalance\_peak-2P}$ under conditions specified in 145.3.8.9	PDSS:M	Yes [ ] N/A [ ]
PD70	Pair-to-pair current unbalance for dual-signature PDs	145.3.8.9	Not to exceed I_{Con_PD-2P} under conditions specified in 145.3.8.9	PDDS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD71	Pair-to-pair peak current unbalance for dual-signature PDs	145.3.8.9	Not to exceed $I_{Peak\_PD\text{-}2P}$ under conditions specified in 145.3.8.9	PDDS:M	Yes [ ] N/A [ ]
PD72	PD that requires power from the PI	145.3.9	Provide a valid MPS at the PI	M	Yes [ ] N/A [ ]
PD73	MPS for single-signature PDs	145.3.9	Current draw ≥ I_{Port_MPS} for at least T_{MPS_PD}	PDSS:M	Yes [ ] N/A [ ]
PD74	I_{Port_MPS} value for single-signature PDs assigned Class 1 to 4	145.3.9	Per Table 145–32 and 145.3.9	PDSS:M	Yes [ ] N/A [ ]
PD75	I_{Port_MPS} value for single-signature PDs assigned Class 5 to 8	145.3.9	Per Table 145–32 and 145.3.9	PDSS:M	Yes [ ] N/A [ ]
PD76	I_{Port_MPS} value when using DLL Autoclass	145.3.9	Associated with assigned Class	M	Yes [ ] N/A [ ]
PD77	MPS for dual-signature PDs on each pairset independently	145.3.9	Current draw ≥ $I_{Port\_MPS\text{-}2P}$ for at least T_{MPS_PD}	PDDS:M	Yes [ ] N/A [ ]
PD78	Input impedance for PDs connected to Type 1 or Type 2 PSEs	145.3.9	With resistive and capacitive components defined in Table 145–33	M	Yes [ ] N/A [ ]
PD79	T_{MPS_PD} and T_{MPDO_PD}	145.3.9	Met with any series resistance in the range of 0 to R_{Chan} max	M	Yes [ ] N/A [ ]
PD80	Powered PDs that no longer require power, and identify the PSE as Type 1 or Type 2	145.3.9	Remove both the current draw and impedance components of the MPS	M	Yes [ ] N/A [ ]
PD81	Powered PDs that no longer require power and identify the PSE as Type 3 or Type 4	145.3.9	Remove the current draw component of the MPS	M	Yes [ ] N/A [ ]

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145.7.3.3 Electrical specifications applicable to the PSE and PD

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Conductor isolation	145.4.1	Provided between accessible external conductors including frame ground and all MDI leads	M	Yes [ ]
EL2	Strength tests for electrical isolation	145.4.1	Conforms to J.1 with electrical strength test c) details as specified in 145.4.1	M	Yes [ ]
EL3	Isolation and grounding requirements	145.4.1	Conductive link segments that have different requirements have those requirements provided by the port-to-port isolation of the NID	M	Yes [ ]
EL4	Environment A requirements for multiple instances of PSE and/or PD	145.4.1.1.1	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL5	Environment A requirement	145.4.1.1.1	Switch more negative conductor	M	Yes [ ]
EL6	Environment B requirements for multiple instances of PSE and/or PD	145.4.1.1.2	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL7	Environment B requirements for PSE that supports 4-pair power	145.4.1.1.2	Switch more negative conductor	PS4P:M	Yes [ ] N/A [ ]
EL8	Fault tolerance for PIs encompassed within the MDI	145.4.2	Meet requirements of the appropriate specifying clause	!MID:M	Yes [ ] N/A [ ]
EL9	Fault tolerance for PSE PIs not encompassed within an MDI	145.4.2	Meet the requirements of 145.4.2	MID:M	Yes [ ] N/A [ ]
EL10	Common-mode fault tolerance	145.4.2	Each wire pair withstands without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity	M	Yes [ ]
EL11	The shape of the impulse for item common-mode fault tolerance	145.4.2	0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value)	M	Yes [ ]
EL12	Common-mode to differential-mode impedance balance for transmit and receive pairs	145.4.3	Exceeds value in Table 145–34 for all supported PHY speeds	M	Yes [ ]
EL13	Common-mode AC output voltage	145.4.4	Magnitude while transmitting data and with power applied does not exceed the values in Table 145–35 while operating at the specified speed, when measured over the specified bandwidth	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
EL14	Common-mode AC output voltage measurement	145.4.4	While the PHY is transmitting data, the PSE or PD is operating, and with the enumerated PSE load or PD source	M	Yes [ ]
EL15	Noise from an operating 10/100/1000 Mb/s PSE or PD to the differential transmit and receive pairs	145.4.6	Per the limits in 145.4.6 under the conditions specified in 145.4.4	M	Yes [ ]
EL16	Noise from an operating 2.5GBASE-T, 5GBASE-T, or 10GBASE-T PSE or PD to the differential transmit and receive pairs	145.4.6	Per the limits in 145.4.6	M	Yes [ ]
EL17	Return loss requirements	145.4.7	Specified in 145.4.7 per PHY	M	Yes [ ]
EL18	100BASE-TX Endpoint PSE and 100BASE-TX PD unbalance	145.4.8	Meet requirements of Clause 25 in the presence of (I_{unb} / 2)	M	Yes [ ]

145.7.3.4 Electrical specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL1	Withstand short circuits without damage	145.4.2	Of any conductors in the cable for an indefinite period of time	M	Yes [ ]
PSEEL2	Magnitude of short circuit current between any two conductors for Type 3 PSEs	145.4.2	Does not exceed $I_{PSEUT\text{-}Type3\text{-}2P}$, as defined in Equation (145–17)	PSET3:M	Yes [ ] N/A [ ]
PSEEL3	Magnitude of short circuit current between any two conductors for Type 4 PSEs	145.4.2	Does not exceed $I_{PSEUT\text{-}Type4\text{-}2P}$, as defined in Equation (145–18)	PSET4:M	Yes [ ] N/A [ ]
PSEEL4	Limitation of electromagnetic interference.	145.4.5	PSE complies with applicable local and national codes	M	Yes [ ]
PSEEL5	Alternative A Midspan PSEs that support 100BASE-TX	145.4.8	Enforce channel unbalance currents less than or equal to 10.5mA or meet 145.4.9.3.	MIDA:M	Yes [ ] N/A [ ]
PSEEL6	Insertion of Midspan at FD	145.4.9	Comply with the guidelines specified in 145.4.9 items a), b), and c)	MID:M	Yes [ ] N/A [ ]
PSEEL7	Resulting “channel”	145.4.9	Installation of a Midspan PSE does not increase the length to more than 100 m as defined in ISO/IEC 11801-1.	MID:M	Yes [ ] N/A [ ]
PSEEL8	Configurations with Midspan PSE	145.4.9	Not alter transmission requirements of the “permanent link”	MID:M	Yes [ ] N/A [ ]
PSEEL9	DC continuity in power injecting pairs	145.4.9	Does not provide DC continuity between the two sides of the segment for the pairs that inject power	MID:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL10	Connector Midspan PSE device transmission requirements	145.4.9.1	Meet transmission parameters NEXT, insertion loss, and return loss	MID:M	Yes [ ] N/A [ ]
PSEEL11	Midspan PSE NEXT when operating with 10/100/1000 Mb/s or 2.5GBASE-T	145.4.9.1.1	Meet values determined by Equation (145–31) from 1 MHz to 100 MHz, but not greater than 65 dB	MID:M	Yes [ ] N/A [ ]
PSEEL12	Midspan PSE NEXT when operating with 5GBASE-T	145.4.9.1.1	Meet the values determined by Equation (145–31) from 1 MHz to 250 MHz, but not greater than 65 dB	MID:M	Yes [ ] N/A [ ]
PSEEL13	Midspan PSE NEXT when operating with 10GBASE-T	145.4.9.1.1	Meet the values determined by Equation (145–31)from 1 MHz to 500 MHz, but not greater than 75 dB	MID:M	Yes [ ] N/A [ ]
PSEEL14	Midspan PSE Insertion Loss when operating with 10/100/1000 Mb/s or 2.5GBASE-T	145.4.9.1.2	Meet values determined by Equation (145–33) from 1 MHz to 100 MHz, but not less than 0.1 dB	MID:M	Yes [ ] N/A [ ]
PSEEL15	Midspan PSE Insertion Loss when operating at 5GBASE-T	145.4.9.1.2	Meet values determined by Equation (145–33) from 1 MHz to 250 MHz, but not less than 0.1 dB	MID:M	Yes [ ] N/A [ ]
PSEEL16	Midspan PSE Insertion Loss when operating at 10GBASE-T	145.4.9.1.2	Meet values determined by Equation (145–33) from 1 MHz to 500 MHz, but not less than 0.1 dB	MID:M	Yes [ ] N/A [ ]
PSEEL17	Midspan PSE Return Loss	145.4.9.1.3	Meet or exceed values in Table 145–36	MID:M	Yes [ ] N/A [ ]
PSEEL18	Cord Midspan PSE	145.4.9.2	Meet the requirements of this clause and the specifications for a (jumper) cord for insertion loss, NEXT, and return loss for transmit and receive pairs, as defined in Table 145–37	MID:M	Yes [ ] N/A [ ]
PSEEL19	Midspan PSE maximum link delay	145.4.9.2.1	Not to exceed 2.5 ns from 1 MHz to the highest referenced frequency	MID:M	Yes [ ] N/A [ ]
PSEEL20	Midspan PSE maximum link delay skew	145.4.9.2.2	Not to exceed 1.25 ns from 1 MHz to the highest referenced frequency	MID:M	Yes [ ] N/A [ ]
PSEEL21	Alternative A Midspan PSE signal path requirements	145.4.9.3	Exceed transfer function gain expressed in Equation (145–34) from 0.1 MHz to 1 MHz at the pins of the PI used as 100BASE-TX transmit pins	MIDA:M	Yes [ ] N/A [ ]
PSEEL22	Alternative A Midspan PSE signal path requirements bias current	145.4.9.3	Met with DC bias current, I_{bias}, between 0 mA and (I_{unb}/2)	MIDA:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL23	Midspan PSE PSANEXT loss for 2.5G/5G/10GBASE-T	145.4.9.4.1	Meet or exceed the values determined using Equation (145–35)	MID:M	Yes [ ] N/A [ ]
PSEEL24	PSANEXT loss values greater than 67 dB	145.4.9.4.1	Revert to a requirement of 67 dB minimum	MID:M	Yes [ ] N/A [ ]
PSEEL25	Midspan PSE PSAFEXT loss for 2.5G/5G/10GBASE-T	145.4.9.4.2	Meet or exceed the values determined using Equation (145–35)	MID:M	Yes [ ] N/A [ ]
PSEEL26	PSAFEXT loss values greater than 67 dB	145.4.9.4.2	Revert to a requirement of 67 dB minimum	MID:M	Yes [ ] N/A [ ]

145.7.3.5 Electrical specifications applicable to the PD

Item	Feature	Subclause	Value/Comment	Status	Support
PDEL1	Isolation for dual-signature PDs when V_{PD} of either Mode is less than V_{Off_PD} min	145.4.1	Less than or equal to 10 μA of current between any one negative conductor of Mode A and any one negative conductor of Mode B	PDDS:M	Yes [ ] N/A [ ]
PDEL2	PD common-mode test requirement	145.4.4	The PIs that require power terminated as illustrated in Figure 145–36	M	Yes [ ]

145.7.3.6 Data Link Layer classification requirements

Item	Feature	Subclause	Value/Comment	Status	Support
DLL1	Data Link Layer classification standards compliance	145.5.1	Meet mandatory parts of IEEE Std 802.1AB-2016	DLLC:M	Yes [ ] N/A [ ]
DLL2	TLV frame definitions	145.5.1	Support the Power via MDI Type, Length, and Value (TLV) defined in 79.3.2	DLLC:M	Yes [ ] N/A [ ]
DLL3	Control state diagrams	145.5.1	Meet state diagrams defined in 145.5.3	DLLC:M	Yes [ ] N/A [ ]
DLL4	Reserved fields in Power via MDI TLVs	145.5.1	Transmitted containing zero and ignored when received	DLLC:M	Yes [ ] N/A [ ]
DLL5	PSE LLDPDU	145.5.2	Transmitted within 10 seconds of Data Link Layer classification being enabled as indicated by pse_dll_enable	DLLC:M	Yes [ ] N/A [ ]
DLL6	PD Data Link Layer classification ready	145.5.2	Set pd_dll_ready within 5 minutes of Data Link Layer classification being enabled as indicated by pd_dll_enable	DLLC:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DLL7	PD requested power value or PD requested power value Mode A/B changes	145.5.2	Updated LLDPDU sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL8	PSE allocated power value or PSE allocated power value Alternative A/B changes	145.5.2	Updated LLDPDU sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL9	PSE power control state diagrams	145.5.3	Meet the behavior shown in Figure 145–40, Figure 145–41, Figure 145–42, and Figure 145–43	DLLC:M	Yes [ ] N/A [ ]
DLL10	Single-signature PD power control state diagrams	145.5.3	Meet the behavior shown in Figure 145–44 and Figure 145–45	DLLC* PDSS:M	Yes [ ] N/A [ ]
DLL11	Dual-signature PD power control state diagrams	145.5.3	Meet the behavior shown in Figure 145–46 and Figure 145–47	DLLC* PDDS:M	Yes [ ] N/A [ ]
DLL12	PSEAllocatedPowerValue, PSEAllocatedPowerValue_alt(A), and PSEAllocatedPowerValue_alt(B)	145.5.4	PSE sets value in the range defined in Table 145–41	DLLC:M	Yes [ ] N/A [ ]
DLL13	PDRequestedPowerValue, PDRequestedPowerValue_alt(A), and PDRequestedPowerValue_alt(B)	145.5.4	PD sets value in the range defined in Table 145–42	DLLC:M	Yes [ ] N/A [ ]
DLL14	Transition from 4-pair to 2-pair operation for PSEs connected to dual-signature PDs	145.5.6.1	Assign value of PSEAllocatedPowerValue_alt(X), to PSEAllocatedPowerValue	DLLC*PS4P:M	Yes [ ] N/A [ ]
DLL15	Transition from 2-pair to 4-pair operation for PSEs connected to dual-signature PDs	145.5.6.1	Assign value of PSEAllocatedPowerValue, to PSEAllocatedPowerValue_alt(X)	DLLC*PS4P:M	Yes [ ] N/A [ ]
DLL16	PSE receives request for Autoclass when Autoclass is enabled	145.5.7	Measure the power consumption per the requirements in 145.2.8.2	DLLC* PSEAC:M	Yes [ ] N/A [ ]

145.7.3.7 Environmental specifications applicable to PSEs and PDs

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Safety	145.6.1	Conforms to J.2	M	Yes [ ]
ES2	Safety	145.6.1	Comply with all applicable local and national codes	M	Yes [ ]
ES3	Electromagnetic interference	145.6.5	Comply with all applicable local and national codes	M	Yes [ ]

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145.7.3.8 Environmental specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEES1	Safety	145.6.1	Limited Power Source in accordance with Annex Q of IEC 62368-1:2018, as applicable.	M	Yes [ ]

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146. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1L

146.1 Overview

This clause defines the type 10BASE-T1L Physical Coding Sublayer (PCS) and type 10BASE-T1L Physical Medium Attachment (PMA) sublayer. Together, the PCS and PMA sublayers comprise a 10BASE-T1L Physical Layer device (PHY). Provided in this clause are functional and electrical specifications for the type 10BASE-T1L PCS, PMA, and MDI. 10BASE-T1L does not define an AUI.

The 10BASE-T1L PHY is a full-duplex PHY specification, capable of operating at 10 Mb/s. The 10BASE-T1L PHY is intended to be operated over a single balanced pair of conductors, defined in 146.7. The cabling supporting the operation of the 10BASE-T1L PHY is defined in terms of performance requirements between the DTE attachment points [Medium Dependent Interface (MDI)], allowing implementers to provide their own cabling to operate the 10BASE-T1L PHY as long as the normative requirements included in this clause are met.

This clause also specifies an optional Energy-Efficient Ethernet (EEE) capability. A 10BASE-T1L PHY that supports this capability may enter a Low Power Idle (LPI) mode of operation during periods of low link utilization as described in Clause 78.

146.1.1 Relationship of 10BASE-T1L to other standards

The relationship between the 10BASE-T1L PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet model are shown in Figure 146–1. The PHY sublayers (shown shaded) in Figure 146–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto-Negotiation for 10BASE-T1L is defined in Clause 98. MII is defined in Clause 22.

146.1.2 Operation of 10BASE-T1L

The 10BASE-T1L PHY operates using full-duplex communications over a single balanced pair of conductors with an effective data rate of 10 Mb/s in each direction simultaneously. The PHY supports operation on a link segment supporting up to ten in-line connectors using a single balanced pair of conductors for up to at least 1000 meters.

The 10BASE-T1L PHY utilizes 3-level Pulse Amplitude Modulation (PAM3) transmitted at 7.5 MBd on the link segment. A 33-bit scrambler is used to improve the EMC performance. MII TXD<3:0>, TX_EN, and TX_ER are encoded together using 4B3T encoding, where 4B3T encoding is used to keep the running average (DC baseline) of the transmitted PAM3 symbols within bounds. The PAM3 mapping, scrambler, and 4B3T encoder/decoder are all contained in the PCS (see 146.3).

The 10BASE-T1L PHY may optionally support an increased transmit and receive capability, supporting 2.4 Vpp differential. See 146.5.4.1.

Auto-Negotiation may be used by 10BASE-T1L devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for normal operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding. If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.

A 10BASE-T1L PHY optionally supports Energy-Efficient Ethernet (see Clause 78) and advertises the EEE capability during Auto-Negotiation as described in 98B.3. The EEE capability is a mechanism by which 10BASE-T1L PHYs are able to reduce power consumption during periods of low link utilization.

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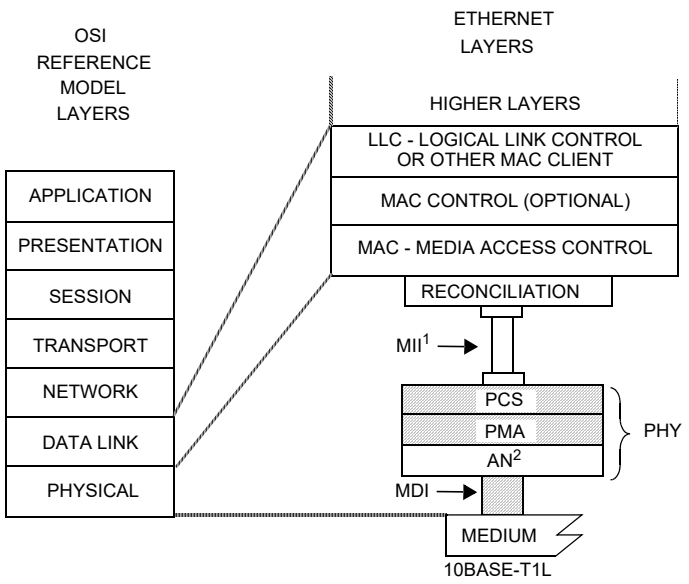

MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE

NOTE 1—MII is optional
NOTE 2—Auto-Negotiation is optional

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

Figure 146–1—Relationship of 10BASE-T1L PHY to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

A 10BASE-T1L PHY is capable of operating both as MASTER or SLAVE, with one mode active as determined according to 146.6.2. A MASTER PHY uses a local clock to determine the timing of transmitter operations. A SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations. When Auto-Negotiation is used, the MASTER-SLAVE relationship between two devices sharing a link segment is established during Auto-Negotiation (see Clause 98). If Auto-Negotiation is not used, a MASTER-SLAVE relationship shall be established by management or hardware configuration of the PHYs. The MASTER and SLAVE are synchronized by a PMA Clock Recovery function (see 146.4.6).

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

The 10BASE-T1L PMA couples messages from the PCS to the MDI and provides clock recovery, link management, and PHY Control functions. The PMA provides full duplex communications at 7.5 MBd over a single balanced pair of conductors. PMA functionality is described in 146.4. The MDI is specified in 146.8.

146.1.2.1 Physical Coding Sublayer (PCS)

The 10BASE-T1L PCS couples a Media Independent Interface (MII), as described in Clause 22, to the 10BASE-T1L Physical Medium Attachment (PMA) sublayer.

146.1.2.2 Physical Medium Attachment (PMA) sublayer

The 10BASE-T1L PMA couples messages from the PCS service interface onto a single balanced pair of conductors and supports the link management and the 10BASE-T1L PHY Control function. The PMA provides full duplex communications over a single balanced pair of conductors up to 1000 m in length.

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146.1.2.3 EEE capability

A 10BASE-T1L PHY optionally supports the EEE capability, as described in 78.3. The EEE capability is a mechanism by which 10BASE-T1L PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter the LPI mode of operation after completing training. Each direction of the full duplex link is able to enter and exit the LPI mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full duplex link is in a period of low utilization. The transition to or from LPI mode does not cause any MAC frames to be lost or corrupted.

In the transmit direction, the transition to the LPI transmit mode begins when the PCS transmit function detects an "Assert Low Power Idle" condition on the MII. If this condition is detected, tx_lpi_active is set true and shortly after this the PHY asserts the loc_lpi signal, which is transmitted within the IDLE symbol stream to the remote PHY. This sleep signal indicates to the link partner that the transmit function of the PHY is entering the LPI transmit mode. After the transmission of the sleep indications, the transmit function of the local PHY enters the LPI transmit mode. While the transmit function is in the LPI mode, the PHY may cease transmission to save power and the link partner may disable receiver functions to save additional power. Periodically, the transmit function of the local PHY enters a refresh mode during which idle transmission resumes, and this may be used by the link partner to update adaptive filters and timing recovery circuits. Alternation between LPI quiet and refresh transmit modes proceeds according to a synchronized process between the PHYs, independent of data traffic patterns at the MII. The quiet-refresh cycling continues until the PCS function detects a condition that is not Assert Low Power Idle on the MII. This condition signals to the PHY that the LPI transmit mode should end. The PHY transmits an IDLE symbol stream with loc_lpi de-asserted, indicating to the remote PHY that the local PHY is back to normal transmit mode.

Support for EEE capability is advertised during Auto-Negotiation. See 98B.3 for details. Transitions to and from the LPI transmit mode are controlled via MII signaling. Transitions to and from the LPI receive mode are controlled by the link partner using sleep and wake signaling.

146.1.2.4 Signaling

10BASE-T1L signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over a single balanced pair of conductors. The signaling scheme achieves a number of objectives including the following:

a) Algorithm mapping and inverse mapping from nibble data to ternary symbols and back.
b) Uncorrelated symbols in the transmitted symbol stream.
c) No correlation between symbol streams traveling both directions.
d) Ability to rapidly or immediately determine if a symbol stream represents data or idle.
e) Robust delimiters for Start-of-Stream delimiter (SSD), End-of-Stream delimiter (ESD), and other control signals.
f) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
g) Optionally, ability to signal to the remote PHY that the transmitting PHY is entering the LPI mode or exiting the LPI mode and returning to normal power operation.

146.1.3 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

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146.1.3.1 State diagram notation

The conventions of 21.5 are adopted with the extension that some states in the state diagrams use an IF-THEN-ELSE-END construct to condition which actions are taken within the state. If the logical expression associated with the IF evaluates TRUE, all the actions listed between THEN and ELSE will be executed. In the case where ELSE is omitted, the actions listed between THEN and END will be executed. If the logical expression associated with the IF evaluates FALSE, the actions listed between ELSE and END will be executed. After executing the actions listed between THEN and ELSE, between THEN and END, or between ELSE and END, the actions following the END, if any, will be executed.

146.1.3.2 State diagram timer specifications

All timers operate in the manner described in 40.4.5.2.

146.1.3.3 Service specifications

The method and notation used in the service specification follows the conventions of 1.2.2.

146.2 Service primitives and interfaces

The 10BASE-T1L PHY uses the service primitives and interfaces in 40.2, with exception of the following clarifications and differences noted in this subclause, in support of 10 Mb/s operations over a single balanced pair of conductors. Figure 146–2 shows the relationship of the service primitives and interfaces used by the 10BASE-T1L PHY.

The 10BASE-T1L PHY uses the Media Independent Interface (MII) as specified in Clause 22. The optional Technology Dependent Interface is used for Auto-Negotiation and is described in 98.4.

As shown in Figure 146–2, 10BASE-T1L uses the following service primitives to exchange symbol vectors, status indications, and control signals across the PMA service interface:

PMA_LINK.request (link_control)
PMA_LINK.indication (link_status)
PMA_TXMODE.indication (tx_mode)
PMA_UNITDATA.indication (rx_symb_vector)
PMA_UNITDATA.request (tx_symb_vector)
PMA_RXSTATUS.indication (loc_rcvr_status)
PMA_REMRXSTATUS.request (rem_rcvr_status)
PMA_SCRSTATUS.request (scr_status)
PMA_TXEN.request (tx_enable_mii)
PMA_RX_LPI_STATUS.request (rx_lpi_active)
PMA_TX_LPI_STATUS.request (tx_lpi_active)
PMA_LPI_STATUS.indication (loc_lpi)

146.2.1 PMA_LINK.request

This primitive allows the Auto-Negotiation or the PHY Link Synchronization algorithm to enable and disable operation of the PMA, as specified in 98.4.2.

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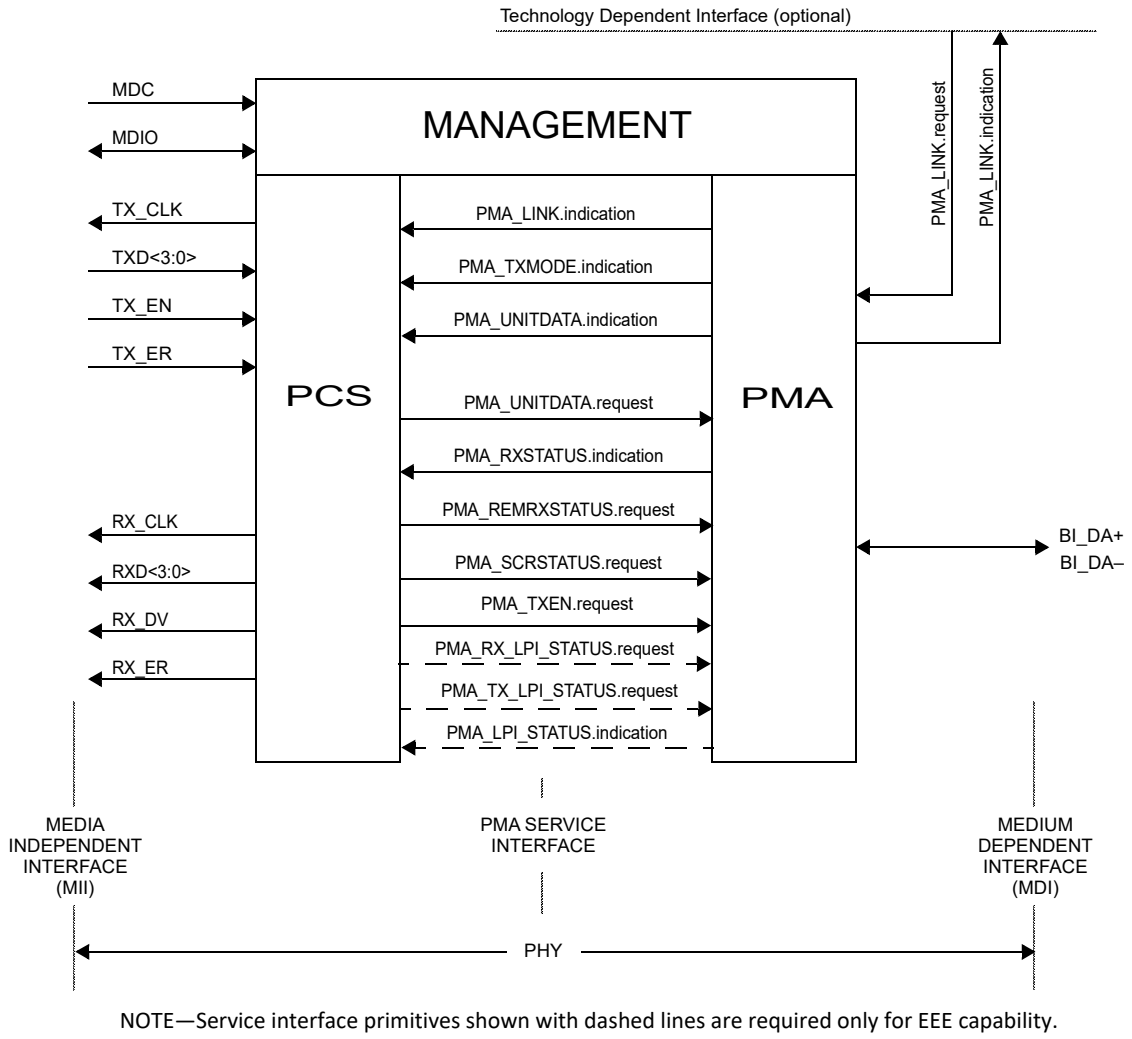

NOTE—Service interface primitives shown with dashed lines are required only for EEE capability.

Figure 146–2—10BASE-T1L PHY interfaces

146.2.1.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of the following two values:

DISABLE:	Used by the Auto-Negotiation function to disable the PHY.
ENABLE:	Used by the Auto-Negotiation function to enable the PHY.

146.2.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in 98.4.

146.2.1.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in 146.4.4 and the PMA Link Monitor function as described in 146.4.5.

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146.2.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 98.4.1. This primitive informs the Auto-Negotiation functions about the status of the underlying link.

146.2.2.1 Semantics of the primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on the following two values:

FAIL	No valid link established.
OK	The Link Monitor function indicates that a valid 10BASE-T1L link is established. Reliable reception of signals transmitted from the remote PHY is possible.

146.2.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 146–18.

146.2.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 98.4.1.

146.2.3 PMA_TXMODE.indication

The transmitter in a 10BASE-T1L link normally sends symbols over the MDI that represent an MII data stream with framing, scrambling and encoding of data, control information, or idles.

146.2.3.1 Semantics of the primitive

PMA_TXMODE.indication (tx_mode)

The PMA_TXMODE.indication specifies to PCS Transmit, via the parameter tx_mode, what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following three values of the form:

SEND_N	This value is continuously asserted during transmission of sequences of symbols representing an MII data stream in the data mode.
SEND_I	This value is continuously asserted when transmission of sequences of idle symbols is to take place.
SEND_Z	This value is continuously asserted when transmission of sequences of zeros is required.

146.2.3.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

146.2.3.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 146.3.3.

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146.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb_vector parameter from the PMA to the PCS.

146.2.4.1 Semantics of the primitive

PMA_UNITDATA.indication (rx_symb_vector)

During reception, the PMA_UNITDATA.indication conveys to the PCS, via the parameter rx_symb_vector, the value of symbols detected on the MDI during each cycle of the recovered clock.

146.2.4.2 When generated

The PMA generates PMA_UNITDATA.indication (rx_symb_vector) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is 7.5 MHz, as governed by the recovered clock.

146.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

146.2.5 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb_vector parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 146.3.3 to represent MII data, idle data, or zero data.

146.2.5.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA, via the parameter tx_symb_vector, the value of the symbols to be sent over the MDI. The tx_symb_vector may take on one of the values in the set {–1, 0, +1}.

146.2.5.2 When generated

The PCS generates PMA_UNITDATA.request (tx_symb_vector) synchronously with every transmit clock cycle.

146.2.5.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols after processing with optional transmit filtering and other specified PMA Transmit processing.

146.2.6 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Receive and PMA PHY Control function the information on whether the status of the overall receive link is satisfactory or not. The criterion for setting the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting disparity errors during reception of the symbol stream.

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146.2.6.1 Semantics of the primitive

PMA_RXSTATUS.indication (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the following form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

146.2.6.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

146.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 146.3.3.4.3 and 146.3.4.

146.2.7 PMA_REMRXSTATUS.request

This primitive is generated by PMA Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received within the idle data stream of the remote PHY.

146.2.7.1 Semantics of the primitive

PMA_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the following form:

OK	The receive link of the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

146.2.7.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages to indicate a change in rem_rcvr_status based on the PCS decoding the loc_rcvr_status bit in the idle data received from the remote PHY.

146.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in 146.4.4.

146.2.8 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the descrambler has achieved synchronization.

146.2.8.1 Semantics of the primitive

PMA_SCRSTATUS.request (scr_status)

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The scr_status parameter can take on one of two values of the following form:

OK	The descrambler has achieved synchronization.
NOT_OK	The descrambler is not synchronized.

146.2.8.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

146.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 146–15.

146.2.9 PMA_TXEN.request (tx_enable_mii)

This primitive is generated by PCS Data Transmission Enable function to communicate the status of the tx_enable_mii signal to the PMA. The parameter tx_enable_mii conveys to the PMA PHY Control function the information about the actual data transmission status.

146.2.9.1 Semantics of the primitive

PMA_TXEN.request (tx_enable_mii)

The tx_enable_mii parameter can take on one of two values of the following form:

TRUE	Transmission is enabled.
FALSE	Transmission is disabled.

146.2.9.2 When generated

PCS Data Transmission Enable function generates PMA_TXEN.request messages to indicate a change in tx_enable_mii variable.

146.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 146–15.

146.2.10 PMA_RX_LPI_STATUS.request (rx_lpi_active)

When the PHY supports the EEE capability, this primitive is generated by the PCS receive function to indicate the status of the receive link of the local PHY. The parameter PMA_RX_LPI_STATUS.request conveys to the PMA receive function and the PMA PHY control function information regarding whether the PCS receive function is in the LPI receive mode.

146.2.10.1 Semantics of the primitive

PMA_RX_LPI_STATUS.request (rx_lpi_active)

The rx_lpi_active parameter can take on one of two values of the following form:

TRUE	The PCS receive function is in the LPI receive mode.
FALSE	The PCS receive function is not in the LPI receive mode.

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146.2.10.2 When generated

The PCS generates PMA_RX_LPI_STATUS.request messages to indicate a change in the rx_lpi_active variable as described in Figure 146–9 and Figure 146–10.

146.2.10.3 Effect of receipt

The receiver may adjust the clock recovery while being in low power idle mode. Additionally, checking of the descrambler status in the PHY control state diagram is suppressed, as the receiver is disabled.

146.2.11 PMA_TX_LPI_STATUS.request (tx_lpi_active)

When the PHY supports the EEE capability, this primitive is generated by the PCS transmit function to indicate the status of "Assert Low Power Idle" on the MII. The parameter PMA_TX_LPI_STATUS.request conveys to the PMA control function information regarding whether the PCS transmit function is receiving "Assert Low Power Idle" on the MII.

146.2.11.1 Semantics of the primitive

PMA_TX_LPI_STATUS.request (tx_lpi_active)

The tx_lpi_active parameter can take on one of two values of the following form:

TRUE	The PCS transmit function is receiving "Assert Low Power Idle" on the MII.
FALSE	The PCS transmit function is not receiving "Assert Low Power Idle" on the MII.

146.2.11.2 When generated

The PCS generates PMA_TX_LPI_STATUS.request messages to indicate a change in the tx_lpi_active variable to the PMA PHY control function. Tx_lpi_active is set to true if "Assert Low Power Idle" is received from the MII; otherwise, it is set to false.

146.2.11.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 146–15 and Figure 146–17.

146.2.12 PMA_TX_LPI_STATUS.indication

When the PHY supports the EEE capability, this primitive is generated by the PMA PHY control function to indicate a sleep or wake event. The parameter PMA_TX_LPI_STATUS.indication conveys to the PCS transmit function information regarding whether the PHY should indicate a sleep or a wake event to the remote PHY.

146.2.12.1 Semantics of the primitive

PMA_TX_LPI_STATUS.indication (loc_lpi)

The loc_lpi parameter can take on one of two values of the following form:

TRUE	Communicate to the remote PHY that LPI mode will be entered by the local PHY.
FALSE	Communicate to the remote PHY that normal IDLE mode will be entered by the local PHY.

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146.2.12.2 When generated

The PMA generates PMA_TX_LPI_STATUS.indication messages to indicate a change in the loc_lpi variable.

146.2.12.3 Effect of receipt

The effect of receipt of this primitive is specified in 146.3.3.4.3.

146.3 Physical Coding Sublayer (PCS) functions

The Physical Coding Sublayer (PCS) consists of PCS Reset, the PCS Data Transmission Enable, PCS Transmit, and PCS Receive functions as shown in Figure 146–3. The PCS Reset function is explained in 146.3.1, the PCS Data Transmission Enable function is explained in 146.3.2, the PCS Transmit function is explained in 146.3.3, the PCS Receive function is explained in 146.3.4, and the PCS Loopback function is explained in 146.3.5.

146.3.1 PCS Reset function

PCS reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

PCS Reset shall set pcs_reset = TRUE while any of the above reset conditions holds true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

146.3.2 PCS Data Transmission Enable

The PCS Data Transmission Enable function shall conform to the PCS data transmission enabling state diagram in Figure 146–4. When tx_mode is equal to SEND_N, the signals tx_enable_mii and tx_error_mii are equal to the values of the MII signals TX_EN and TX_ER respectively; otherwise, tx_enable_mii and tx_error_mii are set to the value FALSE.

146.3.2.1 Variables

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: TRUE or FALSE

tx_enable_mii
: The tx_enable_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 146–4. When this variable is set to FALSE transmission is disabled, when set to TRUE transmission is enabled.
Values: TRUE or FALSE

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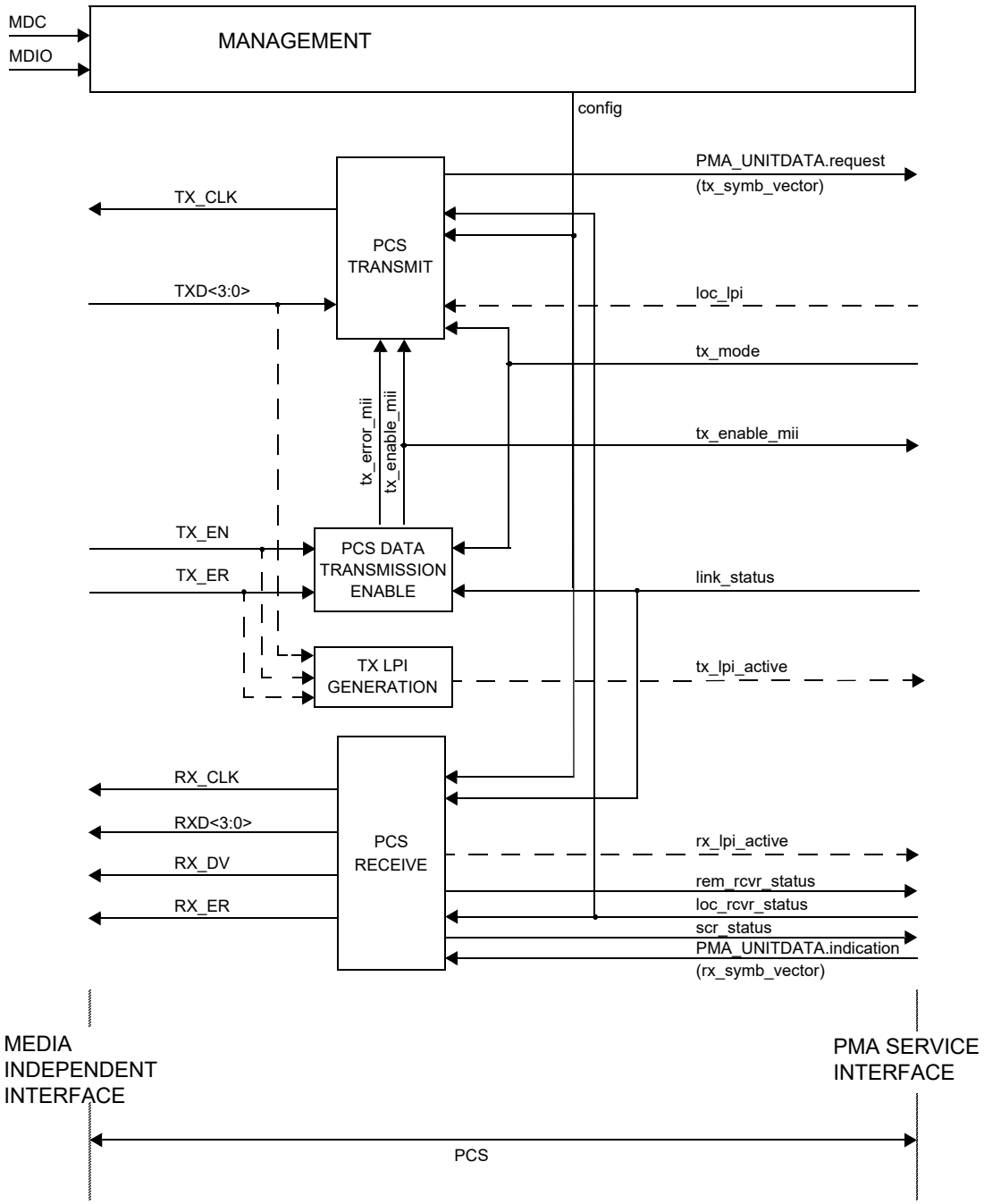

NOTE—Signals shown with dashed lines are required only for EEE capability.

Figure 146–3—PCS reference diagram

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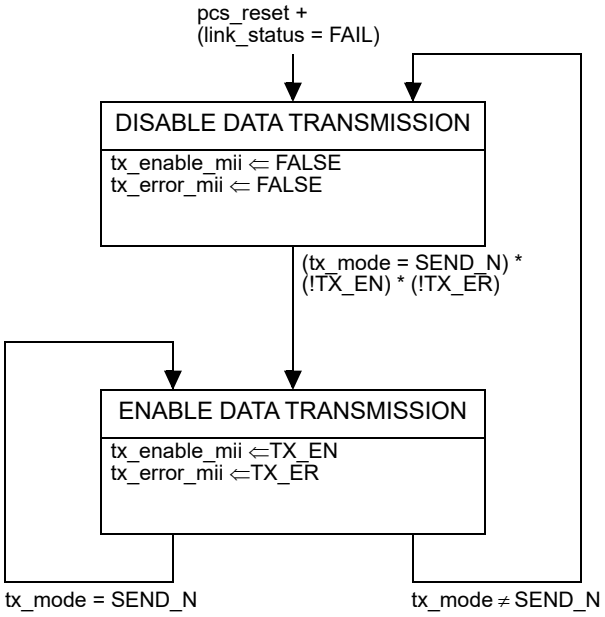

Figure 146–4—PCS data transmission enabling state diagram

tx_error_mii
: The tx_error_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 146–4.When this variable is set to FALSE it indicates a non-errored transmission, when set to TRUE it indicates an errored transmission.
Values: TRUE or FALSE

TX_EN
: The TX_EN signal of the MII as specified in 22.2.2.3.

TX_ER
: The TX_ER signal of the MII as specified in 22.2.2.5.

tx_mode
: The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

146.3.3 PCS Transmit

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 146–5 (see 146.3.3.1.6) and the PCS Transmit multiplexer state diagram in Figure 146–6 (see 146.3.3.2.4) and to the associated state variables, functions, timers, and messages.

146.3.3.1 PCS Transmit state diagram

Upon the assertion of TX_EN, the PCS Transmit state diagram passes an SSD of 4 code-groups to the PMA, which replaces the first 2 bytes of the preamble. Following SSD, TXD[3:0] is encoded into ternary symbols using encoding rules, specified in 146.3.3.5.1, until TX_EN is de-asserted.

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Following the de-assertion of TX_EN, a special code ESD (or ERR_ESD when a transmit error is encountered, which means that TX_ER was high at any point during the transmission) of 4 code-groups is generated, after which the transmission of idle mode according to 146.3.3.5.1 is resumed.

10BASE-T1L has one special code-group {0, 0, 0} that is not used by Idle or Data symbols. This code-group is used for the COMMA symbols within the delimiters. See Figure 146–5 for more details.

The 10BASE-T1L PHY supports normal operation and link training operation. In training operation, the PCS ignores signals from the MII and sends only the idle signals to the PMA until the training process is complete.

If tx_mode has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA.

If tx_mode has the value SEND_I, PCS Transmit generates sequences of symbols according to the encoding rule in idle mode as described in 146.3.3.5.1.

If tx_mode has the value SEND_N, PCS Transmit generates symbols A_n at each symbol period representing data, special control symbols like SSD/ESD, or IDLE symbols as defined in 146.3.3.5.1. The transition from idle to data is signaled by an SSD and the end of transmission of data is signaled by an ESD.

During training operation (when tx_mode is SEND_I), knowledge of the transmitted symbols may be used at the receiver side to perform any signal conditioning necessary for meeting the required performance during normal operation. When the link is up, the PHY enters SEND_N mode and the transmitted PAM3 symbols are used at the receiver PHY for continued clock frequency/phase tracking.

146.3.3.1.1 Variables

error
: PCS local variable that records if an errored transmission has occured during data transmission.
Values: TRUE or FALSE

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: TRUE or FALSE

tx_enable_mii
: The tx_enable_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 146–4. When this variable is set to FALSE transmission is disabled, when set to TRUE transmission is enabled.
Values: TRUE or FALSE

tx_error_mii
: The tx_error_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 146–4.When this variable is set to FALSE it indicates a non-errored transmission, when set to TRUE it indicates an errored transmission.
Values: TRUE or FALSE

tx_mode
: The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

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loc_rcvr_status

The loc_rcvr_status parameter set by the PMA Receive function and passed to the PCS via the PMA_RXSTATUS.indication primitive.
Values: OK or NOT_OK

loc_lpi

The variable loc_lpi is set by the PHY Control function in the PMA to indicate that it has entered low power idle mode.
Values: TRUE or FALSE

$Sy_n[4:0]$

The $Sy_n[4:0]$ bits from the scrambler as defined in 146.3.3.4.2.

$Sd_n[3:0]$

The $Sd_n[3:0]$ signal of the scrambler output as defined in 146.3.3.4.3.

Tx_n

Alias for tx_symb_vector at time n.

tx_code_group $\{TA_n, TB_n, TC_n\}$

A triplet of ternary symbols generated by the PCS Transmit state diagram. These include 4B3T encoded data and assigned values (see 146.3.3.5). The element TA_n is the first ternary symbol transmitted; TC_n is the last ternary symbol transmitted.
Value: A triplet of ternary transmit symbols. Each of the ternary symbols may take on one of the values {–1, 0, +1}.

tx_disparity

PCS local variable containing the running disparity. After PCS Reset, the initial value shall be set to 2.
Values: 1 to 4, depending on running disparity.

146.3.3.1.2 Functions

ENCODE

In the PCS Transmit process, this function takes as its arguments $Sd_n[3:0]$ and the tx_disparity and returns the corresponding tx_code_group as well as the updated tx_disparity. ENCODE follows the 4B3T rules defined in 146.3.3.5.1.

$$\{tx\_code\_group, tx\_disparity\} = ENCODE(Sd_n[3:0], tx\_disparity)$$

The tx_disparity can be between 1 and 4 and the respective tx_code_group is taken from the 4B3T encoding rules defined in Table 146–1 based on the $Sd_n[3:0]$ value and the tx_disparity:

$$tx\_code\_group = table_{4B3T}(Sd_n[3:0], tx\_disparity)$$

The second output value of this function is an updated tx_disparity value, which is calculated in the following way:

$$tx\_disparity = tx\_disparity + disparity\ of\ currently\ encoded\ tx\_code\_group$$

DISPRES

The function DISPRES returns one of the eight possible DISPRESET3 values for tx_code_group (see Table 146–2), depending on the values of $Sy_n[4]$ and tx_disparity:

$$tx\_code\_group = table_{DISPRESET3}(Sy_n[4], tx\_disparity)$$

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RND_SSD4

The function RND_SSD4 takes $Sy_{n-1}[4]$ as its argument and returns the corresponding tx_code_group as well as the updated tx_disparity.

{tx_code_group, tx_disparity} = RND_SSD4($Sy_{n-1}[4]$)

The returned tx_code_group corresponds to one of the two possible SSD4 code-groups (see Table 146–3), depending on the value of $Sy_{n-1}[4]$:

tx_code_group = $table_{SSD4}(Sy_{n-1}[4])$

The returned tx_disparity also depends on the value of $Sy_{n-1}[4]$ as follows:

tx_disparity = *2, if $Sy_{n-1}[4] = 0$*
3, otherwise

RND_ESD4

The function RND_ESD4 takes $Sy_{n-1}[4]$ as its argument and returns the corresponding tx_code_group as well as the updated tx_disparity.

{tx_code_group, tx_disparity} = RND_ESD4($Sy_{n-1}[4]$)

The returned tx_code_group corresponds to one of the two possible ESD4 code-groups (see Table 146–3), depending on the value of $Sy_{n-1}[4]$:

tx_code_group = $table_{ESD4}(Sy_{n-1}[4])$

The returned tx_disparity also depends on the value of $Sy_{n-1}[4]$ as follows:

tx_disparity = *2, if $Sy_{n-1}[4] = 0$*
3, otherwise

RND_ESD_ERR4

The function RND_ESD_ERR4 takes $Sy_{n-1}[4]$ as its argument and returns the corresponding tx_code_group as well as the updated tx_disparity.

{tx_code_group, tx_disparity} = RND_ESD_ERR4($Sy_{n-1}[4]$)

The returned tx_code_group corresponds to one of the two possible ESD_ERR4 code-groups (see Table 146–3), depending on the value of $Sy_{n-1}[4]$:

tx_code_group = $table_{ESD\_ERR4}(Sy_{n-1}[4])$

The returned tx_disparity also depends on the value of $Sy_{n-1}[4]$ as follows:

tx_disparity = *2, if $Sy_{n-1}[4] = 0$*
3, otherwise

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146.3.3.1.3 Timers

symb_triplet_timer
: A continuous free-running timer that shall expire synchronously with every third expiration of symb_timer. TX_CLK (see 22.2.2.1) shall be generated from symb_triplet_timer with the rising edge of TX_CLK generated synchronously with symb_triplet_timer_done.
Restart time: Immediately after expiration; restarting the timer resets the condition symb_triplet_timer_done.
Duration: Three symbol times (see 146.5.4.5)

146.3.3.1.4 Abbreviations

STD
: Alias for symb_triplet_timer_done.

146.3.3.1.5 Constants

COMMA
: A vector of three ternary symbols in the first or second code-group of any delimiter as specified in 146.3.3.5.1.

ZERO
: A vector of three zero symbols sent when tx_mode = SEND_Z as specified in 146.3.3.5.2.

146.3.3.1.6 State diagram

146.3.3.2 PCS Transmit multiplexer state diagram

In each symbol period, the PCS Transmit multiplexer generates a ternary symbol that can take the values of {–1, 0, +1} and passes it to the PMA sublayer via the PMA_UNITDATA.request primitive. The nominal symbol clock frequency is specified in 146.5.4.5.

146.3.3.2.1 Variables

pcs_reset
: The pcs_reset parameter set by the PCS reset function.
Values: TRUE or FALSE

tx_symb_vector
: A ternary symbol generated through serialization of tx_code_group. This symbol is conveyed to the PMA as the parameter of a PMA_UNITDATA.request(tx_symb_vector) service primitive.
Values: A ternary transmit symbol. The ternary symbol may take on one of the values {–1, 0, +1}.

tx_code_group {TA_n, TB_n, TC_n}
: A triplet of ternary symbols generated by the PCS Transmit state diagram. The element TA_n is the first ternary symbol transmitted; TC_n is the last ternary symbol transmitted.
Value: A triplet of ternary transmit symbols. Each of the ternary symbols may take on one of the values {–1, 0, +1}.

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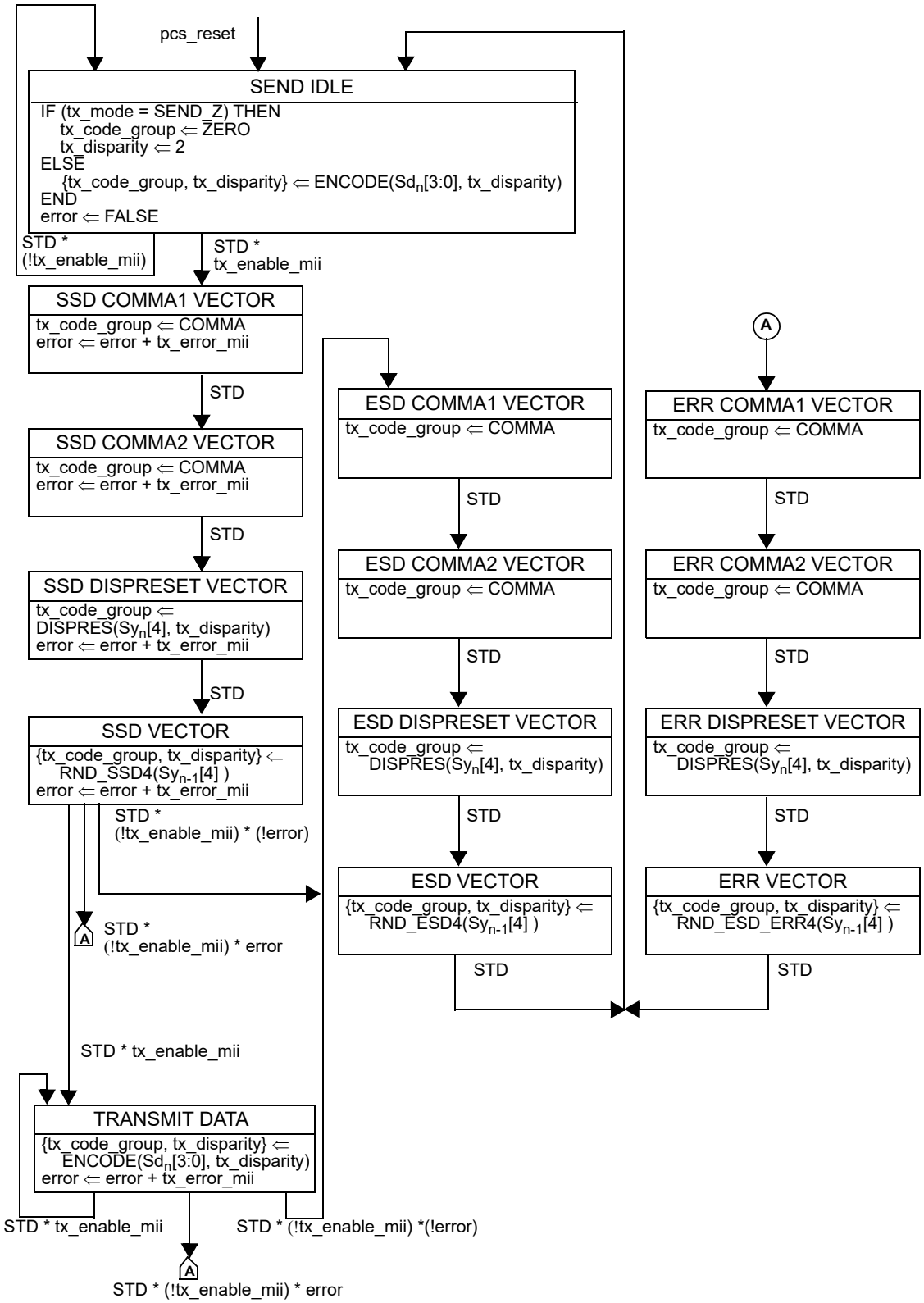

Figure 146–5—PCS Transmit state diagram

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146.3.3.2.2 Timers

symb_timer

A continuous free-running timer. The symb_timer expires when the PMA_UNITDATA.request is serviced, synchronously with TX_TCLK.
Continuous timer: The condition symb_timer_done becomes true upon timer expiration.
Restart time: Immediately after expiration; restarting the timer resets the condition symb_timer_done.
Duration: One symbol time (see 146.5.4.5)

146.3.3.2.3 Abbreviations

PUDR

Alias for PMA_UNITDATA.request(tx_symb_vector).

146.3.3.2.4 State diagram

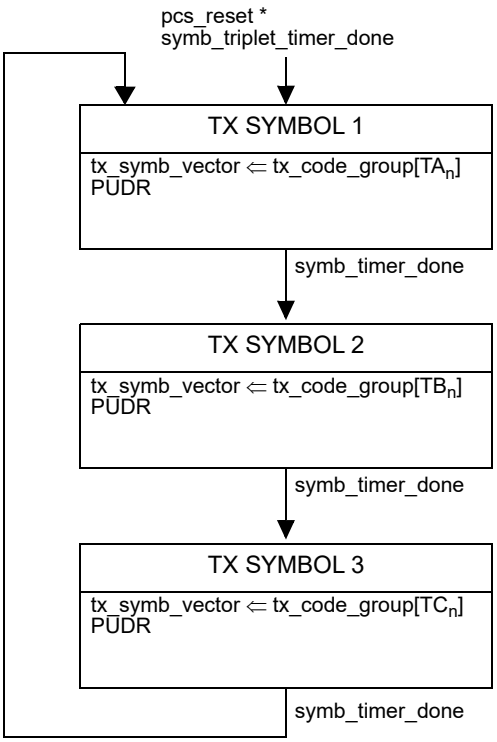

Figure 146–6—TX multiplexer state diagram

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146.3.3.3 PCS Transmit symbol generation

The reference diagram of transmit symbol generation is indicated in Figure 146–7. The tx_code_group is the code-group $\{TA_n, TB_n, TC_n\}$.

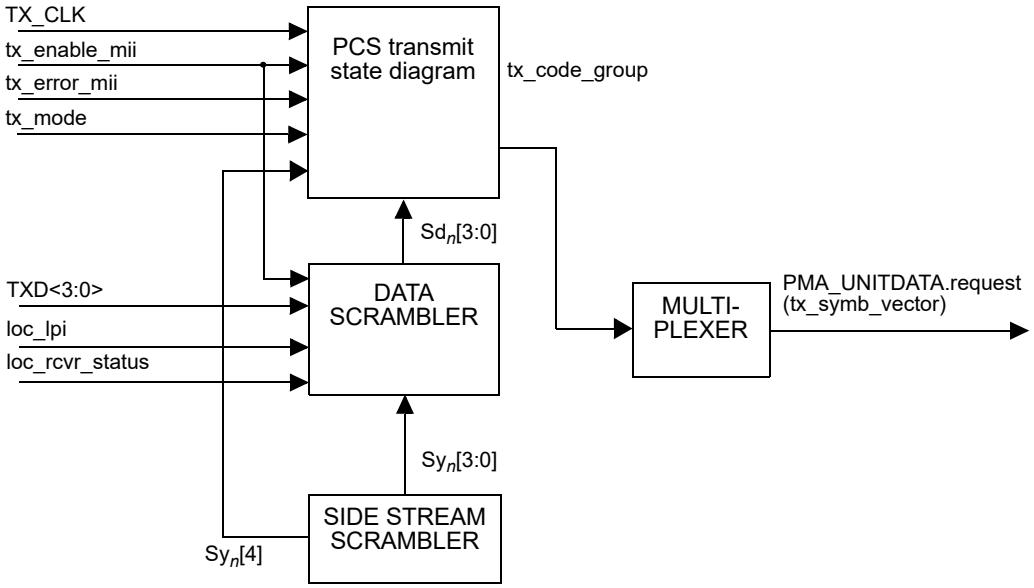

Figure 146–7—PCS transmit symbol generation

146.3.3.4 Data and idle stream scrambling

The scrambled bits $Sd_n[3:0]$ used by the ENCODE function defined in 146.3.3.1.2 are generated as follows.

146.3.3.4.1 Side-stream scrambler polynomial

The PCS Transmit function shall employ side-stream scrambling. For the master PHY, PCS Transmit shall employ

$$g_m(x) = 1 + x^{13} + x^{33} \tag{146–1}$$

as transmitter side-stream scrambler generator polynomial. For the slave PHY, PCS Transmit shall employ

$$g_s(x) = 1 + x^{20} + x^{33} \tag{146–2}$$

as transmitter side-stream scrambler generator polynomial. An implementation of master and slave PHY side-stream generator polynomials by linear-feedback shift registers is shown in Figure 146–8. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each tx_code_group period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. The scrambler state shall not be initialized to all zeros.

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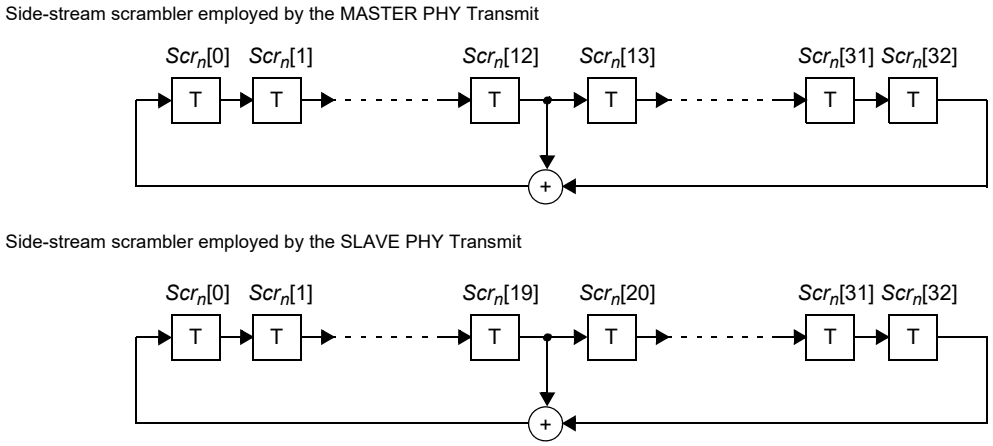

Figure 146–8—A realization of side-stream scramblers by linear feedback shift registers

146.3.3.4.2 Generation of $Sy_n[3:0]$

PCS Transmit encoding rules are based on the generation, at time n, of the five bits $Sy_n[4:0]$. The four bits $Sy_n[3:0]$ are used for de-correlating the MII data word TXD<3:0> during data transmission and for generating the idle symbols. The bit $Sy_n[4]$ is used to randomize the frame delimiters. These five bits are generated as described below, using the auxiliary generating polynomial, g(x) defined in Equation (146–3):

$$g(x) = x^3 \wedge x^8 \tag{146–3}$$

The five bits $Sy_n[4:0]$ shall be generated using the bit $Scr_n[0]$ and $g(x)$ as in the following equations:

$$Sy_n[0] = Scr_n[0]$$
$$Sy_n[1] = g(Scr_n[0]) = Scr_n[3] \wedge Scr_n[8]$$
$$Sy_n[2] = g^2(Scr_n[0]) = Scr_n[6] \wedge Scr_n[16]$$
$$Sy_n[3] = g^3(Scr_n[0]) = Scr_n[9] \wedge Scr_n[14] \wedge Scr_n[19] \wedge Scr_n[24].$$
$$Sy_n[4] = g^4(Scr_n[0]) = Scr_n[12] \wedge Scr_n[32]$$

By construction, the five bits $Sy_n[4:0]$ are derived from elements of the same maximum-length shift register sequence of length $2^{33}–1$ as $Scr_n[0]$, but shifted in time by varying delays. The associated delays are all large and different so that there is no apparent correlation among the bits.

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146.3.3.4.3 Generation of scrambled bits $Sd_n[3:0]$

From scrambler bits $Sy_n[3:0]$ and $TXD_n[3:0]$, bits $Sd_n[3:0]$ shall be generated as follows:

$$Sd_n[3] = \begin{cases} Sy_n[3] \wedge TXD_n[3] & \text{if (tx\_enable\_mii = TRUE)} \\ Sy_n[3] \wedge 1 & \text{else if (loc\_rcvr\_status = OK)} \\ Sy_n[3] & \text{else} \end{cases}$$

$$Sd_n[2] = \begin{cases} Sy_n[2] \wedge TXD_n[2] & \text{if (tx\_enable\_mii = TRUE)} \\ Sy_n[1] \wedge 1 & \text{else if (loc\_lpi = TRUE)} \\ Sy_n[1] & \text{else} \end{cases}$$

$$Sd_n[1:0] = \begin{cases} Sy_n[1:0] \wedge TXD_n[1:0] & \text{if (tx\_enable\_mii = TRUE)} \\ (Sy_n[2], Sy_n[0]) & \text{else} \end{cases}$$

Note that during transmission of idles, bits $Sy_n[1]$ and $Sy_n[2]$ shall be swapped, compared to data transmission, to reliably distinguish idle data transmission from data transmission at the receiver side.

146.3.3.5 Generation of code-groups

The PCS transmit state diagram generates code-groups as follows. A code-group $\{TA_n, TB_n, TC_n\}$ is sent in the following order: TA_n, TB_n, TC_n, TA_{n+1}, TB_{n+1}, TC_{n+1}, ...

146.3.3.5.1 Generation of code-groups in mode SEND_N and SEND_I

Both SEND_I and SEND_N use the following ternary symbol encoding. The scrambled bits $Sd_n[3:0]$ are converted to a code-group $\{TA_n, TB_n, TC_n\}$ using the 4B3T algorithm in conjunction with a running disparity value, shown in Table 146–1. The 4B3T coding is DC-free. To achieve this, the difference between the number of transmitted “+1” and “–1” symbols is limited. The running disparity reflects this difference and is used to choose the coding of the next symbol.

The code-group {0, 0, 0} is used as the COMMA value and never occurs during normal 4B3T mapping. This can also be used to synchronize the receiver’s demultiplexer code-group boundary during training.

The DISPRESET3 code-group, together with the following fourth code-group, is used to bring back the running disparity to a defined value of either 2 or 3, depending on the value of bit $Sy_n[4]$ from the scrambler. The coding shown in Table 146–2 is used for the DISPRESET3 code-group.

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Table 146–1—4B3T encoding

$Sd_n[3:0]$	Disparity = 1 $\{TA_n, TB_n, TC_n\}$		Disparity = 2 $\{TA_n, TB_n, TC_n\}$		Disparity = 3 $\{TA_n, TB_n, TC_n\}$		Disparity = 4 $\{TA_n, TB_n, TC_n\}$	
	Code-Group[1]	Disparity Change	Code-Group	Disparity Change	Code-Group	Disparity Change	Code-Group	Disparity Change
0000	+ 0 +	2	0 – 0	–1	0 – 0	–1	0 – 0	–1
0001	0 – +	0	0 – +	0	0 – +	0	0 – +	0
0010	+ – 0	0	+ – 0	0	+ – 0	0	+ – 0	0
0011	0 0 +	1	0 0 +	1	0 0 +	1	– – 0	–2
0100	– + 0	0	– + 0	0	– + 0	0	– + 0	0
0101	0 + +	2	– 0 0	–1	– 0 0	–1	– 0 0	–1
0110	– + +	1	– + +	1	– – +	–1	– – +	–1
0111	– 0 +	0	– 0 +	0	– 0 +	0	– 0 +	0
1000	+ 0 0	1	+ 0 0	1	+ 0 0	1	0 – –	–2
1001	+ – +	1	+ – +	1	+ – +	1	– – –	–3
1010	+ + –	1	+ + –	1	+ – –	–1	+ – –	–1
1011	+ 0 –	0	+ 0 –	0	+ 0 –	0	+ 0 –	0
1100	+ + +	3	– + –	–1	– + –	–1	– + –	–1
1101	0 + 0	1	0 + 0	1	0 + 0	1	– 0 –	–2
1110	0 + –	0	0 + –	0	0 + –	0	0 + –	0
1111	+ + 0	2	0 0 –	–1	0 0 –	–1	0 0 –	–1

NOTE–The Code-Group is {TAn, TBn, TCn}.

[1]In Table 146–1 '–' is an abbreviation for the ternary symbol value '–1' and '+' is an abbreviation for the ternary symbol value '+1'.

Table 146–2—Disparity reset

DISPRESET3	Disparity = 1	Disparity = 2	Disparity = 3	Disparity = 4
$Sy_n[4] = 0$	{–1, 0, +1}	{–1, 0, 0}	{–1, 0, –1}	{–1, –1, –1}
$Sy_n[4] = 1$	{+1, +1, +1}	{+1, 0, +1}	{+1, 0, 0}	{+1, 0, –1}

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The fourth code-group (SSD4/ESD4/ESD_ERR4) is encoded as shown in Table 146–3:

Table 146–3—Delimiters

	Delimiter	$\{TA_n, TB_n, TC_n\}$
$Sy_{n-1}[4] = 0$	SSD4	{+1, +1, –1}
	ESD4	{+1, –1, +1}
	ESD_ERR4	{–1, +1, +1}
$Sy_{n-1}[4] = 1$	SSD4	{–1, –1, +1}
	ESD4	{–1, +1, –1}
	ESD_ERR4	{+1, –1, –1}

146.3.3.5.2 Generation of code-groups in mode SEND_Z

The code-group $\{TA_n, TB_n, TC_n\}$ is a zero vector {0, 0, 0} when tx_mode = SEND_Z.

146.3.4 PCS Receive

146.3.4.1 PCS Receive overview

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 146–9 and associated state variables.

The received code-group Rx_n, generated by PCS Receive at time n, is decoded using the inverse of the mapping shown in Table 146–1. The result of the decoding is $Sr_n[3:0]$.

The PCS Receive function shall conform to the Receive watchdog state diagram in Figure 146–11. This prevents the possible lock-up of the PCS Receive state diagram in the DATA state due to mis-detection of an ESD. The maximum dwelling time in DATA state shall be less than the period specified for rcv_max_timer. When rcv_max_timer expires, the PCS Receive state diagram is reset and transitions to IDLE.

In Figure 146–9, there are a total of five states after SSD4 detection before the DATA state; meanwhile, there are also five states before the IDLE state (including the DATA state) that perform data decoding. As a result, the depth of the data flush-in delay line is the same as the flush-out delay line ensuring correct packet reception at the MII. These delay lines are necessary to decode the stream delimiters prior to forwarding the received data to the MII interface.

The variables, functions, and timers used in Figure 146–9, Figure 146–10, and Figure 146–11 (in 146.3.4.1.5) are defined next. For the definition of IDLE, COMMA, DISPRESET3, SSD4, ESD4, and ESD_ERR4, see 146.3.3.5.1.

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146.3.4.1.1 Variables

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: TRUE or FALSE

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

receiving
: Generated by the PCS Receive function; if set as TRUE, it indicates that the PCS is in Data mode.
Values: TRUE or FALSE

loc_rcvr_status
: The loc_rcvr_status parameter set by the PMA Receive function and passed to the PCS via the PMA_RXSTATUS.indication primitive.
Values: OK or NOT_OK

lpi_enabled
: This variable indicates whether Energy Efficient Ethernet is enabled for the PHY or not. If Auto-Negotiation is enabled, lpi_enabled reflects whether both PHYs have EEE capability advertised. If Auto-Negotiation is not enabled, and MDIO is implemented, lpi_enabled reflects bit 1.2294.10 as described in 45.2.1.231.5.
Values: TRUE or FALSE

RX_ER
: The RX_ER signal of the MII as specified in 22.2.2.10.

RX_DV
: The RX_DV signal of the MII as specified in 22.2.2.7.

RXD[3:0]
: The RXD signal of the MII as specified in 22.2.2.8.

Rx_n
: Received code-group generated by PCS Receive at time n.

rx_lpi_active
: This variable indicates to the PMA receive function if the receive state diagram is in low power idle state.
Values: TRUE or FALSE

rx_symb_vector
: A vector of ternary symbols received by the PMA and passed to the PCS via the PMA_UNITDATA.indication primitive.
Value: single ternary symbol

rx_disparity
: PCS local variable containing the calculated running disparity at the receiver side. After PCS Reset, the initial value shall be set to 2.
Values: 1 to 4, depending on running disparity.

scr_status
: The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.
Values: OK: The descrambler has achieved synchronization.
NOT_OK: The descrambler is not synchronized.

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disparity_error

The disparity_error is set by the 4B3T decoder in the receiver, when a rx_code_group is received that is not allowed according to the running disparity calculated in the decoder.
Values: TRUE or FALSE

rcv_overrun_detected

Variable set as TRUE when in RECEIVE OVERRUN state as shown in Receive watchdog state diagram in Figure 146–11 and set FALSE otherwise.
Values: TRUE or FALSE

146.3.4.1.2 Functions

valid_idle

This function checks whether the decoded data bits $Sr_n[1:0]$ are equal to the expected $Sd_n[1:0]$ values from the local descrambler.
Values: TRUE or FALSE

check_idle

The check_idle function indicates a reliable detection of the idle data stream.
Values: TRUE or FALSE

rem_lpi

The rem_lpi function provides reliable detection of the received loc_lpi information from the remote PHY within the IDLE data stream.
Values: TRUE or FALSE

valid_dispreset

Determines if the received code-group is one of the DISPRESET3 code-groups as specified in 146.3.3.5.1. It returns a Boolean value indicating whether or not one of the eight possible DISPRESET3 code-groups has been received.
Values: TRUE or FALSE

valid_ssd4

Determines if the received code-group is one of the SSD4 code-groups as specified in 146.3.3.5.1. It returns a Boolean value indicating whether or not one of the two possible SSD4 code-groups has been received.
Values: TRUE or FALSE

valid_esd4

Determines if the received code-group is one of the ESD4 code-groups as specified in 146.3.3.5.1. It returns a Boolean value indicating whether or not one of the two possible ESD4 code-groups has been received.
Values: TRUE or FALSE

valid_esd_err4

Determines if the received code-group is one of the ESD_ERR4 code-groups as specified in 146.3.3.5.1. It returns a Boolean value indicating whether or not one of the two possible ESD_ERR4 code-groups has been received.
Values: TRUE or FALSE

DESCRAMBLE

This function takes as its arguments the value of Rx_n and returns the descrambler output according to 146.3.4.3.

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DECODE

In the PCS Receive process, this function takes as its arguments the value of the received code-group and rx_disparity and returns the corresponding RXD[3:0] as well as the updated rx_disparity. DECODE follows the rules outlined in 146.3.4.2 and the inverse encoding rules stated in Table 146–1.

$RXD[3:0] = DESCRAMBLE(inverse\_table_{4B3T}(Rx_n))$

$rx\_disparity = rx\_disparity + disparity\ of\ currently\ received\ Rx_n$

CHECK_DISP

The CHECK_DISP function checks if the currently received code-group is allowed for the current rx_disparity, and returns TRUE or FALSE according to the relation:

$Rx_n \neq table_{4B3T}(inverse\_table_{4B3T}(Rx_n), rx\_disparity).$

The encoding rules for the 4B3T encoding are stated in Table 146–1.

RESET_DISP

This function takes as its argument the value of Rx_n, corresponding to a valid SSD4 code-group, and returns the updated rx_disparity as follows:

$$rx\_disparity = \begin{cases} 2, & \text{if } Rx_n = \{+1, +1, -1\} \\ 3, & \text{otherwise} \end{cases}$$

146.3.4.1.3 Timers

RSTCD

Abbreviation for Receive Symbol Tripled Conversion Done, which is equivalent to the timer condition rcv_symb_triplet_timer_done.

rcv_max_timer

A timer used to determine the maximum amount of time the Receive watchdog state diagram stays in the RECEIVE state. The timer shall expire 4 ms ± 100 μs after being started. The condition rcv_max_timer_done becomes true upon timer expiration.

rcv_symb_triplet_timer

The rcv_symb_triplet_timer is a continuous free-running timer that shall expire with three times the period of the receive symbol clock synchronously to PMA_UNITDATA.indication. RX_CLK (see 22.2.2.2) shall be generated from rcv_symb_triplet_timer with the falling edge of RX_CLK generated synchronously with rcv_symb_triplet_timer_done. During initial link training, the phase of the rcv_symb_triplet_timer is aligned to the receive symbol clock as described in 146.3.4.2.

Continuous timer: The condition rcv_symb_triplet_timer_done becomes true upon timer expiration.

Restart time: Immediately after expiration.

Duration: Three symbol times (see 146.5.4.5)

146.3.4.1.4 Constants

COMMA

A vector of three ternary symbols in the first or second code-group of any delimiter as specified in 146.3.3.5.1.

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146.3.4.1.5 State diagrams

The PCS Receive state diagram is shown in Figure 146–9 and Figure 146–10 while the Receive watchdog state diagram is shown in Figure 146–11.

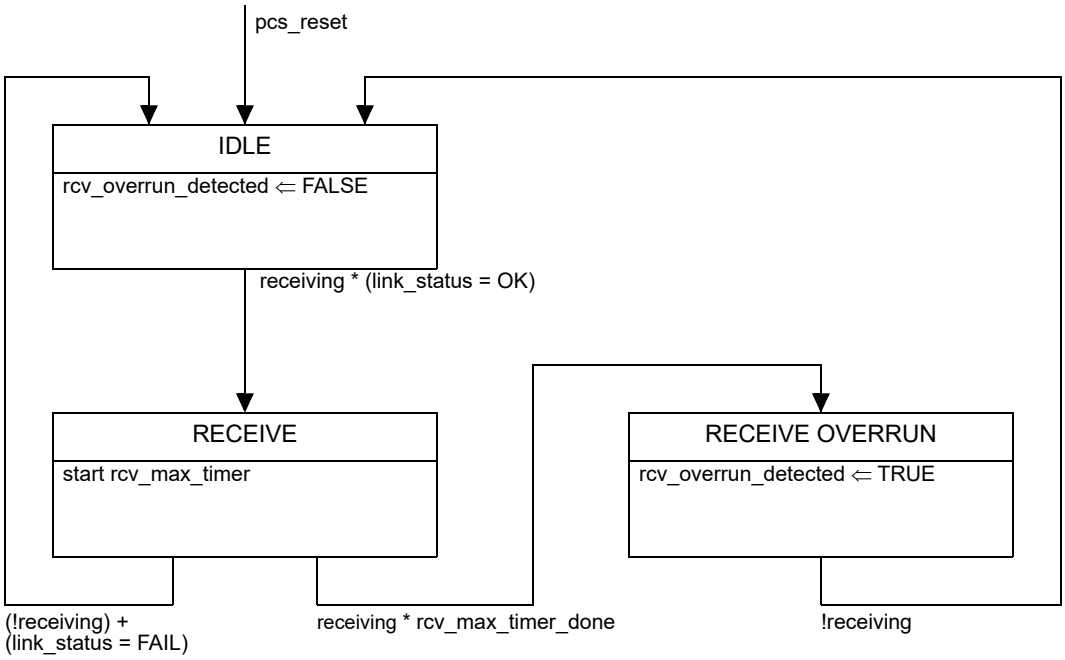

Figure 146–11—Receive watchdog state diagram

146.3.4.2 PCS Receive symbol decoding

When PMA Receive indicates normal operation and sets loc_rcvr_status = OK, the PCS Receive function checks the symbol sequences and searches for an SSD or a receive error indicator.

The received symbols, rx_symb_vector, are de-interleaved to generate received code-groups {RA_n, RB_n, RC_n}. To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode. The code-group {0, 0, 0} should never occur. The symbol synchronization in the de-interleaving block needs to be adjusted if the code-group {0, 0, 0} is being received. PCS Receive generates the sequence of symbols and indicates the reliable acquisition of the descrambler state by setting the parameter scr_status to OK. The descrambler can acquire synchronization during the PHY training.

The received code-groups {RA_n, RB_n, RC_n} are decoded to generate signals RXD[3:0], RX_DV, and RX_ER at the MII. The decoder shall also generate the disparity_error signal for the PCS Receive state diagram when a code-group is received that is not allowed according to the current running disparity value. Each time a code-group is received, the running disparity is updated. This is done using the current running disparity and adding the disparity change value as specified in Table 146–1 for the currently received code-group.

PCS Receive shall set RX_DV = TRUE when it receives an SSD, and shall set RX_DV = FALSE when it receives an ESD or ESD with error.

PCS Receive shall set RX_ER = TRUE when it receives bad ESDs, ERR_ESD, or bad SSDs. When the state diagram reaches the IDLE state, RX_ER shall be reset to FALSE.

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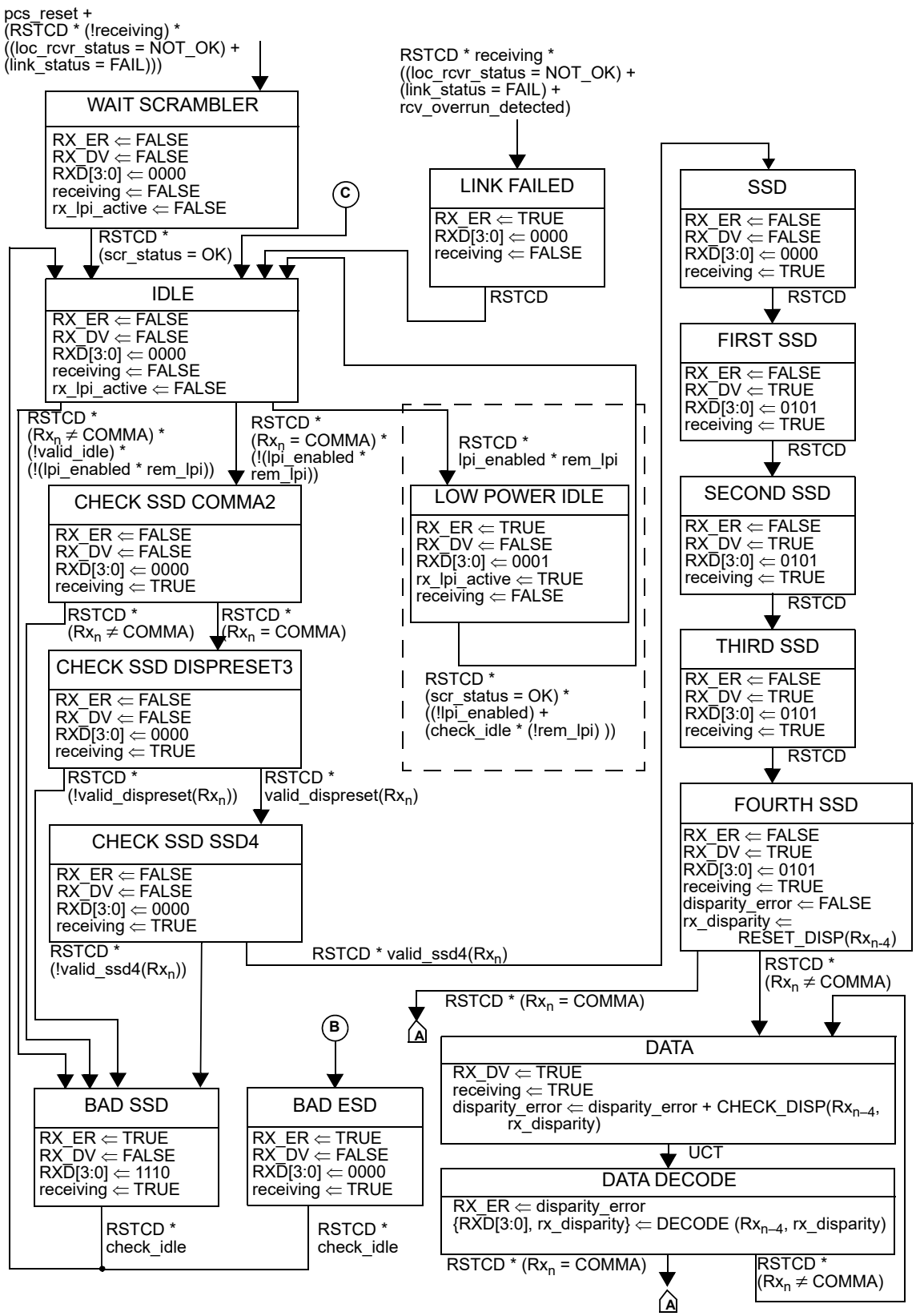

NOTE—Transitions inside dashed boxes are required only for the EEE capability.

Figure 146–9—PCS Receive state diagram, part a

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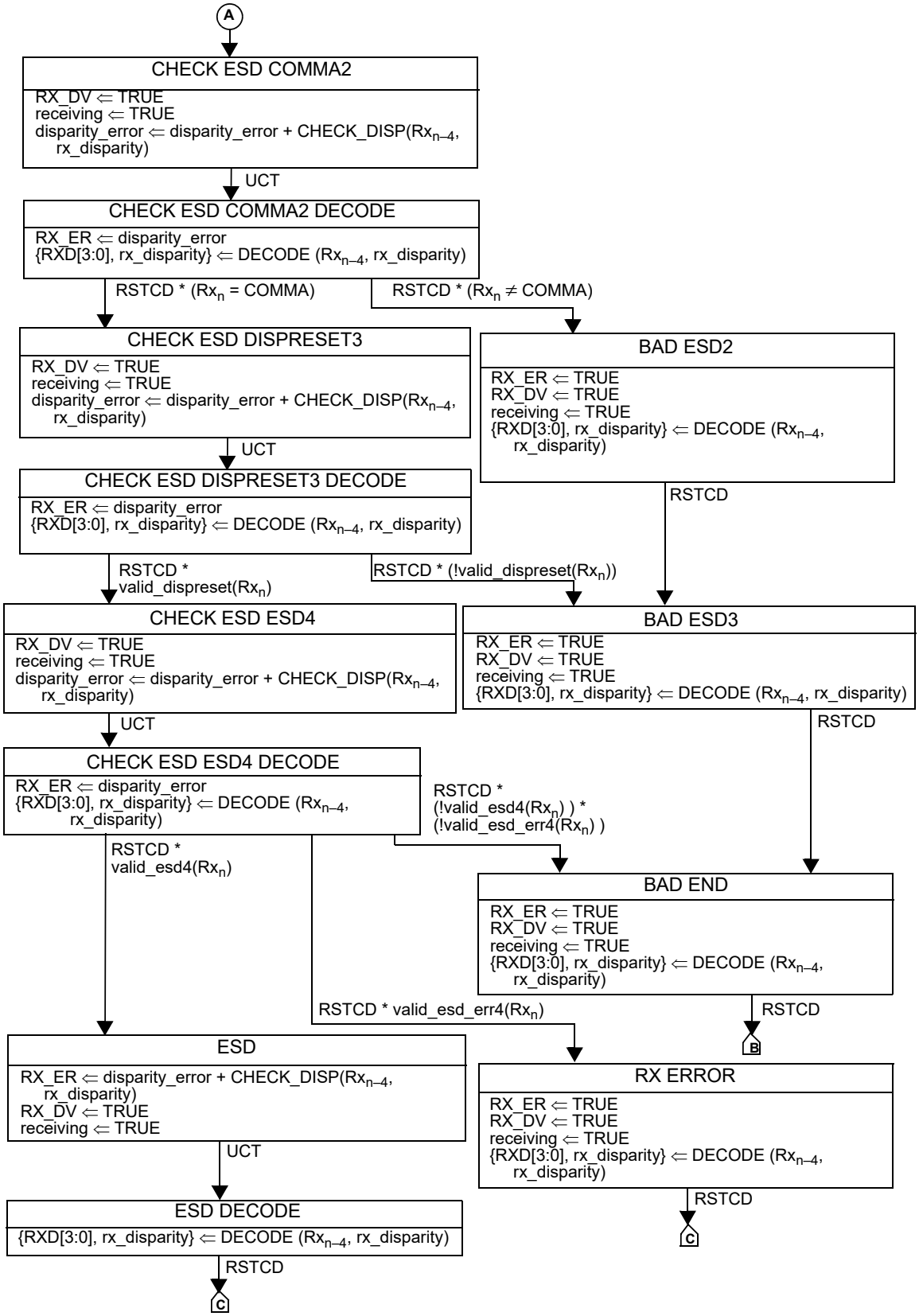

Figure 146–10—PCS Receive state diagram, part b

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146.3.4.3 PCS Receive descrambler polynomial

The PHY decodes the code-groups and returns the proper bit stream to the descrambling process for generation of RXD<3:0> to the MII. For side-stream descrambling, the MASTER PHY shall employ the following receiver descrambler generator polynomial:

$$g'_M(x) = 1 + x^{20} + x^{33} \quad (146–4)$$

and the SLAVE PHY shall employ the following receiver descrambler generator polynomial:

$$g'_S(x) = 1 + x^{13} + x^{33} \quad (146–5)$$

146.3.4.4 PCS Receive automatic polarity detection

An automatic polarity detection and correction shall be implemented on the receive side of both master and slave PHY.

Polarity can be automatically detected in a recursive process: one assumption of polarity is made first and the descrambler synchronization is monitored within a certain period to determine whether such an assumption is correct; if not, the same procedure is repeated with a different polarity assumption and vice versa.

Receive polarity detection and correction can be done simultaneously at the earliest link up stages. Link up starts with the MASTER PHY sending symbols to the SLAVE PHY. If a polarity flip is detected, the SLAVE changes the sign of its received signals $\{RA_n, RB_n, RC_n\}$ to correct the polarity. There is no change in the polarity of the transmit signal. After the SLAVE PHY has started transmission, the MASTER PHY can use the same method for determining its receive polarity.

146.3.5 PCS loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, or the loopback bit in MDIO register 3.2278.14, defined in 45.2.3.70.2, is set to one (or by a similar functionality if MDIO is not implemented). In this mode, the PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium.

NOTE—The signal path through the PCS that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompasses as much of the PCS circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function testing the transmit and receive data paths.

146.4 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PMA service interface specified in 146.3 onto the 10BASE-T1L physical medium, and provides the link management and PHY Control functions. The PMA provides full duplex communications to and from medium employing 3-level Pulse Amplitude Modulation (PAM3). The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 146.8.

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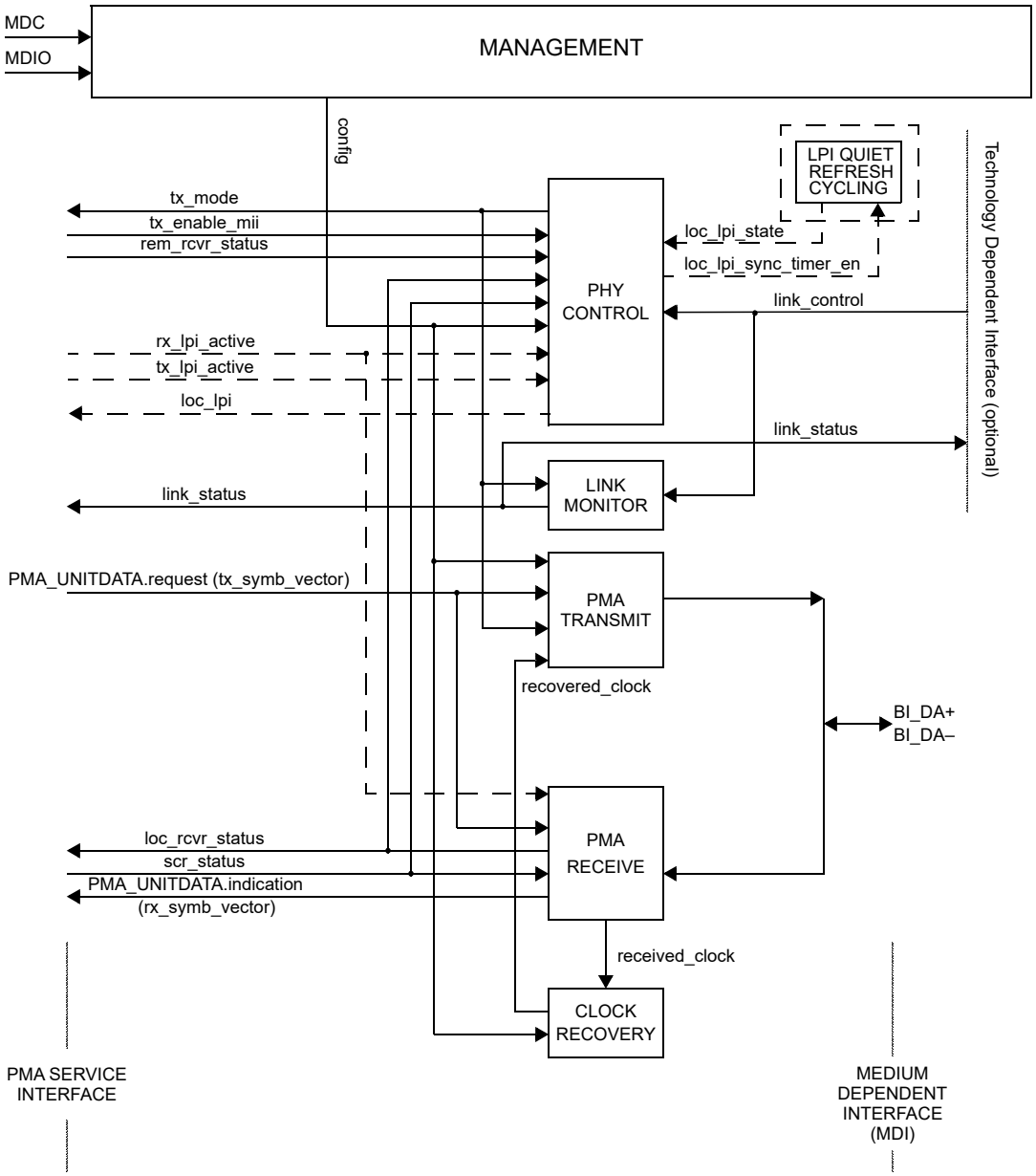
PMA functions are illustrated in Figure 146–12.



NOTE 1—The “recovered_clock” shown indicates the delivery of the recovered clock back to PMA TRANSMIT in SLAVE mode for loop timing.

NOTE 2—Signals shown with dashed lines and blocks within dashed lines are required only for EEE functionality.

Figure 146–12—PMA functional block diagram

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146.4.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

PMA Reset shall set pma_reset = TRUE while any of the above reset conditions hold true. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

146.4.2 PMA Transmit function

Figure 146–13 illustrates the signal flow of the 10BASE-T1L PMA Transmit function. During transmission, PMA_UNITDATA.request conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over the single transmit pair.

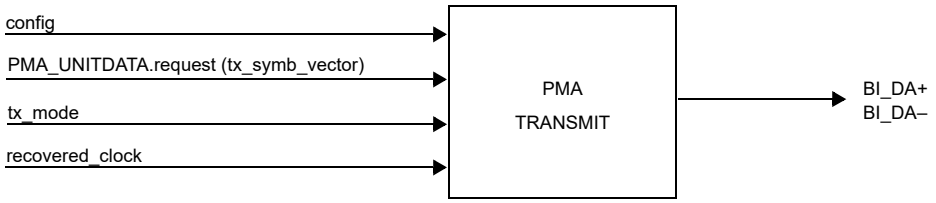

Figure 146–13—PMA Transmit

A single transmitter is used to generate the PAM3 signal BI_DA on the wire using the transmit clock, TX_TCLK (see 146.5.4.5). When the config parameter is set to MASTER, the PMA Transmit function derives the TX_TCLK from a local clock source. When the config parameter is set to SLAVE, the PMA Transmit function derives the TX_TCLK from the recovered clock.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

146.4.3 PMA Receive function

Figure 146–14 illustrates the signal flow of the 10BASE-T1L PMA Receive function. To achieve the indicated performance, it is highly recommended that PMA Receive includes the functions of signal equalization and echo cancellation. The sequence of symbols assigned to tx_symb_vector is needed to perform echo cancellation.

The 10BASE-T1L PMA Receive function comprises a single receiver (PMA Receive) for PAM3 modulated signals on a single balanced pair, BI_DA. PMA Receive has the ability to translate the received signals on the MDI into the PMA_UNITDATA.indication parameter rx_symb_vector. It detects ternary symbol sequences from the signals received at the MDI and presents these sequences to the PCS Receive function. The parameter loc_rcvr_status is generated by PMA Receive to indicate the status of the receive link at the local PHY. This variable indicates to the PCS Transmitter, PCS Receiver, and PMA PHY Control function whether the status of the overall received link is ok or not. Signal scr_status is generated by the PCS Receiver to indicate the status of the descrambler to the local PHY. It conveys the information on whether the scrambler has achieved synchronization or not to the PMA receive function.

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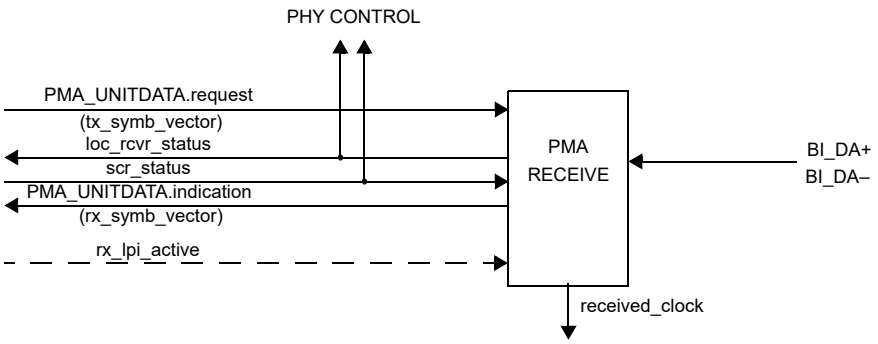

NOTE—Signals shown with dashed lines are required only for EEE functionality.

Figure 146–14—PMA Receive

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.232.7.

146.4.4 PHY Control function

If the Auto-Negotiation process (Clause 98) is not implemented or not enabled, PMA_CONFIG MASTER-SLAVE configuration is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup.

The PHY Control functions block governs the control actions needed to bring the PHY into the 10BASE-T1L mode of operation so that frames can be exchanged with the link partner. PMA PHY Control also generates the signals that control PCS and PMA sublayer operations. It determines whether the PHY operates in the normal mode, enabling data transmission over the link segment, or whether the PHY sends idle data. PHY Control sets tx_mode to SEND_N (transmission of normal MII Data Stream, Control Information, or Idle Data), SEND_I (transmission of Idle Data), or SEND_Z (transmission of zero symbol vectors).

If the time to reach link_status = OK exceeds the duration of the link_fail_inhibit timer used in the Auto-Negotiation Arbitration state diagram (see Figure 98–7), the training may be considered failed. Management reset of the PHY control state diagram when Auto-Negotiation is not enabled (or not present) is outside the scope of this standard.

To maximize power savings, maintain link integrity, and ensure interoperability, EEE-capable PHYs shall synchronize refresh intervals during the low power idle (LPI) mode.

LPI synchronization is established by the PHY Control function, towards the end of link startup, using a handshake scheme initiated by the MASTER. This scheme initiates LPI quiet-refresh cycling at the same time as a transition from TRUE to FALSE of the loc_lpi variable. As loc_lpi is conveyed to the link partner PHY, the time of the start of LPI quiet-refresh cycling is also conveyed. LPI quiet-refresh cycling is defined in 146.4.7.

Thereafter, the LPI quiet-refresh cycling runs freely, with a cycle of fixed period, and, because the SLAVE maintains timing lock with the MASTER, the timing relationship between the quiet-refresh cycling in both PHYs remains fixed.

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PHY Control shall comply with the state diagram shown in Figure 146–15, Figure 146–16, and Figure 146–17. Figure 146–15 describes link startup sequencing. Figure 146–16 describes LPI synchronization sequencing (required only to support EEE capability). Figure 146–17 describes entry and exit to LPI mode (also required only to support EEE capability).

146.4.4.1 Variables

pma_reset
: Allows reset of all PMA functions.
Values: TRUE or FALSE
Set by: PMA Reset

link_control
: This variable is set by management control or via hardware.
Values: ENABLE or DISABLE

config
: The config parameter is set by management or set by auto-negotiation and passed to the PMA and PCS.
Values: MASTER or SLAVE

loc_lpi:
: The variable loc_lpi is set by the PHY Control function to indicate that it has entered low power idle mode.
Values: TRUE or FALSE

loc_lpi_timer_sync_en
: The variable loc_lpi_timer_sync_en is set by the PHY Control function to enable low power idle quiet-refresh cycling.
Values: TRUE: LPI quiet-refresh cycling is enabled.
FALSE: LPI quiet-refresh cycling is disabled.

loc_rcvr_status
: Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive function for the local PHY.
Values: OK: The receive function for the local PHY is operating reliably.
NOT_OK: Operation of the receive function for the local PHY is unreliable.

lpi_enabled
: This variable indicates whether Energy Efficient Ethernet is enabled for the PHY or not.
Values: TRUE: Energy Efficient Ethernet is enabled.
FALSE: Energy Efficient Ethernet is not enabled.

mr_autoneg_enable
: See 98.5.1.

rem_rcvr_status
: Variable set by the PCS Receive function to indicate whether correct operation of the receive function for the remote PHY is detected or not.
Values: OK: The receive function for the remote PHY is operating reliably.
NOT_OK: Reliable operation of the receive function for the remote PHY is not detected.

rx_lpi_active
: This variable indicates to the PMA receive function if the receive state diagram is in low power idle state.
Values: TRUE or FALSE

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scr_status

The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.
Values: OK: The descrambler has achieved synchronization.
NOT_OK: The descrambler is not synchronized.

slave_clock_locked

Variable indicates the status of the clock recovery on a slave PHY. Implementations may benefit from checking scr_status for determining whether the slave clock is locked to the master PHY.
Values: TRUE: The slave clock is stable and locked to the master PHY clock.
FALSE: The slave clock is not locked to the master PHY clock, or is otherwise unstable.

tx_enable_mii

The tx_enable_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 146–4. When set to FALSE transmission is disabled; when set to TRUE transmission is enabled.
Values: TRUE or FALSE

tx_lpi_active

This variable indicates to the PMA PHY control function whether the “Assert Low Power Idle” condition on the MII is active.
Values: TRUE or FALSE

tx_mode

PCS Transmit sends code-groups according to the value of this variable.
Values: SEND_N: This value is continuously asserted when transmitting data, control information or idle during normal operation.
SEND_I: This value is continuously asserted when transmitting idle data during training.
SEND_Z: This value is asserted when transmitting zero code-groups.

146.4.4.2 Timers

maxtraining_timer

A timer used to limit the maximum allowed training time of the receiver. The timer shall expire 3000 ms ± 30 ms after being started.

mintraining_timer

A timer to define the minimum time a slave PHY stays in training mode before going to SILENT state when the slave loses clock lock. The slave clock may be unstable during this period. The timer shall expire 100 ms ± 1 ms after being started.

lpi_sleep_timer

A timer used to determine the duration of the SEND SLEEP state, where transmission comprises IDLE symbols with loc_lpi set. The timer shall expire 150 TX_TCLK periods (nominally 20 μs) after being started.

lpi_wake_timer

A timer used to determine how long the WAKE signal is being sent to the remote PHY. The timer shall expire 1875 TX_TCLK periods (nominally 250 μs) after being started.

maxwait_timer

A timer used to limit the amount of time during which a receiver dwells in the SEND IDLE state. The timer shall expire 200 ms ± 2 ms after being started.

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minwait_timer

A timer used to determine the minimum amount of time the PHY Control stays in the SEND IDLE or DATA states. The timer shall expire 20 μs ± 1 μs after being started.

silent_timer

A timer used to set the time a PHY stays in the SILENT state. The timer shall expire 245 ms ± 5 ms after being started.

NOTE—After a disturbance on the link segment, e.g., when the current consumption on a powered link segment is quickly changed, the maxwait_timer allows the PHYs to stay in the SEND IDLE state before going to the SILENT state. This allows the PHYs to attempt to recover the link before a full retrain.

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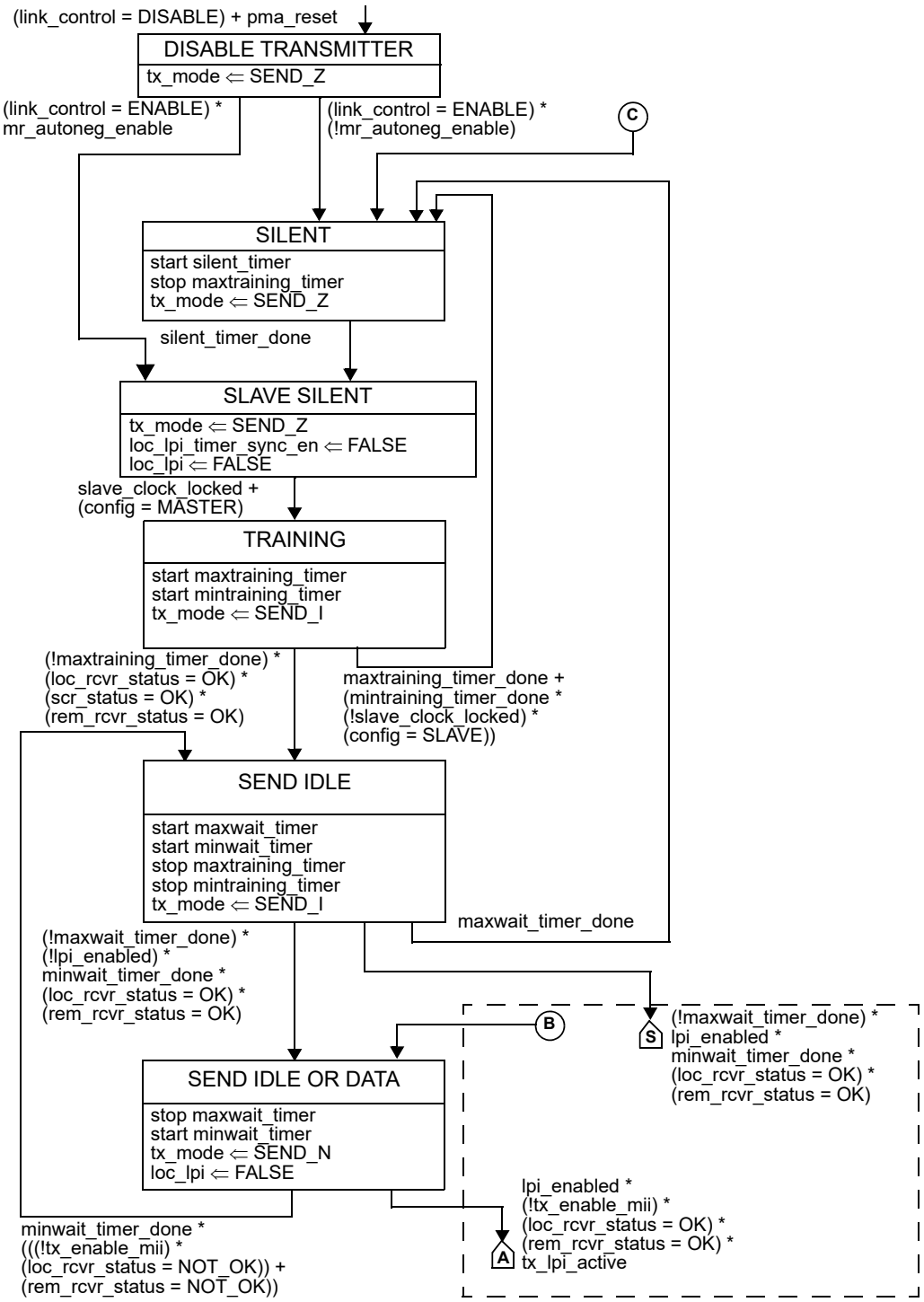
146.4.4.3 State diagram



NOTE—Transitions inside dashed boxes are required only for the EEE capability.

Figure 146–15—PHY Control state diagram, part a

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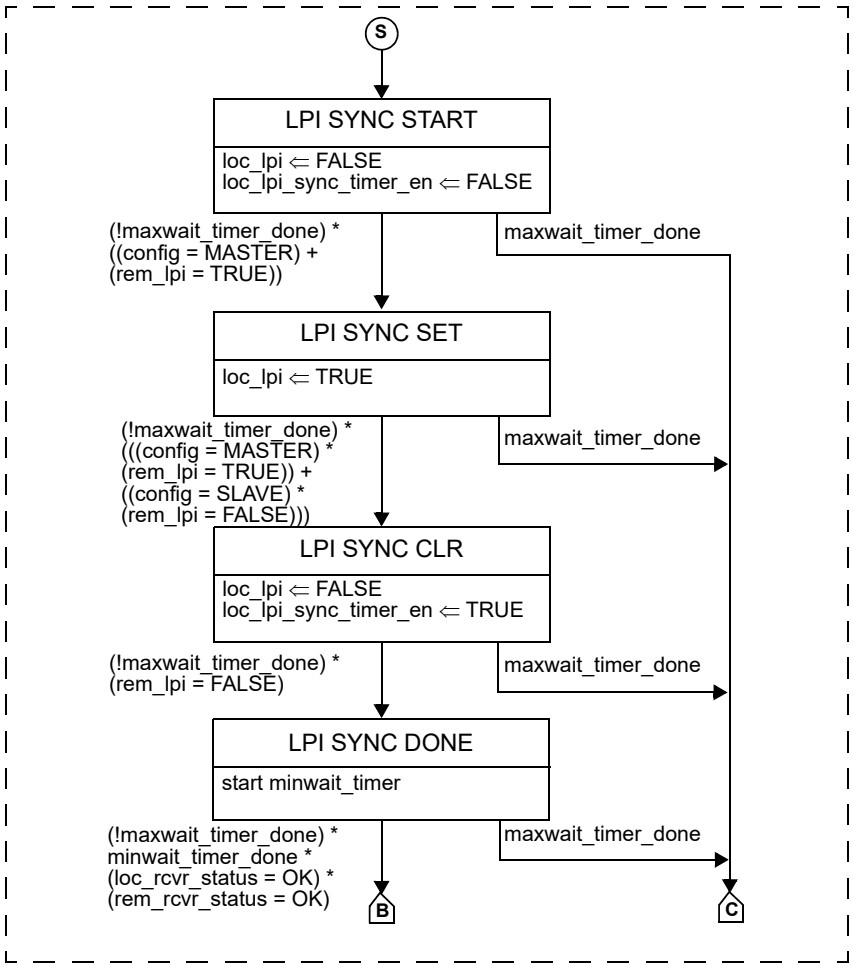

NOTE—Transitions inside dashed boxes are required only for the EEE capability.

Figure 146–16—PHY Control state diagram, part b

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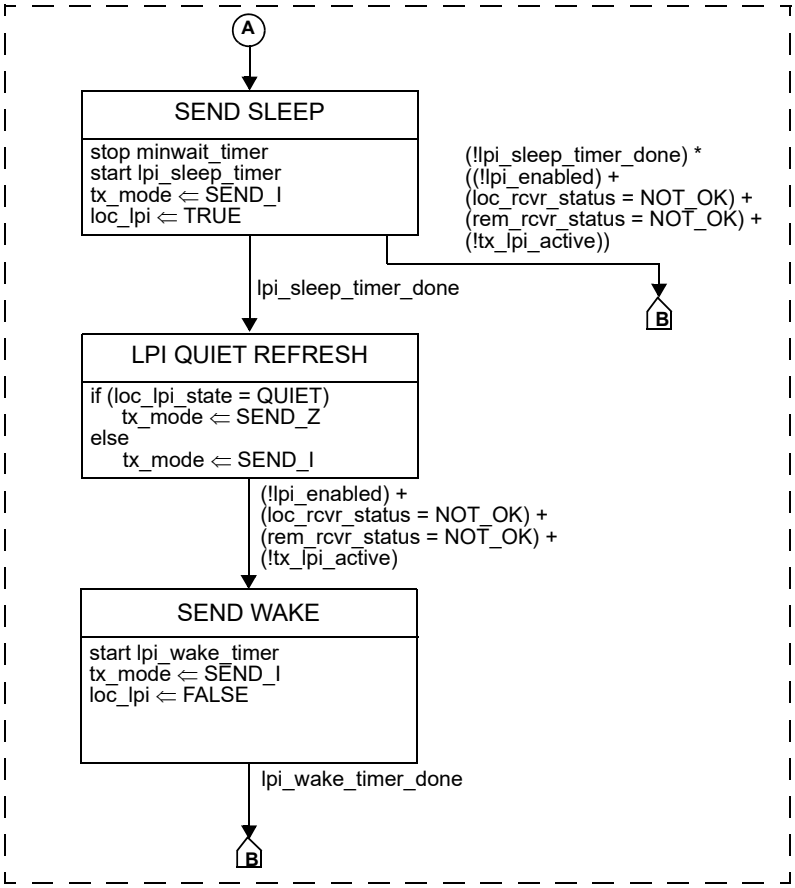

NOTE—Transitions inside dashed boxes are required only for the EEE capability.

Figure 146–17—PHY Control state diagram, part c

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146.4.5 Link Monitor function

Link Monitor operation, as shown in state diagram of Figure 146–18, shall be provided to support PHY Control. Variable link_control is set to ENABLE through management control during the PHY initialization or via default hardware set-up.

146.4.5.1 Variables

tx_mode

The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

146.4.5.2 State diagram

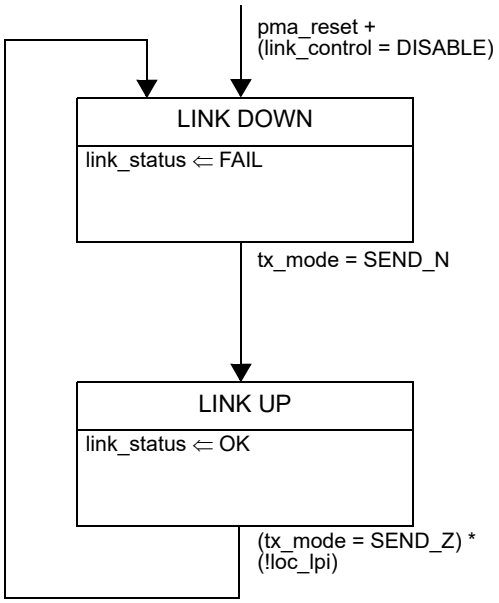

Figure 146–18—PHY Link Monitor state diagram

146.4.6 PMA clock recovery

The clock recovery provides a synchronous clock for sampling the signal on the pair. While it may not drive the MII directly, the Clock Recovery function is the underlying source of TX_CLK. This PMA function recovers the clock from the received stream. It is coupled to the receiver in order to provide for the SLAVE PHY a clock synchronous to the transmit clock of the MASTER PHY.

146.4.7 LPI quiet-refresh cycling

LPI quiet-refresh cycling is initiated on direction from the PHY Control function using the LPI synchronization mechanism.

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Once initiated, LPI quiet-refresh cycling runs freely for the lifetime of the link.

The SLAVE PHY is required to implement an initial offset delay, to ensure that refresh intervals of MASTER and SLAVE are not coincident.

The quiet-refresh cycle timing is defined in terms of transmit symbol periods (TX_TCLK periods). As the SLAVE has to maintain timing lock with the MASTER, the timing relationship between the LPI quiet-refresh cycling of the two PHYs has to remain fixed for the lifetime of the link.

LPI quiet-refresh cycling shall comply with the state diagram of Figure 146–19.

146.4.7.1 Variables

loc_lpi_timer_sync_en

The variable loc_lpi_timer_sync_en is set by the PHY Control function to enable low power idle quiet-refresh cycling.

Values: TRUE: LPI quiet-refresh cycling is enabled.
FALSE: LPI quiet-refresh cycling is disabled.

loc_lpi_state

The variable loc_lpi_state sets the quiet-refresh state when the PHY is in low power idle mode.

Values:
- IDLE: LPI quiet-refresh cycling is not enabled.
- REFRESH: The PHY is in the low power idle refresh phase.
- QUIET: The PHY is in the low power idle quiet phase.

146.4.7.2 Timers

lpi_init_timer

A timer used to set the duration of the LPI TIMER INIT state, which is intended to introduce a fixed offset between LPI refresh phases of the MASTER and SLAVE PHYs.
If config = MASTER, this timer shall expire after 0 TX_TCLK periods.
If config = SLAVE, this timer shall expire after 22500 TX_TCLK periods (nominally 3000 μs).

lpi_refresh_timer

A timer used to set the duration of the LPI refresh phase.
This timer shall expire after 1875 TX_TCLK periods (nominally 250 μs).

lpi_quiet_timer

A timer used to set the duration of the LPI quiet phase.
This timer shall expire after 45 000 TX_TCLK periods (nominally 6000 μs).

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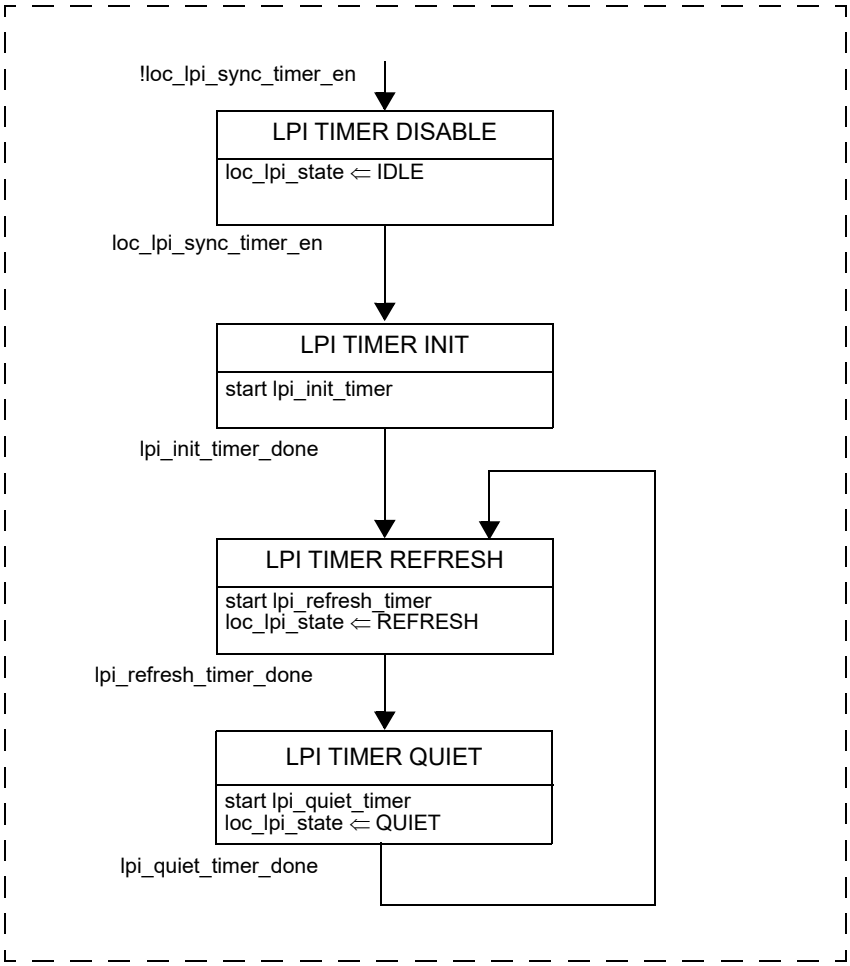
146.4.7.3 State diagram



NOTE—Transitions inside dashed boxes are required only for the EEE capability.

Figure 146–19—LPI quiet-refresh cycling state diagram

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146.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA for a 10BASE-T1L Ethernet PHY.

146.5.1 EMC tests

Direct Power Injection (DPI) and 150 Ω emission tests for noise immunity and emission as per 146.5.1.1 and 146.5.1.2 can be used to establish a baseline for PHY EMC performance. These tests provide a high degree of repeatability and a good correlation to immunity and emission measurements.

146.5.1.1 Immunity—DPI test

In a real application, radio frequency (RF) common-mode (CM) noise at the PHY is the result of electromagnetic interference coupling to the cabling system. Additional differential-mode (DM) noise at the PHY is generated from the CM noise by mode conversion of all parts of the cabling system and the MDI. The sensitivity of the PMA's receiver to RF CM noise can be tested according to the DPI method of IEC 62132-4.

146.5.1.2 Emission—Conducted emission test

The emission of the PMA transmitter to its electrical environment can be tested according to the 150 Ω direct coupling method of IEC 61967-4.

146.5.2 Test modes

The test modes described in this subclause are provided to allow testing of the transmitter waveform, transmitter distortion, transmitter jitter, and transmitter droop. Test modes 1 through 3 shall be implemented as follows. The test modes can be enabled by setting bits 1.2296.15:13 (10BASE-T1L Test Mode Control Register) of the PHY Management register set as described in 45.2.1.233.1. If MDIO is not implemented, a similar functionality shall be provided by another interface. These test modes shall change only the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

a) Test mode 1—Transmitter output voltage and timing jitter test mode
b) Test mode 2—Transmitter output droop test mode
c) Test mode 3—Normal operation in Idle mode. This is for the PSD mask test.

When test mode 1 is enabled, the PHY shall repeatedly transmit the data symbol sequence (+1, –1). See 146.5.4.5 for transmit clock requirements.

When test mode 2 is enabled, the PHY shall transmit ten "+1" symbols followed by ten "–1" symbols. This sequence is repeated continually.

When test mode 3 is enabled, the 10BASE-T1L PHY shall transmit as in non-test operation and in the MASTER data mode with data set to normal Inter-Frame idle signals.

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146.5.3 Test fixture

The following fixtures (illustrated by Figure 146–20 and Figure 146–21), or their functional equivalents, can be used for measuring the transmitter specifications described in 146.5.4. All the transmitter tests are defined at the MDI.

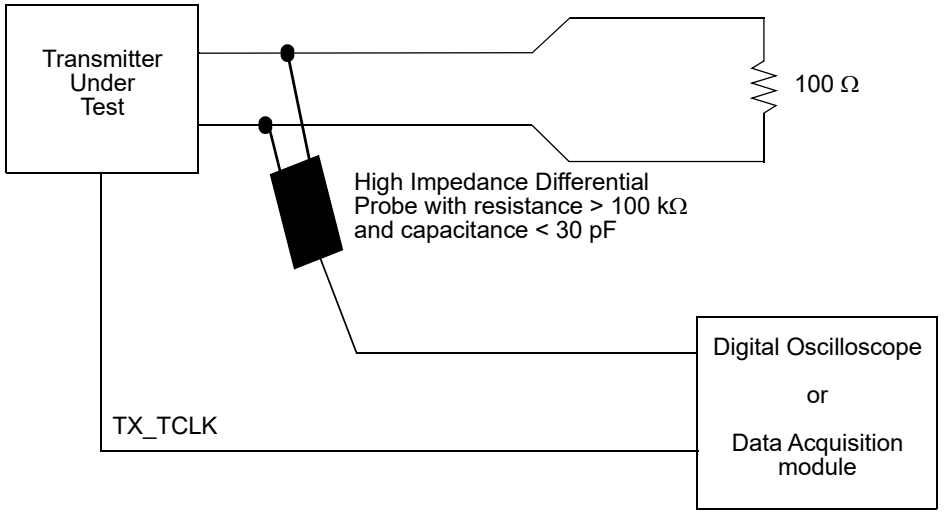

Figure 146–20—Transmitter test fixture 1 for transmitter voltage, transmitter droop, and transmitter timing jitter

To allow an easy synchronization of the measurement equipment, the PHY shall provide access to the symbol rate clock TX_TCLK, which times the transmitted symbols. For a MASTER PHY this is the output of the (divided) clock oscillator; for the SLAVE PHY this is the recovered clock.

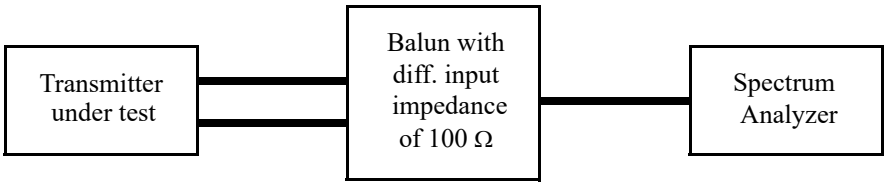

Figure 146–21—Transmitter test fixture 2 for power spectral density measurement and transmit power level measurement

146.5.4 Transmitter electrical specifications

The PMA shall operate with AC coupling to the MDI. Where a load is not specified, the transmitter shall meet the requirements of 146.5.4 with a 100 Ω ± 0.1% resistive differential load connected to the transmitter output.

146.5.4.1 Transmitter output voltage

When tested with the test fixture shown in Figure 146–20 with the transmitter in test mode 1, the transmitter output voltage shall be 2.4 V + 5%/– 15% peak-to-peak (for the 2.4 Vpp operating mode) and 1.0 V + 5%/– 15% peak-to-peak (for the 1.0 Vpp operating mode). Transmitter output voltage can be set using the management interface or by hardware default set-up.

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NOTE—In all transmit modes, including SEND_I and SEND_N, when measured with a 100 Ω ± 0.1% termination, the transmit differential signal at the MDI is less than 2.64 Vpp for the 2.4 Vpp operating mode and 1.10 Vpp for the 1.0 Vpp operating mode including the signal droop.

146.5.4.2 Transmitter output droop

With the transmitter in test mode 2 and using the transmitter test fixture shown in Figure 146–20, the magnitude of both the positive and negative droop shall be less than 10% measured with respect to an initial value at 133.3 ns after the zero crossing and a final value at 800 ns after the zero crossing.

146.5.4.3 Transmitter timing jitter

When tested using the test fixture shown in Figure 146–20 with the transmitter in test mode 1, the maximum jitter at the transmitter side shall be less than 10 ns symbol-to-symbol jitter.

146.5.4.4 Transmitter Power Spectral Density (PSD) and power level

In test mode 3 (reflecting normal operation), the transmit power shall be 8.6 ± 1.2 dBm for the 2.4 Vpp operating mode and 1.0 ± 1.2 dBm for the 1.0 Vpp operating mode. The power spectral density of the transmitter, measured into a 100 Ω load using the test fixture shown in Figure 146–21, shall be between the upper and lower masks specified in Equation (146–6) and Equation (146–7) for the 2.4 Vpp transmit amplitude, and by Equation (146–8) and Equation (146–9) for the 1.0 Vpp transmit amplitude. The masks are shown in Figure 146–22 and Figure 146–23.

For the 2.4 Vpp transmit signal amplitude:

$$\text{Upper PSD Limit } (f) \geq \begin{cases} -54 \text{ dBm/Hz} & 0 \leq f \leq 2.5 \\ -54 - 1.6 \times (f - 2.5) \text{ dBm/Hz} & 2.5 < f < 12.5 \\ -70 \text{ dBm/Hz} & 12.5 \leq f \leq 20 \end{cases} \quad (146\text{–}6)$$

$$\text{Lower PSD Limit } (f) \geq \begin{cases} -60 \text{ dBm/Hz} & 0.625 \leq f \leq 2.5 \\ -60 - 4 \times (f - 2.5) \text{ dBm/Hz} & 2.5 < f \leq 5 \end{cases} \quad (146\text{–}7)$$

where f is the frequency in MHz, and for the 1.0 Vpp transmit signal amplitude:

$$\text{Upper PSD Limit } (f) \geq \begin{cases} -61.6 \text{ dBm/Hz} & 0 \leq f \leq 2.5 \\ -61.6 - 1.6 \times (f - 2.5) \text{ dBm/Hz} & 2.5 < f < 12.5 \\ -77.6 \text{ dBm/Hz} & 12.5 \leq f \leq 20 \end{cases} \quad (146\text{–}8)$$

$$\text{Lower PSD Limit } (f) \geq \begin{cases} -67.6 \text{ dBm/Hz} & 0.625 \leq f \leq 2.5 \\ -67.6 - 4 \times (f - 2.5) \text{ dBm/Hz} & 2.5 < f \leq 5 \end{cases} \quad (146\text{–}9)$$

where f is the frequency in MHz.

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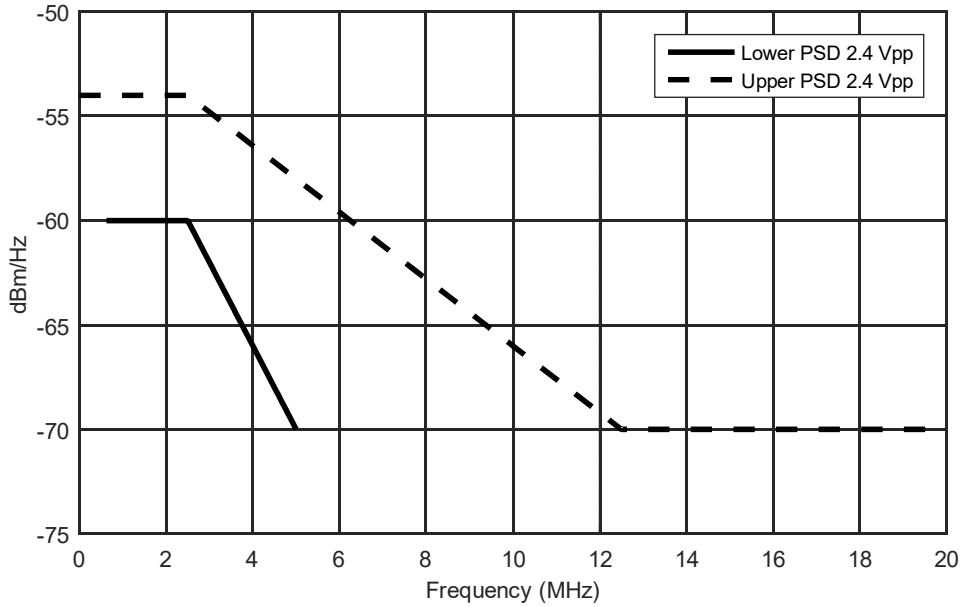

Figure 146–22—Transmitter Power Spectral Density, 2.4 Vpp Transmit Amplitude, Upper and Lower Masks

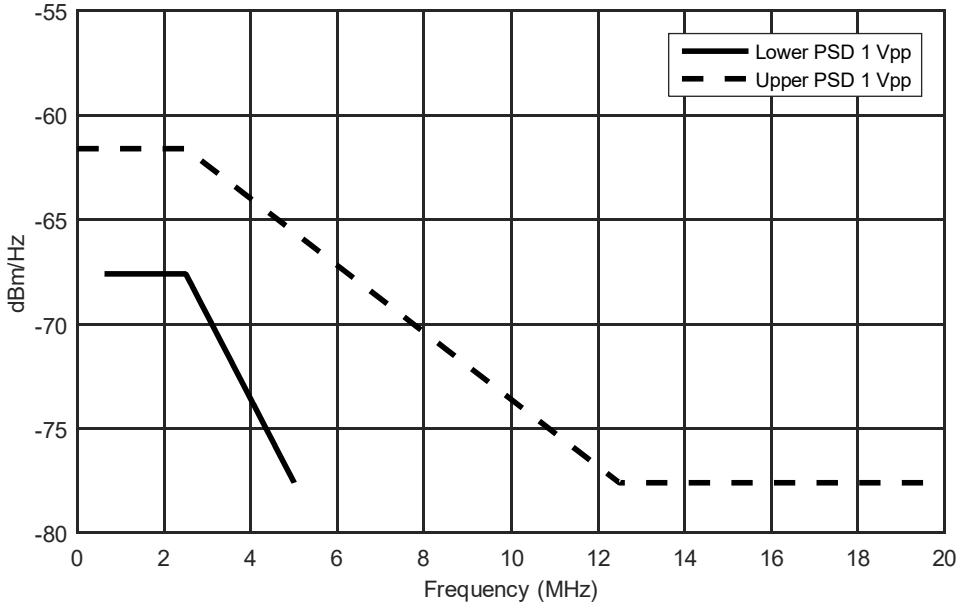

Figure 146–23—Transmitter Power Spectral Density, 1 Vpp Transmit Amplitude, Upper and Lower Masks

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146.5.4.5 Transmit clock frequency

The symbol transmission rate of the MASTER PHY shall be within the range 7.5 MBd ± 50 ppm. For a MASTER PHY, when the transmitter is in the LPI transmit mode, the transmitter clock short-term rate of frequency variation shall be less than 0.1 ppm/second. The short-term frequency variation limit shall also apply when switching to and from the LPI mode.

146.5.5 Receiver electrical specifications

The PMA shall meet the requirements specified in PMA Receive function and the electrical specifications of this subclause. The link segment used in the test configurations shall be within the limits specified in 146.7.

146.5.5.1 Receiver differential input signals

Differential signals received at the MDI, that were transmitted from a remote transmitter within the specifications of 146.5.4, and have passed through a link segment specified in 146.7, shall be received with a bit error ratio less than 10^{-9} after PCS processing and sent to the MII after completion of link training. This specification can be verified by a frame error ratio less than 10^{-6} for 125 octet frames.

146.5.5.2 Receiver frequency tolerance

The receiver shall properly receive incoming data with a symbol rate within the range 7.5 MBd ± 50 ppm.

146.5.5.3 Alien crosstalk noise rejection

This specification is provided to verify the receiver's tolerance to alien crosstalk noise. The test is performed with a noise source such that noise with a Gaussian distribution, bandwidth of 10 MHz, and magnitude of –106 dBm/Hz is present at the MDI. The receive DUT is connected to these noise sources through a resistive network, as shown in Figure 146–24, with a link segment as defined in 146.7. The BER shall be less than 10^{-9}. This specification may be considered satisfied when the frame loss ratio is less than 10^{-6} for 125 octet packets measured at MAC/PLS service interface.

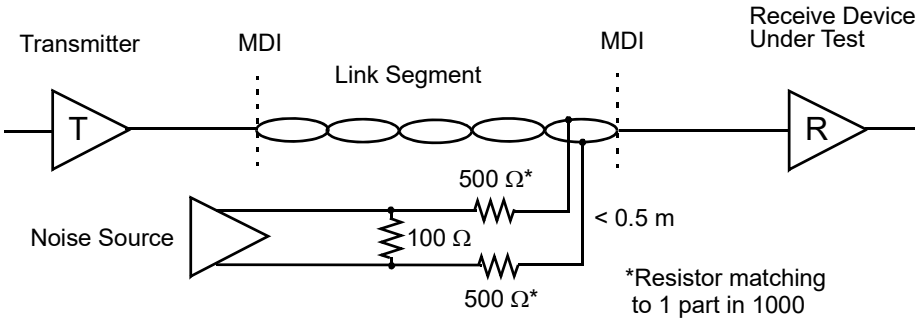

Figure 146–24—Alien crosstalk noise rejection test set-up

NOTE—If the output level is too high for the noise generator, the resistor divider network may be adapted to allow for a lower noise generator output level so that the noise signal fed into the receiver has a magnitude of –106 dBm/Hz with a bandwidth of 10 MHz, taking the 100 Ω termination within the PHY into account.

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146.5.6 PMA local loopback

The PMA local loopback function is optional. If supported, the PMA shall be placed in local loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, or the PMA loopback bit in MDIO register 1.2294.0, defined in 45.2.1.231.6, is set to one (or PMA loopback mode is enabled by a similar functionality if MDIO is not implemented). When the PHY is in the PMA local loopback mode, the PMA Receive function utilizes the echo signals from the open MDI and decodes these signals to pass the data back to the MII Receive interface. The data flow of the external loopback is shown in Figure 146–25. When PMA loopback mode is present and enabled, the PCS transmit scrambler polynomial and the receiver descrambler polynomial should be matched, e.g., the MASTER scrambler polynomial and the SLAVE descrambler polynomial, in order for looped data to be properly descrambled at the MII.

A MAC client can compare the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the 10BASE-T1L PCS and PMA functions.

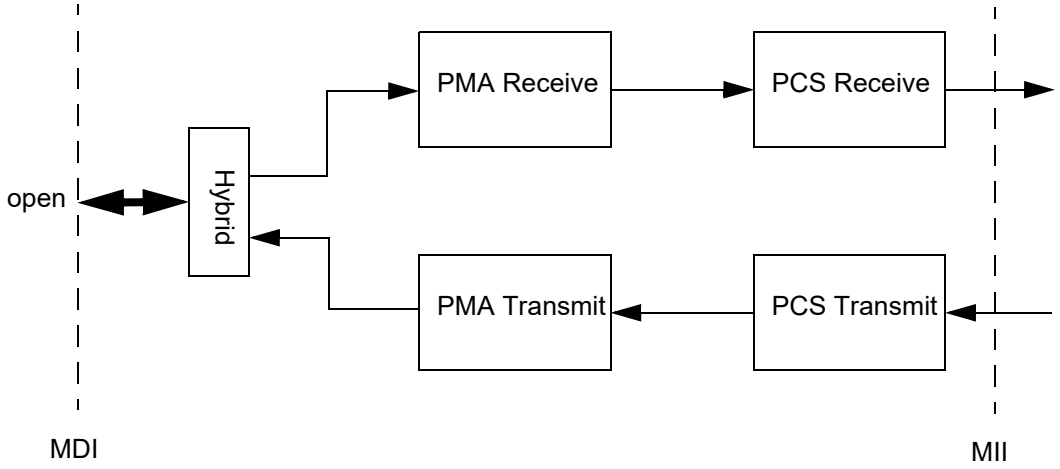

Figure 146–25—PMA loopback data flow

146.6 Management interface

10BASE-T1L uses the management interface as specified in Clause 45. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

146.6.1 Support for Auto-Negotiation

If Auto-Negotiation is supported and enabled, the mechanism described in Clause 98 shall be used. Auto-Negotiation may be performed as part of the initial set-up of the link and allows negotiation of MASTER/SLAVE for loop timing, increased transmit level, and EEE capabilities.

146.6.2 MASTER-SLAVE configuration

MASTER-SLAVE assignment for each link configuration is necessary for establishing the timing control of each PHY. In 10BASE-T1L, one PHY should be configured as MASTER and one PHY should be configured as SLAVE to operate. In the case where both PHYs are configured to be MASTER or both to be SLAVE, operation is undefined.

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If Auto-Negotiation is available and enabled, the MASTER-SLAVE configuration between the PHYs is established using the method being described in 98.2.1.2.5 and Table 98–4. If there is no Auto-Negotiation functionality present or if Auto-Negotiation function has been disabled, the MASTER-SLAVE configuration is performed for each PHY using bit 1.2100.14 (BASE-T1 PMA/PMD control register) or equivalent functionality.

146.6.3 PHY initialization

Both PHYs sharing a link segment are capable of being MASTER or SLAVE. A forced assignment scheme or an Auto-Negotiation process is employed depending on the use case of the PHY. This process is conducted at the power-up or reset condition. The station management systems can manually configure the 10BASE-T1L PHY to be MASTER or to be SLAVE (before the link acquisition process starts) or a hardware set-up using bootstrap options can be implemented.

When MDIO is implemented, MASTER/SLAVE mode can be selected by setting bit 1.2100.14 (BASE-T1 PMA/PMD Control Register) of the PHY Management register set as described in 45.2.1.214. If MDIO is not implemented, a similar functionality shall be provided by another interface. The default setting is to use Auto-Negotiation, if available.

146.6.4 Increased transmit level configuration

The transmitter output voltage can be selected by setting bit 1.2294.12 (10BASE-T1L PMA control register) of the PHY Management register set as described in 45.2.1.231.3 if Auto-Negotiation is disabled or not present. If MDIO is not implemented, a similar functionality shall be provided by another interface.

When Auto-Negotiation is implemented and enabled, bit A23 shall contain a one if the PHY is requesting the increased transmit level from its link partner, and it shall contain a zero if the 2.4 Vpp operating mode is not requested from the link partner (see 146.5.4.1). Bit A24 shall contain a one if the PHY is supporting and advertising the 2.4 Vpp operating mode, and it shall contain a zero if the 2.4 Vpp operating mode is not supported or not advertised.

When Auto-Negotiation is present and enabled and both PHYs advertise an increased transmit/receive ability if at least one PHY requests the 10BASE-T1L increased transmit level, then both PHYs shall use the 2.4 Vpp operating mode, in all other cases both PHYs shall use the 1.0 Vpp operating mode.

146.6.5 EEE configuration

When Auto-Negotiation is implemented and enabled, bit A25 shall contain a one if the 10BASE-T1L PHY is supporting and advertising Energy Efficient Ethernet ability and it shall contain a zero if Energy Efficient Ethernet is not supported or not advertised.

146.6.6 PMA and PCS MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA and PCS. When MDIO is implemented, mapping of MDIO register bits to PMA and PCS control/status variables is shown in Table 146–4. If no MDIO is implemented, a similar functionality shall be implemented to access the needed variables.

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Table 146–4—MDIO register bit mapping

Register Name	Register/Bit Number	Control/Status variable
BASE-T1 PMA/PMD control register	1.2100.3:0	T1 PHY type selection
BASE-T1 PMA/PMD control register	1.2100.14	Master/Slave mode
PMA/PMD Control 1 register 10BASE-T1L PMA control register	1.0.15 1.2294.15	pma_reset
PMA/PMD Control 1 register 10BASE-T1L PMA control register	1.0.0 1.2294.0	PMA loopback
PMA/PMD Status 1 register 10BASE-T1L PMA status register	1.1.2 1.2295.0	link_status
10BASE-T1L PMA control register	1.2294.12	Transmit voltage amplitude control
PCS Control 1 register 10BASE-T1L PCA control register	3.0.15 3.2278.15	pcs_reset
PCS Control 1 register 10BASE-T1L PCA control register	3.0.14 3.2278.14	PCS loopback

146.7 Link segment characteristics

10BASE-T1L is designed to operate over a single balanced pair of conductors that meets the requirements specified in this subclause. The single balanced pair of conductors supports an effective data rate of 10 Mb/s in each direction simultaneously. The term “link segment” used in this clause refers to a single balanced pair of conductors operating in full duplex. Note that Annex 146B provides information on the optional powering topologies. The class power requirements are specified in Clause 104.

The link segment specified in this clause is based on process control application requirements and supports up to ten in-line connectors using a single balanced pair of conductors for up to at least 1000 m.

146.7.1 Link transmission parameters for 10BASE-T1L

The transmission characteristics for the 10BASE-T1L link segment are specified to support applications requiring long reach such as industrial and process control, for up to at least 1000 m. 10BASE-T1L link segments may be shielded or screened, consistent with the specification in 146.7.1.6 and 146.7.2 or unshielded consistent with the specifications in 146.7.1.6 and 146.7.1.4.

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146.7.1.1 Insertion loss

All 10BASE-T1L PHYs support the insertion loss specified in 146.7.1.1.2, but support of the insertion loss specified in 146.7.1.1.1 is required only when the 2.4 Vpp transmit/receive ability is operational.

146.7.1.1.1 Insertion loss for PHYs in the 2.4 Vpp operation mode

For PHYs in the 2.4 Vpp operation mode, the insertion loss of each 10BASE-T1L link segment shall meet the values determined using Equation (146–10).

$$\text{Insertion loss}(f) \le 10\left(1.23 \times \sqrt{f} + 0.01 \times f + \frac{0.2}{\sqrt{f}}\right) + 10 \times 0.02 \times \sqrt{f} \quad \text{(dB)} \tag{146–10}$$

where

f is the frequency in MHz; $0.1 \le f \le 20$

The insertion loss is illustrated in Figure 146–26.

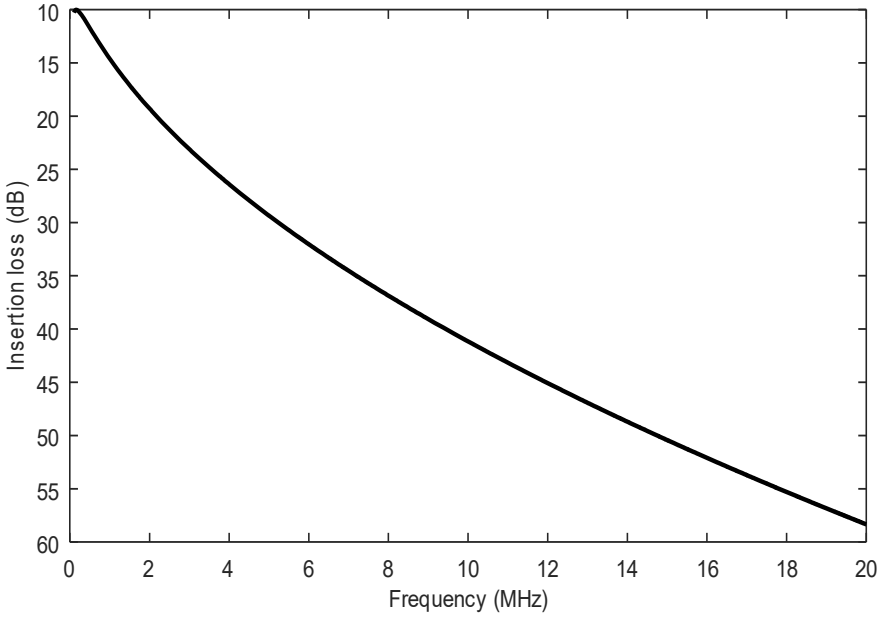

Figure 146–26—Insertion loss calculated using Equation (146–10)

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146.7.1.1.2 Insertion loss supported for PHYs in 1.0 Vpp operation mode

For PHYs in the 1.0 Vpp operation mode, the insertion loss of each 10BASE-T1L link segment shall meet the values determined using Equation (146–11).

$$\text{Insertion loss}(f) \le 5.9\left(1.23 \times \sqrt{f} + 0.01 \times f + \frac{0.2}{\sqrt{f}}\right) + 10 \times 0.02 \times \sqrt{f} \quad \text{(dB)} \tag{146–11}$$

where

f is the frequency in MHz; $0.1 \le f \le 20$

The insertion loss is illustrated in Figure 146–27.

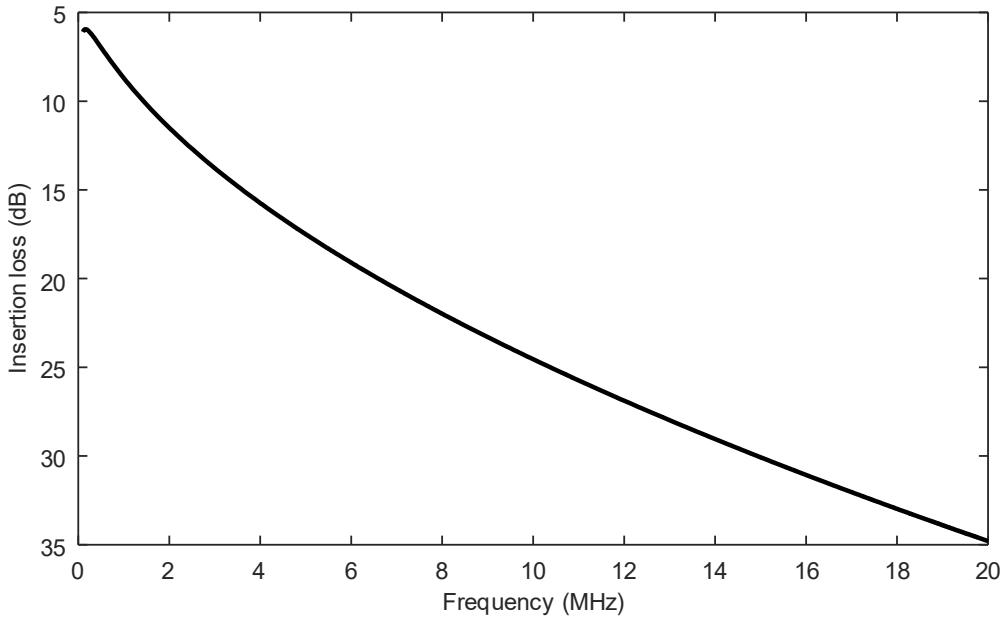

Figure 146–27—Insertion loss calculated using Equation (146–11)

146.7.1.2 Return loss

In order to limit the noise at the receiver due to impedance mismatches, each 10BASE-T1L link segment shall meet the values determined using Equation (146–12) at all frequencies from 0.1 MHz to 20 MHz. The reference impedance for the return loss specification is 100 Ω.

$$\text{Return loss} \ge \left\{ \begin{array}{rl} 9 + 8 \times f & 0.1 \le f < 0.5 \text{ MHz} \\ 13 & 0.5 \le f \le 20 \text{ MHz} \end{array} \right\} \text{dB} \tag{146–12}$$

where

f is the frequency in MHz; $0.1 \le f \le 20$

The return loss is illustrated in Figure 146–28.

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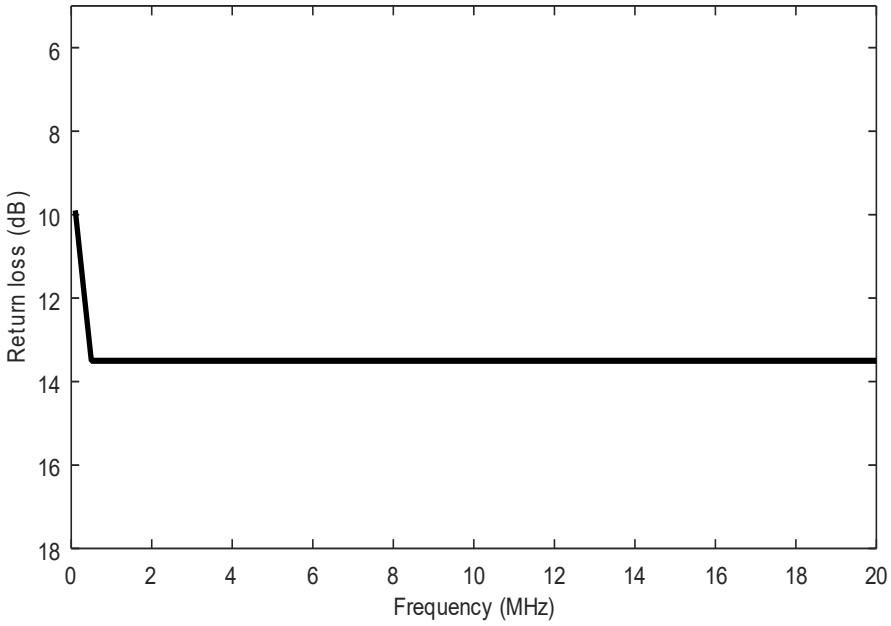

Figure 146–28—Return loss calculated using Equation (146–12)

146.7.1.3 Maximum link delay

The propagation delay of a 10BASE-T1L link segment shall not exceed 8834 ns at all frequencies between 0.1 MHz and 20 MHz. Note that the delay is derived from the point-to-point 1.63 mm (14 AWG) link segment length of 1589 m given in Table 146B–1 using Equation (80–1) with an 'n' of 0.6.

146.7.1.4 Differential-to-common-mode conversion

The differential-to-common-mode conversion requirement applies to unshielded link segments and depends on the electromagnetic noise environment. The requirements of Table 146–5 shall be met based on the local environment as described by the electromagnetic classifications given in Table 146–7, E_1 or E_2.

Table 146–5—Differential-to-common-mode conversion

	Frequency (MHz)	E_1	E_2
TCL	$0.1 \leq f \leq 10$	≥ 50 dB	≥ 50 dB
TCL	$10 < f \leq 20$	$\geq 50 - 20\log_{10}\left(\frac{f}{10}\right)$ dB	$\geq 50 - 20\log_{10}\left(\frac{f}{10}\right)$ dB

146.7.1.5 Coupling attenuation

The coupling attenuation requirement applies to shielded link segments and depends on the electromagnetic noise environment. The requirements in Table 146–6 shall be met based on the local environment as described by the electromagnetic classifications given in Table 146–7, E1, E2, or E3.

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Table 146–6—Coupling attenuation

Frequency (MHz)	(dB)		
	E_1	E_2	E_3
0.1 to 20	≥ 50	≥ 50	≥ 60

146.7.1.6 Electromagnetic classifications

Electromagnetic classifications for the link segment local environments are given in Table 146–7, for E_1, E_2, or E_3.

Table 146–7—Link segment electromagnetic classifications (ISO/IEC 11801-1)

Electromagnetic	E_1	E_2	E_3
Conducted RF	3 V at 150 kHz to 80 MHz	3 V at 150 kHz to 80 MHz	10 V at 150 kHz to 80 MHz

146.7.2 Coupling parameters between 10BASE-T1L link segments

Noise coupled between the disturbed 10BASE-T1L link segment and other disturbing 10BASE-T1L link segments is referred to as alien crosstalk noise. To ensure that the total alien NEXT loss and alien FEXT loss coupled between 10BASE-T1L link segments are limited, multiple disturber alien near-end crosstalk (MDANEXT) loss and multiple disturber alien far-end crosstalk (MDAFEXT) loss are specified.

146.7.2.1 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

In order to limit the alien crosstalk at the near end of a 10BASE-T1L link segment, the differential pair-to-pair near-end crosstalk (NEXT) loss between the disturbed 10BASE-T1L link segment and other disturbing 10BASE-T1L link segments is specified to meet the bit error ratio objective. To ensure that the total alien NEXT coupled into a 10BASE-T1L link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT disturbers.

PSANEXT loss is determined by summing the power of the individual pair-to-pair differential alien NEXT loss values over the frequency range 0.1 MHz to 20 MHz as follows in Equation (146–13).

$$\mathrm{PSANEXT}_N(f) = -10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AN}(f)_{j,N}}{10}} \ \mathrm{dB} \qquad (146\text{–}13)$$

where the function $\mathrm{AN}(f)_{j,N}$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing 10BASE-T1L link segment j (1 to m) for the disturbed 10BASE-T1L link segment N.

The power sum ANEXT loss between a disturbed 10BASE-T1L link segment and other disturbing 10BASE-T1L link segments shall meet the values determined using Equation (146–14) or 60 dB, whichever is less.

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$$\text{PSANEXT}(f) \geq 37.5 - 17\log_{10}\left(\frac{f}{20}\right) \text{ dB} \quad (146\text{–}14)$$

where

f is the frequency in MHz; $0.1 \leq f \leq 20$

146.7.2.2 Multiple disturber power sum alien far-end crosstalk (PSAFEXT) loss

In order to limit the alien crosstalk at the far-end of a 10BASE-T1L link segment, the differential pair-to-pair alien far-end crosstalk (FEXT) loss between the disturbed 10BASE-T1L link segment and other disturbing 10BASE-T1L link segments is specified to meet the bit error ratio objective. To ensure that the total alien FEXT coupled into a 10BASE-T1L link segment is limited, multiple disturber AFEXT is specified as the power sum of the individual alien FEXT disturbers. Note that the MDAFEXT is specified as the power sum of the individual alien FEXT disturbers (PSAFEXT) and not individual alien ACRF disturbers (PSAACR-F).

PSAFEXT is determined by summing the power of the individual pair-to-pair differential alien FEXT values over the frequency range 0.1 MHz to 20 MHz as follows in Equation (146–15).

$$\text{PSAFEXT}_N(f) = -10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\text{AF}(f)_{j,N}}{10}} \text{ dB} \quad (146\text{–}15)$$

where the function $\text{AF}(f)_{j,N}$ represents the magnitude (expressed in dB) of the alien FEXT of the disturbing 10BASE-T1L link segment j (1 to m) for disturbed 10BASE-T1L link segment N.

The power sum AFEXT between a disturbed 10BASE-T1L link segment and other disturbing 10BASE-T1L link segments shall meet the values determined using Equation (146–16) or 60 dB, whichever is less.

$$\text{PSAFEXT}(f) \geq 38 - 18\log_{10}\left(\frac{f}{20}\right) \text{ dB} \quad (146\text{–}16)$$

where

f is the frequency in MHz; $0.1 \leq f \leq 20$

146.8 MDI specification

This subclause describes connectors that may be used at the MDI. It also specifies electrical requirements, including fault tolerance, at the MDI.

146.8.1 MDI connectors

The mechanical interface to the balanced cabling is a 3-pin connector (BI_DA+, BI_DA–, and optional SHIELD) or alternatively a 2-pin connector with an optional additional mechanical shield connection that conforms to the link segment specification defined in 146.7.

Specific systems or applications can use connectors or terminals that support the link segment specification defined in 146.7.

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Connectors meeting the mechanical requirements of IEC 63171-1 [B36] or IEC 63171-6:2020 [B37] may be used as the mechanical interface to the balanced cabling. The plug connector is used on the balanced cabling and the MDI jack connector on the PHY. The IEC 63171-1 plug and jack are depicted (for informational use only) in Figure 146–29 and Figure 146–30 respectively, and the mating interface is depicted in Figure 146–31. The IEC 63171-6 plug and jack are depicted (for informational use only) in Figure 146–32 and Figure 146–33 respectively, and the mating interface is depicted in Figure 146–34. These connectors should support link segment DCR characteristics for 1.02 mm (18 AWG) to 0.40 mm (26 AWG) in Table 146B–1.

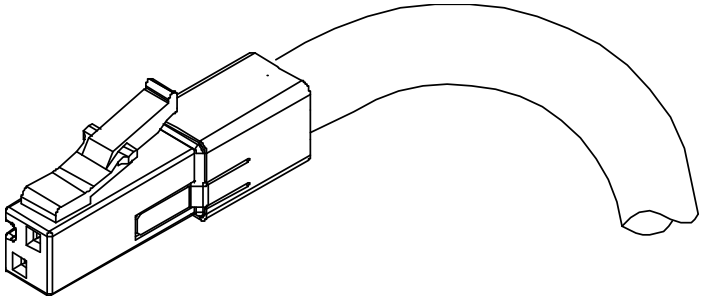

Figure 146–29—IEC 63171-1 plug

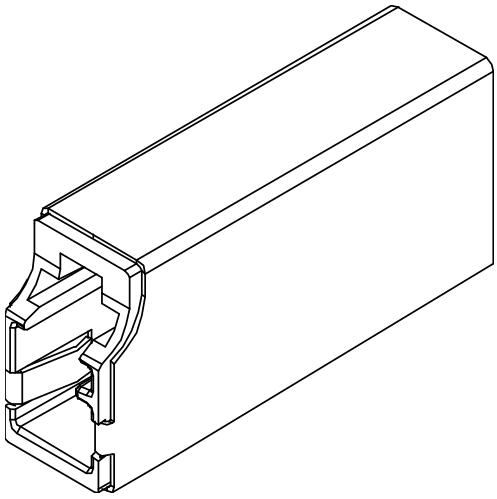

Figure 146–30—IEC 63171-1 jack

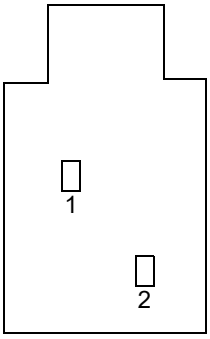

Figure 146–31—IEC 63171-1 mating face

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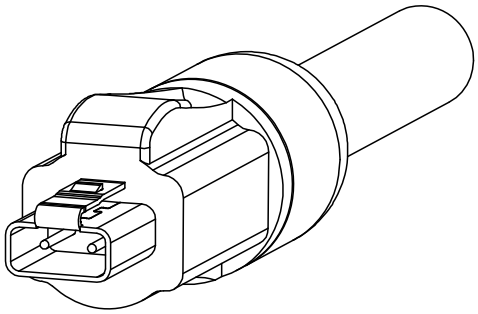

Figure 146–32—IEC 63171-6 plug

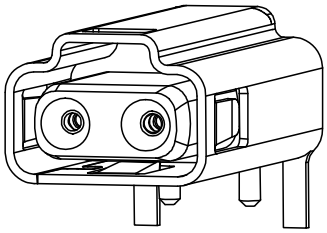

Figure 146–33—IEC 63171-6 jack

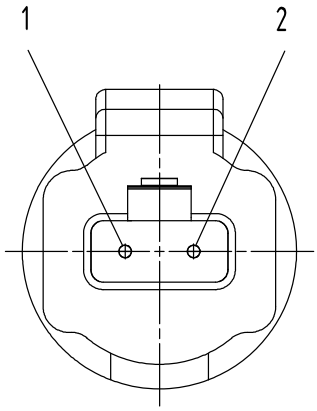

Figure 146–34—IEC 63171-6 mating face

The assignment of PMA signals to connector contacts for PHYs are given in Table 146–8.

Table 146–8—Assignment of PMA signals to MDI contacts

Contact	PMA signal
1	BI_DA+
2	BI_DA–

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146.8.2 MDI electrical specification

The electrical requirements specified in 146.5.4 and 146.5.5 shall be met when the PHY is connected to the MDI connector mated with the specified plug connector.

146.8.3 MDI return loss

The MDI return loss (RL) shall meet or exceed Equation (146–17) for all frequencies from 100 kHz to 20 MHz (with 100 Ω ± 0.1% reference impedance) at all times when the PHY is transmitting data or idle symbols.

$$\text{Return Loss } (f) \geq \begin{cases} 20 - 18 \times \log_{10}\left(\frac{0.2}{f}\right) \text{ dB} & 0.1 \leq f < 0.2 \text{ MHz} \\ 20 \text{ dB} & 0.2 \leq f \leq 1 \text{ MHz} \\ 20 - 16.7 \times \log_{10}(f) \text{ dB} & 1 < f \leq 10 \text{ MHz} \\ 3.3 - 7.6 \times \log_{10}\left(\frac{f}{10}\right) \text{ dB} & 10 < f \leq 20 \text{ MHz} \end{cases} \quad (146\text{–}17)$$

where f is the frequency in MHz.

146.8.4 MDI mode conversion loss

Mode conversion LCL (Sdc11) or TCL (Scd11) of the PHY measured at the MDI shall meet the values determined using Equation (146–18).

$$\text{Conversion Loss } (f) \geq \begin{bmatrix} 25 \text{ dB} & 0.1 \leq f \leq 10 \text{ MHz} \\ 25 - 20 \times \log_{10}\left(\frac{f}{10}\right) \text{ dB} & 10 < f \leq 20 \text{ MHz} \end{bmatrix} \quad (146\text{–}18)$$

where f is the frequency in MHz.

146.8.5 MDI DC power voltage tolerance

The DTE shall withstand without damage the application of any voltages between 0 V dc and 60 V dc with the source current limited to 2000 mA, applied across BI_DA+ and BI_DA–, in either polarity, under all operating conditions, for an indefinite period of time. This requirement ensures that all devices tolerate DC powering voltages, such as those in Clause 104, even if the device does not require power.

146.8.6 MDI fault tolerance

The wire pair of the MDI shall withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential, as per Table 146–9, under all operating conditions, for an indefinite period of time with the source current limited to 2000 mA. Normal operation shall resume after the short circuit(s) is/are removed.

The wire pair of the MDI is expected to withstand, without damage, high-voltage transient noises and ESD per application requirements. Table 146–9 gives an overview about possible connection faults for the wire pair (BI_DA+ and BI_DA–).

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Table 146–9—Fault conditions

BI_DA+	BI_DA–
BI_DA–	BI_DA+
Ground	No fault
No fault	Ground
Ground	Ground
+60 V dc	No fault
No fault	+60 V dc
+60 V dc	+60 V dc
Ground	+60 V dc
+60 V dc	Ground

146.9 Environmental specifications

146.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2 or IEC 61010-1, as appropriate. All equipment subject to this clause may be additionally required to conform to any applicable local, state, or national standards

146.9.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner. All 10BASE-T1L cabling is expected to be routed according to any applicable local, state, or national standards considering all relevant safety requirements.

146.9.2.1 Environmental safety

In industrial applications, all equipment subject to this clause is expected to conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications, where applicable:

— Environmental loads: IEC 60529 and ISO 4892
— Mechanical loads: IEC 60068-2-6 and IEC 60068-2-31
— Climatic loads: IEC 60068-2-1, IEC 60068-2-2, IEC 60068-2-14, IEC 60068-2-27, IEC 60068-2-30, IEC 60068-2-38, IEC 60068-2-52, and IEC 60068-2-78

146.9.2.2 Electromagnetic compatibility

A system integrating the 10BASE-T1L PHY is expected to comply with all applicable local and national codes for electromagnetic compatibility.

146.10 Delay constraints

Every 10BASE-T1L PHY associated with MII shall comply with the bit delay constraints for full duplex operation. The delay for the transmit path, from the MII input to the MDI, shall be less than

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3.2 μs (32 bit times). The delay for the receive path, from the MDI to the MII output, shall be less than 6.4 μs (64 bit times).

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146.11 Protocol implementation conformance statement (PICS) proforma for Clause 146, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1L[242]

146.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 146, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1L, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

146.11.2 Identification

146.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

146.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 146, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1L
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[242] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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146.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
MII	PHY associated with MII	146.1.1		O	Yes [ ] No [ ]
*EEE	Energy Efficient Ethernet (EEE) capability	146.1.2, 78		O	Yes [ ] No [ ]
*AN	Auto-Negotiation	98		O	Yes [ ] No [ ]
*INS	Installation / cabling	146.7	Items marked with INS include installation practices and cabling specifications not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]
PCS	10BASE-T1L PCS	146.3		M	Yes [ ]
PMA	10BASE-T1L PMA	146.4		M	Yes [ ]
*MDIO	MDIO capability	45.1		O	Yes [ ] No [ ]
*RTDL	2.4 Vpp operating mode	146.5.4.1		O	Yes [ ] No [ ]

146.11.4 PICS proforma tables for Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1L

146.11.4.1 Physical Coding Sublayer (PCS)

146.11.4.1.1 PCS Transmit

Item	Feature	Subclause	Value/Comment	Status	Support
PCST1	PCS reset	146.3.1	See 146.3.1	M	Yes [ ]
PCST2	PCS Data Transmission Enable function	146.3.2	Conform to the PCS Transmit State diagram	M	Yes [ ]
PCST3	PCS Transmit function	146.3.3.1	Conform to the PCS Transmit state diagram in Figure 146–5 and PCS Transmit multiplexer state diagram in Figure 146–6 and the associated state variables, functions, and messages	M	Yes [ ]
PCST4	Master PHY PCS side-stream scrambler	146.3.3.4.1	See Equation (146–1)	M	Yes [ ]
PCST5	Slave PHY PCS side-stream scrambler	146.3.3.4.1	See Equation (146–2)	M	Yes [ ]
PCST6	PCS scrambler seed values	146.3.3.4.1	Never initialized to zeros	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PCST7	Sy_n[4:0]	146.3.3.4.2	See 146.3.3.4.2	M	Yes [ ]
PCST8	Sd_n[3:0]	146.3.3.4.3	See 146.3.3.4.3	M	Yes [ ]
PCST9	Sy_n[1] and Sy_n[2]	146.3.3.4.3	Swapped compared to data transmission	M	Yes [ ]

146.11.4.1.2 PCS Receive

Item	Feature	Subclause	Value/Comment	Status	Support
PCSR1	PCS Receive function	146.3.4.1	Conform to the PCS Receive state diagram and associated variables	M	Yes [ ]
PCSR2	Receive watchdog state diagram	146.3.4.1	See Figure 146–11	M	Yes [ ]
PCSR3	Maximum dwelling time in DATA state of PCS receive state diagram	146.3.4.1	Less than rcv_max_timer	M	Yes [ ]
PCSR4	disparity_error signal	146.3.4.2	Generated by the decoder when a code-group is received that is not allowed according to the current running disparity value	M	Yes [ ]
PCSR5	RX_DV	146.3.4.2	RX_DV = TRUE when SSD is received, RX_DV = FALSE when ESD or ESD with error is received	M	Yes [ ]
PCSR6	RX_ER	146.3.4.2	RX_ER = TRUE when bad ESDs, ERR_ESD, or bad SSDs are received, RX_ER reset to FALSE when in IDLE state of PCS Receive state diagram	M	Yes [ ]
PCSR7	MASTER PHY side-stream descrambler	146.3.4.3	See Equation (146–4)	M	Yes [ ]
PCSR8	SLAVE PHY side-stream descrambler	146.3.4.3	See Equation (146–5)	M	Yes [ ]
PCSR9	Automatic polarity detection	146.3.4.4	Implemented in the PHY receiver	M	Yes [ ]

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146.11.4.1.3 PCS loopback

Item	Feature	Subclause	Value/Comment	Status	Support
PCSL1	PCS loopback	146.3.5	The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2 or the loopback bit in MDIO register 3.2278.14, defined in 45.2.3.70.2, is set to one	MDIO:M	Yes [ ] N/A [ ]
PCSL2	PCS loopback function	146.3.5	The PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII	M	Yes [ ]
PCSL3	PHY receive circuitry isolation	146.3.5	The PHY receive circuitry shall be isolated from the network medium	M	Yes [ ]
PCSL4	PHY transmit circuity isolation	146.3.5	The assertion of TX_EN at the MII shall not result in the transmission of data on the network medium	M	Yes [ ]

146.11.4.2 Physical Medium Attachment (PMA)

146.11.4.2.1 PMA function

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	PMA reset function	146.4.1	See 146.4.1	M	Yes [ ]
PMA2	PMA reset	146.4.1	Set pma_reset = TRUE while reset conditions hold true	M	Yes [ ]
PMA3	PMA Transmit fault function	146.4.2	Mapped to the transmit fault bit as specified in 45.2.1.7.4	MDIO:O	Yes [ ] No [ ] N/A [ ]
PMA4	PMA Receive fault function	146.4.3	Contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.232.7	MDIO:O	Yes [ ] No [ ] N/A [ ]
PMA5	LPI synchronization	146.4.4	EEE-capable PHYs synchronize refresh intervals during periods of low-power idle	EEE:M	Yes [ ] N/A [ ]
PMA6	PHY Control	146.4.4	See Figure 146–15, Figure 146–16, and Figure 146–17	M	Yes [ ]
PMA7	Link Monitor operation	146.4.5	See Figure 146–18	M	Yes [ ]
PMA8	Quiet-Refresh cycling state diagram	146.4.7	See Figure 146–19	EEE:M	Yes [ ] N/A [ ]

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146.11.4.2.2 PMA electrical specification

Item	Feature	Subclause	Value/Comment	Status	Support
PMAE1	Test modes	146.5.2	Implemented in PHY to allow testing transmitter electrical requirements	M	Yes [ ]
PMAE2	Enable test modes	146.5.2	Enable by setting bits 1.2296.15:13 as described in 45.2.1.233.1 when MDIO implemented; similar functionality provided otherwise	MDIO: M	Yes [ ] N/A [ ]
PMAE3	These test modes shall change only the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation	146.5.2		M	Yes [ ]
PMAE4	Test mode 1	146.5.2	When enabled, PHY repeatedly transmits the data symbol sequence (+1, –1)	M	Yes [ ]
PMAE5	Test mode 2	146.5.2	When enabled, PHY repeatedly transmits ten “+1” symbols followed by ten “–1” symbols	M	Yes [ ]
PMAE6	Test mode 3	146.5.2	Transmit as in non-test operation and in the MASTER data mode with data set to normal Inter-Frame idle signals	M	Yes [ ]
PMAE7	TX_TCLK	146.5.3	PHY to provide access to the symbol rate clock	M	Yes [ ]
PMAE8	AC coupling at MDI	146.5.4		M	Yes [ ]
PMAE9	The transmitter shall meet the requirements of this subclause with a 100 Ω ± 0.1% resistive differential load connected to the transmitter output	146.5.4		M	Yes [ ]
PMAE10	Transmitter output voltage	146.5.4.1	2.4 V + 5%/– 15% peak-to-peak in the 2.4 Vpp operating mode when measured on test mode 1, 1.0 V + 5%/– 15% peak-to-peak in the 1.0 Vpp operating mode when measured on test mode 1	RTDL: M	Yes [ ] N/A [ ]
PMAE11	Transmitter output droop	146.5.4.2	Less than 10%	M	Yes [ ]
PMAE12	Transmitter timing jitter	146.5.4.3	Less than 10 ns symbol-to-symbol jitter when measured on test mode 1	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PMAE13	Transmit power in test mode 3	146.5.4.4	8.6 ± 1.0 dBm for the 2.4 Vpp transmit amplitude, and 1 ± 1.2 dBm for the 1.0 Vpp transmit amplitude, when measured into a 100 Ω load using the test fixture shown in Figure 146–21	M	Yes [ ]
PMAE14	Transmit power spectral density in test mode 3	146.5.4.4	Between the upper and lower masks specified in Equation (146–6) and Equation (146–7) for the 2.4 Vpp transmit amplitude and Equation (146–8) and Equation (146–9) for the 1.0 Vpp transmit amplitude, when measured into a 100 Ω load using the test fixture shown in Figure 146–21	M	Yes [ ]
PMAE15	Transmitter clock frequency	146.5.4.5	Within the range of 7.5 MBd ± 50 ppm	M	Yes [ ]
PMAE16	LPI mode the short-term rate of frequency variation	146.5.4.5	Less than 0.1 ppm/second	EEE:M	Yes [ ] N/A [ ]
PMAE17	PMA receive function	146.5.5	Requirements met using link segment defined in 146.7	M	Yes [ ]
PMAE18	Receiver differential input signals	146.5.5.1	Received with a bit error ratio less than 10^{-9}	M	Yes [ ]
PMAE19	Receiver frequency tolerance	146.5.5.2	Within the range of 7.5 MBd ± 50 ppm	M	Yes [ ]
PMAE20	Alien crosstalk noise rejection	146.5.5.3	BER < 10^{-9} with an alien crosstalk noise of magnitude of –106 dBm/Hz and bandwidth of 10 MHz at the MDI	M	Yes [ ]
PMAE21	PMA local loopback	146.5.6	The PMA shall be placed in loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, or in MDIO register 1.2294.0, defined in 45.2.1.231.6 is set to one	MDIO:O	Yes [ ] No [ ] N/A [ ]

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146.11.4.3 Management interface

Item	Feature	Subclause	Value/Comment	Status	Support
MI1	Auto-Negotiation	146.1.2, 146.6.1	Clause 98 is used if Auto-Negotiation is supported and enabled	AN:M	Yes [ ] N/A [ ]
MI2	MASTER-SLAVE relationship when Auto-Negotiation is not used	146.1.2	Established by management or hardware configuration of the PHYs	M	Yes [ ]
MI3	MASTER/SLAVE mode selection	146.6.3	Default setting chosen by Auto-Negotiation, by setting bits 1.2100.14 as described in 45.2.1.214 when MDIO is implemented; similar functionality provided otherwise	AN:M MDIO:M	Yes [ ] N/A [ ]
MI4	Transmitter output voltage setting	146.6.4	Default setting chosen by Auto-Negotiation, by setting bit 1.2294.12 as described in 45.2.1.231.3 when MDIO implemented; similar functionality provided otherwise	RTDL:O	Yes [ ] No [ ] N/A [ ]
MI5	Increased transmit level request	146.6.4	Bit A23 contains a one if the PHY is requesting the increased transmit level; otherwise, bit A23 contains a zero	RTDL:O AN:M	Yes [ ] No [ ] N/A [ ]
MI6	Increased transmit level support	146.6.4	Bit A24 contains a one if the PHY is supporting and advertising the 2.4 Vpp operating mode; otherwise, bit A24 contains a zero	RTDL:O AN:M	Yes [ ] No [ ] N/A [ ]
MI7	Increased transmit level selection	146.6.4	If both PHYs advertise increased transmit/receive ability and at least one PHY requests an increased transmit level, the 2.4 Vpp operating mode is selected; otherwise, the 1.0 Vpp operating mode is selected	RTDL:O AN:M	Yes [ ] No [ ] N/A [ ]
MI8	Energy Efficient Ethernet ability	146.6.5	Bit A25 contains a one if Energy Efficient Ethernet is supported and advertised; otherwise, bit A25 contains a zero	EEE:M AN:M	Yes [ ] N/A [ ]
MI9	PMA and PCS MDIO function mapping	146.6.6	See Table 146–4 when MDIO is implemented; similar functionality provided otherwise	MDIO:M	Yes [ ] N/A [ ]

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146.11.4.4 Link Segment characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
LMF1	Insertion loss (1.0 Vpp operating mode)	146.7.1.1.2	See Equation (146–11)	INS:M	Yes [ ]
LMF2	Insertion loss (2.4 Vpp operating mode)	146.7.1.1.1	See Equation (146–10)	INS:O, RTDL:M	Yes [ ] N/A[]
LMF3	Return loss	146.7.1.2	See Equation (146–12)	INS:M	Yes [ ]
LMF4	Maximum link delay	146.7.1.3	Not exceed 8834 ns for all frequencies between 1 MHz to 20 MHz	INS:M	Yes [ ]
LMF5	Differential-to-common-mode conversion	146.7.1.4	See Table 146–5	INS:M	Yes [ ]
LMF6	Coupling attenuation	146.7.1.5	See Table 146–6	INS:M	Yes [ ]
LMF7	Power sum ANEXT loss between a disturbed 10BASE-T1L link segment and the disturbing 10BASE-T1L link segment	146.7.2.1	See Equation (146–14) or 60 dB, whichever is less	INS:M	Yes [ ]
LMF8	Power sum AFEXT loss between a disturbed 10BASE-T1L link segment and the disturbing 10BASE-T1L link segment	146.7.2.2	See Equation (146–16) or 60 dB, whichever is less	INS:M	Yes [ ]

146.11.4.5 MDI specifications

Item	Feature	Subclause	Value/Comment	Status	Support
MDI1	Mated MDI performance	146.8.2	Electrical requirements specified in 146.5.4 and 146.5.5 shall be met when the PHY is connected to the MDI connector mated with the specified plug connector	M	Yes [ ]
MDI2	MDI Return Loss	146.8.3	Meets or exceeds Equation (146–17)	M	Yes [ ]
MDI3	MDI Mode conversion loss	146.8.4	Meets or exceeds Equation (146–18)	M	Yes [ ]
MDI4	MDI line powering voltage tolerance	146.8.5	Up to 60 V DC with the source current limited to 2000 mA	M	Yes [ ]
MDI5	MDI fault tolerance	146.8.6	Withstand without damage the application of a short circuit of any wire to the other wire of the same pair or ground potential, operation resumes after removing the short(s)	M	Yes [ ]

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146.11.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	146.9.1	Conform to the general safety requirements in J.2 or IEC 61010-1, as appropriate	M	Yes [ ]

146.11.4.7 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	10BASE-T1L PHY associated with MII	146.10	Comply with the bit delay constraints for full duplex operation	M	Yes [ ]
DC2	Transmit path delay	146.10	Less than 3.2 μs (32 bit times)	M	Yes [ ]
DC3	Receive path delay	146.10	Less than 6.4 μs (64 bit times)	M	Yes [ ]

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147. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S

147.1 Overview

This clause defines the type 10BASE-T1S Physical Coding Sublayer (PCS) and type 10BASE-T1S Physical Medium Attachment (PMA) sublayer. Together, the PCS and PMA sublayers comprise a 10BASE-T1S Physical Layer device (PHY). Provided in this clause are full functional and electrical specifications for the type 10BASE-T1S PCS, PMA, and MDI.

The 10BASE-T1S PHY is specified to be capable of operating at 10 Mb/s in several modes. All 10BASE-T1S PHYs can operate as a half-duplex PHY with a single link partner over a point-to-point link segment defined in 147.7, and, additionally, there are two mutually exclusive optional operating modes: a full-duplex point-to-point mode over the link segment, defined in 147.7, and a half-duplex shared-medium mode, referred to as multidrop mode, capable of operating with multiple stations connected to a mixing segment, defined in 147.8. The medium supporting the operation of the 10BASE-T1S PHY is defined in terms of performance requirements between the attachment points (Medium Dependent Interface (MDI)), allowing implementers to specify their own media to operate the 10BASE-T1S PHY as long as the normative requirements included in this clause are met.

10BASE-T1S PHYs optionally support PHY Level Collision Avoidance (PLCA), described in Clause 148.

10BASE-T1S follows an integrated PCS and PMA architecture and therefore does not support an AUI (see Figure 1–1).

147.1.1 Relationship of 10BASE-T1S to other standards

The relationship between the 10BASE-T1S, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet model are shown in Figure 147–1. The PHY sublayers (shown shaded) in Figure 147–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto-Negotiation for 10BASE-T1S is defined in Clause 98 and is not available in multidrop mode. Selection between multidrop and point-to-point mode is made via the appropriate configuration bit. A Management Entity is required using MDIO or equivalent functionality. Optional MDIO is defined in Clause 45.

147.1.2 Operation of 10BASE-T1S

All 10BASE-T1S PHYs can operate using half-duplex point-to-point communications on a link segment using a single balanced pair of conductors, supporting up to four in-line connectors and up to at least 15 meters in reach, with an effective data rate of 10 Mb/s shared between the two directions of transmission. 10BASE-T1S PHYs supporting the option of full-duplex point-to-point operation may operate with an effective data rate of 10 Mb/s in each direction simultaneously, supporting up to four in-line connectors and up to at least 15 meters in reach.

Additionally, the 10BASE-T1S PHY may operate using half-duplex communications on a mixing segment using a single balanced pair of conductors, interconnecting up to at least 8 PHYs to a trunk up to at least 25 m. PHYs may be attached in-line with the trunk or at the end of stubs with a length of up to 10 cm. An overall effective data rate of 10 Mb/s is shared among the nodes. Larger PHY count and reach may be achieved provided the mixing segment specifications in 147.8 are met.

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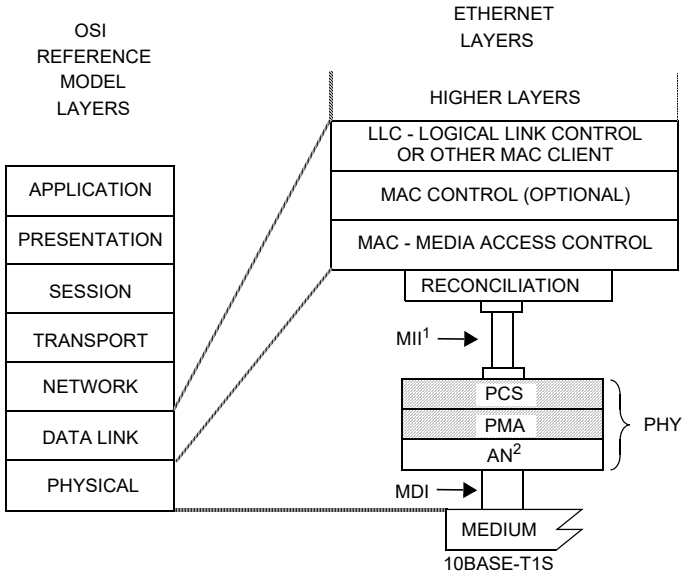
The 10BASE-T1S PHY utilizes two level Differential Manchester Encoding (DME). A 17-bit self-synchronizing scrambler is used to improve the EMC performance. Following scrambling of the data, 4B/5B encoding is performed (see 147.3.2.4). DME is a self-clocked and intrinsically balanced line coding that guarantees very low DC baseline wander and allows for robust clock and data recovery in noisy environments. The 4B/5B mapping and the scrambler are contained within the PCS (see 147.3) while the DME encoder/decoder is contained in the PMA (see 147.4).



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE

NOTE 1—MII is optional
NOTE 2—Auto-Negotiation is optional

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

Figure 147–1—Relationship of 10BASE-T1S PHY to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

147.1.3 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

147.1.3.1 State diagram notation

The conventions of 21.5 are adopted with the extension that some states in the state diagrams use an IF-THEN-ELSE-END construct to condition which actions are taken within the state. If the logical expression associated with the IF evaluates TRUE, all the actions listed between THEN and ELSE will be executed. In the case where ELSE is omitted, the actions listed between THEN and END will be executed. If the logical expression associated with the IF evaluates FALSE, the actions listed between ELSE and END will be executed. After executing the actions listed between THEN and ELSE, between THEN and END, or between ELSE and END, the actions following the END, if any, will be executed.

147.1.3.2 State diagram timer specifications

All timers operate in the manner described in 40.4.5.2.

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147.1.3.3 Service specifications

The method and notation used in the service specification follows the conventions of 1.2.2.

147.2 Service primitives and interfaces

The 10BASE-T1S PHY uses the service primitives and interfaces in 40.2, with exception of the following clarifications and differences noted in this subclause. Figure 147–2 shows the relationship of the service primitives and interfaces used by the 10BASE-T1S PHY.

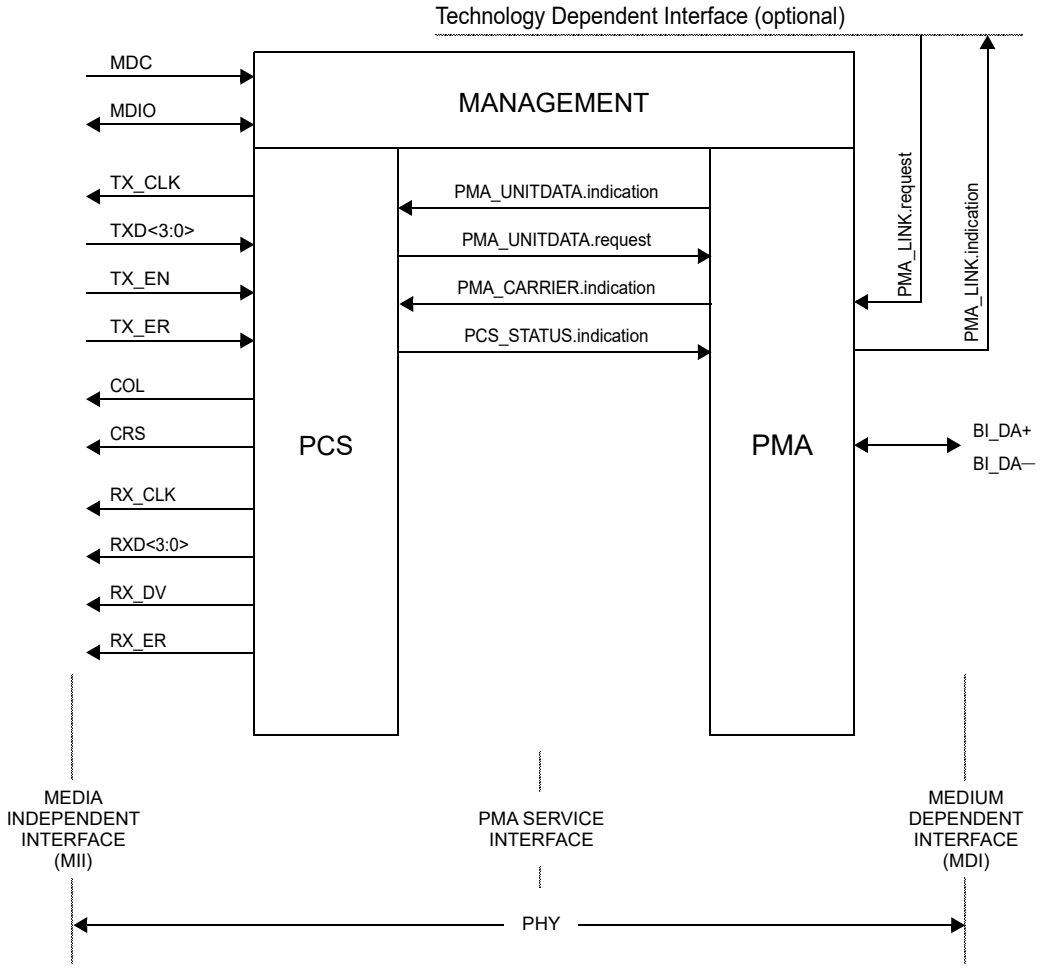

Figure 147–2—10BASE-T1S PHY interfaces

The 10BASE-T1S PHY uses the Media Independent Interface (MII) as specified in Clause 22.

As shown in Figure 147–2, 10BASE-T1S uses the following service primitives to exchange symbol vectors, status indications, and control signals across the PMA service interface:

PMA_UNITDATA.indication (rx_sym)
PMA_UNITDATA.request (tx_sym)
PMA_CARRIER.indication (pma_crs)
PMA_LINK.indication (link_status)

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PMA_LINK.request (link_control)

PCS_STATUS.indication (pcs_status)

147.2.1 PMA_UNITDATA.indication

This primitive defines the transfer of one 5B symbol in the form of the rx_sym parameter from the PMA to the PCS.

147.2.1.1 Semantics of the primitive

PMA_UNITDATA.indication (rx_sym)

During reception, the PMA_UNITDATA.indication conveys to the PCS, via the parameter rx_sym, the value of the 5B symbol detected on the MDI during each cycle of the recovered clock.

147.2.1.2 When generated

The PMA generates PMA_UNITDATA.indication (rx_sym) messages synchronously for every 5B symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is 2.5 MHz, as governed by the recovered clock.

147.2.1.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

147.2.2 PMA_UNITDATA.request

This primitive defines the transfer of one symbol in the form of the tx_sym parameter from the PCS to the PMA.

The symbol is obtained in the PCS Transmit function using the encoding rules defined in 147.3.2 to represent 4B/5B encoded MII data or special out of band signaling.

147.2.2.1 Semantics of the primitive

PMA_UNITDATA.request (tx_sym)

During transmission, the PMA_UNITDATA.request conveys the value of the symbol to be sent over the MDI, via the parameter tx_sym.

The tx_sym parameter is one of the allowed 5B codes specified in Table 147–1.

147.2.2.2 When generated

The PCS generates PMA_UNITDATA.request (tx_sym) synchronously with every symb_timer expiration. The symb_timer is defined in 147.3.2.6.

147.2.2.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated 5B symbol after processing it with DME following the rules in 147.4.

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147.2.3 Mapping of PMA_CARRIER.indication

Reports whether a signal compatible with DME encoding rules specified in 147.4.2 is detected on the medium.

147.2.3.1 Function

Maps the primitive PMA_CARRIER.indication to the MII CRS signal.

147.2.3.2 Semantic of the service primitive

PMA_CARRIER.indication (pma_crs)

The pma_crs parameter can take one of two values: CARRIER_ON or CARRIER_OFF.

The pma_crs parameter is set to CARRIER_ON if a signal compatible with DME encoding rules specified in 147.4.2 is present on the medium. Otherwise, the pma_crs parameter is set to CARRIER_OFF.

147.2.3.3 When generated

The PMA_CARRIER.indication primitive is generated continuously by the PMA sublayer.

147.2.4 PMA_LINK.request

This primitive allows Auto-Negotiation to enable and disable operation of the PMA, as specified in 98.4.2.

147.2.4.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of the following two values:

DISABLE	Used by Auto-Negotiation function to disable the PHY.
ENABLE	Used by Auto-Negotiation function to enable the PHY.

147.2.4.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in 98.4.

147.2.5 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 98.4.1. This primitive informs Auto-Negotiation functions about the status of the underlying link.

147.2.5.1 Semantics of the primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on the following two values:

FAIL	No valid link established.
OK	The Link Monitor function indicates that a valid 10BASE-T1S link is established. Reliable reception of signals transmitted from the remote PHY is possible.

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147.2.5.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 147–14.

147.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 98.4.1.

147.2.6 PCS_STATUS.indication

This primitive is generated by the PCS to indicate PCS status to the PMA.

147.2.6.1 Semantics of the primitive

PCS_STATUS.indication (pcs_status)

The pcs_status parameter can take on the following two values:

NOT_OK	PCS is not receiving valid packets or heartbeat signals from the remote PHY.
OK	PCS is actively receiving valid packets and/or heartbeat signals from the remote PHY.

147.2.6.2 When generated

The PCS generates this primitive continuously. The pcs_status parameter is set according to the state diagram in Figure 147–11.

147.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 147.4.4.

147.3 Physical Coding Sublayer (PCS) functions

The Physical Coding Sublayer (PCS) consists of PCS Reset, PCS Transmit, and PCS Receive functions as shown in Figure 147–3. The PCS Reset function is explained in 147.3.1, the PCS Transmit function is explained in 147.3.2, the PCS Receive function is explained in 147.3.3, and the PCS Loopback function is explained in 147.3.4.

147.3.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever any of the following conditions occur:

a) Power on causes power_on = TRUE (see 36.2.5.1.3) while pcs_reset = FALSE.
b) The receipt of a request for reset from the management entity (bit 3.2291.15 defined in 45.2.3.72.1), independently from the current state of pcs_reset.

All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. PCS Reset shall keep pcs_reset = TRUE until the complete execution of the PCS Reset function, after which it is set to pcs_reset = FALSE. The reference diagrams do not explicitly show the PCS Reset function.

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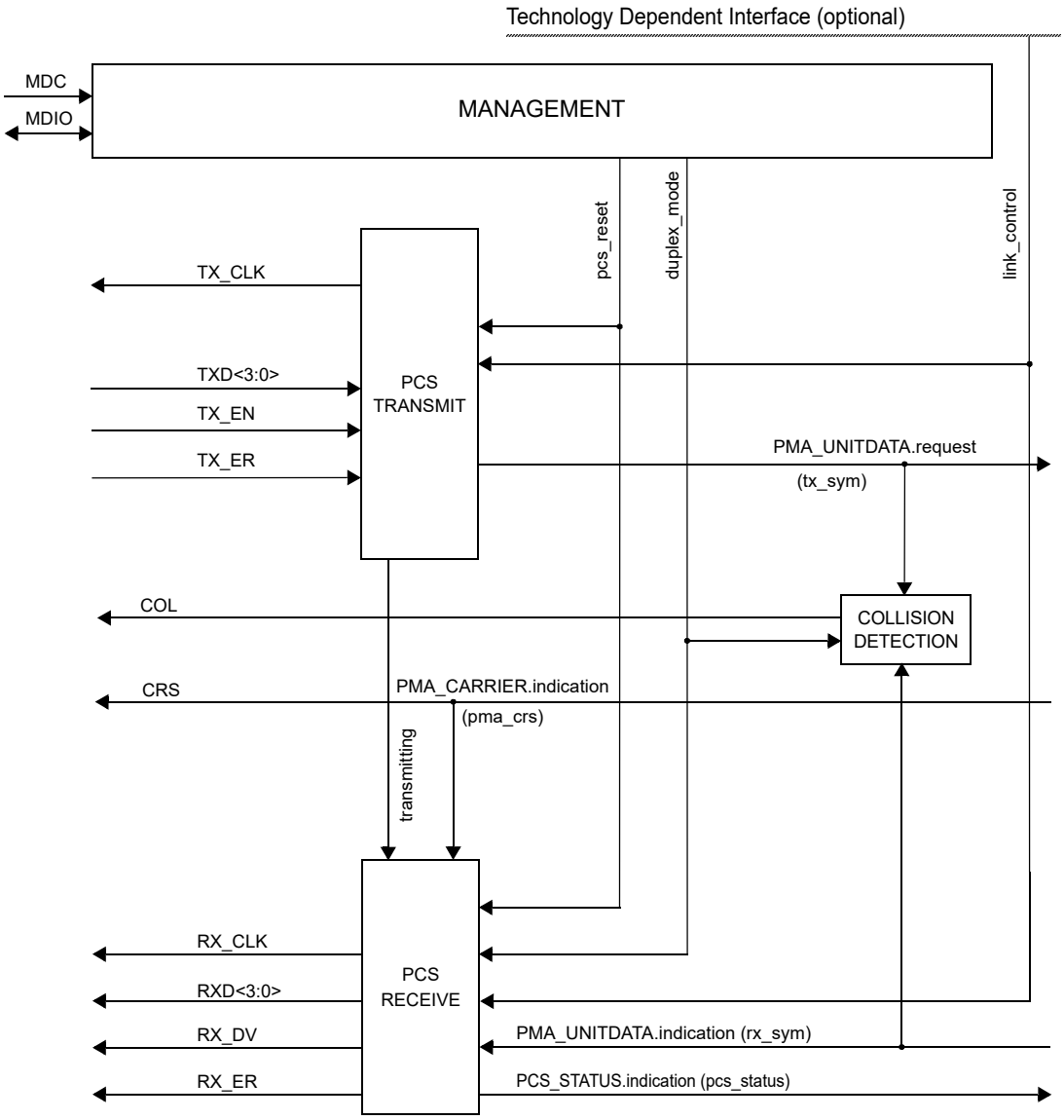

Figure 147–3—PCS reference diagram

147.3.2 PCS Transmit

147.3.2.1 PCS Transmit overview

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 147–4 and Figure 147–5, and the associated state variables, functions, timers, and messages.

At each symbol period, PCS Transmit generates a symbol tx_sym conveyed to the PMA through the PMA_UNITDATA.request service primitive, where tx_sym is a 5B symbol. The PMA encodes tx_sym, LSB first, into a DME stream over the wire pair BI_DA as specified in Table 147–2.

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Upon assertion of TX_EN, the PCS Transmit function passes two SYNC symbols to the PMA, followed by two SSD symbols that replace the first 16 bits of the packet preamble. Following the second SSD, TXD<3:0> is encoded into 5B symbols using the encoding rules specified in Table 147–1, until TX_EN is deasserted.

Following the deassertion of TX_EN, the PCS Transmit generates a special code ESD. When there is no transmit error, ESD is followed by ESDOK. When there is a transmit error, ESD is followed by ESDERR. When a jabber condition is detected, ESD is followed by ESDJAB.

The 10BASE-T1S PHY has one special 5B symbol 'I' (see Table 147–1) which represents SILENCE. SILENCE represents an indication for the PMA to change the output according to 147.4.2.

147.3.2.2 Variables

err

This variable is set in the PCS Transmit state, as described in Figure 147–4 and Figure 147–5.
This variable is used to detect and latch a TX_ER = TRUE condition during data transmission; if such error is detected, an ESDERR symbol is sent at the end of transmission.
Values: TRUE or FALSE

hb_cmd

See 147.3.7.1.1.

link_control

This variable is generated by the Auto-Negotiation function. When Auto-Negotiation is not present or Auto-Negotiation is disabled, link_control has a default value of ENABLE, and may be provided by implementation-dependent functionality. When set to DISABLE, all PCS functions are switched off and no data can be sent or received.
Values: ENABLE or DISABLE

pcs_reset

The pcs_reset parameter set by the PCS Reset function.
Values: TRUE or FALSE

TX_EN

The TX_EN signal of the MII as specified in 22.2.2.3.
When set to FALSE transmission is disabled.
When set to TRUE transmission is enabled.
Values: TRUE or FALSE

TX_ER

The TX_ER signal of the MII as specified in 22.2.2.5.
When set to FALSE it indicates a non-errored transmission.
When set to TRUE it indicates an errored transmission.
Values: TRUE or FALSE

TXD

The TXD signal of the MII as specified in 22.2.2.4.
This signal represents a 4B data nibble to be transmitted.

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tx_cmd

Encoding present on TXD<3:0>, TX_ER, and TX_EN as defined in Table 22–1.
Values:
BEACON: PLCA BEACON indication encoding present on TXD<3:0>, TX_ER, and TX_EN.
COMMIT: PLCA COMMIT indication encoding present on TXD<3:0>, TX_ER, and TX_EN.
SILENCE: TXD<3:0> does not encode any of the above requests, or TX_ER = FALSE, or TX_EN = TRUE.

tx_sym

5B symbol to be conveyed to the PMA Transmit function by the means of the PMA_UNITDATA.request primitive specified in 147.2.2.

transmitting

This variable is set in the PCS Transmit state, as described in Figure 147–4.
When this variable is set to TRUE, it indicates a transmission is ongoing.
Values: TRUE or FALSE

147.3.2.3 Constants

SYNC / COMMIT

5B symbol defined as 'J' in 4B/5B encoding.

SSD

5B symbol defined as 'H' in 4B/5B encoding.

ESD

5B symbol defined as 'T' in 4B/5B encoding.

ESDERR

5B symbol defined as 'K' in 4B/5B encoding.

ESDOK / ESDBRS

5B symbol defined as 'R' in 4B/5B encoding.

SILENCE

5B symbol defined as 'I' in 4B/5B encoding.

ESDJAB

5B symbol defined as 'S' in 4B/5B encoding.

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147.3.2.4 Functions

ENCODE

This function takes a 4 bit input parameter Sc_n<3:0> and returns a 5B symbol according to the following procedure:

1. Convert Sc_n<3:0> into Sd_n<3:0> as specified in 147.3.2.8.
2. Convert Sd_n<3:0> (4B symbol) into the corresponding 5B symbol defined in Table 147–1.

Table 147–1—4B/5B Encoding

Name	4B	5B	Special function
0	0000	11110	—
1	0001	01001	—
2	0010	10100	—
3	0011	10101	—
4	0100	01010	—
5	0101	01011	—
6	0110	01110	—
7	0111	01111	—
8	1000	10010	—
9	1001	10011	—
A	1010	10110	—
B	1011	10111	—
C	1100	11010	—
D	1101	11011	—
E	1110	11100	—
F	1111	11101	—
I	N/A	11111	SILENCE
J	N/A	11000	SYNC / COMMIT
K	N/A	10001	ESDERR
T	N/A	01101	ESD / HB
R	N/A	00111	ESDOK / ESDBRS
H	N/A	00100	SSD
N	N/A	01000	BEACON
S	N/A	11001	ESDJAB

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TXCMD_ENCODE

In the PCS transmit process, this function takes as its arguments the values of tx_cmd and hb_cmd variables and returns a 5B symbol based on the following mapping:
'N' when the tx_cmd variable is set to BEACON,
'J' when the tx_cmd variable is set to COMMIT,
'T' when the hb_cmd variable is set to HEARTBEAT and the tx_cmd variable is not set to BEACON or COMMIT,
'I' otherwise.

147.3.2.5 Abbreviations

STD — Alias for symb_timer_done.

147.3.2.6 Timers

symb_timer

A continuous free-running timer. PMA_UNITDATA.request messages are issued by the PCS concurrently with symb_timer_done (see 147.2.2). TX_CLK (see 22.2.2.1) shall be generated from symb_timer with the rising edge of TX_CLK generated synchronously with symb_timer_done.
Continuous timer: The condition symb_timer_done becomes true upon timer expiration.
Restart time: Immediately after expiration.
Duration: 400 ns ± 100 ppm (see 22.2.2.1)

unjab_timer

Optionally times the minimum duration the PHY suppresses any transmission before reverting to normal operations.
Duration: 16 ms ± 100 μs

xmit_max_timer

Defines the maximum time the PCS Transmit state diagram can stay in DATA state.
The xmit_max_timer shall be implemented in such a way that, upon expiration, an even number of nibbles has been sent to prevent the MAC from counting false alignment errors.
Duration: 2 ms ± 100 μs
NOTE—This is approximately 25% greater than maxEnvelopeFrameSize specified in 4.2.7.1.

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147.3.2.7 State diagram

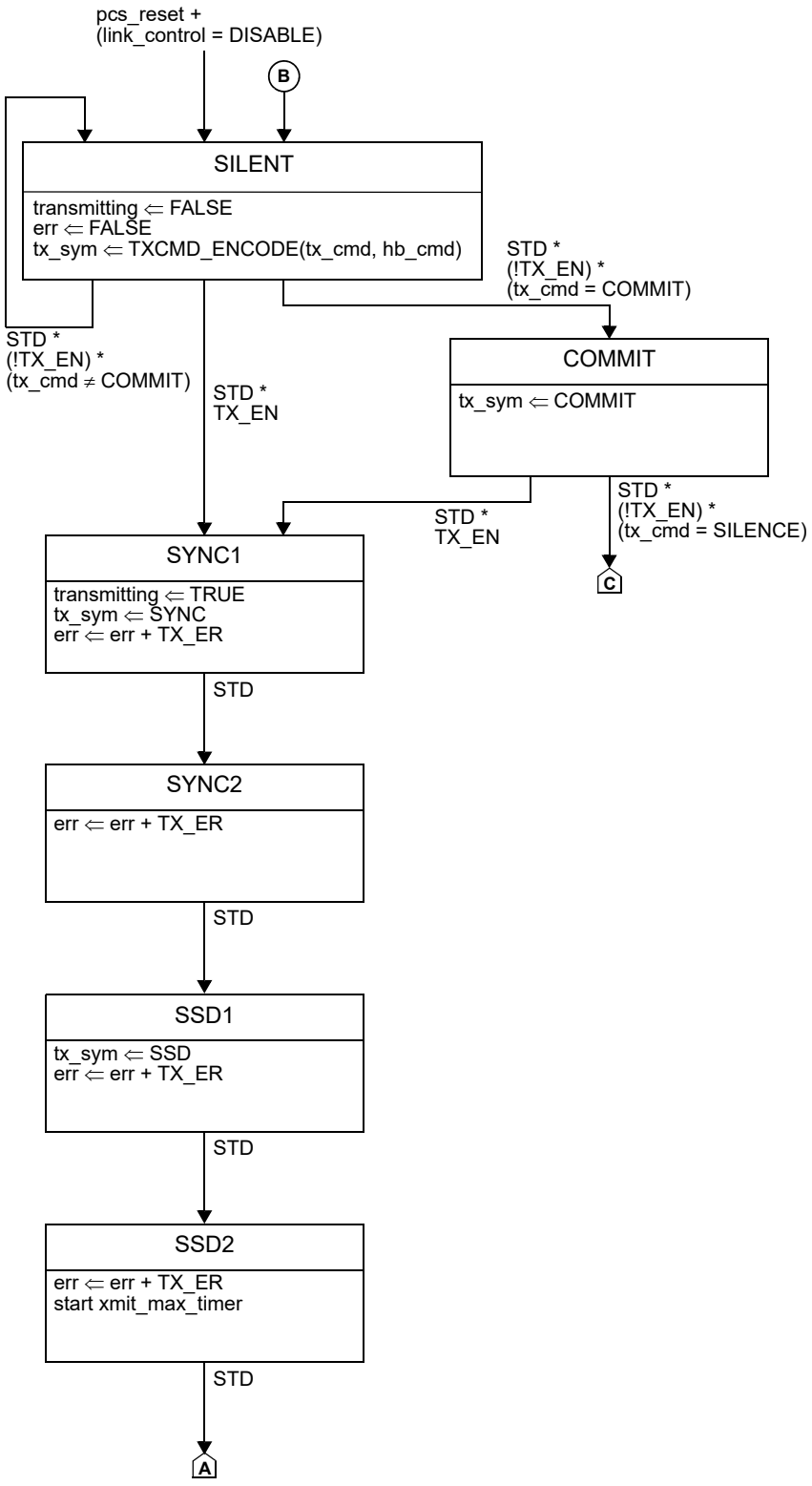

Figure 147–4—PCS Transmit state diagram, part a

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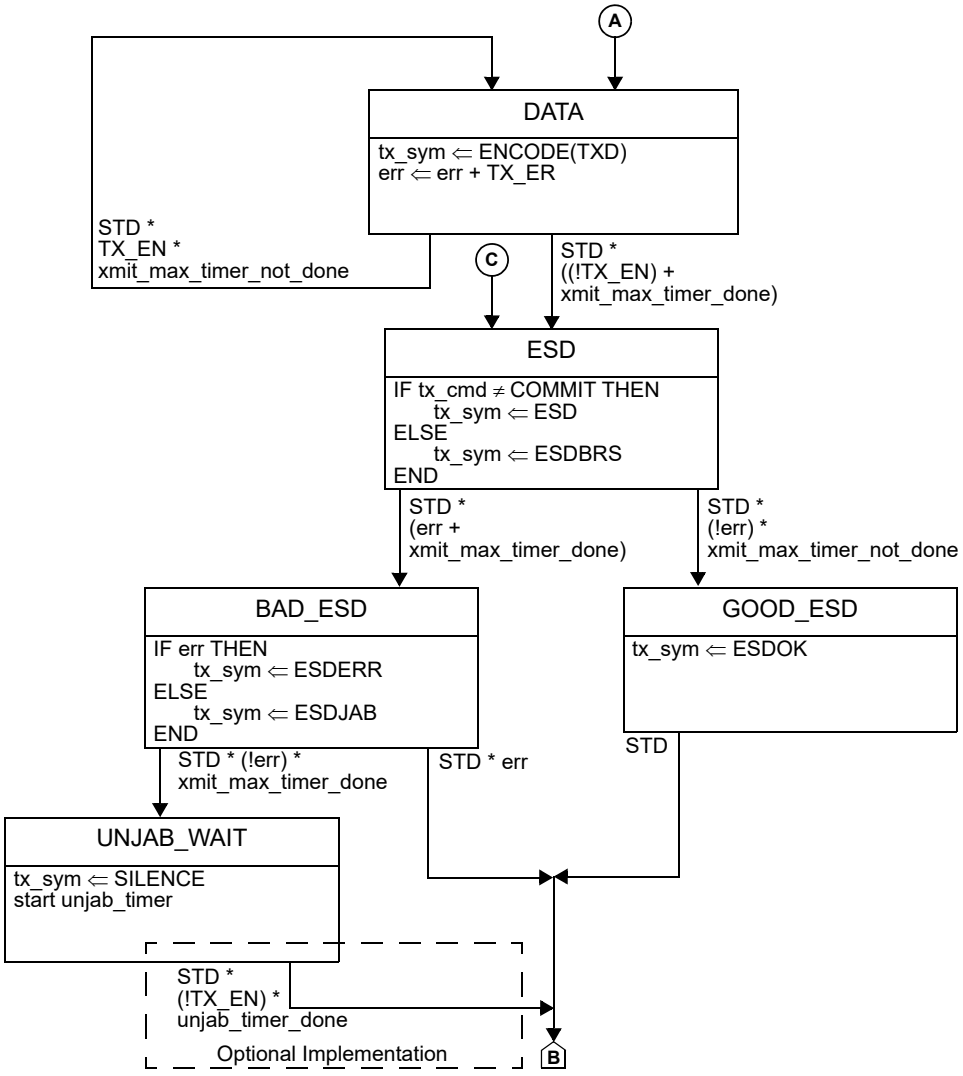

Figure 147–5—PCS Transmit state diagram, part b

147.3.2.8 Self-synchronizing scrambler

The PCS Transmit function shall implement multiplicative scrambling using the following generator polynomial $g(x) = x^{17} + x^{14} + 1$.

An implementation of a self-synchronizing scrambler by a linear-feedback shift register is shown in Figure 147–6. The bits stored in the shift register delay line at time n are denoted by Scr_n<16:0>. The '+' symbol denotes the exclusive-OR logical operation. When Sc_n<3:0> is presented at the input of the scrambler, Sd_n<3:0> is produced by shifting in each bit of Sc_n<3:0> as Sc_n<i>, with i ranging from 0 to 3 (i.e., LSB first). The scrambler is reset upon execution of the PCS Reset function. If the PCS Reset is executed, all bits of the 17-bit vector representing the self-synchronizing scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros. At every STD, if no data is presented at the scrambler input via Sc_n<3:0>, the scrambler may be fed with arbitrary inputs.

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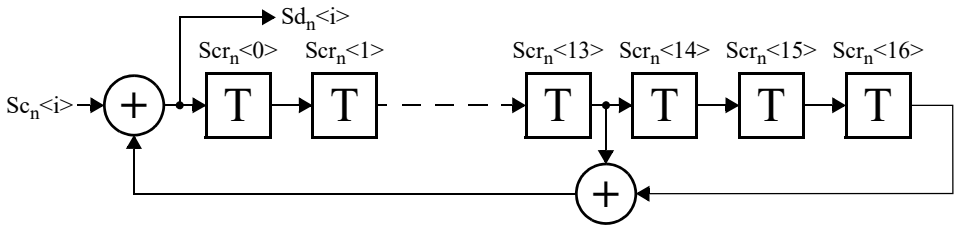

Figure 147–6—Self-synchronizing scrambler

147.3.2.9 Jabber functional requirements

The PCS Transmit function contains the capability to interrupt a transmission that exceeds a time duration determined by xmit_max_timer. If the packet being transmitted continues longer than the specified time duration, the PCS Transmit sends an ESD, ESDJAB symbol sequence to notify the receivers, then it inhibits further transmissions for at least the duration of unjab_timer. The PCS Transmit may return to normal operation automatically after unjab_timer elapsed and the error condition has been cleared, or it may keep silent until reset.

147.3.3 PCS Receive

147.3.3.1 PCS Receive overview

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 147–7 and Figure 147–8, and associated state variables.

The state diagram defined in Figure 147–7 is triggered by the reception of a SYNC symbol from the PMA Receive function and waits for two SSD symbols to start regenerating the packet preamble whose start has been replaced with the SYNC, SYNC, SSD, SSD sequence by the PCS Transmit function as described in Figure 147–4. After the second SSD is received, the PCS Receive function discards the next nine symbols. These symbols can be used to achieve lock of the self-synchronizing descrambler.

During the descrambler locking time, the special value 5 is conveyed to the MII via the RXD variable in order to rebuild the original preamble transmitted by the MAC.

The DATA state, in which 5B symbols are decoded into MII data, is left when ESD or ESDBRS followed by either ESDOK, ESDERR, or ESDJAB symbol is encountered, or when the PMA detects SILENCE on the media (e.g., the transmitter prematurely stops data transmission).

During the WAIT_SYNC state, the PCS notifies the RS of a received BEACON indication by the means of the MII as specified in 22.2.2.8. When a sequence of at least two consecutive 'N' symbols is received, the MII signals RX_DV, RX_ER, and RXD<3:0> are set to the BEACON indication as shown in Table 22–2. Additionally, the PCS notifies the RS of a received COMMIT indication by the means of the MII as specified in 22.2.2.8. When a sequence of at least two consecutive SYNC is received, the MII signals RX_DV, RX_ER, and RXD<3:0> are set to the COMMIT indication as shown in Table 22–2.

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147.3.3.2 Variables

duplex_mode

This variable indicates whether the PHY is configured for full-duplex operation (DUPLEX_FULL) or half-duplex operation (DUPLEX_HALF). If Multidrop mode MDIO register bit 1.2297.10 is set to one and multidrop mode is supported according to bit 1.2298.10 then duplex_mode is set to DUPLEX_HALF. Else, if Auto-Negotiation is enabled then duplex_mode is set by the priority resolution defined in 98B.4. Otherwise, this variable is set by MDIO register bit 3.2291.8. If MDIO is not implemented, duplex_mode is set by equivalent means.
Values: DUPLEX_FULL or DUPLEX_HALF

link_control

See 147.3.2.2.

multidrop

See 147.3.7.1.1.

precnt

Counter for preamble regeneration.

rx_cmd

See 147.3.7.1.1.

RX_DV

The RX_DV signal of the MII as specified in 22.2.2.7.

RX_ER

The RX_ER signal of the MII as specified in 22.2.2.10.

RXD

PCS decoded data synchronous to RX_CLK as specified in 22.2.2.8.

pcs_reset

See 147.3.2.2.

RXn

The rx_sym parameter of the PMA_UNITADATA.indication primitive defined in 147.2.1.
The 'n' subscript denotes the rx_sym conveyed in the most recent recv_symb_conv_timer cycle.
The 'n-x' subscript indicates the rx_sym conveyed 'x' cycles before the most recent one.

transmitting

See 147.3.2.2.

147.3.3.3 Constants

fc_supported

Indicates whether the optional False Carrier detection is supported.
Values: TRUE or FALSE

BEACON

5B symbol defined as 'N' in 4B/5B encoding.

HB

5B symbol defined as 'T' in 4B/5B encoding.

See also 147.3.2.3.

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147.3.3.4 Functions

DECODE

This function takes a 5B symbol input parameter and returns a 4 bit value Dc_n<3:0> value according to the following procedure:
1. Convert the 5B input symbol into Dr_n<3:0> by performing a reverse lookup in Table 147–1. If no 4B value is associated to the given 5B symbol, the PCS Receive function shall assert RX_ER for at least one symbol period and Dr_n<3:0> may be set arbitrarily.
2. Convert Dr_n<3:0> to Dc_n<3:0> as specified in 147.3.3.8.

147.3.3.5 Abbreviations

RSCD Alias for recv_symb_conv_timer_done.

147.3.3.6 Timers

recv_symb_conv_timer

A continuous timer which expires when the PMA_UNITDATA.indication message is generated (see 147.2.1).
Continuous timer: The condition recv_symb_conv_timer_done becomes true upon timer expiration.
Restart time: Immediately after expiration.
Duration: timed by the PMA_UNITDATA.indication message generation.

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147.3.3.7 State diagrams

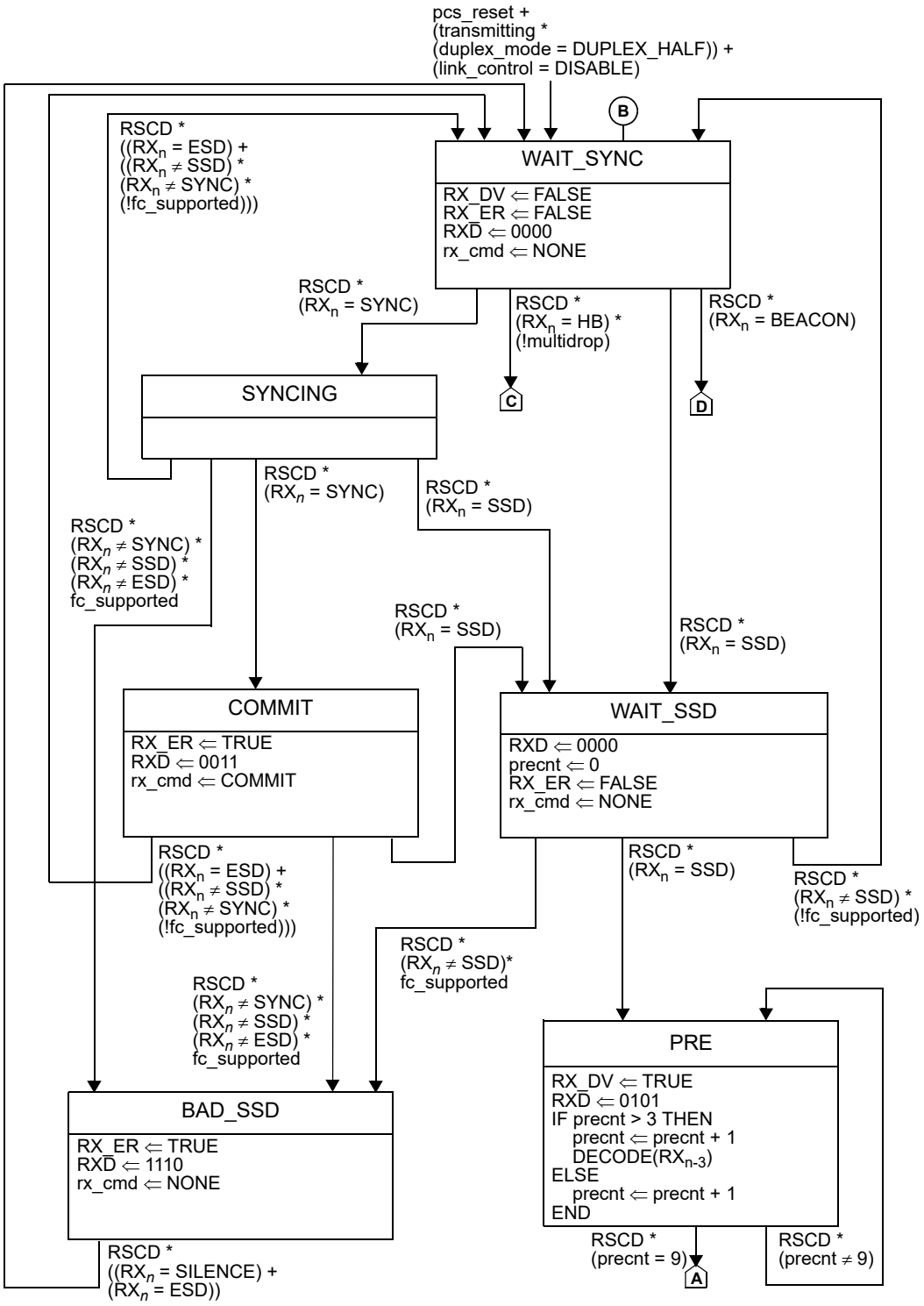

Figure 147–7—PCS Receive state diagram, part a

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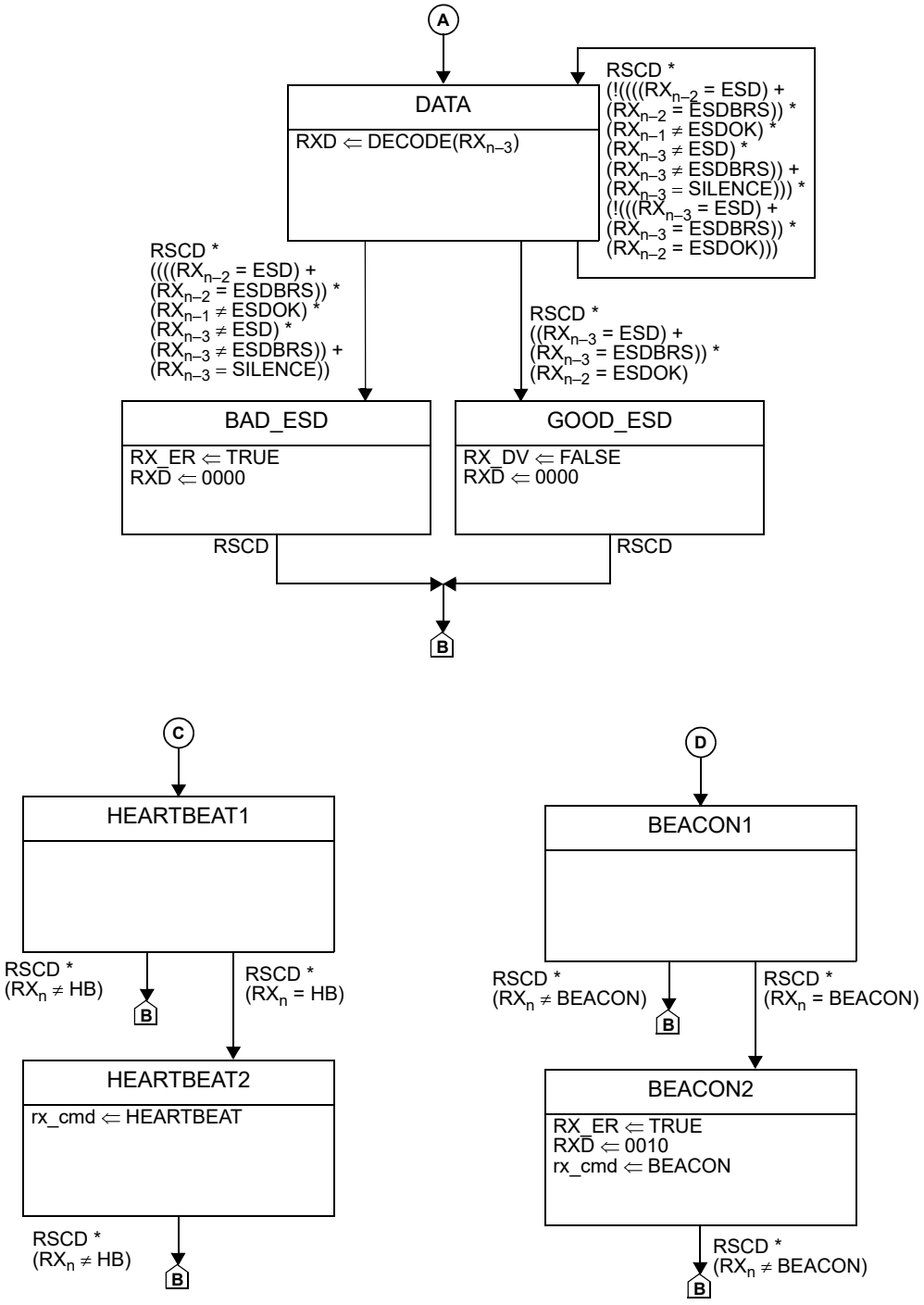

Figure 147–8—PCS Receive state diagram, part b

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147.3.3.8 Self-synchronizing descrambler

The PCS Receive function descrambles the 5B/4B decoded data stream and returns the value of RXD<3:0> to the MII. The descrambler shall employ the polynomial $g(x)$ defined in 147.3.2.8. The implementation of the self-synchronizing descrambler by linear-feedback shift register is shown in Figure 147–9. The bits stored in the shift register delay line at time n are denoted by Dcr_n<16:0>. The '+' symbol denotes the exclusive-OR logical operation.

When Dr_n<3:0> is presented at the input of the descrambler, Dc_n<3:0> is produced by shifting in each bit of Dr_n<3:0> as Dr_n<i>, with i ranging from 0 to 3 (i.e., LSB first). The descrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all the bits of the 17-bit vector representing the self-synchronizing descrambler state are arbitrarily set. The initialization of the descrambler state is left to the implementer. At every RSCD, if no data is presented at the descrambler input via Dr_n<3:0>, the descrambler may be fed with arbitrary inputs.

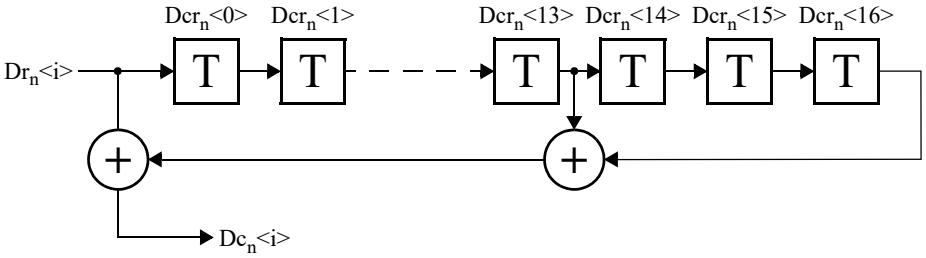

Figure 147–9—Self-synchronizing descrambler

147.3.3.9 Jabber diagnostics

The ESDJAB symbol informs the PCS Receiver that a frame was terminated by the jabber function. The number of received ESDJAB events can be reported to the management entity be the means of MDIO register 3.2293 or similar functionality if MDIO is not implemented.

147.3.4 PCS loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to one (or PCS loopback mode is enabled by a similar functionality if MDIO is not implemented). In this mode, the PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium.

147.3.5 Collision detection

When operating in half-duplex mode, the 10BASE-T1S PHY shall detect when a transmission initiated locally results in a corrupted signal at the MDI as a collision. When collisions are detected, the PHY shall assert the signal COL on the MII for the duration of the collision or until TX_EN signal is FALSE.

The method for detecting a collision is implementation dependent but the following requirements have to be fulfilled:

a) The PHY shall assert COL when it is transmitting, and one or more other stations are also transmitting at the same time.
b) The PHY shall assert CRS in the presence of a signal resulting from a collision between two or more other stations.

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147.3.6 Carrier sense

When operating in half-duplex mode, the 10BASE-T1S PHY senses when the media is busy and conveys this information to the MAC by asserting the signal CRS on the MII as specified in 22.2.2.11.

CRS is generated by mapping the PMA_CARRIER.indication (pma_crs) primitive to the MII signal CRS:

a) CRS shall be asserted when the pma_crs parameter is CARRIER_ON.
b) CRS shall be deasserted when the pma_crs parameter is CARRIER_OFF.

147.3.7 Support for PCS status generation

If Clause 98 Auto-Negotiation functions are implemented and enabled, the PCS shall conform to the Heartbeat (HB) transmit and receive state diagrams in Figure 147–10, Figure 147–11, and the associated state variables, functions, timers, messages, and constants.

If Clause 98 Auto-Negotiation functions are not implemented or disabled, the PCS_STATUS.indication primitive conveys NOT_OK.

The pcs_status parameter of PCS_STATUS.indication primitive is set to OK after the reception of HB signals or valid data reception (RX_DV) according to the logic described in the HB receive state diagram.

The HB generation is disabled when the PHY is configured for operation over a mixing segment or a BEACON is detected.

147.3.7.1 Heartbeat transmit overview

HB signals are sent unsolicited by the PHY that negotiated the master role during auto-negotiation, while the slave PHY replies back to received HB signals.

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

A heartbeat is sent only when the PHY is not in the multidrop mode and Auto-Negotiation has completed. The state diagram in Figure 147–10 is held in the INIT state when in the multidrop mode, Auto-Negotiation is not enabled, or Auto-Negotiation signals link_control = DISABLE.

When the PHY is not in multidrop mode and a BEACON request is received from the MII (see Table 22–2) or a BEACON signal is received from the line (see Table 147–1), the state diagram in Figure 147–10 enters the DISABLE_HB state. It remains in the DISABLE_HB state until at least one of the following occurs: PCS Reset is asserted, multidrop mode is enabled, the disable_hb_timer expires, Auto-Negotiation is disabled, or Auto-Negotiation stops reporting that it is complete.

NOTE—Any BEACON received either from the MII or the PMA restarts the disable_hb_timer.

147.3.7.1.1 Variables

pcs_reset
: See 147.3.2.2.

mr_autoneg_enable
: See 98.5.1.

link_control
: See 147.3.2.2.

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multidrop

If MDIO is implemented, this variable is set according to bit 1.2297.10.
If MDIO is not implemented, multidrop should be set by equivalent means.
Values: TRUE or FALSE

master

Result of the role negotiated using method in 98.2.1.2.5 and Table 98–4.
Values: TRUE (negotiated role is master) or FALSE (negotiated role is slave)

hb_cmd

Enumerated variable that conveys the command to send an HB message to the PCS transmit function. This command is ignored or interrupted by the PCS transmit function when normal data is being sent or a higher priority request is in effect, as specified in 147.3.2.4.
Values: HEARTBEAT or NONE

rx_cmd

PLCA or HEARTBEAT signaling decoded by the PCS.

tx_cmd

See 147.3.2.2.

COL

The MII signal COL.
Values: TRUE or FALSE

CRS

The MII signal CRS.
Values: TRUE or FALSE

RX_DV

The MII signal RX_DV.
Values: TRUE or FALSE

147.3.7.1.2 Timers

disable_hb_timer

Time the heartbeat state diagram dwells in the DISABLE_HB state without receiving or transmitting a BEACON.
Duration: 1 s
Tolerance: ± 100 ms

hb_send_timer

Times the duration of the HB signal on the line.
Duration: 20 bit times
Tolerance: ± 0.5 bit times

hb_timer

Period between the transmission of two consecutive HB signals.
Duration: 50 ms
Tolerance: ± 100 μs

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147.3.7.1.3 State diagram

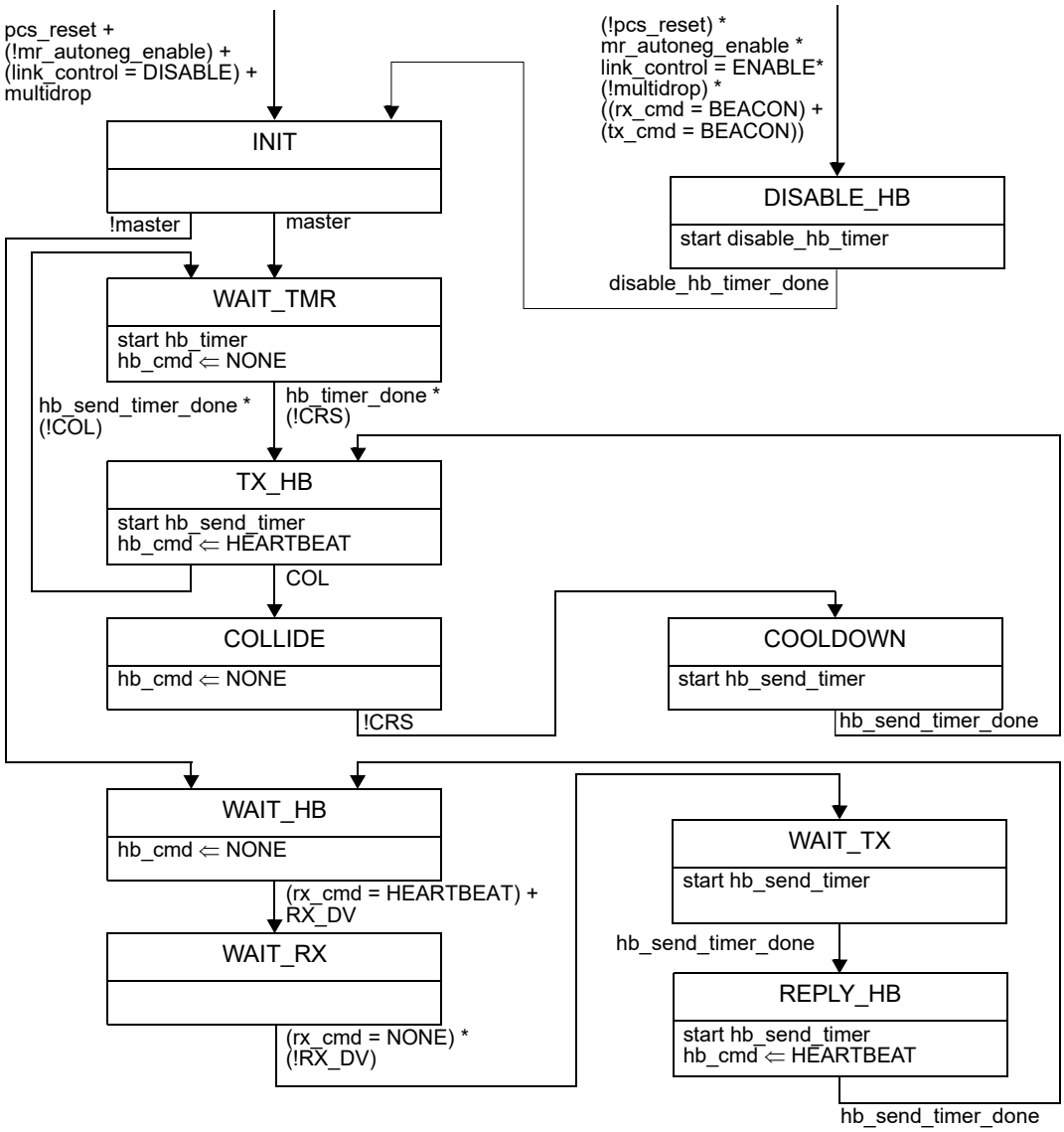

Figure 147–10—Heartbeat transmit state diagram

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147.3.7.2 Heartbeat receive overview

The HB receive state diagram in Figure 147–11 generates the pcs_status parameter of the PCS_STATUS.indication primitive based on the reception of valid data packets and HB signals from the remote PHY.

The pcs_status is reported as OK when at least ACTIVE_CNT valid packets or HB messages, separated at max by link_hold_timer ms, are received.

The pcs_status is reported as NOT_OK when PCS is reset or when no valid packets nor HB messages are received within link_hold_timer for INACTIVE_CNT times in a row.

147.3.7.2.1 Variables

pcs_reset
: See 147.3.2.2.

pcs_status
: Parameter of the PCS_STATUS.indication primitive.
Values: OK or NOT_OK

mr_autoneg_enable
: See 98.5.1.

link_control
: See 147.3.2.2.

multidrop
: See 147.3.7.1.1.

rx_cmd
: See 147.3.7.1.1.

cnt_l
: Count of link_hold_timer expiration periods without HBs or receive packet when pcs_status is OK.
Values: integer number between 0 and INACTIVE_CNT

cnt_h
: Counter of HBs and receive packets when pcs_status is NOT_OK.
Values: integer number between 0 and ACTIVE_CNT

COL
: The MII signal COL.
Values: TRUE or FALSE

CRS
: The MII signal CRS.
Values: TRUE or FALSE

RX_DV
: The MII signal RX_DV.
Values: TRUE or FALSE

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147.3.7.2.2 Constants

ACTIVE_CNT

Number of combined HBs and receive packets required to signal pcs_status = OK.
Value: integer number between 0 and 7
Default value: 2

INACTIVE_CNT

Number of link_hold_timer expirations without HBs or receive packets required to signal pcs_status = NOT_OK.
Value: integer number between 0 and 7
Default value: 5

147.3.7.2.3 Timers

link_hold_timer

Timer used to check inactivity.
Duration: 75 ms
Tolerance: ± 100 μs

147.3.7.2.4 State diagram

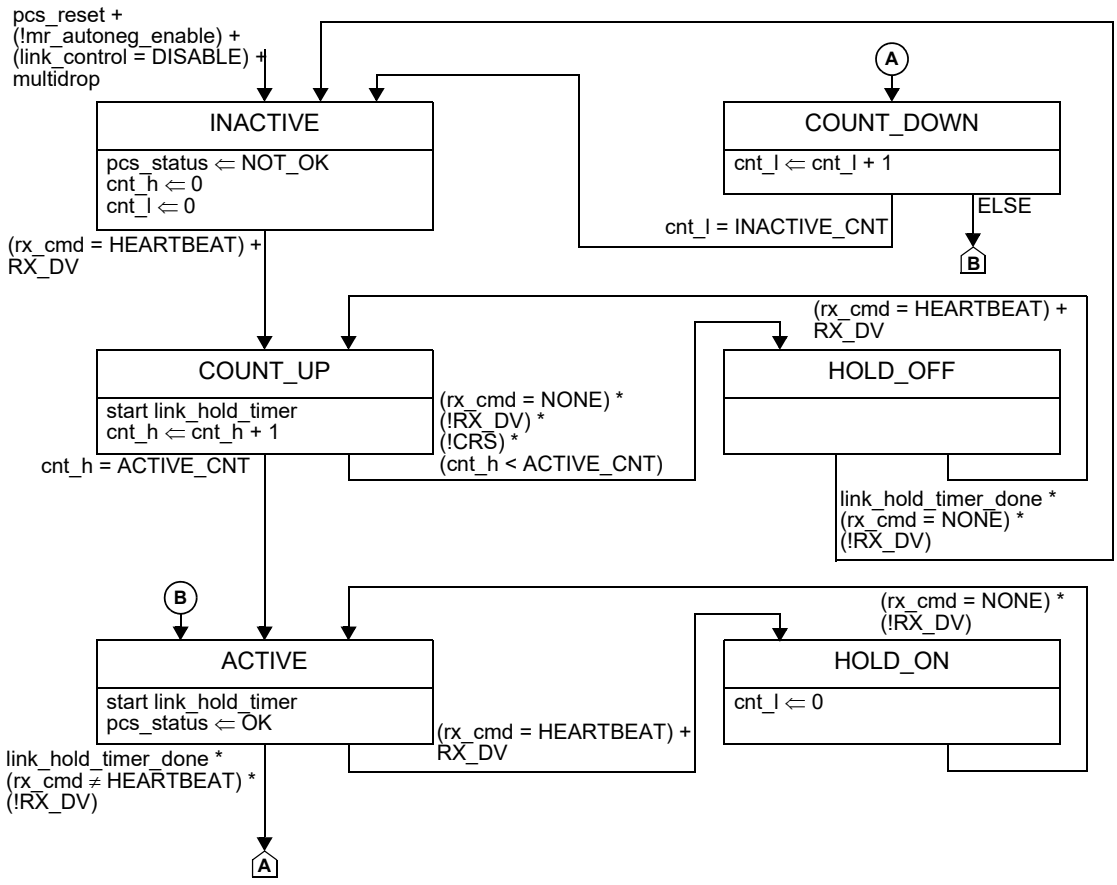

Figure 147–11—Heartbeat receive state diagram

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147.4 Physical Medium Attachment (PMA) sublayer

PMA functions are illustrated in Figure 147–12.

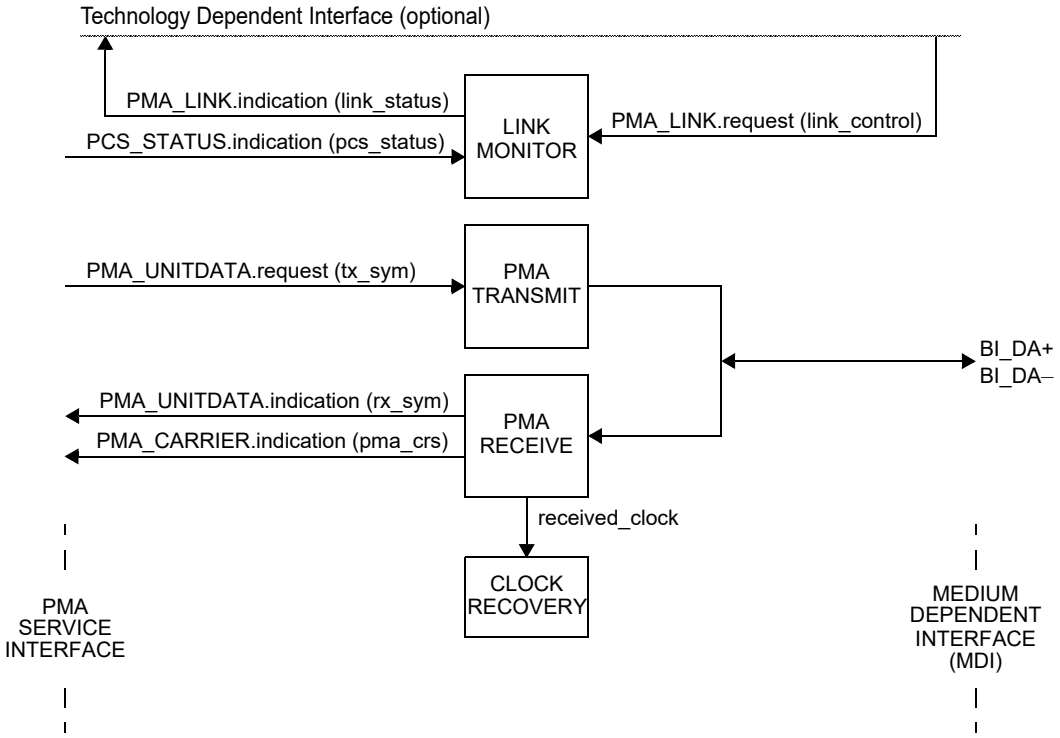

Figure 147–12—PMA functional block diagram

The reference diagrams do not explicitly show the PMA Reset function.

The PMA couples messages from the PMA service interface specified in 147.3.1 onto the 10BASE-T1S physical medium. The PMA provides half duplex communications to and from the medium. Optionally, the PMA may also provide full duplex communications to and from the medium. The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 147.9.

147.4.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

— Power on (see 36.2.5.1.3).
— The receipt of a request for reset from the management entity.

The PMA Reset function carries out the following tasks:

— PMA Transmit output is set to high-impedance state.
— PMA_UNITDATA.indication is cleared.

147.4.2 PMA Transmit function

During transmission, PMA_UNITDATA.request conveys the tx_sym variable to the PMA. The value of the tx_sym variable is sent over the single balanced pair of conductors, BI_DA.

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The tx_sym variable is a 5B symbol, to be encoded LSB first, using DME rules defined below:

If the tx_sym parameter value is the special 5B symbol 'I', the PMA shall, in the following order:

a) Transmit an additional DME encoded 0 if the previous value of the tx_sym parameter was anything but the 5B symbol 'I'.
b) When operating in multidrop mode, present the minimum impedance described in 147.9.2 at the MDI. This shall happen within 40 ns after the additional DME encoded 0 has been transmitted.
c) When operating in point-to-point mode, drive BI_DA+ and BI_DA– to the same voltage with 100 Ω nominal impedance, so that their difference is 0 V.

If tx_sym value is anything other than 'I', the following rules apply:

— A “clock transition” shall always be generated at the start of each bit.
— A “data transition” in the middle of a nominal bit period shall be generated if the bit to be transmitted is a logical '1'. Otherwise, no transition shall be generated until the next bit.

See Figure 147–13 and Table 147–2.

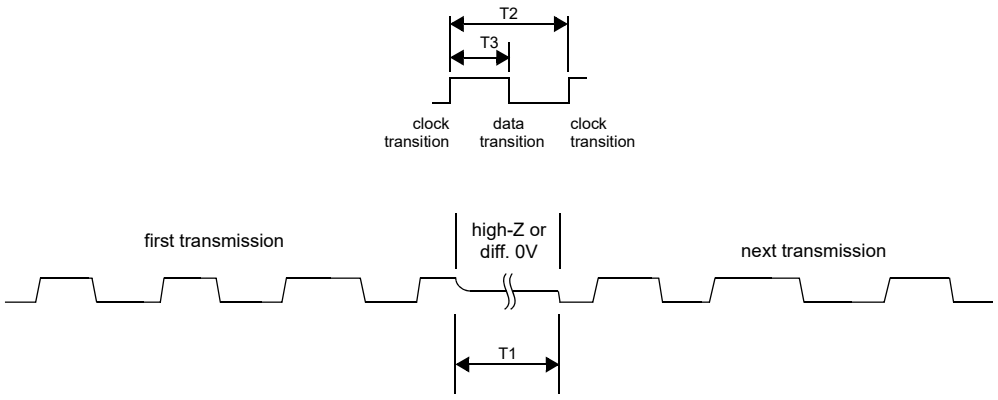

Figure 147–13—DME encoding scheme

Table 147–2—DME timings

Parameter name	Description	Minimum value	Nominal value	Maximum value	Unit of measure
T1	Delay between transmissions	480	—	—	ns
T2	Clock transition to clock transition	–100 ppm	80	+100 ppm	ns
T3	Clock transition to data transition (data = 1)	38	40	42	ns

147.4.3 PMA Receive function

The 10BASE-T1S PMA Receive function comprises a single receiver (PMA Receive) for DME modulated signals on a single balanced pair of conductors, BI_DA. PMA Receive has the ability to translate the received signals on the single balanced pair of conductors into the PMA_UNITDATA.indication parameter rx_sym. It detects 5B symbols from the signals received at the MDI and presents these sequences to the PCS Receive function.

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The PMA Receive function recovers encoded clock and data information from the DME encoded stream received at the MDI. The clock recovery provides a synchronous clock for sampling the signal on the pair. While it may not drive the MII directly, the clock recovery function is the underlying source of RX_CLK. In order to meet the specifications of 147.5.5.1, the PMA Receive function has to achieve proper synchronization on both the DME stream and the 5B boundary within 800 ns.

The PMA Receive function interprets the signals at the MDI using the inverse mapping described in 147.4.2 for the PMA Transmit function and transfers the 5B code groups by the means of the PMA_UNITDATA.indication. When the PMA Receive function does not detect activity on the line, it shall convey the symbol 'I' (meaning SILENCE).

147.4.4 Link Monitor function

The PMA shall conform to the Link Monitor state diagram in Figure 147–14 and associated variables.

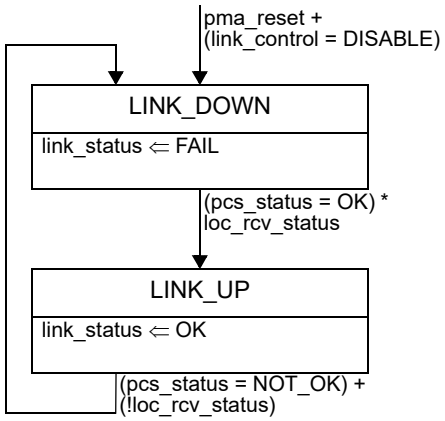

Figure 147–14—Link Monitor state diagram

147.4.4.1 Link Monitor overview

The link monitor function generates the link_status parameter of the PMA_LINK.indication primitive for the Clause 98 Auto-Negotiation function.

The link_status parameter is set after the result of the PCS_STATUS.indication primitive and the implementation defined variable loc_rcv_status.

147.4.4.2 Variables

pma_reset
: Allows reset of all PMA functions.
Values: TRUE or FALSE
Set by: PMA Reset function.

link_control
: See 147.3.2.2.

loc_rcv_status
: Implementation defined variable set to TRUE when the PMA is ready to decode valid data from the line, FALSE otherwise.
Values: TRUE or FALSE

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link_status

The link_status parameter set by PMA Link Monitor and communicated to the Technology Dependent Interface through the PMA_LINK.indication primitive.
Values: OK or FAIL

pcs_status

See 147.3.7.2.1.

147.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA for a 10BASE-T1S PHY.

147.5.1 EMC tests

Direct Power Injection (DPI) and 150 Ω emission tests for noise immunity and emission as per 147.5.1.1 and 147.5.1.2 may be used to establish a baseline for PHY EMC performance. These tests provide a high degree of repeatability and a good correlation to immunity and emission measurements. Operational requirements of the transceiver during the test are determined by the manufacturer.

Applications for the specified device commonly have additional requirements that limit its conducted radio frequency emission and its susceptibility to electromagnetic interference. Such requirements are beyond the scope of this standard.

147.5.1.1 Immunity—DPI test

In a real application radio frequency (RF) common-mode (CM) noise at the PHY is the result of electromagnetic interference coupling to the cabling system. Additional differential-mode (DM) noise at the PHY is generated from the CM noise by mode conversion of all parts of the cabling system and the MDI. The sensitivity of the PMA's receiver to RF CM noise may be tested according to the DPI method of IEC 62132-4.

147.5.1.2 Emission—Conducted emission test

The emission of the PMA transmitter to its electrical environment may be tested according to the 150 Ω direct coupling method of IEC 61967-4, and may need to comply with more stringent requirements.

147.5.2 Test modes

The test modes described in this subclause shall be provided to allow testing of the transmitter. The test modes can be enabled by setting bits 1.2299.15:13 (10BASE-T1S test mode control register) of the PHY Management register set as described in 45.2.1.236.1. If MDIO is not implemented a similar functionality shall be provided by equivalent means. These test modes shall change only the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

a) Test mode 1—Transmitter output voltage, timing jitter
b) Test mode 2—Transmitter output droop test mode
c) Test mode 3—Transmitter PSD mask
d) Test mode 4—Transmitter high impedance mode

When test mode 1 is enabled, the PHY shall repeatedly transmit DME encoded ones.

When test mode 2 is enabled, the PHY shall transmit a positive differential voltage for 1.6 μs followed by a negative differential voltage level for 1.6 μs. This sequence is repeated continually.

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When test mode 3 is enabled, the PHY shall transmit continually a pseudo-random sequence of positive and negative voltage levels, generated by the scrambler defined in 147.3.2.8 and encoded using DME as in 147.4.2.

PHYs supporting multidrop mode shall implement test mode 4. When test mode 4 is enabled and the PHY is configured for multidrop mode, the transmitter shall present a high impedance termination to the line as specified in 147.4.2 for the 'I' symbol when operating in multidrop mode.

PHYs not supporting multidrop mode are not required to implement test mode 4. When test mode 4 is enabled and the PHY is not configured for multidrop mode, the transmitter behavior is undefined and left up to the implementer.

147.5.3 Test fixtures

The following fixtures (illustrated by Figure 147–15 and Figure 147–16), or their functional equivalents, can be used for measuring the transmitter specifications described in 147.5.4.

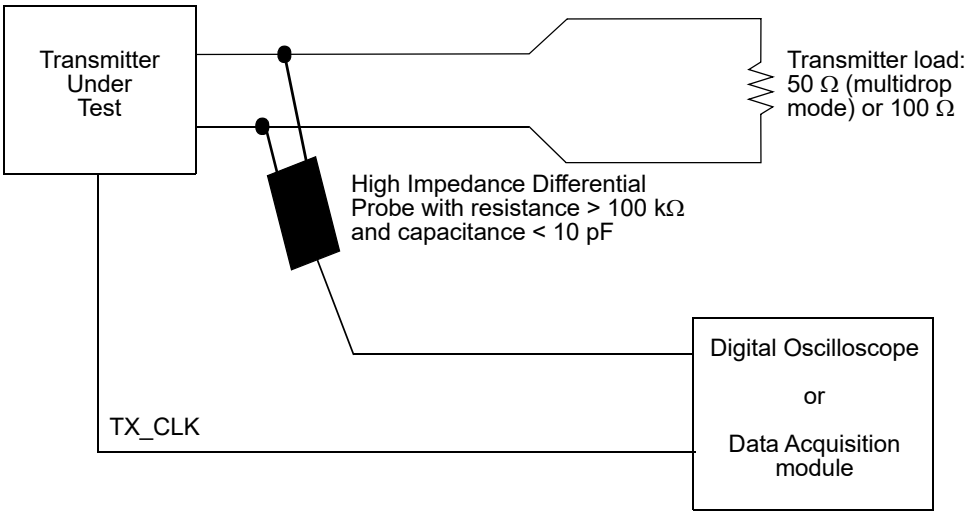

Figure 147–15—Transmitter test fixture 1 for transmitter voltage, transmitter droop, and transmitter timing jitter

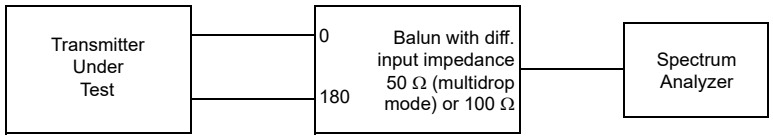

Figure 147–16—Transmitter test fixture 2 for power spectral density (PSD) measurement

To allow an easy synchronization of the measurement equipment, the PHY shall provide access to TX_CLK.

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147.5.4 Transmitter electrical specification

The PMA shall operate with AC coupling to the MDI.

Where a load is not specified and multidrop mode is supported and enabled, the transmitter shall meet the requirements of this subclause with a 50 Ω resistive differential load connected to the transmitter output. Otherwise, the transmitter shall meet the requirements of this subclause with a 100 Ω resistive differential load connected to the transmitter output. Transmitter electrical tests are specified with a load tolerance of ± 0.1%.

Unless otherwise specified, the specifications in 147.5.4.1 through 147.5.4.5 apply to transmitters in both point-to-point and multidrop mode, if supported.

147.5.4.1 Transmitter output voltage

When tested using the test fixture shown in Figure 147–15 with the transmitter in test mode 1, the transmitter output voltage shall be 1 V ± 20% peak-to-peak differential.

147.5.4.2 Transmitter output droop

When tested using the text fixture shown in Figure 147–15 with the transmitter in test mode 2, the magnitude of both the positive and negative droop measured with respect to the initial peak value after the zero crossing and the value 800 ns after the initial peak, depicted by Figure 147–17, shall be less than 30%.

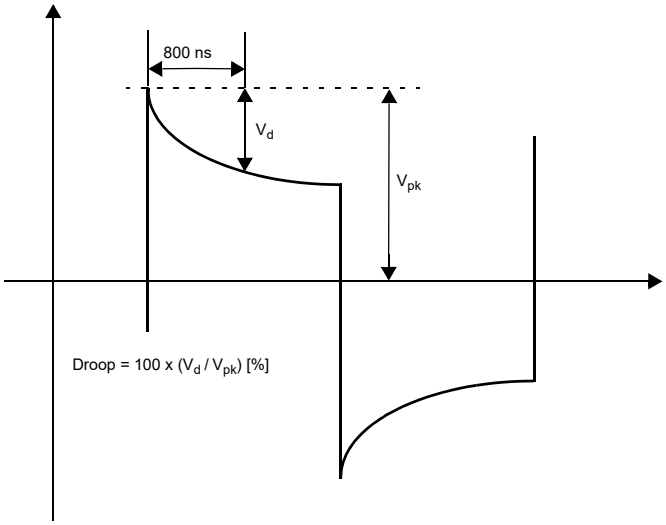

Figure 147–17—Transmitter output droop

147.5.4.3 Transmitter timing jitter

When measured using the test fixture shown in Figure 147–15 with the transmitter in test mode 1, the maximum jitter at the transmitter side shall be less than 5 ns symbol-to-symbol.

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147.5.4.4 Transmitter Power Spectral Density (PSD)

When measured using test mode 3 and the test fixture shown in Figure 147–16, or equivalent, the transmitter Power Spectral Density (PSD) shall be between the upper and lower masks specified in Equation (147–1) and Equation (147–2).

The upper and lower limits for multidrop mode are given in Equation (147–1) and Equation (147–2), and shown in Figure 147–18. In point-to-point mode both upper and lower limits are 3 dB lower than those for multidrop mode.

147.5.4.4.1 Upper PSD

$$\text{UpperPSD}(f) = \left\{ \begin{array}{ll} -61 & 0.3 \le f < 15 \\ -40 - 1.4f & 15 \le f < 25 \\ -75 & 25 \le f \le 40 \end{array} \right\} \text{ dBm/Hz} \quad (147\text{–}1)$$

where

f is the frequency in MHz; $0.3 \le f \le 40$

Lower PSD

$$\text{LowerPSD}(f) = \left\{ \begin{array}{ll} -87 + 2f & 5 \le f < 10 \\ -47 - 2f & 10 \le f \le 15 \end{array} \right\} \text{ dBm/Hz} \quad (147\text{–}2)$$

where

f is the frequency in MHz; $5 \le f \le 15$

147.5.4.4.2 PSD mask

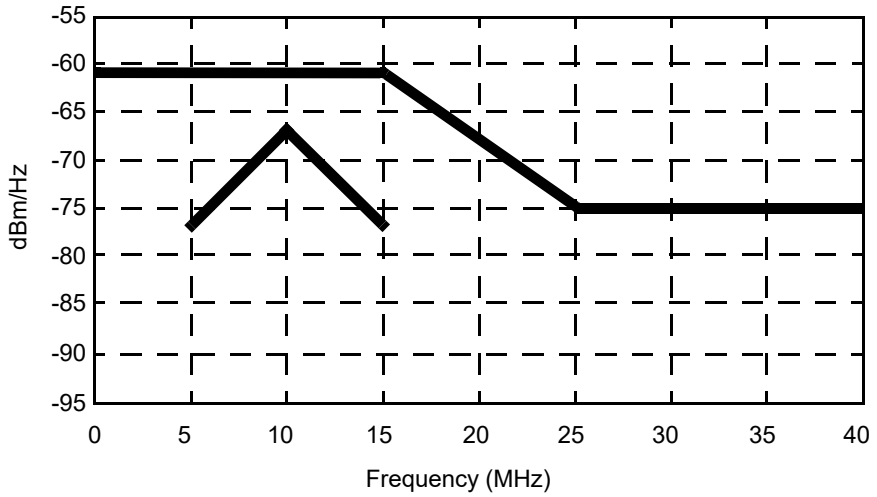

Figure 147–18—PSD upper and lower limits

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147.5.4.5 Transmitter high impedance mode

In test mode 4, a transmitter with multidrop mode supported and enabled shall present the minimum parallel impedance across the MDI attachment points as specified in 147.9.2.

147.5.5 Receiver electrical specifications

147.5.5.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 147.5.4 and have passed through a link segment specified in 147.7 or a mixing segment specified in 147.8 shall be received with a Bit Error Ratio (BER) of less than 10^{-10}, and sent to the MII during normal data transmission. This specification can be verified by a frame error ratio less than 10^{-7} for 125 octet frames.

147.5.5.2 Alien crosstalk noise rejection

The test is performed with a noise source such that noise with a Gaussian distribution, bandwidth of 40 MHz, and magnitude of –101 dBm/Hz is present at the MDI.

The receive DUT is connected to these noise sources through a resistive network, as shown in Figure 147–19, with link segments as defined in 147.7 and 147.8. The BER shall be less than 10^{-10}. This specification may be considered satisfied when the frame loss ratio is less than 10^{-7} for 125 octet frames measured at MAC/PLS service interface.

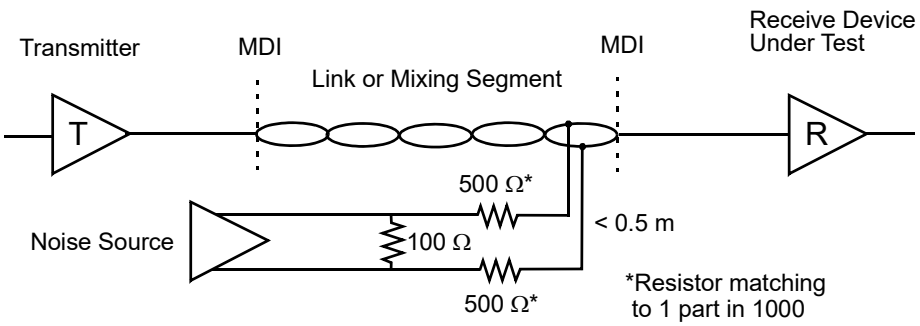

Figure 147–19—Alien crosstalk noise rejection test set-up

147.5.6 PMA local loopback

The PMA local loopback function is optional. If supported, the PMA shall be placed in local loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, or the PMA loopback bit in MDIO register 1.2297.13, defined in 45.2.1.234.5, is set to one (or PMA loopback mode is enabled by a similar functionality if MDIO is not implemented).

When the PHY is in the PMA local loopback mode, if the PHY supports full-duplex mode of operation, the PMA Receive function utilizes the echo signals from the open MDI and decodes these signals to pass the data back to the MII Receive interface.

If the PHY supports half-duplex mode of operation, the PMA and PCS Receive functions shall pass to the MII RX the data decoded from the signal which is normally received during a transmission for the purpose of detecting collisions.

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A MAC client can compare the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the 10BASE-T1S PCS and PMA functions.

147.6 Management interface

10BASE-T1S uses the management interface as specified in Clause 45. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

147.6.1 Support for Auto-Negotiation

Auto-Negotiation may be performed as part of the initial set-up of the link and allows negotiation of the duplex mode of operation. When Auto-Negotiation is used, Technology Ability Field bit A22 contains a one if the PHY is supporting and advertising 10BASE-T1S half duplex ability, and it contains a zero if 10BASE-T1S half duplex communication is not supported or not advertised. When Auto-Negotiation is used, Technology Ability Field bit A1 contains a one if the PHY is supporting and advertising 10BASE-T1S full duplex ability, and it contains a zero if 10BASE-T1S full duplex communication is not supported or not advertised. See 98B.4 for priority resolution.

147.7 Point-to-point link segment characteristics

The transmission characteristics for the 10BASE-T1S point-to-point link segment are specified to support applications requiring short physical reach, such as industrial, automotive, and building automation controls, for up to at least 15 m.

147.7.1 Insertion loss

The insertion loss of each 10BASE-T1S point-to-point link segment shall meet the values determined using Equation (147–3).

$$\text{Insertion loss}(f) < \left\{ \begin{array}{ll} 1.0 + \frac{1.6\,(f-1)}{9} & 0.3 \le f < 10 \\ 2.6 + \frac{2.3\,(f-10)}{23} & 10 \le f < 33 \\ 4.9 + \frac{2.3\,(f-33)}{33} & 33 \le f \le 40 \end{array} \right\} \text{ dB} \qquad (147\text{–}3)$$

where

f is the frequency in MHz; $0.3 \le f \le 40$

147.7.2 Return loss

In order to limit the noise at the receiver due to impedance mismatches, each 10BASE-T1S point-to-point link segment shall meet the values determined using Equation (147–4) at all frequencies from 0.3 MHz to 40 MHz. The reference impedance for the return loss specification is 100 Ω.

$$\text{Return loss}(f) > \left\{ \begin{array}{ll} 14 & 0.3 \le f < 10 \\ 14 - 10\log_{10}\left(\frac{f}{10}\right) & 10 \le f \le 40 \end{array} \right\} \text{ dB} \qquad (147\text{–}4)$$

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where

f is the frequency in MHz; $0.3 \le f \le 40$

147.7.3 Mode conversion loss

The mode conversion loss of each 10BASE-T1S point-to-point link segment shall meet the values determined using Equation (147–5).

$$\text{Mode conversion loss}(f) > \left\{ \begin{array}{ll} 43 & 0.3 \le f < 20 \\ 43 - 20\log_{10}\left(\frac{f}{20}\right) & 20 \le f \le 200 \end{array} \right\} \text{ dB} \quad (147\text{–}5)$$

where

f is the frequency in MHz; $0.3 \le f \le 200$

147.7.4 Power sum alien near-end crosstalk (PSANEXT)

There is no FEXT or NEXT as 10BASE-T1S is a single pair solution. Noise coupled between the disturbed 10BASE-T1S link segment and other disturbing 10BASE-T1S link segments is referred to as alien crosstalk noise. Since the transmitted symbols from the alien noise source in one cable are not available to another cable, cancellation cannot be done. When there are multiple pairs of cables bundled together, where all pairs carry 10 Mb/s links, then each duplex link is disturbed by neighboring links, degrading the signal quality on the victim pair. In order to limit the near-end crosstalk noise for a 5-around-1 cable bundle (up to 15 m length and up to four in-line connectors, equally spaced), the power sum alien near-end crosstalk (PSANEXT) loss shall meet Equation (147–6).

$$\text{PSANEXT}(f) \ge 31.5 - 10\log_{10}\left(\frac{f}{100}\right) \text{ dB} \quad (147\text{–}6)$$

where

f is the frequency in MHz; $1 \le f \le 40$

147.7.5 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

The power sum alien attenuation to crosstalk ratio far-end (PSAACRF) loss for a 5-around-1 cable bundle (up to 15 m length and up to four in-line connectors, equally spaced) shall meet Equation (147–7).

$$\text{PSAACRF}(f) \ge 16.5 - 20\log_{10}\left(\frac{f}{100}\right) \text{ dB} \quad (147\text{–}7)$$

where

f is the frequency in MHz; $1 \le f \le 40$

147.8 Mixing segment characteristics

10BASE-T1S PHYs supporting multidrop mode are designed to operate over media that meet the requirements specified in this subclause. The 10BASE-T1S mixing segment (1.4.403) is a single balanced pair of conductors that may have more than two MDIs attached.

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A mixing segment is specified based on cabling that supports up to at least 8 nodes and 25 m in reach. Larger PHY count and/or reach may be achieved provided the mixing segment specifications in 147.8 are met. An example mixing segment and reference points are shown in Figure 147–20.

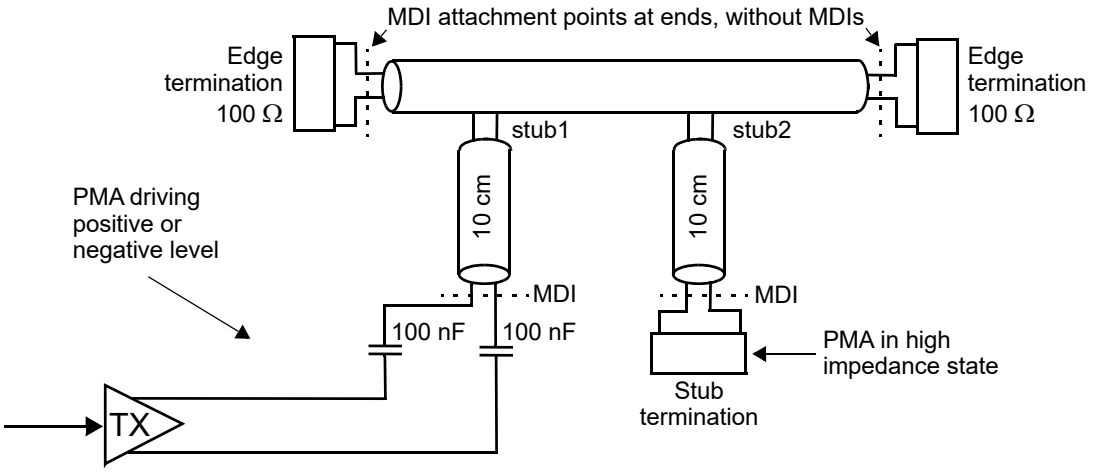

Figure 147–20—Multidrop line termination and PMA

147.8.1 Insertion loss

The mixing segment shall meet the insertion loss characteristics specified for link segments in 147.7.1 between any two MDI attachment points.

147.8.2 Return loss

The mixing segment shall meet the return loss characteristics specified for link segments in 147.7.2 at any MDI attachment point. The reference impedance for the return loss specification is 50 Ω.

147.8.3 Mode conversion loss

The mixing segment shall meet the mode conversion loss characteristics specified for link segments in 147.7.3 between any two MDI attachment points.

147.9 MDI specification

This subclause describes connectors which may be used at the MDI. It also specifies electrical requirements, including fault tolerance, at the MDI.

147.9.1 MDI connectors

In its minimum configuration, the mechanical interface to the balanced cabling is a 3-pin connector (BI_DA+, BI_DA–, and optional SHIELD) or alternatively a 2-pin connector with an optional additional mechanical shield connection which conforms to the link segment specification defined in 147.7 or to the mixing segment specification defined in 147.8.

Specific systems or applications can use connectors or terminals that support the link segment specification defined in 147.7 or the mixing segment specification defined in 147.8.

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Connectors meeting the mechanical requirements of IEC 63171-1 [B36] or IEC 63171-6:2020 [B37] may be used as the mechanical interface to the balanced cabling. The plug connector is used on the balanced cabling and the MDI jack connector on the PHY. The IEC 63171-1 plug and jack are depicted (for informational use only) in Figure 147–21 and Figure 147–22 respectively, and the mating interface is depicted in Figure 147–23. The IEC 63171-6 plug and jack are depicted (for informational use only) in Figure 147–24 and Figure 147–25 respectively, and the mating interface is depicted in Figure 147–26. These connectors should support link segment DCR characteristics for 1.02 mm (18 AWG) to 0.40 mm (26 AWG) in Table 146B–1.

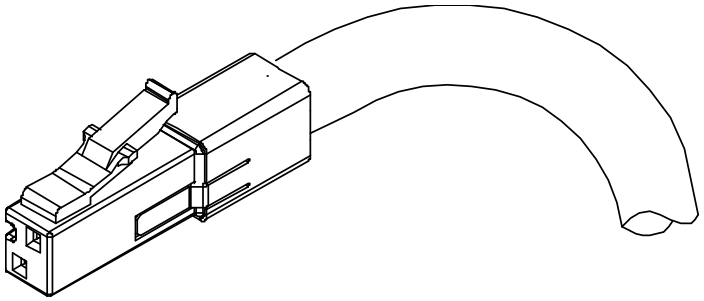

Figure 147–21—IEC 63171-1 plug

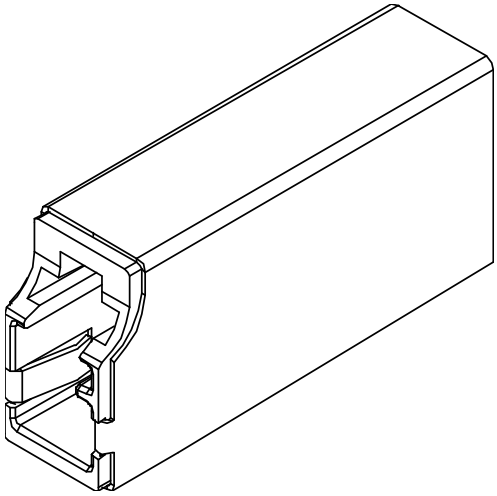

Figure 147–22—IEC 63171-1 jack

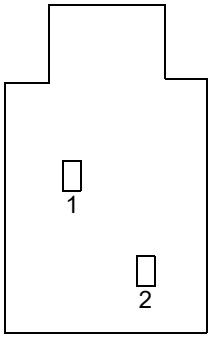

Figure 147–23—IEC 63171-1 mating face

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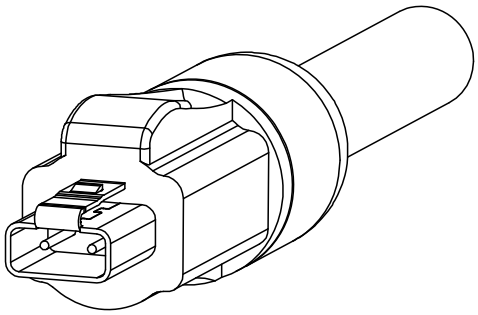

Figure 147–24—IEC 63171-6 plug

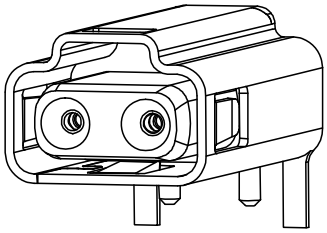

Figure 147–25—IEC 63171-6 jack

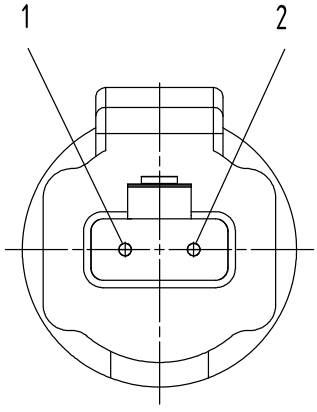

Figure 147–26—IEC 63171-6 mating face

The assignment of PMA signals to connector contacts for PHYs are given in Table 147–3.

Table 147–3—Assignment of PMA signals to MDI contacts

Contact	PMA signal
1	BI_DA+
2	BI_DA–

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147.9.2 MDI electrical specification

When not in multidrop mode, the MDI shall meet the return loss limits as specified in Equation (96–12) in 96.8.2.1.

When in multidrop mode, the MDI shall present a minimum parallel impedance across the MDI attachment points per Equation (147–8) and the limits for R, L, C_{tot}, and C_{node} given in Table 147–4 over the stated frequency range. C_{tot} is the maximum total capacitance across all MDI attachment points, while R, L, and C_{node} are the resistance, inductance, and capacitance for each MDI attachment point.

Inductive elements are often used when power is applied across the data lines, and may be absent in non-powered implementations. Removing the parallel inductance is equivalent to setting L to infinity in Equation (147–8). The parasitic capacitance of inductive elements forms a portion of C_{node}.

$$|Z| = \frac{1}{\sqrt{\frac{1}{R^2} + \left(\frac{1}{2\pi \cdot f \cdot L} - 2\pi \cdot f \cdot C_{node}\right)^2}} \quad (147–8)$$

where

f is the frequency in MHz; $0.3 \leq f \leq 40$

Table 147–4—MDI impedance limit parameters

Parameter name	Unit of measure	Minimum value	Maximum value
R	kΩ	10	—
L	μH	80	—
C_{tot}	pF	—	180
C_{node}	pF	—	15

NOTE—The implementer is cautioned that loading the mixing segment with multiple nodes with worst case capacitance at the same location on the mixing segment may cause the mixing segment to exceed its return loss specification.

147.9.3 MDI line powering voltage tolerance

The DTE shall withstand without damage the application of any voltages between 0 V dc and 60 V dc with the source current limited to 2000 mA, applied across BI_DA+ and BI_DA–, in either polarity, under all operating conditions, for an indefinite period of time.

147.9.4 MDI fault tolerance

The wire pair of the MDI shall withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential, as per Table 147–5, under all operating conditions indefinitely. Normal operation shall resume after all short circuits have been removed.

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Table 147–5—Fault conditions

BI_DA+	BI_DA–
BI_DA–	BI_DA+
Ground	No fault
No fault	Ground
Ground	Ground
+60 V dc	No fault
No fault	+60 V dc
+60 V dc	+60 V dc
Ground	+60 V dc
+60 V dc	Ground

147.10 Environmental specifications

147.10.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2 or IEC 61010-1, as appropriate. All equipment subject to this clause is expected to conform to all applicable local, state, national, and application-specific standards.

147.10.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner. All 10BASE-T1S cabling is expected to be routed according to any applicable local, state, or national standards considering all relevant safety requirements. In automotive applications, all 10BASE-T1S cabling is expected to be routed to provide maximum protection by the motor vehicle sheet metal and structural components, following SAE J1292, ISO 14229, and ISO 15764. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

147.10.2.1 Environmental safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; this list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

Systems described in this subclause are subject to various environmental hazards during their installation and use. In particular, equipment used in automotive and industrial environments can expect to meet the potential environmental stresses with respect to their mounting location defined for the application. Stresses expected in these environments may include but are not limited to those found in the listed specifications.

The following specifications describe potential environmental stresses in an automotive environment:

— General loads: ISO 16750-1
— Electrical loads: ISO 16750-2, ISO 7637-2, and ISO 8820-1
— Mechanical loads: ISO 16750-3, ASTM D4728, and ISO 12103-1

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— Climatic loads: ISO 16750-4, and IEC 60068-2-1, IEC 60068-2-27, IEC 60068-2-30, IEC 60068-2-38, IEC 60068-2-52, IEC 60068-2-64, and IEC 60068-2-78
— Chemical loads: ISO 16750-5 and ISO 20653

The following specifications define potential environmental stresses in an industrial environment:

— Environmental loads: IEC 60529 and ISO 4892
— Mechanical loads: IEC 60068-2-6 and IEC 60068-2-31
— Climatic loads: IEC 60068-2-1, IEC 60068-2-2, IEC 60068-2-14, IEC 60068-2-27, IEC 60068-2-30, IEC 60068-2-38, IEC 60068-2-52, and IEC 60068-2-78

Additional environment(s) require careful analysis prior to implementation to determine appropriate environmental safety requirements.

147.10.2.2 Electromagnetic compatibility

A system integrating the 10BASE-T1S PHY is expected to comply with all applicable local and national codes for electromagnetic compatibility. In addition, the system may need to comply with more stringent requirements for the limitation of electromagnetic interference.

147.11 Delay constraints

The PHY shall comply with the timing requirements specified in Table 147–6.

Table 147–6—10BASE-T1S delay constraints

Event	Minimum value	Maximum value	Unit of measure	Input timing reference	Output timing reference
TX_EN/TX_ER sampled to MDI output	120	440	ns	Rising edge of MII TX_CLK	First DME clock transition at the MDI
MDI input to CRS asserted	400	1040	ns	First DME clock transition at the MDI	Rising edge of CRS
MDI input to CRS deasserted	640	1120	ns	Last DME encoded zero clock transition at the MDI	Falling edge of CRS
MDI input to COL asserted	0	5	µs	Start of corrupted transmitted signal at the MDI	Rising edge of COL
MDI input to COL deasserted	0	3.2	µs	End of transmission at the MDI	Falling edge of COL
MDI input to RX_DV asserted	2.4	4	µs	First DME clock transition at the MDI	Rising edge of RX_DV
MDI input to RX_ER asserted	1.6	4	µs	First DME clock transition at the MDI	Rising edge of RX_ER

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147.12 Protocol implementation conformance statement (PICS) proforma for Clause 147, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S[243]

147.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 147, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

147.12.2 Identification

147.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

147.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 147, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[243] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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147.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*MDIO	MDIO Capability	45.1	Register and Interface supported	O	Yes [ ] No [ ]
*HALF	Half-duplex mode			M	Yes [ ] No [ ]
*INS-P2P	Installation / Point-to-point cabling	147.7	Items marked with *INS-P2P include installation practices and cabling specifications for link segments and are not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]
*INS-MIX	Installation / Mixing segment	147.8	Items marked with *INS-MIX include installation practices and cabling specifications for mixing segments and are not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]
*MULT	Multidrop mode			O	Yes [ ] No [ ]
MII	PHY associated with MII	147.1.1		O	Yes [ ] No [ ]
PCS	10BASE-T1S PCS	147.3		M	Yes [ ] No [ ]
PMA	10BASE-T1S PMA	147.4		M	Yes [ ] No [ ]
AN	Auto-Negotiation	98		O	Yes [ ] No [ ]
FULL	Full-duplex mode			O	Yes [ ] No [ ]

147.12.4 PICS proforma tables for Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S

147.12.4.1 PCS Transmit

Item	Feature	Subclause	Value/Comment	Status	Support
PCST1	PCS Reset	147.3.1	See 147.3.1	M	Yes [ ]
PCST2	PCS Data Transmission Enable function	147.3.2.1	Conform to the PCS Transmit state diagram	M	Yes [ ]
PCST3	Values of tx_cmd variable	147.3.2.2	See 147.3.2.2	M	Yes [ ]
PCST4	PCS Transmit function scrambler polynomial	147.3.2.8	$g(x) = x^{17} + x^{14} + 1$	M	Yes [ ]
PCST5	PCS scrambler seed values	147.3.2.8	Never initialized to zeros	M	Yes [ ]
PCST6	xmit_max_timer	147.3.2.6	Upon expiration, an even number of nibbles have been sent	M	Yes [ ]

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147.12.4.2 PCS Receive

Item	Feature	Subclause	Value/Comment	Status	Support
PCSR1	PCS Receive function	147.3.3.1	Conform to the PCS Receive state diagram and associated variables	M	Yes [ ]
PCSR2	Generation of RXD<3:0> to the MII	147.3.3.8	Descramble the 5B/4B decoded data stream and return the proper sequence of nibbles	M	Yes [ ]
PCSR3	self-synchronizing descrambler	147.3.3.8	See 147.3.2.8	M	Yes [ ]
PCSR4	False Carrier supported	147.3.3.7	See Figure 147–7	O	Yes [ ]

147.12.4.3 PCS loopback

Item	Feature	Subclause	Value/Comment	Status	Support
PCSL1	PCS loopback	147.3.4	The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to one	MDIO: M	Yes [ ] N/A[ ]
PCSL2	PCS loopback function	147.3.4	The PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII	M	Yes [ ]
PCSL3	PHY receive circuitry isolation	147.3.4	The PHY receive circuitry shall be isolated from the network medium	M	Yes [ ]
PCSL4	PHY transmit circuity isolation	147.3.4	The assertion of TX_EN at the MII shall not result in the transmission of data on the network medium	M	Yes [ ]

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147.12.4.4 Collision detection

Item	Feature	Subclause	Value/Comment	Status	Support
CD1	Detect collisions on the media during data transmission	147.3.5	When a transmission initiated locally results in a corrupted signal at the MDI, a collision is detected	HALF: M	Yes [ ] N/A[ ]
CD2	When collisions are detected	147.3.5	Assert the signal COL on the MII for the duration of the collision or until TX_EN signal is FALSE	HALF: M	Yes [ ] N/A[ ]
CD3	CRS asserted during collision of two or more other stations	147.3.5	See 147.3.5	HALF: M	Yes [ ] N/A[ ]
CD4	Sense when the media is busy	147.3.6	Assert the signal CRS on the MII as specified in 22.2.2.11	HALF: M	Yes [ ] N/A[ ]

147.12.4.5 Support for PCS status generation

Item	Feature	Subclause	Value/Comment	Status	Support
HB1	Heartbeat behavior when Auto-Negotiation is implemented and enabled	147.3.7	Conforms to Figure 147–10 and Figure 147–11	AN:M	Yes [ ] N/A[ ]

147.12.4.6 Physical Medium Attachment (PMA)

147.12.4.6.1 PMA function

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	PMA reset function	147.4.1	See 147.4.1	M	Yes [ ]
PMA2	tx_sym parameter value is the special 5B symbol 'I'	147.4.2	See 147.4.2	M	Yes [ ]
PMA3	receive SILENCE	147.4.3	PMA receive conveys symbol ‘I’ when no activity is detected on the line.	M	Yes [ ]
PMA4	Link Monitor Function	147.4.4	Conforms to Figure 147–14	M	Yes [ ]

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147.12.4.6.2 PMA electrical specification

Item	Feature	Subclause	Value/Comment	Status	Support
PMAE1	Test modes	147.5.2	Implemented in PHY to allow testing transmitter electrical requirements	M	Yes [ ]
PMAE2	Enable test modes	147.5.2	Enable by setting bits 1.2299.15:13 as described in 45.2.1.236 when MDIO implemented; similar functionality provided otherwise	MDIO:M	Yes [ ] N/A[ ]
PMAE3	These test modes shall change only the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation	147.5.2		M	Yes [ ]
PMAE4	Test mode 1	147.5.2	When enabled, PHY repeatedly transmits DME encoded ones	M	Yes [ ]
PMAE5	Test mode 2	147.5.2	When enabled, PHY repeatedly transmits a positive differential voltage for 1.6 μs followed by a negative differential voltage level for 1.6 μs	M	Yes [ ]
PMAE6	Test mode 3	147.5.2	When test mode 3 is enabled, the PHY shall transmit continually a pseudo-random sequence of positive and negative voltage levels, generated by the scrambler defined in 147.3.2.8 and encoded using Differential Manchester Encoding (DME) as in 147.4.2.	M	Yes [ ]
PMAE7	Test mode 4	147.5.2	When enabled, PHY transmitter shall present a high impedance termination to the line as specified in 147.4.2	MULT:M	Yes [ ] N/A[ ]
PMAE8	TX_CLK	147.5.3	PHY to provide access to TX_CLK	M	Yes [ ]
PMAE9	AC coupling at MDI	147.5.4		M	Yes [ ]
PMAE10	The transmitter shall meet the requirements of this subclause with a 100 Ω ± 0.1% resistive differential load connected to the transmitter output	147.5.4		M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PMAE11	The transmitter shall meet the requirements of this subclause with a 50 Ω ± 0.1% resistive differential load connected to the transmitter output when multidrop mode is supported and enabled	147.5.4		MULT:M	Yes [ ] N/A[ ]
PMAE12	Transmitter output voltage	147.5.4.1	1.0 V ± 20% peak-to-peak differential when measured on test mode 1	M	Yes [ ]
PMAE13	Transmitter output droop	147.5.4.2	Less than 30% when measured on test mode 2	M	Yes [ ]
PMAE14	Transmitter timing jitter	147.5.4.3	Less than 5 ns symbol-to-symbol jitter when measured on test mode 1	M	Yes [ ]
PMAE15	Transmit power spectral density	147.5.4.4	Between the upper and lower masks specified in Equation (147–1) and Equation (147–2) when measured on test mode 3	M	Yes [ ]
PMAE16	A transmitter with multidrop mode supported and enabled, and configured for test mode 4	147.5.4.5	Presents the minimum parallel impedance across the MDI attachment points	M	Yes [ ]
PMAE17	Receiver differential input signals	147.5.5.1	Can be verified with a frame error ratio less than 1×10^{-7} for 125 octet frames	M	Yes [ ]
PMAE18	Alien crosstalk noise rejection	147.5.5.2	BER < 10^{-10} with an alien crosstalk noise of Gaussian distribution of magnitude of –101 dBm/Hz and bandwidth of 40 MHz at the MDI	M	Yes [ ]
PMAE19	PMA local loopback	147.5.6	The PMA shall be placed in loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, or in MDIO register 1.2297.13, defined in 45.2.1.234.5 is set to one	MDIO:O	Yes [ ] No [ ] N/A[ ]
PMAE20	PMA local loopback in half-duplex mode	147.5.6	The PMA and PCS Receive functions pass the data decoded from the signal to the MII RX	HALF*M DIO:M	Yes [ ] No [ ] N/A[ ]

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147.12.4.7 Point-to-point link Segment characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
PPLS1	Insertion loss	147.7.1	See Equation (147–3)	INS-P2P:M	Yes [ ]
PPLS2	Return loss	147.7.2	See Equation (147–4)	INS-P2P:M	Yes [ ]
PPLS3	Mode conversion loss	147.7.3	See Equation (147–5)	INS-P2P:M	Yes [ ]
PPLS4	Power sum ANEXT loss between a disturbed 10BASE-T1S link segment and the disturbing 10BASE-T1S link segment	147.7.4	Power sum alien near-end crosstalk (PSANEXT) loss shall meet Equation (147–6)	INS-P2P:M	Yes [ ]
PPLS5	Power sum AACRF loss between a disturbed 10BASE-T1S link segment and the disturbing 10BASE-T1S link segment	147.7.5	Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) loss shall meet Equation (147–7)	INS-P2P:M	Yes [ ]

147.12.4.8 Mixing Segment characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
MXS1	Insertion loss	147.8.1	See 147.7.1. Measured between any pair of MDI attachment points	INS-MIX:M	Yes [ ]
MXS2	Return loss	147.8.2	See 147.7.2. Measured with a reference impedance of 50 Ω	INS-MIX:M	Yes [ ]
MXS3	Mode conversion loss	147.8.3	See 147.7.3. Measured between any two MDI attachment points	INS-MIX:M	Yes [ ]

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147.12.4.9 MDI specification

Item	Feature	Subclause	Value/Comment	Status	Support
MDI1	MDI return loss when not in multidrop mode	147.9.2	Meet Equation (96–12)	M	Yes [ ]
MDI2	Minimum parallel impedance across the MDI attachment points when in multidrop mode	147.9.2	See Equation (147–8)	MULT: M	Yes [ ] N/A[ ]
MDI3	MDI line powering voltage tolerance	147.9.3	Up to 60 V dc with the source current limited to 2000 mA	M	Yes [ ]
MDI4	MDI fault tolerance	147.9.4	Withstand without damage the application of a short circuit of any wire to the other wire of the same pair or ground potential. Normal operation resumes after all short circuits are removed.	M	Yes [ ]

147.12.4.10 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	Delay constraints	147.11	Comply with Table 147–6	M	Yes [ ]

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148. PLCA Reconciliation Sublayer (RS)

148.1 Introduction

This clause specifies a Reconciliation Sublayer to provide optional Physical Layer Collision Avoidance (PLCA) capabilities among participating stations. The PLCA RS is specified for operation with Clause 147 (10BASE-T1S) PHYs operating in half-duplex multidrop mode. PLCA can be dynamically enabled or disabled via management interface. When PLCA is disabled, the Reconciliation Sublayer mapping is identical to that specified in Clause 22.

When enabled, the PLCA RS aligns data from the MAC with transmission opportunities of the Physical Layer and maps the Physical Layer signals to PLS primitives towards the MAC. The use of PLCA-enabled Physical Layers in CSMA/CD half-duplex shared-medium networks can provide enhanced bandwidth and improved access latency under heavily loaded traffic conditions. PLCA-enabled nodes can coexist with nodes without PLCA enabled on the same mixing segment, all using IEEE 802.3 CSMA/CD.

148.1.1 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

148.1.1.1 State diagram notation

The conventions of 21.5 are adopted with the extension that some states in the state diagrams use an IF-THEN-ELSE-END construct to condition which actions are taken within the state. If the logical expression associated with the IF evaluates TRUE, all the actions listed between THEN and ELSE will be executed. In the case where ELSE is omitted, the actions listed between THEN and END will be executed. If the logical expression associated with the IF evaluates FALSE, the actions listed between ELSE and END will be executed. After executing the actions listed between THEN and ELSE, between THEN and END, or between ELSE and END, the actions following the END, if any, will be executed.

148.1.1.2 State diagram timer specifications

All timers operate in the manner described in 40.4.5.2.

148.1.1.3 Service specifications

The method and notation used in the service specification follows the conventions of 1.2.2.

148.2 Overview

The working principle of PLCA is that transmit opportunities on a mixing segment are granted in sequence based on a node ID unique to the local collision domain (set by the management entity). The method of determination of the node ID and to_timer by the management entity is beyond the scope of this standard. Proper operation of the Clause 148 functionality assumes that the assigned node ID is unique in the local collision domain.

The node ID assignment value does not appear externally or in the payload packet format. The node ID assignment value is fully contained within the local collision domain.

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Transmit opportunities are generated in a round-robin fashion. The node with ID = 0 signals a BEACON on the medium. Reception of a BEACON indicates the start of a new cycle of transmit opportunities. If the node with ID = 0 fails, the network is still operational with the same performance level of a CSMA/CD network without PLCA.

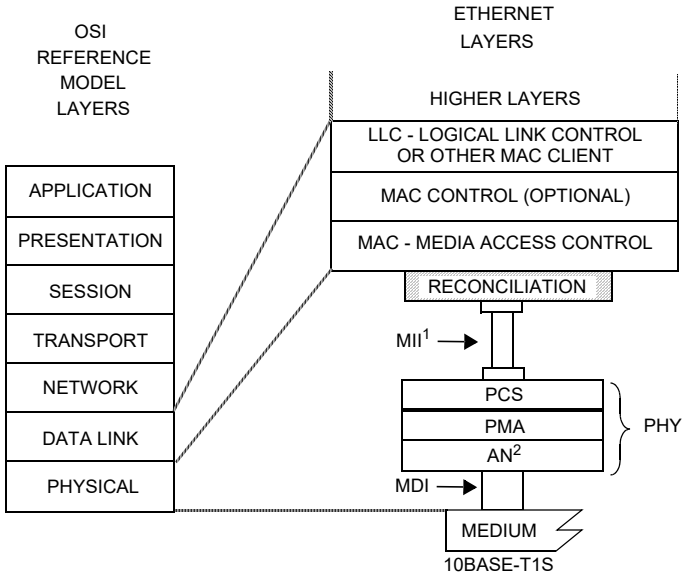
Each node is allowed to transmit a single packet during its own transmit opportunity. Individual nodes can be enabled to transmit a number of additional packets, up to the configured limit, within the same transmit opportunity.

PLCA relies on the PLS_SIGNAL.indication and PLS_CARRIER.indication primitives to have the MAC delay transmission until a transmit opportunity is available.

PLCA-enabled nodes may be used in the same CSMA/CD collision domain as non-PLCA enabled nodes. As the percentage of non-PLCA enabled nodes increases, performance advantages also decrease. If the node with ID = 0 fails, the network is still operational with the same performance level of a CSMA/CD network without PLCA.

148.3 Relationship with other IEEE standards

The relationship between the PLCA Reconciliation Sublayer, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet model is shown in Figure 148–1. The Reconciliation Sublayer (shown shaded) in Figure 148–1 connects one Clause 4 Media Access Control (MAC) layer to the PHY. MII is defined in Clause 22.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE

NOTE 1—MII is optional
NOTE 2—Auto-Negotiation is optional

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

Figure 148–1—Relationship of PLCA Reconciliation Sublayer to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model

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148.4 PLCA Reconciliation Sublayer operation

148.4.1 General

This subclause specifies services provided by the PLCA RS as an extension to the RS specified in Clause 22. Figure 148–2 depicts the RS interlayer service interfaces. The PLCA RS contains the Control and Data state diagrams, the variable delay line, and command detect logic. When PLCA functions are not supported or are disabled by the management interface (plca_en = FALSE), RS operation shall conform to the RS definition in Clause 22.

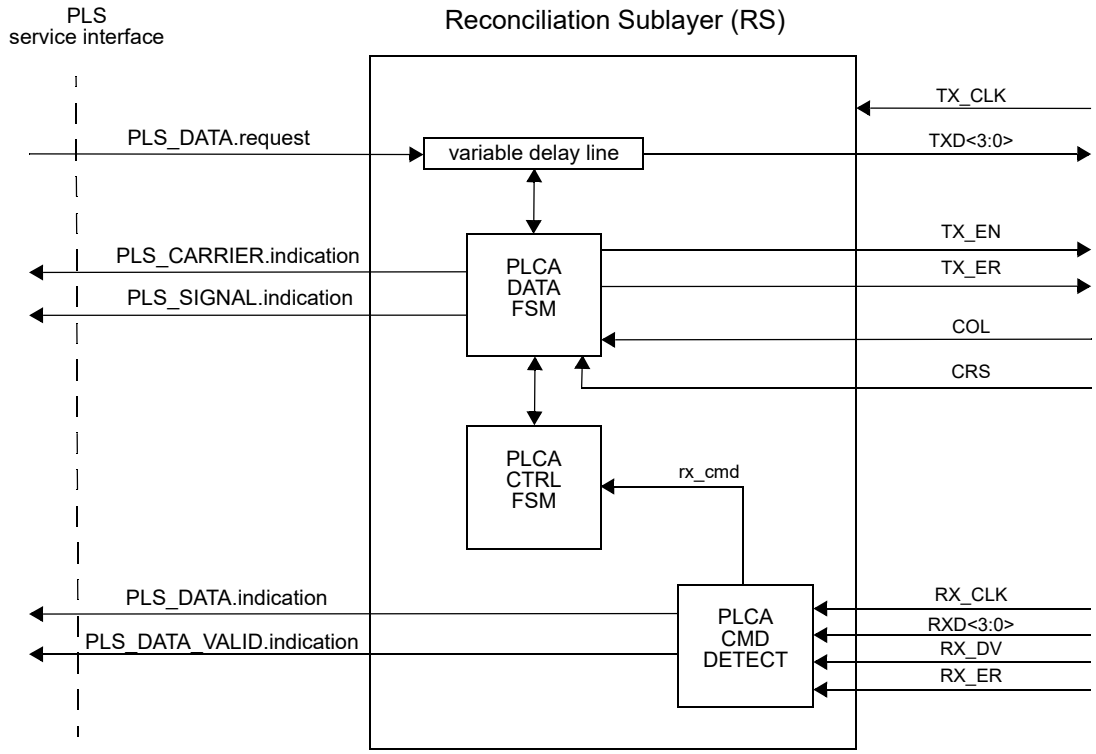

Figure 148–2—PLCA functions within the Reconciliation Sublayer (RS)

148.4.2 Mapping of MII signals to PLS service primitives and PLCA functions

The RS maps the signals provided at the MII to the PLS service primitives defined in Clause 6 via the PLCA state diagrams, variables, and functions (see 148.4.4 and 148.4.5). The PLS service primitives provided by the RS behave in exactly the same manner as defined in Clause 6.

148.4.2.1 Mapping of PLS_DATA.request

When PLCA is disabled (plca_en = FALSE), the mapping of the PLS_DATA.request primitive shall be the one specified in 22.2.1.1. Otherwise, the following applies.

148.4.2.1.1 Function

Maps the primitive PLS_DATA.request to PLCA variables which in turn generate the MII signals TXD<3:0> and TX_EN.

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148.4.2.1.2 Semantic of the service primitive

PLS_DATA.request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take one of three values: ONE, ZERO, or DATA_COMPLETE. It represents a single data bit. The values ONE and ZERO are conveyed by the individual bits of the four-bit variable plca_txd<3:0>. Each bit of plca_txd<3:0> conveys one bit of data while plca_txen is set to TRUE. The value DATA_COMPLETE is conveyed by setting the variable plca_txen to FALSE. MII signals TXD<3:0> and TX_EN are generated by way of the PLCA Data state diagrams specified in 148.4.5. Synchronization between the RS and the PHY is achieved by way of the TX_CLK signal.

148.4.2.1.3 When generated

The plca_txd<3:0> and plca_txen variables are assigned after every group of four PLS_DATA.request transactions from the MAC sublayer to request the PLCA functions to transmit a nibble of data when the transmit opportunity is available, or to signal the end of the transmission. The TX_CLK signal is generated by the PHY. The TXD<3:0> and TX_EN signals are generated by the RS according to PLCA Data state diagrams (see 148.4.5).

148.4.2.2 Mapping of PLS_DATA.indication

Map of the primitive PLS_DATA.indication shall comply with 22.2.1.2.

148.4.2.3 Mapping of PLS_CARRIER.indication

When PLCA is disabled (plca_en = FALSE), the mapping of the PLS_CARRIER.indication primitive shall be the one specified in 22.2.1.3. Otherwise, the following applies

148.4.2.3.1 Function

Maps the primitive PLS_CARRIER.indication to the PLCA Data state diagram.

148.4.2.3.2 Semantic of the service primitive

PLS_CARRIER.indication (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF.

148.4.2.3.3 When generated

The PLS_CARRIER.indication service primitive is generated by the RS according to the PLCA Data state diagram specified in 148.4.5.

148.4.2.4 Mapping of PLS_SIGNAL.indication

When PLCA is disabled (plca_en = FALSE) the mapping of the PLS_SIGNAL.indication primitive shall be the one specified in 22.2.1.4. Otherwise, the following applies.

148.4.2.4.1 Function

Map the primitive PLS_SIGNAL.indication to the PLCA Data state diagram.

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148.4.2.4.2 Semantic of the service primitive

PLS_SIGNAL.indication (SIGNAL_STATUS)

The SIGNAL_STATUS parameter can take one of two values: SIGNAL_ERROR or NO_SIGNAL_ERROR.

148.4.2.4.3 When generated

SIGNAL_STATUS is generated by the PLCA Data state diagram specified in 148.4.5.

148.4.2.5 Mapping of PLS_DATA_VALID.indication

Map of the primitive PLS_DATA_VALID.indication shall comply with 22.2.1.7.

148.4.2.6 Generation of TX_ER

Generation of TX_ER shall comply with the PLCA Data state diagram specified in 148.4.5.1.

148.4.2.7 Response to RX_ER indication

Response to RX_ER indication from the MII shall comply with 22.2.1.5.

148.4.3 Requirements for the PHY

In order to support PLCA, the RS has to be connected to a 10BASE-T1S PHY.

148.4.3.1 PHY response to PLCA commands and notifications

148.4.3.1.1 BEACON request

The BEACON function is specified in 148.4.4.1.

The RS conveys the BEACON request via MII interface.

Upon the reception of this request, the PHY encodes and transmits a signal communicating the BEACON to other PHYs on the segment so that they generate a BEACON indication.

Upon the reception of this request, the RX_DV signal is not asserted.

PHYs may map the BEACON request to any suitable line coding as long as the requirements defined in this subclause are met.

148.4.3.1.2 COMMIT request

The COMMIT function is specified in 148.4.4.1.

The PLCA Control state diagram generates a COMMIT request by way of the tx_cmd variable as specified in 148.4.4.2. The RS conveys such request via MII interface as defined in 22.2.2.4.

Upon the reception of this request, the RX_DV signal is not asserted.

PHYs may map the COMMIT request to any suitable line coding as long as the requirement defined in this subclause are met.

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148.4.3.2 Mapping of MII signals to PLCA variables

The PLCA RS is required to decode PLCA-specific signaling out of the MII.

148.4.3.2.1 BEACON indication

When the PHY receives a BEACON, it indicates this information to the RS by asserting MII signals.

The RS shall react to such indication by setting the PLCA variable rx_cmd to the value BEACON. The RS shall also reset the rx_cmd variable to NONE when the BEACON indication on the MII ceases, unless a COMMIT indication is signaled, in which case rx_cmd shall be set as specified in 148.4.3.2.2.

148.4.3.2.2 COMMIT indication

When the PHY receives a COMMIT from the line, it indicates this information to the RS by asserting MII signals. The PHY asserts CRS when a COMMIT indication is detected.

The RS shall react to such indication by setting the PLCA variable rx_cmd to the value COMMIT. The RS shall also reset the rx_cmd variable to NONE when the COMMIT indication on the MII ceases, unless a BEACON indication is signaled, in which case rx_cmd shall be set as specified in 148.4.3.2.1.

148.4.4 PLCA Control

148.4.4.1 PLCA Control state diagram

The PLCA Control function shall conform to the PLCA Control state diagram in Figure 148–3 and Figure 148–4 and associated state variables, functions, timers, and messages.

To achieve error free operation the PLCA node should be configured appropriately before transmit functions are enabled. Appropriate configuration includes the following:

a) Each local_nodeID is unique to the local collision domain.
b) There is one and only one node with local_nodeID = 0 on the local collision domain.
c) The transmit opportunity timer (to_timer) is set equal across all the nodes on the local collision domain.
d) plca_node_count is set on the node with local_nodeID = 0 to the maximum number of nodes supported on the local collision domain.

When PLCA functions are enabled and local_nodeID equals zero, PLCA switches to RECOVER state and waits one cycle of transmit opportunities. This prevents sending a BEACON at an inappropriate time (e.g., when the node with local_nodeID = 0 resets in the middle of a cycle of transmit opportunities and other nodes could still be sending valid data). A BEACON is then generated by such node by switching to SEND_BEACON state. On reception of a BEACON, all other nodes reset their own transmit opportunity counter and related timer.

When PLCA functions are enabled, nodes with nonzero local_nodeID wait in RESYNC state until a BEACON is received.

All nodes, including the one generating the BEACON, detect the end of the BEACON condition before proceeding to WAIT_TO state, in order to minimize latency differences across the network.

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Entering WAIT_TO state, the node waits for one of these possible conditions:

1) CRS is asserted by the PHY through MII, indicating there is activity on the line.
2) curID becomes equal to local_nodeID while packetPending variable is TRUE, meaning that this node now owns a transmit opportunity and does have a packet to transmit.
3) curID becomes equal to local_nodeID while packetPending variable is FALSE, meaning that this node now owns a transmit opportunity but does not have a packet to transmit.
4) to_timer elapses, indicating the current transmit opportunity is yielded.

If condition (1) occurs, the node is about to receive either a valid packet, a COMMIT request, a BEACON request or it might be receiving a false carrier event.

In EARLY_RECEIVE state, the PLCA Control state diagram is waiting for the PHY to properly decode the incoming signal and to take the following actions:

— Switch to RECEIVE state if a COMMIT indication is reported or a valid packet is being decoded. The PLCA Control state diagram then remains in the RECEIVE state until the line is free (CRS deasserted).
— Switch to SYNCING state if a BEACON is received with local_nodeID ≠ 0, which starts a new cycle of transmit opportunities.
— Switch to RESYNC state if CRS is not followed by the reception of a packet and local_nodeID ≠ 0, meaning that a false carrier occurred and the curID variable might be out of synchronization. In this case, the node skips its transmit opportunity (TO) and waits for a new BEACON in order not to disrupt the current cycle of transmit opportunities.
— Switch to RECOVER state if local_nodeID is 0 and CRS is de-asserted but no packet is being received. In RECOVER state, since the curID variable might be out of synchronization, this node waits for the end of the current cycle of transmit opportunities before sending a new BEACON. This is required so as not to send a BEACON while other nodes might still be using their TO.

When condition (2) occurs, the node now gets a TO having at least one packet to be transmitted. COMMIT state is then entered to signal other nodes to stop their to_timer and wait for a packet by the means of a COMMIT request. COMMIT state is left once the data to be transmitted is available from the MAC or the PLCA delay line.

When condition (3) occurs, the node now gets a TO without being ready to send any packet. In this case, the YIELD state is entered to skip the TO, allowing other nodes a chance to transmit. In some rare cases (e.g., a non-PLCA enabled node is connected to the network) it is possible to receive data in YIELD state. If this unlikely event happens, PLCA switches to RECEIVE state to wait until the end of the transmission and increment curID properly.

When condition (4) is met, another node has yielded its transmit opportunity, causing the curID variable to be incremented and to_timer to be reset.

148.4.4.2 PLCA Control variables

plca_reset

The plca_reset signal is used to reset the optional PLCA function in the RS. This signal maps to TRUE when acPLCAReset is in reset and to FALSE when acPLCAReset is normal, but is further qualified.
Values: TRUE or FALSE

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plca_en

The plca_en signal controls the optional PLCA function in the RS. This signal maps to TRUE when aPLCAAdminState is enabled and to FALSE when aPLCAAdminState is disabled.
Values: TRUE or FALSE

CRS

The MII signal CRS.
Values: TRUE or FALSE

RX_DV

The MII signal RX_DV.
Values: TRUE or FALSE

receiving

Defined as: (RX_DV = TRUE) + (rx_cmd = COMMIT).
Values: TRUE or FALSE

tx_cmd

Command for the PLCA Data state diagram to convey to the PHY via the MII.
Values: NONE, BEACON or COMMIT

rx_cmd

Encoding present on RXD<3:0>, RX_ER, and RX_DV as defined in Table 22–2.
Values:
BEACON: PLCA BEACON indication encoding present on RXD<3:0>, RX_ER, and RX_DV
COMMIT: PLCA COMMIT indication encoding present on RXD<3:0>, RX_ER, and RX_DV
NONE: PLCA BEACON or COMMIT indication encoding not present on RXD<3:0>, RX_ER, and RX_DV

TX_EN

The MII signal TX_EN.
Values: TRUE or FALSE

local_nodeID

ID representing the PLCA transmit opportunity number assigned to the node. This signal maps to aPLCALocalNodeID.
Values: integer value from 0 to 255

plca_node_count

Maximum number of PLCA nodes on the mixing segment receiving transmit opportunities before the node with local_nodeID = 0 generates a new BEACON, reflecting the value of aPLCANodeCount. This parameter is meaningful only for the node with local_nodeID = 0; otherwise, it is ignored.
Values: integer number from 0 to 255

committed

Internal variable used to synchronize PLCA Control and Data functions.
It is set by PLCA Control state diagram to signal that the current transmit opportunity has been committed and the PLCA Data state diagram is now allowed to convey MII data to the PHY.
Values: TRUE or FALSE

packetPending

Internal variable used to synchronize PLCA Control and Data functions.
The PLCA Data state diagram sets this variable when it detects the MAC is ready to send a packet and have PLCA Control state diagram actually commit for the next available transmit opportunity.
Values: TRUE or FALSE

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bc

Counts the number of additional packets currently sent in a burst after the first transmission.
Values: integer from 0 to 255

max_bc

Maximum number of additional packets the node is allowed to transmit in a single burst. This signal maps to aPLCAMaxBurstCount attribute.
Values: integer from 0 to 255

plca_active

Notifies the PLCA Status function whether the node is waiting for sending or receiving a BEACON or it already sent or received one.
Values: TRUE or FALSE

curID

Integer variable tracking the ID of the node that currently owns a transmit opportunity.
Values: integer from 0 to 255

PMCD

Prescient mii_clock_timer_done. This variable is set to FALSE on entry to the RESYNC state and becomes TRUE 1 ± ½ bit time prior to mii_clock_timer_done becoming TRUE.
Values: TRUE or FALSE

148.4.4.3 Functions

No functions are defined for the PLCA Control state diagram.

148.4.4.4 Timers

beacon_timer

Times the duration of the BEACON signal.
Duration: 20 bit times.
Tolerance: ± ½ bit time.

beacon_det_timer

Timer for detecting received BEACONs.
Duration: 22 bit times.
Tolerance: ± 1 bit time.

invalid_beacon_timer

Timer used for BEACON validation. This timer is stopped any time rx_cmd = BEACON.
Duration: 4000 ns.
Tolerance: ± 400 ns.

burst_timer

This timer determines how long to wait for the MAC to send a new packet before yielding the transmit opportunity. For PLCA burst mode to work properly this timer should be set greater than one IPG. Timer duration maps to aPLCABurstTimer attribute.
Duration: integer number between 0 and 255, expressed in bit times.
Tolerance: ± ½ bit time.
The default value is specified in 30.16.1.1.7.

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to_timer

The transmit opportunity timer maps to aPLCATransmitOpportunityTimer. The timer value needs to meet Equation (148–1). The to_timer should be set equal across the mixing segment for PLCA to work properly.

$$\begin{aligned} to\_timer > {} & 2 \times \max(t_{propdelay}) + \\ & \max(TX\_EN\ sampled\ to\ MDI\ output) + \\ & \max(MDI\ input\ to\ CRS\ asserted) + \\ & \max(MDI\ input\ to\ CRS\ deasserted) - \\ & \min(MDI\ input\ to\ CRS\ deasserted) + \\ & \max(MII\ propagation\ delay) \end{aligned} \tag{148–1}$$

where $t_{propdelay}$ is the propagation delay between any two nodes on the mixing segment, and the delay specifications are the maxima and minima for the PHY type on the mixing segment (for 10BASE-T1S, see 147.11).

Duration: integer number between 1 and 255, expressed in bit times.
Tolerance: 100 ppm.
The default value is specified in 30.16.1.1.5.

148.4.4.5 Abbreviations

MCD See 148.4.5.5

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148.4.4.6 State diagram

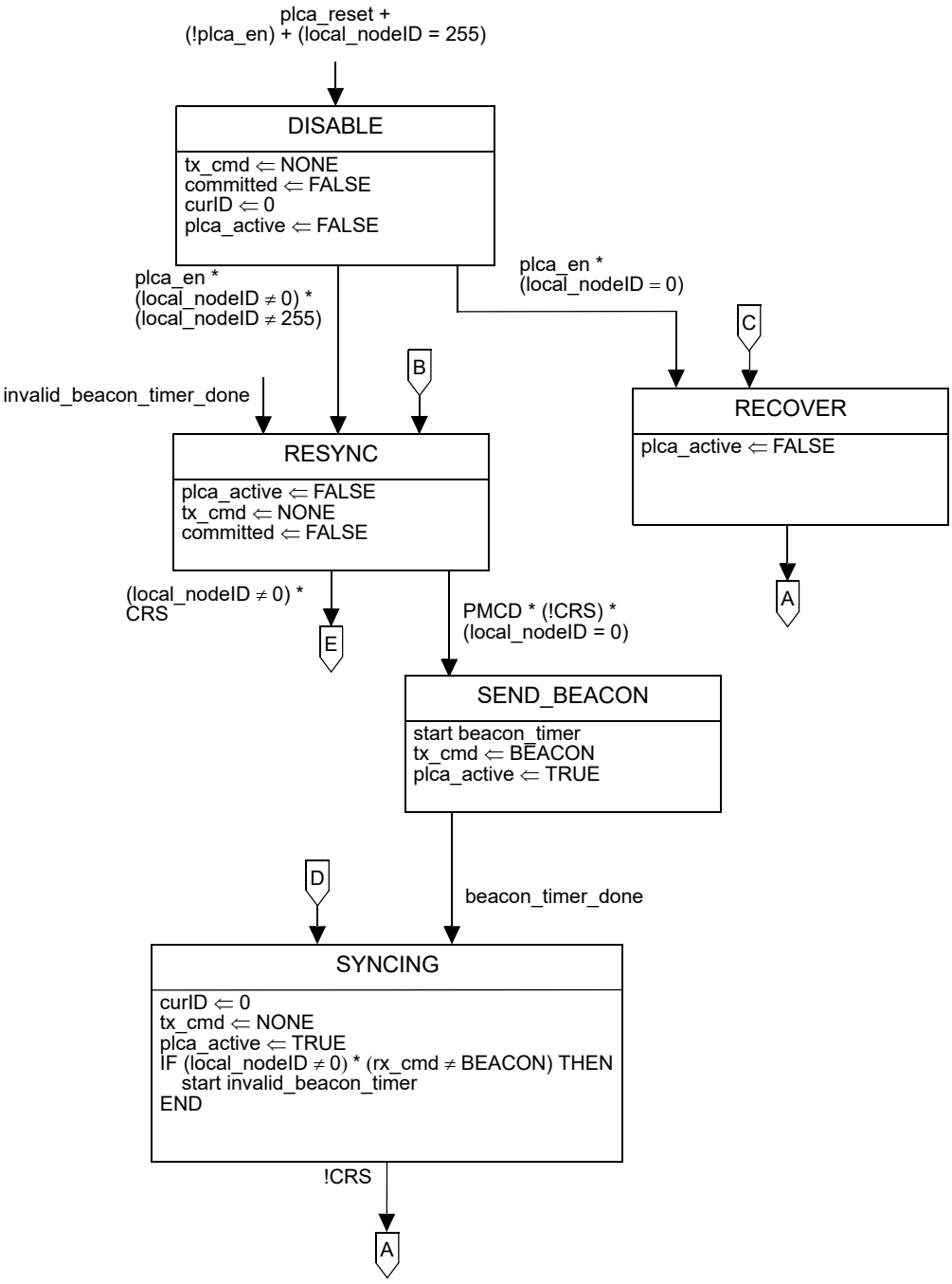

Figure 148–3—PLCA Control state diagram, part a

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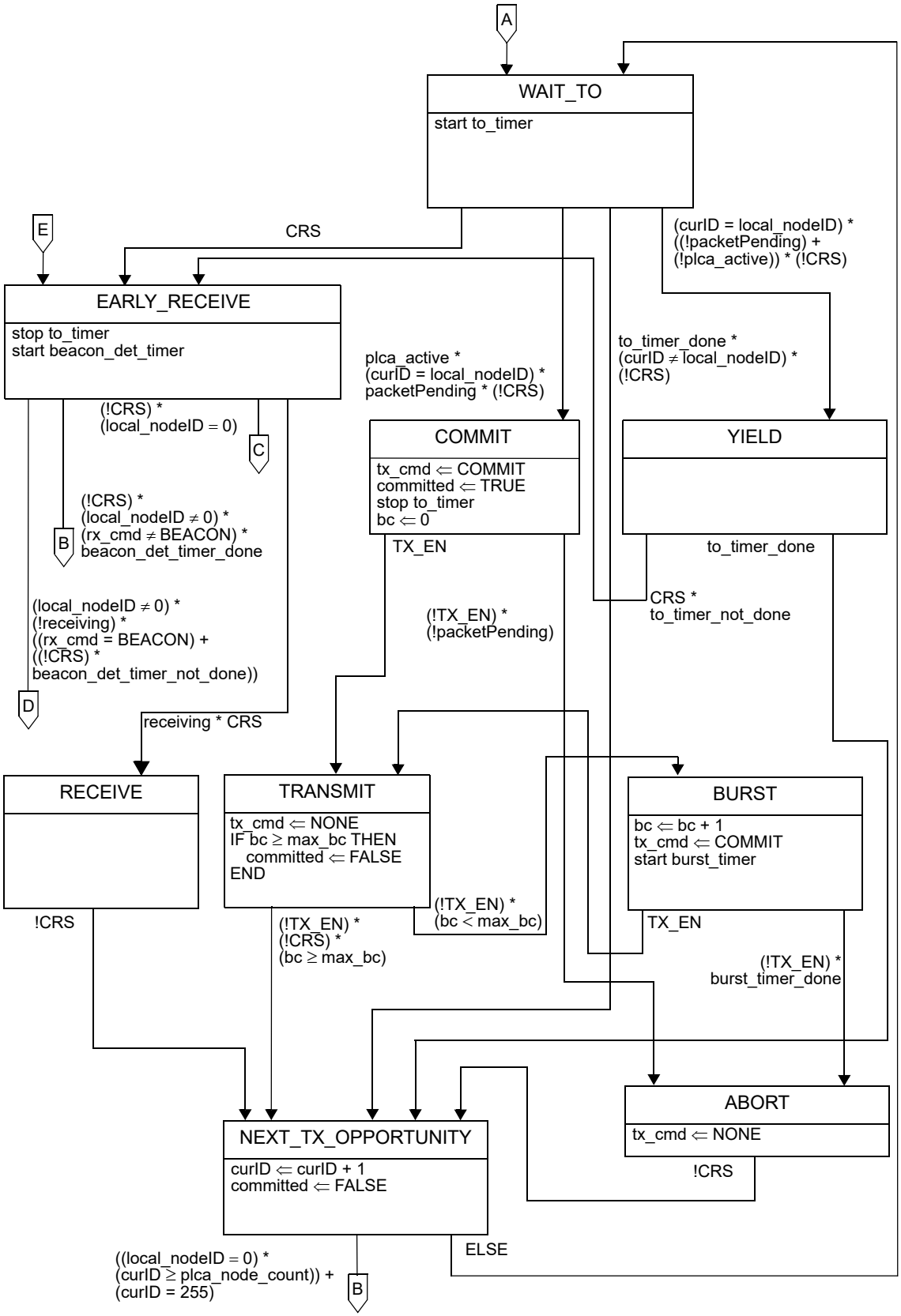

Figure 148–4—PLCA Control state diagram, part b

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148.4.5 PLCA Data

148.4.5.1 PLCA Data state diagram

The PLCA Data state diagram is responsible for detecting when the MAC is ready to send a packet and delaying the transmission until a transmit opportunity is detected.

The PLCA Data function shall conform to the PLCA Data state diagram in Figure 148–5 and Figure 148–6 and associated state variables, functions, timers, and messages.

When PLCA functions are enabled, the PLCA Data state diagram transitions to the IDLE state and waits for the MAC to start a transmission or the PHY to assert carrier sense. In the former case, the data conveyed by the MAC through the PLS_DATA.request primitive is delayed by switching to HOLD state. In the latter case, CARRIER_ON is signaled through the PLS_CARRIER.indication to have the MAC defer any new transmission, then the RECEIVE state is entered.

The MAC however, might have started a transmission right before a carrier is detected. In this case, the Data state diagram switches to the COLLIDE state asserting SIGNAL_STATUS = SIGNAL_ERROR via PLS_SIGNAL.indication primitive to have the MAC perform a backoff and send the packet again later, without actually forwarding any data for the PHY to transmit on the medium.

During the HOLD state, the PLCA Control state diagram is notified via the packetPending variable that data is available to be transmitted and the beginning of the transmission is held in the variable delay line. At the next transmit opportunity, the PLCA Control state diagram allows transmitting the delayed data by setting the committed variable to TRUE. In such a case, the PLCA Data state diagram switches to TRANSMIT state to actually deliver the data for the PHY to encode and transmit on the medium.

The variable delay line is a small buffer that aligns a transmission with the transmit opportunity.

If plca_txer is asserted during the HOLD state, the PLCA Data state diagram switches to ABORT state to assert packetPending = FALSE and to wait until the MAC stops sending data. The aborted packet will not be transmitted on the medium.

If another node starts a transmission during the HOLD state, the delayed data is dropped and a collision is triggered by switching to COLLIDE state.

During the COLLIDE state, packetPending = FALSE and CARRIER_STATUS = CARRIER_ON are asserted via the PLS_CARRIER.indication primitive. When the MAC has completed sending the jam bits as described in Clause 4, the PLCA Data state diagram waits for the next transmit opportunity by switching to DELAY_PENDING state. The PLCA Data state diagram transitions to the PENDING state after waiting for the pending_timer. The pending_timer is used to prevent committing to a transmit opportunity before transmit data is available. This prevents conveying unwanted long COMMIT requests to the PHY.

During the PENDING state, the PLCA Data state diagram asserts packetPending = TRUE and keeps CARRIER_STATUS = CARRIER_ON via the PLS_CARRIER.indication primitive to prevent the MAC from making new transmit attempts until the PLCA Control state diagram signals that a new transmit opportunity is available. At that point, CARRIER_STATUS is set to CARRIER_OFF to have the MAC resend data after waiting one IPG period as described in Clause 4.

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148.4.5.2 Variables

a
: Current delay counter.

b
: Flush counter.

CARRIER_STATUS
: See 148.4.2.3.2.

COL
: The MII signal COL specified in 22.2.2.12.

committed
: See 148.4.4.2.

CRS
: The MII signal CRS (see 22.2.2.11).

packetPending
: See 148.4.4.2.

plca_en
: See 148.4.4.2.

plca_reset
: See 148.4.4.2.

plca_status
: See 148.4.6.2.

plca_txd<3:0>
: A four-bit data value conveying a nibble of data to transmit from four successive PLS_DATA.request(OUTPUT_UNIT) primitives where OUTPUT_UNIT has a value of ONE or ZERO. See 148.4.2.1.2. The addition of a subscript 'n-a', i.e., $plca\_txd_{n-a}$ indicates the plca_txd conveyed ‘a’ mii_clock_timer expirations before the most recent one.

plca_txen
: See 148.4.2.1.2.

plca_txer
: The conditions for generating plca_txer are the same as defined in 22.2.1.6 and 22.2.2.5 for the TX_ER MII signal.
Values: TRUE or FALSE

receiving
: See 148.4.4.2.

rx_cmd
: See 148.4.4.2.

SIGNAL_STATUS
: See 148.4.2.4.2

tx_cmd
: See 148.4.4.2.

tx_cmd_sync
: The value of the tx_cmd variable sampled on the rising edge of the MII TX_CLK.
Values: see tx_cmd in 148.4.4.2

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TXD
: The MII signals TXD<3:0> specified in 22.2.2.4.

TX_EN
: The MII signal TX_EN specified in 22.2.2.3.

TX_ER
: The MII signal TX_ER specified in 22.2.2.5.

148.4.5.3 Functions

ENCODE_TXER
: This function takes as its argument the tx_cmd_sync variable defined in 148.4.5.2.
It returns TRUE if tx_cmd_sync is BEACON or COMMIT. Otherwise, it returns the value of the plca_txer variable, defined in 148.4.5.2.

ENCODE_TXD
: This function takes as its argument the tx_cmd_sync variable defined in 148.4.5.2.
If tx_cmd_sync is BEACON, the return value is the TXD encoding defined in Table 22–1 for the BEACON request.
If tx_cmd_sync is COMMIT, the return value is the TXD encoding defined in Table 22–1 for the COMMIT request.
Otherwise, the return value is 0000.

148.4.5.4 Timers

commit_timer
: Defines the maximum time the PLCA Data state machine is allowed to stay in WAIT_MAC state.
Duration: 288 bit times.
Tolerance: ± ½ bit time.

mii_clock_timer
: A continuous free-running timer that shall expire synchronously with the rising edge of the MII TX_CLK.
Restart time: Immediately after expiration; restarting the timer resets the condition mii_clock_timer_done.
Duration: see 22.2.2.1.

pending_timer
: Defines the time the PLCA Data state diagram waits in the DELAY_PENDING state before switching to PENDING state.
Duration: 512 bit times.
Tolerance: ± ½ bit time.

148.4.5.5 Abbreviations

MCD Alias for mii_clock_timer_done

148.4.5.6 Constants

delay_line_length
: This constant is implementation dependent and specifies the maximum number of nibbles that the PLCA RS variable delay line can hold.
Value: up to 99

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148.4.5.7 State diagram

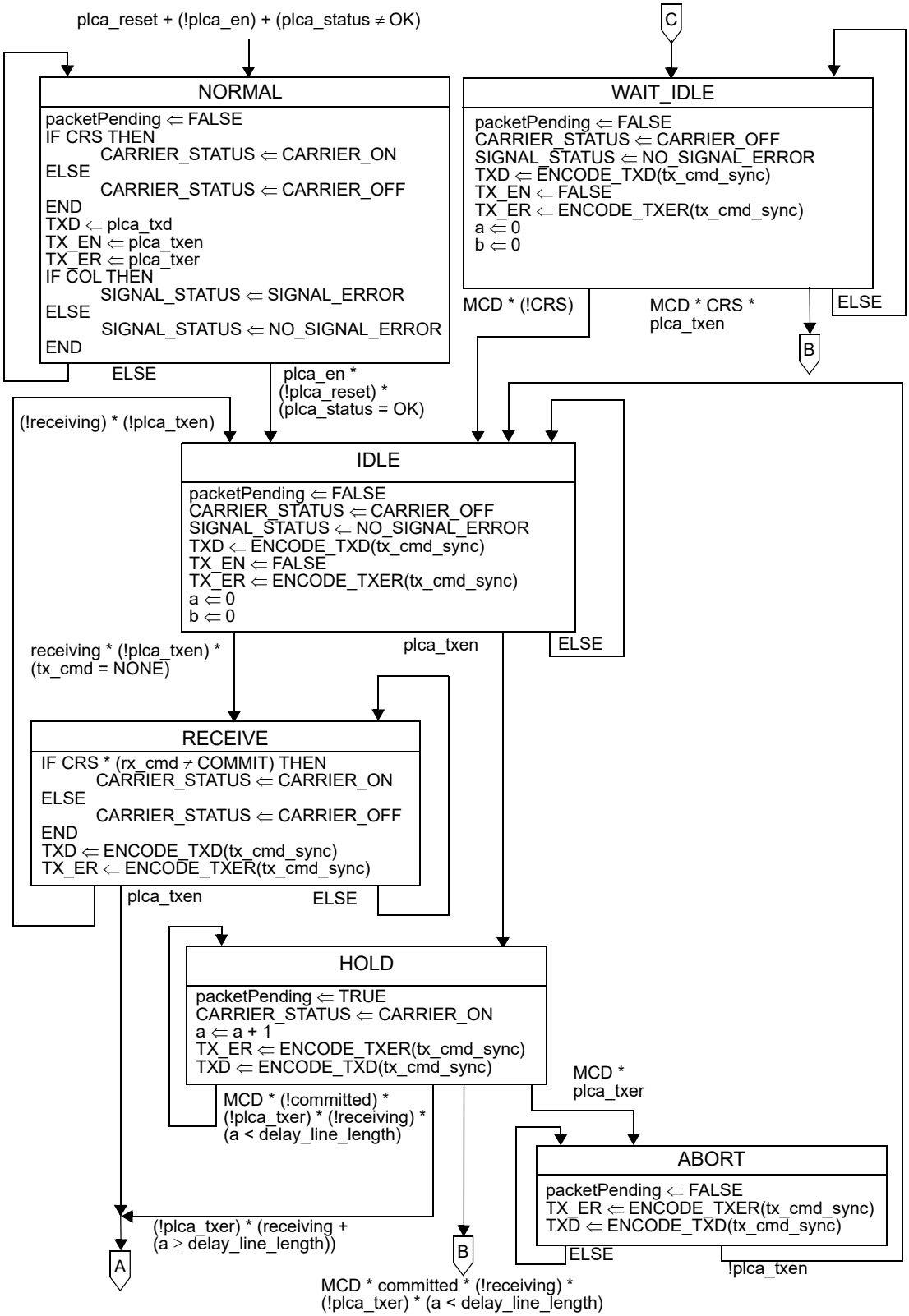

Figure 148–5—PLCA Data state diagram, part a

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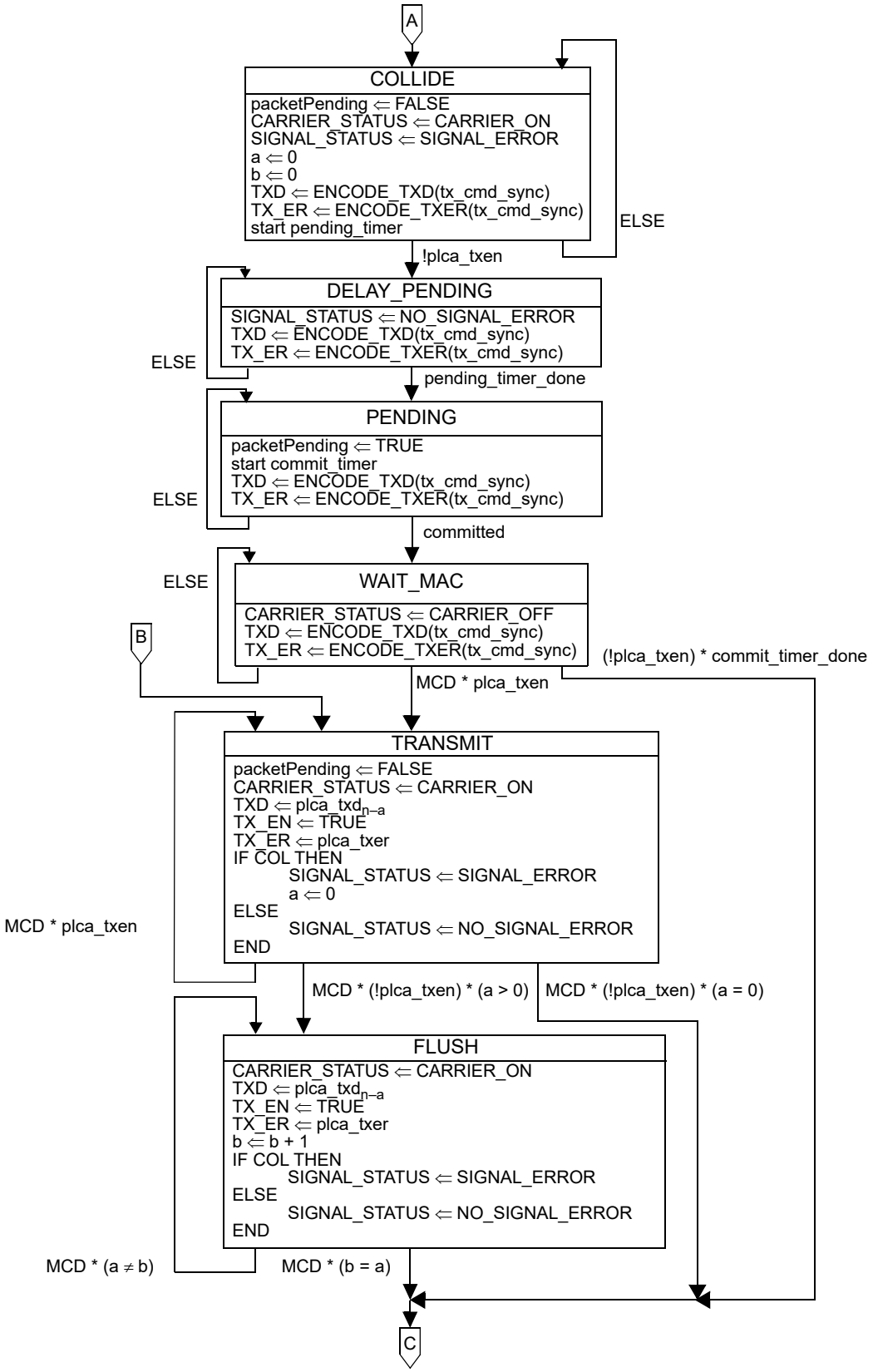

Figure 148–6—PLCA Data state diagram, part b

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148.4.6 PLCA Status

148.4.6.1 PLCA Status state diagram

The PLCA Status state diagram is responsible for reporting whether nodes are actively sending/receiving the BEACON. The PLCA Status function shall conform to the PLCA Status state diagram in Figure 148–7 and associated state variables, functions, timers, and messages.

Upon reset or when PLCA is disabled, the PLCA Status function enters the INACTIVE state and reports plca_status as FAIL. As soon as the PLCA Control function enters the SYNCING state (i.e., receiving or transmitting the BEACON), the plca_active variable is set to TRUE and PLCA Status switches to the ACTIVE state, reporting plca_status as OK.

From the ACTIVE state, whenever plca_active is set to FALSE by the PLCA Control function, the PLCA Status function enters the HYSTERESIS state, still reporting plca_status as OK and arming plca_status_timer.

If plca_active is reset to TRUE, then PLCA Status reverts to the ACTIVE state, effectively filtering the momentarily inactive state. Instead, if plca_status_timer expires while plca_active is still FALSE, the PLCA Status function reverts to the INACTIVE state, reporting plca_status as FAIL.

148.4.6.2 PLCA Status variables

plca_status
: If plca_status is OK, BEACONs are being received or transmitted, and the PLCA Control state diagram is in normal operation. If plca_status is FAIL, the PLCA Control state diagram has been in the DISABLE, RESYNC, or RECOVER state for greater than the duration of the plca_status timer. This signal maps to aPLCAStatus attribute as specified in 30.16.1.1.2.
Values: OK or FAIL

plca_active
: See 148.4.4.2.

plca_en
: See 148.4.4.2.

plca_reset
: See 148.4.4.2.

148.4.6.3 Functions

No functions are defined for PLCA Status state diagram.

148.4.6.4 Timers

plca_status_timer
: Represents the time plca_status is maintained in OK state when plca_active is FALSE while in the HYSTERESIS state.
Duration: the duration of this timer is 130 090 bit times, which is 2 × (max to_timer × max plca_node_count + beacon_timer).
Tolerance: timer may expire up to 10 000 BT (nominally 1 ms at 10 Mb/s) greater than the specified duration

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148.4.6.5 State diagram

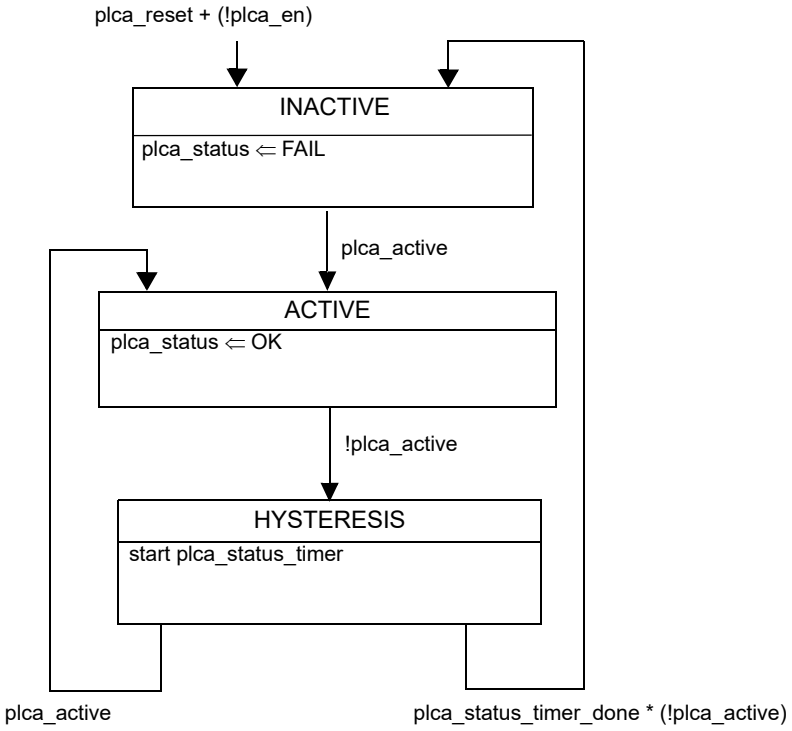

Figure 148–7—PLCA Status state diagram

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148.5 Protocol implementation conformance statement (PICS) proforma for Clause 148, PLCA Reconciliation Sublayer (RS)[244]

148.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 148, PLCA Reconciliation Sublayer (RS), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

148.5.2 Identification

148.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

148.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 148, PLCA Reconciliation Sublayer (RS)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[244]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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148.5.3 PICS proforma tables for PLCA Reconciliation Sublayer (RS)

148.5.3.1 Reconciliation Sublayer

Item	Feature	Subclause	Value/Comment	Status	Support
RS1	PLCA not supported or disabled by management interface	148.4.1	Conform to MII RS definition in Clause 22	M	Yes [ ]

148.5.3.2 Mapping of MII signals to PLS service primitives and PLCA functions

Item	Feature	Subclause	Value/Comment	Status	Support
MAP1	Mapping of PLS_DATA.request when PLCA is disabled	148.4.2.1	Specified in 22.2.1.1	M	Yes [ ]
MAP2	Mapping of PLS_DATA.indication	148.4.2.2	Specified in 22.2.1.2	M	Yes [ ]
MAP3	Mapping of PLS_CARRIER.indication when PLCA is disabled	148.4.2.3	Specified in 22.2.1.3	M	Yes [ ]
MAP4	Mapping of PLS_CARRIER.indication when PLCA is enabled	148.4.2.3.1	Maps the primitive PLS_CARRIER.indication to the PLCA Data state diagram	M	Yes [ ]
MAP5	Mapping of PLS_SIGNAL.indication when PLCA is disabled	148.4.2.4	Specified in 22.2.1.4	M	Yes [ ]
MAP6	Mapping of PLS_SIGNAL.indication when PLCA is enabled	148.4.2.4.1	Map the primitive PLS_SIGNAL.indication to the PLCA Data state diagram	M	Yes [ ]
MAP7	Mapping of PLS_DATA_VALID.indication	148.4.2.5	Specified in 22.2.1.7	M	Yes [ ]
MAP8	Generation of TX_ER	148.4.2.6	Specified in 148.4.5.1	M	Yes [ ]
MAP9	Response to RX_ER indication	148.4.2.7	Specified in 22.2.1.5	M	Yes [ ]

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148.5.3.3 Specific RS and PHY specification

Item	Feature	Subclause	Value/Comment	Status	Support
PLCA1	RS reaction to BEACON indication reception	148.4.3.2.1	PLCA variable rx_cmd is set to the value BEACON	M	Yes [ ]
PLCA2	RS reaction when BEACON indication ceases	148.4.3.2.1	PLCA variable rx_cmd is reset to NONE unless a COMMIT indication is signaled, in which case rx_cmd shall be set as specified in 148.4.3.2.2	M	Yes [ ]
PLCA3	RS reaction to COMMIT indication reception	148.4.3.2.2	PLCA variable rx_cmd is set to the value COMMIT	M	Yes [ ]
PLCA4	RS reaction when COMMIT indication ceases	148.4.3.2.2	PLCA variable rx_cmd is reset to NONE unless a BEACON indication is signaled, in which case rx_cmd shall be set as specified in 148.4.3.2.1	M	Yes [ ]

148.5.3.4 PLCA Control

Item	Feature	Subclause	Value/Comment	Status	Support
CON1	PLCA Control function	148.4.4.1	Conform to Figure 148–3 and Figure 148–4	M	Yes [ ]

148.5.3.5 PLCA Data

Item	Feature	Subclause	Value/Comment	Status	Support
DAT1	PLCA Data function	148.4.5.1	Conforms to Figure 148–5 and Figure 148–6	M	Yes [ ]

148.5.3.6 PLCA Status

Item	Feature	Subclause	Value/Comment	Status	Support
STS1	PLCA Status function	148.4.6.1	Conforms to Figure 148–7	M	Yes [ ]

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149. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1

149.1 Overview

This clause defines the type 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 Physical Coding Sublayer (PCS) as well as the 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 Physical Medium Attachment (PMA) sublayers. Together, the corresponding PCS and PMA sublayers comprise a 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 Physical Layer device (PHY). Provided in this clause are functional and electrical specifications for the type 2.5GBASE-T1 PCS and PMA, 5GBASE-T1 PCS and PMA, and 10GBASE-T1 PCS and PMA.

The 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs are intended to be operated over a single balanced pair of conductors. The link segment specifications defined in 149.7 were derived from automotive requirements, but may also be used for non-automotive applications. The conductors supporting the operation of the 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs are defined in terms of performance requirements between the Medium Dependent Interfaces (MDIs) allowing implementers to provide their own conductors to operate the 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs as long as the normative requirements included in 149.7 are met.

This clause also specifies an optional Energy-Efficient Ethernet (EEE) capability. A 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHY that supports this capability may enter a Low Power Idle (LPI) mode of operation during periods of low link utilization as described in Clause 78.

149.1.1 Nomenclature

The 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs described in this clause represent three distinct PHY types that share the same PCS, PMA, and MDI specifications subject to frequency scaling. In order to efficiently describe the three PHYs, the nomenclature MultiGBASE-T1 is used to describe specifications that apply to the 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs. Additionally, for parameters that scale with the PHY's data rate, the parameter *S* is used for scaling, see Table 149–1.

Table 149–1—Scaling parameter

PHY type	*S*
10GBASE-T1	1
5GBASE-T1	0.5
2.5GBASE-T1	0.25

149.1.2 Relationship of 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 to other standards

The relationship between the 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model are shown in Figure 149–1. The PHY sublayers (shown shaded) in Figure 149–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto-Negotiation for 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs is defined in Clause 98. The XGMII is defined in Clause 46.

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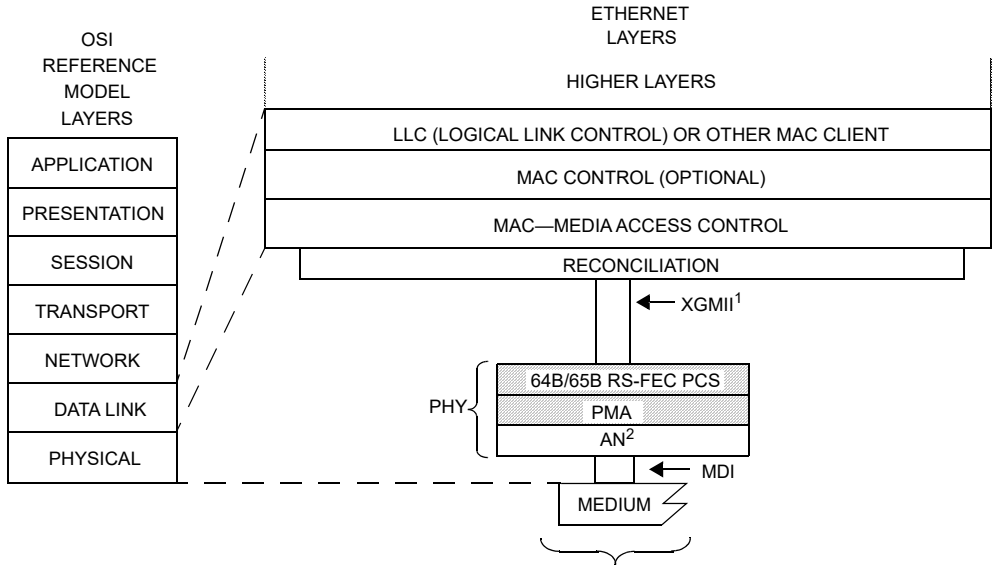

MDI = MEDIUM DEPENDENT INTERFACE
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE

NOTE 1—XGMII is optional
NOTE 2—Auto-Negotiation is optional

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

Figure 149–1—Relationship of 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model

149.1.3 Operation of 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1

The 2.5GBASE-T1 PHY, 5GBASE-T1 PHY, and 10GBASE-T1 PHY each operate using full-duplex communications over a single balanced pair of conductors with an effective rate of 2.5 Gb/s, 5 Gb/s, or 10 Gb/s in each direction simultaneously while meeting the requirements (EMC, temperature, etc.) of automotive environments. The PHY supports operation on an automotive link segment supporting up to four in-line connectors using a single balanced pair of conductors for up to at least 15 m. The 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs utilize 4-level pulse amplitude modulation (PAM4) transmitted at 1406.25 MBd, 2812.5 MBd, and 5625 MBd rates, respectively. A 33-bit scrambler is used to improve the EMC performance. XGMII TX_D, TX_EN, and TX_ER are encoded together using 64B/65B encoding. To maintain a bit error ratio (BER) of less than or equal to 10^{-12}, the 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs add 340 bits of Reed-Solomon forward error correction (RS-FEC) parity to each group of 50 64B/65B blocks. The PAM4 mapping, scrambler, RS-FEC, interleaver, and PAM4 encoder/decoder are all contained in the PCS (see 149.3).

Auto-Negotiation (Clause 98) may optionally be used by 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for normal operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding. The implementation of the Auto-Negotiation function is optional. If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.

A 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHY shall be capable of operating as MASTER or SLAVE, per runtime configuration. A MASTER PHY uses a local clock to determine the timing of transmitter operations. A SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations. When Auto-Negotiation is used, the MASTER-SLAVE relationship between two devices sharing a link segment is established during Auto-Negotiation (see Clause 98). If

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Auto-Negotiation is not used, a MASTER-SLAVE relationship shall be established by management or hardware configuration of the PHYs, and the MASTER and SLAVE are synchronized by the PHY Link Synchronization function in the PHY (see 149.4.2.6).

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

A 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHY may optionally support Energy-Efficient Ethernet (see Clause 78) and advertise the EEE capability as described in 149.4.2.4.5. The EEE capability is a mechanism by which 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHYs are able to reduce power consumption during periods of low link utilization.

The 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHY may optionally support the MultiGBASE-T1 PCS-based operations, administration, and maintenance (OAM). The MultiGBASE-T1 OAM is useful for monitoring link operation by exchanging PHY link health status and messages. The MultiGBASE-T1 OAM information is exchanged between two 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHYs out of band, that is, outside of the specified 2.5 Gb/s, 5 Gb/s, or 10 Gb/s Ethernet data stream. The MultiGBASE-T1 OAM is specified in 149.3.9, and the 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHY advertises its MultiGBASE-T1 OAM capability as described in 149.4.2.4.5.

The 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PMA couples messages from the PCS to the MDI and provides clock recovery, link management, and PHY Control functions. The PMA provides full duplex communications at 1406.25 MBd for 2.5GBASE-T1, 2812.5 MBd for 5GBASE-T1, and 5625 MBd for 10GBASE-T1 over the single balanced pair of conductors. PMA functionality is described in 149.4. The MDI is specified in 149.8. Figure 149–2 shows the functional block diagram.

149.1.3.1 Physical Coding Sublayer (PCS)

The MultiGBASE-T1 PCS couples a 10 Gigabit Media Independent Interface (XGMII), as described in Clause 46, to the 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 Physical Medium Attachment (PMA) sublayer.

In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in normal mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 50 blocks. The contents of each group are contained in a vector tx_group50x65B. Next, a 10-bit OAM field is appended to form a 3260-bit block. A number, L, of these 3260-bit blocks are formed into an RS-FEC input superframe, then encoded by the RS-FEC (360, 326, 2^{10}) and the round–robin interleaving as described in 149.3.2.2.16. The RS-FEC output superframe consists of L × 3600 bits. The duration of the superframe is L × 320 / *S* ns. Finally these bits are exclusive OR’d with a degree 33 scrambler to create the MultiGBASE-T1 payload. PCS transmit functions are described in 149.3.2.2.

tx_group50x65B<3249:0> is defined as:

$$\text{tx\_group50x65B}\langle 65 \times i + j \rangle = \text{tx\_coded}_i\langle j \rangle$$

where i = 0 to 49, j = 0 to 64, and tx_coded_i<64:0> is the ith 64B/65B block where tx_coded_0<64:0> is the first block transmitted.

In the training mode (see 149.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges EEE and MultiGBASE-T1 OAM capabilities.

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Details of the PCS functions and state diagrams are covered in 149.3. The interface to the PMA is an abstract message-passing interface specified in 149.4.

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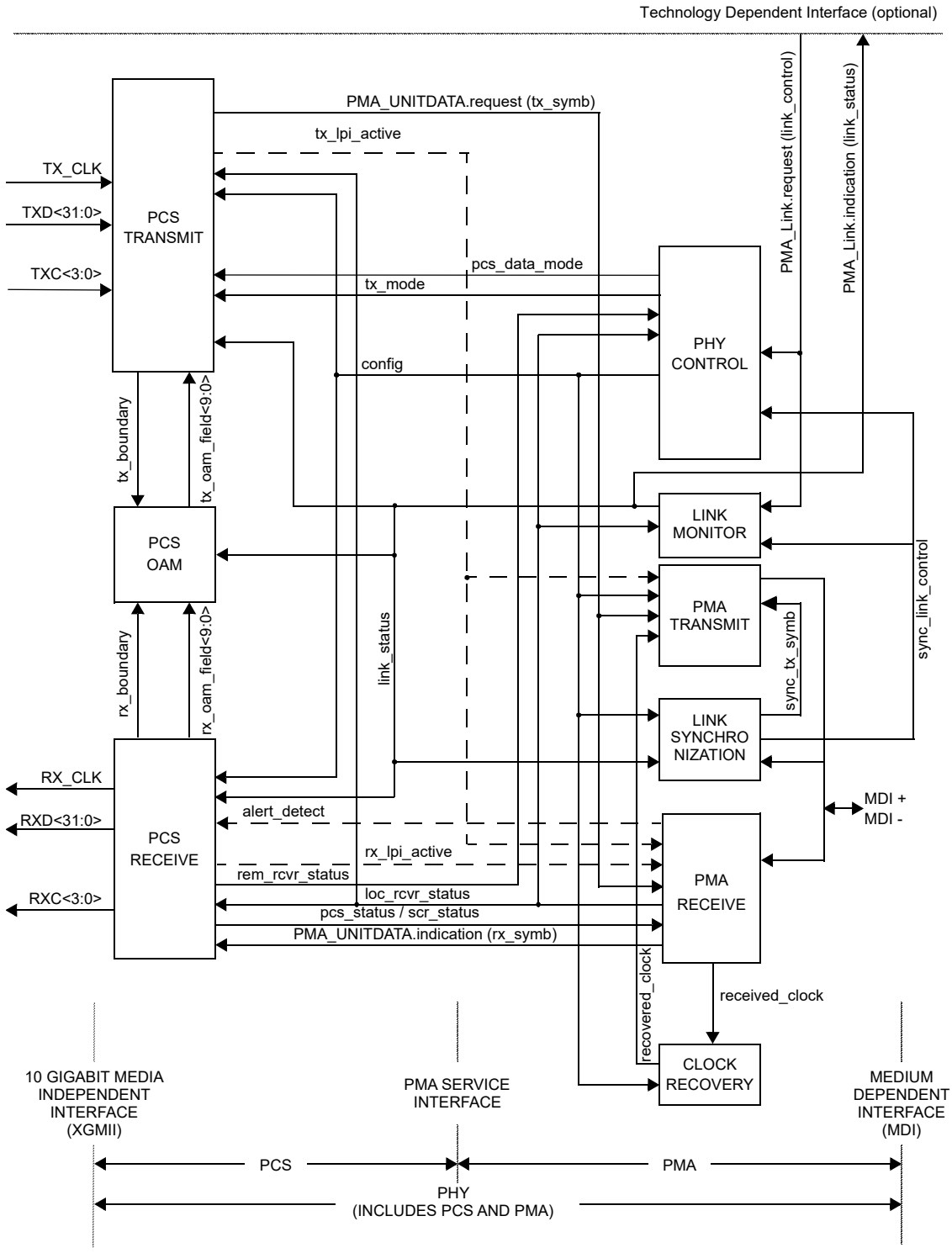

NOTE 1—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

NOTE 2—Signals and functions shown with dashed lines are optional.

Figure 149–2—Functional block diagram

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149.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto the single balanced pair of conductors via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions. The PMA provides full duplex communications at 5625 × *S* MBd. See Table 149–1 for the definition of *S*.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled following the completion of Auto-Negotiation or PHY Link Synchronization and provides the startup functions required for successful MultiGBASE-T1 operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link channel and communicates this status to other functional blocks. A failure of the receive channel causes the data mode operation to stop and Auto-Negotiation or Link Synchronization to restart.

PMA functions and state diagrams are specified in 149.4. The electrical parameters of the PMA, i.e., test modes and electrical specifications for the transmitter and receiver, are specified in 149.5.

149.1.3.3 EEE Capability

A MultiGBASE-T1 PHY may optionally support the EEE capability, as described in 78.3. The EEE capability is a mechanism by which MultiGBASE-T1 PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter the LPI mode of operation after completing training. Each direction of the full duplex link is able to enter and exit the LPI mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full duplex link is in a period of low utilization. The transition to or from LPI mode is not expected to cause any MAC frames to be lost or corrupted.

Support for the EEE capability is advertised in the Infofield (Octet 10 bit 6) during link startup. Transitions to and from the LPI transmit mode are controlled via XGMII signaling. Transitions to and from the LPI receive mode are controlled by the link partner using sleep and wake signaling.

When the PHY Health status received from the link partner indicates that LPI is insufficient to maintain PHY SNR, the PHY may temporarily exit LPI mode and send idles.

The PCS 64B/65B Transmit state diagram in Figure 149–16 and Figure 149–17 includes additional states for EEE. The PCS 64B/65B Receive state diagram in Figure 149–18 and Figure 149–19 includes additional states for EEE. The EEE transmit state diagram is contained in the PCS Transmit function and is specified in Figure 149–20.

149.1.3.4 Link Synchronization

The Link Synchronization function is used when Auto-Negotiation is disabled or not implemented to detect the presence of the link partner, time and control link failure, and act as the data source for the PHY control state diagram. Link Synchronization operates in a half-duplex fashion. Link Synchronization is defined in 149.4.2.6.

149.1.4 Signaling

MultiGBASE-T1 signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over the single balanced pair of conductors. The signaling scheme achieves a number of objectives including:

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a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM4 symbols in the transmit path.
c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions.
f) Block framing and other control signals.
g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
h) Ability to automatically detect and correct for incorrect polarity in the connection.
i) Optionally, ability to support refresh, quiet, and alert signaling during LPI operation.

The PHY may operate in three basic modes: the normal data mode, the training mode, or an optional LPI mode.

In normal mode, the PCS generates a continuous stream of PAM4 symbols that are transmitted via the PMA at one of four voltage levels. In training mode, the PCS is directed to generate only PAM2 symbols for transmission by the PMA. (See Figure 149–32.)

PHYs may also support the EEE capability as described in 149.1.3.3. Transitions to the LPI mode are supported after reaching normal mode.

149.1.5 Interfaces

All 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHY implementations are compatible at the MDI and at the XGMII, if implemented. Implementation of the XGMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not.

149.1.6 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5, along with the extensions described in 145.2.5.2. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

Default initializations, unless specified, are left to the implementer.

149.2 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 service primitives and interfaces

MultiGBASE-T1 transfers data and control information across the following four service interfaces:

a) 10 Gigabit Media Independent Interface (XGMII)
b) Technology Dependent Interface
c) PMA service interface
d) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46; the Technology Dependent Interface is specified in 98.4. The PMA service interface is defined in 149.2.2 and the MDI is defined in 149.8.

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149.2.1 Technology Dependent Interface

MultiGBASE-T1 uses the following service primitives to exchange status indications and control signals across the Technology Dependent Interface, required in PHYs that implement Auto-Negotiation, as specified in 98.4:

PMA_LINK.request(link_control)
PMA_LINK.indication(link_status)

149.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation to enable and disable operation of the PMA, as specified in 98.4.2.

149.2.1.1.1 Semantics of the primitive

PMA_LINK.request(link_control)

The link_control parameter can take on one of two values: DISABLE, or ENABLE.

DISABLE Used by the Auto-Negotiation function to disable the PHY.

ENABLE Used by the Auto-Negotiation function to enable the PHY.

149.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in 98.4.

149.2.1.1.3 Effect of receipt

This primitive affects the operation of the PMA Link Monitor function as defined in 149.4.2.5, the PMA PHY Control function as defined in 149.4.2.4, and the PMA Receive function defined in 149.4.2.3.

149.2.1.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 98.4.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation functions about the status of the underlying link.

149.2.1.2.1 Semantics of the primitive

PMA_LINK.indication(link_status)

The link_status parameter can take on one of two values: FAIL or OK.

FAIL No valid link established.

OK The Link Monitor function indicates that a valid MultiGBASE-T1 link is established. Reliable reception of signals transmitted from the remote PHY is possible.

149.2.1.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 149–33.

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149.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 98.4.1.

149.2.2 PMA service interface

MultiGBASE-T1 uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication(tx_mode)
PMA_CONFIG.indication(config)
PMA_UNITDATA.request(tx_symb)
PMA_UNITDATA.indication(rx_symb)
PMA_SCRSTATUS.request(scr_status)
PMA_PCSSTATUS.request(pcs_status)
PMA_RXSTATUS.indication(loc_rcvr_status)
PMA_REMRXSTATUS.request(rem_rcvr_status)
PMA_PCSDATAMODE.indication (pcs_data_mode)

The use of these primitives is illustrated in Figure 149–3. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 149–3.

EEE-capable PHYs additionally support the following service primitives:

PMA_PCS_RX_LPI_STATUS.request(rx_lpi_active)
PMA_PCS_TX_LPI_STATUS.request(tx_lpi_active)
PMA_ALERTDETECT.indication (alert_detect)

149.2.2.1 PMA_TXMODE.indication

The transmitter in a MultiGBASE-T1 link normally sends over the MDI symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

149.2.2.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following values of the form:

SEND_N	This value is continuously asserted during transmission of sequences of symbols representing an XGMII data stream in the data mode.
SEND_T	This value is continuously asserted in case transmission of sequences of symbols representing the training mode is to take place.
SEND_Z	This value is continuously asserted in case transmission of zeros is required.

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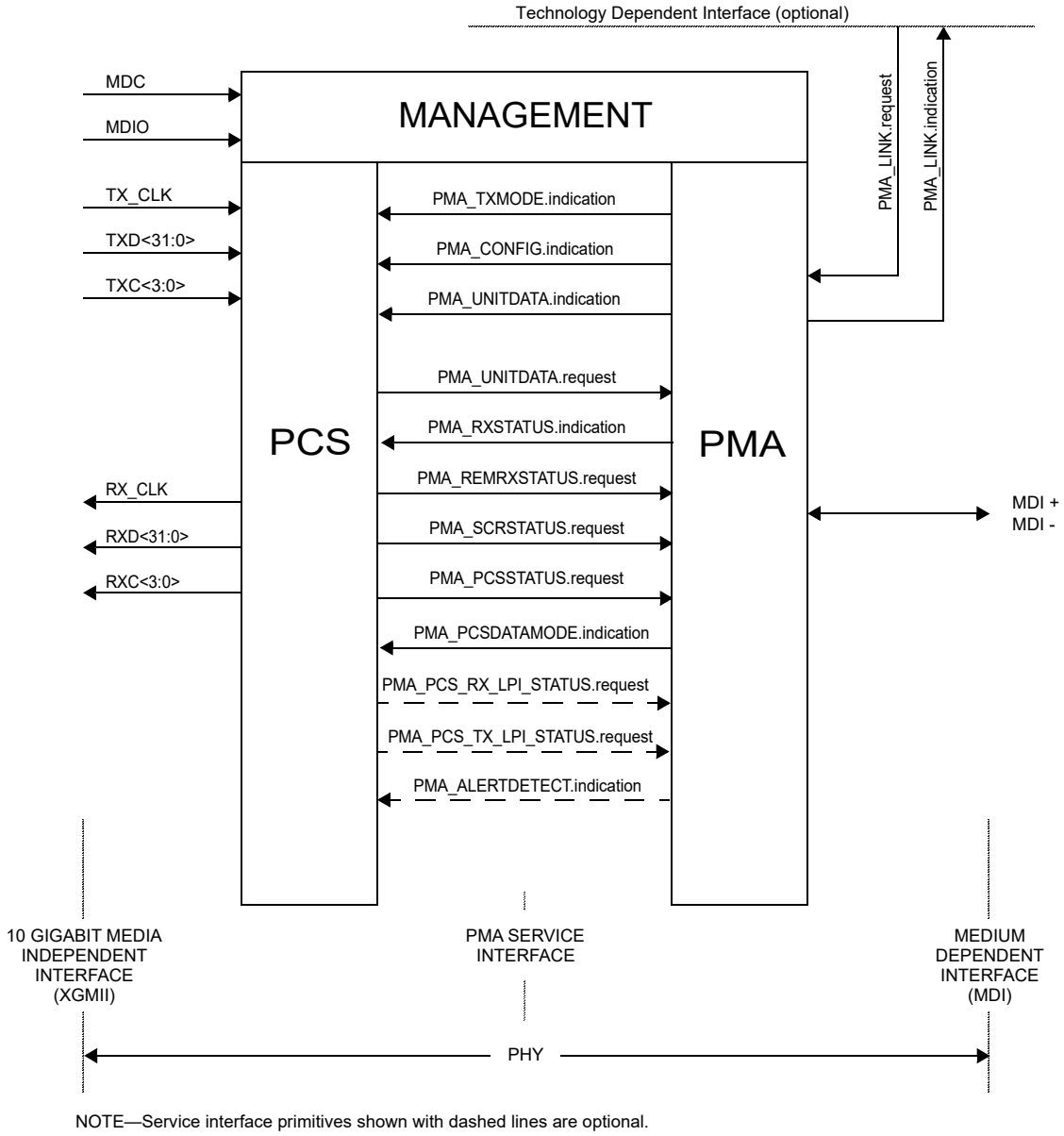

NOTE—Service interface primitives shown with dashed lines are optional.

Figure 149–3—2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 service interfaces

149.2.2.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

149.2.2.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 149.3.2.2.

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149.2.2.2 PMA_CONFIG.indication

Each PHY in a MultiGBASE-T1 link is capable of operating as a MASTER PHY and as a SLAVE PHY. If the Auto-Negotiation process is enabled, PMA_CONFIG MASTER-SLAVE configuration is determined during Auto-Negotiation (see Clause 98) and the result is provided to the PMA. If the Auto-Negotiation process is not implemented or not enabled, PMA_CONFIG MASTER-SLAVE configuration is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup.

149.2.2.2.1 Semantics of the primitive

PMA_CONFIG.indication(config)

PMA_CONFIG.indication specifies to the PCS and PMA Transmit via the parameter config whether the PHY operates as a MASTER PHY or as a SLAVE PHY. The parameter config can take on one of the following two values of the form:

MASTER	This value is continuously asserted when the PHY operates as a MASTER PHY.
SLAVE	This value is continuously asserted when the PHY operates as a SLAVE PHY.

149.2.2.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in configuration.

149.2.2.2.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter config.

149.2.2.3 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 149.3.2.2 to represent XGMII data and control streams or other sequences.

149.2.2.3.1 Semantics of the primitive

PMA_UNITDATA.request(tx_symb)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb the value of the symbols to be sent over the MDI. The tx_symb may take on one of the following values:

{–1, –1/3, +1/3, +1}	in normal operation.
0	when zeros are to be transmitted in the following two cases: 1) when PMA_TXMODE.indication is SEND_Z during PMA training, and 2) after data mode is reached, the transmit function is in the LPI transmit mode, and lpi_tx_mode is QUIET.

149.2.2.3.2 When generated

The PCS generates PMA_UNITDATA.request(tx_symb) synchronously with every transmit clock cycle.

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149.2.2.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols processed to conform to 149.5.2.

149.2.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb parameter from the PMA to the PCS.

149.2.2.4.1 Semantics of the primitive

PMA_UNITDATA.indication(rx_symb)

During reception the PMA_UNITDATA.indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the recovered clock.

149.2.2.4.2 When generated

The PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is 1406.25 MHz for 2.5GBASE-T1, 2812.5 MHz for 5GBASE-T1, and 5625 MHz for 10GBASE-T1; as governed by the recovered clock.

149.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

149.2.2.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the training mode descrambler has achieved synchronization.

149.2.2.5.1 Semantics of the primitive

PMA_SCRSTATUS.request(scr_status)

The scr_status parameter can take on one of two values of the form:

OK	The training mode descrambler has achieved synchronization.
NOT_OK	The training mode descrambler is not synchronized.

149.2.2.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

149.2.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 149.4.2.3 and 149.4.2.4.

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149.2.2.6 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in the data mode.

149.2.2.6.1 Semantics of the primitive

PMA_PCSSTATUS.request(pcs_status)

The pcs_status parameter can take on one of two values of the form:

OK	The PCS is operating reliably in the data mode.
NOT_OK	The PCS is not operating reliably in the data mode.

149.2.2.6.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

149.2.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 149.4.4.1.

149.2.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol stream.

149.2.2.7.1 Semantics of the primitive

PMA_RXSTATUS.indication(loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

149.2.2.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

149.2.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 149–33, 149.3.2.3, 149.4.2.4, and 149.4.5.

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149.2.2.8 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received in the loc_rcvr_status bit in the Infofield from the remote PHY. The rem_rcvr_status is set to NOT_OK if the PCS has not decoded a valid Infofield from the remote PHY.

149.2.2.8.1 Semantics of the primitive

PMA_REMRXSTATUS.request(rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

149.2.2.8.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages to indicate a change in rem_rcvr_status based on the PCS decoding the loc_rcvr_status bit in Infofield messages received from the remote PHY during training.

149.2.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 149–32.

149.2.2.9 PMA_PCSDATAMODE.indication

This primitive indicates whether or not the PCS state diagrams are able to transition from their initialization states. The pcs_data_mode variable is generated by the PMA PHY Control function. It is passed to the PCS Control function via the PMA_PCSDATAMODE.indication primitive.

149.2.2.9.1 Semantics of the primitive

PMA_PCSDATAMODE.indication(pcs_data_mode)

149.2.2.9.2 When generated

The PMA PHY Control function generates PMA_PCSDATAMODE.indication messages continuously.

149.2.2.9.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 149.3.2.2.

149.2.2.10 PMA_PCS_RX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS Receive function to indicate the status of the receive link at the local PHY. The parameter PMA_PCS_RX_LPI_STATUS.request conveys to the PCS Transmit and PMA Receive functions information regarding whether the receive function is in the LPI receive mode.

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149.2.2.10.1 Semantics of the primitive

PMA_PCS_RX_LPI_STATUS.request(rx_lpi_active)

The rx_lpi_active parameter can take on one of two values of the form:

TRUE	The receive function is in the LPI receive mode.
FALSE	The receive function is not in the LPI receive mode.

149.2.2.10.2 When generated

The PCS generates PMA_PCS_RX_LPI_STATUS.request messages to indicate a change in the rx_lpi_active variable as described in 149.3.2.3 and 149.3.7.2.2.

149.2.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in 149.3.7.3.

149.2.2.11 PMA_PCS_TX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS Transmit function to indicate the status of the transmit link at the local PHY. The parameter PMA_PCS_TX_LPI_STATUS.request conveys to the PCS Transmit and PMA Receive functions information regarding whether the transmit function is in the LPI transmit mode.

149.2.2.11.1 Semantics of the primitive

PMA_PCS_TX_LPI_STATUS.request(tx_lpi_active)

The tx_lpi_active parameter can take on one of two values of the form:

TRUE	The transmit function is in the LPI transmit mode.
FALSE	The transmit function is not in the LPI transmit mode.

149.2.2.11.2 When generated

The PCS generates PMA_PCS_TX_LPI_STATUS.request messages to indicate a change in the tx_lpi_active variable as described in 149.3.6 and 149.3.7.2.2.

149.2.2.11.3 Effect of receipt

The effect of receipt of this primitive is specified in 149.3.7.3.

149.2.2.12 PMA_ALERTDETECT.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY when rx_lpi_active is TRUE. The parameter alert_detect conveys to the PCS Receive function information regarding the detection of the LPI alert signal by the PMA Receive function. The criterion for setting the parameter alert_detect is left to the implementer.

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149.2.2.12.1 Semantics of the primitive

PMA_ALERTDETECT.indication (alert_detect)

The alert_detect parameter can take on one of two values of the form:

TRUE	The alert signal has been reliably detected at the local receiver.
FALSE	The alert signal at the local receiver has not been detected.

149.2.2.12.2 When generated

The PMA generates PMA_ALERTDETECT.indication messages to indicate a change in the alert_detect status.

149.2.2.12.3 Effect of receipt

The effect of receipt of this primitive is specified in 149.3.2.3, Figure 149–17.

149.3 Physical Coding Sublayer (PCS) functions

149.3.1 PCS service interface (XGMII)

The PCS service interface allows the MultiGBASE-T1 PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

149.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 149–4, shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 149–4.

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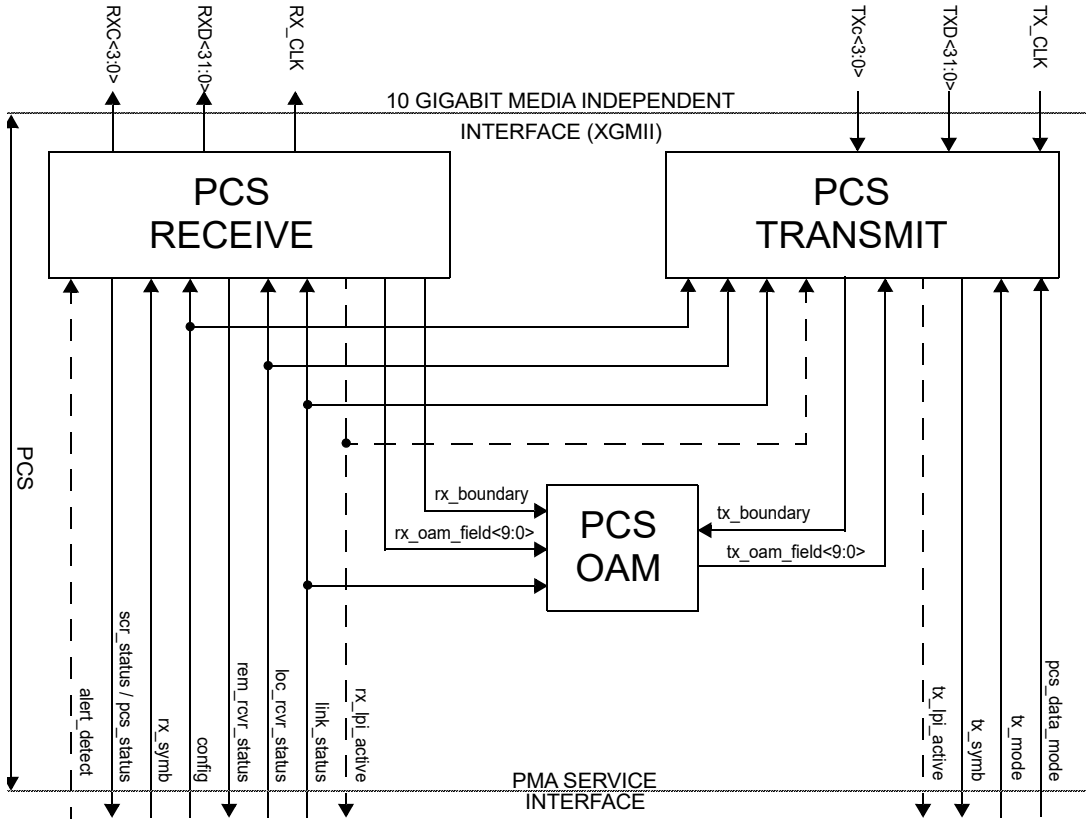

NOTE—rx_lpi_active and tx_lpi_active are only required for the EEE capability.

Figure 149–4—PCS reference diagram

149.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 149.3.7.2.2).
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset = TRUE while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

The control and management interface shall be restored to operation within 10 ms from the setting of bit 3.2322.15.

149.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 149–16 and Figure 149–17, and to the PCS Transmit bit ordering in Figure 149–6.

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Dashed rectangles in Figure 149–16 and Figure 149–17 are used to indicate states and state transitions in the transmit process state diagram that shall be supported by PHYs with the EEE capability. PHYs without the EEE capability do not support these states or transitions.

When communicating with the XGMII, the MultiGBASE-T1 PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

After mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process take L groups of 50 65B blocks and append a 10-bit OAM field to each group. This forms the input to an L-interleaved RS-FEC which adds L × 340 parity bits. The resulting L × 3600 bits are then scrambled. These bits are then mapped, two at a time, into a PAM4 symbol. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a PAM4 symbol that is transferred to the PMA via the PMA_UNITDATA.request primitive. The symbol period, *T*, is 1000 / (5.625 × *S)* ps. See Table 149–1 for the definition of *S*.

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate a sequence (T_n) defined in 149.3.5.1 to the PMA via the PMA_UNITDATA.request primitive. These code-groups are used for training mode and only transmit the values {–1, +1}.

During training mode an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes requests for remote transmitter settings. (See 149.4.2.4.)

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the normal mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control. During transmission, the 50 blocks of 65B encoded bits are appended with a 10-bit OAM field to form the RS-FEC input frame. During data encoding, PCS Transmit utilizes L-interleaved (L = 1, 2, or 4) Reed-Solomon encoders to generate and append 340 parity check bits to form 3600-bit (360,326) RS-FEC frames that are interleaved into an L-interleaved RS-FEC superframe.

Each RS-FEC input superframe consists of 3260 × L bits, or 326 × L Reed-Solomon message symbols. The interleaving function is integrated with the RS-FEC encoding, applying a round-robin interleaving scheme and distributing the 10-bit Reed-Solomon message symbols into L RS-FEC encoders. After encoding, the RS-FEC frames from each encoder are recombined into one single interleaved RS-FEC superframe, which consists of 360 × L symbols, or 3600 × L bits. The bits of the RS-FEC superframe are then scrambled by the PCS using an additive scrambler, encoded in PAM4 symbols, and transferred to the PMA.

L is called the interleaving depth, and the possible choices of L are 1, 2, and 4. The interleaver settings requested in each direction of transmission may be different, and the value of L used by the transmitter is determined by the link partner and signaled during the PAM2 training mode Infofield exchange.

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After reaching the normal mode of operation, EEE-capable PHYs may enter the LPI transmit mode under the control of the RS via the XGMII. The EEE Transmit state diagram is contained within the PCS Transmit function. The EEE capability is described in 149.3.2.2.22.

A block diagram of the PCS Transmit functions is shown in Figure 149–5.

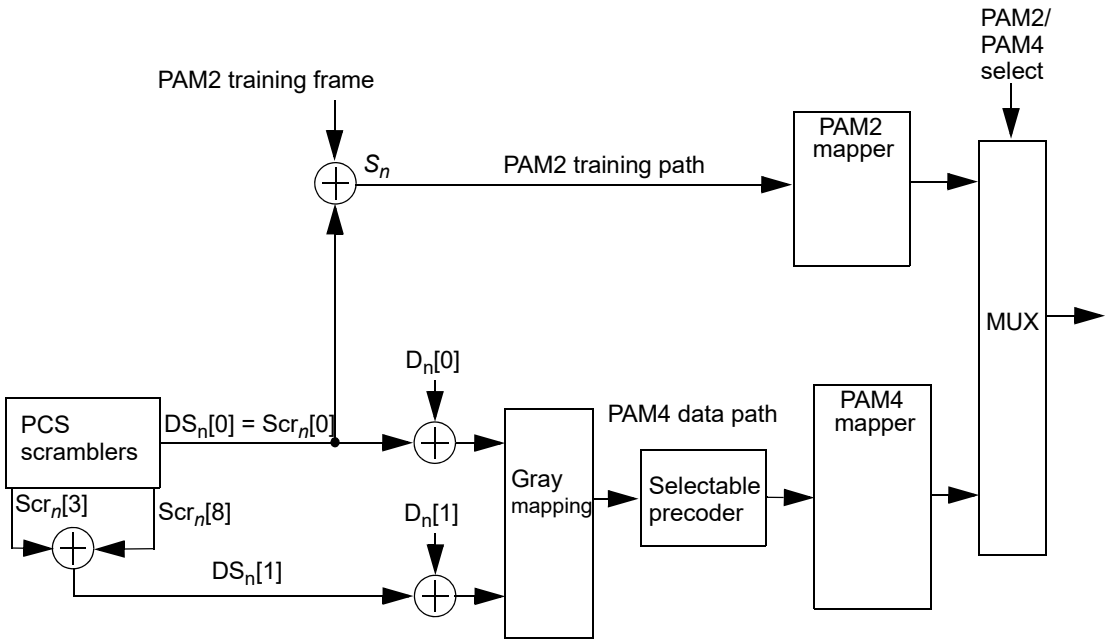

Figure 149–5—PCS Transmit function block diagram

149.3.2.2.1 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an RS-FEC frame, and vice versa, using a 65B RS-FEC coding scheme. The PAM2 PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. During the LPI mode, RS-FEC frame boundaries delimit sleep, wake, refresh, quiet, and alert cycles. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 149.3.2.2.2.

149.3.2.2.2 65B RS-FEC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 149–6 for transmit and Figure 149–7 for receive. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 149.3.2.2.4 for information on how blocks containing control characters are mapped.

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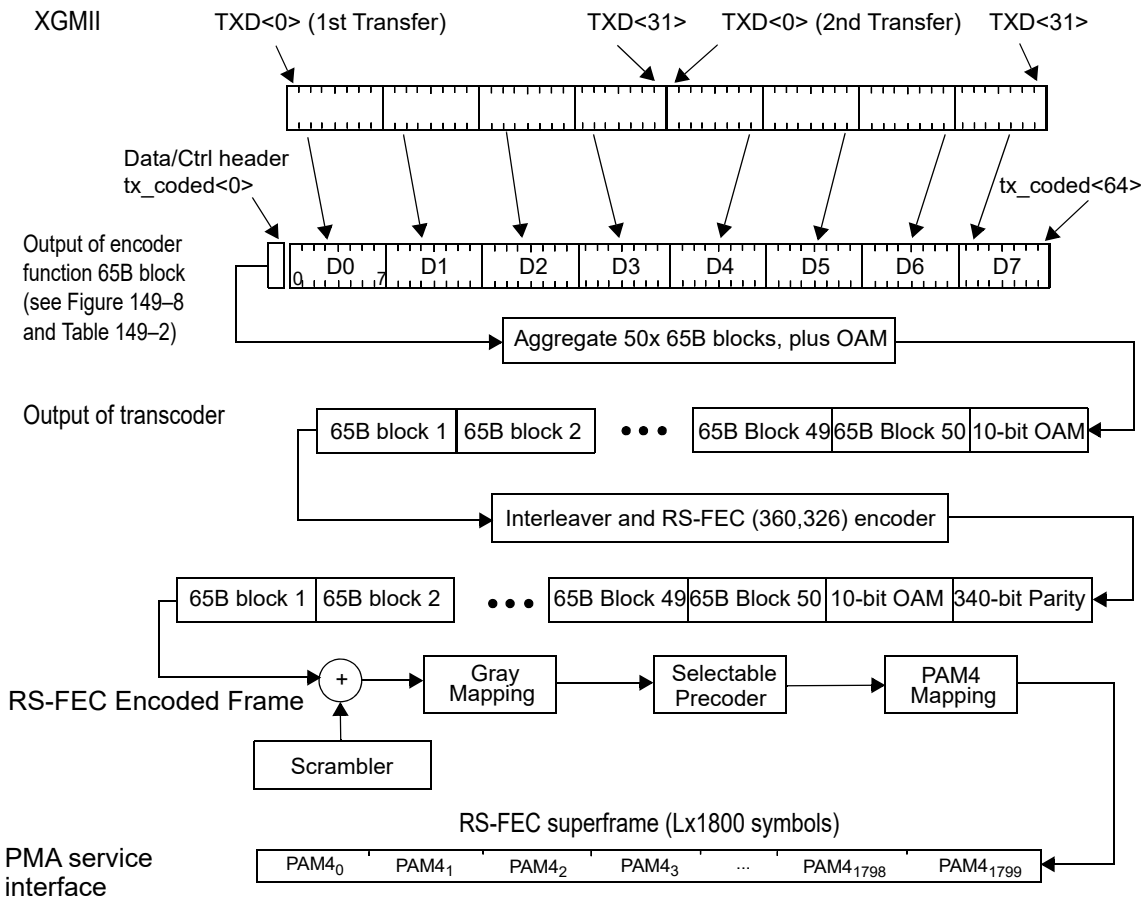

NOTE 1—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

NOTE 2—Figure shown for L = 1.

Figure 149–6—PCS Transmit bit ordering

149.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. Control characters other than /O/, /S/, and /T/ are labeled C_0 to C_7. The control character for ordered set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7.

For MultiGBASE-T1, two XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfer(s).

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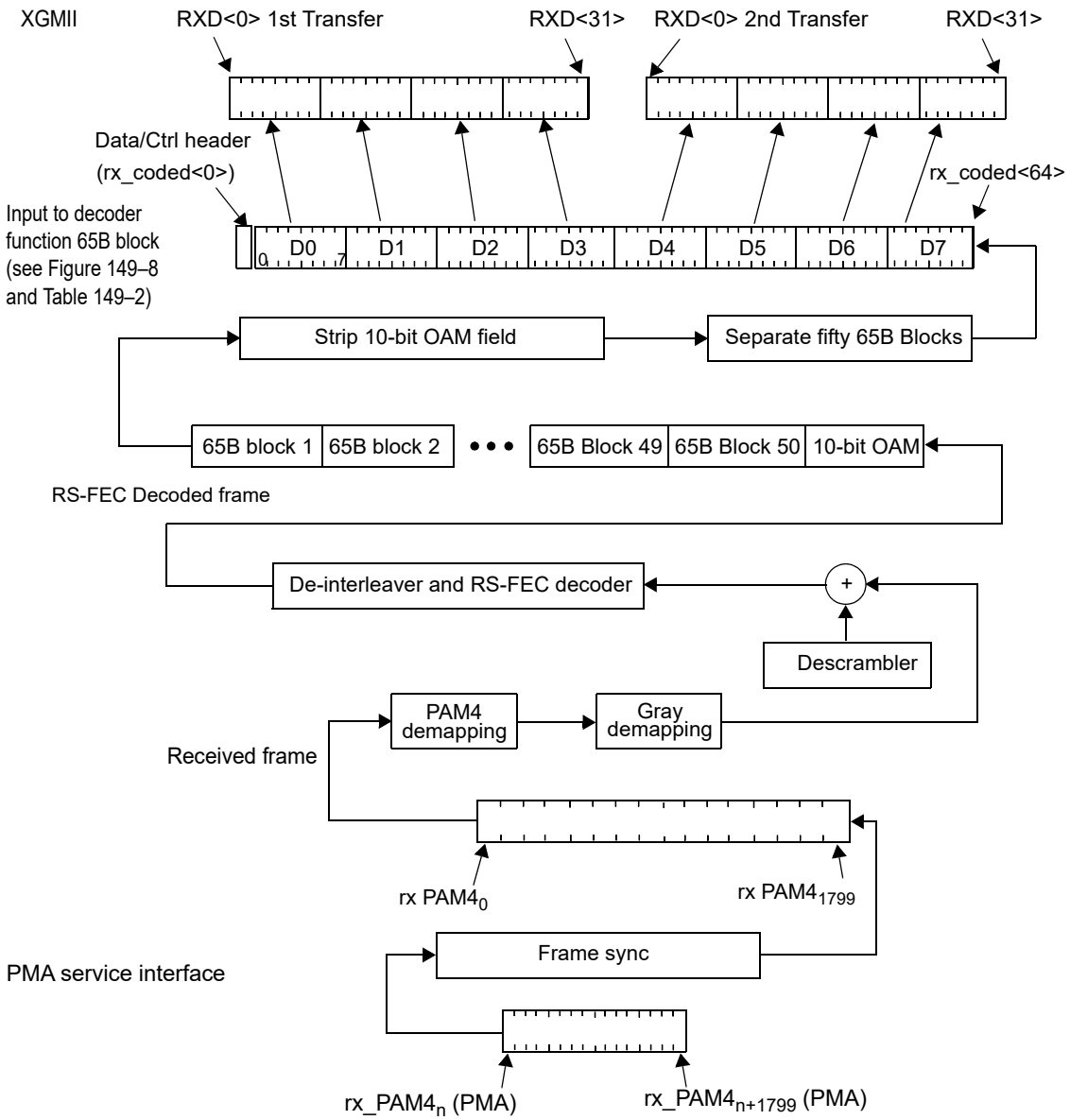

NOTE 1—This figure shows the mapping from a 64B/65B block a block containing eight data characters to the XGMII.

NOTE 2—Figure shown for L = 1.

Figure 149–7—PCS Receive bit ordering

Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled tx_coded<31:0> and rx_coded<31:0> where tx_coded<0> and rx_coded<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

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149.3.2.2.4 Block structure

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an eight-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that character is implied by the block type field. Other control characters are encoded in a seven-bit control code or a four-bit O Code. Each control block contains eight characters.

The format of the blocks for MultiGBASE-T1 is as shown in Figure 149–8. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the Input Data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt.

Input Data	data ctrl header	**Block Payload**							
Bit Position: / **Data Block Format:**	0	1							64
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 149–8—64B/65B block formats for MultiGBASE-T1

Bits and field positions are shown with the least significant bit on the left. Hexadecimal numbers are shown prepended with ‘0x’, and with the least significant digit on the right. For example the block type field 0x1E

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is sent as 01111000 representing bits 1 through 8 of the 65-bit block. The least significant bit for each field is placed in the lowest numbered position of the field.

All unused values of block type field[245] are reserved.

149.3.2.2.5 Control codes

The same set of control characters are supported by the XGMII and the 2.5G/5G/10GBASE-T1 PCS. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an eight-bit value). The 2.5G/5G/10GBASE-T1 PCS encodes the start and terminate control characters implicitly by the block type field. The 2.5G/5G/10GBASE-T1 PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The 2.5G/5G/10GBASE-T1 PCS encodes each of the other control characters into a seven-bit C code.

The control characters and their mappings to 2.5G/5G/10GBASE-T1 control codes and XGMII control codes are specified in Table 149–2. All XGMII control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

149.3.2.2.6 Ordered sets

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and local fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the XGMII. 2.5, 5, and 10 Gigabit Ethernet use one kind of ordered set: the sequence ordered set (see 46.3.4). The sequence ordered set control character is denoted /Q/. An additional ordered set, the signal ordered set, has been reserved and it begins with another control code. The four-bit O field encodes the control code. See Table 149–2 for the mappings.

149.3.2.2.7 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

149.3.2.2.8 LPI (/LI/)

Low Power Idle (LPI) control characters (/LI/) on the XGMII indicate that the LPI client is requesting operation in the LPI transmit mode. A continuous stream of LPI control characters (/LI/) is used to maintain a link in the LPI transmit mode. Idle control characters (/I/) are used to transition from the LPI transmit mode to the normal mode. PHYs that support EEE respond to the LPI XGMII control characters using the procedure outlined in 149.1.3.3. LPI characters may be added or deleted by the PCS to adapt between clock rates. /LI/ insertion and deletion shall occur in groups of four. /LI/s may be added following Low Power Idle characters. They shall not be added while data is being received.

If EEE is not supported, then /LI/ is not a valid control character.

149.3.2.2.9 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<7:0> and RXD<7:0>). Receipt of an /S/ on any other octet of TXD indicates an error.

[245]The block type field values have been chosen to have a four-bit Hamming distance between them. The only unused value that maintains this Hamming distance is 0x00.

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Table 149–2—Control codes for MultiGBASE-T1

Control character	Notation	XGMII control code	2.5G/5G/10G BASE-T1 control code	2.5G/5G/10G BASE-T1 O code
idle	/I/	0x07	0x00	
LPI	/LI/	0x06	0x06	
start	/S/	0xFB	Encoded by block type field	
terminate	/T/	0xFD	Encoded by block type field	
error	/E/	0xFE	0x1E	
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0
reserved0		0x1C	0x2D	reserved0
reserved1		0x3C	0x33	reserved1
reserved2		0x7C	0x4B	reserved2
reserved3		0xBC	0x55	reserved3
reserved4		0xDC	0x66	reserved4
reserved5		0xF7	0x78	reserved5
Signal ordered set[1]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF

[1]Reserved for INCITS T11 Fibre Channel use.

Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

149.3.2.2.10 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and within any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

149.3.2.2.11 Ordered set (/O/)

The ordered set control characters (/O/) indicate the start of an ordered set. There are two kinds of ordered sets: the sequence ordered set and the signal ordered set, which is reserved. When it is necessary to designate the control character for the sequence ordered set specifically, /Q/ is used. /O/ is only valid on the first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered set.

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Sequence ordered sets may be deleted by the PCS to adapt between clock rates. Such deletion shall only occur when two consecutive sequence ordered sets have been received and shall delete only one of the two. Only Idles may be inserted for clock compensation. Signal ordered sets are not deleted for clock compensation.

149.3.2.2.12 Error (/E/)

The /E/ is sent whenever an /E/ is received. The /E/ allows physical sublayers such as the PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 149.3.7.2.4 for further information.

149.3.2.2.13 Transmit process

The transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. 100 XGMII data transfers are encoded into an RS-FEC frame. It takes 1800 PMA_UNITDATA transfers to send an RS-FEC frame of data. Therefore, for MultiGBASE-T1, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 1:18, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 149–16 and Figure 149–17). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the transcoder and scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

149.3.2.2.14 RS-FEC framing and RS-FEC encoder

The resulting RS-FEC frame of 50 65B blocks, followed by the 10-bit OAM field and 340 parity bits is 3600 bits. See Figure 149–6 and 149.3.2.2.17 for details on PCS bit ordering and RS-FEC encoding.

The RS-FEC encoding takes the 3260-bit vector, consisting of tx_group50x65B, and the 10-bit OAM_field, and shall generate the 34 10-bit parity symbols (340 bits total).

149.3.2.2.15 RS-FEC superframe and round-robin interleaving

The interleaver depth L of the transmitter shall be set to the InterleaverDepth requested by the link partner during Infofield exchange, as specified in 149.4.2.4.5.

When the selected interleaving depth L = 1, there is no interleaving, and the RS-FEC superframe is the same as the RS-FEC frame.

When the selected interleaving depth L > 1, the round-robin interleaving scheme as shown in Figure 149–9 shall be applied.

2.5GBASE-T1 only supports L = 1.

5GBASE-T1 supports L = 1 and L = 2.

10GBASE-T1 supports L = 1, L = 2, and L = 4.

The PCS Transmit shall aggregate L RS-FEC input frames into an interleaved RS-FEC input superframe. There are 3260 × L bits, or 326 × L Reed-Solomon message symbols in total in the input superframe. The corresponding message symbols are $m_{326 \times L-1}$, $m_{326 \times L-2}$,…,m_1, m_0. These message symbols are

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distributed to L RS-FEC encoders. When L > 1, each RS-FEC encoder receives one out of every L message symbols from the superframe; otherwise, the RS-FEC encoder operates exactly the same as specified in 149.3.2.2.17.

149.3.2.2.16 RS-FEC recombine

The L encoded RS-FEC frames are recombined into an interleaved RS-FEC superframe. The output symbols are as follows:

$m_{326 \times L-1}, m_{326 \times L-2}, \ldots, m_1, m_0, p_{1,33}, \ldots, p_{L,33}, \ldots, p_{1,0}, \ldots, p_{L,0}$, where $p_{i,r}$ is the rth parity symbol of the ith encoder.

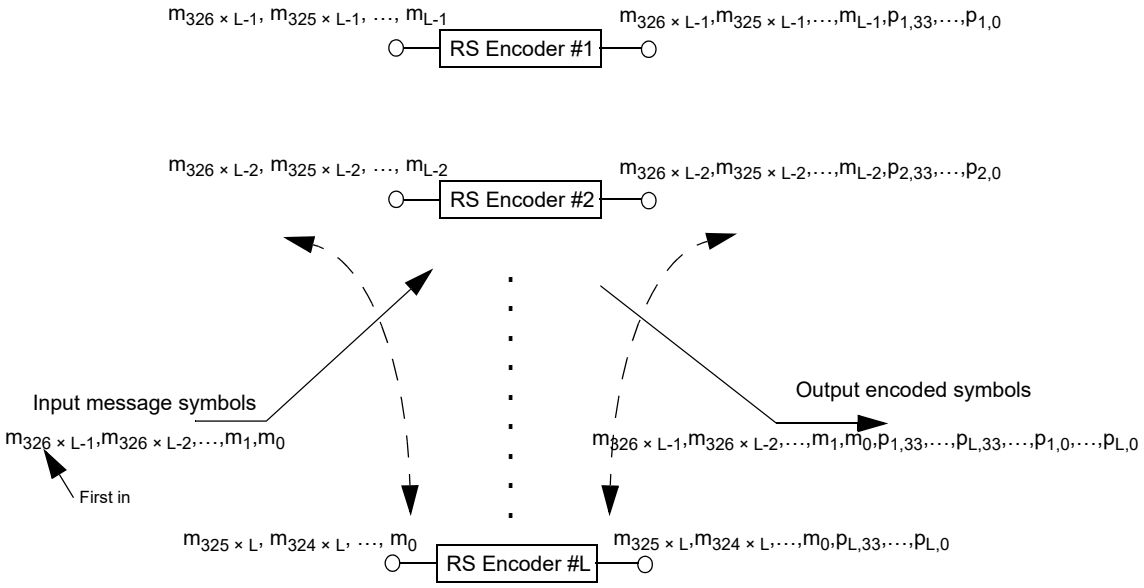

Figure 149–9—Interleaving block diagram with interleaving depth L

149.3.2.2.17 Reed-Solomon encoder

The group of 3260 bits are encoded using a Reed-Solomon encoder operating over the Galois Field GF(2^{10}) where the symbol size is 10 bits. The encoder processes 326 ten-bit RS-FEC message symbols to generate 34 ten-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 360 ten-bit RS-FEC symbols. For the purposes of this clause, the particular Reed-Solomon code is denoted as RS-FEC(360,326).

The code is based on the generating polynomial given by Equation (149–1).

$$g(x) = \prod_{j=0}^{33}(x - \alpha^j) = g_{34}x^{34} + g_{33}x^{33} + \ldots + g_4x^4 + g_3x^3 + g_2x^2 + g_1x + g_0 \quad (149\text{–}1)$$

In Equation (149–1), α, is a primitive element of the finite field defined by the primitive polynomial $0x409 = x^{10} + x^3 + 1$.

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Equation (149–2) defines the message polynomial $m(x)$ whose coefficients are the message symbols m_{325} to $m_{0.}$

$$m(x) = m_{325}x^{359} + m_{324}x^{358} + \ldots + m_1x^{35} + m_0x^{34} \quad (149–2)$$

Each message symbol m_i is the bit vector ($m_{i,9}$, $m_{i,8}$, ... $m_{i,1}$,$m_{i,0}$), which is identified with the element of the finite field. $m_{i,0}$ is the first bit transmitted. The message symbols are composed of the bits in tx_RSmessage<3259:0> where
$m_{i,j}$ = tx_RSmessage <(325 – i) × 10 + j>, for i = 0 to 325, and j = 0 to 9.

tx_RSmessage<3259:0> prior to RS-FEC (360,326) encoder is formed as follows:

tx_RSmessage<3249:0> = tx_group50x65B<3249:0>.
tx_RSmessage<3259:3250> = OAM_field<9:0>.

The first symbol input to the encoder is m_{325}.

Equation (149–3) defines the parity polynomial $p(x)$ whose coefficients are the parity symbols p_{33} to $p_{0.}$

$$p(x) = p_{33}x^{33} + p_{32}x^{32} + \ldots + p_2x^2 + p_1x + p_0 \quad (149–3)$$

Each parity symbol p_i is the bit vector ($p_{i,9}$, $p_{i,8}$, ... $p_{i,1}$,$p_{i,0}$), which is identified with the element of the finite field. $p_{i,0}$ is the first bit transmitted.

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This can be computed using the shift register implementation illustrated in Figure 149–10. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0, is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x, $c_{359} = m_{325}$ is transmitted first and the coefficient of the lowest power of x, $c_0 = p_0$ is transmitted last. The first bit transmitted from each symbol is bit 0.

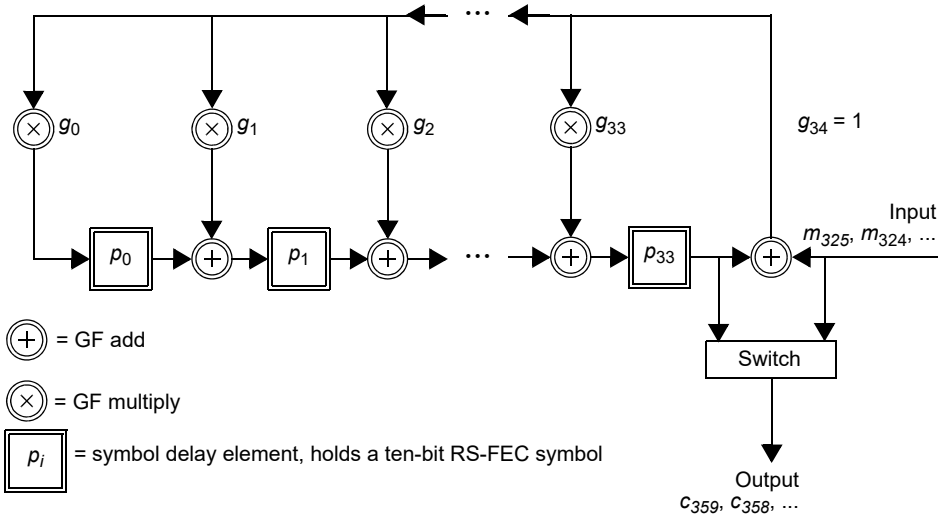

Figure 149–10—Reed-Solomon encoder functional model

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The coefficients of the generator polynomial for the code are presented in Table 149–3.

Table 149–3—Coefficients of the generator polynomial g_i (decimal)

i	RS-FEC(360, 326)	*i*	RS-FEC(360, 326)
0	315	18	615
1	269	19	952
2	594	20	672
3	756	21	636
4	732	22	765
5	709	23	929
6	198	24	173
7	560	25	242
8	444	26	197
9	323	27	886
10	546	28	902
11	161	29	736
12	930	30	168
13	914	31	248
14	412	32	800
15	68	33	951
16	150	34	1
17	878	—	—

149.3.2.2.18 PCS scrambler

The bits of the interleaved RS-FEC superframe are grouped into pairs, and each pair of bits, $D_n[0]$ and $D_n[1]$, where n is an index indicating the symbol number, is scrambled using an additive scrambler. For each pair of interleaved bits, two scrambler bits are generated from the side-stream scrambler. The first (LSB) bit is $DS_n[0]$ equal to $Scr_n[0]$ defined in 149.3.4. The second (MSB) bit is $DS_n[1]$ equal to $Scr_n[3] \oplus Scr_n[8]$.

$DS_n[0]$ and $DS_n[1]$ are applied as additive scrambler sequences to incoming data bits $D_n[0]$ (LSB) and $D_n[1]$ (MSB) to generate two scrambled data bits $\{A_n, B_n\}$ as shown in Equation (149–4).

$$A_n = DS_n[0] \oplus D_n[0]$$
$$B_n = DS_n[1] \oplus D_n[1] \quad (149–4)$$

149.3.2.2.19 Gray mapping for PAM4 encoding

For output symbols, the PCS transmit process shall map consecutive pairs of bits, $\{A_n, B_n\}$, where A_n is the bit arriving first, and n is an index indicating the symbol number, to Gray-coded symbols $G(n)$ with one of

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four levels as follows:

{0, 0} maps to 0,
{0, 1} maps to 1,
{1, 1} maps to 2, and
{1, 0} maps to 3.

For input symbols, the PCS receive process shall map Gray-coded PAM4 symbols G(n), with one of four levels, to pairs of bits, {A_n, B_n}, where A_n is considered to be the first bit as follows:

0 maps to {0, 0},
1 maps to {0, 1},
2 maps to {1, 1}, and
3 maps to {1, 0}.

149.3.2.2.20 Selectable precoder

The PCS transmit process shall precode the Gray-coded symbols as specified in this subclause.

In normal operation the value of precoder_type (see 45.2.1.246.3) shall be set to the value of PrecodeSel received from the link partner in the Infofield messages (see 149.4.2.4.5):

0 0: No precoder,
0 1: Precoder for 1 – D channel,
1 0: Precoder for 1 + D channel, and
1 1: Precoder for 1 – D^2 channel.

For each Gray-coded symbol G(n), a precoded symbol P(n) shall be determined by the following algorithm, where n is an index indicating the symbol number:

P(n) = G(n), when precoder_type = No precoder,
P(n) = (G(n) + P(n–1)) mod 4, when precoder_type = Precoder for 1 – D channel,
P(n) = (G(n) – P(n–1)) mod 4, when precoder_type = Precoder for 1 + D channel, and
P(n) = (G(n) + P(n–2)) mod 4, when precoder_type = Precoder for 1 – D^2 channel.

In normal data mode, the precoder should be initialized to the zero state when entering TX_SWITCH state of the startup sequence. In EEE mode, the precoder should be initialized to the zero state when transitioning to PAM4 encoding. When the precoder is not initialized to the zero state as described, there may be a short period of errors when entering the associated state.

149.3.2.2.21 PAM4 encoding

The PCS transmit process shall encode each precoder output symbol to one of four PAM4 levels as specified in this subclause.

The PAM4 encoded symbols are denoted M(n), where:

n is an index indicating the symbol number.

Each consecutive precoder output symbol, P(n), is mapped to one of four PAM4 levels and assigned to the PAM4 encoder output M(n).

Mapping from the precoder output symbol P(n) to a PAM4 encoded symbol M(n) is as follows:

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0 maps to –1,
1 maps to –1/3,
2 maps to +1/3, and
3 maps to +1.

149.3.2.2.22 EEE capability

The optional 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 EEE capability allows compliant PHYs to transition to an LPI mode of operation when link utilization is low in either direction of transmission.

PHYs that support EEE shall conform to the EEE transmit state diagram, shown in Figure 149–20, within the PCS.

In the transmit direction, the transition to the LPI transmit mode begins when the PCS Transmit function detects an LPI control character in the last 64B/65B block of a Reed-Solomon frame. Following this event, the PMA transmits the sleep signal to indicate to the link partner that it is transitioning to the LPI transmit mode. The sleep signal is composed of eight Reed-Solomon frames that contain only LP_IDLE 64B/65B blocks. Once initiated, the complete sleep signal consisting of eight RS-FEC frames of LP_IDLE shall be transmitted.

Following the transmission of the sleep signal, quiet-refresh signaling begins, as described in 149.3.6.

After the sleep signal is transmitted, LPI control characters shall be input to the PCS scrambler continuously until the PCS Transmit function exits the LPI transmit mode.

While the PMA asserts SEND_N, the lpi_tx_mode variable shall control the transmit signal through the PMA_UNITDATA.request primitive described as follows:

> When the PHY is not in the PCS_DATA state, the lpi_tx_mode variable is ignored.
>
> When the lpi_tx_mode variable takes the value NORMAL and the PMA asserts SEND_N, the PCS passes coded data to the PMA via the PMA_UNITDATA.request primitive as described in 149.3.2.2.
>
> When the lpi_tx_mode variable takes the value QUIET and the PMA asserts SEND_N, the PCS passes zeros to the PMA through the PMA_UNITDATA.request primitive.
>
> When the lpi_tx_mode variable takes the value REFRESH and the PMA asserts SEND_N, the PCS passes the PMA training signal to the PMA, to allow both the local and remote PHY to refresh adaptive filters and timing loops.
>
> When the lpi_tx_mode variable takes the value ALERT, the PMA transmits the link synchronization sequence onto the MDI as provided by the link synchronization block via sync_tx_symb.

The quiet-refresh cycle is repeated until codewords other than LP_IDLE are detected at the XGMII. These codewords indicate that the local system is requesting a transition back to the normal operational mode. Following this event, the PMA_UNITDATA.request parameter tx_symb_vector is set to the value ALERT.

After transmitting the alert signal, the PCS completes the transition from LPI mode to normal mode by sending a wake signal containing lpi_wake_time RS-FEC frames composed of IDLE 64B/65B blocks.

lpi_wake_time is a fixed parameter that is defined in Table 149–4. See Table 149–1 for the definition of *S*.

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Table 149–4—LPI wake time

lpi_wake_time	*lpi_tx_wake_time when wake starts before sleep signal is complete*		*lpi_tx_wake_time when wake starts after sleep signal is complete*	
(frames)	**(frames)**	**(μs)**	**(frames)**	**(μs)**
8	28	8.96/*S*	20	6.4/*S*

149.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 149–18 and Figure 149–19, and the PCS Receive bit ordering in Figure 149–7 including compliance with the associated state variables as specified in 149.3.7.2.2.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received PAM4 symbols are demapped and descrambling is performed.

Following descrambling, the L-interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. The RS-FEC decoded frame is then separated into a 10-bit OAM field and 50 64B/65B blocks. This process generates the 64B/65B block vector rx_coded<64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 149–18 and Figure 149–19). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primitive to OK.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If 40 consecutive RS-FEC frame errors are detected, the block_lock flag is de-asserted. The block_lock flag is re-asserted upon detection of a valid RS-FEC frame. When block_lock is asserted and hi_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication(loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training frame includes an alignment bit every 450 PAM2 symbols, which is aligned with the PCS partial PHY frame boundary, as well as an Infofield, which is inserted in the 16th PCS partial PHY frame. When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.

PHYs with the EEE capability support transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE and subject to the timing requirements of 46.1.7. Transitions to and

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from the LPI mode are allowed to occur independently in the transmit and receive functions. The PCS Receive function is responsible for detecting transitions to and from the LPI receive mode and indicating these transitions using signals defined in 149.2.2.

The link partner signals a transition to the LPI mode of operation by transmitting eight RS-FEC frames composed entirely of 64B/65B blocks of /LI/. When blocks of /LI/ are detected at the output of the 64B/65B decoder, rx_lpi_active is asserted by the PCS Receive function and the /LI/ character is continuously asserted at the receive XGMII. These frames may be preceded by a frame composed partially of /LI/ characters. After these frames, the link partner begins transmitting zeros, and it is recommended that the receiver power down receive circuits to reduce power consumption. The receive function uses RS-FEC frame counters to maintain synchronization with the remote PHY and receives periodic refresh signals that are used to update coefficients, so that the integrity of adaptive filters and timing loops in the PMA is maintained. LPI signaling is defined in 149.3.6. The quiet-refresh cycle continues until the PMA Receive function asserts alert_detect to indicate that the alert (link synchronization) sequence has been reliably detected. After the alert sequence, the link partner transmits repeated /I/ characters, representing a wake signal. The PHY receive function sends /I/ to the XGMII for eight RS-Frame periods (wake duration) and then resumes normal operation.

149.3.2.3.1 Frame and block synchronization

When operating in the data mode, the receiving PCS shall form a PAM4 stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from rx_PAM4_0 to rx_PAM4_1799 (see Figure 149–7). It obtains block lock to the PHY frames during PAM2 training using synchronization bits provided in the training frames.

149.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<31:0> to the XGMII. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial per Equation (149–6) and the SLAVE PHY shall employ the receiver descrambler generator polynomial per Equation (149–5).

149.3.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

a) The block type field contains a reserved value.
b) Any control character contains a value not in Table 149–2.
c) Any O code contains a value not in Table 149–2.
d) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in 149.3.2.2.14. If the check fails the RS-FEC frame is invalid.

The R_BLOCK_TYPE of an invalid block is set to E.

149.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel, and remote receiver. When the transmit PCS is operating in test-pattern mode it shall transmit continuously as illustrated in Figure 149–6, with the input to the RS-FEC encoder set to zero and the initial condition of the scrambler set to any non-zero value. This has the same effect as setting the input to the scrambler to zero.

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When the receiver PCS is operating in test-pattern mode it shall receive continuously as illustrated in Figure 149–7. The output of the received descrambled values should be zero. Any nonzero values correspond to receiver bit errors. The output of the RS-FEC decoder should also be zero; however, there is the possibility that the RS-FEC decoder corrected some errors. This mode is further described as test mode 7 in 149.5.1.

149.3.4 Side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indication message assumes the value MASTER, PCS Transmit shall employ Equation (149–5) as transmitter side-stream scrambler generator polynomial.

$$g_M(x) = 1 + x^{13} + x^{33} \tag{149–5}$$

If the PMA_CONFIG.indication message assumes the value of SLAVE, PCS Transmit shall employ Equation (149–6) as transmitter side-stream scrambler generator polynomial.

$$g_S(x) = 1 + x^{20} + x^{33} \tag{149–6}$$

An implementation of MASTER and SLAVE PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 149–11. The bits stored in the shift register delay line at time *n* are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

This scrambler, once started during PMA training, shall continue to run uninterrupted during the transition from PAM2 to PAM4.

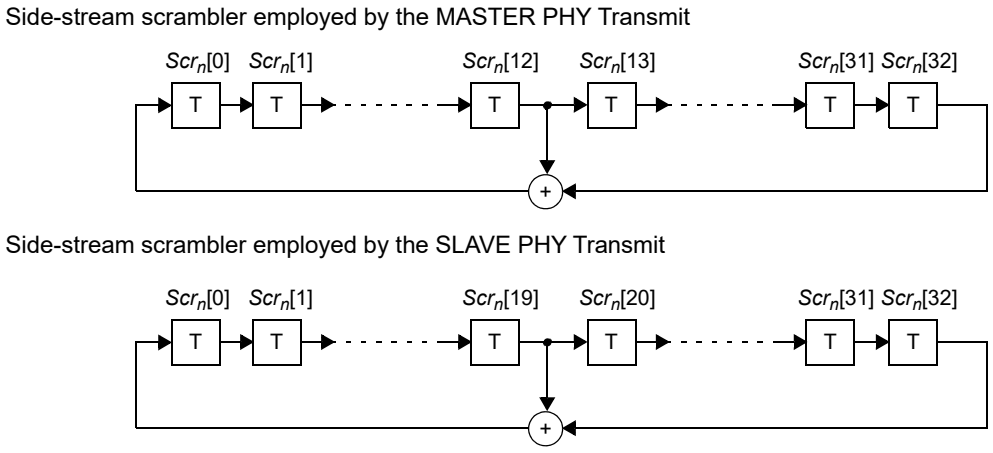

Figure 149–11—Realization of side-stream scramblers by linear feedback shift registers

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149.3.5 PMA training frame

During PMA training, the training frames are embedded with indicators to establish alignment to the RS-FEC superframe composed of 16 partial PHY frames that comprise the block. The last partial PHY frame is embedded with an information field used to exchange messages between link partners. The timing relationship among training frame, partial frame, RS-FEC frame, superframe, and partial PHY frame count (PFC24) are shown in Figure 149–12.

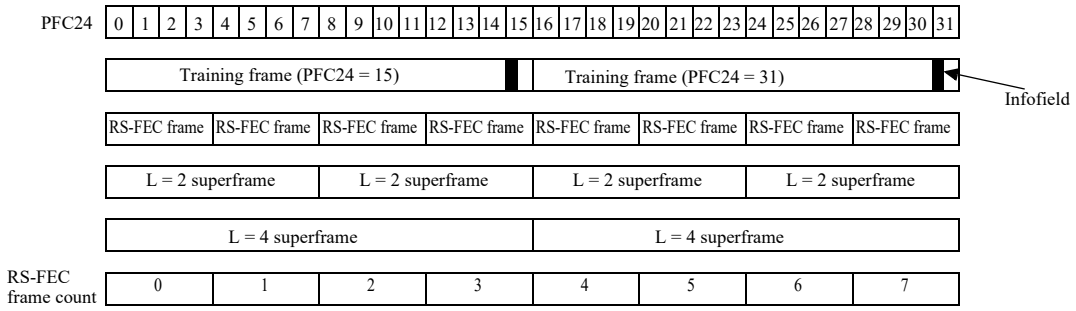

Figure 149–12—Timing relationship to PFC24

PMA training frame encoding is based on the generation, at time n, of the bit S_n. The first bit is inverted in the first 15 partial PHY frames of each RS-FEC block. The first 96 bits of the 16th partial PHY frame are XORed with the contents of the Infofield. Each partial PHY frame is 450 bits long, beginning at S_n where (n mod 450) = 0. See Equation (149–7).

$$S_n = \begin{cases} Scr_n[0] \oplus InfoField_{(n \bmod 450)} & 6750 \le (n \bmod 7200) \le 6845 \\ Scr_n[0] \oplus 1 & \text{else if } (n \bmod 450) = 0 \\ Scr_n[0] & \text{otherwise} \end{cases} \quad (149\text{–}7)$$

149.3.5.1 Generation of symbol T_n

The bit S_n is mapped to the transmit symbol T_n as follows: if $S_n = 0$ then $T_n = +1$, if $S_n = 1$ then $T_n = -1$.

149.3.5.2 PMA training mode descrambler polynomials

The PHY shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. For side-stream descrambling, the MASTER PHY employs the receiver descrambler generator polynomial per Equation (149–6) and the SLAVE PHY employs the receiver descrambler generator polynomial per Equation (149–5).

149.3.6 LPI signaling

PHYs with EEE capability have transmit and receive functions that can enter and leave the LPI mode independently. The PHY can transition to the LPI mode when the PHY has successfully completed training and pcs_data_mode is TRUE. The transmit function of the PHY initiates a transition to the LPI transmit mode by generating the sleep signal composed of eight RS-FEC frames composed entirely of LPI control characters, as described in 149.3.2.2.22. When the transmitter begins to send the sleep signal, it asserts tx_lpi_active and the transmit function enters the LPI transmit mode.

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Within the LPI mode, PHYs use a repeating quiet-refresh cycle (see Figure 149–13 and Figure 149–14). The LPI timing parameters are shown in Table 149–5. The first part of this cycle is known as the quiet period and lasts for a time lpi_quiet_time. The quiet period is defined in 149.3.6.2. The second part of this cycle is known as the refresh period and lasts for a time lpi_refresh_time. The refresh period is defined in 149.3.6.3. A cycle composed of one quiet period and one refresh period is known as an LPI cycle and lasts for a time lpi_qr_time.

The parameters lpi_offset, lpi_quiet_time, lpi_refresh_time, and lpi_qr_time are timing parameters that are integer multiples of the RS-FEC frame period. lpi_offset is a fixed value equal to lpi_qr_time / 2 + 4 (52 RS-FEC frame periods).

The end of LPI mode occurs at the transmission of the alert signal indicating the end of quiet-refresh cycle.

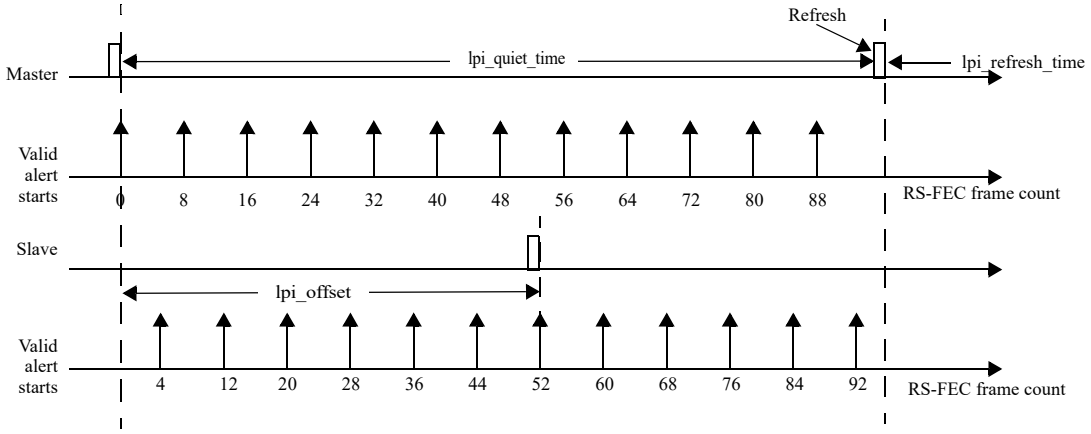

Figure 149–13—Timing periods for LPI signals when Slow Wake not active

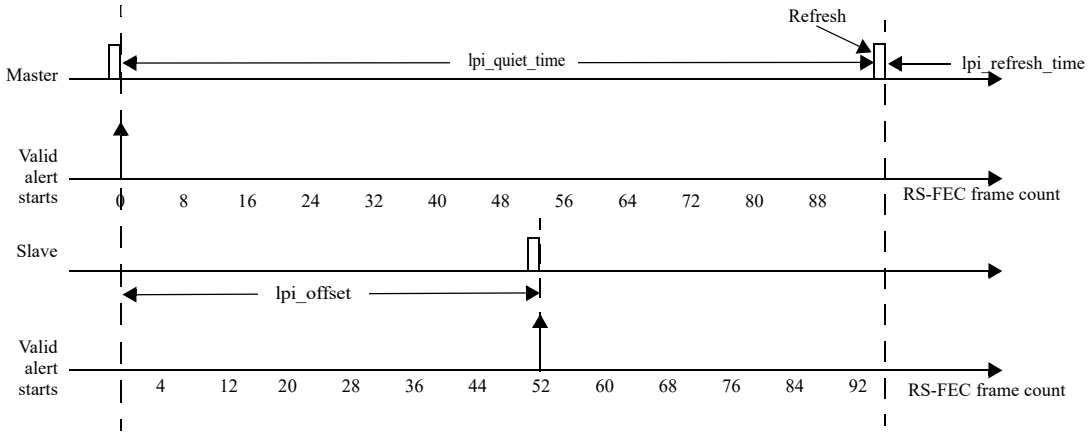

Figure 149–14—Timing periods for LPI signals when Slow Wake is active

149.3.6.1 LPI synchronization

EEE-capable PHYs shall synchronize refresh intervals during the LPI mode. A PHY in SLAVE mode is responsible for synchronizing its partial PHY frame count (PFC24) to the MASTER's PFC24 during PAM2 training. For the requirements on the SLAVE and the MASTER frame alignment, see 149.4.2.4.10.

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Table 149–5—LPI timing parameters

Parameter	Number of RS-FEC frame periods
alert_length	4
alert_period	8
lpi_offset	52
lpi_qr_time	96
lpi_quiet_time	95
lpi_refresh_time	1

Refresh signaling is derived by tracking the RS-FEC frame count as shown in Figure 149–13, where:

RS-FEC frame count = floor (PFC24 / 4) mod 96.

The start of the SLAVE quiet-refresh cycle is delayed from the MASTER by lpi_offset. The MASTER and SLAVE alert windows are offset from each other and the refresh periods are close to half a cycle offset.

Following the transition to PAM4, the PCS continues with the RS-FEC frame count and uses the count to generate refresh, alert, and wake control signals for the transmit functions.

Alert, a four RS-FEC frame long sequence (alert_length), shall start at the beginning of any eighth PHY frame boundary starting at the beginning of the frame following a refresh PHY frame. This offsets the MASTER and SLAVE alert start times by alert_period/2 and provides two benefits. The first benefit is that alert transmissions do not overlap with the device's own refresh. The second benefit is that the MASTER and SLAVE alert transmissions generally do not overlap, and only overlap at the limits of tolerances. The MASTER and SLAVE shall derive the tx_refresh_active and tx_alert_start_next signals from the transmitted PHY frames as shown in Table 149–6 and Table 149–7. When Slow Wake is active, alert can be transmitted in only a single QR cycle location.

Table 149–6—Synchronization logic derived from slave signal RS-FEC frame count

Slave-side variable	Condition (where u = RS-FEC frame count)	Slow Wake
tx_refresh_active = TRUE	lpi_offset – lpi_refresh_time ≤mod(u, lpi_qr_time) < lpi_offset	0 or 1
tx_alert_start_next = TRUE	mod(u, alert_period) = alert_period/2 –1	0
tx_alert_start_next = TRUE	mod(u, lpi_qr_time) = lpi_qr_time/2 + alert_period/2 –1	1

149.3.6.2 Quiet period signaling

During the quiet period the PCS transmitter shall pass zeros to the PMA via the PMA_UNITDATA.request primitive.

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Table 149–7—Synchronization logic derived from master signal RS-FEC frame count

Master-side variable	Condition (where v = RS-FEC frame count)	Slow Wake
tx_refresh_active = TRUE	mod(v, lpi_qr_time) ≥ lpi_quiet_time	0 or 1
tx_alert_start_next = TRUE	mod(v, alert_period) = alert_period –1	0
tx_alert_start_next = TRUE	mod(v, lpi_qr_time) = lpi_qr_time –1	1

149.3.6.3 Refresh period signaling

During the LPI mode the MultiGBASE-T1 PHY uses staggered, out-of-phase refresh signaling. Two-level PAM refresh symbols are generated from the T_n mapping defined in 149.3.5.1 of S_n defined in 149.3.5, with the exception that the Infofield consists of zeros. The 10-bit OAM symbol to be transmitted is XORed with the last 10 bits of the PAM2 refresh transmission.

149.3.7 Detailed functions and state diagrams

149.3.7.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

149.3.7.2 State diagram parameters

149.3.7.2.1 Constants

EBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in 46.3.4.

LBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing two Local Fault ordered sets.

LPBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII containing /LI/ in all the eight character locations.

LPBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing /LI/ in all the eight character locations.

IBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII containing /I/ in all the eight character locations.

IBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing /I/ in all the eight character locations.

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RFER_CNT_LIMIT
TYPE: Integer
VALUE: 16
Number of Reed-Solomon frames with uncorrectable errors.

RFRX_CNT_LIMIT
TYPE: Integer
VALUE: 88
Number of Reed-Solomon frames received over bit error ratio interval.

UBLOCK_R<71:0>
72-bit vector to be sent to the XGMII containing two Link Interruption ordered sets.
The Link Interruption ordered set is defined in 46.3.4.

149.3.7.2.2 Variables

block_lock
Boolean variable that is set TRUE when receiver acquires block delineation.

hi_rfer
Boolean variable that is asserted TRUE when the rfer_cnt reaches 16 errors in one rfer_timer interval.

lp_low_snr
Boolean variable that is set TRUE when the link partner indicates LPI refresh is insufficient to maintain PHY SNR. It is set FALSE otherwise.

pcs_data_mode
Variable set by the PMA PHY Control function. See 149.4.4.1.

pcs_reset
Boolean variable that controls the resetting of the PCS. It is TRUE whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rx_coded<64:0>
Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 149–8. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_raw<71:0>
Vector containing two successive XGMII output transfers. RXC<3:0> for the first transfer are taken from rx_raw<3:0>. RXC<3:0> for the second transfer are taken from rx_raw<7:4>. RXD<31:0> for the first transfer are taken from rx_raw<39:8>. RXD<31:0> for the second transfer are taken from rx_raw<71:40>.

rf_valid
Boolean indication that is set TRUE if received Reed-Solomon frame is valid. Reed-Solomon frame is valid if and only if all parity checks of the Reed-Solomon code are satisfied.

tx_coded<64:0>
Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 149–8. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

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tx_raw<71:0>
: Vector containing two successive XGMII transfers. TXC<3:0> for the first transfer are placed in tx_raw<3:0>. TXC<3:0> for the second transfer are placed in tx_raw<7:4>. TXD<31:0> for the first transfer are placed in tx_raw<39:8>. TXD<31:0> for the second transfer are placed in tx_raw<71:40>.

The following variables are required for PHYs that support the EEE capability:

alert_detect
: Indicates that an alert signal from the link partner has been received at the MDI as indicated by PMA_ALERTDETECT.indication(alert_detect).

lpi_refresh_detect
: Set TRUE when the receiver has reliably detected refresh signaling. It is set FALSE otherwise.

lpi_tx_mode
: A variable indicating the signaling to be used from the PCS to the PMA across the PMA_UNITDATA.request (tx_symb) interface.
lpi_tx_mode controls tx_symb only when tx_mode is set to SEND_N.
The variable is set to NORMAL when (!tx_lpi_qr_active * !tx_lpi_alert_active), indicating that the PCS is in the normal mode of operation and will encode code-groups as described in Figure 149–16 and Figure 149–17.
The variable is set to REFRESH when (tx_lpi_qr_active * tx_refresh active).
The variable is set to QUIET when (tx_lpi_qr_active * !tx_refresh_active).
The variable is set to ALERT when (tx_lpi_alert_active).

rs_fec_frame_done
: A Boolean value. This variable is set TRUE when the final symbol of each RS-FEC frame is transmitted. It is set FALSE otherwise.

rx_lpi_active
: A Boolean variable that is set TRUE when the PHY receive function is operating in the LPI receive mode and set FALSE otherwise. The LPI receive mode begins when the sleep signal is detected and lasts until the alert signal is detected. When the EEE capability is not supported, rx_lpi_active is set FALSE.

rx_lpi_wake
: A Boolean variable that is set TRUE when the PHY receiver is in the WAKE state and sending IDLE to the XGMII. Set FALSE otherwise. When the EEE capability is not supported, rx_lpi_wake is set FALSE.

tx_alert_start_next
: A Boolean variable that is set TRUE on the frame prior to the one on which the alert transmission can start. It is set FALSE otherwise.

tx_lpi_active
: A Boolean variable that is set TRUE when the PHY transmit function is operating in the LPI transmit mode and during transitions to and from the LPI transmit mode (i.e., at any time when the PHY is transmitting sleep, alert, wake, or quiet-refresh signaling). It is set FALSE otherwise.

tx_lpi_qr_active
: A Boolean variable that is set TRUE during the LPI transmit mode, when the PHY is transmitting quiet-refresh signaling. It is set FALSE otherwise.

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tx_refresh_active
: A Boolean value. This variable is set TRUE following the logic described in 149.3.6.1.

tx_sleep_start_next
: A Boolean value. This variable is set TRUE during the seventh RS-FEC frame in every group of eight RS-FEC frames, where the group of eight RS-FEC frames start with the RS-FEC frame after refresh.

tx_lpi_req
: A Boolean variable that is set TRUE when the LPI client indicates that it is requesting operation in the LPI transmit mode via the XGMII. It is set FALSE otherwise.

149.3.7.2.3 Timers

rfer_timer
: Timer that is triggered every $125/(4 \times S)$ μs +1%, –25%. When the timer reaches its terminal count, rfer_timer_done = TRUE. See Table 149–1 for the definition of *S*.

The following timers are required for PHYs that support the EEE capability:

lpi_tx_sleep_timer
: This timer defines the time the local transmitter sends the sleep signal to the link partner.
Values: The condition lpi_tx_sleep_timer_done becomes TRUE upon timer expiration.
Duration: This timer shall have a period equal to eight RS-FEC frame periods.

lpi_tx_alert_timer
: This timer defines the time the local transmitter transmits the alert signal.
Values: The condition lpi_tx_alert_timer_done becomes TRUE upon timer expiration.
Duration: This timer shall have a period equal to four RS-FEC frame periods.

lpi_tx_wake_timer
: This timer defines the time the local transmitter transmits the wake signal.
Values: The condition lpi_tx_wake_timer_done becomes TRUE upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time RS-FEC frame periods.

lpi_rx_wake_timer
: This timer defines the time the receiver sends IDLE blocks to the XGMII after the alert signal is detected.
Values: The condition lpi_rx_wake_timer_done becomes TRUE upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time RS-FEC frame periods.

149.3.7.2.4 Functions

DECODE(rx_coded<64:0>)
: In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the RS-FEC decoder and decodes the 65B RS-FEC bit vector returning a vector rx_raw<71:0>, which is sent to the XGMII. The DECODE function shall decode the block based on code specified in 149.3.2.2.2.

ENCODE(tx_raw<71:0>)
: Encodes the 72-bit vector received from the XGMII, returning 65-bit vector tx_coded. The ENCODE function shall encode the block as specified in 149.3.2.2.2.

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R_BLOCK_TYPE = {C, S, T, D, E, I, LI, LII}

When the EEE capability is not supported, this function classifies each 65-bit rx_coded vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.

When the EEE capability is supported, this function classifies each 65-bit rx_coded vector as belonging to one or more of the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /I/, but in every other case the vector belongs to only one type.

Values: C; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x1E and eight valid control characters other than /E/ and /LI/;
b) A block type field 0x2D or 0x4B, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.

S; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.

T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.

D; The vector contains a data/ctrl header of 0.

I; If the optional EEE capability is supported, then the I type is a special case of the C type where the vector contains a data/ctrl header of 1, a block type field of 0x1E, and eight control characters of /I/.

LI: If the optional EEE capability is supported, then the LI type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and eight control characters of /LI/.

LII: If the optional EEE capability is supported, then the LII type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and one of the following:

a) Four control characters of /LI/ followed by four control characters of /I/;
b) Four control characters of /I/ followed by four control characters of /LI/

E; The vector does not meet the criteria for any other value.

A valid control character is one containing a MultiGBASE-T1 control code specified in Table 149–2. A valid O code is one containing an O code specified in Table 149–2.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E, I, LI, LII}

When the EEE capability is not supported, this function classifies each 72-bit tx_raw vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.

When the EEE capability is supported, this function classifies each 72-bit tx_raw vector as belonging to one or more of the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /I/, but in every other case the vector belongs to only one type.

Values: C; The vector contains one of the following:

a) Eight valid control characters other than /O/, /S/, /T/, /E/, and /LI/;
b) One valid ordered set and four valid control characters other than /O/, /S/, and /T/;
c) Two valid ordered sets.

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S; The vector contains an /S/ in its first or fifth character. Any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

I; If the optional EEE capability is supported, then the I type is a special case of the C type where the vector contains eight control characters of /I/.

LI; If the optional EEE capability is supported, then the LI type occurs when the vector contains eight control characters of /LI/.

LII; If the optional EEE capability is supported, then the LII type occurs when the vector contains one of the following:

a) Four control characters of /LI/ followed by four control characters of /I/;

b) Four control characters of /I/ followed by four control characters of /LI/.

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 149–2. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 149–2.

T_TYPE(tx_raw<71:0>)

Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

T_TYPE_NEXT

Prescient end of packet check function. It returns the FRAME_TYPE of the tx_raw vector immediately following the current tx_raw vector.

149.3.7.2.5 Counters

lpi_rxw_err_cnt

An integer value that counts the number of receive wake time faults. lpi_rxw_err_cnt is reset to zero during PCS_TEST. The counter is reflected in register 3.22 (see 45.2.3.12).

rfer_cnt

Count up to a maximum of RFER_CNT_LIMIT of the number of invalid Reed-Solomon frames within the current RFRX_CNT_LIMIT Reed-Solomon frame period.

rfrx_cnt

Count number Reed-Solomon frames received during current period.

149.3.7.2.6 Messages

RX_FRAME

A signal sent to PCS Receive indicating that a full Reed-Solomon frame has been decoded and the variable rf_valid is updated.

149.3.7.3 State diagrams

The RFER monitor state diagram shown in Figure 149–15 monitors the received signal for high RS-FEC frame error ratio.

The PCS 64B/65B Transmit state diagram shown in Figure 149–16 and Figure 149–17 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though

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the state diagram sends Local Fault ordered sets when reset is asserted, the scrambler and 65B RS-FEC are not guaranteed to be operational during reset. Thus, the Local Fault ordered sets are not guaranteed to appear on the PMA service interface.

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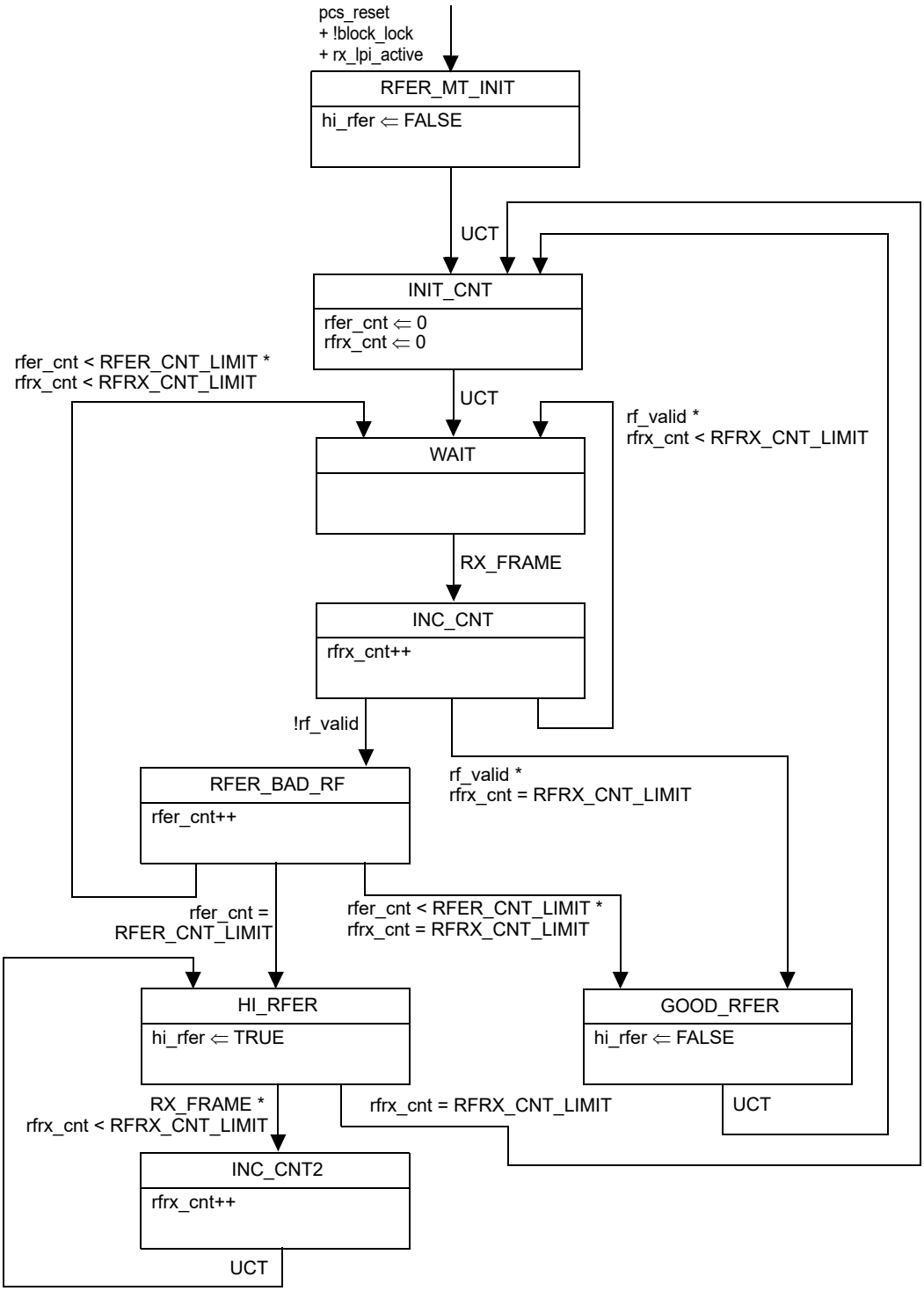

Figure 149–15—RFER monitor state diagram

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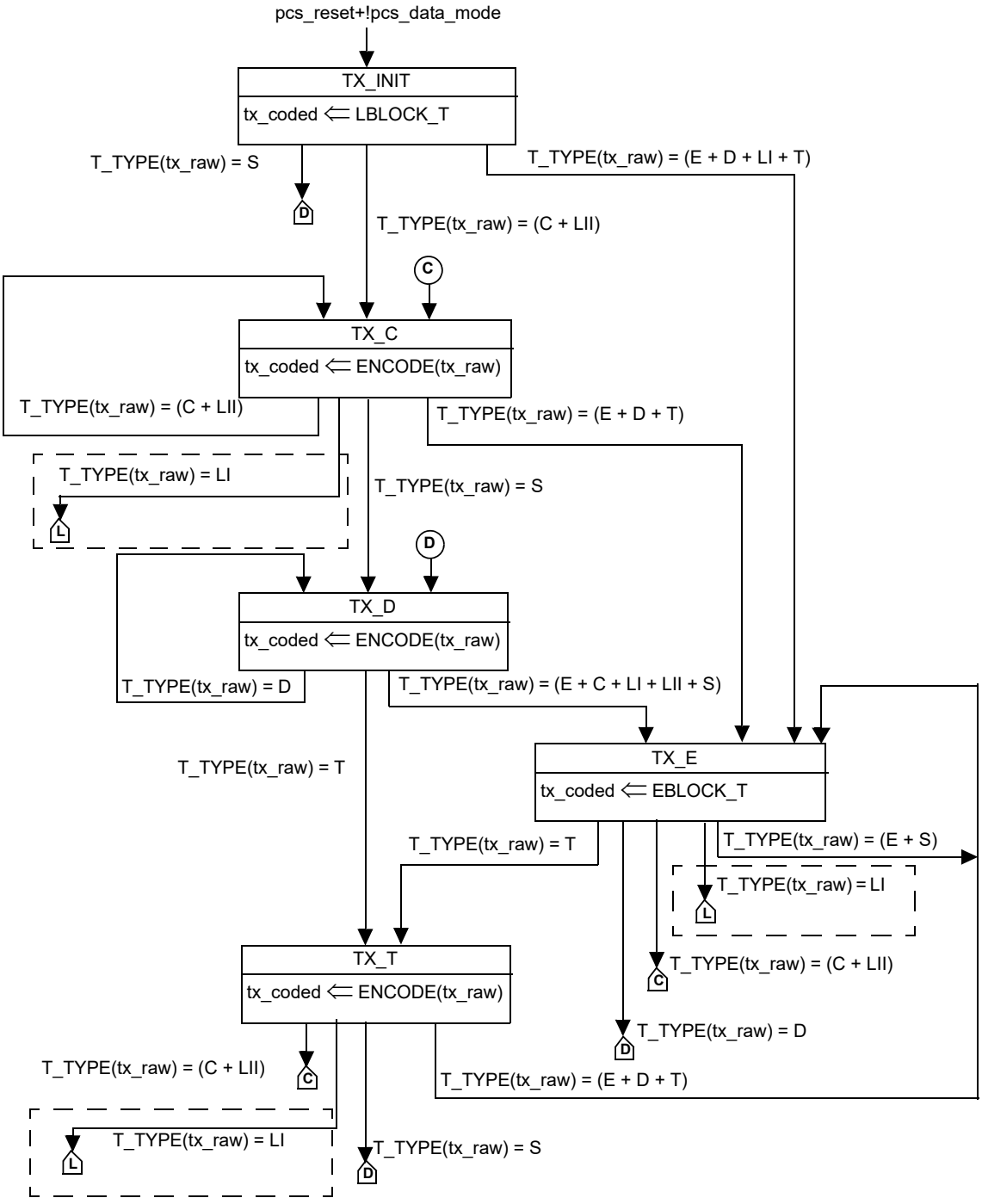

NOTE—Transitions inside dashed boxes are only required for the EEE capability.

Figure 149–16—PCS 64B/65B Transmit state diagram, part a

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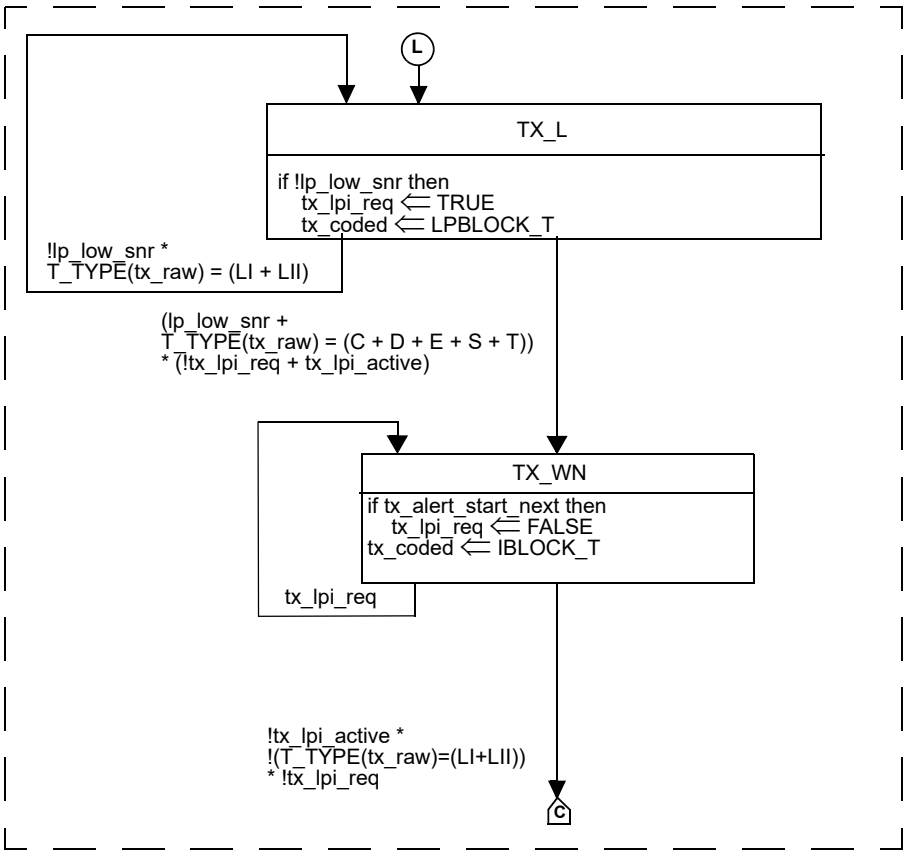

NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 149–17—PCS 64B/65B Transmit state diagram, part b

The PCS 64B/65B Receive state diagram is shown in Figure 149–18 and Figure 149–19 and controls the decoding of 65B received blocks. It makes exactly one transition for each receive block processed except for the transition from RX_WE to RX_E, which occurs immediately after the RX_WE processes are complete.

The PCS shall perform the functions of RFER monitor, Transmit, and Receive as specified in these state diagrams. The PCS shall not perform the RFER monitor function during LPI receive operation from the time that the PCS 64B/65B Receiver enters the state RX_L, until the state RX_W is exited.

Transitions surrounded by dashed rectangles indicate requirements for MultiGBASE-T1 EEE-capable implementations.

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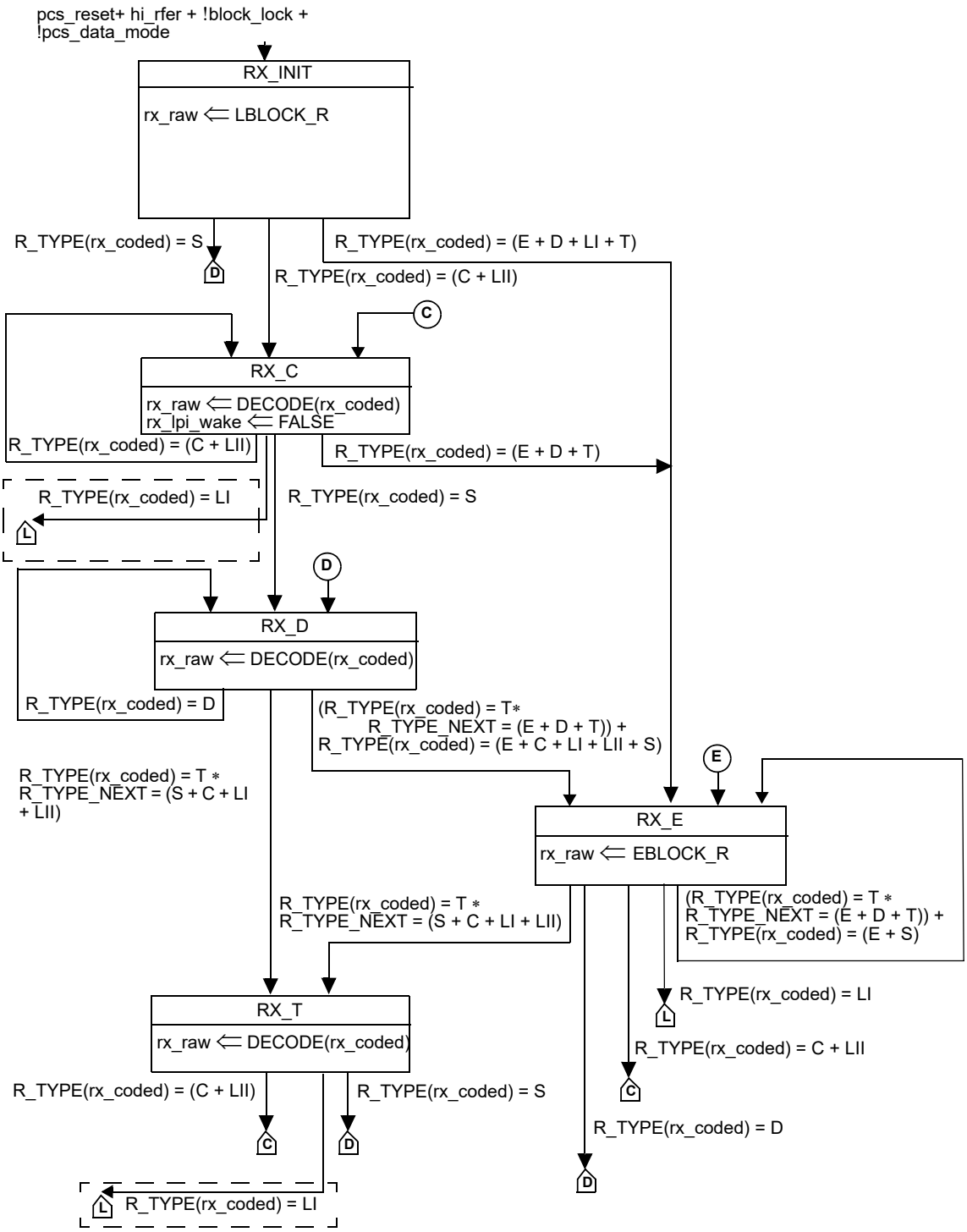

NOTE—Signals and functions shown with dashed lines are only required for the EEE capability.

Figure 149–18—PCS 64B/65B Receive state diagram, part a

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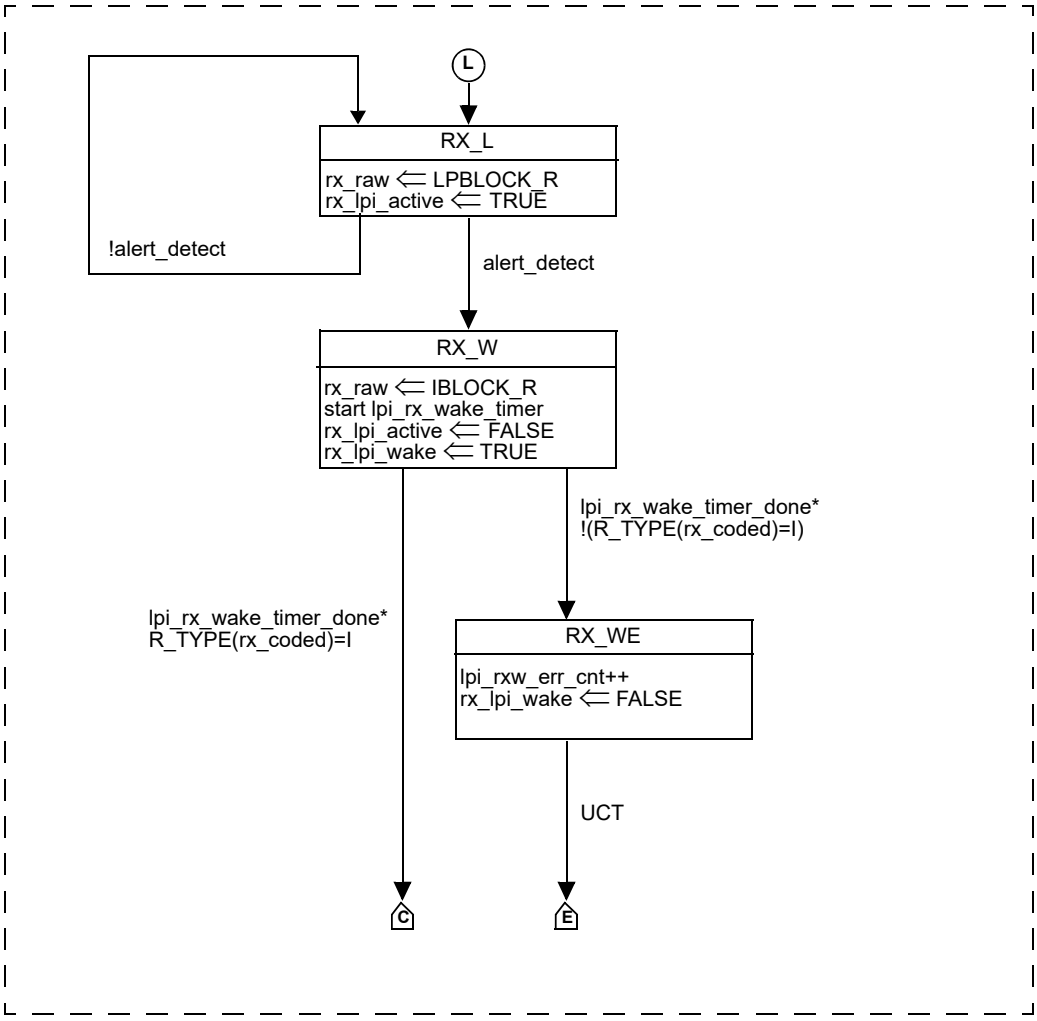

NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 149–19—PCS 64B/65B Receive state diagram, part b

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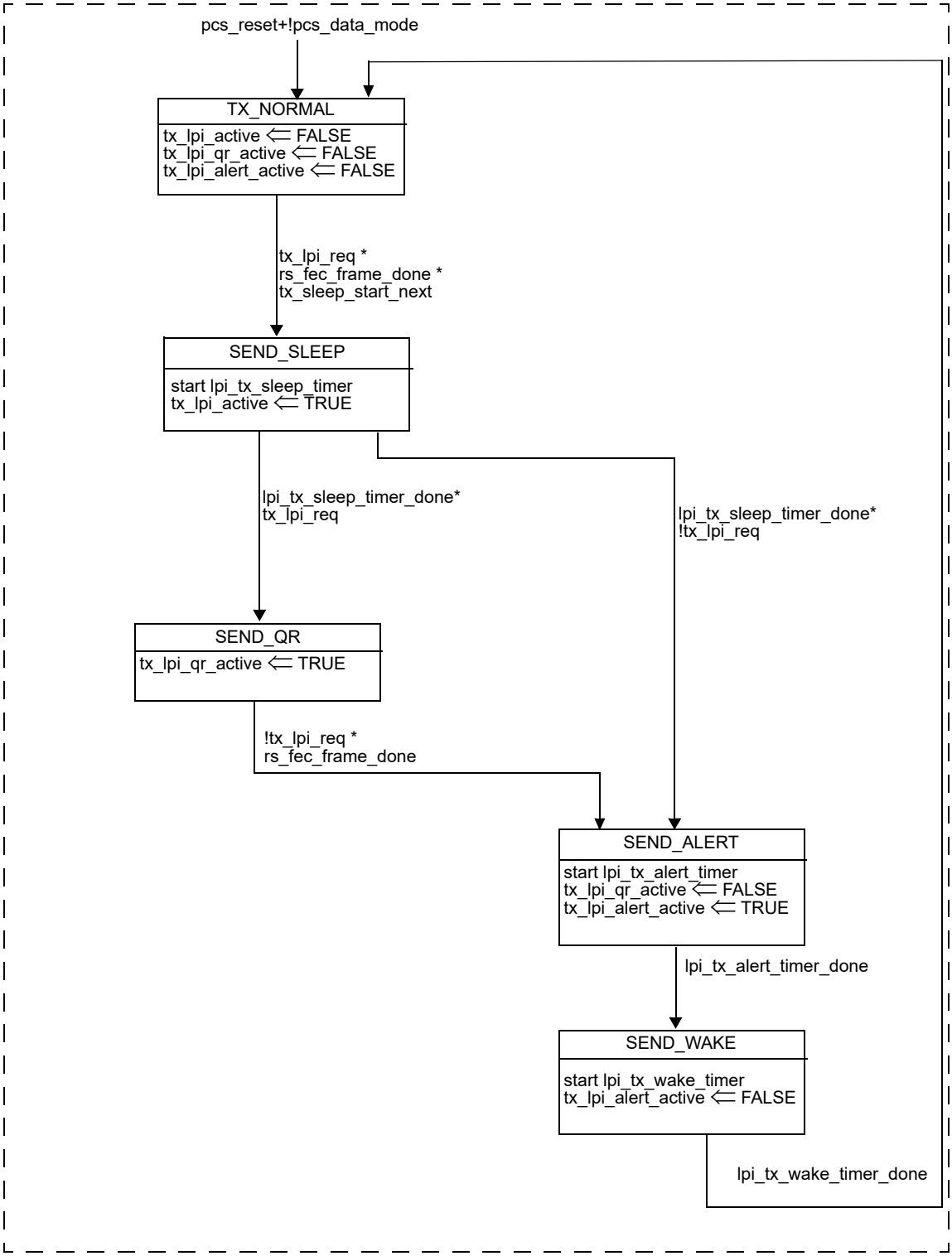

NOTE—This figure is mandatory for PHYs with the EEE capability.

Figure 149–20—EEE transmit state diagram

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149.3.8 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

149.3.8.1 Status

pcs_status:
: Indicates whether the PCS is in a fully operational state. It is only TRUE if pcs_data_mode is TRUE, block_lock is TRUE, and hi_rfer is FALSE. This status is reflected in MDIO bit 3.2324.10. A latch low view of this status is reflected in MDIO bit 3.2323.2 and the inverse of this status is reflected in MDIO bit 3.2323.7.

block_lock:
: Indicates the state of the block_lock variable. This status is reflected in MDIO bit 3.2324.8. A latching low version of this status is reflected in MDIO bit 3.2324.6.

hi_rfer:
: Indicates the state of the hi_rfer variable. This status is reflected in MDIO bit 3.2324.9. A latching high version of this status is reflected in MDIO bit 3.2324.7.

Rx LPI indication:
: For EEE capability, this variable indicates the current state of the receive LPI function. This flag is set to TRUE (register bit set to one) when the PCS Receive state diagram (Figure 149–19) is in the RX_L or RX_W states. This status is reflected in MDIO bit 3.2323.8. A latching high version of this status is reflected in MDIO bit 3.2323.10 (Rx LPI received).

Tx LPI indication:
: For EEE capability, this variable indicates the current state of the transmit LPI function. This flag is set to TRUE (register bit set to one) when the PCS Transmit state diagram (Figure 149–17) is in the TX_L or TX_WN states. This status is reflected in MDIO bit 3.2323.9. A latching high version of this status is reflected in MDIO bit 3.2323.11 (Tx LPI received).

149.3.8.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

RFER_count:
: 6-bit counter that counts each time the RFER_BAD_RF of the RFER monitor state diagram (see Figure 149–15) is entered. This counter is reflected in MDIO register bits 3.2324.5:0. The counter is reset when register 3.2324 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

149.3.8.3 Loopback

The PCS shall be placed in loopback mode when the loopback bit (MDIO bit 3.2322.14) is set to a one. In this mode, the PCS shall accept data on the transmit path from the XGMII and return it on the receive path to the XGMII. In addition, the PCS shall transmit a continuous stream of 65B RS-FEC encoded PAM4 symbols to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer.

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149.3.9 MultiGBASE-T1 operations, administration, and maintenance (OAM)

The MultiGBASE-T1 PCS level operations, administration, and maintenance (OAM) provides an optional mechanism useful for monitoring link operation such as exchanging PHY link health status and message exchange. When OAM is implemented, behavior shall conform to the state diagrams in Figure 149–24 and Figure 149–25. OAM information is exchanged out of band between two PHYs using excess bandwidth available on the link. The OAM is strictly between two PHYs on the Physical Layer and their associated management entities if present. Passing OAM information to other layers is outside the scope of this standard.

OAM is operational as long as both PHYs implement this mechanism and the link is up. It continues to be operational during Low Power Idle, albeit the information is transferred at a slower rate during the refresh cycle.

The OAM frame data is carried in the OAM 10-bit field described in 149.3.2.2.14 for the normal power data mode and 149.3.6.3 for low power mode. This 10-bit field is used to exchange OAM frames. The implementation of the OAM frame exchange function is optional. However, if EEE is implemented, then the OAM frame exchange function is implemented to exchange, at a minimum, the link partner OAM status.

For the remainder of this subclause, the term OAM is specific to the MultiGBASE-T1 PCS level OAM.

149.3.9.1 Definitions

OAM frame: A frame consisting of 14 octets of data, 14 framing bits, 14 reserved bits and two 10-bit Reed-Solomon parity symbols.

OAM symbol: A 10-bit symbol consisting of either one data octet plus a framing bit and a reserved bit, or a 10-bit Reed-Solomon parity symbol. Sixteen OAM symbols make up an OAM frame.

OAM field: A 10-bit field in each PHY frame reserved for the OAM symbol as described in 149.3.2.2.14 or in each refresh cycle as described in 149.3.6.3.

OAM message: A message contains a 4-bit message number plus 8 octets of message data (Message<7:0><7:0>) embedded in an OAM frame. The same OAM message can be repeated on multiple OAM frames.

OAM status: The 4 octets of status data (Message<11:8><7:0>) that is embedded in each OAM frame.

149.3.9.2 Functional specifications

149.3.9.2.1 MultiGBASE-T1 OAM frame structure

Each OAM frame is made up of 16 OAM symbols. Each of the first 14 symbols is made up of one octet of data, one framing bit, and one reserved bit. The last 2 symbols are the Reed-Solomon (16,14) parity symbols.

One OAM symbol is placed in the 10-bit OAM field in each PHY frame during normal power operation in the data mode. One OAM symbol is placed in the 10-bit OAM field in each refresh cycle during Low Power Idle. The sixteen OAM symbols are consecutively inserted into sixteen consecutive PHY frames and/or refresh cycles. Once the sixteen symbols of the current OAM frame are inserted, the sixteen symbols of the next OAM frame are inserted. This process is continuous without any break in the insertion of OAM symbols with the exception noted below.

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When the PCS frame is operating in interleaved mode of 2x or 4x, the first symbol (OAM<0>) shall be inserted in the first RS frame in the superframe so that the full OAM frame can be packed into eight superframes in the 2x interleaved mode, and into four superframes in the 4x interleaved mode.

When transitioning from normal operation to Low Power Idle, it is possible that part of the OAM frame is packed in RS frames and the remainder of the OAM frame is sent over the LPI refreshes.

When transitioning from Low Power Idle to normal operation, it is possible that part of the OAM frame is sent over the LPI refreshes and the remainder of the OAM frame is packed in RS frames. In some instances, it is possible that the remainder of the OAM frame cannot be aligned where the next OAM frame will have its first symbol (OAM<0>) inserted in the first RS frame of the superframe. In such cases, the partially transmitted OAM frame shall be interrupted according to the following rules:

1x interleaving — no interruption is required.

2x interleaving — insert 0 or 1 dummy OAM symbol into the superframe for alignment before continuing.

4x interleaving — insert 0 to 3 dummy OAM symbols into the superframe for alignment before continuing.

The receiver can anticipate when the dummy OAM symbols will be inserted based on the sequence of refresh and wake events.

The dummy OAM symbol is all 0’s and its value is ignored at the receiver.

An example in Figure 149–21 shows two dummy OAM symbols inserted to realign OAM<0> to the 4x interleaved superframe boundary.

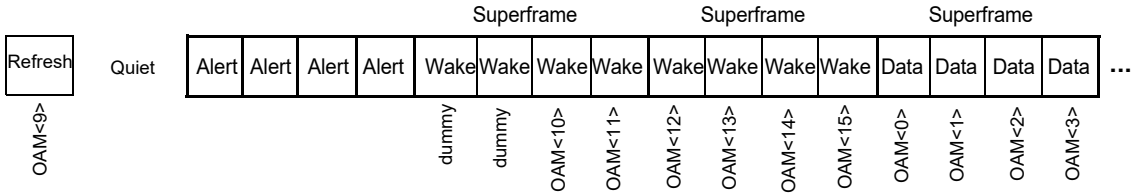

Figure 149–21—Example of 4x interleave dummy data insertion

Bit 0 of each OAM symbol is the first bit transmitted in the 10-bit OAM field. Symbol 0 is the first symbol transmitted in each OAM frame.

The OAM frame boundary can be found at the receiver by looking at bit D8. The boundary is a 0 followed by thirteen 1’s followed by two don’t care.

If OAM is not implemented then the 10-bit OAM field shall be set to all 0’s. If the link partner does not implement OAM, the 10-bit OAM field will remain static.

149.3.9.2.2 OAM frame data

The OAM frame data is shown in Figure 149–22. OAM<*x*><*y*> refers to symbol *x*, bit *y* of the OAM frame. Reserved fields shall be set to 0.

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	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Symbol 0	Reserved	0	Reserved	Reserved	Reserved	Reserved	PingRx	PingTx	SNR<1>	SNR<0>
Symbol 1	Reserved	1	Valid	Toggle	Ack	TogAck	Message_Number<3:0>			
Symbol 2	Reserved	1	Message<0><7:0>							
Symbol 3	Reserved	1	Message<1><7:0>							
Symbol 4	Reserved	1	Message<2><7:0>							
Symbol 5	Reserved	1	Message<3><7:0>							
Symbol 6	Reserved	1	Message<4><7:0>							
Symbol 7	Reserved	1	Message<5><7:0>							
Symbol 8	Reserved	1	Message<6><7:0>							
Symbol 9	Reserved	1	Message<7><7:0>							
Symbol 10	Reserved	1	Message<8><7:0>							
Symbol 11	Reserved	1	Message<9><7:0>							
Symbol 12	Reserved	1	Message<10><7:0>							
Symbol 13	Reserved	1	Message<11><7:0>							
Symbol 14	RS(16,14) parity									
Symbol 15	RS(16,14) parity									

Figure 149–22—OAM frame

149.3.9.2.3 Ping RX

The Ping RX is indicated in OAM<0><3>.

This bit is set by the PHY to the same value as the Ping TX bit received from the link partner.

149.3.9.2.4 Ping TX

The Ping TX is indicated in OAM<0><2>.

This bit is set by the PHY for the link partner to echo on Ping RX.

149.3.9.2.5 PHY health

The PHY Health (SNR<1:0>) is indicated in OAM<0><1:0>.

This status is set by the PHY to indicate the status of the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

— 00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame

— 01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled)

— 10: PHY SNR is marginal

— 11: PHY SNR is good

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149.3.9.2.6 OAM message valid

The OAM message valid (Valid) is indicated in OAM<1><7>.

- 0: Current OAM frame does not contain a valid OAM message
- 1: Current OAM frame contains a valid OAM message

149.3.9.2.7 OAM message toggle

The OAM message toggle (Toggle) is indicated in OAM<1><6>.

The toggle bit lets the management entity determine which OAM message is being referenced. The toggle bit in the current OAM message is set to the opposite value of the toggle bit in the previous OAM message only if link partner acknowledges the OAM message is received. This allows one OAM message to be delineated from a second OAM message since the same OAM message may be repeated over multiple OAM frames. This bit is valid only if Valid is set to 1.

149.3.9.2.8 OAM message acknowledge

The OAM message acknowledge (Ack) is indicated in OAM<1><5>.

Ack is set by the PHY to let the link partner know that the OAM message sent by the link partner was successfully received as defined in 149.3.9.2.14 and the PHY is ready to accept a new OAM message. An OAM message is defined to be Message_Number<3:0> and Message<7:0><7:0>.

- 0: No acknowledge
- 1: Acknowledge

149.3.9.2.9 OAM message toggle acknowledge

The OAM message toggle acknowledge (TogAck) is indicated in OAM<1><4>.

TogAck is set by the PHY to let the link partner know that the OAM message is being acknowledged. TogAck takes the value of Toggle bit of the OAM message being acknowledged. This bit is valid only if Ack is set to 1.

149.3.9.2.10 OAM message number

The OAM message number is indicated in OAM<1><3:0>.

This field is user-defined but it is recommended that it be used to indicate the meaning of the 8-octet message that follows. If used this way, up to 16 different 8-octet messages can be exchanged.

The message number is user-defined and its definition is outside the scope of this standard.

149.3.9.2.11 OAM message data

The OAM message data is indicated in OAM<9:2><7:0>.

The 8-octet message data is user-defined and its definition is outside the scope of this standard.

Ack is set by the PHY to let the link partner know that the OAM frame sent by the link partner is successfully received as defined. The OAM frame octet is the lower 8 bits of the 10-bit OAM symbol.

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149.3.9.2.12 OAM status

The OAM status data is indicated in OAM<13:10><7:0>.

These 32 bits are set by the PHY to convey its status in the mr_tx_message[95:64] to the link partner.

For additional information on the usage of these bits see Annex 149B.

149.3.9.2.13 OAM Reed-Solomon

The RS(16, 14) parity symbols are indicated in OAM<15:14><9:0>.

The OAM frame shall encode the 14 data symbols using Reed-Solomon code (16,14). The FEC code used is a shortened Reed-Solomon (16,14) code over the Galois Field of GF(2^{10}) — a code operating on 10-bit symbols. The code encodes 14 information symbols and adds 2 parity symbols, enabling correction of up to 1 symbol error. The code is systematic, meaning that the information symbols are not disturbed in any way in the encoder and the parity symbols are added separately to each block, and is based on the generating polynomial shown in Equation (149–8).

$$G(Z) = (Z - \alpha)(Z - 1) = A_2Z^2 + A_1Z^1 + A_0Z^0 \quad (149–8)$$

where

α is a root of the binary primitive polynomial $x^{10} + x^3 + 1$ and is represented as 0x002.
A is a series representing the resulting polynomial coefficients of $G(Z)$, (A_2 is equal to 0x001).
Z corresponds to a 10-bit GF(2^{10}) symbol.

The parity calculation shall produce the same result as the shift register implementation shown in Figure 149–23. Before calculation begins, the shift register shall be initialized to zero. The contents of the shift register are transmitted without inversion.

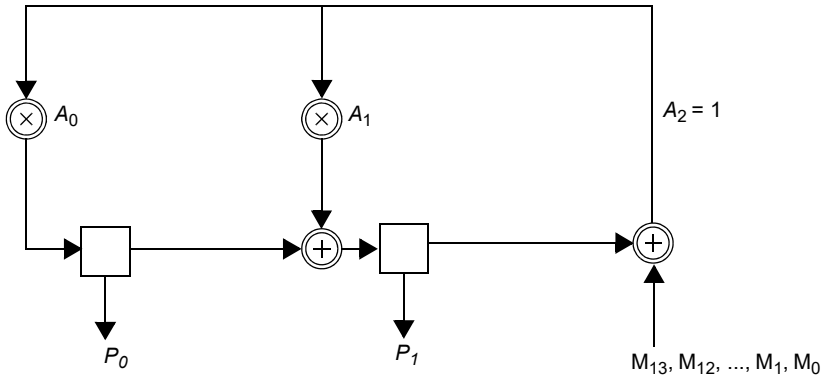

Figure 149–23—OAM FEC parity vector model

An FEC parity vector is represented by Equation (149–9).

$$P(Z) = M(Z) \bmod G(Z) \quad (149–9)$$

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where

M(Z)	is the data vector $M(Z) = M_{13}Z^{15} + M_{12}Z^{14} + \ldots + M_0Z^2$. M_{13} is the first 10-bit data symbol and M_0 is the last. (M_{13} corresponds to OAM<0><9:0>, M_{12} corresponds to OAM<1><9:0>, etc.)
P(Z)	is the parity vector $P(Z) = P_1Z^1 + P_0Z^0$. P_1 (OAM<14><9:0>) is the first 10-bit parity symbol and P_0 (OAM<15><9:0>) is the last.
A data/parity symbol	(d_9, d_8, …, d_0) is identified with the element: $d_9\alpha^9 + d_8\alpha^8 + \ldots + d_0\alpha^0$ in GF(2^{10}), the finite field with 2^{10} elements.
d_0	is identified as the LSB (OAM<*><0>).
d_9	is identified as the MSB (OAM<*><9>) for all symbols.

The OAM Reed-Solomon parity symbol generation/correction is required only when EEE is implemented. When all 16 symbols of the OAM are embedded in tx_RSmessage<9:0> as described in 149.3.2.2.17 then OAM<15:14><9:0> are dummy symbols and are ignored at the receiver.

149.3.9.2.14 MultiGBASE-T1 OAM frame acceptance criteria

All fields of the OAM frame shall be accepted and updated, unless any of the following occurs:

a) RS(16, 14) contains an uncorrectable error, or

b) there is an uncorrectable PHY frame on any of the 16 symbols.

149.3.9.2.15 PHY health indicator

The PHY current health is sent to the link partner on a per OAM frame basis using the SNR<1:0> bits as described in 149.3.9.2.5. It lets the link partner have an early indication of potential problems that can cause the PHY to drop link or have high error rates.

If EEE is implemented, there can be a case where a PHY's receiver can no longer maintain good SNR based on quiet/refresh cycles. Instead of dropping the link, the PHY can attempt to recover the link by forcing the link partner to exit LPI in its egress direction so that the PHY can use normal power mode to recover. This is done by transmitting SNR<1:0> with a value of 01.

If a PHY receives SNR<1:0> set to 01 by its link partner, then it cannot enter into LPI in the egress direction. If the PHY is already in LPI then the PHY shall immediately exit LPI.

149.3.9.2.16 Ping

The PingTx bit is set based on the value in mr_tx_ping. The PingRx bit is set based on the latest PingTx received from the link partner. The value in mr_rx_ping is set based on the received PingRx from the link partner. The user can determine that the link partner OAM is operating properly by toggling mr_tx_ping and observing mr_rx_ping matches after a short delay.

The Ping bits are updated on a per OAM frame basis.

149.3.9.2.17 OAM message exchange

Unlike the PHY health indicator, the ping function, and the OAM status that operate on a per OAM frame basis, the OAM message exchange operates on a per OAM message basis that may occur over many OAM frames. The OAM message exchange mechanism allows a management entity attached to a PHY and its peer attached to the link partner to asynchronously pass OAM messages and verify their delivery.

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The OAM message is first written into the OAM transmit registers in the PHY. The OAM message is then read out of the OAM transmit registers and transmitted to the link partner. After the link partner receives the OAM message, it transfers it into the link partner's OAM receive registers and also sends an acknowledge back to the PHY indicating that the next OAM message can be transmitted. One OAM message can be loaded into the OAM transmit registers while another OAM message is being transmitted by the PHY to the link partner, while yet another OAM message is being read out at the link partner's OAM receive registers. The exchange of OAM messages is occurring concurrently and bi-directionally. The transfers between the management entities can be done asynchronously. On the transmit side, mr_tx_valid = 0 indicates that the next OAM message can be written into the OAM transmit registers. Once the registers are written, the management entity sets mr_tx_valid to 1 to indicate that the OAM transmit registers contain a valid OAM message. Once the message is read out atomically, the state diagram clears the mr_tx_valid to 0 to indicate that the registers are ready to accept the next OAM message.

On the receive side, mr_rx_lp_valid indicates that valid OAM message can be read from the OAM receive registers. Once these registers are read, the mr_rx_lp_valid should be cleared to 0 to indicate that the registers are ready to receive the next OAM message. If mr_rx_lp_valid is not cleared, then the OAM message transfer will eventually stall since the sender cannot send new OAM messages if the receiver does not acknowledge that an OAM message has been transferred into the OAM receive registers.

The management entities can asynchronously read mr_tx_valid and mr_rx_lp_valid to know when OAM messages can be transferred in and out of the OAM registers.

The toggle bit alternates between 0 and 1, which lets the management entity determine which OAM message is being referred to. The toggle bit transitioning rules between one OAM frame and the next OAM frame are shown in Table 149–8.

Table 149–8—Toggle bit transition rules

Previous Valid	Previous Toggle	Current Valid	Current Toggle	Description
0	0	0	0	No valid OAM message
0	0	0	1	Illegal transition (Error)
0	0	1	0	New OAM message starting
0	0	1	1	Illegal transition (Error)
0	1	0	0	Illegal transition (Error)
0	1	0	1	No valid OAM message
0	1	1	0	Illegal transition (Error)
0	1	1	1	New OAM message starting
1	0	0	0	Illegal transition (Error)
1	0	0	1	Received acknowledge, no new OAM message to send
1	0	1	0	Repeating current OAM message, waiting for link partner's acknowledge
1	0	1	1	Previous OAM message ending, new OAM message starting
1	1	0	0	Received acknowledge, no new OAM message to send

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Table 149–8—Toggle bit transition rules *(continued)*

Previous Valid	Previous Toggle	Current Valid	Current Toggle	Description
1	1	0	1	Illegal transition (Error)
1	1	1	0	Previous OAM message ending, new OAM message starting
1	1	1	1	Repeating current OAM message, waiting for link partner's acknowledge

149.3.9.3 State diagram variable to OAM register mapping

The state diagrams of Figure 149–24 and Figure 149–25 generate and accept variables of the form "mr_x," where x is an individual signal name. These variables comprise a management interface to communicate the OAM information to and from the management entity. Clause 45 MDIO registers are defined in MMD3 to support the OAM. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the information is recommended. Table 97–6 and Table 149–9 describe the MDIO register to the state diagrams variable mapping.

Table 149–9—State variables to OAM register mapping

MDIO control/status variable	PCS register name	Register/bit number	PCS control/status variable
MultiGBASE-T1 OAM status Message 8	MultiGBASE-T1 OAM status message register	3.2318.7:0	mr_tx_message[71:64]
MultiGBASE-T1 OAM status Message 9	MultiGBASE-T1 OAM status message register	3.2318.15:8	mr_tx_message[79:72]
MultiGBASE-T1 OAM status Message 10	MultiGBASE-T1 OAM status message register	3.2319.7:0	mr_tx_message[87:80]
MultiGBASE-T1 OAM status Message 11	MultiGBASE-T1 OAM status message register	3.2319.15:8	mr_tx_message[95:88]
Link partner MultiGBASE-T1 OAM status Message 8	Link partner MultiGBASE-T1 OAM status message register	3.2320.7:0	mr_rx_lp_message[71:64]
Link partner MultiGBASE-T1 OAM status Message 9	Link partner MultiGBASE-T1 OAM status message register	3.2320.15:8	mr_rx_lp_message[79:72]
Link partner MultiGBASE-T1 OAM status Message 10	Link partner MultiGBASE-T1 OAM status message register	3.2321.7:0	mr_rx_lp_message[87:80]
Link partner MultiGBASE-T1 OAM status Message 11	Link partner MultiGBASE-T1 OAM status message register	3.2321.15:8	mr_rx_lp_message[95:88]

149.3.9.4 Detailed functions and state diagrams

149.3.9.4.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, counters, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

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149.3.9.4.2 State diagram parameters

149.3.9.4.3 Variables

frame_boundary

Frame boundary detection based on the latest 16 rx_oam_field<8> received. The leftmost bit is the earliest received bit.

Values:

TRUE: latest 16 rx_oam_field<8> = 01111111111111xx

FALSE: latest 16 rx_oam_field<8> ≠ 01111111111111xx

link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_rx_lp_message[95:0]

Twelve octet OAM message from the link partner. mr_rx_lp_message[63:0] in this variable is valid only when mr_rx_lp_valid is 1. mr_rx_lp_message[95:64] is always valid and continuously updated.

mr_rx_lp_message_num[3:0]

Four bit message number from the link partner. The value in this variable is valid only when mr_rx_lp_valid is 1.

mr_rx_lp_SNR[1:0]

Link partner health status.

Values:

00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame.

01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled).

10: PHY SNR is marginal.

11: PHY SNR is good.

The threshold for the status is implementation dependent.

mr_rx_lp_toggle

The toggle bit value associated with the eight octet BASE-T1 OAM message from the link partner.

Values:

The toggle bit alternates between 0 and 1.

mr_rx_lp_valid

Indicates whether the OAM message in mr_rx_lp_message[63:0], mr_rx_lp_message_num[3:0] and the toggle bit in mr_rx_lp_toggle is valid or not. This variable should be cleared when mr_rx_lp_message[63:48] is read and is not explicitly shown in the state diagram. The clearing of this variable indicates to the state diagram that the BASE-T1 OAM message is read by the user and the state diagram can proceed to load in the next BASE-T1 OAM message.

Values:

0: invalid

1: valid

mr_rx_ping

Echoed ping value from the link partner.

Values:

The value can be 0 or 1.

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mr_tx_message[95:0]

Eight-octet BASE-T1 OAM message and four-octet MultiGBASE-T1 status transmitted by the local PHY. mr_tx_message[63:0] in this variable is valid only when mr_tx_valid is 1. mr_tx_message[95:64] in this variable is always valid.

mr_tx_message_num[3:0]

Four-bit message number transmitted by the local PHY. The value in this variable is valid only when mr_tx_valid is 1.

mr_tx_ping

Ping value transmitted by the local PHY.

Values:

The value can be 0 or 1.

mr_tx_received

Indicates whether the most recently transmitted BASE-T1 OAM message with a toggle bit value of mr_tx_received_toggle was received, read, and acknowledged by the link partner. This variable shall clear on read.

Values:

0: BASE-T1 OAM message was not received and read by the link partner.

1: BASE-T1 OAM message was received by the link partner.

mr_tx_received_toggle

Toggle bit value of the BASE-T1 OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if mr_tx_received is 1.

Values:

The value can be 0 or 1.

mr_tx_SNR[1:0]

Status register indicating PHY health status.

Values:

00: PHY link is failing and will drop link and relink within 2 to 4 ms after the end of the current OAM frame.

01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled).

10: PHY SNR is marginal.

11: PHY SNR is good.

The threshold for the status is implementation dependent.

mr_tx_toggle

The toggle bit value associated with the eight-octet BASE-T1 OAM message transmitted by the PHY. The value is automatically set by the state diagram and cannot be set by the user. This bit should be read and recorded prior to setting mr_tx_valid to 1.

Values:

The toggle bit alternates between 0 and 1.

mr_tx_valid

Indicates whether BASE-T1 OAM message in mr_tx_message[63:0] and mr_rx_lp_message_num[3:0] is valid or not. This register will be cleared by the state diagram to indicate whether the next BASE-T1 OAM message can be written into the registers.

Values:

0: invalid

1: valid

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reset

Reset

Values:

FALSE: OAM circuit is not in reset.

TRUE: OAM circuit is in reset.

rs_check

Status of the latest rs_correct() operation

Values:

GOOD: no errors or correctable error

BAD: uncorrectable error

rx_ack

Acknowledge from link partner in response to PHY's BASE-T1 OAM message.

Values:

0: no acknowledge

1: acknowledge

rx_ack_toggle

The toggle value corresponding to the PHY's BASE-T1 OAM message that the link partner is acknowledging. This value is valid only if the rx_ack is set to 1.

Values:

The toggle bit can take on values of 0 or 1.

rx_boundary

This variable is set to TRUE whenever the receive data stream reaches the end of a Reed-Solomon frame and a dummy OAM symbol is not expected per 149.3.9.2.1 during normal power operation in the data mode, or at the end of a received refresh cycle during Low Power Idle operation. This variable is set to FALSE at other times.

Values:

FALSE: Receive stream is not at a boundary end.

TRUE: Receive stream is at a boundary end.

rx_exp_toggle

This variable holds the expected toggle value of the next BASE-T1 OAM message. This is normally the opposite value of the current toggle value, but shall reset on error conditions where two back-to-back BASE-T1 OAM messages separated by BASE-T1 OAM frames without a valid message have the same toggle value.

Values:

The toggle bit can take on values of 0 or 1.

rx_lp_ack

Acknowledge from PHY in response to link partner's BASE-T1 OAM message. Indicates whether valid BASE-T1 OAM message from the link partner has been sampled into the PHY's registers.

Values:

0: no acknowledge / not sampled

1: acknowledge / sampled

rx_lp_ping

Ping value received from the link partner that is looped back.

Values:

The value can be 0 or 1.

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rx_lp_toggle

The toggle bit value in the previous BASE-T1 OAM frame received from the link partner.

Values:

The toggle bit alternates between 0 and 1.

rx_lp_valid

Indicates whether BASE-T1 OAM message in previous BASE-T1 OAM frame received from the link partner is valid or not.

Values:

0: invalid
1: valid

rx_oam_field<9:0>

Ten-bit BASE-T1 OAM symbol extracted from a received Reed-Solomon frame during normal power operation in the data mode, or from a received refresh cycle during Low Power Idle operation.

rx_oam<15 to 0><9:0>

Raw 16-symbol OAM frame received from the link partner.

SNR[1:0]

PHY health status.

Values:

00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame.
01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled).
10: PHY SNR is marginal.
11: PHY SNR is good.

Both the status threshold and condition for generating this status are implementation dependent.

tx_boundary

This variable is set to TRUE whenever the transmit data stream reaches the start of a PHY frame and a dummy OAM symbol is not transmitted per 149.3.9.2.1 during normal power operation in the data mode, or at the start of a transmit refresh cycle during Low Power Idle operation. This variable is set to FALSE at other times.

Values:

FALSE: Transmit stream is not at a boundary end.
TRUE: Transmit stream is at a boundary end.

tx_oam_field<9:0>

Ten-bit BASE-T1 OAM symbol inserted into a transmitted Reed-Solomon frame during normal power operation in the data mode, or into a transmitted refresh cycle during Low Power Idle operation.

tx_oam<15 to 0><9:0>

Raw 16-symbol OAM frame transmitted from the PHY.

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tx_lp_ready

Indicates whether the link partner is ready to receive the next BASE-T1 OAM message from the PHY. If ready, then the PHY will load the next BASE-T1 OAM message from the registers and begin transmitting them.

Values:

0: not ready
1: ready

tx_toggle

The toggle bit value being sent in the current BASE-T1 OAM frame transmitted by the PHY.

Values:

The value can be 0 or 1.

149.3.9.4.4 Counters

rx_cnt

A count of received OAM frame symbols.

Values:

The value can be any integer from 0 to 16, inclusive.

tx_cnt

OAM frame transmit symbol count.

Values:

The value can be any integer from 0 to 16, inclusive.

tx_rec

A count of received RS-FEC block errors, both correctable and uncorrectable.

Values:

The value can be any integer from 0 to 65 535, inclusive.

149.3.9.4.5 Functions

rs (14 OAM symbols)

This function outputs the 2 parity symbols as defined in 149.3.9.2.13.

If all 16 symbols of the OAM frame are embedded in tx_RSmessage<9:0> as described in 149.3.2.2.15 then this function can return any arbitrary value.

rs_correct (16 OAM symbols)

This function outputs the 14 corrected data symbols as defined in 149.3.9.2.13 and sets/clears the rs_check variable when at least one of the 16 symbols of the OAM frame is embedded in a LPI refresh.

Otherwise, this function returns the 14 data symbols unmodified and sets rs_check to GOOD if none of the 16 RS(360, 326) frames are uncorrectable.

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149.3.9.4.6 State diagrams

The receive state diagram is shown in Figure 149–24 and the transmit state diagram is shown in Figure 149–25.

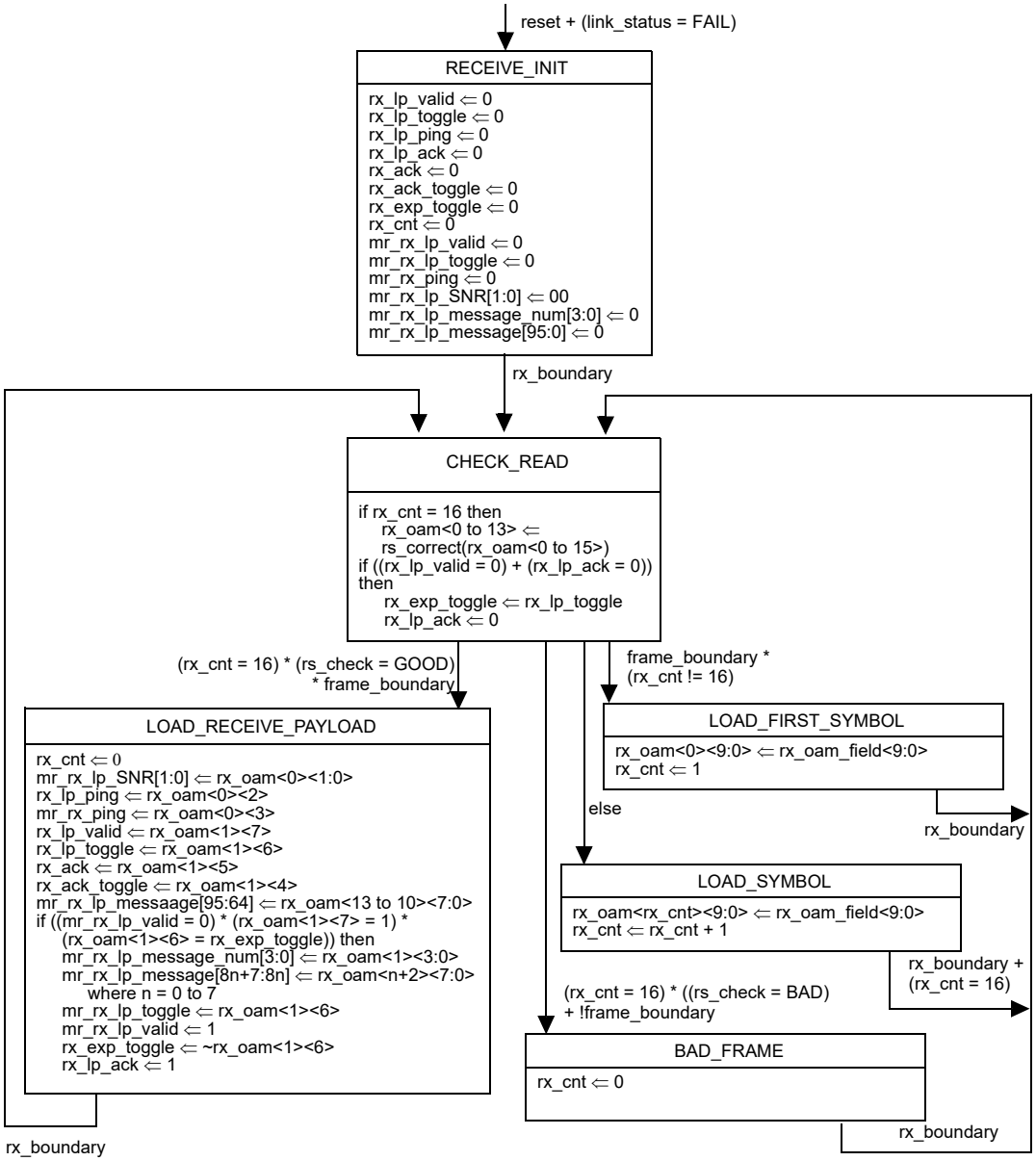

Figure 149–24—Receive state diagram

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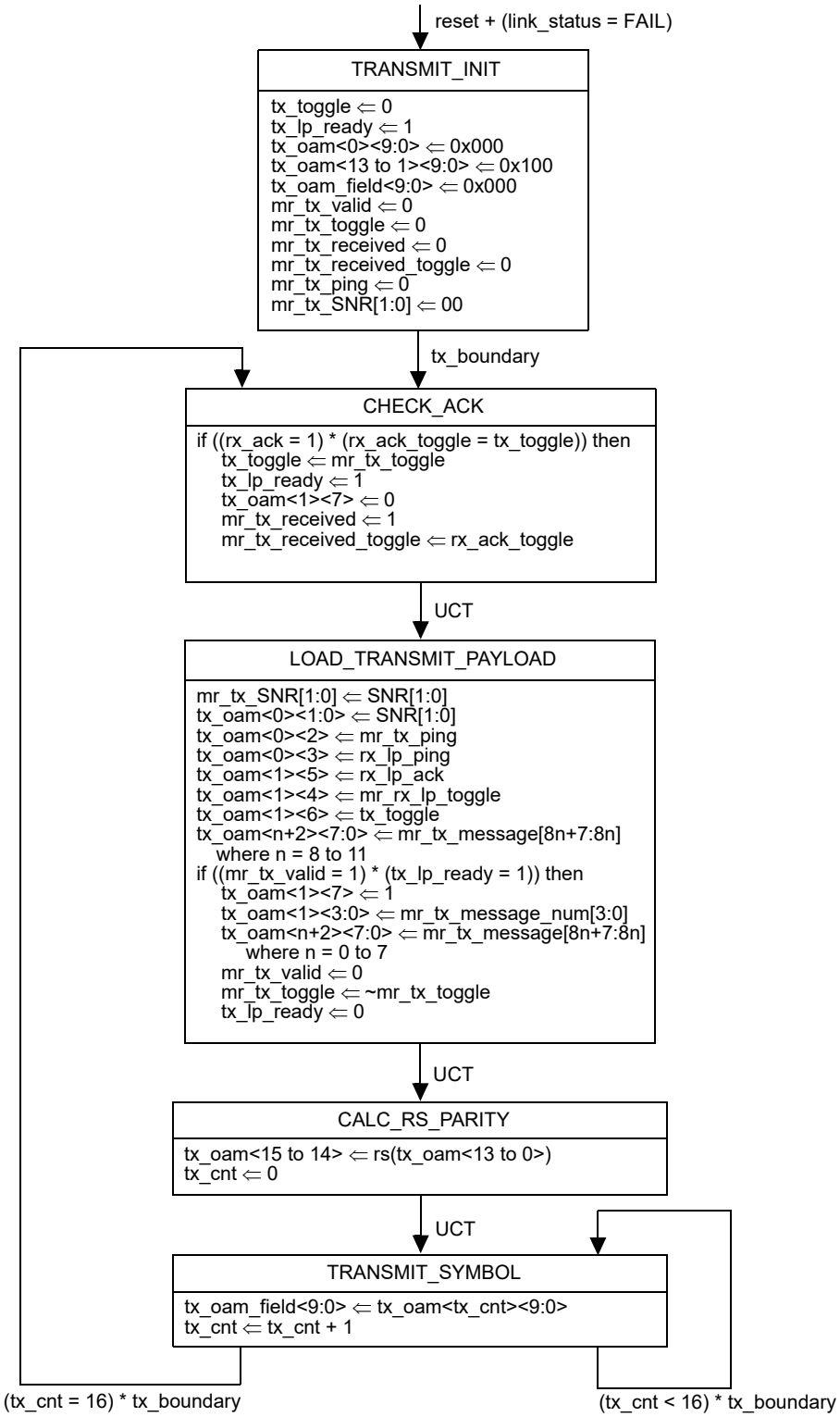

Figure 149–25—Transmit state diagram

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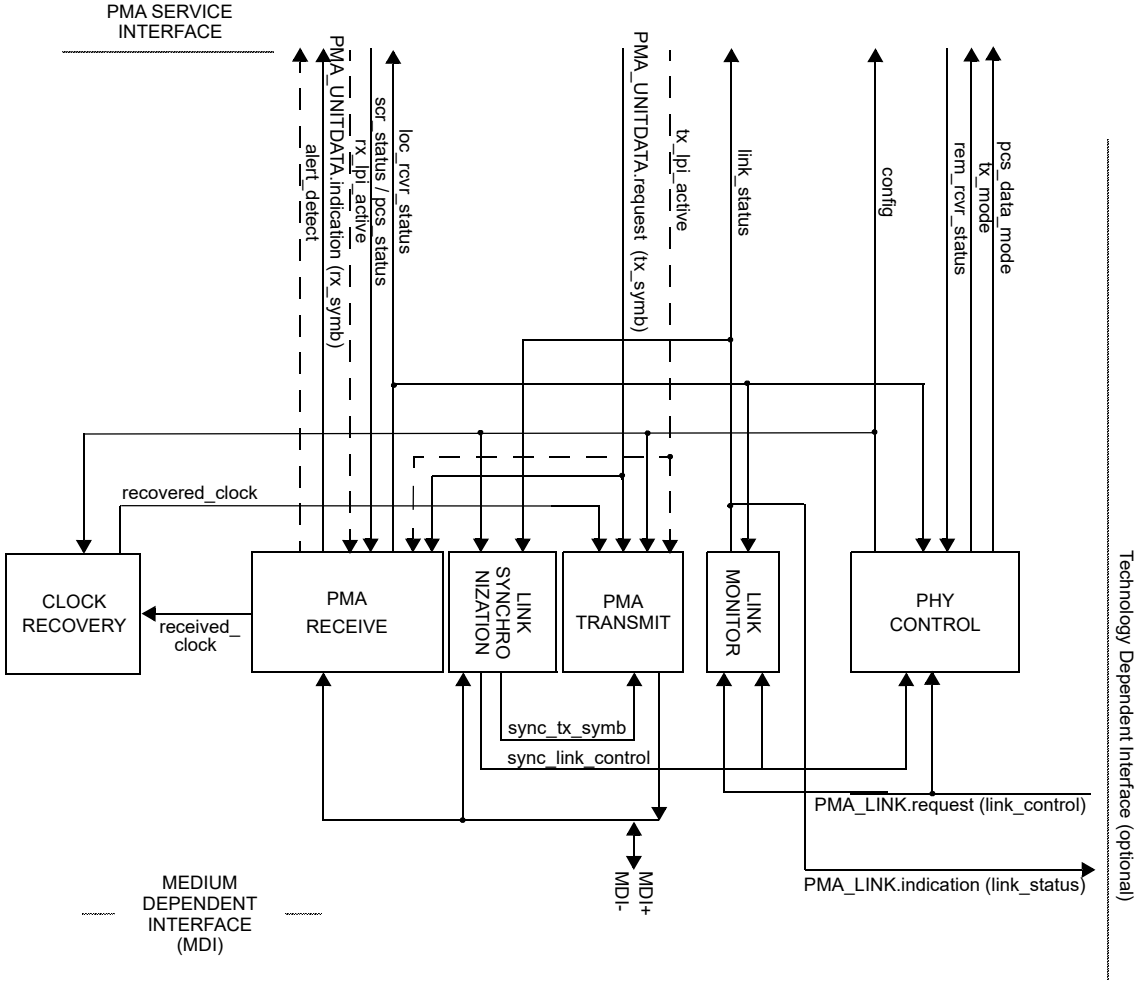
149.4 Physical Medium Attachment (PMA) sublayer

149.4.1 PMA functional specifications

The PMA couples messages from the PMA service interface specified in 149.2.2 to the MultiGBASE-T1 baseband medium, specified in 149.7.

The interface between the PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 149.8.



NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

Figure 149–26—PMA reference diagram

149.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

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The PMA reference diagram, Figure 149–26, shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 149–26.

149.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power for the device containing the PMA has not reached the operating state.
b) The receipt of a request for reset from the management entity.

PMA Reset sets pma_reset = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The MultiGBASE-T1 PMA takes no longer than 100 ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 149–32).

149.4.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a four-level modulated signal on the single balanced pair of conductors. When the PHY Control state diagram (Figure 149–32) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI. During Link Synchronization, when sync_link_control = DISABLE and Auto-Negotiation is either not enabled or is not implemented, the sync_tx_symb output by the PHY Link Synchronization function shall be used in place of tx_symb as the data source for PMA Transmit. When lpi_tx_mode = ALERT, the PN sequence defined in 149.4.2.6 shall be used in place of tx_symb as the data source for PMA Transmit. The signals generated by PMA Transmit shall comply with the electrical specifications given in 149.5.2.

When the PMA_CONFIG.indication parameter config is MASTER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 149.5.2.3. The MASTER-SLAVE relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 149.4.2.8 while meeting the jitter requirements of 149.5.2.3.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

149.4.2.2.1 Global PMA transmit disable

When the PMA_transmit_disable variable is set to TRUE, this function shall turn off the transmitter so that the average launch power of the transmitter is less than –53 dBm.

149.4.2.3 PMA Receive function

The PMA Receive function comprises a receiver for PAM4 signals on the balanced pair. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over the receive pair and to present these sequences to the PCS Receive function. The PMA translates the signals received on the pair into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 2×10^{-10} after RS-FEC decoding, over a channel meeting the requirements of 149.7.

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To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization and echo cancellation. The sequence of symbols assigned to tx_symb is needed to perform echo cancellation.

The PMA Receive function uses the parameters pcs_status and scr_status, and the state of the equalization, cancellation, and estimation functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other value (see the PHY Control state diagram in Figure 149–32). The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for pair polarity swaps.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.243.7.

149.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram in Figure 149–32.

During PMA training (TRAINING and COUNTDOWN states in Figure 149–32), PHY Control information is exchanged between link partners with a 12-octet Infofield, which is XORed with the first 96 bits of the 16th partial PHY frame (bits 6750 to 6845). The Infofield is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions prior to the PAM2 to PAM4 transition.

The 12-octet Infofield shall include the fields in 149.4.2.4.2 through 149.4.2.4.8, also shown in Figure 149–27 and Figure 149–28. Infofield shall be transmitted at least 256 times with each change to octets 7 to 10.

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	PHY Capability Bits	CRC16

Figure 149–27—Infofield TRAINING format

PMA_state = 01

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 149–28—Infofield COUNTDOWN format

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149.4.2.4.1 Infofield notation

For all the Infofield notations in the following subclauses, Reserved<bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The Infofield is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

149.4.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of three octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Octet 1<7:0> and so forth.

149.4.2.4.3 Partial PHY frame count (PFC24)

The partial PHY frame count consists of 3 octets [Oct4<7:0>, Oct5<7:0>, Oct6<7:0>] and indicates the running count of partial PHY frames sent LSB first. There are 16 partial PHY frames per PHY frame and the Infofield is embedded within the 16th partial PHY frame. The first partial PHY frame is zero, thus the first partial PHY frame count field after a reset is 15.

PFC24 continues to run uninterrupted for the duration of the link. The resolution of PFC24 is large enough that it does not rollover during the allotted training time. However, it will rollover if allowed to run indefinitely. PFC24 is defined to rollover to 0 after it reaches 16 776 959 to align with the EEE QR cycle.

149.4.2.4.4 Message Field

The Message Field is one octet. For the MASTER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, en_slave_tx<4>, reserved<3:0>}. For the SLAVE, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING, and PMA_state<7:6> = 01 indicates COUNTDOWN.

All possible Message Field settings are listed in Table 149–10 for the MASTER and Table 149–11 for the SLAVE. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 149–10 for the MASTER and the first or second row of Table 149–11 for the SLAVE. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infofield variable is set to loc_rcvr_status<5> = 1 and set to 0 otherwise.

Table 149–10—Infofield message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

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Table 149–11—Infofield message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

149.4.2.4.5 PHY capability bits

When PMA_state<7:6> = 00, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the PHY capability bits. Each octet is sent LSB first. See Table 149–12 for the details.

Table 149–12—PHY capability bits

octet 8								octet 9								octet 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
VendorSpecificData																Reserved	InterleaverDepth		PrecodeSel		SlowWakeRequest	EEEen	OAMen

The format of PHY capability bits is Oct10<2:1> = InterleaverDepth[1:0], Oct10<4:3> = PrecodeSel[1:0], Oct10<5> = SlowWakeRequest, Oct10<6> = EEEen, Oct10<7> = OAMen, Oct8<7:0> = VendorSpecificData[7:0], and Oct9<7:0> = VendorSpecificData[15:8].

EEEen and OAMen indicate EEE and MultiGBASE-T1 OAM capability enable, respectively. The PHY shall indicate the support of these two optional capabilities by setting the corresponding capability bits.

The optional EEE capability shall be enabled only if both PHYs set the capability bit EEEen = 1. The optional BASE-T1 OAM capability shall be enabled only if both PHYs set the capability bit OAMen = 1. InterleaverDepth indicates the requested data mode interleaving depth. PrecodeSel indicates the requested precoder. SlowWakeRequest is set to indicate to the link partner that the PHY will transmit alert only immediately following a refresh.

The capability bit values shall be considered as valid only when the loc_rcvr_status bit is 1.

The remaining bits shall be reserved and set to 0.

149.4.2.4.6 Data switch partial PHY frame count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the data switch partial PHY frame count (DataSwPFC24) sent LSB first. DataSwPFC24 indicates the partial PHY frame count

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when the transmitter switches from PAM2 to PAM4, which occurs at the start of an RS-FEC superframe. The last value of PFC24 prior to the transition is DataSwPFC24 – 1. DataSwPFC24 shall be set to an integer multiple of 16. When the value of DataSwPFC24 is a multiple of 16 the switch from PAM2 to PAM4 occurs on a PHY frame boundary. DataSwPFC24 shall be a minimum of 4081 and a maximum of 4785 from the current PFC24 value.

149.4.2.4.7 Reserved fields

When PMA_state<7:6> is greater than 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains a reserved field. All Infofield fields denoted reserved are reserved for future use.

149.4.2.4.8 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x + 1)(x^{15} + x + 1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 149–29. In Figure 149–29 the 16 delay elements S0,..., S15, shall be initialized to zero. After initialization, the switch is set to CRCgen, as shown in Figure 149–29, and Oct4 through Oct10 are used to compute the CRC16 output. After all 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

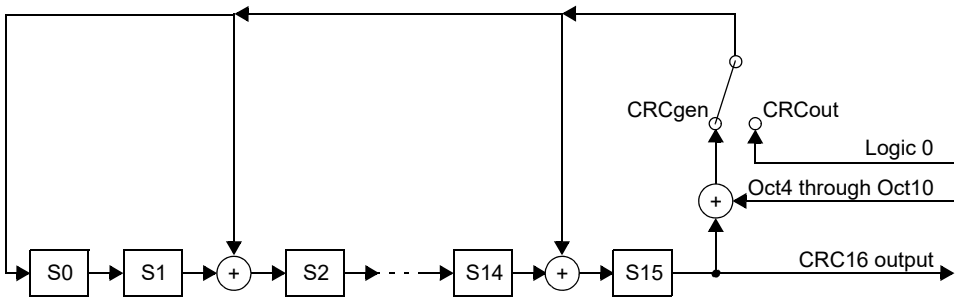

Figure 149–29—CRC16

149.4.2.4.9 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 149–13. Mapping of MDIO status variables to PMA status variables is shown in Table 149–14.

Table 149–13—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	PMA/PMD control 1 register/ MultiGBASE-T1 PMA control register	1.0.15 / 1.2309.15	pma_reset
Transmit disable	MultiGBASE-T1 PMA control register	1.2309.14	PMA_transmit_disable

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Table 149–14—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Receive fault	MultiGBASE-T1 PMA status register	1.2310.1	PMA_receive_fault

149.4.2.4.10 Startup sequence

The startup sequence shall comply with the state diagram description given in Figure 149–32. If the Auto-Negotiation function is not implemented, or disabled (mr_autoneg_en = FALSE), PMA_CONFIG is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup. The Auto-Negotiation function is optional for 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs. If the Auto-Negotiation function is implemented and enabled, Auto-Negotiation is the source of control (via link_control) and MASTER/SLAVE configuration; however, if Auto-Negotiation is either not enabled or is not implemented, the Link Synchronization function is the source of control (via sync_link_control) and MASTER/SLAVE configuration.

During startup, prior to entering the TRAINING state, the SLAVE shall align its transmit 65B RS-FEC frame to within +0/–4 × *S* (See Table 149–1 for the definition of *S*.) partial PHY frames of the MASTER as seen at the SLAVE MDI. The SLAVE Infofield partial PHY frame count shall match the MASTER Infofield partial PHY frame count for the aligned frame.

In the TRAINING state, PAM 2 transmission is used and PHY capabilities are exchanged with Infofields as specified in 149.4.2.4.5.

At any time following the TRAINING state, if the local receiver status (indicated by loc_rcvr_status) transitions to NOT_OK, PHY Control returns to the SILENT state and attempts a retrain.

The startup timing shall comply with Table 149–15 for MASTER and Table 149–16 for SLAVE.

NOTE—See Table 149–1 for the definition of S.

Table 149–15—Startup timing maximums for MASTER

Timing interval	Maximum time (ms)
From entry to SILENT state until en_slave_tx = 1 is transmitted	40 – 0.384 / *S*
From entry of SILENT state until entry to COUNTDOWN state	95.975 – 0.384 / *S*
Entry to COUNTDOWN until entry of TX_SWITCH	0.384 / *S*
Entry to exit of PCS TEST	1.025
Total (Entry to SILENT to exit of PCS TEST)	97

149.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel causes the PMA to set link_status to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the Auto-Negotiation (if enabled) or Link Synchronization (if Auto-Negotiation is not enabled) process.

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Table 149–16—Startup timing maximums for SLAVE

Timing interval	Maximum time (ms)
Entry to exit of SILENT state	40
Entry of SILENT state to exit of TRAINING state	95.975 – 0.384 / *S*
Entry to COUNTDOWN until entry of TX_SWITCH	0.384 / *S*
Entry to exit of PCS TEST	1.025
Total (Entry to SILENT to exit of PCS TEST)	97

The Link Monitor function shall comply with the state diagram of Figure 149–33.

Upon power on, reset, or release from power down, the Auto-Negotiation function sets link_control = DISABLE, or PHY Link Synchronization algorithms set sync_link_control = DISABLE. During this period, link_status = FAIL is asserted. When the Auto-Negotiation function establishes the presence of a remote MultiGBASE-T1 PHY, link_control is set to ENABLE, or when the PHY Link Synchronization finishes the synchronization function, sync_link_control is set to ENABLE, and the Link Monitor state diagram begins monitoring the PCS and receiver lock status. As soon as reliable transmission is achieved, the variable link_status = OK is asserted, upon which further PHY operations can take place.

149.4.2.6 PHY Link Synchronization

If the optional Clause 98 Auto-Negotiation function is disabled or not implemented, then the Link Synchronization function shall establish the start of PHY PMA training as defined in 149.4.2.4.

When operating, the Link Synchronization function is the data source for the PMA Transmit function (see 149.4.2.2), and uses a signal, SEND_S. This signal is used by the MASTER and SLAVE to discover the link partner and synchronize the start of PMA training.

The frequency of the SEND_S signal shall be 703.125 MHz.

Link Synchronization employs the SEND_S signal to achieve synchronization prior to link training. If the PHY is configured as MASTER, Link Synchronization shall employ Equation (149–10) as the PN sequence generator.

$$p_M(x) = x^8 + x^4 + x^3 + x^2 + 1 \quad (149–10)$$

If the PHY is configured as SLAVE, Link Synchronization shall employ Equation (149–11) as PN sequence generator.

$$p_{MS}(x) = x^8 + x^6 + x^5 + x^4 + 1 \quad (149–11)$$

The period of both PN sequences is 255.

An implementation of MASTER and SLAVE PHY SEND_S PN sequence generators by linear-feedback shift registers is shown in Figure 149–30. The bits stored in the shift register delay line at time *n* are denoted by $S_n[7:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $S_n[0]$ is generated. The PN sequence generator shift registers shall be reset to a value of $S_n[7:0]$ = 0000 0001 upon entering into the TRANSMIT_DISABLE state (see Figure 149–30) or on the transmission of the first

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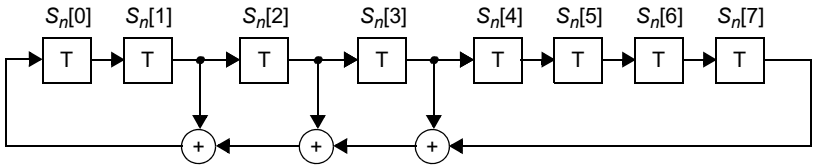
symbol of the alert sequence. The receiver may not necessarily receive a continuous PN sequence between separate periods of the SEND_S signal.

For 10GBASE-T1, the bit $S_n[0]$ shall be mapped to the transmit symbol T_n as follows: if $S_n[0] = 0$ then $T_n = +1\ +1\ +1\ +1\ +1\ +1\ +1\ +1$, if $S_n[0] = 1$ then $T_n = -1\ -1\ -1\ -1\ -1\ -1\ -1\ -1$.

For 5GBASE-T1, the bit $S_n[0]$ shall be mapped to the transmit symbol T_n as follows: if $S_n[0] = 0$ then $T_n = +1\ +1\ +1\ +1$, if $S_n[0] = 1$ then $T_n = -1\ -1\ -1\ -1$.

For 2.5GBASE-T1, the bit $S_n[0]$ shall be mapped to the transmit symbol T_n as follows: if $S_n[0] = 0$ then $T_n = +1\ +1$, if $S_n[0] = 1$ then $T_n = -1\ -1$.

MASTER PHY SEND_S PN sequence generator



SLAVE PHY SEND_S PN sequence generator

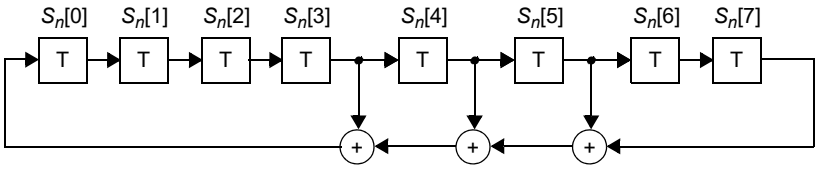


Figure 149–30—SEND_S PN sequence generator by linear feedback shift registers S_n

The PHY Link Synchronization state diagram in Figure 149–31 shall be used to synchronize 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 PHYs prior to the MultiGBASE-T1 link training. If the Clause 98 Auto-Negotiation function is enabled, then the Auto-Negotiation function shall be used as the mechanism for PHY synchronization and the PHY Link Synchronization state diagram in Figure 149–31 remains in the SYNC_DISABLE state.

149.4.2.6.1 State diagram variables

force_config

This variable indicates whether the PHY operates as a MASTER or as a SLAVE. The variable takes on one of the following values:

MASTER: This value is continuously asserted when the PHY operates as a MASTER.
SLAVE: This value is continuously asserted when the PHY operates as a SLAVE.

force_phy_type

This variable indicates what speed the PHY is to operate when Auto-Negotiation is disabled or not implemented. The variable takes on one of the following values:

10G-T1: If Auto-Negotiation is disabled or not implemented and 10GBASE-T1 is selected.
5G-T1: If Auto-Negotiation is disabled or not implemented and 5GBASE-T1 is selected.
2.5G-T1: If Auto-Negotiation is disabled or not implemented and 2.5GBASE-T1 is selected.

Other values are implementation-dependent and beyond the scope of this clause.

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link_status
: The link_status parameter is set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_autoneg_enable:
: see 98.5.1.

mr_main_reset
: see 98.5.1.

power_on
: see 98.5.1.

send_s_sigdet
: This variable indicates whether the SEND_S signal was detected. This variable shall be set FALSE no later than 1 μs after the signal goes quiet on the MDI.
Values:
TRUE: SEND_S signal detected.
FALSE: SEND_S signal not detected.

sync_link_control
: This variable indicates the data source for the PMA Transmit function.
Values:
DISABLE: The data source is the PHY Link Synchronization function (sync_tx_symb).
ENABLE: The data source is PMA_UNITDATA.request (tx_symb).

149.4.2.6.2 State diagram timers

break_link_timer
: see 98.5.2.

link_fail_inhibit_timer
: see 98.5.2.

send_s_timer
: This timer is used to control the duration SEND_S is transmitted. The timer shall expire 1.25 μs ± 0.05 μs after being started.

sigdet_wait_timer
: This timer is used to control the wait time after transmitting or detecting the end of SEND_S. The timer shall expire 5 μs ± 0.15 μs after being started.

149.4.2.6.3 Messages

sync_tx_symb
: The value of sync_tx_symb is set by the Link Synchronization state diagram and indicates the symbols sent from the PHY Link Synchronization block to PMA Transmit. The Link Synchronization block generates sync_tx_symb synchronously with every transmit clock cycle.
Values:
SEND_S: Transmit the SEND_S signal defined in 149.4.2.6.
SEND_Z: Transmit a zero value.

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149.4.2.6.4 State diagrams

The PHY Link Synchronization state diagram is shown in Figure 149–31.

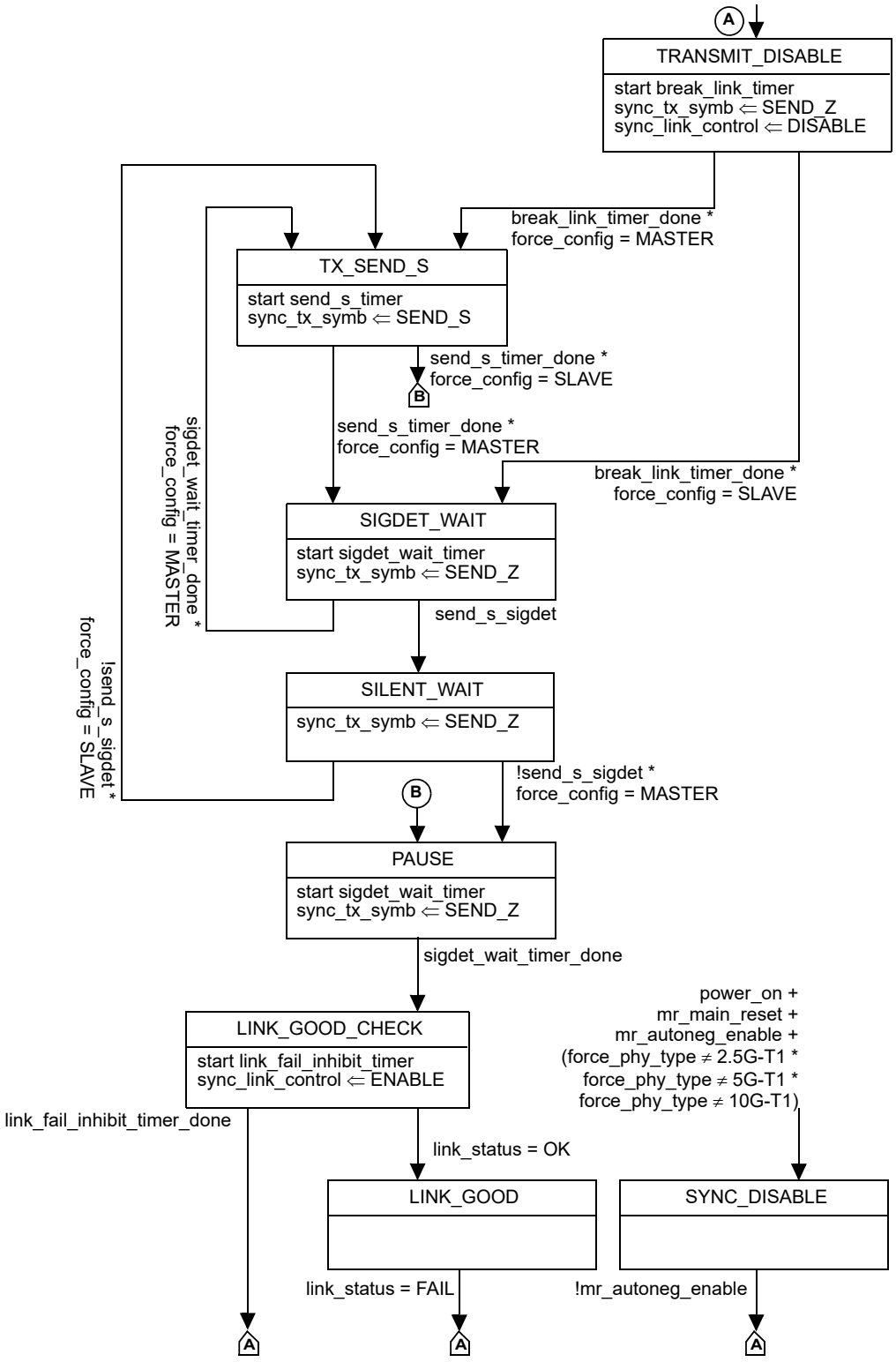

Figure 149–31—PHY Link Synchronization state diagram

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149.4.2.7 Refresh monitor function

The Refresh monitor is required for PHYs that support the EEE capability. The Refresh monitor operates when the PHY is in the LPI receive mode. The Refresh monitor shall comply with the state diagram of Figure 149–34. The Refresh monitor sets the PMA_refresh_status variable, which forces a link retrain if a refresh signal is not reliably detected within a moving time window equivalent to 50 complete quiet-refresh cycles (nominally equal to 1.536/*S* ms), when the PHY is in the lower power receive mode. See Table 149–1 for the definition of *S*.

149.4.2.8 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RFER indicated in 149.4.2.3 is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by received_clock.

149.4.3 MDI

Communication through the MDI is summarized in 149.4.3.1 and 149.4.3.2.

149.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA are denoted by tx_symb. PMA Transmit generates a pulse-amplitude modulated signal on each pair in the following form:

$$s(t) = \sum_{n=0}^{\infty} a_n h_T(t - nT) \quad (149–12)$$

In Equation (149–12), a_n is the PAM4 modulation symbol from the set {–1, –1/3, +1/3, +1} to be transmitted at time nT, and $h_T(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 149.5.2.

149.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed as pulse-amplitude modulated signals that are corrupted by noise as follows:

$$r(t) = \sum_{n=0}^{\infty} a_n h_R(t - nT) + w(t) \quad (149–13)$$

In Equation (149–13) $h_R(t)$ denotes the symbol response of the overall channel impulse response between the transmit symbol source and the receive MDI and $w(t)$ represents the contribution of various noise sources including uncancelled echo. The receive signal is processed within the PMA Receive function to yield the received symbols rx_symb.

149.4.4 State variables

149.4.4.1 State diagram variables

auto_neg_imp
: This variable indicates if an optional Auto-Negotiation sublayer is associated with the PMA.
Values:
TRUE: An optional Auto-Negotiation sublayer is associated with the PMA.
FALSE: An optional Auto-Negotiation sublayer is not associated with the PMA.

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config

The PMA generates this variable continuously and passes it to the PCS via the PMA_CONFIG.indication primitive.
Values: MASTER or SLAVE.

en_slave_tx

The en_slave_tx variable in the Infofield received by the SLAVE.
Values:

0: MASTER is not ready for the SLAVE to transmit.
1: MASTER is ready for the SLAVE to transmit.

infofield_complete

This variable indicates that a complete set of Infofield messages has been sent (see 149.4.2.4).
Values:

FALSE: A complete set of Infofield messages has not been sent.
TRUE: A complete set of Infofield messages has been sent.

link_control

This variable is defined in 149.2.1.1.1.

link_status

The link_status parameter set by PMA Link Monitor state diagram and communicated through the PMA_LINK.indication primitive.
Values: OK or FAIL.

loc_countdown_done

This variable is set to FALSE when the PHY Control state diagram is in the DISABLE_TRANSMITTER state and is set to TRUE immediately after transmitting the last bit of the DataSwPFC24–1 partial PHY frame.

loc_rcvr_status

Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY.
Values:

OK: The receive link for the local PHY is operating reliably.
NOT_OK: Operation of the receive link for the local PHY is unreliable.

loc_SNR_margin

This variable reports whether the local device has sufficient SNR margin to continue to the next state. The criterion for setting the parameter loc_SNR_margin is left to the implementer.
Values:

OK: The local device has sufficient SNR margin.
NOT_OK: The local device does not have sufficient SNR margin.

pcs_data_mode

Generated by the PMA PHY Control function and indicates whether or not the local PHY may transition its PCS state diagrams out of their initialization states. The current value of the pcs_data_mode is passed to the PCS via the PMA_PCSDATAMODE.indication primitive.

PMA_refresh_status

This variable indicates the status of the Refresh monitor as described in 149.4.2.7.
Values: OK or FAIL.

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pma_reset
: Allows reset of the PHY Control and Link Monitor state diagrams.
Values: ON or OFF.

PMA_state
: Variable for the value transmitted in the PMA_state<7:6> of the Infofield by the local PHY.
Values:
00: TRAINING state
01: COUNTDOWN state

rem_countdown_done
: This variable is set to FALSE when the PHY Control state diagram is in the DISABLE_TRANSMITTER state or SILENT state and is set to TRUE once the receiver has transitioned from PAM2 to PAM4.

rem_rcvr_status
: Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not.
Values:
OK: The receive link for the remote PHY is operating reliably.
NOT_OK: Reliable operation of the receive link for the remote PHY is not detected.

sync_link_control
: This variable is defined in 149.4.2.6.1.

tx_mode
: The PMA generates this variable continuously and passes it to the PCS via the PMA_TXMODE.indication primitive.
Values:
SEND_N: This value is continuously asserted when transmission of sequences of symbols representing a XGMII data stream take place.
SEND_T: This value is continuously asserted when transmission of sequences of symbols representing the training sequences of symbols is to take place.
SEND_Z: This value is asserted when transmission of zero symbols is to take place.

149.4.4.2 Timers

All timers operate in the manner described in 14.2.3.2.

minwait_timer
: A timer used to determine the minimum amount of time the PHY Control stays in the SILENT, TRAINING, PCS_TEST, and PCS_DATA states. The timer shall expire 975 μs ± 50 μs after being started.

The following timer is required only for PHYs that support the EEE capability:

lpi_refresh_rx_timer
: This timer is used to monitor link quality during the LPI receive mode. If the PHY does not detect reliable refresh signaling before this timer expires then a full retrain is performed.
Values: The condition lpi_refresh_rx_timer_done becomes TRUE upon timer expiration.
Duration: This timer shall have a period equal to 50 complete quiet-refresh signal periods, equivalent to 1.536/*S* ms. See Table 149–1 for the definition of *S*.

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149.4.5 State diagrams

The PHY Control state diagram is shown in Figure 149–32, the Link Monitor state diagram is shown in Figure 149–33, and the EEE Refresh monitor state diagram is shown in Figure 149–34.

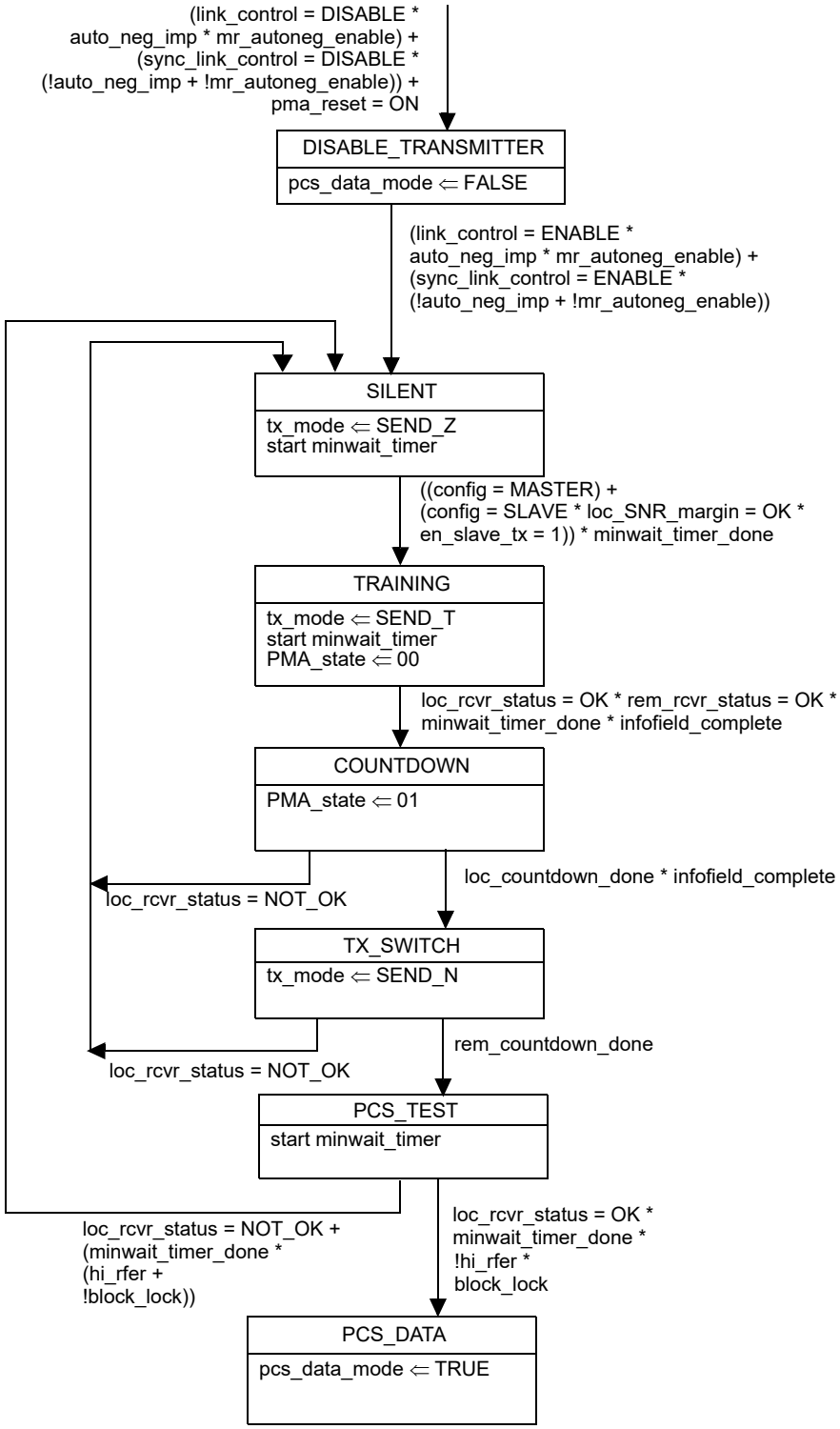

Figure 149–32—PHY Control state diagram

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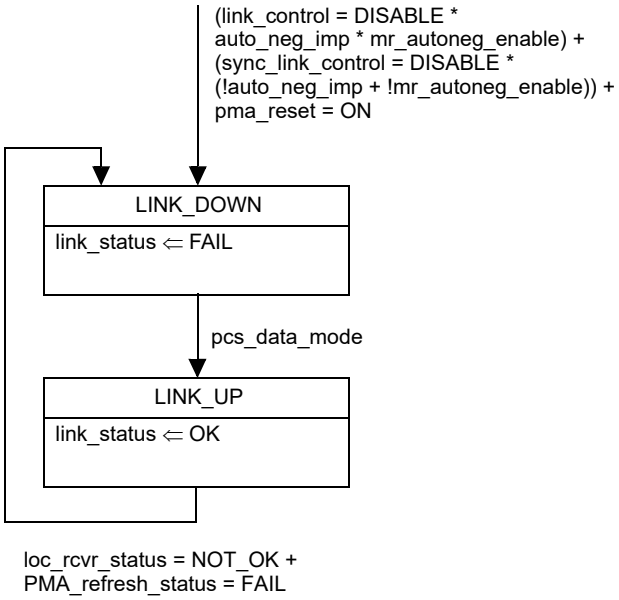
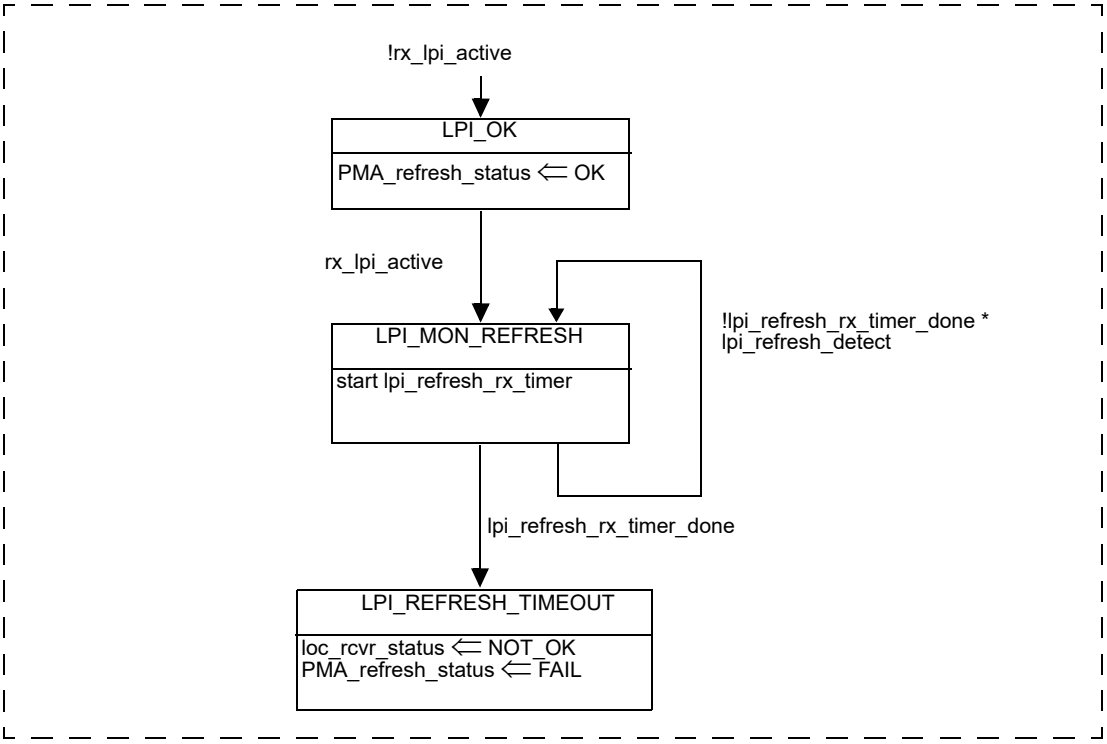


NOTE—The variables link_control and link_status are designated as link_control_mGigT1 and link_status_mGigT1, respectively, by the Auto-Negotiation Arbitration state diagram (Figure 98–7) if the optional Auto-Negotiation function is implemented.

Figure 149–33—Link Monitor state diagram



NOTE—This state diagram is only required when the PHY supports the EEE capability.

Figure 149–34—EEE Refresh monitor state diagram

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149.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

149.5.1 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.

If MDIO is implemented, these test modes shall be enabled by setting a control register, 1.2313.15:13, as shown in Table 149–17. If MDIO is not implemented then equivalent functionality shall be provided. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

Table 149–17—MDIO management registers settings for test modes

Register value	Register description
000	Normal (non-test mode) operation.
001	Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in linked mode.
010	Test mode 2—Transmit MDI jitter test in MASTER mode.
011	Test mode 3—Precoder test mode.
100	Test mode 4—Transmitter linearity test.
101	Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
110	Test mode 6—Transmitter droop test mode.
111	Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Test mode 1 enables testing of timing jitter on MASTER and SLAVE transmitters. MASTER and SLAVE PHYs are connected over a link segment defined in 149.7. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_175. TX_TCLK_175 is equal to 175.78125 MHz.

Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in MASTER timing mode. When test mode 2 is enabled, the PHY shall transmit a continuous pattern of JP03A (as specified in 94.2.9.1) or JP03B (as specified in 94.2.9.2) with the transmitted symbols timed from its local clock source.

Test mode 3 is for testing the precoder operation. When test mode 3 is enabled, the PCS shall generate a continuous pattern of {0, 3} symbols to be input to the transmit precoder specified in 149.3.2.2.20, to be precoded according to the transmit precoder settings as determined by the value set in register 1.2313:10:9, or equivalent functionality if MDIO is not implemented, and transmitted by the PMA timed from its local clock source.

Test mode 4 is for transmitter linearity testing. When test mode 4 is enabled, the PHY shall transmit a continuous pattern of PRBS13Q (as specified in 120.5.11.2.1).

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Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit as in non-test operation and in the MASTER data mode with data set to normal interframe idle signals.

When test mode 6 is enabled, the PHY shall transmit a continuous pattern of 128 × *S* {+1} symbols followed by 128 × *S* {–1} symbols with the transmitted symbols timed from its local clock source. See Table 149–1 for the definition of *S*.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder/decoder, transmit and receive analog front ends of the PHY, and a cable connecting two PHYs. This mode reuses the 2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1 normal (non-test) mode with zero data pattern. Instead of encoding data received from the MAC, continuous zero data pattern is encoded. On the receive side, after PCS FEC decoding processing, a zero data sequence is expected with no errors. Any block received with non-zero data bits is counted as an error and calculated in the RS-FEC block error ratio.

149.5.1.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 149–35, Figure 149–36, Figure 149–37, and Figure 149–38, in stated respective tests, are defined for measuring the transmitter specifications for data communication only.

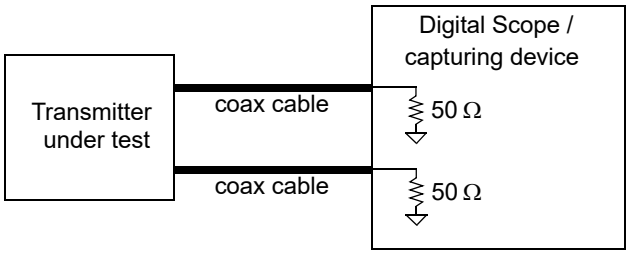

Figure 149–35—Transmitter test fixture 1 for transmitter droop measurement and transmitter linearity measurement

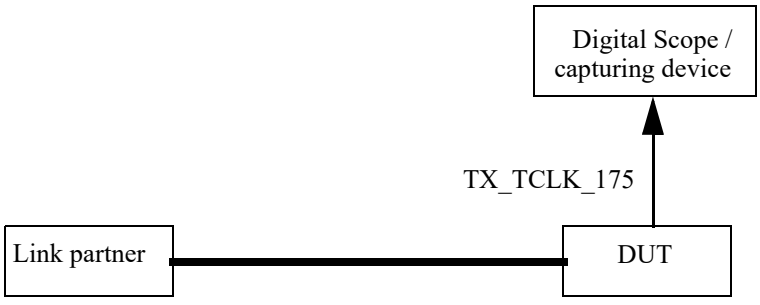

Figure 149–36—Transmitter test fixture 2 for MASTER and SLAVE clock jitter measurement

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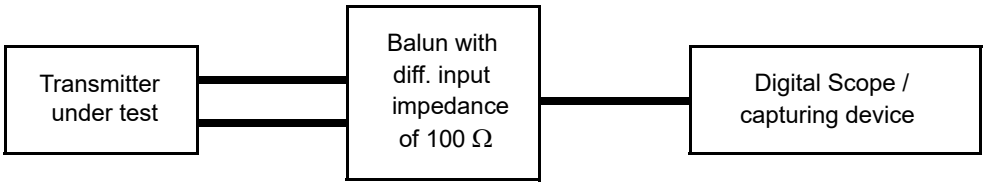

Figure 149–37—Transmitter test fixture 3 for MDI jitter measurement

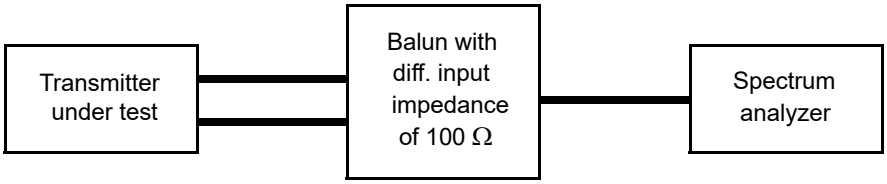

Figure 149–38—Transmitter test fixture 4 for power spectral density measurement and transmit power level measurement

149.5.2 Transmitter electrical specifications

The PMA provides the Transmit function specified in 149.4.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be AC-coupled, i.e., it shall present a high DC common-mode impedance at the MDI. There may be various methods for AC-coupling in actual implementations.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output. Transmitter electrical tests are specified with a load tolerance of ± 0.1%.

149.5.2.1 Maximum output droop

With the transmitter in test mode 6 and using the transmitter test fixture 1 shown in Figure 149–35, the magnitude of both the positive and negative droop shall be less than 15%, measured with respect to an initial value at 4 ns after the zero crossing and a final value at 16 ns after the zero crossing (12 ns period).

149.5.2.2 Transmitter linearity

With the transmitter in test mode 4 and using the transmitter test fixture 1 shown in Figure 149–35, the test defined in 120D.3.1.2 shall be performed. The ideal PAM4 level of 1/3 should be used for effective symbol levels of ES1 and ES2. The transmitter SNDR distortion, as specified in 120D.3.1.6, shall exceed 38 dB in 10GBASE-T1, 36 dB in 5GBASE-T1, and 35 dB in 2.5G modes.

149.5.2.3 Transmitter timing jitter

The transmitter timing jitter is measured by capturing the TX_TCLK_175 waveform in both MASTER and SLAVE configurations while in test mode 1 using the transmitter test fixture 2 shown in Figure 149–36.

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When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the MASTER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 1/*S* ps. The peak-to-peak value of the MASTER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 10/*S* ps. See Table 149–1 for the definition of *S*.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the SLAVE TX_TCLK_175 jitter relative to an unjittered reference shall be less than 2/*S* ps. The peak-to-peak value of the SLAVE TX_TCLK_175 jitter relative to an unjittered reference shall be less than 20/*S* ps.

TX_TCLK_175 jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the capturing device shall be at least 200 MHz (this is equivalent to phase noise integration of the clock over a bandwidth of at least 100 MHz from the carrier frequency). The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK_175. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

149.5.2.3.1 Transmit MDI random jitter in MASTER mode

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 with the square wave pattern (see Table 149–18) and using test fixture 3 as shown in Figure 149–37. The RMS value of the MDI output jitter relative to an unjittered reference shall be less than 1/*S* ps. The peak-to-peak value of the MDI output jitter relative to an unjittered reference shall be less than 10/*S* ps. Jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the measurement device shall be larger than 200 MHz. The unjittered reference is a constant clock frequency extracted from each record of captured differential output on MDI. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

Table 149–18—Jitter test modes

Bit 1.2313.1	Bit 1.2313.0	Test pattern
0	0	Square wave: TX_TCLK_175
0	1	JP03A (as specified in 94.2.9.1)
1	0	JP03B (as specified in 94.2.9.2)
1	1	Reserved

149.5.2.3.2 Transmit MDI deterministic jitter in MASTER mode

Jitter measurements in this subclause are performed with the transmitter enabled in MASTER timing mode in test mode 2, with the patterns as defined by Table 149–18, and timed with a local clock.

To measure the peak-to-peak deterministic jitter ($DJ_{pk\text{-}pk}$) follow the steps as specified in 94.3.12.6.1, with the following modifications to step 5:

$f_n = 1 \times S$ MHz, $T = 68 / S$ ns.

Using this method, $DJ_{pk\text{-}pk}$ shall be less than 9 / *S* ps.

To measure peak-to-peak even-odd jitter ($EOJ_{pk\text{-}pk}$) follow the steps as specified in 94.3.12.6.2.

Using this method, $EOJ_{pk\text{-}pk}$ shall be less than 4 / *S* ps. See Table 149–1 for the definition of *S*.

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149.5.2.4 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation), the transmit power shall be in the range of –1 dBm to 2 dBm and the power spectral density of the transmitter, measured into a 100 Ω load using test fixture 4 shown in Figure 149–38 shall be between the upper and lower masks specified in Equation (149–14) and Equation (149–15). The upper and lower masks for each data rate, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s, are shown in Figure 149–39. See Table 149–1 for the definition of *S*.

$$UPSD(f) = \begin{cases} -90 - K & \text{dBm/Hz} \quad 0 < f \le 600 \times S \\ -89 - K - \dfrac{f}{600 \times S} & \text{dBm/Hz} \quad 600 \times S < f \le 3000 \times S \\ -82 - K - \dfrac{f}{250 \times S} & \text{dBm/Hz} \quad 3000 \times S < f \le 5500 \times S \end{cases} \tag{149–14}$$

$$LPSD(f) = \begin{cases} -96 - K & \text{dBm/Hz} \quad 5 < f \le 400 \times S \\ -95 - K - \dfrac{f}{400 \times S} & \text{dBm/Hz} \quad 400 \times S < f \le 2000 \times S \\ -90 - K - \dfrac{f}{200 \times S} & \text{dBm/Hz} \quad 2000 \times S < f \le 3000 \times S \end{cases} \tag{149–15}$$

where

f is the frequency in MHz

$$K = 10\log_{10}(S) \tag{149–16}$$

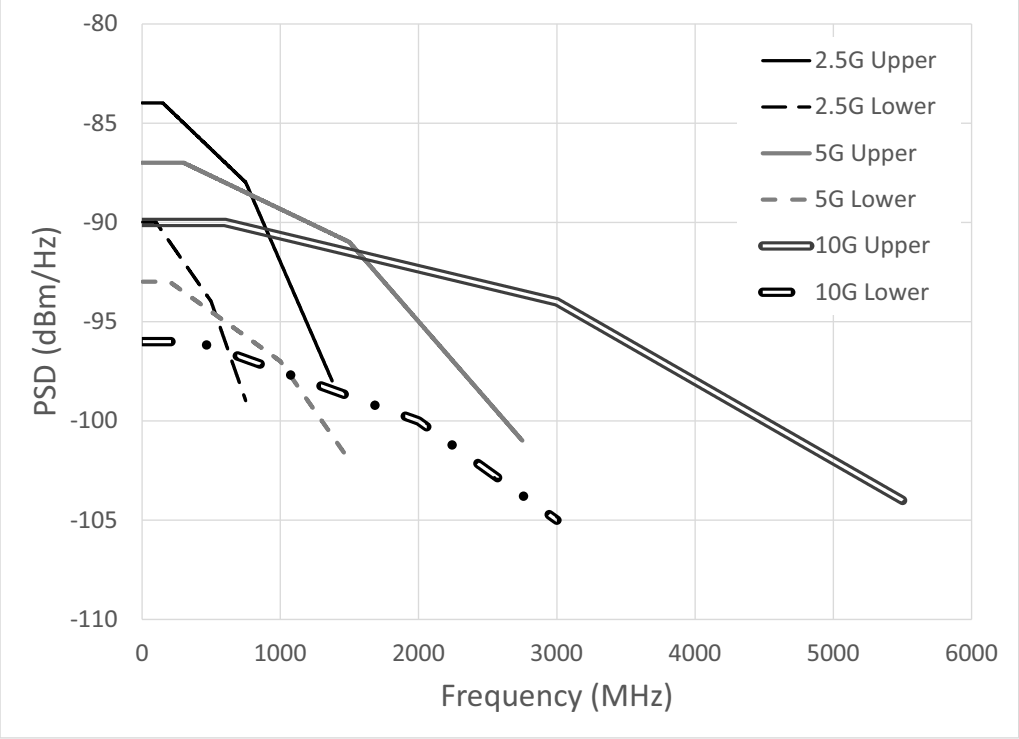

Figure 149–39—Transmitter power spectral density, upper and lower masks

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149.5.2.5 Transmitter peak differential output

When measured with 100 Ω termination, the transmit differential signal at the MDI shall be less than 1.3 V peak-to-peak. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

149.5.2.6 Transmitter clock frequency

The symbol transmission rate of the MASTER PHY shall be within the range $5625 \times S$ MHz ± 50 ppm. See Table 149–1 for the definition of *S*.

For a MASTER PHY, when the transmitter is in the LPI transmit mode, the transmitter clock short-term rate of frequency variation shall be less than 0.1 ppm/second. The short-term frequency variation limit shall also apply when switching to and from the LPI mode.

149.5.3 Receiver electrical specifications

The PMA provides the Receive function specified in 149.4.2.3 in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 149.7.

149.5.3.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 149.5.2 and have passed through a link specified in 149.7 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link reset completion. This specification can be verified by a frame error ratio less than 7.8×10^{-9} for 800 octet frames with minimum IPG or greater than 220-octet IPG.

149.5.3.2 Alien crosstalk noise rejection

This specification is provided to verify the receiver's tolerance to alien crosstalk noise. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidths, and magnitudes shown in Table 149–19. The receive DUT is connected to the noise source through a directional coupler, as shown in Figure 149–40, with a link segment as defined in 149.7. The BER is expected to be less than 10^{-12}, and to satisfy this specification the frame loss ratio is less than 10^{-9} for 125-octet packets measured at the MAC/PLS service interface.

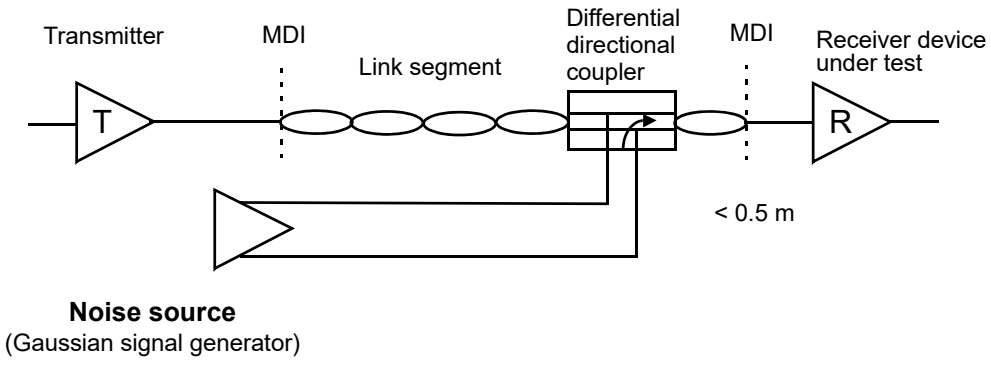

Figure 149–40—Alien crosstalk noise rejection test setup

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Table 149–19—Alien crosstalk noise source

PHY type	Noise bandwidth (MHz)	Added noise at MDI (dBm/Hz)
10GBASE-T1	3500	–152
5GBASE-T1	1750	–149
2.5GBASE-T1	875	–146

149.6 Management interface

2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 make extensive use of the management functions that may be provided by the optional MDIO (Clause 45), and the communication and self-configuration functions provided by the optional Auto-Negotiation (Clause 98).

149.6.1 Optional Support for Auto-Negotiation

If Auto-Negotiation is supported and enabled the mechanism described in Clause 98 shall be used.

Auto-Negotiation is performed as part of the initial setup of the link, and allows the PHYs at each end to advertise their capabilities and to automatically select the operating mode for communication on the link. Auto-Negotiation signaling is used for the following primary purposes for 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1:

a) To negotiate that the PHY is capable of supporting 2.5GBASE-T1 transmission.
b) To negotiate that the PHY is capable of supporting 5GBASE-T1 transmission.
c) To negotiate that the PHY is capable of supporting 10GBASE-T1 transmission.
d) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.

149.7 Link segment characteristics

2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 are designed to operate over a single shielded balanced pair of conductors that meet the requirements specified in this subclause. The single shielded balanced pair of conductors supports an effective data rate of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s in each direction simultaneously. The term *link segment* used in this clause refers to a single balanced pair of conductors (cable or backplane) operating in full duplex.

For the three different PHY types, link segment parameters are specified to different upper frequencies, given by the parameter F_{max} shown in Equation (149–17).

$$F_{max} = 4000 \times S \quad (149–17)$$

See Table 149–1 for the definition of *S*.

149.7.1 Link transmission parameters

The transmission characteristics for the MultiGBASE-T1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

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149.7.1.1 Insertion loss

The insertion loss of each MultiGBASE-T1 link segment shall meet the values determined using Equation (149–18).

$$Insertion\ loss(f) \le 0.002\,f + 0.68 f^{0.45} \quad \text{(dB)} \tag{149–18}$$

where

f is the frequency in MHz; $1 \le f \le F_{max}$

The insertion loss is illustrated in Figure 149–41.

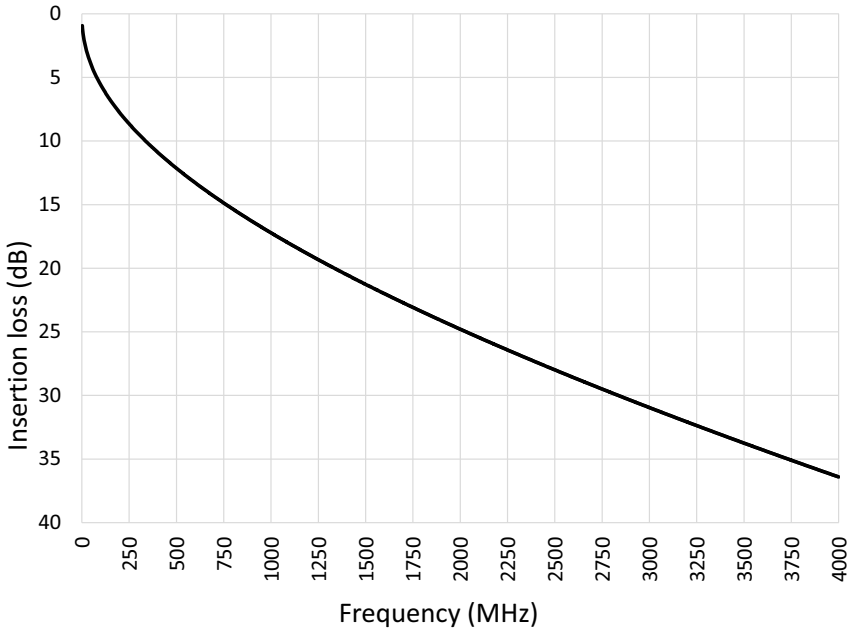

Figure 149–41—Insertion loss calculated using Equation (149–18)

149.7.1.2 Differential characteristic impedance

The nominal differential characteristic impedance of the link segment is 100 Ω.

149.7.1.3 Return loss

149.7.1.3.1 2.5GBASE-T1 link segment return loss

In order to limit the noise at the receiver due to impedance mismatches each 2.5GBASE-T1 link segment shall meet the values determined by using Equation (149–19) at all frequencies from 1 MHz to 1000 MHz. The reference impedance for the return loss specification is 100 Ω.

$$2.5G\_Return\_Loss \ge \left\{ \begin{array}{ll} 20 & 1 \le f < 240 \\ 20 - 10\log_{10}(f/240) & 240 \le f \le 1000 \end{array} \right\} \text{(dB)} \tag{149–19}$$

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where

f is the frequency in MHz; $1 \le f \le 1000$

The 2.5GBASE-T1 return loss is illustrated in Figure 149–42.

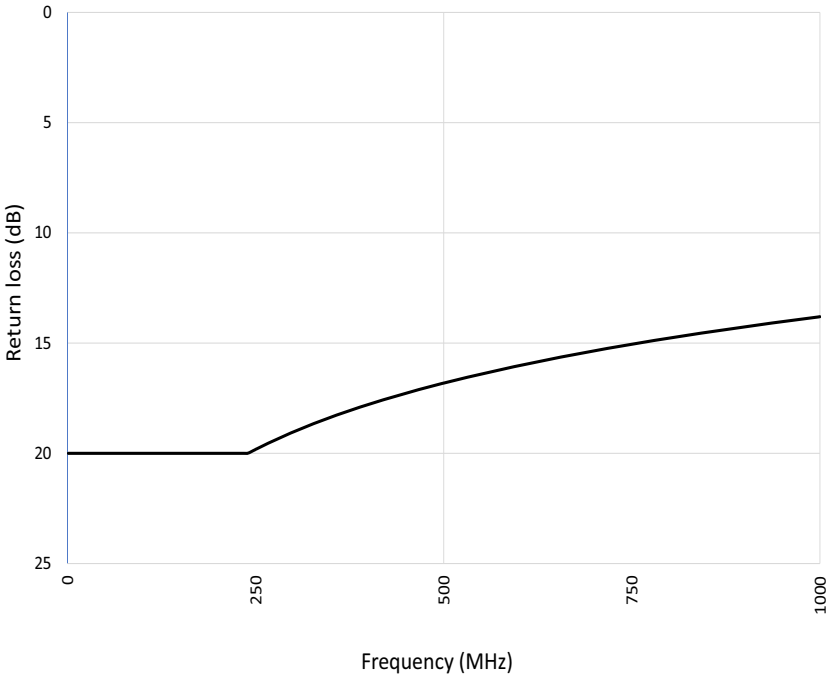

Figure 149–42—Return loss calculated using Equation (149–19)

149.7.1.3.2 5GBASE-T1 link segment return loss

In order to limit the noise at the receiver due to impedance mismatches each 5GBASE-T1 link segment shall meet the values determined by using Equation (149–20) at all frequencies from 1 MHz to 2000 MHz. The reference impedance for the return loss specification is 100 Ω. The return loss is dependent on the insertion loss at 1.5 GHz as determined by using Equation (149–21) to calculate *N*.

$$5G\_Return\_Loss \ge \left\{ \begin{array}{ll} 20 & 1 \le f < 480/2^N \\ 20 - 10\log_{10}((2^N \times f)/480) & 480/2^N \le f \le 2000 \end{array} \right\} \text{(dB)} \qquad (149\text{–}20)$$

where

f is the frequency in MHz; $1 \le f \le 2000$

$$N = \left\{ \begin{array}{ll} 0 & 15 \text{ dB} < IL\ (1.5\ GHz) \\ 1 & IL\ (1.5\ GHz) \le 15 \text{ dB} \end{array} \right. \qquad (149\text{–}21)$$

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The 5GBASE-T1 return loss is illustrated in Figure 149–43.

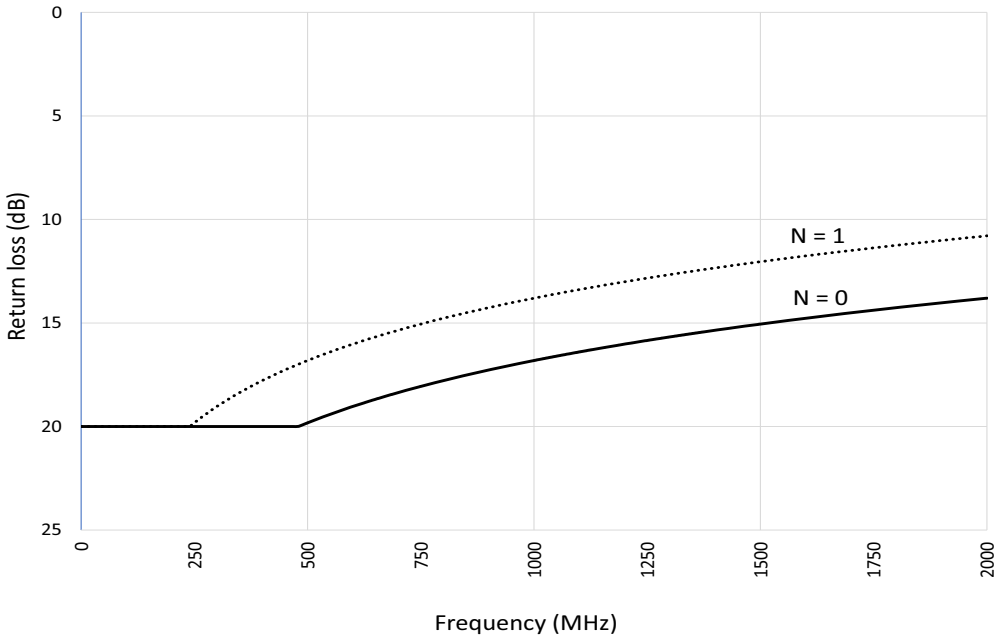

Figure 149–43—Return loss calculated using Equation (149–20) and Equation (149–21)

149.7.1.3.3 10GBASE-T1 link segment return loss

In order to limit the noise at the receiver due to impedance mismatches each 10GBASE-T1 link segment shall meet the values determined by using Equation (149–22) at all frequencies from 1 MHz to 4 GHz. The reference impedance for the return loss specification is 100 Ω. The return loss is dependent on the insertion loss at 3 GHz as determined by using Equation (149–23) to calculate *N*.

$$10G\_Return\_Loss \geq \left\{ \begin{array}{rl} 20 & 1 \leq f < 480/2^N \\ 20 - 10\log_{10}((2^N \times f)/480) & 480/2^N \leq f < 3000 \\ 12 - 3N & 3000 \leq f \leq 4000 \end{array} \right\} \text{(dB)} \qquad (149\text{–}22)$$

where

f is the frequency in MHz; $1 \leq f \leq 4000$

$$N = \left\{ \begin{array}{ll} 0 & 15 \text{ dB} < IL\ (3\ GHz) \\ 1 & IL\ (3\ GHz) \leq 15 \text{ dB} \end{array} \right. \qquad (149\text{–}23)$$

The 10GBASE-T1 return loss is illustrated in Figure 149–44.

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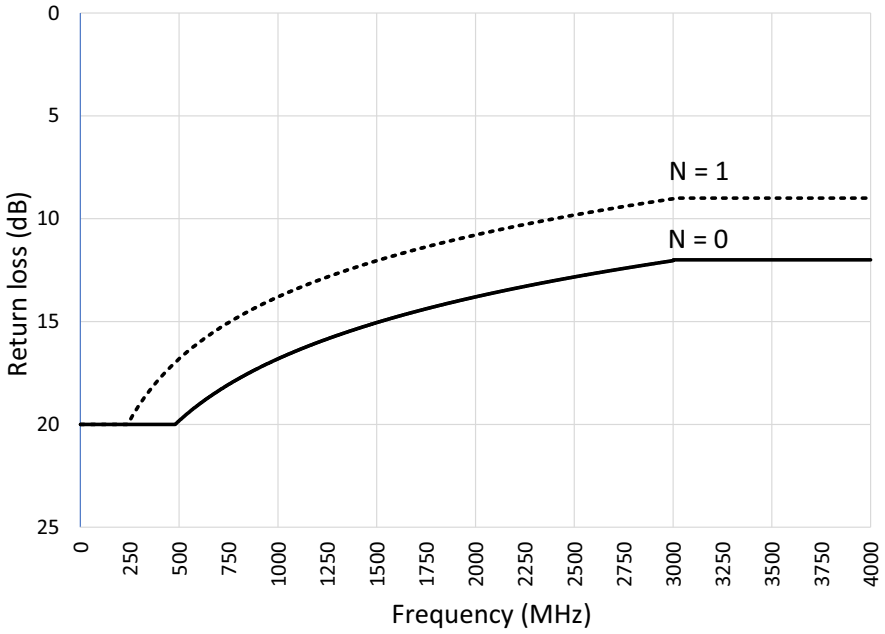

Figure 149–44—Return loss calculated using Equation (149–22) and Equation (149–23)

149.7.1.4 Coupling attenuation

In order to limit the noise at the receiver as well as emissions, when tested using the IEC 62153-4-7 triaxial tube in tube method as specified in Annex 149A, where shielded balanced pair cabling is used, the MultiGBASE-T1 link segment shall meet the coupling attenuation values determined by using Equation (149–24).

$$Coupling\ Attenuation(f) \geq \left\{ \begin{array}{ll} 70 & 30 \leq f < 750\ \text{MHz} \\ 50 - 20\log_{10}\left(\frac{f}{7500}\right) & 750 \leq f \leq 4000\ \text{MHz} \end{array} \right\} \text{(dB)} \qquad (149–24)$$

where

f is the frequency in MHz; $30 \leq f \leq 4000$

The coupling attenuation is illustrated in Figure 149–45.

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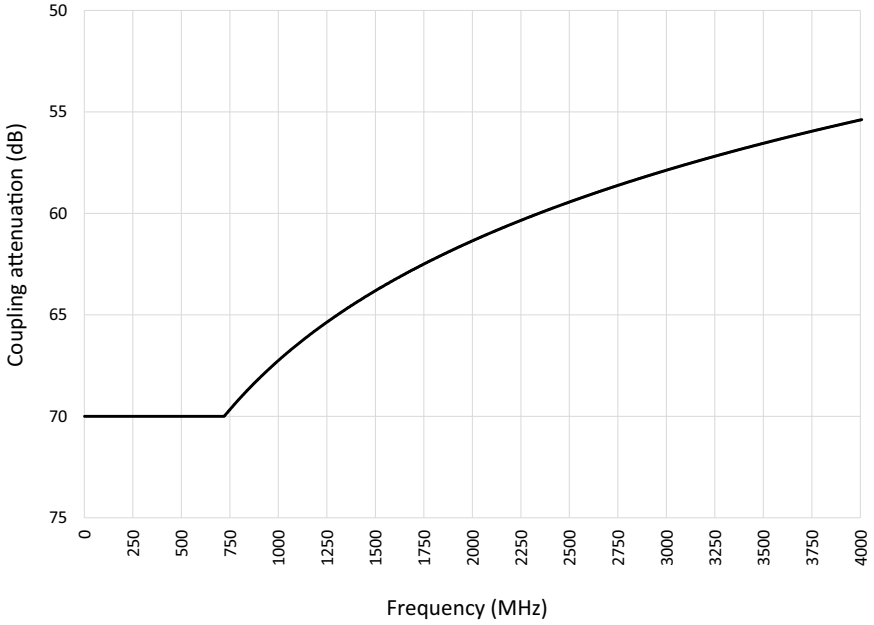

Figure 149–45—Coupling attenuation calculated using Equation (149–24)

149.7.1.5 Screening attenuation

Where shielded balanced pair cabling is used, the minimum screening attenuation for a link segment is 45 dB for all frequencies between 30 MHz and F_{max} MHz. Screening attenuation is tested as specified in IEC 62153-4-7 using triaxial tube-in-tube method. Additional screening attenuation test methodologies are defined in Annex 149A.

149.7.1.6 Maximum link delay

The propagation delay of a link segment shall not exceed 94 ns at all frequencies between 2 MHz and F_{max} MHz.

149.7.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as *alien crosstalk noise*. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in Annex 97B.

For implementations with multiple MultiGBASE-T1 ports on the same MDI connector assembly, coupling between ports on the MDI connector is not considered to be part of the alien crosstalk specifications. For further information, see 149C.5.

149.7.2.1 Power sum alien near-end crosstalk (PSANEXT)

The differential pair-to-pair near-end crosstalk (NEXT) loss between the disturbed link segment and the disturbing link segment is specified to meet the bit error ratio objective by limiting the alien crosstalk at the near end of a link segment. Multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT disturbers. The power ANEXT loss is derived using Equation (97–25).

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The power sum ANEXT loss between a disturbed link segment and the disturbing link segment shall meet the values determined using Equation (149–25).

$$\text{PSANEXTloss}(f) \geq \min\left(75,\ 80 - 15\log_{10}\frac{f}{100}\right)\ \text{dB} \qquad (149\text{–}25)$$

where

f is the frequency in MHz; $1 \leq f \leq 4000$

PSANEXT is illustrated in Figure 149–46.

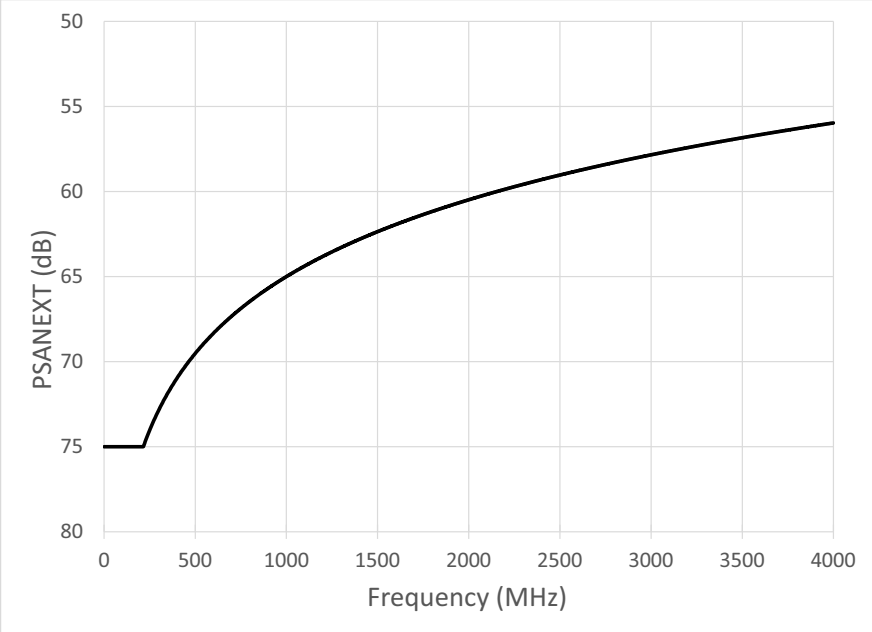

Figure 149–46—PSANEXT calculated using Equation (149–25)

149.7.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

In order to limit the alien crosstalk at the far-end of a link segment, the differential pair-to-pair alien far-end crosstalk (FEXT) loss between the disturbed link segment and the disturbing link segment is specified to meet the bit error ratio objective. Multiple disturber attenuation to crosstalk ratio far-end ACRF is specified as the power sum of the individual alien ACRF disturbers to limit the total alien FEXT coupled into a link segment. The power AACRF is derived using Equation (97–27).

The power sum AACRF between a disturbed link segment and the disturbing link segment shall meet the values determined using Equation (149–26).

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$$\text{PSAACRF}(f) \geq \min\left(75,\ 86 - 20\log_{10}\frac{f}{100}\right)\ \text{dB} \qquad (149\text{–}26)$$

where

f is the frequency in MHz; $1 \leq f \leq 4000$

PSAACRF is illustrated in Figure 149–47.

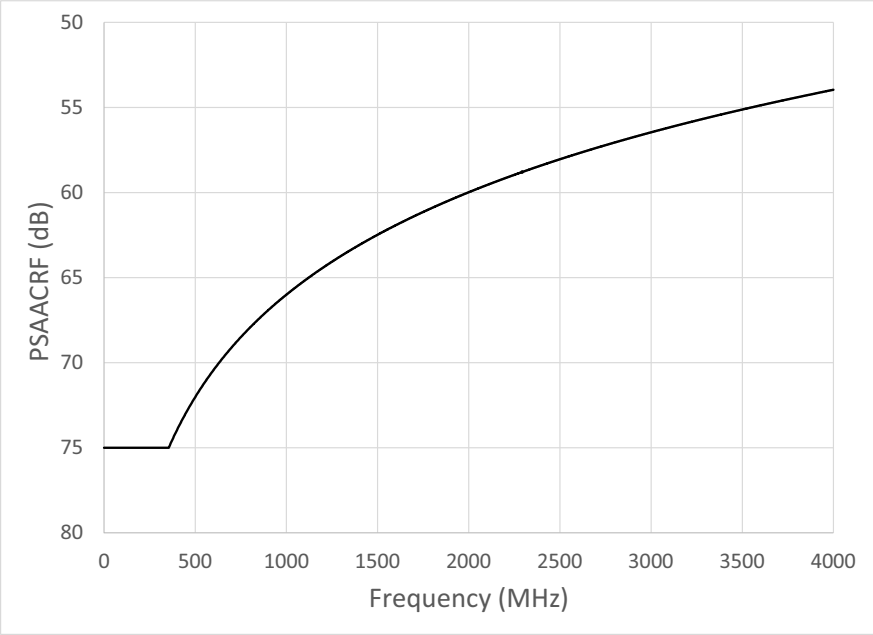

Figure 149–47—PSAACRF calculated using Equation (149–26)

149.8 MDI specification

149.8.1 MDI connectors

Where shielded balanced pair cabling is used, the mechanical interface to the shielded balanced cabling is a 2-pin connector with a shield. Further specification of the mechanical interface is beyond the scope of this standard.

149.8.2 MDI electrical specification

The electrical requirements specified in 149.5.2 and 149.5.3 shall be met when the PHY is connected to the MDI connector mated with a specified connector to a shielded balanced pair of conductors.

149.8.2.1 MDI return loss

The differential impedance at the MDI (see Figure 149–48) for each transmit/receive channel shall be such that any reflection (due to differential signals incident upon the MDI with a test port having a differential impedance of 100 Ω) is attenuated relative to the incident signal per Equation (149–27).

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$$MDI\_Return\_Loss(f) \leq \begin{cases} 20 - 20\left(\log_{10}\frac{10}{f}\right) & 1 \leq f < 10 \\ 20 & 10 \leq f < 280S \\ 20 - 10\log_{10}(f/(280S)) & 280S \leq f < 2800S \\ 10 - 16\log_{10}(f/(2800S)) & 2800S \leq f \leq F_{\max} \end{cases} \text{ (dB)} \quad (149\text{–}27)$$

where

f is the frequency in MHz.

For 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1, the maximum applicable frequency for the MDI return loss is 4000 × S MHz. See Table 149–1 for the definition of S.

The MDI return loss is illustrated in Figure 149–48.

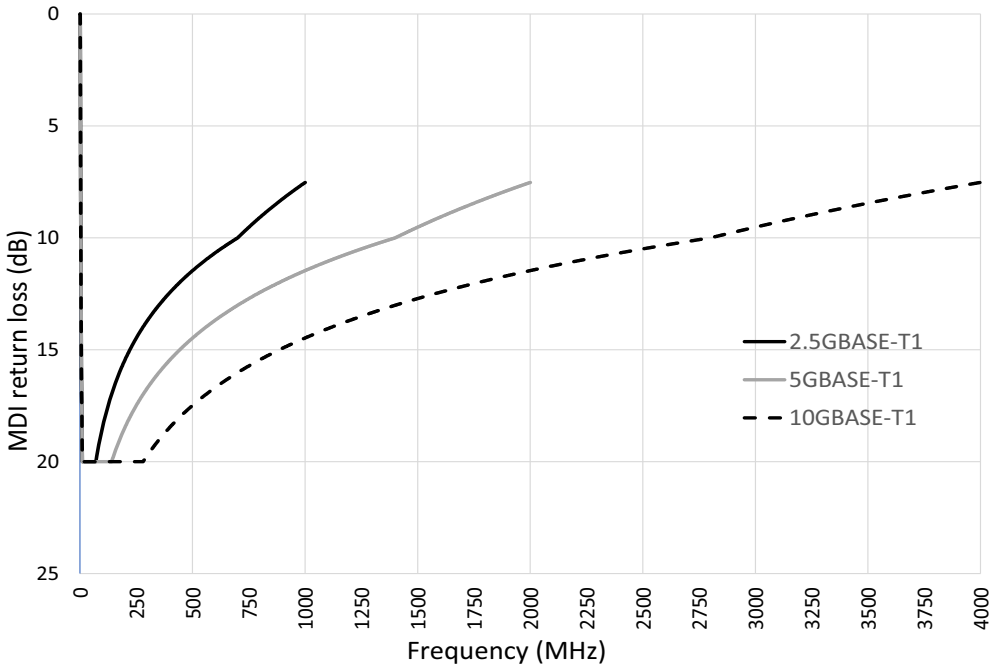

Figure 149–48—MDI return loss calculated using Equation (149–27)

149.8.3 MDI fault tolerance

See 96.8.3.

149.9 Environmental specifications

149.9.1 General safety

All equipment subject to this clause is expected to conform to all applicable local, state, national, and application-specific standards.

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149.9.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner.

149.9.2.1 Environmental safety

All equipment subject to this clause, when used in the automotive environment, is expected to conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications:

a) General loads: ISO 16750–1
b) Electrical loads: ISO 16750–2, ISO 7637–2:2008, and ISO 8820–1
c) Mechanical loads: ISO 16750–3, ASTM D4728, and ISO 12103–1
d) Climatic loads: ISO 16750–4, IEC 60068–2–1, IEC 60068–2–27, IEC 60068–2–30, IEC 60068–2–38, IEC 60068–2–52, IEC 60068–2–64, and IEC 60068–2–78
e) Chemical loads: ISO 16750–5 and ISO 20653

Automotive environmental conditions are generally more severe than those found in many commercial and industrial environments. The target automotive, industrial, or commercial environment(s) require careful analysis prior to implementation.

149.9.2.2 Electromagnetic compatibility

A system integrating a PHY intended for automotive applications is expected to comply with all applicable local and national codes. In addition, the system may need to comply with more stringent requirements for the limitation of electromagnetic interference. When used in an automotive environment, the PHY is expected to meet the following motor vehicle EMC requirements:

a) Radiated/conducted emissions: CISPR 25, IEC 61967–1, IEC 61967–4, and IEC 61000–4–21
b) Radiated/conducted immunity: ISO 11452, IEC 62132–1, IEC 62132–4, and IEC 61000–4–21
c) Electrostatic discharge: ISO 10605, IEC 61000–4–2, and IEC 61000–4–3
d) Electrical disturbances: IEC 62215–3, ISO 7637–2, and ISO 7637–3

Exact test setup and test limit values may be adapted to each specific application.

149.10 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of the PHY shall not exceed the limits shown in Table 149–20. Transmit data delay is measured from the input of a given unit of data at the XGMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the XGMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link.

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Table 149–20—Delay Limits

Mode	Interleave	Bit times	Pause Quanta	Delay (ns)
2.5GBASE-T1	1x	10 240	20	4096
5GBASE-T1	1x	10 240	20	2048
5GBASE-T1	2x	13 824	27	2764.8
10GBASE-T1	1x	10 240	20	1024
10GBASE-T1	2x	13 824	27	1382.4
10GBASE-T1	4x	20 480	40	2048

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149.11 Protocol implementation conformance statement (PICS) proforma for Clause 149, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1[246]

149.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 149, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

149.11.2 Identification

149.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

149.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 149, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1.
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[246]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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149.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*AN	Auto-Negotiation	98		O	Yes [ ] No [ ]
*EEE	Support of EEE capability	149.1.3.3		O	Yes [ ] No [ ]
*INS	Installation/cabling	149.7	Items marked with INS include installation practices and cabling specifications applicable when the link segment is balanced pair cabling, and not applicable to backplane link segments.	O	Yes [ ] No [ ]
*OAM	Support of MultiGBASE-T1 PCS level operations, administration, and maintenance	149.3.9		O	Yes [ ] No [ ]
*MDIO	Support of MDIO capability	45.1	Register and Interface support.	O	Yes [ ] No [ ]

149.11.4 PICS proforma tables for Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1

149.11.4.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.	98		AN:M	Yes [ ] N/A [ ]
G2	Capable of operating as MASTER or SLAVE, per runtime configuration.	149.1.3		M	Yes [ ]
G3	If Auto- Negotiation is not used, a MASTER-SLAVE relationship shall be established by management or hardware configuration of the PHYs.	149.1.3		AN:M	Yes [ ] N/A [ ]

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149.11.4.2 Physical Coding Sublayer (PCS)

149.11.4.2.1 PCS Transmit

Item	Feature	Subclause	Value/Comment	Status	Support
PCT1	PCS Reset	149.3.2.1	Described in 149.3.2.1.	M	Yes [ ]
PCT2	Management interface restore to operation	149.3.2.1	Within 10 ms from the setting of bit 1.2309.15.	M	Yes [ ]
PCT3	PCS 64B/65B Transmit state diagram	149.3.2.2	Figure 149–16 and Figure 149–17.	M	Yes [ ]
PCT4	PCS Transmit bit ordering	149.3.2.2	Figure 149–6.	M	Yes [ ]
PCT5	If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.	149.3.2.2		M	Yes [ ]
PCT6	If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate a sequence (T_n) defined in 149.3.5.1 to the PMA via the PMA_UNITDATA.request primitive.	149.3.2.2		M	Yes [ ]
PCT7	If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the normal mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control.	149.3.2.2		M	Yes [ ]
PCT8	All XGMII control code values that do not appear in the Table 149–2 shall not be transmitted and shall be treated as an error if received.	149.3.2.2.5		M	Yes [ ]
PCT9	Idle control characters	149.3.2.2.7	/I/ insertion and deletion shall occur in groups of 4.	M	Yes [ ]
PCT10	Adding Idle control characters	149.3.2.2.7	/I/s shall not be added while data is being received.	M	Yes [ ]
PCT11	Deleting Idle control characters	149.3.2.2.7	When deleting /I/s, the first four characters after a /T/ shall not be deleted.	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PCT12	LPI control characters	149.3.2.2.8	/LI/ insertion and deletion shall occur in groups of four.	M	Yes [ ]
PCT13	Adding LPI control characters	149.3.2.2.8	/LI/s shall not be added while data is being received.	M	Yes [ ]
PCT14	Ordered set	149.3.2.2.11	Sequence ordered set deletion shall only occur when two consecutive sequence ordered sets have been received and shall delete only one of the two.	M	Yes [ ]
PCT15	RS-FEC encoding	149.3.2.2.14	The RS-FEC encoding takes the 3260-bit vector tx_group50x65B, and shall generate the 34 10-bit parity symbols (340 bits total).	M	Yes [ ]
PCT16	Interleave set to depth setting	149.3.2.2.15	Interleaver depth set to value requested by link partner during Infofield exchange.	M	Yes [ ]
PCT17	Round-robin interleaving scheme	149.3.2.2.15	Figure 149–9.	M	Yes [ ]
PCT18	The PCS Transmit shall aggregate L RS-FEC input frames into an interleaved RS-FEC input superframe.	149.3.2.2.15		M	Yes [ ]
PCT19	Gray mapping for PAM4 encoding	149.3.2.2.19	Described in 149.3.2.2.19.	M	Yes [ ]
PCT20	Selectable precoder	149.3.2.2.20	Described in 149.3.2.2.20.	M	Yes [ ]
PCT21	PAM4 encoding	149.3.2.2.21	Described in 149.3.2.2.21.	M	Yes [ ]
PCT22	EEE transmit state diagram	149.3.2.2.22	Figure 149–20.	EEE:M	Yes [ ] N/A [ ]
PCT23	Sleep signal	149.3.2.2.22	Shall be transmitted when an LPI control character in the last 64B/65B block of a Reed-Solomon frame is detected by the PCS Transmit function.	EEE:M	Yes [ ] N/A [ ]
PCT24	After the sleep signal is transmitted, LPI control characters shall be input to the PCS scrambler continuously until the PCS Transmit function exits the LPI transmit mode.	149.3.2.2.22		EEE:M	Yes [ ] N/A [ ]
PCT25	While the PMA asserts SEND_N, the lpi_tx_mode variable shall control the transmit signal through the PMA_UNITDATA.request primitive.	149.3.2.2.22	Described in 149.3.2.2.22.	M	Yes [ ]

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149.11.4.2.2 PCS Receive

Item	Feature	Subclause	Value/Comment	Status	Support
PCR1	PCS 64B/65B Receive state diagram	149.3.2.3	Figure 149–18 and Figure 149–19	M	Yes [ ]
PCR2	PCS receive bit ordering	149.3.2.3	Figure 149–7	M	Yes [ ]
PCR3	Frame and block synchronization	149.3.2.3.1	Described in 149.3.2.3.1	M	Yes [ ]
PCR4	MASTER PHY receiver descrambler generator polynomial	149.3.2.3.2	Equation (149–6)	M	Yes [ ]
PCR5	SLAVE PHY receiver descrambler generator polynomial	149.3.2.3.2	Equation (149–5)	M	Yes [ ]
PCR6	RS-FEC parity bits	149.3.2.3.3	Defined in 149.3.2.2.14	M	Yes [ ]

149.11.4.2.3 Test-pattern generators

Item	Feature	Subclause	Value/Comment	Status	Support
TPG1	Transmit PCS operating in test-pattern mode.	149.3.3	Transmit continuously as illustrated in Figure 149–6, with the input to the RS-FEC encoder set to zero and the initial condition of the scrambler set to any non-zero value.	M	Yes [ ]
TPG2	Receive PCS operating in test-pattern mode.	149.3.3	Receive continuously as illustrated in Figure 149–7.	M	Yes [ ]

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149.11.4.2.4 Side-stream scrambler

Item	Feature	Subclause	Value/Comment	Status	Support
SSS1	MASTER PCS transmit side-stream scrambler	149.3.4	Equation (149–5).	M	Yes [ ]
SSS2	SLAVE PCS transmit side-stream scrambler	149.3.4	Equation (149–6).	M	Yes [ ]
SSS3	Initialized scrambler state	149.3.4	Never all zeros.	M	Yes [ ]
SSS4	Scrambler starting during PMA training	149.3.4	Continue to run uninterrupted during the transition from PAM2 to PAM4.	M	Yes [ ]
SSS5	Descrambler state synchronization	149.3.5.2	The PHY shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status.	M	Yes [ ]

149.11.4.2.5 LPI signaling

Item	Feature	Subclause	Value/Comment	Status	Support
LPI1	EEE-capable PHYs shall synchronize refresh intervals during LPI mode	149.3.6.1		EEE:M	Yes [ ] N/A [ ]
LPI2	Alert	149.3.6.1	Start at the beginning of any eighth PHY frame boundary starting at the beginning of the frame following a refresh PHY frame.	EEE:M	Yes [ ] N/A [ ]
LPI3	tx_refresh_active	149.3.6.1	Derived from the transmitted PHY frames as shown in Table 149–6.	EEE:M	Yes [ ] N/A [ ]
LPI4	tx_alert_start_next	149.3.6.1	Derived from the transmitted PHY frames as shown in Table 149–7.	EEE:M	Yes [ ] N/A [ ]
LPI5	During the quiet period	149.3.6.2	PHY stops transmitting.	EEE:M	Yes [ ] N/A [ ]

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149.11.4.2.6 Functions and state diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
FSD1	lpi_tx_sleep_timer	149.3.7.2.3	Period equal to eight RS-FEC frame periods.	EEE:M	Yes [ ] N/A [ ]
FSD2	lpi_tx_alert_timer	149.3.7.2.3	Period equal to four RS-FEC frame periods.	EEE:M	Yes [ ] N/A [ ]
FSD3	lpi_tx_wake_timer	149.3.7.2.3	Period equal to lpi_wake_time RS-FEC frame periods.	EEE:M	Yes [ ] N/A [ ]
FSD4	lpi_rx_wake_timer	149.3.7.2.3	Period equal to lpi_wake_time RS-FEC frame periods.	EEE:M	Yes [ ] N/A [ ]
FSD5	DECODE function	149.3.7.2.4	Decode the block based on code specified in 149.3.2.2.2.	M	Yes [ ]
FSD6	ENCODE function	149.3.7.2.4	Encode the block as specified in 149.3.2.2.2.	M	Yes [ ]
FSD7	RFER monitor state diagram functions	149.3.7.3	Implemented.	M	Yes [ ]
FSD8	PCS Transmit state diagram functions	149.3.7.3	Implemented.	M	Yes [ ]
FSD9	PCS Receive state diagram functions	149.3.7.3	Implemented.	M	Yes [ ]
FSD10	RFER function during LPI receive operation	149.3.7.3	Not performed from the time that the PCS 64B/65B Receiver enters the state RX_L, until the state RX_W is exited.	EEE:M	Yes [ ] N/A [ ]

149.11.4.2.7 PCS loopback

Item	Feature	Subclause	Value/Comment	Status	Support
PCSL1	Placed in loopback mode	149.3.8.3	When MDIO register 3.0.14 is set to a one.	MDIO:M	Yes [ ] N/A [ ]
PCSL2	When in PCS loopback mode	149.3.8.3	Accept data on the transmit path from the XGMII and return it on the receive path to the XGMII.	M	Yes [ ]
PCSL3	When in PCS loopback mode	149.3.8.3	Transmit a continuous stream of 65B RS-FEC encoded PAM4 symbols to the PMA sublayer.	M	Yes [ ]
PCSL4	When in PCS loopback mode	149.3.8.3	Ignore all data presented to it by the PMA sublayer.	M	Yes [ ]

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149.11.4.2.8 OAM

Item	Feature	Subclause	Value/Comment	Status	Support
OAM1	State diagram behavior	149.3.9.4	Conforms to Figure 149–24 and Figure 149–25	OAM:M	Yes [ ] N/A [ ]
OAM2	When the PCS frame is operating in interleaved mode of 2x or 4x, the first symbol (OAM<0>) shall be inserted in the first RS frame in the superframe so that the full OAM frame can packed into 8 superframes in the 2x interleaved mode, and into 4 superframes in the 4x interleaved mode.	149.3.9.2.1		OAM:M	Yes [ ] N/A [ ]
OAM3	Partially transmitted OAM frame	149.3.9.2.1	Described in 149.3.9.2.1	OAM:M	Yes [ ] N/A [ ]
OAM4	When OAM is not implemented	149.3.9.2.1	10-bit OAM field shall be set to all 0's	OAM:M	Yes [ ] N/A [ ]
OAM5	OAM frame data	149.3.9.2.2	Reserved fields shall be set to 0	OAM:M	Yes [ ] N/A [ ]
OAM6	OAM frame data symbol encoding	149.3.9.2.13	Using Reed-Solomon code (16,14)	OAM:M	Yes [ ] N/A [ ]
OAM7	Parity calculation	149.3.9.2.13	Same result as the shift register implementation shown in Figure 149–23	OAM:M	Yes [ ] N/A [ ]
OAM8	OAM Reed-Solomon shift register	149.3.9.2.13	Initialized to zero	OAM:M	Yes [ ] N/A [ ]
OAM9	BASE-T1 OAM Frame acceptance criteria	149.3.9.2.14	Described in 149.3.9.2.14	OAM:M	Yes [ ] N/A [ ]
OAMl0	If a PHY is already in LPI mode and receives SNR<1:0> set to 01 by its link partner.	149.3.9.2.15	Immediately exit LPI	EEE*O AM:M	Yes [ ] N/A [ ]
OAMl1	mr_tx_received	149.3.9.4.3	Clear on read	OAM:M	Yes [ ] N/A [ ]

149.11.4.3 Physical Medium Attachment (PMA)

149.11.4.3.1 PMA Reset function

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	PMA Reset	149.4.2.1	Described in 149.4.2.1	M	Yes [ ]

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149.11.4.3.2 PMA Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
PMAT1	When the PHY Control state diagram is not in the DISABLE_TRANSMITTER state, PMA Transmit.	149.4.2.2	Continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI.	M	Yes [ ]
PMAT2	During Link Synchronization, when sync_link_control = DISABLE and Auto-Negotiation is either not enabled or is not implemented, the sync_tx_symb output by the PHY Link Synchronization function shall be used in place of tx_symb as the data source for PMA Transmit.	149.4.2.2		AN:M	Yes [ ] N/A [ ]
PMAT3	When lpi_tx_mode = ALERT, the PN sequence defined in 149.4.2.6 shall be used in place of tx_symb as the data source for PMA Transmit.	149.4.2.2		EEE:M	Yes [ ] N/A [ ]
PMAT4	Signals generated by PMA Transmit.	149.4.2.2	Comply with 149.1.3.	M	Yes [ ]
PMAT5	TX_TCLK when MASTER	149.4.2.2	Sourced from a local clock source while meeting the transmit jitter requirements of 149.5.2.3.	M	Yes [ ]
PMAT6	MASTER-SLAVE relationship	149.4.2.2	Include loop timing.	M	Yes [ ]
PMAT7	TX_TCLK when SLAVE	149.4.2.2	Sourced from the recovered clock of 149.4.2.8 while meeting the transmit jitter requirements of 149.5.2.3.	M	Yes [ ]
PMAT8	PMA transmit fault function	149.4.2.2	Mapped to the transmit fault bit as specified in 45.2.1.7.4.	MDIO:M	Yes [ ] N/A [ ]
PMAT9	Average launch power of the transmitter when the PMA_transmit_disable variable is set to TRUE.	149.4.2.2.1	Less than –53 dBm.	M	Yes [ ]

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149.11.4.3.3 PMA Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
PMAR1	Quality of received symbols	149.4.2.3	RFER of less than 2×10^{-10} after RS-FEC decoding, over a channel meeting the requirements of 149.7.	M	Yes [ ]
PMAR2	If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.243.7.	149.4.2.3		MDIO:M	Yes [ ] N/A [ ]

149.11.4.3.4 PHY Control function

Item	Feature	Subclause	Value/Comment	Status	Support
PCF1	PHY Control state diagram	149.4.2.4	Figure 149–32	M	Yes [ ]
PCF2	12-octet Infofield	149.4.2.4	Include the fields in 149.4.2.4.2 through 149.4.2.4.8	M	Yes [ ]
PCF3	Infofield shall be transmitted at least 256 times with each change to octets 7 to 10.	149.4.2.4		M	Yes [ ]
PCF4	Infofield reserved bits	149.4.2.4.1	Set to zero on transmit and ignored when received by the link partner	M	Yes [ ]
PCF5	Start of Frame Delimiter hexadecimal value	149.4.2.4.2	0xBBA700	M	Yes [ ]
PCF6	PMA_state<7:6>	149.4.2.4.4	Communicate the state of the transmitting transceiver to the link partner	M	Yes [ ]
PCF7	Any Message Field value not listed in Table 149–10 or Table 149–11 shall not be transmitted and shall be ignored at the receiver.	149.4.2.4.4		M	Yes [ ]
PCF8	Any Message Field value not listed in Table 149–10 or Table 149–11 shall be ignored at the receiver.	149.4.2.4.4		M	Yes [ ]
PCF9	The Message Field setting for the first transmitted PMA frame shall be the first row of Table 149–10 for the MASTER and the first or second row of Table 149–11 for the SLAVE.	149.4.2.4.4		M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PCF10	For a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting.	149.4.2.4.4		M	Yes [ ]
PCF11	The optional EEE capability shall be enabled only if both PHYs set the capability bit EEEen = 1.	149.4.2.4.5		EEE:M	Yes [ ] N/A [ ]
PCF12	The optional BASE-T1 OAM capability shall be enabled only if both PHYs set the capability bit OAMen = 1.	149.4.2.4.5		OAM:M	Yes [ ] N/A [ ]
PCF13	The capability bit values shall be considered as valid only when the loc_rcvr_status bit is 1.	149.4.2.4.5		M	Yes [ ]
PCF14	Remaining PHY capability bits shall be reserved and set to 0.	149.4.2.4.5		M	Yes [ ]
PCF15	DataSwPFC24	149.4.2.4.6	Set to an integer multiple of 16	M	Yes [ ]
PCF16	DataSwPFC24 on switch from PAM2 to PAM4		Minimum of 4081 and maximum of 4785	M	Yes [ ]
PCF17	CRC16 polynomial	149.4.2.4.8	$(x + 1)(x^{15} + x + 1)$ of the previous 7 octets	M	Yes [ ]
PCF18	CRC16	149.4.2.4.8	Figure 149–29	M	Yes [ ]
PCF19	CRC16 delay elements	149.4.2.4.8	All initialized to zero	M	Yes [ ]
PCF20	Startup sequence	149.4.2.4.10	Comply with Figure 149–32	M	Yes [ ]
PCF21	During startup, prior to entering the COUNTDOWN state, the SLAVE shall align its transmit 65B RS-FEC frame to within +0/–4 × *S* partial PHY frames of the MASTER as seen at the SLAVE MDI.	149.4.2.4.10		M	Yes [ ]
PCF22	SLAVE Infofield partial PHY frame count	149.4.2.4.10	Match the MASTER Infofield partial PHY frame count for the aligned frame	M	Yes [ ]
PCF23	MASTER startup timing	149.4.2.4.10	Comply with values in Table 149–15	M	Yes [ ]
PCF24	SLAVE startup timing	149.4.2.4.10	Comply with values in Table 149–16	M	Yes [ ]

149.11.4.3.5 Link Monitor function

Item	Feature	Subclause	Value/Comment	Status	Support
LMK1	Link Monitor function	149.4.2.5	Comply with Figure 149–33	M	Yes [ ]

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149.11.4.3.6 PHY Link Synchronization

Item	Feature	Subclause	Value/Comment	Status	Support
PLS1	Link Synchronization PHY PMA training when Auto-Negotiation is disabled or not implemented.	149.4.2.6	Described in 149.4.2.4.	M	Yes [ ]
PLS2	SEND_S signal frequency	149.4.2.6	703.125 MHz.	M	Yes [ ]
PLS3	MASTER PN sequence generator	149.4.2.6	Equation (149–10).	M	Yes [ ]
PLS4	SLAVE PN sequence generator	149.4.2.6	Equation (149–11).	M	Yes [ ]
PLS5	PN sequence generator shift registers when entering TRANSMIT_DISABLE state.	149.4.2.6	reset to S[7:0] = 0000 0001.	M	Yes [ ]
PLS6	10GBASE-T1 mapping of $S_n[0]$ to T_n	149.4.2.6	If $Sn[0] = 0$ then $T_n = +1\ +1\ +1\ +1\ +1\ +1\ +1\ +1$. If $Sn[0] = 1$ then $T_n = -1\ -1\ -1\ -1\ -1\ -1\ -1\ -1$.	M	Yes [ ]
PLS7	5GBASE-T1 mapping of $S_n[0]$ to T_n	149.4.2.6	If $Sn[0] = 0$ then $T_n = +1\ +1\ +1\ +1$. If $Sn[0] = 1$ then $T_n = -1\ -1\ -1\ -1$.	M	Yes [ ]
PLS8	2.5GBASE-T1 mapping of $S_n[0]$ to T_n	149.4.2.6	If $Sn[0] = 0$ then $T_n = +1\ +1$. If $Sn[0] = 1$ then $T_n = -1\ -1$.	M	Yes [ ]
PLS9	The synchronization state diagram shall be used to synchronize 2.5GBASE-T1, 5GBASET1, or 10GBASE-T1 PHYs prior to the MultiGBASE-T1 link training.	149.4.2.6		M	Yes [ ]
PLS10	If Clause 98 Auto-Negotiation function is enabled, then the Auto-Negotiation function shall be used as the mechanism for PHY synchronization and the synchronization state diagram in Figure 149–31 remains in the SYNC_DISABLE state.	149.4.2.6		AN:M	Yes [ ] N/A [ ]
PLS11	send_s_sigdet	149.4.2.6.1	This variable shall be set FALSE no later than 1 µs after the signal goes quiet on the MDI.	M	Yes [ ]
PLS12	send_s_timer	149.4.2.6.2	Expires 1.25 µs ± 0.05 µs after being started.	M	Yes [ ]
PLS13	sigdet_wait_timer	149.4.2.6.2	Expires 5 µs ± 0.15 µs after being started.	M	Yes [ ]

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149.11.4.3.7 Refresh monitor function

Item	Feature	Subclause	Value/Comment	Status	Support
RMF1	Refresh monitor function	149.4.2.7	Comply with Figure 149–34	EEE:M	Yes [ ] N/A [ ]

149.11.4.3.8 Clock Recovery function

Item	Feature	Subclause	Value/Comment	Status	Support
CRF1	Clock Recovery function	149.4.2.8	Provide a clock suitable for signal sampling so that the RS FER indicated in 149.4.2.3 is achieved	M	Yes [ ]

149.11.4.3.9 MDI

Item	Feature	Subclause	Value/Comment	Status	Support
MDIS1	Symbol response $s(t)$	149.4.3.1	Comply with the electrical specifications given in 149.5.2	M	Yes [ ]

149.11.4.3.10 PMA State variables

Item	Feature	Subclause	Value/Comment	Status	Support
PMAS1	minwait_timer	149.4.4.2	Expires 975 μs ± 50 μs after being started	M	Yes [ ]
PMAS2	lpi_refresh_rx_timer	149.4.4.2	Period equal to 50 complete quiet-refresh signal periods, equivalent to 1.536/S ms	EEE:M	Yes [ ] N/A [ ]

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149.11.4.4 PMA electrical specifications

149.11.4.4.1 Test modes

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Test modes	149.5.1	Provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER testing	M	Yes [ ]
TM2	Test mode enabling	149.5.1	Enabled by setting a control register, 1.2313.15:13, or equivalent functionality	MDIO:M	Yes [ ] N/A [ ]
TM3	The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal operation.	149.5.1		M	Yes [ ]
TM4	Test Mode 1	149.5.1	Described in 149.5.1	M	Yes [ ]
TM5	Test Mode 2	149.5.1	Described in 149.5.1	M	Yes [ ]
TM6	Test Mode 3	149.5.1	Described in 149.5.1	M	Yes [ ]
TM7	Test Mode 4	149.5.1	Described in 149.5.1	M	Yes [ ]
TM8	Test Mode 5	149.5.1	Described in 149.5.1	M	Yes [ ]
TM9	Test Mode 6	149.5.1	Described in 149.5.1	M	Yes [ ]

149.11.4.4.2 Transmitter electrical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
TES1	Coupling	149.5.2	Operate with AC coupling to the MDI	M	Yes [ ]
TES2	Resistive differential load	149.5.2	Meet electrical requirements of this clause with a 100 Ω resistive differential load connected to transmitter output if load is not specified	M	Yes [ ]
TES3	Maximum output droop	149.5.2.1	Positive and negative droop shall be less than 15%	M	Yes [ ]
TES4	Transmitter linearity	149.5.2.2	Defined in 120D.3.1.2	M	Yes [ ]
TES5	Transmitter SNDR distortion for 10GBASE-T1	149.5.2.2	Exceed 38 dB	M	Yes [ ]
TES6	Transmitter SNDR distortion for 5GBASE-T1	149.5.2.2	Exceed 36 dB	M	Yes [ ]
TES7	Transmitter SNDR distortion for 2.5GBASE-T1	149.5.2.2	Exceed 35 dB	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TES8	RMS value of the MASTER TX_TCLK_175 jitter	149.5.2.3	Less than 1/*S* ps	M	Yes [ ]
TES9	Peak-to-peak value of the MASTER TX_TCLK_175 jitter	149.5.2.3	Less than 10/*S* ps	M	Yes [ ]
TES10	RMS value of the SLAVE TX_TCLK_175 jitter	149.5.2.3	Less than 2/*S* ps	M	Yes [ ]
TES11	Peak-to-peak value of the SLAVE TX_TCLK_175 jitter	149.5.2.3	Less than 20/*S* ps	M	Yes [ ]
TES12	TX_TCLK_175 jitter measurement interval	149.5.2.3	Measured over an interval of 1 ms ± 10%	M	Yes [ ]
TES13	TX_TCLK_175 jitter capture device bandwidth	149.5.2.3	Larger than 200 MHz	M	Yes [ ]
TES14	RMS value of the MDI output jitter	149.5.2.3.1	Less than 1/*S* ps	M	Yes [ ]
TES15	Peak-to-peak value of the MDI output jitter	149.5.2.3.1	Less than 10/*S* ps	M	Yes [ ]
TES16	MDI jitter measurement interval	149.5.2.3.1	Measured over an interval of 1 ms ± 10%	M	Yes [ ]
TES17	MDI jitter capture device bandwidth	149.5.2.3.1	Larger than 200 MHz	M	Yes [ ]
TES18	DJpk-pk jitter	149.5.2.3.2	Less than 9/*S* ps	M	Yes [ ]
TES19	EOJpk-pk jitter	149.5.2.3.2	Less than 4/*S* ps	M	Yes [ ]
TES20	Transmit power level	149.5.2.4	In the range of –1 dBm to 2 dBm	M	Yes [ ]
TES21	PSD of the transmitter	149.5.2.4	See Equation (149–14) and Equation (149–15)	M	Yes [ ]
TES22	Transmitter peak differential output	149.5.2.5	Less than 1.3 V peak-to-peak	M	Yes [ ]
TES23	Transmitter clock frequency	149.5.2.6	Within the range 5625×*S* MHz ± 50 ppm	M	Yes [ ]
TES24	Clock short-term rate of frequency variation	149.5.2.6	Less than 0.1 ppm/second when in LPI mode	EEE:M	Yes [ ] N/A [ ]
TES25	Clock short-term rate of frequency variation	149.5.2.6	Less than 0.1 ppm/second when switching to and from LPI mode	EEE:M	Yes [ ] N/A [ ]

149.11.4.4.3 Receiver electrical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
RES1	Receiver differential input signals	149.5.3.1	BER less than 10^{-12} after RS-FEC decoding	M	Yes [ ]

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149.11.4.5 Link segment characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
LSC1	Insertion loss	149.7.1.1	See Equation (149–18)	M	Yes [ ]
LSC2	2.5GBASE-T1 return loss	149.7.1.3	See Equation (149–19)	M	Yes [ ]
LSC3	5GBASE-T1 return loss	149.7.1.3	See Equation (149–20)	M	Yes [ ]
LSC4	10GBASE-T1 return loss	149.7.1.3	See Equation (149–22)	M	Yes [ ]
LSC5	Coupling attenuation	149.7.1.4	See Equation (149–24)	INS:M	Yes [ ] N/A [ ]
LSC6	Maximum link delay	149.7.1.6	Not to exceed 94 ns at all frequencies between 2 MHz and F_{max} MHz	M	Yes [ ]
LSC7	PSANEXT	149.7.2.1	See Equation (149–25)	M	Yes [ ]
LSC8	PSAACRF	149.7.2.2	See Equation (149–26)	M	Yes [ ]

149.11.4.6 MDI specifications

Item	Feature	Subclause	Value/Comment	Status	Support
MDI1	The electrical requirements specified in 149.5.2 and 149.5.3 shall be met when the PHY is connected to the MDI connector mated with a specified connector to a shielded balanced pair of conductors.	149.8.2		M	Yes [ ]
MDI2	Return loss	149.8.2.1	See Equation (149–27)	M	Yes [ ]

149.11.4.7 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	Sum of the transmit and receive data delays.	149.10	Not to exceed the limits in Table 149–20	M	Yes [ ]

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150. Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR4.2

150.1 Overview

This clause specifies the 400GBASE-SR4.2 PMD together with the multimode fiber medium. 400GBASE-SR4.2 uses the same media as 200GBASE-SR4. The 4.2 nomenclature is used to indicate that transmission is over four fiber pairs (eight individual fibers) with the use of two wavelengths. For 400GBASE-SR4.2 these wavelengths propagate in opposite directions on each individual fiber. The optical signal generated by this PMD type is modulated using a 4-level pulse amplitude modulation (PAM4) format. The PMD sublayer provides point-to-point 400 Gigabit Ethernet links over four pairs of multimode fiber, with a reach of up to at least 70 m on OM3, 100 m on OM4, and 150 m on OM5. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA, as shown in Table 150–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 150–1—Physical Layer clauses associated with the 400GBASE-SR4.2 PMD

Associated clause	400GBASE-SR4.2
117—RS	Required
117—400GMII[a]	Optional
118—400GMII Extender	Optional
119—PCS for 400GBASE-R	Required
120—PMA for 400GBASE-R	Required
120B—400GAUI-16 C2C	Optional
120C—400GAUI-16 C2M	Optional
120D—400GAUI-8 C2C	Optional
120E—400GAUI-8 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a]The 400GMII is an optional interface. However, if the 400GMII is not implemented, a conforming implementation is required to behave functionally as though the RS and 400GMII were present.

Figure 150–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 400 Gigabit Ethernet is introduced in Clause 116 and the purpose of each PHY sublayer is summarized in 116.2.

400GBASE-SR4.2 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

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Further relevant information may be found in Clause 1 (terminology and conventions, references, definitions and abbreviations) and Annex A (bibliography, referenced as [B1], [B2], etc.).

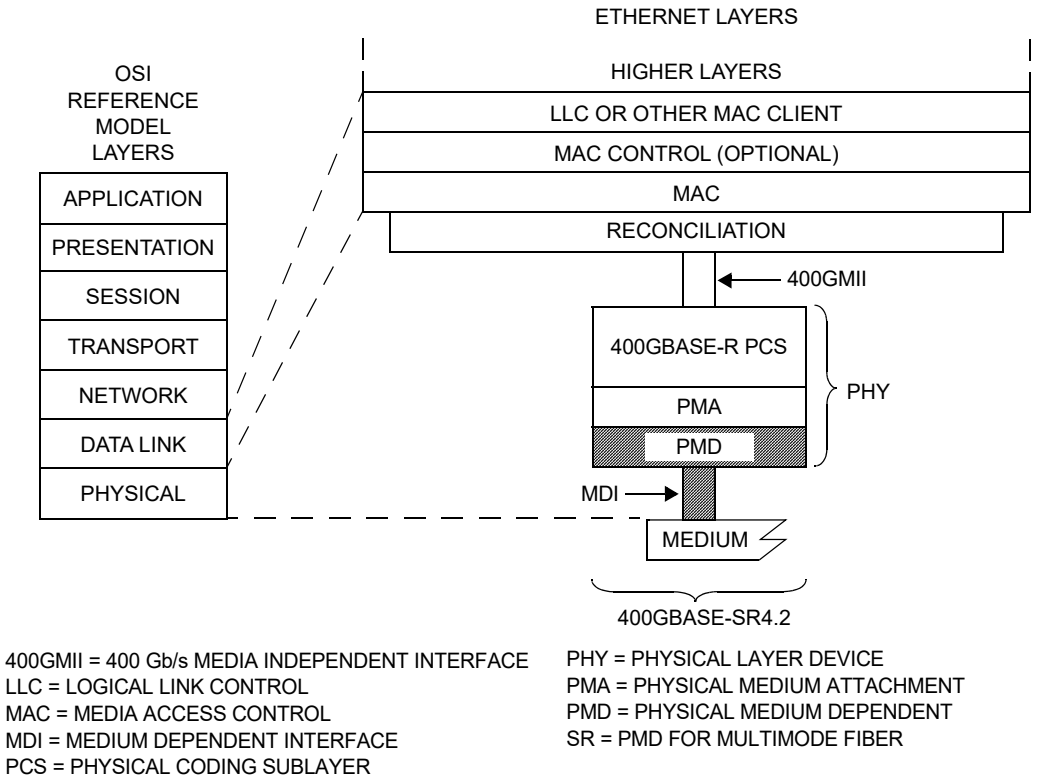

Figure 150–1—400GBASE-SR4.2 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

150.1.1 Bit error ratio

The bit error ratio (BER) when processed by the PMA (Clause 120) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when additionally processed by the PCS (Clause 119). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces. If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap.

150.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 400GBASE-SR4.2 PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

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The 400GBASE-SR4.2 PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with eight parallel symbol streams (n = 8).

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 400GBASE-SR4.2 PMD has eight parallel symbol streams, hence i = 0 to 7.

In the transmit direction, the PMA continuously sends n streams of PAM4 symbols to the PMD, one per lane, using the PMD:IS_UNITDATA_*i*.request primitive, at a nominal signaling rate of 26.5625 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends n streams of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, one per lane, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of 26.5625 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable SIGNAL_DETECT parameter as defined in 150.5.4. The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 150.1.1.

150.3 Delay and Skew

150.3.1 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation.

The sum of the transmit and receive delays at one end of the link contributed by the 400GBASE-SR4.2 PMD including 2 m of fiber in one direction shall be no more than 8192 bit times (16 pause_quanta or 20.48 ns).

Descriptions of overall system delay constraints and the definitions for bit times and pause_quanta, can be found in 116.4 and its references.

150.3.2 Skew constraints

The Skew (relative delay) between the PCS lanes is kept within limits so that the information on the PCS lanes can be reassembled by the PCS. The Skew Variation is also limited to ensure that a given PCS lane always traverses the same physical lane.

Skew and Skew Variation are defined in 116.5 and specified at the points SP1 to SP6 shown in Figure 116–4 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

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The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 116.5.

150.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 150–2, and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 150–3.

Table 150–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable 7 to PMD transmit disable 0	PMD transmit disable register	1.9.8 to 1.9.1	PMD_transmit_disable_7 to PMD_transmit_disable_0

Table 150–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect 7 to PMD receive signal detect 0	PMD receive signal detect register	1.10.8 to 1.10.1	PMD_signal_detect_7 to PMD_signal_detect_0

150.5 PMD functional specifications

The 400GBASE-SR4.2 PMD performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

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150.5.1 PMD block diagram

The PMD block diagram is shown in Figure 150–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a multimode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 150.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 150.10.3). Unless specified otherwise, all receiver measurements and tests defined in 150.8 are made at TP3.

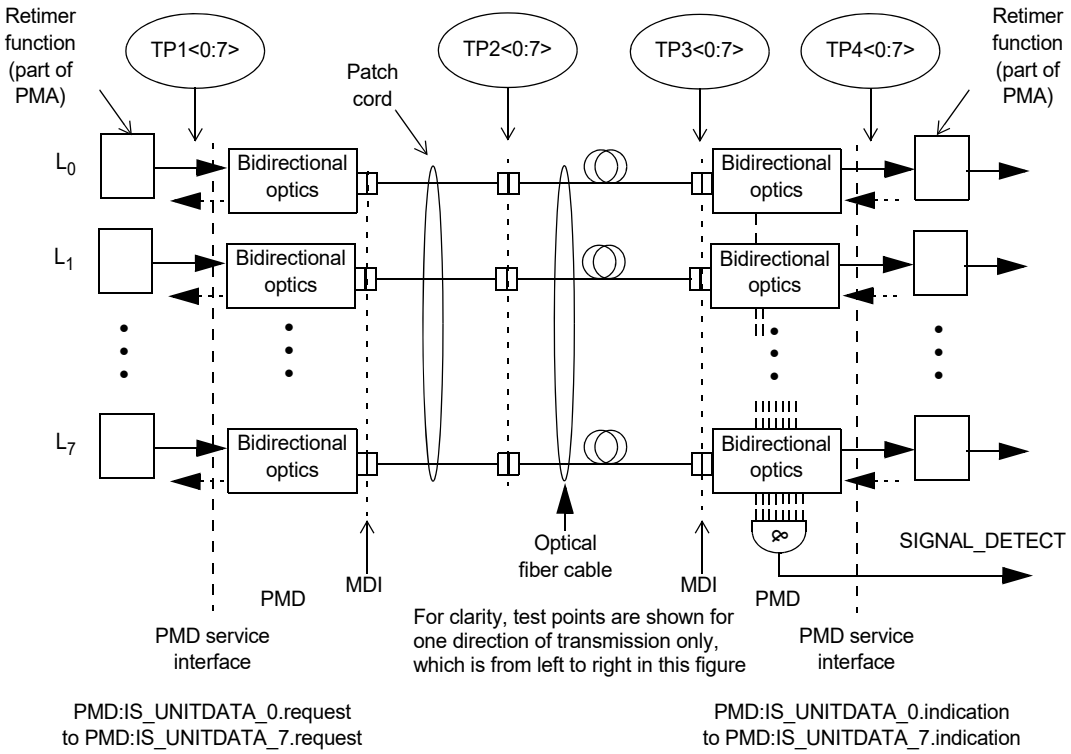

Figure 150–2—Block diagram for 400GBASE-SR4.2 transmit/receive paths

TP1<0:7> and TP4<0:7> are optional reference points that may be useful to implementers for testing components (these test points will not typically be accessible in an implemented system).

150.5.2 PMD transmit function

The PMD Transmit function shall convert the eight signals requested by the PMD service interface messages PMD:IS_UNITDATA_*i*.request into eight separate optical signals. The 400GBASE-SR4.2 PMD has eight parallel symbol streams, hence $i = 0$ to 7. Each optical signal shall then be delivered to the MDI, which contains eight parallel light paths for transmit, according to the transmit optical specifications in this clause. The four optical power levels in the signal in order from lowest to highest shall correspond to tx_symbol values zero, one, two, and three, respectively.

150.5.3 PMD receive function

The PMD Receive function shall convert the eight parallel optical signals received from the MDI into separate symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_7.indication, all according to the receive

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optical specifications in this clause. The four optical power levels in each signal in order from lowest to highest shall correspond to rx_symbol values zero, one, two, and three, respectively.

150.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 116.3.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 150–4. The PMD receiver is not required to verify whether a compliant 400GBASE-SR4.2 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 150–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For TxRx pair type TR[a]; Average optical power at TP3 ≤ –30 dBm for wavelength range 900 nm to 918 nm	FAIL
For TxRx pair type RT[a]; Average optical power at TP3 ≤ –30 dBm for wavelength range 844 nm to 863 nm	FAIL
For TxRx pair type TR[a]; [(Optical power at TP3 ≥ average receive power, each lane (min) in Table 150–7 for wavelength range 900 nm to 918 nm) AND (compliant 400GBASE-SR4.2 signal input)]	OK
For TxRx pair type RT[a]; [(Optical power at TP3 ≥ average receive power, each lane (min) in Table 150–7 for wavelength range 844 nm to 863 nm) AND (compliant 400GBASE-SR4.2 signal input)]	OK
All other conditions	Unspecified

[a]TxRx pair types are defined in 150.6.

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

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150.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:7, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 150–4.

150.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

150.5.7 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 150–7.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter in each lane.

150.5.8 PMD lane-by-lane transmit disable function (optional)

The PMD lane-by-lane transmit disable function is optional and allows the optical transmitter in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:7) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 150–7.

b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* to one, turning off the optical transmitter in each lane.

If the optional PMD lane-by-lane transmit disable function is not implemented in MDIO, an alternative method may be provided to independently disable each transmit lane.

150.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

150.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set PMD_transmit_fault to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

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150.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

150.6 Wavelength ranges

The transmit and receive wavelength ranges for the 400GBASE-SR4.2 PMD are defined in Table 150–5. Two TxRx pair types (combinations of Tx and Rx types that connect to a single fiber) are defined:

— TxRx pair type TR comprises a transmitter that uses the wavelength range 844 nm to 863 nm and a receiver that uses the wavelength range 900 nm to 918 nm.

— TxRx pair type RT comprises a transmitter that uses the wavelength range 900 nm to 918 nm and a receiver that uses the wavelength range 844 nm to 863 nm.

When connecting a 400GBASE-SR4.2 PMD to another 400GBASE-SR4.2 PMD, it is a requirement that every TxRx pair type RT at each end of the link be connected to a TxRx pair type TR at the other end of the link. The positioning of transmit and receive lanes at the MDI is specified in 150.10.3.1.

NOTE—There is no requirement to associate a particular electrical lane with a particular optical lane, as the PCS is capable of receiving lanes in any arrangement.

Table 150–5—Wavelength ranges

TxRx pair type	Transmit wavelength range	Receive wavelength range
TR	844 nm to 863 nm	900 nm to 918 nm
RT	900 nm to 918 nm	844 nm to 863 nm

150.7 PMD to MDI optical specifications for 400GBASE-SR4.2

The operating range for the 400GBASE-SR4.2 PMD is defined in Table 150–6. A compliant PMD operates on 50/125 μm multimode fibers, type A1a.2 (OM3), type A1a.3 (OM4), or type A1a.4 (OM5), according to the specifications defined in Table 150–13. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 400GBASE-SR4.2 PMD operating at 120 m on OM4 meets the operating range requirement of 0.5 m to 100 m on OM4).

Table 150–6—Operating range

PMD type	Required operating range[a]
400GBASE-SR4.2	0.5 m to 70 m for OM3
	0.5 m to 100 m for OM4
	0.5 m to 150 m for OM5

[a]The PCS FEC correction function may not be bypassed for any operating distance.

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150.7.1 Transmitter optical specifications

Each lane of a 400GBASE-SR4.2 transmitter shall meet the specifications in Table 150–7 per the definitions in 150.8.

Table 150–7—Transmit characteristics

Description	Value	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm	GBd
Modulation format	PAM4	—
Center wavelength (range), λ_1 for TxRx pair type TR Center wavelength (range), λ_2 for TxRx pair type RT	844 to 863 900 to 918	nm nm
RMS spectral width[a] (max) for TxRx pair type TR RMS spectral width[a] (max) for TxRx pair type RT	0.6 0.65	nm nm
Average launch power, each lane (max)	4	dBm
Average launch power, each lane (min)	–6.2	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	3	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)[b]	–4.2	dBm
Launch power in OMA_{outer} minus TDECQ (min)	–5.6	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	4.5	dB
TDECQ – $10\log_{10}(C_{eq})$[c], each lane (max)	4.5	dB
Average launch power of OFF transmitter, each lane (max)	–30	dBm
Extinction ratio, each lane (min)	3	dB
Transmitter transition time, each lane (max)	31	ps
$RIN_{12}OMA$ (max)	–128	dB/Hz
Optical return loss tolerance (max)	12	dB
Encircled flux[d]	≥ 86% at 19 μm ≤ 30% at 4.5 μm	—

[a]RMS spectral width is the standard deviation of the spectrum.
[b]Even if the TDECQ < 1.4 dB, the OMA (min) has to exceed this value.
[c]C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[d]If measured into type A1a.2, type A1a.3, or type A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4:2009.

150.7.2 Receiver optical specifications

Each lane of a 400GBASE-SR4.2 receiver shall meet the specifications in Table 150–8 per the definitions in 150.8.

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Table 150–8—Receive characteristics

Description	Value	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm	GBd
Modulation format	PAM4	—
Center wavelength (range), λ_1 for TxRx pair type RT Center wavelength (range), λ_2 for TxRx pair type TR	844 to 863 900 to 918	nm nm
Damage threshold[a] (min)	5	dBm
Average receive power, each lane (max)	4	dBm
Average receive power, each lane[b] (min)	–8.2	dBm
Receive power, each lane (OMA_{outer}) (max)	3	dBm
Receiver reflectance (max)	–12	dB
Stressed receiver sensitivity (OMA_{outer}), each lane[c] (max)	–3.5	dBm
Receiver sensitivity (OMA_{outer}), each lane[d] (max)	Equation (150–1)	dBm
Conditions of stressed receiver sensitivity test:[e]		
Stressed eye closure for PAM4 (SECQ), lane under test	4.5	dB
SECQ – $10\log_{10}(C_{eq})$[f] (max), lane under test	4.5	dB
OMA_{outer} of each aggressor lane	3	dBm

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
[b]Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Measured with conformance test signal at TP3 (see 150.8.10) for the BER specified in 150.1.1.
[d]Receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 4.5 dB.
[e]These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f]C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

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150.7.3 Illustrative link power budget

An illustrative power budget and penalties for 400GBASE-SR4.2 channels, which apply to both wavelength ranges, are shown in Table 150–9.

Table 150–9—Illustrative link power budget

Parameter	OM3	OM4	OM5	Unit
Effective modal bandwidth at 850 nm (min)[a]	2000	4700		MHz·km
Effective modal bandwidth at 910 nm (min)[a]	1260	1980	3100	MHz·km
Power budget (for max TDECQ)	6.9			dB
Operating distance	0.5 to 70	0.5 to 100	0.5 to 150	m
Channel insertion loss[b]	1.7	1.8	2	dB
Allocation for penalties[c] (for max TDECQ)	4.9			dB
Additional insertion loss allowed	0.3	0.2	0	dB

[a]Per IEC 60793-2-10.
[b]The channel insertion loss is calculated using the maximum distance specified in Table 150–6 and cabled optical fiber attenuation of 3 dB/km at 850 nm plus an allocation for connection and splice loss given in 150.10.2.2.1.
[c]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

150.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

150.8.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 150–11 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 150–11 may be used to perform that test. The test patterns used in this clause are shown in Table 150–10.

Table 150–10—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle	119.2.4.9
6	SSPRQ	120.5.11.2.3

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Table 150–11—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength, spectral width	3, 4, 5, 6, or valid 400GBASE-SR4.2 signal	150.8.2
Average optical power	3, 4, 5, 6, or valid 400GBASE-SR4.2 signal	150.8.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	150.8.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	150.8.5
Extinction ratio	4 or 6	150.8.6
Transmitter transition time	Square wave or 6	150.8.7
$RIN_{12}OMA$	Square wave	150.8.8
Stressed receiver sensitivity	3, 5, or valid 400GBASE-SR4.2 signal	150.8.10
Stressed eye closure for PAM4 (SECQ), calibration	6	150.8.10

150.8.1.1 Multi-lane testing considerations

Stressed receiver sensitivity is defined for each lane at the BER specified in 150.1.1. Measurements with Pattern 3 (PRBS31Q) allow lane-by-lane BER measurements. In stressed receiver sensitivity measurements, unstressed lanes may be created by setting the power at the receiver under test well above its sensitivity and/or not stressing those lanes with ISI and jitter, or by other means. Each receive lane is stressed in turn while all are operated. All aggressor lanes are operated as specified. Where relevant, parameters are defined with all co-propagating and counter-propagating lanes operational so that crosstalk effects are included. Where not otherwise specified, the maximum amplitude (OMA_{outer}) for a particular situation is used. Alternative test methods that generate equivalent results may be used. While the lanes in a particular direction may share a common clock, the Tx and Rx directions are not synchronous to each other. If Pattern 3 is used for the lanes not under test using a common clock, there is at least 31 UI delay between the PRBS31Q patterns on one lane and any other lane so that the symbols on each lane are not correlated within the PMD.

150.8.2 Center wavelength and spectral width

The center wavelength and RMS spectral width of each optical lane shall be within the range given in Table 150–7 if measured per IEC 61280-1-3. The lane under test is modulated using one of the test patterns specified in Table 150–11.

150.8.3 Average optical power

The average optical power of each lane shall be within the limits given in Table 150–7 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using one of the test patterns defined in Table 150–11.

150.8.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} of each lane shall be within the limits given in Table 150–7 if measured as defined in 121.8.4.

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150.8.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

TDECQ is a measure of each optical transmitter's vertical eye closure as measured through an optical to electrical converter (O/E) with a bandwidth equivalent to a combined reference receiver and worst case optical channel, and equalized with the reference equalizer specified in 150.8.5.1. Table 150–11 specifies the test pattern to be used for measurement of TDECQ.

The TDECQ and TDECQ – $10\log_{10}(C_{eq})$ of each lane shall be within the limits given in Table 150–7 if measured using the methods specified in 121.8.5, with the following exceptions:

— The polarization rotator and test fiber shown in Figure 121–4 are not used.

— The optical channel requirements in 121.8.5.2 do not apply. Instead, the optical splitter and variable reflector are adjusted so that each transmitter is tested with an optical return loss equal to the "Optical return loss tolerance (max)" given in Table 150–7.

— The combination of the O/E converter and the oscilloscope used to measure the optical waveform has a 3 dB bandwidth of 8.96 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 17.92 GHz. At frequencies above 1.5 × 17.92 GHz the response should not exceed −24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

— The reference equalizer to be used for TDECQ is specified in 150.8.5.1.

150.8.5.1 TDECQ reference equalizer

The reference equalizer for 400GBASE-SR4.2 is a 5-tap, T-spaced, feed-forward equalizer (FFE), where T is the symbol period. A functional model of the reference equalizer is shown in Figure 150–3. The sum of the equalizer tap coefficients is equal to 1. Tap 1, tap 2, or tap 3, has the largest magnitude tap coefficient, which is constrained to be at least 0.85.

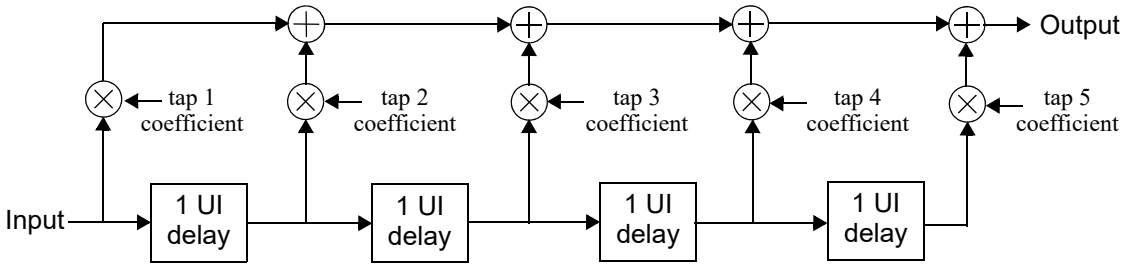

Figure 150–3—TDECQ reference equalizer functional model

NOTE—This reference equalizer is part of the TDECQ test and does not imply any particular receiver implementation.

150.8.6 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 150–7 if measured using the methods specified in 121.8.6.

150.8.7 Transmitter transition time

The transmitter transition time of each lane shall be within the limits given in Table 150–7 if measured using a test pattern specified for transmitter transition time in Table 150–11.

Transmitter transition time is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer}, or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling

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edges respectively, as measured through an O/E converter and oscilloscope with response defined as follows. The combined response of the O/E converter and oscilloscope has a 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz. At frequencies above 1.5 × 26.5625 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The 0% level and the 100% level are P_0 and P_3 as defined by the OMA_{outer} measurement procedure (see 150.8.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence and the falling edge is that within the 33333000000 symbol sequence

150.8.8 Relative intensity noise ($RIN_{12}OMA$)

$RIN_{12}OMA$ shall be as defined by the measurement methodology of 52.9.6 using an optical return loss of 12 dB and with the following exceptions:

a) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 26.6 GHz).

b) The test pattern is according to Table 150–11.

150.8.9 Receiver sensitivity

Receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 4.5 dB. Receiver sensitivity should meet Equation (150–1), which is illustrated in Figure 150–4.

$$RS = \max(-6.6, SECQ - 8) \quad \text{(dBm)} \tag{150–1}$$

where

RS	is the receiver sensitivity
SECQ	is the SECQ of the transmitter used to measure the receiver sensitivity

The normative requirement for receivers is stressed receiver sensitivity.

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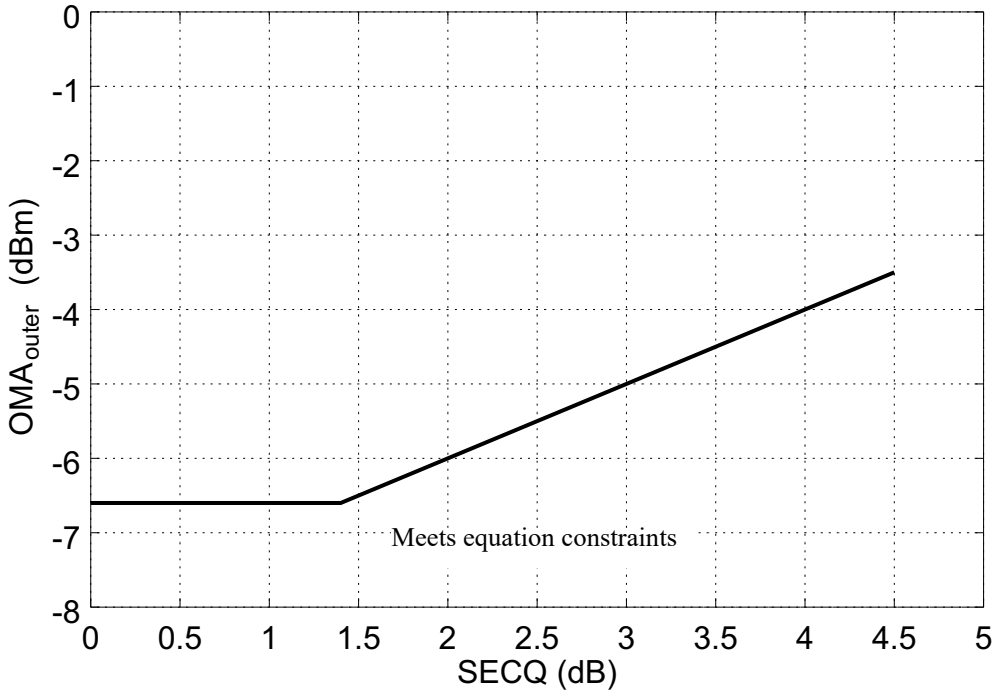

Figure 150–4—Illustration of receiver sensitivity

150.8.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 150–8 if measured using the methodology defined in 121.8.10.1 and 121.8.10.3, with the conformance test signal at TP3 as described in 121.8.10.2, with the following exceptions:

- The SECQ of the stressed receiver conformance test signal is measured according to 150.8.5, except that the combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz. At frequencies above 1.5 × 26.5625 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response. The optical splitter and variable reflector shown in Figure 121–4 are not used, and the transition time is no greater than the value specified in Table 150–7.
- With the Gaussian noise generator on and the sinusoidal jitter and sinusoidal interferer turned off, the $RIN_{12}OMA$ of the SRS test source should be no greater than the $RIN_{12}OMA$ (max) specified for the transmit characteristics in Table 150–7.
- The test patterns used for stressed receiver sensitivity are specified in Table 150–11.
- The signaling rate, the required stressed eye closure (SECQ), and the maximum $SECQ - 10\log_{10}(C_{eq})$ of the stressed receiver conformance test signal are as specified in Table 150–8.
- The applied sinusoidal jitter is specified in 150.8.10.1.
- The OMA_{outer} of the aggressor lanes is specified in Table 150–8.

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The BER is required to be met for each lane under test on its own. Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. Any of the patterns specified for stressed receiver sensitivity in Table 150–11 is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal.

150.8.10.1 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table 150–12.

Table 150–12—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter peak-to-peak (UI)
$f < 40$ kHz	Not specified
40 kHz $< f \leq 4$ MHz	2×10^5 Hz/f
4 MHz $< f \leq 10\ LB$[a]	0.05

[a]LB = loop bandwidth; upper frequency bound for added sinusoidal jitter should be at least 10 times the loop bandwidth of the receiver being tested.

150.9 Safety, installation, environment, and labeling

150.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

150.9.2 Laser safety

400GBASE-SR4.2 optical transceivers shall conform to Hazard Level 1M laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[247]

150.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

[247]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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150.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 400GBASE-SR4.2 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate, in the literature associated with the PHY, the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

150.9.5 Electromagnetic emission

A system integrating a 400GBASE-SR4.2 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

150.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

150.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (i.e., 400GBASE-SR4.2).

Labeling requirements for Hazard Level 1M lasers are given in the laser safety standards referenced in 150.9.2.

150.10 Fiber optic cabling model

The fiber optic cabling (channel) contains eight optical fibers, each of which carries bidirectional traffic, to support 400GBASE-SR4.2. The fiber optic cabling interconnects the TxRx pairs (see 150.6) at the MDI on one end of the channel to the TxRx pairs at the MDI on the other end of the channel. As defined in 150.10.3, the optical lanes appear in defined locations at the MDI but the locations are not assigned specific lane numbers within this standard because any TxRx pair at the MDI on one end of the channel may be connected to any TxRx pair of the opposite type on the other end of the channel.

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150.10.1 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 150–5.

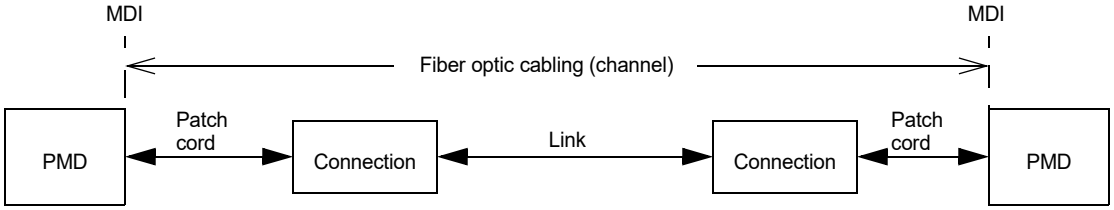

Figure 150–5—Fiber optic cabling model

The channel insertion loss is given in Table 150–13. A channel may contain additional connectors as long as the optical characteristics of the channel (such as attenuation, modal dispersion, reflections and losses of all connectors and splices) meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-1 one-cord method. As OM4 and OM5 optical fiber meet the requirements for OM3, a channel compliant to the "OM3" column may use OM4 or OM5 optical fiber, or a combination of OM3, OM4, and OM5. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 150–13—Fiber optic cabling (channel) characteristics

Description	OM3	OM4	OM5	Unit
Operating distance (max)	70	100	150	m
Cabling Skew (max)	79			ns
Cabling Skew Variation[a] (max)	2.4			ns
Channel insertion loss[b] (max)	1.7	1.8	2	dB
Channel insertion loss (min)	0			dB

[a]An additional 400 ps of Skew Variation could be caused by wavelength changes, which are attributable to the transmitter not the channel.

[b]These channel insertion loss values include cable loss plus 1.5 dB allocated for connection and splice loss, over the wavelength ranges 844 nm to 863 nm and 900 nm to 918 nm. Compliant channel insertion loss at 850 nm also demonstrates compliance at 910 nm.

150.10.2 Characteristics of the fiber optic cabling (channel)

The fiber optic cabling shall meet the specifications defined in Table 150–13. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

150.10.2.1 Optical fiber cable

The fiber contained within the fiber optic cabling shall comply with the specifications and parameters of Table 150–14. A variety of multimode cable types may satisfy these requirements, provided the resulting channel also meets the specifications of Table 150–13.

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Table 150–14—Optical fiber and cable characteristics

Description	OM3[a]	OM4[b]	OM5[c]	Unit
Nominal core diameter	50			μm
Nominal fiber specification wavelength	850		850 and 953	nm
Effective modal bandwidth at 850 nm (min)[d]	2000	4700		MHz·km
Effective modal bandwidth at 910 nm (min)[d]	Not specified[e]			MHz·km
Effective modal bandwidth at 953 nm (min)[d]	Not specified[e]		2470	MHz·km
Cabled optical fiber attenuation (max)	3			dB/km
Zero dispersion wavelength (λ_0)	$1295 \le \lambda_0 \le 1340$		$1297 \le \lambda_0 \le 1328$	nm
Chromatic dispersion slope (max) (S_0)	0.105 for $1295 \le \lambda_0 \le 1310$ and $0.000375 \times (1590 - \lambda_0)$ for $1310 \le \lambda_0 \le 1340$		$-412/(840(1-(\lambda_0/840)^4))$	ps/(nm^2·km)

[a]IEC 60793-2-10 type A1a.2.
[b]IEC 60793-2-10 type A1a.3.
[c]IEC 60793-2-10 type A1a.4.
[d]When measured with the launch conditions specified in Table 150–7.
[e]Effective modal bandwidth guidance is provided at all wavelengths in the 840 nm to 953 nm range in IEC 60793-2-10. For OM3, the guidance is 1260 MHz·km at 910 nm and 1033 MHz·km at 953 nm. For OM4, the guidance is 1980 MHz·km at 910 nm and 1459 MHz·km at 953 nm. For OM5, the guidance is 3100 MHz·km at 910 nm.

150.10.2.2 Optical fiber connection

An optical fiber connection, as shown in Figure 150–5, consists of a mated pair of optical connectors.

150.10.2.2.1 Connection insertion loss

The maximum link distance is based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an average insertion loss per connection of 0.5 dB. Connections with lower loss characteristics may be used provided the requirements of Table 150–13 are met. However, the loss of a single connection shall not exceed 0.75 dB.

150.10.2.2.2 Maximum discrete reflectance

The maximum discrete reflectance shall be less than –20 dB.

150.10.3 Medium Dependent Interface (MDI)

The 400GBASE-SR4.2 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 150–5). The 400GBASE-SR4.2 PMD is coupled to the fiber optic cabling through one connector plug into the MDI optical receptacle as shown in Figure 150–7. Example constructions of the MDI include the following:

a) PMD with a connectorized fiber pigtail plugged into an adapter;
b) PMD receptacle.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 150.5.1, not at the MDI.

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150.10.3.1 Optical lane assignments

The four type TR and four type RT TxRx pairs of 400GBASE-SR4.2 shall occupy the positions depicted in Figure 150–6 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains 8 active positions within 12 total positions. The four center positions are unused. The TR TxRx pair types occupy the leftmost four positions. The RT TxRx pair types occupy the rightmost four positions. Transmit wavelengths in the range defined for λ_1 in Table 150–7 and receive wavelengths in the range defined for λ_2 in Table 150–7 shall use TR positions. Receive wavelengths in the range defined for λ_1 and transmit wavelengths in the range defined for λ_2 shall use RT positions.

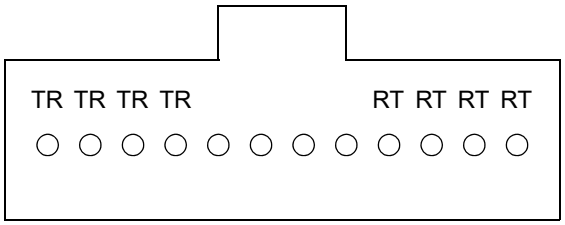

Figure 150–6—Optical lane assignments

150.10.3.2 MDI requirements

The MDI shall optically mate with the compatible plug on the optical fiber cabling. The MDI adapter or receptacle shall meet the dimensional specifications for interface 7-1-3: *MPO adapter interface - opposed keyway configuration*, or interface 7-1-10: *MPO active device receptacle, flat interface*, as defined in IEC 61754-7-1. The plug terminating the optical fiber cabling shall meet the dimensional specifications of interface 7-1-4: *MPO female plug connector, flat interface for 2 to 12 fibers*, as defined in IEC 61754-7-1. Figure 150–7 shows an MPO female plug connector with flat interface, and an MDI. The MDI connection shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2 for performance grade Bm/2m.

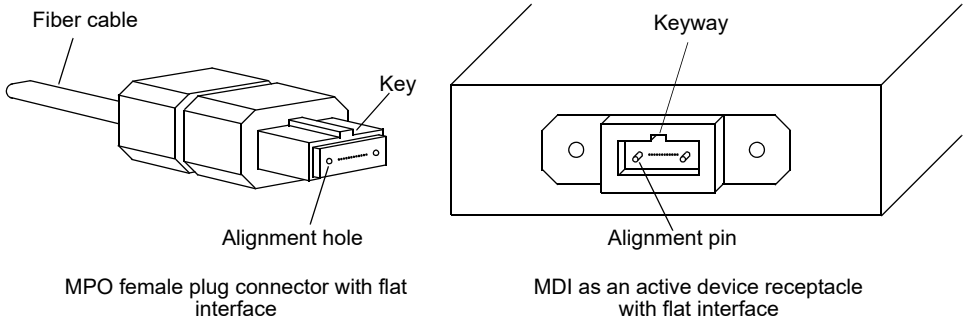

Figure 150–7—MPO female plug with flat interface and MDI active device receptacle with flat interface

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150.11 Protocol implementation conformance statement (PICS) proforma for Clause 150, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR4.2[248]

150.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 150, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR4.2, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

150.11.2 Identification

150.11.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

150.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 150, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR4.2
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[248]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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150.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*INS	Installation / cable	150.10.1	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	150.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	150.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	150.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	150.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	150.4	Registers and interface supported	O	Yes [ ] No [ ]

150.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR4.2

150.11.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 400GBASE-R PCS and PMA	150.1		M	Yes [ ]
F2	Integration with management functions	150.1		O	Yes [ ] No [ ]
F3	Bit error ratio	150.1.1	Meets the BER specified in 150.1.1	M	Yes [ ]
F4	Transmit function	150.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
F5	Mapping between optical signal and logical signal for transmitter	150.5.2	Optical power levels from lowest to highest correspond to tx_symbol values zero, one, two, and three, respectively	M	Yes [ ]
F6	Receive function	150.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]
F7	Conversion of 8 optical signals to 8 electrical signals	150.5.3	For delivery to the PMD service interface	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F8	Mapping between optical signal and logical signal for receiver	150.5.3	Optical power levels from lowest to highest correspond to rx_symbol values zero, one, two, and three, respectively	M	Yes [ ]
F9	Global Signal Detect function	150.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication(SIGNAL_DETECT)	M	Yes [ ]
F10	Global Signal Detect behavior	150.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all 8 lanes	M	Yes [ ]
F11	Lane-by-lane Signal Detect function	150.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 150–4	MD:O	Yes [ ] No [ ] N/A [ ]
F12	PMD reset function	150.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

150.11.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	150.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	150.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD_lane_by_lane_transmit_ disable function	150.5.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_*i* variable	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD lane-by-lane transmit disable	150.5.8	Disables each optical transmitter independently if M3 = No	!MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_fault function	150.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M6	PMD_transmit_fault function	150.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
M7	PMD_receive_fault function	150.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

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150.11.4.3 PMD to MDI optical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Transmitter meets specifications in Table 150–7	150.7.1	Per definitions in 150.8	M	Yes [ ]
S2	Receiver meets specifications in Table 150–8	150.7.2	Per definitions in 150.8	M	Yes [ ]

150.11.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	150.8	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and spectral width	150.8.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	150.8.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA_{outer} measurements	150.8.4	Each lane	M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	150.8.5	Each lane	M	Yes [ ]
OM6	Extinction ratio	150.8.6	Per IEC 61280-2-2	M	Yes [ ]
OM7	Transmitter transition time	150.8.7	Each lane	M	Yes [ ]
OM8	$RIN_{12}OMA$ measurement procedure	150.8.8	Each lane	M	Yes [ ]
OM9	Stressed receiver sensitivity	150.8.10	See 150.8.10	M	Yes [ ]

150.11.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	150.9.1	Conforms to the general safety requirements in J.2	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1M	150.9.2	Conforms to Hazard Level 1M laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	150.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

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150.11.4.6 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	150.10	Meets requirements specified in Table 150–13	INS:M	Yes [ ] N/A [ ]
OC2	Optical fiber characteristics	150.10.1	Per Table 150–14	INS:M	Yes [ ] N/A [ ]
OC3	Maximum discrete reflectance	150.10.2.2	Less than –20 dB	INS:M	Yes [ ] N/A [ ]
OC4	MDI layout	150.10.3.1	Optical lane assignments per Figure 150–6	M	Yes [ ]
OC5	MDI mating	150.10.3.2	MDI optically mates with plug on the cabling	M	Yes [ ]
OC6	MDI dimensions	150.10.3.2	Per IEC 61754-7-1 interface 7-1-3 or interface 7-1-10	M	Yes [ ]
OC7	Cabling connector dimensions	150.10.3.2	Per IEC 61754-7-1 interface 7-1-4	INS:M	Yes [ ] N/A [ ]
OC8	MDI requirements	150.10.3.2	Per IEC 61753-1 and IEC 61753-022-2, performance grade Bm/2m	INS:M	Yes [ ] N/A [ ]

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151. Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-FR4 and 400GBASE-LR4-6

151.1 Overview

This clause specifies the 400GBASE-FR4 and the 400GBASE-LR4-6 PMDs together with the single-mode fiber medium. The optical signals generated by these two PMD types are modulated using a 4-level pulse amplitude modulation (PAM4) format. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 151–1 to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 151–1—Physical Layer clauses associated with the 400GBASE-FR4 and 400GBASE-LR4-6 PMDs

Associated clause	400GBASE-FR4, 400GBASE-LR4-6
117—RS	Required
117—400GMII[a]	Optional
118—400GMII Extender	Optional
119—PCS for 400GBASE-R	Required
120—PMA for 400GBASE-R	Required
120B—400GAUI-16 C2C	Optional
120C—400GAUI-16 C2M	Optional
120D—400GAUI-8 C2C	Optional
120E—400GAUI-8 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a]The 400GMII is an optional interface. However, if the 400GMII is not implemented, a conforming implementation behaves functionally as though the RS and 400GMII were present.

Figure 151–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 400 Gb/s Ethernet is introduced in Clause 116 and the purpose of each PHY sublayer is summarized in 116.2.

400GBASE-FR4 and 400GBASE-LR4-6 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

151.1.1 Bit error ratio

The bit error ratio (BER) when processed according to Clause 120 shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when processed according to Clause 120 and

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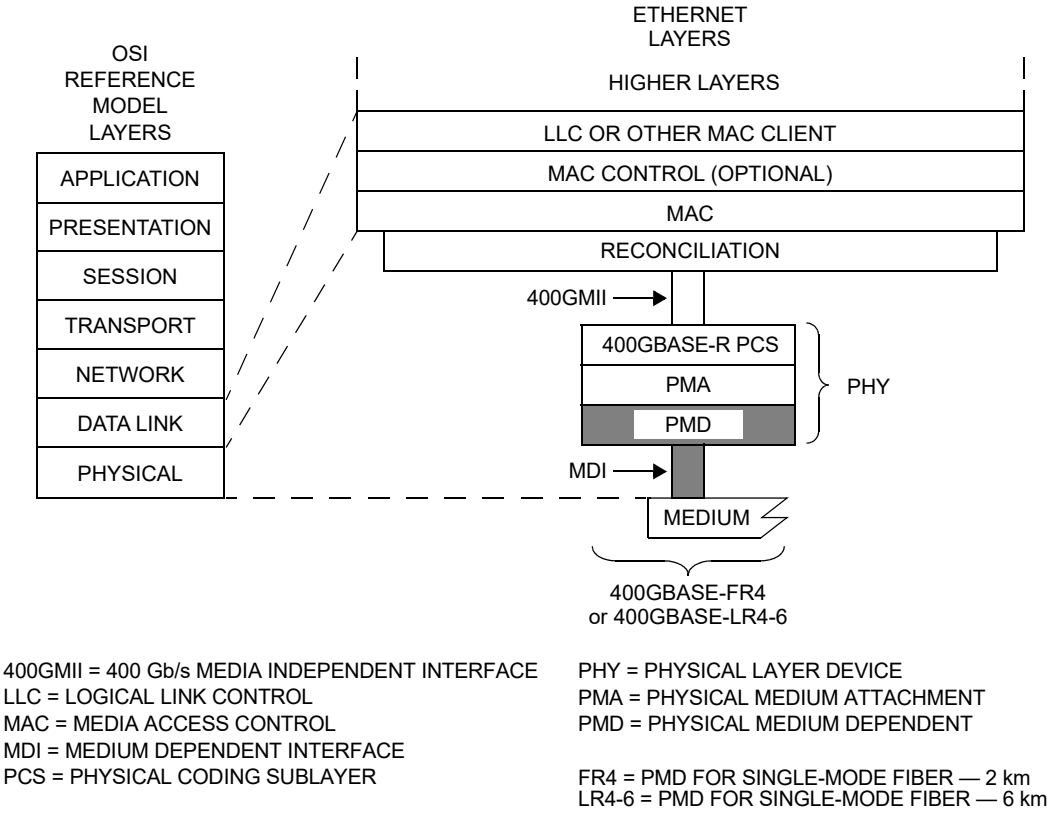

Figure 151–1—400GBASE-FR4 and 400GBASE-LR4-6 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

then Clause 119. For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap.

151.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 400GBASE-FR4 and 400GBASE-LR4-6 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 116.3. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

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In the transmit direction, the PMA continuously sends four parallel symbol streams to the PMD, one per lane, each at a nominal signaling rate of 53.125 GBd. The PMD then converts these streams of data units into the appropriate signals on the MDI.

In the receive direction, the PMD continuously sends four parallel symbol streams to the PMA corresponding to the signals received from the MDI, one per lane, each at a nominal signaling rate of 53.125 GBd.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication(SIGNAL_OK) inter-sublayer service interface primitive defined in 116.3.

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 151.1.1.

151.3 Delay and Skew

151.3.1 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the 400GBASE-FR4 or 400GBASE-LR4-6 PMD including 2 m of fiber in one direction shall be no more than 8192 bit times (16 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 116.4 and its references.

151.3.2 Skew constraints

The Skew (relative delay between the lanes) and Skew Variation are kept within limits so that the information on the lanes can be reassembled by the PCS. Skew and Skew Variation are defined in 116.5 and specified at the points SP1 to SP6 shown in Figure 116–4 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 116.5. The measurements of Skew and Skew Variation are defined in 87.8.2.

151.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO

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control variables to PMD control variables shall be as shown in Table 151–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 151–3.

Table 151–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable 3 to PMD transmit disable 0	PMD transmit disable register	1.9.4 to 1.9.1	PMD_transmit_disable_3 to PMD_transmit_disable_0

Table 151–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect 3 to PMD receive signal detect 0	PMD receive signal detect register	1.10.4 to 1.10.1	PMD_signal_detect_3 to PMD_signal_detect_0

151.5 PMD functional specifications

The 400GBASE-FR4 and 400GBASE-LR4-6 PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

151.5.1 PMD block diagram

The PMD block diagram is shown in Figure 151–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 151.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 151.11.3). Unless specified otherwise, all receiver measurements and tests defined in 151.8 are made at TP3.

TP1<0:3> and TP4<0:3> are optional reference points that may be useful to implementers for testing components (these test points are not typically accessible in an implemented system).

151.5.2 PMD transmit function

The PMD Transmit function shall convert the four symbol streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request into four separate optical signals. The four optical signals shall then be wavelength division multiplexed and delivered to the MDI, all

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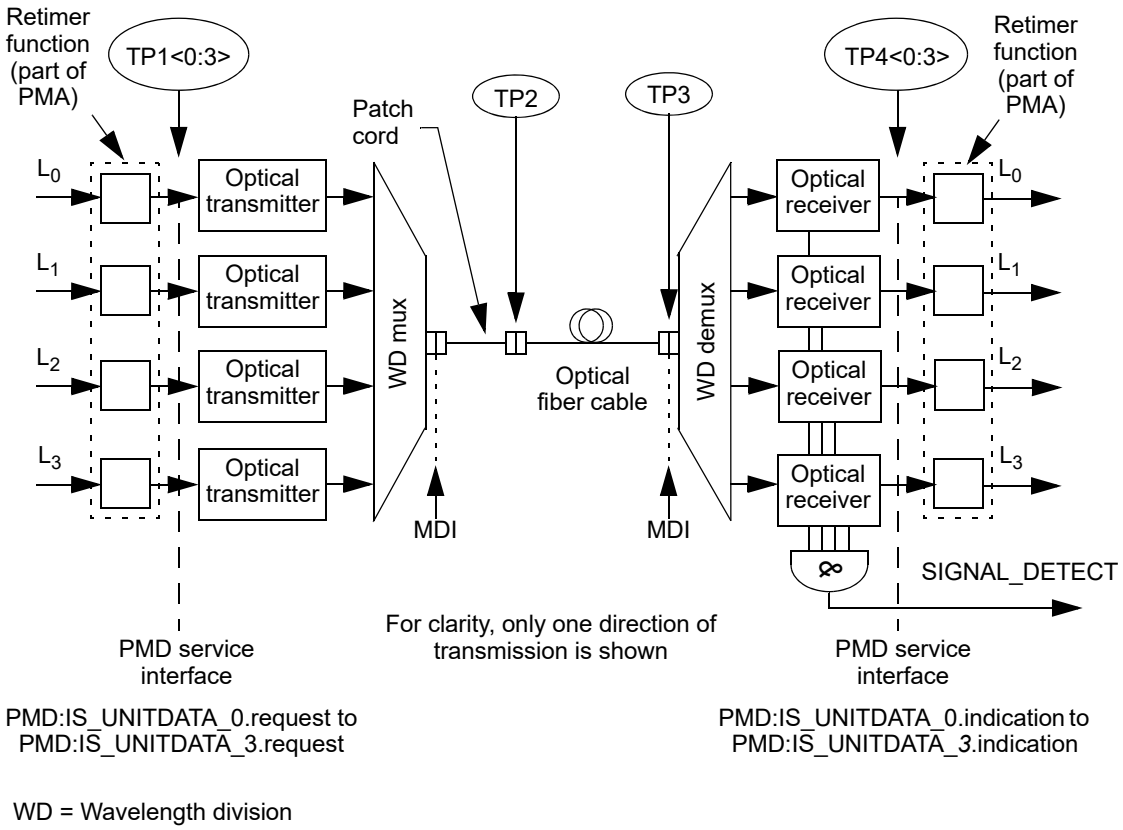

NOTE—Specification of the retimer function and the electrical implementation of the PMD service interface is beyond the scope of this standard.

Figure 151–2—Block diagram for 400GBASE-FR4 and 400GBASE-LR4-6 transmit/receive paths

according to the transmit optical specifications in this clause. The four optical power levels in the signal in order from lowest to highest shall correspond to tx_symbol values zero, one, two, and three, respectively.

151.5.3 PMD receive function

The PMD Receive function shall demultiplex the composite optical signal received from the MDI into four separate optical signals. The four optical signals shall then be converted into four symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication, all according to the receive optical specifications in this clause. The four optical power levels in each signal in order from lowest to highest shall correspond to rx_symbol values zero, one, two, and three, respectively.

151.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 151.2.

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SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all four lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 151–4. The PMD receiver is not required to verify whether a compliant 400GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 151–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –16 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ average receive power, each lane (min) in Table 151–8) AND (compliant 400GBASE-R signal input)]	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

151.5.5 PMD lane-by-lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:3, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 151–4.

151.5.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

151.5.7 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows all of the optical transmitters to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off all of the optical transmitters so that each transmitter meets the requirements of the average launch power of the OFF transmitter in Table 151–7.

b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter in each lane.

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151.5.8 PMD lane-by-lane transmit disable function

The PMD lane-by-lane transmit disable function allows the optical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:3 for 400GBASE-FR4 and 400GBASE-LR4-6) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 151–7.

b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_*i* variable to one, turning off the optical transmitter in each lane.

If the PMD lane-by-lane transmit disable function is not implemented in MDIO, an alternative method shall be provided to independently disable each transmit lane for testing purposes.

151.5.9 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

151.5.10 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

151.5.11 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

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151.6 Wavelength-division-multiplexed lane assignments

The wavelength range for each lane of the 400GBASE-FR4 and 400GBASE-LR4-6 PMDs is defined in Table 151–5. The 400GBASE-FR4 and 400GBASE-LR4-6 center wavelengths are members of the CWDM wavelength grid defined in ITU-T G.694.2 and are spaced at 20 nm.

Table 151–5—400GBASE-FR4 and 400GBASE-LR4-6 wavelength-division-multiplexed lane assignments

Lane	Center wavelength	Wavelength range
L_0	1271 nm	1264.5 to 1277.5 nm
L_1	1291 nm	1284.5 to 1297.5 nm
L_2	1311 nm	1304.5 to 1317.5 nm
L_3	1331 nm	1324.5 to 1337.5 nm

NOTE—There is no requirement to associate a particular electrical lane with a particular optical lane, as the PCS is capable of receiving lanes in any arrangement.

151.7 PMD to MDI optical specifications for 400GBASE-FR4 and 400GBASE-LR4-6

The operating ranges for the 400GBASE-FR4 and 400GBASE-LR4-6 PMDs are defined in Table 151–6. A 400GBASE-FR4 or 400GBASE-LR4-6 compliant PMD operates on type G.652.B, G.652.D, G.657.A1, or G.657.A2 single-mode fibers according to the specifications defined in Table 151–14. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 400GBASE-FR4 PMD operating at 2.5 km meets the operating range requirement of 2 m to 2 km).

The 400GBASE-LR4-6 PMD interoperates with the 400GBASE-FR4 PMD provided that the channel guidelines defined in 151.12 are met.

Table 151–6—400GBASE-FR4 and 400GBASE-LR4-6 operating ranges

PMD type	Required operating range
400GBASE-FR4	2 m to 2 km
400GBASE-LR4-6	2 m to 6 km

151.7.1 400GBASE-FR4 and 400GBASE-LR4-6 transmitter optical specifications

The 400GBASE-FR4 transmitter shall meet the specifications defined in Table 151–7 per the definitions in 151.8. The 400GBASE-LR4-6 transmitter shall meet the specifications defined in Table 151–7 per the definitions in 151.8.

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Table 151–7—400GBASE-FR4 and 400GBASE-LR4-6 transmit characteristics

Description	400GBASE-FR4	400GBASE-LR4-6	Unit
Signaling rate, each lane (range)	53.125 ± 100 ppm		GBd
Modulation format	PAM4		—
Lane wavelengths (range)	1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5		nm
Side-mode suppression ratio (SMSR), (min)	30		dB
Total average launch power (max)	10.4	11.1	dBm
Average launch power, each lane (max)	4.4	5.1	dBm
Average launch power, each lane[a] (min)	–3.2	–2.7	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	3.7	4.4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min) for TDECQ <1.4 dB for 1.4 dB ≤ TDECQ ≤ 3.4 dB	 –0.2 –1.6 + TDECQ	 0.3 –1.1 + TDECQ	 dBm dBm
Difference in launch power between any two lanes (OMA_{outer}) (max)	3.9	4	dB
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	3.4	3.4	dB
Transmitter eye closure for PAM4 (TECQ), each lane (max)	3.4	3.4	dB
| TDECQ – TECQ | (max)	2.5	2.5	dB
Over/under-shoot (max)	22	22	%
Transmitter power excursion (max)	1.8	2.5	dBm
Extinction ratio, each lane (min)	3.5	3.5	dB
Transmitter transition time (max)	17		ps
Average launch power of OFF transmitter, each lane (max)	–16	–16	dBm
$RIN_{17.1}OMA$ (max)	–136	—	dB/Hz
$RIN_{15.6}OMA$ (max)	—	–136	dB/Hz
Optical return loss tolerance (max)	17.1	15.6	dB
Transmitter reflectance[b] (max)	–26		dB

[a] Average launch power, each lane (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b] Transmitter reflectance is defined looking into the transmitter.

The values for OMA_{outer} each lane (min) in Table 151–7 vary with TDECQ. The relationships are illustrated in Figure 151–3 along with the values for OMA_{outer} each lane (max).

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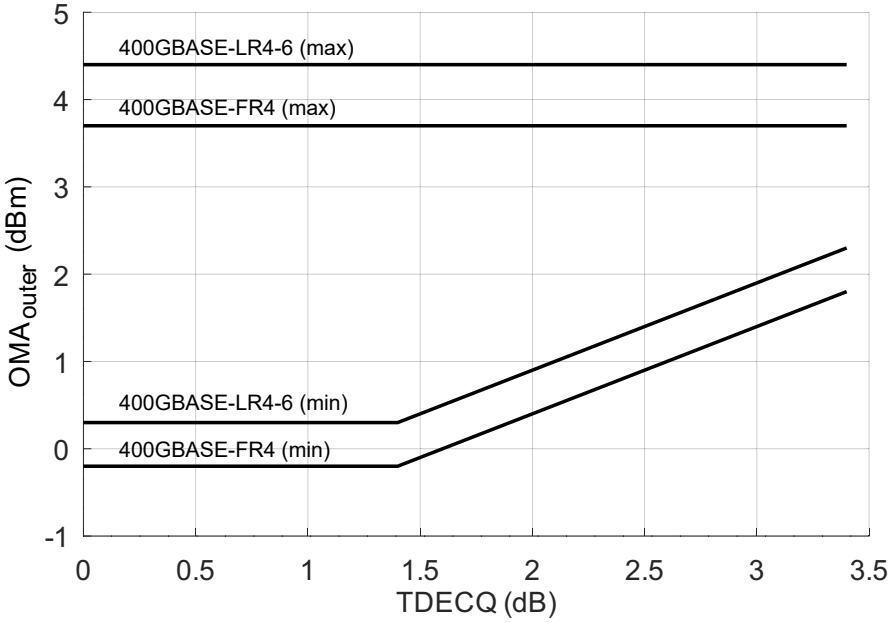

Figure 151–3—OMA_{outer} each lane (max) and OMA_{outer} each lane (min) versus TDECQ for 400GBASE-FR4 and 400GBASE-LR4-6

151.7.2 400GBASE-FR4 and 400GBASE-LR4-6 receive optical specifications

The 400GBASE-FR4 receiver shall meet the specifications in Table 151–8 per the definitions in 151.8. The 400GBASE-LR4-6 receiver shall meet the specifications in Table 151–8 per the definitions in 151.8.

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Table 151–8—400GBASE-FR4 and 400GBASE-LR4-6 receive characteristics

Description	400GBASE-FR4	400GBASE-LR4-6	Unit
Signaling rate, each lane (range)	53.125 ± 100 ppm		GBd
Modulation format	PAM4		—
Lane wavelengths (range)	1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5		nm
Damage threshold[a], each lane	5.4	6.1	dBm
Average receive power, each lane (max)	4.4	5.1	dBm
Average receive power, each lane[b] (min)	–7.2	–9	dBm
Receive power (OMA_{outer}), each lane (max)	3.7	4.4	dBm
Difference in receive power between any two lanes (OMA_{outer}) (max)	4.1	4.3	dB
Receiver reflectance (max)	–26		dB
Receiver sensitivity (OMA_{outer}), each lane (max) for TECQ < 1.4 dB for 1.4 dB ≤ TECQ ≤ 3.4 dB	 –4.6 –6 + TECQ	 –6.8 –8.2 + TECQ	 dBm dBm
Stressed receiver sensitivity (OMA_{outer}), each lane[c] (max)	–2.6	–4.8	dBm
Conditions of stressed receiver sensitivity test:[d]			
Stressed eye closure for PAM4 (SECQ), lane under test	3.4	3.4	dB
OMA_{outer} of each aggressor lane	1.4	–0.4	dBm

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
[b] Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] Measured with conformance test signal at TP3 (see 151.8.13) for the BER specified in 151.1.1.
[d] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

The values for receiver sensitivity (OMA_{outer}), each lane (max) in Table 151–8 vary depending on the value of TECQ for the test source used for measurement. Figure 151–4 illustrates this.

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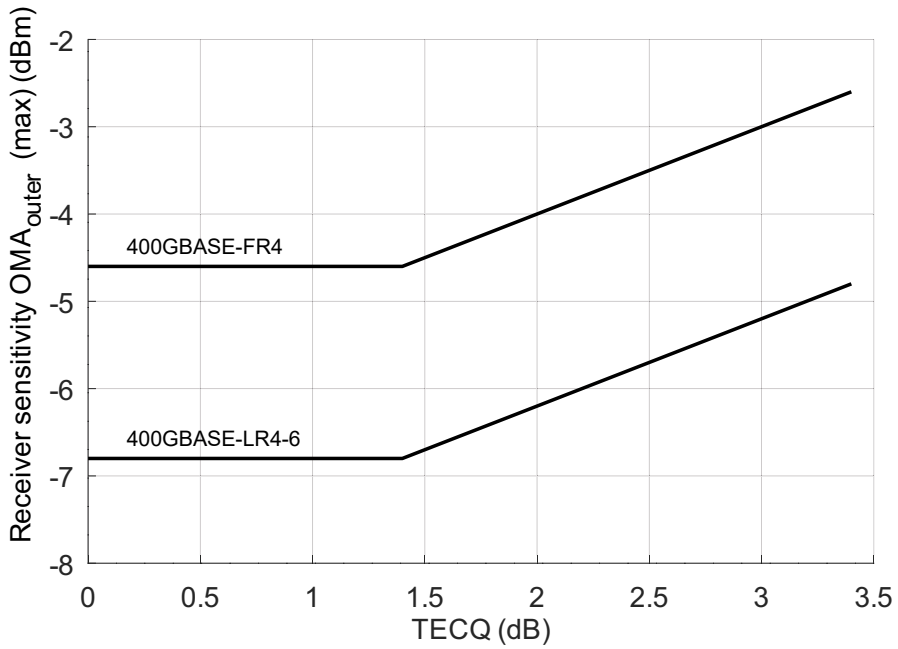

Figure 151–4—Receiver sensitivity (OMA_{outer}), each lane (max) for 400GBASE-FR4 and 400GBASE-LR4-6

151.7.3 400GBASE-FR4 and 400GBASE-LR4-6 illustrative link power budgets

Illustrative power budgets and penalties for 400GBASE-FR4 and 400GBASE-LR4-6 channels are shown in Table 151–9.

Table 151–9—400GBASE-FR4 and 400GBASE-LR4-6 illustrative link power budgets

Parameter	400GBASE-FR4	400GBASE-LR4-6	Unit
Power budget (for maximum TDECQ)	7.8	10.5	dB
Operating distance	2	6	km
Channel insertion loss[a]	4	5	dB
Maximum discrete reflectance[b]	–35[c]	–35[d]	dB
Allocation for penalties[e] (for maximum TDECQ)	3.8	4.2	dB
Additional insertion loss allowed[f]	0	1.3	dB

[a] The channel insertion loss is calculated using the maximum distance specified in Table 151–6 and fiber attenuation of 0.5 dB/km plus an allocation for connection and splice loss given in 151.11.2.1.
[b] See 151.11.2.2 for details and specifications as a function of the number of discrete reflectances within the channel.
[c] Maximum value for each discrete reflectance with 4 discrete reflectances above –55 dB within the channel.
[d] Maximum value for each discrete reflectance with 6 discrete reflectances above –55 dB within the channel.
[e] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[f] The additional insertion loss may be allocated for cable, connectors or splices, provided the fiber optic cabling (channel) characteristics in 151.11 are met.

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The values of transmitter OMA_{outer} (max), transmitter OMA_{outer} (min) versus TDECQ, and receiver sensitivity (OMA_{outer}) (max) versus TECQ are illustrated in Figure 151–5 for 400GBASE-FR4 and in Figure 151–6 for 400GBASE-LR4-6.

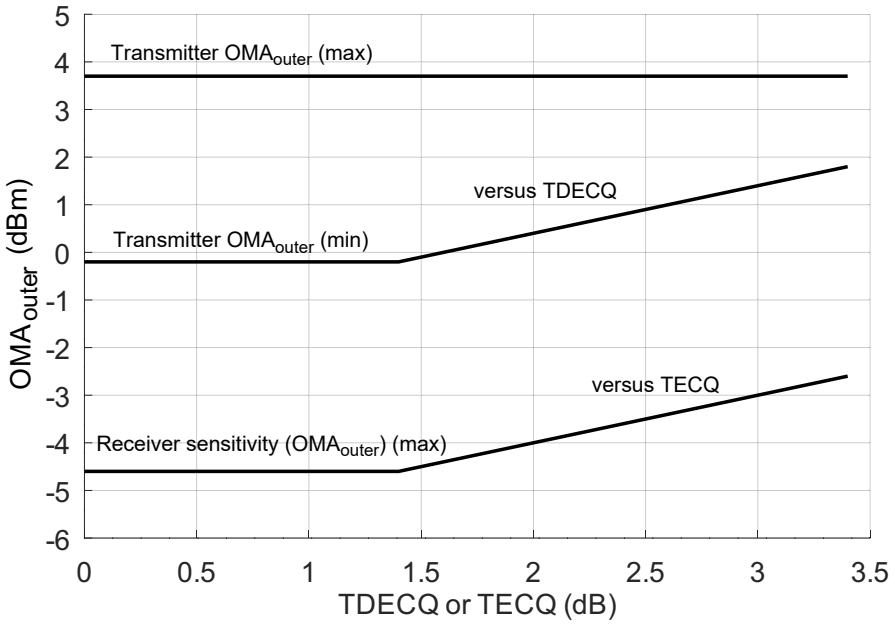

Figure 151–5—Transmitter OMA_{outer} each lane versus TDECQ and receiver sensitivity (OMA_{outer}) each lane versus TECQ for 400GBASE-FR4

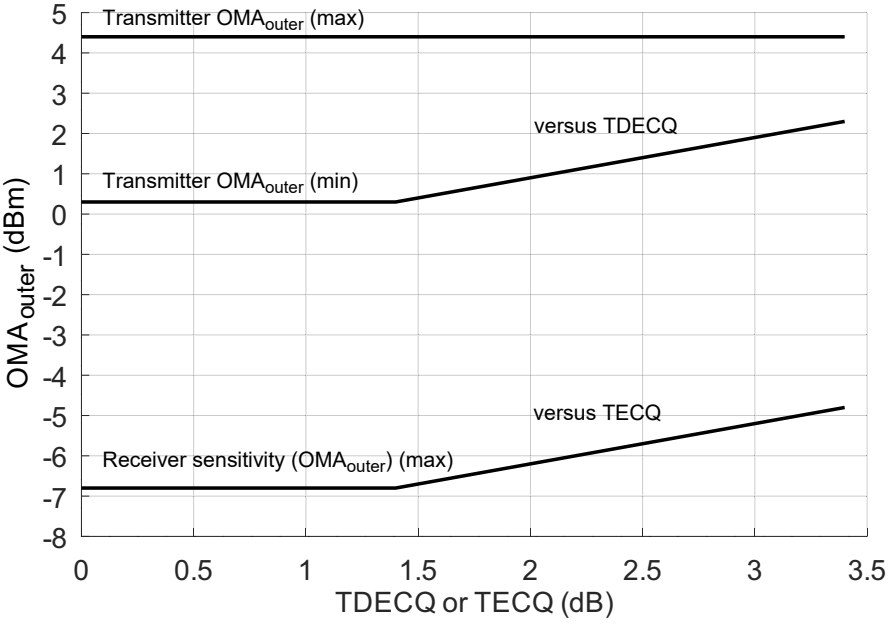

Figure 151–6—Transmitter OMA_{outer} each lane versus TDECQ and receiver sensitivity (OMA_{outer}) each lane versus TECQ for 400GBASE-LR4-6

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151.8 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

151.8.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 151–11 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 151–11 may be used to perform that test. The test patterns used in this clause are shown in Table 151–10.

Table 151–10—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle	119.2.4.9
6	SSPRQ	120.5.11.2.3

Table 151–11—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 400GBASE-R signal	151.8.2
Side mode suppression ratio	3, 5, 6 or valid 400GBASE-R signal	151.8.2
Average optical power	3, 5, 6 or valid 400GBASE-R signal	151.8.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	151.8.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	151.8.5
Transmitter eye closure for PAM4 (TECQ)	6	151.8.6
Over/under-shoot	6	151.8.7
Transmitter power excursion	6	151.8.8
Extinction ratio	4 or 6	151.8.9
Transmitter transition time	Square wave or 6	151.8.10
$RIN_{17.1}OMA$ and $RIN_{15.6}OMA$	Square wave	151.8.11
Receiver sensitivity	3 or 5	151.8.12
Stressed receiver conformance test signal calibration	6	151.8.13
Stressed receiver sensitivity	3 or 5	151.8.13

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151.8.2 Wavelength and side mode suppression ratio (SMSR)

The wavelength and SMSR of each optical lane shall be within the ranges given in Table 151–7 if measured per IEC 61280-1-3. The lane under test is modulated using the test pattern defined in Table 151–11.

151.8.3 Average optical power

The average optical power of each lane shall be within the limits given in Table 151–7 if measured using the methods given in IEC 61280-1-1, with the sum of the optical power from all of the lanes not under test below –30 dBm, per the test setup in Figure 53–6.

151.8.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} of each lane shall be within the limits given in Table 151–7. OMA_{outer} is measured using a test pattern specified for OMA_{outer} in Table 151–11, using the measurement method in 122.8.4.

151.8.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

The TDECQ of each lane shall be within the limits given in Table 151–7 if measured using the test setup specified in 122.8.5.1, with the optical channel specified in 151.8.5.1, the measurement method in 121.8.5.3, and the reference equalizer in 122.8.5.4, with the following exceptions:

— The signaling rate of the test pattern generator is as given in Table 151–7 and uses a test pattern specified for TDECQ in Table 151–11.

— The combination of O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 26.5625 GHz with a fourth-order Bessel-Thomson response to at least 1.3 × 53.125 GHz and at frequencies above 1.3 × 53.125 GHz the response should not exceed –20 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

— The normalized noise power density spectrum, $N(f)$ in Equation (121–9), is equivalent to white noise filtered by a fourth-order Bessel-Thomson response filter with a 3 dB bandwidth of 26.5625 GHz.

151.8.5.1 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 151–12.

Table 151–12—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]	Max mean DGD
	Minimum	Maximum			
400GBASE-FR4	$0.046\times\lambda\times[1-(1324/\lambda)^4]$	$0.046\times\lambda\times[1-(1300/\lambda)^4]$	Minimum	17.1 dB	0.8 ps
400GBASE-LR4-6	$0.138\times\lambda\times[1-(1324/\lambda)^4]$	$0.138\times\lambda\times[1-(1300/\lambda)^4]$	Minimum	15.6 dB	0.8 ps

[a] The dispersion is measured for the wavelength of the transmitter lane under test (λ in nm). The coefficient assumes 2 km for 400GBASE-FR4 and 6 km for 400GBASE-LR4-6.
[b] There is no intent to stress the sensitivity of the O/E converter associated with the oscilloscope.
[c] The optical return loss is applied at TP2.

A 400GBASE-FR4 or 400GBASE-LR4-6 transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 151–12 for the wavelength of the transmitter lane under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

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To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss specified in Table 151–12. The state of polarization of the back reflection is adjusted to create the greatest RIN.

The mean DGD of the channel is to be less than the value specified in Table 151–12.

151.8.6 Transmitter eye closure for PAM4 (TECQ)

The transmitter eye closure for PAM4 (TECQ) is a measure of the optical transmitter's eye closure at TP2. The TECQ of each lane shall be within the limits given in Table 151–7 if measured using a test pattern specified for TECQ in Table 151–11. The TECQ of each lane is measured using the methods specified for TDECQ in 151.8.5, except that the test fiber is not used.

151.8.7 Over/under-shoot

The over/under-shoot of each lane shall be within the limits given in Table 151–7 if measured using a test pattern specified for over/under-shoot in Table 151–11.

Overshoot and undershoot are measured using the waveform captured for the TDECQ test (see 151.8.5) and the waveform captured for the TECQ test (see 151.8.6), but without the reference equalizer being applied in each case.

Overshoot and undershoot are calculated using the methods in 140.7.7.

151.8.8 Transmitter power excursion

The transmitter power excursion of each lane shall be within the limits given in Table 151–7 if measured using a test pattern specified for transmitter power excursion in Table 151–11.

Transmitter power excursion is measured using the waveforms captured for the TECQ test (see 151.8.6), but without the reference equalizer being applied. Transmitter power excursion is defined as:

$$\text{Transmitter power excursion} = \max\left(P_{max} - P_{average}, P_{average} - P_{min}\right)$$

where

P_{max} and P_{min}	are defined in 140.7.7
$P_{average}$	is the average optical power of each lane defined in 151.8.3

151.8.9 Extinction ratio

The extinction ratio of each lane shall be within the limits given in Table 151–7 if measured using a test pattern specified for extinction ratio in Table 151–11 with the sum of the optical power from all of the lanes not under test being below –30 dBm, or if other lanes are operating, a suitable optical filter may be used to separate the lane under test. The extinction ratio of a PAM4 optical signal is defined as the ratio of the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 122–3.

151.8.10 Transmitter transition time

The transmitter transition time of each lane shall be within the limits given in Table 151–7 if measured using a test pattern specified for transmitter transition time in Table 151–11.

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Transmitter transition time is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer} or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling edges respectively, as measured through an O/E converter and oscilloscope with response defined as follows. The combined response of the O/E converter and oscilloscope has a 3 dB bandwidth of approximately 26.5625 GHz with a fourth-order Bessel-Thomson response to at least 1.3 × 53.125 GHz. At frequencies above 1.3 × 53.125 GHz the response should not exceed –20 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The 0% level and the 100% level are P_0 and P_3 as defined by the OMA_{outer} measurement procedure (see 151.8.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence and the falling edge is that within the 33333000000 symbol sequence.

151.8.11 Relative intensity noise ($RIN_{17.1}OMA$ and $RIN_{15.6}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 17.1 dB for 400GBASE-FR4 and 15.6 dB for 400GBASE-LR4-6.

b) Each lane may be tested individually with the sum of the optical power from all of the lanes not under test being below –30 dBm, or if other lanes are operating, a suitable optical filter may be used to separate the lane under test.

c) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 53.125 GHz).

d) The test pattern is according to Table 151–11.

151.8.12 Receiver sensitivity

The receiver sensitivity (OMA_{outer}) of each lane shall be within the limits given in Table 151–8 if measured using a test pattern specified for receiver sensitivity in Table 151–11.

The conformance test signal applied at TP3 meets the requirements for a 400GBASE-FR4 or 400GBASE-LR4-6 transmitter followed by an attenuator. An optical demultiplexer may be used to separate the lane having the wavelength for the lane under test as specified in Table 151–8 for calibrating the TECQ.

The TECQ of the conformance test signal is measured according to 151.8.5, except that the test fiber is not used. The measured value of TECQ is then used to calculate the limit for receiver sensitivity (OMA_{outer}) as specified in Table 151–8.

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151.8.13 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 151–8 if measured using the method defined in 122.8.10, with the following exceptions:

- The SECQ of the stressed receiver conformance test signal is measured according to 151.8.5, except that the test fiber is not used. The transition time of the stressed receiver conformance test signal is no greater than the value specified in Table 151–7.
- With the Gaussian noise generator on and the sinusoidal jitter and sinusoidal interferer turned off, the $RIN_x OMA$ of the SRS test source (where x is the value for optical return loss tolerance from Table 151–7) shall be no greater than the value specified in Table 151–7.
- An example stressed receiver conformance test setup is shown in Figure 122–8; however, alternative test setups that generate equivalent stress conditions may be used.
- The signaling rate of the test pattern generator and the extinction ratio of the E/O converter are as given in Table 151–7.
- The values of over/under-shoot and transmitter power excursion of the stressed receiver conformance test signal are within the limits specified in Table 151–7.
- The required values of the "Stressed receiver sensitivity (OMA_{outer}), each lane (max)", "Stressed eye closure for PAM4 (SECQ), lane under test" and "OMA_{outer} of each aggressor lane" are as given in Table 151–8.

151.9 Safety, installation, environment, and labeling

151.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

151.9.2 Laser safety

400GBASE-FR4 and 400GBASE-LR4-6 optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[249]

151.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

[249]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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151.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 400GBASE-FR4 or 400GBASE-LR4-6 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause are met.

151.9.5 Electromagnetic emission

A system integrating a 400GBASE-FR4 or 400GBASE-LR4-6 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

151.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

151.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 400GBASE-FR4).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 151.9.2.

151.10 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 151–7.

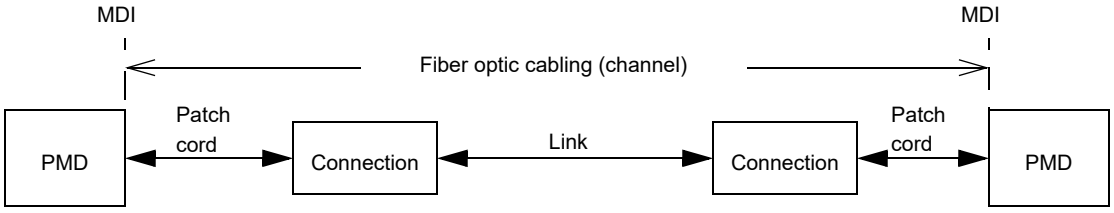

Figure 151–7—Fiber optic cabling model

The channel insertion loss is given in Table 151–13. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards..

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Table 151–13—Fiber optic cabling (channel) characteristics

Description	400GBASE-FR4	400GBASE-LR4-6	Unit
Operating distance (max)	2	6	km
Channel insertion loss[a, b](max)	4	6.3	dB
Channel insertion loss (min)	0	0	dB
Positive dispersion[b] (max)	6.6	19.9	ps/nm
Negative dispersion[b] (min)	–11.7	–35.2	ps/nm
DGD_max[c]	2.3	4	ps
Optical return loss (min)	25	22	dB

[a] These channel insertion loss values include cable, connectors, and splices.
[b] Over the wavelength range 1264.5 nm to 1337.5 nm for 400GBASE-FR4 and 400GBASE-LR4-6.
[c] Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

151.11 Characteristics of the fiber optic cabling (channel)

The 400GBASE-FR4 and 400GBASE-LR4-6 fiber optic cabling shall meet the specifications defined in Table 151–13. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

151.11.1 Optical fiber cable

The optical fiber cable requirements are satisfied by cables containing ITU-T G.652.B (dispersion unshifted), type G.652.D (low water peak, dispersion unshifted), or type G.657.A1, or type G.657.A2 (bend insensitive) fibers, or the requirements in Table 151–14 where they differ.

Table 151–14—Optical fiber and cable characteristics

Description	Value	Unit
Nominal fiber specification wavelength	1310	nm
Cabled optical fiber attenuation (max)	0.47[a] or 0.5[b]	dB/km
Zero dispersion wavelength (λ_0)	$1300 \leq \lambda_0 \leq 1324$	nm
Dispersion slope (max) (S_0)	0.092	ps/nm^2 km

[a] The 0.47 dB/km at 1264.5 nm attenuation for optical fiber cables is derived from Appendix I of ITU-T G.695.
[b] The 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA 568-C.3.

151.11.2 Optical fiber connection

An optical fiber connection, as shown in Figure 151–7, consists of a mated pair of optical connectors.

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151.11.2.1 Connection insertion loss

The maximum link distance for 400GBASE-LR4-6 is based on an allocation of 2 dB total connection and splice loss. For example, this allocation supports four connections with an average insertion loss per connection of 0.5 dB. The maximum link distance for 400GBASE-FR4 is based on an allocation of 3 dB total connection and splice loss. Connections with different loss characteristics may be used provided the requirements of Table 151–13 are met.

151.11.2.2 Maximum discrete reflectance

The maximum value for each discrete reflectance shall be less than or equal to the value shown in Table 151–15 corresponding to the number of discrete reflectances above –55 dB within the channel. For numbers of discrete reflectances in between two numbers shown in the table, the lower of the two corresponding maximum discrete reflectance values applies.

Table 151–15—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance		Unit
	400GBASE-FR4	400GBASE-LR4-6	
1	–25	–22	dB
2	–31	–29	dB
4	–35	–33	dB
6	–38	–35	dB
8	–40	–37	dB
10	–41	–39	dB

151.11.3 Medium Dependent Interface (MDI) requirements

The 400GBASE-FR4 or 400GBASE-LR4-6 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 151–7). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 151.5.1, not at the MDI.

151.12 Interoperation between 400GBASE-LR4-6 and 400GBASE-FR4

The 400GBASE-LR4-6 and 400GBASE-FR4 PMDs can interoperate with each other (over an engineered link) provided that the fiber optic cabling (channel) characteristics for 400GBASE-FR4 are met, with the

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exception of the maximum and minimum channel insertion loss values, which are given in Table 151–16 for the two link directions separately. Attenuators may be used to achieve the required losses.

Table 151–16—Channel insertion loss for interoperation between 400GBASE-LR4-6 and 400GBASE-FR4

Direction	Min loss	Max loss	Unit
400GBASE-LR4-6 transmitter to 400GBASE-FR4 receiver	0.7	4.5	dB
400GBASE-FR4 transmitter to 400GBASE-LR4-6 receiver	0	5.8	dB

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151.13 Protocol implementation conformance statement (PICS) proforma for Clause 151, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-FR4 and 400GBASE-LR4-6[250]

151.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 151, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-FR4 and 400GBASE-LR4-6, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

151.13.2 Identification

151.13.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

151.13.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 151, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-FR4 and 400GBASE-LR4-6
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[250]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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151.13.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*FR4	400GBASE-FR4	151.7	Device supports requirements for 400GBASE-FR4 PHY	O.1	Yes [ ] No [ ]
*LR4-6	400GBASE-LR4-6	151.7	Device supports requirements for 400GBASE-LR4-6 PHY	O.1	Yes [ ] No [ ]
*INS	Installation / cable	151.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	151.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	151.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	151.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	151.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	151.4	Registers and interface supported	O	Yes [ ] No [ ]

151.13.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-FR4 and 400GBASE-LR4-6

151.13.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 400GBASE-R PCS and PMA	151.1		M	Yes [ ]
F2	Integration with management functions	151.1		O	Yes [ ] No [ ]
F3	Bit error ratio	151.1.1	Meets the BER specified in 151.1.1	M	Yes [ ]
F4	Transmit function	151.5.2	Conveys symbols from PMD service interface to MDI	M	Yes [ ]
F5	Optical multiplexing and delivery to the MDI	151.5.2	Optically multiplexes the four optical signals for delivery to the MDI	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F6	Mapping between optical signal and logical signal for transmitter	151.5.2	Optical power levels from lowest to highest correspond to tx_symbol values zero, one, two, and three, respectively	M	Yes [ ]
F7	Receive function	151.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]
F8	Conversion of four optical signals to four electrical signals	151.5.3	For delivery to the PMD service interface	M	Yes [ ]
F9	Mapping between optical signal and logical signal for receiver	151.5.3	Optical power levels from lowest to highest correspond to rx_symbol values zero, one, two, and three, respectively	M	Yes [ ]
F10	Global Signal Detect function	151.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F11	Global Signal Detect behavior	151.5.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all four lanes	M	Yes [ ]
F12	Lane-by-lane Signal Detect function	151.5.5	Sets PMD_signal_detect_*i* values on a lane-by-lane basis per requirements of Table 151–4	MD:O	Yes [ ] No [ ] N/A [ ]
F13	PMD reset function	151.5.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

151.13.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	151.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	151.5.7	Disables all of the optical transmitters with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD lane-by-lane transmit disable function	151.5.8	Disables the optical transmitter via MDIO on the lane associated with the PMD_transmit_disable_*i* variable	MD:O.2	Yes [ ] No [ ] N/A [ ]
M4	PMD lane-by-lane transmit disable	151.5.8	Disables each optical transmitter independently if M3 = No	O.2	Yes [ ] N/A [ ]
M5	PMD_fault function	151.5.9	Sets PMD_fault to one if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
M6	PMD_transmit_fault function	151.5.10	Sets PMD_transmit_fault to one if a local fault is detected on any transmit lane	MD:O	Yes [ ] No [ ] N/A [ ]
M7	PMD_receive_fault function	151.5.11	Sets PMD_receive_fault to one if a local fault is detected on any receive lane	MD:O	Yes [ ] No [ ] N/A [ ]

151.13.4.3 PMD to MDI optical specifications for 400GBASE-FR4

Item	Feature	Subclause	Value/Comment	Status	Support
FRF1	Transmitter meets specifications in Table 151–7	151.7.1	Per definitions in 151.8	FR4:M	Yes [ ] N/A [ ]
FRF2	Receiver meets specifications in Table 151–8	151.7.2	Per definitions in 151.8	FR4:M	Yes [ ] N/A [ ]

151.13.4.4 PMD to MDI optical specifications for 400GBASE-LR4-6

Item	Feature	Subclause	Value/Comment	Status	Support
LRF1	Transmitter meets specifications in Table 151–7	151.7.1	Per definitions in 151.8	LR4-6:M	Yes [ ] N/A [ ]
LRF2	Receiver meets specifications in Table 151–8	151.7.2	Per definitions in 151.8	LR4-6:M	Yes [ ] N/A [ ]

151.13.4.5 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	151.8	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and SMSR	151.8.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	151.8.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA measurements	151.8.4	Each lane	M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	151.8.5	Each lane	M	Yes [ ]
OM6	Transmitter eye closure for PAM4 (TECQ)	151.8.6	Each lane	M	Yes [ ]
OM7	Over/under-shoot	151.8.7	Each lane	M	Yes [ ]
OM8	Transmitter power excursion	151.8.8	Each lane	M	Yes [ ]
OM9	Extinction ratio	151.8.9	Each lane	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
OM10	Transmitter transition time	151.8.10	Each lane	M	Yes [ ]
OM11	Relative intensity noise	151.8.11	Each lane	M	Yes [ ]
OM12	Receiver sensitivity	151.8.12	Each lane	M	Yes [ ]
OM13	Stressed receiver sensitivity	151.8.13	Each lane	M	Yes [ ]

151.13.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	151.9.1	Conforms to the general safety requirements in J.2	M	Yes [ ]
ES2	Laser safety—IEC Hazard Level 1	151.9.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	151.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

151.13.4.7 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	151.11	Meets requirements specified in Table 151–13 and Table 151–14	INS:M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	151.11.2.2	Meets requirements specified in Table 151–15	INS:M	Yes [ ] N/A [ ]
OC3	MDI Requirements	151.11.3	Meets IEC 61753-1 and IEC 61753-021-2	INS:M	Yes [ ] N/A [ ]

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152. Inverse RS-FEC sublayer

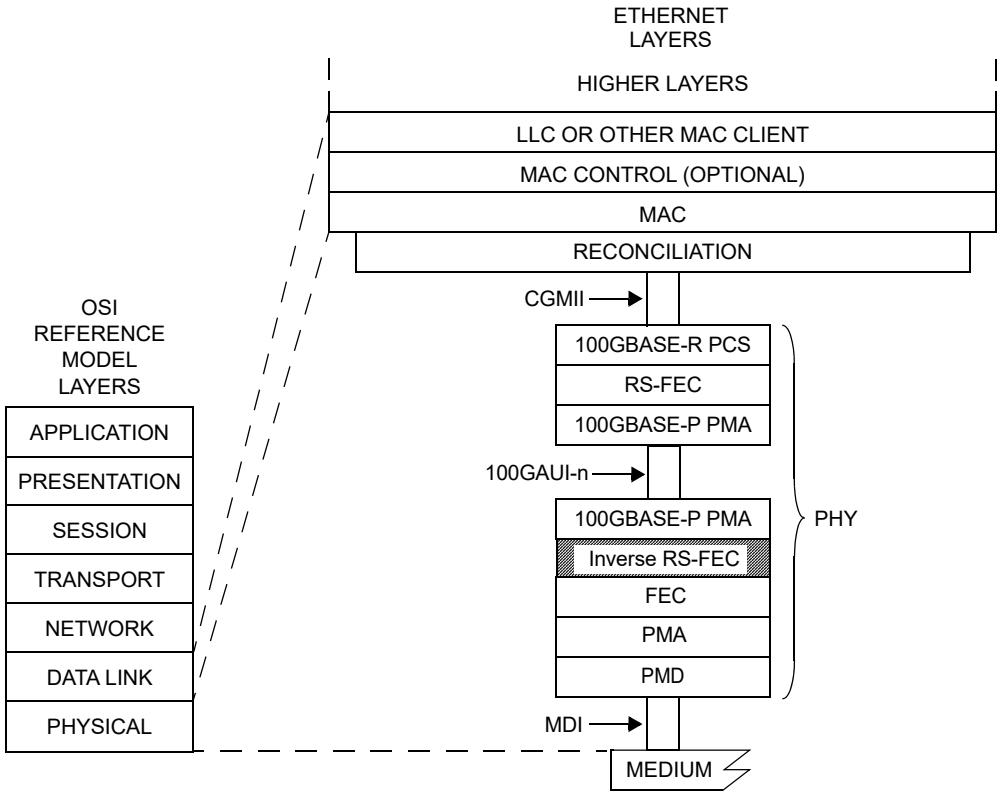
152.1 Overview

152.1.1 Scope

The Inverse RS-FEC sublayer specifies a Reed-Solomon forward error correction (RS-FEC) sublayer for 100GBASE-R, 100GBASE-P, and 100GBASE-Z PHYs. This sublayer is used in cases where the RS-FEC specified in Clause 91 is used across a physically instantiated 100GAUI-n and a different FEC is used for the PMD.

152.1.2 Position of Inverse RS-FEC in the 100GBASE-R sublayers

Figure 152–1 shows the relationship of the Inverse RS-FEC sublayer to the ISO/IEC Open System Interconnection (OSI) reference model.



100GAUI-n = 100 Gb/s n-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
Inverse RS-FEC = Inverse REED-SOLOMON FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 152–1—Inverse RS-FEC relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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152.2 Inverse RS-FEC service interface

This subclause specifies the services provided by the Inverse RS-FEC sublayer. The service interface is described in an abstract manner and does not imply any particular implementation. The Inverse RS-FEC service interface is an instance of the inter-sublayer service interface defined in 80.3. The service interface primitives are summarized as follows:

IFEC:IS_UNITDATA_*i*.request
IFEC:IS_UNITDATA_*i*.indication
IFEC:IS_SIGNAL.indication

The primitives are defined for $i = 0$ to 3. The PMA continuously sends 4 parallel bit streams to the Inverse RS-FEC sublayer, each at a nominal signaling rate of 26.5625 GBd. The Inverse RS-FEC sublayer continuously sends 4 parallel bit streams to the PMA, each at a nominal signaling rate of 26.5625 GBd.

The SIGNAL_OK parameter of the IFEC:IS_SIGNAL.indication primitive can take one of two values: OK or FAIL. The value is set to OK when align_status (see 152.6.12) is true. The value is set to FAIL when align_status is false.

152.3 PMA or FEC sublayer compatibility

The Inverse RS-FEC sublayer requires that the PMA or FEC service interface below the Inverse RS-FEC sublayer consists of twenty upstream lanes and twenty downstream lanes. The restriction that all PMA service interfaces between the RS-FEC sublayer and the PMD sublayer consist of four or fewer lanes (see 91.3) is removed below the Inverse RS-FEC sublayer.

152.4 Delay constraints

The maximum delay contributed by the Inverse RS-FEC sublayer (sum of transmit and receive delays at one end of the link) shall be no more than 40 960 bit times (80 pause_quanta or 409.6 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

152.5 Functions within the Inverse RS-FEC sublayer

The Inverse RS-FEC sublayer performs a subset of the functions defined for the RS-FEC sublayer described in Clause 91 with the Tx and Rx directions reversed. Specific limitations as compared to Clause 91 are that only RS(544,514) FEC is supported and EEE deep sleep mode is not supported. The FEC optional states in Clause 91 are mandatory for the Inverse RS-FEC sublayer.

152.5.1 Functional block diagram

A functional block diagram of the Inverse RS-FEC sublayer is shown in Figure 152–2.

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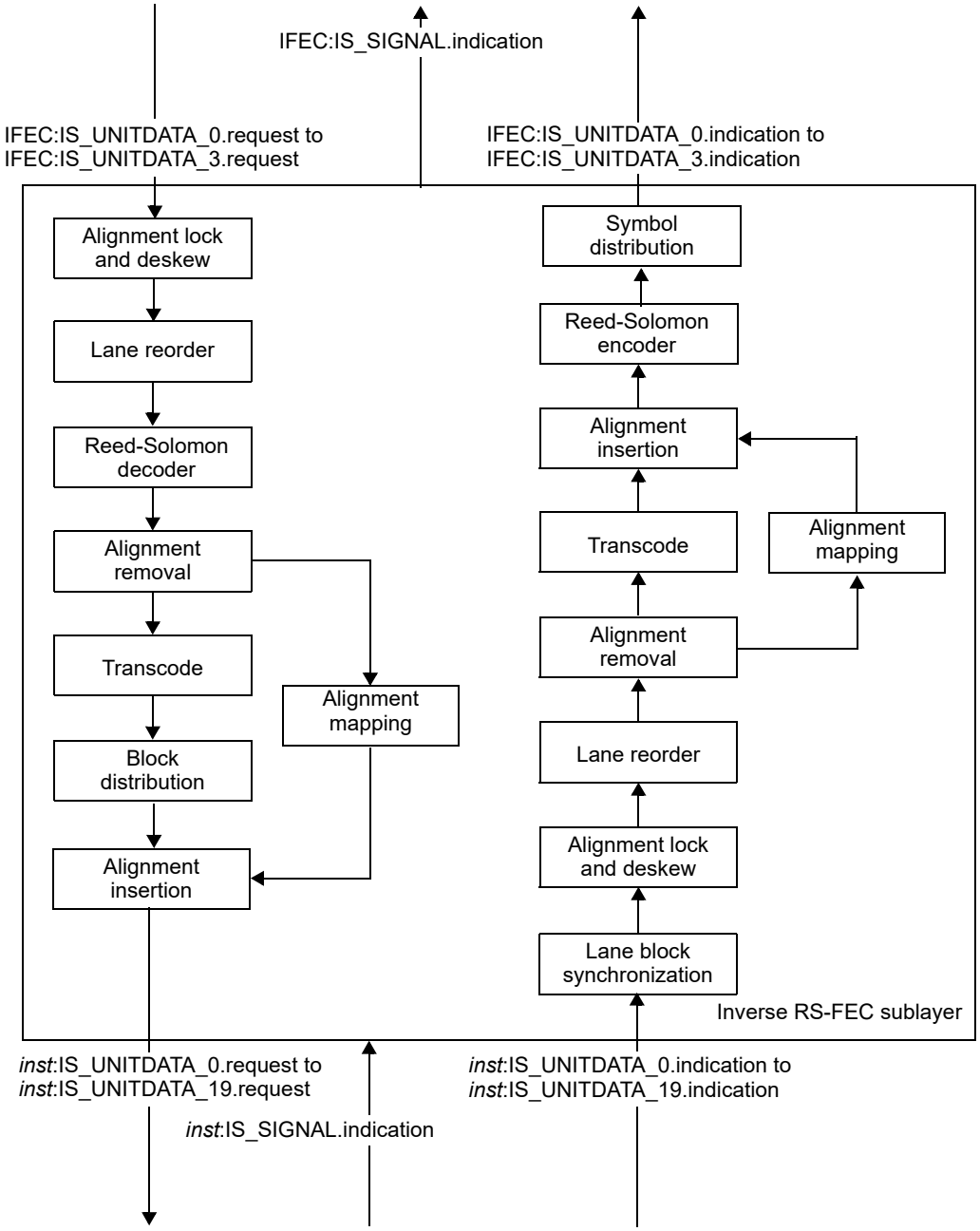

inst PMA or FEC, depending on which sublayer is below the Inverse RS-FEC sublayer

Figure 152–2—Inverse RS-FEC sublayer functional block diagram

152.5.2 Transmit function

152.5.2.1 Alignment lock and deskew

The Inverse RS-FEC transmit function forms 4 bit streams by concatenating the bits received from each of the 4 IFEC:IS_UNITDATA_*i*.request primitives in the order they are received. It obtains lock to the

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alignment markers as specified by the FEC synchronization state diagram shown in Figure 91–8. The FEC optional states and transition A in Figure 91–8 are mandatory for the Inverse RS-FEC sublayer.

After alignment marker lock is achieved on all 4 lanes, all inter-lane Skew is removed as specified by the FEC alignment state diagram shown in Figure 91–9. The Inverse RS-FEC transmit function shall support a maximum Skew of 49 ns between FEC lanes and a maximum Skew Variation of 400 ps.

152.5.2.2 Lane reorder

A particular FEC lane can be received on any of the lanes of the Inverse FEC service interface. The Inverse RS-FEC transmit function shall order the FEC lanes according to the FEC lane number (see 91.5.2.6). The FEC lane number is defined by the sequence of alignment markers that are mapped to each FEC lane.

After all FEC lanes are aligned, deskewed, and reordered, the FEC lanes are multiplexed together in the proper order to reconstruct the original stream of FEC codewords.

152.5.2.3 Reed-Solomon decoder

The Reed-Solomon decoder implements the RS(544,514) FEC decoder described in 91.5.3.3 with the exception that message symbols come from tx_scrambled rather than rx_scrambled. The optional subclause 91.5.3.3.1 is not supported for the Inverse RS-FEC sublayer.

152.5.2.4 Alignment marker removal

The first 1285 message bits in every 4096th codeword is the vector am_txmapped<1284:0> where bit 0 is the first bit received. The specific codewords that include this vector are indicated by the alignment lock and deskew function (refer to 152.5.2.1).

The vector am_txmapped shall be removed prior to transcoding.

152.5.2.5 256B/257B to 64B/66B transcoder

The transcoder extracts a group of four 66-bit blocks, tx_coded_j<65:0> where j = 0 to 3, from each 257-bit block tx_scrambled<256:0>. Bit 0 of the 257-bit block is the first bit received.

First, descramble the first 5 bits, based on reception order, of tx_scrambled<256:0> to yield tx_xcoded<256:0> as follows:

a) Set tx_xcoded<4:0> to the result of the bit-wise exclusive-OR of tx_scrambled<4:0> and tx_scrambled<12:8>.
b) Set tx_xcoded<256:5> to tx_scrambled<256:5>.

If tx_xcoded<0> is 1, tx_coded_j<65:0> for j = 0 to 3 shall be derived as follows:

a1) tx_coded_j<65:2> = tx_xcoded<(64j + 64):(64j + 1)> for j = 0 to 3.
b1) tx_coded_j<0> = 0 and tx_coded_j<1> = 1 for all j = 0 to 3.

If tx_xcoded<0> is 0 and any tx_xcoded<j + 1> = 0 for j = 0 to 3, tx_coded_j<65:0> for j = 0 to 3 shall be derived as follows:

a2) Let c be the smallest value of j such that tx_xcoded<j + 1> = 0. In other words, tx_coded_c is the first 66-bit control block in the resulting group of four blocks.

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b2) Let tx_payloads be a vector representing the payloads of the four 66-bit blocks. It is derived using the following expressions:
tx_payloads<(64*c* + 3):0> = tx_xcoded<(64*c* + 8):5>
tx_payloads<(64*c* + 7):(64*c* + 4)> = 0000 (an arbitrary value that is later replaced by s_*c*)
tx_payloads<255:(64*c* + 8)> = tx_xcoded<256:(64*c* + 9)>

c2) tx_coded_*j*<65:2> = tx_payloads<(64*j* + 63):64*j*> for *j* = 0 to 3.

d2) Let f_*c*<3:0> = tx_coded_*c*<5:2> be the scrambled first nibble (based on transmission order) of the block type field for tx_coded_*c*.

e2) Descramble f_*c*<3:0> to yield g<3:0> per the following expression where "^" denotes the exclusive-OR operation. When *c* = 0, tx_coded_(*c* – 1) corresponds to tx_coded_3 from the previous 257-bit block.
g<*i*> = f_*c*<*i*> ^ tx_coded_(*c* – 1)<*i* + 8> ^ tx_coded_(*c* – 1)<*i* + 27> for *i* = 0 to 3.

f2) The block type field may be uniquely identified by either its most or least significant nibble. Since g<3:0> is the least significant nibble of the block type field (per the transmission order), derive h<3:0> by cross-referencing to g<3:0> using Figure 82–5. For example, if g<3:0> is 0xE then h<3:0> is 0x1. If no match to g<3:0> is found, h<3:0> is set to 0000.

g2) If tx_xcoded<*j* + 1> = 0, tx_coded_*j*<0> = 1 and tx_coded_*j*<1> = 0 for *j* = 0 to 3.

h2) If tx_xcoded<*j*+1> = 1, tx_coded_*j*<0> = 0 and tx_coded_*j*<1> = 1 for *j* = 0 to 3.

i2) If h<3:0> = 0000, tx_coded_*c*<1> = 1 (invalidate synchronization header).

If tx_xcoded<0> is 0 and all tx_xcoded<*j* + 1> = 1 for *j* = 0 to 3, tx_coded_*j*<65:0> for *j* = 0 to 3 shall be derived as follows:

a3) Set *c* = 0 and h<3:0> = 0000.

b3) Let tx_payloads be a vector representing the payloads of the four 66-bit blocks. It is derived using the following expressions.
tx_payloads<(64*c* + 3):0> = tx_xcoded<(64*c* + 8):5>
tx_payloads<(64*c* + 7):(64*c* + 4)> = 0000 (an arbitrary value that is later replaced by s_*c*)
tx_payloads<255:(64*c* + 8)> = tx_xcoded<256:(64*c* + 9)>

c3) tx_coded_*j*<65:2> = tx_payloads<(64*j* + 63):(64*j*)> for *j* = 0 to 3.

d3) tx_coded_*j*<0> = 0 and tx_coded_*j*<1> = 0 for *j* = 0 and 2.

e3) tx_coded_*j*<0> = 1 and tx_coded_*j*<1> = 1 for *j* = 1 and 3.

If tx_xcoded<0> is 0, scramble h<3:0> to yield s_*c*<3:0> and assign it to tx_coded_*c* per the following expressions.

a4) s_*c*<*i*> = h<*i*> ^ tx_coded_(*c* – 1)<*i* + 12> ^ tx_coded_(*c* – 1)<*i* + 31> for *i* = 0 to 3.

b4) tx_coded_*c*<9:6> = s_*c*<3:0>.

The 66-bit blocks are transmitted in order from *j* = 0 to 3. Bit 0 of each block is the first bit transmitted.

152.5.2.6 Block distribution

After the data has been transcoded, it shall be distributed to 20 PCS lanes, one 66-bit block at a time in a round-robin distribution from the lowest to the highest numbered PCS lanes. The distribution process is shown in Figure 82–6.

152.5.2.7 Alignment marker mapping and insertion

The alignment marker mapping function compensates for the operation of the lane reorder function (refer to 152.5.2.2) to derive the PCS lane alignment markers, am_tx_*x*<65:0> for *x* = 0 to 19, from am_txmapped<1284:0> (refer to 152.5.2.4).

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The alignment markers shall be derived from am_txmapped<1284:0> in a manner that yields the same result as the following process.

Given $i = 0$ to 3, $k = 0$ to 31, and $y = i + 4k$, am_txpayloads may be derived from am_txmapped per the following expression:

am_txpayloads<i, ($10k$ + 9):$10k$> = am_txmapped<($10y$ + 9):$10y$>

The 5-bit pad am_txmapped<1284:1280> is ignored. Given $i = 0$ to 3, $j = 0$ to 4, and $x = i + 4j$, amp_tx_x may be derived from am_txpayloads by the following expression:

amp_tx_x<63:0> = am_txpayloads<i, (64j + 63):64j>

For $x = 0$ to 19, am_tx_x<65:0> is constructed as follows:

a) am_tx_x<0> = 1 and am_tx_x<1> = 0.
b) am_tx_x<25:2> is set to M_0, M_1, and M_2 as shown in Figure 82–9 using the values in Table 82–2 for PCS lane number x.
c) am_tx_x<33:26> = amp_tx_x<31:24>.
d) am_tx_x<57:34> is set to M_4, M_5, and M_6 as shown in Figure 82–9 using the values in Table 82–2 for PCS lane number x.
e) am_tx_x<65:58> = amp_tx_x<63:56>.

One vector is mapped to 20 alignment markers every 4096 Reed-Solomon codewords (see 152.5.2.4). The alignment markers are simultaneously transmitted on the 20 PCS lanes after every 16 383rd column of 20 66-bit blocks.

The alignment markers am_tx_0 to am_tx_3 shall be inserted so that they are immediately followed by tx_coded_0 to tx_coded_3, respectively, as derived from the first 257-bit block following am_txmapped. Similarly am_tx_4 to am_tx_7 are followed by the 66-bit blocks corresponding to the second 257-bit block following am_txmapped, and so on.

152.5.2.8 Transmit bit ordering

The transmit bit ordering is illustrated in Figure 152–3. This illustration shows the case where the FEC lanes appear across the IFEC:IS_UNITDATA_i.request primitives in the correct order.

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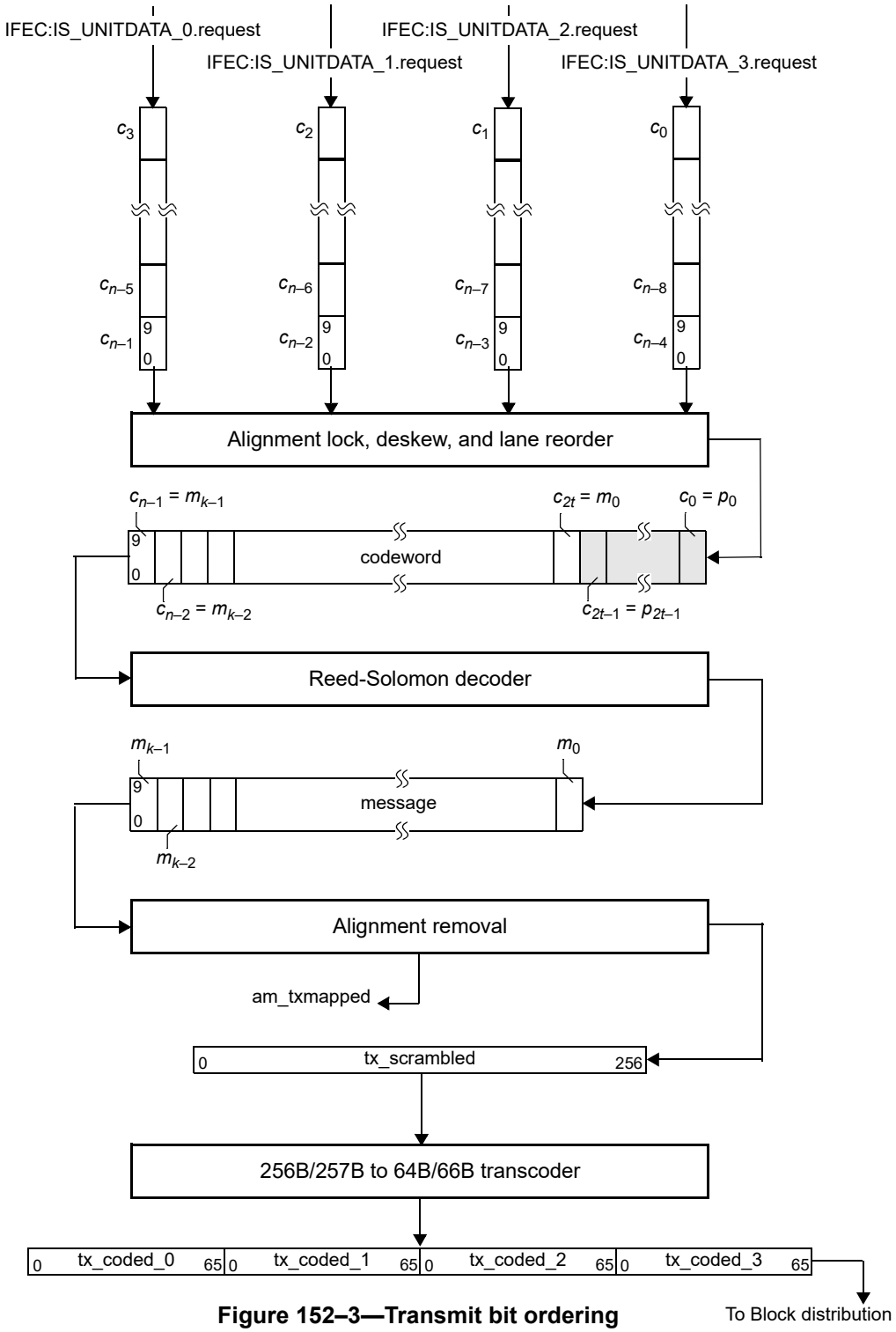

Figure 152–3—Transmit bit ordering

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152.5.3 Receive function

152.5.3.1 Lane block synchronization

The Inverse RS-FEC receive function forms 20 bit streams by concatenating the bits from each of the 20 FEC:IS_UNITDATA_*i*.indication primitives from the sublayer below in the order they are received. It obtains lock to the 66-bit blocks in each bit stream using the sync headers and outputs 66-bit blocks. Block lock is obtained as specified in the block lock state diagram shown in Figure 82–12.

152.5.3.2 Alignment lock and deskew

Once the Inverse RS-FEC receive function achieves block lock on a PCS lane, it then begins obtaining alignment marker lock as specified in the alignment marker lock state diagram shown in Figure 82–13. This process identifies the PCS lane number received on a particular lane of the service interface of the sublayer below. After alignment marker lock is achieved on all 20 lanes, all inter-lane Skew is removed as specified by the PCS deskew state diagram shown in Figure 82–14. The Inverse RS-FEC receive function shall support a maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps. Skew and Skew Variation are defined in 80.5.

152.5.3.3 Lane reorder

Any PCS lane may be received on any lane of the service interface. The Inverse RS-FEC receive function shall order the PCS lanes according to the PCS lane number.

152.5.3.4 Alignment marker removal

After all PCS lanes are aligned and deskewed, the PCS lanes are multiplexed together in the proper order to reconstruct the original stream of blocks and the alignment markers are removed from the data stream. Note that an alignment marker is always removed when am_lock is true for a given PCS lane even if it does not match the expected alignment marker value (due to a bit error, for example). Repeated alignment marker errors result in am_lock being set to false for a given PCS lane, but until that happens, it is sufficient to remove the block in the alignment marker position.

As part of the alignment marker removal process, the BIP_3 field is compared to the calculated Bit Interleaved Parity (BIP) value (see 82.2.8) for each PCS lane. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register (registers 1.230 to 1.249) is incremented by one each time the calculated BIP value does not equal the value received in the BIP_3 field. The bit error ratio in the data received from the far-end PCS can be estimated by dividing the BIP block error ratio by a factor of 1 081 344.

152.5.3.5 64B/66B to 256B/257B transcoder

The transcoder constructs a 257-bit block, rx_scrambled<256:0>, from a group of four 66-bit blocks, rx_coded_*j*<65:0> where *j* = 0 to 3. For each group of four 66-bit blocks, *j* = 3 corresponds to the most recently received block. Bit 0 in each 66-bit block is the first bit received and corresponds to the first bit of the synchronization header.

If for all *j* = 0 to 3, rx_coded_*j*<0> = 0 and rx_coded_*j*<1> = 1, rx_xcoded<256:0> shall be constructed as follows:

a) rx_xcoded<0> = 1.
b) rx_xcoded<(64*j* + 64):(64*j* + 1)> = rx_coded_*j*<65:2> for *j* = 0 to 3.

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If for all j = 0 to 3, rx_coded_j<0> ≠ rx_coded_j<1> (valid synchronization header) and for any j = 0 to 3, rx_coded_j<0> = 1 and rx_coded_j<1> = 0, rx_xcoded<256:0> shall be constructed as follows:

a1) rx_xcoded<0> = 0.
b1) rx_xcoded<j + 1> = rx_coded_j<1> for j = 0 to 3.
c1) Let c be the smallest value of j such that rx_coded_c<0> = 1. In other words, rx_coded_c is the first 66-bit control block that was received in the current group of four blocks.
d1) Let rx_payloads<(64j + 63):64j> = rx_coded_j<65:2> for j = 0 to 3.
e1) Omit rx_coded_c<9:6>, which is the second nibble (based on transmission order) of the block type field for rx_coded_c, from rx_xcoded per the following expressions:
rx_xcoded<(64c + 8):5> = rx_payloads<(64c + 3):0>
rx_xcoded<256:(64c + 9)> = rx_payloads<255:(64c + 8)>

If for any j = 0 to 3, rx_coded_j<0> = rx_coded_j<1> (invalid synchronization header), rx_xcoded<256:0> shall be constructed as follows:

a2) rx_xcoded<0> = 0.
b2) rx_xcoded<j + 1> = 1 for j = 0 to 3.
c2) Let rx_payloads<(64j + 63):64j> = rx_coded_j<65:2> for j = 0 to 3.
d2) Omit the second nibble (based on transmission order) of rx_coded_0 per the following expressions.
rx_xcoded<8:5> = rx_payloads<3:0>
rx_xcoded<256:9> = rx_payloads<255:8>

Finally, scramble the first 5 bits, based on transmission order, of rx_xcoded<256:0> to yield rx_scrambled<256:0> as follows:

a3) Set rx_scrambled<4:0> to the result of the bit-wise exclusive-OR of rx_xcoded<4:0> and rx_xcoded<12:8>.
b3) Set rx_scrambled<256:5> to rx_xcoded<256:5>.

For each 257-bit block, bit 0 shall be the first bit transmitted.

152.5.3.6 Alignment marker mapping and insertion

The alignment markers that were removed per 152.5.3.4 are re-inserted after being processed by the alignment marker mapping function. The alignment marker mapping function compensates for the operation of the symbol distribution function defined in 152.5.3.8 and rearranges the alignment marker bits so that they appear on the FEC lanes intact and in the desired sequence. This preserves the properties of the alignment markers (e.g., DC balance, transition density) and provides a deterministic pattern for the purpose of synchronization. The receive function in the RS-FEC sublayer above uses knowledge of this mapping to determine the FEC lane that is received on a given lane of the PMA service interface below the RS-FEC sublayer, to compensate for skew between FEC lanes, and to identify RS-FEC codeword boundaries.

The alignment marker mapping function operates on a group of 20 aligned and reordered alignment markers. Let am_rx_x<65:0> be the alignment marker for PCS lane x, x = 0 to 19, where bit 0 is the first bit transmitted. The alignment markers shall be mapped to am_rxmapped<1284:0> in a manner that yields the same result as the following process.

For x = 0 to 19, amp_rx_x<63:0> is constructed as follows:

a) Set y = 0 when $x \leq 3$, set y = 16 when $x \geq 16$, otherwise set $y = x$.
b) amp_rx_x<23:0> is set to M_0, M_1, and M_2 as shown in Figure 82–9 (bits 25 to 2) using the values in Table 82–2 for PCS lane number y.
c) amp_rx_x<31:24> = am_rx_x<33:26>.

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d) amp_rx_*x*<55:32> is set to M_4, M_5, and M_6 as shown in Figure 82–9 (bits 57 to 34) using the values in Table 82–2 for PCS lane number *y*.
e) amp_rx_*x*<63:56> = am_rx_*x*<65:58>.

This process replaces the fixed bytes of the alignment markers received, possibly with errors, with the values from Table 82–2. In addition it substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 1, 2, and 3 with the fixed bytes for the alignment marker corresponding to PCS lane 0. Similarly, it substitutes the fixed bytes of the alignment markers corresponding to PCS lanes 17, 18, and 19 with the fixed bytes for the alignment marker corresponding to PCS lane 16. The variable bytes BIP or CD are unchanged. This process simplifies receiver synchronization since the receiver only needs to search for the fixed bytes corresponding to PCS lane 0 on each FEC lane.

Construct a matrix of 4 rows and 320 columns, am_rxpayloads, as shown in Figure 152–4. Given $i = 0$ to 3, $j = 0$ to 4, and $x = i + 4j$, the matrix is derived per the following expression:

am_rxpayloads<*i*, (64*j* + 63):64*j*> = amp_rx_*x*<63:0>

Given $i = 0$ to 3, $k = 0$ to 31, and $y = i + 4k$, am_rxmapped may then be derived from am_rxpayloads per the following expression:

am_rxmapped<(10*y* + 9):10*y*> = am_rxpayloads<*i*, (10*k* + 9):10*k*>

A 5-bit pad is appended to the mapped alignment markers to yield the equivalent of five 257-bit blocks. The pad bits, am_rxmapped<1284:1280>, shall be set to the binary values 00101 and 11010 (the leftmost bit is assigned to the highest bit index) in an alternating pattern. In other words, if a pad value of 00101 is used for the current iteration of the mapping function, a value of 11010 is used in the next iteration and vice versa.

The result of the alignment marker mapping function is a deterministic mapping between alignment marker payloads and FEC lanes. The alignment marker payloads corresponding to PCS lanes 0, 4, 8, 12, and 16 are transmitted on FEC lane 0, the alignment marker payloads corresponding to PCS lanes 0, 5, 9, 13, and 16 are transmitted on FEC lane 1, and so on (see Figure 152–4).

As a result of this process, the BIP_3 and BIP_7 fields from normal alignment markers are carried across the link protected by FEC. These fields cannot be used to monitor errors on the link protected by FEC as 64B/66B to 256B/257B transcoding and Reed-Solomon encoding alters the bit sequence. However, these fields may again be used to monitor errors after the original bit sequence is restored, that is following Reed-Solomon decoding and 256B/257B to 64B/66B transcoding.

One group of aligned and reordered alignment markers are mapped every 20 × 16 384 66-bit blocks. This corresponds to 4096 Reed-Solomon codewords (refer to 152.5.3.7). The mapped alignment markers, am_txmapped<1284:0> shall be inserted as the first 1285 message bits to be transmitted from every 4096th codeword.

The first 257-bit block inserted after am_rxmapped shall correspond to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective lane.

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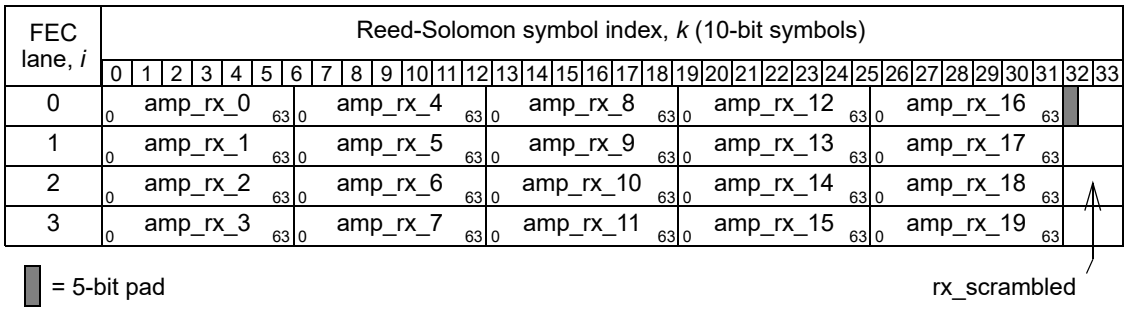

Figure 152–4—Alignment marker mapping to FEC lanes

152.5.3.7 Reed-Solomon encoder

The Reed-Solomon encoder implements the RS(544,514) FEC encoder described in 91.5.2.7. Since the encoder is used in the receive direction of transmission, the message symbols come from rs_scrambled and rx_ammapped rather than tx_scrambled and tx_ammapped.

152.5.3.8 Symbol distribution

Once the data has been Reed-Solomon encoded, it shall be distributed to 4 FEC lanes, one 10-bit symbol at a time in a round-robin distribution from the lowest to the highest numbered FEC lane. The distribution process is shown in Figure 152–5.

152.5.3.9 Receive bit ordering

The receive bit ordering is illustrated in Figure 152–5.

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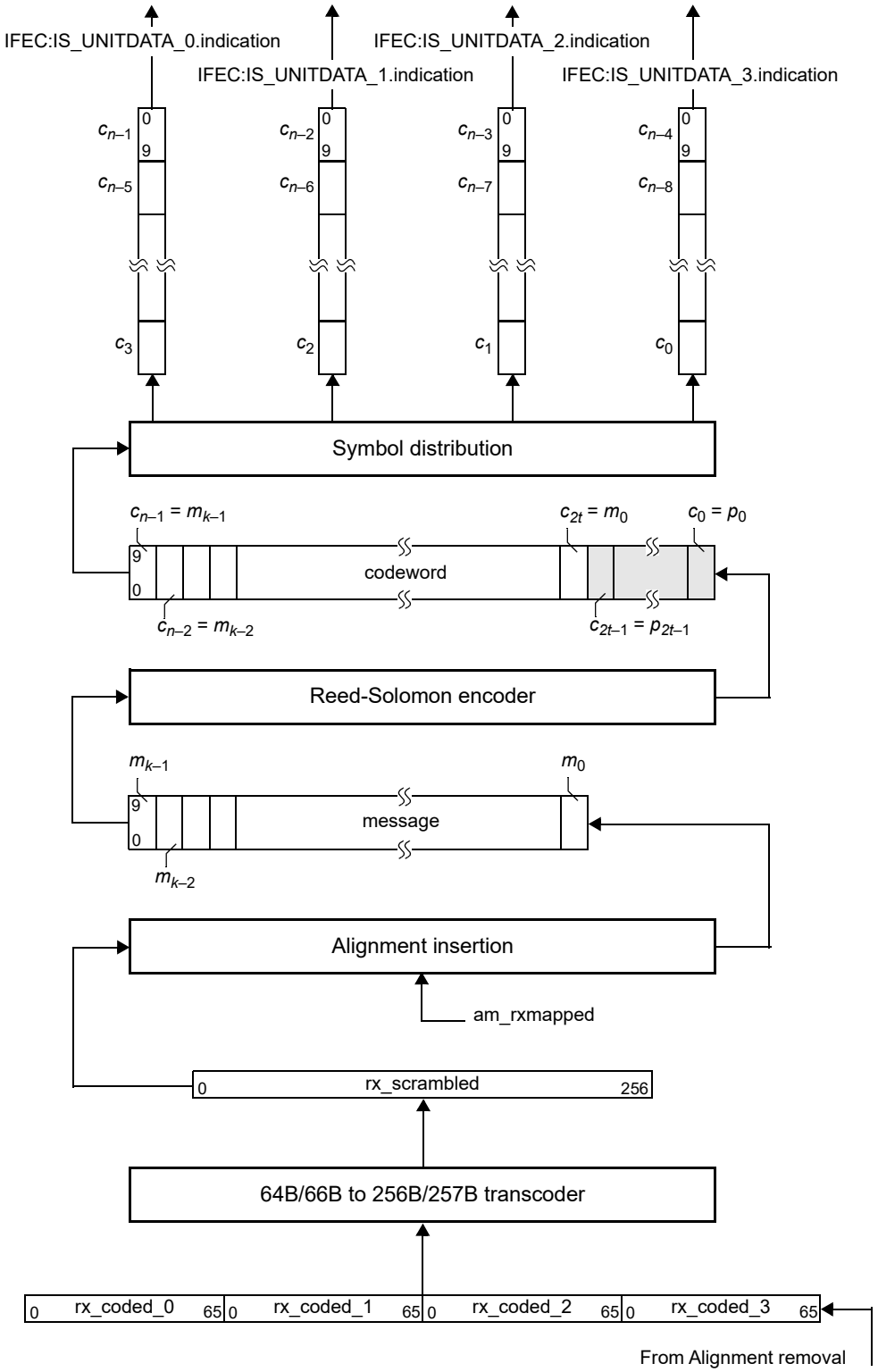

Figure 152–5—Receive bit ordering

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152.5.4 Detailed functions and state diagrams

Most functions and state diagrams are identical to those described in 91.5.4, with only the modifications to variable naming that arise from reversing the Tx and Rx directions, and omission of EEE deep sleep capability due to the fact that this sublayer only supports optical PHY types.

152.5.4.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, functions, and counters. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

152.5.4.2 State variables

152.5.4.2.1 Variables

all_locked
: A Boolean variable that is set to true when amps_lock<*x*> is true for all *x* and is set to false when amps_lock<*x*> is false for any *x*.

amp_counter_done
: Boolean variable that indicates that amp_counter has reached its terminal count.

amp_match
: Boolean variable that holds the output of the function AMP_COMPARE.

amp_valid
: Boolean variable that is set to true if the received 64-bit block is a valid alignment marker payload. The alignment marker payload, mapped to an FEC lane according to the process described in 152.5.3.6, consists of 48 known bits and 16 variable bits (the BIP_3 or CD_3 field and its complement BIP_7 or CD_7, see 82.2.7). The bits of the candidate block that are in the positions of the known bits in the alignment marker payload are compared on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles in the alignment marker payload, the candidate block is considered a valid alignment marker payload. Each FEC lane compares the candidate block to the alignment marker payload for PCS lane 0.

amps_lock<*x*>
: Boolean variable that is set to true when the receiver has detected the location of the alignment marker payload sequence for a given lane on the IFEC service interface, where *x* = 0:3.

current_pcsl
: A variable that holds the PCS lane number corresponding to the current alignment marker payload that is recognized on a given lane of the FEC service interface. It is compared to the variable first_pcsl to confirm that the location of the alignment marker payload sequence has been detected.

cw_bad
: A Boolean variable that is set to true if the Reed-Solomon decoder (see 152.5.2.3) fails to correct the current FEC codeword and is set to false otherwise.

deskew_done
: A Boolean variable that is set to true when fec_enable_deskew is set to true and the deskew process is completed. Otherwise, this variable is set to false.

fec_align_status
: A Boolean variable set by the FEC alignment process to reflect the status of FEC lane-to-lane alignment. Set to true when all lanes are synchronized and aligned and set to false when the deskew process is not complete.

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fec_alignment_valid
: Boolean variable that is set to true if all FEC lanes are aligned. FEC lanes are considered to be aligned when amps_lock<*x*> is true for all *x*, each FEC lane is locked to a unique alignment marker payload sequence (see 152.5.3.6), and the FEC lanes are deskewed. Otherwise, this variable is set to false.

fec_enable_deskew
: A Boolean variable that enables and disables the deskew process. Received bits may be discarded whenever deskew is enabled. It is set to true when deskew is enabled and set to false when deskew is disabled.

fec_lane
: A variable that holds the FEC lane number (0 to 3) received on lane *x* of the IFEC service interface when amps_lock<*x*> = true. The FEC lane number is determined by the alignment marker payloads in the 2nd, 3rd, or 4th positions of the sequence based on the mapping defined in 152.5.3.6. The 48 bits that are in the positions of the known bits in the received alignment marker payload are compared to the expected values for a given payload position and FEC lane on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles for any payload position on a given FEC lane, then the FEC lane number is assigned accordingly.

fec_optional_states
: Boolean variable that is always set to true to indicate that the optional states in the FEC synchronization state diagram in Figure 91–8 are implemented.

first_pcsl
: A variable that holds the PCS lane number that corresponds to the first alignment marker payload that is recognized on a given lane of the FEC service interface. It is compared to the PCS lane number corresponding to the second alignment marker payload that is tested.

reset
: Boolean variable that controls the resetting of the Inverse RS-FEC sublayer. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on.

restart_lock
: Boolean variable that is set by the FEC alignment process to reset the synchronization process on all FEC lanes. It is set to true after 3 consecutive uncorrected codewords are received (3_BAD state) and set to false upon entry into the LOSS_OF_ALIGNMENT state. It is also set to true when 5 Alignment Markers in a row fail to match (5_BAD state).

rx_align_status
: Boolean variable that is set by the alignment lock and deskew function (see 152.5.3.2).

signal_ok
: Boolean variable that is set based on the most recently received value of FEC:IS_SIGNAL.indication(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done
: Boolean variable that is set to true when the SLIP requested by the synchronization state diagram has been completed indicating that the next candidate 64-bit block position can be tested.

test_amp
: Boolean variable that is set to true when a candidate block position is available for testing and false when the FIND_1ST state is entered.

test_cw
: Boolean variable that is set to true when a new FEC codeword is available for decoding and is set to false when the TEST_CW state is entered.

152.5.4.2.2 Functions

The AMP_COMPARE and SLIP functions as defined in 91.5.4.2.2 are used by the Inverse RS-FEC sublayer.

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152.5.4.2.3 Counters

amp_bad_count
: Counts the number of consecutive alignment markers that don't match the expected values for a given FEC lane.

amp_counter
: This counter counts the 4096 FEC codewords that separate the ends of two consecutive normal alignment marker payload sequences. An FEC codeword is 1360 bits per FEC lane.

cw_bad_count
: Counts the number of consecutive uncorrected FEC codewords. This counter is set to zero when an FEC codeword is received and cw_bad is false for that codeword.

152.5.4.3 State diagrams

The FEC shall implement four synchronization processes as shown in Figure 91–8. The synchronization process operates independently on each lane. The synchronization state diagram determines when the FEC has detected the location of the alignment marker payload sequence in the received bit stream for a given lane of the service interface.

The FEC shall implement the alignment process as shown in Figure 91–9.

152.6 Inverse RS-FEC MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the Inverse RS-FEC. If MDIO is implemented, it shall map MDIO control bits to Inverse RS-FEC control variables as shown in Table 152–1, and MDIO status bits to Inverse RS-FEC status variables as shown in Table 152–2, and if a separated PMA (see 45.2.1) is connected to the FEC service interface it shall map additional MDIO status bits to additional RS-FEC status variables as shown in Table 152–3.

Table 152–1—MDIO/Inverse RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	IFEC variable
IFEC bypass correction enable	IFEC control	1.2200.0	IFEC_bypass_correction_enable
IFEC bypass indication enable	IFEC control	1.2200.1	IFEC_bypass_indication_enable

The following subclauses define variables that are not otherwise defined, for example for use by state diagrams.

152.6.1 IFEC_bypass_correction_enable

When this variable is set to one, the Reed-Solomon decoder performs error detection without error correction (see 152.5.2.3). When this variable is set to zero, the decoder also performs error correction. The default value of the variable is zero. This variable is mapped to the bit defined in 45.2.1.216.2 (1.2200.0).

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Table 152–2—MDIO/Inverse RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
IFEC bypass correction ability	IFEC status	1.2201.0	IFEC_bypass_correction_ability
IFEC bypass indication ability	IFEC status	1.2201.1	IFEC_bypass_indication_ability
IFEC high SER	IFEC status	1.2201.2	hi_ser
IFEC AM lock *x*, *x* = 0 to 3	IFEC status	1.2201.8:11	amps_lock<*x*>
IFEC align status	IFEC status	1.2201.14	IFEC_align_status
IFEC corrected codewords	IFEC corrected codewords counter	1.2202, 1.2203	IFEC_corrected_cw_counter
IFEC uncorrected codewords	IFEC uncorrected codewords counter	1.2204, 1.2205	IFEC_uncorrected_cw_counter
RS-FEC lane *x* mapping	IFEC lane mapping	1.2206	IFEC_lane_mapping<*x*>
IFEC symbol errors, lane 0 to 3	IFEC symbol error counter, lane 0 to 3	1.2210 to 1.2217	IFEC_symbol_error_counter_*i*

Table 152–3—MDIO/Inverse RS-FEC status variable mapping for separated PMA

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
PCS align status	RS-FEC status	1.201.15	align_status
BIP error counter, lane 0 to 19	RS-FEC BIP error counter, lane 0 to 19	1.230 to 1.249	BIP_error_counter_*i*
Lane *x* mapping	RS-FEC PCS lane *x* mapping	1.250 to 1.269	lane_mapping<*x*>
Block lock *x*	RS-FEC PCS alignment status 1 and 2	1.280, 1.281	block_lock<*x*>
Lane *x* aligned	RS-FEC PCS alignment status 3 and 4	1.282, 1.283	am_lock<*x*>

152.6.2 IFEC_bypass_indication_enable

This variable is set to one to bypass the error indication function (see 152.5.2.3) when this ability is supported. When this variable is set to zero, the decoder indicates errors to the PCS sublayer. This variable has no effect (the decoder does not bypass error indication) if IFEC_bypass_correction_enable (1.2200.0) is set to one. The default value of this variable is zero. This variable is mapped to the bit defined in 45.2.1.216.1 (1.2200.1).

152.6.3 IFEC_bypass_correction_ability

The Reed-Solomon decoder may have the option to perform error detection without error correction (see 152.5.2.3) to reduce the delay contributed by the Inverse RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass error correction. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.217.9 (1.2201.0).

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152.6.4 IFEC_bypass_indication_ability

The Reed-Solomon decoder may have the option to bypass the error indication function (see 152.5.2.3) to reduce the delay contributed by the Inverse RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass the error indication function. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.217.8 (1.2201.1).

152.6.5 hi_ser

This variable is defined when the FEC_bypass_indication_ability variable is set to one. When FEC_bypass_indication_enable is set to one, this bit is set to one if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 152.5.2.3) and is set to zero otherwise. This variable is mapped to the bit defined in 45.2.1.217.7 (1.2201.2).

152.6.6 amps_lock<*x*>

These variables are assigned by the FEC synchronization state diagram shown in Figure 91–8 (see 152.5.4.3). They are mapped to the bits defined in 45.2.1.217 (1.2201.8 to 1.2201.11 for FEC lanes 0 to 3, respectively).

152.6.7 IFEC_align_status

This variable is assigned by the FEC alignment state diagram shown in Figure 91–9 (see 152.5.4.3). It is mapped to the bit defined in 45.2.1.217.2 (1.2201.14).

152.6.8 IFEC_corrected_cw_counter

A corrected FEC codeword is a codeword that contained errors and was corrected.

The IFEC_corrected_cw_counter is a 32-bit counter that counts once for each corrected FEC codeword processed when IFEC_align_status is true. This variable is mapped to the registers defined in 45.2.1.218 (1.2202, 1.2203).

152.6.9 IFEC_uncorrected_cw_counter

An uncorrected FEC codeword is a codeword that contains errors (when the bypass correction feature is supported and enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled).

The IFEC_uncorrected_cw_counter is a 32-bit counter that counts once for each uncorrected FEC codeword processed when IFEC_align_status is true. This variable is mapped to the registers defined in 45.2.1.219 (1.2204, 1.2205).

152.6.10 IFEC_lane_mapping<*x*>

When the Inverse RS-FEC transmit function detects and locks to an alignment marker payload on the service interface lane *x*, the FEC lane number corresponding to the detected alignment marker payload is assigned to the variable IFEC_lane_mapping<*x*>. These variables are mapped to the register defined in 45.2.1.220 (1.2206).

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152.6.11 IFEC_symbol_error_counter_*i*

IFEC_symbol_error_counter_*i*, where *i* = 0 to 3, is a 32-bit counter that counts once for each 10-bit symbol corrected on FEC lane *i* when IFEC_align_status is true. These variables are mapped to the registers defined in 45.2.1.221 and 45.2.1.222 (1.2210 to 1.2217).

152.6.12 align_status

This variable is assigned the value of rx_align_status as defined by the PCS deskew state diagram shown in Figure 82–14 (see 152.5.3.2). It is mapped to the bit defined in 45.2.1.117 (1.201.15).

152.6.13 BIP_error_counter_*i*

BIP_error_counter_*i*, where *i* = 0 to 19, is a 16-bit counter that holds the BIP error count for PCS lane *i* as calculated by the RS-FEC receive function (see 152.5.3.4). These variables are mapped to the registers defined in 45.2.1.123 and 45.2.1.124 (1.230 to 1.249).

152.6.14 lane_mapping<*x*>

When the RS-FEC transmit function detects and locks to an alignment marker on FEC service interface lane *x*, the PCS lane number corresponding to the detected alignment marker is assigned to the variable lane_mapping<*x*>. These variables are mapped to the registers defined in 45.2.1.125 and 45.2.1.126 (1.250 to 1.269).

152.6.15 block_lock<*x*>

These variables are assigned by the block lock state diagram shown in Figure 82–12 (see 152.5.3.1). They are mapped to the registers defined in 45.2.1.127 and 45.2.1.128 (1.280 and 1.281).

152.6.16 am_lock<*x*>

These variables are assigned by the alignment marker lock state diagram shown in Figure 82–13 (see 152.5.3.2). They are mapped to the registers defined in 45.2.1.129 and 45.2.1.130 (1.282 and 1.283).

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152.7 Protocol implementation conformance statement (PICS) proforma for Clause 152, Inverse RS-FEC sublayer[251]

152.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 152, Inverse RS-FEC sublayer, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

152.7.2 Identification

152.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

152.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 152, Inverse RS-FEC sublayer
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[251] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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152.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
DC	Delay constraints	152.4	Conforms to delay constraints specified in 152.4	M	Yes [ ]
*MD	MDIO capability	152.6	Registers and interface supported	O	Yes [ ] No [ ]
*BEC	Bypass error correction	152.5.2.3	Capability is supported	O	Yes [ ] No [ ]
*BEI	Bypass error indication	152.5.2.3	Capability is supported	O	Yes [ ] No [ ]

152.7.4 PICS proforma tables for Inverse RS-FEC sublayer

152.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Skew tolerance	152.5.2.1	Maximum Skew of 49 ns between FEC lanes and a maximum Skew Variation of 400 ps	M	Yes [ ]
TF2	Lane reorder	152.5.2.2	Order the FEC lanes according to the FEC lane number	M	Yes [ ]
TF3	Reed-Solomon decoder	152.5.2.3	RS(544,514) corrects any combination of up to $t = 15$ symbol errors in a codeword unless error correction bypassed	M	Yes [ ]
TF4	Reed-Solomon decoder uncorrected codeword detection	152.5.2.3	Capable of indicating when a codeword was not corrected	M	Yes [ ]
TF5	Error indication function	152.5.2.3	Corrupts 66-bit block synchronization headers for uncorrected errored codewords (or errored codewords when correction is bypassed)	M	Yes [ ]
TF6	Error indication when error correction is bypassed	152.5.2.3	Error indication is not bypassed	BEI:M	Yes [ ] N/A [ ]
TF7	Error monitoring while error indication is bypassed	152.5.2.3	When the number of symbol errors in a block of 8192 codewords exceeds 6380, corrupt 66-bit block synchronization headers	BEI:M	Yes [ ] N/A [ ]
TF8	Alignment marker removal	152.5.2.4	am_txmapped removed prior to transcoding	M	Yes [ ]
TF9	256B/257B to 64B/66B transcoder	152.5.2.5	tx_coded_j<65:0>, $j = 0$ to 3 constructed per 152.5.2.5	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TF10	Block distribution	152.5.2.6	One 66-bit block at a time in a round-robin fashion from the lowest to the highest numbered PCS lane	M	Yes [ ]
TF11	Alignment marker mapping	152.5.2.7	Map to am_tx_*x*, *x* = 0 to 19 per 152.5.2.7	M	Yes [ ]
TF12	Alignment marker insertion point	152.5.2.7	Alignment markers immediately followed by the 66-bit blocks derived from the 256-bit blocks immediately following am_txmapped	M	Yes [ ]

152.7.4.2 Receive Function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	152.5.3.2	Maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps	M	Yes [ ]
RF2	Lane reorder	152.5.3.3	Order the PCS lanes according to the PCS lane number	M	Yes [ ]
RF3	64B/66 to 256B/257B transcoder	152.5.3.5	rx_coded<256:0> constructed per 152.5.3.5	M	Yes [ ]
RF4	257-bit block transmission order	152.5.3.5	First bit transmitted in bit 0	M	Yes [ ]
RF5	Alignment marker mapping	152.5.3.6	Map to am_rx-mapped<1284:0> per 152.5.3.6	M	Yes [ ]
RF6	Pad value	152.5.3.6	Binary values 00101 and 11010 (the leftmost bit is assigned to the highest bit index) in an alternating pattern	M	Yes [ ]
RF7	Alignment marker insertion	152.5.3.6	First 1285 message bits to be transmitted from every 4096th codeword	M	Yes [ ]
RF8	Alignment marker insertion point	152.5.3.6	First 257-bit block inserted after am_rxmapped corresponds to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective lane	M	Yes [ ]
RF9	Reed-Solomon encoder	152.5.3.7	RS(544,514)	M	Yes [ ]
RF10	Symbol distribution	152.5.3.8	Distributed to 4 FEC lanes, one 10-bit symbol at a time in a round-robin distribution from the lowest to the highest numbered FEC lane	M	Yes [ ]

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152.7.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	SLIP function	152.5.4.2.2	Ensures that all possible block positions are evaluated	M	Yes [ ]
SD2	Synchronization process	152.5.4.3	One instance per FEC lane per Figure 91–8	M	Yes [ ]
SD3	Alignment process	152.5.4.3	Per Figure 91–9	M	Yes [ ]
SD4	FEC synchronization enhancement	152.5.4.3	Check AMs after synchronization is achieved per Figure 91–8	M	Yes [ ]

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153. SC-FEC and 100GBASE-ZR Physical Medium Attachment (PMA) sublayer for 100GBASE-ZR PHYs

153.1 Overview

153.1.1 Scope

This clause specifies a staircase FEC (SC-FEC) and PMA sublayer for 100GBASE-ZR PHYs.

153.1.2 Position of SC-FEC and 100GBASE-ZR PMA in the 100GBASE-R sublayers

Figure 153–1 shows the relationship of the SC-FEC and 100GBASE-ZR PMA to the ISO/IEC Open System Interconnection (OSI) reference model.

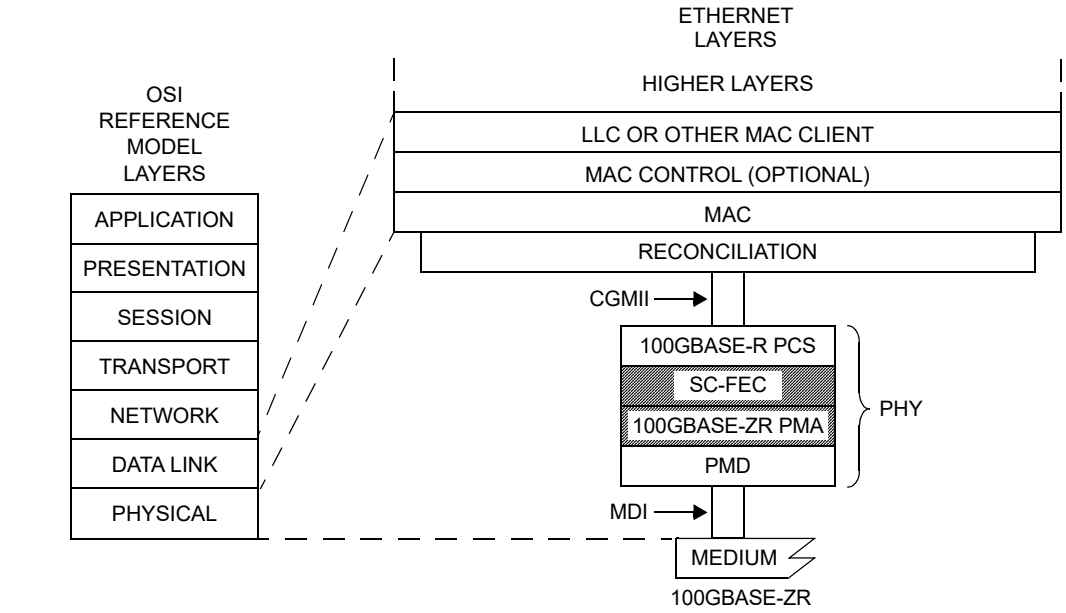

Figure 153–1—SC-FEC and 100GBASE-ZR PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

153.2 SC-FEC sublayer

153.2.1 FEC service interface

This subclause specifies the services provided by the SC-FEC sublayer.

The FEC service interface is provided to allow the PCS, Inverse RS-FEC, or PMA to transfer information to and from the SC-FEC. The service interface is described in an abstract manner and does not imply any particular implementation. The FEC service interface is an instance of the inter-sublayer service interface defined in 80.3. The service interface primitives are summarized as follows:

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FEC:IS_UNITDATA_*i*.request
FEC:IS_UNITDATA_*i*.indication
FEC:IS_SIGNAL.indication

The FEC:IS_UNITDATA_*i* primitives are defined for $i = 0$ to 19. The PCS, Inverse RS-FEC, or PMA continuously sends 20 parallel bit streams to the SC-FEC sublayer, each at a nominal signaling rate of 5.15625 GBd. The SC-FEC sublayer continuously sends 20 parallel bit streams to the PCS, Inverse RS-FEC, or PMA, one per lane, each at a nominal signaling rate of 5.15625 GBd.

The SIGNAL_OK parameter of the FEC:IS_SIGNAL.indication primitive can take one of two values: OK or FAIL. The value is set to OK when the FEC receive function has identified codeword boundaries as indicated by fec_align_status equal to TRUE. The value is set to FAIL when the FEC receive function is unable to reliably establish codeword boundaries as indicated by fec_align_status equal to FALSE. When SIGNAL_OK is FAIL, the rx_bit parameters of the FEC:IS_UNITDATA_*i*.indication primitives are undefined.

The PCS or Inverse RS-FEC may be connected to the SC-FEC using an optional instantiation of the PMA service interface (see Annex 83A, Annex 83B, Annex 83D, and Annex 83E) in which case a PMA (see Clause 83) or Inverse FEC (see Clause 152) is a client of the FEC service interface.

153.2.2 Delay constraints

The maximum delay contributed by the SC-FEC sublayer (sum of transmit and receive delays at one end of the link) shall be no more than 1 827 840 bit times (3570 pause_quanta or 18 278.4 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

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153.2.3 Functions within the SC-FEC sublayer

153.2.3.1 Functional block diagram

A functional block diagram of the SC-FEC sublayer is shown in Figure 153–2.

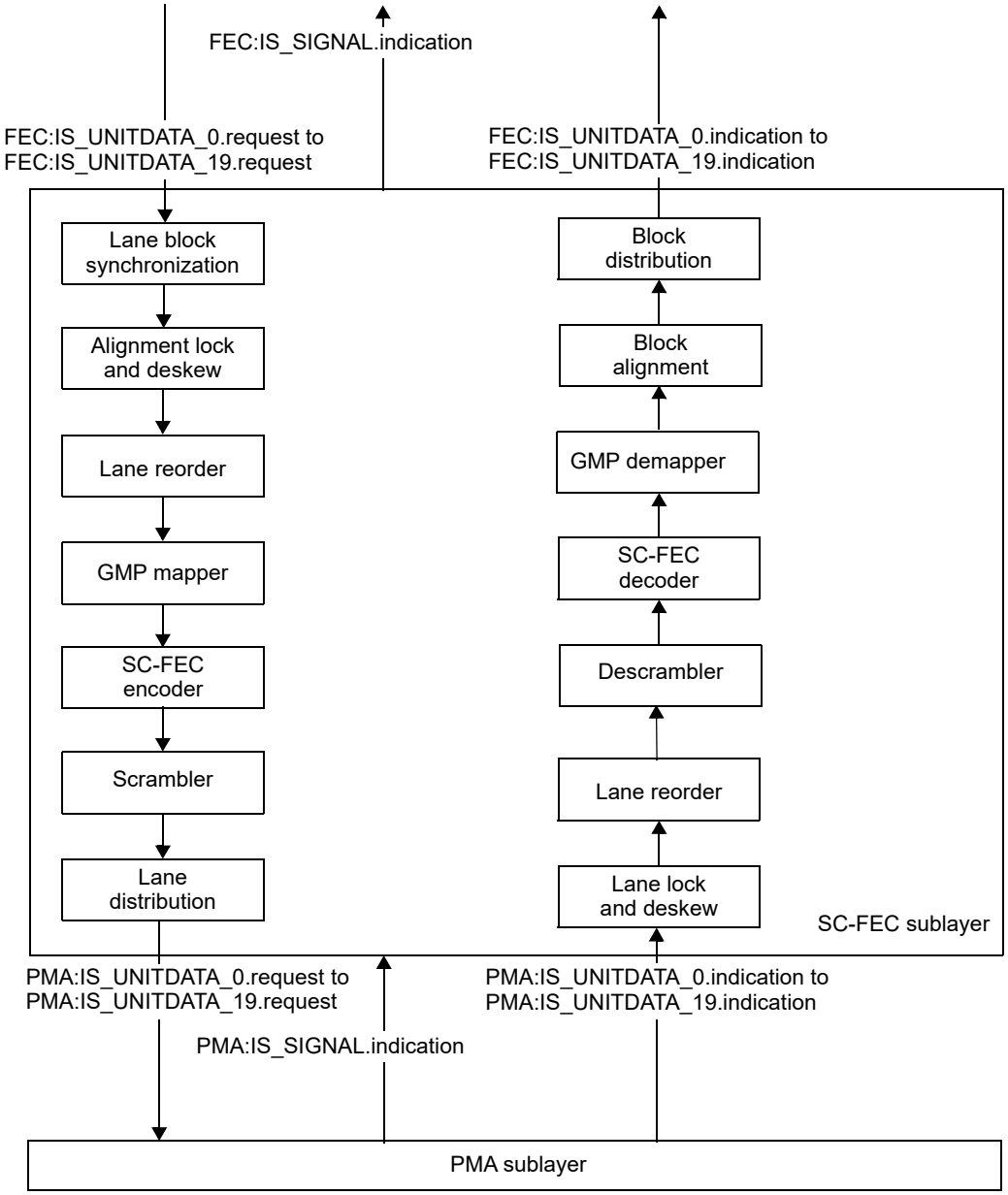

Figure 153–2—SC-FEC functional block diagram

153.2.3.2 Transmit function

153.2.3.2.1 Lane block synchronization

The SC-FEC transmit function forms 20 bit streams by concatenating the bits from each of the 20 FEC:IS_UNITDATA_*i*.request primitives in the order they are received. It obtains lock to the 66-bit blocks

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in each bit stream using the sync headers and outputs 66-bit blocks. Block lock is obtained as specified in the block lock state diagram shown in Figure 82–12.

153.2.3.2.2 Alignment lock and deskew

Once the SC-FEC transmit function achieves block lock on a PCS lane, it then begins obtaining alignment marker lock as specified by the alignment marker lock state diagram shown in Figure 82–13. This process identifies the PCS lane number received on a particular lane of the service interface. After alignment marker lock is achieved on all 20 lanes, all inter-lane Skew is removed as specified by the PCS deskew state diagram shown in Figure 82–14. The SC-FEC transmit function shall support a maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps. Skew and Skew Variation are defined in 80.5.

153.2.3.2.3 Lane reorder

PCS lanes can be received on different lanes of the service interface from which they were originally transmitted due to Skew between lanes and multiplexing by the PMA. The SC-FEC transmit function shall order the PCS lanes according to the PCS lane number. The result of this process is a logically serial stream of 66B block encoded information, including alignment markers, at a nominal signaling rate of 103.125 Gb/s.

153.2.3.2.4 GMP mapper

The generic mapping procedure (GMP) mapper inserts the serialized and deskewed stream of 66B blocks into an SC-FEC frame. The frame is similar to the OTU4 frame specified in ITU-T G.709 with the insertion of an SC-FEC parity specified in ITU-T G.709.2 Annex A. The frame consists of 16 320 octets, which for the purpose of description are illustrated as a four row, 4080 column structure with a logical transmission order left to right, top to bottom. This frame is illustrated in Figure 153–3.

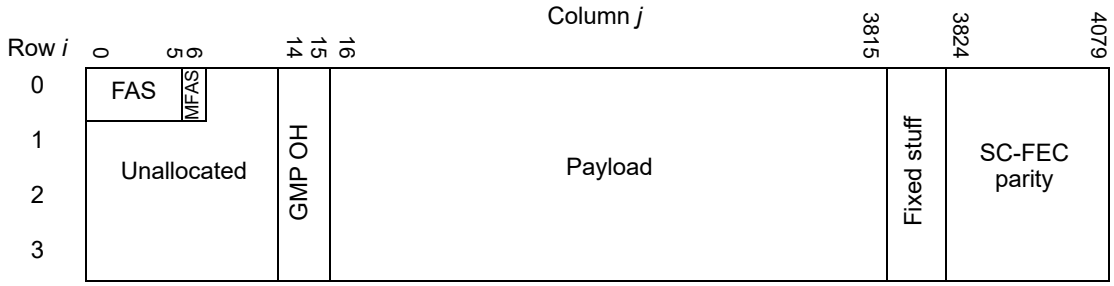

Figure 153–3—SC-FEC frame

The majority of the frame is scrambled prior to transmission (see 153.2.3.2.6). The information in the SC-FEC frame includes the following, described before scrambling:

1) The frame alignment signal (FAS) is similar in concept to the codeword marker described in Clause 108, being a fixed bit pattern occurring in the data stream at regular intervals allowing the receiver to locate and distinguish various elements in the transmitted data stream such as the payload and the FEC parity. The FAS is the following fixed bit pattern, transmitted left to right:
   1111 0110 1111 0110 1111 0110 0010 1000 0010 1000 0010 1000
2) The multi-frame alignment signal (MFAS) is a field that counts from 0 to 255, encoded with the most significant bit transmitted first. This is used for aligning SC-FEC base blocks with the SC-FEC frame and synchronizing the SC-FEC error decorrelator.
3) The unallocated portion of the frame corresponds to octet positions that are used for OTN path and section overhead in ITU-T G.709.2. These byte positions are not used for 100GBASE-ZR. They are transmitted with the value zero and are ignored on receipt.

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4) The GMP mapping overhead (GMP OH) is encoded in the eight octets from columns 14 and 15 of each of the four rows of the SC-FEC frame.
5) The 100GBASE-R PCS payload is GMP mapped in the area of the SC-FEC frame in the octets in columns 16 through 3815 in each of the four rows as shown in Figure 153–3.
6) The octets in the fixed stuff area of the frame are transmitted with the value zero and are ignored on receipt.
7) The SC-FEC parity area of the frame is allocated for FEC parity to be inserted as described in 153.2.3.2.5.

GMP is a generic mechanism that uses a sigma/delta distribution algorithm to accommodate an arbitrary signaling rate difference between a payload and the space in which it is carried. The principles of the GMP mapper are described in ITU-T G.709 (06/2020) Annex D, with details of the encoding of the GMP overhead in ITU-T G.709 Clause 19.4.3.2.

The payload area of the SC-FEC frame is divided into 190 GMP words of 80 octets each. Each 80-octet GMP word is either filled with data (the logically serialized 66B encoded stream produced according to 153.2.3.2.3) or stuff, which is transmitted as zero prior to scrambling and ignored on receipt.

The 66B encoded data is a logically serial stream at a rate of 103.125 Gb/s ± 100 ppm. The payload area of the SC-FEC frame has a capacity of (255/227) × (3800/4080) × 99.5328 Gb/s ± 20 ppm (~104.1367 Gb/s). The clocks for the PCS and the SC-FEC frame are independent. This results in an average number of 80-octet GMP words filled per SC-FEC frame between ~188.1315 and ~188.1766. Since the number of GMP words filled in a frame is always an integer, a given SC-FEC frame will have either 188 or 189 filled GMP words. While the GMP mechanism is generic, the particular clock rates and tolerances for this application result in a small number of cases, allowing the positions of data and stuff to be pre-computed. For either 188 or 189 GMP words filled in the SC-FEC frame, the GMP word consisting of the octets from column 16 to column 95 of row 0 will always be stuff (filled with zero rather than 66B encoded data prior to scrambling). In the case of 188 GMP words filled in the SC-FEC frame, the GMP word consisting of the octets from column 16 to column 95 of row 2 will also be stuff. Given the range of clock rate differences that may exist between the 66B encoded data and the SC-FEC frame payload capacity, there will tend to be between 4 and 7 frames with 188 filled GMP words between every frame with 189 filled GMP words. There is not a circumstance where there would be two consecutive frames containing 189 filled GMP words.

The GMP overhead is illustrated in Figure 153–4.

	Column															
	14								15							
Row	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	D9	D8	D7	D6	D5	C13	C12	C11	C10	C9	C8	C7	C6
1	0	0	0	D4	D3	D2	D1	D0	C5	C4	C3	C2	C1	C0	II	DI
2	0	0	0	CRC-5					CRC-8							
3	0x00								0x00							

Figure 153–4—GMP overhead encoding

The information in rows 0 and 1 of column 15 indicates how many (188 or 189) GMP words are filled in the next SC-FEC frame. While GMP is a generic mechanism, the particular use on this interface leaves only a small number of ways to fill in this information. Since the number of GMP words to be filled in a frame is normally expected to vary within a small range, special coding is used to indicate when the number of filled GMP words is the same, one greater, or one fewer than in the previous frame. The following cases exist for this interface:

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— The number of GMP words to be filled in the next SC-FEC frame is the same as the number of GMP words filled in this frame. This can only occur in the case of 188 filled GMP words, as the ratio of the two clock rates does not provide a case where two consecutive frames will contain 189 filled GMP words. The number 188 is encoded in bits C0 through C13, with C0 being the least significant bit and C13 being the most significant bit. The increment indicator (II bit) and decrement indicator (DI bit) are set to zero.

— The number of GMP words to be filled in the next SC-FEC frame is one greater than the number of GMP words filled in this SC-FEC frame. This will only occur in the case where the number of GMP words filled in this SC-FEC frame is 188 and the number of GMP words to be filled in the next SC-FEC frame is 189. This is signaled by inverting all of the odd-numbered C bits (C13, C11, C9, C7, C5, C3, and C1) from the value in the previous frame, setting the increment indicator (II bit) to one, and setting the decrement indicator (DI bit) to zero.

— The number of GMP words to be filled in the next SC-FEC frame is one fewer than the number of GMP words filled in this SC-FEC frame. This will only occur in the case where the number of GMP words filled in this SC-FEC frame is 189 and the number of GMP words to be filled in the next SC-FEC frame is 188. This is signaled by inverting all of the even-numbered C bits (C12, C10, C8, C6, C4, C2, C0) from the numeric value of GMP words filled in the previous frame (189), setting the decrement indicator (DI bit) to one, and setting the increment indicator (II bit) to zero.

The bit values for these three cases are shown in Table 153–1.

Table 153–1—Encoding of GMP words in next SC-FEC frame

This frame	Next frame	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0	II	DI
188	188	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0
	189	1	0	1	0	1	0	0	0	0	1	0	1	1	0	1	0
189	188	0	1	0	1	0	1	1	1	1	0	1	0	0	0	0	1

While there is an 8-bit Hamming distance between valid values that can go in rows 0 and 1 of column 15, this information is also protected by a CRC-8 inserted into row 2 of column 15. The generator polynomial for this CRC-8 is $x^8 + x^3 + x^2 + 1$, and is calculated as follows:

— The octets from rows 0 and 1 of column 15 are taken in network octet order, most significant/first transmitted bit first, to form a 16-bit pattern representing the coefficients of a polynomial $M(x)$ of degree 15.

— $M(x)$ is multiplied by x^8 and divided (modulo 2) by the generating polynomial, producing a remainder $R(x)$ of degree 7 or less.

— The coefficients of $R(x)$ are considered to be an 8-bit sequence, where x^7 is the most significant bit.

— This 8-bit sequence is the CRC-8 where the first bit of the CRC-8 to be transmitted is the coefficient of x^7 and the last bit transmitted is the coefficient of x^0.

To reduce the mapping jitter, extra timing information is provided to allow the Tx to inform the Rx how many octets of 66B encoded PCS data are received in each SC-FEC frame period. This can be understood as the number of extra octets (or portions of octets) that are held in the Tx buffer, whose fill level varies with the clock offset of the incoming 66B blocks and depending on whether 188 or 189 GMP words are filled in a given SC-FEC frame. As an example, consider a case where both the PCS and SC-FEC clocks are running at approximately nominal rate, and an average of 15 052 octets of 66B encoded PCS data are to be transmitted in each SC-FEC frame period. This is 12 octets more than 188 filled GMP words of 80 octets.

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Assume in the first frame period, where 188 GMP words are filled, that there are 15 excess octets in the Tx buffer, fewer than required to fill 189 GMP words. 188 × 80 octets of 66B encoded data are transmitted, and in the next SC-FEC frame period the Tx buffer fill has grown to 27 excess octets. The Tx buffer fill grows by 12 octets each frame period when 188 GMP words are filled, so grows from 39 to 51 to 63 to 75 octets. Then, in the seventh SC-FEC frame, there are sufficient extra octets in the Tx buffer to fill 189 × 80 octets in the SC-FEC frame, so 189 × 80 octets are transmitted, and the buffer fill level drops to 75 + 12 – 80 = 7 octets.

This extra timing information, essentially the number of excess octets in the Tx buffer, is signaled from the Tx to the Rx in rows 0 and 1 of column 14 of the SC-FEC frame. This is signaled as a 10-bit value in bits D0 through D9, with D0 being the least significant bit. This field may take values from 0 to 80 to reflect the number of excess full or partial octets in the Tx buffer. This information allows the Rx to know how many octets to distribute from its buffer in each SC-FEC frame period, and hence allows maintaining one-octet timing granularity even though the mapping granularity into the SC-FEC frame is 80 octet groups.

The bits D0 through D9 are protected by a CRC-5, which is calculated using a generator polynomial of $x^5 + x + 1$. This is calculated by the following steps:

— The bits D9 through D0 are taken in transmission order, most significant bit first, to form a 10-bit pattern representing the coefficients of a polynomial $M(x)$ of degree 9.
— $M(x)$ is multiplied by x^5 and divided (modulo 2) by the generator polynomial, producing a remainder $R(x)$ of degree 4 or less.
— The coefficients of $R(x)$ are considered to be a 5-bit sequence, where x^4 is the most significant bit.
— This 5-bit sequence is the CRC-5 where the first bit of the CRC-5 to be transmitted is the coefficient of x^4 and the last bit transmitted is the coefficient of x^0.

The third row of the GMP overhead is transmitted as zero and ignored on receipt.

153.2.3.2.5 SC-FEC encoder

The SC-FEC parity is calculated and inserted into the octets in columns 3824 through 4079 of each row of the FEC frame shown in Figure 153–3. The SC-FEC code is a blockwise recursively encoded 512 × 510 staircase code, sandwiched between a 30 592 + 2048 bit-wide optimized error decorrelator interleaver and error correlator de-interleaver. Computation of the FEC parity is described in ITU-T G.709.2 Annex A. The 512 × 510 code block distributes over two of the FEC frames shown in Figure 153–3.

153.2.3.2.6 Scrambler

The operation of the scrambler shall be functionally identical to a frame synchronous scrambler of length 65 535 operating at the bit-rate of the SC-FEC frame. The generating polynomial shall be $1 + x + x^3 + x^{12} + x^{16}$. The scrambler shall be reset to 0xFFFF at the first transmitted bit of the MFAS octet. The FAS octets are not scrambled. Figure 153–5 provides a functional block diagram of the frame synchronous scrambler.

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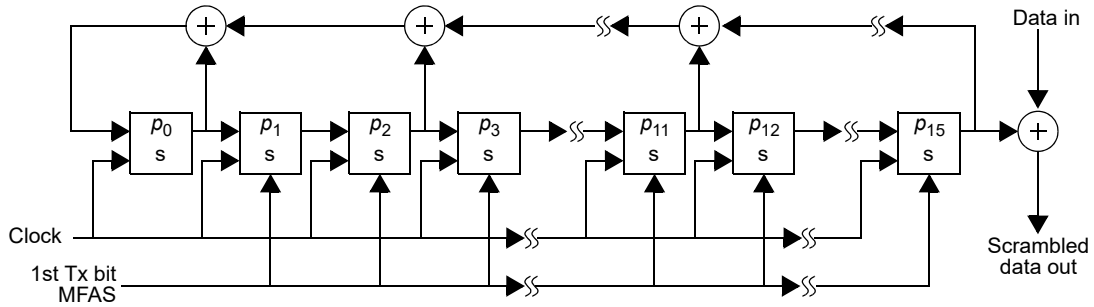

Figure 153–5—Frame synchronous scrambler

153.2.3.2.7 Lane distribution

The octets of the FEC frame are distributed to 20 FEC lanes as follows: The 6th octet of the FAS is replaced by a lane counter that increments from 0 to 239 on successive frames, with the most significant bit of the counter transmitted first. The lane counter 0 position shall be aligned with MFAS = 0 position every 3840 (the least common multiple of 240 and 256) frame periods. The counter resets to 0 on the first frame following the frame where the counter reaches the value 239.

Starting from the beginning of an FEC frame where the lane counter modulo 20 equals zero, the FEC frame is distributed to 20 FEC lanes 16 octets at a time in a round-robin manner as illustrated in Figure 153–6.

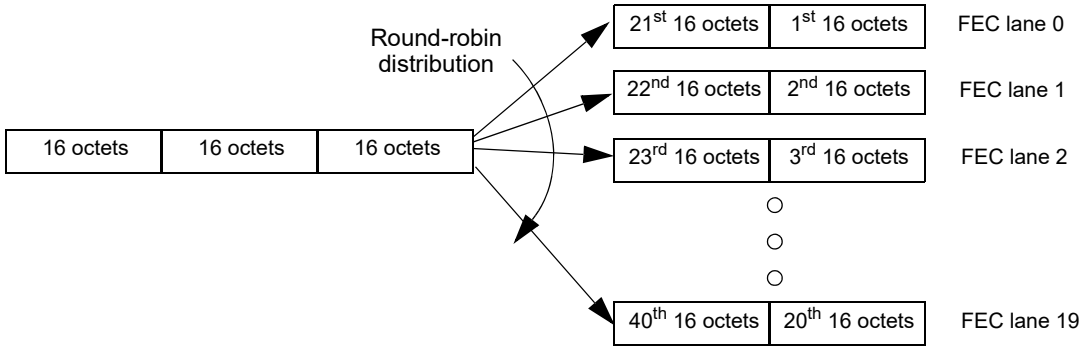

Figure 153–6—Lane distribution

51 groups of 16 octets are distributed from the FEC frame (consisting of 4080 × 4 octets) to each of the 20 FEC lanes.

At each FEC frame boundary, the assignment of 16-octet groups to FEC lanes is rotated, such that for each FEC frame where the lane counter modulo 20 equals 1, the first 16 octets of the FEC frame is distributed to FEC lane 1, the second 16 octets of the FEC frame is distributed to FEC lane 2, and so forth, with the 20th 16 octets of the FEC frame distributed to FEC lane 0. This pattern continues, with the final rotation occurring where the lane counter modulo 20 equals 19, where the first 16 octets of the FEC frame is distributed to FEC lane 19.

NOTE—This distribution to FEC lanes follows the distribution method of OTU4 to parallel lanes described in ITU-T G.709 Annex C.

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153.2.3.3 Receive function

153.2.3.3.1 Lane lock and deskew

The SC-FEC receive function forms 20 bit streams by concatenating the bits from each of the 20 PMA:IS_UNITDATA_*i*.indication primitives in the order they are received. It obtains lock to the FAS as specified by the SC-FEC synchronization state diagram shown in Figure 153–7. After frame alignment lock is achieved on all 20 lanes, all inter-lane Skew is removed as specified by the SC-FEC deskew state diagram shown in Figure 153–8. The FEC receive function shall support a maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns.

NOTE—An alternative method for frame alignment of OTU4 distributed to parallel lanes described in ITU-T G.709 Annex C is described in ITU-T G.798 [B46]. Equipment using this alternative method of frame alignment can interconnect with equipment implementing the SC-FEC synchronization state diagram shown in Figure 153–7, with each end of the link identifying and deskewing lanes according to its own method. The methods should not be combined at the same end of the link: in particular, if the ITU-T G.798 [B46] process is used, SIGNAL_OK=FALSE should not be indicated when in the out-of-frame (OOF) or out-of-recovery (OOR) states.

153.2.3.3.2 Lane reorder

Transmit FEC lanes can be received on different lanes of the service interface from which they were originally transmitted due to Skew between lanes and multiplexing by the PMA. The receive SC-FEC shall order the received FEC lanes according to the FEC lane number, which is the 6th octet of the FAS (inserted as per 153.2.3.2.7) modulo 20. As the reordered lanes are interleaved in the original order, the FEC lane number is replaced by the original final octet of the FAS, which has a value of 0010 1000.

153.2.3.3.3 De-scrambler

The de-scrambler reverses the effects of the scrambler described in 153.2.3.2.6. Since the scrambler is frame synchronous, this is accomplished by XORing each bit after the FAS, which is not scrambled, with the same sequence resulting from the generating polynomial used by the scrambler.

153.2.3.3.4 SC-FEC decoder

Errors are corrected by applying the process described in ITU-T G.709.2 Annex A. This operates by passing the received information and parity bits through an error decorrelator interleaver process, a parity compute, compare, and error correction process, and an error decorrelator deinterleaver process. The FEC parity is removed from the frame shown in Figure 153–3 after error correction.

The SC-FEC decoder indicates errors to the PCS sublayer by replacing all 66-bit blocks (extracted from the SC-FEC frame using the process described in 153.2.3.3.5) that are fully or partially contained within an uncorrected codeword (including uncorrectable codewords, or potentially mis-corrected or not fully corrected codewords) with error control blocks. An error control block has control block type 0x1E and carries eight /E/ control characters. The marking includes a 66-bit block that begins in the SC-FEC codeword preceding the uncorrected SC-FEC codeword and ending in the uncorrected codeword, and a 66-bit block that begins in the uncorrected codeword and ends in the next codeword. The probability that the SC-FEC decoder fails to replace 66-bit blocks in an uncorrectable codeword is expected to be less than 10^{-6}.

153.2.3.3.5 GMP demapper

The GMP demapper extracts the deskewed and serialized stream of 66B blocks that was inserted according to the process described in 153.2.3.2.4 from the SC-FEC frame.

The principles of the GMP demapper are described in ITU-T G.709 Annex D, with details of the encoding of the GMP overhead in ITU-T G.709 Clause 19.4.3.2.

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The GMP demapper extracts 188 or 189 groups of 80 octets of 66B encoded data from each SC-FEC frame (frame *n*), controlled by the GMP overhead (see Table 153–1) in the previous SC-FEC frame (frame *n* – 1). If a C13:C0 value other than 188 or 189, or DI=1 and II=1 is received, the GMP demapper behavior is undefined. The number of 80-octet groups demapped from SC-FEC frame *n*, together with the change in value of the extra timing information (see 153.2.3.2.4) in between SC-FEC frames *n* – 1 and *n* – 2 are used to calculate how many octets of 66B encoded data are sent towards the FEC service interface in each SC-FEC frame period.

153.2.3.3.6 Block alignment

Block lock is obtained on the bit sequence extracted by the GMP demapper using the block lock state diagram shown in Figure 82–12.

153.2.3.3.7 Block distribution

Once block alignment has been achieved per 153.2.3.3.6, 66B blocks are distributed round robin to the lanes of the service interface as described in 82.2.6.

153.2.4 Detailed functions and state diagrams

The body of this subclause includes state diagrams, including the associated definitions of variables, functions, and counters. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

153.2.4.1 State variables

153.2.4.1.1 Variables

all_locked
: A Boolean variable that is set to TRUE when fas_lock<*x*> is TRUE for all *x* and is set to FALSE when fas_lock<*x*> is FALSE for any *x*.

current_fecl
: A variable that holds the FEC lane identification octet corresponding to the current FAS that is recognized on a given lane of the PMA service interface. The value of this variable modulo 20 represents the FEC lane number. It is compared to the expected value based on the variable prev_fecl to confirm that the location of the FAS has been detected. This value is interpreted with the most significant bit transmitted first.

fas_counter_done
: Boolean variable that indicates that fas_counter has reached its terminal count.

fas_match
: Boolean variable that holds the output of the function FAS_COMPARE.

fas_valid
: Boolean variable that is set to TRUE if the received 6-octet sequence is a valid FAS. The FAS consists of five known octets and one variable octet. The sequence is considered to be valid if at least four of the first five octets match the known bits of the pattern described in 153.2.3.2.4, and the 6th octet represents a numerical value in the range 0 to 239 with the most-significant bit transmitted first.

fas_lock<*x*>
: Boolean variable that is set to TRUE when the receiver has detected the location of the FAS for a given lane on the PMA service interface, where *x* = 0:19.

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fec_align_status
: A Boolean variable set by the FEC alignment process to reflect the status of FEC lane-to-lane alignment. Set to TRUE when all lanes are synchronized and aligned and set to FALSE when the deskew process is not complete.

fec_alignment_valid
: Boolean variable that is set to TRUE if all FEC lanes are aligned. FEC lanes are considered to be aligned when fas_lock<*x*> is TRUE for all *x*, each FEC lane has a unique lane number, and the FEC lanes are deskewed. Otherwise, this variable is set to FALSE.

fec_enable_deskew
: A Boolean variable that indicates the enabling and disabling of the deskew process. Data may be discarded whenever deskew is enabled. TRUE when deskew is enabled. FALSE when deskew is disabled.

fec_lane
: A variable that holds the FEC lane number (0 to 19) received on lane *x* of the PMA service interface when fas_lock<*x*> = TRUE. The FEC lane number is determined by the 6th octet of the FAS, interpreted with the most significant bit transmitted first, modulo 20. It is set to current_fecl modulo 20 when the expected FAS is found in the expected location in a second consecutive SC-FEC frame.

FEC_lane_mapping<*x*>
: This variable indicates which FEC lane is received on lane *x* of the PMA service interface when fas_lock<*x*> = TRUE, where *x* = 0:19.

prev_fecl
: A variable that holds the value of the lane identification octet (or the expected value of the lane identification octet) from the previous SC_FEC frame. The value is interpreted with the most significant bit transmitted first. The lane represented is this value modulo 20. It is used to calculate the expected value of the lane identification octet in the next SC-FEC frame period that is tested.

reset
: Boolean variable that controls the resetting of the SC-FEC sublayer. It is TRUE whenever a reset is necessary including when reset is initiated from the MDIO and during power on.

restart_lock
: Boolean variable that is set by the FEC alignment process to reset the synchronization process on all FEC lanes. It is set to TRUE when 15 FASs in a row fail to match (15_BAD state).

rx_align_status
: Boolean variable that is set by the lane lock and deskew function (see 153.2.3.3.1).

signal_ok
: Boolean variable that is set based on the most recently received value of PMA:IS_SIGNAL.indication (SIGNAL_OK). It is TRUE if the value was OK and FALSE if the value was FAIL.

slip_done
: Boolean variable that is set to TRUE when the SLIP requested by the synchronization state diagram has been completed indicating that the next candidate FAS position can be tested.

test_fas
: Boolean variable that is set to TRUE when a candidate FAS position is available for testing and FALSE when the FIND_1ST state is entered.

153.2.4.2 Functions

FAS_COMPARE
: This function compares the FAS with its expected value to determine if a valid frame alignment sequence has been detected and returns the result of the comparison using the variable fas_match. FAS_COMPARE is TRUE if fas_valid is TRUE, and current_fecl (interpreted with the most significant bit transmitted first) is equal to the prev_fecl plus 20 modulo 240. Otherwise, fas_match is FALSE.

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SLIP

Causes the next candidate FAS position to be tested. The precise method for determining the next candidate FAS position is not specified and is implementation dependent. An implementation shall ensure that the FAS pattern can be detected in any possible position.

153.2.4.3 Counters

fas_bad_count

Counts the number of consecutive FASs that don't match the expected value for a given FEC lane.

fas_counter

Counts the 16 320 octets between the starting position of one FAS and the expected starting position of the next FAS on an FEC lane. This counter starts with a value of zero when start fas_counter is asserted (at the position of the first octet of a matched FAS pattern on an FEC lane), is incremented for each octet on that FEC lane, and reaches a terminal value of 16 320 at the expected position of the next FAS pattern on that FEC lane.

153.2.4.4 State diagrams

The SC-FEC shall implement 20 synchronization processes as shown in Figure 153–7. The synchronization process operates independently on each lane. The SC-FEC sublayer uses this process to detect the location of the frame alignment sequence in the received bit stream on each lane of the PMA service interface.

The SC-FEC shall implement the deskew process as shown in Figure 153–8.

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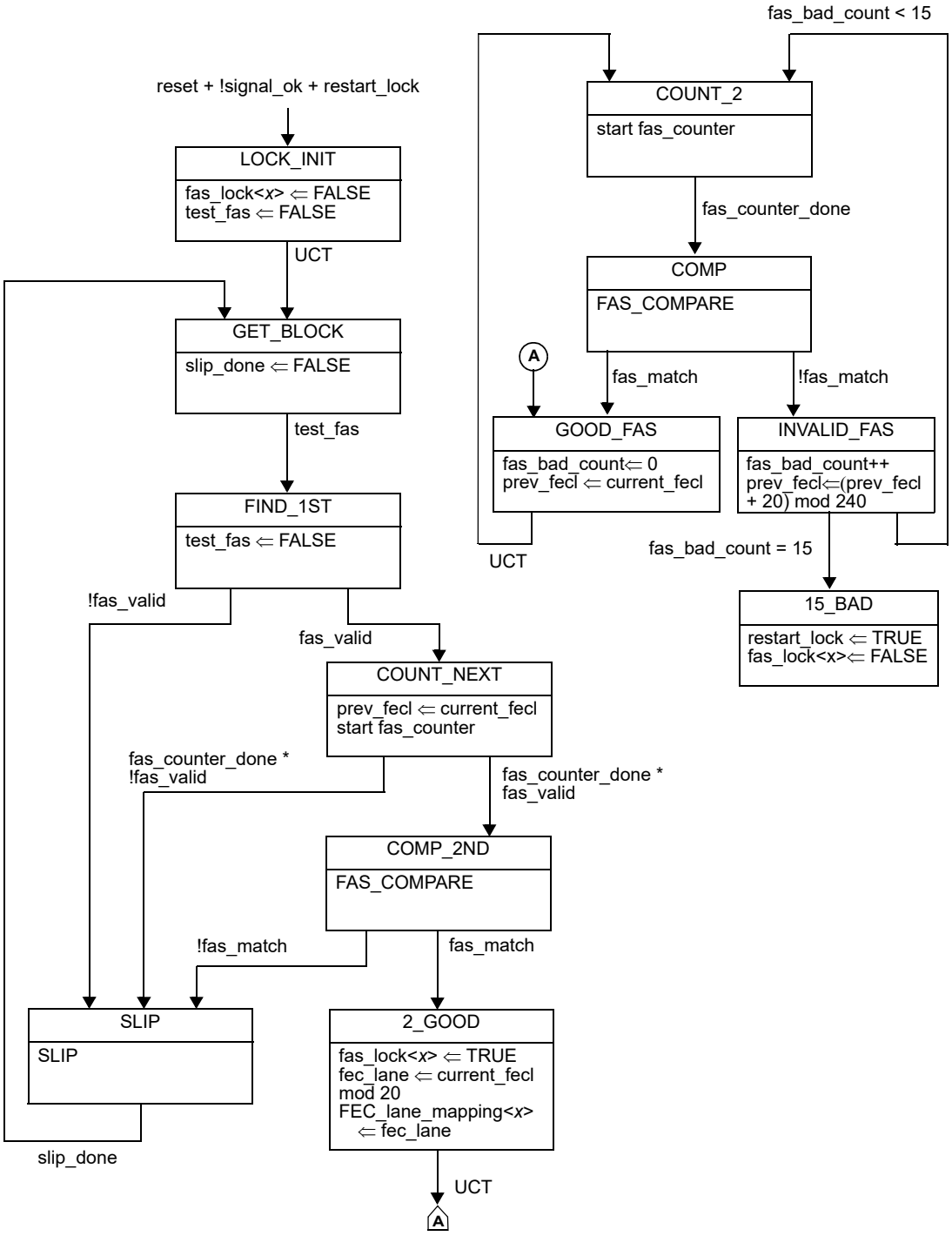

Figure 153–7—SC-FEC synchronization state diagram

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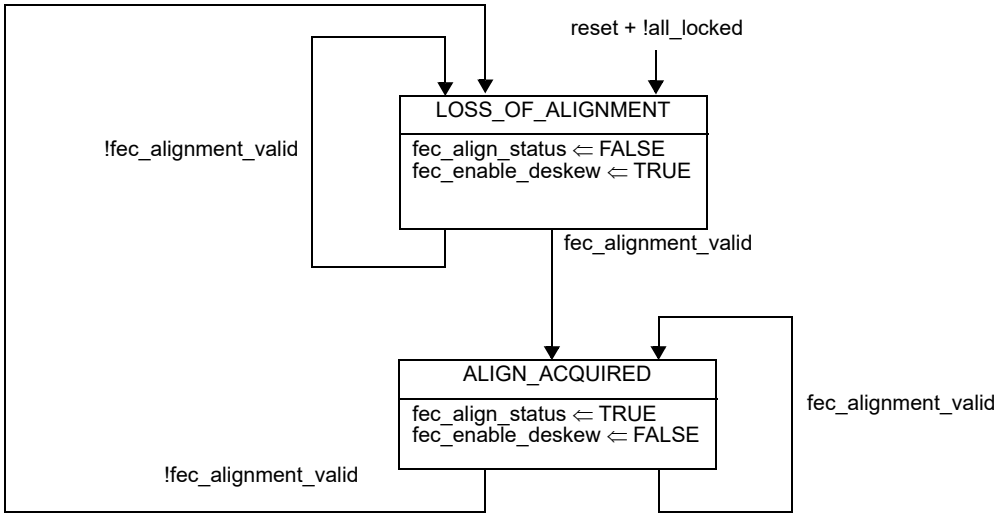

Figure 153–8—SC-FEC deskew state diagram

153.2.5 SC-FEC MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the SC-FEC. If MDIO is implemented, it shall map MDIO status bits to SC-FEC status variables as shown in Table 153–2.

153.2.5.1 FEC_corrected_cw_counter

A corrected FEC codeword is a codeword that contained errors and was corrected.

The FEC_corrected_cw_counter is a 32-bit counter that counts once for each corrected FEC codeword processed when fec_align_status is TRUE. This variable is mapped to the registers defined in 45.2.1.227 (1.2276, 1.2277).

153.2.5.2 FEC_uncorrected_cw_counter

An uncorrected FEC codeword is a codeword that contains errors that were not corrected, including FEC codewords that may have been mis-corrected or not completely corrected.

The FEC_uncorrected_cw_counter is a 32-bit counter that counts once for each uncorrected FEC codeword processed when fec_align_status is TRUE. This variable is mapped to the registers defined in 45.2.1.228 (1.2278, 1.2279).

153.2.5.3 FEC_total_bits_counter

The FEC_total_bits_counter is a 64-bit counter that counts once for each bit processed by the SC-FEC decoder. This variable is mapped to the registers defined in 45.2.1.229 (1.2280, 1.2281, 1.2282, 1.2283). This may used together with the FEC_corrected_bits_counter (see 153.2.5.4) as a measure of pre-FEC BER.

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Table 153–2—MDIO/SC-FEC Status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
SC-FEC FAS lock *x*, *x* = 0 to 19	SC-FEC alignment status 1 and 2 registers	1.2246.7:0 1.2247.11:0	fas_lock<*x*>
SC-FEC align status	SC-FEC alignment status 1 register	1.2246.12	fec_align_status
Lane *x* mapping, *x* = 0 to 19	SC-FEC lane mapping, lane *x* register	1.2250 through 1.2269	FEC_lane_mapping<*x*>
FEC corrected codewords	SC-FEC corrected codewords counter register	1.2276, 1.2277	FEC_corrected_cw_counter
FEC uncorrected codewords	SC-FEC uncorrected codewords counter register	1.2278, 1.2279	FEC_uncorrected_cw_counter
FEC total bits	SC-FEC total bits register	1.2280, 1.2281, 1.2282, 1.2283	FEC_total_bits_counter
FEC corrected bits	SC-FEC corrected bits register	1.2284, 1.2285, 1.2286, 1.2287	FEC_corrected_bits_counter

153.2.5.4 FEC_corrected_bits_counter

The FEC_corrected_bits_counter is a 64-bit counter that counts once for each bit corrected by the SC-FEC decoder. This variable is mapped to the registers defined in 45.2.1.230 (1.2284, 1.2285, 1.2286, 1.2287). This may be used together with the FEC_total_bits_counter (see 153.2.5.3) to calculate pre-FEC BER.

153.3 100GBASE-ZR PMA sublayer

153.3.1 100GBASE-ZR PMA service interface

This subclause specifies the services provided by the 100GBASE-ZR PMA sublayer. The 100GBASE-ZR PMA service interface is provided to allow the SC-FEC to transfer information to and from the 100GBASE-ZR PMD. The service interface is specified in an abstract manner and does not imply any particular implementation. The service interface primitives are summarized as follows:

PMA:IS_UNITDATA_*i*.request
PMA:IS_UNITDATA_*i*.indication
PMA:IS_SIGNAL.indication

The primitives are defined for i = 0 to 19. The SC-FEC continuously sends 20 parallel bit streams to the 100GBASE-ZR PMA sublayer, each at a nominal signaling rate of (255/227) × 4.97664 Gb/s ± 20 ppm (~5.59049868 Gb/s). Likewise the 100GBASE-ZR PMA sublayer continuously sends 20 parallel bit streams to the SC-FEC sublayer, each at a nominal signaling rate of (255/227) × 4.97664 Gb/s ± 20 ppm (~5.59049868 Gb/s).

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153.3.2 Functions within the 100GBASE-ZR PMA sublayer

153.3.2.1 Functional block diagram

A functional diagram of the 100GBASE-ZR PMA sublayer is shown in Figure 153–9.

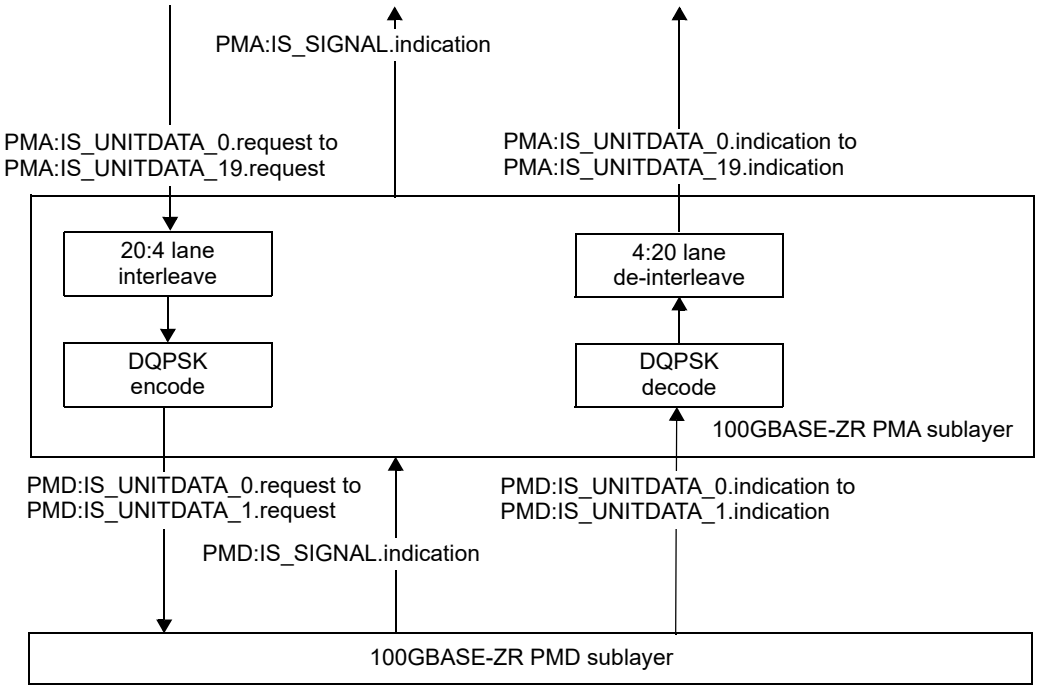

Figure 153–9—100GBASE-ZR PMA functional block diagram

153.3.2.2 Transmit function

153.3.2.2.1 Lane interleave

The lane interleave function bit-multiplexes groups of five lanes of the PMA service interface to form four logical bit streams operating at five times the service interface signaling rate. Each of the four bit streams constructed in this manner operates at a signaling rate of (255/227) × 24.8832 Gb/s ± 20 ppm (~27.9525 Gb/s). The selection of which five lanes of the service interface is used to form each lane of the four-lane interface is arbitrary, but the combination of service interface lanes used to form each of the four lanes, and the order in which the bits are multiplexed from each of the input lanes, does not change while the link is in service. Each service interface lane is bit-multiplexed into exactly one lane of the four-lane interface.

NOTE—This four-lane interface format is referred to in ITU-T G.709 and ITU-T G.709.2 as OTL4.4.

153.3.2.2.2 DQPSK encode

The differential quadrature phase shift keying (DQPSK) encode function takes information from pairs of lanes (A, B) of the four-lane interface produced by the lane interleave function described in 153.3.2.2.1 and encodes them as a two streams of DQPSK symbols, one stream formed from each lane pair. The selection of the two lanes of the four-lane interface used to form each stream of DQPSK symbols is arbitrary, but does not change while the link is in service. The signaling rate of each stream of DQPSK symbols is (255/227) × 24.8832 GBd ± 20 ppm (~27.9525 GBd).

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With differential encoding, each DQPSK symbol can take one of four values 0 to 3. These four values are associated with the values of the pair of bits from the two lanes of the four-lane interface used to form each DQPSK symbol stream. The mapping of pairs of bits to DQPSK symbol values is given in Table 153–3.

Table 153–3—Bit mapping to DQPSK symbol values

Lane bit values A, B	DQPSK symbol value
00	0
10	1
11	2
01	3

153.3.2.3 Receive function

153.3.2.3.1 DQPSK decode

The 100GBASE-ZR PMA receives from the 100GBASE-ZR PMD two streams of DQPSK symbols at a signaling rate of (255/227) × 24.8832 GBd ± 20 ppm (~27.9525 Gbd). The two streams of DQPSK symbols are converted to a four-lane digital interface as follows:

1) Each received DQPSK symbol is converted to a pair of bits as shown in Table 153–3.
2) One bit of each DQPSK symbol (A, B) is sent on a different lane of the four-lane digital interface. The assignment of each bit-position from the DQPSK symbols on the two DQPSK symbol streams to lanes of the four-lane digital interface is arbitrary, but does not change while the link is in service.

NOTE—This four-lane interface format is referred to in ITU-T G.709 and ITU-T G.709.2 as OTL4.4.

153.3.2.3.2 Lane de-interleave

Each lane of the four-lane digital signal produced by decoding of DQPSK symbols described in 153.3.2.3.1 is de-interleaved to five lanes of the 100GBASE-ZR PMA service interface by distributing successive bits round robin to each of the 100GBASE-ZR PMA service interface lanes. The assignment of bit positions on each of the lanes of the four-lane interface to the service interface lanes is arbitrary, but does not change while the link is in service.

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153.4 Protocol implementation conformance statement (PICS) proforma for Clause 153, SC-FEC and 100GBASE-ZR Physical Medium Attachment (PMA) sublayer for 100GBASE-ZR PHYs[252]

153.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 153, SC-FEC and 100GBASE-ZR Physical Medium Attachment (PMA) sublayer for 100GBASE-ZR PHYs, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

153.4.2 Identification

153.4.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

153.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 153, SC-FEC and 100GBASE-ZR Physical Medium Attachment (PMA) sublayer for 100GBASE-ZR PHYs
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[252]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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153.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
DC	Delay constraints	153.2.2	Conforms to delay constraints specified in 153.2.2	M	Yes [ ]
*MD	MDIO capability	153.2.5	Registers and interface supported	O	Yes [ ] No [ ]

153.4.4 PICS proforma tables for SC-FEC sublayer for 100GBASE-ZR PHYs

153.4.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	PCS lane Skew tolerance	153.2.3.2.2	Maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps	M	Yes [ ]
TF2	PCS lane reorder	153.2.3.2.3	Order the PCS lanes according to the PCS lane number	M	Yes [ ]
TF3	GMP mapper	153.2.3.2.4	Create the SC-FEC frame and GMP map the deskewed and serialized PCS lanes into the payload area of the frame	M	Yes [ ]
TF4	SC-FEC encoder	153.2.3.2.5	Compute and insert the SC-FEC parity into the SC-FEC frame	M	Yes [ ]
TF5	Scrambler	153.2.3.2.6	Frame synchronous scrambler	M	Yes [ ]
TF6	Lane distribution	153.2.3.2.7	Distribute SC-FEC frame to FEC lanes according to 153.2.3.2.7	M	Yes [ ]

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153.4.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	FEC lane Skew tolerance	153.2.3.3.1	Maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	FEC lane reorder	153.2.3.3.2	Order the FEC lanes according to the FEC lane number	M	Yes [ ]
RF3	De-scrambler	153.2.3.3.3	De-scramble according to 153.2.3.3.3	M	Yes [ ]
RF4	SC-FEC decoder	153.2.3.3.4	Correct errors by decoding SC-FEC parity	M	Yes [ ]
RF5	GMP demapper	153.2.3.3.5	Extract 66B encoded block stream from SC-FEC frame	M	Yes [ ]
RF6	Block Alignment	153.2.3.3.6	Distribute blocks as PCS lanes to the FEC service interface	M	Yes [ ]

153.4.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	100GBASE-R block lock	153.2.3.2.1	Implements 20 block lock processes as depicted in Figure 82–12	M	Yes [ ]
SD2	The SLIP function evaluates all possible bit positions	153.2.3.2.1		M	Yes [ ]
SD3	100GBASE-R alignment marker lock	153.2.3.2.2	Implements 20 alignment marker lock processes as depicted in Figure 82–13	M	Yes [ ]
SD4	The AM_SLIP function evaluates all possible blocks	153.2.3.2.2		M	Yes [ ]
SD5	100GBASE-R PCS deskew state diagram	153.2.3.2.2	Meets the requirements of Figure 82–14	M	Yes [ ]
SD6	SC-FEC synchronization state diagram	153.4.4.3	One instance per FEC lane per Figure 153–7	M	Yes [ ]
SD7	FEC lane reorder	153.2.3.3.2	Order the FEC lanes according to the FEC lane number	M	Yes [ ]

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154. Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-ZR

154.1 Overview

This clause specifies the 100GBASE-ZR PMD together with the associated single-mode fiber-based dense wavelength division multiplexing (DWDM) channel that may contain one or more optical amplifiers and is specified using a black link approach (see 154.6). The optical signal generated by this PMD type is modulated using a dual polarization differential quadrature phase shift keying (DP-DQPSK) format suitable for reception by a coherent optical receiver. When forming a complete Physical Layer, a PMD shall be connected to the 100GBASE-ZR PMA as shown in Table 154–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 154–1—Physical Layer clauses associated with the 100GBASE-ZR PMD

Associated clause	100GBASE-ZR
81—RS	Required
81—CGMII[a]	Optional
82—PCS	Required
83—100GBASE-R PMA	Optional
91—RS-FEC	Optional
83A—CAUI-10 C2C	Optional
83B—CAUI-10 C2M	Optional
83D—CAUI-4 C2C	Optional
83E—CAUI-4 C2M	Optional
152—Inverse RS-FEC	Conditional[b]
153—SC-FEC	Required
153—100GBASE-ZR PMA	Required
135—100GBASE-P PMA	Optional
135D—100GAUI-4 C2C	Optional
135E—100GAUI-4 C2M	Optional
135F—100GAUI-2 C2C	Optional
135G—100GAUI-2 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a]The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation behaves functionally as though the RS and CGMII were present.
[b]Clause 152 inverse RS-FEC mandatory when Clause 91 RS-FEC is present.

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Figure 154–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 100 Gigabit Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2.

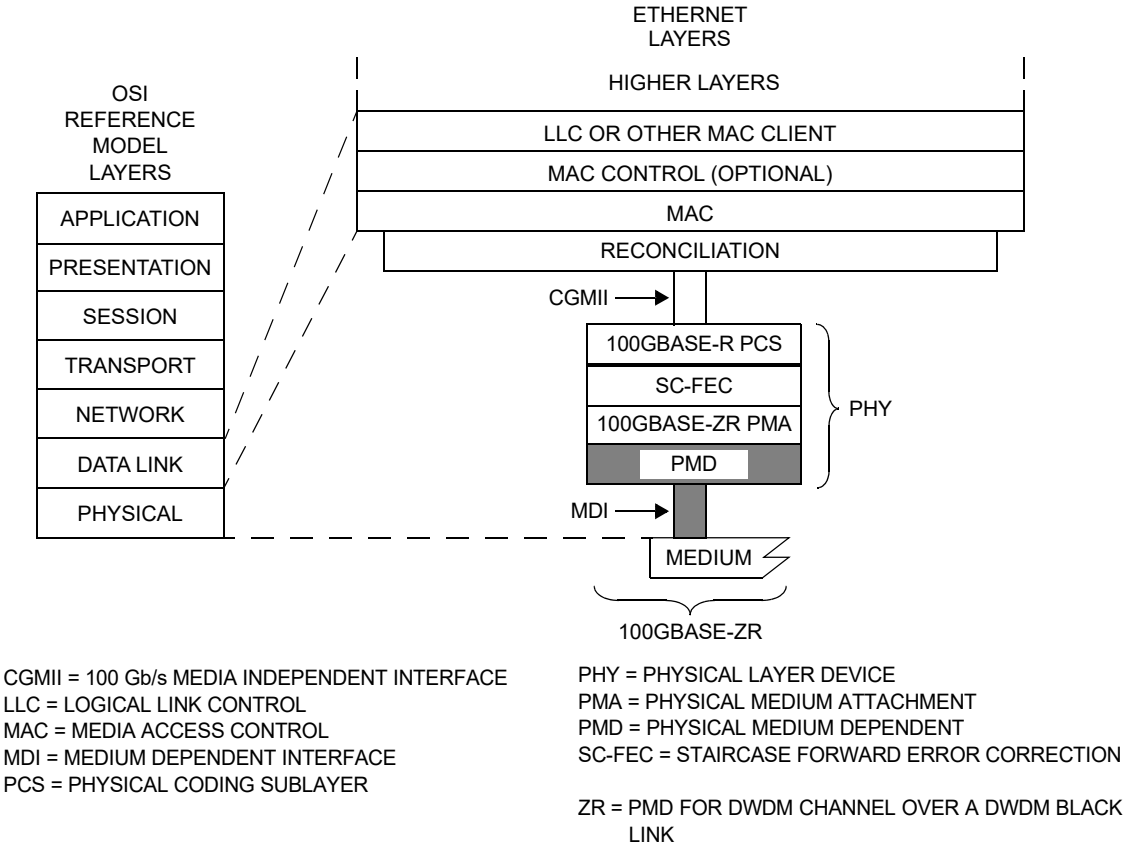

Figure 154–1—100GBASE-ZR PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

100GBASE-ZR PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

154.1.1 Bit error ratio

The bit error ratio (BER) when processed by the PMA (Clause 153) shall be less than 4.62×10^{-3} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap when additionally processed by the FEC (Clause 153) and PCS (Clause 82).

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap.

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154.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 100GBASE-ZR PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The 100GBASE-ZR PMD service interface is an instance of the inter-sublayer service interface defined in 116.3, with two symbol streams, one for each polarization. The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 100GBASE-ZR PMD has two parallel symbol streams, in which case $i = 0$ to 1.

In the transmit direction, the PMA continuously sends two parallel DQPSK symbol streams to the PMD, one stream per polarization, each with symbol values 0 to 3 and at a nominal signaling rate of (255/227) × 24.8832 GBd (~27.9525 GBd), using the PMD:IS_UNITDATA_*i*.request primitive. The PMD then converts these streams of symbols into the appropriate signals on the MDI.

In the receive direction, the PMD continuously sends two parallel DQPSK symbol streams to the PMA, corresponding to the signals received from the MDI, each with symbol values 0 to 3, using the PMD:IS_UNITDATA_*i*.indication primitive, at a nominal signaling rate of (255/227) × 24.8832 GBd (~27.9525 GBd).

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable SIGNAL_DETECT parameter as defined in 154.5.4. The SIGNAL_DETECT parameter takes a fixed value of OK.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 154.1.1.

154.3 Delay and Skew

154.3.1 Delay constraints

The sum of the transmit and receive delays at one end of the link contributed by the 100GBASE-ZR PMD including 2 m of fiber in one direction shall be no more than 2048 bit times (4 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 and its references.

154.3.2 Skew constraints

The Skew (relative delay) between the FEC lanes is kept within limits so that the information on the FEC lanes can be reassembled by the FEC. The Skew Variation is also limited to ensure that a given FEC lane always traverses the same physical lane. Skew and Skew Variation are defined in 80.5 and specified at the points SP0 to SP7 shown in Figure 80–9.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

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The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation, see 80.5.

154.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 154–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 154–3.

Table 154–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
Tx optical channel index	Tx optical channel control register	1.800.5:0	Tx_optical_channel_index
Rx optical channel index	Rx optical channel control register	1.820.5:0	Rx_optical_channel_index

Table 154–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
Tx index ability 0 to Tx index ability 47	Tx optical channel ability 1 register to Tx optical channel ability 3 register	1.801 to 1.803	Tx_index_ability_0 to Tx_index_ability_47
Tx Rx different optical channel ability	Rx optical channel control register	1.820.15	Tx_Rx_diff_opt_chan_ability
Rx index ability 0 to Rx index ability 47	Rx optical channel ability 1 register to Rx optical channel ability 3 register	1.821 to 1.823	Rx_index_ability_0 to Rx_index_ability_47

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154.5 PMD functional specifications

The 100GBASE-ZR PMD performs the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

154.5.1 PMD block diagram

The PMD block diagram is shown in Figure 154–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 154.9 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 154.11). Unless specified otherwise, all receiver measurements and tests defined in 154.9 are made at TP3.

TP1 and TP4 are optional reference points that may be useful to implementers for testing components (these test points will not typically be accessible in an implemented system).

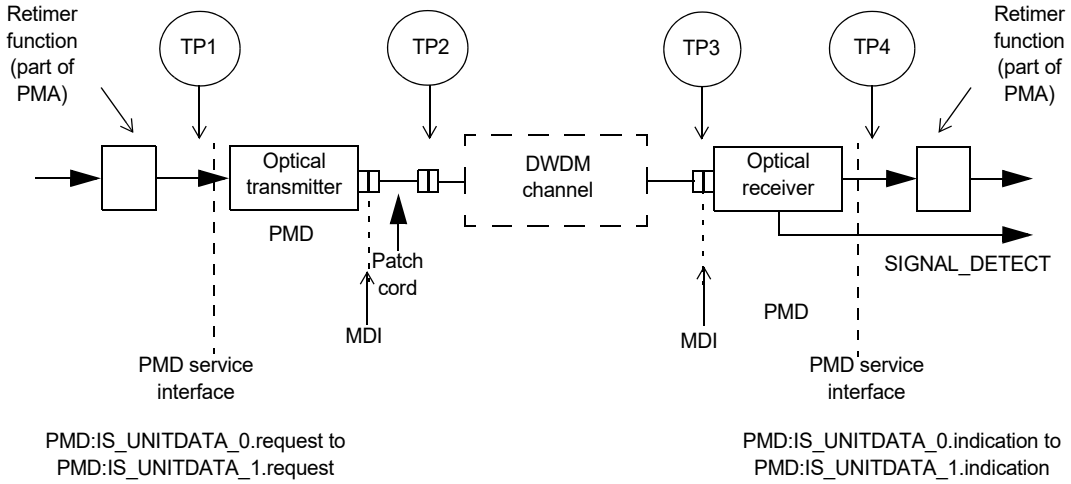

Figure 154–2—Block diagram for 100GBASE-ZR transmit/receive paths

154.5.2 PMD transmit function

The PMD Transmit function shall convert the two DQPSK symbol streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request(tx_symbol) and PMD:IS_UNITDATA_1.request(tx_symbol) into two DQPSK optical signals on orthogonal polarizations and delivered to the MDI, all according to the transmit optical specifications in this clause.

The PMD maps symbols from each tx_symbol parameter to phase changes of each of the DQPSK optical signals as specified in Table 154–4.

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Table 154–4—Symbol mapping for the phase change of one polarization of the DP-DQPSK 100 Gb/s optical signal

DQPSK symbol value	Phase change between successive symbols (radians)
0	0
1	$\pi/2$, $-3\pi/2$
2	π, $-\pi$
3	$3\pi/2$, $-\pi/2$

154.5.3 PMD receive function

The PMD Receive function shall convert the composite optical signal received from the MDI into two DQPSK symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication(rx_symbol) and PMD:IS_UNITDATA_1.indication(rx_symbol), all according to the receive optical specifications in this clause. The PMD maps the phase changes of each of the retrieved DQPSK signals to the DQPSK rx_symbol streams for delivery to the PMD service interface, as specified in Table 154–4.

NOTE—After transmission through the DWDM black link the direct correlation between symbol stream and polarization has been lost due to non-negligible polarization rotation and signal mixing. It is therefore the task of the receiver to retrieve the original symbol streams transmitted from the composite optical signal at TP3.

154.5.4 PMD global signal detect function

The PMD global signal detect function shall set the state of the SIGNAL_DETECT parameter to a fixed OK value. The presence of a valid signal is determined only by the SC-FEC sublayer (see 153.2.1).

NOTE—Average input power is not a reliable indication of signal failure in an optically amplified system.

154.5.5 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

154.5.6 PMD global transmit disable function (optional)

The PMD global transmit disable function is optional and allows the optical transmitter to be disabled.

a) When the PMD_global_transmit_disable variable is set to one, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of the OFF transmitter in Table 154–7.
b) If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter.

154.5.7 PMD fault function (optional)

If the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

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154.5.8 PMD transmit fault function (optional)

If the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

154.5.9 PMD receive fault function (optional)

If the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

154.6 DWDM channel over a DWDM black link

This subclause provides details of the medium associated with the 100GBASE-ZR PMD, over which the PHY operates at a single optical frequency (often also referred to by its associated wavelength) on a defined frequency grid. The medium associated with the 100GBASE-ZR PMD (excluding the patch cord between the MDI and TP2, if present) is also referred to as a DWDM channel.

In this application, DWDM technology is used to enable the transport of multiple DWDM channels over a single fiber. A black link approach is used to allow specification of the (single) DWDM channel in a way that takes into account the effects of other DWDM channels that may be simultaneously present on the multi-channel part of the link. By using this methodology this PMD type can support a wide range of applications, as long as the link requirements specified in 154.8 are met.

Figure 154–3 shows a generic example of a DWDM black link. Functions carried out by the DWDM black link may include:

— Optical wavelength division multiplexing and demultiplexing.
— Simultaneous transport of a number of DWDM channels on a single fiber, where the channels supporting the full duplex links may be implemented on one fiber per direction, as illustrated in Figure 154A–1, or implemented on one fiber for both directions, as illustrated in Figure 154A–2.
— Optical amplification.

The arrangement of (DWDM) elements within the DWDM black link example shown in Figure 154–3 is not intended to place constraints on the construction of the DWDM black link, but simply to define the location of the single channel interfaces at TP2 and TP3. The DWDM black link in Figure 154–3 is an example of a DWDM black link, where a grey shaded box is used to illustrate that the details of the DWDM black link are not specified.

The black link approach implies that no details are provided on how the DWDM black link is constructed, configured or operated so that the end-to-end parameter requirements are met. This approach enables interoperability at the single-channel points (TP2 and TP3). However, it does not enable interoperability at multichannel points between TP2 and TP3 inside the DWDM black link.

NOTE 1—The presence of one or more optical add-drop multiplexers (OADMs) is not directly assumed but also not specifically excluded as long at the end-to-end link requirements are met.

Optical interface parameters are specified only at the single-channel points at the input (TP2 in Figure 154–2) and output (TP3 in Figure 154–2) of the DWDM black link, which are applicable for all

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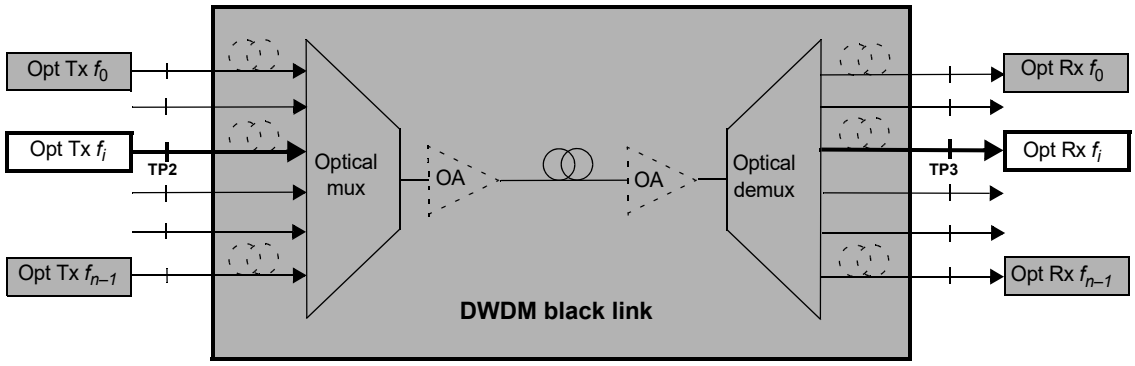
channel frequencies f_i. Additional specifications are provided for the transfer parameters from TP2 to TP3, such as chromatic dispersion, ripple, polarization mode dispersion, etc. In this way the (single channel) DWDM channel is completely specified.

NOTE 2—Coexistence of DWDM optical signals with characteristics other than the 100GBASE-ZR PMD over the same DWDM black link is not covered by this standard.



For clarity, only one direction of transmission is shown

Figure 154–3—DWDM black link example configuration for specifying *n* DWDM channels

The 100GBASE-ZR PMD is specified on the basis that it can be connected to a DWDM black link that contains a portion where multiple DWDM optical channels are present, each connected to a separate 100GBASE-ZR transmitter. These multiple DWDM channels have optical channel center frequencies that are part of a DWDM frequency grid defined in ITU-T G.694.1. Table 154–5 shows the mapping of the 100GBASE-ZR channel index numbers to the optical channel center frequencies. The 100GBASE-ZR PMD specification covers a maximum of 48 channels over a DWDM black link that supports between 1 and 48 channels with center frequencies defined in Table 154–5. In a working 100GBASE-ZR link the PMD operates on one of 48 frequencies in each direction of transmission over a pair of DWDM channels. The 100GBASE-ZR Tx, the associated DWDM channel, and the 100GBASE-ZR Rx connected to the output of the DWDM black link, are all selected to have the same channel center frequency.

Table 154–5—Mapping of the 100GBASE-ZR channel index numbers to optical channel center frequencies

Channel index number	Channel center frequency [THz]	Approximate channel center wavelength [nm]	Channel index number	Channel center frequency [THz]	Approximate channel center wavelength [nm]
0	191.4	1566.31	24	193.8	1546.92
1	191.5	1565.50	25	193.9	1546.12
2	191.6	1564.68	26	194	1545.32
3	191.7	1563.86	27	194.1	1544.53
4	191.8	1563.05	28	194.2	1543.73
5	191.9	1562.23	29	194.3	1542.94
6	192	1561.42	30	194.4	1542.14

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Table 154–5—Mapping of the 100GBASE-ZR channel index numbers to optical channel center frequencies *(continued)*

Channel index number	Channel center frequency [THz]	Approximate channel center wavelength [nm]	Channel index number	Channel center frequency [THz]	Approximate channel center wavelength [nm]
7	192.1	1560.61	31	194.5	1541.35
8	192.2	1559.79	32	194.6	1540.56
9	192.3	1558.98	33	194.7	1539.77
10	192.4	1558.17	34	194.8	1538.98
11	192.5	1557.36	35	194.9	1538.19
12	192.6	1556.55	36	195	1537.40
13	192.7	1555.75	37	195.1	1536.61
14	192.8	1554.94	38	195.2	1535.82
15	192.9	1554.13	39	195.3	1535.04
16	193	1553.33	40	195.4	1534.25
17	193.1	1552.52	41	195.5	1533.47
18	193.2	1551.72	42	195.6	1532.68
19	193.3	1550.92	43	195.7	1531.90
20	193.4	1550.12	44	195.8	1531.12
21	193.5	1549.32	45	195.9	1530.33
22	193.6	1548.51	46	196	1529.55
23	193.7	1547.72	47	196.1	1528.77

The transmitter nominal center frequency is the optical frequency in Table 154–5 corresponding to the variable Tx_optical_channel_index. If the PMD is able to operate with an Rx_optical_channel_index that is different from the Tx_optical_channel_index (Tx_Rx_diff_opt_chan_ability is one), the receiver nominal center frequency is the optical frequency in Table 154–5 corresponding to the variable Rx_optical_channel_index, otherwise it is the same as the transmitter nominal center frequency. The mapping of the Tx_optical_channel_index, the Rx_optical_channel_index, and the Tx_Rx_diff_opt_chan_ability variables to the relevant optional MDIO variables and PMA/PMD register names is shown in 154.4.

154.7 PMD to MDI optical specifications for 100GBASE-ZR

The operating range for the 100GBASE-ZR PMD is defined in Table 154–6. A 100GBASE-ZR compliant PMD operates over a DWDM black link meeting the specifications in Table 154–9. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant

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(e.g., a 100GBASE-ZR PMD that could operate over 90 km would meet the operating range requirement of 2 m to 80 km).

Table 154–6—100GBASE-ZR operating range

PMD type	Required operating range
100GBASE-ZR	2 m to 80 km

154.7.1 100GBASE-ZR transmitter optical specifications

The 100GBASE-ZR transmitter shall meet the specifications defined in Table 154–7 per the definitions in 154.9.

Table 154–7—100GBASE-ZR transmit characteristics

Description	Value	Unit
Signaling rate (range)	27.9525 ± 20 ppm	GBd
Modulation format	DP-DQPSK	—
Minimum channel spacing	100	GHz
Average channel output power (max)	0	dBm
Average channel output power (min)	–8	dBm
Nominal center frequency	The frequency in Table 154–5 where the channel index number equals the variable Tx_optical_channel_index	THz
Spectral excursion (max)	±15	GHz
Side-mode suppression ratio (SMSR) (min)	30	dB
Laser linewidth (max)	1000	kHz
Offset between the carrier and the nominal center frequency (max)	1.8	GHz
Power difference between X and Y polarizations (max)	1.5	dB
Skew between X and Y polarizations (max)	10	ps
Error vector magnitude (max)	23	%
I-Q offset (max)	–25	dB
Transmitter in-band OSNR (min)	35	dB (12.5 GHz)
Average launch power of OFF transmitter (max)	–35	dBm
Transmitter reflectance[a] (max)	–20	dB

[a] Transmitter reflectance is defined looking into the transmitter.

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154.7.2 100GBASE-ZR receive optical specifications

The 100GBASE-ZR receiver shall meet the specifications defined in Table 154–8 per the definitions in 154.9.

Table 154–8—100GBASE-ZR receive characteristics

Description	Value	Unit
Signaling rate (range)	27.9525 ± 20 ppm	GBd
Modulation format	DP-DQPSK	—
Nominal center frequency	The frequency in Table 154–5 where the channel index number equals the variable Rx_optical_channel_index	THz
Damage threshold[a]	3	dBm
Average receive power (max)	0	dBm
Average receive power (min)	–27	dBm
Receiver sensitivity[b] (max)	–30	dBm
Receiver OSNR (min): for average receive power < –16 dBm for average receive power ≥ –16 dBm	 35 19.5	 dB (12.5 GHz) dB (12.5 GHz)
Receiver OSNR tolerance[b] for average receive power ≥ –16 dBm	16.5	dB (12.5 GHz)
Receiver reflectance (max)	–20	dB

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
[b] Receiver sensitivity (max), for OSNR ≥ 35 dB (12.5 GHz), and Receiver OSNR tolerance are optional.

154.8 100GBASE-ZR DWDM black link transfer characteristics

The 100GBASE-ZR DWDM black link characteristics shall meet the specifications defined in Table 154–9 per the definitions in 154.9. Some clarification of the requirements in Table 154–9 is provided in informative Annex 154A, as well as examples of compliant DWDM black links.

154.9 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

154.9.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 154–11 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 154–11 may be used to perform that test. The test pattern used in this clause is shown in Table 154–10.

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Table 154–9—100GBASE-ZR DWDM black link characteristics

Description	Value	Unit
Channel spacing (min)	100	GHz
Ripple (max)	2.5	dB
Average output power at TP3 (max)	0	dBm
Average output power at TP3 (min): for OSNR at TP3 < 35 dB (12.5 GHz) for OSNR at TP3 ≥ 35 dB (12.5 GHz)	 –16 –27	 dBm dBm
OSNR at TP3 (min)	19.5	dB (12.5 GHz)
Optical path OSNR penalty (max), for OSNR at TP3 < 35 dB (12.5 GHz)	3	dB
Optical path power penalty (max), for OSNR at TP3 ≥ 35 dB (12.5 GHz)	3	dB
Chromatic dispersion (max)	2000	ps/nm
Chromatic dispersion (min)	0	ps/nm
Fiber chromatic dispersion slope at channel center frequencies[a] (min)	0.05	ps/nm^2 km
Optical return loss at TP2 (min)	25	dB
Maximum differential group delay, DGD_max[b]	20	ps
Polarization dependent loss (max)	1.5	dB
Polarization rotation speed (max)	50	krad/s
Inter-channel crosstalk at TP3 (max)	–16	dB
Interferometric crosstalk at TP3 (max)	–25	dB

[a] The applicable channel center frequencies are specified in Table 154–5.
[b] Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

Table 154–10—Test pattern

Pattern	Pattern description	Defined in
5	Scrambled idle encoded by SC-FEC	82.2.11, Clause 153

Table 154–11—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Optical center frequency (wavelength)	valid 100GBASE-R signal, 5	154.9.2
Side-mode suppression ratio	valid 100GBASE-R signal, 5	154.9.2
Average channel output power	valid 100GBASE-R signal, 5	154.9.3
Spectral excursion	5	154.9.4
Laser linewidth	5	154.9.5

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Table 154–11—Test-pattern definitions and related subclauses *(continued)*

Parameter	Pattern	Related subclause
Offset between the carrier and the nominal center frequency	5	154.9.6
Power difference between X and Y polarizations	5	154.9.7
Skew between X and Y polarizations	5	154.9.8
Error vector magnitude	5	154.9.9
I-Q offset	5	154.9.10
Optical signal-to-noise ratio (OSNR)	5	154.9.11
Transmitter in-band OSNR	5	154.9.12
Average receive power	5	154.9.13
Receiver sensitivity	5	154.9.14
Receiver OSNR	5	154.9.15
Receiver OSNR tolerance	5	154.9.16
Ripple	5	154.9.17
Optical path OSNR penalty	5	154.9.18
Optical path power penalty	5	154.9.19
Polarization dependent loss	5	154.9.20
Polarization rotation speed	5	154.9.21
Inter-channel crosstalk at TP3	5	154.9.22
Interferometric crosstalk at TP3	5	154.9.23

154.9.2 Optical center frequency (wavelength) and side-mode suppression ratio (SMSR)

The optical frequency (wavelength) and SMSR shall be within the range given in Table 154–7 if measured per IEC 61280-1-3. The transmitter is modulated using the test pattern defined in Table 154–11.

154.9.3 Average channel output power

The average channel output power shall be within the limits given in Table 154–7 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using the test pattern defined in Table 154–11, per the test setup in Figure 53–6.

154.9.4 Spectral excursion

The maximum spectral excursion, as defined in ITU-T G.698.2 for DP-DQPSK signals, shall be within the limits given in Table 154–7.

154.9.5 Laser linewidth

The laser linewidth, as defined in ITU-T G.698.2, shall be within the limits given in Table 154–7.

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154.9.6 Offset between the carrier and the nominal center frequency

The offset between the carrier and the nominal center frequency, as defined in ITU-T G.698.2, shall be within the limits given in Table 154–7.

154.9.7 Power difference between X and Y polarizations

The power difference between X and Y polarizations, as defined in ITU-T G.698.2, shall be within the limits given in Table 154–7.

154.9.8 Skew between X and Y polarizations

The skew between X and Y polarizations, as defined in ITU-T G.698.2, shall be within the limits given in Table 154–7.

154.9.9 Error vector magnitude

The error vector magnitude shall be within the limits given in Table 154–7 and is as defined in ITU-T G.698.2, with the exception that the samples are acquired with the effect of a clock recovery unit (CRU) with a corner frequency of 1.5 MHz and a slope of 20 dB/decade.

NOTE—This definition in ITU-T G.698.2 includes the definition of a reference equalizer.

154.9.10 I-Q offset

The I-Q offset, as defined in ITU-T G.698.2 for DP-DQPSK signals, shall be within the limits given in Table 154–7.

154.9.11 Optical signal-to-noise ratio (OSNR)

The optical signal-to-noise ratio (OSNR) at TP3 shall be within the limits given in Table 154–9. The OSNR is defined as the ratio of the average signal power in the wanted channel to the highest noise power density (referred to 12.5 GHz) in the range of the central frequency plus and minus the maximum spectral excursion. For the purposes of this definition, the noise is defined to be that which would be present if the signal in the wanted channel were removed from the DWDM black link while keeping all other DWDM black link conditions the same (e.g., the gain and noise figure of all amplifiers).

NOTE—This definition of OSNR is consistent with the definition of OSNR in ITU-T G.698.2, except that in this clause the noise power density is referred to 12.5 GHz, instead of 0.1 nm in G.698.2. At a frequency of 193.6 GHz a measurement bandwidth of 0.1 nm is identical to 12.5 GHz.

154.9.12 Transmitter in-band OSNR

The transmitter in-band OSNR shall be within the limits given in Table 154–7. OSNR is defined in 154.9.11.

154.9.13 Average receive power

The average receive power shall be within the limits given in Table 154–8. These limits define the range of average receiver input power over which the BER requirement in 154.1.1 has to be met at the values of minimum OSNR defined in Table 154–8.

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154.9.14 Receiver sensitivity

Receiver sensitivity is defined as the minimum value of average receive power at TP3 to achieve the specified maximum BER in 154.1.1. This is to be met with a transmitter with worst-case values of error vector magnitude, optical return loss at TP2, connector degradations, and OSNR. This does not have to be met in the presence of impairments caused by the DWDM black link, such as dispersion or reflections from the optical path. These effects are specified separately in the allocation of maximum optical path power penalty.

Receiver sensitivity is optional and compliance is not required.

154.9.15 Receiver OSNR

The Receiver shall be able to tolerate an OSNR specified in Table 154–8 while achieving the specified maximum BER in 154.1.1 over the average receive power range specified in Table 154–8. This parameter is defined at TP3, which is after the DWDM black link and at the input to the receiver, and therefore includes effects associated with impairments of the transmitter and inside the DWDM black link.

OSNR is defined in 154.9.11.

154.9.16 Receiver OSNR tolerance

Receiver OSNR tolerance is as defined in ITU-T G.698.2 for “100 Gbit/s applications”, with the exception that it is valid for all frequencies, due to the definition of a measurement bandwidth of 12.5 GHz instead of 0.1 nm in ITU-T G.698.2.

OSNR tolerance is optional and compliance is not required.

154.9.17 Ripple

The ripple, as defined in ITU-T G.698.2, shall be within the limit given in Table 154–9.

154.9.18 Optical path OSNR penalty

The optical path OSNR penalty, as defined in ITU-T G.698.2, shall be within the limit given in Table 154–9.

154.9.19 Optical path power penalty

The optical path power penalty shall be within the limit given in Table 154–9 and is defined as the apparent reduction of receiver sensitivity due to distortion of the signal during its transmission over the DWDM black link, using the reference receiver as defined in Annex A of ITU-T G.698.2. It is manifested as a shift of the system's BER curves towards higher receiver input power levels. This corresponds to a positive path penalty. Negative path penalties may exist under some circumstances, but should be small. A negative path penalty indicates that a less than perfect transmitter signal has been partially improved by the path-dependent distortions. Since the path penalty is a change in the receiver's sensitivity, it is measured at the BER defined in 154.1.1.

154.9.20 Polarization dependent loss

The polarization dependent loss, as defined in ITU-T G.698.2, shall be within the limit given in Table 154–9.

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154.9.21 Polarization rotation speed

The polarization rotation speed, as defined in ITU-T G.698.2, shall be within the limit given in Table 154–9.

154.9.22 Inter-channel crosstalk at TP3

The inter-channel crosstalk at TP3, as defined in ITU-T G.698.2, shall be within the limit given in Table 154–9.

154.9.23 Interferometric crosstalk at TP3

The interferometric crosstalk at TP3, as defined in ITU-T G.698.2, shall be within the limit given in Table 154–9.

154.10 Safety, installation, environment, and labeling

154.10.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

154.10.2 Laser safety

100GBASE-ZR optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

NOTE—The laser safety requirements apply only to the single channel points at TP2 and TP3, as shown in Figure 154–3, and not to any (multi-channel) point inside the DWDM black link, which is outside the scope of this clause.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[253]

154.10.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

154.10.4 Environment

Normative specifications in this clause shall be met by a system integrating a 100GBASE-ZR PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

[253]A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

154.10.5 Electromagnetic emission

A system integrating a 100GBASE-ZR PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

154.10.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

154.10.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 100GBASE-ZR).

Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 154.10.2.

154.11 Medium Dependent Interface (MDI)

The 100GBASE-ZR PMD is coupled to the DWDM black link medium at the MDI, being the interface between the PMD and the medium. Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 154.5.1, not at the MDI.

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154.12 Protocol implementation conformance statement (PICS) proforma for Clause 154, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-ZR[254]

154.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 154, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-ZR, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

154.12.2 Identification

154.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

154.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 154, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-ZR
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[254]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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154.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
ZR	100GBASE-ZR	154.7	Device supports requirements for 100GBASE-ZR PHY	M	Yes [ ]
TP1	Reference point TP1 exposed and available for testing	154.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	154.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
*INS	Installation / cable	154.6	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
DC	Delay constraints	154.3.1	Device conforms to delay constraints	M	Yes [ ]
SC	Skew constraints	154.3.2	Device conforms to Skew and Skew Variation constraints	M	Yes [ ]
*MD	MDIO capability	154.4	Registers and interface supported	O	Yes [ ] No [ ]

154.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-ZR

154.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 100GBASE-ZR PCS and PMA	154.1		M	Yes [ ]
F2	Integration with management functions			O	Yes [ ] No [ ]
F3	Bit error ratio	154.1.1	Meets BER specified in 154.1.1	M	Yes [ ]
F4	Transmit function	154.5.2	Conveys symbols from PMD service interface to MDI	M	Yes [ ]
F5	Receive function	154.5.3	Conveys symbols from PMD service interface to MDI	M	Yes [ ]
F6	Global signal detect function	154.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	O	Yes [ ] No [ ]
F7	PMD reset function	154.5.5	Resets the PMD sublayer	O	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F8	Transmitter nominal center frequency	154.6	Controls the transmitter center frequency via the Tx_optical_channel_index variable	O	Yes [ ] No [ ]
F9	Receiver nominal center frequency	154.6	Controls the receiver center frequency via the Rx_optical_channel_index variable	O	Yes [ ] No [ ]

154.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	154.4		MD:M	Yes [ ] N/A [ ]
M2	PMD global transmit disable function	154.5.6	Disables the optical transmitter with the PMD_global_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
M3	PMD fault function	154.5.7	Sets PMD_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD transmit fault function	154.5.8	Sets PMD_transmit_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD receive fault function	154.5.9	Sets PMD_receive_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M6	PMD receive center frequency ability	154.6	Reports the ability to operate with different Tx and Rx center frequencies via the Tx_Rx_diff_opt_channel_ability variable	MD:O	Yes [ ] No [ ] N/A [ ]

154.12.4.3 PMD to MDI optical specifications for 100GBASE-ZR

Item	Feature	Subclause	Value/Comment	Status	Support
ZR1	Transmitter meets specifications in Table 154–7	154.7.1	Per definitions in 154.9	M	Yes [ ]
ZR2	Receiver meets specifications in Table 154–8	154.7.2	Per definitions in 154.9	M	Yes [ ]

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154.12.4.4 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	154.9	2 m to 5 m in length	M	Yes [ ]
OM2	Optical center frequency (wavelength) and side-mode suppression ratio (SMSR)	154.9.2	Per definitions in Table 154–11	M	Yes [ ]
OM3	Average channel output power	154.9.3	Per definitions in Table 154–11	M	Yes [ ]
OM4	Error vector magnitude	154.9.9	Per definitions in Table 154–7	M	Yes [ ]
OM5	I-Q offset	154.9.10	Per definitions in Table 154–7	M	Yes [ ]
OM6	Transmitter in-band (OSNR)	154.9.12	Per definitions in Table 154–7	M	Yes [ ]
OM7	Average receive power	154.9.13	Per definitions in Table 154–8	M	Yes [ ]
OM8	Receiver OSNR	154.9.15	Per definitions in Table 154–8	M	Yes [ ]
OM9	Receiver OSNR tolerance	154.9.16	Per definitions in Table 154–8	M	Yes [ ]

154.12.4.5 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	154.10.1	Conforms to J.2	M	Yes [ ]
ES2	Laser safety	154.10.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Temperature, humidity, and handling	154.10.6	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

154.12.4.6 Characteristics of DWDM black link and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	DWDM black link requirements	154.8	Meets the requirements in Table 154–9	M	Yes [ ]
OC2	MDI requirements	154.11	Meets IEC 61753-1 and IEC 61753-021-2	INS:M	Yes [ ] N/A [ ]

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156. Clause 156 is reserved for future use

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157. Introduction to 10 Gb/s, 25 Gb/s, and 50 Gb/s BiDi PHYs

157.1 Overview

157.1.1 Scope

This clause describes the general requirements for 10 Gb/s, 25 Gb/s, and 50 Gb/s Ethernet bidirectional Physical Layer devices (PHYs). Within this clause this family of PHYs is collectively referred to as Multi-Gigabit Ethernet BiDi PHYs. These PHYs are divided into two variants based on the direction of transmission; optical line terminal (OLT) PHYs transmit in the downstream direction and optical network unit (ONU) PHYs transmit in the upstream direction.

All Multi-Gigabit Ethernet BiDi PHYs specified herein use the IEEE 802.3 MAC sublayer operating at a data rate of 10 Gb/s, 25 Gb/s, or 50 Gb/s as appropriate and are defined for full duplex operation only.

The Multi-Gigabit Ethernet BiDi PHYs provide a frame loss ratio of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap.

157.1.2 Relationship of Multi-Gigabit Ethernet BiDi PHYs to the ISO OSI reference model

The Multi-Gigabit Ethernet BiDi PHYs couple to the IEEE 802.3 MAC. The relationships among the IEEE 802.3 Multi-Gigabit Ethernet BiDi Physical Coding Sublayer (PCS), forward error correction (FEC), physical medium attachment (PMA), and physical medium dependent (PMD) sublayers and the IEEE 802.3 MAC, with respect to the ISO Open System Interconnection (OSI) reference model are shown in Figure 157–1. While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data path widths for implementation convenience. Exceptions to this are specified in 44.1.3 (for 10 Gb/s), 105.1.2 (for 25 Gb/s), and 131.1.2 (for 50 Gb/s). In addition to these exceptions the MDI specifications for Multi-Gigabit Ethernet BiDi PHYs are as follows:

— For 10 Gb/s PHYs, see Clause 158
— For 25 Gb/s PHYs, see Clause 159
— For 50 Gb/s PHYs, see Clause 160

157.1.3 Nomenclature

For Multi-Gigabit Ethernet BiDi PHYs, the following nomenclature is used, with individual elements shown in Table 157–1:

rGBASE-BRx-d

Table 157–1—PMD parameter elements

Parameter	Description	Allowed values
r	PMD rate	10, 25, 50
x	PMD reach in km	10, 20, 40
d	PMD transmit direction	D = OLT PMDs, U = ONU PMDs

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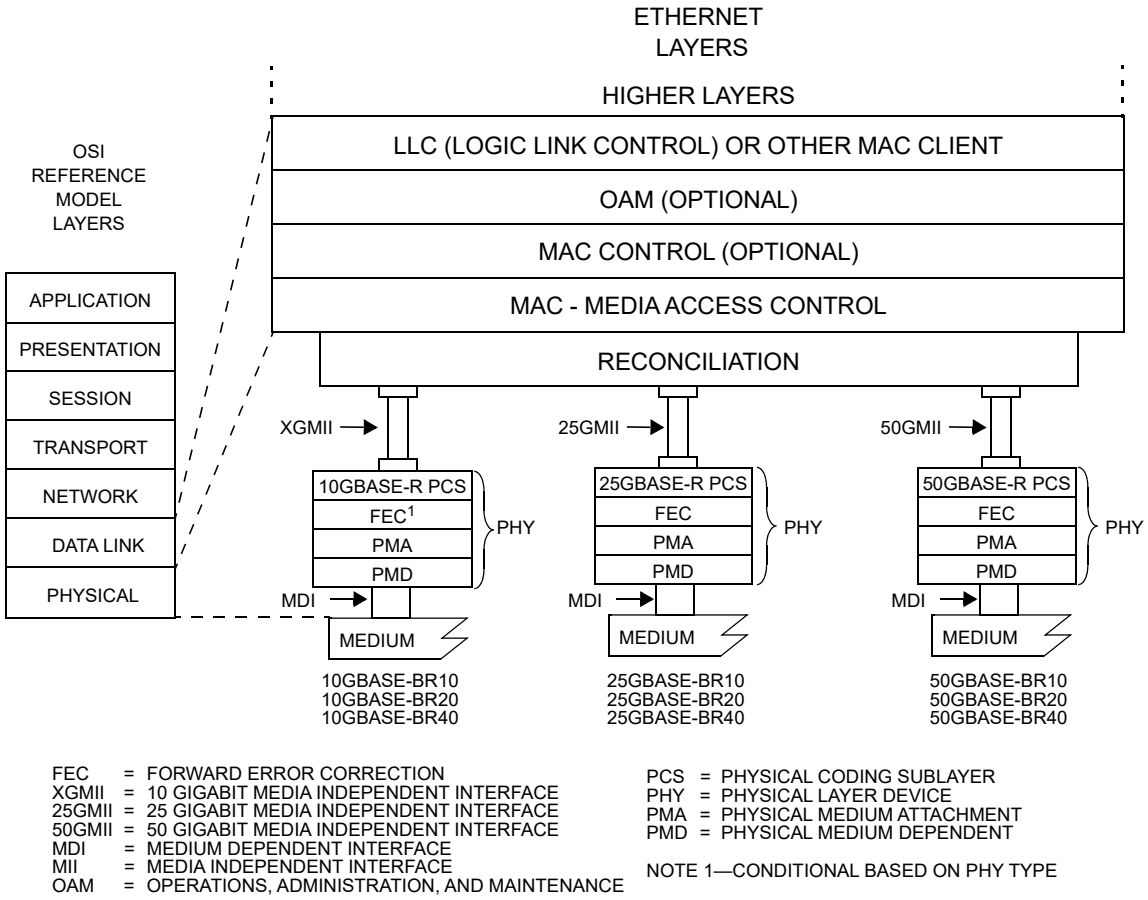

Figure 157–1—Architectural positioning of Multi-Gigabit Ethernet BiDi PHYs

B refers to bidirectional, and R refers to the 64B/66B encoding. The term xMII is used to generically refer to the family of Media Independent Interfaces (MII) including the XGMII, 25GMII, or 50GMII. All Multi-Gigabit Ethernet BiDi PHYs are listed in Table 157–2.

Table 157–2—Multi-Gigabit Ethernet BiDi PHYs

Name	Description
10GBASE-BR10-D	10 Gb/s OLT PHY using 10GBASE-R encoding over one single-mode fiber, with reach up to at least 10 km (see Clause 158).
10GBASE-BR20-D	10 Gb/s OLT PHY using 10GBASE-R encoding over one single-mode fiber, with reach up to at least 20 km (see Clause 158).
10GBASE-BR40-D	10 Gb/s OLT PHY using 10GBASE-R encoding over one single-mode fiber, with reach up to at least 40 km (see Clause 158).
10GBASE-BR10-U	10 Gb/s ONU PHY using 10GBASE-R encoding over one single-mode fiber, with reach up to at least 10 km (see Clause 158).

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Table 157–2—Multi-Gigabit Ethernet BiDi PHYs *(continued)*

Name	Description
10GBASE-BR20-U	10 Gb/s ONU PHY using 10GBASE-R encoding over one single-mode fiber, with reach up to at least 20 km (see Clause 158).
10GBASE-BR40-U	10 Gb/s ONU PHY using 10GBASE-R encoding over one single-mode fiber, with reach up to at least 40 km (see Clause 158).
25GBASE-BR10-D	25 Gb/s OLT PHY using 25GBASE-R encoding over one single-mode fiber, with reach up to at least 10 km (see Clause 159).
25GBASE-BR20-D	25 Gb/s OLT PHY using 25GBASE-R encoding over one single-mode fiber, with reach up to at least 20 km (see Clause 159).
25GBASE-BR40-D	25 Gb/s OLT PHY using 25GBASE-R encoding over one single-mode fiber, with reach up to at least 40 km (see Clause 159).
25GBASE-BR10-U	25 Gb/s ONU PHY using 25GBASE-R encoding over one single-mode fiber, with reach up to at least 10 km (see Clause 159).
25GBASE-BR20-U	25 Gb/s ONU PHY using 25GBASE-R encoding over one single-mode fiber, with reach up to at least 20 km (see Clause 159).
25GBASE-BR40-U	25 Gb/s ONU PHY using 25GBASE-R encoding over one single-mode fiber, with reach up to at least 40 km (see Clause 159).
50GBASE-BR10-D	50 Gb/s OLT PHY using 50GBASE-R encoding over one single-mode fiber, with reach up to at least 10 km (see Clause 160).
50GBASE-BR20-D	50 Gb/s OLT PHY using 50GBASE-R encoding over one single-mode fiber, with reach up to at least 20 km (see Clause 160).
50GBASE-BR40-D	50 Gb/s OLT PHY using 50GBASE-R encoding over one single-mode fiber, with reach up to at least 40 km (see Clause 160).
50GBASE-BR10-U	50 Gb/s ONU PHY using 50GBASE-R encoding over one single-mode fiber, with reach up to at least 10 km (see Clause 160).
50GBASE-BR20-U	50 Gb/s ONU PHY using 50GBASE-R encoding over one single-mode fiber, with reach up to at least 20 km (see Clause 160).
50GBASE-BR40-U	50 Gb/s ONU PHY using 50GBASE-R encoding over one single-mode fiber, with reach up to at least 40 km (see Clause 160).

157.1.4 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. Table 157–3, Table 157–4, and Table 157–5 specify the correlation between PHY types and specific clauses for the PCS, FEC, PMA and PMD. Implementations conforming to one or more PHY types meet the requirements of the corresponding clauses.

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Table 157–3—Nomenclature and clause correlation, 10GBASE-BRx

Nomenclature	Clause								
	78	46		49	108	51	158		
	EEE	RS	XGMII	10GBASE-R PCS	FEC	Serial PMA	10GBASE-BR10 PMD	10GBASE-BR20 PMD	10GBASE-BR40 PMD
10GBASE-BR10-D	O	M[a]	O	M		M	M		
10GBASE-BR20-D	O	M	O	M	M	M		M	
10GBASE-BR40-D	O	M	O	M		M			M
10GBASE-BR10-U	O	M	O	M		M	M		
10GBASE-BR20-U	O	M	O	M	M	M		M	
10GBASE-BR40-U	O	M	O	M		M			M

[a]M = Mandatory, O = Optional

Table 157–4—Nomenclature and clause correlation, 25GBASE-BRx

Nomenclature	Clause										
	78	106		107	108	109	109A	109B	159		
	EEE	RS	25GMII	25GBASE-R PCS	25GBASE-R FEC	PMA	25GAUI C2C	25GAUI C2M	25GBASE-BR10 PMD	25GBASE-BR20 PMD	25GBASE-BR40 PMD
25GBASE-BR10-D	O[a]	M	O	M	M	M	O	O	M		
25GBASE-BR20-D	O	M	O	M	M	M	O	O		M	
25GBASE-BR40-D	O	M	O	M	M	M	O	O			M
25GBASE-BR10-U	O	M	O	M	M	M	O	O	M		
25GBASE-BR20-U	O	M	O	M	M	M	O	O		M	
25GBASE-BR40-U	O	M	O	M	M	M	O	O			M

[a]M = Mandatory, O = Optional

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Table 157–5—Nomenclature and clause correlation, 50GBASE-BRx

Nomenclature	Clause														
	78	132		133	134	135	135B	135C	135D	135E	135F	135G	160		
	EEE	RS	50GMII	50GBASE-R PCS	50GBASE-R FEC	PMA	50GAUI C2C	50GAUI C2M	50GAUI-2 C2C	50GAUI-2 C2M	50GAUI-1 C2C	50GAUI-1 C2M	50GBASE-BR10 PMD	50GBASE-BR20 PMD	50GBASE-BR40 PMD
50GBASE-BR10-D	O[a]	M	O	M	M	M	O	O	O	O	O	O	M		
50GBASE-BR20-D	O	M	O	M	M	M	O	O	O	O	O	O		M	
50GBASE-BR40-D	O	M	O	M	M	M	O	O	O	O	O	O			M
50GBASE-BR10-U	O	M	O	M	M	M	O	O	O	O	O	O	M		
50GBASE-BR20-U	O	M	O	M	M	M	O	O	O	O	O	O		M	
50GBASE-BR40-U	O	M	O	M	M	M	O	O	O	O	O	O			M

[a]M = Mandatory, O = Optional

157.2 Summary of Multi-Gigabit Ethernet BiDi sublayers

157.2.1 Reconciliation Sublayer (RS) and Media Independent Interface (XGMII, 25GMII, and 50GMII)

The RS provides a mapping between the signals provided at the xMII and the MAC/PLS service definition. The xMII provides a logical interconnection between the MAC sublayer and Physical Layer devices (PHYs). The xMII may be physically instantiated or can logically connect layers within a device. While the xMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for the Physical Coding Sublayer (PCS). The specific RS and xMII for each Multi-Gigabit Ethernet BiDi PHY are given in Table 157–3, Table 157–4, and Table 157–5.

157.2.2 Physical Coding Sublayer (PCS)

The PCS performs encoding of data from the xMII to 64B/66B code blocks and transfers the encoded data to the PMA or FEC sublayer and performs decoding of 64B/66B blocks from the PMA or FEC sublayer and transfers the decoded data to the xMII. The specific PCS for each Multi-Gigabit Ethernet BiDi PHY is given in Table 157–3, Table 157–4, and Table 157–5.

157.2.3 Forward error correction (FEC) sublayer

An FEC sublayer is required for all Multi-Gigabit BiDi PHYs except 10GBASE-BR10 and 10GBASE-BR40, where the FEC sublayer is not applicable. The FEC sublayer can be placed in between the PCS and PMA sublayers or between two PMA sublayers. The specific FEC for each Multi-Gigabit Ethernet BiDi PHY is given in Table 157–3, Table 157–4, and Table 157–5.

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157.2.4 Physical Medium Attachment (PMA) sublayer

The PMA sublayer provides a medium independent means for the PCS or FEC sublayers to support the use of a range of physical media. The PMA performs the mapping of transmit and receive data streams between the PCS or FEC and PMA via the PMA service interface and mapping of transmit and receive data streams between the PMA and PMD via the PMD service interface.

The PMA performs retiming of the received data stream when appropriate, optionally provides data loopback at the PMA or PMD service interface, and optionally provides test pattern generation and checking. The PMA also may provide an observable electrical interface for the 25GAUI or 50GAUI chip-to-chip (C2C) or chip-to-module (C2M).

The specific PMA for each Multi-Gigabit Ethernet BiDi PHY is given in Table 157–3, Table 157–4, and Table 157–5.

157.2.5 Physical Medium Dependent (PMD) sublayer

The PMD sublayer is responsible for interfacing to the transmission medium. The MDI connects the PMD to the medium and is defined in the associated PMD clause. The specific PMD for each Multi-Gigabit Ethernet BiDi PHY is given in Table 157–3, Table 157–4, and Table 157–5.

157.2.6 Management interface (MDIO/MDC)

The optional MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMDs) and Station Management (STA) entities.

157.2.7 Management

Managed objects, attributes, and actions are defined for all Multi-Gigabit Ethernet BiDi PHY components. These items are defined in Clause 30.

157.3 Service interface specification method and notation

The service interface specification for Multi-Gigabit Ethernet BiDi Physical Layers is as per the definition in 1.2.2.

The 10GBASE-BRx PHYs use the inter-sublayer service interfaces specified in 49.2.2.

The 25GBASE-BRx PHYs use the inter-sublayer service interfaces specified in 105.4.

The 50GBASE-BRx PHYs use the inter-sublayer service interfaces specified in 131.3.

157.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The maximum delay constraints for 10GBASE-BRx PHY sublayers are specified in 44.3.

The maximum delay constraints for 25GBASE-BRx PHY sublayers are specified in 105.5.

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The maximum delay constraints for 50GBASE-BRx PHY sublayers are specified in 131.4.

157.5 ONU silent start

Silent start is provided by Multi-Gigabit Ethernet BiDi ONU PHYs to reduce the likelihood of disruption to established services if a Multi-Gigabit Ethernet BiDi ONU PHY is inadvertently attached to a point-to-multipoint network.

All members of the Multi-Gigabit Ethernet BiDi PHY family include PCS registers or variable equivalents that:

a) Indicate the receive status of the PCS (see 49.2.14.1 and 45.2.3.15.1).
b) Disable the PHYs transmitter (see 45.2.1.8).

By monitoring the PCS receive status indicator and appropriately setting the PHY transmitter control, upper layer management can prevent transmission by a Multi-Gigabit Ethernet BiDi ONU PHY when connected to an incompatible network (e.g., an EPON).

Transmission by a Multi-Gigabit Ethernet BiDi ONU PHY is disallowed whenever a receive fault is declared by the status indicator; once the status indicator declares the PCS is receiving a proper Multi-Gigabit Ethernet BiDi PHY signal for a pre-determined time period (e.g., 1 second) transmission may be enabled. Note that silent start does not apply to the OLT PHY types.

157.6 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 45, Clause 49, Clause 73, Clause 74, Clause 106 through Clause 112, Clause 114, Clause 158 through Clause 160, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the Multi-Gigabit Ethernet BiDi PICS conforms to the same notation and conventions used in 21.6.

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158. Physical Medium Dependent (PMD) sublayer and medium, types 10GBASE-BR10, 10GBASE-BR20, and 10GBASE-BR40

158.1 Overview

This clause specifies the 10GBASE-BR10, 10GBASE-BR20, and 10GBASE-BR40 PMDs together with the single-mode fiber medium, shown in Table 158–1. Within this clause these PMDs are jointly referred to by the term 10GBASE-BRx. The 10GBASE-BRx PHYs are divided into two variants based on the direction of transmission. Optical line terminal (OLT) PMDs transmit in the downstream direction and receive in the upstream direction. Optical network unit (ONU) PMDs transmit in the upstream direction and receive in the downstream direction. The PMD variant is indicated with a suffix of D for OLT PMDs and U for ONU PMDs.

In order to form a complete Physical Layer, each PMD is combined with the appropriate physical sublayers indicated in Table 158–1 and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 158–1—PMD type and associated clauses

Associated clause	10GBASE-BR10 10GBASE-BR40	10GBASE-BR20
46—RS	Required	Required
46—XGMII	Optional	Optional
47—XGXS and XAUI	Optional	Optional
49—Type R PCS	Required	Required
108—RS-FEC	Not applicable	Required[a]
51—Serial PMA	Required	Required

[a] The option to bypass the Clause 108 RS-FEC correction function is not supported (see 108.6.3).

Figure 158–1 depicts the relationships of the serial PMD (shown shaded) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

158.1.1 Bit error ratio

For the 10GBASE-BR10 and 10GBASE-BR40 PMDs, the bit error ratio (BER) shall be less than 10^{-12}.

For the 10GBASE-BR20 PMD, the BER shall be less than 5×10^{-5} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap when processed according to Clause 108. If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap when processed according to Clause 108.

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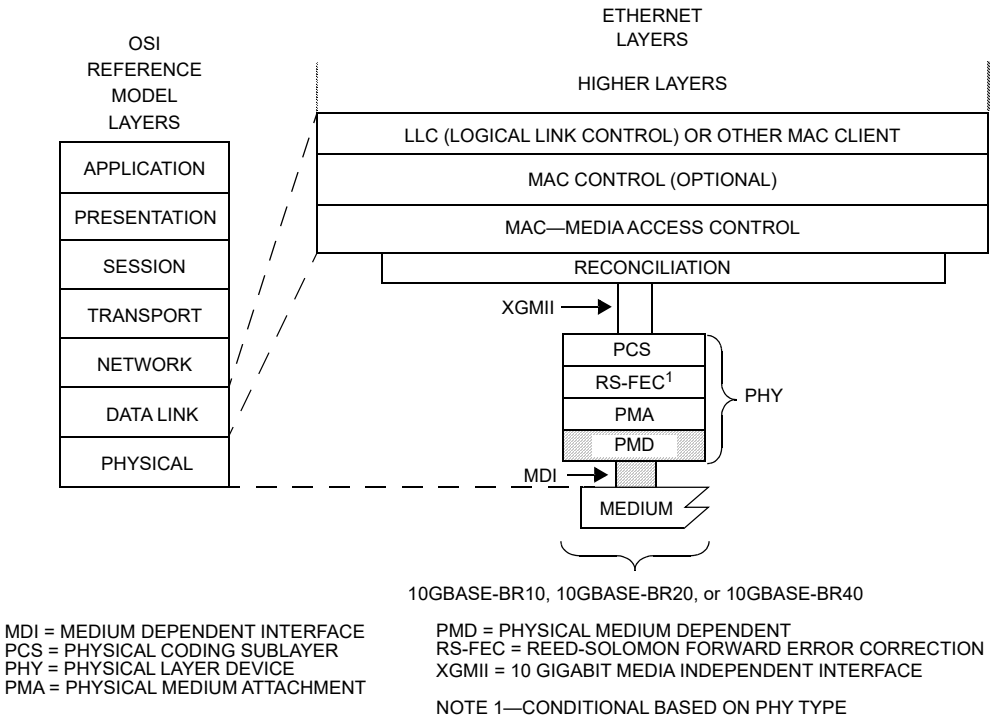

Figure 158–1—10GBASE-BRx PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

158.2 PMD sublayer service interface

The PMD service interfaces for 10GBASE-BRx are the same as PMD service interface for 10GBASE-R as described in 49.2 with the BER as specified in 158.1.1.

158.3 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation. The PMA and PMD shall incur a round-trip delay (transmit and receive) of not more than 512 bit times, or 1 pause_quantum, including 2 m of fiber. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 44.3.

158.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control variables to PMD control variables as shown in Table 158–2, and MDIO status variables to PMD status variables as shown in Table 158–3.

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Table 158–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
Global Transmit Disable	Transmit disable register	1.9.0	PMD_global_transmit_disable

Table 158–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD Receive signal detect	Receive signal detect register	1.10.0	PMD_global_signal_detect

158.5 PMD functional specifications

The 10GBASE-BRx PMDs perform the Transmit and Receive functions that convey data between the PMD service interface and the MDI.

158.5.1 PMD block diagram

For purposes of system conformance, the PMD sublayer is standardized at test points TP2 and TP3 as shown in Figure 158–2. The optical transmit signal is defined at the output end of a patch cord (TP2), between 2 m and 5 m in length, of a type consistent with the link type connected to the transmitter. Unless specified otherwise, all transmitter measurements and tests defined in 158.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) connected to the receiver. Unless specified otherwise, all receiver measurements and tests defined in 158.8 are made at TP3. TP1 and TP4 are optional reference points that may be useful to implementers for testing components (these test points are not typically accessible in an implemented system).

158.5.2 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) defined in 52.1.1.1 to the MDI according to the optical specifications in this clause. The higher optical power level shall correspond to tx_bit = ONE.

158.5.3 PMD receive function

The PMD Receive function shall convey the bits received from the MDI according to the optical specifications in this clause to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit) defined in 52.1.1.2. The higher optical power level shall correspond to rx_bit = ONE.

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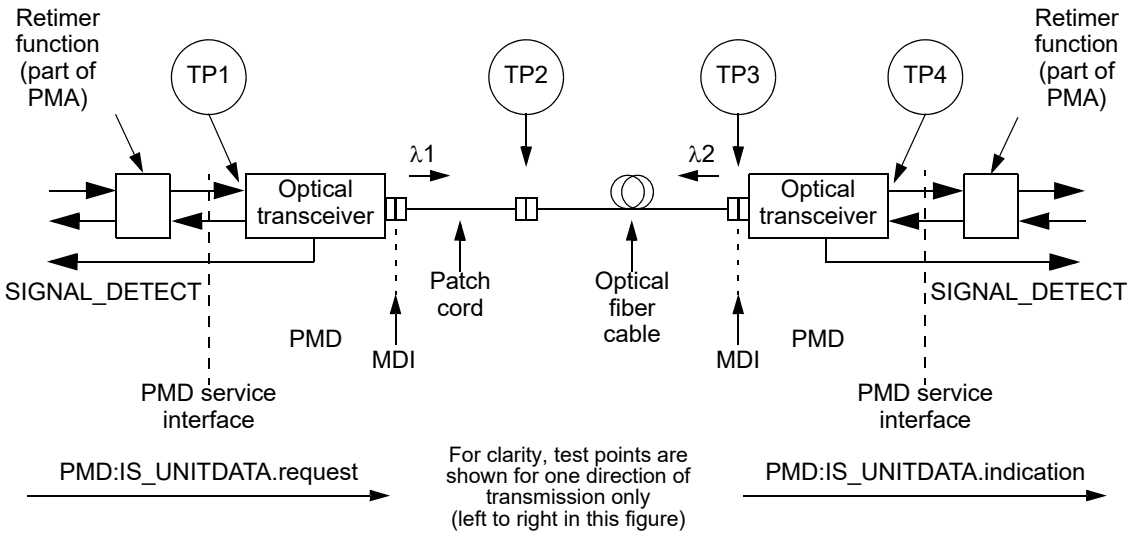

Figure 158–2—Block diagram for 10GBASE-BRx transmit/receive paths

158.5.4 PMD signal detect function

The PMD Signal Detect function shall report to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT) which is signaled continuously. PMD_SIGNAL.indication is intended to be an indicator of optical signal presence. If the MDIO interface is implemented, then PMD_global_signal_detect (MDIO register bit 1.10.0) shall be continuously set to the value of SIGNAL_DETECT as described in 45.2.1.9.7.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 158–4. The PMD receiver is not required to verify whether a compliant 10GBASE-BRx signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Implementations should provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Table 158–4—SIGNAL_DETECT value definition

Receive conditions	Signal Detect value
Input optical power ≤ –30 dBm average power for 10GBASE-BR10 and 10GBASE-BR40, input optical power ≤ –33 dBm average power for 10GBASE-BR20	FAIL
Input optical power ≥ Receiver sensitivity (max) in OMA in Table 158–7 AND compliant 10GBASE-BRx signal input	OK
All other conditions	Unspecified

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the

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modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

158.5.5 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

158.5.6 PMD global transmit disable function

PMDs compliant with this clause shall include the PMD_global_transmit_disable function that allows the optical transmitter to be disabled.

When asserted, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of OFF transmitter in Table 158–6.

If a PMD_transmit_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter.

158.5.7 PMD fault function

If the MDIO is implemented, PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault and any other implementation specific fault.

158.5.8 PMD transmit fault function

The PMD_transmit_fault function is optional. The faults detected by this function are implementation specific, but should not include the assertion of the PMD_global_transmit_disable function.

If a PMD_transmit_fault (optional) is detected, then the PMD_global_transmit_disable function should also be asserted.

158.5.9 PMD receive fault function

The 10GBASE-BRx-U PMD shall include the PMD_receive_fault function, in the 10GBASE-BRx-D PMD this function is optional. PMD_receive_fault is the logical OR of NOT SIGNAL_DETECT and any implementation specific fault.

158.5.10 ONU silent start

Silent start shall be provided by 10GBASE-BR10-U, 10GBASE-BR20-U, and 10GBASE-BR40-U PHYs. See 157.5.

158.6 PMD to MDI optical specifications for 10GBASE-BRx

The operating range for 10GBASE-BR10, 10GBASE-BR20, and 10GBASE-BR40 PMDs is defined in Table 158–5. A 10GBASE-BRx compliant PMD supports Types B1.1 and B1.3 single-mode fibers according to the specifications defined in 158.11. A PMD that exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., operating at 12.5 km meets the minimum range requirement of 2 m to 10 km).

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Table 158–5—10GBASE-BRx operating ranges

PMD Type	Required operating range
10GBASE-BR10	2 m to 10 km
10GBASE-BR20[a]	2 m to 20 km
10GBASE-BR40	2 m to 40 km

[a] The RS-FEC correction function may not be bypassed for any operating distance.

158.6.1 10GBASE-BRx transmitter optical specifications

The 10GBASE-BR10, 10GBASE-BR20, and 10GBASE-BR40 transmitters shall meet the specifications defined in Table 158–6 per the measurement techniques defined in 158.8.

Table 158–6—10GBASE-BRx transmit characteristics

Description	10GBASE-BR10	10GBASE-BR20	10GBASE-BR40	Unit
Signaling speed (nominal)	10.3125			GBd
Signaling speed variation from nominal (max)	±100			ppm
10GBASE-BRx-D center wavelength (range)	1320 to 1340			nm
10GBASE-BRx-U center wavelength (range)	1260 to 1280			nm
Side-mode suppression ratio (min)	30			dB
Average launch power (max)	0.5	–5.6	3	dBm
Average launch power[a] (min)	–8.2	–12	–3	dBm
Optical Modulation Amplitude[b] (OMA) (min)	–5.2	–9	0	dBm
Transmitter and dispersion penalty (TDP) (max)	3.2	2	2.6	dB
Launch power (min) in OMA minus TDP	–6.2	–10	–1	dBm
Average launch power of OFF transmitter[c] (max)	–30			dBm
Extinction ratio (min)	3.5	5	5.5	dB
RIN_xOMA (max)[d]	–128			dB/Hz
Optical return loss tolerance (max)	12	21		dB
Transmitter reflectance[e] (max)	–12			dB
Transmitter eye mask definition B {X1, X2, X3, Y1, Y2, Y3}, hit ratio 5×10^{-5} per sample	{0.235, 0.395, 0.45, 0.235, 0.265, 0.4}			—

[a] Average launch power (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b] The OMA (min) requirement holds even if the TDP < 1 dB.
[c] Examples of an OFF transmitter are: no power supplied to the PMD, laser shutdown for safety conditions, activation of a PMD_global_transmit_disable, or other optional transmitter shutdown conditions.
[d] In RIN_xOMA, "*x*" is the optical return loss tolerance (max) for the PHY under test.
[e] Transmitter reflectance is defined looking into the transmitter.

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158.6.2 10GBASE-BRx receive optical specifications

The 10GBASE-BR10, 10GBASE-BR20, and 10GBASE-BR40 receivers shall meet the specifications defined in Table 158–7 per the measurement techniques defined in 158.8.

Table 158–7—10GBASE-BRx receive characteristics

Description	10GBASE-BR10	10GBASE-BR20	10GBASE-BR40	Unit
Signaling speed (nominal)	10.3125			GBd
Signaling speed variation from nominal (max)	±100			ppm
10GBASE-BRx-D center wavelength (range)	1260 to 1280			nm
10GBASE-BRx-U center wavelength (range)	1320 to 1340			nm
Damage threshold[a] (min)	4	–4.6	4	dBm
Average receive power (max)	0.5	–5.6	–7	dBm
Average receive power[b] (min)	–14.4	–27.2	–21.2	dBm
Receiver sensitivity (max) in OMA[c]	–12.6	–25	–19	dBm
Receiver reflectance (max)	–12	–26		dB
Stressed receiver sensitivity (max) in OMA[d, e]	–10.3	–22.7	–16.8	dBm
Conditions of stressed receiver sensitivity test:				
Vertical eye closure penalty[f] (min)	2.2	—	2.7	dB
Stressed eye jitter[g] (min)	0.3	—	0.3	UI pk-pk
Stressed eye closure[h]	—	2.5	—	dB
Stressed eye J2 Jitter[h]	—	0.27	—	UI
Stressed eye J4 Jitter[h]	—	0.39	—	UI
SRS eye mask definition {X1, X2, X3, Y1, Y2, Y3}, hit ratio 5×10^{-5} hits per sample	—	{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}	—	—

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
[b] Average receive power (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] Receiver sensitivity is optional.
[d] Measured with conformance test signal at TP3 (see 158.8.9.1.3) for BER = 10^{-12} for BR10 and BR40, and for BER = 5×10^{-5} for BR20.
[e] The stressed sensitivity values in the table are for system level BER measurements, which include the effects of CDR circuits. It is recommended that at least 0.4 dB additional margin be allocated if component level measurements are made without the effect of CDR circuits.
[f] Vertical eye closure penalty is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.
[g] Stressed eye jitter is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.
[h] Stressed eye closure, stressed eye J2 Jitter, and stressed eye J4 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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158.6.3 10GBASE-BRx illustrative link power budgets

Illustrative power budgets and penalties for a 10GBASE-BRx channel are shown in Table 158–8.

Table 158–8—10GBASE-BRx illustrative link power budget[a, b]

Parameter	10GBASE-BR10	10GBASE-BR20	10GBASE-BR40	Unit
Power budget	9.4	18	21	dB
Operating distance	10	20	40[c]	km
Channel insertion loss	6.2[d]	15[e]	18[e]	dB
Maximum discrete reflectance (max)	–26			dB
Allocation for penalties	3.2	3		dB

[a] Budget numbers are rounded to nearest 0.1 dB.
[b] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[c] Links longer than 30 km are considered engineered links.
[d] The channel insertion loss is calculated using the maximum distance specified in Table 158–5 and cabled optical fiber attenuation of 0.4 dB/km plus an allocation for connection and splice loss given in 158.11.2.1.
[e] The channel insertion loss is calculated using the maximum distance specified in Table 158–5 and cabled optical fiber attenuation of 0.5 dB/km plus an allocation for connection and splice loss given in 158.11.2.1.

158.7 Jitter specifications for 10GBASE-BRx

The jitter specifications for 10GBASE-BRx are defined by the transmitter eye mask requirements in Table 158–7, using the definitions in 158.8.7 and the reference receiver defined in 158.8.10.3.

158.8 Definition of optical parameters and measurement methods

All optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

158.8.1 Test patterns

Compliance is to be achieved in normal operation. Two types of test pattern are used, square wave (158.8.1.2) and others (158.8.1.1). Table 158–11 shows the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined.

Test pattern generation and checking functions, such as the ones defined in 49.2.8 and in 49.2.12, are required for testing a PMD. Tests may utilize test pattern generators and checkers in other sublayers (e.g., the PCS of Clause 49) or in the test equipment, as appropriate.

NOTE—Test patterns for specific optical tests are designed to emulate system operation, which would entail passing valid 10GBASE-BRx data.

158.8.1.1 Test pattern definition

Patterns 1, 2, and 3 are defined in Table 158–10.

For 10GBASE-BRx, two test pattern segments are specified, in two variants, “normal” (n) and “inverted” (i). Both are 8448 bits long. They may be generated dynamically by the 58-bit scrambler and

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"control block" sync header generation defined in 49.2.6, and using the scrambler starting seeds specified in Table 158–9 and the method of generation in 49.2.8. The segments are assembled into patterns, each containing four segments, as described in Table 158–10. Each may be held as a static pattern in test equipment, or generated or detected dynamically using the methods of 49.2.8 and 49.2.12 respectively, or otherwise.

Each segment contains a sync header transition every 66 bits.

Table 158–9—Pattern segments

Segments	Seed[57:0][a]
A_n	0x3C8B44DCAB6804F
B_n	0x34906BB85A38884

[a] The "invert" segments A_i and B_i are generated using the inverted seeds for A_n and B_n, respectively.

Table 158–10—Test patterns

Pattern	Pattern for 10GBASE-R
1	$B_n\, B_i\, B_n\, B_i$
2	$A_n\, A_i\, A_n\, A_i$
3	PRBS31[a]

[a] The PRBS31 test pattern is identical to the one defined in 49.2.8.

Test pattern 1 is generated with the data input mode programmed to select LF data input. Test pattern 2 is generated with the data input mode programmed to select all zero data input.

Pattern 1 represents typical scrambled data while pattern 2 represents a less typical pattern that could happen by chance and is thought to be more demanding of the transmission process including the clock recovery subsystem. Both patterns are balanced over their length of 33 792 bits.

NOTE—While other test methods and patterns could be used, it is the implementer's responsibility to ensure that measurements carried out with the specified patterns achieve the requirements specified.

158.8.1.2 Square wave pattern definition

A pattern consisting of four to eleven consecutive ones followed by an equal run of zeros may be used as a square wave. These patterns have fundamental frequencies between approximately 469 MHz and 1289 MHz.

158.8.2 Wavelength and side-mode suppression ratio (SMSR)

The wavelength and SMSR shall be within the range given in Table 158–6 if measured per IEC 61280-1-3. The transmitter is modulated using the test pattern defined in Table 158–11.

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Table 158–11—Test pattern definitions and related subclauses

Test	Pattern	Related subclause
Average optical power	1, 3, or valid 10GBASE-R signal	158.8.3
OMA (modulated optical power)	Square	158.8.5
Extinction ratio	1 or 3	158.8.4
Transmit eye	1 or 3	158.8.7
RIN_xOMA	Square	158.8.6
Wavelength	1, 3, or valid 10GBASE-R signal	158.8.2
Side-mode suppression ratio	1, 3, or valid 10GBASE-R signal	158.8.2
Vertical eye closure penalty calibration	2 or 3	158.8.9
Receiver sensitivity	1 or 3	158.8.9
Receiver overload	1 or 3	—
Stressed receive conformance	2 or 3	158.8.9
Transmitter and dispersion penalty	2 or 3	158.8.10

158.8.3 Average optical power

The average optical power shall be within the limits given in Table 158–6 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using the test pattern specified in Table 158–11.

158.8.4 Extinction ratio

The extinction ratio shall be within the limits given in Table 158–6 if measured using the methods specified in IEC 61280-2-2. The extinction ratio is measured using the test pattern defined in Table 158–11.

158.8.5 Optical Modulation Amplitude (OMA)

OMA shall meet the requirements in Table 158–7 when measured using the method defined in 52.9.5. See 158.8.1 for test pattern information.

158.8.6 Relative Intensity Noise (RIN_xOMA)

RIN_xOMA shall meet the requirement in Table 158–7 when measured using the method of 52.9.6, with x being the “Optical return loss tolerance (max)” specified in Table 158–7 for the PMD under test.

158.8.7 Transmitter optical waveform (transmitter eye)

The required optical transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 86–4. The transmitter optical waveform of a port transmitting

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the test pattern specified in Table 158–11 shall meet specifications according to the methods specified in 86.8.4.6.1 with the filter nominal reference frequency f_r of 7.5 GHz and the filter tolerances as specified for STM-64 in ITU-T G.691. Compensation may be made for variation of the reference receiver filter response from an ideal fourth-order Bessel-Thomson response.

158.8.8 Receiver sensitivity

Receiver sensitivity, which is defined for an ideal input signal, is optional and testing is not required. If measured, the test signal should have negligible impairments such as intersymbol interference (ISI), rise/fall times, jitter and RIN. Instead, the normative requirement for receivers is stressed receiver sensitivity.

158.8.9 Stressed receiver sensitivity

158.8.9.1 Stressed receiver sensitivity for 10GBASE-BR10 and 10GBASE-BR40

Stressed receiver sensitivity shall be within the limits given in Table 158–7 if measured using the method defined in 158.8.9.1.1, 158.8.9.1.2, and 158.8.9.1.4, with the conformance test signal at TP3 as described in 158.8.9.1.3 and 158.8.9.1.5, using the test pattern specified for SRS in Table 158–11.

Receivers shall operate with BER less than 10^{-12} when tested with a conditioned input signal that combines vertical eye closure and jitter according to this clause.

The measurements in this subclause are performed with asynchronous data flowing out of the optical transmitter of the system under test. The output data pattern from the transmitter of the system under test is to be the same pattern defined for this measurement in 158.8.1. The reflectance of the optical link should be at its maximum level.

158.8.9.1.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 158–3. A suitable pattern generator is used to continuously generate a signal or test pattern according to 158.8.1. The optical test signal is conditioned (stressed) using the methodology as defined in 158.8.9.1.3, while applying sinusoidal jitter as defined in 158.8.9.1.5. The receiver of the system under test is tested for conformance by enabling the error counter on the receiving side. The optical power penalty for the stressed eye is intended to be similar to its vertical eye closure penalty. This is not necessarily the same as the highest TDP anticipated in service, but represents a standardized test condition for the receiver.

A suitable test set is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics. The test fiber called out for 10GBASE-BRx is not needed to characterize the receiver input signal; nor is it used during testing.

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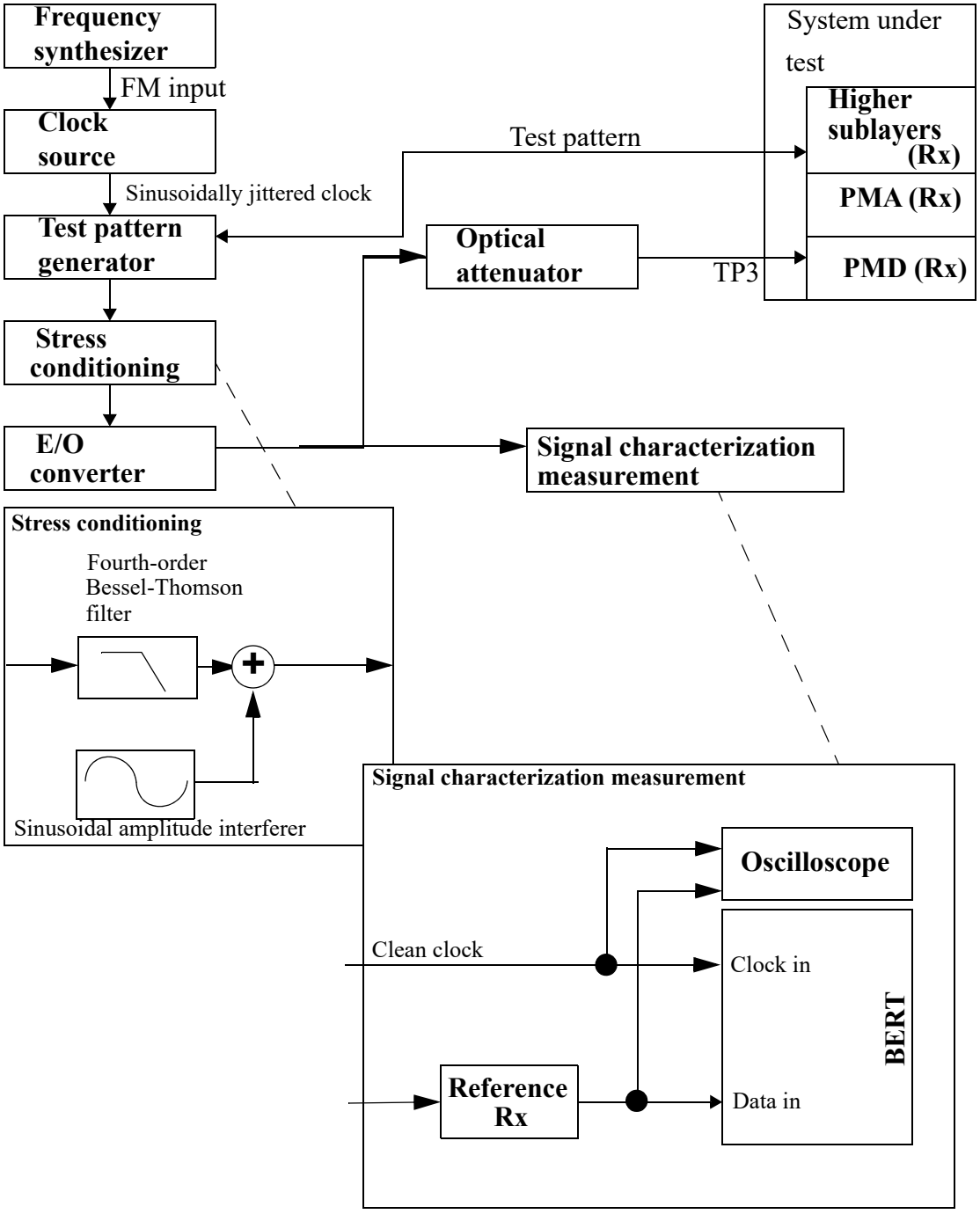

Figure 158–3—Stressed receiver conformance test block diagram

The fourth-order Bessel-Thomson filter is used to create ISI-induced vertical eye closure penalty (VECP). The sinusoidal amplitude interferer causes additional eye closure, but in conjunction with the slowed edge rates from the filter, also causes jitter. The nature of the jitter is intended to emulate instantaneous bit shrinkage that can occur with DDJ. This type of jitter cannot be created by simple phase modulation. The sinusoidal phase modulation represents other forms of jitter and also verifies that the receiver under test can

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track low-frequency jitter. The frequency of the sinusoidal interference may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid a harmonic relationship between the sinusoidal interference, the sinusoidal jitter, the data rate, and the pattern repetition rate.

For improved visibility for calibration, it is imperative that the Bessel-Thomson filter and all other elements in the signal path (cables, DC blocks, E/O converter, etc.) have wide and smooth frequency response and linear phase response throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be minimized. If this is achieved, then data dependent effects should be minimal, and short data patterns can be used for calibration with the benefit of providing much improved trace visibility on sampling oscilloscopes. Actual patterns for testing the receiver shall be as specified in Table 158–11.

To further improve visibility for calibration, random noise effects, such as RIN and random clock jitter, should also be minimized. A small amount of residual noise and jitter from all sources is unavoidable, but should be less than 0.25 UI peak-peak of jitter at the 10^{-12} points.

The Bessel-Thomson filter and the E/O converter should have the appropriate frequency response to result in the appropriate level of initial ISI eye closure before the sinusoidal terms are added. The E/O converter should be fast and linear such that the waveshape and edge rates are predominantly controlled or limited by the electrical circuitry. Electrical summing requires high linearity of all elements including the E/O converter. Summing with an optical coupler after the E/O converter is an option that eases linearity requirements, but requires a second source for the interfering signal, complicates settings of extinction ratio, and adds more RIN.

The vertical and horizontal eye closures to be used for receiver conformance testing are verified using an optical reference receiver with a 7.5 GHz fourth-order ideal Bessel-Thomson response. Use of ITU-T G.691 tolerance filters may significantly degrade this calibration. Care should be taken to ensure that all the light from the fiber is collected by the fast photodetector and that there is negligible mode selective loss, especially in the optical attenuator and the optical coupler, if used.

The clock output from the clock source in Figure 158–3 is modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye jitter that includes the sinusoidal jitter component, a separate clock source (clean clock of Figure 158–3) is required that is synchronized to the source clock, but not modulated with the jitter source.

158.8.9.1.2 Parameter definitions

The primary parameters of the conformance test signal are vertical eye closure penalty (VECP) and stressed eye jitter, J. Vertical eye closure penalty is measured at the time center of the eye (halfway between 0 and 1 on the unit interval scale as defined in 158.8.7) and is calculated relative to the measured OMA value. J is defined from the 0.5th to the 99.5th percentile of the jitter histogram. J is measured at the average optical power, which can be obtained with AC-coupling. The values of these components are defined by their histogram results.

The vertical eye closure penalty is given by Equation (158–1).

$$\text{Vertical eye closure penalty [dB, optical]} = 10 \times \log\frac{OMA}{A_O} \tag{158–1}$$

where

A_O is the amplitude of the eye opening from the 99.95th percentile of the lower histogram to the 0.05th percentile of the upper histogram.

OMA is the normal amplitude without ISI, as shown in Figure 158–4.

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158.8.9.1.3 Stressed receiver conformance test signal characteristics and calibration

The conformance test signal is used to validate that the PMD receiver meets BER requirements with near worst case waveforms including pulse width shrinkage, power, simulated channel penalties, and a swept frequency sinusoidal jitter contribution applied at TP3.

Signal characteristics are described below along with a suggested approach for calibration.

The test signal includes vertical eye closure and high-probability jitter components. For this test, these two components are defined by peak values that include all but 0.1% for VECP and all but 1% for jitter of their histograms. Histograms should include at least 10 000 hits, and should be about 1% width in the direction not being measured. Residual low-probability noise and jitter should be minimized—that is, the outer slopes of the final histograms should be as steep as possible down to very low probabilities.

The following steps describe a suggested method for calibrating a stressed eye generator:

1) Set the signaling speed of the test pattern generator to satisfy the requirements of 158.6.2.
2) Turn on the calibration pattern. A short pattern may be used for calibration if the conditions described in 158.8.9.1.1 are met, but this increases the risk that the longer test pattern used during testing over-stresses the device under test. In any case, a pattern shorter than PRBS10 is not recommended.
3) Set the extinction ratio to approximately the “Extinction ratio (min)” value given in 158.6.1. Sinusoidal interference and jitter signals should be turned off at this point. If optical summing is used, the extinction ratio may need to be adjusted after the sinusoidal interference signal is added below.
4) Measure the OMA of the test signal (without attenuation). OMA is measured per the method in 158.8.5 using the square wave pattern.
5) The requirements for vertical eye closure and jitter of the stressed eye test signal are given by the Vertical eye closure penalty (VECP) and Stressed eye jitter (J) values given in Table 158–7.

   There are three components involved in calibration for vertical eye closure and J. These are a linear phase filter, sinusoidal interference, and sinusoidal jitter.

   Without sinusoidal jitter or sinusoidal interference, greater than two thirds of the vertical eye closure penalty value should be created by use of a linear phase, low jitter filter (such as Bessel-Thomson). The filter should be tested with the prescribed test patterns to verify that residual jitter and baseline wander are small, not to exceed 0.25 UI peak-peak. If not, the stress may be more than desired, leading to conservative results. However, compensation is not allowed. Once done, revert to the calibration pattern, if different than the final test pattern specified in Table 158–11.

   Any remaining vertical eye closure required should be created with sinusoidal interference or sinusoidal jitter.

   Sinusoidal jitter (phase modulation) should be added per the template of Table 158–12. For calibration purposes, sinusoidal jitter frequencies should be well within the flat portion of the template greater than 4 MHz.

   Iterate the settings for sinusoidal interference and/or jitter until all constraints are met, including jitter (J), vertical eye closure (VECP), and that sinusoidal jitter above 4 MHz is as specified in Table 158–12.

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Verify that the optical power penalty for the stressed eye (relative to the reference transmitter per 158.8.10) is greater than or equal to VECP.

To emulate the effects of DCD or data-dependent jitter, at least 5 ps peak-to-peak of pulse shrinkage jitter should have been achieved.

6) Decrease the amplitude with the optical attenuator until the OMA complies with the OMA values given in Table 158–7 for 10GBASE-BRx. If high linearity exists, then the sinusoidal interference should not change the OMA value. OMA can be approximated with histograms as suggested in Figure 158–4. However, the normative definition for OMA is as given in 158.8.5.

7) For testing, turn on the actual required test pattern(s) per 158.8.1.

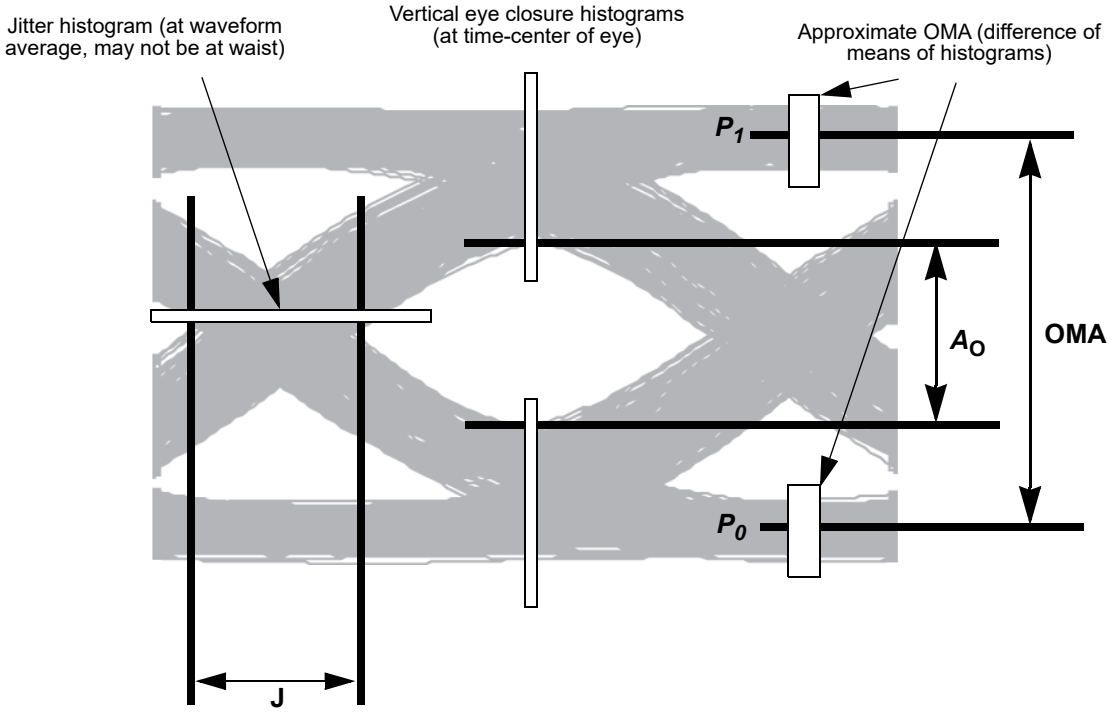

Figure 158–4—Required characteristics of the conformance test signal at TP3

Care should be taken when characterizing the signal used to make receiver tolerance measurements. In the case of a transmit jitter measurement, excessive and/or uncalibrated noise/jitter in the test system makes it more difficult to meet the specification and may have a negative impact on yield but does not effect interoperability. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. Care should be taken to minimize and/or correct for the noise/jitter introduced by the reference receiver, filters, oscilloscope, and BERT. While the details of measurement and test equipment are beyond the scope of this standard, it is recommended that the implementer fully characterize the test equipment and apply appropriate guard bands to ensure that the receive input signal meets the specified requirements.

158.8.9.1.4 Stressed receiver conformance test procedure

The test apparatus is set up as described in 158.8.9.1.1, 158.8.9.1.2 and 158.8.9.1.3. The sinusoidal jitter is then stepped across the frequency and amplitude range specified in 158.8.9.1.5 while monitoring BER at the receiver. The BER is to be compliant for all jitter frequencies. This method does not result in values for jitter contributed by the receiver. A receiver meeting the requirements of this test is expected to operate with the worst-case optical input.

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158.8.9.1.5 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table 158–12.

Table 158–12—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter, peak-to-peak (UI)
$f < 40$ kHz	Not specified
40 kHz $< f \leq 4$ MHz	2×10^5 Hz/ f
4 MHz $< f <$ 10 LB[a]	0.05

[a] LB = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

158.8.9.2 Stressed receiver sensitivity for 10GBASE-BR20

Stressed receiver sensitivity shall be within the limits given in Table 158–7 if measured using the method defined in 95.8.8 with the following exceptions:

a) The centers of the vertical histograms through the eye diagram are 0.45 UI and 0.55 UI, and the width of each histogram is 0.02 UI (see Figure 95–4).
b) Added sinusoidal jitter is as specified in Table 158–12.
c) The stressed eye J2 Jitter, stressed eye J4 Jitter, stressed eye closure, and SRS eye mask are as given in Table 158–7.
d) The test pattern is as given in Table 158–11.
e) The reference receiver used to verify the conformance test signal is required to have the bandwidth given in 158.8.7.
f) The SEC created by the selection of the appropriate bandwidth for the combination of the low-pass filter and the E/O converter with the sinusoidal jitter, sinusoidal interferer 1, sinusoidal interferer 2, and the Gaussian noise generator turned off is at least 1.5 dB.
g) The conditions for receiver aggressor lanes do not apply.
h) The reflectance of the optical link should be at its maximum level.

158.8.10 Transmitter and dispersion penalty (TDP)

Transmitter and dispersion penalty (TDP) shall be as defined in 52.9.10 with the BER as specified in 158.1.1. The measurement procedure for 10GBASE-BRx is detailed in 158.8.10.1 to 158.8.10.4.

158.8.10.1 Reference transmitter requirements

The reference transmitter is a high-quality instrument-grade device, which can be implemented by a CW laser modulated by a high-performance modulator. The basic requirements are as follows:

a) The rise/fall times are less than 30 ps at 20% to 80%.
b) The output optical eye is symmetric and passes the eye mask test of 158.8.7.
c) In the center 20% region of the eye, the worst case vertical eye closure penalty as defined in 87.8.11.2 is less than 0.5 dB.

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d) Jitter less than 0.2 UI peak-peak.

e) RIN is minimized to less than –136 dB/Hz.

158.8.10.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 158–13.

Table 158–13—Transmitter compliance channel specifications

PMD Type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c] (max)
	Minimum	Maximum		
10GBASE-BR10	$0.23 \times \lambda \times [1 - (1324 / \lambda)^4]$	$0.23 \times \lambda \times [1 - (1300 / \lambda)^4]$	Minimum	12 dB
10GBASE-BR20	$0.46 \times \lambda \times [1 - (1324 / \lambda)^4]$	$0.46 \times \lambda \times [1 - (1300 / \lambda)^4]$	Minimum	21 dB
10GBASE-BR40	$0.92 \times \lambda \times [1 - (1324 / \lambda)^4]$	$0.92 \times \lambda \times [1 - (1300 / \lambda)^4]$	Minimum	21 dB

[a] The dispersion is measured for the wavelength of the device under test. The coefficient assumes 10 km for 10GBASE-BR10, 20 km for 10GBASE-BR20, and 40 km for 10GBASE-BR40. The link may be as short as 2 m, and the minimum or maximum dispersion may be 0.
[b] There is no intent to stress the sensitivity of the BERT's optical receiver.
[c] The optical return loss is applied at TP2.

A 10GBASE-BRx transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 158–13 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides a maximum optical return loss specified in Table 158–13. The state of polarization of the back reflection is adjusted to create the greatest RIN. The method of 158.8.6 may be used.

158.8.10.3 Reference receiver requirements

The reference receiver is required to have the bandwidth given in 158.8.7. The sensitivity of the reference receiver is limited by Gaussian noise. The receiver has minimal threshold offset, deadband, hysteresis, baseline wander, deterministic jitter, or other distortions. Decision sampling is instantaneous with minimal uncertainty and setup/hold properties.

The nominal sensitivity of the reference receiver, S, is measured in OMA using the set up of Figure 52–12 without the test fiber and with the transversal filter removed. The sensitivity S has to be corrected for any significant reference transmitter impairments including any vertical eye closure. It is measured while sampling at the eye center or corrected for off-center sampling. It is calibrated at the wavelength of the transmitter under test.

For all transmitter and dispersion penalty measurements, determination of the center of the eye is required. Center of the eye is defined as the time halfway between the left and right sampling points within the eye where the measured BER is greater than or equal to 10^{-3}.

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The clock recovery unit (CRU) used in the TDP measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low-frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.

158.8.10.4 Test procedure

The test procedure is as defined in 52.9.10.4 with the BER as specified in 158.1.1.

158.9 Safety, installation, environment, and labeling

158.9.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

158.9.2 Laser safety

10GBASE-BRx optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[255]

158.9.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

158.9.4 Environment

Normative specifications in this clause shall be met by a system integrating a 10GBASE-BRx PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause are met.

158.9.5 Electromagnetic emission

A system integrating a 10GBASE-BRx PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

[255] A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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158.9.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

158.9.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 10GBASE-BR10-D). Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 158.9.2.

158.10 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 158–5.

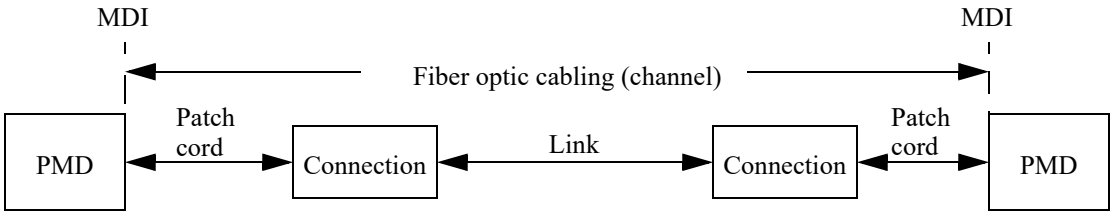

Figure 158–5—Fiber optic cabling model

The channel insertion loss is given in Table 158–8. A channel may contain additional connectors or other optical elements as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

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Table 158–14—Fiber optic cabling (channel) characteristics

Description	10GBASE-BR10	10GBASE-BR20	10GBASE-BR40	Unit
Operating distance (max)	10	20	40	km
Channel insertion loss[a, b] (max)	6.2	15	18	dB
Channel insertion loss (min)	0	0	10	dB
Positive dispersion[b] (max)	35	70	141	ps/nm
Negative dispersion[b] (min)	–64	–127	–254	ps/nm
DGD_max[c]	10	10	10	ps
Optical return loss (min)	21	21	21	dB

[a] These channel insertion loss values include cable, connectors, and splices.
[b] Over the wavelength range 1260 nm to 1340 nm.
[c] Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

158.11 Characteristics of the fiber optic cabling (channel)

The 10GBASE-BRx fiber optic cabling shall meet the specifications defined in Table 158–14. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

158.11.1 Optical fiber and cable

The optical fiber cable requirements are satisfied by cables containing ITU-T G.652.B (dispersion unshifted), type G.652.D (low water peak, dispersion unshifted), or type G.657.A1 or type G.657.A2 (bend insensitive) fibers or the requirements in Table 158–14 where they differ.

158.11.2 Optical fiber connection

An optical fiber connection, as shown in Figure 158–5, consists of a mated pair of optical connectors.

158.11.2.1 Connection insertion loss

The maximum link distances for single-mode fiber are calculated based on an allocation of 2 dB total connection and splice loss for 10GBASE-BR10 and 10GBASE-BR40. The maximum link distances for single-mode fiber are calculated based on an allocation of 5 dB total connection and splice loss for 10GBASE-BR20.

158.11.2.2 Maximum discrete reflectance

The maximum discrete reflectance for 10GBASE-BR10 shall be less than –20 dB.

The maximum discrete reflectance for 10GBASE-BR20 and 10GBASE-BR40 shall be less than –26 dB.

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158.11.3 Medium Dependent Interface (MDI) requirements

The 10GBASE-BRx PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 158–5). Examples of an MDI include the following:

a) Connectorized fiber pigtail.

b) PMD receptacle.

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1, IEC 61753-021-2, and IEC 61753-022-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 158.5.1, not at the MDI.

158.12 Requirements for interoperation between 10GBASE-BRx PMDs

The 10GBASE-BR10 and 10GBASE-BR40 PMDs can interoperate with each other (over an engineered link) provided that the fiber optic cabling (channel) characteristics are met, with the exception of the maximum and minimum channel insertion loss values, which are given in Table 158–15 for the two link directions separately. Attenuators may be used to achieve the required losses.

Table 158–15—Channel insertion loss requirements for interoperation between 10GBASE-BR10 and 10GBASE-BR40

Direction	Min loss	Max loss	Unit
10GBASE-BR10 transmitter to 10GBASE-BR40 receiver	7.5	12.8	dB
10GBASE-BR40 transmitter to10GBASE-BR10 receiver	2.5	11.6	dB

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158.13 Protocol implementation conformance statement (PICS) proforma for Clause 158, Physical Medium Dependent (PMD) sublayer and medium, types 10GBASE-BR10, 10GBASE-BR20, and 10GBASE-BR40[256]

158.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 158, Physical Medium Dependent (PMD) sublayer and medium, types 10GBASE-BR10, 10GBASE-BR20, and 10GBASE-BR40, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

158.13.2 Identification

158.13.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

158.13.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 158, Physical Medium Dependent (PMD) sublayer and medium, types 10GBASE-BR10, 10GBASE-BR20, and 10GBASE-BR40
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[256]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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158.13.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*BR10	10GBASE-BR10 PMD	158.6	Device supports requirements for 10GBASE-BR10 PHY	O.1	Yes [ ] No [ ]
*BR20	10GBASE-BR20 PMD	158.6	Device supports requirements for 10GBASE-BR20 PHY	O.1	Yes [ ] No [ ]
*BR40	10GBASE-BR40 PMD	158.6	Device supports requirements for 10GBASE-BR40 PHY	O.1	Yes [ ] No [ ]
*INS	Installation / cable	158.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	158.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	158.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	158.3	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO capability	158.4	Registers and interface supported	O	Yes [ ] No [ ]

158.13.4 PICS proforma tables for PMD sublayer and medium, types 10GBASE-BR10, 10GBASE-BR20, and 10GBASE-BR40

158.13.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 10GBASE-R PCS and PMA	158.1		M	Yes [ ]
F2	Integration with management functions	158.1		O	Yes [ ] No [ ]
F3	Bit error ratio	158.1.1	Meets the BER specified in 158.1.1	M	Yes [ ]
F4	Transmit function	158.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
F5	Mapping between optical signal and logical signal for transmitter	158.5.2	Higher optical power is a one	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F6	Receive function	158.5.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
F7	Conversion of optical signal to electrical signal	158.5.3	For delivery to the PMD service interface	M	Yes [ ]
F8	Mapping between optical signal and logical signal for receiver	158.5.3	Higher optical power is a one	M	Yes [ ]
F9	Global Signal Detect function	158.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F10	Global Signal Detect behavior	158.5.4	SIGNAL_DETECT is a global indicator of the presence of an optical signal	M	Yes [ ]
F11	PMD reset function	158.5.5	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]
F12	Jitter	158.7	Meets the specifications defined in 158.7	M	Yes [ ]
F13	ONU silent start	158.5.10	Meets the specifications defined in 158.5.10	M	Yes [ ]

158.13.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	158.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	158.5.6	Disables the optical transmitter with the PMD_global_transmit_disable variable	M	Yes [ ]
M3	PMD_receive_fault function	158.5.9	PMD_receive_fault is the logical OR of NOT SIGNAL_DETECT and any implementation specific fault	MD:O	Yes [ ] No [ ] N/A [ ]

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158.13.4.3 PMD to MDI optical specifications for 10GBASE-BR10

Item	Feature	Subclause	Value/Comment	Status	Support
BR101	Transmitter meets specifications in Table 158–6	158.6.1	Per measurement techniques defined in 158.8	BR10:M	Yes [ ] N/A [ ]
BR102	Receiver meets specifications in Table 158–7	158.6.2	Per measurement techniques defined in 158.8	BR10:M	Yes [ ] N/A [ ]

158.13.4.4 PMD to MDI optical specifications for 10GBASE-BR20

Item	Feature	Subclause	Value/Comment	Status	Support
BR201	Transmitter meets specifications in Table 158–6	158.6.1	Per measurement techniques defined in 158.8	BR20:M	Yes [ ] N/A [ ]
BR202	Receiver meets specifications in Table 158–7	158.6.2	Per measurement techniques defined in 158.8	BR20:M	Yes [ ] N/A [ ]

158.13.4.5 PMD to MDI optical specifications for 10GBASE-BR40

Item	Feature	Subclause	Value/Comment	Status	Support
BR401	Transmitter meets specifications in Table 158–6	158.6.1	Per measurement techniques defined in 158.8	BR40:M	Yes [ ] N/A [ ]
BR402	Receiver meets specifications in Table 158–7	158.6.2	Per measurement techniques defined in 158.8	BR40:M	Yes [ ] N/A [ ]

158.13.4.6 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
M1	General measurement	158.8	Meets the specifications defined in 158.8	M	Yes [ ]

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158.13.4.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	158.9.1	Conforms to J.2	M	Yes [ ]
ES2	Laser safety —IEC Hazard Level 1	158.9.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	158.9.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

158.13.4.8 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	158.11	Meets the specifications defined in Table 158–14	INS: M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	158.11.2.2	Less than –20 dB for 10GBASE-BR10, less than –26 dB for 10GBASE-BR20 and 10GBASE-BR40	INS: M	Yes [ ] N/A [ ]
OC3	MDI requirements	158.11.3	Meets IEC 61753-1-1, IEC 61753-021-2, and IEC 61753-022-2	INS: M	Yes [ ] N/A [ ]

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159. Physical Medium Dependent (PMD) sublayer and medium, types 25GBASE-BR10, 25GBASE-BR20, and 25GBASE-BR40

159.1 Overview

This clause specifies the 25GBASE-BR10, 25GBASE-BR20, and 25GBASE-BR40 PMDs together with the single-mode fiber medium. Within this clause these PMDs are jointly referred to by the term 25GBASE-BRx. The 25GBASE-BRx PHYs are divided into two variants based on the direction of transmission. Optical line terminal (OLT) PMDs transmit in the downstream direction and receive in the upstream direction. Optical network unit (ONU) PHYs transmit in the upstream direction and receive in the downstream direction. The PMD variant is indicated with a suffix of D for OLT PMDs and U for ONU PMDs. The PMD sublayer provides a point-to-point 25 Gb/s Ethernet link over one single-mode fiber. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 159–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 159–1—Physical Layer clauses associated with the 25GBASE-BRx PMDs

Associated clause	25GBASE-BR10, 25GBASE-BR20, 25GBASE-BR40
106—RS	Required
106—25GMII[a]	Optional
107—PCS for 25GBASE-R	Required
108—RS-FEC[b]	Required
109—PMA for 25GBASE-R	Required
109A—25GAUI C2C	Optional
109B—25GAUI C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a] The 25GMII is an optional interface. However, if the 25GMII is not implemented, a conforming implementation behaves functionally as though the RS and 25GMII were present.
[b] The option to bypass the Clause 108 RS-FEC correction function is not supported.

Figure 159–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 25 Gigabit Ethernet is introduced in Clause 105 and the purpose of each PHY sublayer is summarized in 105.3.

The 25GBASE-BRx PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

Further relevant information may be found in Clause 1 (terminology and conventions, references, definitions, and abbreviations) and Annex A (Bibliography, referenced as [B1], [B2], etc.).

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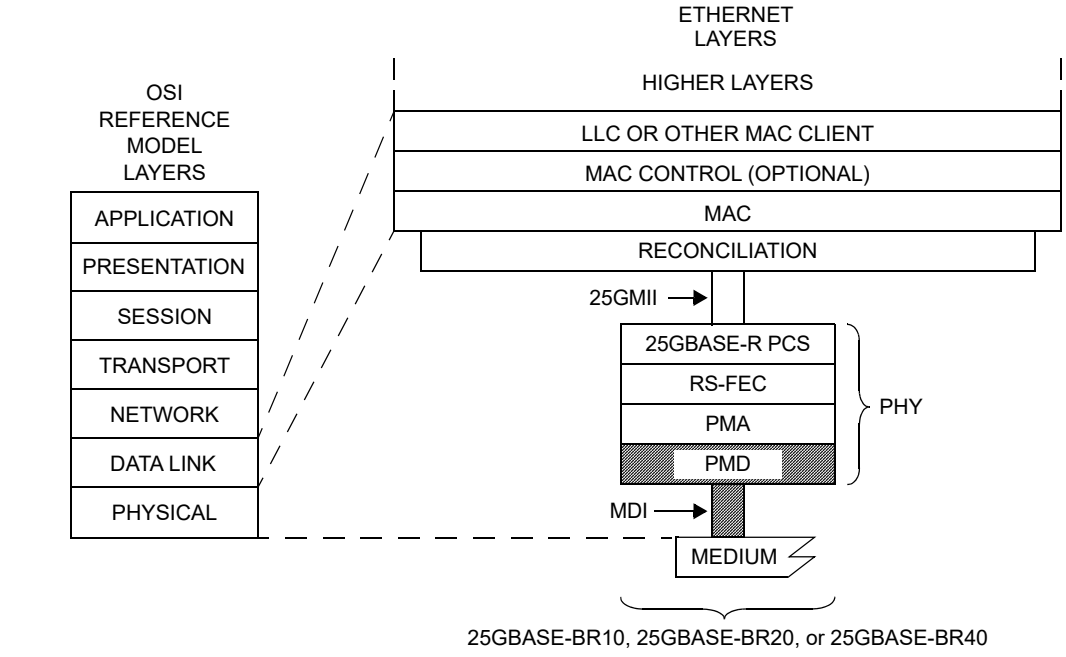

25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 159–1—25GBASE-BRx PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

159.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 5×10^{-5} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap when processed according to Clause 108.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap when processed according to Clause 108.

159.2 Physical Medium Dependent (PMD) service interface

The PMD service interfaces for 25GBASE-BRx are the same as PMD service interface for 25GBASE-SR as described in 112.2 with the BER as specified in 159.1.1.

159.3 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation. The sum of the transmit and receive delays at one end of the link contributed by

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a 25GBASE-BRx PMD including 2 m of fiber in one direction shall be no more than 512 bit times (1 pause_quantum or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quantum can be found in 105.5 and its references.

159.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 159–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 159–3.

Table 159–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable

Table 159–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect

159.5 PMD functional specifications

The 25GBASE-BRx PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

159.5.1 PMD block diagram

The PMD block diagram is shown in Figure 159–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 159.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 88.11.3). Unless specified otherwise, all receiver measurements and tests defined in 159.7 are made at TP3. TP1 and TP4 are optional reference points that may be useful to implementers for testing components (these test points are not typically accessible in an implemented system).

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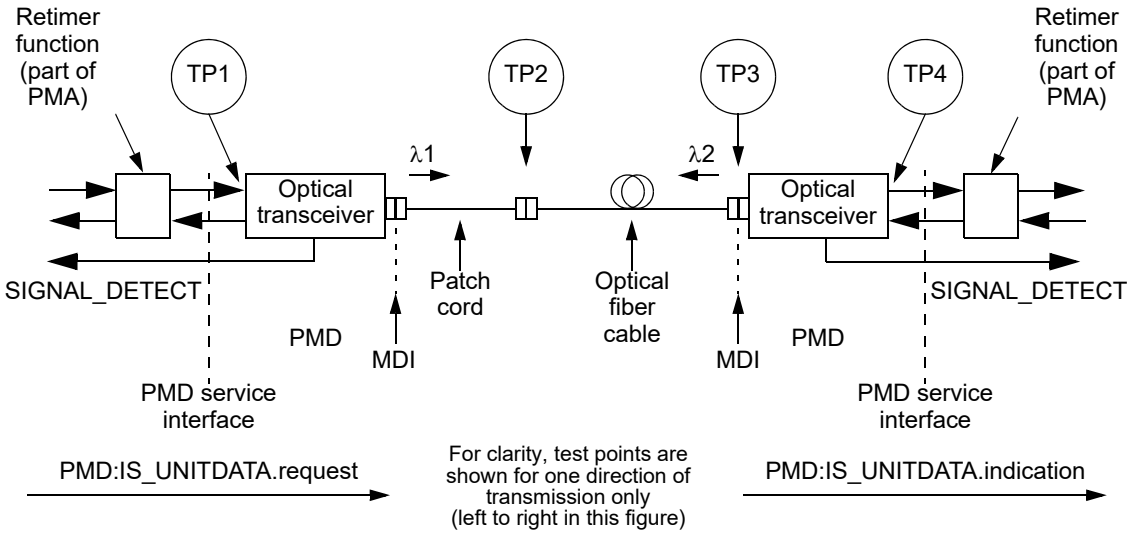

Figure 159–2—Block diagram for 25GBASE-BRx transmit/receive paths

159.5.2 PMD transmit function

The PMD Transmit function shall convert the bit stream requested by the PMD service interface messages PMD:IS_UNITDATA.request into an optical signal. The optical signal shall then be delivered to the MDI, all according to the transmit optical specifications in this clause. The higher optical power level in the signal shall correspond to tx_bit = one.

159.5.3 PMD receive function

The PMD Receive function shall convert the optical signal received from the MDI into a bit stream for delivery to the PMD service interface using the messages PMD:IS_UNITDATA.indication, all according to the receive optical specifications in this clause. The higher optical power level in the signal shall correspond to rx_bit = one.

159.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 105.4.

SIGNAL_DETECT shall be the indicator of the presence of the optical signal. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 159–4. The PMD receiver is not required to verify whether a compliant 25GBASE-BRx signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

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Table 159–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
Average optical power at TP3 ≤ –20 dBm for 25GBASE-BR10 and ≤ –26 dBm for 25GBASE-BR20 and 25GBASE-BR40	FAIL
[(Optical power at TP3 ≥ receiver sensitivity (max) in OMA in Table 159–7) AND (compliant 25GBASE–BRx signal input)]	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the PMD global signal detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal. When the MDIO is implemented, the SIGNAL_DETECT value shall be continuously set in response to the magnitude of the optical signal, according to the requirements of Table 159–4.

159.5.5 PMD reset function

If PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

159.5.6 PMD global transmit disable function

PMDs compliant with this clause shall include the PMD global transmit disable function that allows the optical transmitter to be disabled.

When the PMD_global_transmit_disable variable is set to one, this function shall turn off the optical transmitter so that it meets the requirement of the average launch power of the OFF transmitter in Table 159–6.

If PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter.

159.5.7 PMD fault function (optional)

If the PMD has detected a local fault on the transmit or receive paths, the PMD shall set PMD_fault to one.

159.5.8 PMD transmit fault function (optional)

If the PMD has detected a local fault on the transmitter, the PMD shall set PMD_transmit_fault to one.

PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

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159.5.9 PMD receive fault function

The 25GBASE-BRx-U PMD shall include the PMD_receive_fault function, in the 25GBASE-BRx-D PMD this function is optional. If the PMD has detected a local fault on the receiver, the PMD shall set PMD_receive_fault to one.

PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

159.5.10 ONU silent start

Silent start shall be provided by 25GBASE-BR10-U, 25GBASE-BR20-U, and 25GBASE-BR40-U PHYs. See 157.5.

159.6 PMD to MDI optical specifications for 25GBASE-BRx

The operating ranges for the 25GBASE-BRx PMDs are defined in Table 159–5. 25GBASE-BRx compliant PMDs operate on ITU-T G.652.B (dispersion unshifted), type G.652.D (low water peak, dispersion unshifted), or type G.657.A1 or type G.657.A2 (bend insensitive) single-mode fibers according to the specifications defined in 159.7. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 25GBASE-BR10 PMD operating at 12.5 km meets the operating range requirement of 2 m to 10 km).

Table 159–5—25GBASE-BRx operating ranges

PMD type	Required operating range[a]
25GBASE-BR10	2 m to 10 km
25GBASE-BR20	2 m to 20 km
25GBASE-BR40	2 m to 40 km

[a] The RS-FEC correction function may not be bypassed for any operating distance.

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159.6.1 25GBASE-BRx transmitter optical specifications

The 25GBASE-BRx transmitters shall meet the specifications in Table 159–6 per the definitions in 159.7.

Table 159–6—25GBASE-BRx transmit characteristics

Description	25GBASE-BR10	25GBASE-BR20	25GBASE-BR40	Unit
Signaling rate (range)	25.78125 ± 100 ppm			GBd
25GBASE-BRx-D center wavelength (range)	1320 to 1340	1306 to 1322		nm
25GBASE-BRx-U center wavelength (range)	1260 to 1280	1281 to 1297		nm
Side-mode suppression ratio (SMSR), (min)	30			dB
Average launch power (max)	2	0	6	dBm
Average launch power[a] (min)	–7	–7.5	–3	dBm
Optical Modulation Amplitude (OMA), (max)	2.2	3	6	dBm
Optical Modulation Amplitude (OMA)[b], (min)	–4	–4.5	0	dBm
Launch power in OMA minus TDP (min)	–5	–5.5	–1	dBm
Transmitter and dispersion penalty (TDP), (max)	2.7			dB
Average launch power of OFF transmitter (max)	–20			dBm
Extinction ratio (min)	3	4		dB
$RIN_{20}OMA$ (max)	–130			dB/Hz
Optical return loss tolerance (max)	20			dB
Transmitter reflectance[c] (max)	–26			dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}, hit ratio 5×10^{-5} hits per sample.	{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}			—

[a] Average launch power (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b] The OMA (min) requirement holds even if the TDP < 1 dB.
[c] Transmitter reflectance is defined looking into the transmitter.

159.6.2 25GBASE-BRx receiver optical specifications

The 25GBASE-BRx receivers shall meet the specifications in Table 159–7 per the definitions in 159.7.

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Table 159–7—25GBASE-BRx receive characteristics

Description	25GBASE-BR10	25GBASE-BR20	25GBASE-BR40	Unit
Signaling rate (range)	25.78125 ± 100 ppm			GBd
25GBASE-BRx-D center wavelength (range)	1260 to 1280	1281 to 1297		nm
25GBASE-BRx-U center wavelength (range)	1320 to 1340	1306 to 1322		nm
Damage threshold[a] (min)	3	1	–3	dBm
Average receive power (max)	2	0	–4	dBm
Average receive power[b] (min)	–13.3	–22.5	–21	dBm
Receive power (OMA), (max)	2.2	–4		dBm
Receiver reflectance (max)	–26			dB
Receiver sensitivity (OMA)[c], (max)	–12	–20.5	–19	dBm
Stressed receiver sensitivity (OMA)[d], (max)	–9.5	–16.5		dBm
Conditions of stressed receiver sensitivity test				
Stressed eye closure[e]	2.5			dB
Stressed eye J2 Jitter[e]	0.27			UI
Stressed eye J4 Jitter[e]	0.39			UI
SRS eye mask definition {X1, X2, X3, Y1, Y2, Y3}, hit ratio 5×10^{-5} hits per sample.	{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}			—

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
[b] Average receive power (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] Receiver sensitivity (OMA), (max) is optional.
[d] Measured with conformance test signal at TP3 (see 159.7) for the BER specified in 159.1.1.
[e] Stressed eye closure, stressed eye J2 Jitter, and stressed eye J4 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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159.6.3 25GBASE-BRx illustrative link power budgets

Illustrative power budgets and penalties for 25GBASE-BRx channels are shown in Table 159–8.

Table 159–8—25GBASE-BRx illustrative link power budgets

Parameter	25GBASE-BR10	25GBASE-BR20	25GBASE-BR40	Unit
Power budget (for maximum TDP)	9	17.7	20.7	dB
Operating distance	10	20	40	km
Channel insertion loss	6.3[a]	15[b]	18[a]	dB
Maximum discrete reflectance	See 159.10	–26		dB
Allocation for penalties[c] (for maximum TDP)	2.7			dB

[a] The channel insertion loss is calculated using the maximum distance specified in Table 159–5 and fiber attenuation of 0.4 dB/km plus an allocation for connection and splice loss given in 159.10.2.1.
[b] The channel insertion loss is calculated using the maximum distance specified in Table 159–5 and fiber attenuation of 0.5 dB/km plus an allocation for connection and splice loss given in 159.10.2.1.
[c] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

159.7 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

159.7.1 Test patterns for optical parameters

The test patterns used in this clause shall be the same as those used for 100GBASE-SR4, as described in 95.8.1 and shown in Table 159–9, with the exception that pattern 5, the scrambled idle test pattern defined in 82.2.11, is encoded by Clause 108 RS-FEC for 25GBASE-BRx. The multi-lane testing considerations described in 95.8.1.1 do not apply. Table 159–9 shows the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined.

159.7.2 Wavelength and side-mode suppression ratio (SMSR)

The wavelength and SMSR shall be within the ranges given in Table 159–6 if measured per IEC 61280-1-3. The signal is modulated using the test pattern specified in Table 159–9.

159.7.3 Average optical power

The average optical power shall be within the limits given in Table 159–6 if measured using the methods given in IEC 61280-1-1. The average optical power is measured using the test pattern specified in Table 159–9.

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Table 159–9—Test pattern definitions and related subclauses

Test	Pattern	Related subclause
Wavelength	3, 5 or valid 25GBASE-R signal	159.7.2
Side--mode suppression ratio	3, 5 or valid 25GBASE-R signal	159.7.2
Average optical power	3, 5 or valid 25GBASE-R signal	159.7.3
Optical modulation amplitude (OMA)	Square wave or 4	159.7.4
Transmitter and dispersion penalty (TDP)	3, 5 or valid 25GBASE-R signal	159.7.5
Extinction ratio	3, 5 or valid 25GBASE-R signal	159.7.6
$RIN_{20}OMA$	Square wave or 4	159.7.7
Transmitter optical waveform	3, 5 or valid 25GBASE-R signal	159.7.8
Stressed receiver sensitivity	3, 5 or valid 25GBASE-R signal	159.7.10
Calibration of OMA for receiver tests	Square wave or 4	87.8.11
Vertical eye closure penalty calibration	3, 5 or valid 25GBASE-R signal	87.8.11

159.7.4 Optical Modulation Amplitude (OMA)

OMA shall meet the requirements in Table 159–6 when measured using the method defined in 52.9.5 with a square wave (8 ones, 8 zeros) test pattern, or in 68.6.2 (from the variable MeasuredOMA in 68.6.6.2) with a PRBS9 test pattern. See 159.7.1 for test pattern information.

159.7.5 Transmitter and dispersion penalty (TDP)

Transmitter and dispersion penalty (TDP) shall be as defined in 52.9.10 with the BER as specified in 159.1.1. The measurement procedure for 25GBASE-BRx is detailed in 159.7.5.1 to 159.7.5.4.

159.7.5.1 Reference transmitter requirements

The reference transmitter is a high-quality instrument-grade device, which can be implemented by a CW laser modulated by a high-performance modulator. The basic requirements are as follows:

a) Rise/fall times of less than 12 ps at 20% to 80%.
b) The output optical eye is symmetric and passes the transmitter optical waveform test of 159.7.8.
c) In the center 20% region of the eye, the worst-case vertical eye closure penalty as defined in 87.8.11.2 is less than 0.5 dB.
d) Total Jitter less than 0.2 UI peak-to-peak.
e) RIN of less than –138 dB/Hz.

159.7.5.2 Channel requirements

The channel requirements for testing the transmitter are described in 88.8.5.2, where the requirements for 100GBASE-LR4 apply to 25GBASE-BR10 and the requirements for 100GBASE-ER4 apply to 25GBASE-BR20 and 25GBASE-BR40.

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159.7.5.3 Reference receiver requirements

The reference receiver is required to have the bandwidth given in 159.7.8. The sensitivity of the reference receiver is limited by Gaussian noise. The receiver has minimal threshold offset, deadband, hysteresis, baseline wander, deterministic jitter, or other distortions. Decision sampling has minimal uncertainty and setup/hold times.

The nominal sensitivity of the reference receiver, S, is measured in OMA using the setup of Figure 52–12 without the test fiber and with the transversal filter removed. The sensitivity S has to be corrected for any significant reference transmitter impairments including any vertical eye closure. It is measured while sampling at the eye center or corrected for off-center sampling. It is calibrated at the wavelength of the transmitter under test.

For all transmitter and dispersion penalty measurements, determination of the center of the eye is required. Center of the eye is defined as the time halfway between the left and right sampling points within the eye where the measured BER is greater than or equal to 10^{-3}.

The clock recovery unit (CRU) used in the TDP measurement has a corner frequency of 10 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low-frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.

159.7.5.4 Test procedure

The test procedure is as defined in 52.9.10.4 with the BER as specified in 159.1.1.

159.7.6 Extinction ratio

The extinction ratio shall be within the limits given in Table 159–6 if measured using the methods specified in IEC 61280-2-2. The extinction ratio is measured using the test pattern defined in Table 159–9.

NOTE—Extinction ratio and OMA are defined with different test patterns (see Table 159–9).

159.7.7 Relative Intensity Noise ($RIN_{20}OMA$)

RIN shall be as defined by the measurement methodology of 52.9.6 with the following exceptions:

a) The optical return loss is 20 dB.

b) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 25.8 GHz).

159.7.8 Transmitter optical waveform (transmit eye)

The required optical transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 86–4. The transmitter optical waveform of a port transmitting the test pattern specified in Table 159–9 shall meet specifications according to the methods specified in 86.8.4.6.1 with the exception that the clock recovery unit's high-frequency corner bandwidth is 10 MHz. The filter nominal reference frequency f_r is 19.34 GHz and the filter tolerances are as specified for STM-64 in ITU-T G.691. Compensation may be made for variation of the reference receiver filter response from an ideal fourth-order Bessel-Thomson response and for any excess reference receiver noise.

159.7.9 Receiver sensitivity

Receiver sensitivity, which is defined for an ideal input signal, is optional and compliance is not required. If measured, the test signal should have negligible impairments such as intersymbol interference (ISI), rise/fall times, jitter and RIN. Instead, the normative requirement for receivers is stressed receiver sensitivity.

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159.7.10 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 159–7 if measured using the method defined in 95.8.8 with the following exceptions:

a) The centers of the vertical histograms through the eye diagram are 0.45 UI and 0.55 UI, and the width of each histogram is 0.02 UI (see Figure 95–4).
b) Added sinusoidal jitter is as specified in Table 159–10.
c) The stressed eye J2 Jitter, stressed eye J4 Jitter, stressed eye closure, and SRS eye mask are as given in Table 159–7.
d) The test pattern is as given in Table 159–9.
e) The reference receiver used to verify the conformance test signal is required to have the bandwidth given in 159.7.8.
f) The SEC created by the selection of the appropriate bandwidth for the combination of the low-pass filter and the E/O converter with the sinusoidal jitter, sinusoidal interferer 1, sinusoidal interferer 2, and the Gaussian noise generator turned off is at least 1.5 dB.
g) The conditions for receiver aggressor lanes do not apply.
h) The reflectance of the optical link should be at its maximum level.

Table 159–10—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter, peak-to-peak (UI)
$f < 100$ kHz	Not specified
100 kHz $< f \leq 10$ MHz	5×10^5 Hz/f
10 MHz $< f <$ 10 LB[a]	0.05

[a] LB = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

159.8 Safety, installation, environment, and labeling

159.8.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

159.8.2 Laser safety

25GBASE-BRx optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[257]

[257] A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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159.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

159.8.4 Environment

Normative specifications in this clause shall be met by a system integrating a 25GBASE-BRx PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause are met.

159.8.5 Electromagnetic emission

A system integrating a 25GBASE-BRx PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

159.8.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

159.8.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 25GBASE-BR10-D). Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 159.8.2.

159.9 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 159–3.

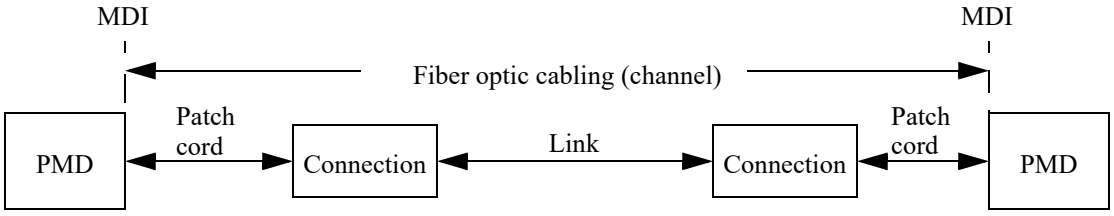

Figure 159–3—Fiber optic cabling model

The channel insertion loss is given in Table 159–8. A channel may contain additional connectors or other optical elements as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. Insertion loss measurements of

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installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards. The maximum channel insertion loss for 25GBASE-BR40 is specified by Table 159–11.

Table 159–11—Maximum channel insertion loss versus number of discrete reflectances for 25GBASE-BR40

Maximum channel insertion loss (dB)		Number of discrete reflectances > –55 dB and ≤ –35 dB										
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
Number of discrete reflectances > –35 dB and ≤ –26 dB	**0**	18	18	18	17.9	17.9	17.9	17.8	17.8	17.8	17.7	17.7
	1	17.9	17.9	17.9	17.8	17.8	17.7	17.7	17.6	17.6	17.5	—[a]
	2	17.8	17.8	17.7	17.7	17.6	17.6	17.5	17.4	17.4	—[a]	—[a]
	3	17.7	17.6	17.6	17.4	17.4	17.3	—[a]	—[a]	—[a]	—[a]	—[a]
	4	17.5	17.4	17.3	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]
	> 4	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]

[a]The indicated combination of reflectances is not supported.

159.10 Characteristics of the fiber optic cabling (channel)

The 25GBASE-BRx fiber optic cabling shall meet the specifications defined in Table 159–12. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

Table 159–12—Fiber optic cabling (channel) characteristics

Description	25GBASE-BR10	25GBASE-BR20	25GBASE-BR40	Unit
Operating distance (max)	10	20	40	km
Channel insertion loss[a, b](max)	6.2	15	18	dB
Channel insertion loss (min)	0	0	10	dB
Positive dispersion[b] (max)	35	38.5	79	ps/nm
Negative dispersion[b] (min)	–64	–83	–166	ps/nm
DGD_max[c]	8	10.3	10.3	ps
Optical return loss (min)	21	21	21	dB

[a] These channel insertion loss values include cable, connectors, and splices.
[b] Over the wavelength range 1260 nm to 1340 nm for 25GBASE-BR10 and 1281 nm to 1322 nm for 25GBASE-BR20 and 25GBASE-BR40.
[c] Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

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159.10.1 Optical fiber cable

The optical fiber cable requirements are satisfied by cables containing ITU-T G.652.B (dispersion unshifted), type G.652.D (low water peak, dispersion unshifted), or type G.657.A1 or type G.657.A2 (bend insensitive) fibers or the requirements in Table 159–12 where they differ.

159.10.2 Optical fiber connection

An optical fiber connection, as shown in Figure 159–3, consists of a mated pair of optical connectors.

159.10.2.1 Connection insertion loss

Connections with different loss characteristics may be used provided the requirements of Table 159–12 are met. The maximum link distance for 25GBASE-BR10 and 25GBASE-BR40 is based on an allocation of 2 dB total connection and splice loss. The maximum link distance for 25GBASE-BR20 is based on an allocation of 5 dB total connection and splice loss.

159.10.2.2 Maximum discrete reflectance

For 25GBASE-BR10, the maximum value for each discrete reflectance shall be less than or equal to the value shown in Table 159–13 corresponding to the number of discrete reflectances above –55 dB within the channel.

For 25GBASE-BR40, the maximum value of channel insertion loss is dependent on the number and maximum value of the discrete reflectances within the channel as given in Table 159–11. Discrete reflectances below –55 dB may be ignored when determining the supported channel insertion loss.

Table 159–13—Maximum value of each discrete reflectance for 25GBASE-BR10

Number of discrete reflectances above –55 dB[a]	Maximum value for each discrete reflectance for 25GBASE-BR10
1 to 4	–26 dB
6	–30 dB
8	–32 dB
10	–34 dB

[a] For numbers of discrete reflectances in between two numbers shown in the table, the lower of the two corresponding maximum discrete reflectance values applies.

159.10.3 Medium Dependent Interface (MDI) requirements

The 25GBASE-BRx PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the “fiber optic cabling” (as shown in Figure 159–3). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

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When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 159.5.1, not at the MDI.

159.11 Requirements for interoperation between 25GBASE-BRx PMDs

The 25GBASE-BR20 and 25GBASE-BR40 PMDs can interoperate with each other (over an engineered link) provided that the fiber optic cabling (channel) characteristics are met, with the exception of the maximum and minimum channel insertion loss values, which are given in Table 159–14 for the two link directions separately. Attenuators may be used to achieve the required losses.

Table 159–14—Channel insertion loss requirements for interoperation between 25GBASE-BR20 and 25GBASE-BR40

Direction	Min loss	Max loss	Unit
25GBASE-BR20 transmitter to 25GBASE-BR40 receiver	4	15	dB
25GBASE-BR40 transmitter to 25GBASE-BR20 receiver	6	18	dB

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159.12 Protocol implementation conformance statement (PICS) proforma for Clause 159, Physical Medium Dependent (PMD) sublayer and medium, types 25GBASE-BR10, 25GBASE-BR20, and 25GBASE-BR40[258]

159.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 159, Physical Medium Dependent (PMD) sublayer and medium, types 25GBASE-BR10, 25GBASE-BR20, and 25GBASE-BR40, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

159.12.2 Identification

159.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

159.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 159, Physical Medium Dependent (PMD) sublayer and medium, types 25GBASE-BR10, 25GBASE-BR20, and 25GBASE-BR40
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[258] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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159.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*BR10	25GBASE-BR10 PMD	159.6	Device supports requirements for 25GBASE-BR10 PHY	O.1	Yes [ ] No [ ]
*BR20	25GBASE-BR20 PMD	159.6	Device supports requirements for 25GBASE-BR20 PHY	O.1	Yes [ ] No [ ]
*BR40	25GBASE-BR40 PMD	159.6	Device supports requirements for 25GBASE-BR40 PHY	O.1	Yes [ ] No [ ]
*INS	Installation / cable	159.9	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	159.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	159.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	159.3	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO capability	159.4	Registers and interface supported	O	Yes [ ] No [ ]

159.12.4 PICS proforma tables for PMD sublayer and medium, types 25GBASE-BR10, 25GBASE-BR20, and 25GBASE-BR40

159.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 25GBASE-R PCS, RS-FEC, and PMA	159.1		M	Yes [ ]
F2	Integration with management functions	159.1		O	Yes [ ] No [ ]
F3	Bit error ratio	159.1.1	Meets the BER specified in 159.1.1	M	Yes [ ]
F4	Transmit function	159.5.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
F5	Mapping between optical signal and logical signal for transmitter	159.5.2	Higher optical power is a one	M	Yes [ ]
F6	Receive function	159.5.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F7	Conversion of optical signal to electrical signal	159.5.3	For delivery to the PMD service interface	M	Yes [ ]
F8	Mapping between optical signal and logical signal for receiver	159.5.3	Higher optical power is a one	M	Yes [ ]
F9	Global Signal Detect function	159.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F10	Global Signal Detect behavior	159.5.4	SIGNAL_DETECT is a global indicator of the presence of an optical signal	M	Yes [ ]
F11	PMD reset function	159.5.5	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]
F12	ONU silent start	159.5.10	Meets the specifications defined in 159.5.10	M	Yes [ ]

159.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	159.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	159.5.6	Disables the optical transmitter with the PMD_global_transmit_disable variable	M	Yes [ ]
M3	PMD_fault function	159.5.7	Sets PMD_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD_transmit_fault function	159.5.8	Sets PMD_transmit_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_receive_fault function	159.5.9	Sets PMD_receive_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]

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159.12.4.3 PMD to MDI optical specifications for 25GBASE-BR10

Item	Feature	Subclause	Value/Comment	Status	Support
BR101	Transmitter meets specifications in Table 159–6	159.6.1	Per the definitions in 159.7	BR10:M	Yes [ ] N/A [ ]
BR102	Receiver meets specifications in Table 159–7	159.6.2	Per the definitions in 159.7	BR10:M	Yes [ ] N/A [ ]

159.12.4.4 PMD to MDI optical specifications for 25GBASE-BR20

Item	Feature	Subclause	Value/Comment	Status	Support
BR201	Transmitter meets specifications in Table 159–6	159.6.1	Per the definitions in 159.7	BR20:M	Yes [ ] N/A [ ]
BR202	Receiver meets specifications in Table 159–7	159.6.2	Per the definitions in 159.7	BR20:M	Yes [ ] N/A [ ]

159.12.4.5 PMD to MDI optical specifications for 25GBASE-BR40

Item	Feature	Subclause	Value/Comment	Status	Support
BR401	Transmitter meets specifications in Table 159–6	159.6.1	Per the definitions in 159.7	BR40:M	Yes [ ] N/A [ ]
BR402	Receiver meets specifications in Table 159–7	159.6.2	Per the definitions in 159.7	BR40:M	Yes [ ] N/A [ ]

159.12.4.6 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
M1	General measurement	159.7	Meets the specifications defined in 159.7	M	Yes [ ]

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159.12.4.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	159.8.1	Conforms to the general safety requirements in J.2	M	Yes [ ]
ES2	Laser safety —IEC Hazard Level 1	159.8.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	159.8.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

159.12.4.8 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	159.10	Meets the specifications defined in Table 159–12	INS: M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	159.10	Less than or equal to the value shown in Table 159–13	INS: M	Yes [ ] N/A [ ]

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160. Physical Medium Dependent (PMD) sublayer and medium, types 50GBASE-BR10, 50GBASE-BR20, and 50GBASE-BR40

160.1 Overview

This clause specifies the 50GBASE-BR10, 50GBASE-BR20, and 50GBASE-BR40 PMDs together with one single-mode fiber medium. Within this clause these PMDs are jointly referred to by the term 50GBASE-BRx. The 50GBASE-BRx PHYs are divided into two variants based on the direction of transmission. Optical line terminal (OLT) PMDs transmit in the downstream direction and receive in the upstream direction. Optical network unit (ONU) PMDs transmit in the upstream direction and receive in the downstream direction. The PMD variant is indicated with a suffix of D for OLT PMDs and U for ONU PMDs. The optical signals generated by these three PMD types are modulated using a 4-level pulse amplitude modulation (PAM4) format. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 160–1, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Table 160–1—Physical Layer clauses associated with the 50GBASE-BRx PMDs

Associated clause	50GBASE-BR10, 50GBASE-BR20, 50GBASE-BR40
132—RS	Required
132—50GMII[a]	Optional
133—PCS for 50GBASE-R	Required
134—RS-FEC for 50GBASE-R	Required
135—PMA for 50GBASE-R	Required
135B—LAUI-2 C2C	Optional
135C—LAUI-2 C2M	Optional
135D—50GAUI-2 C2C	Optional
135E—50GAUI-2 C2M	Optional
135F—50GAUI-1 C2C	Optional
135G—50GAUI-1 C2M	Optional
78—Energy-Efficient Ethernet	Optional

[a] 50GMII is an optional interface. However, if the appropriate interface is not implemented, a conforming implementation behaves functionally as though the RS and 50GMII were present.

Figure 160–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 50 Gigabit Ethernet is introduced in Clause 131 and the purpose of each PHY sublayer is summarized in 131.2.

50GBASE-BRx PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

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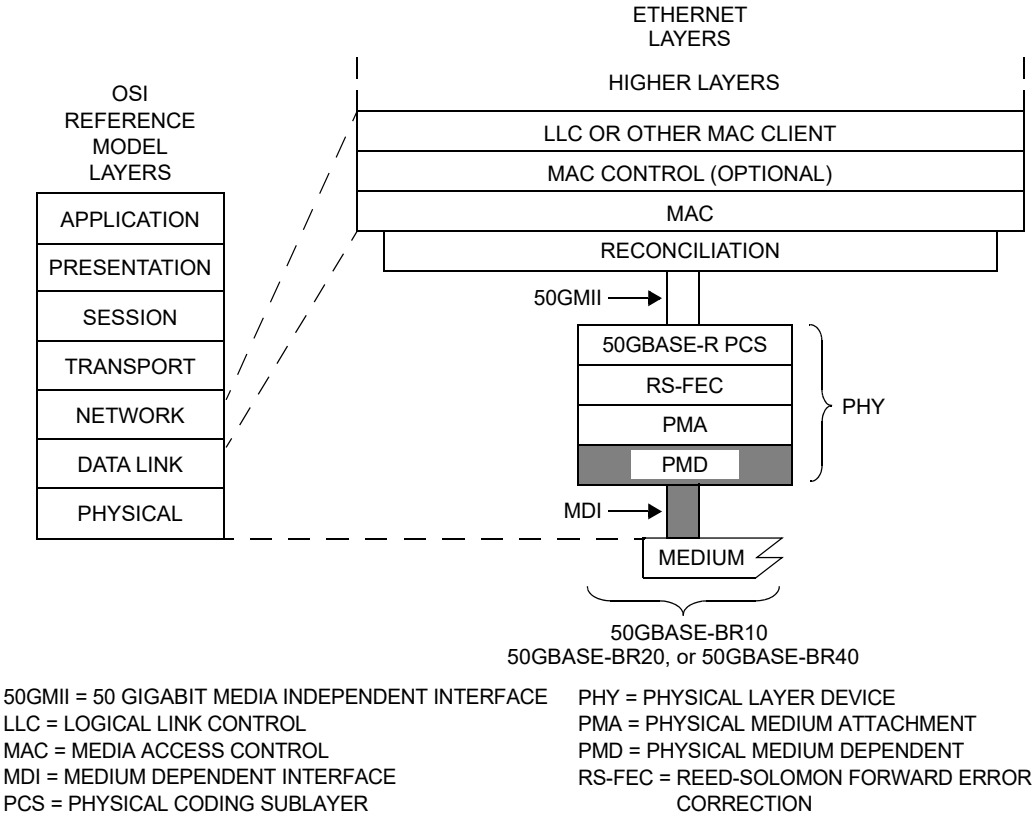

Figure 160–1—50GBASE-BRx PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

160.1.1 Bit error ratio

The bit error ratio (BER) when processed by the PMA (Clause 135) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap when additionally processed by the FEC (Clause 134) and PCS (Clause 133). For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-10} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 9.2×10^{-13} for 64-octet frames with minimum interpacket gap.

160.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 50GBASE-BRx PMDs. The service interface for these PMDs is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

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The 50GBASE-BRx PMD service interface is an instance of the inter-sublayer service interface defined in 131.3, with a single symbol stream (n = 1).

The service interface primitives are summarized as follows:

PMD:IS_UNITDATA_0.request
PMD:IS_UNITDATA_0.indication
PMD:IS_SIGNAL.indication

In the transmit direction, the PMA continuously sends one stream of PAM4 symbols to the PMD using the PMD:IS_UNITDATA_0.request primitive, at a nominal signaling rate of 26.5625 GBd. The PMD converts these streams of symbols into appropriate signals on the MDI.

In the receive direction, the PMD continuously sends one stream of PAM4 symbols to the PMA, corresponding to the signals received from the MDI, using the PMD:IS_UNITDATA_0.indication primitive, at a nominal signaling rate of 26.5625 GBd.

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable SIGNAL_DETECT parameter as defined in 160.5.4. The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, the rx_symbol parameters are undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that the rx_symbol parameters are known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the BER defined in 160.1.1.

160.3 Delay and Skew

160.3.1 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation. The sum of the transmit and receive delays at one end of the link contributed by the 50GBASE-BRx PMDs including 2 m of fiber in one direction shall be no more than 1024 bit times (2 pause_quanta or 20.48 ns). A description of overall system delay constraints and the definitions for bit times and pause_quantum can be found in 131.4 and its references.

160.3.2 Skew constraints

The Skew (relative delay) between the FEC lanes is kept within limits so that the information on the lanes can be reassembled by the FEC. The Skew Variation is also limited to ensure that a given FEC lane always traverses the same physical lane. Skew and Skew Variation are defined in 131.5 and specified at the points SP0 to SP7 shown in Figure 131–3.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns as defined by 135.5.3.5. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns. Since the signal at the MDI represents a serial bit stream, there is no Skew Variation at this point.

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If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns. Since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation, see 131.5. The measurements of Skew and Skew Variation are defined in 89.7.2 with the exception that the measurement clock and data recovery unit high-frequency corner bandwidth is 4 MHz.

160.4 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PMD. If the MDIO interface is implemented, the mapping of MDIO control variables to PMD control variables shall be as shown in Table 160–2 and the mapping of MDIO status variables to PMD status variables shall be as shown in Table 160–3.

Table 160–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable

Table 160–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect

160.5 PMD functional specifications

The 50GBASE-BRx PMDs perform the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

160.5.1 PMD block diagram

The PMD block diagram is shown in Figure 160–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 160.7 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 160.10.3). Unless specified otherwise, all receiver measurements and tests defined in 160.7 are made at TP3. TP1 and TP4 are optional reference points that

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may be useful to implementers for testing components (these test points are not typically be accessible in an implemented system).

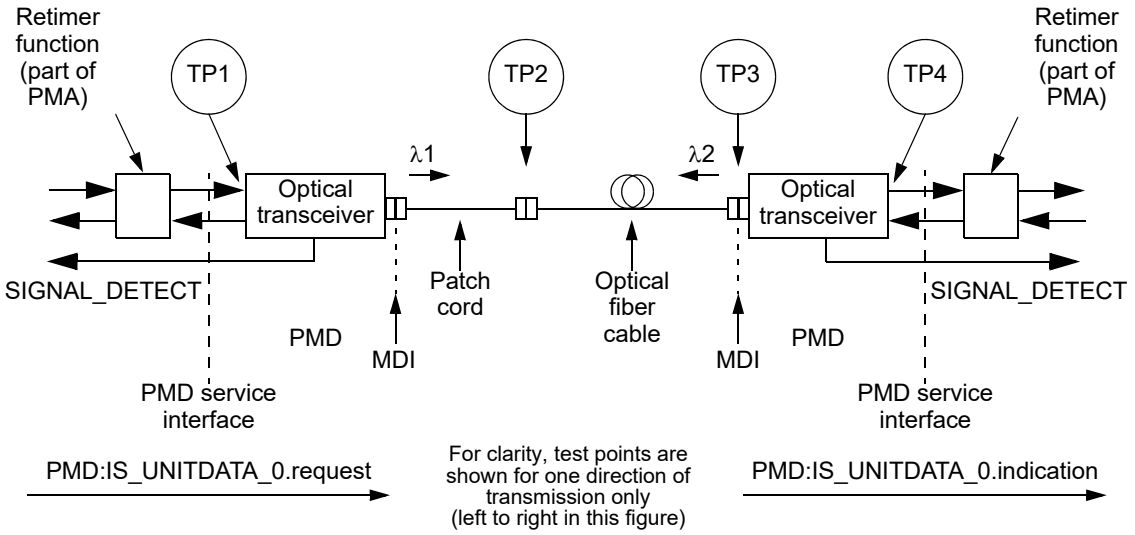

Figure 160–2—Block diagram for 50GBASE-BRx transmit/receive paths

160.5.2 PMD transmit function

The PMD Transmit function shall convert the symbol stream requested by the PMD service interface messages PMD:IS_UNITDATA_0.request into an optical signal. The optical signal shall then be delivered to the MDI, according to the transmit optical specifications in this clause. The four optical power levels in the signal in order from lowest to highest shall correspond to tx_symbol values zero, one, two, and three, respectively.

160.5.3 PMD receive function

The PMD receive function shall convert the optical signal received from the MDI into a symbol stream for delivery to the PMD service interface using the message PMD:IS_UNITDATA_0.indication, all according to the receive optical specifications in this clause. The four optical power levels in each signal in order from lowest to highest shall correspond to rx_symbol values zero, one, two, and three, respectively.

160.5.4 PMD global signal detect function

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 131.3.

SIGNAL_DETECT shall be a global indicator of the presence of the optical signal. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 160–4. The PMD receiver is not required to verify whether a compliant 50GBASE-BRx signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

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Table 160–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
Average optical power at TP3 ≤ –20 dBm	FAIL
[(Optical power at TP3 ≥ average receive power in Table 160–7) AND (compliant 50GBASE-BRx signal input)]	OK
All other conditions	Unspecified

As a consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations need to provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD including the effects of crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

160.5.5 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

160.5.6 PMD global transmit disable function

PMDs compliant with this clause shall include the PMD global transmit disable function that allows the optical transmitter to be disabled.

When the PMD_global_transmit_disable variable is set to one, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of the OFF transmitter in Table 160–6.

If a PMD_fault is detected, then the PMD may set the PMD_global_transmit_disable variable to one, turning off the optical transmitter.

160.5.7 PMD fault function (optional)

If the PMD has detected a local fault on the transmit or receive paths, the PMD shall set PMD_fault to one.

If the MDIO interface is implemented, PMD_fault shall be mapped to the fault bit as specified in 45.2.1.2.3.

160.5.8 PMD transmit fault function (optional)

If the PMD has detected a local fault on the transmitter, the PMD shall set the PMD_transmit_fault variable to one.

If the MDIO interface is implemented, PMD_transmit_fault shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

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160.5.9 PMD receive fault function

The 50GBASE-BRx-U PMD shall include the PMD_receive_fault function, in the 50GBASE-BRx-D PMD this function is optional. If the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to one.

If the MDIO interface is implemented, PMD_receive_fault shall be mapped to the receive fault bit as specified in 45.2.1.7.5.

160.5.10 ONU silent start

Silent start shall be provided by 50GBASE-BR10-U, 50GBASE-BR20-U, and 50GBASE-BR40-U PHYs. See 157.5.

160.6 PMD to MDI optical specifications for 50GBASE-BRx

The operating ranges for the 50GBASE-BRx PMDs are defined in Table 160–5. A 50GBASE-BRx compliant PMD operates on type B1.1, B1.3, or B6_a single-mode fibers according to the specifications defined in Table 160–12. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 50GBASE-BR10 PMD operating at 12.5 km meets the operating range requirement of 2 m to 10 km). The 50GBASE-BR40 PMD interoperates with the 50GBASE-BR10 or 50GBASE-BR20 PMD provided that the channel requirements for the 50GBASE-BR10 or 50GBASE-BR20 PMD are met.

Table 160–5—50GBASE-BRx operating ranges

PMD type	Required operating range[a]
50GBASE-BR10	2 m to 10 km
50GBASE-BR20	2 m to 20 km
50GBASE-BR40	2 m to 40 km

[a] The RS-FEC correction function may not be bypassed for any operating distance.

160.6.1 50GBASE-BRx transmitter optical specifications

The 50GBASE-BRx transmitters shall meet the specifications defined in Table 160–6 per the definitions in 160.7.

Table 160–6—50GBASE-BRx transmit characteristics

Description	50GBASE-BR10	50GBASE-BR20	50GBASE-BR40	Unit
Signaling rate (range)	26.5625 ± 100 ppm			GBd
Modulation format	PAM4			—
50GBASE-BRx-D center wavelengths (range)	1320 to 1340	1306 to 1322		nm
50GBASE-BRx-U center wavelengths (range)	1260 to 1280	1281 to 1297		nm

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Table 160–6—50GBASE-BRx transmit characteristics *(continued)*

Description	50GBASE-BR10	50GBASE-BR20	50GBASE-BR40	Unit
Side-mode suppression ratio (SMSR), (min)	30			dB
Average launch power (max)	4.2	3.6	6.6	dBm
Average launch power[a] (min)	–4.5	–2.6	0.4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (max)	4	4.4	7.4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}) (min)[b]: for TDECQ < 1.4 dB for 1.4 dB ≤ TDECQ ≤ 3.2 dB	 –1.5 –2.9 + TDECQ	 0.4 –1 + TDECQ	 3.4 2 + TDECQ	 dBm dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ) (max)	3.2			dB
TDECQ – $10\log_{10}(C_{eq})$[c] (max)	3.2			dB
TECQ (max)	3.2			dB
| TDECQ – TECQ | (max)	2.5			dB
Average launch power of OFF transmitter (max)	–16	–20	–15	dBm
Extinction ratio (min)	3.5	6		dB
Transmitter transition time (max)	34			ps
RIN_xOMA (max)[d]	–132			dB/Hz
Optical return loss tolerance (max)	15.6	15		dB
Transmitter reflectance[e] (max)	–26			dB

[a] Average launch power (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b] The OMA_{outer} (min) requirement holds even if the TDECQ < 1.4 dB. Even though the representation of the OMA_{outer} requirement is different from that in Clause 139, they are consistent.
[c] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[d] In RIN_xOMA, "x" is the optical return loss tolerance (max) for the PHY under test.
[e] Transmitter reflectance is defined looking into the transmitter.

160.6.2 50GBASE-BRx receive optical specifications

The 50GBASE-BRx receiver shall meet the specifications defined in Table 160–7 per the definitions in 160.7.

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Table 160–7—50GBASE-BRx receive characteristics

Description	50GBASE-BR10	50GBASE-BR20	50GBASE-BR40	Unit
Signaling rate (range)	26.5625 ± 100 ppm			GBd
Modulation format	PAM4			—
50GBASE-BRx-D center wavelengths (range)	1260 to 1280	1281 to 1297		nm
50GBASE-BRx-U center wavelengths (range)	1320 to 1340	1306 to 1322		nm
Damage threshold[a]	5.2	4.6	–2.4	dBm
Average receive power (max)	4.2	3.6	–3.4	dBm
Average receive power[b] (min)	–10.8	–17.6		dBm
Receive power (OMA_{outer}) (max)	4	4.4	–2.6	dBm
Receiver reflectance (max)	–26			dB
Receiver sensitivity (OMA_{outer})[c] (max) for TECQ < 1.4 dB for 1.4 dB ≤ TECQ ≤ 3.2 dB	 –8.4 –9.8 + TECQ	 –15.1 –16.5 + TECQ		 dBm dBm
Stressed receiver sensitivity (OMA_{outer})[d] (max)	–6.6	–13.3		dBm
Conditions of stressed receiver sensitivity test:[e]				
Stressed eye closure for PAM4 (SECQ)	3.2			dB

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
[b] Average receive power (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] Receiver sensitivity (OMA_{outer}) (max) is optional and is defined for a transmitter with a value of SECQ up to 3 dB for 50GBASE-BR10 and 3.2 dB for 50GBASE-BR20, and 50GBASE-BR40.
[d] Measured with conformance test signal at TP3 (see 160.7) for the BER specified in 160.1.1.
[e] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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160.6.3 50GBASE-BRx illustrative link power budgets

Illustrative power budgets and penalties for 50GBASE-BRx channels are shown in Table 160–8.

Table 160–8—50GBASE-BRx illustrative link power budgets

Parameter	50GBASE-BR10	50GBASE-BR20	50GBASE-BR40	Unit
Power budget (for maximum TDECQ)	10.1	18.7	21.7	dB
Operating distance	10	20	40	km
Channel insertion loss	6.3[a]	15[b]	18[a]	dB
Maximum discrete reflectance	–26	–26	–26	dB
Allocation for penalties[c] (for maximum TDECQ)	3.8	3.7	3.7	dB

[a] The channel insertion loss is calculated using the maximum distance specified in Table 160–5 for 50GBASE-BR10 and 50GBASE-BR40 and fiber attenuation of 0.4 dB/km plus an allocation for connection and splice loss given in 160.10.2.1.
[b] The channel insertion loss is calculated using the maximum distance specified in Table 160–5 for 50GBASE-BR20 and fiber attenuation of 0.5 dB/km plus an allocation for connection and splice loss given in 160.10.2.1.
[c] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

160.7 Definition of optical parameters and measurement methods

All transmitter optical measurements shall be made through a short patch cable, between 2 m and 5 m in length, unless otherwise specified.

160.7.1 Test patterns for optical parameters

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 160–10 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Any of the test patterns given for a particular test in Table 160–10 may be used to perform that test. The test patterns used in this clause are shown in Table 160–9.

Table 160–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle encoded by RS-FEC	82.2.11[a], 134
6	SSPRQ	120.5.11.2.3

[a]As modified by Clause 133.

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Table 160–10—Test pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6 or valid 50GBASE-R signal	160.7.2
Side-mode suppression ratio	3, 5, 6 or valid 50GBASE-R signal	160.7.2
Average optical power	3, 5, 6 or valid 50GBASE-R signal	160.7.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	160.7.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	160.7.5
Transmitter eye closure for PAM4 (TECQ)	6	160.7.6
Extinction ratio	4 or 6	160.7.7
Transmitter transition time	Square wave or 6	160.7.8
$RIN_x OMA$	Square wave	160.7.9
Receiver sensitivity	3 or 5	160.7.10
Stressed receiver conformance test signal calibration	6	160.7.11.2
Stressed receiver sensitivity	3 or 5	160.7.11

160.7.2 Wavelength and side-mode suppression ratio (SMSR)

The wavelength and SMSR shall be within the ranges given in Table 160–6 for 50GBASE-BRx, if measured per IEC 61280-1-3. The transmitter is modulated using the test pattern defined in Table 160–10.

160.7.3 Average optical power

The average optical power shall be within the limits given in Table 160–6 for 50GBASE-BRx if measured using the methods given in IEC 61280-1-1.

160.7.4 Outer Optical Modulation Amplitude (OMA_{outer})

The OMA_{outer} shall be within the limits given in Table 160–6 for 50GBASE-BRx. The OMA_{outer} is measured using a test pattern specified for OMA_{outer} in Table 160–10 as the difference between the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 160–3.

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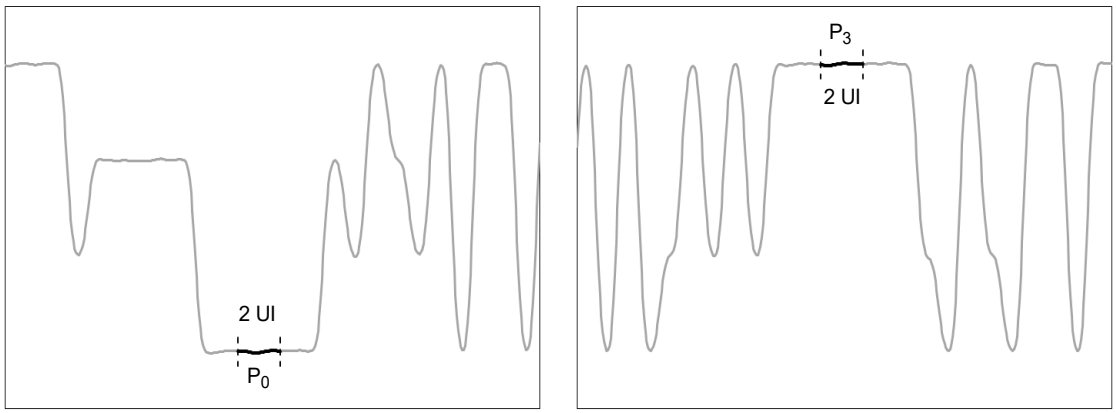

Figure 160–3—Example power levels P_0 and P_3 from PRBS13Q test pattern

160.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

The TDECQ shall be within the limits given in Table 160–6 for 50GBASE-BRx if measured using the methods specified in 160.7.5.1, 160.7.5.2, and 160.7.5.3.

TDECQ is a measure of each optical transmitter's vertical eye closure when transmitted through a worst case optical channel (specified in 160.7.5.2), as measured through an optical to electrical converter (O/E) with a bandwidth equivalent to a reference receiver, and equalized with the reference equalizer (as described in 160.7.5.4). The reference receiver and equalizer may be implemented in software or may be part of the oscilloscope.

Table 160–10 specifies the test patterns to be used for measurement of TDECQ.

160.7.5.1 TDECQ conformance test setup

A block diagram for the TDECQ conformance test is shown in Figure 160–4. Other equivalent measurement implementations may be used with suitable calibration.

The optical splitter and variable reflector are adjusted so that each transmitter is tested with the optical return loss specified in Table 160–11. The state of polarization of the back reflection is adjusted to create the greatest RIN. The signal is tested with the optical channel described in 160.7.5.2. The combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5×26.5625 GHz and at frequencies above 1.5×26.5625 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The test pattern (specified in Table 160–10) is transmitted repetitively and the oscilloscope is set up to capture the complete pattern for TDECQ analysis as described in 160.7.5.3. The clock recovery unit (CRU) has a corner frequency of 4 MHz and a slope of 20 dB/decade. The CRU can be implemented in hardware or software depending on oscilloscope technology.

160.7.5.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 160–11.

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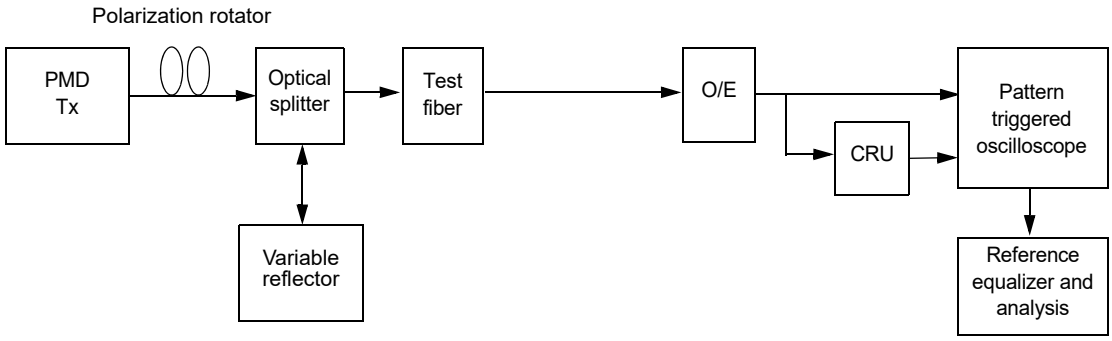

Figure 160–4—TDECQ conformance test block diagram

Table 160–11—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]	Max mean DGD
	Minimum	Maximum			
50GBASE-BR10	$0.23 \times \lambda \times [1 - (1324 / \lambda)^4]$	$0.23 \times \lambda \times [1 - (1300 / \lambda)^4]$	Minimum	15.6 dB	0.8 ps
50GBASE-BR20	$0.46 \times \lambda \times [1 - (1324 / \lambda)^4]$	$0.46 \times \lambda \times [1 - (1300 / \lambda)^4]$	Minimum	15 dB	0.8 ps
50GBASE-BR40	$0.92 \times \lambda \times [1 - (1324 / \lambda)^4]$	$0.92 \times \lambda \times [1 - (1300 / \lambda)^4]$	Minimum	15 dB	0.8 ps

[a] The dispersion is measured for the wavelength of the device under test (λ in nm). The coefficient assumes 10 km for 50GBASE-BR10, 20 km for 50GBASE-BR20, and 40 km for 50GBASE-BR40. The link may be as short as 2 m, and the minimum or maximum dispersion may be 0.
[b] There is no intent to stress the sensitivity of the O/E converter associated with the oscilloscope.
[c] The optical return loss is applied at TP2.

A 50GBASE-BRx transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 160–11 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss specified in Table 160–11. The state of polarization of the back reflection is adjusted to create the greatest RIN.

The mean DGD of the channel is to be less than the value specified in Table 160–11.

160.7.5.3 TDECQ measurement method

TDECQ for 50GBASE-BRx is measured as described in 121.8.5.3 with the following exception:

— The reference equalizer is as specified in 160.7.5.4.

160.7.5.4 TDECQ reference equalizer

The reference equalizer for 50GBASE-BRx is a 5-tap, T-spaced, feed-forward equalizer (FFE), where T is the symbol period. A functional model of the reference equalizer is shown in Figure 160–5. The sum of the

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equalizer tap coefficients is equal to 1. Tap 1, tap 2, or tap 3, has the largest magnitude tap coefficient, which is constrained to be at least 0.8.

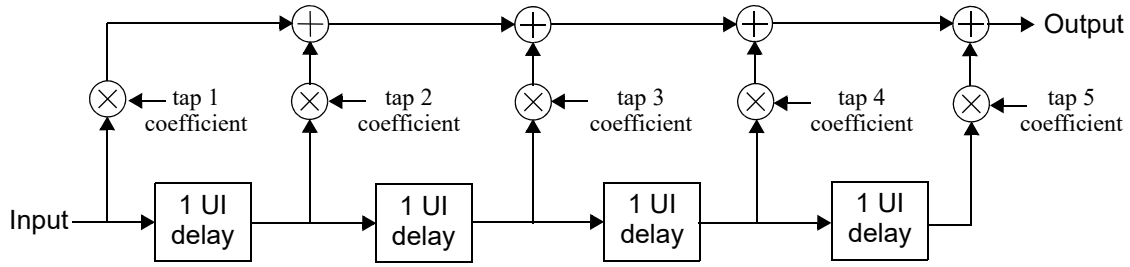

Figure 160–5—TDECQ reference equalizer functional model

NOTE—This reference equalizer is part of the TDECQ test and does not imply any particular receiver equalizer implementation.

160.7.6 Transmitter eye closure for PAM4 (TECQ)

The transmitter eye closure for PAM4 (TECQ) is a measure of the optical transmitter's eye closure at TP2. The TECQ of each lane shall be within the limits given in Table 160–6 for 50GBASE-BRx if measured using a test pattern specified for TECQ in Table 160–10. The TECQ of each lane is measured using the methods specified for TDECQ in 160.7.5, except that the test fiber is not used.

160.7.7 Extinction ratio

The extinction ratio shall be within the limits given in Table 160–6 for 50GBASE-BRx if measured using a test pattern specified for extinction ratio in Table 160–10. The extinction ratio of a PAM4 optical signal is defined as the ratio of the average optical launch power level P_3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P_0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 160–3.

160.7.8 Transmitter transition time

The transmitter transition time of each lane shall be within the limits given in Table 160–6 if measured using a test pattern specified for transmitter transition time in Table 160–10.

Transmitter transition time is defined as the slower of the time interval of the transition from 20% of OMA_{outer} to 80% of OMA_{outer}, or from 80% of OMA_{outer} to 20% of OMA_{outer}, for the rising and falling edges respectively, as measured through an O/E converter and oscilloscope with a combined 3 dB bandwidth of approximately 13.28125 GHz with a fourth-order Bessel-Thomson response to at least 1.5 × 26.5625 GHz and at frequencies above 1.5 × 26.5625 GHz the response should not exceed –24 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.

The 0% level and the 100% level are P_0 and P_3 as defined by the OMA_{outer} measurement procedure (see 160.7.4), with the exception that the square wave test pattern can be used. When the SSPRQ pattern is used, the rising edge used for the measurement is that within the 00000333333 symbol sequence and the falling edge is that within the 33333000000 symbol sequence.

160.7.9 Relative intensity noise (RIN_xOMA)

RIN_xOMA shall meet the requirements in Table 160–7 when measured using the method defined in 52.9.6

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with the following exceptions:

a) The optical return loss *x* is 15.6 dB for 50GBASE-BR10, 15 dB for 50GBASE-BR20, and 15 dB for 50GBASE-BR40.
b) The upper –3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate (i.e., 26.6 GHz).
c) The test pattern is according to Table 160–10.

160.7.10 Receiver sensitivity

For 50GBASE-BR10, receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 3.2 dB. Receiver sensitivity should meet Equation (160–1), which is illustrated in Figure 160–6.

For 50GBASE-BR20 and 50GBASE-BR40, receiver sensitivity is optional and is defined for a transmitter with a value of SECQ up to 3.2 dB. Receiver sensitivity should meet Equation (160–2), which is illustrated in Figure 160–6.

$$RS = \max(-8.4, SECQ - 9.8) \quad \text{(dBm)} \tag{160–1}$$

$$RS = \max(-15.1, SECQ - 16.5) \quad \text{(dBm)} \tag{160–2}$$

where

RS is the receiver sensitivity
SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

The normative requirement for receivers is stressed receiver sensitivity.

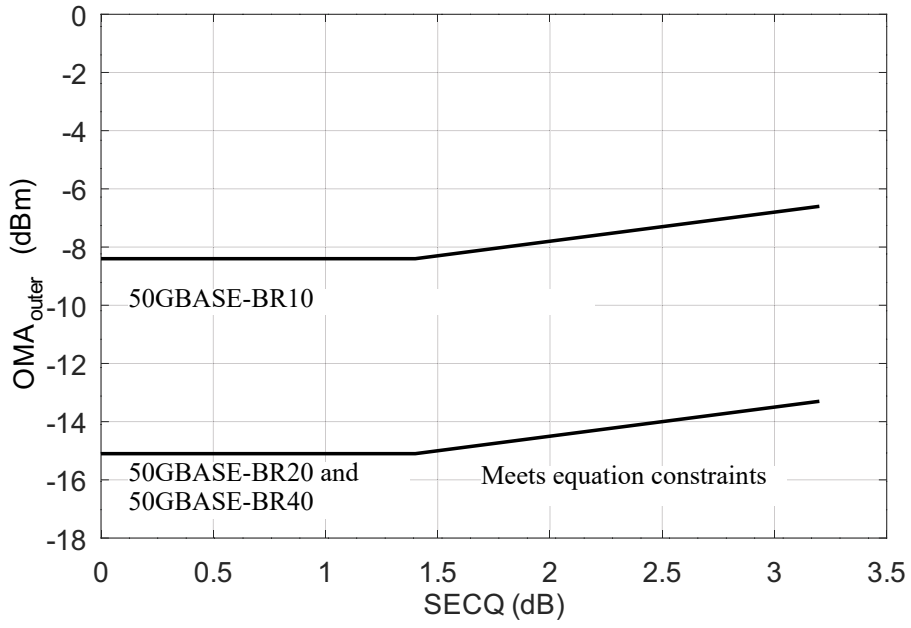

Figure 160–6—Illustration of receiver sensitivity

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160.7.11 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 160–7 for 50GBASE-BRx if measured using the method defined in 160.7.11.1 and 160.7.11.3, with the conformance test signal at TP3 as described in 160.7.11.2, using the test pattern specified for SRS in Table 160–10.

Any of the patterns specified for SRS in Table 160–10 is sent from the transmit section of the PMD under test. The signal being transmitted is asynchronous to the received signal. The reflectance of the optical link should be at its maximum level.

160.7.11.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 160–7. The patterns used for the received conformance signal are specified in Table 160–10. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 160.7.11.2 and has sinusoidal jitter applied as specified in 121.8.10.4. A suitable test set is needed to characterize the signal used to test the receiver. Stressed receiver conformance test signal verification is described in 160.7.11.3.

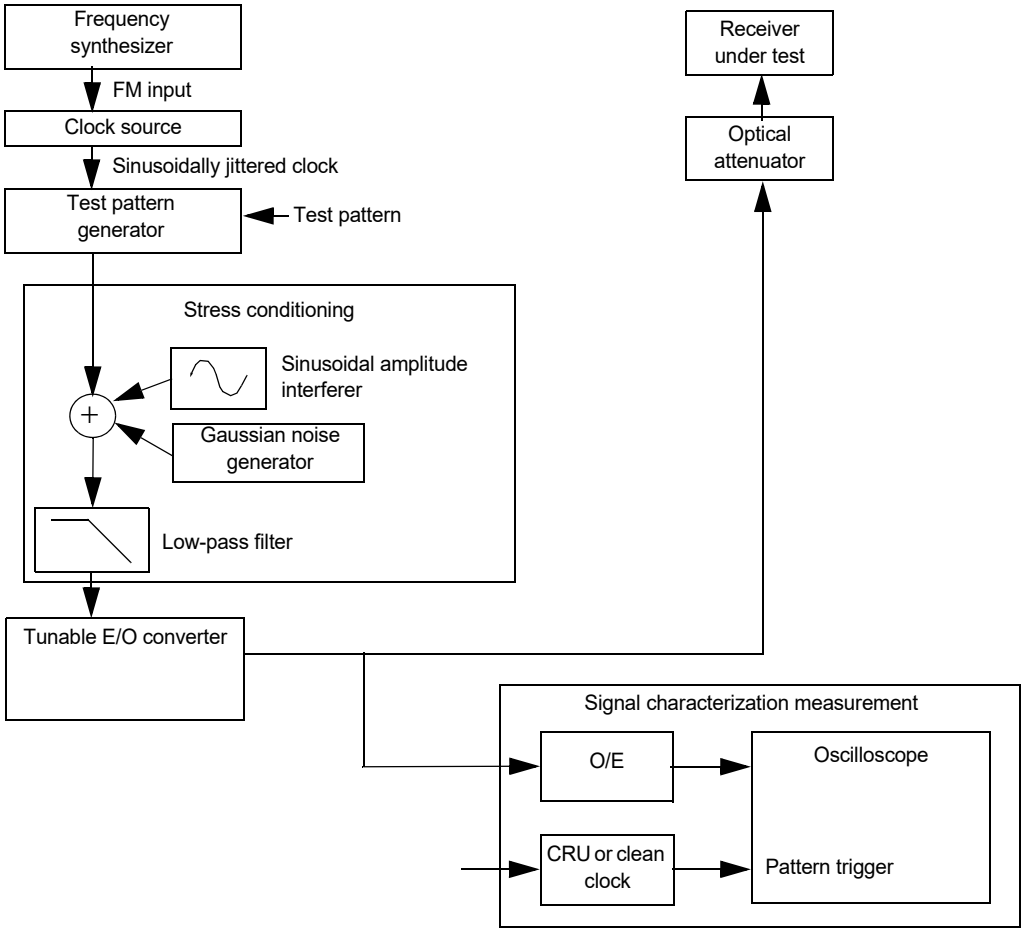

Figure 160–7—Stressed receiver conformance test block diagram

The low-pass filter is used to create ISI. The sinusoidal amplitude interferer causes additional eye closure, but in conjunction with the finite edge rates, also causes some jitter.

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The sinusoidally jittered clock represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter. The sinusoidal amplitude interferer may be set at any frequency between 100 MHz and 2 GHz, although care should be taken to avoid harmonic relationships between the sinusoidal interferer, the sinusoidal jitter, the signaling rate, and the pattern repetition rate. The Gaussian noise generator, the amplitude of the sinusoidal interferer, and the low-pass filter are adjusted so that the SECQ specified in Table 160–7 is met, according to the methods specified in 160.7.11.2.

For improved visibility for calibration, all elements in the signal path (cables, DC blocks, E/O converter, etc.) should have wide and smooth frequency response, and linear phase response, throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be negligible.

160.7.11.2 Stressed receiver conformance test signal characteristics and calibration

The stressed receiver conformance test signal characteristics and calibration methods are as described in 121.8.10.2 with the following exceptions:

- The SECQ of the stressed receiver conformance test signal is measured according to 160.7.5, except that the test fiber is not used. The transition time of the stressed receiver conformance test signal is no greater than the value specified in Table 160–6.
- With the Gaussian noise generator on and the sinusoidal jitter and sinusoidal interferer turned off, $RIN_{15.6}OMA$, $RIN_{15}OMA$, and $RIN_{15}OMA$ of the SRS test source for 50GBASE-BR10, 50GBASE-BR20, and 50GBASE-BR40, respectively, should be no greater than the values specified in Table 160–6.
- An example stressed receiver conformance test setup is shown in Figure 160–7; however, alternative test setups that generate equivalent stress conditions may be used.
- The signaling rate of the test pattern generator and the extinction ratio of the E/O converter are as given in Table 160–6 for 50GBASE-BRx.
- The required values of the “Stressed receiver sensitivity (OMA_{outer}) (max)” and “Stressed eye closure for PAM4 (SECQ)” are as given in Table 160–7 for 50GBASE-BRx.

160.7.11.3 Stressed receiver conformance test signal verification

The SECQ of the stressed receiver conformance test signal is measured according to 160.7.5, except that the test fiber is not used. The clock output from the clock source in Figure 160–7 is modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye jitter that includes the sinusoidal jitter component, a separate clock source (clean clock of Figure 160–7) is required that is synchronized to the source clock, but not modulated with the jitter source.

Care should be taken when characterizing the test signal because excessive noise/jitter in the measurement system would result in an input signal that does not fully stress the receiver under test. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. The noise/jitter introduced by the O/E, filters, and oscilloscope should be negligible or the results should be corrected for its effects. While the details of test equipment are beyond the scope of this standard, it is recommended that the implementer fully characterize the test equipment and apply appropriate guard bands to ensure that the stressed receiver conformance input signal meets the stress and sinusoidal jitter specified in 160.7.11.2 and 121.8.10.4.

160.8 Safety, installation, environment, and labeling

160.8.1 General safety

Equipment subject to this clause shall conform to the general safety requirements in J.2.

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160.8.2 Laser safety

50GBASE-BRx optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly defines requirements and usage restrictions on the host system necessary to meet these safety certifications.[259]

160.8.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

160.8.4 Environment

Normative specifications in this clause shall be met by a system integrating a 50GBASE-BRx PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause are met.

160.8.5 Electromagnetic emission

A system integrating a 50GBASE-BRx PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

160.8.6 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

160.8.7 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 50GBASE-BR10-D). Labeling requirements for Hazard Level 1 lasers are given in the laser safety standards referenced in 160.8.2.

[259] A host system that fails to meet the manufacturer's requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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160.9 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 160–8.

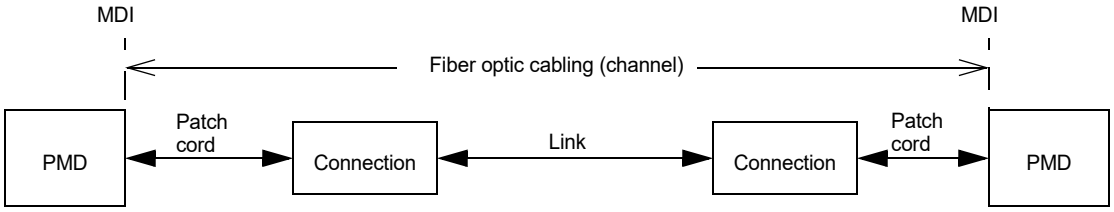

Figure 160–8—Fiber optic cabling model

The channel insertion loss is given in Table 160–12. A channel may contain additional connectors as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, and polarization mode dispersion meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with IEC 61280-4-2 one-cord reference method. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 160–12—Fiber optic cabling (channel) characteristics

Description	50GBASE-BR10	50GBASE-BR20	50GBASE-BR40	Unit
Operating distance (max)	10	20	40	km
Channel insertion loss[a, b] (max)	6.2	15	18	dB
Channel insertion loss (min)	0	0	10	dB
Positive dispersion[b] (max)	35	38.5	79	ps/nm
Negative dispersion[b] (min)	–64	–83	–166	ps/nm
DGD_max[c]	8	10.3	10.3	ps
Optical return loss (min)	21	21	21	dB

[a] These channel insertion loss values include cable, connectors, and splices.
[b] Over the wavelength range 1260 nm to 1340 nm for 50GBASE-BR10 and 1281 nm to 1322 nm for 50GBASE-BR20 and 50GBASE-BR40.
[c] Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

160.10 Characteristics of the fiber optic cabling (channel)

The 50GBASE-BRx fiber optic cabling shall meet the specifications defined in Table 160–12. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

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160.10.1 Optical fiber cable

The optical fiber cable requirements are satisfied by cables containing ITU-T G.652.B (dispersion unshifted), type G.652.D (low water peak, dispersion unshifted), or type G.657.A1 or type G.657.A2 (bend insensitive) fibers or the requirements in Table 160–12 where they differ.

160.10.2 Optical fiber connection

An optical fiber connection, as shown in Figure 160–8, consists of a mated pair of optical connectors.

160.10.2.1 Connection insertion loss

Connections with different loss characteristics may be used provided the requirements of Table 160–12 are met. The maximum link distance for 50GBASE-BR10 and 50GBASE-BR40 is based on an allocation of 2 dB total connection and splice loss. The maximum link distance for 50GBASE-BR20 is based on an allocation of 5 dB total connection and splice loss.

160.10.2.2 Maximum discrete reflectance

The maximum value for each discrete reflectance shall be less than or equal to the value shown in Table 160–13 corresponding to the number of discrete reflectances above –55 dB within the channel. For numbers of discrete reflectances in between two numbers shown in the table, the lower of the two corresponding maximum discrete reflectance values applies.

Table 160–13—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance		
	50GBASE-BR10	50GBASE-BR20	50GBASE-BR40
1	–25 dB	–22 dB	–19 dB
2	–31 dB	–29 dB	–27 dB
4	–35 dB	–34 dB	–32 dB
6	–38 dB	–37 dB	–35 dB
8	–40 dB	–39 dB	–37 dB
10	–41 dB	–40 dB	–39 dB

160.10.3 Medium Dependent Interface (MDI) requirements

The 50GBASE-BRx PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the “fiber optic cabling” (as shown in Figure 160–8). Examples of an MDI include the following:

a) Connectorized fiber pigtail
b) PMD receptacle

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of IEC 61753-1-1 and IEC 61753-021-2.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 160.5.1, not at the MDI.

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160.11 Requirements for interoperation between 50GBASE-BRx PMDs

The 50GBASE-BR20 and 50GBASE-BR40 PMDs can interoperate with each other (over an engineered link) provided that the fiber optic cabling (channel) characteristics are met, with the exception of the maximum and minimum channel insertion loss values, which are given in Table 160–14 for the two link directions separately. Attenuators may be used to achieve the required losses.

Table 160–14—Channel insertion loss requirements for interoperation between 50GBASE-BR20 and 50GBASE-BR40

Direction	Min loss	Max loss	Unit
50GBASE-BR20 transmitter to 50GBASE-BR40 receiver	7	15	dB
50GBASE-BR40 transmitter to 50GBASE-BR20 receiver	3	18	dB

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160.12 Protocol implementation conformance statement (PICS) proforma for Clause 160, Physical Medium Dependent (PMD) sublayer and medium, types 50GBASE-BR10, 50GBASE-BR20, and 50GBASE-BR40[260]

160.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 160, Physical Medium Dependent (PMD) sublayer and medium, types 50GBASE-BR10, 50GBASE-BR20, and 50GBASE-BR40, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

160.12.2 Identification

160.12.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

160.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Clause 160, Physical Medium Dependent (PMD) sublayer and medium, types 50GBASE-BR10, 50GBASE-BR20, and 50GBASE-BR40,
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[260]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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160.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*BR10	50GBASE-BR10 PMD	160.6	Device supports requirements for 50GBASE-BR10 PHY	O.1	Yes [ ] No [ ]
*BR20	50GBASE-BR20 PMD	160.6	Device supports requirements for 50GBASE-BR20 PHY	O.1	Yes [ ] No [ ]
*BR40	50GBASE-BR40 PMD	160.6	Device supports requirements for 50GBASE-BR40 PHY	O.1	Yes [ ] No [ ]
*INS	Installation / cable	160.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Reference point TP1 exposed and available for testing	160.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Reference point TP4 exposed and available for testing	160.5.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	160.3	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO capability	160.4	Registers and interface supported	O	Yes [ ] No [ ]

160.12.4 PICS proforma tables for PMD sublayer and medium, types 50GBASE-BR10, 50GBASE-BR20, and 50GBASE-BR40

160.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 50GBASE-R PCS, RS-FEC, and PMA	160.1		M	Yes [ ]
F2	Integration with management functions	160.1		O	Yes [ ] No [ ]
F3	Bit error ratio	160.1.1	Meets the BER specified in 160.1.1	M	Yes [ ]
F4	Transmit function	160.5.2	Conveys symbols from PMD service interface to MDI	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
F5	Mapping between optical signal and logical signal for transmitter	160.5.2	Optical power levels from lowest to highest correspond to tx_symbol values zero, one, two, and three, respectively	M	Yes [ ]
F6	Receive function	160.5.3	Conveys symbols from MDI to PMD service interface	M	Yes [ ]
F7	Conversion of optical signal to electrical signal	160.5.3	For delivery to the PMD service interface	M	Yes [ ]
F8	Mapping between optical signal and logical signal for receiver	160.5.3	Optical power levels from lowest to highest correspond to rx_symbol values zero, one, two, and three, respectively	M	Yes [ ]
F9	Global Signal Detect function	160.5.4	Report to the PMD service interface the message PMD:IS_SIGNAL.indication (SIGNAL_DETECT)	M	Yes [ ]
F10	Global Signal Detect behavior	160.5.4	SIGNAL_DETECT is a global indicator of the presence of an optical signal	M	Yes [ ]
F11	PMD reset function	160.5.5	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]
F12	ONU silent start	160.5.10	Meets the specifications defined in 160.5.10	M	Yes [ ]

160.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Management register set	160.4		MD:M	Yes [ ] N/A [ ]
M2	Global transmit disable function	160.5.6	Disables the optical transmitter with the PMD_global_transmit_disable variable	M	Yes [ ]
M3	PMD_fault function	160.5.7	Sets PMD_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M4	PMD_transmit_fault function	160.5.8	Sets PMD_transmit_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
M5	PMD_receive_fault function	160.5.9	Sets PMD_receive_fault to one if a local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]

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160.12.4.3 PMD to MDI optical specifications for 50GBASE-BR10

Item	Feature	Subclause	Value/Comment	Status	Support
BR101	Transmitter meets specifications in Table 160–6	160.6.1	Per the definitions in 160.7	BR10:M	Yes [ ] N/A [ ]
BR102	Receiver meets specifications in Table 160–7	160.6.2	Per the definitions in 160.7	BR10:M	Yes [ ] N/A [ ]

160.12.4.4 PMD to MDI optical specifications for 50GBASE-BR20

Item	Feature	Subclause	Value/Comment	Status	Support
BR201	Transmitter meets specifications in Table 160–6	160.6.1	Per the definitions in 160.7	BR20:M	Yes [ ] N/A [ ]
BR202	Receiver meets specifications in Table 160–7	160.6.2	Per the definitions in 160.7	BR20:M	Yes [ ] N/A [ ]

160.12.4.5 PMD to MDI optical specifications for 50GBASE-BR40

Item	Feature	Subclause	Value/Comment	Status	Support
BR401	Transmitter meets specifications in Table 160–6	160.6.1	Per the definitions in 160.7	BR40:M	Yes [ ] N/A [ ]
BR402	Receiver meets specifications in Table 160–7	160.6.2	Per the definitions in 160.7	BR40:M	Yes [ ] N/A [ ]

160.12.4.6 Optical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
M1	General measurement	160.7	Meets the specifications defined in 160.7	M	Yes [ ]

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160.12.4.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	160.8.1	Conforms to the general safety requirements in J.2	M	Yes [ ]
ES2	Laser safety —IEC Hazard Level 1	160.8.2	Conforms to Hazard Level 1 laser requirements defined in IEC 60825-1 and IEC 60825-2	M	Yes [ ]
ES3	Electromagnetic interference	160.8.5	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

160.12.4.8 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	160.10	Meets the specifications defined in Table 160–12	INS: M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	160.12.2.2	Less than or equal to the value shown in Table 160–13	INS: M	Yes [ ] N/A [ ]
OC3	MDI requirements	160.6.3	Meets IEC 61753-1-1 and IEC 61753-021-2	INS: M	Yes [ ] N/A [ ]

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Annex B

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System guidelines

B.1 Baseband system guidelines and concepts, 10 Mb/s

B.1.1 Overall system objectives

The CSMA/CD Access Method, supported by baseband technology, depends on a variety of analog system components at and below the physical level of the OSI Reference Model. These components provide basic interconnection facilities for the CSMA/CD access mechanism itself and are defined throughout Clause 6, Clause 7, and Clause 8.

Overall performance of the analog baseband medium and related Physical Layer capabilities depends on an optimal and known set of analog capabilities within each of these critical system elements: the coaxial trunk cable, MAUs, branch cables, DTEs, and repeater units. These system elements affect the integrity with which the serial data bit stream analog signals are carried between open systems. There are at least three critical parameters of interest: bits lost in the transmission system, signal delays, and phase jitter. It is important that these be apportioned properly among the affected system elements.

The successful interconnection of multivendor system components mandates that the values for bits lost, signal delays, and phase jitter be allocated fairly and realistically among the various system elements. The balance of Annex B identifies the upper limits of values to be placed on the subject parameters. These values are based on the maximal system configuration (for example, four repeater units, 2.5 km trunk coaxial cable medium).

B.1.2 Analog system components and parameter values

The values given in the following table are in terms of bits and are stated as maximum values except for values given within ranges.

The initial mnemonic under each component entry refers to the system component as identified in Figure B–1. System parameters are stated in terms of the intralayer or interlayer messages sent within a station. Specific delays are called out as = delay.

The repeater concepts described throughout this annex are considered to be an acceptable set of specifications for a multirepeatered system. It is noted that the exact parametric values specified for the repeater environment are subject to minor refinement.

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Component and parameter	Startup delay	Last in to last out delay	Startup loss
MEDIUM			
Trunk Coaxial Cable			
C1 Propagation	0.0	21.65	0.0
POINT-TO-POINT LINK			
P1 Propagation	0.0	25.64	0.0
AUI			
A1 Propagation	0.0	2.57	0.0
MEDIUM ACCESS UNIT			
M1 DATA IN ASSERT → INPUT	6.0	0.5	5.0
M2 OUTPUT → DATA OUT ASSERT	3.0	0.5	2.0
M3 DATA IN COLLISION → SQE ASSERT	17.0	—	—
M4 COLLISION DEASSERT → SQE DEASSERT	20.0	—	—
M5 OUTPUT IDLE → SQE ASSERT	$6 < x < 16$	—	—
M6 SQE TEST ASSERT → SQE DEASSERT	$5 \leq x \leq 15$	—	—
DTE			
D1 INPUT → INPUT UNIT	18.0	—	18.0
D2 OUTPUT UNIT → OUTPUT	—	3.0	—
D3 INPUT → CARRIER STATUS = CARRIER ON	3.0	—	—
D4 INPUT IDLE → CARRIER STATUS = OFF	$3.0 < x \leq 6.0$	—	—
D5 SQE ASSERT → CARRIER STATUS = ON	3.0	—	—
D6 SQE DEASSERT → CARRIER STATUS = OFF	$3.0 < x \leq 6.0$	—	—
D7 SQE ASSERT → SIGNAL STATUS = ERROR	3.0	—	—
D8 SQE DEASSERT → SIGNAL STATUS = NO ERROR	$3.0 < x \leq 6.0$	—	—
D9 CARRIER STATUS = OFF → OUTPUT UNIT	$96 \leq x \leq 100$	—	—
D10 INPUT → OUTPUT	8.0	—	—
D11 SIGNAL STATUS = ERROR → JAM OUTPUT	16.0	—	—
D12 JAM OUTPUT DURATION	=32.0	—	—
REPEATER UNIT			$22 < x < 34$
R1 INPUT 1,2 → OUTPUT 2,1	7.5	—	—
R2 INPUT IDLE 1,2 → OUTPUT IDLE 2,1	—	12.5	—
R3 INPUT 1,2 → CARRIER STATUS = ON	3.0	—	—
R4 SQE → SOURCED OUTPUT	6.5	—	—
R5 JAM OUTPUT → OUTPUT IDLE	=96.0	—	—

Figure B–1 indicates the maximal system configuration and identifies the various system component parameters considered critical in determining analog system performance.

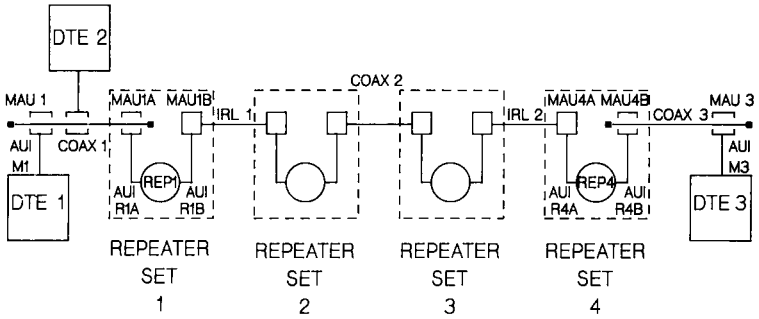

Figure B–1—Maximal system configuration bit budget apportionments

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B.1.3 Minimum frame length determination

The following table indicates the system elements that make up the minimum frame length calculation based on the worst-case numbers as outlined in the bit budget of B.1.2. The compilation in the following table is based on the following scenario:

a) DTE 1 transmits to an adjacent DTE 2 on coaxial segment 1.
b) DTE 3 transmission collides with DTE 1 transmission.
c) DTE 3 is assumed to be the worst-case distance from DTE 1 and its transmission just misses deferring to the DTE 1 message.
d) The collision fragment travels back down the network to inform DTE 1 that a collision has occurred on its message.

Component and function	Direction	Table entry	Delay	Total delay
DTE 1 STARTS TO PUT OUT FIRST BIT				0.0
DTE 1	FWD	D2	3.0	3.0
AUI M1	FWD	A1	2.57	5.57
MAU1	FWD	M2	3.0	8.6
COAX1	FWD	C1	21.65	30.2
REPEATER SET 1				
MAU 1A	FWD	M1	6.0	36.2
AUI R1A	FWD	A1	2.57	38.8
REP 1	FWD	R1	7.5	46.3
AUI R1B	FWD	A1	2.57	48.9
MAU 1B	FWD	M2	3.0	51.9
REPEATER SET TOTAL			21.64	
IRL 1	FWD	P1	25.64	77.5
REPEATER SET 2	FWD		21.6	99.1
COAX 2	FWD	C1	21.65	120.8
REPEATER SET 3	FWD		21.6	142.4
IRL 2	FWD	P1	25.64	168.1
REPEATER SET 4	FWD		21.6	189.7
COAX 3	FWD	C1	21.65	211.4
MAU 3	FWD	M1	6.0	217.4
AUI 3	FWD	A1	2.57	219.9
DTE 3 PUTS OUT A BIT	REV	D10	8.0	227.9
AUI 3	REV	A1	2.57	230.5
MAU 3	REV	M2	3.0	233.5
COAX 3	REV	C1	21.65	255.1
REPEATER SET 4				
MAU 4B	REV	M3	17.0	272.1
AUI 4B	REV	A1	2.57	274.7
REP 4	REV	R4	6.5	281.2
AI 4A	REV	A1	2.57	283.8
MAU 4A	REV	M2	3.0	286.8
REPEATER SET TOTAL			31.64	
IRL 2	REV	P1	25.64	312.4
REPEATER SET 3	REV		31.64	344.1
COAX 2	REV	C1	21.65	365.7
REPEATER 2	REV		31.64	397.4
IRL 1	REV	P1	25.64	423.0
REPEATER SET 1	REV		31.64	454.6
COAX 1	REV	C1	21.65	476.3
MAU 1	REV	M3	17.0	493.3
AUI M1	REV	A1	2.57	495.9
DTE 1	REV	D7	3.0	498.9

The frame length is constrained by two parameters:

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— The message from DTE 1 shall be long enough so that it is still sending when the collision is detected.
— The message from DTE 1 shall be short enough such that DTE 2 can throw out the message on the basis of being too short.

The above table provides the scenario that enables DTE 1 to determine a collision is taking place. DTE 1 shall transmit for at least 499 bit times. To determine how much longer DTE 2 will continue to receive bits, assume that DTE 1 is the last transmitter to provide bits to the DTE 2 MAU. DTE 2 then sees the following:

Component and function	Direction	Table entry	Delay	Total delay
DTE 1	FWD	D11	16.0	514.9
DTE 1	FWD	D12	32.0	547.9
AUI M1	FWD	A1	2.57	549.4

If Repeater Set 1 is the last system component to provide bits to DTE 2, then DTE 2 will see the following:

Component and function	Direction	Table entry	Delay	Total delay
REPEATER SET 1 (1st JAM BIT)				454.6
REP 1	REV	R5	96.0	550.6
COAX 1	REV	C1	21.65	572.3

The Repeater Set is the last transmitter to provide a bit to DTE 2. The DTE 2 MAU starts seeing bits at time 8.6, which means that DTE 2 sees 563.7 bits (572.3 – 8.6). DTE 2 sees a minimum of 61 preamble bits and 8 SFD bits. The preamble and SFD bits can be deleted from the 563.7 total because they are not counted in minimum frame length.

The minimum frame length determination from the above scenario is then 564.7 – 69.0 = 494.7 bits. The 10 Mb/s system value for minimum frame length has been set at 512 bits.

B.1.4 System jitter budgets

The typical jitter budget expected for the baseband system is apportioned in the following manner:

Encoder	0.5 ns
AUI Cable	1.0 ns (transmit end)
MAU Transmit	2.0 ns
Trunk Coax	7.0 ns
MAU Receive	–1.0 ns (with compensation)
AUI Cable	1.0 ns (receive end)
SNR on COAX	5.0 ns (SNR = 5:1)
SNR on AUI	0.5 ns (SNR = 5:1, transmit end)
SNR on AUI	0.5 ns (SNR = 5:1, receive end)
	16.5 ns

The 18 ns jitter budget leaves adequate design margin for implementation-dependent considerations.

B.1.4.1 Nominal jitter values

The jitter budget values given above are not expected to accommodate all step changes in phase jitter due to system parameter variations within one or a few bit times.

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B.1.4.2 Decoder evaluation

The phase decoder in the PLS sublayer should correctly decode a Manchester-encoded signal whose data transition point (center of a bit cell) has a peak-to-peak jitter of no more than 36 ns (± 18 ns deviation from the bit cell center). Figure B–2 and Figure B–3 show the test method.

Evaluation of decoder performance may be simulated and tested by application of three distinct waveforms representing worst-case and normal conditions. The waveforms contain Manchester-encoded bits whose center transitions represent the extremes of maximum skew. A 5 MHz (repetition rate) pulse train whose pulse width is either 64 ns or 136 ns simulates the two worst-case jitter conditions. The data output from the decoder should remain stable for each of the three test patterns and shifts between these extremes where there is a low rate of change in center transition skew. Note that the actual transmission system is not expected to permit sudden drastic changes in the steady-state edge deviation during the reception of any given frame. The above evaluation process is not intended to guarantee proper decoder performance under all operating conditions.

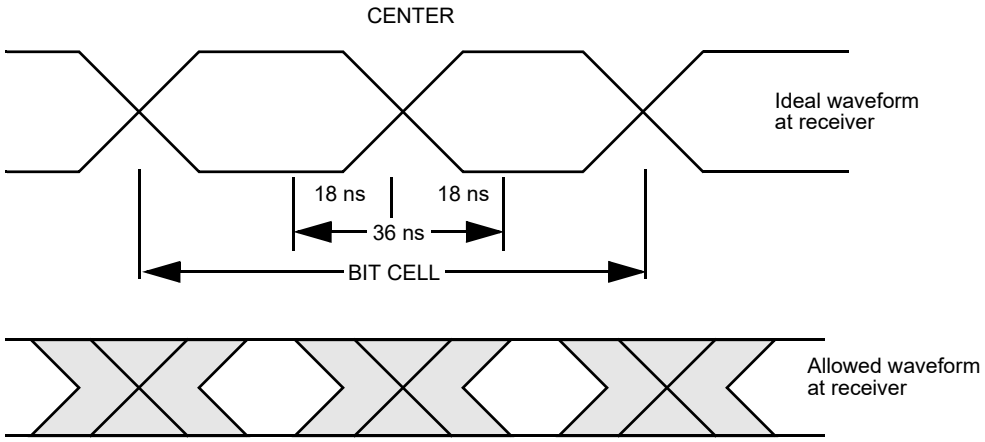

Figure B–2—Typical signal waveforms

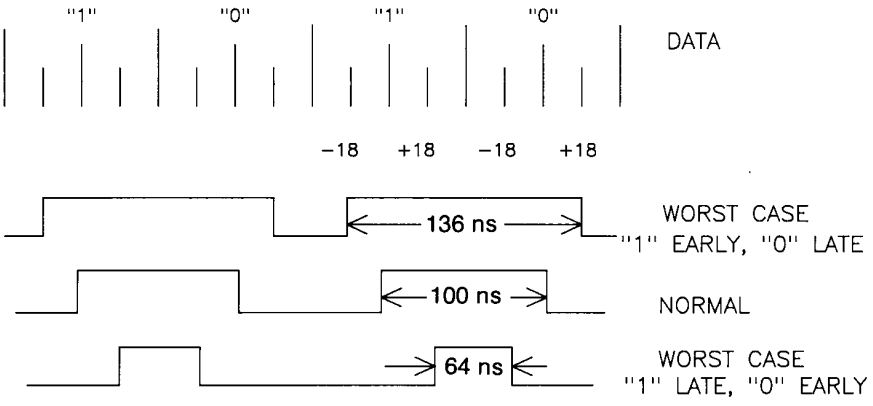

Figure B–3—Worst-case signal waveform variations

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B.1.5 Systems consideration calculations

B.1.5.1 Overview

Subclause B.1.3 contains a calculation of maximum fragment size for a network of 10BASE5 and IRL segments. That calculation was based on the maximum delay for a transmission to reach the far end of the network and for a collision to propagate back. Since that calculation was written, many new media and MAU types have been added to this standard. Also, the calculation of B.1.3 did not address the interpacket gap shrinkage, which can limit the network size. It is not practical to perform a separate calculation for each possible combination of segment types.

Some new segment types also support much longer media (up to 2 km). Introduction of longer media also required a more flexible calculation method that allowed trading segment length for repeaters. The method in this section was developed to meet these needs.

Actual numbers used to calculate delay and variability are tabulated (Table B–1) at the end of this subclause.

B.1.5.2 Maximum collision fragment size

The round-trip delay has to be calculated to determine that collision will be received within the collision window of transmitting DTEs and that collision fragments will be less than the minimum frame size. The following scenario is used for the calculations (see Figure B–4):

a) DTE1 transmits.
b) DTE1's transmission propagates to DTE2.
c) DTE2 begins transmitting at the last possible time, colliding and transmitting 96 bits.
d) DTE2's transmission propagates to DTE1.
e) DTE1 detects collision, jams, and stops transmitting.

The following conditions have to be met for proper network operation:

— DTE1 has to detect collision before having transmitted the 512th bit (including preamble and SFD bits).
— DTE1 has to stop transmitting before having transmitted a minimum length frame, 576 bits (512 bits after SFD).
— The overlap between DTE1's transmission and DTE2's transmission has to be less than 575 bits (511 bits after the SFD transmitted by DTE1).

For all existing segment types, the last condition is the limiting factor; if it is met then the other two conditions are also met.

The maximum time between the first bit and the last bit of the overlapping transmissions of the two DTEs colliding across a path will be called the Path Delay Value (PDV). Many factors contribute to this delay. Simplification of the delay calculation, as compared to the method used in B.1.3, can be achieved by using a set of base numbers, Segment Delay Values (SDV), for each segment type that combines the factors that contribute to the round-trip delay associated with that segment. The PDV is the sum of SDVs of the segments that comprise the path.

For each segment type, one of three base SDVs is used depending on the position of the segment: left-end, mid-, or right-end. The left-end segment is connected to the DTE that transmits first (DTE1). The right-end segment is connected to the colliding DTE (DTE2). All segments between these are mid-segments.

For this calculation, the left-end base SDV contains all delays from DTE1 through the MAU and its AUI connected to the repeater unit. Each mid-base SDV includes the delays from the repeater unit on the left

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through the MAU and its AUI connected to the right repeater unit. The right-end base SDV includes the delays from the repeater unit immediately to its left through DTE2. (See Figure B–4.)

Only the bit loss of DTE1's MAU on the left-end segment contributes to fragment size. The steady-state delay of that MAU and the AUI cable delay do not contribute. For the remainder of the network, startup delay (the sum of steady-state delay and bit loss) contribute. Therefore, the left-end base SDV uses MAU transmit bit loss and 1 AUI delay. In all other cases, startup delay and 2 AUI delays are used.

Propagation delays for media are not included in the base SDVs. These are added in separately to allow for various segment lengths (see 13.4.1). The base SDVs for the mid- and right-end segments (except 10BASE-FB) include two 2 m AUI cables and the delay of each one is experienced twice, once in the forward path and once in the reverse path. Therefore, a delay of 0.5 BT per segment is added and corresponds to the round-trip delay through two 2 m AUI cables. The base numbers for the left segment include one 2 m AUI cable, 0.25 BT.

For each segment type, both the delay to transmission of the 96th bit after collision rise and delay to transmission of the last bit due to collision fall are calculated. The base SDV is the larger of these two.

The maximum allowed sum of SDVs plus media propagation delays is 575 BT.

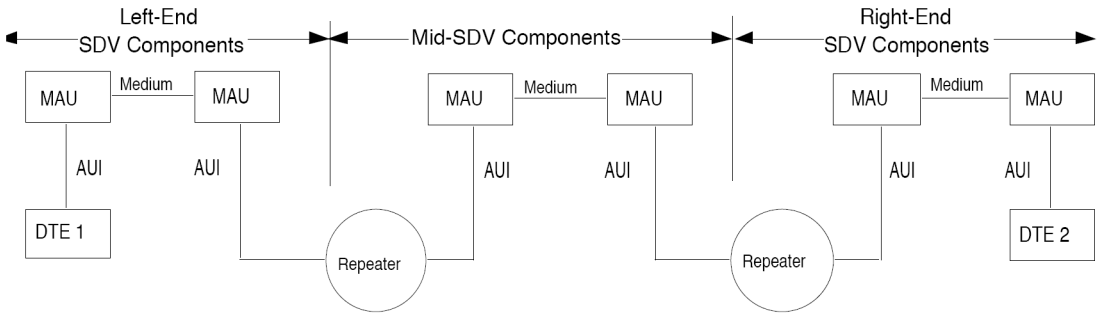

Figure B–4—Round-trip delay calculation model

B.1.5.2.1 Left-end base SDV

The Left-End Segment collision delay is the sum of the following:

Forward delay:
- AUI
- MAU transmit bit-loss delay
- Media rise time
- MAU receive startup delay

Reverse delay:
- MAU transmit fall delay after collision
- MAU receive fall delay after collision

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B.1.5.2.2 Mid-base SDV

The Mid-Segment collision rise delay is the sum of the following:

Forward delay:
- AUI × 2
- Repeater start-of-packet propagation delay
- MAU transmit startup delay
- Media rise time
- MAU receive startup delay

Reverse delay:
- MAU transmit startup delay
- MAU collision detect delay
- Repeater start-of-collision propagation delay

The Mid-Segment collision fall delay is the sum of the following:

Forward delay:
- AUI × 2
- Repeater start-of-packet propagation delay
- MAU transmit startup delay
- Media rise time
- MAU receive startup delay

Reverse delay:
- MAU transmit fall delay
- MAU collision fall delay
- Repeater cessation-of-jam propagation delay

B.1.5.2.3 Right-end base SDV

The Right-End Segment collision rise delay is the sum of the following:

Forward delay:
- AUI × 2
- Repeater start-of-packet propagation delay
- MAU transmit startup delay
- Media rise time
- MAU receive startup delay
- DTE receive-to-transmit-not-deferred delay

Reverse delay:
- MAU transmit startup delay
- MAU collision detect delay
- Repeater start-of-collision propagation delay
- Repeater minimum transmit length

The Right-End Segment collision fall delay is the sum of the following:

Forward delay:
- AUI × 2
- Repeater start-of-packet propagation delay
- MAU transmit startup delay

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Media rise time
MAU receive startup delay
DTE receive-to-transmit-not-deferred delay
DTE minimum transmit length

Reverse delay:
MAU transmit fall delay
MAU collision fall delay
Repeater cessation-of-jam propagation delay

B.1.5.3 Interpacket Gap (IPG) shrinkage

IPG shrinkage occurs because two successive packets may experience differing bit loss on the same path. When the packet passes through a repeater, the lost preamble bits are regenerated. If the first packet experiences greater bit loss than the second, the IPG between them will shrink.

IPG shrinkage is also calculated using a lumped number for each segment, the Segment Variability Value (SVV). For each segment type, one of two SVVs is used depending on the position of the segment: transmitting end or mid. The transmitting end segment is connected to the transmitting DTE or DTEs. The mid-segments are all the remaining segments except the one connected to the receiving DTE.

The transmitting end segment and the mid-segment SVVs each include the variability from the transmitting MAU through the repeater unit. Since, IPG shrinkage only occurs when a repeater restores the lost bits, the final segment does not contribute any variability (see Figure B–5).

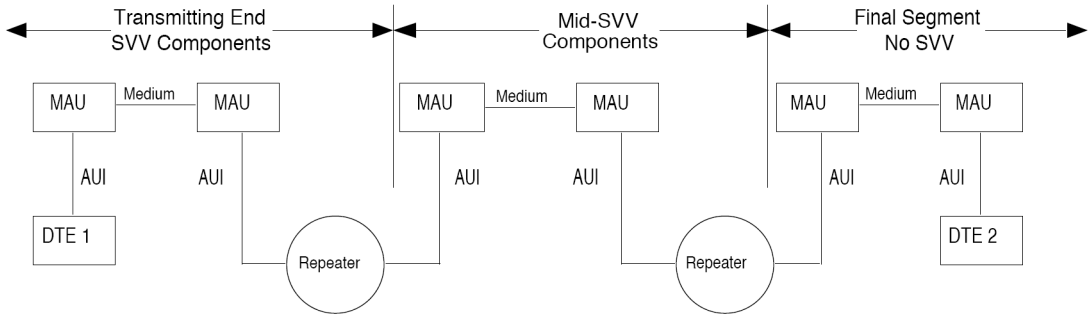

Figure B–5—Variability calculation model

B.1.5.3.1 Transmitting end segment variability value

The transmitting end segment variability value is the sum of the following:
MAU transmit startup-delay variability
MAU transmit startup-delay variability correction
MAU receive startup-delay variability
MAU receive startup-delay variability correction
Repeater start-of-packet propagation delay variability
Clock skew (2.5 BT)

NOTE—The variability correction values account for the possibility that on mixing segments the two successive packets can be originated by two different MAUs.

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B.1.5.3.2 Mid-segment variability value

The mid-segment variability value is the sum of the following:

MAU transmit startup-delay variability
MAU receive startup-delay variability
Repeater start-of-packet propagation delay variability

B.1.5.4 Timing parameters for round-trip delay and variability calculations

Table B–1 contains the timing parameters used in the calculation of SDVs and SVVs. The values in the table for MAU Collision Rise and MAU Collision Fall are those specific to the worst-case scenario. The parameters are defined in the following subclauses.

B.1.5.4.1 MAU parameters

Transmit Bit Loss: Number of bits received on the DO circuit and not transmitted to the MDI.

Transmit Startup Delay: Delay from the first bit received on the DO circuit to the first bit transmitted to the MDI. This is the sum of transmit bit loss and steady-state delay.

Receive Startup Delay: Delay from the first bit received on the MDI to the first bit transmitted to the DI circuit. This is the sum of receive bit loss and steady-state delay.

Collision Detect Delay: Delay from the arrival of collision at the MDI to transmission of signal_quality_error to the CI circuit. For 10BASE2 and 10BASE5, this includes the DC rise time on the media, given that the MAU has been transmitting for at least 20 BT when the collision arrives. For 10BASE-FP, this includes the delay until the second CRV occurs on the media (16.3.4.3).

Transmit Fall Delay: Delay from the last bit received on the DO circuit to the last bit transmitted to the MDI. This is the same as the steady-state delay.

Collision Fall Delay: Delay from arrival of end of collision at the MDI to end of transmission of signal_quality_error to the CI circuit. For 10BASE2 and 10BASE5, it includes the DC fall time of the media. For 10BASE-FP it includes the delay of 33 BT to pass with no more than one ORD_crv.

Transmit Startup Delay Variability: Packet-to-packet variations in transmit startup delay.

Transmit Startup Delay Variability Correction: Additional variability, when the transmitting end segment is a mixing segment, due to two MAUs transmitting with different startup delays. For 10BASE5 and 10BASE2, startup delay variability plus transmit startup delay variability correction equal transmit startup delay since these MAUs may transmit with as little as 0 BT delay. For 10BASE-FP MAUs, implementation considerations imposed by the requirements of 16.3.1.1 require the MAU to have at least 2 BT startup delay. Therefore, the transmit startup delay variability correction equals the transmit startup delay minus 2 BT.

Receive Startup Delay Variability: Packet-to-packet variability in receive startup delay.

Transmit Fall Delay After Collision: Delay from the last bit received on the DO circuit to the last bit transmitted to the MDI after the MAU has detected a collision. For all MAUs except 10BASE-FB, this is the same as transmit fall delay.

Receive Fall Delay After Collision: Delay from the last bit received on the MDI to the last bit transmitted to DI. For all MAUs except 10BASE-FB and 10BASE-FP, this is the same as receive steady-state delay.

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B.1.5.4.2 Repeater parameters

Start-of-Packet Propagation Delay: Delay from first bit received on DI to first bit transmitted on DO.

Start-of-Collision Propagation Delay: Delay from start of signal_quality_error on CI to first bit transmitted on DO.

Cessation-of-Jam Propagation Delay: Delay from end of signal_quality_error on CI to last bit transmitted on DO.

Minimum Transmit Length: Minimum delay from first bit transmitted on DO to last bit transmitted on DO.

Start-of-Packet Propagation Delay Variability: Packet-to-packet variation in start-of-packet propagation delay.

B.1.5.4.3 Media parameters

Media Rise Time: Start-of-packet DC rise time on 10BASE2 and 10BASE5 segments.

B.1.5.4.4 DTE parameters

Receive-to-Transmit-Not-Deferred Delay: Delay from first bit on DI to first bit on DO when the DTE does not detect carrier in time to defer.

Minimum Transmit Length: Minimum delay from first bit transmitted on DO to last bit transmitted on DO.

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Table B–1—Timing parameters for round-trip delay and variability calculations in bit times (BT)

Parameter	10BASE 5	10BASE 2	FOIRL	10BASE -T	10BASE-FP	10BASE-FB	10BASE-FL
AUI (2 m)	0.25	0.25	0.25	0.25	0.25	0.00	0.25
MAU							
Transmit bit loss	3.00	3.00	3.00	3.00	2.00	0.00	3.00
Transmit startup delay	3.50	3.50	3.50	5.00	5.50	2.00	5.00
Receive startup delay	6.50	6.50	3.50	8.00	2.50	2.00	5.00
Collision detect delay	17.00	17.00	3.50	9.00	9.50	3.50	3.50
Transmit fall delay	0.50	0.50	0.50	2.00	3.50	2.00	2.00
Collision fall delay	20.00	20.00	7.00	9.00	36.00	5.00	7.00
Transmit startup delay variability	2.00	2.00	2.00	2.00	3.00	0.00	2.00
Transmit startup delay variability correction	1.50	1.50	0.00	0.00	0.50	0.00	0.00
Receive startup delay variability	5.00	5.00	2.00	2.00	1.00	0.00	2.00
Receive startup delay variability correction	1.00	1.00	0.00	0.00	0.00	0.00	0.00
Transmit fall delay after collision	0.50	0.50	0.50	2.00	3.50	5.00	2.00
Receive fall delay after collision	0.50	0.50	0.50	2.00	3.00	5.00	2.00
REPEATER							
Start-of-packet propagation delay	8.00	8.00	8.00	8.00	8.00	8.00	8.00
Start-of-collision propagation delay	6.50	6.50	6.50	6.50	6.50	6.50	6.50
Cessation-of-jam propagation delay	5.00	5.00	5.00	5.00	5.00	5.00	5.00
Minimum transmit length	96.00	96.00	96.00	96.00	96.00	96.00	96.00
Start-of-packet propagation delay variability	4.00	4.00	4.00	4.00	4.00	2.00	4.00
MEDIA RISE TIME	1.00	1.00	0.00	0.00	0.00	0.00	0.00
DTE							
Receive-to-transmit-not-deferred delay	27.00	27.00	27.00	27.00	27.00	N/A[a]	27.00
Minimum transmit length	96.00	96.00	96.00	96.00	96.00	N/A[a]	96.00

[a]Not applicable; 10 BASE-FB does not support end (DTE) connections.

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B.2 System parameters and budgets for 1BASE5

B.2.1 Delay budget

The successful interconnection of multivendor system components mandates that the values for bits lost and signal delays be allocated fairly and realistically among the various system elements. The following table summarizes and indicates the derivation of some of the delays specified in 12.9. The breakdowns shown for the parameters are illustrative only; implementers are free to make other allocations of delay *within* a device so long as the specifications of 12.9 are not violated.

Component	Delay (BT)
DTE Initial Transmit Delay (see 12.9.2)	**3**
DTE Deference Delay (see 12.9.2)	**21**
unsquelch	3
Carrier detect	5
MAC detects carrier and defers	10
DTE Initial Transmit Delay	3
DTE Collision Shutdown Delay (see 12.9.2)	**58**
detect CP and report SIGNAL_ERROR	10
detect SIGNAL_ERROR and start jamming	16
jamSize	32
Medium Transit Delay (see 12.9.3)	**4**
Special Link Transit Delay (see 12.9.4)	**15**
Hub Startup Delay (see 12.9.5)	**12**
unsquelch	4
half fill FIFO	6
analogue of DTE Initial Transmit Delay	3
Hub Idle Collision Startup Delay (see 12.9.5) (same as Hub Startup Delay)	**12**
Hub Transit Delay (see 12.9.5)	**9**
half fill FIFO	6
analogue of DTE Initial Transmit Delay	3
Hub Delay Stretch/Shrink (see 12.9.5) ((preamble + <sfd> + maxFrameSize) · 0.01% · 2)	**3**
Hub Collision Detect Delay (see 12.9.5)	**21**
unsquelch	3
detect collision	6
Hub Transit Delay	9
First CVL or CVH may be preceded by CD0s and CD1s	3
Hub Active Collision Startup Delay (see 12.9.5)	**12**
Hub Transit Delay	9
First CVL or CVH may be preceded by CD0s and CD1s	3
Hub Collision Shutdown Delay (downward) (see 12.9.5) (same as Hub Transit Delay)	**9**
Hub Collision Shutdown Delay (upward) (see 12.9.5)	**25**
detect loss of carrier	20
clear FIFO, if necessary	2
analogue of DTE Initial Transmit Delay	3

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B.2.2 Minimum frame length determination

The minimum frame length for 1BASE5 is determined using the values specified in 4.4.2 and 12.9, applied to the following (worst) case:

a) DTE 1, connected to Hub 1 at a network extremity, transmits a message upward toward Hub 5.
b) There is a special link in the path between Hub 1 and Hub 5.
c) DTE 2, also connected to Hub 1, transmits, just missing deferring to the downward signal from DTE 1 that was wrapped around at Hub 5.
d) DTE 3, also connected to Hub 1, receives the transmission from DTE 1.
e) Hub 1 generates CP, which travels up and then back down the network to inform DTE 1 and DTE 2 that a collision has occurred on their messages.
f) DTE 1 and DTE 2 continue to transmit until they have received CP, reacted to it, and completed their jams.
g) DTE 3 continues to receive until the end of CP.

The minimum frame length has to allow both of the following conditions to be met:

— DTE 1 is still sending when CP is received and recognized.
— DTE 3 can discard the message fragment it receives because it is too short.

Event	Bits	Total
DTE 1 → DTE 2		
DTE Initial Transmit Delay	3	3
8 · Medium Transit Delay	32	35
2 · Special Link Transit Delay	30	65
10 · Hub Startup Delay	120	185
DTE Deference Delay	21	206
DTE 2 → HUB 1 CP		
Medium Transit Delay	4	210
Hub Collision Detect Delay	21	231
HUB 1 CP → HUB 5 CP		
3 · Medium Transit Delay	12	243
Special Link Transit Delay	15	358
4 · max(Hub Startup Delay, Hub Active Collision Startup Delay, Hub Idle Collision Startup Delay)	48	306
HUB 5 CP → DTE 1 receives CP		
5 · Hub Active Collision Startup Delay	60	366
4 · Medium Transit Delay	16	382
Special Link Transit Delay	15	397
DTE 1 receives CP → DTE 1 stops transmitting DTE Collision Shutdown Delay	58	455
COMPUTATION OF MINIMUM FRAME SIZE	–64	391 = data bits transmitted
original preamble + <sfd>		
5 · (Hub Collision Shutdown Delay (upward) – Hub Transit Delay)	80	471
5 · (Hub Collision Shutdown Delay (downward) – Hub Transit Delay)	0	471
Tiny fraction of Hub Delay Stretch/Shrink	0	471 = data bits received

The minimum frame length has to exceed both the maximum number of bits sent before recognizing CP (391 – jamsize = 359) and the maximum collision fragment size (471), as computed above. The 1BASE5

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system value for minimum frame length has been set at 512 bits, which exceeds both of these values with a margin for error.

B.2.3 Jitter budget

The total edge jitter of the signals on each link has to be limited to allow proper decoding at the receiver. The following budget has been used to allocate jitter to the indicated components that contribute to the total jitter on each link:

Component	Jitter (ns)
Transmitter skew	±10
Cable intersymbol interference	9
Cable reflections	8
Reflections due to receiver termination mismatch	5
Total	±32

The cable intersymbol interference and reflection allowances form the basis for the limit specified in 12.7.2.3; the reflection component is sufficient to allow a single 20 Ω impedance mismatch anywhere along a cable segment. The receiver-mismatch allowance is derived from the reflection attenuation specified in 12.5.3.2.4. The total forms the basis for the specification in 12.5.3.2.2.

The remainder of the jitter that can be tolerated by the Manchester decoder in a receiver is allocated to allow for distortion of the signal due to noise, receiver threshold offset, receiver skew, and receiver sampling timing error.

A simple clocked receiver/decoder with an 8 MHz sampling rate (the worst case allowed for in the design of this standard), can achieve proper decoding with up to ± 125 ns of jitter between two edges, which is equivalent to ±62.5 ns on each edge. Other receiver designs may tolerate more edge jitter. For example, a 6 MHz sampling rate would allow up to ±83.33 ns of jitter on each edge and a 16 MHz sampling rate allows up to ±93.75 ns of jitter.

It may be necessary to use a low-pass filter as part of the receiver to reduce the noise level seen by that receiver (see 12.7.4 for a description of the noise environment). A filter that reduces the noise may also have an effect on the amplitude and edge rate of the received signal. The filtered signal's edge rate near the zero-crossing is used in the critical translation from mV of noise and receiver offset into ns of jitter.

An example receiver design using an 8 MHz sampling rate and a 2 MHz Butterworth input filter might be based on the following jitter budget:

Component	Jitter (ns)
Input jitter (from above)	±32
Noise and receiver threshold offset	19.5
Receiver skew (analog)	4
Receiver skew (digital)	7
Total	±62.5

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The two primary contributors to noise in a 1BASE5 cable are self-crosstalk and impulse noise (see 12.7.4). Because it is unlikely that both will be present at their 1% worst-case levels on any particular cable, the required bit error ratio attributable to each source can be set at half of the one in 10^8 error ratio required by 12.5.3.2.6.

Crosstalk noise is specified to be no more than 105 mV (peak) through a 2 MHz filter (see 12.7.4.2). Because crosstalk is present for the entire transmission of a packet, some crosstalk will coincide with the most sensitive part of the received signal. Therefore, the receiver has to operate without error in the presence of this 105 mV of noise.

Impulse noise has a peak amplitude of 170 mV for ≤ 0.005 counts/s through the 2 MHz filter (see 12.7.4.1). This threshold does not directly correlate to jitter, however, because the derivation of the 62.5 ns jitter tolerance for an 8 MHz clock assumed worst-case sampling error. Assuming a random phasing of the sampling clock to the received signals, it can be shown that the 170 mV of noise is equivalent to a level of 85 mV with a worst-phase clock.

Jitter due to noise should be computed using the larger of the above two levels. The 105 mV for crosstalk noise, therefore, should be added to 50 mV for receiver threshold offset and the result should be divided by the edge rate of the filtered signal near the zero-crossing (7.9 mV/ns for the 2 MHz filter), yielding the 19.5 ns indicated above.

B.3 Example crosstalk computation for multiple disturbers, balanced-pair cable

A method for computing multiple-disturber, near end, crosstalk attenuation (MDNEXT) into each 1BASE5 pair is specified in 12.7.3.2. This annex provides example computations of MDNEXT using that method when only the distribution of X_{ij} is known.

The single-disturber probability distribution curve (labelled “1”) shown in Figure B–6 is based on actual measurement of 25-pair, 24-gauge, unshielded, twisted pair cable. The remaining probability distribution curves (labeled with the number of disturbing pairs) were computed using Monte Carlo simulation. To compute each sample $MDNEXT_j$ for N disturbers, N values of crosstalk attenuation (X_i) were chosen from the single-disturber distribution and N values of crosstalk phase (θ_i) were chosen from a uniform distribution between 0 and 2π rad. These values were then used with the following equations to compute $MDNEXT_j$:

$$H_j = \sum_{1 \le i \le N} 10^{(-X_i/20)} \cos\theta_i$$

$$V_j = \sum_{1 \le i \le N} 10^{(-X_i/20)} \sin\theta_i$$

$$MDNEXT_j = 10\log_{10}(H_j^2 + V_j^2)$$

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Iterating this process several hundred times, each time producing a single $MDNEXT_j$ sample, resulted in distributions for MDNEXT that are summarized in the following table and Figure B–6:

Disturbers	Iterations	MDNEXT: Mean (dB)	Std. Dev. (dB)	99% (dB)
1		61.2	7.0	48.6
2	500	57.2	6.2	46.4
3	500	55.1	5.8	45.2
6	500	52.0	5.7	42.5
13	1000	48.5	5.4	39.1
18	500	47.1	5.3	37.8
24	500	45.9	5.9	36.2

Because two pairs are used for each 1BASE5 connection, the entries in this table for 18 and 24 disturbers are not applicable for normal installation of 25-pair cables. Furthermore, telephone cables with larger numbers of pairs are often constructed using sub-bundles of 25 pairs each and so might yield similar results (for example, the curves for 13 or fewer disturbers would be the most applicable ones).

The calculation method of this annex, though not the numeric values, applies to 10BASE-T.

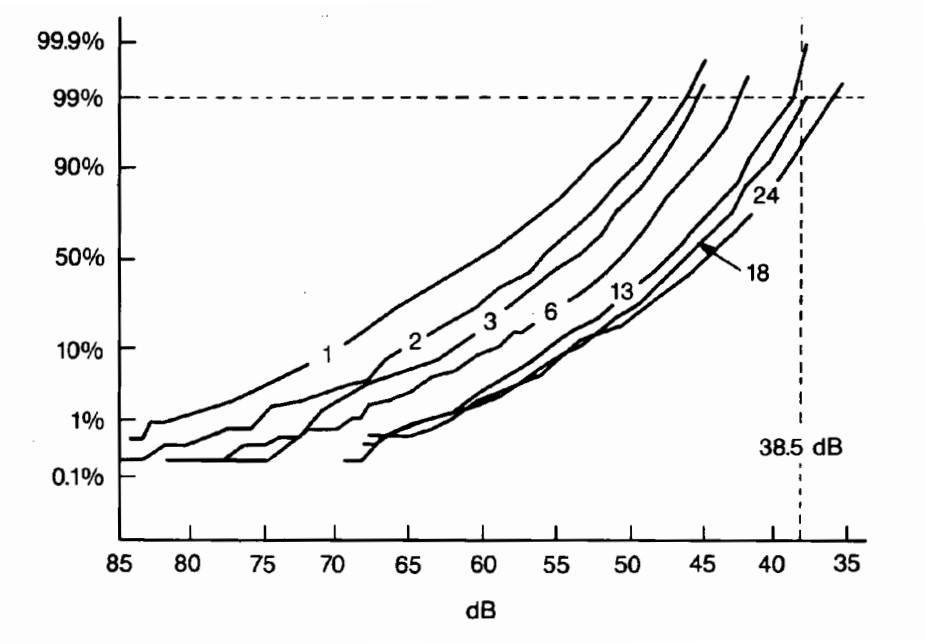

Figure B–6—MDNEXT cumulative probability distribution

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B.4 10BASE-T guidelines

B.4.1 System jitter budget

The jitter budget for 10BASE-T is apportioned as follows:

Jitter budget	Maximum-length twisted-pair link	Short-length twisted-pair link
	(jitter expressed in ±ns)	
Encoder	0.5	0.5
AUI cable including SNR (DO pair)	1.5	1.5
MAU transmitter	2.0	2.0
Twisted-pair medium with equalization	1.5	6.0
Noise jitter on twisted-pair medium	8.0	2.5
MAU receiver	1.5	1.5
AUI cable including SNR (DI pair)	1.5	1.5
Total	16.5	15.5

NOTE—Total transmit jitter for the combination of the MAU transmitter and link segment (14.3.1.2.3) is ±3.5 ns and ±8.0 ns for maximum- and short-length twisted-pair link segments, respectively. It is the sum of the entries for MAU transmitter and twisted-pair medium with equalization. The individual components cannot be easily observed on MAUs. Short-length segment is defined as a short, non-zero-length twisted-pair link. A short- rather than a zero-length segment is used in the calculation since a zero-length segment will have no significant noise and is a less severe case.

B.4.2 Filter characteristics

The implementation of the 3-pole, low-pass Butterworth filter should have the following characteristics:

3 dB cutoff frequency	15 MHz
Insertion loss (5 MHz to 10 MHz)	≤ 1.0 dB
30 MHz attenuation	≥17.5 dB
Input impedance (5 MHz to 10 MHz)	100 Ω
Return loss with 100 Ω load (5 MHz to 10 MHz)	≥20 dB

This filter is only used for the tests described in 14.3.1.3.2, 14.4.4.1, and 14.4.4.2. A buffer may be needed to achieve the above return loss when using an LC implementation of this filter.

B.4.3 Notes for conformance testing

The following notes are provided to assist in developing the conformance test.

B.4.3.1 Notes for 14.3.1.2.1 on differential output voltage

For testing harmonics measured on the TD circuit when the DO circuit is driven by an all-ones Manchester-encoded signal, it is acceptable to use a pattern of maximum length packets whose data field is all ones.

For testing of the maximum and minimum output signal to the template in Figure 14–10, the recommended measurement procedure is described as follows. An oscilloscope set for a zero voltage trigger with a positive slope is allowed to accumulate an eye pattern that has to be within the template. Acquisition has to be long

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enough to ensure that all data variations have been observed. When using packetized data, the TP_IDL and the first transmitted bit should be excluded from this measurement. Also, the interpacket interval may be adjusted so that transition-to-idle transient effects are excluded. When testing with the inverted template, the slope of the scope trigger should be negative.

B.4.3.2 Note for 14.3.1.2.2 on transmitter differential output impedance

The return loss (*RL*) is defined as follows:

$$RL = 20\log_{10}\frac{|Z_{\text{transmitter}} + Z_{\text{cable}}|}{|Z_{\text{transmitter}} - Z_{\text{cable}}|}$$

and also

$$RL = 20\log_{10}\frac{|V_{\text{i}}|}{|V_{\text{r}}|}$$

where

$Z_{\text{transmitter}}$ is the impedance of the transmitter
Z_{cable} is the impedance of the cable
V_{i} is the differential voltage incident upon the transmitter
V_{r} is the differential voltage reflected from the transmitter

a) A transmitter with a purely resistive source impedance of 96 Ω ± 20% will satisfy this requirement.
b) The requirement of 14.3.1.2.2 is equivalent to the following two constraints:
    1) The return loss when measured with an 85 Ω resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.
    2) The return loss when measured with a 111 Ω resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.

B.4.3.3 Note for 14.3.1.2.3 on output timing jitter

Adherence to the template of 14.3.1.2.1 with a jitterless source driving DO and the zero crossings constrained to 46.5 ns to 53.5 ns and 96.5 ns to 103.5 ns is sufficient to demonstrate compliance with the 3.5 ns jitter requirement. When measuring an integrated MAU, the zero crossing time interval should be constrained to 44.5 ns to 55.5 ns and 94.5 ns to 105.5 ns due to the additional allocation for encoder and AUI jitter. This test is simpler to perform than the test which follows, but failure of this test does not demonstrate noncompliance.

When triggering on one edge of the transmitted signal and observing another edge, the observed jitter measures the difference between the jitter of the triggering edge and the observed edge. When the two edges are separated such that the jitter of the edges is independent and clock drift is insignificant, the observed jitter is twice that of a single edge.

Therefore, a test that demonstrates compliance or noncompliance is as follows: Observe the zero crossings 8 BT and 8.5 BT from the triggering zero crossing while transmitting a pseudo-random data sequence of at least 511 bits. An external MAU with a jitterless source driving DO is compliant when all zero crossings fall within the time intervals 8.0 BT ± 7 ns and 8.5 BT ± 7 ns. An integrated MAU is compliant when all zero crossings fall within the time intervals 8.0 BT ± 11 ns and 8.5 BT ± 11 ns.

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When using packetized data, the TP_IDL and the first transmitted bit should be excluded from these measurements.

B.4.3.4 General note on common-mode tests

When performing tests specified as balanced or common-mode, the balance of the test equipment (such as matching resistors) has to exceed that required by the test.

B.4.3.5 Note for 14.3.1.3.4 on receiver differential input impedance

The return loss (*RL*) is defined as follows:

$$RL = 20\log_{10}\frac{\left|Z_{\text{receiver}} + Z_{\text{cable}}\right|}{\left|Z_{\text{receiver}} - Z_{\text{cable}}\right|}$$

and also

$$RL = 20\log_{10}\frac{\left|V_{\text{i}}\right|}{\left|V_{\text{r}}\right|}$$

where

Z_{receiver} is the impedance of the receiver
Z_{cable} is the impedance of the cable
V_{i} is the differential voltage incident upon the receiver
V_{r} is the differential voltage reflected from the receiver

a) A receiver with a resistive input impedance of 96 Ω ± 20% will satisfy this requirement.
b) The requirement of 14.3.1.3.4 is equivalent to the following two constraints:
    1) The return loss when measured with an 85 Ω resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.
    2) The return loss when measured with a 111 Ω resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.

B.4.3.6 Note for 14.3.1.3.3 on receiver idle input behavior

For conformance testing of receivers, the start of idle shall conform to the template shown in Figure 14–11. Additionally, the magnitude of the voltage-time integral of the undershoot (measured from the negative zero crossing that ends the positive idle pulse to the time when the differential signal settles to 0.0 mV ± 50 mV) shall be no greater than 1.2 times the voltage-time integral of the positive idle pulse (measured from the last positive zero crossing to the negative zero crossing).

B.4.3.7 Note for 14.3.1.3.5 on receiver common-mode rejection

For a stand-alone MAU, the receiver common-mode test may be performed with a jitterless E_s, so that the DI circuit should have no more than 4.0 ns of edge jitter.

For an integrated MAU, the common-mode test is performed with an E_s that has zero crossing jitter up to 11 ns from the ideal.

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B.5 10BASE-F

B.5.1 System jitter budget

The jitter budgets for 10BASE-FP, 10BASE-FB, and 10BASE-FL are apportioned as shown in Table B–2.

Table B–2—System jitter budgets

Encoder	10BASE-FP	10BASE-FB	10BASE-FL
Encoder	0.5	0.5	0.5
AUI Cable including SNR (DO Pair)	1.5	N/A	1.5
MAU DO Receiver (10BASE-FP only)	2.0	N/A	N/A
10BASE-FP total at retiming	4.0	N/A	N/A
Subtotal (10BASE-FP Retimes)	0.0	0.5	2.0
Transmitter*	2.0	4.0	4.5
Subtotal (at the MDI)	2.0	4.5	6.5
Fiber optic medium	0.0	0.0	0.0
10BASE-FP Passive Star	0.0	N/A	N/A
Fiber optic medium (10BASE-FP return)	0.0	N/A	N/A
Receiver**	1.0	2.0	8.5
10BASE-FP total at retiming	3.0	N/A	N/A
Subtotal (10BASE-FP Retimes)	0.0	6.5	15.0
Unallocated	8.5	10.0	0.0
MAU DI Transmitter (10BASE-FP only)	6.5	N/A	N/A
AUI cable incl-SNR (DI Pair)	1.5	N/A	1.5
Total	16.5 ns	16.5 ns	16.5 ns
*Includes jitter plus duty cycle distortion.			
** 10BASE-FL figure includes MAU DI Transmitter jitter allocation.			

B.5.2 10BASE-FP fiber optic segment loss budget

The 10BASE-FP MDI optical parameters specified in 15.2.1 and 15.2.2 have been selected to guarantee operation using a properly specified system of up to 500 m radius segment. This annex illustrates how the

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loss budget may be allocated to star, optical fiber, and patch panel connectors, including examples at 100 m and 500 m radius.

The allowed system attenuation values are determined by the average transmit and receive power ranges specified in Table 15–1. The average optical power launched into a 62.5 μm fiber has to be greater than –15 dBm and less than –11 dBm. (This includes any launch power variation and source degradation.) Receiver operation is specified for average received power greater than –41 dBm and less than –27 dBm. Thus the maximum attenuation allowed for optical plant, including star, is 26 dB, and the minimum allowed attenuation is 16 dB.

This attenuation can be allocated between the star, cabled optical fiber, and patch panel connectors in any manner as long as the maximum and minimum losses are within the limits stated in Table B–3. Note that the 10BASE-FP Star insertion loss includes the loss of one optical connector pair as specified in 16.5.2.1.

Table B–3—10BASE-FP fiber optic segment loss budget

Item	Min (dB)	Max (dB)
Star	16	20
Cabled optical fiber and connectors	0	6
Totals	16	26

Example 1: For a 500 m radius segment (1 km MDI to MDI) of 3.75 dB/km (measured at 850 nm) cabled optical fiber and a connector system with a maximum loss of 2 dB, the worst-case optical fiber and connector loss would be 5.75 dB. This would fall within the 6 dB limit, and result in a worst-case margin of 0.25 dB

Example 2: A horizontal structured building wiring system (e.g., as detailed in ANSI/TIA-568-C.0) of 100 m from the wiring closet to the desk top (100 m radius segment, 200 m MDI to MDI) of 3.75 dB/km optical fiber would have a loss of 0.75 dB. With four connector pairs in the path from MDI to MDI (wall plate, patch panel, patch panel, wall plate [see Figure 15–2]) and one connector pair at the 10BASE-FP Star (the other star connector pair is already included in the star loss [see 16.5.2.1)], and using a worst-case loss of 1 dB for each connector pair, the worst-case optical fiber and connector loss would be 5.75 dB. This would fall within the 6 dB limit, and would result in a worst-case margin of 0.25 dB.

In addition to these loss budgets, the overall system return loss has to be greater than 27 dB. The return loss is the ratio of the desired signal to all undesired, multiple reflected signals, observed at a 10BASE-FP MAU MDI. Use of connectors with less return loss than specified in 15.3.2.2 as well as use of more than two patch panels on each side of the star is permitted, as long as the overall system return loss requirement is met.

The 8.0 dB differential flux budget (16.3.4.2) can be allocated as shown in Table B–4.

Table B–4—Eight decibel differential flux budget

Contribution	(dB)
Variation at Star Input due to combined effects	4.8
1/2 star connector	0.5
Star including 1/2 connector	2.5
Wavelength in ORD leg	0.2
Total	8.0

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Each of these contributions to the differential budget is a measurable quantity. For example, the variation in the optical power at the star input due to combined effects of launch power, LED lifetime degradation, connectors, distance from 10BASE-FP MAU to Star, and wavelength of transmitter can be measured at the star input port. Also, star differential loss measurement is described in 16.5.2.2.

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Annex C

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State diagram, MAC sublayer

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Annex D

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Application context, selected medium specifications

D.1 Introduction

This annex provides general guidance, to both the design engineer and the eventual user of specific product implementations, on the particular clauses of this standard considered useful for different 10 Mb/s application environments. It is to be emphasized that the material in this annex is very general, as the standard specifications are intended to be relatively application-independent. Nevertheless, certain specifications may apply more to one application environment than another. What follows are brief descriptions of application environments and lists of those generic parameters of the Physical Layer specifications thought to be useful in relating a general set of user requirements to a specific standard specification and its related medium. *Once a basic relationship is identified, the reader is directed to a specific clause of the standard for detailed design specifications.*

D.2 Type 10BASE5 applications

One of the major arenas for local area networks is the interconnection of work stations throughout a large department or single building. The ability to handle all kinds of message traffic at relatively high data rates among a large set of work stations are typical characteristics of these environments. Usually the basic interconnection trunk cable is installed and left in place permanently or for extended periods while work station placement may shift from time to time. The Type 10BASE5 specification provides the primary baseband backbone for intraplant CSMA/CD interconnections. Clause 7 and Clause 8 of the standard provide detailed specifications for the Physical Layers associated with Type 10BASE5 environments. The generic Physical Layer parameters are as follows:

Maximum unrepeatered cable segment500 m
Maximum number of MAUs per segment100
Connector typeType N or coaxial “tap”
Breakdown voltage, MAU function250 V ac rms
MTBF1 million hours
Total Segment Resistance5 Ω
MAU separation2.5 m
Connection shunt capacitance4 pF
AUI functionalityDO, DI, CI, (CO optional)

D.3 Type 10BASE2 applications

Another major arena for local area networks is the interconnection of work stations throughout a small department or work area. The ability to handle all kinds of message traffic at relatively high data rates among a selected set of locally clustered work stations are the typical characteristics of these environments. In addition, the basic interconnection trunk cable is likely to be moved frequently by the local users of the equipment to suit evolving needs. The Type 10BASE2 specification provides an interconnection schema that complements the Type 10BASE5 backbone in a hierarchical manner for intradepartment or work area CSMA/CD interconnections. Clause 7 and Clause 10 of the standard provide detailed specifications for the

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Physical Layers associated with Type 10BASE2 environments. The generic Physical Layer parameters are as follows:

Maximum unrepeatered cable segment185 m
Maximum number of MAUs per segment30
Connector typeType BNC “T”
Breakdown voltage, MAU function500 V ac rms
MTBF100 000 hours
Total Segment Resistance10 Ω
MAU separation0.5 m
Connection shunt capacitance8 pF
AUI functionalityDO, DI, CI

D.4 Type FOIRL and 10BASE-F applications; alternative fiber optic medium applications

D.4.1 Alternative fiber types

Table D–1 provides a listing of other fiber types that may be used in an FOIRL or a 10BASE-F Cable Link Segment. These fiber types have not been studied, and details for their use are not provided for in the main body of the standard. Therefore, using these fiber types may reduce the maximum achievable distance.

Table D–1—Alternative fiber types

Nominal Core diameter (µm) IEC 60793-2:1992	Nominal cladding diameter (µm) IEC 60793-2:1992	Nominal Numerical aperture IEC 60793-2:1992
50	125	0.2
50	125	0.21
50	125	0.22
85	125	0.26
100	140	0.29

D.4.1.1 Theoretical coupling losses

The body of the standard references a single fiber type to facilitate interoperability and conformance testing; however, other fiber types may also be used. The use of an alternative fiber type with a particular implementation may have the following consequences. At the transmit MDI, more or less light may be launched into the fiber, depending on whether the optics are optimized for a core size and a numerical aperture (NA) that are smaller or larger than that of the alternative fiber size. At the receive MDI, the sensitivity may be increased or decreased depending on the optimization of the collecting optics. Table D–2 summarizes the potential effects of the use of alternative fiber sizes and provides the loss budget remaining for cable plant attenuation. All adjustments are relative to an implementation using the minimum diameter and NA 62.5 µm core fiber as specified in IEC 60793-2:1992, Type A1b, Category ≤ 3.5 dB/km. This cable plant has a loss budget of 9 dB for FOIRL segments and 12.5 dB for 10BASE-FL and 10BASE-FB link segments.

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The worst-case loss budget in Table D–2 is calculated on the assumption that the transmitter and receiver core diameter and NA are 62.5 µm and 0.275, respectively. Launching into a smaller core diameter or NA will incur a loss. Launching into a larger core diameter or NA will not result in a gain.

Similarly, receiving from a larger core diameter or NA incurs a loss, but receiving from smaller core diameter or NA provides no gain.

The values for transmit powers assume a worst-case condition that no additional power is launched into an increased core diameter and NA link fiber when referred to the 62.5 µm core fiber. This assumption is valid for underfilled launch conditions such as may occur from a MAU containing a pigtailed or laser emitter.

Table D–2—Worst-case loss budget

Fiber type	Transmit loss (dB)	Receive loss (dB)	Loss budget remaining (dB)	
			FOIRL	10BASE-FB/L
50 µm/NA=0.20	5.7	0	3.3	6.8
50 µm/NA=0.21	5.2	0	3.8	7.3
50 µm/NA=0.22	4.8	0	4.2	7.7
85 µm/NA=0.26	1.6	2.6	4.8	8.3
100 µm/NA=0.29	0.5	4.5	4.0	7.5

D.4.1.2 Maximum launch power

When large core diameter and NA launch conditions are used in conjunction with a launch fiber of larger core diameter and NA than the 62.5 µm reference, significantly greater launch power can occur. For example, this is typically the case with wide area surface emitter LED devices that are directly aligned with a fiber in a device mount header.

Table D–3 summarizes the maximum launch power into fibers with larger core diameters than 62.5 µm and the corresponding excess power that can result with a receiver utilizing all the optical power from the fiber.

Table D–3—Worst-case launch power

Fiber type	Maximum transmit power (dBm)	Maximum excess power (dBm)
85 µm/NA=0.26	–6.1	2.9
100 µm/NA=0.29	–3.8	5.2

In this case, sufficient attenuation should be installed in the link segment to ensure that for FOIRL segments the peak received optical power does not exceed –9 dBm, and for 10BASE-F segments the average received optical power does not exceed the appropriate optical Receive Average Power (Max) in Table 15–1.

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D.4.2 Type 10BASE-FP applications using 50/125 μm fiber

It is recognized that, in some cases, designers are constrained to use fiber sizes other than 62.5/125 μm in LAN designs. Such LAN designs are beyond the scope of this standard but can operate properly if optical power and loss budgets are adjusted to compensate for the different fiber characteristics. The following guidance is provided for system implementers who are constrained to design LANs with the 50/125 μm fiber described in D.4.1.

WARNING

Interoperability of nonconforming implementations cannot be ensured. It is the responsibility of the designer(s) of nonconforming implementation(s) to assure LAN operation. The following is only advisory information for implementations outside the scope of this standard.

D.4.2.1 Coupled transmit power

As shown in D.4.1, reduction of coupled power introduces the greatest difference between LANs using 62.5/125 μm and those using 50/125 μm fiber. Typically, for an emitter technology that produces a uniform, overfilled launch condition, this difference will be 3.5 dB. Implementers of 50/125 μm systems may choose to deal with this by trying one of the following alternatives:

a) Selecting an emitter technology with coupled power that is less susceptible to variation with fiber size, or
b) Increasing receiver sensitivity and dynamic range, or
c) Reducing the star coupler loss to compensate for the reduction in coupled transmit power. This may be accomplished by reducing the number of ports on the star coupler, or
d) Reducing the connector losses in the system, either by reducing the number of in-line connectors or reducing the loss per connector.

D.4.2.2 Star coupler loss

Also in accordance with D.4.1, the transmission loss of 50/125 μm star couplers may be as much as 1 dB greater than their 62.5/125 μm counterparts. Implementers of 50/125 μm systems may choose to deal with this by trying one of the following alternatives:

a) Procurement—specification of coupler loss characteristics to be the same as those shown for 62.5/125 μm star couplers, per 16.5, or
b) Compensation—all items shown in D.4.2.1 a) to d) may be used to compensate for an increase in coupler loss.

For example, a passive-star coupler (with connectors) with 33 ports typically has the following losses:

Contributor	Loss (dB)
Splitting	–15
Connector (1)	–1
Excess	0 to –4
Total	–16 to –20

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If, in a LAN that used 50/125 μm fiber, the maximum allowable number of ports per passive-star coupler was reduced to 17, the appropriate losses would be as follows:

Contributor	Loss (dB)
Splitting:	–12
Connector (1):	–1
Excess:	0 to –3
Total:	–13 to –16

The 3.5 dB lost to the MDI OTD would then be recovered allowing this "reduced nodes" LAN to still operate at the proposed maximum of 500 m MAU to the star.

It should be noted that the MAU parameters remain unchanged.

D.4.2.3 Collision detection

Reliable collision detection requires that designers of systems using nonconforming fiber optic cable ensure that the optical power levels of all possible colliding signals on the LAN differ at the mixing element (passive-star coupler) by no more than that specified in 16.3.4.2. This requires that
$10 \times \text{abs}\,(\log((P_{Ti} - L_{Ti} - U_{Ti})/(P_{Tj} - L_{Tj} - U_{Tj}))) \leq$ that specified in 16.3.4.2.

for all *i* not equal *j*, and

where

P_{Tn} is coupled optical transmit power, MAU *n*
L_{Tn} is optical cable and connector and transmit fiber loss, from MAU n to star input port *m*
U_{Tm} is input port uniformity, port *m*

D.5 10BASE-T use of cabling systems with a nominal differential characteristic impedance of 120 Ω

Clause 14 specifies the use of 100 Ω link segments. This subclause specifies the conditions for the use of cabling with a nominal characteristic impedance of 120 Ω by 10BASE-T conformant stations.

The use of cables with a characteristic impedance outside the range specified in 14.4.2.2 will generally increase the mismatching effects in the link components, inducing additional jitter in the received signal.

In particular, the use of a homogeneous link segment having a characteristic impedance of 120 Ω ± 15 Ω over the frequency band 1 to 16 MHz may add from 0.15 ns (maximum-length segment) up to 0.63 ns (short-length segment) of additional jitter to the signal at the input of the receiver.

Consequently, in order to keep the overall jitter budget at the same value as for a 100 Ω link segment when using a 120 Ω link segment, the following modifications to the specifications of 14.4 apply:

a) The maximum medium timing jitter specified in 14.4.2.3 for a simplex link segment is increased from 5 ns to 5.5 ns.

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b) The NEXT loss values specified in 14.4.3 are increased by 3 dB, i.e., the applicable formulas are replaced by the following:
   1) in 14.4.3.1.1 for 25-pair cables/binder groups: $33–15 \log_{10}(f/10)$ dB.
   2) in 14.4.3.1.2 for 4-pair cables: $29–15 \log_{10}(f/10)$ dB.
   3) in 14.4.3.2 for MDNEXT: $26–15 \log_{10}(f/10)$ dB.

NOTE—In addition to the case of 120 Ω homogeneous link segments, the above figures encompass the case where 100 Ω terminal cords are used in conjunction with 120 Ω premises cabling. This configuration results in adding up to 0.5 ns of jitter for a maximum-length segment (instead of 0.15 ns) and up to 1.3 ns for a short-length segment (instead of 0.63 ns).

The use of 100 Ω cords at any intermediate cross-connects on 120 Ω links as well as the use of cords with a characteristic impedance of 120 Ω ± 15 Ω in conjunction with 100 Ω ±15 Ω premises cabling is not allowed since it would result in worst-case jitter greater than that allowed in the standard.

D.6 10BASE-T use of cabling systems with a nominal differential characteristic impedance of 150 Ω

This subclause outlines the philosophy and methodology for allowing 10BASE-T stations to support transmission on 150 Ω balanced STP cabling, as specified by ISO/IEC 11801:1995, Clause 8, with the use of impedance matching transformers.

The 10BASE-T specification was designed to support Manchester signaling over a link segment consisting of 100 Ω cabling system. The MAU link interface specifications were designed to ensure that jitter due to impedance discontinuities were minimized as specified in 14.4.2.3. In theory and in practice, a 150 Ω cabling system may be used to provide the link segment function provided the proper impedance match (100 Ω) with the MAU over the frequency range of interest as specified in 14.4, and the resultant transmission characteristics of the cabling system used to provide the link segment function meet or exceed those specified in 14.4. Therefore, to ensure the jitter specification of 14.4.2.3 and the jitter budget of B.4.1 are met, the following approach is recommended when using 150 Ω balanced STP cabling (as specified in ISO/IEC 11801:1995):

a) The 150 Ω section included in the link segment shown in Figure D–1 meets the specifications of ISO/IEC 11801:1995, 7.2.

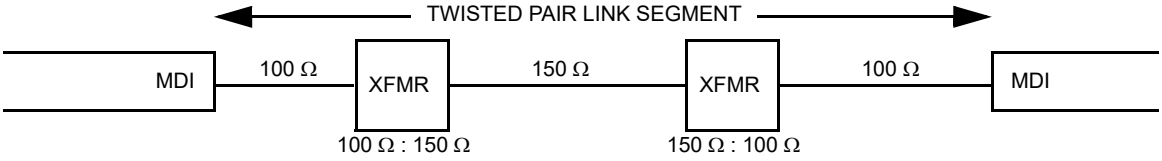

Figure D–1—Link segment incorporating 150 Ω cable section

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b) The link segment, including impedance matching transformers as shown in Figure D–2, meets all applicable specifications of 14.4.

c) A link test point is shown in Figure D–2. The transformers shown are the same as the ones shown in Figure D–1. The attaching cables between the MAU and the link test point should be the minimum required to attach the components. As tested in this configuration, the MAU transmitter requirements meet all applicable requirements for the MAU as specified in Clause 14, except for signal levels which may be up to 1.0 dB lower than that specified there.

NOTE—This 1.0 dB (0.5 dB per transformer) effectively requires the attenuation of the 150 Ω cable section of the twisted-pair link segment (see Figure D–1) to be less than or equal to 10.5 dB in order to meet the requirements of 14.4.2.

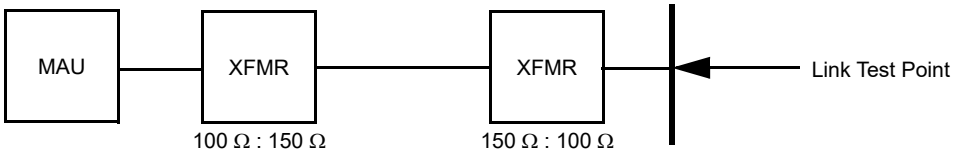

Figure D–2—Link test point for 150 Ω cabling

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Annex E

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Receiver wavelength design considerations (FOIRL)

NOTE—This annex relates to a clause that is not recommended for new installations. This annex is not recommended for new installations. Since March 2012, maintenance changes are no longer being considered for this annex.

The center wavelength of the optical source emission is specified in 9.9.4.1.1 to be between 790 nm and 860 nm. Although these limits are acceptable, it is currently recognized, through the examination of manufacturers' current data, that greater choices of emitters can be obtained by extending the allowable wavelength to 910 nm.

An upper limit of 910 nm allows the selection of devices nominally centered at a lower wavelength, for example, 880 nm. This allows a tolerance for manufacturing variations, for example, ±20 nm, and a tolerance for an operating temperature range (typically, 0.3 nm/°C).

It is anticipated that future fiber optic applications including Local Area Networks will use the 910 nm upper limit for first window systems. It is therefore recommended that implementers specify receiver sensitivity over a center wavelength range from 790 nm to 910 nm.

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Annex F

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Additional attributes required for systems

F.1 Introduction

During the development of Repeater Management, some attributes and operations were identified as items that were necessary to fill out the management of a complete intermediate system such as a repeater. These items are generic in the sense that they are required for managed systems in general. They are not normally specified as attributes of the lower layers. In repeater management, the entire system is at the lowest layers so there is no other group to turn to for systems management. The following items are defined to aid in the completeness of this standard, although it is recognized that they are outside the bounds of the definition area for a layer1/2 device.

F.1.1 Scope

This annex defines additional managed objects and attributes that have been identified by the IEEE 802.3 Repeater Management Task Force as being necessary to the management of an IEEE 802.3 repeater. These objects and attributes, while necessary to the management of an IEEE 802.3 repeater, are not specifically related to the CSMA/CD access method or to Clause 9 repeaters; rather, they are objects and attributes that are appropriate for any managed system.

This annex does not necessarily define the complete set of generic objects and attributes required to support a managed system. It contains only those objects and attributes that were identified in the process of developing the repeater management standard and were identified as not being uniquely appropriate to a CSMA/CD layer management standard.

When a generic systems management standard is available that is appropriate for managed systems of the complexity of a repeater, it is expected that this portion of the standard will no longer be appropriate and will be deprecated.

F.2 Objects/Attributes/Actions/Notifications

F.2.1 TimeSinceSystemReset attribute

aTimeSinceSystemReset **ATTRIBUTE**
DERIVED FROM AttributeModule.ResettableCounter32;
BEHAVIOUR bTimeSinceSystemReset;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) sysResetTime(47)};

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bTimeSinceSystemReset **BEHAVIOUR**
DEFINED AS The time in tens of milliseconds since the last time that the system including network management was reset. This may have been caused by ResetSystemAction or other means. This counter has a value of 0 when initialized.

Though the count is reported in tens of milliseconds, the required resolution is to the nearest 100 ms. The clocking source for the counter shall be accurate to within 1% throughout the full counting range.;

NOTE—The approximate minimum time for counter rollover is 497 days.

F.2.2 RepeaterResetTimeStamp attribute

aRepeaterResetTimeStamp **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX AttributeModule.Integer32;
BEHAVIOUR bRepeaterResetTimeStamp;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) repeaterResetTimeStamp(48)};

bRepeaterResetTimeStamp **BEHAVIOUR**
DEFINED AS Not a counter, this attribute provides the value of aTimeSinceSystemReset when the repeater was last reset. This value is recorded whenever the repeater enters the START state of Figure 9–2 in the 802.3 repeater standard. This value may never be greater than aTimeSinceSystemReset.;

F.2.3 ResetSystemAction action

acResetSystemAction **ACTION**
BEHAVIOUR acResetSystem;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) action(9) resetSystem(49)};

acResetSystem **BEHAVIOUR**
DEFINED AS This action initializes the resettable management counters of the system and also of all contained objects. The value of non-resettable counters may change as a result of this action.;

NOTE—This action may result in the loss of packets.

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Annex G

(normative)

Additional material required for conformance testing

NOTE—This annex relates to a clause that has been deprecated. Since March 2012, maintenance changes are no longer being considered for this annex.

G.1 Introduction

This material was generated during the development of Clause 19. It was felt that it was required to support the development of conformance test material that was not included in the charter of the development of the original repeater management standard.

G.1.1 Material in support of the aDataRateMismatches attribute

A vendor submitting equipment for conformance testing under Clause 19 shall provide minimum frequency difference data (two values) such that a test can be done for exertion and another test can be done for non-exertion of the aDataRateMismatch attribute (see 19.2.6.2).

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Annex H

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GDMO specifications for CSMA/CD managed objects

NOTE—GDMO specifications were moved to Annex B of IEEE Std 802.3.1-2011 and removed from this annex in IEEE Std 802.3-2012.

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Annex J

(normative)

Electrical isolation and general safety

The requirements specified in this annex are to be used in conjunction with the requirements in the clause that specifies the interface(s) under consideration.

J.1 Electrical isolation

Electrical isolation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz. This test voltage amplitude is raised from zero to the prescribed voltage and held at that value for 60 s.

b) 2250 V dc. This test voltage is raised from zero to the prescribed voltage and held at that value for 60 s.

c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses is 1.2/50 (1.2 μs virtual front time, 50 μs virtual time to half value), such as one produced by a 1.2/50-8/20 combination wave generator, as defined in ITU-T Recommendation K.44.

NOTE 1—If the MDI is also a Clause 33 or Clause 145 PI then see 33.4.1 or 145.4.1 for specific requirements associated with option c).

There shall be no insulation breakdown during the test. Insulation breakdown is considered to have occurred when the current that flows as a result of the application of the test voltage rapidly increases in an uncontrolled manner; that is, the insulation does not restrict the flow of the current. Corona discharge is not regarded as insulation breakdown. The resistance after the test shall be at least 2 MΩ, measured at 500 V dc.

NOTE 2—IEEE Std 802.3-2018 and previous revisions provided references to various editions of the IEC 60950-1 standard for guidance in performing the isolation test for options a) and b). IEC 60950-1 has been withdrawn. References to IEC standards are not essential to performing the isolation test specified in J.1. No technical change is implied by the removal of these references.

NOTE 3—Implementers should consider the effect of whether other ports are terminated or unterminated when testing the insulation of multi-port devices.

J.2 General safety

Equipment shall comply with all applicable local, state, national and application-specific standards, such as the applicable sections of IEC 62368-1:2018.

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J.3 Protocol implementation conformance statement (PICS) proforma for Annex J, Electrical isolation and general safety[270]

J.3.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex J, Electrical isolation and general safety, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

J.3.2 Identification

J.3.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

J.3.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex J, Electrical isolation and general safety
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[270]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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J.3.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*ISO	Electrical isolation	J.1		O	Yes [ ] No [ ]
*SAF	General safety	J.2		O	Yes [ ] No [ ]

J.3.4 PICS proforma tables for electrical isolation and general safety

J.3.4.1 Electrical isolation

Item	Feature	Subclause	Value/Comment	Status	Support
ISO1	Electrical isolation test a) performed	J.1	J.1 item a)	ISO:O.1	Yes [ ] No [ ] N/A [ ]
ISO2	Electrical isolation test b) performed	J.1	J.1 item b)	ISO:O.1	Yes [ ] No [ ] N/A [ ]
ISO3	Electrical isolation test c) performed	J.1	J.1 item c)	ISO:O.1	Yes [ ] No [ ] N/A [ ]
ISO4	Insulation breakdown after test	J.1	>2 MΩ, measured at 500 V dc	ISO:M	Yes [ ] N/A [ ]

J.3.4.2 General safety

Item	Feature	Subclause	Value/Comment	Status	Support
SAF1	Conformance to safety specifications	J.2	IEC 62368-1:2018, where applicable	SAF:M	Yes [ ] N/A [ ]

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Annex K

(informative)

Optional alternative terminology for “master” and “slave”

The IEEE 802.3 Ethernet standard uses the terms “master” and “slave” to assign roles, for example to define timing roles for certain PHYs. These terms, even while used strictly in a technical context, still have widely held negative social connotations. Because of this, some organizations with an interest in IEEE 802.3 Ethernet have policies, or are considering policies, to discontinue the use of the master-slave terminology and replace it with other terms that have less negative social connotations.

If alternative terms for “master” and “slave” are used in implementations, then the following substitutions are recommended:

In place of “master”, the term “leader” should be used. In place of the term “slave”, the term “follower” should be used. For example, “MASTER PHY” would be replaced with “LEADER PHY”. This includes the use of “master” or “slave” as part of a compound term. For example, “slave_transition_counter” would be replaced with “follower_transition_counter”.

When translating into languages other than English, synonyms may be selected for “leader” and “follower” to avoid widely held negative social connotations.

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NOTE—This annex is numbered in correspondence to its associated clause; i.e., Annex 4A corresponds to Clause 4.

Annex 4A

(normative)

Simplified full duplex media access control

This annex is based on the Clause 4 MAC, with simplifications for use in networks that do not require the half duplex operational mode. Additional functionality is included for managing Physical Layer congestion and for support of interframe spacing outside this sublayer. This annex stands alone and does not rely on information within Clause 4 to be implemented.

4A.1 Functional model of the MAC method

4A.1.1 Overview

The architectural model described in Clause 1 is used in this clause to provide a functional description of the LAN full duplex MAC sublayer.

The MAC sublayer defines a medium-independent facility, built on the medium-dependent physical facility provided by the Physical Layer, and under the access-layer-independent LAN LLC sublayer (or other MAC client). It is applicable to a general class of media suitable for use with the full duplex media access discipline.

The LLC sublayer and the MAC sublayer together are intended to have the same function as that described in the OSI model for the Data Link Layer alone. The partitioning of functions presented in this standard requires two main functions generally associated with a data link control procedure to be performed in the MAC sublayer. They are as follows:

a) Data encapsulation (transmit and receive)
    1) Framing (frame boundary delimitation, frame synchronization)
    2) Addressing (handling of source and destination addresses)
    3) Error detection (detection of physical medium transmission errors)
b) Media access management (Physical Layer congestion)

This MAC does not support the *half duplex* mode of operation so there is no need for collision detection or handling. However, this MAC does have the ability to avoid congestion within the Physical Layer. Therefore, Media Access Management comprises the transmission of bits to the Physical Layer and optionally delaying any transmission for an interframe gap or for a longer period of time based on congestion within the Physical Layer.

An optional MAC control sublayer, architecturally positioned between LLC (or other MAC client) and the MAC, is specified in Clause 31 and Clause 64. This MAC Control sublayer is transparent to both the underlying MAC and its client (typically LLC). The MAC sublayer operates independently of its client; i.e., it is unaware whether the client is LLC or the MAC Control sublayer. This allows the MAC to be specified and implemented in one manner, whether or not the MAC Control sublayer is implemented. References to LLC as the MAC client in text and figures apply equally to the MAC Control sublayer, if implemented.

The remainder of this clause provides a functional model of this MAC method.

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4A.1.2 Full duplex operation

This subclause provides an overview of frame transmission and reception in terms of the functional model of the architecture. This overview is descriptive, rather than definitional; the formal specifications of the operations described here are given in 4A.2 and 4A.3. Specific implementations for full duplex mechanisms that meet this standard are given in 4A.4. Figure 1–1 provides the architectural model described functionally in the subclauses that follow.

The Physical Layer Signaling (PLS) component of the Physical Layer provides an interface to the MAC sublayer for the serial transmission of bits onto the physical media. For completeness, in the operational description that follows some of these functions are included as descriptive material. The concise specification of these functions is given in 4A.2 for the MAC functions and in Clause 7 for PLS.

Transmit frame operations are independent from receive frame operations and respond to different signals from the Physical Layer. The carrierSense signal indicates that the transmit function has to defer because of congestion at the Physical Layer (see 4A.2.3.2.1). The receiveDataValid signal indicates the presence of incoming data to the receive function (see 4A.2.4.2).

4A.1.2.1 Transmission

When a MAC client requests the transmission of a frame, the Transmit Data Encapsulation component of the full duplex MAC sublayer constructs the frame from the client-supplied data. It prepends a preamble and a Start Frame Delimiter to the beginning of the frame. Using information provided by the client, the MAC sublayer also appends a Pad at the end of the MAC information field of sufficient length to ensure that the transmitted frame length satisfies a minimum frame-size requirement (see 4A.2.3.2.4). It also prepends destination and source addresses, the length/type field, and appends a frame check sequence to provide for error detection. If the MAC supports the use of client-supplied frame check sequence values, then it shall use the client-supplied value, when present. If the use of client-supplied frame check sequence values is not supported, or if the client-supplied frame check sequence value is not present, then the MAC shall compute this value. Frame transmission may be initiated once the carrierSense signal has been removed and after the interframe delay, regardless of the presence of receive activity.

The Physical Layer performs the task of generating the signals on the medium that represent the bits of the frame. Once the Physical Layer has indicated its readiness to transmit another frame by removing the carrierSense signal, it shall accept a complete frame from the MAC layer. A functional description of the Physical Layer is given in Clause 7 and beyond.

When transmission has completed, the MAC sublayer so informs the MAC client and awaits the next request for frame transmission.

4A.1.2.2 Reception

At each receiving station, the arrival of a frame is first detected by the Physical Layer, which responds by synchronizing with the incoming preamble, and by turning on the receiveDataValid signal. As the encoded bits arrive from the medium, they are decoded and translated back into binary data. The Physical Layer passes subsequent bits up to the MAC sublayer, where the leading bits are discarded, up to and including the end of the preamble and Start Frame Delimiter.

Meanwhile, the Receive Media Access Management component of the MAC sublayer, having observed receiveDataValid, has been waiting for the incoming bits to be delivered. Receive Media Access Management collects bits from the Physical Layer entity as long as the receiveDataValid signal remains on. When the receiveDataValid signal is removed, the frame is truncated to an octet boundary, if necessary, and passed to Receive Data Decapsulation for processing.

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Receive Data Decapsulation checks the frame's Destination Address field to decide whether the frame should be received by this station. If so, it passes the Destination Address (DA), the Source Address (SA), the Length/Type, the Data, and (optionally) the Frame Check Sequence (FCS) fields to the MAC client, along with an appropriate status code, as defined in 4A.3.2. It also checks for invalid MAC frames by inspecting the FCS to detect any damage to the frame enroute, and by checking for proper octet-boundary alignment of the end of the frame. Frames with a valid FCS may also be checked for proper octet-boundary alignment.

4A.1.3 Relationships to the MAC client and Physical Layers

The MAC sublayer provides services to the MAC client required for the transmission and reception of frames. Access to these services is specified in 4A.3. The MAC sublayer makes a best effort to transfer a serial stream of bits to the Physical Layer. Although certain errors are reported to the client, error recovery is not provided by MAC. Error recovery may be provided by the MAC client or higher (sub)layers.

4A.2 Media access control (MAC) method: precise specification

4A.2.1 Introduction

A precise algorithmic definition is given in this subclause, providing a procedural model for the MAC process with a program in the computer language Pascal. See references [B9] and [B17] for resource material. Note whenever there is any apparent ambiguity concerning the definition of some aspect of the MAC method, it is the Pascal procedural specification in 4A.2.7 through 4A.2.10 that should be consulted for the definitive statement. Subclauses 4A.2.2 through 4A.2.6 provide, in prose, a description of the access mechanism with the formal terminology to be used in the remaining subclauses.

4A.2.2 Overview of the procedural model

The functions of the MAC method are presented below, modeled as a program written in the computer language Pascal. This procedural model is intended as the primary specification of the functions to be provided in any MAC sublayer implementation. It is important to distinguish, however, between the model and a real implementation. The model is optimized for simplicity and clarity of presentation, while any realistic implementation shall place heavier emphasis on such constraints as efficiency and suitability to a particular implementation technology or computer architecture. In this context, several important properties of the procedural model shall be considered.

4A.2.2.1 Ground rules for the procedural model

a) First, it shall be emphasized that *the description of the MAC sublayer in a computer language is in no way intended to imply that procedures shall be implemented as a program executed by a computer.* The implementation may consist of any appropriate technology including hardware, firmware, software, or any combination.
b) Similarly, it shall be emphasized that it is the behavior of any MAC sublayer implementations that shall match the standard, not their internal structure. The internal details of the procedural model are useful only to the extent that they help specify that behavior clearly and precisely.
c) The handling of incoming and outgoing frames is rather stylized in the procedural model, in the sense that frames are handled as single entities by most of the MAC sublayer and are only serialized for presentation to the Physical Layer. In reality, many implementations will instead handle frames serially on a bit, octet or word basis. This approach has not been reflected in the procedural model, since this only complicates the description of the functions without changing them in any way.
d) The model consists of algorithms designed to be executed by a number of concurrent processes; these algorithms collectively implement the MAC procedure. The timing dependencies introduced by the need for concurrent activity are resolved in two ways:

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1) *Processes Versus External Events.* It is assumed that the algorithms are executed "very fast" relative to external events, in the sense that a process never falls behind in its work and fails to respond to an external event in a timely manner. For example, when a frame is to be received, it is assumed that the Media Access procedure ReceiveFrame is always called well before the frame in question has started to arrive.
2) *Processes Versus Processes.* Among processes, no assumptions are made about relative speeds of execution. This means that each interaction between two processes shall be structured to work correctly independent of their respective speeds. Note, however, that the timing of interactions among processes is often, in part, an indirect reflection of the timing of external events, in which case appropriate timing assumptions may still be made.

It is intended that the concurrency in the model reflect the parallelism intrinsic to the task of implementing the MAC client and MAC procedures, although the actual parallel structure of the implementations is likely to vary.

4A.2.2.2 Use of Pascal in the procedural model

Several observations need to be made regarding the method with which Pascal is used for the model. Some of these observations are as follows:

a) The following limitations of the language have been circumvented to simplify the specification:
   1) The elements of the program (variables and procedures, for example) are presented in logical groupings, in top-down order. Certain Pascal ordering restrictions have thus been circumvented to improve readability.
   2) The *process* and *cycle* constructs of Concurrent Pascal, a Pascal derivative, have been introduced to indicate the sites of autonomous concurrent activity. As used here, a process is simply a parameterless procedure that begins execution at "the beginning of time" rather than being invoked by a procedure call. A cycle statement represents the main body of a process and is executed repeatedly forever.
   3) The lack of variable array bounds in the language has been circumvented by treating frames as if they are always of a single fixed size (which is never actually specified). The size of a frame depends on the size of its data field, hence the value of the "pseudo-constant" frameSize should be thought of as varying in the long term, even though it is fixed for any given frame.
   4) The use of a variant record to represent a frame (as fields and as bits) follows the spirit but not the letter of the Pascal Report, since it allows the underlying representation to be viewed as two different data types.
b) The model makes no use of any explicit interprocess synchronization primitives. Instead, all interprocess interaction is done by way of carefully stylized manipulation of shared variables. For example, some variables are set by only one process and inspected by another process in such a manner that the net result is independent of their execution speeds. While such techniques are not generally suitable for the construction of large concurrent programs, they simplify the model and more nearly resemble the methods appropriate to the most likely implementation technologies (microcode, hardware state machines, etc.)

4A.2.2.3 Organization of the procedural model

The procedural model used here is based on five cooperating concurrent processes. The Frame Transmitter process and the Frame Receiver process are provided by the clients of the MAC sublayer (which may include the LLC sublayer) and make use of the interface operations provided by the MAC sublayer. The other three processes are defined to reside in the MAC sublayer. The five processes are as follows:

a) Frame Transmitter process
b) Frame Receiver process
c) Bit Transmitter process
d) Bit Receiver process
e) Deference process

This organization of the model is illustrated in Figure 4A–1 and reflects the fact that the communication of entire frames is initiated by the client of the MAC sublayer, while the timing of individual bit transfers is based on interactions between the MAC sublayer and the Physical-Layer-dependent bit time.

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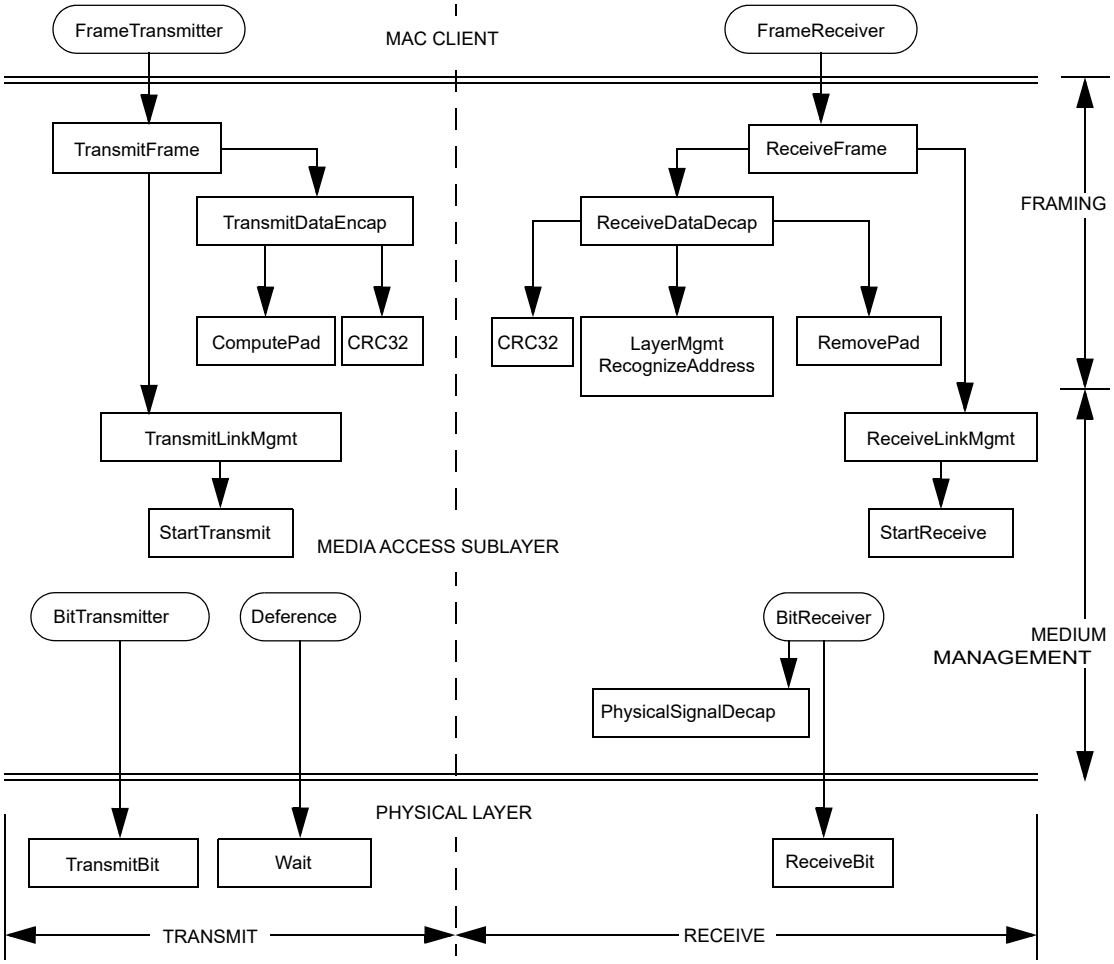

Figure 4A–1—Relationship among MAC procedures

Figure 4A–1 depicts the static structure of the procedural model, showing how the various processes and procedures interact by invoking each other. Figure 4A–2a, Figure 4A–2b, and Figure 4A–2c summarize the dynamic behavior of the model during transmission and reception, focusing on the steps that shall be performed, rather than the procedural structure that performs them. The usage of the shared state variables is not depicted in the figures, but is described in the comments and prose in the following subclauses.

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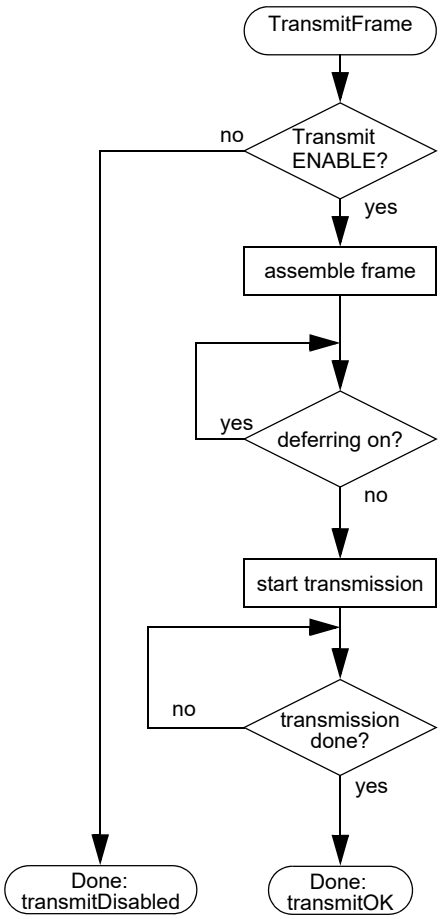

a) TransmitFrame

Figure 4A–2a—Control flow summary

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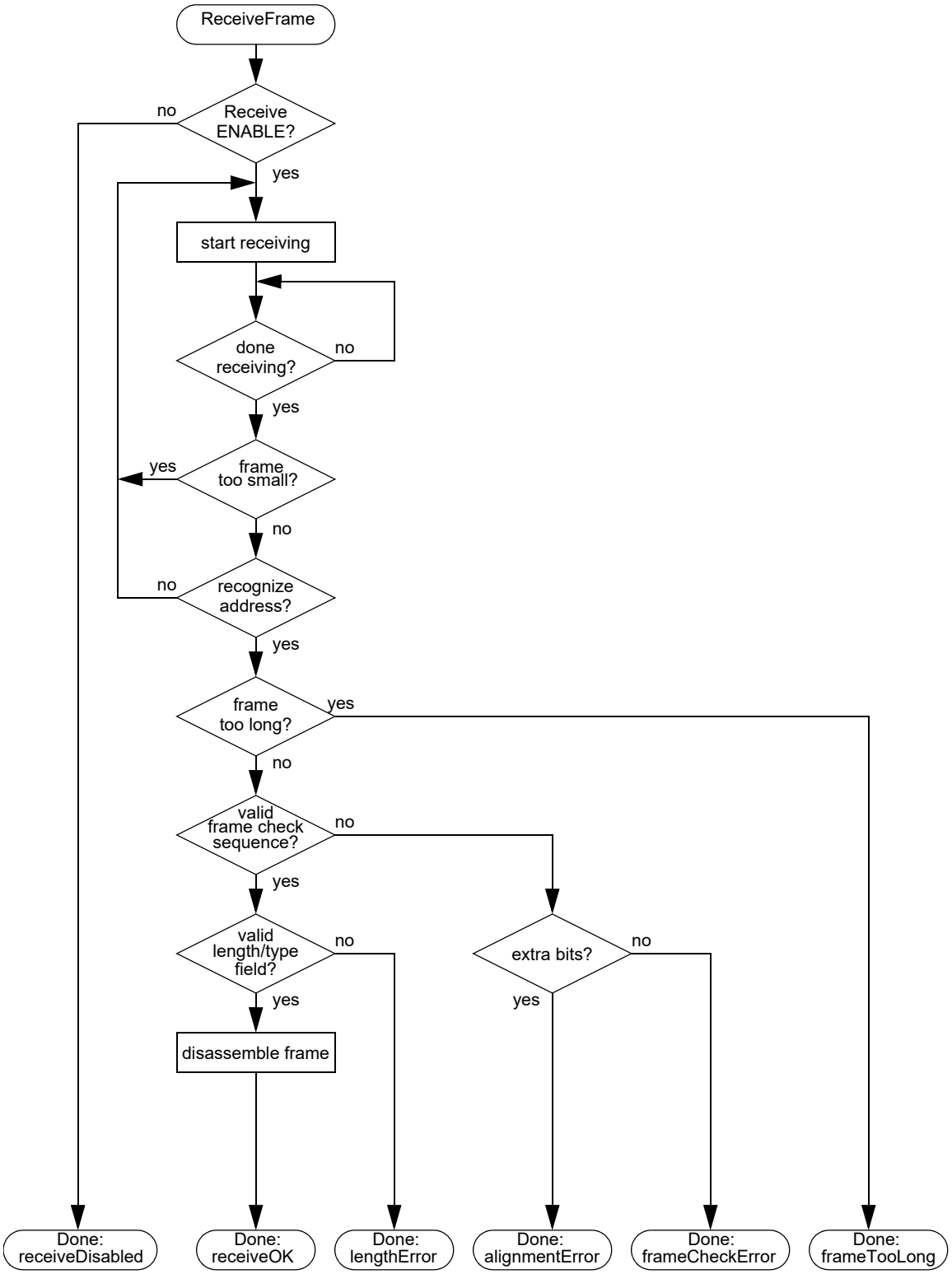

b) ReceiveFrame

Figure 4A–2b—Control flow summary

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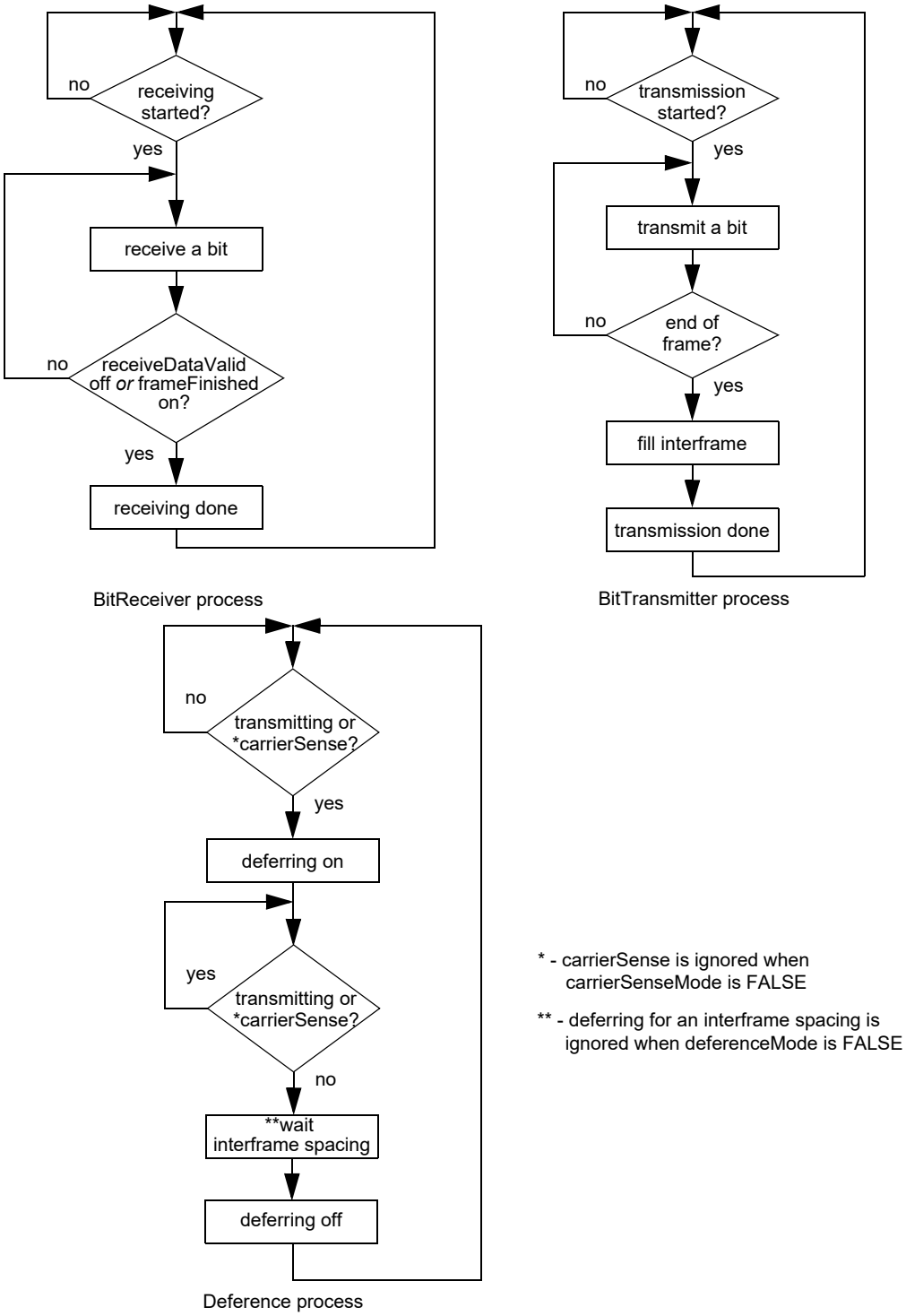

c) MAC sublayer

Figure 4A–2c—Control flow

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4A.2.2.4 Layer management extensions to procedural model

In order to incorporate network management functions, this Procedural Model has been expanded. Network management functions have been incorporated in two ways. First, 4A.2.7–4A.2.10, 4A.3.2, Figure 4A–2a, and Figure 4A–2b have been modified and expanded to provide management services. Second, Layer Management procedures have been added as 5.2.4. The Pascal variables are shared between Annex 4A and Clause 5.

The Pascal procedural specification shall be consulted for the definitive statement when there is any apparent ambiguity concerning the definition of some aspect of the MAC access method.

The Layer Management facilities provided by the MAC and Physical Layer management definitions provide the ability to manipulate management counters and initiate actions within the layers. The managed objects within this standard are defined as sets of attributes, actions, notifications, and behaviours in accordance with IEEE Std 802.1F-1993, and ISO/IEC International Standards for network management.

4A.2.3 Packet transmission model

Packet transmission includes data encapsulation and Media Access management aspects:

a) Transmit Data Encapsulation includes the assembly of the outgoing packet (from the values provided by the MAC client) and frame check sequence generation.
b) Transmit Media Access Management includes carrier deference, interpacket gap and bit transmission.

4A.2.3.1 Transmit data encapsulation

The fields of the MAC frame are set to the values provided by the MAC client as arguments to the TransmitFrame operation (see 4A.3) with the following possible exceptions: the padding field and the frame check sequence. The padding field is necessary to enforce the minimum frame size. The frame check sequence field may be (optionally) provided as an argument to the MAC sublayer. It is optional for a MAC to support the provision of the frame check sequence in such an argument. If this field is provided by the MAC client, the padding field shall also be provided by the MAC client, if necessary. If this field is not provided by the MAC client, or if the MAC does not support the provision of the frame check sequence as an external argument, it is set to the CRC value as generated by the MAC sublayer, after appending the padding field, if necessary.

4A.2.3.2 Transmit media access management

4A.2.3.2.1 Deference

When a packet is submitted by the MAC client for transmission, the transmission is initiated as soon as possible, but in conformance with the following rules. The variable carrierSense is ignored in process Deference when the variable carrierSenseMode is FALSE.

The MAC sublayer monitors the transmitting variable, which indicates the MAC is transmitting data to the Physical Layer, as well as the carrierSense signal provided by the PLS, which indicates the Physical Layer is not ready for the next frame. When either transmitting or carrierSense is true, the MAC delays any pending transmission. When both are false, the MAC continues to defer for a proper interPacketGap (see 4A.2.3.2.2).

If, at the end of the interPacketGap, a packet is waiting to be transmitted, transmission is initiated. When transmission has completed (or immediately, if there was nothing to transmit) the MAC sublayer resumes its original monitoring of transmitting and carrierSense.

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4A.2.3.2.2 Interpacket gap

As defined in 4A.2.3.2.1, the rules for deferring ensure a minimum interpacket spacing of interPacketGap bit times. This is intended to provide interframe recovery time to aid in packet delineation on the physical medium.

Note that interPacketGap is the minimum value of the interpacket gap. If necessary for implementation reasons, a transmitting sublayer may use a larger value with a resulting decrease in its throughput. The larger value is determined by the parameters of the implementation, see 4A.4.

4A.2.3.2.3 Transmission

Transmissions may be initiated whenever the station has a frame queued, subject only to the Physical Layer congestion and interframe spacing required to allow recovery for the physical medium. In certain implementations, interframe spacing is accomplished outside this layer. These implementations are allowed to ignore the deference process and always initiate transmissions immediately, subject only to conditions enforced outside this sublayer.

4A.2.3.2.4 Minimum frame size

The MAC requires that a minimum frame length of minFrameSize bits be transmitted. If frameSize is less than minFrameSize, then the MAC sublayer shall append extra bits in units of octets (pad), after the end of the MAC client data field but prior to calculating, and appending, the FCS (if not provided by the MAC client). The number of extra bits shall be sufficient to ensure that the frame, from the DA field through the FCS field inclusive, is at least minFrameSize bits. If the FCS is (optionally) provided by the MAC client, the pad shall also be provided by the MAC client. The content of the pad is unspecified.

4A.2.4 Frame reception model

The MAC sublayer frame reception includes both data decapsulation and Media Access management aspects:

a) Receive data decapsulation comprises address recognition, frame check sequence validation, and frame disassembly to pass the fields of the received frame to the MAC client.

b) Receive media access management comprises recognition of collision fragments from incoming frames and truncation of frames to octet boundaries.

4A.2.4.1 Receive data decapsulation

4A.2.4.1.1 Address recognition

The MAC sublayer is capable of recognizing individual and group addresses.

a) *Individual Addresses.* The MAC sublayer recognizes and accepts any frame whose DA field contains the individual address of the station.

b) *Group Addresses.* The MAC sublayer recognizes and accepts any frame whose DA field contains the Broadcast address.

The MAC sublayer is capable of activating some number of group addresses as specified by higher layers. The MAC sublayer recognizes and accepts any frame whose Destination Address field contains an active group address. An active group address may be deactivated.

The MAC sublayer may also provide the capability of operating in the promiscuous receive mode. In this mode of operation, the MAC sublayer recognizes and accepts all valid frames, regardless of their Destination Address field values.

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4A.2.4.1.2 Frame check sequence validation

FCS validation is essentially identical to FCS generation. If the bits of the incoming frame (exclusive of the FCS field itself) do not generate a CRC value identical to the one received, an error has occurred and the frame is identified as invalid.

4A.2.4.1.3 Frame disassembly

Upon recognition of the Start Frame Delimiter at the end of the preamble sequence, the MAC sublayer accepts the frame. If there are no errors, the frame is disassembled and the fields are passed to the MAC client by way of the output parameters of the ReceiveFrame operation.

4A.2.4.2 Receive media access management

The MAC sublayer recognizes the boundaries of an incoming MAC frame by monitoring the receiveDataValid signal provided by the Physical Layer. Two possible length errors can occur that indicate ill-framed data: the MAC frame may be too long, or its length may not be an integer number of octets.

a) *Maximum Frame Size.* The receiving MAC sublayer is not required to enforce the MAC frame size limit, but it is allowed to truncate MAC frames longer than maxFrameSizeLimit octets (see 4.2.7.1). If optional layer management is implemented, such frames may be counted whether or not they are truncated. They may also be reported as an implementation-dependent error.

CAUTION

It is recommended that any implementation that truncates MAC frames should invalidate those frames as they may have severely weakened error protection and may cause serious problems if forwarded to the MAC client.

b) *Integer Number of Octets in Frame.* Since the format of a valid MAC frame specifies an integer number of octets, only a collision or an error can produce a MAC frame with a length that is not an integer multiple of 8 bits. Complete MAC frames (that is, not rejected for being too small) that do not contain an integer number of octets are truncated to the nearest octet boundary. If frame check sequence validation detects an error in such a MAC frame, the status code alignmentError is reported

4A.2.5 Preamble generation

In a LAN implementation, most of the Physical Layer components are allowed to provide valid output some number of bit times after being presented valid input signals. Thus it is necessary for a preamble to be sent before the start of data, to allow the PLS circuitry to reach its steady state. Upon request by TransmitLinkMgmt to transmit the first bit of a new frame, BitTransmitter shall first transmit the preamble, a bit sequence used for physical medium stabilization and synchronization, followed by the Start Frame Delimiter. The preamble pattern is:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

The bits are transmitted in order, from left to right. The nature of the pattern is such that, for Manchester encoding, it appears as a periodic waveform on the medium that enables bit synchronization. It should be noted that the preamble ends with a 0.

4A.2.6 Start frame sequence

The receiveDataValid signal is the indication to the MAC that the frame reception process should begin. Upon reception of the sequence 10101011 following the assertion of receiveDataValid, PhysicalSignalDecap shall begin passing successive bits to ReceiveLinkMgmt for passing to the MAC client.

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4A.2.7 Global declarations

This subclause provides detailed formal specifications for the MAC sublayer. It is a specification of generic features and parameters to be used in systems implementing this media access method. 4A.4 provides values for these sets of parameters for recommended implementations of this media access mechanism.

4A.2.7.1 Common constants, types, and variables

The following declarations of constants, types and variables are used by the MAC frame transmission and reception sections of each MAC sublayer:

```
const
    addressSize = 48; {In bits, in compliance with 3.2.3}
    lengthOrTypeSize = 16; {In bits}
    clientDataSize = ...; {In bits, size of MAC Client Data; see 4A.2.2.2, a) 3)}
    padSize = ...; {In bits, = max (0, minFrameSize ─ (2 × addressSize + lengthOrTypeSize +
                                                        clientDataSize + crcSize))}
    dataSize = ...; {In bits, = clientDataSize + padSize}
    crcSize = 32; {In bits, 32-bit CRC}
    frameSize = ...; {In bits, = 2 × addressSize + lengthOrTypeSize + dataSize + crcSize; see 4A.2.2.2, a)}
    minFrameSize = ...; {In bits, see 4A.4}
    maxBasicFrameSize = 1518; {In octets, see 3.2.7, 4A.4}
    maxEnvelopeFrameSize = 2000; {In octets, see 3.2.7, 4A.4}
    qTagPrefixSize = 4; {In octets, length of Q-tag Prefix, see 3.2.7, 4A.4}
    maxFrameSizeLimit = maxBasicFrameSize or (maxBasicFrameSize + qTagPrefixSize) or
                        maxEnvelopeFrameSize ; {in octets}
    minTypeValue = 1536; {Minimum value of the Length/Type field for Type interpretation}
    maxBasicDataSize = 1500;
                        {In octets, the maximum length of the MAC Client Data field of the basic frame.}
    preambleSize = 56; {In bits, see 4A.2.5}
    sfdSize = 8; {In bits, Start Frame Delimiter}
    headerSize = 64; {In bits, sum of preambleSize and sfdSize}
type
    Bit = (0, 1);
    AddressValue = array [1..addressSize] of Bit;
    LengthOrTypeValue = array [1..lengthOrTypeSize] of Bit;
    DataValue = array [1..dataSize] of Bit; {Contains the portion of the MAC frame that starts with the first
                                             bit following the Length/Type field and ends with the last bit
                                             prior to the FCS field.
    CRCValue = array [1..crcSize] of Bit;
    PreambleValue = array [1..preambleSize] of Bit;
    SfdValue = array [1..sfdSize] of Bit;
    ViewPoint = (fields, bits); {Two ways to view the contents of a MAC frame}
    HeaderViewPoint = (headerFields, headerBits);
    Frame = record {Format of MAC frame}
        case view: ViewPoint of
            fields: (
                destinationField: AddressValue;
                sourceField: AddressValue;
                lengthOrTypeField: LengthOrTypeValue;
                dataField: DataValue;
                fcsField: CRCValue);
            bits: (contents: array [1..frameSize] of Bit)
        end; {MAC frame}
    Header = record {Format of Preamble and Start Frame Delimiter}
        case headerView: HeaderViewPoint of
```


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```
        headerFields: (
          preamble: PreambleValue;
          sfd: SfdValue);
        headerBits: (headerContents: array [1..headerSize] of Bit)
    end; {Defines header for MAC frame}
  TransmitStatus = (transmitDisabled, transmitOK, excessiveCollisionError, lateCollisionErrorStatus);
  ReceiveStatus = (receiveDisabled, receiveOK, frameTooLong, frameCheckError, lengthError,
                   alignmentError);
```

4A.2.7.2 Transmit state variables

The following items are specific to packet transmission. (See also 4A.4.)

```
const
  interPacketGap = ...; {In bit times, minimum gap between packets,
                         see 4A.4}
var
  outgoingFrame: Frame; {The frame to be transmitted}
  outgoingHeader: Header;
  currentTransmitBit, lastTransmitBit: 1..frameSize; {Positions of current and last outgoing bits in
                                                      outgoingFrame}
  lastHeaderBit: 1..headerSize;
  deferring: Boolean; {Implies any pending transmission has to wait for the Physical Layer to be ready for
                       the next packet and for the interpacket gap}
  deferenceMode: Boolean; {Indicates the desired mode of operation, and enables waiting for
                           interpacket gap during the deference process}
  carrierSenseMode: Boolean; {Indicates the desired mode of operation, and enables using carrierSense
                              to extend deference due to congestion in the PHY}
```

4A.2.7.3 Receive state variables

The following items are specific to frame reception. (See also 4A.4.)

```
var
  incomingFrame: Frame; {The frame being received}
  receiving: Boolean; {Indicates that a frame reception is in progress}
  excessBits: 0..7; {Count of excess trailing bits beyond octet boundary}
  receiveSucceeding: Boolean; {Running indicator of whether reception is succeeding}
  validLength: Boolean; {Indicator of whether received frame has a length error}
  exceedsMaxLength: Boolean; {Indicator of whether received frame has a length longer than the
                              maximum permitted length}
  passReceiveFCSMode: Boolean; {Indicates the desired mode of operation, and enables passing of
                                the frame check sequence field of all received frames from the
                                MAC sublayer to the MAC client. passReceiveFCSMode is a
                                static variable}
```

4A.2.7.4 State variable initialization

The procedure Initialize has to be run when the MAC sublayer begins operation, before any of the processes begin execution. Initialize sets certain crucial shared state variables to their initial values. (All other global variables are appropriately reinitialized before each use.) Initialize then waits for the medium to be idle, and starts operation of the various processes.

NOTE—Care should be taken to ensure that the time from the completion of the Initialize process to when the first packet transmission begins is at least an interFrameGap.

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If Layer Management is implemented, the Initialize procedure shall only be called as the result of the initializeMAC action (30.3.1.2.1).

```
procedure Initialize;
begin
    deferring := false;
    transmitting := false; {An interface to Physical Layer; see below}
    receiving := false;
    passReceiveFCSMode := ...; {True when enabling the passing of the frame check sequence of all
                                received frames from the MAC sublayer to the MAC client is desired and
                                supported, false otherwise}
    deferenceMode := ...; {False for implementations that cannot rely on deference within the MAC to
                           provide an interframe gap, true otherwise}
    carrierSenseMode := ...; {True for implementations that use carrierSense to indicate congestion in the
                           PHY, false otherwise.}
    while ((carrierSenseMode and carrierSense) or receiveDataValid) do nothing
    {Start execution of all processes}
end; {Initialize}
```

4A.2.8 Frame transmission

The algorithms in this subclause define MAC sublayer frame transmission. The function TransmitFrame implements the frame transmission operation provided to the MAC client.

The TransmitFrame operation is synchronous. Its duration is the entire attempt to transmit the frame; when the operation completes, transmission has either succeeded or failed, as indicated by the TransmitStatus status code.

The transmitDisabled status code indicates that the transmitter is not enabled. Successful transmission is indicated by the status code transmitOK. The codes excessiveCollisionError and lateCollisionErrorStatus are artifacts of the CSMA/CD MAC and maintained here for historical purposes. These codes are never generated by this full duplex MAC. TransmitStatus is not used by the service interface defined in 2.3.1. TransmitStatus may be used in an implementation dependent manner.

```
function TransmitFrame (
    destinationParam: AddressValue;
    sourceParam: AddressValue;
    lengthOrTypeParam: LengthOrTypeValue;
    dataParam: DataValue;
    fcsParamValue: CRCValue;
    fcsParamPresent: Bit): TransmitStatus;
procedure TransmitDataEncap; {Nested procedure; see body below}
begin
    if transmitEnabled then
        begin
            TransmitDataEncap;
            TransmitFrame := TransmitLinkMgmt
        end
    else TransmitFrame := transmitDisabled
end; {TransmitFrame}
```


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If transmission is enabled, TransmitFrame calls the internal procedure TransmitDataEncap to construct the frame. Next, TransmitLinkMgmt is called to perform the actual transmission. The TransmitStatus returned indicates the success or failure of the transmission attempt.

TransmitDataEncap builds the frame and places the 32-bit CRC in the frame check sequence field:

```
procedure TransmitDataEncap;
begin
   with outgoingFrame do
      begin {Assemble frame}
         view := fields;
         destinationField := destinationParam;
         sourceField := sourceParam;
         lengthOrTypeField := lengthOrTypeParam;
         if fcsParamPresent then
            begin
               dataField := dataParam; {No need to generate pad if the FCS is passed from MAC client}
               fcsField := fcsParamValue {Use the FCS passed from MAC client}
            end
         else
            begin
               dataField := ComputePad(dataParam);
               fcsField := CRC32(outgoingFrame)
            end;
         view := bits
      end {Assemble frame}
   with outgoingHeader do
      begin
         headerView := headerFields;
         preamble := ...; {* '1010...10,' LSB to MSB*}
         sfd := ...; {* '10101011,' LSB to MSB*}
         headerView := headerBits
      end
end; {TransmitDataEncap}
```

If the MAC client chooses to generate the frame check sequence field for the frame, it passes this field to the MAC sublayer via the fcsParamValue parameter. If the fcsParamPresent parameter is true, TransmitDataEncap uses the fcsParamValue parameter as the frame check sequence field for the frame. Such a frame shall not require any padding, since it is the responsibility of the MAC client to ensure that the frame meets the minFrameSize constraint. If the fcsParamPresent parameter is false, the fcsParamValue parameter is unspecified. TransmitDataEncap first calls the ComputePad function, followed by a call to the CRC32 function to generate the padding (if necessary) and the frame check sequence field for the frame internally to the MAC sublayer.

ComputePad appends an array of arbitrary bits to the MAC client data to pad the frame to the minimum frame size:

```
function ComputePad(var dataParam: DataValue): DataValue;
begin
   ComputePad := {Append an array of size padSize of arbitrary bits to the MAC client dataField}
end; {ComputePad}
```

TransmitLinkMgmt attempts to transmit the frame. When deferenceMode is true, it first defers to the Physical Layer if it is not ready for the next packet and to ensure proper interframe spacing. When deferenceMode is false, it begins transmitting immediately:

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```
function TransmitLinkMgmt: TransmitStatus;
begin
   while deferring do nothing {Defer to Physical Layer congestion and IFS}
   StartTransmit;
   while transmitting do nothing
   LayerMgmtTransmitCounters; {Update transmit and transmit error counters in 5.2.4.2}
   TransmitLinkMgmt := transmitOK
end; {TransmitLinkMgmt}
```

Each time a frame transmission attempt is initiated, StartTransmit is called to alert the BitTransmitter process that bit transmission should begin:

```
procedure StartTransmit;
begin
   currentTransmitBit := 1;
   lastTransmitBit := frameSize;
   lastHeaderBit:= headerSize;
   transmitting := true
end; {StartTransmit}
```

The Deference process runs asynchronously to continuously compute the proper value for the variable deferring:

```
process Deference;
begin
   cycle {Main loop}
      while (not transmitting and not (carrierSenseMode and carrierSense)) do nothing; {Wait for the start
                                                                                          of transmission or congestion}
      deferring := true; {Inhibit future transmissions}
      while (transmitting or (carrierSenseMode and carrierSense)) do nothing; {Wait for the end of
                                                                                transmission and congestion}
      if deferenceMode then Wait(interPacketGap);
            {Time out entire interpacket gap if enabled}
      deferring := false {Don't inhibit transmission}
   end {Main loop}
end; {Deference}
```

The BitTransmitter process runs asynchronously, transmitting bits at a rate determined by the Physical Layer's TransmitBit operation:

```
process BitTransmitter;
begin
   cycle {Outer loop}
      if transmitting then
         begin {Inner loop}
            while (currentTransmitBit ≤ lastHeaderBit) do
               begin
                  TransmitBit(outgoingHeader[currentTransmitBit]);
                  currentTransmitBit := currentTransmitBit + 1
               end;
            currentTransmitBit := 1;
            while transmitting do
               begin
                  TransmitBit(outgoingFrame[currentTransmitBit]);
                  currentTransmitBit := currentTransmitBit + 1;
                  transmitting := (currentTransmitBit ≤ lastTransmitBit)
               end
```


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```
            end {Inner loop}
        end {Outer loop}
    end; {BitTransmitter}
```

4A.2.9 Frame reception

The algorithms in this subclause define the MAC sublayer frame reception.

The function ReceiveFrame implements the frame reception operation provided to the MAC client.

The ReceiveFrame operation is synchronous. The operation does not complete until a frame has been received. The fields of the frame are delivered via the output parameters with the ReceiveStatus status code.

The receiveDisabled status indicates that the receiver is not enabled. Successful reception is indicated by the status code receiveOK. The frameTooLong error indicates that the last frame received had a frameSize beyond the maximum allowable frame size. The code frameCheckError indicates that the frame received was damaged by a transmission error. The lengthError indicates that the lengthOrTypeParam value was both consistent with a length interpretation of this field (i.e., its value was less than or equal to maxValidFrame), and inconsistent with the frameSize of the received frame. The code alignmentError indicates that the frame received was damaged, and that in addition, its length was not an integer number of octets. ReceiveStatus is not mapped to any MAC client parameter by the service interface defined in 2.3.2. ReceiveStatus may be used in an implementation dependent manner.

```
    function ReceiveFrame (
        var destinationParam: AddressValue;
        var sourceParam: AddressValue;
        var lengthOrTypeParam: LengthOrTypeValue;
        var dataParam: DataValue;
        var fcsParamValue: CRCValue;
        var fcsParamPresent: Bit): ReceiveStatus;

    function ReceiveDataDecap: ReceiveStatus; {Nested function; see body below}
    begin
        if receiveEnabled then
            repeat
                ReceiveLinkMgmt;
                ReceiveFrame := ReceiveDataDecap;
            until receiveSucceeding
        else ReceiveFrame := receiveDisabled
    end; {ReceiveFrame}
```

If enabled, ReceiveFrame calls ReceiveLinkMgmt to receive the next valid frame, and then calls the internal function ReceiveDataDecap to return the frame's fields to the MAC client if the frame's address indicates that it should do so. The returned ReceiveStatus indicates the presence or absence of detected transmission errors in the frame.

```
    function ReceiveDataDecap: ReceiveStatus;
        var status: ReceiveStatus; {Holds receive status information}
    begin
        with incomingFrame do
            begin
                view := fields;
                receiveSucceeding := LayerMgmtRecognizeAddress(destinationField);
                if receiveSucceeding then
```


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```
            begin {Disassemble MAC frame}
               destinationParam := destinationField;
               sourceParam := sourceField;
               lengthOrTypeParam := lengthOrTypeField;
               dataParam := RemovePad(lengthOrTypeField, dataField);
               fcsParamValue := fcsField;
               fcsParamPresent := passReceiveFCSMode;
               exceedsMaxLength := ...; {Check to determine if received MAC frame size exceeds
                                         maxFrameSizeLimit.
                                         MAC implementations use maxFrameSizeLimit to
                                         determine if management counts the frame as too long.
                                         It is recommended that new implementations support
                                         maxFrameSizeLimit = maxEnvelopeFrameSize )
               if exceedsMaxLength then status := frameTooLong
               else if fcsField = CRC32(incomingFrame) then
                     if validLength then status := receiveOK else status := lengthError
               else if excessBits = 0 then status := frameCheckError
               else status := alignmentError;
               LayerMgmtReceiveCounters(status); {Update receive counters in 5.2.4.3}
               view := bits
            end {Disassemble MAC frame}
         end; {With incomingFrame}
      ReceiveDataDecap := status
   end; {ReceiveDataDecap}

   function LayerMgmtRecognizeAddress(address: AddressValue): Boolean;
   begin
      if {promiscuous receive enabled} then LayerMgmtRecognizeAddress := true;
      else if address = ... {MAC station address} then LayerMgmtRecognizeAddress := true;
      else if address = ... {Broadcast address} then LayerMgmtRecognizeAddress := true;
      else if address = ... {One of the addresses on the multicast list and multicast reception is enabled} then
                                                                  LayerMgmtRecognizeAddress := true;
      else LayerMgmtRecognizeAddress := false
   end; {LayerMgmtRecognizeAddress}
```

The function RemovePad strips any padding that was generated to meet the minFrameSize constraint, if possible. When the MAC sublayer operates in the mode that enables passing of the frame check sequence field of all received MAC frames to the MAC client (passReceiveFCSMode variable is true), it shall not strip the padding and it shall leave the data field of the MAC frame intact. Length checking is provided for Length interpretations of the Length/Type field. For Length/Type field values in the range between maxBasicDataSize and minTypeValue the behavior of the RemovePad function is unspecified:

```
   function RemovePad(var lengthOrTypeParam: LengthOrTypeValue; dataParam: DataValue): DataValue;
   begin
      if lengthOrTypeParam ≥ minTypeValue then
         begin
            validLength := true; {Don't perform length checking for Type interpretation}
            RemovePad := dataParam
         end
      else if lengthOrTypeParam ≤ maxBasicDataSize then
         begin
            validLength := {For length interpretations of the Length/Type field, check to determine if value
                              represented by Length/Type field matches the received clientDataSize};
            if validLength and not passReceiveFCSMode then
```


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```
            RemovePad := {Truncate the dataParam (when present) to the value represented by the
                          lengthOrTypeParam (in octets) and return the result}
        else RemovePad := dataParam
      end
end; {RemovePad}
```

ReceiveLinkMgmt attempts repeatedly to receive the bits of a frame, discarding any fragments smaller than the minimum valid frame size:

```
procedure ReceiveLinkMgmt;
begin
  repeat
    StartReceive;
    while receiving do nothing; {Wait for frame to finish arriving}
    excessBits := frameSize mod 8;
    frameSize := frameSize – excessBits; {Truncate to octet boundary}
    receiveSucceeding := (frameSize ≥ minFrameSize) {Reject frames too small}
  until receiveSucceeding
end; {ReceiveLinkMgmt}

procedure StartReceive;
begin
  receiving := true
end; {StartReceive}
```

The BitReceiver process runs asynchronously, receiving bits from the medium at the rate determined by the Physical Layer's ReceiveBit operation, partitioning them into frames, and optionally receiving them:

```
process BitReceiver;
  var   b: Bit;
        currentReceiveBit: 1..frameSize; {Position of current bit in incomingFrame}
begin
  cycle {Outer loop}
    if receiveEnabled then
      begin {Receive next frame from Physical Layer}
        currentReceiveBit := 1;
        PhysicalSignalDecap; {Skip idle, strip off preamble and sfd}
        while receiveDataValid do
          begin {Inner loop to receive the rest of an incoming frame}
            b := ReceiveBit; {Next bit from physical medium}
            if receiving then {Append to frame}
            begin
              incomingFrame[currentReceiveBit] := b;
              currentReceiveBit := currentReceiveBit + 1
            end; {append bit to frame}
            receiving := receiveDataValid
          end; {Inner loop}
        frameSize := currentReceiveBit – 1
      end {Enabled}
  end {Outer loop}
end; {BitReceiver}

procedure PhysicalSignalDecap;
begin
  {Receive one bit at a time from physical medium until a valid sfd is detected, discard bits and return}
end; {PhysicalSignalDecap}
```


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4A.2.10 Common procedures

The function CRC32 is used by both the transmit and receive algorithms to generate a 32-bit CRC value:

```
function CRC32(f: Frame): CRCValue;
begin
    CRC32 := {The 32-bit CRC for the entire frame as defined in 3.2.9, excluding the FCS field (if
             present)}
end; {CRC32}
```

Purely to enhance readability, the following procedure is also defined:

procedure nothing; *begin end*;

The idle state of a process (that is, while waiting for some event) is cast as repeated calls on this procedure.

4A.3 Interfaces to/from adjacent layers

4A.3.1 Overview

The purpose of this clause is to provide precise definitions of the interfaces between the architectural layers defined in Clause 1 in compliance with the Media Access Service Specification given in Clause 2. In addition, the services required from the physical medium are defined.

The notation used here is the Pascal language, in keeping with the procedural nature of the precise MAC sublayer specification (see 4A.2). Each interface is described as a set of procedures or shared variables, or both, that collectively provide the only valid interactions between layers. The accompanying text describes the meaning of each procedure or variable and points out any implicit interactions among them.

The description of the interfaces in Pascal is a notational technique, and in no way implies that they can or should be implemented in software. This point is discussed more fully in 4A.2, that provides complete Pascal declarations for the data types used in the remainder of this clause. The synchronous (one frame at a time) nature of the frame transmission and reception operations is a property of the architectural interface between the MAC client and MAC sublayers, and need not be reflected in the implementation interface between a station and its sublayer.

4A.3.2 MAC service

The services provided to the MAC client by the MAC sublayer are transmission and reception of MAC frames using service primitives MA_DATA.request and MA_DATA.indication, as defined in Clause 2. For historical reasons the MAC sublayer definitions use two functions, TransmitFrame and ReceiveFrame, defined in 4A.2.8 and 4A.2.9. The relationship between these two functions and the service primitives is defined by the MAC client state diagrams in 4A.3.2.1 and 4A.3.2.2.

The state machines in 4A.3.2 follow the conventions in 21.5.

4A.3.2.1 MAC client transmit interface state diagram

4A.3.2.1.1 Variables

data
: The value of mac_service_data_unit excluding the first two octets (Length/Type field).

destination_address
: The Destination Address field parsed from the client request.

fcsPresent
: Indicates whether the MA_DATA.request service primitive contained the frame_check_sequence field.

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frame_check_sequence
: The fcs field parsed from the client request.

lengthOrType
: The value of the first two octets at the start of the mac_service_data_unit.

mac_service_data_unit
: The concatenation of the lengthOrType field and the data field parsed from the client request.

source_address
: The Source Address field parsed from the client request

TransmitStatus
: Indicates the status of the transmitted MAC frame. See 4.2.8.

4A.3.2.1.2 Functions

TransmitFrame
: The MAC sublayer function invoked to transmit a MAC frame with the specified parameters. See 4A.2.8.

4A.3.2.1.3 Messages

MA_DATA.request
: The service primitive used to convey a MAC frame to be transmitted from the MAC client. See 2.3.1. The action invoked is not considered to end until the transmission of the frame by the MAC has concluded.

4A.3.2.1.4 MAC client transmit interface state diagram

Figure 4A–3 specifies the behavior of the transmit interface from the MAC client

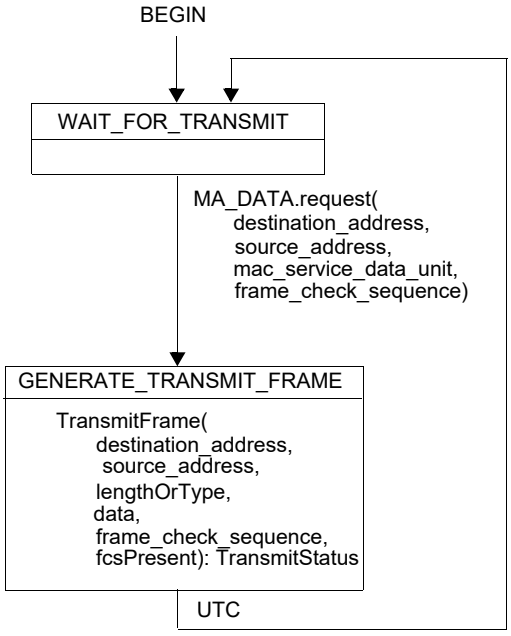

Figure 4A–3—MAC client transmit interface state diagram

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4A.3.2.2 MAC client receive interface state diagram

4A.3.2.2.1 Variables

destination_address
: The Destination Address field parsed from the received MAC frame.

source_address
: The Source Address field parsed from the received MAC frame.

lengthOrType
: The lengthOrType field parsed from the received MAC frame.

data
: The data payload field parsed from the received MAC frame.

fcsPresent
: A Boolean set by the MAC sublayer.

ReceiveStatus
: Indicates the status of the received MAC frame.

mac_service_data_unit
: The concatenation of the lengthOrType field and the data field parsed from the received MAC frame.

frame_check_sequence
: The fcs field parsed from the received MAC frame.

4A.3.2.2.2 Functions

ReceiveFrame
: The MAC sublayer function invoked to accept an incoming MAC frame with the specified parameters. See 4A.2.9.

4A.3.2.2.3 Messages

MA_DATA.indication
: The service primitive used to transfer an incoming MAC frame to the MAC client with the specified parameters. See 2.3.2.

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4A.3.2.2.4 MAC client receive interface state diagram

Figure 4A–4 specifies the behavior of the receive interface to the MAC client.

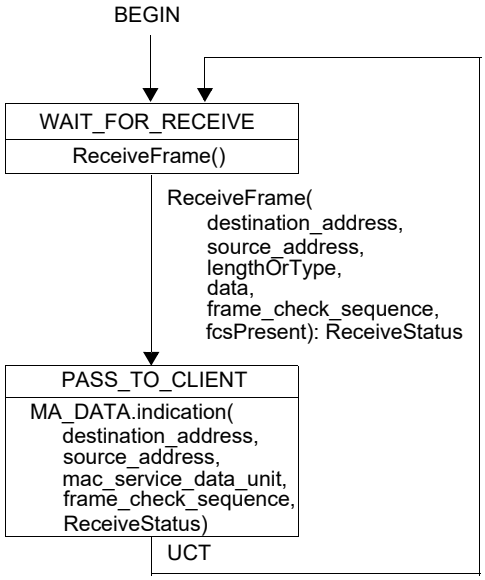

Figure 4A–4—MAC client receive interface state diagram

4A.3.3 Services required from the Physical Layer

The interface through which the MAC sublayer uses the facilities of the Physical Layer consists of a function, a pair of procedures and four Boolean variables as described in Table 4A–1.

Table 4A–1—Full duplex MAC functions, procedures and variables

Function	Procedures	Variables
ReceiveBit	**TransmitBit**	**collisionDetect**
	Wait	**carrierSense**
		receiveDataValid
		transmitting

During transmission, the contents of an outgoing frame are passed from the MAC sublayer to the Physical Layer by way of repeated use of the TransmitBit operation:

procedure TransmitBit (bitParam: Bit);

Each invocation of TransmitBit passes one new bit of the outgoing frame to the Physical Layer. The TransmitBit operation is synchronous. The duration of the operation is the entire transmission of the bit. The operation completes when the Physical Layer is ready to accept the next bit and it transfers control to the MAC sublayer.

The overall event of data being transmitted is signaled to the Physical Layer by way of the variable transmitting:

var transmitting: Boolean*;*

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Before sending the first bit of a frame, the MAC sublayer sets transmitting to true, to inform the Physical Layer that a stream of bits will be presented via the TransmitBit operation. After the last bit of the frame has been presented, the MAC sublayer sets transmitting to false to indicate the end of the frame.

The collisionDetect variable is not used by this full duplex MAC but maintained as an artifact of the CSMA/CD MAC's interface to the Physical Layer.

var collisionDetect: Boolean*;*

During reception, the contents of an incoming frame are retrieved from the Physical Layer by the MAC sublayer via repeated use of the ReceiveBit operation:

function ReceiveBit: Bit;

Each invocation of ReceiveBit retrieves one new bit of the incoming frame from the Physical Layer. The ReceiveBit operation is synchronous. Its duration is the entire reception of a single bit. Upon receiving a bit, the MAC sublayer shall immediately request the next bit until all bits of the frame have been received (see 4A.2 for details).

The overall event of data being received is signaled to the MAC sublayer by the variable receiveDataValid:

var receiveDataValid: Boolean*;*

When the Physical Layer sets receiveDataValid to true, the MAC sublayer shall immediately begin retrieving the incoming bits by the ReceiveBit operation. When receiveDataValid subsequently becomes false, the MAC sublayer can begin processing the received bits as a completed frame. If an invocation of ReceiveBit is pending when receiveDataValid becomes false, ReceiveBit returns an undefined value, which should be discarded by the MAC sublayer (see 4A.2 for details).

The overall event of congestion at the Physical Layer, indicating that the Physical Layer is not ready to accept the next packet, is signaled to the MAC sublayer by the variable carrierSense:

var carrierSense: Boolean*;*

When the value of variable carrierSenseMode is set to TRUE, the MAC sublayer shall monitor the value of carrierSense to defer its own transmissions when the Physical Layer is busy. The Physical Layer sets carrierSense to true immediately upon congestion within the Physical Layer. After the congestion ceases, carrierSense is set to false. When the value of variable carrierSenseMode is set to FALSE, the carrierSense variable is ignored by the MAC.

While the label carrierSense does not accurately describe the condition presented by this variable, the name is maintained as an artifact of the CSMA/CD MAC interface to the Physical Layer.

The Physical Layer also provides the procedure Wait:

procedure Wait (bitTimes: integer)*;*

This procedure waits for the specified number of bit times. This allows the MAC sublayer to measure time intervals in units of the (physical-medium-dependent) bit time.

4A.4 Specific implementations

4A.4.1 Compatibility overview

To provide total compatibility at all levels of the standard, it is required that each network component implementing the MAC sublayer procedure adheres rigidly to these specifications. The information provided in 4A.4.2 provides design parameters for specific implementations of this access method. Variations from these values result in a system implementation that violates the standard. See the warning in 4A.4.2.

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4A.4.2 MAC parameters

The parameter values shown in Table 4A–2 shall be used.

Table 4A–2—Full duplex MAC parameter values

Parameters	Values
interPacketGap	96 bits
maxBasicFrameSize	1518 octets
maxEnvelopeFrameSize	2000 octets
minFrameSize	512 bits (64 octets)

The minimum interPacketGap shall be enforced in this sublayer, when the deferenceMode variable is set to TRUE, or outside this sublayer, when the deferenceMode variable is set to FALSE.

NOTE 1—For 10 Mb/s operation, the spacing between two successive non-colliding packets, from start of idle at the end of the first packet to start of Preamble of the subsequent packet, can have a minimum value of 47 BT (bit times), at the AUI receive line of the DTE. This interpacket gap shrinkage is caused by variable network delays, added preamble bits, and clock skew.

NOTE 2—For 1 Gb/s operation, the spacing between two non-colliding packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet, can have a minimum value of 64 BT (bit times), as measured at the GMII receive signals at the DTE. This interpacket gap shrinkage may be caused by variable network delays, added preamble bits, and clock tolerances.

NOTE 3—For 10 Gb/s and 25 Gb/s operation, the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet, can have a minimum value of 40 BT (bit times), as measured at the XGMII or 25GMII receive signals at the DTE. This interpacket gap shrinkage may be caused by variable network delays and clock tolerances.

NOTE 4—For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s operation, the received interpacket gap (the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet) can have a minimum value of 8 BT (bit times), as measured at the XLGMII, 50GMII, CGMII, 200GMII, or 400GMII receive signals at the DTE due to clock tolerance and lane alignment requirements.

WARNING

Any deviation from the above specified values may affect proper operation of the network.

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NOTE—The remaining annexes in the standard are numbered in correspondence to their associated clauses; e.g., Annexes 22A, 22B, 22C, and 22D correspond to Clause 22.

Annex 22A

(informative)

MII output delay, setup, and hold time budget

22A.1 System model

The discussion of signal timing characteristics that follows will refer to the system model depicted in Figure 22A–1, Figure 22A–2, and Figure 22A–3. This system model can be applied to each of the three application environments defined in 22.2.1.

Figure 22A–1 depicts a simple system model in which the MII is used to interconnect two integrated circuits on the same circuit assembly. In this model the Reconciliation sublayer comprises one integrated circuit, and the PHY comprises the other. A Reconciliation sublayer or a PHY may actually be composed of several separate integrated circuits. The system model in Figure 22A–1 includes two unidirectional signal transmission paths, one from the Reconciliation sublayer to the PHY and one from the PHY to the Reconciliation sublayer. The path from the Reconciliation sublayer to the PHY is separated into two sections, labeled A1 and B1. The path from the PHY to the Reconciliation sublayer is separated into two sections, labeled C1 and D1.

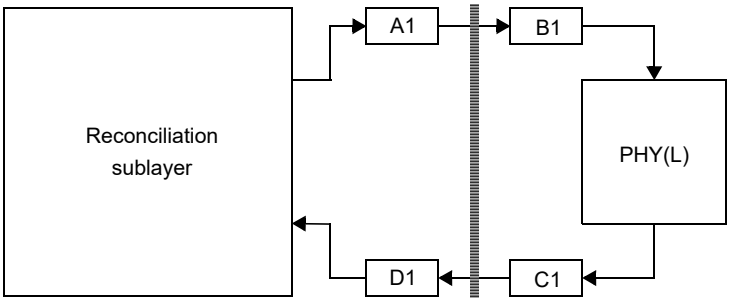

Figure 22A–1—Model for integrated circuit to integrated circuit connection

Figure 22A–2 depicts a system model for the case where the MII is used to interconnect two circuit assemblies. The circuit assemblies may be physically connected in a motherboard/daughterboard arrangement, or they may be physically connected with the cable defined in 22.4.5 and the line interface connector defined in 22.6. The system model in Figure 22A–2 includes two unidirectional signal transmission paths, one from the Reconciliation sublayer to the PHY and one from the PHY to the Reconciliation sublayer. The path from the Reconciliation sublayer to the PHY is separated into two sections, labeled A2 and B2. The path from the PHY to the Reconciliation sublayer is separated into two sections, labeled C2 and D2.

Figure 22A–3 depicts a system model in which the MII is used to interconnect both integrated circuits and circuit assemblies. This system model allows for separate signal transmission paths to exist between the Reconciliation sublayer and a local PHY(L), and between the Reconciliation sublayer and a remote PHY(R). The unidirectional paths between the Reconciliation sublayer and the PHY(L) are composed of sections A1,

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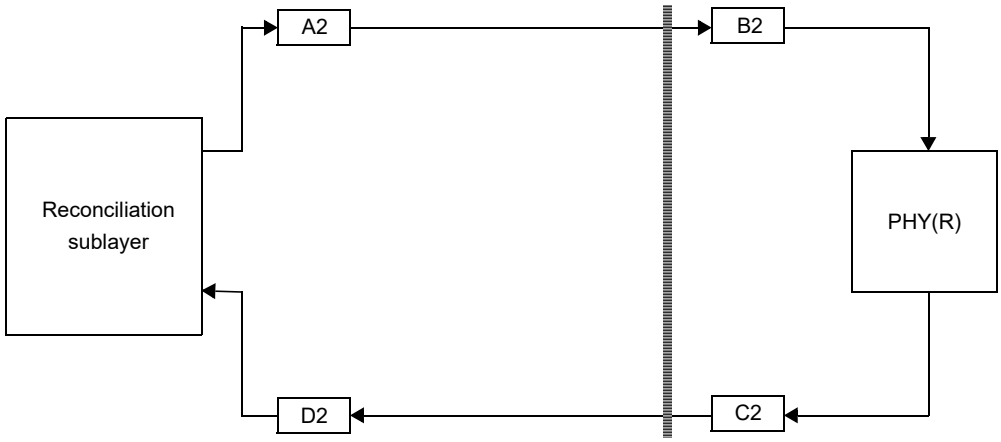

Figure 22A–2—Model for circuit assembly to circuit assembly connection

B1, C1, and D1. The unidirectional paths between the Reconciliation sublayer and the remote PHY(R) are composed of sections A2, B2, C2, and D2.

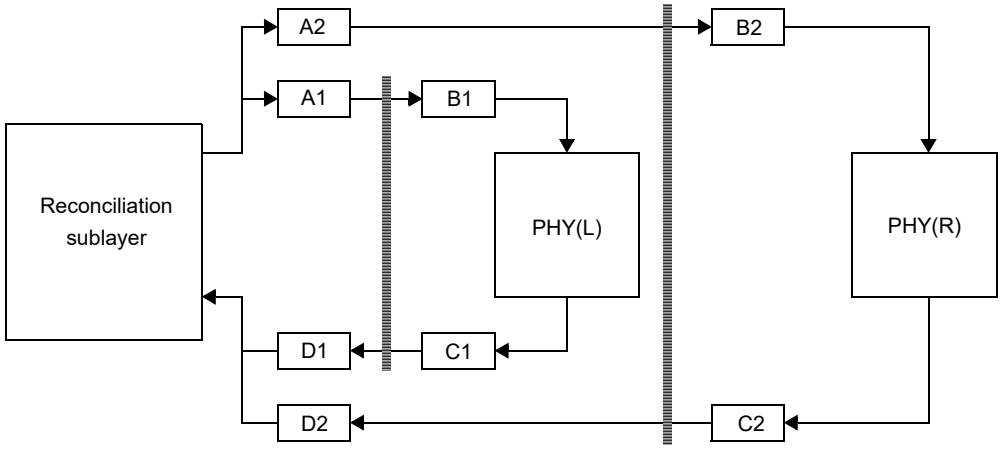

Figure 22A–3—Combined model

Each of these system models assumes a set of common timing and electrical characteristics that shall be met at the input and output ports of the Reconciliation sublayer and PHY devices. The characteristics of the signal transmission paths are identified for each of the sections A1, B1, C1, D1, A2, B2, C2, and D2.

22A.2 Signal transmission path characteristics

The signal transmission path characteristics are specified for each of the path sections defined in 22A.1. The characteristics for these sections are specified so as to allow sections A1, B1, C1, and D1 to be implemented in the form of printed circuit board traces, while sections A2, B2, C2, and D2 may be implemented with a combination of printed circuit board traces and wire conductors in a cable assembly.

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The signal transmission path characteristics are stated in terms of their maximum delay and their characteristic impedance. These values are summarized in Table 22A–1.

Table 22A–1—Signal transmission path characteristics

Section	Maximum delay (ns)	Impedance (Ω)
A1, D1	5	68 ± 15%
B1, C1	2.5	68 ± 15%
A2, D2	5	68 ± 10%
B2, C2	2.5	68 ± 10%

The driver characteristics specified in 22.4.3, the receiver characteristics specified in 22.4.4, and the signal transmission path characteristics specified in Table 22A–1 can be applied to the system models shown in Figure 22A–1 or Figure 22A–2. The combination of loads presented in Figure 22A–3 cannot be adequately driven by an output buffer that meets the driver characteristics specified in 22.4.3 while being sampled by an input buffer that meets the receiver characteristics specified in 22.4.4.

To address the system model depicted in Figure 22A–3, it is permissible to incorporate an additional stage of buffering into path sections A1, A2, D1, and D2, provided that the resulting maximum delay characteristic for those path sections does not exceed the value stated in Table 22A–1. The delay characteristic for transmission path sections A2 and D2 includes an allowance for the delay that results from the presence of a lumped capacitive load at the end of the path. For a transmission path section with a characteristic impedance Z_o, with a lumped capacitive load C_L, this delay is nominally Z_oC_L. In the case of a maximum transmission path section impedance of 78 Ω with a lumped load of 8 pF, the nominal delay is 0.6 ns. Thus the allowable delay for a buffer inserted into transmission path section A2 or D2 is 4.4 ns.

22A.3 Budget calculation

A recommended timing budget is shown in Table 22A–2. This budget assumes that the combined system model shown in Figure 22A–3 represents a worst case.

Table 22A–2—Round-trip delay budget

Description	Incremental delay (ns)	Cumulative delay (ns)
TX_CLK output at PHY(R)	0.0	0.0
Transmission path section C2	2.5	2.5
Transmission path section D2	5.0	7.5
Clock to output in Reconciliation sublayer	15.0	22.5

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Table 22A–2—Round-trip delay budget *(continued)*

Description	Incremental delay (ns)	Cumulative delay (ns)
Transmission path section A2	5.0	27.5
Transmission path section B2	2.5	30.0
Setup time at PHY(R)	10.0	40.0

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Annex 22B

(informative)

MII driver ac characteristics

22B.1 Implications of CMOS ASIC processes

For MII drivers that drive rail to rail, such as those commonly used in CMOS ASICs (complimentary metal oxide semiconductor application-specific integrated circuits), the ac characteristic performance requirements of 22.4.3.2 can be met if the V_{oh} vs. I_{oh} and V_{ol} vs. I_{ol} dc characteristics of the driver stay within the unshaded areas of Figure 22B–1.

The variation in output resistance of a field effect transistor (FET) due to variations in supply voltage, temperature, and process may require that a resistance be placed in series with the output of the FETs to meet this specification. The series resistance can be part of the driver circuit, or external to the driver. If the series resistance is not part of the driver circuit, the driver vendor shall specify the value of series resistance required to meet the specification. A series resistor used to meet this specification is conceptually part of the driver regardless of whether it is physically internal or external to the driver.

The propagation delay of the path between the driver and an external series resistor used to meet the specification shall not exceed 10% of the 10–90% rise/fall time of the driver.

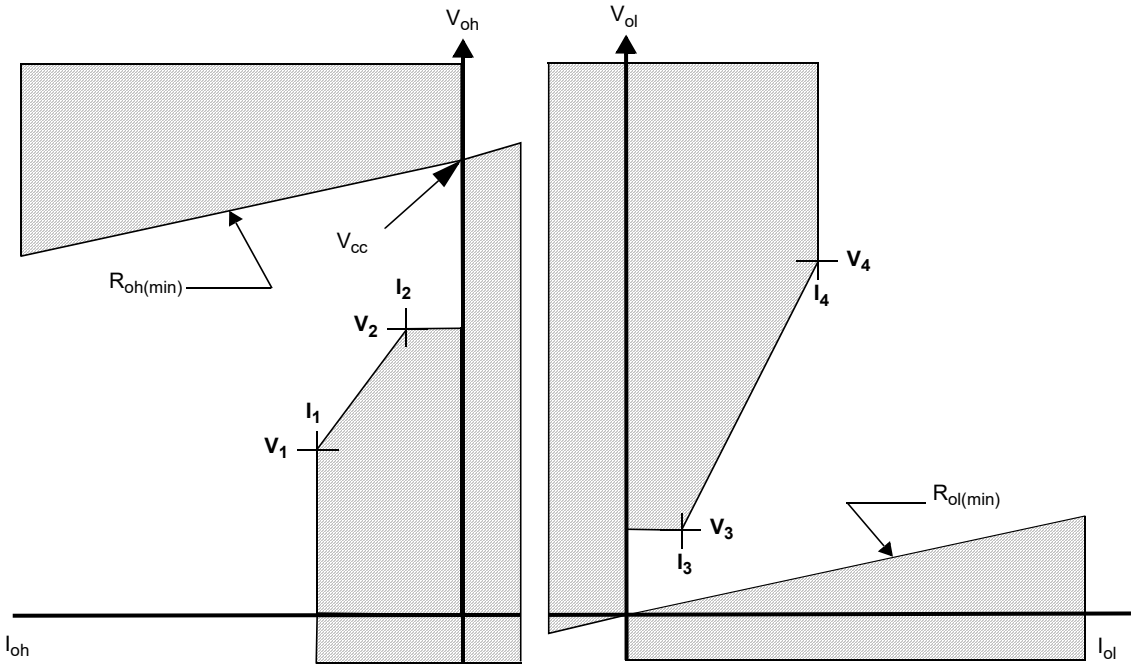

Figure 22B–1—Driver output V–I curve

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22B.2 $R_{o(min)}$ and V, I values for operation from 5 V ± 10% supply

Referring to Figure 22B–1, $R_{oh(min)}$ and $R_{ol(min)}$ both equal 40 Ω, and the values for the V-I points on the curve are given in Table 22B–1 for MII drivers that drive rail to rail from a +5 V ± 10% power supply.

Table 22B–1—Values for driver output V-I curve (5 V supply)

V–I point	I (mA)	V (V)
I_1, V_1	–20	1.10
I_2, V_2	–4	2.4
I_3, V_3	4	0.40
I_4, V_4	43	3.05

22B.3 $R_{o(min)}$ and V, I values for operation from 3.3 V ± 0.3 V supply

Referring to Figure 22B–1, $R_{oh(min)}$ and $R_{ol(min)}$ both equal 33 Ω, and the values for the V–I points on the curve are given in Table 22B–2 for MII drivers that drive rail to rail from a +3.3 V ± 0.3 V power supply.

Table 22B–2—Values for driver output V-I curve (3.3 V supply)

V-I point	I (mA)	V (V)
I_1,V_1	–20	1.10
I_2,V_2	–4	2.4
I_3,V_3	4	0.40
I_4,V_4	26	2.10

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Annex 22C

(informative)

Measurement techniques for MII signal timing characteristics

22C.1 Measuring timing characteristics of source terminated signals

The measurement of timing relationships between MII signals at the MII connector is complicated by the use of driver output impedance to control transmission line reflections on point-to-point transmission paths passing through the connector. The voltage waveforms on point-to-point transmission paths can be different at the MII connector and at the end of the paths. A clean transition (or step) from one logic state to the other at the end of a point to point path can appear as two half-steps at the MII connector.

To eliminate ambiguity as to where on a two half-step state transition to measure timing, all timing measurements on point-to-point transmission paths will be at the end of the path. In some cases, an end of path has to be artificially created.

22C.2 Measuring timing characteristics of transmit signals at the MII

The timing of TX_EN, TX_ER, and TXD<3:0> relative to TX_CLK at the MII connector is measured as follows.

Use the time base for TX_CLK as a timing reference. Break the TX_CLK path at the MII connector, forcing the TX_CLK point-to-point transmission path to end at the connector. Measure when the rising edge of TX_CLK passes through $V_{ih(min)}$ at the MII connector. Call this time T_{clk}. Reconnect the TX_CLK path at the MII connector and break the paths of TX_EN, TX_ER, and TXD<3:0> at the MII connector, forcing the paths to end at the connector. Measure when TX_EN, TX_ER, and TXD<3:0> exit the switching region at the MII connector. Call these times T_{en}, T_{er}, and $T_{<3:0>}$, respectively.

The timing relationships at the MII connector for TX_EN, TX_ER, and TXD<3:0> relative to TX_CLK are met if ($T_{en} - T_{clk}$), ($T_{er} - T_{clk}$), ($T_3 - T_{clk}$), ($T_2 - T_{clk}$), ($T_1 - T_{clk}$), and ($T_0 - T_{clk}$), respectively, meet the timing relationships specified in 22.3.1.

22C.3 Measuring timing characteristics of receive signals at the MII

The timing of RX_DV, RX_ER, and RXD<3:0> relative to RX_CLK at the MII connector is measured as follows.

Break the paths of RX_CLK, RX_DV, RX_ER, and RXD<3:0> at the MII connector, forcing the paths to end at the connector. Measure when RX_DV, RX_ER, and RXD<3:0> exit the switching region at the MII connector relative to when the rising edge of RX_CLK passes through $V_{il(max)}$). Also measure when RX_DV, RX_ER, and RXD<3:0> reenter the switching region relative to when the rising edge of RX_CLK passes through $V_{ih(min)}$.

The timing relationships at the MII connector for RX_DV, RX_ER, and RXD<3:0> relative to RX_CLK are met if the times measured in the previous step meet the timing relationships specified in 22.3.2.

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22C.4 Measuring timing characteristics of MDIO

The MDIO and MDC signal timing characteristics cannot be measured using the techniques defined for the transmit and receive signals since MDIO and MDC may connect a single station management entity to multiple PHY devices. The MDIO and MDC timing characteristics are measured with a PHY connected to the MII connector. The signal timing characteristics for MDC and MDIO have to be met over the range of conditions which occur when from one to 32 PHYs are connected to an STA. When 32 PHYs are connected to an STA, the total capacitance can be as large as 390 pF on MDC, and as large as 470 pF on MDIO.

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Annex 22D

(informative)

Clause 22 access to Clause 45 MMD registers

Clause 22 provides access to registers in a Clause 45 MMD using registers 13 and 14. This informative annex provides users with some insight how these registers can be utilized to access Clause 45 MMD registers. Accesses to registers 13 and 14, for the purpose of accessing registers in a Clause 45 MMD, should be performed atomically to avoid the chance of another process changing the Function, DEVAD or address fields within the MMD. This is the same requirement of Clause 45 accesses.

22D.1 Write operation

To write a Clause 45 register using the Clause 22 access mechanism, perform the following accesses using the appropriate PHY address for the PHY of interest:

a) To register 13, write the Function field to 00 (address) and DEVAD field to the device address value for the desired MMD;
b) To register 14, write the desired address value to the MMD's address register;
c) To register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value for the desired MMD;
d) To register 14, write the content of the MMD's selected register.

Step a) and Step b) can be skipped if the MMD's address register was previously configured.

22D.2 Read operation

To read a Clause 45 register using the Clause 22 access mechanism, perform the following accesses using the appropriate PHY address for the PHY of interest:

a) To register 13, write the Function field to 00 (address) and DEVAD field to the device address value for the desired MMD;
b) To register 14, write the desired address value to the MMD's address register;
c) To register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value for the desired MMD;
d) From register 14, read the content of the MMD's selected register.

Step a) and Step b) can be skipped if the MMD's address register was previously configured.

22D.3 MMD address operations

22D.3.1 Address

While the Function field contains the value 00 (address):

a) subsequent writes to register 14 continue to rewrite MMD DEVAD's address register;
b) subsequent reads from register 14 continue to reread MMD DEVAD's address register.

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22D.3.2 Data, no post increment

While the Function field contains the value 01 (Data, no post increment):

a) subsequent writes to register 14 continue to rewrite the data register selected by the value in MMD DEVAD's address register;
b) subsequent reads from register 14 continue to reread the data register selected by the value in MMD DEVAD's address register.

22D.3.3 Data, post increment on reads and writes

While the Function field contains the value 10 (Data, post increment on reads and writes):

a) subsequent writes to register 14 write the next higher addressed data register selected by the value in MMD DEVAD's address register, i.e. MMD DEVAD's address register is incremented after each access;
b) subsequent reads from register 14 read the next higher addressed data register selected by the value in MMD DEVAD's address register, i.e. MMD DEVAD's address register is incremented after each access.

22D.3.4 Data, post increment on writes only

While the Function field contains the value 11 (Data, post increment on writes only):

a) subsequent writes to register 14 write the next higher addressed data register selected by the value in MMD DEVAD's address register, i.e. MMD DEVAD's address register is incremented after each access;
b) subsequent reads from register 14 continue to reread the data register selected by the value in MMD DEVAD's address register.

This Function enables a read-modify-write capability for successively addressed registers within a MMD.

22D.4 PHY Coexistence and bus conflict avoidance

There are multiple levels of coexistence on the MDIO bus:

a) PHYs accessible via the Clause 22 access mechanism can coexist on the same bus using different PHY address values;
b) Ports accessible via the Clause 45 access mechanism can coexist on the same bus using different port address values;
c) PHYs accessible via the Clause 22 access mechanism can coexist on the same bus with ports accessible via the Clause 45 access mechanism, even with identical PHY/port address values due to the different ST (start of frame) encodings of the frame structures (see 45A.3 and 45A.4, which discuss the need for protocol aware voltage translators for this type of coexistence);
d) MMDs accessible via the Clause 45 access mechanism with the same port address can coexist on the same bus using different device address values.

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Annex 23A

(normative)

6T codewords

The *leftmost* ternary symbol of each 6T Code group shown in Table 23A–1 (broken into 23A–1a and 23A–1b for pagination) shall be transmitted *first.* The *leftmost* nibble of each data octet is the *most significant.*

Table 23A–1a—100BASE-T4 8B6T code table

Data octet	6T code group	Data octet	6T code group	Data octet	6T code group	Data octet	6T code group
00	+ − 0 0 + −	20	0 0 − + + −	40	+ 0 + 0 0 −	60	0 − 0 + + 0
01	0 + − + − 0	21	− − + 0 0 +	41	+ + 0 0 − 0	61	0 0 − + 0 +
02	+ − 0 + − 0	22	+ + − 0 + −	42	+ 0 + 0 − 0	62	0 − 0 + 0 +
03	− 0 + + − 0	23	+ + − 0 − +	43	0 + + 0 − 0	63	− 0 0 + 0 +
04	− 0 + 0 + −	24	0 0 + 0 − +	44	0 + + 0 0 −	64	− 0 0 + + 0
05	0 + − − 0 +	25	0 0 + 0 + −	45	+ + 0 − 0 0	65	0 0 − 0 + +
06	+ − 0 − 0 +	26	0 0 − 0 0 +	46	+ 0 + − 0 0	66	0 − 0 0 + +
07	− 0 + − 0 +	27	− − + + + −	47	0 + + − 0 0	67	− 0 0 0 + +
08	− + 0 0 + −	28	− 0 − + + 0	48	0 0 0 + 0 0	68	− + − + + 0
09	0 − + + − 0	29	− − 0 + 0 +	49	0 0 0 − + +	69	− − + + 0 +
0A	− + 0 + − 0	2A	− 0 − + 0 +	4A	0 0 0 + − +	6A	− + − + 0 +
0B	+ 0 − + − 0	2B	0 − − + 0 +	4B	0 0 0 + + −	6B	+ − − + 0 +
0C	+ 0 − 0 + −	2C	0 − − + + 0	4C	0 0 0 − + 0	6C	+ − − + + 0
0D	0 − + − 0 +	2D	− − 0 0 + +	4D	0 0 0 − 0 +	6D	− − + 0 + +
0E	− + 0 − 0 +	2E	− 0 − 0 + +	4E	0 0 0 + − 0	6E	− + − 0 + +
0F	+ 0 − − 0 +	2F	0 − − 0 + +	4F	0 0 0 + 0 −	6F	+ − − 0 + +
10	+ 0 + − − 0	30	+ − 0 0 − +	50	+ 0 + − − +	70	− + + 0 0 0
11	+ + 0 − 0 −	31	0 + − − + 0	51	+ + 0 − + −	71	+ − + 0 0 0
12	+ 0 + − 0 −	32	+ − 0 − + 0	52	+ 0 + − + −	72	+ + − 0 0 0
13	0 + + − 0 −	33	− 0 + − + 0	53	0 + + − + −	73	0 0 + 0 0 0
14	0 + + − − 0	34	− 0 + 0 − +	54	0 + + − − +	74	− 0 + 0 0 0
15	+ + 0 0 − −	35	0 + − + 0 −	55	+ + 0 + − −	75	0 − + 0 0 0
16	+ 0 + 0 − −	36	+ − 0 + 0 −	56	+ 0 + + − −	76	+ 0 − 0 0 0
17	0 + + 0 − −	37	− 0 + + 0 −	57	0 + + + − −	77	0 + − 0 0 0
18	0 + − 0 + −	38	− + 0 0 − +	58	+ + + 0 − −	78	0 − − + + +
19	0 + − 0 − +	39	0 − + − + 0	59	+ + + − 0 −	79	− 0 − + + +
1A	0 + − + + −	3A	− + 0 − + 0	5A	+ + + − − 0	7A	− − 0 + + +
1B	0 + − 0 0 +	3B	+ 0 − − + 0	5B	+ + 0 − − 0	7B	− − 0 + + 0
1C	0 − + 0 0 +	3C	+ 0 − 0 − +	5C	+ + 0 − − +	7C	+ + − 0 0 −
1D	0 − + + + −	3D	0 − + + 0 −	5D	+ + 0 0 0 −	7D	0 0 + 0 0 −
1E	0 − + 0 − +	3E	− + 0 + 0 −	5E	− − + + + 0	7E	+ + − − − +
1F	0 − + 0 + −	3F	+ 0 − + 0 −	5F	0 0 − + + 0	7F	0 0 + − − +

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Table 23A–1b—100BASE-T4 8B6T code table

Data octet	6T code group	Data octet	6T code group	Data octet	6T code group	Data octet	6T code group
80	+ − + 0 0 −	A0	0 − 0 + + −	C0	+ − + 0 + −	E0	+ − 0 + + −
81	+ + − 0 − 0	A1	0 0 − + − +	C1	+ + − + − 0	E1	0 + − + − +
82	+ − + 0 − 0	A2	0 − 0 + − +	C2	+ − + + − 0	E2	+ − 0 + − +
83	− + + 0 − 0	A3	− 0 0 + − +	C3	− + + + − 0	E3	− 0 + + − +
84	− + + 0 0 −	A4	− 0 0 + + −	C4	− + + 0 + −	E4	− 0 + + + −
85	+ + − − 0 0	A5	0 0 − − + +	C5	+ + − − 0 +	E5	0 + − − + +
86	+ − + − 0 0	A6	0 − 0 − + +	C6	+ − + − 0 +	E6	+ − 0 − + +
87	− + + − 0 0	A7	− 0 0 − + +	C7	− + + − 0 +	E7	− 0 + − + +
88	0 + 0 0 0 −	A8	− + − + + −	C8	0 + 0 0 + −	E8	− + 0 + + −
89	0 0 + 0 − 0	A9	− − + + − +	C9	0 0 + + − 0	E9	0 − + + − +
8A	0 + 0 0 − 0	AA	− + − + − +	CA	0 + 0 + − 0	EA	− + 0 + − +
8B	+ 0 0 0 − 0	AB	+ − − + − +	CB	+ 0 0 + − 0	EB	+ 0 − + − +
8C	+ 0 0 0 0 −	AC	+ − − + + −	CC	+ 0 0 0 + −	EC	+ 0 − + + −
8D	0 0 + − 0 0	AD	− − + − + +	CD	0 0 + − 0 +	ED	0 − + − + +
8E	0 + 0 − 0 0	AE	− + − − + +	CE	0 + 0 − 0 +	EE	− + 0 − + +
8F	+ 0 0 − 0 0	AF	+ − − − + +	CF	+ 0 0 − 0 +	EF	+ 0 − − + +
90	+ − + − − +	B0	0 − 0 0 0 +	D0	+ − + 0 − +	F0	+ − 0 0 0 +
91	+ + − − + −	B1	0 0 − 0 + 0	D1	+ + − − + 0	F1	0 + − 0 + 0
92	+ − + − + −	B2	0 − 0 0 + 0	D2	+ − + − + 0	F2	+ − 0 0 + 0
93	− + + − + −	B3	− 0 0 0 + 0	D3	− + + − + 0	F3	− 0 + 0 + 0
94	− + + − − +	B4	− 0 0 0 0 +	D4	− + + 0 − +	F4	− 0 + 0 0 +
95	+ + − + − −	B5	0 0 − + 0 0	D5	+ + − + 0 −	F5	0 + − + 0 0
96	+ − + + − −	B6	0 − 0 + 0 0	D6	+ − + + 0 −	F6	+ − 0 + 0 0
97	− + + + − −	B7	− 0 0 + 0 0	D7	− + + + 0 −	F7	− 0 + + 0 0
98	0 + 0 − − +	B8	− + − 0 0 +	D8	0 + 0 0 − +	F8	− + 0 0 0 +
99	0 0 + − + −	B9	− − + 0 + 0	D9	0 0 + − + 0	F9	0 − + 0 + 0
9A	0 + 0 − + −	BA	− + − 0 + 0	DA	0 + 0 − + 0	FA	− + 0 0 + 0
9B	+ 0 0 − + −	BB	+ − − 0 + 0	DB	+ 0 0 − + 0	FB	+ 0 − 0 + 0
9C	+ 0 0 − − +	BC	+ − − 0 0 +	DC	+ 0 0 0 − +	FC	+ 0 − 0 0 +
9D	0 0 + + − −	BD	− − + + 0 0	DD	0 0 + + 0 −	FD	0 − + + 0 0
9E	0 + 0 + − −	BE	− + − + 0 0	DE	0 + 0 + 0 −	FE	− + 0 + 0 0
9F	+ 0 0 + − −	BF	+ − − + 0 0	DF	+ 0 0 + 0 −	FF	+ 0 − + 0 0

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Annex 23B

(informative)

Noise budget

Worst-case values for noise effects in the 100BASE-T4 system are as shown in Tables 23B–1 and 23B–2.

Table 23B–1—Carrier presence analysis

Received signal peak amplitude (min.)	792 mVp
NEXT noise	325 mVp

Table 23B–2—Far-end signal analysis

Received signal peak amplitude (min.)	796 mVp
Baseline wander	14 mVp
ISI	80 mVp
Reflections	60 mVp
FEXT noise	87 mVp

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Annex 23C

(informative)

Use of cabling systems with a nominal differential characteristic impedance of 120 Ω

The 100BASE-T4 standard specifies only the use of 100 Ω link segments for conformance. Since ISO/IEC 11801: 1995 also recognizes 120 Ω cabling, this informative annex specifies the conditions for using cabling systems with a nominal characteristic impedance of 120 Ω by 100BASE-T4 conformant stations.

The use of cables with a characteristic impedance outside the range specified in 23.6 will generally increase the mismatching effects in the link components, inducing additional noise in the received signals.

In particular, the use of a homogeneous link segment having a characteristic impedance of 120 Ω ±15 Ω over the frequency band 1 to 16 MHz may add up to 1.4% of additional noise to the signals at the input of the receivers (worst-case short-length link segment).

Therefore, in order to keep the overall noise (MDFEXT + reflections) at the same value as for a 100 Ω link segment when using a 120 Ω link segment, the minimum ELFEXT loss requirement for the cable has to be increased by 2 dB (i.e., from 23 dB to 25 dB at 12.5 MHz, see 23.6.3.2). Accordingly, the MDFEXT noise requirement shall be decreased from 87 mV peak to 69 mV peak. In practice, this means that cables rated category 4 or higher, as specified in ISO/IEC 11801: 1995, are required when 120 Ω cables are used with 100BASE-T4 compliant PMDs.

NOTE 1—The use of 100 Ω cords at end points in conjunction with 120 Ω premises cabling may be tolerated provided that all the components of the link are of Category 5, as defined in ISO/IEC 11801: 1995.

NOTE 2—The use of 100 Ω cords at any intermediate cross-connect points on 120 Ω links as well as the use of 120 Ω cords in conjunction with 100 Ω premises cabling is not allowed since it would result in worst-case jitter greater than that allowed in this standard.

CAUTION

Users of this annex are further advised to check with the manufacturer of the particular 100BASE-T4 couplers they intend to use with a 120 Ω link to see whether those couplers can operate correctly on cables with Z_c as high as 120 Ω ± 15 Ω.

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Annex 27A

(normative)

Repeater delay consistency requirements

Proper operation of the network requires that repeaters do not cause the interpacket gap (IPG) to disappear by propagating the end of any carrier event to different output ports with greatly different delay times. Maximum port-to-port delays have been assigned as absolute delays to meet requirements for detection of collision within a slot time and limiting the length of collision fragments to less than minimum frame size. To avoid specification of minimum input-to-output propagation time as absolute values that reduce implementation flexibility, these delays are instead implied by imposing a triangular delay inequality relationship.

Consider three ports {A, B, C}. Using the notation SOP(xy) to mean the start-of-packet delay for an input at port x to resulting output on port y, repeaters shall achieve this relationship for all groups of three ports within a repeater set:

SOP(AC) < SOP(AB) + SOP(BC)

Following a frame transmitted by node A that propagates to nodes B and C, this constraint ensures that node B cannot complete an IPG timer and initiate a transmission that arrives at node C before node C has also advanced its own IPG timer sufficiently that a pending frame can contend for access to the network.

There is a second delay consistency requirement, one that relates to jam propagation by repeaters. Using a notation similar to that above, SOJ(xy) stands for the start-of-jam propagation delay from port x to port y and EOJ(xy) for the end-of-jam delay between same two ports.

To ensure proper detection of collisions and avoid generation of fragments that exceed minimum frame size, maximum values have been imposed on SOJ and EOJ delays through repeaters. No specific minima have been specified as all delays less than the maxima meet the collision detection and fragment length criteria. To prevent the jam pattern from shrinking excessively as it propagates through repeaters, repeaters shall meet this relationship between all pairs of ports:

EOJ(AB) >= SOJ(AB) – 4 bit times

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Annex 28A

(normative)

Selector Field definitions

The Selector Field, S[4:0] in the link codeword, shall be used to identify the type of message being sent by Auto-Negotiation. The following table identifies the types of messages that may be sent. As new messages are developed, this table will be updated accordingly.

The Selector Field uses a 5-bit binary encoding, which allows 32 messages to be defined. All unspecified combinations are reserved. Reserved combinations shall not be transmitted.

Table 28A–1—Selector Field value mappings

S4	S3	S2	S1	S0	Selector description
0	0	0	0	0	Reserved for future Auto-Negotiation development
0	0	0	0	1	IEEE Std 802.3
0	0	0	1	0	IEEE Std 802.9a-1995 (withdrawn)
0	0	0	1	1	IEEE Std 802.5v-2001 (withdrawn)
0	0	1	0	0	IEEE Std 1394
0	0	1	0	1	INCITS
0	0	1	1	X	Reserved for future Auto-Negotiation development
0	1	X	X	X	Reserved for future Auto-Negotiation development
1	X	X	X	X	Reserved for future Auto-Negotiation development

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Annex 28B

(normative)

IEEE 802.3 Selector Base Page definition

This annex provides the Technology Ability Field bit assignments, Priority Resolution table, and Message Page transmission conventions relative to the IEEE 802.3 Selector Field value within the Base Page encoding for devices using Clause 28 Auto-Negotiation.

As new IEEE 802.3 LAN technologies are developed, a reserved bit in the Technology Ability field may be assigned to each technology by the standards body.

The new technology will then be inserted into the Priority Resolution hierarchy and made a part of the Auto-Negotiation standard. The relative hierarchy of the existing technologies will not change, thus providing backward compatibility with existing Auto-Negotiation implementations.

It is important to note that the reserved bits are required to be transmitted as logic zeros. This guarantees that devices implemented using the current priority table will be forward compatible with future devices using an updated priority table.

28B.1 Selector field value

The value of the IEEE 802.3 Selector Field is S[4:0] = 00001.

28B.2 Technology Ability Field bit assignments

The Technology bit field consists of bits D5 through D11 (A0–A6, respectively) in the IEEE 802.3 Selector Base Page. Table 28B–1 summarizes the bit assignments.

Note that the order of the bits within the Technology Ability Field has no relationship to the relative priority of the technologies.

Setting Bit A5 or Bit A6 indicates that the DTE has implemented both the optional MAC control sublayer and the PAUSE function as specified in Clause 31 and Annex 31B. This capability is significant only when the link is configured for full duplex operation, regardless of data rate and medium. The encoding of Bits A5 and A6 is specified in Table 28B–2.

Table 28B–1—Technology Ability Field bit assignments

Bit	Technology	Minimum cabling requirement
A0	10BASE-T	Two-pair Category 3
A1	10BASE-T full duplex	Two-pair Category 3
A2	100BASE-TX	Two-pair Category 5
A3	100BASE-TX full duplex	Two-pair Category 5

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Table 28B–1—Technology Ability Field bit assignments

Bit	Technology	Minimum cabling requirement
A4	100BASE-T4	Four-pair Category 3
A5	PAUSE operation for full duplex links	Not applicable
A6	Asymmetric PAUSE operation for full duplex Links	Not applicable

Table 28B–2—Pause encoding

PAUSE (A5)	ASM_DIR (A6)	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. The ASM_DIR bit indicates that asymmetric PAUSE is supported. The value of the PAUSE bit when the ASM_DIR bit is set indicates the direction the PAUSE frames are supported for flow across the link. Asymmetric PAUSE configuration results in independent enabling of the PAUSE receive and PAUSE transmit functions as defined by Annex 31B. See 28B.3 regarding PAUSE configuration resolution.

28B.3 Priority resolution

Since two devices may have multiple abilities in common, a prioritization scheme exists to ensure that the highest common denominator ability is chosen. The following list shall represent the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value, where priorities are listed from highest to lowest.

a) 40GBASE-T full duplex
b) 25GBASE-T full duplex
c) 10GBASE-T full duplex
d) 5GBASE-T full duplex
e) 2.5GBASE-T full duplex
f) 1000BASE-T full duplex
g) 1000BASE-T
h) 100BASE-T2 full duplex
i) 100BASE-TX full duplex
j) 100BASE-T2
k) 100BASE-T4
l) 100BASE-TX
m) 10BASE-T full duplex
n) 10BASE-T

The rationale for this hierarchy is straightforward. First, higher rates are always higher in priority than lower rates. Second, full duplex solutions are always higher in priority than their half duplex counterparts. Third, higher priority is given to PHY types that run on broader spectrum of copper cabling. 100BASE-T2 is ahead of 100BASE-TX and 100BASE-T4 because 100BASE-T2 runs across a broader spectrum of copper cabling and can support a wider base of configurations. 100BASE-T4 is ahead of 100BASE-TX because 100BASE-

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T4 runs across a broader spectrum of copper cabling. The relative order of the technologies specified herein shall not be changed. As each new technology is added, it shall be inserted into its appropriate place in the list, shifting technologies of lesser priority lower in priority. If a vendor-specific technology is implemented, the priority of all IEEE 802.3 standard technologies shall be maintained, with the vendor specific technology inserted at any appropriate priority location.

NOTE—Refer to 28.2.1.2.3 for resolution of Extended Next Pages.

The use of the PAUSE operation for full duplex links (as indicated by bits A5 and A6) is orthogonal to the negotiated data rate, medium, or link technology. The setting of these bits indicates the availability of additional DTE capability when full duplex operation is in use. The PAUSE function shall be enabled according to Table 28B–3 only if the highest common denominator is a full duplex technology. There is no priority resolution associated with the PAUSE operation.

Table 28B–3—Pause resolution

Local device		Link partner		Local device resolution	Link partner resolution
PAUSE	**ASM_DIR**	**PAUSE**	**ASM_DIR**		
0	0	Don’t care	Don’t care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	0	Don’t care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	1	Enable PAUSE transmit Disable PAUSE receive	Enable PAUSE receive Disable PAUSE transmit
1	0	0	Don’t care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	Don’t care	1	Don’t care	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive
1	1	0	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	1	0	1	Enable PAUSE receive Disable PAUSE transmit	Enable PAUSE transmit Disable PAUSE receive

28B.4 Message Page transmission convention

Each series of Unformatted Pages shall be preceded by a Message Page containing a message code that defines how the following Unformatted Pages will be used.

Next Page message codes should be allocated globally across Selector Field values so that meaningful communication is possible between technologies using different Selector Field values.

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Annex 28C

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Next Page Message Code field definitions

This Annex defines the Next Page message code fields for devices using Clause 28 Auto-Negotiation. The Message Code Field of a message page used in Next Page exchange shall be used to identify the meaning of a message. The following table identifies the types of messages that may be sent. As new messages are developed, this table will be updated accordingly.

The Message Code Field uses an 11-bit binary encoding that allows 2048 messages to be defined. All message codes not specified shall be reserved for IEEE use or allocation. Devices that have negotiated Extended Next Page support transmit Extended Next Pages but not other Next Pages.

Extended Next Pages are used to transmit Extended Next Page message codes and the subsequent Extended Next Pages and extended Unformatted Pages. In addition, Extended Next Pages may be used to transmit multiple Message Pages and Unformatted Pages in the following manner. The Message Code Field is mapped to bits M0:10 of the extended Message Page, and the first two Unformatted Code Fields associated with the Message Code Field value are mapped to bits U0:U10 and U16:U26, respectively, of the extended Message Page. Additional Unformatted Code Fields would be mapped to bits U0:U42 of subsequent extended Unformatted Pages. Any unused bits in the Extended Next Pages are transmitted as zero and ignored by the receiver.

If more than two Unformatted Code fields are required by a message code, then additional Unformatted Code Fields are transmitted in the extended Unformatted Pages immediately following the extended Message Page. Up to three Unformatted Code Fields can be transmitted in each extended Unformatted Page, the first in bits U0:10, the second in bits U11:21, and the third in bits U27:37.

When a message code requires the transmission of one or more extended Unformatted Pages, due to the number of Unformatted Code Fields it defines, the Unformatted Code Fields in the extended Message and extended Unformatted Pages shall be in the order specified by the message code.

Table 28C–1—Message code field values

Message code	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message code description
0	0	0	0	0	0	0	0	0	0	0	0	Reserved for future Auto-Negotiation use
1	0	0	0	0	0	0	0	0	0	0	1	Null Message
2	0	0	0	0	0	0	0	0	0	1	0	One UP with Technology Ability Field follows
3	0	0	0	0	0	0	0	0	0	1	1	Two UPs with Technology Ability Field follow
4	0	0	0	0	0	0	0	0	1	0	0	One UP with Binary coded Remote fault follows
5	0	0	0	0	0	0	0	0	1	0	1	Organizationally Unique Identifier Tagged Message

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Table 28C–1—Message code field values *(continued)*

Message code	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message code description
6	0	0	0	0	0	0	0	0	1	1	0	PHY Identifier Tag Code
7	0	0	0	0	0	0	0	0	1	1	1	100BASE-T2 Technology message code. 100BASE-T2 Ability Page to follow using Unformatted Next Page
8	0	0	0	0	0	0	0	1	0	0	0	1000BASE-T Technology message code. Two 1000BASE-T Ability Pages to follow using Unformatted Next Pages.
9	0	0	0	0	0	0	0	1	0	0	1	MultiGBASE-T and 1000BASE-T Technology message code (Extended Next Page)
10	0	0	0	0	0	0	0	1	0	1	0	EEE Technology Message Code. EEE capability to follow using Unformatted Next Page.
11	0	0	0	0	0	0	0	1	0	1	1	Organizationally Unique Identifier Tagged Message (Extended Next Page)
12.....	0	0	0	0	0	0	0	1	1	0	0	Reserved for future Auto-Negotiation use
.....2047	1	1	1	1	1	1	1	1	1	1	1	Reserved for future Auto-Negotiation use

28C.1 Message code 0—Auto-Negotiation reserved code 1

This code is reserved for future Auto-Negotiation function enhancements. Devices shall not transmit this code.

28C.2 Message code 1—Null Message code

The Null Message code shall be transmitted during Next Page exchange when the Local Device has no further messages to transmit and the Link Partner is still transmitting valid Next Pages. See 28.2.3.4 for more details.

28C.3 Message code 2—Technology Ability extension code 1

This message code is reserved for future expansion of the Technology Ability Field and indicates that a defined user code with a specific Technology Ability Field encoding follows.

28C.4 Message code 3—Technology Ability extension code 2

This message code is reserved for future expansion of the Technology Ability Field and indicates that two defined user codes with specific Technology Ability Field encodings follow.

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28C.5 Message code 4—Remote fault number code

This message code shall be followed by a single user code whose encoding specifies the type of fault that has occurred. The following user codes are defined:

0: RF Test
This code can be used to test Remote Fault operation.
1: Link Loss
2: Jabber
3: Parallel Detection Fault
This code may be sent to identify when bit 6.4 is set.

28C.6 Message code 5—Organizationally Unique Identifier (OUI) tag code

The OUI Tagged Message shall consist of a single message code of 0000 0000 0101 followed by four user codes defined as follows. The first user code shall contain the most significant 11 bits of the OUI or CID (bits 23:13) with the most significant bit in bit 10 of the user code. The second user code shall contain the next most significant 11 bits of the OUI or CID (bits 12:2) with the most significant bit in bit 10 of the user code. The third user code shall contain the remaining least significant 2 bits of the OUI or CID (bits 1:0) with the most significant bit in bit 10 of the user code. Bits 8:0 of the third user code contain a user-defined user code value that is specific to the OUI or CID transmitted. The fourth and final user code shall contain a user-defined user code value that is specific to the OUI or CID transmitted.

For example, assume that a manufacturer's IEEE-assigned OUI/CID value is AC-DE-48 and the manufacturer-selected user-defined user code associated with the OUI or CID is 0xCE1FC (binary 1100 1110 0001 1111 1100). The message code values generated from these two numbers is encoded into four message codes, as specified in Figure 28C–1. For clarity, the position of the M bit[271] is illustrated.

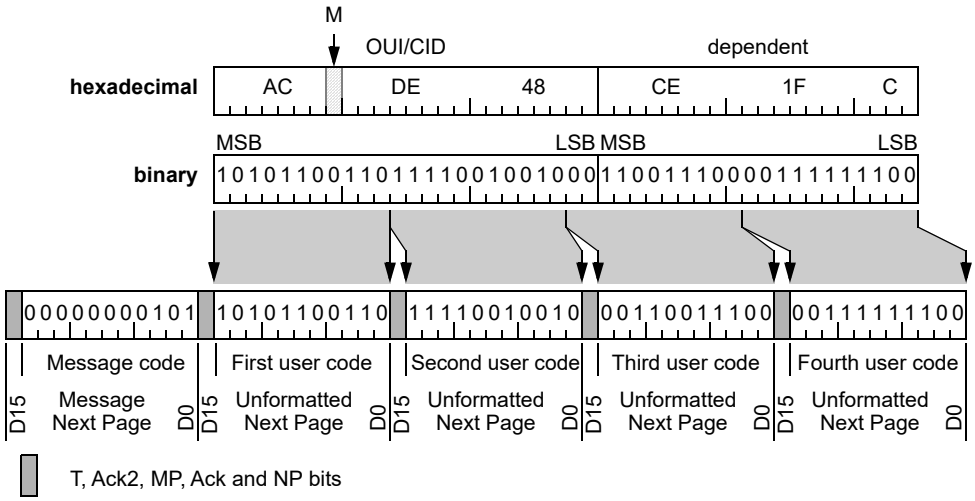

Figure 28C–1—Message code 5 sequence

NOTE—Figure 28C–1 shows the order Next Pages are transmitted, with the first transmitted Next Page shown in the leftmost position. While Figure 28–11 and Figure 28–12 use the convention that the most significant bit (i.e., the last bit to be transmitted) is the rightmost bit, Figure 28C–1 uses the opposite convention, i.e., the most significant bit of each

[271] See IEEE Std 802, subclause 9.3.

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page is shown in the leftmost position. This is a pictorial difference only; there is no difference in the actual order of bits transmitted.

Devices that negotiate the use of Extended Next Page messages may use this message encapsulated within the Extended Next Page message as described in Annex 28C, however it is recommended that devices use message code 11 for Extended Next Page OUI tagged messages.

28C.7 Message code 6—PHY identifier tag code

The PHY ID tag code message shall consist of a single message code of 0000 0000 0110 followed by four user codes defined as follows. The first user code shall contain the most significant 11 bits of the PHY ID (2.15:5) with the most significant bit in bit 10 of the user code. The second user code shall contain bits 2.4:0 to 3.15:10 of the PHY ID with the most significant bit in bit 10 of the user code. The third user code shall contain bits 3.9:0 of the PHY ID with the most significant bit in bit 10 of the user code. Bit 0 in the third user code shall contain a user-defined user code value that is specific to the PHY ID transmitted. The fourth and final user code shall contain a user-defined user code value that is specific to the PHY ID transmitted.

28C.8 Message code 2047—Auto-Negotiation reserved code 2

This code is reserved for future Auto-Negotiation function enhancements. Devices shall not transmit this code.

28C.9 Message code 7—100BASE-T2 technology message code

Clause 32 (100BASE-T2) uses Next Page message code 7 to indicate that T2 implementations will follow the transmission of this page [the initial, Message (formatted) Next Page] with two Unformatted Next Pages which contain information defined in 32.5.4.2.

28C.10 Message code 8—1000BASE-T technology message code

Clause 40 (1000BASE-T) uses Next Page message code 8 to indicate that 1000BASE-T implementations will follow the transmission of this page [the initial, Message (formatted) Next Page] with two Unformatted Next Pages that contain information defined in 40.5.1.2.

28C.11 Message code 9—MultiGBASE-T and 1000BASE-T technology message code

Clause 55 (10GBASE-T), Clause 126 (2.5G/5GBASE-T), and Clause 113 (25GBASE-T and 40GBASE-T) use Extended Next Page message code 9 to indicate that 40GBASE-T, 25GBASE-T, 2.5G/5GBASE-T, 10GBASE-T, and 1000BASE-T abilities are contained within this Extended Next Page. The Next Page that contains this information is defined in 55.6.1, 113.6.1, and 126.6.1. This page shall not be sent if Extended Next Page mode is disabled.

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28C.12 Message code 10—EEE technology message code

Multiple clauses use Next Page message code 10 to indicate that EEE technology messages will follow the transmission of this page [the initial, Message (formatted) Next Page] with one Unformatted Next Page. The contents of the unformatted code field bits (U10:U0) shall be as defined in 45.2.7.14.

EEE capability negotiation is defined in 78.3.

28C.13 Message code 11—Organizationally Unique Identifier Tagged Message (Extended Next Page)

Devices that negotiate the use of Extended Next Page messages may use the Extended Next Page OUI Tagged Message. This shall consist of a single message code of 000 0000 1011 and bits U23-U0 of the unformatted code field shall contain the OUI or CID (with most significant bit of the OUI or CID in U23, the second most significant bit in U22, etc.). Bits U31-U24 contain user-defined data. If the Next Page flag is set, the message page shall be followed by an unformatted Extended Next Page containing user-defined data.

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Annex 28D

(normative)

Description of extensions to Clause 28 and associated annexes

28D.1 Introduction

This annex is to be used to document extensions and modifications to Clause 28 required by IEEE 802.3 clauses and other standards that use Auto-Negotiation and that were approved after July 1995. It provides a single location to define such extensions and modifications without changing the basic contents of Clause 28.

Subclause 28D.2 lists those clauses and standards that require extensions to Clause 28 and provides pointers to the subclauses where those extensions are listed.

28D.2 Extensions to Clause 28

28D.2.1 Extensions required for Clause 31 (full duplex)

Clause 31 (full duplex) requires the use of Auto-Negotiation. Extensions to Clause 28 and associated annexes required for the correct operation of full duplex are shown in 28D.3.

28D.2.2 Extensions required for Clause 32 (100BASE-T2)

Clause 32 (100BASE-T2) requires the use of Auto-Negotiation. Extensions to Clause 28 required for correct operation of 100BASE-T2 are shown in 28D.4.

28D.3 Extensions for Clause 31

Full duplex requires the use of bit A5 in the Technology Ability Field of the IEEE 802.3 Selector Base Page. (This bit is also defined as MII bit 4.10.) This bit was previously defined as “reserved for future technology.”

Bit	Technology	Minimum cabling requirement
A5	PAUSE operation for full duplex links	Not applicable

Bit A5 (PAUSE operation for full duplex links) signifies that the DTE has implemented both the optional MAC Control sublayer and the PAUSE function as specified in Clause 31 and Annex 31B. This capability is significant only when the link is configured for full duplex operation, regardless of data rate and medium.

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28D.4 Extensions for Clause 32 (100BASE-T2)

Clause 32 (100BASE-T2) makes special use of Auto-Negotiation and requires additional MII registers. This use is summarized below. Details are provided in 32.5.

Auto-Negotiation is mandatory for 100BASE-T2 (32.1.3.4).

100BASE-T2 introduces the concept of MASTER and SLAVE to define DTEs and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER/SLAVE status (32.5.4.3).

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

100BASE-T2 uses unique Next Page transmit and receive registers (MII registers 8, 9, and 10) in conjunctions with Auto-Negotiation. These registers are in addition to registers 0–7 as defined in 28.2.4 (32.5.2).

100BASE-T2 use of Auto-Negotiation generates information which is stored in configuration and status bits defined for the MASTER-SLAVE Control register (MII register 9) and the MASTER-SLAVE Status register (MII register 10).

100BASE-T2 requires an ordered exchange of Next Page messages (32.5.1).

100BASE-T2 parameters are configured based on information provided by the ordered exchange of Next Page messages.

100BASE-T2 adds new message codes to be transmitted during Auto-Negotiation (32.5.4.2).

100BASE-T2 adds 100BASE-T2 full duplex and half duplex capabilities to the priority resolution table (28B.3) and MII Status Register (22.2.4.2).

T2 is defined as a valid value for “x” in 28.3.1 (e.g., link_status_T2). T2 represents that the 100BASE-T2 PMA is the signal source.

28D.5 Extensions required for Clause 40 (1000BASE-T)

Clause 40 (1000BASE-T) makes special use of Auto-Negotiation and requires additional MII registers. This use is summarized below. Details are provided in 40.5.

a) Auto-Negotiation is mandatory for 1000BASE-T (see 40.5.1).
b) 1000BASE-T requires an ordered exchange of Next Page messages (see 40.5.1.2), or optionally an exchange of an Extended Next Page message
c) 1000BASE-T parameters are configured based on information provided by the exchange of Next Page messages.
d) 1000BASE-T uses MASTER and SLAVE to define PHY operations and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER-SLAVE status (see 40.5.2).
e) 1000BASE-T transmits and receives Next Pages for exchange of information related to MASTER-SLAVE operation. The information is specified in MII registers 9 and 10 (see 32.5.2 and 40.5.1.1), which are required in addition to registers 0-8 as defined in 28.2.4.
f) 1000BASE-T adds new message codes to be transmitted during Auto-Negotiation (see 40.5.1.3).
g) 1000BASE-T adds 1000BASE-T full duplex and half duplex capabilities to the priority resolution table (see 28B.3) and MII Extended Status Register (see 22.2.2.4).

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h) 1000BASE-T is defined as a valid value for "x" in 28.3.1 (e.g., link_status_1GigT.) 1GigT represents that the 1000BASE-T PMA is the signal source.
i) 1000BASE-T supports Asymmetric Pause as defined in Annex 28B.

28D.6 Extensions required for Clause 55 (10GBASE-T)

Clause 55 (10GBASE-T) makes special use of Auto-Negotiation and requires additional MDIO registers. This use is summarized below. Details are provided in 55.6.

a) Auto-Negotiation is mandatory for 10GBASE-T.
b) Extended Next Page support is mandatory for 10GBASE-T.
c) 10GBASE-T requires an exchange of an Extended Next Page message.
d) 10GBASE-T parameters are configured based on information provided by the exchange of an Extended Next Page message.
e) 10GBASE-T uses MASTER and SLAVE to define PHY operations and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER-SLAVE status.
f) 10GBASE-T transmits and receives an Extended Next Page for exchange of information related to MASTER-SLAVE operation. The information is specified in 45.2.7.
g) 10GBASE-T adds new message codes to be transmitted during Auto-Negotiation.
h) 10GBASE-T adds 10GBASE-T full duplex capabilities to the priority resolution table (see 28B.3).
i) 10GBASE-T is defined as a valid value for "x" in 28.3.1 (e.g., link_status_10GigT.) 10GigT represents that the 10GBASE-T PMA is the signal source.
j) 10GBASE-T supports Asymmetric Pause as defined in Annex 28B.

28D.7 Extensions required for Energy-Efficient Ethernet (Clause 78)

Energy-Efficient Ethernet (Clause 78) makes use of Auto-Negotiation and requires additional MDIO registers. Auto-negotiation is mandatory for all EEE PHYs that support LPI. Details are provided in 78.3.

28D.8 Extensions required for Clause 113 (25GBASE-T and 40GBASE-T)

Clause 113 (25GBASE-T and 40GBASE-T) makes special use of Auto-Negotiation and defines additional MDIO registers for use when Clause 45 is implemented. This use is summarized below. Details are provided in 113.6.

a) Auto-Negotiation is mandatory for 25GBASE-T and 40GBASE-T.
b) Extended Next Page support is mandatory for 25GBASE-T and 40GBASE-T.
c) 25GBASE-T and 40GBASE-T require an exchange of an Extended Next Page message.
d) 25GBASE-T and 40GBASE-T parameters are configured based on information provided by the exchange of an Extended Next Page message.
e) 25GBASE-T and 40GBASE-T use MASTER and SLAVE to define PHY operations and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER-SLAVE status.
f) 25GBASE-T and 40GBASE-T transmit and receive an Extended Next Page for exchange of information related to MASTER-SLAVE operation. The information is specified in 45.2.7.
g) 25GBASE-T and 40GBASE-T add 25GBASE-T and 40GBASE-T full duplex capabilities to the priority resolution table (see 28B.3).
h) 25GBASE-T and 40GBASE-T are defined as a valid value for "x" in 28.3.1 (e.g., link_status_25GigT and link_status_40GigT). 25GigT represents that the 25GBASE-T PMA is the signal source, and 40GigT represents that the 40GBASE-T PMA is the signal source.
i) 25GBASE-T and 40GBASE-T support Asymmetric Pause as defined in Annex 28B.

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28D.9 Extensions required for Clause 126 (2.5G/5GBASE-T)

Clause 126 (2.5G/5GBASE-T) makes special use of Auto-Negotiation and defines additional MDIO registers for use when Clause 45 is implemented. This use is summarized in the following list. Details are provided in 126.6.

a) Auto-Negotiation is mandatory for 2.5BASE-T and 5GBASE-T.
b) Extended Next Page support is mandatory for 2.5BASE-T and 5GBASE-T.
c) 2.5GBASE-T and 5GBASE-T require an exchange of an Extended Next Page message.
d) 2.5GBASE-T and 5GBASE-T parameters are configured based on information provided by the exchange of an Extended Next Page message and information provided by the exchange of Infofields during link training.
e) 2.5GBASE-T and 5GBASE-T use MASTER and SLAVE to define PHY operations and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER-SLAVE status.
f) 2.5GBASE-T and 5GBASE-T transmit and receive an Extended Next Page for exchange of information related to MASTER-SLAVE operation. The information is specified in 45.2.7.
g) 2.5GBASE-T and 5GBASE-T add 2.5GBASE-T and 5GBASE-T full duplex capabilities to the priority resolution table (see 28B.3).
h) 2.5GBASE-T and 5GBASE-T are defined as valid values for “x” in 28.3.1 (e.g., link_status_2p5GigT or link_status_5GigT.) 2p5GigT represents that the 2.5GBASE-T PMA is the signal source, and 5GigT represents that the 5GBASE-T PMA is the signal source.
i) 2.5GBASE-T and 5GBASE-T support Asymmetric Pause as defined in Annex 28B.

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Annex 29A

(informative)

DTE and repeater delay components

29A.1 DTE delay

Round-trip DTE delay = MAC transmit start to MDI output
+ MDI input to MDI output (worst case, nondeferred)
+ MDI input to collision detect

NOTE 1—Refer to Clause 23, Clause 24, Clause 25, and Clause 26.

NOTE 2—Worst-case values are used for the one T4 and one TX/FX value shown in Table 29–3. (TX/FX values for MAC transmit start and MDI input to collision detect; T4 value for MDI input to MDI output.)

29A.2 Repeater delay

Repeater delay= SOP (start-of-packet propagation delay)
+ SOJ (start-of-jam propagation delay)

NOTE—Refer to Clause 27.

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Annex 29B

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Recommended topology documentation

It is strongly recommended that detailed records documenting the topology components of 100BASE-T networks be prepared and maintained to facilitate subsequent modification. Proper 100BASE-T topology design requires an accurate knowledge of link segment and hub parameters to ensure proper operation of single and multisegment, single collision domain networks. Link segment documentation is site-specific and requires careful documentation. It is recommended that the information shown in Table 29B–1 be collected for each link segment and archived for future reference. Hub performance parameters may be obtained from manufacturer documentation.

Table 29B–1—Recommended link segment documentation

	Horizontal wiring (wiring closet, from punch-down block to end station wall plate)	MII cable(s)	Wiring closet patch cord	End station connecting cable
Length				
Type (e.g., Category 3)				
Cable manufacturer				
Cable code/id (from manufacturer)				
Cable delay (in bit times per meter)				

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Annex 30A

(normative)

GDMO specification for IEEE 802.3 managed object classes

NOTE—The GDMO specification was moved to IEEE Std 802.3.1-2011.

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Annex 30B

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GDMO and ASN.1 definitions for management

NOTE—The GDMO specification was moved to IEEE Std 802.3.1-2011 Clause C.1 Common attributes template.

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Annex 30C

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SNMP MIB definitions for Link Aggregation

NOTE—The SNMP for Link Aggregation specification was moved to IEEE Std 802.1AX-2008.

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Annex 31A

(normative)

MAC Control opcode assignments

Table 31A–1 shows the currently defined opcode values and interpretations:

Table 31A–1—MAC Control opcodes

Opcode (Hexadecimal)	MAC Control function	Specified in	Value/Comment	Timestamp[a]
00-00	Reserved			
00-01	PAUSE	Annex 31B	Requests that the recipient stops transmitting non-control frames for a period of time indicated by the parameters of this function.	No
00-02	GATE	Clause 64, Clause 77, Clause 103	Request that the recipient allows transmission of frames at a time, and for a period of time indicated by the parameters of this function.	Yes
00-03	REPORT	Clause 64, Clause 77, Clause 103	Notify the recipient of pending transmission requests as indicated by the parameters of this function.	Yes
00-04	REGISTER_REQ	Clause 64, Clause 77, Clause 103	Request that the station be recognized by the protocol as participating in a gated transmission procedure as indicated by the parameters of this function.	Yes
00-05	REGISTER	Clause 64, Clause 77, Clause 103	Notify the recipient that the station is recognized by the protocol as participating in a gated transmission procedure as indicated by the parameters of this function.	Yes
00-06	REGISTER_ACK	Clause 64, Clause 77, Clause 103	Notify the recipient that the station acknowledges participation in a gated transmission procedure.	Yes
00-07 through 00-11	Reserved			
00-12	GATE	144.3.6.1	Request that the recipient allows transmission of frames at a time, and for a period of time indicated by the parameters of this function.	Yes
00-13	REPORT	144.3.6.2	Notify the recipient of pending transmission requests as indicated by the parameters of this function.	Yes
00-14	REGISTER_REQ	144.3.6.3	Request that the station be recognized by the protocol as participating in a gated transmission procedure as indicated by the parameters of this function.	Yes

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Table 31A–1—MAC Control opcodes *(continued)*

Opcode (Hexadecimal)	MAC Control function	Specified in	Value/Comment	Timestamp[a]
00-15	REGISTER	144.3.6.4	Notify the recipient that the station is recognized by the protocol as participating in a gated transmission procedure as indicated by the parameters of this function.	Yes
00-16	REGISTER_ACK	144.3.6.5	Notify the recipient that the station acknowledges participation in a gated transmission procedure.	Yes
00-17	DISCOVERY	144.3.6.6	Request that recipients attempt registration during the discovery window.	Yes
00-18	SYNC_PATTERN	144.3.6.7	Announces burst synchronization patterns to all unregistered ONUs, multiple/all registered ONUs, or individual registered ONUs.	Yes
00-19 through 00-1F	Reserved			
00-20	CC_REQUEST	144.4.3.1	Query or change the state of ONU channel(s).	No
00-21	CC_RESPONSE	144.4.3.2	Report current channel(s) state and action result code.	No
00-22 through 01-00	Reserved			
01-01	PFC	Annex 31D and IEEE Std 802.1Q	Requests that the recipient stops transmissions in the priorities indicated in the parameters of the function for a period of time also indicated in the parameters.	No
01-02 through FF-FD	Reserved			
FF–FE	EXTENSION	Annex 31C	This frame is used for Organization–Specific Extension. Upon reception of this message, the MAC Control generates MA_CONTROL.Indication informing the MAC Control Client to perform the relevant action.	No
FF-FF	Reserved			

[a]The value of the Timestamp field is generated by MAC Control and is not exposed through the client interface.

Opcodes are transmitted high-order octet first. Within each octet, bits are transmitted least-significant bit first. Reserved opcodes shall not be used by MAC Control sublayer entities.

Table 31A–2 through Table 31A–9 show the elements and semantics of the indication_operand_list for MA_CONTROL.indication primitives for each currently defined opcode value in Table 31A–1:

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Table 31A–2—PAUSE MAC Control indications

PAUSE (opcode 0x0001)		
indication_operand_list element	**Value**	**Interpretation**
pause_status	paused	Indicates that the PAUSE function is inhibiting transmission of data frames by the MAC client.
	not_paused	Indicates that the PAUSE function is not inhibiting transmission of data frames by the MAC client.

Table 31A–3—GATE MAC Control indications

GATE (opcode 0x0002)		
indication_operand_list element	**Value**	**Interpretation**
start	32 bit	Time when transmission should be initiated.
length	16 bit	Interval of time during which transmission is allowed.
status	arrive	Indicates that a grant has been received for future activation.
	active	Indicates that the GATE function is allowing transmission of frames.
	deactive	Indicates that the GATE function is inhibiting transmission of frames.
force_report	true	The OLT expects the ONU to transmit a REPORT message during the transmission opportunity identified by start and length fields.
	false	The OLT does not request the ONU to transmit a REPORT message during the transmission opportunity identified by start and length fields.
discovery	true	This grant is reserved for use during discovery.
	false	This grant is not reserved for use by the discovery process, and is available for use by all traffic.
discoveryInformation[a]	16 bits	See Table 77–3 for the internal structure of the discoveryInformation field.

[a]Only present in 10G–EPON GATE MAC Control indication (Clause 77).

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Table 31A–4—REPORT MAC Control indications

REPORT (opcode 0x0003)		
indication_operand_list element	**Value**	**Interpretation**
RTT	32 bit	Indicates the calculated round trip time for the station, as calculated following the REPORT message reception.
n	Integer	Indicates the number of queue status reports present
report_list	valid[8]	Indicates whether the corresponding status element is present when set to true.
	status[8]	Indicates amount of data waiting in the corresponding queue including the associated transmission overhead.

Table 31A–5—REGISTER_REQ MAC Control indications

REGISTER_REQ (opcode 0x0004)		
indication_operand_list element	**Value**	**Interpretation**
status	incoming	Indicates that a station is requesting recognition.
	retry	Indicates that the station should reattempt registration.
flags	register	Indicates that the station is requesting to register.
	deregister	Indicates that the station is requesting to deregister.
pending_grants	Integer	Indicates the maximum number of future GATES that can be stored by the GATE function.
RTT	32 bit	Indicates the calculated round trip time for the station, as calculated following the REGISTER_REQ message reception.
laserOnTime[a]	8 bits	Indicates the Laser On Time characteristic for the given ONU transmitter, expressed in the units of time_quanta.
laserOffTime[a]	8 bits	Indicates the Laser Off Time characteristic for the given ONU transmitter, expressed in the units of time_quanta.
discoveryInformation[a]	16 bits	See Table 77–7 for the internal structure of the discoveryInformation field.

[a]Only present in 10G–EPON REGISTER_REQ MAC Control indication (Clause 77).

Table 31A–6—REGISTER MAC Control indications

REGISTER (opcode 0x0005)		
indication_operand_list element	**Value**	**Interpretation**
SA	48 bit	MAC address of OLT to which registration is being performed.
ID	16 bit	LLID assigned by the OLT for use by the ONU.

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Table 31A–6—REGISTER MAC Control indications *(continued)*

REGISTER (opcode 0x0005)		
indication_operand_list element	**Value**	**Interpretation**
status	accepted	Indicates that the requested registration is successful.
	denied	Indicates that the requested registration attempt is denied by the higher-layer-entity.
	deregistered	Indicates that the ONU has been deregistered, i.e., the associated LLID has been deallocated.
	reregistered	Indicates that the ONU is explicitly asked to re-register.
laserOnTime[a]	8 bits	Indicates the Laser On Time characteristic for the given ONU transmitter, expressed in the units of time_quanta.
laserOffTime[a]	8 bits	Indicates the Laser Off Time characteristic for the given ONU transmitter, expressed in the units of time_quanta.

[a]Only present in 10G–EPON REGISTER MAC Control indication (Clause 77).

Table 31A–7—REGISTER_ACK MAC Control indications

REGISTER_ACK (opcode 0x0006)		
indication_operand_list element	**Value**	**Interpretation**
SA	48 bit	MAC address of ONU to which registration is being performed.
ID	16 bit	Indicates the LLID allocated to the ONU.
status	accepted	Indicates the station has been recognized as participating in gated transmission.
	denied	Indicates the station has been excluded from participating in gated transmission.
	reset	Indicates the station has been requested to resubmit a registration request.
	deregistered	Indicates that the station will no longer be participating in gated transmission.
RTT	32 bit	Indicates the calculated round trip time for the station, as calculated following the REGISTER_ACK message reception.

Table 31A–8—EXTENSION MAC Control indications

EXTENSION (opcode 0xFFFE)		
indication_operand_list element	**Value**	**Interpretation**
OUI	24 bits	Organizationally-Unique Identifier (OUI) or Company ID (CID) that determines the format and semantics of the Value field and its subfields, if any are defined.
Value	Variable	Organization-specific value, distinguished by the OUI or CID.

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Table 31A–9—PFC MAC Control indications

PFC (opcode 0x0101)		
indication_operand_list element	**Value**	**Interpretation**
priority_enable_vector	2 octets	The most significant octet is reserved (i.e., set to zero on transmission and ignored on receipt). Each bit of the least significant octet indicates if the corresponding field in the time_vector parameter is valid. The bits of the least significant octet are named e[0] (the least significant bit) to e[7] (the most significant bit). Bit e[n] refers to Priority n. For each e[n] bit set to one, the corresponding time[n] value is valid. For each e[n] bit set to zero, the corresponding time[n] value is invalid.
time_vector	a list of eight 2-octet unsigned integers	A list of eight 2-octet fields named time[0] to time[7]. The eight time[n] values are always present regardless of the value of the corresponding e[n] bit. Each time[n] field is a 2-octet, unsigned integer containing the length of time for which the receiving station is requested to inhibit transmission of data frames associated with Priority n. The field is transmitted most significant octet first, and least significant octet second. The time[n] fields are transmitted sequentially, with time[0] transmitted first and time[7] transmitted last. Each time[n] value is measured in units of pause_quanta, equal to the time required to transmit 512 bits of a frame at the data rate of the MAC. Each time[n] field can assume a value in the range of 0 to 65 535 pause_quanta.

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Annex 31B

(normative)

MAC Control PAUSE operation

31B.1 PAUSE description

The PAUSE operation is used to inhibit transmission of data frames for a specified period of time. A MAC Control client wishing to inhibit transmission of data frames from another station on the network generates a MA_CONTROL.request primitive specifying the following:

a) The globally assigned 48-bit multicast address 01-80-C2-00-00-01
b) The PAUSE opcode
c) A request_operand indicating the length of time for which it wishes to inhibit data frame transmission (see 31B.2)

The PAUSE operation cannot be used to inhibit transmission of MAC Control frames.

PAUSE frames shall only be sent by DTEs configured to the full duplex mode of operation.

The globally assigned 48-bit multicast address 01-80-C2-00-00-01 has been reserved for use in MAC Control PAUSE frames for inhibiting transmission of data frames from a DTE in a full duplex mode IEEE 802.3 LAN. IEEE 802.1Q-conformant bridges will not forward frames sent to this multicast destination address, regardless of the state of the bridge's ports, or whether or not the bridge implements the MAC Control sublayer. To allow generic full duplex flow control, stations implementing the PAUSE operation shall instruct the MAC (e.g., through layer management) to enable reception of frames with destination address equal to this multicast address.

NOTE—By definition, an IEEE 802.3 LAN operating in full duplex mode comprises exactly two stations, thus there is no ambiguity regarding the destination DTE's identity. The use of a well-known multicast address relieves the MAC Control sublayer and its client from having to know, and maintain knowledge of, the individual 48-bit address of the other DTE in a full duplex environment.

When MAC Control PFC operation (see Annex 31D and IEEE Std 802.1Q) has been enabled, MAC Control PAUSE operation shall be disabled.

31B.2 Parameter semantics

The PAUSE opcode takes the following request_operand:

pause_time
: A 2-octet, unsigned integer containing the length of time for which the receiving station is requested to inhibit data frame transmission. The field is transmitted most-significant octet first, and least-significant octet second. The pause_time is measured in units of pause_quanta, equal to 512 bit times of the particular implementation (see 4.4). The range of possible pause_time is 0 to 65535 pause_quanta.

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31B.3 Detailed specification of PAUSE operation

The state machines in 31B.3 follow the conventions in 21.5. (See 25.1.1 for an example statement. That also covers the timer conventions from 14 which apply here.)

31B.3.1 Transmit operation

Upon receipt of a MA_CONTROL.request primitive containing the PAUSE opcode from a MAC client, the MAC Control sublayer calls the MAC sublayer MAC:MA_DATA.request service primitive with the following parameters:

a) The destination_address is set equal to the destination_address parameter of the MA_CONTROL.request primitive. This parameter is currently restricted to the value specified in 31B.1.
b) The source_address is set equal to the 48-bit individual address of the station.
c) The length/type field (i.e., the first two octets) within the mac_service_data_unit parameter is set to the IEEE 802.3 MAC Control EtherType value assigned in 31.4.1.3.
d) The remainder of the mac_service_data_unit is set equal to the concatenation of the PAUSE opcode encoding (see Annex 31A), the pause_time request_operand specified in the MA_CONTROL.request primitive, and a field containing zeros of the length specified in 31.4.1.6.
e) The frame_check_sequence is omitted.

Upon receipt of a data transmission request from the MAC client through the MCF:MA_DATA.request primitive, if the transmission of data frames has not been inhibited due to reception of a valid MAC Control frame specifying the PAUSE operation and a non-zero pause_time, the MAC Control sublayer calls the MAC sublayer MAC:MA_DATA.request service primitive with its parameters identical to the MCF:MA_DATA.indication primitive.

31B.3.2 Transmit state diagram for PAUSE operation

It is not required that an implementation be able to transmit PAUSE frames. MAC Control sublayer entities that transmit PAUSE frames shall implement the Transmit state diagram specified in this subclause.

31B.3.2.1 Constants

pause_command
: The 2-octet encoding of the PAUSE command, as specified in Annex 31A.

reserved_multicast_address
: The 48-bit address specified in 31B.1 item a).

802.3_MAC_Control
: The 16 bit EtherType field assignment for IEEE 802.3 MAC Control specified in 31.4.1.3.

phys_Address
: A 48-bit value, equal to the unicast address of the station implementing the MAC Control sublayer.

31B.3.2.2 Variables

transmitEnabled
: A Boolean set by network management to indicate that the station is permitted to transmit on the network.
: Values: true; Transmitter is enabled by management
false; Transmitter is disabled by management

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transmission_in_progress
: A Boolean used to indicate to the Receive state diagram that a MAC:MA_DATA.request service primitive call is pending.

  Values: true; transmission is in progress
  false; transmission is not in progress

n_quanta_tx
: An integer indicating the number of pause_quanta that the transmitter of a PAUSE frame is requesting that the receiver pause.

pause_timer_Done
: A Boolean set by the MAC Control PAUSE Operation Receive state diagram to indicate the expiration of a pause_timer initiated by reception of a MAC Control frame with a PAUSE opcode.

  Values: true; The pause_timer has expired.
  false; The pause_timer has not expired.

pause_mac_service_data_unit
: The concatenation of IEEE 802.3_MAC_Control, pause_command, n_quanta_tx, zeros.

31B.3.2.3 Functions

None

31B.3.2.4 Timers

pause_timer
: The timer governing the inhibition of transmission of data frames (see 31.5.1) from a MAC Client by the PAUSE function.

31B.3.2.5 Messages

MA_CONTROL.request
: The service primitive used by a client to request a MAC Control sublayer function with the specified request_operands.

MCF:MA_DATA.request
: The service primitive used by a client to request MAC data transmission with the specified parameters.

MAC:MA_DATA.request
: The service primitive issued by the MAC Control sublayer to transmit a MAC frame with the specified parameters. The action invoked is not considered to end until the transmission of the frame by the MAC has concluded and the ability of the MAC control layer to determine this is implementation dependent.

31B.3.2.6 Transmit state diagram for PAUSE operation

Figure 31B–1 depicts the Transmit state diagram for a MAC Control sublayer entity implementing the PAUSE operation.

31B.3.3 Receive operation

The opcode-independent MAC Control sublayer Receive state diagram accepts and parses valid frames received from the MAC sublayer. MAC Control sublayer entities that implement the PAUSE operation shall implement the Receive state diagram specified in this subclause. The functions specified in this subclause are performed upon receipt of a valid Control frame containing the PAUSE opcode, and define the function called by the INITIATE MAC CONTROL FUNCTION state of Figure 31–4. (See 31.5.3.)

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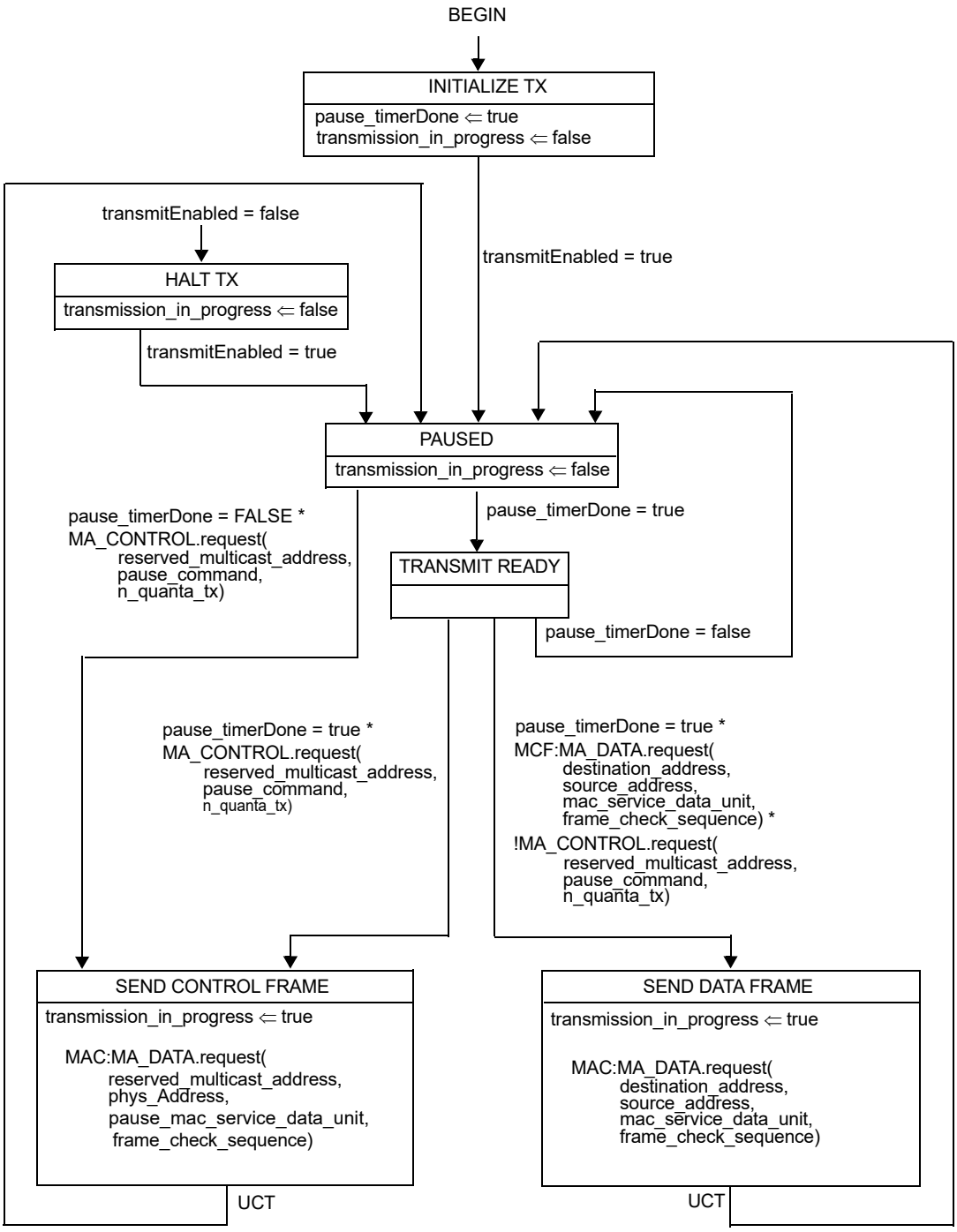

Figure 31B–1—PAUSE Operation Transmit state diagram

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Upon receipt of a valid MAC Control frame with the opcode indicating PAUSE and the destination address indicating either: (1) the globally assigned multicast address specified in 31B.1, or (2) the unique physical address associated with this station, the MAC Control sublayer starts a timer for the length of time specified by the pause_time request_operand in the Control frame (see 31B.2). The value of the variable pause_timer_Done is set to false upon the setting of the pause_timer to a non-zero value by the MAC Control PAUSE Operation Receive state diagram. The value of the variable pause_timer_Done is set to true when the timer value reaches zero (i.e., the timer expires). If the received PAUSE operation indicates a pause_timer value of zero, the value of pause_timer_Done is set to true immediately.

The receipt of a valid MAC Control frame with the opcode indicating PAUSE and the destination address indicating the globally assigned multicast address specified in 31B.1 or the unique physical address associated with this station will cause the pause_timer to be set according to the pause_time request_operand in the newly received frame, regardless of the current setting of the pause_timer, i.e., new PAUSE operations override earlier PAUSE operations.

31B.3.4 Receive state diagram for PAUSE operation

31B.3.4.1 Constants

pause_quantum
: The unit of measurement for pause time specified in 31B.2

pause_command
: The 2-octet encoding of the PAUSE command, as specified in Annex 31A.

reserved_multicast_address
: The 48-bit address specified in 31B.1 item a).

phys_Address
: A 48-bit value, equal to the unicast address of the station implementing the MAC Control sublayer.

31B.3.4.2 Variables

n_quanta_rx
: An integer used to extract the number of pause_quanta to set the pause_timer from the dataParam of the received MAC frame.

opcode
: The opcode parsed from the received MAC frame.

DA
: The destination address from the MAC:MA_DATA.indication service primitive.

data
: The data payload parsed from the received MAC frame.

transmission_in_progress
: A Boolean used by the Transmit state diagram to indicate that a MAC:MA_DATA.request service primitive call is pending.

  Values: true; transmission is in progress
  false; transmission is not in progress

31B.3.4.3 Timers

pause_timer
: The timer governing the inhibition of transmission of data frames.

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31B.3.4.4 Receive state diagram (INITIATE MAC CONTROL FUNCTION) for PAUSE operation

Figure 31B–2 depicts the INITIATE MAC CONTROL FUNCTION for the PAUSE operation. (See 31.5.3.)

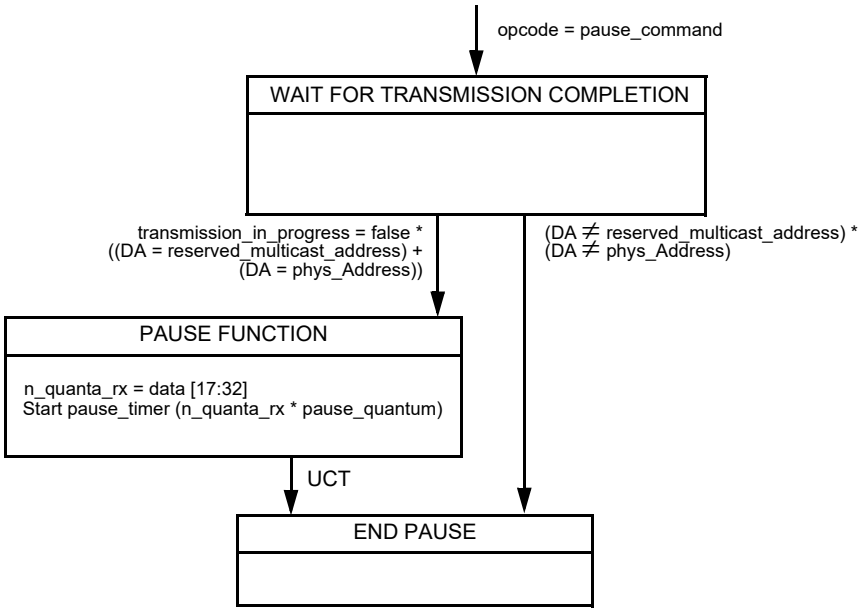

Figure 31B–2—PAUSE Operation Receive state diagram

31B.3.5 Status indication operation

MAC Control sublayer entities that implement the PAUSE operation shall implement the Indication state diagram specified in this subclause.

The PAUSE function sets the pause_status variable to one of two values: paused or not_paused, and indicates this to its client through the MA_CONTROL.indication primitive.

31B.3.6 Indication state diagram for pause operation

31B.3.6.1 Constants

pause_command
: The 2-octet encoding of the PAUSE command, as specified in Annex 31A.

31B.3.6.2 Variables

pause_status
: Used to indicate the state of the MAC Control sublayer for the PAUSE operation. It takes one of two values: paused or not_paused.

pause_timer_Done
: A Boolean set by the MAC Control PAUSE Operation Receive state diagram to indicate the expiration of a pause_timer initiated by reception of a MAC Control frame with a PAUSE opcode.

Values: true; The pause_timer has expired.
false; The pause_timer has not expired.

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31B.3.6.3 Messages

MA_CONTROL.indication

The service primitive used to indicate the state of the MAC Control sublayer to its client.

31B.3.6.4 Indication state diagram for PAUSE operation

Figure 31B–3 depicts the Indication State Diagram for a MAC Control sublayer implementing the PAUSE operation.

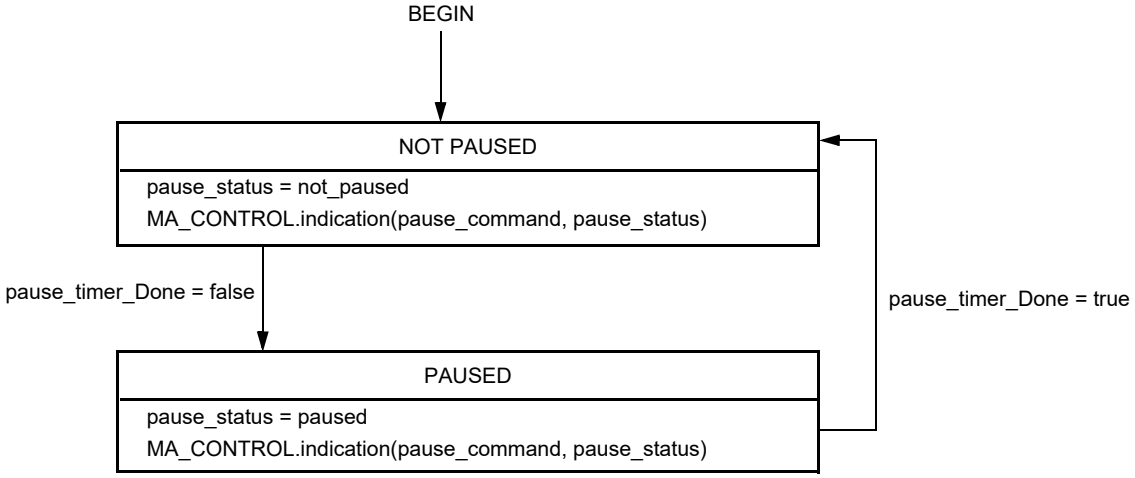

Figure 31B–3—PAUSE Operation Indication state diagram

31B.3.7 Timing considerations for PAUSE operation

In a full duplex mode DTE, it is possible to receive PAUSE frames asynchronously with respect to the transmission of MAC frames. For effective flow control, it is necessary to place an upper bound on the length of time that a DTE can transmit data frames after receiving a valid PAUSE frame with a non-zero pause_time request_operand.

Reception of a PAUSE frame shall not affect the transmission of a MAC frame that has been submitted by the MAC Control sublayer to the underlying MAC (i.e., the MAC:MA_DATA.request service primitive is synchronous, and is never interrupted).

At operating speeds of 100 Mb/s or less, a station that implements an exposed MII, shall not begin to transmit a (new) frame (assertion of TX_EN at the MII, see 22.2.2.3) more than one pause_quantum after the reception of a valid PAUSE frame (deassertion of RX_DV at the MII, see 22.2.2.7) that contains a nonzero value of pause_time. Stations that do not implement an exposed MII, shall measure this time at the MDI, with the timing specification increased to one pause_quantum + 64 BT.

At an operating speed of 1000 Mb/s, a station shall not begin to transmit a (new) frame more than two pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

At operating speeds of 2.5 Gb/s, a station with a 2.5GBASE-T PHY shall not begin to transmit a (new) frame more than 34 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI. A station using any other 2.5 Gb/s PHY shall not begin to transmit a (new) frame more than 6 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

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At operating speeds of 5 Gb/s, a station with a 5GBASE-T PHY shall not begin to transmit a (new) frame more than 42 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI. A station using any other 5 Gb/s PHY shall not begin to transmit a (new) frame more than 12 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

At operating speeds of 10 Gb/s, a station with a 10GBASE-T PHY shall not begin to transmit a (new) frame more than 74 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI. A station using any other 10 Gb/s PHY shall not begin to transmit a (new) frame more than 60 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

At operating speeds of 25 Gb/s, a station shall not begin to transmit a (new) frame more than 80 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

At operating speeds of 40 Gb/s, a station shall not begin to transmit a (new) frame more than 118 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

At operating speeds of 50 Gb/s, a station shall not begin to transmit a (new) frame more than 117 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

At operating speeds of 100 Gb/s, a station shall not begin to transmit a (new) frame more than 394 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

At operating speeds of 200 Gb/s, a station shall not begin to transmit a (new) frame more than 453 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

At operating speeds of 400 Gb/s, a station shall not begin to transmit a (new) frame more than 905 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

In addition to DTE and MAC Control delays, system designers should take into account the delay of the link segment when designing devices that implement the PAUSE operation.

The PAUSE response time may be verified by demonstrating that no more than max_overrun bytes of frame data are sent by the station after reception of a valid PAUSE frame that contains a non-zero value of pause_time. The value of max_overun is defined for the following operating speeds, where frame_length is the maximum frame length transmitted by the station during the test:

2.5 Gb/s (using 2.5GBASE-T) – max_overrun = 2176 + frame_length.

2.5 Gb/s (not using 2.5GBASE-T) – max_overrun = 384 + frame_length

5 Gb/s (using 5GBASE-T) – max_overrun = 2624 + frame_length.

5 Gb/s (not using 5GBASE-T) – max_overrun = 768 + frame_length

10 Gb/s (using 10GBASE-T) – max_overrun = 4736 + frame_length.

10 Gb/s (not using 10GBASE-T) – max_overrun = 3840 + frame_length.

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25 Gb/s – max_overrun = 5120 + frame_length.

40 Gb/s – max_overrun = 7552 + frame_length.

50 Gb/s – max_overrun = 7488 + frame_length.

100 Gb/s – max_overrun = 25216 + frame_length.

200 Gb/s – max_overrun = 28992 + frame_length.

400 Gb/s – max_overrun = 57920 + frame_length.

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31B.4 Protocol implementation conformance statement (PICS) proforma for MAC Control PAUSE operation[272]

31B.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 31B, MAC Control PAUSE operation, shall complete the following PICS proforma in addition to the PICS of Clause 31.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

31B.4.2 Identification

31B.4.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations, other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

31B.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 31B, MAC Control PAUSE operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2022)	

Date of Statement	

[272]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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31B.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PST	Support for transmit of PAUSE frames	31B.3.2	N/A	O	Yes [ ] No [ ]
*MIIa	At operating speeds of 100 Mb/s or less, MII connection exists and is accessible for test.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIb	At operating speeds of 100 Mb/s or less, MII connection does not exist or is not accessible for test.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIc	At operating speeds of 1000 Mb/s	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIId	At operating speeds of 2.5 Gb/s with PHY types other than 2.5GBASE-T.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIe	At operating speeds of 2.5 Gb/s with PHY types of 2.5GBASE-T.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIf	At operating speeds of 5 Gb/s with PHY types other than 5GBASE-T.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIg	At operating speeds of 5 Gb/s with PHY types of 5GBASE-T.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIh	At operating speeds of 10 Gb/s with PHY types other than 10GBASE-T.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIi	At operating speeds of 10 Gb/s with PHY types of 10GBASE-T.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIj	At operating speeds of 25 Gb/s.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIk	At operating speeds of 40 Gb/s.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIl	At operating speeds of 50 Gb/s.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIm	At operating speeds of 100 Gb/s.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIn	At operating speeds of 200 Gb/s.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIo	At operating speeds of 400 Gb/s.	31B.3.7	N/A	O	Yes [ ] No [ ]

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31B.4.4 PAUSE command requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PCR1	Duplex mode of DTE	31B.1	Full duplex	M	Yes [ ]
PCR2	Reception of frames with destination address equal to the multicast address 01-80-C2-00-00-01	31B.1	Enabled	M	Yes [ ]
PCR3	PAUSE operation on PFC enable	31B.1	Disabled	PFC: M	Yes [ ]

31B.4.5 PAUSE command state diagram requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PSD1	Transmit state diagram for PAUSE operation	31B.3.2	Meets requirements of Figure 31B–1	PST: M	N/A [ ] M:Yes [ ]
PSD2	Receive state diagram for PAUSE operation	31B.3.4	Meets requirements of Figure 31B–2	M	Yes [ ]
PSD3	Indication state diagram for PAUSE operation	31B.3.6	Meets requirements of Figure 31B–3	M	Yes [ ]

31B.4.6 PAUSE command MAC timing considerations

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	Effect of PAUSE frame on a frame already submitted to underlying MAC	31B.3.7	Has no effect	M	Yes [ ]
TIM2	Measurement point for station with MII	31B.3.7	Delay at MII ≤ one pause_quantum[a]	MIIa:M	Yes [ ] N/A [ ]
TIM3	Measurement point for station without MII at 100 Mb/s or less	31B.3.7	Delay at MDI ≤ one pause_quantum + 64 BT[a]	MIIb:M	Yes [ ] N/A [ ]
TIM4	Measurement point for station at 1000 Mb/s	31B.3.7	Delay at MDI ≤ two pause_quanta[a]	MIIc:M	Yes [ ] N/A [ ]
TIM5	Measurement point for station at 2.5 Gb/s with PHY type other than 2.5GBASE-T	31B.3.7	Delay at MDI ≤ 6 pause_quanta[a]	MIId:M	Yes [ ] N/A [ ]
TIM6	Measurement point for station at 2.5 Gb/s with PHY type of 2.5GBASE-T	31B.3.7	Delay at MDI ≤ 34 pause_quanta[a]	MIIe:M	Yes [ ] N/A [ ]
TIM7	Measurement point for station at 5 Gb/s with PHY type other than 5GBASE-T	31B.3.7	Delay at MDI ≤ 12 pause_quanta[a]	MIIf:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TIM8	Measurement point for station at 5 Gb/s with PHY type of 5GBASE-T	31B.3.7	Delay at MDI ≤ 42 pause_quanta[a]	MIIg:M	Yes [ ] N/A [ ]
TIM9	Measurement point for station at 10 Gb/s with PHY types other than 10GBASE-T	31B.3.7	Delay at MDI ≤ 60 pause_quanta[a]	MIIh:M	Yes [ ] N/A [ ]
TIM10	Measurement point for station at 10Gb/s with PHY type of 10GBASE-T	31B.3.7	Delay at MDI ≤ 74 pause_quanta[a]	MIIi:M	Yes [ ] N/A [ ]
TIM11	Measurement point for station at 25 Gb/s	31B.3.7	Delay at MDI ≤ 60 pause_quanta[a]	MIIj:M	Yes [ ] N/A [ ]
TIM12	Measurement point for station at 40 Gb/s	31B.3.7	Delay at MDI ≤ 118 pause_quanta[a]	MIIk:M	Yes [ ] N/A [ ]
TIM13	Measurement point for station at 50 Gb/s	31B.3.7	Delay at MDI ≤ 118 pause_quanta[a]	MIIl:M	Yes [ ] N/A [ ]
TIM14	Measurement point for station at 100 Gb/s	31B.3.7	Delay at MDI ≤ 117 pause_quanta[a]	MIIm:M	Yes [ ] N/A [ ]
TIM15	Measurement point for station at 200 Gb/s	31B.3.7	Delay at MDI ≤ 453 pause_quanta[a]	MIIn: M	Yes [ ] N/A [ ]
TIM16	Measurement point for station at 400 Gb/s	31B.3.7	Delay at MDI ≤ 905 pause_quanta[a]	MIIo: M	Yes [ ] N/A [ ]

[a]Delay from receiving valid PAUSE command, with nonzero value for pause_time, to cessation of transmission.

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Annex 31C

(normative)

MAC Control organization specific extension operation

31C.1 Organization specific extension description

The extension operation is used to provide a standardized means for other organizations, to define their own MAC Control protocols outside the scope of this standard. The requirements defined in Clause 31 apply to these protocols.

31C.2 Transmission of Extension MAC Control frame

Upon receipt of a MA_CONTROL.request primitive containing the EXTENSION opcode from a MAC client, the MAC control sublayer calls the MAC sublayer MAC:MA_DATA.request service primitive with the following parameters:

a) The destination_address is set equal to the destination_address parameter of the MA_CONTROL.request primitive. This parameter is currently restricted to either the value 01–80–C2–00–00–01 or to the 48 bit individual address of the destination station.
b) The source_address is set equal to the 48 bit individual address of the station.
c) The length/type field (i.e., the first two octets) within the mac_service_data_unit parameter is set to the IEEE 802.3 MAC Control EtherType value assigned in 31.4.1.3.
d) The remainder of the mac_service_data_unit is set to the concatenation of the Extension Opcode, Organizationally Unique Identifier (OUI) or Company ID (CID)[273] assigned to the organization by the IEEE, and the organization-specific data.
e) The frame_check_sequence is omitted.

MAC Control sublayer entities that transmit or receive EXTENSION frames shall pass them through without additional processing.

31C.3 Receive operation

The opcode–independent MAC Control sublayer Receive state diagram accepts and parses valid frames received from the MAC sublayer. MAC Control sublayer entities that implement the EXTENSION operation shall implement the Receive state diagram specified in this subclause. The functions specified in this subclause are performed upon receipt of a valid Control frame containing the EXTENSION opcode and define the function called by the INITIATE MAC CONTROL FUNCTION state of Figure 31–4 (see 31.5.3).

[273]Details defining the format of OUIs and CIDs can be found in IEEE Std 802 Overview and Architecture. Interested applicants should contact the IEEE Standards Department, Institute of Electrical and Electronics Engineers, https://standards.ieee.org/develop/regauth/, 445 Hoes Lane, Piscataway, NJ 08854, USA.

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31C.3.1 Receive state diagram (INITIATE MAC CONTROL FUNCTION) for EXTENSION operation

Figure 31C–2 depicts the INITIATE MAC CONTROL FUNCTION for the EXTENSION operation (see 31.5.3). Upon reception of EXTENSION frames, the frame is sent to the MAC CONTROL client.

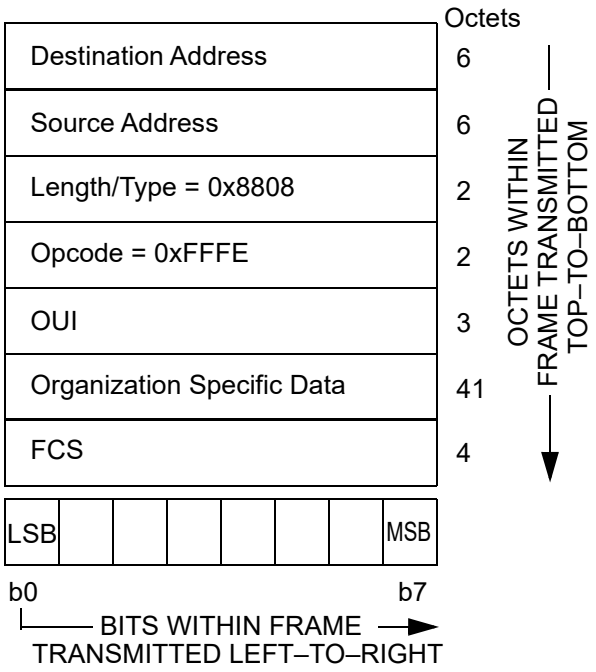

Figure 31C–1—MAC Control EXTENSION Frame

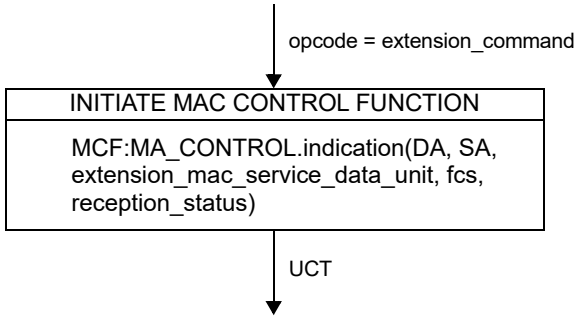

Figure 31C–2—EXTENSION receive function

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31C.4 Protocol implementation conformance statement (PICS) proforma for MAC Control organization specific extension operation[274]

31C.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 31A, MAC Control organization specific extension operation, shall complete the following PICS proforma in addition to the PICS of Clause 31.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

31C.4.2 Identification

31C.4.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations, other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

31C.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 31C, MAC Control organization specific extension operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2022)	

Date of Statement	

31C.4.3 EXTENSION command state diagram requirements

Item	Feature	Subclause	Value/Comment	Status	Support
ESD1	Receive state diagram for EXTENSION operation	31C.3	Meets requirements of Figure 31C–2	M	Yes [ ]

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Annex 31D

(normative)

MAC Control PFC operation

31D.1 PFC description

The Priority-based Flow Control (PFC) operation is used to inhibit transmission of data frames on one or more priorities for a specified period of time. The behavior of a MAC Control client supporting PFC operation is specified in IEEE Std 802.1Q. A MAC Control client wishing to inhibit transmission of data frames from the link partner generates a MA_CONTROL.request primitive specifying:

a) The globally assigned 48-bit multicast address 01-80-C2-00-00-01.
b) The PFC opcode.
c) A request_operand list with two operands: priority_enable_vector and time_vector. (See 31D.2.)

Unlike the MAC Control PAUSE operation, the inhibition of frames for the PFC operation occurs in the MAC Control client. Upon receiving a PFC frame, the only action in MAC Control is to generate a MA_CONTROL.indication primitive with the indication_operand list specified in Table 31A–9.

The PFC operation does not inhibit transmission of MAC Control frames.

PFC operation shall not be enabled on DTEs configured to the half-duplex mode of operation. PFC is intended for use over full-duplex point-to-point links. Use on shared media such as EPON is out of the scope of this standard.

The globally assigned 48-bit multicast address 01-80-C2-00-00-01 has been assigned for use in MAC Control frames. Bridges conformant to IEEE Std 802.1Q will not forward frames sent to this multicast destination address, regardless of the state of the bridge's ports, and whether or not the bridge implements the MAC Control sublayer. To allow PFC full duplex flow control, stations implementing the PFC operation shall instruct the MAC (e.g., through layer management) to enable reception of frames with destination address equal to this multicast address.

NOTE—By definition, an IEEE 802.3 LAN operating in full duplex mode comprises exactly two stations, thus there is no ambiguity regarding the destination DTE's identity. The use of a well-known multicast address relieves the MAC Control sublayer and its client from having to know, and maintain knowledge of, the individual 48-bit address of the other DTE in a full duplex environment.

31D.2 Parameter semantics

The PFC opcode takes the following request_operand_list:

priority_enable_vector:

A 2-octet vector. The most significant octet is reserved (i.e., set to zero on transmission and ignored on receipt). Each bit of the least significant octet indicates if the corresponding field in the time_vector parameter is valid. The bits of the least significant octet are named e[0] (the least significant bit) to e[7] (the most significant bit). Bit e[n] refers to Priority n. For each e[n] bit set to one, the corresponding time[n] value is valid. For each e[n] bit set to zero, the corresponding time[n] value is invalid.

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time_vector:

A list of eight 2-octet fields named time[0] to time[7]. The eight time[n] values are always present regardless of the value of the corresponding e[n] bit. Each time[n] field is a 2-octet, unsigned integer containing the length of time for which the receiving station is requested to inhibit transmission of data frames associated with Priority n. The field is transmitted most significant octet first, and least significant octet second. The time[n] fields are transmitted sequentially, with time[0] transmitted first and time[7] transmitted last. Each time[n] value is measured in units of pause_quanta, equal to the time required to transmit 512 bits of a frame at the data rate of the MAC. Each time[n] field can assume a value in the range of 0 to 65 535 pause_quanta.

31D.3 PFC transmit

The state machines in 31D.3 follow the conventions in 21.5. (See 25.1.1 for an example statement. That also covers the timer conventions from 14 which apply here.)

Upon receipt of a MA_CONTROL.request primitive containing the PFC opcode from a MAC client, the MAC Control sublayer calls the MAC sublayer MAC:MA_DATA.request service primitive with the following parameters:

a) The destination_address is set equal to the destination_address parameter of the MA_CONTROL.request primitive. This parameter is currently restricted to the value specified in 31D.1.
b) The source_address is set equal to the 48-bit individual address of the station.
c) The length/type field (i.e., the first two octets) within the mac_service_data_unit parameter is set to the IEEE 802.3 MAC Control EtherType value assigned in 31.4.1.3.
d) The remainder of the mac_service_data_unit is set equal to the concatenation of the PFC opcode encoding (see Annex 31A), the priority_enable_vector and the time_vector specified in the MA_CONTROL.request primitive, and a field containing zeros of the length specified in 31.4.1.6.
e) The frame_check_sequence is omitted.

Figure 31D–1 depicts the MAC Control PFC Frame transmitted in response to an MA_Control.request primitive with the PFC opcode.

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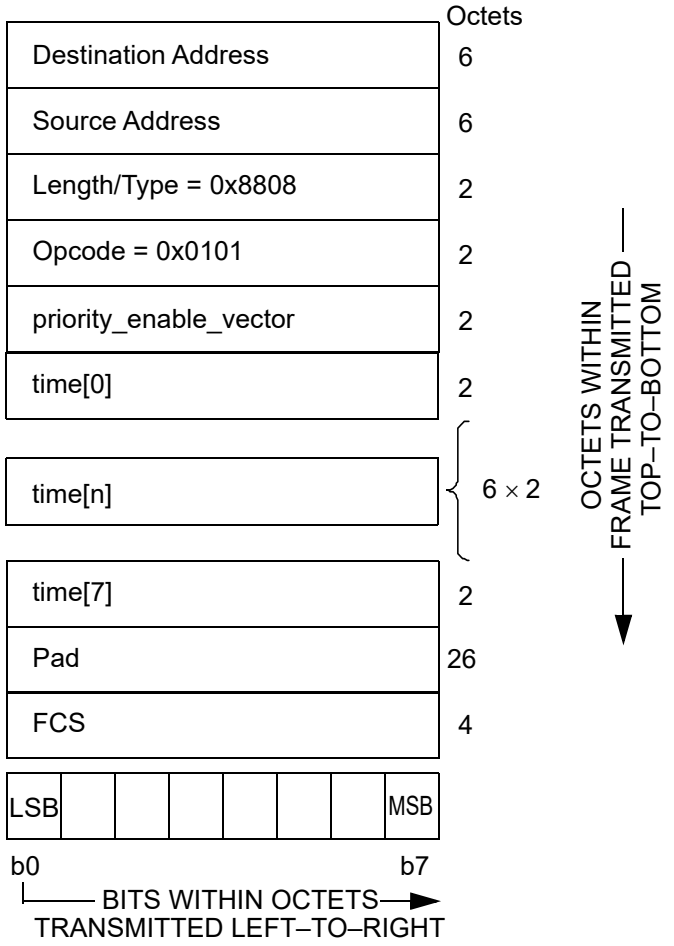

Figure 31D–1—MAC Control EXTENSION Frame

31D.4 Transmit state diagram for PFC operation

MAC Control sublayer entities that transmit PFC frames shall implement the Transmit state diagram specified in this subclause.

31D.4.1 Constants

pfc_command
: The 2-octet encoding of the PFC opcode, as specified in Annex 31A.

phys_Address
: A 48-bit value, equal to the unicast address of the station implementing the MAC Control sublayer.

reserved_multicast_address
: The 48-bit address specified in 31D.1 item a).

802.3_MAC_Control
: The 16 bit EtherType field assignment for IEEE 802.3 MAC Control specified in 31.4.1.3.

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31D.4.2 Variables

transmitEnabled
: A Boolean set by network management to indicate that the station is permitted to transmit on the network.

  Values: true; Transmitter is enabled by management
  false; Transmitter is disabled by management

pfc_operand_list
: The priority_enable_vector and time_vector from the MA_CONTROL.request.

pfc_mac_service_data_unit
: The concatenation of IEEE 802.3_MAC_Control, pfc_command, priority_enable_vector, time_vector, zeros.

31D.4.3 Messages

MA_CONTROL.request
: The service primitive used by a client to request a MAC Control sublayer function with the specified request_operands.

MCF:MA_DATA.request
: The service primitive used by a client to request MAC data transmission with the specified parameters.

MAC:MA_DATA.request
: The service primitive issued by the MAC Control sublayer to transmit a MAC frame with the specified parameters. The action invoked is not considered to end until the transmission of the frame by the MAC has concluded and the ability of the MAC control layer to determine this is implementation dependent.

31D.4.4 Transmit state diagram for PFC operation

Figure 31B–1 depicts the Transmit state diagram for a MAC Control sublayer entity implementing the PFC operation.

31D.5 PFC receive

The opcode-independent MAC Control sublayer Receive state diagram accepts and parses valid frames received from the MAC sublayer. The functions specified in this subclause are performed upon receipt of a valid Control frame containing the PFC opcode, and define the function called by the INITIATE MAC CONTROL FUNCTION state of Figure 31–4. (See 31.5.3.) Upon receipt of a valid MAC Control frame with the opcode indicating PFC and the destination address indicating the globally assigned multicast address specified in 31D.1, the MAC Control sublayer generates the MA_CONTROL.indication to the MAC Control Client.

31D.6 Receive state diagram for PFC operation

MAC Control sublayer entities that transmit PFC frames shall implement the Receive state diagram specified in this subclause.

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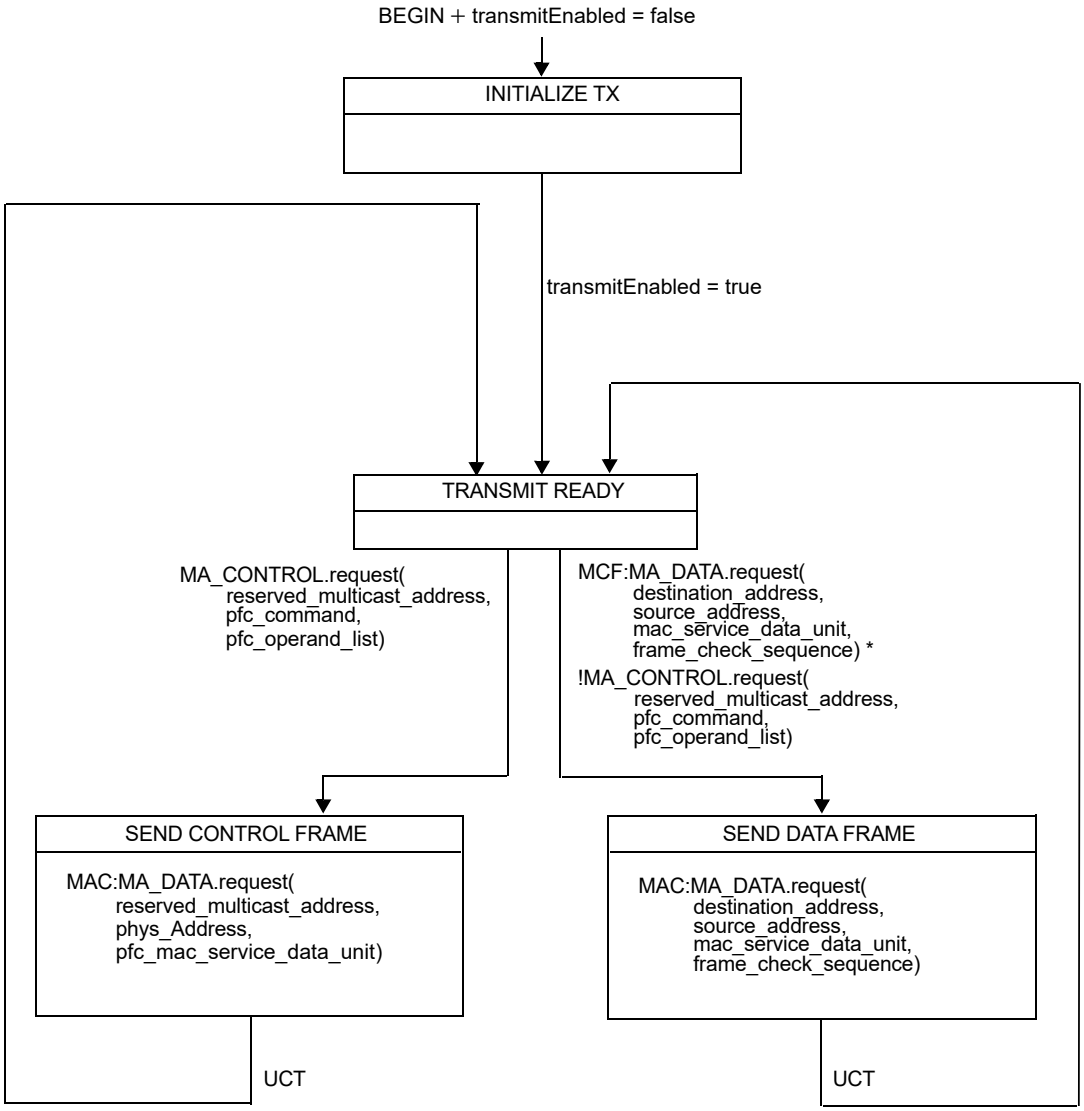

Figure 31D–2—PFC Operation Transmit state diagram

31D.6.1 Constants

pfc_command
: The 2-octet encoding of the PFC opcode, as specified in Annex 31A.

reserved_multicast_address
: The 48-bit address specified in 31D.1 item a).

31D.6.2 Variables

opcode
: The opcode parsed from the received MAC frame.

DA
: The destination address from the MAC:MA_DATA.indication service primitive.

pfc_operand_list
: The priority_enable_vector and time_vector parsed from the received frame.

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31D.6.3 Receive state diagram (INITIATE MAC CONTROL FUNCTION) for PFC operation

Figure 31B–2 depicts the INITIATE MAC CONTROL FUNCTION for the PFC operation. (See 31.5.3.)

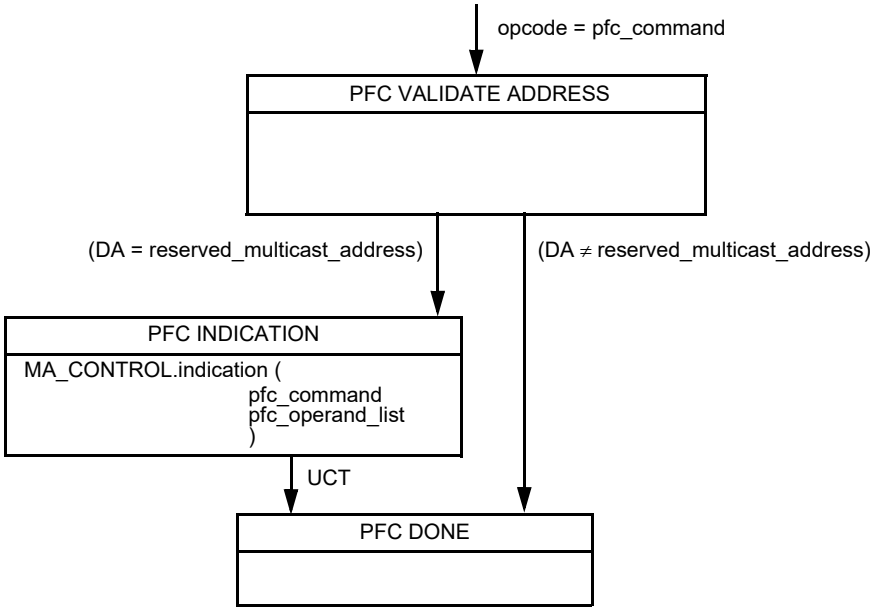

Figure 31D–3—PFC Operation Receive state diagram

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31D.7 Protocol implementation conformance statement (PICS) proforma for MAC Control PFC operation[275]

31D.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 31D, MAC Control PFC operation, shall complete the following PICS proforma in addition to the PICS of Clause 31.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

31D.7.2 Identification

31D.7.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations, other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

31D.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 31D, MAC Control PFC operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2022)	

Date of Statement	

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31D.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
PFC	Support for transmit and reception of PFC frames	31D.3 and 31D.5	N/A	M	Yes [ ]

31D.7.4 PFC command requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PFC1	Duplex mode of DTE	31D.1	Full duplex	M	Yes [ ]
PFC2	Reception of frames with destination address equal to the multicast address 01-80-C2-00-00-01	31D.1	Enabled	M	Yes [ ]

31D.7.5 PFC command state diagram requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PSDT	Transmit state diagram for PFC operation	31D.4	Meets requirements of Figure 31D–2	M	Yes [ ]
PSDR	Receive state diagram for PFC operation	31D.6	Meets requirements of Figure 31D–3	M	Yes [ ]

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Annex 32A

(informative)

Use of cabling systems with nominal differential characteristic impedance of 120 Ω or 150 Ω

The 100BASE-T2 standard specifies only the use of 100 Ω link segments for conformance. Since ISO/IEC 11801: 1995 also recognizes 120 Ω and 150 Ω cabling, this informative annex specifies the conditions for using cabling systems with nominal characteristic impedances of 120 Ω and 150 Ω by 100BASE-T2 conformant stations.

The use of cabling with a characteristic impedance outside the range specified in 32.7.2.2 will generally increase the mismatching effects in the link components if directly coupled to the PHY without a impedance transforming balun and results in the following consequences:

a) Increased echo due primarily to poorer hybrid performance
b) Increased cabling attenuation roughness due to increased reflections
c) Increased transmitter launch amplitude
d) Possible non-linearities in transmitter

The effect of increased echo and reflection is more than compensated by use of Category 4 or higher 120 Ω cabling or 150 Ω cabling consistent with ISO/IEC 11801 specifications. The increased transmitter launch level will not be an additional noise or EMC problem on these quality cabling. Manufacturers intending to support a direct connection of 120 Ω or 150 Ω cabling to the 100BASE-T2 PHY have to ensure that the transmitters can tolerate the impedance without additional non-linearity.

If baluns are used instead of a direct connection, care has to be taken to ensure that the corner frequencies of the baluns do not substantially interfere with the 100BASE-T2 signals. In practice, a lower corner frequency less than 100 kHz and an upper corner frequency greater than 30 MHz should be adequate for use with Category 4 or higher 120 Ω cabling or 150 Ω cabling consistent with ISO/IEC 11801 specifications.

CAUTION

Users of the present annex are further advised to check with the manufacturer of the particular 100BASE-T2 devices they intend to use with a 120 Ω or 150 Ω link whether those devices can operate correctly on cabling with Zc as high as 120 Ω ± 15 Ω and 150 Ω ± 15 Ω.

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Annex 33A

(informative)

PSE-PD stability

33A.1 Recommended PSE design guidelines and test setup

In order to prevent potential oscillations between the PSE and PD, the sum of the PSE port output impedance (Zo_port), the cable impedance (Zc), the PD input port circuitry impedance (Zpd_cir) and the PD EMI output filter impedance (Z_emi) should be lower than the PD power supply input impedance (Zin_ps_pd). This subclause focuses on the PSE part.

Port output impedance consists of two parts:

a) PSE power supply output impedance (Zo_ps), which is a function of the load (P_{Port}), and
b) Series elements (Z_ser) that connect the PSE power supply output to the port.

Therefore, the total Port output impedance during normal powering mode is Zo_port = Zo_ps + Z_ser.

In order to maintain PSE-PD stability, the following guidelines apply:

c) Zo_ps max = 0.3 Ω. at frequencies up to 100 kHz at $P_{port} = P_{Type}$ as defined in Table 33–11.
   Zo_ps can be extracted from Z_{port} by measuring V_{Port} / I_{Port} (with an external power dynamic analyzer system) as a function of frequency and subtracting from Z_{port} the value of Zser (f = DC) which is limited by the value of Zser at DC (low frequency).
d) If Zo_ps < Zo_ser and V_{Port} is kept to V_{Port} min and V_{Port} max as defined in Table 33–11 during dynamic load changes from 10 Hz to 100 kHz, then the value of Zo_ps is not limited.

Compliance to the above requirements should be made by measuring the port output impedance from 10 Hz to 100 kHz with a load of P_{Type} as defined in Table 33–11 at short cable length, or by presenting simulation results.

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See Figure 1 for the PSE-PD system impedance allocation.

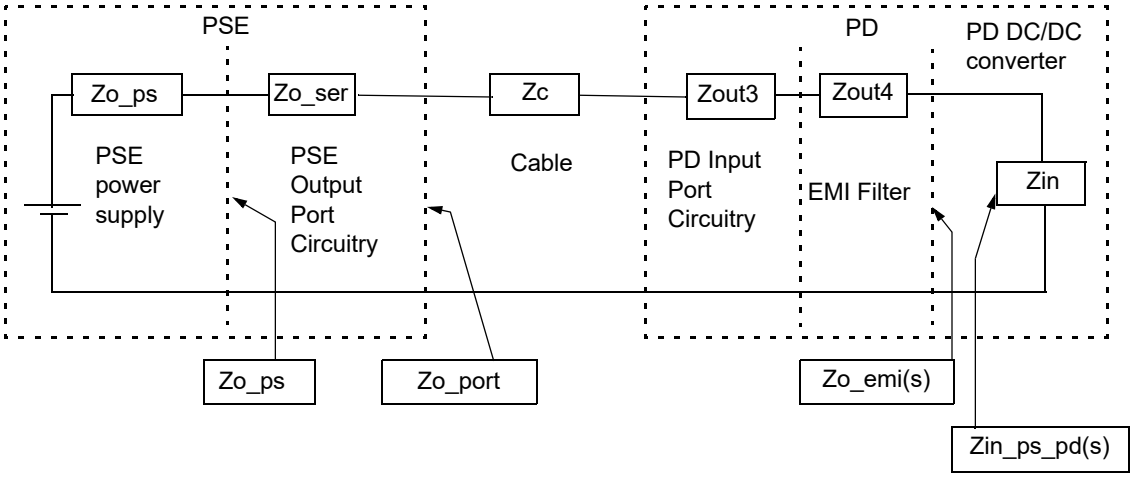

Figure 33A–1—PSE-PD system impedance allocation

See Figure 33A–2 for the test setup and Figure 33A–3 for the test requirements.

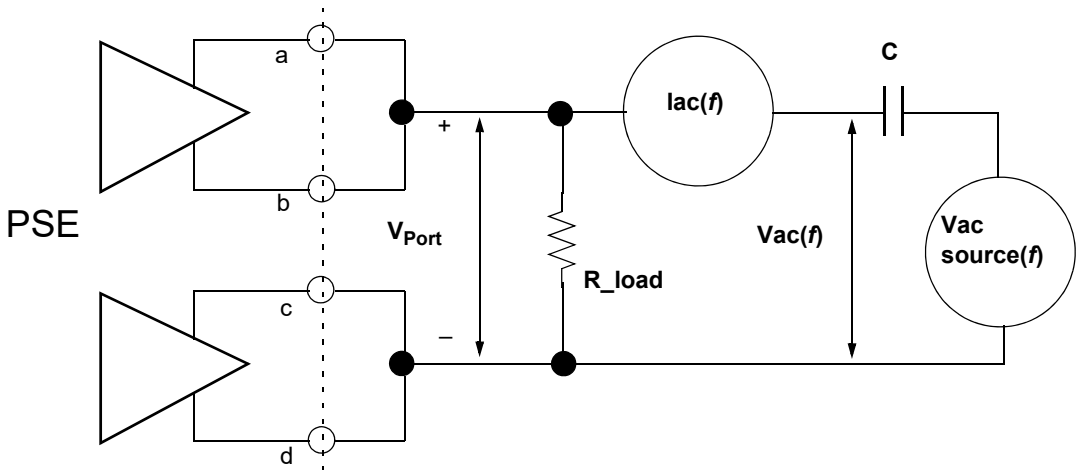

Figure 33A–2—Test setup for measuring Zo_port

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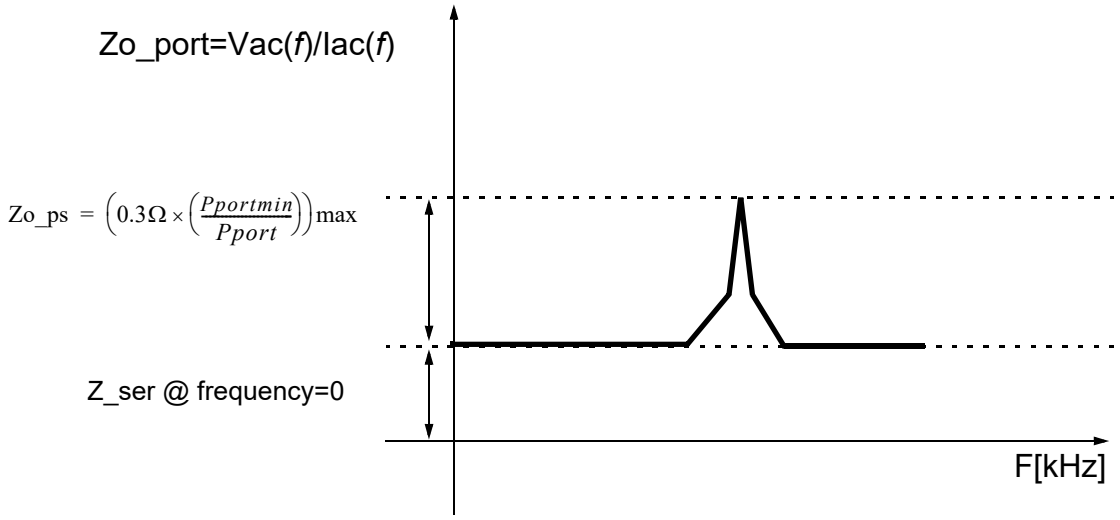

Figure 33A–3—Test requirements for measuring Zo_port

33A.2 Recommended PD design guidelines

PD port input impedance consists of the following two parts:

a) PD port input circuits including the EMI filter (Zin_ser), and
b) PD power supply input impedance (Zin_ps_pd), which is fed by the output of the EMI filter (Zo_emi).

In order to maintain stability with the PSE, the PD power supply input impedance (Zin_ps_pd) should be higher than the output impedance of the total network including the PD EMI output filter impedance fed by the cable (MDI) output impedance, which is fed by the PSE port output impedance.

The worst-case scenario is when the cable (MDI) length is zero (in terms of lower damping factor).

The access to the PD input power supply is not possible through the PD port for evaluating the various impedances and derivation of the above parameters. Because of this, measuring the PD input impedance is a complicated task and the following guidelines should be followed by the PD vendor:

c) The PD power supply input impedance (Zin_ps_pd) at max load of $P_{port} = P_{Port}$ max as defined in Table 33–18 should be higher than 30 Ω at any frequency up to the PD power supply crossover frequency. If the PD power supply is consuming less than $P_{port} = P_{Port}$ max as defined in Table 33–18, then Zin_ps_pd min = $30 \times P_{Port}$ max / P_{port}.
d) The PD power supply EMI filter output impedance should be Zo_emi = 2.7 Ω max. If the PD power supply is consuming less than $P_{port} = P_{Port}$ max, then Zo_emi = $2.7 \times P_{Port}$ max / P_{port}.

See Figure 33A–1 for the PSE-PD system impedance allocation.

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Annex 36A

(informative)

Jitter test patterns

This annex defines test patterns for 1000BASE-X PMDs. The applicability of these patterns is specified in the relevant PMD clauses. The patterns may be implemented at a bit, code-group, or frame level and may be used for transmitter testing. The receiver may not have the capability to accept these diagnostic sequences; however, system debug can be improved if a receiver is able to test for one or more of these patterns and report bit errors (e.g., 8B/10B decoder errors) back to the user.

36A.1 High-frequency test pattern

The intent of this test pattern is to test random jitter (RJ) at a BER of 10^{-12}, and also to test the asymmetry of transition times. This high-frequency test pattern generates a one, or light on, for a duration of 1 bit time, followed by a zero, or light off, for a duration of 1 bit time. This pattern repeats continuously for the duration of the test. For example: 10101010101010101010101010101010101010...

NOTE—This pattern can be generated by the repeated transmission of the D21.5 code-group. Disparity rules are followed.

36A.2 Low-frequency test pattern

The intent of this test pattern is to test low-frequency RJ and also to test PLL tracking error. This low frequency test pattern generates a one, or light on, for a duration of 5 bit times, followed by a zero, or light off, for a duration of 5 bit times. This pattern repeats continuously for the duration of the test. For example: 11111000001111100000111110000011111100000...

NOTE—This pattern can be generated by the repeated transmission of the K28.7 code-group. Disparity rules are followed.

36A.3 Mixed frequency test pattern

The intent of this test pattern is to test the combination of RJ and deterministic jitter (DJ). This mixed frequency test pattern generates a one, or light on, for a duration of 5 bit times, followed by a zero, or light off, for a duration of 1 bit times, followed by a one for 1 bit time followed by a zero for 1 bit time followed by a one for 2 bit times followed by a zero for 5 bit times followed by a one for 1 bit time followed by a zero for 1 bit time followed by a one for 1 bit time followed by a zero for 2 bit times. This pattern repeats continuously for the duration of the test. For example: 11111010110000010100111110101100000101000...

NOTE—This pattern can be generated by the repeated transmission of the K28.5 code-group. Disparity rules are followed.

36A.4 Long continuous random test pattern

The long continuous random test pattern is a random test pattern intended to provide broad spectral content and minimal peaking that can be used for the measurement of jitter at either a component or system level.

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NOTE—The derivation of this pattern may be found in *Fibre Channel Jitter Working Group Technical Report* [B24]. This technical report modified the original RPAT as defined by Fibre Channel so that it would maintain its intended qualities but fit into a Fibre Channel frame. This annex uses similar modifications to fit the same RPAT into an IEEE 802.3 frame.

The long continuous random test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within SPD and EPD delimiters as specified in Clause 36 in the ordinary way. The contents of each packet is composed of the following octet sequences, as observed at the GMII, before 8B/10B coding.

Each packet in the long continuous random test pattern consists of 8 octets of PREAMBLE/SFD, followed by 1512 data octets (126 repetitions of the 12-octet modified RPAT sequence), plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE.

PREAMBLE/SFD:

55 55 55 55 55 55 55 D5

MODIFIED RPAT SEQUENCE (LOOP 126 TIMES)

BE D7 23 47 6B 8F B3 14 5E FB 35 59

CRC

94 D2 54 AC

IPG (TX_EN and TX_ER low)

00 00 00 00 00 00 00 00 00 00 00 00

END

36A.5 Short continuous random test pattern

The short continuous random test pattern is a random test pattern intended to provide broad spectral content and minimal peaking that can be used for the measurement of jitter at either a component or system level.

NOTE—The derivation of this pattern may be found in *Fibre Channel Jitter Working Group Technical Report* [B24]. This technical report modified the original RPAT as defined by Fibre Channel so that it would maintain its intended qualities but fit into a Fibre Channel frame. This annex uses similar modifications to fit the same RPAT into an IEEE 802.3 frame.

The short continuous random test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within SPD and EPD delimiters as specified in Clause 36 in the ordinary way. The contents of each packet is composed of the following octet sequences, as observed at the GMII, before 8B/10B coding.

Each packet in the short continuous random test pattern consists of 8 octets of PREAMBLE/SFD, followed by 348 data octets (29 repetitions of the 12-octet modified RPAT sequence), plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE.

The format of this packet is such that the PCS will generate the following ordered sets for the IPG: /T/ /R/ /I1/ /I2/ /I2/ /I2/ /I2/

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PREAMBLE/SFD:

55 55 55 55 55 55 55 D5

MODIFIED RPAT SEQUENCE (LOOP 29 TIMES)

BE D7 23 47 6B 8F B3 14 5E FB 35 59

CRC

2F E0 AA EF

IPG (TX_EN and TX_ER low)

00 00 00 00 00 00 00 00 00 00 00 00

END

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Annex 36B

(informative)

8B/10B transmission code running disparity calculation examples

Detection of a invalid code-group in the 8B/10B transmission code does not necessarily indicate that the code-group in which the error was detected was the one in which the error occurred. Invalid code-groups may result from a prior error that altered the running disparity of the bit stream but that did not result in a detectable error at the code-group in which the error occurred. The examples shown in Tables 36B–1 and 36B–2 exhibit this behavior. The example shown in Table 36B–3 exhibits the case where a bit error in a received code-group is detected in that code-group, affects the next code group, and error propagation is halted upon detection of the running disparity error.

Table 36B–1—RD error detected two code-groups following error

Stream	Code-group			Code-group			Code-group		
	RD	RD	RD	RD	RD	RD	RD	RD	RD
Transmitted code-group	–	D21.1	–	D10.2	–	D23.5	+		
Transmitted bit stream	–	101010 - 1001	–	010101 – 0101	–	111010 + 1010	+		
Received bit stream	–	101010 - 10**1**1[a]	+	010101 + 0101	+	111010 +[b] 1010	+		
Received code-group	–	D21.0	+	D10.2	+	invalid code-group[b]	+[c]		

[a]Bit error introduced (1001 ⇒ 10**1**1)
[b]Nonzero disparity blocks have to alternate in polarity (+ ⇒ –). In this case, RD does not alternate (+ ⇒ +), the received code group is not found in the Current RD+ column in either Table 36–1a–e or Table 36–2, and an invalid code-group is recognized.
[c]Running disparity is calculated on the received code-group regardless of the validity of the received code-group. Nonzero disparity blocks prevent the propagation of errors and normalize running disparity to the transmitted bit stream (i.e., equivalent to the received bit stream had an error not occurred).

Table 36B–2—RD error detected in next code-group following error

Stream	Code-group			Code-group			Code-group		
	RD	RD	RD	RD	RD	RD	RD	RD	RD
Transmitted code-group	–	D21.1	–	D23.4	–	D23.5	+		
Transmitted bit stream	–	101010 – 1001	–	111010 + 0010	–	111010 + 1010	+		
Received bit stream	–	101010 – 10**1**1[a]	+	111010 +[b] 0010	–	111010 + 1010	+		
Received code-group	–	D21.0	+	invalid code-group[b]	–	D23.5	+		

[a]Bit error introduced (1001 ⇒ 10**1**1)
[b]Nonzero disparity blocks have to alternate in polarity (+ ⇒ –).

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Table 36B–3—A single bit error affects two received code-groups

Stream	Code-group			Code-group			Code-group		
	RD		RD		RD			RD	
Transmitted code-group	–	D3.6 (FCS3)	–	K29.7 (/T/)		–	K23.7 (/R/)		–
Transmitted bit stream	–	110001 - 0110	–	101110 + 1000		–	111010 + 1000		–
Received bit stream	–	110001 - 011**1**[a]	+[b]	101110	+[c] 1000	–	111010 + 1000		–
Received code-group	–	invalid code-group[d]	+	invalid code-group[e]		–	K23.7 (/R/)		–

[a]Bit error introduced (0110 ⇒ 011**1**).
[b]Nonzero disparity blocks have to alternate in polarity (– ⇒ +). Received RD differs from transmitted RD.
[c]Nonzero disparity blocks have to alternate in polarity (+ ⇒ –). Invalid code-group due to RD error since RD remains at +.
[d]Received code-group is not found in either Table 36–1a–e or Table 36–2.
[e]Nonzero disparity blocks prevent the propagation of errors and normalize running disparity to the transmitted bit stream (i.e. equivalent to the received bit stream had an error not occurred). All code-groups contained in PCS End_of_Packet delimiters (/T/R/R or /T/R/K28.5/) include nonzero disparity blocks.

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Annex 38A

(informative)

Fiber launch conditions

38A.1 Overfilled Launch

Overfilled Launch (OFL), as described in IEC 60793-1-4 [B32], is the standard launch used to define optical fiber bandwidth. This launch uniformly overfills the fiber both angularly and spatially. It excites both radial and azimuthal modes of the fiber equally, thus providing a reproducible bandwidth which is insensitive to small misalignments of the input fiber. It is also relatively insensitive to microbending and macrobending when they are not sufficient to affect power distribution carried by the fiber. A restricted launch gives a less reproducible bandwidth number and is dependent on an exact definition of the launch. Overfilled launch is commonly used to measure the bandwidth of LED-based links.

38A.2 Radial Overfilled Launch (ROFL)

A Radial Overfilled Launch is created when a multimode optical fiber is illuminated by the coherent optical output of a source operating in its lowest order transverse mode in a manner that excites predominantly the radial modes of the multimode fiber. This contrasts with the OFL, which is intended to excite both radial and azimuthal modes of the fiber equally. In practice an ROFL is obtained when

a) A spot of laser light is projected onto the core of the multimode fiber,
b) The laser spot is approximately symmetrical about the optical center of the multimode fiber,
c) The optical axis of both the fiber and the laser beam are approximately aligned,
d) The angle of divergence of the laser beam is less than the numerical aperture of the multimode fiber,
e) The laser spot is larger than the core of the multimode fiber.

An ROFL cannot be created using a multi-transverse mode laser or by simply projecting a speckle pattern through an aperture.

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Annex 40A

(informative)

Additional cabling design guidelines

This annex provides additional cabling guidelines when installing a new Category 5/Class D balanced cabling system or using an existing Category 5/Class D balanced cabling system. These guidelines are intended to supplement those in Clause 40. 1000BASE-T is designed to operate over 4-pair twisted-pair cabling systems that meet the requirements described in ANSI/TIA/EIA-568-A-1995 (Category 5) and ISO/IEC 11801:1995 (Class D), and the additional transmission parameters of return loss, ELFEXT loss, and MDELFEXT loss specified in 40.7. There are additional steps that may be taken by network designers that provide additional operating margins and ensure the objective BER of 10^{-10} is achieved. Cabling systems that meet or exceed the specifications in 40.7 for a worst case 4-connector topology are recommended for new installations. Whether installing a new Category 5/Class D balanced cabling system or reusing one that is already installed, it is highly recommended that the cabling system be measured/certified before connecting 1000BASE-T equipment following the guidelines in ANSI/EIA/TIA 568-B1 Annex D.

40A.1 Alien crosstalk

40A.1.1 Multipair cabling (i.e., greater than 4-pair)

Multiple Gigabit Ethernet links [(n*4-Pair) with n greater than 1] should not share a common sheath as in a 25-pair binder group in a multipair cable. When the multipair cable is terminated into compliant connecting hardware (TIA does not specify 25 position connecting hardware), the NEXT loss contributions between the adjacent 4-pair Gigabit Ethernet link, from connecting hardware and the cable combined, cannot be completely cancelled.

40A.1.2 Bundled or hybrid cable configurations

Another source of alien crosstalk can occur in a bundled or hybrid cable configuration where two or more 4-pair cables are assembled together.

In order to limit the noise coupled between adjacent 1000BASE-T link segments in a bundled or hybrid cable configuration, the PSNEXT loss between a 1000BASE-T duplex channel in a link segment and all duplex channels in adjacent 1000BASE-T link segments should be greater than $35 - 15*\log(f/100)$ (dB) at all frequencies from 1 MHz to 100 MHz.

40A.2 Cabling configurations

The primary application for the Clause 40 specification is expected to be between a workstation and the local telecommunications closet. In commercial buildings this application is generally referred to as the horizontal cabling subsystem. As specified in ISO/IEC 11801:1995 the maximum length of a horizontal subsystem building wiring channel is 100 m. The channel consists of cords, cables, and connecting hardware. The maximum configuration for this channel is shown in Figure 40A–1.

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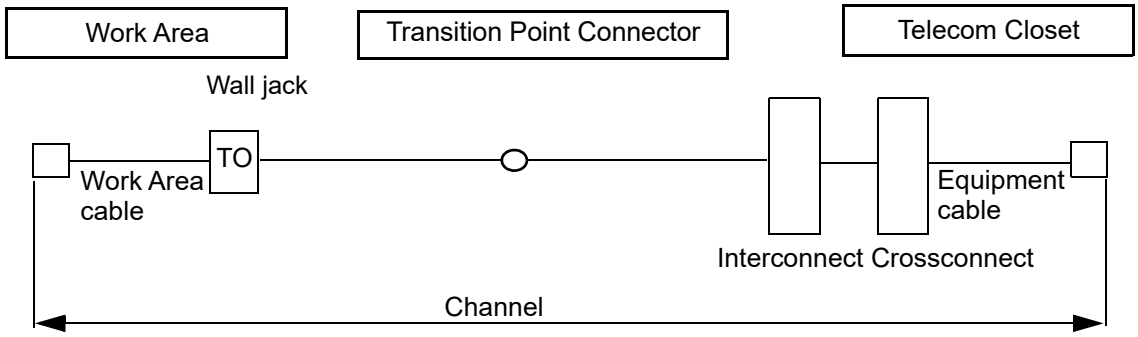

Figure 40A–1—Maximum horizontal subsystem configuration

On the other hand, a minimum configuration can be achieved by removing the patch cord and transition point, which is shown in Figure 40A–2.

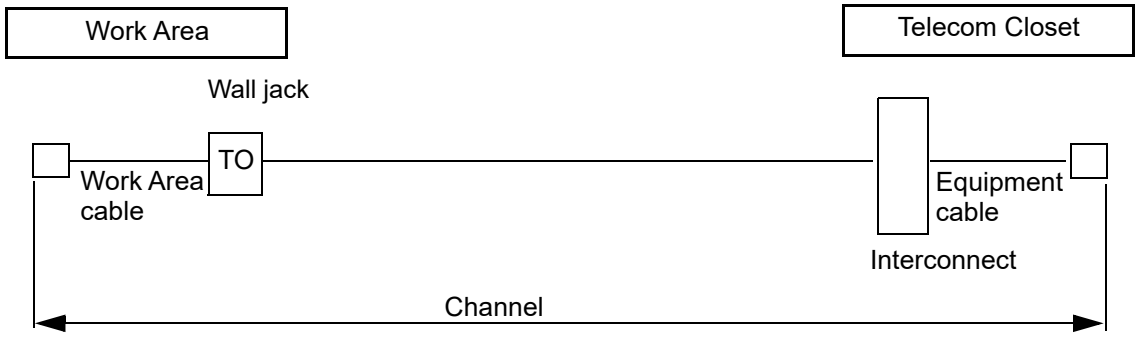

Figure 40A–2—Minimum horizontal subsystem configuration

1000BASE-T is designed to operate over a channel that meets the specifications of 40.7 and the channel configuration shown in Figure 40A–1. However, if the channel specifications of 40.7 cannot be met when using the channel configuration shown in Figure 40A–1, the configuration shown in Figure 40A–2 is recommended. This optimized channel for a 1000BASE-T link segment deletes the transition point and runs an equipment patch cord directly between the LAN equipment and the connector termination of the permanent link. This reduces the number of connectors and their associated crosstalk in the link. The minimum link configuration:

a) Minimizes crosstalk, both near-end and far-end, which maximizes the BER margin; and
b) Minimizes link insertion loss.

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Annex 40B

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Description of cable clamp

This annex describes the cable clamp used in the common-mode noise rejection test of 40.6.1.3.3, which is used to determine the sensitivity of the 1000BASE-T receiver to common-mode noise from the link segment. As shown in Figure 40B–1, the clamp is 300 mm long, 58 mm wide, 54 mm high with a center opening of 6.35 mm (0.25 in). The clamp consists of two halves that permit the insertion of a cable into the clamp.

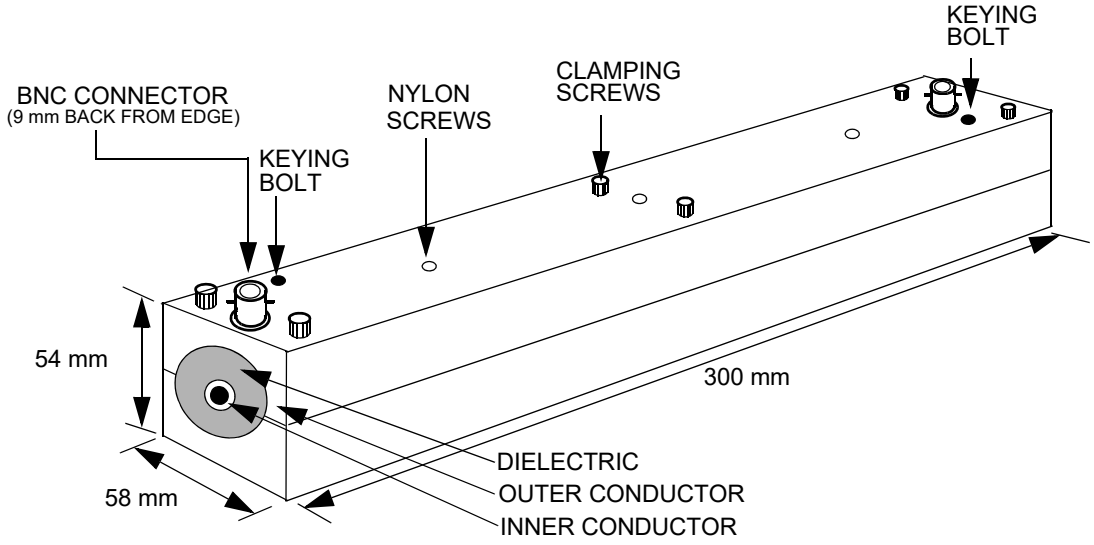

Figure 40B–1—Cable clamp

The clamp has a copper center conductor and an aluminum outer conductor with a high density polyethylene dielectric. The following is a review of the construction and materials of the clamp:

a) *Inner conductor*—Copper tubing with an inner diameter of 6.35 mm (0.25 in) and an outer diameter of 9.4 mm (0.37 in).
b) *Outer conductor*—Aluminum bar that is 300 mm long and approximately 54 mm by 58 mm. The bar is milled to accept the outer diameter of the dielectric material.
c) *Dielectric*—High Density Polyethylene (Residual, TypeF) with dielectric constant of 2.32. An outside diameter of 33.5 mm and an inner diameter that accepts the outside diameter of the copper inner conductor.
d) *Connectors*—BNC connectors are located 9 mm (0.39 in) from each end of the clamp and are recessed into the outer conductor. The center conductor of the connector is connected to the inter conductor as shown in Figure 40B–2.
e) *Clamping screws*—Six screws are used to connect the two halves of the clamp together after the cable has been inserted. Although clamping screws are shown in Figure 40B–1, any clamping method may be used that ensures the two halves are connected electrically and permits quick assembly and disassembly.
f) *Nylon screws*—Used to align and secure the inner conductor and dielectric to the outer conductor. The use and location of the screws is left to the manufacturer.

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g) *Keying bolts*—Two studs used to align the two halves of the clamp.

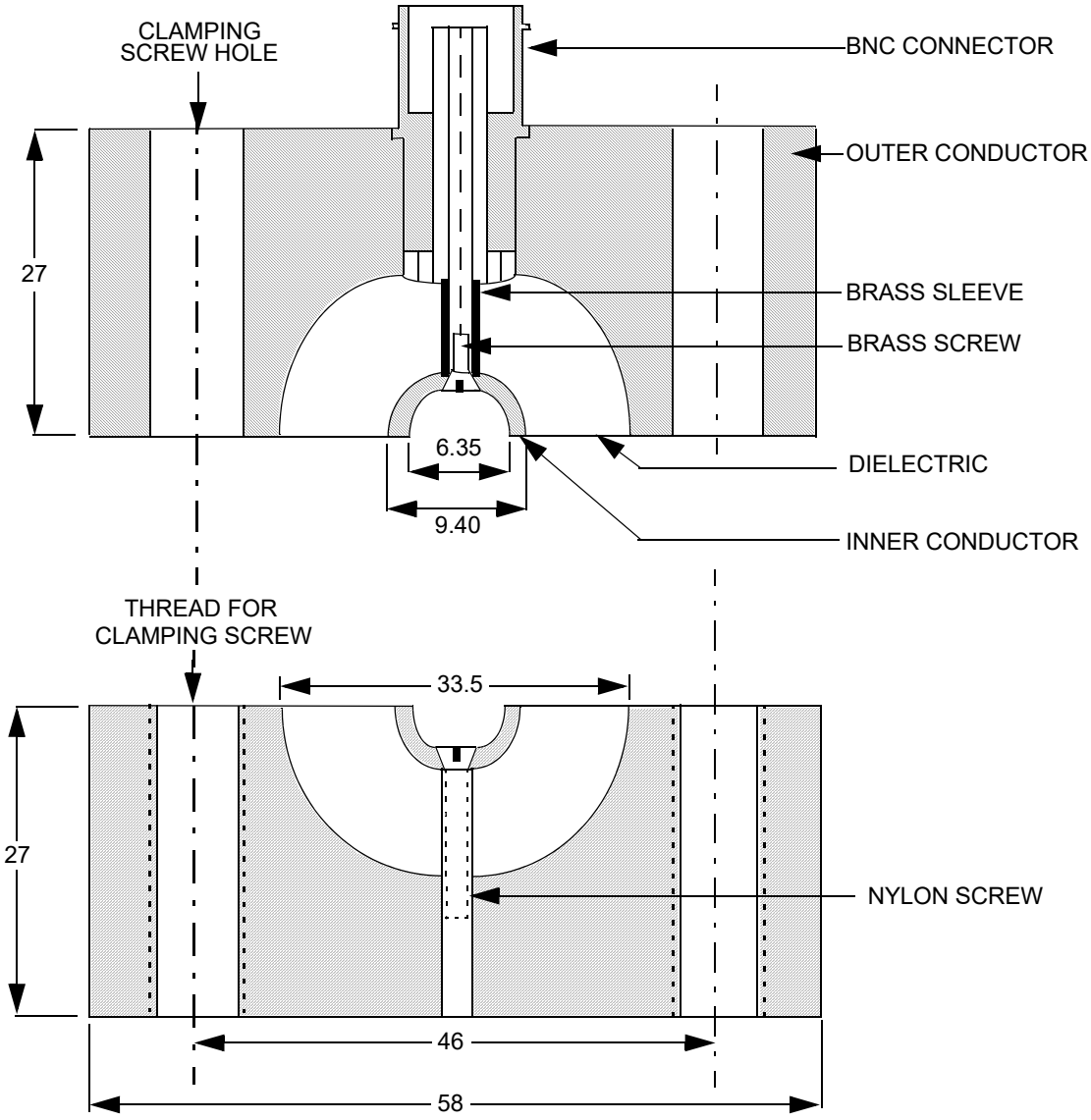

Figure 40B–2—Cross-section of cable clamp

As shown in Figure 40B–2 the inner conductor on the bottom half of the clamp extends slightly (~ 0.1mm) above the dielectric to ensure there is good electrical connection with the inner conductor of the top half of the clamp along the full length of the conductor when the two halves are clamped together.

The electrical parameters of the clamp between 1MHz and 250 MHz are as follows:

a) Insertion loss: < 0.2 dB

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b) Return loss: > 20.0 dB

40B.1 Cable clamp validation

In order to ensure the cable clamp described above is operating correctly, the following test procedure is provided. Prior to conducting the following test shown in Figure 40B–3, the clamp should be tested to ensure the insertion loss and return loss are as specified above. The cable clamp validation test procedure uses a well-balanced 4-pair Category 5 unshielded test cable or better that meets the specifications of 40.7. The test hardware consists of the following:

a) *Resistor network*—Network consists of three 50 ±0.1% Ω resistors; two resistors are connected in series as a differential termination for cable pairs and the other resistor is connected between the two and the ground plane as a common-mode termination.
b) *Balun*—3 ports, laboratory quality with a 100 Ω differential input, 50 Ω differential output, and a 50 Ω common-mode output:
   Insertion Loss (100 Ω balanced <->50 Ω unbalanced): <1.2 dB (1-350MHz)
   Return Loss: >20 dB (1-350 MHz)
   Longitudinal Balance: >50 dB (1-350 MHz)
c) *Test cable*—4-pair 100 Ω UTP category 5 balanced cable at least 30 m long.
d) *Chokes (2)*—Wideband Ferrite Material:
   Inter-diameter: 6.35 to 6.86 mm
   Impedance: 250 Ω @ 100 MHz
e) *Ground plane*—Copper sheet or equivalent.
f) *Signal generator*
g) *Oscilloscope*
h) *Receiver*

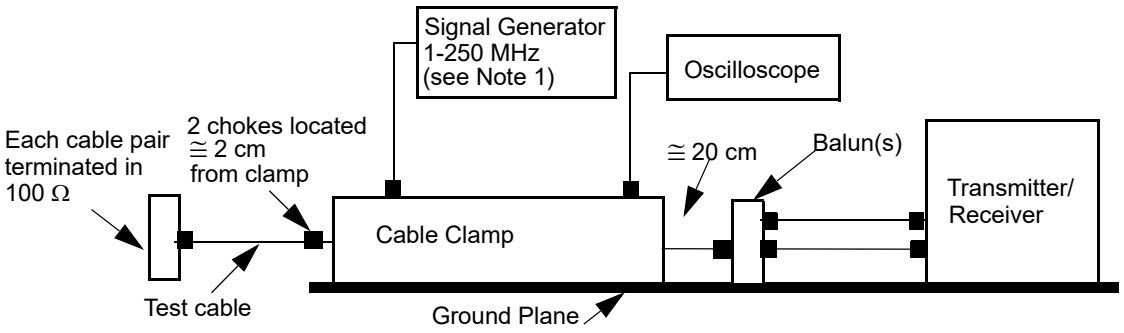

Figure 40B–3—Cable clamp validation test configuration

With the test cable inserted in the cable clamp, a signal generator with a 50 Ω output impedance is connected to one end of the cable clamp and an oscilloscope with a 50 Ω input impedance is connected to the other end. The signal generator shall be capable of providing a sine wave signal of 1 MHz to 250 MHz. The output of the signal generator is adjusted for a voltage of 1.0 Vrms (2.83 Vpp) at 20 MHz on the oscilloscope. The remainder of the test is conducted without changing the signal generator voltage. The cable pairs not connected to the balun are terminated in a resistor network, although when possible it is recommended that each cable pair be terminated in a balun. It very important that the cable clamp, balun, receiver, and resistor networks have good contact with the ground plane. The two chokes, which are located next to each other, are

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located approximately 2.0 cm from the clamp. The cable between the clamp and the balun should be straight and not in contact with the ground plane.

The differential-mode and common-mode voltage outputs of the balun should meet the limits shown in Table 40B–1 over the frequency range 1 MHz to 250 MHz for each cable pair. The differential mode voltage at the output of the balun has to be increased by 3 dB to take into account the 100-to-50 impedance matching loss of the balun.

Table 40B–1—Common- and differential-mode output voltages

Frequency (*f*)	Common-mode voltage	Differential-mode voltage
1-30 MHz	<0.1+0.97(f/30) Vpp	<2.4 + 19.68 (f/30) mVpp
30-80 MHz	<1.07 Vpp	<22 mVpp
80-250 MHz	<1.07 – 0.6 (f-80)/170 Vpp	<22 mVpp

NOTE—Prior to conducting the validation test the cable clamp should be tested without the cable inserted to determine the variation of the signal generator voltage with frequency at the output of the clamp. The signal generator voltage should be adjusted to 1 Vrms (2.83 Vpp) at 20 MHz on the oscilloscope. When the frequency is varied from 20 MHz to 250 MHz, the voltage on the oscilloscope should not vary more than ±7.5%. If the voltage varies more than ±7.5%, then a correction factor has to be applied at each measurement frequency.

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Annex 40C

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Add-on interface for additional Next Pages

This annex describes a technique for implementing Auto-Negotiation for 1000BASE-T when the implementer wishes to send additional Next Pages (other than those required to configure for 1000BASE-T operation). To accomplish this mode of Auto-Negotiation, the implementer has to ensure that the three Next Pages required for 1000BASE-T configuration are sent first.

The add-on interface described in this annex shows one technique for supporting the transmission of additional Next Pages. This mechanism utilizes the existing Clause 28 Auto-Negotiation mechanism and variables defined in Clause 28. Its purpose is merely to provide optional NEXT PAGE WAIT responses to the Auto-Negotiation Arbitration state diagram (see Figure 28–18).

The add-on interface for Auto-Negotiation is intended to interface directly between the defined registers and the Auto-Negotiation mechanism defined in Clause 28. The mechanism described includes five main blocks (see Figure 40C–1).

The first three blocks are used by the MASTER-SLAVE resolution function. They are used to generate and store random seeds and to resolve the status of the MASTER-SLAVE relationship. Their operation is described later in this annex. The final two blocks, the transmit state diagram for the 1000BASE-T Next Page exchange and the receive state diagram for the 1000BASE-T Next Page exchange, are described in this annex.

NOTE—Annex K defines optional alternative terminology for “master” and “slave”.

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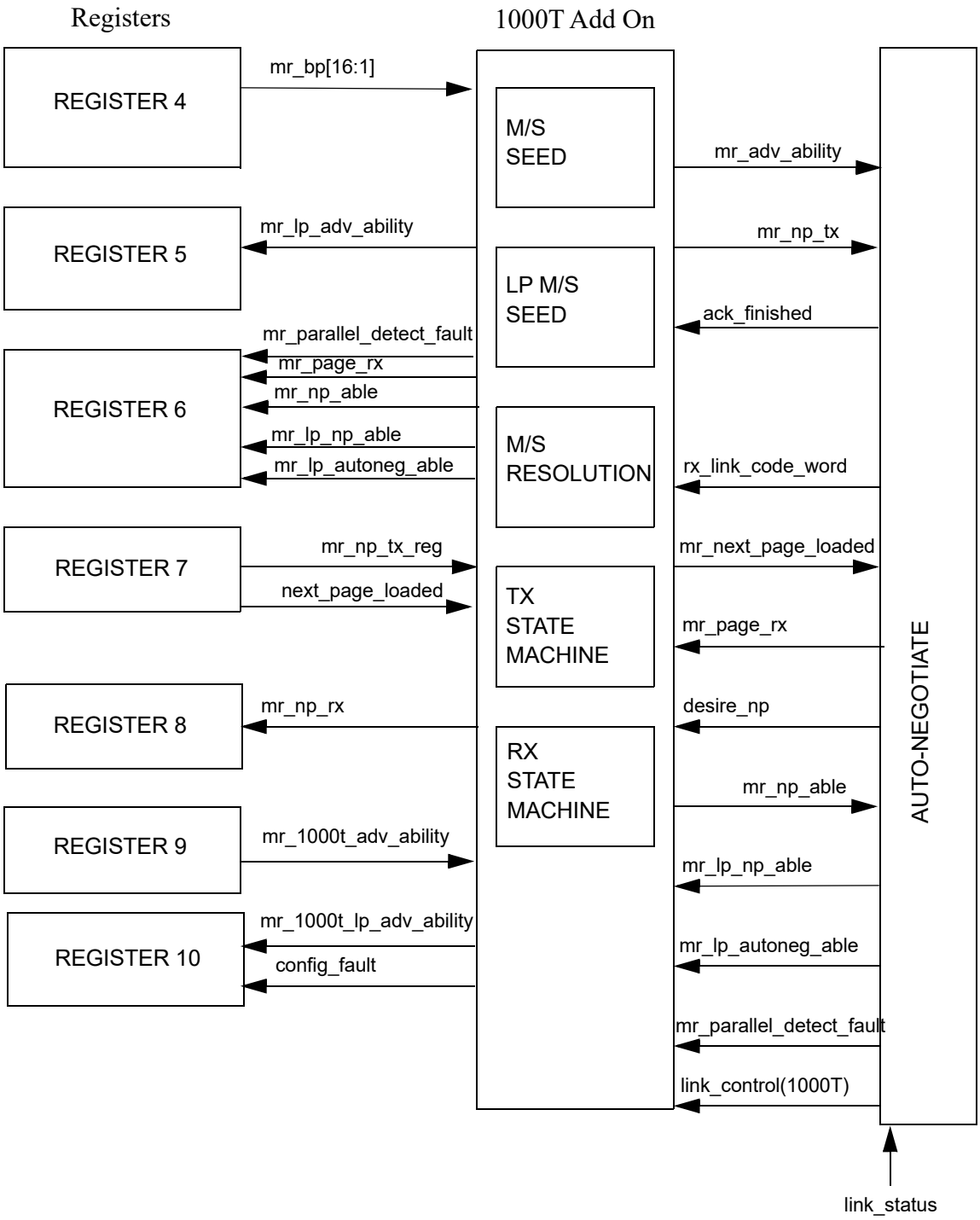

Figure 40C–1—Auto-Negotiate add-on diagram for 1000BASE-T

NOTE—When the exchange of Next Pages is complete, the MASTER-SLAVE relationship can be determined using Table 40–5 with the 1000BASE-T Technology Ability Next Page bit values specified in Table 40–4 and information received from the link partner. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown in the Auto-Negotiation Arbitration state diagram (Figure 28–18).

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40C.1 State variables

ATMP_CNT
: This variable is used to count the number of failed MASTER-SLAVE resolutions. It has a maximum value of 7.

config_fault
: This variable indicates the result of the MASTER-SLAVE resolution function.

desire_1000T_adv
: The local device desires a 1000BASE-T link.
Values: true; bits 9.8 or 9.9 do not contain a logic zero.
false; bits 9.8 and 9.9 both contain a logic zero.

mr_bp
: This variable is used as an intermediate signal from register 4. Normally register 4 would directly source the mr_adv_ability information. This information is now sourced from the transmit state machine.

mr_1000t_adv_ability
: A 16-bit array used to store and indicate the contents of register 9.

mr_1000t_lp_adv_ability
: A 16-bit array used to write information to register 10.

mr_np_tx_reg
: This variable is an intermediate signal from register 7. Normally register 7 would directly source the information to the Auto-Negotiation function via mr_np_tx. This information is now sourced from the transmit state diagram.

mr_np_rx
: A 16-bit array used to write information to register 8.
Values: Zeros; data bit is logical zero.
One; data bit is logical one.

next_page_loaded
: This variable is an intermediate signal from register 7. Normally register 7 would directly source the information to the Auto-Negotiation function via mr_next_page_loaded. This information is now sourced from the transmit state diagram.

reg_random
: An 11-bit array used to store the received random seed from the link partner. It is used by the MASTER-SLAVE resolution function.

All other signals are defined in Clause 28.

40C.2 State diagrams

40C.2.1 Auto-Negotiation Transmit state diagram add-on for 1000BASE-T

The Auto-Negotiation transmit state diagram add-on (see Figure 40C–2) is responsible for sending the Base Page, 1000BASE-T Next Pages, as well as additional Next Pages as specified by the management interface.

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1000BASE-T Next Pages will automatically be sent by the PHY whenever there are no additional Next Pages to be sent. If the user desires to send additional Next Pages, then the user has to first send three pages of any format. Management will automatically replace these three pages with the appropriate 1000BASE-T Message Page and the two following unformatted pages and then will send the additional Next Pages as specified by the user. All other steps are performed by the management interface. The management interface is now required to complete the Next Page exchange by sourcing its own NULL page. This is shown in Figure 40C–2 for illustration only.

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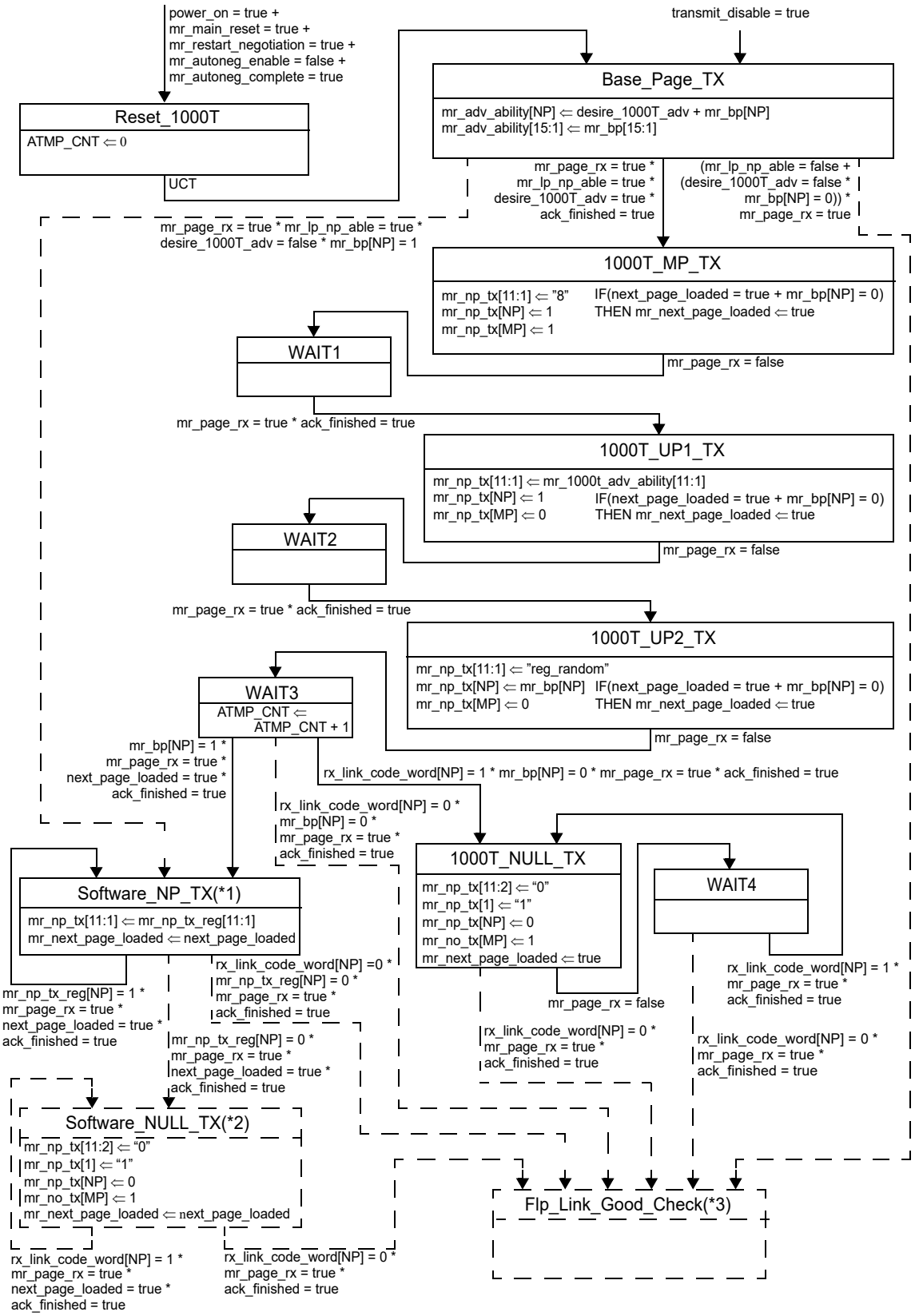

Figure 40C–2—Auto-Negotiation Transmit state diagram add-on for 1000BASE-T

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NOTES for Figure 40C–2

1—(Software_NP_TX) If the user desires to send additional Next Pages, then the contents of the first three Next Pages will be overwritten by the three 1000BASE-T Next Pages. In this case, the user is responsible for stepping through the Next Page sequence (by creating the initial three Next Pages to be overwritten by the three 1000BASE-T Next Pages); otherwise the process is automatic. (next_page_loaded signals clear operation as per Clause 28.)

2—(Software_NULL_TX) This is shown for illustration only. This is done in software and is required.

3—(Flp_Link_Good_Check) This is shown for illustration only. This state is from the Auto-Negotiation Arbitration state diagram and indicates the conclusion of pages being sent. (The transition desire_1000T_adv = false is to show sequence for non 1000BASE-T implementations.)

40C.2.2 Auto-Negotiation Receive state diagram add-on for 1000BASE-T

The Auto-Negotiation receive state diagram add-on for 1000BASE-T Next Pages (see Figure 40C–3) is responsible for receiving the Base Page, 1000BASE-T Next Pages, and any additional Next Pages received. 1000BASE-T Next Pages will automatically be received whenever the user does not wish to participate in Next Page exchanges. In this case, the appropriate 1000BASE-T message page and its two unformatted pages will automatically be received and stored in their appropriate registers. Any additional Next Pages received will still be placed in register 8, but will be overwritten automatically when a new page is received. The net result is that the management interface does not need to poll registers 6 and 8. The information in register 8 will be meaningless in this case. If the user desires to participate in additional Next Page exchanges via setting the appropriate bit in register 4, the user now becomes responsible (as was previously the case) for defining how this will be accomplished. In this situation, the first three Next Pages received may be 1000BASE-T and should be discarded. This information will automatically be stored internally in the appropriate register 10 and reg_random. The management interface/user can ignore the information received for the 1000BASE-T Next Pages.

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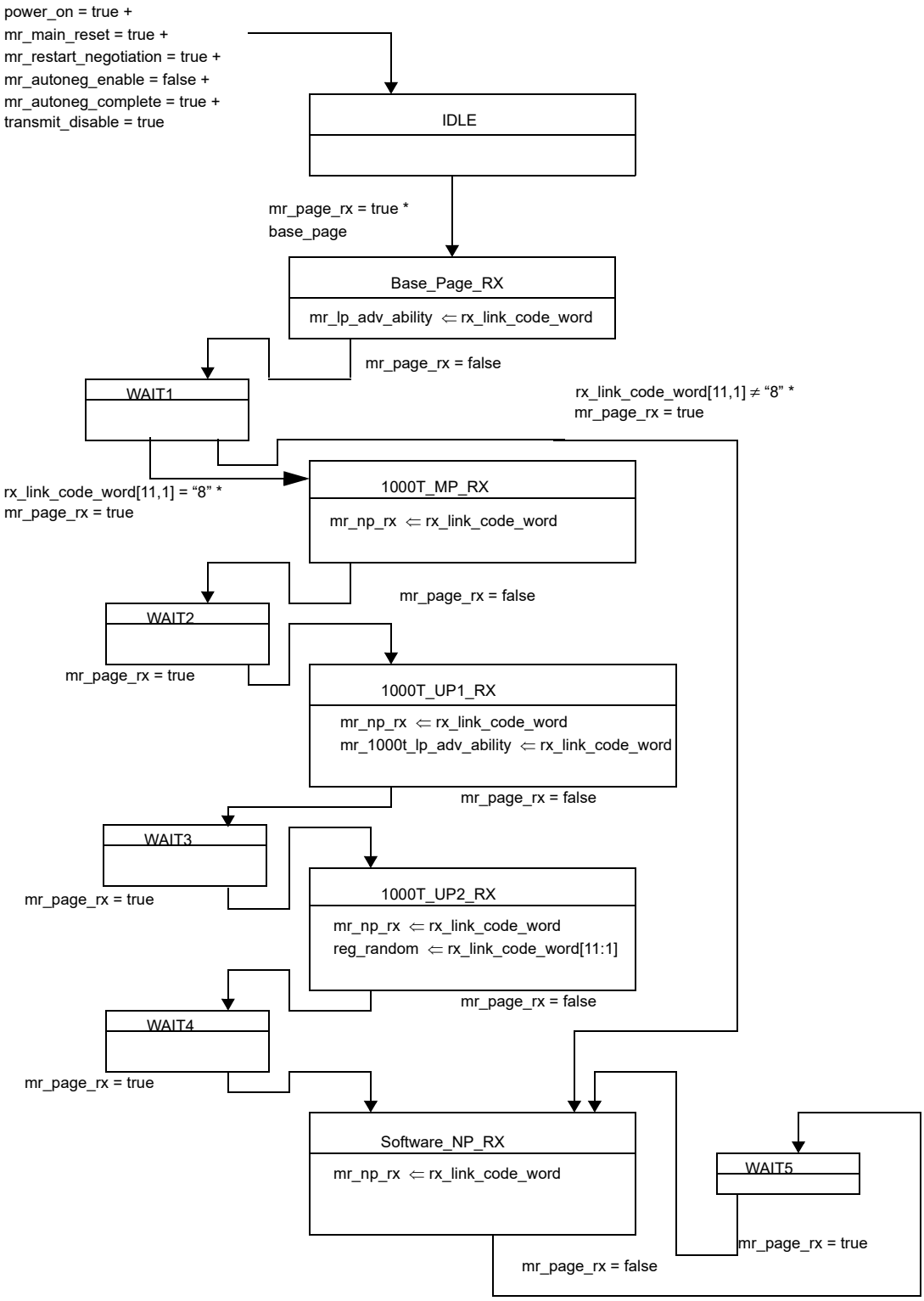

Figure 40C–3—Auto-Negotiation Receive state diagram add-on for 1000BASE-T

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Annex 43A

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Annex 43A is no longer in use.

NOTE—The Link Aggregation specification, including Annex 43A, *Collection and Distribution functions,* was moved to IEEE Std 802.1AX-2008 during the IEEE Std 802.3-2008 revision.

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Annex 43B

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Annex 43B is no longer in use.

NOTE—When the Link Aggregation specification contained in Clause 43, Annex 43A, and Annex 43 C were moved to IEEE Std 802.1AX-2008 during the IEEE Std 802.3-2008 revision the content of Annex 43B was moved to become Annex 57A.

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Annex 43C

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Annex 43C is no longer in use.

NOTE—The Link Aggregation specification, including Annex 43C ‘LACP standby link selection and dynamic Key management’ was moved to IEEE Std 802.1AX-2008 during the IEEE Std 802.3-2008 revision.

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Annex 44A

(informative)

Diagram of Data Flow

This annex contains diagrams of the data flow from the MAC to the MDI in the transmit direction and from the MDI to the MAC in the receive direction. The diagrams are provided as a reference, and the corresponding clause should be reviewed for the complete information.

44A.1 10GBASE-R bit ordering

Figure 44A–1 shows the bit ordering on the LAN serial transmit data path.

Figure 44A–2 shows the bit ordering on the LAN serial receive data path.

The 10GBASE-R diagrams reference the following clauses: 46 (XGMII and RS), 47 (XGXS and XAUI), 49 (64B/66B PCS), and 51 (serial PMA).

44A.2 10GBASE-W serial bit ordering

Figure 44A–3 shows the bit ordering on the WAN serial transmit data path.

Figure 44A–4 shows the bit ordering on the WAN serial receive data path.

The 10GBASE-W serial diagrams reference the following clauses: 46 (XGMII and RS), 47 (XGXS and XAUI), 49 (64B/66B PCS), 50 (WIS), and 51 (serial PMA).

44A.3 10GBASE-LX4 bit ordering

Figure 44A–5 shows the bit ordering on the LAN WDM transmit path.

Figure 44A–6 shows the bit ordering on the LAN WDM receive path.

The 10GBASE-LX4 diagrams reference the following clauses: 46 (XGMII and RS) and 48 (8B/10B PCS and PMA).

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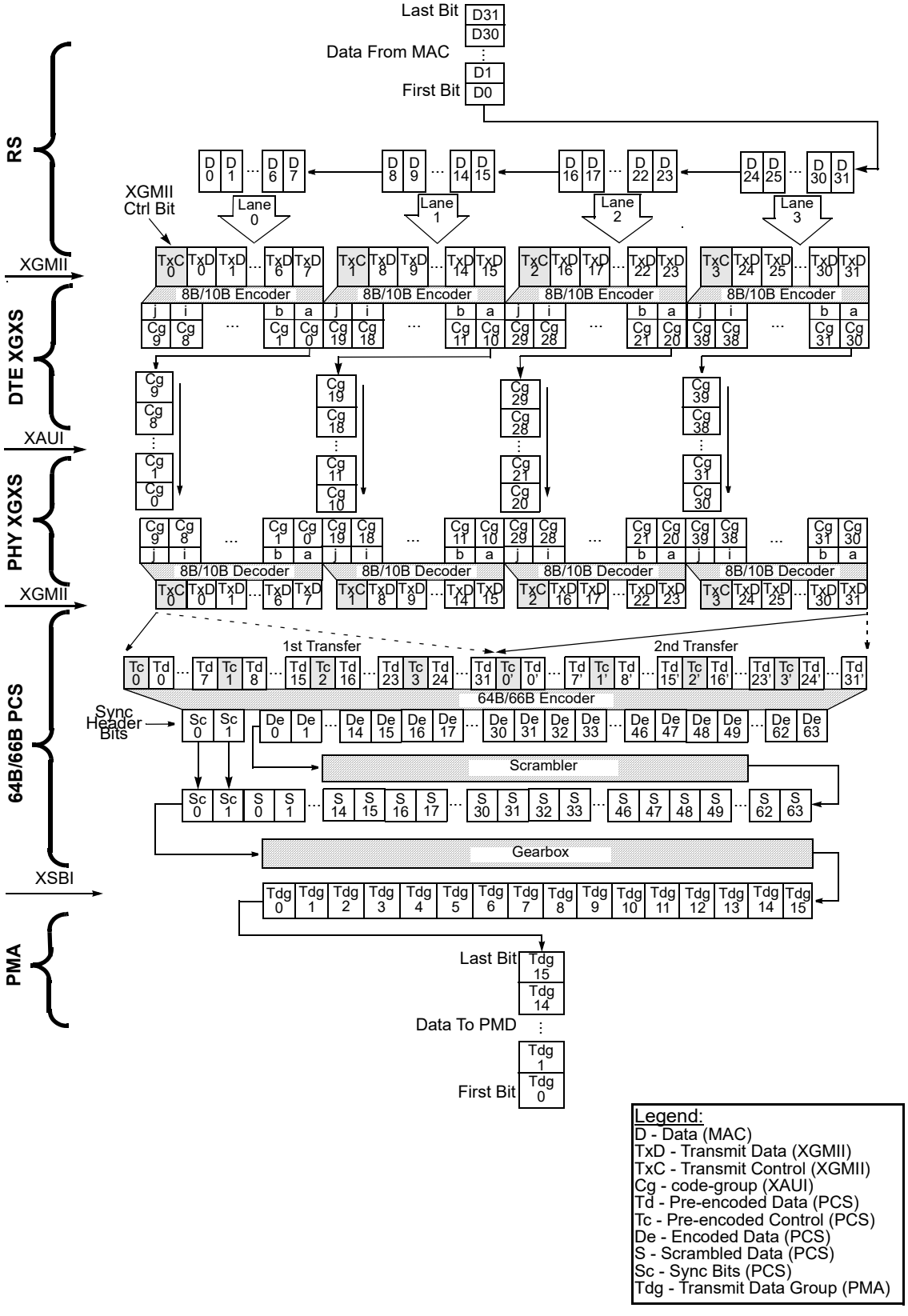

Figure 44A–1—10GBASE-R transmit data path bit ordering

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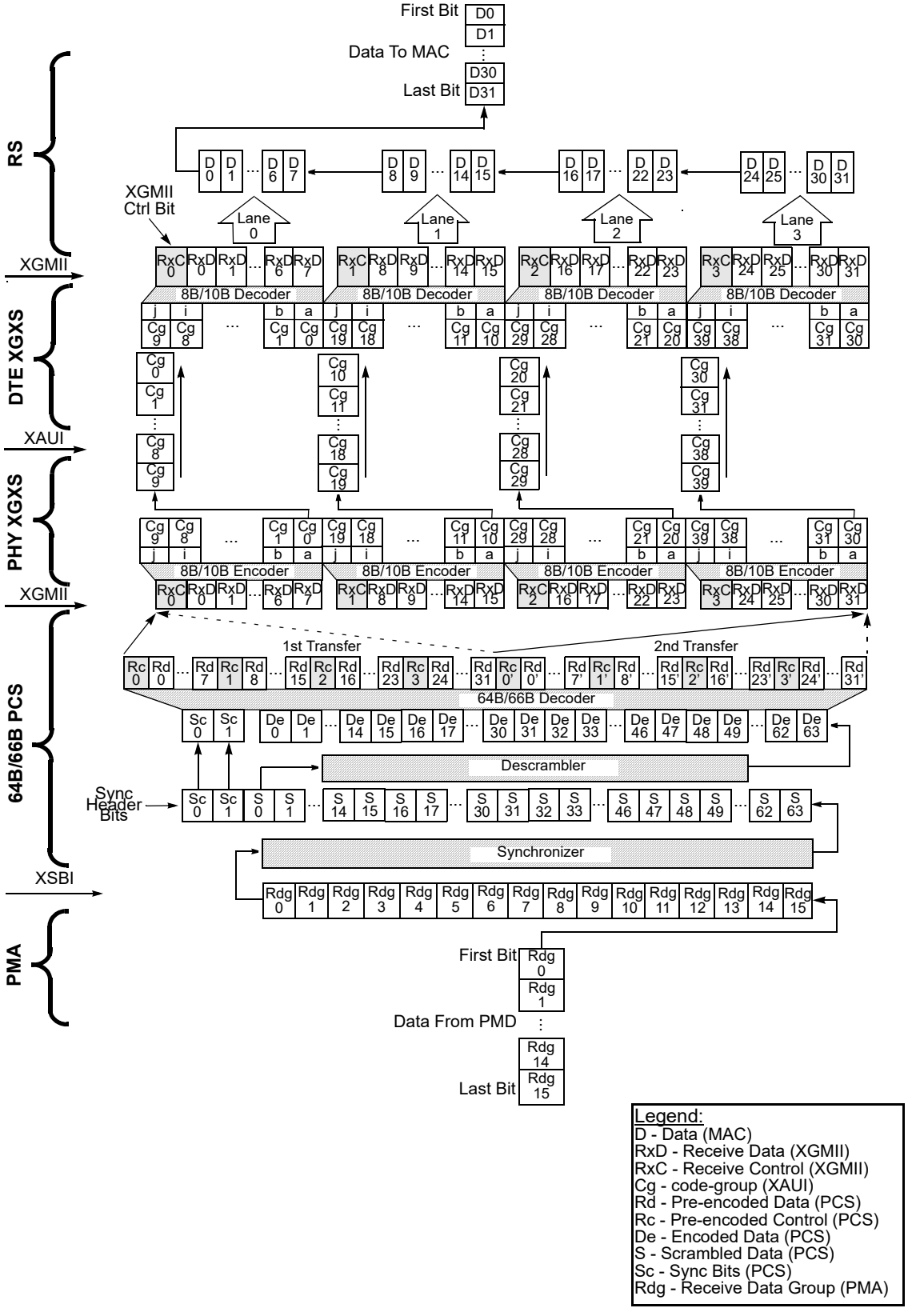

Figure 44A–2—10GBASE-R receive data path bit ordering

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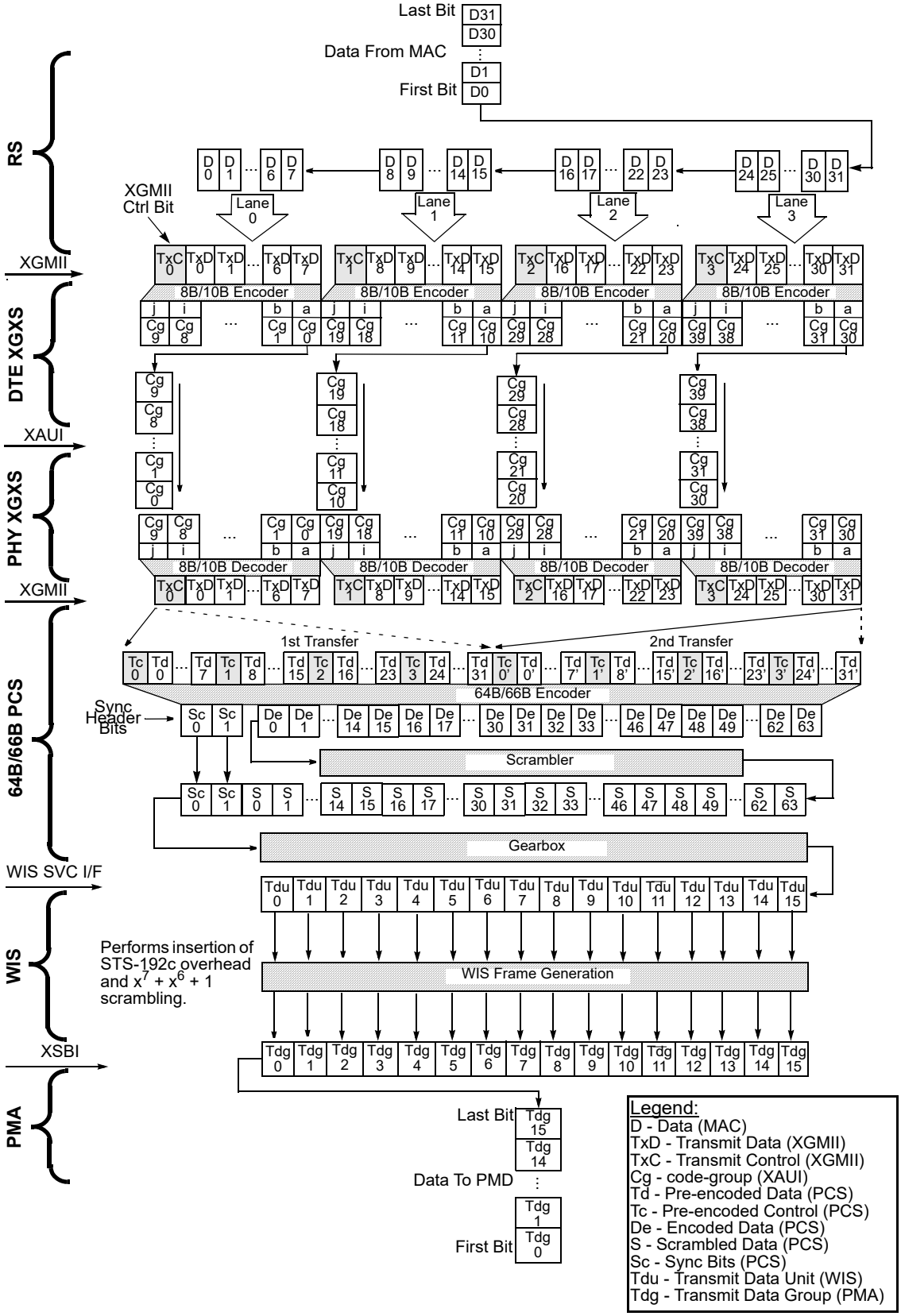

Figure 44A–3—10GBASE-W serial transmit data path bit ordering

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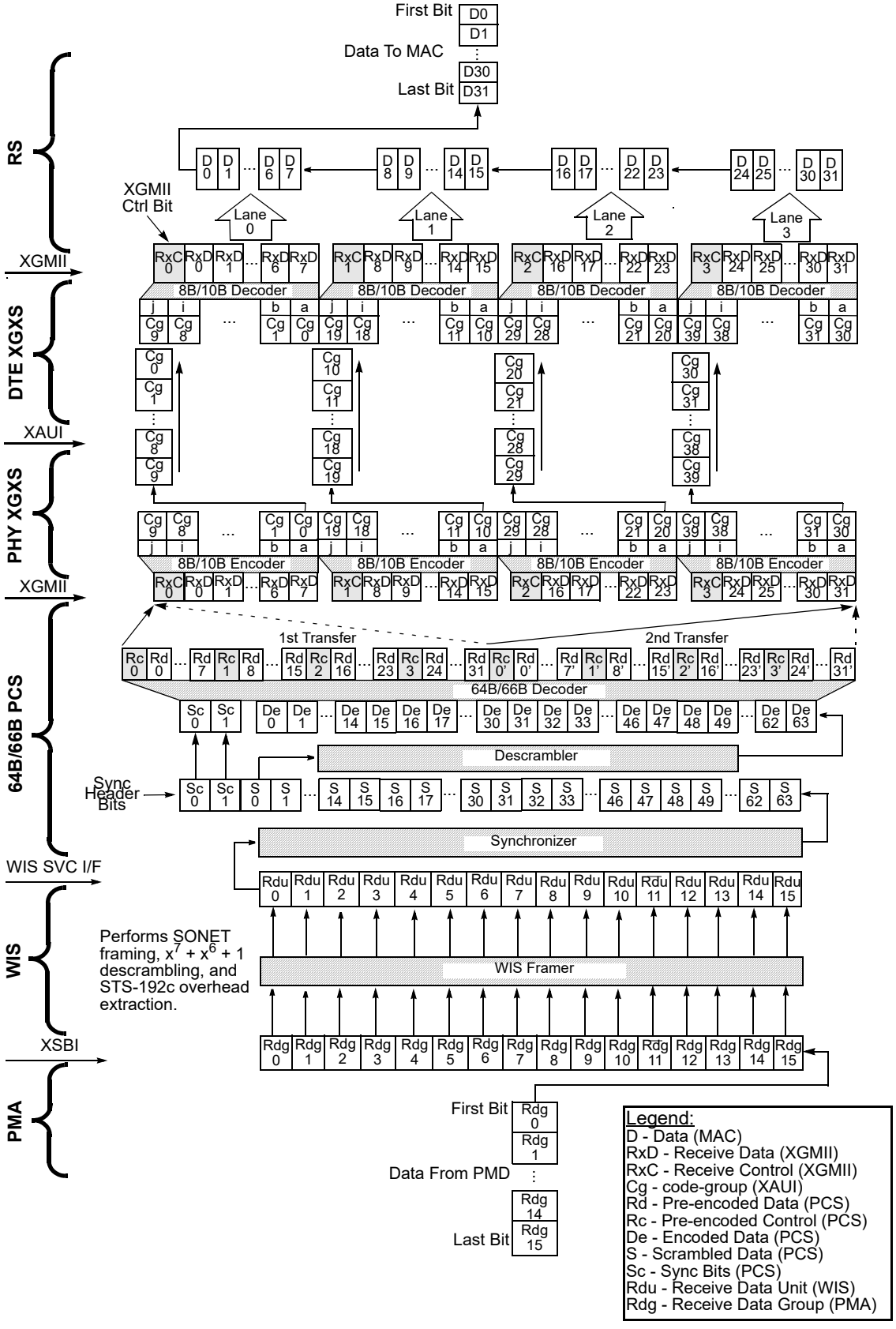

Figure 44A–4—10GBASE-W serial receive data path bit ordering

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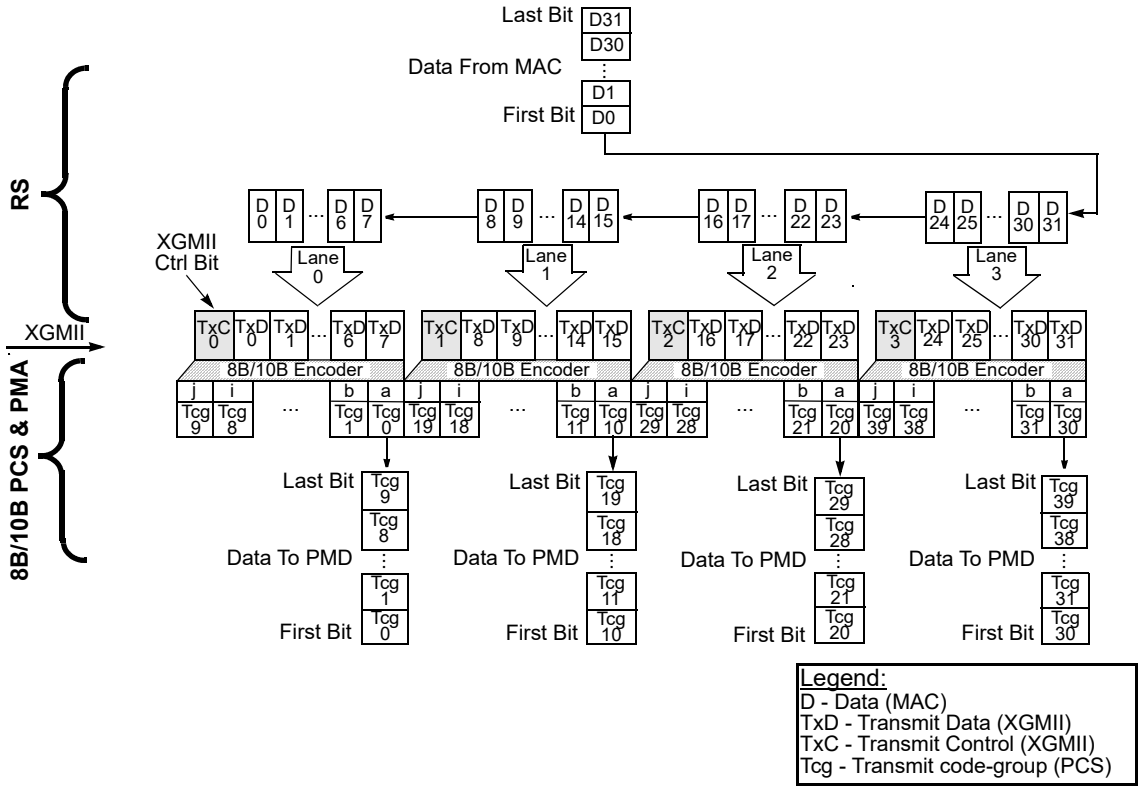

Figure 44A–5—10GBASE-LX4 transmit data path bit ordering

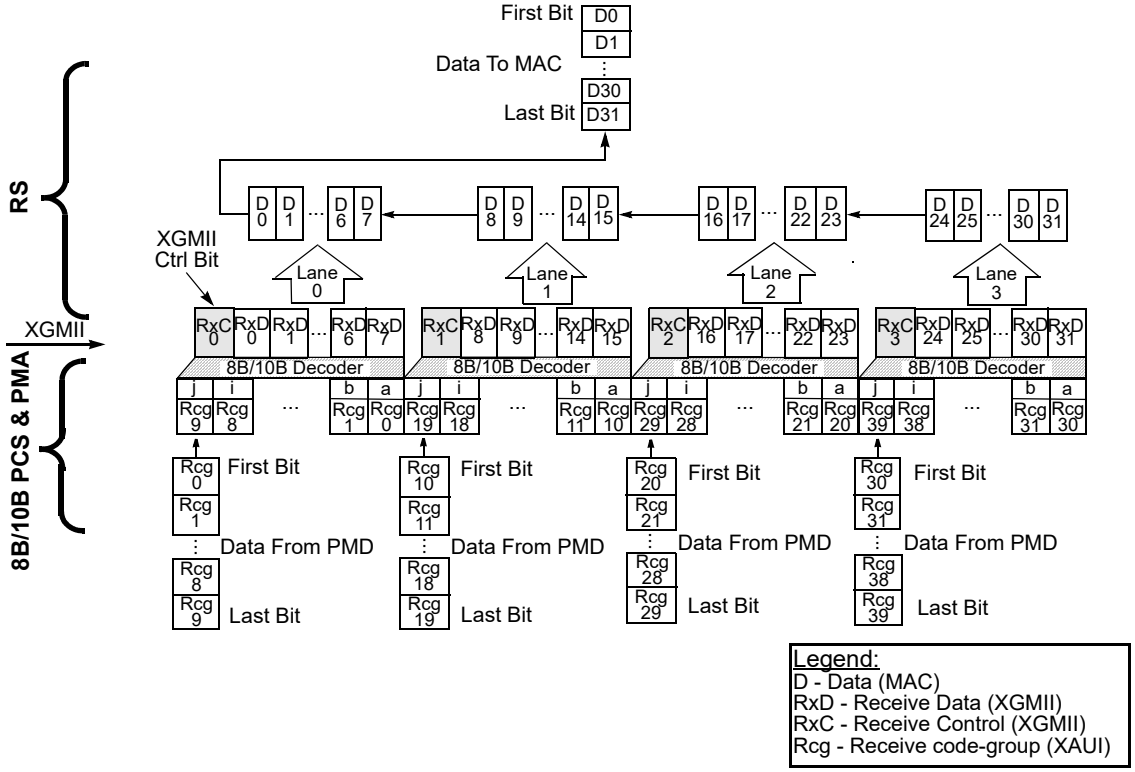

Figure 44A–6—10GBASE-LX4 receive data path bit ordering

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44A.4 Loopback locations

Figure 44A–7 diagrams the impact of the various loopback signals on the generation of signal detect and local fault. Clause 46 describes the handling of local fault via the XGMII. If the WIS is not present, the PMA_SIGNAL.indication passes directly from the PMA sublayer to the PCS as is the case in 10GBASE-X and 10GBASE-R devices.

Figure 44A–7 represents an implementation of loopback where loopback is implemented in accordance with the recommendation that it exercises as much of the circuitry in the sublayer as possible. If the loopback is implemented above part of the circuitry in a sublayer, then any data valid signals produced below the loopback point should be ignored during loopback as are any data valid signals from below the sublayer. For instance, if loopback in a WIS implementation was done above the framer, then data valid signals from the framer should be logically OR'ed with loopback.

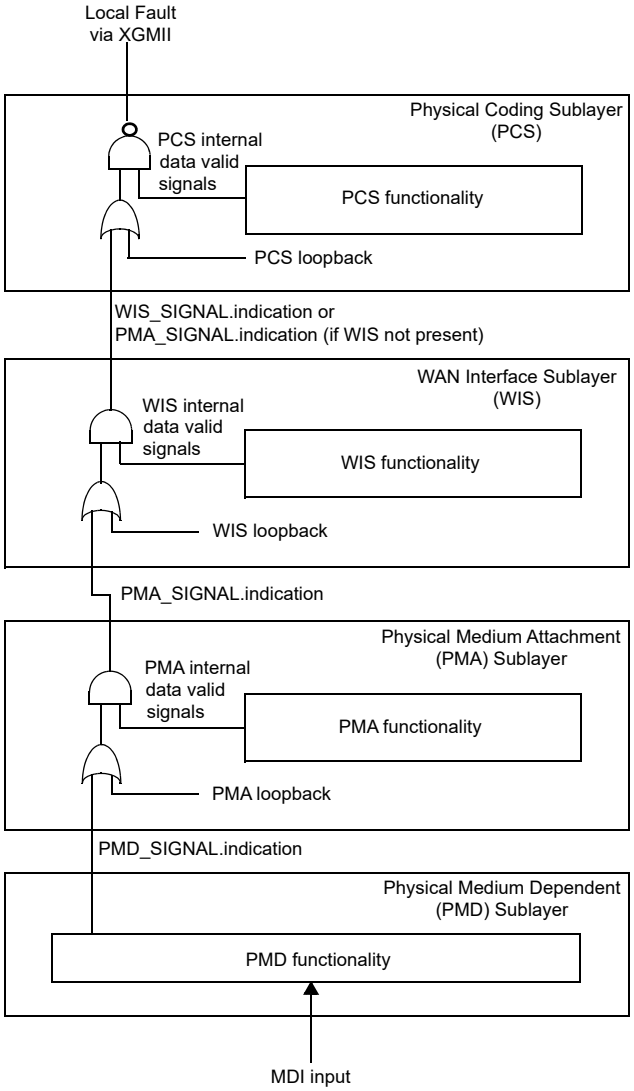

Figure 44A–7—Signal Detect handling across sublayers

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Annex 45A

(informative)

Clause 45 MDIO electrical interface

45A.1 MDIO driver

It is possible to implement the MDIO electrical driver using an open drain driver, as the MDIO signal is pulled up to 1.2 V using a resistor. This is shown in Figure 45A–1.

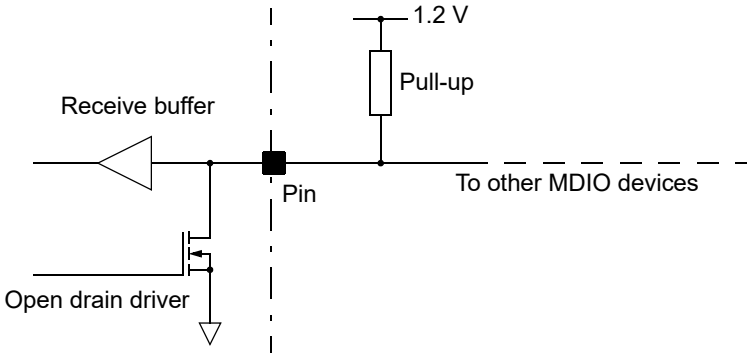

Figure 45A–1—Use of open drain driver for MDIO electrical interface

45A.2 Single Clause 45 electrical interface

As the Clause 45 MDIO electrical interface is significantly different from the Clause 22 MII Management electrical interface, it is not possible to directly attach a Clause 45 MMD to a Clause 22 MII Management Interface. Clause 45 MMDs that include Clause 22 registers may have their Clause 22 registers accessed via the Clause 45 electrical interface. This obviates the requirement to provide a Clause 22 compliant electrical interface in such systems. This is shown in Figure 45A–2.

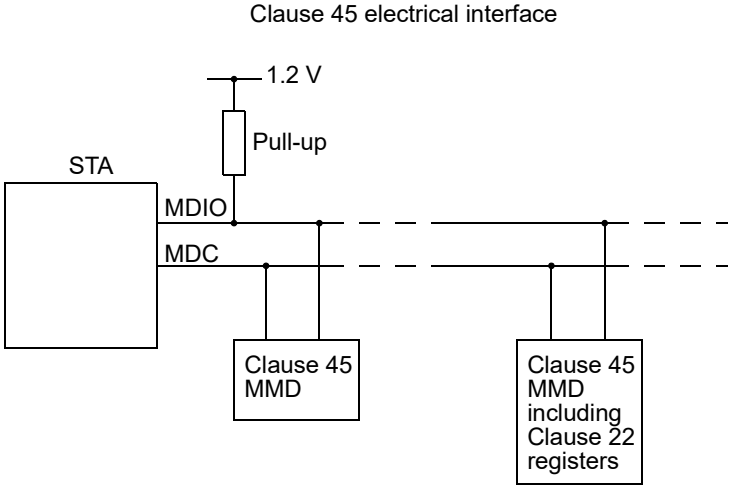

Figure 45A–2—Support of Clause 22 registers via the Clause 45 MDIO interface

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45A.3 Clause 45 electrical interface for STA with Clause 22 electrical interface to PHYs

If Clause 22 PHYs are to be attached to a Clause 45 MDIO interface, then a voltage translation device is required. One possible solution is a protocol aware voltage translation device. This arrangement is shown in Figure 45A–3. Such a translation device has to correctly drive both the Clause 45 MDIO interface and the Clause 22 MII Management interface using the voltages and timings specified in the appropriate clause. In order to drive the interfaces correctly, the device needs to have knowledge of the Clause 22 PHY addresses present on the Clause 22 Management interface. When any PHY attached to the Clause 22 MII Management interface is driving the MDIO, the translation device has to drive the Clause 45 MDIO interface with the same logical state that is being driven on to the Clause 22 Management interface by the PHY. Whenever the STA drives the Clause 45 MDIO interface, the translation device has to drive the Clause 22 Management interface with the same logical state that is being driven on to the Clause 45 MDIO interface. In addition, the translation device has to drive the Clause 45 MDC on to the Clause 22 Management interface. Even though the Clause 45 MDIO frames using the ST=00 frame code will also be driven on to the Clause 22 MII Management interface, the Clause 22 PHYs will ignore the frames.

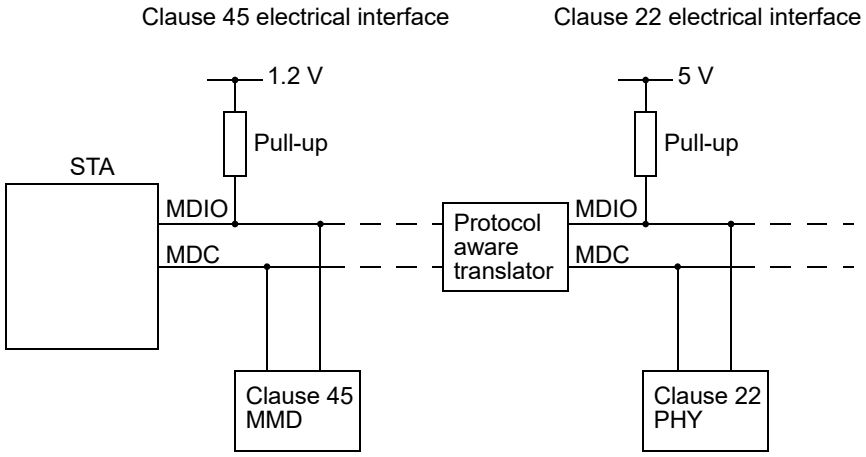

Figure 45A–3—Protocol aware voltage translator between Clause 45 and Clause 22

45A.4 Clause 22 electrical interface for STA with Clause 45 electrical interface to MMDs

If Clause 45 MMDs are to be attached to a Clause 22 MII management interface, then a voltage translation device is required. One possible solution is a protocol aware voltage translation device. This arrangement is shown in Figure 45A–4. Such a translation device has to correctly drive both the Clause 22 MII Management interface and the Clause 45 MDIO interface using the voltages and timings specified in the appropriate clause. In order to drive the interfaces correctly, the device needs to have knowledge of any Clause 22 PHY addresses present within MMDs attached to the Clause 45 MDIO Management interface. When any Clause 45 MMD, including embedded Clause 22 PHYs, attached to the Clause 45 MDIO Management interface is driving the MDIO, the translation device has to drive the Clause 22 MII Management interface with the same logical state that is being driven on to the Clause 45 MDIO interface by the PHY. Whenever the STA drives the Clause 22 MII Management interface, the translation device has to drive the Clause 45 MDIO interface with the same logical state that is being driven on to the Clause 22 MII Management interface. In addition, the translation device has to drive the Clause 22 MII Management interface MDC on to the Clause 45 MDIO interface. The Clause 22 MII Management interface has to be capable of generating the MDIO frame structure specified in Clause 45. Even though the Clause 45 MDIO

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frames using the ST=00 frame code will be driven on to the Clause 22 MII Management interface, the Clause 22 PHYs will ignore such frames.

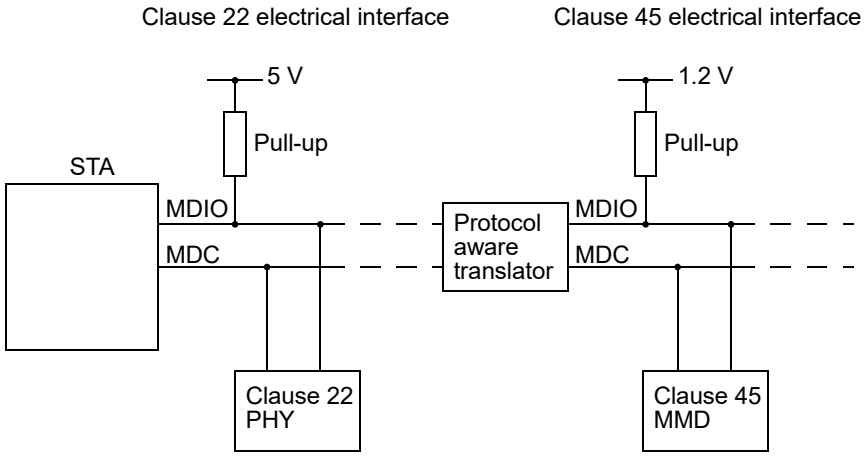

Figure 45A–4—Protocol aware voltage translator between Clause 22 and Clause 45

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Annex 48A

(normative)

Jitter test patterns

This annex defines test patterns that allow the 10GBASE-X PHY described in Clause 48 to test either its attached PMD described in Clause 53 or its XAUI interface described in Clause 47 for compliance in a system environment, or for unspecified diagnostic purposes. The patterns may be implemented at a bit, code-group or frame level and may be used for transmitter testing. The receiver may not have the capability to accept these diagnostic sequences; however, system debug can be improved if a receiver is able to test for one or more of these patterns and report bit errors (e.g., 8B/10B decoder errors) back to the user.

48A.1 High-frequency test pattern

The intent of this test pattern is to test random jitter (RJ) at a BER of 10^{-12}, and also to test the asymmetry of transition times. This pattern is not intended for jitter compliance testing. This high-frequency test pattern generates a one, or light on, for a duration of 1 unit interval (UI), followed by a zero, or light off, for a duration of 1 UI. This pattern repeats continuously on each lane for the duration of the test. For example, 10101010101010101010101010101010101010...

NOTE—This pattern can be generated by the repeated transmission of the D21.5 code-group on each lane. Disparity rules are followed.

48A.2 Low-frequency test pattern

The intent of this test pattern is to test low-frequency RJ and also to test PLL tracking error. This pattern is not intended for jitter compliance testing. This low-frequency test pattern generates a one, or light on, for a duration of 5 UI, followed by a zero, or light off, for a duration of 5 UI. This pattern repeats continuously on each lane for the duration of the test. For example, 11111000001111100000111110000011111100000...

NOTE—This pattern can be generated by the repeated transmission of the K28.7 code-group on each lane. Disparity rules are followed.

48A.3 Mixed-frequency test pattern

The intent of this test pattern is to test the combination of RJ and deterministic jitter (DJ) due to high-frequency ISI. This pattern is not intended for jitter compliance testing. This mixed-frequency test pattern generates a one, or light on, for a duration of 5 UI, followed by a zero, or light off, for a duration of 1 UI, followed by a one for 1 UI followed by a zero for 1 UI followed by a one for 2 UI followed by a zero for 5 UI followed by a one for 1 UI followed by a zero for 1 UI followed by a one for 1 UI followed by a zero for 2 UI. This pattern repeats continuously on each lane for the duration of the test. For example, 11111010110000010100111110101100000101000...

NOTE—This pattern can be generated by the repeated transmission of the K28.5 code-group on each lane. Disparity rules are followed.

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48A.4 Continuous random test pattern (CRPAT)

The continuous random test pattern is intended to provide broad spectral content and minimal peaking that can be used for the measurement of jitter at either a component or system level. This pattern is not intended for jitter compliance testing.

NOTE—The basis of this pattern may be found in NCITS TR-25:1999 [B42], “Fibre Channel - Methodologies for Jitter Specification”. This annex uses similar modifications to fit the RPAT test pattern into an IEEE 802.3 frame.

The continuous random test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within delimiters as specified in Clause 48 in the ordinary way. The contents of each packet is composed of the following octet sequences, as observed at the XGMII, before 8B/10B coding.

Each packet in the continuous random test pattern consists of 8 octets of PREAMBLE/SFD, followed by 1488 data octets (124 repetitions of the 12-octet modified RPAT sequence), plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE.

START/PREAMBLE/SFD:

FB 55 55 55 55 55 55 D5

MODIFIED RPAT SEQUENCE (REPEAT ENTIRE SEQUENCE 31 TIMES CONSECUTIVELY):

BE for 4 octets;

D7 for 4 octets;

23 for 4 octets;

47 for 4 octets;

6B for 4 octets;

8F for 4 octets;

B3 for 4 octets;

14 for 4 octets;

5E for 4 octets;

FB for 4 octets;

35 for 4 octets;

59 for 4 octets.

CRC

F8 79 05 59

IPG

FD 07 07 07 07 07 07 07 07 07 07 07

END

NOTE—The data values for this pattern are in hexadecimal.

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48A.5 Continuous jitter test pattern (CJPAT)

The continuous jitter test pattern is intended to expose a receiver's CDR to large instantaneous phase jumps. The pattern alternates repeating low-transition density patterns with repeating high-transition density patterns. The repeating code-group durations should be longer than the time constants in the receiver clock recovery circuit. This assures that the clock phase has followed the systematic pattern jitter and the data sampling circuitry is exposed to large systematic phase jumps. This stresses the timing margins in the received eye. The following pattern is intended for receive jitter compliance testing.

NOTE—The basis of this pattern may be found in NCITS TR-25:1999 [B42]. This annex uses similar modifications to fit the JTPAT test pattern into an IEEE 802.3 frame.

The continuous jitter test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within delimiters, as specified in Clause 48, in the ordinary way. The contents of each packet is composed of the following octet sequences, as observed at the XGMII, before 8B/10B coding.

Each packet in the continuous jitter test pattern consists of 8 octets of PREAMBLE/SFD, followed by 1504 data octets, plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE.

START/PREAMBLE/SFD:

FB 55 55 55 55 55 55 D5

MODIFIED JTPAT SEQUENCE

0B for 1 octet (lane 0);

7E for 3 octets (lanes 1, 2, 3);

7E for 524 octets—Low-density transition pattern;

F4 for 4 octets—Phase jump;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump;

AB for 4 octets—Phase jump;

B5 for 160 octets—High-density transition pattern;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump;

EB for 4 octets—Phase jump;

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F4 for 4 octets—Phase jump;

7E for 528 octets—Low-density transition pattern;

F4 for 4 octets—Phase jump;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump;

AB for 4 octets—Phase jump;

B5 for 160 octets—High-density transition pattern;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump;

EB for 4 octets—Phase jump;

F4 for 4 octets—Phase jump.

CRC

BD 9F 1E AB

IPG

FD 07 07 07 07 07 07 07 07 07 07 07

END

NOTE—The data values for this pattern are in hexadecimal.

48A.5.1 Continuous jitter test pattern (CJPAT) 10 bit values

The following tables depict a 10-bit encoding for CJPAT. This is the encoding which will occur when each lane has negative disparity before the Start column. The actual 10-bit encoding sent when CJPAT is transmitted will be one of 16 encodings depending upon the disparity of each lane at the beginning of the packet. CJPAT has been designed to produce the same disparity on each lane after the Terminate column as that lane had before the Start column. When CJPAT is sent continuously, two of the sixteen possible encodings will occur because Idle will either leave the disparity the same or flip the disparity on all lanes.

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Table 48A–1—Start/Preamble/SFD/First 8 Data Octets

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
FB	1101101000	55	1010100101	55	1010100101	55	1010100101
55	1010100101	55	1010100101	55	1010100101	D5	1010100110
0B	1101001011	7E	0111100011	7E	0111100011	7E	0111100011
7E	1000011100	7E	1000011100	7E	1000011100	7E	1000011100

Table 48A–2—Low-density transition pattern (repeat 65 times)

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
7E	0111100011	7E	0111100011	7E	0111100011	7E	0111100011
7E	1000011100	7E	1000011100	7E	1000011100	7E	1000011100

Table 48A–3—Phase jump

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
F4	0010110111	F4	0010110111	F4	0010110111	F4	0010110111
EB	1101001000	EB	1101001000	EB	1101001000	EB	1101001000
F4	0010110111	F4	0010110111	F4	0010110111	F4	0010110111
EB	1101001000	EB	1101001000	EB	1101001000	EB	1101001000
F4	0010110111	F4	0010110111	F4	0010110111	F4	0010110111
EB	1101001000	EB	1101001000	EB	1101001000	EB	1101001000
F4	0010110111	F4	0010110111	F4	0010110111	F4	0010110111
AB	1101001010	AB	1101001010	AB	1101001010	AB	1101001010

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Table 48A–4—High-density transition pattern (repeat 20 times)

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
B5	1010101010	B5	1010101010	B5	1010101010	B5	1010101010
B5	1010101010	B5	1010101010	B5	1010101010	B5	1010101010

Table 48A–5—Phase jump (repeat 4 times)

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
EB	1101001000	EB	1101001000	EB	1101001000	EB	1101001000
F4	0010110111	F4	0010110111	F4	0010110111	F4	0010110111

Table 48A–6—Low-density transition pattern (repeat 66 times)

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
7E	1000011100	7E	1000011100	7E	1000011100	7E	1000011100
7E	0111100011	7E	0111100011	7E	0111100011	7E	0111100011

Table 48A–7—Phase jump

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
F4	0010110001	F4	0010110001	F4	0010110001	F4	0010110001
EB	1101001110	EB	1101001110	EB	1101001110	EB	1101001110
F4	0010110001	F4	0010110001	F4	0010110001	F4	0010110001
EB	1101001110	EB	1101001110	EB	1101001110	EB	1101001110
F4	0010110001	F4	0010110001	F4	0010110001	F4	0010110001
EB	1101001110	EB	1101001110	EB	1101001110	EB	1101001110
F4	0010110001	F4	0010110001	F4	0010110001	F4	0010110001
AB	1101001010	AB	1101001010	AB	1101001010	AB	1101001010

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Table 48A–8—High-density transition pattern (repeat 20 times)

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
B5	1010101010	B5	1010101010	B5	1010101010	B5	1010101010
B5	1010101010	B5	1010101010	B5	1010101010	B5	1010101010

Table 48A–9—Phase jump (repeat 4 times)

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
EB	1101001110	EB	1101001110	EB	1101001110	EB	1101001110
F4	0010110001	F4	0010110001	F4	0010110001	F4	0010110001

Table 48A–10—CRC/Terminate/IPG

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
BD	1011101010	9F	1010110010	1E	0111100100	AB	1101001010
FD	0100010111	07	0011111010	07	0011111010	07	0011111010
07	1100001100	07	1100001100	07	1100001100	07	1100001100
07	0011110100	07	0011110100	07	0011110100	07	0011110100

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Annex 48B

(informative)

Jitter test methods

This annex specifies the definitions and measurement requirements for the jitter specification of the XGXS and XAUI described in Clause 47, the 10GBASE-LX4 PMD described in Clause 53 and the 10GBASE-CX4 PMD described in Clause 54. These measurement methods and specifications are intended to be used for jitter and wander compliance testing, but are not definitive.

While jitter specifications are required to be met for all lanes during operation, the methods described in this annex are written for testing of a single lane. Each lane can be tested with these methods individually or concurrently.

48B.1 BER and jitter model

Measurement of BER within a data eye is not only the fundamental indicator of signal quality, it is a valuable tool to infer jitter properties. Insight into the relationship between jitter, eye opening and error ratio can be gained through mathematical modeling.

48B.1.1 Description of dual Dirac mathematical model

Figure 48B–1 considers a typical eye diagram that may be seen on an oscilloscope. For the purpose of discussion, assume that an ideal trigger source is used so that the eye is accurately depicted. Jitter is indicated by distributed transitions (crossings) of the threshold as the data toggles between logic states. Histograms of transition regions can be taken at the threshold level. The width of the histograms can then be estimated, including standard deviation, etc.

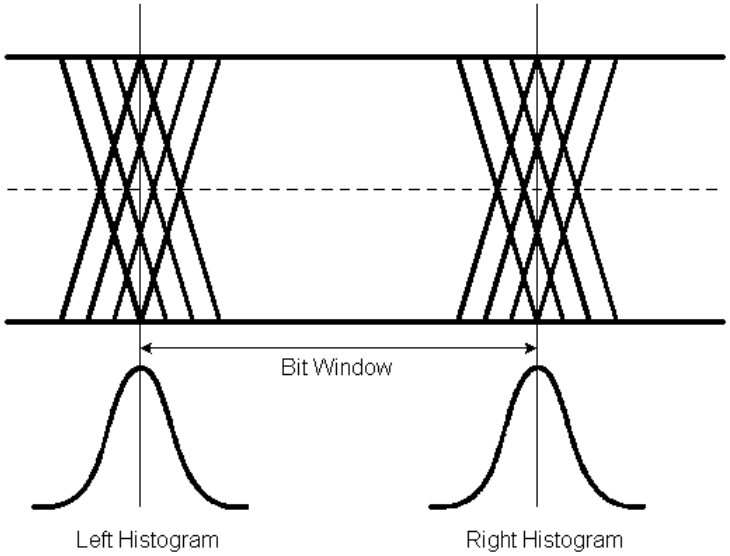

Figure 48B–1—Eye Diagram sketch

The histograms represent probability density functions (PDFs) of the jitter and statistically describe the locations in time of the transitions. The PDFs are placed with their means at the ideal transition times of the

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logic states. To simplify matters, the time scale is given in terms of unit intervals (UI) with 0.5 located at the exact center of the eye. The means of the two PDFs are at 0 and +1 UI.

Ideally, the receiver samples the eye at the center where the tails of the transition histograms are small, as shown in Figure 48B–2. To calculate the probability of either transition causing an error due to jitter, the area under its PDF tail on the errored side of the sample point (time) has to be calculated. This is the complementary cumulative distribution function, or CDF. For the left hand PDF, the tail is integrated from to the sample point to $+\infty$; the right hand PDF's tail is integrated from $-\infty$ to the sample point. The overall probability of transition error is the sum of the two CDFs. It is assumed that the tails of the neighboring bits do not contribute to the probability of error.

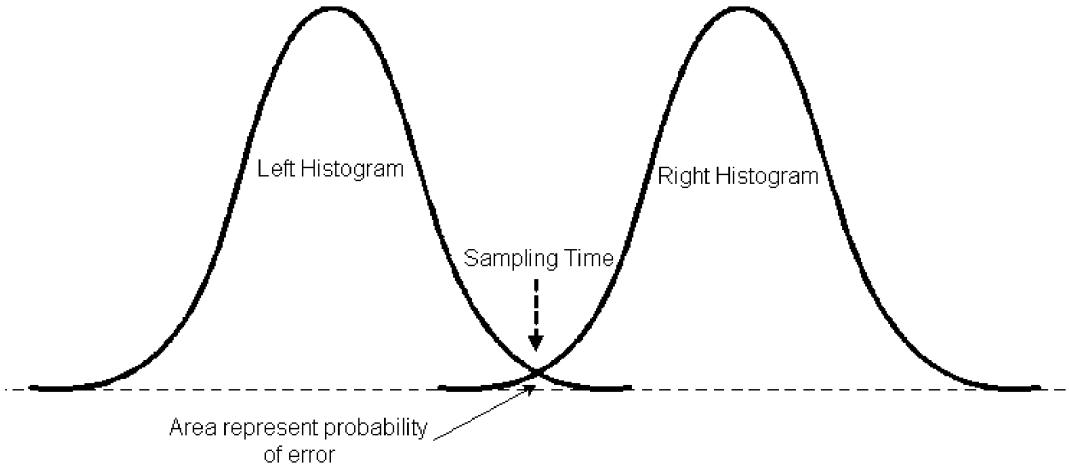

Figure 48B–2—Eye sampling and probability of error

To determine the BER, the probability of a transition-caused error is multiplied by the probability of a transition occurring. Nominally, the latter may be seen as the average transition density. This model assumes typical data streams have a transition density of 50%.

To demonstrate these concepts, define a general jitter PDF, $JT(\tau, W, \sigma)$, centered at 0, where τ is time, W is the peak-to-peak value of deterministic jitter, and σ is the rms value of random jitter. The left PDF histogram (centered at 0) causes bit errors as:

$$BER_{left}(\tau_{sample}, W, \sigma) = \Gamma_{transistion} \cdot \int_{\infty}^{\tau_{sample}} JT(\tau, W, \sigma)\delta\tau \tag{48B-1}$$

where τ_{sample} is the sampling instant in time, and $\Gamma_{transistion}$ is the transition density. Similarly, the right PDF histogram (shifted and centered at 1 UI) causes bit errors as

$$BER_{right}(\tau_{sample}, W, \sigma) = \Gamma_{transistion} \cdot \int_{-\infty}^{\tau_{sample}} JT(\tau - UI, W, \sigma)\delta\tau \tag{48B-2}$$

The sum of these two functions provides the total (BER) due to jitter,

$$BER_{total}(\tau_{sample}, W, \sigma) = BER_{left}(\tau_{sample}, W, \sigma) + BER_{right}(\tau_{sample}, W, \sigma) \tag{48B-3}$$

In the BERT scan, BER is measured as the sample point, τ_{sample}, is swept between the two eye crossings. The probability of error as a function of the sample point is commonly known as a BER bathtub curve.

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48B.1.2 Random Jitter

For random or Gaussian jitter (RJ) only the standard deviation, σ, is necessary to define the PDF

$$RT(\tau, \sigma) = \frac{1}{\sqrt{2\pi}} \cdot \frac{1}{\sigma} \cdot e^{-\left(\frac{\tau^2}{2\sigma^2}\right)} \tag{48B-4}$$

The CDF for this Gaussian PDF function is the complementary error function (erfc).

48B.1.3 Addition of Deterministic Jitter

Total jitter is composed of both random and deterministic components. The DJ component can be defined, as for RJ, by a PDF, where the combined total jitter PDF is a convolution of the DJ and RJ PDFs.

Simple peak-to-peak is insufficient as the measurement of DJ. An overall weighting function that captures not only the peak-to-peak but also the shape of the density function is required. This may be known as "effective DJ." For purposes of simplicity, effective DJ in this annex is based on the dual Dirac function, where it is assumed that the DJ PDF is comprised only of a pair of delta functions. Other PDFs are certainly possible, however, in the prediction of low BERs, this simplification is sufficient. All references to DJ in Clauses 47 and 53 should be understood as effective DJ.

An example of effective DJ is duty cycle distortion (DCD), which when convolved with RJ results in two Gaussian functions, one centered at each of the two delta functions.

The magnitude of the DJ, is given as peak-to-peak amplitude, *W*. Therefore, each delta function is offset from the mean crossing position by the peak value of DJ, *W*/2. The PDF for deterministic jitter, centered at 0, is therefore defined as:

$$JT(\tau, W, \sigma) = \frac{\delta\left(\tau, -\frac{W}{2}\right)}{2} + \frac{\delta\left(\tau, \frac{W}{2}\right)}{2} \tag{48B-5}$$

When convolved with random jitter, the PDF, centered at 0, becomes:

$$JT(\tau, W, \sigma) = \frac{1}{2\sqrt{2\pi}} \cdot \frac{1}{\sigma} \cdot \left(e^{-\left(\frac{\left(\tau - \frac{W}{2}\right)^2}{2\sigma^2}\right)} + e^{-\left(\frac{\left(\tau + \frac{W}{2}\right)^2}{2\sigma^2}\right)} \right) \tag{48B-6}$$

48B.1.4 Effects of jitter high-pass filtering and CJPAT on deterministic jitter

It is understood that CDRs track low-frequency jitter, and that including this effect in the specifications could ease requirements on clock oscillators (lower cost designs tend to exhibit low-frequency RJ), serializer (SERDES, same advantage) designs and switching power supplies, layouts, bypassing, etc. All jitter specifications include the effects of a high-pass filter (to suppress the significance of low-frequency jitter) to emulate CDR tracking.

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It is also realized that, due to frequency content, long complex patterns cause phenomena that are not observed with short patterns—data dependent jitter (DDJ, a form of DJ) can have extreme ranges of frequency content from well below to well above the CDR corner frequencies. Effects are usually seen in both transmitters and receivers. Jitter test patterns are specified in Annex 48A.

48B.2 Jitter tolerance test methodologies

An important measurement in determining link integrity is the characterization of a receiver's (i.e., CDR's) ability to tolerate jittered inputs yet recover error-free data. This is accomplished by inputting a well-controlled, jittered signal to a CDR while measuring the BER at the output of the CDR. As the source signal is modified in amplitude and spectral content, the change in BER is measured. This subclause describes some useful test methodologies for testing a receiver's jitter tolerance.

48B.2.1 Calibration of a signal source using the BERT scan technique

The jitter model described in 48B.1 can be used to calibrate the signal source for tolerance measurements as well as to provide a method for extrapolating lower BER. In this approach, curve fitting of the dual Dirac model onto bathtub curves derived from BERT Scans give the jitter content.

Figure 48B–3 shows an example of how to generate controlled amounts of jitter in a signal to be used for tolerance measurement.[276] Three sources of jitter are provided: Deterministic (DDJ and sinusoidal (SJ)) and Gaussian (RJ). Each of these is added to the serial signal generated by a BERT Pattern Generator. A sinewave generator modulates the clock to the Pattern Generator to provide Sinusoidal jitter modulation from 10 Hz to 20 MHz. A filter or cable adds deterministic jitter. A white noise source[277] with a bandwidth greater than 500 MHz[278] is added to the signal to provide random jitter.

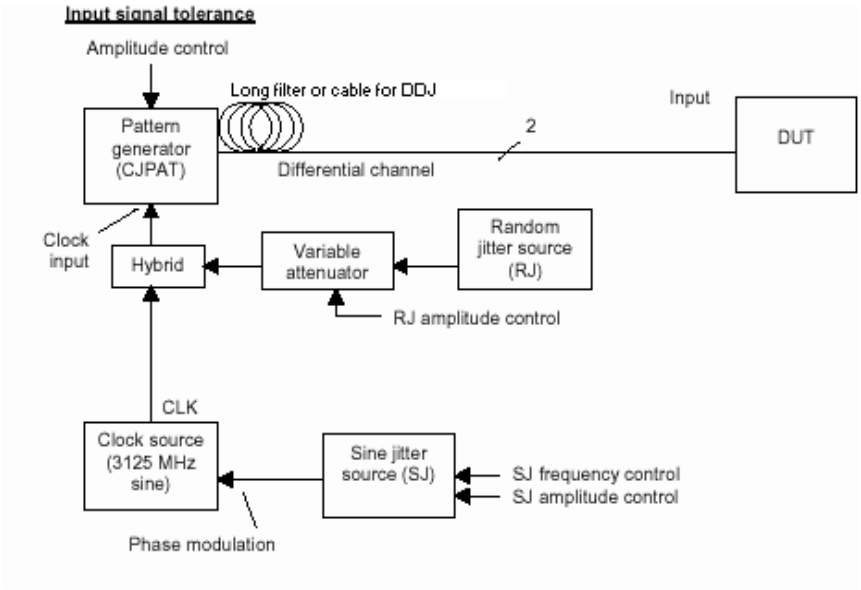

Figure 48B–3—BERT Jitter Tolerance Source

[276]Beware of instrument noise floors and data dependencies, as these may lead to test signals with less stress than intended.

[277]RJ has to be Gaussian and not clipped out to >BER being tested (spec is 1E-12). Simply measuring the rms value does not guarantee that the tails exist and that the Rx will be sufficiently stressed as specified.

[278]The spectrum of the portion of RJ that is calibrated has to be from greater than 20MHz. The sketch as shown assumes the pattern generator passes clock input jitter through to the data with >>20 MHz BW. This may not be the case. The RJ spectrum need not be white above 20 MHz, but a wider spectrum is preferred.

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Amplitude calibration is not possible on a scope due to the low probability of the peak-to-peak RJ effects. For better visibility for amplitude calibration, the RJ portion may be temporarily replaced with an equivalent amount of peak-to-peak SJ to bring TJ up to the same specified output jitter level, allowing the desired amplitude value to be met.[279,280]

If the clock data recovery circuit of the system under test has a corner frequency above the maximum sine wave generator frequency, be sure to increase the amount of the applied deterministic jitter by the amount of the specified high-frequency value sinusoidal jitter.

When calibrating the jitter tolerance test setup, the effects of high pass filtering in the time/jitter domain need to be understood and included per the specifications. Per 48B.1.4, high pass filtering can have profound effects on pattern dependent jitter (it will increase measured DJ with patterns such as CJPAT) and also track out jitter below the specified corner frequency. [281]

After complete, calibration has to be verified using the methods described in 48B.3 and iterated as needed until the required specifications are met.

It should be noted that the XAUI is a differential input and calibration of the test signal is performed using the differential signal. If test equipment only provides single-ended possibilities, care should be taken to calibrate and test with a balun to convert differential signals to single-ended signals. Single-ended signals should not be directly used, due to the possibility of asymmetric characteristics.

48B.3 Jitter output test methodologies

Three viable methodologies for measuring jitter output are described in this subclause. They are as follows:

a) Time domain measurement using an oscilloscope to characterize the data eye.
b) Time domain measurement using BERT scan by moving of the data sampling point within the data eye.
c) Time interval analysis based on accurate measurement of the time interval between threshold crossings of the transmitter waveform;

48B.3.1 Time domain measurement—Scope and BERT scan

It is easy to grasp that if the eye is larger than the eye mask, it has to be ok. This is not necessarily true. Given the probabilistic nature of random jitter, it is necessary either to test for an extended amount of time to reach a high confidence level for achieving 1×10^{-12} BER or to perform some kind of statistical extrapolation.

48B.3.1.1 Jitter high pass filtering (using Golden PLL)

Due to the issues mentioned in 48B.1.4, when testing either at the component level or the system level, the test clock should be derived from the data with a given high-pass filter function of the jitter using, for example, a golden PLL.

[279]Amplitude calibration should be done before addition of SJ, as SJ is designed to add margin into the design. This footnote is not referring to the suggestion of temporarily substituting SJ and RJ during amplitude calibration, but to the SJ that is required as part of the specifications.
[280]It may be required to add amplification to achieve the required test signal amplitude.
[281]Beware of autocorrelation effects.

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Given a typical test setup, the serial bit pattern is transmitted to the input of a BERT and a golden PLL. The golden PLL extracts a reference clock to trigger the sampling scope or clock the BERT.

48B.3.1.2 Time domain scope measurement

Time domain measurement uses the high-speed sampling scopes to view the jitter output data eye. Most high-speed sampling scopes today provide features to collect and present data on the output jitter. Some oscilloscopes provide a feature to compare the measured data to an "eye mask." An eye mask is a specification for allowed eye opening. The advantage of an eye mask is that it tests for amplitude as well as timing compliance. The general physical media transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram at any of the compliance measurement points. These characteristics include rise time, fall time, pulse overshoot, pulse undershoot, and ringing, all of which prevent excessive degradation of the receiver sensitivity. For the purpose of an assessment of the transmit signal, it is important to not only consider the eye opening, but also the overshoot and undershoot limitations. The parameters specifying the mask of the transmitter diagram (eye mask) can be found in the clause of the applicable Physical Layer specification whether it be copper or fiber physical media. The eye mask, through its use of a specified time range in which the transmit signal can change state from the logic low to logic high levels, is also specifying a measure of the allowed jitter.

It is strongly advised not to use the eye mask to verify that total jitter is within specification because of the nature of the test. The eye mask test is generally a short test, and thus the eye diagram is not captured for a sufficient time to capture the full extent of the random jitter's peak-to-peak value. It is necessary to capture the eye pattern for a sufficient period to insure the full extent of the deterministic jitter is captured by the test instrument. Since the peak-to-peak of the random jitter for a BER of 1×10^{-12} is 14 times the sigma, it is not possible to capture the full extent of random jitter's peak-to-peak value due to the low sampling rate.

48B.3.1.3 BERT scan

As implied by the jitter model in 48B.1, a BERT scan approach can provide random and deterministic jitter components and provides a mechanism to extrapolate to lower BER (less than 1×10^{-12}) without impossibly long test times due to the inherent high sampling rate.

48B.3.1.3.1 Approximate curve-fitting for BERT scan

48B.3.1.3 describes a technique for using a BERT scan to determine eye opening and jitter. For highest accuracy, the bathtub curve should be measured over a high number points at low BER and curve-fitted with a least-squares method to estimate equivalent DJ, RJ, and TJ values. However, a simple and fast method for estimating these values may be applied using only two measurement points.

The following steps describe a process for estimating equivalent RJ, DJ, and TJ values from a two point BERT scan measurement:

a) Measure the eye opening at 2 different BER, BER_0 @τ_0 and BER_1 @τ_1 (e.g., 10^{-9} and 10^{-5}).

b) For each BER_n, determine the associated Q_n from the inverse normal cumulative probability distribution, adjusted for transition density, e.g., $Q = 3.94$ for BER = 10^{-5}, and $Q = 5.77$ for BER = 10^{-9}, where transition density is assumed to be 0.5.

c) Calculate the individual jitter components using the equations for Random Jitter and Deterministic Jitter, and then calculate the total jitter for the given BER = 10^{-12}, using the following three equations:

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Random Jitter—

$$RJ_{RMS} = 0.5\left|\frac{t_1 - t_0}{Q_1 - Q_0}\right| \quad (48B\text{-}7)$$

Deterministic Jitter—

$$DJ = UI - t_0 - (2Q_0 RJ_{RMS}) \quad (48B\text{-}8)$$

Total Jitter—

$$TJ = DJ + 13.8 \cdot RJ_{RMS} \quad (48B\text{-}9)$$

The minimum value for measured BER is constrained by test time (10 errors are suggested as an absolute minimum to get reasonable statistical confidence); the maximum value is constrained by potential departure of actual results from the assumed curve fit shape (BER = 10^{-5} should be the maximum value used).

48B.3.2 Time Interval Analysis

Time Interval Analysis (TIA) uses many accurate, single-shot, edge-to-edge time measurements. The statistics of these measurements can be used to perform jitter calculations. True random jitter (RJ) and true deterministic jitter (DJ) can be measured using this technique on repeated patterns as well as random data streams. From the true RJ and DJ measurements, an error probability density function, or bathtub curve can be generated. Using the bathtub curve, effective DJ and effective RJ can be calculated. There are two measurement methods defined for executing this test:

a) TIA with Golden PLL
b) TIA armed on pattern trigger

Each method uses the basic TIA methodology, but with different schemes for acquiring the data. In the first method, the TIA is used with a Golden PLL, as described in 48B.3.1.1, and time measurements are made from the recovered reference clock to the data transitions. The low-frequency content that would be tracked by the receiver is presented on the reference clock, and thus eliminated from the jitter data before being presented to the TIA. The second method is used to acquire data when a Golden PLL is not available, or, when jitter on just the data is desired. This method requires a pattern trigger to synchronize the jitter measurements relative to a specific location in the pattern. The TIA can extract the pattern trigger from the data based on a unique bit sequence or pattern length.

48B.3.2.1 TIA with Golden PLL

In this option, a Golden PLL is required to provide a reference clock derived from the data stream to trigger the TIA. This scheme effectively removes low-frequency content from the measured data in a manner similar to that done in a receiver. The configuration used for this option is shown in Figure 48B–4 (note that only a single channel is shown). The Golden PLL in Figure 48B–4 is shown with a differential input; other approaches are possible, but it is important that the balance of the data signals is not disturbed and that both phases are included in clock recovery. A Golden PLL is used for each data signal so as to ensure proper CDR modeling on each data signal. Each Golden PLL is intended to track low-frequency jitter content occurring on the data signal applied to the input stage of that PLL. It cannot be assumed that the clock extracted from one data signal can be used for the other signals since the low-frequency jitter content may be different. Some TIA models have this algorithm integrated internally in the instrument, and some TIA models have integrated Golden PLL or high-pass filtering algorithms.

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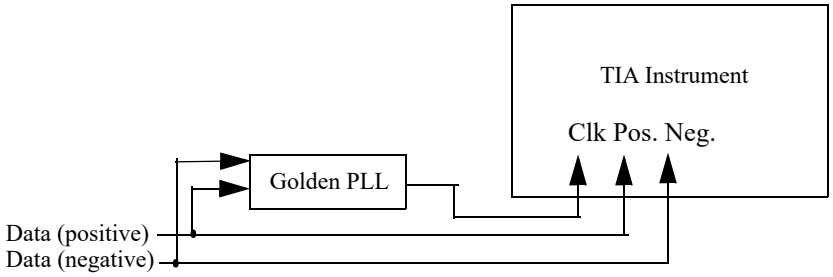

Figure 48B–4—TIA with Golden PLL configured for jitter measurement

48B.3.2.1.1 Test method

The TIA is capable of measuring the time from the data transitions to the reference clock as extracted with the Golden PLL. This results in a clock to data histogram that describes the jitter occurring on the data transitions relative to the reference clock (as is the case with a bit clock triggered BERT measurement). RJ can be estimated by fitting a Gaussian curve to the tail region of the histogram. DJ can be estimated by measuring the separation of the means of the fitted Gaussian curves. Some sampling TIA instruments have built in algorithms specifically designed for this process, and can automatically estimate RJ, DJ, and TJ in this configuration. Figure 48B–5 shows a typical clock to data histogram for a communication signal. Note the highlighted curves that represent the fitted Gaussian curves. Also note that the rising edges are treated separately from the falling edges so as to accurately group the jitter contributors. This is critical in cases where the cross point of the data signal is not at the measured voltage. In Figure 48B–5, the rising edge histogram is shifted to the right of the falling edge histogram, indicating that the cross point was below the test voltage. The outer most histogram on a given side is used for the RJ and DJ calculations for that side of the histogram. Each side is treated independently.

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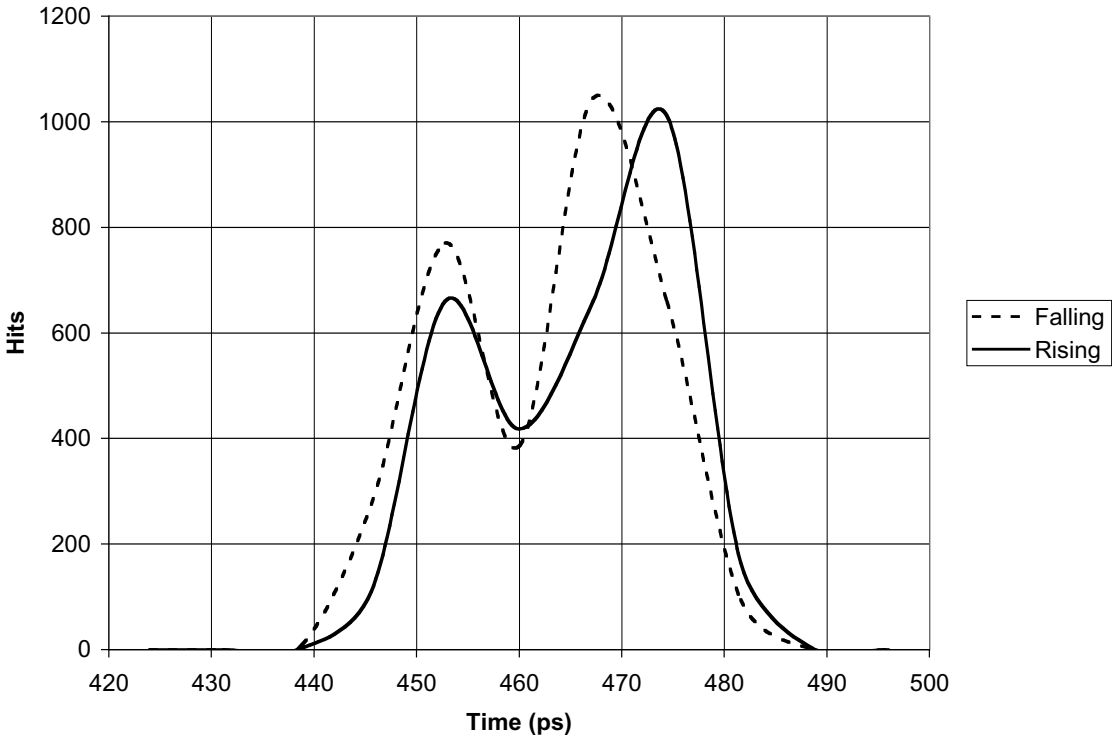

Figure 48B–5—Typical clock to data histogram with fitted Gaussian curves

Jitter values such as DJ, RJ, and TJ can also be displayed on the plot corresponding to 1E-12 BER as shown in Figure 48B–5. Effective Jitter is calculated from the bathtub curve using the same calculations used by the BERT scan method described in 48B.3.1.3.1. To quantify the quality of the measurement, a goodness of fit calculation can be made which compares the quality of the fit of the Gaussian to the actual histogram. Acceptable goodness-of-fit values (χ) for probability confidence level (approximately 1E-4) should be in the range of $0.8 < \chi < 1.2$. The measured DJ and TJ values using this method can be compared against the maximum jitter as specified.

48B.3.2.2 TIA with pattern trigger

The basic setup for this option is shown in Figure 48B–6 (note that only one channel is shown). The pattern trigger can be generated internally to the TIA based on the identification of a unique bit sequence within the data stream or pattern length of the repeated pattern. No measurements are made from the pattern trigger. All measurements are made within the data signal thereby eliminating any error attributed to the bit clock. The high-pass filter characteristic of the Golden PLL is applied using a DSP algorithm thereby eliminating the need for external hardware. Some TIA instruments have this algorithm fully integrated.

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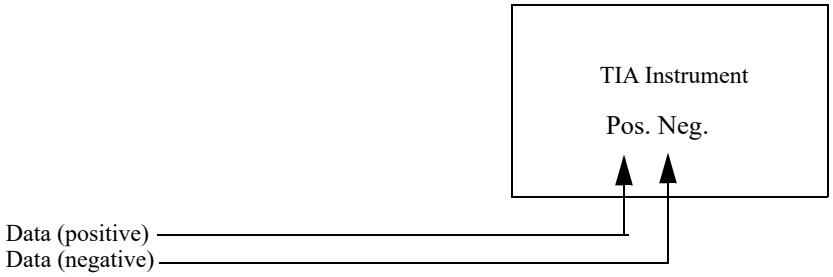

Figure 48B–6—TIA with pattern trigger configured for jitter measurement

48B.3.2.2.1 Test method

All time measurement are made from the same reference edge within the data pattern. This edge is identified by the pattern trigger. Thousands of measurements are made of each transition within the data pattern relative to the reference edge. Histograms for each transition are captured from this data. An FFT of the autocorrelation algorithm of the variance information from these histograms is used to extract SJ. Using the tail fit algorithm described in 48B.3.2.1.1, RJ is measured from each of these histograms and the results plotted in the FFT display. The RJ, bounded by the high-pass filter function is calculated from the FFT of the autocorrelation function. Data dependent jitter is measured from the histograms of each transition based on the displacement of each histogram mean relative to integer multiples of the measured bit period. TJ is calculated and the bathtub curve generated based on the convolution of the RJ PDF, DDJ PDF, and the SJ PDF. This method directly measures the DJ PDF and thereby does not need to assume that the DJ PDF is a dual Dirac function. Effective DJ and Effective RJ is calculated from the bathtub curve using the same formulas used for the BERT scan method, thereby ensuring correlation. Some TIA instruments have this algorithm fully integrated, simplifying the measurement methodology.

48B.3.2.3 Approximate curve fitting for TIA bathtub curve

Since the TIA is capable of measuring true DJ and its probability density function (PDF), the TIA can accurately display total jitter (TJ) as a function of BER in the form of an error probability density function, or bathtub curve. From the Error PDF, the effective DJ can be estimated using the same curve fit technique described in 48B.3.1.3.1.

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Annex 50A

(informative)

Thresholds for Severely Errored Second calculations

This annex provides tables of threshold values that may be used to determine the generation of Section, Line and Path Severely Errored Second (SES) events for various error ratios. An SES event is deemed to have occurred when the number of bit errors, detected via the corresponding Bit Interleaved Parity (BIP) check, exceeds some predefined threshold value when accumulated over a 1 s interval; reporting of an SES event indicates that the actual bit error ratio on the medium has increased to a point where Station Management has to be notified. These threshold values are referred to as *x* in the Layer Management definitions in Clause 30. This annex also defines the terms “Path Block Error” and “Far End Path Block Error.”

The values in these tables are derived according to the algorithms given in Annex C of ANSI T1.231-1997.

50A.1 Section SES threshold

The Section SES threshold is referenced as *x* in 30.8.1.1.3.

Table 50A–1 gives the values to be used for the Section SES threshold in order to report Section SES events at various limiting bit error ratios. A BER of 10^{-6} corresponds to the default Section SES threshold of 8554 in 30.8.1.1.3.

Table 50A–1—Section SES

BER	Threshold, *x*
10^{-6}	8554
10^{-7}	980
10^{-8}	99
10^{-9}	10
10^{-10}	1

50A.2 Line SES threshold

The Line SES threshold is referenced as *x* in 30.8.1.1.11.

Table 50A–2 gives the values to be used for the Line SES threshold in order to report Line SES events at various limiting bit error ratios. A BER of 10^{-6} corresponds to the default Line SES threshold of 9835 in 30.8.1.1.11.

50A.3 Path SES threshold

The Path SES threshold is referenced as *x* in 30.8.1.1.19.

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Table 50A–2—Line SES

BER	Threshold, *x*
10^{-6}	9835
10^{-7}	984
10^{-8}	98
10^{-9}	10
10^{-10}	1

Table 50A–3 gives the values to be used for the Path SES threshold in order to report Path SES events at various limiting bit error ratios. The default Path SES threshold of 2400 in 30.8.1.1.19 corresponds to a situation where 30% of all the SPEs being received have parity errors detected via the Path BIP checks.

Table 50A–3—Path SES

Fraction of SPEs with parity errors	Threshold, *x*
30%	2400
25%	2000
20%	1600
15%	1200
10%	800

50A.4 Definition of Path Block Error

A Path Block Error (see Section 8.1.1.1.2 of ANSI T1.231-1997) is declared when one or more of the 8 BIP-8 parity bits that are computed over the received Synchronous Payload Envelope, and compared to the B3 octet of the Path Overhead, are found to be in error. At most one Path Block Error can be declared per WIS frame (i.e., a maximum rate of 8000 counts per second), regardless of the actual number of parity errors detected using a particular B3 octet.

50A.5 Definition of Far End Path Block Error

A Far End Path Block Error is declared when the G1 octet extracted from a received WIS frame indicates that the far end WIS has detected one or more BIP-8 parity errors in the SPE of a previously transmitted WIS frame. The far end WIS reports these parity errors via the REI-P field of the G1 octet. At most one Far End Path Block Error can be declared per received WIS frame (i.e., a maximum rate of 8000 counts per second), regardless of the actual number of parity errors reported in the REI-P field of a particular G1 octet.

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Annex 55A

(normative)

LDPC details

55A.1 Generator matrix

The generator matrix, G, uniquely specifies the mapping of information bits to codewords. G.txt contains a representation of G. G.txt contains 1723 rows, one for each row of G. Each row has numbers ranging from 0 to 2047 separated by spaces. Each number represents the column index of the "1" entries in the specific row. All other entries of G are "0" and are not referenced in G.txt. G.txt is available online in the file matrices.zip.[282]

55A.2 Sparse parity check matrix H

Codewords that are generated using G are in the null space of a sparse parity check matrix H. The H matrix is available in machine readable format in file H.txt. This H matrix was obtained by permuting the columns of another sparse matrix using the permutations specified in col_swap.txt. The file row_swap.txt describes row permutations of H that can put it in pseudo-lower triangular form.[282]

For further information on LDPC codes, see Gallagher [B26].

[282]The files are available at: https://standards.ieee.org/downloads/802.3/.

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Annex 55B

(informative)

Additional cabling design guidelines for 10GBASE-T

This annex provides additional cabling guidelines for 10GBASE-T deployment on balanced copper cabling systems as specified in 55.7. These guidelines are intended to supplement those in Clause 55.

55B.1 Alien crosstalk considerations

The noise coupled between the adjacent link segments illustrated in Figure 55B–3 and Figure 55B–4 is referred to as alien crosstalk (Figure 55B–1).

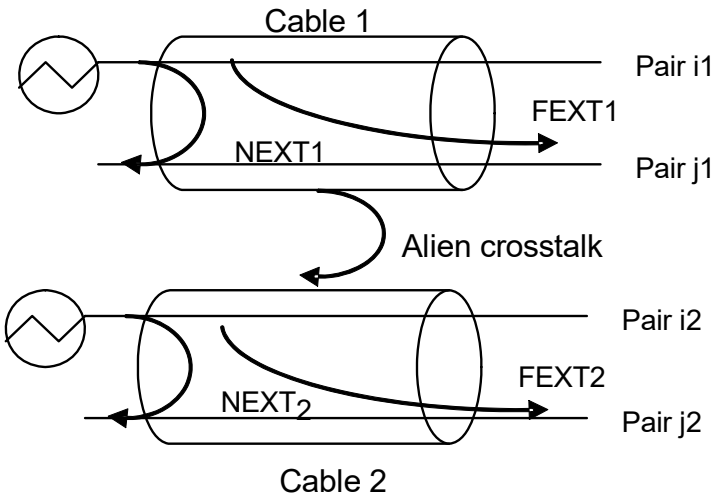

Figure 55B–1—Alien crosstalk coupling between link segments

The alien crosstalk noise levels are dependent on the number and proximity of adjacent cables and connectors. The alien crosstalk link segment specifications of PS ANEXT and PS AELFEXT given in 55.7 are based on the alien crosstalk measurements between cabling channels configured in a six-around-one orientation where the disturbed cable is the central cable and adjacent to all of the other disturbing cables. The alien crosstalk coupling between a cable and six adjacent cables tightly bound in a six-around-one configuration exhibits a “worst case”.

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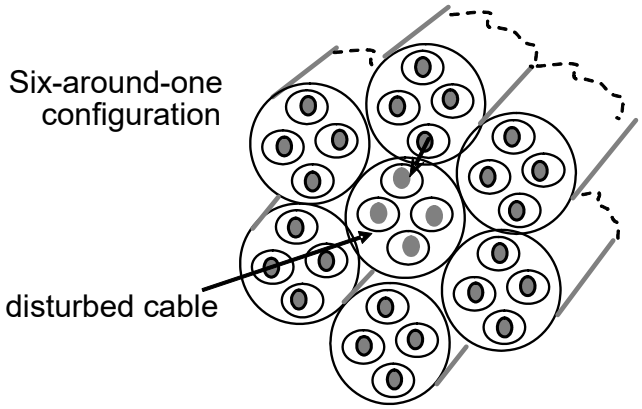


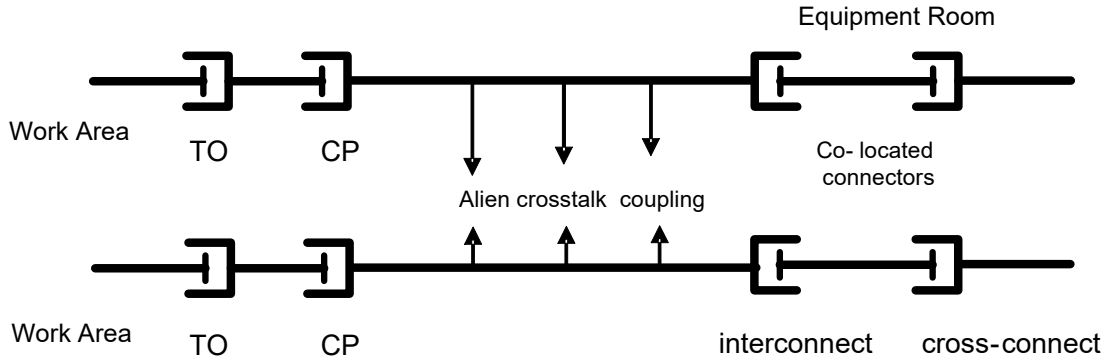
Figure 55B–2—Six-around-one cable configuration

The alien crosstalk coupling is a function of the distance between the cabling components. Removing or loosening cable bindings, separating equipment and patch cordage, and utilizing non-adjacent connectors all have a significant impact on reducing the levels of alien crosstalk noise.

In many topologies, the cables are only bundled together for relatively short distances and laid in cable trays. The star wiring topology, where the cables are distributed radially from a centralized telecommunication closet to each work area, reduces the distances over which link segments are in close proximity.

55B.1.1 Alien crosstalk mitigation

10GBASE-T is designed to operate over a channel that meets the specifications of 55.7 and the channel configuration shown Figure 55B–3. However, if the channel specifications of 55.7 cannot be met when using the channel configuration shown in Figure 55B–3, the configuration shown in Figure 55B–4 is recommended. This optimized channel for a 10GBASE-T link segment deletes the consolidation point or optional transition point and runs an equipment patch cord directly between the LAN equipment and the connector termination of the permanent link. This reduces the number of connectors and cordage and their associated alien crosstalk.



CP = consolidation point connector
TO = telecommunication outlet connector

Figure 55B–3—Maximum horizontal cabling configuration

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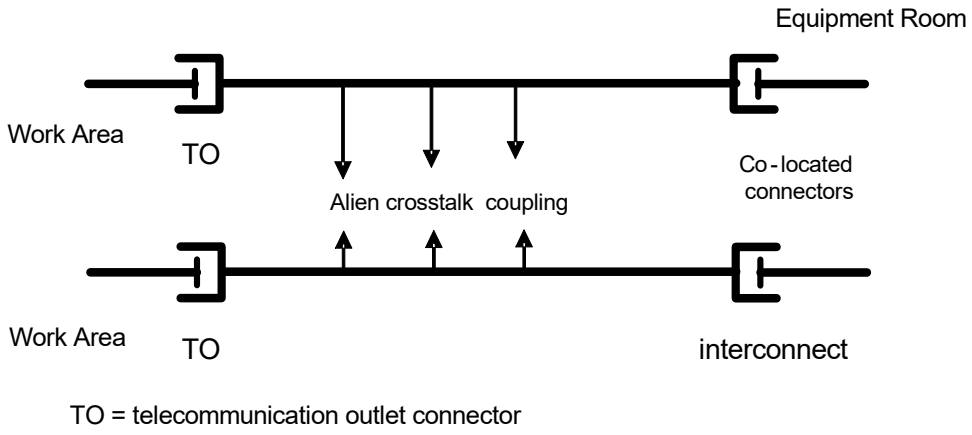

Figure 55B–4—Minimum horizontal cabling configuration

55B.1.2 Alien crosstalk mitigation procedure

This annex provides procedures and cabling guidelines designed to mitigate the alien crosstalk in the event that the alien crosstalk transmission parameters given in 55.7 are not met. For more information on mitigation techniques, see TIA TSB-155-A and ISO/IEC TR 24750.

The mitigation actions outlined below are based on four connector channels. In the majority of initially non-compliant cases, fewer than all corrective actions are required. Select the option(s) that is most appropriate for your situation.

a) When selective deployment of 10GBASE-T is possible, non-adjacent patch panel positions in the equipment room should be used. The adjacent positions may be used for other applications.
b) Reduce the number of co-located connectors by implementing an interconnect configuration to attach equipment to the horizontal cabling rather than a cross-connect. In general, connectors and cordage in the work area are not co-located.
c) Reduce the alien crosstalk coupling in the first 5 m to 20 m of the horizontal cabling by separating the equipment cords and the patch cords and un-bundling the horizontal cabling: in the case of a telecommunications room un-bundle the cabling to the point it exits the telecommunications room. A significant portion of the ANEXT coupling occurs in less than the first 20 m of cabling.
d) An alternative to separating equipment cords is to utilize equipment cords sufficiently specified to mitigate the alien crosstalk coupling.
e) Replace connectors with Category 6A/Class E_A.

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Annex 57A

(normative)

Requirements for support of Slow Protocols

57A.1 Introduction and rationale

There are two distinct classes of protocols used to control various aspects of the operation of IEEE 802.3 devices. They are as follows:

a) Protocols such as the MAC Control PAUSE operation (Annex 31B) that need to process and respond to PDUs rapidly in order to avoid performance degradation. These are likely to be implemented as embedded hardware functions, making it relatively unlikely that existing equipment could be easily upgraded to support additional such protocols.

   NOTE—This consideration was one of the contributing factors in the decision to use a separate group MAC address to support LACP and the Marker protocol, rather than re-using the group MAC address currently used for PAUSE frames.

b) Protocols such as LACP, with less stringent frequency and latency requirements. These may be implemented in software, with a reasonable expectation that existing equipment be upgradeable to support additional such protocols, depending upon the approach taken in the original implementation.

In order to place some realistic bounds upon the demands that might be placed upon such a protocol implementation, this annex defines the characteristics of this class of protocols and identifies some of the behaviors that an extensible implementation needs to exhibit.

57A.2 Slow Protocol transmission characteristics

Protocols that make use of the addressing and protocol identification mechanisms identified in this annex are subject to the following constraints:

a) The number of frames transmitted in any one-second period per Slow Protocol subtype shall not exceed aSlowProtocolFrameLimit (see 30.3.1.1.38).
b) The maximum number of Slow Protocols subtypes is 10.
c) The MAC Client data generated by any of these protocols shall be no larger than maxBasicDataSize (see 4.2.7.1). It is recommended that the maximum length for a Slow Protocol frame be limited to 128 octets.

The effect of these restrictions is to restrict the bandwidth consumed and performance demanded by this set of protocols; by default the maximum traffic loading that would result is 100 maximum length frames per second per point-to-point link and 100 maximum length frames per ONU for point-to-multipoint topologies.

57A.3 Addressing

The Slow_Protocols_Multicast address has been allocated exclusively for use by Slow Protocols PDUs; its value is identified in Table 57A–1.

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Table 57A–1—Slow_Protocols_Multicast address

Name	Value
Slow_Protocols_Multicast address	01-80-C2-00-00-02

NOTE 1—This address is within the range used by IEEE Std 802.1Q for link-constrained protocols. As such, frames sent to this address will not be forwarded by conformant MAC Bridges; its use is restricted to a single link.

NOTE 2—Although the two currently existing Slow Protocols (i.e., LACP and the Marker protocol) always use this MAC address as the destination address in transmitted PDUs, this may not be true for all Slow Protocols. In some yet-to-be-defined protocol, unicast addressing may be appropriate and necessary. Rather, the requirement is that this address not be used by any protocols that are not Slow Protocols.

57A.4 Protocol identification

All Slow Protocols use type interpretation of the Length/Type field, and use the Slow_Protocols_Type value as the primary means of protocol identification; its value is shown in Table 57A–2.

Table 57A–2—Slow_Protocols_Type value

Name	Value
Slow_Protocols_Type	88-09

The first octet of the MAC Client data following the Length/Type field is a protocol subtype identifier that distinguishes between different Slow Protocols. Table 57A–3 identifies the semantics of this subtype.

Table 57A–3—Slow Protocols subtypes

Protocol Subtype value	Protocol name
0	Unused—Illegal value
1	Link Aggregation Control Protocol (LACP)
2	Link Aggregation—Marker Protocol
3	Operations, Administration, and Maintenance (OAM)
4	Reserved for future use
5	Reserved for future use
6	Reserved for future use
7	Reserved for future use
8	Reserved for future use
9	Reserved for future use
10	Organization Specific Slow Protcol (OSSP)
11–255	Unused—Illegal values

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NOTE—Although this mechanism is defined as part of an IEEE 802.3 standard, it is the intent that the reserved code points in this table will be made available to protocols defined by other working groups within IEEE 802, should this mechanism be appropriate for their use.

57A.5 Handling of Slow Protocol frames

Any received MAC frame that carries the Slow_Protocols_Type field value is assumed to be a Slow Protocol frame. An implementation that claims conformance to this standard shall handle all Slow Protocol frames as follows:

a) Discard any Slow Protocol frame that carries an illegal value of Protocol Subtype (see Table 57A–3). Such frames shall not be passed to the MAC Client.

b) Pass any Slow Protocol frames that carry Protocol Subtype values that identify supported Slow Protocols to the protocol entity for the identified Slow Protocol.

c) Pass any Slow Protocol frames that carry Protocol Subtype values that identify unsupported Slow Protocols to the MAC Client.

NOTE—The intent of these rules is twofold. First, they rigidly enforce the maximum number of Slow Protocols, ensuring that early implementations of this mechanism do not become invalidated as a result of "scope creep." Second, they make it clear that the appropriate thing to do in any embedded frame parsing mechanism is to pass frames destined for unsupported protocols up to the MAC Client rather than discarding them, thus allowing for the possibility that, in soft configurable systems, the MAC Client might be enhanced in the future in order to support protocols that were not implemented in the hardware.

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57A.6 Protocol implementation conformance statement (PICS) proforma for Annex 57A, Requirements for support of Slow Protocols[283]

57A.6.1 Introduction

The supplier of an implementation that is claimed to conform to Annex 57A shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

57A.6.2 Identification

57A.6.2.1 Implementation identification

Supplier (Note 1)	
Contact point for inquiries about the PICS (Note 1)	
Implementation Name(s) and Version(s) (Notes 1 and 3)	
Other information necessary for full identification—e.g., name(s) and version(s) of machines and/or operating system names (Note 2)	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

57A.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 57A, Requirements for support of Slow Protocols.
Identification of amendments and corrigenda to the PICS proforma that have been completed as part of the PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21: the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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57A.6.2.3 Transmission characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
SP1	Transmission rate	57A.2	Max 10 frames in any one-second period	M	Yes [ ]
SP2	Data field	57A.2	No larger than maxBasicDataSize (see 4.2.7.1)	M	Yes [ ]

57A.6.2.4 Frame handling

Item	Feature	Subclause	Value/Comment	Status	Support
FH1	Handling of Slow Protocol frames	57A.5	As specified in 57A.5	M	Yes [ ]

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Annex 57B

(normative)

Organization specific slow protocol (OSSP)

The organization specific slow protocol (OSSP) provides a standardized means for organizations to define their own slow protocols outside the scope of this standard. The requirements defined in Annex 57A apply to these slow protocols.

57B.1 Transmission and representation of octets

An organization specific slow protocol data unit (OSSPDU) comprises an integral number of octets. The bits in each octet are numbered from 0 to 7, where 0 is the least significant bit. When consecutive octets are used to represent a numerical value, the most significant octet is transmitted first, followed by successively less significant octets.

57B.1.1 OSSPDU frame structure

The OSSPDU frame structure shall be as depicted in Figure 57B–1. In this figure:

a) Octets are transmitted from top to bottom.
b) Within an octet, bits are shown with bit 0 to the left and bit 7 to the right, and are transmitted from left to right.
c) When consecutive octets are used to represent a binary number, the octet transmitted first has the more significant value.
d) When consecutive octets are used to represent a MAC address, the least significant bit of the first octet is assigned the value of the first bit of the MAC address, the next most significant bit the value of the second bit of the MAC address, and so on through the eighth bit. Similarly the least significant through most significant bits of the second octet are assigned the value of the ninth through seventeenth bits of the MAC address, and so on for all the octets of the MAC address.
e) OSSPDUs are at least minFrameSize in length.

A OSSPDU shall have the following fields:

f) *Destination Address (DA).* The DA in OSSPDUs is the Slow_Protocols_Multicast address. Its use and encoding are specified in Annex 57A.
g) *Source Address (SA).* The SA in OSSPDUs is the individual MAC address associated with the port through which the OSSPDU is transmitted.
h) *Length/Type.* The Length/Type in OSSPDUs carries the Slow_Protocols_Type field value specified in 57A.4.
i) *Subtype.* The Subtype field identifies the specific Slow Protocol being encapsulated. OSSPDUs carry the Subtype value 0x0A as specified in Annex 57A.
j) *Organizationally Unique Identifier (OUI) or Company ID (CID).* The OUI/CID field contains the OUI or CID to identify the Organization Specific Data. The bit/octet ordering of the OUI/CID field within an OSSPDU is identical to the bit/octet ordering of the OUI portion of the DA/SA.
k) *Organization Specific Data*. The format and function of the Organization Specific Data field is dependent on the value of the OUI/CID field and is beyond the scope of this standard.
l) *FCS.* This field is the Frame Check Sequence, typically generated by the underlying MAC.

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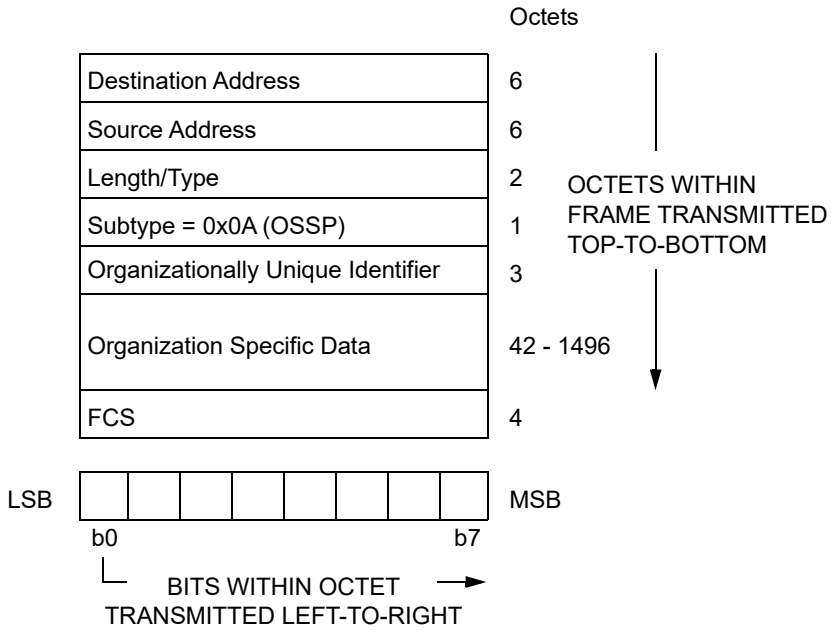

Figure 57B–1—OSSPDU structure

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57B.2 Protocol implementation conformance statement (PICS) proforma for Annex 57B, Organization specific slow protocol (OSSP)[284]

57B.2.1 Introduction

The supplier of an implementation that is claimed to conform to Annex 57B shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

57B.2.2 Identification

57B.2.2.1 Implementation identification

Supplier (Note 1)	
Contact point for inquiries about the PICS (Note 1)	
Implementation Name(s) and Version(s) (Notes 1 and 3)	
Other information necessary for full identification—e.g., name(s) and version(s) of machines and/or operating system names (Note 2)	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

57B.2.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 57B, Organization specific slow protocol (OSSP).
Identification of amendments and corrigenda to the PICS proforma that have been completed as part of the PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21: the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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57B.2.2.3 OSSPDU structure

Item	Feature	Subclause	Value/Comment	Status	Support
OS1	Organization Specific Protocol Data Unit (OSSPDU) frame structure	57B.1.1	As shown in Figure 57B–1 and as described	M	Yes [ ]

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Annex 58A

(informative)

Frame-based testing

The use of the frame-based test patterns described in Clause 58, Clause 59, and Clause 60 provides for the most general testing of the external interfaces. They combine patterns appropriate for testing the desired parameters with a flexible frame structure that allows the test pattern to be passed through a compliant system. However, the frame-based nature of the patterns may cause difficulties with some bit oriented test systems if care is not taken.

The concern is that streams of data that are passed through a system under test may have their inter-frame gap altered by rate control mechanisms. This changes the bit sequence, even in the presence of no errors, and causes difficulties with bit sequence oriented test systems. There are several methods of addressing this issue. The solutions fall roughly into the following three categories:

a) Error detection internal to the equipment under test
b) Use of frame-based test equipment
c) Synchronized systems

An example of the first type of test where the internal error detection would be used is a receiver sensitivity test. The input pattern may be generated by any method, including a bit oriented serial pattern generator or a frame-based pattern generator. Errored frames would be rejected internal to the system under test based on FCS errors. This type of test has the advantage of testing all of the components of an input interface. The error count may be made by accessing the error counters internal to the system under test.

The number of bit errors may be assumed to be the same as the number of frame errors to a 90% confidence level as long as frame error ratio is less than 0.2. The bit error ratio may be determined by dividing the frame error ratio by the number of bits in the test frame that are used in the computation of the FCS.

If the internal error counters are not accessible, the test frames may be passed to an output port and the number of received frames may the counted. Any missing frames may be assumed to have had errors. The frame count may be made by conventional frame-based test equipment. The missing frames render the use of bit stream oriented test equipment inappropriate.

When testing transmitter outputs, frames may be passed to the port under test from another port in the system under test. In this case, loss of frames within the system is not expected and testing may be done using a bit oriented test system by making the system synchronous. This may be done by recovering the clock from the output under test and using this as a clock source for the input. If there are no variable delays in the system under test, such as variable queuing delays, the input data stream will be reproduced in the output and conventional Bit Error Ratio Testing (BERT) systems may be used. In the case of 100BASE-X, the output bit stream may be inverted.

Two frame-based alternatives avoid the need for synchronization. The first is to use a frame-based tester for both the pattern generation and the error detection. The optical signal will need to be received by an optical receiver with the proper characteristics for the specific test. The processed data stream would then be sent to the frame-based receiver to determine possible frame errors.

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Another method would be to use a bit oriented test system suitable for burst mode operation. This type of tester will examine only the frame contents for errors. Two methods are used for determining the frame contents. An external gating signal may be used. This has to be triggered by the data source and include any latency associated with the system under test. Alternately, the test set may recognize the frame boundaries in the incoming data stream.

As the behavior above the MAC is not specified by this standard, the system under test might not be able to forward, return or respond to incoming frames at line rate. Diluting the frame rate is thought to be acceptable for 1000BASE-X but for 100BASE-X testing, groups of 12 frames should be kept together. A system might emit additional frames from a port and may need to be configured so that it does not.

NOTE—Users are advised to take care that the system under test is not connected to a network in service.

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Annex 58B

(informative)

Jitter, OMA, and TDP

58B.1 Jitter at TP1 and TP4 for 100BASE-LX10 and 100BASE-BX10

The entries in Table 58B–1 represent high-frequency jitter (above 20 kHz) and do not include low frequency jitter or wander. The informative Table 58B–1 shows jitter specifications which may be of interest to implementers. High probability jitter at TP2 is constrained by the eye mask. Total jitter at TP3 (and therefore at TP2 also) is constrained by the error detector timing offsets. High levels of high probability jitter at TP2, TP3 and TP4 are expected, caused by high probability baseline wander. The jitter difference between TP2 and TP3 is expected to be lower than for higher speed PMDs.

Table 58B–1—100BASE-LX10 and 100BASE-BX10 jitter budget

[a]	Total jitter		High probability jitter (*W*)	
Reference point	**UI**	**ns**	**UI**	**ns**
TP1	0.09	0.72	0.05	0.40
TP2	0.40	3.2	0.305	2.44
TP3	0.43	3.54	0.305	2.44
TP4	0.51	4.04	0.305	2.44

[a]Informative jitter values are chosen to be compatible with the limits for eye mask and TDP (see 58.7.9). Because of the way the different components may interact, the differences in jitter between test points cannot be used to indicate a performance level of the intervening sections.

Total jitter in this table is defined at 10^{-12} BER. In a commonly used model,

$$TJ_{12} = 14.1\sigma + W \text{ at } 10^{12} \quad (58B–1)$$

The total jitter at 10^{-10} BER may be calculated assuming

$$TJ_{10} = 12.7\sigma + W \quad (58B–2)$$

NOTE—As an example, TJ_{10} at TP1 is 0.085 UI (0.69 ns).

W is similar but not necessarily identical to deterministic jitter (DJ). A jitter measurement procedure is described in 58B.4. Jitter at TP2 or TP3 is defined with a receiver of the same bandwidth as specified for the transmitted eye.

58B.2 OMA relationship to extinction ratio and power measurements

This subclause is intended to inform on how the three quantities OMA, extinction ratio, and mean power, are related to each other.

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Optical modulation amplitude (OMA) is the difference between light levels for “1” and “0”. Extinction ratio is the ratio between light levels for “1” and “0”. If a signal contains equal density of “1” and “0” bits, and does not suffer from duty cycle distortion, the mean power is close to the mean of the light levels for “1” and “0”.

$$OMA = P_1 - P_0 \tag{58B–3}$$

OMA may be expressed in Watts or dBm.

$$ER = \frac{P_1}{P_0} \tag{58B–4}$$

Extinction ratio may be expressed in dB, as $10 \times \log_{10} (P_1 / P_0)$, or directly as a ratio. Sometimes extinction ratio is defined as P_0 / P_1.

$$P_{mean} \approx \frac{P_0 + P_1}{2} \tag{58B–5}$$

Mean power may be expressed in Watts or dBm.

P_1 and P_0 are usually measured with a standardized instrument bandwidth to reduce the effects of overshoot. It should be noted that the values of P_1 and P_0 depend on the measurement technique and pattern to be used, which vary with PMD type. For some PMD types, e.g. 10GBASE, different patterns leading to different values of P_1 and P_0 are used for OMA on the one hand, and extinction ratio on the other.

Aside from these differences:

$$P_1 \approx 2 \times P_{mean} \times \frac{ER}{ER + 1} \tag{58B–6}$$

$$P_0 \approx 2 \times \frac{P_{mean}}{ER + 1} \tag{58B–7}$$

$$OMA \approx 2 \times P_{mean} \times \frac{ER - 1}{ER + 1} \tag{58B–8}$$

Receiver sensitivity, which is an optical power, can be expressed in OMA or mean power terms according to the same relations.

NOTE—The OMA relationship to extinction ratio and power measurements applies to Clause 52, Clause 53, Clause 58, Clause 59, and Clause 60.

58B.3 Approximate measures of TDP

Transmitter and dispersion penalty may be considered as a transmitter penalty (TP) followed by a dispersion penalty, which is also attributable to the transmitter. Measurements at TP2 can reveal the transmitter penalty. TP can be related to eye mask margin (MM) as follows.

In the absence of any noise or significant jitter,

$$TP = 10 \times \log_{10}\left(\frac{1}{H}\right) \tag{58B–9}$$

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$$MM = \frac{H - M}{1 - M} \quad (58B–10)$$

where H is height of inner eye and M is the height of the central polygon of the mask.

Transmitter noise or noise-like impairments degrade both apparent MM and actual TP. To obtain a useful correlation between the two, MM is defined to an appropriate percentile of measured samples, to give the right weight to this noise; see 58.7.8. Oscilloscope noise degrades apparent MM only. This would distort the correlation, but in many measurement circumstances the error is reduced at the appropriate percentile. The one-dimensional statistics of MM measurement and the hit ratio are related by the frequency of relevant bit patterns in a stream (typically 1/4 of bits are flanked by two opposite bits) and by a factor related to mask dimensions.

This approach could be applied to a situation with combinations of noise of jitter.

It may be feasible to correlate TDP to eye measurements at TP3. However, the signal at TP3 is weaker, so oscilloscope noise is more of a concern.

The following suggestions apply to 100 Mb/s optical PMDs.

In practice it may be necessary to do without the clock recovery unit at 100 Mb/s. Experimentally, timing stability at this rate may be acceptable, and the jitter due to the CRU could be accounted for by adjusting the eye mask length and the TDP decision timing offsets.

A significant component of TDP is baseline wander. A wander of ± OMA/10 will be created by many receivers if it is not already present in the transmitted signal. Higher levels of pattern dependent penalty can in some cases be estimated from the mask margin (if necessary, by ignoring the upper and lower mask regions). The mask margin may also be measured with an AC-coupled measurement instrument with a high-pass filter of 10 kHz. It is likely that compliant implementations will pass the transmitter mask with both DC and AC-coupling. Certain implementations may be characterized by comparing the transmitted signal with the STM-1 mask, using a benign pattern such as PRBS7.

The accuracy of these approaches have not been established by the committee. Oscilloscope measurements at TP3 may be degraded by instrument noise.

58B.4 Jitter measurements

A jitter measurement method for use at 100 Mb/s or 1000 Mb/s is described in this subclause. The measurement is performed after any relevant fiber dispersion (at virtual TP3). The test pattern is specified in 58.7.1 or 59.7.1 as appropriate.

The transmit jitter is tested using a bit error ratio tester (BERT), where the tester scans the eye opening horizontally (varying the decision time) at the average optical power, at a virtual TP3 (hereafter referred to as simply TP3) and measures the bit error ratio at each point in time. The plot of BER as a function of sampling time is called the “bathtub curve.” The channel and receiver are as specified in e.g., 58.7.9.2 and 58.7.9.3. The receiver includes a defined filter function. The test pattern is the same as for receiver sensitivity measurements.

NOTE—The parameter W may also be estimated from jitter histograms using an oscilloscope. Jitter of an optical signal is measured with a test optical receiver with the receiver bandwidth specified (e.g., for eye mask conformance) for the transmitter under test concerned.

The experimental curve is compared with a mask defined by Equation (58B–11) and Equation (58B–12) and illustrated in Figure 58B–1:

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$$\log_{10}(BER) \le A - B\left(\frac{t - 0.5W}{\sigma}\right)^2 \quad (58B–11)$$

$$\log_{10}(BER) \le A - B\left(\frac{1 - t - 0.5W}{\sigma}\right)^2 \quad (58B–12)$$

where:

$$A = -1.75, B = \frac{\log_{10}(e)}{2} \approx 0.217$$

and t is the decision time specified in unit intervals (UI). $t = 0$ at the mean crossing time, which may be estimated as the mid-point between the 10^{-3} BER points.

The BER mask is defined for $10^{-12} < \text{BER} < 10^{-6}$. All points on the BER "bathtub curve" have to fall within the white area or below. It can be seen that in the case of an asymmetric measured bathtub curve, the worse side determines W and σ.

W ("high probability jitter") and deterministic jitter (DJ) are not necessarily the same, but may be similar. The quantity σ can be similar to random jitter (RJ) although it is determined by low probability pattern dependent jitter also. "Total jitter" (TJ) is taken to be $W + 14\sigma$.

.

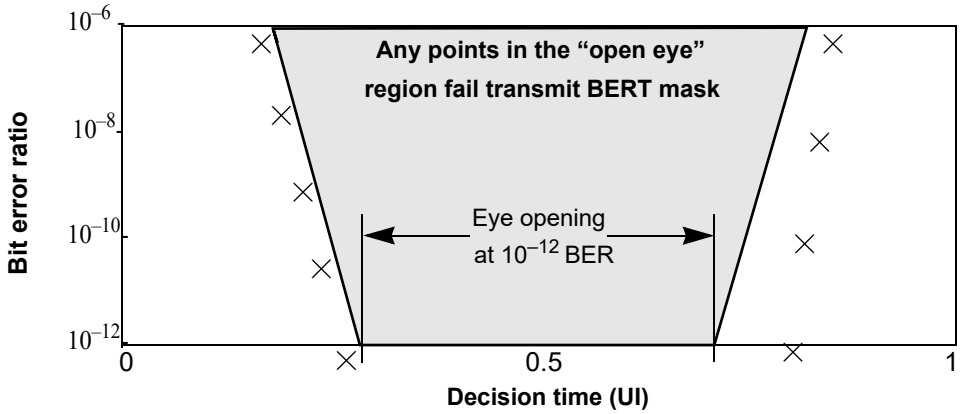

Figure 58B–1—Example transmit BER mask at TP3

NOTE—This jitter measurement method applies to Clause 58, Clause 59, and Clause 60.

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Annex 59A

(informative)

Jitter budget and measurements

59A.1 Jitter specifications

The entries for the 1000BASE-LX10 jitter budget on MMF in Table 59A–1 and the 1000BASE-LX10 and 1000BASE-BX10 jitter budget on SMF in Table 59A–2 represent high-frequency jitter (above 637 kHz) and do not include low frequency jitter or wander. All values are informative.

Table 59A–1—1000BASE-LX10 jitter budget on MMF

	Total jitter		*W*	
Reference point	**UI**	**ps**	**UI**	**ps**
TP1	0.240	192	0.100	80
TP1 to TP2	0.284	227	0.100	80
TP2	0.431	345	0.200	160
TP2 to TP3	0.170	136	0.050	40
TP3	0.510	408	0.250	200
TP3 to TP4	0.332	266	0.212	170
TP4	0.749	599	0.462	370

W is similar but not necessarily identical to deterministic jitter (DJ). A jitter measurement procedure is described in 58B.4. Other jitter measurements are described in 59A.2 and 59A.3. Jitter at TP2 or TP3 is defined with a receiver of the same bandwidth as specified for the transmitted eye.

Table 59A–2—1000BASE-LX10 and 1000BASE-BX10 jitter budget on SMF

	Total jitter		*W*	
Reference point	**UI**	**ps**	**UI**	**ps**
TP1	0.240	192	0.100	80
TP1 to TP2	0.334	267	0.150	120
TP2	0.481	385	0.250	200
TP2 to TP3	0.119	95	0	0
TP3	0.510	408	0.250	200
TP3 to TP4	0.332	266	0.212	170
TP4	0.749	599	0.462	370

NOTE—Informative jitter values are chosen to be compatible with the limits for eye mask and TDP (see 58.7.9). A margin between the total jitter at TP4 and the eye opening imposed by the decision point offsets for TDP is intended to allow for the performance of test equipment used for TDP measurement, to avoid very involved jitter calibrations.

Total jitter in this table is defined at 10^{-12} BER. In a commonly used model,

$$TJ = 14.1\sigma + DJ \text{ at } 10^{-12} \quad (59A–1)$$

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59A.2 Total jitter measurements

Total jitter measurements may be made according to the method in ANSI INCITS 230-1994 (R1999) (FC-PH), Annex A, A.4.2, or according to 58B.4. Total jitter at TP2 should be measured utilizing a BERT (bit error ratio tester). References to use of the Bessel-Thomson filter should substitute use of the Bessel-Thomson filter defined in 59.7.8. The test should utilize the mixed frequency test pattern specified in 59.7.1.

Total jitter at TP4 should be measured using the conformance test signal at TP3, as specified in 59.7.14. The optical power should be at the stressed receive sensitivity level in Table 59–5 for 1000BASE-LX10 and in Table 59–7 for 1000BASE-BX10. This power level should be corrected if the extinction ratio differs from the specified extinction ratio (minimum). Measurements at TP4 should be taken directly without additional Bessel-Thomson filters.

Jitter measurement may use a clock recovery unit (commonly referred to in the industry as a “golden PLL”) to remove low-frequency jitter from the measurement as shown in Figure 59A–1. The clock recovery unit has a low-pass filter with 20 dB/decade rolloff with –3 dB point of 637 kHz. For this measurement, the recovered clock will run at the signaling speed. The golden PLL is used to approximate the PLL in the deserializer function of the PMA. The PMA deserializer is able to track a large amount of low-frequency jitter (such as drift or wander) below its bandwidth. This low-frequency jitter would create a large measurement penalty, but does not affect operation of the link.

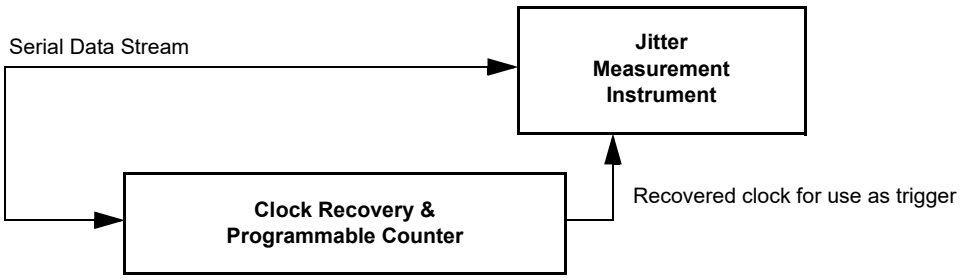

Figure 59A–1—Utilization of clock recovery unit during measurement

59A.3 Deterministic or high probability jitter measurement

Deterministic jitter may be measured according to ANSI INCITS 230-1994 (FC-PH), Annex A, A.4.3, DJ Measurement or high probability jitter may be measured according to 58B.4. The test utilizes the mixed frequency test pattern specified in 36A.3. This method utilizes a digital sampling scope to measure actual vs. predicted arrival of bit transitions of the 36A.3 data pattern (alternating K28.5 code-groups).

It is convenient to use the clock recovery unit described in 59A.2 for purposes of generating a trigger for the test equipment. This recovered clock should have a frequency equivalent to 1/20th of the signaling speed.

Measurements at TP2 and TP3 use the filter specified in 59.7.8, measurements at TP1 and TP4 do not use this filter.

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Annex 60A

(informative)

Jitter at TP1 to TP4 for 1000BASE-PX

The entries in Table 60A–1 and Table 60A–2 represent high-frequency jitter (above 637 kHz) and do not include low frequency jitter or wander. They are two sided (peak-to-peak) measures. Table 60A–1 applies to the downstream direction (D to U) while Table 60A–2 applies to the upstream direction (U to D). All values are informative.

Table 60A–1—1000BASE-PX downstream jitter budget

	Total jitter		Deterministic jitter	
Reference point	**UI**	**ps**	**UI**	**ps**
TP1	0.24	192	0.10	80
TP1 to TP2	0.191	153	0.15	120
TP2	0.431	345	0.25	200
TP2 to TP3	0.009	7	0	0
TP3	0.44	352	0.25	200
TP3 to TP4	0.309	247	0.212	170
TP4	0.749	599	0.462	370

Table 60A–2—1000BASE-PX upstream jitter budget

	No Jitter input to ONU				Jitter input to ONU			
	Total jitter		*W*		Total jitter		*W*	
Reference point	**UI**	**ps**	**UI**	**ps**	**UI**	**ps**	**UI**	**ps**
TP1	0.19	152	0.06	48	0.24	192	0.11	88
TP1 to TP2	0.16	128	0.14	112	0.16	128	0.14	112
TP2	0.35	280	0.2	160	0.4	320	0.25	200
TP2 to TP3	0.09	72	0.05	40	0.09	72	0.05	40
TP3	0.44	352	0.25	200	0.49	392	0.30	24
TP3 to TP4	0.18	144	0.15	120	0.18	144	0.15	120
TP4	0.62	496	0.4	320	0.67	536	0.45	360

For the 1000BASE-PX upstream jitter budget, the jitter transfer function is defined by Equation (60A–2) where the value is given in Figure 60A–1 when input sinusoidal jitter according to the mask defined in

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58.7.11.4 and values in Table 60–5, Table 60–8, Table 60–11, and Table 60–13 are applied to the receiver input of the ONU. Two sets of upstream jitter values are defined in Table 60A–2, one set corresponds to testing the upstream link with no jitter on the downstream (jitter generation) and the other set with maximum jitter on the downstream (generated and transferred jitter).

NOTE—Informative jitter values are chosen to be compatible with the limits for eye mask and TDP (see 58.7.9).

Total jitter in this table is defined at 10^{-12} BER. In a commonly used model,

$$TJ = 14.1\sigma + DJ \text{ at } 10^{12} \tag{60A–1}$$

W is similar but not necessarily identical to deterministic jitter (DJ). A jitter measurement procedure is described in 58B.4. Other jitter measurements are described in 59A.2 and 59A.3. Jitter at TP2 or TP3 is defined with a receiver of the same bandwidth as specified for the transmitted eye.

$$\text{Jitter Transfer} = 20\log_{10}\left[\frac{\text{Jitter on upstream signal (UI)}}{\text{Jitter on downstream signal (UI)}}\right] \tag{60A–2}$$

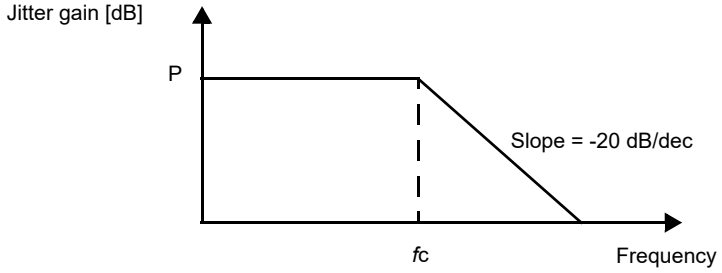

Figure 60A–1—Jitter gain curve values for 1000BASE-PX10-U and 1000BASE-PX20-U

Table 60A–3—Jitter gain curve values for 1000BASE-PX10-U and 1000BASE-PX20-U

	Value	Unit
P	0.3	dB
*f*c	1274	kHz

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Annex 61A

(informative)

EFM Copper examples

61A.1 Purpose and scope

The purpose of this informative annex is to provide practical examples of the use of

a) Aggregation Discovery, for aggregated operation of 10PASS-TS PHYs (Clause 62) or 2BASE-TL PHYs (Clause 63); see 61A.2.
b) 64/65-octet encapsulation, as specified in 61.3.3; see 61A.3.

61A.2 Aggregation Discovery example

An example procedure for PME aggregation discovery is described for system components as shown in Figure 61A–1, connected as in Figure 61A–2. Additional information on example discovery transactions are shown in Figure 61A–3. An example procedure for discovering this connectivity follows:

a) -O system writes remote_discovery_register to value *alpha* (*alpha* may be any 48-bit value, but would benefit from being locally unique e.g. MAC address) using PME-1.
b) -O system reads remote_discovery_register for all other PMEs.
c) -O system discovers that PME-2, PME-6 and PME-7 are associated with the same remote MAC device as PME-1.
d) -O system writes remote_discovery_register to value *alpha* using PME-3— the next non-associated PME.
e) -O system reads remote_discovery_register for all other PMEs.
f) -O system expects that PME-1, PME-2, PME-3, PME-6 and PME-7 will already be written to value *alpha*.
g) -O system discovers that no other PME is associated with the same remote MAC device as PME-3.
h) -O system writes remote_discovery_register to value *alpha* using PME-4—the next non-associated PME.
i) -O system reads remote_discovery_register for all other PMEs.
j) -O system expects that PME-1, PME-2, PME-3, PME-4, PME-6 and PME-7 will already be written to value *alpha*.
k) -O system discovers that PME-5, PME-9 and PME-11 are associated with the same remote MAC device as PME-4.
l) This procedure repeats for all of the PMEs connected to -O system.

An alternate example procedure for discovering this connectivity uses two different 48-bit values:

m) -O system writes remote_discovery_register to value *alpha* (*alpha* may be any 48-bit value, but would benefit from being locally unique e.g. MAC address) using PME-1.
n) -O system reads remote_discovery_register for all other PMEs.
o) -O system discovers that PME-2, PME-6 and PME-7 are associated with the same remote MAC device as PME-1.
p) -O system rewrites remote_discovery_register to value *beta* (*beta* may be any 48-bit value, different to *alpha*) using PME-1.
q) -O system writes remote_discovery_register to value *alpha* using PME-3— the next non-associated PME.

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r) -O system reads remote_discovery_register for all other PMEs.
s) -O system discovers that no other PME is associated with the same remote MAC device as PME-3.
t) -O system rewrites remote_discovery_register to value *beta* using PME-3.
u) -O system writes remote_discovery_register to value *alpha* using PME-4—the next non-associated PME.
v) -O system reads remote_discovery_register for all other PMEs.
w) -O system discovers that PME-5, PME-9 and PME-11 are associated with the same remote MAC device as PME-4.
x) -O system rewrites remote_discovery_register to value *beta* using PME-4.
y) This procedure repeats for all of the PMEs connected to -O system.

NOTE— This procedure can be expanded at the -O end to provide up to 32 unique alpha values. The -O end would then write a different alpha value on each port and then read all remote_discovery_register. Since the write operation is an atomic write, only one alpha value for each remote PCS will be written. All other subsequent write operations on that PCS will fail.

Observe also that a large and complex -O system may perform multiple discovery operations in parallel by using multiple unique 48-bit values for writing the remote_discovery_register.

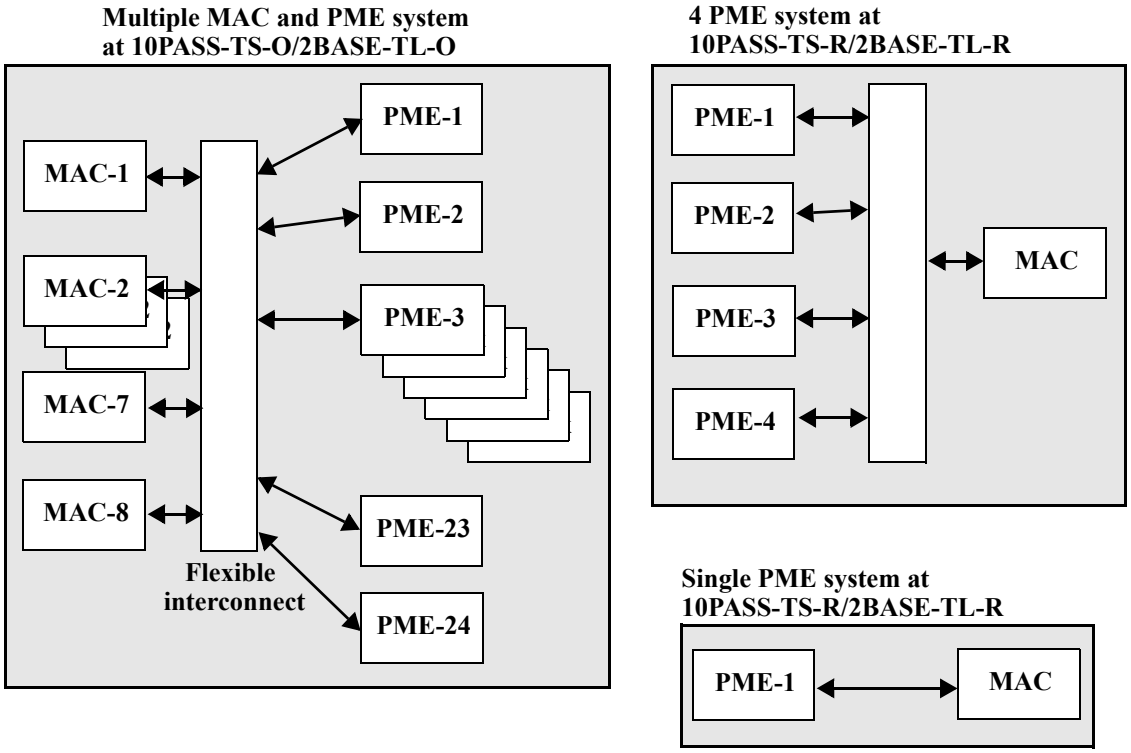

Figure 61A–1—Example systems for discovery

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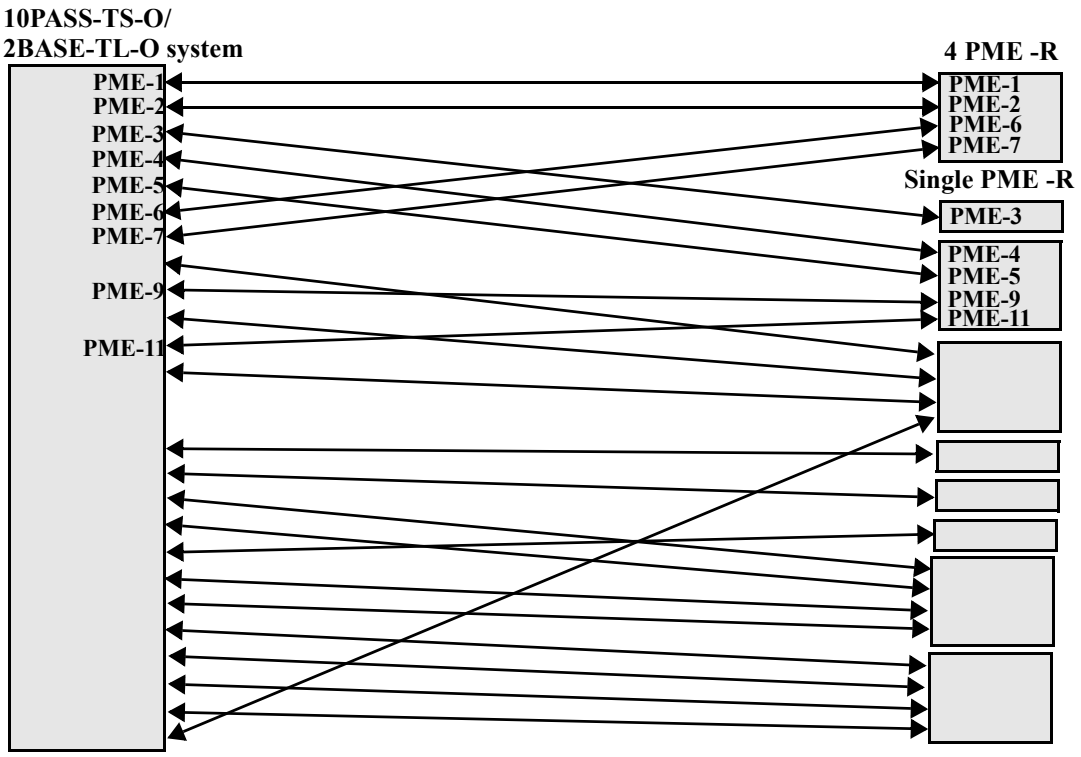

Figure 61A–2—System connectivity for discovery example

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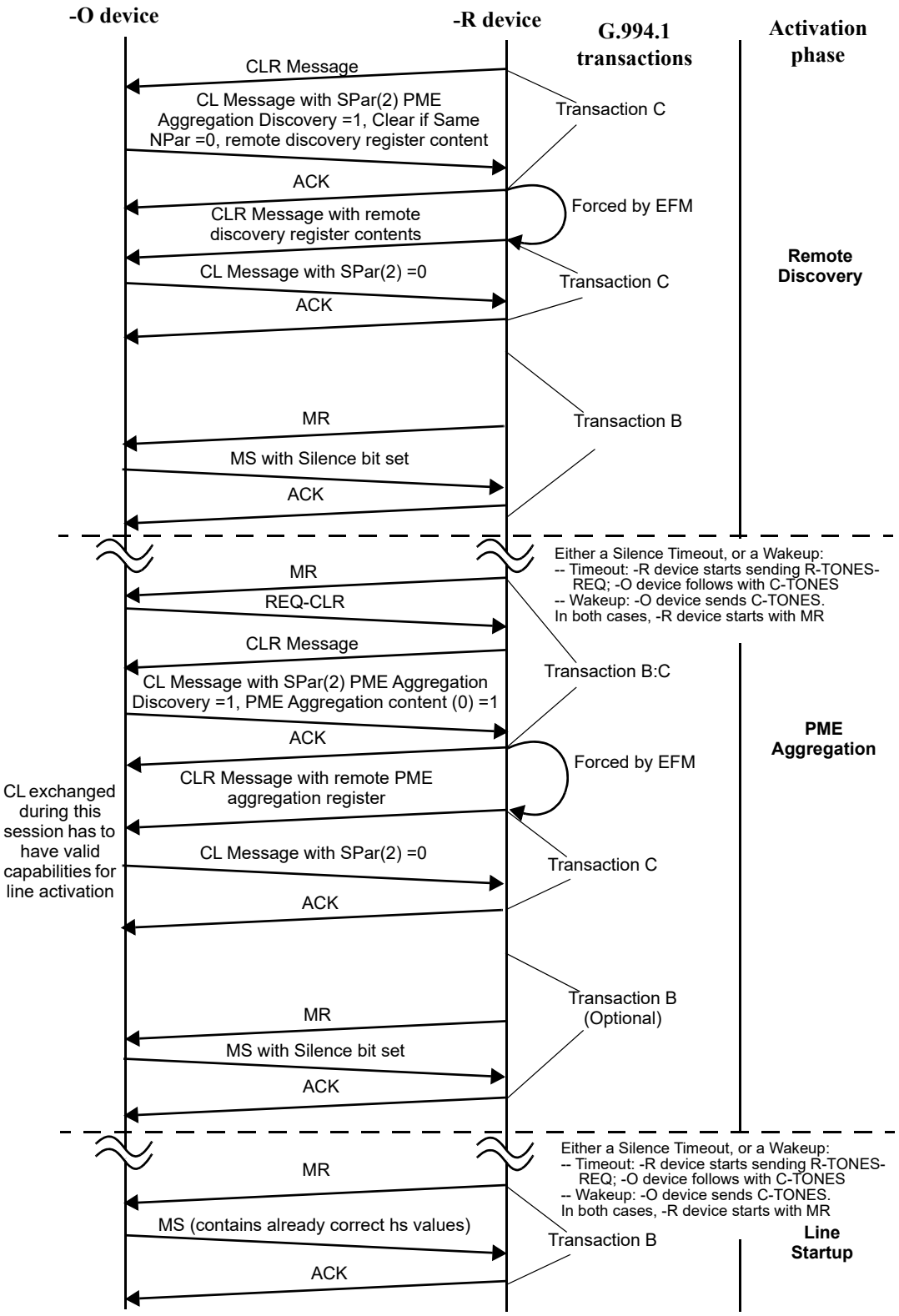

Figure 61A–3—Example activation sequence example

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61A.3 Example of 64/65-octet encapsulation

The code below [Equation (61A–1)] consists of an example "C" implementation of the 64/65-octet encapsulation specified in 61.3.3.

NOTE—The example implementation operates under the assumption that the receiver is synchronized at all times.

```
/*
*   802.3ah (EFM) 2BASE-TL (SHDSL) TC Transmitter simulator from 61.2.3
*/

#include <stdio.h>

/* test frame data */
char p0[] = {0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07,
 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E, 0x0F,
 0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x17,
 0x18, 0x19, 0x1A, 0x1B, 0x1C, 0x1D, 0x1E, 0x1F,
 0x20, 0x21, 0x22, 0x23, 0x24, 0x25, 0x26, 0x27,
 0x28, 0x29, 0x2A, 0x2B, 0x2C, 0x2D, 0x2E, 0x2F,
 0x30, 0x31, 0x32, 0x33, 0x34, 0x35, 0x36, 0x37,
 0x38, 0x39, 0x3A, 0x3B, 0x3C, 0x3D, 0x3E, 0x3F};

char p1[] = {0x40, 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47,
 0x48, 0x49, 0x4A, 0x4B, 0x4C, 0x4D, 0x4E, 0x4F,
 0x50, 0x51, 0x52, 0x53, 0x54, 0x55, 0x56, 0x57,
 0x58, 0x59, 0x5A, 0x5B, 0x5C, 0x5D, 0x5E, 0x5F,
 0x60, 0x61, 0x62, 0x63, 0x64, 0x65, 0x66, 0x67,
 0x68, 0x69, 0x6A, 0x6B, 0x6C, 0x6D, 0x6E, 0x6F,
 0x70, 0x71, 0x72, 0x73, 0x74, 0x75, 0x76, 0x77,
 0x78, 0x79, 0x7A, 0x7B, 0x7C, 0x7D, 0x7E, 0x7F,
 0x80, 0x81, 0x82, 0x83, 0x84, 0x85, 0x86, 0x87,
 0x88, 0x89, 0x8A, 0x8B, 0x8C, 0x8D, 0x8E, 0x8F};

char p2[] = {0x65, 0x43, 0x21};

#define NUM_CODEWORDS 14    /* number of 65 byte EFM codewords to transmit */

/*
* Define a list of user frames to transmit
*  NOTE: This list defines the set of test cases to transmit.
*/

struct frame {
 int  startingByteNum;    /* byte position at which frame is available to send */
 int  length;             /* number of bytes in ethernet frame */
 char *theBytes;          /* pointer to ethernet frame bytes */
} FrameList[] = {      /* To test: */
 {200, 64, p0},   /* vanilla frame, scrambler, C(k), crc */
 {389, 64, p0},   /* all data sync byte, sync splitting S/data/crc */
 {465, 50, p1},   /* end frame & start new frame in same codeword, C(0) */
 {530,  3, p2},   /* align small frame to span sync byte */
 {650, 64, p0},   /* S following sync byte */
 {700, 55, p1},   /* back-to-back frames, sync byte within crc */
 {0,0,0}          /* end test */
};

/* constants as per TC spec */

#define CODEWORD_BYTE_COUNT     65
#define SYNC_ALL_DATA           0x0F /* all data sync byte */
#define SYNC_NOT_ALL_DATA       0xF0     /* not all data sync byte */
#define START_OF_FRAME_BYTE     0x50     /* start data byte */
#define IDLE_BYTE               0x00     /* idle data byte */
#define EFM_CRC_POLY 0x82F63B78  /* X**28 + X**27 + X**26 + X**25 + X**23 +
 X**22 + X**20 + X**19 + X**18 + X**14 +
 X**13 + X**11 + X**10 + X**09 + X**08 +
 X**06 + X**00  (lsb is x**31) */

/* the EFM TC crc accumulator */
unsigned long CrcAccum;

void EfmCrcReset(void) {
 CrcAccum = 0xFFFFFFFF;
}

void EfmCrc(unsigned char TheByte) {
```


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```
 int i;
 /* for all the bits in TheByte, lsb first */
 for( i=0; i<8; i++) {
    /* xor the lsb of TheByte with the x**31 of CrcAccum */
    int FeedBack = 0x01 & (CrcAccum ^ TheByte);
    TheByte  = TheByte  >> 1;
    CrcAccum = CrcAccum >> 1;
    if(FeedBack) {
       CrcAccum = CrcAccum ^ EFM_CRC_POLY;
    }
 }
}

/* run with an argument to get test tags in output, else just the numbers */
main(int argc, char * argv[])
{
 int   ByteNum;
 int   UserFrameIndex   = 0;
 int   HaveUserFrame    = 0;
 int   FrameBytesToGo   = 0;
 char *FrameBytePointer = 0;
 int   NeedCZero        = 0;
 int   b;
 char  Foo[50];

 for(ByteNum=0; ByteNum < (CODEWORD_BYTE_COUNT * NUM_CODEWORDS) ; ByteNum++) {
    unsigned char ByteToSend;
    int BytesLeftInCodeword = CODEWORD_BYTE_COUNT - (ByteNum % CODEWORD_BYTE_COUNT);
    char *FrameTag = 0;
    /* decide what I'm doing */
    switch(ByteNum % CODEWORD_BYTE_COUNT) {
       case 0: /* output start of a codeword */
          if(FrameBytesToGo >= (CODEWORD_BYTE_COUNT-1)) {
             /* 64 or more bytes to go, send an all data codeword */
             ByteToSend = SYNC_ALL_DATA;
             FrameTag = "CODEWORD START (all data)";
          } else {
             ByteToSend = SYNC_NOT_ALL_DATA;
             FrameTag = "CODEWORD START (not all data)";
             if( ByteNum == 0) FrameTag = "EFM bitstream reading right to left.";
          }
          break;
       case 1: /* if a C(k) byte is needed */
          if((FrameBytesToGo && (FrameBytesToGo < (CODEWORD_BYTE_COUNT-1))) ||
NeedCZero) {
             int kVal = FrameBytesToGo;
             /* output a C(k) */
             ByteToSend = 0x10 + kVal;
             /* calculate even parity */
             for(b=0x40; b; b=b>>1) {
             if(ByteToSend & b) {
                ByteToSend ^= 0x80;
             }
          }
          NeedCZero = 0;
          /* display C(k) with decimal k */
          sprintf(Foo,"    C(%d)",kVal);
          FrameTag = Foo;
          break;
       }
       /* else fall into default case */
       default:
          /* if I'm
          *   not sending a frame and
          *   there are more to send, and
          *   it's time to start (next frame is available), and
          *   the frame is not too short to start now (including S and crc bytes)
          */
          if(   (FrameBytesToGo == 0)
          && (FrameList[UserFrameIndex].length != 0)
          && (ByteNum >= FrameList[UserFrameIndex].startingByteNum)
          && ((FrameList[UserFrameIndex].length+5) >= BytesLeftInCodeword) )
          {
             /* then start a new frame */
             FrameTag = "  Start Frame";
             ByteToSend = START_OF_FRAME_BYTE;
             FrameBytesToGo = FrameList[UserFrameIndex].length + 4;
             FrameBytePointer = FrameList[UserFrameIndex].theBytes;
             UserFrameIndex++;
             EfmCrcReset();
          } else if(FrameBytesToGo) {
```


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```
                /* else if inside a frame then handle outputting
                 * a data byte (or the crc to go with it) */
                switch(FrameBytesToGo) {
                case 4: /* send first crc byte */
                    FrameTag = "    First Crc Byte";
                    ByteToSend = 0xFF & ~CrcAccum;
                    break;
                case 3:
                    ByteToSend = 0xFF & ~(CrcAccum >> 8);
                    break;
                case 2:
                    ByteToSend = 0xFF & ~(CrcAccum >> 16);
                    break;
                case 1: /* send last crc byte */
                    FrameTag = "    Last Crc Byte";
                    ByteToSend = 0xFF & ~(CrcAccum >> 24);
                    /* if crc ends just before sync byte,
                     * prepare to send C(0) byte */
                    if (ByteNum % CODEWORD_BYTE_COUNT == 64) {
                    NeedCZero = 1;
                    }
                    break;
                default: /* just send next data byte and update crc */
                    ByteToSend = (unsigned char)*FrameBytePointer++;
                    /* calculate CRC on data (61.2.3.3) */
                    EfmCrc(ByteToSend);
                    break;
                }
            FrameBytesToGo--;
        } else {
            /* else just output an idle byte */
            ByteToSend = IDLE_BYTE;
        }
    }
    /* output the byte (msb on left) (transmission order is right to left)*/
    printf("%05.5d: %02.2X ", ByteNum, ByteToSend);
    for(b=0x80; b; b = b >> 1) {
        if(ByteToSend & b) {
            printf("1");
        } else {
            printf("0");
        }
    }
    if((argc > 1) && FrameTag) {
        printf("    ;%s", FrameTag);
    }
    printf("\n");
  }
  return(0);
}                                                                                    (61A-1)
```

The following data represents a valid data stream generated by the 64/65-octet encapsulation function (read left-to-right, then top-to-bottom).

```
F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 F0 00 00 00 00 50 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16
17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F 30 31 32 33 34 35 36
37 38 39 3A F0 99 3B 3C 3D 3E 3F EB 36 6D FB 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
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00 00 00 00 00 50 0F 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16 17 18
19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F 30 31 32 33 34 35 36 37 38
39 3A 3B 3C 3D 3E 3F F0 14 EB 36 6D FB 00 00 00 00 50 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D
4E 4F 50 51 52 53 54 55 56 57 58 59 5A 5B 5C 5D 5E 5F 60 61 62 63 64 65 66 67 68 69 6A 6B 6C 6D
6E 6F 70 71 55 A6 27 CE F0 90 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 50 65 43 21 93 8D FC 64 F0 90 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 F0 50 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13
14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F 30 31 32 33
34 35 36 37 38 39 3A 3B 3C 3D 3E F0 95 3F EB 36 6D FB 50 40 41 42 43 44 45 46 47 48 49 4A 4B 4C
4D 4E 4F 50 51 52 53 54 55 56 57 58 59 5A 5B 5C 5D 5E 5F 60 61 62 63 64 65 66 67 68 69 6A 6B 6C
6D 6E 6F 70 71 72 73 74 75 76 16 7C F0 12 07 58 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
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```
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00
```


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Annex 61B

(informative)

Handshake codepoints for 2BASE-TL and 10PASS-TS

61B.1 Purpose and scope

This annex contains the G.994.1 “standard information field” codepoints to be used by 2BASE-TL and 10PASS-TS in the procedures described in 61.4.

61B.2 Level-1 S field codepoints for 2BASE-TL and 10PASS-TS

The Npar(1) codepoints common to 2BASE-TL and 10PASS-TS are specified in Table 10 of G.994.1.

The SPar(1) codepoints to be used by 2BASE-TL and 10PASS-TS transceivers are specified in ITU-T Recommendation G.994.1. The EFM-specific codepoints are shown in Table 61B–1 for information only.

Table 61B–1—Standard information field — SPar(1) coding – Octet 4

Bits								
8	7	6	5	4	3	2	1	**SPar(1)s – Octet 4**
x	x	1	x	x	x	x	x	2BASE-TL
x	1	x	x	x	x	x	x	10PASS-TS
x	0	0	0	0	0	0	0	No parameters in this octet

61B.3 Codepoints for 2BASE-TL

61B.3.1 Level-2 S field codepoints for 2BASE-TL

Table 61B–2 through Table 61B–5 contain the level-2 codepoints specific to 2BASE-TL.

To support a wide range of data rates and multiple encodings, this section introduces a new way to encode data rates in G.994.1 code points. This method of encoding rates is used for both the PMMS rates and the training rates. Data rates are encoded as a set of ranges, where each range is expressed as a 3-tuple (minimum, maximum, step). The 3-tuple represents all rates of the form (m + ks)(64 kb/s) where m is the minimum value, s is the step value, and k is the set of all integers greater than or equal to zero such that m+ks is less than or equal to the maximum value. Thus, for example, the 3-tuple (40, 70, 10) represents the rates (40)(64 kb/s), (50)(64 kb/s), (60)(64 kb/s), and (70)(64 kb/s).

Each data rate parameter can be expressed as a set of between 1 to 8 ranges, where the supported rates are the union of those supported by the individual ranges. Thus, for example, the 3-tuples (20,30,4), (40,70,10) represent the rates (20)(64 kb/s), (24)(64 kb/s), (28)(64 kb/s), (40)(64 kb/s), (50)(64 kb/s), (60)(64 kb/s), and (70)(64 kb/s). If all bits of the extended base data rate minimum and maximum are set to zero, then those rates are not supported for line probe. If only one range of rates is required, then only the octets associated with (min1,max1,step1) shall be sent.

Also, in many cases, the values in the data range 3-tuple can be less than or equal to 89 (representing the maximum data rate of 5696 kb/s supported by 2BASE-TL). When using G.994.1 code point representation, only 6 bits are available for the value of an NPar(3). To support numbers greater than 63, the value has to be

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split across multiple octets. When encoding a data range using G.994.1, 4 octets are used, where the first octet contains the highest order bit from each of the values in the 3-tuple.

The following definition is added to the G.994.1 code point definitions in 6.4.1 of G.991.2 for the support of the extended data rates specified in this subclause.

Extended Base Data Rate These octets are used to specify payload rates, as follows:

- The PMMS octets indicate rates for line probing segments. Note that while PMMS uses 2-PAM modulation, the PMMS symbol rates are specified assuming 32 TC-PAM encoding, so the PMMS symbol rate (in kbaud) would be equal to the (payload data rate (kb/s) + 8 kb/s)/4. Valid values for minimum and maximum shall be between 4 and 89, inclusive, and valid values for step shall be between 1 and 89, inclusive. The variables j_5 and j_6 associated with the PMMS rates shall be independent, and shall range from 2 to 8, inclusive. If only one range of rates is required, then only the octets associated with (min1,max1,step1) shall be sent. If more than one range of rates is required, then j_5*4 and j_6*4 correspond to the number of octets sent.
- The training parameter octets indicate extended payload data rates supported.
- In CLR, upstream training parameters indicate which data mode rates the 2BASE-TL-R is capable of transmitting and downstream training parameters indicate which data mode rates the 2BASE-TL-R is capable of receiving. If the optional line probe is used, the receiver training parameters will be further limited by the probe results. Valid values for minimum and maximum shall be between 3 and 60, inclusive, for 16-TCPAM and between 12 and 89, inclusive, for 32-TCPAM. Valid values for step shall be between 1 and 89, inclusive. The variables j_1, j_2, j_3, and j_4 associated with the training rates shall be independent, and shall range from 2 to 8, inclusive. If only one range of rates is required, then only the octets associated with (min1,max1,step1) shall be sent. If more than one range of rates is required, then j_1*4, j_2*4, j_3*4, and j_4*4 correspond to the number of octets sent.
- In CL, downstream training parameters indicate which data mode rates the 2BASE-TL-O is capable of transmitting and upstream training parameters indicate which data mode rates the 2BASE-TL-O is capable of receiving. Valid values for minimum and maximum shall be between 3 and 60, inclusive, for 16-TCPAM and between 12 and 89, inclusive, for 32-TCPAM. Valid values for step shall be between 1 and 89, inclusive. The variables j_1, j_2, j_3, and j_4 associated with the training rates shall be independent, and shall range from 2 to 8, inclusive. If only one range of rates is required, then only the octets associated with (min1,max1,step1) shall be sent. If more than one range of rates

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is required, then j_1*4, j_2*4, j_3*4, and j_4*4 correspond to the number of octets sent. If optional line probe is used, the receiver training parameters will be further limited by the probe results.

— Data rate selections shall be specified in MP and MS messages by setting the maximum and minimum rates to the same value.

Table 61B–2—Standard information field – 2BASE-TL NPar(2) coding – Octet 1

Bits								
8	7	6	5	4	3	2	1	**2BASE-TL NPar(2)s – Octet 1**
x	x	x	x	x	x	x	1	2BASE-TL Training mode[a]
x	x	x	x	x	x	1	x	2BASE-TL PMMS mode[a]
x	x	x	x	x	1	x	x	2BASE-TL G.991.2 Annex A Operation
x	x	x	x	1	x	x	x	2BASE-TL G.991.2 Annex B Operation
x	x	x	1	x	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	1	x	x	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	0	0	0	0	0	0	No parameters in this octet

[a]Only one of these bits shall be set at any given time.

Table 61B–3—Standard information field – 2BASE-TL NPar(2) coding – Octet 2

Bits								
8	7	6	5	4	3	2	1	**2BASE-TL NPar(2)s – Octet 2**
x	x	x	x	x	x	x	1	Regenerator silent period[a,b]
x	x	x	x	x	x	1	x	SRU[b]
x	x	x	x	x	1	x	x	Diagnostic Mode[b]
x	x	x	x	1	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	x	1	x	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	1	x	x	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	0	0	0	0	0	0	No parameters in this octet

[a]This bit shall be set to 0_b if the 2BASE-TL PMMS mode NPar(2) bit is set to 1_b or the 2BASE-TL Training mode NPar(2) bit is set to 1_b.
[b]The specification and use of regenerators is outside the scope of this standard.

61B.3.2 Level-3 S field codepoints for 2BASE-TL

61B.3.2.1 Training parameter codepoints

Tables 61B–6 through 61B–39 contain the level-3 codepoints specific to 2BASE-TL training parameters.

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Table 61B–4—Standard information field – 2BASE-TL SPar(2) coding – Octet 1

Bits								
8	7	6	5	4	3	2	1	**2BASE-TL SPar(2)s – Octet 1**
x	x	x	x	x	x	x	1	2BASE-TL Downstream training parameters
x	x	x	x	x	x	1	x	2BASE-TL Downstream training rates - 16-TCPAM
x	x	x	x	x	1	x	x	2BASE-TL Downstream training rates - 32-TCPAM
x	x	x	x	1	x	x	x	2BASE-TL Upstream training parameters
x	x	x	1	x	x	x	x	2BASE-TL Upstream training rates - 16-TCPAM
x	x	1	x	x	x	x	x	2BASE-TL Upstream training rates - 32-TCPAM
x	x	0	0	0	0	0	0	No parameters in this octet

Table 61B–5—Standard information field – 2BASE-TL SPar(2) coding – Octet 2

Bits								
8	7	6	5	4	3	2	1	**2BASE-TL SPar(2)s – Octet 2**
x	x	x	x	x	x	x	1	2BASE-TL Downstream PMMS parameters
x	x	x	x	x	x	1	x	2BASE-TL Downstream PMMS rates
x	x	x	x	x	1	x	x	2BASE-TL Upstream PMMS parameters
x	x	x	x	1	x	x	x	2BASE-TL Upstream PMMS rates
x	x	x	1	x	x	x	x	2BASE-TL Downstream framing parameters
x	x	1	x	x	x	x	x	2BASE-TL Upstream framing parameters
x	x	0	0	0	0	0	0	No parameters in this octet

Table 61B–6—Standard information field – 2BASE-TL - Downstream training parameters - NPar(3) coding – Octet 1

Bits								
8	7	6	5	4	3	2	1	**2BASE-TL downstream training NPar(3)s – Octet 1**
x	x	0	x	x	x	x	x	Downstream PBO (dB) (bits 5–1 × 1.0 dB)
x	x	1	x	x	x	x	x	Reserved for allocation by IEEE Std 802.3

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Table 61B–7—Standard information field – 2BASE-TL - Downstream training rate - 16-TCPAM- NPar(3) coding – Octet 1

Bits								2BASE-TL downstream training rate - 16-TCPAM NPar(3)s – Octet 1
8	7	6	5	4	3	2	1	
x	x						x	Downstream base data rate -16-TCPAM Minimum 1 (bit 7)
x	x					x		Downstream base data rate -16-TCPAM Maximum 1 (bit 7)
x	x				x			Downstream base data rate -16-TCPAM Step 1 (bit 7)
x	x	x	x	x				Reserved for allocation by IEEE Std 802.3

Table 61B–8—Standard information field – 2BASE-TL - Downstream training rate - 16-TCPAM- NPar(3) coding – Octet 2

Bits								2BASE-TL downstream training rate - 16-TCPAM NPar(3)s – Octet 2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Downstream base data rate -16-TCPAM Minimum 1 (bit 1–6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–9—Standard information field – 2BASE-TL - Downstream training rate - 16-TCPAM - NPar(3) coding – Octet 3

Bits								2BASE-TL downstream training rate - 16-TCPAM NPar(3)s – Octet 3
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Downstream base data rate -16-TCPAM Maximum 1 (bit 1–6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–10—Standard information field – 2BASE-TL - Downstream training rate - 16-TCPAM - NPar(3) coding – Octet 4

Bits								2BASE-TL downstream training rate - 16-TCPAM NPar(3)s Octet 4
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Downstream base data rate -16-TCPAM Step 1 (bit 1–6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

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Table 61B–11—Standard information field – 2BASE-TL - Downstream training rate - 16-TCPAM- NPar(3) coding – Octet j_1*4-3

Bits								2BASE-TL downstream training rate - 16-TCPAM NPar(3)s – Octet j_1*4-3
8	7	6	5	4	3	2	1	
x	x						x	Extended Downstream base data rate -16-TCPAM Minimum j_1 (bit 7)
x	x					x		Extended Downstream base data rate -16-TCPAM Maximum j_1 (bit 7)
x	x				x			Extended Downstream base data rate -16-TCPAM Step j_1 (bit 7)
x	x	x	x	x				Reserved for allocation by IEEE Std 802.3

Table 61B–12—Standard information field – 2BASE-TL - Downstream training rate - 16-TCPAM- NPar(3) coding – Octet j_1*4-2

Bits								2BASE-TL downstream training rate - 16-TCPAM NPar(3)s – Octet j_1*4-2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Extended Downstream base data rate -16-TCPAM Minimum j_1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–13—Standard information field – 2BASE-TL - Downstream training rate - 16-TCPAM - NPar(3) coding – Octet j_1*4-1

Bits								2BASE-TL downstream training rate - 16-TCPAM NPar(3)s – Octet j_1*4-1
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Extended Downstream base data rate -16-TCPAM Maximum j_1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–14—Standard information field – 2BASE-TL - Downstream training rate - 16-TCPAM - NPar(3) coding – Octet j_1*4

Bits								2BASE-TL downstream training rate - 16-TCPAM NPar(3)s Octet j_1*4
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Extended Downstream base data rate -16-TCPAM Step j_1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

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Table 61B–15—Standard information field – 2BASE-TL - Downstream training rate - 32-TCPAM- NPar(3) coding – Octet 1

Bits								2BASE-TL downstream training rate - 32-TCPAM NPar(3)s – Octet 1
8	7	6	5	4	3	2	1	
x	x						x	Downstream base data rate -32-TCPAM Minimum 1 (bit 7)
x	x					x		Downstream base data rate -32-TCPAM Maximum 1 (bit 7)
x	x				x			Downstream base data rate -32-TCPAM Step 1 (bit 7)
x	x	x	x	x				Reserved for allocation by IEEE Std 802.3

Table 61B–16—Standard information field – 2BASE-TL - Downstream training rate - 32-TCPAM- NPar(3) coding – Octet 2

Bits								2BASE-TL downstream training rate - 32-TCPAM NPar(3)s – Octet 2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Downstream base data rate -32-TCPAM Minimum 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–17—Standard information field – 2BASE-TL - Downstream training rate - 32-TCPAM - NPar(3) coding – Octet 3

Bits								2BASE-TL downstream training rate - 32-TCPAM NPar(3)s – Octet 3
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Downstream base data rate -32-TCPAM Maximum 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–18—Standard information field – 2BASE-TL - Downstream training rate - 32-TCPAM - NPar(3) coding – Octet 4

Bits								2BASE-TL downstream training rate - 32-TCPAM NPar(3)s Octet 4
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Downstream base data rate -32-TCPAM Step 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

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Table 61B–19—Standard information field – 2BASE-TL - Downstream training rate - 32-TCPAM- NPar(3) coding – Octet j_2*4-3

Bits								2BASE-TL downstream training rate - 32-TCPAM NPar(3)s – Octet j_2*4-3
8	7	6	5	4	3	2	1	
x	x						x	Extended Downstream base data rate - 32-TCPAM Minimum j_2 (bit 7)
x	x					x		Extended Downstream base data rate - 32-TCPAM Maximum j_2 (bit 7)
x	x				x			Extended Downstream base data rate - 32-TCPAM Step j_2 (bit 7)
x	x	x	x	x				Reserved for allocation by IEEE Std 802.3

Table 61B–20—Standard information field – 2BASE-TL - Downstream training rate - 32-TCPAM- NPar(3) coding – Octet j_2*4-2

Bits								2BASE-TL downstream training rate - 32-TCPAM NPar(3)s – Octet j_2*4-2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Extended Downstream base data rate - 32-TCPAM Minimum j_2 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–21—Standard information field – 2BASE-TL - Downstream training rate - 32-TCPAM - NPar(3) coding – Octet j_2*4-1

Bits								2BASE-TL downstream training rate - 32-TCPAM NPar(3)s – Octet j_2*4-1
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Extended Downstream base data rate - 32-TCPAM Maximum j_2 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–22—Standard information field – 2BASE-TL - Downstream training rate - 32-TCPAM - NPar(3) coding – Octet j_2*4

Bits								2BASE-TL downstream training rate - 32-TCPAM NPar(3)s Octet j_2*4
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Extended Downstream base data rate - 32-TCPAM Step j_2 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

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Table 61B–23—Standard information field – 2BASE-TL - Upstream training parameters - NPar(3) coding – Octet 1

Bits								2BASE-TL upstream training NPar(3)s – Octet 1
8	7	6	5	4	3	2	1	
x	x	0	x	x	x	x	x	Upstream PBO (dB) (bits 5-1 × 1.0 dB)
x	x	1	x	x	x	x	x	Reserved for allocation by IEEE Std 802.3

Table 61B–24—Standard information field – 2BASE-TL - upstream training rate - 16-TCPAM-NPar(3) coding – Octet 1

Bits								2BASE-TL upstream training rate - 16-TCPAM NPar(3)s – Octet 1
8	7	6	5	4	3	2	1	
x	x						x	Upstream base data rate -16-TCPAM Minimum 1 (bit 7)
x	x					x		Upstream base data rate -16-TCPAM Maximum 1 (bit 7)
x	x				x			Upstream base data rate -16-TCPAM Step 1 (bit 7)
x	x	x	x	x				Reserved for allocation by IEEE Std 802.3

Table 61B–25—Standard information field – 2BASE-TL - upstream training rate - 16-TCPAM-NPar(3) coding – Octet 2

Bits								2BASE-TL upstream training rate - 16-TCPAM NPar(3)s – Octet 2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Upstream base data rate -16-TCPAM Minimum 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–26—Standard information field – 2BASE-TL - upstream training rate - 16-TCPAM - NPar(3) coding – Octet 3

Bits								2BASE-TL upstream training rate - 16-TCPAM NPar(3)s – Octet 3
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Upstream base data rate -16-TCPAM Maximum 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

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Table 61B–27—Standard information field – 2BASE-TL - Upstream training rate - 16-TCPAM - NPar(3) coding – Octet 4

Bits								2BASE-TL upstream training rate - 16-TCPAM NPar(3)s Octet 4
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Upstream base data rate -16-TCPAM Step 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–28—Standard information field – 2BASE-TL - Upstream training rate - 16-TCPAM-NPar(3) coding – Octet j_3*4-3

Bits								2BASE-TL upstream training rate - 16-TCPAM NPar(3)s – Octet j_3*4-3
8	7	6	5	4	3	2	1	
x	x						x	Extended Upstream base data rate - 16-TCPAM Minimum j_3 (bit 7)
x	x					x		Extended Upstream base data rate -16-TCPAM Maximum j_3 (bit 7)
x	x				x			Extended Upstream base data rate -16-TCPAM Step j_3 (bit 7)
x	x	x	x	x				Reserved for allocation by IEEE 802.3

Table 61B–29—Standard information field – 2BASE-TL - Upstream training rate - 16-TCPAM-NPar(3) coding – Octet j_3*4-2

Bits								2BASE-TL upstream training rate - 16-TCPAM NPar(3)s – Octet j_3*4-2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Extended Upstream base data rate -16-TCPAM Minimum j_3 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–30—Standard information field – 2BASE-TL - Upstream training rate - 16-TCPAM - NPar(3) coding – Octet j_3*4-1

Bits								2BASE-TL upstream training rate - 16-TCPAM NPar(3)s – Octet j_3*4-1
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Extended Upstream base data rate -16-TCPAM Maximum j_3 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

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Table 61B–31—Standard information field – 2BASE-TL - Upstream training rate - 16-TCPAM - NPar(3) coding – Octet j_3*4

Bits								2BASE-TL upstream training rate - 16-TCPAM NPar(3)s Octet j_3*4
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Extended Upstream base data rate -16-TCPAM Step j_3 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–32—Standard information field – 2BASE-TL - Upstream training rate - 32-TCPAM-NPar(3) coding – Octet 1

Bits								2BASE-TL upstream training rate - 32-TCPAM NPar(3)s – Octet 1
8	7	6	5	4	3	2	1	
x	x						x	Upstream base data rate -32-TCPAM Minimum 1 (bit 7)
x	x					x		Upstream base data rate -32-TCPAM Maximum 1 (bit 7)
x	x				x			Upstream base data rate -32-TCPAM Step 1 (bit 7)
x	x	x	x	x				Reserved for allocation by IEEE Std 802.3

Table 61B–33—Standard information field – 2BASE-TL - Upstream training rate - 32-TCPAM-NPar(3) coding – Octet 2

Bits								2BASE-TL upstream training rate - 32-TCPAM NPar(3)s – Octet 2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Upstream base data rate -32-TCPAM Minimum 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–34—Standard information field – 2BASE-TL - Upstream training rate - 32-TCPAM - NPar(3) coding – Octet 3

Bits								2BASE-TL upstream training rate - 32-TCPAM NPar(3)s – Octet 3
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Upstream base data rate -32-TCPAM Maximum 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

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Table 61B–35—Standard information field – 2BASE-TL - Upstream training rate - 32-TCPAM - NPar(3) coding – Octet 4

Bits								2BASE-TL upstream training rate - 32-TCPAM NPar(3)s Octet 4
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Upstream base data rate -32-TCPAM Step 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–36—Standard information field – 2BASE-TL - Upstream training rate - 32-TCPAM-NPar(3) coding – Octet j_4*4-3

Bits								2BASE-TL upstream training rate - 32-TCPAM NPar(3)s – Octet j_4*4-3
8	7	6	5	4	3	2	1	
x	x						x	Extended Upstream base data rate - 32-TCPAM Minimum j_4 (bit 7)
x	x					x		Extended Upstream base data rate - 32-TCPAM Maximum j_4 (bit 7)
x	x				x			Extended Upstream base data rate - 32-TCPAM Step j_4 (bit 7)
x	x	x	x	x				Reserved for allocation by IEEE Std 802.3

Table 61B–37—Standard information field – 2BASE-TL - Upstream training rate - 32-TCPAM-NPar(3) coding – Octet j_4*4-2

Bits								2BASE-TL upstream training rate - 32-TCPAM NPar(3)s – Octet j_4*4-2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Extended Upstream base data rate - 32-TCPAM Minimum j_4 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–38—Standard information field – 2BASE-TL - Upstream training rate - 32-TCPAM - NPar(3) coding – Octet j_4*4-1

Bits								2BASE-TL upstream training rate - 32-TCPAM NPar(3)s – Octet j_4*4-1
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Extended Upstream base data rate -32-TCPAM Maximum j_4 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

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Table 61B–39—Standard information field – 2BASE-TL - Upstream training rate - 32-TCPAM - NPar(3) coding – Octet j_4*4

Bits								2BASE-TL upstream training rate - 32-TCPAM NPar(3)s Octet j_4*4
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Extended Upstream base data rate -32-TCPAM Step j_4 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

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61B.3.2.2 PMMS parameter codepoints

Tables 61B–40 through 61B–67 contain the level-3 codepoints specific to 2BASE-TL PMMS parameters.

Table 61B–40—Standard information field – 2BASE-TL - Downstream PMMS parameters - NPar(3) coding – Octet 1

Bits								2BASE-TL downstream PMMS NPar(3)s – Octet 1
8	7	6	5	4	3	2	1	
x	x	0	x	x	x	x	x	Downstream PBO (dB) (bits 5-1 × 1.0 dB)
x	x	1	x	x	x	x	x	Reserved for allocation by IEEE Std 802.3

Table 61B–41—Standard information field – 2BASE-TL - Downstream PMMS parameters - NPar(3) coding – Octet 2

Bits								2BASE-TL downstream PMMS NPar(3)s – Octet 2
8	7	6	5	4	3	2	1	
x	x	0	0	0	0	0	0	Downstream PMMS duration unspecified by terminal
x	x	x	x	x	x	x	x	Downstream PMMS duration (bits 6-1 x 50 ms)
x	x	1	1	1	1	1	1	Reserved for allocation by IEEE Std 802.3

Table 61B–42—Standard information field – 2BASE-TL - Downstream PMMS parameters - NPar(3) coding – Octet 3

Bits								2BASE-TL downstream PMMS NPar(3)s – Octet 3
8	7	6	5	4	3	2	1	
x	x	0	0	0	x	x	x	Downstream PMMS scrambler polynomial Index (i2, i1, i0)

Table 61B–43—Standard information field – 2BASE-TL - Downstream PMMS parameters - NPar(3) coding – Octet 4

Bits								2BASE-TL downstream PMMS NPar(3)s – Octet 4
8	7	6	5	4	3	2	1	
x	x	1	x	x	x	x	x	Worst-case PMMS target margin (dB) (bits 5-1 × 1.0 dB - 10 dB)
x	x	0	0	0	0	0	0	Worst-case PMMS target margin unspecified by terminal (values of bits 6-1 from 1 to 31 reserved for allocation by IEEE Std 802.3)

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Table 61B–44—Standard information field – 2BASE-TL - Downstream PMMS parameters - NPar(3) coding – Octet 5

Bits								2BASE-TL downstream PMMS NPar(3)s – Octet 5
8	7	6	5	4	3	2	1	
x	x	1	x	x	x	x	x	Current-condition PMMS target margin (dB) (bits 5-1 × 1.0 dB - 10 dB)
x	x	0	0	0	0	0	0	Current-condition PMMS target margin unspecified by terminal (values of bits 6-1 from 1 to 31 reserved for allocation by IEEE Std 802.3)

Table 61B–45—Standard information field – 2BASE-TL - Downstream PMMS parameters - NPar(3) coding – Octet 6

Bits								2BASE-TL downstream PMMS NPar(3)s – Octet 6
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	1	Reserved for allocation by IEEE Std 802.3
x	x	x	x	x	x	1	x	Transmit Silence
x	x	x	x	x	1	x	x	Reserved for allocation by IEEE Std 802.3
x	x	x	x	1	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	x	1	x	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	1	x	x	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	0	0	0	0	0	0	No parameters in this octet

Table 61B–46—Standard information field – 2BASE-TL - Downstream PMMS rates - NPar(3) coding – Octet 1

Bits								2BASE-TL downstream PMMS NPar(3)s – Octet 1
8	7	6	5	4	3	2	1	
x	x						x	Downstream base data rate- 32-TCPAM Minimum 1 (bit 7)
						x		Downstream base data rate- 32-TCPAM Maximum 1 (bit 7)
x	x				x			Downstream base data rate- 32-TCPAM Step 1 (bit 7)
x	x	x	x	x				Reserved for allocation by IEEEStd 802.3

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Table 61B–47—Standard information field – 2BASE-TL - Downstream PMMS rates - NPar(3) coding – Octet 2

Bits								2BASE-TL downstream PMMS rates NPar(3)s – Octet 2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Downstream base data rate- 32-TCPAM Minimum 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–48—Standard information field – 2BASE-TL - Downstream PMMS rates - NPar(3) coding – Octet 3

Bits								2BASE-TL downstream PMMS rates NPar(3)s – Octet 3
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Downstream base data rate- 32-TCPAM Maximum 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–49—Standard information field – 2BASE-TL - Downstream PMMS rates - NPar(3) coding – Octet 4

Bits								2BASE-TL downstream PMMS NPar(3)s Octet 6
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Downstream base data rate- 32-TCPAM Step 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–50—Standard information field – 2BASE-TL - Downstream PMMS rates - NPar(3) coding – Octet j_5*4-3

Bits								2BASE-TL downstream PMMS NPar(3)s – Octet j_5*4-3
8	7	6	5	4	3	2	1	
x	x						x	Downstream base data rate- 32-TCPAM Minimum j_5 (bit 7)
x	x					x		Downstream base data rate- 32-TCPAM Maximum j_5 (bit 7)
x	x				x			Downstream base data rate- 32-TCPAM Step j_5 (bit 7)
x	x	x	x	x				Reserved for allocation by IEEE Std 802.3

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Table 61B–51—Standard information field – 2BASE-TL - Downstream PMMS rates - NPar(3) coding – Octet j_5*4-2

Bits								2BASE-TL downstream PMMS rates NPar(3)s – Octet j_5*4-2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Downstream base data rate- 32-TCPAM Minimum j_5 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–52—Standard information field – 2BASE-TL - Downstream PMMS rates - NPar(3) coding – Octet j_5*4-1

Bits								2BASE-TL downstream PMMS rates NPar(3)s – Octet j_5*4-1
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Downstream base data rate- 32-TCPAM Maximum j_5 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–53—Standard information field – 2BASE-TL - Downstream PMMS rates - NPar(3) coding – Octet j_5*4

Bits								2BASE-TL downstream PMMS NPar(3)s Octet j_5*4
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Downstream base data rate- 32-TCPAM Step j_5 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–54—Standard information field – 2BASE-TL - Upstream PMMS parameters - NPar(3) coding – Octet 1

Bits								2BASE-TL upstream PMMS NPar(3)s – Octet 1
8	7	6	5	4	3	2	1	
x	x	0	x	x	x	x	x	Upstream PBO (dB) (bits 5-1 × 1.0 dB)
x	x	1	x	x	x	x	x	Reserved for allocation by IEEE Std 802.3

Table 61B–55—Standard information field – 2BASE-TL - Upstream PMMS parameters - NPar(3) coding – Octet 2

Bits								2BASE-TL upstream PMMS NPar(3)s – Octet 2
8	7	6	5	4	3	2	1	
x	x	0	0	0	0	0	0	Upstream PMMS duration unspecified by terminal
x	x	x	x	x	x	x	x	Upstream PMMS duration (bits 6-1 × 50 ms)
x	x	1	1	1	1	1	1	Reserved for allocation by IEEE Std 802.3

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Table 61B–56—Standard information field – 2BASE-TL - Upstream PMMS parameters - NPar(3) coding – Octet 3

Bits								2BASE-TL upstream PMMS NPar(3)s – Octet 3
8	7	6	5	4	3	2	1	
x	x	0	0	0	x	x	x	Upstream PMMS scrambler polynomial Index (i2, i1, i0)

Table 61B–57—Standard information field – 2BASE-TL - Upstream PMMS parameters - NPar(3) coding – Octet 4

Bits								2BASE-TL upstream PMMS NPar(3)s – Octet 4
8	7	6	5	4	3	2	1	
x	x	1	x	x	x	x	x	Worst-case PMMS target margin (dB) (bits 5-1 × 1.0 dB - 10 dB)
x	x	0	0	0	0	0	0	Worst-case PMMS target margin unspecified by terminal (values of bits 6-1 from 1 to 31 reserved for allocation by IEEE Std 802.3)

Table 61B–58—Standard information field – 2BASE-TL - Upstream PMMS parameters - NPar(3) coding – Octet 5

Bits								2BASE-TL upstream PMMS NPar(3)s – Octet 5
8	7	6	5	4	3	2	1	
x	x	1	x	x	x	x	x	Current-condition PMMS target margin (dB) (bits 5-1 × 1.0 dB – 10 dB)
x	x	0	0	0	0	0	0	Current-condition PMMS target margin unspecified by terminal (values of bits 6-1 from 1 to 31 reserved for allocation by IEEE Std 802.3)

Table 61B–59—Standard information field – 2BASE-TL - Upstream PMMS parameters - NPar(3) coding – Octet 6

Bits								2BASE-TL upstream PMMS NPar(3)s – Octet 6
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	1	Reserved for allocation by IEEE Std 802.3
x	x	x	x	x	x	1	x	Transmit Silence
x	x	x	x	x	1	x	x	Reserved for allocation by IEEE Std 802.3
x	x	x	x	1	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	x	1	x	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	1	x	x	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	0	0	0	0	0	0	No parameters in this octet

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Table 61B–60—Standard information field – 2BASE-TL - Upstream PMMS rates - NPar(3) coding – Octet 1

Bits								2BASE-TL upstream PMMS NPar(3)s – Octet 1
8	7	6	5	4	3	2	1	
x	x						x	Upstream base data rate- 32-TCPAM Minimum 1 (bit 7)
x	x					x		Upstream base data rate- 32-TCPAM Maximum 1 (bit 7)
x	x				x			Upstream base data rate- 32-TCPAM Step 1 (bit 7)
x	x	x	x	x				Reserved for allocation by IEEE Std 802.3

Table 61B–61—Standard information field – 2BASE-TL - Upstream PMMS rates - NPar(3) coding – Octet 2

Bits								2BASE-TL upstream PMMS rates NPar(3)s – Octet 2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Upstream base data rate- 32-TCPAM Minimum 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–62—Standard information field – 2BASE-TL - Upstream PMMS rates - NPar(3) coding – Octet 3

Bits								2BASE-TL upstream PMMS rates NPar(3)s – Octet 3
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Upstream base data rate- 32-TCPAM Maximum 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–63—Standard information field – 2BASE-TL - Upstream PMMS rates - NPar(3) coding – Octet 4

Bits								
8	7	6	5	4	3	2	1	2BASE-TL upstream PMMS NPar(3)s Octet 6
x	x	x	x	x	x	x	x	Upstream base data rate- 32-TCPAM Step 1 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

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Table 61B–64—Standard information field – 2BASE-TL - Upstream PMMS rates - NPar(3) coding – Octet j_6*4-3

Bits								2BASE-TL upstream PMMS NPar(3)s – Octet j_6*4-3
8	7	6	5	4	3	2	1	
x	x						x	Upstream base data rate- 32-TCPAM Minimum j_6 (bit 7)
x	x					x		Upstream base data rate- 32-TCPAM Maximum j_6 (bit 7)
x	x				x			Upstream base data rate- 32-TCPAM Step j_6 (bit 7)
x	x	x	x	x				Reserved for allocation by IEEE Std 802.3

Table 61B–65—Standard information field – 2BASE-TL - Upstream PMMS rates - NPar(3) coding – Octet j_6*4-2

Bits								2BASE-TL upstream PMMS rates NPar(3)s – Octet j_6*4-2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Upstream base data rate- 32-TCPAM Minimum j_6 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–66—Standard information field – 2BASE-TL - Upstream PMMS rates - NPar(3) coding – Octet j_6*4-1

Bits								2BASE-TL upstream PMMS rates NPar(3)s – Octet j_6*4-1
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Upstream base data rate- 32-TCPAM Maximum j_6 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

Table 61B–67—Standard information field – 2BASE-TL - Upstream PMMS rates - NPar(3) coding – Octet j_6*4

Bits								2BASE-TL upstream PMMS NPar(3)s Octet j_6*4
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Upstream base data rate- 32-TCPAM Step j_6 (bit 1-6)[a]

[a]Note that the rates are determined by combining (bit 7) and the 6-bits in this octet to create a 7-bit number.

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61B.3.2.3 Framing parameter codepoints

Tables 61B–68 through 61B–73 contain the level-3 codepoints specific to 2BASE-TL framing parameters.

Table 61B–68—Standard information field – 2BASE-TL - Downstream framing parameters - NPar(3) coding – Octet 1

Bits								2BASE-TL Downstream framing NPar(3)s – Octet 1
8	7	6	5	4	3	2	1	
x	x					x	x	Sync Word (bits 14 and 13)
x	x			x	x			Stuff Bits (bits 1 to 2)
		x	x					Reserved for allocation by IEEE Std 802.3

Table 61B–69—Standard information field – 2BASE-TL - Downstream framing parameters - NPar(3) coding – Octet 2

Bits								2BASE-TL Downstream framing NPar(3)s – Octet 2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Sync Word (bits 12 to 7)

Table 61B–70—Standard information field – 2BASE-TL - Downstream framing parameters - NPar(3) coding – Octet 3

Bits								2BASE-TL Downstream framing NPar(3)s – Octet 3
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Sync Word (bits 6 to 1)

Table 61B–71—Standard information field – 2BASE-TL - Upstream framing parameters - NPar(3) coding – Octet 1

Bits								2BASE-TL Upstream framing NPar(3)s – Octet 1
8	7	6	5	4	3	2	1	
x	x					x	x	Sync Word (bits 14 and 13)
x	x			x	x			Stuff Bits (bits 1 to 2)
		x	x					Reserved for allocation by IEEE Std 802.3

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Table 61B–72—Standard information field – 2BASE-TL - Upstream framing parameters - NPar(3) coding – Octet 2

Bits								2BASE-TL Upstream framing NPar(3)s – Octet 2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Sync Word (bits 12 to 7)

Table 61B–73—Standard information field – 2BASE-TL - Upstream framing parameters - NPar(3) coding – Octet 3

Bits								2BASE-TL Upstream framing NPar(3)s – Octet 3
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Sync Word (bits 6 to 1)

61B.4 Codepoints for 10PASS-TS

61B.4.1 Level-2 S field codepoints for 10PASS-TS

Table 61B–74 and Table 61B–75 contain the level-2 codepoints specific to 10PASS-TS.

Table 61B–74—Standard information field – 10PASS-TS NPar(2) coding – Octet 1

Bits								10PASS-TS NPar(2)s
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	1	Upstream use of 25–138 KHz band
x	x	x	x	x	x	1	x	Downstream use of 25–138 KHz band
x	x	x	x	x	1	x	x	Reserved for allocation by IEEE Std 802.3
x	x	x	x	1	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	x	1	x	x	x	x	Reserved for allocation by IEEE Std 802.3
x	x	1	x	x	x	x	x	G.997.1 - Clear EOC OAM
x	x	0	0	0	0	0	0	No parameters in this octet

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Table 61B–75—Standard information field – 10PASS-TS SPar(2) coding – Octet 1

Bits								
8	7	6	5	4	3	2	1	**10PASS-TS SPar(2)s**
x	x	x	x	x	x	x	1	Reserved for allocation by IEEE Std 802.3
x	x	x	x	x	x	1	x	Used bands in upstream[a]
x	x	x	x	x	1	x	x	Used bands in downstream[a]
x	x	x	x	1	x	x	x	IDFT/DFT size
x	x	x	1	x	x	x	x	Initial length of CE
x	x	1	x	x	x	x	x	MCM RFI bands[a]
x	x	0	0	0	0	0	0	No parameters in this octet

[a]The length of the corresponding NPar(3) field is variable and is a multiple of 4 octets. The length depends on the total number of bands to be specified.

61B.4.2 Level-3 S field codepoints for 10PASS-TS

61B.4.2.1 Used bands in upstream codepoints

Tables 61B–76 through 61B–79 contain the level-3 codepoints specific to 10PASS-TS Used bands in upstream.

Table 61B–76—Standard information field – Used bands in upstream NPar(3) coding – Octet 4n-3 (n = 1, 2, 3, 4, 5)

Bits								
8	7	6	5	4	3	2	1	**10PASS-TS Used bands in upstream NPar(3)s Octet 4n-3 (n = 1, 2, 3, 4, 5)**
x	x	x	x	x	x	x	x	End tone index of band n (bits 7 to 12)[a]

[a]n is the band index, starting from 1.

Table 61B–77—Standard information field – Used bands in upstream NPar(3) coding – Octet 4n-2 (n = 1, 2, 3, 4, 5)

Bits								
8	7	6	5	4	3	2	1	**10PASS-TS Used bands in upstream NPar(3)s Octet 4n-2 (n = 1, 2, 3, 4, 5)**
x	x	x	x	x	x	x	x	End tone index of band n (bits 1 to 6)[a]

[a]n is the band index, starting from 1.

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Table 61B–78—Standard information field – Used bands in upstream NPar(3) coding – Octet 4n-1 (n = 1, 2, 3, 4, 5)

Bits								10PASS-TS Used bands in upstream NPar(3)s Octet 4n-1 (n = 1, 2, 3, 4, 5)
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Start tone index of band n (bits 7 to 12)[a]

[a]n is the band index, starting from 1.

Table 61B–79—Standard information field – Used bands in upstream NPar(3) coding – Octet 4n (n = 1, 2, 3, 4, 5)

Bits								10PASS-TS Used bands in upstream NPar(3)s Octet 4n (n = 1, 2, 3, 4, 5)
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Start tone index of band n (bits 1 to 6)[a]

[a]n is the band index, starting from 1.

61B.4.2.2 Used bands in downstream codepoints

Table 61B–80 through Table 61B–83 contain the level-3 codepoints specific to 10PASS-TS Used bands in downstream.

Table 61B–80—Standard information field – Used bands in downstream NPar(3) coding – Octet 4n-3 (n = 1, 2, 3, 4, 5)

Bits								10PASS-TS Used bands in downstream NPar(3)s Octet 4n-3 (n = 1, 2, 3, 4, 5)
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	End tone index of band n (bits 7 to 12)[a]

[a]n is the band index, starting from 1.

Table 61B–81—Standard information field – Used bands in downstream NPar(3) coding – Octet 4n-2 (n = 1, 2, 3, 4, 5)

Bits								10PASS-TS Used bands in downstream NPar(3)s Octet 4n-2 (n = 1, 2, 3, 4, 5)
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	End tone index of band n (bits 1 to 6)[a]

[a]n is the band index, starting from 1.

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Table 61B–82—Standard information field – Used bands in downstream NPar(3) coding – Octet 4n-1 (n = 1, 2, 3, 4, 5)

Bits								10PASS-TS Used bands in downstream NPar(3)s Octet 4n-1 (n = 1, 2, 3, 4, 5)
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Start tone index of band n (bits 7 to 12)[a]

[a]n is the band index, starting from 1.

Table 61B–83—Standard information field – Used bands in downstream NPar(3) coding – Octet 4n (n = 1, 2, 3, 4, 5)

Bits								10PASS-TS Used bands in downstream NPar(3)s Octet 4n (n = 1, 2, 3, 4, 5)
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Start tone index of band n (bits 1 to 6)[a]

[a]n is the band index, starting from 1.

61B.4.2.3 IDFT/DFT size codepoints

Table 61B–84 contains the level-3 codepoints specific to 10PASS-TS IDFT/DFT size.

Table 61B–84—Standard information field – IDFT/DFT size NPar(3) coding – Octet 1

Bits								10PASS-TS IDFT/DFT size NPar(3)s Octet 1
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	IDFT/DFT size (bits 6-1 × 256 points)

61B.4.2.4 Initial length of CE codepoints

Table 61B–85 through Table 61B–86 contain the level-3 codepoints specific to 10PASS-TS Initial length of CE.

Table 61B–85—Standard information field – Initial length of CE NPar(3) coding – Octet 1

Bits								10PASS-TS Initial length of CE NPar(3)s Octet 1
8	7	6	5	4	3	2	1	
x	x	0	0	x	x	x	x	Initial sample length of cyclic extension (bits 7 to 10)

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Table 61B–86—Standard information field – Initial length of CE NPar(3) coding – Octet 2

Bits								10PASS-TS Initial length of CE NPar(3)s Octet 2
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Initial sample length of cyclic extension (bits 6-1)

61B.4.2.5 MCM RFI band codepoints

Table 61B–87 through Table 61B–90 contain the level-3 codepoints specific to 10PASS-TS MCM RFI bands.

Table 61B–87—Standard information field – MCM RFI bands NPar(3) coding – Octet 4n-3 (n = 1, 2, 3, 4, 5)

Bits								10PASS-TS MCM RFI bands NPar(3)s Octet 4n-3 (n = 1, 2, 3, 4, 5)
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	End tone index of band n (bits 7 to 12)[a]

[a]n is the band index, starting from 1.

Table 61B–88—Standard information field – MCM RFI bands NPar(3) coding – Octet 4n-2 (n = 1, 2, 3, 4, 5)

Bits								10PASS-TS MCM RFI bands NPar(3)s Octet 4n-2 (n = 1, 2, 3, 4, 5)
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	End tone index of band n (bits 1 to 6)[a]

[a]n is the band index, starting from 1.

Table 61B–89—Standard information field – MCM RFI bands NPar(3) coding – Octet 4n-1 (n = 1, 2, 3, 4, 5)

Bits								10PASS-TS MCM RFI bands NPar(3)s Octet 4n-1 (n = 1, 2, 3, 4, 5)
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Start tone index of band n (bits 7 to 12)[a]

[a]n is the band index, starting from 1.

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Table 61B–90—Standard information field – MCM RFI bands NPar(3) coding – Octet 4n (n = 1, 2, 3, 4, 5)

Bits								10PASS-TS MCM RFI bands NPar(3)s Octet 4n (n = 1, 2, 3, 4, 5)
8	7	6	5	4	3	2	1	
x	x	x	x	x	x	x	x	Start tone index of band n (bits 1 to 6)[a]

[a]n is the band index, starting from 1.

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61B.5 Protocol implementation conformance statement (PICS) proforma for Annex 61B, Handshake codepoints for 2BASE-TL and 10PASS-TS[285]

61B.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 61B, Handshake codepoints for 2BASE-TL and 10PASS-TS, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

61B.5.2 Identification

61B.5.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., names and versions for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

61B.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 61B, Handshake codepoints for 2BASE-TL and 10PASS-TS.
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

61B.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
HSCP	Handshake Codepoints	61B	The coding rules for 2BASE-TL handshake messages are implemented.	M	Yes [ ]

[285] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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61B.5.4 2BASE-TL handshake coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
HSCP-1	PMMS coding	61B.3.1	Values for min and max are between 4 and 89, inclusive.	M	Yes [ ]
HSCP-2	PMMS coding	61B.3.1	Valid values for step are between 1 and 89, inclusive.	M	Yes [ ]
HSCP-3	PMMS coding	61B.3.1	The variables j_5 and j_6 associated with the PMMS rates are independent, and range from 2 to 8, inclusive.	M	Yes [ ]
HSCP-4	PMMS coding	61B.3.1	If only one range of rates is required, then only the octets associated with (min1,max1,step1) are sent.	M	Yes [ ]
HSCP-5	CLR coding	61B.3.1	Valid values for minimum and maximum are between 3 and 60, inclusive, for 16-TCPAM and between 12 and 89, inclusive, for 32-TCPAM.	M	Yes [ ]
HSCP-6	CLR coding	61B.3.1	Valid values for step are between 1 and 89, inclusive.	M	Yes [ ]
HSCP-7	CLR coding	61B.3.1	The variables j_1, j_2, j_3 and j_4 associated with the training rates are independent, and range from 2 to 8, inclusive.	M	Yes [ ]
HSCP-8	CLR coding	61B.3.1	If only one range of rates is required, then only the octets associated with (min1,max1,step1) is sent. If more than one range of rates is required, then j_1*4, j_2*4, j_3*4 and j_4*4 correspond to the number of octets sent.	M	Yes [ ]
HSCP-9	CL coding	61B.3.1	Valid values for minimum and maximum are between 3 and 60, inclusive, for 16-TCPAM and between 12 and 89, inclusive, for 32-TCPAM.	M	Yes [ ]
HSCP-10	CL coding	61B.3.1	Valid values for step are between 1 and 89, inclusive.	M	Yes [ ]
HSCP-11	CL coding	61B.3.1	The variables j_1, j_2, j_3 and j_4 associated with the training rates are independent, and range from 2 to 8, inclusive.	M	Yes [ ]
HSCP-12	CL coding	61B.3.1	If only one range of rates is required, then only the octets associated with (min1,max1,step1) is sent. If more than one range of rates is required, then j_1*4, j_2*4, j_3*4 and j_4*4 correspond to the number of octets sent.	M	Yes [ ]
HSCP-13	SPar(2) coding	61B.3.1	Only one of the bits 2BASE-TL training mode and 2BASE-TL PMMS mode is set at any given time.	M	Yes [ ]
HSCP-14	SPar(2) coding	61B.3.1	The Regenerator silent period bit is set to 0_b if the 2BASE-TL PMMS mode NPar(2) bit is set to 1_b or the 2BASE-TL Training mode NPar(2) bit is set to 1_b.	M	Yes [ ]

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Annex 62A

(normative)

PMD profiles for 10PASS-TS

62A.1 Introduction and rationale

Annex 62A defines the PMD profiles for 10PASS-TS. These profiles define the transmission characteristics of the PHY on the media. 10PASS-TS PHYs are required to operate across varying media quality, regulatory and noise environments.

The profiles defined in this clause have two purposes. The first is to describe a bounded set of operating modes that a party might choose from when implementing, integrating and installing 10PASS-TS equipment. 10PASS-TS PHYs are inherently flexible in their transmission capabilities. The possible combination of transmission parameters are nearly infinite. The defined profiles collect a small subset of these parameters into modes that work well in most deployments. For deployments that require an operating mode not defined in this Annex, profiles can be overridden by setting PHY PMD registers directly, via Clause 45 for example. Informative Annex 62C contains examples of such user-defined modes of operation.

The second purpose of profiles is to define a set of operating modes against which PHY performance compliance may be tested. The topic of performance compliance is addressed for 10PASS-TS in Annex 62B.

62A.2 Relationship to other clauses

Clause 30 describes how the selection of Annex 62A profiles is exported to a management entity.

Clause 45 registers describe an optional mechanism for configuring a 10PASS-TS PHY to use a particular profile. The register settings for each profile are contained in 62A.4.

62A.3 Profile definitions

The following sections define the mandatory profiles for 10PASS-TS operation, in terms of bandplan, PSD mask, UPBO Reference PSD, notching parameters and payload rate.

62A.3.1 Bandplan and PSD mask profiles

The spectral characteristics of 10PASS-TS communication on the copper medium are defined by a choice of bandplans and PSD Masks.

Each of 5 standard frequency bands (Band 0, D1, U1, D2, U2) used for 10PASS-TS communication are defined in a bandplan. 10PASS-TS PHYs operating in the same cable bundle should use the same bandplan to ensure spectral compatibility. Furthermore, the selection of bandplan may be governed by regional regulations that pertain to the deployment. While all 10PASS-TS PHYs may operate in any of the below bandplans, installers should be aware of any regulations that might restrict their choice of modes. Bandplan profiles specify the use of 2, 3, 4, or 5 standard frequency bands.

PSD Masks further define the spectral environment by specifying the maximum transmit power spectral density at a given frequency. Like bandplans, the PSD mask should be selected to be compatible with applicable regulations and to match other PHYs operating in the same cable bundle.

Profiles are defined here for various regulatory environments as well as for private installation. Additionally, operation with a bandplan or PSD mask not defined in this clause is supported by configuration through Clause 45 registers. All 10PASS-TS PHYs shall be capable of operating in all profiles listed in this clause.

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Profile definitions are listed in Table 62A-1.
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Table 62A-1—Bandplan and PSD Mask Profiles

Profile Number	PSD Mask	Band Assignment[a]	Bandplan
1	ATIS-0600424 FTTCab.M1	x/D/U/D/U	G.993.1 Bandplan A
2	ATIS-0600424 FTTEx.M1		
3	ATIS-0600424 FTTCab.M2		
4	ATIS-0600424 FTTEx.M2		
5	ATIS-0600424 FTTCab.M1	D/D/U/D/U	
6	ATIS-0600424 FTTEx.M1		
7	ATIS-0600424 FTTCab.M2		
8	ATIS-0600424 FTTEx.M2		
9	ATIS-0600424 FTTCab.M1	U/D/U/D/x	
10	ATIS-0600424 FTTEx.M1		
11	ATIS-0600424 FTTCab.M2		
12	ATIS-0600424 FTTEx.M2		
13	TS1 101 270-1 Pcab.M1.A	x/D/U/D/U	G.993.1 Bandplan B
14	TS1 101 270-1 Pcab.M1.B		
15	TS1 101 270-1 Pex.P1.M1		
16	TS1 101 270-1 Pex.P2.M1		
17	TS1 101 270-1 Pcab.M2		
18	TS1 101 270-1 Pex.P1.M2		
19	TS1 101 270-1 Pex.P2.M2		
20	TS1 101 270-1 Pcab.M1.A	U/D/U/D/x	
21	TS1 101 270-1 Pcab.M1.B		
22	TS1 101 270-1 Pex.P1.M1		
23	TS1 101 270-1 Pex.P2.M1		
24	TS1 101 270-1 Pcab.M2		
25	TS1 101 270-1 Pex.P1.M2		
26	TS1 101 270-1 Pex.P2.M2		
27	G.993.1 F.1.2.1 (VDSL over POTS)	x/D/U/D/U	G.993.1 Annex F
28	G.993.1 F.1.2.2 (VDSL over TCM-ISDN)		
29	G.993.1 F.1.2.3 (PSD reduction)		
30	ATIS-0600424 FTTCab.M1 (extended)	x/D/U/D/U/D	G.993.1 Annex A[b]

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[a]For each band in the bandplan, the Band Assignment indicates the use or direction of communication for that band. U=upstream, D=downstream, x=band is unused. Bands are listed in this order: 0/1/2/3/4.
[b]This profile uses a 5th band (12 MHz—16.5 MHz) for downstream transmission at –60 dBm/Hz.

62A.3.2 Bandplan definitions

The management entity should load the appropriate Clause 45 registers according to the bandplan specified by the selected profile. 62A.4 contains examples of the use of Clause 45 registers for the purpose of setting profiles.

The VDSL bandplans defined in ITU-T Recommendation G.993.1 shall be supported by all 10PASS-TS PMDs. These bandplans are represented for information in Table 62A-2.

Table 62A-2—Bandplans defined by ITU-T Recommendation G.993.1

Plan	Band 0 (optional) US/DS	Band D1	Band U1	Band D2	Band U2
Bandplan A (formerly Plan 998)	25 kHz – 138 kHz	138 kHz – 3.75 MHz	3.75 Mhz – 5.2 MHz	5.2 MHz – 8.5 MHz	8.5 MHz – 12 MHz
Bandplan B (formerly Plan 997)	25 kHz – 138 kHz	138 kHz – 3.0 MHz	3.0 MHz – 5.1 MHz	5.2 MHz – 7.05 MHz	7.05 MHz – 12 MHz
Bandplan C[a]	25 kHz – 138 kHz	138 kHz – 2.5MHz	2.5 MHz – 3.75 MHz	3.75 MHz – *Fx*	*Fx* – 12MHz
Annex F[b,c]	25 kHz – 138 kHz	138 kHz – 3.75 MHz	3.75 Mhz – 5.2 MHz	5.2 MHz – 8.5 MHz	8.5 MHz – 12 MHz

[a]Bandplan C is characterized by a variable split frequency between band D2 and band U2, represented as "*Fx*". 10PASS-TS shall support operation in Bandplan C for $Fx = 3750\ \text{kHz} + n \times 250\ \text{kHz}$, where $0 \le n \le 33$.
[b]Subsets composed of at least one downstream band and one upstream band among D1, U1, D2 and U2 may be implemented.
[c]Band 1D starts at 640 kHz when operating in the frequency region above TCM-ISDN DSL band. Band 1D starts at 1.104 MHz when operating with PSD reduction function in the frequency region below 1.104 Mhz.

62A.3.3 PSD mask definitions

The management entity should load the appropriate Clause 45 registers according to the PSD Mask specified by the selected profile. 62A.4 contains examples of the use of Clause 45 registers for the purpose of setting profiles.

The VDSL PSD Masks defined in ITU-T Recommendation G.993.1, ATIS-0600424 and ETSI TS 101 270-1 shall be supported by all 10PASS-TS PMDs.

NOTE—The reference documents in which the PSD Masks are specified also specify the relationship between PSD Mask and PSD template, and the appropriate method to assess compliance with a PSD Mask or a PSD template.

62A.3.4 UPBO Reference PSD Profiles

Upstream Power Back-Off (UPBO) is defined in 62.3.4.1. Its operation requires the specification of a Reference PSD, by means of which the 10PASS-TS-R calculates the maximum upstream transmit PSD.

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Different UPBO Reference PSDs have been standardized in ATIS-0600424 and ETSI TS 101 270-1, as shown in Table 62A-3. 10PASS-TS implementations shall support all UPBO Reference PSDs listed in Table 62A-3. The 10PASS-TS PHY shall additionally allow a profile value of "0" to be selected, which indicates that UPBO is to be disabled.

Table 62A-3—UPBO Reference PSD Profiles
(*f* is in MHz, the PSD level is in dBm/Hz)

#	Reference PSD			1U	2U
1	ATIS-0600424	Noise A	M1	$-60-22.00\sqrt{f}$	$-60-17.18\sqrt{f}$
2			M2	$-53-24.47\sqrt{f}$	$-54-18.93\sqrt{f}$
3		Noise F	M1	$-60-18.54\sqrt{f}$	$-60-16.865\sqrt{f}$
4			M2	$-53-21.19\sqrt{f}$	$-54-18.69\sqrt{f}$
5	ETSI TS 101 270-1	Noise A&B		$-47.3-28.01\sqrt{f}$	$-54-19.22\sqrt{f}$
6		Noise C		$-47.3-21.14\sqrt{f}$	$-54-16.29\sqrt{f}$
7		Noise D		$-47.3-26.21\sqrt{f}$	$-54-17.36\sqrt{f}$
8		Noise E		$-47.3-27.27\sqrt{f}$	$-54-18.1\sqrt{f}$
9		Noise F		$-47.3-19.77\sqrt{f}$	$-54-15.77\sqrt{f}$

62A.3.5 Band Notch Profiles

In certain deployments, 10PASS-TS operation may interfere with nearby amateur radio equipment. The Band Notch profiles specify notches that 10PASS-TS PHYs shall add to their transmit PSDs when selected. When a notch is activated, the transmitter shall reduce its PSD to less than –80 dBm/Hz in the frequencies of the notch. More than one notch may be activated at one time.

All Band Notches specified in the following standards shall be supported:

a) ITU-T Recommendation G.993.1 Annex F, Table F-5
b) ATIS-0600424, Annex A
c) ETSI TS1 101 270 subclause 9.3.3.6.1

The Band Notch Profiles are listed for information in Table 62A-4. This table includes notches that are above 12MHz, that are therefore outside the scope of this standard.

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Table 62A-4—Band Notch Profile definitions

Band Notch Profile	Specification			Start Frequency (MHz)	End Frequency (MHz)
	ITU-T Rec. G.993.1	ATIS-0600424.2004 (S2015)	TS 101 270-1		
1	Table F-5 #01	—	—	1.810	1.825
2	Table 6-2	Table A.1	Table 17	1.810	2.000
3	Table F-5 #02	—	—	1.9075	1.9125
4	Table F-5 #03	—	—	3.500	3.575
5	Table 6-2	—	Table 17	3.500	3.800
6	—	Table A.1	—	3.500	4.000
7	Table F-5 #04	—	—	3.747	3.754
8	Table F-5 #05	—	—	3.791	3.805
9	Table 6-2	—	Table 17	7.000	7.100
10	Table F-5 #06	Table A.1	—	7.000	7.300
11	Table 6-2	Table A.1	Table 17	10.100	10.150
—	Table 6-2 Table F-5 #08	Table A.1	Table 17	14.000	14.350
—	Table 6-2 Table F-5 #09	Table A.1	Table 17	18.068	18.168
—	Table 6-2 Table F-5 #10	Table A.1	Table 17	21.000	21.450
—	Table 6-2 Table F-5 #11	Table A.1	Table 17	24.890	24.990
—	Table 6-2	—	Table 17	28.000	29.100
—	Table F-5 #12	Table A.1	—	28.000	29.700

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62A.3.6 Payload rate profiles

The Payload Rate Profile describes the payload bitrate as seen at the MII interface.

The Payload Rate Profile consists of a payload rate for each of the downstream and upstream directions. The profile is specified in the format Drate/Urate as the payload bitrate that the PHY link shall provide, where *Drate* and *Urate* are expressed in Mb/s. For example a Payload Rate Profile of 10/2.5 corresponds to a downstream payload rate of 10 Mb/s and an upstream payload rate of 2.5 Mb/s. *Drate* values of 2.5, 5, 7.5, 10, 12.5, 15, 25, 35, 50, 70, and 100 shall be supported where the loop environment, bandplan and PSD mask allow this. *Urate* values of 2.5, 5, 7.5, 10, 12.5, 15, 25, 35, and 50 shall be supported where the loop environment, bandplan and PSD mask allow this. This leads to a total of 9 symmetric and 90 asymmetric Payload Rate Profiles.

The selected Payload Rate Profile sets a target for the PHY's operation. If the payload rates of the selected profile cannot be achieved based on the loop environment, bandplan and PSD mask, the PHY shall drop the link.

62A.3.7 Complete profiles

The complete PMD operation of the 10PASS-TS PHY can be selected by choosing one Bandplan and PSD Mask profile, one UPBO Reference PSD profile, one Payload Rate profile, and any number of Band Notch profiles.

62A.3.8 Default profile

A 10PASS-TS device that is not managed (i.e., no management functions are provided, or enabled) shall operate in the default profile and the default mode specified in this subclause and summarized in Table 62A-5.

Table 62A-5—Default profile and default mode settings

Profile / Setting	Value
Payload bitrate profile	10/10
Bandplan and PSD mask profile	#1
Band notch profiles	#2, #6, #10, and #11
UPBO reference PSD profile	#3
Reed-Solomon setting	(240, 224)
Interleaver setting	I=30, M=62

The default profile shall consist of the 10/10 payload bitrate profile, bandplan and PSD mask profile #1, band notch profiles #2, #6, #10, and #11 enabled, and UPBO reference PSD profile #3.

In addition, the default mode of 10PASS-TS implementations shall use Reed-Solomon setting (240, 224)[286], and interleaver setting I=30, M=62.

NOTE—The default profile may not be spectrally compatible to any particular regional requirement, nor may it be the optimal profile for a particular cable segement.

[286]See 62.2.4.2.

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62A.4 Register settings

Tables 62A-6 through 62A-8 contain the register settings required to implement the profiles described in this Annex. The referenced registers are defined in 45.2.

Table 62A-6 contains the MCM tone group definitions to be used in order to support the band plan profiles described in 62A.3.2. For each of the listed tone groups, the Tone Active and/or Tone Direction bits in the 10P MCM tone control parameter register shall be set according to the use indicated in the first column of the table.

Table 62A-6—MCM register settings implementing bandplan profiles

Band Allocation	Band Plan A 10P MCM Tone Group Register		Band Plan B 10P MCM Tone Group Register		Band Plan C 10P MCM Tone Group Register		Band Plan Ann. F 10P MCM Tone Group Register	
	lower	upper	lower	upper	lower	upper	lower	upper
0 (upstream, downstream or not used)	0007_{16}	$001F_{16}$	0007_{16}	$001F_{16}$	0007_{16}	$001F_{16}$	0007_{16}	$001F_{16}$
1D (downstream)	0021_{16}	0365_{16}	0021_{16}	$02B7_{16}$	0021_{16}	0243_{16}	0021_{16}	0365_{16}
1U (upstream)	0367_{16}	$04B5_{16}$	$02B9_{16}$	$049E_{16}$	0245_{16}	0365_{16}	0367_{16}	$04B5_{16}$
2D (downstream)	$04B7_{16}$	$07B2_{16}$	$04A0_{16}$	0662_{16}	0367_{16}	fx1[a]	$04B7_{16}$	$07B2_{16}$
2U (upstream)	$07B4_{16}$	$0ADE_{16}$	0664_{16}	$0ADE_{16}$	fx2[b]	$0ADE_{16}$	$07B4_{16}$	$0ADE_{16}$
3D (downstream)[c]	$0ADF_{16}$	$0EF2_{16}$	—	—	—	—	—	—

[a]Values for fx1 shall be in the range 0369_{16} to $0ADA_{16}$
[b]Values for fx2 shall be in the range (fx1 + 2) to $0ADE_{16}$
[c]Band 3D is only used in Band Plan and PSD Mask profile #30.

Unlike the other parameters governed by the profiles specified in the Annex, PSDs are typically defined by means of a functional expression, rather than a set of values. Transmit PSDs and Reference PSDs typically vary for each individual tone. A pseudo-C procedure for setting a PSD profile and a Reference PSD profile is shown in Equation (62A–1) below. It assumes the existence of the functions getPSDLevel(float frequencyInKHz) and getReferencePSD(float frequencyInKHz) specifying the transmit PSD and Reference PSD respectively, both expressed as a floating-point value in dBm/Hz. Registers are addressed by means of pointers ToneGroupRegister, ToneControlParameterRegister and ToneControlActionRegister.

```
for (int tone=0;tone<4096;tone++) {
 ToneGroupRegister[0] = tone;                // set lower bound of tone group
 ToneGroupRegister[1] = tone;                // set upper bound of tone group
                                             // to the same value
 short TxPSD = floor(4*(getPSDLevel(tone*4.3125)+100)) & 0x01FF;
                                             // convert to 9-bit value
 ToneControlParameterRegister[1] &= 0xFFFC;  // clear first two bits of PSD level
 ToneControlParameterRegister[2] &= 0x01FF;  // clear remaining 7 bits of PSD level
 ToneControlParameterRegister[1] |= TxPSD >> 7;// store first two bits of PSD level
 ToneControlParameterRegister[2] |= (TxPSD << 9) & 0xFE00;
                                             // store remaining 7 bits of PSD level
 short RefPSD = floor(4*(getReferencePSD(tone*4.3125)+100)) & 0x01FF;
                                             // convert to 9-bit value
 ToneControlParameterRegister[2] &= 0xFFE0;  // clear Reference PSD level
 ToneControlParameterRegister[2] |= RefPSD;  // store Reference PSD level
 *ToneControlActionRegister |= 0x0020;       // refresh contents of the selected
                                             // tones entries in table
}
*ToneControlActionRegister |= 0x0002;        // activates PSD level setting as in
                                             // ToneControlParameterRegister
*ToneControlActionRegister |= 0x0001;        // activates UPBO Ref. PSD level
                                             // setting as in
                                             // ToneControlParameterReg          (62A–1)
```


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Functions specifying standard transmit PSDs can be found in the documents referenced in 62A.3.3. Functions specifying UPBO Reference PSDs can be found in Table 62A-3.

Table 62A-7 contains the MCM tone group definitions to be used in order to support the band notch profiles described in 62A.3.5. For each of the listed tone groups, the Tone Active bit in the 10P MCM tone control parameter register shall be cleared to activate the corresponding band notch.

Table 62A-7—MCM register settings implementing band notch profiles

Band Notch Profile	10P MCM Tone Group Register	
	lower	upper
1	$01A3_{16}$	$01A7_{16}$
2	$01A3_{16}$	$01D0_{16}$
3	$01B9_{16}$	$01BB_{16}$
4	$032B_{16}$	$033D_{16}$
5	$032B_{16}$	0371_{16}
6	$032B_{16}$	$03A0_{16}$
7	0364_{16}	0366_{16}
8	$036E_{16}$	0372_{16}
9	0656_{16}	$066E_{16}$
10	0656_{16}	$069D_{16}$
11	0925_{16}	0932_{16}

Table 62A-8 contains the MCM register settings for the payload rate profiles listed in 62A.3.6. When operating under a payload rate profile, the minimum and maximum data rates in the 10P MCM upstream/ downstream data rate configuration registers shall be set to the same value.

Table 62A-8—MCM register settings implementing payload rate profiles

Profile (payload rate in Mb/s)	Downstream Data Rate Configuration Register setting (bits 15:0)	Upstream Data Rate Configuration Register setting (bits 15:0)
2.5	0027_{16}	0027_{16}
5	$004E_{16}$	$004E_{16}$
7.5	0075_{16}	0075_{16}
10	$009C_{16}$	$009C_{16}$
12.5	$00C3_{16}$	$00C3_{16}$
15	$00EA_{16}$	$00EA_{16}$
25	0186_{16}	0186_{16}
35	0222_{16}	0222_{16}
50	$030D_{16}$	$030D_{16}$
70	0445_{16}	no profile defined
100	$061A_{16}$	no profile defined

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62A.5 Protocol implementation conformance statement (PICS) proforma for Annex 62A, PMD profiles for 10PASS-TS[287]

62A.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 62A, PMD profiles for 10PASS-TS, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

62A.5.2 Identification

62A.5.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., names and versions for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

62A.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 62A, PMD profiles for 10PASS-TS.
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

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62A.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
10PProf	PMD profiles for 10PASS-TS	Annex 62A	The PMD profiles listed in Annex 62A are supported.	10PASS-TS: M	Yes [ ]

62A.5.4 PICS proforma tables for PMD profiles for 10PASS-TS

Item	Feature	Subclause	Value/Comment	Status	Support
10PProf-1	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHYs is capable of operating in all profiles listed in this Clause.	M	Yes [ ]
10PProf-2	Bandplan and PSD mask profiles	62A.3.1	The VDSL bandplans defined in ITU-T Recommendation G.993.1 are supported.	M	Yes [ ]
10PProf-3	Bandplan and PSD mask profiles	62A.3.1	The VDSL PSD Masks defined in ITU-T Recommendation G.993.1, ATIS-0600424 and ETSI TS 101 270-1 are supported by all 10PASS-TS PMDs.	M	Yes [ ]
10PProf-4	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #1 as specified in Table 62A-1.	M	Yes [ ]
10PProf-5	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #2 as specified in Table 62A-1.	M	Yes [ ]
10PProf-6	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #3 as specified in Table 62A-1.	M	Yes [ ]
10PProf-7	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #4 as specified in Table 62A-1.	M	Yes [ ]
10PProf-8	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #5 as specified in Table 62A-1.	M	Yes [ ]
10PProf-9	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #6 as specified in Table 62A-1.	M	Yes [ ]
10PProf-10	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #7 as specified in Table 62A-1.	M	Yes [ ]
10PProf-11	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #8 as specified in Table 62A-1.	M	Yes [ ]
10PProf-12	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #9 as specified in Table 62A-1.	M	Yes [ ]
10PProf-13	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #10 as specified in Table 62A-1.	M	Yes [ ]

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10PProf-14	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #11 as specified in Table 62A-1.	M	Yes [ ]
10PProf-15	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #12 as specified in Table 62A-1.	M	Yes [ ]
10PProf-16	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #13 as specified in Table 62A-1.	M	Yes [ ]
10PProf-17	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #14 as specified in Table 62A-1.	M	Yes [ ]
10PProf-18	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #15 as specified in Table 62A-1.	M	Yes [ ]
10PProf-19	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #16 as specified in Table 62A-1.	M	Yes [ ]
10PProf-20	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #17 as specified in Table 62A-1.	M	Yes [ ]
10PProf-21	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #18 as specified in Table 62A-1.	M	Yes [ ]
10PProf-22	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #19 as specified in Table 62A-1.	M	Yes [ ]
10PProf-23	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #20 as specified in Table 62A-1.	M	Yes [ ]
10PProf-24	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #21 as specified in Table 62A-1.	M	Yes [ ]
10PProf-25	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #22 as specified in Table 62A-1.	M	Yes [ ]
10PProf-26	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #23 as specified in Table 62A-1.	M	Yes [ ]
10PProf-27	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #24 as specified in Table 62A-1.	M	Yes [ ]
10PProf-28	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #25 as specified in Table 62A-1.	M	Yes [ ]
10PProf-29	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #26 as specified in Table 62A-1.	M	Yes [ ]
10PProf-30	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #27 as specified in Table 62A-1.	M	Yes [ ]

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10PProf-31	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #28 as specified in Table 62A-1.	M	Yes [ ]
10PProf-32	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #29 as specified in Table 62A-1.	M	Yes [ ]
10PProf-33	Bandplan and PSD mask profiles	62A.3.1	The 10PASS-TS PHY is capable of operating in profile #30 as specified in Table 62A-1.	M	Yes [ ]
10PProf-34	UPBO Reference PSD Profiles	62A.3.4	The implementation supports all UPBO Reference PSDs listed in Table 62A-3.	M	Yes [ ]
10PProf-35	Band Notch Profiles	62A.3.5	The 10PASS-TS PHY adds the notches specified by the band notch profile to their transmit PSDs when selected.	M	Yes [ ]
10PProf-36	Band Notch Profiles	62A.3.5	When a notch is activated, the transmitter reduces its PSD to less than -80 dBm/Hz in the frequencies of the notch.	M	Yes [ ]
10PProf-37	Band Notch Profiles	62A.3.5	All Band Notches specified in the following standards are supported: -ITU-T Recommendation G.993.1 Annex F, Table F-5 -ATIS-0600424.2004 (S2015), Annex A -ETSI TS1 101 270 subclause 9.3.3.6.1	M	Yes [ ]
10PProf-38	Payload rate profiles	62A.3.6	Drate values of 2.5, 5, 7.5, 10, 12.5, 15, 25, 35, 50, 70, and 100 are supported where the loop environment, bandplan and PSD mask allow this.	M	Yes [ ]
10PProf-39	Payload rate profiles	62A.3.6	Urate values of 2.5, 5, 7.5, 10, 12.5, 15, 25, 35, and 50 are supported where the loop environment, bandplan and PSD mask allow this.	M	Yes [ ]
10PProf-40	Payload rate profiles	62A.3.6	If the payload rates of the selected profile cannot be achieved based on the loop environment, bandplan and PSD mask, the PHY drops the link.	M	Yes [ ]
10PProf-41	Default profile	62A.3.8	A 10PASS-TS device that is not managed operates in the default profile and the default mode specified in 62A.3.8 and summarized in Table 62A-5.	M	Yes [ ]

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10PProf-42	Register settings	62A.4	For each of the listed tone groups, the Tone Active and/or Tone Direction bits in the 10P MCM tone control parameter register are set according to the use indicated in the first column of Table 62A-6.	M	Yes [ ]
10PProf-43	Register settings	62A.4	For each of the listed tone groups, the Tone Active bit in the 10P MCM tone control parameter register are cleared to activate the corresponding band notch.	M	Yes [ ]
10PProf-44	Register settings	62A.4	When operating under a payload rate profile, the minimum and maximum data rates in the 10P MCM upstream/ downstream data rate configuration registers are set to the same value.	M	Yes [ ]

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Annex 62B

(normative)

Performance guidelines for 10PASS-TS PMD profiles

62B.1 Introduction and rationale

Annex 62B defines performance guidelines for 10PASS-TS PMD profiles. The definition of these guidelines is challenging due to the varying nature of the access network. The access network has large variations in cable characteristics from region to region. In addition, the make-up of a cable can encompass multiple cable gauges and/or different configuration of bridged taps. Finally, services may vary from region to region creating different noise scenarios. Typically, deployment guidelines are a function of the telecommunications operator, which is operating a loop and the regional spectrum management policies, which govern deployment on that loop.

Given that one cannot test every possible combination of loop make-up and noise conditions, the performance guidelines are covered from two perspectives. Firstly, 62B.3 lists a suite of artificial tests crafted to test the 10PASS-TS PHYs under representative worst-case noise and loop conditions. Secondly, 62B.4 defines a deployment guideline rule which allows a service provider to determine whether a given loop will support a given profile.

62B.2 Relationship to other clauses

Annex 62A lists a set of PMD profiles for 10PASS-TS. Clause 30 describes how the selection of Annex 62A profiles is exported to a management entity. Clause 45 registers describe an optional mechanism for configuring a 10PASS-TS PHY to use a particular profile. The register settings for each profile are contained in 62A.4.

62B.3 Performance test cases

The performance test cases are derived from the standard definition of test loops in ATIS-0600424.2004(S2015), section 12.1, the noise models are defined in ATIS-0600424.2004(S2015), section 12.2 and the profiles are defined in 62A.3.1. In all cases the PHYs shall attain link in the specified profile in the presence of noise and impairments and maintain link with a Bit Error Ratio less than 10^{-7} with the noise raised by 6dB.

During the test the PHY shall meet the requirements of the bandplan, PSD and Upstream Power Back Off (where appropriate) specified. The control of the profile shall be through the Clause 30 MIB if supported. If the PHY under test includes any implementation options defined in the reference document (but out of scope for this standard) these options shall be disabled in such a manner as to render the behavior identical to implementations without such options.

If a PHY is capable of operating as both CO-subtype and CPE-subtype then both modes of operation shall be tested. If the PHY is capable of supporting PME aggregation then each PME shall be capable of passing the performance tests independently.

Table 62B-1 lists the performance test cases. The test loops are described in ATIS-0600424.2004(S2015), section 12.1. For tests using test loop “VDSL1” the table specifies which of the two cable types (TP1 or TP2) is used. The length value refers to the dimension “x”, “y”, “z”, “u” or “v” depending on the test loop. If “notch” is specified to be “on” then the RF notches specified in ATIS-0600424.2004 (S2015)/Trial-Use, part 1, Annex 1 are applied as described in section 13.3.3. If “UPBO” is specified to be “on” then the Power Back Off specified in 62.3.4.4 is applied. The noise model applied will be noise model “A” or “F” as

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described in ATIS-0600424.2004(S2015), section 12.2.1.1. The definition of self crosstalk is in section 12.2.1.4.1.

Table 62B-1—Test cases for 10PASS-TS

Test	Test Loop	L (m)	Profile	Payload Data Rate down/up (Mb/s)	Notch	UPBO	Noise Model[a]
1	TP1	750	13	10/10	—	5	AWGN
2	TP2	750	13	10/10	—	5	ETSI A
3	TP2	300	1	10/10	—	1	ATIS-0600424 A
4	TP2	200	16	50/50	—	—	AWGN
5	TP2	100	16	35/25	—	—	self
6	TP1	650	6	25/5	—	—	self
7	TP2	700	17	15/15	—	—	self
8	TP1	1000	8	15/2.5	—	—	self
9	TP2	400	4	12.5/12.5	—	—	self
10	TP2	750	4	7.5/7.5	—	—	self
11	TP2	1000	23	5/5	—	—	self
12	TP2	1200	23	2.5/2.5	—	—	self
13	TP2	150	16	50/50	2, 5, 9, 11	—	AWGN
14	TP2	100	16	35/25	2, 5, 9, 11	—	self
15	TP1	650	6	25/5	2, 6, 10, 11	—	self
16	TP2	600	17	15/15	2, 5, 9, 11	—	self
17	TP1	1000	8	15/2.5	2, 6, 10, 11	—	self
18	TP2	400	4	12.5/12.5	2, 6, 10, 11	—	self
19	TP2	750	4	7.5/7.5	2, 6, 10, 11	—	self
20	TP2	900	23	5/5	2, 5, 9, 11	—	self
21	TP2	1200	23	2.5/2.5	2, 5, 9, 11	—	self
22	TP2	150	30	100/25	—	—	AWGN

[a]"AWGN" means that only white gaussian noise at -140 dBm/Hz is present. "Self" means that the equivalent crosstalk generated by 20 10PASS-TS transceivers operating in the same mode (assuming the same loop length and the same UPBO configuration) as the device under test is present in addition to white gaussian noise at -140 dBm/Hz. "ATIS-0600424 A" means that alien crosstalk according to ATIS-0600424 Noise Model A is present in addition to white gaussian noise at –140 dBm/Hz. "ETSI A" means that alien crosstalk according to ETSI TS 101 270-1 Noise Model A is present in addition to white gaussian noise. Self crosstalk and alien crosstalk are not to be applied simultaneously.

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62B.3.1 Additional tests

Additional testing to prove the requirements for link establishment, UPBO, burst noise immunity, link state and error reporting, etc. may be performed using any test scenarios from Table 62B-1.

62B.4 Deployment guidelines

The relationship between specific cable parameters and performance is complex and cannot be guaranteed. The performance tests described in section 62B.3 are designed to ensure that compliant PHYs will achieve a similar level of performance when applied in similar environments. The tests are designed to represent realistic worst case conditions but real world installations may sometimes experience worse performance for apparently similar conditions.

Annex A of ETSI TS1 101 270-1 (1999) contains some additional information regarding performance expectations related to cable parameters.

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62B.5 Protocol implementation conformance statement (PICS) proforma for Annex 62B, Performance guidelines for 10PASS-TS PMD profiles[288]

62B.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 62B, Performance guidelines for 10PASS-TS PMD profiles, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

62B.5.2 Identification

62B.5.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., names and versions for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

62B.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 62B, Performance guidelines for 10PASS-TS PMD profiles.
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

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62B.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
10PPerf	Performance guidelines for 10PASS-TS PMD profiles	Annex 62B	The performance guidelines listed in Annex 62B are supported.	10PASS-TS: M	Yes [ ]

62B.5.4 PICS proforma tables for Performance guidelines for 10PASS-TS PMD profiles

Item	Feature	Subclause	Value/Comment	Status	Support
10PPerf-1	Performance test cases	62B.3	In all cases the PHY attains link in the specified profile in the presence of noise and impairments and maintains link with a Bit Error Ratio less than 10^{-7} with the noise raised by 6dB.	M	Yes [ ]
10PPerf-2	Performance test cases	62B.3	During the test the PHY meets the requirements of the bandplan, PSD and Upstream Power Back Off specified.	M	Yes [ ]
10PPerf-3	Performance test cases	62B.3	The control of the profile is through the Clause 30 MIB if supported.	MDIO: M	Yes [ ] No [ ]
10PPerf-4	Performance test cases	62B.3	If the PHY under test includes any implementation options defined in the reference document these options are disabled in such a manner as to render the behavior identical to implementations without such options.	M	Yes [ ]
10PPerf-5	Performance test cases	62B.3	If a PHY is capable of operating as both CO-subtype and CPE-subtype then both modes of operation are tested.	M	Yes [ ]
10PPerf-6	Performance test cases	62B.3	If the PHY is capable of supporting PME aggregation then each PME is capable of passing the performance tests independently.	M	Yes [ ]

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Annex 62C

(informative)

10PASS-TS Examples

62C.1 Introduction

Annex 62A contains profiles for deployment of 10PASS-TS in typical environments, as well as for testing purposes. Certain situations may require the full use of the 10PASS-TS PHY's flexibility, going beyond what is offered by the predefined profiles, in order to obtain optimal performance. Examples of such circumstances:

a) the 10PASS-TS system shares a cable bundle with a legacy system; the PSD mask can be configured to minimize crosstalk between 10PASS-TS and the legacy system
b) for a specific application, a particular symmetry ratio is required, which is not easily obtained with the standard band plans
c) the desired payload bit rates are beyond the ones that can be set by means of the standard payload rate profiles
d) other unanticipated situations

To use this flexibility, the 10PASS-TS equipment is configured by means of the appropriate Clause 45 registers. This Annex provides examples of such configurations.

62C.2 Bandplan configuration

Example situation: a user wishes to implement a custom bandplan for a 10PASS-TS deployment in a private network, in order to minimize near-end crosstalk to and from a certain legacy system.

Band plans can be configured by selecting any group of tones in the Tone Group register (45.2.1.53), and allocating them to either upstream or downstream by setting the tone direction bit to the appropriate value (0 = downstream, 1 = upstream) in the Tone Control Parameter register (45.2.1.54). This procedure is repeated until the desired number of frequency bands has been allocated. The new configuration is applied by writing binary 1 to the Change Tone Direction bit in the Tone Control Action register (45.2.1.55).

An example of a custom bandplan and PSD is shown in Figure 62C–1 (the solid line represents the upstream PSD, the dashed line represents the downstream PSD). The overall transmission power is assumed to be 14.5 dBm in either direction which is similar to the ATIS-0600424 M2 mask and SHDSL transmit power. The example defined here is such that it should meet VDSL compatibility requirements for up to 1524 m (5000 ft).

The example PSD was tested for spectral compatibility with existing VDSL systems using ITU-T Bandplan A (formerly known as plan 998). The spectral compatibility guideline was obtained by assuring that the new service will not disturb the guaranteed data rates for VDSL basis system as shown in Table 62C–1.

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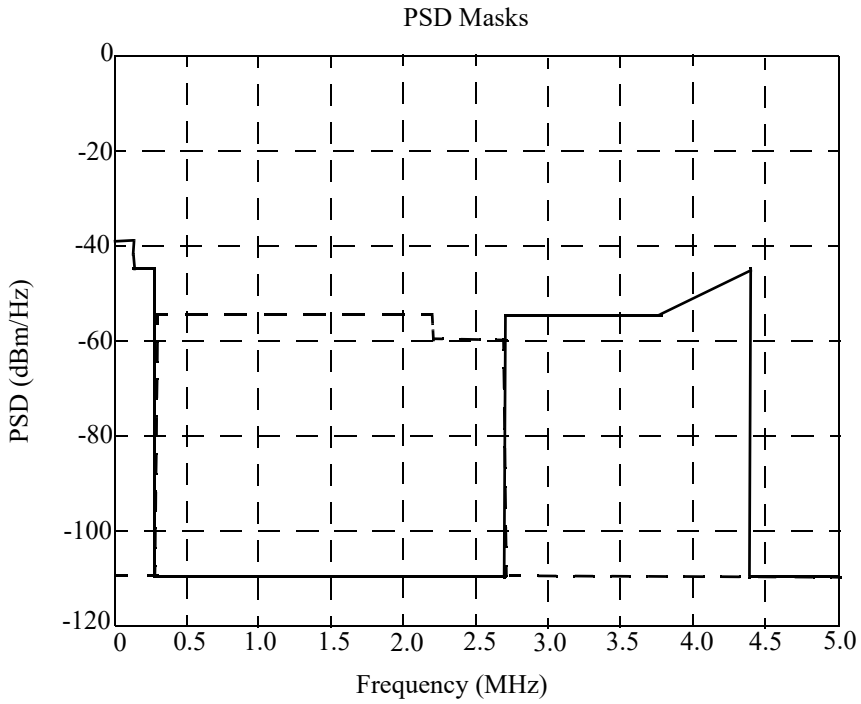

Figure 62C–1—Example PSD Masks for MCM 10PASS-TS

Table 62C–1—Required VDSL performance for spectral compatibility

Performance Level	Loop length (m)[a]	Upstream (Mb/s)	Downstream (Mb/s)
A	152.4	15.66	42.29
B	304.8	14.01	42.29
C	457.2	12.86	38.85
D	609.6	11.97	36.29
E	762.0	9.08	32.5
F	914.4	5.47	26.3
G	1066.8	3.66	22.12
H	1219.2	1.65	18.70
I	1371.6	0.42	15.40
J	1524.0	0.074	11.67

[a]NOTE—The performance requirements are taken from ATIS-0600417, which specifies loop lengths in 500 ft (152.4 m) increments.

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The results of the spectral compatibility analysis are shown in Figures 62C–1 through 62C–4.

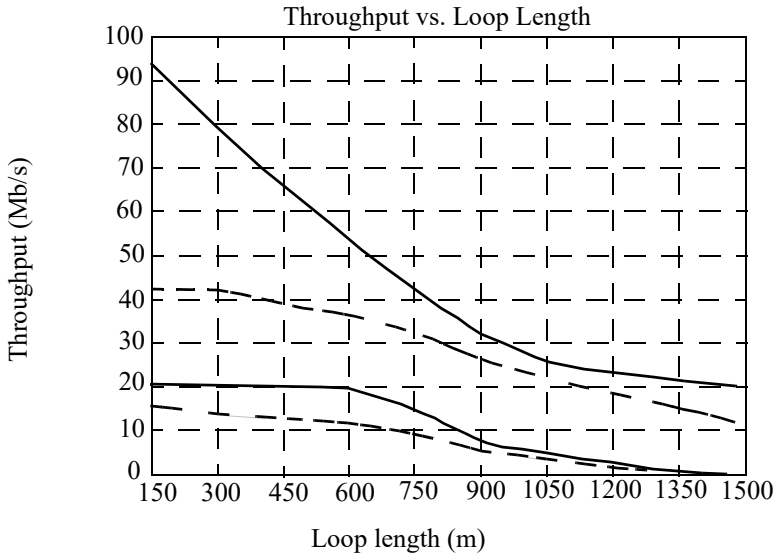

Figure 62C–2—Simulated performance of a VDSL system (using ITU-T Bandplan A) in the presence of 24 disturbers using the example PSD of this subclause.

NOTE—Dashed line = minimum VDSL performance required for spectral compatibility; solid line = simulated VDSL performance in presence of new disturbers.

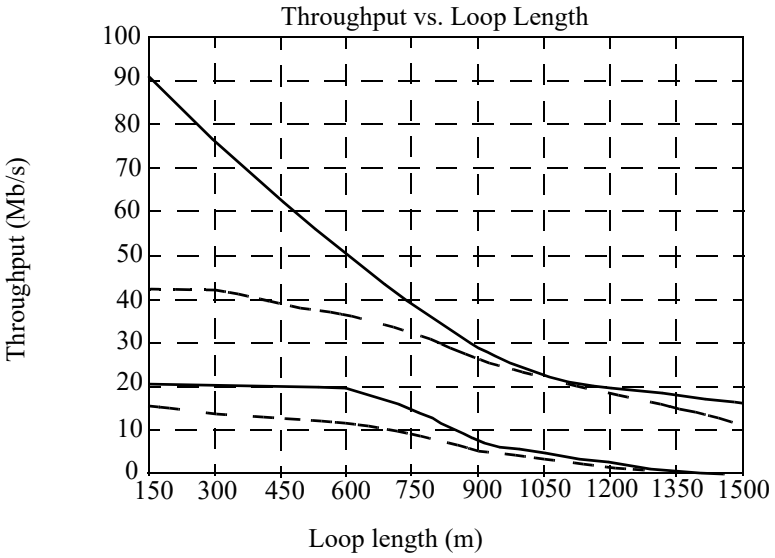

Figure 62C–3—Simulated performance of a VDSL system (using ITU-T Bandplan A) in the presence of 12 disturbers using the example PSD of this subclause and 12 disturbers using ATIS-0600417 mask SM class 9.

NOTE—Dashed line = minimum VDSL performance required for spectral compatibility; solid line = simulated VDSL performance in presence of new disturbers.

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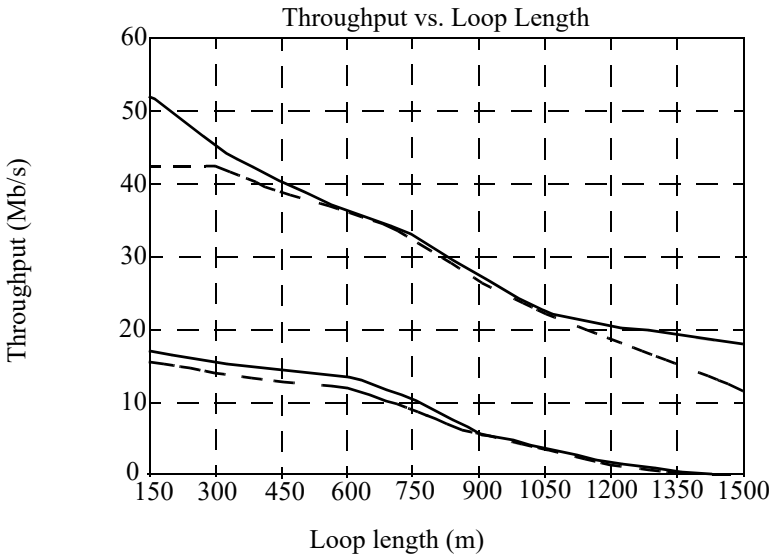

Figure 62C–4—Simulated performance of a VDSL system (using ITU-T Bandplan A) in the presence of 12 disturbers using the example PSD of this subclause and 12 disturbers using ATIS-0600417 mask SM class 6.

NOTE—Dashed line = minimum VDSL performance required for spectral compatibility; solid line = simulated VDSL performance in presence of new disturbers.

62C.2.1 Plan A with variable LF region

As an additional example, this subclause describes a modified version of ITU-T Bandplan A (formerly known as 998) with variable low-frequency region. Its target is to improve the reach of symmetric bitrates using 10PASS-TS or VDSL.

Plan A with variable LF region is shown in Figure 62C–5. The transition frequency between band 0 (used in upstream) and band 1D can be varied between 25 kHz and 490 kHz to boost the upstream channel bitrate. This principle is similar to the variable bandwidth capability of 2BASE-TL and SHDSL. A supporting PSD which observes spectral compatibility requirements is described in 62C.3.2.

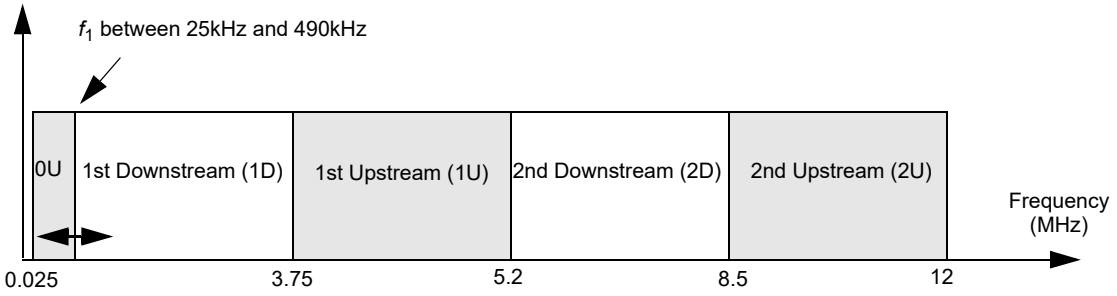

Figure 62C–5—Plan A with variable LF region

This family of bandplans can be implemented by assigning the appropriate tones to upstream and downstream, as shown in Table 62C–2.

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Table 62C–2—Implementation of Plan A with variable LF region

Band	Tone Group
0 (upstream)	$6 \rightarrow \lfloor f_1/(4.3125\text{kHz}) \rfloor$
1D (downstream)	$\lceil f_1/(4.3125\text{kHz}) \rceil \rightarrow 869$
1U (upstream)	$870 \rightarrow 1205$
2D (downstream)	$1206 \rightarrow 1970$
2U (upstream)	$1972 \rightarrow 2782$

62C.3 PSD mask configuration

62C.3.1 General procedure

Example situation: a mixed (transitional) deployment where certain subscribers are served with a 10PASS-TS line from a central office (longer lines), while others are served with a 10PASS-TS line from a cabinet (shorter lines). In order to guarantee high link quality for all subscribers, the transmit PSDs from the cabinet are reduced to mimic a longer line (downstream power back-off).

The properties of the different tones are configured by means of the Tone Group register (1.x.15:0; 1.x + 1.15:0, defined in 45.2.1.53). The 8-bit PSD Level field in the Tone Control Parameter register (45.2.1.54) is used to set the TX PSD level for the selected group of tones. Given the tone spacing of 4.3125 kHz, a very fine-grained PSD control is possible. To implement a gradual frequency-dependent power back-off, a narrow sliding window is defined in the Tone Group register; each time the window is moved towards higher frequencies, the allowed TX PSD for that frequency range is set. The new configuration is applied by writing binary 1 to the Change PSD Level bit in the Tone Control Action register (45.2.1.55). This approach is illustrated by the algorithm in Equation (62C–1).[289]

```
for (tone=0;tone<4096;tone+=16) {
 ToneGroupRegister[0] = tone;
 ToneGroupRegister[1] = tone+16;
 ToneControlParameterRegister[1] &= 0xFFFC; // clear first 2 bits
 ToneControlParameterRegister[2] &= 0x01FF; // clear last 7 bits
 ToneControlParameterRegister[1] |= TxPSD[tone] >> 7;
 ToneControlParameterRegister[2] |= (TxPSD[tone] << 9) & 0xFE00;
}
*ToneControlActionRegister |= 0x0002; // activate PSD level setting
```

(62C–1)

62C.3.2 PSD Masks for Plan A with variable LF region

As an additional example, this –subclause describes PSD masks for Plan A with variable LF region, as introduced in 62C.2.1.

In band 0 (up to f_1 between 25 kHz and 490 kHz), the PSD is limited to –50 dBm/Hz, as is the case for 2.32 Mb/s SHDSL.

The PSD in bands 1D, 1U, 2D and 2U is limited to comply with mask M2 as defined in ATIS-0600424.

[289]Variables and pointers are used as described in 62A.4.

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Annex 63A

(normative)

PMD Profiles for 2BASE-TL

63A.1 Introduction and rationale

Annex 63A defines the PMD profiles for 2BASE-TL. These profiles define the transmission characteristics of the PHY on the media. 2BASE-TL PHYs are required to operate across varying media quality, regulatory and noise environments. The profiles defined in this clause have two purposes.

The first is to describe a bounded set of operating modes that a party might choose from when implementing, integrating and installing 2BASE-TL equipment. 2BASE-TL PHYs are inherently flexible in their transmission capabilities. The defined profiles collect a subset of these parameters into modes that work well in most deployments. For deployments that require an operating mode not defined in this Annex, profiles can be overridden by setting PHY PMD registers directly, via Clause 45 for example.

The second purpose of the profiles is to define a set of operating modes against which PHY performance compliance may be tested. The topic of performance compliance is addressed for 2BASE-TL in Annex 63B.

63A.2 Relationship to other clauses

Clause 30 describes how the selection of Annex 63A profiles is exported to a management entity.

Clause 45 registers describe an optional mechanism for configuring a 2BASE-TL PHY to use a particular profile. The register settings for each profile are contained in 63A.4.

63A.3 Profile definitions

A 2BASE-TL profile is characterized by 4 parameters: data rate, power, constellation size and region. Different regions have different constraints on the PHY. ITU-T Recommendation G.991.2 distinguishes 3 regions and lists regional requirements in three annexes labeled A, B, C. Reference Annex A generally describes those specifications that are unique to SHDSL systems operating under conditions such as those typically encountered within the North American network; Reference Annex B, within European networks; and Reference Annex C, within networks with existing TCM-ISDN service.

The profiles of Table 63A–1 will generate a net data rate greater than 2 Mb/s at the MII interface on 1 to 4 pairs. Note that the profiles are defined on a single pair basis. The aggregation mechanism is specified in Clause 61. The data rate is the closest multiple of 64 kb/s greater than a net data rate of 2 Mb/s plus the corresponding 64/65-octet encapsulation overhead divided by the number of pairs. The line rate has an additional 8 kb/s of SHDSL overhead.

The default profile shall be profile #7 (Annex B).

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Table 63A–1—2BASE-TL profiles

Profile #	Data rate per pair (kb/s)	Line rate per pair (kb/s)	Power (dBm)	Region	Constellation
1	5696	5704	13.5	Annex A sec. A.4.1	32-TCPAM
2	3072	3080	13.5	Annex A sec. A.4.1	32-TCPAM
3	2048	2056	13.5	Annex A sec. A.4.1	16-TCPAM
4	1024	1032	13.5	Annex A sec. A.4.1	16-TCPAM
5	704	712	13.5	Annex A sec. A.4.1	16-TCPAM
6	512	520	13.5	Annex A sec. A.4.1	16-TCPAM
7	5696	5704	14.5	Annex B sec. B.4.1	32-TCPAM
8	3072	3080	14.5	Annex B sec. B.4.1	32-TCPAM
9	2048	2056	14.5	Annex B sec. B.4.1	16-TCPAM
10	1024	1032	13.5	Annex B sec. B.4.1	16-TCPAM
11	704	712	13.5	Annex B sec. B.4.1	16-TCPAM
12	512	520	13.5	Annex B sec. B.4.1	16-TCPAM

63A.4 Register settings

This subclause contains Clause 45 register settings required to comply with the profiles defined in 63A.3. The 2B general parameter register (see 45.2.1.61) selects a region. The 2B PMD parameters register (see 45.2.1.62) selects values for data rate, power and constellation size. The 2B extended PMD parameters registers (see 45.2.1.76) define four additional data range sets to be used in conjunction with the 2B PMD parameters registers when additional PMD configuration detail is desired. Detailed register settings are shown in Table 63A–2.

Table 63A–2—2BASE-TL register settings

Profile #	2B general parameter register	2B PMD parameters register	
		1.81.15:0	1.82.15:0
1	0000_{16}	5959_{16}	0045_{16}
2	0000_{16}	3030_{16}	0045_{16}
3	0000_{16}	2020_{16}	0046_{16}
4	0000_{16}	1010_{16}	0046_{16}
5	0000_{16}	$0B0B_{16}$	0046_{16}
6	0000_{16}	0808_{16}	0046_{16}
7	0001_{16}	5959_{16}	$004D_{16}$
8	0001_{16}	3030_{16}	$004D_{16}$
9	0001_{16}	2020_{16}	$004E_{16}$
10	0001_{16}	1010_{16}	0046_{16}
11	0001_{16}	$0B0B_{16}$	0046_{16}
12	0001_{16}	0808_{16}	0046_{16}

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63A.5 Protocol implementation conformance statement (PICS) proforma Annex 63A, PMD Profiles for 2BASE-TL[290]

63A.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 63A, PMD Profiles for 2BASE-TL, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

63A.5.2 Identification

63A.5.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., names and versions for machines and/or operating systems; System Name(s)	

NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification.

NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).

63A.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 63A, 2BASE-TL PMD profiles.
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

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63A.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
2BProf	2BASE-TL PMD profiles	Annex 63A	The PMD profiles listed in Annex 63A are supported.	2BASE-TL: M	Yes [ ]

63A.5.4 PICS proforma tables for Performance guidelines for 2BASE-TL PMD profiles

Item	Feature	Subclause	Value/Comment	Status	Support
2BProf-1	Default Profile	63A.3	The default profile shall be profile #7.	M	Yes [ ]
2BProf-2	Register settings	63A.4	The register settings comply with Table 63A–2.	M	Yes [ ]
2BProf-3	Profiles	63A.3	A 2BASE-TL PHY supports all profiles listed in Table 63A–1.	M	Yes [ ]

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Annex 63B

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Performance guidelines for 2BASE-TL PMD profiles

63B.1 Introduction and rationale

This annex defines performance guidelines for 2BASE-TL PMD profiles. The definition of those guidelines is challenging due to the varying nature of the access network. The access network has large variations in cable characteristics from region to region. In addition, the make-up of a cable can encompass multiple cable gauges and/or different configuration of bridged taps. Finally, services may vary from region to region creating different noise scenarios. Typically, deployment guidelines are a function of the telecommunications operator, which is operating a loop and the regional spectrum management policies, which govern deployment on that loop.

Given that one cannot test every possible combination of loop make-up and noise conditions, the performance guidelines are covered from two perspectives. Firstly, 63B.3 lists a suite of artificial tests crafted to test the 2BASE-TL PHYs under representative worst-case noise and loop conditions. Secondly, 63B.4 defines a deployment guideline rule which allows a service provider to determine whether a given loop will support a given profile.

63B.2 Relationship to other clauses

Annex 63A lists a set of PMD profiles for 2BASE-TL.

Clause 30 describes how the selection of Annex 63A profiles is exported to a management entity.

Clause 45 registers describe an optional mechanism for configuring a 2BASE-TL PHY to use a particular profile. The register settings for each profile are contained in 63A.4.

63B.3 Performance test cases.

The profiles associated with the 5696, 3072, 1024, 704 and 512 kb/s (profiles 1, 2, 4, 5, and 6) shall satisfy the tests described in Table 63B-1. The same test methodology defined in G.991.2 Annex A shall be applied. The test cases are numbered 57 to 78 to differentiate them from the existing tests 1 to 56 in Table A-1 of G.991.2. Profile 3 shall successfully pass the corresponding tests described in Table A-1 of G.991.2.

Table 63B-1—Additional tests for the Annex A data rate

Test	Test loop	L (km)	Test unit	Payload data rate (kb/s)	PSD	Interferer Combination	Required Margin (dB)
57	S	2.80	2BASE-TL-O	1024	symmetric	49-HDSL	5 + Δ*
58	BT1-C	2.47	2BASE-TL-O	1024	symmetric	49-SHDSL_768_sym	5 + Δ*
59	BT1-C	2.47	2BASE-TL-O	1024	symmetric	49-HDSL	5 + Δ*
60	S	2.83	2BASE-TL-R	1024	symmetric	49-HDSL	5 + Δ*
61	BT1-R	2.47	2BASE-TL-R	1024	symmetric	49-SHDSL_768_sym	5 + Δ*
62	BT1-R	2.47	2BASE-TL-R	1024	symmetric	49-HDSL	5 + Δ*

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Table 63B-1—Additional tests for the Annex A data rate *(continued)*

Test	Test loop	L (km)	Test unit	Payload data rate (kb/s)	PSD	Interferer Combination	Required Margin (dB)
63	S	3.44	2BASE-TL-O	704	symmetric	49-HDSL	5 + Δ*
64	BT1-C	3.17	2BASE-TL-O	704	symmetric	49-SHDSL_768_sym	5 + Δ*
65	BT1-C	3.17	2BASE-TL-O	704	symmetric	49-HDSL	5 + Δ*
66	S	3.44	2BASE-TL-R	704	symmetric	49-HDSL	5 + Δ*
67	BT1-R	3.17	2BASE-TL-R	704	symmetric	49-SHDSL_768_sym	5 + Δ*
68	BT1-R	3.17	2BASE-TL-R	704	symmetric	49-HDSL	5 + Δ*
69	S	4.08	2BASE-TL-O	512	symmetric	49-HDSL	5 + Δ*
70	BT1-C	3.75	2BASE-TL-O	512	symmetric	49-SHDSL_768_sym	5 + Δ*
71	BT1-C	3.75	2BASE-TL-O	512	symmetric	49-HDSL	5 + Δ*
72	S	4.08	2BASE-TL-R	512	symmetric	49-HDSL	5 + Δ*
73	BT1-R	3.75	2BASE-TL-R	512	symmetric	49-SHDSL_768_sym	5 + Δ*
74	BT1-R	3.75	2BASE-TL-R	512	symmetric	49-HDSL	5 + Δ*
75	S	1.37	2BASE-TL-O	3072	symmetric	49-SHDSL_2304 (case 11)	5 + Δ*
76	S	1.37	2BASE-TL-R	3072	symmetric	49-SHDSL_2304 (case 11)	5 + Δ*
77	S	0.85	2BASE-TL-O	5696	symmetric	24-HDSL2+24-T1 (case 4)	5 + Δ*
78	S	0.85	2BASE-TL-R	5696	symmetric	24-HDSL2+24-T1 (case 14)	5 + Δ*

Profiles 7 and 8 shall be tested using tests B-1 to B-4 defined in Table 63B-2. The same test methodology defined in G.991.2 Annex B shall be applied. Profile 9, 10 and 12 shall be tested using the tests defined in Annex B of ITU-T Recommendation G.991.2. The loops defined in Annex B do not scale as well as the loops of Annex A because they are defined in terms of insertion loss at a given frequency (with a granularity of 0.5 dB), rather than a length in meters. The 704 kb/s data rate (profile 11) is expected to successfully pass the test associated with the 768 kb/s data rate. Therefore, for Annex B testing, the 704 kb/s data rate shall be tested using the 768 kb/s test.

Table 63B-2—Additional tests for the Annex B data rate

Test	Test loop	L (km)	Test unit	Payload data rate (kb/s)	PSD	Interferer Combination[a]	Required Margin (dB)
B-1	Loop 2	1.37	2BASE-TL-O	3072	symmetric	C2048sD2	5 + Δ*
B-2	Loop 2	1.37	2BASE-TL-R	3072	symmetric	R1536sB2	5 + Δ*
B-3	Loop 2	0.85	2BASE-TL-O	5696	symmetric	C2304sD2	5 + Δ*
B-4	Loop 2	0.85	2BASE-TL-R	5696	symmetric	R2048sA2	5 + Δ*

[a]The following nomenclature is used to describe Annex B noise shapes: ABBBCDE; where A is the Side (either C or R), BBB, the rate, C the PSD type (either ‘s’ for symmetric or ‘a’ for asymmetric), D the Noise type (A,B,C or D) and E, the loop number (from 1 to 7).

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63B.4 Deployment Guidelines

The ITU-T G.991.2 defines an equivalent loop attenuation which can be used to determine whether a cable insertion loss function 1/H(f), can support a given profile associated with a nominal transmit signal power spectral density S(f). The loop attenuation should not be confused with another popular metric called the loop insertion loss at a given frequency. The latter specifies the insertion loss of the loop at a single frequency while the former weights the transmitted signal PSD and insertion loss of the loop over a frequency range corresponding to the transmitted signal bandwidth. The loop attenuation provides a more precise estimate of the loop capability to support a given data rate.

The SHDSL Loop Attenuation shall be defined as follows (section 9.5.5.7.5 of G.991.2):

$$LoopAtten_{SHDSL}(H) = \frac{2}{f_{\text{Baud}}}\left(\int_{0}^{\frac{f_{\text{Baud}}}{2}} 10\log\left[\sum_{n=0}^{1} S(f - nf_{\text{Baud}})\right] df - \int_{0}^{\frac{f_{\text{Baud}}}{2}} 10\log\left[\sum_{n=0}^{1} S(f - nf_{\text{Baud}})\left|H(f - nf_{\text{Baud}})\right|^2\right] df \right) \quad \text{(63B–1)}$$

where f_{Baud} is the symbol rate, $1/H(f)$ is the insertion loss of the loop, and $S(f)$ is the nominal transmit PSD.

Table 63B-3 lists the maximum loop attenuation for a margin of 5 dB assuming the presence of 49 and 12 self-interferers for the profiles defined in Annex 63A. The 49 self-interferer case corresponds to a very conservative deployment reach.

Assuming a data rate of 2048 kb/s, the deployment reach for AWG24 gauge cable corresponds to 2.8 km for the 49-self number and 3.2 km for the 12-self number.

Table 63B-3—Loop attenuation guideline

Profile	Data rate (kb/s)	Maximum SHDSL Loop Attenuation for 49-self-interferers	Maximum SHDSL Loop Attenuation for 12-self-interferers
2 and 7	2048	24.0	27.7
3 and 8	1024	28.6	32.1
4 and 9	704	31.0	34.7
5 and 10	512	33.1	36.7

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63B.5 Protocol implementation conformance statement (PICS) proforma for Annex 63B, Performance guidelines for 2BASE-TL PMD profiles[291]

63B.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 63B, Performance guidelines for 2BASE-TL PMD profiles, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

63B.5.2 Identification

63B.5.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., names and versions for machines and/or operating systems; System Name(s)	

NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification.

NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).

63B.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 63B, Performance guidelines for 2BASE-TL PMD profiles.
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21, the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

[291] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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63B.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
2BPerf	Performance guidelines for 2BASE-TL PMD profiles	Annex 63B	The performance guidelines listed in Annex 63B are supported.	2BASE-TL: M	Yes [ ]

63B.5.4 PICS proforma tables for Performance guidelines for 2BASE-TL PMD profiles

Item	Feature	Subclause	Value/Comment	Status	Support
2BPerf-1	Performance	63B.3	A 2BASE-TL PHY successfully passes the performance tests described in 63B.3.	M	Yes [ ]

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Annex 67A

(informative)

Environmental characteristics for Ethernet subscriber access networks

67A.1 Introduction

The purpose of EFM and its distinction from traditional Ethernet networks, is that it specifies functionality required for the subscriber access network, i.e., public network access. Network design considerations for "public" access that may differ from traditional Ethernet LANs include the operations, administration and management (OAM) function, and the regulatory requirements, as well as the environmental factors that are addressed in this annex. This annex applies to Clause 56 through Clause 67 with particular relevance for Clause 58, Clause 59, and Clause 60.

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). implementers are expected to indicate in their literature the operating environmental conditions to facilitate selection, installation, and maintenance, and may also give summary information on a product label. The normative specifications of this standard are understood to apply over the range of conditions defined by the implementer.

This informative annex provides information, to both the design engineer and the eventual user of specific product implementations, on the environmental factors to be considered when designing EFM network topologies. It is intended to record the assumptions used in developing the specifications contained in the normative specifications. The following sections give an example of likely deployment of the different Physical Layer types, followed by a discussion of temperature issues. Informative references may be found in Annex A.

It is believed that the most critical environmental factor on an Ethernet terminal will be temperature and that the most temperature sensitive element in a link is the semiconductor laser. The temperature sensitivity of these components may impact potential deployment scenarios if not considered. The remaining environmental factors (humidity, vibration, etc.) are not considered to be of such major importance and may be handled by conventional design practice. Therefore, the remainder of this annex addresses temperature.

67A.1.1 Terminal deployment scenarios

The terminal equipment of a link may or may not be in a weather-protected environment. 100BASE-LX10 and 1000BASE-LX10 links may be widely deployed with conventional building cabling for general purpose IT applications, as well as in Ethernet subscriber access applications. The other link types in Table 67A–1 are intended for Ethernet subscriber access applications. The table gives an example deployment scenario. Other scenarios are also supported by this standard, and may be deployed in significant numbers.

This example scenario places the customer premises equipment in a non-weather-protected position, e.g. the outside wall of a house, to allow ease of access for installation and maintenance. Where the premises is a large building such as a hotel, apartment block or office, a weather-protected space such as a basement within the building may be accessible enough.

It is expected that the physical format of the equipment at each end of the link will be different; however, this is outside the scope of the standard. The Physical Layer type (e.g., 2BASE-TL) and the PMD type (e.g., 1000BASE-PX20-U) are classifications of the signal on the line, and do not imply a temperature range or physical format.

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Table 67A–1—Informative deployment examples

Head end (nearer the center of the network)	Customer premises (nearer the periphery of the network)
Weather-protected	Not weather-protected or weather-protected
100BASE-LX10	100BASE-LX10
100BASE-BX10-D	100BASE-BX10-U
1000BASE-LX10	1000BASE-LX10
1000BASE-BX10-D	1000BASE-BX10-U
1000BASE-PX10-D	1000BASE-PX10-U
1000BASE-PX20-D	1000BASE-PX20-U
10PASS-TS-O	10PASS-TS-R
2BASE-TL-O	2BASE-TL-R

67A.2 Temperature

Large portions of Ethernet subscriber access optical and copper links are expected to operate in environmental conditions consistent with the outside plant. However, it is recognized that the exact requirements for a particular deployment will vary greatly depending on the geographic location, system structure, and governing regulations. It is also recognized that portions of the network may be deployed in more benign and protected environments and that in some geographic location the outside environment may also be considered benign.

There are many factors. The temperatures in coastal regions are not usually extreme. Tropical regions are usually hot or hot and wet. The widest temperature swings are found in dry regions in the interior of large continents, e.g. central North America or central Asia. High altitude may reduce the efficacy of air cooling systems. To an extent, this is offset by the typically cooler air temperature at high altitude. Direct sunshine can add up to 1120 W/m^2 heating - see Table 1 of ETSI EN 300 019-1-3 [B21].

As a reference, Table 67A–2 shows the annual extreme air temperature values for the nine classes of climates from IEC 60721-2-1 [B31].

The climate is the basic determining factor in the component temperature. However, the temperature of the equipment using the component is significantly modified by a number of factors related to the location of the equipment. Some of these are:

— Is the equipment location weather-protected or non-weather-protected
— Is the building temperature controlled
— Are locations without temperature control subject to solar heating

Equipment temperatures for a number of locations from ETSI and Telcordia documents are shown in Table 67A–3.

An additional factor is the internal thermal design of the equipment using the optical component. The component temperature will be higher than the equipment ambient and the increase will be implementation dependant. For equipment with the complexity of EFM systems an internal temperature rise of 15 ºC to 20 ºC may be anticipated.

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Table 67A–2—Informative listing of climate types

Type of climate	Low temperature (°C)	High temperature (°C)
Extremely cold (except the Central Antarctic)	–65	+32
Cold	–50	+32
Cold temperate	–33	+34
Warm temperate	–20	+35
Warm dry	–20	+40
Mild warm dry	–5	+40
Extremely warm dry	+3	+55
Warm damp	+5	+40
Warm damp, equable	+13	+35

Table 67A–3—Informative listing of equipment temperature ranges

Climate or location	Specified ambient temperature	Reference
Weather-protected		
Telecom control rooms	15 – 30°C	ETSI Class 3.6
Temperature controlled	5 – 40°C (–5 – 45°C with cooling failure)	ETSI Class 3.1
Controlled - long term	5 – 40°C (–5 – 50°C short term)	Telcordia GR-63 [B29]
Partly temperature-controlled	–5 – 45°C	ETSI Class 3.2
Not temperature-controlled	–25 – 55°C	ETSI Class 3.3
Sheltered locations	–40 – 40°C	ETSI Class 3.5
Extended/uncontrolled	–40 – 46°C (-40 to 65°C inside enclosure)	Telcordia GR-487 [B28], GR-468 [B27]
Sites with heat trap	–40 – 70°C	ETSI Class 3.4
Non-weather-protected		
Temperate	–33 – 40°C	ETSI Class 4.1
Extended	–45 – 45°C	ETSI Class 4.1E
Extremely cold	–65 – 35°C	ETSI Class 4.2L
Extremely warm dry	–20 – 55°C	ETSI Class 4.2H

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67A.3 Temperature impact on optical components

Components are often commercially available in two grades, 0 to 70°C and –40 to 85°C, although optoelectronic components are also available in –20 or –10 to 85°C grade, depending on format. The GBIC MSA requires an operating temperature range of 0 to 50°C in moving air. Because of the varied physical format of equipment and components, the reader is advised to refer to specific product literature or multi source agreements for precise information.

The most temperature sensitive sub-component in an Ethernet terminal is expected to be the semiconductor laser, if for a fiber optic link. There are two categories of laser presently commonplace in the Physical Layers addressed here; Fabry-Perot (FP), a type of multi longitudinal mode (MLM) laser, and distributed feedback (DFB), a type of single longitudinal mode (SLM) laser.

Fabry-Perot lasers may have a temperature coefficient of wavelength around 0.45 nm/K, so the operating wavelength of a particular FP may vary by 55 nm over the range –40 to 85°C. The operating wavelength windows within this standard are generally 100 nm wide where FPs are anticipated, allowing adequate margin for manufacturing tolerances. To allow for the widest variety of implementation the spectral width is specified as a function of wavelength where appropriate. However, the requirement for low error ratios over substantial distances of fiber, as specified by transmitter and dispersion penalty (TDP), forces the implementer of 1000 Mb/s FP laser based implementations to pay careful attention to both wavelength and spectral width to avoid excessive mode partition noise. In practice, the full range of wavelengths in the standard is not actually available for use because at the temperature extremes the required spectral width would be too narrow. It can be seen that the wider the temperature range required, the more precisely the wavelength and spectral width has to be contained to achieve a particular reach. This may have an impact on cost. This consideration would be expected to apply to 1000BASE-LX10, 1000BASE-BX10-U and 1000BASE-PX10-U.

Where the dispersion of the link or the wavelength limits are more demanding than can be met cost-effectively with FPs, DFBs may be used. They may have a temperature coefficient of wavelength under 0.1 nm/K and much narrower spectral widths than FPs. Because only a single longitudinal mode is present, a DFB does not suffer from mode partition noise. DFBs are generally more expensive than FPs. A DFB's lasing wavelength varies at 0.1 nm/K while its gain peak varies at around 0.45 nm/K. At extremes of temperature these two wavelengths are far apart and the laser may perform poorly. For this reason, DFBs for extended temperature range may be more expensive again. This consideration would be expected to apply to 1000BASE-BX10-D, 1000BASE-PX10-D, and 1000BASE-PX20.

67A.3.1 Component case temperature recommendations

67A.2 discussed the temperature progression from climate to equipment to component. 67A.3 discussed the impact of temperature, and particularly temperature range, on the design and cost of laser based optical components. In order to balance these two effects, contain costs, and yet cover the widest range of climates to allow access to the greatest markets the following recommendations are made.

Two component case temperature ranges, and by inference a third, are developed. These are defined as follows:

- Warm Extended: Intended for outdoor application in warmer climate locations.
- Cool Extended: Intended for outdoor applications in cooler climate locations.
- Universal Extended: (This is not a separate class, but is defined by simultaneously complying with the Warm and Cool Extended temperature ranges) This is a combination of the requirements for the Warm Extended and Cool Extended Classes and is intended for general outdoor applications in areas with wide seasonal variations or those designs intended for deployment in multiple geographic locations.

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The recommended component case temperature ranges for these two classes are shown in Table 67A–4.

Table 67A–4—Component case temperature class recommendations

Class	Low temperature (°C)	High temperature (°C)
Warm extended	–5	+85
Cool extended	–40	+60
Universal extended	–40	+85

It will be noted that the recommendations of Table 67A–4 do not address the extremely cold climates of Table 67A–2 or the cold non-weather-protected equipment requirements of Table 67A–3. In these geographic locations it is common practice to avoid non-weather-protected locations for systems of EFM complexity and place the equipment indoors.

These temperature ranges are optional and conformance with these ranges is not required. This allows lower cost components to be had for those applications that require less extreme temperature ranges. This may be done by taking advantage of the reduced wavelength change to ease the central wavelength tolerance and spectral width requirements from the trade-off curves and more particularly, the TDP limit. This allows equipment and component suppliers, at their discretion, to develop systems and components that tolerate less severe environmental conditions that they view as suitable for their market as long as the PMD is consistent with the PICS proforma of the relevant clause. This limitation assures interoperability while allowing the equipment to be developed for specific markets. It is to be noted that the PMD specifications included in the optics Clause 58, Clause 59, and Clause 60 are based on a temperature range of –40 to 85°C in terms of the wavelength ranges and spectral widths defined.

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Annex 69A

(normative)

Interference tolerance testing

69A.1 Introduction

A major problem in communicating across crowded backplanes is interference. The interfering signal can come from a variety of sources including:

a) Crosstalk from other data channels running the same kind of signals as the channel of interest. This type of interference is usually subdivided into:
   1) Far-end crosstalk (FEXT) coming from data traveling in the same general direction as the channel of interest.
   2) Near-end crosstalk (NEXT) originating from a channel with a transmitter near the receiver of the channel of interest.
b) Self interference caused by reflections due to impedance discontinuities, stubs, etc. This is a form of intersymbol interference (ISI) that is beyond what a reasonable equalizer can compensate.
c) Alien crosstalk which is defined to be interference from unrelated sources such as clocks, other kinds of data, power supply noise, etc.

For the channel to work, the receiver has to be able to extract correct data from the lossy channel in the presence of interference. The ability of the receiver to extract data in the presence of interference is an important characteristic of the receiver and needs to be measured. This ability is called interference tolerance.

69A.2 Test setup

The interference tolerance test is performed with the setup shown in Figure 69A–1.

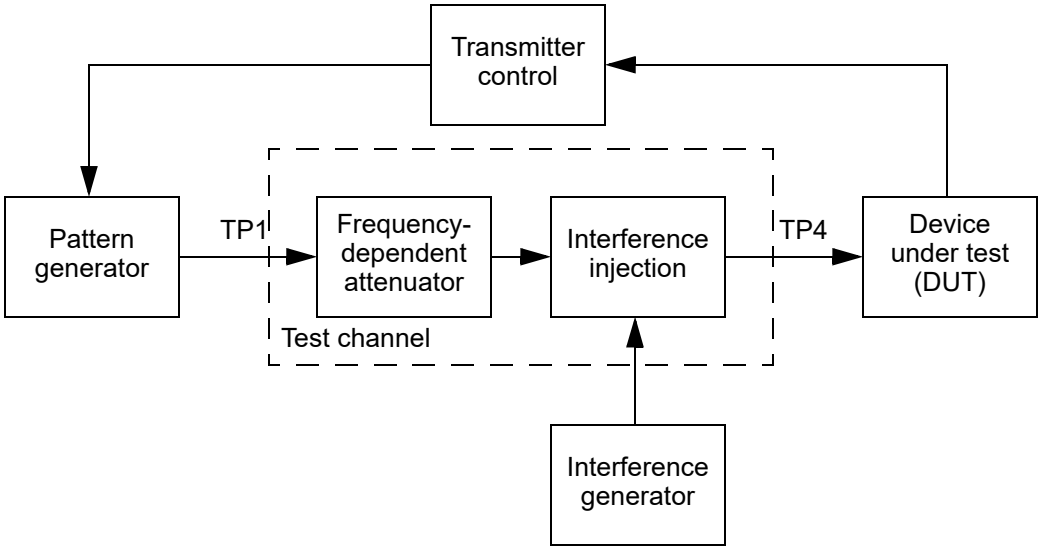

Figure 69A–1—Interference tolerance test setup

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69A.2.1Pattern generator

For 1000BASE-KX and 10GBASE-KX4, the amplitude delivered by the pattern generator to the test channel shall be no greater than the specified minimum transmitter output amplitude for the port type being tested adjusted by a gain b_{TC} as defined in 69A.2.2.

For 2.5GBASE-KX, the peak-to-peak amplitude delivered by the pattern generator, as measured on a sequence of alternating ones and zeros, shall be no more than 800 mV, adjusted by a gain b_{TC} as defined in 69A.2.2.

For 5GBASE-CR, 10GBASE-KR, and 40GBASE-KR4, the peak-to-peak amplitude delivered by the pattern generator, as measured on a sequence of alternating ones and zeros, shall be no more than 800 mV, adjusted by a gain b_{TC} as defined in 69A.2.2, regardless of equalization setting.

The applied transition time at the pattern generator output shall be no less than the minimum value specified for the port type being tested. If the transition time of the pattern generator is less than the minimum specified applied transition time, an equivalent stress may be introduced in the test channel. The test channel, defined in 69A.2.2, is chosen so that the insertion loss of the test channel has a specific relationship to the maximum fitted attenuation, A_{max}, defined in 69B.4.2. If the minimum specified applied transition time is T_r(min), and the transition time of the pattern generator is T_r, then the test channel may be used to generate an equivalent stress by incrementing the parameter b_3 in A_{max} by Δb_3 as defined in Equation (69A–1).

$$\Delta b_3 = 6.8 \times (T_r(\min)^2 - T_r^2) \quad (69A–1)$$

The signaling speed of the pattern generator shall be offset ±100 ppm relative to the nominal signaling speed of the port type being tested.

The pattern generator shall have jitter on its output. This jitter shall consist of sinusoidal jitter at a frequency no less than 1/250 of signaling speed, duty cycle distortion, and random jitter. The random jitter shall be measured at the output of a single pole high-pass filter with cut-off frequency at 1/250 of the signaling speed. The sinusoidal jitter, duty cycle distortion, and random jitter shall each be no less than the amount specified for the port type being tested.

The pattern generator may include equalization depending on the port type being tested. For 1000BASE-KX and 2.5GBASE-KX, the pattern generator shall not include equalization. For 5GBASE-KR, equalization equivalent to a two-tap transversal filter meeting the requirements of Table 130–4 shall be included. For 10GBASE-KX4, the pattern generator shall include equalization such that the differential output template defined in 71.7.1.6 is met. For 10GBASE-KR, equalization equivalent to a three-tap transversal filter meeting the requirements of 72.7.1.10 shall be included.

69A.2.2Test channel

The test channel is a 100 Ω differential system consisting of a frequency-dependent attenuator and an interference injection block.

The interference injection block may be a pair of directional couplers, a pair of pick-off tees, or any other component, as long as the combination of the interference injection block and the frequency-dependent attenuator satisfies the requirements of the test channel.

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The frequency dependent attenuator is recommended to be constructed in such a way that it accurately represents the insertion loss and group delay characteristics of differential traces on an FR-4 printed circuit board.

The test channel is specified with respect to transmission magnitude response, IL_{TC}, and return loss. Assuming the transmission magnitude response is measured at N uniformly-spaced frequencies f_n spanning the frequency range f_1 to f_2, the transmission magnitude is described by two parameters, m_{TC} and b_{TC}, as defined in Equation (69A–2) through Equation (69A–7).

$$m_X = \frac{1}{N}\sum_n A_{max}(f_n) \tag{69A–2}$$

$$m_Y = \frac{1}{N}\sum_n IL_{TC}(f_n) \tag{69A–3}$$

$$m_{XY} = \frac{1}{N}\sum_n A_{max}(f_n) IL_{TC}(f_n) \tag{69A–4}$$

$$m_{XX} = \frac{1}{N}\sum_n A_{max}(f_n) A_{max}(f_n) \tag{69A–5}$$

$$m_{TC} = \frac{m_{XY} - m_X m_Y}{m_{XX} - m_X m_X} \tag{69A–6}$$

$$b_{TC} = m_Y - m_{TC} m_X \tag{69A–7}$$

The values f_1 and f_2 are a function of the port type under test (see Table 69B–1 and Table 69B–2) and A_{max} is defined in 69B.4.2.

The test channel shall have m_{TC} greater than the minimum value specified for the port type under test and the test being performed. The test channel return loss, as measured at TP1 (see Figure 69A–1) and TP4 (see Figure 69A–1), shall be greater than or equal to 20 dB from f_{min} to f_2.

69A.2.3Interference generator

The interference generator is a broadband noise generator capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from f_1 to 0.5 times the signaling speed for the port type under test with a crest factor of no less than 5. The noise shall be measured at the output of a filter connected to TP4. The filter for this measurement shall have no more than a 40 dB/decade roll-off and a 3 dB cut-off frequency at least 0.5 times the signaling speed.

69A.2.4Transmitter control

For 10GBASE-KR testing, the pattern generator is controlled by transmitter control. Transmitter control responds to inputs from the receiver to adjust the equalization of the pattern generator. The receiver may communicate through its associated transmitter, using the protocol described in 72.6.10, or by other means. For 2.5GBASE-KX and 5GBASE-KR testing, transmitter control is not used.

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69A.3 Test methodology

For 10GBASE-KR testing, the pattern generator shall first be configured to transmit the training pattern defined in 72.6.10.2. During this initialization period, the DUT shall configure the pattern generator equalizer, via transmitter control, to the coefficient settings it would select using the protocol described in 72.6.10. During training, the broadband noise measured at TP4 (see Figure 69A–1) shall have RMS amplitude less than 1 mV. Training patterns and transmitter control are not used for 2.5GBASE-KX and 5GBASE-KR testing.

The pattern generator shall be configured to transmit the test pattern defined for the port type under test.

The broadband noise source shall then be set to the amplitude specified for the port type being tested, as measured at TP4 (see Figure 69A–1). The measured BER shall be less than the target BER specified for the port type under test.

The interference tolerance test parameters are specified in Table 70–7 for 1000BASE-KX, in Table 71–7 for 10GBASE-KX4, in Table 128–6 for 2.5GBASE-KX, in Table 130–6 for 5GBASE-KR, and in Table 72–10 for 10GBASE-KR and 40GBASE-KR4.

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Annex 69B

(informative)

Interconnect characteristics

69B.1 Overview

Backplane Ethernet is primarily intended to operate over differential, controlled impedance traces up to 1 m, including two connectors, on printed circuit boards residing in a backplane environment. The performance of such an interconnect is highly dependent on implementation.

69B.2 Reference model

The backplane interconnect is defined between test points TP1 and TP4 as shown in Figure 69B–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

Informative characteristics and methods of calculation for the insertion loss, insertion loss deviation, return loss, crosstalk, and the ratio of insertion loss to crosstalk between TP1 and TP4 are defined in 69B.4.3, 69B.4.4, 69B.4.5, 69B.4.6, and 69B.4.6.4 respectively. These characteristics may be applied to a specific implementation of the full path (including transmitter and receiver packaging and supporting components) for a complete assessment of system performance and the interaction of these components.

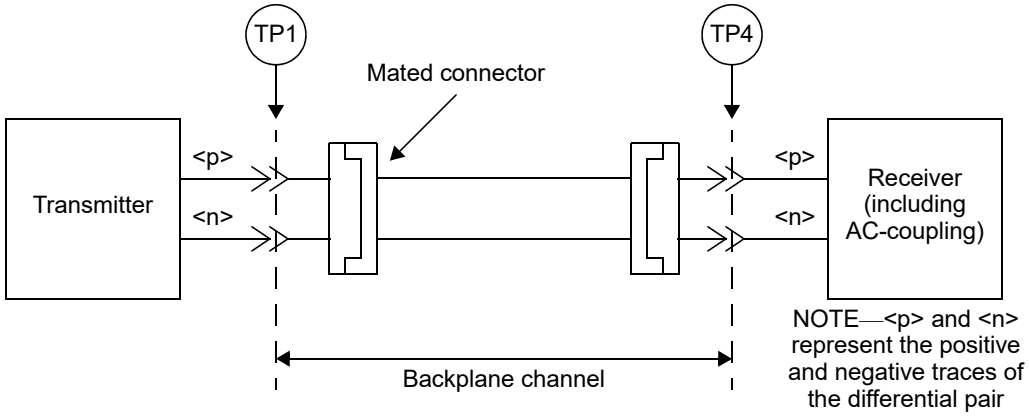

Figure 69B–1—Interconnect reference model

69B.3 Characteristic impedance

The recommended differential characteristic impedance of circuit board trace pairs is 100 Ω ± 10%.

The total differential skew from TP1 to TP4 is recommended to be less than the minimum transition time for port type of interest.

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69B.4 Channel parameters

69B.4.1 Overview

A series of informative parameters are defined for use in backplane channel evaluation. These parameters address the channel insertion loss and crosstalk.

The informative parameters for channel insertion loss are based on the amount of loss allowed for a given level of interference as verified by the interference tolerance test procedure defined in Annex 69A.

The informative parameters for channel insertion loss are summarized in Table 69B–1 and Table 69B–2.

The maximum fitted attenuation (A_{max}) due to trace skin effect and dielectric properties is defined in 69B.4.2. The maximum insertion loss (IL_{max}) is defined in 69B.4.3. The maximum deviation of insertion loss from the best-fit attenuation (ILD) is defined in 69B.4.4. The minimum return loss (RL_{min}) is defined in 69B.4.5. The limit on crosstalk in relation to insertion loss (ICR_{min}) is defined in 69B.4.6.4. All of the different parameters have to be considered together in evaluating the overall channel performance.

Table 69B–1—Insertion loss parameters for 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, and 40GBASE-KR4

Parameter	1000BASE-KX	10GBASE-KX4	10GBASE-KR 40GBASE-KR4	Units
f_{min}	0.05			GHz
f_{max}	15.00			GHz
b_1	2.00×10^{-5}			
b_2	1.10×10^{-10}			
b_3	3.20×10^{-20}			
b_4	-1.20×10^{-30}			
f_1	0.125	0.312	1.000	GHz
f_2	1.250	3.125	6.000	GHz
f_a	0.100	0.100	0.100	GHz
f_b	1.250	3.125	5.15625	GHz

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Table 69B–2—Insertion loss parameters for 2.5GBASE-KX and 5GBASE-KR

Parameter	2.5GBASE-KX	5GBASE-KR	Units
f_{min}	0.05		GHz
f_{max}	2.34375	3.8671875	GHz
b_1	2.4×10^{-5}		
b_2	1.3×10^{-10}		
b_3	4.9×10^{-20}		
b_4	-1.9×10^{-30}		
f_1	0.312	0.5	GHz
f_2	1.5625	2.578125	GHz
f_a	0.1		GHz
f_b	1.5625	2.578125	GHz

69B.4.2 Fitted attenuation

The fitted attenuation, A, is defined to be the least mean squares line fit to the insertion loss computed over the frequency range f_1 to f_2. Assuming the transmission magnitude response is measured at N uniformly-spaced frequencies f_n spanning the frequency range f_1 to f_2, the least mean squares line fit procedure is defined by Equation (69B–1) through Equation (69B–5).

$$f_{avg} = \frac{1}{N}\sum_n f_n \tag{69B–1}$$

$$IL_{avg} = \frac{1}{N}\sum_n IL(f_n) \tag{69B–2}$$

$$m_A = \frac{\sum_n (f_n - f_{avg})(IL(f_n) - IL_{avg})}{\sum_n (f_n - f_{avg})^2} \tag{69B–3}$$

$$b_A = IL_{avg} - m_A f_{avg} \tag{69B–4}$$

$$A(f) = m_A f + b_A \tag{69B–5}$$

It is recommended that the fitted attenuation of the channel be less than or equal to A_{max} as defined by the Equation (69B–6), where f is expressed in Hz and the coefficients b_1 through b_4 are given in Table 69B–1 and Table 69B–2.

$$A(f) \le A_{max}(f) = 20\log_{10}(e) \times (b_1\sqrt{f} + b_2 f + b_3 f^2 + b_4 f^3) \tag{69B–6}$$

for $f_1 \le f \le f_2$. The fitted attenuation limit is illustrated in Figure 69B–2 and Figure 69B–3.

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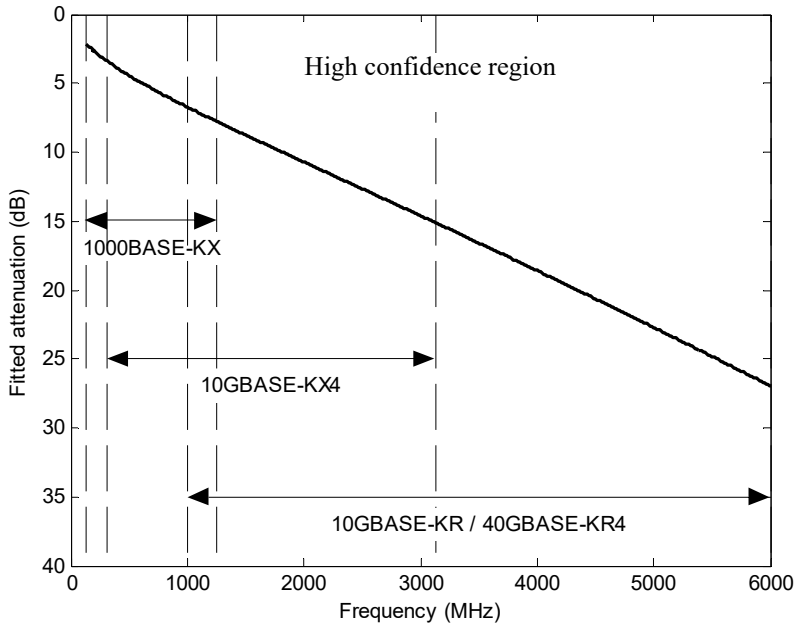

Figure 69B–2—Fitted attenuation limit for 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, and 40GBASE-KR4

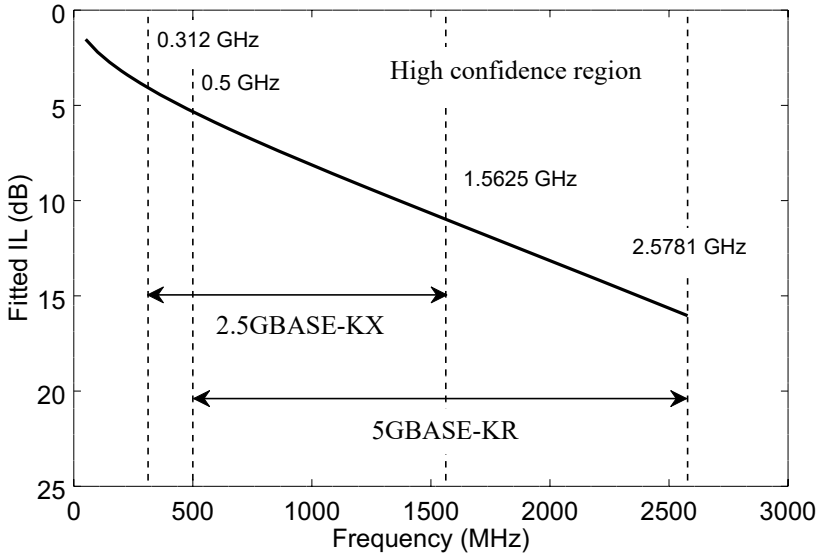

Figure 69B–3—Fitted attenuation limit for 2.5GBASE-KX and 5GBASE-KR

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69B.4.3 Insertion loss

Insertion loss is defined as the magnitude, expressed in decibels, of the differential response measured from TP1 to TP4. For 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, and 40GBASE-KR, it is recommended that the insertion loss magnitude, *IL*, be within the high confidence region defined by Equation (69B–7) and Equation (69B–8).

$$IL(f) \le IL_{\max}(f) = A_{\max}(f) + 0.8 + 2.0\times10^{-10} f \quad \text{(69B–7)}$$

for $f_{\min} \le f \le f_2$

$$IL(f) \le IL_{\max}(f) = A_{\max}(f) + 0.8 + 2.0\times10^{-10} f_2 + 1\times10^{-8}(f - f_2) \quad \text{(69B–8)}$$

for $f_2 < f \le f_{\max}$

For 2.5GBASE-KX, it is recommended that the insertion loss magnitude, *IL*, be within the high confidence region defined by Equation (69B–9).

$$IL(f) \le \left\{ \begin{array}{cc} 0.668 + 3.755\sqrt{f} + 3.608f & f_{\min} \le f < f_2 \\ -23.753 + 22.242f & f_2 \le f < f_{\max} \end{array} \right\} \text{ (dB)} \quad \text{(69B–9)}$$

For 5GBASE-KR, it is recommended that the insertion loss magnitude, *IL*, be within the high confidence region defined by Equation (69B–10).

$$IL(f) \le \left\{ \begin{array}{cc} 0.668 + 3.755\sqrt{f} + 3.608f & f_{\min} \le f < f_2 \\ -18.753 + 13.48f & f_2 \le f < f_{\max} \end{array} \right\} \text{ (dB)} \quad \text{(69B–10)}$$

The values of $f_{\min}$, f_2, and $f_{\max}$ are given in Table 69B–1 and Table 69B–2 and $A_{\max}$ is given in Equation (69B–6). The insertion loss limit is illustrated in Figure 69B–4 through Figure 69B–8.

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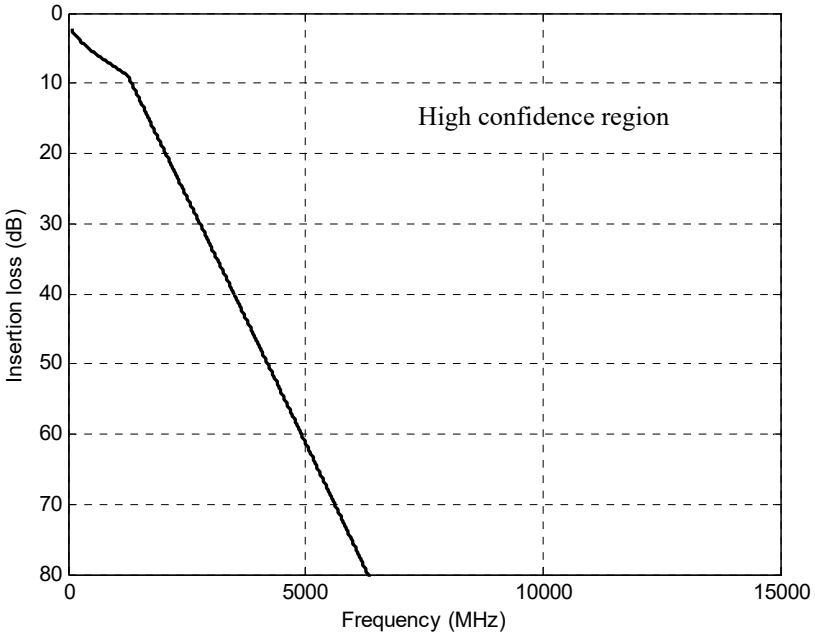

Figure 69B–4—Insertion loss limit for 1000BASE-KX

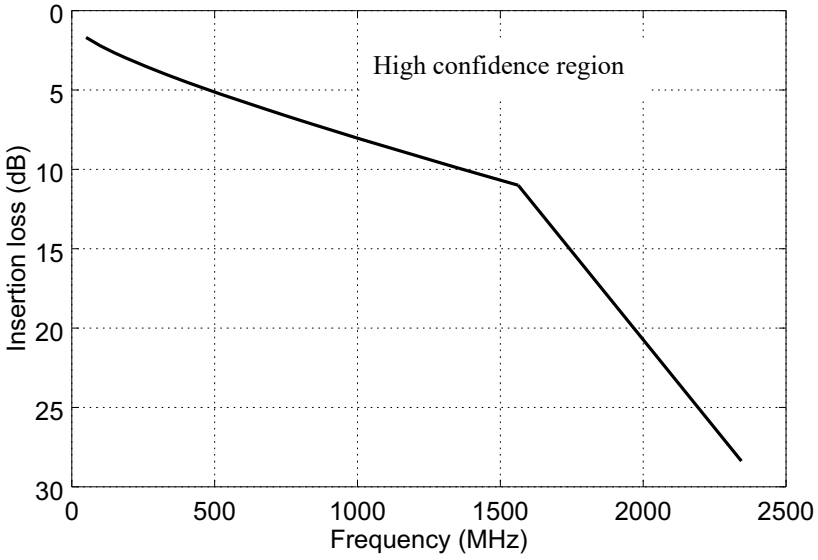

Figure 69B–5—Insertion loss limit for 2.5GBASE-KX

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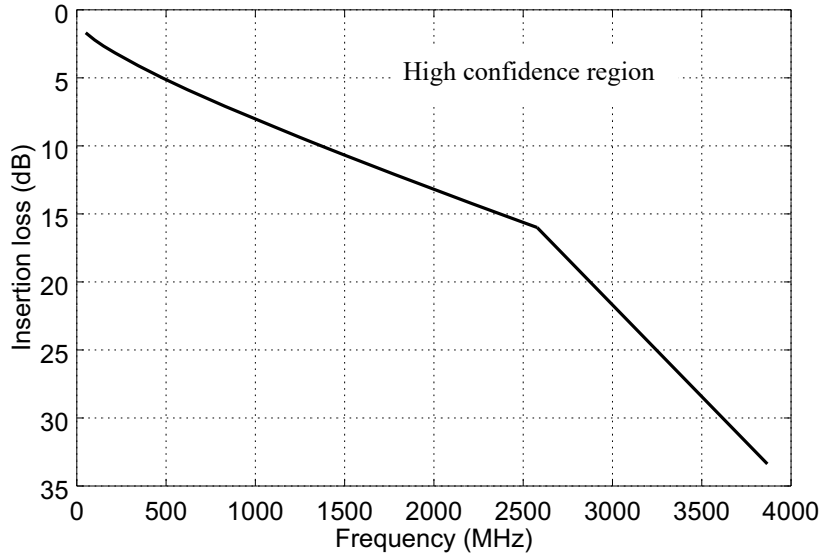

Figure 69B–6—Insertion loss limit for 5GBASE-KR

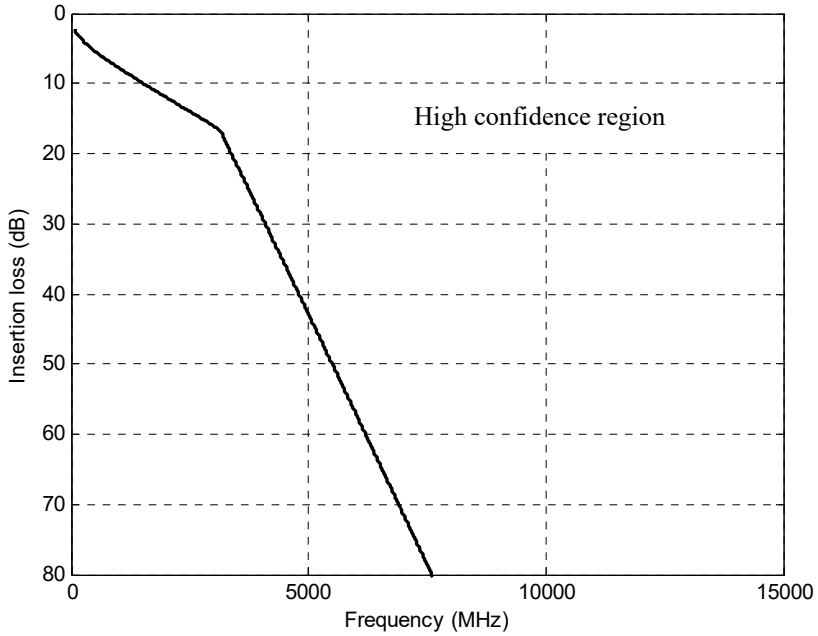

Figure 69B–7—Insertion loss limit for 10GBASE-KX4

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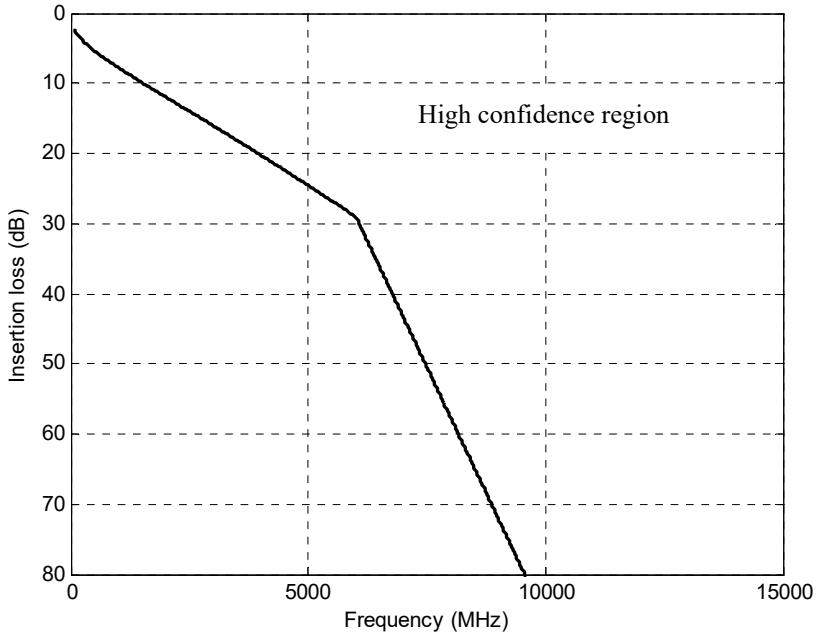

Figure 69B–8—Insertion loss limit for 10GBASE-KR and 40GBASE-KR4

69B.4.4 Insertion loss deviation

The insertion loss deviation, as defined by Equation (69B–11), is the difference between the insertion loss and the fitted attenuation defined in 69B.4.2.

$$ILD(f) = IL(f) - A(f) \tag{69B–11}$$

For 100BASE-KX, 10GBASE-KX4, 10GBASE-KR, and 40GBASE-KR, it is recommended that *ILD* be within the high confidence region defined by Equation (69B–12) and Equation (69B–13).

$$ILD(f) \geq ILD_{\min}(f) = -1.0 - 0.5\times10^{-9}f \tag{69B–12}$$

$$ILD(f) \leq ILD_{\max}(f) = 1.0 + 0.5\times10^{-9}f \tag{69B–13}$$

for $f_1 \leq f \leq f_2$.

For 2.5GBASE-KX and 5GBASE-KR, it is recommended that ILD be within the high confidence region defined by Equation (69B–14) and Equation (69B–15).

$$ILD(f) \geq ILD_{min}(f) = -1.0 - 0.7\times10^{-9}f \tag{69B–14}$$

$$ILD(f) \leq ILD_{max}(f) = 1.0 + 0.7\times10^{-9}f \tag{69B–15}$$

for $f_1 \leq f \leq f_2$.

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The recommendation applies over the frequency range $f_1 \le f \le f_2$. The values of f_1 and f_2 are dependent on port type and are given in Table 69B–1 and Table 69B–2. The insertion loss deviation limits for each port type is illustrated in Figure 69B–9 and Figure 69B–10.

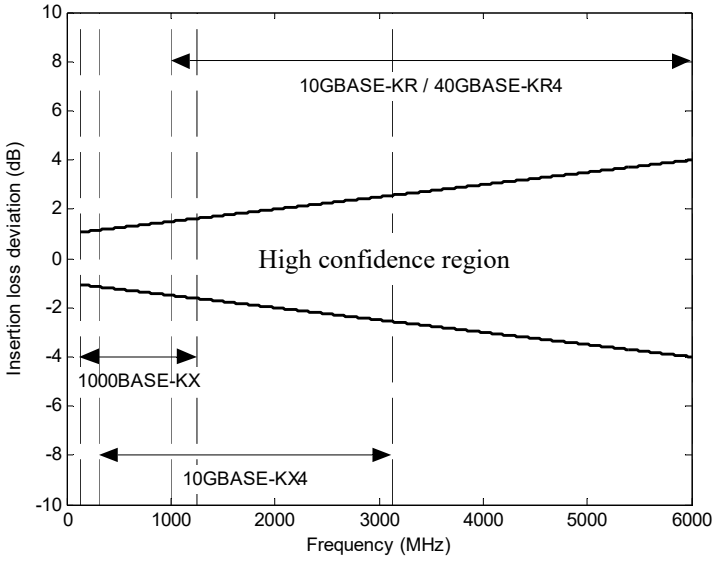

Figure 69B–9—Insertion loss deviation limits for 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, and 40GBASE-KR4

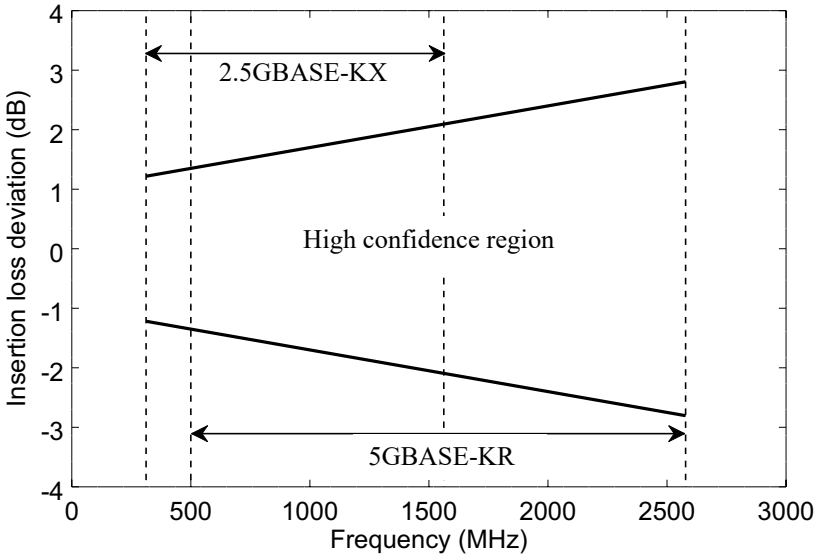

Figure 69B–10—Insertion loss deviation limits for 2.5GBASE-KX and 5GBASE-KR

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69B.4.5 Return loss

It is recommended that the channel return loss, *RL*, measured in dB at TP1 and TP4, be greater than or equal to $RL_{\min}$ as defined by Equation (69B–16) through Equation (69B–18).

$$RL(f) \geq RL_{\min}(f) = 12 \tag{69B–16}$$

for 50 MHz $\leq f <$ 275 MHz and

$$RL(f) \geq RL_{\min}(f) = 12 - 6.75\log_{10}\left(\frac{f}{275\ \text{MHz}}\right) \tag{69B–17}$$

for 275 MHz $\leq f <$ 3000 MHz and

$$RL(f) \geq RL_{\min}(f) = 5 \tag{69B–18}$$

for 3000 MHz $\leq f \leq$ 10312.5 MHz.

The recommendation applies from 50 MHz to the signaling speed of the PHY type of interest. The return loss limit is illustrated in Figure 69B–11 and Figure 69B–12.

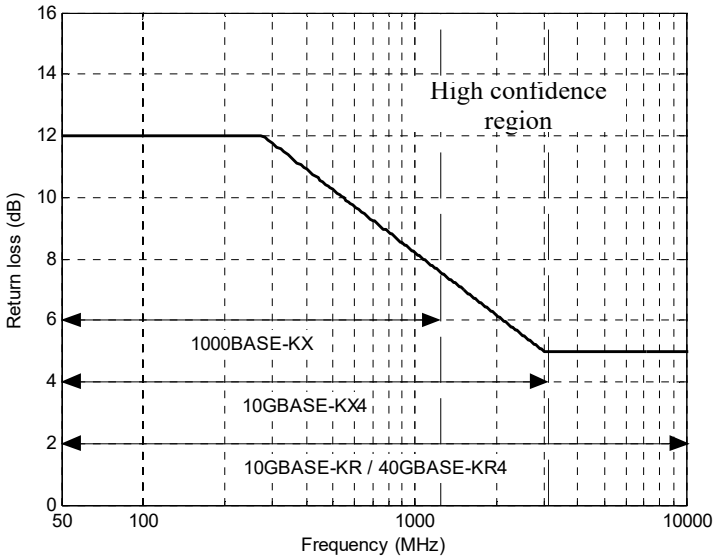

Figure 69B–11—Return loss limit for 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, and 40GBASE-KR4

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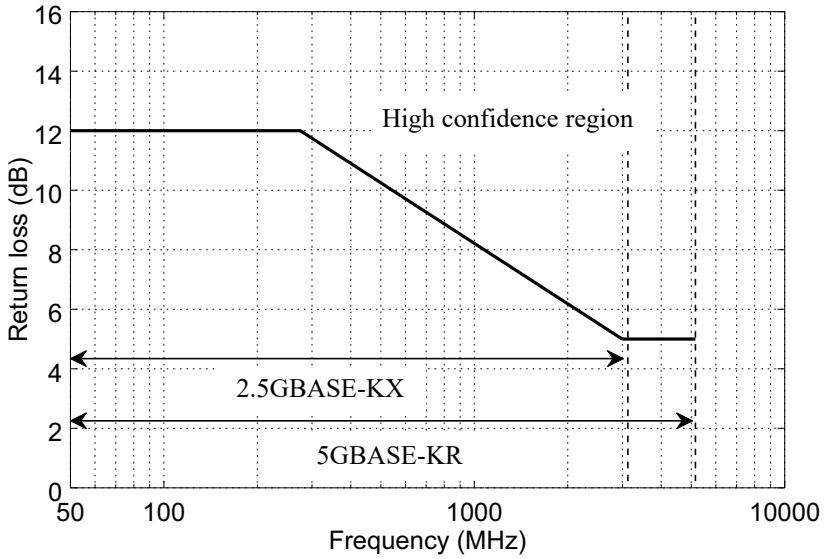

Figure 69B–12—Return loss limit for 2.5GBASE-KX and 5GBASE-KR

69B.4.6 Crosstalk

The following equations and informative model assume that aggressors and victim are driven by a compliant PHY of any type.

69B.4.6.1 Power sum differential near-end crosstalk (PSNEXT)

The differential near-end crosstalk at TP4 is calculated as the power sum of the individual NEXT aggressors (*PSNEXT*). *PSNEXT* is computed as shown in Equation (69B–19), where $NEXT_n$ is the crosstalk loss, in dB, of aggressor *n*. Note that for the case of a single aggressor, *PSNEXT* will be the crosstalk loss for that single aggressor.

$$PSNEXT(f) = -10\log\left(\sum_n 10^{-NEXT_n(f)/10}\right) \quad \text{(69B–19)}$$

69B.4.6.2 Power sum differential far-end crosstalk (PSFEXT)

The differential far-end crosstalk at TP4 is calculated as the power sum of the individual FEXT aggressors (*PSFEXT*). *PSFEXT* is computed as shown in Equation (69B–20), where $FEXT_{\mathrm{n}}$ is the crosstalk loss, in dB, of aggressor *n*. Note that for the case of a single aggressor, *PSFEXT* will be the crosstalk loss for that single aggressor.

$$PSFEXT(f) = -10\log\left(\sum_n 10^{-FEXT_n(f)/10}\right) \quad \text{(69B–20)}$$

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69B.4.6.3 Power sum differential crosstalk

The differential crosstalk at TP4 is calculated as the power sum of the individual NEXT and FEXT aggressors (*PSXT*). *PSXT* may be computed as shown in the following equation:

$$PSXT(f) = -10\log(10^{-PSNEXT(f)/10} + 10^{-PSFEXT(f)/10}) \quad (69B–21)$$

69B.4.6.4 Insertion loss to crosstalk ratio (ICR)

Insertion loss to crosstalk ratio (*ICR*) is the ratio of the insertion loss, measured from TP1 to TP4, to the total crosstalk measured at TP4. *ICR* may be computed from *IL* and *PSXT* as shown in the following equation:

$$ICR(f) = -IL(f) + PSXT(f) \quad (69B–22)$$

Assuming ICR is computed at N uniformly-spaced frequencies f_n spanning the frequency range f_a to f_b, ICR_{fit} may be computed using Equations (69B–23) through (69B–27). The values of f_a and f_b are dependent on port type and are provided in Table 69B–1.

$$x_{avg} = \frac{1}{N}\sum_n \log(f_n) \quad (69B–23)$$

$$ICR_{avg} = \frac{1}{N}\sum_n ICR(f_n) \quad (69B–24)$$

$$m_{ICR} = \frac{\sum_n (\log(f_n) - x_{avg})(ICR(f_n) - ICR_{avg})}{\sum_n (\log(f_n) - x_{avg})^2} \quad (69B–25)$$

$$b_{ICR} = ICR_{avg} - m_{ICR}x_{avg} \quad (69B–26)$$

$$ICR_{fit}(f) = m_{ICR}\log(f) + b_{ICR} \quad (69B–27)$$

It is recommended that ICR_{fit} be greater than or equal to ICR_{min}. For 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, and 40GBASE-KR, ICR_{min} is defined by Equation (69B–28). For 2.5GBASE-KX and 5GBASE-KR, ICR_{min} is defined by Equation (69B–29).

$$ICR_{fit}(f) \geq ICR_{min}(f) = 23.3 - 18.7\log_{10}\left(\frac{f}{5\text{ GHz}}\right) \quad (69B–28)$$

$$ICR_{fit}(f) \geq ICR_{min}(f) = 28 - 18\log_{10}\left(\frac{f}{2\text{ GHz}}\right) \quad (69B–29)$$

ICR_{min} is defined over the frequency range $f_a \leq f \leq f_b$. ICR_{fit} accounts for the worst-case differences in characteristics (e.g. amplitude, transition times) between the victim and aggressor transmitters. It also assumes a 3 dB signal-to-noise ratio penalty related to insertion loss deviation.

The insertion loss to crosstalk ratio limit for each port type is illustrated in Figure 69B–13 and Figure 69B–14.

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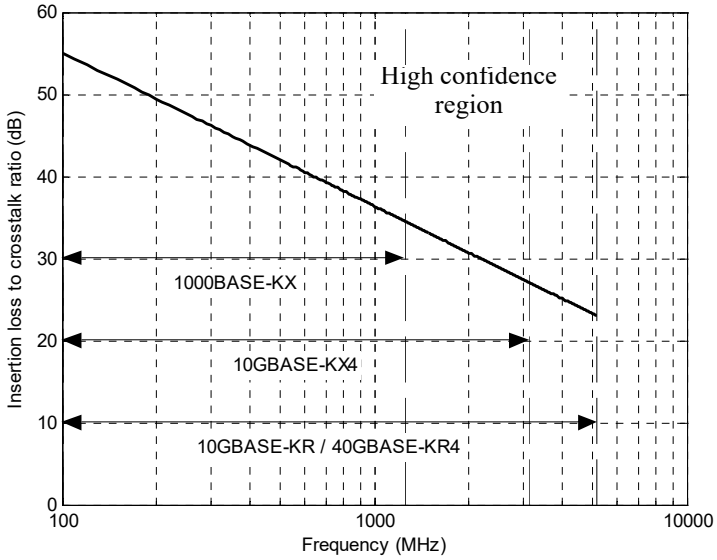

Figure 69B–13—Insertion loss to crosstalk ratio limit for 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, and 40GBASE-KR4

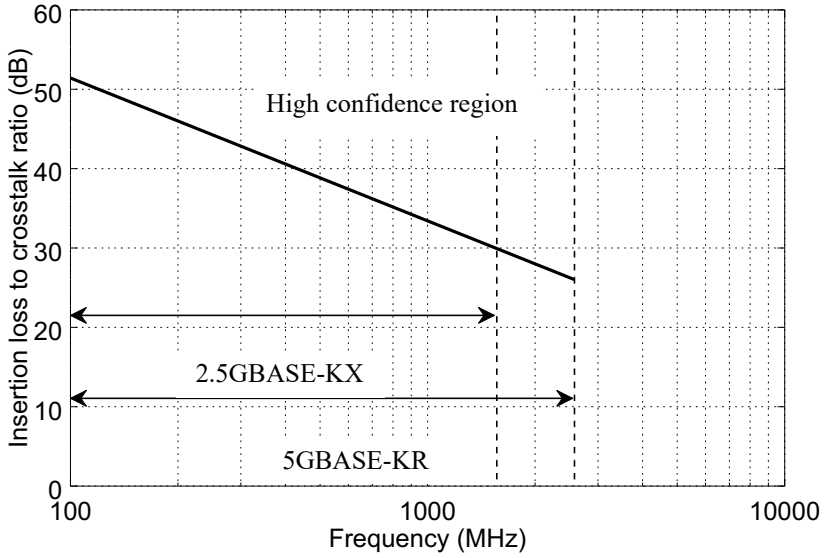

Figure 69B–14—Insertion loss to crosstalk ratio limit for 2.5GBASE-KX and 5GBASE-KR

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Annex 73A

(normative)

Next page message code field definitions

This Annex defines the Next Page message code fields for devices using Clause 73 Auto-Negotiation. The message code field of a message page used in Next Page exchange shall be used to identify the meaning of a message. Table 73A–1 identifies the types of messages that may be sent. As new messages are developed, this table will be updated accordingly.

The Message code field uses an 11-bit binary encoding that allows 2048 messages to be defined. All message codes not specified are reserved for IEEE use or allocation.

Table 73A–1—Message code field values

Message code	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message code description
1	0	0	0	0	0	0	0	0	0	0	1	Null Message
5	0	0	0	0	0	0	0	0	1	0	1	Organizationally Unique Identifier Tagged Message
6	0	0	0	0	0	0	0	0	1	1	0	AN device Identifier Tag Code
10	0	0	0	0	0	0	0	1	0	1	0	EEE Technology Message Code. EEE capability is advertised using unformatted message code field in the Message Next Page (see 73A.4).

73A.1 Message code 1—Null Message code

The Null Message code shall be transmitted during Next Page exchange when the Local Device has no further messages to transmit and the Link Partner is still transmitting valid Next Pages. See 73.7.7 for more details.

73A.2 Message code 5—Organizationally Unique Identifier (OUI) tag code

The OUI tag code message shall consist of a Message Next Page with the message code field 000 0000 0101 followed by one Unformatted Next Page defined as follows. The unformatted code field of Message Next Page 5 shall contain the most significant 11 bits of the OUI or CID (bits 23:13) in bits 26:16 (bits U10 to U0) with the most significant OUI or CID bit in bit 26 (bit U10) of the unformatted code field, the next 11 most significant bits of the OUI or CID (bits 12:2) in bits 42:32 (bit U26 to U16) with the most significant bit in bit 42 (bit U26). The unformatted code field of the Unformatted Next Page shall contain the remaining least significant 2 bits of the OUI or CID (bits 1:0) in bits 10:9 (U10 and U9) with OUI or CID bit 1 in bit 10 (bit U10) with the bits 8:0, 26:16 (bits U8 to U0, U21 to U11) as a user-defined user code value that is specific to the OUI or CID transmitted. The remaining unformatted code field bits in the Message Next Page and the Unformatted Next Page shall be sent as zero and ignored on receipt.

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For example, assume that a manufacturer's IEEE-assigned OUI/CID value is AC-DE-48 and the manufacturer-selected user-defined user code associated with the OUI or CID is 0xCE1FC (binary 1100 1110 0001 1111 1100). The message code values generated from these two numbers is encoded into the message Next Page and Unformatted Next Page codes, as specified in Figure 73A–1. For clarity, the position of the M bit[292] is illustrated.

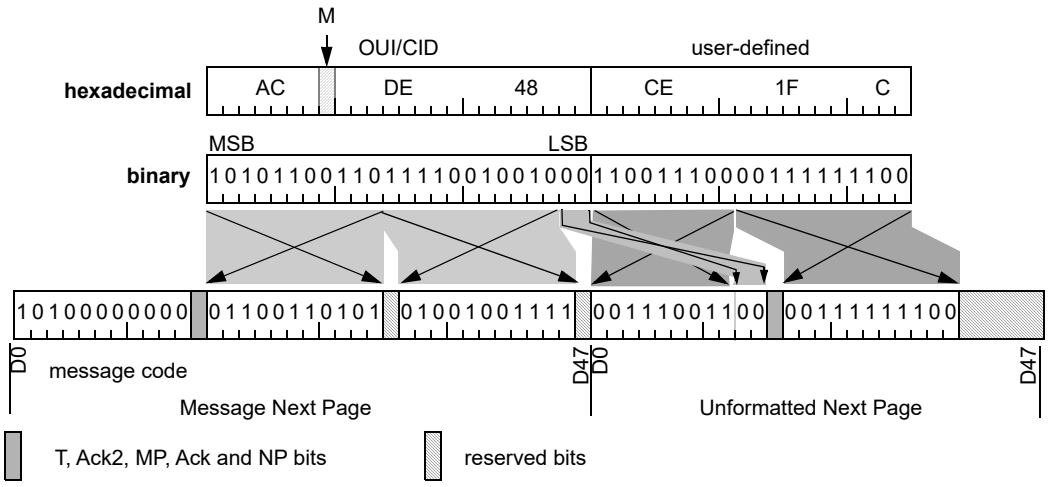

Figure 73A–1—Message code 5 sequence

NOTE—Figure 73A–1 shows the order Next Pages are transmitted, with the first transmitted Next Page shown in the leftmost position. This bits within each page are shown with the first transmitted bit (i.e., least significant bit) in the leftmost position. This is the same convention for bit order in the figures of Clause 73. Figure 28C–1 uses the opposite convention for bit order.

73A.3 Message code 6—AN device identifier tag code

The AN device ID tag code message shall consist of a Message Next Page with the message code field 000 0000 0110 followed by one Unformatted Next Page defined as follows. The unformatted fields of this message contain the AN device identifier. If a Clause 45 MDIO is implemented, the AN device identifier is accessible through registers 7.2 and 7.3 (see 45.2.7.3).

The unformatted code field of Message Next Page 6 shall contain the most significant 11 bits of the AN device identifier (7.2.15:5) in bits 26:16 (bits U0 to U10) with the most significant AN device identifier bit in bit 26 (bit U10) of the unformatted code field, and the next 11 most significant bits of the AN device identifier (bits 7.2.4:0 to 7.3.15:10) in bits 42:32 (bit U26 to U16) with the most significant bit in bit 42 (bit U26) of the unformatted code field. The unformatted code field of the Unformatted Next Page shall contain the remaining least significant 10 bits of the AN device identifier (bits 7.3.9:0) in bits 10:1 (bit U10 to U1). Bits 0, 26:16 (bits U0, U21 to U11) of the unformatted code field of the Unformatted Next Page shall contain a user-defined user code value that is specific to the device identifier transmitted. The remaining unformatted code field bits in the Message Next Page and the Unformatted Next Page shall be sent as zero and ignored on receipt.

[292]See IEEE Std 802, subclause 9.3

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73A.4 Message code 10—EEE technology message code

Multiple clauses use Next Page message code 10 as an identifier for EEE technology. The EEE technology code message shall consist of only a Message Next Page. The message code field, 000 0000 1010, shall be contained in bits 10:0. The contents of the unformatted code bits U31:U0 (D47:D16) shall be as defined in 45.2.7.14.

EEE capability negotiation is defined in 78.3.

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Annex 74A

(informative)

FEC block encoding examples

This annex provides an example FEC block encoding with (2112, 2080) code. See Table 74–1 for the format of the FEC block. The length of the FEC block is 2112 bits. Each FEC block contains 32 rows of 65 bits each; 64 bits of payload and 1 bit transcoding overhead (T bits). At the end of each block there is 32-bit overhead or parity check bits.

The data pattern in this annex is represented in a tabular form. For the tables within this annex the contents are transmitted from left to right within each row and from top to bottom between rows. The first bit out on the wire starts at the top left hand corner. Note that there is both binary representation and hexadecimal symbol representation in the table; in case of the hex symbol, the most significant bit of each hex symbol is sent first.

74A.1 Input to the FEC (2112,2080) Encoder

Table 74A–1 provides an example 64B/66B block stream at the input to the FEC (2112,2080) encoder. The example shows a stream of 32 64B/66B symbols generated from the output of the PCS layer when the link was sending out IDLE symbols.

Table 74A–1— 64B/66B block stream

Sync [0:1]	64 bit payload hex [0:63]	Sync [0:1]	64 bit payload hex [0:63]	Sync [0:1]	64 bit payload hex [0:63]	Sync [0:1]	64 bit payload hex [0:63]
10	40EA1E77EED301EC	10	AD5A3BF86D9ACF5C	10	DE55CB85DF0F7CA0	10	E6CCFF8E8212B1C6
10	D63BC6C309000638	10	70E3B0CE30E0497D	10	DC8DF31EC3AB4491	10	66FB9139C81CD37B
10	B57477D4F05E3602	10	8CFD495012947A31	10	E7777CF0C6D06280	10	44529CF4B4900528
10	85CE1D27750AD61B	10	456D5C71743F5C69	10	C1BF62E5DC5464B5	10	DC6011BE7EA1ED54
10	1CF92C450042A75F	10	CC4B940EAF3140DB	10	77BB612A7ABF401F	10	C22D341E90545D98
10	CE6DAF1F248BBD6D	10	DD22D0B3F9551ED6	10	574686C3F9E93898	10	2E52628F4A1282CE
10	F20C86D71944AAB1	10	55133C9333808A2C	10	1AA825D8B817DB4D	10	637959989F3021EB
10	976806641B26AAE9	10	6A37D4531B7ED5F2	10	53C3E96D3B12FB46	10	528C7EB8481BC969

74A.2 Output of the FEC (2112,2080) Encoder

Table 74A–2 provides one FEC block (65b block stream) at the output of the FEC (2112,2080) encoder. The corresponding 64B/66B block stream input to the encoder is as described in Table 74A–1. The example shows one FEC block, a stream of 32 65b symbols generated from the output of the FEC (2112,2080) encoder with 32 bit parity appended at the end of the FEC block.

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Table 74A–2— Transcoded FEC block

T bit [0]	64 bit payload hex [0:63]	T bit [0]	64 bit payload hex [0:63]	T bit [0]	64 bit payload hex [0:63]	T bit [0]	64 bit payload hex [0:63]
1	40EA1E77EED301EC	0	AD5A3BF86D9ACF5C	0	DE55CB85DF0F7CA0	1	E6CCFF8E8212B1C6
0	D63BC6C309000638	1	70E3B0CE30E0497D	1	DC8DF31EC3AB4491	1	66FB9139C81CD37B
0	B57477D4F05E3602	1	8CFD495012947A31	0	E7777CF0C6D06280	0	44529CF4B4900528
1	85CE1D27750AD61B	0	456D5C71743F5C69	1	C1BF62E5DC5464B5	0	DC6011BE7EA1ED54
1	1CF92C450042A75F	0	CC4B940EAF3140DB	1	77BB612A7ABF401F	0	C22D341E90545D98
0	CE6DAF1F248BBD6D	0	DD22D0B3F9551ED6	0	574686C3F9E93898	0	2E52628F4A1282CE
0	F20C86D71944AAB1	0	55133C9333808A2C	1	1AA825D8B817DB4D	0	637959989F3021EB
0	976806641B26AAE9	0	6A37D4531B7ED5F2	1	53C3E96D3B12FB46	1	528C7EB8481BC969
Parity hex [0:31] D96E7685							

74A.3 Output of the FEC (2112,2080) Encoder after scrambling with PN-2112 sequence

Table 74A–3 provides the data stream at the output of the FEC (2112,2080) encoder after the data is scrambled with the PN-2112 sequence as described in 74.7.4.4.1. The corresponding 2112 bit FEC block input to the scrambler is as described in Table 74A–2. The example shows the stream of data in 64 bit format (33 64b symbols) generated from the output of the FEC (2112,2080) encoder after the PN-2112 scrambler.

Table 74A–3— FEC block scrambled with PN-2112 sequence

	64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]
	5F8AF0C4083CD5B6		2B57DBAB4E33E17D		B1354680BBE0BAC1		4193315242CB81B6
	CC1BA1C9F7B7FE64		90838EC46D969470		A913B019C27F5689		7633F46EC762B6D9
	D1E410905587D0E4		F9B66A42540AF04A		9909B64535A725B8		5005107C48B4A6AA
	F9D684CE4396F7A9		1B26E0A025C5D0FD		A4F2C62BC4611217		3638DC7504EA755E
	13FE232E3CDD2A84		5C5118ED10F6FFD8		5077FBA23970C87D		52EC1279D355FC57
	48263899CC6652DA		F746EC8B31BD6B40		006F5809784C86A7		989B9BD1AAB70F0F
	57D99A87B9A9CC74		09FFB2754F318F33		CA8FCE7654FB1E57		03A9C3ACC87E6CDD
	B2574BE1E93FCC9A		26C4FDE242DF5CA6		C645FD2BF2D3D525		5B25E6D7F9D78153
	BD49683CD87B293A						

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74A.4 Output of the PN-2112 sequence generator

Table 74A–4 provides the PN-2112 sequence of length 2112 bits as described in 74.7.4.4.1.

Table 74A–4— PN-2112 sequence

	64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]
	FFFFFFFFFF555540		00015555555552AA		AAFFFFF000015555		5FFFFEAAAAEAAAAA
	AAAA7FFFEFFFFE55		5540000755551555		5EAAABFFFFF80000		55550FFFFEAAAA0A
	AABEAAABBFFFFFFF		F8D55510000E5554		155558AAABBFFFB4		0001555587FFEFAA
	AB5AAABEAAAD5FFF		ABFFF51554000000		D555455501AAAABF		FF52001515540BFF
	FEAAAD52AAFFAAA5		0FFEABFFF5F55414		004115555555872A		BAEFFE5B00141552
	0DFFBEEAA11EABFE		AAAD87FFBAFFA4A5		541400A7F5410154		4AEAABFFF8D58045
	455B54FEBFEAA7F8		ABAAEAE00BFEABFF		2AAD455501FFA540		0152AA0AFFEBF554
	41555555527FFFBA		FFF1AAABEA000DEA		ABBEAAE1555407FF		2D00105AAB5BFFEB
	F552A15501155FBF						

74A.5 Output of the FEC (2112,2080) Encoder to Support Rapid Block during the wake state in EEE (optional)

If the optional EEE function is supported (see Clause 78) then the reverse gearbox of the remote FEC encoder will be receiving unscrambled data. PCS sublayer will be encoding /I/ during the wake state, which produces the deterministic FEC frame.

Table 74A–5 provides the data stream at the output of the FEC (2112,2080) encoder after the data is scrambled with the PN-2112 sequence as described in 74.7.4.4.1. The example shows the stream of data in 64 bit format (33 64b symbols) generated from the output of the FEC (2112,2080) encoder after the PN-2112 scrambler.

74A.6 Output of the FEC (2112,2080) Encoder to Support Rapid Block during the refresh state in EEE (optional)

If the optional EEE capability is supported (see Clause 78) then the reverse gearbox of the remote FEC encoder will be receiving unscrambled data. PCS sublayer will be encoding /LI/ during the refresh state, which produces the deterministic FEC frame.

Table 74A–6 provides the data stream at the output of the FEC (2112,2080) encoder after the data is scrambled with the PN-2112 sequence as described in 74.7.4.4.1. The example shows the stream of data in 64 bit format (33 64b symbols) generated from the output of the FEC (2112,2080) encoder after the PN-2112 scrambler.

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Table 74A–5—FEC block scrambled with PN-2112 sequence for the wake state

	64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]
	C3FFFFFFF555540		1E015555555552AA		A5FFFFF000015555		587FFEAAAAEAAAAA
	A96A7FFFEFFFFE55		54A0000755551555		5E5AABFFFFF80000		552D0FFFFEAAAA0A
	AA82AAABBFFFFFFF		F8CB5510000E5554		155A58AAABBFFFB4		0006D55587FFEFAA
	AB596ABEAAAD5FFF		ABFE151554000000		D555B55501AAAABF		FF52781515540BFF
	FEAA9152AAFFAAA5		0FFEB5FFF5F55414		00411A555555872A		BAEFF9DB00141552
	0DFFBD2AA11EABFE		AAAD861FBAFFA4A5		54140057F5410154		4AEAAB87F8D58045
	455B54C2BFEAA7F8		ABAAEAFE0BFEABFF		2AAD455A01FFA540		0152AA0D7FEBF554
	41555556927FFFBA		FFF1AAAA0A000DEA		ABBEAAE1A55407FF		2D00105AD35BFFEB
	F552A155ABB5586A						

Table 74A–6—FEC block scrambled with PN-2112 sequence for the refresh state

	64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]
	C3CF9F3E7C535958		1E19653594D654A6		A5F3E7C060C0D653		5879F2B29A8A6B29
	A96979F3F7CF9E94		D4A18301594D2535		9E5A6A7CF9F41830		352D6F3E7DACA612
	9A829ACB7E7CF9F3		E0CB4D2060CFD652		195A54B29BDF3E37		0606D3599FCF8F6B
	285969B8A6B56F9F		6A7E1496520C1830		B595B59482ACA6A7		CF327875D4D70DF3
	E69A9162CA3E29A3		03E6B5E7C5959597		064D1A594D65E7EB		39E9F9DD0C0C2532
	CC7CBD29A712B3CE		CA6C061E39F9A8BD		6474C05734C20758		52DACB8798140343
	494364C28F8A667B		ADA6F2FE13CECB3E		A9AB495A0DE79520		C0D1AC0D79E7ED64
	2194D6569179F3A2		CF916B2A0B830BE6		B38ECA21A59584F9		2118203AD33B3E68
	F35EB9658ED5D943						

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Annex 75A

(informative)

Dual-rate receiver implementation

75A.1 Overview

The OLT receiver supports burst mode operation. If the OLT supports a single upstream data rate e.g., only 1 Gb/s or 10 Gb/s, the receiver can be designed to handle the designated upstream data rate and line code. However, if the OLT supports both 1 Gb/s and 10 Gb/s upstream data rates, the OLT receiver supports both data rates via TDMA.

From a topological point of view, the PMD has a single optical input, sensitive to 1260–1360 nm signal, and two corresponding derived electrical outputs: 1.25 GBd and 10.3125 GBd. Thus, at a certain point in the implementation it is necessary to introduce a signal split, where the location of such a signal split is an implementation choice. The incoming signal can be split in the optical domain and fed into two, independent photodetectors as shown in Figure 75A–1(a). Alternatively, the signal can be detected using a single photodetector as shown in Figure 75A–1(b) and then split in the electrical domain after the transimpedance amplifier (TIA) block.

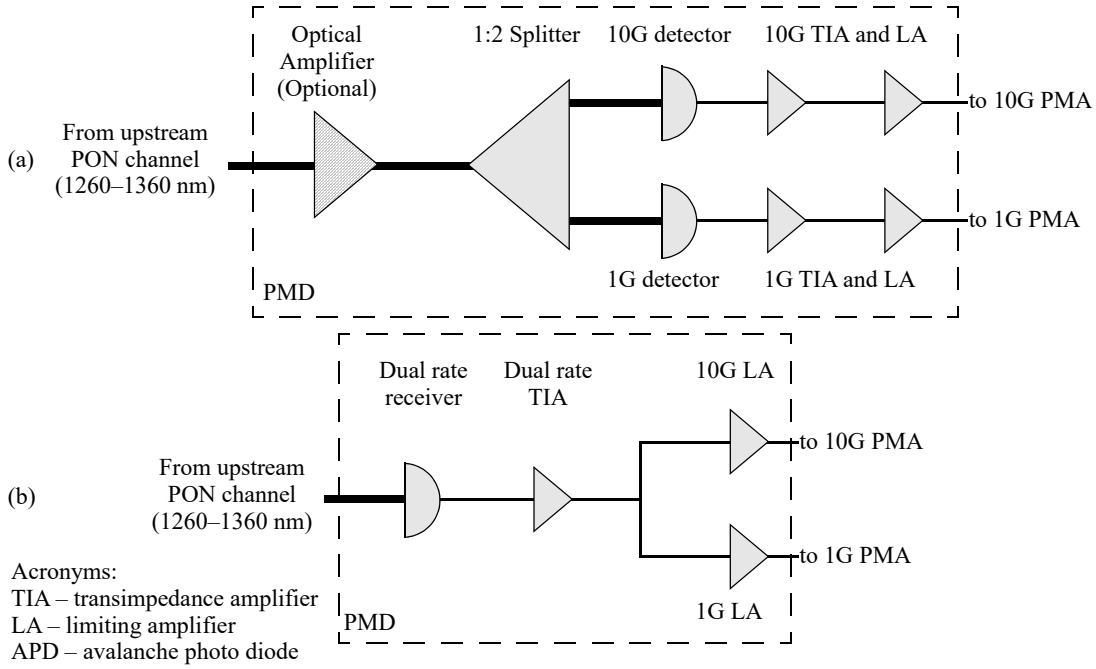

Figure 75A–1—Dual-rate PMD topologies with the split in the (a) optical domain, (b) electrical domain

When the incoming signal is split in the optical domain, it is possible to design each PMD channel specifically to match the signaling speed, offering optimum sensitivity for both 1 Gb/s and 10 Gb/s signals. However, the additional 1:2 optical splitter presented in Figure 75A–1(a) degrades the sensitivity of the

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PMD by introducing additional loss and lowering the power of the optical signal. Such a sensitivity reduction may be tolerable in the PX10/PR10/PRX10 type PMDs, but the more stringent power budgets including PX20, PR20, PRX20, PX30, PR30, PRX30, PX40, PR40, and PRX40, may be very challenging or even impossible to implement with such an additional loss on the OLT receiver side.

When the incoming signal is split in the electrical domain, only one photodetector and one TIA unit is used. The resulting optical sensitivity theoretically can be maintained without the need for optical amplification, reducing the complexity of the OLT receiver. However, the photodetector and TIA cope with both data rates in quick succession, switching between 1 Gb/s and 10 Gb/s bursts during the guardband. The key aspect here is that the detector-TIA bandwidth directly affects the sensitivity. If the circuit parameters of the detector-TIA can be rapidly adapted to the correct value, optimum sensitivity can be maintained. There are several implementation choices in this regard, three examples of which are shown in Figure 75A–2(a)–(c):

a) This implementation fixes the detector parameters at some predefined value, resulting in the reduction of the OLT receiver sensitivity by approximately 2 dB. However, it should be noted that this penalty can be divided in such a way that both 1 Gb/s and 10 Gb/s sensitivities are 1 dB lower than their ideal values.
b) This implementation fixes the avalanche photo diode (APD) bias, but switches the TIA transimpedance depending on the target signaling speed for the given incoming burst, resulting in the reduction of the receiver sensitivity by approximately 1 dB. The said sensitivity penalty could be subdivided to both data rates by setting the APD bias to a compromise value.
c) This implementation switches both the APD bias and the TIA transimpedance depending on the signaling speed of the incoming burst. This results in ideal performance at both 1 Gb/s and 10 Gb/s data rates. However, it is the most complex implementation in terms of the number of elements and the control complexity.

In the case of dynamic detector designs, it is necessary to determine the data rate of the incoming burst before adjusting the dynamic detector to match the target data rate.

In general, the PMD layer does not have prior knowledge of which data rate is used in the given burst; such information is available only to the MAC Client and is not available to the PMD sublayer. Therefore, some sort of data rate detector circuit should be utilized. One of the simple methods is based on measuring the spectral energy content of the received signal at frequencies well above 1.25 GHz (e.g., in the range of 2–10 GHz). The 1 Gb/s signal has very little energy in this frequency range, while the 10 Gb/s signal has ample energy there. Thus, the presence of 5 GHz energy indicates that a 10 Gb/s signal is incident.

In the dual-rate PMD topologies with the split in the electrical domain, the 10 Gb/s detector and TIA are implemented for receiving both 1 Gb/s and 10 Gb/s signals. Therefore, the damage threshold (max) of the 1/10 Gb/s dual-rate receiver should comply with the 10 Gb/s receiver specification in Table 75–6. Those values for 1000BASE–PX10–D in Table 60–5, for 1000BASE–PX20–D in Table 60–8, for 1000BASE–PX30–D in Table 60–11, and for 1000BASE–PX40–D in Table 60–13, and also those of 10/1GBASE–PRX–D1, 10/1GBASE–PRX–D2, 10/1GBASE–PRX–D3, and 10/1GBASE–PRX–D4 in Table 75–5 cannot be applied for dual-rate OLT receivers.

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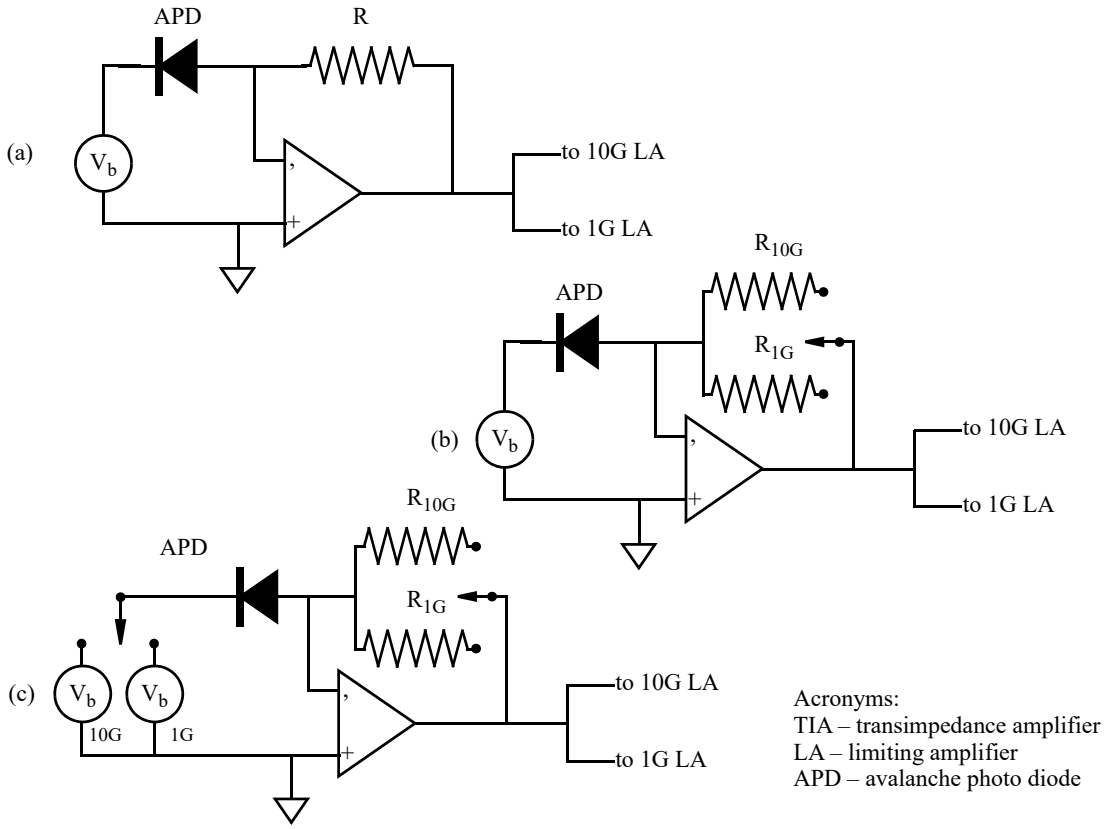

Figure 75A–2—Dual rate APD–TIA implementations:
(a) static, (b) half–dynamic, (c) fully–dynamic

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Annex 75B

(informative)

Illustrative channels and penalties for 10GBASE-PR and 10/1GBASE-PRX power budget classes

75B.1 Overview

Illustrative power budgets for PR10, PR20, PR30, and PR40 power budget classes are shown in Table 75B–1. Illustrative power budgets for PRX10, PRX20, PRX30, and PRX40 power budget classes are shown in Table 75B–2.

NOTE—The budgets include an allowance for –12 dB reflection at the receiver.

75B.2 Wavelength allocation

The wavelength allocation plan for 10G–EPON systems is specified below.

75B.2.1 Downstream wavelength allocation

The 1 Gb/s downstream transmission uses the 1480–1500 nm wavelength band, as specified in Clause 60. The 10 Gb/s downstream transmission uses the 1575–1580 nm wavelength band, as specified in Clause 75. An OLT supporting both downstream channels may multiplex the output of the two transmitters using a WDM coupler, while the optical filters at an ONU are tuned to receive only one downstream wavelength.

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Table 75B–1—Illustrative 10GBASE–PR channel insertion loss and penalties (symmetric-rate, 10 Gb/s power budget classes)

Description[a]	PR10		PR20		PR30		PR40		Unit
	US	DS	US	DS	US	DS	US	DS	
Fiber Type[b]	IEC 60793–2 B1.1, B1.3 SMF ITU–T G.652, G.657 SMF								
Measurement wavelength for fiber	1270	1577[c]	1270	1577[c]	1270	1577[c]	1270	1577[c]	nm
Nominal distance[d]	10		20		20		20		km
Available power budget[e]	23	21.5	27	25.5	32	30.5	35	34.5	dB
Channel insertion loss (max)[f]	20		24		29		33		dB
Channel insertion loss (min)[g]	5		10		15		18		dB
Allocation for penalties[h]	3	2.5[i]	3	1.5	3	1.5	2	1.5	dB
Optical return loss of ODN (min)	20								dB

[a]US stands for Upstream, DS stands for Downstream.
[b]Other fiber types are acceptable if the resulting ODN meets channel insertion loss and dispersion requirements.
[c]The nominal transmit wavelength is 1577 nm.
[d]Nominal distance refers to the expected maximum distance a PMD is capable of achieving in a typical ODN. Numerous ODN implementation practices may result in longer or shorter distances being actually achievable in a user's network.
[e]The available power budget assumes a BER at the PMD service interface of 10^{-3}. The required BER of 10^{-12} at the PCS service interface is achieved by the FEC function of the PCS.
[f]The channel insertion loss is based on the cable attenuation at the target distance and nominal measurement wavelength. The channel insertion loss also includes the loss for connectors, splices and other passive components such as splitters.
[g]The power budgets for PR10, PR20, PR30, and PR40 power budget classes are such that a minimum insertion loss is assumed between transmitter and receiver. This minimum attenuation is required for PMD testing.
[h]The allocation for penalties is the difference between the available power budget and the channel insertion loss; insertion loss difference between nominal and worst case operating wavelength is considered a penalty. This allocation may be used to compensate for transmission related penalties. Further details are given in 75.7.2.
[i]The extra 1 dB of penalty here is to unify the downstream Tx and Rx specifications.

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Table 75B–2—Illustrative 10/1GBASE–PRX channel insertion loss and penalties (asymmetric-rate, 10 Gb/s downstream, 1 Gb/s upstream power budget classes)

Description[a]	PRX10		PRX20		PRX30		PRX40		Unit
	US	DS	US	DS	US	DS	US	DS	
Fiber Type[b]	IEC 60793–2 B1.1, B1.3 SMF ITU–T G.652, G.657 SMF								
Measurement wavelength for fiber	1310	1577[c]	1310	1577[c]	1310	1577[c]	1310	1577[c]	nm
Nominal distance[d]	10		20		20		20		km
Available power budget	23	21.5[e]	26	25.5[e]	30.4	30.5[e]	34	34.5[e]	dB
Channel insertion loss (max)[f]	20		24		29		33		dB
Channel insertion loss (min)[g]	5		10		15		18		dB
Allocation for penalties[h]	3	2.5[i]	2	1.5	1.4	1.5	1	1.5	dB
Optical return loss of ODN (min)	20								dB

[a]US stands for Upstream, DS stands for Downstream.
[b]Other fiber types are acceptable if the resulting ODN meets channel insertion loss and dispersion requirements.
[c]The nominal transmit wavelength is 1577 nm.
[d]Nominal distance refers to the expected maximum distance a PMD is capable of achieving in a typical ODN. Numerous ODN implementation practices may result in longer or shorter distances being actually achievable in a user's network.
[e]The available power budget assumes a BER at the PMD service interface of 10^{-3}. The required BER of 10^{-12} at the PCS service interface is achieved by the FEC function of the PCS.
[f]The channel insertion loss is based on the cable attenuation at the target distance and nominal measurement wavelength. The channel insertion loss also includes the loss for connectors, splices and other passive components such as splitters.
[g]The power budgets for PRX10, PRX20, PRX30, and PRX40 power budget classes are such that a minimum insertion loss is assumed between transmitter and receiver. This minimum attenuation is required for PMD testing.
[h]The allocation for penalties is the difference between the available power budget and the channel insertion loss; insertion loss difference between nominal and worst case operating wavelength is considered a penalty. This allocation may be used to compensate for transmission related penalties. Further details are given in 75.7.2.
[i]The extra 1 dB of penalty here is to unify the downstream Tx and Rx specifications.

75B.2.2 Upstream wavelength allocation

The 1 Gb/s upstream transmission uses the 1260 to 1360 nm wavelength band for 1000BASE–PX10–U, 1000BASE–PX20–U, 1000BASE–PX30–U, 10/1GBASE–PRX–U1, 10/1GBASE–PRX–U2, and 10/1GBASE–PRX–U3 compliant ONUs, and the 1290 to 1330 nm wavelength for 1000BASE–PX40–U and 10/1GBASE–PRX–U4 compliant ONUs, as specified in Clause 60. The 10 Gb/s upstream transmission uses the 1260 to 1280 nm wavelength band, as specified in Clause 75. The two wavelength bands overlap, thus WDM channel multiplexing cannot be used to separate the 1G upstream links operating in 1260 to 1360 nm wavelength band from 10G upstream links operating in 1260 to 1280 nm wavelength band.

An OLT supporting both upstream data rates uses TDMA techniques to avoid collisions between transmissions originating from different ONUs, resulting in a dual-rate burst–mode reception as discussed in 75.6.

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Annex 75C

(informative)

Jitter at TP1 to TP8 for 10GBASE–PR and 10/1GBASE–PRX

75C.1 Overview

The jitter values at frequencies above 4 MHz are listed in Table 75C–1 for PR10, PR20, PR30, PR40, PRX10, PRX20, PRX30, and PRX40 downstream and in Table 75C–2 for PR10, PR20, PR30, and PR40 upstream. Those in Table 75C–3 relate to the jitter frequencies above 637 kHz for PRX10, PRX20, PRX30, and PRX40 upstream.

Table 75C–1—10GBASE–PR and 10/1GBASE–PRX downstream jitter budgets

Reference point	DJ (UI p–p)	RJ (UI p–p)	TJ (UI p–p)
TP1	0.09	0.14	0.23
TP2	0.19	0.20	0.39
TP3	0.24	0.20	0.44
TP4	0.42	0.34	0.76

NOTE 1—Jitter measurements should be performed at nominal operating conditions.
NOTE 2—BER conditions for TP1, TP2, and TP3 are 10^{-12}, for TP4 is 10^{-3}.
NOTE 3—All jitter values relate to high frequency (>4 MHz) jitter.
NOTE 4—0.1 UI of sinusoidal jitter stress is assumed at the receiver.
NOTE 5—The Gaussian jitter is assumed to be a weak function of BER.

The upstream jitter transfer function is defined Equation (75C-1). The jitter gain curve and the corresponding jitter gain values are shown in Figure 75C–1 where the jitter gain P and the jitter corner frequency f_c are specified in Table 75C–4 for PR10, PR20, PR30, and PR40, and in Table 75C–5 for PRX10, PRX20, PRX30, and PRX40, respectively.

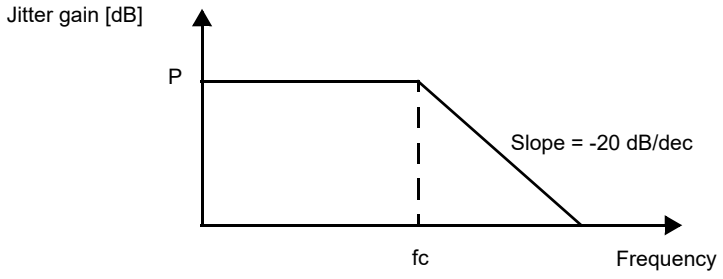

Figure 75C–1—Jitter gain curve values for 10GBASE–PR10/1GBASE-PRX

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Table 75C–2—10GBASE–PR upstream jitter budgets

Reference point	DJ (UI p–p)	RJ (UI p–p)	TJ (UI p–p)
TP5	0.12	0.16	0.28
TP6	0.30	0.21	0.51
TP7	0.35	0.21	0.56
TP8	0.53	0.23	0.76

NOTE 1—Jitter measurements should be performed at nominal operating conditions.
NOTE 2—BER conditions for TP5, TP6, and TP7 are 10^{-12}, for TP8 is 10^{-3}.
NOTE 3—All jitter values relate to high frequency (>4 MHz) jitter.
NOTE 4—0.1 UI of sinusoidal jitter stress is assumed at the receiver.
NOTE 5—The Gaussian jitter is assumed to be a weak function of BER.

Table 75C–3—10/1GBASE–PRX upstream jitter budgets

Reference point	Total jitter	
	UI	ps
TP5	0.24	192
TP6	0.40	320
TP7	0.49	392
TP8	0.67	536

Table 75C–4—Jitter gain curve values for 10GBASE–PR

	Value	Unit
P	0.3	dB
f_c	8	MHz

Table 75C–5—Jitter gain curve values for 10/1GBASE–PRX

	Value	Unit
P	0.3	dB
f_c	1274	kHz

$$\text{Jitter Transfer} = 20\log_{10}\left[\frac{\text{Jitter on upstream signal (UI)}}{\text{Jitter on downstream signal (UI)}} \times \frac{\text{downstream\_line\_rate}}{\text{upstream\_line\_rate}}\right] \quad (75C\text{-}1)$$

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Annex 76A

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FEC Encoding example

76A.1 Introduction and rationale

This Annex provides an example of FEC encoding with RS (255,223) code. See 76.3.2.4.3 for the format of the FEC codeword.[293]

76A.2 64B/66B block input

Table 76A–1 provides an example of a 64B/66B block stream received at the input to the RS (255,223) encoder. The example shows a stream of 27 scrambled 64B/66B blocks generated from the output of the PCS layer when the link was sending out Idles.

The 66 bit blocks in the Table 76A–1 are transmitted from left to right within each row and from top to bottom between rows. The 64 bit payload portion of the 66 bit block is described as a series of hexadecimal octets—the left-most octet of each payload portion is transmitted first. Bits within each octet of the payload are transmitted in least-significant bit-first order (i.e., the right-most bit of each octet is transmitted first). Thus, the first ten bits transmitted are: 10 0100 0000 …

[293]The tables in this annex are available at https://standards.ieee.org/downloads/802.3/.

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Table 76A–1—Example 64B/66B block stream at the input to FEC encode[a]

Sync [0:1]	64 bit payload [7:0]-[15:8]-[23:16]-[31:24]-[39:32]-[47:40]-[55:48]-[63:56]
10	02-57-78-EE-77-CB-80-37
10	B5-5A-DC-1F-B6-59-F3-3A
10	7B-AA-D3-A1-FB-F0-3E-05
10	67-33-FF-71-41-48-8D-63
10	6B-DC-63-C3-90-00-60-1C
10	0E-C7-0D-73-0C-07-92-BE
10	3B-B1-CF-78-C3-D5-22-89
10	66-DF-89-9C-13-38-CB-DE
10	AD-2E-EE-2B-0F-7A-6C-40
10	31-BF-92-0A-48-29-5E-8C
10	E7-EE-3E-0F-63-0B-46-01
10	22-4A-39-2F-2D-09-A0-14
10	A1-73-B8-E4-AE-50-6B-D8
10	A2-B6-3A-8E-2E-FC-3A-96
10	83-FD-46-A7-3B-2A-26-AD
10	3B-06-88-7D-7E-85-B7-2A
10	38-9F-34-A2-00-42-E5-FA
10	33-D2-29-70-F5-8C-02-DB
10	EE-DD-86-54-5E-FD-02-F8
10	43-B4-2C-78-09-2A-BA-19
10	73-B6-F5-F8-24-D1-BD-B6
10	BB-44-0B-CD-9F-AA-78-6B
10	EA-62-61-C3-9F-97-1C-19
10	74-4A-46-F1-52-48-41-73
10	4F-30-61-EB-98-22-55-8D
10	AA-C8-3C-C9-CC-01-51-34
10	58-15-A4-1B-1D-E8-DB-B2

[a]64 bit payload values are shown in hexadecimal notation.

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76A.3 66 bit block input in binary format

Table 76A–2—Example 64B/66B block stream at the input to FEC encoder (binary)

Sync [0:1]	64 bit payload (transmitted from left to right)
10	0100 0000 1110 1010 0001 1110 0111 0111 1110 1110 1101 0011 0000 0001 1110 1100
10	1010 1101 0101 1010 0011 1011 1111 1000 0110 1101 1001 1010 1100 1111 0101 1100
10	1101 1110 0101 0101 1100 1011 1000 0101 1101 1111 0000 1111 0111 1100 1010 0000
10	1110 0110 1100 1100 1111 1111 1000 1110 1000 0010 0001 0010 1011 0001 1100 0110
10	1101 0110 0011 1011 1100 0110 1100 0011 0000 1001 0000 0000 0000 0110 0011 1000
10	0111 0000 1110 0011 1011 0000 1100 1110 0011 0000 1110 0000 0100 1001 0111 1101
10	1101 1100 1000 1101 1111 0011 0001 1110 1100 0011 1010 1011 0100 0100 1001 0001
10	0110 0110 1111 1011 1001 0001 0011 1001 1100 1000 0001 1100 1101 0011 0111 1011
10	1011 0101 0111 0100 0111 0111 1101 0100 1111 0000 0101 1110 0011 0110 0000 0010
10	1000 1100 1111 1101 0100 1001 0101 0000 0001 0010 1001 0100 0111 1010 0011 0001
10	1110 0111 0111 0111 0111 1100 1111 0000 1100 0110 1101 0000 0110 0010 1000 0000
10	0100 0100 0101 0010 1001 1100 1111 0100 1011 0100 1001 0000 0000 0101 0010 1000
10	1000 0101 1100 1110 0001 1101 0010 0111 0111 0101 0000 1010 1101 0110 0001 1011
10	0100 0101 0110 1101 0101 1100 0111 0001 0111 0100 0011 1111 0101 1100 0110 1001
10	1100 0001 1011 1111 0110 0010 1110 0101 1101 1100 0101 0100 0110 0100 1011 0101
10	1101 1100 0110 0000 0001 0001 1011 1110 0111 1110 1010 0001 1110 1101 0101 0100
10	0001 1100 1111 1001 0010 1100 0100 0101 0000 0000 0100 0010 1010 0111 0101 1111
10	1100 1100 0100 1011 1001 0100 0000 1110 1010 1111 0011 0001 0100 0000 1101 1011
10	0111 0111 1011 1011 0110 0001 0010 1010 0111 1010 1011 1111 0100 0000 0001 1111
10	1100 0010 0010 1101 0011 0100 0001 1110 1001 0000 0101 0100 0101 1101 1001 1000
10	1100 1110 0110 1101 1010 1111 0001 1111 0010 0100 1000 1011 1011 1101 0110 1101
10	1101 1101 0010 0010 1101 0000 1011 0011 1111 1001 0101 0101 0001 1110 1101 0110
10	0101 0111 0100 0110 1000 0110 1100 0011 1111 1001 1110 1001 0011 1000 1001 1000
10	0010 1110 0101 0010 0110 0010 1000 1111 0100 1010 0001 0010 1000 0010 1100 1110
10	1111 0010 0000 1100 1000 0110 1101 0111 0001 1001 0100 0100 1010 1010 1011 0001
10	0101 0101 0001 0011 0011 1100 1001 0011 0011 0011 1000 0000 1000 1010 0010 1100
10	0001 1010 1010 1000 0010 0101 1101 1000 1011 1000 0001 0111 1101 1011 0100 1101

76A.4 RS(255,223) input buffer in Binary Format

The input buffer to the RS function begins with 29 ‘0’ bits followed by the 27 65 bit inputs as illustrated in Figure 76–12 and Figure 76–13.

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Table 76A–3—Input buffer to the FEC encoder (binary)

0000 0000 0000 0000 0000 0000 0000 0001 0000 0011 1010 1000 0111 1001 1101 1111
1011 1011 0100 1100 0000 0111 1011 0001 0101 1010 1011 0100 0111 0111 1111 0000
1101 1011 0011 0101 1001 1110 1011 1000 1101 1110 0101 0101 1100 1011 1000 0101
1101 1111 0000 1111 0111 1100 1010 0000 0111 0011 0110 0110 0111 1111 1100 0111
0100 0001 0000 1001 0101 1000 1110 0011 0011 0101 1000 1110 1111 0001 1011 0000
1100 0010 0100 0000 0000 0001 1000 1110 0000 1110 0001 1100 0111 0110 0001 1001
1100 0110 0001 1100 0000 1001 0010 1111 1010 1101 1100 1000 1101 1111 0011 0001
1110 1100 0011 1010 1011 0100 0100 1001 0001 0011 0011 0111 1101 1100 1000 1001
1100 1110 0100 0000 1110 0110 1001 1011 1101 1010 1101 0101 1101 0001 1101 1111
0101 0011 1100 0001 0111 1000 1101 1000 0000 1001 0001 1001 1111 1010 1001 0010
1010 0000 0010 0101 0010 1000 1111 0100 0110 0010 1110 0111 0111 0111 0111 1100
1111 0000 1100 0110 1101 0000 0110 0010 1000 0000 0010 0010 0010 1001 0100 1110
0111 1010 0101 1010 0100 1000 0000 0010 1001 0100 0010 0001 0111 0011 1000 0111
0100 1001 1101 1101 0100 0010 1011 0101 1000 0110 1100 1000 1010 1101 1010 1011
1000 1110 0010 1110 1000 0111 1110 1011 1000 1101 0010 1100 0001 1011 1111 0110
0010 1110 0101 1101 1100 0101 0100 0110 0100 1011 0101 0110 1110 0011 0000 0000
1000 1101 1111 0011 1111 0101 0000 1111 0110 1010 1010 0000 0111 0011 1110 0100
1011 0001 0001 0100 0000 0001 0000 1010 1001 1101 0111 1101 1001 1000 1001 0111
0010 1000 0001 1101 0101 1110 0110 0010 1000 0001 1011 0110 0111 0111 1011 1011
0110 0001 0010 1010 0111 1010 1011 1111 0100 0000 0001 1111 0110 0001 0001 0110
1001 1010 0000 1111 0100 1000 0010 1010 0010 1110 1100 1100 0011 0011 1001 1011
0110 1011 1100 0111 1100 1001 0010 0010 1110 1111 0101 1011 0101 1011 1010 0100
0101 1010 0001 0110 0111 1111 0010 1010 1010 0011 1101 1010 1100 0101 0111 0100
0110 1000 0110 1100 0011 1111 1001 1110 1001 0011 1000 1001 1000 0001 0111 0010
1001 0011 0001 0100 0111 1010 0101 0000 1001 0100 0001 0110 0111 0011 1100 1000
0011 0010 0001 1011 0101 1100 0110 0101 0001 0010 1010 1010 1100 0100 1010 1010
0010 0110 0111 1001 0010 0110 0110 0111 0000 0001 0001 0100 0101 1000 0001 1010
1010 1000 0010 0101 1101 1000 1011 1000 0001 0111 1101 1011 0100 1101

76A.5 RS(255,223) input buffer

Table 76A–4 illustrates the 223 octets of the input buffer constructed by the RS(255,223) encoder prior to computation of the parity octets. The octets of the buffer are formed from the input 66 bit blocks according to the procedure depicted in Figure 76–12 and Figure 76–13.

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Note that in Figure 76–12 and Figure 76–13 the right-most bit of each formed octet is the most significant, whereas Table 76A–4 lists the octets in the more typical notation i.e., the least significant bit appears on the right.

Table 76A–4—223 octet input buffer within FEC encoder before computation of parity octets[a]

	Dn	Dn -1	Dn -2	Dn -3	Dn -4	Dn -5	Dn -6	Dn -7	Dn -8	Dn -9	Dn -10	Dn -11	Dn -12	Dn -13	Dn -14	Dn -15
n= 222	00	00	00	80	C0	15	9E	FB	DD	32	E0	8D	5A	2D	EE	0F
n= 206	DB	AC	79	1D	7B	AA	D3	A1	FB	F0	3E	05	CE	66	FE	E3
n= 190	82	90	1A	C7	AC	71	8F	0D	43	02	80	71	70	38	6E	98
n= 174	63	38	90	F4	B5	13	FB	8C	37	5C	2D	92	C8	EC	3B	91
n= 158	73	02	67	D9	5B	AB	8B	FB	CA	83	1E	1B	90	98	5F	49
n= 142	05	A4	14	2F	46	E7	EE	3E	0F	63	0B	46	01	44	94	72
n= 126	5E	5A	12	40	29	84	CE	E1	92	BB	42	AD	61	13	B5	D5
n= 110	71	74	E1	D7	B1	34	D8	6F	74	BA	A3	62	D2	6A	C7	00
n= 94	B1	CF	AF	F0	56	05	CE	27	8D	28	80	50	B9	BE	19	E9
n= 78	14	B8	7A	46	81	6D	EE	DD	86	54	5E	FD	02	F8	86	68
n= 62	59	F0	12	54	74	33	CC	D9	D6	E3	93	44	F7	DA	DA	25
n= 46	5A	68	FE	54	C5	5B	A3	2E	16	36	FC	79	C9	91	81	4E
n= 30	C9	28	5E	0A	29	68	CE	13	4C	D8	3A	A6	48	55	23	55
n= 14	64	9E	64	E6	80	28	1A	58	15	A4	1B	1D	E8	DB	B2	

[a]Dn octet values are shown in hexadecimal notation.

76A.6 Parity symbol output

Table 76A–5 illustrates the 32 parity octets computed by the RS(255,223) encoder for the inputs given above.

Note that in Figure 76–12 and Figure 76–13 the right-most bit of each parity octet is the most significant, whereas Table 76A–5 lists the octets in the more typical notation i.e., the least significant bit is on the right.

Table 76A–5—32 parity octets computed by FEC encoder[a]

	Pn	Pn -1	Pn -2	Pn -3	Pn -4	Pn -5	Pn -6	Pn -7	Pn -8	Pn -9	Pn -10	Pn -11	Pn -12	Pn -13	Pn -14	Pn -15
n= 31	7E	62	35	FB	DB	9F	5E	8E	FD	B2	81	3E	F9	1D	9B	1A
n= 15	32	1E	70	CF	DD	C2	2C	54	43	F1	00	78	3C	4F	BD	F4

[a]Pn values are shown in hexadecimal notation.

76A.7 Parity symbols in binary format

As with the input buffer, this is written with least significant bit left most to correspond with Table 76A–6.

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Table 76A–6—32 parity octets computed by FEC encoder (binary)

0111 1110 0100 0110 1010 1100 1101 1111 1101 1011 1111 1001 0111 1010 0111 0001
1011 1111 0100 1101 1000 0001 0111 1100 1001 1111 1011 1000 1101 1001 0101 1000
0100 1100 0111 1000 0000 1110 1111 0011 1011 1011 0100 0011 0011 0100 0010 1010
1100 0010 1000 1111 0000 0000 0001 1110 0011 1100 1111 0010 1011 1101 0010 1111

76A.8 64B/66B Parity Blocks for Transmit

Table 76A–7 illustrates the 64B/66B blocks carrying parity that are generated by the RS (255,223) encoder for the input blocks in Table 76A–6 above. The RS (255,223) encoder inserts the parity blocks into the transmission stream to the gearbox subsequent to its transmission of the corresponding input 66 bit blocks (as described in 76.3.2.4).

The 66 bit blocks in the Table 76A–7 are transmitted from left to right within each row and from top to bottom between rows. The 64 bit payload portion of the 66 bit block is described as a series of hexadecimal octets—the left-most octet of each payload portion is transmitted first. Bits within each octet of the payload are transmitted in least-significant bit-first order (i.e., the right-most bit of each octet is transmitted first).

Thus, the first 18 bits of the parity blocks transmitted are: 00 0111 1110 0100 0110 …

Table 76A–7—64B/66B blocks carrying 32 parity octets generated by FEC encoder

Sync [0:1]	**64 bit payload** [7:0]-[15:8]-[23:16]-[31:24]-[39:32]-[47:40]-[55:48]-[63:56]
00	7E-62-35-FB-DB-9F-5E-8E
11	FD-B2-81-3E-F9-1D-9B-1A
11	32-1E-70-CF-DD-C2-2C-54
00	43-F1-00-78-3C-4F-BD-F4

76A.9 Parity 66 bit blocks in binary format

Table 76A-8—64B/66B blocks carrying 32 parity octets generated by FEC encoder (binary)

Sync [0:1]	**64 bit payload (transmitted from left to right)**
00	0111 1110 0100 0110 1010 1100 1101 1111 1101 1011 1111 1001 0111 1010 0111 0001
11	1011 1111 0100 1101 1000 0001 0111 1100 1001 1111 1011 1000 1101 1001 0101 1000
11	0100 1100 0111 1000 0000 1110 1111 0011 1011 1011 0100 0011 0011 0100 0010 1010
00	1100 0010 1000 1111 0000 0000 0001 1110 0011 1100 1111 0010 1011 1101 0010 1111

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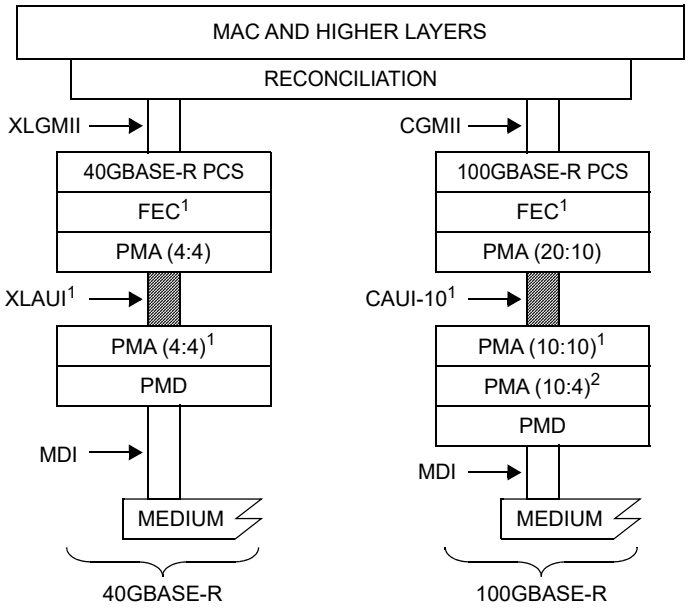
Annex 83A

(normative)

40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10)

83A.1 Overview

This annex defines the functional and electrical characteristics for the optional 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10). Figure 83A–1 shows the relationships of the XLGMII, PMA, XLAUI, and PMD for 40 Gb/s and CGMII, PMA, CAUI-10, and PMD for 100 Gb/s.



CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—OPTIONAL OR OMITTED DEPENDING ON PHY TYPE
NOTE 2—CONDITIONAL BASED ON PMD TYPE

Figure 83A–1—Example relationship of XLAUI and CAUI-10 to IEEE 802.3 Ethernet model

The purpose of the optional XLAUI or CAUI-10 is to provide a flexible chip-to-chip and chip-to-module interconnect for 40 Gb/s or 100 Gb/s components. Annex 83A provides compliance requirements for

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XLAUI/CAUI-10 transmitters and receivers while Annex 83B specifies the electrical requirements for the chip-to-module interconnection.

The XLAUI/CAUI-10 allows interconnect distances of approximately 25 cm over printed circuit board including one connector, see 83A.4.

An example application of CAUI-10 includes providing a physical connection between a ten-lane 100 Gb/s PMA and a 10:4 PMA mapping element. An example application of XLAUI is to provide lane extension for interfacing MAC and PHY components in a 40 Gb/s Ethernet system distributed across a circuit board.

The optional XLAUI/CAUI-10 interface has the following characteristics:

a) Independent transmit and receive data paths
b) Differential AC-coupled signaling with low voltage swing
c) Self-timed interface
d) Shared technology with other 40 Gb/s or 100 Gb/s interfaces
e) Utilization of 64B/66B coding

83A.1.1 Summary of major concepts

The following is a list of the major concepts of XLAUI and CAUI-10:

a) The optional XLAUI/CAUI-10 interface can be inserted between PMA layers in the IEEE 802.3 Ethernet model to transparently enable chip-to-chip communication
b) The XLAUI is organized into four lanes, the CAUI-10 is organized into ten lanes
c) The XLAUI/CAUI-10 interface is a parallel electrical interface with each lane running at a nominal rate of 10.3125 Gb/s

83A.1.2 Rate of operation

The XLAUI interface supports the 40 Gb/s data rate and the CAUI-10 interface supports the 100 Gb/s data rate. For 40 Gb/s applications, the data stream shall be presented in four lanes as described in Clause 83. For 100 Gb/s applications, the data stream shall be presented in ten lanes as described in Clause 83. The data is 64B/66B coded. The nominal signaling rate for each lane in both 40 Gb/s and 100 Gb/s applications shall be 10.3125 Gb/s.

83A.2 XLAUI/CAUI-10 link block diagram

XLAUI/CAUI-10 link is illustrated in Figure 83A–2. XLAUI/CAUI-10 channel is defined from the transmit pad to the receive pad including any AC-coupling in the path.

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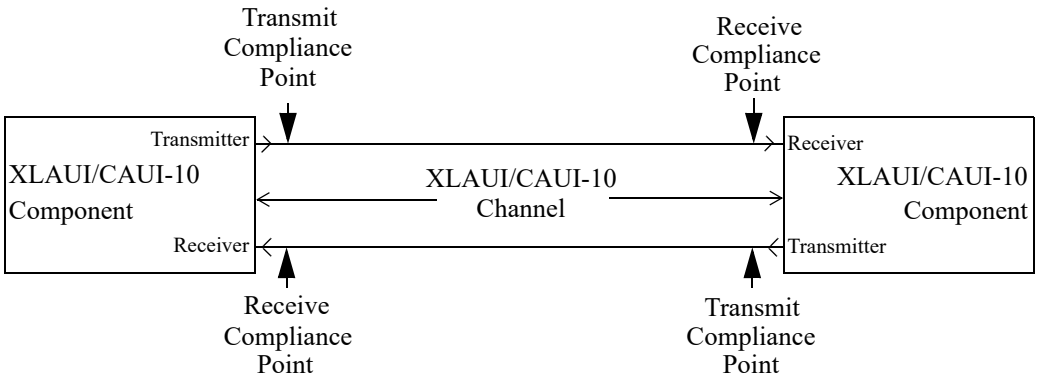

Figure 83A–2—Definition of transmit and receive compliance points

83A.2.1 Transmitter compliance points

The reference differential insertion loss, expressed in decibels, between the transmitter and the transmit compliance point is defined in Equation (83A–1) and illustrated in Figure 83A–3. The effects of differences between the actual insertion loss and the reference insertion loss are to be accounted in the measurements.

$$Insertion\_loss(f) = -0.00086 + 0.2286\sqrt{f} + 0.08386f \quad \text{dB} \qquad 0.01 \le f \le 11.1 \qquad \text{(83A–1)}$$

where

Insertion_loss(*f*) is the differential insertion loss at frequency *f*
f is the frequency in GHz

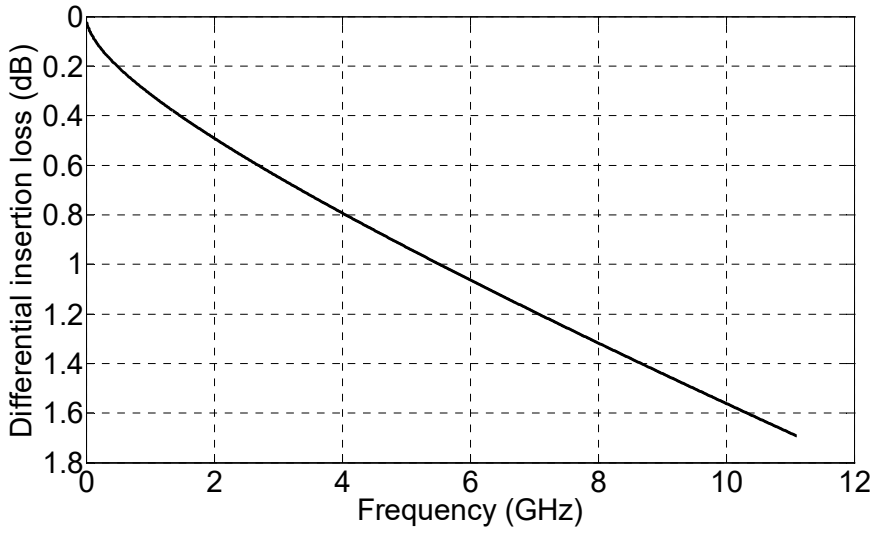

Figure 83A–3—Insertion loss between transmitter and transmit compliance point

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83A.2.2 Receiver compliance points

The reference differential insertion loss, expressed in decibels, between the receiver compliance point and the receiver is defined in Equation (83A–2) and illustrated in Figure 83A–4. The effects of differences between the actual insertion loss and the reference insertion loss are to be accounted in the measurements.

$$Insertion\_loss(f) = -0.00086 + 0.2286\sqrt{f} + 0.08386f \quad \text{dB} \qquad 0.01 \le f \le 11.1 \qquad \text{(83A–2)}$$

where

Insertion_loss(*f*) is the differential insertion loss at frequency *f*
f is the frequency in GHz

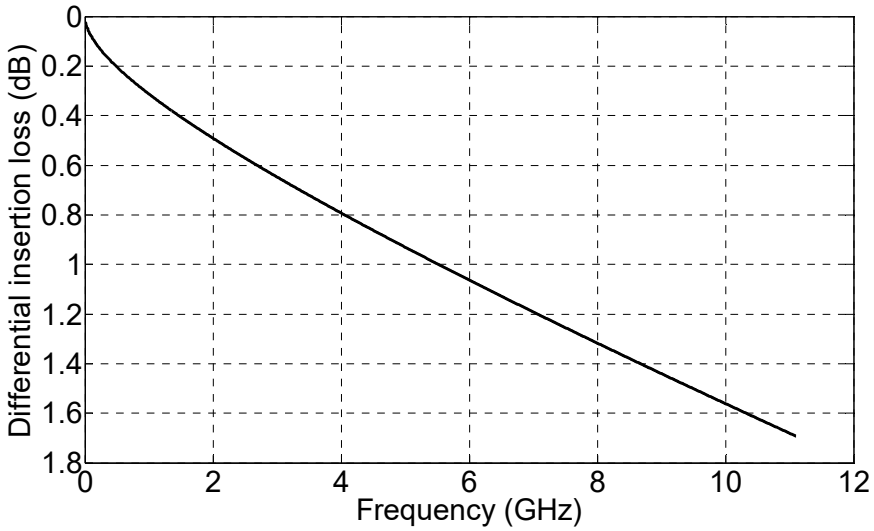

Figure 83A–4—Insertion loss between receive compliance point and receiver

83A.3 XLAUI/CAUI-10 electrical characteristics

The electrical characteristics of the XLAUI/CAUI-10 interface are specified such that they can be applied within a variety of 40 Gb/s Ethernet or 100 Gb/s Ethernet equipment types. The electrical characteristics for XLAUI/CAUI-10 shall meet the specifications defined in 83A.3.1, 83A.3.2, 83A.3.4, and 83A.3.5.

83A.3.1 Signal levels

The XLAUI/CAUI-10 is a low-swing AC-coupled differential interface. AC-coupling allows for interoperability between components operating from different supply voltages. Differential signal swings are defined in the following subclauses, and depend on several factors such as transmitter de-emphasis and transmission line losses.

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83A.3.2 Signal paths

The XLAUI/CAUI-10 signal paths are point-to-point connections. Each path corresponds to a XLAUI/CAUI-10 lane, and is composed of two complementary signals making a balanced differential pair. For XLAUI, there are four differential paths in each direction for a total of eight pairs, or sixteen connections. For CAUI-10, there are ten differential paths in each direction for a total of twenty pairs, or 40 connections.

83A.3.3 EEE operation

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78, 78.1.3.3.1), then the inter-sublayer service interface includes four additional primitives as described in 83.3 and may also support CAUI-10 shutdown.

If the EEE capability includes XLAUI/CAUI-10 shutdown (see 78.5.2), then when aui_tx_mode (see 83.5.11.3) is set to ALERT, the transmit direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00, which is transmitted across the XLAUI/CAUI-10. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When aui_tx_mode is QUIET, the transmit direction XLAUI/CAUI-10 transmitter is disabled as specified in 83A.3.4.1.1. Similarly when the received aui_tx_mode is set to ALERT, the receive direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00, which is transmitted across the XLAUI/CAUI-10. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When the received aui_tx_mode is QUIET, the receive direction XLAUI/CAUI-10 transmitter is disabled as specified in 83A.3.4.1.1.

83A.3.4 Transmitter characteristics

The XLAUI/CAUI-10 transmitter characteristics measured at the transmitter compliance point are specified in Table 83A–1. The XLAUI/CAUI-10 signaling rate shall be the signaling rate defined in Table 83A–1.

Table 83A–1—Transmitter characteristics

Parameter	Subclause reference	Value	Units
Signaling rate per lane (range)	—	10.3125 ± 100 ppm	GBd
Single-ended output voltage maximum minimum	83A.3.4.1	 4 –0.4	 V V
Maximum differential output voltage, peak-to-peak	83A.3.4.1	760	mV
Minimum de-emphasis	83A.3.4.1	4.4	dB
Maximum de-emphasis	83A.3.4.1	7	dB
Minimum VMA	83A.3.4.1	See Equation (83A–4)	mV
Maximum termination mismatch at 1 MHz	86A.5.3.2	5	%
Maximum output AC common-mode voltage, RMS	86A.5.3.1	15	mV
Minimum output rise and fall time (20% to 80%)	83A.3.4.2	24	ps
Differential output return loss	83A.3.4.3	See Equation (83A–5)	dB

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Table 83A–1—Transmitter characteristics *(continued)*

Parameter	Subclause reference	Value	Units
Common-mode output return loss	83A.3.4.4	See Equation (83A–6)	dB
Maximum Total Jitter	83A.3.4.5	0.32	UI
Maximum Deterministic Jitter	83A.3.4.5	0.17	UI
Transmitter eye mask definition X1	83A.3.4.5	0.16	UI
Transmitter eye mask definition X2	83A.3.4.5	0.38	UI
Transmitter eye mask definition Y1	83A.3.4.5	200	mV
Transmitter eye mask definition Y2	83A.3.4.5	380	mV

83A.3.4.1 Output amplitude

Driver differential output amplitude shall be less than the maximum differential output voltage defined in Table 83A–1 including any transmit de-emphasis. DC-referenced logic levels are not defined since the receiver is AC-coupled. Single-ended output voltage shall be within the range specified in Table 83A–1 with respect to ground.

De-emphasis shall be greater than the minimum de-emphasis and less than the maximum de-emphasis defined in Table 83A–1. De-emphasis is defined as the ratio between the amplitude following a transition and the amplitude during a non-transition bit as seen in Equation (83A–3). VMA is defined in 86A.5.3.5 using the square wave or PRBS9 (Pattern 4) defined in Table 86–11.

See Figure 83A–5 for an illustration of absolute driver output voltage limits, definition of differential peak-to-peak amplitude, and definition of the parameters used to calculate de-emphasis. SLi<P> and SLi<N> are positive and negative sides of a differential signal pair for lane i (i = 0, 1, 2, 3 for XLAUI. For CAUI-10 i = 0:9).

$$\text{De-emphasis (dB)} = 20\log_{10}\left(\frac{\text{Differential peak-to-peak amplitude}}{\text{VMA}}\right) \quad \text{(83A–3)}$$

$$\text{Minimum VMA (mV)} = (234.64 - 2.13x + 0.18x^2) \times 1.32(10^{-y/20}) \quad \text{(83A–4)}$$

where

x is the rise or fall time (whichever is larger) in ps
y is de-emphasis value in dB

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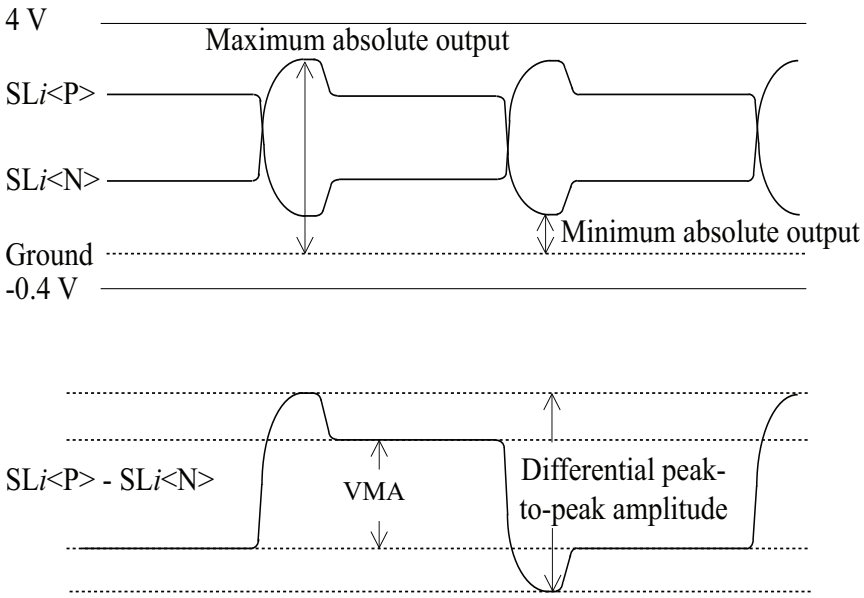

Figure 83A–5—Driver output voltage limits and definitions

83A.3.4.1.1 Amplitude and swing

For EEE capability with XLAUI/CAUI-10 shutdown, the XLAUI/CAUI-10 transmitter lane's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of aui_tx_mode changing to QUIET in the relevant direction. Furthermore, the XLAUI/CAUI-10 transmitter lane's differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of aui_tx_mode ceasing to be QUIET in the relevant direction.

83A.3.4.2 Rise/fall time

Differential rise/fall times shall be greater than the minimum output rise and fall time defined in Table 83A–1, as measured from the 20% to the 80% levels. Shorter transitions may result in excessive high-frequency components and increase EMI and crosstalk. The upper limit is defined by the transmit eye mask shown in Figure 83A–8. Rise/fall time is measured with de-emphasis off as defined in 83A.5.1. Rise/fall time measurements are taken using a square wave test pattern as defined in 83.5.10.

83A.3.4.3 Differential output return loss

Differential output return loss shall meet the requirements defined in Table 83A–1. Differential output return loss is given in Equation (83A–5) and is illustrated Figure 83A–6. Differential output return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 Ω. The maximum termination mismatch at 1 MHz shall be less than the requirement defined in Table 83A–1.

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$$Return\_loss(f) \geq \begin{cases} 12 & 0.01 \leq f < 2.125 \\ 6.5 - 13.33\log_{10}\left(\frac{f}{5.5}\right) & 2.125 \leq f \leq 11.1 \end{cases} \text{ (dB)} \quad \text{(83A–5)}$$

where

Return_loss(*f*) is the differential output return loss at frequency *f*
f is the frequency in GHz

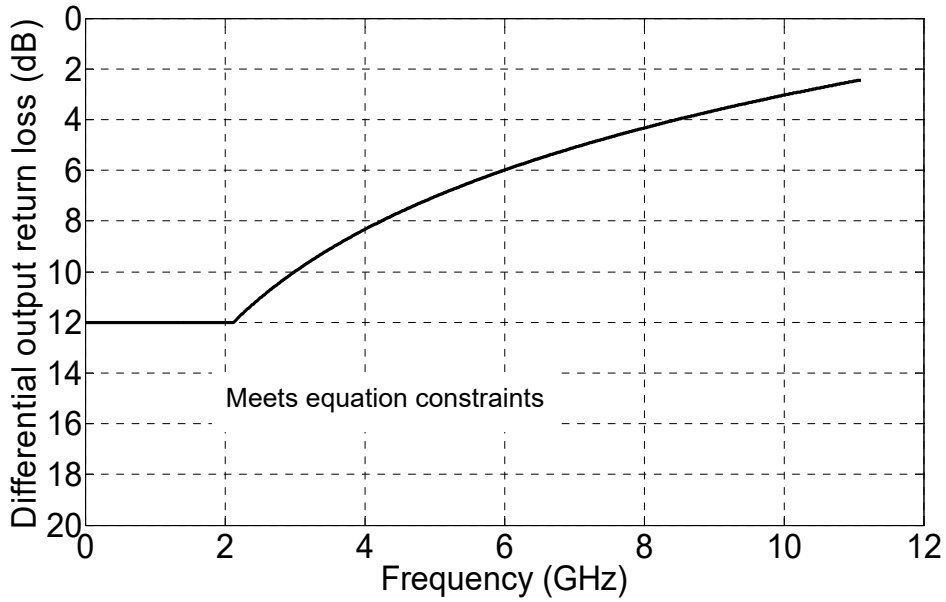

Figure 83A–6—Differential output return loss

83A.3.4.4 Common-mode output return loss

Common-mode output return loss shall meet the requirements defined in Table 83A–1. Common-mode output return loss is given in Equation (83A–6) and is illustrated in Figure 83A–7. Common-mode output return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for common-mode return loss measurements is 25 Ω.

$$Return\_loss(f) \geq \begin{cases} 9 & 0.01 \leq f < 2.125 \\ 3.5 - 13.33\log_{10}\left(\frac{f}{5.5}\right) & 2.125 \leq f < 7.1 \\ 2 & 7.1 \leq f \leq 11.1 \end{cases} \text{ (dB)} \quad \text{(83A–6)}$$

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where

Return_loss(*f*) is the common-mode output return loss at frequency *f*
f is the frequency in GHz

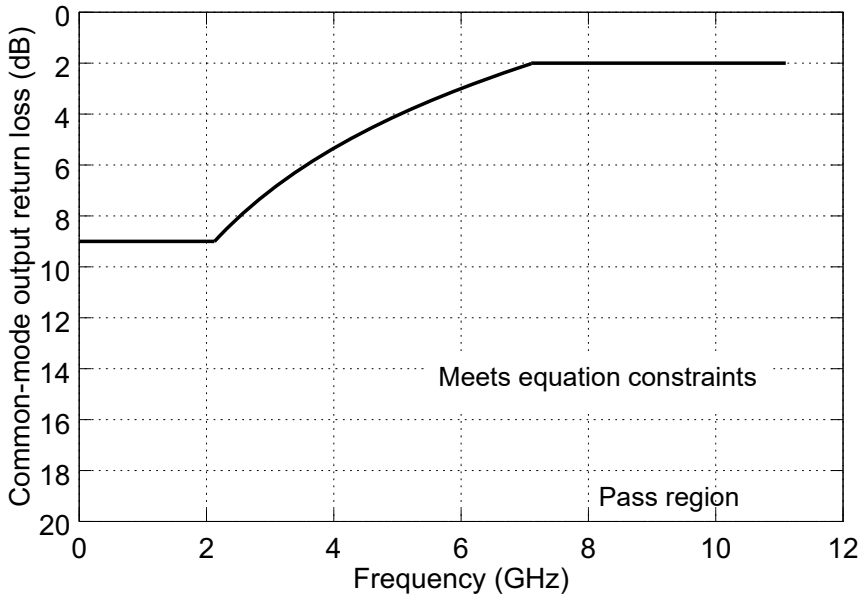

Figure 83A–7—Common-mode output return loss

83A.3.4.5 Transmitter eye mask and transmitter jitter definition

The measured transmit signal at the transmit compliance point shall meet the eye template specified in Figure 83A–8 and Table 83A–1. The template measurement requirements are specified in 83A.5.1. The measured jitter at the transmit compliance point shall be less than the maximum Total Jitter as defined in Table 83A–1 and a maximum Deterministic Jitter as defined in Table 83A–1. Jitter and eye mask measurement requirements are described in 83A.5.1 and are conducted with de-emphasis off.

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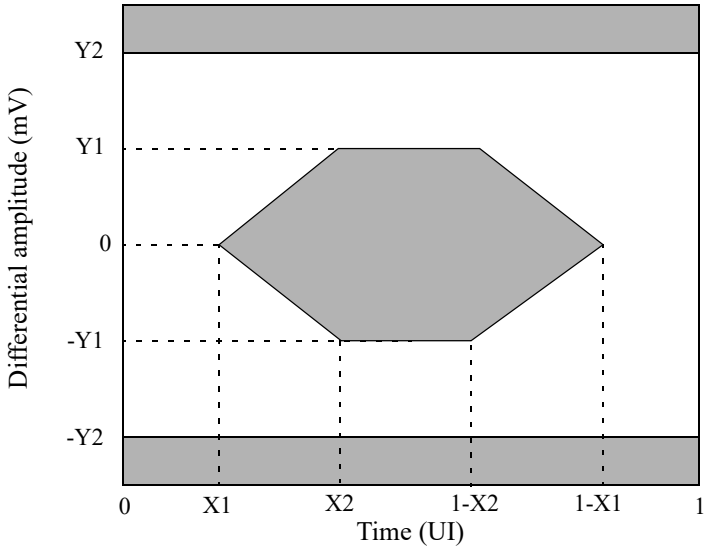

Figure 83A–8—Transmitter eye mask

83A.3.4.6 Global transmit disable function

Global transmit disable is optional for EEE capability. The transmit disable function shall turn off all transmitter lanes for a physically instantiated AUI in either the ingress or the egress direction. In the egress direction, the PMA may turn off all the transmitter lanes for the egress direction XLAUI/CAUI-10 if PEASE is asserted and aui_tx_mode is QUIET. In the ingress direction, the PMA may turn off all the transmitter lanes for the ingress direction XLAUI/CAUI-10 if PIASE is asserted and the received aui_tx_mode is QUIET. In both directions, the transmit disable function shall turn on all transmitter lanes after the appropriate direction aui_tx_mode changes to any state other than QUIET within a time and voltage level specified in 83A.3.4.1.1.

83A.3.5 Receiver characteristics

Receiver characteristics at the receiver compliance point are specified in Table 83A–2 and detailed in 83A.3.5.1 through 83A.3.5.6.

83A.3.5.1 Bit error ratio

The receiver shall operate with a BER of better than 10^{-12} in the presence of a compliant input signal as defined in 83A.3.5.2.

NOTE—A transmitter capable of operating at TJ = 0.3 UI and DJ = 0.16 UI and receiver capable of operating at stress jitter tolerance of TJ = 0.64 UI and DJ= 0.41 UI would have sufficient margin for operation at approximately BER 10^{-15}.

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Table 83A–2—Receiver characteristics

Parameter	Subclause reference	Value	Units
Signaling rate per lane (range)	—	10.3125 ± 100 ppm	GBd
Minimum input AC common-mode voltage tolerance, RMS	86A.5.3.1	20	mV
Minimum input rise and fall time tolerance (20% to 80%)	83A.3.4.2	24	ps
Differential input return loss	83A.3.5.3	See Equation (83A–7)	dB
Differential to common-mode input return loss	83A.3.5.4	See Equation (83A–8)	dB
Stressed receiver tolerance			
Minimum Total Input Jitter Tolerance	83A.3.5.2	0.62	UI
Minimum Deterministic Input Jitter Tolerance	83A.3.5.2	0.42	UI
Receiver eye mask definition X1	83A.3.5.2	0.31	UI
Receiver eye mask definition X2	83A.3.5.2	0.5	UI
Receiver eye mask definition Y1	83A.3.5.2	42.5	mV
Receiver eye mask definition Y2	83A.3.5.2	425	mV

83A.3.5.2 Input signal definition

A compliant input signal to a XLAUI/CAUI-10 receiver has characteristics determined by a compliant XLAUI/CAUI-10 driver and channel. The input signal definition satisfies the eye mask defined in Table 83A–2 and Figure 83A–9. Input signal jitter does not exceed the jitter tolerance requirements specified in 83A.3.5.6. Stressed receiver measurement requirements are specified in 83A.5.2.

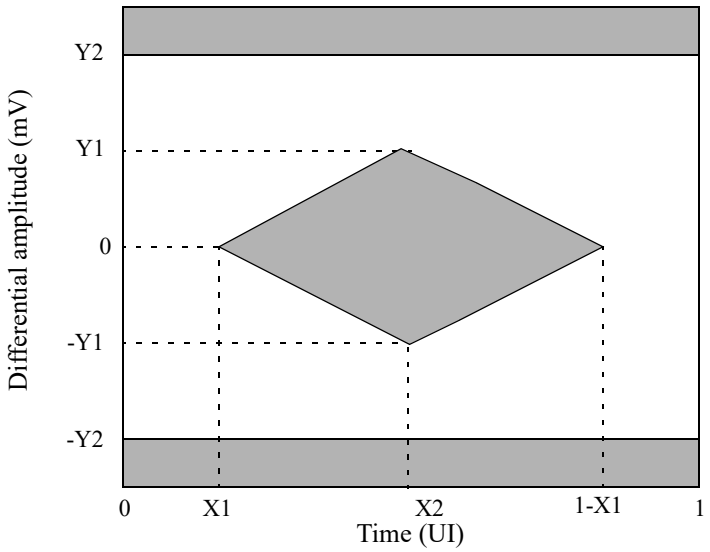

Figure 83A–9—Receiver template

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83A.3.5.3 Differential input return loss

Differential input return loss shall meet the requirements defined in Table 83A–2. Differential input return loss is given in Equation (83A–7) and is illustrated in Figure 83A–10. Differential input return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the receiver. The reference impedance for differential return loss measurements is 100 Ω.

$$Return\_loss(f) \geq \begin{cases} 12 & 0.01 \leq f < 2.125 \\ 6.5 - 13.33\log_{10}\left(\frac{f}{5.5}\right) & 2.125 \leq f \leq 11.1 \end{cases} \quad \text{(dB)} \qquad \text{(83A–7)}$$

where

Return_loss(*f*) is the differential input return loss at frequency *f*
f is the frequency in GHz

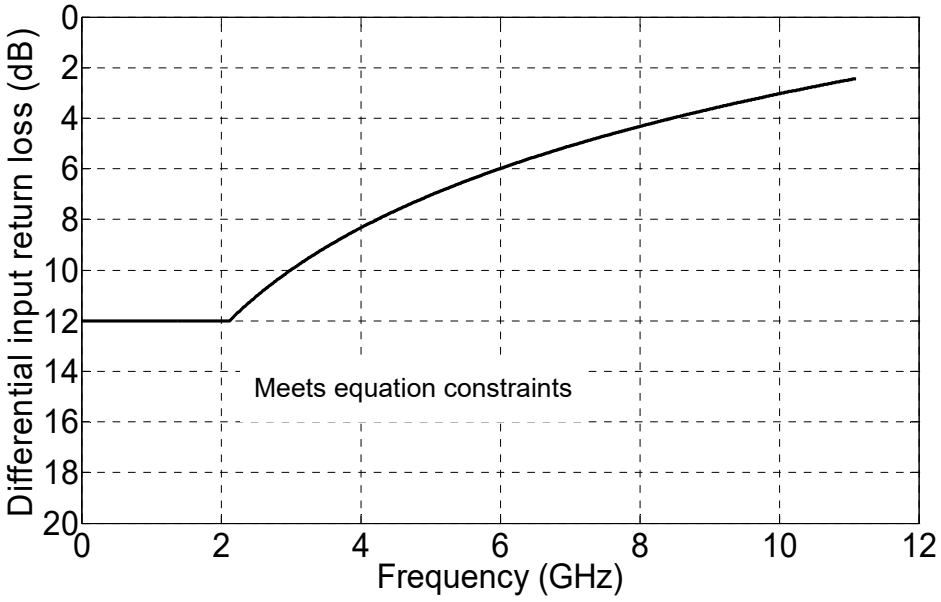

Figure 83A–10—Differential input return loss

83A.3.5.4 Differential to common-mode input return loss

Differential to common-mode input return loss shall meet the requirements defined in Table 83A–2. Differential to common-mode input return loss is given in Equation (83A–8) and is illustrated in Figure 83A–11. Differential to common-mode input return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the receiver. The reference impedance for differential return loss measurements is 100 Ω. The reference impedance for common-mode return loss measurements is 25 Ω.

$$Return\_loss(f) \geq 15 \qquad 0.01 \leq f < 11.1 \qquad \text{(dB)} \qquad \text{(83A–8)}$$

where

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Return_loss(*f*) is the differential to common-mode input return loss at frequency *f*
f is the frequency in GHz

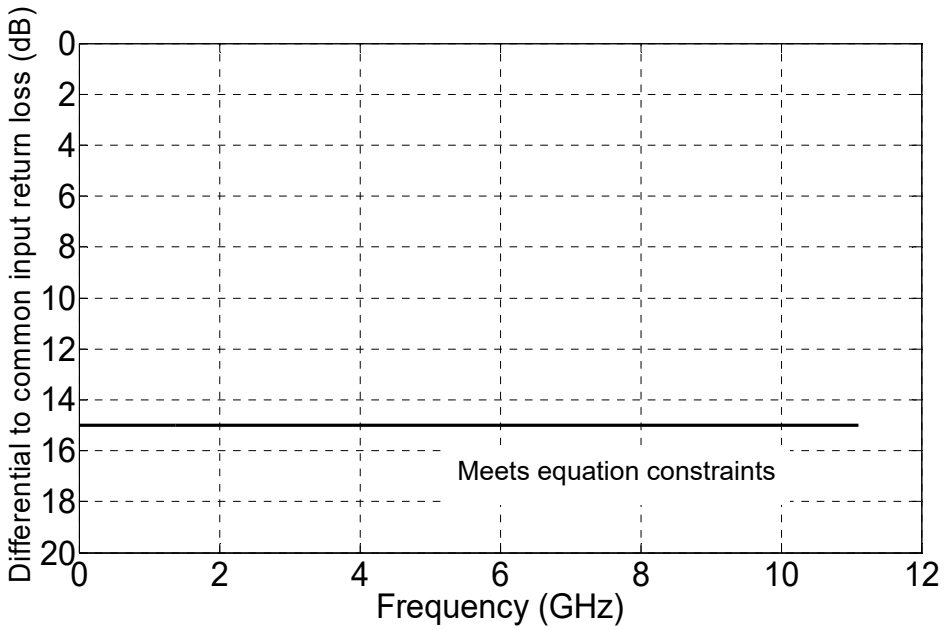

Figure 83A–11—Differential to common-mode input return loss

83A.3.5.5 AC-coupling

The XLAUI/CAUI-10 receiver shall be AC-coupled to the XLAUI/CAUI-10 transmitter to allow for maximum interoperability between various 10 Gb/s components. AC-coupling is considered to be part of the receiver for the purposes of this specification except when interfacing with modules defined in Annex 83B or explicitly stated otherwise. It should be noted that there may be various methods for AC-coupling in actual implementations.

83A.3.5.6 Jitter tolerance

The XLAUI/CAU-10 receiver shall have a peak-to-peak total jitter amplitude tolerance of at least the minimum total input jitter tolerance defined in Table 83A–2. This total jitter is composed of two components: deterministic jitter and random jitter. Deterministic jitter tolerance shall be at least the minimum deterministic input jitter tolerance defined in Table 83A–2. The XLAUI/CAUI-10 receiver shall tolerate sinusoidal jitter with any frequency and amplitude defined by the mask of Figure 83A–12. This sub-component of deterministic jitter is intended to ensure margin for low-frequency jitter, wander, noise, crosstalk, and other variable system effects.

83A.3.5.7 Global energy detect function

The global energy detect function is mandatory for EEE capability with the deep sleep mode option and XLAUI/CAUI-10 shutdown. The global energy detect function indicates whether or not signaling energy is being received on the physical instantiation of the inter sublayer interface (in each direction as appropriate). The energy detection function may be considered a subset of the signal indication logic. If no energy is being received on the XLAUI/CAUI-10 for the ingress direction, SIGNAL_DETECT is set to FAIL following a transition from aui_rx_mode = DATA to aui_rx_mode = QUIET. When aui_rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver

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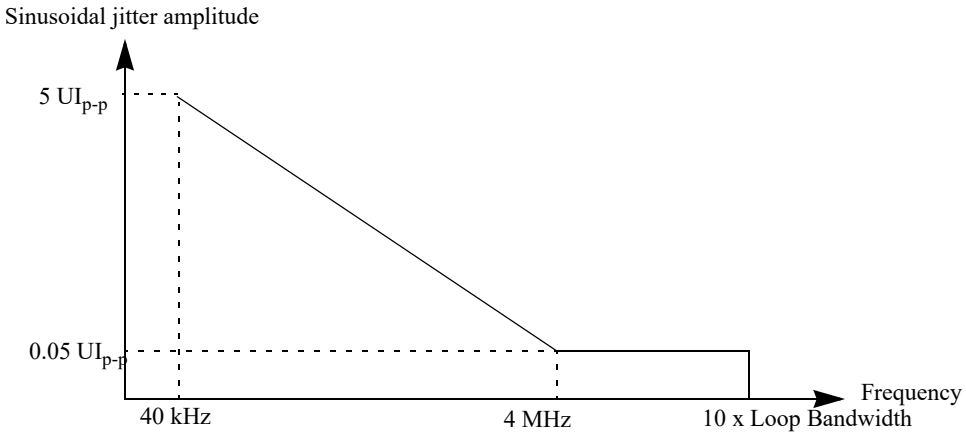

Figure 83A–12—Single-tone sinusoidal jitter mask

input that corresponds to an ALERT signal driven from the XLAUI/CAUI-10 link partner. While aui_rx_mode = QUIET, SIGNAL_DETECT changes from FAIL to OK only after the valid ALERT signal is received.

83A.4 Interconnect characteristics

This subclause describes recommended characteristics which are used to characterize a XLAUI/CAUI-10 channel as shown in Figure 83A–2. The value for differential insertion loss is summarized in Equation (83A–9) and illustrated in Figure 83A–13. The value for minimum return loss is summarized in Equation (83A–10) and illustrated in Figure 83A–14. The channel is terminated with 100 Ω differential impedance. Other impairments such as crosstalk can have a material impact on the link performance and should be minimized.

$$Insertion\_loss(f) < \left\{ \begin{array}{ll} 0.15 + 1.39\sqrt{f} + 1.4f & 0.01 \le f < 7 \\ -15.86 + 4.2f & 7 \le f \le 11.1 \end{array} \right\} \text{ (dB)} \quad \text{(83A–9)}$$

where

Insertion_loss(*f*) is the differential insertion loss at frequency *f*
f is the frequency in GHz

$$Return\_loss(f) \ge \left\{ \begin{array}{ll} 12.5 & 0.01 \le f < 5 \\ 12.5 - 27.5\log_{10}\left(\frac{f}{5}\right) & 5 \le f \le 11.1 \end{array} \right\} \text{ (dB)} \quad \text{(83A–10)}$$

where

Return_loss(*f*) is the differential input return loss at frequency *f*
f is the frequency in GHz

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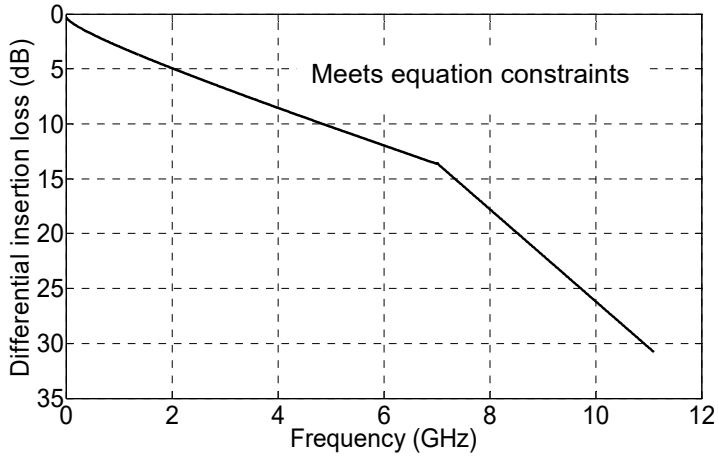

Figure 83A–13—Differential insertion loss

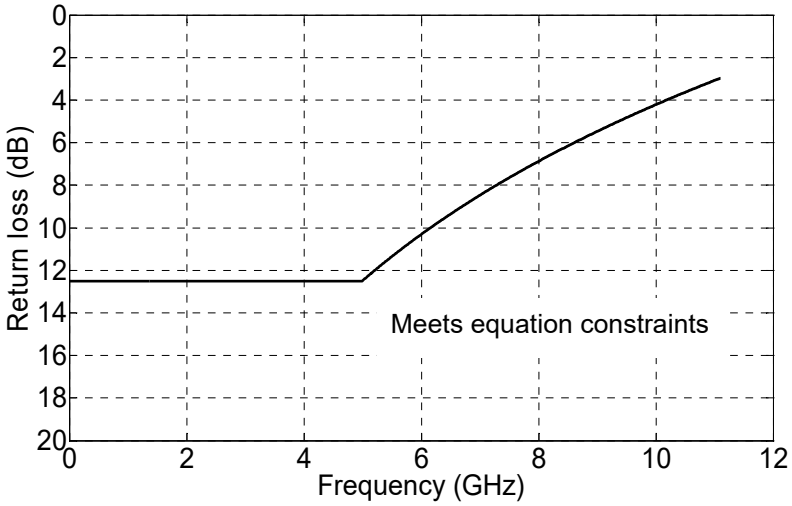

Figure 83A–14—Differential input return loss

The XLAUI/CAUI-10 is primarily intended as a point-to-point interface of up to approximately 25 cm between integrated circuits using controlled impedance traces on low-cost printed circuit boards (PCBs). Longer reaches for the XLAUI/CAUI-10 may be achieved by the use of better PCB materials, as the performance of an actual XLAUI/CAUI-10 interconnect is highly dependent on the implementation.

83A.4.1 Characteristic impedance

The recommended differential characteristic impedance of circuit board trace pairs is 100 Ω ± 10%.

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83A.5 Electrical parameter measurement methods

This subclause describes the measurement methodology that is to be used to verify XLAUI/CAUI-10 compliance. Eye templates are measured with AC-coupling and centered at 0 V differential. The signal waveform, eye, and jitter may be measured using a receiver with at least an equivalent 12 GHz low-pass filter response. Jitter values and eye masks are specified for BER 10^{-12}.

83A.5.1 Transmit jitter

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in Annex 48B.3. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 4 MHz is applied to the jitter. The test pattern for jitter measurements shall be PRBS31 test pattern in 83.5.10 or scrambled idle in 82.2.11. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal. De-emphasis shall be off during jitter testing. Transmit de-emphasis off state is defined by any setting that gives optimal performance for transmitter jitter and eye mask evaluation. All XLAUI/CAUI-10 transmitter lanes shall be active and all XLAUI/CAUI-10 receive lanes shall be receiving maximum amplitude and fastest rise time (as defined in Table 83A–1) during transmit jitter testing to ensure maximum lane-lane crosstalk is included in the jitter evaluation.

83A.5.2 Receiver tolerance

The XLAUI/CAUI-10 jitter tolerance test setup in Figure 83A–15 or its equivalent shall meet the receiver eye mask defined in Table 83A–2. Applied jitter is measured using the methodology described in Annex 48B.3. Deterministic jitter is added to a clean test pattern by adding sinusoidal jitter as defined in 83A.3.5.6, along with low-pass filter stress, followed by a limiting function, and frequency-dependent attenuation. The low-pass filter stress is added until the 0.34 UI Deterministic Jitter is achieved. Frequency-dependent attenuation is then added using PCB trace or frequency-dependent attenuation which emulates PCB loss. Frequency-dependent attenuation is added until 0.42 UI Deterministic Jitter is achieved. Random jitter is added to the test signal using an interference generator which is a broadband noise source capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from 50 MHz to 6 GHz with a crest factor of no less than 5. The amplitude and output jitter of the filter stress plus limiter and random jitter injection shall meet the receiver eye mask defined in Table 83A–2. All XLAUI/CAUI-10 lanes shall be active during jitter tolerance testing. The PRBS31 pattern defined in 83.5.10 or scrambled idle defined in 82.2.11 is used for evaluating XLAUI/CAUI-10 jitter tolerance.

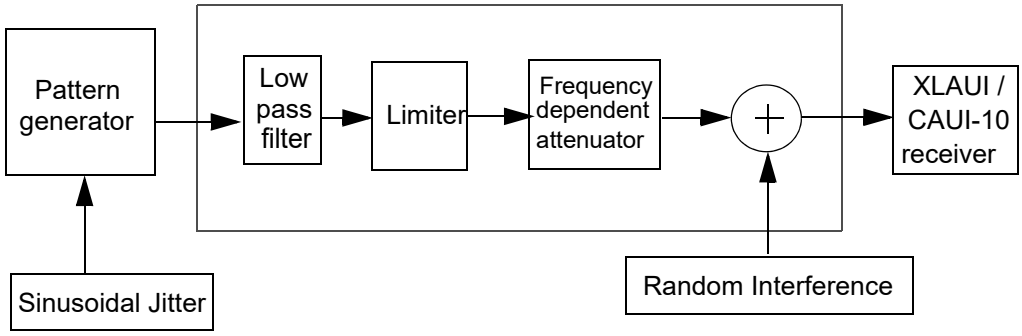

Figure 83A–15—Stressed-eye and jitter tolerance test setup

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83A.6 Environmental specifications

83A.6.1 General safety

Equipment subject to this annex shall conform to the general safety requirements in J.2.

83A.6.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

83A.6.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

83A.6.4 Electromagnetic compatibility

A system integrating the XLAUI/CAUI-10 shall comply with applicable local and national codes for the limitation of electromagnetic interference.

83A.6.5 Temperature and humidity

A system integrating the XLAUI/CAUI-10 is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

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83A.7 Protocol implementation conformance statement (PICS) proforma for Annex 83A, 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10)[294]

83A.7.1 Introduction

The supplier of a XLAUI/CAUI-10 implementation that is claimed to conform to Annex 83A, 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the same, can be found in Clause 21.

83A.7.2 Identification

83A.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

83A.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 83A, 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[294]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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83A.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	XLAUI is organized into four lanes, CAUI-10 is organized into ten lanes	83A.1.2	See Clause 83	M	Yes [ ]
RATE	Each XLAUI/CAUI-10 lane operates at 10.3125 Gb/s	83A.1.2	10.3125 Gb/s (nominal)	M	Yes [ ]
IO	Meets XLAUI/CAUI-10 Electrical Characteristics	83A.3	Supports transmit and receive compliance points	M	Yes [ ]
*LPI	Support for CAUI-10 shutdown	83A.3.3		O	Yes [ ] No [ ]

83A.7.4 XLAUI/CAUI-10 transmitter requirements

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	83A.3.4	10.3125 GBd ±100 ppm	M	Yes [ ]
TC2	Single ended output voltage range	83A.3.4.1	–0.4 V to 4 V	M	Yes [ ]
TC3	Minimum de-emphasis	83A.3.4.1	4.4 dB	M	Yes [ ]
TC4	Maximum de-emphasis	83A.3.4.1	7 dB	M	Yes [ ]
TC5	Maximum termination mismatch	83A.3.4.3	5%	M	Yes [ ]
TC6	Maximum differential output voltage	83A.3.4.1	760 mV	M	Yes [ ]
TC7	Minimum output rise and fall time (20% to 80%)	83A.3.4.2	24 ps	M	Yes [ ]
TC8	Differential output return loss	83A.3.4.3	See Equation (83A–5)	M	Yes [ ]
TC9	Common-mode output return loss	83A.3.4.4	See Equation (83A–6)	M	Yes [ ]
TC10	Transmitter eye mask	83A.3.4.5	See Figure 83A–8	M	Yes [ ]
TC11	Amplitude and swing for XLAUI/CAUI-10 shutdown	83A.3.4.1.1		LPI:M	Yes [ ] N/A [ ]
TC12	Transmit disable for XLAUI/CAUI-10 shutdown	83A.3.4.6		LPI:M	Yes [ ] N/A [ ]

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83A.7.5 XLAUI/CAUI-10 receiver requirements

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Receiver BER	83A.3.5.1	Better than 10^{-12}	M	Yes [ ]
RC2	Differential input return loss	83A.3.5.3	See Equation (83A–7)	M	Yes [ ]
RC3	Differential to common-mode input return loss	83A.3.5.4	See Equation (83A–8)	M	Yes [ ]
RC4	Total Jitter Tolerance	83A.3.5.6	0.62 UI	M	Yes [ ]
RC5	Deterministic Jitter Tolerance	83A.3.5.6	0.42 UI	M	Yes [ ]
RC6	Sinusoidal Jitter Tolerance	83A.3.5.6	See Figure 83A–12	M	Yes [ ]
RC7	Receiver AC-coupling	83A.3.5.5	Present	M	Yes [ ]
RC8	Signal detect for XLAUI/CAUI-10 shutdown	83A.3.5.7		LPI:M	Yes [ ] N/A [ ]

83A.7.6 Electrical measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
EM1	De-emphasis setting during jitter measurements	83A.5.1	Off	M	Yes [ ]
EM2	Jitter Tolerance stressed input	83A.5.2	0.42 UI DJ, 0.2 UI RJ	M	Yes [ ]
EM3	Random jitter interference generator	83A.5.2	±3 dB from 50 MHz to 6 GHz with a crest factor of no less than 5	M	Yes [ ]
EM4	Meet jitter tolerance requirement with all XLAUI/CAUI-10 channels active	83A.5.2	Yes	M	Yes [ ]
EM5	XLAUI/CAUI-10 Jitter Tolerance Test Pattern	83A.5.2	PRBS31 or scrambled idle	M	Yes [ ]

83A.7.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Conforms to J.2	83A.6.1	Yes	M	Yes [ ]
ES2	Compliance with applicable local and national codes for the limitation of electromagnetic interference	83A.6.4	Yes	M	Yes [ ]

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Annex 83B

(normative)

Chip-to-module 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10)

83B.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10). The purpose of this annex is to provide electrical characteristics and associated compliance points for pluggable module applications that use the XLAUI/CAUI-10 interface and shall use the same number of lanes and signaling rate defined in Annex 83A. Figure 83B–3 and Table 83B–1 summarize an example differential insertion loss budget associated with the chip-to-module application. The insertion loss of Equation (83A–9), excluding a 0.5 dB connector loss at 5.15625 GHz, is linearly scaled to 7.9 dB loss at 5.15625 GHz for the host XLAUI/CAUI-10 component, and 2.1 dB loss at 5.15625 GHz for the module as per Table 83B–1 and Equation (83B–1) for the host and Equation (83B–2) for the module. Tradeoffs can be made between the host PCB insertion loss and the connector loss. Equation (83B–1) is illustrated in Figure 83B–1 and Equation (83B–2) is illustrated in Figure 83B–2.

$$Insertion\_loss(f) \le \left\{ \begin{array}{ll} 0.111 + 1.046\sqrt{f} + 1.05f & 0.01 \le f < 7 \\ -11.82 + 3.15f & 7 \le f \le 11.1 \end{array} \right\} \text{ (dB)} \qquad \text{(83B–1)}$$

where

Insertion_loss(*f*) is the differential insertion loss at frequency *f*
f is the frequency in GHz

$$Insertion\_loss(f) \le \left\{ \begin{array}{ll} 0.03 + 0.278\sqrt{f} + 0.28f & 0.01 \le f < 7 \\ -3.155 + 0.84f & 7 \le f \le 11.1 \end{array} \right\} \text{ (dB)} \qquad \text{(83B–2)}$$

where

Insertion_loss(*f*) is the differential insertion loss at frequency *f*
f is the frequency in GHz

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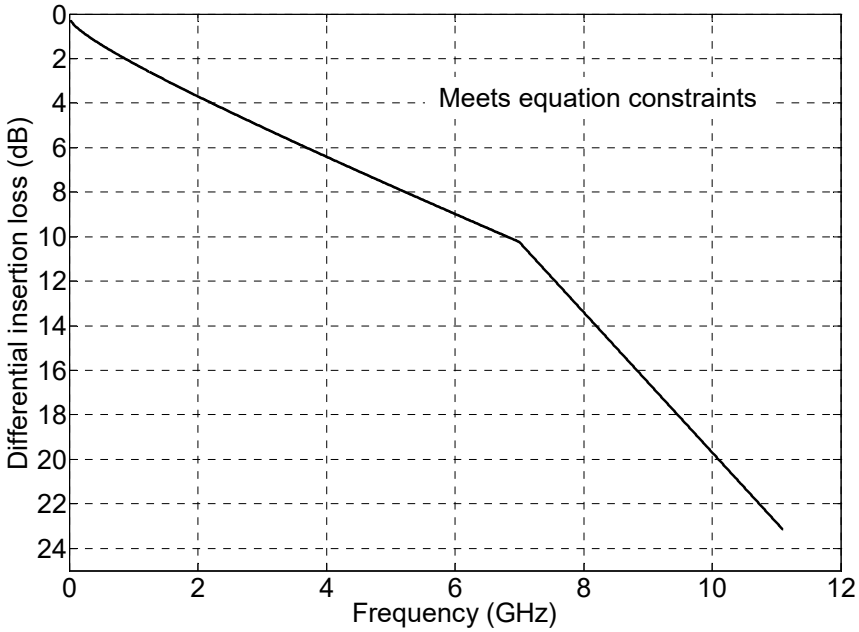

Figure 83B–1—Host insertion loss

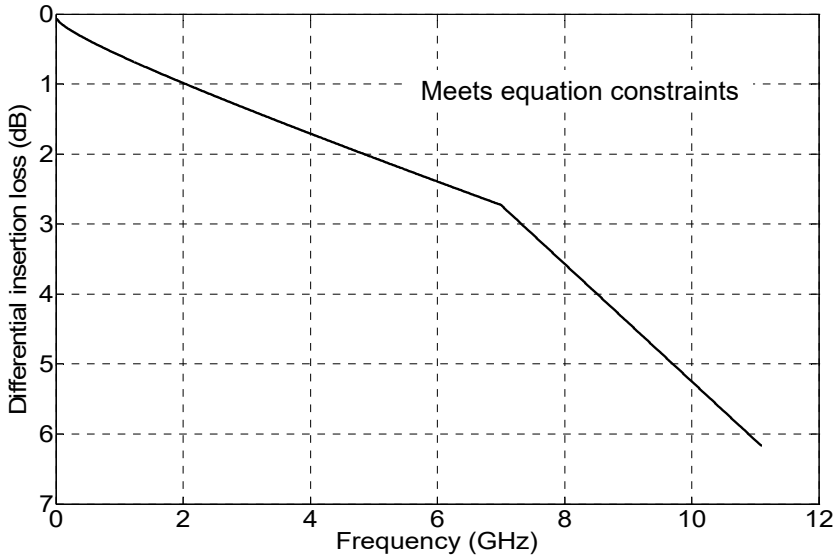

Figure 83B–2—Module insertion loss

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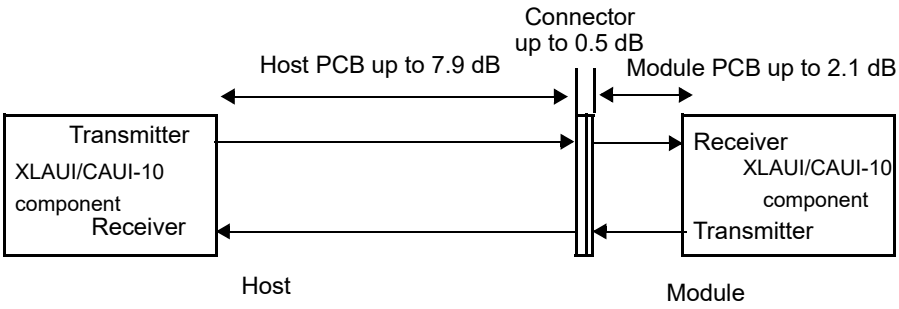

Figure 83B–3—Chip-to-module loss budget at 5.15625 GHz

Table 83B–1—Chip-to-module loss budget

Section	Differential insertion loss max. (at 5.15625 GHz)
Host XLAUI/CAUI-10 component to connector	7.9 dB
Connector loss	0.5 dB
Connector to module XLAUI/CAUI-10 component	2.1 dB

83B.2 Compliance point specifications for chip-to-module XLAUI/CAUI-10

The chip-to-module XLAUI/CAUI-10 interface specifies compliance points around the module connector as depicted in Figure 83B–5 and Figure 83B–7. Chip-to-module devices shall meet the electrical characteristics defined in 83B.2, 83B.2.1, 83B.2.2, and 83B.2.3. Compliance points are defined to ensure interoperability between hosts and modules. A Module Compliance Board (MCB) is used to isolate the characteristics of the module, and a Host Compliance Board (HCB) is used to isolate the characteristics of the host. Figure 83B–5 and Figure 83B–7 include the loss associated with the HCB and MCB at 5.15625 GHz.

The reference differential insertion loss of the HCB PCB is given in Equation (83B–3) and illustrated in Figure 83B–4. The effects of differences between the insertion loss of an actual HCB and the reference insertion loss are to be accounted in the measurements.

$$Insertion\_loss(f) = 0.017 + 0.5\sqrt{f} + 0.1836f \qquad 0.01 \le f \le 11.1 \qquad \text{(83B–3)}$$

where

$Insertion\_loss(f)$ is the differential insertion loss at frequency f
f is the frequency in GHz

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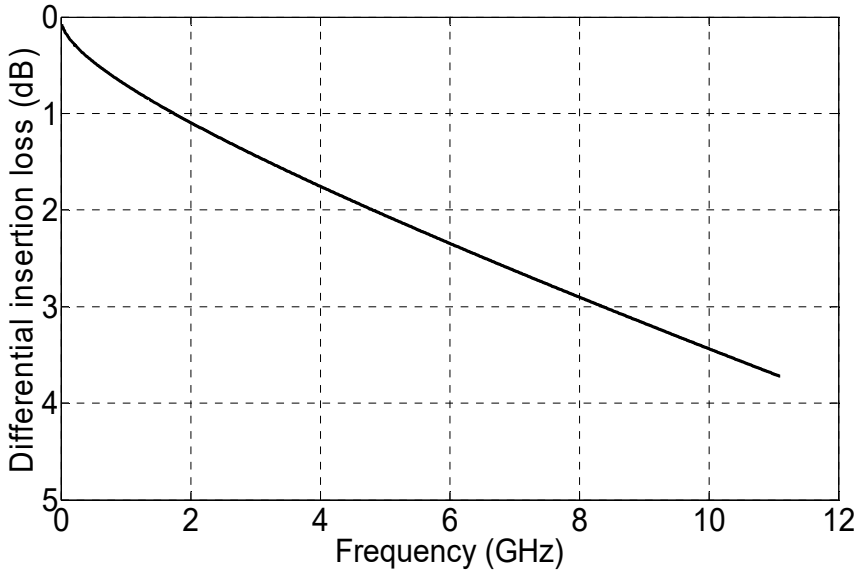

Figure 83B–4—HCB insertion loss

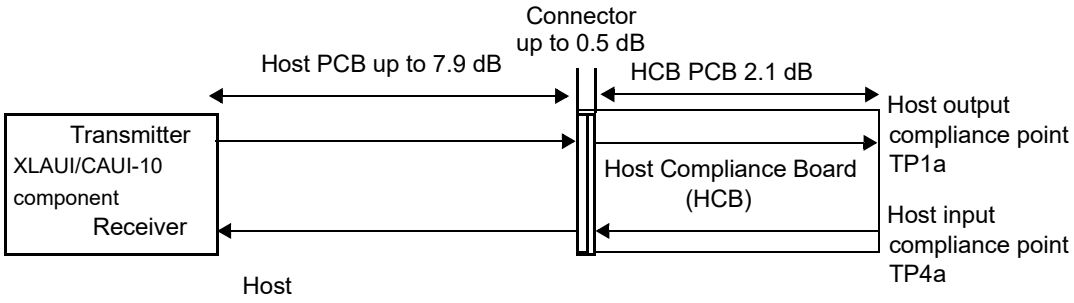

Figure 83B–5—Chip-to-module HCB insertion loss budget at 5.15625 GHz

The reference differential insertion loss of the MCB PCB is given in Equation (83B–4) and illustrated in Figure 83B–6. The effects of differences between the insertion loss of an actual MCB and the reference insertion loss are to be accounted in the measurements.

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$$Insertion\_loss(f) = -0.00086 + 0.2286\sqrt{f} + 0.08386f \quad \text{dB} \qquad 0.01 \le f \le 11.1 \qquad (83B–4)$$

where

Insertion_loss(*f*) is the differential insertion loss at frequency *f*
f is the frequency in GHz

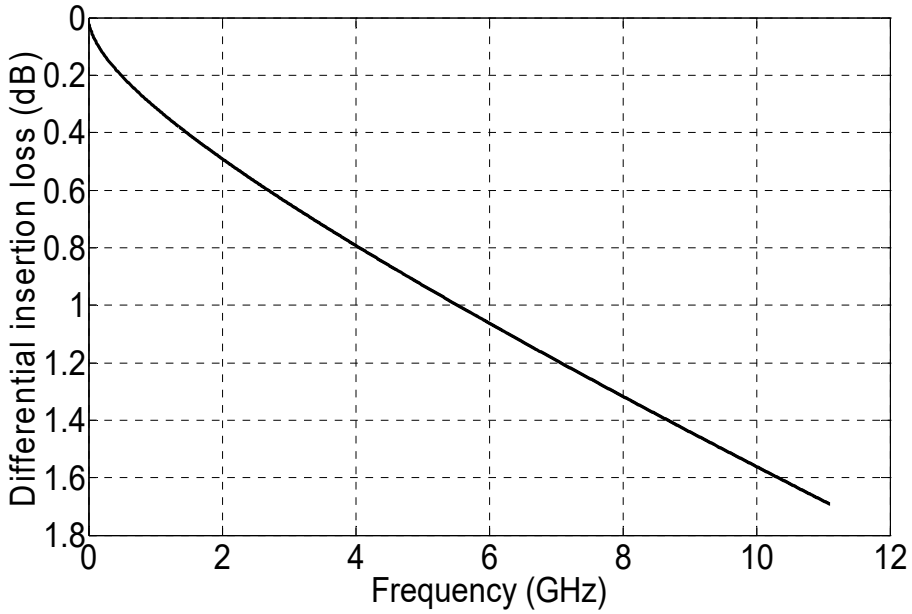

Figure 83B–6—MCB insertion loss

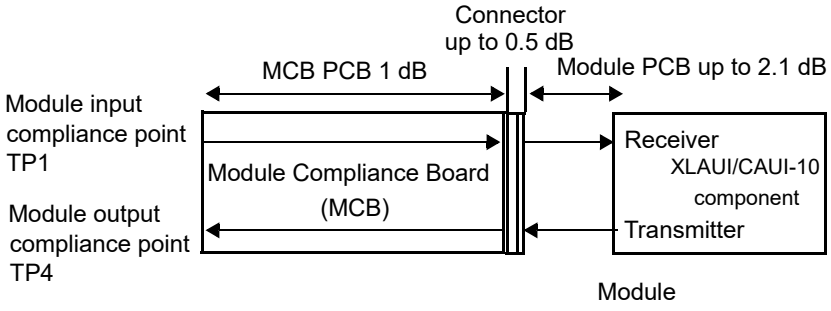

Figure 83B–7—Chip-to-module with MCB insertion loss budget at 5.15625 GHz

83B.2.1 Module specifications

A module that uses XLAUI/CAUI-10 to interface with a host shall meet the characteristics outlined in Table 83B–2 and Table 83B–3 when measured using the MCB and HCB (where the HCB is used to calibrate

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inputs to the module). Table 83B–2 also lists the equivalent test points for the XLPPI/CPPI (see Figure 86–3).

Modules may support additional de-emphasis states, but the specification of additional states is outside the scope of this standard. De-emphasis shall be off during eye mask and jitter testing. Module electrical output de-emphasis off state is the optimal setting for module electrical output jitter and eye mask evaluation. AC-coupling for both Tx and Rx paths shall be located in the module.

Table 83B–2—Specifications at module compliance points

Reference	Compliance point		Value	Unit
Minimum module differential input return loss	MCB input	TP1	See Equation (83B–5)	dB
Module input tolerance signal	HCB output	TP1a	See 83A.5.2	
Module output signal	MCB output	TP4	See Table 83B–3	
Minimum module differential output return loss	MCB output	TP4	See Equation (83B–5)	dB

$$Return\_loss(f) \geq \begin{cases} 12 - 2\sqrt{f} & 0.01 \leq f < 2.19 \\ 5.56 - 8.7\log_{10}\left(\frac{f}{5.5}\right) & 2.19 \leq f \leq 11.1 \end{cases} \text{ (dB)} \qquad (83B–5)$$

where

Return_loss(*f*) is the differential input return loss at frequency *f*
f is the frequency in GHz

Minimum module differential input/output return loss is illustrated in Figure 83B–8.

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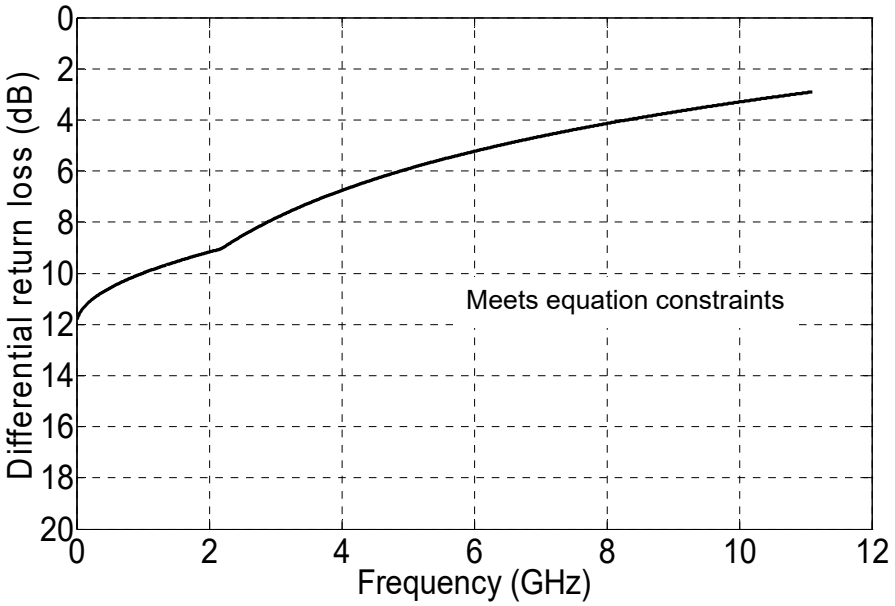

Figure 83B–8—Module input/output return loss

Table 83B–3—Module electrical output

Parameter	Subclause reference	Value	Unit
Maximum differential output voltage, peak-to-peak	83A.3.4.1	760	mV
Minimum de-emphasis	83A.3.4.1	3.5	dB
Maximum de-emphasis	83A.3.4.1	6	dB
Minimum VMA	83A.3.4.1	See Equation (83B–6)	mV
Maximum termination mismatch at 1 MHz	86A.5.3.2	5	%
Maximum output AC common-mode voltage, RMS	86A.5.3.1	15	mV
Minimum output rise and fall time (20% to 80%)	83A.3.4.2	24	ps
Maximum Total Jitter	83A.3.4.5	0.4	UI
Maximum Deterministic Jitter	83A.3.4.5	0.25	UI
Module electrical output eye mask definition X1	83A.3.4.5	0.2	UI
Module electrical output eye mask definition X2	83A.3.4.5	0.5	UI
Module electrical output eye mask definition Y1	83A.3.4.5	136	mV
Module electrical output eye mask definition Y2	83A.3.4.5	380	mV

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$$\text{Minimum VMA (mV)} = (-110 - 2.13x + 0.32x^2) \times (10^{-y/20}) \quad (83B–6)$$

where

x is the rise or fall time, or 38, (whichever is larger) in ps
y is de-emphasis value in dB

83B.2.2 Host specifications

A host that uses XLAUI/CAUI-10 to interface with a module shall meet the characteristics outlined in Table 83B–4 and Table 83B–5 when measured using the HCB and MCB (where MCB is used to calibrate inputs to the host). Table 83B–4 also lists the equivalent test points for the XLPPI/CPPI.

Table 83B–4—Specifications at host compliance points

Reference	Compliance point		Value	Unit
Host output signal specifications	HCB output	TP1a	See Table 83B–5	
Minimum host differential output return loss	HCB output	TP1a	See Equation (83B–7)	dB
Minimum host differential input return loss	HCB input	TP4a	See Equation (83B–7)	dB
Host input tolerance signal	MCB output	TP4	See 83B.2.3	

$$Return\_loss(f) \geq \begin{cases} 12 - 2\sqrt{f} & 0.01 \leq f < 2.19 \\ 5.56 - 8.7\log_{10}\left(\frac{f}{5.5}\right) & 2.19 \leq f \leq 11.1 \end{cases} \text{ (dB)} \quad (83B–7)$$

where

$Return\_loss(f)$ is the differential input/output return loss at frequency f
f is the frequency in GHz

Minimum host differential input/output return loss is illustrated in Figure 83B–9.

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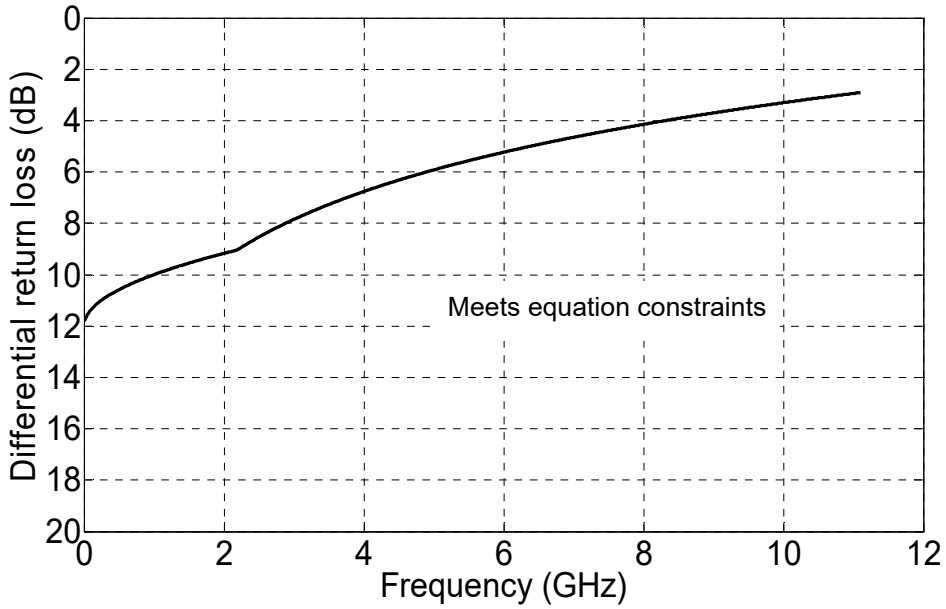

Figure 83B–9—Host input/output return loss

Table 83B–5—Host electrical output

Parameter	Subclause reference	Value	Units
Maximum output AC common-mode voltage, RMS	86A.5.3.1	20	mV
Minimum output rise and fall time (20% to 80%)	83A.3.4.2	24	ps
Maximum Total Jitter	83A.3.4.5	0.62	UI
Maximum Deterministic Jitter	83A.3.4.5	0.42	UI
Host electrical output eye mask definition X1	83A.3.4.5	0.31	UI
Host electrical output eye mask definition X2	83A.3.4.5	0.5	UI
Host electrical output eye mask definition Y1	83A.3.4.5	42.5	mV
Host electrical output eye mask definition Y2	83A.3.4.5	425	mV

83B.2.3 Host input signal tolerance

Host XLAUI/CAUI-10 jitter tolerance evaluation shall be defined by a stressed input signal that comprises 0.25 UI Deterministic Jitter, and 0.15 UI random jitter for BER 10^{-12}. Deterministic Jitter is added to a clean test pattern as sinusoidal jitter defined in 83A.3.5.6. The limited low-pass filter stress is added until the 0.22 UI Deterministic Jitter is achieved. Frequency-dependent attenuation is then added using PCB trace or frequency-dependent attenuation that emulates PCB loss. Frequency-dependent attenuation is added until 0.25 UI Deterministic Jitter is achieved. Random jitter is added to the test signal using an interference generator, which is a broadband noise source capable of producing white Gaussian noise with adjustable

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amplitude. The power spectral density shall be flat to ±3 dB from 50 MHz to 6 GHz with a crest factor of no less than 5. Figure 83B–10 depicts a XLAUI/CAUI-10 jitter tolerance test setup. The amplitude and output jitter of the filter stress plus limiter and random jitter injection shall meet the receiver eye mask illustrated in Figure 83A–9 with the values for X1, X2, Y1, Y2 given in Table 83B–3. All XLAUI/CAUI-10 lanes shall be active during jitter tolerance testing. The PRBS31 pattern defined in 83.5.10 or scrambled idle defined in 82.2.11 is used for evaluating XLAUI/CAUI-10 jitter tolerance.

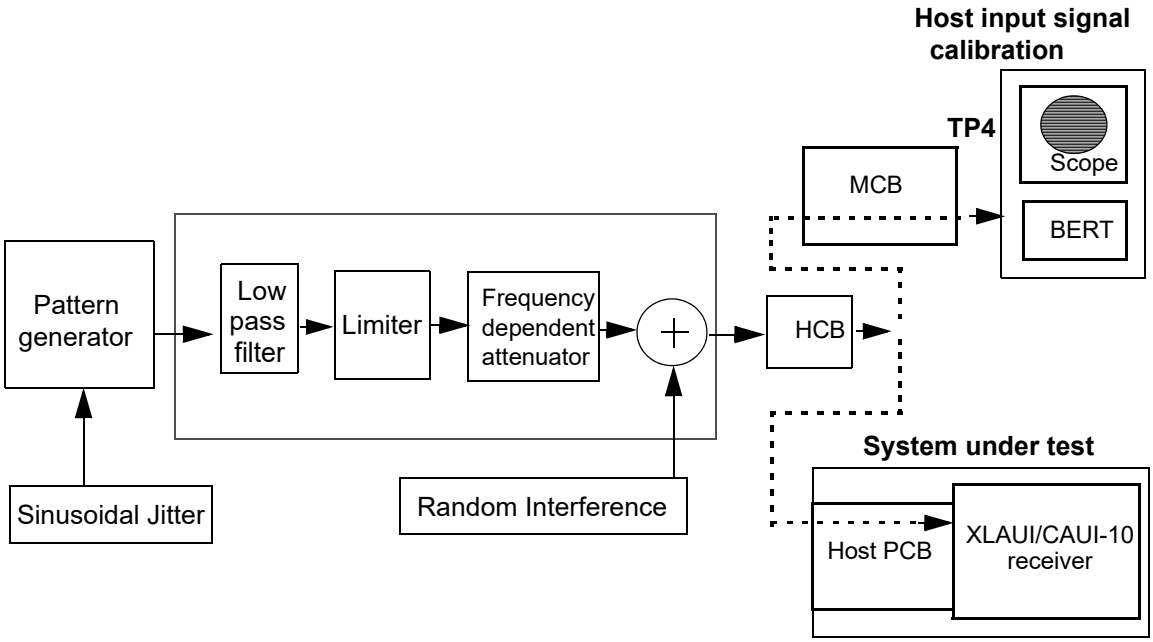

Figure 83B–10—Stressed-eye and jitter tolerance test setup

83B.3 Environmental specifications

83B.3.1 General safety

Equipment subject to this annex shall conform to the general safety requirements in J.2.

83B.3.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

83B.3.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

83B.3.4 Electromagnetic compatibility

A system integrating the XLAUI/CAUI-10 shall comply with applicable local and national codes for the limitation of electromagnetic interference.

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83B.3.5 Temperature and humidity

A system integrating the XLAUI/CAUI-10 is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

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83B.4 Protocol implementation conformance statement (PICS) proforma for Annex 83B, Chip-to-module 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10)[295]

83B.4.1 Introduction

The supplier of a chip to module XLAUI/CAUI-10 implementation that is claimed to conform to Annex 83B, Chip-to-module 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the same, can be found in Clause 21.

83B.4.2 Identification

83B.4.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

83B.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 83B, Chip-to-module 40 Gb/s Attachment Unit Interface (XLAUI) and 100 Gb/s ten-lane Attachment Unit Interface (CAUI-10)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[295] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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83B.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	XLAUI is organized into four lanes, CAUI-10 is organized into ten lanes	83A.1.2	See Clause 83	M	Yes [ ]
RATE	Each XLAUI/CAUI-10 lane operates at 10.3125 Gb/s	83A.1.2	10.3125 Gb/s (nominal)	M	Yes [ ]
IO	Meets chip-module XLAUI/CAUI-10 Electrical Characteristics	83B.2	Supports host/module compliance points	M	Yes [ ]

83B.4.4 Module requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MC1	XLAUI/CAUI-10 compliant module	83B.2.1	Meets requirements defined in Table 83B–2 and Table 83B–3	M	Yes [ ]
MC2	De-emphasis setting during module jitter evaluation	83B.2.1	Off	M	Yes [ ]
MC3	AC-coupling for Tx and Rx	83B.2.1	Present in module	M	Yes [ ]

83B.4.5 Host requirements

Item	Feature	Subclause	Value/Comment	Status	Support
HC1	XLAUI/CAUI-10 compliant host	83B.2.2	Meets requirements defined in Table 83B–4 and Table 83B–5	M	Yes [ ]
HC2	All XLAUI/CAUI-10 lanes active during jitter evaluation	83B.2.3	Yes	M	Yes [ ]
HC3	Applied jitter for host jitter tolerance evaluation	83B.2.3	0.25UI Deterministic Jitter, 0.15UI random jitter	M	Yes [ ]

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83B.4.6 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Conforms to J.2	83B.3.1	Yes	M	Yes [ ]
ES2	Compliance with applicable local and national codes for the limitation of electromagnetic interference	83B.3.4	Yes	M	Yes [ ]

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Annex 83C

(informative)

PMA sublayer partitioning examples

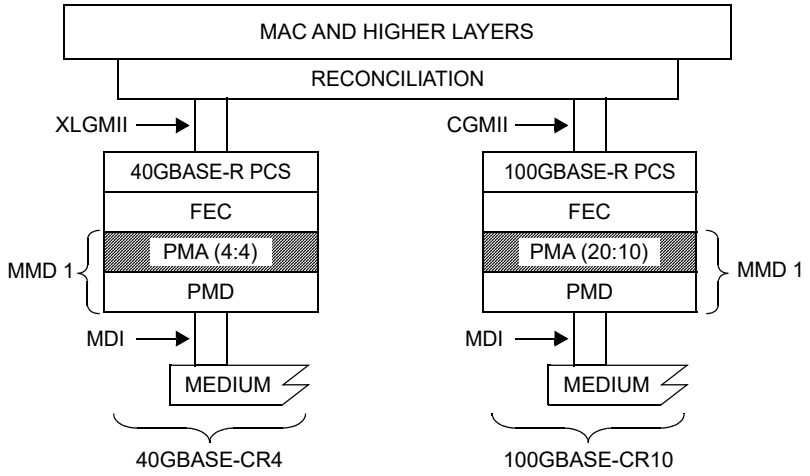
The following subclauses provide various partitioning examples. Partitioning guidelines and MMD numbering conventions are described in 83.1.4.

83C.1 Partitioning examples with FEC

The example of BASE-R FEC (see Clause 74) implemented in a separate device from either the PCS or the PMD is illustrated in Figure 83–2.

83C.1.1 FEC implemented with PCS

Figure 83C–1 depicts an example of FEC implemented with the PCS sublayer.



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 83C–1—Example FEC implemented with PCS

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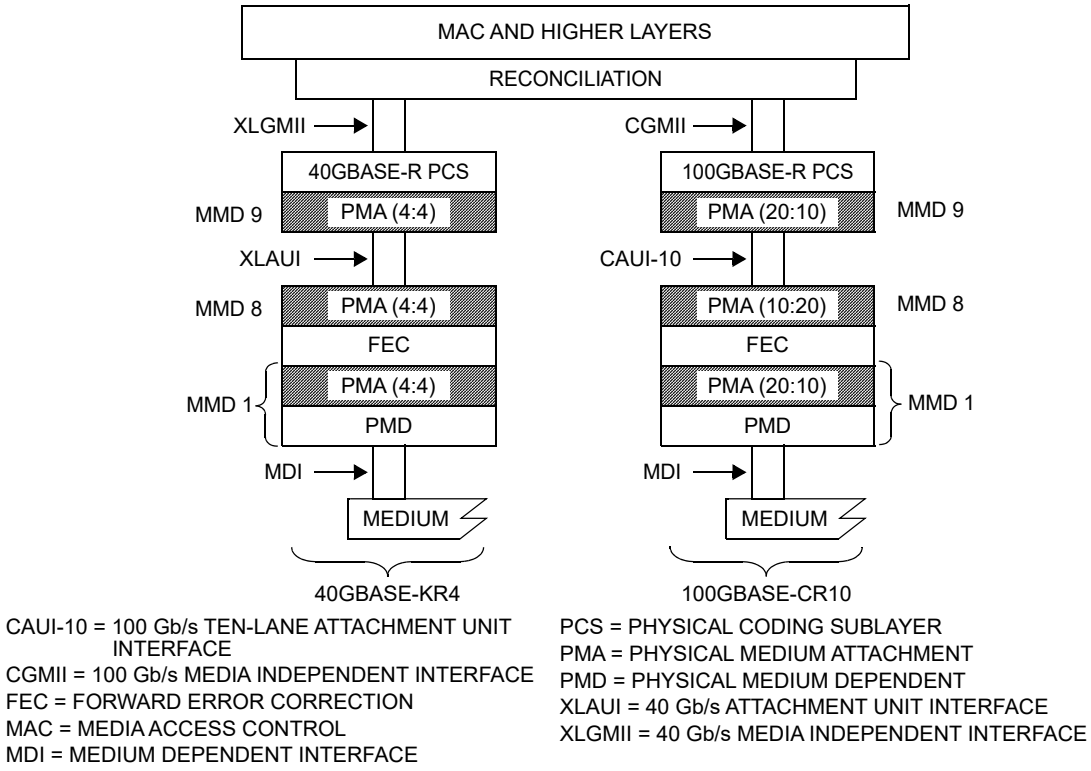
83C.1.2 FEC implemented with PMD

Figure 83C–2 depicts an example of FEC implemented with the PMD sublayer.



CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 83C–2—Example FEC implemented with PMD

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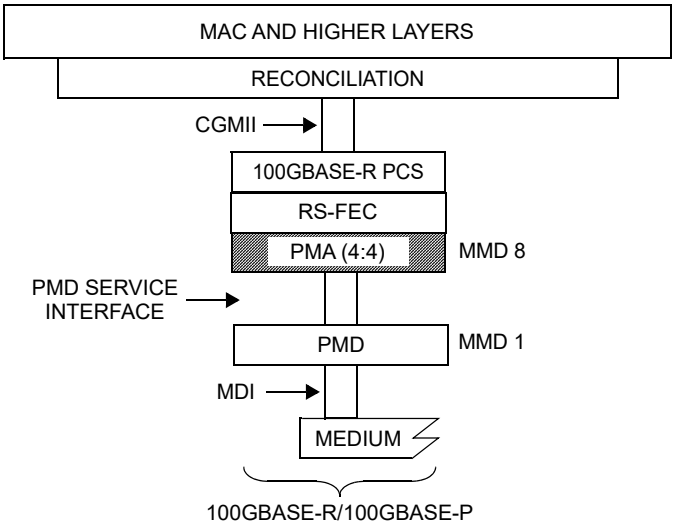
83C.2 Partitioning examples with RS-FEC

83C.2.1 Single PMA sublayer with RS-FEC

Figure 83C–3 depicts an example of a single PMA sublayer with RS-FEC.



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 83C–3—Example single PMA sublayer with RS-FEC

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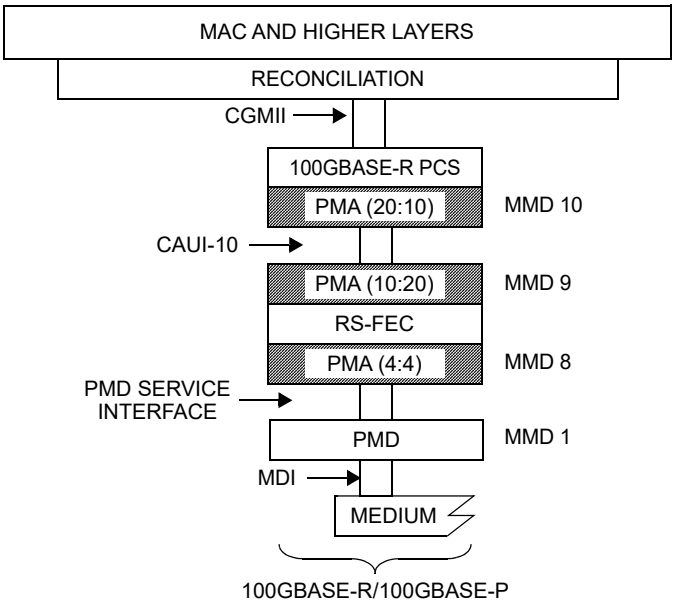
83C.2.2 Single CAUI-10 with RS-FEC

Figure 83C–4 depicts an example of a single CAUI-10 interface with RS-FEC.



CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 83C–4—Example single CAUI-10 with RS-FEC

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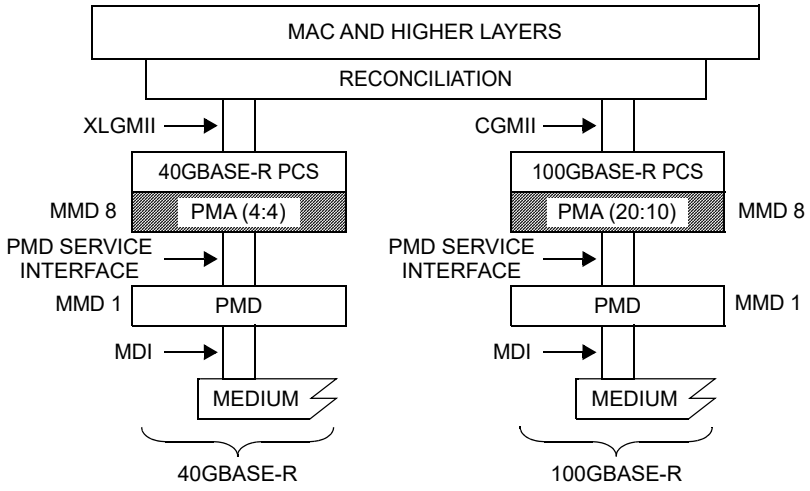
83C.3 Partitioning examples without FEC

83C.3.1 Single PMA sublayer without FEC

Figure 83C–5 depicts an example of a single PMA sublayer without FEC.



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

Figure 83C–5—Example single PMA sublayer without FEC

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83C.3.2 Single XLAUI/CAUI-4 without FEC

Figure 83C–6 depicts an example of a single XLAUI/CAUI-4 interface without FEC.

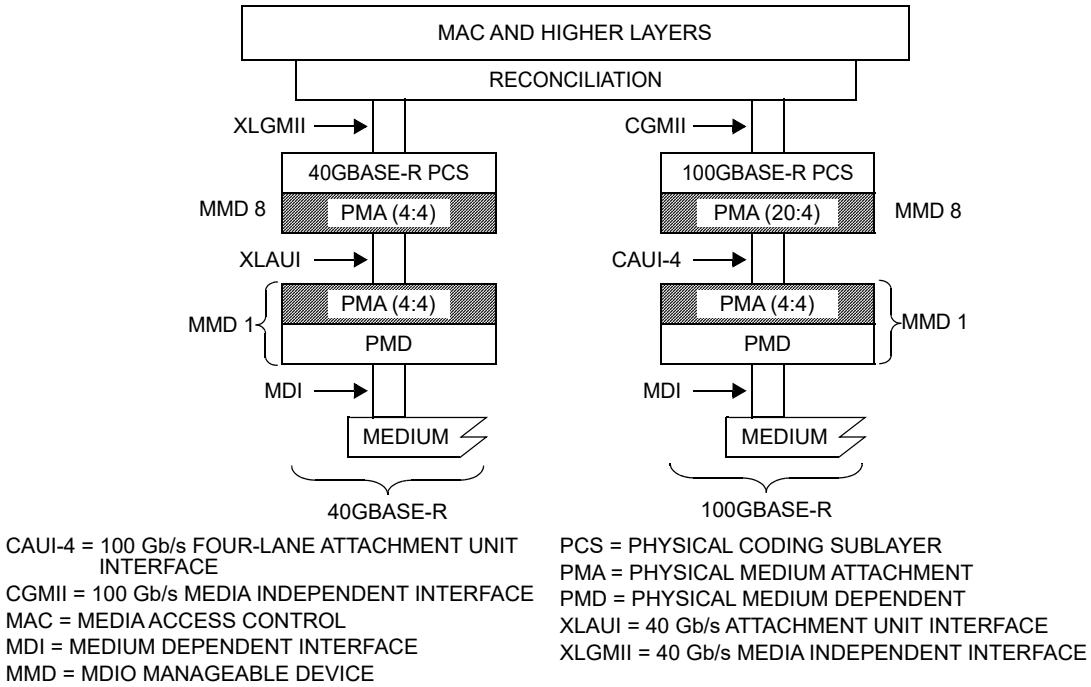

Figure 83C–6—Example single XLAUI/CAUI-4 without FEC

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83C.3.3 Separate SERDES for optical module interface

Figure 83C–7 depicts an example of a separate SERDES for an optical module interface.

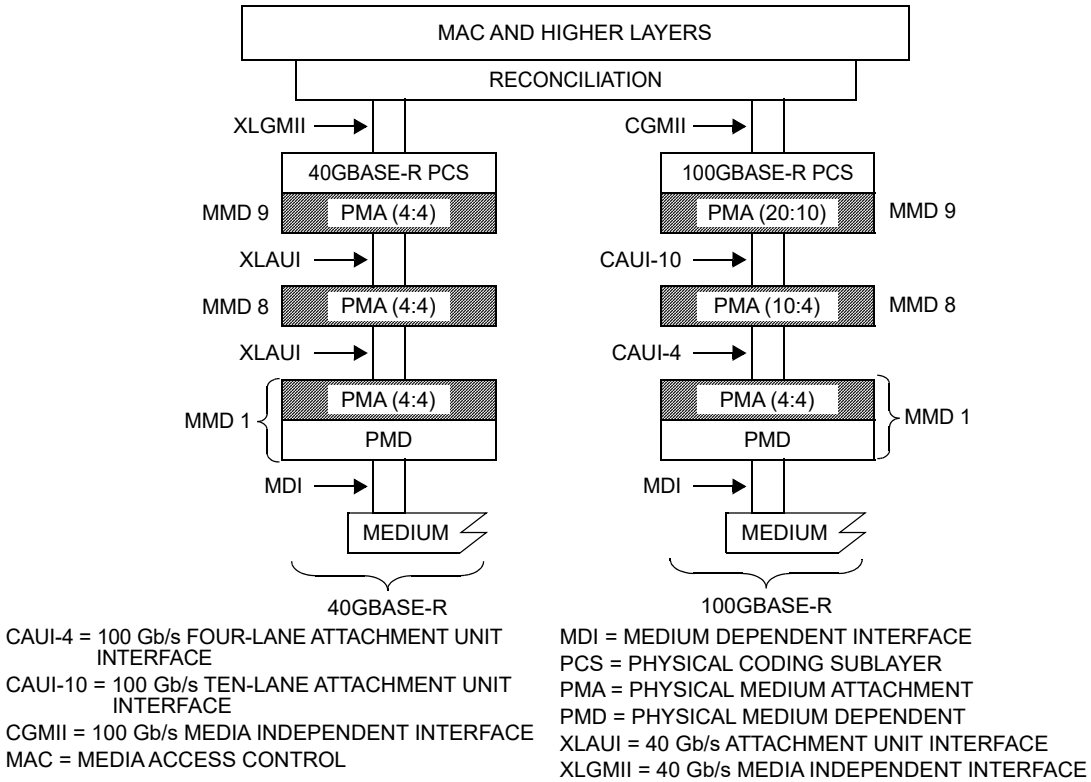

Figure 83C–7—Separate SERDES for optical module interface

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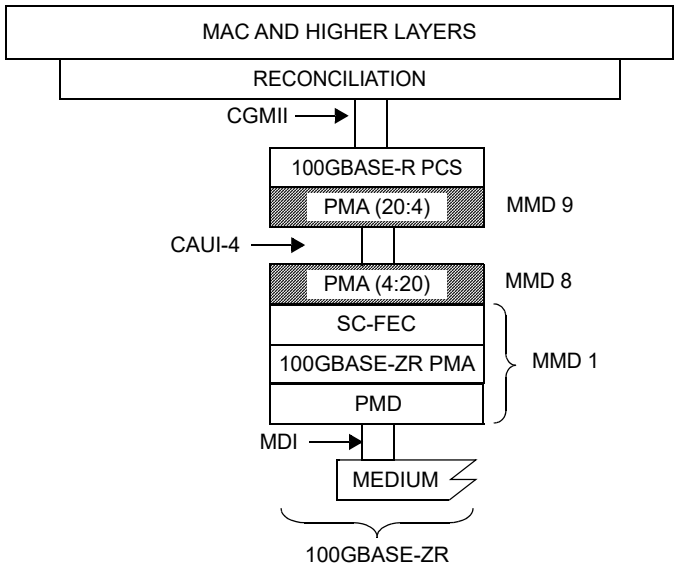
83C.4 Partitioning examples with SC-FEC

83C.4.1 CAUI-4 with SC-FEC

Figure 83C–8 depicts an example of a single CAUI-4 with SC-FEC.



CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
SC-FEC = STAIRCASE FORWARD ERROR CORRECTION

Figure 83C–8—Example single CAUI-4 with SC-FEC

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Annex 83D

(normative)

Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83D.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4). Figure 83D–1 shows an example relationship of the CAUI-4 chip-to-chip interface to the ISO/IEC Open System Interconnection (OSI) reference model. The chip-to-chip interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.

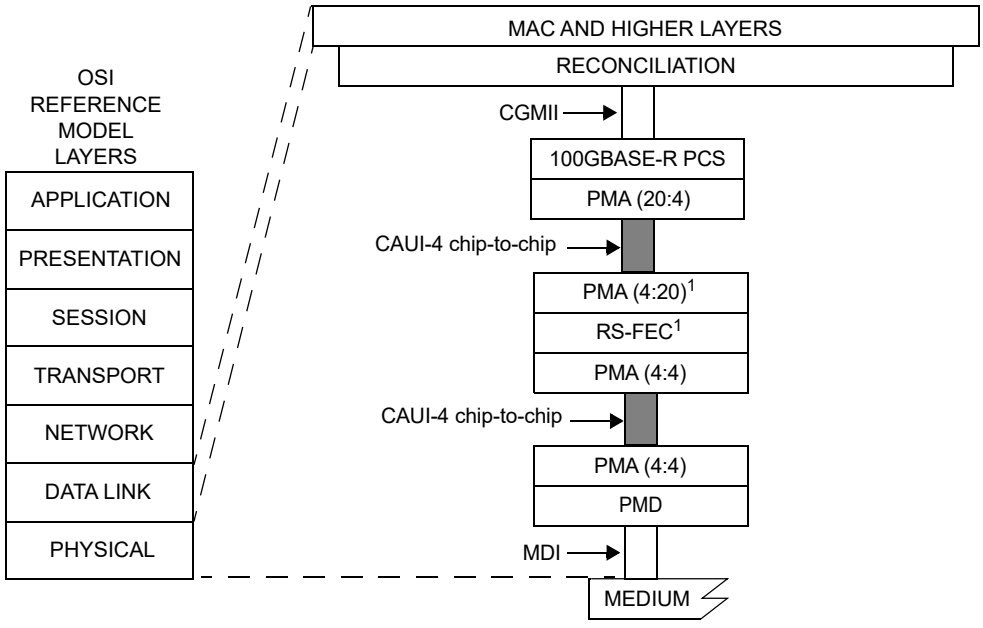

Figure 83D–1—Example CAUI-4 chip-to-chip relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The CAUI-4 bidirectional link is described in terms of a CAUI-4 transmitter, a CAUI-4 channel, and a CAUI-4 receiver. Figure 83D–2 depicts a typical CAUI-4 application, and Equation (83D–1) (illustrated in Figure 83D–3) summarizes the recommended differential insertion loss budget associated with the chip-to-chip application. The CAUI-4 chip-to-chip interface comprises independent data paths in each direction. Each data path contains four differential lanes, which are AC-coupled. The nominal signaling rate for each lane is 25.78125 GBd. The CAUI-4 transmitter on each end of the link is adjusted to an appropriate setting

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based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 83D.3.3.2 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.

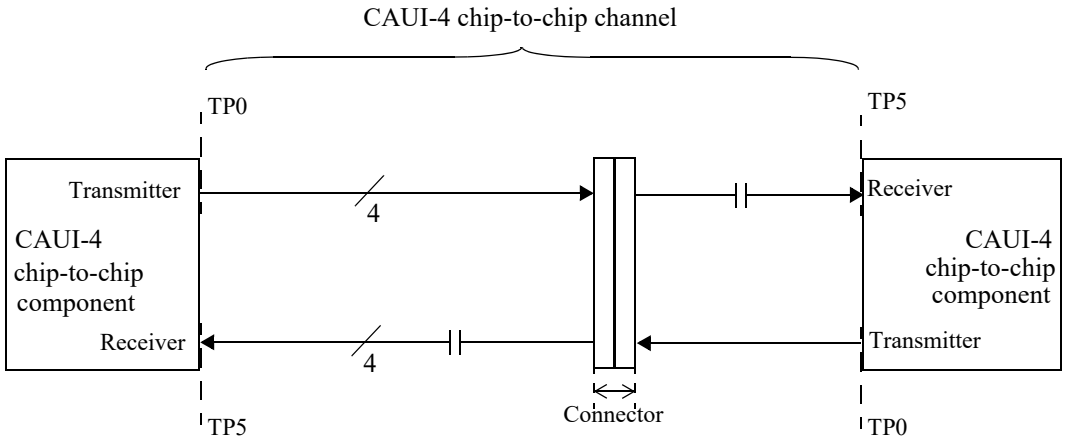

Figure 83D–2—Typical CAUI-4 chip-to-chip application

The normative channel compliance is through CAUI-4 COM as described in 83D.4. Actual channel loss could be higher or lower than that given by Equation (83D–1) due to the channel ILD, return loss, and cross-talk.

$$Insertion\_loss(f) \le \left\{ \begin{array}{cc} 1.083 + 2.543\sqrt{f} + 0.761f & 0.01 \le f < 12.89 \\ -17.851 + 2.936f & 12.89 \le f < 25.78 \end{array} \right\} \text{ (dB)} \qquad (83D–1)$$

where

f	is the frequency in GHz
Insertion_loss(f)	is the recommended CAUI-4 chip-to-chip insertion loss

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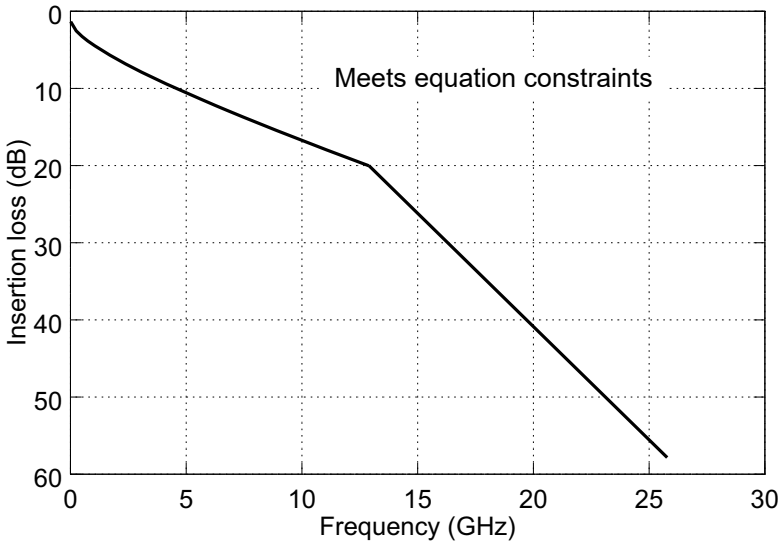

Figure 83D–3—CAUI-4 chip-to-chip channel insertion loss

83D.2 CAUI-4 chip-to-chip compliance point definition

The electrical characteristics for the CAUI-4 chip-to-chip interface are defined at compliance points for the transmitter (TP0a) and receiver (TP5a), respectively. The location of TP0a and electrical characteristics of the test fixture used to measure transmitter characteristics are defined in Figure 93–5 and 93.8.1.1, respectively. The location of TP5a and electrical characteristics of the test fixture used to measure the receiver are defined in Figure 93–10 and 93.8.2.1, respectively.

83D.3 CAUI-4 chip-to-chip electrical characteristics

83D.3.1 CAUI-4 transmitter characteristics

A CAUI-4 chip-to-chip transmitter shall meet the specifications defined in Table 83D–1 if measured at TP0a. While the CAUI-4 chip-to-chip transmitter requirements are similar to those in Clause 93, they differ in that they do not assume transmitter training or a back-channel communications path. Also, the transmit output waveform is not manipulated via the PMD control function described in 93.7.12, but may optionally be manipulated via the feedback mechanism described in 83D.3.3.2.

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified.

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Table 83D–1—CAUI-4 transmitter characteristics at TP0a

Parameter	Reference	Value	Units
Signaling rate per lane (range)	93.8.1.2	25.78125 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	93.8.1.3	 30 1200	 mV mV
Common-mode voltage (max)	93.8.1.3	1.9	V
Common-mode voltage (min)	93.8.1.3	0	V
AC common-mode output voltage (max, RMS)	93.8.1.3	12	mV
Differential output return loss (min)	93.8.1.4	Equation (93–3)	dB
Common-mode output return loss (min)	93.8.1.4	Equation (93–4)	dB
Output waveform[a] Steady state voltage v_f(max) Steady state voltage v_f(min) Linear fit pulse peak (min) Pre-cursor equalization Post-cursor equalization	 93.8.1.5.2[b] 93.8.1.5.2[b] 93.8.1.5.2[b] 83D.3.1.1 83D.3.1.1	 0.6 0.4 0.71 × v_f Table 83D–2 Table 83D–3	 V V V — —
Signal-to-noise-and-distortion ratio, SNDR (min)	93.8.1.6[b]	27	dB
Output Jitter (max) Even-odd jitter Effective bounded uncorrelated jitter, peak-to-peak[c] Effective total uncorrelated jitter, peak-to-peak[c,d]	92.8.3.8	 0.035 0.1 0.26	 UI UI UI

[a]The state of the transmit equalizer is controlled by management interface.
[b]The values of the parameters are measured as defined in the referenced subclause except that the values of N_p and N_w are 5.
[c]Effective bounded uncorrelated jitter and effective total uncorrelated jitter are measured as defined in 92.8.3.8.2 except that the range for fitting $CDFL_i$ and $CDFR_i$, as defined in 92.8.3.8.2 c), shall be from 10^{-6} to 10^{-4}.
[d]Effective total uncorrelated jitter, peak-to-peak is specified to a 10^{-15} probability.

83D.3.1.1 Transmitter equalization settings

The CAUI-4 chip-to-chip transmitter includes programmable equalization to compensate for the frequency-dependent loss of the channel and to facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in Figure 83D–4. The transmitter output equalization is characterized using the linear fit method described in 93.8.1.5.1 where the state of the CAUI-4 transmit output is manipulated via management.

The variable *Local_eq_cm1* controls the weight of the pre-cursor tap c(–1), by changing the ratio c(–1)/(|c(–1)|+|c(0)|+|c(1)|). The valid values of *Local_eq_cm1* and the corresponding ratios are specified in Table 83D–2. The variable *Local_eq_c1* controls the weight of the post-cursor tap c(1), by changing the ratio c(1)/(|c(–1)|+|c(0)|+|c(1)|). The valid values of *Local_eq_c1* and the corresponding ratios are specified in Table 83D–3. *Local_eq_cm1* and *Local_eq_c1* are independent of each other and independent on each lane. Each successive step in *Local_eq_cm1* and *Local_eq_c1* value shall result in a monotonic change in transmitter equalization.

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If a Clause 45 MDIO is implemented, *Local_eq_cm1* and *Local_eq_c1* for each lane (0 through 3) and direction (transmit and receive) are accessible through registers 1.180 through 1.187 (see 45.2.1.112 through 45.2.1.115).

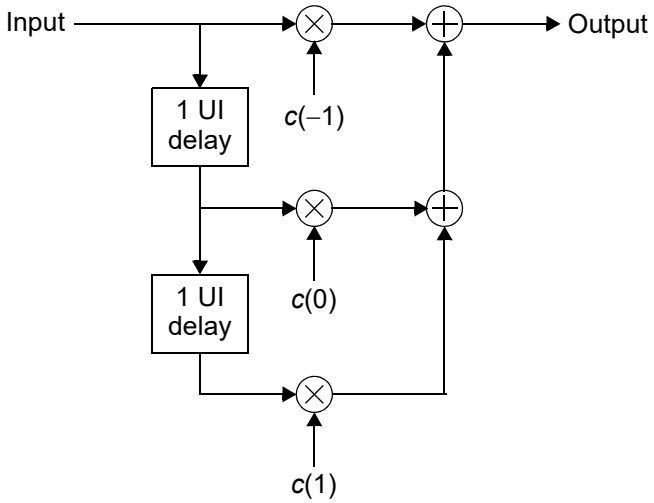

Figure 83D–4—Transmit equalizer functional model

.

Table 83D–2—Pre-cursor equalization

***Local_eq_cm1* value**	***c*(–1) ratio** $\left(\frac{c(-1)}{\lvert c(-1)\rvert + \lvert c(0)\rvert + \lvert c(1)\rvert}\right)$
0	0 ±0.04
1	–0.05 ±0.04
2	–0.1 ±0.04
3	–0.15 ±0.04

83D.3.2 Optional EEE operation

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78 and 78.3), then the inter-sublayer service interface includes four additional primitives as described in 83.3 and may also support CAUI-4 shutdown.

If the EEE capability includes CAUI-4 shutdown (see 78.5.2), then when aui_tx_mode (see 83.5.11.3) is set to ALERT, the transmit direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00, which is transmitted across the CAUI-4. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When aui_tx_mode is QUIET, the transmit direction CAUI-4 transmitter is disabled as specified below. Similarly when the received aui_tx_mode is set to ALERT, the receive direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00, which is transmitted across the CAUI-4. This sequence is

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Table 83D–3—Post-cursor equalization

Local_eq_c1 value	*c*(1) ratio $\left(\frac{c(1)}{\lvert c(-1)\rvert + \lvert c(0)\rvert + \lvert c(1)\rvert}\right)$
0	0 ±0.04
1	–0.05 ±0.04
2	–0.1 ±0.04
3	–0.15 ±0.04
4	–0.2 ±0.04
5	–0.25 ±0.04

transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When the received aui_tx_mode is QUIET, the receive direction CAUI-4 transmitter is disabled as specified below.

For EEE capability with CAUI-4 shutdown, the CAUI-4 transmitter lane's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of aui_tx_mode changing to QUIET in the relevant direction. Furthermore, the CAUI-4 transmitter lane's differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of aui_tx_mode ceasing to be QUIET in the relevant direction.

Global transmit disable is optional for EEE capability. The transmit disable function shall turn off all transmitter lanes for a physically instantiated AUI in either the ingress or the egress direction. In the egress direction, the PMA may turn off all the transmitter lanes for the egress direction CAUI-4 if PEASE is asserted and aui_tx_mode is QUIET. In the ingress direction, the PMA may turn off all the transmitter lanes for the ingress direction CAUI-4 if PIASE is asserted and the received aui_tx_mode is QUIET. In both directions, the transmit disable function shall turn on all transmitter lanes after the appropriate direction aui_tx_mode changes to any state other than QUIET within a time and voltage level specified in this subclause.

83D.3.3 CAUI-4 receiver characteristics

A CAUI-4 chip-to-chip receiver shall meet the specifications defined in Table 83D–4 if measured at TP5a.

Table 83D–4—CAUI-4 receiver characteristics at TP5a

Parameter	Subclause reference	Value	Units
Differential input return loss (min)	93.8.2.2	Equation (93–3)	dB
Differential to common-mode input return loss	93.8.2.2	Equation (93–5)	dB
Interference tolerance	83D.3.3.1	Table 83D–5	—

83D.3.3.1 Receiver interference tolerance

The receiver shall satisfy the requirements for interference tolerance defined in Table 83D–5. The interference tolerance test uses the method described in Annex 93C as specified by 93.8.2.3, with the following exceptions:

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a) The parameters in Table 83D–5 replace the parameters in Table 93–6.

b) The transmitter taps are set via management (see 83D.3.1.1) to the settings that provide the lowest BER.

c) Sinusoidal jitter is added to the test transmitter by modulating the clock source.

Table 83D–5—Receiver interference tolerance parameters

Parameter	Test 1 values			Test 2 values			Units
	Min	Max	Target	Min	Max	Target	
Bit error ratio[ab]	—	10^{-15}		—	10^{-15}		—
Applied pk-pk sinusoidal jitter			Table 8 8–13			Table 8 8–13	
Insertion loss at 12.89 GHz[c]	19.5	20.5		9.5	10.5		dB
Coefficients of fitted insertion loss[d] a_0 a_1 a_2 a_4	 –1 0 0 0	 2 2.937 1.599 0.03		 –1 0 0 0	 1 0.817 0.801 0.01		 dB dB/GHz$^{1/2}$ dB/GHz dB/GHz^2
RSS_DFE2[e]	0.05	—		0.025	—		—
COM including effects of broad-band noise	—	—	2	—	—	2	dB

[a]Bit error ratio replaces the RS symbol error ratio measurement in 93.8.2.3.
[b]Maximum BER assumes errors are not correlated to ensure sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding. Actual implementation of the receiver is beyond the scope of this standard.
[c]Measured between TPt and TP5 (see Figure 93C–4).
[d]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C–4) using the method in 93A.3 with f_{min} = 0.05 GHz, and f_{max} = 25.78125 GHz, and maximum Δf = 0.01 GHz.
[e]RSS_DFE2 is equivalent to RSS_DFE4 described in 93A.2 except that n_1=2 and n_2=5.

83D.3.3.2 Transmitter equalization feedback (optional)

Transmitter equalization feedback is an optional capability for a CAUI-4 chip-to-chip receiver. If implemented, it shall operate as described in this subclause.

Transmitter equalization feedback is generated for each lane (0 through 3) and direction (transmit and receive) independently. The variables that control transmitter equalization feedback are specific for each lane and direction.

A CAUI-4 chip-to-chip receiver may generate a request to change the transmit equalization coefficients of the remote transmitter to new values by setting the *Request_flag* variable to 1. The variables *Requested_eq_cm1* and *Requested_eq_c1* indicate the request values of *Local_eq_cm1* and *Local_eq_c1*, respectively, in the remote transmitter (see Table 83D–2 and Table 83D–3). The requested setting may be generated from the remote CAUI-4 chip-to-chip transmitter's equalization setting, which is stored in variables *Remote_eq_cm1* and *Remote_eq_c1*, and from information internal to the receiver, in an implementation specific manner.

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When a CAUI-4 chip-to-chip receiver does not request a change of the remote transmitter's transmit equalization setting, it sets the *Request_flag* variable to 0. A CAUI-4 chip-to-chip receiver that does not implement transmitter equalization feedback always sets *Requests_flag* to 0.

If a Clause 45 MDIO is implemented, the variables *Request_flag, Requested_eq_cm1, Requested_eq_c1, Remote_eq_cm1,* and *Remote_eq_c1* for each lane and direction are accessible through registers 1.180 through 1.187 (see 45.2.1.112 through 45.2.1.115).

83D.3.4 Global energy detect function for optional EEE operation

The global energy detect function is mandatory for EEE capability with the deep sleep mode option and CAUI-4 shutdown. The global energy detect function indicates whether or not signaling energy is being received on the physical instantiation of the inter sublayer interface (in each direction as appropriate). The energy detection function may be considered a subset of the signal indication logic. If no energy is being received on the CAUI-4 for the ingress direction, SIGNAL_DETECT is set to FAIL following a transition from aui_rx_mode = DATA to aui_rx_mode = QUIET. When aui_rx_mode = QUIET, SIGNAL_DETECT shall be set to OK within 500 ns following the application of a signal at the receiver input that corresponds to an ALERT signal driven from the CAUI-4 link partner. While aui_rx_mode = QUIET, SIGNAL_DETECT changes from FAIL to OK only after the valid ALERT signal is received.

83D.4 CAUI-4 chip-to-chip channel characteristics

The Channel Operating Margin (COM), computed using the procedure in Annex 93A and the parameters in Table 83D–6, shall be greater than or equal to 2 dB. This minimum value allocates margin for practical limitations on the receiver implementation as well as the allowed transmitter equalization coefficients.

Table 83D–6—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	$f_{\min}$	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended board capacitance	 C_d z_p z_p C_p	 2.5×10^{-4} 12 30 1.8×10^{-4}	 nF mm mm nF
Single-ended reference resistance	R_0	50	ohms
Single-ended termination resistance	R_d	55	ohms
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.6	—
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.15 0 0.05	—

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Table 83D–6—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	—
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –12 0 1	dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	$f_b/4$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b/4$ f_b	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 Av A_{fe} A_{ne}	 0.4 0.4 0.6	 V V V
Number of signal levels	L	2	—
Level separation mismatch ratio	R_{LM}	1	
Transmitter signal-to-noise ratio	SNR_{TX}	27	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	5	UI
Normalized DFE coefficient magnitude limit, for $n = 1$ to N_b	$b_{max}(n)$	0.3	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.05	UI
One-sided noise spectral density	η_o	5.2×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-15}	—

83D.5 Example usage of the optional transmitter equalization feedback

83D.5.1 Overview

If implemented, transmitter equalization feedback from a CAUI-4 chip-to-chip receiver may be used to tune the equalization settings of the transmitter at the other end of the CAUI-4 chip-to-chip link to the values requested by the receiver. An example of a possible transmitter equalization tuning process using transmitter equalization feedback is provided in this subclause.

In this example, two components, A and B, are connected by a CAUI-4 chip-to-chip link, such that A is closest to the PCS and B is closest to the PMD. Clause 45 MDIO is implemented by both components, with component A at device address 11 and component B at device address 10. Transmitter equalization feedback is implemented by either component A, component B, or both. One Station Management (STA) controls both components.

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Figure 83D–5 depicts the components of the CAUI-4 chip-to-chip link and the registers used during the tuning procedure.

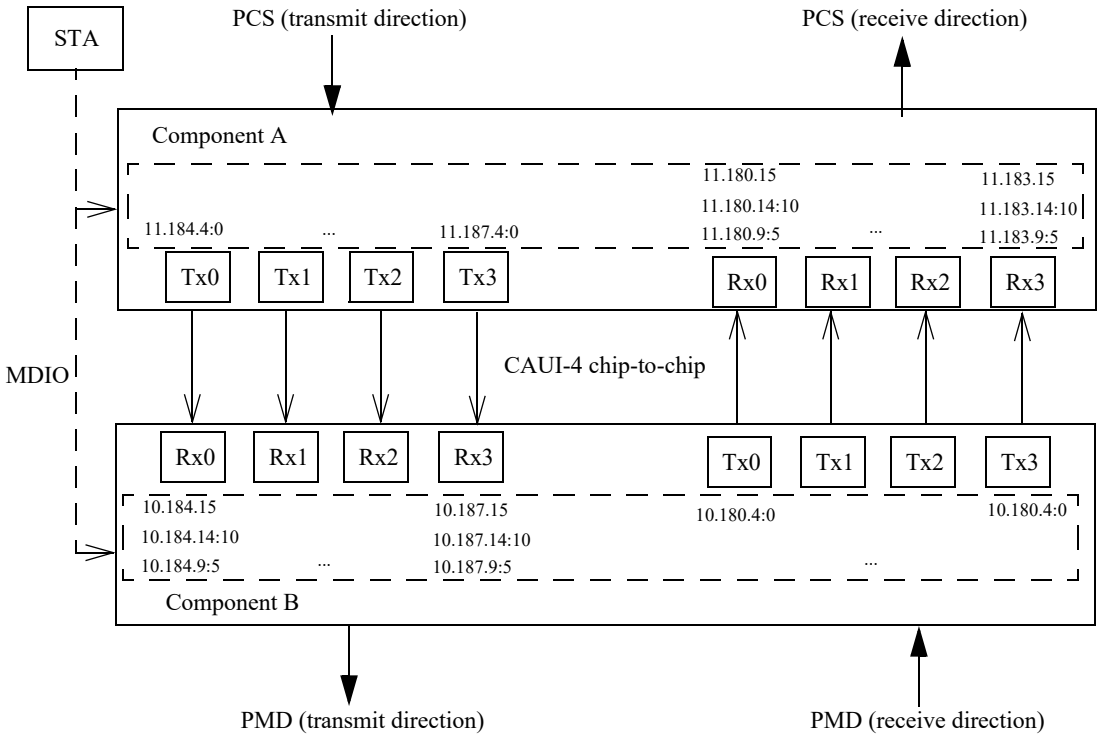

Figure 83D–5—Example transmitter equalization feedback components and registers

The STA performs the procedures described in 83D.5.2 and 83D.5.3 to tune lane 0 equalization settings in both sides of the CAUI-4 chip-to-chip link. When these procedures are completed, the STA uses similar procedures to tune equalization settings in lanes 1 through 3. When all lanes are tuned, the STA may repeat the process with another pair of components connected by CAUI-4 chip-to-chip.

NOTE—Using non-optimal transmitter equalization settings (or changing them) during the tuning procedure may interrupt data communication. The CAUI-4 bit error ratio is assumed to meet the requirements of 83D.3.3.1 upon completion of the tuning process.

83D.5.2 Tuning equalization settings on lane 0 in the transmit direction

1) Read *Local_eq_cm1* (11.184.1:0) and *Local_eq_c1* (11.184.4:2) from component A.
2) Write *Local_eq_cm1* and *Local_eq_c1* read from component A to *Remote_eq_cm1* (10.184.6:5) and *Remote_eq_c1* (10.184.9:7), respectively, in component B.
3) Read *Request_flag* (10.184.15), *Requested_eq_cm1* (10.184.11:10), and *Requested_eq_c1* (10.184.14:12) from component B.
4) If *Request_flag* is 0, go to tuning equalization settings on lane 0 in the Receive direction (83D.5.3).
5) If *Request_flag* is 1, write *Requested_eq_cm1* and R*equested_eq_c1* read from component B to *Local_eq_cm1* (11.184.1:0) and *Local_eq_c1* (11.184.4:2), respectively, in component A.
6) Go to step 1).

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83D.5.3 Tuning equalization settings on lane 0 in the receive direction

1) Read *Local_eq_cm1* (10.180.1:0) and *Local_eq_c1* (10.180.4:2) from component B.
2) Write *Local_eq_cm1* and *Local_eq_c1* read from component B to *Remote_eq_cm1* (11.180.6:5) and *Remote_eq_c1* (11.180.9:7), respectively, in component A.
3) Read *Request_flag* (11.180.15), *Requested_eq_cm1* (11.180.11:10), and *Requested_eq_c1* (11.180.14:12) from component A.
4) If *Request_flag* is 0, proceed to tuning lane 1.
5) If *Request_flag* is 1, write *Requested_eq_cm1* and *Requested_eq_c1* read from component A to *Local_eq_cm1* (10.180.1:0) and *Local_eq_c1* (10.180.4:2), respectively, in component B.
6) Go to step 1).

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83D.6 Protocol implementation conformance statement (PICS) proforma for Annex 83D, Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)[296]

83D.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 83D, Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

83D.6.2 Identification

83D.6.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

83D.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 83D, Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[296]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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83D.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	83D.1	Four independent data paths in each direction	M	Yes [ ]
*CHAN	Channel	83D.4	Items marked with CHAN include channel specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
*LPI	Support for CAUI-4 shutdown	83D.3.2		O	Yes [ ] No [ ]

83D.6.4 PICS proforma tables for chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83D.6.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	83D.3.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TC2	Peak-to-peak differential output voltage	83D.3.1	1200 mV (max)	M	Yes [ ]
TC3	Peak-to-peak differential output voltage, transmitter disabled	83D.3.1	Less than or equal to 30 mV	M	Yes [ ]
TC4	DC common-mode voltage	83D.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC5	AC common-mode output voltage	83D.3.1	12 mV RMS with respect to signal ground	M	Yes [ ]
TC6	Differential output return loss	83D.3.1	Meets Equation (93–3) constraints	M	Yes [ ]
TC7	Common-mode output return loss	83D.3.1	Meets Equation (93–4) constraints	M	Yes [ ]
TC8	Output waveform	83D.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC9	Output jitter	83D.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC10	Amplitude and swing for CAUI-4 shutdown	83D.3.2		LPI:M	Yes [ ] N/A [ ]
TC11	Transmit disable for CAUI-4 shutdown	83D.3.2		LPI:M	Yes [ ] N/A [ ]
TC12	Transmit equalization	83D.3.1.1	Each successive step results in a monotonic change	M	Yes [ ]

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83D.6.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	93.8.2.2	Meets Equation (93–3) constraints	M	Yes [ ]
RC2	Differential to common-mode input return loss	93.8.2.2	Meets Equation (93–5) constraints	M	Yes [ ]
RC3	Interference tolerance	83D.3.3.1	Satisfy requirements in Table 83D–5	M	Yes [ ]
RC4	Jitter tolerance	93.8.2.4	Satisfy requirements in Table 93–7	M	Yes [ ]
RC5	Signal detect for CAUI-4 shutdown	83D.3.4		LPI:M	Yes [ ] N/A [ ]

83D.6.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	83D.4	Greater than or equal to 2 dB	CHAN:M	Yes [ ] N/A [ ]

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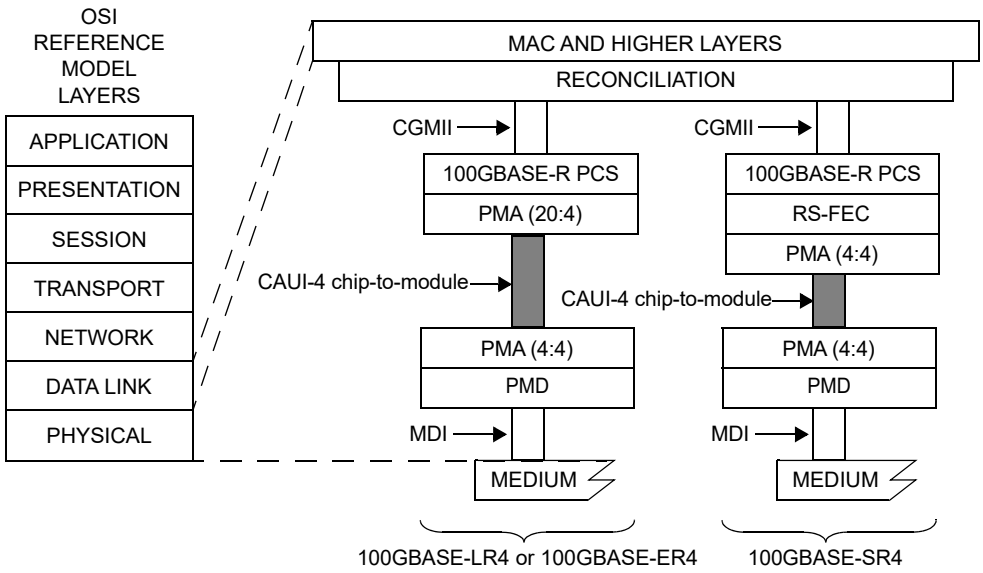
Annex 83E

(normative)

Chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83E.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4). Figure 83E–1 shows the relationship of the CAUI-4 chip-to-module interface to the ISO/IEC Open System Interconnection (OSI) reference model. The chip-to-module interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable module interfaces.



CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 83E–1—Example CAUI-4 chip-to-module relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The CAUI-4 link is described in terms of a host CAUI-4 component, a CAUI-4 channel with associated insertion loss, and a module CAUI-4 component. Figure 83E–2 and Equation (83E–1) depict a typical CAUI-4 application and summarize the differential insertion loss budget associated with the chip-to-module application, which is shown in Figure 83E–3. The CAUI-4 chip-to-module interface comprises independent data paths in each direction. Each data path contains four differential lanes, which are AC-coupled within the module. The nominal signaling rate for each lane is 25.78125 GBd. The chip-to-module interface is

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defined using a specification and test methodology that is similar to that used for CEI-28G-VSR defined in OIF-CEI-03.1 [B57].

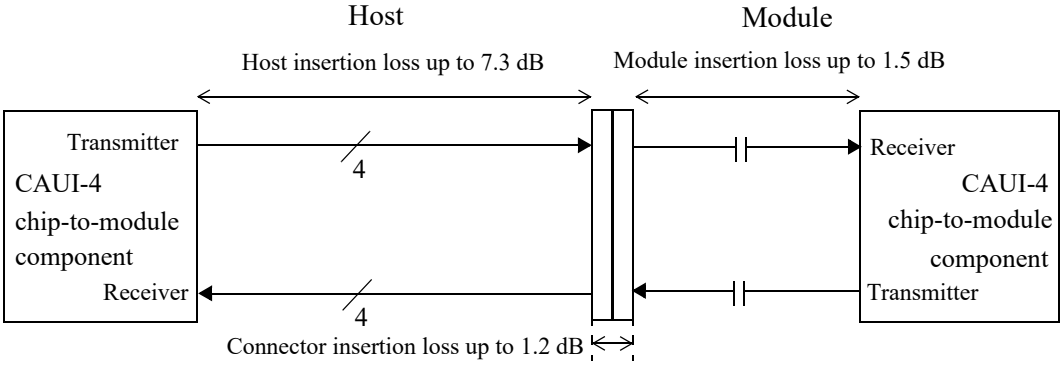

Figure 83E–2—Chip-to-module insertion loss budget at 12.89 GHz

$$Insertion\_loss(f) \le \begin{cases} 1.076(0.075 + 0.537\sqrt{f} + 0.566f) & 0.01 \le f < 14 \\ 1.076(-18 + 2f) & 14 \le f < 18.75 \end{cases} \text{ (dB)} \qquad (83E–1)$$

where

f is the frequency in GHz
Insertion_loss(f) is the CAUI-4 chip-to-module insertion loss

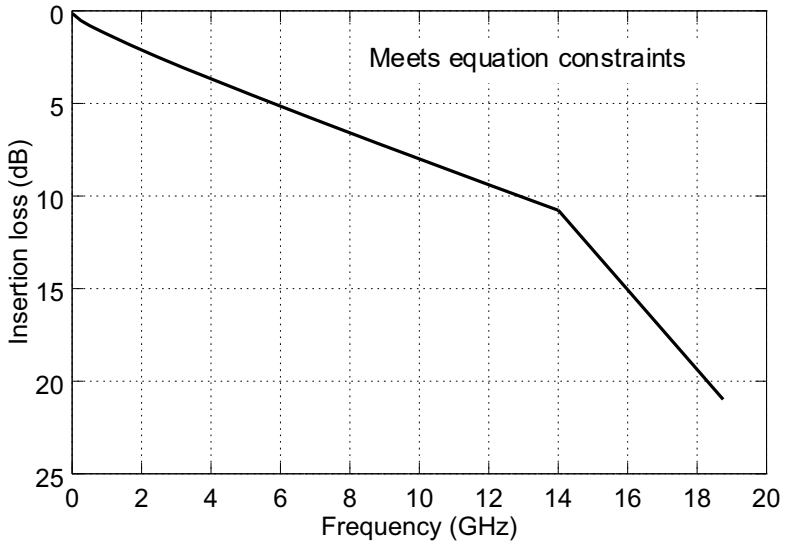

Figure 83E–3—CAUI-4 chip-to-module channel insertion loss

83E.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 10^{-15} with any errors sufficiently uncorrelated to ensure an acceptably high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding.

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83E.2 CAUI-4 chip-to-module compliance point definitions

The electrical characteristics for the CAUI-4 chip-to-module interface are defined at compliance points for the host and module, respectively. Reference test fixtures, called compliance boards, are used to access the electrical specification parameters. Figure 83E–4 depicts the location of compliance points when measuring host CAUI-4 compliance. The output of the Host Compliance Board (HCB) is used to verify the host electrical output signal at TP1a. Similarly, the input of the HCB at TP4a is used to verify the host input compliance.

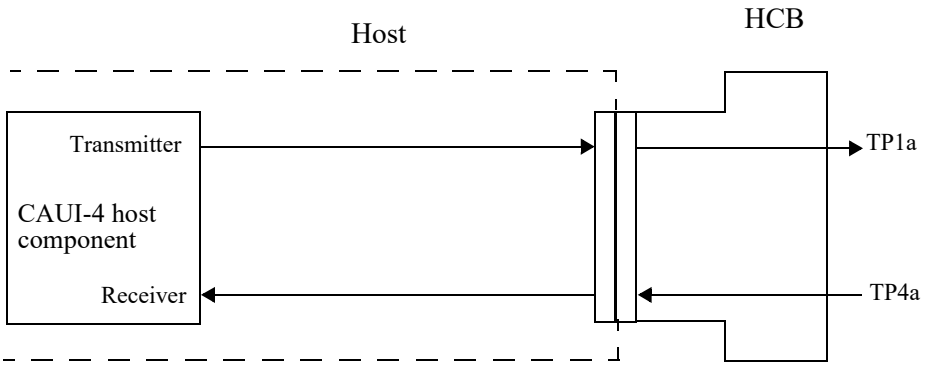

Figure 83E–4—Host CAUI-4 compliance points

Figure 83E–5 depicts the location of compliance points when measuring module CAUI-4 compliance. The output of the Module Compliance Board (MCB) is used to verify the module electrical output signal at TP4. Similarly, the input of the MCB at TP1 is used to verify the module input compliance. Additional details on the requirements for the MCB and HCB are given in 83E.4.1.

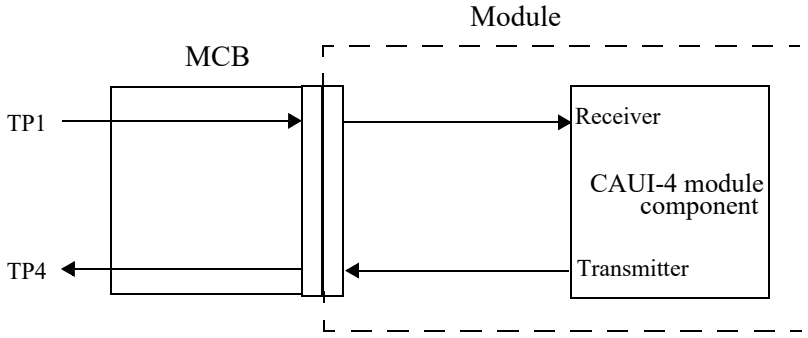

Figure 83E–5—Module CAUI-4 compliance points

83E.3 CAUI-4 chip-to-module electrical characteristics

83E.3.1 CAUI-4 host output characteristics

A CAUI-4 host output shall meet the specifications defined in Table 83E–1 if measured at TP1a.

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Table 83E–1—CAUI-4 host output characteristics at TP1a

Parameter	Reference	Value	Units
Signaling rate per lane (range)	83E.3.1.1	25.78125 ± 100 ppm	GBd
DC common-mode output voltage (max)	83E.3.1.2	2.8	V
DC common-mode output voltage (min)	83E.3.1.2	–0.3	V
Single-ended output voltage (max)	83E.3.1.2	3.3	V
Single-ended output voltage (min)	83E.3.1.2	–0.4	V
AC common-mode output voltage (max, RMS)	83E.3.1.2	17.5	mV
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	83E.3.1.2	 35 900	mV
Eye width (min)	83E.3.1.6	0.46	UI
Eye height A, differential (min)	83E.3.1.6	95	mV
Eye height B, differential (min)	83E.3.1.6	80	mV
Differential output return loss (min)	83E.3.1.3	Equation (83E–2)	dB
Common-to-differential-mode output return loss (min)	83E.3.1.3	Equation (83E–3)	dB
Differential termination mismatch (max)	83E.3.1.4	10	%
Transition time (min, 20% to 80%)	83E.3.1.5	10	ps

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

83E.3.1.1 Signaling rate and range

The CAUI-4 signaling rate is 25.78125 GBd ± 100 ppm per lane. This translates to a nominal unit interval of 38.787879 ps.

83E.3.1.2 Signal levels

The differential output voltage v_{di} is defined to be the difference between the single-ended output voltages, SL*i*<p> minus SL*i*<n>. The common-mode voltage v_{cmi} is defined to be one half of the sum of SL*i*<p> and SL*i*<n>. These definitions are illustrated by Figure 83E–6.

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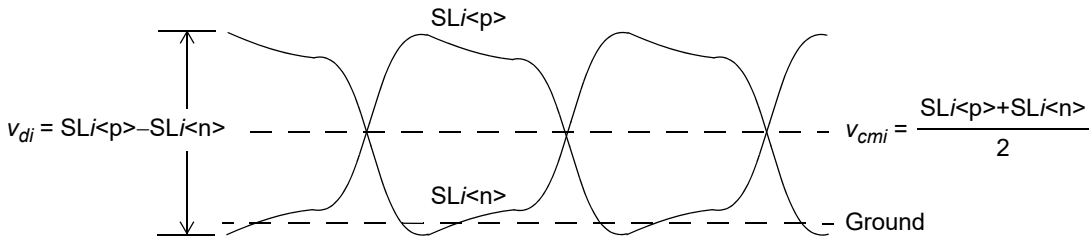

Figure 83E–6—Voltage definitions

The peak-to-peak differential output voltage is less than or equal to 900 mV. The peak-to-peak differential output voltage is less than or equal to 35 mV when the transmitter is disabled.

The DC common-mode output voltage and AC common-mode output voltage are defined with respect to signal ground.

83E.3.1.3 Output return loss

The differential output return loss, in dB, of the output is shown in Equation (83E–2) and illustrated in Figure 83E–7. This output requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 Ω.

$$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} \text{ (dB)} \quad \text{(83E–2)}$$

where

f	is the frequency in GHz
RLd	is the CAUI-4 chip-to-module host output differential return loss

Common-to-differential-mode output return loss, in dB, is shown in Equation (83E–3) and illustrated in Figure 83E–8.

$$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases} \text{ (dB)} \quad \text{(83E–3)}$$

where

f	is the frequency in GHz
$RLdc$	is the CAUI-4 chip-to-module output common-to-differential-mode output return loss

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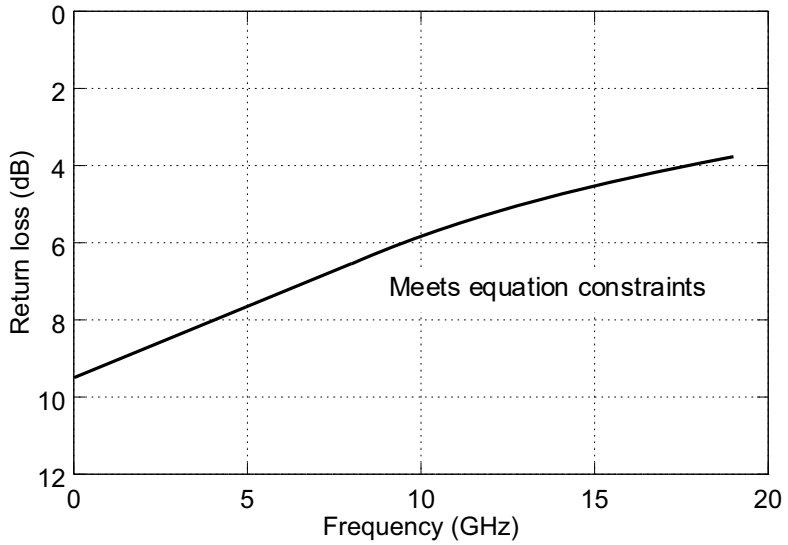

Figure 83E–7—Output differential return loss

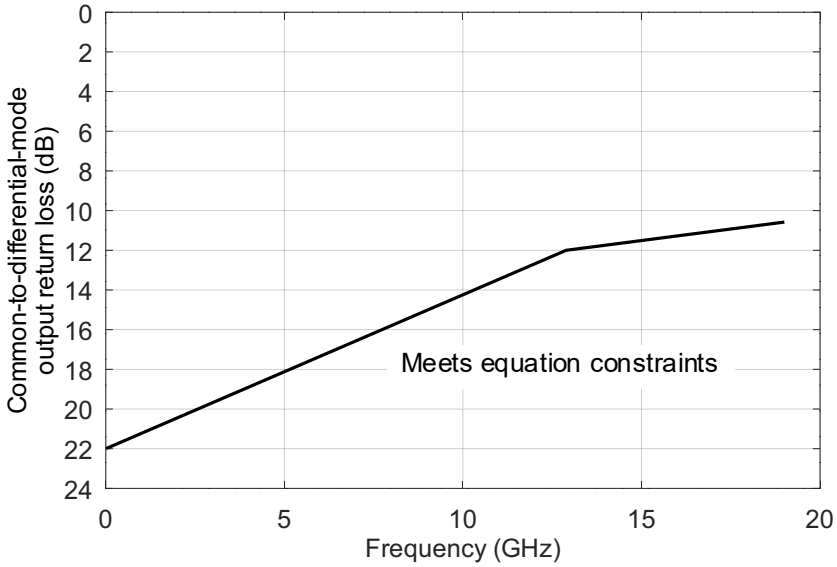

Figure 83E–8—Common-to-differential-mode output return loss

83E.3.1.4 Differential termination mismatch

Differential termination mismatch is defined in 86A.5.3.2.

83E.3.1.5 Transition time

The transition times (rise and fall times) are defined in 86A.5.3.3 with the exception that the observation is through a 33 GHz low-pass filter response.

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83E.3.1.6 Host output eye width and eye height

Figure 83E–9 depicts an example host output eye width and eye height test configuration. Host output eye width and eye height are measured at TP1a using compliance boards defined in 83E.2. The host output eye is measured using a reference receiver with a continuous time linear equalizer (CTLE) defined in 83E.3.1.6.1. The recommended CTLE peaking value is used for host output eye measurements. In addition, it is provided to the module via the variable *Recommended_CTLE_value.* If a Clause 45 MDIO is implemented, this variable is accessible in the module through register 1.179 (see 45.2.1.111). Eye width and eye height measurement methodology is described in 83E.4.2. All counter-propagating signals shall be asynchronous to the co-propagating signals using Pattern 5 (with or without FEC encoding), Pattern 3, or a valid 100GBASE-R signal. Patterns 3 and 5 are described in Table 86–11. For the case where Pattern 3 is used with a common clock, there is at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. The crosstalk generator is calibrated at TP4 with target differential peak-to-peak amplitude of 900 mV and target transition time of 12 ps.

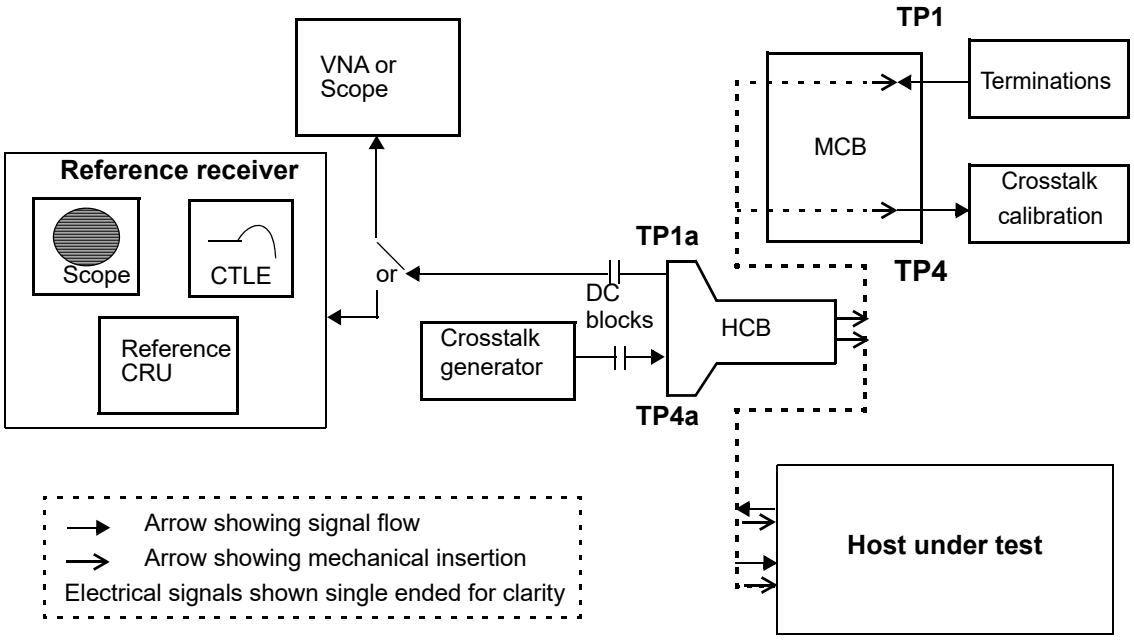

Figure 83E–9—Example host output test configuration

83E.3.1.6.1 Reference receiver for host output eye width and eye height evaluation

The reference receiver is used to measure host eye width and eye height. The reference receiver includes a selectable continuous time linear equalizer (CTLE), which is described by Equation (83E–4) with coefficients given in Table 83E–2 and illustrated in Figure 83E–10. The equalizer may be implemented in software; however, the measured signal is not averaged.

$$H(f) = \frac{GP_1P_2}{Z_1} \times \frac{\mathrm{j}2\pi f + Z_1}{(\mathrm{j}2\pi f + P_1)(\mathrm{j}2\pi f + P_2)} \tag{83E–4}$$

where

$H(f)$ is the CTLE transfer function
G is the CTLE gain

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P_1, P_2	are the CTLE poles in Grad/s
Z_1	is the CTLE zero in Grad/s
j	is the square root of –1
f	is the frequency in GHz

Table 83E–2—Reference CTLE coefficients

Peaking (dB)	G	$\frac{P_1}{2\pi}$	$\frac{P_2}{2\pi}$	$\frac{Z_1}{2\pi}$
1	0.89125	18.6	14.1	8.364
2	0.79433	18.6	14.1	7.099
3	0.70795	15.6	14.1	5.676
4	0.63096	15.6	14.1	4.9601
5	0.56234	15.6	14.1	4.358
6	0.50119	15.6	14.1	3.844
7	0.44668	15.6	14.1	3.399
8	0.39811	15.6	14.1	3.012
9	0.35481	15.6	14.1	2.672

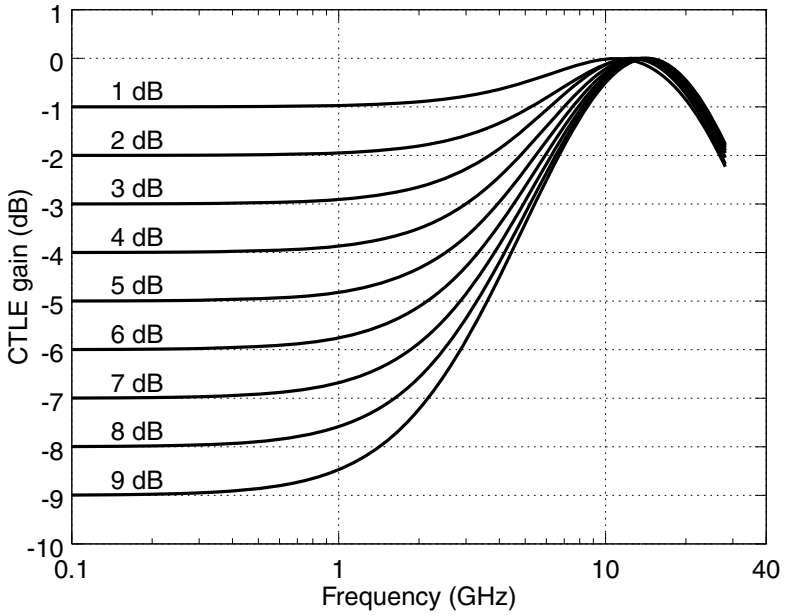

Figure 83E–10—Selectable continuous time linear equalizer (CTLE) characteristic

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83E.3.2 CAUI-4 module output characteristics

A CAUI-4 module output shall meet the specifications defined in Table 83E–3 if measured at TP4. A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

Table 83E–3—CAUI-4 module output characteristics at TP4

Parameter	Reference	Value	Units
Signaling rate per lane (range)	83E.3.1.1	25.78125 ± 100 ppm	GBd
AC common-mode output voltage (max, RMS)	83E.3.1.2	17.5	mV
Differential output voltage (max)	83E.3.1.2	900	mV
Eye width (min)	83E.3.2.1	0.57	UI
Eye height, differential (min)	83E.3.2.1	228	mV
Vertical eye closure (max)	83E.4.2.1	5.5	dB
Differential output return loss (min)	83E.3.1.3	Equation (83E–2)	dB
Common-to-differential-mode output return loss (min)	83E.3.1.3	Equation (83E–3)	dB
Differential termination mismatch (max)	83E.3.1.4	10	%
Transition time (min, 20% to 80%)	83E.3.1.5	12	ps
DC common-mode voltage tolerance (min)[a]	83E.3.1.2	–350	mV
DC common-mode voltage tolerance (max)[a]	83E.3.1.2	2850	mV

[a]DC common-mode voltage is generated by the host. A compliant module meets the output specifications with any DC common-mode voltage within the specified range applied at TP4. The specification includes effects of ground offset voltage.

83E.3.2.1 Module output eye width and eye height

Module output eye width is greater than 0.57 UI. Module output eye height is greater than 228 mV. Figure 83E–11 depicts an example module output eye width and eye height test configuration. Module output eye width and eye height are measured at TP4 using compliance boards defined in 83E.2. The module output eye is measured using a reference receiver with a continuous time linear equalizer (CTLE) defined in 83E.3.2.1.1. Eye width and eye height measurement methodology is described in 83E.4.2. All counter-propagating signals shall be asynchronous to the co-propagating signals using Pattern 5 (with or without FEC encoding), Pattern 3, or a valid 100GBASE-R signal. Patterns 3 and 5 are described in Table 86–11. For the case where Pattern 3 is used with a common clock, there is at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. The crosstalk generator is calibrated at TP1a with target differential peak-to-peak amplitude of 900 mV and target transition time of 19 ps.

83E.3.2.1.1 Reference receiver for module output eye width and eye height evaluation

A reference receiver is used to measure module eye width and eye height. The reference receiver includes a selectable continuous time linear equalizer (CTLE), which is described by Equation (83E–4) with coefficients given in the first two rows of Table 83E–2. The equalizer may be implemented in software; however, the measured signal is not averaged. Either of the two equalizer settings may be used to meet the output eye width and eye height requirement.

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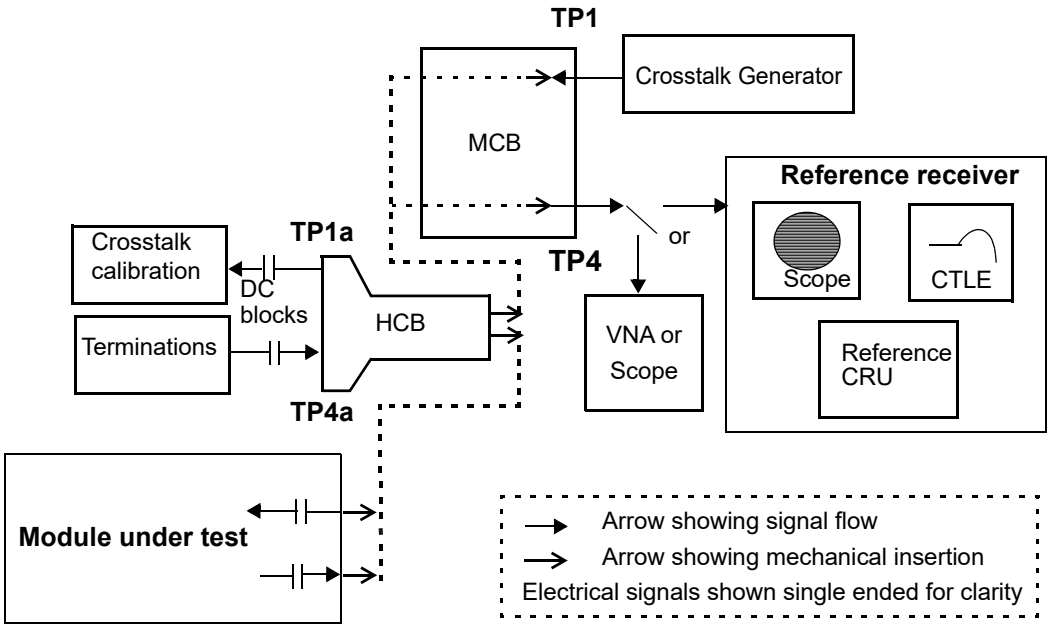

Figure 83E–11—Example module output test configuration

83E.3.3 CAUI-4 host input characteristics

A CAUI-4 host input shall meet the specifications defined in Table 83E–4 if measured at the appropriate test point.

Table 83E–4—CAUI-4 host input characteristics

Parameter	Reference	Test point	Value	Units
Signaling rate, per lane (range)	83E.3.1.1	TP4a	25.78125 ± 100 ppm	GBd
Differential pk-pk input voltage tolerance (min)	83E.3.1.2	TP4	900	mV
Differential input return loss (min)	83E.3.3.1	TP4a	Equation (83E–5)	dB
Differential-to-common-mode input return loss (min)	83E.3.3.1	TP4a	Equation (83E–6)	dB
Host stressed input test[a]	83E.3.3.2	TP4	See 83E.3.3.2	
Differential termination mismatch (max)	83E.3.1.4	TP4a	10	%
Common-mode voltage[b] Min Max	83E.3.1.2	TP4a	 –0.3 2.8	V

[a]Meets BER specified in 83E.1.1.
[b]Generated by host, referred to host ground.

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83E.3.3.1 Input return loss

The differential input return loss, in dB, of the input is shown in Equation (83E–5) and illustrated in Figure 83E–12. The reference impedance for differential return loss measurements is 100 Ω.

$$RLd(f) \geq \left\{ \begin{array}{ll} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{array} \right\} \text{ (dB)} \qquad \text{(83E–5)}$$

where

f	is the frequency in GHz
RLd	is the CAUI-4 chip-to-module input differential return loss

Differential-to-common-mode input return loss, in dB, of the input is shown in Equation (83E–6) and illustrated in Figure 83E–13.

$$RLcd(f) \geq \left\{ \begin{array}{ll} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{array} \right\} \text{ (dB)} \qquad \text{(83E–6)}$$

where

f	is the frequency in GHz
$RLcd$	is the CAUI-4 chip-to-module input differential-to-common-mode input return loss

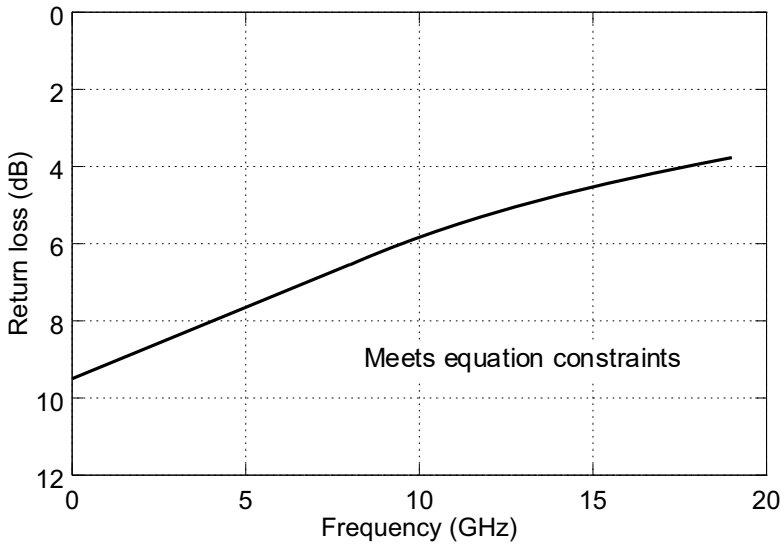

Figure 83E–12—Differential input return loss

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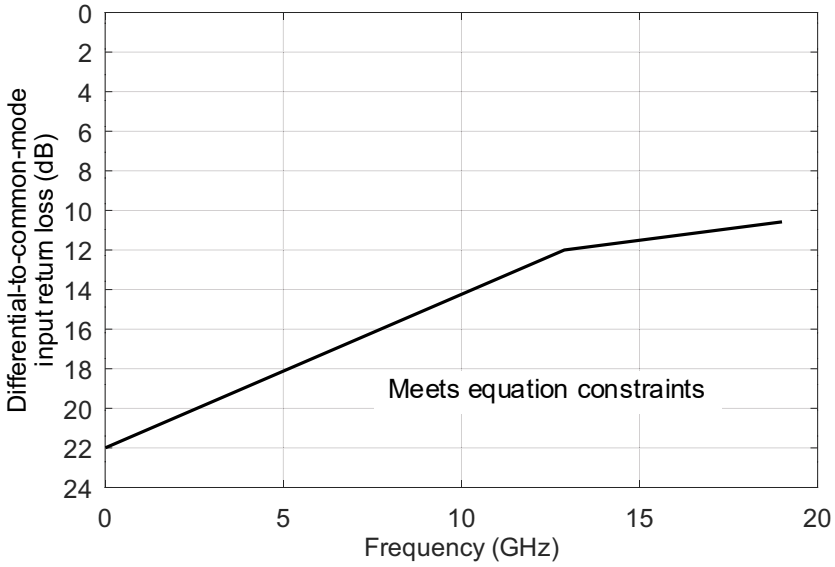

Figure 83E–13—Differential-to-common-mode input return loss

83E.3.3.2 Host stressed input test

The host stressed input tolerance is measured using the procedure defined in 83E.3.3.2.1. The input shall satisfy the input tolerance defined in Table 83E–5.

Table 83E–5—Host stressed input parameters

Parameter	Value
Eye width	0.57 UI
Applied pk-pk sinusoidal jitter	Table 88–13
Eye height	228 mV

83E.3.3.2.1 Host stressed input test procedure

The host stressed input test is summarized in Figure 83E–14. The stressed signal is applied at TP4a and is calibrated at TP4. A reference CRU with a corner frequency of 10 MHz and slope of 20 dB/decade is used to calibrate the stressed signal using Pattern 4 (PRBS9, see Table 86–11 and Table 68–6). The reference receiver includes a selectable CTLE given by Equation (83E–4) and the first two rows of Table 83E–2. The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean signal. The amount of applied peak-to-peak sinusoidal jitter used for the host stressed input test is given in Table 83E–5. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the pattern. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9. The PRBS signaling rate should be approximately 1/10 of the stressed signal's signaling rate (i.e., approximately

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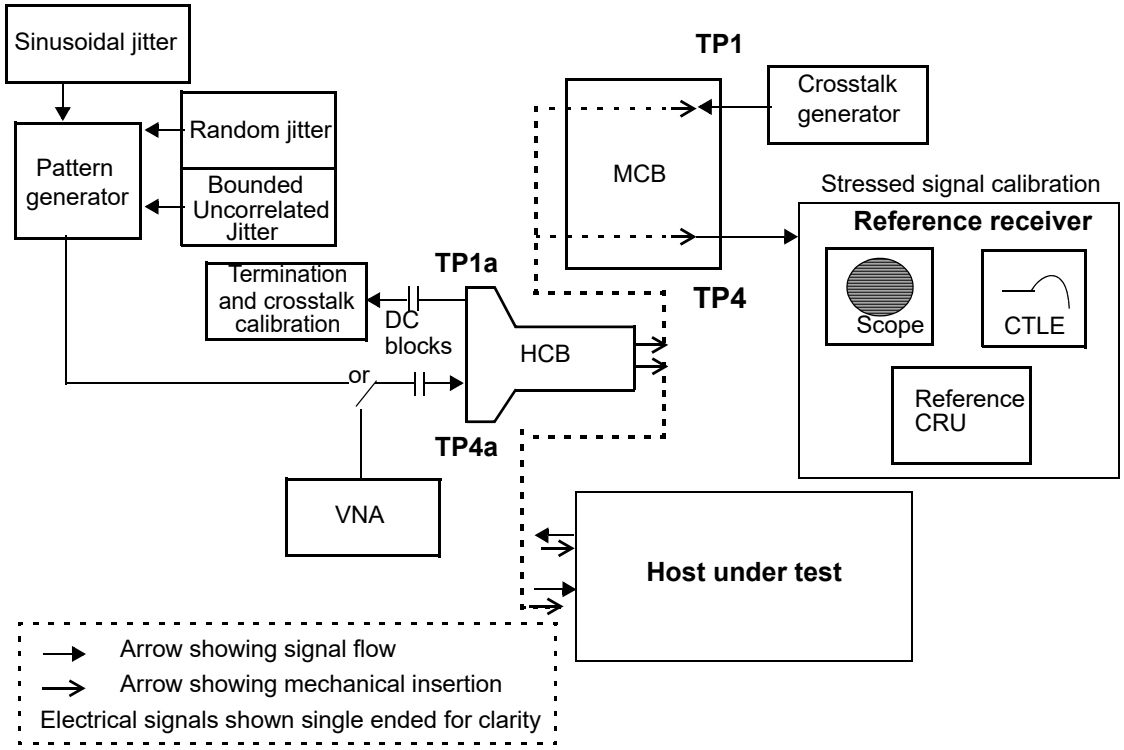

Figure 83E–14—Example host stressed input test

2.578 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value also has to be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates a jitter profile given in Table 83E–6.

Table 83E–6—Pattern generator jitter characteristics

Parameter	Value
Total Jitter (pk-pk)[a]	0.28 UI
Random Jitter (pk-pk)[b]	0.15 UI
Max even-odd jitter (pk-pk)[c]	0.035 UI

[a]Total Jitter at BER of 10^{-15}
[b]Random Jitter at BER of 10^{-15}
[c]As defined in 92.8.3.8.1

The counter propagating crosstalk signals during calibration of the stressed signal are asynchronous with target amplitude of 900 mV peak-to-peak differential and 20% to 80% target transition time of 19 ps as measured at TP1a. The crosstalk signal transition time is calibrated with Pattern 4. The pattern is changed to Pattern 5 (with or without FEC encoding), Pattern 3, or a valid 100GBASE-R signal for amplitude calibration and the stressed input test. Patterns 3, 4, and 5 are described in Table 86–11. For the case where Pattern 3 is used with a common clock, there is at least 31 UI delay between the PRBS31 patterns on one

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lane and any other lane. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes active during the stressed input test.

Eye height and eye width, extrapolated to a probability of 10^{-15}, are then measured at TP4 based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude are adjusted (without exceeding the differential pk-pk input voltage tolerance specification as shown in Table 83E–4) to result in the eye height and eye width given in Table 83E–5 using the reference receiver with the setting of the CTLE that maximizes the product of eye height and eye width.

A host input stressed signal should have a vertical eye closure in the range of 4.5 dB to 5.5 dB with a target value of 5 dB.

The pattern is then changed to Pattern 5 (with or without FEC encoding), Pattern 3, or a valid 100GBASE-R signal for the input test, which is conducted by inserting the HCB into the host under test.

83E.3.4 CAUI-4 module input characteristics

A CAUI-4 module input shall meet the specifications defined in Table 83E–7 if measured at the appropriate test point.

Table 83E–7—CAUI-4 module input characteristics

Parameter	Reference	Test point	Value	Units
Signaling rate per lane (range)	83E.3.1.1	TP1	25.78125 ± 100 ppm	GBd
Differential pk-pk input voltage tolerance (min)	83E.3.1.2	TP1a	900	mV
Differential input return loss (min)	83E.3.3.1	TP1	Equation (83E–5)	dB
Differential-to-common-mode input return loss (min)	83E.3.3.1	TP1	Equation (83E–6)	dB
Differential termination mismatch (max)	83E.3.1.4	TP1	10	%
Module stressed input test[a]	83E.3.4.1	TP1a	See 83E.3.4.1	
Single-ended voltage tolerance range (min)	83E.3.1.2	TP1a	–0.4 to 3.3	V
DC common-mode voltage tolerance (min)[b]	83E.3.1.2	TP1	–350	mV
DC common-mode voltage tolerance (max)[b]	83E.3.1.2	TP1	2850	mV

[a]Meets BER specified in 83E.1.1.
[b]DC common-mode voltage is generated by the host. A compliant module meets the input specifications with any DC common-mode voltage within the specified range applied at TP1. The specification includes effects of ground offset voltage.

83E.3.4.1 Module stressed input test

The module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1. The input shall satisfy the input tolerance defined in Table 83E–8.

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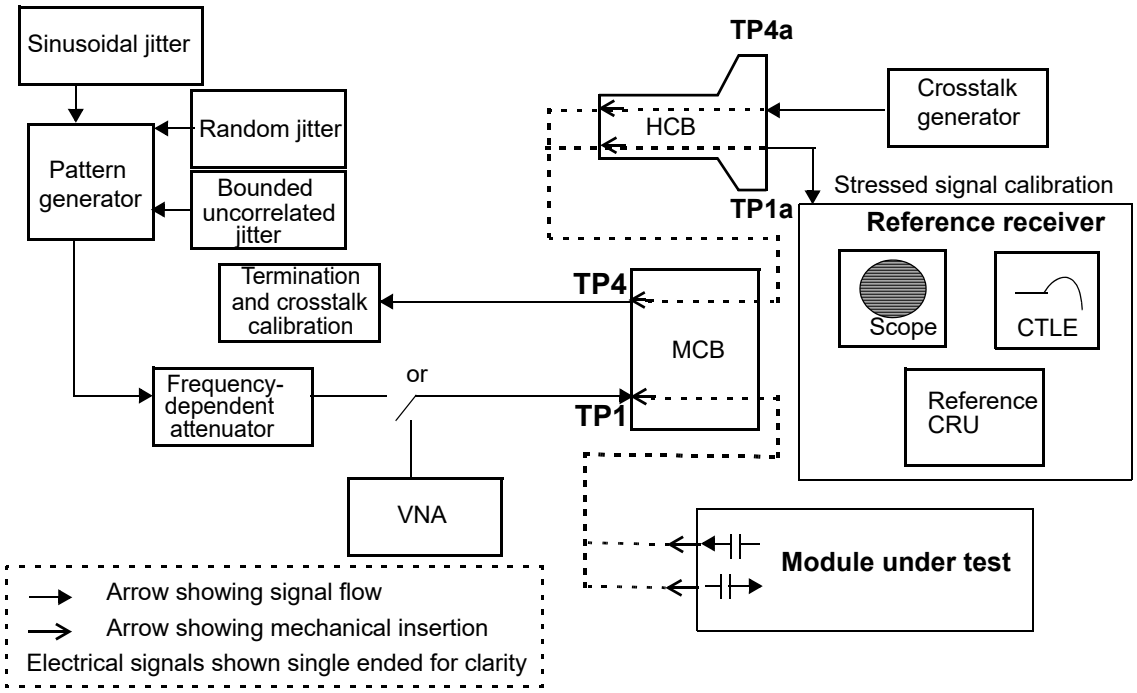

Figure 83E–15—Example module stressed input test

Table 83E–8—Module stressed input parameters

Parameter	Value
Eye width	0.46 UI
Applied pk-pk sinusoidal jitter	Table 88–13
Eye height	95 mV

83E.3.4.1.1 Module stressed input test procedure

The module stressed input test is summarized in Figure 83E–15. The stressed signal is applied at TP1 and is calibrated at TP1a. A reference CRU with a corner frequency of 10 MHz and slope of 20 dB/decade is used to calibrate the stressed signal using Pattern 4. The reference receiver includes a selectable CTLE given by Equation (83E–4) and Table 83E–2. The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean signal, followed by frequency-dependent attenuation. The frequency-dependent attenuator represents the host channel and may be implemented with PCB traces. The amount of applied peak-to-peak sinusoidal jitter used for the module stressed input test is given in Table 83E–8. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the pattern. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9. The PRBS signaling rate should be approximately 1/10 of the stressed signal's signaling rate (i.e., approximately 2.578 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz

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and 300 MHz. This value also has to be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates a jitter profile given in Table 83E–9. The target pattern generator 20% to 80% transition time in the module stressed input test is 9.5 ps. The return loss of the test system as measured at TP1 meets the specification given in Equation (83E–2).

Table 83E–9—Pattern generator jitter characteristics

Parameter	Value
Total Jitter (pk-pk)[a]	0.28 UI
Random Jitter (pk-pk)[b]	0.15 UI
Max even-odd jitter (pk-pk)[c]	0.035 UI

[a]Total Jitter at BER of 10^{-15}.
[b]Random Jitter at BER of 10^{-15}.
[c]As defined in 92.8.3.8.1.

The counter propagating crosstalk signals during calibration of the stressed signal are asynchronous with target amplitude of 900 mV peak-to-peak differential and 20% to 80% target transition time of 12 ps as measured at TP4. The crosstalk signal transition time is calibrated with Pattern 4. The pattern is changed to Pattern 5 (with or without FEC encoding), Pattern 3, or a valid 100GBASE-R signal for amplitude calibration and the stressed input test. Patterns 3, 4, and 5 are described in Table 86–11. For the case where Pattern 3 is used with a common clock, there is at least 31 UI delay between the PRBS31 patterns on one lane and any other lane. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes being active during the stressed input test.

Two levels of frequency-dependent attenuation are used for the module stressed input test: high loss and low loss. For the high loss case, frequency-dependent attenuation is added such that the loss at 12.89 GHz from the output of the pattern generator to TP1a is 13.8 dB. The 13.8 dB loss represents 10.25 dB channel loss with an additional allowance for host transmitter package loss. Eye height and eye width, extrapolated to a probability of 10^{-15}, are then measured at TP1a based on the eye measurement methodology given in 83E.4.2. Random jitter and the pattern generator output amplitude are adjusted (without exceeding the differential pk-pk input voltage tolerance specification as shown in Table 83E–7) to result in the eye height and eye width given in Table 83E–8 using the reference receiver with the setting of the CTLE that maximizes the product of eye height and eye width. For the low loss case, discrete frequency-dependent attenuation is removed such that the connection from the output of the pattern generator to TP1a comprises the mated HCB/MCB pair as described in 83E.4.1. Eye height and eye width at TP1a are then adjusted in the same way as described for the high loss case. In both the low loss and high loss cases, the module under test is provided with the reference CTLE setting used to meet eye width and eye height requirements via the variable *Recommended_CTLE_value*. If a Clause 45 MDIO is implemented, this variable is accessible through register 1.179 (see 45.2.1.111). The pattern is then changed to Pattern 5 (with or without FEC encoding), Pattern 3, or a valid 100GBASE-R signal for the input test, which is conducted by inserting the module into the MCB. The module CAUI-4 receiver under test shall meet the BER requirement as described in 83E.1.1 using three *Recommended_CTLE_value* values for both the high loss test and low loss test:

a) The CTLE setting used to meet eye width and eye height requirements
b) The value 1 dB higher if present in Table 83E–2
c) The value 1 dB lower if present in Table 83E–2

Modules may optionally elect not to use the *Recommended_CTLE_value.*

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83E.4 CAUI-4 measurement methodology

This subclause describes common measurement tools and methodologies to be used for the CAUI-4 chip-to-module interface. Details of HCB and MCB characteristics are given in 83E.4.1 and details of the eye diagram measurement methodology are given in 83E.4.2.

83E.4.1 HCB/MCB characteristics

HCB characteristics are described in 92.11.1 where the HCB performs the equivalent function as the TP2 or TP3 test fixture. The MCB characteristics are described in 92.11.2 where the MCB performs the equivalent functionality as the cable assembly test fixture.

83E.4.2 Eye width and eye height measurement method

Eye diagrams in CAUI-4 chip-to-module are measured using a reference receiver. The reference receiver includes a fourth-order Bessel-Thomson low-pass filter response with 33 GHz 3 dB bandwidth, and a selectable continuous time linear equalizer (CTLE) to measure eye height and width. The pattern used for output eye diagram measurements is Pattern 4. The following procedure should be used to obtain eye height and eye width parameters:

1) Capture Pattern 4 using a clock recovery unit with a corner frequency of 10 MHz and slope of 20 dB/decade and a minimum sampling rate of 3 samples per bit. Collect sufficient samples equivalent to at least 4 million bits to allow for construction of a normalized cumulative distribution function (CDF) to a probability of 10^{-6} without extrapolation.
2) Apply the reference receiver including the appropriate CTLE to the captured signal. For modules, any single CTLE setting as described in 83E.3.2.1.1 that meets both eye width and eye height requirements is acceptable. For host compliance, the CTLE peaking in the reference receiver shall be set to three values:
   a) The recommended CTLE peaking value provided by the host
   b) The value 1 dB higher if present in Table 83E–2
   c) The value 1 dB lower if present in Table 83E–2

   A compliant host passes both the eye width and eye height A limit specified in Table 83E–1 using at least one of the settings and passes eye height B in Table 83E–1 at all of the two or three settings.
3) Use the differential equalized signal from step 2) to construct the CDF of the jitter zero crossing for both the left edge (CDFL) and right edge (CDFR), as a distance from the center of the eye. Calculate the eye width (EW6) as the difference in time between CDFR and CDFL with a value of 10^{-6}. CDFL and CDFR are calculated as the cumulative sum of histograms of the zero crossing samples at the left and right edges of the eye normalized by the total number of sampled bits. For a pattern with 50% transition density the maximum value for the CDFL and CDFR would be 0.5. The CDFL and CDFR are equivalent to bath tub curves where the BER is plotted versus sampling time.
4) Leveraging the Dual-Dirac jitter model described in 48B.1.1, estimate the random jitter. Calculate the best linear fit in Q-scale over the range of probabilities of 10^{-4} to 10^{-6} of the CDFL and CDFR to yield the random jitter on the left edge (RJL) and the random jitter on the right edge (RJR), respectively. The eye width is then given by Equation (83E–7).

$$EW15 = EW6 - 3.19 \times (RJR + RJL) \quad \text{(83E–7)}$$

where

$EW15$	is the eye width extrapolated to 10^{-15} probability
$EW6$	is the eye width at 10^{-6} probability
RJL	is the RMS value of the jitter estimated from CDFL
RJR	is the RMS value of the jitter estimated from the CDFR

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5) Use the differential equalized signal from step 2) to construct the CDF of the signal voltage in the central 5% of the eye, for both logic 1 (CDF1) and logic 0 (CDF0), as a distance from the center of the eye. Calculate the eye height (EH6) as the difference in voltage between CDF1 and CDF0 with a value of 10^{-6}. CDF0 and CDF1 are calculated as the cumulative sum of histograms of the voltage at the top and bottom of the eye normalized by the total number of sampled bits. For a well-balanced number of ones and zeros, the maximum value for CDF0 and CDF1 will be 0.5.

6) Apply the Dual-Dirac and tail fitting techniques to CDF1 and CDF0 to estimate the noise at the middle of the eye. Calculate the best linear fit in Q-scale over the range of probabilities of 10^{-4} and 10^{-6} of CDF1 and CDF0 to yield relative noise one (RN1) and relative noise zero (RN0). The eye height is then given by Equation (83E–8)

$$EH15 = EH6 - 3.19 \times (RN0 + RN1) \quad \text{(83E–8)}$$

where

$EH15$	is the eye height extrapolated to 10^{-15} probability
$EH6$	is the eye height at 10^{-6} probability
$RN1$	is the RMS value of the noise estimated from CDF1
$RN0$	is the RMS value of the noise estimated from CDF0

83E.4.2.1 Vertical eye closure

Vertical eye closure is calculated using Equation (83E–9).

$$VEC = 20\log\left(\frac{AV}{EH15}\right) \quad \text{(83E–9)}$$

where

VEC	is vertical eye closure in dB
AV	is the eye amplitude of the equalized waveform. Eye amplitude is defined as the mean value of logic one minus the mean value of logic zero in the central 5% of the eye
$EH15$	is given in Equation (83E–8)

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83E.5 Protocol implementation conformance statement (PICS) proforma for Annex 83E, Chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)[297]

83E.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 83E, Chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

83E.5.2 Identification

83E.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

83E.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 83E, Chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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83E.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	83E.1	Four independent data paths in each direction	M	Yes [ ]
BER	Meets CAUI-4 BER requirement	83E.1.1	See 83E.1.1	M	Yes [ ]
ADR	Adaptive receiver	83E.3.4.1.1	Module CAUI-4 receiver does not use *Recommended_CTLE_value*	O	Yes [ ] No [ ]

83E.5.4 PICS proforma tables for chip-to-module 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)

83E.5.4.1 Host output

Item	Feature	Subclause	Value/Comment	Status	Support
TH1	Signaling rate	83E.3.1.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TH2	Peak-to-peak differential output voltage	83E.3.1.2	900 mV (max)	M	Yes [ ]
TH3	Peak-to-peak differential output voltage, transmitter disabled	83E.3.1.2	Less than or equal to 35 mV	M	Yes [ ]
TH4	DC common-mode output voltage	83E.3.1	Between –0.3 V and 2.8 V with respect to signal ground	M	Yes [ ]
TH5	AC common-mode output voltage	83E.3.1	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TH6	Differential output return loss	83E.3.1.3	Meets Equation (83E–2) constraints	M	Yes [ ]
TH7	Reference impedance for output return loss	83E.3.1.3	100 Ω.	M	Yes [ ]
TH8	Common to differential mode conversion	83E.3.1.3	Meets Equation (83E–3) constraints	M	Yes [ ]
TH9	Differential termination mismatch	83E.3.1	Less than 10%	M	Yes [ ]
TH10	Transition time	83E.3.1.5	Greater than or equal to 10 ps	M	Yes [ ]
TH11	Eye width	83E.3.1	0.46 UI	M	Yes [ ]
TH12	Eye height A	83E.3.1	95 mV	M	Yes [ ]
TH13	Eye height B	83E.3.1	80 mV	M	Yes [ ]
TH14	Crosstalk source	83E.3.1.6	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 100GBASE-R signal	M	Yes [ ]

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83E.5.4.2 Module output

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Signal rate	83E.3.1.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TM2	Peak-to-peak differential output voltage	83E.3.1.2	900 mV (max)	M	Yes [ ]
TM3	AC common-mode output voltage	83E.3.1.2	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TM4	Differential output return loss	83E.3.1.3	Meets Equation (83E–2) constraints	M	Yes [ ]
TM5	Reference impedance for output return loss	83E.3.1.3	100 Ω.	M	Yes [ ]
TM6	Common to differential mode conversion	83E.3.1.3	Meets Equation (83E–3) constraints	M	Yes [ ]
TM7	Differential termination mismatch	83E.3.1.4	Less than 10%	M	Yes [ ]
TM8	Transition time	83E.3.1.5	Greater than or equal to 12 ps	M	Yes [ ]
TM9	Eye width	83E.3.2.1	0.57 UI	M	Yes [ ]
TM10	Eye height	83E.3.2.1	228 mV	M	Yes [ ]
TM11	Crosstalk source	83E.3.2.1	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 100GBASE-R signal	M	Yes [ ]
TM12	Vertical eye closure	83E.4.2.1	5.5 dB (max)	M	Yes [ ]

83E.5.4.3 Host input

Item	Feature	Subclause	Value/Comment	Status	Support
RH1	CAUI-4 host input characteristics	83E.3.3	Table 83E–4	M	Yes [ ]

83E.5.4.4 Module input

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	CAUI-4 module input characteristics	83E.3.4	Table 83E–7	M	Yes [ ]
RM2	BER requirement	83E.3.4.1.1	As 83E.1.1 with settings associated with *Recommended_CTLE_value*	M	Yes [ ]

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Annex 85A

(informative)

40GBASE-CR4 and 100GBASE-CR10 TP0 and TP5 test point parameters

85A.1 Overview

Annex 85A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system. TP0 and TP5 test points are illustrated in the 40GBASE-CR4 and 100GBASE-CR10 link block diagram of Figure 85–2.

85A.2 Transmitter characteristics at TP0

The specifications at TP0 are summarized in Table 85A–1.

Table 85A–1—Transmitter characteristics at TP0 summary

Parameter	Subclause reference	Value	Units
Signaling rate, per lane	85.8.3.9	10.3125 ± 100 ppm	GBd
Unit interval nominal	85.8.3.9	96.969697	ps
Differential peak-to-peak output voltage (max) with Tx disabled		30	mV
Common-mode voltage limits	72.7.1.4	0 to 1.9	V
Differential output return loss (min)	72.7.1.5	See Equation (72–4) and Equation (72–5)	dB
Common-mode output return loss (min)	72.7.1.6	See Equation (72–6)and Equation (72–7)	dB
AC common-mode output voltage (max, RMS)		30	mV
Transition time (20%–80%)	72.7.1.7	24 to 47	ps
Max output jitter (peak-to-peak)[a] Random jitter[b] Deterministic jitter Duty Cycle Distortion[c] Total jitter	72.7.1.9	 0.15 0.15 0.035 0.28	 UI UI UI UI

[a]Jitter is measured with emphasis off.
[b]Jitter is specified at BER 10^{-12}.
[c]Duty Cycle Distortion is considered part of the deterministic jitter distribution.

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85A.3 Receiver characteristics at TP5

The receiver characteristics at TP5 are summarized in Table 85A–2.

Table 85A–2—Receiver characteristics at TP5 summary

Parameter	Subclause reference	Value	Units
Bit error ratio	85.8.4.3	10^{-12}	
Signaling rate, per lane	85.8.4.4	10.3125 ± 100 ppm	GBd
Unit interval (UI) nominal	85.8.4.4	96.969697	ps
Receiver coupling	85.8.4.5	AC	
Differential input peak-to-peak amplitude (max)	72.7.2.4	1200[a]	mV
Differential input return loss (min)[b]	72.7.2.5	See Equation (72–4) and Equation (72–5)	dB
Differential to common-mode input return loss	85.8.4	10 min from 10 MHz to 10 GHz	dB

[a]The receiver shall tolerate amplitudes up to 1600 mV without permanent damage.
[b]Relative to 100 Ω differential.

85A.4 Transmitter and receiver differential printed circuit board trace loss

With the insertion loss TP0 to TP2 or TP3 to TP5 given in 85.8.3.4 and an assumed mated connector loss of 1.74 dB, the maximum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards for each differential lane (i.e., the maximum value of the sum of the insertion losses from TP0 to the MDI host receptacle and from TP5 to the MDI host receptacle) are determined using Equation (85A–1). The maximum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards is 7 dB at 5.15625 GHz. The maximum insertion loss for the transmitter or the receiver differential controlled impedance printed circuit board is one half of the maximum insertion loss $IL_{PCBmax}(f)$.

$$IL_{\mathrm{PCB}}(f) \le IL_{\mathrm{PCBmax}}(f) \;=\; (0.3)[20\log_{10}(\mathrm{e})(b_1\sqrt{f} + b_2 f + b_3 f^2 + b_4 f^3)] \;\; (\mathrm{dB}) \qquad (85\text{A}–1)$$

for 10 MHz ≤ f ≤ 7500 MHz.

where

f is the frequency in Hz
$IL_{\mathrm{PCB}}(f)$ is the insertion loss for the transmitter and receiver PCB
$IL_{\mathrm{PCBmax}}(f)$ is the maximum insertion loss for the transmitter and receiver PCB
b_1 2×10^{-5}
b_2 1.1×10^{-10}
b_3 3.2×10^{-20}
b_4 -1.2×10^{-30}
e ≈ 2.71828

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The minimum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards for each differential lane (i.e., the minimum value of the sum of the insertion losses from TP0 to MDI receptacle and TP5 to MDI receptacle) are determined using Equation (85A–2) and the coefficients b_1 through b_4 are given in Equation (85A–1). The minimum insertion loss for the transmitter or the receiver differential controlled impedance printed circuit board is one half of the minimum insertion loss $IL_{\mathrm{PCBmin}}(f)$.

$$IL_{\mathrm{PCB}}(f) \geq IL_{\mathrm{PCBmin}}(f) = (0.0574)[20\log_{10}(\mathrm{e})(b_1\sqrt{f} + b_2 f + b_3 f^2 + b_4 f^3)] \text{ (dB)} \quad (85\text{A–}2)$$

for 10 MHz $\leq f \leq$ 7500 MHz.

where

f is the frequency in Hz
$IL_{\mathrm{PCB}}(f)$ is the insertion loss for the transmitter and receiver PCB
$IL_{\mathrm{PCBmin}}(f)$ is the minimum insertion loss for the transmitter and receiver PCB

85A.5 Channel insertion loss

This subclause provides information on channel insertion losses for intended topologies ranging from 0.5 m to 7 m in length. The maximum channel insertion loss associated with the 7 m topology is determined using Equation (85A–3). The channel insertion loss associated with the 0.5 m topology and a maximum host channel is determined by Equation (85A–4). The channel insertion loss budget at 5.15625 GHz is illustrated in Figure 85A–1.

The maximum channel insertion loss is determined using Equation (85A–3). The maximum channel insertion loss is 24.44 dB at 5.15625 GHz.

$$IL_{\mathrm{Chmax}}(f) = IL_{\mathrm{Camax}}(f) + 2IL_{\mathrm{Host}}(f) - 2IL_{\mathrm{MatedTF}}(f) \text{ (dB)} \quad (85\text{A–}3)$$

for 50 MHz $\leq f \leq$ 7500 MHz.

where

f is the frequency in MHz
$IL_{\mathrm{Ch}max}(f)$ is the maximum channel insertion loss between TP0 and TP5
$IL_{\mathrm{Camax}}(f)$ is the maximum cable assembly insertion loss using Equation (85–19)
$IL_{\mathrm{Host}}(f)$ is the maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (85–14)
$IL_{\mathrm{MatedTF}}(f)$ is the maximum insertion loss of the mated test fixture using Equation (85–36)

The channel insertion loss between TP0 and TP5 representative of a 0.5 m cable assembly and a maximum host channel is determined using Equation (85A–4).

$$(IL_{\mathrm{Ch0.5}m}(f) = 0.275IL_{\mathrm{Camax}}(f) + 2IL_{\mathrm{Host}}(f) - 2IL_{\mathrm{MatedTF}}(f) \text{ (dB)} \quad (85\text{A–}4)$$

for 50 MHz $\leq f \leq$ 7500 MHz.

where

f is the frequency in MHz

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$IL_{\mathrm{Ch0.5}m}(f)$ is the channel insertion loss between TP0 and TP5 representative of a 0.5 m cable assembly and a maximum host channel

$IL_{\mathrm{Camax}}(f)$ is the maximum cable assembly insertion loss from TP1 to TP4 using Equation (85–19)

$IL_{\mathrm{Host}}(f)$ is the maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (85–14)

$IL_{\mathrm{MatedTF}}(f)$ is the maximum insertion loss of the mated test fixture using Equation (85–36)

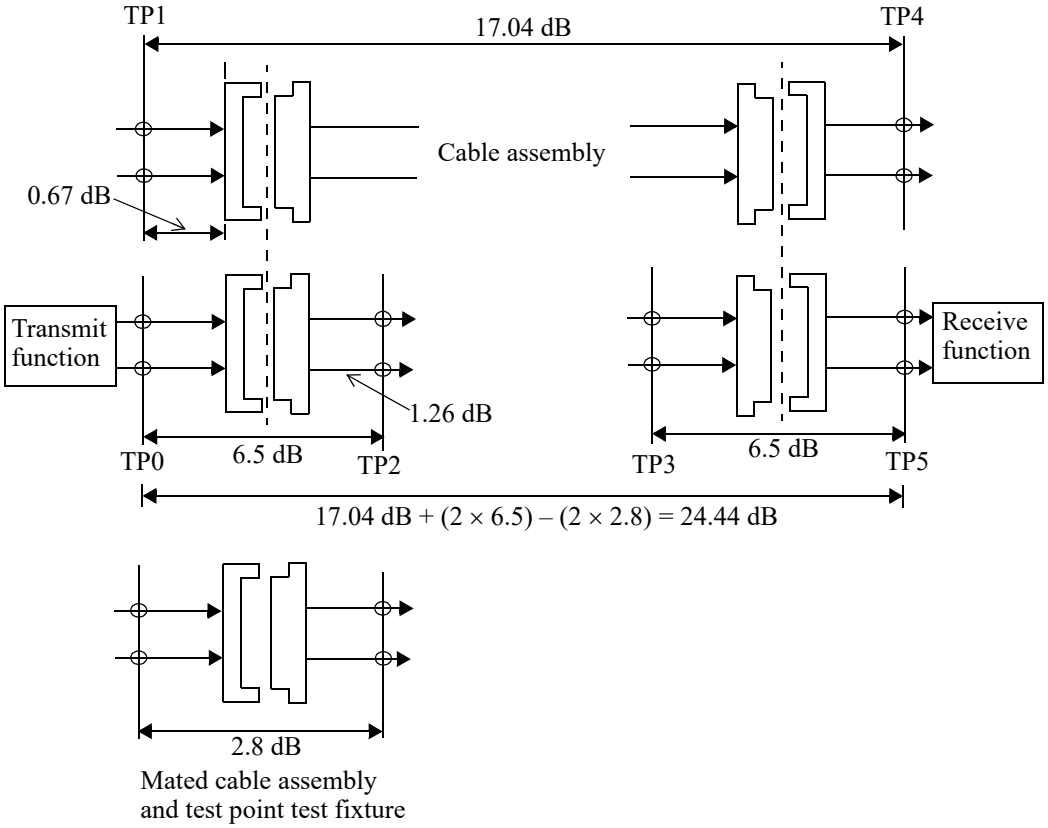

Figure 85A–1—Illustration of channel insertion loss budget at 5.15625 GHz

85A.6 Channel return loss

The return loss of each lane of the 40GBASE-CR4 or 100GBASE-CR10 channel is recommended to meet the values determined using Equation (85–25).

85A.7 Channel insertion loss deviation (ILD)

The channel insertion loss deviation is the difference between the channel insertion loss and the fitted channel insertion loss is determined using Equation (85A–5).

$$ILD(f) = IL_{\mathrm{Ch}}(f) - IL_{\mathrm{fitted}}(f) \text{ (dB)} \quad (85A–5)$$

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where

f is the frequency in MHz

$ILD(f)$ is the channel insertion loss deviation at frequency f

$IL_{\text{fitted}}(f)$ is defined in Equation (85–19)

Given the channel insertion loss is at N uniformly-spaced frequencies f_n spanning the frequency range 50 MHz to 7500 MHz with a maximum frequency spacing of 10 MHz, the coefficients of the fitted channel insertion loss are determined using Equation (85–20) and Equation (85–21).

The channel insertion loss deviation is recommended to be within the region defined by Equation (85–23) and Equation (85–24) for all frequencies from 50 MHz to 7500 MHz.

85A.8 Channel integrated crosstalk noise (ICN)

Since four lanes or ten lanes are used to transfer data between PMDs, the near-end crosstalk (NEXT) that is coupled into a victim receiver will be from the four or ten adjacent transmitters. The channel multiple disturber NEXT loss, $MDNEXT\_loss_1(f)$, is specified using the individual NEXT losses as shown in Equation (85–26).

In addition, the far-end Crosstalk (FEXT) that is coupled into a receiver will be from the three or nine other transmitters adjacent to the victim transmitter. The channel multiple disturber FEXT loss, $MDFEXT\_loss(f)$, is specified using the individual FEXT losses as shown in Equation (85–27).

Given the channel $MDNEXT\_loss(f)$ and $MDFEXT\_loss(f)$ measured over N uniformly-spaced frequencies f_n spanning the frequency range 50 MHz to 10000 MHz with a maximum frequency spacing of 10 MHz, the RMS value of the integrated crosstalk noise is determined using Equation (85–28) through Equation (85–32) and the parameters shown in Table 85–11.

The total integrated crosstalk RMS noise voltage of the channel is recommended to meet the values determined using Equation (85A–6) illustrated in Figure 85A–2.

$$\sigma_{x,\,ch} \leq \left\{ \begin{array}{ll} 10 & 3 \leq IL \leq 7.5 \\ 13.4 - 0.45IL & 7.5 < IL \leq 24.44 \end{array} \right\} \quad \text{(mV)} \qquad \text{(85A–6)}$$

where IL is the value of the channel insertion loss in dB at 5.15625 GHz.

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Figure 85A–2—Channel integrated crosstalk noise

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Annex 86A

(normative)

Parallel Physical Interface (nPPI) for 40GBASE-SR4 and 40GBASE-LR4 (XLPPI) and 100GBASE-SR10 (CPPI)

86A.1 Overview

The Parallel Physical Interface (nPPI) is an optional instantiation of the PMD service interface for the PMDs in Clause 86, which is described in 86.2 and 80.3, or for the 40GBASE-LR4 PMD service interface described in 87.2 and 80.3. It allows the construction of compact optical transceiver modules for 40GBASE-SR4, 40GBASE-LR4, or 100GBASE-SR10 with no clock and data recovery circuits inside. The 40 Gb/s Parallel Physical Interface (XLPPI, four lanes) is used with 40GBASE-SR4 or 40GBASE-LR4, and the 100 Gb/s Parallel Physical Interface (CPPI, ten lanes) with 100GBASE-SR10. The term “nPPI” denotes either or both.

The PMD and PMA attached to the nPPI are required to comply with the delay, Skew, and Skew Variation requirements in 86.3, 83.5.3, and 83.5.4 as appropriate. The PMD MDIO function mapping given in 86.4 may apply. The PMD functional specifications are as given in 86.5.

This annex is arranged as follows: following the overview, a reminder of the block diagram, a brief introduction to the test points, and lane assignments, 86A.4 contains the electrical specifications for nPPI from host to module (Tx side) and then module to host (Rx side). Test points, compliance boards, and electrical parameters are defined in 86A.5. The host PCB (“channel”) response recommendation is provided in 86A.6. Safety, installation, environment, and labeling is addressed in 86A.7 and PICS is provided in 86A.8. This annex is very closely related to Clause 86.

86A.2 Block diagram and test points

The PMD block diagram is shown in Figure 86–2. Figure 86–3 shows the test points.

The nPPI is standardized at the test points described in 86.8.1. The transmit side electrical signal (host electrical output and module electrical input) is defined at the output of the Host Compliance Board (TP1a), and other specifications of the module electrical input port are defined at the input of the Module Compliance Board (TP1). The receive side electrical signal (module electrical output and host electrical input) is defined at the output of the Module Compliance Board (TP4), and other specifications of the host electrical input port are defined at the input of the Host Compliance Board (TP4a). Test points and compliance boards are defined more thoroughly in 86A.5.1.

86A.3 Lane assignments

There are no lane assignments (within a group of transmit or receive lanes) for XLPPI or CPPI. While it is expected that a PMD will map electrical lane *i* to optical lane *i* and vice versa, there is no need to define the physical ordering of the lanes, as the PCS is capable of receiving the lanes in any arrangement.

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86A.4 Electrical specifications for nPPI

The signaling rate for a lane of an XLPPI or CPPI interface shall be as defined in Table 86–2. 86A.4.1 and 86A.4.2 specify the host to module (Tx side) and module to host (Rx side) respectively of the nPPI. Parameters are defined in 86A.5 and 86.8. A recommended PCB ("channel") response for the host (PMA) is provided in 86A.6. Test points are defined in 86A.5.1.

86A.4.1 nPPI host to module electrical specifications

Each output lane and signal of the nPPI host (PMA), if measured at TP1a (see 86A.5.1) with the specified crosstalk signals applied on all input lanes, shall meet the specifications of Table 86A–1 per the definitions in 86A.5. Each lane of the nPPI module (PMD) electrical input, if measured at TP1 and TP1a with all Rx lanes (module output) operating, shall meet the specifications of Table 86A–2 per the definitions in 86A.5. The module electrical input shall be AC-coupled, i.e., it shall present a high DC common-mode impedance at TP1. There may be various methods for AC-coupling in actual implementations.

Table 86A–1—nPPI host electrical output specifications at TP1a

Parameter description	Min	Max	Units	Conditions
Single ended output voltage	–0.3	4	V	Referred to signal common
AC common-mode output voltage	—	15	mV	RMS
Termination mismatch at 1 MHz	—	5	%	
Differential output return loss	See 86A.4.1.1	—	dB	
Output transition time, 20% to 80%	28	—	ps	
J2 Jitter output	—	0.17	UI	
J9 Jitter output	—	0.29	UI	
Data Dependent Pulse Width Shrinkage (DDPWS)	—	0.07	UI	
Q_{sq} for XLPPI	45	—	V/V	
Q_{sq} for CPPI	43	—	V/V	
	Specification values			
Eye mask coordinates: X1, X2 Y1, Y2	0.11, 0.31 95, 350		UI mV	Hit ratio = 5×10^{-5}
Crosstalk source VMA, each input lane	700		mV	At TP4
Crosstalk source transition times, 20% to 80%	34		ps	At TP4

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Table 86A–2—nPPI module electrical input specifications at TP1 and TP1a

Parameter description	Test point	Min	Max	Units	Conditions
Single ended input voltage tolerance[a]	TP1a	–0.3	4	V	Referred to TP1 signal common
AC common-mode input voltage tolerance	TP1a	15	—	mV	RMS
Differential input return loss	TP1	See 86A.4.1.1	—	dB	10 MHz to 11.1 GHz
Differential to common-mode input return loss	TP1	10	—	dB	10 MHz to 11.1 GHz
J2 Jitter tolerance	TP1a	0.17	—	UI	
J9 Jitter tolerance	TP1a	0.29	—	UI	
Data Dependent Pulse Width Shrinkage (DDPWS) tolerance	TP1a	0.07	—	UI	
		Specification values			
Eye mask coordinates: X1, X2 Y1, Y2	TP1a	0.11, 0.31 95, 350		UI mV	Hit ratio = 5×10^{-5}
Crosstalk calibration signal VMA	TP4	850		mV	While calibrating compliance signal[b]
Crosstalk calibration signal transition times, 20% to 80%	TP4	34		ps	

[a] The single ended input voltage tolerance is the allowable range of the instantaneous input signals.
[b] The crosstalk calibration signals are applied to the mated HCB-MCB at TP4a and measured at TP4 following the same principles as the host electrical input calibration (see 86A.5.3.8.5). They are removed before testing.

86A.4.1.1 Differential return losses at TP1 and TP1a

From 10 MHz to 11.1 GHz, the magnitude in decibels of the module differential input return loss at TP1 and the host differential output return loss at TP1a (see 86A.5.1) shall not exceed the limit given in Equation (86A–1) and illustrated in Figure 86A–1.

$$Return\_loss(f) \geq \begin{cases} 12 - 2\sqrt{f} & 0.01 \leq f < 4.11 \\ 6.3 - 13\log_{10}\left(\frac{f}{5.5}\right) & 4.11 \leq f \leq 11.1 \end{cases} \text{ dB} \qquad (86A–1)$$

where
$Return\_loss(f)$ is the return loss at frequency f
f is the frequency in GHz

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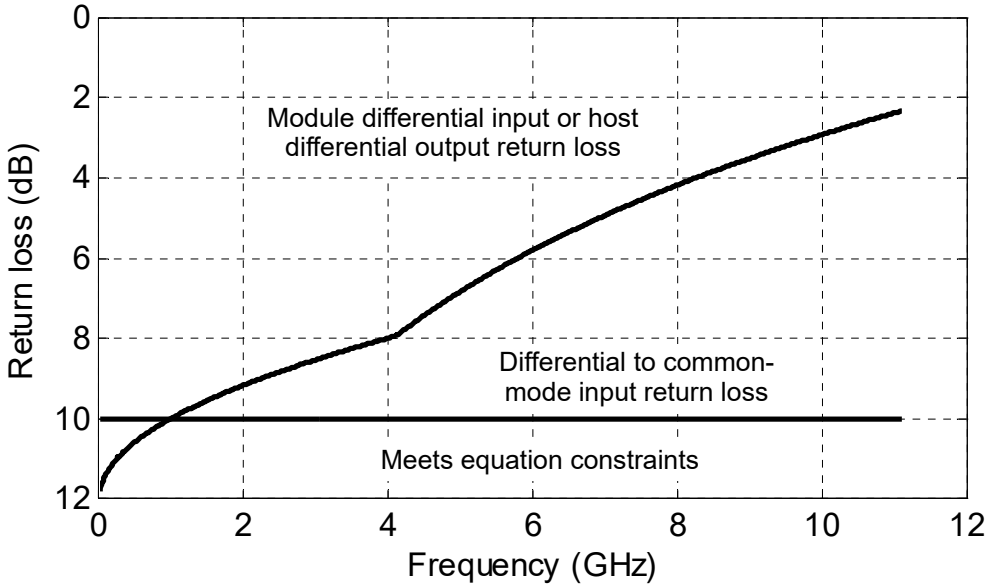

Figure 86A–1—Return loss specifications

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86A.4.2 nPPI module to host electrical specifications

Each electrical output lane and signal of the nPPI module (PMD), if measured at TP4 shall meet the specifications of Table 86A–3 per the definitions in 86A.5 while the specified crosstalk sources are applied to the module's electrical input Each lane of the nPPI host (PMA) input shall meet the specifications of Table 86A–4 at TP4 and/or TP4a per the definitions in 86A.5. The module electrical output shall be AC-coupled, i.e., it shall present a high DC common-mode impedance at TP4. There may be various methods for AC-coupling in actual implementations..

Table 86A–3—nPPI module electrical output specifications at TP4

Parameter description	Min	Max	Units	Conditions
Single ended output voltage tolerance	–0.3	4	V	Referred to signal common
AC common-mode output voltage (RMS)	—	7.5	mV	
Termination mismatch at 1 MHz	—	5	%	
Differential output return loss	See 86A.4.2.1	—	dB	10 MHz to 11.1 GHz
Output transition time, 20% to 80%	28	—	ps	
J2 Jitter output	—	0.42	UI	
J9 Jitter output	—	0.65	UI	
	Specification values			
Eye mask coordinates: X1, X2 Y1, Y2	0.29, 0.5 150, 425		UI mV	Hit ratio = 5×10^{-5}
Crosstalk source VMA, each lane	700		mV	At TP1a
Crosstalk source transition times, 20% to 80%	37		ps	At TP1a

86A.4.2.1 Differential return losses at TP4 and TP4a

From 10 MHz to 11.1 GHz, the magnitude in decibels of the module differential output return loss at TP4 and the host differential input return loss at TP4a shall not exceed the limit given in Equation (86A–2) and illustrated in Figure 86A–1.

$$Return\_loss(f) \geq \begin{cases} 12 - 2\sqrt{f} & 0.01 \leq f < 4.11 \\ 6.3 - 13\log_{10}\left(\frac{f}{5.5}\right) & 4.11 \leq f \leq 11.1 \end{cases} \text{ dB} \qquad (86A–2)$$

where

$Return\_loss(f)$ is the return loss at frequency f
f is the frequency in GHz

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Table 86A–4—nPPI host electrical input specifications at TP4 and TP4a

Parameter description	Test point	Min	Max	Units	Conditions
Single ended input voltage[a]	TP4	–0.3	4	V	Referred to signal common
AC common-mode input voltage tolerance	TP4	7.5	—	mV	RMS
Differential input return loss	TP4a	See 86A.4.2.1	—	dB	
Differential to common-mode input return loss	TP4a	10	—	dB	10 MHz to 11.1 GHz
Host input signal tolerance, interface BER limit		—	10^{-12}	—	
Conditions of host electrical receiver signal tolerance test:[b]					
		Specification values			
Eye mask coordinates: X1, X2 Y1, Y2	TP4	0.29, 0.5 150, 425		UI mV	Hit ratio = 5×10^{-5}
Transition time, 20% to 80%		34		ps	
J2 Jitter	TP4	0.42		UI	
J9 Jitter	TP4	0.65		UI	
Data Dependent Pulse Width Shrinkage (DDPWS)		0.34		UI	
VMA of aggressor lanes	TP4	850		mV	
Crosstalk calibration signal VMA	TP1a	700		mV	
Crosstalk calibration signal transition times, 20% to 80%	TP1a	37		ps	

[a] The host is required to tolerate (work correctly with) input signals with instantaneous voltages anywhere in the specified range.
[b] The specification values are test conditions for measuring signal tolerance and are not characteristics of the host (see 86A.5.3.8).

86A.5 Definitions of electrical parameters and measurement methods

Test points are defined in 86A.5.1, compliance boards in 86A.5.1.1, test patterns in 86A.5.2 and parameters in 86A.5.3 and 86.8. Multi-lane testing considerations are given in 86.8.2.1.

86A.5.1 Test points and compliance boards

Figure 86–3 shows the six test points for 40GBASE-SR4 and 100GBASE-SR10. These are TP1, TP1a, TP2, TP3, TP4, and TP4a; four of these are Skew points SP2, SP3, SP4, and SP5 as shown. For 40GBASE-LR4, points TP1, TP1a, TP4, TP4a, SP2, and SP5 are in equivalent positions. Figure 86–3 also shows the substitution of compliance boards for module (PMD) or host (PMA). These compliance boards are defined to connect generic test equipment to the module and host for test purposes. The module can be plugged into

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the Module Compliance Board (MCB), which has specified electrical parameters. The Host Compliance Board (HCB), which also has specified electrical parameters, can plug into the host. The MCB and the HCB can be plugged together for calibration of compliance signals and to check the electrical parameters of the boards. Table 86A–5 shows the parameters or signals measured at each point. Also, TP0 and TP5 define the host ends of the electrical channel, at the PMA IC.

All electrical measurements and parameters are defined as through HCB and/or MCB as appropriate, with corrections if necessary.

CAUTION

A PMD with an nPPI interface is AC-coupled; however, an HCB is not. The user should take care that the test equipment does not improperly load or damage a host under test.

Table 86A–5—Parameters defined at each test point

Test point	Direction	Parameter
TP1	Looking downstream into module transmitter input	Module transmitter input return loss
TP1a	Looking upstream into host transmitter output	Host transmitter output signal and output return loss, module transmitter compliance signal calibration, host receiver compliance crosstalk signal calibration
TP4	Looking upstream into module receiver output	Module receiver output signal and output return loss, host receiver compliance signal calibration
TP4a	Looking downstream into host receiver input	Host receiver input return loss

86A.5.1.1 Compliance board parameters

The electrical characteristics of the HCB and MCB are given in 86A.5.1.1.1 and 86A.5.1.1.2. If boards are used that do not match the specifications given, the measurement results for nPPI shall be corrected for the differences between the actual HCB or MCB's properties and the reference differential insertion losses given in 86A.5.1.1.1. As it may be impractical to correct eye measurements for a board with differential insertion loss outside the limits given in 86A.5.1.1.2, such boards shall not be used. Boards that do not meet the specifications for mated HCB-MCB in 86A.5.1.1.2 shall not be used.

86A.5.1.1.1 Reference insertion losses of HCB and MCB

The reference differential insertion loss in decibels of the HCB and of the MCB, excluding the module connector, are given in Equation (86A–3) and Equation (86A–4) respectively, and illustrated in Figure 86A–2.

For the HCB,

$$Insertion\_loss(f) = 0.01 + 0.3\sqrt{f} + 0.11f \quad \text{dB} \qquad 0.01 \le f \le 11.1 \qquad \text{(86A–3)}$$

where

$Insertion\_loss(f)$ is the insertion loss at frequency f
f is the frequency in GHz

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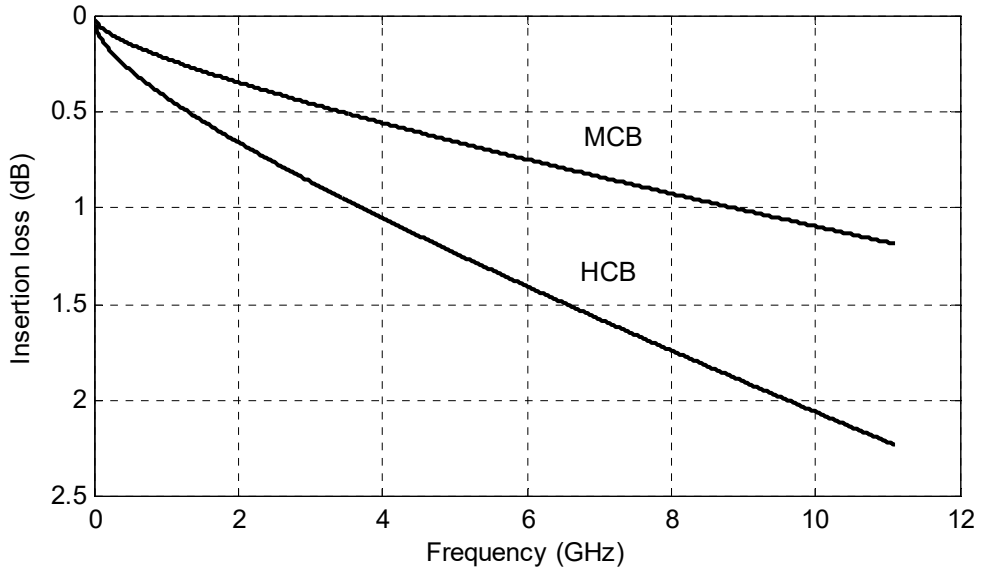

Figure 86A–2—Reference differential insertion losses of HCB, MCB excluding connector

For the MCB,

$$Insertion\_loss(f) = 0.0006 + 0.16\sqrt{f} + 0.0587f \quad \text{dB} \qquad 0.01 \le f \le 11.1 \tag{86A–4}$$

where

Insertion_loss(*f*) is the insertion loss at frequency *f*
f is the frequency in GHz

86A.5.1.1.2 Electrical specifications of mated HCB and MCB

The limits on the differential insertion loss in decibels of the mated HCB and MCB (in either direction) are given in Equation (86A–5) (which defines the minimum insertion loss) and Equation (86A–6) (which defines the maximum insertion loss). These limits are illustrated in Figure 86A–3.

$$Insertion\_loss(f) \ge -0.11 + 0.46\sqrt{f} + 0.16f \quad \text{dB} \qquad 0.01 \le f \le 11.1 \tag{86A–5}$$

$$Insertion\_loss(f) \le \left\{ \begin{array}{ll} 0.029 + 0.861\sqrt{f} + 0.158f & 0.01 \le f < 5.5 \\ 0.2 + 0.65f & 5.5 \le f \le 11.1 \end{array} \right\} \quad \text{dB} \tag{86A–6}$$

where

Insertion_loss(*f*) is the insertion loss at frequency *f*
f is the frequency in GHz

The limit on the differential return loss in decibels of the mated HCB and MCB, looking into the HCB or looking into the MCB, is given in Equation (86A–7), and illustrated in Figure 86A–4.

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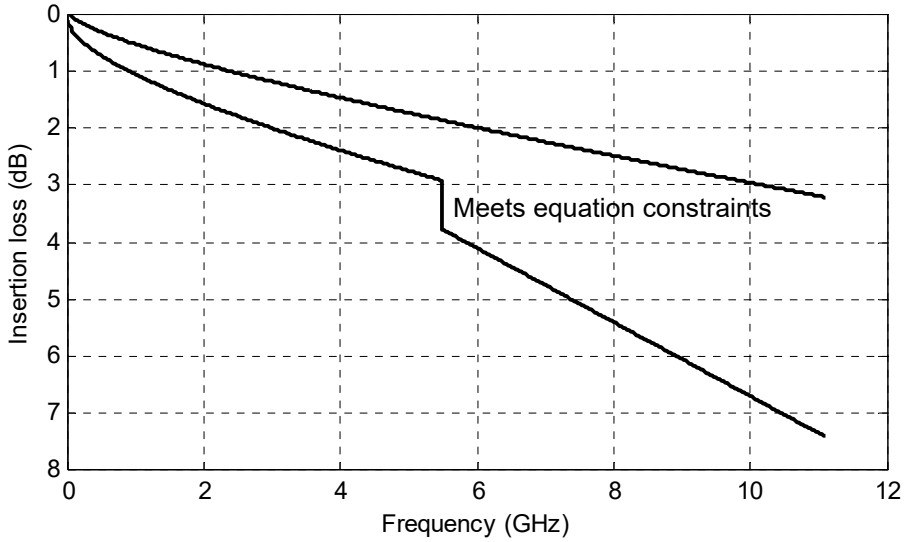

Figure 86A–3—Differential insertion loss limits of mated HCB-MCB

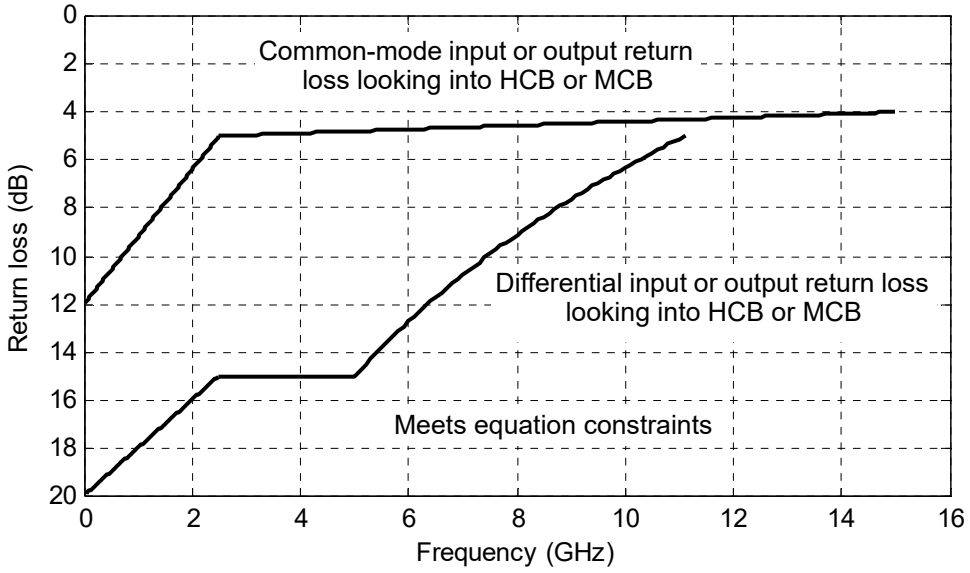

Figure 86A–4—Return loss limits of mated HCB-MCB

$$Return\_loss(f) \geq \begin{cases} 20 - 2f & 0.01 \leq f < 2.5 \\ 15 & 2.5 \leq f < 5 \\ 13.8 - 28.85\log_{10}\left(\frac{f}{5.5}\right) & 5 \leq f \leq 11.1 \end{cases} \text{ dB} \qquad (86A–7)$$

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where

Return_loss(*f*) is the return loss at frequency *f*
f is the frequency in GHz

The limit on the common-mode return loss in decibels of the mated HCB and MCB is given in Equation (86A–8) and illustrated in Figure 86A–4.

$$Return\_loss(f) \geq \left\{ \begin{array}{ll} 12 - 2.8f & 0.01 \leq f < 2.5 \\ 5.2 - 0.08f & 2.5 \leq f \leq 15 \end{array} \right\} \text{ dB} \quad \text{(86A–8)}$$

where

Return_loss(*f*) is the return loss at frequency *f*
f is the frequency in GHz

The limit on the differential to common-mode conversion loss in decibels of the mated HCB and MCB, for input to HCB and output from MCB, or input to MCB and output from HCB, is given in Equation (86A–9) and illustrated in Figure 86A–5.

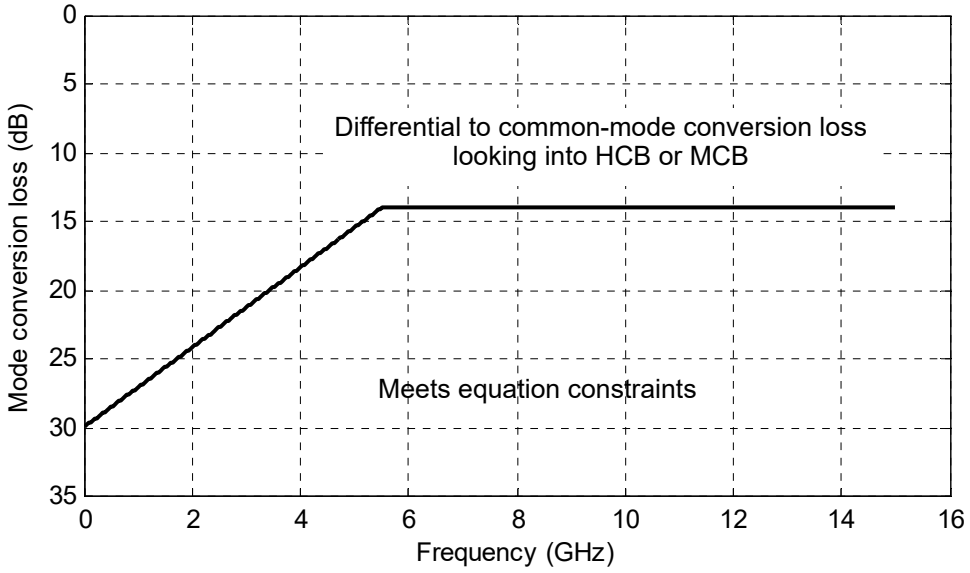

Figure 86A–5—Differential to common-mode conversion loss limit of mated HCB-MCB

$$Mode\_conversion\_loss(f) \geq \left\{ \begin{array}{ll} 30 - 2.91f & 0.01 \leq f < 5.5 \\ 14 & 5.5 \leq f \leq 15 \end{array} \right\} \text{ dB} \quad \text{(86A–9)}$$

where

Mode_conversion_loss(*f*) is the mode conversion loss at frequency *f*
f is the frequency in GHz

The limits on integrated crosstalk noise of the mated HCB and MCB for XLPPI and CPPI are as specified in 85.10.9.4 for 40GBASE-CR4 and 100GBASE-CR10 respectively, with the exception that the frequency range is 0.01 GHz to 12 GHz.

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86A.5.2 Test patterns and related subclauses

While compliance is to be achieved in normal operation, specific test patterns are defined for measurement consistency and to enable measurement of some parameters. Table 86–11 lists the defined test patterns, and Table 86A–6 gives the test patterns to be used in each measurement, unless otherwise specified, and also lists references to the subclauses in which each parameter is defined. Multi-lane testing considerations are

Table 86A–6—Test patterns and related subclauses

Parameter	Pattern	Related subclause
J2 Jitter	3, 5, or valid 40GBASE-SR4 or 100GBASE-SR10 signal	86.8.3.3.1
J9 Jitter	3 or 5	86.8.3.3.2
Data Dependent Pulse Width Shrinkage (DDPWS)	4	86A.5.3.4
AC common-mode voltage	3, 5, or valid 40GBASE-SR4 or 100GBASE-SR10 signal	86A.5.3.1
Transition time	Square wave or 4	86A.5.3.3
Electrical waveform (eye mask)	3, 5, or valid 40GBASE-SR4 or 100GBASE-SR10 signal	86.8.3.2, 86A.5.3.6
Q_{sq}	Square wave or 4	86A.5.3.5
Host electrical receiver signal tolerance	3 or 5	86A.5.3.8

given in 86.8.2.1. As Pattern 3 is more demanding than Pattern 5 (which itself is the same or more demanding than other 40GBASE-R or 100GBASE-R bit streams) an item which is compliant using Pattern 5 is considered compliant even if it does not meet the required limit using Pattern 3.

86A.5.3 Parameter definitions

In addition to the parameter definitions in the following subclause, some definitions with dual use (both optical and electrical) are given in 86.8.3.

86A.5.3.1 AC common-mode voltage

The common-mode voltage of a differential signal at any time is the average of signal+ and signal– at that time. RMS AC common-mode voltage may be calculated by applying the histogram function over 1 UI to the common-mode signal. As AC common-mode generation is very sensitive to the cable or oscilloscope delay mismatch, it is recommended to delay match the oscilloscope inputs for any measurements.

86A.5.3.2 Termination mismatch

Termination mismatch is the percentage difference between the two low-frequency impedances to common of a differential electrical port. Termination mismatch is defined as shown in Equation (86A–10).

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$$\Delta Z_M = 2 \times \frac{|Z_p - Z_n|}{Z_p + Z_n} \times 100\ \% \quad (86A–10)$$

Termination mismatch can be measured by applying a low-frequency test tone to the differential inputs as shown in Figure 86A–6. The test frequency has to be high enough to overcome the high pass effects of any AC-coupling capacitors. The measured differential output or input impedance is designated by Z_{diff}.

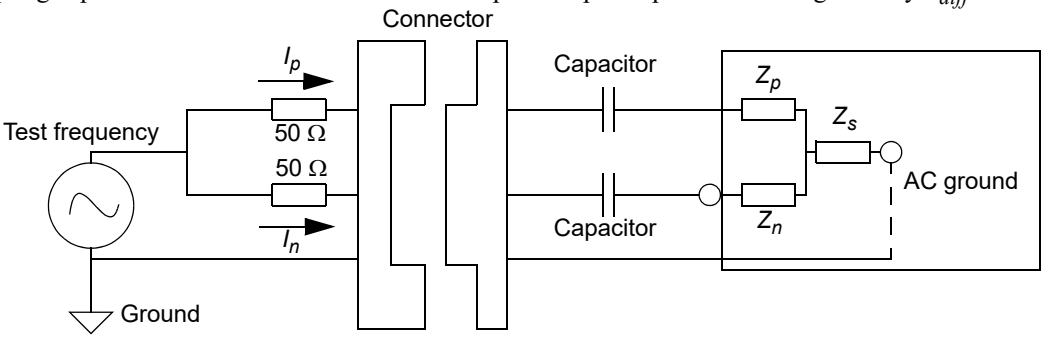

Figure 86A–6—Measurement of AC termination mismatch

For a 100 Ω port, low-frequency termination mismatch is then given by Equation (86A–11).

$$\Delta Z_M = 2 \times \frac{|I_p - I_n|}{I_p + I_n} \times \frac{Z_{diff} + 100}{Z_{diff}} \times 100\ \% \quad (86A–11)$$

where I_p and I_n are the currents flowing into the port as shown in Figure 86A–6.

Z_s is the effective series impedance between the terminations Z_p and Z_n and the AC ground.

86A.5.3.3 Transition time

In this annex, transition times (rise and fall times) are defined as the time between the 20% and 80% times, or 80% and 20% times, respectively, of isolated edges.

If the test pattern is the square wave with eight ones and eight zeros, the 0% level and the 100% level are as defined by the OMA measurement procedure (see 68.6.2).

If the test pattern is PRBS9, the transitions within sequences of five zeros and four ones, and nine ones and five zeros, respectively, are measured. These are bits 10 to 18 and 1 to 14, respectively, where bits 1 to 9 are the run of nine ones. In this case, the 0% level and the 100% level may be estimated as ZeroLevel and ZeroLevel + MeasuredOMA in the TWDP code (see 68.6.6.2), or by the average signal within windows from –3 UI to –2 UI and from 2 UI to 3 UI relative to the edge.

For electrical signals, the waveform is observed through a 12 GHz low-pass filter response (such as a Bessel-Thomson response).

NOTE—This definition is not the same as the rise and fall times typically reported by an oscilloscope from an eye diagram, which take all the edges into account.

86A.5.3.4 Data Dependent Pulse Width Shrinkage (DDPWS)

An oscilloscope, time interval analyzer, or other instrument with equivalent capability may be used to measure DDPWS. A clock recovery unit (CRU) as defined in 86.8.3.2 is used to trigger the oscilloscope. A repeating PRBS9 pseudo-random test pattern, 511 bits long, is used. For electrical jitter measurements, the

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measurement bandwidth is 12 GHz (such as a Bessel-Thomson response). If the measurement bandwidth affects the result, it can be corrected for by post-processing. However, a bandwidth above 12 GHz is expected to have little effect on the results.

The crossing level is the average value of the entire waveform being measured. The instrument is synchronized to the pattern repetition frequency and the waveforms or the crossing times are averaged sufficiently to remove the effects of random jitter and noise in the system. The PRBS9 pattern has 128 positive-going transitions and 128 negative-going transitions. The crossing times t_1 to t_{256} of each transition of the averaged waveform (when the averaged waveform crosses the crossing level) are found as shown in Figure 86A–7.

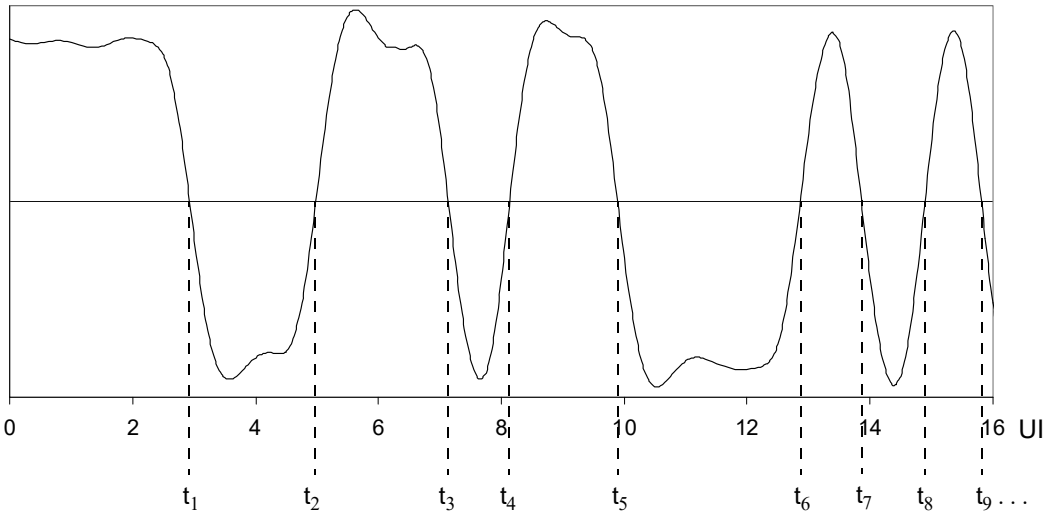

Figure 86A–7—Data Dependent Pulse Width Shrinkage test method

The DDPWS is the difference between one symbol period and the minimum of all the differences between pairs of adjacent transitions as follows in Equation (86A–12).

$$DDPWS = \mathrm{T} - \min(t_2 - t_1, t_3 - t_2, \ldots\ldots t_{256+1} - t_{256}) \quad (86A–12)$$

where T is one symbol period.

Note that the difference from the next edge in the repeating sequence, t_{256+1}, is also considered.

86A.5.3.5 Signal to noise ratio Q_{sq}

Q_{sq} is a measure of signal to noise ratio. For an electrical signal, it is analogous to Q_{sq} defined for an optical signal in 68.6.7, and it relates the low-frequency signal amplitude to the noise in an electrical –3 dB bandwidth of 12 GHz. It is defined with all co-propagating and counter-propagating crosstalk sources active, using one of patterns 3, 5, or a valid 40GBASE-SR4 or 100GBASE-SR10 signal. The input lanes of the item under test are receiving signals that are asynchronous to those being output.

Q_{sq} may be measured using an oscilloscope as follows:

a) The Voltage Modulation Amplitude (VMA) of the output lane is measured, using a square wave (8 ones, 8 zeros) or PRBS9 (Pattern 4). VMA is the difference between the 0% level and the 100% level defined in 86A.5.3.3; it is defined by analogy to OMA (see 68.6.2) but with a 12 GHz observation bandwidth.

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b) Using the same pattern, the RMS noise over flat regions of the logic one and logic zero portions of the signal (see Figure 68–4 for the analogous optical measurement), is measured, compensating for noise in the measurement system. If possible, means should be used to prevent noise of frequency less than 1 MHz from affecting the result.
c) Q_{sq} is given by Equation (86A–13).

$$Q_{sq} = VMA / (n1 + n0) \quad (86A–13)$$

where

n1 is the RMS noise of logic one
n0 is the RMS noise of logic zero

86A.5.3.6 Eye mask for TP1a and TP4

The eye mask is defined by parameters X1, X2, Y1, and Y2. Unlike the optical eye mask, the vertical dimensions are fixed rather than scaled to the signal. Figure 83A–8 (an example of a hexagonal eye mask such as at TP1a) and Figure 83A–9 (a diamond mask such as at TP4) show the meaning of the parameters X1, X2, Y1 and Y2. The eye is defined as measured using a receiver with an electrical –3 dB bandwidth of 12 GHz (such as a Bessel-Thomson response). Further requirements are given in 86.8.3.2.

86A.5.3.7 Reference impedances for electrical measurements

The reference impedance for differential electrical measurements is 100 Ω and the reference impedance for common-mode electrical measurements is 25 Ω.

86A.5.3.8 Host input signal tolerance

To be compliant the host input signal tolerance shall satisfy the requirements of 86A.5.3.8.1 to 86A.5.3.8.6.

86A.5.3.8.1 Introduction

This subclause provides guidance for jitter tolerance testing at the host input (PMA) compliance point TP4/TP4a. Compliance is required with input jitter, vertical eye closure (Y1), and vertical peak level (Y2) as specified in Table 86A–4. Compliance is defined at an interface BER (the average of the BERs of all the lanes when stressed) of 10^{-12}. There are two test conditions: one each for the sensitivity and overload vertical eye parameters conditions. The reference test procedure is described in detail for a single stressed lane. Each Rx lane is tested in turn while all lanes are operated. Aggressor lanes are operated with the VMA specified in Table 86A–4.

86A.5.3.8.2 Test equipment and setup

A jitter tolerance test configuration is shown in Figure 86A–8. A test source is used to continuously generate the test signal. The test signal is conditioned within the guidelines outlined in 86A.5.3.8.3 to exhibit the appropriate jitter stress.

An RF attenuator or other output amplitude control of the test source may be required to set the vertical eye opening of the stressed eye.

The test equipment measured at TP4a looking towards the test signal source has better than 20 dB output return loss up to 12 GHz. The output return loss of the test system when measured at TP4 with the Module Compliance Board (looking towards the test signal source) is 2 dB better than the specifications of Table 86A–3 up to 8 GHz and 1 dB better up to 11 GHz.

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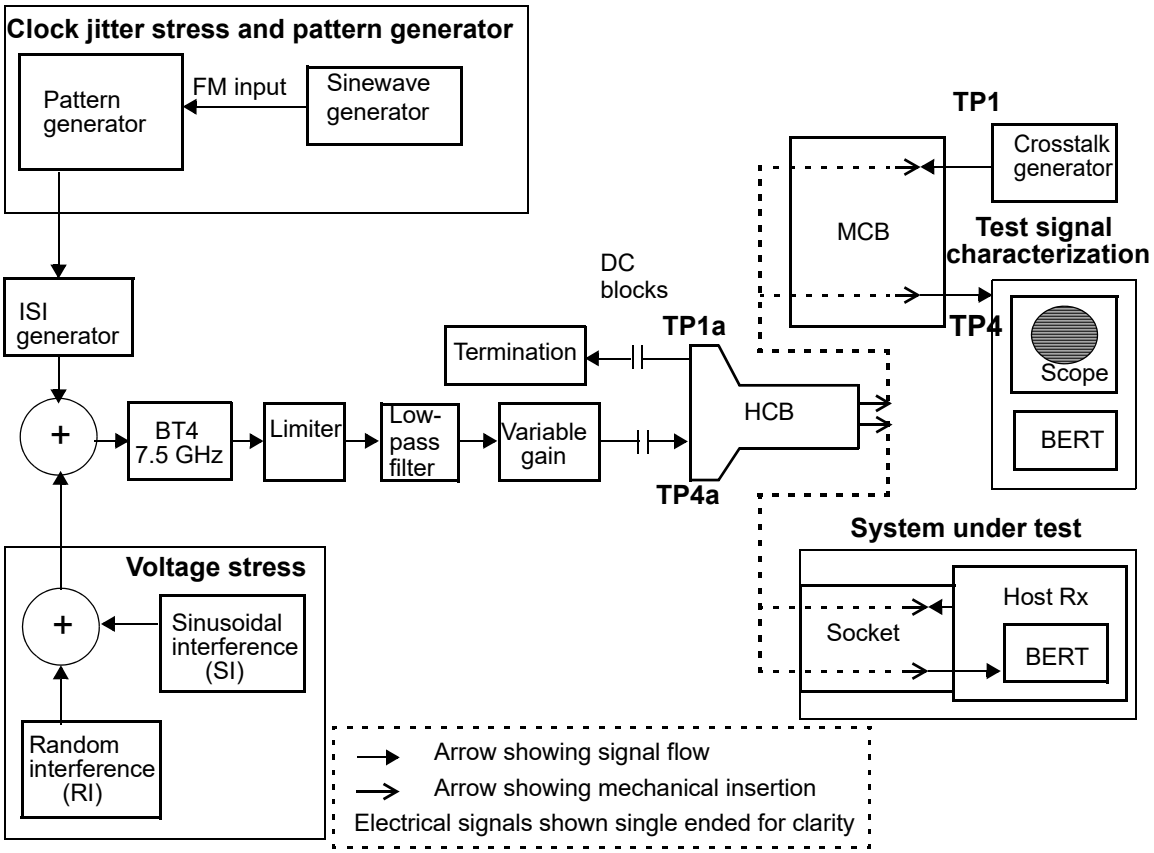

Figure 86A–8—Example jitter tolerance test configuration

86A.5.3.8.3 Stressed eye jitter characteristics

This subclause describes required test signal characteristics along with considerations and suggested approaches for test signal generation. The test signal is generated by the functions shown in Figure 86A–8 or by equivalent means. Figure 86A–9 illustrates how the jitter parameters in Table 86A–4 map to the jitter components in the stressed-eye test signal.

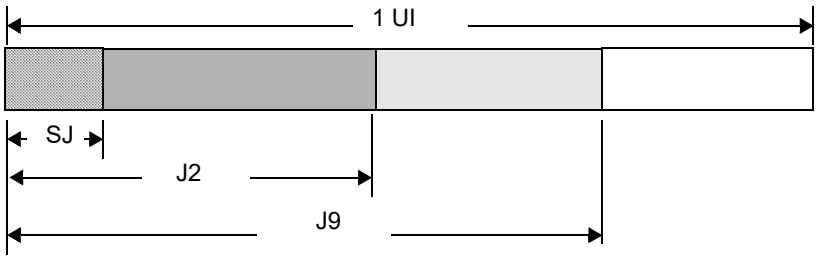

Figure 86A–9—Stressed eye jitter components

The 0.05 UI Sinusoidal Jitter (SJ) component of J2 Jitter is defined for frequencies much higher than the CDR bandwidth (e.g., ~20 MHz). At lower frequencies, the CDR has to track additional applied SJ as detailed in the relevant specifications (see Figure 86A–10 and 52.8.1).

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The balance of the J2 Jitter is created by the following mechanisms: an ISI generator, sinusoidal interference (SI), and random interference (RI), all passed through a limiting function.

The test signal at TP4 has DDPWS as defined by Table 86A–4. Any duty cycle distortion (DCD) in the test signal does not exceed 0.02 UI. DCD is the difference between the mean position of all falling edges and the mean position of all rising edges of a waveform. It is measured at the average level of the waveform in a 12 GHz bandwidth, using Pattern 3 (PRBS31), Pattern 4 (PRBS9), Pattern 5, or a valid 40GBASE-SR4 or 100GBASE-SR10 signal.

The ISI generator may be implemented by a low-pass filter, length of FR4 trace, length of coax cable, or other equivalent method. It is required that the resulting signal be passed through a limiter function. A suitable limiter function may be implemented using a discrete limiting amplifier followed by a low-pass filter and an attenuator. The low-pass filter emulates the bandwidth and/or slew rate of a practical limiter. The attenuator is used to set the output amplitude to minimum and maximum values allowed by the eye mask coordinates of Table 86A–4.

A voltage stress is to be applied before the limiter function. This stress is composed of a single tone sinusoidal interferer (SI) in the frequency range 100 MHz to 2 GHz and a broadband noise source (RI) with a minimum power spectrum –3 dB point of 6 GHz and minimum crest factor of 7. It is the intent that this combination of voltage stress and limiting function introduce pulse-shrinkage jitter behavior. However, no more than 20% of the J2 Jitter is created by the sinusoidal interferer.

Jitter generation mechanisms for the pattern generator are typically based on phase modulation of the clock source, edge modulation of a variable delay line or a combination thereof.

Any approach that modulates or creates the appropriate levels and frequencies of the jitter components is acceptable.

86A.5.3.8.4 Calibration

Calibration of the test signal is performed using the guidelines for test setup in 86A.5.3.8.2 and illustrated in Figure 86A–8. The aim of the calibration is to achieve a test signal exhibiting jitter stress in accordance with Table 86A–4.

The test signal is calibrated differentially into standard instrumentation loads. If complementary single-ended signals are used, they are carefully matched in both amplitude and phase.

For accurate calibration, it is imperative that all elements in the signal path (cables, DC blocks, etc.) have wide and smooth frequency response as well as linear phase response throughout the spectrum of interest. Baseline wander and overshoot/undershoot are minimized.

An AC-coupling –3 dB corner frequency of 20 kHz is expected to be adequate to eliminate baseline wander effects; however, high-frequency performance is critical and should not be sacrificed by the AC-coupling.

Given random jitter and the nature of the long test patterns, low probability jitter events will likely be present. It is recommended for jitter calibration that a technique that can accurately measure low probability events be used to avoid overly stressful test conditions.

It is recommended that the actual compliance test pattern be used during calibration. For jitter stress calibration it is permissible, however, to use any appropriate test pattern that still results in the creation of a compliance test pattern with the appropriate jitter stress.

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86A.5.3.8.5 Calibration procedure

The vertical eye opening and peak level are set approximately to the levels specified in Table 86A–4.

With an applied calibration test pattern and no additional jitter stress applied, the intrinsic J2 Jitter and J9 Jitter of the test source due to intrinsic noise and finite bandwidth effects are measured. At this stage, J2 Jitter is less than 0.15 UI and J9 Jitter less than 0.25 UI.

SJ is added until the J2 Jitter increases by 0.05 UI above this intrinsic J2 Jitter level. The SJ jitter frequency is well above the CDR bandwidth and asynchronous to the characteristic frequencies of the signal.

Next, additional high probability jitter as specified in 86A.5.3.8.3 is added by the ISI generator until at least 80% of the J2 Jitter has been created. The sinusoidal interferer amplitude is then turned on and adjusted until the required level of J2 Jitter is achieved. The frequency of any sinusoidal interferer is asynchronous to the characteristic frequencies of the signal.

A compliant test signal exhibits Data Dependent Pulse Width Shrinkage (defined in 86A.5.3.4) as specified in Table 86A–4. This is measured with noise and clock-jitter sources turned off.

Once the required level of J2 Jitter has been achieved, turn on the crosstalk source that is set such that at the output of the Host Compliance Board, the amplitude and the transition time are as given in Table 86A–4. The crosstalk pattern is Pattern 3 (PRBS31), Pattern 5, or a valid 40GBASE-SR4 or 100GBASE-SR10 signal, and is asynchronous with the test signal. Then the RI (random interference) voltage stress is added until the specified value of J9 Jitter is achieved.

If necessary, the sine interferer is readjusted to obtain the required level of J2 Jitter and if the sinusoidal interferer is changed then the random interferer is readjusted to obtain the required level of J9 Jitter. Iterative adjustments of the sinusoidal interferer and random interferer are made until the required values of both J2 Jitter and J9 Jitter are achieved.

If necessary, the vertical eye opening is readjusted to required levels.

The vertical eye opening and peak level specifications are verified.

Care should be taken when characterizing the signal used to make receiver tolerance measurements. The intrinsic noise and jitter introduced by the calibration measurement equipment (e.g., filters, oscilloscope and BERT) have to be accounted for and controlled. If equipment imperfections affect the results materially, corrections such as root-sum-of-squares deconvolution of Gaussian noise and jitter are used.

86A.5.3.8.6 Test procedure

Testing is performed differentially through a Host Compliance Board (see 86A.5.1).

Using a test signal arranged according to 86A.5.3.8.2 and calibrated according to 86A.5.3.8.5, operate the system with the test pattern specified in Table 86A–6. Each lane is tested in turn while all are operated. Aggressor lanes are operated with the VMA specified in Table 86A–4. The BERs of all the lanes when stressed are averaged to form the interface BER. See 86.8.2.1.

All signals and reference clocks that operate during normal operation are active during the test including all the other host lanes in both directions. The test signal and the host's transmitted signals are asynchronous. The host transmits Pattern 3 (PRBS31), Pattern 5, or a valid 40GBASE-SR4 or 100GBASE-SR10 signal. The sinusoidal jitter is stepped across the frequency and amplitude range according to Table 86A–7 and illustrated in Figure 86A–10, while monitoring the BER of the lane(s). The interface BER of a compliant host receiver remains below 10^{-12}.

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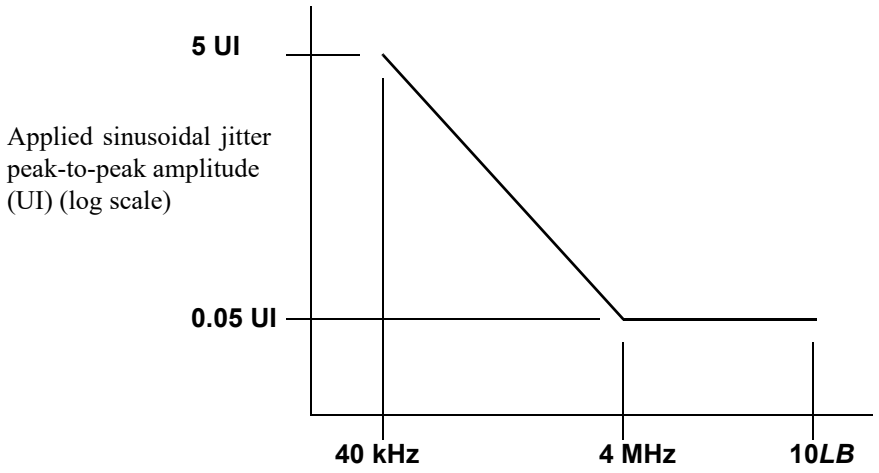

Figure 86A–10—Mask of the sinusoidal component of jitter tolerance

Table 86A–7—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter, peak-to-peak, (UI)
$f < 40$ kHz	Not specified
40 kHz $\le f <$ 4 MHz	2×10^5 Hz / f
4 MHz $\le f \le 10\ LB$[a]	0.05

[a]*LB* = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

86A.6 Recommended electrical channel

The recommended limits for the differential insertion loss in decibels of the host PCB and connector mated to the HCB, between the PMA IC (TP0 or TP5) and TP1a or TP4a, are given in Equation (86A–14) and Equation (86A–15), and illustrated in Figure 86A–11. It is recommended that

$$Insertion\_loss(f) \le \left\{ \begin{array}{ll} 0.5 & 0.01 \le f < 0.11 \\ 0.114 + 0.8914\sqrt{f} + 0.846f & 0.11 \le f < 7 \\ -35.91 + 6.3291f & 7 \le f < 8 \\ 14.72 & 8 \le f \le 11.1 \end{array} \right\} \text{ dB} \qquad (86A–14)$$

and

$$Insertion\_loss(f) \ge \left\{ \begin{array}{ll} -0.22 + 0.46f & 0.01 \le f < 7 \\ 3 & 7 \le f \le 11.1 \end{array} \right\} \text{ dB} \qquad (86A–15)$$

where

Insertion_loss(*f*) is the insertion loss at frequency *f*
f is the frequency in GHz

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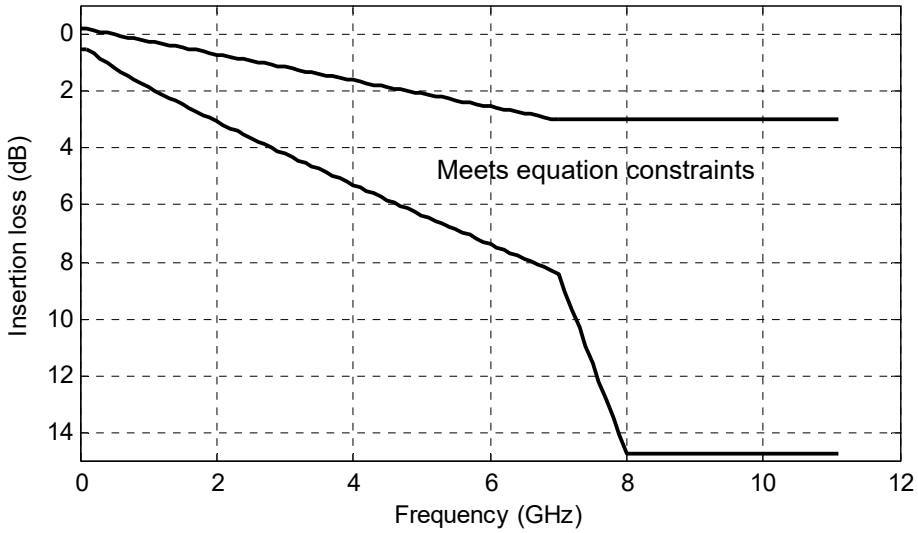

Figure 86A–11—Recommended insertion loss limits of host PCB, connector and HCB

The recommended maximum loss of the host PCB only (without connector or HCB) at 5.15625 GHz is 4.4 dB.

86A.7 Safety, installation, environment, and labeling

86A.7.1 General safety

Equipment subject to this annex shall conform to the general safety requirements in J.2.

86A.7.2 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

86A.7.3 Environment

The 40GBASE–SR4 and 100GBASE–SR10 operating environment specifications are as defined in 52.11, as defined in 52.11.1 for electromagnetic emission, and as defined in 52.11.2 for temperature, humidity, and handling.

86A.7.4 PMD labeling

The 40GBASE–SR4 and 100GBASE–SR10 labeling recommendations and requirements are as defined in 52.12.

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86A.8 Protocol implementation conformance statement (PICS) proforma for Annex 86A, Parallel Physical Interface (nPPI) for 40GBASE-SR4 and 40GBASE-LR4 (XLPPI) and 100GBASE-SR10 (CPPI)[298]

86A.8.1 Introduction

The supplier of an XLPPI/CPPI implementation that is claimed to conform to Annex 86A, Parallel Physical Interface (nPPI) for 40GBASE-SR4 and 40GBASE-LR4 (XLPPI) and 100GBASE-SR10 (CPPI), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the same, can be found in Clause 21.

86A.8.2 Identification

86A.8.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

86A.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 86A, Parallel Physical Interface (nPPI) for 40GBASE-SR4 and 40GBASE-LR4 (XLPPI) and 100GBASE-SR10 (CPPI)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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86A.8.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*R4	40GBASE–R4	86A.4	Can operate as part of 40GBASE–SR4 or 40GBASE-LR4 PMA or PMD	O.1	Yes [ ] No [ ]
*R10	100GBASE–SR10	86A.4	Can operate as part of 100GBASE–SR10 PMA or PMD	O.1	Yes [ ] No [ ]
*MO	Module		Items marked with MO are applicable to a module (PMD)	O.2	Yes [ ] No [ ]
*HO	Host		Items marked with HO are applicable to a host (PMA)	O.2	Yes [ ] No [ ]
*MD	MDIO capability	86A.1	Registers and interface supported	O	Yes [ ] No [ ]

86A.8.4 PICS proforma tables for Parallel Physical Interface (nPPI) for 40GBASE-SR4 and 40GBASE-LR4 (XLPPI) and 100GBASE-SR10 (CPPI)

86A.8.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
SF1	Compatible with 40GBASE–R or 100GBASE–R PCS and PMA and 40GBASE–SR4, 40GBASE–LR4 or 100GBASE–SR10 PMD	86A.1		M	Yes [ ]

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86A.8.4.2 Electrical specifications for nPPI

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Signaling rate per Table 86–2	86A.4	10.3125 GBd ±100 ppm	M	Yes [ ]
S2	Host output signal per Table 86A–1	86A.4.1	Per definitions in 86A.5	HO:M	Yes [ ] N/A [ ]
S3	Module electrical input per Table 86A–2	86A.4.1	Per definitions in 86A.5	MO:M	Yes [ ] N/A [ ]
S4	Module electrical input AC-coupled	86A.4.1		MO:M	Yes [ ] N/A [ ]
S5	Module electrical differential input return loss at TP1	86A.4.1.1	Per Equation (86A–1)	MO:M	Yes [ ] N/A [ ]
S6	Host differential output return loss at TP1a	86A.4.1.1	Per Equation (86A–1)	HO:M	Yes [ ] N/A [ ]
S7	Module electrical output per Table 86A–3	86A.4.2	Per definitions in 86A.5	MO:M	Yes [ ] N/A [ ]
S8	Host input per Table 86A–4	86A.4.2	Per definitions in 86A.5	HO:M	Yes [ ] N/A [ ]
S9	Module electrical output AC-coupled	86A.4.2		MO:M	Yes [ ] N/A [ ]
S10	Module electrical output return loss at TP4	86A.4.2.1	Per Equation (86A–2)	MO:M	Yes [ ] N/A [ ]
S11	Host differential input return loss at TP4a	86A.4.2.1	Per Equation (86A–2)	HO:M	Yes [ ] N/A [ ]

86A.8.4.3 Definitions of parameters and measurement methods

Item	Feature	Subclause	Value/Comment	Status	Support
SEM1	Compliance boards	86A.5.1	Use compliance boards, correct as necessary	M	Yes [ ]
SEM2	Compliance boards	86A.5.1.1	Results corrected	M	Yes [ ]
SEM3	Compliance boards	86A.5.1.1	Individual insertion losses per 86A.5.1.1.2	M	Yes [ ]
SEM4	Compliance boards	86A.5.1.1	Mated HCB-MCB per 86A.5.1.1.2	M	Yes [ ]
SEM5	Host input signal tolerance	86A.5.3.8	As specified	HO:M	Yes [ ] N/A [ ]

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86A.8.4.4 Environmental and safety specifications

Item	Feature	Subclause	Value/Comment	Status	Support
SES1	General safety	86A.7.1	Conforms to J.2	M	Yes [ ]
SES2	Electromagnetic interference	86A.7.3	Complies with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

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Annex 91A

(informative)

RS-FEC codeword examples

This annex provides example RS-FEC codewords produced by the 64B/66B to 256B/257B transcoding and Reed-Solomon encoding defined in Clause 91. This annex presents data in a tabular form. The contents of the tables are transmitted from left to right within each row starting from the top row and ending at the bottom row. The tables contain both binary and hexadecimal representations of the data. For the hexadecimal representation, the most significant bit of each hex symbol is transmitted first.

91A.1 Input to the 64B/66B to 256B/257B transcoder

Table 91A–1 contains a sequence of 80 66-bit blocks corresponding to the PCS transmission of Idle control characters. The initial value of the scrambler was set to bits 6 to 63 of the first 64-bit payload in the first row of Table 74A–2. Bit 6 is assigned to S57 and bit 63 is assigned to S0 (see 49.2.6).

Table 91A–1—64B/66B to 256B/257B transcoder input

Sync <0:1>	64-bit payload, hex <2:65>	Sync <0:1>	64-bit payload, hex <2:65>	Sync <0:1>	64-bit payload, hex <2:65>	Sync <0:1>	64-bit payload, hex <2:65>
10	AD5A3BF86D9ACF5C	10	DE55CB85DF0F7CA0	10	E6CCFF8E8212B1C6	10	D63BC6C309000638
10	70E3B0CE30E0497D	10	DC8DF31EC3AB4491	10	66FB9139C81CD37B	10	B57477D4F05E3602
10	8CFD495012947A31	10	E7777CF0C6D06280	10	44529CF4B4900528	10	85CE1D27750AD61B
10	456D5C71743F5C69	10	C1BF62E5DC5464B5	10	DC6011BE7EA1ED54	10	1CF92C450042A75F
10	CC4B940EAF3140DB	10	77BB612A7ABF401F	10	C22D341E90545D98	10	CE6DAF1F248BBD6D
10	DD22D0B3F9551ED6	10	574686C3F9E93898	10	2E52628F4A1282CE	10	F20C86D71944AAB1
10	55133C9333808A2C	10	1AA825D8B817DB4D	10	637959989F3021EB	10	976806641B26AAE9
10	6A37D4531B7ED5F2	10	53C3E96D3B12FB46	10	528C7EB8481BC969	10	AB8F9980D5A54559
10	9A4D2ABFDA65CC33	10	94FE646EFE5AF02D	10	9A65AE5FCD88C03A	10	5EF08673168DEF9B
10	220C871A953FFFC6	10	CE0BB95AC263E6C1	10	4F6A917D1A676571	10	5890918C7B687D75
10	44D2B3E43096F836	10	84CDD4FC48B79608	10	B3E4503E3C824A8C	10	FD6D0B1A39687929
10	1730167C08302A69	10	4C15FF56DE92B1AD	10	D0C2F0D4FF0DEE95	10	E1422EE2E8B92125
10	ED5ACAF86592FCEE	10	DE799BE0B903C880	10	2714FFBF40BC09F6	10	C3BE97C3C285009F
10	1020FAF19F606631	10	93007CABBB3F8C9D	10	EF6955F7F43DF5D0	10	4DBD0616AFE60E1F
10	3A1E49B7C7F7BB5D	10	901D828746CEEC61	10	71ED3C097158C224	10	11ADB3D81E13D263
10	A350D1A343B2394B	10	EAB30CA27B5B34E3	10	90359EF711ED53D9	10	9B446763C8627EA8
10	6E891C0F4842B823	10	C4D786A25727A7FC	10	094FE7DA31FB60CD	10	9F9A004DE5E70767
10	054BDD77B7CB4E7B	10	C598CB710558AF67	10	FC386D1F99D3A925	10	4928E0B43E781893
10	5A44DD3EB8B2AD6C	10	94462AF4F583D770	10	8061BA9381F51F55	10	476D4EDED7C90FCC
10	1EFC25AA6A7E0B4C	10	93DD968C06A56809	10	9768E9D1BA74D3B6	10	014E9DC9F13670BB

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91A.2 Output of the RS(528,514) encoder

Table 91A–2 contains a RS(528,514) codeword. Each row of Table 91A–1 is a set of four 66-bit blocks that is converted to one 257-bit block using the procedure defined in 91.5.2.5. The resulting set of 20 257-bit blocks constitute the message portion of the codeword. The parity is computed using the encoder defined in 91.5.2.7 and is appended to the message to complete the codeword.

Table 91A–2—RS(528,514) codeword

Header <0:4>	Payload, hex <5:64>	Payload, hex <65:128>	Payload, hex <129:192>	Payload, hex <193:256>
00101	A5A3BF86D9ACF5C	DE55CB85DF0F7CA0	E6CCFF8E8212B1C6	D63BC6C309000638
11110	7E3B0CE30E0497D	DC8DF31EC3AB4491	66FB9139C81CD37B	B57477D4F05E3602
01111	8FD495012947A31	E7777CF0C6D06280	44529CF4B4900528	85CE1D27750AD61B
00110	46D5C71743F5C69	C1BF62E5DC5464B5	DC6011BE7EA1ED54	1CF92C450042A75F
00100	C4B940EAF3140DB	77BB612A7ABF401F	C22D341E90545D98	CE6DAF1F248BBD6D
10010	D22D0B3F9551ED6	574686C3F9E93898	2E52628F4A1282CE	F20C86D71944AAB1
10001	5133C9333808A2C	1AA825D8B817DB4D	637959989F3021EB	976806641B26AAE9
00011	637D4531B7ED5F2	53C3E96D3B12FB46	528C7EB8481BC969	AB8F9980D5A54559
10100	94D2ABFDA65CC33	94FE646EFE5AF02D	9A65AE5FCD88C03A	5EF08673168DEF9B
00000	20C871A953FFFC6	CE0BB95AC263E6C1	4F6A917D1A676571	5890918C7B687D75
01101	4D2B3E43096F836	84CDD4FC48B79608	B3E4503E3C824A8C	FD6D0B1A39687929
10011	130167C08302A69	4C15FF56DE92B1AD	D0C2F0D4FF0DEE95	E1422EE2E8B92125
00101	E5ACAF86592FCEE	DE799BE0B903C880	2714FFBF40BC09F6	C3BE97C3C285009F
10010	120FAF19F606631	93007CABBB3F8C9D	EF6955F7F43DF5D0	4DBD0616AFE60E1F
10001	31E49B7C7F7BB5D	901D828746CEEC61	71ED3C097158C224	11ADB3D81E13D263
00101	A50D1A343B2394B	EAB30CA27B5B34E3	90359EF711ED53D9	9B446763C8627EA8
01000	6891C0F4842B823	C4D786A25727A7FC	094FE7DA31FB60CD	9F9A004DE5E70767
00100	04BDD77B7CB4E7B	C598CB710558AF67	FC386D1F99D3A925	4928E0B43E781893
10100	544DD3EB8B2AD6C	94462AF4F583D770	8061BA9381F51F55	476D4EDED7C90FCC
11111	1FC25AA6A7E0B4C	93DD968C06A56809	9768E9D1BA74D3B6	014E9DC9F13670BB
Parity, hex <0:63>	**Parity, hex <64:127>**	**Parity, hex <128:139>**		
ED0E78F1734BC808	A38C0C417BD68F36	825		

91A.3 Output of the RS(544,514) encoder

Table 91A–3 contains a RS(544,514) codeword. Each row of Table 91A–1 is a set of four 66-bit blocks that is converted to one 257-bit block using the procedure defined in 91.5.2.5. The resulting set of 20 257-bit blocks constitute the message portion of the codeword. The parity is computed using the encoder defined in 91.5.2.7 and is appended to the message to complete the codeword.

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Table 91A–3—RS(544,514) codeword

Header <0:4>	Payload, hex <5:64>	Payload, hex <65:128>	Payload, hex <129:192>	Payload, hex <193:256>
00101	A5A3BF86D9ACF5C	DE55CB85DF0F7CA0	E6CCFF8E8212B1C6	D63BC6C309000638
11110	7E3B0CE30E0497D	DC8DF31EC3AB4491	66FB9139C81CD37B	B57477D4F05E3602
01111	8FD495012947A31	E7777CF0C6D06280	44529CF4B4900528	85CE1D27750AD61B
00110	46D5C71743F5C69	C1BF62E5DC5464B5	DC6011BE7EA1ED54	1CF92C450042A75F
00100	C4B940EAF3140DB	77BB612A7ABF401F	C22D341E90545D98	CE6DAF1F248BBD6D
10010	D22D0B3F9551ED6	574686C3F9E93898	2E52628F4A1282CE	F20C86D71944AAB1
10001	5133C9333808A2C	1AA825D8B817DB4D	637959989F3021EB	976806641B26AAE9
00011	637D4531B7ED5F2	53C3E96D3B12FB46	528C7EB8481BC969	AB8F9980D5A54559
10100	94D2ABFDA65CC33	94FE646EFE5AF02D	9A65AE5FCD88C03A	5EF08673168DEF9B
00000	20C871A953FFFC6	CE0BB95AC263E6C1	4F6A917D1A676571	5890918C7B687D75
01101	4D2B3E43096F836	84CDD4FC48B79608	B3E4503E3C824A8C	FD6D0B1A39687929
10011	130167C08302A69	4C15FF56DE92B1AD	D0C2F0D4FF0DEE95	E1422EE2E8B92125
00101	E5ACAF86592FCEE	DE799BE0B903C880	2714FFBF40BC09F6	C3BE97C3C285009F
10010	120FAF19F606631	93007CABBB3F8C9D	EF6955F7F43DF5D0	4DBD0616AFE60E1F
10001	31E49B7C7F7BB5D	901D828746CEEC61	71ED3C097158C224	11ADB3D81E13D263
00101	A50D1A343B2394B	EAB30CA27B5B34E3	90359EF711ED53D9	9B446763C8627EA8
01000	6891C0F4842B823	C4D786A25727A7FC	094FE7DA31FB60CD	9F9A004DE5E70767
00100	04BDD77B7CB4E7B	C598CB710558AF67	FC386D1F99D3A925	4928E0B43E781893
10100	544DD3EB8B2AD6C	94462AF4F583D770	8061BA9381F51F55	476D4EDED7C90FCC
11111	1FC25AA6A7E0B4C	93DD968C06A56809	9768E9D1BA74D3B6	014E9DC9F13670BB
Parity, hex <0:63>	**Parity, hex <64:127>**	**Parity, hex <128:191>**	**Parity, hex <192:255>**	**Parity, hex <256:299>**
D6983839EDC3E5AC	C3CB45691DDBA6CB	C26D756EA6F5B73D	249E30F415AA60B1	5743DC81C21

91A.4 Reed-Solomon encoder model

This annex also includes a model of the Reed-Solomon encoder, defined in 91.5.2.7, written in the C programming language. To emulate the RS(528,514) encoder, declare global variables per 91A.4.1. To emulate the RS(544,514) encoder, declare global variables per 91A.4.2. The generic components of the model are defined in 91A.4.3 to 91A.4.6.

91A.4.1 Global variable declarations for RS(528,514)

These global variables define the codeword size (in symbols) and generator polynomial coefficients (see Table 91–1) for the RS(528,514) code. Elements of GF(2^{10}) are presented as decimal values.

```
long n_symbols = 528;
unsigned long generator_polynomial[1024] =
   {904,6,701,32,656,925,900,614,391,592,265,945,290,432};
```


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91A.4.2 Global variable declarations for RS(544,514)

These global variables define the codeword size and generator polynomial coefficients for the RS(544,514) code.

```
long n_symbols = 544;
unsigned long generator_polynomial[1024] =
   {575,552,187,230,552,1,108,565,282,249,593,132,94,720,495,385,942,503,883,36
   1,788,610,193,392,127,185,158,128,834,523};
```

91A.4.3 Other global variable declarations

The following global variables are declared for both RS(528,514) and RS(544,514). The field polynomial is assigned its decimal representation (1033 corresponds to $x^{10}+x^3+1$).

```
long polynomial = 1033;
long k_symbols = 514;
long check_symbols;
unsigned long codeword[1024];
```

91A.4.4 GF(2^{10}) multiplier function

This function implements multiplication over GF(2^{10}) using the expansion and reduction algorithm.

```
unsigned long multiply(long aa, long bb)
{
   unsigned long expand = 0;
   long k;

   for (k = 0; k < 10; k++)
   {
      if (bb & (1 << k))
         expand = expand ^ (aa << k);
   }

   for (k = 0; k < 9; k++)
   {
      if ((expand >> (18-k)) & 1)
         expand = expand ^ (polynomial << (8-k));
   }

   return expand;
}
```

91A.4.5 Reed-Solomon encoder function

This function implements the Reed-Solomon encoder. It uses the multiply() function.

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```
void encode()
{
    long k, j;
    unsigned long multiplier;
    unsigned long generator_vector[1024];
    unsigned long encoder_divide[1024];

    for (k = 0; k < check_symbols; k++)
        encoder_divide[k] = 0;

    for (k = 0; k < k_symbols; k++)
    {
        multiplier = codeword[k] ^ encoder_divide[0];

        for (j = 0; j < check_symbols; j++)
            generator_vector[j] = multiply(multiplier, generator_polynomial[j]);

        for (j = 0; j < check_symbols-1; j++)
            encoder_divide[j] = generator_vector[j] ^ encoder_divide[j+1];

        encoder_divide[check_symbols-1] = generator_vector[check_symbols-1];

        for (j = 0; j < check_symbols; j++)
            codeword[j+k_symbols] = encoder_divide[j];
    }
}
```

91A.4.6 Main function

This sample main function defines a hypothetical message consisting of a countdown from 1023 to 510 (514 Reed-Solomon symbols). It then computes the parity and produces a codeword using the encode() function. The resulting codeword is printed to the console.

```
void main()
{
    long k;
    check_symbols = n_symbols-k_symbols;

    //*** Generate simple message symbols ***
    for (k = 0; k < k_symbols; k++)
        codeword[k] = 1023-k;

    encode();

    for (k = 0; k < n_symbols; k++)
        printf("%ld ", codeword[k]);
}
```


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Annex 92A

(informative)

100GBASE-CR4 TP0 and TP5 test point parameters and channel characteristics

92A.1 Overview

Annex 92A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system. TP0 and TP5 test points are illustrated in the 100GBASE-CR4 link block diagram of Figure 92–2. It also provides information on channel characteristics.

92A.2 Transmitter characteristics at TP0

The transmitter characteristics at TP0 are constrained at TP0a by 93.8.1.

92A.3 Receiver characteristics at TP5

The receiver characteristics at TP5 are constrained at TP5a by 93.8.2.

92A.4 Transmitter and receiver differential printed circuit board trace loss

The recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is determined using Equation (92A–1) and illustrated in Figure 92A–1. Note that the recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is 6.81 dB at 12.8906 GHz. The recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is consistent with the insertion loss TP0 to TP2 or TP3 to TP5 given in 92.8.3.6 and an assumed mated connector loss of 1.69 dB.

$$IL_{\mathrm{PCB}}(f) \le IL_{\mathrm{PCBmax}}(f) \;=\; 0.5(0.0694 + 0.4248\sqrt{f} + 0.9322f) \quad \text{(dB)} \qquad \text{(92A–1)}$$

for 0.01 GHz $\le f \le$ 19 GHz.

where

f	is the frequency in GHz
$IL_{\mathrm{PCB}}(f)$	is the insertion loss for the transmitter and receiver PCB
$IL_{\mathrm{PCBmax}}(f)$	is the recommended maximum insertion loss for the transmitter and receiver PCB

The minimum insertion loss allocation for the transmitter and receiver differential controlled impedance printed circuit boards for each differential lane (i.e., the minimum value of the sum of the insertion losses from TP0 to MDI receptacle or TP5 to MDI receptacle) is determined using Equation (92A–2) and illustrated in Figure 92A–1.

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$$IL_{PCB}(f) \geq IL_{PCBmin}(f) = 0.086(0.0694 + 0.4248\sqrt{f} + 0.9322f) \quad \text{(dB)} \qquad \text{(92A–2)}$$

for 0.01 GHz ≤ f ≤ 19 GHz.

where

f	is the frequency in GHz
$IL_{PCB}(f)$	is the insertion loss for the transmitter and receiver PCB
$IL_{PCBmin}(f)$	is the minimum insertion loss for the transmitter and receiver PCB

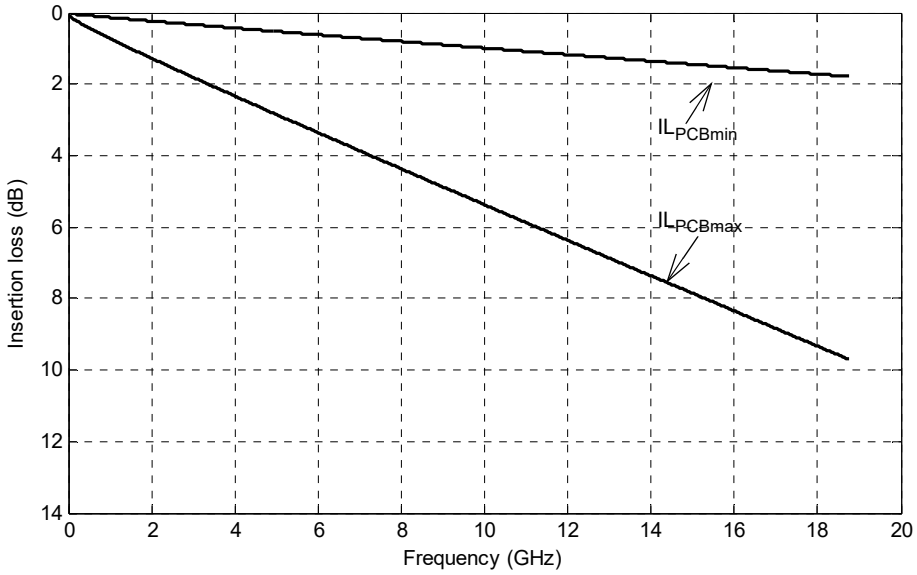

Figure 92A–1—Insertion Loss Tx or Rx PCB max and min

92A.5 Channel insertion loss

This subclause provides information on channel insertion losses for intended topologies ranging from 0.5 m to 5 m in length. The maximum channel insertion loss associated with the 5 m topology is determined using Equation (92A–3). The channel insertion loss associated with the 0.5 m topology and a maximum host channel is determined by Equation (92A–5). The channel insertion loss budget at 12.8906 GHz for the 5 m topology is illustrated in Figure 92A–2.

The maximum channel insertion loss for the 5 m topology is determined using Equation (92A–3). The maximum channel insertion loss is 35 dB at 12.8906 GHz.

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$$IL_{\text{Chmax35dB}}(f) = IL_{\text{Camax5m}}(f) + 2IL_{\text{Host}}(f) - 2IL_{\text{MatedTF}}(f) \quad \text{(dB)} \tag{92A–3}$$

for 0.05 GHz ≤ f ≤ 19 GHz.

where

f	is the frequency in GHz
$IL_{\text{Chmax35dB}}(f)$	is the maximum channel insertion loss between TP0 and TP5 representative of a 5 m cable assembly and a maximum host channel
$IL_{\text{Camax5m}}(f)$	is the maximum 5 m cable assembly insertion loss.
$IL_{\text{Host}}(f)$	is the maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (92–8)
$IL_{\text{MatedTF}}(f)$	is the nominal insertion loss of the mated test fixture using Equation (92A–4)

The nominal insertion loss of the mated test fixture is determined using Equation (92A–4).

$$IL_{\text{MatedTF}}(f) = 0.1148\sqrt{f} + 0.287f \quad \text{(dB)} \tag{92A–4}$$

for 0.01 GHz ≤ f ≤ 25 GHz.

where

f	is the frequency in GHz
$IL_{\text{MatedTF}}(f)$	is the nominal insertion loss of the mated test fixture.

The channel insertion loss between TP0 and TP5 representative of a 0.5 m cable assembly and a maximum host channel is determined using Equation (92A–5).

$$IL_{\text{Ch0.5m}}(f) = IL_{\text{Camin0.5m}}(f) + 2IL_{\text{Host}}(f) - 2IL_{\text{MatedTF}}(f) \quad \text{(dB)} \tag{92A–5}$$

for 0.05 GHz ≤ f ≤ 19 GHz.

where

f	is the frequency in GHz
$IL_{\text{Ch0.5m}}(f)$	is the channel insertion loss between TP0 and TP5 representative of a 0.5 m cable assembly and a maximum host channel
$IL_{\text{Camin0.5m}}(f)$	is the minimum 0.5 m cable assembly insertion loss given in Equation (92–26) and illustrated in Figure 92–12.
$IL_{\text{Host}}(f)$	is the maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (92–8)
$IL_{\text{MatedTF}}(f)$	is the nominal insertion loss of the mated test fixture using Equation (92A–4)

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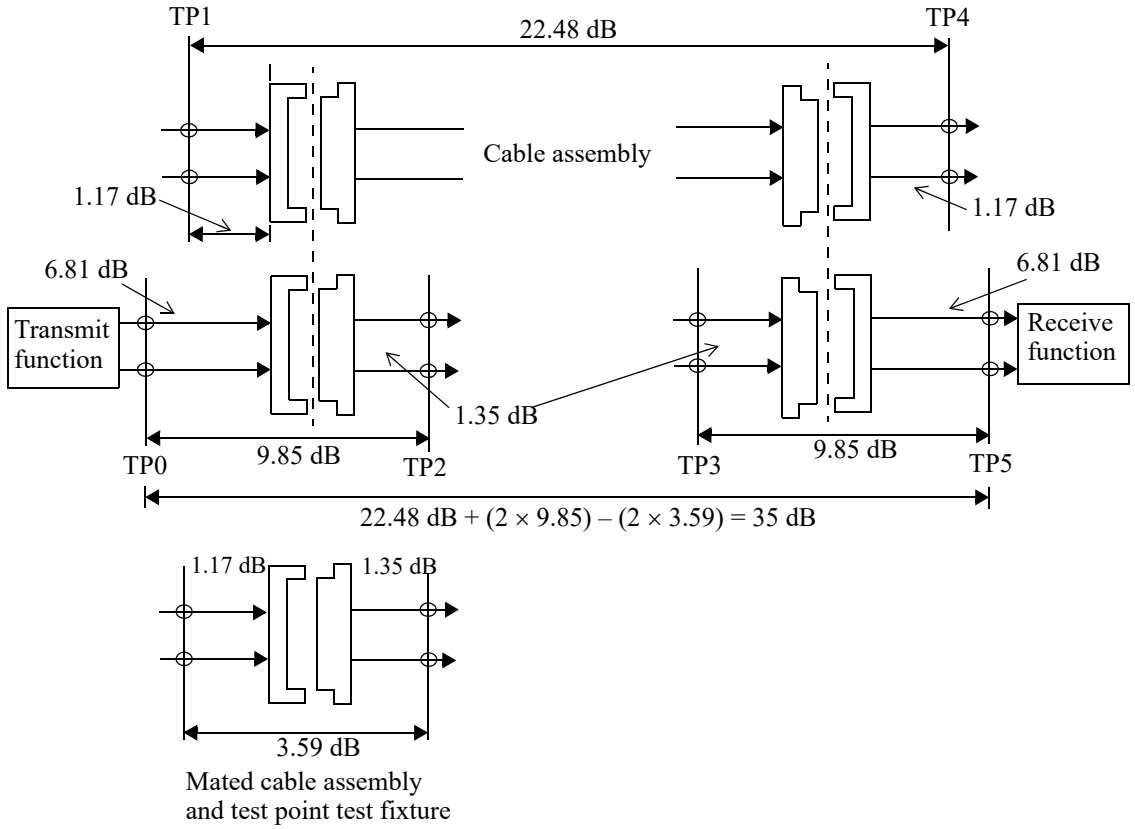

NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Figure 92A–2—35 dB channel insertion loss budget at 12.8906 GHz

92A.6 Channel return loss

The return loss of each lane of the 100GBASE-CR4 channel is recommended to meet the values determined using Equation (92–27).

92A.7 Channel Operating Margin (COM)

The Channel Operating Margin (COM) for the channel between TP0 and TP5, computed using the procedure in 93A.1 and the parameters in Table 93–8, is recommended to be greater than or equal to 3 dB.

NOTE—For cable lengths greater than 4 m, a frequency step (Δf) no larger than 5 MHz is recommended.

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Annex 93A

(normative)

Specification methods for electrical channels

93A.1 Channel Operating Margin

The Channel Operating Margin (COM) is a figure of merit for a channel derived from a measurement of its scattering parameters. COM is related to the ratio of a calculated signal amplitude to a calculated noise amplitude as defined by Equation (93A–1).

$$COM = 20\log_{10}(A_s/A_{ni}) \quad (93A–1)$$

COM shall be calculated using the method described in this annex. The signal amplitude A_s is defined in 93A.1.6 and the noise amplitude A_{ni} is defined in 93A.1.7.

Figure 93A–1 illustrates the reference model that is the basis for the calculation for COM. The parameters used to calculate COM are listed in Table 93A–1. The values assigned to these parameters are defined by the Physical Layer specification that invokes the method (see Table 93A–2).

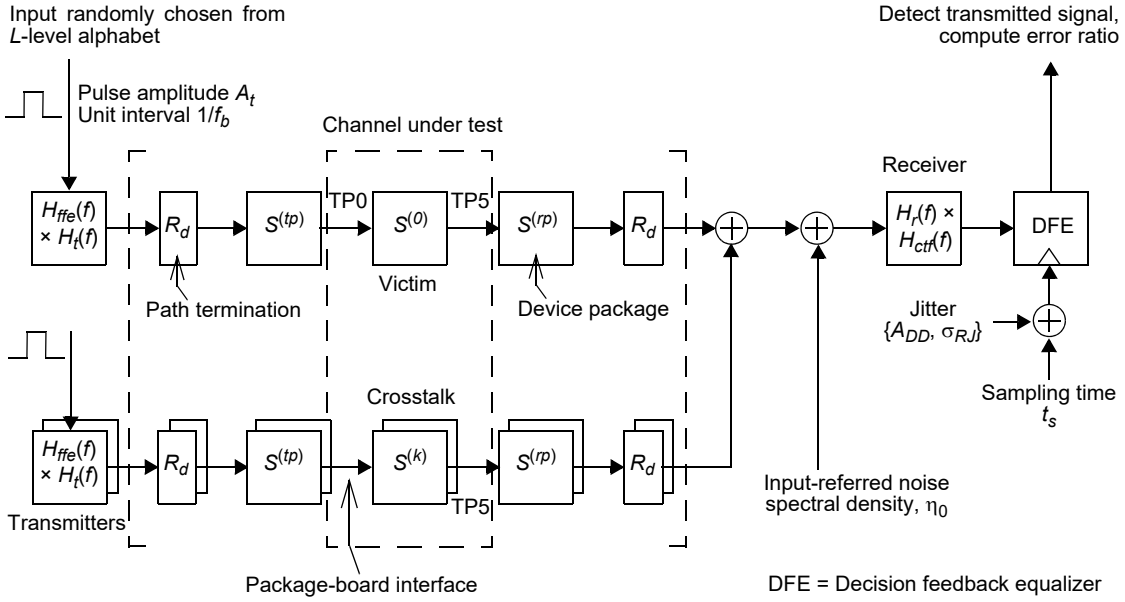

Figure 93A–1—COM reference model

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Table 93A–1—COM parameters

Parameter	Reference	Symbol	Units
Signaling rate	93A.1.1	f_b	GBd
Maximum start frequency	93A.1.1	$f_{\min}$	GHz
Maximum frequency step	93A.1.1	Δf	GHz
Device package model Single-ended device capacitance Transmission line length Single-ended package capacitance at package-to-board interface Transmission line characteristic impedance[a]	93A.1.2	 C_d z_p C_p Z_c	 nF mm nF Ω
Single-ended reference resistance	93A.1.2	R_0	Ω
Single-ended termination resistance	93A.1.3	R_d	Ω
Receiver 3 dB bandwidth	93A.1.4.1	f_r	GHz
Transmitter equalizer, minimum cursor coefficient	93A.1.4.2	$c(0)$	—
Transmitter equalizer, 2nd pre-cursor coefficient[b] Minimum value Maximum value Step size	93A.1.4.2	$c(-2)$	 — — —
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	93A.1.4.2	$c(-1)$	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	93A.1.4.2	$c(1)$	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	93A.1.4.3	g_{DC}	 dB dB dB
Continuous time filter, DC gain 2[c] Minimum value Maximum value Step size	93A.1.4.3	g_{DC2}	 dB dB dB
Continuous time filter, zero frequency for $g_{DC} = 0$	93A.1.4.3	f_z	GHz
Continuous time filter, pole frequencies	93A.1.4.3	f_{p1} f_{p2}	GHz
Continuous time filter, low frequency pole/zero[d]	93A.1.4.3	f_{LF}	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	93A.1.5	 A_v A_{fe} A_{ne}	 V V V
Number of signal levels	93A.1.6	L	—
Level separation mismatch ratio	93A.1.6	R_{LM}	—
Transmitter signal-to-noise ratio	93A.1.6	SNR_{TX}	dB

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Table 93A–1—COM parameters *(continued)*

Parameter	Reference	Symbol	Units
Number of samples per unit interval	93A.1.6	M	—
Decision feedback equalizer (DFE) length	93A.1.6	N_b	UI
Normalized DFE coefficient magnitude limit	93A.1.6	$b_{\max}(n)$	—
Random jitter, RMS	93A.1.6	σ_{RJ}	UI
Dual-Dirac jitter, peak	93A.1.6	A_{DD}	UI
One-sided noise spectral density	93A.1.6	η_0	V^2/GHz
Target detector error ratio	93A.1.7	DER_0	—

[a]Some clauses that invoke this method do not provide a value for Z_c. See 93A.1.2.
[b]Some clauses that invoke this method do not provide a value for $c(-2)$. See 93A.1.6.
[c]Some clauses that invoke this method do not provide a value for g_{DC2}. See 93A.1.4.3.
[d]Some clauses that invoke this method do not provide a value for f_{LF}. See 93A.1.4.3.

Table 93A–2—Physical Layer specifications that employ COM

Physical Layer	Parameter values
25GBASE-CR (Clause 110)	Table 110–11
25GBASE-CR-S (Clause 110)	Table 110–11
25GBASE-KR (Clause 111)	Table 111–8
25GBASE-KR-S (Clause 111)	Table 111–8
25GAUI C2C (Annex 109A)	Table 83D–6
50GBASE-CR (Clause 136)	Table 136–18
50GBASE-KR (Clause 137)	Table 137–6
LAUI-2 C2C (Annex 135B)	Table 83D–6
50GAUI-2 C2C (Annex 135D)	Table 83D–6
50GAUI-1 C2C (Annex 135F)	Table 120D–8
100GBASE-CR4 (Clause 92)	Table 93–8
100GBASE-CR2 (Clause 136)	Table 136–18
100GBASE-KR4 (Clause 93)	Table 93–8
100GBASE-KP4 (Clause 94)	Table 94–17
100GBASE-KR2 (Clause 137)	Table 137–6
CAUI-4 C2C (Annex 83D)	Table 83D–6
100GAUI-4 C2C (Annex 135D)	Table 83D–6
100GAUI-2 C2C (Annex 135F)	Table 120D–8
200GBASE-CR4 (Clause 136)	Table 136–18
200GBASE-KR4 (Clause 137)	Table 137–6

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Table 93A–2—Physical Layer specifications that employ COM

Physical Layer	Parameter values
200GAUI-8 (Annex 120B)	Table 83D–6[a]
200GAUI-4 (Annex 120D)	Table 120D–8
400GAUI-16 (Annex 120B)	Table 83D–6[a]
400GAUI-8 (Annex 120D)	Table 120D–8

[a]With the exceptions given in 120B.4.

93A.1.1 Measurement of the channel

The channel consists of a victim signal path plus some number of far-end and near-end crosstalk paths. The total number of paths for a given channel is denoted as K and, by convention, the path index k=0 corresponds to the victim path. The number of crosstalk paths is a function of the structure of the system. All significant contributors to the channel crosstalk should be included in the calculation of COM.

Each signal path is represented by a set of frequency-dependent scattering parameters. For the purpose of the calculation of COM, references to scattering parameters correspond to the differential-mode scattering parameters. The scattering parameters measured at frequency f are presented as the 2 x 2 matrix $S(f)$ as defined by Equation (93A–2).

$$S(f) = \begin{bmatrix} s_{11}(f) & s_{12}(f) \\ s_{21}(f) & s_{22}(f) \end{bmatrix} \quad \text{(93A–2)}$$

The relationship between $S(f)$ and other commonly cited characteristics is as follows. The insertion loss is the magnitude in dB of either $1/s_{12}(f)$ or $1/s_{21}(f)$. The input and output return loss are the magnitude in dB of $1/s_{11}(f)$ and $1/s_{22}(f)$, respectively.

The scattering parameters for the victim signal path are measured from TP0 to TP5. The scattering parameters for each crosstalk path are measured from the package-to-board interface of the aggressor transmitter to TP5. The frequency-dependent scattering matrix for signal path k is denoted as $S^{(k)}(f)$. The reference impedance for scattering parameter measurements is 100 Ω.

It is recommended that the scattering parameters be measured with uniform frequency step no larger than Δf from a start frequency no larger than $f_{\min}$ to a stop frequency of at least the signaling rate f_b.

93A.1.2 Transmitter and receiver device package models

Each signal path in the channel is augmented to reflect the likely influence of transmitter and receiver device packages. The device package models are two-port networks defined by their scattering parameters. The scattering parameters are calculated using the method defined in 93A.1.2.1 through 93A.1.2.4.

Each signal path in the channel is represented by the scattering matrix $S^{(k)}$. The augmented signal path is denoted as $S_p^{(k)}$ and is defined by Equation (93A–3).

$$S_p^{(k)} = \text{cascade}(\text{cascade}(S^{(tp)}, S^{(k)}), S^{(rp)}) \quad \text{(93A–3)}$$

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The function cascade() is defined in 93A.1.2.1. $S^{(tp)}$ and $S^{(rp)}$ are defined in 93A.1.2.4. If k corresponds to a near-end crosstalk path, $S^{(tp)}$ is calculated with the smallest value of z_p specified by the clause that invokes this method.

93A.1.2.1 Cascade connection of two-port networks

The connection of a pair of two-port networks x and y such that port 2 of network x is connected to port 1 of network y may be represented by an equivalent two-port network z. Port 1 of network z corresponds to port 1 of network x and port 2 network z corresponds to port 2 of network y. The scattering parameters of network z are given in terms of the scattering parameters of networks x and y by Equation (93A–4) through Equation (93A–7).

$$s_{11}^{(z)} = s_{11}^{(x)} + \frac{s_{21}^{(x)} s_{11}^{(y)} s_{12}^{(x)}}{1 - s_{22}^{(x)} s_{11}^{(y)}} \tag{93A–4}$$

$$s_{12}^{(z)} = \frac{s_{12}^{(x)} s_{12}^{(y)}}{1 - s_{22}^{(x)} s_{11}^{(y)}} \tag{93A–5}$$

$$s_{21}^{(z)} = \frac{s_{21}^{(x)} s_{21}^{(y)}}{1 - s_{22}^{(x)} s_{11}^{(y)}} \tag{93A–6}$$

$$s_{22}^{(z)} = s_{22}^{(y)} + \frac{s_{12}^{(y)} s_{22}^{(x)} s_{21}^{(y)}}{1 - s_{22}^{(x)} s_{11}^{(y)}} \tag{93A–7}$$

For the purpose of this annex, this set of operations is referred to using the shorthand notation $S^{(z)} = \text{cascade}(S^{(x)}, S^{(y)})$.

93A.1.2.2 Two-port network for a shunt capacitance

The scattering parameters for a shunt capacitance with value C are defined by Equation (93A–8) where $j = \sqrt{-1}$ and $\omega = 2\pi f$.

$$S(C) = \frac{1}{2 + j\omega C R_0} \begin{bmatrix} -j\omega C R_0 & 2 \\ 2 & -j\omega C R_0 \end{bmatrix} \tag{93A–8}$$

The scattering parameters for the device capacitance C_d are denoted as $S^{(d)} = S(C_d)$ and the scattering parameters for the board capacitance C_p are denoted as $S^{(p)} = S(C_p)$.

93A.1.2.3 Two-port network for the package transmission line

The scattering parameters for the package transmission line model are a function of the complex propagation coefficient defined by Equation (93A–9), Equation (93A–10), and Equation (93A–11) and the reflection coefficient defined by Equation (93A–12). The values of the parameters that appear in these equations are defined in Table 93A–3. Where a value for Z_c is not provided by the clause that invokes this method, it takes the value 78.2 Ω. The units of f are GHz.

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$$\gamma(f) = \left\{ \begin{array}{cc} \gamma_0 & f = 0 \\ \gamma_0 + \gamma_1\sqrt{f} + \gamma_2(f)f & f > 0 \end{array} \right\} \quad \text{(93A–9)}$$

$$\gamma_1 = a_1(1 + j) \quad \text{(93A–10)}$$

$$\gamma_2(f) = a_2(1 - j(2/\pi)\log_e(f/1\ \text{GHz})) + j2\pi\tau \quad \text{(93A–11)}$$

$$\rho = \frac{Z_c - 2R_0}{Z_c + 2R_0} \quad \text{(93A–12)}$$

Table 93A–3—Transmission line model parameters and values

Parameter	Value	Units
γ_0	0	1/mm
a_1	1.734×10^{-3}	$ns^{1/2}$/mm
a_2	1.455×10^{-4}	ns/mm
τ	6.141×10^{-3}	ns/mm

The scattering parameters for a package transmission line of length z_p are defined by Equation (93A–13) and Equation (93A–14). The units of z_p are mm.

$$s_{11}^{(l)}(f) = s_{22}^{(l)}(f) = \frac{\rho(1 - \exp(-\gamma(f)2z_p))}{1 - \rho^2\exp(-\gamma(f)2z_p)} \quad \text{(93A–13)}$$

$$s_{21}^{(l)}(f) = s_{12}^{(l)}(f) = \frac{(1 - \rho^2)\exp(-\gamma(f)z_p)}{1 - \rho^2\exp(-\gamma(f)2z_p)} \quad \text{(93A–14)}$$

The transmission line scattering parameter matrix is then denoted as $S^{(l)}$.

93A.1.2.4 Assembly of transmitter and receiver device package models

The scattering parameters for the transmitter device package model $S^{(tp)}$ are the result of the cascade connection of the device capacitance, package transmission line, and board capacitance as defined by Equation (93A–15).

$$S^{(tp)} = \text{cascade}(\text{cascade}(S^{(d)}, S^{(l)}), S^{(p)}) \quad \text{(93A–15)}$$

Similarly, the scattering parameters for the receiver device package model $S^{(rp)}$ are the result of the cascade connection of the board capacitance, package transmission line, and device capacitance as defined by Equation (93A–16).

$$S^{(rp)} = \text{cascade}(\text{cascade}(S^{(p)}, S^{(l)}), S^{(d)}) \quad \text{(93A–16)}$$

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93A.1.3 Path terminations

The input to each signal path is terminated by an impedance defined by the reflection coefficient Γ_1. The output of each signal path is terminated by an impedance defined by the reflection coefficient Γ_2.

The reflection coefficients Γ_1 and Γ_2 are defined by Equation (93A–17).

$$\Gamma_1 = \Gamma_2 = \frac{R_d - R_0}{R_d + R_0} \tag{93A–17}$$

The voltage transfer function of the terminated signal path is defined by Equation (93A–18) where $\Delta S(f) = s_{11}(f)s_{22}(f) - s_{12}(f)s_{21}(f)$.

$$H_{21}(f) = \frac{s_{21}(f)(1-\Gamma_1)(1+\Gamma_2)}{1 - s_{11}(f)\Gamma_1 - s_{22}(f)\Gamma_2 + \Gamma_1\Gamma_2\Delta S(f)} \tag{93A–18}$$

The voltage transfer function for the signal path represented by $S_p^{(k)}(f)$ is denoted $H_{21}^{(k)}(f)$.

93A.1.4 Filters

The voltage transfer function for each signal path $H_{21}^{(k)}(f)$ (see 93A.1.3) is multiplied by a set of filter transfer functions to yield $H^{(k)}(f)$ as shown in Equation (93A–19).

$$H^{(k)}(f) = H_{ffe}(f)H_t(f)H_{21}^{(k)}(f)H_r(f)H_{ctf}(f) \tag{93A–19}$$

The receiver noise filter $H_r(f)$ is defined in 93A.1.4.1, the transmitter transition time filter $H_t(f)$ is defined by Equation (93A–46) where T_r is 0 unless defined otherwise for the Physical Layer specification that invokes this method, the transmitter equalizer $H_{ffe}(f)$ is defined in 93A.1.4.2, and the receiver equalizer $H_{ctf}(f)$ is defined in 93A.1.4.3.

The filtered voltage transfer function $H^{(k)}(f)$ is used to compute the pulse response (see 93A.1.5).

93A.1.4.1 Receiver noise filter

$H_r(f)$ is a noise filter defined by Equation (93A–20).

$$H_r(f) = \frac{1}{1 - 3.414214(f/f_r)^2 + (f/f_r)^4 + j2.613126(f/f_r - (f/f_r)^3)} \tag{93A–20}$$

93A.1.4.2 Transmitter equalizer

$H_{ffe}(f)$ is defined by Equation (93A–21) and is intended to represent the transmitter equalizer. If k corresponds to a near-end crosstalk path, then $c(-2)$, $c(-1)$, and $c(1)$ are all zero regardless of the values used for the other paths. The value of the "cursor" coefficient $c(0)$ is set to $1 - |c(-2)| - |c(-1)| - |c(1)|$ for any value of $c(-2)$, $c(-1)$, and $c(1)$. If the value of $c(0)$ is less than the specified minimum value, the corresponding combination of $c(-2)$, $c(-1)$, and $c(1)$ is considered invalid and is not used to calculate COM.

$$H_{ffe}(f) = \sum_{i=-2}^{1} c(i)\exp\left(-j2\pi(i+2)\frac{f}{f_b}\right) \tag{93A–21}$$

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93A.1.4.3 Receiver equalizer

$H_{ctf}(f)$ is defined by Equation (93A–22). Where values for g_{DC2} and f_{LF} are not provided by the clause that invokes this method, g_{DC2} takes the value 0 and f_{LF} takes the value 1.

$$H_{ctf}(f) = \frac{\left(10^{\frac{g_{DC}}{20}} + j\frac{f}{f_z}\right)\left(10^{\frac{g_{DC2}}{20}} + j\frac{f}{f_{LF}}\right)}{\left(1 + j\frac{f}{f_{p1}}\right)\left(1 + j\frac{f}{f_{p2}}\right)\left(1 + j\frac{f}{f_{LF}}\right)} \quad (93A–22)$$

93A.1.5 Pulse response

The pulse response of a signal path is defined to be the output of the path following the application of a rectangular pulse one unit interval in duration at its input. First define the function $X(f)$ per Equation (93A–23) where $\mathrm{sinc}(x) = \sin(\pi x)/(\pi x)$ and $T_b = 1/f_b$ is the unit interval.

$$X(f) = A_t T_b \mathrm{sinc}(fT_b) \quad (93A–23)$$

$X(f)$ is a function of A_t, which in turn is based on the path index k. If k=0, i.e., the victim path, then $A_t = A_v$. If k corresponds to a far-end crosstalk path, then $A_t = A_{fe}$. If k corresponds to a near-end crosstalk path, then $A_t = A_{ne}$.

The pulse response $h^{(k)}(t)$ is derived from the voltage transfer function $H^{(k)}(f)$ (see 93A.1.4) using Equation (93A–24).

$$h^{(k)}(t) = \int_{-\infty}^{\infty} X(f)H^{(k)}(f)\exp(j2\pi ft)df \quad (93A–24)$$

NOTE 1—COM is expected to be computed from measurements at discrete frequencies that cover a limited span (see 93A.1.1). The inverse Fourier transform depicted in Equation (93A–24) is likely to be implemented as a discrete Fourier transform and the filtered voltage transfer function may need to be extrapolated (both to DC and to one half of the sampling frequency) for this computation. The extrapolation method and sampling frequency should be chosen carefully to limit the error in the COM computation.

NOTE 2—The time span of the pulse response in unit intervals, N, is limited in practice by frequency step Δf ($N = f_b/\Delta f$) but in general should be set to include all significant components of the pulse response.

93A.1.6 Determination of variable equalizer parameters

COM is a function of the variables $c(-2)$, $c(-1)$, $c(1)$, g_{DC}, and g_{DC2}. The following procedure is used to determine the values of these variables that are used to calculate COM.

a) Compute the pulse response $h^{(k)}(t)$ of each signal path k for a given $c(-2)$, $c(-1)$, $c(1)$, g_{DC}, and g_{DC2} using the procedure defined in 93A.1.5.
b) Define t_s to be the time that satisfies Equation (93A–25). If there are multiple values of t_s that satisfy the equation, then the first value prior to the peak of $h^{(0)}(t)$ is selected. The coefficients of the decision feedback equalizer $b(n)$ are computed as shown in Equation (93A–26). If N_b is 0, then the $b(n)$ is considered to be zero for all n.
c) Define A_s to be $R_{LM}h^{(0)}(t_s)/(L–1)$.
d) Compute σ_{TX}^2 per Equation (93A–30) and Equation (93A–29). This represents the noise output from the transmitter.

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e) Compute $h_{ISI}(n)$ per Equation (93A–27). This represents the residual intersymbol interference (ISI) after decision feedback equalization. The corresponding ISI amplitude variance σ_{ISI}^2 is computed per Equation (93A–31) and Equation (93A–29).

f) Compute the slope of the pulse response of the victim path $h_J(n)$ as shown in Equation (93A–28). The variance of the amplitude error due to timing jitter σ_J^2 is computed per Equation (93A–32) and Equation (93A–29).

g) The variance of the amplitude for path k is given by Equation (93A–33) where the phase index m can assume any integer value from 0 to M–1. Denote the value of m that maximizes the variance for path k as i. The variance of the amplitude for the combination of all crosstalk paths σ_{XT}^2 is then computed using Equation (93A–34), which is the sum of the maximum variances for the individual paths k=1 to K–1.

h) Compute the variance of the noise at the output of the receive equalizer σ_N^2 based on the one-sided spectral density η_0 referred to the receiver noise filter input per Equation (93A–35).

i) Compute the figure of merit (FOM) per Equation (93A–36).

$$h^{(0)}(t_s - T_b) = h^{(0)}(t_s + T_b) - h^{(0)}(t_s)b(1) \tag{93A–25}$$

$$b(n) = \begin{Bmatrix} -b_{\max}(n) & h^{(0)}(t_s + nT_b)/h^{(0)}(t_s) < -b_{\max}(n) \\ b_{\max}(n) & h^{(0)}(t_s + nT_b)/h^{(0)}(t_s) > b_{\max}(n) \\ h^{(0)}(t_s + nT_b)/h^{(0)}(t_s) & \text{otherwise} \end{Bmatrix} \tag{93A–26}$$

$$h_{ISI}(n) = \begin{Bmatrix} 0 & n = 0 \\ h^{(0)}(t_s + nT_b) - h^{(0)}(t_s)b(n) & 1 \le n \le N_b \\ h^{(0)}(t_s + nT_b) & \text{otherwise} \end{Bmatrix} \tag{93A–27}$$

$$h_J(n) = \frac{h^{(0)}(t_s + (n + 1/M)T_b) - h^{(0)}(t_s + (n - 1/M)T_b)}{2/M} \tag{93A–28}$$

$$\sigma_X^2 = \frac{L^2 - 1}{3(L - 1)^2} \tag{93A–29}$$

$$\sigma_{TX}^2 = [h^{(0)}(t_s)]^2 10^{-SNR_{TX}/10} \tag{93A–30}$$

$$\sigma_{ISI}^2 = \sigma_X^2 \sum_n h_{ISI}^2(n) \tag{93A–31}$$

$$\sigma_J^2 = (A_{DD}^2 + \sigma_{RJ}^2)\sigma_X^2 \sum_n h_J^2(n) \tag{93A–32}$$

$$[\sigma_m^{(k)}]^2 = \sigma_X^2 \sum_n [h^{(k)}((m/M + n)T_b)]^2 \tag{93A–33}$$

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$$\sigma_{XT}^2 = \sum_{k=1}^{K-1} [\sigma_i^{(k)}]^2 \quad (93A–34)$$

$$\sigma_N^2 = \eta_0 \int_0^\infty \left| H_r(f) H_{ctf}(f) \right|^2 df \quad (93A–35)$$

$$FOM = 10\log_{10}\left(\frac{A_s^2}{\sigma_{TX}^2 + \sigma_{ISI}^2 + \sigma_J^2 + \sigma_{XT}^2 + \sigma_N^2} \right) \quad (93A–36)$$

The FOM is calculated for each permitted combination of $c(-2)$, $c(-1)$, $c(1)$, g_{DC}, and g_{DC2} values per Table 93A–1, where any parameters not provided by the clause that invokes this method are set to 0. The combination of values that maximizes the FOM, including the corresponding value of t_s, is used for the calculation of the interference and noise amplitude in 93A.1.7 and the calculation of COM in 93A.1.

93A.1.7 Interference and noise amplitude

Given the values of $c(-1)$, $c(1)$, g_{DC}, g_{DC2}, and t_s derived in 93A.1.6, compute the combined interference and noise distribution $p(y)$ per 93A.1.7.3. The corresponding cumulative distribution function is $P(y)$ as defined by Equation (93A–37).

$$P(y) = \int_{-\infty}^{y} p(y) dy \quad (93A–37)$$

The noise amplitude, A_{ni}, is the magnitude of the value of y_0 that satisfies the relationship $P(y_0) = DER_0$ where DER_0 is the target detector error ratio. The detector error ratio is the probability that the detector fails to identify the signal level that was transmitted.

In 93A.1.7.1 through 93A.1.7.3, "*" denotes convolution, which is defined by Equation (93A–38).

$$f(t) * g(t) = \int_{-\infty}^{\infty} f(\tau) g(t - \tau) d\tau \quad (93A–38)$$

93A.1.7.1 Interference amplitude distribution

The interference amplitude distribution is computed from the sampled pulse response $h(n)$ with the assumption that the transmitted symbols are independent, identically distributed random variables and that the symbols are uniformly distributed across the set of L possible values. For the purpose of this subclause, $h(n)$ is a general notation that corresponds to $A_{DD}h_f(n)$ (see 93A.1.7.2), $h_{ISI}(n)$, or $h^{(k)}((i / M + n)T_b)$ (see 93A.1.7.3).

Equation (93A–39) defines the nth component of the interference amplitude distribution function where $\delta(y)$ is the Dirac delta function.

$$p_n(y) = \frac{1}{L} \sum_{l=0}^{L-1} \delta\left(y - \left(\frac{2l}{L-1} - 1 \right) h(n) \right) \quad (93A–39)$$

The set of N such components are combined via convolution to obtain the complete interference amplitude distribution. Initialize $p(y)$ to $\delta(y)$ and then evaluate Equation (93A–40) sequentially for n=0 to N–1.

$$p(y) = p(y) * p_n(y) \quad (93A–40)$$

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NOTE 1—COM is expected to be numerically computed using a quantized amplitude axis y. The amplitude step Δy introduces quantization error in the calculated distribution function that is compounded by subsequent convolutions with other quantized distribution functions. It is recommended that Δy be no larger than 0.1% of A_s or 0.01 mV, whichever is smaller.

NOTE 2—It is recommended that components of the pulse response whose amplitude is less than 0.1% of A_s be ignored as they likely correspond to measurement noise or numerical artifacts.

93A.1.7.2 Noise amplitude distribution

The calculation of COM includes two noise terms that are described in terms of their distribution function. The first term has a Gaussian amplitude distribution function with zero mean and variance σ_G^2. The variance is defined by Equation (93A–41) where $H_r(f)$ is defined in 93A.1.4.1, $H_{ctf}(f)$ is defined in 93A.1.4.3, and σ_X^2 and $h_J(n)$ are defined in 93A.1.6.

$$\sigma_G^2 = \sigma_{TX}^2 + \sigma_{RJ}^2\sigma_X^2\sum_n h_J^2(n) + \eta_0\int_0^\infty \left|H_r(f)H_{ctf}(f)\right|^2 df \tag{93A–41}$$

The amplitude distribution of the Gaussian noise term is defined by Equation (93A–42).

$$p_G(y) = \frac{\exp(-y^2/(2\sigma_G^2))}{\sqrt{2\pi\sigma_G^2}} \tag{93A–42}$$

The second term is denoted as p_{DD} and is related to the amplitude noise resulting from dual-Dirac jitter. It is computed using the procedure defined in 93A.1.7.1 with $h(n) = A_{DD}h_J(n)$.

The components are combined using convolution to yield the overall noise amplitude distribution function as defined in Equation (93A–43).

$$p_n(y) = p_G(y) * p_{DD}(y) \tag{93A–43}$$

93A.1.7.3 Combination of interference and noise distributions

Compute the intersymbol interference amplitude distribution using the procedure defined in 93A.1.7.1 with $h(n) = h_{ISI}(n)$ as defined by Equation (93A–27) and denote the result as $p(y)$.

The contributions of the K–1 crosstalk paths to the total interference are included as follows. Determine the phase index $m = i$ that maximizes the variance of the amplitude for path k as defined by Equation (93A–33). Compute the interference amplitude distribution using the procedure defined in 93A.1.7.1 with $h(n) = h^{(k)}((i / M + n)T_b)$ and denote the result as $p^{(k)}(y)$.

Compute $p^{(k)}(y)$ and evaluate Equation (93A–44) sequentially for integer values k=1 to K–1.

$$p(y) = p(y) * p^{(k)}(y) \tag{93A–44}$$

The noise distribution $p_n(y)$ defined in 93A.1.7.2 is then included to yield the combined interference and noise amplitude distribution as shown in Equation (93A–45).

$$p(y) = p(y) * p_n(y) \tag{93A–45}$$

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93A.2 Test channel calibration using COM

A generalized block diagram of the interference tolerance test channel is shown in Figure 93A–2.

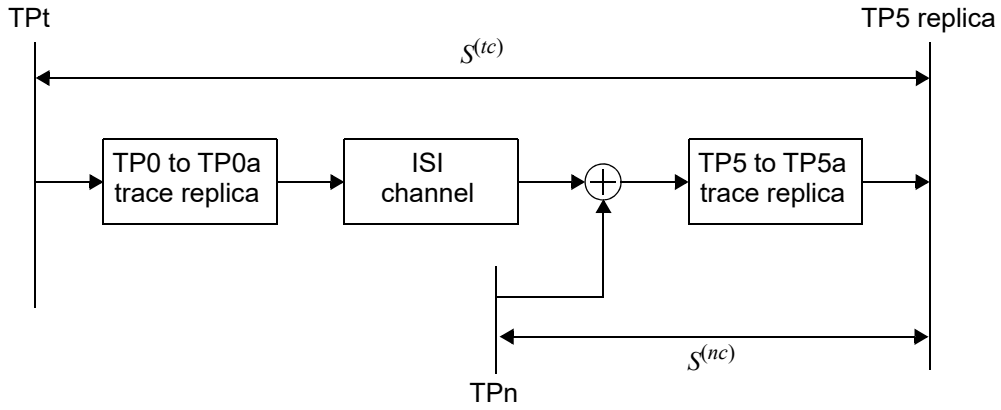

Figure 93A–2—Generalized interference tolerance test channel

The signal path from the test transmitter connected at TPt to the receiver under test connected at TP5 consists of replicas of the test fixture traces, a controlled ISI channel, and the means by which additive broadband noise is coupled into the path. This path is represented by the scattering parameters $S^{(tc)}$ measured from TPt to the TP5 replica. The signal path from the broadband noise source connected at TPn to the receiver consists of the means of broadband noise coupling and a replica of TP5 to TP5a test fixture trace. This path is represented by scattering parameters $S^{(nc)}$ measured from TPn to the TP5 replica.

COM is used to calibrate the interference tolerance test channel. The values assigned to the parameters listed in Table 93A–1 are defined by the Physical Layer specification that invokes this method.

The calculations defined in 93A.1 are evaluated for $S^{(tc)}$ with the following exceptions.

If the test transmitter presents a high-quality termination, e.g., it is a piece of test equipment, the transmitter device package model $S^{(tp)}$ is omitted from the calculation of $S_p^{(k)}$ and the filtered voltage transfer function $H^{(k)}(f)$ in 93A.1.4 includes the filter $H_t(f)$ defined by Equation (93A–46) where T_r is the 20% to 80% transition time in ns (see 86A.5.3.3) of the signal as measured at TP0a and f is frequency in GHz.

$$H_t(f) = \exp(-2(\pi f T_r / 1.6832)^2) \tag{93A–46}$$

The approximate voltage transfer function for the path from TPn to the output of the receiver equalizer is defined by Equation (93A–47).

$$H^{(ne)}(f) = s_{21}^{(nc)}(f)\, s_{21}^{(rp)}(f) H_r(f)\, H_{ctf}(f) \tag{93A–47}$$

The broadband noise source applies noise at TPn that has a Gaussian amplitude distribution with zero mean and standard deviation σ_{bn}. The power spectral density of the noise is flat from $-f_b / 2$ to $f_b / 2$ and is zero elsewhere. The standard deviation of the noise at the receiver equalizer output σ_{ne} is defined by Equation (93A–48).

$$\sigma_{ne}^2 = \frac{2\sigma_{bn}^2}{f_b} \int_0^{f_b/2} \left| H^{(ne)}(f) \right|^2 df \tag{93A–48}$$

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Equation (93A–41) defines the standard deviation of the Gaussian noise amplitude distribution function. When COM is used to calibrate the interference tolerance test channel, this definition is replaced by Equation (93A–49). The value of σ_{bn} is adjusted until the target COM value is achieved.

$$\sigma_G^2 = \sigma_{TX}^2 + \sigma_{RJ}^2\sigma_X^2\sum_n h_J^2(n) + \eta_0\int_0^\infty \left|H_r(f)H_{ctf}(f)\right|^2 df + \sigma_{ne}^2 \tag{93A–49}$$

An additional figure of merit for the test channel is the root-sum-square of the magnitude terms n_1 to n_2 of the equalized pulse response where n_2 is less than or equal to N_b. This measure of the relative usage of the decision feedback equalizer is defined by Equation (93A–50).

$$u_b(n_1, n_2) = \frac{1}{A_s}\sqrt{\sum_{n=n_1}^{n_2}\left(h^{(0)}(t_s + nT_b)\right)^2} \tag{93A–50}$$

The shorthand notation RSS_DFE4 is used to represent $u_b(4, N_b)$.

93A.3 Fitted insertion loss

The fitted insertion loss as a function of frequency is given by Equation (93A–51).

$$IL_{fitted}(f) = a_0 + a_1\sqrt{f} + a_2 f + a_4 f^2 \tag{93A–51}$$

Denote the insertion loss, in dB, measured at frequency f_n as $IL(f_n)$. Given the insertion loss measured at N uniformly-spaced frequencies from start frequency $f_{\min}$ to stop frequency $f_{\max}$ with step no larger than Δf, the coefficients for the fitted insertion loss shall be calculated as follows.

Define the weighted frequency matrix F using Equation (93A–52).

$$F = \begin{bmatrix} 10^{-IL(f_1)/20} & \sqrt{f_1}10^{-IL(f_1)/20} & f_1 10^{-IL(f_1)/20} & f_1^2 10^{-IL(f_1)/20} \\ 10^{-IL(f_2)/20} & \sqrt{f_2}10^{-IL(f_2)/20} & f_2 10^{-IL(f_2)/20} & f_2^2 10^{-IL(f_2)/20} \\ \cdots & \cdots & \cdots & \cdots \\ 10^{-IL(f_N)/20} & \sqrt{f_N}10^{-IL(f_N)/20} & f_N 10^{-IL(f_N)/20} & f_N^2 10^{-IL(f_N)/20} \end{bmatrix} \tag{93A–52}$$

Define the weighted insertion loss vector L using Equation (93A–53).

$$L = \begin{bmatrix} IL(f_1)10^{-IL(f_1)/20} \\ IL(f_2)10^{-IL(f_2)/20} \\ \cdots \\ IL(f_N)10^{-IL(f_N)/20} \end{bmatrix} \tag{93A–53}$$

The fitted insertion loss coefficients are then given by Equation (93A–54).

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$$\begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ a_4 \end{bmatrix} = (F^T F)^{-1} F^T L \quad \text{(93A–54)}$$

The values assigned to f_{min}, f_{max}, and Δf are defined by the Physical Layer specification that invokes this method.

93A.4 Insertion loss deviation

The insertion loss deviation $ILD(f)$ is the difference between the measured insertion loss $IL(f)$ and the fitted insertion loss $IL_{fitted}(f)$ (see 93A.3) as shown in Equation (93A–55).

$$ILD(f) = IL(f) - IL_{fitted}(f) \quad \text{(93A–55)}$$

A figure of merit for a channel that is based on $ILD(f)$ is given by Equation (93A–56). In Equation (93A–56), f_n are the frequencies considered in the computation of the fitted insertion loss and $W(f_n)$ is the weight at each frequency as defined by Equation (93A–57).

$$FOM_{ILD} = \left[\frac{1}{N}\sum_n W(f_n) ILD^2(f_n)\right]^{1/2} \quad \text{(93A–56)}$$

$$W(f_n) = \text{sinc}^2(f_n/f_b)\left[\frac{1}{1+(f_n/f_t)^4}\right]\left[\frac{1}{1+(f_n/f_r)^8}\right] \quad \text{(93A–57)}$$

The variable f_b is the signaling rate. The 3 dB transmit filter bandwidth f_t is inversely proportional to the 20% to 80% rise and fall time T_t. The constant of proportionality is 0.2365 (e.g., $T_t f_t = 0.2365$; with f_t in Hertz and T_t in seconds). The variable f_r is the 3 dB reference receiver bandwidth.

The values assigned to f_b, T_t, and f_r are defined by the Physical Layer specification that invokes this method.

93A.5 Effective Return Loss

Effective Return Loss (ERL) is a figure of merit for the electromagnetic wave reflection from a device or a channel input or output. ERL shall be calculated using the method described in this annex.

The parameters used to calculate ERL are listed in Table 93A–4. The values assigned to these parameters are defined by the Physical Layer specification that invokes the ERL method.

93A.5.1 Pulse time-domain reflection signal

ERL is derived from a unity pulse time-domain reflection signal, PTDR(t). PTDR(t) is defined at the test points defined in the Physical Layer specification that invokes the ERL method. PTDR(t) may be acquired directly from an appropriately filtered time domain reflectometer (TDR), or derived mathematically from measured differential scattering parameters $S(f)$ and transmitter and receiver filters, according to the procedure in this subclause. See 93A.1.1 for scattering parameters measurement recommendations including frequency step, start frequency, and stop frequency.

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Table 93A–4—ERL parameters

Parameter	Reference	Symbol	Units
Signaling rate	93A.1.1	f_b	GBd
Transition time associated with a pulse	93A.2	T_r	ns
Receiver 3 dB bandwidth	93A.1.4.1	f_r	GHz
Number of signal levels	93A.1.6	L	—
Length of the reflection signal		N	UI
Number of samples per unit interval	93A.1.6	M	—
Equalizer length associated with reflection signal	93A.5.2	N_{bx}	UI
Incremental available signal loss factor	93A.5.2	β_x	GHz
Permitted reflection from a transmission line external to the device under test	93A.5.2	ρ_x	—
Target detector error ratio	93A.1.7	DER_0	—

The filtered return loss, $H_{ii}(f)$, is defined by Equation (93A–58).

$$H_{ii}(f) = H_t(f)s_{ii}(f)H_r(f) \quad \text{(93A–58)}$$

where

f is the frequency in GHz
$H_r(f)$ is defined by Equation (93A–20)
$H_t(f)$ is defined by Equation (93A–46)
i is the port index of the scattering parameters, 1 or 2

The pulse TDR signal, PTDR(t), is defined by Equation (93A–59).

$$PTDR(t) = \int_{-\infty}^{\infty} X(f)H_{ii}(f)\exp(j2\pi ft)df \quad \text{(93A–59)}$$

where

t is the time in ns starting from the peak of the injected pulse
$X(f)$ is defined by Equation (93A–23) with A_t set to 1

93A.5.2 Effective reflection waveform

The effective reflection waveform, $R_{eff}(t)$, is computed by time gating and weighting the PTDR waveform, PTDR(t), according to Equation (93A–60). $R_{eff}(t)$ is a pure number.

$$R_{eff}(t) = PTDR(t) \times G_{rr}(t) \times G_{loss}(t) \quad \text{(93A–60)}$$

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where $G_{rr}(t)$ and $G_{loss}(t)$ are time gating weighting functions defined in Equation (93A–61) and Equation (93A–62) with t in nanoseconds.

$$G_{rr}(t) = \begin{cases} 0 & t < T_{fx} \\ \rho_x(1+\rho_x)\exp\left(-\dfrac{[(t-T_{fx})f_b-(N_{bx}+1)]^2}{(N_{bx}+1)^2}\right) & T_{fx} \le t < T_{fx}+\dfrac{N_{bx}+1}{f_b} \\ 1 & t \ge T_{fx}+\dfrac{N_{bx}+1}{f_b} \end{cases} \quad \text{(93A–61)}$$

where

t	is the time in ns starting from the peak of the injected pulse
T_{fx}	is twice the propagation delay in ns associated with the test fixture, obtained by measurement or inspection
ρ_x, f_b, N_{bx}	are supplied by the clause that invokes this method

$$G_{loss}(t) = \begin{cases} 0 & t < T_{fx} \\ 10^{\frac{\frac{\beta_x}{f_b}[(t-T_{fx})f_b-(N_{bx}+1)]}{20}} & T_{fx} \le t < T_{fx}+\dfrac{N_{bx}+1}{f_b} \\ 1 & t \ge T_{fx}+\dfrac{N_{bx}+1}{f_b} \end{cases} \quad \text{(93A–62)}$$

where

t	is the time in ns starting from the peak of the injected pulse
T_{fx}	is twice the propagation delay in ns associated with the test fixture, obtained by measurement or inspection
β_x, f_b, N_{bx}	are supplied by the clause that invokes this method

93A.5.3 Sampled effective reflection

The sampled effective reflection for each phase m is computed per Equation (93A–63).

$$h^{(m)}(n) = R_{eff}\left(T_{fx}+\frac{n+m/M}{f_b}\right) \quad \text{(93A–63)}$$

where

n	is an integer ranging from 0 to N–1
m	is an integer ranging from 0 to M–1
N and M	are supplied by the clause that invokes this method

The standard deviation of the distribution of the reflection signal for each phase m, $\sigma^{(m)}{}_h$, is defined by Equation (93A–64).

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$$\sigma^{(m)}{}_h = \sqrt{\sum_{n=1}^{N} h^{(m)}(n)^2} \quad \text{(93A–64)}$$

where

m is an integer ranging from 0 to *M*–1
N and *M* are supplied by the clause that invokes this method

93A.5.4 x-quantile of the reflection distribution

The reflection signal distribution $p(y)$ is computed from the sampled effective reflection using the procedure defined in 93A.1.7.1, with $h(n) = h^{(m)}(n)$, where m maximizes $\sigma^{(m)}{}_h$. The value of L in Equation (93A–39) is supplied by the clause that invokes this method. The corresponding cumulative distribution function $P(y)$ is calculated from $p(y)$ using Equation (93A–37).

The x-quantile of the distribution, $P^{-1}(x)$, is the value of y that satisfies the relationship $P(y)=x$.

93A.5.5 ERL

ERL is defined as $-20 \times \log_{10} P^{-1}(DER_0)$ where DER_0 is the target detector error ratio.

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Annex 93B

(informative)

Electrical backplane reference model

This annex describes additional informative test points that may used to partition the electrical backplane channel. See Figure 93B–1 and Table 93B–1

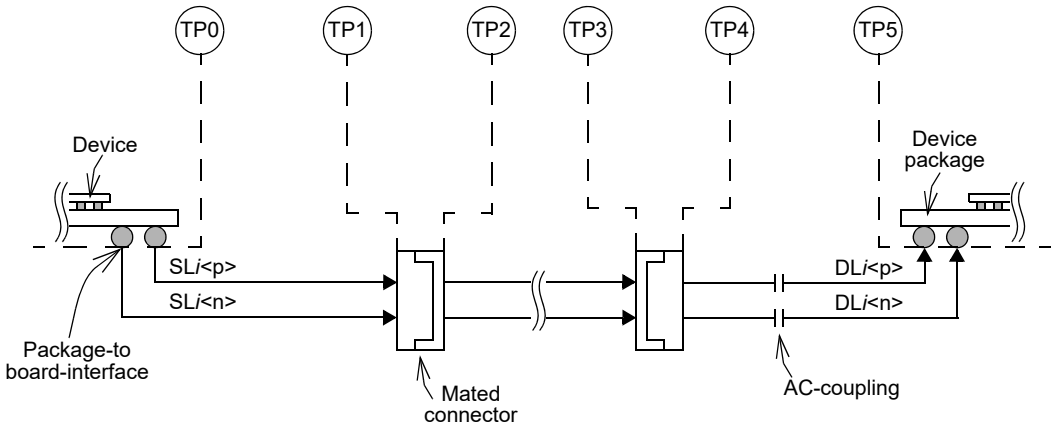

Figure 93B–1—Reference model (one direction from one lane is illustrated)

Table 93B–1—Description of channel components

Test points	Description
TP0 to TP1	The printed circuit board between the transmitter and the separable connector closest to the transmitter. TP1 is defined to be the interface between the board and connector plug.
TP2 to TP3	The electrical path from the separable connector closest to the transmitter to the separable connector closest to the receiver. TP2 and TP3 are defined to be the interface between connector receptacle and the printed circuit board.
TP4 to TP5	The printed circuit board between the receiver and the separable connector closest to the receiver. TP4 is defined to be the interface between the board and connector plug. It is recommended that the AC-coupling capacitors are implemented between TP4 and TP5
TP0 to TP5	The electrical backplane channel as defined in 93.9 or 111.9. TP0 and TP5 are defined to be the interface between the device package and the printed circuit board.

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Annex 93C

(normative)

Receiver interference tolerance

This annex defines a test setup (see 93C.1) and method (see 93C.2) for testing receiver interference tolerance. The PMD clause that invokes this method specifies the following items:

a) Constraint limit values for peak-to-peak voltage, the pre-cursor peaking ratio, and the post-cursor peaking ratio for test setup,
b) Lower frequency bound for the noise spectral density constraints (f_{NSD1}),
c) Jitter parameters to be measured in test method step 3,
d) Target Channel Operating Margin (COM) and RSS_DFE4 values for the test system in test method step 7,
e) COM parameter table in test method step 7,
f) Jitter transformation method in test method step 7,
g) Test pattern in test method step 9, and
h) Test system frequency response.

NOTE—The intent of the interference tolerance test is to ensure that the PHY receiver operates correctly with transmitter parameters anywhere within the specified limits including the case where all parameters are at the specified limits. Testing of the receiver with transmitter parameters beyond the specified limits may be helpful to determine margin or to provide comparative metrics, but failure of the receiver to operate correctly under these conditions is not to be interpreted as non-compliance.

93C.1 Test setup

The interference tolerance test is performed with the setup shown in Figure 93C–2 or its equivalent. Calibration and characterization of the various elements in the test setup is accomplished using the test configurations in Figure 93C–3, Figure 93C–4, Figure 93C–5, and Figure 93C–6.

The transmitter is functionally and parametrically compliant to the requirements of the invoking PMD clause. The ISI channel emulates the frequency dependent loss of a backplane channel. The channel noise source emulates crosstalk, transmitter noise, and unequalizable signal distortions introduced by a channel.

The transmitter output, as measured at TP0a, meets all transmitter specifications as indicated by the invoking PMD clause. In addition, the transmitter output, as measured at TP0a, is constrained such that for any transmitter equalizer setting the maximum differential peak-to-peak voltage, the pre-cursor peaking ratio, and the post-cursor peaking ratio are constrained as indicated by the PMD clause that invokes this method.

The channel noise source has an adjustable output such that the level may be set according to the test procedure. The noise produced by the channel noise source is measured directly at the output of the noise source (see Figure 93C–6). The noise is Gaussian with a crest factor of at least 5. The noise spectral density, $NSD(f)$, is normalized and constrained according to the relations in Equation (93C–1), where f_b is the symbol rate and f_{NSD1} is specified by the PMD clause that invokes this method. $NSD(f)$ is in units of V^2/Hz. The average noise spectral density, NSD_{average}, is determined according Equation (93C–2). An example constraint template with f_{NSD1} equal to $0.08f_b$ is illustrated in Figure 93C–1.

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$$\left.\begin{aligned} 10\log_{10}\left(\frac{NSD(f)}{NSD_{average}}\right) &< 3 \\ 10\log_{10}\left(\frac{NSD(f)}{NSD_{average}}\right) &> -3(1 - 1.2f/f_b) \end{aligned}\right\} f_{NSD1} \le f \le f_b/2 \quad \text{(93C–1)}$$

$$NSD_{average} = \frac{\int_{f_{NSD1}}^{f_b/2} NSD(f)df}{f_b/2 - f_{NSD1}} \quad \text{(93C–2)}$$

The receiver on one lane at a time is tested for compliance. The input to the receiver on each of the other lanes is generated by a transmitter with similar levels and equalization settings and transmitted through a similar channel, such that the input signals are similar to the input signal on the lane under test.

NOTE—FEXT and NEXT in the test setup are not accounted for in the test channel calibration (see 93A.2). It is recommended that the test setup be designed to minimize these effects.

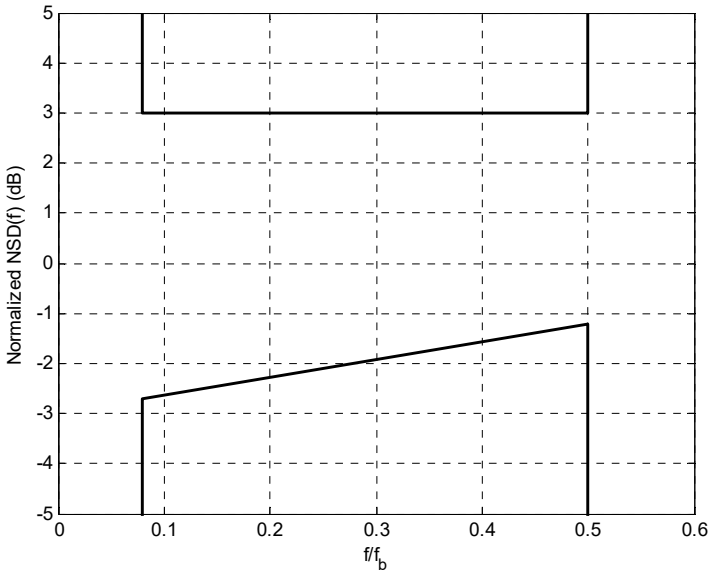

Figure 93C–1—Example NSD(f) constraint template

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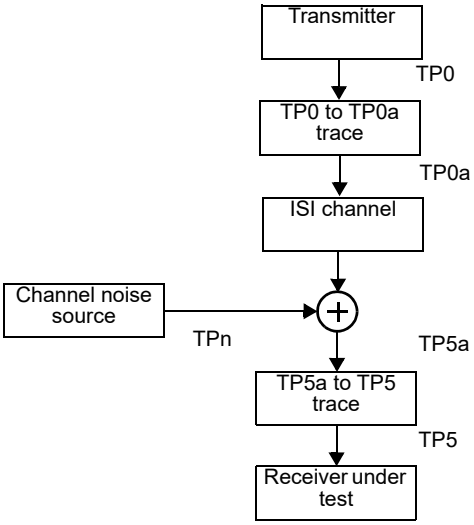

Figure 93C–2—Interference tolerance test setup

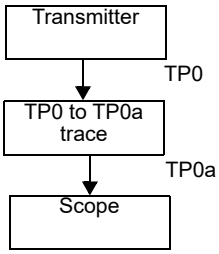

Figure 93C–3—Interference tolerance transmitter test setup

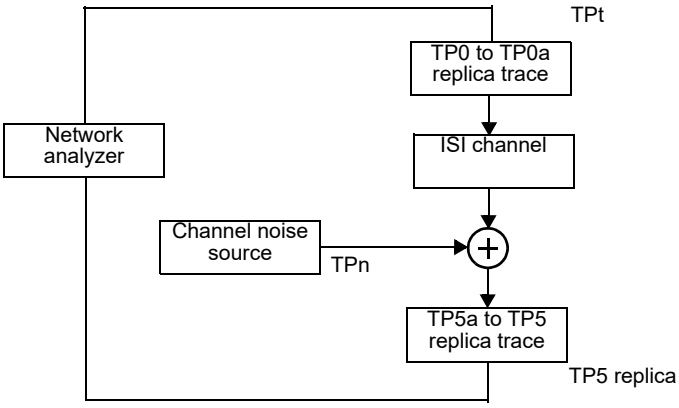

Figure 93C–4—Interference tolerance channel s-parameter test setup

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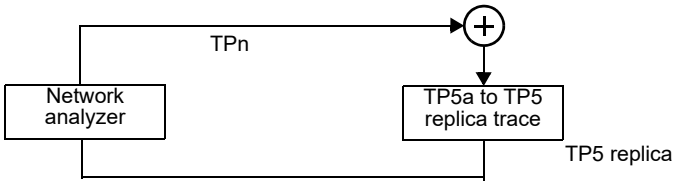

Figure 93C–5—Interference tolerance channel noise path test setup

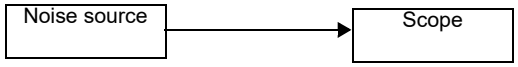

Figure 93C–6—Interference tolerance channel noise level test setup

93C.2 Test method

The interference tolerance test is performed using the following method:

1) Set the channel noise source to zero.
2) Using the test setup in Figure 93C–2, initiate the training sequence, allow the training sequence to complete, and retain the resulting transmitter tap coefficients.
3) Measure the jitter parameters relevant to the PMD clause that invokes this method that are to be used to set the value of σ_{RJ} and A_{DD} in step 7.
4) Measure the noise parameters relevant to the PMD clause that invokes this method that are to be used to set the value SNR_{TX}.
5) Using the test setup in Figure 93C–4 (also see Figure 93A–2), measure the scattering parameters, $S^{(tc)}$, of the test channel (TPt to TP5 replica).
6) Using the test setup in Figure 93C–5 (also see Figure 93A–2), measure the scattering parameters, $S^{(nc)}$, of the noise addition network (TPn to TP5 replica).
7) Using the procedure defined in 93A.2: (a) determine the receiver noise level, σ_{bn}, required to achieve the COM value specified in the PMD clause that invokes this method, and (b) verify that RSS_DFE4 is greater than or equal to the value specified in the PMD clause that invokes this method. The procedure is based on the calculation of COM, which uses the parameters defined in the COM parameter table in the PMD clause that invokes this method with the following exceptions. The value of σ_{RJ} and A_{DD} are set based on a transformation of measured parameters as specified in the PMD clause that invokes this method. The value of SNR_{TX} is set based on a transformation of the measured parameters specified in the PMD clause that invokes this method. In the COM computation the transmitter package model is included only if a compliant transmitter with a similar termination is used. If a transmitter with high quality termination is used, in the COM calculation, the termination is modeled as ideal and a Gaussian low pass filter is added to Equation (93A–19), which has the same 20% to 80% transition time as the transmitter measured at TP0a.
8) Using the test setup in Figure 93C–6, measure the channel noise voltage σ_{bnm} and adjust it so that it equals σ_{bn} determined in step 7. The channel noise voltage is determined from the measured $NSD(f)$ according to Equation (93C–3).
9) Using the test setup in Figure 93C–2, the transmitter taps as determined in step 2, and the channel noise as determined in step 7, configure the transmitter to transmit the test pattern specified in the PMD clause that invokes this method. Also configure the transmitters of the PMD under test to transmit the same test pattern, with their transmitters in the preset condition.

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10) Measure the FEC symbol error ratio on the receiver under test using the errored symbol counter, FEC_symbol_error_counter_*i*, where *i* is the lane number of the receiver under test.

$$\sigma_{bnm} = \sqrt{\int_0^{f_b/2} NSD(f)df} \quad \text{(93C–3)}$$

A test system with frequency response specified in the PMD clause that invokes this method is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.

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Annex 97A

(normative)

Common-mode conversion test methodology

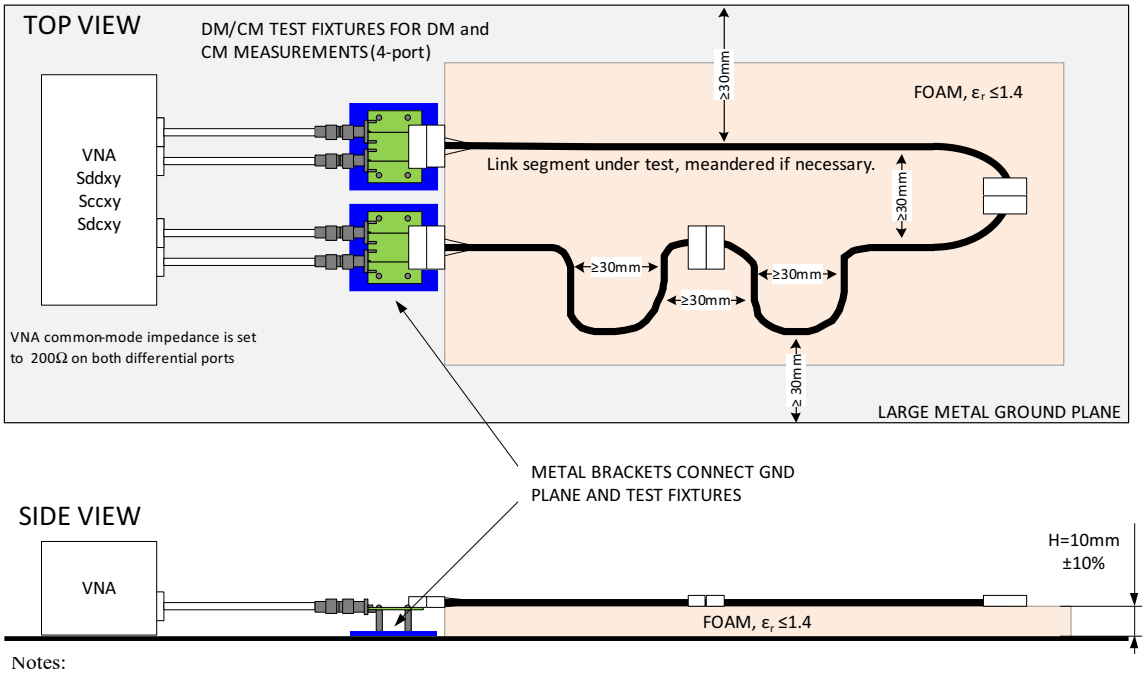
97A.1 Introduction

This annex describes the test methodologies that shall be used to measure the 1000BASE-T1 link segment differential-to-common-mode conversion loss specified in 97.6.1.4.

97A.2 Test configuration and measurement

The common-mode conversion loss is measured in a specified test environment to ensure repeatability. Individual test fixtures are illustrated in Figure 97A–1 and Figure 97A–2. The 1000BASE-T1 link segment is placed on a reference plane raised 10 mm from the surface of the ground plane.

To avoid ground-plane edge effects the 1000BASE-T1 link segment is placed 30 mm from the edge of the ground plane, this same spacing is used between adjacent sections of the same link segment to avoid unwanted coupling. The link segment parameters specified in 97.6 are to be measured using Annex 97A methodology.



Notes:
1. Two DM/CM test fixtures are used for all 4-port differential-mode and common-mode measurements.
2. Brackets provide reference “0V” for CM at the ends of DUT and VNA cables.
3. The entire setup is on a large metal GND plane, which extends at least 30 mm beyond the setup.

Figure 97A–1—Four-port test setup

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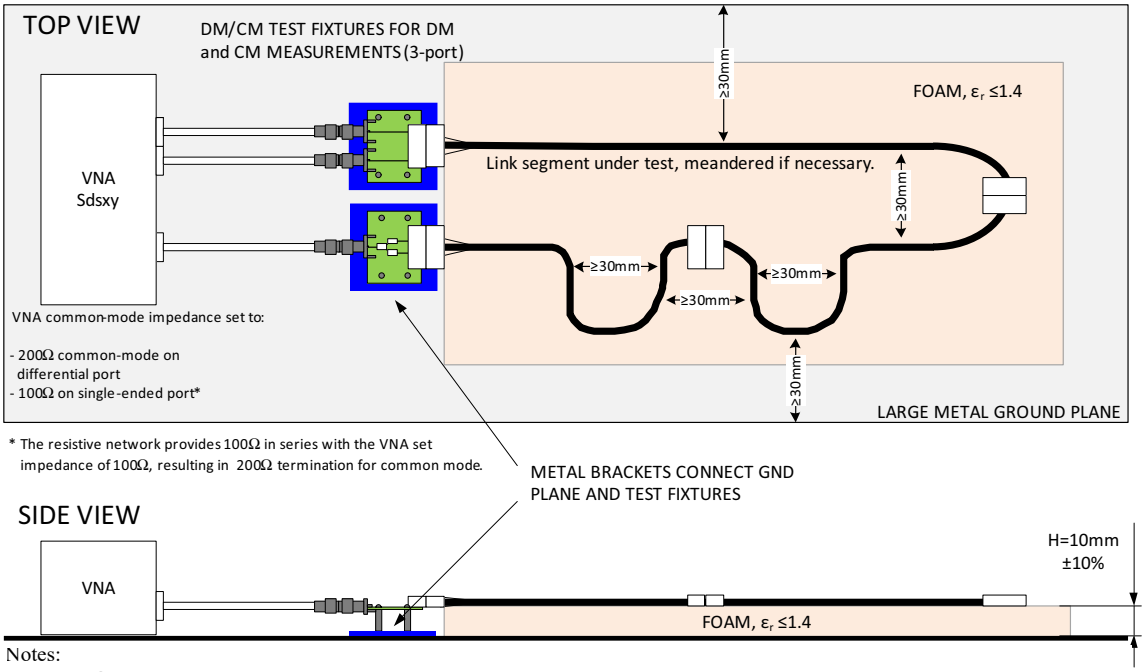

Notes:
1. The 50 Ω 0.1% resistors are RF-type DMS 0805 or smaller, e.g., Vishay FC series thing-film resistors.
2. Brackets provide reference “0V” for CM at the ends of DUT and VNA cables.
3. The entire setup is on a large metal GND plane, which extends at least 30 mm beyond the setup.

Figure 97A–2—Three-port common-mode conversion loss measurement

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97A.3 Protocol implementation conformance statement (PICS) proforma for Annex 97A, Common-mode conversion test methodology[299]

97A.3.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 97A, Common-mode conversion test methodology, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

97A.3.2 Identification

97A.3.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

97A.3.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 97A, Common-mode conversion test methodology
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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97A.3.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
CMC1	1000BASE-T1 test methodologies	97A.1	Used to measure the 1000BASE-T1 link segment differential-to-common-mode conversion loss specified in 97.6.1.4	M	Yes [ ] No [ ]

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Annex 97B

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Alien Crosstalk Test Procedure

97B.1 Introduction

Annex 97B describes a procedure for measuring ANEXT loss and AFEXT loss between pairs of adjacent link segments consisting of cables and in-line connectors.

The procedure is required to assess the alien crosstalk performance of the link segments as specified in 97.6.3 and 97.6.4. This procedure is intended for use in the laboratory, to evaluate that the link segments complies with the PSANEXT loss and PSAACRF requirements, when properly installed.

97B.1.1 Alien crosstalk test configurations

The limits for PSANEXT and PSAACRF are based on the alien crosstalk test configurations in Figure 97B–2, Figure 97B–3, Figure 97B–4, and Figure 97B–5. The automotive link segment test configurations are derived from two automotive industry use cases representative of common scenarios.

Measurements to be performed at 23°C ± 5°C relative humidity 25% to 75%.

Multiport test fixtures are used for multiport link segments. The number of disturbing ports to be included in the power sum calculation is dependent on the configuration. Significant connectors may be located in the same or other mounting systems in close proximity and are assessed as follows. For any given configuration, the determination of which ports to be included can be made based on the ANEXT loss contribution to the disturbed port. If at any frequency point the ANEXT measurement is less than 90 dB, then the entire ANEXT loss and PSAACRF response of that connector combination shall be included in the overall power sum result.

Link segment ends not under test are terminated in 100 Ω differential mode and 200 Ω common mode.

97B.2 Alien crosstalk coupled between type A link segments

The use case 1 alien crosstalk test configuration consists of three link segments of 5 m length and two in-line connectors, equally spaced at 1.66 m distance.

The use case 2 alien crosstalk test configuration consists of 5 link segments bundled together over a 5 m length with the center link segment extending unbundled for 3 m. The 3 m unbundled section includes 2 in-line connectors in addition to the 2 in-line connectors in the 5 m bundled section.

The alien crosstalk measurements are to be performed utilizing the test setup and methodology specified in Annex 97B.

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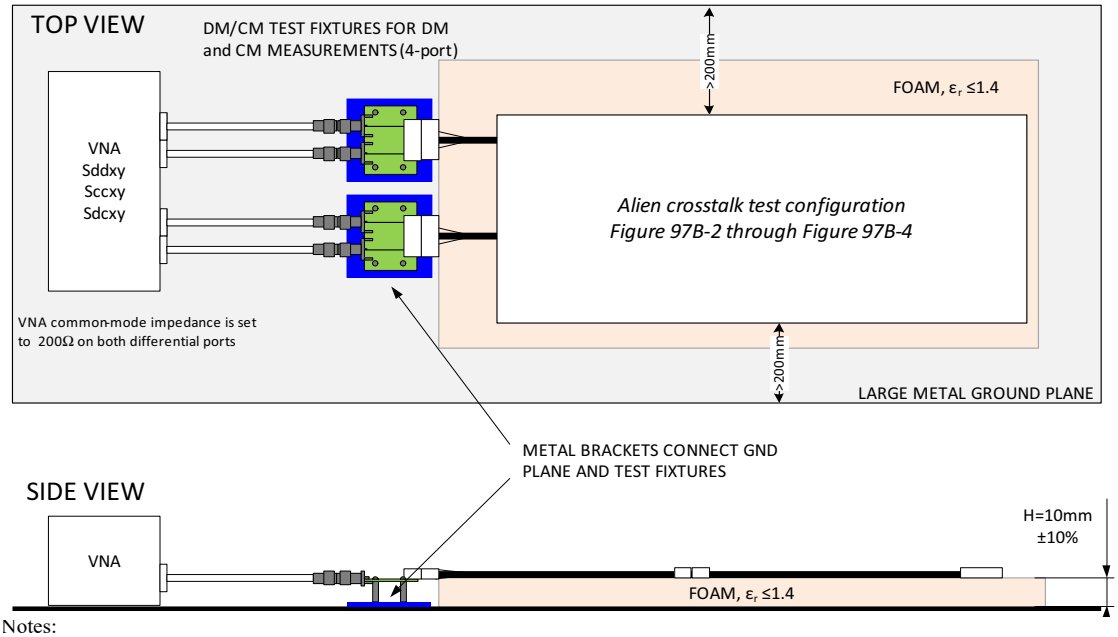

Notes:
1. Two DM/CM test fixtures are used for all 4-port differential-mode and common-mode measurements.
2. Brackets provide reference “0V” for CM at the ends of DUT and VNA cables.
3. The entire setup is on a large metal GND plane, which extends at least 200 mm beyond the setup.

Figure 97B–1—Alien crosstalk test setup

97B.3 Cable bundling

The cable bundle shall be placed on dielectric insulation material (εR < 1.4) of 10 mm height over conducting ground plane. The cables are uniformly fixed in their position by means of cable straps or adhesive tape to keep the cables attached together with a maximum distance between the fixation devices of 30 cm.

The measurement test fixtures are to be connected to the reference ground plane by means of conducting stands, copper braid, or foil.

If it is necessary to split up the wiring harness at the end of the bundle in order to accommodate the measurement fixtures, the length of the area split up is limited to the maximum of 30 cm.

An example of cable bundling for the 2-around–1 alien crosstalk test configuration is illustrated in Figure 97B–4.

An example of cable bundling for the 4-around–1 alien crosstalk test configuration is illustrated in Figure 97B–5. For use case 2, the link segment extending unbundled for 3 m is centered in the cable bundle e.g., cable 2 in Figure 97B–5.

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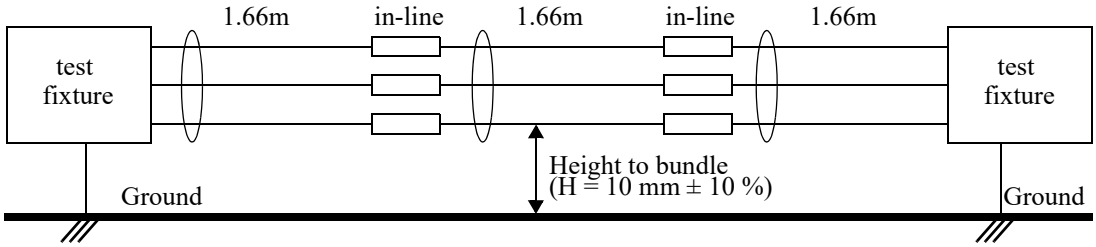

Figure 97B–2—Use Case 1 test configuration

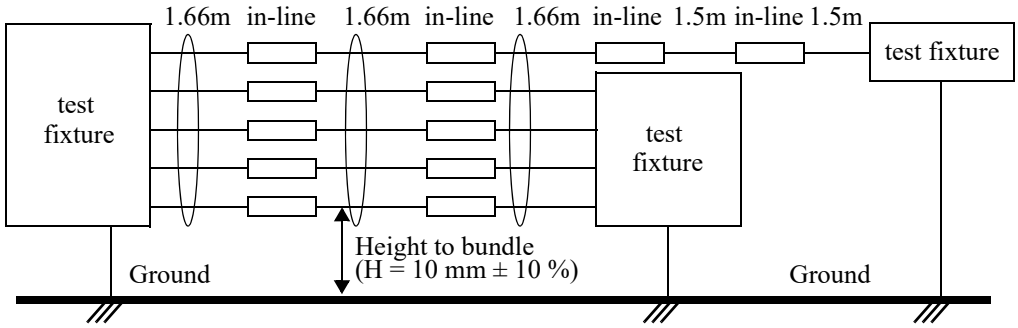

Figure 97B–3—Use Case 2 test configuration

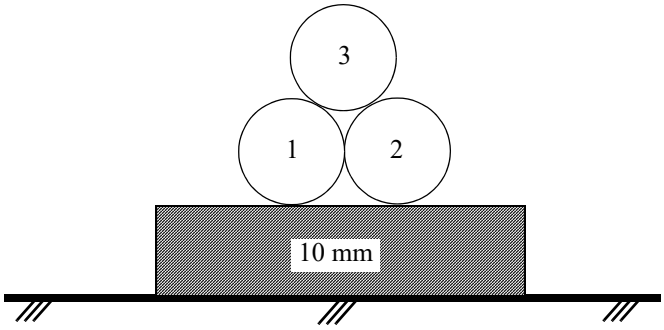

Figure 97B–4—Cable bundle in 2-around–1 configuration

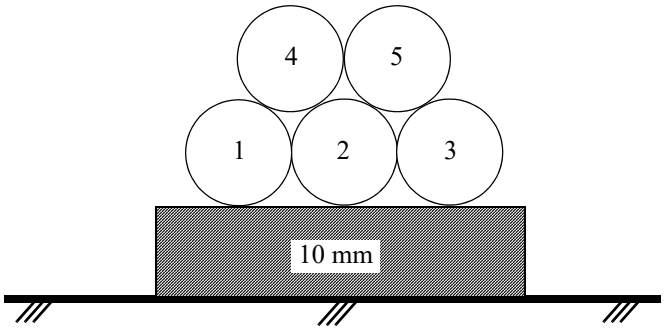

Figure 97B–5—Cable bundle in 4-around–1 configuration

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97B.4 Protocol implementation conformance statement (PICS) proforma for Annex 97B, Alien Crosstalk Test Procedure[300]

97B.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 97B, Alien Crosstalk Test Procedure, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

97B.4.2 Identification

97B.4.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

97B.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 97B, Alien Crosstalk Test Procedure
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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97B.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
ACTP1	Sum of ANEXT loss and PSAACRF response	97B.1.1	Include entire ANEXT loss and PSAACRF response of connector combination in the overall power sum result, if at any frequency point the ANEXT measurement is less than 90 dB	M	Yes [ ] No [ ]
ACTP2	Cable bundle placement	97B.3	On dielectric insulation material ($\varepsilon R < 1.4$) of 10 mm height over conducting ground plane	M	Yes [ ] No [ ]

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Annex 98A

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Selector Field definitions

98A.1 Introduction

The Selector Field, S[4:0] in the link codeword, shall be used to identify the type of message being sent by Auto-Negotiation. The following table identifies the types of messages that may be sent. The Selector Field uses a 5-bit binary encoding, which allows 32 messages to be defined. All unspecified combinations are reserved. Reserved combinations shall not be transmitted.

Table 98A–1—Selector Field Encoding

S4	S3	S2	S1	S0	Selector description
0	0	0	0	0	Reserved
0	0	0	0	1	IEEE Std 802.3
0	0	0	1	X	Reserved
0	0	1	X	X	Reserved
0	1	X	X	X	Reserved
1	X	X	X	X	Reserved

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Annex 98B

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IEEE 802.3 Selector Base Page definition

98B.1 Introduction

This annex provides the Technology Ability Field bit assignments, Priority Resolution table, and Message Page transmission conventions relative to the IEEE 802.3 Selector Field value within the Base Page encoding for devices using Clause 98 Auto-Negotiation.

The Technology Ability Field is inserted into the Priority Resolution hierarchy and made a part of the Auto-Negotiation process. The relative hierarchy of the existing technologies is designed in such a way that backward compatibility with existing Auto-Negotiation implementations is maintained.

Reserved bits shall be transmitted as zeros. This is to ensure that devices implemented using the current priority table forward updated priority tables.

98B.2 Selector field value

The value of the IEEE 802.3 Selector Field is S[4:0] = 00001.

98B.3 Technology Ability Field bit assignments

The Technology Ability Field consists of bits D21 through D47 (A0–A26, respectively) in the IEEE 802.3 Selector Base Page. Table 98B–1 summarizes bit assignments in the Technology Ability Field. Note that the order of the bits within the Technology Ability Field has no relationship to the relative priority of the technologies.

Table 98B–1—Technology Ability Field bit assignments

bit	Selector description
A0	100BASE-T1 ability
A1	10BASE-T1S full duplex ability
A2	1000BASE-T1 ability
A3	2.5GBASE-T1 ability
A4	5GBASE-T1 ability
A5	10GBASE-T1 ability
A6 through A8	Reserved
A9	10BASE-T1L capability
A10 through A21	Reserved

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Table 98B–1—Technology Ability Field bit assignments *(continued)*

bit	Selector description
A22	10BASE-T1S half duplex capability
A23	10BASE-T1L increased transmit level request
A24	10BASE-T1L increased transmit/receive level ability
A25	10BASE-T1L EEE ability
A26	Reserved

98B.3.1 10BASE-T1L-specific bit assignments

Configuration of 10BASE-T1L specific bits A23, A24, and A25 are specified in 146.6.

98B.4 Priority Resolution

Since a local device and a link partner may have multiple abilities in common, a prioritization scheme exists to ensure that the highest common denominator ability is chosen. The following list shall represent the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value, where priorities are listed from highest to lowest:

— 10GBASE-T1
— 5GBASE-T1
— 2.5GBASE-T1
— 1000BASE-T1
— 100BASE-T1
— 10BASE-T1S full duplex
— 10BASE-T1S half duplex
— 10BASE-T1L

98B.5 Message Page transmission convention

Each series of Unformatted Pages shall be preceded by a Message Page containing a message code that defines how the following Unformatted Pages is used.

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Annex 98C

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Next Page Message Code Field definitions

98C.1 Introduction

This Annex defines the Next Page message code fields for devices using Clause 98 Auto-Negotiation. The Message Code Field of a message page used in Next Page exchange shall be used to identify the meaning of a message. Table 98C–1 identifies the types of messages that may be sent.

The Message Code Field uses an 11-bit binary encoding that allows 2048 messages to be defined. All message codes not specified shall be reserved.

Table 98C–1—Message Code Field values

Message code	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	Message code description
0	0	0	0	0	0	0	0	0	0	0	0	Reserved
1	0	0	0	0	0	0	0	0	0	0	1	Null Message
2 to 4												Reserved
5	0	0	0	0	0	0	0	0	1	0	1	Organizationally Unique Identifier Tagged Message
6	0	0	0	0	0	0	0	0	1	1	0	AN device Identifier Tag Code
7 to 2047	1	1	1	1	1	1	1	1	1	1	1	Reserved

98C.2 Message code 1—Null Message code

The Null Message code shall be transmitted during Next Page exchange when the Local Device has no further messages to transmit and the Link Partner is still transmitting valid Next Pages. See 98.2.4.3 for more details.

98C.3 Message code 5—Organizationally Unique Identifier (OUI) tag code

The OUI tag code message shall consist of a Message Next Page with the message code field 000 0000 0101 followed by one Unformatted Next Page defined as follows. The unformatted code field of Message Next Page 5 shall contain the most significant 11 bits of the OUI or CID (bits 23:13) in bits 26:16 (bits U0 to U10) with the most significant OUI or CID bit in bit 26 (bit U10) of the unformatted code field, the next 11 most significant bits of the OUI or CID (bits 12:2) in bits 42:32 (bit U26 to U16) with the most significant bit in bit 42 (bit U26). The unformatted code field of the Unformatted Next Page shall contain the remaining least significant 2 bits of the OUI or CID (bits 1:0) in bits 10:9 (U10 and U9) with OUI or CID bit 1 in bit 10 (bit U10) with the bits 8:0, 26:16 (bits U8 to U0, U21 to U11) as a user-defined user code value that is specific to

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the OUI or CID transmitted. The remaining unformatted code field bits in the Message Next Page and the Unformatted Next Page shall be sent as zero and ignored on receipt.

For example, assume that a manufacturer's IEEE-assigned OUI/CID value is AC-DE-48 and the manufacturer-selected user-defined user code associated with the OUI or CID is 1100 1110 0001 1111 1100_2. The message code values generated from these two numbers is encoded into the message Next Page and Unformatted Next Page codes, as specified in Figure 98C–1. For clarity, the position of the M bit[301] is illustrated.

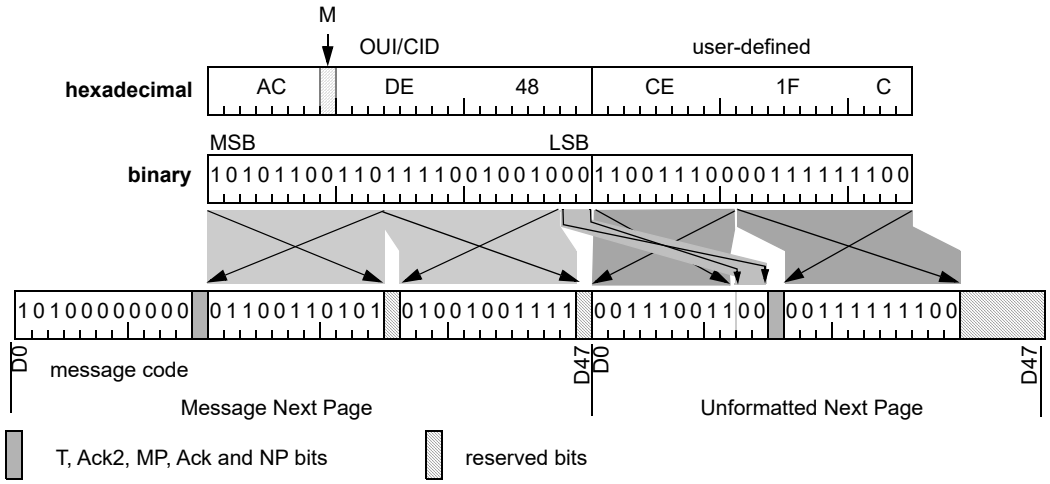

Figure 98C–1—Message code 5 sequence

NOTE—Figure 98C–1 shows the order Next Pages are transmitted, with the first transmitted Next Page shown in the leftmost position. This bits within each page are shown with the first transmitted bit (i.e., least significant bit) in the leftmost position. This is the same convention for bit order in the figures of Clause 98. Figure 28C–1 uses the opposite convention for bit order.

98C.4 Message code 6—AN device identifier tag code

The AN device ID tag code message shall consist of a Message Next Page with the message code field 000 0000 0110 followed by one Unformatted Next Page defined as follows. The unformatted fields of this message contain the AN device identifier (registers 7.2 and 7.3). The unformatted code field of Message Next Page 6 shall contain the most significant 11 bits of the AN device identifier (7.2.15:5) in bits 26:16 (bits U0 to U10) with the most significant AN device identifier bit in bit 26 (bit U10) of the unformatted code field, and the next 11 most significant bits of the AN device identifier (bits 7.2.4:0 to 7.3.15:10) in bits 42:32 (bit U26 to U16) with the most significant bit in bit 42 (bit U26) of the unformatted code field. The unformatted code field of the Unformatted Next Page shall contain the remaining least significant 10 bits of the AN device identifier (bits 7.3.9:0) in bits 10:1 (bit U10 to U1). Bits 0, 26:16 (bits U0, U21 to U11) of the unformatted code field of the Unformatted Next Page shall contain a user-defined user code value that is specific to the device identifier transmitted. The remaining unformatted code field bits in the Message Next Page and the Unformatted Next Page shall be sent as zero and ignored on receipt.

[301] See IEEE Std 802, subclause 9.3

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Annex 100A

(normative)

EPoC OFDM channel model

100A.1 Topology

The normative EPoC baseline channel conditions and OFDM channel parameters are referenced to the topology shown in Figure 100A–1. Numerous other topologies are possible that may exhibit better or worse performance than that shown in Figure 100A–1. When operating in a network that does not meet the parameters given in Table 100A–1 and Figure 100A–1 degraded performance is expected.

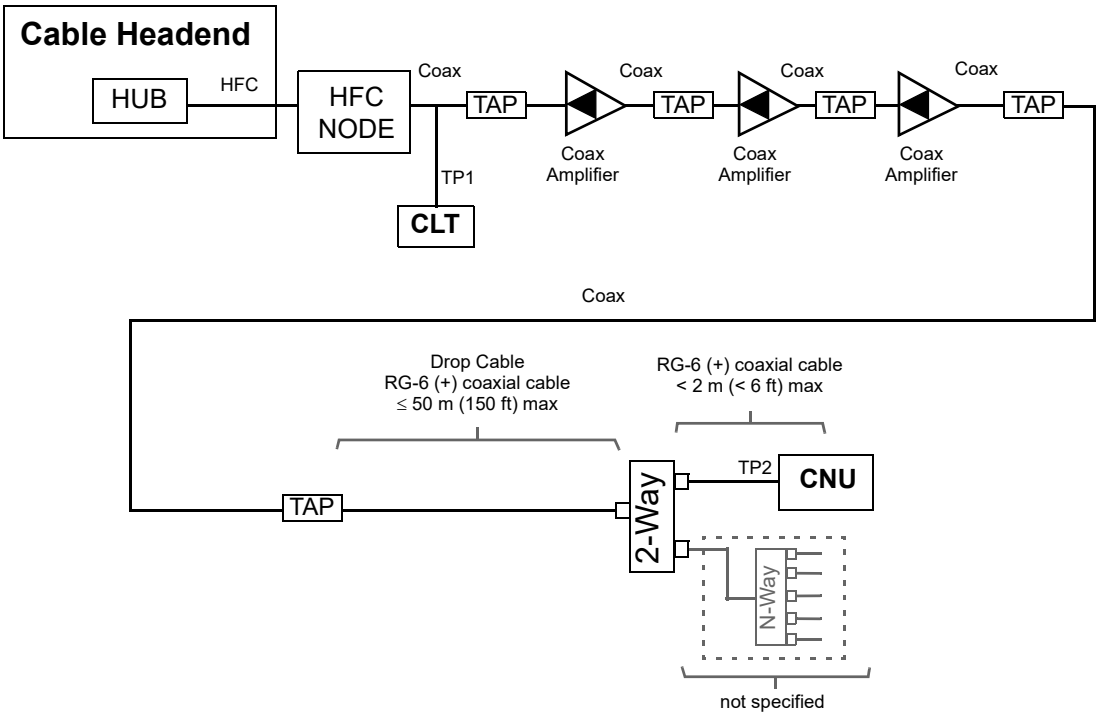

Figure 100A–1—EPoC network topology

NOTE—Additional information on cable coaxial network topology can be found in Modern Cable Television Technology [B55] and SCTE Measurement Recommended Practices for Cable Systems [B61].

100A.2 Downstream channel parameters

Devices designed to the EPoC PHY standard shall meet or exceed normative performance when operated in any network that meets or exceeds the parameters given in Table 100A–1 regardless of the network topology. The normative network operating parameters for the downstream direction in an EPoC network are

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given in Table 100A–1. These parameters are based on the following conditions:

— HFC downstream spectrum of 1 GHz.
— An amplifier cascade depth of N+3 (HFC Node plus CLT plus three coax amplifiers as in Figure 100A–1).
— A channel loading of 48 Analog TV channels (32 removed for EPoC) + 75 digital TV channels + 1 EPoC band (digital PSD@ –6 dBc).
— An HFC optical architecture of linear optics operating at 1310 nm (nominal link length) legacy with the EPoC RF coupled after HFC Node.
— A home architecture of up to the maximum drop cable length and one 2-way splitter.

Table 100A–1—Downstream EPoC channel parameters

Parameter	Nominal Conditions	Units
Spectrum		
Frequency range	54 to 1000	MHz
OFDM modulated spectrum	190	MHz
RF Level		
OFDM power at CPE input [2,3,4]		
6 MHz bandwidth	–2	dBmV
24 MHz bandwidth	4	dBmV
192 MHz bandwidth[5]	14	dBmV
Signal-to-noise Ratio		
Signal to composite noise ratio (SCN) ratio[6]	44	
Variation over 6 MHz bandwidth[15]	N/A	
Variation over 24 MHz bandwidth	1.5	dB
Variation over 192 MHz bandwidth	3	dB
Narrowband Interference		
Composite triple beat (CTB) interference (20 kHz bandwidth) number of interfered subcarriers [7,8]		
@ 35 to 40 dBc	0	%
@ 40 to 45 dBc	1	%
@ > 45 dBc	0	%
Composite second order (CSO) interference (20 kHz bandwidth) number of interfered subcarriers[9]		
@ 35 to 40 dBc	0	%
@ 40 to 45 dBc	0	%
@ 45 to 50 dBc	2	%
@ > 50 dBc	0	%
Narrowband interference (other)		
Bandwidth (MHz)	N/A	
Level, dBc (PSD)	N/A	
Wideband Interference		
Burst interference[10]		

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Table 100A–1—Downstream EPoC channel parameters *(continued)*

Parameter	Nominal Conditions	Units
Bandwidth	30	MHz
Level, dBc	–20	PSD
Duration	16	μs
Period	infrequent	Hz
Impulse (white) noise[11]		
Level, dBc	N/A	PSD
Duration	N/A	μs
Period	N/A	Hz
Frequency response / amplitude		
Amplitude slope[12]	0.01	dB/MHz
Amplitude variation[14]		
per 6 MHz	1	dB peak to peak
per 24 MHz	3	dB peak to peak
per 192 MHz	5	dB peak to peak
Total downstream bandwidth	9	dB peak to peak
Frequency Response / Phase		
Group delay variation		
Over 24 MHz		
Mid band	25	ns
Band edge (24 MHz)	145	ns
Over 192 MHz		
Mid band	200	ns
Band edge (24 MHz)	320	ns
Frequency Response / Echo		
Echo profile[13]		
0.5 μs	–20	dBc
1 μs	–25	dBc
1.5 μs	–30	dBc
2 μs	–35	dBc
3 μs	–40	dBc
4.5 μs	–45	dBc
5 μs	–50	dBc
AM/carrier hum modulation	3	%

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Table 100A–1—Downstream EPoC channel parameters *(continued)*

Parameter	Nominal Conditions	Units
NOTE 1—If not defined otherwise, assume typically behaving link but where the behavior is the worst (frequency, location). NOTE 2—Frequency dependence of coax for broadband calculations: Loss B (dB) = Loss A (dB) × SQRT(B/A). NOTE 3—Reference virtual port level for 6 MHz signal at 1 GHz; 15 dBmV Tap port level, 100 ft drop, 2-way splitter. NOTE 4—(Maximum frequency – OFDM bandwidth) spectrum range used for drop loss. NOTE 5—The tilt due to the drop cable has a small effect on calculation. NOTE 6—SCN includes HFC geography impact (location in cascade depth). NOTE 7—Subchannel reference, live video, fully contained within subchannel subcarriers with interference (subcarriers): Every 70 subcarriers, a cluster of three interferes: I_0, I_0 + 25 kHz, I_0 – 25 kHz. NOTE 8—Typically = CTB/CSO worst case frequency; good CTB/CSO in low-distortion band, Analog contiguous at low end of band National Cable & Telecommunications Association measurement method (average); Error rate simulation should account for peak-to-average ratio (PAR) and peak durations. NOTE 9—Worst spectrum regions for CTB and CSO are not the same. NOTE 10—Downstream burst characterization in process; bandwidth based on percentage of errored carriers in 8-Channel wide DOCSIS® [a] cable modem (CM) duration based on large scale CM sweep of uncorrectable codeword error rate with known interleaver settings; levels per ReDesign channel model. NOTE 11—Laser clipping PSD captured in SCN for out-of-band EPoC Signals. NOTE 12—Typical tilt, first tap, not equalized, 50 ft drop assumed (minimum drop impact). NOTE 13—Echo mask range for a single dominant echo - does not imply assumptions about multiple echoes. NOTE 14—Society of Cable and Telecommunication Engineers (SCTE) definition, echo not included. NOTE 15—Reference basis 6 MHz.		

[a]DOCSIS is a registered trademark of CableLabs.

100A.3 Upstream channel parameters

Devices designed to the EPoC PHY standard shall meet or exceed normative performance when operated in any network that meets or exceeds the parameters given in Table 100A–2 regardless of the network topology. The normative network operating parameters for the upstream direction in an EPoC network are given in Table 100A–2. These parameters are based on the following conditions:

— HFC upstream spectrum of 300 MHz.
— An amplifier cascade depth of N+3 (HFC Node plus CLT plus three coax amplifiers as in Figure 100A–1).
— A channel loading of remote transmitter and receiver.
— Head end architecture is not applicable as this section only address EPoC upstream path.
— A home architecture of up to the maximum drop cable length and one 2-way splitter.

Table 100A–2—Upstream EPoC channel parameters

Parameter	Nominal Conditions	Units
Spectrum		
Frequency range	100 to 292	MHz
OFDM modulated spectrum	190	MHz
Path Loss		
Path loss (max loss to first active)	44	dB
Variation frequency 24 MHz bandwidth[1]	1	dB

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Table 100A–2—Upstream EPoC channel parameters *(continued)*

Parameter	Nominal Conditions	Units
Variation frequency 192 MHz bandwidth	5	dBmV
Added Noise		
Input noise PSD (contributions of amplifiers)	–115	dBmV/Hz
Narrowband Interference		
FM band interference		
Bandwidth (spectrum overlap)	8	MHz
Level [2]	–40	dBc (PSD)
Common path distortion		
	N/A	dBc
affected subcarriers	N/A	%
Other bands (42 MHz to upstream band edge)		
	–50 [3]	dBc
affected subcarriers	1	%
Wideband Interference		
Burst interference [4]		
Bandwidth[5]	Occupied spectrum	MHz
Level	0	dBc (PSD)
Duration	1	μs
Period (poisson process)	1000	Hz
Frequency Response / Amplitude		
Amplitude slope (captured in path loss)	N/A	dB/MHz
Amplitude variation [8]		
per 24 MHz	1.5	dB peak to peak
per 192 MHz	3	dB peak to peak
Frequency Response / Phase		
Group delay variation		
Over 24 MHz		
Mid band	25	ns
Band edge (24 MHz)	280	ns
Over 48 MHz		
Mid band	50	ns
Band edge (24 MHz)	305	ns
Over 192 MHz	575	ns
Frequency Response / Echo		
Echo profile [6,7]		
0.5 μs	–16	dBc
1 μs	–22	dBc
1.5 μs	–29	dBc
2 μs	–35	dBc

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Table 100A–2—Upstream EPoC channel parameters *(continued)*

Parameter	Nominal Conditions	Units
3 μs	–42	dBc
4.5 μs	–51	dBc
Frequency Response / Spurious Modulation		
AM/carrier hum modulation	5	%

NOTE 1—Path loss adopted for consistency although return path, although RF actives include upstream gain.
NOTE 2—Measured samples in cable operator location of high field strength environment.
NOTE 3—Projected (for 50 kHz) from acceptable downstream interference level for analog video band (now upstream band); single dominant interferer and ingress point.
NOTE 4—Reference CableLabs 1997 Report "Characterization of Upstream Transient Impairments on Cable Television Systems."
NOTE 5—No linear optical return - no upstream laser clipping (white) impairment.
NOTE 6—Measured upstream CNU (97% criteria) extrapolated to band (30 MHz measured to 100 MHz).
NOTE 7—Echo mask range for a single dominant echo - does not imply any assumptions about multiple echoes.
NOTE 8—SCTE definition, echo not included.

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100A.4 Protocol implementation conformance statement (PICS) proforma for Annex 100A, EPoC OFDM channel model[302]

100A.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 100A, EPoC OFDM channel model, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

100A.4.2 Identification

100A.4.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

100A.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 100A, EPoC OFDM channel model
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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100A.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
PERF1	PHY downstream performance	100A.2	Meet or exceed normative performance when operated in any network that meets or exceeds the parameters given in Table 100A–1	M	Yes [ ] No [ ]
PERF2	PHY upstream performance	100A.3	Meet or exceed normative performance when operated in any network that meets or exceeds the parameters given in Table 100A–2	M	Yes [ ] No [ ]

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Annex 109A

(normative)

Chip-to-chip 25 Gigabit Attachment Unit Interface (25GAUI C2C)

109A.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 25 Gigabit Attachment Unit Interface (25GAUI C2C). Figure 109A–1 shows an example relationship of the 25GAUI C2C interface to the ISO/IEC Open System Interconnection (OSI) reference model. The 25GAUI C2C interface provides electrical characteristics and associated compliance points that can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.

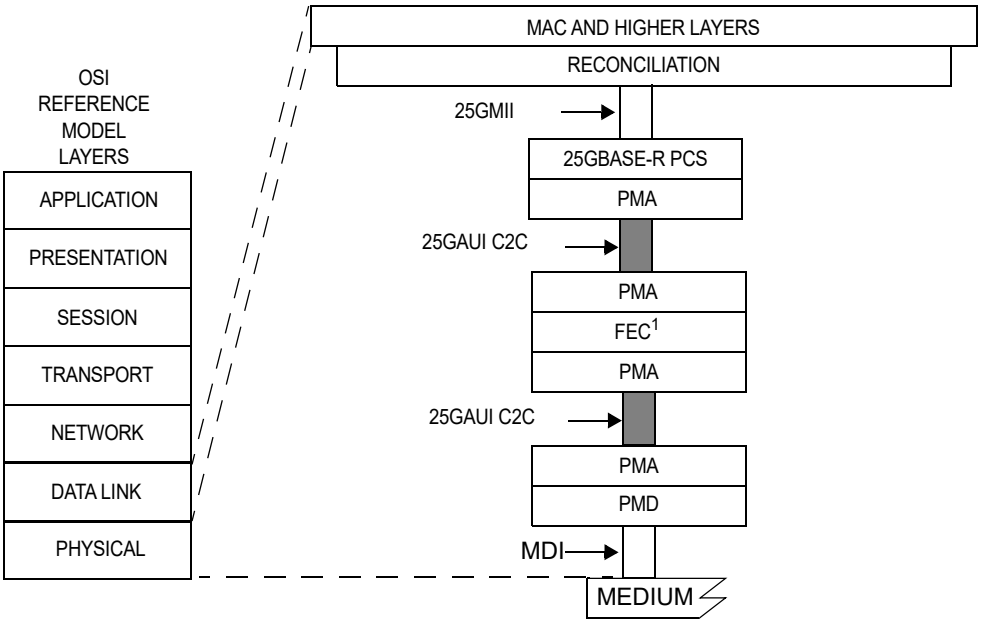

Figure 109A–1—Example 25GAUI C2C relationship to the ISO/IEC Open System Interconnection reference model and the IEEE 802.3 Ethernet model

The 25GAUI C2C bidirectional link is described in terms of a 25GAUI C2C transmitter, a 25GAUI C2C channel, and a 25GAUI C2C receiver. Figure 109A–2 depicts a typical 25GAUI C2C application, and Equation (83D–1) (illustrated in Figure 83D–3) summarizes the recommended differential insertion loss budget associated with the chip-to-chip application. The 25GAUI C2C interface comprises independent, differential data paths in each direction, which are AC-coupled. The nominal signaling rate is 25.78125 GBd. The 25GAUI C2C transmitter on each end of the link is adjusted to an appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 83D.3.3.2 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.

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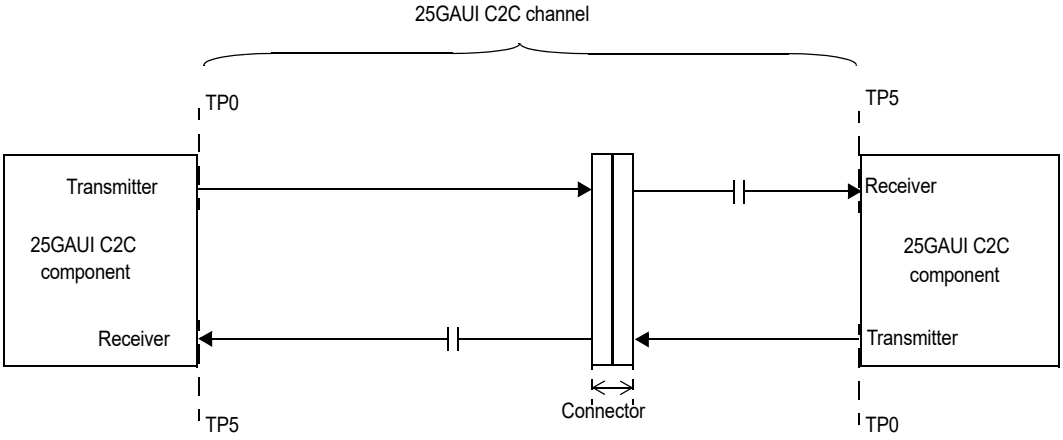

Figure 109A–2—Typical 25GAUI C2C application

The normative channel compliance is through 25GAUI C2C channel operating margin (COM) as described in 83D.4. Actual channel loss could be higher or lower than that given by Equation (83D–1) due to the channel ILD, return loss, and crosstalk.

109A.2 25GAUI C2C compliance point definition

The compliance points for the 25GAUI C2C interface are defined in 83D.2.

109A.3 25GAUI C2C electrical characteristics

109A.3.1 25GAUI C2C transmitter characteristics

A 25GAUI C2C transmitter shall meet all specifications of a single CAUI-4 lane as specified in 83D.3.1.

109A.3.2 25GAUI C2C receiver characteristics

A 25GAUI C2C receiver shall meet all specifications in Table 83D–4 for a single CAUI-4 lane. If the receiver supports the optional transmitter equalization feedback, it shall meet all requirements in 83D.3.3.2.

109A.3.3 Optional EEE operation

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78 and 78.3) then the inter-sublayer service interface includes four additional primitives as described in 83.3 and may also support 25GAUI shutdown (see 78.5.2).

If the EEE capability includes 25GAUI shutdown then the transmitter shall meet all requirements in 83D.3.2 and the receiver shall meet all requirements in 83D.3.4.

109A.4 25GAUI C2C channel characteristics

The 25GAUI C2C channel shall meet the requirements specified in 83D.4.

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109A.5 Protocol implementation conformance statement (PICS) proforma for Annex 109A, Chip-to-chip 25 Gigabit Attachment Unit Interface (25GAUI C2C)[303]

109A.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 109A, Chip-to-chip 25 Gigabit Attachment Unit Interface (25GAUI C2C), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

109A.5.2 Identification

109A.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

109A.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 109A, Chip-to-chip 25 Gigabit Attachment Unit Interface (25GAUI C2C)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

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109A.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*CHAN	Channel	83D.4	Items marked with CHAN include channel specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
*LPI	Support for 25GAUI shutdown	83D.3.2		O	Yes [ ] No [ ]

109A.5.4 PICS proforma tables for chip-to-chip 25 Gigabit Attachment Unit Interface (25GAUI C2C)

109A.5.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	83D.3.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TC2	Peak-to-peak differential output voltage	83D.3.1	1200 mV (max)	M	Yes [ ]
TC3	Peak-to-peak differential output voltage, transmitter disabled	83D.3.1	less than our equal to 30 mV	M	Yes [ ]
TC4	DC common-mode voltage	83D.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC5	AC common-mode output voltage	83D.3.1	12 mV RMS with respect to signal ground	M	Yes [ ]
TC6	Differential output return loss	83D.3.1	Meets Equation (93–3) constraints	M	Yes [ ]
TC7	Common-mode output return loss	83D.3.1	Meets Equation (93–4) constraints	M	Yes [ ]
TC8	Output waveform	83D.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC9	Output jitter	83D.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC10	Amplitude and swing for CAUI-4 shutdown	83D.3.2	Meets amplitude and swing requirements in 83D.3.2.	LPI:M	Yes [ ]
TC11	Transmit disable for CAUI-4 shutdown	83D.3.2	Meets transmit disable requirements in 83D.3.2.	LPI:M	Yes [ ]
TC12	Transmit equalization	83D.3.1.1	Each successive step results in a monotonic change	M	Yes [ ]

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109A.5.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	93.8.2.2	Meets Equation (93–3) constraints	M	Yes [ ]
RC2	Differential-to-common-mode input return loss	93.8.2.2	Meets Equation (93–5) constraints	M	Yes [ ]
RC3	Interference tolerance	83D.3.3.1	Satisfy requirements in Table 83D–5	M	Yes [ ]
RC4	Jitter Tolerance	93.8.2.4	Satisfy requirements in Table 93–7	M	Yes [ ]
RC5	Signal detect for 25GAUI shutdown	83D.3.4	Meets requirement of 83D.3.4.	LPI:M	Yes [ ]

109A.5.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	83D.4	Greater than or equal to 2 dB	CHAN :M	Yes [ ]

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Annex 109B

(normative)

Chip-to-module 25 Gigabit Attachment Unit Interface (25GAUI C2M)

109B.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 25 Gigabit Attachment Unit Interface (25GAUI C2M). Figure 109B–1 shows the relationship of the 25GAUI C2M interface to the ISO/IEC Open System Interconnection (OSI) reference model. The 25GAUI C2M interface provides electrical characteristics and associated compliance points that can optionally be used when designing systems with pluggable module interfaces.

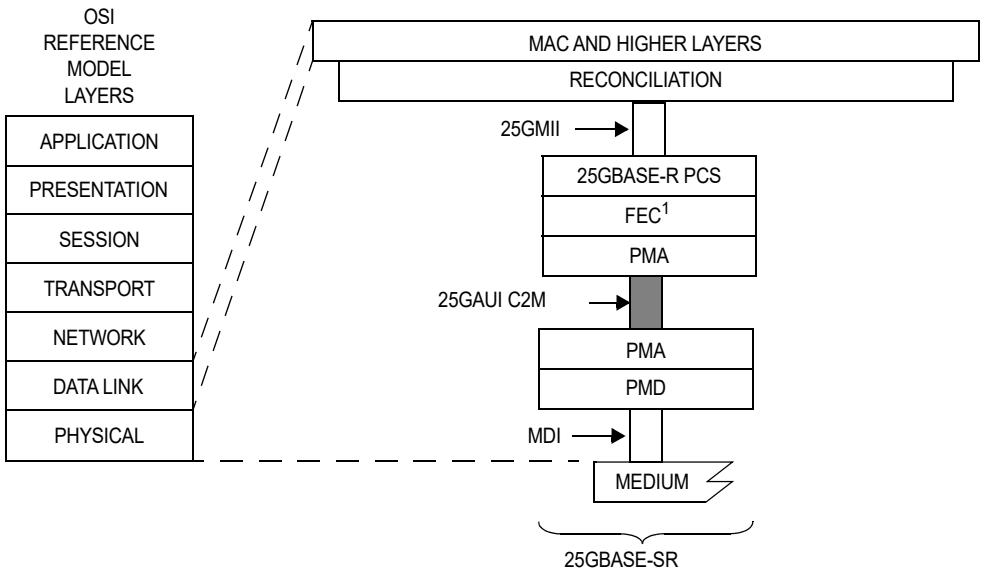

Figure 109B–1—Example 25GAUI C2M relationship to the ISO/IEC Open System Interconnection reference model and the IEEE 802.3 Ethernet model

The 25GAUI C2M link is described in terms of a host 25GAUI C2M component, a 25GAUI C2M channel with associated insertion loss, and a module 25GAUI C2M component.

For module form factors with more than one 25GAUI C2M lane, each lane comprises a separate 25GAUI C2M interface with independent management.

Figure 109B–2 depicts a typical 25GAUI C2M application with loss budget per section. The supported insertion loss budget is characterized by Equation (83E–1) and illustrated in Figure 83E–3.

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The 25GAUI C2M interface comprises independent data paths in each direction. Each data path contains a differential pair that is AC-coupled within the module. The nominal signaling rate is 25.78125 GBd. The 25GAUI C2M interface is defined using a specification and test methodology that is similar to that used for CEI-28G-VSR defined in OIF-CEI-03.1 [B57].

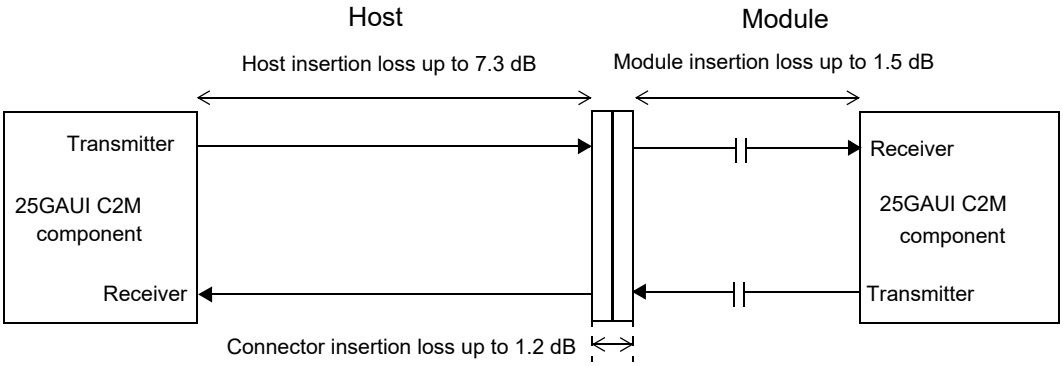

Figure 109B–2—25GAUI C2M insertion loss budget at 12.89 GHz

109B.1.1 Bit error ratio

For a PHY without the RS-FEC sublayer (Clause 108), the 25GAUI C2M bit error ratio (BER) is less than 10^{-15} with any errors sufficiently uncorrelated to ensure an acceptably high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding.

For a PHY with the RS-FEC sublayer (Clause 108), the 25GAUI C2M bit error ratio is less than 10^{-6} with any errors sufficiently uncorrelated to ensure a frame loss ratio (see 1.4.344) of less than 6.2×10^{-10} for 64-octet frames with minimum interpacket gap when processed according to Clause 108.

109B.2 25GAUI C2M compliance point definitions

25GAUI C2M compliance points are defined in 83E.2. The HCB and MCB for a four-lane connector (e.g., QSFP28) are described and specified in 92.11.2. The HCB and MCB for a single-lane connector (e.g., SFP28) are described and specified in Annex 110B.

109B.3 25GAUI C2M electrical characteristics

109B.3.1 25GAUI C2M host output characteristics

A 25GAUI C2M host output shall meet all specifications in 83E.3.1.

109B.3.2 25GAUI C2M module output characteristics

A 25GAUI C2M module output shall meet all specifications in 83E.3.2 with the exception of eye height, eye width, and vertical eye closure.

A 25GAUI C2M module output also shall meet the eye height, eye width, and vertical eye closure specified in 109B.3.2.1.

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109B.3.2.1 25GAUI C2M module output eye opening

Figure 83E–11 depicts an example module output eye test configuration. The module output eye is measured at TP4, as shown in Figure 83E–5. The module output eye is measured using a reference receiver with a continuous-time linear equalizer (CTLE) defined in 83E.3.2.1.1. The crosstalk generator is calibrated at TP1a with target differential peak-to-peak amplitude of 900 mV and target transition time of 19 ps.

For a PHY that includes an RS-FEC sublayer (Clause 108), the module output eye opening shall meet the eye opening requirements in either 109B.3.2.1.1 or 109B.3.2.1.2.

For a PHY that does not include an RS-FEC sublayer, the module output eye opening shall meet the eye opening requirements in 109B.3.2.1.1.

109B.3.2.1.1 Eye opening using measurement method A

Module output eye width (*EW15*) shall be greater than 0.57 UI. Module output eye height (*EH15*) shall be greater than 228 mV. Module output vertical eye closure (*VEC*) shall be less than 5.5 dB.

Eye width, eye height, and vertical eye closure are measured using the methodology described in 83E.4.2.

The input (counter-propagating) signal is asynchronous with the output signal and is modulated with a scrambled idle pattern (82.2.11), a PRBS31 pattern (49.2.8), or a valid 25GBASE-R signal.

109B.3.2.1.2 Eye opening using measurement method B

Module output eye width (*EW8*) shall be greater than 0.57 UI. Module output eye height (*EH8*) shall be greater than 228 mV. Module output vertical eye closure (*VEC8*) shall be less than 5 dB.

Eye width, eye height, and vertical eye closure are measured using the methodology described in 109B.4.1.

The input (counter-propagating) signal is asynchronous with the output signal and is modulated with a scrambled idle pattern (82.2.11) with RS-FEC encoding, a PRBS31 pattern (49.2.8), or a valid 25GBASE-R signal with RS-FEC encoding.

109B.3.3 25GAUI C2M host input characteristics

A 25GAUI C2M host input shall meet all specifications in 83E.3.3.

109B.3.4 25GAUI C2M module input characteristics

The 25GAUI C2M module input shall meet all specifications in 83E.3.3, with the exception of the module stressed input test. Channel equalization is provided by an equalizer in the module that uses the reference CTLE setting provided by the host or an adaptive equalizer in the module that does not use the setting provided by the host.

For a PHY that includes an RS-FEC sublayer, the 25GAUI C2M module input shall meet the module stressed input test requirements in either 109B.3.4.1 or 109B.3.4.2.

For a PHY that does not include an RS-FEC sublayer (Clause 108), the 25GAUI C2M module input shall meet the module stressed input test requirements in 109B.3.4.1.

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109B.3.4.1 Module stressed input test using measurement method A

The module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.

109B.3.4.2 Module stressed input test using measurement method B

The module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1 with the following exceptions. The input eye height and eye width are measured according to the method in 109B.4.1. The stressed input signal shall satisfy the input tolerance defined in Table 109B–1. The module receiver shall operate with a BER of better than 10^{-6} in the presence of a compliant stressed input signal.

Table 109B–1—Module stressed input parameters for method B

Parameter	Value
Eye width (EW8)	0.46 UI
Applied pk-pk sinusoidal jitter	Table 88–13
Eye height (EH8)	95 mV

109B.4 25GAUI C2M measurement methodology

109B.4.1 Eye width, eye height, and eye closure measurement method B

Eye width and eye height are measured using the methodology described in 83E.4.2 with the following exceptions:

a) For step 1, collect sufficient samples equivalent to at least 400 000 bits to allow for construction of a normalized cumulative distribution function (CDF) to a probability of 10^{-5} without extrapolation.

b) For step 4, calculate the best linear fit in Q-scale over the range of probabilities of 10^{-3} to 10^{-5} of CDFL and CDFR and calculate the eye width (*EW8*) using Equation (109B–1).

c) For step 6, calculate the best linear fit in Q-scale over the range of probabilities of 10^{-3} and 10^{-5} of CDF1 and CDF0 and calculate the eye height (*EH8*) using Equation (109B–2).

d) Measure the eye amplitude (*AV*) of the equalized waveform. Eye amplitude is defined as the mean value of logic one minus the mean value of logic zero in the central 5% of the eye. Calculate the vertical eye closure (*VEC8*) using Equation (109B–3).

$$EW8 = EW5 - 1.35\,(RJR + RJL) \quad (109B–1)$$

where

EW8 is the eye width extrapolated to 10^{-8} probability
EW5 is the eye width at 10^{-5} probability
RJL is the RMS value of the jitter estimated from CDFL
RJR is the RMS value of the jitter estimated from CDFR

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$$EH8 = EH5 - 1.35\ (RN0 + RN1) \quad (109B–2)$$

where

EH8 is the eye height extrapolated to 10^{-8} probability
EH5 is the eye height at 10^{-5} probability
RN1 is the RMS value of the noise estimated from CDF1
RN0 is the RMS value of the noise estimated from CDF0

$$VEC8 = 20\ \log_{10}(\mathrm{AV}/EH8) \quad (109B–3)$$

where

VEC8 is vertical eye closure in dB, extrapolated to 10^{-8} probability
AV is the eye amplitude of the equalized waveform
EH8 is the eye height defined in Equation (109B–2)

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109B.5 Protocol implementation conformance statement (PICS) proforma for Annex 109B, Chip-to-module 25 Gigabit Attachment Unit Interface (25GAUI C2M)[304]

109B.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 109B, Chip-to-module 25 Gigabit Attachment Unit Interface (25GAUI C2M), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

109B.5.2 Identification

109B.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

109B.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 109B, Chip-to-module 25 Gigabit Attachment Unit Interface (25GAUI C2M)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[304]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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109B.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
ADE	Adaptive equalizer	83E.3.4.1.1	Module 25GAUI receiver does not use *Recommended_CTLE_value*	O	Yes [ ] No [ ]
*RSFEC	PHY with 25G RS-FEC	109B.1.1		O	Yes [ ] No [ ]

109B.5.4 PICS proforma tables for chip-to-module 25 Gigabit Attachment Unit Interface (25GAUI C2M)

109B.5.4.1 Host output

Item	Feature	Subclause	Value/Comment	Status	Support
TH1	Signaling rate	83E.3.1.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TH2	Peak-to-peak differential output voltage	83E.3.1.2	900 mV (max)	M	Yes [ ]
TH3	Peak-to-peak differential output voltage, transmitter disabled	83E.3.1.2	Less than or equal to 35 mV	M	Yes [ ]
TH4	DC common-mode output voltage	83E.3.1	Between –0.3 V and 2.8 V with respect to signal ground	M	Yes [ ]
TH5	AC common-mode output voltage	83E.3.1	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TH6	Differential output return loss	83E.3.1.3	Meets Equation (83E–2) constraints	M	Yes [ ]
TH7	Reference impedance for output return loss	83E.3.1.3	100 Ω.	M	Yes [ ]
TH8	Common to differential mode conversion	83E.3.1.3	Meets Equation (83E–3) constraints	M	Yes [ ]
TH9	Differential termination mismatch	83E.3.1	Less than 10%	M	Yes [ ]
TH10	Transition time	83E.3.1.5	Greater than or equal to 10 ps	M	Yes [ ]
TH11	Eye width	83E.3.1	0.46 UI	M	Yes [ ]
TH12	Eye height A	83E.3.1	95 mV	M	Yes [ ]
TH13	Eye height B	83E.3.1	80 mV	M	Yes [ ]
TH14	Crosstalk source	83E.3.1.6	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 25GBASE-R signal	M	Yes [ ]

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109B.5.4.2 Module output

Item	Feature	Subclause	Value/Comment	Status	Support
*TM1	Module eye opening measured using method A	109B.3.2.1	Mandatory for PHY without RS-FEC and optional for PHY with RS-FEC.	!RSFEC: M RSFEC: O	Yes [ ] No [ ]
*TM2	Module eye opening measured using method B	109B.3.2.1	Mandatory for PHY with RS-FEC and not using method A.	RSFEC* !TM1:M	Yes [ ] No [ ]
TM3	Signaling rate	83E.3.1.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TM4	Peak-to-peak differential output voltage	83E.3.1.2	900 mV (max)	M	Yes [ ]
TM5	AC common-mode output voltage	83E.3.1.2	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TM6	Differential output return loss	83E.3.1.3	Meets Equation (83E–2) constraints	M	Yes [ ]
TM7	Reference impedance for output return loss	83E.3.1.3	100 Ω.	M	Yes [ ]
TM8	Common to differential mode conversion	83E.3.1.3	Meets Equation (83E–3) constraints	M	Yes [ ]
TM9	Differential termination mismatch	83E.3.1.4	Less than 10%	M	Yes [ ]
TM10	Transition time	83E.3.2	Greater than or equal to 12 ps	M	Yes [ ]
TM11	Eye width, *EW15*	109B.3.2.1.1	> 0.57 UI	TM1:M	Yes [ ]
TM12	Eye height, *EH15*	109B.3.2.1.1	> 228 mV	TM1:M	Yes [ ]
TM13	Vertical eye closure, *VEC*	109B.3.2.1.1	< 5.5 dB (max)	TM1:M	Yes [ ]
TM14	Eye width, *EW8*	109B.3.2.1.2	> 0.57 UI	TM2:M	Yes [ ]
TM15	Eye height, *EH8*	109B.3.2.1.2	> 228 mV	TM2:M	Yes [ ]
TM15	Vertical eye closure, *VEC8*	109B.3.2.1.2	< 5 dB (max)	TM2:M	Yes [ ]

109B.5.4.3 Host input

Item	Feature	Subclause	Value/Comment	Status	Support
RH1	Host input characteristics	83E.3.3	Table 83E–4	M	Yes [ ]

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109B.5.4.4 Module input

Item	Feature	Subclause	Value/Comment	Status	Support
*RM1	Module stressed input using method A	109B.3.4	Mandatory for PHY without RS-FEC and optional for PHY with RS-FEC	!RSFEC: M RSFEC: O	Yes [ ] No [ ]
*RM2	Module stressed input measured using method B	109B.3.4	Mandatory for PHY with RS-FEC and not using method A	RSFEC* !RM1:M	Yes [ ] No [ ]
RM3	Module input stressed input tolerance using measurement method A	109B.3.4.1	Meets requirements in 83E.3.4.1	RM1:M	Yes [ ]
RM4	Module input stressed signal using measurement method B	109B.3.4.2	Meets requirements in Table 109B–1	RM2:M	Yes [ ]
RM5	Receiver BER using measurement method B	109B.3.4.2	BER less than 10^{-6} with compliant stressed input signal	RM2:M	Yes [ ]
RM6	Meet BER requirement with three values of *Recommended_CTLE_value*	83E.3.4.1.1		M	Yes [ ]

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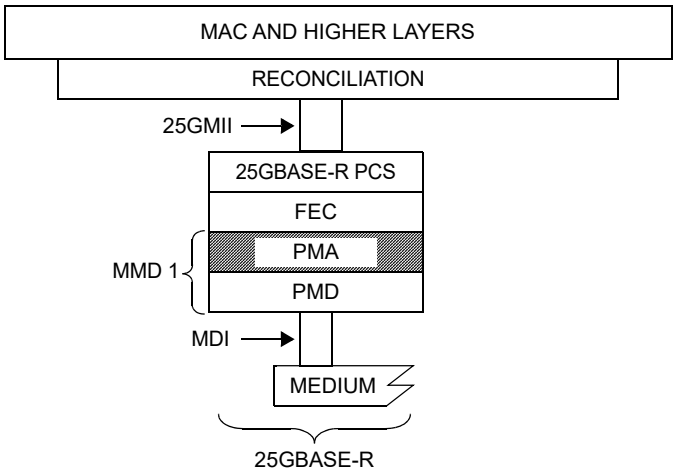
Annex 109C

(informative)

25GBASE-R PMA sublayer partitioning examples

The following figures provide various partitioning examples using the PMA, PMA service interface, and 25GAUI (see Figure 109C–1 through Figure 109C–6). Partitioning guidelines and MMD numbering conventions are described in 109.1.4. These partitioning examples are informative and do not specify a particular sublayer combination for any PHY. Specific and compliant sublayer combinations for a particular PHY are provided in the appropriate normative clause.

An example of an FEC (e.g., Clause 74, Clause 108) implemented in a separate device from either the PCS or the PMD is illustrated in Figure 109–3.



25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 109C–1—Example FEC implemented with PCS and PMD

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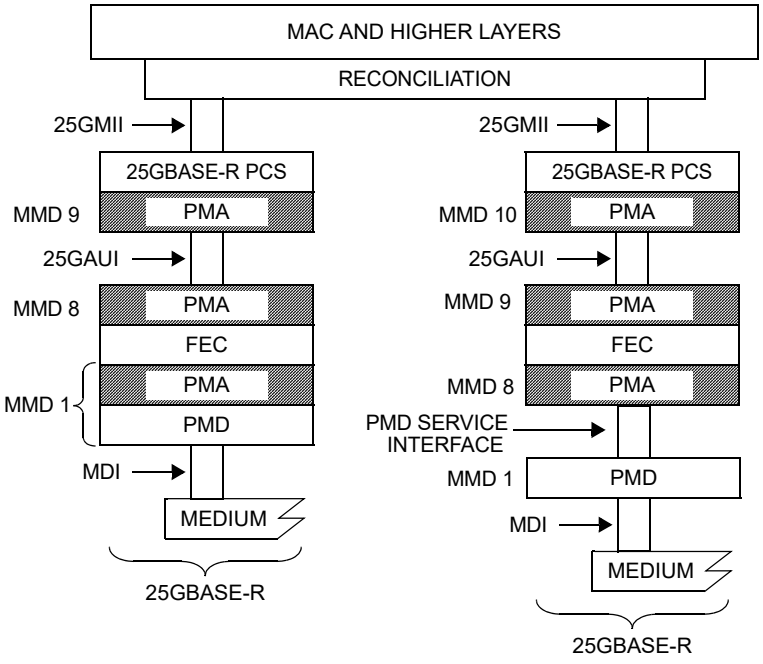
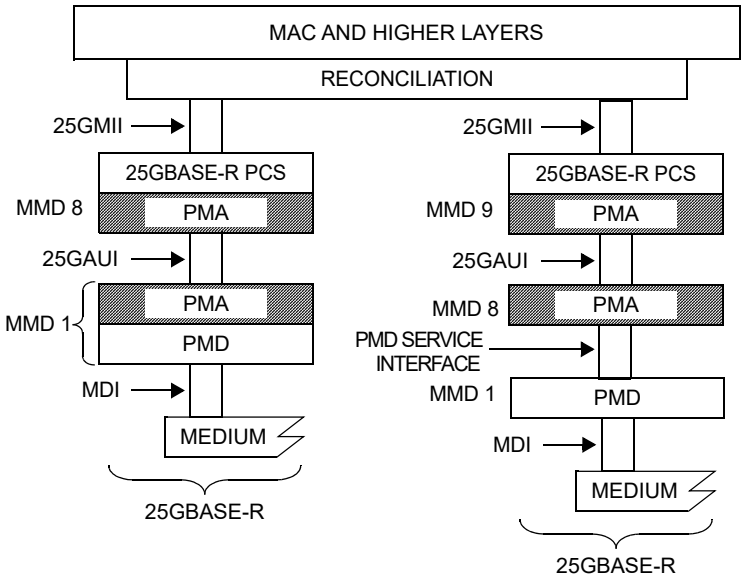


25GAUI = 25 GIGABIT ATTACHMENT UNIT INTERFACE
25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 109C–2—Example FEC implemented with PMD



25GAUI = 25 GIGABIT ATTACHMENT UNIT INTERFACE
25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 109C–3—Example single 25GAUI without FEC

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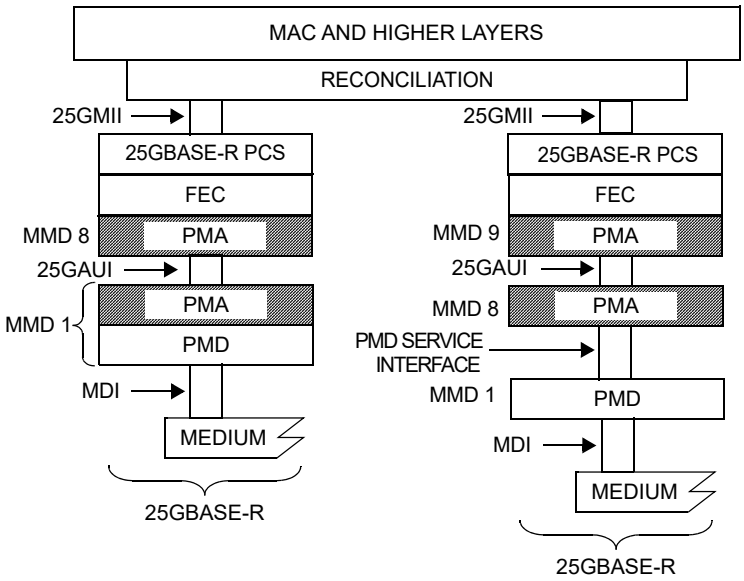
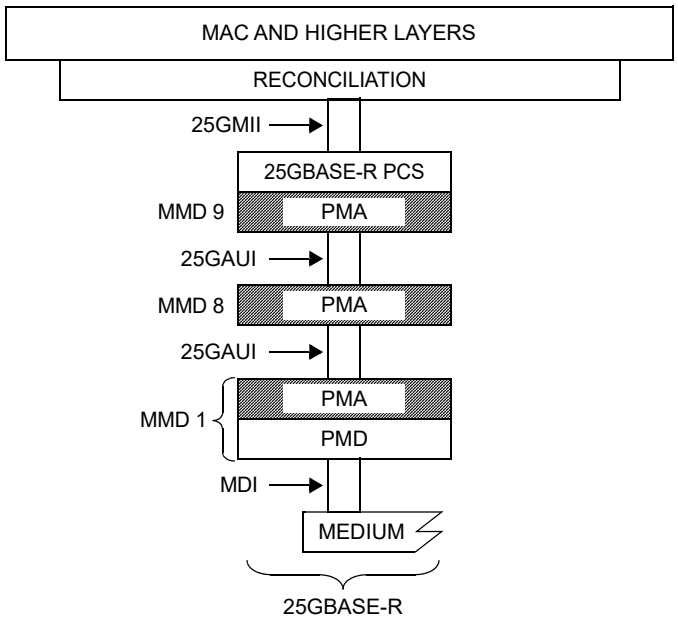


25GAUI = 25 GIGABIT ATTACHMENT UNIT INTERFACE
25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 109C–4—Example single 25GAUI, FEC implemented with PCS



25GAUI = 25 GIGABIT ATTACHMENT UNIT INTERFACE
25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
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Figure 109C–5—Intermediate PMA device for optical module interface

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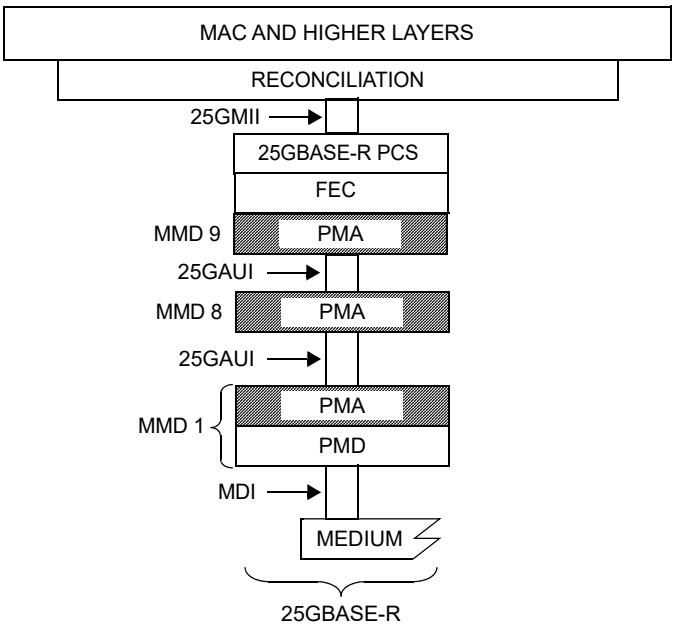

25GAUI = 25 GIGABIT ATTACHMENT UNIT INTERFACE
25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 109C–6—Intermediate PMA device for optical module interface, FEC implemented with PCS

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Annex 110A

(informative)

TP0 and TP5 test point parameters and channel characteristics for 25GBASE-CR and 25GBASE-CR-S

110A.1 Overview

Annex 110A provides information on parameters associated with test points TP0 and TP5 that may not be testable in an implemented system. TP0 and TP5 test points are illustrated in the 25GBASE-CR and 25GBASE-CR-S link block diagram of Figure 110–2. This annex also provides information on channel characteristics.

110A.2 Transmitter characteristics at TP0

The transmitter characteristics at TP0 are constrained at TP0a by 93.8.1, with the exception that the value of linear fit pulse peak (min.) is $0.75 \times v_f$.

110A.3 Receiver characteristics at TP5

The receiver characteristics at TP5 are constrained at TP5a by 93.8.2.

110A.4 Transmitter and receiver differential printed circuit board trace loss

The recommended maximum and minimum printed circuit board trace insertion losses are specified in 92A.4.

110A.5 Channel insertion loss

This subclause provides information on channel insertion losses for the maximum-loss and minimum-loss cabling topologies.

The maximum channel insertion loss associated with the CA-25G-L, CA-25G-S, and CA-25G-N topologies is determined using Equation (110A–1). The channel insertion loss budget at 12.8906 GHz for the CA-25G-L topology is illustrated in Figure 110A–1. Loss budget parameters for all cable topologies are provided in Table 110A–1.

$$IL_{\mathrm{Chmax}}(f) = IL_{\mathrm{Camax}}(f) + 2IL_{\mathrm{Host}}(f) - 2IL_{\mathrm{MatedTF}}(f) \quad \text{(dB)} \qquad (110A–1)$$

for $0.05\ \mathrm{GHz} \le f \le 19\ \mathrm{GHz}$.

where

f	is the frequency in GHz
$IL_{\mathrm{Chmax}}(f)$	is the maximum channel insertion loss between TP0 and TP5

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$IL_{Camax}(f)$ is the maximum cable assembly insertion loss (TP1 to TP4) for each topology (see Table 110–10)
$IL_{Host}(f)$ is the maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (92–8)
$IL_{MatedTF}(f)$ is the nominal insertion loss of the mated test fixture using Equation (92A–4)

The channel insertion loss associated with the 0.5 m topology and a maximum host channel is determined by Equation (110A–2).

$$IL_{Ch0.5m}(f) = IL_{Camin}(f) + 2IL_{Host}(f) - 2IL_{MatedTF}(f) \quad \text{(dB)} \qquad (110A–2)$$

for 0.05 GHz ≤ f ≤ 19 GHz.

where
f is the frequency in GHz
$IL_{Ch0.5m}(f)$ is the channel insertion loss between TP0 and TP5 representative of a 0.5 m cable assembly and a maximum host channel
$IL_{Camin}(f)$ is the minimum cable assembly insertion loss (TP1 to TP4) given in Equation (92–26) and illustrated in Figure 92–12
$IL_{Host}(f)$ is the maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (92–8)
$IL_{MatedTF}(f)$ is the nominal insertion loss of the mated test fixture using Equation (92A–4)

The loss budget parameter values at 12.8906 GHz are provided in Table 110A–1.

Table 110A–1—Cable insertion loss budget values at 12.8906 GHz

Parameter	CA-25G-L	CA-25G-S	CA-25G-N	Units
IL_{Chmax}	35	29	28.02	dB
IL_{Camax}	22.48	16.48	15.50	dB
$IL_{Ch0.5m}$	20.52			dB
IL_{Camin}	8			dB
IL_{Host}	9.85			dB
$IL_{MatedTF}$	3.59			dB

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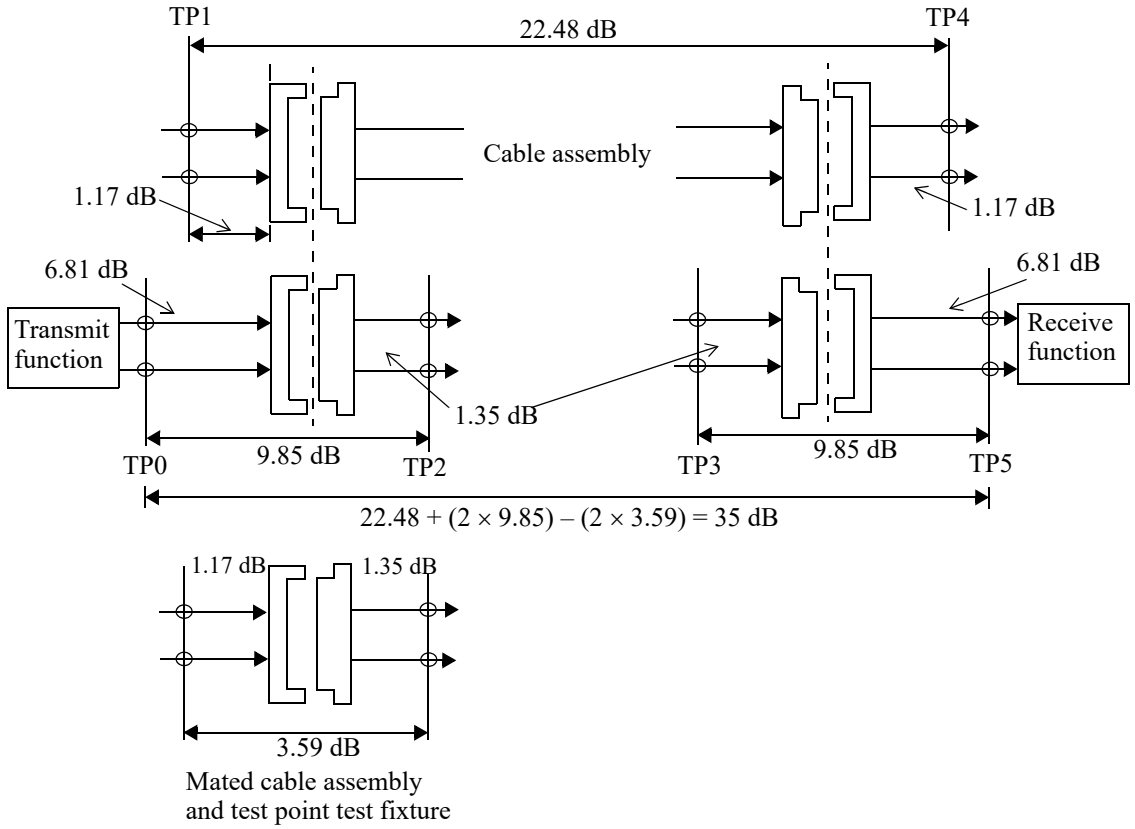

NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Figure 110A–1—35 dB channel insertion loss budget at 12.8906 GHz

110A.6 Channel return loss

The recommended return loss of the 25GBASE-CR and 25GBASE-CR-S channels is specified in 92A.6.

110A.7 Channel Operating Margin (COM)

The Channel Operating Margin (COM) for the channel between TP0 and TP5, computed using the procedure in 93A.1 and the parameters in Table 110–11, is recommended to be greater than or equal to the Channel Operating Margin (min.) value in Table 110–11 for the cable assembly type being used.

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Annex 110B

(normative)

Test fixtures for 25GBASE-CR, 25GBASE-CR-S, and 25GAUI C2M

110B.1 Test fixtures

Transmitter and receiver measurements at TP2 or TP3 for 25GBASE-CR and 25GBASE-CR-S PHYs in an SFP28 host form factor (see 110C.2.1), and at TP1a or TP4a for the 25GAUI C2M host (see 109B.2), are made utilizing the test fixture specified in 110B.1.1. Transmitter and receiver measurements at TP2 or TP3 for 25GBASE-CR and 25GBASE-CR-S PHYs in a QSFP28 host form factor (see 110C.2.2) are made utilizing the test fixture specified in 92.11.1.

Cable assembly measurements for the SFP28-SFP28 form factor (see 110C.3.1) are made between TP1 and TP4 with cable assembly test fixtures as specified in 110B.1.2 on both ends. Cable assembly measurements for the QSFP28-QSFP28 form factor (see 110C.3.2) are made between TP1 and TP4 with cable assembly test fixtures as specified in 92.11.2 on both ends. Cable assembly measurements for the QSFP28-4×SFP28 form factor (see 110C.3.3) are made between TP1 and TP4 with a cable assembly test fixture as specified in 110B.1.2 for each connector on the SFP28 end, and with a cable assembly test fixture as specified in 92.11.2 for the QSFP28 end.

The test fixtures are specified in a mated state to enable connections to measurement equipment. The reference insertion loss of the mated test fixtures is 3.59 dB (see 110A.5). The requirements in the referenced subclauses are not the MDI connector specifications for an implemented design.

110B.1.1 SFP28 TP2 or TP3 test fixture

The TP2 or TP3 test fixture, also known as Host Compliance Board (HCB), is required for measuring the transmitter specifications in 110.7.2 at TP2 and the receiver return loss at TP3. The TP2 and TP3 test points are illustrated in Figure 110–2.

This test fixture is also required for verifying 25GAUI C2M host output characteristics in 109B.3.1 at TP1a and host input characteristics in 109B.3.3 at TP4a. The TP1a and TP4a test points are illustrated in Figure 83E–4.

The test fixture printed circuit board reference insertion loss is given in Equation (92–34). The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the host measurements.

110B.1.2 SFP28 Cable assembly test fixture

The cable assembly test fixture, also known as Module Compliance Board (MCB), is required for measuring the cable assembly specifications in 110.10 at TP1 and TP4. The TP1 and TP4 test points are illustrated in Figure 110–2.

This test fixture is also required for verifying 25GAUI C2M module output characteristics in 109B.3.2 at TP1 and module input characteristics in 109B.3.4 at TP4. The TP1 and TP4 test points are illustrated in Figure 83E–5.

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The test fixture printed circuit board reference insertion loss is given in Equation (92–35). The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the cable assembly or module measurements.

110B.1.3 SFP28 Mated test fixtures

The TP2 or TP3 and cable assembly test fixtures are specified in a mated state illustrated in Figure 92–18. The mated test fixtures specifications are listed in 92.11.3.

110B.1.3.1 Mated test fixtures differential insertion loss

The differential insertion loss of the mated test fixtures shall meet the requirements of 92.11.3.1.

The FOM_{ILD} of the mated test fixtures shall meet the requirements of 92.11.3.1.

110B.1.3.2 Mated test fixtures differential return loss

The differential return loss of the mated test fixtures shall meet the requirements of 92.11.3.2.

110B.1.3.3 Mated test fixtures common-mode conversion insertion loss

The common-mode conversion insertion loss of the mated test fixtures shall meet the requirements of 92.11.3.3.

110B.1.3.4 Mated test fixtures common-mode return loss

The common-mode return loss of the mated test fixtures shall meet the requirements of 92.11.3.4.

110B.1.3.5 Mated test fixtures common-mode to differential mode return loss

The common-mode to differential mode return loss of the mated test fixtures shall meet the requirements of 92.11.3.5.

110B.1.3.6 Mated test fixtures integrated near-end crosstalk noise

The integrated near-end crosstalk noise voltage for the disturber near-end crosstalk loss determined according to the method in this subclause shall meet the specification in Table 110B–1.

Table 110B–1—Mated test fixtures integrated near-end crosstalk noise

Parameter	Value	Units
Integrated near-end crosstalk noise voltage	Less than 1.8	mV

Given the disturber near-end crosstalk loss $NEXT_{loss}(f)$ measured over N uniformly spaced frequencies f_n spanning the frequency range 50 MHz to 19 000 MHz with a maximum frequency spacing of 10 MHz, the RMS value of the integrated near-end crosstalk noise is determined using Equation (110B–1) and Equation (110B–2).

The RMS crosstalk noise is characterized at the output of a specified receive filter utilizing a specified transmitter waveform and the measured disturber crosstalk transfer functions. The transmitter and receiver filters

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are used in Equation (110B–1) to define a weighting function to the multiple-disturber crosstalk in Equation (110B–2). The sinc function is defined by $\mathrm{sinc}(x) = \sin(\pi x)/(\pi x)$.

Define the weight at each frequency f_n using Equation (110B–1).

$$W_{nt}(f_n) = (A_{nt}^2/f_b)\mathrm{sinc}^2(f_n/f_b)\left[\frac{1}{1+(f_n/f_{nt})^4}\right]\left[\frac{1}{1+(f_n/f_r)^8}\right] \quad (110B–1)$$

where the equation parameters are given in Table 110B–2.

Note that the 3 dB transmit filter bandwidth f_{nt} is inversely proportional to the 20% to 80% rise and fall time T_{nt}. The constant of proportionality is 0.2365 (e.g., $T_{nt}f_{nt} = 0.2365$; with f_{nt} in hertz and T_{nt} in seconds). In addition, f_r is the 3 dB reference receiver bandwidth, which is set to 18.75 GHz.

The integrated near-end crosstalk noise σ_{nx} is calculated using Equation (110B–2).

$$\sigma_{nx} = \left[2\Delta f\sum_n W_{nt}(f_n)10^{-NEXT_{loss}(f_n)/10}\right]^{1/2} \quad (110B–2)$$

where Δf is the uniform frequency step of f_n.

The total integrated near-end crosstalk noise for the mated test fixture is computed using the parameters shown in Table 110B–2.

Table 110B–2—Mated test fixture integrated near-end crosstalk noise parameters

Description	Symbol	Value	Units
Symbol rate	f_b	25.78125	GBd
Near-end disturber peak differential output amplitude	A_{nt}	600	mV
Near-end disturber 20% to 80% rise and fall times	T_{nt}	9.6	ps

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110B.2 Protocol implementation conformance statement (PICS) proforma for Annex 110B, Test fixtures for 25GBASE-CR, 25GBASE-CR-S, and 25GAUI C2M[305]

110B.2.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 110B, Test fixtures for 25GBASE-CR, 25GBASE-CR-S, and 25GAUI C2M shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

110B.2.2 Identification

110B.2.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

110B.2.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 110B, Test fixtures for 25GBASE-CR, 25GBASE-CR-S, and 25GAUI C2M
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[305] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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110B.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
HTF	TP2 or TP3 test fixture	110B.1.1		O	Yes [ ] No [ ]
CATF	Cable assembly test fixture	110B.1.2		O	Yes [ ] No [ ]

110B.2.4 PICS proforma tables for test fixtures for 25GBASE-CR, 25GBASE-CR-S, and 25GAUI C2M

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Mated test fixtures insertion loss	110B.1.3.1	IL and FOM_{ILD} meet the requirements of 92.11.3.1	M	Yes [ ]
TF2	Mated test fixtures differential return loss	110B.1.3.2	Meets the requirements of 92.11.3.2	M	Yes [ ]
TF3	Mated test fixtures common-mode conversion insertion loss	110B.1.3.3	Meets the requirements of 92.11.3.3	M	Yes [ ]
TF4	Mated test fixtures common-mode return loss	110B.1.3.4	Meets the requirements of 92.11.3.4	M	Yes [ ]
TF5	Mated test fixtures common-mode to differential mode return loss	110B.1.3.5	Meets the requirements of 92.11.3.5	M	Yes [ ]
TF6	Mated test fixtures integrated near-end crosstalk noise	110B.1.3.6	Meets the requirements of 110B.1.3.6	M	Yes [ ]

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Annex 110C

(normative)

Host and cable assembly form factors for 25GBASE-CR and 25GBASE-CR-S PHYs

110C.1 Overview

This annex describes form factors for the three cable assemblies specified in 110.10 and for hosts with either 25GBASE-CR or 25GBASE-CR-S Physical Layers.

Hosts have two specified MDI connectors, single-lane (SFP28, specified in 110.11.1) and multi-lane (QSFP28, specified in 92.12). This creates two host interface types and three cable assembly types with different combinations of the connectors at each end. These host and cable assembly types are referred to as form factors, distinguishing both the host receptacle (MDI) and the cable assembly plug.

Cable assemblies have three sets of electrical specifications, denoted CA-25G-L, CA-25G-S, and CA-25G-N, as specified in 110.10. The CA-25G-L specifications are based on a single lane of 100GBASE-CR4 cable assembly (see 92.10), enabling a 5 m length, and are compatible with 25GBASE-CR PHYs that operate in RS-FEC mode. The CA-25G-S specifications enable a shorter length of 3 m with lower loss than CA-25G-L, and are required for compatibility with 25GBASE-CR or 25GBASE-CR-S PHYs that operate in BASE-R FEC mode. The CA-25G-N specifications enable a shorter length of 3 m with lower loss than CA-25G-S, and are required for compatibility with 25GBASE-CR or 25GBASE-CR-S PHYs that operate in no-FEC mode.

The possible combinations of host form factors, cable assembly form factors and lengths are summarized in Table 110C–1.

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Table 110C–1—Host and cable assembly combinations

Cable assembly form factor	Cable assembly type	Host, first end	Hosts, second end	Length[a]	FEC modes supported[b]
SFP28 to SFP28 (see 110C.3.1)	CA-25G-L	One, SFP28 form factor (see 110C.2.1)	One, SFP28 form factor (see 110C.2.1)	5 m	RS-FEC
	CA-25G-S			3 m	RS-FEC BASE-R FEC
	CA-25G-N			3 m	RS-FEC BASE-R FEC no FEC
QSFP28 to QSFP28 (see 110C.3.2)	CA-25G-L	One, QSFP28 form factor (see 110C.2.2)	One, QSFP28 form factor (see 110C.2.2)	5 m	RS-FEC
	CA-25G-S			3 m	RS-FEC BASE-R FEC
	CA-25G-N			3 m	RS-FEC BASE-R FEC no FEC
QSFP28 to 4×SFP28 (see 110C.3.3)	CA-25G-L	One, QSFP28 form factor (see 110C.2.2)	Four, SFP28 form factor (see 110C.2.1)	5 m	RS-FEC
	CA-25G-S			3 m	RS-FEC BASE-R FEC
	CA-25G-N			3 m	RS-FEC BASE-R FEC no FEC

[a]Indicates the achievable length of compliant cable assemblies. It may be possible to construct compliant cable assemblies longer than indicated. Length of the cable assembly does not imply compliance to specifications.
[b]FEC mode is selected through Auto-Negotiation (Clause 73). See 110.6.

110C.2 Host form factors

110C.2.1 SFP28 host form factor

A host may use the SFP28 receptacle specified in 110.11.1 as the MDI for each 25GBASE-CR or 25GBASE-CR-S PHY. This is referred to as an SFP28 host form factor.

A SFP28 form factor host can form a single 25 Gb/s link to either another SFP28 form factor host, using a SFP28 to SFP28 form factor cable assembly (see 110C.3.1), or a QSFP28 form factor host (see 110C.2.2), using a QSFP28 to 4×SFP28 form factor cable assembly (see 110C.3.3).

110C.2.2 QSFP28 host form factor

A host may use the QSFP28 receptacle specified in 92.12 as the MDI for up to four 25GBASE-CR or 25GBASE-CR-S PHYs. This is referred to as a QSFP28 host form factor.

A QSFP28 form factor host can form up to four 25 Gb/s links to either another QSFP28 form factor host, using a QSFP28 to QSFP28 form factor cable assembly (see 110C.3.2), or to separate SFP28 form factor hosts (see 110C.2.1) using a QSFP28 to 4×SFP28 form factor cable assembly (see 110C.3.3).

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110C.3 Cable assembly form factors

110C.3.1 SFP28 to SFP28 cable assembly form factor

The SFP28 to SFP28 cable assembly has SFP28 plugs, specified in 110.11.1, on both ends. It may be used to connect two SFP28 form factor hosts (see 110C.2.1) with a single 25 Gb/s link. The cable assembly is illustrated in Figure 110C–1.

The electrical characteristics of a cable assembly for this form factor are specified in 110.10, using the definitions in 110.10.7.2.1.

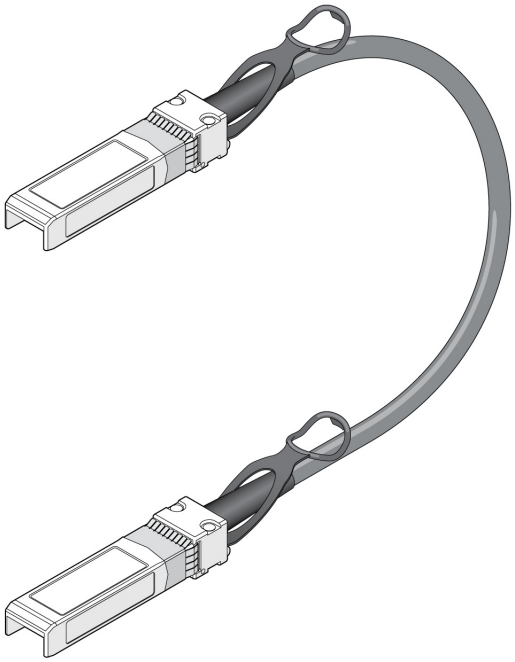

Figure 110C–1—SFP28 to SFP28 cable assembly

110C.3.2 QSFP28 to QSFP28 cable assembly form factor

The QSFP28 to QSFP28 cable assembly has QSFP28 plugs, specified in 92.12, on both ends. It may be used to connect two QSFP28 form factor hosts (see 110C.2.2) with up to four 25 Gb/s links. The cable assembly is illustrated in Figure 110C–2.

The electrical characteristics of a cable assembly for this form factor are specified in 110.10, using the definitions in 110.10.7.2.4.

110C.3.3 QSFP28 to 4×SFP28 cable assembly form factor

The QSFP28 to 4×SFP28 cable assembly has a QSFP28 plug as specified in 92.12 on one end, and four SFP28 plugs as specified in 110.11.1 on the other end. It may be used to connect a QSFP28 form factor host (see 110C.2.2) to up to four SFP28 form factor hosts (see 110C.2.1) with one 25 Gb/s link to each SFP28 host. The cable assembly is illustrated in Figure 110C–3.

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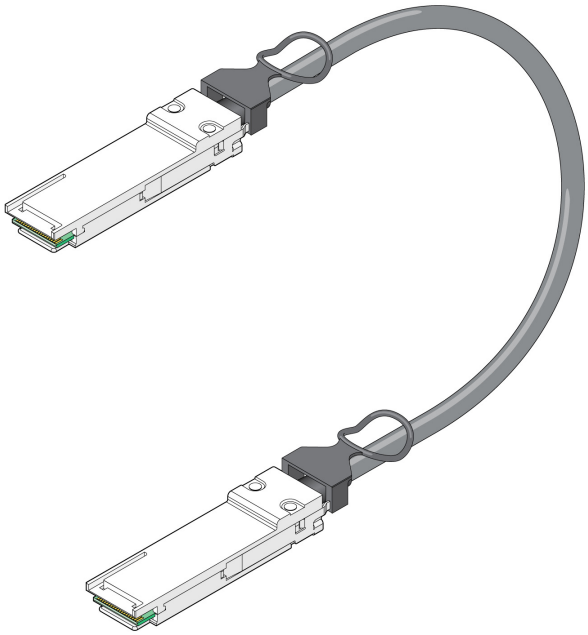

Figure 110C–2—QSFP28 to QSFP28 cable assembly

The electrical characteristics of a cable assembly for this form factor are specified in 110.10, using the definitions in 110.10.7.2.2 and 110.10.7.2.3.

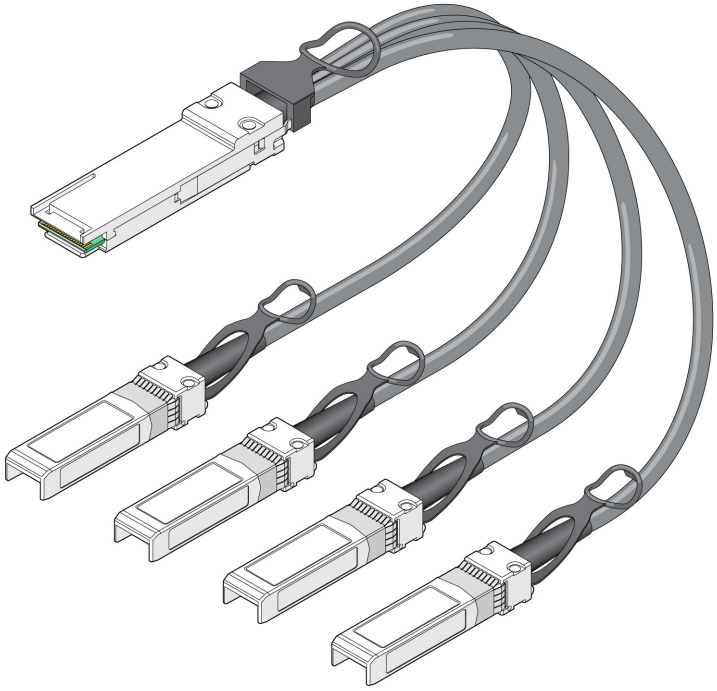

Figure 110C–3—QSFP28 to 4×SFP28 cable assembly

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Annex 113A

(informative)

Description of cable clamp and test setup

113A.1 Overview

This annex describes an example of a cable clamp and a representative methodology that should be used in common-mode noise rejection, rejection of external EM fields, or similar MultiGBASE-T receiver tests using EM clamp injection techniques, which are used to determine the sensitivity of the PMA receiver to external EM fields introduced by the cabling and interconnect system. Variations of this methodology may also be useful for other testing as applicable for design and development purposes. Refer to the receiver specifications of the PHY under test for specific impairments, impairment source power levels, and relevant frequency ranges.

113A.2 Description of cable clamp

NOTE—The larger inner diameter clamp is described here; see Annex 40B for the description of an alternate clamp for use with smaller diameter cable types.

As shown in Figure 113A–1 and Figure 113A–2 the clamp is 300 mm long, 75 mm wide, 78 mm high with a center opening of 9.53 mm (0.375 in). The clamp consists of two halves that permit the insertion of a cable into the clamp.

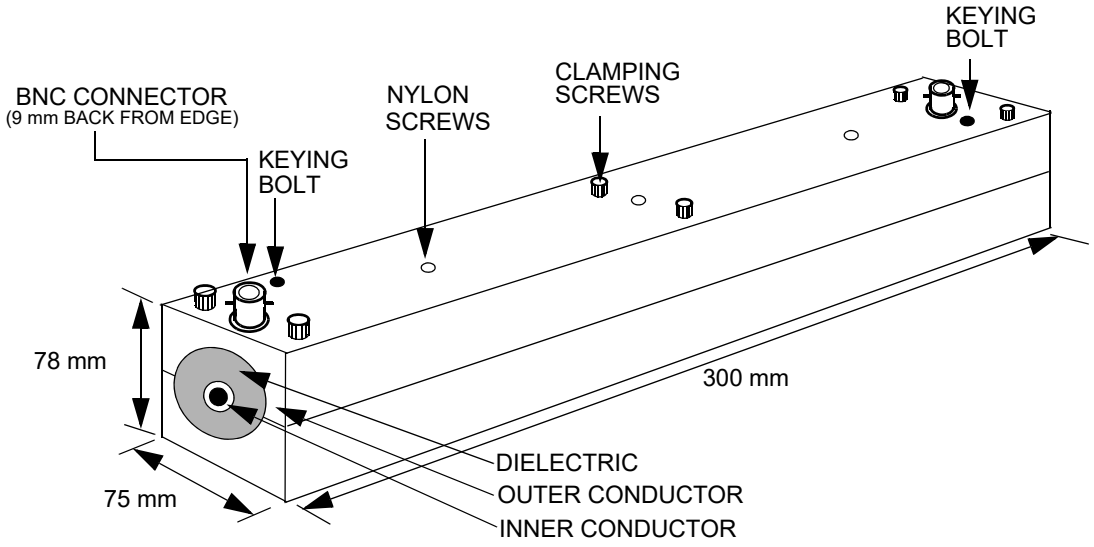

Figure 113A–1—Cable clamp

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The clamp has a copper center conductor and an aluminum outer conductor with a high density polyethylene dielectric. The following is a review of the construction and materials of the clamp:

a) *Inner conductor*—Copper tubing with an inner diameter of 9.53 mm (0.375 in) and an outer diameter of 12.7 mm (0.50 in).

b) *Outer conductor*—Aluminum bar that is 300 mm long and approximately 78 mm by 75 mm. The bar is milled to accept the outer diameter of the dielectric material.

c) *Dielectric*—High density polyethylene (residual, TypeF) with dielectric constant of 2.32. The hollow cylinder has an outside diameter of 45 mm and an inner diameter that accepts the outside diameter of the copper inner conductor.

d) *Connectors*—BNC connectors are located 9 mm (0.39 in) from each end of the clamp and are recessed into the outer conductor. The center conductor of the connector is connected to the inner conductor as shown in Figure 113A–2.

e) *Clamping screws*—Six screws are used to connect the two halves of the clamp together after the cable has been inserted. Although clamping screws are shown in Figure 113A–1, any clamping method may be used that ensures the two halves are connected electrically and permits quick assembly and disassembly.

f) *Nylon screws*—Used to align and secure the inner conductor and dielectric to the outer conductor. The use and location of the screws is left to the manufacturer.

g) *Keying bolts*—Two studs used to align the two halves of the clamp

The inner conductor on the bottom half of the clamp extends slightly (~ 0.1 mm) above the dielectric to ensure there is good electrical connection with the inner conductor of the top half of the clamp along the full length of the conductor when the two halves are clamped together.

The electrical parameters of the clamp between 1 MHz and 2000 MHz are summarized in Table 113A–1.

Table 113A–1—Cable clamp electrical parameters (1 MHz to 2000 MHz)

Frequency range	Insertion loss	Return loss
1 MHz to 250 MHz	< 0.2 dB	> 20.0 dB
250 MHz to 500 MHz	< 1.0 dB	> 7.0 dB
500 MHz to 1000 MHz	< 3.5 dB	> 3.5 dB
1000 MHz to 2000 MHz	< 15.0 dB	> 1.0 dB

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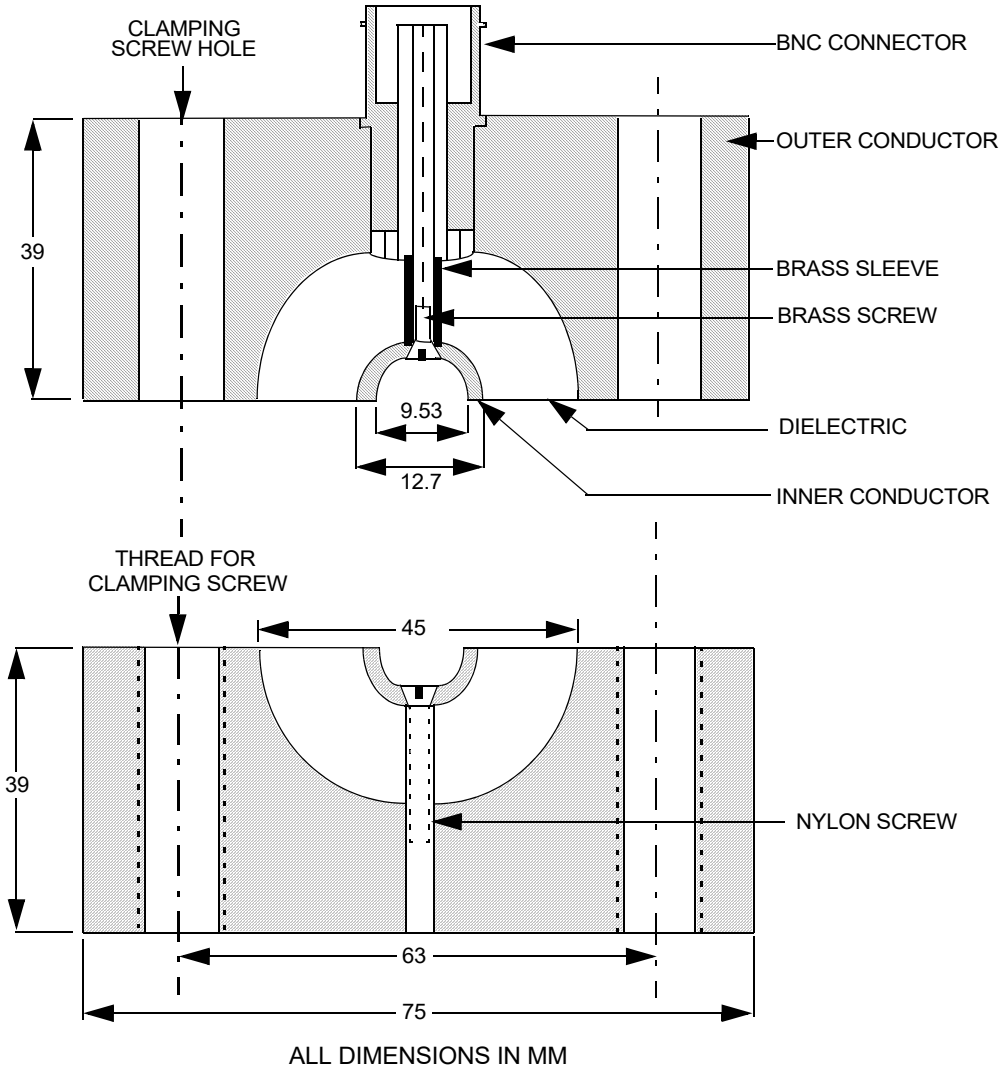

Figure 113A–2—Cross-section of cable clamp

113A.3 Cable clamp measurement, calibration, and validation

In order to ensure the cable clamp is operating correctly, the following electrical measurement, calibration, and validation procedures are provided and should be completed prior to conducting the test described in 113A.4 and illustrated in Figure 113A–4. Note that other methods are allowed providing they can demonstrate equivalent results to the method described in this annex.

Cable clamp electrical measurement—The clamp should be tested to ensure the insertion loss and return loss are as specified in Table 113A–1. Electrical parameters of the clamp are measured between the source connections and without cabling (that is, no cabling inserted in the clamp inner conductor).

Cable clamp calibration—Prior to making validation measurements or performing the test described in 113A.4, the cable clamp should be tested without the cable inserted to determine the variation of the signal generator voltage with frequency at the output of the clamp. The signal generator output should be adjusted to the specified signal power (for example, 6 dBm for 40GBASE-T) at 20 MHz on the signal sensor. The

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signal generator output frequency is swept incrementally from 1 MHz to 2000 MHz with a step size that should not exceed 1% of the preceding frequency value. When the frequency is varied from 1 MHz to 2000 MHz, the measured power should not vary more than ±10%. If the power varies more than ±10%, then a correction factor may be applied at each measurement frequency. If used, the signal power correction factor should not result in common-mode and differential-mode voltages that exceed the limits defined in Table 113A–2.

Cable clamp validation—This validation procedure is provided to verify proper operation of the test setup before performing any tests. In contrast to the clamp electrical measurement, the cable clamp validation test procedure uses the clamp with cabling that meets the PHY link segment specifications inserted into the clamp.

The validation test hardware consists of the following:

a) Transmitter/receiver—A link partner system, configured for the data rate being evaluated, with the transmitter disabled.

b) Breakout fixture—A passive fixture with an MDI connector jack input and individual outputs for each of the 8 signal wires. Wires of pairs not being measured should be terminated to the ground plane with a 50 Ω resistor.

c) Balun—Three ports, laboratory quality with a 100 Ω balanced differential input (Port 1), a 50 Ω unbalanced single-ended output for the differential component (Port 2), and a 50 Ω unbalanced single-ended output for the common-mode component (Port 3):

   Insertion loss (Port 1 to Port 2): < 4 dB (1 MHz to 2000 MHz)

   Return loss (Port 1): > 8 dB (1 MHz to 3 MHz), > 15 dB (3 MHz to 2000 MHz)

   Common-mode rejection (Port 1 to Port 2):
   > 50 dB (1 MHz to 1000 MHz), > 40 dB up to 2000 MHz

   Common-mode return loss (Port 1): > 8 dB (1 MHz to 2000 MHz)

   Note that other devices for detecting differential and common-mode signals may also be used, provided the performance is demonstrated to be equivalent or better. The use of two separate differential and common-mode signal component measurement configurations is permissible provided the preceding specifications are met for each measurement device. The common-mode reference (termination) impedance may be standard specific. The common-mode return loss requirement does not change, but Z_{ref} (common-mode) may be 50 Ω for shielded and 75 Ω for unshielded applications.

d) 50 Ω resistors—Used to terminate unmeasured conductors.

e) Test cable—A 30 m, 4-pair 100 Ω plug-terminated cable that meets the PHY link segment specifications.

f) Chokes (minimum 5)—Wideband ferrite material:

   Inner diameter: Selected to minimize the gap between the ferrite and the test cable.

   Minimum impedance:
   175 Ω @ 100 MHz, 275 Ω @ 250 MHz, 375 Ω @ 500 MHz, 400 Ω @ 1000 MHz

g) Ground plane—Copper sheet or equivalent large enough to span the equipment interface under test and the clamp, including the portion of the cable between the equipment and the chokes (see Figure 113A–3).

h) Signal generator capable of providing a sine wave signal of 1 MHz to 2000 MHz, with adequate test power for adjustments, low harmonic distortion, and the ability to control and monitor power and frequency transitions.

i) Signal sensor and measurement system—Oscilloscopes, power meters, or spectrum analyzers with at least 4000 MHz bandwidth

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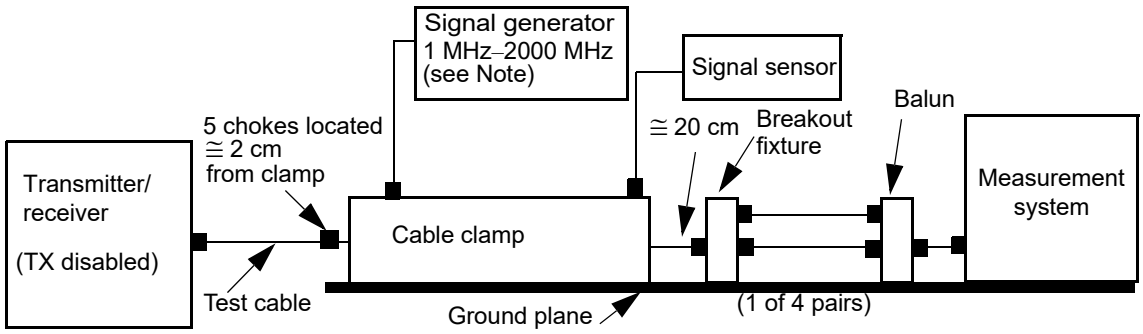

NOTE—The signal generator may include elements needed to control signal generator performance, harmonic distortion, switching transients, and reflections so as not to influence signal level and frequency content at specified levels.

Figure 113A–3—Cable clamp validation test configuration

With the test cable inserted in the cable clamp, a signal generator with a 50 Ω output impedance is connected to one end of the cable clamp and a signal sensor with a 50 Ω input impedance is connected to the other end.

The signal generator should be capable of providing a sine wave signal of 1 MHz to 2000 MHz. The output of the signal generator is adjusted for the specified signal power at 20 MHz on the signal sensor. The remainder of the test is conducted without changing the signal generator voltage. The cable pairs not connected to the balun (or equivalent measurement network) are terminated in a resistor network. The cable clamp, breakout fixture, and balun are in direct contact with the ground plane in a manner consistent with good RF measurement practices. The chokes are placed on the cable, located next to each other and approximately 2.0 cm from the clamp.

The cable between the clamp and the breakout fixture should be positioned straight from the clamp to the breakout port and not contact the ground plane. Any plug shield contacts should mate with the breakout jack shield. The cable between the transmitter and the cable clamp should be installed either in a linear run or wrapped randomly on a cable rack. The cable rack should be at least 3 m from the cable clamp.

The differential-mode and common-mode voltage outputs of the balun and breakout fixture should meet the limits shown in Table 113A–2 over the frequency range 1 MHz to 2000 MHz for each cable pair.

Table 113A–2—Common- and differential-mode output voltages

Frequency (*f*)	Common-mode voltage	Differential-mode voltage
1 MHz to 30 MHz	< 0.1 + 0.97 (f / 30) Vpp	< 2.4 + 19.68 (f / 30) mVpp
30 MHz to 80 MHz	< 1.07 Vpp	< 22 mVpp (–29 dBm)
80 MHz to 250 MHz	< 1.07 – 0.6 (f-80) / 170 Vpp	< 22 mVpp (–29 dBm)
250 MHz to 2000 MHz	< 470mVpp (–2.6 dBm)	< 22 mVpp (–29 dBm)

After the setup has been validated, the clamp, cabling, and choke positions should remain unchanged when performing any receiver tests.

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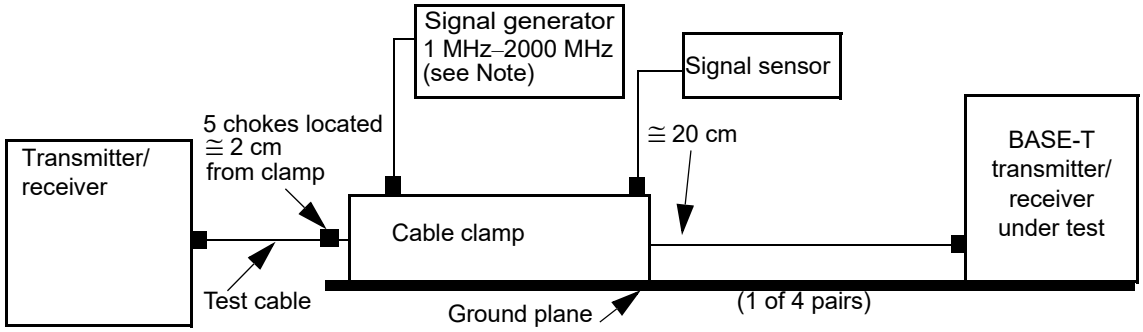
113A.4 Test setup

Cabling up to the maximum specified length that meets the link segment specification for the PHY under test (for example, 113.7 for 40GBASE-T) is connected between two such PHYs and inserted into the cable clamp. The cable should be terminated on each end with an MDI connector plug specified for the PHY under test (for example, 113.8.1 for 40GBASE-T).

The breakout fixture and balun are replaced by the transmitter/receiver under test, with the system port positioned at the original location of the breakout. The clamp should be located a distance of ~20 cm from the receiver port.

As described in the validation setup, the cable clamp and transmitter/receiver under test should be placed on a common ground plane and the system ground of the receiver should be in direct contact with the ground plane. The chassis grounds of all test equipment used should be connected to the ground plane. A signal generator with a 50 Ω impedance is connected to one end of the clamp and measurement equipment with a 50 Ω input is connected to the other end of the clamp. The signal generator should be capable of providing a sine wave signal of 1 MHz to 2000 MHz or other cable-clamp-coupled impairment as specified. See Figure 113A–4.

The output of the signal generator (as calibrated in 113A.3) is applied to the clamp input to simulate the specified impairment (for example, an external electromagnetic field of approximately 3 V/m). As with the calibration procedure, the signal generator output frequency is swept incrementally over the specified frequency range with a step size that should not exceed 1% of the preceding frequency value and with a dwell time at each step of at least 500 ms. The signal generator output should be controlled between steps to minimize any frequency switching transients.



NOTE—The signal generator may include elements needed to control signal generator performance, harmonic distortion, switching transients, and reflections so as not to influence signal level and frequency content at specified levels.

Figure 113A–4—Cable clamp test configuration

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Annex 115A

(informative)

BCH codeword examples

This annex provides example BCH codewords produced by the physical header BCH encoder and the payload BCH encoder defined in Clause 115. This annex presents data in a tabular form to facilitate reading of data. The contents of the tables are transmitted from left to right within each row starting from the top row and ending at the bottom row. The tables contain hexadecimal representations of the data. For the hexadecimal representation, the most significant bit of each hex symbol is transmitted first.

115A.1 Output of the BCH(896, 720) encoder

Table 115A–1 contains an example output codeword of the systematic BCH(896, 720) encoder defined in 115.2.3.3. Because it is a systematic code, the first 720 bits are copied from the input. The input bits were produced by the physical header binary scrambler from the PHD plus CRC16 (see 115.2.3). The last 176 bits are the parity calculated by the BCH encoder.

Table 115A–1—BCH(896, 720) codeword

Input information bits [0:719]			
9549d35f83a4d1cf	412fdaa42887c2b6	48eb825ddbc85982	c54aca778e4ce5fe
15e5075d669edb29	3401304a04590d13	48b2c48692705900	f9488399864faada
197e0569471711bf	d7ce20b4df928911	8360cecc335c56d4	6139
Parity bits [720:895]			
81d34d0b2544af02	374d3fa97bbeb49e	db4e0dea80f7	

115A.2 Output of the BCH(1976, 1668) encoder

Table 115A–2 contains an example output codeword of the systematic BCH(1976, 1668) encoder defined in 115.2.4.3.2.

The BCH codeword in Table 115A–2 corresponds to the first MLCC codeword transmitted in a Transmit Block when a 1000BASE-H based PHY is configured in test mode 1 (see 115.5.1). Because it is a systematic code, the first 1668 bits of the BCH codeword are copied from the input. The input bits were transferred by the MLCC demultiplexer (see 115.2.4.3.1) from the payload data binary scrambler (115.2.4.2) to the BCH encoder. The last 308 bits are the parity calculated by the BCH encoder.

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Table 115A–2—BCH(1976, 1668) codeword

Input information bits [0:1667]			
ef195e8cf2d1db57	6af0c3edeff2a098	0f7de28fa05bbfd9	d87ec8f498c0360a
f6c8b62e0ca0fef7	01b84630e35735bf	cbb886c03f65460e	a23733dd9831a186
41ed6962b4351338	24acd3040ed21d2b	8253abb0c27b31f6	8999be52622aeec7
5fec0b2dc42e9a5b	6292c00fb0e2871d	377dffe020980bc9	ee06e438f1caa337
74fd58ae5c74aee1	3a060fcf15738db1	bb7b49234d884509	0e93a60f503c33ee
02ade8b4fa112019	d48582b78148b898	14abee89cb6816f4	05cd0e611523ebc9
a529246463083af3	9e432b7ba29f89f1	f	
Parity bits [1668:1975]			
47e674016ad23eca	0b1ef6e7f5029901	0087d563401a9440	b5c74236b2dce6a4
d103d1ad3d4c3			

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Annex 119A

(informative)

200GBASE-R and 400GBASE-R PCS FEC codeword examples

This annex provides example PCS FEC codewords produced by the 64B/66B to 256B/257B transcoding, scrambling, pre-FEC distribution, and Reed-Solomon encoding defined in Clause 119. This annex presents data in a tabular form. The contents of the tables are hexadecimal representations of the data and are transmitted to the symbol distribution function from left to right within each row starting from the top row and ending at the bottom row. The most significant bit of each hex symbol is transmitted first.

A constant transmission of Idle control characters is sent to the 256B/257B transcoder resulting in a continuous stream of 257-bit blocks, tx_xcoded<0:256>, shown in hex:

tx_xcoded<0:256> = 0070000000000000078000000000000007800000000000000780000000000000

In this example, an alignment marker is due for insertion and the scrambler seed [see Equation (49–1)] just before the 257-bit block was scrambled was:
S<0:57> = 24E6959D0FA5DBD

After scrambling and inserting the alignment marker group am_mapped, the variable tx_scrambled_am is produced as shown in Table 119A–1 for 200GBASE-R and Table 119A–2 for 400GBASE-R. In these tables, italicized characters are alignment markers and bold characters are padding for the alignment markers. Just prior to insertion, the seed of the PRBS9 generator used for padding was P<0:8> = 0x100.

After distributing into two message blocks, and PCS FEC encoding, codewords c_A and c_B are produced. c_A and c_B may be illustrated as two 5440-bit representations cx_A and cx_B as follows:

For all i=0 to 543:
cx_A <(10i+9):(10i)> = c_A<i>
cx_B <(10i+9):(10i)> = c_B<i>

The expanded codewords are shown in Table 119A–3 and Table 119A–4 for 200GBASE-R and Table 119A–5 and Table 119A–6 for 400GBASE-R (bold characters are parity).

The example codewords have tx_am_sf<2:0> = {0,0,0}.

Table 119A–1—Example tx_scrambled with alignment marker group for 200GBASE-R

Index <*i*:*j*>	tx_scrambled_am<*i*:*j*>
<0:256>	*0B2ACAB2ACAB2ACAB2ACA9324C9324C9324C9324C942108C22C90A2697A225314*
<257:513>	*1AA6A9BA6E98A629AB6ADAB6ADAB6ADAB6ADAB6AD9BE6D9B26DDB76E5B46DEF365BDF1*
<514:770>	*0C42A493A18D4F681A02679E4456DD1C98CFC35417A7B1742DB5334A1BD2041B7*
<771:1027>	*07ACE48B2FD61333BFB75C3DC524204CEBD0955D1B04967A***00846139561BD3720**
<1028:1284>	**08CCD177010357E8DAB65B6F9160968075341AC958CFC828D8372DC66242646D8**

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Table 119A–1—Example tx_scrambled with alignment marker group for 200GBASE-R *(continued)*

Index <*i*:*j*>	tx_scrambled_am<*i*:*j*>
<1285:1541>	026FEAA09736E915DD54C5F7E600ECFCBD7D7C207941C5D7182D8B95FE412ED12
<1542:1798>	014CCE446415F10CDC7BBAFB1CC4B442EF5737AFB4F3BED48D240C9095F5FD3A6
<1799:2055>	10219FBE135EDE0B73C15238C150007886562E30A50CB27DF341954DB8CA1C564
<2056:2312>	16598EAD3C229838CB9BEE7F793139EE1F89FDAD9071687CBEDF89B4E527A03CD
<2313:2569>	1C2044F260A85EE6EB506C25E7C1196298548B4B3576F1B084C83F2E3CB5FC5F6
<2570:2826>	1C9D40EF27471536FE9EB5E3BC3870D46755080EA6D29F09CF8FA697A738DD3EC
<2827:3083>	193FA8A7675CE03706A49019B93544E19DD66CE78E6A94BEBD07ECCAE7DF2076D
<3084:3340>	081919F234C00959E5AFFC9F83C909805378B5F3F2E4917F3E48B5DE4758CEA42
<3341:3597>	1D378C193CDD3D0F781ABC3529BF76A66B7C73A7230B517D96DAFF6A39F9EA9B6
<3598:3854>	05E852B6917E9D1410B6509E778629A516FB2BCEABA79F12241DBC94CDAFFFF02
<3855:4111>	1D98F5991744C9FC5393EFD6299558CB4F28DF3BF3C8636DBA505E3A296C7BD2E
<4112:4368>	00FAACFBFDBC1C29CED046C73C9AAAFE3DE8849ADAD16E864814846BB8CB889AD
<4369:4625>	04D11BFE0E8DEF5ECFDBE45D1EE4607B4B44DF874F8E976DD828FCFD38158A8FF
<4626:4882>	00EE28B635049BA9506024BA13862A1D6BAE22D0DB5DDB1F4DBE0F80E9EDBBCC6
<4883:5139>	1CD0769BC76446DA04136E7C6D19905DFB81AC3BFD931426901028D729E529F5A
<5140:5396>	14C3FF33243D7D2B5137B63359FD25B82CDE769D0F10D2E60A0386E60820BE8F4
<5397:5653>	1993F1FE2D6C60459F26A74BD0265C2959899E4C5B24196AFD51DB241CFCF9091
<5654:5910>	18EE61EA5A0D584DE8AC602618874BBA60A907115513BC960F6BE32C68F1F2458
<5911:6167>	042251FD6EF16662F5C99D9779B20B865B1401C96034C99550401BCB2792E5638
<6168:6424>	0CE3AE06476B769F33E5577CE4BA6D62071CABE3EA9561D6077FD23909568A25A
<6425:6681>	1BBC46AC3DF26A5BB0EA4FDBCBFB42738A84007619C594E24AB396AFB5F05FBFF
<6682:6938>	076C96A407E106D494AA6B0C5168E1F335B812D7BC530CE8C6FC13F6C54EC2165
<6939:7195>	056CC06AFE2BD2A9894C4D1AD9E632F861208AD3894EFF0DE8B0291C486EA3281
<7196:7452>	094534A897031E6307E32C1906C85E99CD4696FC818D2B5EAF26A576DE149AE12
<7453:7709>	085AE9048EDDC5401827FAA937411FF35C10287236FFDC87E7E7E334B038EE3F9
<7710:7966>	014179E0E2359D3B961A1302FA4B7AC384F0564B15D7504DADBE3C65EE8F6F13A
<7967:8223>	08D40F4B092621CCA4919E81D0C15014204622D41814894DBE389C149E5E2257A
<8224:8480>	0E4772C6718DA5361ABFAAD60F5C32D304740DE671045CDAD6617125F4BBF457D
<8481:8737>	071A7D2B02B41F13971A22FE8A29F0A03C1CEC43CA0411D7872F18D12E0A2BD06
<8738:8994>	1344403844B360B4A61968D045941FF821511C2E95455C300EED811D314AD7018
<8995:9251>	0275A5C4A36F6B8B13AFAFFFCDFDBD9B13F00488494886CDEB13B31FC9F7941CF
<9252:9508>	168E51B4882712DECD042307B45EBFF549E07C92FD3C3DAB5A655CC419BBA06F1
<9509:9765>	02B88C8D61954691B36009D54637647F750E1B99733303EA76E0805B182D3B9D0
<9766:10022>	1C50996262A56FB5D7631247C2F52B5150C17BA61FEB56A37BE13F2ABC226AA0A
<10023:10279>	1A1F1CF493816E6F69603FF83E895BA5AFF2ECB8E9090CB28AE93C232756FEDAF

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Table 119A–2—Example tx_scrambled with alignment marker group for 400GBASE-R

Index <*i*:*j*>	tx_scrambled_am<*i*:*j*>
<0:256>	*0B2ACAB2ACAB2ACAB2ACAB2ACAB2ACAB2ACAB2ACA9324C9324C9324C9324C9324*
<257:513>	*19264992649926499 1B421184592144D2F445014D517435064290242CA669AA6A*
<514:770>	*1374DD314C5354D5354DD314C5334DD356D5B56D5B56D5B56D5B56D5B56D5B56D*
<771:1027>	*0B6ADAB66F9B96C9B76DDB96D1B76D1BF6E1B26CDBD6D9B8B8196F7C588549274*
<1028:1284>	*063530AC615723489C7AA5333D91C8099E79115B747311F9C333AE74ADEAEFBF9*
<1285:1541>	*1D7E1AA0BD3D8BA16DAAB83C86F1C6A4C3D959E99A91DE9020DB9EB3922FA719F*
<1542:1798>	*036FA98F2DAB3957B8B0999DFDBAE1EE2924183BB157354862E1154102985E84A*
<1799:2055>	*15D1B04967A30D5178CE48F0569849A***00846139561BD37228569FB24B7E4D4CC0**
<2056:2312>	**08CCD177010357E8DAB65B6F9160968075341AC958CFC828D8372DC66242646D8**
<2313:2569>	**026FEAA09736E915DD54C5F7E600ECFCBD7D7C207941C5D7182D8B95FE412ED12**
<2570:2826>	**014CCE446415F10CDC7BBAFB1CC4B442EF5737AFB4F3BED48D240C9095F5FD3A6**
<2827:3083>	**10219FBE135EDE0B73C15238C150007886562E30A50CB27DF341954DB8CA1C564**
<3084:3340>	**16598EAD3C229838CB9BEE7F793139EE1F89FDAD9071687CBEDF89B4E527A03CD**
<3341:3597>	**1C2044F260A85EE6EB506C25E7C1196298548B4B3576F1B084C83F2E3CB5FC5F6**
<3598:3854>	**1C9D40EF27471536FE9EB5E3BC3870D46755080EA6D29F09CF8FA697A738DD3EC**
<3855:4111>	**193FA8A7675CE03706A49019B93544E19DD66CE78E6A94BEBD07ECCAE7DF2076D**
<4112:4368>	**081919F234C00959E5AFFC9F83C909805378B5F3F2E4917F3E48B5DE4758CEA42**
<4369:4625>	**1D378C193CDD3D0F781ABC3529BF76A66B7C73A7230B517D96DAFF6A39F9EA9B6**
<4626:4882>	**05E852B6917E9D1410B6509E778629A516FB2BCEABA79F12241DBC94CDAFFFF02**
<4883:5139>	**1D98F5991744C9FC5393EFD6299558CB4F28DF3BF3C8636DBA505E3A296C7BD2E**
<5140:5396>	**00FAACFBFDBC1C29CED046C73C9AAAFE3DE8849ADAD16E864814846BB8CB889AD**
<5397:5653>	**04D11BFE0E8DEF5ECFDBE45D1EE4607B4B44DF874F8E976DD828FCFD38158A8FF**
<5654:5910>	**00EE28B635049BA9506024BA13862A1D6BAE22D0DB5DDB1F4DBE0F80E9EDBBCC6**
<5911:6167>	**1CD0769BC76446DA04136E7C6D19905DFB81AC3BFD931426901028D729E529F5A**
<6168:6424>	**14C3FF33243D7D2B5137B63359FD25B82CDE769D0F10D2E60A0386E60820BE8F4**
<6425:6681>	**1993F1FE2D6C60459F26A74BD0265C2959899E4C5B24196AFD51DB241CFCF9091**
<6682:6938>	**18EE61EA5A0D584DE8AC602618874BBA60A907115513BC960F6BE32C68F1F2458**
<6939:7195>	**042251FD6EF16662F5C99D9779B20B865B1401C96034C99550401BCB2792E5638**
<7196:7452>	**0CE3AE06476B769F33E5577CE4BA6D62071CABE3EA9561D6077FD23909568A25A**
<7453:7709>	**1BBC46AC3DF26A5BB0EA4FDBCBFB42738A84007619C594E24AB396AFB5F05FBFF**

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Table 119A–2—Example tx_scrambled with alignment marker group for 400GBASE-R *(continued)*

Index <*i*:*j*>	tx_scrambled_am<*i*:*j*>
<7710:7966>	076C96A407E106D494AA6B0C5168E1F335B812D7BC530CE8C6FC13F6C54EC2165
<7967:8223>	056CC06AFE2BD2A9894C4D1AD9E632F861208AD3894EFF0DE8B0291C486EA3281
<8224:8480>	094534A897031E6307E32C1906C85E99CD4696FC818D2B5EAF26A576DE149AE12
<8481:8737>	085AE9048EDDC5401827FAA937411FF35C10287236FFDC87E7E7E334B038EE3F9
<8738:8994>	014179E0E2359D3B961A1302FA4B7AC384F0564B15D7504DADBE3C65EE8F6F13A
<8995:9251>	08D40F4B092621CCA4919E81D0C15014204622D41814894DBE389C149E5E2257A
<9252:9508>	0E4772C6718DA5361ABFAAD60F5C32D304740DE671045CDAD6617125F4BBF457D
<9509:9765>	071A7D2B02B41F13971A22FE8A29F0A03C1CEC43CA0411D7872F18D12E0A2BD06
<9766:10022>	1344403844B360B4A61968D045941FF821511C2E95455C300EED811D314AD7018
<10023:10279>	0275A5C4A36F6B8B13AFAFFFCDFDBD9B13F00488494886CDEB13B31FC9F7941CF

Table 119A–3—RS(544,514) codeword A for 200GBASE-R

Index <*i*:*j*>	cx_A<*i*:*j*>
<5439:5120>	A6A9AA6A9A64992649921486284BD26519565D946D5B56D5B57D936ED8B6CF7EFA842EDE6024F1DB
<5119:4800>	63156BC9A159A5EDB273FD0CCBB63B810BD2EA92401C8F6204458108BF4D44C2D1675209D8331CC8
<4799:4480>	40D556CEEAA30193F3AF9E2E8B43EA7494144FD4767AE467A1D9F9656C125225F1007DEDFCE7100A
<4479:4160>	84474C2BBEA631DA8F34E5832CE9FCE47F0ADD1CE9F2325278204197782B7A662A1B4BF6C844FEB4
<4159:3840>	6F8155CB65AF1EE61D57AE3CA3E74B6399B457AE3B092274729AF1E4A60BD4C4F0ADF3018F39FE78
<3839:3520>	00DA3A7FD18904FB9B2E9832E1EF0FFD999CE031BEBD69C6552F4B672E84F2230D15EACBA247B6D9
<3519:3200>	1FF19A27932706B6A8F273E1376C7ADA74BAAF7FA1C16E72AABDEB2B4424B13A65AF62171EB7D9E2
<3199:2880>	E048B2E3A541AFC1A83FA290552920391C28EAD81B7EDE02EDCED9689A059D98BEEB586FE420214E
<2879:2560>	E5065667D74558D5FE83B711E338380822FC991F0613ED2E999A89E24FD5DBBCE90B3BB490D6A032
<2559:2240>	A5E8311EE4E0E631E0D129376199937B9D0A36934CA0A4F749870EBB71F25524E35A71BE30DF7138
<2239:1920>	8B76B5613EDDBC9FD3390226172B35DF7E8DCD2B10D491ACB499E40478B907D1B0876AD58BDA458B
<1919:1600>	19C61D4729EC1408494C515223C4FC4C34259FED58EAF5290F439D6710A8E4325F8A0E4E2FFE7F31
<1599:1280>	1C27F3D223B942CBE9AF1E46915EDA4C7784BAF092533E630BA006260A9171D2811CE51A763C36AB
<1279:960>	D79968151CD9D0C7D05F8E75282FA7F4651C04DC053AE8F5D2BD516438360C858050208711501800D
<959:640>	518076B85275B5CFFFDBF21124497B336F9CE14E08B69105BCFE8F2A4B872D467EED1E3126189401
<639:320>	62B8970BA6C0DDBDA32D70B4C4A9D691BA115B41F0EB50FAAAAC85ABCE815BFFC45DA5DD09734C97
<319:0>	9337F1A9130B2CF27EA48EB65E77EADCEAB99C502FBC45E7F255A8ADA28CCA6D50F528D5740A36F4

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Table 119A–4—RS(544,514) codeword B for 200GBASE-R

Index <*i*:*j*>	cx_B<*i*:*j*>
<5439:5120>	A6A9AA6A9A6499264992109A2C8A226519565D946D5B56D5B56DBB69DBB66986849163C0BCC51271
<5119:4800>	1FBD07455BC28405E74486BF7C3892732A40D979621AAEC9981DF56AB7B620D706B398629A748DB1
<4799:4480>	FDA9025EABFBF70AF443E098E7442722E6613211EF31B1695EFAFB958926D7ECBF9AB2D06A083380
<4479:4160>	6A5434D0B3B2A14D26B88858EEFA4FEF3C81370BF6F960BC3D3CA155D8360F94644AAC36013F1E3F
<4159:3840>	C9DEE472FE3D438314215B3212F9CBE5FF26E41C562602AEE673559D7CDFBE5B813162523AD3F084
<3839:3520>	D967D24FE7758D784B1ECF30B5614A5BBED394ADDA56FE7C6DA53D11454DF70B26FAAE7CF0494BFE
<3519:3200>	BA26B22E8FF7E65D32C5CFDB10A517DE381BE41EE71B1B263F421ADC2C943B8882C87FDEFF3E8A27
<3199:2880>	4B5FBC7FB6FC41CC54EE637B2304BAA33AD5A37597FE0BC867E0B8FB632063C261DF708C825B169E
<2879:2560>	5AFFE84AA5BD8D6B4BD9172580A33BA0997E3F6B68A5602D43645A3A60AB091F38E2F0582F603023
<2559:2240>	2EC1255527EB6C627D08BF9A3AF66E4DA9880301A9A00E4DA98E530DDBE67DF2EC0BEA5283597D48
<2239:1920>	48A3DF0E565C3DB0B551B81A3491693EBFD49BC05B0AA51B0EED7D6866C67E6E55340C47E552326D
<1919:1600>	F4C121CBFDD14E2574A0A5A0718DA66C0CB2C4095AB276DEC984A09EED8057C2EB3D40DB213F9CD2
<1599:1280>	1DC5083F3534C196903835175D938FBBD1E2B03484649816A0042D12836C3929EEA7711CE52FA835
<1279:960>	98710CF510D6A47BA5F5F954023C5845D0FE0FC2208E12C450580046925AB4F44FFD154B875BB971
<959:640>	5A9033A7DB8D3D7FB36600E48363233F8A72DD6C1C99B18BD155DF097EAD54CC1C09D4AC62AB36B9
<639:320>	BB2EF760CC95C100639D850C8FB4DDF1295854BB6BFD87E48782A3EC919D06B07DABFD1D0245150F
<319:0>	6AFD68CE7558FB5C8911150C62F97B29D912BCA53CCCF26F707B9AF277C6FD62055979796D2B8F85

Table 119A–5—RS(544,514) codeword A for 400GBASE-R

Index <*i*:*j*>	cx_A<*i*:*j*>
<5439:5120>	A6A9AA6A9AA6A9AA6A9A64992649926499264992D886284BD280BA2609026519565D946559565196
<5119:4800>	6D5B56D5B56D5B56D5B57D936ED8B62D876CD9B6077EFA842E86550894ABDE6024F1DBC4598972EA
<4799:4480>	BCD56BC9A11D7D8256A659A5EDB273E5F63E326A3BCCCBB63B3054625443810BD2EA92C331E3C619
<4479:4160>	401C8F61447E7EDCCA66077D56AFED4815C9AFE6D8B691236C7F7A4894AA7ECDCEBC10380639D209
<4159:3840>	48B9904D84BBDC645B57BEBEE96049F5CB27E7ACB40A8A0DE01AA509342C6CB8534AAEA22633BD93
<3839:3520>	3BFF204FC2FD8E502D0F4F285D750D83E51D13AB0DB043C68F7267B51CBF8F70ECC40896DC8CBE72
<3519:3200>	F95FC9B807959988ABB99CD56F5F37EFB6EC4E58D4BEB0FF21F679F490F9DD635A10C7B3FC2D5A52
<3199:2880>	56CFB4E62BB695B79D1BA97F4050533DD2C9BEAB1F1C1653FF6E99AC88A3FDE99B4FB1F3F6C82945
<2879:2560>	F7BE0EFB07B9C6CACB8F9096B308258EF228B01FF7AFCBA189D2C7E71EED3F207F163B58EEC0C02E
<2559:2240>	A8EEB169DD65CF86F319B82E36DAC8D8E09077DCA3009AC4A7569FFE11A96F735ED0F685E96028CE
<2239:1920>	E8265F8CDA9A39540A509936869A2A8267CE3ABC560BD80F08CBB0415749FACB149C42AFE68EBE9B
<1919:1600>	135A6E02C0AA5807906AE384CB74F99F6CB700FA5480D25D52D208FBC295570F642C546E2685255A
<1599:1280>	0FBFFD27F056F2A147C33B6F561BB1DF9B994E0351D95C8F9B7D104470FF3463815D28A958106069
<1279:960>	9B3324B302D6AC9DB6B2A10823B86055E0BACC50F6F847E434C7414E0DCD0D206DA50E4D75DB65E3
<959:640>	2EE470AD0DE1092E04A8812B44A3DB0E7A77A9DCC7194FEA0DA61C433F4435891EE97DBE750C8D16

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Table 119A–5—RS(544,514) codeword A for 400GBASE-R *(continued)*

Index <*i*:*j*>	cx_A<*i*:*j*>
<639:320>	51543380F0881388B114962019A6962D0D13FC4552E1D6EE5CD6A408EAF6237F5FECD980292CD9C8
<319:0>	4FC29E524AC56D33248BE7CBB1EBA5F71F5D872E35E9AFA1B54DB4D1A4FC09E8057F65FBC3E55FD5

Table 119A–6—RS(544,514) codeword B for 400GBASE-R

Index <*i*:*j*>	cx_B<*i*:*j*>
<5439:5120>	A6A9AA6A9AA6A9AA6A9A6499264992649926499264992109A2C8A22ACAC250B426599565D946559765197
<5119:4800>	6D5B56D5B56D5B56D5B59DBB69DBB6FD936BD8766986849163C6A27C7265713CC5127173FAEF6BEF
<4799:4480>	1FBD07455B4F238F0D79E24405E744E62BEDA55386BF7C3892EE19DA30550CAA40D9798A89C6A164
<4479:4160>	621AAEC9A824EC9203458118BB4F4402C1635209D83314CA401576CEEBA30193FFAE9EAE9B4FEB74
<4159:3840>	940447D476FAE46BA3D97965681352E5E1087DED3CC7100984C74C2FBEA631DA8335E5832CEDFCE4
<3839:3520>	3F1ADD1FE9B232567A2041A7782A7AA62A1348F6C874FEB76F8145CB65AF1ED61554AE7CA3EF4B63
<3519:3200>	999453AC3B093278719A71F4AE09D404C0A9F0014F09F279005A3A7FD289C4EB9B2C98F2C1EB0EFD
<3199:2880>	599CE431BEFD79C6542F4B572684F2A32D19EBCB2267BAD81FF1BA2F93274686A4F37361176C78DA
<2879:2560>	749AAB7CA1415E7EA8BD6B3B4026B13A65AF6317DEA7DDE1E0C8B2EBA5412FD1A83DA29055292039
<2559:2240>	5C08E6DB1B3EEE0EEECED94892079D98BEE35A6F6410294FE5866667D64598E5F680B711C33C3A08
<2239:1920>	E2FC9D1E0693FD2E999AC9C24FD4DBFCC90338B490C6AC33A5A8111EE5E0A631E0D229F75199927B
<1919:1600>	1D0A36924C20B4F749870EAB79F355A4E35A72BE70FF713A8B76B5693CDDFC9FD73802E6072736DF
<1599:1280>	7EADC1281094A1A8B599A41478B9075190836BD54BCA458B19862D4729EC9418414E51D233C8FC4C
<1279:960>	F41597EE58EAF5250E435D7710ABE4B27F820C4EEFFE7B331C27F3D623B942CBE1AC1E46815EDB4C
<959:640>	B784B2F192531E6308A04606029071929114E71AB62C36A9D71958111ED9D0D7D45D8E353823A7F4
<639:320>	E53C08DE057AD8F1D0BD114438370C05B05422875160140E51C056BC5075F5CFFBDBF211044D7A33
<319:0>	EFBCE079F39FDD0E6BDD2B8ED1CC0790B29C992D54C852DDD29825193C8CAEE6F675E83ECA4495AD

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Annex 120A

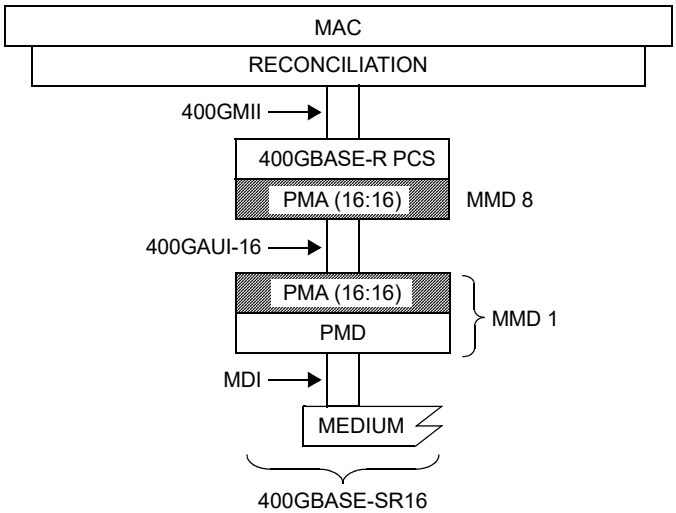
(informative)

200 Gb/s and 400 Gb/s PMA sublayer partitioning examples

The following subclauses provide various partitioning examples. Partitioning guidelines and MMD numbering conventions are described in 120.1.4.

120A.1 Partitioning example supporting 400GBASE-SR16

Figure 120A–1 depicts an example of 400GBASE-SR16 PMA layering with a single 400GAUI-16 chip-to-module interface.



400GAUI = 400 Gb/s ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120A–1—Example 400GBASE-SR16 PMA layering with single 400GAUI-16 chip-to-module interface

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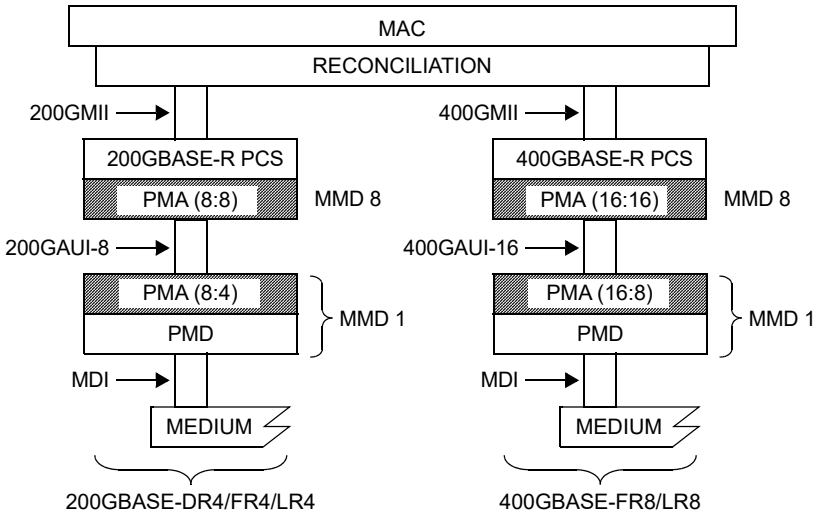
120A.2 Partitioning examples supporting 200GBASE-DR4/FR4/LR4 and 400GBASE-FR8/LR8

Figure 120A–2 depicts an example of 200GBASE-DR4/FR4/LR4 or 400GBASE-FR8/LR8 PMA layering with a single 200GAUI-8 or 400GAUI-16 chip-to-module interface.



200GAUI = 200 Gb/s ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GAUI = 400 Gb/s ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120A–2—Example 200GBASE-DR4/FR4/LR4 or 400GBASE-FR8/LR8 PMA layering with single 200GAUI-8 or 400GAUI-16 chip-to-module interface

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Figure 120A–3 depicts an example of 200GBASE-DR4/FR4/LR4 or 400GBASE-FR8/LR8 PMA layering with a single 200GAUI-4 or 400GAUI-8 chip-to-module interface.

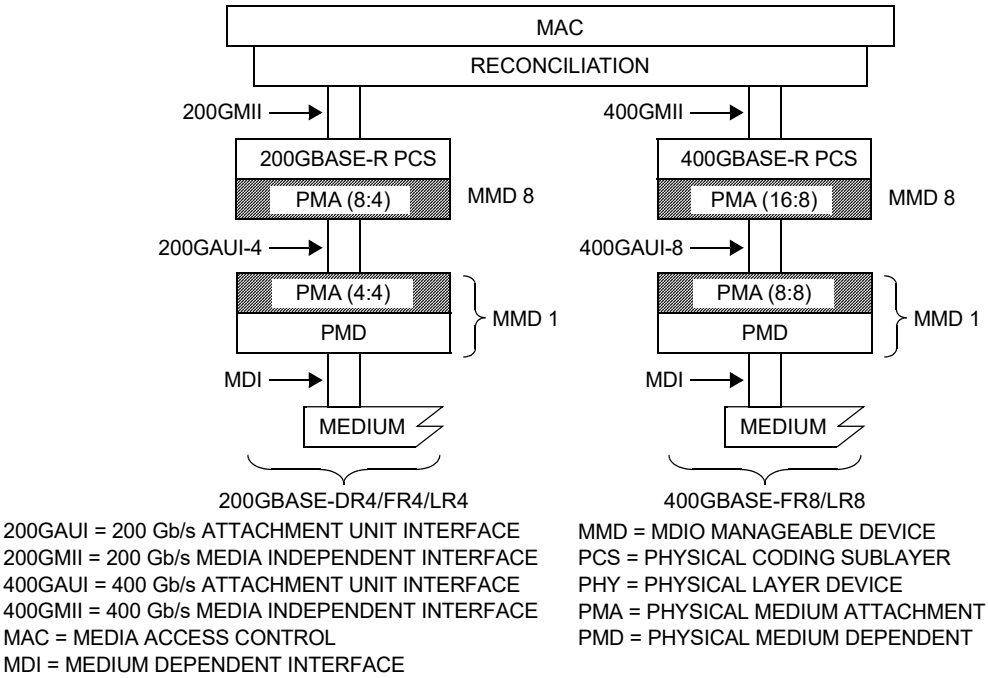

Figure 120A–3—Example 200GBASE-DR4/FR4/LR4 or 400GBASE-FR8/LR8 PMA layering with single 200GAUI-4 or 400GAUI-8 chip-to-module interface

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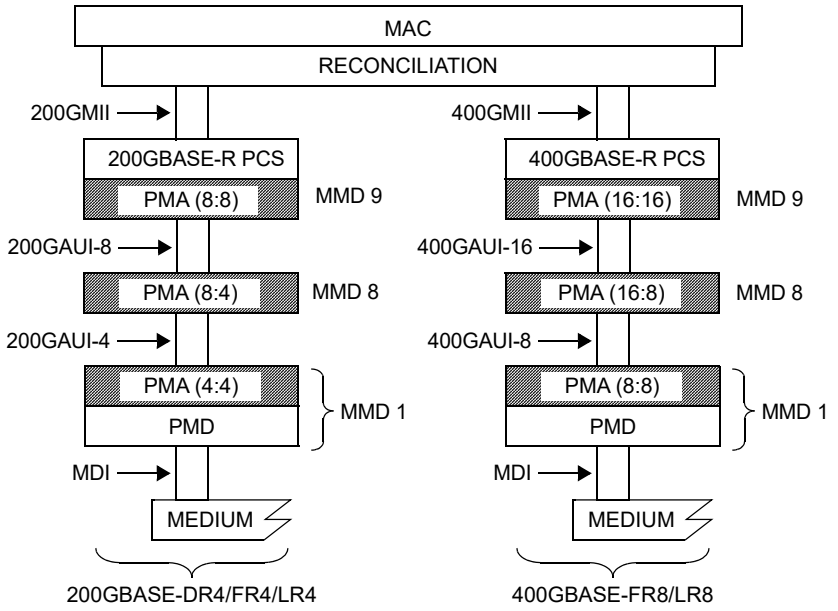
Figure 120A–4 depicts an example of 200GBASE-DR4/FR4/LR4 or 400GBASE-FR8/LR8 PMA layering with 200GAUI-8 or 400GAUI-16 chip-to-chip and 200GAUI-4 or 400GAUI-8 chip-to-module interfaces.



200GAUI = 200 Gb/s ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GAUI = 400 Gb/s ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120A–4—Example 200GBASE-DR4/FR4/LR4 or 400GBASE-FR8/LR8 PMA layering with 200GAUI-8 or 400GAUI-16 chip-to-chip and 200GAUI-4 or 400GAUI-8 chip-to-module interfaces

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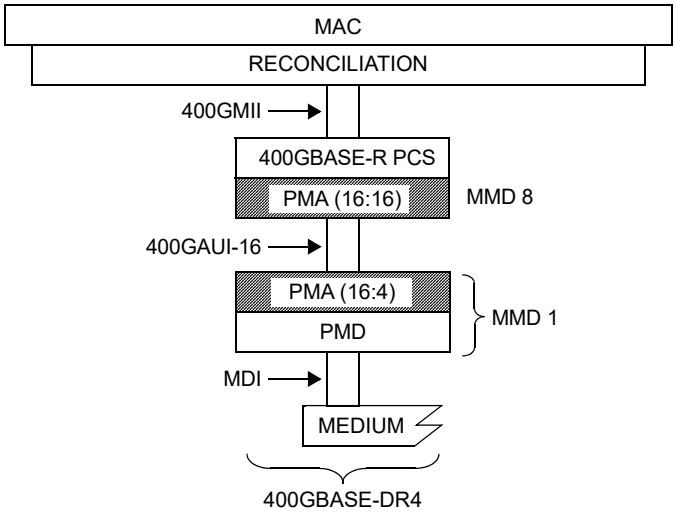
120A.3 Partitioning examples supporting 400GBASE-DR4

Figure 120A–5 depicts an example of 400GBASE-DR4 PMA layering with a single 400GAUI-16 chip-to-module interface.



400GAUI = 400 Gb/s ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120A–5—Example 400GBASE-DR4 PMA layering with single 400GAUI-16 chip-to-module interface

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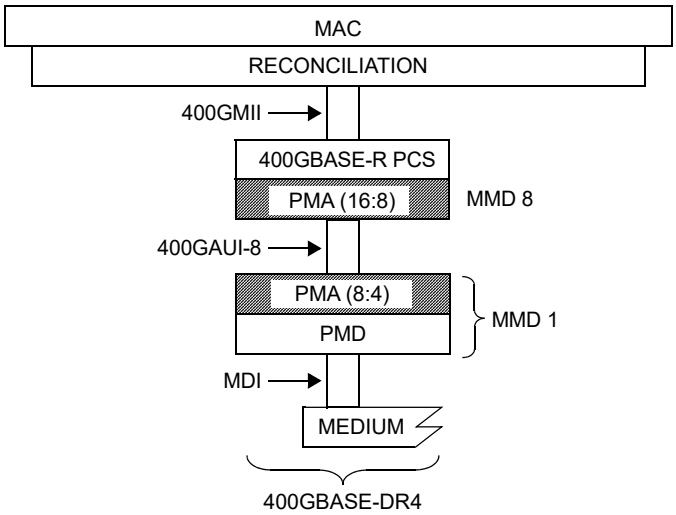
Figure 120A–6 depicts an example of 400GBASE-DR4 PMA layering with a single 400GAUI-8 chip-to-module interface.



400GAUI = 400 Gb/s ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120A–6—Example 400GBASE-DR4 PMA layering with single 400GAUI-8 chip-to-module interface

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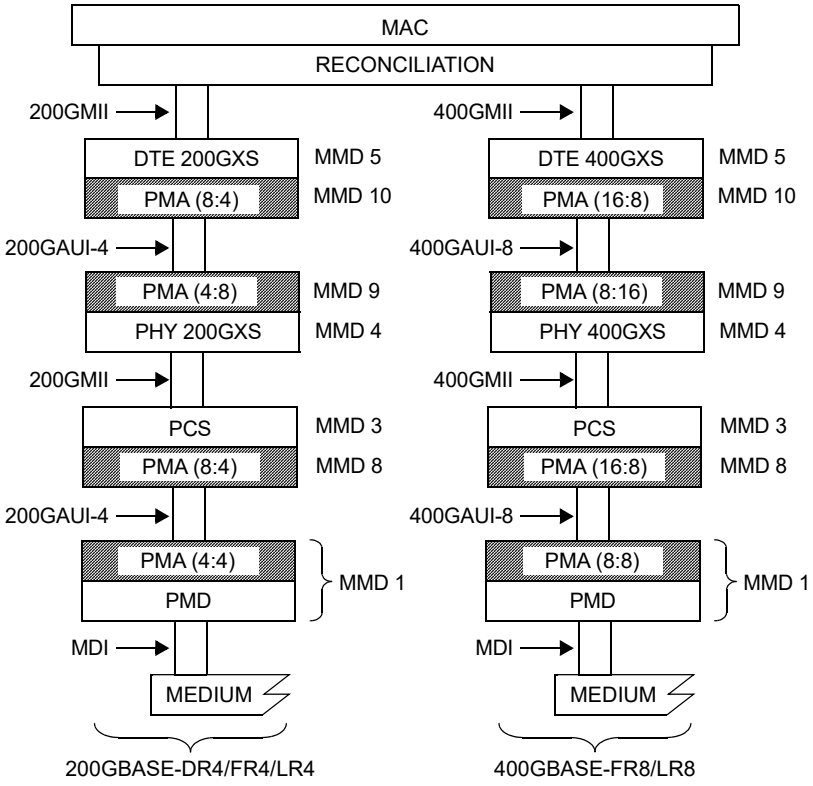
120A.4 Partitioning example using 200GXS and 400GXS

Figure 120A–7 depicts an example of 200GBASE-DR4/FR4/LR4 and 400GBASE-FR8/LR8 PMA layering with 200GXS, 400GXS, and two 200GAUI-4, 400GAUI-8 interfaces.



200GAUI = 200 Gb/s ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
200GXS = 200 Gb/s EXTENDER SUBLAYER
400GAUI = 400 Gb/s ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
400GXS = 400 Gb/s EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120A–7—Example 200GBASE-DR4/FR4/LR4 and 400GBASE-FR8/LR8 PMA layering with 200GXS, 400GXS, and two 200GAUI-4, 400GAUI-8 interfaces

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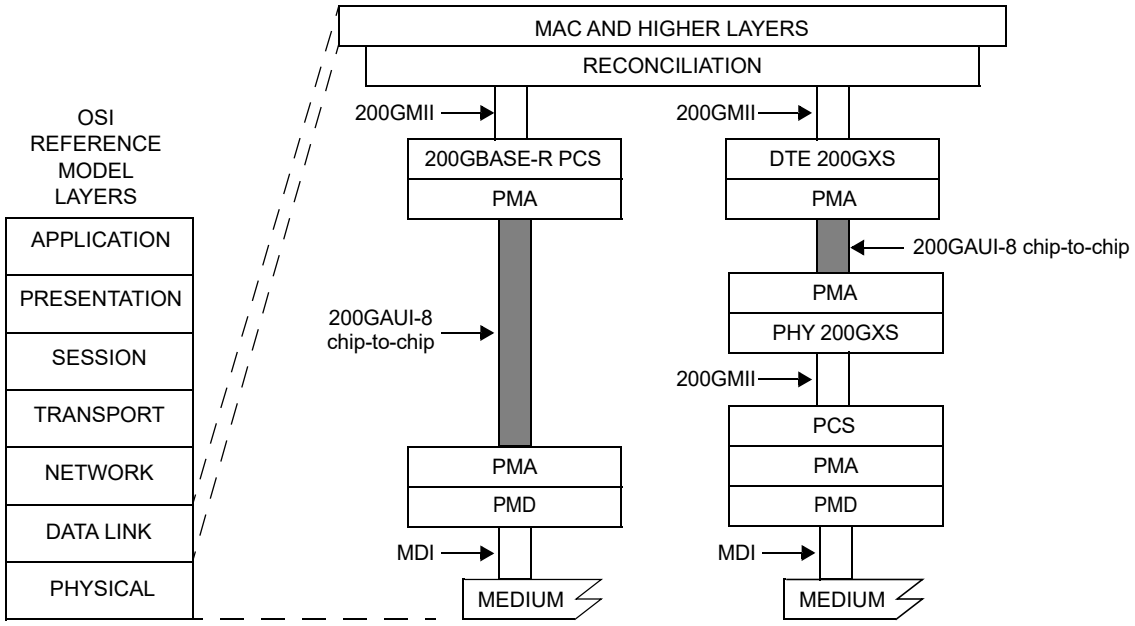
Annex 120B

(normative)

Chip-to-chip 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2C) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2C)

120B.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2C) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2C). Figure 120B–1 and Figure 120B–2 show example relationships of the 200GAUI-8 and 400GAUI-16 C2C interfaces to the ISO/IEC Open System Interconnection (OSI) reference model, respectively. The 200GAUI-8 and 400GAUI-16 C2C interfaces provide electrical characteristics and associated compliance points, which can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.



200GAUI-8 = 200 Gb/s EIGHT-LANE ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
200GXS = 200GMII EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120B–1—Example 200GAUI-8 chip-to-chip relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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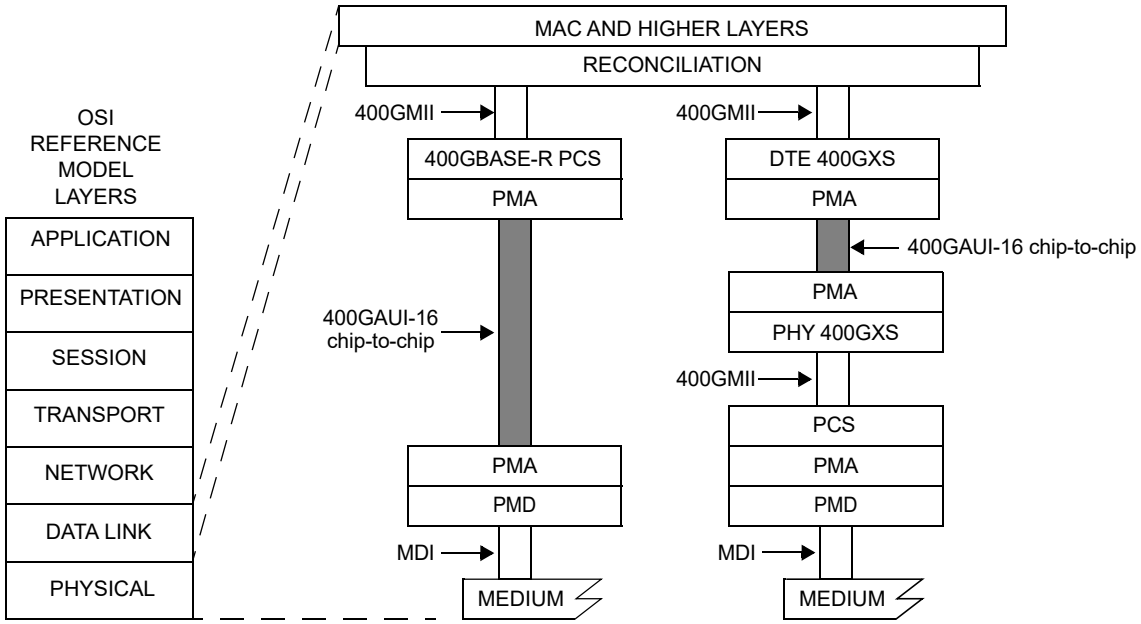

400GAUI-16 = 400 Gb/s SIXTEEN-LANE ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
400GXS = 400GMII EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120B–2—Example 400GAUI-16 chip-to-chip relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The 200GAUI-8 C2C link is described in terms of a 200GAUI-8 C2C transmitter, a 200GAUI-8 C2C channel, and a 200GAUI-8 C2C receiver. Figure 120B–3 depicts a typical 200GAUI-8 C2C application, and Equation (83D–1) (illustrated in Figure 83D–3) summarizes the recommended differential insertion loss budget associated with the chip-to-chip application. The 200GAUI-8 C2C interface comprises independent data paths in each direction. Each data path contains eight AC-coupled differential lanes using 2-level NRZ (also known as PAM2) signaling, where the highest differential voltage level corresponds to the symbol one and the lowest level corresponds to the symbol zero. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

The 400GAUI-16 C2C link is described in terms of a 400GAUI-16 C2C transmitter, a 400GAUI-16 C2C channel, and a 400GAUI-16 C2C receiver. Figure 120B–4 depicts a typical 400GAUI-16 C2C application, and Equation (83D–1) (illustrated in Figure 83D–3) summarizes the recommended differential insertion loss budget associated with the chip-to-chip application. The 400GAUI-16 C2C interface comprises independent data paths in each direction. Each data path contains sixteen AC-coupled differential lanes using 2-level NRZ (also known as PAM2) signaling, where the highest differential voltage level corresponds to the symbol one and the lowest level corresponds to the symbol zero. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

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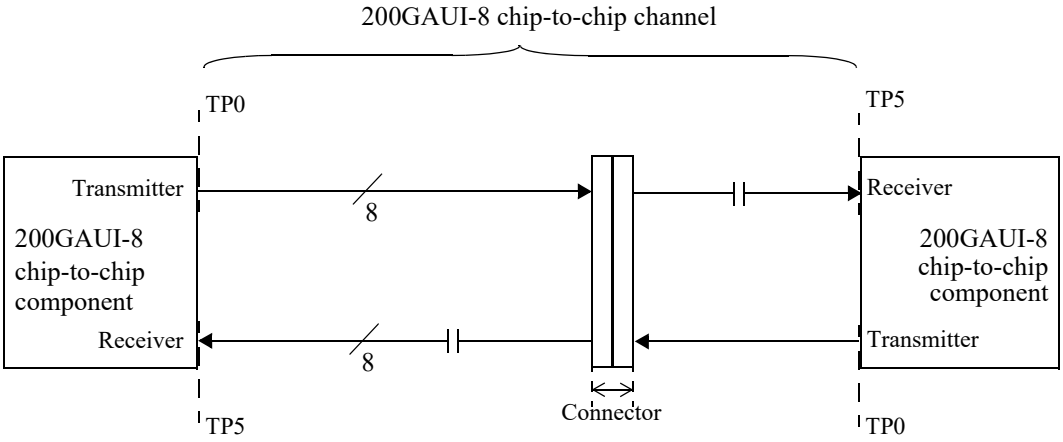

Figure 120B–3—Typical 200GAUI-8 chip-to-chip application

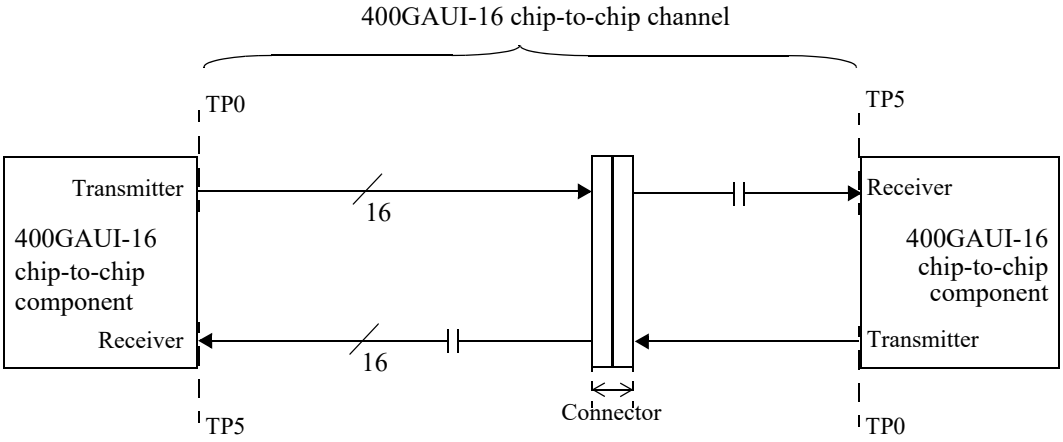

Figure 120B–4—Typical 400GAUI-16 chip-to-chip application

The nominal signaling rate for each lane is 26.5625 GBd. The 200GAUI-8 C2C or 400GAUI-16 C2C transmitter on each end of the link is adjusted to an appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 83D.3.3.2 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.

The normative channel compliance is through 200GAUI-8 C2C or 400GAUI-16 C2C channel operating margin (COM) as described in 120B.4. Actual channel loss could be higher or lower than that given by Equation (83D–1) due to the channel ILD, return loss, and crosstalk.

120B.2 200GAUI-8 and 400GAUI-16 chip-to-chip compliance point definition

The compliance points for the 200GAUI-8 and 400GAUI-16 chip-to-chip interfaces are as defined in 83D.2.

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120B.3 200GAUI-8 and 400GAUI-16 chip-to-chip electrical characteristics

120B.3.1 200GAUI-8 and 400GAUI-16 C2C transmitter characteristics

A 200GAUI-8 or a 400GAUI-16 chip-to-chip transmitter shall meet all specifications in 83D.3.1 with the following exceptions:

- The signaling rate per lane is 26.5625 GBd ± 100 ppm.
- The value for the "Linear fit pulse peak (min)" in Table 83D–1 is $0.75 \times v_f$.
- The value for the "Effective total uncorrelated jitter, peak-to-peak" in Table 83D–1 is 0.19 UI.
- The value of the probability in Table 83D–1 footnote d is 10^{-6}.
- The high-pass filter used for the jitter measurements in 92.8.3.8 has a 3 dB frequency of 4 MHz.

If a Clause 45 MDIO is implemented, *Local_eq_cm1* and *Local_eq_c1* for each lane (0 through 7 for 200GAUI-8 and 0 through 15 for 400GAUI-16) and direction (transmit and receive) are accessible through registers 1.500 through 1.531 (see 45.2.1.135 through 45.2.1.138).

120B.3.2 200GAUI-8 and 400GAUI-16 C2C receiver characteristics

A 200GAUI-8 or a 400GAUI-16 chip-to-chip receiver shall meet all specifications in 83D.3.3 with the following exceptions:

- The signaling rate per lane is 26.5625 GBd ± 100 ppm.
- The "Bit error ratio" parameter in Table 83D–5 is replaced with "PCS FEC symbol error ratio" with max values of 1.1×10^{-5}.
- The target values for the parameter "COM including effects of broadband noise" in Table 83D–5 are 3 dB.
- The transmitter device package model $S^{(tp)}$ is omitted from Equation (93A–3) in the calculation of COM. The filtered voltage transfer function $H^{(k)}(f)$ calculated in Equation (93A–19) uses the filter $H_t(f)$ defined by Equation (93A–46), where T_r is calculated as $T_r = 1.09 \times T_{\mathrm{rm}} - 4.32$ ps and T_{rm} is the measured 20% to 80% transition time of the signal at TP0a. T_{rm} is measured using the method in 86A.5.3.3, with the exception that the observation filter bandwidth is 33 GHz instead of 12 GHz. T_{rm} is measured with the transmit equalizer turned off (i.e., *Local_eq_cm1* and *Local_eq_c*1 both equal to zero, see 83D.3.1.1).
- Table 83D–5 footnote a is replaced by Table 93–6 footnote a.
- Table 83D–5 footnote b does not apply.
- The "Applied pk-pk sinusoidal jitter" for Test 1 and Test 2 in Table 83D–5 is according to Table 87–13.

If the 200GAUI-8 or 400GAUI-16 chip-to-chip receiver supports the optional transmitter equalization feedback, it shall meet all requirements in 83D.3.3.2. If a Clause 45 MDIO is implemented, the variables *Request_flag*, *Requested_eq_cm1*, *Requested_eq_c1*, *Remote_eq_cm1*, and *Remote_eq_c1* for each lane (0 through 7 for 200GAUI-8 and 0 through 15 for 400GAUI-16) and direction are accessible through registers 1.500 through 1.531 (see 45.2.1.135 through 45.2.1.138).

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120B.4 200GAUI-8 and 400GAUI-16 chip-to-chip channel characteristics

The 200GAUI-8 or 400GAUI-16 chip-to-chip channel shall meet the requirements specified in 83D.4 with the following exceptions:

— The signaling rate per lane is 26.5625 GBd ± 100 ppm.

— The "Target detector error ratio" (DER_0) value in Table 83D–6 is 10^{-6}.

— The "Normalized DFE coefficient magnitude limit, for n = 1 to N_b" ($b_{max}(n)$) value in Table 83D–6 is 1.

— The Channel Operating Margin (COM) shall be greater than or equal to 3 dB.

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120B.5 Protocol implementation conformance statement (PICS) proforma for Annex 120B, Chip-to-chip 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2C) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2C)[306]

120B.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 120B, Chip-to-chip 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2C) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2C), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

120B.5.2 Identification

120B.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

120B.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 120B, Chip-to-chip 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2C) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2C)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[306]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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120B.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	120B.1	Eight independent data paths in each direction for 200GAUI-8 and sixteen independent data paths in each direction for 400GAUI-16	M	Yes [ ]
*CHAN	Channel	120B.4	Items marked with CHAN include channel specifications not applicable to a PMA manufacturer	O	Yes [ ] No [ ]

120B.5.4 PICS proforma tables for Chip-to-chip 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2C) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2C)

120B.5.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	120B.3.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TC2	Peak-to-peak differential output voltage	120B.3.1	1200 mV (max)	M	Yes [ ]
TC3	Peak-to-peak differential output voltage, transmitter disabled	120B.3.1	Less than or equal to 30 mV	M	Yes [ ]
TC4	DC common-mode voltage	120B.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC5	AC common-mode output voltage	120B.3.1	12 mV RMS with respect to signal ground	M	Yes [ ]
TC6	Differential output return loss	120B.3.1	Meets Equation (93–3) constraints	M	Yes [ ]
TC7	Common-mode output return loss	120B.3.1	Meets Equation (93–4) constraints	M	Yes [ ]
TC8	Output waveform	120B.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC9	Output jitter	120B.3.1	Meets Table 83D–1 constraints with the exceptions in 120B.3.1	M	Yes [ ]
TC10	Transmit equalization	120B.3.1	Each successive step results in a monotonic change	M	Yes [ ]

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120B.5.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	120B.3.2	Meets Equation (93–3) constraints	M	Yes [ ]
RC2	Differential to common-mode input return loss	120B.3.2	Meets Equation (93–5) constraints	M	Yes [ ]
RC3	Interference tolerance	120B.3.2	Satisfy requirements in Table 83D–5with the exceptions in 120B.3.2	M	Yes [ ]

120B.5.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	120B.4	Greater than or equal to 3 dB	CHAN:M	Yes [ ]

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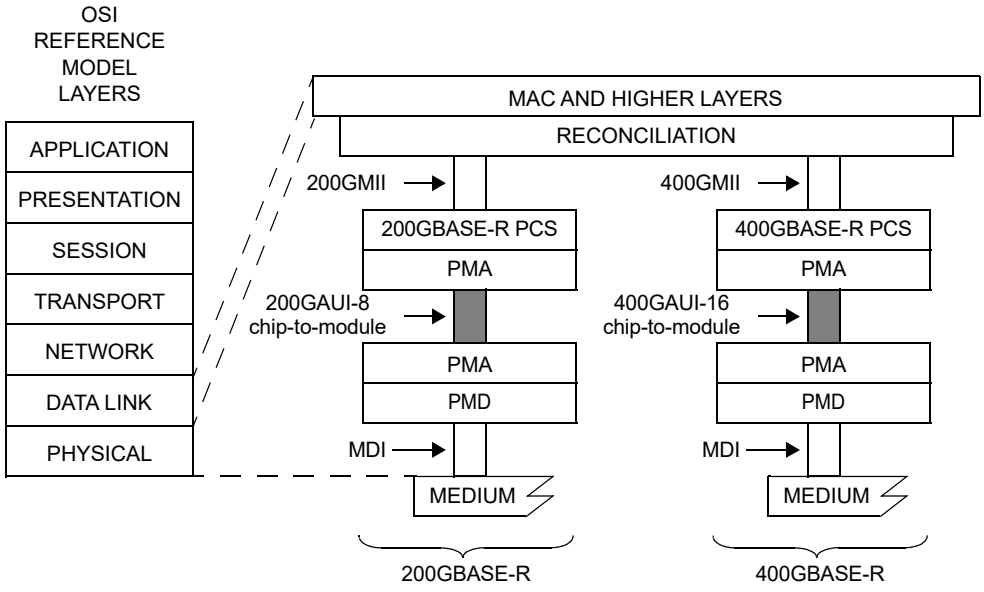
Annex 120C

(normative)

Chip-to-module 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2M) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2M)

120C.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2M) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2M). Figure 120C–1 shows the relationship of the 200GAUI-8 and 400GAUI-16 C2M interfaces to the ISO/IEC Open System Interconnection (OSI) reference model. The chip-to-module interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable module interfaces.



200GAUI-8 = 200 Gb/s EIGHT-LANE ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GAUI-16 = 400 Gb/s SIXTEEN-LANE ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120C–1—Example 200GAUI-8 and 400GAUI-16 chip-to-module relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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The sublayers (including the PCS and associated FEC) of each PHY that can optionally include a 200GAUI-8 C2M or 400GAUI-16 C2M are summarized in the tables in 116.1.4 and are specified in the corresponding PMD clause. The positioning of the 200GAUI-8 C2M or 400GAUI-16 C2M relative to other sublayers is shown in 120.1 with further examples in Annex 120A.

The 200GAUI-8 C2M link is described in terms of a host 200GAUI-8 C2M component, a 200GAUI-8 C2M channel with associated insertion loss, and a module 200GAUI-8 C2M component. Figure 120C–2 depicts a typical 200GAUI-8 C2M application and summarizes the differential insertion loss budget associated with the chip-to-module application. The supported insertion loss budget is characterized by Equation (83E–1) and illustrated in Figure 83E–3. The 200GAUI-8 C2M interface comprises independent data paths in each direction. Each data path contains eight differential lanes using 2-level NRZ (also known as PAM2) signaling, where the highest differential voltage level corresponds to the symbol one and the lowest level corresponds to the symbol zero. Each lane is AC-coupled within the module.

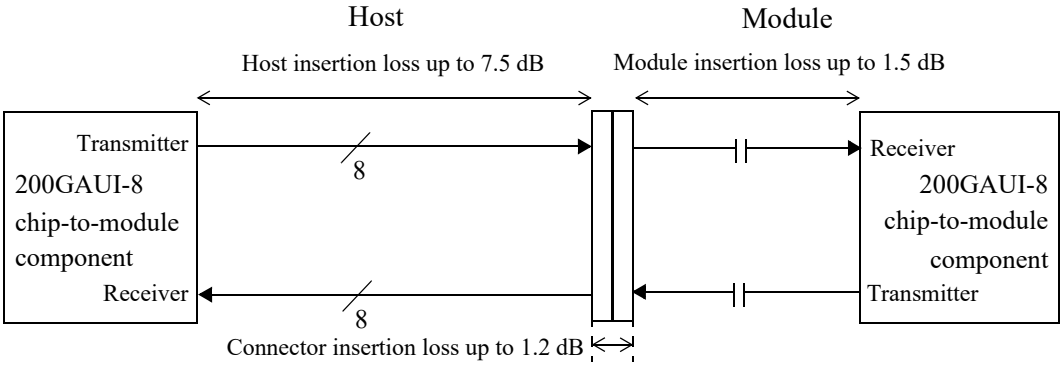

Figure 120C–2—200GAUI-8 chip-to-module insertion loss budget at 13.28 GHz

The 400GAUI-16 C2M link is described in terms of a host 400GAUI-16 C2M component, a 400GAUI-16 C2M channel with associated insertion loss, and a module 400GAUI-16 C2M component. Figure 120C–3 depicts a typical 400GAUI-16 C2M application and summarizes the differential insertion loss budget associated with the chip-to-module application. The supported insertion loss budget is characterized by Equation (83E–1) and illustrated in Figure 83E–3. The 400GAUI-16 C2M interface comprises independent data paths in each direction. Each data path contains sixteen differential lanes using 2-level NRZ (also known as PAM2) signaling, where the highest differential voltage level corresponds to the symbol one and the lowest level corresponds to the symbol zero. Each lane is AC-coupled within the module.

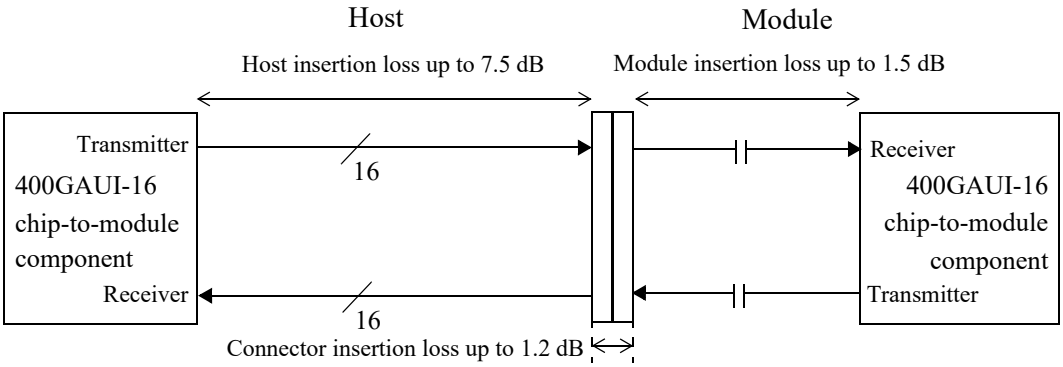

Figure 120C–3—400GAUI-16 chip-to-module insertion loss budget at 13.28 GHz

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The nominal signaling rate for each lane is 26.5625 GBd. The 200GAUI-8 and 400GAUI-16 chip-to-module interfaces are defined using a specification and test methodology that is similar to that used for CEI-28G-VSR defined in OIF-CEI-03.1 [B57].

120C.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 10^{-6}.

120C.2 200GAUI-8 and 400GAUI-16 chip-to-module compliance point definitions

The compliance points for the 200GAUI-8 and 400GAUI-16 chip-to-module interfaces are as defined in 83E.2.

120C.3 200GAUI-8 and 400GAUI-16 chip-to-module electrical characteristics

120C.3.1 200GAUI-8 and 400GAUI-16 C2M host output characteristics

A 200GAUI-8 or 400GAUI-16 C2M host output shall meet all specifications in 83E.3.1 with the following exceptions:

— The signaling rate per lane is 26.5625 GBd ± 100 ppm.
— The clock recovery unit corner frequency is 4 MHz.

If a Clause 45 MDIO is implemented, the variable *Recommended_CTLE_value* is accessible in the module for lanes 0 through 7 for 200GAUI-8 and 0 through 15 for 400GAUI-16 through registers 1.400 to 1.415 (see 45.2.1.111 and 45.2.1.133).

120C.3.2 200GAUI-8 and 400GAUI-16 C2M module output characteristics

A 200GAUI-8 or a 400GAUI-16 C2M module output shall meet all specifications in 83E.3.2 with the following exceptions:

— The signaling rate per lane is 26.5625 GBd ± 100 ppm.
— The eye height, eye width, and vertical eye closure are as specified in 109B.3.2.1 for a PHY that includes an RS-FEC sublayer.
— The clock recovery unit corner frequency is 4 MHz.

120C.3.3 200GAUI-8 and 400GAUI-16 C2M host input characteristics

A 200GAUI-8 or a 400GAUI-16 C2M host input shall meet all specifications in 83E.3.3 with the following exceptions:

— The signaling rate per lane is 26.5625 GBd ± 100 ppm.
— The BER for the host stressed input test meets the requirement in 120C.1.1 rather than those in 83E.1.1.
— The “Applied pk-pk sinusoidal jitter” in Table 83E–5 is according to Table 87–13.

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120C.3.4 200GAUI-8 and 400GAUI-16 C2M module input characteristics

A 200GAUI-8 or a 400GAUI-16 C2M module input shall meet all specifications in 83E.3.4 with the following exceptions:

— The signaling rate per lane is 26.5625 GBd ± 100 ppm.

— The BER for the module stressed input test meets the requirement in 120C.1.1 rather than those in 83E.1.1.

— The "Applied pk-pk sinusoidal jitter" in Table 83E–8 is according to Table 87–13.

Channel equalization is provided by an equalizer in the module which uses the *Recommended_CTLE_value* provided by the host or an adaptive equalizer in the module which does not use the setting provided by the host.

If a Clause 45 MDIO is implemented, the variable *Recommended_CTLE_value* is accessible in the module for lanes 0 through 7 for 200GAUI-8 and 0 through 15 for 400GAUI-16 through registers 1.400 to 1.415 (see 45.2.1.111 and 45.2.1.133).

120C.4 200GAUI-8 and 400GAUI-16 C2M measurement methodology

The 200GAUI-8 and 400GAUI-16 C2M measurement methodology is as defined in 83E.4 with the following exceptions:

— The module output eye height, eye width, and vertical eye closure are measured as specified in 109B.3.2.1 for a PHY that includes an RS-FEC sublayer.

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120C.5 Protocol implementation conformance statement (PICS) proforma for Annex 120C, Chip-to-module 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2M) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2M)[307]

120C.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 120C, Chip-to-module 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2M) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2M), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

120C.5.2 Identification

120C.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

120C.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 120C, Chip-to-module 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2M) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2M)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[307] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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120C.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	120C.1	Eight independent data paths in each direction for 200GAUI-8 and sixteen independent data paths in each direction for 400GAUI-16	M	Yes [ ]
BER	Meets BER requirement	120C.1.1	See 120C.1.1	M	Yes [ ]
ADE	Adaptive equalizer	120C.3.4	Module receiver does not use *Recommended_CTLE_value*	O	Yes [ ] No [ ]

120C.5.4 PICS proforma tables for Chip-to-module 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2M) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2M)

120C.5.4.1 Host output

Item	Feature	Subclause	Value/Comment	Status	Support
TH1	Signaling rate	120C.3.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TH2	Peak-to-peak differential output voltage	120C.3.1	900 mV (max)	M	Yes [ ]
TH3	Peak-to-peak differential output voltage, transmitter disabled	120C.3.1	Less than or equal to 35 mV	M	Yes [ ]
TH4	DC common-mode output voltage	120C.3.1	Between –0.3 V and 2.8 V with respect to signal ground	M	Yes [ ]
TH5	AC common-mode output voltage	120C.3.1	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TH6	Differential output return loss	120C.3.1	Meets Equation (83E–2) constraints	M	Yes [ ]
TH7	Reference impedance for output return loss	120C.3.1	100 Ω.	M	Yes [ ]
TH8	Common to differential mode conversion	120C.3.1	Meets Equation (83E–3) constraints	M	Yes [ ]
TH9	Differential termination mismatch	120C.3.1	Less than 10%	M	Yes [ ]
TH10	Transition time	120C.3.1	Greater than or equal to 10 ps	M	Yes [ ]
TH11	Eye width	120C.3.1	0.46 UI	M	Yes [ ]
TH12	Eye height A	120C.3.1	95 mV	M	Yes [ ]
TH13	Eye height B	120C.3.1	80 mV	M	Yes [ ]
TH14	Crosstalk source	120C.3.1	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 200GBASE-R/400GBASE-R signal	M	Yes [ ]

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120C.5.4.2 Module output

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Signal rate	120C.3.2	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TM2	Peak-to-peak differential output voltage	120C.3.2	900 mV (max)	M	Yes [ ]
TM3	AC common-mode output voltage	120C.3.2	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TM4	Differential output return loss	120C.3.2	Meets Equation (83E–2) constraints	M	Yes [ ]
TM5	Reference impedance for output return loss	120C.3.2	100 Ω.	M	Yes [ ]
TM6	Common to differential mode conversion	120C.3.2	Meets Equation (83E–3) constraints	M	Yes [ ]
TM7	Differential termination mismatch	120C.3.2	Less than 10%	M	Yes [ ]
TM8	Transition time	120C.3.2	Greater than or equal to 12 ps	M	Yes [ ]
TM9	Eye width	120C.3.2	0.57 UI	M	Yes [ ]
TM10	Eye height	120C.3.2	228 mV	M	Yes [ ]
TM11	Crosstalk source	120C.3.2	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 200GBASE-R/400GBASE-R signal	M	Yes [ ]
TM12	Vertical eye closure	120C.3.2	5.5 dB (max)	M	Yes [ ]

120C.5.4.3 Host input

Item	Feature	Subclause	Value/Comment	Status	Support
RH1	Host input characteristics	120C.3.3	Table 83E–4 with the exceptions in 120C.3.3	M	Yes [ ]

120C.5.4.4 Module input

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Module input characteristics	120C.3.4	Table 83E–7 with the exceptions in 120C.3.4	M	Yes [ ]
RM2	Module stressed input test BER requirement	120C.3.4	Meet BER requirement of 120C.1.1 with three values of *Recommended_CTLE_value*	M	Yes [ ]

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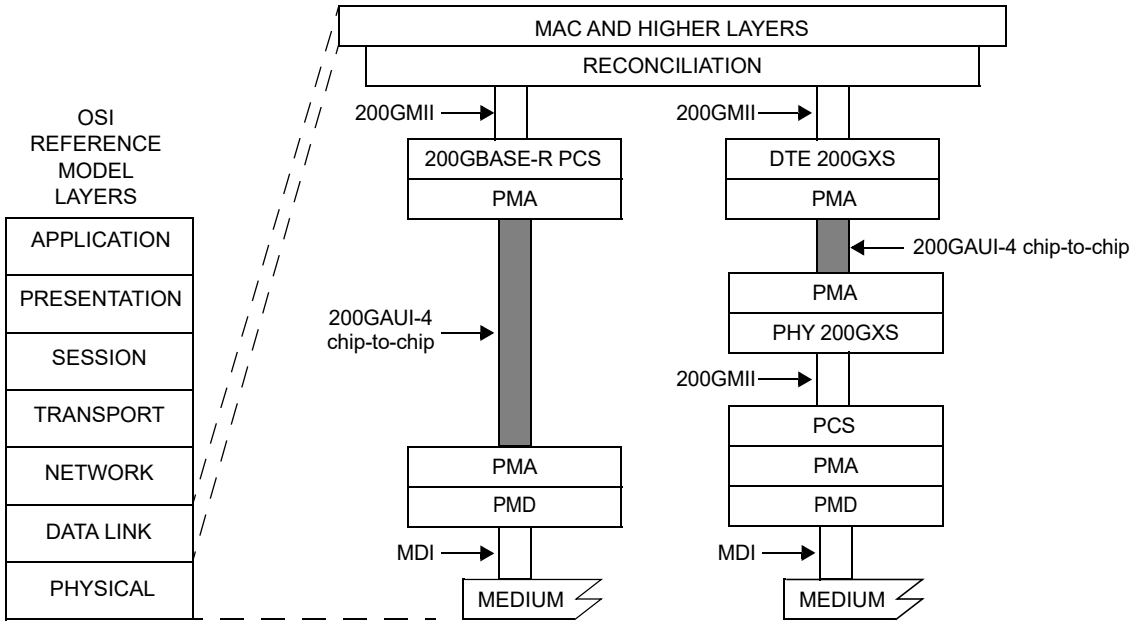
Annex 120D

(normative)

Chip-to-chip 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2C) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2C)

120D.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2C) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2C). Figure 120D–1 and Figure 120D–2 show example relationships of the 200GAUI-4 and 400GAUI-8 C2C interfaces to the ISO/IEC Open System Interconnection (OSI) reference model, respectively. The 200GAUI-4 and 400GAUI-8 C2C interfaces provide electrical characteristics and associated compliance points, which can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.



200GAUI-4 = 200 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
200GXS = 200GMII EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120D–1—Example 200GAUI-4 chip-to-chip relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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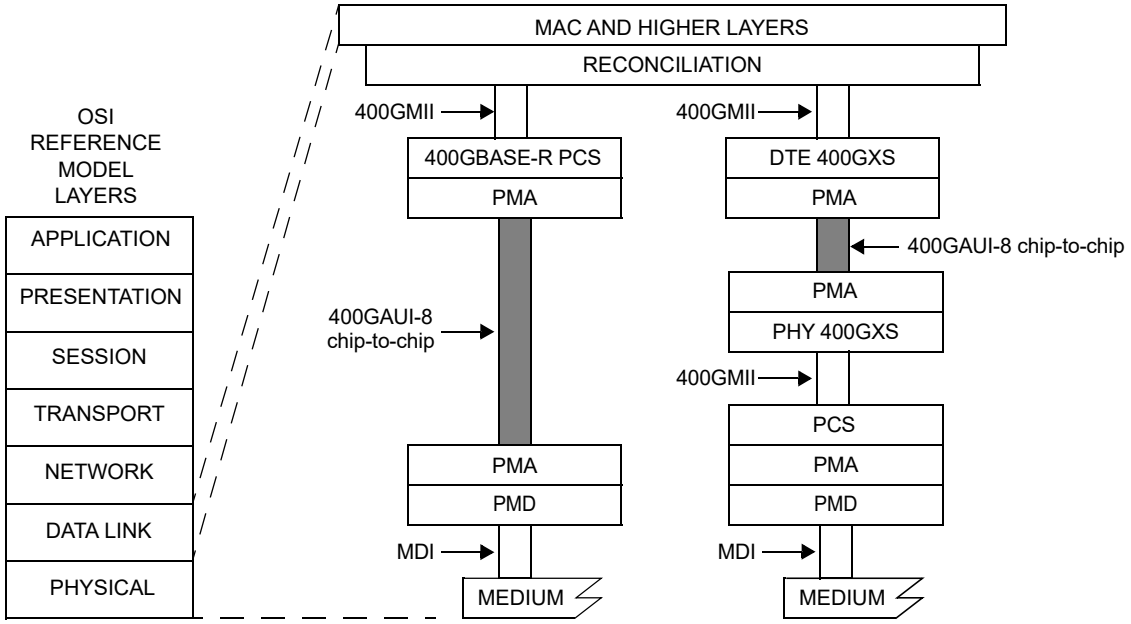

400GAUI-8 = 400 Gb/s EIGHT-LANE ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
400GXS = 400GMII EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120D–2—Example 400GAUI-8 chip-to-chip relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The 200GAUI-4 C2C link is described in terms of a 200GAUI-4 C2C transmitter, a 200GAUI-4 C2C channel, and a 200GAUI-4 C2C receiver. Figure 120D–3 depicts a typical 200GAUI-4 C2C application, and Equation (120D–1) (illustrated in Figure 120D–5) summarizes the recommended differential insertion loss budget associated with the chip-to-chip application. The 200GAUI-4 C2C interface comprises independent data paths in each direction. Each data path contains four AC-coupled differential lanes using PAM4 signaling, where the highest differential level corresponds to the symbol three and the lowest level corresponds to the symbol zero. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

The 400GAUI-8 C2C link is described in terms of a 400GAUI-8 C2C transmitter, a 400GAUI-8 C2C channel, and a 400GAUI-8 C2C receiver. Figure 120D–4 depicts a typical 400GAUI-8 C2C application, and Equation (120D–1) (illustrated in Figure 120D–5) summarizes the recommended differential insertion loss budget associated with the chip-to-chip application. The 400GAUI-8 C2C interface comprises independent data paths in each direction. Each data path contains eight AC-coupled differential lanes using PAM4 signaling, where the highest differential level corresponds to the symbol three and the lowest level corresponds to the symbol zero. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

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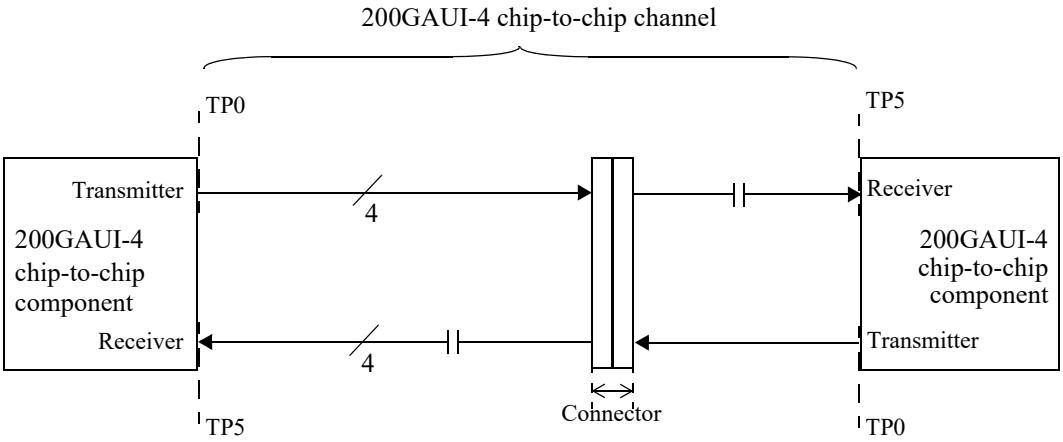

Figure 120D–3—Typical 200GAUI-4 chip-to-chip application

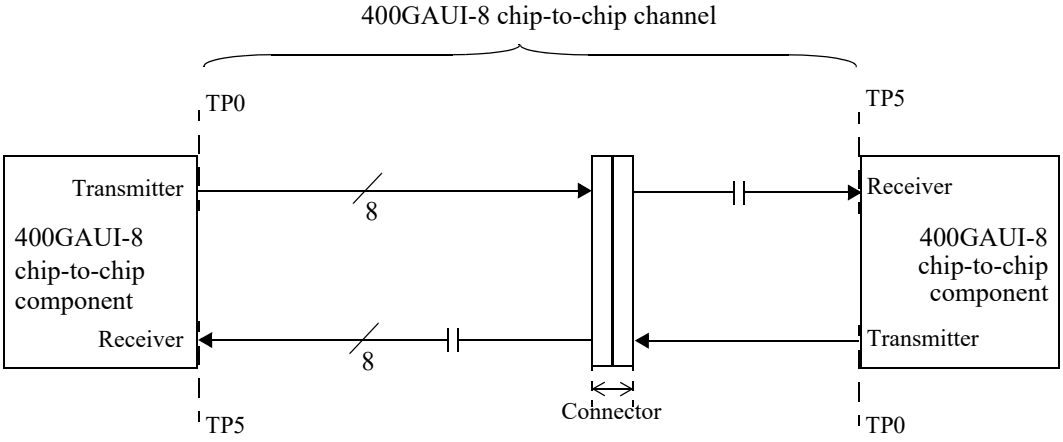

Figure 120D–4—Typical 400GAUI-8 chip-to-chip application

The nominal signaling rate for each lane is 26.5625 GBd. The 200GAUI-4 C2C or 400GAUI-8 C2C transmitter on each end of the link is adjusted to an appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 120D.3.2.3 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.

The channel is normatively defined using channel operating margin (COM) as described in 120D.4. Actual channel loss could be higher or lower than that given by Equation (120D–1) due to the channel ILD, return loss, and crosstalk. Note that for this equation the channel loss at the Nyquist frequency is lower than or equal to 20.457 dB.

$$Insertion\_loss(f) \le 1.083 + 2.543\sqrt{f} + 0.761f \quad \text{(dB)}$$
$$\text{for } 0.01 \le f \le 26.5625 \qquad \text{(120D–1)}$$

where

f is the frequency in GHz

Insertion_loss(f) is the recommended 200GAUI-4 or 400GAUI-8 chip-to-chip insertion loss

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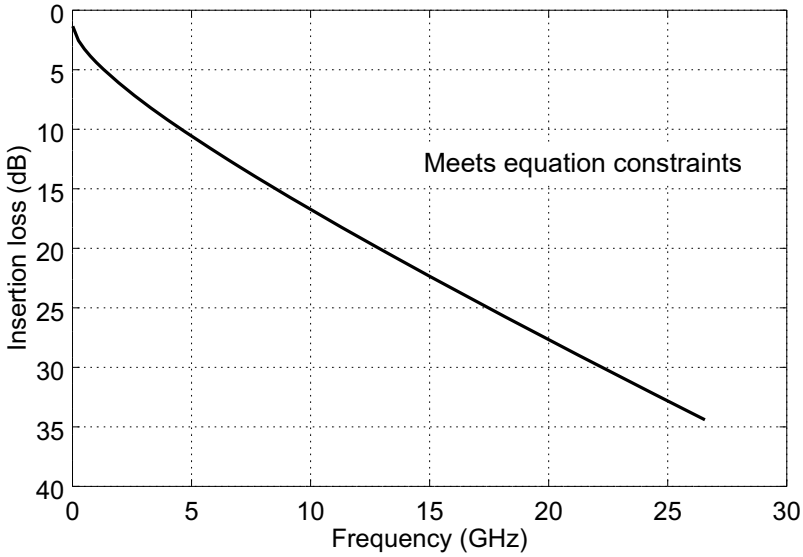

Figure 120D–5—200GAUI-4 or 400GAUI-8 chip-to-chip channel insertion loss

120D.2 200GAUI-4 and 400GAUI-8 chip-to-chip compliance point definition

The electrical characteristics for the 200GAUI-4 and 400GAUI-8 chip-to-chip interfaces are defined at compliance points for the transmitter (TP0a) and receiver (TP5a). The location of TP0a and electrical characteristics of the test fixture used to measure transmitter characteristics are defined in Figure 93–5 and 93.8.1.1, respectively, with the exception that the upper frequency for Equation (93–1) and Equation (93–2) is 26.5625 GHz. The location of TP5a and electrical characteristics of the test fixture used to measure the receiver are defined in Figure 93–10 and 93.8.2.1, respectively, with the exception that the upper frequency for Equation (93–1) and Equation (93–2) is 26.5625 GHz.

120D.3 200GAUI-4 and 400GAUI-8 chip-to-chip electrical characteristics

120D.3.1 200GAUI-4 and 400GAUI-8 C2C transmitter characteristics

A 200GAUI-4 or a 400GAUI-8 chip-to-chip transmitter shall meet the specifications given in Table 120D–1. The transmit output waveform may optionally be manipulated via the feedback mechanism described in 120D.3.2.3.

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified.

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Table 120D–1—200GAUI-4 and 400GAUI-8 C2C transmitter characteristics at TP0a

Parameter	Reference	Value	Units
Signaling rate per lane (range)		26.5625 ± 100 ppm	GBd
Differential peak-to-peak output voltage[a] (max) Transmitter disabled Transmitter enabled	93.8.1.3	 30 1200	 mV mV
Common-mode voltage[a] (max)	93.8.1.3	1.9	V
Common-mode voltage[a] (min)	93.8.1.3	0	V
AC common-mode output voltage[a] (max, RMS)	93.8.1.3	30	mV
Differential output return loss (min)	120D.3.1.1	Equation (120D–2)	dB
Common-mode output return loss (min)	93.8.1.4	Equation (93–4)	dB
Output waveform[b] Level separation mismatch ratio R_{LM}(min) Steady state voltage v_f(max) Steady state voltage v_f(min) Linear fit pulse peak (min) Pre-cursor equalization Post-cursor equalization	 120D.3.1.2 120D.3.1.4 120D.3.1.4 120D.3.1.4 120D.3.1.5 120D.3.1.5	 0.95 0.6 0.4 $0.76 \times v_f$ Table 120D–2 Table 120D–3	 — V V V — —
Signal-to-noise-and-distortion ratio SNDR (min)	120D.3.1.6	31.5	dB
Transmitter Output residual ISI SNR_{ISI} (min)	120D.3.1.7	34.8	dB
Output jitter J_{RMS} (max) J4u (max) Even-odd jitter (max)	 120D.3.1.8 120D.3.1.8 120D.3.1.8	 0.023 0.118 0.019	 UI UI UI

[a]Measurement uses the method described in 93.8.1.3 with the exception that the PRBS13Q test pattern is used.
[b]The state of the transmit equalizer is controlled by management interface.

120D.3.1.1 Transmitter differential output return loss

The differential output return loss, in dB, of the transmitter shall meet Equation (120D–2) where f is the frequency in GHz. This requirement applies to all valid output levels. The reference impedance for differential return loss is $100\,\Omega$. The test fixture return loss may be de-embedded from return loss measurements. For the treatment of the insertion loss of the test fixture see 93.8.1.1.

$$RL_d(f) \geq \begin{cases} 14.25 - f & 0.05 \leq f \leq 6 \\ 8.7 - 0.075f & 6 < f \leq 19 \end{cases} \quad \text{dB} \qquad \text{(120D–2)}$$

The differential return loss limit is illustrated by Figure 120D–6.

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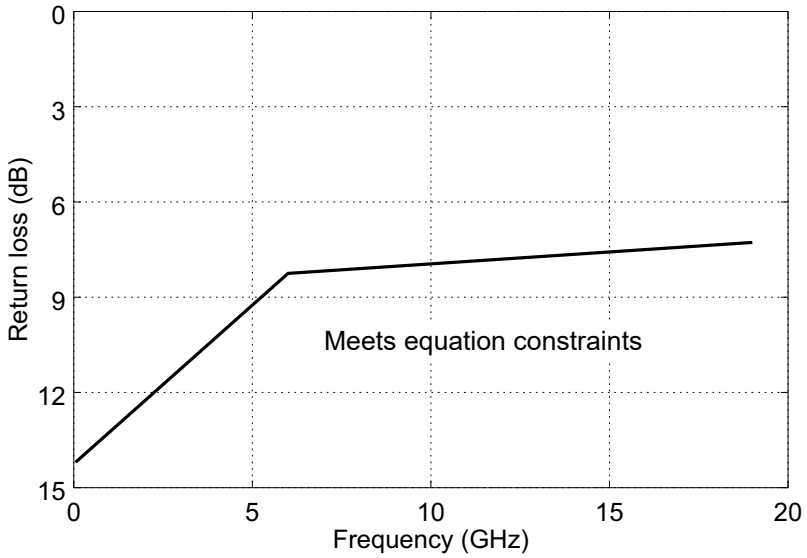

Figure 120D–6—Differential return loss limit

120D.3.1.2 Transmitter linearity

Transmitter linearity is defined as a function of the mean signal level transmitted for each PAM4 symbol level. The mean signal levels of the symbols corresponding to the PAM4 symbol levels 0, 1, 2, and 3 are defined as V_0, V_1, V_2, and V_3 respectively, as defined in 120D.3.1.2.1. The mid-range level V_{mid} is defined by Equation (120D–3). The mean signal levels are then normalized and offset adjusted so that V_{mid} corresponds to 0, V_0 to −1, V_1 to $-ES1$, V_2 to $ES2$, and V_3 to 1. $ES1$ is defined by Equation (120D–4) and $ES2$ is defined by Equation (120D–5).

$$V_{\text{mid}} = \frac{V_0 + V_3}{2} \tag{120D–3}$$

$$ES1 = \frac{V_1 - V_{\text{mid}}}{V_0 - V_{\text{mid}}} \tag{120D–4}$$

$$ES2 = \frac{V_2 - V_{\text{mid}}}{V_3 - V_{\text{mid}}} \tag{120D–5}$$

The level separation mismatch ratio R_{LM} is defined by Equation (120D–6).

$$R_{\text{LM}} = \min((3 \times ES1), (3 \times ES2), (2 - 3 \times ES1), (2 - 3 \times ES2)) \tag{120D–6}$$

120D.3.1.2.1 Measurement of mean signal levels

The signal levels are measured from a waveform captured using the procedure defined in 85.8.3.3.4 while the transmitter is transmitting the PRBS13Q test pattern. The waveform consists of M samples per unit interval and is aligned such that the first M samples of the waveform correspond to the first PAM4 symbol of the test pattern, the second M samples to the second PAM4 symbol, and so on. This allows each sample of the waveform to be associated with a specific PAM4 symbol in the test pattern.

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Denote the number of PAM4 symbols in the test pattern as N. Reduce the captured waveform to N samples by choosing the central sample from each unit interval. The central sample is defined as m^{th} sample in a given unit interval where m is the integer closest to $M/2$.

For each PAM4 symbol level x, V_x is the mean value of the waveform samples that correspond to that symbol level.

120D.3.1.3 Linear fit to the measured waveform

The following test procedure shall be followed to determine the linear fit pulse response, linear fit error, and normalized transmitter coefficient values.

For each configuration of the transmit equalizer, capture at least one complete cycle of the PRBS13Q test pattern (120.5.11.2.1) at TP0a per 85.8.3.3.4.

Compute the linear fit pulse response $p(k)$ and linear fit error $e(k)$ from the captured waveform per 85.8.3.3.5 using $N_p = 200$ and $D_p = 2$. The aligned symbols *x(n)* are assigned normalized amplitudes −1, $-ES$, ES, and 1 to represent the PAM4 symbol values 0, 1, 2, and 3 respectively. ES is defined to be $(|ES1| + |ES2|)/2$ where *ES1* and *ES2* are defined in 120D.3.1.2.

Define $r(k)$ to be the linear fit pulse response with *Local_eq_cm1* and *Local_eq_c1* set to zero.

For each configuration of the transmit equalizer, compute the normalized transmit equalizer coefficients, *c(i)*, according to 92.8.3.5.1.

The clock recovery unit (CRU) used in the output waveform measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade

120D.3.1.4 Steady-state voltage and linear fit pulse peak

The linear fit pulse, $p(k)$, is determined according to the linear fit procedure in 120D.3.1.3 with *Local_eq_cm1* and *Local_eq_c1* set to zero. The steady-state voltage v_f is defined to be the sum of the linear fit pulse $p(1)$ through $p(M \times N_v)$ divided by M, determined in step 3 of the linear fit procedure. Here, N_v represents the number of symbols to take into account for the steady-state voltage v_f and has a value of 13.

120D.3.1.5 Transmitter equalization settings

The 200GAUI-4 and 400GAUI-8 chip-to-chip transmitters include programmable equalization to compensate for the frequency-dependent loss of the channel and to facilitate data recovery at the receiver. The functional model for the transmit equalizer is the three tap transversal filter shown in Figure 120D–7. The transmitter output equalization is characterized using the linear fit method described in 120D.3.1.3.

The state of the 200GAUI-4 or 400GAUI-8 C2C transmit output is manipulated via management.

The variable *Local_eq_cm1* controls the weight of the pre-cursor tap $c(-1)$, by changing the ratio $c(-1)/(|c(-1)|+|c(0)|+|c(1)|)$. The valid values of *Local_eq_cm1* and the corresponding ratios are specified in Table 120D–2. The variable *Local_eq_c1* controls the weight of the post-cursor tap $c(1)$, by changing the ratio $c(1)/(|c(-1)|+|c(0)|+|c(1)|)$. The valid values of *Local_eq_c1* and the corresponding ratios are specified in Table 120D–3. *Local_eq_cm1* and *Local_eq_c1* are independent of each other and independent on each lane. Each successive step in *Local_eq_cm1* and *Local_eq_c1* value shall result in a monotonic change in transmitter equalization.

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If a Clause 45 MDIO is implemented, *Local_eq_cm1* and *Local_eq_c1* for each lane (0 through 3 for 200GAUI-4 C2C and 0 through 7 for 400GAUI-8 C2C) and direction (transmit and receive) are accessible through registers 1.500 through 1.507 for receive, and 1.516 through 1.523 for transmit (see 45.2.1.135 through 45.2.1.138).

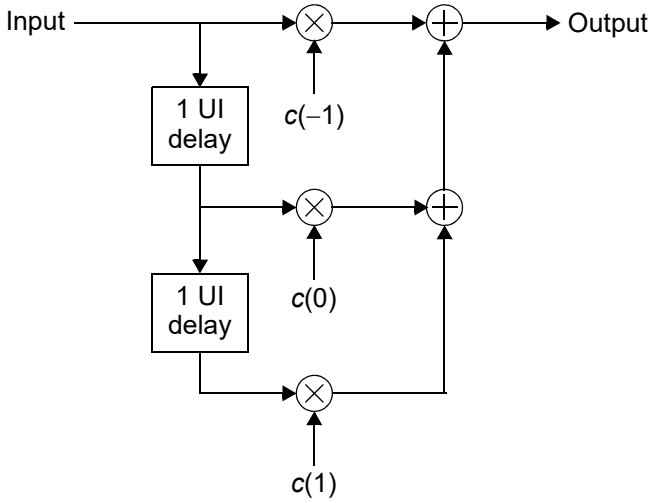

Figure 120D–7—Transmit equalizer functional model

Table 120D–2—Pre-cursor equalization

***Local_eq_cm1* value**	***c*(–1) ratio** $\left(\frac{c(-1)}{\lvert c(-1)\rvert + \lvert c(0)\rvert + \lvert c(1)\rvert}\right)$
0	0 ±0.04
1	–0.05 ±0.04
2	–0.1 ±0.04
3	–0.15 ±0.04

Table 120D–3—Post-cursor equalization

***Local_eq_c1* value**	***c*(1) ratio** $\left(\frac{c(1)}{\lvert c(-1)\rvert + \lvert c(0)\rvert + \lvert c(1)\rvert}\right)$
0	0 ±0.04
1	–0.05 ±0.04
2	–0.1 ±0.04
3	–0.15 ±0.04
4	–0.2 ±0.04
5	–0.25 ±0.04

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120D.3.1.6 Transmitter output noise and distortion

Signal-to-noise and distortion ratio (SNDR) is measured at the transmitter output using the following method, with transmitters on all lanes enabled, with identical transmit equalizer settings, and the lanes not under test transmitting PRBS31Q or a valid 200GBASE-R or 400GBASE-R signal.

Compute the linear fit to the captured waveform and the linear fit pulse response, $p(k)$, and error, $e(k)$, according to 120D.3.1.3. Denote the standard deviation of $e(k)$ as σ_e.

Using the same configuration of the transmitter equalizer, measure the RMS deviation from the mean voltage at a fixed low-slope point in runs of at least 6 consecutive identical PAM4 symbols. PRBS13Q includes such a run for each of the PAM4 levels. The average of the four measurements is denoted as σ_n.

SNDR is defined by Equation (120D–7) where $p_{\max}$ is the maximum value of $p(k)$.

$$SNDR = 10\log_{10}\left(\frac{p_{\max}^2}{\sigma_e^2 + \sigma_n^2}\right) \quad \text{(120D–7)}$$

120D.3.1.7 Transmitter output residual ISI

SNR_{ISI} is defined by Equation (120D–9) computed from $p_{\max}$ and ISI_{cursors} after these have been re-calculated with the continuous time filter described in 93A.1.4.3 using the parameters in Table 120D–8 applied and optimized for maximum SNR_{ISI}. The SNR_{ISI} specification shall be met for all transmit equalization settings.

$$ISI_{\text{cursors}} = [p(t_p + M \times (N_b + 1)), p(t_p + M \times (N_b + 2)), \ldots, p(t_p + M \times (N_p - D_p - 1))] \quad \text{(120D–8)}$$

$$SNR_{\text{ISI}} = 20\log_{10}\left(\frac{p_{\max}}{\sqrt{\sum(ISI_{\text{cursors}}{}^2)}}\right) \quad \text{(120D–9)}$$

ISI_{cursors} are computed from the linear fit pulse response, $p(k)$ in accordance with 120D.3.1.3, using Equation (120D–8), where

t_p is the index of the linear fit pulse where $p(t_p)$ equals $p_{\max}$
M is the oversampling ratio of the measured waveform and linear fit pulse as defined in 85.8.3.3.4
N_p is the linear fit pulse length given in 120D.3.1.3
N_b is given in Table 120D–8

NOTE—The observed SNR_{ISI} can be significantly influenced by the measurement setup, e.g., reflections in cables and connectors. High-precision measurement and careful calibration of the setup are recommended.

120D.3.1.8 Output jitter

J4u, J_{RMS}, and Even-odd jitter are defined by measurements of 12 specific transitions in a PRBS13Q pattern (see 120.5.11.2.1) in order to exclude correlated jitter. The 12 transitions represent all possible combinations of four identical symbols followed by two different identical symbols as shown in Table 120D–4. The sequences are located by the symbol indices given in the table where symbols 1 to 7 are the run of seven 3s.

The threshold used to define each transition is given in Table 120D–4 where V_0, V_1, V_2, and V_3 are as defined in 120D.3.1.2.

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Table 120D–4—PRBS13Q pattern symbols used for jitter measurement

Label	Description	Gray coded PAM4 symbols	Index of first symbol	Index transition begins	Index transition ends	Index of last symbol	Threshold level
REF	Reference for symbol index	3333333	1	—	—	7	—
R03	0 to 3 rise	10000 330	1830	1834	1835	1837	$(V_0+V_3)/2$
F30	3 to 0 fall	23333 001	1269	1273	1274	1276	
R12	1 to 2 rise	0111111 2222221	3638	3644	3645	3651	$(V_1+V_2)/2$
F21	2 to 1 fall	022222 113	1198	1203	1204	1206	
R01	0 to 1 rise	100000 113	6835	6840	6841	6843	$(V_0+V_1)/2$
F10	1 to 0 fall	21111 003	2992	2996	2997	2999	
R23	2 to 3 rise	32222 330	6824	6828	6829	6831	$(V_2+V_3)/2$
F32	3 to 2 fall	033333 2222223	7734	7739	7740	7746	
R02	0 to 2 rise	10000 223	3266	3270	3271	3273	$(V_0+V_2)/2$
F20	2 to 0 fall	122222 0000002	7282	7287	7288	7294	
R13	1 to 3 rise	011111 331	133	138	139	141	$(V_1+V_3)/2$
F31	3 to 1 fall	23333 112	7905	7909	7910	7912	

The jitter is measured with a clock recovery unit (CRU) with a corner frequency of 4 MHz and a slope of 20 dB/decade. Jitter measurements are performed with transmitters on all lanes enabled and using identical transmitter equalizer settings. Transmitters on lanes not under test transmit PRBS31Q, or a valid 200GBASE-R or 400GBASE-R signal. PRBS31Q is described in 120.5.11.2.2.

The J4u, J_{RMS}, and Even-odd jitter specifications shall be met regardless of the transmit equalization setting.

120D.3.1.8.1 J4u and J_{RMS} jitter

For each transition i, $1 \le i \le 12$, of the transitions specified in Table 120D–4, obtain a set $S_i = \{t_i(1), t_i(2), ...\}$ of transition times modulo the period of the pattern. The 12 sets should be of equal size and the size of all sets should be chosen to enable calculation of J4u (as defined below) with sufficient accuracy.

Calculate the average of each set S_i, $T\text{avg}_i$, and subtract it from all elements of that set, to create a set $S0_i = \{t_i(1) - T\text{avg}_i, t_i(2) - T\text{avg}_i, ...\}$.

Combine the sets $S0_i$, i=1 to 12, to create an estimated probability distribution $f_J(t)$.

J4u is defined as the time interval that includes all but 10^{-4} of $f_J(t)$, from the 0.005th to the 99.995th percentile of $f_J(t)$.

J_{RMS} is defined as the standard deviation of $f_J(t)$.

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120D.3.1.8.2 Even-odd Jitter

For one of the 12 specific transitions in PRBS13Q in Table 120D–4:

a) Trigger once in 3 repeats of the PRBS13Q test pattern
   1) Obtain the mean time ($T3$) for this transition in the first PRBS13Q.
   2) Obtain the mean time ($T4$) for the same transition in the second PRBS13Q.
b) The difference between the two means ($T4 – T3$), is the estimated period of the repeating pattern

For each of the 12 specific transitions in PRBS13Q in Table 120D–4:

a1) Trigger once in 2 repeats of the PRBS13Q test pattern.
   1) Obtain the mean time ($T1$) for the specific transition in the first PRBS13Q.
   2) Obtain the mean time ($T2$) for the same transition in the second PRBS13Q.
b1) Calculate even-odd jitter for this transition as $|(T2 – T1) – (T4 – T3)|$

Even-odd jitter EOJ is the maximum of the 12 measurements.

NOTE 1—Both of ($T2 – T1$) and ($T4 – T3$) are about 8191 UI, which is much larger than the EOJ value. Hence, each of $T1$ through $T4$ should have high precision.

NOTE 2—Even-odd jitter has been referred to as *duty cycle distortion* by other Physical Layer specifications for operation over electrical backplane or twinaxial copper cable assemblies (see 72.7.1.9). The term *even-odd jitter* is used here to distinguish it from the duty cycle distortion referred to by Physical Layer specifications for operation over fiber optic cabling.

120D.3.2 200GAUI-4 and 400GAUI-8 C2C receiver characteristics

A 200GAUI-4 or a 400GAUI-8 chip-to-chip receiver shall meet the specifications given in Table 120D–5.

Table 120D–5—200GAUI-4 and 400GAUI-8 C2C receiver characteristics at TP5a

Parameter	Reference	Value	Units
Differential input return loss (min)	120D.3.1.1	Equation (120D–2)	dB
Differential-to-common-mode input return loss	93.8.2.2	Equation (93–5)	dB
Interference tolerance	120D.3.2.1	Table 120D–6	—
Jitter tolerance	120D.3.2.2	Table 120D–7	—

120D.3.2.1 Receiver interference tolerance

Receiver interference tolerance is defined by the procedure in Annex 93C with the exception that transmitter equalization is configured by management (see 120D.3.2.3) to the settings that provide the lowest PCS FEC symbol error ratio. The receiver on each lane shall meet the PCS FEC symbol error ratio requirement with channels matching the Channel Operating Margin (COM) and loss parameters for Test 1 and Test 2 in Table 120D–6. The following additional considerations apply to the interference tolerance test.

a) The test transmitter is constrained such that for any transmitter equalizer setting the differential peak-to-peak voltage (see 93.8.1.3) is less than or equal to 800 mV.
b) The return loss of the test setup in Figure 93C–4 measured at TP5 replica towards TPt meets the requirements of Equation (93–2).
c) The lower frequency bound for the noise spectral density constraints, f_{NSD1}, is 1 GHz.

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d) The transmitter device package model $S^{(tp)}$ is omitted from Equation (93A–3) in the calculation of COM. The filtered voltage transfer function $H^{(k)}(f)$ calculated in Equation (93A–19) uses the filter $H_t(f)$ defined by Equation (93A–46), where T_r is calculated as $T_r = 1.09 \times T_{rm} - 4.32$ ps and T_{rm} is the measured 20% to 80% transition time of the signal at TP0a. T_{rm} is measured using the method in 120E.3.1.5. T_{rm} is measured with *Local_eq_cm1* and *Local_eq_c*1 set to zero (see 120D.3.1.5).

e) For the calculation of test channel COM, the following parameters are based on values measured from the test transmitter. The parameter SNR_{TX} is set to the measured value of SNDR with *Np*=13, the parameter R_{LM} is set to the measured value of R_{LM}, and the parameters A_{DD} and σ_{RJ} are calculated from the measured values of J4u and J_{RMS} using Equation (120D–10), and Equation (120D–11), respectively.

f) Other COM parameters are set according to the values in Table 120D–8.

g) COM is calculated using both Test 1 and Test 2 device package model transmission line lengths listed in Table 120D–8 on the receiver side. The value of COM is taken as the lower of the two calculated values.

h) The test pattern is the scrambled idle test pattern defined in 119.2.4.9.

i) As an alternative to using the scrambled idle test pattern and measuring FEC symbol error ratio it is permissible to use the PRBS31Q pattern as described in 120.5.11.2.2 and bit error ratio testing. In this case the required bit error ratio is equal to the required FEC symbol error ratio divided by 10. Note that this requirement can be somewhat more stringent than using the scrambled idle test pattern and measuring FEC symbol error ratio, and therefore failing this test requirement with the PRBS31Q pattern does not necessarily imply a failure of the interference tolerance test.

j) A test system with a fourth-order Bessel-Thomson low pass response with 33 GHz 3 dB bandwidth is to be used for measurement of the signal applied by the pattern generator and for measurements of the broadband noise.

$$A_{DD} = \left(\left(\frac{J4u}{2}\right) + Q4\sqrt{\left((Q4^2+1)\times {J_{RMS}}^2 - \left(\frac{J4u}{2}\right)^2\right)}\right)/(Q4^2+1) \quad (120D–10)$$

$$\sigma_{RJ} = \left(\frac{J4u}{2} - A_{DD}\right)/(Q4) \quad (120D–11)$$

where $Q4$ is 3.8906.

Table 120D–6—Receiver interference tolerance parameters

Parameter	Test 1 (low loss)			Test 2 (high loss)			Units
	Min	Max	Target	Min	Max	Target	
PCS FEC Symbol error ratio[a]	—	10^{-4}	—	—	10^{-4}	—	—
Insertion loss at 13.2813 GHz[b]	9.5	10.5	—	19.5	20.5	—	dB
RSS_DFE4[c]	0.025	—	—	0.05	—	—	—
COM including effects of broadband noise[d]	—	—	3	—	—	3	dB

[a] The FEC symbol error ratio is measured in step 10 of the receiver interference tolerance method defined in 93C.2
[b] Measured between TPt and TP5 (see Figure 93C–4).
[c] RSS_DFE4 is described in 93A.2.
[d] The COM value is the target for the receiver noise level calibration defined in 93C.2 step 7. The channel noise voltage applied in 93C.2 step 8 should be as close as practical to the value needed to produce the target COM. If higher amplitude values are used, this would demonstrate margin to the specification but this is not required for compliance.

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120D.3.2.2 Receiver jitter tolerance

Receiver jitter tolerance is verified for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 120D–7. The test setup shown in Figure 93–12, or its equivalent, is used. The test channel meets the insertion loss requirement for Test 2 in Table 120D–6. The synthesizer frequency is set to the specified jitter frequency and the synthesizer output amplitude is adjusted until the specified peak-to-peak jitter amplitude for that frequency is measured at TP0a. The test procedure is the same as the one described in 120D.3.2.1, with the following exceptions:

a) No broadband noise is added.

b) The test channel COM, calculated per items d) through g) in 120D.3.2.1, is at least 3 dB.

c) For the COM parameter calibration described in 120D.3.2.1 item e), the test channel transmitter J_{RMS} and J4u values are measured with the jitter frequency and amplitude set according to Case F from Table 120D–7.

d) As an alternative to using the scrambled idle test pattern and measuring FEC symbol error ratio it is permissible to use the PRBS31Q pattern as described in 120.5.11.2.2 and bit error ratio testing. In this case the required bit error ratio is equal to the required FEC symbol error ratio divided by 10. Note that this requirement can be somewhat more stringent than using the scrambled idle test pattern and measuring FEC symbol error ratio, and therefore failing this test requirement with the PRBS31Q pattern does not necessarily imply a failure of the jitter tolerance test.

The receiver under test shall meet the PCS FEC symbol error ratio requirements for each case in Table 120D–7.

Table 120D–7—200GAUI-4 and 400GAUI-8 C2C receiver jitter tolerance parameters

Parameter	Case A	Case B	Case C	Case D	Case E	Case F	Units
PCS FEC Symbol error ratio	10^{-4}	10^{-4}	10^{-4}	10^{-4}	10^{-4}	10^{-4}	—
Jitter frequency	0.04	0.4	1.333	4	12	40	MHz
Jitter amplitude (pk-pk)	5	0.5	0.15	0.05	0.05	0.05	UI

120D.3.2.3 Transmitter equalization feedback (optional)

Transmitter equalization feedback is an optional capability for a 200GAUI-4 or a 400GAUI-8 chip-to-chip receiver. If implemented, it shall operate as described in this subclause.

Transmitter equalization feedback is generated for each lane (0 through 3 for 200GAUI-4 C2C and 0 through 7 for 400GAUI-8 C2C) and direction (transmit and receive) independently. The variables that control transmitter equalization feedback are specific for each lane and direction.

A 200GAUI-4 or a 400GAUI-8 chip-to-chip receiver may generate a request to change the transmit equalization coefficients of the remote transmitter to new values by setting the *Request_flag* variable to 1. The variables *Requested_eq_cm1* and *Requested_eq_c1* indicate the requested values of *Local_eq_cm1* and *Local_eq_c1*, respectively, in the remote transmitter (see Table 120D–2 and Table 120D–3). The requested setting may be generated from the remote 200GAUI-4 or 400GAUI-8 chip-to-chip transmitter's equalization setting, which is stored in variables *Remote_eq_cm1* and *Remote_eq_c1*, and from information internal to the receiver, in an implementation specific manner.

When a 200GAUI-4 or a 400GAUI-8 chip-to-chip receiver does not request a change of the remote transmitter's transmit equalization setting, it sets the *Request_flag* variable to 0. A 200GAUI-4 or a

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400GAUI-8 chip-to-chip receiver that does not implement transmitter equalization feedback always sets *Request_flag* to 0.

If a Clause 45 MDIO is implemented, the variables *Request_flag, Requested_eq_cm1, Requested_eq_c1, Remote_eq_cm1,* and *Remote_eq_c1* for each lane and direction are accessible through registers 1.500 through 1.507 for receive, and 1.516 through 1.523 for transmit (see 45.2.1.135 through 45.2.1.138).

An example of a possible transmitter equalization tuning process using transmitter equalization feedback is provided in 83D.5. Note that 400GAUI-8 C2C uses a different number of lanes and both 200GAUI-4 and 400GAUI-8 use a different register set to those in 83D.5.

120D.4 200GAUI-4 and 400GAUI-8 chip-to-chip channel characteristics

120D.4.1 Channel Operating Margin

The Channel Operating Margin (COM), computed using the procedure in 93A.1, where T_r is 13 ps for $H_t(f)$ in Equation (93A–19), and the parameters in Table 120D–8, shall be greater than or equal to 3 dB. This minimum value allocates margin for practical limitations on the receiver implementation as well as the allowed transmitter equalization coefficients.

Table 120D–8—COM parameter values

Parameter	Symbol	Value	Units
Signaling rate	f_b	26.5625	GBd
Maximum start frequency	$f_{\min}$	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface Transmission line characteristic impedance	 C_d z_p z_p C_p Z_c	 1.8×10^{-4} 12 30 1.1×10^{-4} 95	 nF mm mm nF Ω
Single-ended reference resistance	R_o	50	Ω
Single-ended termination resistance	R_d	50	Ω
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.6	—
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.15 0 0.05	—
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	—

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Table 120D–8—COM parameter values *(continued)*

Parameter	Symbol	Value	Units
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –15 0 1	dB
Continuous time filter, DC gain 2 Minimum value Maximum value Step size	g_{DC2}	 –4 0 1	dB
Continuous time filter, zero frequency for $g_{DC} = 0$	f_z	$f_b/2.5$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b/2.5$ $2 \times f_b$	GHz
Continuous time filter, low frequency pole/zero	f_{LF}	$f_b/40$	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 Av A_{fe} A_{ne}	 0.418 0.418 0.604	 V V V
Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.95	
Transmitter signal-to-noise ratio	SNR_{TX}	31	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	10	UI
Normalized DFE coefficient magnitude limit, for $n = 1$ for $n = 2$ to N_b	$b_{max}(n)$	 0.5 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_o	2.6×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-5}	—

120D.4.2 Channel return loss

The differential return loss of the channel shall meet Equation (120D–12) if the computed value of the Channel Operating Margin (COM) is less than or equal to 4 dB. For COM greater than 4 dB it is recommended that the differential return loss of the channel meet Equation (120D–12).

$$RL_d(f) \geq \begin{cases} 12 & 0.05 \leq f \leq f_b/4 \\ 12 - 15\log_{10}(4f/f_b) & f_b/4 < f \leq f_b \end{cases} \quad \text{dB} \qquad \text{(120D–12)}$$

where

f is the frequency in GHz
f_b is the signaling rate (26.5625) in GHz
$RL(f)$ is the return loss at frequency f

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The differential return loss limit is illustrated in Figure 120D–8.

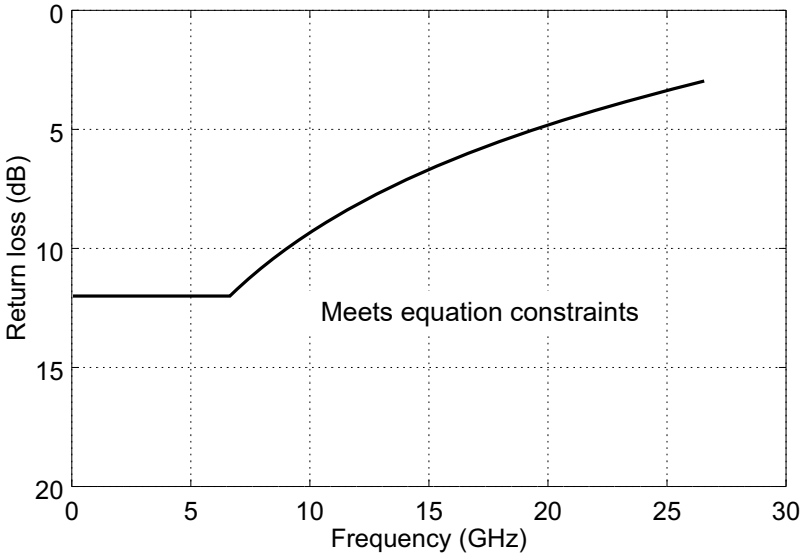

Figure 120D–8—Channel differential return loss limit

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120D.5 Protocol implementation conformance statement (PICS) proforma for Annex 120D, Chip-to-chip 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2C) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2C)[308]

120D.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 120D, Chip-to-chip 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2C) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2C), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

120D.5.2 Identification

120D.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

120D.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 120D, Chip-to-chip 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2C) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2C)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[308]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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120D.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	120D.1	Four independent data paths in each direction for 200GAUI-4 C2C and eight independent data paths in each direction for 400GAUI-8 C2C	M	Yes [ ]
*CHAN	Channel	120D.4	Items marked with CHAN include channel specifications not applicable to a PMA manufacturer	O	Yes [ ] No [ ]

120D.5.4 PICS proforma tables for Chip-to-chip 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2C) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2C)

120D.5.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	120D.3.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TC2	Peak-to-peak differential output voltage	120D.3.1	1200 mV (max)	M	Yes [ ]
TC3	Peak-to-peak differential output voltage, transmitter disabled	120D.3.1	Less than or equal to 30 mV	M	Yes [ ]
TC4	DC common-mode voltage	120D.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC5	AC common-mode output voltage	120D.3.1	30 mV RMS with respect to signal ground	M	Yes [ ]
TC6	Differential output return loss	120D.3.1	Meets Equation (120D–2) constraints	M	Yes [ ]
TC7	Common-mode output return loss	120D.3.1	Meets Equation (93–4) constraints	M	Yes [ ]
TC8	Output waveform	120D.3.1	Meets Table 120D–1 constraints	M	Yes [ ]
TC9	Output jitter	120D.3.1	Meets Table 120D–1 constraints	M	Yes [ ]
TC10	Transmit equalization	120D.3.1.5	Each successive step results in a monotonic change	M	Yes [ ]
TC11	Transmitter Output residual ISI	120D.3.1	Meets Table 120D–1 constraints	M	Yes [ ]
TC12	Signal-to-noise-and-distortion ratio	120D.3.1	Meets Table 120D–1 constraints	M	Yes [ ]

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120D.5.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	120D.3.2	Meets Equation (120D–2) constraints	M	Yes [ ]
RC2	Differential-to-common-mode input return loss	120D.3.2	Meets Equation (93–5) constraints	M	Yes [ ]
RC3	Interference tolerance	120D.3.2.1	Satisfy requirements in Table 120D–6	M	Yes [ ]
RC4	Jitter tolerance	120D.3.2.2	Satisfy requirements in Table 120D–7	M	Yes [ ]

120D.5.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	120D.4.1	Greater than or equal to 3 dB	CHAN: M	Yes [ ]
CC2	Return loss for channels with COM less than or equal to 4 dB	120D.4.2	Meets Equation (120D–12) constraints	CHAN: M	Yes [ ]

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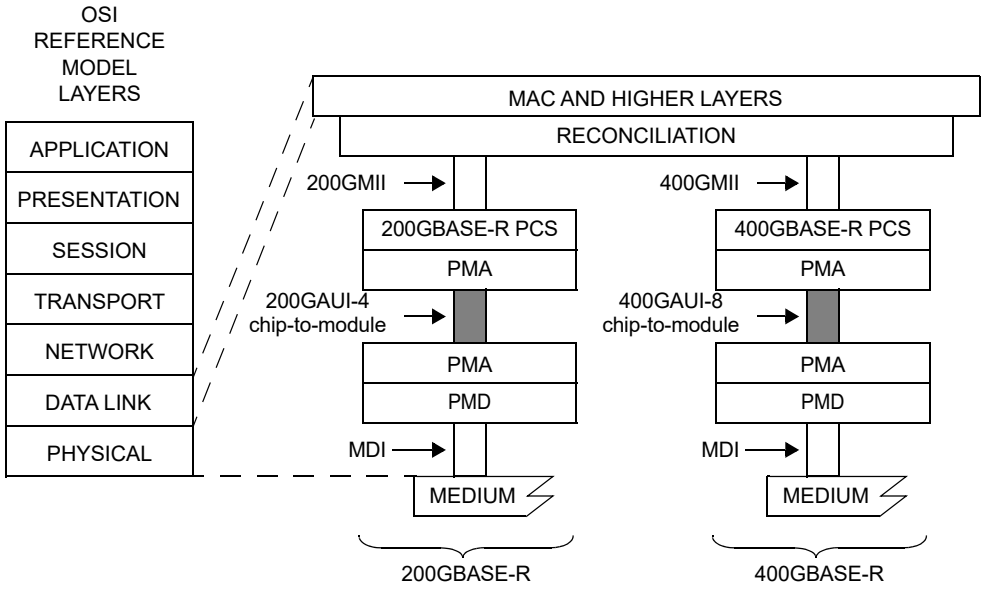
Annex 120E

(normative)

Chip-to-module 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2M) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2M)

120E.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2M) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2M). Figure 120E–1 shows the relationship of the 200GAUI-4 and 400GAUI-8 C2M interfaces to the ISO/IEC Open System Interconnection (OSI) reference model. The chip-to-module interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable module interfaces.



200GAUI-4 = 200 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GAUI-8 = 400 Gb/s EIGHT-LANE ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120E–1—Example 200GAUI-4 and 400GAUI-8 chip-to-module relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

The sublayers (including the PCS and associated FEC) for each PHY that can optionally include a 200GAUI-4 C2M or 400GAUI-8 C2M are summarized in the tables in 116.1.4 and are specified in the corresponding PMD clause. The positioning of the 200GAUI-4 C2M or 400GAUI-8 C2M relative to other sublayers is shown in 120.1 with further examples in Annex 120A.

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The 200GAUI-4 C2M link is described in terms of a host 200GAUI-4 C2M component, a 200GAUI-4 C2M channel with associated insertion loss, and a module 200GAUI-4 C2M component. Figure 120E–2 depicts a typical 200GAUI-4 C2M application and summarizes the differential insertion loss budget associated with the chip-to-module application. The supported insertion loss budget is characterized by Equation (120E–1) and illustrated in Figure 120E–4. The 200GAUI-4 C2M interface comprises independent data paths in each direction. Each data path contains four differential lanes using PAM4 signaling, where the highest differential level corresponds to the symbol three and the lowest level corresponds to the symbol zero. Each lane is AC-coupled within the module.

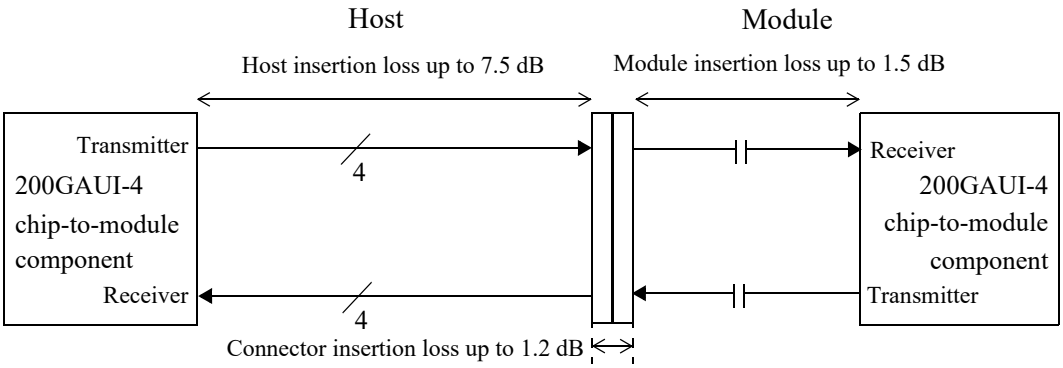

Figure 120E–2—200GAUI-4 chip-to-module insertion loss budget at 13.28 GHz

The 400GAUI-8 C2M link is described in terms of a host 400GAUI-8 C2M component, a 400GAUI-8 C2M channel with associated insertion loss, and a module 400GAUI-8 C2M component. Figure 120E–3 depicts a typical 400GAUI-8 C2M application and summarizes the differential insertion loss budget associated with the chip-to-module application. The recommended insertion loss budget is characterized by Equation (120E–1) and illustrated in Figure 120E–4. The 400GAUI-8 C2M interface comprises independent data paths in each direction. Each data path contains eight differential lanes using PAM4 signaling, where the highest differential level corresponds to the symbol three and the lowest level corresponds to the symbol zero. Each lane is AC-coupled within the module.

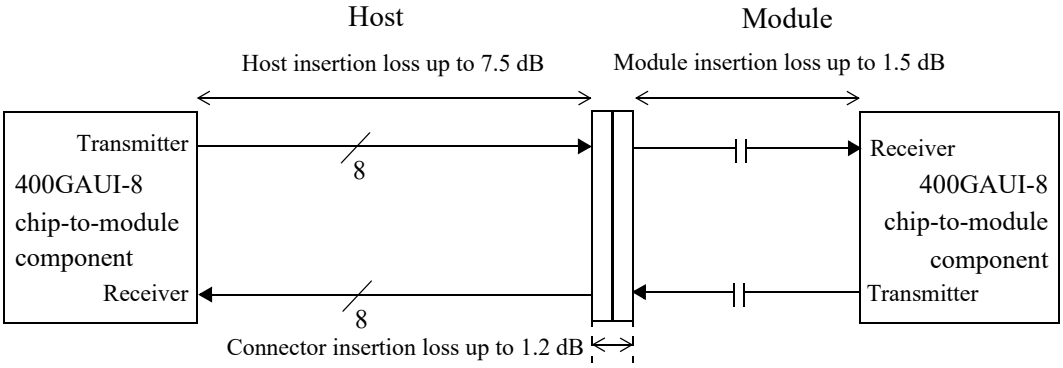

Figure 120E–3—400GAUI-8 chip-to-module insertion loss budget at 13.28 GHz

The nominal signaling rate for each lane is 26.5625 GBd. The chip-to-module interface is defined using a specification and test methodology that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.0 [B58].

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$$Insertion\_loss(f) \le \left\{ \begin{array}{cc} 0.05 + 1.8\sqrt{f} + 0.2705f & 0.01 \le f \le 13.28 \\ -4.0096 + 1.07f & 13.28 < f \le 26.5625 \end{array} \right\} (\text{dB}) \quad (120\text{E–}1)$$

where

f is the frequency in GHz

Insertion_loss(f) is the 200GAUI-4 or 400GAUI-8 chip-to-module insertion loss

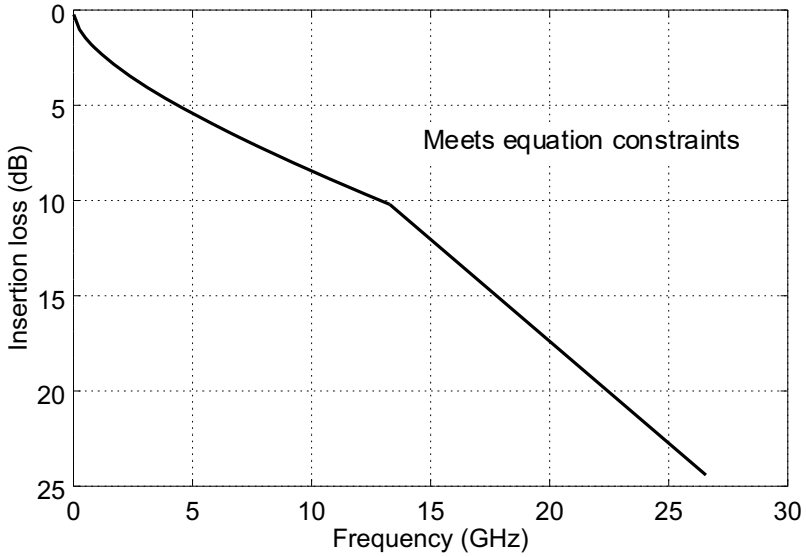

Figure 120E–4—Recommended 200GAUI-4 or 400GAUI-8 chip-to-module channel insertion loss

120E.1.1 Bit error ratio

The bit error ratio (BER) when processed according to Clause 120 shall be less than 10^{-5}.

120E.2 200GAUI-4 and 400GAUI-8 chip-to-module compliance point definitions

The electrical characteristics for the 200GAUI-4 and 400GAUI-8 chip-to-module interfaces are defined at compliance points for the host and module, respectively. Reference test fixtures, called compliance boards, are used to access the electrical specification parameters. Figure 120E–5 depicts the location of compliance points when measuring host 200GAUI-4 or 400GAUI-8 C2M compliance. The output of the Host Compliance Board (HCB) is used to verify the host electrical output signal at TP1a. Similarly, the input of the HCB at TP4a is used to verify the host input compliance.

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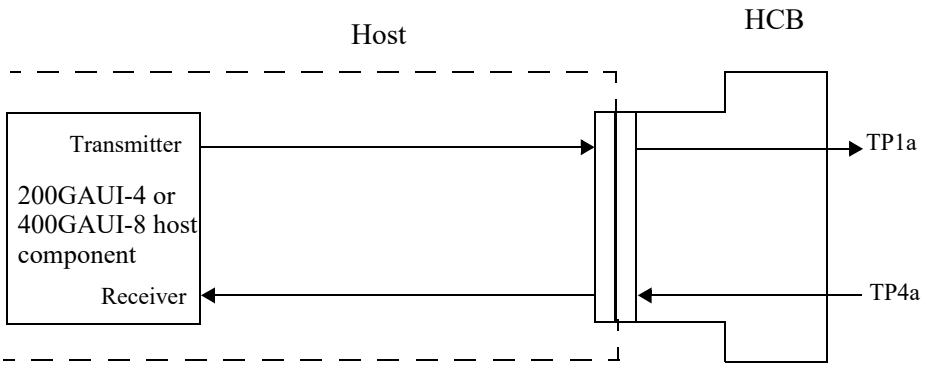

Figure 120E–5—Host 200GAUI-4 or 400GAUI-8 C2M compliance points

Figure 120E–6 depicts the location of compliance points when measuring module 200GAUI-4 or 400GAUI-8 C2M compliance. The output of the Module Compliance Board (MCB) is used to verify the module electrical output signal at TP4. Similarly, the input of the MCB at TP1 is used to verify the module input compliance. Additional details on the requirements for the MCB and HCB are given in 120E.4.1.

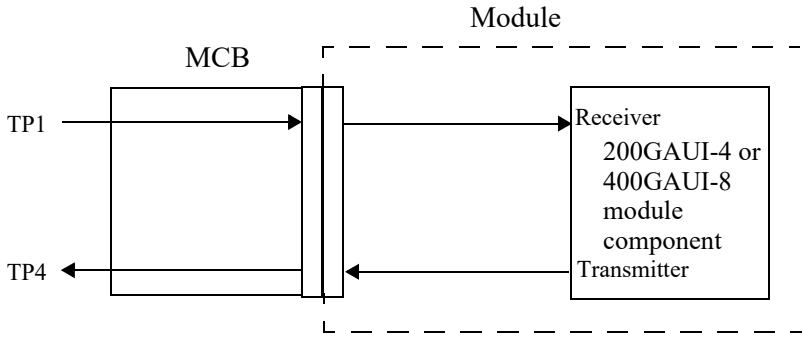

Figure 120E–6—Module 200GAUI-4 or 400GAUI-8 C2M compliance points

120E.3 200GAUI-4 and 400GAUI-8 chip-to-module electrical characteristics

120E.3.1 200GAUI-4 and 400GAUI-8 C2M host output characteristics

A 200GAUI-4 or a 400GAUI-8 C2M host output shall meet the specifications given in Table 120E–1.

A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

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Table 120E–1—200GAUI-4 and 400GAUI-8 C2M host output characteristics at TP1a

Parameter	Reference	Value	Units
Signaling rate per lane (range)	120E.3.1.1	26.5625 ± 100 ppm	GBd
DC common-mode output voltage (max)	120E.3.1.2	2.8	V
DC common-mode output voltage (min)	120E.3.1.2	–0.3	V
Single-ended output voltage (max)	120E.3.1.2	3.3	V
Single-ended output voltage (min)	120E.3.1.2	–0.4	V
AC common-mode output voltage (max, RMS)	120E.3.1.2	17.5	mV
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	120E.3.1.2	 35 880	mV
ESMW (Eye symmetry mask width)	120E.4.2	0.22	UI
Eye height, differential (min)	120E.4.2	32	mV
Vertical eye closure (max)	120E.4.3	12	dB
Differential output return loss (min)	83E.3.1.3	Equation (83E–2)	dB
Common to differential mode conversion return loss (min)	83E.3.1.3	Equation (83E–3)	dB
Differential termination mismatch (max)	120E.3.1.4	10	%
Transition time (min, 20% to 80%)	120E.3.1.5	10	ps

120E.3.1.1 Signaling rate and range

The 200GAUI-4 and 400GAUI-8 C2M signaling rate is 26.5625 GBd ± 100 ppm per lane. This translates to a nominal unit interval of 37.647059 ps.

120E.3.1.2 Signal levels

The differential output voltage v_{di} is defined to be the difference between the single-ended output voltages, SL*i*<p> minus SL*i*<n>. The common-mode voltage v_{cmi} is defined to be one half of the sum of SL*i*<p> and SL*i*<n>. These definitions are illustrated by Figure 120E–7.

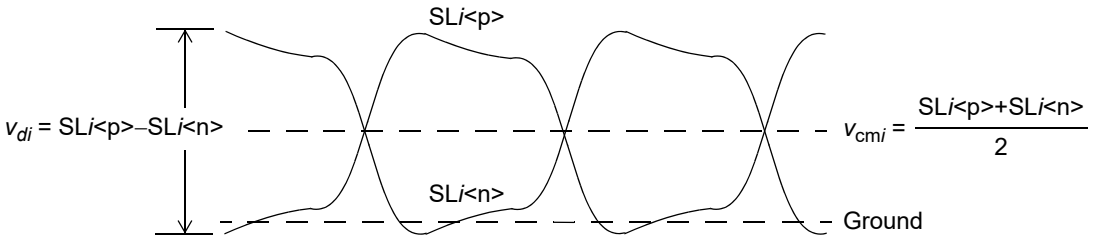

Figure 120E–7—Voltage definitions

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The DC common-mode output voltage and AC common-mode output voltage are defined with respect to signal ground.

Unless otherwise noted, differential and common-mode signal voltages are measured with a PRBS13Q test pattern.

120E.3.1.3 Output return loss

Differential output return loss is defined in 83E.3.1.3.

120E.3.1.4 Differential termination mismatch

Differential termination mismatch is defined in 86A.5.3.2.

120E.3.1.5 Transition time

In this annex, transition times are specified for transitions between three consecutive “zero” symbols and three consecutive “three” symbols, or vice versa. The specified times are between the crossings of 20% and 80% levels of the signal.

The test pattern used is PRBS13Q, the transitions within sequences of three zeros and three threes, and three threes and three zeros, respectively, are measured. These are PAM4 symbols 1820 to 1825 and 2086 to 2091, respectively, where symbols 1 to 7 are the run of seven threes. The 0% level and the 100% level are defined as the average signal within windows from –1.5 UI to –1 UI and from 1.5 UI to 2 UI relative to the edge.

The waveform is observed through a fourth-order Bessel-Thomson low-pass response with a 3 dB bandwidth of 33 GHz.

NOTE—This definition is not the same as the rise and fall times typically reported by an oscilloscope from an eye diagram, which take all the edges into account.

120E.3.1.6 Host output eye width and eye height

Figure 120E–8 depicts an example host output eye width and eye height test configuration. Host output eye width and eye height are measured at TP1a using compliance boards defined in 120E.4.1. The host output eye is measured using a reference receiver with a continuous time linear equalizer (CTLE) defined in 120E.3.1.7. Eye width and eye height measurement methodology is described in 120E.4.2. All counter-propagating signals shall be asynchronous to the co-propagating signals using the PRBS13Q or PRBS31Q pattern, or a valid 200GBASE-R or 400GBASE-R signal. PRBS13Q is described in 120.5.11.2.1. PRBS31Q is described in 120.5.11.2.2. For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated. The crosstalk generator is calibrated at TP4 (without the use of a CTLE) with target differential peak-to-peak amplitude of 900 mV and slew time of 12 ps between ± 0.27 V.

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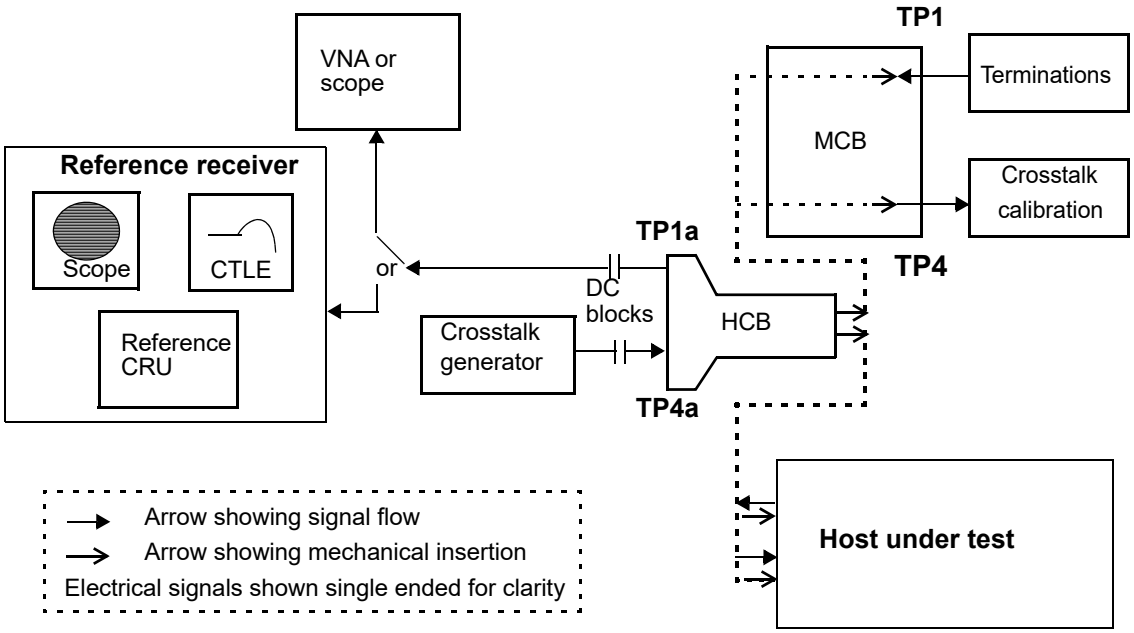

Figure 120E–8—Example host output test configuration

120E.3.1.7 Reference receiver for eye width and eye height evaluation

The reference receiver is used to measure eye width and eye height. The reference receiver includes a selectable continuous time linear equalizer (CTLE), which is described by Equation (120E–2) with coefficients given in Table 120E–2 and illustrated in Figure 120E–9. The equalizer may be implemented in software; however, the measured signal is not averaged.

$$H(f) = \frac{GP_1P_2P_{\mathrm{LF}}}{Z_1Z_{\mathrm{LF}}} \times \frac{\mathrm{j}2\pi f + Z_1}{(\mathrm{j}2\pi f + P_1)(\mathrm{j}2\pi f + P_2)} \times \frac{\mathrm{j}2\pi f + Z_{\mathrm{LF}}}{\mathrm{j}2\pi f + P_{\mathrm{LF}}} \quad (120\text{E–}2)$$

where

$H(f)$	is the CTLE transfer function
G	is the CTLE gain
P_1, P_2	are the CTLE poles in Grad/s
Z_1	is the CTLE zero in Grad/s
P_{LF}	is the low frequency CTLE pole in Grad/s
Z_{LF}	is the low frequency CTLE zero in Grad/s
j	is the square root of –1
f	is the frequency in GHz

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Table 120E–2—Reference CTLE coefficients

Peaking (dB)	G	$\frac{P_1}{2\pi}$	$\frac{P_2}{2\pi}$	$\frac{Z_1}{2\pi}$	$\frac{P_{LF}}{2\pi}$	$\frac{Z_{LF}}{2\pi}$
1	0.891251	26.5625	14.1	9.463748	1.2	1.2
1.5	0.841395	26.5625	14.1	9.248465	1.2	1.15
2	0.794328	26.5625	14.1	9.069645	1.2	1.1
2.5	0.749894	26.5625	14.1	8.640319	1.2	1.075
3	0.707946	26.5625	14.1	8.255665	1.2	1.05
3.5	0.668344	26.5625	14.1	7.906766	1.2	1.025
4	0.630957	26.5625	14.1	7.58765	1.2	1
4.5	0.595662	26.5625	14.1	7.076858	1.2	1
5	0.562341	26.5625	14.1	6.614781	1.2	1
5.5	0.530884	26.5625	14.1	6.193091	1.2	1
6	0.501187	26.5625	14.1	5.805801	1.2	1
6.5	0.473151	26.5625	14.1	5.448395	1.2	1
7	0.446684	26.5625	14.1	5.117337	1.2	1
7.5	0.421697	26.5625	14.1	4.809777	1.2	1
8	0.398107	26.5625	14.1	4.523367	1.2	1
8.5	0.375837	26.5625	14.1	4.256129	1.2	1
9	0.354813	26.5625	14.1	4.006377	1.2	1

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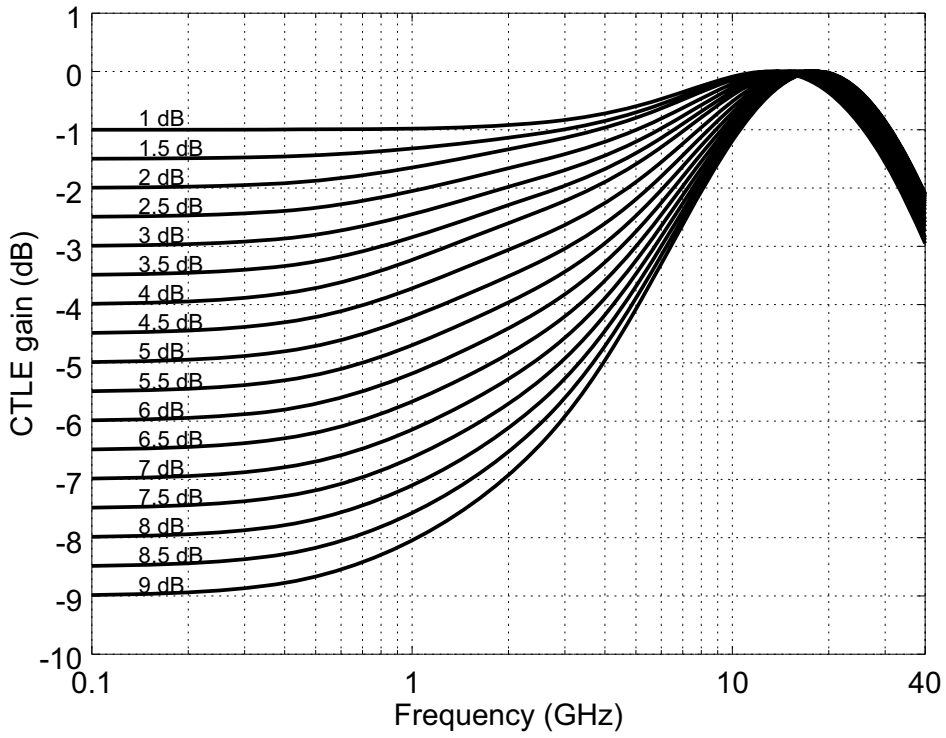

Figure 120E–9—Reference continuous time linear equalizer (CTLE) characteristic

120E.3.2 200GAUI-4 and 400GAUI-8 C2M module output characteristics

A 200GAUI-4 or a 400GAUI-8 C2M module output shall meet the specifications given in Table 120E–3. The low-frequency 3 dB cutoff of the output AC-coupling within the module should be less than 100 kHz. A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

Table 120E–3—200GAUI-4 and 400GAUI-8 C2M module output characteristics at TP4

Parameter	Reference	Value	Units
Signaling rate per lane (range)	120E.3.1.1	26.5625 ± 100 ppm	GBd
AC common-mode output voltage (max, RMS)	120E.3.1.2	17.5	mV
Differential peak-to-peak output voltage (max)	120E.3.1.2	900	mV
Near-end ESMW (Eye symmetry mask width)	120E.4.2	0.265	UI
Near-end Eye height, differential (min)	120E.4.2	70	mV
Far-end ESMW (Eye symmetry mask width)	120E.4.2	0.2	UI
Far-end Eye height, differential (min)	120E.4.2	30	mV
Far-end pre-cursor ISI ratio	120E.3.2.1.2	–4.5 to +2.5	%

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Table 120E–3—200GAUI-4 and 400GAUI-8 C2M module output characteristics at TP4 *(continued)*

Parameter	Reference	Value	Units
Differential output return loss (min)	83E.3.1.3	Equation (83E–2)	dB
Common-to-differential-mode output return loss (min)	83E.3.1.3	Equation (83E–3)	dB
Differential termination mismatch (max)	120E.3.1.4	10	%
Transition time (min, 20% to 80%)	120E.3.1.5	9.5	ps
DC common-mode voltage (min)[a]	120E.3.1.2	–350	mV
DC common-mode voltage (max)[a]	120E.3.1.2	2850	mV

[a] DC common-mode voltage is generated by the host. Specification includes effects of ground offset voltage.

120E.3.2.1 Module output eye width, eye height, and pre-cursor ISI ratio

Figure 120E–10 depicts an example module output eye width and eye height test configuration. Module output eye width and eye height are measured at TP4 using compliance boards defined in 120E.4.1. The module output eye is measured using a reference receiver with a continuous time linear equalizer (CTLE) defined in 120E.3.2.1.1. Eye width and eye height measurement methodology is described in 120E.4.2. All counter-propagating signals shall be asynchronous to the co-propagating signals using the PRBS13Q or PRBS31Q pattern, or a valid 200GBASE-R or 400GBASE-R signal. PRBS13Q is described in 120.5.11.2.1 and PRBS31Q is described in 120.5.11.2.2. For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated. The crosstalk generator is calibrated at TP1a (without the use of a CTLE) with target differential peak-to-peak amplitude of 880 mV and target transition time of 19 ps.

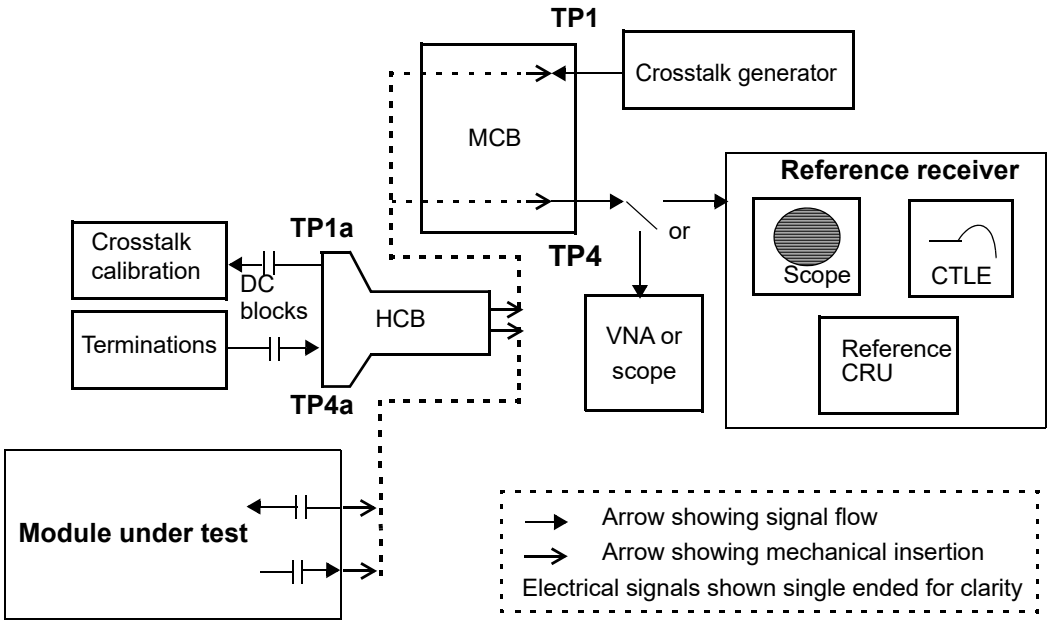

Figure 120E–10—Example module output test configuration

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120E.3.2.1.1 Reference receiver for module output evaluation

A reference receiver is used to measure module eye width and eye height. The reference receiver includes a selectable continuous time linear equalizer (CTLE), which is defined in 120E.3.1.7. The equalizer may be implemented in software; however, the measured signal is not averaged.

The near-end eye is measured with the reference receiver. Equalizer settings corresponding to less than or equal to 3 dB of peaking from Table 120E–2 may be used to meet the output eye width and height requirements.

For the far-end eye, the signal measured at TP4 is first convolved with a loss channel (~6.4 dB loss at Nyquist) that represents the worst case channel loss. The loss channel is the host trace defined in 92.10.7.1.1 with Z_p = 151 mm. The reference receiver is then used to measure the eye width and height. Any of the equalizer settings from Table 120E–2 may be used.

120E.3.2.1.2 Far-end pre-cursor ISI ratio

Capture the PRBS13Q waveform corresponding to the far-end eye (see 120E.3.2.1.1) and calculate the linear fit pulse using the procedure defined in 120D.3.1.3. Any setting of the reference CTLE for which the far-end eye width and height satisfy the limits in Table 120E–3, may be used.

The peak amplitude of the linear fit pulse is p_{max}. The pre-cursor ISI p_{pre} is the value of the linear fit pulse 1 UI prior to the time of the pulse peak. The pre-cursor ISI ratio is p_{pre} / p_{max}.

120E.3.3 200GAUI-4 and 400GAUI-8 C2M host input characteristics

A 200GAUI-4 or a 400GAUI-8 C2M host input shall meet the specifications given in Table 120E–4.

Table 120E–4—200GAUI-4 and 400GAUI-8 C2M host input characteristics

Parameter	Reference	Test point	Value	Units
Signaling rate, per lane (range)	120E.3.1.1	TP4a	26.5625 ± 100 ppm	GBd
Differential pk-pk input voltage tolerance (min)	120E.3.1.2	TP4	900	mV
Differential input return loss (min)	83E.3.3.1	TP4a	Equation (83E–5)	dB
Differential-to-common-mode input return loss (min)	83E.3.3.1	TP4a	Equation (83E–6)	dB
Host stressed input test[a]	120E.3.3.2	TP4	See 120E.3.3.2	
Differential termination mismatch (max)	120E.3.1.4	TP4a	10	%
Common-mode voltage[b] Min Max	120E.3.1.2	TP4a	 –0.3 2.8	V

[a]Meets BER specified in 120E.1.1.
[b]Generated by host, referred to host ground.

120E.3.3.1 Input return loss

Differential input return loss is defined in 83E.3.3.1.

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120E.3.3.2 Host stressed input test

The host stressed input tolerance is measured using the procedure defined in 120E.3.3.2.1. The input shall satisfy the input tolerance with the parameters in Table 120E–5.

Table 120E–5—Host stressed input parameters

Parameter	Value
Far-end ESMW (Eye symmetry mask width)	0.2 UI
Far-end Eye width	0.2 UI
Applied pk-pk sinusoidal jitter	Table 120E–6
Far-end Eye height	30 mV

120E.3.3.2.1 Host stressed input test procedure

The host stressed input test is summarized in Figure 120E–11. The stressed signal is applied at TP4a and is calibrated at TP4. A reference CRU with a corner frequency of 4 MHz and slope of 20 dB/decade is used to calibrate the stressed signal using the PRBS13Q Pattern (see 120.5.11.2.1). The reference receiver includes a selectable CTLE as specified in 120E.3.2.1.1. The stressed signal is generated by adding sinusoidal jitter, random jitter, and bounded uncorrelated jitter to a clean signal. The frequency and peak-to-peak amplitude of the sinusoidal jitter used for the host stressed input test is given in Table 120E–6.

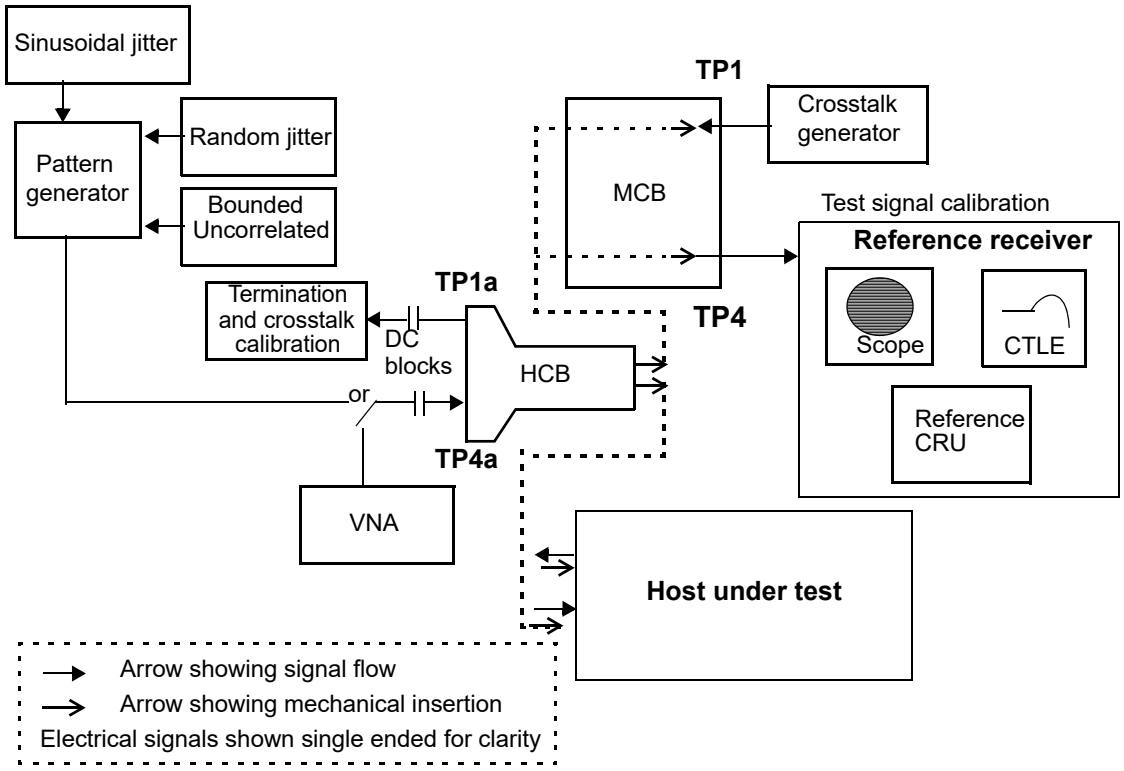

Figure 120E–11—Example host stressed input test

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Table 120E–6—Applied sinusoidal jitter

Parameter	Case A	Case B	Case C	Case D	Case E	Case F	Units
Jitter frequency	0.04	0.4	1.333	4	12	40	MHz
Jitter amplitude (pk-pk)	5	0.5	0.15	0.05	0.05	0.05	UI

Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the pattern. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9 with a signaling rate approximately 1/10 of the stressed pattern signaling rate (e.g., 2.65625 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low-pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value also has to be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the 200GAUI-4 and 400GAUI-8 C2C output jitter profile given in Table 120D–1.

The counter propagating crosstalk signals during calibration of the stressed signal are asynchronous with target amplitude of 880 mV peak-to-peak differential and 20% to 80% target transition time of 19 ps as measured at TP1a (without the use of a CTLE). The crosstalk signal transition time is calibrated with PRBS13Q. The pattern may be changed to a valid 400GBASE-R signal for amplitude calibration and the stressed input test. The PRBS13Q pattern is described in 120.5.11.2.1. For the case where the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane, so that the symbols on each lane are not correlated. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes active during the stressed input test.

The far-end eye height and eye width, measured to a probability of 10^{-5}, are then measured at TP4 with the reference receiver defined in 120E.3.2.1.1 using the measurement methodology given in 120E.4.2. Note that the reference receiver for far-end eye height and width measurements includes a loss channel. Random jitter and the pattern generator output levels are adjusted (without exceeding the differential pk-pk input voltage tolerance specification as shown in Table 120E–4) to result in the eye height for all three eyes and eye width for the smallest eye given in Table 120E–5 with the setting of the CTLE that maximizes the product of eye height and eye width.

The far-end pre-cursor ISI ratio is measured using the method defined in 120E.3.2.1.2 and it shall meet the specification in Table 120E–3. Pre-emphasis capability is likely to be required in the pattern generator to meet this requirement.

The pattern is then changed to Pattern 5, Pattern 3, or a valid 200GBASE-R/400GBASE-R signal for the input test which is conducted by inserting the HCB into the host under test. Patterns 3 and 5 are described in Table 124–9.

If the test is performed with pattern 3, the host BER may be calculated using the host's PMA test pattern checker (see 120.5.11.2.2). If the test is performed with pattern 5 or a valid 200GBASE-R/400GBASE-R signal, the BER may be calculated using the host's PCS Reed-Solomon decoder error counters (see 119.3.1), as the number of FEC symbol errors divided by the number of received bits. The number of received bits may be estimated based on the test time.

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120E.3.4 200GAUI-4 and 400GAUI-8 C2M module input characteristics

A 200GAUI-4 or a 400GAUI-8 C2M module input shall meet the specifications given in Table 120E–7. Channel equalization is provided by an adaptive equalizer in the module.

Table 120E–7—200GAUI-4 and 400GAUI-8 C2M module input characteristics

Parameter	Reference	Test point	Value	Units
Signaling rate per lane (range)	120E.3.1.1	TP1	26.5625 ± 100 ppm	GBd
Differential pk-pk input voltage tolerance (min)[a]	120E.3.1.2	TP1a	900	mV
Differential input return loss (min)	83E.3.3.1	TP1	Equation (83E–5)	dB
Differential-to-common-mode input return loss (min)	83E.3.3.1	TP1	Equation (83E–6)	dB
Differential termination mismatch (max)	120E.3.1.4	TP1	10	%
Module stressed input test[b]	120E.3.4.1	TP1a	See 120E.3.4.1	
Single-ended voltage tolerance range (min)	120E.3.1.2	TP1a	–0.4 to 3.3	V
DC common-mode voltage (min)[c]	120E.3.1.2	TP1	–350	mV
DC common-mode voltage (max)[c]	120E.3.1.2	TP1	2850	mV

[a] With the exception to 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
[b] Meets BER specified in 120E.1.1.
[c] DC common-mode voltage generated by the host. Specification includes effects of ground offset voltage.

120E.3.4.1 Module stressed input test

The module stressed input tolerance is measured using the procedure defined in 120E.3.4.1.1. The input shall satisfy the input tolerance with the parameters in Table 120E–8.

Table 120E–8—Module stressed input parameters

Parameter	Value
ESMW (Eye symmetry mask width)	0.22 UI
Eye width	0.22 UI
Applied pk-pk sinusoidal jitter	Table 120E–6
Eye height	32 mV

120E.3.4.1.1 Module stressed input test procedure

The module stressed input test is summarized in Figure 120E–12. The stressed signal is applied at TP1 and is calibrated at TP1a. A reference CRU with a corner frequency of 4 MHz and slope of 20 dB/decade is used to calibrate the stressed signal using a PRBS13Q pattern. The reference receiver includes a selectable CTLE as specified in 120E.3.1.7. The stressed signal is generated by adding sinusoidal jitter, random jitter, and

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bounded uncorrelated jitter to a clean signal, followed by frequency-dependent attenuation. The frequency-dependent attenuator represents the host channel and may be implemented with PCB traces. The amount of applied peak-to-peak sinusoidal jitter used for the module stressed input test is given in Table 120E–6. Bounded uncorrelated jitter provides a source of bounded high probability jitter uncorrelated with the signal stream. This jitter stress source may not be present in all stressed pattern generators or bit error ratio testers. It can be generated by driving the pattern generator external jitter modulation input with a filtered PRBS pattern. The PRBS pattern length should be between PRBS7 and PRBS9 with a signaling rate approximately 1/10 of the stressed pattern signaling rate (e.g., 2.65625 GBd). The clock source for the PRBS generator is asynchronous to the pattern generator clock source to assure non-correlation of the jitter. The low-pass filter that operates on the PRBS pattern to generate the bounded uncorrelated jitter should exhibit 20 dB/decade roll-off with a –3 dB corner frequency between 150 MHz and 300 MHz. This value also has to be below the upper frequency limit of the pattern generator external modulator input. Random jitter and bounded uncorrelated jitter are added such that the output of the pattern generator approximates the 200GAUI-4 and 400GAUI-8 C2C output jitter profile given in Table 120D–1. The target pattern generator 20% to 80% transition time at the input to the test channel in the module stressed input test is 10.5 ps. The return loss of the test system as measured at TP1 meets the specification given in Equation (83E–2).

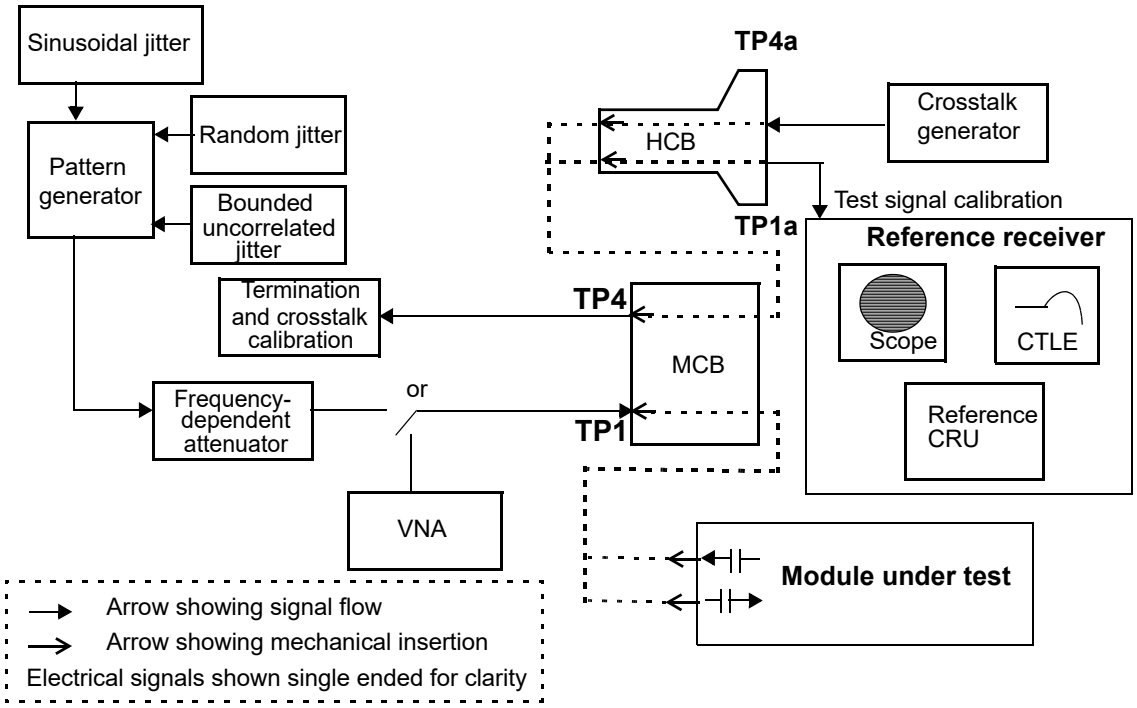

Figure 120E–12—Example module stressed input test

For the high loss case, pre-emphasis capability is likely to be required in the pattern generator to meet the TP1a eye height and eye width specifications.

The counter propagating crosstalk signals during calibration of the stressed signal are asynchronous with target amplitude of 900 mV peak-to-peak differential and target slew time between ± 270 mV of 12 ps as measured at TP4 (without the use of a CTLE). The crosstalk signal transition time is calibrated with a PRBS13Q pattern. The pattern may be changed to a valid 200GBASE-R/400GBASE-R signal for amplitude calibration and the stressed input test. The PRBS13Q pattern is described in 120.5.11.2.1. For the case where the PRBS13Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS13Q patterns on one lane and any other lane, so that the symbols on each lane are not correlated. Any one of these patterns is sufficient as a crosstalk aggressor with all lanes being active during the stressed input test.

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Two levels of frequency-dependent attenuation are used for the module stressed input test: high loss and low loss. For the high loss case, frequency-dependent attenuation is added such that the loss at 13.28 GHz from the output of the pattern generator to TP1a is 12.2 dB. The 12.2 dB loss represents 10.5 dB channel loss with an additional allowance for host transmitter package loss. Eye height and eye width are then measured at TP1a based on the eye measurement methodology given in 120E.4.2 and vertical eye closure is measured according to 120E.4.3. Random jitter and the pattern generator output levels are adjusted (without exceeding the differential pk-pk input voltage tolerance specification as shown in Table 120E–7) to result in the eye height for all three eyes and eye width for the smallest eye given in Table 120E–8 using the reference receiver with the setting of the CTLE that maximizes the product of eye height and eye width. This CTLE setting has to be greater than or equal to 7 dB. For the low loss case, discrete frequency-dependent attenuation is removed such that from the output of the pattern generator to TP1a comprises the mated HCB/MCB pair as described in 120E.4.1. Eye height and eye width at TP1a are then adjusted in the same way as described for the high loss case except that the restriction that the CTLE setting has to be greater than or equal to 7 dB does not apply. In both cases, the input vertical eye closure is less than 12 dB.

The pattern is then changed to Pattern 5, Pattern 3, or a valid 200GBASE-R/400GBASE-R signal for the input test, which is conducted by inserting the module into the MCB. Patterns 3 and 5 are described in Table 124–9.

If the test is performed with pattern 3, the module bit errors may be counted using a PMA test pattern checker (see 120.5.11.2.2) if this option is implemented in the module.

If the test is performed with pattern 5 or a valid 200GBASE-R/400GBASE-R signal, the module BER may be calculated by placing the module under test into local loopback (see 120.5.9) and feeding the module output into a compliant host or its equivalent. The BER may then be calculated using the host's PCS Reed-Solomon decoder error counters (see 119.3.1), as the number of FEC symbol errors divided by the number of received bits.

Methods of extracting the received bit pattern and counting errors other than the ones described above may be used if they generate equivalent results.

The number of received bits may be estimated based on the test time.

The module 200GAUI-4 or 400GAUI-8 C2M receiver under test shall meet the BER requirement as described in 120E.1.1 for both the high loss test and low loss test.

120E.4 200GAUI-4 and 400GAUI-8 C2M measurement methodology

This subclause describes common measurement tools and methodologies to be used for the 200GAUI-4 and 400GAUI-8 chip-to-module interface. Details of HCB and MCB characteristics are given in 120E.4.1 and details of the eye diagram measurement methodology are given in 120E.4.2.

120E.4.1 HCB/MCB characteristics

HCB characteristics are described in 92.11.1 where the HCB performs the equivalent function as the TP2 or TP3 test fixture with the exception that the upper frequency of 25 GHz is replaced with 26.5625 GHz. The MCB characteristics are described in 92.11.2 where the MCB performs the equivalent functionality as the cable assembly test fixture with the exception that the upper frequency of 25 GHz is replaced with 26.5625 GHz.

The mated compliance board characteristics are described in 92.11.3 where the MCB and HCB perform the equivalent functionality as the cable assembly test fixtures with the exceptions that the upper frequency of

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25 GHz is replaced with 26.5625 GHz, MDNEXT shall be less than 1.5 mV RMS, MDFEXT shall be less than 4.2 mV RMS, ICN shall be less than 4.4 mV RMS, FOM_{ILD} limit is 0.1 dB, and the reference insertion loss is given in Equation (120E–3) for 0.01 GHz ≤ f ≤ 25 GHz.

$$IL(f) = 0.471\sqrt{f} + 0.1194f + 0.002f^2 \quad \text{(dB)} \tag{120E–3}$$

where

f is the frequency in GHz
$IL(f)$ is the mated compliance board reference insertion loss

120E.4.2 Eye width and eye height measurement method

Eye diagrams in 200GAUI-4 and 400GAUI-8 chip-to-module are measured using a reference receiver. The reference receiver includes a fourth-order Bessel-Thomson low-pass filter response with 33 GHz 3 dB bandwidth, and a selectable continuous time linear equalizer (CTLE) to measure eye height and width. The pattern used for output eye diagram measurements is PRBS13Q. Unless specified otherwise the probabilities are relative to the number of PAM4 symbols measured. The following procedure should be used to obtain the eye height and eye width parameters, as illustrated by Figure 120E–13:

1) Capture the PRBS13Q using a clock recovery unit with a corner frequency of 4 MHz and slope of 20 dB/decade. The capture includes a minimum of 3 samples per symbol, or equivalent. Collect sufficient samples equivalent to at least 1.2 million PAM4 symbols to allow for construction of a normalized cumulative distribution function (CDF) to a probability of 10^{-5} without extrapolation.
2) Apply the reference receiver including the appropriate CTLE to the captured signal. For module compliance, any single CTLE setting as described in 120E.3.2.1.1 that meets both eye width and eye height requirements is acceptable. For host compliance, any single CTLE setting as described in 120E.3.1.7 that meets both eye width and eye height requirements is acceptable.
3) Use the differential equalized signal from step 2) to construct the CDF of the signal threshold crossing for both the left edge (MID0CDFL) and right edge (MID0CDFR) of the middle eye, as a function of the distance from the center of the eye. Calculate the time center of the middle eye width (TCmid) as the mid-point in time between MID0CDFR and MID0CDFL with a value of 10^{-3}. MID0CDFL and MID0CDFR are calculated as the cumulative sum of histograms of the zero crossing samples at the left and right edges of the middle eye normalized by the total number of sampled symbols. The MID0CDFL and MID0CDFR are equivalent to bath tub curves where the BER is plotted versus sampling time.
4) Use the differential equalized signal from step 2) to construct the CDF of the signal voltage of the middle eye within 0.025 UI of time TCmid, for both +1/3 (MIDCDF1) and –1/3 (MIDCDF0), as a function of the distance from the center of the eye. Calculate the eye height (Vmid) as the difference in voltage between MIDCDF1 and MIDCDF0 with a value of 10^{-5}. Calculate the voltage center (VCmid) of the middle eye as the mid-point in voltage between MIDCDF1 and MIDCDF0 with a value of 10^{-5}. MIDCDF0 and MIDCDF1 are calculated as the cumulative sum of histograms of the voltage at the top and bottom of the eye normalized by the total number of sampled bits.
5) Using the method in step 4), construct CDFs of signal voltages of the upper eye within 0.025 UI of time TCmid, and calculate the 10^{-5} upper eye height (Vupp). Calculate the voltage center (VCupp) of the upper eye as the mid-point in voltage between UPPCDF1 and UPPCDF0 with a value of 10^{-5}.
6) Using the method in step 4), construct CDFs of signal voltages of the lower eye within 0.025 UI of time TCmid, and calculate the 10^{-5} lower eye height (Vlow). Calculate the voltage center (VClow) of the lower eye as the mid-point in voltage between LOWCDF1 and LOWCDF0 with a value of 10^{-5}.
7) The eye height is defined as the minimum of Vmid, Vupp, and Vlow.

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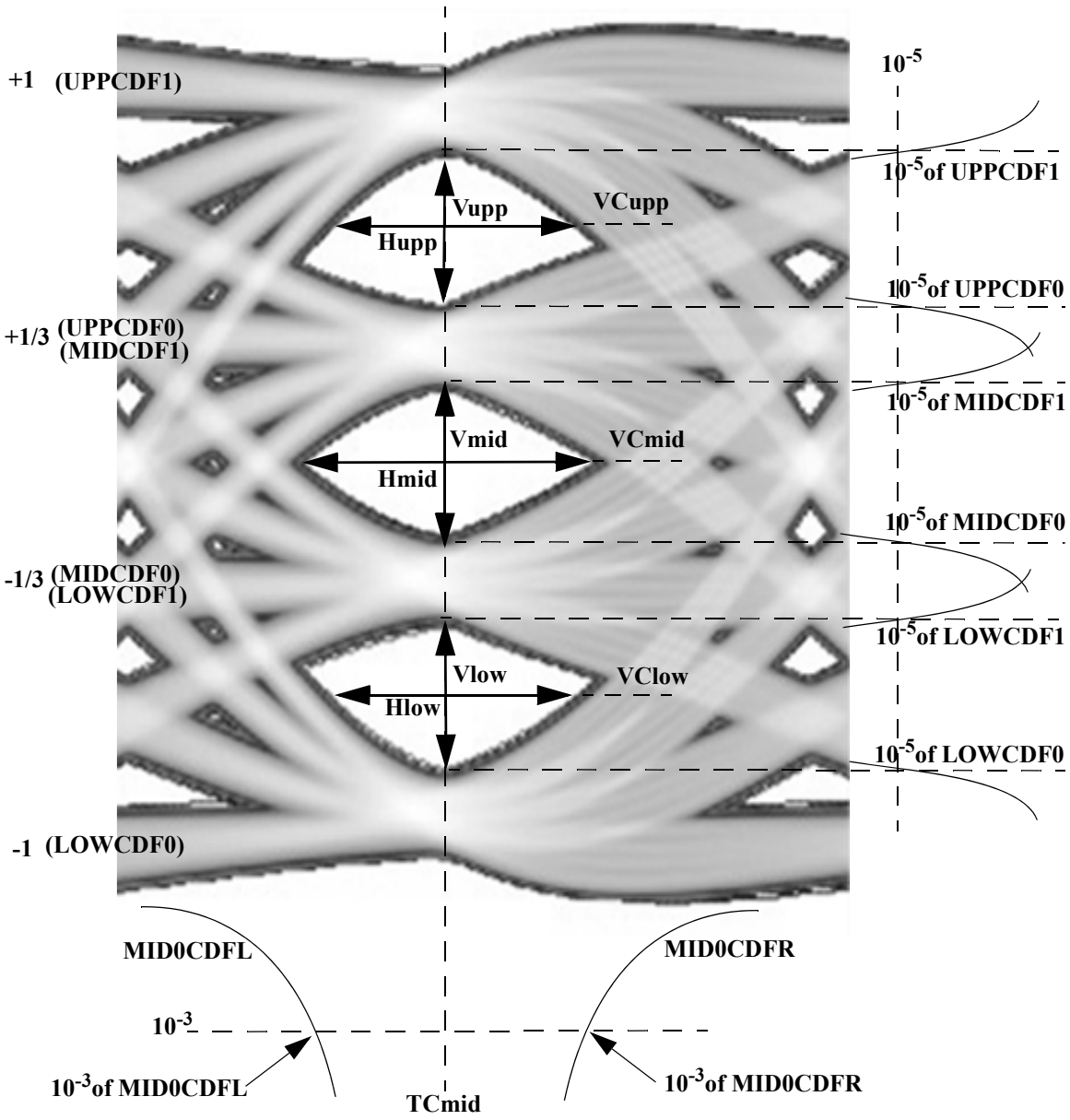

Figure 120E–13—PAM4 eye measurements

8) Use the differential equalized signal from step 2) to construct new CDFs of the signal for both the left edge (MIDCDFL) and right edge (MIDCDFR) of the middle eye at VCmid, as a function of the distance from the center of the eye. Calculate the middle eye width (Hmid) as the difference in time between MIDCDFR and MIDCDFL with a value of 10^{-5}.

9) Using the method in step 8), calculate the 10^{-5} upper eye width (Hupp) sliced at VCupp.

10) Using the method in step 8), calculate the 10^{-5} lower eye width (Hlow) sliced at VClow.

11) The eye width is defined as the minimum of Hmid, Hupp, and Hlow.

12) Check the upper and lower eye alignment to the middle eye. Apply an ESMW wide mask centered on TCmid, as illustrated by Figure 120E–14. The 10^{-5} horizontal openings of the middle eye at VCmid, the upper eye at VCupp, and of the lower eye at VClow all have to extend beyond this mask.

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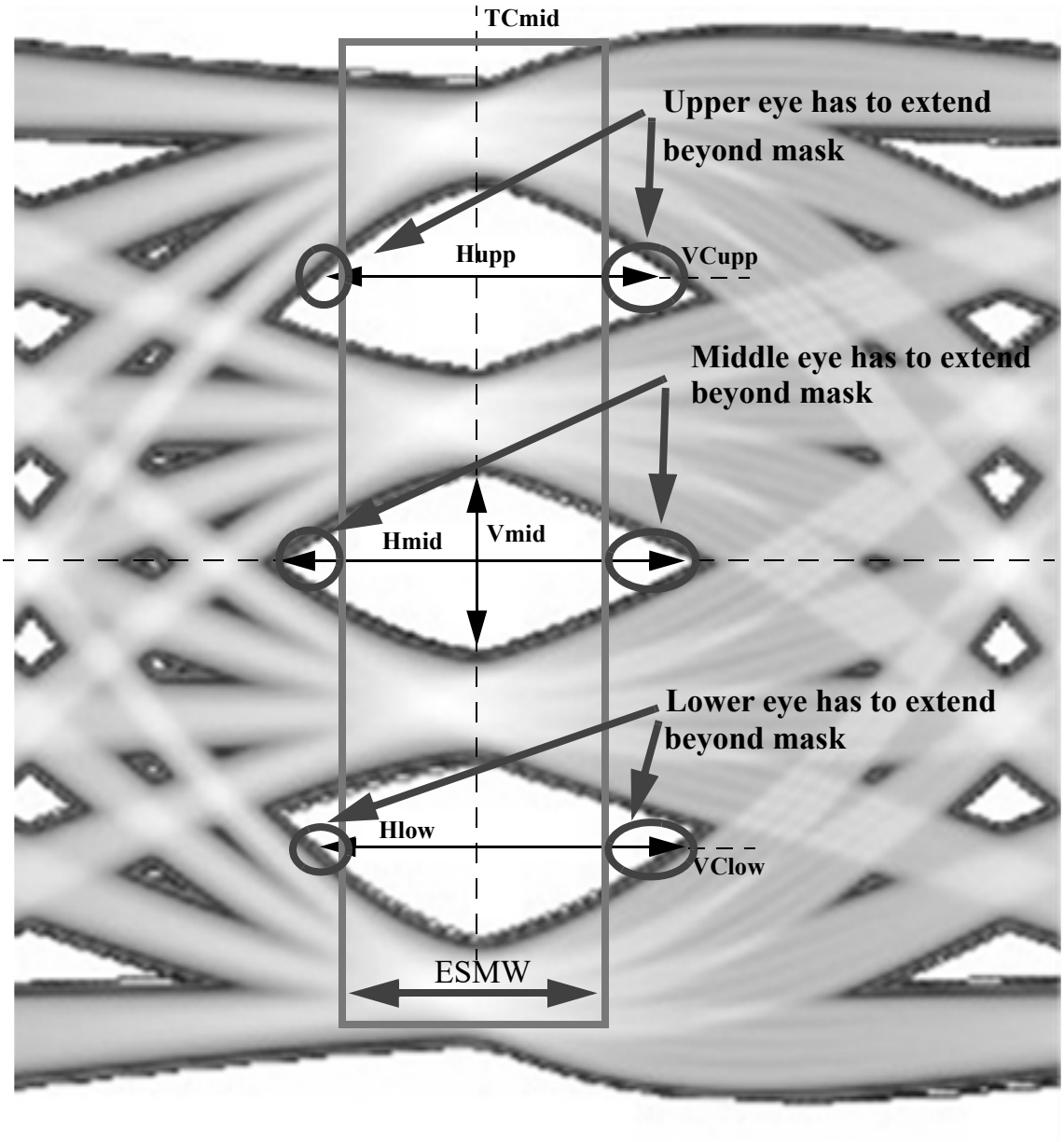

Figure 120E–14—PAM4 upper, middle, and lower eye mask

120E.4.3 Vertical eye closure

Vertical eye closure is defined by Equation (120E–4) for a PRBS13Q differential equalized signal captured and processed according to 120E.4.2.

$$VEC = 20\log_{10}\left(\max\left(\frac{AV_{\text{upp}}}{V_{\text{upp}}}, \frac{AV_{mid}}{V_{\text{mid}}}, \frac{AV_{\text{low}}}{V_{\text{low}}}\right)\right) \text{ (dB)} \quad \text{(120E–4)}$$

where

VEC is the vertical eye closure, in dB

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V_{upp}	is the 10^{-5} upper eye height per 120E.4.2
V_{mid}	is the 10^{-5} middle eye height per 120E.4.2
V_{low}	is the 10^{-5} lower eye height per 120E.4.2
AV_{upp}	is the amplitude of the upper eye (AVupp), equal to VM3–VM2
AV_{mid}	is the amplitude of the middle eye (AVmid), equal to VM2–VM1
AV_{low}	is the amplitude of the lower eye (AVlow), equal to VM1–VM0
VM3	is the mean of the differential equalized signal above VCupp within 0.025 UI of TCmid
VM2	is the mean of the differential equalized signal between VCupp and VCmid within 0.025 UI of TCmid
VM1	is the mean of the differential equalized signal between VCmid and VClow within 0.025 UI of TCmid
VM0	is the mean of the differential equalized signal below VClow within 0.025 UI of TCmid
VCupp	is the voltage center of the upper eye per 120E.4.2
VCmid	is the voltage center of the middle eye per 1120E.4.2
VClow	is the voltage center of the lower eye per 120E.4.2
TCmid	is the time center of the middle eye width per 120E.4.2

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120E.5 Protocol implementation conformance statement (PICS) proforma for Annex 120E, Chip-to-module 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2M) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2M)[309]

120E.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 120E, Chip-to-module 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2M) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2M), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

120E.5.2 Identification

120E.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

120E.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 120E, Chip-to-module 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2M) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2M)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[309] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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120E.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	120E.1	Four independent data paths in each direction for 200GAUI-4 C2M and eight independent data paths in each direction for 400GAUI-8 C2M	M	Yes [ ]
BER	Meets BER requirement	120E.1.1	See 120E.1.1	M	Yes [ ]
ADE	Adaptive Equalizer	120E.3.4	See 120E.3.4	M	Yes [ ]

120E.5.4 PICS proforma tables for Chip-to-module 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2M) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2M)

120E.5.4.1 Host output

Item	Feature	Subclause	Value/Comment	Status	Support
TH1	Signaling rate	120E.3.1.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TH2	DC common-mode output voltage	120E.3.1	Between –0.3 V and 2.8 V with respect to signal ground	M	Yes [ ]
TH3	Peak-to-peak differential output voltage, transmitter disabled	120E.3.1.2	Less than or equal to 35 mV	M	Yes [ ]
TH4	Peak-to-peak differential output voltage	120E.3.1.2	880 mV (max)	M	Yes [ ]
TH5	AC common-mode output voltage	120E.3.1	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TH6	Eye width, all 3 eyes	120E.3.1	0.22 UI	M	Yes [ ]
TH7	Eye height, all 3 eyes	120E.3.1	32 mV	M	Yes [ ]
TH8	Vertical eye closure	120E.3.1	12 dB	M	Yes [ ]
TH9	Differential output return loss	120E.3.1.3	Meets Equation (83E–2) constraints	M	Yes [ ]
TH10	Common to differential mode conversion	120E.3.1.3	Meets Equation (83E–3) constraints	M	Yes [ ]
TH11	Differential termination mismatch	120E.3.1	Less than 10%	M	Yes [ ]
TH12	Transition time	120E.3.1.5	Greater than or equal to 10 ps	M	Yes [ ]
TH13	Reference impedance for output return loss	120E.3.1.3	100 Ω.	M	Yes [ ]
TH14	Crosstalk source	120E.3.1.6	Asynchronous crosstalk source using PRBS13Q or PRBS31Q pattern, or valid 200GBASE-R/400GBASE-R signal	M	Yes [ ]

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120E.5.4.2 Module output

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Signal rate	120E.3.1.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TM2	AC common-mode output voltage	120E.3.1	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TM3	Peak-to-peak differential output voltage	120E.3.1.2	900 mV (max)	M	Yes [ ]
TM4	Near-end eye width, all 3 eyes	120E.3.2.1	0.265 UI	M	Yes [ ]
TM5	Near-end eye height, all 3 eyes	120E.3.2.1	70 mV	M	Yes [ ]
TM6	Far-end eye width, all 3 eyes	120E.3.2.1	0.2 UI	M	Yes [ ]
TM7	Far-end eye height, all 3 eyes	120E.3.2.1	30 mV	M	Yes [ ]
TM8	Far-end pre-cursor ISI ratio	120E.3.2.1.2	–4.5% to +2.5%	M	Yes [ ]
TM9	Differential output return loss	120E.3.1.3	Meets Equation (83E–2) constraints	M	Yes [ ]
TM10	Common to differential mode conversion	120E.3.1.3	Meets Equation (83E–3) constraints	M	Yes [ ]
TM11	Differential termination mismatch	120E.3.1	Less than 10%	M	Yes [ ]
TM12	Transition time	120E.3.1.5	Greater than or equal to 9.5 ps	M	Yes [ ]
TM13	Reference impedance for output return loss	120E.3.1.3	100 Ω.	M	Yes [ ]
TM14	Crosstalk source	120E.3.2.1	Asynchronous crosstalk source using PRBS13Q or PRBS31Q pattern, or valid 200GBASE-R/400GBASE-R signal	M	Yes [ ]

120E.5.4.3 Host input

Item	Feature	Subclause	Value/Comment	Status	Support
RH1	Host input characteristics	120E.3.3	Table 120E–4	M	Yes [ ]

120E.5.4.4 Module input

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Module input characteristics	120E.3.4	Table 120E–7	M	Yes [ ]

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Annex 127A

(informative)

Compatibility of 2.5GBASE-X PCS/PMA with 1000BASE-X PCS/PMA running 2.5 times faster

This annex discusses the restrictions when operating 2.5GBASE-X PCS/PMA with a 1000BASE-X PCS/PMA link partner running 2.5 times faster. Compatibility of the PMD is outside the scope of this annex. In this annex when 1000BASE-X PCS/PMA is referred to, the 2.5 times speed up is implied.

The 2.5GBASE-X PCS/PMA is specified to be compatible with a link partner running 1000BASE-X PCS/PMA running 2.5 times faster as shown in Figure 127A–1 with some restrictions.

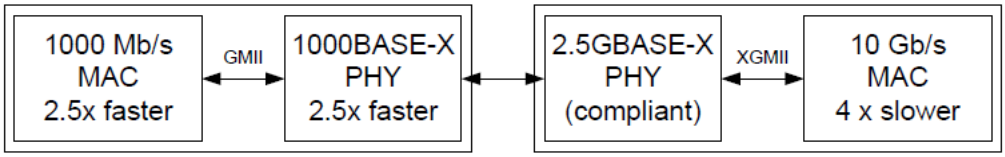

Figure 127A–1—2.5X speed 1000BASE-X to 2.5GBASE-X Link

2.5GBASE-X is defined to operate only in full duplex. Hence the 1000BASE-X PCS can only operate in full duplex. If the half duplex carrier extend or carrier extend with errors is sent by the 1000BASE-X PCS, the 2.5GBASE-X PCS will convert it to receive errors. A /T/R/ or a /T/R/R/ at the end of packet are correctly converted as idles.

The 2.5GBASE-X PCS does not support Clause 37 Auto-Negotiation. Hence, the 1000BASE-X PCS is expected to have its Clause 37 Auto-Negotiation functionality disabled so that the /C/ ordered set will not be transmitted. If a 2.5GBASE-X PCS receives /C/ ordered set, then undefined behavior may occur.

Since the 2.5GBASE-X PCS is attached to an RS that can send out sequence ordered set (/Q/), a compliant 1000BASE-X PCS will interpret each /Q/ ordered set as four /I/ ordered sets. Unlike /I/, /LI/, and /C/ ordered sets, there is no concept of correcting vs preserving the running disparity when /Q/ ordered sets are generated.

Unlike the GMII, there is no false carrier defined in the XGMII. The 2.5GBASE-X PCS Receive process can detect false carriers, but these will be converted to receive errors by the PCS Word Decode process.

It is permissible for a compliant 1000BASE-X PCS transmit process to truncate the first byte of a preamble in order to align the start of packet on the EVEN boundary. The implication of this is the 2.5 Gb/s RS (see 46.3.3.3) has to be able to accept a seven byte preamble on the XGMII with the SFD positioned on lane 2.

Since the start of packet has to align to lane 0 of the XGMII the 2.5 Gb/s RS may delete idle bytes in order to do the alignment. The 1G RS running 2.5 times faster has to be able to handle IPG shrinkage.

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Annex 128A

(normative)

2.5 Gb/s Storage Enclosure Interface (2.5GSEI)

128A.1 Overview

This clause defines the functional and electrical characteristics for 2.5GSEI. This interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable storage drive module interfaces. The compliance point definitions provide a unique partitioning of the channel defined in Annex 69B, such that the test points $TP0_{D\text{-}H}$ and $TP0_{H\text{-}D}$ defined in this annex are equivalent to TP1, and $TP5_{D\text{-}H}$ and $TP5_{H\text{-}D}$ are equivalent to TP4. Figure 128A–1 shows the test point locations associated with 2.5GSEI.

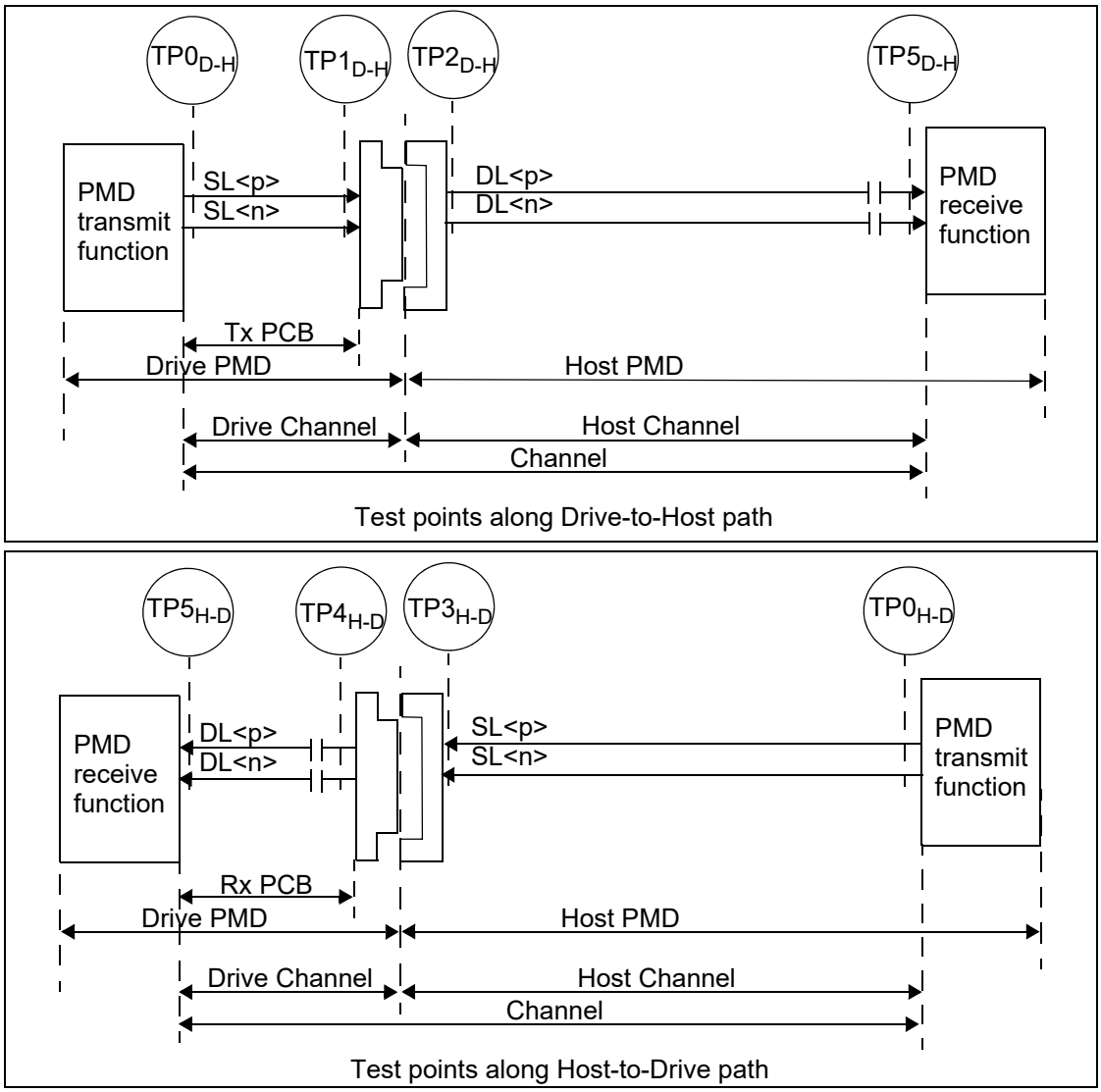

Figure 128A–1—Test points

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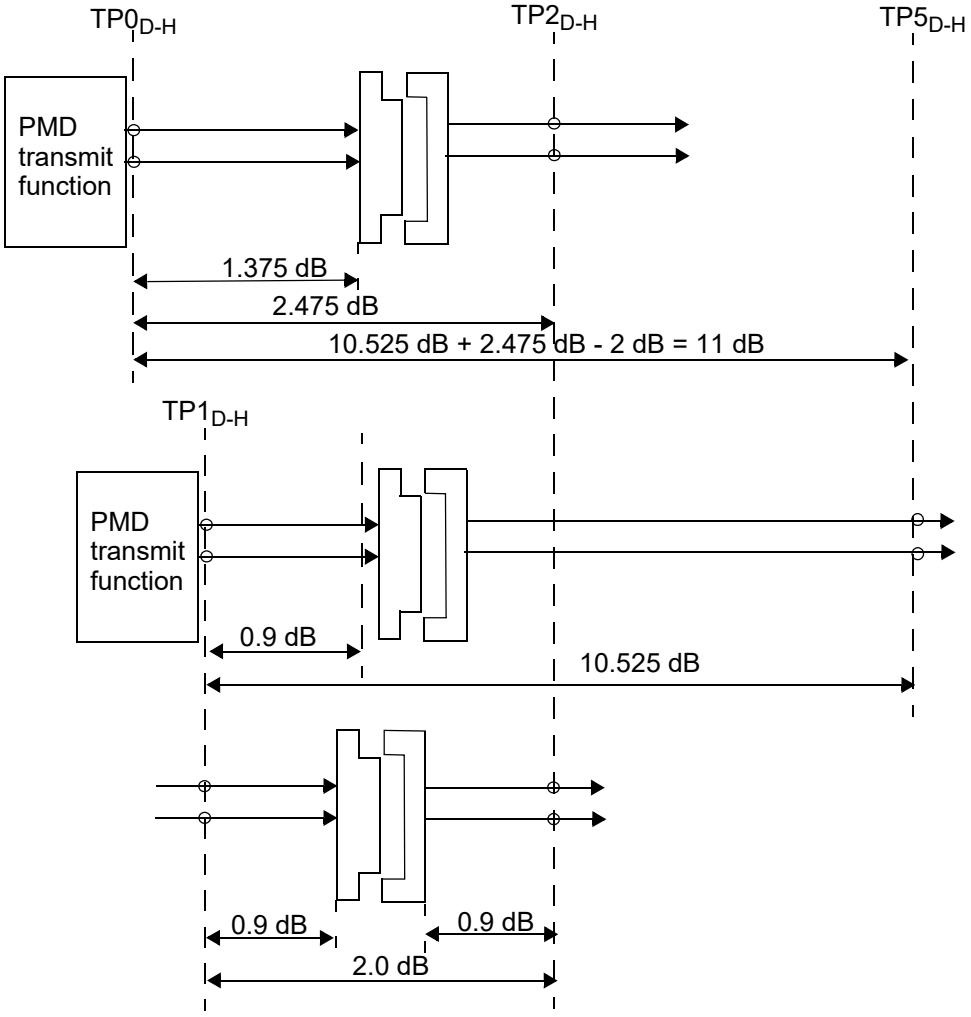
The 2.5GSEI link is described in terms of a host 2.5GSEI component with associated insertion loss and a drive 2.5GSEI component. Figure 128A–2 (one direction shown) depicts the recommended differential insertion loss budget at 1.5625 GHz for a typical 2.5GSEI application. The recommended maximum differential insertion loss from TP0 to TP5 is given in Equation (128A–1) and depicted in Figure 128A–3. The 2.5GSEI interface consists of independent data paths in each direction. Each data path contains one differential lane, which is AC-coupled on the receiver side. The nominal signaling rate for each lane is 3.125 GBd.



NOTE—The connector insertion loss is 0.2 dB for the mated test fixture.

Figure 128A–2—Insertion loss budget at 1.5625 GHz

$$Insertion\_loss(f) \le \begin{cases} 0.668 + 3.755\sqrt{f} + 3.608f & 0.05 \le f < 1.5625 \\ -23.753 + 22.242f & 1.5625 \le f < 2.34375 \end{cases} \text{ (dB)} \qquad (128A–1)$$

where

f is the frequency in GHz

Insertion_loss(f) is chip to chip (C2C) insertion loss

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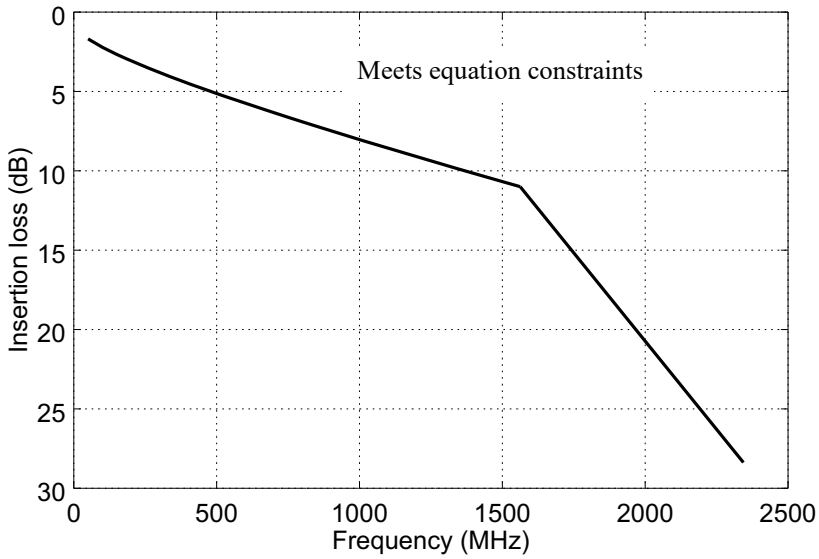

Figure 128A–3—Illustration of recommended maximum differential insertion loss from TP0 to TP5

128A.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 10^{-12} with any errors sufficiently uncorrelated to ensure an acceptably high mean time to false packet acceptance (MTTFPA) assuming 8B/10B coding.

128A.2 2.5GSEI compliance point definitions

The electrical characteristics for 2.5GSEI are defined at compliance points for the host and drive, respectively. Reference test fixtures, called compliance boards, are used to access the electrical specification parameters. Figure 128A–4 depicts the location of compliance points when measuring host 2.5GSEI compliance. The output of the Host Compliance Board (HCB) is used to verify the host electrical output signal at $TP4_{H\text{-}D}$ (see Figure 128A–1). Similarly, the input of the HCB at $TP1_{D\text{-}H}$ (see Figure 128A–2) is used to verify the host input compliance.

Figure 128A–5 depicts the location of compliance points when measuring drive 2.5GSEI compliance. The output of the Drive Compliance Board (DCB) is used to verify the Drive electrical output signal at $TP2_{D\text{-}H}$ (see Figure 128A–5). Similarly, the input of the DCB at $TP3_{H\text{-}D}$ (see Figure 128A–5) is used to verify the Drive input compliance. Additional details on the requirements for the HCB and DCB are given in Annex 128B.

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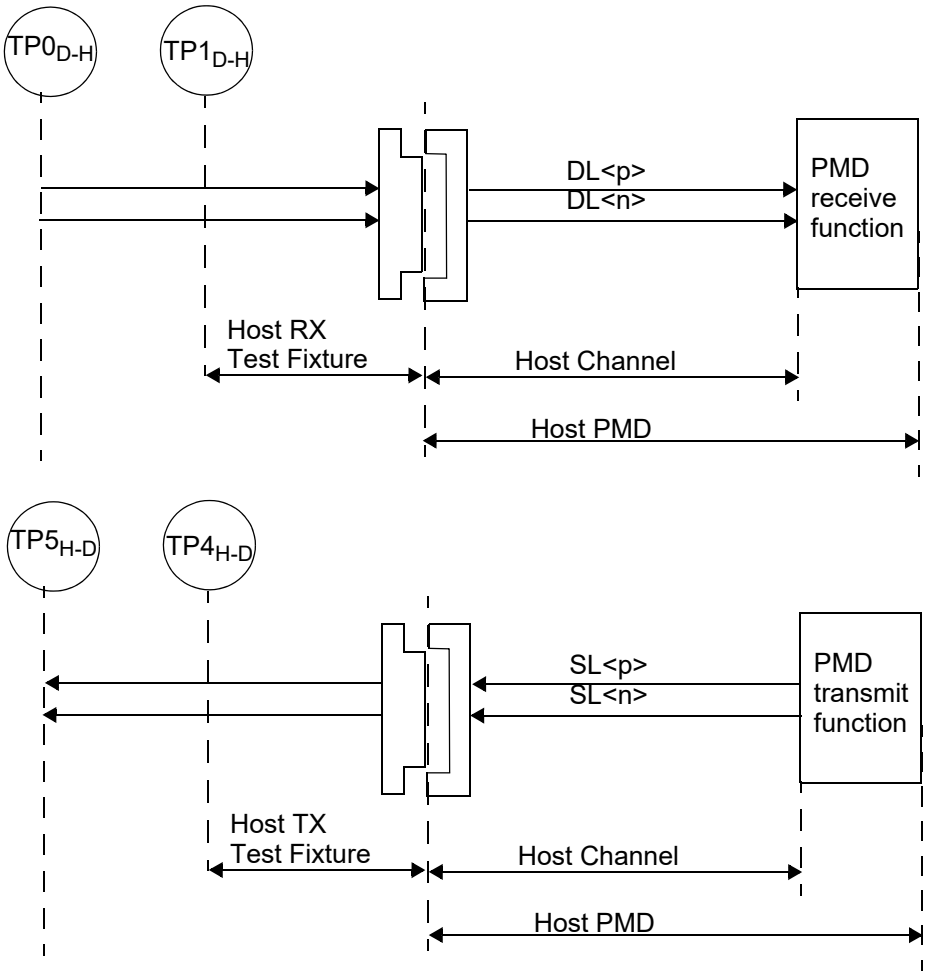

Figure 128A–4—Host compliance board

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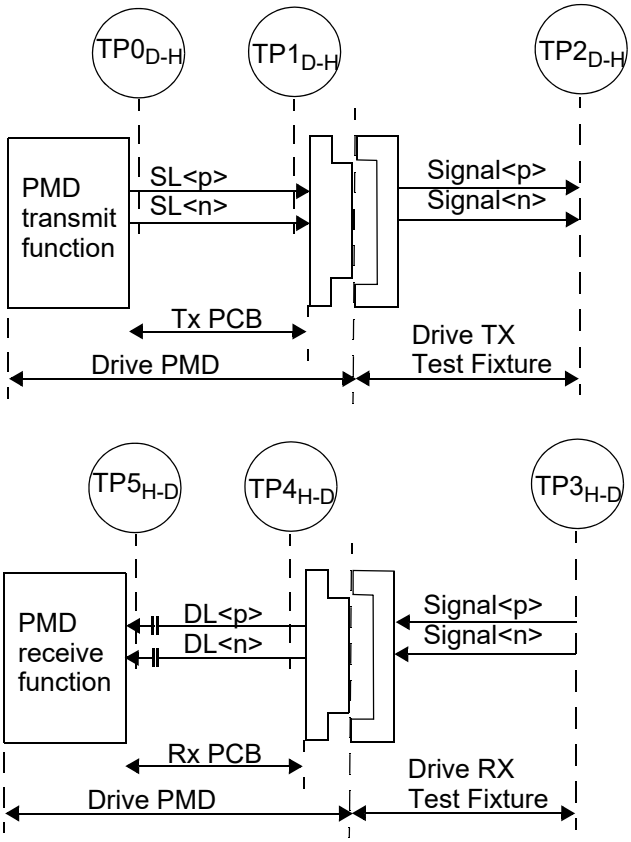

Figure 128A–5—Drive compliance board

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128A.3 2.5GSEI electrical characteristics

128A.3.1 2.5GSEI host output characteristics

A 2.5GSEI host output shall meet the specifications defined in Table 128A–1 if measured at $TP4_{H\text{-}D}$ (see Figure 128A–4).

Table 128A–1—2.5GSEI host output characteristics

Parameter	Subclause reference	Value	Units
Signaling rate	128A.3.1.1	3.125 ± 100 ppm	GBd
Nominal unit interval	128A.3.1.1	320	ps
DC common-mode output voltage (max)	128A.3.1.2	1.9	V
AC common-mode output voltage (max, RMS)	128A.3.1.2	30	mV
Peak-to-peak differential output voltage (min) transmitter enabled	128.7.1.4	580	mV
Peak-to-peak differential output voltage (max) transmitter enabled	128.7.1.4	1200	mV
Peak-to-peak differential output voltage (max) transmitter disabled	128.7.1.4	35	mV
Maximum transition time (20%–80%)	128.7.1.7	460	ps
Differential output return loss (min)	128A.3.1.3	See Equation (128A–2)	dB
Max output jitter (peak-to-peak) Random jitter Deterministic jitter Duty Cycle Distortion[1] Total jitter	128A.3.1.5	 0.2 0.12 0.035 0.32	 UI UI UI UI
Signal-to-noise-and-distortion ratio (min) (SNDR)	128A.3.1.6	25	dB

[1]Duty Cycle Distortion is considered part of deterministic jitter distribution.

A test system, as depicted in Figure 128B–1, with a fourth-order Bessel-Thomson low-pass response with 8 GHz 3 dB bandwidth, is to be used for all output signal measurements, unless otherwise specified.

128A.3.1.1 Signaling rate and range

The 2.5GSEI signaling rate is specified in Table 128A–1. The nominal unit interval is the inverse of the signaling rate.

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128A.3.1.2 Signaling levels

The differential output voltage V_d is defined to be the difference between the single-ended output voltages, *SL*<*p*> minus *SL*<*n*>. The common-mode voltage V_{cm} is defined to be one half of the sum of *SL*<*p*> and *SL*<*n*>. These definitions are illustrated by Figure 128A–6.

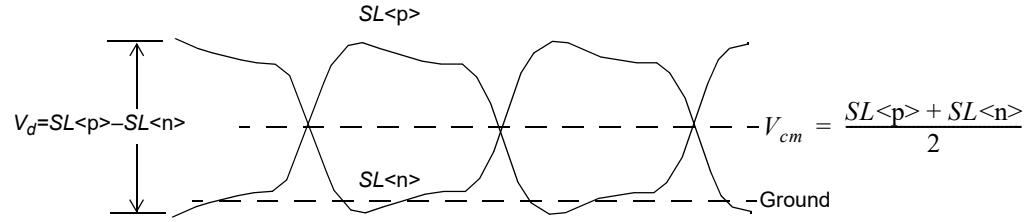

Figure 128A–6—Voltage definitions

The DC common-mode output voltage and AC common-mode output voltage are defined with respect to signal ground.

128A.3.1.3 Output return loss

The differential output return loss, in dB, of the output is shown in Equation (128A–2) and illustrated in Figure 128A–7. This output requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 Ω.

$$Return\_loss(f) \geq \begin{cases} Return\_loss_{min} = 12 & 50 \leq f < 275 \\ Return\_loss_{min} = 12 - 6.75\log_{10}\left(\frac{f}{275\text{MHz}}\right) & 275 \leq f < 2343.75 \end{cases} \text{(dB)} \qquad \text{(128A–2)}$$

where

f is the frequency in MHz

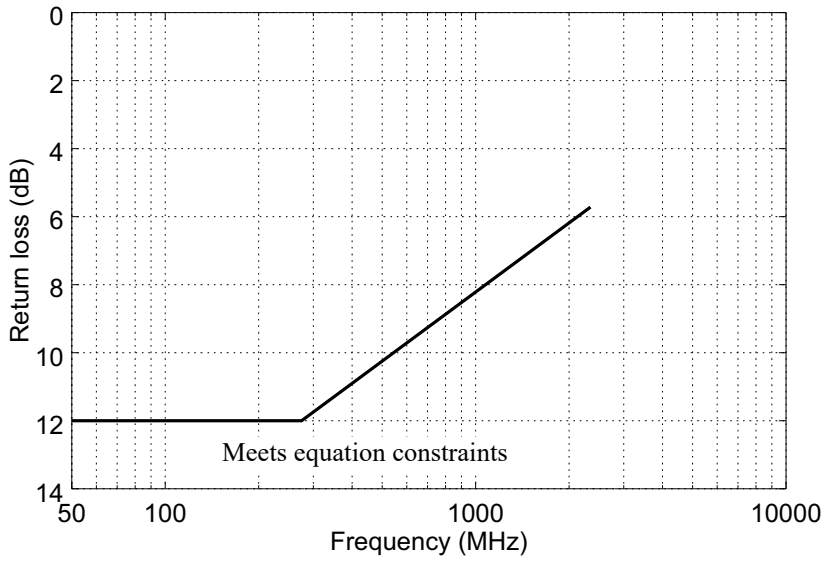

Figure 128A–7—Differential return loss limit

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128A.3.1.4 Transmit jitter test requirements

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in 48B.3. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements shall be the test pattern defined in 48A.2. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal.

128A.3.1.5 Transmit jitter

The transmitter shall have a maximum total jitter, composed of a maximum deterministic component and a maximum random component as shown in Table 128A–1. Duty cycle distortion (DCD) is considered a component of deterministic jitter and shall not exceed the value shown in Table 128A–1. The peak-to-peak duty cycle distortion is defined as the absolute value of the difference in the mean pulse width of a 1 pulse or the mean pulse width of a 0 pulse (as measured at the mean of the high- and low-voltage levels in a clock like repeating bit sequence) and the nominal pulse width. Jitter specifications are specified for BER = 10^{-12}. Transmit jitter test requirements are specified in 128A.3.1.4.

128A.3.1.6 Transmitter output noise and distortion

Signal-to-noise-and-distortion ratio (SNDR) is measured at the transmitter output using the following method:

a) Capture at least one complete cycle of the test pattern PRBS9 as specified in Table 68–6 at $TP4_{H\_D}$ (see Figure 128A–4) per 85.8.3.3.4.
b) Apply the reference equalizer from 93A.1.4.3, using the values from Table 128A–2.
c) Compute the linear fit pulse response $p(k)$ and the linear fit error waveform $e(k)$ from the resulting waveform per 85.8.3.3.5 using N_p=3 and D_p = 1. Denote the standard deviation of $e(k)$ as σ_e.
d) Measure the RMS deviation from the mean voltage at a fixed point in a run of at least 8 consecutive identical bits in a suitable pattern. PRBS9 is an example of a pattern that includes runs suitable to perform the measurement. It is recommended that the deviation is measured within the flattest portion of the waveform at a point where the slope is closest to zero. The RMS deviation is measured for a run of zeros and also a run of ones. The average of the two measurements is denoted as σ_n.

Table 128A–2—2.5G host receiver equalizer parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	3.125 ± 100 ppm	GBd
Continuous time filter, DC gain [1] Minimum value Maximum value Step size	g_{DC}	 –9.5 0 0.5	 dB dB dB
Continuous time filter, zero frequency	f_z	$f_b/2$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b/2$ f_b	GHz GHz

[1]The DC gain, gDC, is optimized to satisfy the SNDR requirement.

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SNDR is defined by Equation (128A–3).

$$SNDR = 10\log_{10}\left(\frac{p_{max}^{2}}{\sigma_e^{2} + \sigma_n^{2}}\right)\text{dB} \quad (128A–3)$$

where

$p_{\max}$ is the maximum value of $p(k)$

128A.3.2 2.5GSEI host input characteristics

A 2.5GSEI host input shall meet the specifications defined in Table 128A–3 if measured at the appropriate test point.

Table 128A–3—2.5GSEI host input characteristics

Parameter	Subclause reference	Value	Units
Differential input return loss (min)	128A.3.2.1	See Equation (128A–2)	dB
Interference tolerance	128A.3.2.2	—	—
Jitter tolerance	128A.3.2.3	—	—

128A.3.2.1 Input differential return loss

The host input differential return loss shall meet Equation (128A–2) measured at $TP1_{D\text{-}H}$ (see Figure 128A–4).

128A.3.2.2 Receiver interference tolerance

The following considerations apply to the interference tolerance test. The pattern generator is calibrated at $TP2_{D\text{-}H}$ (see Figure 128A–8) to produce the values in the calibration procedure shown below. The channel noise source is a broadband noise generator capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from f_1 in Table 69B–2 to 0.5 times the signaling speed for the port type under test with a crest factor of no less than 5. The noise shall be measured at the output of a filter connected to the output of the noise source. The filter for this measurement shall have no more than a 40 dB per decade roll-off and a 3 dB cut-off frequency shall be equal to 0.5 times the signaling speed. Figure 128A–8 illustrates the calibration and test configurations that are needed for the host interference tolerance test. The data pattern used for the receiver interference tolerance test shall be the test pattern defined in 48A.5. The BER shall be less than or equal to 10^{-12} for any signaling speed in the range of 3.125 GBd ± 100 ppm.

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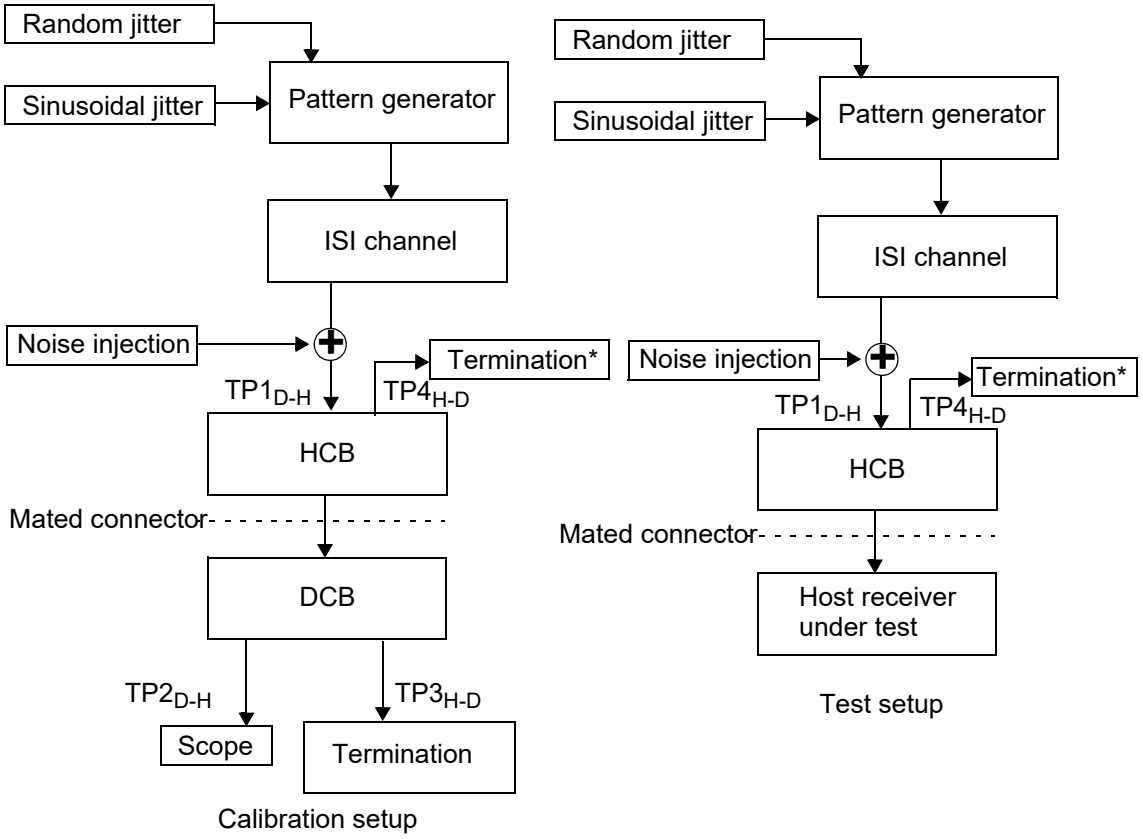
Calibration procedure is as follows:

a) Create a channel (ISI channel + HCB + DCB) with as close to 5 dB of loss at 1.5625 GHz as possible.
b) Measure signal through the ISI channel at $TP2_{D\text{-}H}$ (see Figure 128A–8).
c) Adjust the ISI channel to the limit of the maximum transition time in Table 128A–1.
d) Adjust the amplitude to meet the peak-to-peak differential output voltage in Table 128A–1.
e) Adjust noise to meet the required SNDR in Table 128A–1.
f) Adjust pattern generator random jitter to the required value in Table 128A–1.



* The single-ended transmit signals are terminated in 50 Ω to provide a 100 Ω differential termination.

Figure 128A–8—Host interference calibration and test setup

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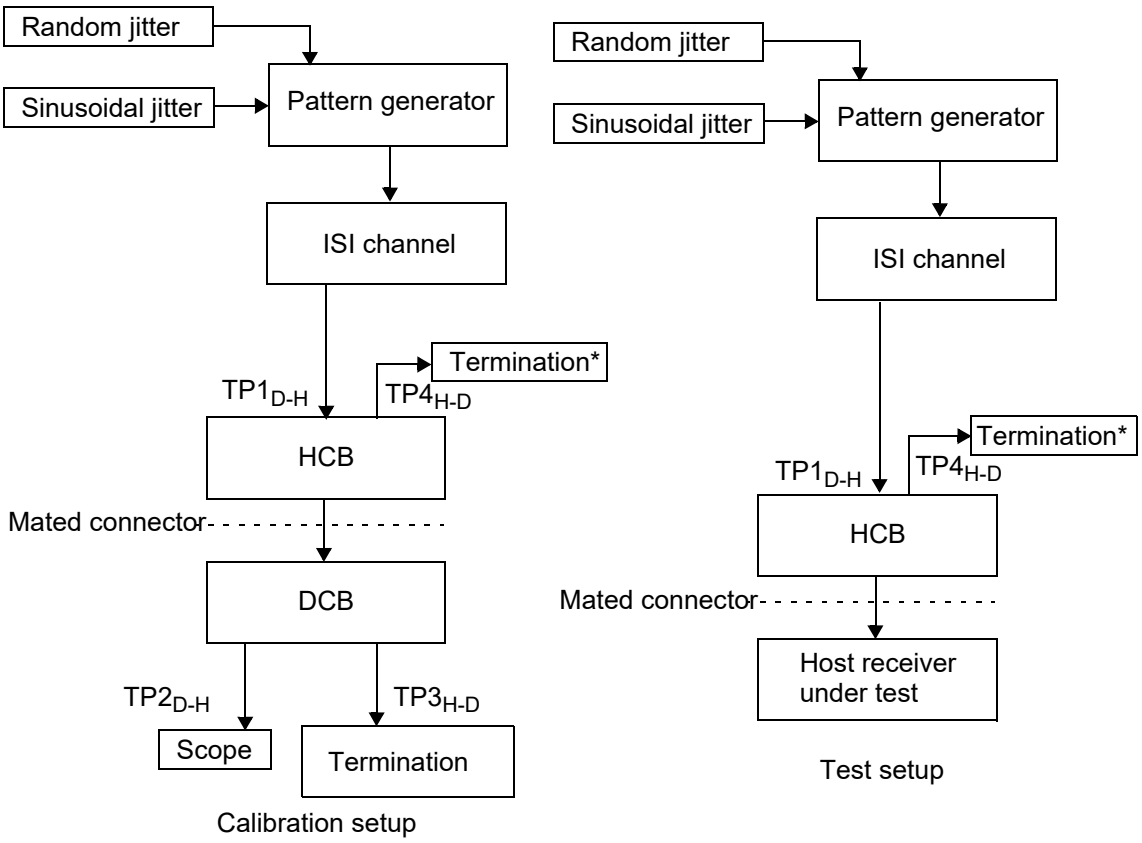
128A.3.2.3 Receiver jitter tolerance

The following considerations apply to the jitter tolerance test. The transmitter is calibrated at $TP2_{D\text{-}H}$ (see Figure 128A–9) to produce the values in the calibration procedure shown below. Broadband noise is not injected during this test except for what is inherently present in the host. Figure 128A–9 illustrates the calibration and test configurations that are needed for the host jitter tolerance test. The data pattern used for the receiver jitter tolerance test shall be the test pattern defined in 48A.5. The BER shall be less than or equal to 10^{-12} for any signaling speed in the range of 3.125 GBd ± 100 ppm.

Calibration procedure is as follows:

a) Create a channel (ISI channel + HCB + DCB) with as close to 5 dB of loss at 1.5625 GHz as possible.
b) Measure signal through the ISI channel at $TP2_{D\text{-}H}$ (see Figure 128A–9).
c) Adjust the ISI channel to the limit of the maximum transition time in Table 128A–1.
d) Adjust the amplitude to meet the Peak-to-peak differential output voltage (min) transmitter enabled in Table 128A–1.
e) Adjust pattern generator random jitter to the required value in Table 128A–1.
f) Adjust sinusoidal jitter until the values in Table 128A–6 are met.



* The single-ended transmit signals are terminated in 50 Ω to provide a 100 Ω differential termination.

Figure 128A–9—Host jitter tolerance calibration and test setup

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128A.3.3 2.5GSEI drive output characteristics

A 2.5GSEI drive output shall meet the specifications defined in Table 128A–4 if measured at $TP2_{D\text{-}H}$ (see Figure 128A–5).

Table 128A–4—2.5GSEI drive output characteristics

Parameter	Subclause reference	Value	Units
Signaling rate	128A.3.1.1	3.125 ± 100 ppm	GBd
Nominal unit interval	128A.3.1.1	320	ps
DC common-mode output voltage (max)	128A.3.1.2	1.9	V
AC common-mode output voltage (max, RMS)	128A.3.1.2	30	mV
Peak-to-peak differential output voltage (min) transmitter enabled	128.7.1.4	800	mV
Peak-to-peak differential output voltage (max) transmitter enabled	128.7.1.4	1200	mV
Peak-to-peak differential output voltage (max) transmitter disabled	128.7.1.4	35	mV
Maximum transition time (20%-80%)	128.7.1.7	229	ps
Differential output return loss (min)	128A.3.1.3	See Equation (128A–2)	dB
Max output jitter (peak-to-peak) Random jitter Deterministic jitter Duty Cycle Distortion[1] Total jitter	 128A.3.1.5 128A.3.1.5 128A.3.1.5 128A.3.1.5	 0.2 0.12 0.035 0.32	 UI UI UI UI
Signal-to-noise-and-distortion ratio (min) - SNDR	128A.3.1.6	25	dB

[1]Duty Cycle Distortion is considered part of deterministic jitter distribution.

A test system with a fourth-order Bessel-Thomson low-pass response with 8 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

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128A.3.4 2.5GSEI drive input characteristics

A 2.5GSEI drive input shall meet the specifications defined in Table 128A–5 if measured at the appropriate test point.

Table 128A–5—2.5GSEI drive input characteristics

Parameter	Subclause reference	Value	Units
Differential input return loss (min)	128A.3.4.1	See Equation (128A–2)	dB
Interference tolerance	128A.3.4.2	—	—
Jitter tolerance	128A.3.4.3	—	—

128A.3.4.1 Input differential return loss

The drive input differential return loss shall meet Equation (128A–2) measured at $TP3_{H\text{-}D}$ (see Figure 128A–5).

128A.3.4.2 Receiver interference tolerance

The following considerations apply to the interference tolerance test. The pattern generator is calibrated at $TP4_{H\text{-}D}$ (see Figure 128A–10) to produce the values in the calibration procedure shown below. The channel noise source is a broadband noise generator capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from f_1 in Table 69B–2 to 0.5 times the signaling speed for the port type under test with a crest factor of no less than 5. The noise shall be measured at the output of a filter connected to the output of the noise source. The filter for this measurement shall have no more than a 40 dB per decade roll-off and a 3 dB cut-off frequency shall be equal to 0.5 times the signaling speed. Figure 128A–10 illustrates the calibration and test configurations that are needed for the drive interference tolerance test. The data pattern used for the receiver interference tolerance test shall be the test pattern defined in 48A.5. The BER shall be less than or equal to 10^{-12} for any signaling speed in the range of 3.125 GBd ± 100 ppm.

Calibration procedure is as follows:

a) Create a channel (ISI channel + HCB + DCB) with as close to 13.5 dB of loss at 1.5625 GHz as possible.
b) Measure signal through the ISI channel at $TP2_{H\text{-}D}$ (see Figure 128A–10).
c) Adjust the ISI channel to the limit of the maximum transition time in Table 128A–4.
d) Adjust the amplitude to meet the peak-to-peak differential output voltage in Table 128A–4.
e) Adjust noise to meet the required SNDR (see 128A.3.1.6).
f) Adjust pattern generator random jitter to the required value in Table 128A–4.

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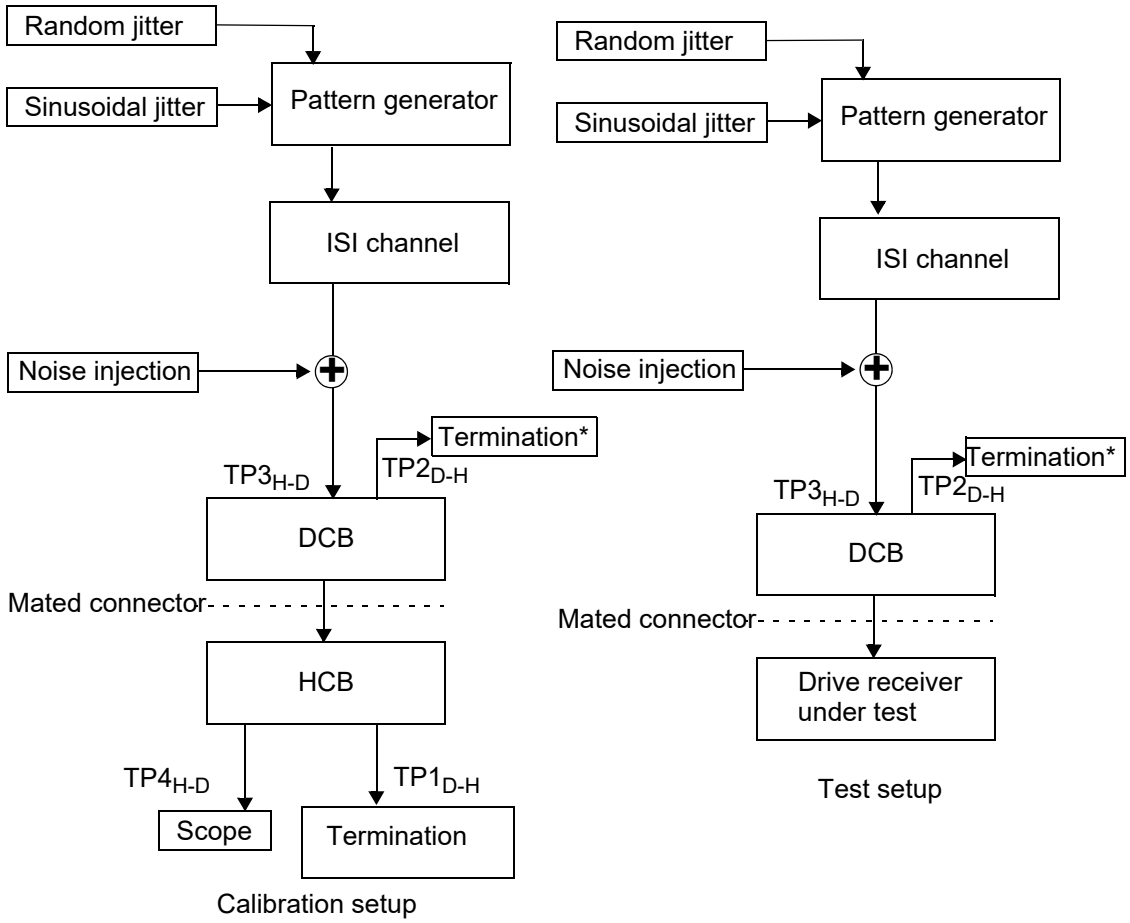

* The single-ended transmit signals are terminated in 50 Ω to provide a 100 Ω differential termination.

Figure 128A–10—Drive interference calibration and test setup

128A.3.4.3 Receiver jitter tolerance

The following considerations apply to the jitter tolerance test. The transmitter is calibrated at $TP4_{H\text{-}D}$ (see Figure 128A–11) to produce the values in the calibration procedure shown below. Broadband noise is not injected during this test except for what is inherently present in the drive. Figure 128A–11 illustrates the calibration and test configurations that are needed for the drive jitter tolerance test. The data pattern used for the receiver jitter tolerance test shall be the test pattern defined in 48A.5. The BER shall be less than or equal to 10^{-12} for any signaling speed in the range of 3.125 GBd ± 100 ppm.

Calibration procedure is as follows:

a) Create a channel (ISI channel + HCB + DCB) with as close to 13.5 dB of loss at 1.5625 GHz as possible.
b) Measure signal through the ISI channel at $TP4_{H\text{-}D}$ (see Figure 128A–11).
c) Adjust the ISI channel to the limit of the maximum transition time in Table 128A–4.
d) Adjust the amplitude to meet the Peak-to-peak differential output voltage (min) transmitter enabled in Table 128A–4.
e) Adjust pattern generator random jitter to the required value in Table 128A–4.
f) Adjust sinusoidal jitter until the values in Table 128A–6 are met.

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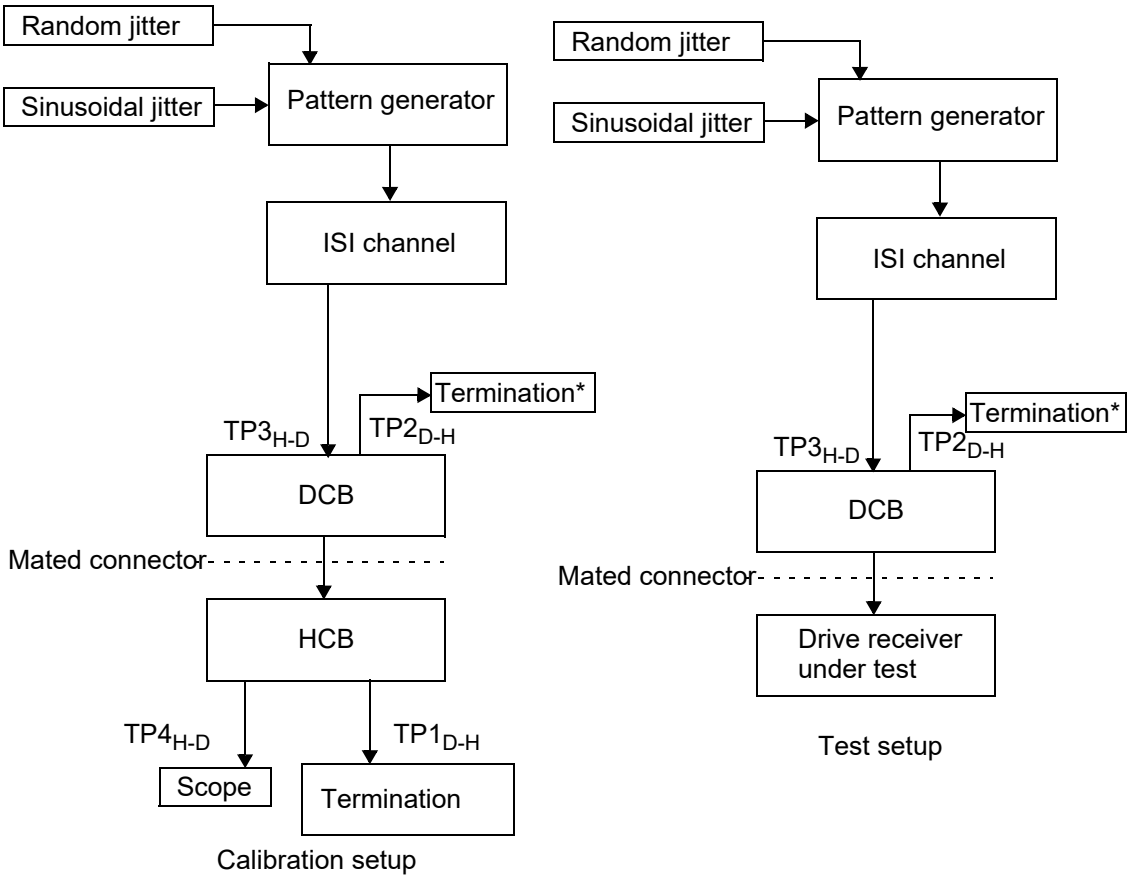

* The single-ended transmit signals are terminated in 50 Ω to provide a 100 Ω differential termination.

Figure 128A–11—Drive receiver jitter tolerance test setup

Table 128A–6—Applied peak-to-peak sinusoidal jitter

Parameter	Case 1	Case 2	Case 3	Units
Jitter frequency	0.02	1.875	20	MHz
Peak-to-peak jitter amplitude	5	0.15	0.15	UI

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128A.4 Protocol implementation conformance statement (PICS) proforma for Annex 128A, 2.5 Gb/s Storage Enclosure Interface (2.5GSEI)[310]

128A.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 128A, 2.5 Gb/s Storage Enclosure Interface (2.5GSEI), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

128A.4.2 Identification

128A.4.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

128A.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 128A, 2.5 Gb/s Storage Enclosure Interface (2.5GSEI)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

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128A.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
2.5GSEI	2.5GSEI Storage Enclosure Interface	128A		O	Yes [ ] No [ ]

128A.4.4 PICS proforma tables for 2.5 Gb/s Storage Enclosure Interface (2.5GSEI)

Item	Feature	Subclause	Value/Comment	Status	Support
OV1	Bit Error Ratio	128A.1.1	BER < 10^{-12}	M	Yes [ ]

128A.4.4.1 Host output functions

Item	Feature	Subclause	Value/Comment	Status	Support
HO1	2.5GSEI host output characteristics	128A.3.1	Table 128A–1, measured at $TP4_{H\text{-}D}$ (see Figure 128A–11)	M	Yes [ ]
HO2	Tx jitter test waveform	128A.3.1.4	Square wave defined in 52.9.1.2	M	Yes [ ]
HO3	Transmit jitter requirements	128A.3.1.5	Table 128A–1	M	Yes [ ]
HO4	Tx DCD limit	128A.3.1.5	Table 128A–1	M	Yes [ ]
HO5	Tx SNDR limit	128A.3.1.6	Table 128A–1	M	Yes [ ]

128A.4.4.2 Host input functions

Item	Feature	Subclause	Value/Comment	Status	Support
HI1	2.5GSEI host input characteristics	128A.3.2	Table 128A–3, measured at $TP1_{D\text{-}H}$	M	Yes [ ]
HI2	Input differential return loss	128A.3.2.1	Shall meet Equation (128A–2) at $TP1_{D\text{-}H}$	M	Yes [ ]
HI3	Receiver interference tolerance test pattern	128A.3.2.2	Test pattern defined in 48A.5	M	Yes [ ]
HI4	Receiver interference tolerance BER	128A.3.2.2		M	Yes [ ]
HI5	Receiver jitter tolerance test pattern	128A.3.2.3	Test pattern defined in 48A.5	M	Yes [ ]
HI6	Receiver jitter tolerance BER	128A.3.2.3		M	Yes [ ]

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128A.4.4.3 Drive output functions

Item	Feature	Subclause	Value/Comment	Status	Support
DO1	2.5GSEI drive output characteristics	128A.3.3	Table 128A–4, measured at $TP2_{D\text{-}H}$	M	Yes [ ]

128A.4.4.4 Drive input functions

Item	Feature	Subclause	Value/Comment	Status	Support
DI1	2.5GSEI drive input characteristics	128A.3.4	Table 128A–5, measured at $TP3_{H\text{-}D}$	M	Yes [ ]
DI2	Input differential return loss	128A.3.4.1	Shall meet Equation (128A–2) at $TP3_{H\text{-}D}$	M	Yes [ ]
DI3	Receiver interference tolerance test pattern	128A.3.4.2	Test pattern defined in 48A.5	M	Yes [ ]
DI4	Receiver interference tolerance BER	128A.3.4.2		M	Yes [ ]
DI5	Receiver jitter tolerance test pattern	128A.3.4.3	Test pattern defined in 48A.5	M	Yes [ ]
DI6	Receiver jitter tolerance BER	128A.3.4.3		M	Yes [ ]

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Annex 128B

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Test fixtures for 2.5 Gb/s and 5 Gb/s Storage Enclosure Interfaces

Transmitter and receiver measurements are made utilizing the test fixtures specified in Figure 128B–1. The requirements in this clause are not MDI connector specifications for an implemented design.

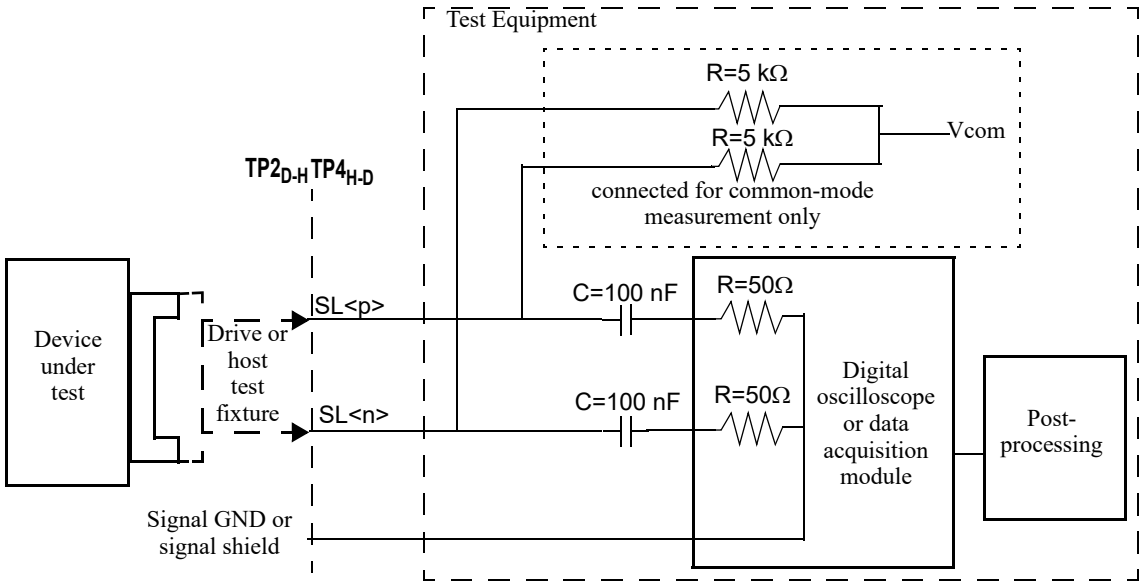

Figure 128B–1—Test configuration

128B.1 Host and drive compliance boards

128B.1.1 Test fixture return loss

The differential return loss, in dB, of the test fixture is specified in a mated state and shall meet the requirements of 128B.2.2.

128B.1.2 Test fixture insertion loss

The test fixture printed circuit board insertion loss values determined using Equation (128B–1) shall be used as the reference test fixture insertion loss.

$$Insertion\_loss_{tfref}(f) = 0.44\sqrt{f} + 0.2293f \text{ (dB)} \quad (128B–1)$$

for $0.05 \le f \le 5.15625$

where

f is the frequency in GHz
$Insertion\_loss_{tfref}$ is the reference test fixture insertion loss at frequency f

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The reference test fixture insertion loss limit is illustrated in Figure 128B–2.

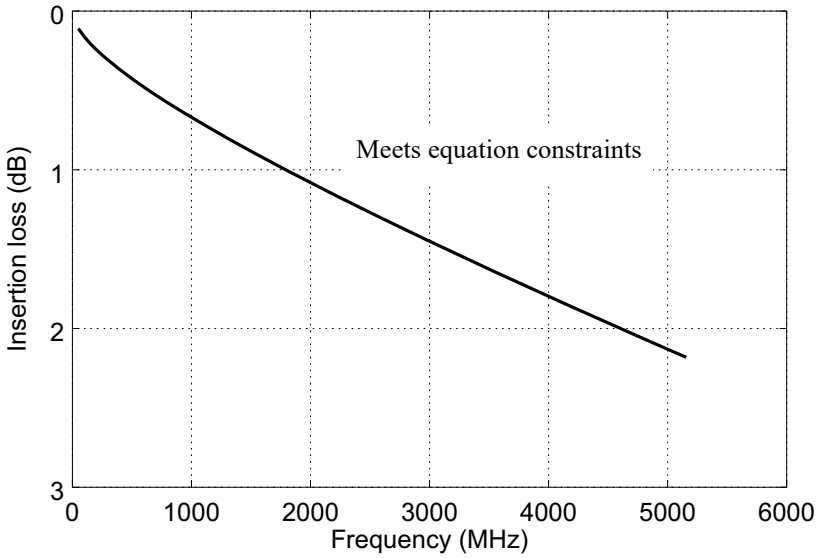

Figure 128B–2—Reference test fixture insertion loss limit

128B.2 Mated test fixtures

The test fixtures are specified in a mated state illustrated in Figure 128B–3. Return loss shall be verified at all test points shown in Figure 128B–3. A connector that meets the following requirements is specified in SFF-8482.

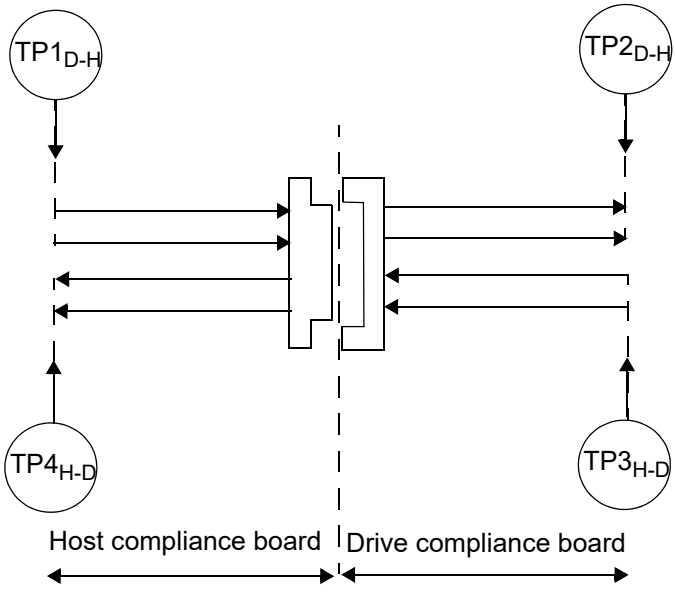

Figure 128B–3—Mated test fixture

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128B.2.1 Mated test fixtures insertion loss

The insertion loss of the mated test fixtures shall meet the values determined using Equation (128B–2) and Equation (128B–3).

$$Insertion\_loss(f) \le Insertion\_loss_{MTF_{max}}(f) = \left\{ \begin{array}{ll} 1.6782\sqrt{f} + 0.293f & 0.05 \le f < 2.578125 \\ -2.4145 + 2.2747f & 2.578125 \le f < 5.15625 \end{array} \right\} \text{(dB)} \quad \text{(128B–2)}$$

$$Insertion\_loss(f) \le Insertion\_loss_{MTF_{min}}(f) = (0.9486\sqrt{f} + 0.1656f) \quad 0.05 \le f \le 5.15625 \text{ (dB)} \quad \text{(128B–3)}$$

where

f	is the frequency in GHz
Insertion_loss(f)	is the test fixture insertion loss at frequency f

The mated test fixture insertion loss limit is illustrated in Figure 128B–4.

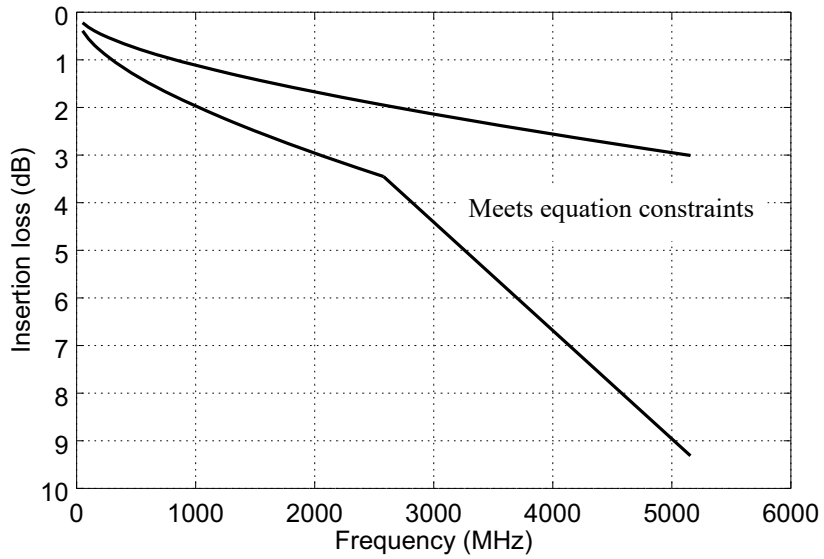

Figure 128B–4—Mated test fixtures insertion loss limit

128B.2.2 Mated test fixtures return loss

The return loss of the mated test fixtures measured at each test fixture interface shall meet the values determined using Equation (128B–4).

$$Return\_loss(f) \le Return\_loss_{MTF_{max}}(f) = \left\{ \begin{array}{ll} 17 - f & 0.01 \le f < 4 \\ 15 - 0.5f & 4 \le f < 5.15625 \end{array} \right\} (dB) \quad \text{(128B–4)}$$

where

f	is the frequency in GHz
Return_loss(f)	is the insertion loss at frequency f

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The mated test fixture return loss limit is illustrated in Figure 128B–5.

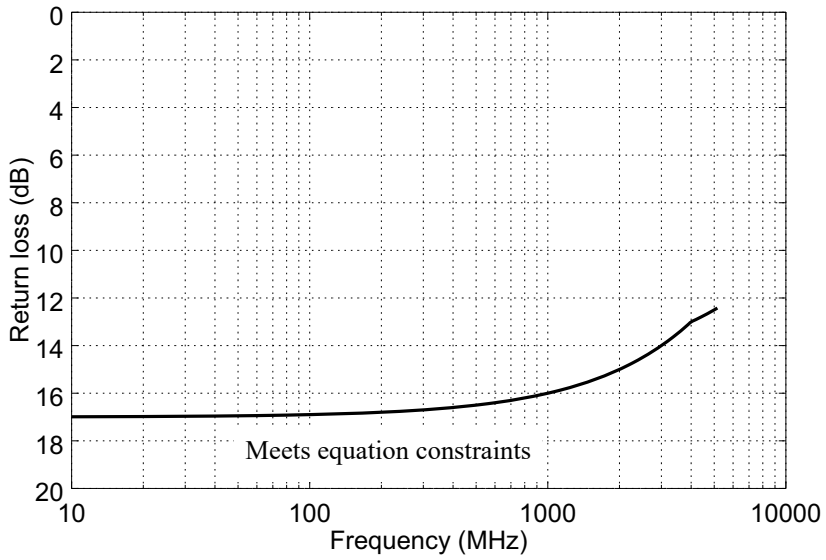

Figure 128B–5—Mated test fixture return loss limit

128B.2.3 Mated test fixtures integrated crosstalk noise

The values of the mated test fixtures integrated crosstalk RMS noise voltages determined using Equation (128B–5) through Equation (128B–7) for the near-end crosstalk loss shall meet the specifications in Table 128B–1.

Table 128B–1—Mated test fixtures integrated crosstalk noise

Parameter	ICN	Units
NEXT integrated crosstalk noise voltage	less than 1.8	mV

128B.2.3.1 Mated test fixture near-end crosstalk (NEXT) loss

ICN is calculated from the *NEXT*. Given the near-end crosstalk loss *NEXT_loss(f)* measured over N uniformly-spaced frequencies f_n spanning the frequency range 50 MHz to 5.15625 GHz with a maximum frequency spacing of 10 MHz, the RMS value of the integrated crosstalk noise is determined using Equation (128B–5) through Equation (128B–7). The RMS crosstalk noise is characterized at the output of a specified receive filter utilizing a specified transmitter waveform and the measured crosstalk transfer functions. The combined transmitter and receiver filters are defined by Equation (128B–5) as a weighting function to the crosstalk in Equation (128B–6). The sinc function is defined by $\mathrm{sinc}(x) = \sin(\pi x)/(\pi x)$.

Define the weight at each frequency f_n using Equation (128B–5).

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$$W_{nt}(f_n) = \left(\frac{A_{nt}^2}{f_b}\right)\mathrm{sinc}^2\left(\frac{f_n}{f_b}\right)\left[\frac{1}{1+\left(\frac{f_n}{f_{nt}}\right)^4}\right]\left[\frac{1}{1+\left(\frac{f_n}{f_r}\right)^8}\right] \quad (128B–5)$$

The 3 dB transmit filter bandwidth f_{nt} is inversely proportional to the 20% to 80% rise and fall time T_{nt}. The constant of proportionality is 0.2365 (e.g., $T_{nt}f_{nt} = 0.2365$; with f_{nt} in hertz and T_{nt} in seconds). In addition, f_r is the 3 dB reference receiver bandwidth, which is set to 8 GHz.

The near-end integrated crosstalk noise is calculated using Equation (128B–6).

$$\sigma_{nx} = \left[2\Delta f\sum_n W_{nt}(f_n)10^{\frac{-NEXT\_loss(f_n)}{10}}\right]^{1/2} \quad (128B–6)$$

where

Δf	is the uniform frequency step of f_n
NEXT_loss(f)	is the NEXT loss at frequency f in dB

The total integrated crosstalk noise is calculated using Equation (128B–7).

$$\sigma_x = \sigma_{nx} \quad (128B–7)$$

The total integrated crosstalk noise for the mated test fixture is computed using the parameters shown in Table 128B–2.

Table 128B–2—Integrated crosstalk noise characteristics

Parameter	Subclause reference	Value	Units
Symbol rate	f_b	5.51625	GBd
Near-end disturber peak differential output amplitude	A_{nt}	600	mV
Near-end disturber 20% to 80% rise and fall times	T_{nt}	20	ps

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128B.3 Protocol implementation conformance statement (PICS) proforma for Annex 128B, Test fixtures for 2.5 Gb/s and 5 Gb/s Storage Enclosure Interfaces[311]

128B.3.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 128B, Test fixtures for 2.5 Gb/s and 5 Gb/s Storage Enclosure Interfaces, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

128B.3.2 Identification

128B.3.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

128B.3.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 128B, Test fixtures for 2.5 Gb/s and 5 Gb/s Storage Enclosure Interfaces
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

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128B.3.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
TFS	Test fixtures - Storage	128B		O	Yes [ ] No [ ]

128B.3.4 PICS proforma tables for test fixtures

128B.3.4.1 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Reference test fixture return loss	128B.1.1	Mated connector return loss as required in 128B.2.2	M	Yes [ ]
TF2	Reference test fixture insertion loss	128B.1.2	Values using Equation (128B–1)	M	Yes [ ]
TF3	Return loss test points	128B.2	Return loss verified at all test points in Figure 128B–3	M	Yes [ ]
TF4	Insertion loss of mated test fixtures	128B.2.1	Values using Equation (128B–2) and Equation (128B–3)	M	Yes [ ]
TF5	Return loss of mated test fixtures	128B.2.2	Values using Equation (128B–4)	M	Yes [ ]
TF6	Mated fixture single disturber crosstalk	128B.2.3	Meet parameters in Table 128B–1	M	Yes [ ]

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Annex 130A

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5 Gb/s Storage Enclosure Interface (5GSEI)

130A.1 Overview

This clause defines the functional and electrical characteristics for 5GSEI. This interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable storage drive module interfaces.The compliance point definitions provide a unique partitioning of the channel defined in Annex 69B, such that the test points $TP0_{D\text{-}H}$ and $TP0_{H\text{-}D}$ defined in this Annex are equivalent to TP1 defined in Figure 130–1, and $TP5_{D\text{-}H}$ and $TP5_{H\text{-}D}$ defined in this Annex are equivalent to TP4 defined in Figure 130–1. Figure 130A–1 shows the test point locations associated with 5GSEI.

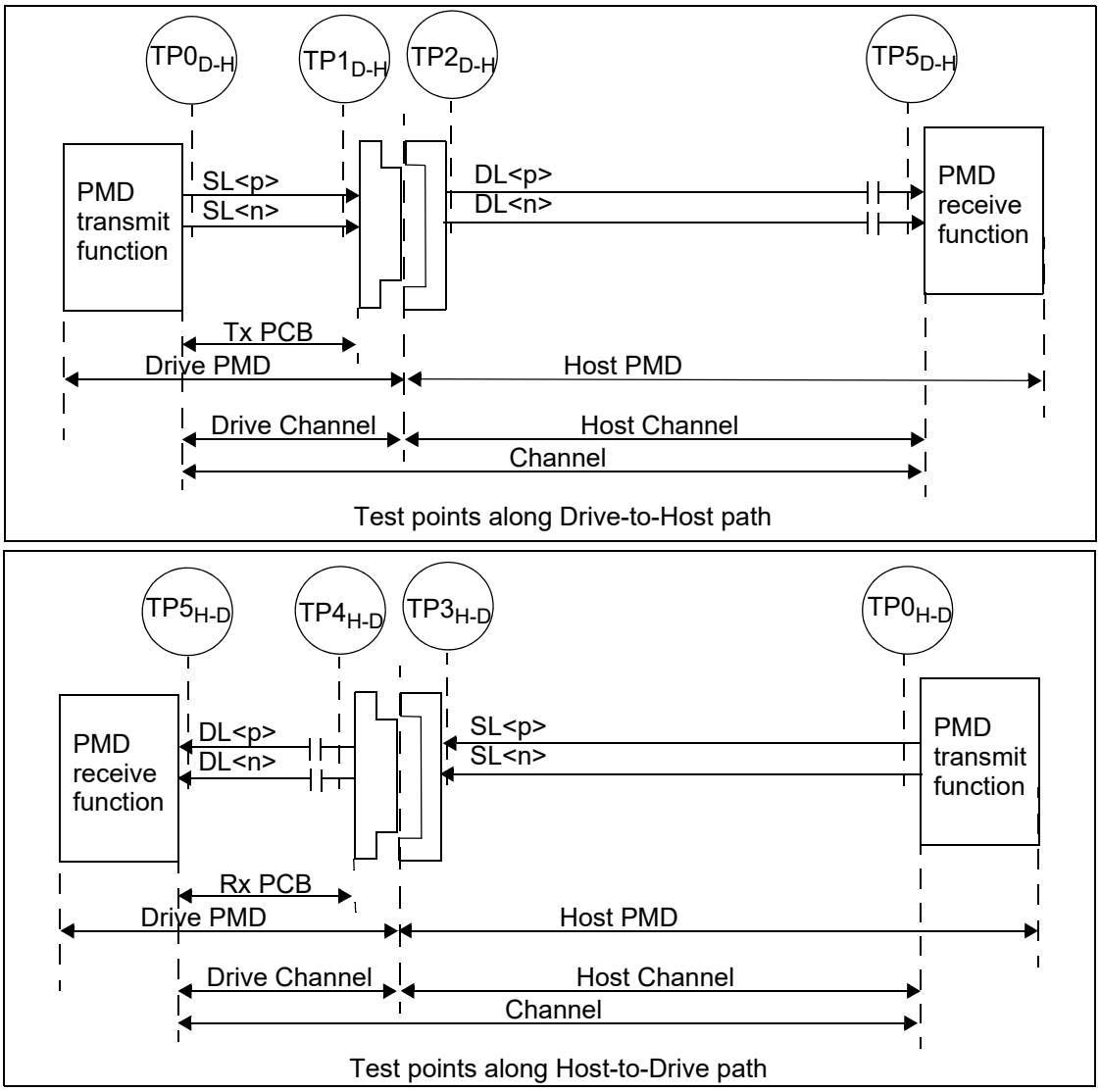

Figure 130A–1—Test points

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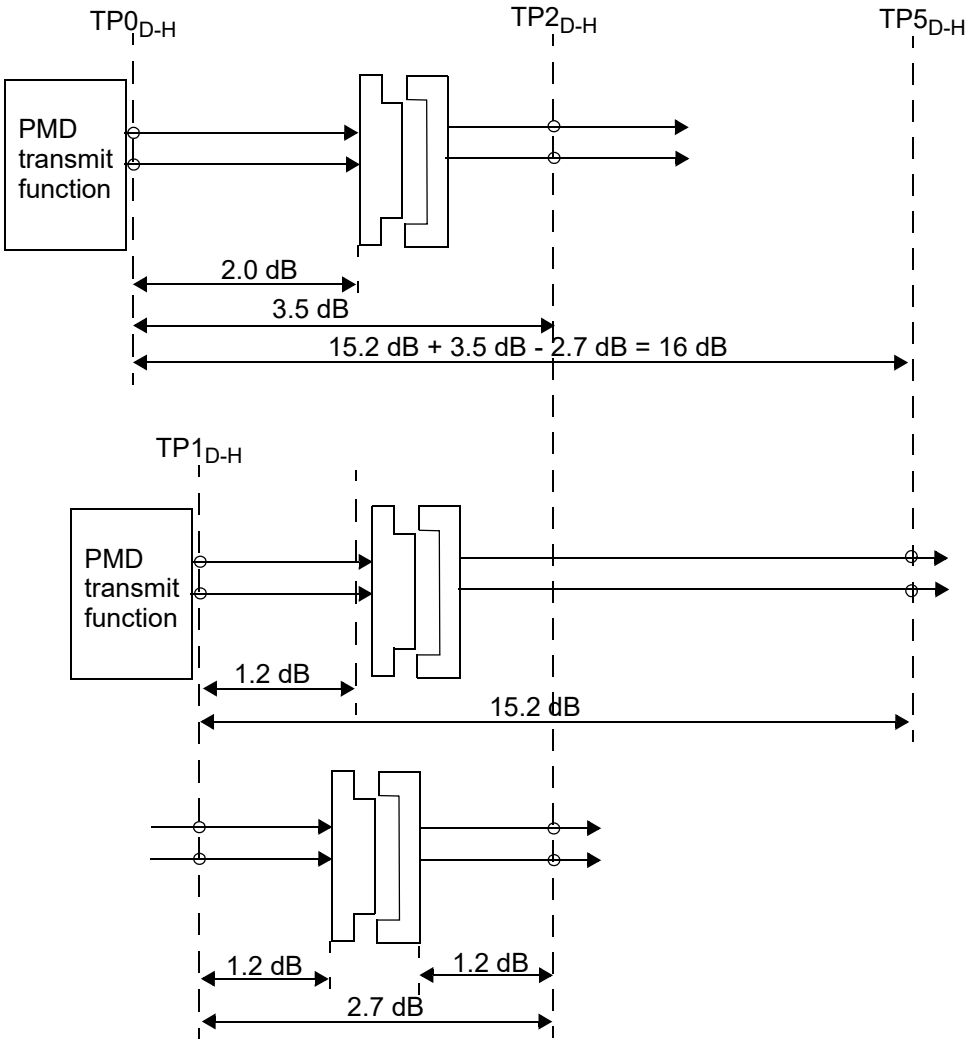
The 5GSEI link is described in terms of a host 5GSEI component with associated insertion loss and a drive 5GSEI component. Figure 130A–2 (one direction shown) depicts the recommended differential insertion loss budget at 2.578125 GHz for a typical 5GSEI application. The recommended maximum differential insertion loss from TP0 to TP5 is given in Equation (130A–1) and depicted in Figure 130A–3. The 5GSEI interface consists of independent data paths in each direction. Each data path contains one differential lane, which is AC-coupled on the receiver side. The nominal signaling rate for each lane is 5.15625 GBd.



NOTE—The connector insertion loss is 0.3 dB for the mated test fixture.

Figure 130A–2—Insertion loss budget at 2.578125 GHz

$$Insertion\_loss(f) \le \begin{cases} 0.668 + 3.755\sqrt{f} + 3.608f & 0.05 \le f < 2.578125 \\ -18.753 + 13.48f & 2.578125 \le f < 3.8671875 \end{cases} \text{ (dB)} \qquad (130A\text{–}1)$$

where

f is the frequency in GHz

Insertion_loss(f) is chip to chip (C2C) insertion loss

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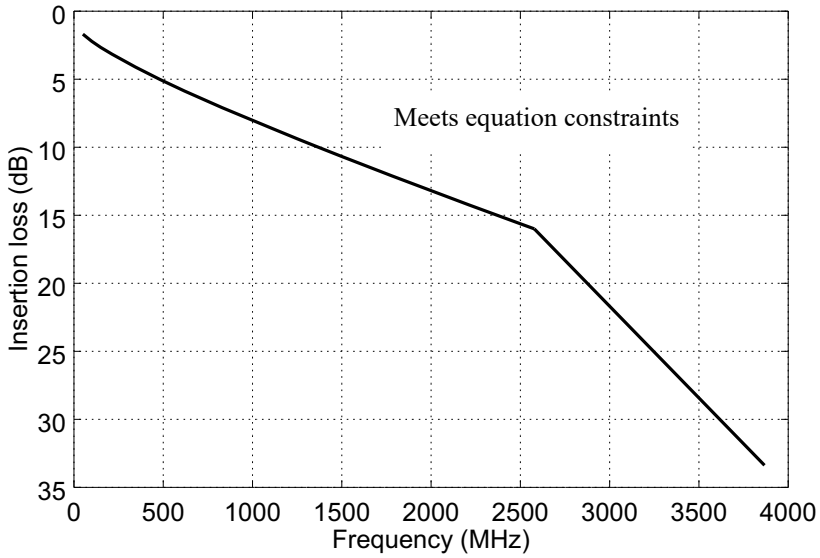

Figure 130A–3—Illustration of recommended maximum differential insertion loss from TP0 to TP5

130A.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 10^{-12} with any errors sufficiently un-correlated to ensure an acceptably high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding.

130A.2 5GSEI compliance point definitions

The electrical characteristics for 5GSEI are defined at compliance points for the host and drive, respectively. Reference test fixtures, called compliance boards, are used to access the electrical specification parameters. Figure 130A–4 depicts the location of compliance points when measuring host 5GSEI compliance. The output of the Host Compliance Board (HCB) is used to verify the host electrical output signal at $TP4_{H\text{-}D}$. Similarly, the input of the HCB at $TP1_{D\text{-}H}$ is used to verify the host input compliance.

Figure 130A–5 depicts the location of compliance points when measuring drive 5GSEI compliance. The output of the Drive Compliance Board (DCB) is used to verify the drive electrical output signal at $TP2_{D\text{-}H}$. Similarly, the input of the DCB at $TP3_{H\text{-}D}$ is used to verify the drive input compliance. Additional details on the requirements for the HCB and DCB are given in Annex 128B.

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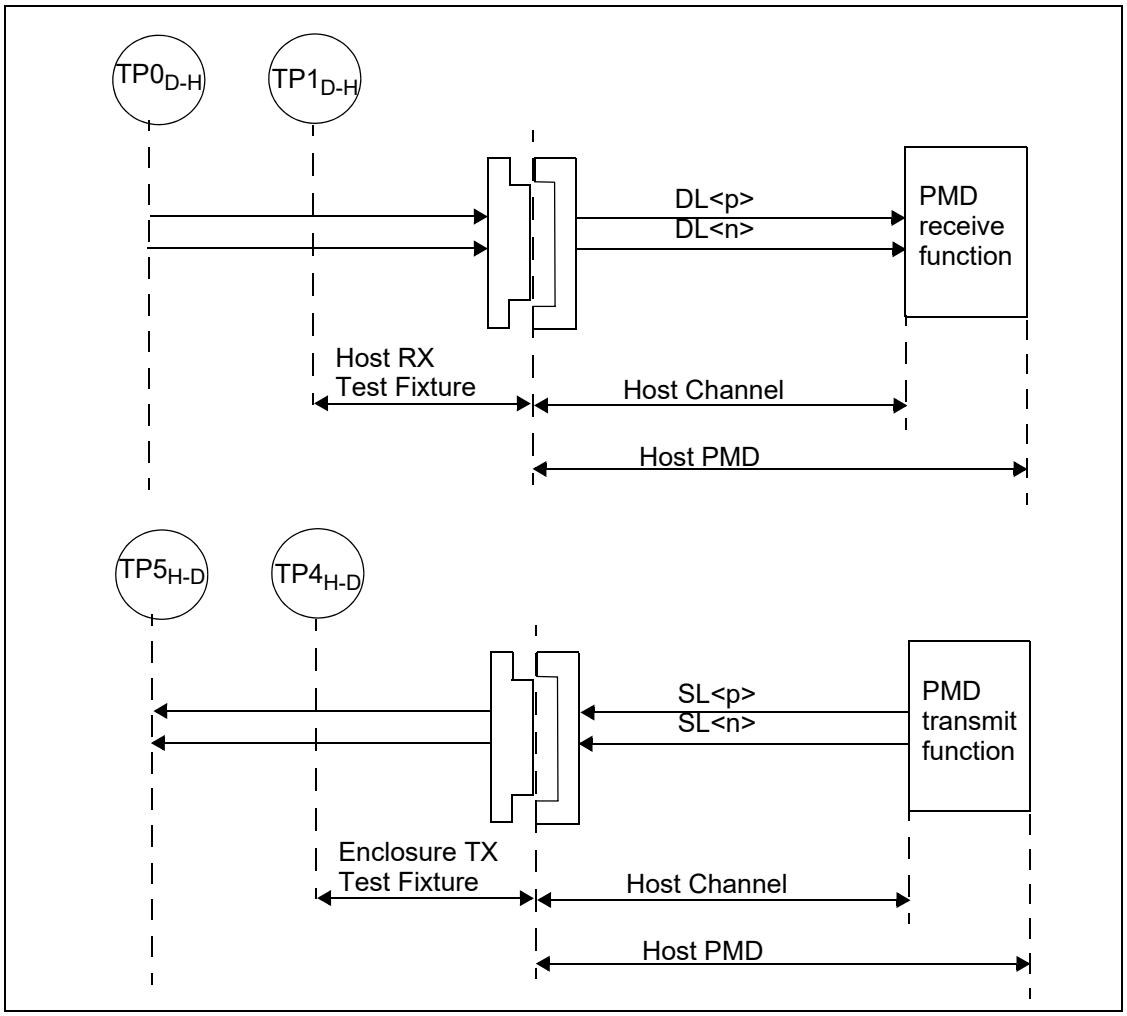

Figure 130A–4—Host compliance board

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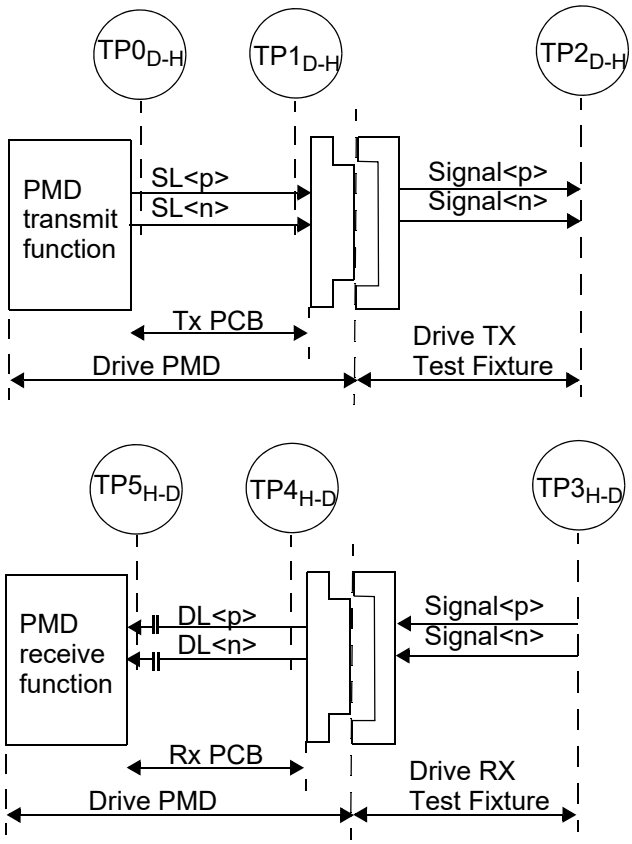

Figure 130A–5—Drive compliance board

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130A.3 5GSEI electrical characteristics

130A.3.1 5GSEI host output characteristics

A 5GSEI host output shall meet the specifications defined in Table 130A–1 if measured at $TP4_{H\text{-}D}$ (see Figure 130A–4).

Table 130A–1—5GSEI host output characteristics

Parameter	Subclause reference	Value	Units
Signaling rate	130A.3.1.1	5.15625 ± 100 ppm	GBd
Nominal unit interval	130A.3.1.1	193.9	ps
DC common-mode output voltage (max)	130A.3.1.2	1.9	V
AC common-mode output voltage (max, RMS)	130A.3.1.2	30	mV
Peak-to-peak differential output voltage (min) transmitter enabled	130A.3.1.2	800	mV
Peak-to-peak differential output voltage (max) transmitter enabled	130A.3.1.2	1200	mV
Peak-to-peak differential output voltage (max) transmitter disabled	130A.3.1.2	35	mV
Differential output return loss (min)	130A.3.1.3	See Equation (130A–2)	dB
Output waveform			
Transmitter steady-state voltage, v_f(max)	130A.3.1.4.2	600	mV
Transmitter steady-state voltage, v_f(min)		285	mV
Linear fit pulse peak (min)	130A.3.1.4.2	0.41 × v_f	mV
Pre-cursor coefficient	130A.3.1.4.3	0.65 ± 0.1	—
Max output jitter (peak-to-peak)			
Random jitter	130A.3.1.6	0.15	UI
Deterministic jitter	130A.3.1.6	0.12	UI
Duty Cycle Distortion[1]	130A.3.1.6	0.035	UI
Total jitter	130A.3.1.6	0.27	UI
Signal-to-noise-and-distortion ratio (min) - SNDR	130A.3.1.7	25	dB

[1]Duty Cycle Distortion is considered part of deterministic jitter distribution.

A test system as depicted in Figure 128B–1, with a fourth-order Bessel-Thomson low-pass response with 8 GHz 3 dB bandwidth, is to be used for all output signal measurements, unless otherwise specified.

130A.3.1.1 Signaling rate and range

The 5GSEI signaling rate is specified in Table 130A–1. The nominal unit interval is the inverse of the signaling rate.

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130A.3.1.2 Signaling levels

The differential output voltage V_d is defined to be the difference between the single-ended output voltages, *SL*<*p*> minus *SL*<*n*>. The common-mode voltage V_{cm} is defined to be one half of the sum of *SL*<*p*> and *SL*<*n*>. These definitions are illustrated by Figure 130A–6.

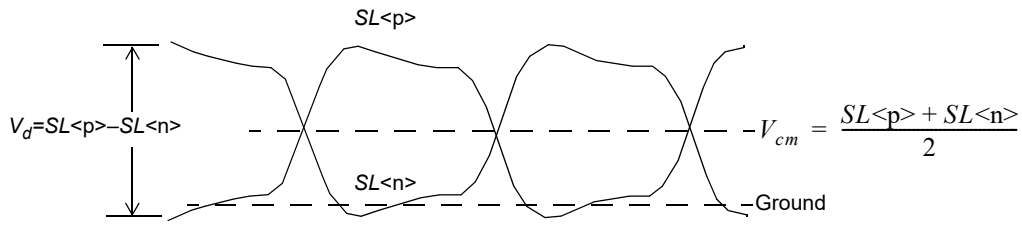

Figure 130A–6—Voltage definitions

The peak-to-peak differential output voltage is specified in Table 130A–1, when the transmitter is enabled and disabled. The DC common-mode output voltage and AC common-mode output voltage are defined with respect to signal ground.

130A.3.1.3 Output return loss

The differential output return loss, in dB, of the output is shown in Equation (130A–2) and illustrated in Figure 130A–7. This output requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 Ω.

$$Return\_loss(f) \geq \begin{cases} Return\_loss_{min}(f) = 12 & 50 \leq f < 275 \\ Return\_loss_{min}(f) = 12 - 6.75\log_{10}\left(\frac{f}{275\ \text{MHz}}\right) & 275 \leq f < 3000 \\ Return\_loss_{min}(f) = 5 & 3000 \leq f < 3867.1875 \end{cases} \text{ (dB)} \quad (130A\text{–}2)$$

where

f is the frequency in MHz

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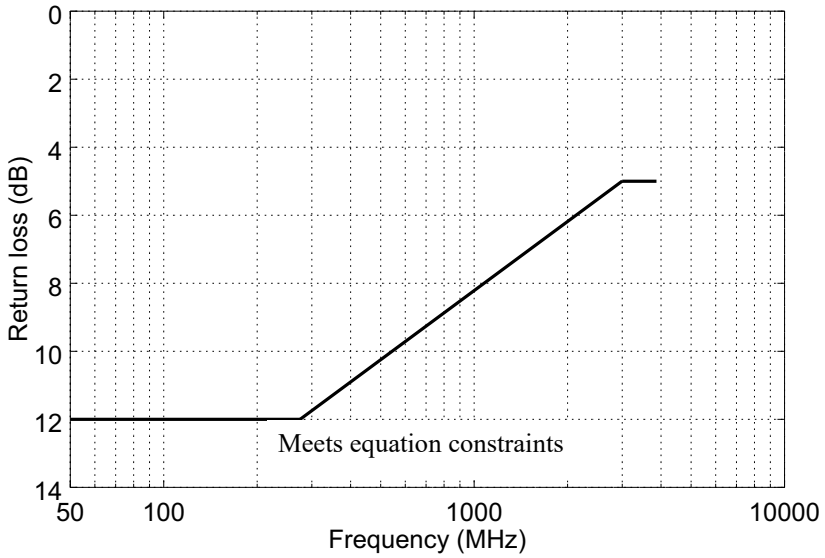

Figure 130A–7—Differential return loss limit

130A.3.1.4 Transmitter output waveform

The 5GSEI transmit function includes programmable equalization to compensate for the frequency dependent loss of the channel and facilitate data recovery at the receiver. The functional model for the transmit equalizer is the two tap transversal filter shown in Figure 130A–8. The state of the transmit equalizer and hence the transmitted output waveform may be manipulated via the management interface.

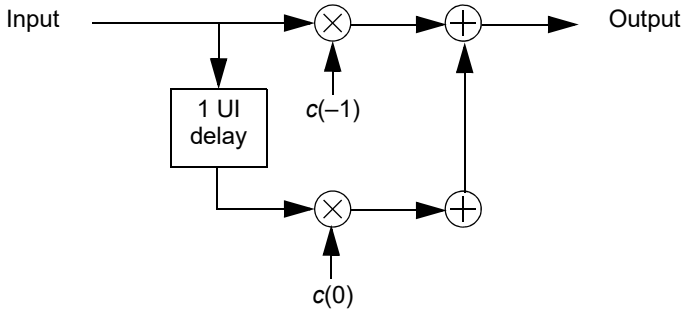

Figure 130A–8—Transmit equalizer functional model

130A.3.1.4.1 Linear fit to the measured waveform

The linear fit pulse response and normalized transmitter coefficient values are characterized using the procedure described in 92.8.3.5.1 with the exception that the measurement is performed at $TP4_{H\text{-}D}$ (see Figure 130A–4) rather than TP2, N_p =8.

130A.3.1.4.2 Steady-state voltage and linear fit pulse peak

The linear fit pulse, $p(k)$, is determined according to 130A.3.1.4.1. The steady-state voltage v_f is defined to be the sum of the linear fit pulse $p(k)$ divided by M, determined in step 3 of the linear fit procedure.

130A.3.1.4.3 Pre-cursor coefficient

The Pre-cursor coefficient, c(-1), is determined according to 130A.3.1.4.1.

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130A.3.1.5 Transmit jitter test requirements

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in 48B.3. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 4 MHz is applied to the jitter. The data pattern for jitter measurements shall be a square wave as defined in 52.9.1.2 with 5 consecutive 1's and 0's. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal.

130A.3.1.6 Transmit jitter

The transmitter shall have a maximum total jitter, composed of a maximum deterministic component and a maximum random component as shown in Table 130A–1. Duty cycle distortion (DCD) is considered a component of deterministic jitter and shall not exceed the value shown in Table 130A–1. The peak-to-peak duty cycle distortion is defined as the absolute value of the difference in the mean pulse width of a 1 pulse or the mean pulse width of a 0 pulse (as measured at the mean of the high- and low-voltage levels in a clock like repeating bit sequence) and the nominal pulse width. Jitter specifications are specified for BER = 10^{-12}. Transmit jitter test requirements are specified in 130A.3.1.5.

130A.3.1.7 Transmitter output noise and distortion

Signal-to-noise-and-distortion ratio (SNDR) is measured at the transmitter output using the following method:

a) Capture at least one complete cycle of the test pattern PRBS9 as specified in Table 68–6 at $TP4_{H\_D}$ (see Figure 130A–4) per 85.8.3.3.4.

b) Apply the reference equalizer from 93A.1.4.3, using the values from Table 130A–2.

c) Compute the linear fit pulse response $p(k)$ and the linear fit error waveform $e(k)$ from the resulting waveform per 85.8.3.3.5 using N_p=8 and D_p = 1. Denote the standard deviation of $e(k)$ as σ_e.

d) Measure the RMS deviation from the mean voltage at a fixed point in a run of at least 8 consecutive identical bits in a suitable pattern. PRBS9 is an example of a pattern that includes runs suitable to perform the measurement. It is recommended that the deviation is measured within the flattest portion of the waveform at a point where the slope is closest to zero. The RMS deviation is measured for a run of zeros and also a run of ones. The average of the two measurements is denoted as σ_n.

Table 130A–2—5G host receiver equalizer parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	5.15625 ± 100 ppm	GBd
Continuous time filter, DC gain [1] Minimum value Maximum value Step size	g_{DC}	 –14.5 0 0.5	 dB dB dB
Continuous time filter, zero frequency	f_z	$f_b/2$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b/2$ f_b	GHz

[1] The DC gain, gDC, is optimized to satisfy the SNDR requirement.

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SNDR is defined by Equation (130A–3).

$$SNDR = 10\log_{10}\left(\frac{p_{max}^{2}}{\sigma_e^{2} + \sigma_n^{2}}\right)\text{dB} \quad (130A–3)$$

where

$p_{\max}$ is the maximum value of $p(k)$

130A.3.2 5GSEI host input characteristics

A 5GSEI host input shall meet the specifications defined in Table 130A–3, measured at $TP1_{D\text{-}H}$ (see Figure 130A–4).

Table 130A–3—5GSEI host input characteristics

Parameter	Subclause reference	Value	Units
Differential input return loss (min)	130A.3.2.1	See Equation (130A–2)	dB
Interference tolerance	130A.3.2.2	Table 130A–4	—
Jitter tolerance	130A.3.2.3	Table 130A–5	—

130A.3.2.1 Input differential return loss

The host input differential return loss shall meet Equation (130A–2) measured at $TP1_{D\text{-}H}$ (see Figure 130A–4).

130A.3.2.2 Receiver interference tolerance

The following considerations apply to the interference tolerance test. The pattern generator is calibrated at $TP2_{D\text{-}H}$ (see Figure 130A–9) to produce the values in Table 130A–4. The channel noise source is a broadband noise generator capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from f_1 in Table 69B–2 to 0.5 times the signaling speed for the port type under test with a crest factor of no less than 5. The noise shall be measured at the output of a filter connected to the output of the noise source. The filter for this measurement shall have no more than a 40 dB per decade roll-off and a 3 dB cut-off frequency shall be equal to 0.5 times the signaling speed. Figure 130A–9 illustrates the calibration and test configurations that are needed for the host interference tolerance test. The data pattern used for the receiver interference tolerance test shall be PRBS31 (see 49.2.8). The BER shall be less than or equal to 10^{-12} for any signaling speed in the range of 5.15625 GBd ± 100 ppm.

Calibration procedure is as follows:

a) Create a channel (ISI channel + HCB + DCB) with as close to 6 dB of loss at 2.578125 GHz as possible.
b) Measure signal through the ISI channel at $TP2_{D\text{-}H}$ (see Figure 130A–9).
c) Adjust pattern generator output and ISI channel to meet the required linear fit pulse peak and precursor equalization ratio values.

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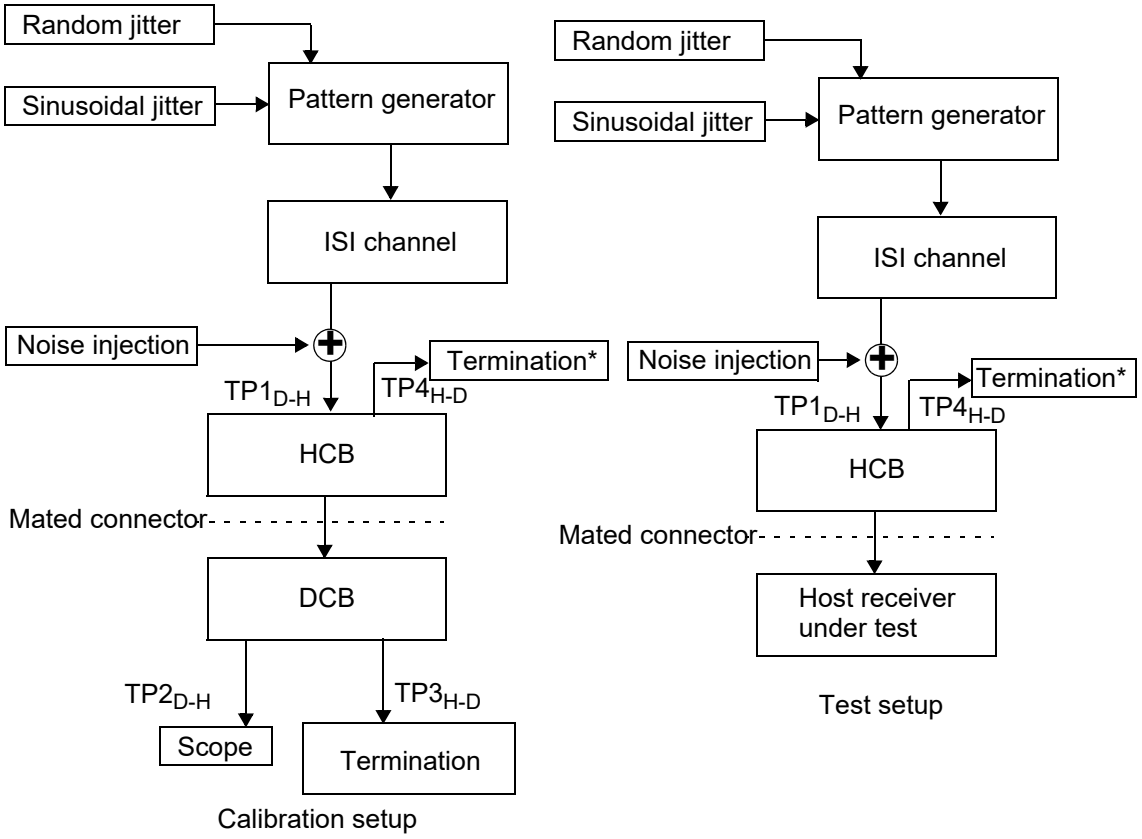
d) Adjust pattern generator amplitude to meet the required steady-state voltage.

e) Adjust noise to meet the required SNDR (see 130A.3.1.7).

f) Adjust pattern generator random jitter to the required value and then add sinusoidal jitter at 20 MHz to reach the total jitter requirement.



* The single-ended transmit signals are terminated in 50 Ω to provide a 100 Ω differential termination.

Figure 130A–9—Host interference calibration and test setup

Table 130A–4—5GSEI host interference parameters

Parameter	Value	Units
Transmitter steady-state voltage, v_f	360	mV
Linear fit pulse peak	$0.85 \times v_f$	mV
Pre-cursor equalization ratio	1.2	—
Total Jitter	0.3	UI
Random Jitter	0.15	UI
SNDR	28	dB

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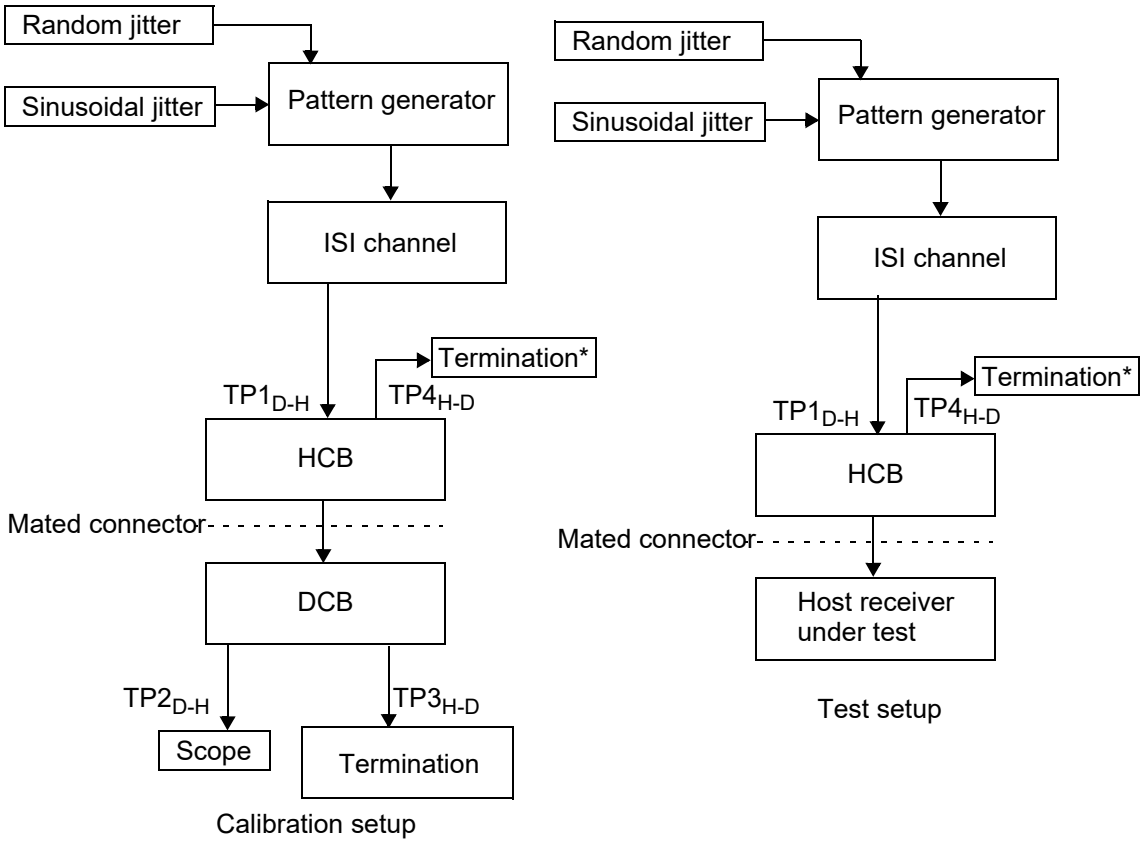
130A.3.2.3 Receiver jitter tolerance

The following considerations apply to the jitter tolerance test. The transmitter is calibrated at $TP2_{D\text{-}H}$ (see Figure 130A–10) to produce the values in Table 130A–5. Broadband noise is not injected during this test except for what is inherently present in the host. Figure 130A–12 illustrates the calibration and test configurations that are needed for the host jitter tolerance test. The data pattern used for the receiver jitter tolerance test shall be PRBS31 (see 49.2.8). The BER shall be less than or equal to 10^{-12} for any signaling speed in the range of 5.15625 GBd ± 100 ppm.

Calibration procedure is as follows:

a) Create a channel (ISI channel + HCB + DCB) with as close to 6 dB of loss at 2.578125 GHz as possible.
b) Measure signal through the ISI channel at $TP2_{D\text{-}H}$ (see Figure 130A–10).
c) Adjust pattern generator output and ISI channel to meet the required linear fit pulse peak and precursor equalization ratio values.
d) Adjust pattern generator amplitude to meet the required steady-state voltage.
e) Adjust pattern generator random jitter to the required value.
f) Adjust sinusoidal jitter until the values in Table 130A–6 are met.



* The single-ended transmit signals are terminated in 50 Ω to provide a 100 Ω differential termination.

Figure 130A–10—Host jitter tolerance calibration and test setup

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Table 130A–5—5GSEI host jitter tolerance parameters

Parameter	Value	Units
Transmitter steady-state voltage, v_f	360	mV
Linear fit pulse peak	0.85 × v_f	mV
Pre-cursor equalization ratio	1.2	—
Random Jitter	0.15	UI
Applied peak-to-peak sinusoidal jitter	Table 130A–6	

Table 130A–6—Applied peak-to-peak sinusoidal jitter

Parameter	Case 1	Case 2	Case 3	Units
Jitter frequency	0.02	4	20	MHz
Peak-to-peak jitter amplitude	5	0.15	0.15	UI

130A.3.3 5GSEI drive output characteristics

A 5GSEI drive output shall meet the specifications defined in Table 130A–7 if measured at $TP2_{D\text{-}H}$ (see Figure 130A–5).

Table 130A–7—5GSEI drive output characteristics

Parameter	Subclause reference	Value	Units
Signaling rate	130A.3.1.1	5.15625 ± 100 ppm	GBd
Nominal unit interval	130A.3.1.1	193.9	ps
DC common-mode output voltage (max)	130A.3.1.2	1.9	mV
AC common-mode output voltage (max, RMS)	130A.3.1.2	30	mV
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	 130A.3.1.2 130A.3.1.2	 35 1200	mV
Differential output return loss (min)	130A.3.1.3	See Equation (130A–2)	dB
Output waveform Transmitter steady-state voltage, v_f(max) Transmitter steady-state voltage, v_f(min) Linear fit pulse peak (min) Pre-cursor coefficient	 130A.3.3.2 130A.3.3.2 130A.3.3.2 130A.3.3.3	 600 360 0.85 × v_f –0.125 to –0.075	 mV mV mV —
Max output jitter (peak-to-peak) Random jitter Deterministic jitter Duty Cycle Distortion[1] Total jitter	 130A.3.1.6 130A.3.1.6 130A.3.1.6 130A.3.1.6	 0.15 0.12 0.035 0.27	 UI UI UI UI
Signal-to-noise-and-distortion ratio (min) (SNDR)	130A.3.3.4	28	dB

[1]Duty Cycle Distortion is considered part of deterministic jitter distribution.

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A test system as depicted in Figure 128B–1, with a fourth-order Bessel-Thomson low-pass response with 8 GHz 3 dB bandwidth, is to be used for all output signal measurements, unless otherwise specified.

130A.3.3.1 Linear fit to the measured waveform

The linear fit pulse response and normalized transmitter coefficient values are characterized using the procedure described in 92.8.3.5.1 with the exception that the measurement is performed at $TP2_{D\text{-}H}$ (see Figure 130A–5) rather than TP2, and set $N_p = 8$.

130A.3.3.2 Steady-state voltage and linear fit pulse peak

The linear fit pulse, $p(k)$, is determined according to 130A.3.3.1. The steady-state voltage v_f shall have the limits shown in Table 130A–7.

130A.3.3.3 Precursor coefficient

The Precursor coefficient, c(-1), is determined according to 130A.3.3.1.

130A.3.3.4 Transmitter output noise and distortion

Signal-to-noise-and-distortion ratio (SNDR) is measured at the transmitter output using the following method:

a) Capture at least one complete cycle of the test pattern PRBS9 as specified in Table 68–6 at $TP2_{D\_H}$ (see Figure 130A–5) per 85.8.3.3.4.
b) Apply the reference equalizer from 93A.1.4.3, using the values from Table 130A–8
c) Compute the linear fit pulse response $p(k)$ and the linear fit error waveform $e(k)$ from the resulting waveform per 85.8.3.3.5 using N_p=8 and $D_p = 1$. Denote the standard deviation of $e(k)$ as σ_e.
d) Measure the RMS deviation from the mean voltage at a fixed point in a run of at least 8 consecutive identical bits in a suitable pattern. PRBS9 is an example of a pattern that includes runs suitable to perform the measurement. It is recommended that the deviation is measured within the flattest portion of the waveform at a point where the slope is closest to zero. The RMS deviation is measured for a run of zeros and also a run of ones. The average of the two measurements is denoted as σ_n.

Table 130A–8—5G Drive receiver equalizer parameter

Parameter	Symbol	Value	Units
Signaling rate	f_b	5.15625 ± 100 ppm	GBd
Continuous time filter, DC gain [1] Minimum value Maximum value Step size	g_{DC}	 –2.0 0 1	 dB dB dB
Continuous time filter, zero frequency	f_z	$f_b/2$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b/2$ f_b	GHz

[1] The DC gain, gDC, is optimized to satisfy the SNDR requirement.

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SNDR is defined by Equation (130A–4).

$$SNDR = 10\log_{10}\left(\frac{p_{max}^{2}}{\sigma_e^{2} + \sigma_n^{2}}\right)\text{dB} \quad (130A–4)$$

where

$p_{\max}$ is the maximum value of $p(k)$

130A.3.4 5GSEI drive input characteristics

A 5GSEI drive input shall meet the specifications defined in Table 130A–9, measured at $TP3_{H\text{-}D}$ (see Figure 130A–5).

Table 130A–9—5GSEI drive input characteristics

Parameter	Subclause reference	Value	Units
Differential input return loss (min)	130A.3.4.1	See Equation (130A–2)	dB
Interference tolerance	130A.3.4.2	Table 130A–10	
Jitter tolerance	130A.3.4.3	Table 130A–11	

130A.3.4.1 Input differential return loss

The drive input differential return loss shall meet Equation (130A–2) measured at $TP3_{H\text{-}D}$ (see Figure 130A–5).

130A.3.4.2 Receiver interference tolerance

The following considerations apply to the interference tolerance test. The pattern generator is calibrated at $TP4_{H\text{-}D}$ (see Figure 130A–11) to produce the values in Table 130A–10. The channel noise source is a broadband noise generator capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from f_1 in Table 69B–2 to 0.5 times the signaling speed for the port type under test with a crest factor of no less than 5. The noise shall be measured at the output of a filter connected to the output of the noise source. The filter for this measurement shall have no more than a 40 dB per decade roll-off and a 3 dB cut-off frequency shall be equal to 0.5 times the signaling speed. Figure 130A–11 illustrates the calibration and test configurations that are needed for the drive interference tolerance test. The data pattern used for the receiver interference tolerance test shall be PRBS31 (see 49.2.8). The BER shall be less than or equal to 10^{-12} for any signaling speed in the range of 5.15625 GBd ± 100 ppm.

Calibration procedure is as follows:

a) Create a channel (ISI channel + HCB + DCB) with as close to 18.5 dB of loss at 2.578125 GHz as possible.
b) The FOM ILD (see 93A.4) of the channel shall be greater than 1 dB, with f_b set to the signaling rate of Table 130A–7, T_t set to 42 ps, and f_r set to 0.75 x f_b.
c) Measure signal through the ISI channel at $TP4_{H\text{-}D}$ (see Figure 130A–11).

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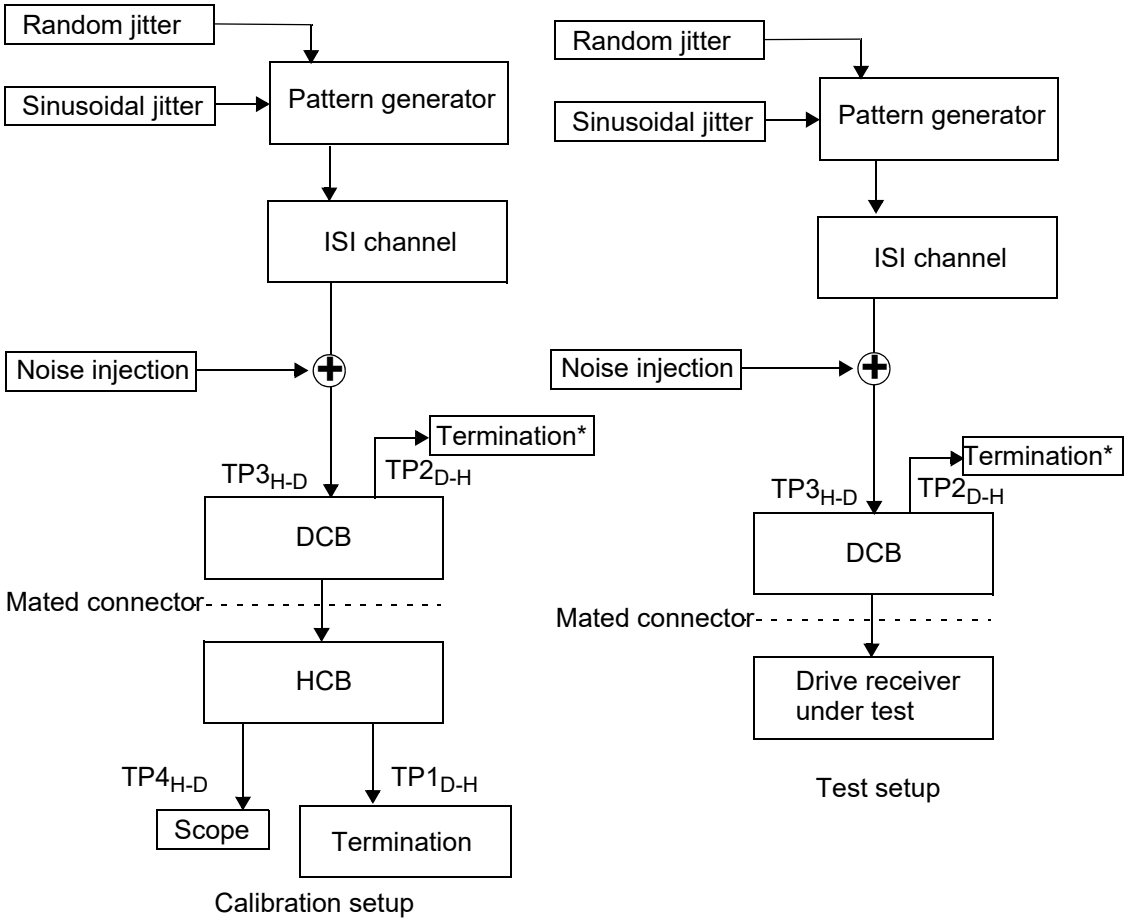
d) Adjust pattern generator output and ISI channel to meet the required linear fit pulse peak value.

e) Adjust pattern generator amplitude to meet the required steady-state voltage.

f) Adjust noise to meet the required SNDR (see 130A.3.1.7).

g) Adjust pattern generator random jitter to the required value and then add sinusoidal jitter at 20 MHz to reach the total jitter requirement.



* The single-ended transmit signals are terminated in 50 Ω to provide a 100 Ω differential termination.

Figure 130A–11—Drive interference calibration and test setup

Table 130A–10—5GSEI drive interference parameters

Parameter	Value	Units
Transmitter steady-state voltage, v_f	285	mV
Linear fit pulse peak	0.41 × v_f	mV
Total Jitter	0.3	UI
Random Jitter	0.15	UI
SNDR	25	dB

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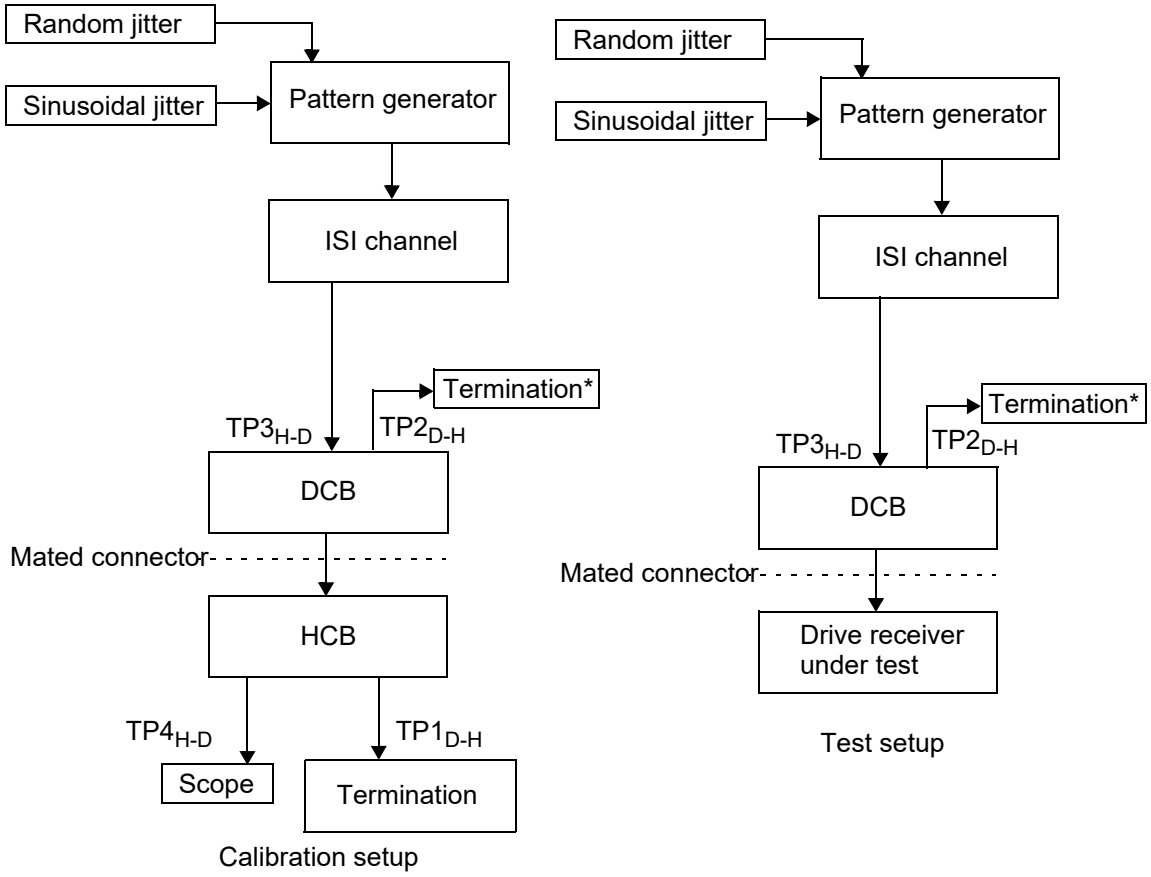
130A.3.4.3 Receiver jitter tolerance

The following considerations apply to the jitter tolerance test. The transmitter is calibrated at $TP4_{H\text{-}D}$ (see Figure 130A–12) to produce the values in Table 130A–11. Broadband noise is not injected during this test except for what is inherently present in the drive. Figure 130A–12 illustrates the calibration and test configurations that are needed for the drive jitter tolerance test. The data pattern used for the receiver jitter tolerance test shall be PRBS31 (see 49.2.8). The BER shall be less than or equal to 10^{-12} for any signaling speed in the range of 5.15625 GBd ± 100 ppm.

Calibration procedure is as follows:

a) Create a channel (ISI channel + HCB + DCB) with as close to 18.2 dB of loss at 2.578125 GHz as possible.
b) The FOM ILD (see 93A.4) of the channel shall be greater than 1 dB, with f_b set to the signaling rate of Table 130A–7, T_t set to 42 ps, and f_r set to 0.75 x f_b.
c) Measure signal through the ISI channel at $TP4_{H\text{-}D}$.
d) Adjust pattern generator output and ISI channel to meet the required linear fit pulse peak value.
e) Adjust pattern generator amplitude to meet the required steady-state voltage.
f) Adjust pattern generator random jitter to the required value.
g) Adjust sinusoidal jitter until the values in Table 130A–12 are met.



* The single-ended transmit signals are terminated in 50 Ω to provide a 100 Ω differential termination.

Figure 130A–12—Drive receiver jitter tolerance test setup

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Table 130A–11—5GSEI drive receiver jitter tolerance parameters

Parameter	Value	Units
Transmitter steady-state voltage, v_f	285	mV
Linear fit pulse peak	$0.41 \times v_f$	mV
Random Jitter	0.15	UI
Applied peak-to-peak sinusoidal jitter	Table 130A–12	dB

Table 130A–12—Applied peak-to-peak sinusoidal jitter

Parameter	Case 1	Case 2	Case 3	Units
Jitter frequency	0.02	4	20	MHz
Peak-to-peak jitter amplitude	5	0.15	0.15	UI

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130A.4 Protocol implementation conformance statement (PICS) proforma for Annex 130A, 5 Gb/s Storage Enclosure Interface (5GSEI)[312]

130A.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 130A, 5 Gb/s Storage Enclosure Interface (5GSEI), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

130A.4.2 Identification

130A.4.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

130A.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 130A, 5 Gb/s Storage Enclosure Interface (5GSEI)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	
Date of Statement	

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130A.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
5GSEI	5GSEI Storage Enclosure Interface	130A		O	Yes [ ] No [ ]

130A.4.4 PICS proforma tables for 5 Gb/s Storage Enclosure Interface (5GSEI)

Item	Feature	Subclause	Value/Comment	Status	Support
OV1	Bit Error Ratio	130A.1.1	BER < 10^{-12}	M	Yes [ ]

130A.4.4.1 Host output functions

Item	Feature	Subclause	Value/Comment	Status	Support
HO1	5GSEI host output characteristics	130A.3.1	Table 130A–1, measured at $TP4_{H\text{-}D}$	M	Yes [ ]
HO2	Tx steady-state output	130A.3.1.4.2	≥ 285 mV, ≤ 600 mV	M	Yes [ ]
HO3	Tx peak output	130A.3.1.4.2	$p(k) > 0.41 \times v_f$	M	Yes [ ]
HO4	Tx jitter test waveform	130A.3.1.5	Square wave defined in 52.9.1.2	M	Yes [ ]
HO5	Transmit jitter requirements	130A.3.1.6	Tj ≤ 0.27 UI pk-pk (Dj ≤ 0.12 UI pk-pk and Rj ≤ 0.15 UI pk-pk)	M	Yes [ ]
HO6	Tx DCD limit	130A.3.1.6	≤ 0.035 UI pk-pk	M	Yes [ ]
HO7	Tx SNDR limit	130A.3.1.7	> 25 dB using N_p=8	M	Yes [ ]

130A.4.4.2 Host input functions

Item	Feature	Subclause	Value/Comment	Status	Support
HI1	5GSEI host input characteristics	130A.3.2	Table 130A–3, measured at $TP1_{D\text{-}H}$	M	Yes [ ]
HI2	Input differential return loss	130A.3.2.1	Shall meet Equation (130A–2) at $TP1_{D\text{-}H}$	M	Yes [ ]
HI3	Receiver interference tolerance test pattern	130A.3.2.2	PRBS31	M	Yes [ ]
HI4	Receiver interference tolerance BER	130A.3.2.2	BER ≤ 10^{-12} for any signaling in range of 5.15625 GBd ± 100 ppm	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
HI5	Receiver jitter tolerance test pattern	130A.3.2.3	PRBS31	M	Yes [ ]
HI6	Receiver jitter tolerance BER	130A.3.2.3	BER ≤ 10^{-12} for any signaling in range of 5.15625 GBd ± 100 ppm	M	Yes [ ]

130A.4.4.3 Drive output functions

Item	Feature	Subclause	Value/Comment	Status	Support
DO1	5GSEI drive output characteristics	130A.3.3	Table 130A–7, measured at $TP2_{D\text{-}H}$	M	Yes [ ]
DO2	Tx Steady-State output	130A.3.3.2	≥ 360 mV, ≤ 600 mV	M	Yes [ ]
DO3	Tx peak output	130A.3.3.2	$p(k) > 0.84 \times v_f$	M	Yes [ ]
DO4	Tx SNDR limit	130A.3.3.4	> 28 dB using N_p=8	M	Yes [ ]

130A.4.4.4 Drive input functions

Item	Feature	Subclause	Value/Comment	Status	Support
DI1	5GSEI drive input parameters	130A.3.4	Table 130A–9, measured at $TP3_{H\text{-}D}$	M	Yes [ ]
DI2	Input differential return loss	130A.3.4.1	Shall meet Equation (130A–2) at $TP3_{H\text{-}D}$	M	Yes [ ]
DI3	Receiver interference tolerance test pattern	130A.3.4.2	PRBS31	M	Yes [ ]
DI4	Receiver interference tolerance BER	130A.3.4.2	BER ≤ 10^{-12} for any signaling in range of 5.15625 GBd ± 100 ppm	M	Yes [ ]
DI5	Receiver jitter tolerance test pattern	130A.3.4.3	PRBS31	M	Yes [ ]
DI6	Receiver jitter tolerance BER	130A.3.4.3	BER ≤ 10^{-12} for any signaling in range of 5.15625 GBd ± 100 ppm	M	Yes [ ]

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Annex 135A

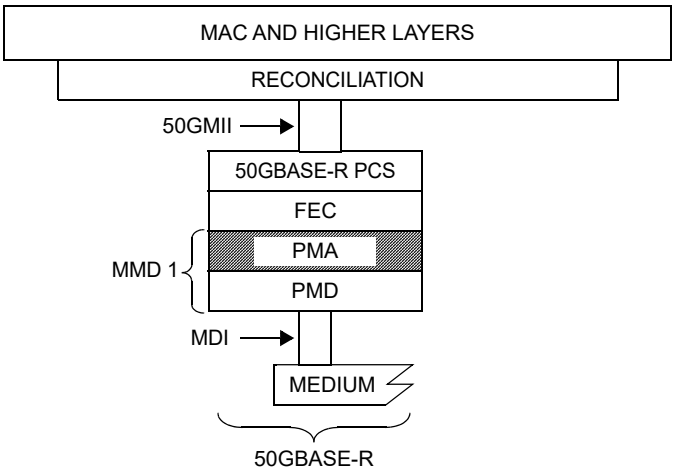
(informative)

50 Gb/s and 100 Gb/s PMA sublayer partitioning examples

The figures in this annex provide various partitioning examples. Partitioning guidelines and MMD numbering conventions are described in 135.1.4. These partitioning examples are informative and do not specify a particular sublayer combination for any PHY. Specific and compliant sublayer combinations for a particular PHY are provided in the appropriate normative clause.

135A.1 Partitioning examples of 50GBASE-R PHYs

Figure 135A–1 depicts an example of an FEC sublayer implemented with the PCS and PMD sublayers.



50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135A–1—Example FEC implemented with PCS and PMD

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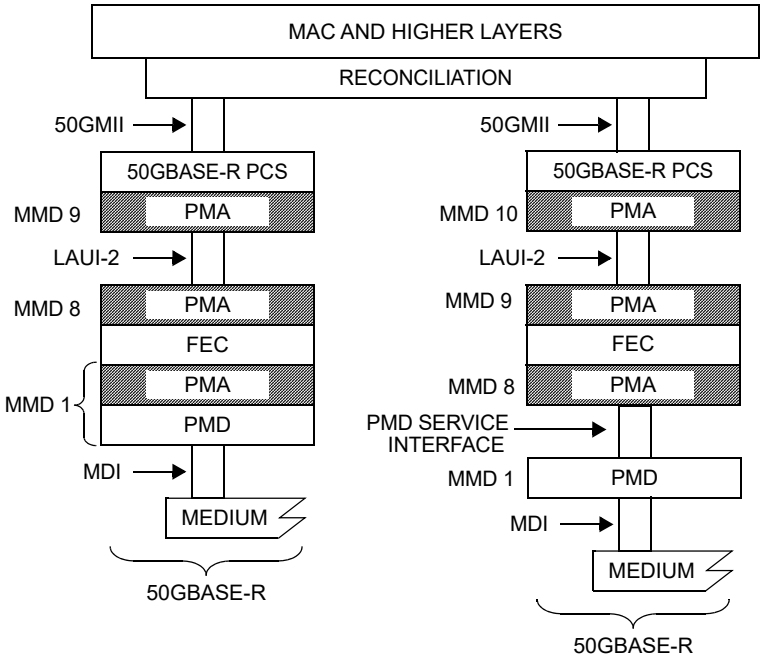
Figure 135A–2 depicts an example of an FEC sublayer implemented with the PMD sublayer.



50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LAUI-2= 50 Gb/s ATTACHMENT UNIT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135A–2—Example FEC implemented with PMD

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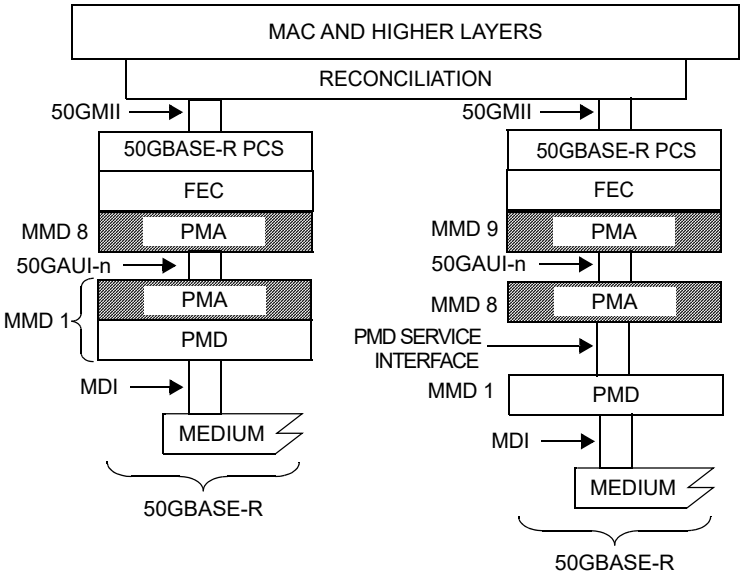
Figure 135A–3 depicts an example of a single 50G with the FEC sublayer implemented with the PCS sublayer.



50GAUI-n = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135A–3—Example single 50G, FEC implemented with PCS

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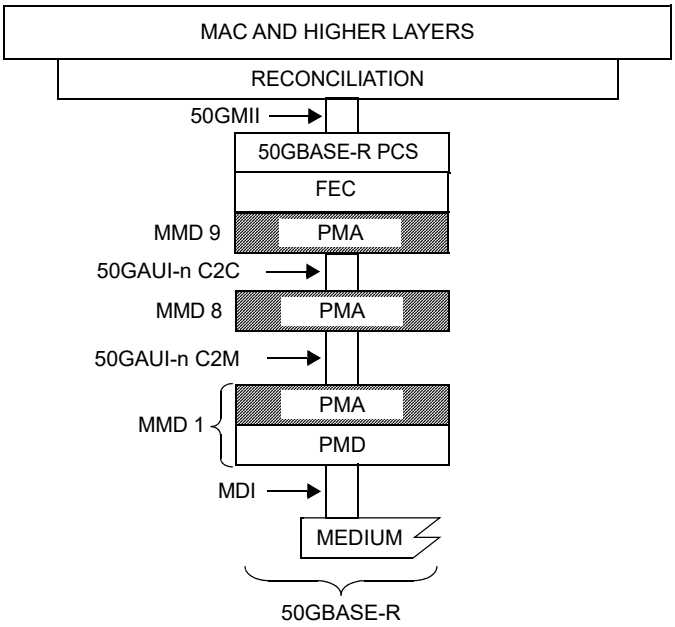
Figure 135A–4 depicts an example of an intermediate PMA device for a module interface with the FEC sublayer implemented with the PCS sublayer.



50GAUI-n = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135A–4—Intermediate PMA device for module interface, FEC implemented with PCS

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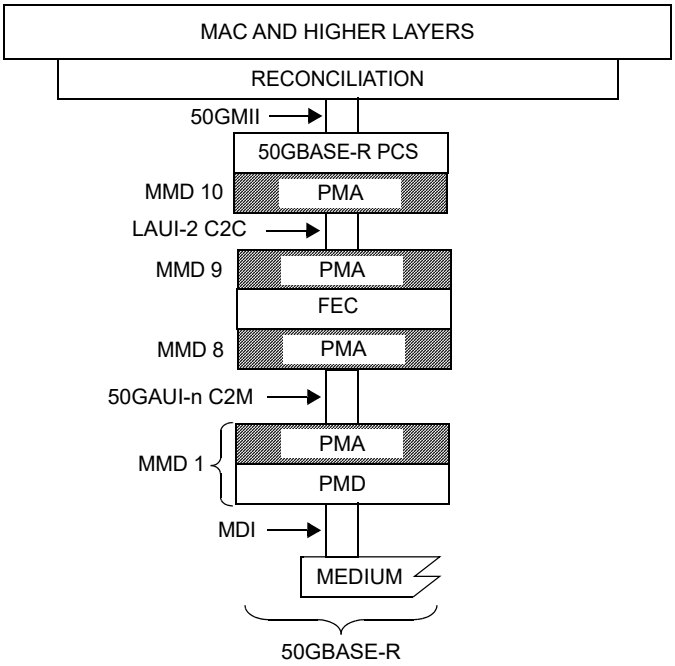
Figure 135A–5 depicts an example of an intermediate PMA device with an FEC sublayer for a module interface.



50GAUI-n = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LAUI-2 = 50 Gb/s ATTACHMENT UNIT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135A–5—Intermediate PMA device with FEC for module interface

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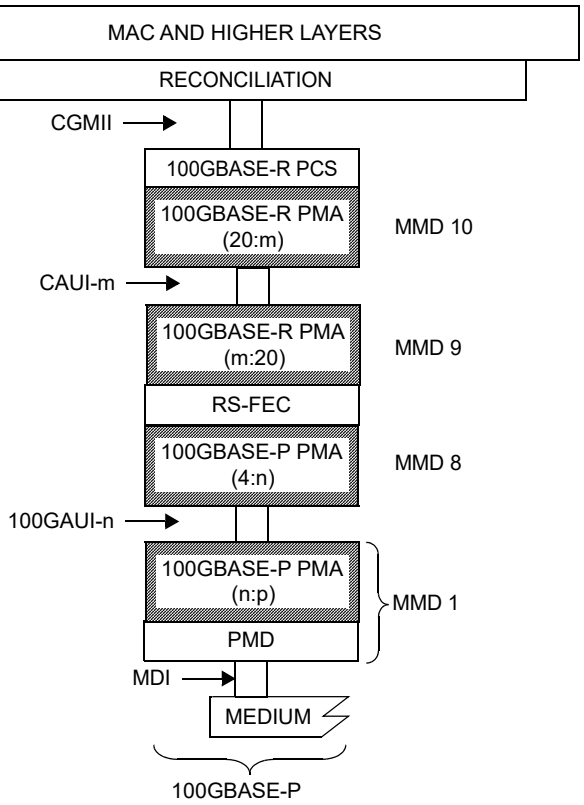
135A.2 Partitioning examples of 100GBASE-P PHYs

Figure 135A–6 depicts an example of a 100GBASE-P PHY with CAUI-n and 100GAUI-n interfaces.



CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
m = 4 or 10
n = 2 or 4
p = 1 or 2

Figure 135A–6—Example 100GBASE-P PHY with CAUI-n and 100GAUI-n

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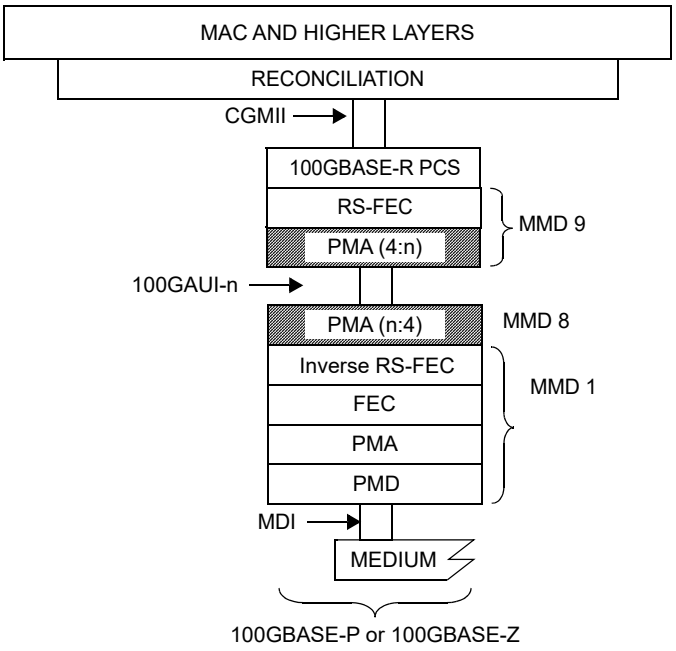
135A.3 Partitioning examples of 100GAUI-n with Inverse RS-FEC

135A.3.1 100GAUI-n with Inverse RS-FEC

Figure 135A–7 depicts an example of a single 100GAUI-n with Inverse RS-FEC.



100GAUI-n = 100 Gb/s n-LANE ATTACHMENT UNIT INTERFACE
CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MMD = MDIO MANAGEABLE DEVICE
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 135A–7—Example single 100GAUI-n with Inverse RS-FEC

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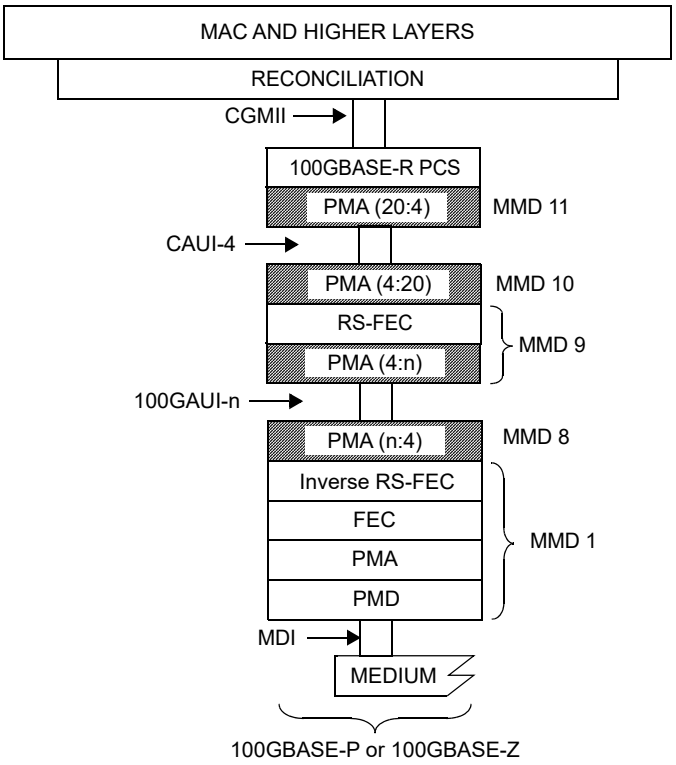
135A.3.2 CAUI-4 chip-to-chip and 100GAUI-n chip-to-module with Inverse RS-FEC

Figure 135A–8 depicts an example of CAUI-4 chip-to-chip and 100GAUI-n chip-to-module interfaces with Inverse RS-FEC.



100GAUI-n = 100 Gb/s n-LANE ATTACHMENT UNIT INTERFACE
CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 135A–8—Example CAUI-4 chip-to-chip and 100GAUI-n chip-to-module with Inverse RS-FEC

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Annex 135B

(normative)

Chip-to-Chip 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2C)

135B.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2C). The LAUI-2 C2C interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.

LAUI-2 C2C is a physical instantiation of the PMA service interface between the PCS and the FEC, as described in 135.1.4. Figure 135B–1 shows an example relationship of the LAUI-2 C2C interface to the ISO/IEC Open System Interconnection (OSI) reference model.

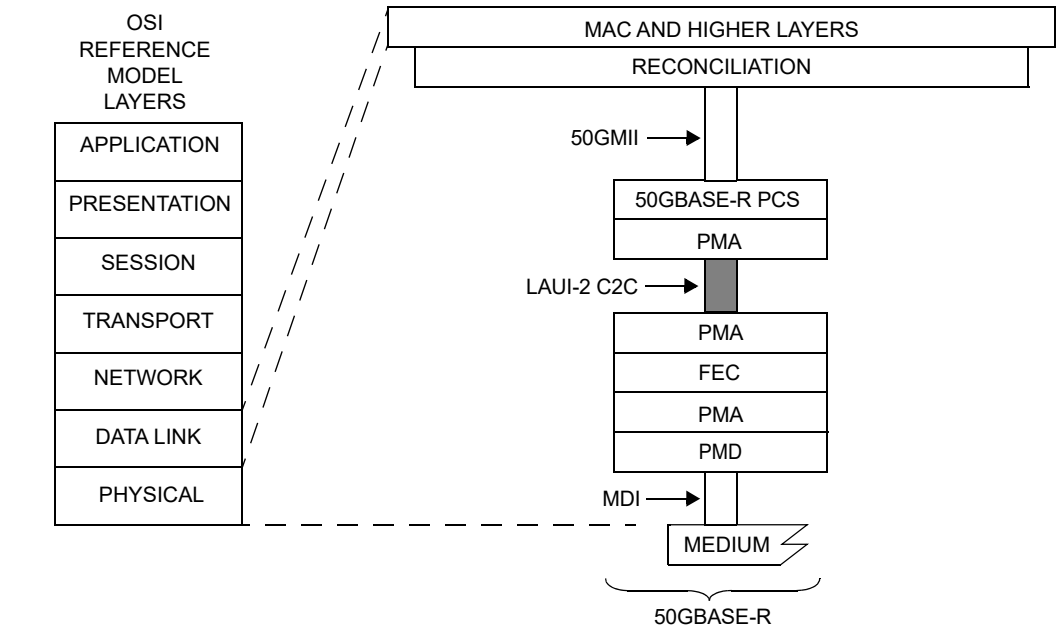

Figure 135B–1—Example LAUI-2 C2C relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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The LAUI-2 C2C bidirectional link is described in terms of a LAUI-2 C2C transmitter, a LAUI-2 C2C channel, and a LAUI-2 C2C receiver. Figure 135B–2 depicts a typical LAUI-2 C2C application.

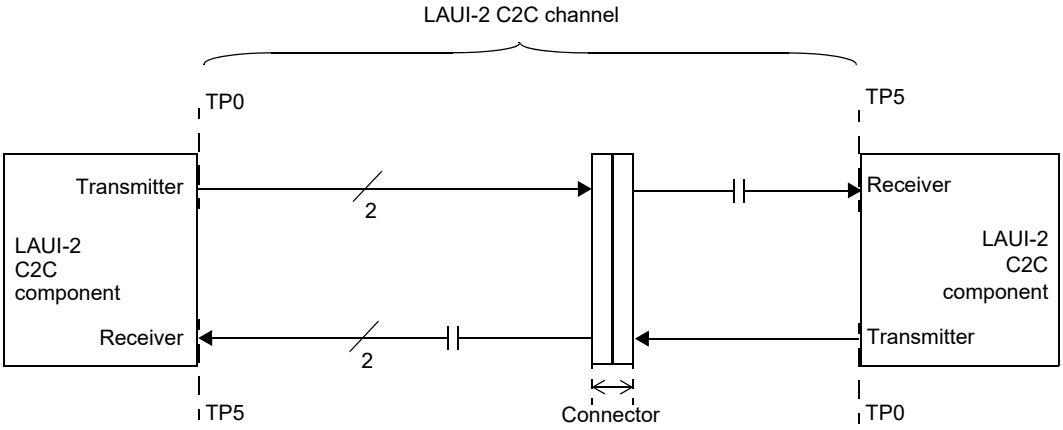

Figure 135B–2—Typical LAUI-2 C2C application

The LAUI-2 C2C interface comprises independent data paths in each direction. Each data path contains two differential lanes, which are AC-coupled. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

LAUI-2 uses NRZ signaling. The nominal signaling rate for each lane is 25.78125 GBd.

The recommended differential insertion loss budget associated with the C2C application can be found in Equation (83D–1) and Figure 83D–3. The normative channel compliance is through LAUI-2 C2C channel operating margin (COM) as described in 83D.4. Actual channel loss could be higher or lower than that given by Equation (83D–1) due to the channel ILD, return loss, and crosstalk.

The LAUI-2 C2C transmitter on each end of the link is adjusted to an appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 83D.3.3.2 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.

135B.2 LAUI-2 C2C compliance point definition

The compliance points for the LAUI-2 C2C interface is defined in 83D.2.

135B.3 LAUI-2 C2C electrical characteristics

135B.3.1 LAUI-2 C2C transmitter characteristics

A LAUI-2 C2C transmitter shall meet all specifications for two CAUI-4 lanes in 83D.3.1.

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135B.3.2 LAUI-2 C2C receiver characteristics

A LAUI-2 C2C receiver shall meet all specifications for two CAUI-4 lanes in 83D.3.3.

If the LAUI-2 C2C receiver supports the optional transmitter equalization feedback, it shall meet all requirements in 83D.3.3.2.

135B.4 LAUI-2 C2C channel characteristics

The LAUI-2 C2C channel shall meet the requirements specified in 83D.4.

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135B.5 Protocol implementation conformance statement (PICS) proforma for Annex 135B, Chip-to-Chip 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2C)[313]

135B.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135B, Chip-to-Chip 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2C), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135B.5.2 Identification

135B.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135B.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 135B, Chip-to-Chip 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2C)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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135B.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135B.1	Two independent data paths in each direction	M	Yes [ ]
*CHAN	Channel	135B.4	Items marked with CHAN include channel specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]

135B.5.4 PICS proforma tables for chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2C)

135B.5.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	135B.3.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TC2	Peak-to-peak differential output voltage	135B.3.1	1200 mV (max)	M	Yes [ ]
TC3	Peak-to-peak differential output voltage, transmitter disabled	135B.3.1	Less than or equal to 30 mV	M	Yes [ ]
TC4	DC common-mode voltage	135B.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC5	AC common-mode output voltage	135B.3.1	12 mV RMS with respect to signal ground	M	Yes [ ]
TC6	Differential output return loss	135B.3.1	Meets Equation (93–3) constraints	M	Yes [ ]
TC7	Common-mode output return loss	135B.3.1	Meets Equation (93–4) constraints	M	Yes [ ]
TC8	Output waveform	135B.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC9	Output jitter	135B.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC10	Transmit equalization	135B.3.1	Each successive step results in a monotonic change	M	Yes [ ]

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135B.5.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	135B.3.2	Meets Equation (93–3) constraints	M	Yes [ ]
RC2	Differential to common-mode input return loss	135B.3.2	Meets Equation (93–5) constraints	M	Yes [ ]
RC3	Interference tolerance	135B.3.2	Satisfy requirements in Table 83D–5	M	Yes [ ]
RC4	Jitter Tolerance	135B.3.2	Satisfy requirements in Table 93–7	M	Yes [ ]

135B.5.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	135B.4	Greater than or equal to 2 dB	CHAN:M	Yes [ ] N/A [ ]

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Annex 135C

(normative)

Chip-to-module 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2M)

135C.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2M). The C2M interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable module interfaces.

LAUI-2 C2M is a physical instantiation of the PMA service interface between the PCS and the FEC, as described in 135.1.4. Figure 135C–1 shows the relationship of the LAUI-2 C2M interface to the ISO/IEC Open System Interconnection (OSI) reference model.

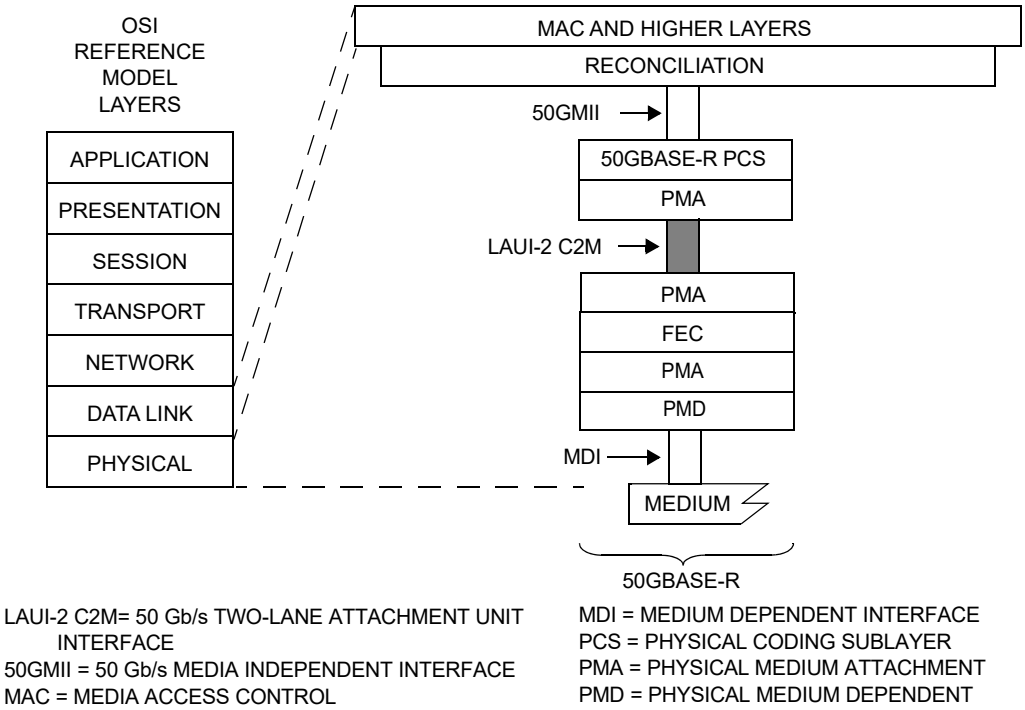

Figure 135C–1—Example LAUI-2 C2M relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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The LAUI-2 C2M link is described in terms of a host LAUI-2 C2M component, a LAUI-2 C2M channel with associated insertion loss, and a module LAUI-2 C2M component. Figure 135C–2 depicts a typical LAUI-2 C2M application and summarizes the differential insertion loss budget associated with the C2M application.

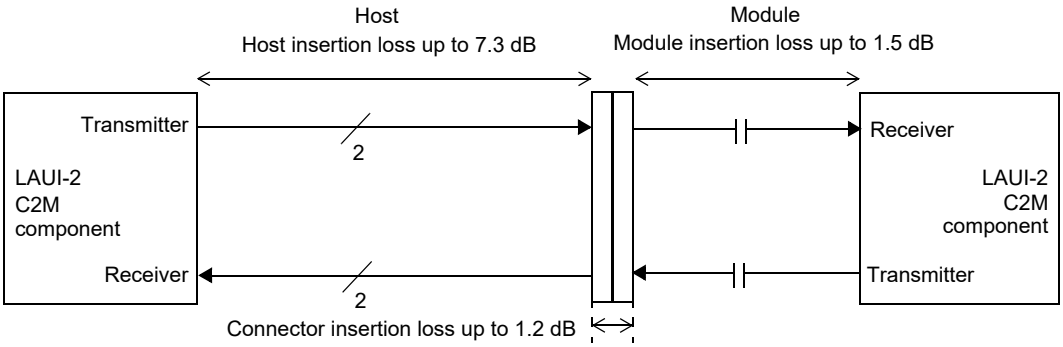

Figure 135C–2—LAUI-2 C2M insertion loss budget at 12.89 GHz

The LAUI-2 C2M interface comprises independent data paths in each direction. Each data path contains two differential lanes, which are AC-coupled within the module.

The LAUI-2 C2M uses NRZ signaling. The nominal signaling rate for each lane is 25.78125 GBd.

The supported insertion loss budget is characterized by Equation (83E–1) and illustrated in Figure 83E–3.

The LAUI-2 C2M interface is defined using a specification and test methodology that is similar to that used for CEI-28G-VSR defined in OIF-CEI-03.1 [B57].

135C.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 10^{-15} with any errors sufficiently uncorrelated to ensure an acceptably high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding.

135C.2 LAUI-2 C2M compliance point definitions

The compliance points for the LAUI-2 C2M interfaces are as defined for two CAUI-4 lanes in 83E.2.

135C.3 LAUI-2 C2M electrical characteristics

135C.3.1 LAUI-2 C2M host output characteristics

A LAUI-2 C2M host output shall meet all specifications for two CAUI-4 lanes in 83E.3.1.

135C.3.2 LAUI-2 C2M module output characteristics

A LAUI-2 C2M module output shall meet all specifications for two CAUI-4 lanes in 83E.3.2.

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135C.3.3 LAUI-2 C2M host input characteristics

A LAUI-2 C2M host input shall meet all specifications for two CAUI-4 lanes in 83E.3.3.

135C.3.4 LAUI-2 C2M module input characteristics

A LAUI-2 C2M module input shall meet all specifications for two CAUI-4 lanes in 83E.3.4.

135C.4 LAUI-2 C2M measurement methodology

The LAUI-2 C2M measurement methodology is as defined in 83E.4.

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135C.5 Protocol implementation conformance statement (PICS) proforma for Annex 135C, Chip-to-module 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2M)[314]

135C.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135C, Chip-to-module 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2M), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135C.5.2 Identification

135C.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135C.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 135C, Chip-to-module 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2M)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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135C.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135C.1	Two independent data paths in each direction	M	Yes [ ]
BER	Meets BER requirement	135C.1.1		M	Yes [ ]
ADR	Adaptive receiver	135C.3.4	Module receiver does not use *Recommended_CTLE_value*	O	Yes [ ] No [ ]

135C.5.4 PICS proforma tables for chip-to-module 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2M)

135C.5.4.1 Host output

Item	Feature	Subclause	Value/Comment	Status	Support
TH1	Signaling rate	135C.3.1	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TH2	Peak-to-peak differential output voltage	135C.3.1	900 mV (max)	M	Yes [ ]
TH3	Peak-to-peak differential output voltage, transmitter disabled	135C.3.1	Less than or equal to 35 mV	M	Yes [ ]
TH4	DC common-mode output voltage	135C.3.1	Between –0.3 V and 2.8 V with respect to signal ground	M	Yes [ ]
TH5	AC common-mode output voltage	135C.3.1	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TH6	Differential output return loss	135C.3.1	Meets Equation (83E–2) constraints	M	Yes [ ]
TH7	Reference impedance for output return loss	135C.3.1	100 Ω.	M	Yes [ ]
TH8	Common to differential mode conversion	135C.3.1	Meets Equation (83E–3) constraints	M	Yes [ ]
TH9	Differential termination mismatch	135C.3.1	Less than 10%	M	Yes [ ]
TH10	Transition time	135C.3.1	Greater than or equal to 10 ps	M	Yes [ ]
TH11	Eye width	135C.3.1	0.46 UI	M	Yes [ ]
TH12	Eye height A	135C.3.1	95 mV	M	Yes [ ]
TH13	Eye height B	135C.3.1	80 mV	M	Yes [ ]
TH14	Crosstalk source	135C.3.1	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 50GBASE-R signal	M	Yes [ ]

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135C.5.4.2 Module output

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Signal rate	135C.3.2	25.78125 GBd ± 100 ppm per lane	M	Yes [ ]
TM2	Peak-to-peak differential output voltage	135C.3.2	900 mV (max)	M	Yes [ ]
TM3	AC common-mode output voltage	135C.3.2	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TM4	Differential output return loss	135C.3.2	Meets Equation (83E–2) constraints	M	Yes [ ]
TM5	Reference impedance for output return loss	135C.3.2	100 Ω.	M	Yes [ ]
TM6	Common to differential mode conversion	135C.3.2	Meets Equation (83E–3) constraints	M	Yes [ ]
TM7	Differential termination mismatch	135C.3.2	Less than 10%	M	Yes [ ]
TM8	Transition time	135C.3.2	Greater than or equal to 12 ps	M	Yes [ ]
TM9	Eye width	135C.3.2	0.57 UI	M	Yes [ ]
TM10	Eye height	135C.3.2	228 mV	M	Yes [ ]
TM11	Crosstalk source	135C.3.2	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 50GBASE-R signal	M	Yes [ ]
TM12	Vertical eye closure	135C.3.2	5.5 dB (max)	M	Yes [ ]

135C.5.4.3 Host input

Item	Feature	Subclause	Value/Comment	Status	Support
RH1	Host input characteristics	135C.3.3	Table 83E–4	M	Yes [ ]

135C.5.4.4 Module input

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Module input characteristics	135C.3.4	Table 83E–7	M	Yes [ ]
RM2	Module stressed input test BER requirement	135C.3.4	As 83E.1.1 with settings associated with *Recommended_CTLE_value*	M	Yes [ ]

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Annex 135D

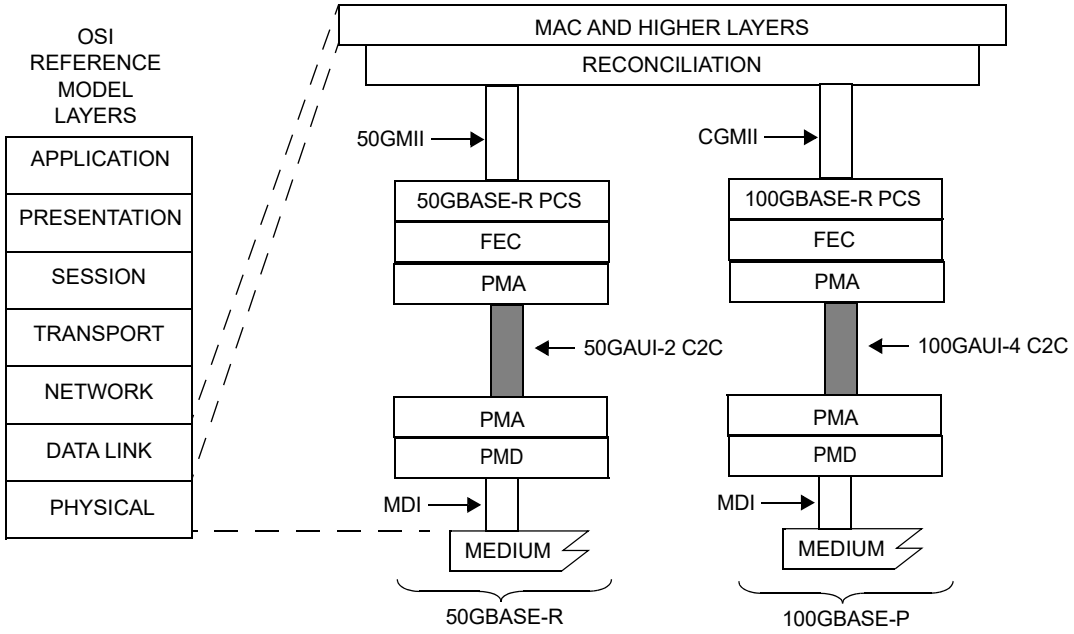
(normative)

Chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2C)

135D.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2C). The 50GAUI-2 C2C and 100GAUI-4 C2C interfaces provide electrical characteristics and associated compliance points, which can optionally be used when designing systems with electrical inter-connect of approximately 25 cm in length.

50GAUI-2 C2C and 100GAUI-4 C2C are physical instantiations of the PMA service interface between the FEC and the PMD, as described in 135.1.4. Figure 135D–1 shows example relationships of the 50GAUI-2 C2C and 100GAUI-4 C2C interfaces to the ISO/IEC Open System Interconnection (OSI) reference model, respectively.



100GAUI-4 C2C= 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
50GAUI-2 C2C = 50 Gb/s TWO-LANE ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135D–1—Example 50GAUI-2 C2C and 100GAUI-4 C2C relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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The 50GAUI-2 C2C bidirectional link is described in terms of a 50GAUI-2 C2C transmitter, a 50GAUI-2 C2C channel, and a 50GAUI-2 C2C receiver. Figure 135D–2 depicts a typical 50GAUI-2 C2C application.

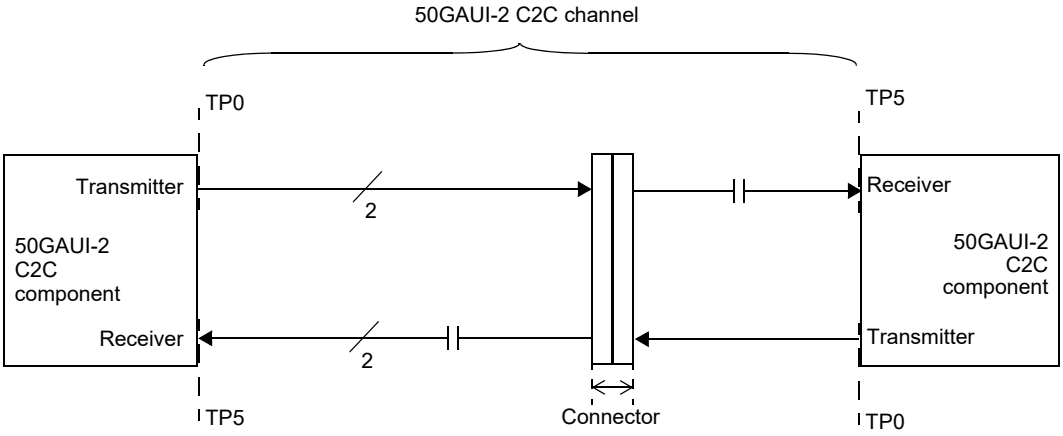

Figure 135D–2—Typical 50GAUI-2 C2C application

The 50GAUI-2 C2C interface comprises independent data paths in each direction. Each data path contains two differential lanes, which are AC-coupled. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

The 100GAUI-4 C2C bidirectional link is described in terms of a 100GAUI-4 C2C transmitter, a 100GAUI-4 C2C channel, and a 100GAUI-4 C2C receiver. Figure 135D–3 depicts a typical 100GAUI-4 C2C application.

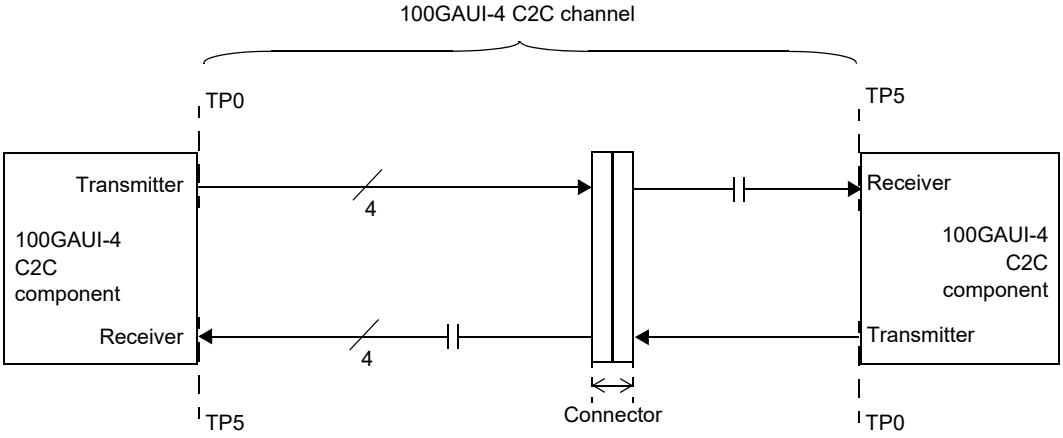

Figure 135D–3—Typical 100GAUI-4 C2C application

The 100GAUI-4 C2C interface comprises independent data paths in each direction. Each data path contains four differential lanes, which are AC-coupled. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

The 50GAUI-2 C2C or 100GAUI-4 C2C use NRZ signaling. The nominal signaling rate for each lane is 26.5625 GBd.

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Equation (83D–1) (illustrated in Figure 83D–3) summarizes the recommended differential insertion loss budget associated with the 50GAUI-2 C2C or 100GAUI-4 C2C application. The normative channel compliance is through 50GAUI-2 C2C or 100GAUI-4 C2C channel operating margin (COM) as described in 83D.4. Actual channel loss could be higher or lower than that given by Equation (83D–1) due to the channel ILD, return loss, and crosstalk.

The 50GAUI-2 C2C or 100GAUI-4C2C transmitter on each end of the link is adjusted to an appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 83D.3.3.2 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.

135D.2 50GAUI-2 C2C and 100GAUI-4 C2C compliance point definition

The compliance points for the 50GAUI-2 C2C and 100GAUI-4 C2C interfaces are as defined in 83D.2.

135D.3 50GAUI-2 C2C and 100GAUI-4 C2C electrical characteristics

135D.3.1 50GAUI-2 C2C and 100GAUI-4 C2C transmitter characteristics

A 50GAUI-2 C2C or a 100GAUI-4 C2C transmitter shall meet all specifications in 120B.3.1.

135D.3.2 50GAUI-2 C2C and 100GAUI-4 C2C receiver characteristics

A 50GAUI-2 C2C or a 100GAUI-4 C2C receiver shall meet all specifications in 120B.3.2.

135D.4 50GAUI-2 C2C and 100GAUI-4 C2C channel characteristics

The 50GAUI-2 C2C or 100GAUI-4 C2C channel shall meet the requirements specified in 120B.4.

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135D.5 Protocol implementation conformance statement (PICS) proforma for Annex 135D, Chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2C)[315]

135D.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135D, Chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2C), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135D.5.2 Identification

135D.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135D.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 135D, Chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2C)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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135D.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135D.1	two independent data paths in each direction for 50GAUI-2 C2C and four independent data paths in each direction for 100GAUI-4 C2C	M	Yes [ ]
*CHAN	Channel	135D.4	Items marked with CHAN include channel specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]

135D.5.4 PICS proforma tables for chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2C)

135D.5.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	135D.3.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TC2	Peak-to-peak differential output voltage	135D.3.1	1200 mV (max)	M	Yes [ ]
TC3	Peak-to-peak differential output voltage, transmitter disabled	135D.3.1	Less than or equal to 30 mV	M	Yes [ ]
TC4	DC common-mode voltage	135D.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC5	AC common-mode output voltage	135D.3.1	12 mV RMS with respect to signal ground	M	Yes [ ]
TC6	Differential output return loss	135D.3.1	Meets Equation (93–3) constraints	M	Yes [ ]
TC7	Common-mode output return loss	135D.3.1	Meets Equation (93–4) constraints	M	Yes [ ]
TC8	Output waveform	135D.3.1	Meets Table 83D–1 constraints	M	Yes [ ]
TC9	Output jitter	135D.3.1	Meets Table 83D–1 constraints with the exceptions in 120B.3.1	M	Yes [ ]
TC10	Transmit equalization	135D.3.1	Each successive step results in a monotonic change	M	Yes [ ]

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135D.5.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	135D.3.2	Meets Equation (93–3) constraints	M	Yes [ ]
RC2	Differential to common-mode input return loss	135D.3.2	Meets Equation (93–5) constraints	M	Yes [ ]
RC3	Interference tolerance	135D.3.2	Satisfy requirements in Table 83D–5with the exceptions in 120B.3.2	M	Yes [ ]

135D.5.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	135D.4	Greater than or equal to 3 dB	CHAN :M	Yes [ ] N/A [ ]

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Annex 135E

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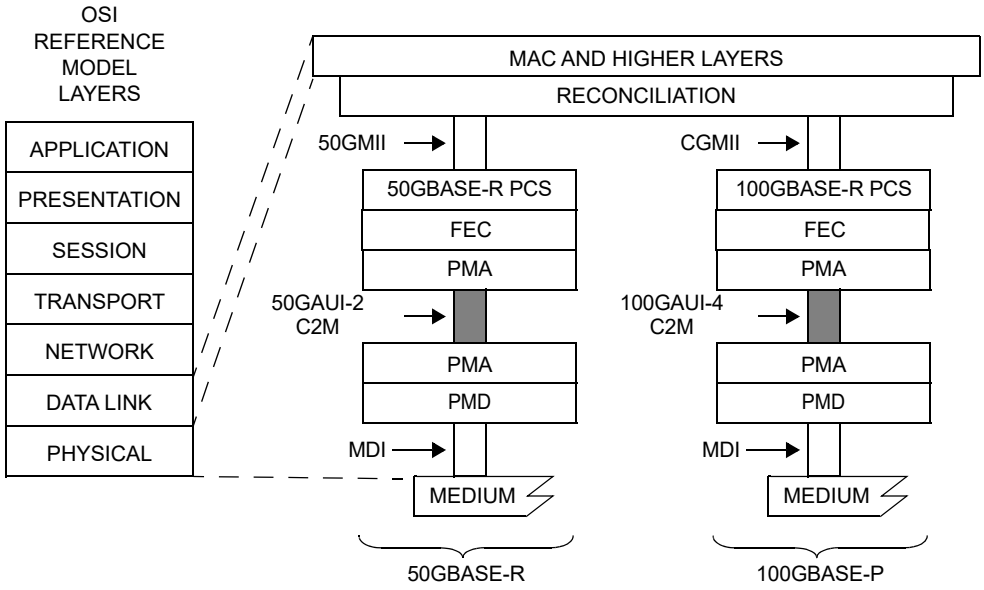
Chip-to-module 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2M)

135E.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2M). The C2M interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable module interfaces.

50GAUI-2 C2M and 100GAUI-4 C2M are physical instantiations of the PMA service interface between the FEC and the PMD, as described in 135.1.4. Figure 135E–1 shows the relationship of the 50GAUI-2 C2M and 100GAUI-4 C2M interfaces to the ISO/IEC Open System Interconnection (OSI) reference model.



100GAUI-4 C2M = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
50GAUI-2 C2M = 50 Gb/s TWO-LANE ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135E–1—Example 50GAUI-2 C2M and 100GAUI-4 C2M relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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The sublayers (including FEC) for each PHY that can optionally include a 50GAUI-2 C2M or 100GAUI-4 C2M are summarized in the tables in 131.1.4 and 80.1.5, respectively, and are specified in the corresponding PMD clause. The positioning of the 50GAUI-2 C2M and 100GAUI-4 C2M relative to other sublayers is shown in Figure 135–2 with further examples in Annex 135A.

The 50GAUI-2 C2M link is described in terms of a host 50GAUI-2 C2M component, a 50GAUI-2 C2M channel with associated insertion loss, and a module 50GAUI-2 C2M component. Figure 135E–2 depicts a typical 50GAUI-2 C2M application and summarizes the differential insertion loss budget associated with the 50GAUI-2 C2M application.

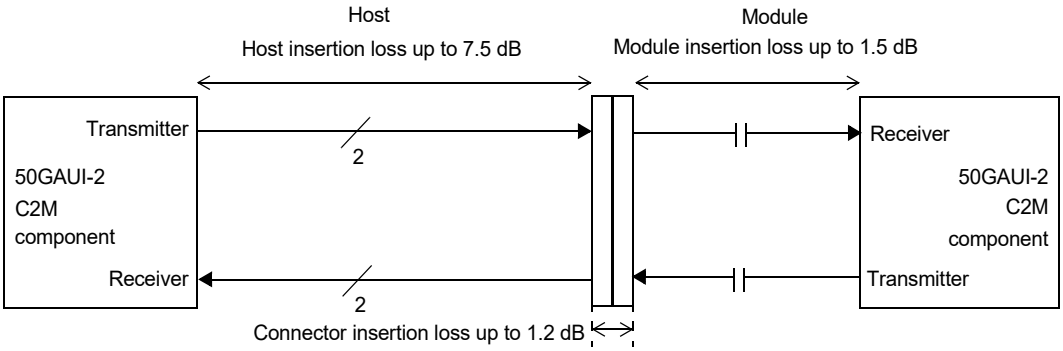

Figure 135E–2—50GAUI-2 C2M insertion loss budget at 13.28 GHz

The 50GAUI-2 C2M interface comprises independent data paths in each direction. Each data path contains two differential lanes, which are AC-coupled within the module.

The 100GAUI-4 C2M link is described in terms of a host 100GAUI-4 C2M component, a 100GAUI-4 C2M channel with associated insertion loss, and a module 100GAUI-4 C2M component. Figure 135E–3 depicts a typical 100GAUI-4 C2M application and summarizes the differential insertion loss budget associated with the C2M application.

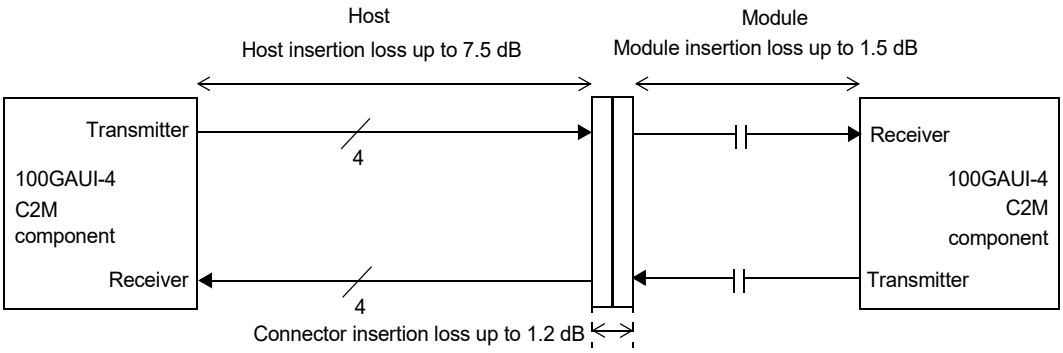

Figure 135E–3—100GAUI-4 C2M insertion loss budget at 13.28 GHz

The 100GAUI-4 C2M interface comprises independent data paths in each direction. Each data path contains four differential lanes, which are AC-coupled within the module.

The 50GAUI-2 C2M and 100GAUI-4 C2M interfaces use NRZ signaling. The nominal signaling rate for each lane is 26.5625 GBd.

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The supported insertion loss budget is characterized by Equation (83E–1) and illustrated in Figure 83E–3.

The 50GAUI-2 C2M and 100GAUI-4 C2M interfaces are defined using a specification and test methodology that is similar to that used for CEI-28G-VSR defined in OIF-CEI-03.1 [B57].

135E.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 10^{-6}.

135E.2 50GAUI-2 C2M and 100GAUI-4 C2M compliance point definitions

The compliance points for the 50GAUI-2 C2M and 100GAUI-4 C2M interfaces are as defined in 83E.2.

135E.3 50GAUI-2 C2M and 100GAUI-4 C2M electrical characteristics

135E.3.1 50GAUI-2 C2M and 100GAUI-4 C2M host output characteristics

A 50GAUI-2 C2M or 100GAUI-4 C2M host output shall meet all specifications in 120C.3.1.

135E.3.2 50GAUI-2 C2M and 100GAUI-4 C2M module output characteristics

A 50GAUI-2 C2M or a 100GAUI-4 C2M module output shall meet all specifications in 120C.3.2.

135E.3.3 50GAUI-2 C2M and 100GAUI-4 C2M host input characteristics

A 50GAUI-2 C2M or a 100GAUI-4 C2M host input shall meet all specifications in 120C.3.3.

135E.3.4 50GAUI-2 C2M and 100GAUI-4 C2M module input characteristics

A 50GAUI-2 C2M or a 100GAUI-4 C2M module input shall meet all specifications in 120C.3.4.

135E.4 50GAUI-2 C2M and 100GAUI-4 C2M measurement methodology

The 50GAUI-2 C2M and 100GAUI-4 C2M measurement methodology is as defined in 120C.4.

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135E.5 Protocol implementation conformance statement (PICS) proforma for Annex 135E, Chip-to-module 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2M)[316]

135E.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135E, Chip-to-module 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2M), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135E.5.2 Identification

135E.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135E.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 135E, Chip-to-module 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2M)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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135E.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135E.1	Two independent data paths in each direction for 50GAUI-2 C2M and four independent data paths in each direction for 100GAUI-4 C2M	M	Yes [ ]
BER	Meets BER requirement	135E.1.1	See 135E.1.1	M	Yes [ ]
ADR	Adaptive receiver	135E.3.4	Module receiver does not use *Recommended_CTLE_value*	O	Yes [ ] No [ ]

135E.5.4 PICS proforma tables for chip-to-module 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2M)

135E.5.4.1 Host output

Item	Feature	Subclause	Value/Comment	Status	Support
TH1	Signaling rate	135E.3.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TH2	Peak-to-peak differential output voltage	135E.3.1	900 mV (max)	M	Yes [ ]
TH3	Peak-to-peak differential output voltage, transmitter disabled	135E.3.1	Less than or equal to 35 mV	M	Yes [ ]
TH4	DC common-mode output voltage	135E.3.1	Between –0.3 V and 2.8 V with respect to signal ground	M	Yes [ ]
TH5	AC common-mode output voltage	135E.3.1	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TH6	Differential output return loss	135E.3.1	Meets Equation (83E–2) constraints	M	Yes [ ]
TH7	Reference impedance for output return loss	135E.3.1	100 Ω.	M	Yes [ ]
TH8	Common to differential mode conversion	135E.3.1	Meets Equation (83E–3) constraints	M	Yes [ ]
TH9	Differential termination mismatch	135E.3.1	Less than 10%	M	Yes [ ]
TH10	Transition time	135E.3.1	Greater than or equal to 10 ps	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TH11	Eye width	135E.3.1	0.46 UI	M	Yes [ ]
TH12	Eye height A	135E.3.1	95 mV	M	Yes [ ]
TH13	Eye height B	135E.3.1	80 mV	M	Yes [ ]
TH14	Crosstalk source	135E.3.1	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 50GBASE-R/100GBASE-R signal	M	Yes [ ]

135E.5.4.2 Module output

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Signal rate	135E.3.2	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TM2	Peak-to-peak differential output voltage	135E.3.2	900 mV (max)	M	Yes [ ]
TM3	AC common-mode output voltage	135E.3.2	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TM4	Differential output return loss	135E.3.2	Meets Equation (83E–2) constraints	M	Yes [ ]
TM5	Reference impedance for output return loss	135E.3.2	100 Ω.	M	Yes [ ]
TM6	Common to differential mode conversion	135E.3.2	Meets Equation (83E–3) constraints	M	Yes [ ]
TM7	Differential termination mismatch	135E.3.2	Less than 10%	M	Yes [ ]
TM8	Transition time	135E.3.2	Greater than or equal to 12 ps	M	Yes [ ]
TM9	Eye width	135E.3.2	0.57 UI	M	Yes [ ]
TM10	Eye height	135E.3.2	228 mV	M	Yes [ ]
TM11	Crosstalk source	135E.3.2	Asynchronous crosstalk source using Pattern 5, Pattern 3, or valid 50GBASE-R/100GBASE-R signal	M	Yes [ ]
TM12	Vertical eye closure	135E.3.2	5.5 dB (max)	M	Yes [ ]

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135E.5.4.3 Host input

Item	Feature	Subclause	Value/Comment	Status	Support
RH1	Host input characteristics	135E.3.3	Table 83E–4 with the exceptions in 120C.3.3	M	Yes [ ]

135E.5.4.4 Module input

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Module input characteristics	135E.3.4	Table 83E–7 with the exceptions in 120C.3.4	M	Yes [ ]
RM2	Module stressed input test BER requirement	135E.3.4	Meet BER requirement of 135E.1.1 with three values of *Recommended_CTLE_value*	M	Yes [ ]

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Annex 135F

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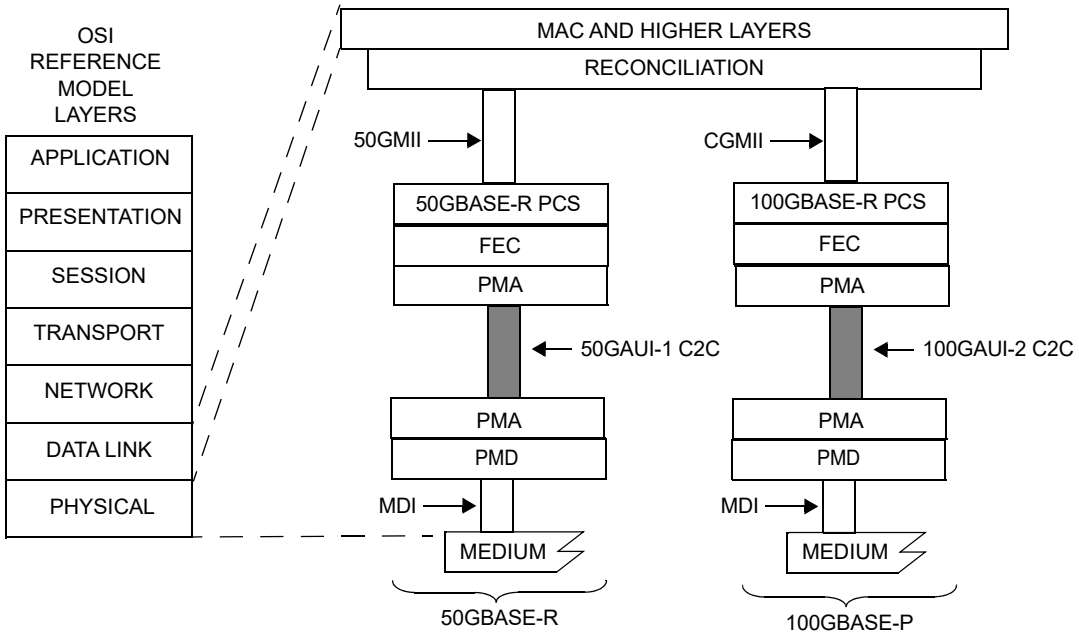
Chip-to-chip 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2C)

135F.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2C). The 50GAUI-1 C2C and 100GAUI-2 C2C interfaces provide electrical characteristics and associated compliance points, which can optionally be used when designing systems with electrical inter-connect of approximately 25 cm in length.

50GAUI-1 C2C and 100GAUI-2 C2C are physical instantiations of the PMA service interface between the FEC and the PMD, as described in 135.1.4. Figure 135F–1 shows example relationships of the 50GAUI-1 C2C and 100GAUI-2 C2C interfaces to the ISO/IEC Open System Interconnection (OSI) reference model, respectively.



100GAUI-2 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
50GAUI-1 = 50 Gb/s ONE-LANE ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135F–1—Example 50GAUI-1 C2C and 100GAUI-2 C2C relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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The 50GAUI-1 C2C bidirectional link is described in terms of a 50GAUI-1 C2C transmitter, a 50GAUI-1 C2C channel, and a 50GAUI-1 C2C receiver. Figure 135F–2 depicts a typical 50GAUI-1 C2C application.

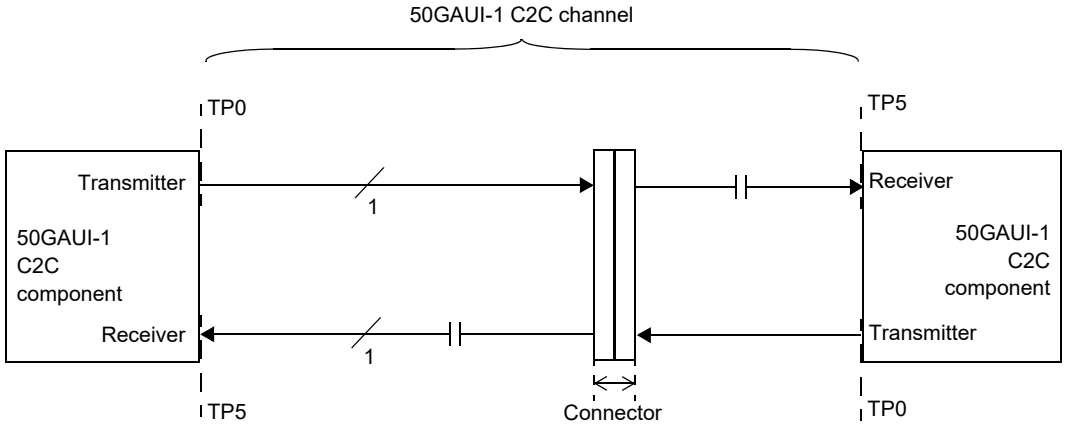

Figure 135F–2—Typical 50GAUI-1 C2C application

The 50GAUI-1 C2C interface comprises independent data paths in each direction. Each data path contains one differential lane, which is AC-coupled. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

The 100GAUI-2 C2C bidirectional link is described in terms of a 100GAUI-2 C2C transmitter, a 100GAUI-2 C2C channel, and a 100GAUI-2 C2C receiver. Figure 135F–3 depicts a typical 100GAUI-2 C2C application.

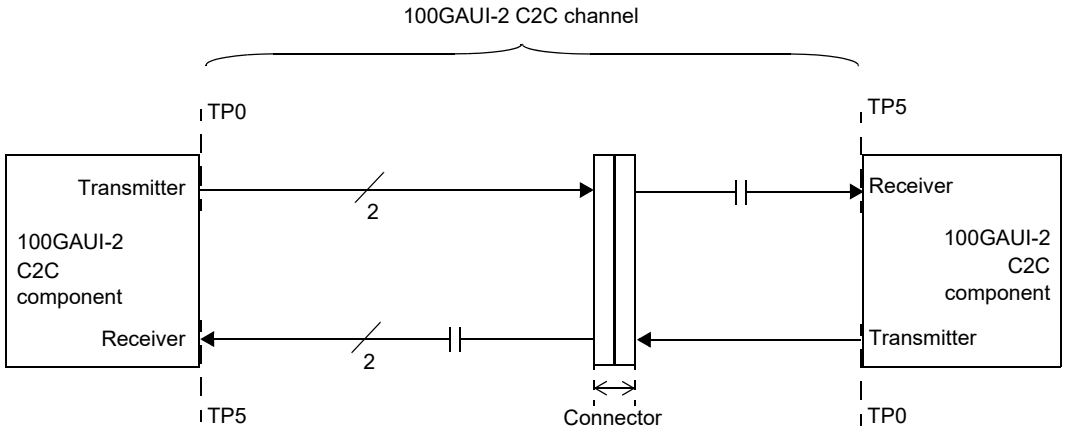

Figure 135F–3—Typical 100GAUI-2 C2C application

The 100GAUI-2 C2C interface comprises independent data paths in each direction. Each data path contains two differential lanes, which are AC-coupled. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.

The 50GAUI-1 C2C and 100GAUI-2 C2C use PAM4 signaling. The nominal signaling rate for each lane is 26.5625 GBd.

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The 50GAUI-2 C2C or 100GAUI-2 C2C channel is specified in 135F.4. The recommended channel insertion loss is described in 120D.1.

The 50GAUI-1 C2C or 100GAUI-2 C2C transmitter on each end of the link is adjusted to an appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 120D.3.2.3 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.

The 50GAUI-1 C2C or 100GAUI-2 C2C transmitter and receiver processing may include precoding as specified in 135F.3.1 and 135F.3.2, respectively. Precoding may be enabled and disabled using the precoder request mechanism specified in 135F.3.2.1.

135F.2 50GAUI-1 C2C and 100GAUI-2 C2C compliance point definition

The compliance points for the 50GAUI-1 C2C and 100GAUI-2 C2C interfaces are as defined in 120D.2.

135F.3 50GAUI-1 C2C and 100GAUI-2 C2C electrical characteristics

135F.3.1 50GAUI-1 C2C and 100GAUI-2 C2C transmitter characteristics

The 50GAUI-1 C2C or 100GAUI-2 C2C transmitter shall support 1/(1+D) mod 4 precoding, as specified in 135.5.7.2, that may be enabled or disabled as required.

A 50GAUI-1 C2C or a 100GAUI-2 C2C transmitter shall meet all specifications in 120D.3.1

135F.3.2 50GAUI-1 C2C and 100GAUI-2 C2C receiver characteristics

The 50GAUI-1 C2C or 100GAUI-2 C2C receiver may optionally support 1/(1+D) mod 4 decoding, as specified in 135.5.7.2, that may be enabled or disabled as required.

A 50GAUI-1 C2C or a 100GAUI-2 C2C receiver shall meet all specifications in 120D.3.2, with precoding enabled on the test transmitter if required by the receiver.

135F.3.2.1 Transmitter precoder request (optional)

The transmitter precoder request is an optional capability for a 50GAUI-1 C2C or 100GAUI-2 C2C receiver. If implemented, it shall operate as described in this subclause.

The transmitter precoder request is generated for each input (Tx and Rx) on each lane. The variables that control the transmitter precoding request are specific for each input and lane.

A 50GAUI-1 C2C or 100GAUI-2 C2C input may generate a request to change the precoder state of the remote output by setting the variable request_precoder_tx_in_flag or request_precoder_rx_in_flag to 1. The variables request_precoder_tx_in_*i* and request_precoder_rx_in_*i* indicate the requested transmitter precoder state for the corresponding interface and lane. A request from a 50GAUI-1 C2C or 100GAUI-2 C2C receiver is generated in an implementation specific manner. An example of a possible precoder update process is provided in 135F.5.

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When a 50GAUI-1 C2C or 100GAUI-2 C2C receiver does not request a change of the remote transmitter's transmit setting, it sets request_precoder_tx_in_flag or request_precoder_rx_in_flag to 0. A 50GAUI-1 C2C or 100GAUI-2 C2C receiver that does not implement transmitter precoder request always sets request_precoder_tx_in_flag or request_precoder_rx_in_flag to 0.

If a Clause 45 MDIO is implemented, the variables request_precoder_rx_in_flag and request_precoder_tx_in_flag are accessible through register 1.604 (see 45.2.1.143), variables request_precoder_rx_in_*i* are accessible through register 1.605 (see 45.2.1.144), and variables request_precoder_tx_in_*i* are accessible through register 1.606 (see 45.2.1.145).

135F.4 50GAUI-1 C2C and 100GAUI-2 C2C channel characteristics

The 50GAUI-1 C2C or 100GAUI-2 C2C channel shall meet the requirements specified in 120D.4.

135F.5 Example usage of the optional transmitter precoder request

135F.5.1 Overview

If implemented, transmitter precoder request from a 50GAUI-1 C2C or 100GAUI-2 C2C receiver may be used to set the precoder configuration for each lane within the link as requested by the receiver. An example of a possible precoder configuration process using the transmitter precoder request is provided in this subclause.

In this example, two components, A and B, are connected by a C2C link, such that A is closest to the PCS and B is closest to the PMD. Clause 45 MDIO is implemented by both components, with component A at device address 11 and component B at device address 10. Transmitter precoder request is implemented by either component A, component B, or both. One Station Management (STA) controls both components.

Figure 135F–4 depicts the components of the C2C link and the registers used during the procedure.

135F.5.2 Configuring precoder setting in the transmit direction

For this example, the following procedure may be used to configure the precoder settings in the transmit direction:

a) For each lane in the link:
   1) Read request_precoder_tx_in_*i* from component B.
   2) Set both precoder_tx_in_enable_*i* of component B and precoder_tx_out_enable_*i* of component A to the read value.
b) If request_precoder_tx_in_flag of component B is 1 then go to step a.
c) Complete.

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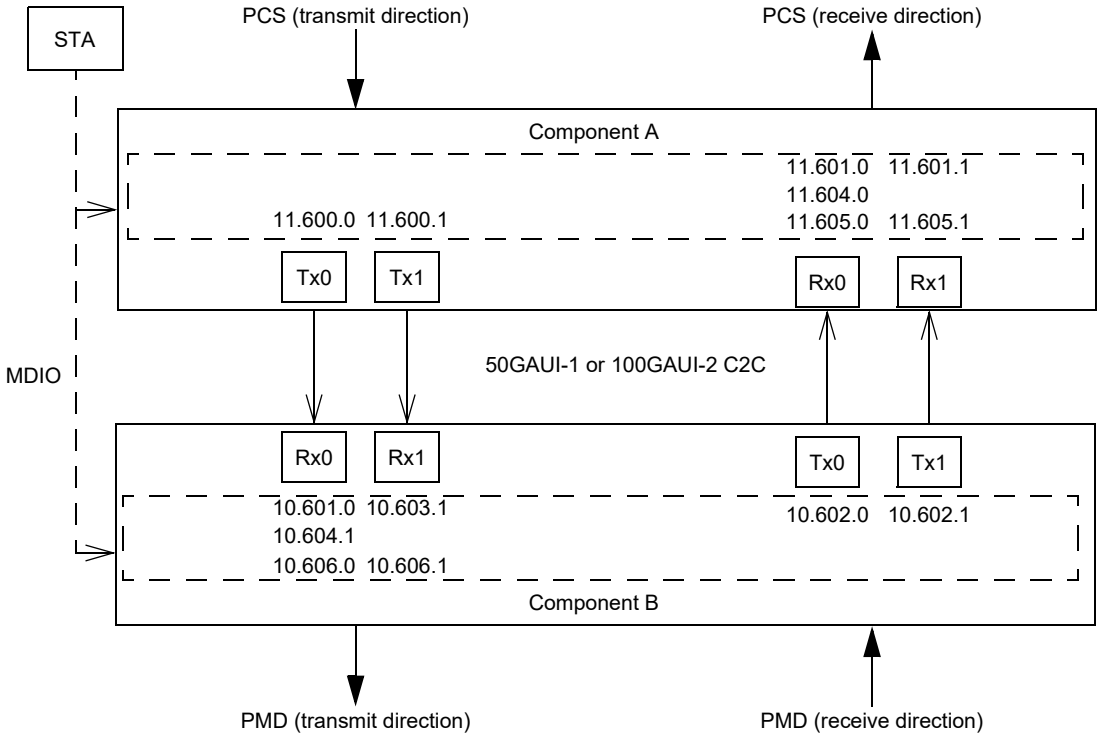

Figure 135F–4—Example transmitter precoder request components and registers

135F.5.3 Configuring precoder setting in the receive direction

For this example, the following procedure may be used to configure the precoder settings in the receive direction:

a) For each lane in the link:
   1) Read request_precoder_rx_in_*i* from component A.
   2) Set both precoder_rx_in_enable_*i* of component A and precoder_rx_out_enable_*i* of component B to the read value.

b) If request_precoder_rx_in_flag of component A is 1 then go to step a.

c) Complete.

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135F.6 Protocol implementation conformance statement (PICS) proforma for Annex 135F, Chip-to-chip 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2C)[317]

135F.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135F, Chip-to-chip 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2C), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135F.6.2 Identification

135F.6.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135F.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 135F, Chip-to-chip 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2C)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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135F.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135F.1	One independent data path in each direction for 50GAUI-1 C2C and two independent data paths in each direction for 100GAUI-2 C2C	M	Yes [ ]
*CHAN	Channel	135F.4	Items marked with CHAN include channel specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TPR	Transmitter precoder request	135F.3.2.1		O	Yes [ ] No [ ]

135F.6.4 PICS proforma tables for chip-to-chip 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2C)

135F.6.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	135F.3.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TC2	Peak-to-peak differential output voltage	135F.3.1	1200 mV (max)	M	Yes [ ]
TC3	Peak-to-peak differential output voltage, transmitter disabled	135F.3.1	Less than or equal to 30 mV	M	Yes [ ]
TC4	DC common-mode voltage	135F.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes [ ]
TC5	AC common-mode output voltage	135F.3.1	30 mV RMS with respect to signal ground	M	Yes [ ]
TC6	Differential output return loss	135F.3.1	Meets Equation (120D–2) constraints	M	Yes [ ]
TC7	Common-mode output return loss	135F.3.1	Meets Equation (93–4) constraints	M	Yes [ ]
TC8	Output waveform	135F.3.1	Meets Table 120D–1 constraints	M	Yes [ ]
TC9	Output jitter	135F.3.1	Meets Table 120D–1 constraints	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TC10	Transmit equalization	135F.3.1	Each successive step results in a monotonic change	M	Yes [ ]
TC11	Transmitter Output residual ISI	135F.3.1	Meets Table 120D–1 constraints	M	Yes [ ]
TC12	Signal-to-noise-and-distortion ratio	135F.3.1	Meets Table 120D–1 constraints	M	Yes [ ]

135F.6.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	135F.3.2	Meets Equation (120D–2) constraints	M	Yes [ ]
RC2	Differential to common-mode input return loss	135F.3.2	Meets Equation (93–5) constraints	M	Yes [ ]
RC3	Interference tolerance	135F.3.2	Satisfy requirements in Table 120D–6	M	Yes [ ]
RC4	Jitter tolerance	135F.3.2	Satisfy requirements in Table 120D–7	M	Yes [ ]

135F.6.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	135F.4	Greater than or equal to 3 dB	CHAN:M	Yes [ ] N/A [ ]
CC2	Return loss for channels with COM less than or equal to 4 dB	135F.4	Meets Equation (120D–12) constraints	CHAN:M	Yes [ ] N/A [ ]

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Annex 135G

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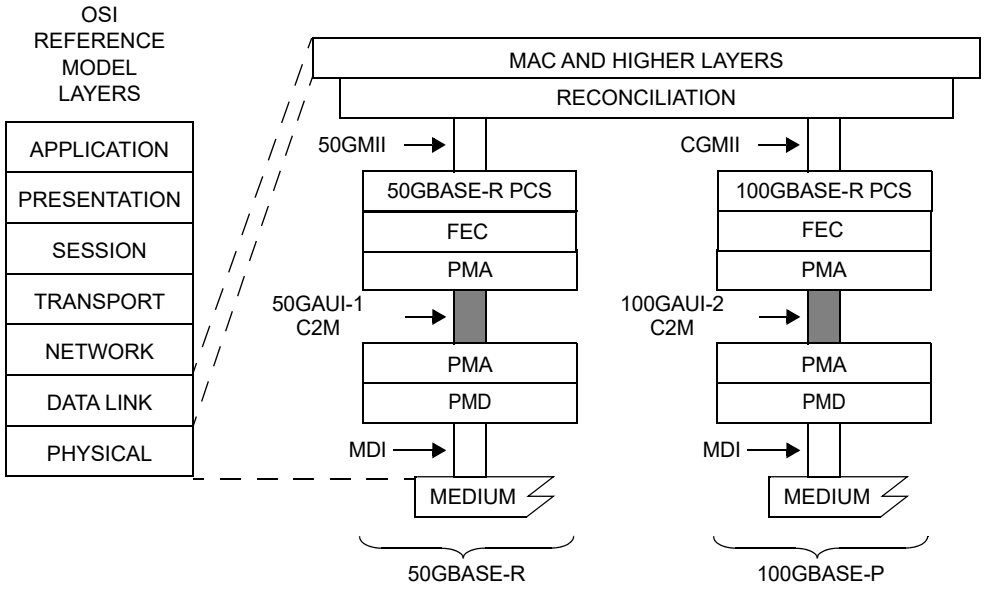
Chip-to-module 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2M)

135G.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-module 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2M). The 50GAUI-1 C2M and 100GAUI-2 C2M interfaces provide electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable module interfaces.

50GAUI-1 C2M and 100GAUI-2 C2M are physical instantiations of the PMA service interface between the FEC and the PMD, as described in 135.1.4. Figure 135G–1 shows the relationship of the 50GAUI-1 C2M and 100GAUI-2 C2M interfaces to the ISO/IEC Open System Interconnection (OSI) reference model.



100GAUI-2 C2M = 100 Gb/s TWO-LANE ATTACHMENT UNIT INTERFACE
50GAUI-1 C2M = 50 Gb/s ONE-LANE ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 135G–1—Example 50GAUI-1 C2M and 100GAUI-2 C2M relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

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The sublayers (including FEC) for each PHY that can optionally include a 50GAUI-1 C2M or 100GAUI-2 C2M are summarized in the tables in 131.1.4 and 80.1.5, respectively, and are specified in the corresponding PMD clause. The positioning of the 50GAUI-1 C2M and 100GAUI-2 C2M relative to other sublayers is shown in Figure 135–2 with further examples in Annex 135A.

The 50GAUI-1 C2M link is described in terms of a host 50GAUI-1 C2M component, a 50GAUI-1 C2M channel with associated insertion loss, and a module 50GAUI-1 C2M component. Figure 135G–2 depicts a typical 50GAUI-1 C2M application and summarizes the differential insertion loss budget associated with the 50GAUI-1 C2M application.

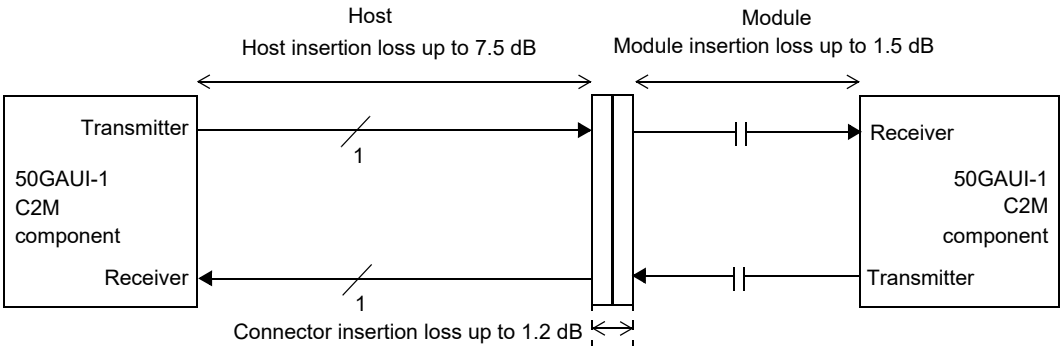

Figure 135G–2—50GAUI-1 C2M insertion loss budget at 13.28 GHz

The 50GAUI-1 C2M interface comprises independent data paths in each direction. The data path contains one differential lane, which is AC-coupled within the module.

The 100GAUI-2 C2M link is described in terms of a host 100GAUI-2 C2M component, a 100GAUI-2 C2M channel with associated insertion loss, and a module 100GAUI-2 C2M component. Figure 135G–3 depicts a typical 100GAUI-2 C2M application and summarizes the differential insertion loss budget associated with the 100GAUI-2 C2M application.

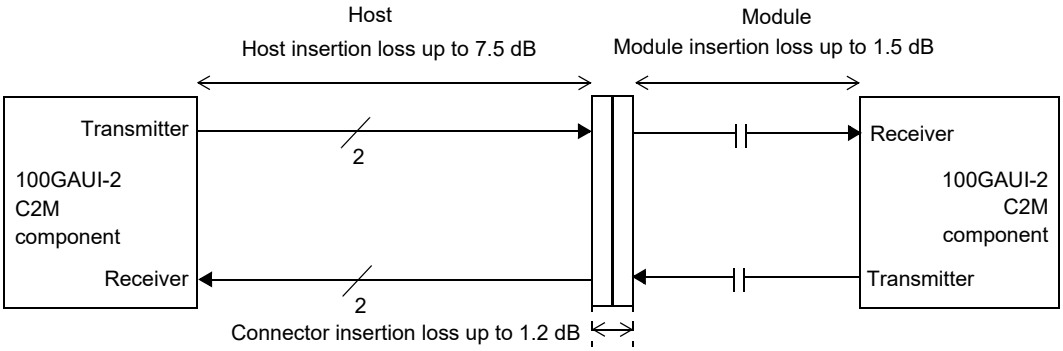

Figure 135G–3—100GAUI-2 C2M insertion loss budget at 13.28 GHz

The 100GAUI-2 C2M interface comprises independent data paths in each direction. Each data path contains two differential lanes, which are AC-coupled within the module.

The 50GAUI-1 C2M and 100GAUI-2 C2M interfaces use PAM4 signaling. The nominal signaling rate for each lane is 26.5625 GBd.

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The supported insertion loss budget is characterized by Equation (120E–1) and illustrated in Figure 120E–4.

The 50GAUI-1 C2M and 100GAUI-2 C2M interfaces are defined using a specification and test methodology that is similar to that used for CEI-56G-VSR defined in OIF-CEI-4.0 [B58].

135G.1.1 Bit error ratio

The bit error ratio (BER) when processed according to Clause 135 shall be less than 10^{-5}.

135G.2 50GAUI-1 C2M and 100GAUI-2 C2M compliance point definitions

The compliance points for the 50GAUI-1 C2M and 100GAUI-2 C2M interfaces are as defined in 120E.2.

135G.3 50GAUI-1 C2M and 100GAUI-2 C2M electrical characteristics

135G.3.1 50GAUI-1 C2M and 100GAUI-2 C2M host output characteristics

A 50GAUI-1 C2M or 100GAUI-2 C2M host output shall meet all specifications in 120E.3.1.

135G.3.2 50GAUI-1 C2M and 100GAUI-2 C2M module output characteristics

A 50GAUI-1 C2M or a 100GAUI-2 C2M module output shall meet all specifications in 120E.3.2.

135G.3.3 50GAUI-1 C2M and 100GAUI-2 C2M host input characteristics

A 50GAUI-1 C2M or a 100GAUI-2 C2M host input shall meet all specifications in 120E.3.3.

135G.3.4 50GAUI-1 C2M and 100GAUI-2 C2M module input characteristics

A 50GAUI-1 C2M or a 100GAUI-2 C2M module input shall meet all specifications in 120E.3.4.

135G.4 50GAUI-1 C2M and 100GAUI-2 C2M measurement methodology

The 50GAUI-1 C2M and 100GAUI-2 C2M measurement methodology is as defined in 120E.4.

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135G.5 Protocol implementation conformance statement (PICS) proforma for Annex 135G, Chip-to-module 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2M)[318]

135G.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135G, Chip-to-module 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2M), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

135G.5.2 Identification

135G.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

135G.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 135G, Chip-to-module 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2M)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[318]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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135G.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135G.1	One independent data path in each direction for 50GAUI-1 C2M and two independent data paths in each direction for 100GAUI-2 C2M	M	Yes [ ]
BER	Meets BER requirement	135G.1.1		M	Yes [ ]
ADE	Adaptive Equalizer	135G.3.4		M	Yes [ ]

135G.5.4 PICS proforma tables for chip-to-module 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2M)

135G.5.4.1 Host output

Item	Feature	Subclause	Value/Comment	Status	Support
TH1	Signaling rate	135G.3.1	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TH2	DC common-mode output voltage	135G.3.1	Between –0.3 V and 2.8 V with respect to signal ground	M	Yes [ ]
TH3	Peak-to-peak differential output voltage, transmitter disabled	135G.3.1	Less than or equal to 35 mV	M	Yes [ ]
TH4	Peak-to-peak differential output voltage	135G.3.1	880 mV (max)	M	Yes [ ]
TH5	AC common-mode output voltage	135G.3.1	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TH6	Eye width, all 3 eyes	135G.3.1	0.22 UI	M	Yes [ ]
TH7	Eye height, all 3 eyes	135G.3.1	32 mV	M	Yes [ ]
TH8	Differential output return loss	135G.3.1	Meets Equation (83E–2) constraints	M	Yes [ ]
TH9	Common to differential mode conversion	135G.3.1	Meets Equation (83E–3) constraints	M	Yes [ ]
TH10	Differential termination mismatch	135G.3.1	Less than 10%	M	Yes [ ]
TH11	Transition time	135G.3.1	Greater than or equal to 10 ps	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TH12	Reference impedance for output return loss	135G.3.1	100 Ω.	M	Yes [ ]
TH13	Crosstalk source	135G.3.1	Asynchronous crosstalk source using PRBS13Q or PRBS31Q pattern, or valid 50GBASE-R / 100GBASE-R signal	M	Yes [ ]
TH14	Vertical eye closure	135G.3.1	Less than 12 dB	M	Yes [ ]

135G.5.4.2 Module output

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Signal rate	135G.3.2	26.5625 GBd ± 100 ppm per lane	M	Yes [ ]
TM2	AC common-mode output voltage	135G.3.2	17.5 mV RMS with respect to signal ground	M	Yes [ ]
TM3	Peak-to-peak differential output voltage	135G.3.2	900 mV (max)	M	Yes [ ]
TM4	Near-end eye width, all 3 eyes	135G.3.2	0.265 UI	M	Yes [ ]
TM5	Near-end eye height, all 3 eyes	135G.3.2	70 mV	M	Yes [ ]
TM6	Far-end eye width, all 3 eyes	135G.3.2	0.2 UI	M	Yes [ ]
TM7	Far-end eye height, all 3 eyes	135G.3.2	30 mV	M	Yes [ ]
TM8	Far-end pre-cursor ISI ratio (max)	135G.3.2	–4.5% to +2.5%	M	Yes [ ]
TM9	Differential output return loss	135G.3.2	Meets Equation (83E–2) constraints	M	Yes [ ]
TM10	Common to differential mode conversion	135G.3.2	Meets Equation (83E–3) constraints	M	Yes [ ]
TM11	Differential termination mismatch	135G.3.2	Less than 10%	M	Yes [ ]
TM12	Transition time	135G.3.2	Greater than or equal to 9.5 ps	M	Yes [ ]
TM13	Reference impedance for output return loss	135G.3.2	100 Ω.	M	Yes [ ]
TM14	Crosstalk source	135G.3.2	Asynchronous crosstalk source using PRBS13Q or PRBS31Q pattern, or valid 50GBASE-R / 100GBASE-R signal	M	Yes [ ]

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135G.5.4.3 Host input

Item	Feature	Subclause	Value/Comment	Status	Support
RH1	Host input characteristics	135G.3.3	Table 120E–4	M	Yes [ ]

135G.5.4.4 Module input

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Module input characteristics	135G.3.4	Table 120E–7	M	Yes [ ]

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Annex 136A

(informative)

TP0 and TP5 test point parameters and channel characteristics for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136A.1 Overview

Annex 136A provides information on parameters associated with test points TP0 and TP5 that might not be testable in an implemented system. TP0 and TP5 test points are illustrated in the 50GBASE-CR, 100GBASE-CR2 and 200GBASE-CR4 link block diagram of Figure 136–2. This annex also provides information on channel characteristics.

136A.2 Transmitter characteristics at TP0

The recommended transmitter characteristics at TP0 as measured at TP0a are described in 137.9.2.

136A.3 Receiver characteristics at TP5

The recommended receiver characteristics at TP5 as measured at TP5a are described in 137.9.3.

136A.4 Transmitter and receiver differential printed circuit board trace loss

The recommended maximum and minimum printed circuit board trace insertion losses are specified in Equation (92A–1) and Equation (92A–2), respectively.

Note that the recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is 7 dB at 13.28 GHz and the recommended minimum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is 1.2 dB at 13.28 GHz. The recommended maximum insertion loss allocation for the transmitter or receiver differential controlled impedance printed circuit boards is consistent with the insertion loss TP0 to TP2 or TP3 to TP5 given in Equation (136–5) and an assumed mated connector loss of 1.69 dB.

Note that the recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 is 10.07 dB at 13.28 GHz.

136A.5 Channel insertion loss

This subclause provides information on channel insertion losses for the maximum-loss and minimum-loss cabling topologies.

The maximum channel insertion loss associated with the cable assembly is determined using Equation (136A–1). The channel insertion loss budget at 13.28 GHz is illustrated in Figure 136A–1. Loss budget parameters for all cable topologies are provided in Table 136A–1.

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$$IL_{Chmax}(f) = IL_{Camax}(f) + 2IL_{Host}(f) - 2IL_{MatedTF}(f) \quad \text{(dB)} \quad \text{(136A–1)}$$

for 0.05 GHz ≤ f ≤ 19 GHz

where

f	is the frequency in GHz
$IL_{Chmax}(f)$	is the maximum channel insertion loss between TP0 and TP5
$IL_{Camax}(f)$	is the maximum cable assembly insertion loss (TP1 to TP4)
$IL_{Host}(f)$	is the maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (136–5)
$IL_{MatedTF}(f)$	is the reference insertion loss of the mated test fixture using Equation (136B–1).

The channel insertion loss associated with the 0.5 m cable assembly and a maximum host channel is determined by Equation (136A–2).

$$IL_{Ch0.5m}(f) = IL_{Camin}(f) + 2IL_{Host}(f) - 2IL_{MatedTF}(f) \quad \text{(dB)} \quad \text{(136A–2)}$$

for 0.05 GHz ≤ f ≤ 19 GHz

where

f	is the frequency in GHz
$IL_{Ch0.5m}(f)$	is the channel insertion loss between TP0 and TP5 representative of a 0.5 m cable assembly and a maximum host channel
$IL_{Camin}(f)$	is the minimum cable assembly insertion loss (TP1 to TP4) given in Equation (92–26) and illustrated in Figure 92–12
$IL_{Host}(f)$	is the maximum insertion loss from TP0 to TP2 or TP3 to TP5 using Equation (136–5)
$IL_{MatedTF}(f)$	is the reference insertion loss of the mated test fixture using Equation (136B–1).

The loss budget parameter values at 13.28 GHz are provided in Table 136A–1.

Table 136A–1—Insertion loss budget values at 13.28 GHz

Parameter	50GBASE-CR	100GBASE-CR2	200GBASE-CR4	Units
IL_{Chmax}	30			dB
IL_{Camax}	17.16			dB
$IL_{Ch0.5m}$	21.14			dB
IL_{Camin}	8.3			dB
IL_{Host}	10.07			dB
$IL_{MatedTF}$	3.65			dB

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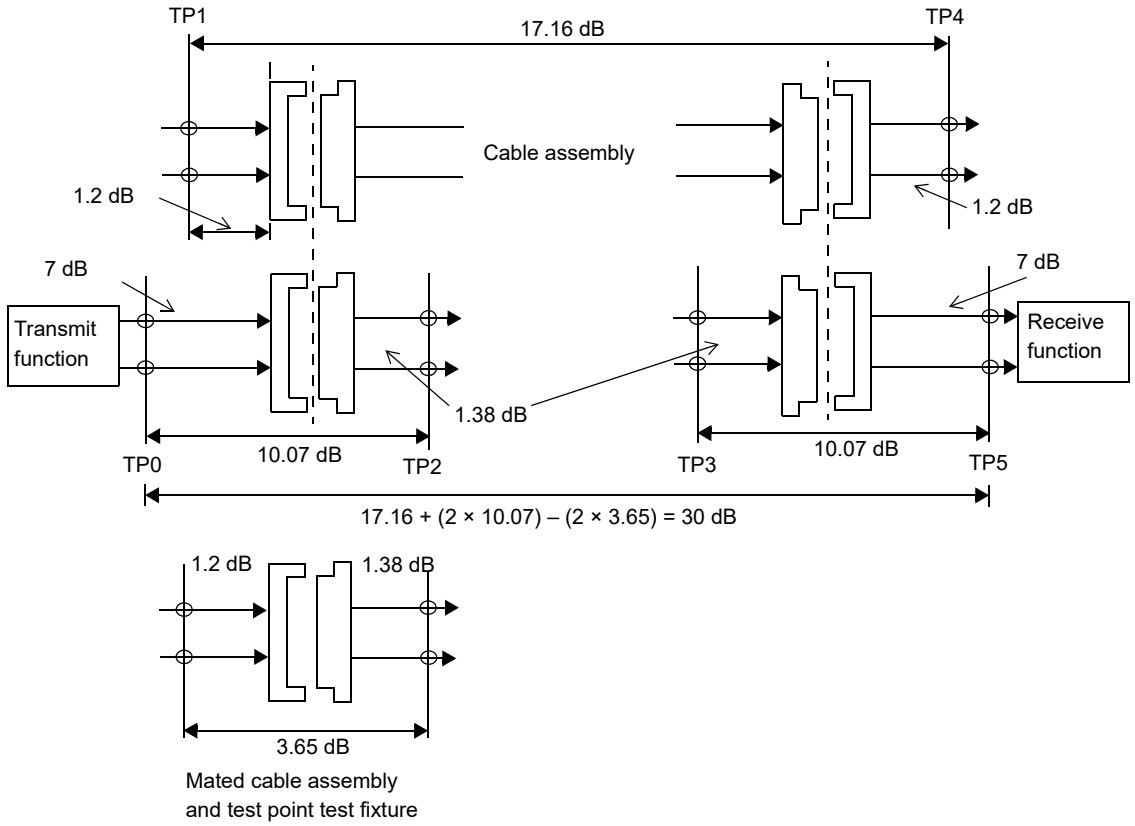

NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Figure 136A–1—30 dB channel insertion loss budget at 13.28 GHz

136A.6 Channel effective return loss

The 50GBASE-CR, 100GBASE-CR2 and 200GBASE-CR4 channels are recommended to meet the effective return loss specified in 137.10.2.

136A.7 Channel Operating Margin (COM)

The Channel Operating Margin (COM) for the channel between TP0 and TP5, computed using the procedure in 93A.1 and the parameters in Table 137–6, is recommended to be greater than or equal to 3 dB.

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Annex 136B

(normative)

Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M

136B.1 Test fixtures

Transmitter and receiver measurements at TP2 or TP3 for the 50GBASE-CR PHY in an SFP28 host form factor (see 136D.2.1), and at TP1a or TP4a for the 50GAUI-1 C2M host (see Annex 135G), are made utilizing the test fixture specified in 110B.1.1. Transmitter and receiver measurements at TP2 or TP3 for the 50GBASE-CR, 100GBASE-CR2 or 200GBASE-CR4 PHYs in a multi-lane host form factor (see 136D.2.2), and at TP1a or TP4a for the 100GAUI-2 C2M host (see Annex 135G), are made utilizing the test fixture specified in 136B.1.1.

Cable assembly measurements for the SFP28-SFP28 form factor (see 136D.3.1) are made between TP1 and TP4 with cable assembly test fixtures as specified in 110B.1.2. on both ends. Cable assembly measurements for the multi-lane form factors (see 136D.3.1) are made between TP1 and TP4 with cable assembly test fixtures as specified in 136B.1.1 on both ends. Cable assembly measurements for the multi-lane-SFP28 form factor (see 136D.3.3) are made between TP1 and TP4 with a cable assembly test fixture as specified in 110B.1.2. for each connector on the SFP28 end, and with a cable assembly test fixture as specified in 136B.1.1 for the multi-lane end.

The test fixtures are specified in a mated state to enable connections to measurement equipment. The reference insertion loss of the mated test fixtures is 3.65 dB at 13.28 GHz using Equation (136B–1). The requirements in the referenced subclauses are not the MDI connector specifications for an implemented design.

136B.1.1 Mated test fixtures

The TP2 or TP3 and cable assembly test fixtures are specified in a mated state illustrated in Figure 92–18. The mated test fixtures specifications are listed in 92.11.3 and using the multi-lane integrated crosstalk noise in 136B.1.1.6.

136B.1.1.1 Mated test fixtures differential insertion loss

The differential insertion loss of the mated test fixtures shall meet the requirements of 92.11.3.1.

The FOM_{ILD} of the mated test fixtures shall meet the requirements of 92.11.3.1.

The reference insertion loss of the mated test fixture is determined using Equation (136B–1).

$$IL_{\mathrm{MatedTF}}(f) = 0.471\sqrt{f} + 0.1194f + 0.002f^2 \ \text{(dB)} \qquad \text{(136B–1)}$$

for $0.01\ \text{GHz} \le f \le 25\ \text{GHz}$

where

f is the frequency in GHz

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136B.1.1.2 Mated test fixtures differential return loss

The differential return loss of the mated test fixtures shall meet the requirements of 92.11.3.2.

136B.1.1.3 Mated test fixtures common-mode conversion insertion loss

The common-mode conversion insertion loss of the mated test fixtures shall meet the requirements of 92.11.3.3.

136B.1.1.4 Mated test fixtures common-mode return loss

The common-mode return loss of the mated test fixtures shall meet the requirements of 92.11.3.4.

136B.1.1.5 Mated test fixtures common-mode to differential mode return loss

The common-mode to differential mode return loss of the mated test fixtures shall meet the requirements of 92.11.3.5.

136B.1.1.6 Mated test fixtures integrated crosstalk noise

The SFP28 mated test fixture integrated near-end crosstalk noise voltage for the disturber near-end crosstalk loss is determined according to the method in 110B.1.3.6 using the parameters shown in Table 136B–1 and shall meet the specification in Table 136B–2.

Table 136B–1—SFP28 mated test fixture integrated near-end crosstalk noise parameters

Description	Symbol	Value	Units
Symbol rate	f_b	26.5625	GBd
3 dB reference receiver bandwidth	f_r	19.92	GHz
Near-end disturber peak differential output amplitude	A_{nt}	600	mV
Near-end disturber 20% to 80% rise and fall times	T_{nt}	9.27	ps

Table 136B–2—SFP28 mated test fixture integrated near-end crosstalk noise voltage

Parameter	Value	Units
Integrated near-end crosstalk noise voltage	Less than 1.6	mV

The multi-lane mated test fixtures integrated crosstalk RMS noise voltages determined using Equation (92–44) through Equation (92–48) for the multiple disturber near-end crosstalk loss, and the multiple-disturber far-end crosstalk loss shall meet the specifications in Table 136B–4 using the parameters shown in Table 136B–3.

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Table 136B–3—Multi-lane mated test fixture integrated crosstalk noise parameters

Description	Symbol	Value	Units
Symbol rate	f_b	26.5625	GBd
3 dB reference receiver bandwidth	f_r	19.92	GHz
Near-end disturber peak differential output amplitude	A_{nt}	600	mV
Far-end disturber peak differential output amplitude	A_{ft}	600	mV
Near-end disturber 20% to 80% rise and fall times	T_{nt}	9.27	ps
Far-end disturber 20% to 80% rise and fall times	T_{ft}	9.27	ps

Table 136B–4—Multi-lane mated test fixture integrated crosstalk noise

Parameters	Multi-lane connector types	Units
MDFEXT integrated crosstalk noise voltage	less than 4.2	mV
MDNEXT integrated crosstalk noise voltage	less than 1.5	mV
Total integrated crosstalk noise voltage	less than 4.4	mV

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136B.2 Protocol implementation conformance statement (PICS) proforma for Annex 136B, Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M[319]

136B.2.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 136B, Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

136B.2.2 Identification

136B.2.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

136B.2.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 136B, Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

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136B.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
HTF1	SFP28 TP2 or TP3 test fixture	110B.1.1		O	Yes [ ] No [ ]
HTF2	Multi-lane TP2 or TP3 test fixture	136B.1.1		O	Yes [ ] No [ ]
CATF1	SFP28 Cable assembly test fixture	110B.1.2		O	Yes [ ] No [ ]
CATF2	Multi-lane Cable assembly test fixture	136B.1.1		O	Yes [ ] No [ ]

136B.2.4 PICS proforma tables for test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Mated test fixtures insertion loss	136B.1.1.1	IL and FOM_{ILD} meet the requirements of 92.11.3.1	M	Yes [ ]
TF2	Mated test fixtures differential return loss	136B.1.1.2	Meets the requirements of 92.11.3.2	M	Yes [ ]
TF3	Mated test fixtures common-mode conversion insertion loss	136B.1.1.3	Meets the requirements of 92.11.3.3	M	Yes [ ]
TF4	Mated test fixtures common-mode return loss	136B.1.1.4	Meets the requirements of 92.11.3.4	M	Yes [ ]
TF5	Mated test fixtures common-mode to differential mode return loss	136B.1.1.5	Meets the requirements of 92.11.3.5	M	Yes [ ]
TF6	SFP28 Mated test fixtures integrated near-end crosstalk noise	136B.1.1.6	Less than 1.6 mV	M	Yes [ ]
TF7	Multi-lane mated test fixtures integrated crosstalk noise	136B.1.1.6	Meets the requirements of Table 136B–4	M	Yes [ ]

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Annex 136C

(normative)

MDIs for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136C.1 Overview

This annex defines the Media Dependent Interface (MDI) for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4. The MDI couples the PMD (specified in 136.8 and 136.9) to the cable assembly (specified in 136.11). The PMDs supportable for each MDI connector type are given in Table 136C–1. The QSFP28, microQSFP, QSFP-DD and OSFP are also referred to as multi-lane connectors.

Table 136C–1—Number of PMDs supportable for each connector type

MDI types	50GBASE-CR	100GBASE-CR2	200GBASE-CR4	Reference
SFP28	1	—	—	110.11.1
QSFP28	1, 2, 4	1, 2	1	92.12.1.1
microQSFP	1, 2, 4	1, 2	1	136C.2.3
QSFP-DD	1, 2, 4, 8	1, 2, 4	1, 2	136C.2.4
OSFP	1, 2, 4, 8	1, 2, 4	1, 2	136C.2.5

For 50GBASE-CR, the mechanical interface between the PMD and the cable assembly may be a mated pair of connectors meeting the requirements of 110.11.1 (SFP28), 92.12.1.1 (QSFP), 136C.2.3 (microQSFP), 136C.2.4 (QSFP-DD), or 136C.2.5 (OSFP). The plug connector is used on the cable assembly and the receptacle is used on the PMD.

For 100GBASE-CR2 and 200GBASE-CR4, the mechanical interface between the PMD and the cable assembly is a mated pair of connectors meeting the requirements of 92.12.1.1 (QSFP), 136C.2.3 (microQSFP), 136C.2.4 (QSFP-DD), or 136C.2.5 (OSFP). The plug connector is used on the cable assembly and the receptacle is used on the PMD.

The cable assembly connector shall be the MDI connector plug. The PMD connector shall be the MDI connector receptacle.

The MDI connector electrical performance is consistent with the signal quality and electrical requirements of 136.9 and 136.10.

An MDI connector type may support one or more PMDs. The assignment of PMD signals to connector signals is specified in Table 136C–2, where as an example 0:DL0n refers to the DL0n signal of the first PMD.

The MDI connectors shall have data signal and signal ground contact assignments as specified in Table 136C–3 for the paired transmit and receive lanes (e.g., (SL0, DL0), (SL1, DL1)).

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Table 136C–2—PMD to connector signal assignments

PMD signal <PMD #>:<PMD signal>			Connector signal
50GBASE-CR	100GBASE-CR2	200GBASE-CR4	
0:DL0n	0:DL0n	0:DL0n	DL0n
0:DL0p	0:DL0p	0:DL0p	DL0p
1:DL0n	0:DL1n	0:DL1n	DL1n
1:DL0p	0:DL1p	0:DL1p	DL1p
2:DL0n	1:DL0n	0:DL2n	DL2n
2:DL0p	1:DL0p	0:DL2p	DL2p
3:DL0n	1:DL1n	0:DL3n	DL3n
3:DL0p	1:DL1p	0:DL3p	DL3p
4:DL0n	2:DL0n	1:DL0n	DL4n
4:DL0p	2:DL0p	1:DL0p	DL4p
5:DL0n	2:DL1n	1:DL1n	DL5n
5:DL0p	2:DL1p	1:DL1p	DL5p
6:DL0n	3:DL0n	1:DL2n	DL6n
6:DL0p	3:DL0p	1:DL2p	DL6p
7:DL0n	3:DL1n	1:DL3n	DL7n
7:DL0p	3:DL1p	1:DL3p	DL7p
0:SL0n	0:SL0n	0:SL0n	SL0n
0:SL0p	0:SL0p	0:SL0p	SL0p
1:SL0n	0:SL1n	0:SL1n	SL1n
1:SL0p	0:SL1p	0:SL1p	SL1p
2:SL0n	1:SL0n	0:SL2n	SL2n
2:SL0p	1:SL0p	0:SL2p	SL2p
3:SL0n	1:SL1n	0:SL3n	SL3n
3:SL0p	1:SL1p	0:SL3p	SL3p
4:SL0n	2:SL0n	1:SL0n	SL4n
4:SL0p	2:SL0p	1:SL0p	SL4p
5:SL0n	2:SL1n	1:SL1n	SL5n
5:SL0p	2:SL1p	1:SL1p	SL5p
6:SL0n	3:SL0n	1:SL2n	SL6n
6:SL0p	3:SL0p	1:SL2p	SL6p
7:SL0n	3:SL1n	1:SL3n	SL7n
7:SL0p	3:SL1p	1:SL3p	SL7p

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Table 136C–3—MDI connector contact mapping

SFP	QSFP	micro QSFP	OSFP	QSFP-DD	Connector signal name	Description
—	1	1	1	1	GND	Ground
—	2	2	3	2	SL1n	Transmitter Inverted Data Input
—	3	3	2	3	SL1p	Transmitter Non-Inverted Data Input
—	4	4	4	4	GND	Ground
—	5	5	6	5	SL3n	Transmitter Inverted Data Input
—	6	6	5	6	SL3p	Transmitter Non-Inverted Data Input
—	7	7	7	7	GND	Ground
—	13	13	—	13	GND	Ground
—	14	14	26	14	DL2p	Receiver Non-Inverted Data Output
—	15	15	25	15	DL2n	Receiver Inverted Data Output
14	16	16	27	16	GND	Ground
13	17	17	29	17	DL0p	Receiver Non-Inverted Data Output
12	18	18	28	18	DL0n	Receiver Inverted Data Output
11	19	19	30	19	GND	Ground
—	20	20	31	20	GND	Ground
—	21	21	33	21	DL1n	Receiver Inverted Data Output
—	22	22	32	22	DL1p	Receiver Non-Inverted Data Output
—	23	23	34	23	GND	Ground
—	24	24	36	24	DL3n	Receiver Inverted Data Output
—	25	25	35	25	DL3p	Receiver Non-Inverted Data Output
—	26	26	37	26	GND	Ground
—	32	32	—	32	GND	Ground
—	33	33	56	33	SL2p	Transmitter Non-Inverted Data Input
—	34	34	55	34	SL2n	Transmitter Inverted Data Input
17	35	35	57	35	GND	Ground
18	36	36	59	36	SL0p	Transmitter Non-Inverted Data Input
19	37	37	58	37	SL0n	Transmitter Inverted Data Input
20	38	38	60	38	GND	Ground
—	—	—	—	39	GND	Ground
—	—	—	9	40	SL5n	Transmitter Inverted Data Input
—	—	—	8	41	SL5p	Transmitter Non-Inverted Data Input
—	—	—	10	42	GND	Ground
—	—	—	12	43	SL7n	Transmitter Inverted Data Input

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Table 136C–3—MDI connector contact mapping *(continued)*

SFP	QSFP	micro QSFP	OSFP	QSFP-DD	Connector signal name	Description
—	—	—	11	44	SL7p	Transmitter Non-Inverted Data Input
—	—	—	18	45	GND	Ground
—	—	—	13	51	GND	Ground
—	—	—	20	52	DL6p	Receiver Non-Inverted Data Output
—	—	—	19	53	DL6n	Receiver Inverted Data Output
—	—	—	21	54	GND	Ground
—	—	—	23	55	DL4p	Receiver Non-Inverted Data Output
—	—	—	22	56	DL4n	Receiver Inverted Data Output
—	—	—	24	57	GND	Ground
—	—	—	—	58	GND	Ground
—	—	—	39	59	DL5n	Receiver Inverted Data Output
—	—	—	38	60	DL5p	Receiver Non-Inverted Data Output
—	—	—	40	61	GND	Ground
—	—	—	42	62	DL7n	Receiver Inverted Data Output
—	—	—	41	63	DL7p	Receiver Non-Inverted Data Output
—	—	—	43	64	GND	Ground
—	—	—	48	70	GND	Ground
—	—	—	50	71	SL6p	Transmitter Non-Inverted Data Input
—	—	—	49	72	SL6n	Transmitter Inverted Data Input
—	—	—	51	73	GND	Ground
—	—	—	53	74	SL4p	Transmitter Non-Inverted Data Input
—	—	—	52	75	SL4n	Transmitter Inverted Data Input
—	—	—	54	76	GND	Ground

136C.2 MDI connector types

136C.2.1 SFP28

For 50GBASE-CR, the mechanical interface between the PMD and the cable assembly may be a mated pair of connectors meeting the requirements of 110.11.1 (SFP28). SFP28 supports one lane.

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136C.2.2 QSFP28

For 50GBASE-CR, 100GBASE-CR2 or 200GBASE-CR4 the mechanical interface between the PMD and the cable assembly may be a mated pair of connectors meeting the requirements of 92.12.1.1 (QSFP28). QSFP28 supports up to four lanes.

136C.2.3 MicroQSFP

For 50GBASE-CR, 100GBASE-CR2 or 200GBASE-CR4 the mechanical interface between the PMD and the cable assembly may be a mated pair of connectors as defined in the microQSFP MSA.[320] microQSFP supports up to four lanes.

The microQSFP cable assembly connector is the plug illustrated in Figure 136C–1. The microQSFP PMD connector is the receptacle with the mechanical mating interface as illustrated in Figure 136C–2. The connectors have data signal and signal ground contact assignments as specified in Table 136C–3.

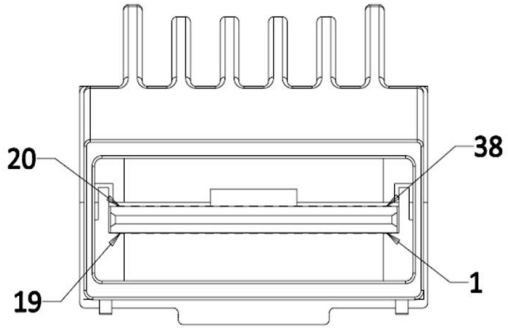

Figure 136C–1— microQSFP cable assembly plug

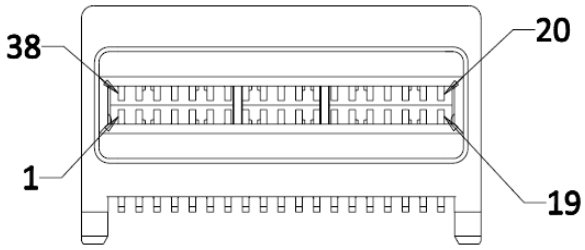

Figure 136C–2—microQSFP PMD receptacle

[320]microQSFP specifications are available at http://www.microqsfp.com.

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136C.2.4 QSFP-DD

For 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4 the mechanical interface between the PMD and the cable assembly may be a mated pair of connectors as defined as defined in the QSFP-DD MSA.[321] QSFP-DD supports up to eight lanes.

The QSFP-DD cable assembly connector is the plug illustrated in Figure 136C–3. The QSFP-DD PMD connector is the receptacle with the mechanical mating interface as illustrated in Figure 136C–4. The connectors have data signal and signal ground contact assignments as specified in Table 136C–3.

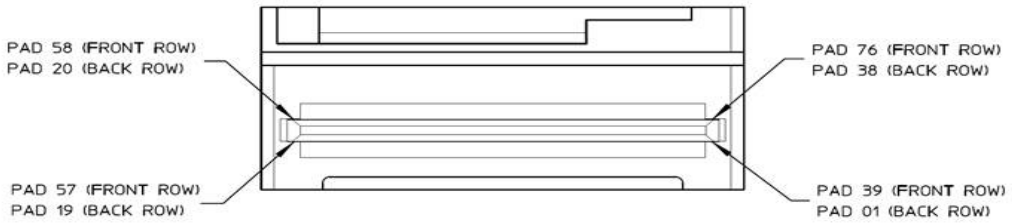

Figure 136C–3—QSFP-DD cable assembly plug

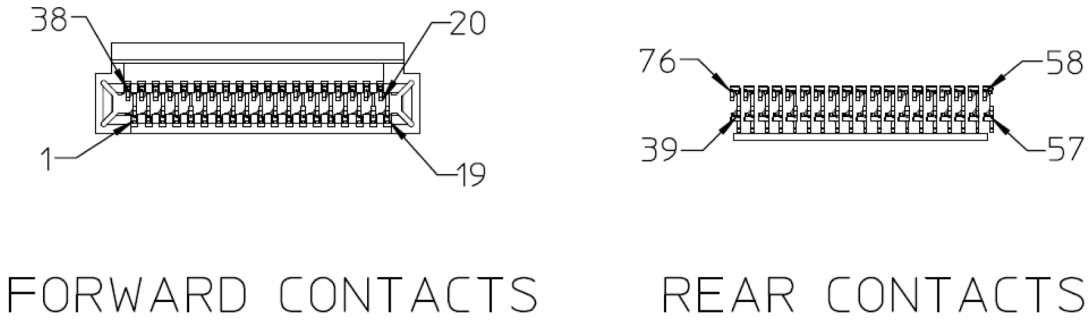

Figure 136C–4—QSFP-DD PMD receptacle

[321] QSFP-DD specifications are available at http://www.qsfp-dd.com.

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136C.2.5 OSFP

For 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4, the mechanical interface between the PMD and the cable assembly may be a mated pair of connectors as defined in the OSFP MSA.[322] OSFP supports up to eight lanes.

The OSFP cable assembly connector is the plug illustrated in Figure 136C–5. The OSFP PMD connector is the receptacle with the mechanical mating interface as illustrated in Figure 136C–6. The connectors have data signal and signal ground contact assignments as specified in Table 136C–3.

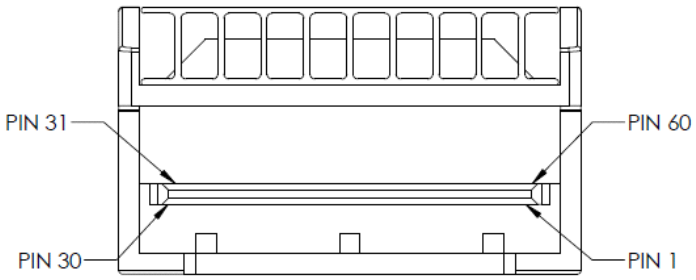

Figure 136C–5—OSFP cable assembly plug

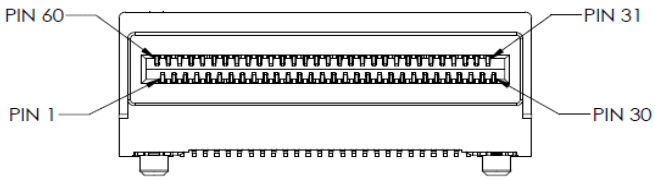

Figure 136C–6—OSFP PMD receptacle

[322]OSFP specifications are available at https://www.osfpmsa.org.

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136C.3 Protocol implementation conformance statement (PICS) proforma for Annex 136C, MDIs for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4[323]

136C.3.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 136C, MDIs for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

136C.3.2 Identification

136C.3.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1, 3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

136C.3.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 136C, MDIs for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[323] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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136C.3.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*MDI1	SFP28 MDI connector	136C.2.1	Device uses SFP28 receptacle as MDI connector	O	Yes [ ] No [ ]
*MDI2	QSFP28 MDI connector	136C.2.2	Device uses QSFP28 receptacle as MDI connector	O	Yes [ ] No [ ]
*MDI3	microQSFP MDI connector	136C.2.3	Device uses microQSFP28 receptacle as MDI connector	O	Yes [ ] No [ ]
*MDI4	QSFP-DD MDI connector	136C.2.4	Device uses QSFP-DD receptacle as MDI connector	O	Yes [ ] No [ ]
*MDI5	OSFP MDI connector	136C.2.5	Device uses OSFP receptacle as MDI connector	O	Yes [ ] No [ ]

136C.3.4 PICS proforma tables for MDIs for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136C.3.4.1 Contact Mapping

Item	Feature	Subclause	Value/Comment	Status	Support
CM1	SFP28 MDI connector contact mapping according to Table 136C–3	136C.1		MDI1:M	Yes [ ] N/A [ ]
CM2	QSFP28 MDI connector contact mapping according to Table 136C–3	136C.1		MDI2:M	Yes [ ] N/A [ ]
CM3	microQSFP MDI connector contact mapping according to Table 136C–3	136C.1		MDI3:M	Yes [ ] N/A [ ]
CM4	QSFP-DD MDI connector contact mapping according to Table 136C–3	136C.1		MDI4:M	Yes [ ] N/A [ ]
CM5	OSFP MDI connector contact mapping according to Table 136C–3	136C.1		MDI5:M	Yes [ ] N/A [ ]

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Annex 136D

(informative)

Host and cable assembly form factors for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4

136D.1 Overview

This annex describes form factors for the cable assemblies specified in 136.11 and for hosts with 50GBASE-CR, 100GBASE-CR2, or 200GBASE-CR4 Physical Layers. Hosts have five specified MDI connectors: single-lane (SFP28 specified in 136C.2.1), four-lane (QSFP28 specified in 136C.2.2 and microQSFP specified 136C.2.3) and eight-lane (QSFP-DD specified in 136C.2.4 and OSFP specified in 136C.2.5). This creates five host interface types and multiple cable assembly types with different combinations of the connectors at each end. These host and cable assembly types are referred to as form factors, distinguishing both the host receptacle (MDI) and the cable assembly plug. Cable assemblies denoted as 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4, have a common set of electrical parameters specified in 136.11. The 50GBASE-CR is a single-lane cable assembly enabling a 3 m length (and can also be implemented as a multiple version using a four-lane or eight-lane plug for high density applications). The 100GBASE-CR2 is a two-lane cable assembly enabling a 3 m length (and can also be implemented as a multiple version using a four-lane and eight-lane plug for high density applications). The 200GBASE-CR4 is a four-lane cable assembly enabling a 3 m length.

136D.2 Host form factors

136D.2.1 SFP28 host form factor

A host may use the SFP28 receptacle specified in 110.11.1 as the MDI for each 50GBASE-CR. This is referred to as an SFP28 host form factor.

A SFP28 form factor host can form a single 50 Gb/s link to either another SFP28 form factor host, using an SFP28 to SFP28 form factor cable assembly (see 136D.3.1), or a QSFP28 form factor host (see 136D.2.2), using a QSFP28 to 4×SFP28 form factor cable assembly (see 136D.3.3).

136D.2.2 QSFP28 host form factor

A host may use the QSFP28 receptacle specified in 136C.2.2 as the MDI for one, two, three or four 50GBASE-CR PHYs, one or two 100GBASE-CR2 PHYs, or one 200GBASE-CR4 PHY. This is referred to as a QSFP28 host form factor.

A QSFP28 form factor host can also form up to four 50 Gb/s links to either another QSFP28 form factor host, using a QSFP28 to QSFP28 form factor cable assembly (see 136D.3.2), or four separate SFP28 form factor hosts (see 136D.2.1) using a QSFP28 to 4×SFP28 form factor cable assembly (see 136D.3.3).

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136D.2.3 microQSFP host form factor

A host may use the microQSFP receptacle specified in 136C.2.3 as the MDI for one, two, three or four 50GBASE-CR PHYs, one or two 100GBASE-CR2 PHYs, or one 200GBASE-CR4 PHY. This is referred to as a microQSFP host form factor.

A microQSFP form factor host can also form up to four 50 Gb/s links to either another microQSFP form factor host, using a microQSFP to microQSFP form factor cable assembly (see 136D.3.2), or four separate SFP28 form factor hosts (see 136D.2.1) using a microQSFP to 4xSFP28 form factor cable assembly (see 136D.3.3).

136D.2.4 QSFP-DD host form factor

A host may use the QSFP-DD receptacle specified in 136C.2.4 as an MDI for eight 50GBASE-CR PHYs, four 100GBASE-CR2 PHYs, or two 200GBASE-CR4 PHYs. This is referred to as a QSFP-DD host form factor.

136D.2.5 OSFP host form factor

A host may use the OSFP receptacle specified in 136C.2.5 as the MDI for eight 50GBASE-CR PHYs, four 100GBASE-CR2 PHYs, or two 200GBASE-CR4 PHYs. This is referred to as an OSFP host form factor.

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136D.3 Cable assembly form factors

A subset of the possible cable assembly form factors are provided as examples in 136D.3.1 through 136D.3.4. The examples are: one-plug to one-plug, one-plug to two-plug, one-plug to four-plug, and one-plug to eight-plug. Cable assembly form factors consisting of any combination of MDIs and number of lanes that meet the requirements of 136.11 are acceptable.

136D.3.1 One-plug to one-plug cable assembly form factor

A one-plug to one-plug cable assembly form factor can use SFP28 plugs as specified in 110.11.1, QSFP28 plugs as specified in 92.12.1.1, microQSFP plugs as specified in 136C.2.3, QSFP-DD plugs as specified in 136C.2.4, or OSFP plugs as specified in 136C.2.5 on both ends. One plug to one plug cables can also have different cable plugs on each end. It may be used to connect the host form factors in 136D.2 with a single or, except for SFP28, multiple 50 Gb/s link.

A SFP28 to SFP28 cable assembly is illustrated in Figure 136D–1. Note that the figure is one example of a one-plug to one-plug cable assembly form factor.

The electrical characteristics of a cable assembly for this form factor are specified in 136.11, using the definitions in 136.11.7.1.1 and 136.11.7.1.2.

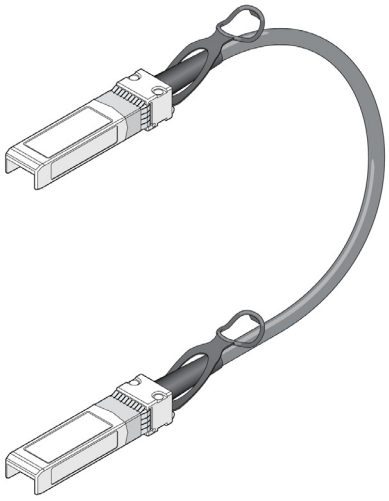

Figure 136D–1—SFP28 to SFP28 cable assembly

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136D.3.2 One-plug to two-plug cable assembly form factor

A one-plug to two-plug cable assembly form factor can use either a QSFP28 plug as specified in 92.12.1.1 or a microQSFP plug as specified in 136C.2.3 on one end, and two QSFP28 or microQSFP plugs on the other end. It may be used to connect a QSFP28 form factor host (see 136D.2.2) or a microQSFP form factor host (see 136D.2.3) on the one-plug end to two QSFP28 or microQSFP form factor hosts on the two-plug end, such that the host on the one-plug end forms two 50GBASE-CR links or one 100GBASE-CR2 link with each of the hosts on the two-plug end.

A QSFP28 to two QSFP28 cable assembly is illustrated in Figure 136D–2. Note that the figure is one example of a one-plug to two-plug cable assembly form factor.

The electrical characteristics of a cable assembly for this form factor are specified in 136.11, using the definitions in 136.11.7.1.1 and 136.11.7.1.2.

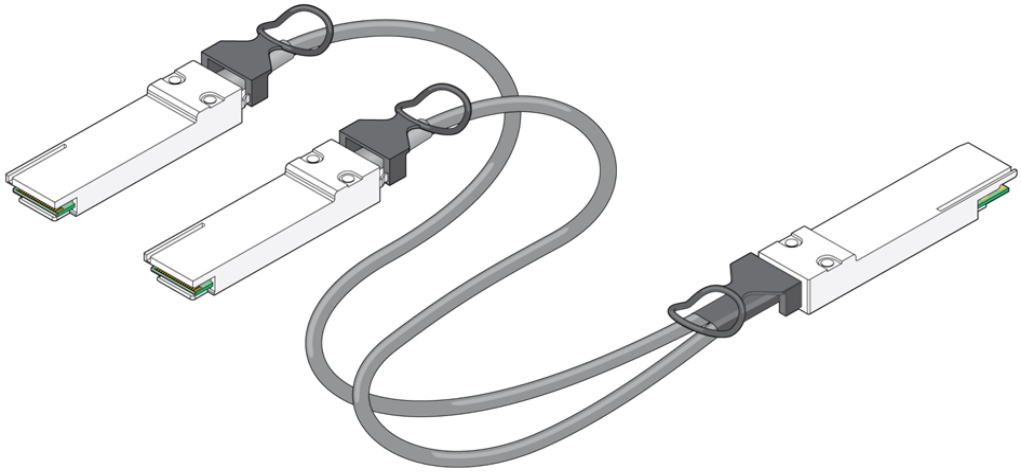

Figure 136D–2—QSFP28 to 2×QSFP28 cable assembly

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136D.3.3 One-plug to four-plug cable assembly form factor

A one-plug to four-plug cable assembly form factor can use either a QSFP28 plug as specified in 92.12.1.1 or a microQSFP plug as specified in 136C.2.3 on one end, and four SFP28 plugs as specified in 110.11.1 on the other end. It may be used to connect a QSFP28 or microQSFP form factor host (see 136D.2.2 or 136D.2.3) to up to four SFP28 form factor hosts (see 136D.2.1) with one 50 Gb/s link to each SFP28 host.

A QSFP28 to four SFP28 cable assembly is illustrated in Figure 136D–3. Note that the figure is one example of a one-plug to four-plug cable assembly form factor.

The electrical characteristics of a cable assembly for this form factor are specified in 136.11, using the definitions in 136.11.7.1.1 and 136.11.7.1.2.

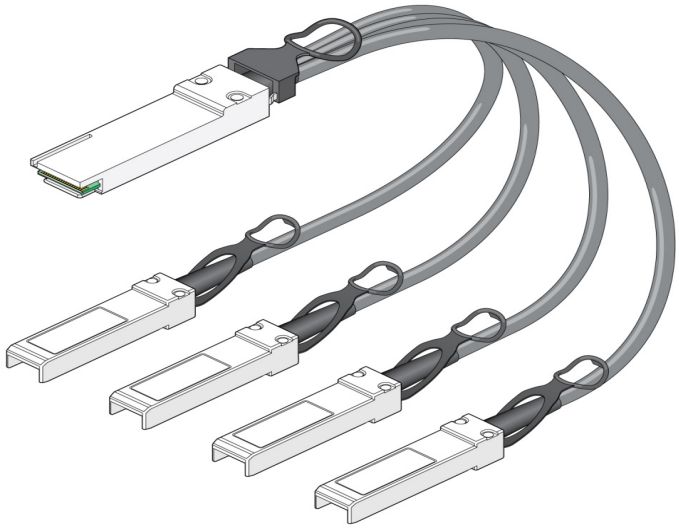

Figure 136D–3—QSFP28 to 4×SFP28 cable assembly

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136D.3.4 One-plug to eight-plug cable assembly form factor

A one-plug to eight-plug cable assembly form factor can use either a QSFP-DD plug as specified in 136C.2.4 or an OSFP plug as specified in 136C.2.5 on one end, and eight SFP28 plugs as specified in 110.11.1 on the other end. It may be used to connect a QSFP-DD or OSFP form factor host (see 136D.2.4 or 136D.2.5) to up to eight SFP28 form factor hosts (see 136D.2.1) with one 50 Gb/s link to each SFP28 host.

A QSFP-DD to eight SFP28 cable assembly is illustrated in Figure 136D–4. Note that the figure is one example of a one-plug to eight-plug cable assembly form factor.

The electrical characteristics of a cable assembly for this form factor are specified in 136.11, using the definitions in 136.11.7.1.1 and 136.11.7.1.2.

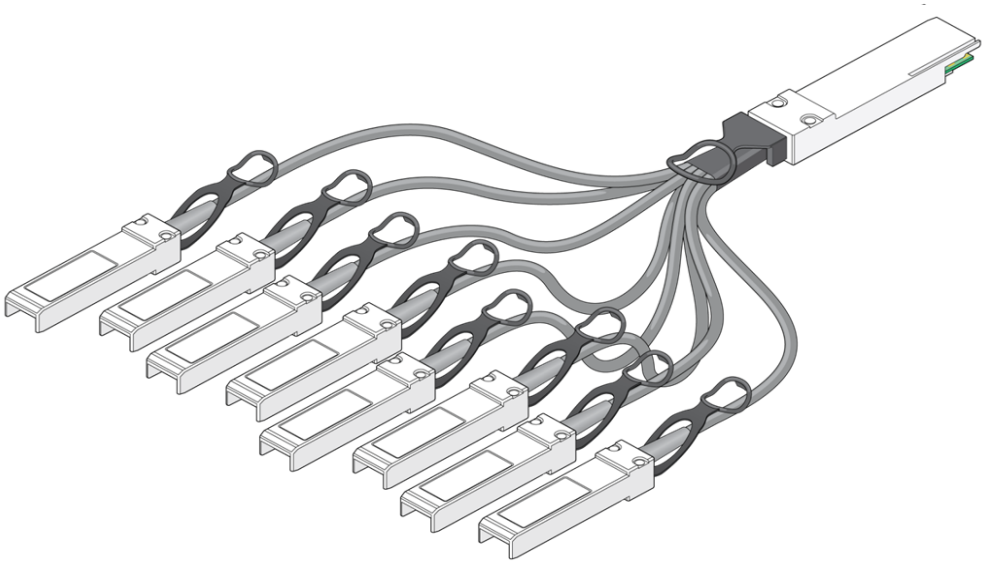

Figure 136D–4—QSFP-DD to 8×SFP28 cable assembly

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Annex 142A

(informative)

Encoding example for QC-LDPC(16952,14392) FEC and interleaving

142A.1 Example of initial control seed sequence

For example, from Table 142–5 the control seed sequence for the first user interleaver is:

0xE3-88-B0-9A-74-F4-94-8E-5D-C0-CC-8A-18-9A-B9-B2

which represents the binary sequence:

```
1 1 1 0   0 0 1 1   1 0 0 0   1 0 0 0   1 0 1 1   0 0 0 0   1 0 0 1   1 0 1 0
0 1 1 1   0 1 0 0   1 1 1 1   0 1 0 0   1 0 0 1   0 1 0 0   1 0 0 0   1 1 1 0
0 1 0 1   1 1 0 1   1 1 0 0   0 0 0 0   1 1 0 0   1 1 0 0   1 0 0 0   1 0 1 0
0 0 0 1   1 0 0 0   1 0 0 1   1 0 1 0   1 0 1 1   1 0 0 1   1 0 1 1   0 0 1 0
```

From Table 142–4, the switch programming sequence for the first stage of the user interleaver is a circular shift (left rotation) of the above control seed by 17 positions:

```
Control bit for switch 127 of the first stage
|
0 1 0 1   1 1 0 0   1 1 0 1   1 0 0 1   0 1 1 1   0 0 0 1   1 1 0 0   0 1 0 0
0 1 0 1   1 0 0 0   0 1 0 0   1 1 0 1   0 0 1 1   1 0 1 0   0 1 1 1   1 0 1 0
0 1 0 0   1 0 1 0   0 1 0 0   0 1 1 1   0 0 1 0   1 1 1 0   1 1 1 0   0 0 0 0
0 1 1 0   0 1 1 0   0 1 0 0   0 1 0 1   0 0 0 0   1 1 0 0   0 1 0 0   1 1 0 1
                                                                        |
                                                                        Control bit for switch 0 of the first stage
```

From Table 142–4, the switch programming sequence for the second stage of the user interleaver is a circular shift (left rotation) of the above control seed by 34 positions:

```
Control bit for switch 127 of the first stage
|
1 0 0 0   0 1 1 0   0 0 1 0   0 1 1 0   1 0 1 0   1 1 1 0   0 1 1 0   1 1 0 0
1 0 1 1   1 0 0 0   1 1 1 0   0 0 1 0   0 0 1 0   1 1 0 0   0 0 1 0   0 1 1 0
1 0 0 1   1 1 0 1   0 0 1 1   1 1 0 1   0 0 1 0   0 1 0 1   0 0 1 0   0 0 1 1
1 0 0 1   0 1 1 1   0 1 1 1   0 0 0 0   0 0 1 1   0 0 1 1   0 0 1 0   0 0 1 0
                                                                        |
                                                                        Control bit for switch 0 of the first stage
```

142A.2 QC-LDPC FEC encoder test vectors

Five test vectors are provided to assist in the implementation and verification of the FEC encoder and interleaver as presented in 142.4. The locations of each of the vectors in the processing path relative to Figure 142–5 are shown in Figure 142A–1.

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The description for each of the five test vectors are provided in Table 142A–1. Bit 0 of word 0 of each test vector is first on the wire. The values for Test Vector 1 are shown in Table 142A–2. The values for Test Vector 2 are shown in Table 142A–3. The values for Test Vector 3 are shown in Table 142A–4. The values for Test Vector 4 are shown in Table 142A–5. The values for Test Vector 5 are shown in Table 142A–6.

NOTE—Files containing the test vectors shown in Table 142A–2, Table 142A–3, Table 142A–4, Table 142A–5, and Table 142A–6 are available at https://standards.ieee.org/downloads/802.3/.

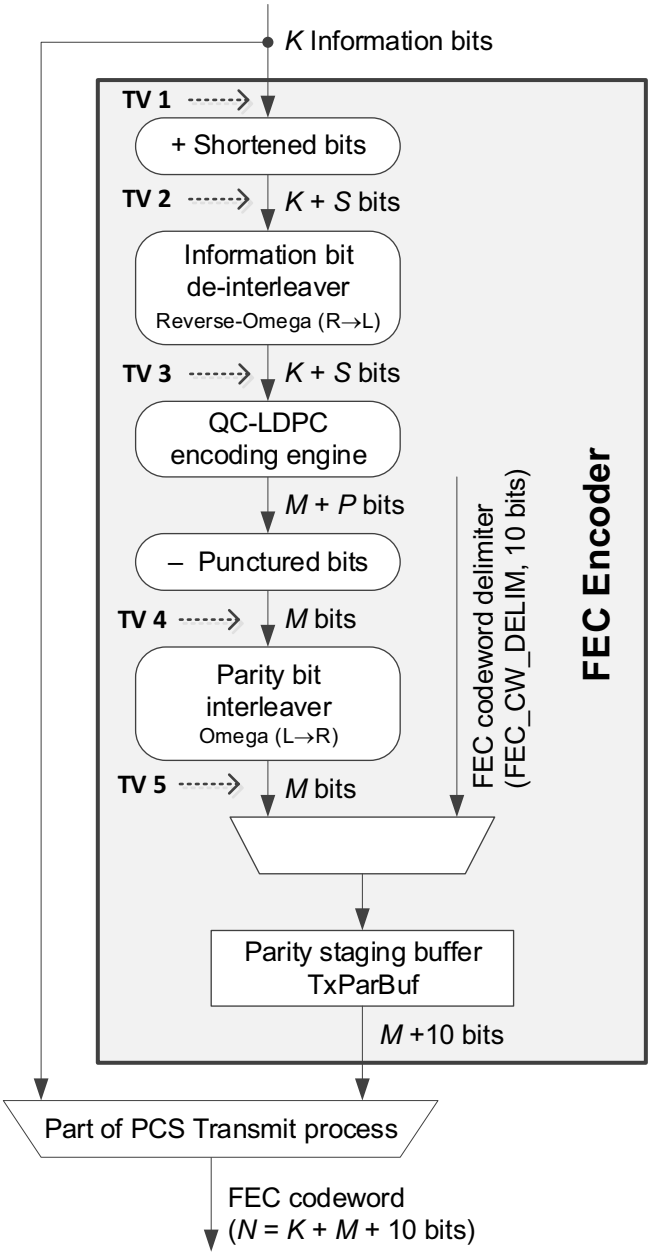

Figure 142A–1—QC-LDPC FEC encoder test vector locations

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Table 142A–1—FEC encoder and interleaver test vector description

Test Vector	Filename	Description
TV 1	ldpc_tv1_pre_zeropadding	56 × 257-bit line coded input, pre-zero padding
TV 2	ldpc_tv2_pre_enc_pre_deintlv	57 × 256 $K + S$ bits, pre-de-interleaving
TV 3	ldpc_tv3_pre_enc_post_deintlv	57 × 256 $K + S$ bits, post-de-interleaving
TV 4	ldpc_tv4_post_enc_pre_intlv	10 × 256 M parity bits pre-interleaving
TV 5	ldpc_tv5_post_enc_post_intlv	10 × 256 M parity bits post-interleaving

Table 142A–2—Test Vector 1 values

Test Vector 1: 56 × 257-bit line coded input, pre-zero padding	
Word	bit 256 <---------- bit 0
0	0_AC37_F816_7AA6_44F5_C564_F932_36B7_7BA7_B635_45B4_FAE8_76AF_0A9C_D3ED_224C_322A
1	0_8583_96FC_8D23_0882_6716_5966_FB87_C9A9_EA93_5B02_C114_8E69_CD0F_4A01_3E6A_9639
2	1_F38D_A7C9_E9F4_D4A8_F0E4_A8E6_EA31_CBA0_0457_9B22_344D_9088_DCDE_31C4_9DCA_FC1A
3	1_0D98_891A_2A4A_61E5_1AEA_9331_4CF1_1216_54D9_6997_0E77_6451_DAD4_1A99_1E8A_37B0
4	0_FE87_D099_ACA0_4E1C_CE78_BC27_5560_D7E1_2801_DC54_9894_4B22_DBE8_35F9_62F3_9A21
5	1_1529_D1A6_B536_6363_8618_196E_4EB5_1E37_25C0_BF2B_BAA2_F59D_2E9C_6F3D_255A_CC0C
6	1_E9C8_EC75_C2FB_87A5_02CF_BD29_4944_CF68_2A02_4F12_18D1_9610_B251_D2CC_0E3C_0AAA
7	0_92BD_10B7_43F7_9DDA_5CFF_664F_112E_9BB2_ECAF_CE51_B26C_D5F6_B14D_4245_337D_D434
8	0_7D6A_1D2D_FB87_0B6F_BBEA_BC03_B642_A226_AEEB_D530_EA0E_9BEA_6988_010B_8387_84A4
9	1_8BC3_B80D_E609_1C23_D36A_7914_CD65_9E58_6955_4819_F064_A716_C1B0_DE4A_02E0_8ACA
10	0_18EA_B9AF_FE74_D4C8_A037_7FF9_72CA_1371_4FB1_D7AA_8871_825D_DC3E_5125_D644_23E3
11	0_7CF6_300D_BB98_8DEC_2C31_86E8_D6FE_6ED4_C1BB_2202_DBDB_E14B_12E1_E2EA_CAA5_0505
12	0_EBB5_2A15_8C13_2AB8_881D_9460_B646_B7EA_D198_421E_99EE_2689_A2C1_B3FE_4DF6_6565
13	1_EE05_8154_6435_F67D_3FAF_F2EC_F320_0E2B_EA39_C67B_F0CC_FBE3_110D_FCDD_8CA5_4707
14	1_6491_F261_CAF6_0787_E48C_64E3_311D_88DA_9202_6A8C_0A33_B8E2_F786_FDF2_5350_7D7D
15	1_9F65_0E02_FEB3_3FB1_BEB5_B769_1A22_C02B_F568_A4EB_9C2D_7678_F4E6_247B_CFD2_E868
16	1_70B6_AB53_E188_8A6D_3CE7_7364_8C4E_05C6_F964_060F_9340_8CD6_489B_4AF7_B97D_CDCD
17	1_C2B8_8F38_C964_1D5C_2D88_4B83_5077_3205_8452_505E_57C7_4499_FC07_2815_14D3_8A4A
18	0_914B_4DAE_68E0_CBB8_4BA4_62EE_B46F_379F_0FEB_5A50_7087_E6D3_060C_F4DD_BF62_0CCC
19	1_A9E5_CA36_82CC_61B3_F544_F308_2D79_6652_7DF6_8DB5_8FEF_2A62_98EF_3E7E_1C05_5474
20	0_68F8_89C0_3C5E_2411_FAA0_4F5B_1E62_68B2_E505_8A67_29D6_C683_99B2_EAFC_28EE_2BAB
21	0_1E75_5997_11B0_07B1_9DA0_5670_66CF_EFBE_95E2_4EA5_FA2F_5FE0_936F_BB13_7CB5_9939
22	0_EFFD_0DD5_8881_6B2B_D226_0F26_E1BE_19C3_4ABB_A0EF_1B9B_9CA1_DD7C_0069_66EA_0AAA
23	1_CEC8_91D3_4D1E_6C50_7FAE_7B26_88FF_CA00_12DE_CBF9_E68D_B3D5_01C8_5E40_A8A4_EF4F
24	0_EB4C_D7E9_A989_DC0B_E8B4_877C_F298_93A9_3F54_F8D6_393E_2268_1173_37A0_297C_90B0
25	1_D93B_4CCD_8C8C_9A67_DD9F_C8D0_DA3C_8DB0_F644_2AFE_0A7C_A272_0544_FF2A_00CD_D393
26	0_7D84_4E33_6317_1BFD_826C_3C95_4254_582A_100A_6751_D9FC_3EBB_854E_A4DF_AB94_5535
27	1_BC2E_169E_A184_415F_83AE_57DD_ABEB_ED9D_9626_45AE_324E_AE2C_5C54_E006_0FAB_4424
28	1_5AF6_70CA_F81C_5A55_36D6_9464_D59A_00FE_F5BA_C782_3E70_7773_605F_8C84_6D8D_5E9E
29	1_3CC1_6A2F_5AE9_EA12_0D18_CA75_A334_3FE5_C1CE_2551_09A5_D744_C961_CD6E_50D8_1494
30	1_3A10_9924_01DF_A2F5_7078_E70F_6B09_5F3D_35DE_6561_0EFB_E192_0BAB_1936_DDDE_B191
31	1_0935_740F_DF07_F9A2_B269_55BA_EB49_3AC5_BD0D_D91B_696D_D342_F91E_19F9_984B_ED6D

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Table 142A–2—Test Vector 1 values *(continued)*

Test Vector 1: 56 × 257-bit line coded input, pre-zero padding	
Word	bit 256 <---------- bit 0
32	1_5E38_2028_3609_BF16_B9EA_DD30_D9C9_D197_4085_A426_C6F0_B20E_3728_CF54_A5C6_1959
33	1_3C9E_9E2D_48B9_0CD8_063C_8B95_BF31_8EE7_BEFE_12B0_0E35_B729_0961_8D2F_BCC8_33B3
34	1_B05A_5175_C731_A38A_22E5_192D_6F4D_4061_114A_6972_9E7E_448B_9A0B_2FE6_FA6D_F2B2
35	0_40B7_CE42_BF91_BDE2_1A4F_D3E6_1E13_B444_E57C_6528_0848_1F30_5CFF_419D_FA34_7D1D
36	0_46F4_64D1_FA1A_6FD2_F0E3_6A62_EBD7_A6C6_CC02_413A_BDCE_E90A_DDB1_1519_5119_6747
37	0_229A_6345_652A_5B2D_EDFD_6CE6_E70A_189A_3C48_7E30_CD40_3027_141B_6EB0_3DDA_01E1
38	0_A62E_1180_87CC_80D0_1B9E_6352_3F4A_7CEF_A805_218F_76AE_DA3F_DA0F_989C_58A5_0A2A
39	1_ADF4_17F0_3988_A4DA_699E_B13D_B40E_8F1B_B64F_39A4_E497_557F_7961_8615_1517_F3D3
40	1_B90F_5A90_AF9D_649D_EF45_19C3_4461_40F7_F958_8FFA_09AF_73CB_B85A_8989_3AED_DB3B
41	0_F115_AEC2_79A2_0088_057A_B031_3E86_0AD1_9FF6_3FB1_6674_97A9_6F7A_C1B6_C513_3D9D
42	0_ACC0_6E95_6C92_F339_6E7C_8894_B5AE_57EE_55DF_EF96_9667_2659_9330_D7C3_8331_E828
43	1_0BDE_2E8F_1DE2_937E_A5E4_777B_F64B_AE60_0CD1_DF67_A907_6223_D833_A2EC_3585_0060
44	0_393A_00C4_1AE5_2B52_EBEA_6C7B_F4C5_A522_4E3F_573A_DB8E_1CE2_4C49_873F_D360_CDED
45	0_30A7_E83A_D65E_0247_E9B2_F383_C9F0_E7C4_7044_6EFA_F1E6_A020_C51F_A61F_8D6B_F7D7
46	1_0485_EEAE_1500_05E1_21C7_8FBD_B1F6_C176_A9CD_3A55_DAFA_E9F5_2E70_30B8_B8AD_65E5
47	1_34EA_AE14_B8BA_0A5A_7BE0_CA52_37C8_DF67_E3DE_68F6_3F29_111D_D5B9_8738_FAA3_5616
48	1_3830_CB5F_6543_0066_6C3E_1A5E_938B_C4EA_771B_D947_99D9_C6A6_FE22_8E22_27B5_E282
49	0_0D3D_C899_DC8F_7312_A110_7255_2D96_6E1A_89DF_C470_9D15_9A00_C4B1_04B1_65F0_A2E2
50	0_F363_A4B4_96F7_6262_34A5_6BB1_10AE_B598_FFE9_F3B9_15DA_4B84_B30C_7824_F996_71F1
51	0_FF63_8DCB_A05B_6FB4_B515_E44A_AA52_B767_1395_F0D8_2AB6_D392_3F0E_71EB_6389_87E7
52	1_202D_A75B_AD01_6DE8_26D4_D231_DA1D_4E4A_1CFD_CFE9_3EAE_BA52_E839_A748_9F47_8929
53	0_AA1D_9AA3_D9DD_2E11_22A4_8CA2_E6DF_D793_53D1_42C3_9FAD_9821_4754_980D_7867_A9C9
54	0_6C5C_0DDD_6AEE_33C6_D17B_AD75_CE22_4770_1605_5FB3_2367_B769_77BA_C23F_81AA_2484
55	1_E19D_2B31_30F3_4466_0FC6_0DB4_FD67_892F_00A6_8D2B_8847_35C8_CF1A_5301_5BAD_5676

Table 142A–3—Test Vector 2 values

Test Vector 2: 57 × 256-bit *K* + *S* information bits, pre de-interleaver reverse-Omega (R→L)	
Word	bit 255 <---------- bit 0
0	AC37_F816_7AA6_44F5_C564_F932_36B7_7BA7_B635_45B4_FAE8_76AF_0A9C_D3ED_224C_322A
1	0B07_2DF9_1A46_1104_CE2C_B2CD_F70F_9353_D526_B605_8229_1CD3_9A1E_9402_7CD5_2C72
2	CE36_9F27_A7D3_52A3_C392_A39B_A8C7_2E80_115E_6C88_D136_4223_7378_C712_772B_F069
3	6CC4_48D1_5253_0F28_D754_998A_6788_90B2_A6CB_4CB8_73BB_228E_D6A0_D4C8_F451_BD87
4	E87D_099A_CA04_E1CC_E78B_C275_560D_7E12_801D_C549_8944_B22D_BE83_5F96_2F39_A218
5	A53A_34D6_A6CC_6C70_C303_2DC9_D6A3_C6E4_B817_E577_545E_B3A5_D38D_E7A4_AB59_818F
6	723B_1D70_BEE1_E940_B3EF_4A52_5133_DA0A_8093_C486_3465_842C_9474_B303_8F02_AAA2
7	5E88_5BA1_FBCE_ED2E_7FB3_2788_974D_D976_57E7_28D9_366A_FB58_A6A1_2299_BEEA_1A7A
8	6A1D_2DFB_870B_6FBB_EABC_03B6_42A2_26AE_EBD5_30EA_0E9B_EA69_8801_0B83_8784_A449
9	8770_1BCC_1238_47A6_D4F2_299A_CB3C_B0D2_AA90_33E0_C94E_2D83_61BC_9405_C115_947D
10	AAE6_BFF9_D353_2280_DDFF_E5CB_284D_C53E_C75E_AA21_C609_7770_F944_9759_108F_8F17
11	B180_6DDC_C46F_6161_8C37_46B7_F376_A60D_D910_16DE_DF0A_5897_0F17_5655_2828_2863

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Table 142A–3—Test Vector 2 values *(continued)*

Test Vector 2: 57 × 256-bit *K* + *S* information bits, pre de-interleaver reverse-Omega (R→L)	
Word	bit 255 <---------- bit 0
12	52A1_58C1_32AB_8881_D946_0B64_6B7E_AD19_8421_E99E_E268_9A2C_1B3F_E4DF_6656_53E7
13	B02A_8C86_BECF_A7F5_FE5D_9E64_01C5_7D47_38CF_7E19_9F7C_6221_BF9B_B194_A8E0_EEBB
14	7C98_72BD_81E1_F923_1938_CC47_6236_A480_9AA3_028C_EE38_BDE1_BF7C_94D4_1F5F_7DC0
15	8701_7F59_9FD8_DF5A_DBB4_8D11_6015_FAB4_5275_CE16_BB3C_7A73_123D_E7E9_7434_5924
16	AB53_E188_8A6D_3CE7_7364_8C4E_05C6_F964_060F_9340_8CD6_489B_4AF7_B97D_CDCD_CFB2
17	1E71_92C8_3AB8_5B10_9706_A0EE_640B_08A4_A0BC_AF8E_8933_F80E_502A_29A7_1495_70B6
18	36B9_A383_2EE1_2E91_8BBA_D1BC_DE7C_3FAD_6941_C21F_9B4C_1833_D376_FD88_3333_8571
19	51B4_1663_0D9F_AA27_9841_6BCB_3293_EFB4_6DAC_7F79_5314_C779_F3F0_E02A_A3A2_452D
20	9C03_C5E2_411F_AA04_F5B1_E626_8B2E_5058_A672_9D6C_6839_9B2E_AFC2_8EE2_BABD_4F2E
21	32E2_3600_F633_B40A_CE0C_D9FD_F7D2_BC49_D4BF_45EB_FC12_6DF7_626F_96B3_2726_8F88
22	7562_205A_CAF4_8983_C9B8_6F86_70D2_AEE8_3BC6_E6E7_2877_5F00_1A59_BA82_AA83_CEAB
23	E9A6_8F36_283F_D73D_9344_7FE5_0009_6F65_FCF3_46D9_EA80_E42F_2054_5277_A7BB_FF43
24	E9A9_89DC_0BE8_B487_7CF2_9893_A93F_54F8_D639_3E22_6811_7337_A029_7C90_B0E7_6448
25	9B19_1934_CFBB_3F91_A1B4_791B_61EC_8855_FC14_F944_E40A_89FE_5401_9BA7_26EB_4CD7
26	CD8C_5C6F_F609_B0F2_5509_5160_A840_299D_4767_F0FA_EE15_3A93_7EAE_5154_D7B2_7699
27	F50C_220A_FC1D_72BE_ED5F_5F6C_ECB1_322D_7192_7571_62E2_A700_307D_5A21_21F6_1138
28	AF81_C5A5_536D_6946_4D59_A00F_EF5B_AC78_23E7_0777_3605_F8C8_46D8_D5E9_EDE1_70B4
29	EB5D_3D42_41A3_194E_B466_87FC_B839_C4AA_2134_BAE8_992C_39AD_CA1B_0292_95AF_670C
30	0077_E8BD_5C1E_39C3_DAC2_57CF_4D77_9958_43BE_F864_82EA_C64D_B777_AC64_6798_2D45
31	EF83_FCD1_5934_AADD_75A4_9D62_DE86_EC8D_B4B6_E9A1_7C8F_0CFC_CC25_F6B6_CE84_2649
32	3609_BF16_B9EA_DD30_D9C9_D197_4085_A426_C6F0_B20E_3728_CF54_A5C6_1959_849A_BA07
33	9172_19B0_0C79_172B_7E63_1DCF_7DFC_2560_1C6B_6E52_12C3_1A5F_7990_6767_5E38_2028
34	1CC6_8E28_8B94_64B5_BD35_0184_4529_A5CA_79F9_122E_682C_BF9B_E9B7_CACA_793D_3C5A
35	FC8D_EF10_D27E_9F30_F09D_A227_2BE3_2940_4240_F982_E7FA_0CEF_D1A3_E8EE_C169_45D7
36	A1A6_FD2F_0E36_A62E_BD7A_6C6C_C024_13AB_DCEE_90AD_DB11_5195_1196_7472_05BE_7215
37	A54B_65BD_BFAD_9CDC_E143_1347_890F_C619_A806_04E2_836D_D607_BB40_3C24_6F46_4D1F
38	F320_3406_E798_D48F_D29F_3BEA_0148_63DD_ABB6_8FF6_83E6_2716_2942_8A84_534C_68AC
39	C452_6D34_CF58_9EDA_0747_8DDB_279C_D272_4BAA_BFBC_B0C3_0A8A_8BF9_E9A9_8B84_6021
40	9D64_9DEF_4519_C344_6140_F7F9_588F_FA09_AF73_CBB8_5A89_893A_EDDB_3BD6_FA0B_F81C
41	4401_100A_F560_627D_0C15_A33F_EC7F_62CC_E92F_52DE_F583_6D8A_267B_3BB9_0F5A_90AF
42	4BCC_E5B9_F222_52D6_B95F_B957_7FBE_5A59_9C99_664C_C35F_0E0C_C7A0_A1E2_2B5D_84F3
43	149B_F52F_23BB_DFB2_5D73_0066_8EFB_3D48_3B11_1EC1_9D17_61AC_2803_02B3_01BA_55B2
44	52B5_2EBE_A6C7_BF4C_5A52_24E3_F573_ADB8_E1CE_24C4_9873_FD36_0CDE_D85E_F174_78EF
45	C048_FD36_5E70_793E_1CF8_8E08_8DDF_5E3C_D404_18A3_F4C3_F1AD_7EFA_E393_A00C_41AE
46	0178_4871_E3EF_6C7D_B05D_AA73_4E95_76BE_BA7D_4B9C_0C2E_2E2B_5979_4614_FD07_5ACB
47	052D_3DF0_6529_1BE4_6FB3_F1EF_347B_1F94_888E_EADC_C39C_7D51_AB0B_4121_7BAB_8540
48	0066_6C3E_1A5E_938B_C4EA_771B_D947_99D9_C6A6_FE22_8E22_27B5_E282_9A75_570A_5C5D
49	E625_4220_E4AA_5B2C_DC35_13BF_88E1_3A2B_3401_8962_0962_CBE1_45C5_3830_CB5F_6543
50	8988_D295_AEC4_42BA_D663_FFA7_CEE4_5769_2E12_CC31_E093_E659_C7C4_1A7B_9133_B91E
51	7DA5_A8AF_2255_5295_BB38_9CAF_86C1_55B6_9C91_F873_8F5B_1C4C_3F3B_CD8E_92D2_5BDD
52	DE82_6D4D_231D_A1D4_E4A1_CFDC_FE93_EAEB_A52E_839A_7489_F478_9297_FB1C_6E5D_02DB

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Table 142A–3—Test Vector 2 values *(continued)*

Test Vector 2: 57 × 256-bit *K* + *S* information bits, pre de-interleaver reverse-Omega (R→L)	
Word	bit 255 <---------- bit 0
53	C224_5491_945C_DBFA_F26A_7A28_5873_F5B3_0428_EA93_01AF_0CF5_3932_02DA_75BA_D016
54	F1B4_5EEB_5D73_8891_DC05_8157_ECC8_D9ED_DA5D_EEB0_8FE0_6A89_2115_43B3_547B_3BA5
55	3307_E306_DA7E_B3C4_9780_5346_95C4_239A_E467_8D29_80AD_D6AB_3B1B_1703_775A_BB8C
56	0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_0000_00F0_CE95_9898_79A2

Table 142A–4—Test Vector 3 values

Test Vector 3: 57 × 256-bit *K* + *S* information bits, post de-interleaver reverse-Omega (R→L)	
Word	bit 255 <---------- bit 0
0	75BF_2A5D_425D_12F1_18FE_F6EE_51D6_CCEB_52D1_39AC_8BCD_D048_F231_3A5A_CA6B_7CA6
1	87FF_8610_71E9_2633_3062_0E6A_6012_B213_E093_4059_82BF_74FD_145F_55FA_1A02_3DA5
2	037C_2BC0_5ABB_191C_C4C8_4E5C_BAE7_76F3_7A02_5770_1EA5_D93A_7117_C4E8_1CD8_6CA1
3	E342_1358_42CB_D1E4_99E1_14B0_5CF7_40CE_B3C6_9052_822D_173E_37F6_D933_9C1B_6122
4	E3EB_9B3E_785B_529A_4F4C_3E09_7010_64A5_3757_01DC_7F9A_C122_828A_A81D_7660_099A
5	374F_7D3B_073A_A5B0_BD01_EE40_0615_3AEE_82C0_177C_B30B_0F75_5EB7_D6E9_5542_AD5F
6	B044_DCF9_DBC8_C64A_2221_4028_8B0C_886F_9FC5_1444_2F91_FA33_3201_2AD8_D6C4_6E9D
7	12EF_B1CC_579E_FFB8_E4CC_6070_2ACF_F34A_B748_CFE8_4FE8_8C8A_2BA3_7FE3_E4B6_367B
8	C58C_425C_6E5F_C432_9148_DC80_B8CD_4B5F_4E24_2F60_D571_EF9A_08C3_DCA2_BF2B_3495
9	4C49_A430_5B79_BDB4_C56B_34AD_0911_D281_7791_AD8E_AC46_8412_A764_6647_5744_4B0A
10	9E77_EFF9_5892_9FB1_2AB1_1804_DE4F_8EF3_FBB8_C7C5_5A5B_2382_42AC_ECE4_E0BD_8E85
11	DAD9_C397_3C7F_1C08_8A79_40CD_4092_688D_660E_6F2D_92AC_ACFA_9B27_2C27_6D13_8B88
12	5240_F6EA_3C0C_53C4_FC97_FDBE_3966_944D_0A82_6A5F_42CF_08D1_FCAA_0E87_2C24_ED09
13	DDF7_61FC_2D99_F3BD_DD87_D65D_6E8F_4033_DC4D_0861_966E_A4EF_6E03_B359_ED0E_B152
14	714B_153B_BF20_06AB_8EC7_9D5D_D005_33FC_F24A_21A5_A7DA_F90F_A3B9_81DC_204B_7834
15	FB4C_F049_51AA_5D90_7FF3_D0C1_55F9_DFE0_2B38_3D20_4381_AD6C_F7A1_3834_F8DF_ADAB
16	FF0A_35CD_DFC4_1794_2131_2374_143C_A5EB_7608_61DF_2B61_395B_404B_F79F_78BF_908C
17	9F1D_781E_600C_0C45_7880_86DD_2128_6BA3_A832_FFEC_5D16_200A_E564_B625_6B12_940A
18	30E6_8DDF_CED7_062A_4D28_A89E_A666_28FE_DCCD_FD0D_C667_1D1B_64EC_8475_5961_3AD5
19	13EC_F751_CC7B_44A6_C1CA_2F4A_D9D9_1703_708C_8646_F27F_62C7_1A7E_A699_5979_8E33
20	C610_E2D5_1A56_4F85_7570_7690_1BD7_D4E9_8763_3165_2174_0CDA_046A_35F7_ED92_F3E6
21	6969_FEC5_B26A_094F_F479_8452_27F7_7851_27A3_C347_D3A2_1CB2_DD17_22D8_67F6_AEDF
22	7A78_ECDC_B84F_9C12_7CCF_B05D_A39A_92F0_4880_4ED7_F1C3_3087_A20F_CB3B_4112_A9B5
23	0B97_E535_FE16_F9FB_5DFE_BC02_55C8_9A2A_BB98_346C_F860_5E3F_0E20_366C_C5DC_BE71
24	4F9A_EA1F_8683_B764_E669_E290_0A34_E2AA_F809_0122_77DD_9D07_6CC6_CF97_D079_8582
25	51B9_5B5F_CD21_80EE_947B_93F6_A4A6_605F_9444_91C2_69EE_5A37_F702_D4BB_BB86_6031
26	B7A9_63A5_6B07_8503_65B1_8135_C292_44F4_52E1_E74D_299F_DEFE_F93A_90B5_81D6_7352
27	9867_FFFA_F79C_823C_16CF_2490_B722_F4A8_22DF_108C_AC44_052B_6096_BDC9_D1CA_3CAC
28	57DF_22DB_6D7C_D606_0A8C_CDB7_1229_30C8_3F8B_6E77_C0CB_FBD4_B845_B411_70A4_BCEB
29	0C70_D037_283B_E388_B047_66B6_17A6_C7B4_5567_17EE_D11C_5C83_A110_41B7_147B_ADDC
30	CE25_E4F5_BC9D_49F7_B582_4768_01AC_DB36_D4F9_4C49_6522_3B37_04AE_D5F2_45BA_F376
31	3184_6193_794D_8D2A_7BFE_0ED7_699D_E1BE_1FD6_4520_279B_5F4E_D37D_7149_771E_5742

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Table 142A–4—Test Vector 3 values *(continued)*

Test Vector 3: 57 × 256-bit $K + S$ information bits, post de-interleaver reverse-Omega (R→L)	
Word	bit 255 <---------- bit 0
32	8089_D323_AA17_893B_B48A_F28E_33CE_94EB_4CA3_42FD_CD7C_4187_473D_28A9_3928_0FC1
33	8089_D323_AA17_893B_B48A_F28E_33CE_94EB_4CA3_42FD_CD7C_4187_473D_28A9_3928_0FC1
34	4EF0_2AEF_4C86_8F11_094C_827E_1CE2_2270_23A3_7B7D_30D9_6B37_78E8_5B8C_07FB_8F95
35	108E_6545_25D1_6741_DC21_AD13_4446_699C_EDF0_26AF_057F_1FD3_A6F1_3F3F_4DE7_D8A9
36	9764_337A_EEDD_A30C_6F58_7517_CF06_2522_7D41_C5D4_52A3_FD21_6C63_83E2_02D3_14D7
37	B743_DDD3_07CF_34A8_3D19_466C_662D_8FDC_2AC3_0598_8F1C_95B7_8223_76D8_852E_12C8
38	A164_BBA0_1311_8E73_D5AC_CEE9_A1D9_860F_3DD3_B7E8_E081_DEF3_DA2C_0131_E14A_8306
39	6784_54CE_9B8D_1DCE_5815_0E43_5021_75EE_7B55_06B7_2B9D_67EB_0067_CF41_2323_FA1D
40	3757_509B_C147_7F6E_53E4_9BC1_17EB_7F83_2B6F_0217_EF64_5888_1329_DBF7_D717_8978
41	1640_4B9E_70CC_4C24_A95E_13DA_214F_81B6_56F4_35C4_CCB7_4DD4_1EF3_AAF6_AB5C_B92D
42	8D95_372F_8FC6_2C07_7932_F9F1_77FF_B719_4BE7_D299_E344_50B7_A398_A635_0E3C_E805
43	DE28_6B6A_BC86_BF5C_C64C_AAAA_1286_BA76_E38D_F20A_4A24_406F_C7A5_4A05_DAB4_4365
44	3E4D_FF2D_3E39_E78C_A933_DC6D_0FA4_C7F5_0E5B_8EB9_4434_E95D_FEB0_62E7_06A5_F8D4
45	8A02_B5DB_5B51_3CDF_34A9_BC2F_044C_14E9_4AF0_7606_D709_2874_6FE4_CE06_DA65_DF5B
46	30CD_9714_F799_FE16_5E93_D47C_302D_64FB_4A88_856E_BB37_AC8E_48D8_B461_7FA6_CF74
47	FA22_376E_0E66_D8B7_9F83_F31B_C031_990E_D63B_C08A_BE95_B869_2604_D658_FBD2_4D55
48	B2C3_99AF_3402_B24A_B262_D473_0139_22DC_AAFB_F939_5285_F1BC_EE6D_D309_CA74_E0CB
49	2A8A_AF01_5552_08F4_CBB4_3940_7FE4_85C6_94D9_7EBD_330C_0465_01CB_201C_3A70_478B
50	D282_9539_7F66_03A2_1D18_BC33_31B7_DE09_32A1_D9D7_64BD_CBD0_CAAC_048C_EFAA_E737
51	83F0_4604_BBD6_DDDC_184D_AED7_BEB7_E61A_BABD_BBCC_2C90_F352_A0CE_F33F_882C_9157
52	2CC8_39B9_8D11_46D4_7623_392F_7FF6_EE7B_ACDE_6F10_5AA4_3BBE_E03D_2BB8_1794_96F4
53	72A5_6ACF_1A13_8AEC_A28E_234F_B1AB_A339_CD66_5990_4352_271C_A087_0915_6FDA_E22C
54	D70B_2B9A_6E8F_A847_6127_C09A_7607_92B2_AEFC_C3FB_88DC_F2D7_3D14_4C8B_5D43_D571
55	5C4D_B66B_41F6_90E9_F7A8_D7BC_701A_0F06_CA01_2B09_8B4E_8898_6DEE_512C_F0CC_FCEA
56	0000_0A08_C010_0020_0990_0000_0000_0000_9001_0010_1804_0408_0004_0400_2040_2802

Table 142A–5—Test Vector 4 values

Test Vector 4: 10 × 256-bit M parity bits pre-interleaver Omega (L→R)	
Word	bit 255 <---------- bit 0
0	BDB1_0185_C57E_52DA_7BBC_706E_E6C4_0B6A_C2FE_A521_1F16_EFE8_C36A_A078_73C1_ABF1
1	8DF2_8601_7920_0B93_E00D_A86C_DDD7_B754_2A5F_7117_EDA5_4832_C2E7_658C_99D7_E8C1
2	A0D2_326E_02ED_5C67_B43A_49D8_2F5E_E5E2_AB83_E2C9_E145_A8AC_B057_0148_B43B_3CA3
3	37D5_0221_86F9_8DE2_FD9C_73DD_63F3_17B2_A1E2_E96D_366F_8FDC_9611_8EA2_FDDA_C481
4	A225_4E54_8B7B_E30F_80FC_62A7_6587_6287_4E34_5B14_D88B_B64F_945F_B059_C125_64F5
5	CDE0_D7E3_0D13_3A06_1367_B0BF_9CD5_120D_8311_98FD_33F9_8394_F2B8_079C_3C55_7C6A
6	904D_C05B_315C_D4BA_4875_71FD_8BE5_99E0_F57A_3DE7_B734_FE82_6B6C_E74F_CB92_CE09
7	0A29_E39D_7EF1_401B_5E87_4C73_C34E_3D36_3B91_B1A9_66A6_03FC_B429_3507_E109_0DDF
8	6DBD_41A3_2A72_6471_B76A_627F_31F0_4C06_982B_0D97_3D93_F1E8_59C9_DE24_2D8B_9D97
9	759B_73A4_C89D_11B1_15B5_7003_775A_8361_B727_4459_F88C_4A05_73A0_D3E4_1F0A_61DB

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Table 142A–6—Test Vector 5 values

Test Vector 5: 10 × 256-bit *M* parity bits post-interleaver Omega (L→R)	
Word	bit 255 <---------- bit 0
0	E1E8_2EB8_A9B7_DD84_1C48_4ED4_ED0D_0F46_F340_6B32_176A_BDF5_150E_E55F_94FC_D46E
1	0264_C448_630A_5036_5EF7_B360_E184_CAFB_DAF7_267A_1F4F_B94A_4551_2789_0C39_BB79
2	0799_C8E1_9BDD_D580_70A1_7F87_F789_D5EC_4F2F_4A8D_C399_9414_8615_D40A_92C4_0536
3	903A_83E9_32B4_7FFE_F2F6_A2AF_CC77_BF10_5655_FF42_5D42_862C_E0B9_E2B3_EAE8_C0E3
4	4310_6E2F_7F4F_8094_8D05_9B29_7C80_B6B8_E4AF_6984_19ED_50FD_F388_A7A7_5458_A267
5	E9E4_ED75_0EBD_F535_E8B9_0777_98C6_0440_23FB_6583_14C0_BC69_F3F8_70C5_92D1_4326
6	9C79_21CB_D7D1_C638_9A49_4EE7_E7FA_5CFF_DB67_0F48_DEB1_B894_DE90_19A5_D1C6_07A6
7	CAC0_13AF_60DC_81D9_2ACA_BC53_906D_CC66_7EAD_DE07_1F73_902E_53DB_BA03_31A1_CE34
8	5016_8B84_7EDC_87F6_2F95_59CA_EFDC_3DC7_4849_B870_52C4_0510_BD68_9AFD_C8A3_E76B
9	DE80_2A03_320E_E914_4967_D92B_AF17_8666_F30F_1D68_4067_472D_7D11_4708_899D_AA7F

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Annex 145A

(informative)

Resistance and current unbalance

145A.1 Intra pair resistance unbalance

Operation for all PSE and PD Types requires that the intra-pair resistance unbalance be 3% or less. Resistance unbalance is a measure of the difference between the two conductors of a twisted pair in the 100 Ω balanced cabling system. Resistance unbalance is defined as in Equation (145A–1):

$$R_{unb} = \left\{ \frac{(R_{max} - R_{min})}{(R_{max} + R_{min})} \times 100 \right\}_{\%} \quad (145A–1)$$

where

R_{max} is the resistance of the pair conductor with the highest resistance

R_{min} is the resistance of the pair conductor with the lowest resistance

145A.2 Pair-to-pair unbalance overview

Pair-to-pair current unbalance is caused by unequal resistances in a parallel current path of the same polarity. The PSE, the PD, and the link section connecting those independently contribute to unbalance. A system model for the worst-case instance of this is shown in Figure 145A–1.

R_{PSE_min} or R_{PSE_max} common-mode effective resistance is the resistance of the two internal conductors (including the internal components on each conductor) in a powered pair of the same polarity connected in parallel.

$R_{Ch\_unb\_min}$ and $R_{Ch\_unb\_max}$ are respectively the minimum and maximum common-mode link section resistances in the powered pairs of the same polarity from the PSE PI to the PD PI per the model described in Figure 145A–2.

R_{PD_min} and R_{PD_max} are respectively the minimum and maximum common-mode effective PD PI resistances. They account for the effective resistance of the resistive elements, combined with the PD pair-to-pair voltage difference and the effect of system end-to-end pair-to-pair unbalance.

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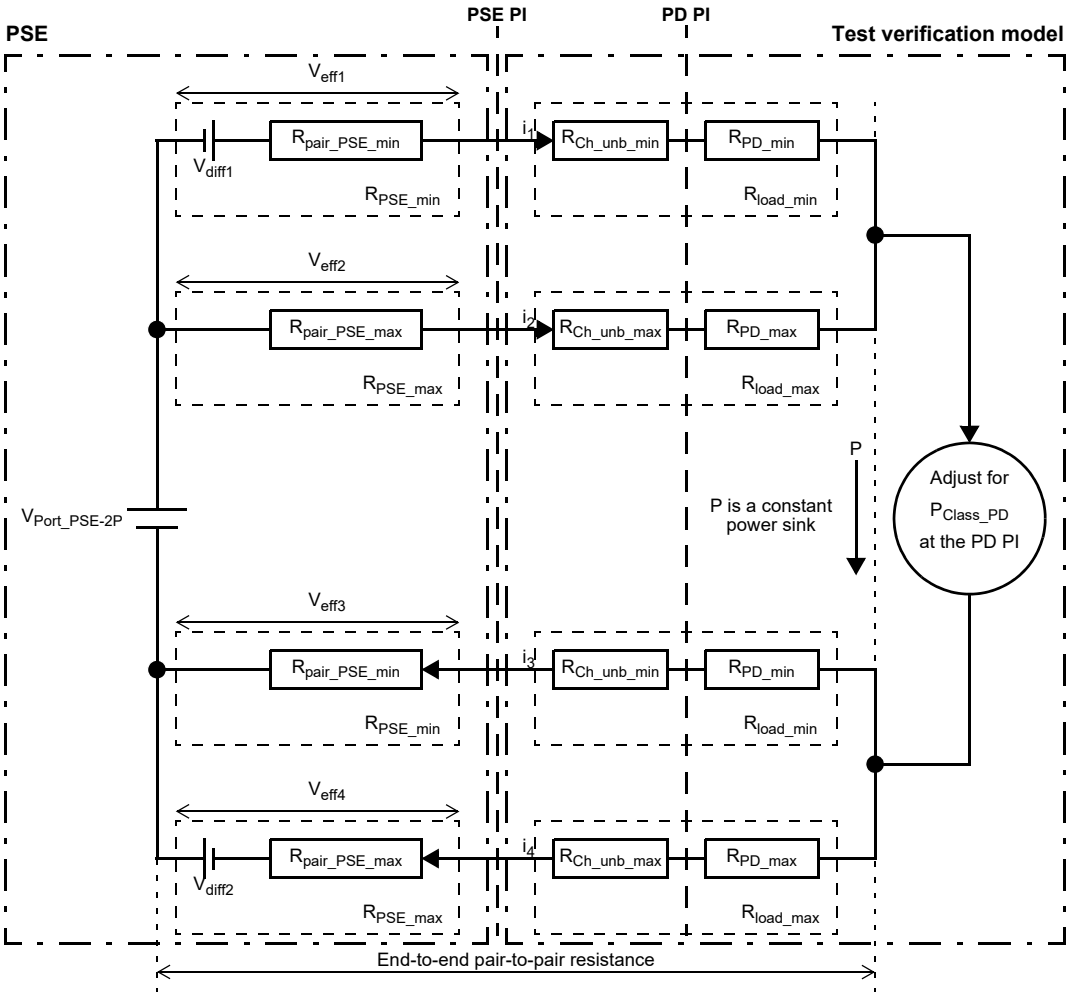
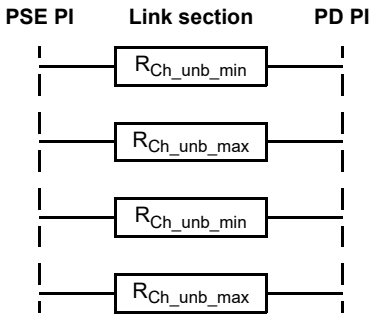


Figure 145A–1—PD current unbalance verification circuit



NOTE—Each resistor in this figure represents two conductors of a pair in parallel.

Figure 145A–2—Common-mode pair-to-pair link section resistance unbalance

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145A.3 Pair-to-pair link section resistance unbalance requirements for 4-pair operation

Operation using 4-pair requires the specification of resistance unbalance between each two pairs of the link section, not greater than 100 mΩ or resistance unbalance of 7 % whichever is a greater unbalance. Resistance unbalance between the link section pairs is a measure of the difference of resistance of the common-mode pairs of conductors used for power delivery. Link section pair-to-pair resistance unbalance is defined by Equation (145A–2):

$$R_{\text{ch\_unb}} = \left\{ \frac{(R_{\text{Ch\_unb\_max}} - R_{\text{Ch\_unb\_min}})}{(R_{\text{Ch\_unb\_max}} + R_{\text{Ch\_unb\_min}})} \times 100 \right\}_{\%} \quad \text{(145A–2)}$$

Operation using 4-pair requires R_{diff} to be less than 100 mΩ or $R_{\text{ch\_unb}}$ to be less than 7 %, whichever results in the greater absolute unbalance. R_{diff} is defined in Equation (145A–3).

$$R_{\text{diff}} = \{R_{\text{Ch\_unb\_max}} - R_{\text{Ch\_unb\_min}}\} \quad \text{(145A–3)}$$

where

$R_{\text{Ch\_unb\_max}}$ is the sum of link section pair components with the highest common-mode resistance from the PSE PI to the PD PI

$R_{\text{Ch\_unb\_min}}$ is the sum of link section pair components with the lowest common-mode resistance from the PSE PI to the PD PI

Link section common-mode resistance is the resistance of the two conductors (including connectors) in a pair, connected in parallel.

The resistance of the common-mode pairs of conductors and connectors $R_{\text{Ch\_unb\_min}}$ and $R_{\text{Ch\_unb\_max}}$ are described by Figure 145A–2.

The values for $I_{\text{Unbalance-2P}}$ and the relation between $R_{\text{PSE\_max}}$ and $R_{\text{PSE\_min}}$, as defined in Equation (145–13), are valid given that $R_{\text{Chan-2P}}$ (see 145.1.3) ranges from 0.2 Ω to 12.5 Ω and that the PD meets 145.3.8.9. In cases where $R_{\text{Chan-2P}}$ is less than 0.2 Ω, or R_{Chan} is less than 0.1 Ω, PSE compliance with $I_{\text{Unbalance-2P}}$ can be evaluated using $R_{\text{load\_min}}$ and $R_{\text{load\_max}}$ both reduced by $0.5 \times R_{\text{Chan-2P}}$. This compliance will require a reduction in the ratio of $R_{\text{PSE\_max}}$ to $R_{\text{PSE\_min}}$ defined in Equation (145–13).

145A.4 PSE resistance and current unbalance

End-to-end pair-to-pair resistance/current unbalance refers to the ratio of current differences in powered pairs of the same polarity to the total 4-pair current. The end-to-end pair-to-pair current unbalance is equal to the end-to-end pair-to-pair effective resistance unbalance which refers to the ratio of effective resistance difference in the powered pairs of the same polarity to the sum of the effective resistance elements of both pairs of the same polarity and is shown by Figure 145A–1. Current unbalance can occur in positive and negative powered pairs when a PSE uses all four pairs to source power to a PD.

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PSE current unbalance requirements need to be met with R_{load_max} and R_{load_min} applied as defined in Equation (145–14), Equation (145–15), and Table 145–18. A compliant unbalanced load, R_{load_min} and R_{load_max}, consists of the link section and PD effective resistances, including the effects (or influence) of system end-to-end unbalance. See Figure 145–21, Figure 145A–1 and Figure 145A–3 for details.

Equation (145–13) is described in 145.2.10.6.1, specified for the PSE, assures that pair-to-pair current unbalance will be met in the presence of all compliant unbalanced loads (R_{load_min} and R_{load_max}) attached to the PSE PI.

Figure 145–21 illustrates the relationship between effective resistances at the PSE PI as defined by Equation (145–13) and R_{load_min} and R_{load_max} as defined by Equation (145–14), Equation (145–15), and Table 145–18. PSE pair-to-pair voltage difference is specified by $V_{Port\_PSE\text{-}2P}$ in Table 145–16.

A method to determine whether R_{PSE_max} and R_{PSE_min} conform to Equation (145–13) is defined in 145A.4.1.

If pair-to-pair balance is actively controlled in a manner that changes effective resistance to achieve balance, then the current unbalance measurement method described in 145.2.10.6.1 should be used.

145A.4.1 Direct R_{PSE} measurement

If there is access to internal circuits, effective resistance may be determined by sourcing current in each path corresponding to maximum P_{Class} operation, and measuring the voltage across all components that contribute to the effective resistance, including circuit board traces and all components passing current to the PSE PI output connection. The effective resistance R_{PSE_min} or R_{PSE_max} is the measured voltage V_{eff}, divided by the current through the path e.g. the effective value of R_{PSE_min} for i_1 is $R_{PSE\_min}=V_{eff1} / i_1$ as shown in Figure 145A–1. R_{PSE_min} and R_{PSE_max} values respectively may be different than $R_{pair\_PSE\_min}$ and $R_{pair\_PSE\_max}$ values.

The R_{PSE_min} or R_{PSE_max} effective resistance verification procedure is as follows:

1) With the PSE powered on and connected to a constant power sink through the elements shown in Figure 145A–1, which is set to $_{PClass\_PD}$ measured at the PD PI, measure the currents i_1, i_2, i_3, and i_4 and the voltages V_{eff1}, V_{eff2}, V_{eff3} and V_{eff4}.
2) Calculate the R_{PSE_min} and R_{PSE_max} values of each pair of the same polarity as follows:
   For the positive pairs:
   $R_1 = R_{PSE\_min} = V_{eff1} / i_1$
   $R_2 = R_{PSE\_max} = V_{eff2} / i_2$
   For the negative pairs:
   $R_3 = R_{PSE\_min} = V_{eff3} / i_3$
   $R_4 = R_{PSE\_max} = V_{eff4} / i_4$
3) Verify that R_{PSE_min} and R_{PSE_max} meet Equation (145–13) on each pair of the same polarity.
4) Repeat steps 1 to 3 with $R_{Ch\_unb\_min}$ and R_{PD_min} exchanged with $R_{Ch\_unb\_max}$ and R_{PD_max}.

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145A.5 PD resistance and current unbalance

$R_{Pair\_PD\_max}$ and $R_{Pair\_PD\_min}$ represent PD common-mode input effective resistance of pairs of the same polarity. Common-mode effective resistance is the resistance of two conductors of the same pair and their other components connected in parallel including the effect of PD pair-to-pair voltage difference of pairs with the same polarity (e.g., $V_{f1} - V_{f3}$). The common-mode effective resistance R_n is the measured voltage $V_{eff\_pd\_n}$, divided by the current through the path as described below and as shown in the example in Figure 145A–3, where *n* is the pair number. PD pair-to-pair voltage difference (e.g. $V_{f1} - V_{f3}$) was limited to 60 mV while generating values for $I_{Unbalance\text{-}2P}$ under worst case conditions.

NOTE—In order to measure the maximum value of $V_{f1} - V_{f3}$, an input current in the range of 1 mA to 10 mA is recommended.

Positive pairs:

$$R_1 = R_{Pair\_PD\_min} = V_{eff\_pd1} / i_1$$
$$R_3 = R_{Pair\_PD\_max} = V_{eff\_pd3} / i_3$$

Negative pairs:

$$R_2 = R_{Pair\_PD\_min} = V_{eff\_pd2} / i_2$$
$$R_4 = R_{Pair\_PD\_max} = V_{eff\_pd4} / i_4$$

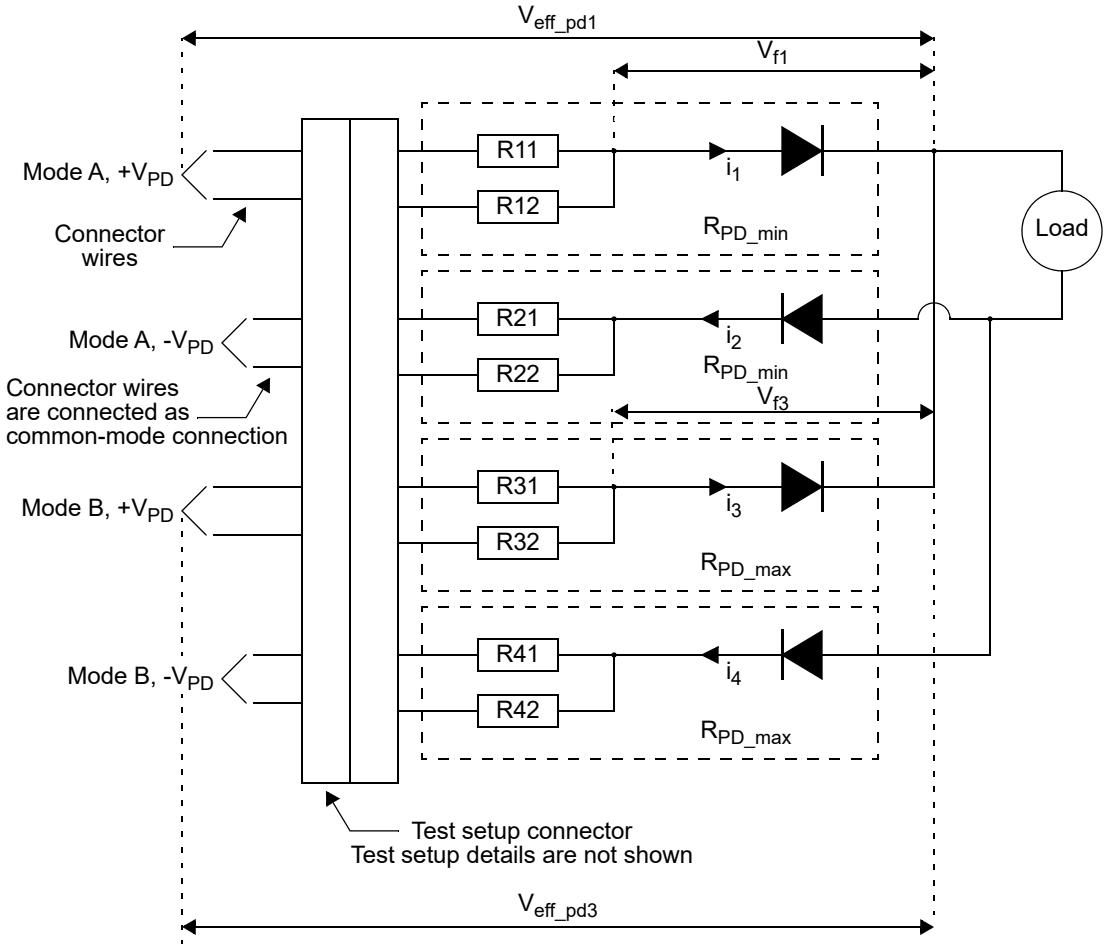

Figure 145A–3—PD resistance unbalance elements overview

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Annex 145B

(informative)

Timing diagrams

The following timing diagrams are provided for informative purpose only.

145B.1 CC_DET_SEQ timing diagrams

Each of the following sample timing diagrams show a PSE performing a sequence of connection check, detection, classification, power up and power on events. A PSE implements one or more of the four defined CC_DET_SEQ sequences based on the results of detection, connection check and 4PID.

When the result of the connection check is dual, the Alternatives are controlled by the semi-independent dual-signature state machine. In this case the detection, classification, and power up are not necessarily synchronized between the Alternatives.

145B.1.1 CC_DET_SEQ=0 timing diagrams

CC_DET_SEQ = 0 is the first of four possible connection check and detection sequences.

Figure 145B–1 illustrates a PSE implementing CC_DET_SEQ=0 when the result of connection check is ‘single’.

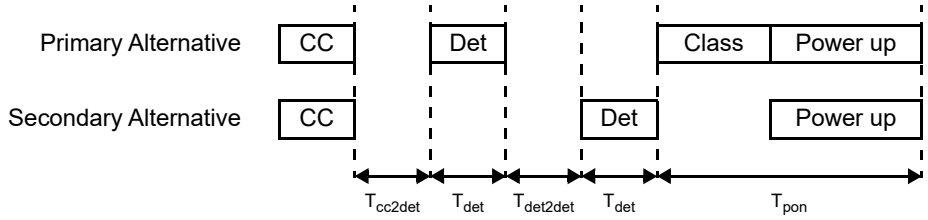

Figure 145B–1—PSE implementing CC_DET_SEQ=0, do_cxn_chk result is single

Figure 145B–2 illustrates a PSE implementing CC_DET_SEQ=0 when the connection check result is dual and Class_4PID_mult_events_sec is TRUE.

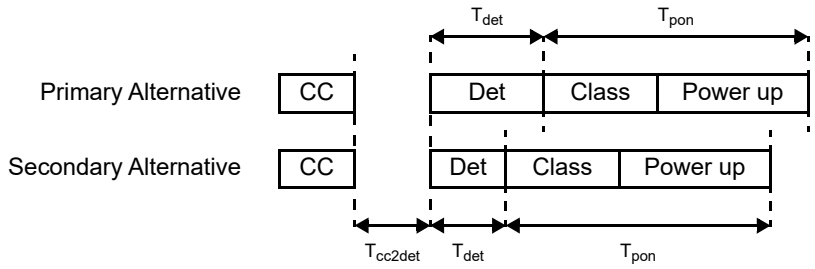

Figure 145B–2—PSE implementing CC_DET_SEQ=0, do_cxn_chk result is dual, quasi-simultaneous power on

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Figure 145B–3 illustrates a PSE implementing CC_DET_SEQ=0 when the connection check result is dual and Class_4PID_mult_events_sec is FALSE.

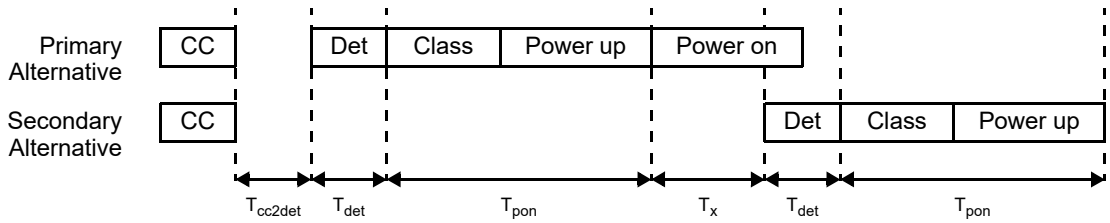

Figure 145B–3—PSE implementing CC_DET_SEQ=0, do_cxn_chk result is dual, staggered power on

145B.1.2 CC_DET_SEQ=1 timing diagrams

CC_DET_SEQ = 1 is the second of four possible connection check and detection sequences.

Figure 145B–4 illustrates a PSE implementing CC_DET_SEQ=1 when the connection check result is single. The power up timing may not be aligned as shown in the figure.

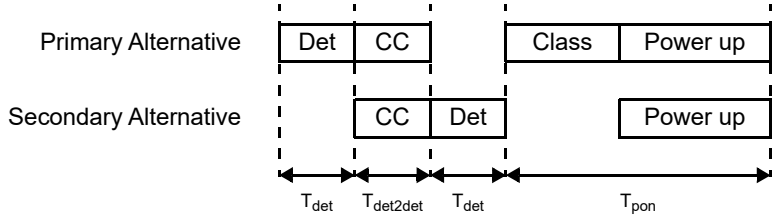

Figure 145B–4—PSE implementing CC_DET_SEQ=1, do_cxn_chk result is single

Figure 145B–5 illustrates a PSE implementing CC_DET_SEQ=1 when the connection check result is dual and class_4PID_mult_events_sec is TRUE.

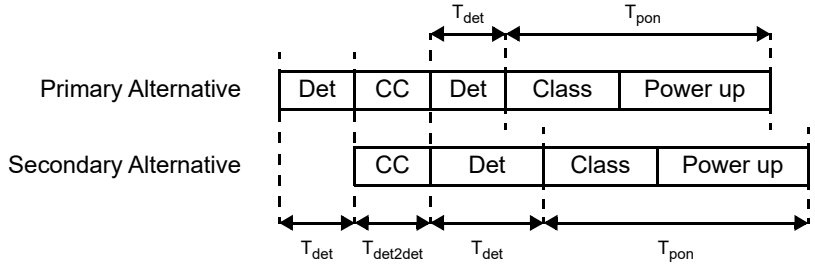

Figure 145B–5—PSE implementing CC_DET_SEQ=1, do_cxn_chk result is dual, quasi-simultaneous power on

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Figure 145B–6 illustrates a PSE implementing CC_DET_SEQ=1 when the connection check result is dual and class_4PID_mult_events_sec is FALSE.

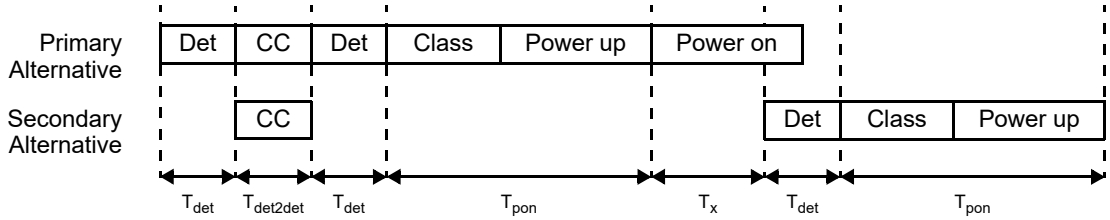

Figure 145B–6—PSE implementing CC_DET_SEQ=1, do_cxn_chk result is dual, staggered power on

145B.1.3 CC_DET_SEQ=2 timing diagrams

CC_DET_SEQ = 2 is the third of four possible connection check and detection sequences.

Figure 145B–7 illustrates a PSE implementing CC_DET_SEQ=2 when the connection check result is single.

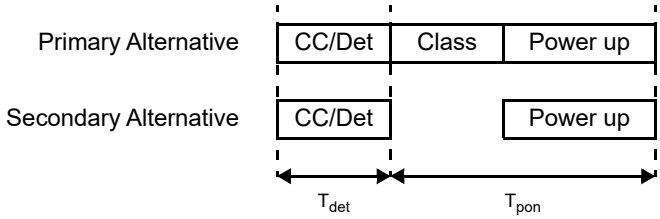

Figure 145B–7—PSE implementing CC_DET_SEQ=2, do_cxn_chk result is single

Figure 145B–8 illustrates a PSE implementing CC_DET_SEQ=2 when the connection check result is dual and pd_4pair_cand is initially TRUE.

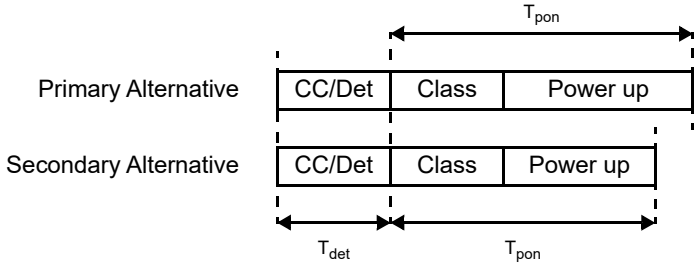

Figure 145B–8—PSE implementing CC_DET_SEQ=2, do_cxn_chk result is dual, simultaneous power on

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Figure 145B–9 illustrates a PSE implementing CC_DET_SEQ=2 when the connection check result is dual and pd_4pair_cand is initially FALSE.

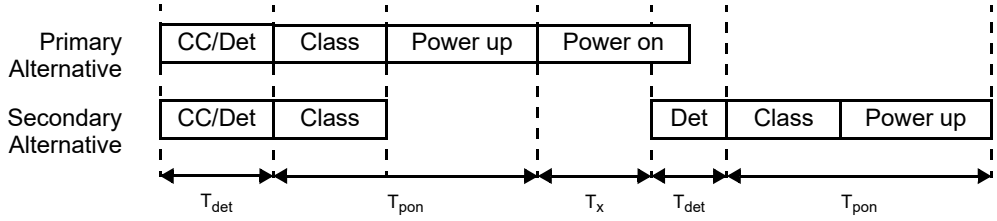

Figure 145B–9—PSE implementing CC_DET_SEQ=2, do_cxn_chk result is dual, staggered power on

145B.1.4 CC_DET_SEQ=3 timing diagrams

CC_DET_SEQ = 3 is the fourth of four possible connection check and detection sequences.

Figure 145B–10 illustrates a PSE implementing CC_DET_SEQ=3 when the connection check result is single.

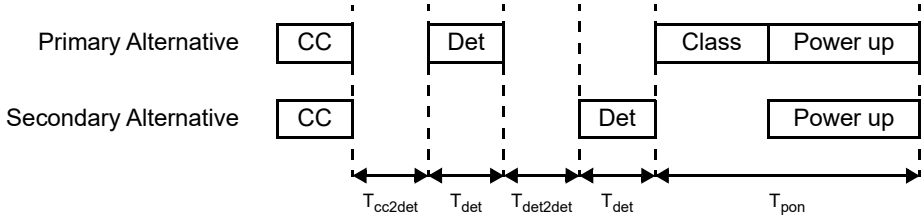

Figure 145B–10—PSE implementing CC_DET_SEQ=3, do_cxn_chk result is single

Figure 145B–11 illustrates a PSE implementing CC_DET_SEQ=3 when the connection check result is dual.

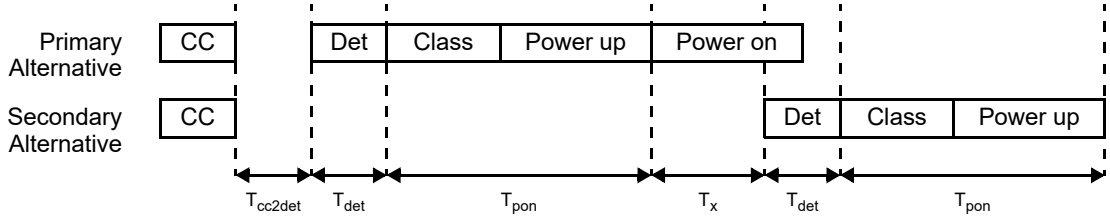

Figure 145B–11—PSE implementing CC_DET_SEQ=3, do_cxn_chk result is dual

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145B.2 PSE Single-Event Physical Layer classification timing diagram

Figure 145B–12 shows a PSE performing a Single-Event Physical Layer classification. No timing relationship between the first class event and the subsequent power on is shown or implied. After T_{pdc} the PSE may transition directly to the power on voltage.

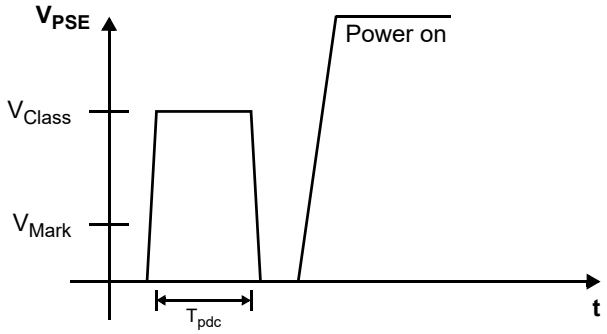

Figure 145B–12—PSE Single-Event Physical Layer classification

145B.3 PSE Multiple-Event Physical Layer classification timing diagram

Figure 145B–13 shows a Type 2 PSE performing a Multiple-Event Physical Layer classification with a Class 4 PD.

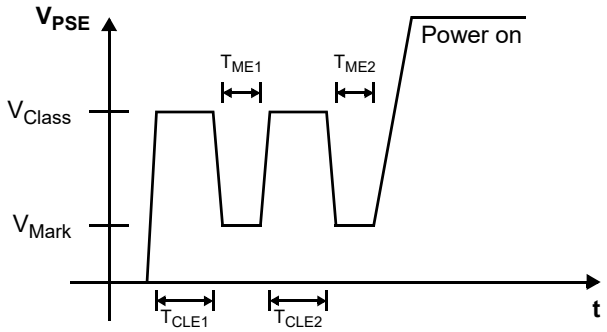

Figure 145B–13—Type 2 PSE, Class 4 PD

Figure 145B–14 shows a Type 4 PSE performing a Multiple-Event Physical Layer classification with a Class 8 PD. Autoclass is not shown in this timing diagram.

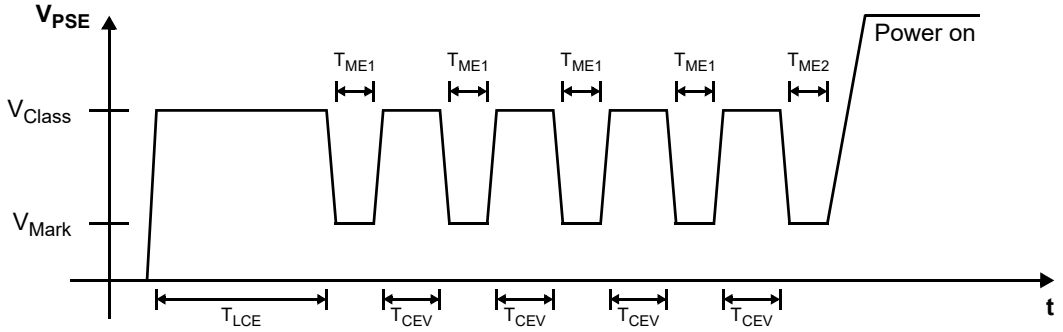

Figure 145B–14—Type 4 PSE, Class 8 PD

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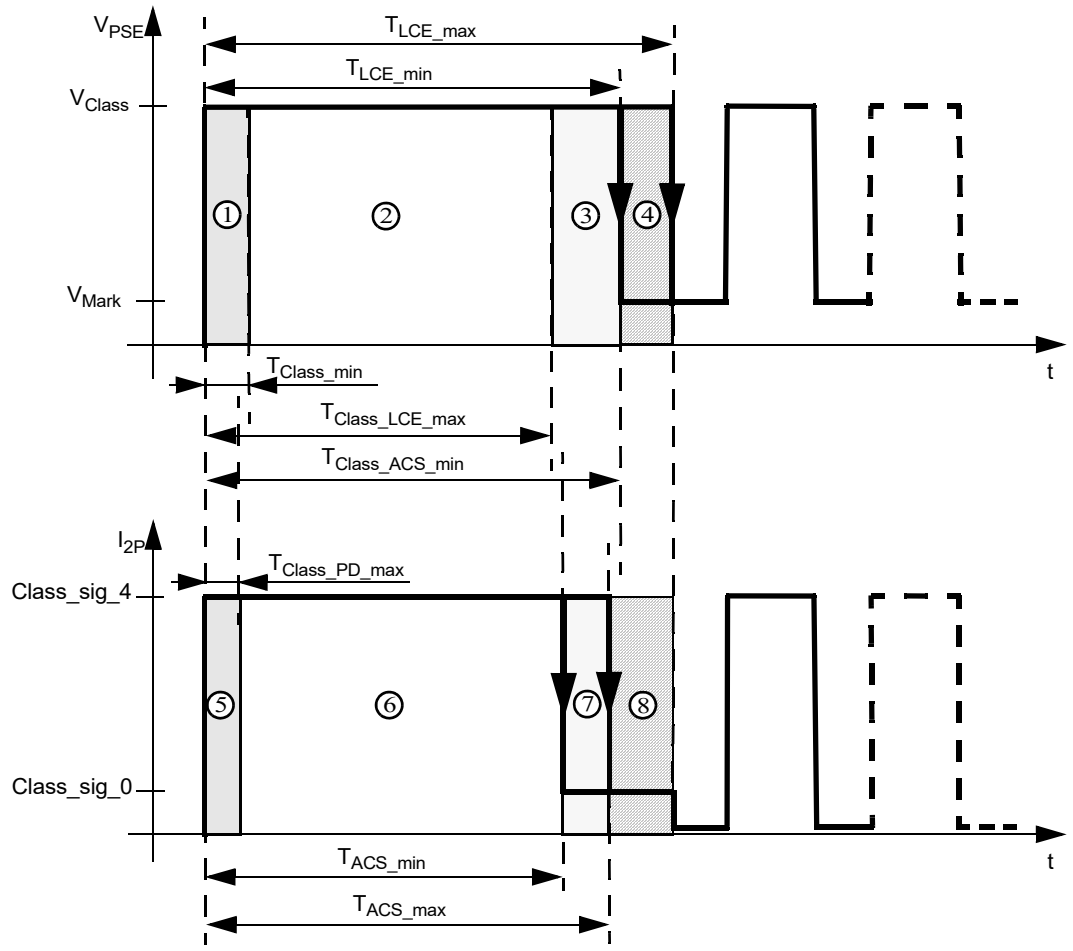
Figure 145B–15 shows a Type 3 or Type 4 PSE performing Multiple-Event Physical Layer classification with Autoclass enabled. The Autoclass-enabled PD responds by requesting an Autoclass measurement.



Legend for numbered areas:

1) PSE may not measure I_{Class}, wait for PD to stabilize class current.
2) PSE measures class signature for first class event.
3) PSE may not measure I_{Class}, PD may switch current level during this time.
4) PSE may measure class signature to check if the PD requests Autoclass.

5) PD to set class current during this window.
6) PD to have valid and stable class current for the first class event.
7) PD may switch current level to class_sig_0 if it requests Autoclass.
8) PD to maintain class signature 0 if it requests Autoclass for the duration of the class event.

Figure 145B–15—Autoclass timing diagram

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Annex 145C

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Power system and parameters

This annex provides additional information for derivation of the system parameters of current and direct current resistance (DCR) given in Table 145–1. This allows analysis of the power delivery system, enabling consideration of applications not operating at the nominal highest current, or maximum DC loop resistance.

145C.1 Constant power

The power system provides constant power to the Powered Device (PD). Powering schematics with the nominal highest current per pair and the maximum DC loop resistance are illustrated in Figure 145C–1 and Figure 145C–2 for a Class 4 PD with a constant power of 25.5 W and in Figure 145C–3 and Figure 145C–4 for a Class 8 PD with a constant power of 71.3 W. Each 4-conductor connection is defined in Clause 145 as a “pairset”.

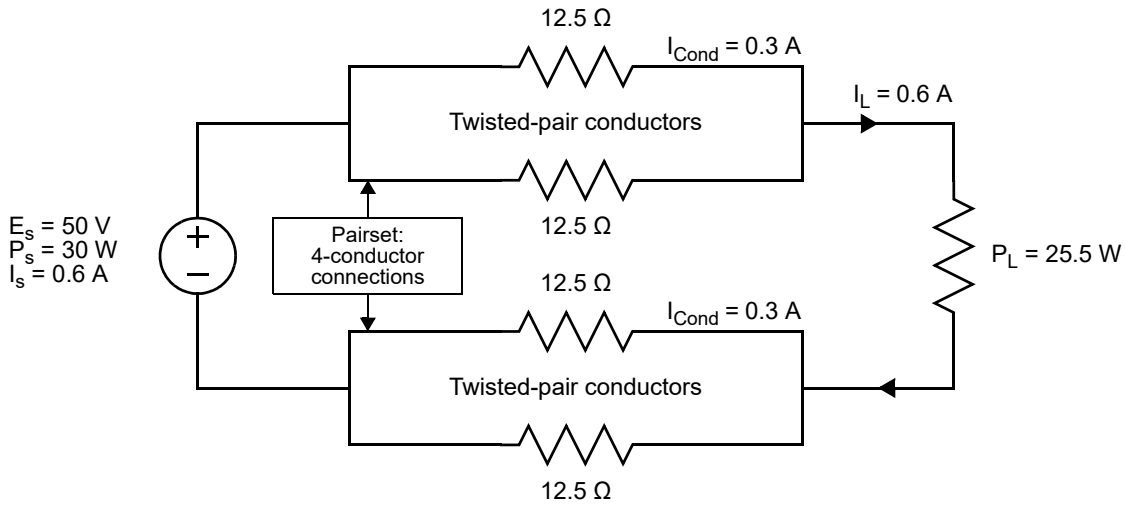

Figure 145C–1—Class 4 PD powering schematic

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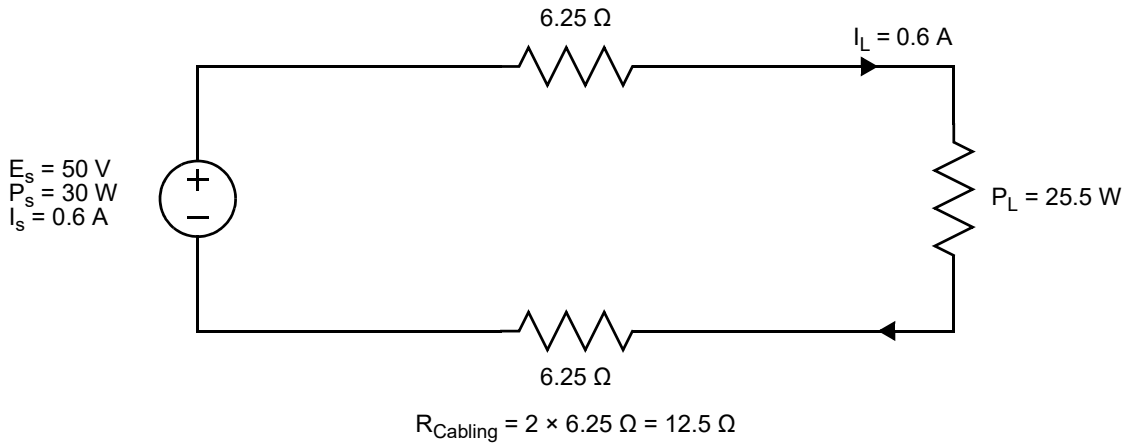

Figure 145C–2—Class 4 PD powering schematic simplified

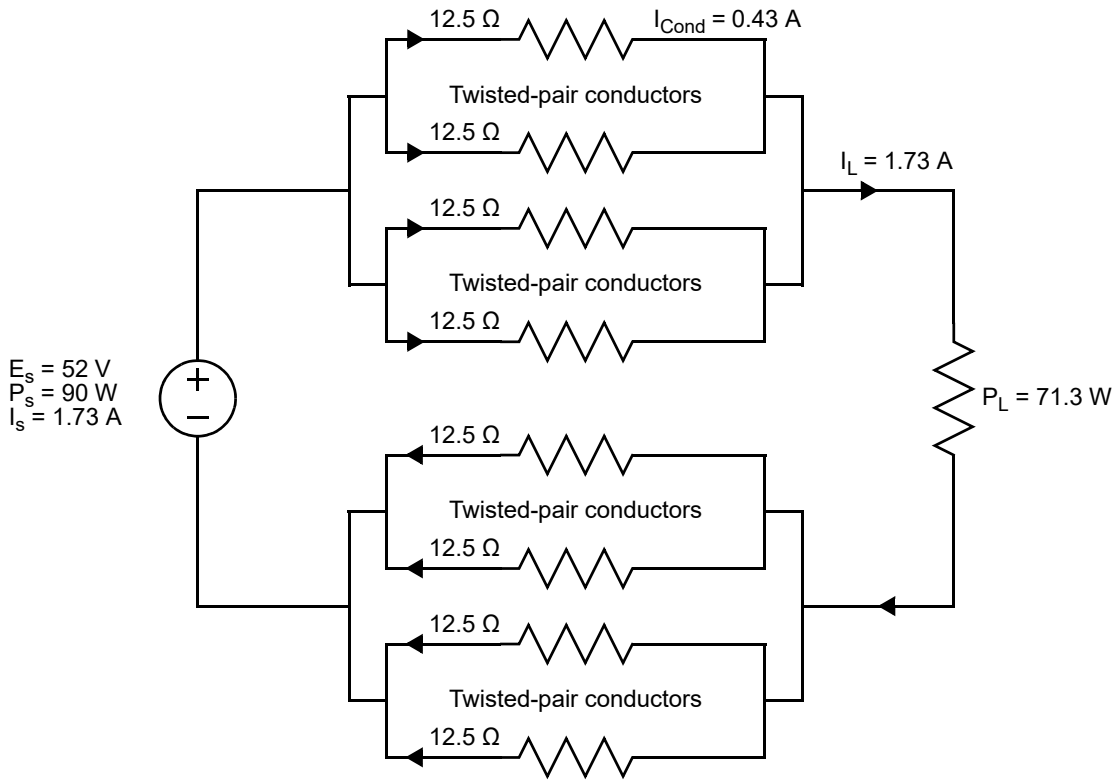

Figure 145C–3—Class 8 PD powering schematic

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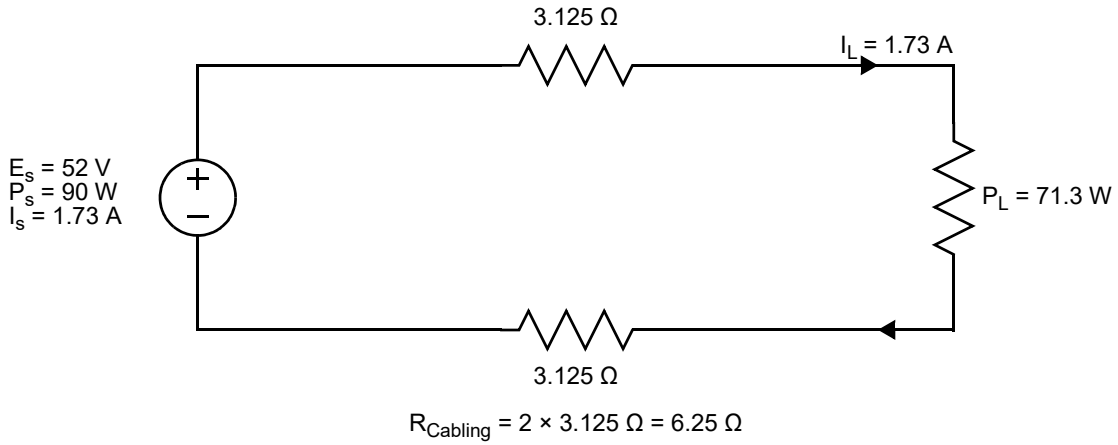

Figure 145C–4—Class 8 powering schematic simplified

145C.2 Current

The value of currents for the example power schematics in Figure 145C–1 through Figure 145C–4 are derived using Equation (145C–1). Note that Equation (145C–1) is of the same form given in Equation (145–3).

$$I_s = \left\{ \frac{E_s - \sqrt{E_s^2 - 4 \times R_{cabling} \times P_L}}{2 \times R_{cabling}} \right\}_A \quad (145C–1)$$

Equation (145C–1) can be applied to all PD Classes. The currents (I_s), calculated using Equation (145C–1), are provided in Table 145C–1 as a function of $R_{Cabling}$ with a constant voltage (52 V) and power (71.3 W) for Class 8.

The maximum value of $R_{Cabling}$ assumes a 100 meter cabling topology along with other worst case elements in the cable plant (see 145C.3). The cable DCR scales linearly such that 50 % of $R_{Cabling}$ is representative of a cabling topology of approximately 50 meters. Note that for a 50 % reduction in the maximum $R_{Cabling}$ (3.125 Ω), equating with approximately 50 meters of cabling, the current decreases from 0.43 A to 0.38 A and the power dissipated in the cabling decreases from 18.7 W to 7.1 W.

Table 145C–1—Current I_s as a function of $R_{Cabling}$

$R_{Cabling}$ (Ω)	I_s (A)	I_{Cond} (A)	$P_{Cabling}$ (W)
0.5	1.39	0.347	0.97
1	1.41	0.352	1.99
1.5	1.43	0.358	3.07
2	1.45	0.363	4.22
2.5	1.48	0.369	5.45

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Table 145C–1—Current I_s as a function of $R_{Cabling}$ *(continued)*

$R_{Cabling}$ (Ω)	I_s (A)	I_{Cond} (A)	$P_{Cabling}$ (W)
3	1.5	0.375	6.76
3.5	1.53	0.382	8.18
4	1.56	0.389	9.71
4.5	1.59	0.397	11.38
5	1.63	0.406	13.20
5.5	1.66	0.416	15.23
6	1.71	0.427	17.5
6.25	1.73	0.433	18.74

145C.3 Direct current resistance (DCR)

The maximum conductor DCR of 12.5 Ω in Figure 145C–1 and Figure 145C–3 is derived from a cabling topology consisting of the following:

— 90 meters of 24 AWG horizontal cable (0.0938 Ω/m)
— 10 meters of 26 AWG patch cord (0.14 Ω/m)
— Four in-line connectors (0.3 Ω per connector)

The DCR of the 90 meters of cable is adjusted for a temperature increase of 45° C from 20° C to 65° C with a 0.4 % increase per degree C (0.1107 Ω/m), shown in Table 145C–2.

Table 145C–2—Cabling conductor DCR with 24 AWG horizontal cable

deg C	90 meters horizontal cable (Ω) (24 AWG)	4 connectors (Ω) (4 × 0.3 Ω per connector)	10 m patch cord (Ω) (26 AWG)	100 m cabling conductor DCR (Ω)
20	8.44	1.2	1.4	11.04
30	8.78	1.2	1.4	11.38
40	9.12	1.2	1.4	11.72
50	9.46	1.2	1.4	12.06
60	9.79	1.2	1.4	12.39
65	9.96	1.2	1.4	12.56

Using 23 AWG and 22 AWG horizontal cable or lower AWG number patch cords reduces the per meter cable DCR; see Table 145C–3.

Using cable smaller than 26 AWG is not recommended in powering applications.

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Table 145C–3—Cable conductor DCR

AWG	Diameter (in)	Resistance per meter (Ω)	Resistance per 100 meter (Ω)	Resistance per 90 meter (Ω)
22	0.025346	0.059	5.9	5.31
23	0.022571	0.0744	7.44	6.7
24	0.0201	0.0938	9.38	8.44

145C.4 Bundled cabling applications

Table 145–1 lists the nominal highest current per pair and the maximum DCR loop resistance. The maximum current is used in ISO/IEC TS 29125, TIA TSB-184A, and the National Electrical Code® (NEC®) (NFPA 70®, 2017 Edition) [B56] to limit the maximum number of 4-pair cables in a bundle. The additional information provided in this Annex will enable considerations for the number of 4-pair cables in a cabling bundle that are not at the nominal highest current or maximum DC loop resistance.

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Annex 146A

(informative)

Guidelines for implementation of the 10BASE-T1L PHY in an intrinsically safe application

The principle of intrinsic safety is based on the limitation of voltage, current, power, capacitance, and inductance of electrical circuits. Within hazardous locations, a circuit following the limits of the intrinsic safety standards will not be able to ignite gas or dust atmospheres in case of a short circuit or any other kind of failure.

The additional requirements to achieve equipment protection by intrinsic safety are described by International Standards (e.g., IEC 60079-11). Possible limits of parameters used for intrinsically safe communication circuits can be derived from these standards. The specification of 10BASE-T1L in Clause 146 is intended to be compatible with implementation of such intrinsically safe systems.

In addition, the PHY implementation has a strong impact on intrinsic safety, while using external and discrete components for intrinsic safety related aspects simplifies the certification process. The following implementation choices can simplify the process for certifying 10BASE-T1L PHYs in intrinsically safe systems:

External termination resistors: These can be used to limit the energy and current to or from the intrinsically safe link segment;

Providing separate high impedance receive pins:
External resistors for current and energy limitation can also be added to the receive path.

Figure 146A–1 and Figure 146A–2 show, in principle, two possible implementations on how to feed power onto an intrinsically safe link segment. The circuits should be seen only as examples. It is in the responsibility of the hardware designer to fulfill all relevant standards (especially IEC 60079-0 and IEC 60079-11, but also others), when implementing devices for the use within intrinsically safe applications.

NOTE—The version shown in Figure 146A–2 may be easier to implement within a PHY IC as the hybrid within the PHY IC does not need to adapt to different external resistor values.

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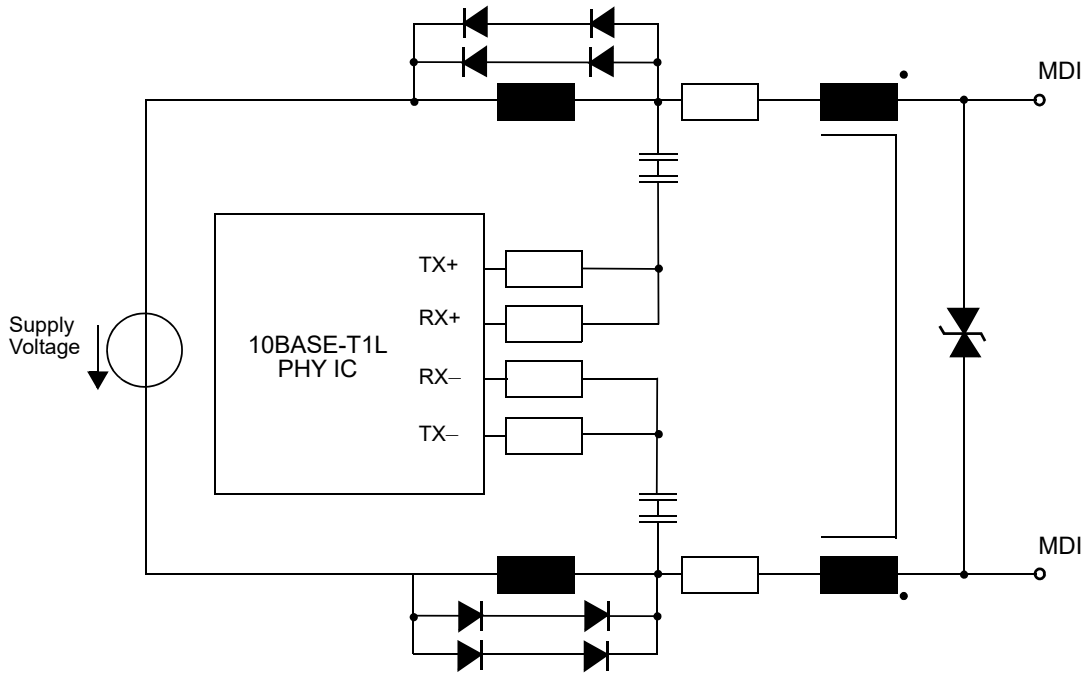

Figure 146A–1—First possible implementation on intrinsically safe power feeding

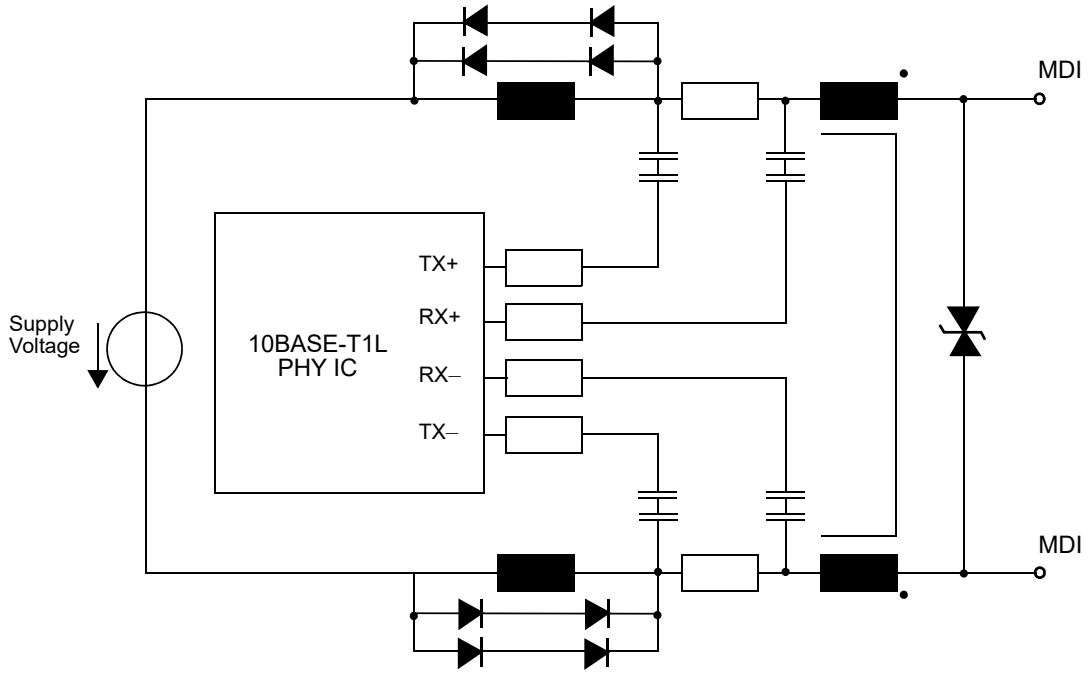

Figure 146A–2—Second possible implementation on intrinsically safe power feeding

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Figure 146A–3 shows, in principle, a possible implementation on how to decouple the power from an intrinsically safe link segment. The circuits should be seen only as examples, and values of the components are implementation and application dependent. It is in the responsibility of the hardware designer to fulfill all relevant standards (especially IEC 60079-0 and IEC 60079-11, but also others), when implementing devices for the use within intrinsically safe applications.

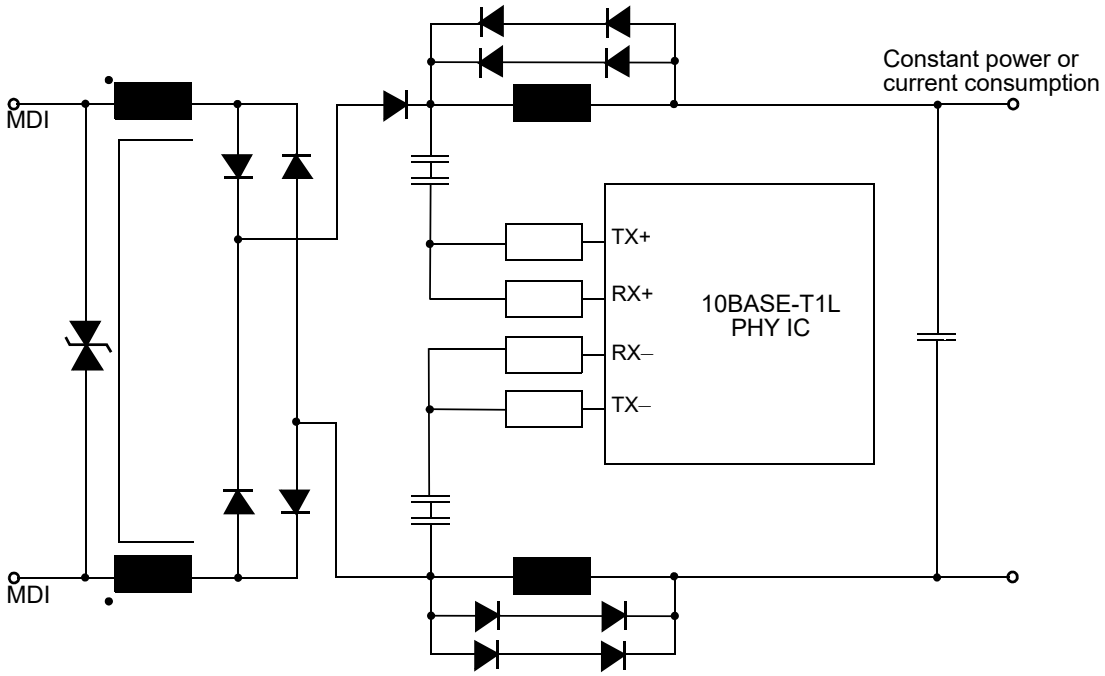

Figure 146A–3—Possible implementation for power decoupling from an intrinsically safe link segment

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Annex 146B

(informative)

Optional power distribution

146B.1 Overview

Annex 146B provides information on the optional powering topologies. The class power requirements are specified in Clause 104.

146B.2 Point-to-point powering topologies

The point-to-point powering topology is defined to enable characterization of the direct current resistance (DCR). The point-to-point powering topology is illustrated in Figure 146B–1.

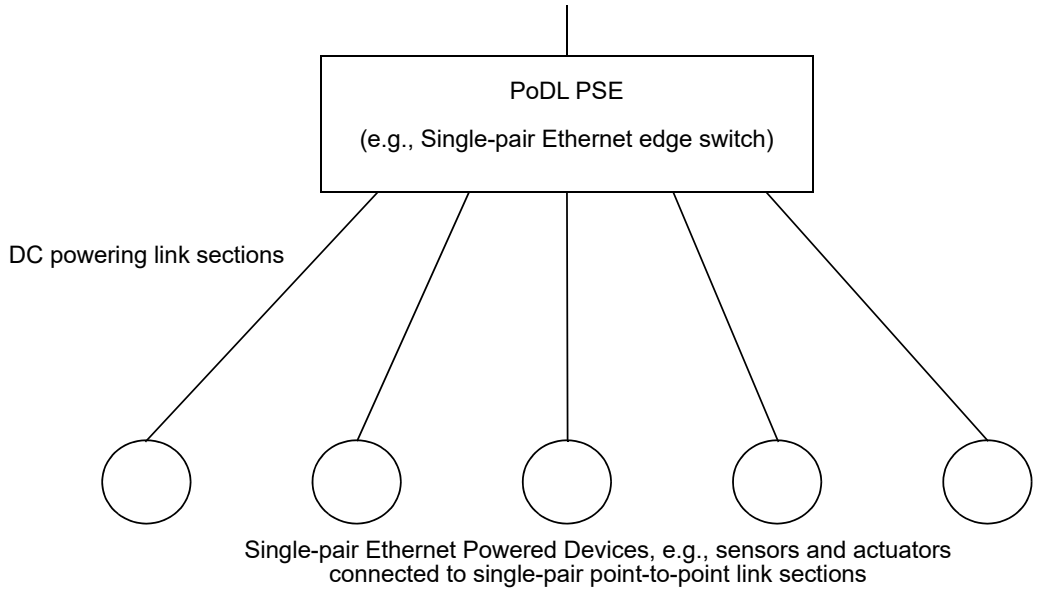

Figure 146B–1—Point-to-point powering topology

The point-to-point link segment DCR characteristics are given in Table 146B–1.

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Table 146B–1—Point-to-point link segment DCR characteristics

Conductor diameter mm (AWG)	Resistance per meter (Ω)	Length at IL limit (m)	Conductor resistance at IL limit (Ω)	Loop resistance at IL limit (Ω)	10 connector DCR (Ω)	Link segment resistance at IL limit (Ω)
1.63 (14)	0.0092	1589	14.67	29.33	1	30.33
1.45 (15)	0.0116	1415	16.47	32.94	1	33.94
1.29 (16)	0.0147	1261	18.50	37.00	1	38.00
1.14 (17)	0.0185	1123	20.78	41.55	1	42.55
1.02 (18)	0.0233	1000	23.33	46.66	1	47.66
0.91 (19)	0.0294	891	26.20	52.40	1	53.40
0.81 (20)	0.0371	793	29.42	58.84	1	59.84
0.72 (21)	0.0468	706	33.04	66.07	1	67.07
0.64 (22)	0.0590	629	37.10	74.19	1	75.19
0.57 (23)	0.0744	560	41.66	83.31	1	84.31
0.51 (24)	0.0938	499	46.78	93.55	1	94.55
0.40 (26)	0.1492	395	58.98	117.96	1	118.96

146B.3 Powered trunk cable topologies

The “powered trunk cable” topology is illustrated in Figure 146B–2. The trunk link section provides power to the single pair field switches. The trunk link section can also interconnect field switches. The spur link sections provides power to the PDs. Powering trunk topologies are considered “engineered”; therefore, DCR characteristics for specified lengths are not given.

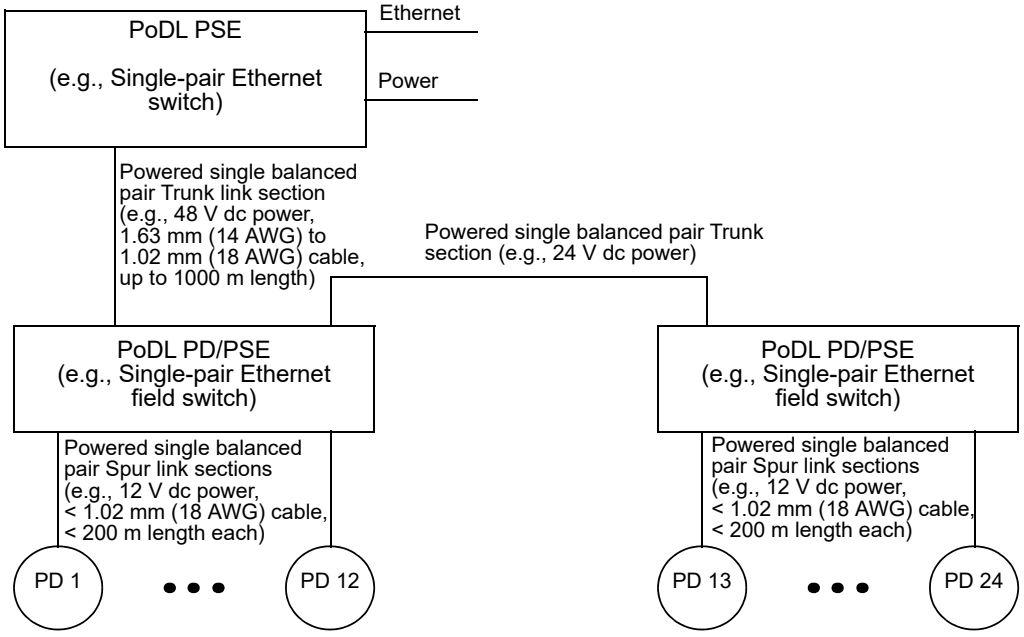

Figure 146B–2—Powered trunk cable topology

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Annex 149A

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Coupling and screening attenuation test methodology

149A.1 Introduction

This annex describes the test methodologies used to measure 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 link segment coupling and screening attenuation specified in 149.7.1.4 and 149.7.1.5.

149A.2 General test conditions

Coupling and screening attenuation are the main parameters for a shielded differential link segment to define its EMC properties. Coupling and screening attenuation are tested as specified in IEC 62153-4-7 using triaxial tube in tube method.

The usable frequency range of the setup may be limited by the dimensions of the triaxial measurement equipment, as higher order modes may occur. IEC 62153-4-7 provides additional information on how to suppress higher order modes in order not to falsify the measurement result.

These test methods are applicable for temperature and humidity as specified by IEC 62153-4-7.

149A.3 Reference cable assembly

The reference cable assembly is intended to be a simplified representation of the components used within a wiring harness. These include cable, PCB connectors, and in-line connectors. In order to reach sufficient accuracy to measure coupling and screening attenuation, the connectors and cable should be matched in terms of balance and shielding.

This topology serves as a common reference to compare link segments made of different components. It also enables the comparison of results from different test houses.

The reference cable assembly has a nominal length of 1.75 m, including one in-line connector and one PCB connector with termination as shown in Figure 149A–1.

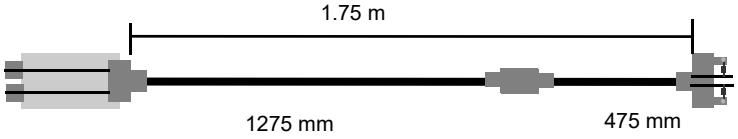

Figure 149A–1—Coupling attenuation reference cable assembly

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149A.4 Measurement setup

Figure 149A–2 shows the reference cable assembly within the triaxial tube in tube method measurement setup.

Additional to the nominal lengths, some length tolerances are allowed. The overall assembly length shall be between 1650 mm and 1800 mm. The exposed cable length within the triaxial tube shall be between 900 mm and 1000 mm. Therefore, the cable length from the measurement fixture to the triaxial tube shall be between 650 mm and 900 mm. This allows easy handling while keeping the influence of the feeding cable section on insertion loss and balance low. In addition, both ends of the cable shield should be connected to the reference plane using techniques suitable for RF applications in the frequency range of interest, see 149.7.1.4 and 149.7.1.5,when implementing cable assemblies in vehicles.

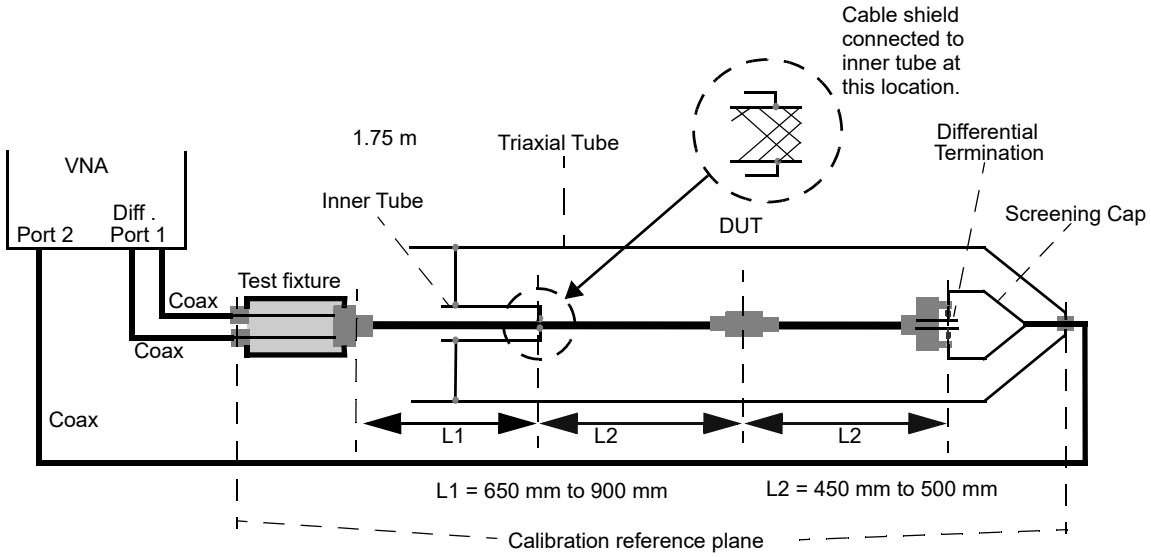

Figure 149A–2—Coupling attenuation reference cable assembly measurement setup

A 3-port vector network analyzer (VNA) measurement setup shall be used without baluns. Two ports of the VNA act as generator and the third port is used as single-ended receiver. For coupling attenuation measurements, the generator port-pair is operated in differential mode. For screening attenuation measurements, the generator port-pair is operated in common mode.

The measurement setup shall be optimized with respect to balance. This includes VNA, accurate and well-balanced test fixture and termination designs, as well as the use of phase stable coaxial cables.

The termination shall be nominal 100 Ω in differential mode and 25 Ω in common mode. The requirements on the single-ended termination of every conductor of the differential pair shall be 50 Ω ± 1% to ground. The two resistors of the differential pair shall be matched to within ±0.1 Ω at DC. The resistors need to be suitable for RF applications in the frequency range under test.

The measurement shall include the transition from the MDI connector to the PCB. Therefore, the termination resistors shall be placed between the signal conductors and ground of a termination housing or equivalent termination fixture as shown in Figure 149A–3. Termination resistors shall not be placed inside the connector in order to omit the transition to the PCB. The termination housing shall be shielded and cover the termination resistors and any signal conductors placed on the bottom of the PCB.

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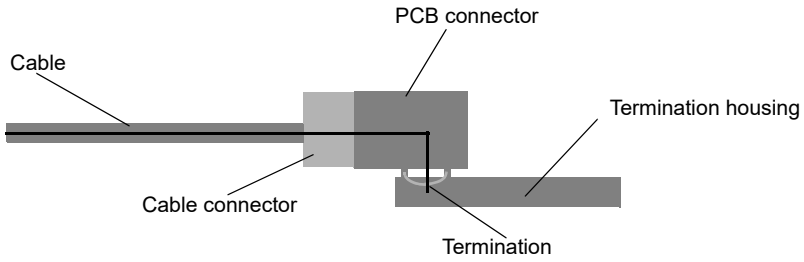

Figure 149A–3—PCB connector and termination

For connectors that provide an additional shield contact from the connector housing to a shielded enclosure, the reference plane at the MDI connector side may be set at the point where the EMC seal is attached. In this case, the connector housing and the transition to the PCB should not be part of the measurement but within the shield cap referenced in Figure 149A–4.

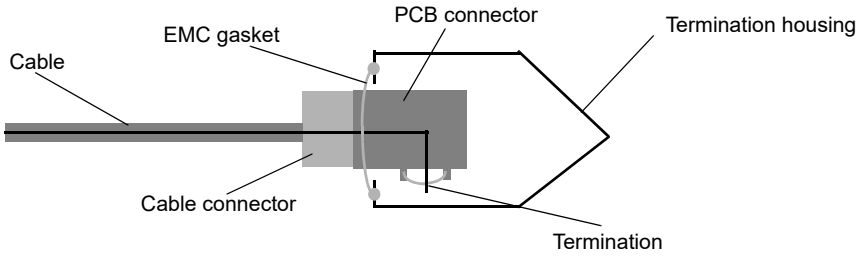

Figure 149A–4—PCB connector with EMC gasket and termination

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149A.5 Protocol implementation conformance statement (PICS) proforma for Annex 149A, Coupling and screening attenuation test methodology[324]

149A.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 149A, Coupling and screening attenuation test methodology, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

149A.5.2 Identification

149A.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

149A.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2022, Annex 149A, Coupling and screening attenuation test methodology
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2022.)	

Date of Statement	

[324] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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149A.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
SDLS	Shielded differential link segment	149A.2		M	Yes [ ]

149A.5.4 PICS proforma tables for Coupling and screening attenuation test methodology

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	The overall assembly length shall be between 1650 mm and 1800 mm.	149A.4		M	Yes [ ]
TM2	The exposed cable length within the triaxial tube shall be between 900 mm and 1000 mm.	149A.4		M	Yes [ ]
TM3	The cable length from the measurement fixture to the triaxial tube shall be between 650 mm and 900 mm.	149A.4		M	Yes [ ]
TM4	A 3-port vector network analyzer (VNA) measurement setup shall be used without baluns.	149A.4		M	Yes [ ]
TM5	The measurement setup shall be optimized with respect to balance.	149A.4		M	Yes [ ]
TM6	The termination shall be nominal 100 Ω in differential mode and 25 Ω in common mode.	149A.4		M	Yes [ ]
TM7	The requirements on the single ended termination of every conductor of the differential pair shall be 50 Ω ± 1% to ground.	149A.4		M	Yes [ ]
TM8	The two resistors of the differential pair shall be matched to within ±0.1 Ω at DC.	149A.4		M	Yes [ ]
TM9	The measurement shall include the transition from the MDI connector to the PCB.	149A.4		M	Yes [ ]
TM10	The termination resistors shall be placed between the signal conductors and ground of a termination housing or equivalent termination fixture as shown in Figure 149A–3.	149A.4		M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
TM11	Termination resistors shall not be placed inside the connector in order to omit the transition to the PCB.	149A.4		M	Yes [ ]
TM12	The termination housing shall be shielded and cover the termination resistors and any signal conductors placed on the bottom of the PCB.	149A.4		M	Yes [ ]

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Annex 149B

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OAM status

149B.1 Purpose

This annex describes a suggested assignment of the OAM status bits for use with the Clause 149 MultiGBASE-T1 PHYs. Suggested bit behaviors, shown in state diagrams, and bit assignments in the OAM frame are detailed in this annex for informative purposes to enable consistent use of the OAM channel. Use of these specific assignments and the behaviors described by the state diagrams is implementation dependent.

149B.2 MultiGBASE-T1 OAM status structure

Each MultiGBASE-T1 OAM frame includes a four-octet MultiGBASE-T1 OAM status message. The status bits transmitted in the MultiGBASE-T1 OAM status message represent the state of health of the transmitting device. The information in these bits should be filled automatically, in an implementation-dependent way, rather than through the management entity.

This information is loaded to registers 3.2318 and 3.2319 for transmission, see 45.2.3.83. The information received from the link partner is read from registers 3.2320 and 3.2321, see 45.2.3.84.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Symbol 10	Reserved	1	Status valid	Power supply warning	Internal temp warning	No MAC messages warning	Degraded link segment	Polarity inversion	Clear REC	REC cleared
Symbol 11	Reserved	1	Vendor-specific field <7:0>							
Symbol 12	Reserved	1	REC<7:0>							
Symbol 13	Reserved	1	REC<15:8>							

Figure 149B–1—MultiGBASE-T1 OAM status

149B.3 MultiGBASE-T1 status message data

The MultiGBASE-T1 status message is shown in Figure 149B–1. OAM<*x*><*y*> refers to symbol *x*, bit *y* of the BASE-T1 OAM frame. Reserved fields should be set to 0.

The definitions that follow are from the transmitting device's point of view.

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149B.3.1 MultiGBASE-T1 status valid

MultiGBASE-T1 status valid is indicated in OAM<10><7>.

— 0: Current OAM frame does not contain valid OAM status data, OAM<10><6:2>.

— 1: Current OAM frame contains valid OAM status data, OAM<10><6:2>.

149B.3.2 Power supply warning

Power supply warning is indicated in OAM<10><6>.

This status bit indicates the state of the local power supply(ies). The definitions of good and near the limit are implementation dependent. It is recommended that this status is set for a minimum of 100 ms.

— 0: Local PHY power supply(ies) is good.

— 1: Local PHY power supply(ies) is near the limit.

149B.3.3 Internal temperature warning

Internal temperature warning is indicated in OAM<10><5>.

This status bit indicates the internal temperature of the PHY. The definitions of good and near the limit are implementation dependent. It is recommended that this status is set for a minimum of 100 ms.

— 0: Local PHY internal temperature is good.

— 1: Local PHY internal temperature is near the limit.

149B.3.4 No MAC messages warning

No MAC messages warning is indicated in OAM<10><4>.

This status bit indicates transmit data is not being received from the MAC. It is recommended that this status is set for a minimum of 100 ms.

— 0: PHY is receiving valid transmit messages from the MAC.

— 1: PHY is not receiving valid transmit messages from the MAC.

149B.3.5 Degraded link segment

Degraded link segment is indicated in OAM<10><3>.

This status is set to indicate the status of the link segment. The definitions of good and degraded are implementation dependent. It is recommended that this status is set for a minimum of 100 ms.

— 0: Link segment is good.

— 1: Link segment is degraded.

149B.3.6 Polarity inversion

Polarity inversion is indicated in OAM<10><2>.

This status is set to indicate the conductors of the pair are swapped and the PHY has accounted for this.

— 0: No polarity inversion detected.

— 1: Polarity inversion detected.

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149B.3.7 Vendor-specific field

Vendor-specific field <7:0> is indicated in OAM<11><7:0> and may be used to convey a vendor defined data field.

149B.3.8 Clear REC

Clear REC is indicated in OAM<10><1>.

This status is set to indicate the link partner should clear the receive error counter (REC) in OAM<13:12><7:0>.

— 0: Do not clear REC.

— 1: Clear REC.

149B.3.9 REC cleared

REC cleared is indicated in OAM<10><0>.

This status is set to indicate the REC (in OAM<13:12><7:0>) has been cleared.

— 0: REC has not been cleared and is counting errors.

— 1: REC has been cleared, set to 0x0000, and has resumed counting errors.

149B.3.10 Receive error counter (REC)

REC<15:0> is indicated in OAM<13:12><7:0>.

This two-byte symbol indicates the number of RS-FEC frame block errors, both correctable and uncorrectable, that have been seen by the receiver since the REC was last cleared. This counter should be cleared when clear REC (OAM<10><1>) is received as 1. If the counter reaches 0xFFFF, it stays at 0xFFFF until cleared by clear REC. See Figure 149B–2 and Figure 149B–3 for additional details on the behavior of this counter in conjunction with clear REC and REC cleared.

149B.4 Detailed functions and state diagrams

149B.4.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, counters, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5, along with the extensions described in 145.2.5.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

149B.4.2 State diagram parameters

149B.4.2.1 Variables

mr_rx_rec

The number of RS-FEC block errors, both correctable and uncorrectable, reported by the link partner.

Values:

The value can be any integer from 0 to 65 535, inclusive.

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mr_rx_rec_cleared
: Indicates whether the link partner has cleared its REC.
Values:
FALSE: Link partner REC counter has not been cleared.
TRUE: Link partner REC counter has been cleared.

mr_tx_rec_cleared
: Indicates whether the local REC counter has been cleared.
Values:
FALSE: REC counter has not been cleared.
TRUE: REC counter has been cleared.

mr_rx_clear_rec
: Request from the link partner to clear the REC counter.
Values:
FALSE: Link partner is not requesting the REC counter be cleared.
TRUE: Link partner is requesting the REC counter be cleared.

mr_tx_clear_rec
: Request to clear the REC counter in the link partner.
Values:
FALSE: Don’t send request to link partner to clear their REC counter.
TRUE: Send request to link partner to clear their REC counter.

rf_valid
: Defined in 149.3.7.2.2.

149B.4.2.2 Counters

mr_tx_rec
: A count of received RS-FEC block errors, both correctable and uncorrectable.
Values:
The value can be any integer from 0 to 65 535, inclusive.

149B.4.2.3 Messages

RX_FRAME
: Defined in 149.3.7.2.6.

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149B.4.2.4 State diagrams

The clear REC state diagram is shown in Figure 149B–2, and the request REC clear state diagram is shown in Figure 149B–3.

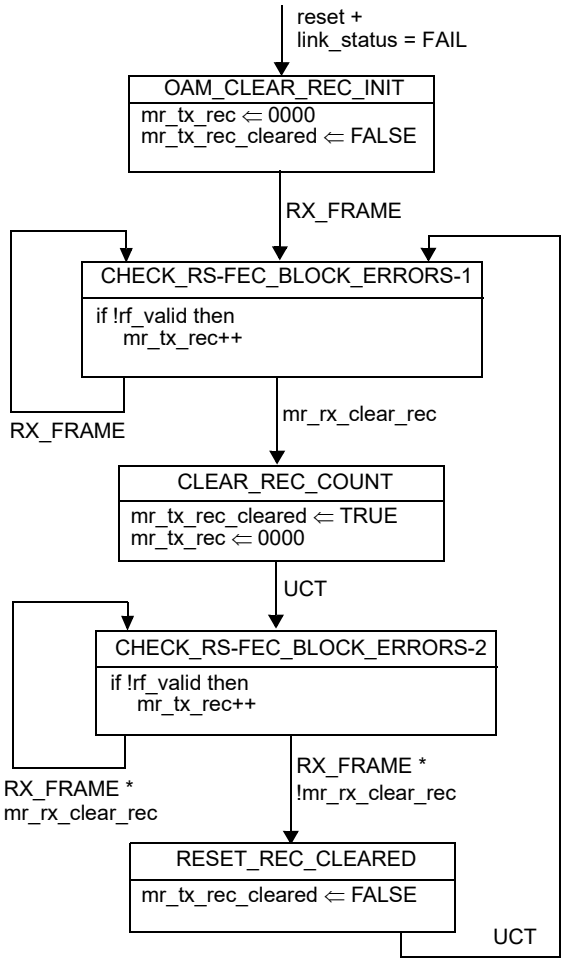

Figure 149B–2—Clear REC state diagram

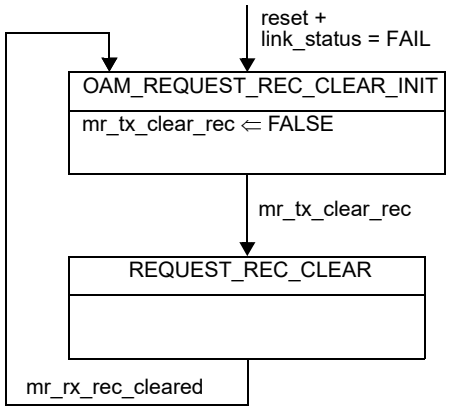

Figure 149B–3—Request REC clear state diagram

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Annex 149C

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Tx Function to Rx function channel characteristics

149C.1 Overview

Annex 149C provides information on insertion loss and return loss parameters of the channel defined between Tx function and Rx function illustrated in Figure 149C–1.

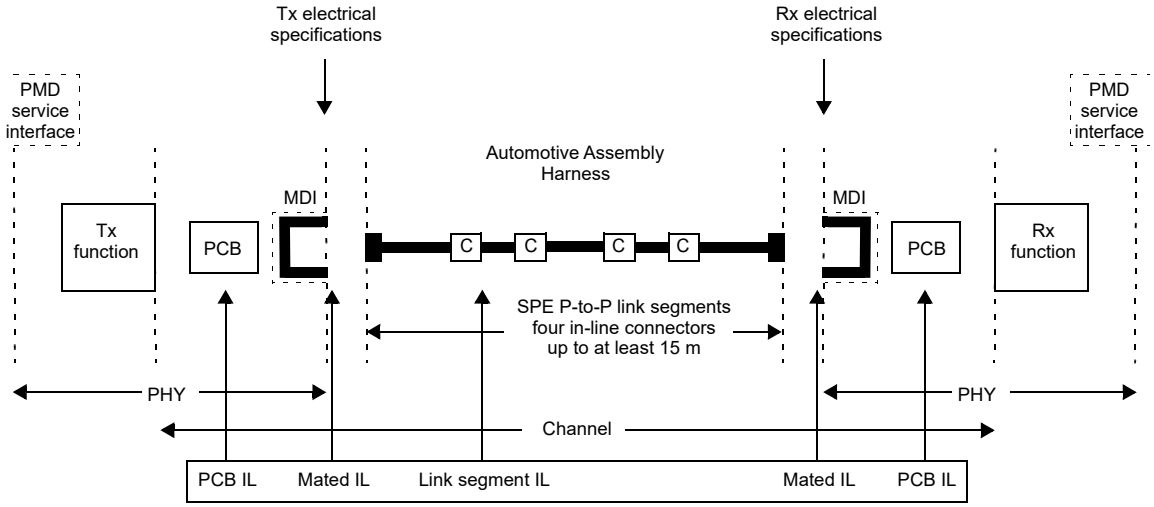

Figure 149C–1—Channel Tx function to Rx function

149C.2 Differential printed circuit board trace loss

The recommended maximum and minimum printed circuit board trace insertion losses are as specified in Equation (149C–1) and Equation (149C–2), respectively.

$$IL_{\mathrm{PCB(76.2mm)}} = \left(0.0071 \times \sqrt{\frac{f}{1000}} + 0.0045 \times \frac{f}{1000}\right) \times 76.2 \text{ (dB)} \quad \text{(149C–1)}$$

$$IL_{\mathrm{PCB(25.4mm)}} = \left(0.0071 \times \sqrt{\frac{f}{1000}} + 0.0045 \times \frac{f}{1000}\right) \times 25.4 \text{ (dB)} \quad \text{(149C–2)}$$

where

f is the frequency in MHz; $1 \le f \le F_{\max}$

$$F_{\max} = 4000 \times S \quad \text{(149C–3)}$$

See Table 149–1 for the definition of *S*.

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149C.3 Channel insertion loss

The channel topology with the 76.2 mm PCB insertion loss is determined using Equation (149C–4), Equation (149C–5), and Equation (149C–6).

$$IL_{\text{channel}} = 2 \times IL_{\text{PCB(76.2mm)}} + 2 \times IL_{\text{MDI}} + IL_{\text{LinkSegment}} \quad (149C–4)$$

$$IL_{\text{MDI}} = 0.1 \times \sqrt{\frac{f}{1000}} \quad (149C–5)$$

$$IL_{\text{LinkSegment}} = 0.002 \times f + 0.68 \times f^{0.45} \quad (149C–6)$$

where

f is the frequency in MHz; $1 \le f \le F_{\max}$

$F_{\max}$ is defined by Equation (149C–3)

The 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs utilize 4-level pulse amplitude modulation (PAM4) transmitted at 1406.25 MBd, 2812.5 MBd, and 5625 MBd rates, respectively. The channel insertion loss values are given in Table 149C–1 at the specified bandwidth for each PHY type.

Table 149C–1—Channel insertion loss for each PHY type

PHY	Rate MBd	Bandwidth (MHz)	$IL_{\text{PCB(76.2mm)}}$ (dB)	$IL_{\text{LinkSegment}}$ (dB)	IL_{MDI} (dB)	IL_{channel} (dB)
2.5GBASE-T1	1406.25	703.125	0.6948	14.3982	0.084	15.955
5GBASE-T1	2812.5	1406.25	1.1238	20.56	0.119	23.045
10GBASE-T1	5625	2812.5	1.8717	29.8688	0.168	33.948

149C.4 Channel return loss

The channel topology between Tx function and Rx function illustrated in Figure 149C–2 consists of the Tx function to MDI, the link segment, and the MDI to Rx function. The channel return loss can be modeled as a concatenation of the Tx function to MDI return loss, the link segment return loss, and the MDI to Rx function return loss.



Figure 149C–2—Tx/Rx function channel topology

149C.4.1 Tx/Rx function to MDI return loss

An example of an implementation of a Tx/Rx function to MDI topology is given in Figure 149C–3 and Figure 149C–4 with associated parameter values given in Table 149C–2. The implementation enables MDI return loss to be considered as a function of PHY termination impedances, PCB impedances, PCB trace

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lengths (insertion loss), external ESD clamp capacitances, and PoDL inductances. The MDI return loss specified in 149.8.2.1 was developed using the example implementation.

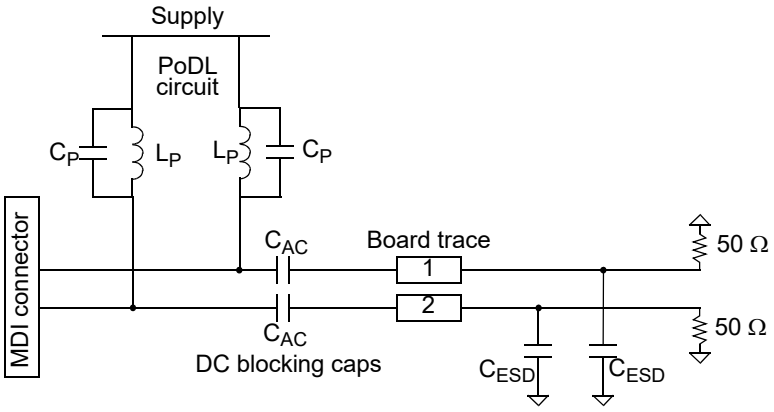

Figure 149C–3—Example implementation MDI to Tx function

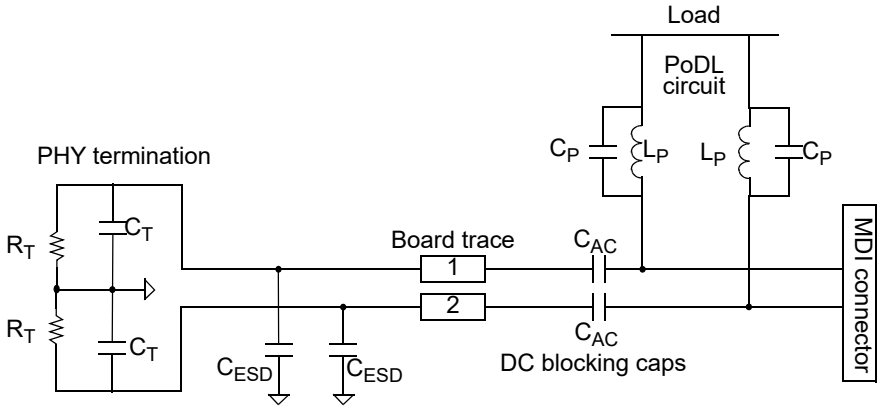

Figure 149C–4—Example implementation Rx function to MDI

Table 149C–2—Analysis parameters and values

Element	Unit	Minimum	Nominal	Maximum
R_T	Ω	45	50	55
Z_O	Ω	45	50	55
C_T	pF	—	0.1	—
L_P	μH	—	4.7	—
C_P	pF	—	0.18	—
C_{ESD}	pF	—	0.4	—
C_{AC}	nF	—	10	—

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149C.4.2 Link segment return loss

Link segment return loss can be modeled as a two-port ladder network, as shown in Figure 149C–5 with sections consisting of cable (Z_{cab}) and connector impedances (Z_{con}).

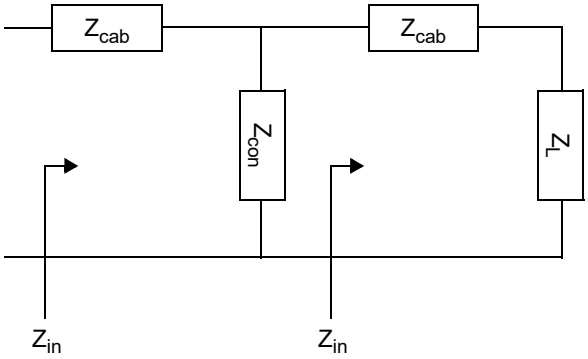

Figure 149C–5—Two–port ladder network

The return loss is derived from the input impedance of the ladder network using Equation (149C–7) and Equation (149C–8). The input impedance is derived using Equation (149C–9) through Equation (149C–12) applied recursively to each section.

$$RL = 20\log_{10}|\Gamma| \tag{149C–7}$$

$$\Gamma = \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \tag{149C–8}$$

$$Z_{in} = Z_o \frac{Z_L + Z_o \tanh(\gamma l)}{Z_o + Z_L \tanh(\gamma l)} \tag{149C–9}$$

$$\gamma = \alpha + j\beta \tag{149C–10}$$

$$\alpha = \frac{\text{Attenuation (dB/m)}}{20\log_{10}(e)} \tag{149C–11}$$

$$\beta = \frac{\omega}{v} \text{ radians/m} \tag{149C–12}$$

where

Z_s is the source impedance
Z_o is the cable (Z_{cab}) or connector (Z_{con}) impedance
Z_L is the initial and recursive impedance
l is the length in m
ω is the angular frequency in radians/s
v is the phase velocity ($c/\sqrt{\text{dielectric constant}}$) in m/s

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149C.4.3 Channel return loss concatenation

The return loss for a channel can be modeled as a concatenation of the Tx function to MDI return loss, the link segment return loss, and the MDI to Rx function return loss using the method in 93A.1.2.1.

149C.5 Coupling between ports on multiport designs

When multiple MultiGBASE-T1 PHYs are implemented on the same board, care should be taken to avoid coupling between ports. The coupling between adjacent ports on a multiport MDI connector or between adjacent balanced pairs is recommended to be approximately the same level, but no greater, than that specified for power sum alien near end crosstalk specified in Equation (149–25).

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Annex 154A

(informative)

Examples of 100GBASE-ZR compliant DWDM black links

154A.1 Introduction

In implementations of the DWDM black link for 100GBASE-ZR, the channels supporting the full duplex links may be implemented on one fiber per direction, as illustrated in Figure 154A–1, or implemented on one fiber for both directions, as illustrated in Figure 154A–2.

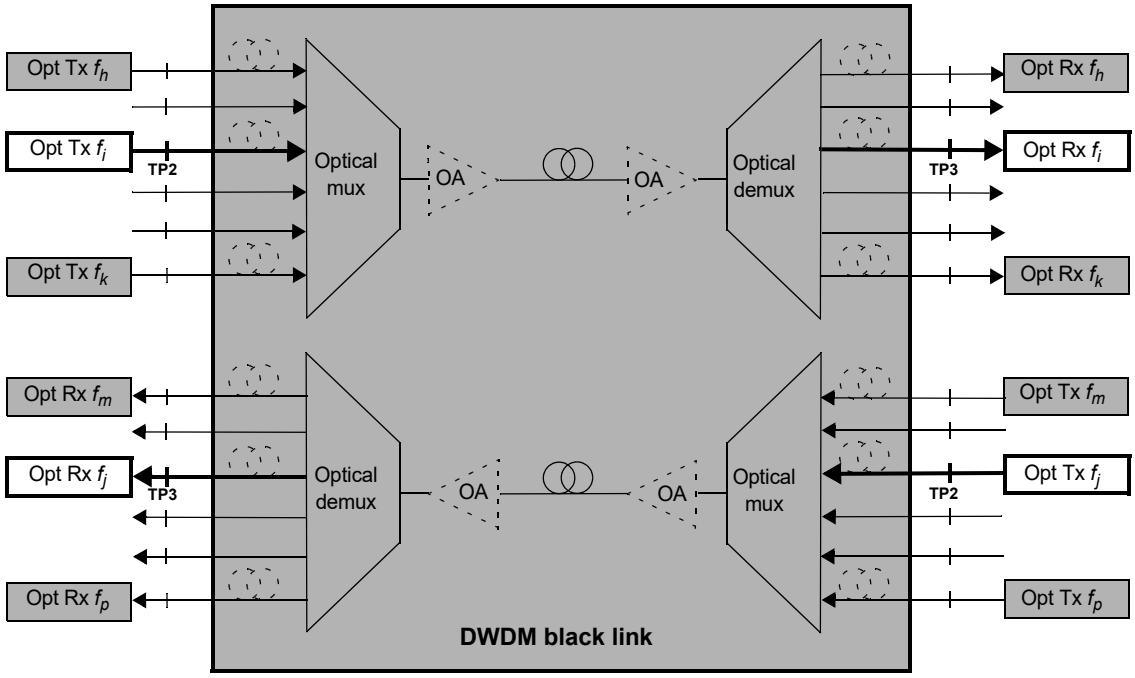

Figure 154A–1—DWDM black link example with one fiber per direction

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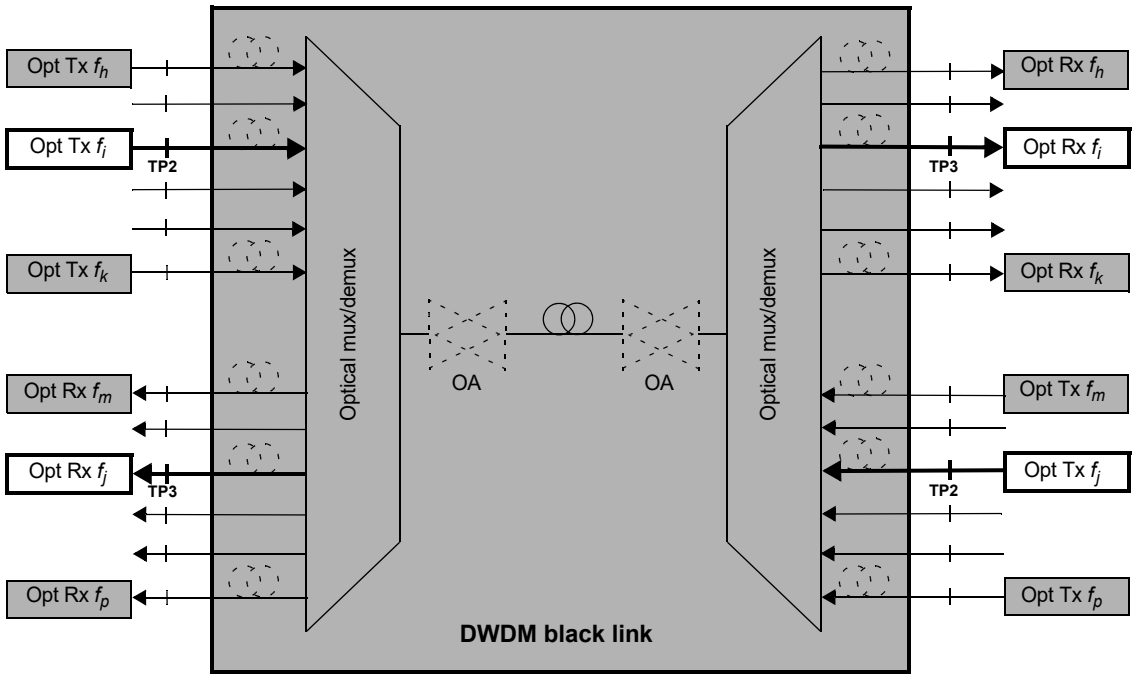

Figure 154A–2—DWDM black link example with one fiber for both directions

154A.2 Relationship between OSNR and average optical power

The DWDM black link requirements for the 100GBASE-ZR PMD are defined in Table 154–9. The relationship between OSNR and average optical power at TP3 defined in Table 154–9 is illustrated in Figure 154A–3. The operating ranges in Figure 154A–3 can be roughly divided into two areas, one where the OSNR is between 19.5 dB (12.5 GHz) and 35 dB (12.5 GHz) together with an average optical power at TP3 between 0 dBm and –16 dBm and a second range where the OSNR is equal to or larger than 35 dB (12.5 GHz) together with an average optical power at TP3 between 0 dBm and –27 dBm.

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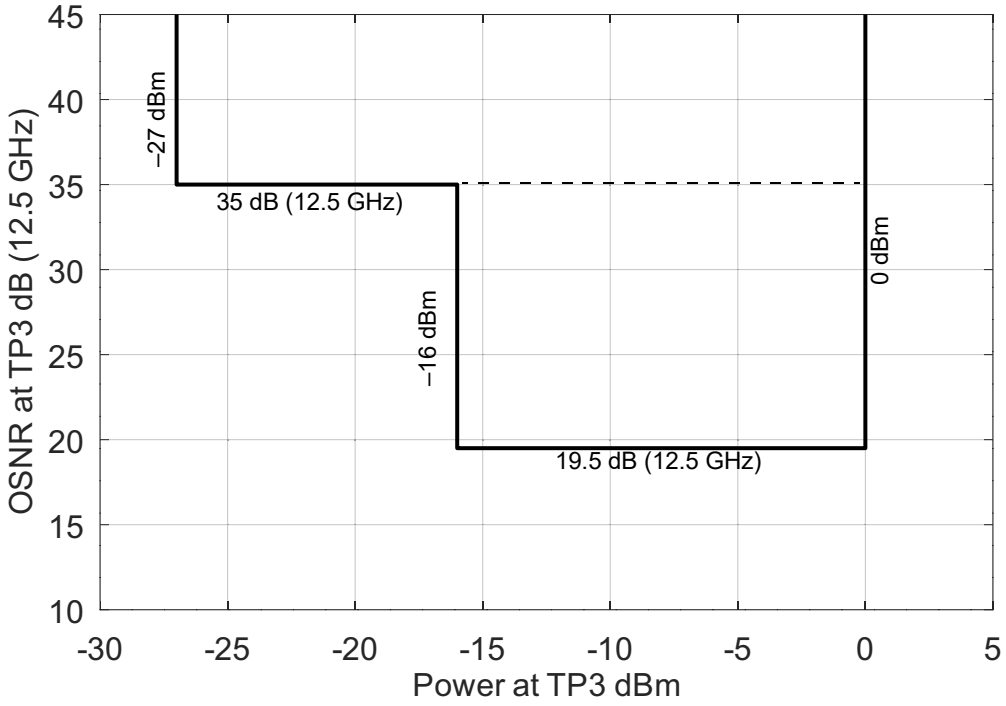

Figure 154A–3—100GBASE-ZR OSNR (TP3) requirements versus average receive power (TP3)

The area for OSNR at TP3 ≥ 35 dB (12.5 GHz) suggests DWDM black links not containing any optical amplifiers, because there is no or negligible reduction of OSNR across the DWDM black link from the minimum transmitter in-band OSNR at TP2 of 35 dB (12.5 GHz). The link performance in this range is generally loss limited.

On the other hand, the area for OSNR at TP3 between 19.5 dB (12.5 GHz) and 35 dB (12.5 GHz) suggests DWDM black links containing one or more optical amplifiers, causing a reduction of the minimum transmitter in-band OSNR at TP2 of 35 dB (12.5 GHz) to the value at TP3. The link performance in this range is generally OSNR limited.

The boundaries shown in Figure 154A–3 indicate the limits of OSNR and average power at TP3 that the DWDM black link should stay within to be compliant to the 100GBASE-ZR requirements. The boundaries also indicate the minimum requirements for a compliant 100GBASE-ZR receiver.

154A.3 Examples of DWDM black link applications with OSNR at TP3 between 19.5 dB (12.5 GHz) and 35 dB (12.5 GHz)

The DWDM black link designed for this region of operation will probably contain one of more optical amplifiers and the achievable distances across the multi-channel fiber between the optical multiplexer and demultiplexer will be determined by the ability of these amplifiers to compensate for the loss of this fiber, while simultaneously meeting the DWDM black link requirements listed in Table 154–9.

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For any application over any DWDM black link distance and any number of channels up to 48 the optical amplifier needs to be designed to achieve the DWDM black link output power and OSNR parameter values at TP3 from the DWDM black link input parameter values at TP2, both listed in Table 154A–1. This implies that the channel input power range of –8 dBm to 0 dBm, attenuated by all of the passive components in the DWDM black link, should be amplified to a channel output range of –16 dBm to 0 dBm.

Specifically in an example application of 40 channels over 80 km of single-mode fiber with a loss coefficient of 0.25 dB/km, optical multiplexer and demultiplexer loss of 6 dB each and 2 dB loss for patching panels (between TP2 and TP3), this means that optical amplifiers need to be designed to allow a total DWDM black link passive loss of 34 dB.

This suggests an amplification between 18 dB per DWDM channel (for maximum difference between DWDM black link input and output power of 16 dB) and 42 dB per DWDM channel (for a maximum difference between DWDM black link input and output power of –8 dB).

NOTE—Suitable attenuation coefficients for optical fiber cables operating in the 1550 nm window can be found in Appendix I of ITU-T G.695. For loss calculations an average value of 0.25 dB/km is used in this annex. The loss values for optical multiplexer, optical demultiplexer, and patch panels used in the examples in this annex are conservative. Other loss values may lead to other potential distances.

Table 154A–1—DWDM black link channel power and OSNR requirements for OSNR at TP3 between 19.5 dB (12.5 GHz) and 35 dB (12.5 GHz)

Description	Value	Unit
Average channel power at TP2	–8 to 0	dBm
OSNR at TP2 (min)	35	dB (12.5 GHz)
Average channel power at TP3	–16 to 0	dBm
OSNR at TP3	19.5 to 35	dB (12.5 GHz)

154A.4 Example of DWDM black link applications with OSNR at TP3 greater than or equal to 35 dB (12.5 GHz)

The DWDM black link designed for this region of operation will not cause a reduction of the OSNR from input to output and therefore it can be assumed to be completely passive.

The achievable distances across the fiber between TP2 and TP3 will be determined by the total loss from TP2 to TP3, minus the total loss of the optical multiplexer and demultiplexer and the loss of potentially present patch panel connectors. The maximum allowable loss from TP2 to TP3 can be calculated from the difference between the minimum average receive power (at TP3) and the minimum transmitter average channel output power (at TP2), which is 19 dB.

In Table 154A–2, Table 154A–3, Table 154A–4, and Table 154A–5, four examples of DWDM black link applications with OSNR at TP3 greater than or equal to 35 dB (12.5 GHz), with associated assumptions for losses of optical multiplexer/demultiplexer, patch panel, and cabled fiber loss coefficient, are provided. Different assumptions will give different results of achievable transmission distances. The example in Table 154A–5 is a separate case, because the DWDM black link does not contain an optical multiplexer or optical demultiplexer, so that the fiber plant inside the DWDM black link is not a multi-channel link, but rather a single channel link, and therefore a conventional point-to-point Ethernet application where the PMDs at TP2 and TP3 are connected only via a combination of fiber and optical connectors.

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Table 154A–2—40 channel example DWDM black link application with OSNR (TP3) ≥ 35 dB (12.5 GHz)

Description	Value	Unit
Available loss budget TP2 to TP3	19	dB
Allocation for loss of 40 channel optical multiplexer	6	dB
Allocation for loss of 40 channel optical demultiplexer	6	dB
Allocation for loss of patch panels	2	dB
Remaining loss available for multi-channel fiber plant	5	dB
Potential distance for 0.25 dB/km cabled fiber attenuation coefficient	20	km

Table 154A–3—16 channel example DWDM black link application with OSNR (TP3) ≥ 35 dB (12.5 GHz)

Description	Value	Unit
Available loss budget TP2 to TP3	19	dB
Allocation for loss of 16 channel optical multiplexer	4	dB
Allocation for loss of 16 channel optical demultiplexer	4	dB
Allocation for loss of patch panels	2	dB
Remaining loss available for multi-channel fiber plant	9	dB
Potential distance for 0.25 dB/km cabled fiber attenuation coefficient	36	km

Table 154A–4—4 channel example DWDM black link application with OSNR (TP3) ≥ 35 dB (12.5 GHz)

Description	Value	Unit
Available loss budget TP2 to TP3	19	dB
Allocation for loss of 4 channel optical multiplexer	2	dB
Allocation for loss of 4 channel optical demultiplexer	2	dB
Allocation for loss of patch panels	2	dB
Remaining loss available for multi-channel fiber plant	13	dB
Potential distance for 0.25 dB/km cabled fiber attenuation coefficient	52	km

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Table 154A–5—1 channel example DWDM black link application with OSNR (TP3) ≥ 35 dB (12.5 GHz)

Description	Value	Unit
Available loss budget TP2 to TP3	19	dB
Allocation for loss of patch panels	2	dB
Remaining loss available for fiber plant	17	dB
Potential distance for 0.25 dB/km cabled fiber attenuation coefficient	68	km

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